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Signetics

TTL Data Manual

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Data Manual

Logic Products

TTL Products

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Signetics would like to thank you for your interest in our products. This manual contains information and specifications on SSI, MSI, and LSI products in Standard Product families such as 7400, 74S, 74LS, and 8T. Signetics offers a broad range of Logic Products besides those described in this data manual. Newer Random Logic families such as 74HC/HCT and 74F are contained in other data manuals. 10K/100K ECL, 4000 Series CMOS, PROM/RAM, and Application Specific Product specifications are contained in separate data manuals.

This manual also includes:

- updated Technology and Function Cross Reference Guides
- TTL User's Guide
- an expanded chapter on SMD Technology
- updated package information.

All reference to military products has been deleted, specifically, to reflect government restrictions imposed via Revision C of MIL-STD 883, including the general provisions of Paragraph 1-2. Specifications for Signetics military products are available in the Signetics Military Products Data Manual.

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Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Logic Products

TECHNOLOGY SELECTION GUIDE

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
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00	Quad 2-Input NAND Gate	A	A	A	A	A	A
01	Quad 2-Input NAND Gate, OC						
02	Quad 2-Input NOR Gate	A	A	A	A	Q1 84	Q1 84
03	Quad 2-Input NAND Gate	A	A				
04	Hex Inverter	A	A	A	A	Q2 84	Q2 84
05	Hex Inverter, OC	A	A	A			
06	Hex Inverter Buffer/Drivers, OC	A					
07	Hex Buffer/Driver, OC	A					
08	Quad 2-Input	A	A	A	A	Q2 84	Q2 84
09	Quad 2-Input AND Gate, OC			A			
10	Triple 3-Input NAND Gate	A	A	A	A	Q2 84	Q2 84
11	Triple 3-Input AND Gate	A	A	A	A	Q2 84	Q2 84
13	Dual 4-Input NAND Schmitt Trigger	A		A	A		
14	Hex Schmitt Trigger	A		A	A	Q2 84	Q2 84
16	Hex Inverter Buffer/Driver, OC	A					
17	Hex Buffer/Driver, OC	A					
20	Dual 4-Input NAND Gate	A	A	A	A	Q2 84	Q2 84
21	Dual 4-Input AND Gate	A	A				
25	Dual 4-Input NOR with Strobe	A					
26	Quad 2-Input NAND Gate, OC	A		A			
27	Triple-3-Input NOR Gate	A		A	A	Q1 84	Q1 84
28	Quad 2-Input NOR Buffer	A					
30	8-Input NAND Gate	A		A	A		
32	Quad 2-Input OR Gate	A	A	A	A	Q2 84	Q2 84
33	Quad 2-Input NOR Buffer	A		A			
37	Quad 2-Input NAND Buffer	A	A	A	A		
38	Quad 2-Input NAND Buffer, OC	A	A	A	A		
39	Quad 2-Input NAND Buffer, OC	A					
40	Dual 4-Input NAND Buffer	A	A	A	A		
42	BCD-to-Decimal Decoder	A		A		Q2 84	Q2 84
45	BCD-to-Decimal Decoder/Driver, OC	A					
50	Expandable Dual 2-Wide 2-Input AOI Gate	A					
51	Dual 2-Wide 2-Input AOI Gate	A	A	A	A		
54	4-Wide 2-Input AOI Gate			A			
64	4-2-3-2 Input AOI Gate		A		A		
73	Dual J-K Master-Slave Flip-Flop	A		A		Q1 84	Q1 84
74	Dual D-Type Positive Edge-Triggered Flip-Flop	A	A	A*	A	A	A
75	Quad Bistable Latch	A		A		Q1 84	Q1 84
76	Dual J-K Master-Slave Flip-Flop	A		A			
83	4-Bit Binary Full Adder, Ripple Carry	A		A*	1H 86		
85	4-Bit Magnitude Comparator	A	A	A	A	Q2 84	Q2 84
86	Quad 2-Input Exclusive-OR Gate	A	A	A	A	A	A
90	Decade Ripple Counter	A		A			
91	8-Bit Shift Register	A					
92	Divide-by-12 Counter	A		A			

*A Version. **B Version

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Technology Selection Guide

TECHNOLOGY SELECTION GUIDE (Continued)

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
93	4-Bit Binary Ripple Counter	A		A			
94	4-Bit PISO Shift Register	A					
95	4-Bit Shift Register	A		A**			
96	5-Bit Shift Register	A		A			
107	Dual J-K Master-Slave Flip-Flop	A		A		Q1 84	Q1 84
109	Dual J-K Positive Edge-Triggered Flip-Flop	A		A*	A	Q1 84	Q1 84
112	Dual J-K Negative Edge-Triggered Flip-Flop		A	A	1H 86	Q2 84	Q2 84
113	Dual J-K Negative Edge-Triggered Flip-Flop		A	A	1H 86		
114	Dual J-K Negative Edge-Triggered Flip-Flop				2H 84		
116	Dual 4-Bit Latch with Clear	A					
121	Monostable Multivibrator	A					
123	Retriggerable Monostable Multivibrator	A				A	A
125	Quad 3-State Buffer	A		A	A		
126	Quad 3-State Buffer	A		A	A		
128	Quad 2-Input NOR Buffer	A					
132	Quad Schmitt Trigger	A		A	A	A	A
133	13-Input NAND Gate		A				
134	12-Input NAND Gate, 3-State		A				
135	Quad Exclusive-OR/NOR Gate		A				
136	Quad Exclusive-OR, OC			A			
138	3-to-8 Decoder/Demultiplexer		A	A	A	Q1 84	Q1 84
139	Dual 2-to-4 Decoder/Demultiplexer		A	A	A	A	A
140	Dual 4-Input NAND Line Driver		A				
145	BCD-to-Decimal Decoder/Driver, OC	A					
147	10-to-4 Priority Encoder	A				Q1 84	Q1 84
148	8-to-3 Priority Encoder	A			A		
150	16-to-6 Multiplexer	A					
151	8-to-1 Multiplexer	A	A	A	A	Q1 84	Q1 84
153	Dual 4-to-1 Multiplexer	A	A	A	A	A	A
154	4-to-16 Decoder/Demultiplexer	A		A		A	A
155	Dual 2-to-4 Decoder/Demultiplexer	A		A			
156	Dual 2-to-4 Decoder/Demultiplexer, OC	A		A			
157	Quad 2-to-1 Multiplexer	A	A	A	A	A	A
158	Quad 2-to-1 Multiplexer	A	A	A	A	A	A
160	Synchronous 4-Bit Decade Counter	A		A*	1H 86	Q2 84	Q2 84
161	Synchronous 4-Bit Binary Counter	A		A*	A*	Q2 84	Q2 84
162	Synchronous 4-Bit Decade Counter			A*	1H 86	Q2 84	Q2 84
163	Synchronous 4-Bit Binary Counter	A		A*	A*	Q2 84	Q2 84
164	8-Bit SIPO Shift Register	A		A	1H 86	A	A
165	8-Bit PISO Shift Register	A				A	A
166	8-Bit PISO Shift Register	A			A	Q1 84	Q1 84
168	Decade Up/Down Counter		A	A*	1H 86		
169	Binary Up/Down Counter		A	A*	1H 86		
170	4 x 4 Register File, OC	A		A			
172	16-Bit Multiple Port Register File		A				
173	Quad D-Type Flip-Flop, 3-State	A		A		Q2 84	Q2 84
174	Hex D-Type Flip-Flop with Clear	A	A	A	A	Q2 84	Q2 84
175	Quad D-Type Flip-Flop	A	A	A	A	Q1 84	Q1 84
180	8-Bit Odd/Even Parity Checker	A					
181	4-Bit Arithmetic Logic Unit	A	A	A	A		

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Technology Selection Guide

TECHNOLOGY SELECTION GUIDE (Continued)

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
182	Look-Ahead Generator		A		A		
189	64-Bit Random Access Memory, 3-State				1H 86		
190	Decade Up/Down Counter	A			1H 86	Q2 84	Q2 84
191	Binary Up/Down Counter	A		A	1H 86	Q2 84	Q2 84
192	Decade Up/Down Counter	A		A	1H 86	Q1 84	Q1 84
193	4-Bit Binary Up/Down Counter	A		A	1H 86	Q2 84	Q2 84
194	4-Bit Bidirectional Shift Register	A	A	A	A	A	A
195	4-Bit Parallel-Access Shift Register	A	A	A	A	A	A
197	Presetable Binary Counter			A			
198	8-Bit Bidirectional Universal Shift Register				1H 86		
199	8-Bit Universal Shift Register	A			1H 86		
221	Dual Monostable Multivibrator	A				P	P
225	FIFO		A				
238	1-of-8 Decoder/Demultiplexer, True/Inverting					Q1 84	Q1 84
240	Octal 3-State Buffer				A	A	A
241	Octal 3-State Buffer		A	A	A	A	A
242	Quad Bus Transceiver		A	A	A	Q1 84	Q1 84
243	Quad Bus Transceiver		A	A	A	Q1 84	Q1 84
244	Octal 3-State Buffer		A	A	A	A	A
245	Octal Bus Transceiver		A	A	A	A	A
251	8-to-1 Multiplexer, 3-State		A	A	1H 86	A	A
253	Dual 4-to-1 Multiplexer, 3-State		A	A	A	A	A
256	Dual 4-Bit Addressable Latch			A	A		
257	Quad 2-to-1 Multiplexer, 3-State		A	A*	A	A	A
258	Quad 2-to-1 Multiplexer, 3-State			A*	A		
259	8-Bit Addressable Latch			A	A	Q2 84	Q2 84
260	Dual 5-Input NOR Gate		A	A	A		
266	Quad Exclusive-OR, OC			A			
269	8-Bit Up/Down Counter			A	A		
273	Octal D Flip-Flop		A	A	A	Q1 84	Q1 84
279	Quad S-R Latch	A					
280	9-Bit Odd/Even Parity Generator/Checker		A		A*	A	A
283	4-Bit Adder			A	A		
290	Decade Counter			A			
293	4-Bit Binary Counter			A			
295	4-Bit Shift Register, 3-State			A**			
297	Digital Phase-Locked Loop Filter					Q1 84	Q1 84
298	Quad 2-Port Register	A		A	A		
299	Octal Shift/Storage Register, 3-State				1H 86	Q1 84	Q1 84
322	Octal Shift/Storage Register				1H 86		
323	Octal Shift/Storage Register				1H 86		
350	4-Bit Four-Way Shifter		A		A		
352	Dual 4-to-1 Multiplexer, Inverting			A	A		
353	Dual 4-to-1 Multiplexer, Inverting, 3-State			A	A		
354	8-Input Multiplexer/Register, 3-State					Q2 84	Q2 84
356	8-Input Multiplexer/Register, 3-State					Q2 84	Q2 84
363	Octal Latch, 3-State, MOS Compatible Outputs			A			
364	Octal D Flip-Flop, 3-State, MOS Compatible Outputs			A			
365	Hex Buffer with Common Enable, 3-State	A		A*	A	Q3 84	Q3 84
366	Hex Inverter with Common Enable, 3-State	A		A*	A	Q1 84	Q1 84

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Technology Selection Guide

TECHNOLOGY SELECTION GUIDE (Continued)

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
367	Hex Buffer, 4-Bit and 2-Bit, 3-State	A		A*	A	Q1 84	Q1 84
368	Hex Inverter, 4-Bit and 2-Bit, 3-State	A		A*	A	Q1 84	Q1 84
373	Octal Latch, 3-State		A	A	A	Q1 84	Q1 84
374	Octal D Flip-Flop, 3-State		A	A	A	Q1 84	Q1 84
375	Quad Latch			A			
377	Octal D-Type Flip-Flop with Enable			A	A	A	A
378	Hex D Flip-Flop with Enable			A	A		
379	Quad D Flip-Flop with Enable				A		
381	4-Bit Arithmetic Logic Unit				A		
382	4-Bit Arithmetic Logic Unit				A		
384	8-Bit Serial/Parallel Two's Complement Multiplier				1H 86	P	P
385	Quad Serial Adder/Subtractor				1H 86		
390	Dual Decade Ripple Counter			A		Q1 84	Q1 84
393	Dual Binary Ripple Counter			A			
395	4-Bit Cascadable Shift Register, 3-State			A	A		
398	4-Bit Flip-Flop, True/Complement				A		
399	4-Bit Flip-Flop, True/Complement				A		
412	Octal Multi-Mode Buffered Latch, 3-State				1H 86		
423	Dual Retriggerable Monostable Multivibrator					P	P
432	Octal Multi-Mode Buffered Latch				1H 86		
445	BCD-to-Decimal Decoder with 7V Output			A			
455	Octal Buffer with Parity Generator Checker				A		
456	Octal Buffer with Parity Generator Checker				A		
490	Dual Decade Ripple Counter			A			
521	8-Bit Comparator				A		
524	8-Bit Register Comparator				1H 86		
533	Inverting Octal D Latch, 3-State				A	Q1 84	Q1 84
534	Octal D Flip-Flop, 3-State				A	A	A
537	1-of-10 Decoder, 3-State				1H 86		
538	1-of-8 Decoder, 3-State				1H 86		
539	Dual 1-of-4 Decoder, 3-State				1H 86		
540	Octal Driver			A	A	Q1 84	Q1 84
541	Octal Driver			A	A	Q1 84	Q1 84
543	Octal Transparent Bidirectional Latch				1H 86		
544	Octal Transparent Bidirectional Latch				1H 86		
545	Octal Bus Transceiver				A		
547	Octal Decoder/DeMUX with Address Latches and Acknowledge				1H 86		
548	Octal Decoder/DeMUX with Acknowledge				1H 86		
563	Octal Transparent Inverting Latch, 3-State				1H 86	A	A
564	Octal D Type Inverting Flip-Flop, 3-State				1H 86	Q1 84	Q1 84
568	BCD Decade Up/Down Synchronous Counter			A*	1H 86		
569	4-Bit Binary Up/Down Synchronous Counter			A*	1H 86		
573	Octal Transparent Latch, 3-State				1H 86	A	A
574	Octal D Type Flip-Flop, Positive Edge-Triggered, 3-State				1H 86	Q2 84	Q2 84
579	8-Bit Up/Down Counter, Common I/O				A		
588	GPIO Compatible Octal Transceiver				A		
595	8-Bit Shift Register with Output Latch				1H 86		
596	8-Bit Shift Register with Output Latch						
597	8-Bit Shift Register with Input Latch				1H 86		
598	8-Bit Shift Register with Input Latch				1H 86		

*A Version. **B Version

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Technology Selection Guide

TECHNOLOGY SELECTION GUIDE (Continued)

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
604	Dual 8-Bit Latch				A		
605	Dual 8-Bit Latch				A		
620	Octal Transceiver, 3-State			A	A		
621	Octal Transceiver, OC			A	A		
622	Octal Transceiver, 3-State			A	A		
623	Octal Transceiver, OC			A	A		
630	Memory Error Detector/Corrector, 3-State				1H 86		
631	Memory Error Detector/Corrector				1H 86		
640	Octal Bus Transceiver, 3-State			A	A	A	A
640-1	Octal Bus Transceiver, 3-State, 48mA Sink Capability			A			
641	Octal Bus Transceiver, OC			A	A		
641-1	Octal Bus Transceiver, OC, 48mA Sink Capability			A			
642	Octal Bus Transceiver, OC			A	A		
642-1	Octal Bus Transceiver, OC, 48mA Sink Capability			A			
643	Octal True/Inverting Transceiver, 3-State					A	A
645	Octal Bus Transceiver, 3-State			A			
645-1	Octal Bus Transceiver, 3-State, 48mA Sink Capability			A			
646	Octal Bus Transceiver with Registers				1H 86	P	P
647	Octal Bus Transceiver with Registers				1H 86		
648	Octal Bus Transceiver with Registers				1H 86	P	P
649	Octal Bus Transceiver with Registers				1H 86		
651	Octal Bus Transceiver and Register, Inverting, 3-State				2H 86		
652	Octal Bus Transceiver and Register, Non-Inverting, 3-State				2H 86		
653	Octal Bus Transceiver and Register, Inverting, OC				2H 86		
654	Octal Bus Transceiver and Register, Non-Inverting, OC				2H 86		
655	Octal Buffer with Parity Generator-Checker				A*		
656	Octal Buffer with Parity Generator-Checker				A*		
657	Octal Bus Transceiver with Parity Generator-Checker				A		
670	4 x 4 Register File, 3-State			A		Q2 84	Q2 84
673	16-Bit SIPO Shift Register				1H 86		
674	16-Bit SIPO Shift Register				1H 86		
675	16-Bit SIPO Shift Register with Serial Output Capability				1H 86		
676	16-Bit SIPO Shift Register with Parallel Output Capability				1H 86		
688	8-Bit Magnitude Comparator					A	A
764	Dual Port RAM Controller with DRAM Refresh				1H 86		
765	Dual Port RAM Controller without Latch				1H 86		
779	8-Bit Counter				A		
784	8-Bit Serial Multiplier and Adder/Subtractor				1H 86		
821	10-Bit Register, Non-Inverting				1H 86		
822	10-Bit Register, Inverting				1H 86		
823	9-Bit Register, Non-Inverting				1H 86		
824	9-Bit Register, Inverting				1H 86		
825	8-Bit Register, Non-Inverting				1H 86		
826	8-Bit Register, Inverting				1H 86		
827	10-Bit Buffer, Non-Inverting				1H 86		
828	10-Bit Buffer, Inverting				1H 86		
841	10-Bit Latch, Non-Inverting				1H 86		
842	10-Bit Latch, Inverting				1H 86		
843	9-Bit Latch, Non-Inverting				1H 86		
844	9-Bit Latch, Inverting				1H 86		

*A Version. **B Version

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Technology Selection Guide

TECHNOLOGY SELECTION GUIDE (Continued)

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
845	8-Bit Latch, Non-Inverting				1H 86		
846	8-Bit Latch, Inverting				1H 86		
861	10-Bit Transceiver, Non-Inverting				1H 86		
862	10-Bit Transceiver, Inverting				1H 86		
881	Arithmetic Logic Unit/Function Generator				1H 86		
882	32-Bit Look-Ahead Carry Generator				1H 86		
1240	Octal Buffer, 3-State, Light Load 'F240				A		
1241	Octal Buffer, 3-State, Light Load 'F241				A		
1242	Quad Transceiver, Inverting, 3-State, Light Load 'F242				A		
1243	Quad Transceiver, 3-State, Light Load 'F243				A		
1244	Octal Buffer, 3-State, Light Load 'F244				A		
1245	Octal Bus Transceiver, 3-State, Light Load 'F245				1H 86		
3037	Quad 2-Input 30Ω Transmission Line Driver, NINV				A		
3038	Quad 2-Input 30Ω Transmission Line Driver, Non-Inverting, OC				A		
3040	Dual 4-Input 30Ω Transmission Line Driver, Non-Inverting				A		
30240	Octal 30Ω Transmission Line Driver, Inverting, OC				1H 86		
30244	Octal 30Ω Transmission Line Driver, Non-Inverting, OC				1H 86		
30245	Octal Transceiver, 30Ω Transmission Line Driver, Non-Inverting, OC				1H 86		
30640	Octal Transceiver, 30Ω Transmission Line Driver, Inverting, OC				1H 86		

*A Version. **B Version

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Logic Products

The Function Cross Reference Guide is provided for customer reference only. It does not represent all the devices available from Signetics' Logic Division.

The device number given is a base number. Check the Number Cross Reference Guide for the complete part number and availability.

GATES

FUNCTION	DEVICE NO.
Inverters	
Octal Inverter/Driver	30240
Octal Driver, Non-Inverting	30244
Octal Transceiver, Non-inverting	30245
Octal Transceiver, Inverting	30640
Hex Inverter	04
Hex Inverter, OC	05
Hex Inverter buffer/Driver, OC (30V)	06
Hex Inverter Schmitt Trigger	14
Hex Inverter Buffer/Driver, OC (15V)	16
Hex Inverter (15V to TTL Levels)	4049
Hex Inverter Unbuffered Outputs	4069UB
Hex Inverter Schmitt Trigger	40106
Dual Complementary Pair and Inverter, Unbuffered	4007UB
NAND	
Quad 2-Input	00
Quad 2-Input, OC	01
Quad 2-Input, OC	03
Quad 2-Input, OC	26
Quad 2-Input NAND Buffer	37
Quad 2-Input NAND Buffer, OC	38
Quad 2-Input NAND Driver, OC	3037
Quad 2-Input NAND Driver, OC	3038
Triple 3-Input	10
Dual 4-Input, Schmitt Trigger	13
Dual 4-Input	20
Dual 4-Input NAND Buffer	40
Dual 4-Input NAND Driver	140
Dual 4-Input NAND Driver	3040
8-Input	30
Quad 2-Input, Schmitt Trigger	132
Quad 2-Input	4011
Quad 2-Input, Unbuffered Outputs	4011UB
Dual 4-Input	4012
Triple 3-Input	4013
8-Input	4068
12-Input	134
13-Input	133
AND	
Quad 2-Input	08
Quad 2-Input	4081
Quad 2-Input, OC	09
Triple 3-Input	11

FUNCTION	DEVICE NO.
AND (Continued)	
Dual 4-Input	21
Dual 4-Input	4082
NOR	
Quad 2-Input	02
Quad 2-Input	28
Quad 2-Input	128
Quad 2-Input	4001
Quad 2-input, Unbuffered Output	4001UB
Quad 2-Input, OC	33
Triple 3-Input	27
Triple 3-Input	4025
Dual 3-input, with Inverter	4000
Dual 4-input	4002
Dual 4-Input, with Strobe	25
Dual 5-Input	260
8-Input	4078
OR	
Quad 2-Input	32
Quad 2-Input	4071
Triple 3-Input	4075
Dual 4-Input	4072
Exclusive-OR	
Quad	86
Quad	4030
Quad, OC	136
Quad	4070
Quad Exclusive OR-NOR	135
Exclusive-NOR	
Quad	4077
Quad, OC	266
Quad Exclusive OR-NOR	135
Combination gates	
Expandable Dual 2-Wide 2-Input AND-OR-Invert	50
Dual 2-Wide 2-Input AND-OR-Invert	51
2-Wide 2-Input AND-OR-Invert	54
4-2-3-2 Input AND-OR-Invert	64
Dual 3-Input NOR Gate with Inverter	4000
Dual Complementary Pair and Inverter, Unbuffered	4007UB
Dual 2-Wide 2-Input AND-OR-Invert	4085
4-Wide 2-Input AND-OR-Invert	4086

Function Cross Reference Guide

DUAL FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	CLEAR
D	74	┌	LOW	LOW
D	4013	┌	HIGH	HIGH
JK	73	└		LOW
JK	76	└	LOW	LOW
JK	107	└		LOW
JK	109	┌	LOW	LOW
JK	112	└	LOW	LOW
JK	113	└	LOW	LOW
JK	114	└	LOW	LOW
JK	4027	┌	HIGH	HIGH

Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	RESET (LEVEL)	CLOCK EDGE	OUTPUT
Quad D	173	HIGH	┌	True
Quad D	175	LOW	┌	True, Comp
Quad D	40175	LOW	┌	True
Quad D with Enable	379		┌	True, Comp
Quad D, 3-State	4079	HIGH	┌	True
Quad D, 3-State	8T10	HIGH	┌	True
Hex D	174	LOW	┌	True
Hex D with Enable	378		┌	True
Octal D	273	LOW	┌	True
Octal D, 3-State	374		┌	True
Octal D with Enable	377		┌	True
Octal D, 3-State	534		┌	Comp
Octal D, 3-State	564		┌	Comp
Octal D, 3-State	574		┌	True
Octal D, 3-State	40374		┌	True
Octal D, 3-State	8TS806		┌	True
Octal D, 3-State	8TS808		┌	Comp
Octal D, 3-State, MOS Compatible Outputs	364		┌	True

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY*	CLOCK
Quad 2 Port	298	4 x 2		2D (mux)	└
Quad 2 Port	398	4 x 2		2D (mux)	┌
Quad 2 Port	399	4 x 2		2D (mux)	┌
10-Bit, Non-Inverting	821	10		2D	┌
10-Bit, Inverting	822	10		2D	┌
9-Bit, Non-Inverting	823	9		2D	┌
9-Bit, Inverting	824	9		2D	┌
8-Bit, Non-Inverting	825	8		2D	┌
8-Bit, Inverting	826	8		2D	┌
Register File, OC	170	4 x 4		4A	└
Multiple Port Register File, 3-State	172	16		3D (mux)	└
4 x 4 Register File, 3-State	670	4 x 4		4A	└
16 x 5 FIFO, 3-State	225	5		5S	┌
4 x 16 FIFO	40105	4	D	4S	┌

*D = D type input, A = Asynchronous data input, S = Synchronous data input

Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

Function Cross Reference Guide

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Serial In/Serial Out Shift Register	91	8	D _A and D _B		┌
Serial In/Serial Out Shift Right	4006	(2 x 4)(2 x 5)	D		└
Serial In/Serial Out Shift Right	4031	64	D _A + D _B		┌
Dual Serial In/Serial Out Shift Right, 3-State	4517	(4 x 16)	D		┌
Quad Serial In/Serial Out Shift Right	4731	64	D		└
Serial In/Serial Out Variable Length Shift Right	4557	1 to 64	D _A + D _B		┌ and └
Serial In/Serial Out Shift Right, 3-State	4094	8	D		┌
Parallel In/Serial Out	674	16	D	16S	└
Serial In/Serial/Parallel Out	675	16	D		└
Serial/Parallel In/Serial Out	676	16	D	16S	└
Parallel/Serial In/Serial Out Shift Right	94	4	D	2 x 4A (mux)	┌
Parallel/Serial In/Serial Out Shift Right	165	8	D	8A	┌
Parallel/Serial In/Serial Out Shift Right	166	8	D	8S	┌
Parallel/Serial In/Serial Out Shift Right	195	4	J, \bar{K}	4S	┌
Parallel/Serial In/Serial Out Shift Right	199	8	J, K	8S	┌
Parallel/Serial In/Serial Out Shift Right	597	8	D	8S	┌
Parallel/Serial In/Serial Out Shift Right	4014	8	D	8S	┌
Parallel/Serial In/Serial Out Shift Right	4021	8	D	8A	┌
Parallel/Serial In/Serial Out Shift Right	8274	10	D	10S	└
Parallel/Serial In/Serial Out Shift Right, 3-State	598	8	S ₀ , S ₁	8S	┌
Serial In/Parallel Out Shift Right	164	8	D ₀ and D ₁		┌
Serial In/Parallel Out Shift Right, with Reset	8273	10	D		└ or ┌
Dual Serial In/Parallel Out Shift Right	4015	4	D		┌
Serial In/Parallel Out, 3-State	595	8	D		┌
Serial In/Parallel Out, OC	596	8	D		┌
Serial In/Parallel Out	673	16	D		└
Parallel In/Serial In/Parallel Out Shift Right	95	4	D	5A	└
Parallel In/Serial In/Parallel Out Shift Right	96	5	D	5A	┌
Parallel In/Serial In/Parallel Out Shift Right	40195	4	J, \bar{K}	4S	┌
Parallel In/Serial In/Parallel Out Shift Right	8271	4	D	4S	└
Parallel In/Serial In/Parallel Out Shift Right	82S71	4	D	4S	└
Parallel In/Serial In/Parallel Out Shift Right	4035	4	J, \bar{K}	4S	┌
Parallel In/Serial In/Parallel Out Shift Right, 3-State	295	4	D	4S	└
Parallel In/Serial In/Parallel Out Shift Right, 3-State	395	4	D	4S	└
Parallel In/Serial In/Parallel Out Shift Right, 3-State	322	8	D ₀ + D ₁	8S (I/O)	┌
Parallel In/Serial In/Parallel Out Bidirectional	194	4	Dr, D _L	4S	┌
Parallel In/Serial In/Parallel Out Bidirectional	198	8	Dr, D _L	8S	┌
Parallel In/Serial In/Parallel Out Bidirectional	40194	4	Dr, D _L	4S	┌
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	299	8	Dr, D _L	8S	┌
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	323	8	Dr, D _L	8S (I/O)	┌
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	40194	4	Dr, D _L	4S	┌
4-Bit Shifter, 3-State	350	4		4A	

S = Synchronous, A = Asynchronous

Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

Function Cross Reference Guide

LATCHES

FUNCTION	DEVICE NUMBER	COMMON CLEAR (LEVEL)	ENABLE INPUT (LEVEL)	OUTPUT
Quad D	75		2 (H)	True, Comp
Quad D	375		2 (H)	True, Comp
Quad D	4042		2 (H)	True
Quad SR	279			True
Quad SR, 3-State	4043			True
Quad SR, 3-State	4044			True
Dual 4-Bit Transparent	116	LOW	2 (L)	True
Dual 4-Bit Addressable	256	LOW	1 (L)	True
Dual 4-Bit, Strobed	4508	HIGH	1 (L)	True
Dual 8-Bit	604			True
Dual 8-Bit	605			True
6-Bit (2-Bit and 4-Bit)	8T3404		1 (L)	Comp
8-Bit Addressable	259	LOW	1 (H)	True
8-Bit Addressable	4724	HIGH	1 (L)	True
8-Bit Addressable	9334	LOW	1 (L)	True
8-Bit, Non-Inverting	845	LOW	1 (H)	True
8-Bit, Inverting	846	LOW	1 (H)	Comp
9-Bit, Non-Inverting	843	LOW	1 (H)	True
9-Bit, Inverting	844	LOW	1 (H)	Comp
10-Bit, Non-Inverting	841		1 (H)	True
10-Bit, Inverting	843		1 (H)	Comp
Octal, 3-State	373		1 (H)	True
Octal Inverting, 3-State	533		1 (H)	Comp
Octal Transparent, Bidirectional	543		4 (L)	True
Octal Transparent, Bidirectional	544		4 (L)	Comp
Octal Transparent, Inverting, 3-State	563		1 (H)	Comp
Octal Transparent, 3-State	573		1 (H)	True
Octal Transparent, 3-State	40373		1 (H)	True
Octal, 3-State with MOS Compatible Outputs	363		1 (H)	True
Multimode Buffered	432	LOW		Comp

Function Cross Reference Guide

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE INPUT (LEVEL)	SELECT INPUTS	OUTPUT
Quad 2-Input	157	1 (L)	1	True
Quad 2-Input	158	1 (L)	1	True
Quad 2-Input	298	Clocked \overline{L}	1	True, Latched
Quad 2-Input	398	1 (H)	1	True, Comp Registered
Quad 2-Input	399	1 (H)	1	True, Registered
Quad 2-Input	4019		2	True
Quad 2-Input	4519		2	True
Quad 2-Input	8266		2	True
Quad 2-Input	9322	1 (L)	1	True
Quad 2-Input, 3-State	257		1	True
Quad 2-Input, 3-State	258		1	Comp
Quad 2-Input, OC	8234		2	Comp
Dual 4-Input	153	2 (L)	2	True, Comp
Dual 4-Input	352	2	2	Comp
Dual 4-Input	9309		2	True, Comp
Dual 4-Input	4539	2 (L)	2	True
Dual 4-Input, 3-State	253		2	True
Dual 4-Input, 3-State	353	2	2	Comp
8-Input	9312	1 (L)	3	True, Comp
8-Input	151	1 (L)	3	True, Comp
8-Input, 3-State	251		1	True, Comp
8-Input, 3-State	356	1 (L)	3	True, Latched
8-Input, 3-State	354	2 (L)	3	True, Latched
8-Input, 3-State	4512	1 (L)	3	True
16-Input	150	1 (L)	4	Comp

ANALOG MULTIPLEXERS/DEMULTIPLEXERS AND SWITCHES

FUNCTION	DEVICE NUMBER
Triple 2-Channel Mux/Demux	4053
Dual 4-Channel Mux/Demux	4052
8-Channel Mux/Demux	4051
16-Channel Mux/Demux	4066
Quad Bilateral Switches	4016

FUNCTION	DEVICE NUMBER
Quad Bilateral Switches	4067
Quad Bilateral Switches	4316
8-Channel Analog Mux/Demux with Latch	4351
Dual 4-Channel Analog Mux/Demux with Latch	4352
Triple 2-Channel Analog Mux/Demux with Latch	4353

Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

Function Cross Reference Guide

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PARALLEL ENTRY	PRESETTABLE	CLOCK EDGE
Asynchronous	90	2 x 5			┌
Asynchronous	290	2 x 5			┌
Asynchronous	92	2 x 6			┌
Asynchronous	93	2 x 8			┌
Asynchronous	293	2 x 8			┌
Asynchronous	176	2 x 5	A	X	┌
Asynchronous	177	2 x 8	A	X	┌
Asynchronous	197	2 x 8	A	X	┌
Asynchronous	290	2 x 5			┌
Asynchronous	293	2 x 8			┌
Asynchronous	390	2 x 5			┌
Asynchronous	393	2 x 8			┌
Asynchronous	490	2 x 5			┌
Asynchronous	4020	12			┌
Asynchronous	4024	7			┌
Asynchronous	4040	14			┌
Asynchronous with Oscillator	4060	14			┌
Synchronous	160	10	S	X	┐
Synchronous	161	16	S	X	┐
Synchronous	162	10	S	X	┐
Synchronous	163	16	S	X	┐
Synchronous	4256	16	A		┐ or ┌
Synchronous	40161	16	S	X	┐
Synchronous	40163	16	S	X	┐
Synchronous (Dual)	4518	10			┐ or ┌
Synchronous (Dual)	4520	16			┐ or ┌
Up/Down	168	10	S	X	┐
Up/Down	169	16	S	X	┐
Up/Down	190	10	A	X	┐
Up/Down	191	16	A	X	┐
Up/Down	192	10	A	X	┐
Up/Down	193	16	A	X	┐
Up/Down	269	8	S	X	┐
Up/Down	4029	10, 16	A	X	┐
Up/Down	4510	10	A	X	┐
Up/Down	4516	16	A	X	┐
Up/Down	40193	16	A	X	┐
Up/Down, 3-State	568	10	S	X	┐
Up/Down, 3-State	569	16	S	X	┐
Up/Down, 3-State	579	8	S(I/O)	X	┐
Up/Down, 3-State	779	8	S(I/O)	X	┐
Frequency Divider	4059	Programmable 3 to 15,999			┐
Johnson	4017	10			┐ or ┌
Johnson	4018	5	A		┐ or ┌
Johnson	4022	8			┐ or ┌

S = Synchronous A = Asynchronous

Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

Function Cross Reference Guide

TRI-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	125	True
Quad Buffer	126	True
Quad Bus Driver	8T09	
Quad Bus Transceiver	242	Comp
Quad Bus Transceiver	243	True
Quad Bus Transceiver	1242	Comp
Quad Bus Transceiver	1243	True
Quad Bus Transceiver	8T34	Comp
Quad Bus Transceiver	8T126	Comp
Quad Bus Transceiver	8T127	Comp
Quad Bus Transceiver	8T128	True
Quad Bus Transceiver	8T129	True
Hex Buffer	365	True
Hex Inverter	366	Comp
Hex Buffer, 4-Bit and 2-Bit	367	True
Hex Inverter, 4-Bit and 2-Bit	368	Comp
Hex Buffer	8T95	True
Hex Inverter	8T96	Comp
Hex Buffer	8T97	True
Hex Inverter	8T98	Comp
Hex Buffer	40097	True
Hex Buffer	40098	Comp
Octal Buffer	240	Comp
Octal Buffer	241	True
Octal Buffer	244	True
Octal Buffer	40240	Comp
Octal Buffer	40244	True
Octal Buffer	540	Comp
Octal Buffer	541	True
Octal Buffer	1240	Comp
Octal Buffer	1241	True
Octal Buffer	1244	True
Octal Buffer with Parity	455	Comp
Octal Buffer with Parity	456	True
Octal Buffer with Parity Generator-Checker	655	Comp
Octal Buffer with Parity Generator-Checker	656	True
Octal Transceiver	245	True
Octal Transceiver	545	True
Octal Transceiver with IEEE-488 Termination Resistors	588	True
Octal Transceiver	620	Comp
Octal Transceiver	622	Comp
Octal Transceiver	640, 640-1	Comp
Octal Transceiver	643	True, Comp
Octal Transceiver	645, 645-1	True
Octal Transceiver	651	Comp
Octal Transceiver	652	True
Octal Bus Transceiver with Parity Generator-Checker	657	True
Octal Transceiver	1245	True
Octal Transceiver	40245	True
Octal Transceiver	8T125	Comp
Octal Transceiver/Register	646	True
Octal Transceiver/Register	648	Comp
10-Bit Buffer	827	True
10-Bit Buffer	828	Comp
10-Bit Transceiver	861	True
10-Bit Transceiver	862	Comp

Function Cross Reference Guide

LEVEL TRANSLATORS

FUNCTION	DEVICE NUMBER
Hex Inverting Buffer, Up to 15V Input, TTL Level Output	4049
Hex Non-Inverting Buffer, Up to 15V Input, TTL Level Output	4050
Quad Voltage Translator, 3-State, TTL Input, 15V Output	4104
Quad Transceiver, MOS/CMOS to TTL	8T26
Quad Transceiver, MOS/CMOS to TTL	8T28

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	INPUT ENABLE (LEVEL)	INPUT/OUTPUT (LEVEL)
8-to-3	148	LOW	Active-LOW
8-to-3	4532	HIGH	Active-HIGH
10-to-4 (BCD)	147		Active-LOW

Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

DECODERS/DEMULPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE (LEVEL)	OUTPUT (LEVEL)
Dual 1 of 4	139	2 + 2	1 (L) + 1 (L)	4 (L) + 4 (L)
Dual 1 of 4	155	2	2 (L) + 1 (L), 1 (H)	4 (L) + 4 (L)
Dual 1 of 4	156	2	2 (L) + 1 (L), 1 (H)	4 (L) + 4 (L)
Dual 1 of 4	539	2 + 2	1 (L) + 1 (L)	4 (H) + 4 (H)
Dual 1 of 4	4555	2 + 2	1 (L) + 1 (L)	4 (H)
Dual 1 of 4	4556	2 + 2	1 (L) + 1 (L)	4 (L)
1 of 8	138	3	2 (L), 1 (H)	8 (L)
1 of 8	82S50	4 (BCD)		8 (L)
1 of 8	538	3	2 (L), 2 (H)	8 (H)
1 of 10	42	4 (BCD)		10 (L)
1 of 10, OC	45	4 (BCD)		10 (L)
1 of 10, OC	145	4 (BCD)		10 (L)
1 of 10, OC	445	4 (BCD)		10 (L)
1 of 10	537	4	1 (L), 1 (H)	10 (H)
1 of 10	4028	4 (BCD)		10 (H)
1 of 10	9301	4 (BCD)		10 (L)
1 of 10	82S52	4 (BCD)		10 (L)
1 of 16	154	4	2 (L)	16 (L)
1 of 16	4514	4 (Latched)	1 (L)	16 (H)
1 of 16	4515	4 (Latched)	1 (L)	16 (L)
BCD to 7 Segment Decoder/Driver	4511	4 (Latched)	1 (L)	7 (H)
BCD to 7 Segment Decoder/Driver	4543	4 (Latched)		7 (H)
Octal with Address Latches and Acknowledge	547	3	1 (L), 2 (H)	8 (L)
Octal with Acknowledge	548	3	2 (L), 2 (H)	8 (L)

Function Cross Reference Guide

BUFFERS, DRIVERS AND RECEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad 2-Input NAND Buffer	37	
Quad 2-Input NOR Buffer	128	
Quad Buffer	4041	True, Comp
Hex Buffer	4049	Comp
Hex Buffer	4050	True
Strobed Hex Inverter/Buffer	4502	Comp
Dual 4-Input NAND Buffer	40	
Dual 4-Input NAND Line Driver	140	
Dual 4-Input NAND Driver	3040	
Dual Line Driver (AND/OR)	8T13	
Dual EIA-232B/MIL Line Driver	8T15	Comp
Dual EIA-232B/MIL Receiver	8T16	
Dual Line Driver for IBM 360/370 Interface	8T23	
Dual Line Receiver for IBM 360/370 Interface	8T24	
Hex Bus Receiver (DM8837)	8T37	

OPEN COLLECTOR, BUFFERS, DRIVERS, AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Bus Transceiver	8T38	
Quad Bus Transceiver	8T26	Comp
Quad Bus Transceiver	8T28	True
Quad 2-Input NAND Buffer	38	
Quad 2-Input NAND Driver	3037	
Quad 2-Input NAND Driver	3038	
Hex Inverter	05	Comp
Hex Inverter/Driver	06	Comp
Hex Buffer/Driver	07	True
Hex Buffer/Driver	16	Comp
Hex Buffer/Driver	17	True
Octal Inverter/Driver	30240	Comp
Octal Driver, Non-Inverting	30244	True
Octal Transceiver, Non-Inverting	30245	True
Octal Transceiver, Inverting	30640	Comp
Octal Transceiver	621	True
Octal Transceiver	623	True
Octal Transceiver	641, 641-1	True
Octal Transceiver	642, 642-2	Comp
Octal Transceiver and Registers	647	True
Octal Transceiver and Registers	649	Comp
BCD to Decimal Decoder/Driver	45	Active-LOW
BCD to Decimal Decoder/Driver	145	Active-LOW

Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

Function Cross Reference Guide

MULTIVIBRATORS AND PHASE LOCKED LOOPS

FUNCTION	DEVICE NUMBER
Monostable Multivibrator	121
Dual Retriggerable Monostable Multivibrator	123
Dual Monostable Multivibrator	221
Dual Retriggerable Monostable Multivibrator	423
Dual Monostable Multivibrator	4528
Dual Retriggerable Monostable Multivibrator	4538
Monostable/Astable Multivibrator	4047
Digital Phase Locked Loop Filter	297
Phase Locked Loop	4046

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit Binary Full Adder, Ripple Carry	83
4-Bit Binary Full Adder, Fast Carry	283
4-Bit Binary Full Adder	4008
4-Bit BCD Full Adder	82S82
4-Bit ALU	181
ALU/Function Generator	881
4-Bit ALU	82S83
Look Ahead Carry Generator	182
Look Ahead Carry Generator	882

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Comparator	85
4-Bit Comparator	4585
5-Bit Comparator	9324
8-Bit Comparator	521
8-Bit Comparator	688

PARITY

FUNCTION	DEVICE NUMBER
8-Bit Odd/Even Parity Checker	180
8-Bit Parity Generator/Checker	8262
8-Bit Parity Generator/Checker	82S62
9-Bit Odd/Even Parity Generator/Checker	280
13-Bit Parity Generator/Checker	4531

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
Dual Port RAM Controller with Dynamic Memory Refresh	764
Dual Port RAM Controller without Latch	765
8-Bit Serial Multiplier with Adder/Subtractor	784
IEC/IEEE Bus Interface	4738
Frequency Synthesizer	4750
A.C. Motor Control Circuit	4752
18-Element Bar Graph LCD Driver	4754

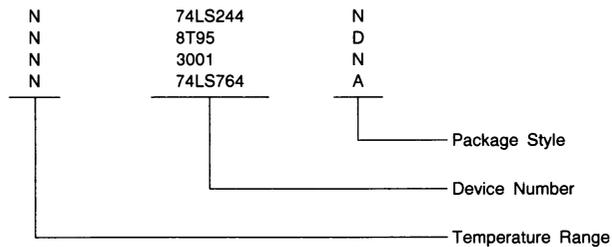
Function not contained in this manual. Please check Technology Selection Guide for appropriate technology — FAST or CMOS.

Logic Products

Signetics commercial TTL products are generally available in both standard dual-in-line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial product, the standard temperature range is 0-70°C. Available package options are shown on individual data sheets in the "Ordering Code" block. For surface mounted devices the S.O. plastic dual-in-line package is supplied up to and including 28 pins. Above 28 pins, the plastic leaded chip carrier is utilized.

A wide variety of functions and package options is available for military products. Information on military products is available from the nearest Signetics sales office, sales representative, or authorized distributor. The Signetics Military Products Data Manual contains specifications, package, and ordering information for all military-grade products.

ORDERING CODE EXAMPLES



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
N = Commercial Range 0°C to 70°C	74XX 74LSXX 74SXX 8TXX etc.	N = Plastic DIP D = Plastic S.O. DIP (surface mounted) A = Plastic Leaded Chip Carrier
S = Military Range -55°C to 125°C	See Military Products Data Manual	

Logic Products

SIGNETICS LOGIC PRODUCTS QUALITY

Signetics has put together a winning process for manufacturing Logic Products. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The products produced in the Standard Products Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 A/cm². Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to ensure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data

also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from -55°C to $+125^\circ\text{C}$ and at $+10\%$ supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 - QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Logic products, sam-

ples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: $T_J = 150^\circ\text{C}$, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: $T_J = 150^\circ\text{C}$, 1000 hours
- Temperature Humidity Biased Life: 85°C , 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): -65°C to $+150^\circ\text{C}$, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C , 100% saturated steam) and 300 cycles of thermal shock (-65°C to $+150^\circ\text{C}$)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality and Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the corporate SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership*.

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100PPM (parts per million), down from an industry practice of 10,000PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented-

low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

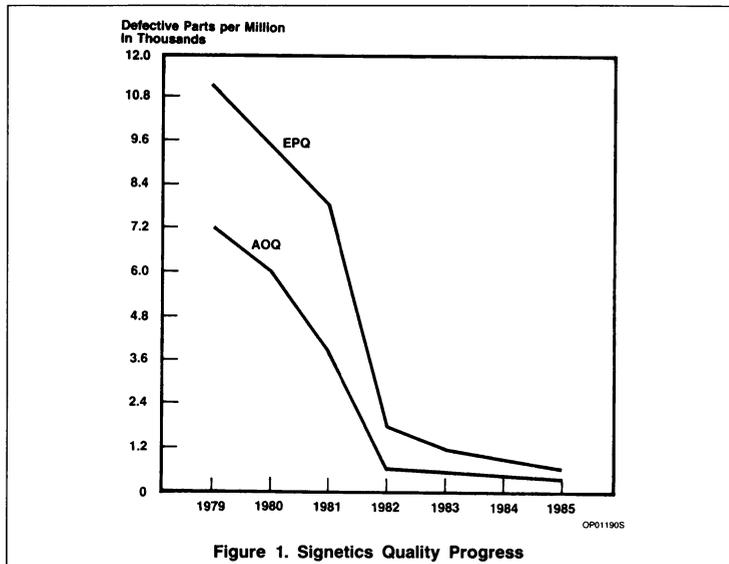


Figure 1. Signetics Quality Progress

Quality and Reliability

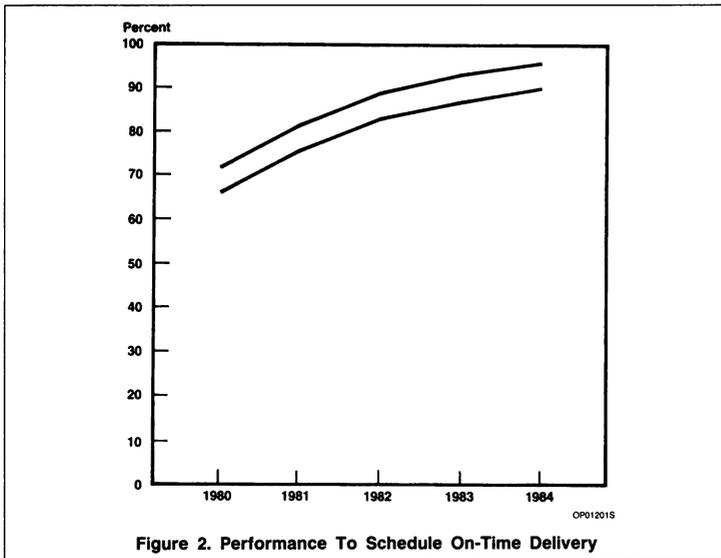


Figure 2. Performance To Schedule On-Time Delivery

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The quality improvement program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" - ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Quality and Reliability

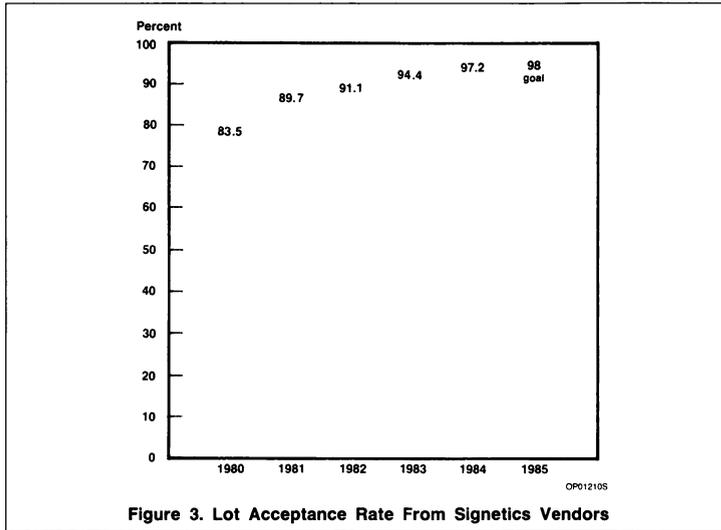


Figure 3. Lot Acceptance Rate From Signetics Vendors

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This team work with you will allow us to achieve our mutual goal of improved product quality.

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

MATERIAL WAIVERS

1985 - 0
 1984 - 0
 1983 - 0
 1982 - 2
 1981 - 134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities - failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letter-head directly to the corporate director of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. During the development of the program many profound changes were made. Figure 4, *Logic Products Generic Process Flow*, shows the result. Key changes included such things as implementing 100% temperature testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of Logic products. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

Quality and Reliability

As time goes on the drive for a product line that has Zero Defects will grow in intensity. These efforts will provide both Signetics and our customers with the ability to achieve the mutual goal of improved product quality.

The Logic Products Quality Assurance department has monitored PPM progress, which can be seen in Figure 5. We are pleased with the progress that has been made, and expect to achieve even more impressive results as the procedures for accomplishing these tasks are fine tuned.

The real measure of any quality improvement program is the result that our customers see. The meaning of *Quality* is more than just working circuits. It means commitment to *On Time Delivery at the Right Place of the Right Quantity of the Right Product at the Agreed Upon Price.*

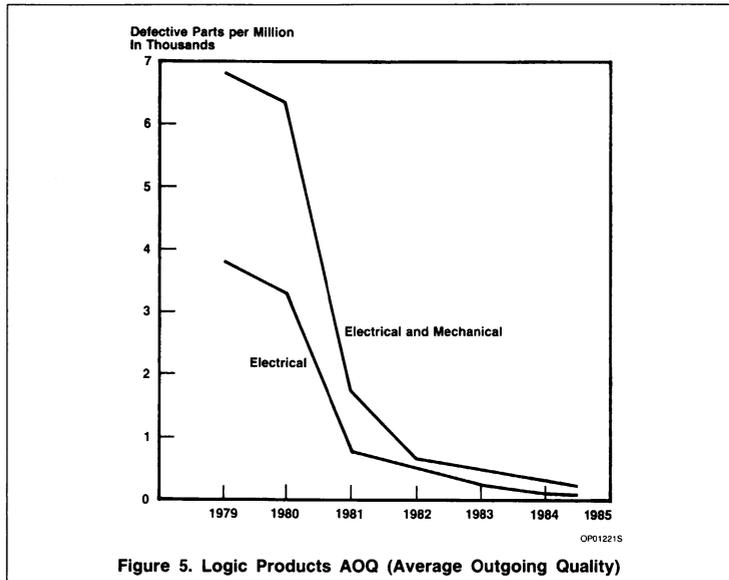


Figure 5. Logic Products AOQ (Average Outgoing Quality)

Signetics



**Section 3
Military Information**

Logic Products

Logic Products

Effective January 1, 1985, this section has been superseded by the 1985 Military Products Data Manual. Information regarding this manual can be obtained from the Military Division in Sacramento. (916) 925-6700.

MILITARY STANDARD PRODUCTS

The Signetics Military product line offering includes JAN Qualified Class S and B, and Class B vendor standard products. These products are designed to offer our customers the optimum of quality, reliability, delivery and cost. The benefits of these products provide our customers:

- Industry-wide standardization.
- Fewer custom specifications.
- Cost savings associated with larger lots.
- Better lead times by reducing specification negotiation time and allowing off-the-shelf procurement.
- Industry standard marking.

JAN QUALIFIED PRODUCT

JAN qualified product is offered to give our customers the highest quality and reliability. The JAN processing levels (Class S and B) are a result of the Governments product standardization programs, and our JAN production lines are certified by the qualifying activity, the Defense Electronics Supply Center (DESC). Signetics strongly recommends the use of JAN product which is listed on the MIL-M-38510 Qualified Products List (QPL).

JAN qualified products are fabricated, assembled, tested, and inspected in U.S. Government certified facilities in Sunnyvale, California (wafer fab), Orem, Utah (wafer fab, assembly), and in Sacramento, California (burn-in, test, quality conformance inspection).

Testing and inspection to MIL-M-38510 is monitored by resident Government Source Inspection (GSI) personnel representing the Defense Contract Administration Services (DCAS).

DESC prohibits any customer imposed additions, deviations, omissions, or waivers on procurement of JAN products. Product must conform completely to Government specifications prior to shipment and is verified by Signetics Quality Control. A Certificate of

Conformance and Procurement Traceability is supplied with each lot shipped.

JAN qualified products are listed in QPL-38510, issued periodically by DESC. For current QPL information, customers may contact their local sales representative, Military Marketing in Sacramento, or directly with DESC-EQM at (513) 296-6355. The JAN products listed herein should be considered valid only on its date of publication.

These categories of product conform to Quality Levels A and B of MIL-HDBK-217 ($\pi_Q = 0.5$ Class S, 1.0 for Class B).

The example at the bottom of this page illustrates the part numbering system for JAN product, the part number is per MIL-M-38510.

SIGNETICS CLASS B STANDARD PRODUCT (RB)

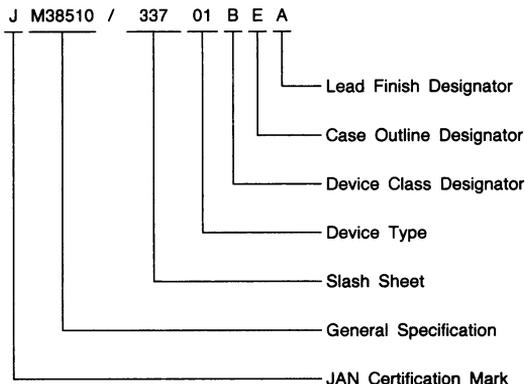
Signetics Class B Standard product is offered for use when no JAN product is qualified on the QPL, DESC Drawing product is not available, or when program requirements allow the use of vendor standard product.

Class B standard product conforms to MIL-STD-883, general provisions Paragraph 1.2.1 (and its sub-paragraphs), except where noted. (See Product Noncompliance Section of Military Data Book and/or Hand Book). No other claims, expressed or implied, are made of equivalence to JAN product or to MIL-M-38510. Signetics compliant product also conforms with JEDEC Publication 101, except for marking content.

Electrical test requirements are as stated in the most current Signetics Military Data Manual only.

- 100% final electrical tests include all Data Manual parameter limits, test conditions, and temperatures applicable to Subgroups 1, 2, 3, 7, and 9 of MIL-STD-883, Method 5004 for digital products, or to Subgroups 1, 2, 3, 4, and 9 for Linear Products.
- Group A sample electrical inspection tests include all final electrical subgroups as well as all other Data Manual parameters with specified minimum or maximum limits.
- End point electrical tests used for QCI inspection sampling (Groups C and D) are those Data Manual parameter limits, test conditions, and temperatures applicable to Group A Subgroups 1, 2, and 3 per MIL-STD-883, Method 5005, or to Subgroup 1 for Linear Products.

Data Manual parameters which have no specified minimum or maximum limits (typical performance only) are not tested. Parameters which have limits specified at 25°C only, are tested only at that temperature. Detailed parameter assignment to subgroups and other test detail are contained in documented Signetics internal Product Electrical specifications, and are available upon request. Actual test program symbolics are available for customer review at the factory, but are considered proprietary and will not be copied or otherwise distributed outside of Signetics.



Military Information

QCI Groups A and B testing are performed on all products and packages per MIL-M-38510 and MIL-STD-883, Method 5005. Signetics utilizes inline Group A and alternate Group B for all lines. QCI Groups C and D are routinely performed on all compliant families and package types.

Waivers, deviations, or exceptions of any kind deemed necessary in the course of the contracts must be issued in accordance with DOD-STD-480. Should Signetics have knowledge of the need for waivers at the time of response to quote (RFQ) or order entry, that

information will be transmitted prior to order entry.

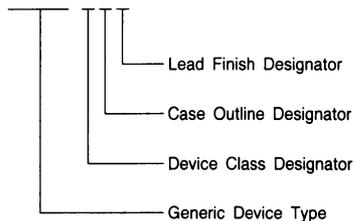
Package types which do not have case outlines letters assigned in MIL-M-38510, Appendix C, will be assigned case outline letters per JEDEC Publication 101.

The Signetics standard Product Assurance Plan documentation is available for customer review at the factory, and is considered proprietary.

This category of product conforms to quality level B-2 of MIL-HDBK-217 ($\pi_Q = 6.5$).

For Class B Standard Product, the part number is listed as follows:

54LS161/ B E A



Signetics



Section 4
TTL User's Guide

Logic Products

Logic Products

INTRODUCTION

The TTL Logic devices described in this data manual differ widely in function, complexity and performance, but their electrical input and output characteristics are very similar and are defined and tested to guarantee compatibility. The data sheets that make up this book cover four major categories of TTL circuits and a series of TTL compatible interface products.

The oldest TTL product category is the gold-doped double-diffused type which is made up of the 7400 family of devices. This family reflects the same performance ranges and differ only in functions and pin configuration.

The remaining two categories of products are fabricated with a non-saturating Schottky clamped transistor technique. The 74S00 family of TTL products are very high performance, high power devices. The most popular TTL category is the 74LS Low Power Schottky family. These products feature the performance of the 74 family at about 1/4 the power.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages and currents as shown below.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	74	74S	74LS
V _{CC} supply voltage, continuous (Note a)	7.0V	7.0V	7.0V
Input voltage, continuous (Notes a and b)	-0.5V to +5.5V	-0.5V to +5.5V	-0.5V to +7.0V ^(b)
Input current, continuous	-30mA to +5mA	-30mA to +5mA	-30mA to +1mA
Voltage applied to HIGH outputs (Note a)	-0.5V to V _{CC}	-0.5V to 7.0V	-0.5V to V _{CC}
Voltage applied to "off" Open Collector outputs (Notes a and c)	-0.5V to 7.0V	-0.5V to 7.0V	-0.5V to 7.0V
Current into LOW standard output, continuous	30mA	40mA	15mA
Current into LOW buffer output, continuous	80mA	100mA	50mA
Operating free air temperature range (Com'l)	0°C to +70°C		
Storage temperature range	-65°C to +150°C		

NOTES:

- Voltages are referenced to device ground terminal.
- LS devices are generally limited to 7.0V maximum input voltage. Exceptions are called out on individual product data sheets.
- Some open collector devices are specially processed to handle higher output voltages of from 15V to 30V. The Absolute Maximum voltage for these devices is 10% over the specified V_{OUT} test condition.

OPERATING TEMPERATURE AND VOLTAGE RANGES

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 volts. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250mV) over an ambient temperature range of 0°C to 70°C.

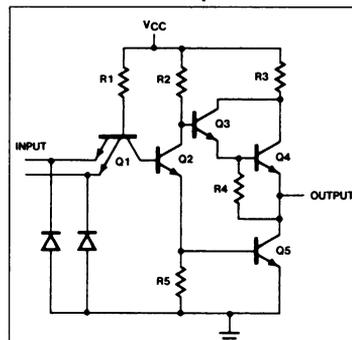
The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature T_A or package (case) temperature T_C. The thermal resistance for the various packages in which the TTL products are offered is specified with the Package Information in Section 9 of this manual.

GENERAL TTL CIRCUIT CHARACTERISTICS

All TTL products are derived from a common NAND logic structure. The NAND circuit is actually five subcircuits as shown in Figure 1 and each performs a separate function. The input circuit (1) is an AND gate usually fabricated with a multi-emitter transistor which characterizes TTL technology. Many Schottky processed circuits have been designed with PNP or diode inputs in order to optimize the speed/power performance of the circuits.

The phase splitter (2) provides the inversion and amplification in the circuit. It determines whether the outputs are active level HIGH or active level LOW. The level shifter (3) pro-

NAND Gate Example



Number of inputs depends on the gate.

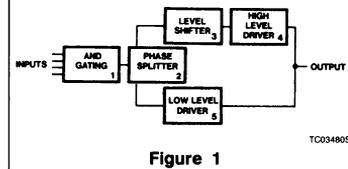


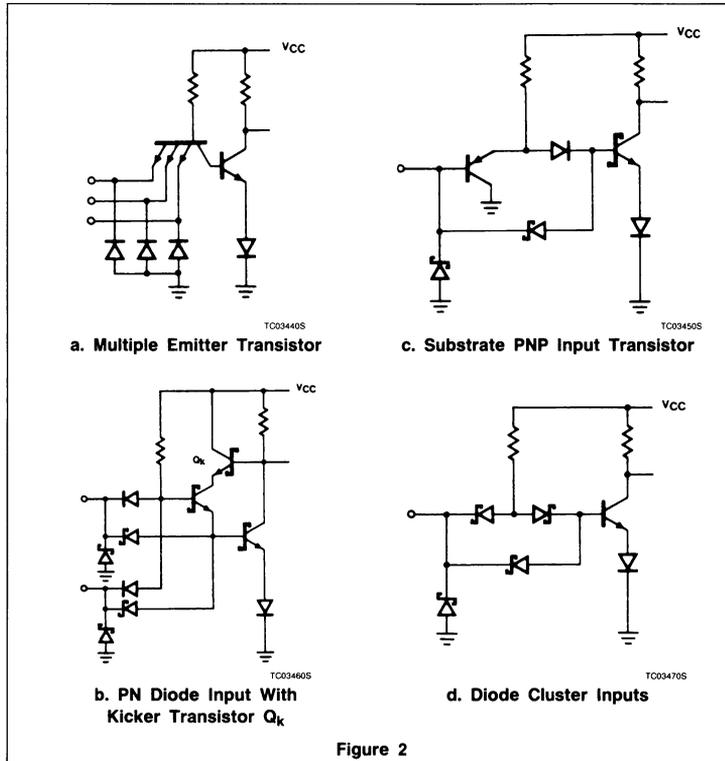
Figure 1

vides noise immunity between the HIGH and LOW output levels, and minimizes the possibility of having both HIGH level driver (4) and LOW level driver (5) on simultaneously.

The level shifter (3) and HIGH level driver (4) combine to form an emitter follower circuit that tracks the voltage at the collector of the

TTL User's Guide

TTL INPUT CONFIGURATIONS



phase splitter. This circuit is usually designed to drive very heavy capacitive loads so that the initial rise time of the output is determined primarily by the rise time at the phase splitter collector. The LOW level driver (5) is usually a saturating transistor for the gold-doped process devices, or a Schottky diode clamped transistor for the Schottky processed devices. These output transistors are designed to sink the rated fan-out current which characterizes the various TTL families.

Input Circuits

The input circuits as described above are basically AND gate configurations designed with multiple-emitter NPN transistors (MET), substrate PNP transistors, or various junction and Schottky diodes as shown in Figure 2. All of the circuit configurations have very high impedance in the HIGH state. When the input voltage is above the circuit threshold voltage, all of the inputs act like reversed biased diodes.

The MET transistors are actually operated in the inverse mode, but the gain is so low there is very little current flowing into the devices.

The LOW level input impedance of the MET and diode inputs is determined by the internal pull-up resistor. This resistor is nominally $2k\Omega$ for 54S/74S inputs, and it is $16k\Omega$ to $20k\Omega$ for the 54LS/74LS inputs. Some 54LS/74LS buffer devices have substrate PNP inputs which exhibit very high impedance at both HIGH and LOW input logic levels. This is used to minimize the input load factor and provide better output drive and performance.

The inputs to all Signetics TTL devices have clamp diodes to ground to minimize negative ringing effects. These diodes are designed to operate in the ac mode and cannot handle heavy dc currents for long periods.

Output Circuits

The output circuit configurations used for the TTL products in this manual are shown in Figure 3. The basic advantages and disadvantages of each configuration are given for reference. The different circuits are used to optimize the functional and performance requirements of the various devices, and are not necessarily restricted to individual TTL families. The pull-down circuit (not shown) on the base of the LOW level driver is usually a

resistor which provides a means of turning off the output transistor. The majority of the 54S/74S and 54LS/74LS devices use a resistor-transistor network which acts to square-up the $V_{IN} - V_{OUT}$ transfer characteristics of the device.

A resistive pull-up can be added to any TTL output circuit increasing V_{OH} to almost V_{CC} , but only circuits "c," "d," and "e" can be pulled higher than V_{CC} , e.g., to +7.0V for driving MOS circuits. Configurations "a" and "b" have a diode associated with the resistor at the output which clamps the output one diode drop above V_{CC} . This is an important consideration in large systems where sections might be powered down ($V_{CC} = 0$). In this state, the outputs of circuits "a" and "b" represent a very low impedance at a fairly low voltage ($< 1.0V$), while the outputs of circuits "c," "d," and "e" represent a high impedance and thus a logic HIGH, more appropriate for isolation from the rest of the system.

The output impedance of a typical TTL device in both the LOW and HIGH state is shown in Figure 4. In the LOW state, the output impedance is determined by a saturated transistor (about 8Ω to 10Ω). However, at very high sinking current, especially at low temperature, the output device is not able to stay in saturation and the output impedance rises as shown.

When switching from the LOW to the HIGH state, the totem-pole output structure provides a low output impedance capable of rapidly charging capacitive loads. However, charge and discharge currents must also flow through the V_{CC} and the ground distribution networks. The V_{CC} and ground lines should therefore be short and adequately decoupled.

3-State Outputs

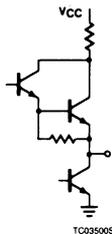
Some of the buffers and registers have 3-state outputs designed for "busing." This type of output electrically performs as a totem-pole output with the additional feature that the output may be disabled, neither sinking nor sourcing current. The 3-state outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active at any time.

DESIGN CONSIDERATIONS

The properties of high speed TTL logic circuits dictate that some care be used in the design and layout of a system. Some general "design considerations" are included in this section. This is not intended to be a thorough guideline for designing TTL systems, but a reference for some of the constraints and

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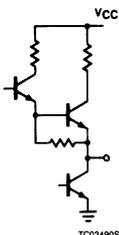
TTL OUTPUT CONFIGURATIONS



a. Darlington

ADVANTAGE:
 High ac drive capability
 $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$
 Small size (transistors share one common isolation)

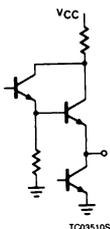
DISADVANTAGE:
 Output cannot be pulled higher than one diode drop above V_{CC}



b. 2-stage Emitter Follower ('Darlington Split')

ADVANTAGE:
 High ac drive capability
 $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$

DISADVANTAGE:
 Larger than Circuit A
 Output cannot be pulled higher than one diode drop above V_{CC}



c. Darlington With Resistor to Ground

ADVANTAGE:
 High ac drive capability
 Lower $V_{OH} = (V_{CC} - 2 V_{BE})$ increases speed
 Outputs can be pulled higher than V_{CC}

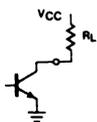
DISADVANTAGE:
 Higher dissipation
 Lower noise immunity in the HIGH state



d. Transistor - Diode

ADVANTAGE:
 Lowest power consumption
 Small size
 Outputs can be pulled higher than V_{CC}

DISADVANTAGE:
 Less ac drive capability



e. Open Collector

ADVANTAGE:
 Bussable, allows collector ANDing (Wired-OR)

DISADVANTAGE:
 High output impedance in the HIGH state
 Slow, especially with capacitive loading
 Requires additional resistor

Figure 3

TYPICAL INPUT/OUTPUT CHARACTERISTICS

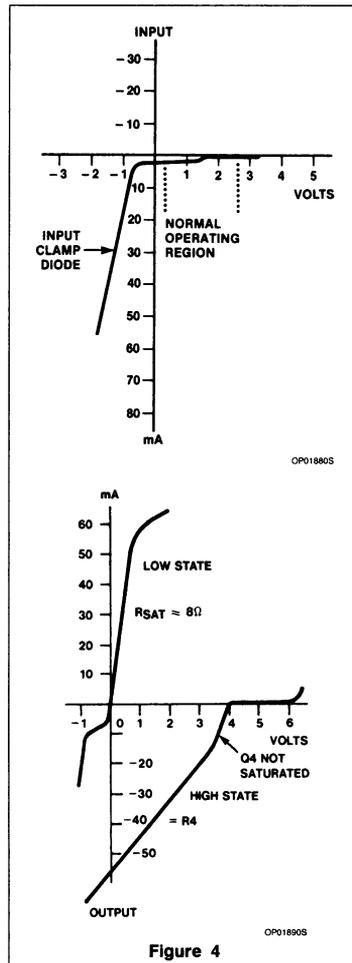


Figure 4

techniques to be considered when designing the system.

Mixing 74 and 74LS is less restrictive, and the overall system design need not be so elaborate. Standard two sided PC boards can be used with good, well decoupled power and ground grid systems. The signal transitions are slower and therefore generate less noise. However, good high speed design techniques are still required, especially when working with counters, registers, or other devices with memory.

Clock Pulse Requirements

Most TTL flip-flop circuits are master-slave devices which makes their clock inputs level

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sensitive. This is an improvement over ac coupled clock inputs, but it does not make the devices fully insensitive to clock edge rates. The dc level at which the data in the master (input section) is transferred to the slave (output section) is the normal threshold voltage for the devices. For most Signetics TTL devices this level is 1.4V at 25°C, and it changes at a rate of about -4mV/°C.

When the clock input reaches the threshold voltage, the internal gates and the changing outputs start to dump current into the ground lead of the device. If there are enough internal gates or loaded outputs changing at the same time, the chip ground reference level (and therefore the clock input reference level) can rise by as much as 500mV. This ground noise is the algebraic sum of the internal and external ground plane noise. If the clock input of a positive edge triggered device is at or near the threshold of the device during the ground noise transient period, it is quite possible for the internal device to receive multiple clock pulses.

For this reason the rise time on positive edge-triggered devices should be less than the nominal clock to output delay time measured between the 0.8V and 2.0V levels of the clock driver. This edge rate is obtainable from almost any Signetics TTL device of the same family, as long as it is driving no more than rated fan out and no more than 12 to 16 inches of line. When clock pulses are distributed on lines over 16 inches long, all of the clock inputs should be clustered at the receiving end of the line to avoid reflection problems at the driving end.

Special Note

Some of the Signetics Counters and registers have been designed with a special clock buffer that includes a small amount of hysteresis to minimize clock edge rate and noise problems. The LS160A, LS161A, LS162A, LS163A, LS364, and LS374 all have the special clock buffers to increase their tolerance of slow positive clock edges and heavy ground noise.

TTL OUTPUTS TIED TOGETHER

The only TTL outputs that are designed to be tied together are open collector and 3-state outputs. Standard TTL outputs should not be tied together unless their logic levels will always be the same; either all HIGH or all LOW. When connecting open collector or 3-state outputs together some general guidelines must be observed.

Open Collector

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added

between the OR-tie connector and V_{CC} to establish an active HIGH level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows:

$$R(\text{Min}) = \frac{V_{CC}(\text{Max}) - V_{OL}}{I_{OL} - N_2(I_{IH})}$$

$$R(\text{Max}) = \frac{V_{CC}(\text{Min}) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

N₂(I_{IH}) = Cumulative maximum input LOW current for all inputs tied to OR-tie connection.

N₁(I_{OH}) = Cumulative maximum output HIGH leakage current for all outputs tied to OR-tie connection.

N₂(I_{IH}) = Cumulative maximum input HIGH leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the HIGH level, the R(Max) must be de-

creased enough to provide the required (V_{OH}/R(pull-down)) current.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in Load Circuit 1, Figure 5.

Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor Load Circuits 2 and 3 give progressively slower propagation delays.

3-STATE OUTPUTS

3-State Outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active at any time. This generally requires that the Output Enable signals be non-overlapping. When TTL decoders are used to enable 3-state outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally be guaranteed when the address is changing.

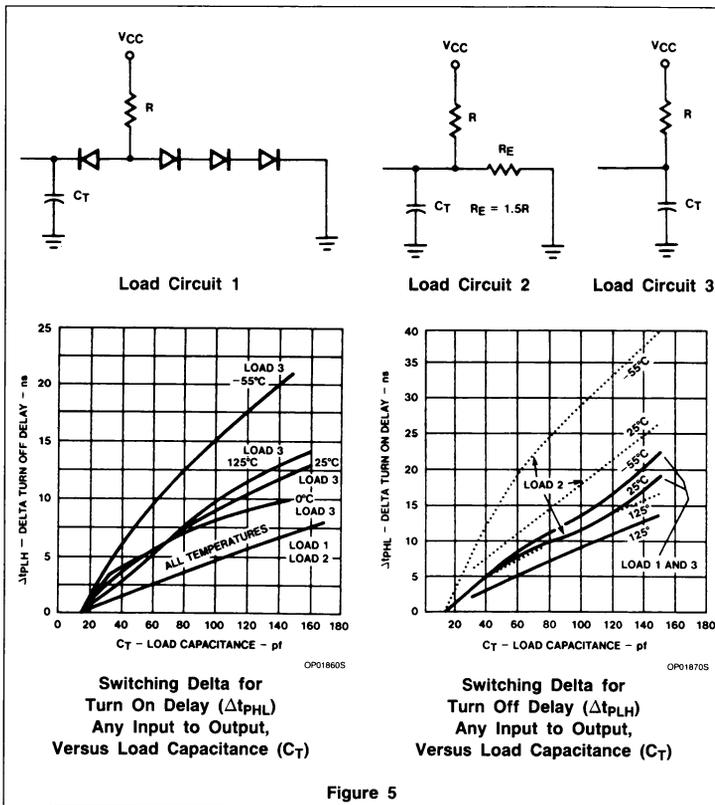


Figure 5

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Since most 3-state Output Enable signals are active LOW, shift registers or edge-triggered storage registers provide good Output Enable buffers. Shift registers with one circulating LOW bit, like the "164" or "194" are ideal for sequential enable signals. The "174" or "273" can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from LOW-to-HIGH faster than from HIGH-to-LOW, the selection of one device at a time is assured.

POWER SUPPLY DECOUPLING

Power supply capacitance decoupling is required for any TTL system. Generally 0.01 μF per synchronously driven gate and at least 0.1 μF for each 20 gates is required regardless of synchronization. Counters and shift registers are especially susceptible to power and ground line noise. They should be decoupled with a 0.1 μF capacitor for each eight internal flip-flops, or one capacitor for each two devices put as close as possible to the devices. Buffers and line drivers should be heavily decoupled at the driver power pins, due to the large current transients needed to charge and discharge the lines.

On-Board Regulation

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transistors, thus creating V_{CC} noise. An on-board regulator would not only regulate the power supplied to the circuits on-board, but also would isolate the noise otherwise propagated to the reset of the system. Systems designed using this technique would not need tight regulation on the main power supply.

LINE DRIVING AND RECEIVING

Open wire connections between TTL circuits should not be bundled, tied, or routed together. Instead, point-to-point wiring should be used, preferably above a ground plane which reduces coupling between conductors.

Single line wire interconnections should not exceed two feet; for wires longer than 15 inches, a ground plane is essential to provide adequate system performance. Over 2-foot twisted pairs or coaxial cable should be used. The characteristic impedance of an open wire over a ground plane is about 150 Ω , while for twisted pairs of #26 wire the impedance is about 120 Ω . For added protection against crosstalk, coaxial cables can be used but coaxial cables having very low characteristic impedances are difficult to drive. For best performance, coaxial cables with a character-

istic impedance R_0 of 100 Ω should be used. Resistive pull-ups at the receiving end can be used to increase noise margins. If reflection effects are unacceptable, the line must be terminated in its characteristic impedance. One method is shown in Figure 6 where the output of the line is tied to V_{CC} through a resistor equivalent to the characteristic impedance of the line. Therefore, R_0 is fairly small, and the driving gate must sink the current through it in addition to the current from the inputs being driven. Terminating the line in a voltage divider with two resistors, each twice the line impedance, reduces the extra sink current by 50%. It is preferable to dedicate gates solely for line driving if the line length is in excess of five feet.

Clamp Diode Effect on Negative Input Voltages

All Signetics TTL circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative dc voltages or long duration negative pulses especially for 74LS product. If the input voltage of an LS device is taken more than 0.5 volts negative (referenced to the device ground terminal) for more than 0.5 microseconds, it is possible to activate a parasitic circuit component which can cause the HIGH level output of that gate to degrade sufficiently to cause a logic error.

Disposition of Unused Inputs

Electrically open inputs degrade ac noise immunity as well as the switching speed of a circuit. To optimize performance, each input must be connected to a low impedance source. Unused active HIGH NOR or OR inputs must be returned to ground or a LOW level output. Unused active HIGH NAND or AND inputs should be maintained at a voltage greater than 2.7V, but not exceeding the Absolute Maximum Rating. This eliminates

the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect the unused active LOW inputs of the TTL devices to ground. The active HIGH inputs should be tied through a resistor of from 1K to 10k Ω to V_{CC} . The unused active HIGH LS inputs can be tied directly to V_{CC} , as long as the leads are very short and the supply is adequately decoupled.
2. Connect the unused HIGH input to the output of an unused gate that is forced HIGH.
3. Tie unused NAND or AND inputs (multi-emitter inputs) of non-LS devices to a used input of the same gate, provided the HIGH level fan out of the driving circuit is not exceeded. Note that the LOW level fan out is not increased by this connection because the inputs share a common base pull-up resistor.

Unused Gates

It is recommended that the outputs of unused gates be forced HIGH by tying a NAND gate input or all NOR gate inputs to ground. This lowers the power dissipation and supplies a logic HIGH at the gate output which can be used at unused inputs to other gates.

Increasing Fan Out

To increase fan out, inputs and outputs of gates on the same package may be paralleled. It is advisable to limit the gates being paralleled to those in a single package to avoid large transient supply currents due to different switching times of the gates. This is not detrimental to the devices, but could cause logic problems if the gates are being used as clock drivers.

TTL DRIVING TWISTED PAIR

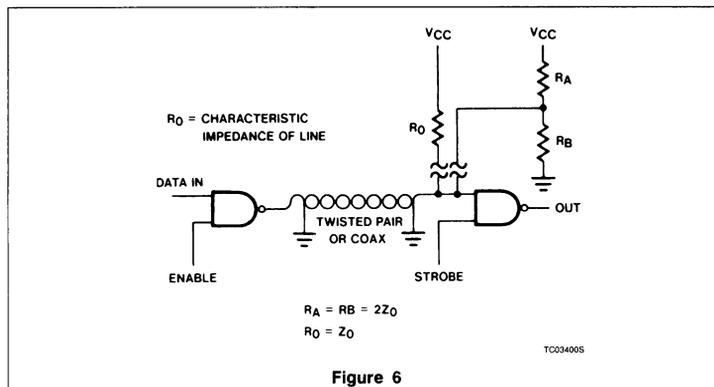


Figure 6

TTL User's Guide

Isolation Diodes

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

Input Loading and Output Drive Characteristics

The logic levels of all the TTL products are fully compatible with each other. However, the inputs loading and output drive characteristics of each of these families is different and must be taken into consideration when mixing the TTL families in a system. Table 1 shows the relative drive capabilities of each family for the Commercial temperature and voltage ranges. For Military ranges the 74LS drive capabilities must be cut in half. You will note that the 74LS Buffers have three times the drive capability of the standard 74LS devices; in fact, they can drive more loads than any other non-buffer TTL device.

Mixing TTL Families

Most TTL families are intended to used together, but this cannot be done indiscriminately. Each family of TTL devices has unique input and output characteristics optimized to get the desired speed or power features. Fast devices like 74S and 74F are designed with relatively low input and output impedances. The speed of these devices is determined primarily by fast rise and fall times internally as well as at the input and output nodes. These fast transitions cause noise of various types in the system. Power and ground line noise is generated by the large currents needed to charge and discharge the circuit and load capacitances during the switching

Table 1

DRIVING DEVICE	NUMBER OF LOADS DRIVEN					
	74F	74LS	74	74S	8200 and 9300	82500
74F	33	50	12.5	10	12	50
74F Buffer	106	160	40	32	40	160
74LS	13	20	5	4	5	20
*74LS Buffer	40	60	15	12	15	60
74	26	40	10	8	10	40
74 Buffer	78	120	30	24	30	120
74S	33	50	12.5	10	12	50
74S Buffer	100	150	37.5	30	37	150
8200 & 9300	26	40	10	8	10	40
82500	33	50	12	10	12	50

*The 74LS Buffers include 3-state outputs except LS253 & LS670

NOTE:

For 74LS devices do not connect multiple inputs of a common gate together. This would increase the input coupling capacitance and reduce the ac noise immunity.

transitions. Signal line noise is generated by the fast output transitions and the relatively low output impedances, which tend to increase reflections.

The noise generated by these 74S and 74F devices can only be tolerated in systems designed with very short signal leads, elaborate ground planes, and good, well decoupled power distribution networks. Mixing the slower TTL families like 74 and 74LS with the higher speed families is also possible but

must be done with caution. The slower speed families are more susceptible to induced noise than the higher speed families due to their higher input and output impedances. The low power Schottky 74LS family is especially sensitive to induced noise and must be isolated as much as possible from the 74S and 74F devices. Separate or isolated power and ground systems are recommended, and the LS input signal lines should not run adjacent to lines driven by 74S and 74F devices.

TTL User's Guide

DC SYMBOLS AND DEFINITIONS

Voltages — All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., -10V is greater than -1.0V).

Currents — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

V_{CC}	Supply voltage: The range of power supply voltage over which the device is guaranteed to operate within the specified limits.	I_{CC}	Supply current: The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.
V_{IK}	Input clamp voltage: The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.	I_I	Input leakage current: The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
V_{IH}	Input HIGH voltage: The range of input voltages recognized by the device as a logic HIGH.	I_{IH}	Input HIGH current: The current flowing into an input when a specified HIGH level voltage is applied to that input.
$V_{IH(MIN)}$	Minimum Input HIGH voltage: This value is the guaranteed input HIGH threshold for the device. The minimum allowed input HIGH in a logic system.	I_{IL}	Input LOW current: The current flowing out of an input when a specified LOW level voltage is applied to that input.
V_{IL}	Input LOW voltage: The range of input voltages recognized by the device as a logic LOW.	I_{OH}	Output HIGH current: The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.
$V_{IL(MAX)}$	Maximum Input LOW voltage: This value is the guaranteed input LOW threshold for the device. The maximum allowed input LOW in a logic system.	I_{OL}	Output LOW current: The current flowing into an output which is in the LOW state.
V_M	Measurement voltage: The reference voltage level on ac waveforms for determining ac performance. Usually specified as 1.5V for most TTL families, but 1.3V for the Low Power Schottky 74LS family.	I_{OS}	Output short-circuit current: The current flowing out of an output which is in the HIGH state when that output is short-circuit to ground.
$V_{OH(MIN)}$	Output HIGH voltage: The minimum guaranteed HIGH voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.	I_{OZH}	Output off current HIGH: The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
$V_{OL(MAX)}$	Output LOW voltage: The maximum guaranteed LOW voltage at an output terminal sinking the specified load current I_{OL} .	I_{OZL}	Output off current LOW: The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.
V_{T+}	Positive-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (MIN).		
V_{T-}	Negative-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+} (MAX).		

TTL User's Guide

AC SWITCHING PARAMETERS AND DEFINITIONS

f_{MAX}	The maximum clock frequency: The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.	t_h	Hold time: The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_{PLH}	Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined HIGH level.	t_s	Set-up time: The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_{PHL}	Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.	t_w	Pulse width: The times between the specified reference points on the leading and trailing edges of a pulse.
t_{PHZ}	Output disable time from HIGH level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the HIGH level to a high impedance "off" state.	t_{rec}	Recovery time: The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.
t_{PLZ}	Output disable time from LOW level of 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the LOW level to a high impedance "off" state.	t_{TLH}	Transition time: LOW to HIGH, the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.
t_{PZH}	Output enable time to a HIGH level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the HIGH level.	t_{THL}	Transition time: LOW to HIGH, the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from LOW to HIGH.
t_{PZL}	Output enable time to a LOW level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the LOW level.	t_r, t_f	Clock input rise and fall times: 10% to 90% value.

Signetics

Section 5
74 Series Data Sheets

Logic Products

7400, LS00, S00 Gates

Quad Two-Input NAND Gate Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7400N, N74LS00N, N74S00N
Plastic SO	N74LS00D, N74S00D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

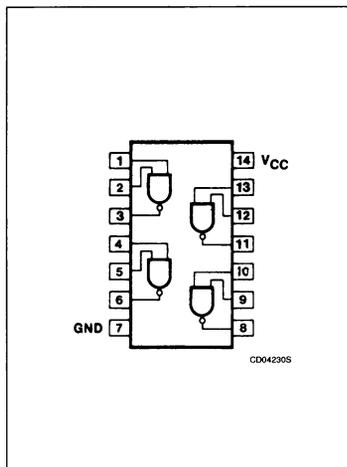
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

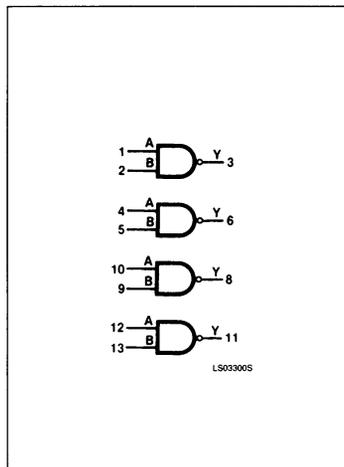
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

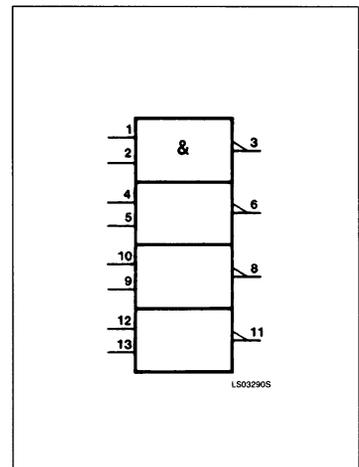
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



5

Gates

7400, LS00, S00

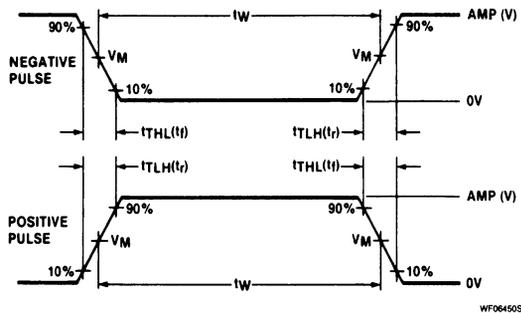
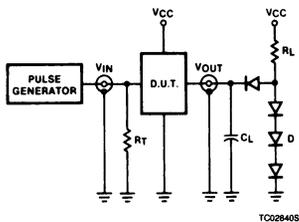
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18			-18	mA
I _{OH}	HIGH-level output current			-400			-400			-1000	µA
I _{OL}	LOW-level output current			16			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

7400, LS00, S00

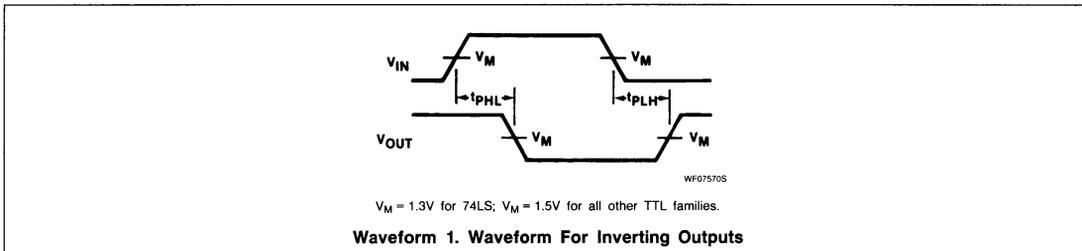
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7400			74LS00			74S00			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0						1.0	mA	
		V _I = 7.0V				0.1					mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40							μA	
		V _I = 2.7V				20				50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V		-1.6				-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-20		-100	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH		4	8		0.8	1.6		10	16	mA
		I _{CC} L Outputs LOW		12	22		2.4	4.4		20	36	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15		15 15		4.5 5.0	ns

74LS01 Gate

Quad Two-Input NAND Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS01	16ns	1.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS01N
Plastic SO	N74LS01D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

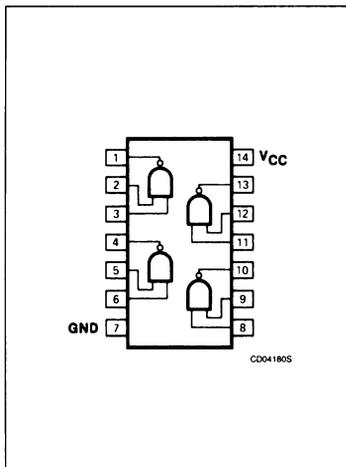
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
A, B	Inputs	1LSul
Y	Output	10LSul

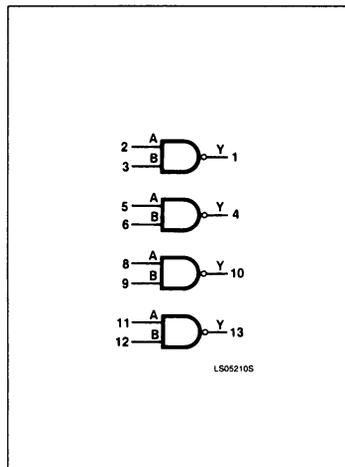
NOTE:

Where a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

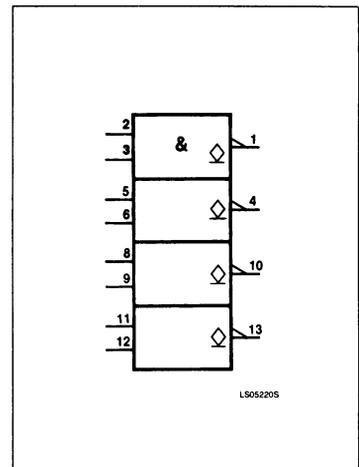
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74LS01

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

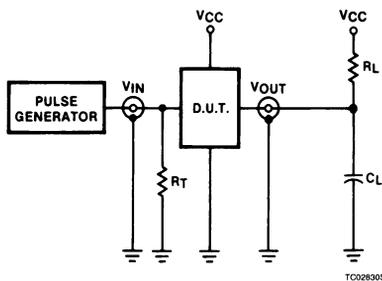
PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

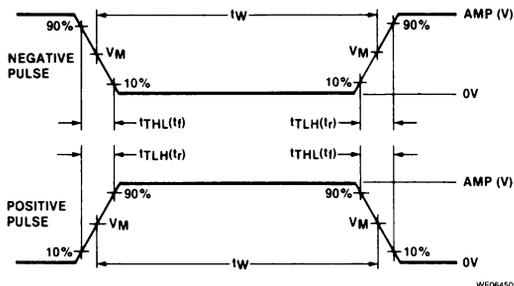
PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
V _{OH}	HIGH-level output voltage			5.5	V
I _{OL}	LOW-level output current			8	mA
T _A	Operating free-air temperature	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

74LS01

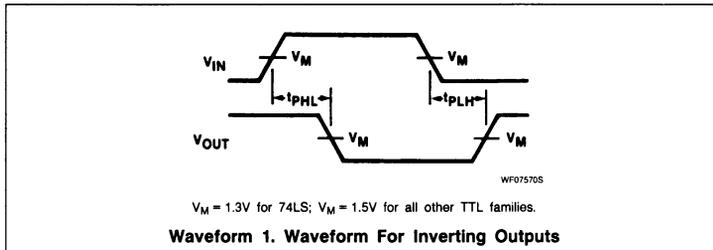
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS01			UNIT	
		Min	Typ ²	Max		
I _{OH}	HIGH-level output current V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			100	μA	
V _{OL}	V _{CC} = MIN, V _{IH} = MIN		0.35	0.5	V	
		I _{OL} = MAX I _{OL} = 4mA	0.25	0.4	V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 7.0V			0.1	mA	
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V			-0.4	mA	
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CC} H	Outputs HIGH	0.8	1.6	mA
		I _{CC} L	Outputs LOW	2.4	4.4	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		32 28	ns

7402, LS02, S02 Gates

Quad Two-Input NOR Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7402	10ns	11mA
74LS02	10ns	2.2mA
74S02	3.5ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7402N, N74LS02N, N74S02N
Plastic SO	N74LS02D, N74S02D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

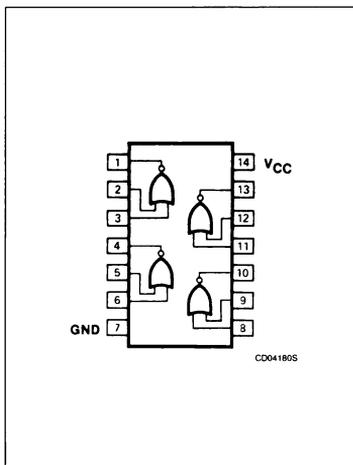
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

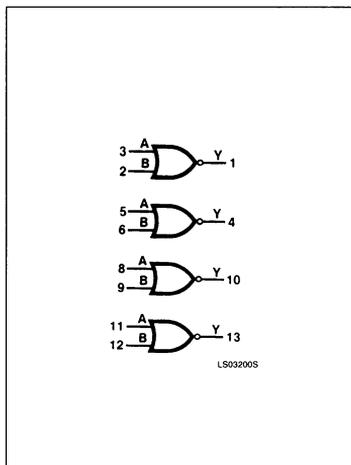
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

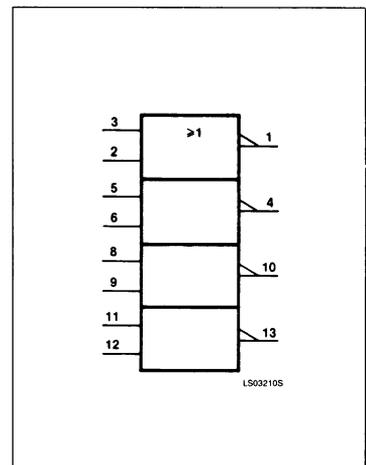
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7402, LS02, S02

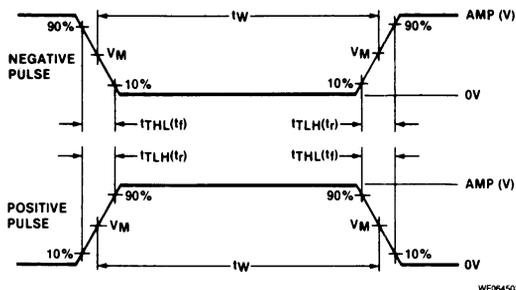
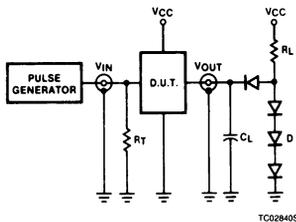
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-400			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definitions

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

7402, LS02, S02

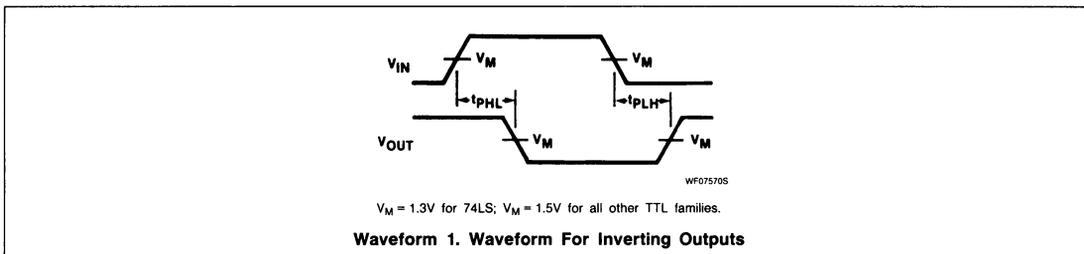
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7402			74LS02			74S02			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA					0.25	0.4			V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5		-1.2	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V						0.1			mA	
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V						20		50	μA	
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-55	-20		-100	-40		-100	mA	
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CCH} Outputs HIGH		8	16		1.6	3.2		17	29	mA
		I _{CCL} Outputs LOW		14	27		2.8	5.4		26	45	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		22 15		15 15		5.5 5.5	ns

7403, S03 Gates

Quad Two-Input NAND Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7403	35ns (t_{PLH}) 8ns (t_{PHL})	8mA
74S03	5ns (t_{PLH}) 4.5ns (t_{PHL})	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7403N, N74S03N
Plastic SO	N74S03D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

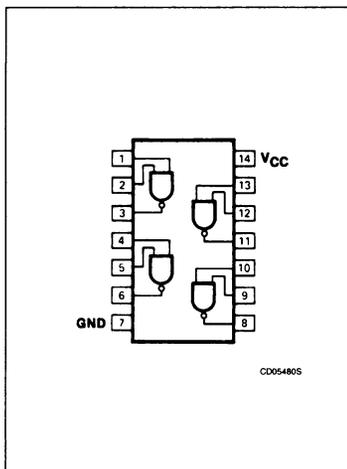
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S
A, B	Inputs	1uI	1Sul
Y	Output	10uI	10Sul

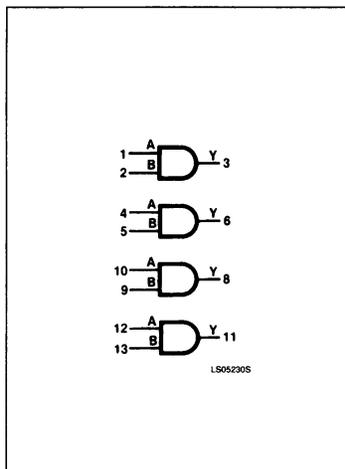
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

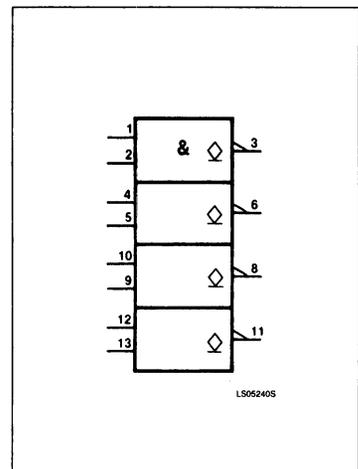
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7403, S03

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

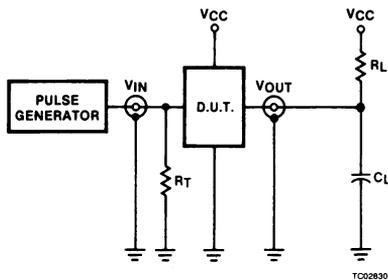
PARAMETER	74	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

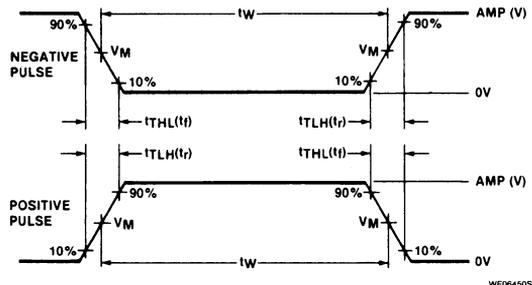
PARAMETER	74			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
V _{OH} HIGH-level output voltage			5.5			5.5	V
I _{OL} LOW-level output current			16			20	mA
T _A Operating free-air temperature	0		70	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open-Collector Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definitions

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

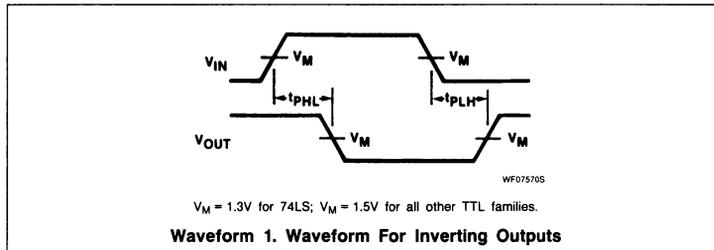
7403, S03

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7403			74S03			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{OH} = 5.5\text{V}$			250			250	μA
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = \text{MAX}$		0.2	0.4			0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5			-1.2	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5\text{V}$			1.0			1.0	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$		40				μA
		$V_I = 2.7\text{V}$					50	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$		-1.6				mA
		$V_I = 0.5\text{V}$					-2.0	mA
I_{CC} Supply current (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	4	8	6	13.2	mA	
		I_{CCL} Outputs LOW	12	22	20	36	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

AC WAVEFORM**AC ELECTRICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL}	For 7403 only, $R_L = 4\text{k}\Omega$ for t_{PLH} . Waveform 1		45 15		7.5 7.0	ns

7404, LS04, S04 Inverters

Hex Inverter
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7404	10ns	12mA
74LS04	9.5ns	2.4mA
74S04	3ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7404N, N74LS04N, N74S04N
Plastic SO	N74LS04D, N74S04D

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

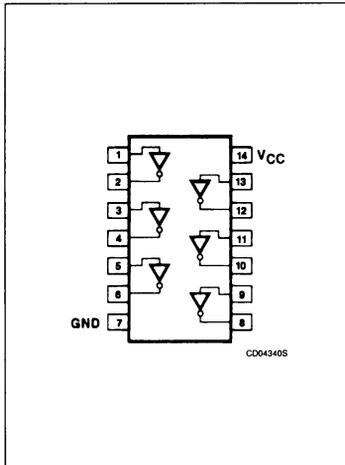
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A	Input	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

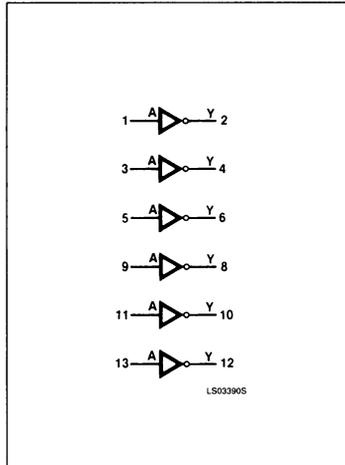
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

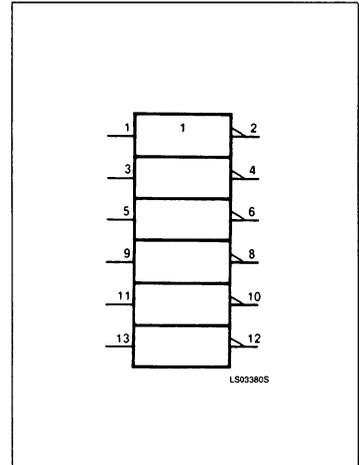
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Inverters

7404, LS04, S04

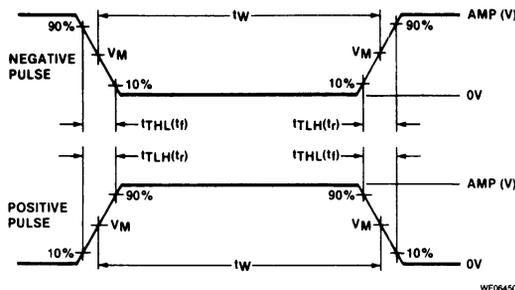
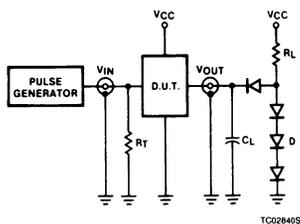
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-400			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Inverters

7404, LS04, S04

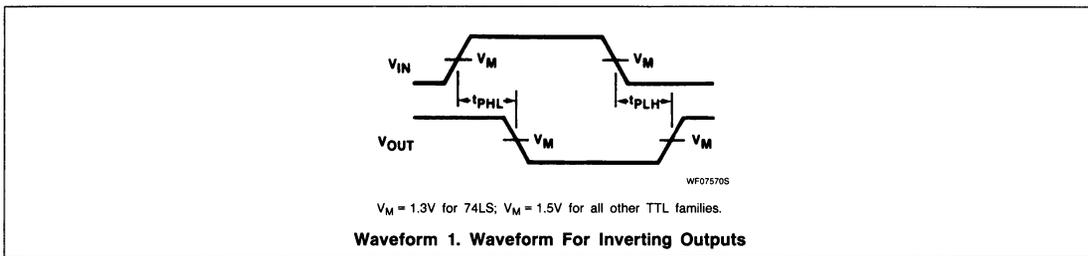
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7404			74LS04			74S04			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V						0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V						20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-20		-100	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		6	12		1.2	2.4		15	24	mA
		I _{CCL} Outputs LOW		18	33		3.6	6.6		30	54	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		22 15		15 15		4.5 5.0	ns

7405, LS05, S05 Inverters

Hex Inverter (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7405	40ns (t_{PLH}) 8ns (t_{PHL})	12mA
74LS05	17ns (t_{PLH}) 15ns (t_{PHL})	2.4mA
74S05	5ns (t_{PLH}) 4.5ns (t_{PHL})	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7405N, N74LS05N, N74S05N
Plastic SO	N74LS05D, N74S05D
Ceramic DIP	

FUNCTION TABLE

INPUT A	OUTPUT Y
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

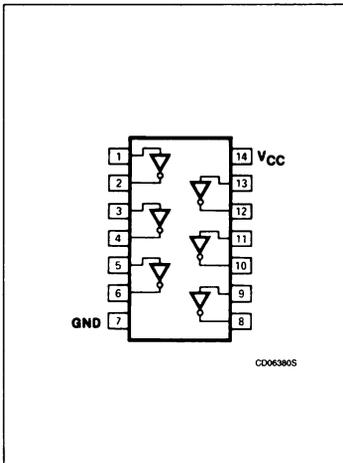
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A	Input	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

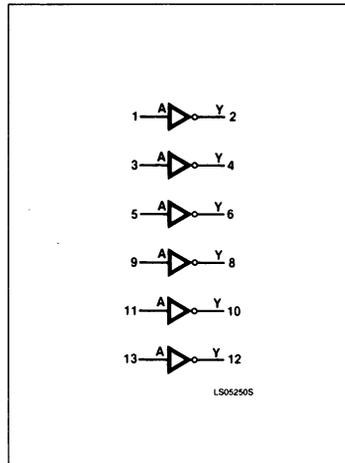
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

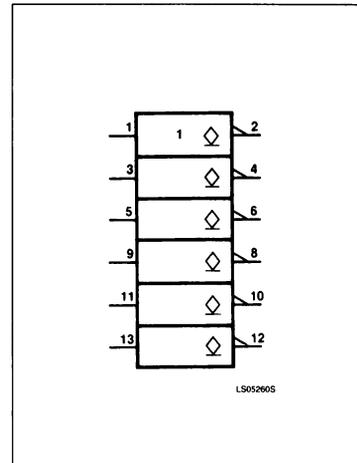
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Inverters

7405, LS05, S05

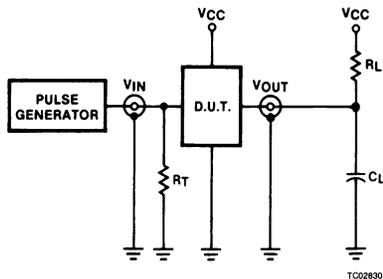
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70			°C

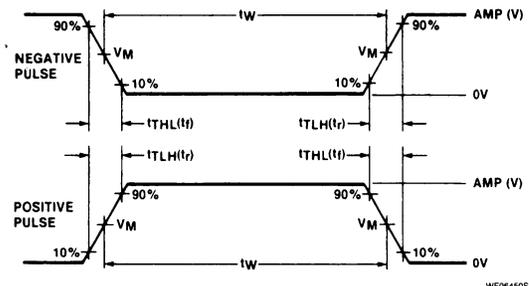
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC}	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	2.0			2.0			2.0			V
V _{IL}			+0.8			+0.8			+0.8	V
I _{IK}			-12			-18			-18	mA
V _{OH}			5.5			5.5			5.5	V
I _{OL}			16			8			20	mA
T _A	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Inverters

7405, LS05, S05

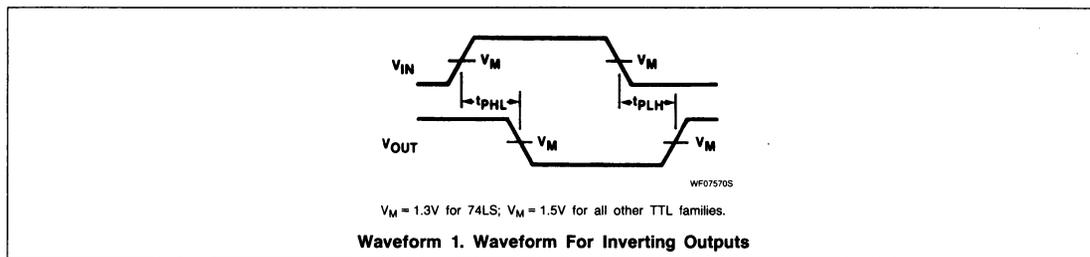
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7405			74LS05			74S05			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
I_{OH}	HIGH-level output current $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$			250			100			250	μA
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$		0.2	0.4	0.35	0.5			0.5	V
		$I_O = 4\text{mA}$ (74LS)				0.25	0.4				
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5			-1.5			-1.2	V
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$			1.0					1.0	mA
		$V_I = 7.0\text{V}$					0.1				mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$			40						μA
		$V_I = 2.7\text{V}$					20			50	μA
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$			-1.6		-0.4				mA
		$V_I = 0.5\text{V}$								-2.0	mA
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}$	Outputs HIGH I_{CCH}		6	12	1.2	2.4	9	19.8		mA
		Outputs LOW I_{CCL}		18	33	3.6	6.6	30	54		mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}, R_L = 400\Omega$		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}, R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay For 7405 only, $R_L = 4\text{k}\Omega$ for t_{PLH} Waveform 1		55 15		32 28	7.5 7.0		ns

7406, 07 Inverter/Buffer/Drivers

'06 Hex Inverter Buffer/Driver (Open Collector)

'07 Hex Buffer/Driver (Open Collector)

Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7406	10ns (t_{PLH}) 15ns (t_{PHL})	31mA
7407	6ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7406N, N7407N
Plastic SO	N7406D, N7407D

FUNCTION TABLE

'06		'07	
INPUT	OUTPUT	INPUT	OUTPUT
A	Y	A	Y
H	L	H	H
L	H	L	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

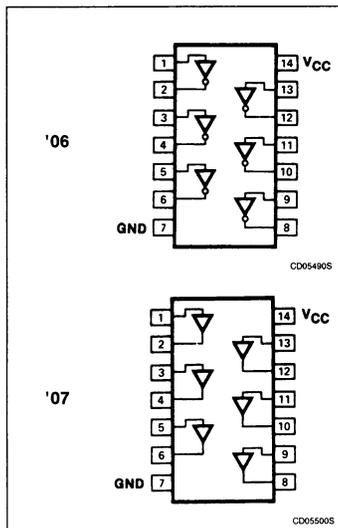
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
A	Input	1ul
Y	Output	10ul

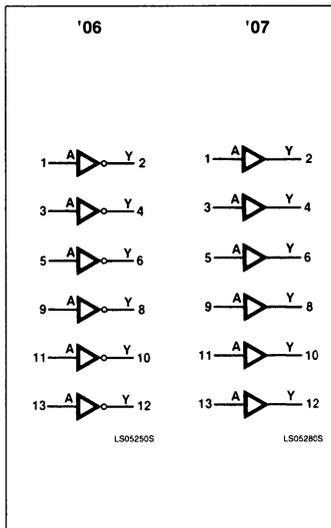
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

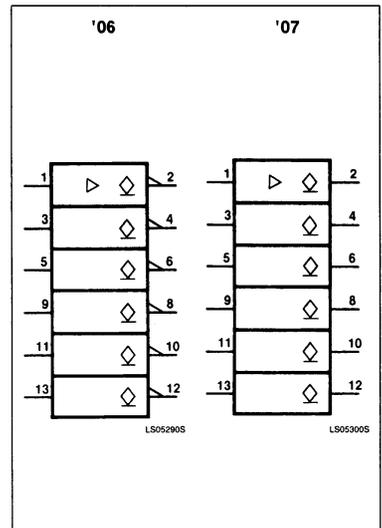
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Inverter/Buffer/Drivers

7406, 07

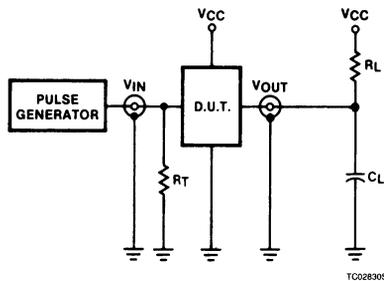
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +30	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
V _{OH} HIGH-level output voltage			30	V
I _{OL} LOW-level output current			40	mA
T _A Operating free-air temperature	0		70	°C

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collectors Outputs

DEFINITIONS

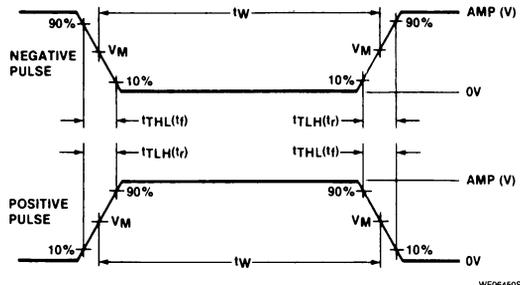
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Inverter/Buffer/Drivers

7406, 07

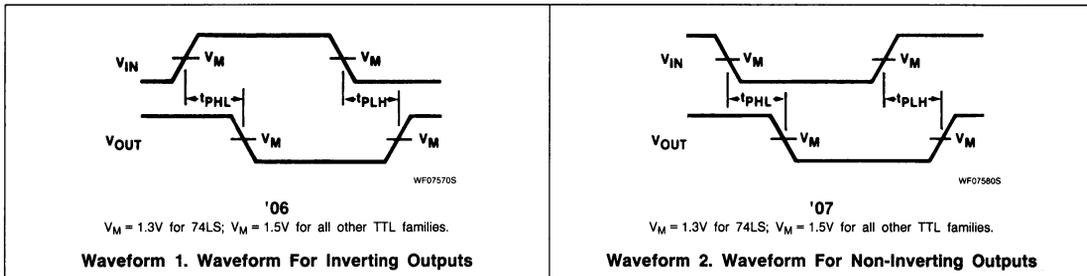
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7406, 7407			UNIT	
		Min	Typ ²	Max		
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 30V			250	μA	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = 16mA		0.4	V	
		I _{OL} = 30mA		0.7	V	
		I _{OL} = 40mA		0.7	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	'06	30	48	mA
		I _{CCL} Outputs LOW		32	51	mA
		I _{CCH} Outputs HIGH	'07	29	41	mA
		I _{CCL} Outputs LOW		21	30	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORMS



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	7406		7407		UNIT
		C _L = 15pF, R _L = 110Ω		C _L = 15pF, R _L = 110Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1, '06 Waveform 2, '07		15 23		10 30	ns

7408, LS08, S08 Gates

Quad Two-Input AND Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7408	15ns	16mA
74LS08	9ns	3.4mA
74S08	5ns	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7408N, N74LS08N, N74S08N
Plastic SO	N74LS08N, N74S08N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

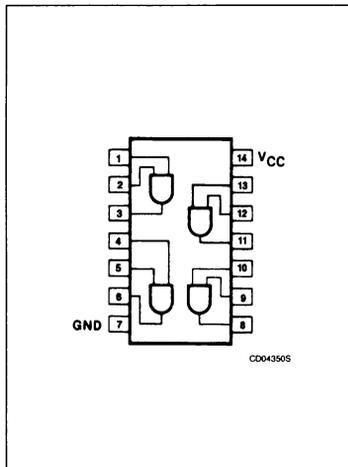
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

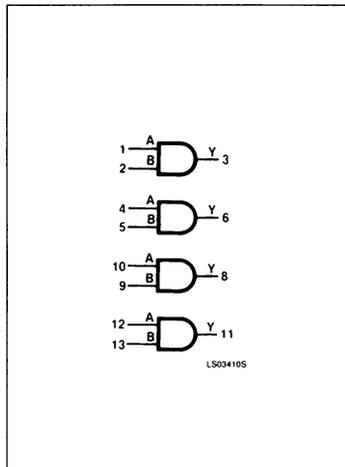
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

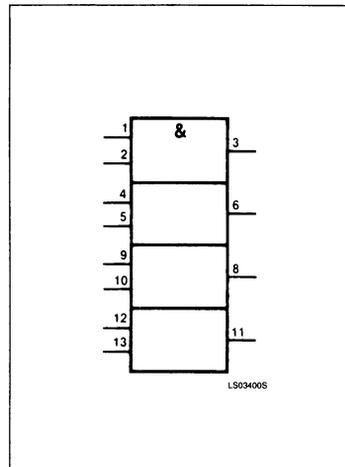
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7408, LS08, S08

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

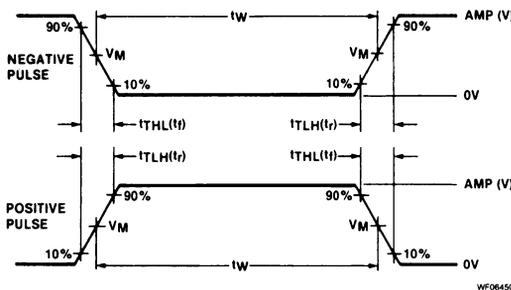
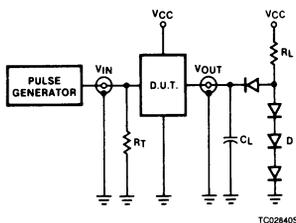
PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

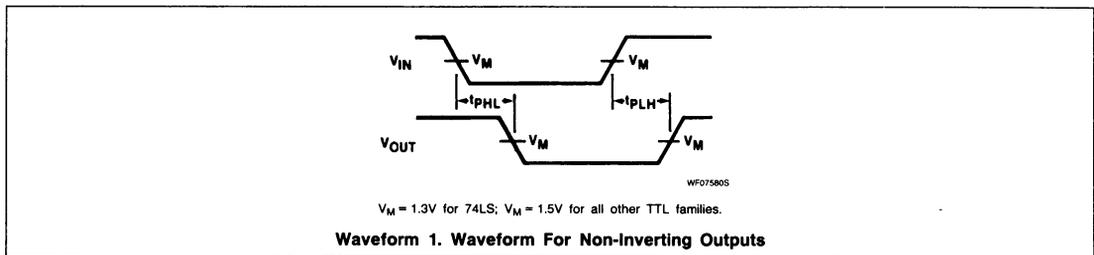
7408, LS08, S08

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7408			74LS08			74S08			UNIT				
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max					
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OH} = MAX			2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX	I _{OL} = MAX				0.2	0.4		0.35	0.5		0.5	V	
			I _{OL} = 4mA (74LS)							0.25	0.4				V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5			-1.5			-1.2	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V										1.0	mA	
			V _I = 7.0V							0.1					mA
I _{IH}	HIGH-level input current	V _{CC} = MAX	V _I = 2.4V										40	μA	
			V _I = 2.7V							20				50	μA
I _{IL}	LOW-level input current	V _{CC} = MAX	V _I = 0.4V										-1.6	mA	
			V _I = 0.5V											-2.0	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX			-18		-55	-20		-100	-40		-100	mA	
I _{CC}	Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH				11	21		2.4	4.8		18	32	mA
			I _{CCL} Outputs LOW				20	33		4.4	8.8		32	57	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM**AC ELECTRICAL CHARACTERISTICS** T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		27 19		15 20		7.0 7.5	ns

74LS09 Gates

Quad Two-Input AND Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS09	23ns	4.3

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS09N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

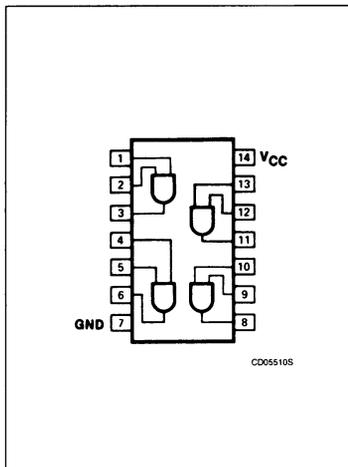
PINS	DESCRIPTION	74LS
A, B	Inputs	1LSul
Y	Output	10LSul

NOTE:

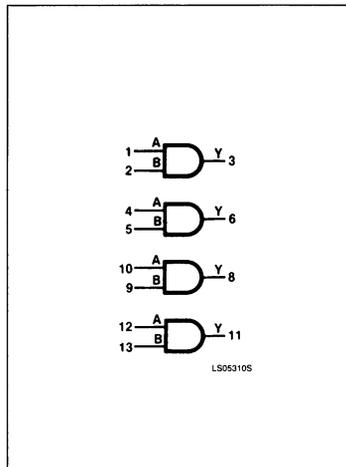
Where 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

5

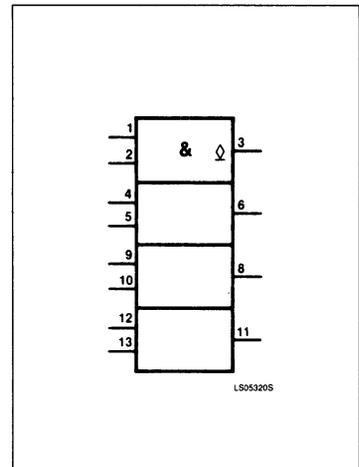
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

74LS09

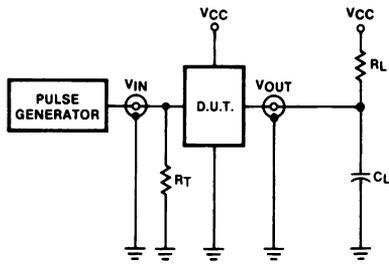
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

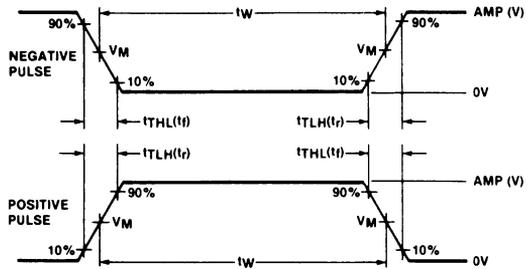
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
V _{OH} HIGH-level output voltage			5.5	V
I _{OL} LOW-level output current			8	mA
T _A Operating free-air temperature	0		70	°C

TEST CIRCUITS AND WAVEFORMS



TC028305



WF064505

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Open Collector Outputs

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

74LS09

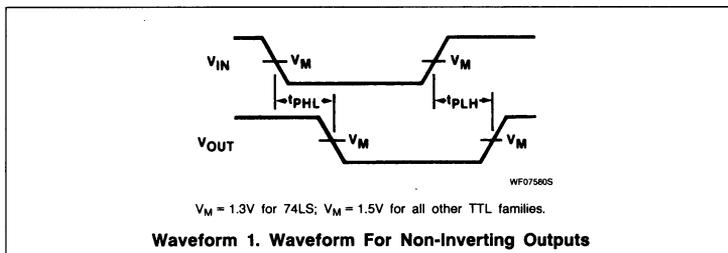
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS09			UNIT
		Min	Typ ²	Max	
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, V _{OH} = MAX			250	μA
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 4mA		0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = 18mA			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	2.4	4.8	mA
		I _{CCL} Outputs LOW	4.4	8.8	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM



5

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		35 35	ns

7410, 7411, LS10, LS11, S10, S11 Gates

Logic Products

Triple Three-Input NAND ('10), AND ('11) Gates
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7410	9ns	6mA
74LS10	10ns	1.2mA
74S10	3ns	12mA
7411	10ns	11mA
74LS11	9ns	2.6mA
74S11	5ns	19mA

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y('10)	Y('11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = HIGH voltage level
L = LOW voltage level

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP '10	N7410N, N74LS10N, N74S10N
'11	N7411N, N74LS11N, N74S11N
Plastic SO '10	N74LS10D, N74S10D
Plastic SO '11	N74LS11D, N74S11D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

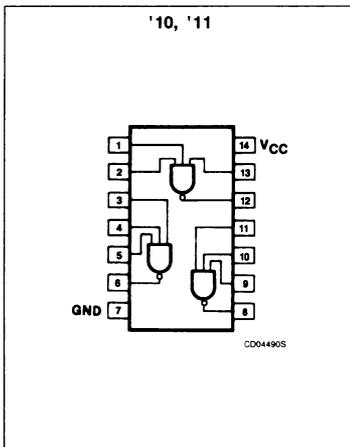
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A - C	Inputs	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

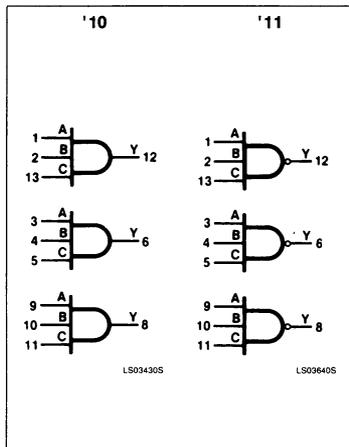
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

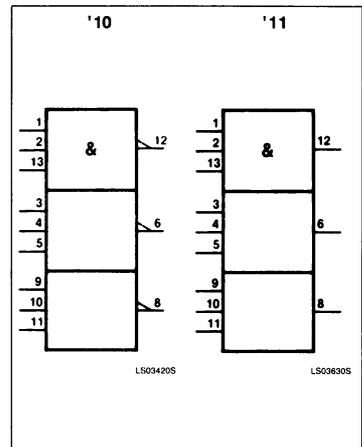
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7410, 7411, LS10, LS11, S10, S11

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperatures unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current	'10			-400			-400			-1000	μA
	'11			-800			-400			-1000	μA
I _{OL} LOW-level output current	Com'l			16			8			20	mA
T _A Operating free-air temperature	Com'l	0		70	0		70	0		70	°C

Gates

7410, 7411, LS10, LS11, S10, S11

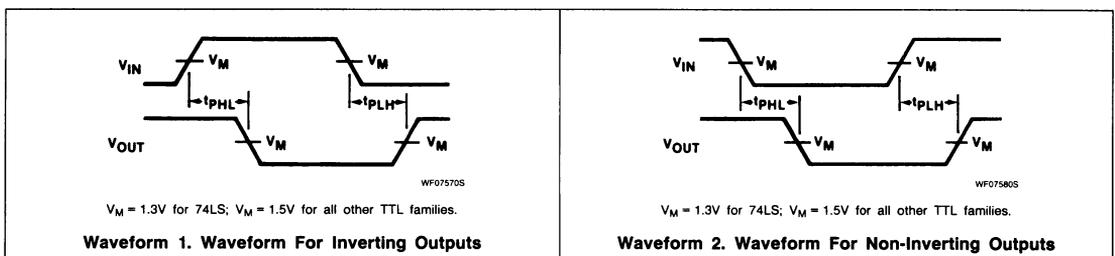
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7410, 11			74LS10, 11			74S10, 11			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN		I _{OL} = MAX	0.2	0.4		0.35	0.5		0.5	V	
			I _{OL} = 4mA (74LS)				0.25	0.4			V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			-1.2	V
I _I	Input current at maximum input voltage V _{CC} = MAX		V _I = 5.5V		1.0					1.0	mA	
			V _I = 7.0V					0.1			mA	
I _{IH}	HIGH-level input current V _{CC} = MAX		V _I = 2.4V		40						μA	
			V _I = 2.7V					20		50	μA	
I _{IL}	LOW-level input current V _{CC} = MAX		V _I = 0.4V		-1.6			-0.4			mA	
			V _I = 0.5V							-2.0	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-55	-20		-100	-40		-100	mA	
I _{CC}	Supply current (total) V _{CC} = MAX	'10	I _{CCH} Outputs HIGH	3	6		0.6	1.2		7.5	12	mA
			I _{CCL} Outputs LOW	9	16.5		1.8	3.3		15	27	mA
		'11	I _{CCH} Outputs HIGH	6	12		1.8	3.6		13.5	24	mA
			I _{CCL} Outputs LOW	15	20		3.3	6.6		24	42	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



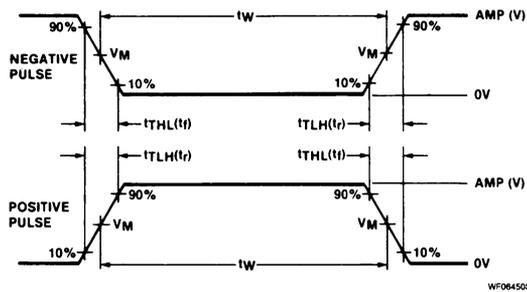
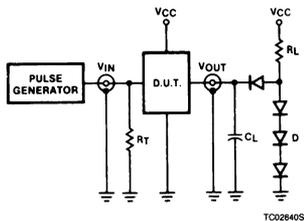
Gates

7410, 7411, LS10, LS11, S10, S11

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1, '10		22 15		15 15		4.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay Waveform 2, '11		27 19		15 20		7.0 7.5	ns

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definitions

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7413, LS13 Gates

Dual 4-Input NAND Schmitt Trigger Product Specification

Logic Products

DESCRIPTION

The '13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{I+MAX} , the gate will respond in the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7413	17ns	17mA
74LS13	17ns	3.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7413N, N74LS13N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

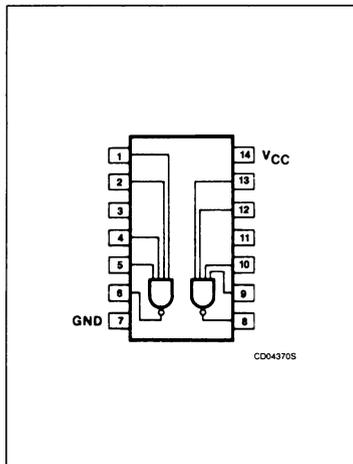
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

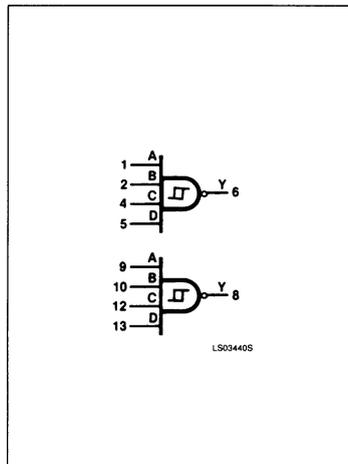
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

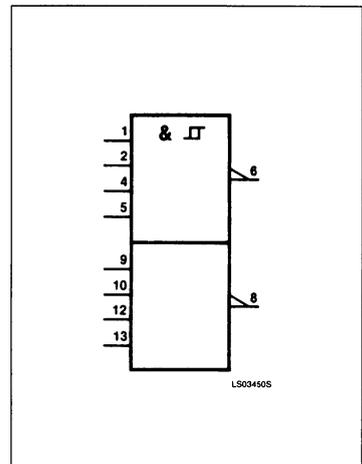
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7413, LS13

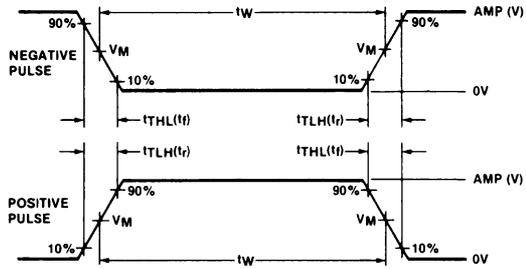
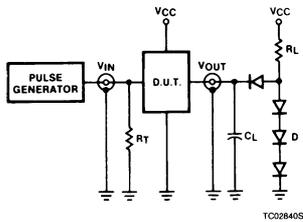
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{PLH}, t_{PLL} Values should be less than or equal to the table entries.

Input Pulse Definitions

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{PLH}	t _{PLL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

7413, LS13

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7413			74LS13			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{T+} Positive-going threshold	V _{CC} = 5.0V	1.5	1.7	2.0	1.4	1.6	1.9	V
V _{T-} Negative-going threshold	V _{CC} = 5.0V	0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV _T Hysteresis (V _{T+} - V _{T-})	V _{CC} = 5.0V	0.4	0.8		0.4	0.8		V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _I = V _{T-MIN} , I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _I = V _{T+MAX}	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _{T+} Input current at positive-going threshold	V _{CC} = 5.0V, V _I = V _{T+}		-0.65			-0.14		mA
I _{T-} Input current at negative-going threshold	V _{CC} = 5.0V, V _I = V _{T-}		-0.85			-0.18		mA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA
		V _I = 7.0V					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA
		V _I = 2.7V					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18	-55	-20		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		14	23	2.9	6	mA
		I _{CCL} Outputs LOW		20	32	4.1	7	mA

NOTES:

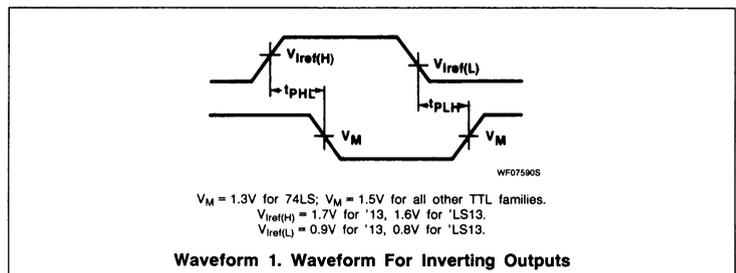
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

AC WAVEFORM



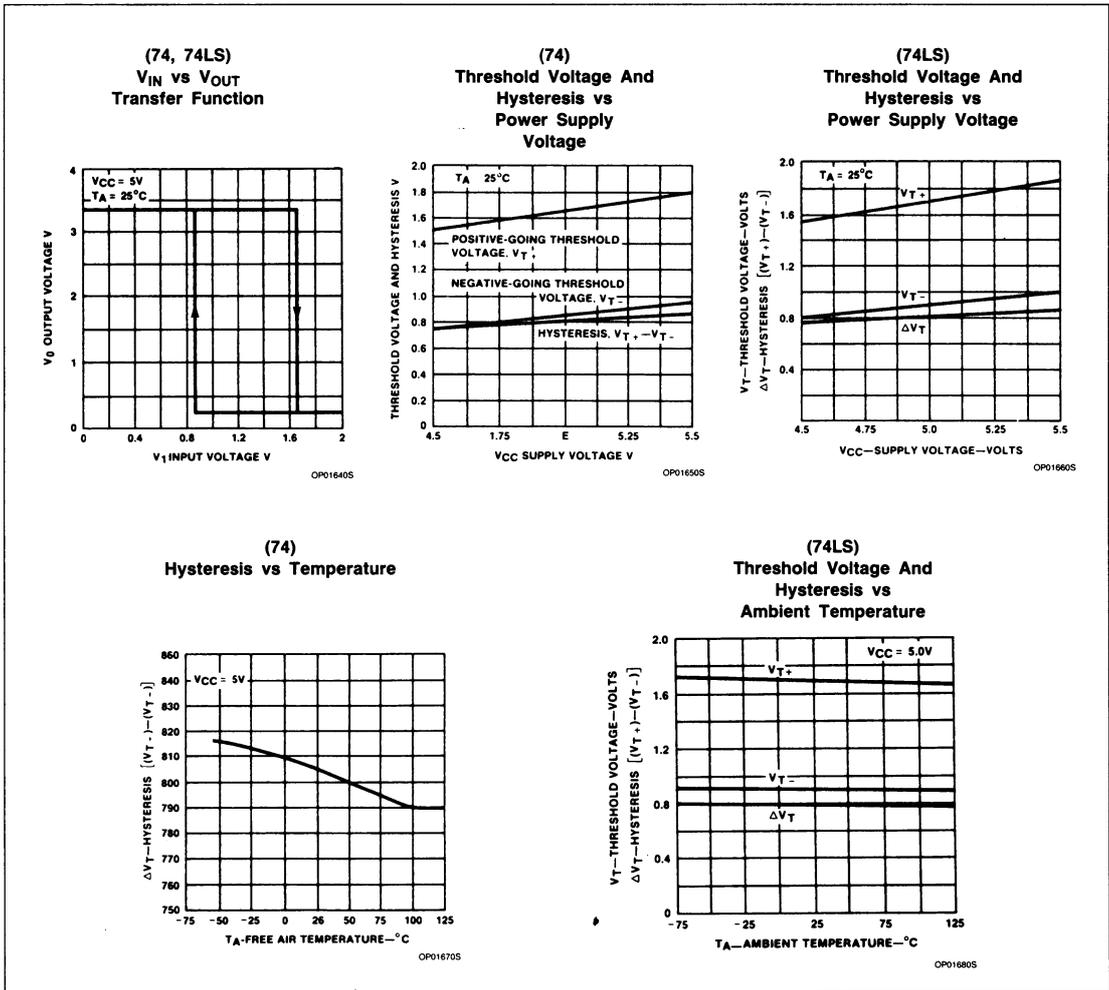
Gates

7413, LS13

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		27 22	22 27	ns

TYPICAL PERFORMANCE CHARACTERISTICS



5

7414, LS14 Schmitt Triggers

Hex Inverter Schmitt Trigger Product Specification

Logic Products

DESCRIPTION

The '14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7414	15ns	31mA
74LS14	15ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7414N, N74LS14N
Plastic SO	N74LS14D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

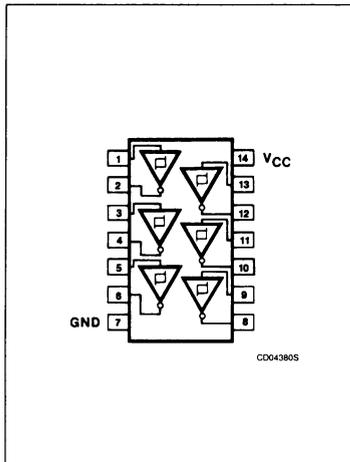
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
A	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

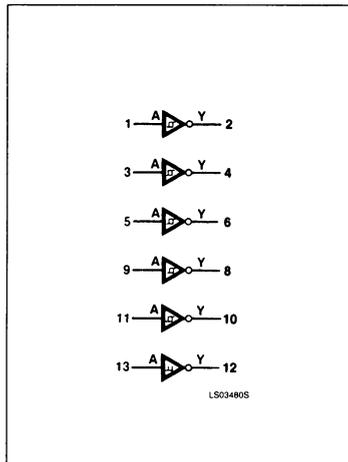
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

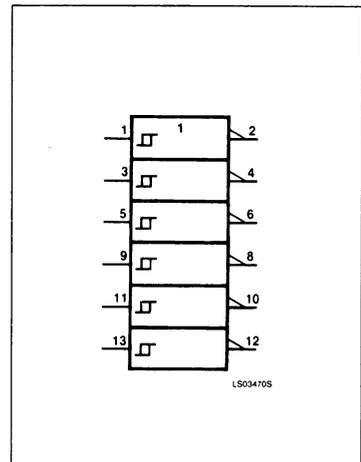
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Schmitt Triggers

7414, LS14

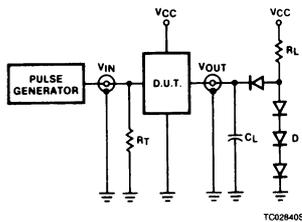
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

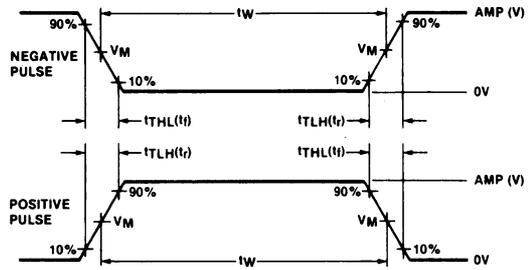
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



TC028405



WF064505

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Schmitt Triggers

7414, LS14

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7414			74LS14			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{T+} Positive-going threshold	V _{CC} = 5.0V	1.5	1.7	2.0	1.4	1.6	1.9	V	
V _{T-} Negative-going threshold	V _{CC} = 5.0V	0.6	0.9	1.1	0.5	0.8	1.0	V	
ΔV _T Hysteresis (V _{T+} - V _{T-})	V _{CC} = 5.0V	0.4	0.8		0.4	0.8		V	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _I = V _{T-MIN} , I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _I = V _{T+MAX}	I _{OL} = MAX		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _{T+} Input current at positive-going threshold	V _{CC} = 5.0V, V _I = V _{T+}		-0.43			-0.14		mA	
I _{T-} Input current at negative-going threshold	V _{CC} = 5.0V, V _I = V _{T-}		-0.56			-0.18		mA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0				mA	
		V _I = 7.0V					0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40				μA	
		V _I = 2.7V					20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.2			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		22	36		8.6	16	mA
		I _{CCL} Outputs LOW		39	60		12	21	mA

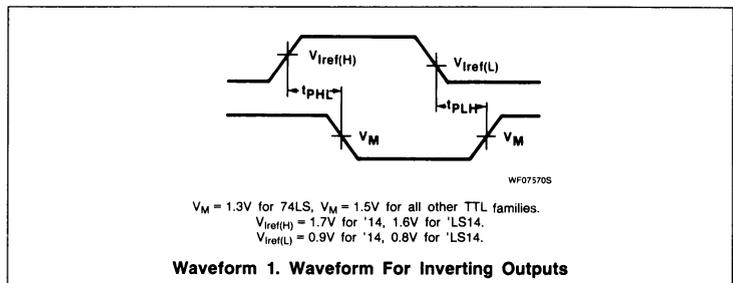
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

FUNCTION TABLE

INPUT	OUTPUT
A	Y
0	1
1	0

AC WAVEFORM



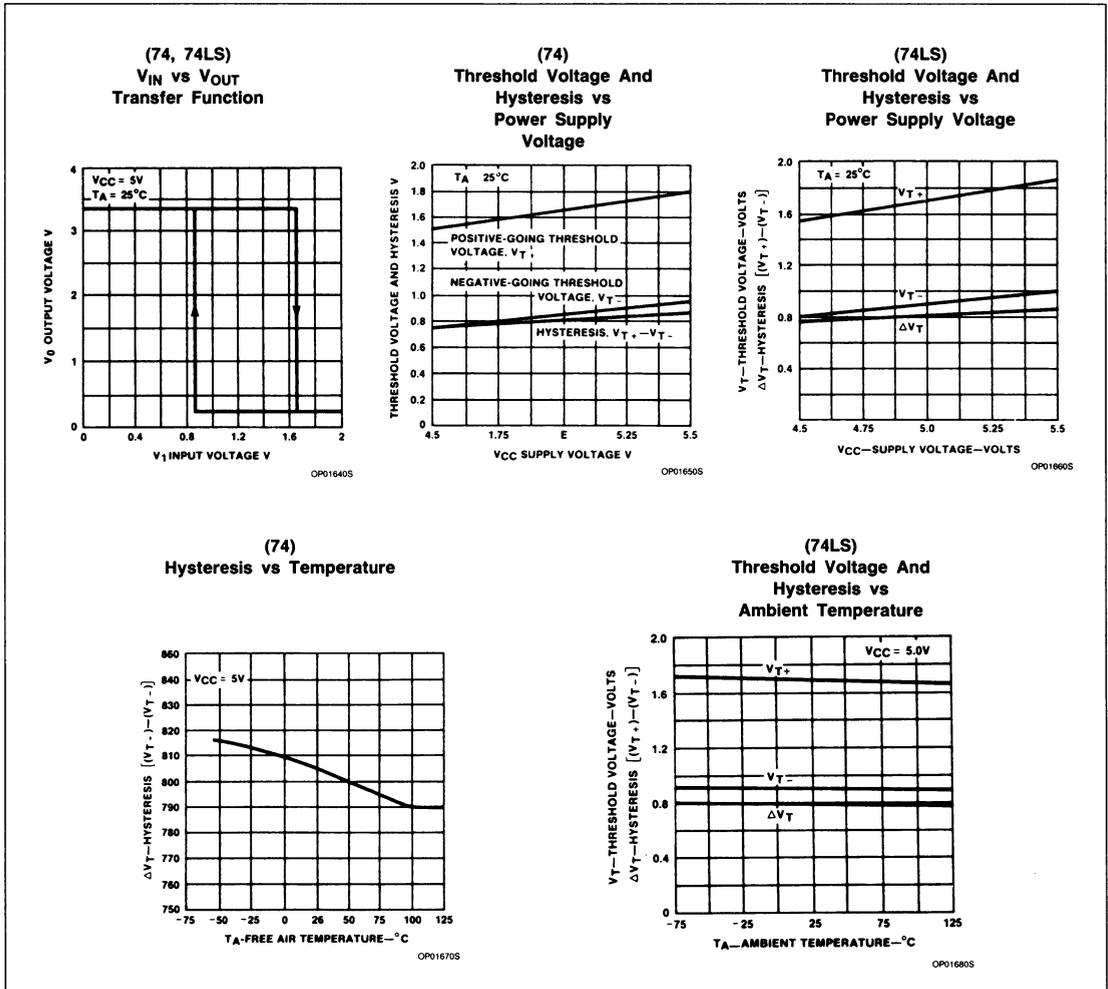
Schmitt Triggers

7414, LS14

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22	22	ns

TYPICAL PERFORMANCE CHARACTERISTICS



7416, 17 Inverter/Buffer/Drivers

'16 Hex Inverter Buffer/Driver (Open Collector)
'17 Hex Buffer/Driver (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7416	10ns (t_{PLH}) 15ns (t_{PHL})	31mA
7417	6ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7416N, N7417N
Plastic SO	N7417D

FUNCTION TABLE

'16		'17	
INPUT	OUTPUT	INPUT	OUTPUT
A	Y	A	Y
L	H	L	L
H	L	H	H

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

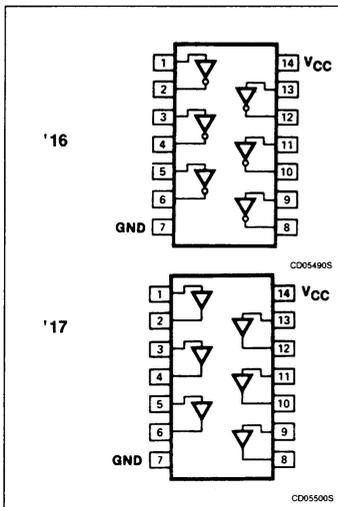
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
A	Input	1ul
Y	Output	10ul

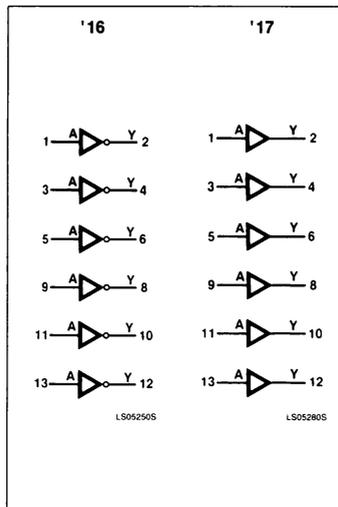
NOTE:

A 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

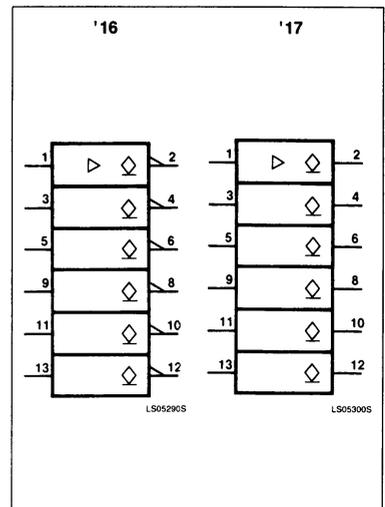
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Inverter/Buffer/Drivers

7416, 17

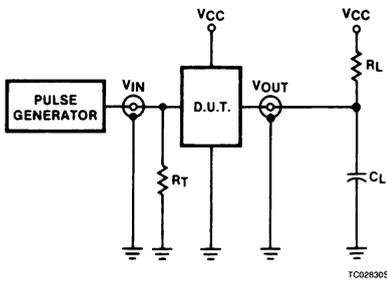
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +15	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
V _{OH} HIGH-level output voltage			15	V
I _{OL} LOW-level output current			40	mA
T _A Operating free-air temperature	0		70	°C

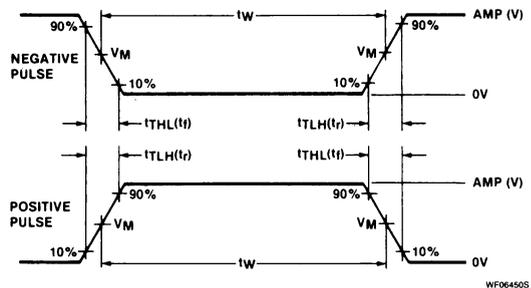
TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Inverter/Buffer/Drivers

7416, 17

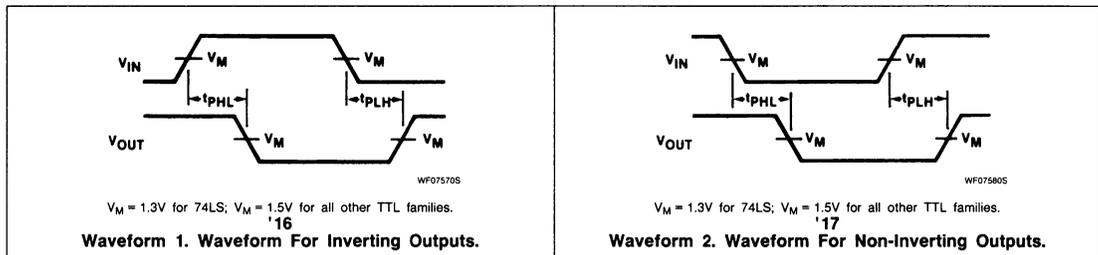
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7416, 7417			UNIT	
		Min	Typ ²	Max		
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 15\text{V}$			250	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = 16\text{mA}$		0.4	V	
		$I_{OL} = 30\text{mA}$				
		$I_{OL} = 40\text{mA}$		0.7	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA	
I_{CC} Supply current (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	'16	30	48	mA
		I_{CCL} Outputs LOW		32	51	mA
		I_{CCH} Outputs HIGH	'17	29	41	mA
		I_{CCL} Outputs LOW		21	30	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORMS



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	7416		7417		UNIT
		$C_L = 15\text{pF}, R_L = 110\Omega$		$C_L = 15\text{pF}, R_L = 110\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1, '16 Waveform 2, '17		15 23		10 30	ns

7420, 7421, LS20, LS21, S20 Gates

Logic Products

Dual Four-Input NAND ('20) AND ('21) Gate
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7420	10ns	8mA
74LS20	10ns	0.8mA
74S20	3ns	8mA
7421	12ns	8mA
74LS21	9ns	1.7mA

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y('20)	Y('21)
L	X	X	X	H	L
X	L	X	X	H	L
X	X	L	X	H	L
X	X	X	L	H	L
H	H	H	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP '20	N7420N, N74LS20N, N74S20N
'21	N7421N, N74LS21N
Plastic SO	N74LS20D, N74S20D, N74LS21D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

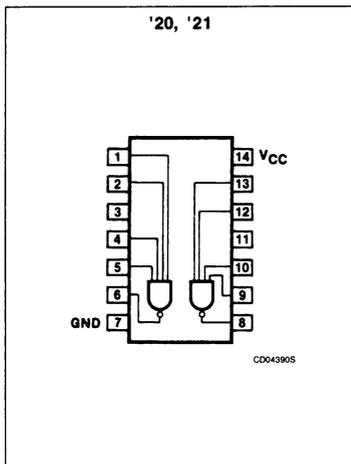
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A - D	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

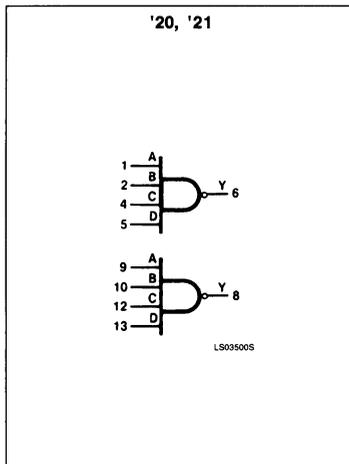
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

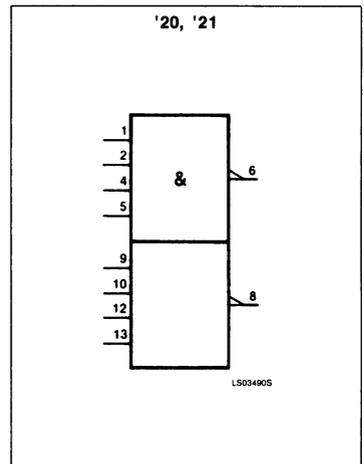
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7420, 7421, LS20, LS21, S20

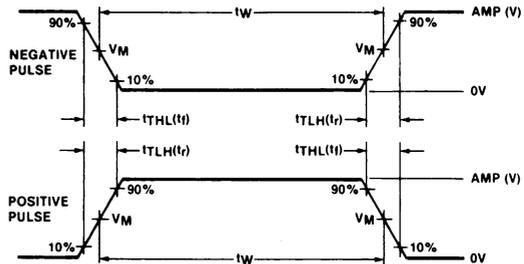
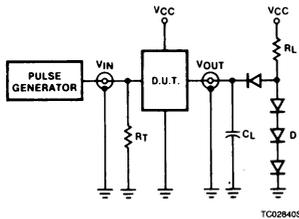
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current	'20		-400			-400			-1000	μA
	'21		-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

7420, 7421, LS20, LS21, S20

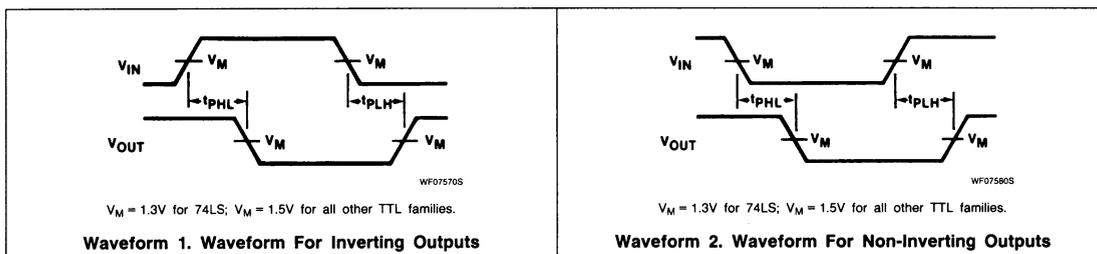
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7420, 21			74LS20, 21			74S20			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V		
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX				0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)							0.25	0.4			V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			-1.2	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V				1.0					1.0	mA	
		V _I = 7.0V							0.1			mA	
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V				40						μA	
		V _I = 2.7V							20		50	μA	
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V				-1.6			-0.4			mA	
		V _I = 0.5V									-2.0	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-55	-20			-100	-40		-100	mA	
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CC} H Outputs HIGH	'20	2	4		0.4	0.8		5	8	mA	
				I _{CC} L Outputs LOW	6	11		1.2	2.2		10	18	mA
		I _{CC} H Outputs HIGH	'21	6	8		1.2	2.4					mA
				I _{CC} L Outputs LOW	11	13		2.2	4.4				

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



Gates

7420, 7421, LS20, LS21, S20

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1, '20		22 15		15 15		4.5 5.0	ns
t_{PLH} t_{PHL} Propagation delay	Waveform 2, '21		27 19		15 20			ns

7425 Gate

Dual Four-Input NOR Gate With Strobe Product Specification

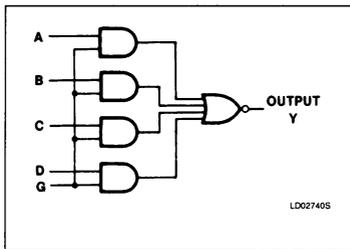
Logic Products

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
X	X	X	X	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7425	9ns	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7425N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

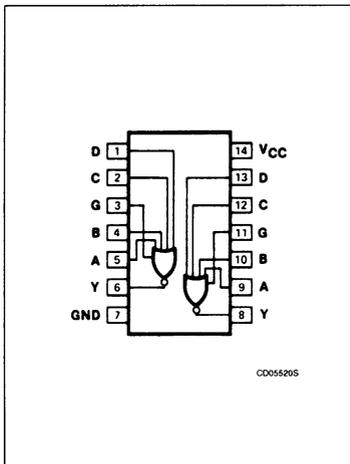
PINS	DESCRIPTION	74
A - D	Inputs	1ul
G	Input	4ul
Y	Output	10ul

NOTE:

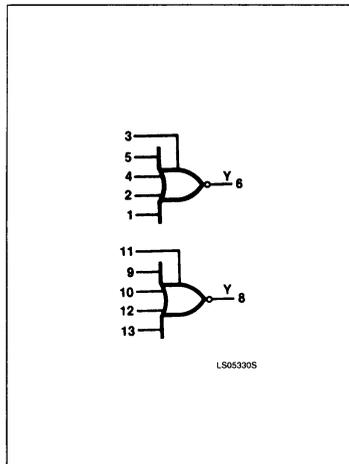
Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

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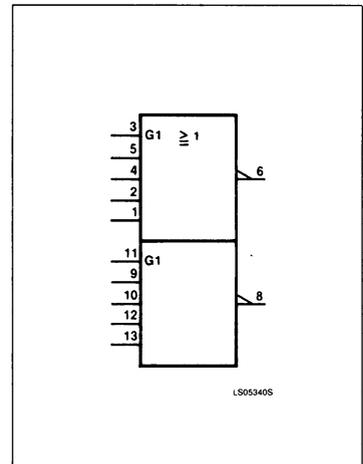
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

7425

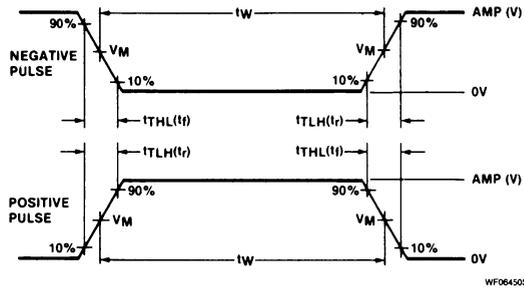
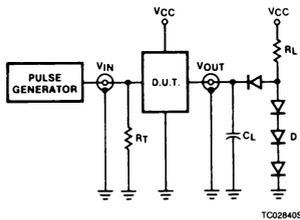
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

7425

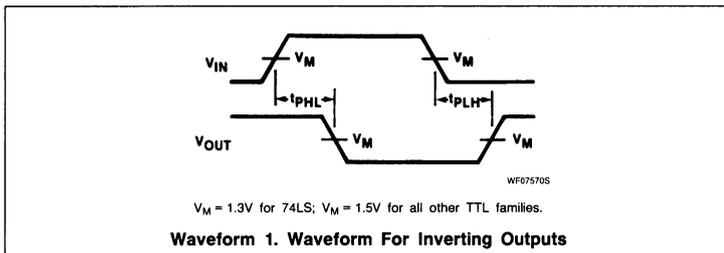
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7425			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	G input		160	μA
		Other inputs		40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	G input		-6.4	mA
		Other inputs		-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	8	16	mA
		I _{CCL} Outputs LOW	10	19	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX+0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15	ns

7426, LS26 Gates

Quad Two-Input NAND Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7426	14ns	8mA
74LS26	16ns	1.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7426N, N74LS26N
Plastic SO	N74LS26D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

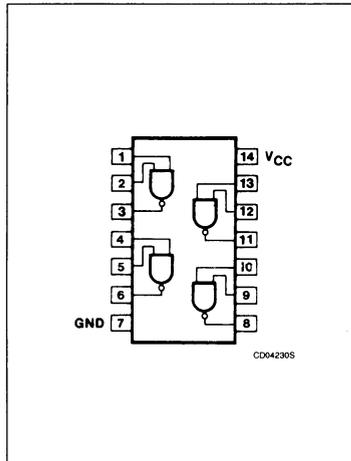
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
A,B	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

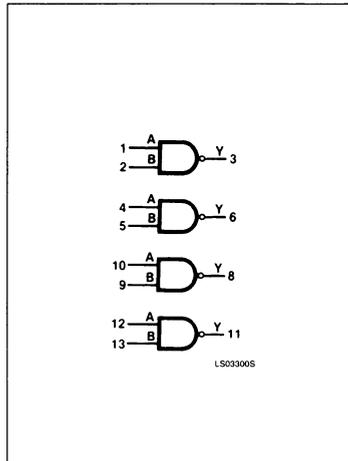
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$ and a 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

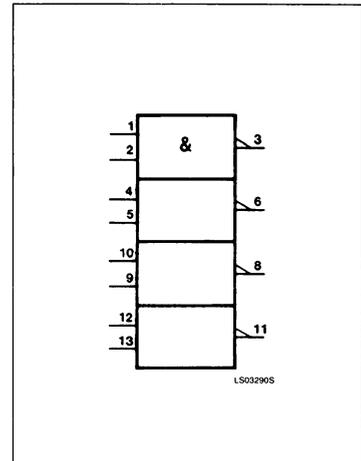
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7426, LS26

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

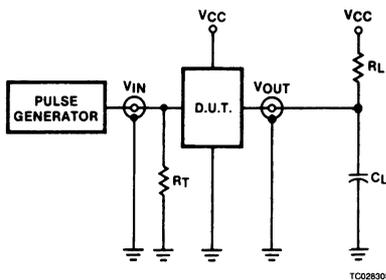
PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +15	-0.5 to +15	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

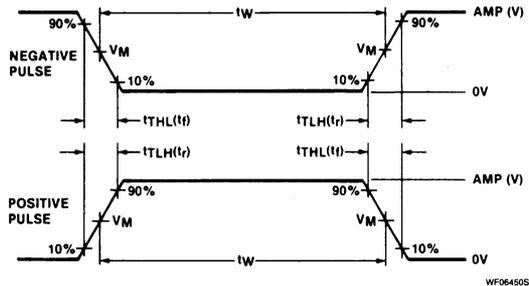
PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			15			15	V
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

7426, LS26

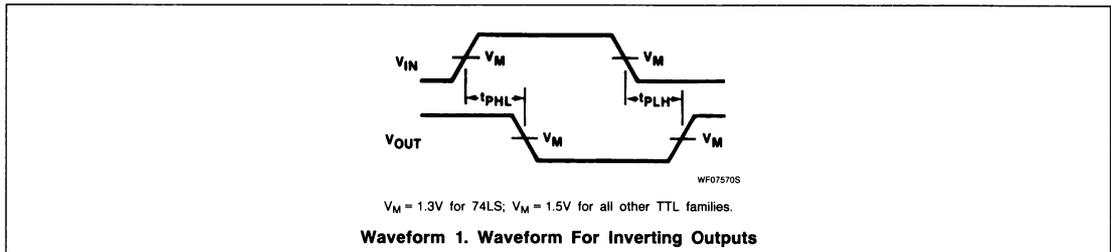
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7426			74LS26			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
I _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX			1000			1000	μA
				50			50	μA
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN			0.2	0.4	0.35	0.5	V
						0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX			1.0				mA
							0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX			40				μA
							20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		4	8	0.8	1.6	mA
		I _{CCL} Outputs LOW		12	22	2.4	4.4	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 1kΩ		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay	Waveform 1				ns
			24 17		32 28	

7427, LS27 Gates

Triple Three-Input NOR Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7427	9ns	13mA
74LS27	10ns	2.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7427N, N74LS27N
Plastic SO	N74LS27D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

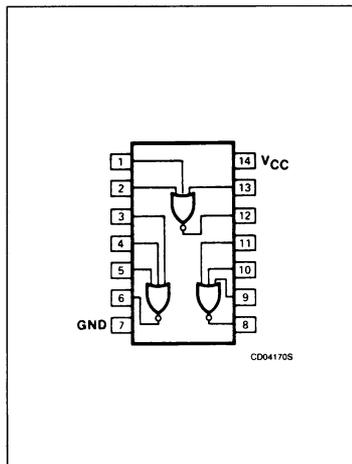
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
A - C	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

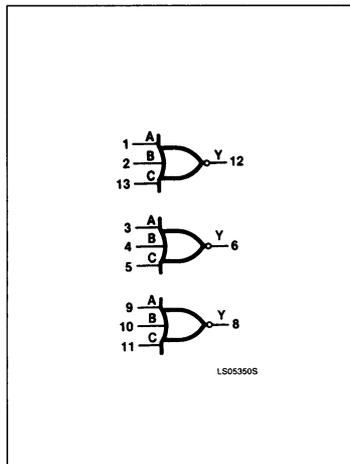
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74LS unit load (LSuI) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

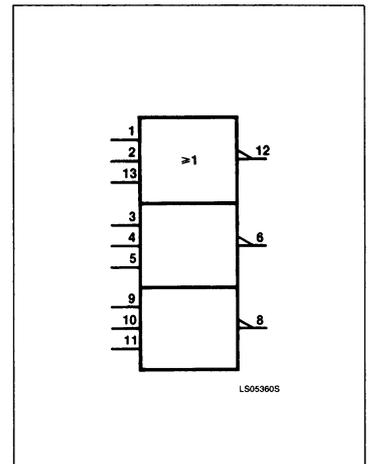
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7427, LS27

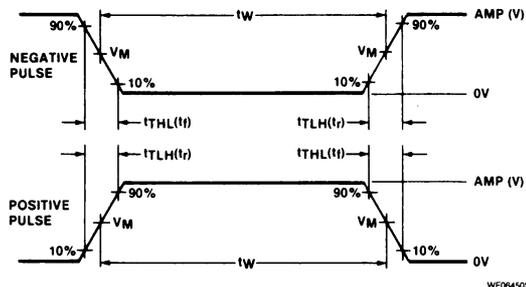
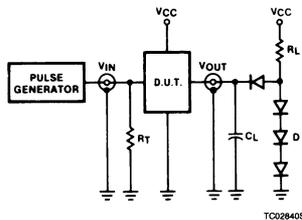
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-800			-400	μA
I _{OL}	LOW-level output current			16			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

7427, LS27

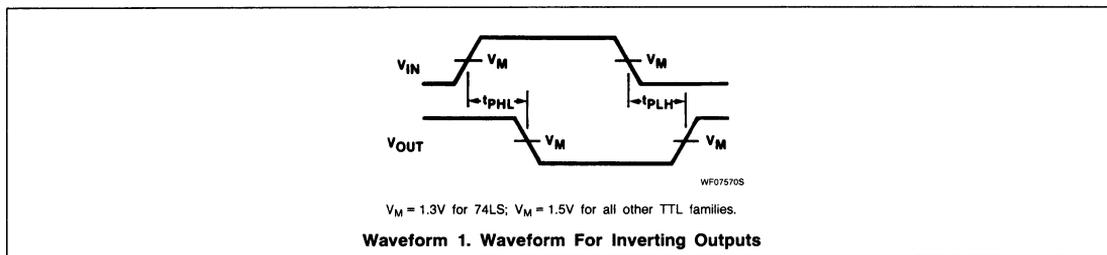
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7427			74LS27			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX				0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)						0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0		mA	
		V _I = 7.0V						0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V					40		μA	
		V _I = 2.7V						20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-55	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH				10	16	2.0	4	mA
		I _{CC} L Outputs LOW				16	26	3.4	6.8	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		15 11		15 15	ns

7428 Buffer

Quad Two-Input NOR Buffer
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7428	7ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7428N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

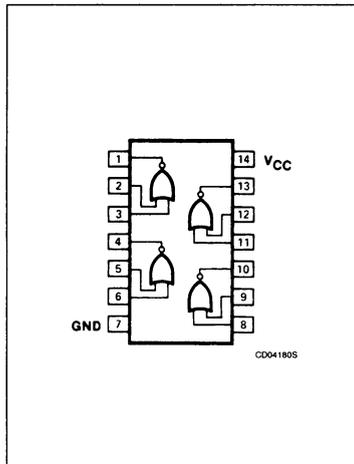
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
A, B	Inputs	1ul
Y	Output	30ul

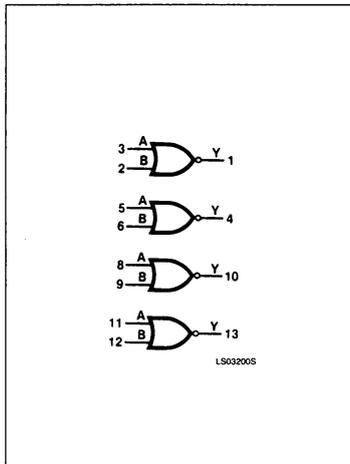
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

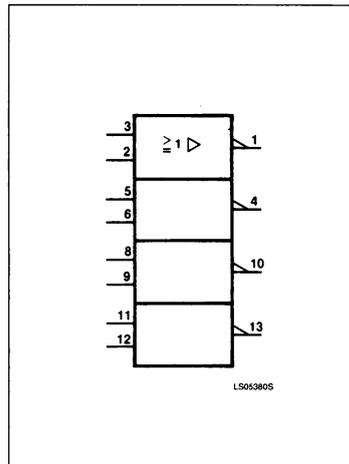
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffer

7428

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

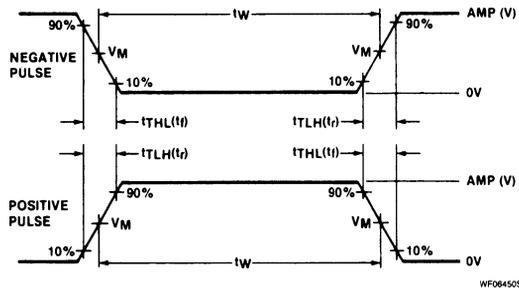
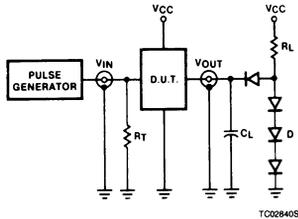
PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
I _{OH} HIGH-level output current			-2400	μA
I _{OL} LOW-level output current			48	mA
T _A Operating free-air temperature	0		70	°C

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TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffer

7428

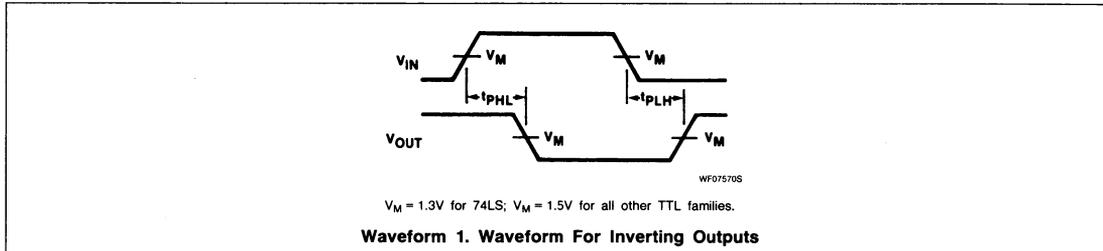
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7428			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-70		-180	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	12	21	mA
		I _{CCL} Outputs LOW	33	57	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		R _L = 133Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1 C _L = 50pF		9.0 12	ns
t _{PLH} t _{PHL} Propagation delay	Waveform 1 C _L = 150pF		15 18	ns

7430, LS30 Gates

Eight-Input NAND Gate Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7430	11ns	2mA
74LS30	11ns	0.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7430N, N74LS30N
Plastic SO	N74LS30D

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

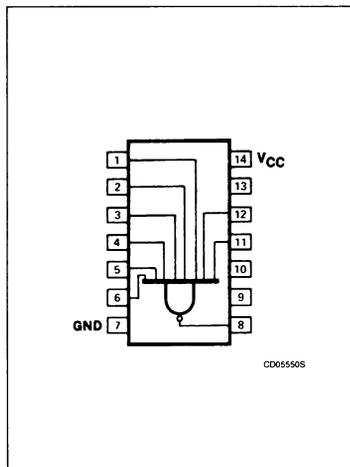
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
A - H	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

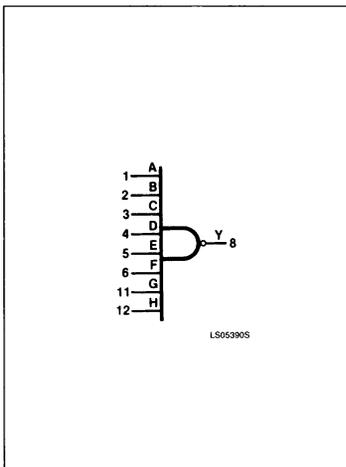
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

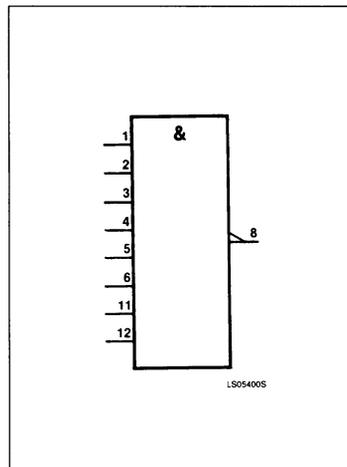
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7430, LS30

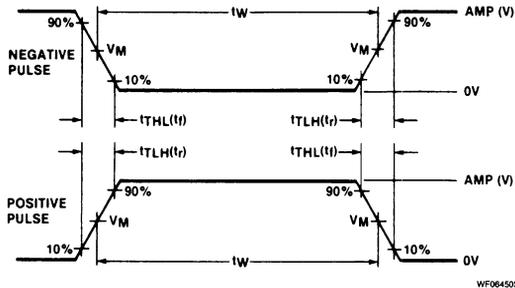
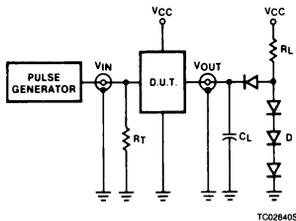
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-400			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

7430, LS30

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

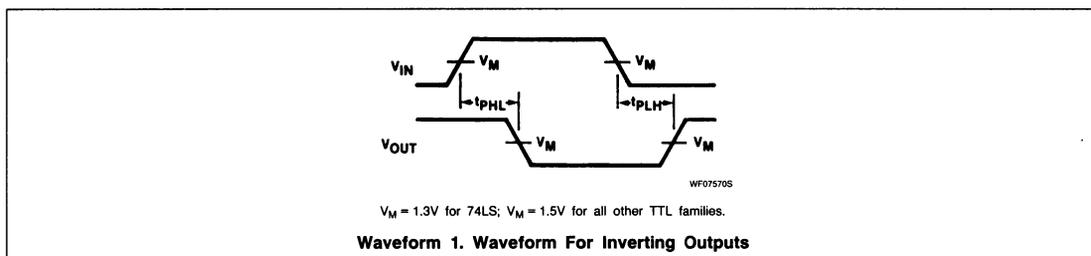
PARAMETER	TEST CONDITIONS ¹	7430			74LS30			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA
		V _I = 7.0V					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA
		V _I = 2.7V					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-20		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		1	2	0.35	0.5	mA
		I _{CCL} Outputs LOW		3	6	0.6	1.1	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15		15 20	ns

7432, LS32, S32 Gates

Quad Two-Input OR Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7432	12ns	19mA
74LS32	14ns	4.0mA
74S32	4ns	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7432N, N74LS32N, N74S32N
Plastic SO-14	N74LS32D, N74S32D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

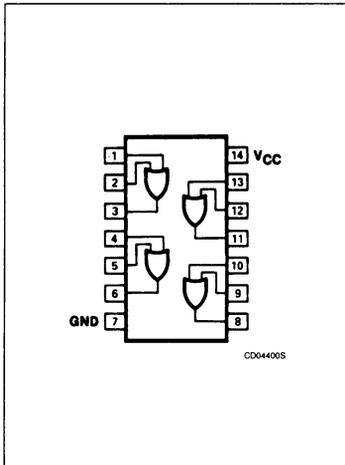
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

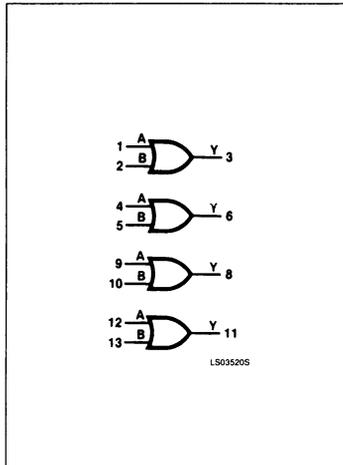
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL}

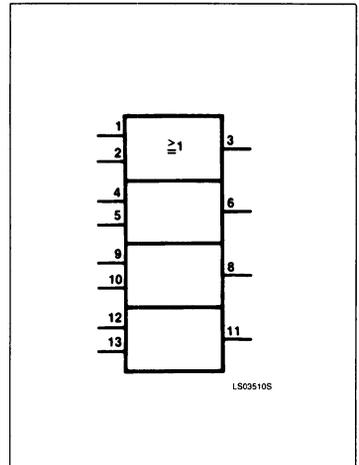
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7432, LS32, S32

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

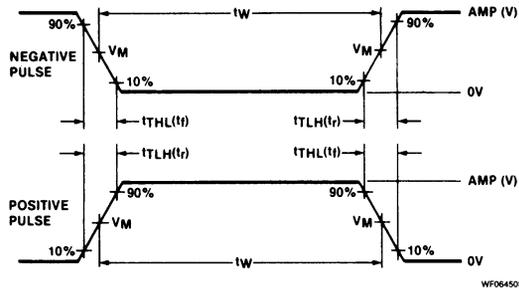
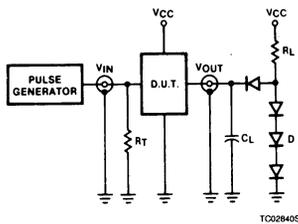
PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

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TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{LH}, t_{HL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS					
	Amplitude	Rep. Rate	Pulse Width	t _{LH}	t _{HL}	
74	3.0V	1MHz	500ns	7ns	7ns	
74LS	3.0V	1MHz	500ns	15ns	6ns	
74S	3.0V	1MHz	500ns	2.5ns	2.5ns	

Gates

7432, LS32, S32

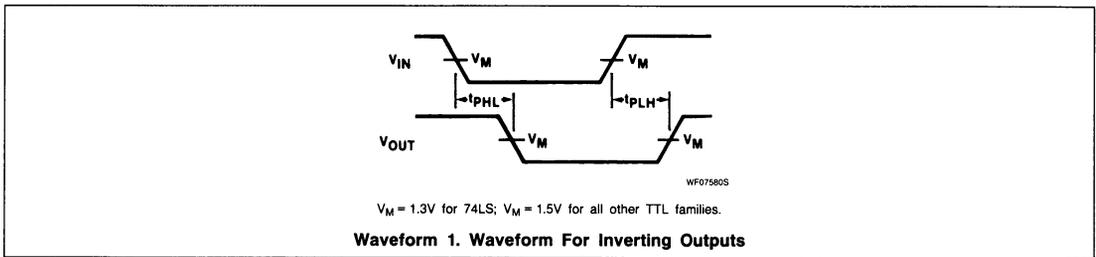
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7432			74LS32			74S32			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V		
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IL} = MAX	I _{OL} = MAX			0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA (74LS)						0.25	0.4			V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			-1.2	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V				1.0					1.0	mA	
		V _I = 7.0V						0.1				mA	
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V				40						μA	
		V _I = 2.7V						20			50	μA	
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V				-1.6			-0.4			mA	
		V _I = 0.5V									-2.0	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-55	-20		-100	-40		-100	mA		
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CCH} Outputs HIGH			15	22		3.1	6.2		18	32	mA
		I _{COL} Outputs LOW			23	38		4.9	9.8		38	68	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		15 22		22 22		7.0 7.0	ns

7433, LS33 Buffers

Quad Two-Input NOR Buffer (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7433	11ns	23mA
74LS33	19ns	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7433N, N74LS33N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

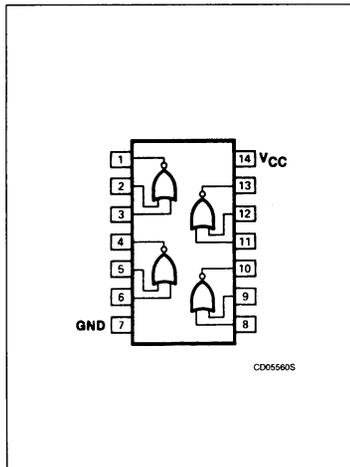
PINS	DESCRIPTION	74	74LS
A, B	Inputs	1uI	1LSuI
Y	Output	30uI	10LSuI

NOTE:

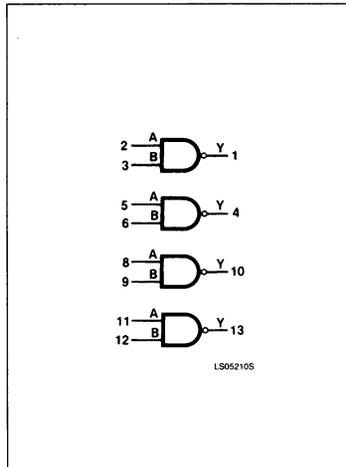
Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

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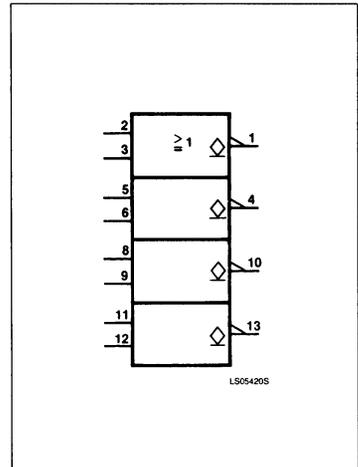
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffers

7433, LS33

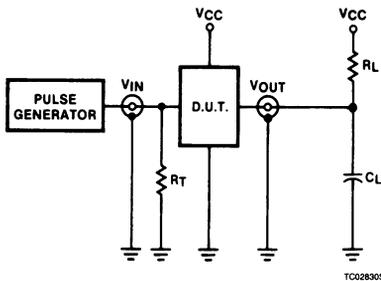
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	2.0			2.0			V
V_{IL}			+0.8			+0.8	V
I_{IK}			-12			-18	mA
V_{OH}			5.5			5.5	V
I_{OL}			48			24	mA
T_A	0		70	0		70	°C

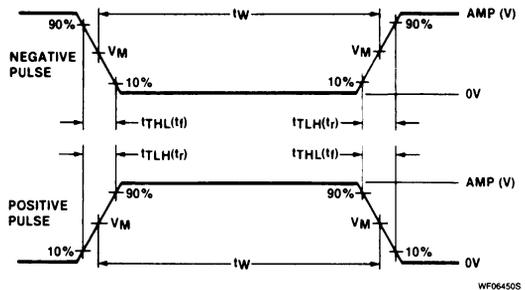
TEST CIRCUITS AND WAVEFORMS



**Test Circuit For 74
Open Collector Outputs**

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffers

7433, LS33

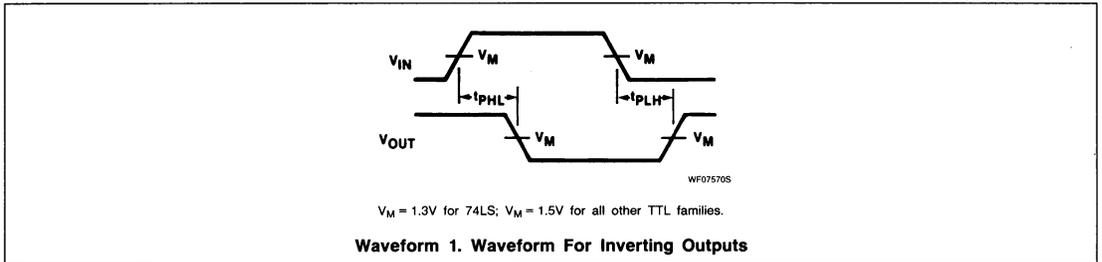
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7433			74LS33			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
I _{OH}	HIGH-level output current V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			250			250	μA
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 12mA (74LS)				0.25	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA
		V _I = 7.0V					0.1	mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40			μA
		V _I = 2.7V					20	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CCH} Outputs HIGH		12	21	1.8	3.6	mA
		I _{CCL} Outputs LOW		33	57	6.9	13.8	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		R _L = 133Ω		C _L = 45pF, R _L = 667Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay C _L = 50pF for 7433 Waveform 1		15 18		32 28	ns
t _{PLH} t _{PHL}	Propagation delay C _L = 150pF for 7433 Waveform 1		22 24			ns

7437, LS37, S37 Buffers

Quad Two-Input NAND Buffer
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7437	11ns	22mA
74LS37	12ns	3.5mA
74S37	4ns	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7437N, N74LS37N, N74S37N
Plastic SO	N74S37D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

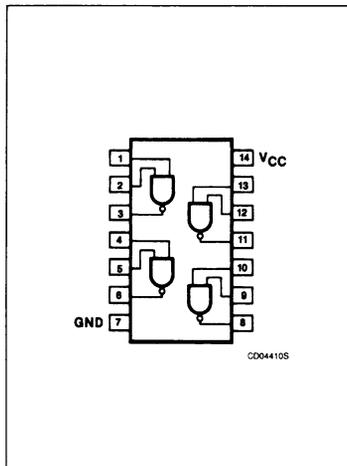
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1ul	2Sul	1LSul
Y	Output	30ul	30Sul	30LSul

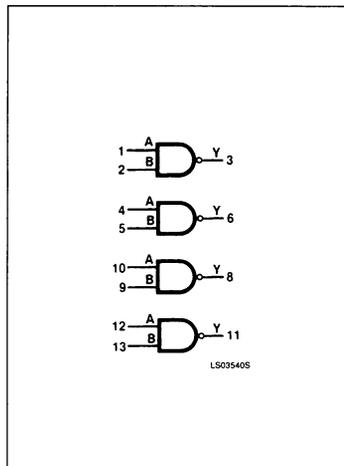
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

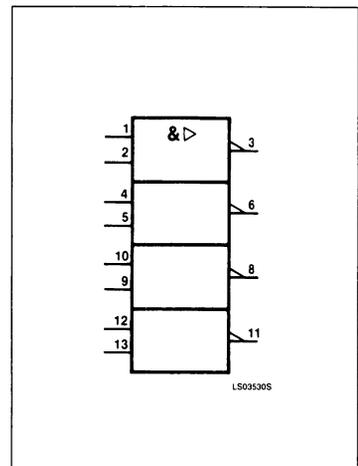
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffers

7437, LS37, S37

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

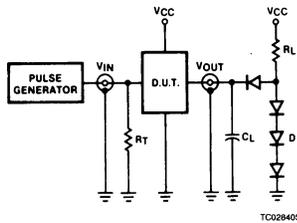
PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

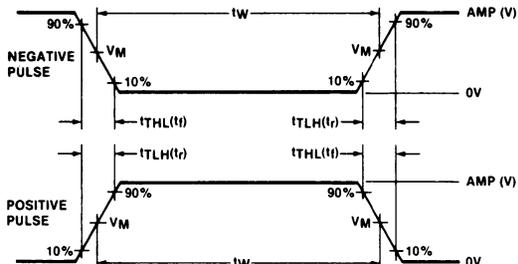
PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-1200			-1200			-3000	μA
I _{OL} LOW-level output current			48			24			60	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



TC028405



WF064505

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffers

7437, LS37, S37

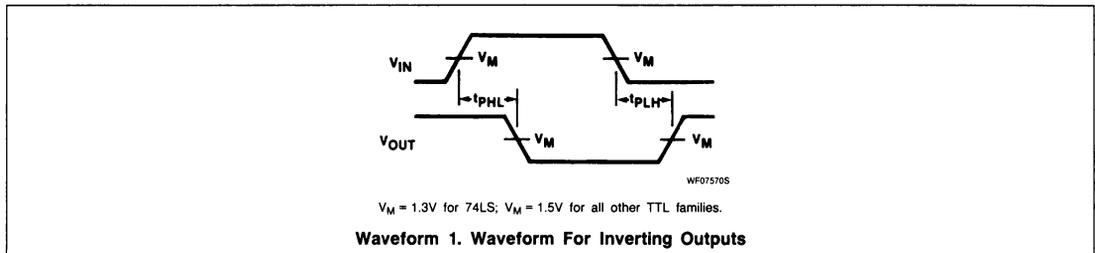
DC ELECTRICAL CHARACTERISTICS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7437			74LS37			74S37			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX			0.2	0.4	0.35	0.5		0.5	V	
		I _{OL} = 12mA (74LS)					0.25	0.4			V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			1.0			mA	
		V _I = 7.0V						0.1			mA	
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V						20			100 μA	
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V									-4.0 mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-70	-30		-100	-50		-225	mA	
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CC} H Outputs HIGH			9	15.5	0.9	2		20	36	mA
		I _{CC} L Outputs LOW			34	54	6	12		46	80	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second for the 7437 and 74LS37, and 100 milliseconds for the 74S37.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 45pF, R _L = 133Ω		C _L = 45pF, R _L = 667Ω		C _L = 50pF, R _L = 93Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		22 15		24 24		6.5 6.5	ns

7438, LS38, S38 Buffers

Quad Two-Input NAND Buffers (Open Collectors)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7438	13ns	28mA
74LS38	19ns	3.5mA
74S38	6.5ns	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7438N, N74LS38N, N74S38N
Plastic SO	N74S38D, N74LS38D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

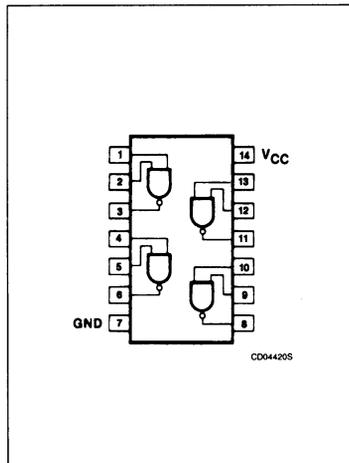
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1uI	2Sul	1LSul
Y	Output	30ul	30Sul	30LSul

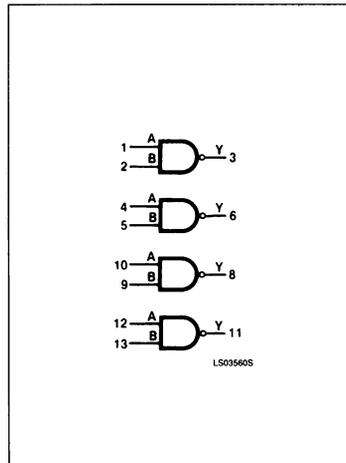
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

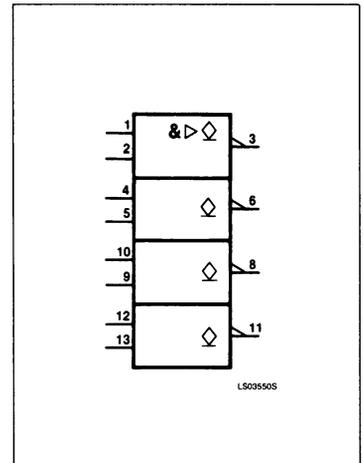
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffers

7438, LS38, S38

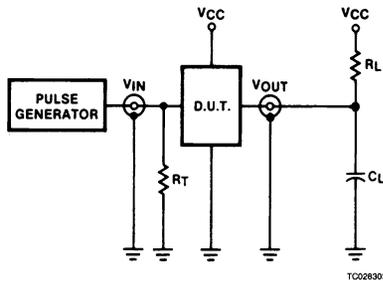
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
V _{OH} HIGH-level output current			5.5			5.5			5.5	V
I _{OL} LOW-level output current			48			24			60	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs

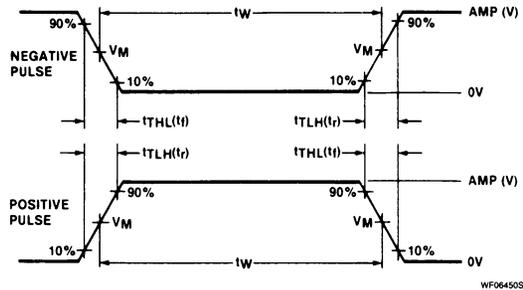
DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffers

7438, LS38, S38

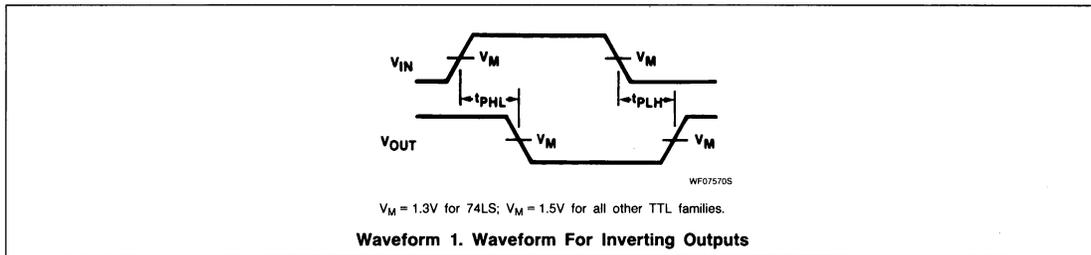
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7438			74LS38			74S38			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
I_{OH}	HIGH-level output voltage $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$			250			250			250	μA
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$			0.2	0.4	0.35	0.5		0.5	V
		$I_{OL} = 12\text{mA (74LS)}$					0.25	0.4			V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5			-1.5			-1.2	V
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$				1.0				1.0	mA
		$V_I = 7.0\text{V}$						0.1			mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$				40					μA
		$V_I = 2.7\text{V}$						20		100	μA
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$				-1.6		-0.4			mA
		$V_I = 0.5\text{V}$								-4.0	mA
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH			5	8.5	0.9	2	20	36	mA
		I_{CCL} Outputs LOW			34	54	6	12	46	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 45\text{pF}, R_L = 133\Omega$		$C_L = 45\text{pF}, R_L = 667\Omega$		$C_L = 50\text{pF}, R_L = 93\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1		22 18		32 28		10 10	ns

7439 Buffer

Quad Two-Input NAND Buffer (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7439	11ns	4.5mA (I_{CCH}) 30mA (I_{CCL})

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7439N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

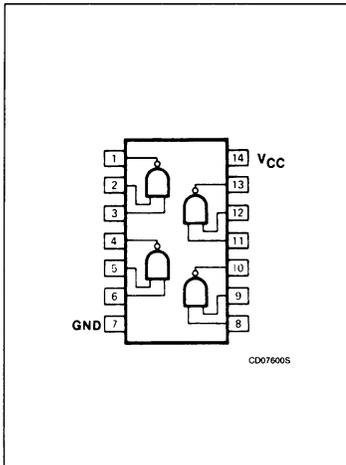
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
A, B	Inputs	1ul
Y	Output	30ul

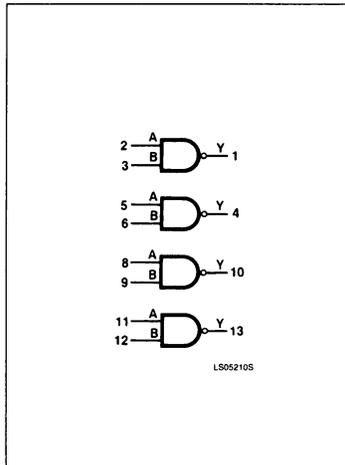
NOTE:

A 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

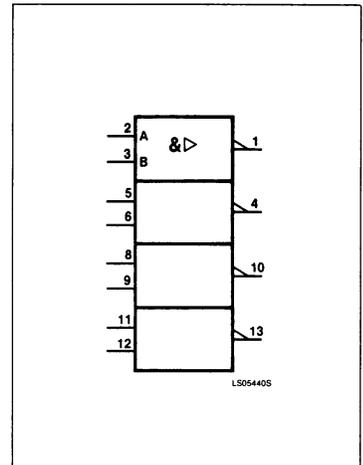
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffer

7439

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

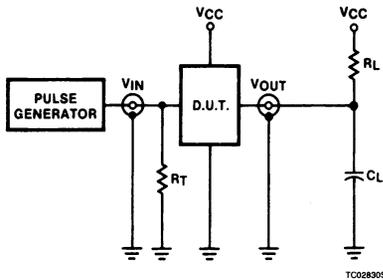
PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
V _{OH} HIGH-level output current			5.5	V
I _{OL} LOW-level output current			48	mA
T _A Operating free-air temperature	0		70	°C

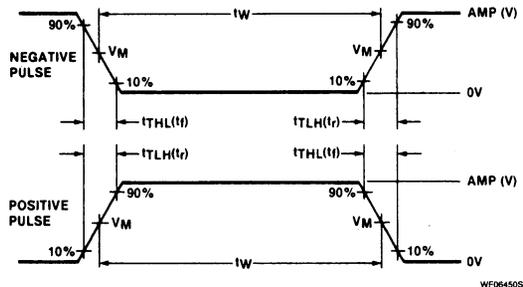
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TEST CIRCUITS AND WAVEFORMS



TC028305

Test Circuit For 74
Open Collector Outputs



WF064505

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffer

7439

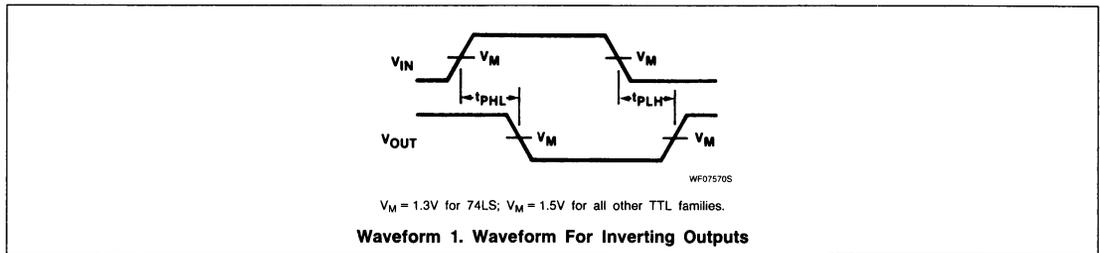
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7439			UNIT
		Min	Typ ²	Max	
I _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			250	μA
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Output HIGH	4.5	8.5	mA
		I _{CC} L Outputs LOW	30	54	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 45pF, R _L = 133Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 18	ns

7440, LS40, S40 Buffers

Dual Four-Input NAND Buffer
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7440	11ns	11mA
74LS40	12ns	1.8mA
74S40	6ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7440N, N74LS40N, N74S40N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

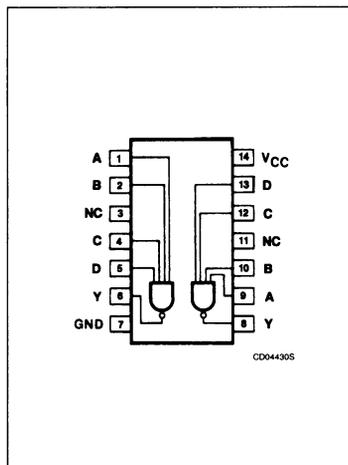
PINS	DESCRIPTION	74	74S	74LS
A - D	Inputs	1ul	2Sul	1LSul
Y	Output	30ul	30Sul	30LSul

NOTE:

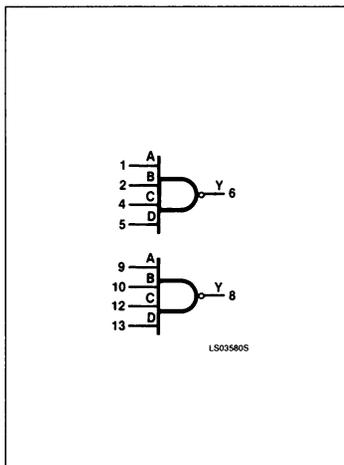
Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

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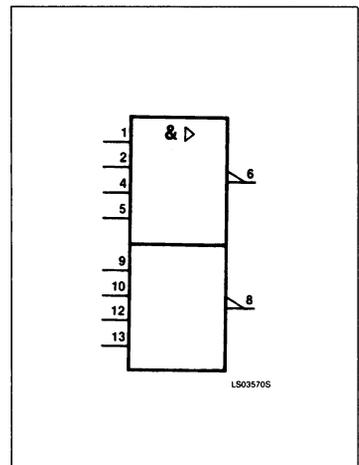
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffers

7440, LS40, S40

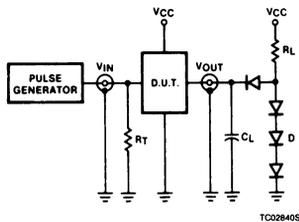
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

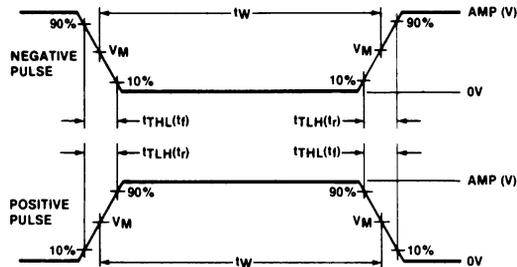
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-1200			-1200			-3000	μA
I _{OL} LOW-level output current			48			24			60	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



TC02840S



WF06450S

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffers

7440, LS40, S40

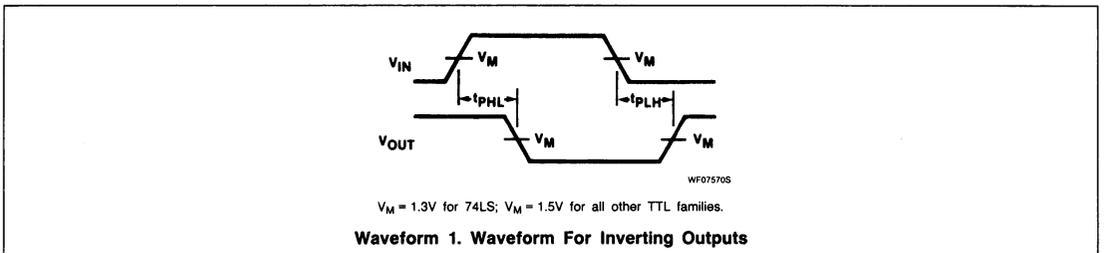
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7440			74LS40			74S40			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V
		I _O = 12mA (74LS)					0.25	0.4			
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			-1.2 V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA
		V _I = 7.0V						0.1			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA
		V _I = 2.7V						20		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA
		V _I = 0.5V								-4.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-70	-15		-100	-50		-225	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH			4	8		0.45	1		10 18 mA
		I _{CC} L Outputs LOW			17	27		3	6		25 44 mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. The 74S40 test time for I_{OS} should not exceed 100ms.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 133Ω		C _L = 45pF, R _L = 667Ω		C _L = 50pF, R _L = 93Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15		24 24		6.5 6.5	ns

7442, LS42 Decoders

BCD-To-Decimal Decoder (1-of-10)
Product Specification

Logic Products

FEATURES

- Mutually exclusive outputs
- 1-of-8 demultiplexing ability
- Outputs disabled for input codes above nine

DESCRIPTION

The '42 decoder accepts four active HIGH BCD inputs and provides 10 mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the '42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input, A_3 , produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7442	15ns	28mA
74LS42	18ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7442N, N74LS42N
Plastic SO	N74LS54D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

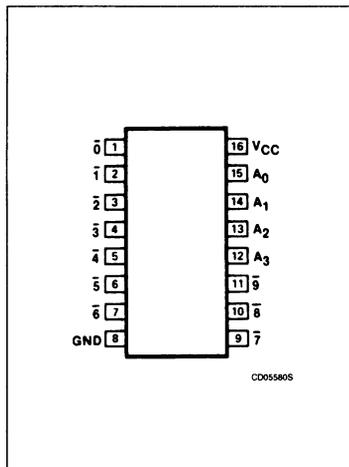
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
$A_0 - A_3$	Inputs	1ul	1LSul
$\bar{0} - \bar{9}$	Outputs	10ul	10LSul

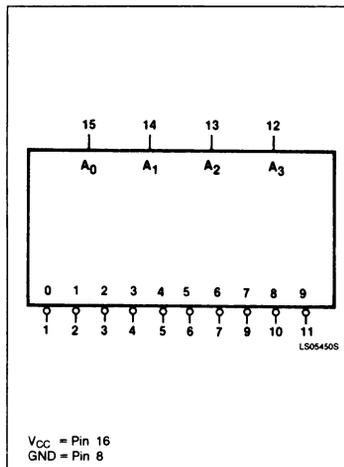
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$ and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

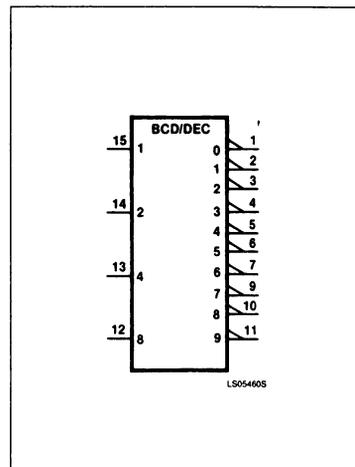
PIN CONFIGURATION



LOGIC SYMBOL



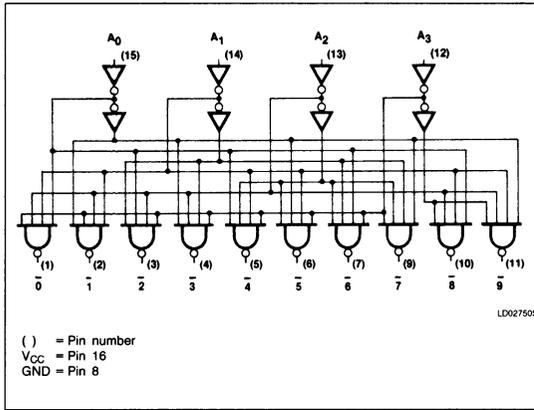
LOGIC SYMBOL (IEEE/IEC)



Decoders

7442, LS42

LOGIC DIAGRAM



FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	L	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	H	H	H	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

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Decoders

7442, LS42

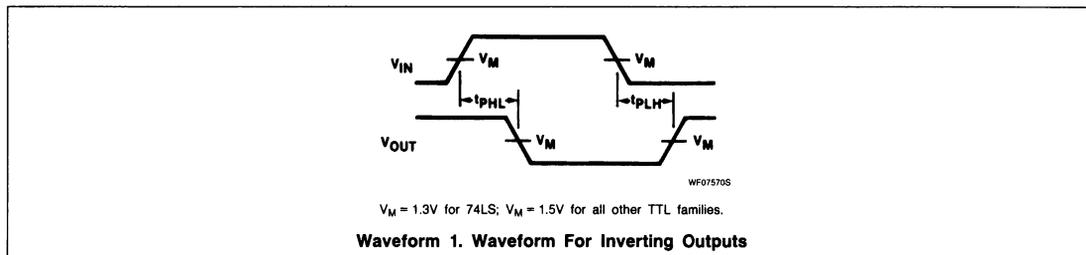
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7442			74LS42			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX				0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						mA
		V _I = 7.0V					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V						μA
		V _I = 2.7V					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		28	56		7	13	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open and all inputs grounded.

AC WAVEFORM



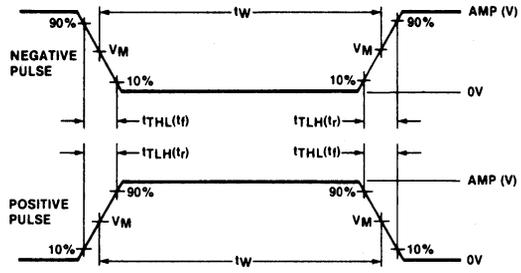
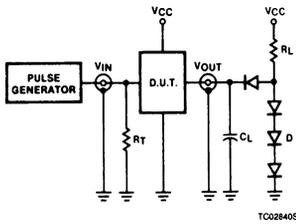
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 409Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} Propagation delay	Waveform 1 3 logic levels		30		30	ns
t _{PHL} Address to output		30		30		
t _{PLH} Propagation delay	Waveform 1 2 logic levels		25		25	ns
t _{PHL} Address to output		25		25		

Decoders

7442, LS42

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7445 Decoder/Driver

BCD-To-Decimal Decoder/Driver (Open Collector)
Product Specification

Logic Products

FEATURES

- 80mA output sink capability
- 30V output breakdown voltage
- Ideally suited as lamp or solenoid driver
- See '42 for standard TTL output version
- See '145 for "LS" version

DESCRIPTION

The '45 decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are off. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable.

The '45 can sink 20mA while maintaining the standardized guaranteed output LOW voltage (V_{OL}) of 0.4V, but it can sink up to 80mA with a guaranteed V_{OL} of less than 0.9V.

The '45 features an output breakdown voltage of 30V and is ideally suited as a lamp or solenoid driver.

TYPE	MAX I_{OL}	TYPICAL SUPPLY CURRENT (TOTAL)
7445	80mA	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7445N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

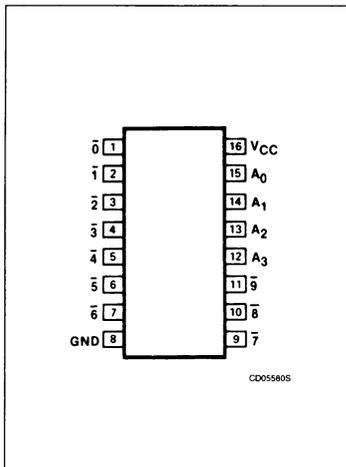
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
$A_0 - A_3$ $\bar{0} - \bar{9}$	Inputs Outputs	1uI 12.5uI

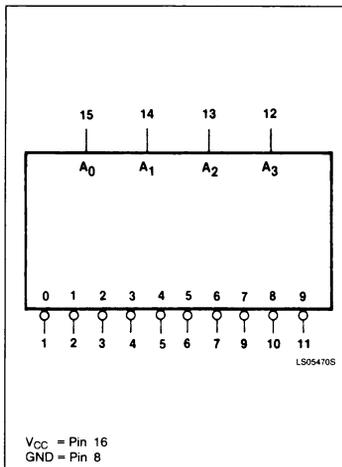
NOTE:

A 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

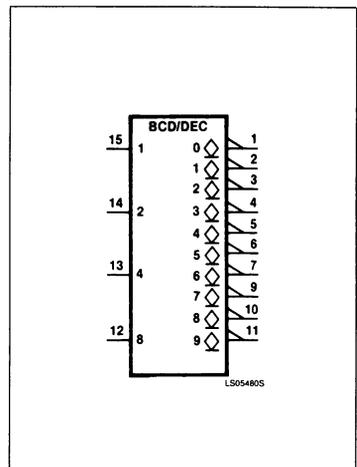
PIN CONFIGURATION



LOGIC SYMBOL



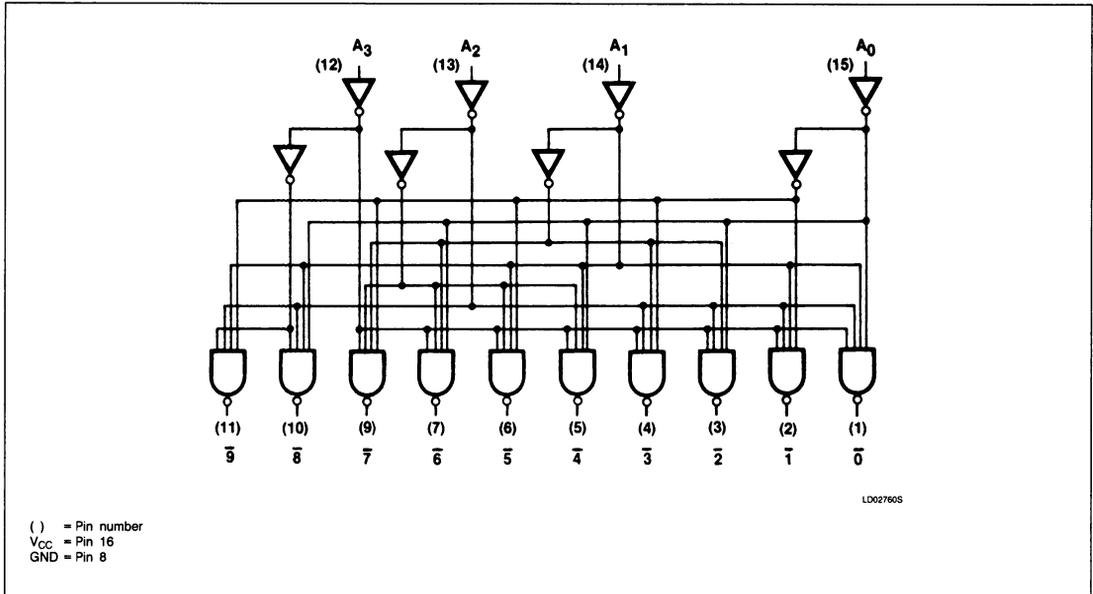
LOGIC SYMBOL (IEEE/IEC)



Decoder/Driver

7445

LOGIC DIAGRAM



FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	0̄	1̄	2̄	3̄	4̄	5̄	6̄	7̄	8̄	9̄
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	L	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L	H
H	L	L	L	H	H	H	H	H	H	H	H	H	L
H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
 L = LOW voltage levels

Decoder/Driver

7445

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to +30	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-12	mA
V_{OH}	HIGH-level output voltage			30	V
I_{OL}	LOW-level output current			80	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7445			UNIT		
		Min	Typ ²	Max			
I_{OH}	HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 30\text{V}$			250	μA	
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = 20\text{mA}$		0.4	V	
			$I_{OL} = 80\text{mA}$	0.5	0.9	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA	
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA	
I_{CC}	Supply current ³ (total)	$V_{CC} = \text{MAX}$			43	70	mA

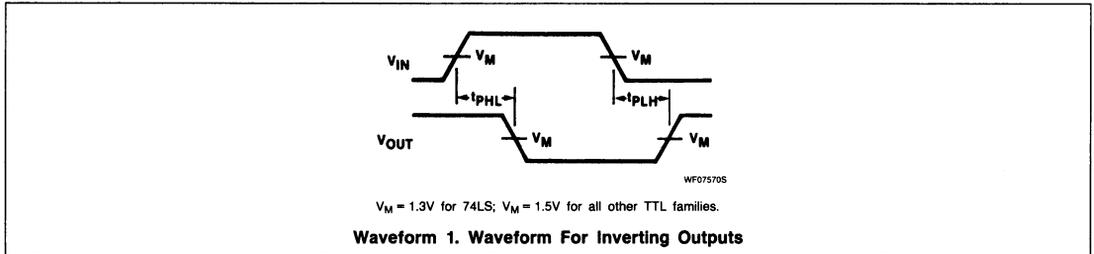
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- Measure I_{CC} with all inputs grounded and outputs open.

Decoder/Driver

7445

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	74		UNIT
		$C_L = 15pF, R_L = 100\Omega$		
		Min	Max	
t_{PLH}	Propagation delay	Waveform 1		ns
t_{PHL}	Address to output			
			50	
			50	

TEST CIRCUITS AND WAVEFORMS

TC028305

**Test Circuit For 74
Open Collector Outputs**

DEFINITIONS
 R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

WF064505

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

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7451, LS51, S51 Gates

'51, 'S51 Dual 2-Wide 2-Input AND-OR-Invert Gate
'LS51 Dual 2-Wide 3-Input, 2-Wide 2-Input AND-OR-Invert Gate

Product Specification

Logic Products

FUNCTION TABLE '51, 'S51, 1/2 'LS51

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

'LS51

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7451	11ns	5.7mA
74LS51	12ns	1.1mA
74S51	3.5ns	11mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7451N, N74LS51N, N74S51N
Plastic SO	N74LS51D, N74S51D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

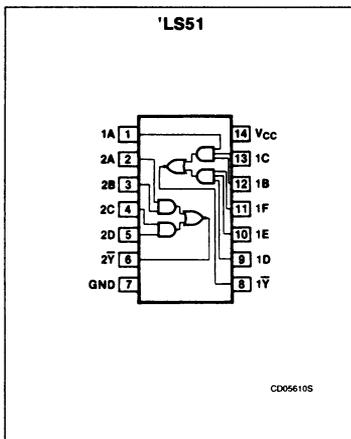
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

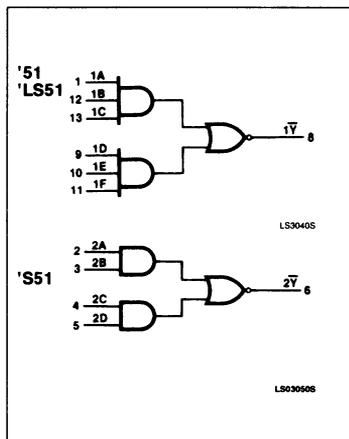
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

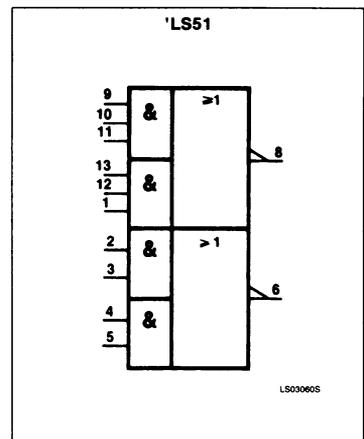
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7451, LS51, S51

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

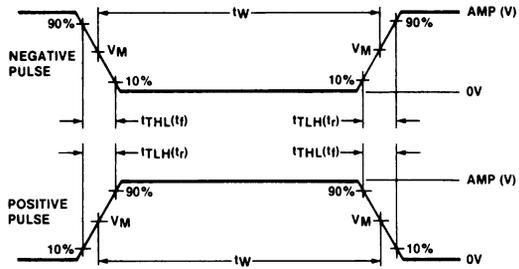
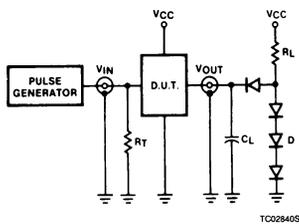
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-400			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

NOTE:

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gates

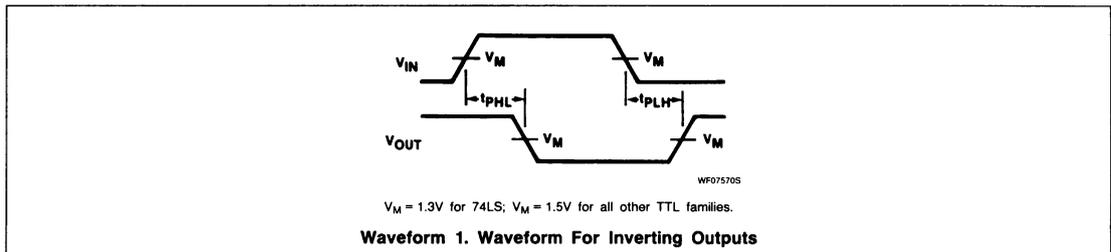
7451, LS51, S51

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7451			74LS51			74S51			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V_{OH}	HIGH-level output voltage $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4	3.4		2.7	3.4		2.7	3.4		V	
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$		0.2	0.4		0.35	0.5		0.5	V	
		$I_{OL} = 4\text{mA (74LS)}$					0.25	0.4				V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5				-1.5		-1.2	V	
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$			1.0					1.0	mA	
		$V_I = 7.0\text{V}$					0.1				mA	
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$			40						μA	
		$V_I = 2.7\text{V}$					20		50		μA	
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$			-1.6		-0.4				mA	
		$V_I = 0.5\text{V}$							-2.0		mA	
I_{OS}	Short-circuit output current ³ $V_{CC} = \text{MAX}$	-18		-55	-20		-100	-40		-100	mA	
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		4	8		0.8	1.6		8.2	17.8	mA
		I_{CCL} Outputs LOW		7.4	14		1.4	2.8		13.6	22	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM**AC ELECTRICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}, R_L = 400\Omega$		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}, R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1		22 15		20 20		5.5 5.5	ns

74LS54 Gate

Four-Wide Two- & Three-Input AND-OR-Invert Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS54	12ns	0.9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS54N
Plastic SO	N74LS54D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
A - K	Inputs	1LSul
Y	Output	10LSul

NOTE:

Where a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

FUNCTION TABLE

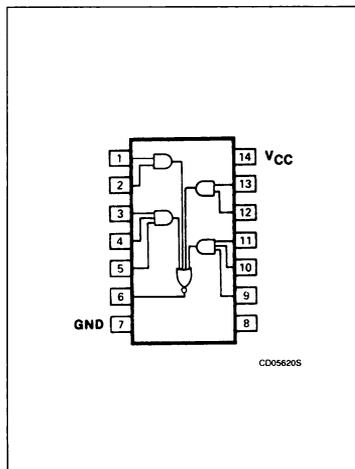
INPUTS										OUTPUT
A	B	C	D	E	F	G	H	J	K	Y
H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	X	X	X	X	X	L
X	X	X	X	X	H	H	X	X	X	L
X	X	X	X	X	X	X	H	H	H	L
All other combinations										H

H = HIGH voltage level

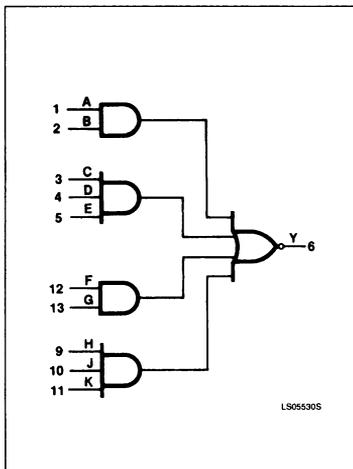
L = LOW voltage level

X = Don't care

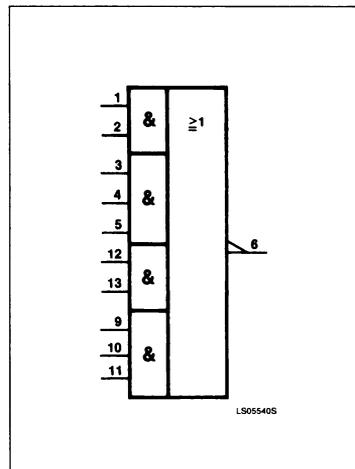
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74LS54

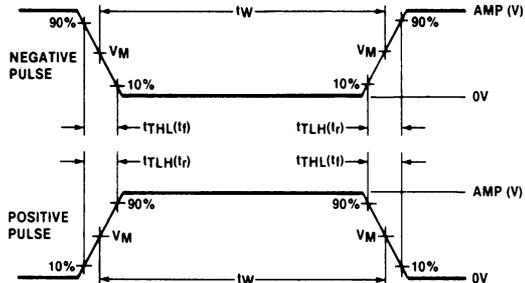
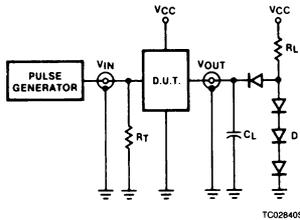
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
I _{OH} HIGH-level output current			-400	μA
I _{OL} LOW-level output current			8	mA
T _A Operating free-air temperature	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

74LS54

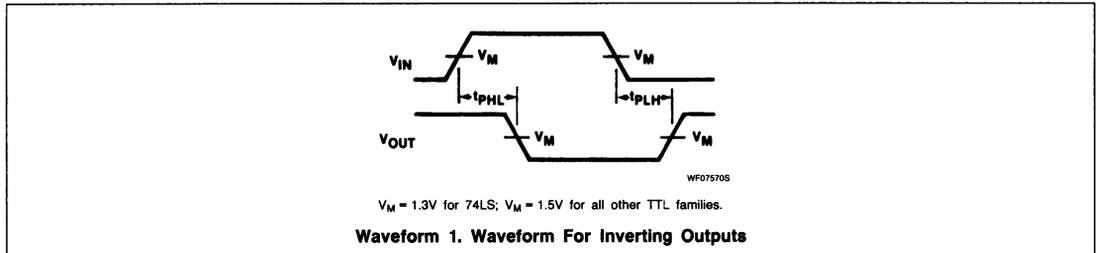
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS54			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX		0.35	0.5	V
		I _{OL} = 4mA (74LS)		0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH	0.8	1.6	mA	
		I _{CC} L Outputs LOW	1.0	2.0	mA	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL}	Waveform 1		20 20	ns

74S64 Gate

Four-Two-Three-Two-Input AND-OR-Invert Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S64	3.5ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S64N
Plastic SO	N74S64D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
A - L	Inputs	1Sul
Y	Output	10Sul

NOTE:

A 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

FUNCTION TABLE

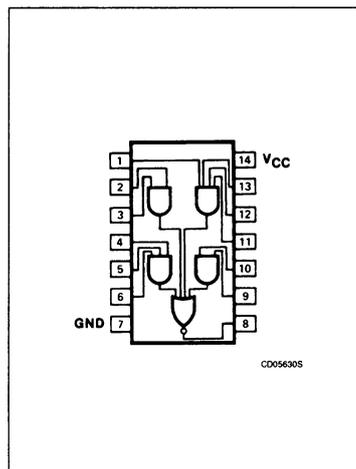
INPUTS											OUTPUT
A	B	C	D	E	F	G	H	J	K	L	Y
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = HIGH voltage level

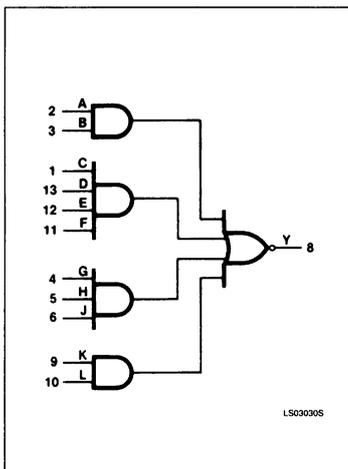
L = LOW voltage level

X = Don't care

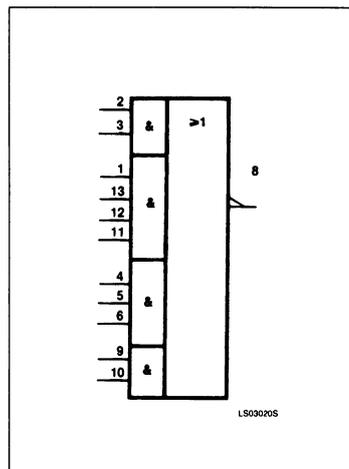
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74S64

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

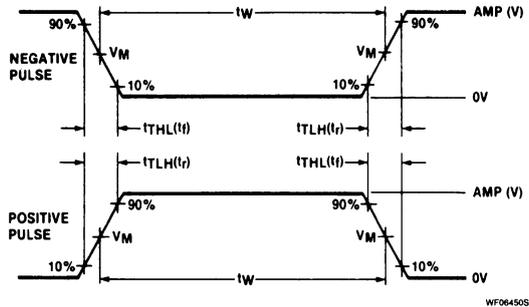
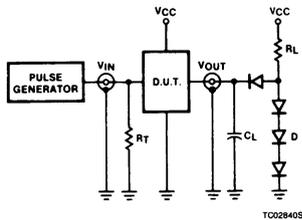
PARAMETER	74S	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74S			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
I _{OH} HIGH-level output current			-1000	μA
I _{OL} LOW-level output current			20	mA
T _A Operating free-air temperature	0		70	°C

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TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

74S64

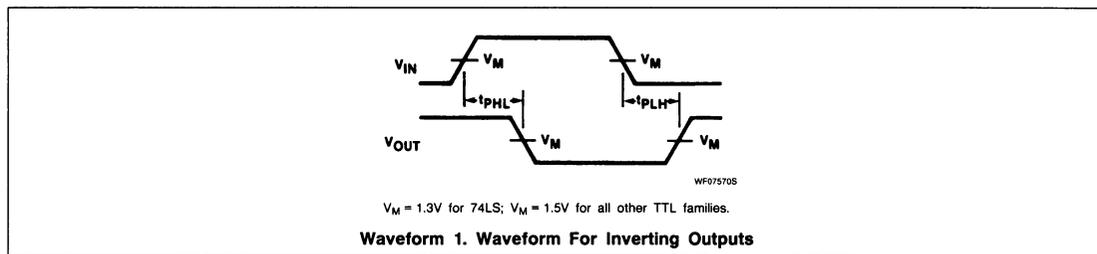
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S64			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX			0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _K			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-40		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH	7	12.5	mA
		I _{CC} L Outputs LOW	8.5	16	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		5.5 5.5	ns

7473, LS73 Flip-Flops

Dual J-K Flip-Flop Product Specification

Logic Products

DESCRIPTION

The '73 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 7473 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW transition. For the 7473, the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the \bar{Q} output HIGH.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7473	20MHz	10mA
74LS73	45MHz	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7473N, N74LS73N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

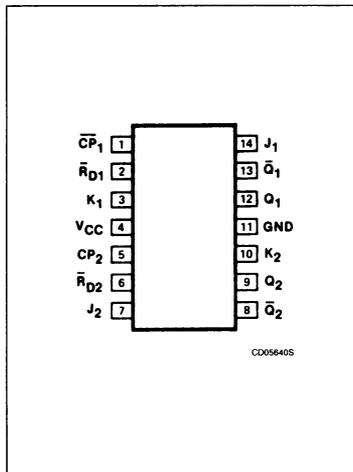
PINS	DESCRIPTION	74	74LS
$\bar{C}P$	Clock input	2ul	4LSul
\bar{R}_D	Reset input	2ul	3LSul
J, K	Data inputs	1ul	1LSul
Q, \bar{Q}	Outputs	10ul	10LSul

NOTE:

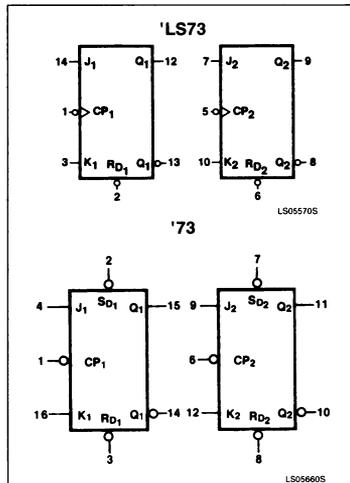
Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

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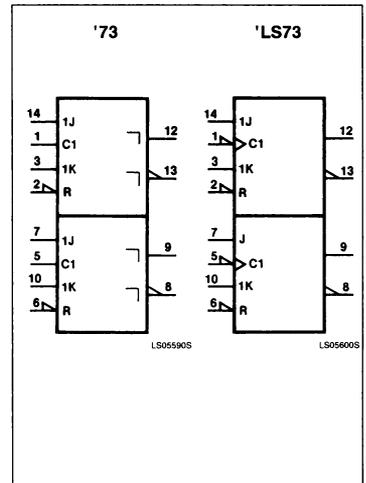
PIN CONFIGURATION



LOGIC SYMBOL



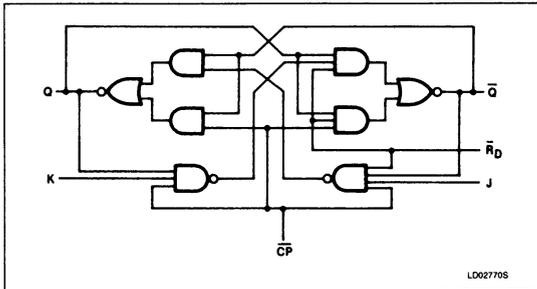
LOGIC SYMBOL (IEE/IEC)



Flip-Flops

7473, LS73

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{R}_D	$\overline{CP}^{(2)}$	J	K	Q	\bar{Q}
Asynchronous reset (Clear)	L	X	X	X	L	H
Toggle	H	\downarrow	h	h	\bar{q}	q
Load "0" (Reset)	H	\downarrow	l	h	L	H
Load "1" (Set)	H	\downarrow	h	l	H	L
Hold "no change"	H	\downarrow	l	l	q	\bar{q}

H = HIGH voltage level steady state.

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.⁽¹⁾

L = LOW voltage level steady state.

l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.⁽¹⁾

q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

X = Don't care

\downarrow = Positive Clock pulse.

NOTES:

1. The J and K inputs of the 7473 must be stable while the Clock is HIGH for conventional operation.

2. The 74LS73 is edge triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	HIGH-level output current			-400			-400	μA
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

Flip-Flops

7473, LS73

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7473			74LS73			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	All inputs		1.0			mA
		V _I = 7.0V	J, K inputs				0.1	mA
			\bar{R}_D inputs				0.3	mA
			$\bar{C}P$ inputs				0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, K inputs		40			μ A
			\bar{R}_D inputs		80			μ A
			$\bar{C}P$ inputs		80			μ A
		V _I = 2.7V	J, K inputs				20	μ A
			\bar{R}_D inputs				60	μ A
			$\bar{C}P$ inputs				80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	J, K inputs		-1.6		-0.4	mA	
		\bar{R}_D inputs		-3.2		-0.8	mA	
		$\bar{C}P$ inputs		-3.2		-0.8	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		10	40		4	8	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 3	15		30		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1, 'LS73 Waveform 3, '73		25 40		20 30	ns
t _{PLH} Propagation delay t _{PHL} \bar{R}_D to output	Waveform 2		25 40		20 30	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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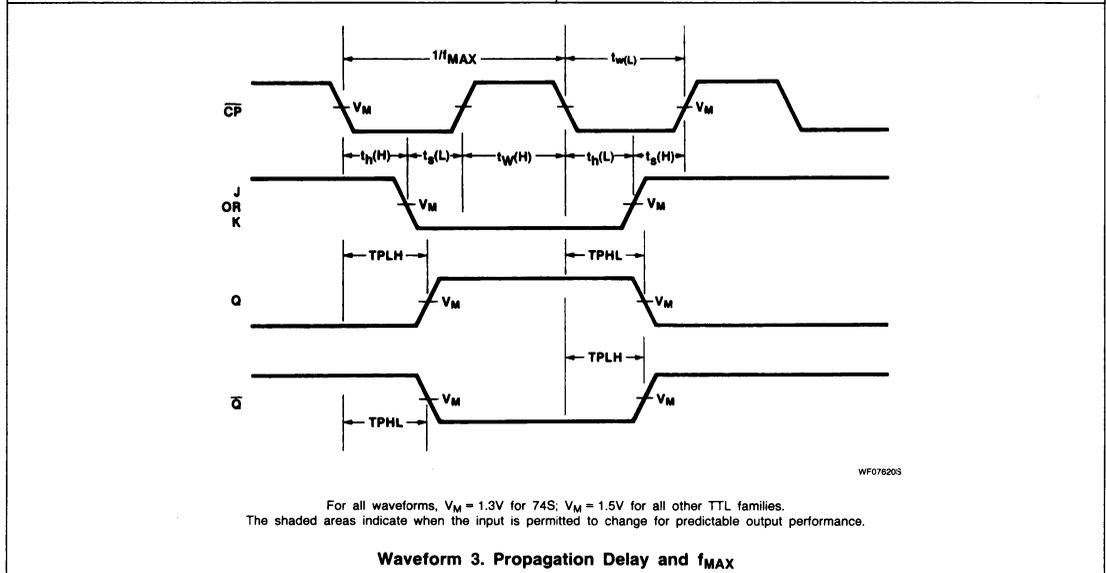
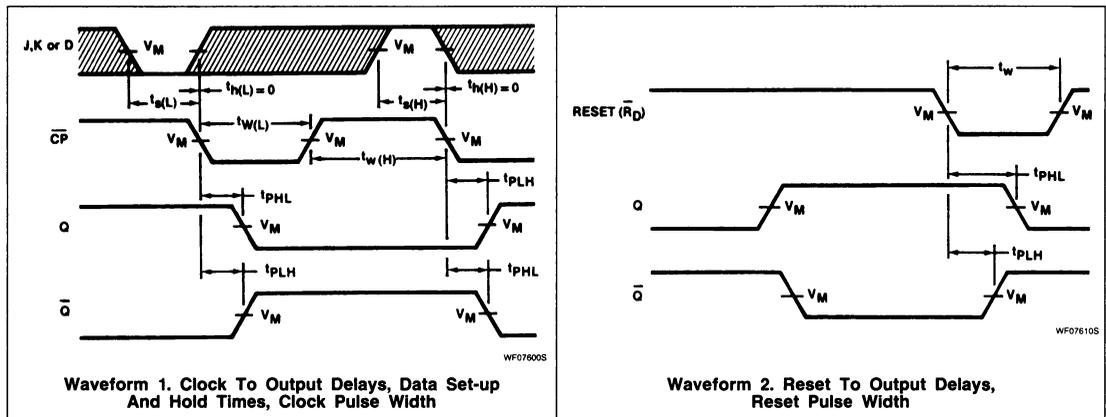
Flip-Flops

7473, LS73

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	20		20		ns
$t_{w(L)}$	Clock pulse width (LOW)	47				ns
$t_{w(L)}$	Reset pulse width (LOW)	25		25		ns
t_s	Set-up time J or K to Clock ^(a)	0		20		ns
t_h	Hold time J or K to Clock	0		0		ns

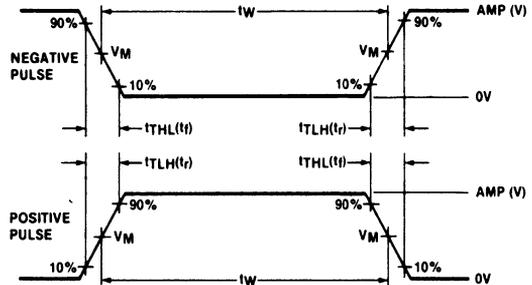
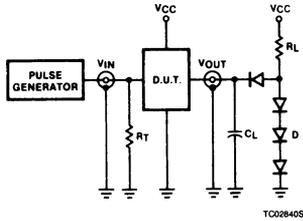
AC WAVEFORMS



Flip-Flops

7473, LS73

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7474, LS74A, S74 Flip-Flops

Dual D-Type Flip-Flop Product Specification

Logic Products

DESCRIPTION

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and \bar{Q} outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7474	25MHz	17mA
74LS74A	33MHz	4mA
74S74	100MHz	30mA

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7474N, N74LS74AN, N74S74N
Plastic SO	N741S74A, N74S74D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

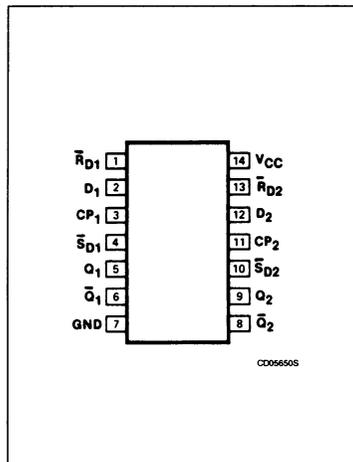
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
D	Input	1ul	1Sul	1LSul
\bar{R}_D	Input	2ul	3Sul	2LSul
\bar{S}_D	Input	1ul	2Sul	2LSul
CP	Input	2ul	2Sul	1LSul
Q, \bar{Q}	Outputs	10ul	10Sul	10LSul

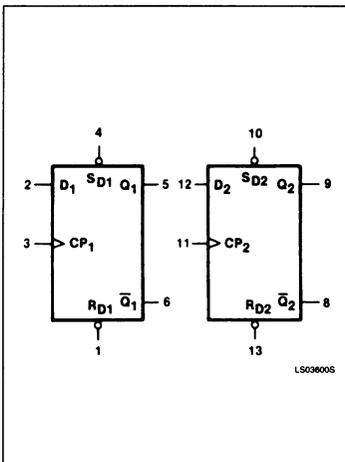
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

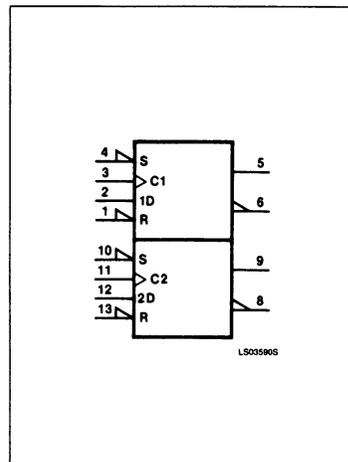
PIN CONFIGURATION



LOGIC SYMBOL



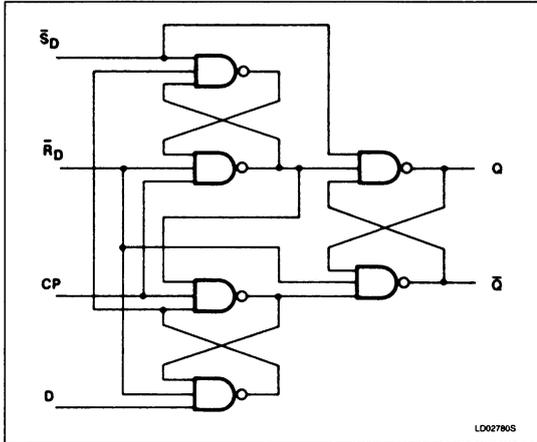
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

7474, LS74A, S74

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	D	Q	\bar{Q}
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined ⁽¹⁾	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	i	L	H

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

NOTE:
 (1) Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I_{IK} Input clamp current			-12			-18			-18	mA
I_{OH} HIGH-level output current			-400			-400			-1000	μA
I_{OL} LOW-level output current			16			8			20	mA
T_A Operating free-air temperature	0		70	0		70	0		70	°C

Flip-Flops

7474, LS74A, S74

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7474			74LS74A			74S74			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			-1.2 V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V	D input					0.1				mA
			\bar{R}_D input					0.2				mA
			\bar{S}_D input					0.2				mA
CP input						0.1				mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	D input			40						μA
			\bar{R}_D input			120						μA
			\bar{S}_D input			80						μA
			CP input			80						μA
		V _I = 2.7V	D input					20			50	μA
			\bar{R}_D input					40			150	μA
\bar{S}_D input						40			100	μA		
CP input						20			100	μA		
I _{IL} LOW-level input current ⁵	V _{CC} = MAX	V _I = 0.4V	D input			-1.6		-0.4				mA
			\bar{R}_D input			-3.2		-0.8				mA
			\bar{S}_D input			-1.6		-0.8				mA
			CP input			-3.2		-0.4				mA
		V _I = 0.5V	D input								-2	mA
			\bar{R}_D input								-6	mA
			\bar{S}_D input								-4	mA
			CP input								-4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		17	30		4	8		30	50	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and \bar{Q} outputs HIGH in turn.
- Set is tested with reset HIGH and reset is tested with set HIGH.

Flip-Flops

7474, LS74A, S74

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	15		25		75		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		25 40		25 40		9 9	ns
t_{PLH} Propagation delay t_{PHL} Set or Reset to output	Waveform 2 Waveform 2 CP = HIGH		25 40		25 40		6 13.5	ns
t_{PHL} Set or Reset to output	Waveform 2 CP = LOW		40		40		8	ns

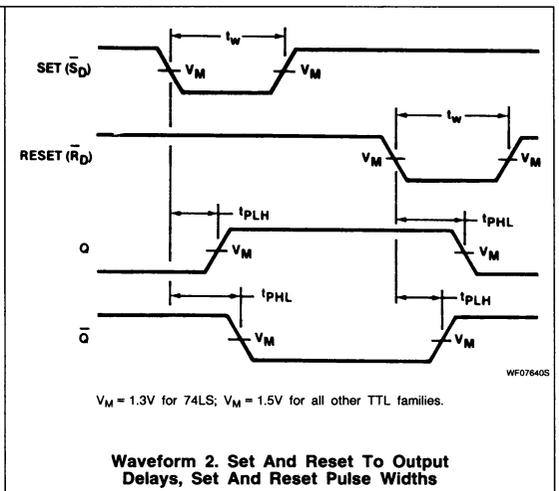
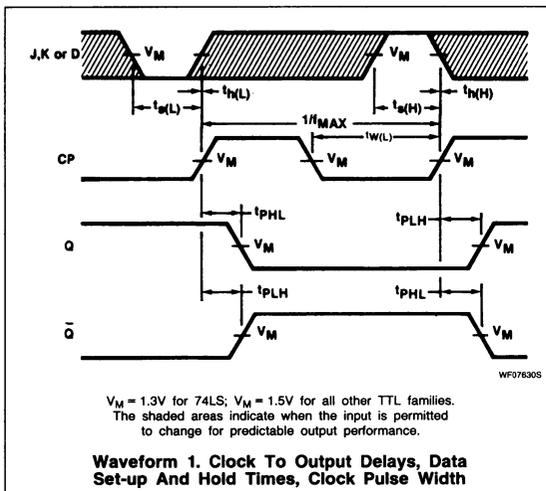
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{\text{W(H)}}$ Clock pulse width (HIGH)	Waveform 1	30		25		6		ns
$t_{\text{W(L)}}$ Clock pulse width (LOW)	Waveform 1	37				7.3		ns
$t_{\text{W(L)}}$ Set or reset pulse width (LOW)	Waveform 2	30		25		7		ns
$t_{\text{s(H)}}$ Set-up time (HIGH) data to clock	Waveform 1	20		20		3		ns
$t_{\text{s(L)}}$ Set-up time (LOW) data to clock	Waveform 1	20		20		3		ns
t_{h} Hold time data to clock	Waveform 1	5		5		2		ns

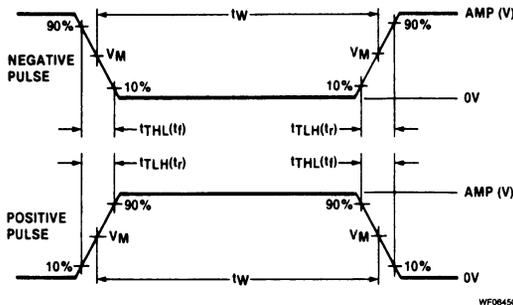
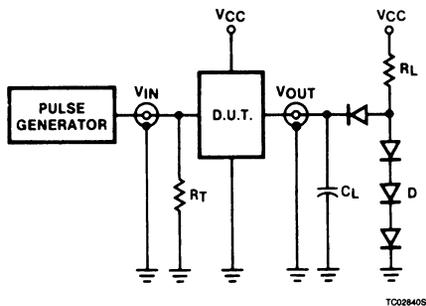
AC WAVEFORMS



Flip-Flops

7474, LS74A, S74

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7475, LS75 Latches

Quad Bistable Latch
Product Specification

Logic Products

FEATURES

- 4-bit bistable latch
- Refer to 74LS375 for V_{CC} and GND on corner pins

DESCRIPTION

The '75 has four bistable latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one set-up time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7475	18ns (t_{PLH}) 9ns (t_{PHL})	32mA
74LS75	15ns (t_{PLH}) 9ns (t_{PHL})	6.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7475N, N74LS75N
Plastic SO	N74LS25D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

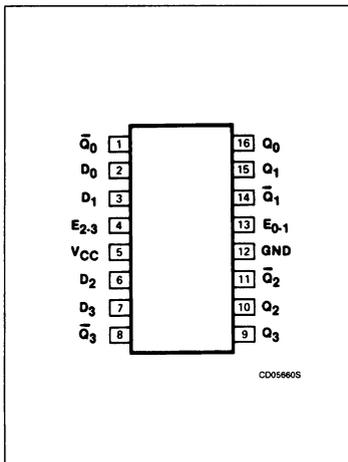
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
D	Input	2ul	1LSUI
E	Input	4ul	4LSUI
All	Outputs	10ul	10LSul

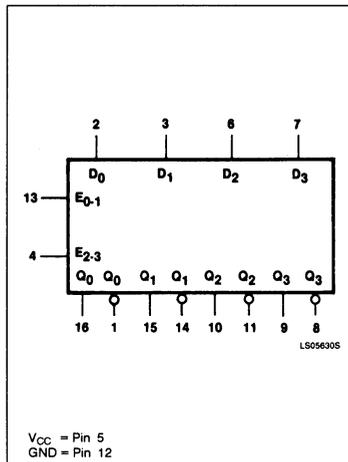
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA$.

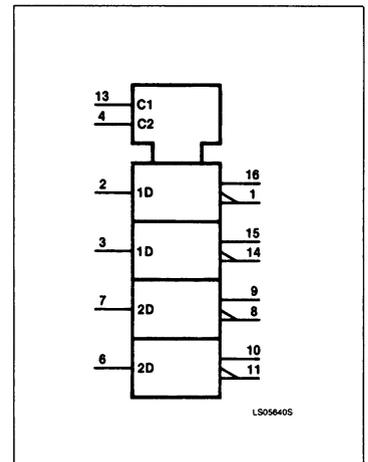
PIN CONFIGURATION



LOGIC SYMBOL



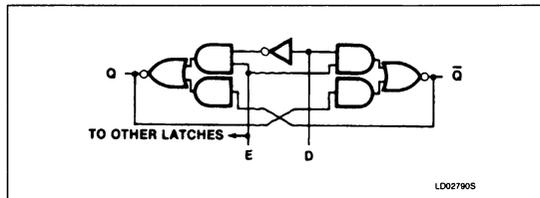
LOGIC SYMBOL (IEEE/IEC)



Latches

7475, LS75

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUT	
	E	D	Q	\bar{Q}
Data enabled	H	L	L	H
	H	H	H	L
Data latched	L	X	q	\bar{q}

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 q = Lower case letters indicate the state of referenced output one set-up time prior to the HIGH-to-LOW Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-400			-400	μ
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

Latches

7475, LS75

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7475			74LS75			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IL} = MAX, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V	
		I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	D inputs				0.1	mA	
			E inputs				0.4	mA	
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V	D inputs		80			μA	
			E inputs		160			μA	
		V _I = 2.7V	D inputs				20	μA	
			E inputs				80	μA	
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V	D inputs		-3.2		-0.4	μA	
			E inputs		-6.4		-1.6	μA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX		-18		-57	-20		-100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		32	53		6.3	12	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to Q output Waveform 1		30 25		27 17	ns
t _{PLH} t _{PHL}	Propagation delay Data to Q̄ output Waveform 2		40 15		20 15	ns
t _{PLH} t _{PHL}	Propagation delay Enable to Q output Waveform 3		30 15		27 25	ns
t _{PLH} t _{PHL}	Propagation delay Enable to Q̄ output Waveform 3		30 15		30 15	ns

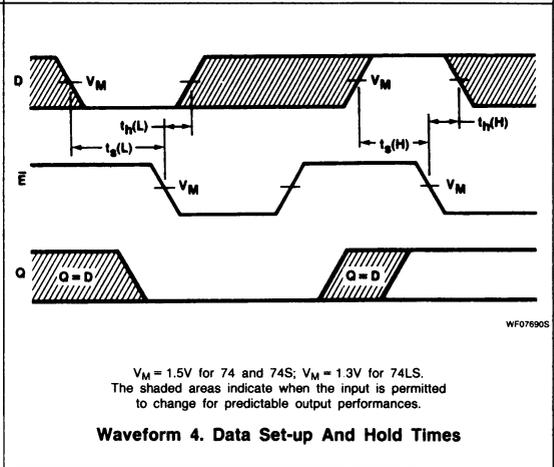
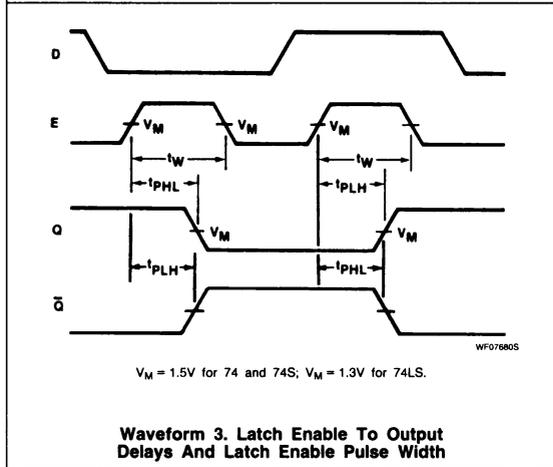
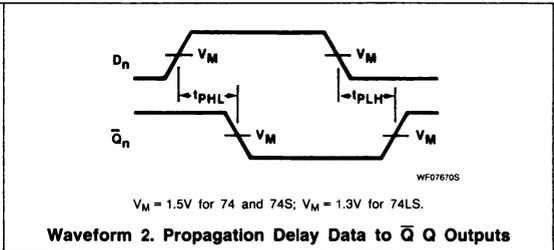
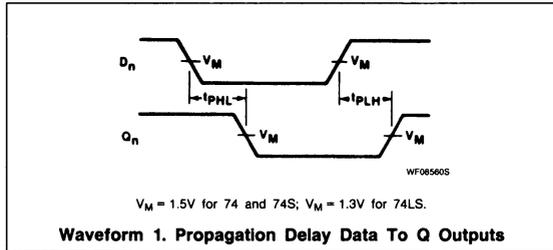
Latches

7475, LS75

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W Enable pulse width	Waveform 3	20		20		ns
t_s Set-up time, Data to Enable	Waveform 4	20		20		ns
t_h Hold time, Data to Enable	Waveform 4	5.0		5.0		ns

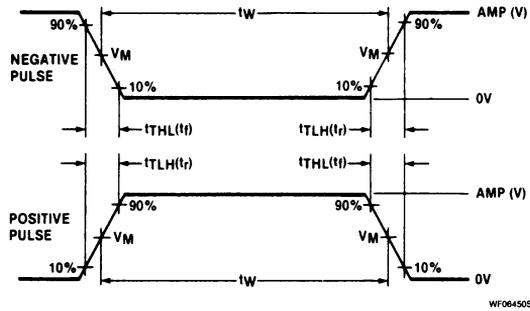
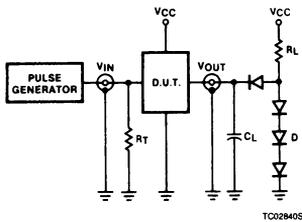
AC WAVEFORMS



Latches

7475, LS75

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7476, LS76 Flip-Flops

Dual J-K Flip-Flop Product Specification

Logic Products

DESCRIPTION

The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one set-up time prior to the HIGH-to-LOW Clock transition.

The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7476	20MHz	10mA
74LS76	45MHz	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7476N, N74LS76N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

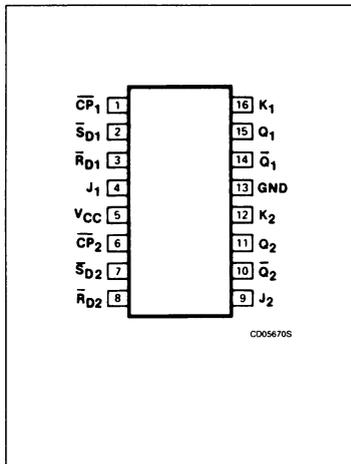
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
$\bar{C}P$	Clock input	2ul	2LSul
\bar{R}_D, \bar{S}_D	Reset and Set inputs	2ul	2LSul
J, K	Data inputs	1ul	1LSul
Q, \bar{Q}	Outputs	10ul	10LSul

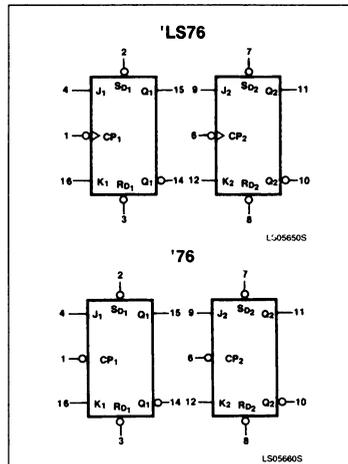
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

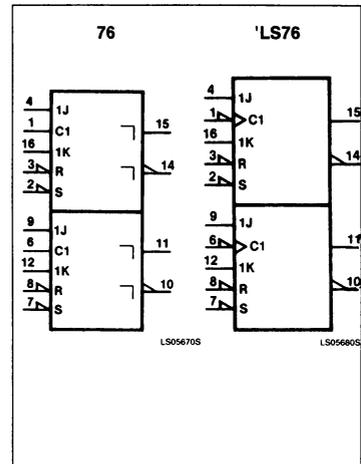
PIN CONFIGURATION



LOGIC SYMBOL



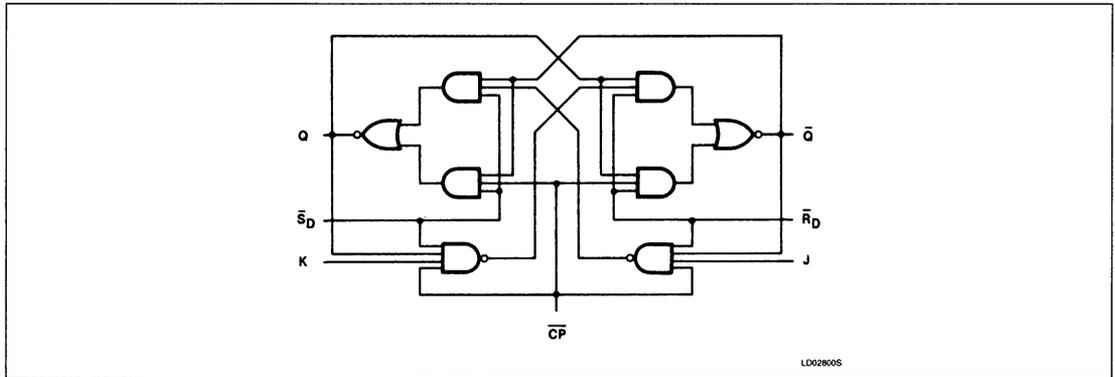
LOGIC SYMBOL (IEE/IEC)



Flip-Flops

7476, LS76

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	$\overline{CP}^{(2)}$	J	K	Q	\bar{Q}
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (Clear)	H	L	X	X	X	L	H
Undetermined ⁽¹⁾	L	L	X	X	X	H	H
Toggle	H	H	\downarrow	h	h	\bar{q}	q
Load "0" (Reset)	H	H	\downarrow	l	h	L	H
Load "1" (Set)	H	H	\downarrow	h	l	H	L
Hold "no change"	H	H	\downarrow	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.⁽³⁾
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.⁽³⁾
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 \downarrow = Positive Clock pulse.

NOTES:

- Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.
- The 74LS76 is edge triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.
- The J and K inputs of the 7476 must be stable while the Clock is HIGH for conventional operation.

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Flip-Flops

7476, LS76

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	2.0			2.0			V
V_{IL}			+0.8			+0.8	V
I_{IK}			-12			-18	mA
I_{OH}			-400			-400	μ A
I_{OL}			16			8	mA
T_A	0		70	0		70	°C

Flip-Flops

7476, LS76

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7476			74LS76			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4	0.35	0.5	V	
		I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	J, K Inputs					0.1	mA
			\bar{S}_D, \bar{R}_D Inputs					0.3	mA
			$\bar{C}\bar{P}$ Inputs					0.4	mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V	J, K Inputs			40		μ A	
			\bar{S}_D, \bar{R}_D Inputs			80		μ A	
			$\bar{C}\bar{P}$ Inputs			80		μ A	
		V _I = 2.7V	J, K Inputs					20	μ A
			\bar{S}_D, \bar{R}_D Inputs					60	μ A
			$\bar{C}\bar{P}$ Inputs					80	μ A
I _{IL}	LOW-level input current ³ V _{CC} = MAX, V _I = 0.4V	J, K Inputs			-1.6		-0.4	mA	
		\bar{S}_D, \bar{R}_D Inputs			-3.2		-0.8	mA	
		$\bar{C}\bar{P}$ Inputs			-3.2		-0.8	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-57	-20		-100	mA	
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		10	40		4	8	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open. I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.
- \bar{S}_D is tested with \bar{R}_D HIGH, and \bar{R}_D is tested with \bar{S}_D HIGH.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency Waveform 3	15		30		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to output Waveform 1, 'LS76 Waveform 3, '76			25 40	20 30	ns
t _{PLH} t _{PHL}	Propagation delay \bar{S}_D or \bar{R}_D to output Waveform 2			25 40	20 30	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width of duty cycle.

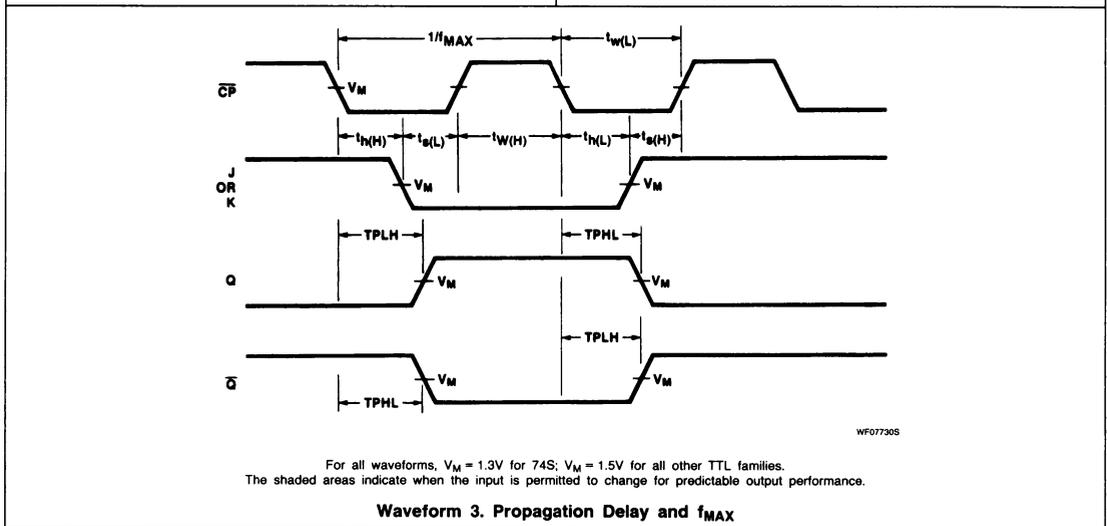
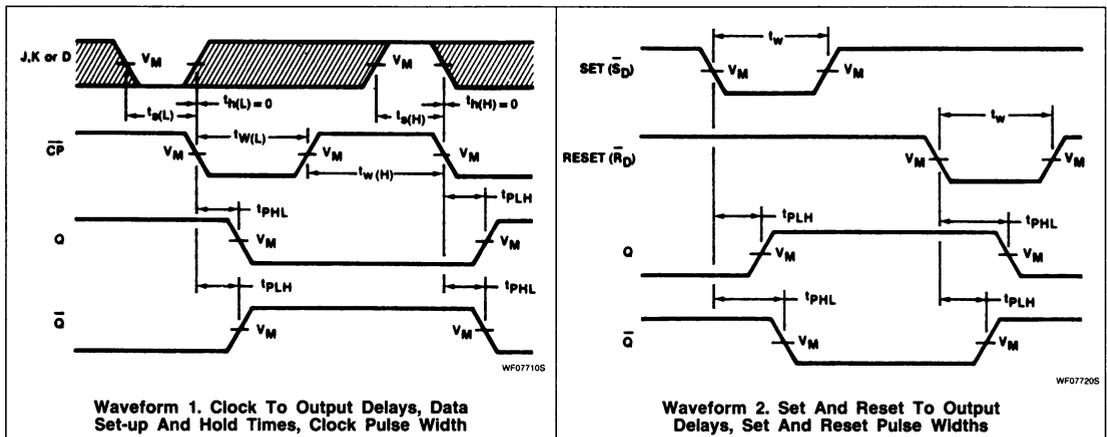
Flip-Flops

7476, LS76

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	47				ns
$t_{W(L)}$ Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s Set-up time J or K to Clock ^(C)	Waveform 1	0		20		ns
t_h Hold time J or K to Clock	Waveform 1	0		0		ns

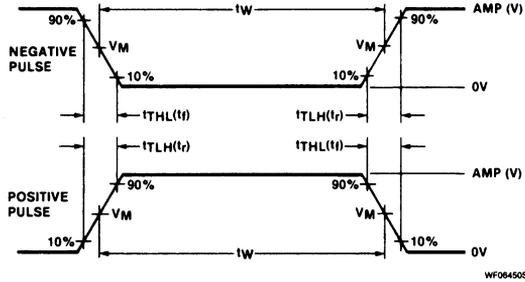
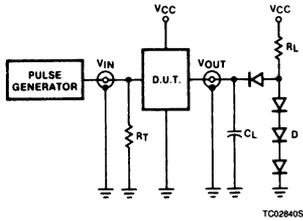
AC WAVEFORMS



Flip-Flops

7476, LS76

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7483, LS83A Adders

4-Bit Full Adder Product Specification

Logic Products

FEATURES

- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- LS83A has fast internal carry lookahead
- See '283 for corner power pin version

DESCRIPTION

The '83 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '83 can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). See Function Table. With active-HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN} , A_1 , B_1 , can arbitrarily be assigned to pins 10, 11, 13, etc.

TYPE	TYPICAL ADD TIMES (TWO 8-BIT WORDS)	TYPICAL SUPPLY CURRENT (TOTAL)
7483	23ns	66mA
74LS83A	25ns	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7483N, N74LS83AN
Plastic SO	N74LS83AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

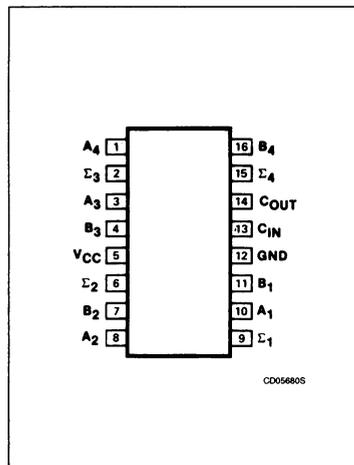
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
$A_1, B_1, A_3, B_3, C_{IN}$	Inputs	2ul	
A_2, B_2, A_4, B_4	Inputs	1ul	
A, B	Inputs		2LSul
C_{IN}	Input		1LSul
Sum	Outputs	10ul	10LSul
Carry	Output	5ul	10LSul

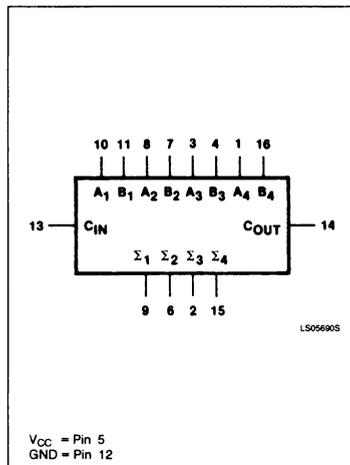
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

PIN CONFIGURATION

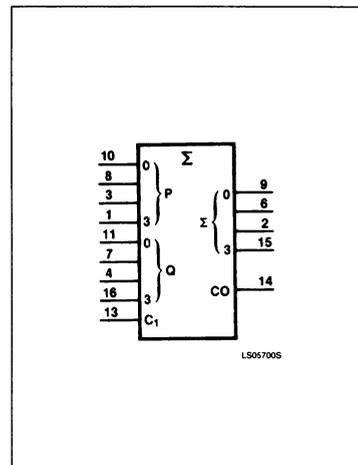


LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

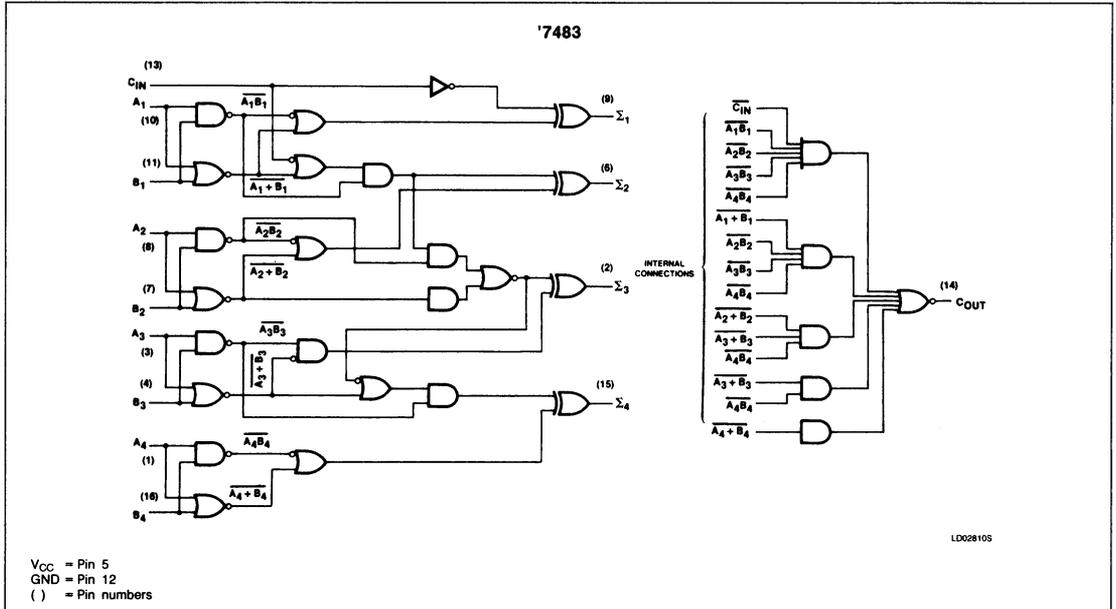
LOGIC SYMBOL (IEEE/IEC)



Adders

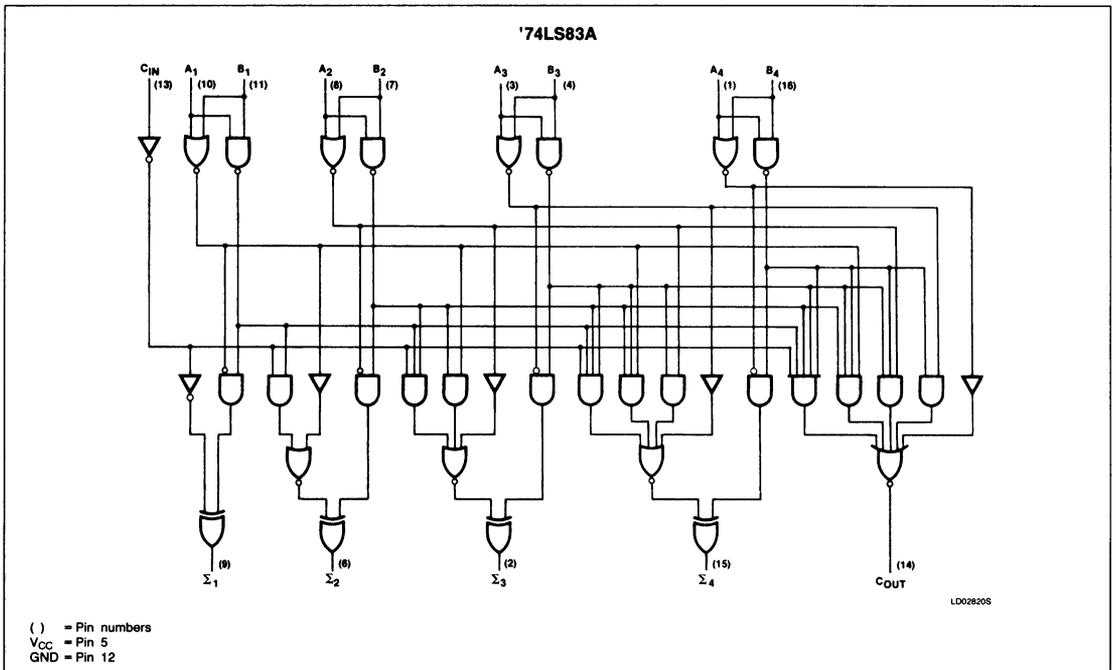
7483, LS83A

LOGIC DIAGRAM



5

LOGIC DIAGRAM



Adders

7483, LS83A

FUNCTION TABLE

PINS	C _{IN}	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C _{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10 + 9 = 19)
(carry + 5 + 6 = 12)

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current	Sum		-800			-400	μA
		Carry		-400			-400	μA
I _{OL}	LOW-level output current	Sum		16			8	mA
		Carry		8			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

Adders

7483, LS83A

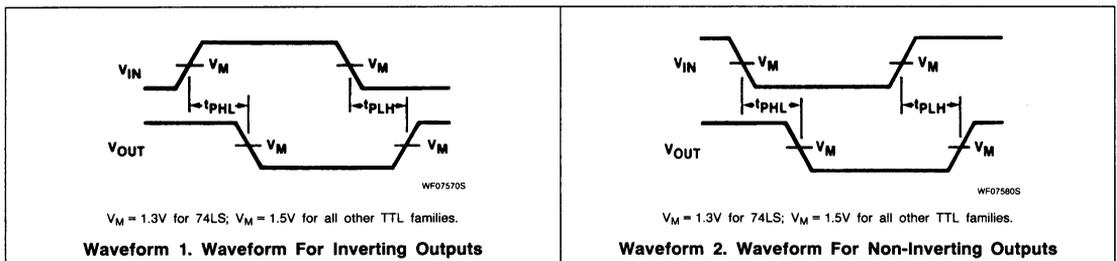
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7483			74LS83A			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX				0.35	0.5	V	
		I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA
		V _I = 7.0V	A, B inputs					0.2	mA
			C _{IN} input					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	A ₁ , B ₁ , A ₃ , B ₃ , C _{IN}			80			μA
			A ₂ , B ₂ , A ₄ , B ₄			40			μA
		V _I = 2.7V	A, B inputs					40	μA
			C _{IN} input					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX V _I = 0.4V	A ₁ , B ₁ , A ₃ , B ₃ , C _{IN}			-3.2			mA	
		A ₂ , B ₂ , A ₄ , B ₄			-1.6			mA	
		A, B inputs					-0.8	mA	
		C _{IN} input					-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Sum outputs		-18	-55	-20	-100	mA	
		C _{OUT} output		-18	-70	-20	-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX outputs open	All inputs at 4.5V			66	110	19	34	mA
		All inputs grounded					22	39	mA
		All B inputs low, other inputs at 4.5V					19	34	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



Adders

7483, LS83A

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 50\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_1	Waveforms 1 & 2		34 34		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_2	Waveforms 1 & 2		35 35		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_3	Waveforms 1 & 2		50 40		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_4	Waveforms 1 & 2		50 50		24 24	ns
t_{PLH} t_{PHL} Propagation delay A_i or B_i to Σ_i	Waveforms 1 & 2		40 35		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to C_{OUT}	Waveform 2 $R_L = 780\Omega$ for 7483		20 20		17 22	ns
t_{PLH} t_{PHL} Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 & 2 $R_L = 780\Omega$ for 7483		22 22		17 17	ns

TEST CIRCUITS AND WAVEFORMS

TC028405

WF064505

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS
 R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

7485, LS85, S85 Comparators

4-Bit Magnitude Comparator Product Specification

Logic Products

FEATURES

- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating
- Use 74S85 for very high speed comparisons

DESCRIPTION

The '85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted ($A_0 - A_3$) and ($B_0 - B_3$), where A_3 and B_3 are the most significant bits.

The operation of the '85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7485	23ns	55mA
74LS85	23ns	10mA
74S85	12ns	73mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7485N, N74LS85N, N74S85N
Plastic SO	N74LS85D, N74S85D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

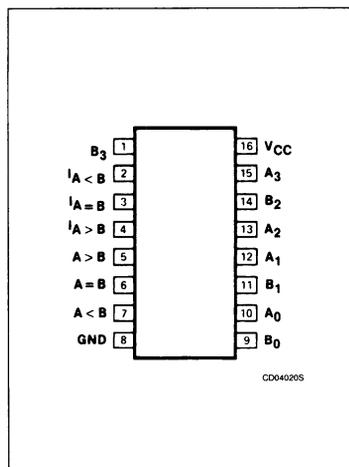
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
$A_0 - A_3, B_0 - B_3, I_A = B$	Inputs	3ul	3Sul	3LSul
$I_A < B, I_A > B$	Inputs	1ul	1Sul	1LSul
$A = B, A < B, A > B$	Outputs	10ul	10Sul	10LSul

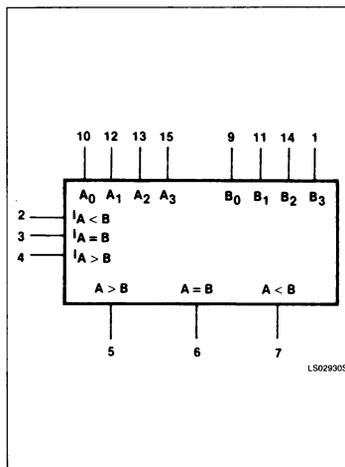
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

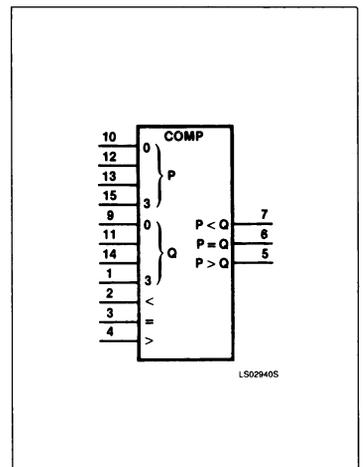
PIN CONFIGURATION



LOGIC SYMBOL



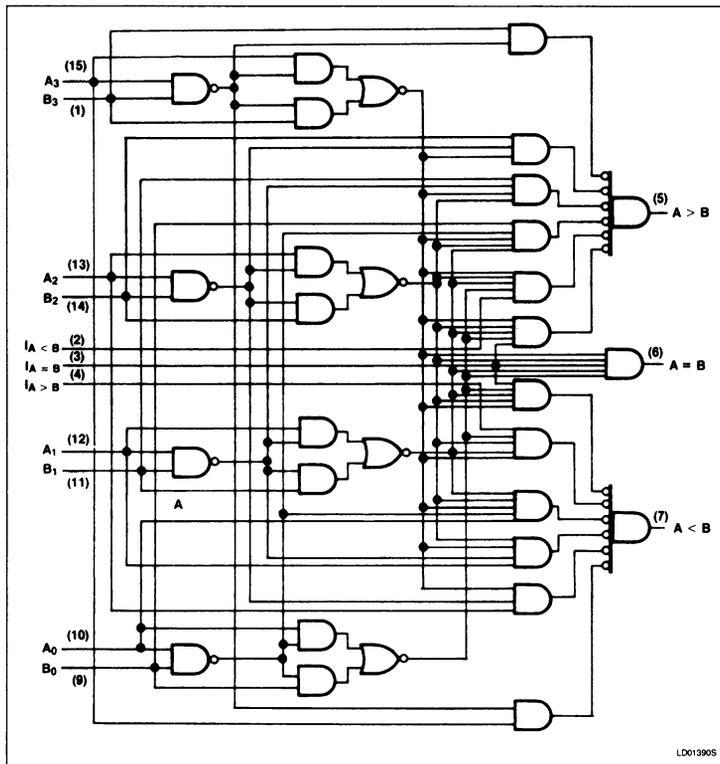
LOGIC SYMBOL (IEEE/IEC)



Comparators

7485, LS85, S85

LOGIC DIAGRAM



In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs I_{A > B}, I_{A = B}, and I_{A < B} are the least significant bit positions. When used for series expansion, the A > B, A = B and A < B outputs of the least significant word are connected to the corresponding I_{A > B}, I_{A = B}, and I_{A < B} inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: I_{A > B} = LOW, I_{A = B} = HIGH, and I_{A < B} = LOW.

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling I_{A > B} as an "A" input, I_{A < B} as a "B" input and setting I_{A = B} LOW. The '85 can be used as a 5-bit comparator only when the outputs are used to drive the (A₀ - A₃) and (B₀ - B₃) inputs of another '85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

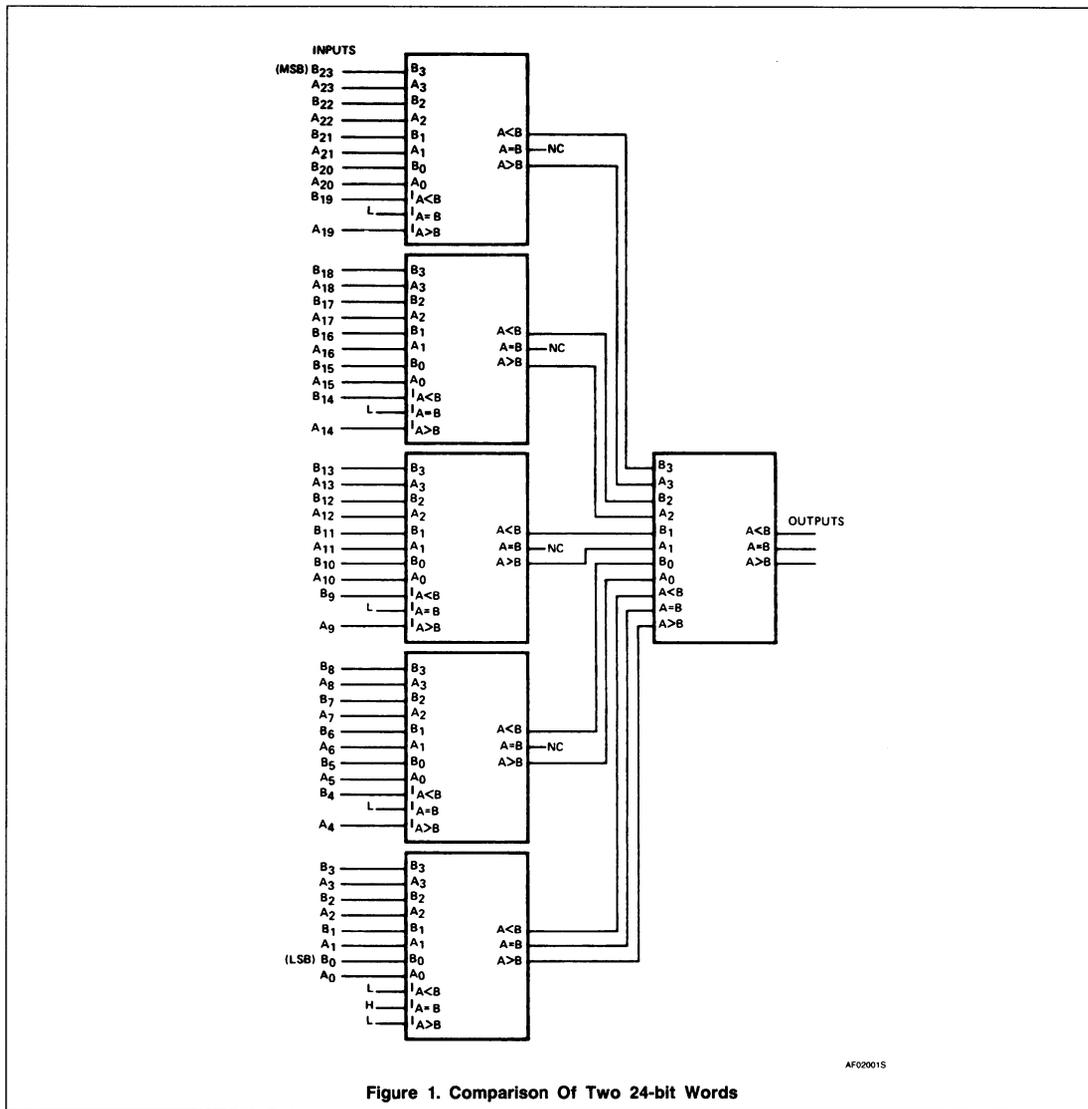
FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A > B}	I _{A < B}	I _{A = B}	A > B	A < B	A = B
A ₃ > B ₃	X	X	X	X	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	X	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	H	L	L	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

Comparators

7485, LS85, S85



AF02001S

Table 1

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS		
		74	74S	74LS
1 - 4 Bits	1	23ns	12ns	23ns
5 - 25 Bits	2 - 6	40ns	22ns	46ns
25 - 120 Bits	8 - 31	63ns	34ns	69ns

Comparators

7485, LS85, S85

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18			-18	mA
I _{OH}	HIGH-level output current			-400			-400			-1000	μA
I _{OL}	LOW-level output current			16			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	0		70	°C

Comparators

7485, LS85, S85

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7485			74LS85			74S85			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA
		V _I = 7.0V	I _A < B, I _A > B					0.1			mA
			Other inputs					0.3			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	I _A < B, I _A > B			40					μA
			Other inputs			120					μA
		V _I = 2.7V	I _A < B, I _A > B					20		50	μA
			Other inputs					60		150	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	I _A < B, I _A > B			-1.6		-0.4			mA
			Other inputs			-4.8		-1.2			mA
		V _I = 0.5V	I _A < B, I _A > B							-2.0	mA
			Other inputs							-6.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		55	88		10.4	20		73	115	mA
	S54S85W only, T _A = 125°C									110	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5V.

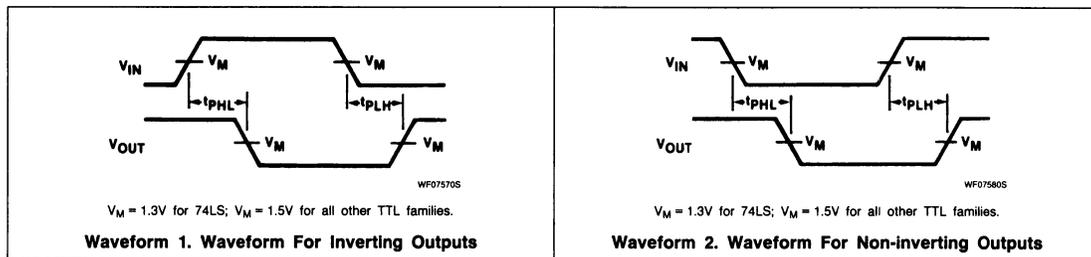
Comparators

7485, LS85, S85

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output Waveform 1 3 logic levels		26 30		36 30		16 16.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output Waveform 2 4 logic levels		35 30		45 45		18 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_A < B$ and $I_A = B$ input to A > B output Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_A = B$ input to A = B output Waveform 2 2 logic levels		20 17		20 26		10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_A > B$ and $I_A = B$ input to A < B output Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns

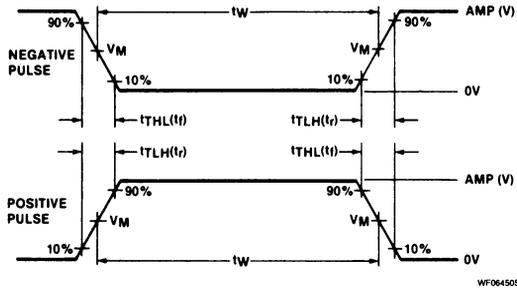
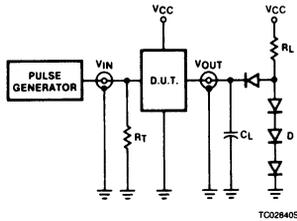
AC WAVEFORMS



Comparators

7485, LS85, S85

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7486, LS86, S86 Gates

Quad Two-Input Exclusive-OR Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7486	14ns	30mA
74LS86	10ns	6.1mA
74S86	7ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7486N, N74LS86N, N74S86N
Plastic SO	N74LS86D, N74S86D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

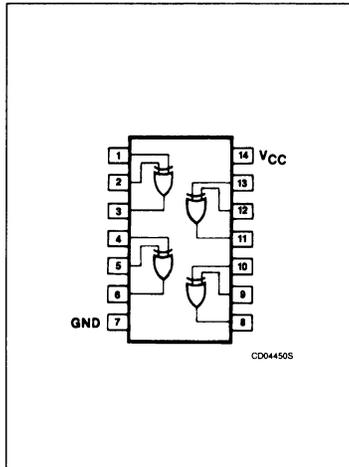
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

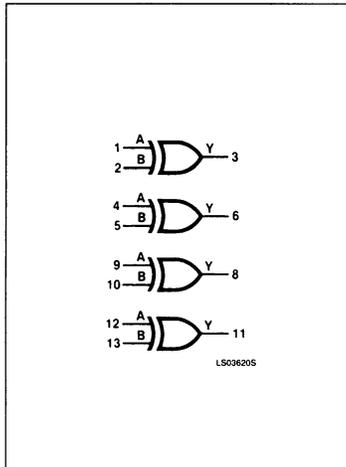
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

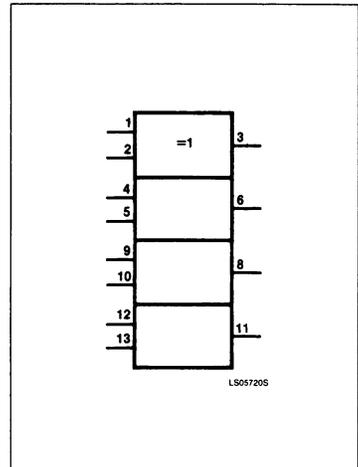
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

7486, LS86, S86

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

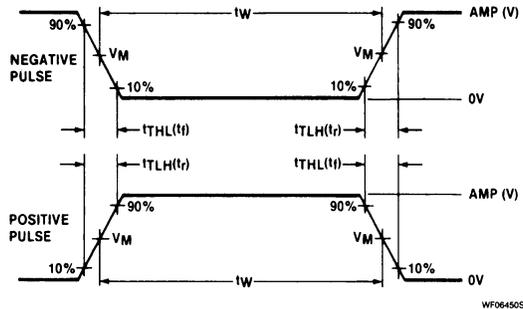
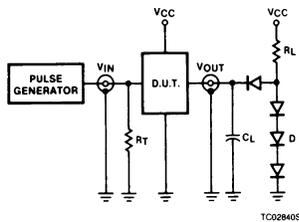
PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS					
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}	
74	3.0V	1MHz	500ns	7ns	7ns	
74LS	3.0V	1MHz	500ns	15ns	6ns	
74S	3.0V	1MHz	500ns	2.5ns	2.5ns	

Gates

7486, LS86, S86

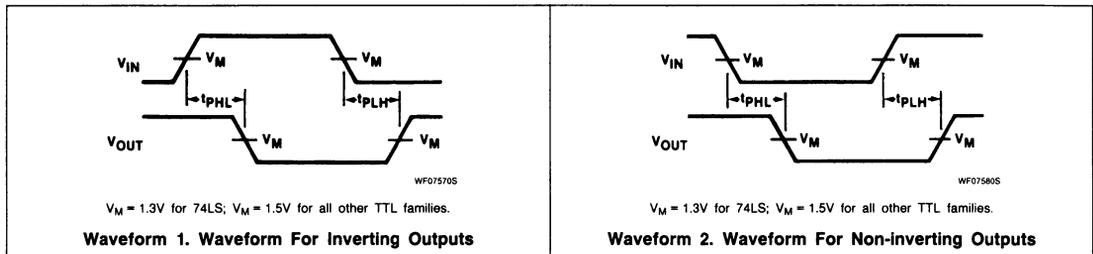
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7486			74LS86			74S86			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5		-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA
		V _I = 7.0V					0.2				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA
		V _I = 2.7V					40		50		μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.8			mA
		V _I = 0.5V							-2.0		mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-15		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		30	50		6.1	10		50	75	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with inputs grounded an outputs open.

AC WAVEFORMS



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay A or B to output	Other input LOW Waveform 2		23		23		10.5	ns
t _{PHL} Propagation delay A or B to output	Other input HIGH Waveform 1		17		17		10	
t _{PLH} Propagation delay A or B to output	Other input LOW Waveform 2		30		30		10.5	ns
t _{PHL} Propagation delay A or B to output	Other input HIGH Waveform 1		22		22		10	

7490, LS90 Counters

Decade Counter
Product Specification

Logic Products

DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the CP_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7490	30MHz	30mA
74LS90	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7490N, N74LS90N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
\overline{CP}_0	Input	2ul	6LSul
\overline{CP}_1	Input	4ul	8LSul
MR, MS	Inputs		1ul
$Q_0 - Q_3$	Outputs	10ul	10LSul

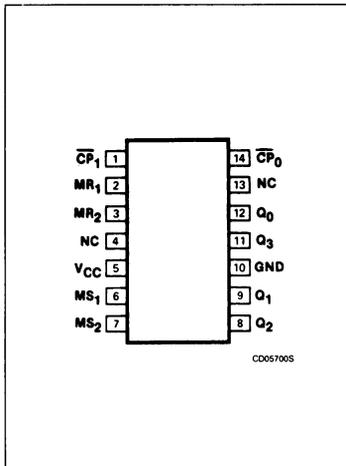
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

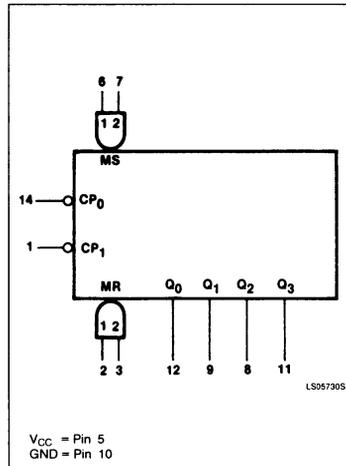
counter the Q_3 output must be connected externally to the \overline{CP}_0 input. The input count is then applied to the CP_1 input and a divide-by-ten square wave is obtained at output Q_0 . To operate as a divide-by-two and a divide-by-five count-

er no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain a divide-by-five operation at the Q_3 output.

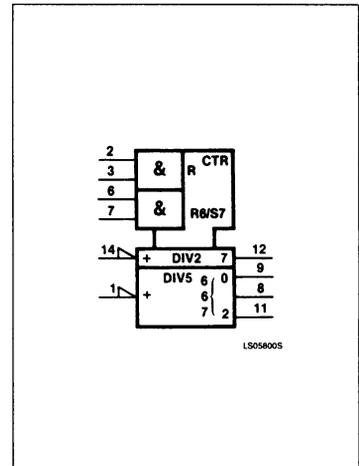
PIN CONFIGURATION



LOGIC SYMBOL



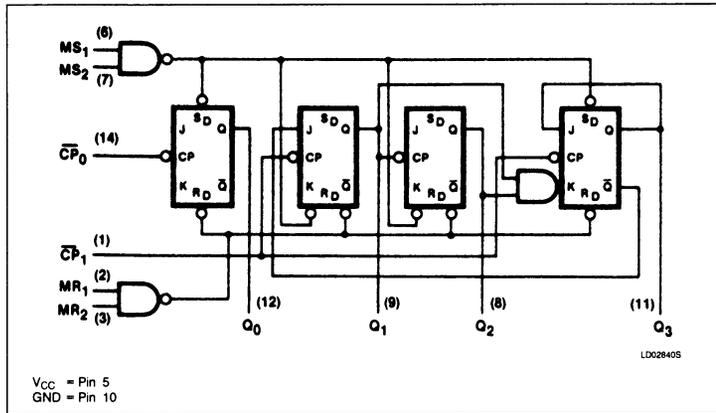
LOGIC SYMBOL (IEEE/IEC)



Counters

7490, LS90

LOGIC DIAGRAM



MODE SELECTION — FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X				Count
X	L	X	L				Count
L	X	X	L				Count
H	L	L	X				Count

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE — FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE:
Output Q₀ connected to input \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

NOTE:
V_{IN} is limited to +5.5V on \overline{CP}_0 and \overline{CP}_1 inputs on the 74LS90 only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

Counters

7490, LS90

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		7490			74LS90			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _i = I _{IK}				-1.5			-1.5	V	
I _i Input current at maximum input voltage	V _{CC} = MAX	V _i = 5.5V	All inputs '90			1.0			mA	
		V _i = 7.0V	MR, MS inputs					0.1	mA	
		V _i = 5.5V	\overline{CP}_0 input						0.2	mA
			\overline{CP}_1 input						0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _i = 2.4V	MR, MS inputs			40			μ A	
			\overline{CP}_0 input			80			μ A	
			\overline{CP}_1 input			160			μ A	
		V _i = 2.7V	MR, MS inputs						20	μ A
			\overline{CP}_0 input ⁵						40	μ A
			\overline{CP}_1 input ⁵						80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX	V _i = 0.4V	MR, MS inputs			-1.6		-0.4	mA	
			\overline{CP}_0 input			-3.2		-2.4	mA	
			\overline{CP}_1 input			-6.4		-3.2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-55	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			30	53		9	15	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
- The maximum limit for the 54LS90 only is 80 μ A for \overline{CP}_0 and 160 μ A for \overline{CP}_1 inputs.

Counters

7490, LS90

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX}	Input count frequency, $\overline{\text{CP}}_0$ to Q_0	10		32		MHz
f_{MAX}	Input count frequency, $\overline{\text{CP}}_1$ to Q_1	10		16		
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ input to Q_0 output				16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ input to Q_1 output				16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ input to Q_2 output				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ input to Q_3 output				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ input to Q_3 output		100 100		48 50	ns
t_{PHL}	MR input to any output				40	ns
t_{PLH}	MS input to Q_0 and Q_3 outputs				30	ns
t_{PHL}	MS input to Q_1 and Q_2 outputs				40	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

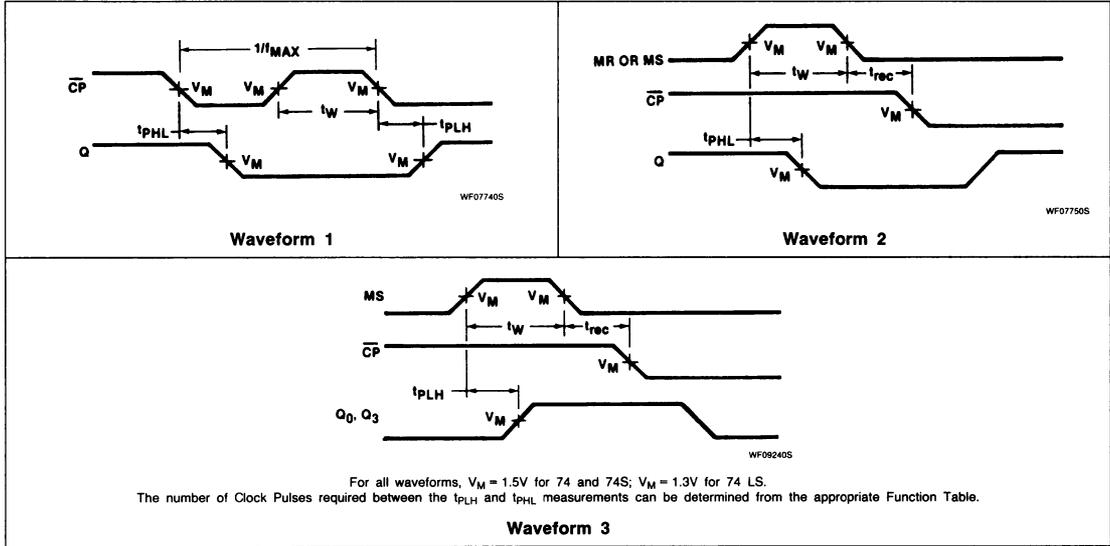
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_w	$\overline{\text{CP}}_0$ pulse width	50		15		ns
t_w	$\overline{\text{CP}}_1$ pulse width	50		30		ns
t_w	MS, MR pulse width	50		15		ns
t_{rec}	Recovery time, MR to $\overline{\text{CP}}$			25		ns
t_{rec}	Recover time, MS to $\overline{\text{CP}}$			25		ns

Counters

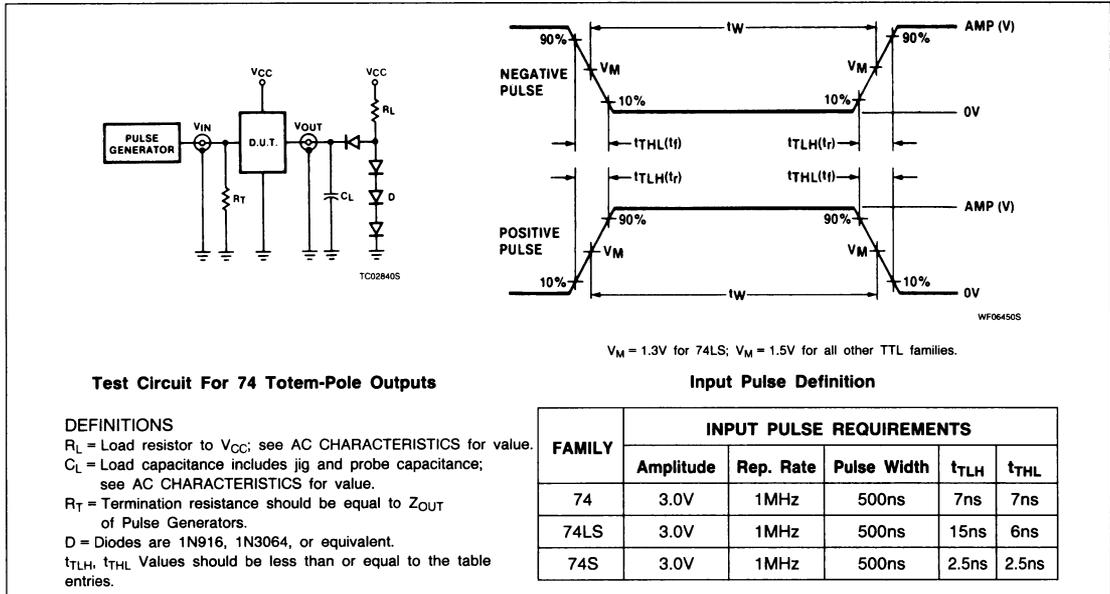
7490, LS90

AC WAVEFORMS



5

TEST CIRCUITS AND WAVEFORMS



7491A Register

8-Bit Shift Register
Product Specification

Logic Products

FEATURES

- 8-bit serial-in-serial-out shift register
- Common buffered clock
- 2-input gate for serial data entry
- True and Complement outputs

DESCRIPTION

The '91A is an 8-bit serial-in-serial-out shift register. The serial data is entered through a 2-input AND gate (D_{Sa} and D_{Sb}). HIGH data is entered when both D_{Sa} and D_{Sb} are HIGH. LOW data is entered when either Serial Data input is LOW. The Data inputs are edge-triggered and must be stable just one set-up time prior to the LOW-to-HIGH transition of the Clock input (CP) for predictable operation. The data is shifted one bit to the right ($Q_0 \rightarrow Q_1 \rightarrow \dots \rightarrow Q_7$) synchronous with each LOW-to-HIGH clock transition. The '91A has no reset capability, so initialization requires the shifting in of at least 8 bits of known data.

Once the register is fully loaded, the Q output follows the Serial inputs delayed by eight clock pulses. The Complement (\bar{Q}) output from the last stage is also available for simpler decoding applications.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7491A	18MHz	3.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7491AN

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

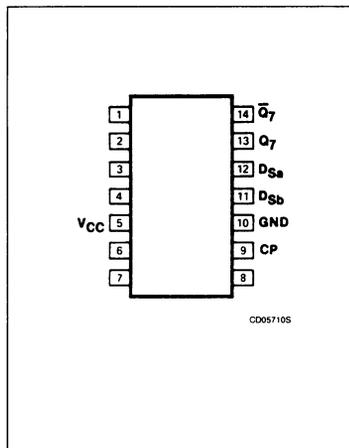
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1uI
All	Outputs	10uI

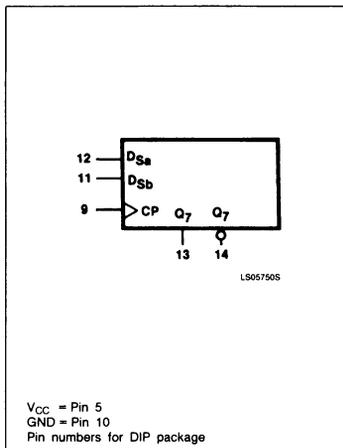
NOTE:

A 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

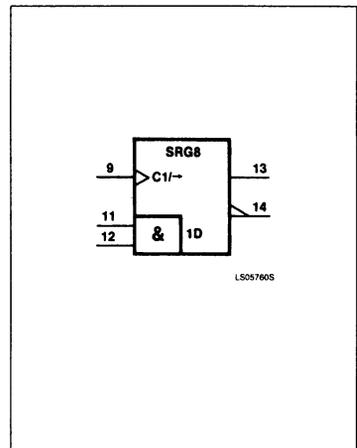
PIN CONFIGURATION



LOGIC SYMBOL



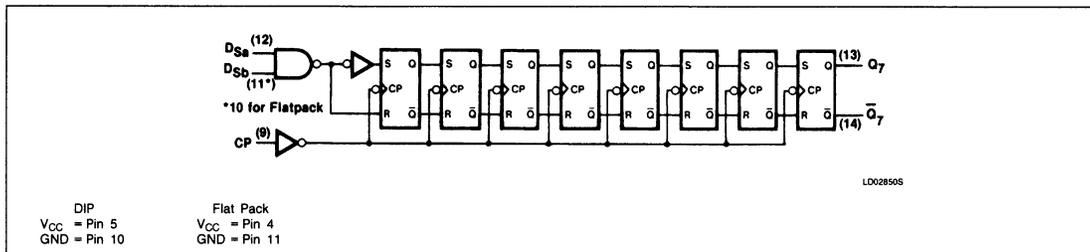
LOGIC SYMBOL (IEEE/IEC)



Register

7491A

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			FIRST STAGE		OUTPUTS	
	CP	D _{Sa}	D _{Sb}	Q ₀	Q ₀ ⁻	Q ₇	Q ₇ ⁻
Shift, reset first stage	↑	l	X	L	H	q ₆	q ₆ ⁻
Shift, set first stage	↑	X	l	L	H	q ₆	q ₆ ⁻
Shift, set first stage	↑	h	h	H	L	q ₆	q ₆ ⁻

H = HIGH voltage level.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 q_n = Lower case letters indicate the state of the referenced register output one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage			2.0	V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
I _{OH} HIGH-level output current			-400	μA
I _{OL} LOW-level output current			16	mA
T _A Operating free-air temperature	0		70	°C

5

Register

7491A

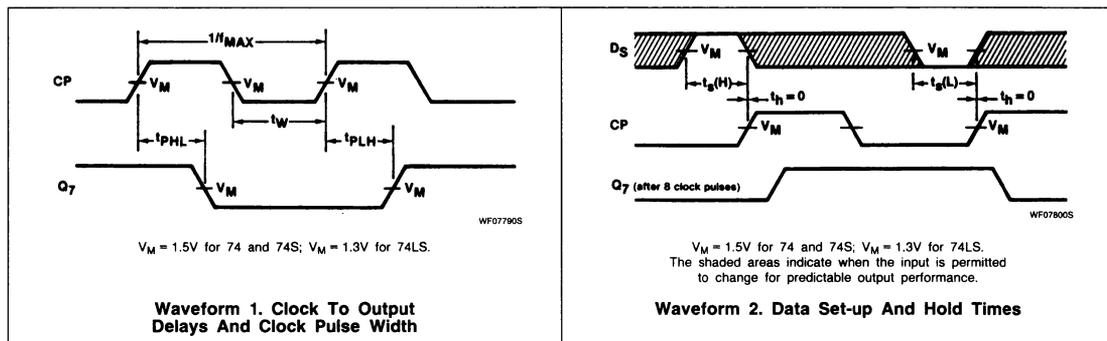
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7491A			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		35	58	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- All typical values are at V_{CC} = +0.5V and V_{CC} = V_{CC}MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after the eighth clock pulse with the output open and D_{Sa} and D_{Sb} inputs grounded.

AC WAVEFORMS



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	10		MHz
t _{PLH} Propagation delay	Waveform 1		40	ns
t _{PHL} Clock to output			40	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

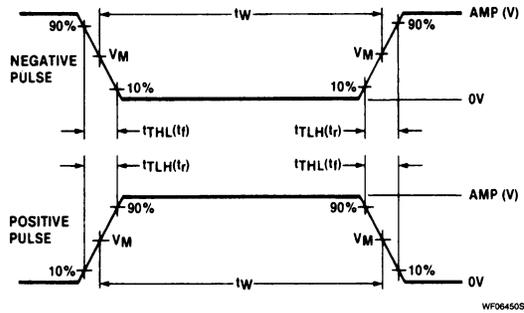
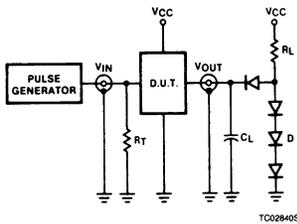
Register

7491A

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t_w Clock pulse width	Waveform 1	25		ns
t_s Set-up time, data to clock	Waveform 2	25		ns
t_h Hold time, data to clock	Waveform 2	0		ns

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

5

7492, LS92 Counters

Divide-By-Twelve Counter
Product Specification

Logic Products

DESCRIPTION

The '92 is a 4-bit, ripple-type Divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-six section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR_1 - MR_2) is provided which overrides both clocks and resets (clears) all the flip-flops.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7492	28MHz	28mA
74LS92	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7492N, N74LS92N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

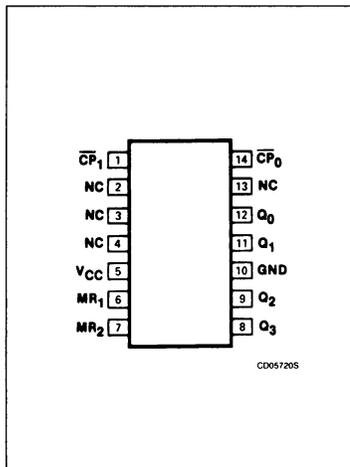
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
MR	Master reset inputs	1ul	1LSul
CP_0	Input	2ul	6LSul
CP_1	Input	4ul	8LSul
$Q_0 - Q_3$	Outputs	10ul	10LSul

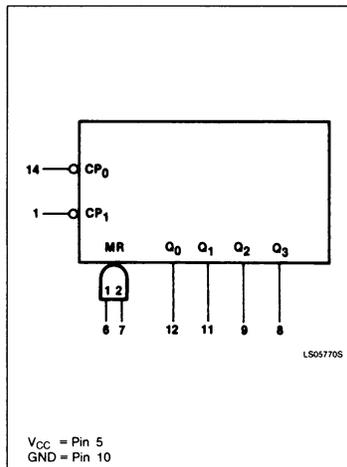
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

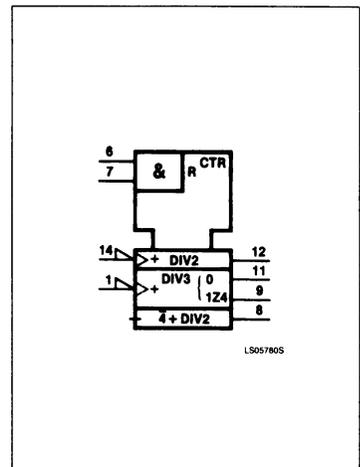
PIN CONFIGURATION



LOGIC SYMBOL



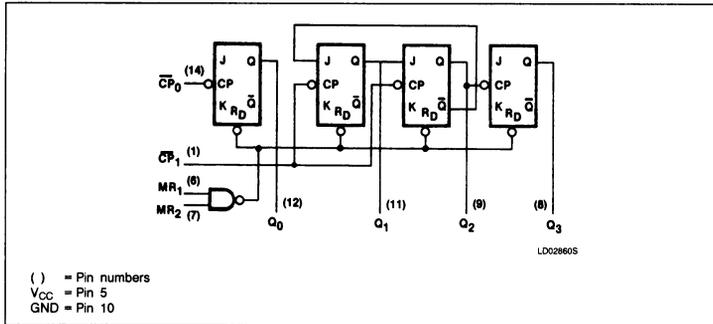
LOGIC SYMBOL (IEEE/IEC)



Counters

7492, LS92

LOGIC DIAGRAM



Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a Modulo-12, Divide-by-12 Counter the \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count and Q_3 produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The \overline{CP}_1 input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H				Count
H	L				Count
L	L				Count

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

NOTE:

Output Q_0 connected to input \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

NOTE:

V_{IN} is limited to 5.5V on \overline{CP}_0 and \overline{CP}_1 inputs only on the 74LS92.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

Counters

7492, LS92

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		7492			74LS92			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V All inputs '92			1.0				mA	
		V _I = 7.0V MR inputs						0.1	mA	
		V _I = 5.5V	\overline{CP}_0 input						0.2	mA
			\overline{CP}_1 input						0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	MR inputs			40			μ A	
			\overline{CP}_0 input			80			μ A	
			\overline{CP}_1 input			160			μ A	
		V _I = 2.7V	MR inputs						20	μ A
			\overline{CP}_0 input ⁵						40	μ A
			\overline{CP}_1 input ⁵						80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	MR inputs			-1.6			-0.4	mA
			\overline{CP}_0 input			-3.2			-2.4	mA
			\overline{CP}_1 input			-6.4			-3.2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-55	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX				51		9	15	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
- The maximum limit for the 54LS92 only is 80 μ A for \overline{CP}_0 and 160 μ A for \overline{CP}_1 inputs.

Counters

7492, LS92

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX}	\overline{CP}_0 input count frequency	Waveform 1	10		32	MHz
f_{MAX}	\overline{CP}_1 input count frequency	Waveform 1	10		16	
t_{PLH} t_{PHL}	Propagation delay \overline{CP}_0 input to Q_0 output	Waveform 1			16 18	ns
t_{PLH} t_{PHL}	Propagation delay \overline{CP}_1 input to Q_1 output	Waveform 1			16 21	ns
t_{PLH} t_{PHL}	Propagation delay \overline{CP}_1 input to Q_2 output	Waveform 1			16 21	ns
t_{PLH} t_{PHL}	Propagation delay \overline{CP}_1 input to Q_3 output	Waveform 1			32 35	ns
t_{PLH} t_{PHL}	Propagation delay \overline{CP}_0 input to Q_3 output	Waveform 1	100 100		48 50	ns
t_{PHL}	\overline{MR} input to any output	Waveform 2			40	ns

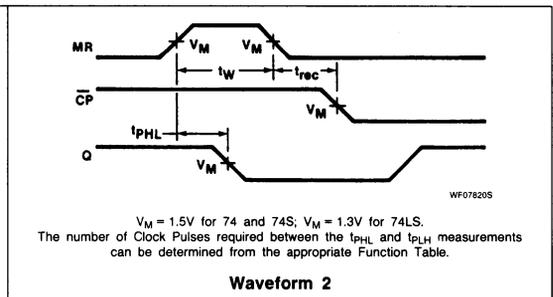
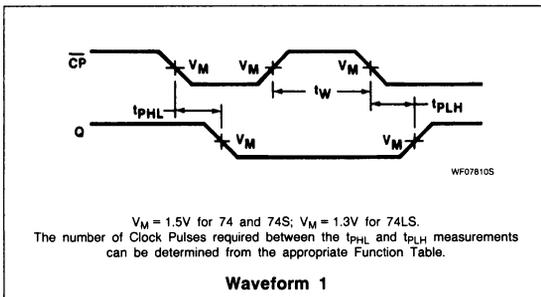
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W	\overline{CP}_0 pulse width	Waveform 1	50		15	ns
t_W	\overline{CP}_1 pulse width	Waveform 1	50		30	ns
t_W	MR pulse width	Waveform 2	50		15	ns
t_{rec}	Recovery time, MR to \overline{CP}	Waveform 2			25	ns

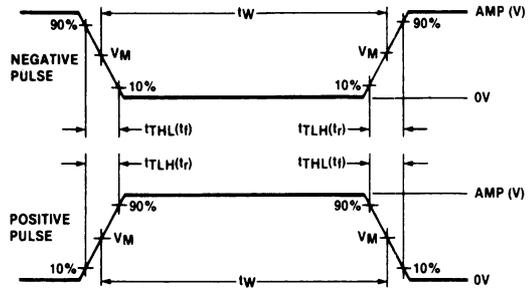
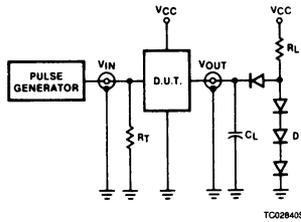
AC WAVEFORMS



Counters

7492, LS92

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{TlL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{TlL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7493, LS93 Counters

4-Bit Binary Ripple Counter Product Specification

Logic Products

DESCRIPTION

The '93 is a 4-bit, ripple-type Binary Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR_1 , MR_2) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input \overline{CP}_1 .

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7493	40MHz	28mA
74LS93	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7493N, N74LS93N
Plastic SO	N74LS93D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

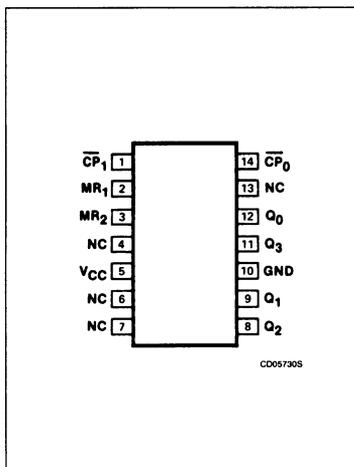
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
MR	Master reset inputs	1uI	1LSuI
\overline{CP}_0	Input	2uI	6LSuI
\overline{CP}_1	Input	2uI	4LSuI
$Q_0 - Q_3$	Outputs	10uI	10LSuI

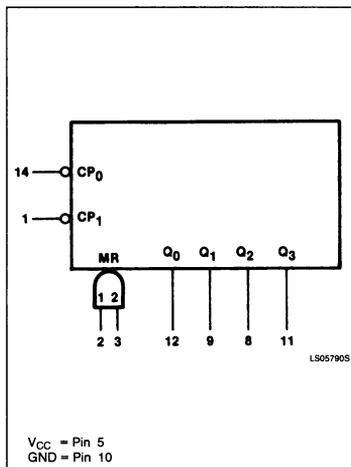
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

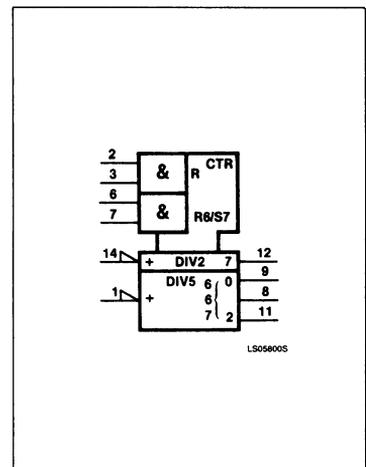
PIN CONFIGURATION



LOGIC SYMBOL



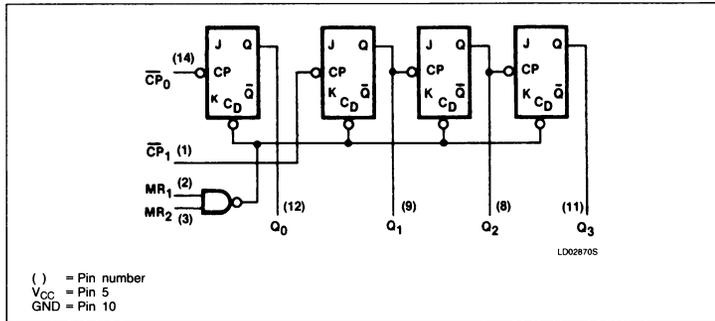
LOGIC SYMBOL (IEEE/IEC)



Counters

7493, LS93

LOGIC DIAGRAM



The input count pulses are applied to input \overline{CP}_0 . Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0 , Q_1 , Q_2 and Q_3 outputs as shown in the Function Table.

As a 3-bit ripple counter the input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1 , Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

NOTE:
 Output Q_0 connected to input \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	2.0			2.0			V
V_{IL}			+0.8			+0.8	V
I_{IK}			-12			-18	mA
I_{OH}			-800			-400	μA
I_{OL}			16			8	mA
T_A	0		70	0		70	°C

Counters

7493, LS93

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7493			74LS93			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		0.2	0.4		0.35	0.5	V
	I _{OL} = MAX I _{OL} = 4mA (74LS)					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	All inputs '93		1.0			mA
		V _I = 7.0V	MR inputs				0.1	mA
		V _I = 5.5V	CP ₀ , CP ₁ inputs				0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	MR inputs		40			μA
			CP ₀ , CP ₁ inputs		80			μA
		V _I = 2.7V	MR inputs				20	μA
			CP ₀ , CP ₁ inputs ⁵				40	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	MR inputs		-1.6		-0.4	mA
			CP ₀ input		-3.2		-2.4	mA
			CP ₁ input		-3.2		-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-55	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		28	53		9	15	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
- The maximum limit for the 54LS93 only is 80μA for CP₀ and CP₁ inputs.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
f _{MAX} CP ₀ input count frequency	Waveform 1	10		32		MHz
f _{MAX} CP ₁ input count frequency		10		16		
t _{PLH} Propagation delay	Waveform 1				16	ns
t _{PHL} CP ₀ input to Q ₀ output					18	
t _{PLH} Propagation delay	Waveform 1				16	ns
t _{PHL} CP ₁ input to Q ₁ output					21	
t _{PLH} Propagation delay	Waveform 1				32	ns
t _{PHL} CP ₁ input to Q ₂ output					35	
t _{PLH} Propagation delay	Waveform 1				51	ns
t _{PHL} CP ₁ input to Q ₃ output					51	
t _{PLH} Propagation delay	Waveform 1		135		70	ns
t _{PHL} CP ₀ input to Q ₃ output			135		70	
t _{PHL} MR input to any output	Waveform 2				40	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Counters

7493, LS93

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W	\overline{CP}_0 pulse width	50		15		ns
t_W	\overline{CP}_1 pulse width	50		30		ns
t_W	MR pulse width	50		15		ns
t_{rec}	Recovery time, MR to \overline{CP}			25		ns

AC WAVEFORMS

WF07830S

Waveform 1

WF07840S

Waveform 2

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.
 The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

TEST CIRCUITS AND WAVEFORMS

TC02840S

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS
 R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7494

Shift Register

4-Bit Shift Register
Product Specification

Logic Products

FEATURES

- 4-bit parallel-to-serial converter
- Two asynchronous ones transfer parallel data ports
- Buffered active HIGH Master Reset
- Buffered positive edge-triggered clock

DESCRIPTION

The '94 is a 4-bit shift register with serial and parallel (ones transfer) data entry. To facilitate parallel ones transfer from two sources, two Parallel Load inputs (PL₀ and PL₁) with associated Parallel Data inputs (D_{0a}-D_{0d} and D_{1a}-D_{1d}) are provided. To accommodate these extra inputs only the output of the last stage is available. The asynchronous Master Reset (MR) is active HIGH. When MR is HIGH, it overrides the clock and clears the register, forcing Q_d LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
7494	25ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V ±5%; T _A = 0°C to +70°C
Plastic DIP	N7494N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

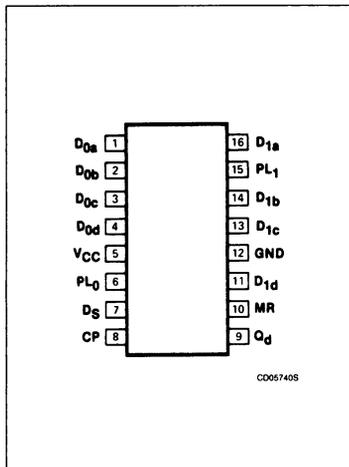
PINS	DESCRIPTION	74
PL ₀ , PL ₁	Parallel load inputs	4ul
D _S , D _n , CP, MR	All other inputs	1ul
Q _d	Serial Data output	10ul

NOTE:

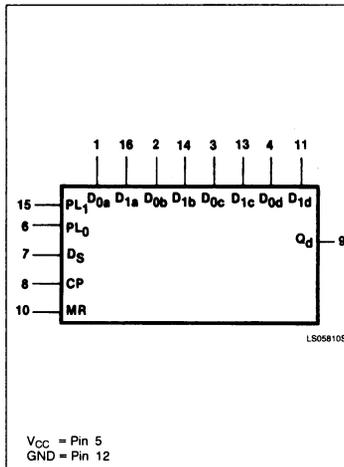
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and -1.6mA I_{IL}.

5

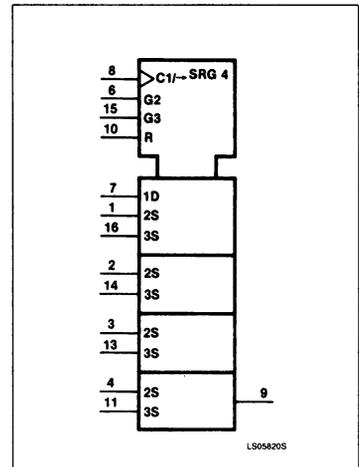
PIN CONFIGURATION



LOGIC SYMBOL



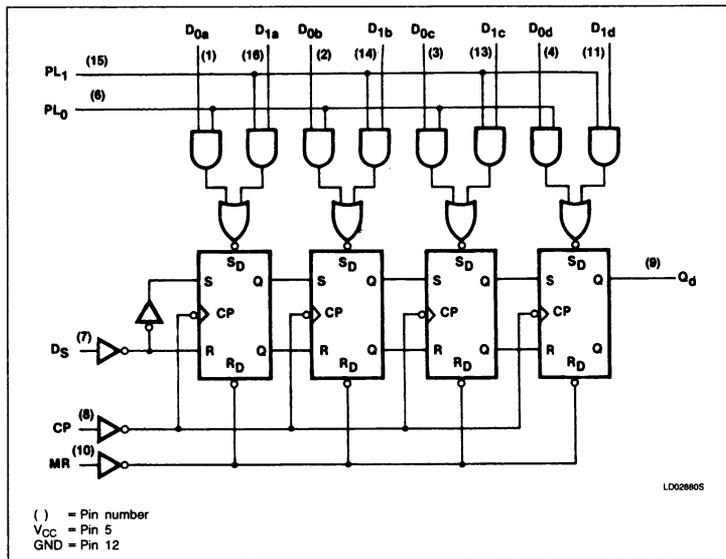
LOGIC SYMBOL (IEEE/IEC)



Shift Register

7494

LOGIC DIAGRAM



Four flip-flops are connected so that shifting is synchronous; they change state when the clock goes from LOW-to-HIGH. Data is accepted at the serial D_S input prior to this clock transition. Two Parallel Load inputs and Parallel Data inputs allow an asynchronous ones transfer from two sources. The flip-flops can be set independently to the HIGH state when the appropriate Parallel input is activated. Parallel inputs D_{0a} through D_{0d} are activated during the time the PL_0 is HIGH and Parallel inputs D_{1a} through D_{1d} are activated when PL_1 is HIGH. If both sets of inputs are activated, a HIGH on either input will set the flip-flops to a HIGH. The register should not be clocked while the Parallel Load inputs are activated. The Parallel Load and Parallel Data inputs will override the MR if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	PL_0	PL_1	D_{0n}	D_{1n}	MR	CP	D_S	Q_a	Q_b	Q_c	Q_d
Parallel load	H	L	L	X	X	X	X	Q_a	Q_b	Q_c	Q_d
	H	L	H	X	X	X	X	H	H	H	H
	L	H	X	L	X	X	X	Q_a	Q_b	Q_c	Q_d
	L	H	X	H	X	X	X	H	H	H	H
Reset (clear)	L	L	X	X	H	X	X	L	L	L	L
Shift right	L	L	X	X	L	\uparrow	l	L	q_a	q_b	q_c
	L	L	X	X	L	\uparrow	h	H	q_a	q_b	q_c

- H = HIGH voltage level.
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
- q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
- X = Don't care.
- \uparrow = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	$^{\circ}C$

Shift Register

7494

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-400	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7494			UNIT
		Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.4V	PL ₀ , PL ₁ inputs		160	μA
		Other inputs		40	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V	PL ₀ , PL ₁ inputs		-6.4	mA
		Other inputs		-1.6	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-57	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		35	58	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Parallel Load inputs grounded. Master Reset grounded following momentary application of 4.5V, all other inputs at 4.5V and outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 1		MHz
t _{PLH}	Propagation delay	Waveform 1		ns
t _{PHL}	Clock to output	40		
t _{PLH}	Propagation delay Parallel Load or Parallel Data to output	Waveform 2		ns
t _{PHL}	Propagation delay MR to output	Waveform 2		ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

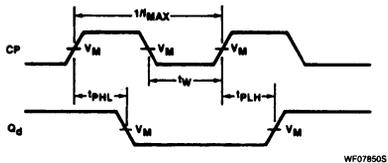
Shift Register

7494

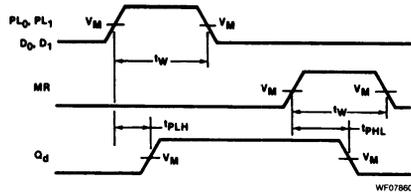
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS ¹	74		UNIT
		Min	Max	
$t_{W(L)}$ Clock pulse width, LOW	Waveform 1	35		ns
$t_{W(H)}$ MR pulse width, HIGH	Waveform 2	30		ns
$t_{W(H)}$ Parallel load or data pulse width, HIGH	Waveform 2	30		ns
$t_s(H)$ Set-up time HIGH, D_S to CP	Waveform 3	35		ns
$t_s(L)$ Set-up time LOW, D_S to CP	Waveform 3	25		ns
t_h Hold time HIGH or LOW, D_S to CP	Waveform 3	0		ns

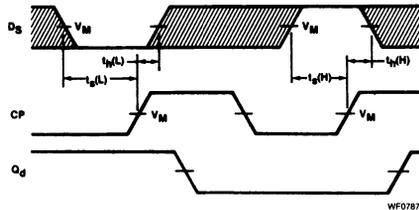
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Parallel Load And Parallel Data To Output Delays And Master Reset To Output Delay



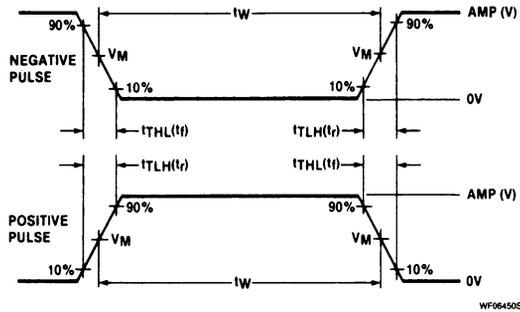
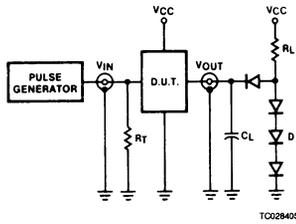
For all waveforms, $V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Serial Data Set-up And Hold Times

Shift Register

7494

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7495, LS95B Shift Registers

4-Bit Shift Register Product Specification

Logic Products

FEATURES

- Separate negative-edge-triggered shift and parallel load clocks
- Common mode control input
- Shift right serial input
- Synchronous shift or load capabilities

DESCRIPTION

The '95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has Serial Data (D_S) and four Parallel Data ($D_0 - D_3$) inputs and four Parallel outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a Mode Select input (S) and two Clock inputs (\overline{CP}_1 and \overline{CP}_2). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected Clock input.

When the Mode Select input (S) is HIGH, \overline{CP}_2 is enabled. A HIGH-to-LOW transition on enabled \overline{CP}_2 loads parallel data from the $D_0 - D_3$ inputs into the register. When S is LOW, \overline{CP}_1 is enabled. A HIGH-to-LOW transition on enabled \overline{CP}_1 shifts the data from Serial input D_S to Q_0 and transfers the data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7495	36MHz	39mA
74LS95B	36MHz	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7495N, N74LS95BN

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
S	Input	2ul	1LSul
Other	Inputs	1ul	1LSul
Q	Output	10ul	10LSul

NOTE:

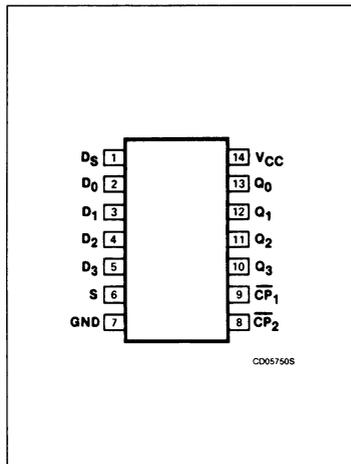
Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

respectively (shift right). Shift left is accomplished by externally connecting Q_3 to D_2 , Q_2 to D_1 , Q_1 to D_0 , and operating the '95 in the parallel mode (S = HIGH).

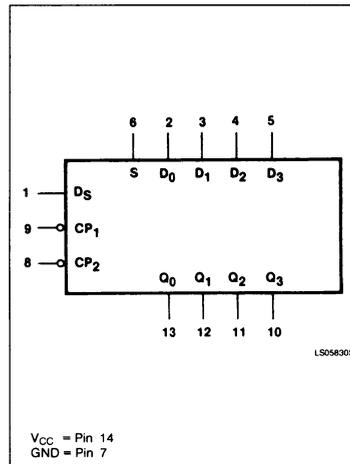
In normal operations the Mode Select (S) should change states only when both

Clock inputs are LOW. However, changing S from HIGH-to-LOW while \overline{CP}_2 is LOW, or changing S from LOW-to-HIGH while \overline{CP}_1 is LOW will not cause any changes on the register outputs.

PIN CONFIGURATION

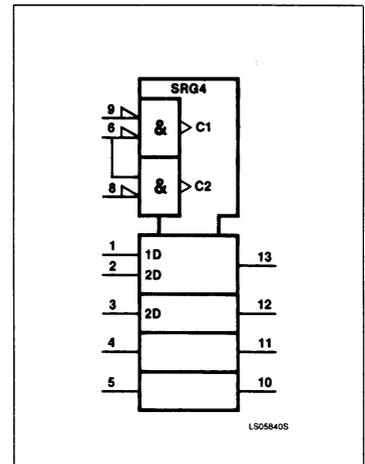


LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

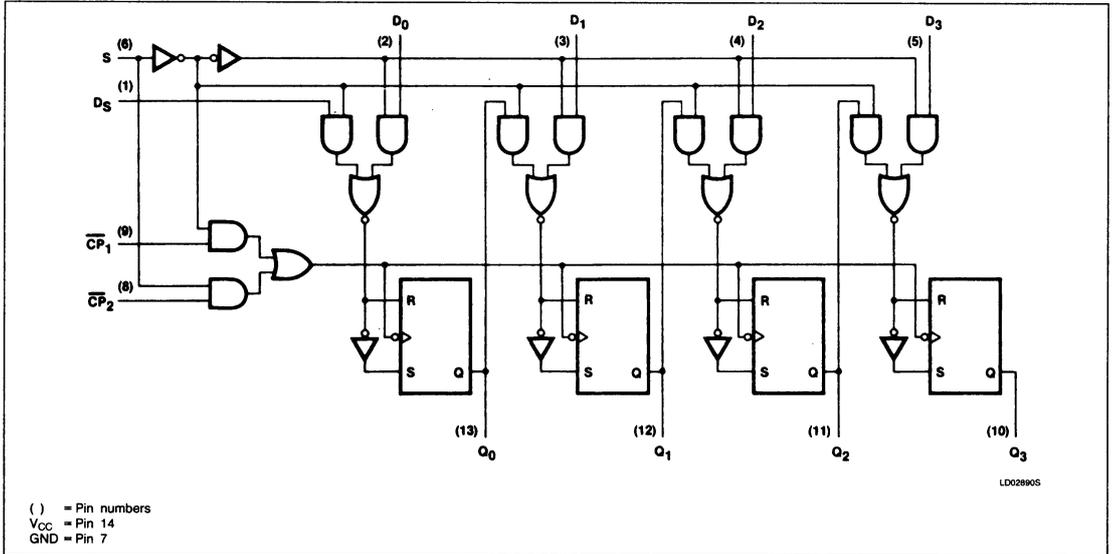
LOGIC SYMBOL (IEEE/IEC)



Shift Registers

7495, LS95B

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	CP ₁	CP ₂	D _S	D _N	Q ₀	Q ₁	Q ₂	Q ₃
Parallel load	H	X	↓	X	l	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	X	l	X	L	q ₀	q ₁	q ₂
	L	↓	X	h	X	H	q ₀	q ₁	q ₂
Mode change	↑	L	X	X	X	no change undetermined no change undetermined			
	↑	H	X	X	X				
	↓	X	L	X	X				
	↓	X	H	X	X				

H = HIGH voltage level steady state.

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition.

L = LOW voltage level steady state.

l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition.

q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW clock transition.

X = Don't care.

↓ = HIGH-to-LOW transition of clock or mode select.

↑ = LOW-to-HIGH transition of mode select.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	+0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

Shift Registers

7495, LS95B

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7495			74LS95B			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.2	0.4		0.35	0.5	V	
		I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0				mA	
		V _I = 7.0V					0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	S input		80			μA	
			Other inputs		40			μA	
		V _I = 2.7V	S input					20	μA
			Other inputs					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX V _I = 0.4V	S input		-3.2			-0.4	mA	
		Other inputs		-1.6			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18	-57	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		39	63		13	21	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Serial Data input and all outputs open; Parallel Data inputs grounded; Mode Select input at 4.5V and a momentary 3V, then ground, applied to the Clock inputs.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		25		MHz
t _{PLH} Propagation delay	Waveform 1		27		27	ns
t _{PHL} Clock to output			32		32	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

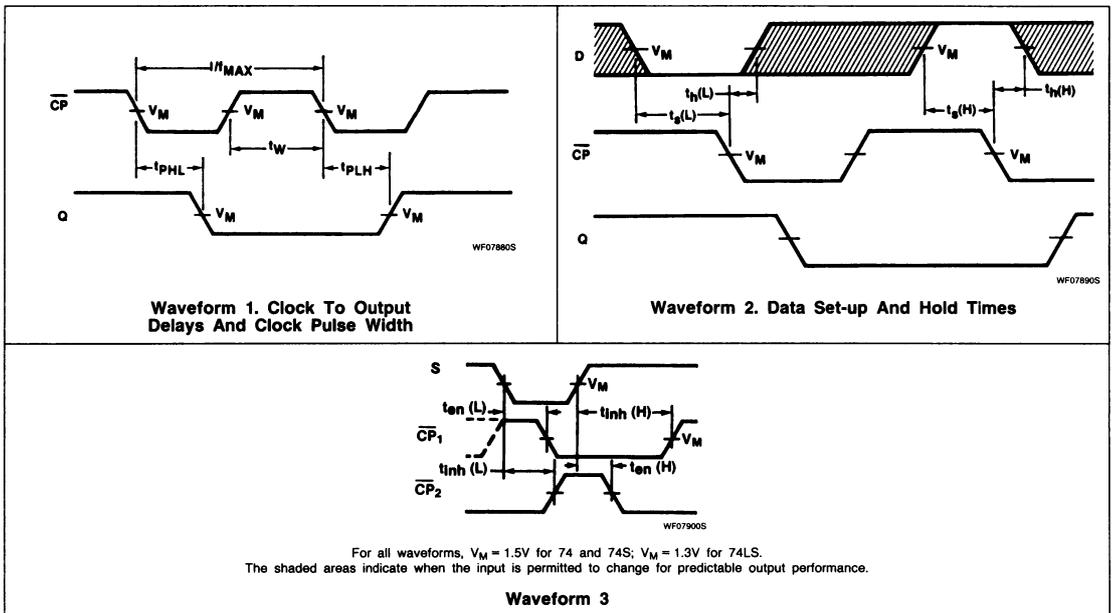
Shift Registers

7495, LS95B

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$	Clock pulse width, HIGH	Waveform 1	20		25	ns
t_s	Set-up time, data to clock	Waveform 2	15		20	ns
t_h	Hold time, data to clock	Waveform 2	0		10	ns
$t_{en(L)}$	Enable time, LOW mode Select to \overline{CP}_1	Waveform 3	30		20	ns
$t_{en(H)}$	Enable time, HIGH mode Select to \overline{CP}_2	Waveform 3	30		20	ns
$t_{inh(H)}$	Inhibit time, HIGH mode Select to \overline{CP}_1 (L \rightarrow H)	Waveform 3	5		20	ns
$t_{inh(L)}$	Inhibit time, LOW Mode Select to \overline{CP}_2 (L \rightarrow H)	Waveform 3	5		20	ns

AC WAVEFORMS

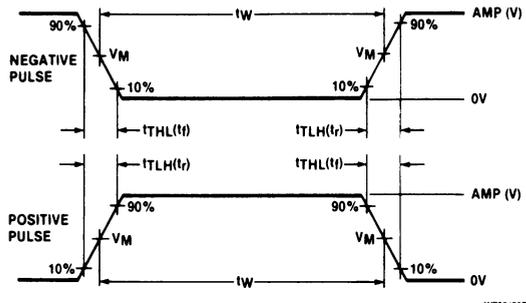
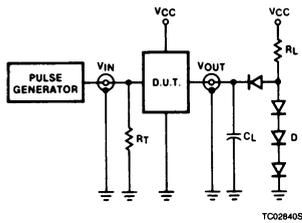


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Shift Registers

7495, LS95B

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

7496, LS96 Shift Registers

5-Bit Shift Register
Product Specification

Logic Products

FEATURES

- 5-bit parallel-to-serial or serial-to-parallel converter
- Asynchronous ones transfer preset entry
- Buffered positive-triggered clock
- Buffered active LOW Clear (Master Reset)

DESCRIPTION

The '96 is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Since the '96 has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The '96 is five master/slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The Serial (S) input is edge-triggered and must be stable only one set-up time before the LOW-to-HIGH clock transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7496	25ns	48mA
74LS96	25ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7496N, N74LS96N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

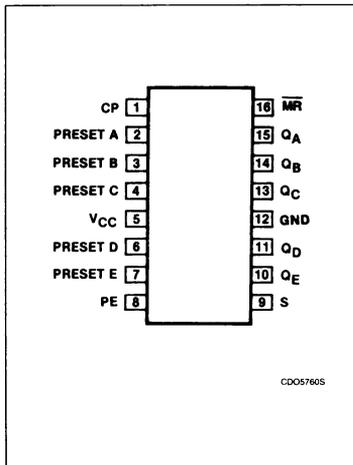
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
Preset enable	Inputs	5ul	5LSul
All other	Inputs	1ul	1LSul
Q	Outputs	10ul	10LSul

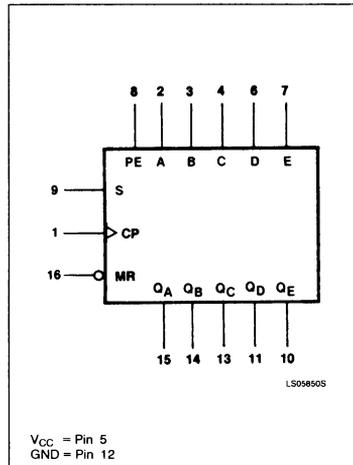
NOTE:

A 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

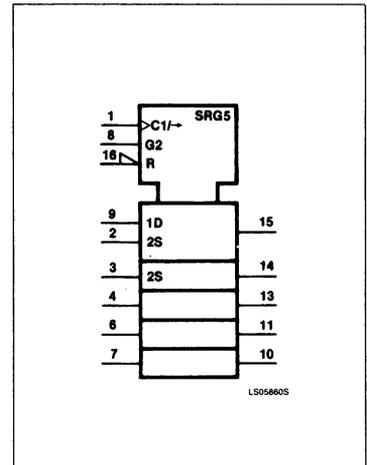
PIN CONFIGURATION



LOGIC SYMBOL



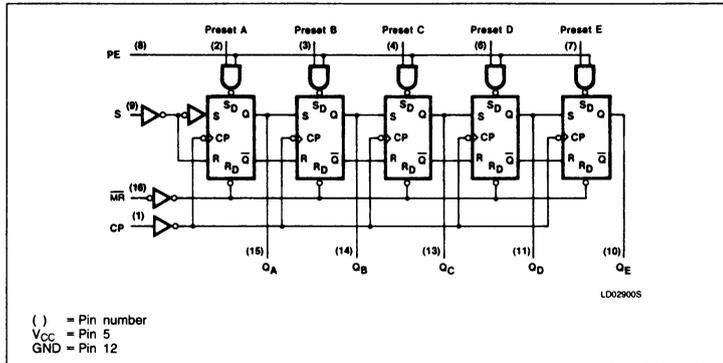
LOGIC SYMBOL (IEEE/IEC)



Shift Registers

7496, LS96

LOGIC DIAGRAM



Each flip-flop has asynchronous set inputs, allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH Preset Enable (PE) input. The PE input is not buffered, and care must be taken not to overload the driving element. When the PE is HIGH, a HIGH on the Preset (A-E) inputs will set the associated flip-flops HIGH. A LOW on the A-E inputs will cause "no change" in the appropriate flip-flops.

The asynchronous active LOW Clear (\overline{MR}) is buffered. When LOW, the \overline{MR} overrides the clock and clears the register if the PE is not active. The Preset inputs override the \overline{MR} , forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

FUNCTION TABLE

Master Reset	Preset Enable	INPUTS					Clock	Serial	OUTPUTS				
		Preset							Q _A	Q _B	Q _C	Q _D	Q _E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	L	L	L	L	L	L
L	X	L	L	L	L	L	X	L	L	L	L	L	L
H	H	H	H	H	H	H	X	H	H	H	H	H	H
H	H	L	L	L	L	L	X	H	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	H
H	H	L	L	L	L	H	L	H	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	H
H	L	X	X	X	X	X	L	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	H
H	L	X	X	X	X	X	↑	Q _{A0}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{E0}	H
H	L	X	X	X	X	X	↑	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	H

H = HIGH voltage level, (steady state)
 L = LOW voltage level, (steady state)
 X = Irrelevant (any input, including transitions)
 ↑ = Transition from LOW-to-HIGH level
 Q_{A0}, Q_{B0}, etc = The level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
 Q_{An}, Q_{Bn}, etc = The level of Q_A, Q_B, etc, respectively before the most recent ↑ transition of the clock.

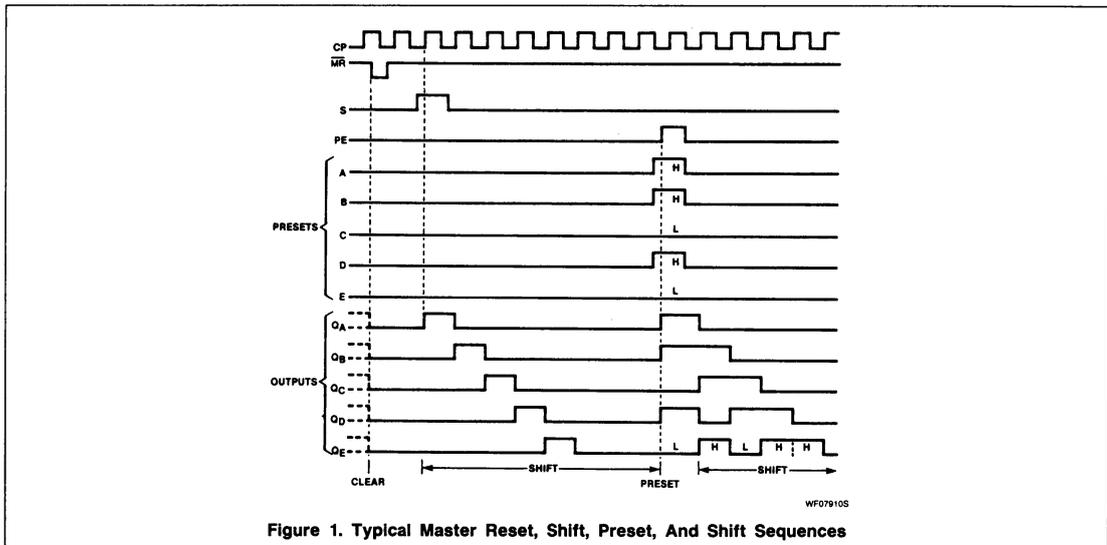


Figure 1. Typical Master Reset, Shift, Preset, And Shift Sequences

Shift Registers

7496, LS96

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-400			-400	μA
I _{OL}	LOW-level output current			16			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7496			74LS96			UNIT			
		Min	Typ ²	Max	Min	Typ ²	Max				
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4	V		
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		I _{OL} = MAX		0.2	0.4	0.35	0.5	V	
				I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.5	V		
I _I	Input current at maximum input voltage	V _{CC} = MAX		V _I = 5.5V			1.0		mA		
				V _I = 7.0V		PE inputs			0.5	mA	
						Other inputs			0.1	mA	
I _{IH}	HIGH-level input current	V _{CC} = MAX		V _I = 2.4V		PE inputs			200	μA	
						Other inputs			40	μA	
				V _I = 2.7V		PE inputs				100	μA
						Other inputs				20	μA
I _{IL}	LOW-level input current	V _{CC} = MAX		V _I = 0.4V		PE inputs			-8	mA	
						Other inputs			-1.6	mA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-18		-57	-20		-100	mA	
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			48	79		12	20	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Clear grounded and all other inputs and outputs open.

Shift Registers

7496, LS96

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	10		25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		40		40	ns
t_{PLH} Propagation delay Preset or preset enable to output	Waveform 2		35		35	ns
t_{PHL} Propagation delay \overline{MR} to output	Waveform 2		55		55	ns

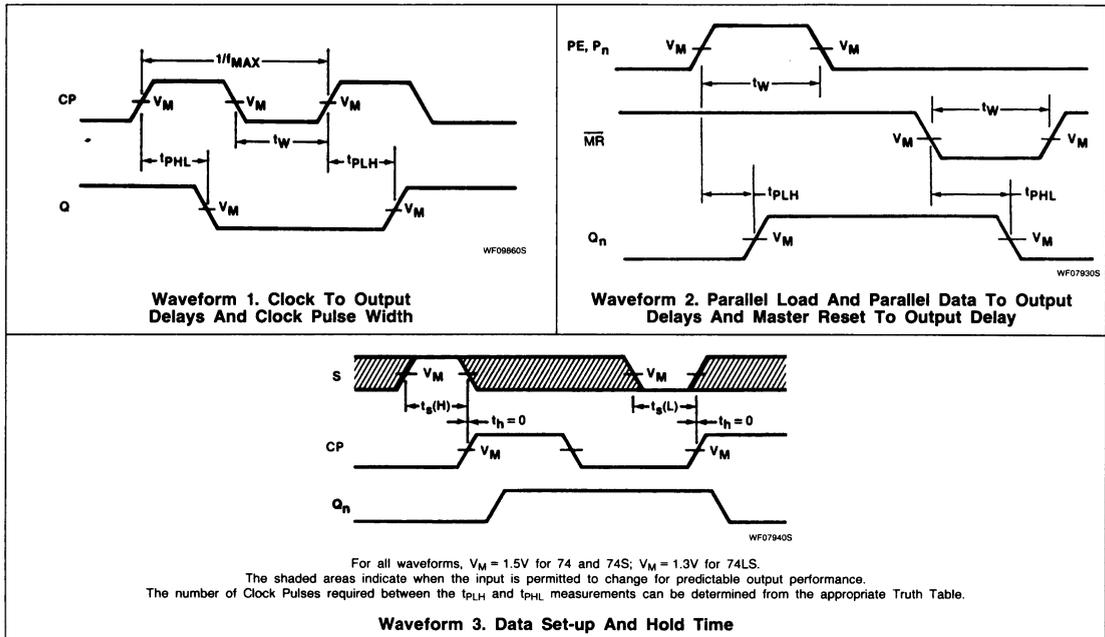
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width, LOW	Waveform 1	35		20		ns
$t_{W(L)}$ \overline{MR} pulse width, LOW	Waveform 2	30		30		ns
$t_{W(H)}$ Preset or preset enable pulse width, HIGH	Waveform 2	30		30		ns
t_s Set-up time, S to CP	Waveform 3	30		30		ns
t_h Hold time, S to CP	Waveform 3	0		0		ns

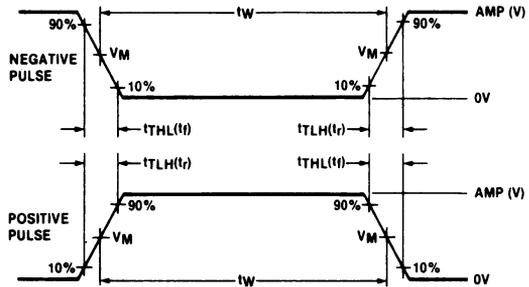
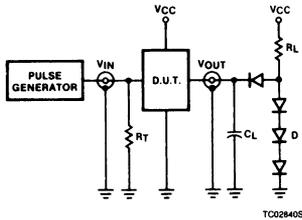
AC WAVEFORMS



Shift Registers

7496, LS96

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74107, LS107 Flip-Flops

Dual J-K Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The '107 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 74107 is a positive pulse-triggered flip-flop. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. For these devices the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS107 is a negative edge-triggered flip-flop. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the \bar{Q} output HIGH.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74107	20MHz	20mA
74LS107	45MHz	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74107N, N74LS107N
Plastic SO	N74LS107D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Manual.

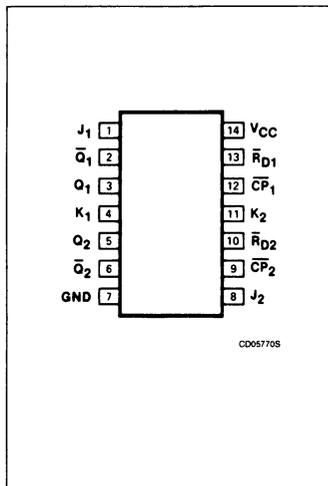
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
\bar{CP}	Clock input	2ul	4LSul
\bar{R}_D	Reset input	2ul	3LSul
J, K	Data inputs	1ul	1LSul
Q, \bar{Q}	Outputs	10ul	10LSul

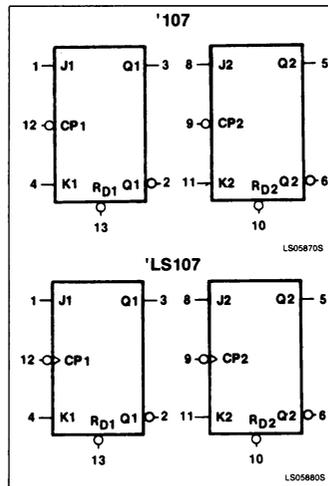
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

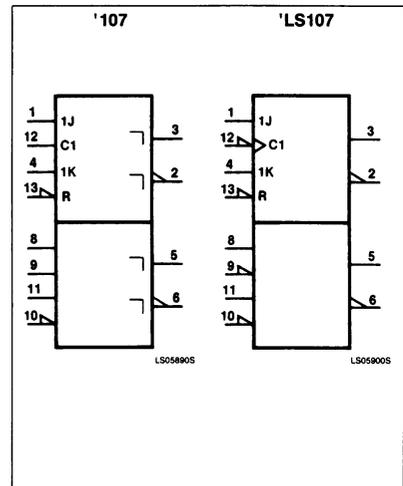
PIN CONFIGURATION



LOGIC SYMBOL



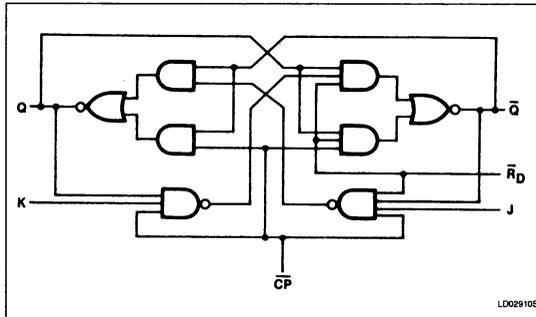
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74107, LS107

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{R}_D	$\overline{CP}^{(2)}$	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	\bar{L}	H
Toggle	H	\downarrow	h	h	\bar{q}	q
Load "0" (Reset)	H	\downarrow	l	h	L	H
Load "1" (Set)	H	\downarrow	h	l	H	L
Hold "no change"	H	\downarrow	l	l	q	\bar{q}

- H = HIGH voltage level steady state.
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.⁽²⁾
- L = LOW voltage level steady state.
- l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.⁽²⁾
- q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
- X = Don't care.
- \downarrow = Positive Clock pulse.

NOTES:

1. The J and K inputs of the 74107 must be stable while the Clock is HIGH for conventional operation.
2. The 74LS107 is edge-triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8	V
I_{IK} Input clamp current			-12			-18	mA
I_{OH} HIGH-level output current			-400			-400	μ A
I_{OL} LOW-level output current			16			8	mA
T_A Operating free-air temperature	0		70	0		70	°C

Flip-Flops

74107, LS107

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74107			74LS107			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V	
		I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	J, K Inputs					0.1	mA
			\overline{R}_D Inputs					0.3	mA
			$\overline{C}\overline{P}$ Inputs					0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, K Inputs			40		μ A	
			\overline{R}_D Inputs			80		μ A	
			$\overline{C}\overline{P}$ Inputs			80		μ A	
		V _I = 2.7V	J, K Inputs					20	μ A
			\overline{R}_D Inputs					60	μ A
			$\overline{C}\overline{P}$ Inputs					80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	J, K Inputs			-1.6		-0.4	mA	
		\overline{R}_D Inputs			-3.2		-0.8	mA	
		$\overline{C}\overline{P}$ Inputs			-3.2		-0.8	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			40			8	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 3	15		30		MHz
t _{PLH} Propagation delay	Waveform 1, 'LS107 Waveform 3, '107		25		20	ns
t _{PHL} Clock to output			40		30	
t _{PLH} Propagation delay	Waveform 2		25		20	ns
t _{PHL} Reset to output			40		30	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

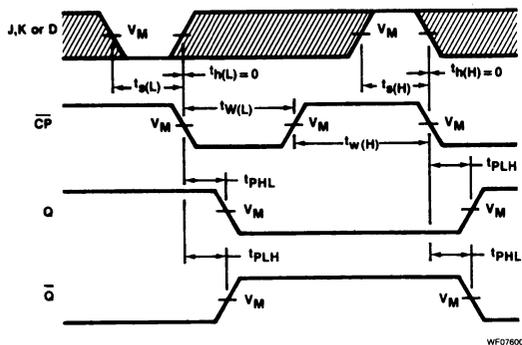
Flip-Flops

74107, LS107

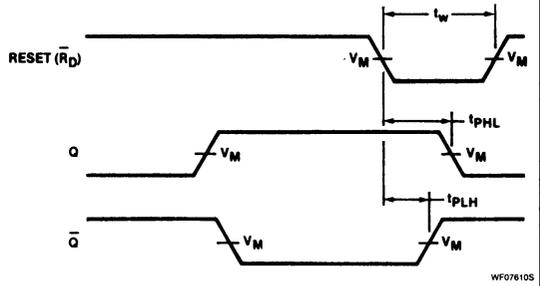
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 1	47		13		ns
$t_{w(L)}$ Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s Setup time J or K to clock ^(b)	Waveform 1	0		20		ns
t_h Hold time J or K to clock	Waveform 1	0		0		ns

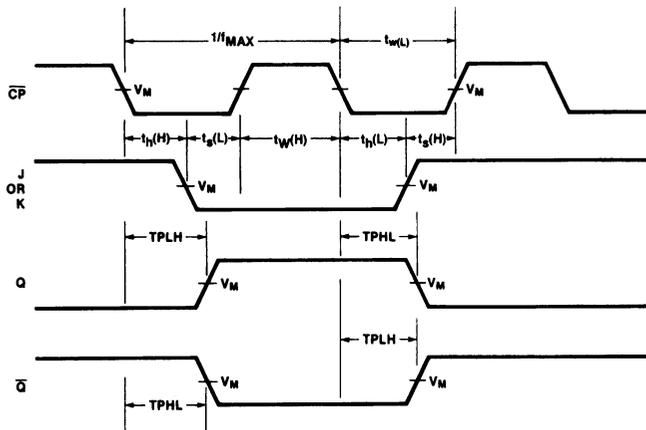
AC WAVEFORMS



Waveform 1. Clock To Output Delays, Data Set-up And Hold Times, Clock Pulse Width



Waveform 2. Reset To Output Delays, Reset Pulse Widths



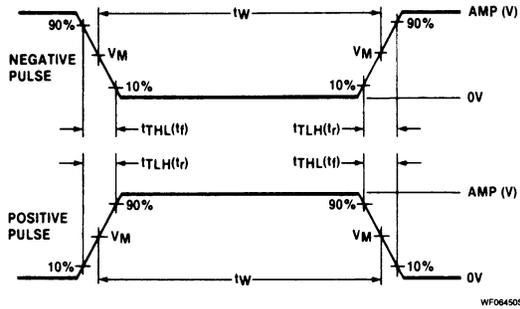
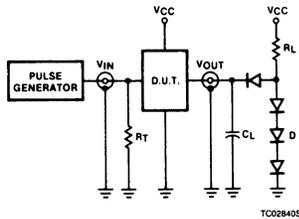
For all waveforms, $V_M = 1.3\text{V}$ for 74S; $V_M = 1.5\text{V}$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Propagation Delay And f_{MAX}

Flip-Flops

74107, LS107

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74109, LS109A Flip-Flops

Dual J-K̄ Positive Edge-Triggered Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The '109 is dual positive edge-triggered JK̄-type flip-flop featuring individual J, K̄, Clock, Set and Reset inputs; also complementary Q and Q̄ outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs and operate independently of the Clock input.

The J and K̄ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and K̄ inputs must be stable just one set-up time prior to the LOW-to-HIGH transition of the Clock for predictable operation. The JK̄ design allows operation as a D flip-flop by tying the J and K̄ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74109	33MHz	9mA
74LS109A	33MHz	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74109N, N74LS109AN
Plastic SO	N74LS109D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

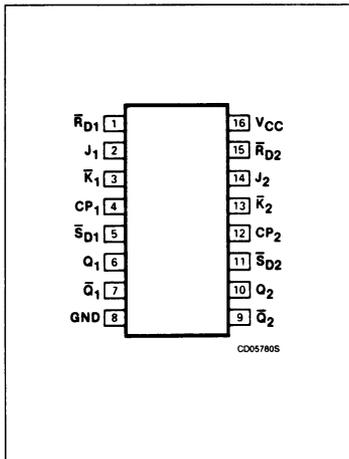
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
CP	Clock input	2ul	1LSul
\bar{R}_D	Reset input	4ul	2LSul
\bar{S}_D	Set input	2ul	2LSul
J, K̄	Data inputs	1ul	1LSul
Q, Q̄	Outputs	10ul	10LSul

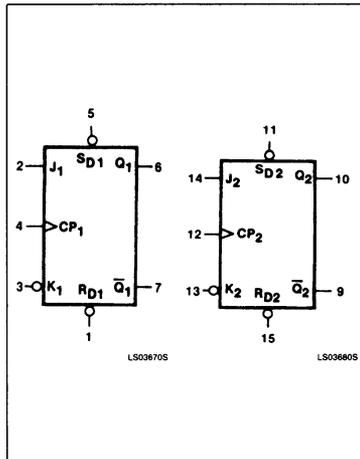
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

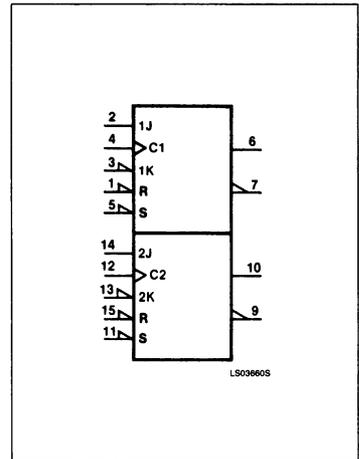
PIN CONFIGURATION



LOGIC SYMBOL



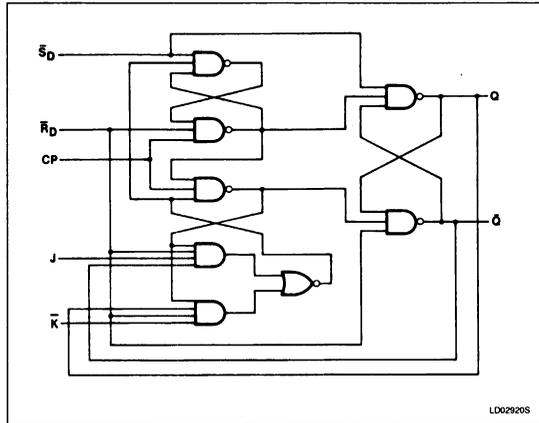
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74109, LS109A

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	J	\bar{K}	Q	\bar{Q}
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined (note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	\bar{q}	q
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition.
 ↑ = LOW-to-HIGH Clock transition.

NOTE:
 Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

Flip-Flops

74109, LS109A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74109			74LS109			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA
		V _I = 7.0V	J, \bar{K} inputs					0.1	mA
			\bar{R}_D , \bar{S}_D inputs					0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, \bar{K} inputs		40				μ A
			\bar{R}_D inputs		160				μ A
			\bar{S}_D , CP inputs		80				μ A
		V _I = 2.7V	J, \bar{K} inputs					20	μ A
			\bar{R}_D , \bar{S}_D inputs					40	μ A
			CP inputs					20	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	J, \bar{K} inputs		-1.6				-0.4	mA
		\bar{R}_D inputs		-4.8				-0.8	mA
		\bar{S}_D inputs		-3.2				-0.8	mA
		CP inputs		-3.2				-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-30		-85	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			9	30		4	8	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		25		MHz
t _{PLH} Propagation delay	Waveform 1		16		25	ns
t _{PHL} Clock to output			28		40	
t _{PLH} Propagation delay	Waveform 2		15		25	ns
t _{PHL} Reset to output			25		40	
t _{PLH} Propagation delay	Waveform 2		15		25	ns
t _{PHL} Set to output			35		40	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

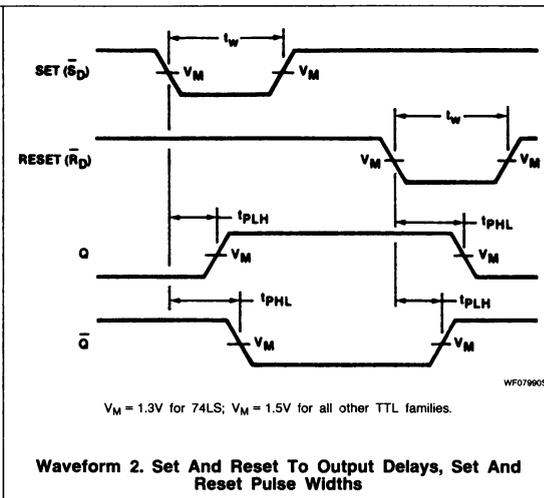
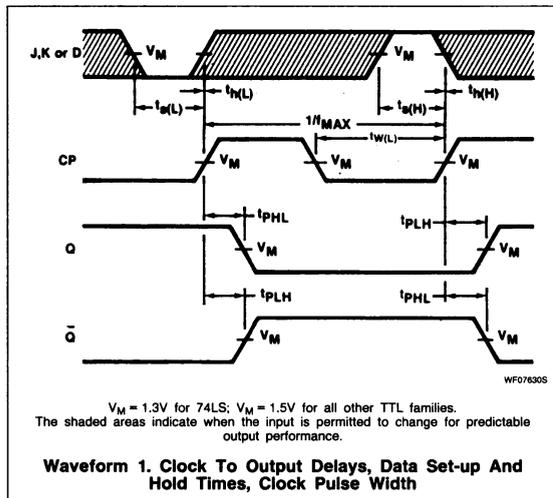
Flip-Flops

74109, LS109A

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 1	20		25		ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 1	20		15		ns
$t_{w(L)}$ Set or reset pulse width (LOW)	Waveform 2	20		25		ns
t_s Set-up time J or K to clock	Waveform 1	10		20		ns
t_h Hold time J or K to clock	Waveform 1	6.0		5.0		ns

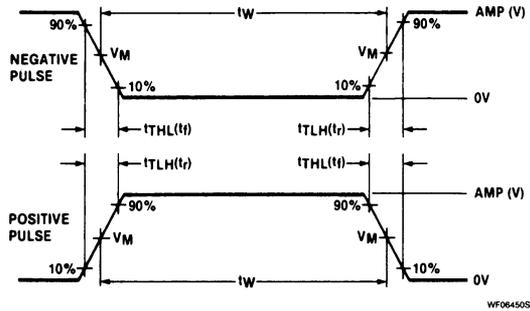
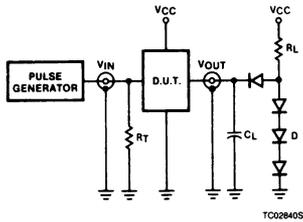
AC WAVEFORMS



Flip-Flops

74109, LS109A

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS112, S112 Flip-Flops

Dual J-K Edge-Triggered Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The '112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\bar{C}\bar{P}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\bar{C}\bar{P}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\bar{C}\bar{P}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS112	45MHz	4mA
74S112	125MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S112N, N74LS112N
Plastic SO	N74LS112D, N74S112D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

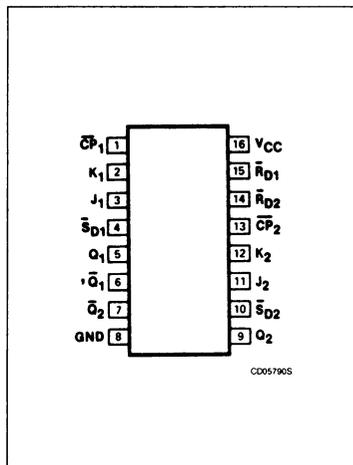
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
$\bar{C}\bar{P}$	Clock input	2Sul	4LSul
\bar{R}_D, \bar{S}_D	Reset and set inputs	3.5Sul	3LSul
J, K	Data inputs	1Sul	1LSul
Q, \bar{Q}	Outputs	10Sul	10LSul

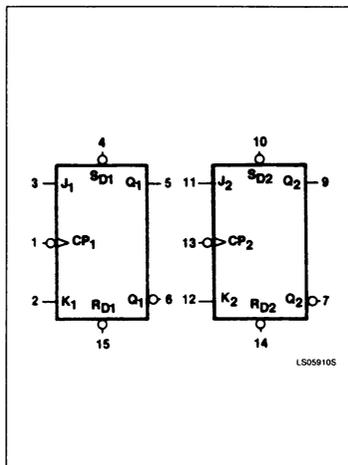
NOTE:

A 74 unit load (ul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

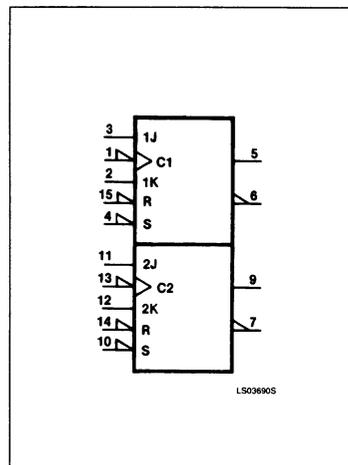
PIN CONFIGURATION



LOGIC SYMBOL



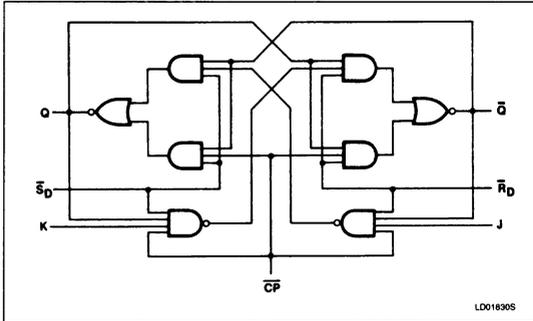
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74LS112, S112

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	$\bar{C}\bar{P}$	J	K	Q	\bar{Q}
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	\bar{q}	q
Load "0" (reset)	H	H	↓	l	h	L	H
Load "1" (set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 ↓ = HIGH-to-LOW Clock transition.

NOTE:
 Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to -7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	HIGH-level output current			-400			-1000	μA
I_{OL}	LOW-level output current			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	°C

Flip-Flops

74LS112, S112

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74LS112			74S112			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5			0.5	V
		I _{OL} = 4mA (74LS)		0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA
		V _I = 7.0V	J, K Inputs		0.1				mA
			\bar{R}_D , \bar{S}_D Inputs		0.3				mA
			$\bar{C}\bar{P}$ Inputs		0.4				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	J, K Inputs		20		50	μ A	
			\bar{R}_D , \bar{S}_D Inputs		60		100	μ A	
			$\bar{C}\bar{P}$ Inputs		80		100	μ A	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	J, K Inputs		-0.4			mA	
			\bar{R}_D , \bar{S}_D Inputs		-0.8			mA	
			$\bar{C}\bar{P}$ Inputs		-0.8			mA	
		V _I = 0.5V	J, K Inputs					-1.6	mA
			\bar{R}_D , \bar{S}_D Inputs					-7	mA
			$\bar{C}\bar{P}$ Inputs					-4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			4	8		15	50	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C _L = 15pF, R _L = 2k Ω		C _L = 15pF, R _L = 280 Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	30		80		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		20 30		7.0 7.0	ns
t _{PLH} Propagation delay t _{PHL} \bar{S}_D or \bar{R}_D to output	Waveform 2		20 30		7.0 7.0	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

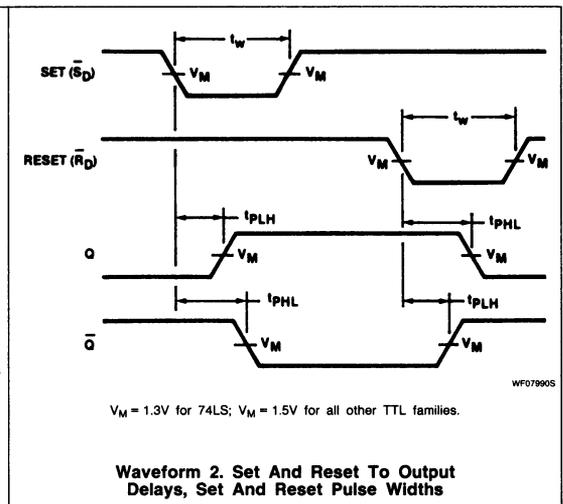
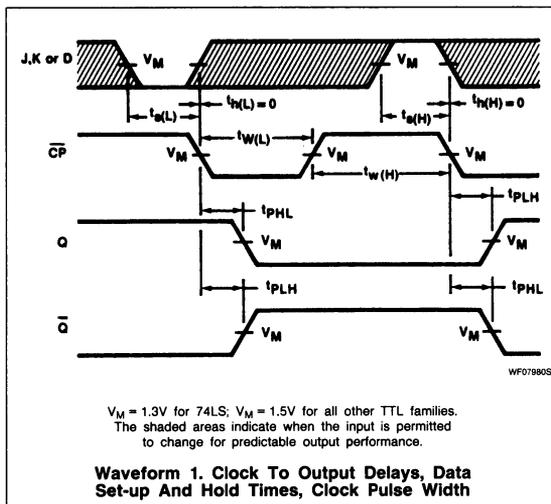
Flip-Flops

74LS112, S112

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	20		6.0		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	13		6.5		ns
$t_{W(L)}$ Set or reset pulse width (LOW)	Waveform 2	25		8.0		ns
t_s Set-up time J or K to clock	Waveform 1	20		3.0		ns
t_h Hold time J or K to clock	Waveform 1	0		0		ns

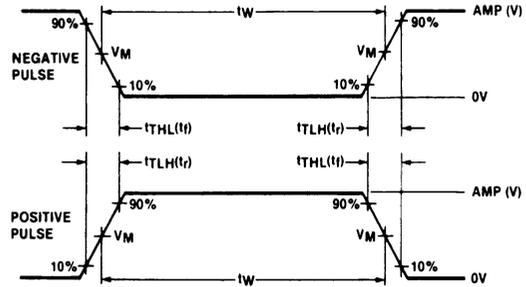
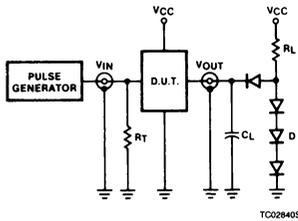
AC WAVEFORMS



Flip-Flops

74LS112, S112

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS113, S113 Flip-Flops

Dual J-K Edge-Triggered Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The '113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set (\bar{S}_D) input, when LOW, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock (\overline{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the \overline{CP} is HIGH and the flip-flop will perform according to the Function Table as long as minimum set-up and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \overline{CP} .

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS113	45MHz	4mA
74S113	125MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S113N, N74LS113N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

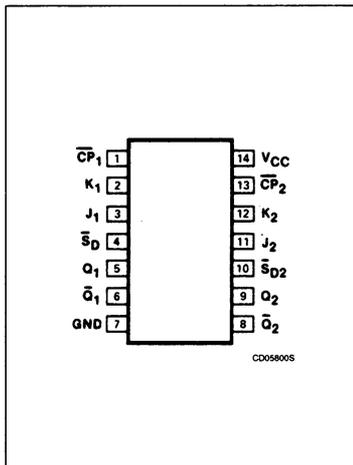
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
\overline{CP}	Clock input	2Sul	4LSul
\bar{S}_D	Set inputs	3.5Sul	3LSul
J, K	Data inputs	1Sul	1LSul
Q, \bar{Q}	Outputs	10Sul	10LSul

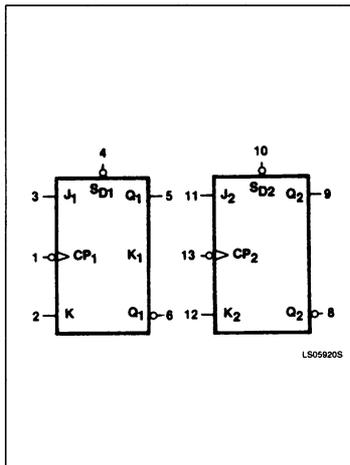
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

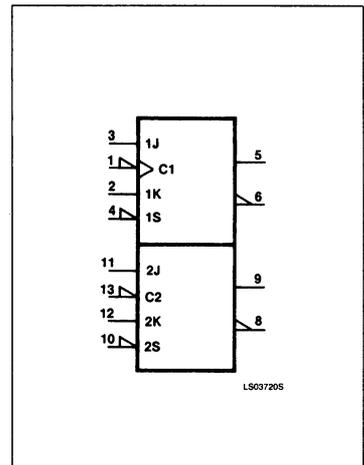
PIN CONFIGURATION



LOGIC SYMBOL



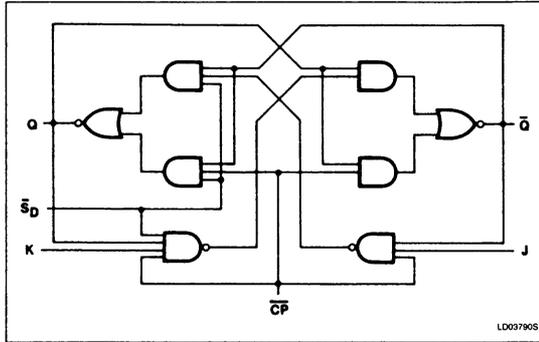
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74LS113, S113

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	$\bar{C}P$	J	K	Q	\bar{Q}
Asynchronous set	L	X	X	X	H	L
Toggle	H	↓	h	h	\bar{q}	q
Load "0" (reset)	H	↓	l	h	L	H
Load "1" (set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 ↓ = HIGH-to-LOW Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to -7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	2.0			2.0			V
V_{IL}			+0.8			+0.8	V
I_{IK}			-18			-18	mA
I_{OH}			-400			-1000	μA
I_{OL}			8			20	mA
T_A	0		70	0		70	°C

Flip-Flops

74LS113, S113

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS113			74S113			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5		0.5	V	
		I _{OL} = 4mA (74LS)		0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA	
		V _I = 7.0V	J, K Inputs		0.1				mA
			\bar{S}_D Inputs		0.3				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	$\bar{C}P$ Inputs		0.4				mA
			J, K Inputs		20			50	μ A
			\bar{S}_D Inputs		60			100	μ A
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	$\bar{C}P$ Inputs		80			100	μ A
			J, K Inputs		-0.4				mA
			\bar{S}_D Inputs		-0.8				mA
		V _I = 0.5V	CP Inputs		-0.8				mA
			J, K Inputs					-1.6	mA
			\bar{S}_D Inputs					-7	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		4	8		15	50	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C _L = 15pF, R _L = 2k Ω		C _L = 15pF, R _L = 280 Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	30		80		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		20 30		7.0 7.0	ns
t _{PLH} Propagation delay t _{PHL} Set to output	Waveform 2		20 30		7.0 7.0	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

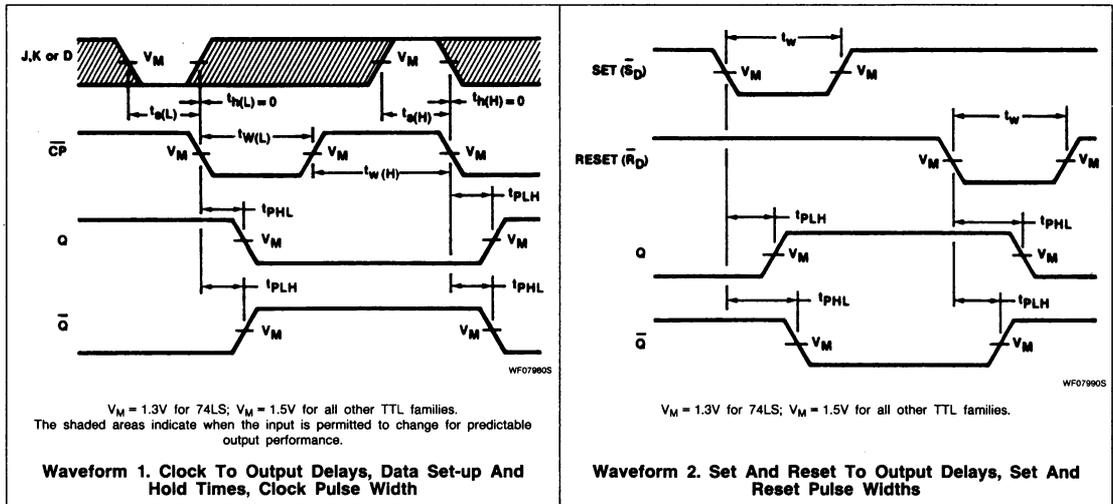
Flip-Flops

74LS113, S113

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	20		6.0		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	13		6.5		ns
$t_{W(L)}$ Set pulse width (LOW)	Waveform 2	25		8.0		ns
t_s Set-up time J or K to clock	Waveform 1	20		3.0		ns
t_h Hold time J or K to clock	Waveform 1	0		0		ns

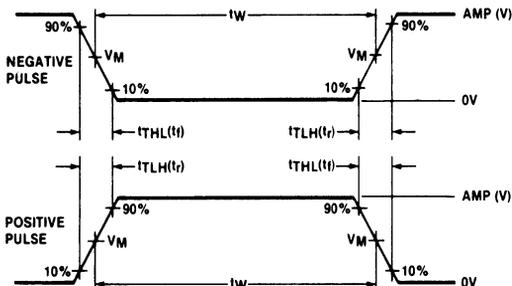
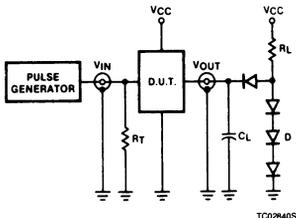
AC WAVEFORMS



Flip-Flops

74LS113, S113

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74116 Latch

Dual 4-Bit Transparent Latch
Product Specification

Logic Products

DESCRIPTION

The '116 has two independent 4-bit transparent latches. Each 4-bit latch is controlled by a two-input active LOW Enable gate (\bar{E}_0 and \bar{E}_1). When both \bar{E}_0 and \bar{E}_1 are LOW, the data enters the latch and appears at the output. The outputs follow the Data inputs as long as \bar{E}_0 and \bar{E}_1 are LOW. The data on the D inputs one set-up time before the LOW-to-HIGH transition of \bar{E}_0 or \bar{E}_1 will be stored in the latch. The Latched outputs remain stable as long as either \bar{E}_0 or \bar{E}_1 is HIGH.

Each 4-bit latch has an active LOW asynchronous Master Reset (\bar{MR}) input. When LOW, the \bar{MR} input overrides the Data and Enable inputs and sets the four Latch outputs LOW.

TYPE	TYPICAL PROPAGATION DELAY—DATA TO OUTPUT	TYPICAL SUPPLY CURRENT (TOTAL)
74116	11ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74116N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

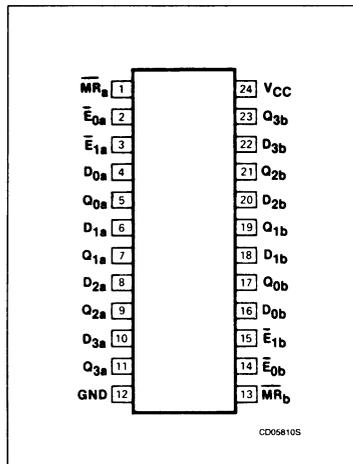
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
\bar{E}_0, \bar{E}_1	Enable inputs	1ul
$D_0 - D_3$	Data inputs	1.5ul
\bar{MR}	Master reset input	1ul
$Q_0 - Q_3$	Latch outputs	10ul

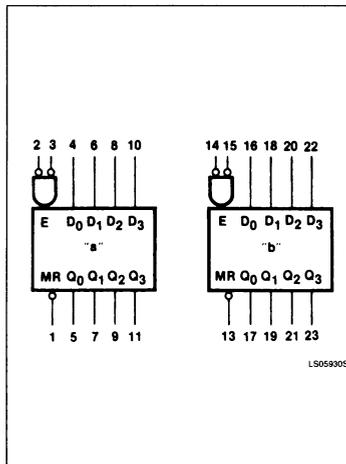
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

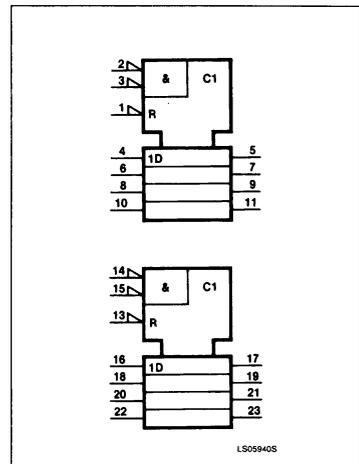
PIN CONFIGURATION



LOGIC SYMBOL



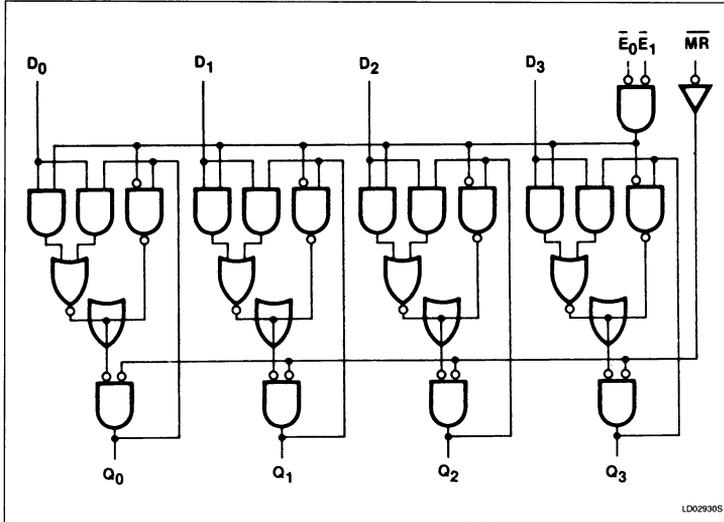
LOGIC SYMBOL (IEEE/IEC)



Latch

74116

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUT
	MR	\bar{E}_0	\bar{E}_1	D_n	Q_n	
Reset (clear)	L	X	X	X	L	L
Enable latch	H	L	L	L	H	H
Latch data	H	H	L	L	↑	L
	H	H	L	L	↑	h
	H	H	L	L	↑	H

H = HIGH voltage level.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Enable transition.
 L = LOW voltage level.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH Enable transition.
 X = Don't care.
 ↑ = LOW-to-HIGH Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to +15	V
T_A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			V
V_{IL} LOW-level input voltage			+0.8	V
I_{IK} Input clamp current			-12	mA
I_{OH} HIGH-level output current			-800	μA
I_{OL} LOW-level output current			16	mA
T_A Operating free-air temperature	0		70	°C

5

Latch

74116

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74116			UNIT
			Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V				1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	E, MR inputs			40	μA
		D inputs			60	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	E, MR inputs			-1.6	mA
		D inputs, initial peak			-2.4	mA
		D inputs, steady-state			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-57	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		60	100	mA
		Condition 2		40	70	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC}MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Condition 1. Measure I_{CC} with all inputs grounded and all outputs open. Condition 2. Measure I_{CC} with E inputs grounded, all other inputs at 4.5V and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} Propagation delay t _{PHL} Enable to output	Waveform 1		30 22	ns
t _{PLH} Propagation delay t _{PHL} Data to output	Waveform 2		15 18	ns
t _{PHL} Propagation delay MR to output	Waveform 3		22	ns

Latch

74116

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t_W Enable pulse width	Waveform 1	18		ns
t_W Master reset pulse width	Waveform 3	18		ns
$t_s(H)$ Set-up time HIGH data to enable	Waveform 4	8.0		ns
$t_h(H)$ Hold time HIGH data to enable	Waveform 4		-2.0	ns
$t_s(L)$ Set-up time LOW data to enable	Waveform 4	14.0		ns
$t_h(L)$ Hold time LOW data to enable	Waveform 4	8.0		ns
$t_h(L)$ Hold time LOW enable to master reset to load HIGH	Waveform 3	8.0		ns

AC WAVEFORMS

WF08040S

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.

Waveform 1. Propagation Delay Enable to Output and Enable Pulse Width

WF08050S

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.5\text{V}$ for 74LS.

Waveform 2. Propagation Delay Data To Output

WF08060S

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.

Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay and Low Enable To Master Reset Hold Time

WF11530S

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.5\text{V}$ for 74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

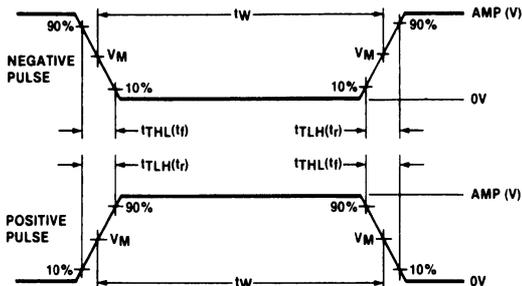
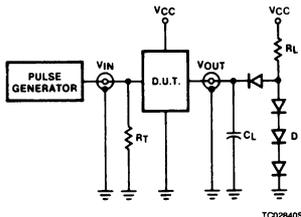
Waveform 4. Data Set-up And Hold Times

5

Latch

74116

TEST CIRCUITS AND WAVEFORMS



WF064505

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74121 Multivibrator

Monostable Multivibrator
Product Specification

Logic Products

FEATURES

- Very good pulse width stability
- Virtually immune to temperature and voltage variations
- Schmitt trigger input for slow input transitions
- Internal timing resistor provided

DESCRIPTION

These multivibrators feature dual active LOW going edge inputs and a single active HIGH going edge input which can be used as an active HIGH enable input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the inputs and are a function only of the

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74121	43ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74121 N
Plastic SO	N74121 D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 20 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC} , C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually

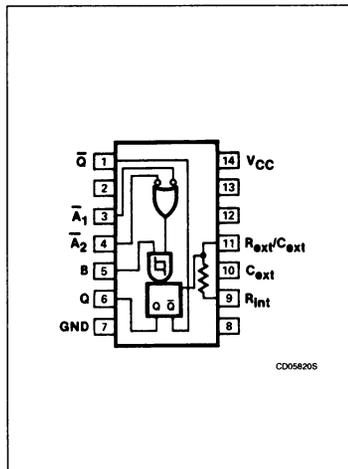
independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10 μ F) and more than one decade of timing resistance (2k Ω to 30k Ω for the 54121 and 2K Ω to 40k Ω for the 74121). Throughout these ranges, pulse width is defined by the relationship: (see Figure 1)

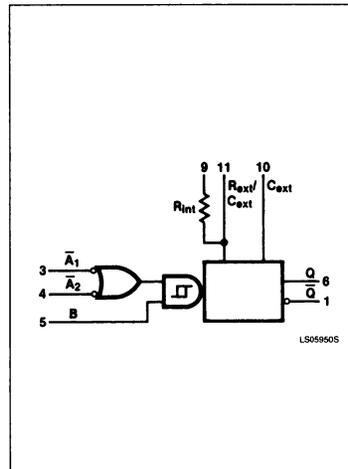
$$t_W(\text{out}) = C_{ext} R_{ext} \ln 2$$

$$t_W(\text{out}) \cong 0.7 C_{ext} R_{ext}$$

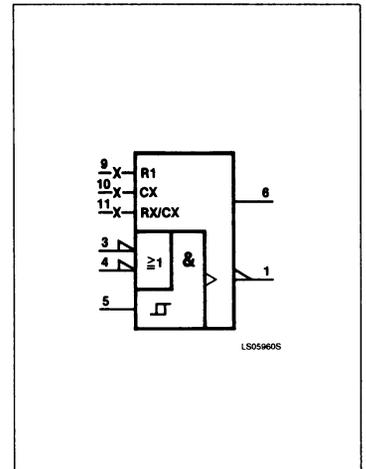
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Multivibrator

74121

FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{A}_1	\bar{A}_2	B	Q	\bar{Q}
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H		
↓	H	H		
↓	↓	H		
L	X	↑		
X	L	↑		

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH transition
 ↓ = HIGH-to-LOW transition

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
\bar{A}_1, \bar{A}_2	Inputs	1ul
B	Input	2ul
Q, \bar{Q}	Outputs	10ul

NOTE:
 A 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

In circuits where pulse cutoff is not critical, timing capacitance up to $1000\mu F$ and timing resistance as low as $1.4k\Omega$ may be used.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	V
T_A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	V
I_{IK} Input clamp current			-12	mA
I_{OH} HIGH-level output current			-400	μA
I_{OL} LOW-level output current			16	mA
dv/dt Rate of rise or fall of input pulse	B input	1		V/s
	\bar{A}_1, \bar{A}_2 inputs	1		V/ μs
T_A Operating free-air temperature	0		70	°C

Multivibrator

74121

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74121			UNIT
		Min	Typ ²	Max	
V _{T+}	Positive-going threshold at \bar{A} and B	V _{CC} = MIN			V
V _{T-}	Negative-going threshold at \bar{A} and B	V _{CC} = MIN			V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX			V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40
		\bar{A}_1, \bar{A}_2 inputs			μ A
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V			80
		B input			μ A
I _{OS}	Short-circuit output current ³	V _{CC} = MAX			-1.6
					mA
I _{CC}	Supply current (total)	V _{CC} = MAX			-18
		Quiescent			13
		Triggered			25
					40
					mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} t _{PHL}	Waveform 1 \bar{A} input to Q & \bar{Q} output C _{ext} = 80pF, R _{int} to V _{CC}	70 80		ns
t _{PLH} t _{PHL}	Waveform 2 B input to Q & \bar{Q} output C _{ext} = 80pF, R _{int} to V _{CC}	55 65		ns
t _w	Minimum output pulse width C _{ext} = 0pF, R _{int} to V _{CC}	20	50	ns
t _w	C _{ext} = 80pF, R _{int} to V _{CC}	70	150	ns
	C _{ext} = 100pF, R _{ext} = 10kΩ	600	800	ns
	C _{ext} = 1μF, R _{ext} = 10kΩ	6.0	8.0	ms

Multivibrator

74121

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t_W	Minimum input pulse width to trigger	50		ns
R_{ext}	External timing resistor range	1.4	40	$k\Omega$
C_{ext}	External timing capacitance range	0	1000	μF
Output duty cycle	$R_{ext} = 2k\Omega$		67	%
	$R_{ext} = R_{ext}(\text{Max})$		90	%

AC WAVEFORMS

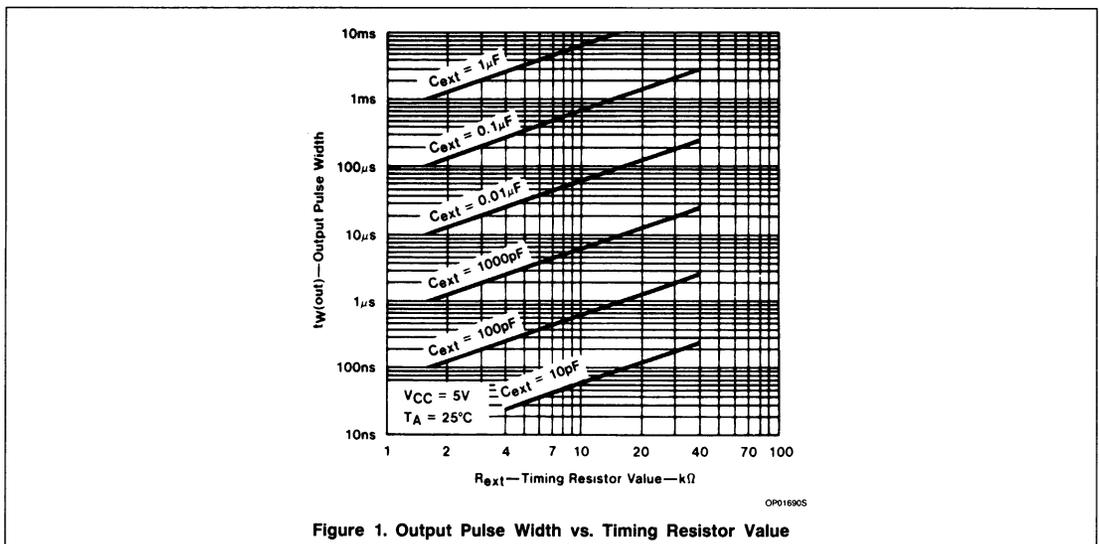
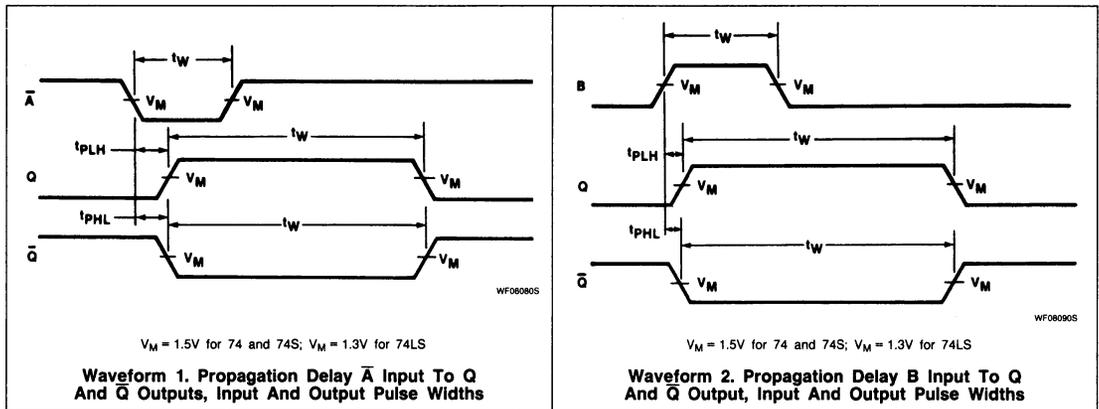
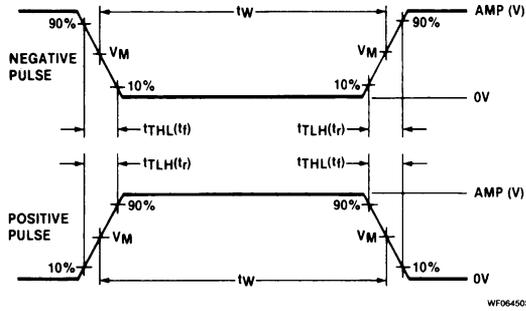
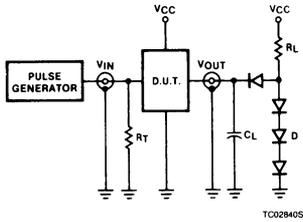


Figure 1. Output Pulse Width vs. Timing Resistor Value

Multivibrator

74121

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74123 Multivibrator

Dual Retriggerable Monostable Multivibrator Product Specification

Logic Products

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses — up to 100% duty cycle
- Direct reset terminates output pulse
- Compensated for V_{CC} and temperature variations

DESCRIPTION

The '123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance (R_{ext}) and capacitance (C_{ext}) values. Once triggered, the basic pulse width may be extended by retriggering the gated active LOW going edge input (\bar{A}) or the active HIGH going edge input (B), or be reduced by use of the overriding active LOW reset.

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74123	24ns	46mA

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74123N
Plastic SO	N74123D

For pulse widths when $C_{ext} \leq 1000pF$, see Figure A.

When $C_{ext} > 1000pF$, the output pulse width is defined as:

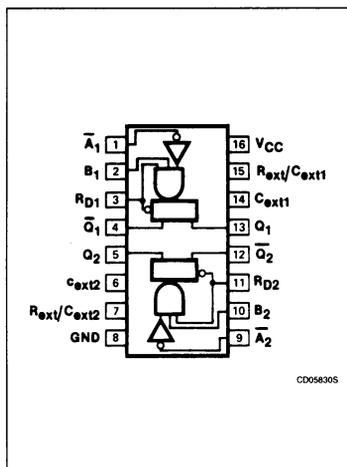
$$t_W \cong 0.28 R_{ext} \cdot C_{ext} (1 + \frac{0.7}{R_{ext}})$$

The external resistance and capacitance are normally connected as shown in Figure B. If an electrolytic capacitor is to be used with an inverse voltage rating of

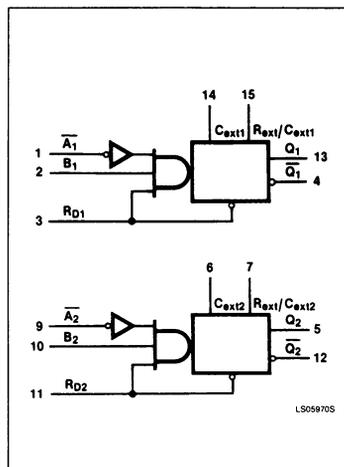
less than 1V then Figure C should be used. (Inverse voltage rating of an electrolytic is normally specified at 5% of the forward voltage rating.) If the inverse voltage rating is 1V or more (this includes a 100% safety margin) then Figure B can be used. Note that if Figure C is used the timing equations change as follows:

$$t_W \cong 0.25 R_{ext} \cdot C_{ext} (1 + \frac{0.7}{R_{ext}})$$

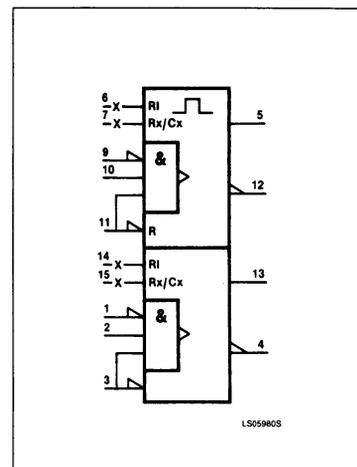
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Multivibrator

74123

FUNCTION TABLE

INPUTS			OUTPUTS	
R _D	\bar{A}	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	L	↓		
↑	L	H		

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH transition
 ↓ = HIGH-to-LOW transition
 = One HIGH-level pulse
 = One LOW-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
\bar{A} , B	Inputs	1ul
R _D	Input	2ul
Q, \bar{Q}	Outputs	10ul

NOTE:
 A 74 unit load (ul) is understood to be 40μA I_{IH} and -1.6mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
I _{IK} Input clamp current			-12	mA
I _{OH} HIGH-level output current			-800	μA
I _{OL} LOW-level output current			16	mA
T _A Operating free-air temperature	0		70	°C
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V

5

Multivibrator

74123

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74123			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage ⁵	V _{CC} = MIN, I _{OH} = MAX	2.4	3.4		V	
V _{OL} LOW-level output voltage ⁵	V _{CC} = MIN, I _{OL} = MAX		0.2	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	A̅, B inputs		40	μA	
		R _D input		80	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	A̅, B inputs		-1.6	mA	
		R _D input		-3.2	mA	
I _{OS} Short-circuit output current ^{3, 5}	V _{CC} = MAX	-10		-40	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Quiescent		46	66	mA
		Triggered		46	66	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Quiescent I_{CC} is measured (after being reset) with 2.4V applied to both R_D and A̅ inputs, B inputs grounded and all outputs open. Triggered I_{CC} is measured with 2.4V applied to all R_D and B inputs, A̅ inputs grounded and all outputs open. For both measurements, C_{ext} = 0.02μF and R_{ext} = 25kΩ.
- Ground C_{ext} to measure V_{OH} at Q, V_{OL} at Q̅, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at Q̅, V_{OL} at Q, or I_{OS} at Q̅.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} t _{PHL}	Waveform 1 C _{ext} = 0pF, R _{ext} = 5kΩ	33 40		ns
t _{PLH} t _{PHL}	Waveform 2 C _{ext} = 0pF, R _{ext} = 5kΩ	28 36		ns
t _{PLH} t _{PHL}	Waveform 3 R _D input to Q & Q̅ output C _{ext} = 0pF, R _{ext} = 5kΩ	40 27		ns
t _{wQ}	Waveforms 1 & 2 C _{ext} = 0pF, R _{ext} = 5kΩ	65		ns
t _{wQ}	Waveforms 1 & 2 C _{ext} = 1000pF, R _{ext} = 10kΩ	2.76	3.37	μs

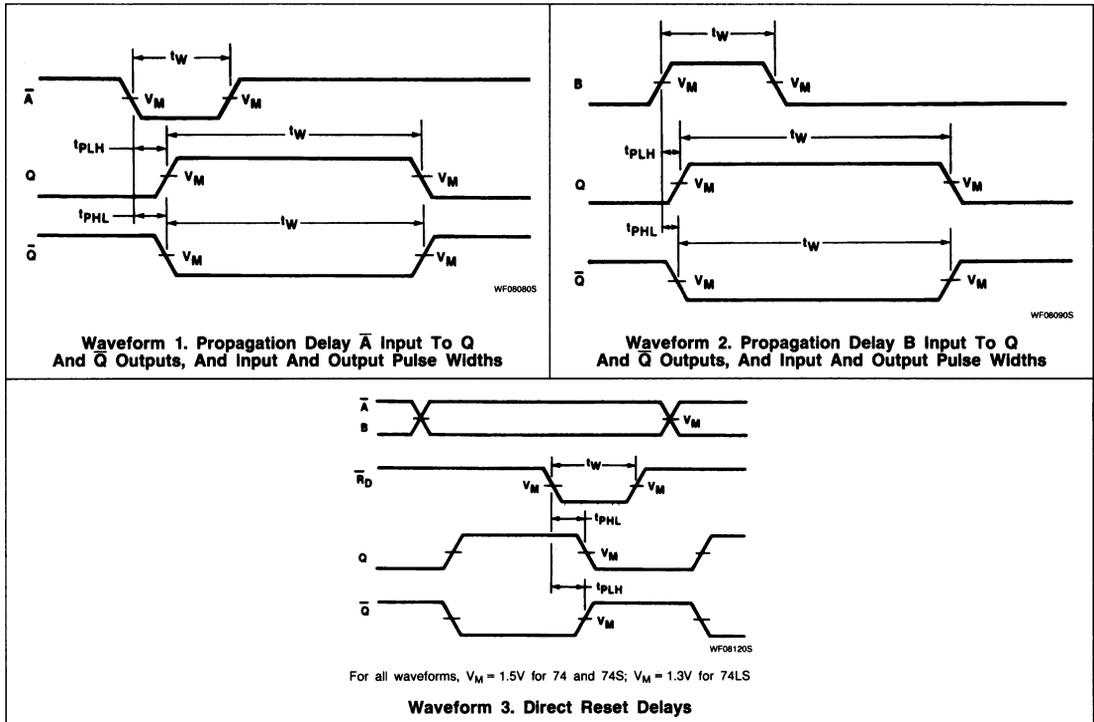
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t _w	Minimum input pulse width	40		ns
R _{ext}	External timing resistor range	5.0	50	kΩ
C _{ext}	External timing capacitance range	No restriction		pF
C _{Rx/Cx}	Stray capacitance to GND at R _{ext} /C _{ext} terminal		50	pF

Multivibrator

74123

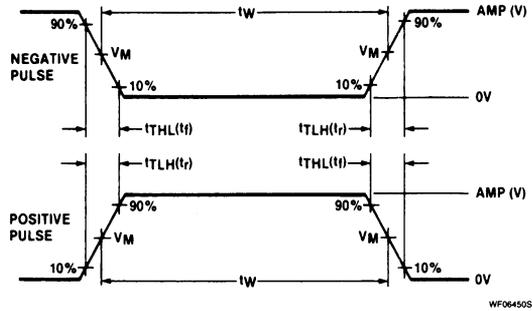
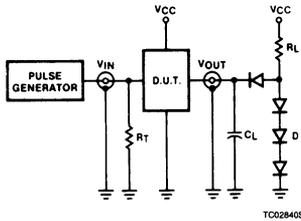
AC WAVEFORMS



Multivibrator

74123

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

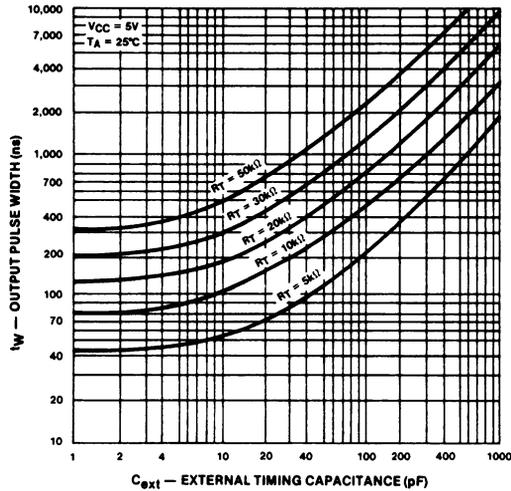
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Multivibrator

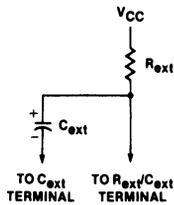
74123

TYPICAL PERFORMANCE CHARACTERISTICS



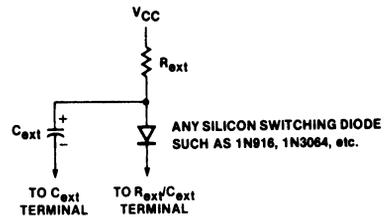
OP01700S

Figure A



TC02870S

Figure B



TC02880S

Figure C

5

74125, 74126, LS125A, LS126A

Buffers

Quad 3-State Buffer
Product Specification

FUNCTION TABLE '125, 'LS125A

INPUTS		OUTPUT
C	A	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE '126, 'LS126A

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74125	10ns	32mA
74LS125A	8ns	11mA
74126	10ns	36mA
74LS126A	9ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74125N, N74LS125N N74126N, N74LS126N
Plastic SO	N74LS125AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

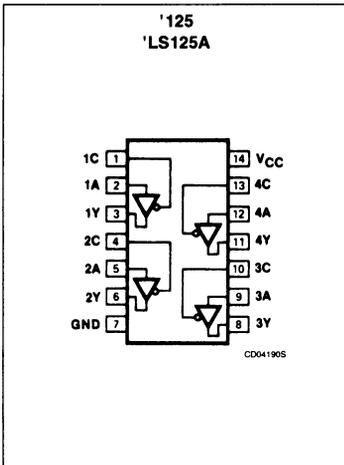
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	30LSul

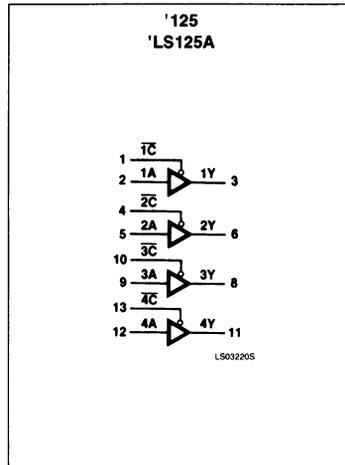
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

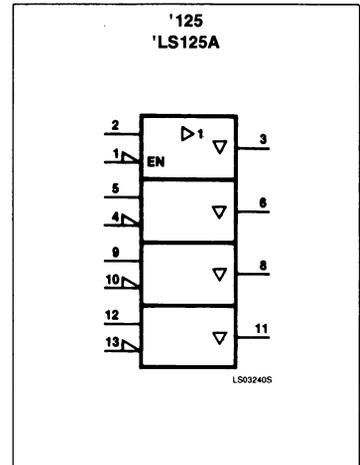
PIN CONFIGURATION



LOGIC SYMBOL



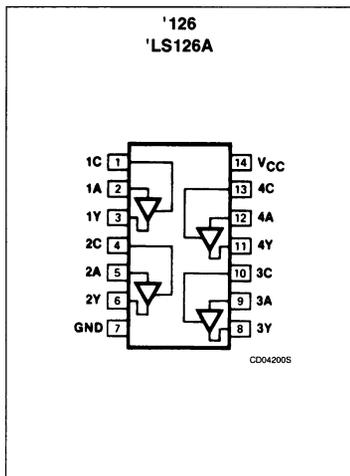
LOGIC SYMBOL (IEEE/IEC)



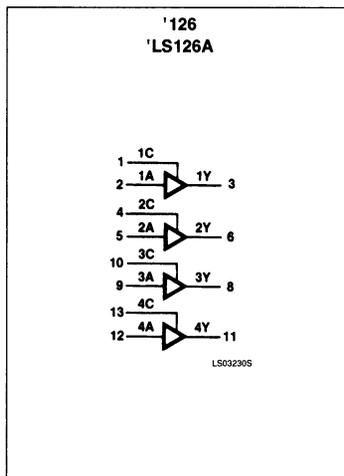
Buffers

74125, 74126, LS125A, LS126A

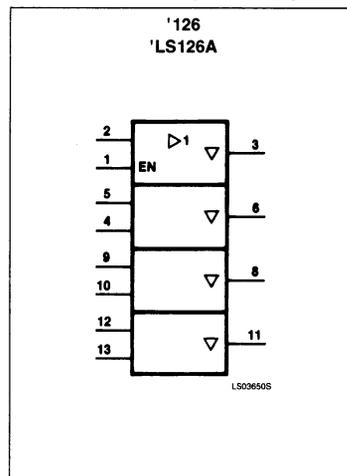
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-5.2			-2.6	mA
I _{OL} LOW-level output current			16			24	mA
T _A Operating free-air temperature	0		70	0		70	°C

Buffers

74125, 74126, LS125A, LS126A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74125 74126			74LS125A 74LS126A			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.1		2.4			V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX			0.4		0.35	0.5	V
		I _{OL} = 12mA (74LS)					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V				40			20	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.4V				-40			-20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA
		V _I = 7.0V						0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40				μA
		V _I = 2.7V						20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-28		-70	-40		-130	mA
I _{CC} Supply current (total)	V _{CC} = MAX	'125		32	54		11	20	mA
		'126		36	62		12	22	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

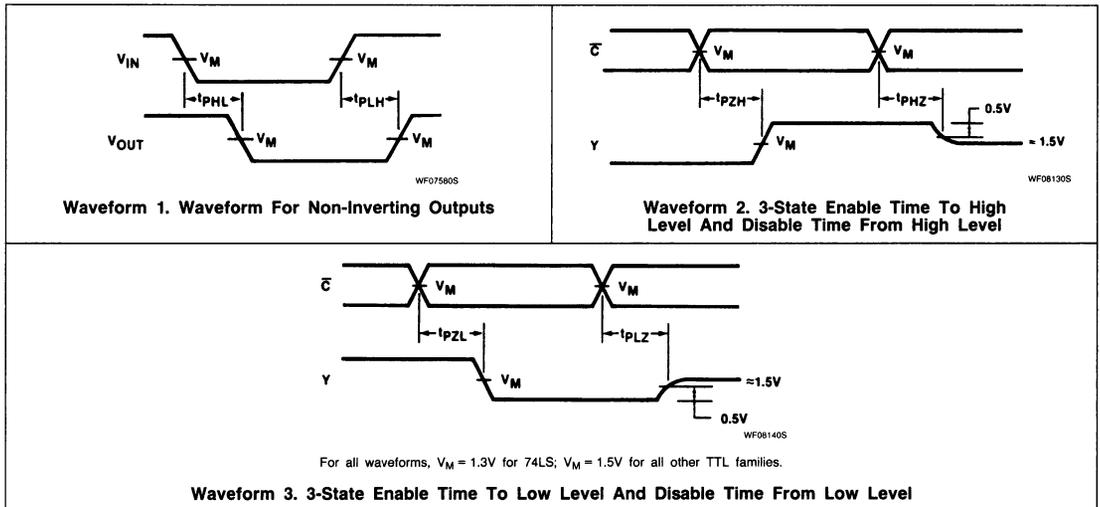
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Buffers

74125, 74126, LS125A, LS126A

AC WAVEFORMS



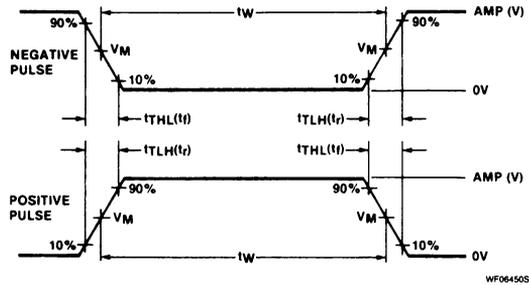
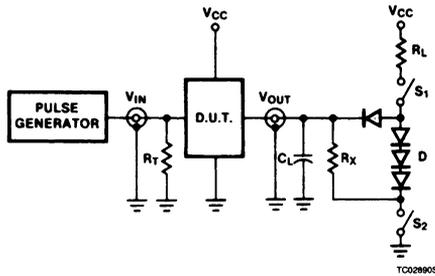
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	74125		74LS125A		74126		74LS126A		UNIT
		$C_L = 50pF$ $R_L = 400\Omega$		$C_L = 45pF$ $R_L = 667\Omega$		$C_L = 50pF$ $R_L = 400\Omega$		$C_L = 45pF$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		13		15		13		15	ns
t_{PHL} Data to output			18		18		18		18	
t_{PZH} Enable to HIGH	Waveform 2		17		20		18		25	ns
t_{PZL} Enable to LOW	Waveform 3		25		25		25		35	ns
t_{PHZ} Disable from HIGH	Waveform 2, $C_L = 5pF$		8.0		20		16		25	ns
t_{PLZ} Disable from LOW	Waveform 3, $C_L = 5pF$		12		20		18		25	ns

Buffers

74125, 74126, LS125A, LS126A

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

74128 Buffer

Quad Two-Input NOR Buffer
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74128	7ns	23mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74128N

NOTES:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

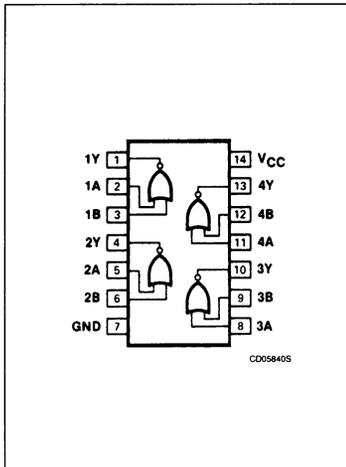
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
A, B	Inputs	1ul
Y	Output	30ul

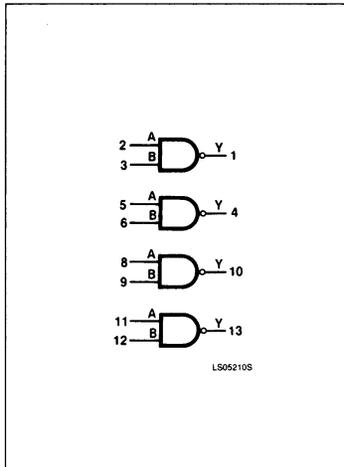
NOTE:

Where a 74 unit load is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

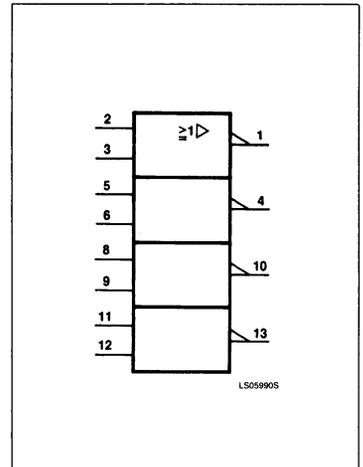
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffer

74128

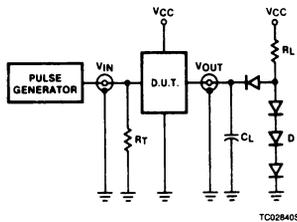
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

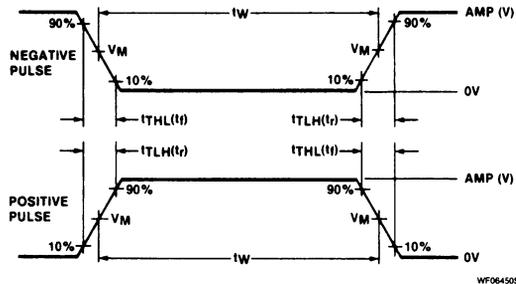
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC}	4.75	5.0	5.25	V
V _{IH}	2.0			V
V _{IL}			+0.8	V
I _{IK}			-12	mA
I _{OH}			-42.4	mA
I _{OL}			48	mA
T _A	0		70	°C

TEST CIRCUITS AND WAVEFORMS



TC028405



WF064505

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffer

74128

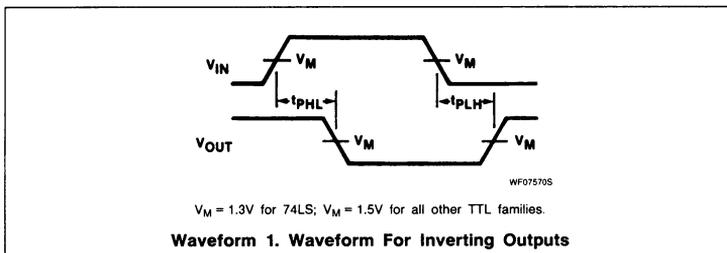
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74128			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = 0.8V, I _{OH} = -2.4mA	2.4	3.4		V
	V _{CC} = MIN, V _{IL} = 0.4V, I _{OH} = -13.2V	2.4			V
	V _{CC} = MIN, V _{IL} = 0.4V, I _{OH} = MAX	2.0			V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-70		-180	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH	12	21	mA
		I _{CC} L Outputs LOW	33	57	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		R _L = 133Ω		
		Min	Max	
t _{PLH} t _{PHL}	Propagation delay C _L = 50pF		9 12	ns
t _{PLH} t _{PHL}	Propagation delay C _L = 150pF		15 18	ns

74132, LS132 Schmitt Triggers

Quad 2-Input NAND Schmitt Trigger
Product Specification

Logic Products

The '132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+MAX} , the gate will respond to the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74132	15ns	21mA
74LS132	15ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74132N, N74LS132N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
A, B	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

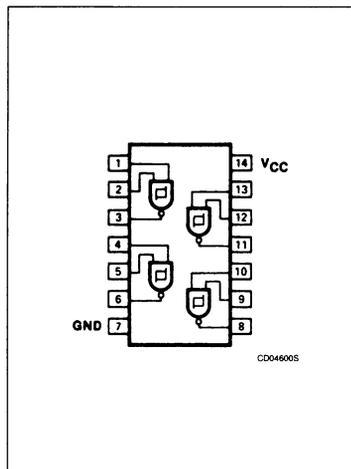
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

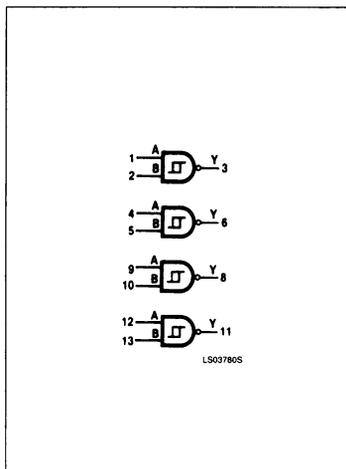
H = HIGH voltage level

L = LOW voltage level

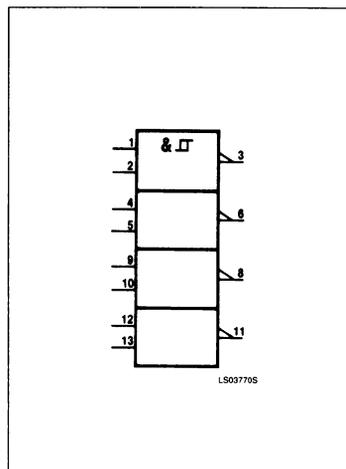
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Schmitt Triggers

74132, LS132

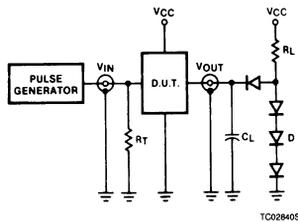
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

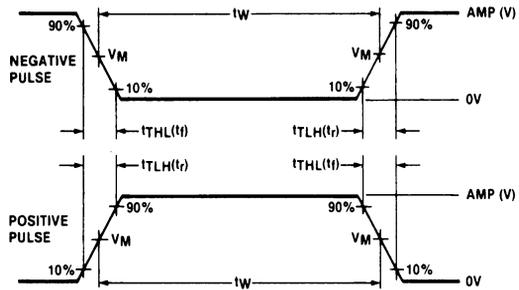
TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Schmitt Triggers

74132, LS132

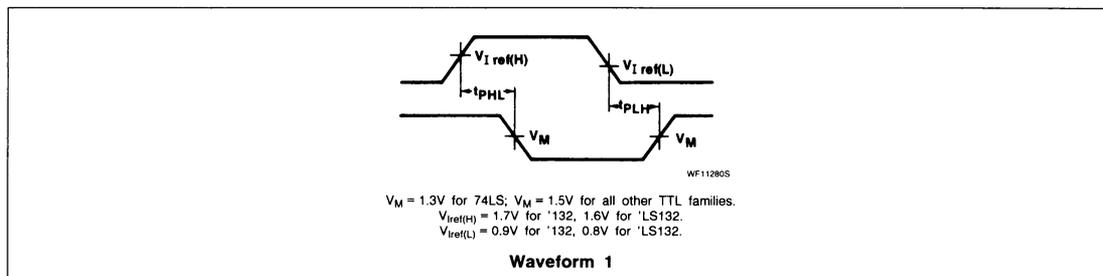
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74132			74LS132			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{T+}	Positive-going threshold	V _{CC} = 5.0V							V
V _{T-}	Negative-going threshold	V _{CC} = 5.0V							V
ΔV _T	Hysteresis (V _{T+} - V _{T-})	V _{CC} = 5.0V							V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _I = V _{T-} - MIN, I _{OH} = MAX							V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _I = V _{T+} + MAX		I _{OL} = MAX				V	
				I _{OL} = 4mA (74LS)				V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}							V
I _{T+}	Input current at positive-going threshold	V _{CC} = 5.0V, V _I = V _{T+}							mA
I _{T-}	Input current at negative-going threshold	V _{CC} = 5.0V, V _I = V _{T-}							mA
I _I	Input current at maximum input voltage	V _{CC} = MAX							mA
		V _I = 5.5V							mA
I _{IH}	HIGH-level input current	V _{CC} = MAX							μA
		V _I = 2.4V							μA
I _{IL}	LOW-level input current	V _{CC} = MAX							μA
		V _I = 2.7V							μA
I _{LOS}	Short-circuit output current ³	V _{CC} = MAX, V _I = 0.4V							mA
I _{CC}	Supply current (total)	V _{CC} = MAX							mA
		I _{CC} H	Outputs HIGH	15	24	5.9	11	mA	
		I _{CC} L	Outputs LOW	26	40	8.2	14	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

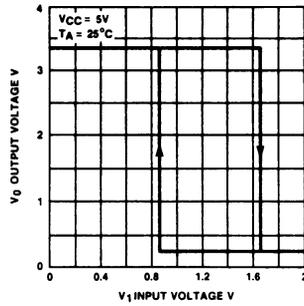
AC WAVEFORM



Schmitt Triggers

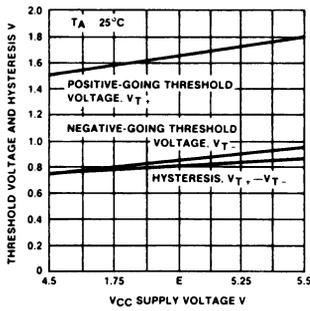
74132, LS132

TYPICAL CHARACTERISTICS



OP01640S

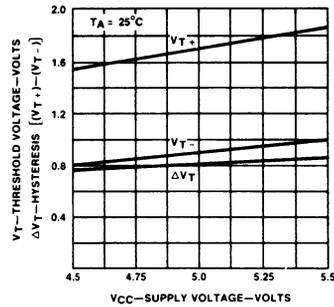
(74, 74LS)
 V_{In} vs V_{Out}
 Transfer Function



OP01650S

(74)

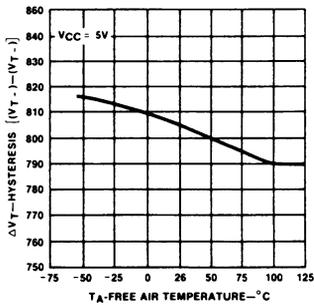
Threshold Voltage And Hysteresis vs Power Supply Voltage



OP01660S

(74LS)

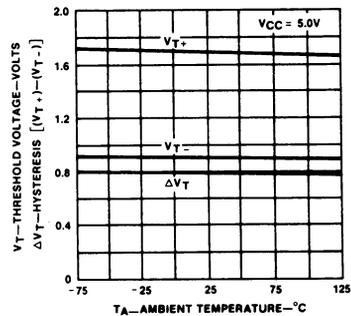
Threshold Voltage And Hysteresis vs Power Supply Voltage



OP01670S

(74)

Hysteresis vs Temperature



OP01680S

(74LS)

Threshold Voltage And Hysteresis vs Ambient Temperature

5

Schmitt Triggers

74132, LS132

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		22 22		22 22	ns

74S133 Gate

13-Input NAND Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S133	4ns	4mA

FUNCTION TABLE

INPUTS	OUTPUT
A ... M	\bar{Y}
H ... H one input = L	L H

H = HIGH voltage level
L = LOW voltage level

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S133N
Plastic SO	N74S133D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

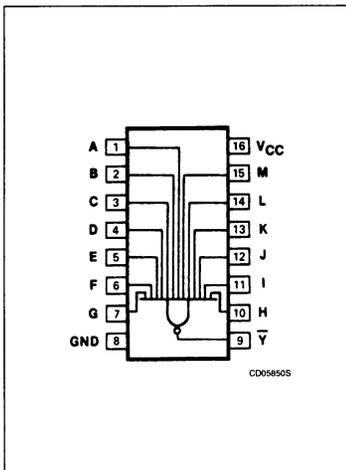
PINS	DESCRIPTION	74S
All	Inputs	1Sul
\bar{Y}	Output	10Sul

NOTE:

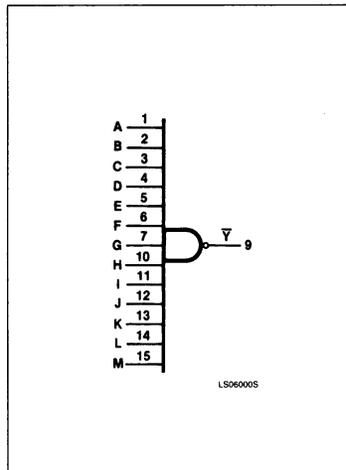
A 74S unit load (Sul) is understood to be $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

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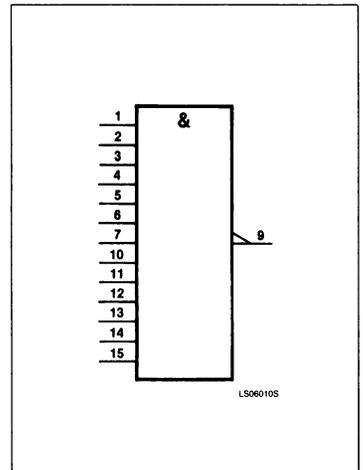
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74S133

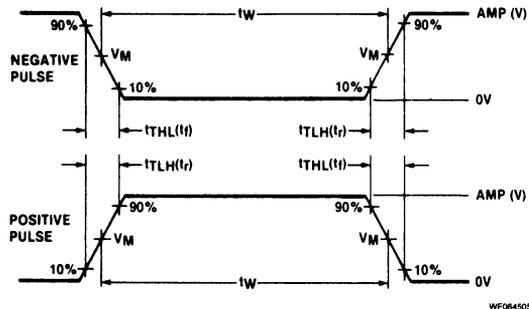
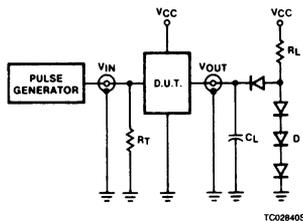
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74S			UNIT
	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	V
V_{IH}	2.0			V
V_{IL}			+0.8	V
I_{IK}			-18	mA
I_{OH}			-1000	μ A
I_{OL}			20	mA
T_A	0		70	°C

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{PLH} , t_{PHL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

74S133

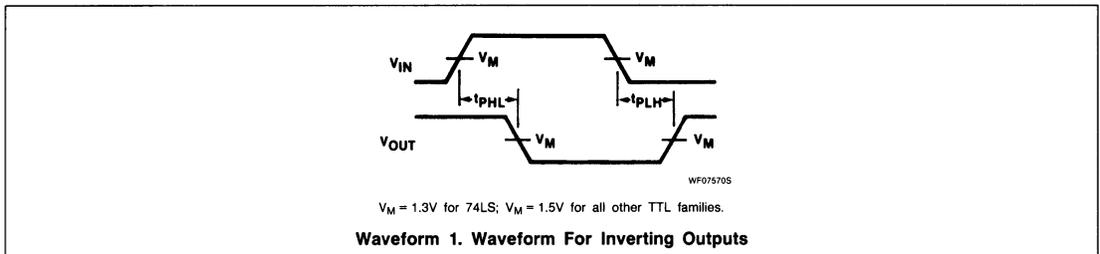
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S133			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX			0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			-2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		3	5	mA
		I _{CCL} Outputs LOW		5.5	10	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		6.0 7.0	ns

74S134 Gate

12-Input NAND Gate (3-State)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
74S134	5ns	10mA

FUNCTION TABLE

INPUTS		OUTPUT
D ₀ ... D ₁₁	\overline{OE}	\overline{Y}
H ... H one input = L	L	L
X ... X	L	H
	H	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V ±5%; T _A = 0°C to +70°C
Plastic DIP	N74S134N
Plastic SO	N74S134D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

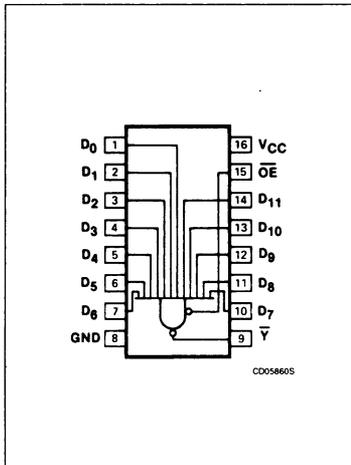
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
\overline{Y}	Output	10Sul

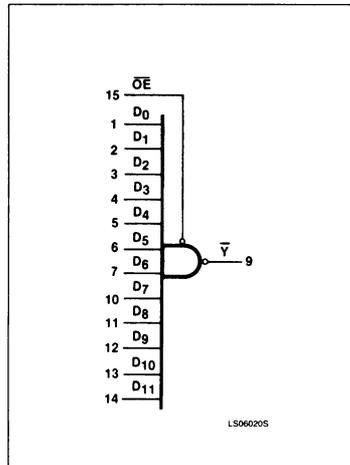
NOTE:

Where a 74S unit load (Sul) is understood to be 50μA I_{IH} and -2.0mA I_{IL}.

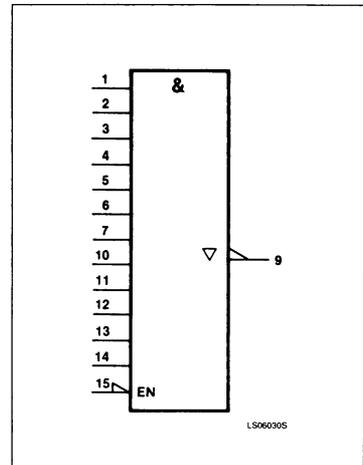
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74S134

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74S			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-6.5	μA
I _{OL}	LOW-level output current			20	mA
T _A	Operating free-air temperature	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS

TC028405

WF064505

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

74S134

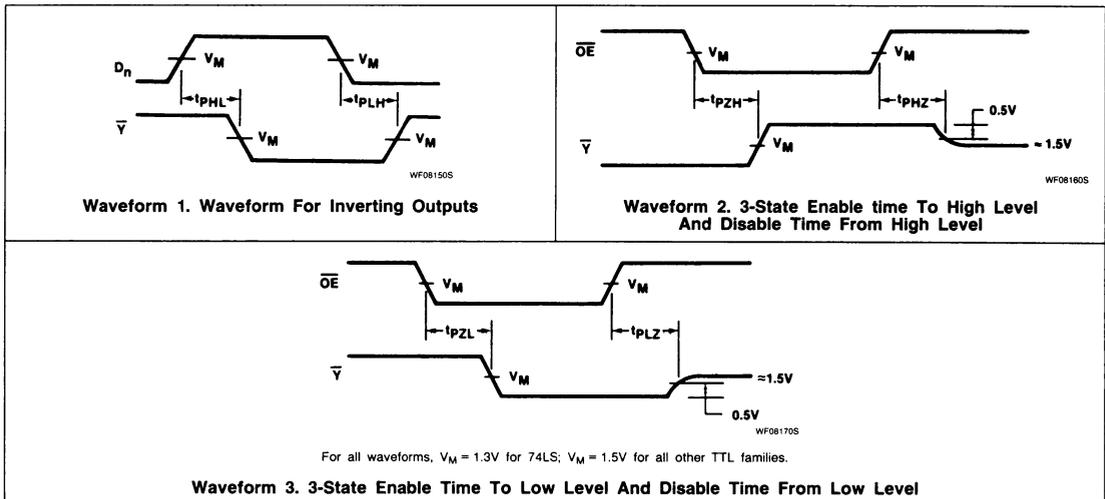
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S134			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX I _{OH} = -2mA I _{OH} = -6.5mA	2.4	3.2		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V	
I _{ozH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V			50	μA	
I _{ozL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.5V			-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			-2	mA	
I _{os} Short-circuit output current ³	V _{CC} = MAX	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH		7	13	mA
		I _{CC} L Outputs LOW		9	16	mA
		I _{CC} Z Outputs OFF		14	25	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



Gate

74S134

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Waveform 1		6.0	ns
t_{PHL} Propagation delay	Waveform 1		7.5	ns
t_{PZH} Enable to HIGH	Waveform 2, $C_L = 50\text{pF}$		19.5	ns
t_{PZL} Enable to LOW	Waveform 3, $C_L = 50\text{pF}$		21	ns
t_{PHZ} Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$		8.5	ns
t_{PLZ} Disable from LOW	Waveform 3, $C_L = 5\text{pF}$		14	ns

74S135 Gate

Quad Exclusive OR/NOR Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S135	9ns	65mA

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = HIGH voltage level
L = LOW voltage level

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S135N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

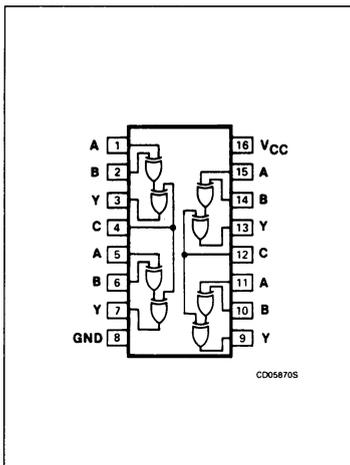
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
All	Outputs	10Sul

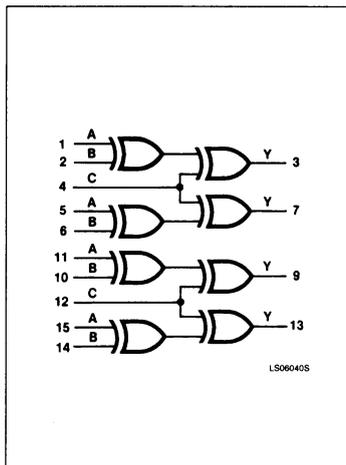
NOTE:

A 74S unit load (Sul) is understood to be $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

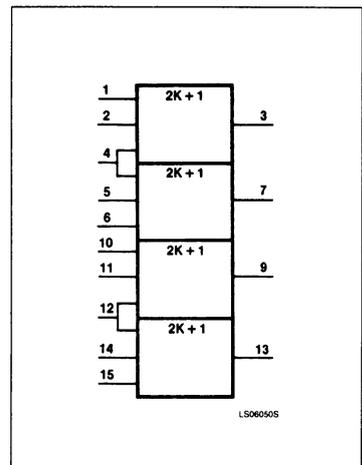
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74S135

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

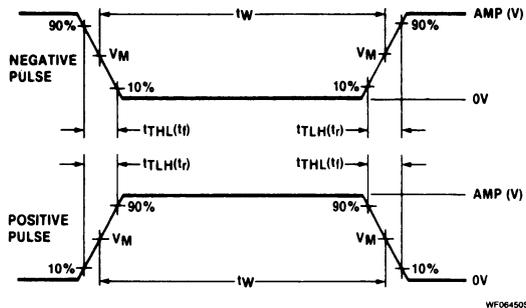
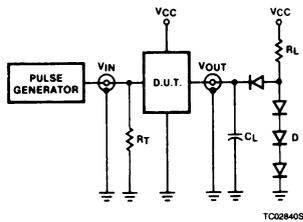
PARAMETER		74S	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74S			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-1000	μA
I _{OL}	LOW-level output current			20	mA
T _A	Operating free-air temperature	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

74S135

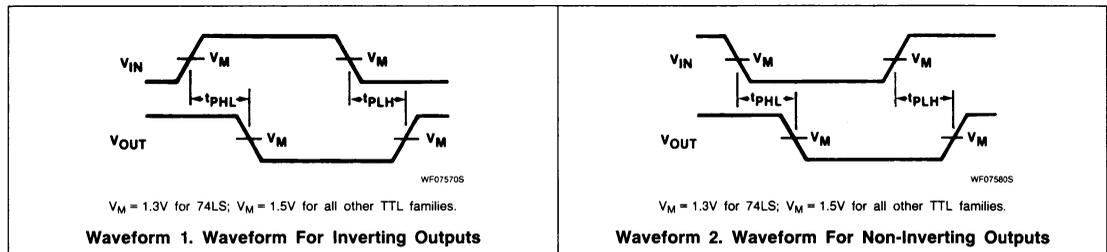
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S135			UNIT
		Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			0.5	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.2	V
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.7V			50	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.5V			-2	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-40		-100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		65	99	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the inputs grounded and the outputs open.

AC WAVEFORMS



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} t _{PHL}	Waveform 2, C = LOW, B or A = LOW		13 15	ns
t _{PLH} t _{PHL}	Waveform 1, C = LOW, B or A = HIGH		12 13.5	ns
t _{PLH} t _{PHL}	Waveform 1, C = HIGH, B or A = LOW		15 10	ns
t _{PLH} t _{PHL}	Waveform 2, C = HIGH, B or A = HIGH		12 11	ns
t _{PLH} t _{PHL}	Waveform 2, A = B		12 14.5	ns
t _{PLH} t _{PHL}	Waveform 1, A ≠ B		11.5 12	ns

74LS136 Gate

Quad Two-Input Exclusive-OR Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS136	18ns	6.1mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS136N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

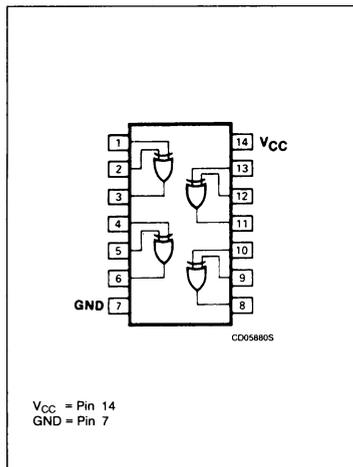
PINS	DESCRIPTION	74LS
A, B	Inputs	2LSul
Y	Output	10LSul

NOTE:

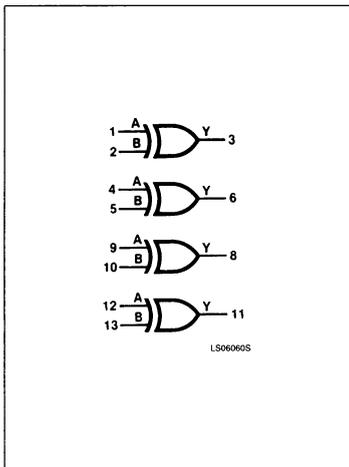
Where a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

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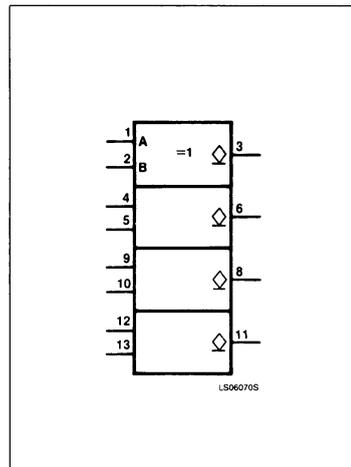
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74LS136

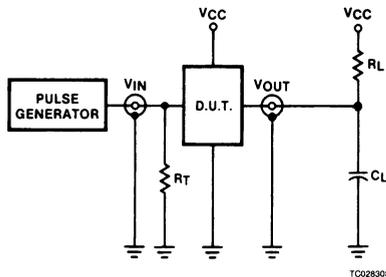
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

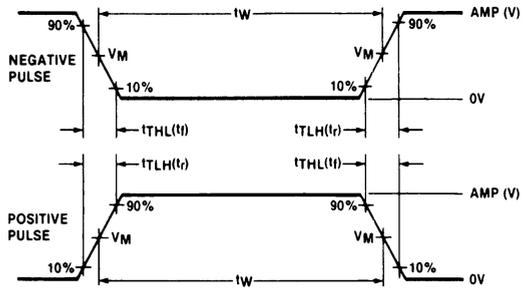
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
V _{OH}	HIGH-level output voltage			5.5	V
I _{OL}	LOW-level output current			8	mA
T _A	Operating free-air temperature	0		70	°C

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Gate

74LS136

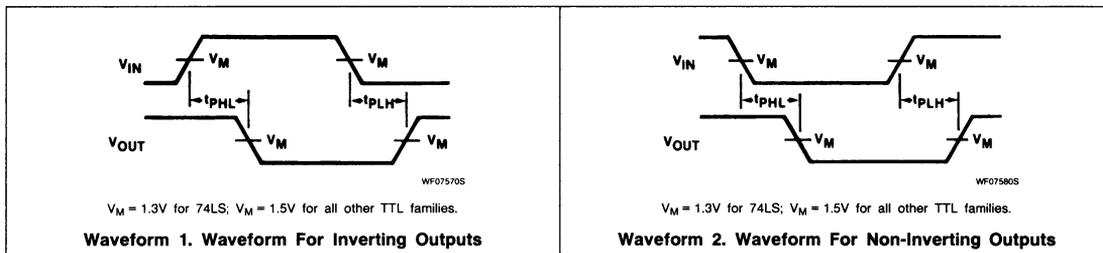
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS136			UNIT
		Min	Typ ²	Max	
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = MAX			100	μA
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.35	0.5	V
		I _{OL} = 4mA (74LS)	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.8	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		6.1	10	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with one input of each gate at 4.5V, the other inputs grounded, and all outputs open.

AC WAVEFORMS



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL}	Other input LOW Waveform 2		30 30	ns
t _{PLH} t _{PHL}	Other input HIGH Waveform 1		30 30	ns

74LS138, S138 Decoders/Demultiplexers

1-Of-8 Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\bar{O}_0 - \bar{O}_7$). The device features three Enable Inputs: two active LOW (\bar{E}_1, \bar{E}_2) and one active HIGH (E_3). Every output will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS138	20ns	6.3mA
74S138	7ns	49mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S138N, N74LS138N
Plastic SO	N74LS138D, N74S138D

NOTE:

For information regarding devices processed to Military Specifications see the Signetics Military Products Data Manual.

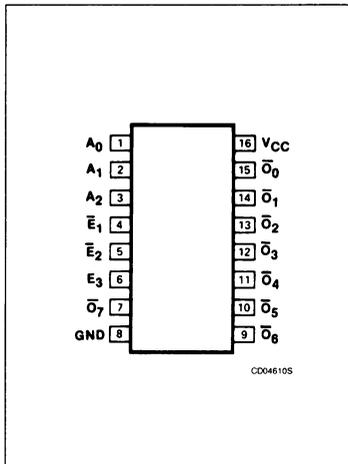
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

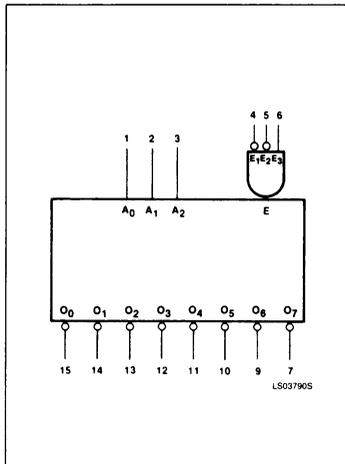
NOTE:

Where a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

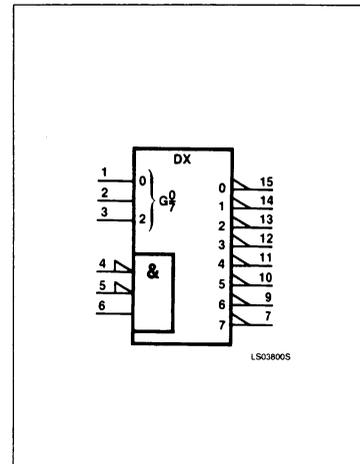
PIN CONFIGURATION



LOGIC SYMBOL



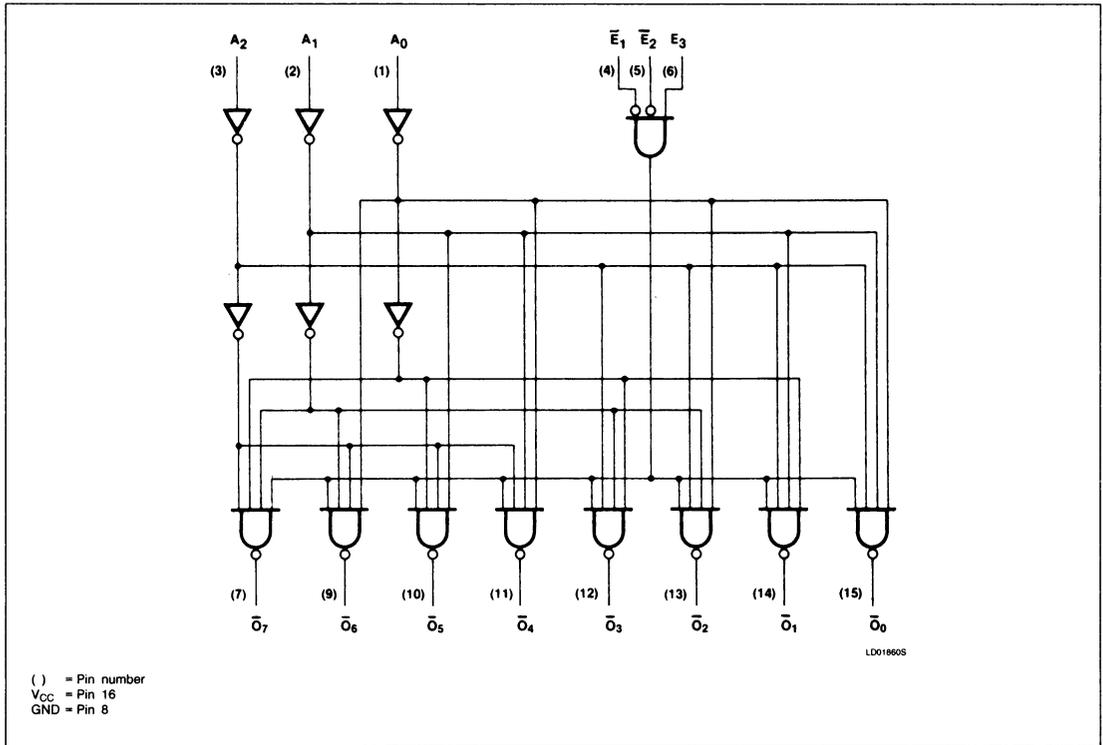
LOGIC SYMBOL (IEEE/IEC)



Decoders/Demultiplexers

74LS138, S138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

Decoders/Demultiplexers

74LS138, S138

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	HIGH-level output current			-400			-1000	μA
I_{OL}	LOW-level output current			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS138			74S138			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.35	0.5		0.5	V
		$I_{OL} = 4\text{mA (74LS)}$		0.25	0.4			V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5		-1.2	V
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$					1.0	mA
		$V_I = 7.0\text{V}$			0.1			mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20		50	μA
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$			-0.4			mA
		$V_I = 0.5\text{V}$					-2	mA
I_{OS}	Short-circuit output current ³ $V_{CC} = \text{MAX}$	-20		-100	-40		-100	mA
I_{CC}	Supply current ⁴ (total) $V_{CC} = \text{MAX}$		6.3	10		49	74	mA

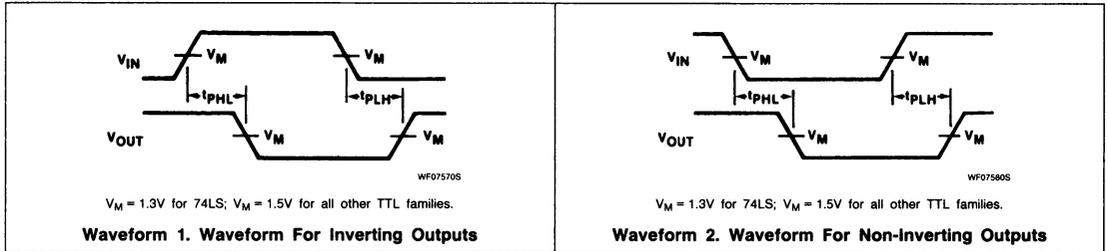
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- To measure I_{CC} , outputs must be enabled and open.

Decoders/Demultiplexers

74LS138, S138

AC WAVEFORMS

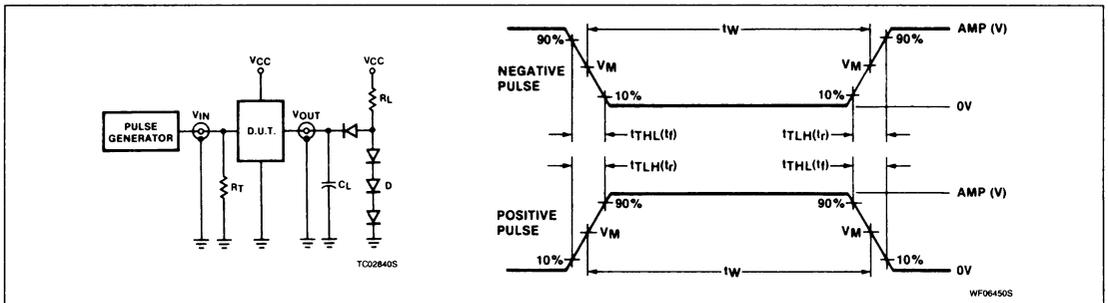


AC ELECTRICAL CHARACTERISTICS TA = 25°C, VCC = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		CL = 15pF, RL = 2kΩ		CL = 15pF, RL = 280Ω		
		Min	Max	Min	Max	
tPLH	Propagation delay		20		7	ns
tPHL	Address to output	2	41	3	10.5	
tPLH	Propagation delay		27		12	ns
tPHL	Address to output	3	39	3	12	
tPLH	Propagation delay		18		8	ns
tPHL	Enable to output	2	32	2	11	
tPLH	Propagation delay		26		11	ns
tPHL	Enable to output	3	38	3	11	

5

TEST CIRCUITS AND WAVEFORMS



VM = 1.3V for 74LS; VM = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

RL = Load resistor to VCC; see AC CHARACTERISTICS for value.

CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

RT = Termination resistance should be equal to ZOUT of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

tTLH, tTHL Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	tTLH	tTHL
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS139, S139 Decoders/Demultiplexers

Dual 1-of-4 Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES

- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multifunction capability
- Replaces 9321 and 93L21 for higher performance

DESCRIPTION

The '139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0 , A_1) and providing four mutually exclusive active LOW outputs ($\bar{0} - \bar{3}$). Each decoder has an active LOW Enable (\bar{E}). When \bar{E} is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

TYPE	TYPICAL PROPAGATION DELAY (ENABLE AT 2 LOGIC LEVELS)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS139	19ns	6.8mA
74S139	6ns	60mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S139N, N74LS139N
Plastic SO	N74LS139D, N74S139D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

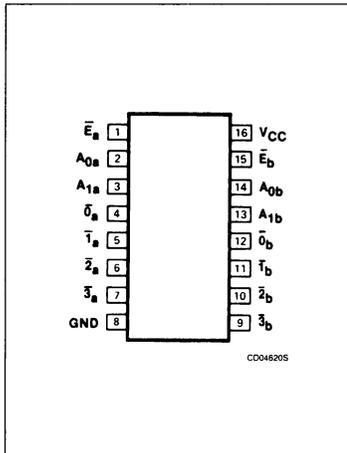
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

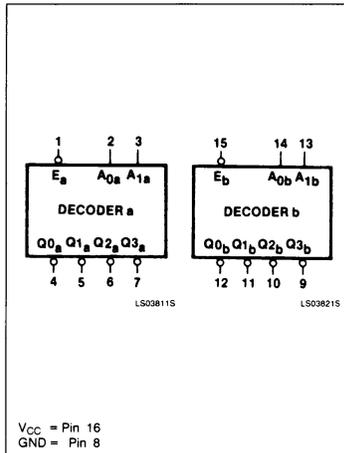
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

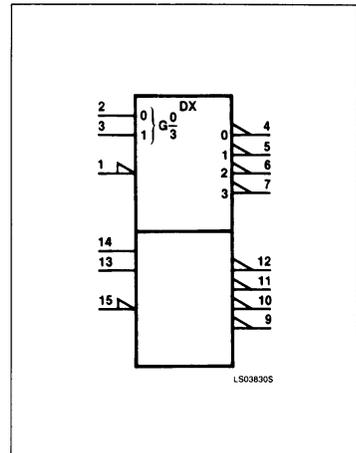
PIN CONFIGURATION



LOGIC SYMBOL



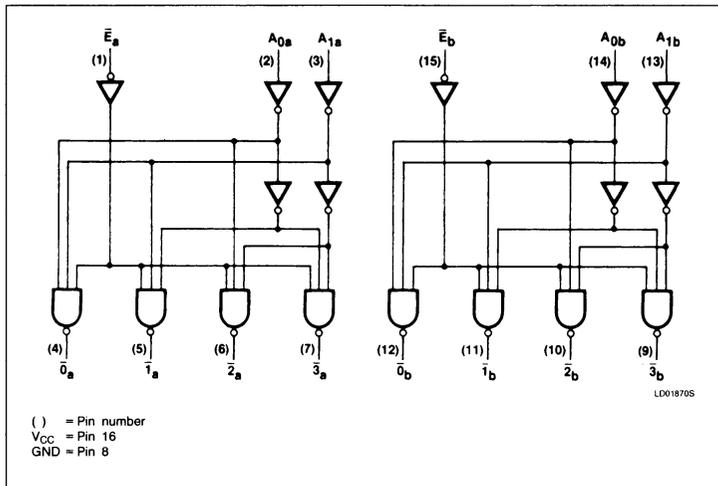
LOGIC SYMBOL (EEE/IEC)



Decoders/Demultiplexers

74LS139, S139

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS			
\bar{E}	A_0	A_1	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	HIGH-level output current			-400			-1000	μA
I_{OL}	LOW-level output current			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	°C

Decoders/Demultiplexers

74LS139, S139

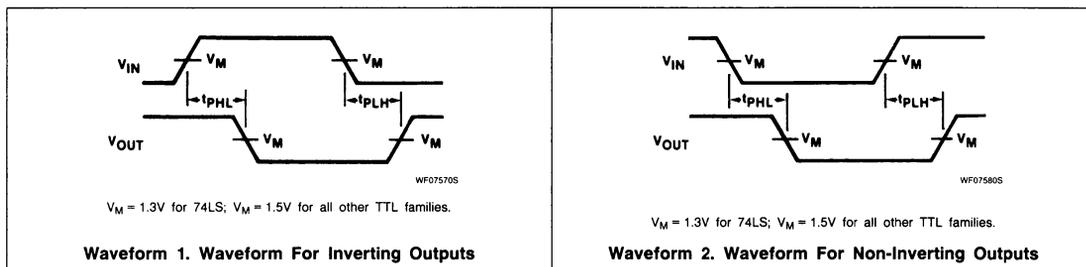
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS139			74S139			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX					0.5	V
		I _{OL} = 4mA (74LS)			0.35	0.4		V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA
		V _I = 7.0V				0.1		mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V				-0.4		mA
		V _I = 0.5V					-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-15		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		6.8	11		60	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.

AC WAVEFORMS



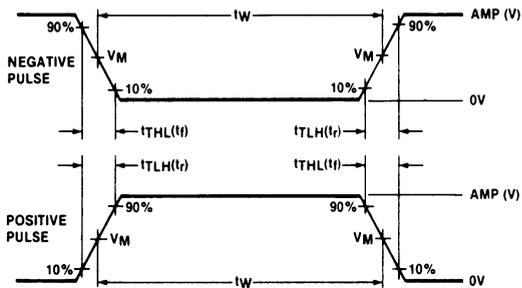
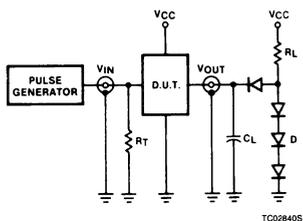
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 33	7.5 10	ns
t _{PLH} t _{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		29 38	12 12	ns
t _{PLH} t _{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		24 32	8 10	ns

Decoders/Demultiplexers

74LS139, S139

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74S140 Line Driver

Dual Four-Input NAND 50-Ohm Line Driver
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S140	4ns	10mA (I_{CCH}) 25mA (I_{CCL})

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	\bar{Y}
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S140N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

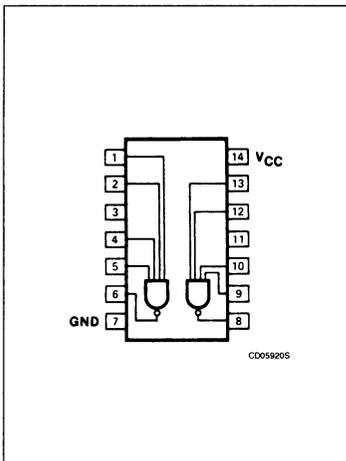
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
A - D	Inputs	2Sul
\bar{Y}	Output	30Sul

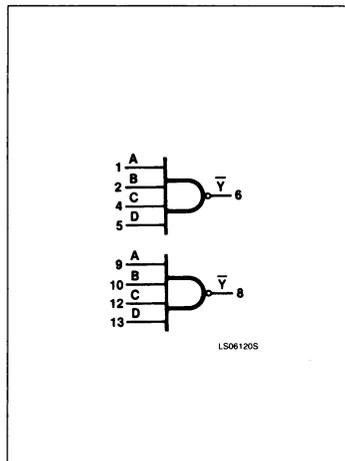
NOTE:

Where a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

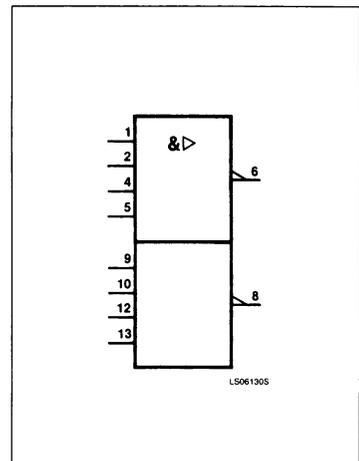
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Line Driver

74S140

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

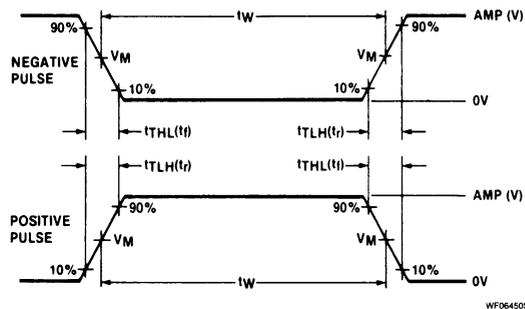
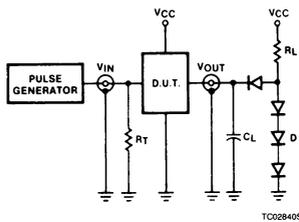
PARAMETER		74S	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74S			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-40	mA
I_{OL}	LOW-level output current			60	mA
T_A	Operating free-air temperature	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Line Driver

74S140

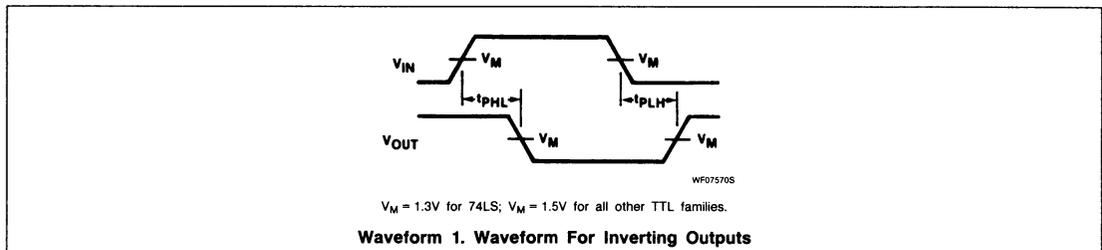
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S140			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -3mA	2.7	3.4		V
	V _{CC} = MIN, V _{IL} = 0.5V, R ₀ = 50Ω to ground	2.0			V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX			0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			100	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			-4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-50		-225	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	10	18	mA
		I _{CCL} Outputs LOW	25	44	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed 100 milliseconds.

AC WAVEFORM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74S		UNIT
		C _L = 50pF, R _L = 93Ω		
		Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		6.5 6.5	ns

74145 Decoder/Driver

BCD-To-Decimal Decoder/Driver (Open Collector)
Product Specification

Logic Products

FEATURES

- 80mA output drive capability
- 15V output breakdown voltage
- See '45 for 30V output voltage
- See '42 for standard TTL outputs

DESCRIPTION

The '145 is a 1-of-10 decoder with Open Collector outputs. This decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than '9' is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable.

The '145 features an output breakdown voltage of 15V. This device is ideal as a lamp or solenoid driver.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74145	24ns	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74145N
Plastic SO	N74145D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

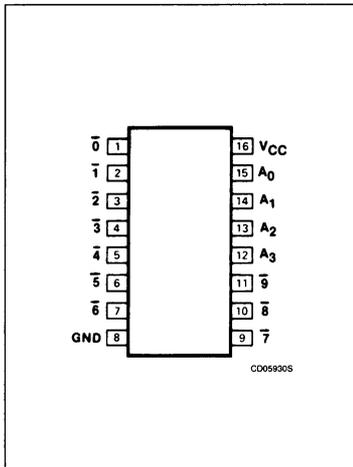
PINS	DESCRIPTION	74
All	Inputs	1ul
All	Outputs	12.5ul

NOTE:

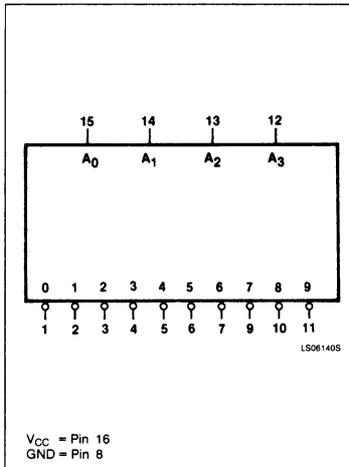
Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

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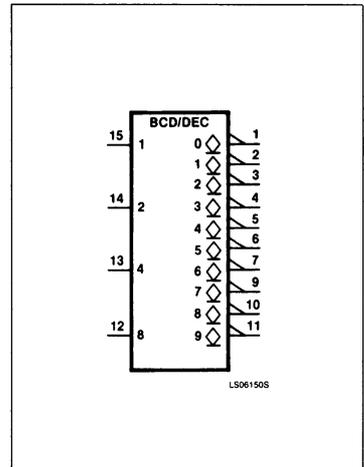
PIN CONFIGURATION



LOGIC SYMBOL



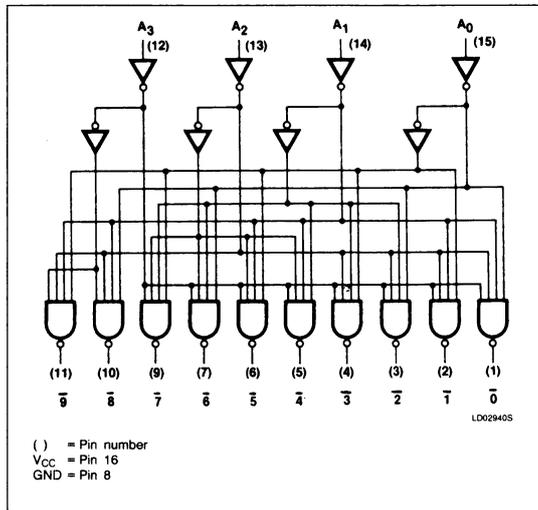
LOGIC SYMBOL (IEEE/IEC)



Decoder/Driver

74145

LOGIC DIAGRAM



FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +15	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
V _{OH} HIGH-level output voltage			15	V
I _{OL} LOW-level output current			80	mA
T _A Operating free-air temperature	0		70	°C

Decoder/Driver

74145

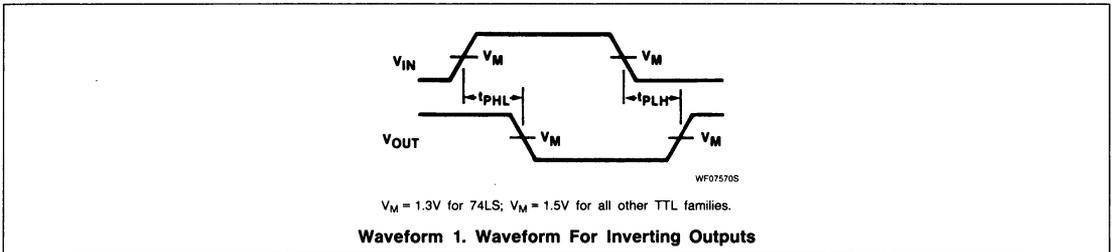
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74145			UNIT	
		Min	Typ ²	Max		
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = \text{MAX}$			250	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = 80\text{mA}$		0.5	0.9	V
		$I_{OL} = 20\text{mA}$			0.4	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA	
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$		43	70	mA	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
3. Measure I_{CC} with all inputs grounded and outputs open.

AC WAVEFORM



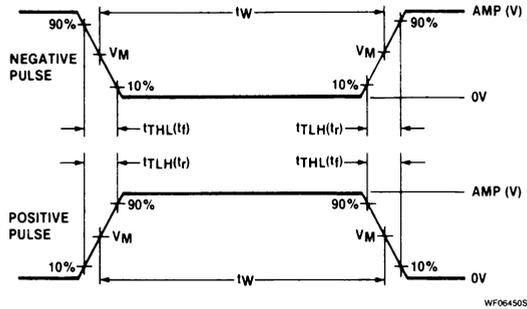
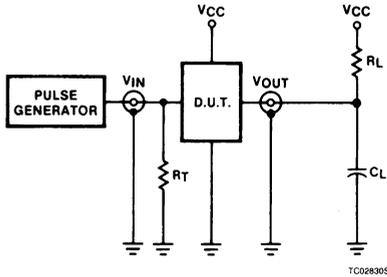
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		$C_L = 15\text{pF}, R_L = 100\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Waveform 1		50	ns
t_{PHL} Address to output			50	

Decoder/Driver

74145

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Open Collector Output

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74147 Encoder

10-Line-To-4-Line Priority Encoder
Product Specification

Logic Products

FEATURES

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators

DESCRIPTION

The '147 9-input priority encoder accepts data from nine active-LOW inputs ($\bar{I}_1 - \bar{I}_9$) and provides a binary representation on the four active-LOW outputs ($A_0 - A_3$). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \bar{I}_9 having the highest priority.

The device provides the 10-line-to-4-line priority encoding function by use of the implied decimal "zero." The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74147	10ns	46mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74147N

NOTE:

For information regarding devices processed to Military Specifications see the Signetics Military Products Data Manual.

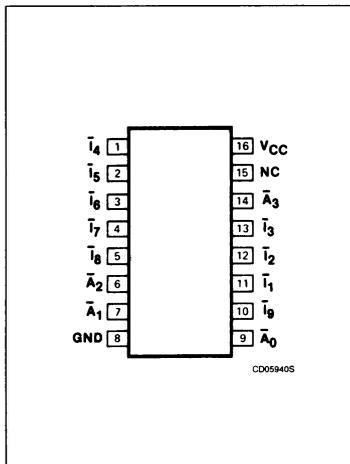
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1ul
All	Outputs	10ul

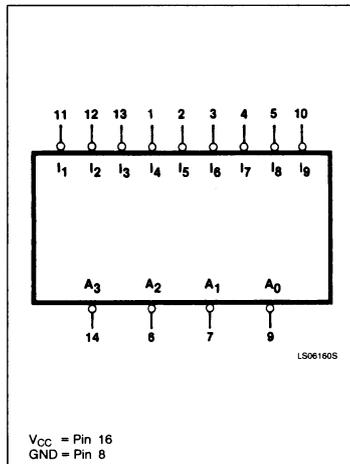
NOTE:

A 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

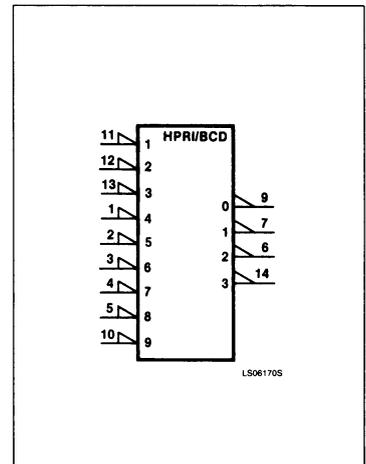
PIN CONFIGURATION



LOGIC SYMBOL



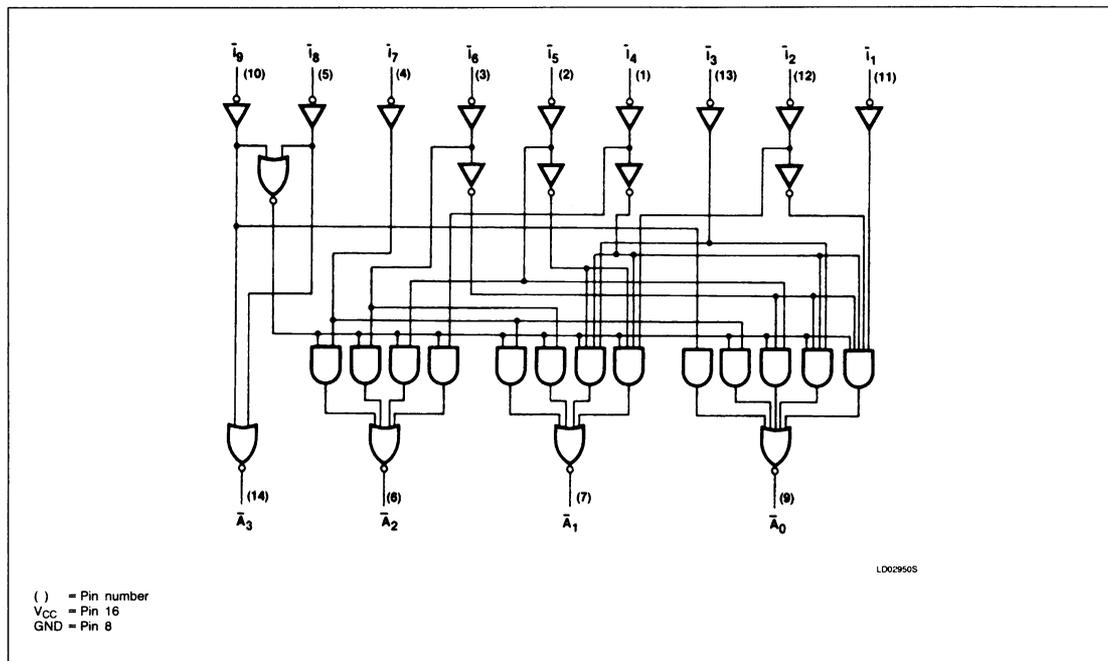
LOGIC SYMBOL (IEEE/IEC)



Encoder

74147

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS			
\bar{i}_1	\bar{i}_2	\bar{i}_3	\bar{i}_4	\bar{i}_5	\bar{i}_6	\bar{i}_7	\bar{i}_8	\bar{i}_9	\bar{A}_3	\bar{A}_2	\bar{A}_1	\bar{A}_0
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	H	H	H	H
X	X	X	X	X	L	H	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	L	L	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

Encoder

74147

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74147			UNIT		
		Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.3		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			0.2	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V				1.0	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V				40	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-35		-85	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		50	70	mA
			Condition 2		42	62	mA

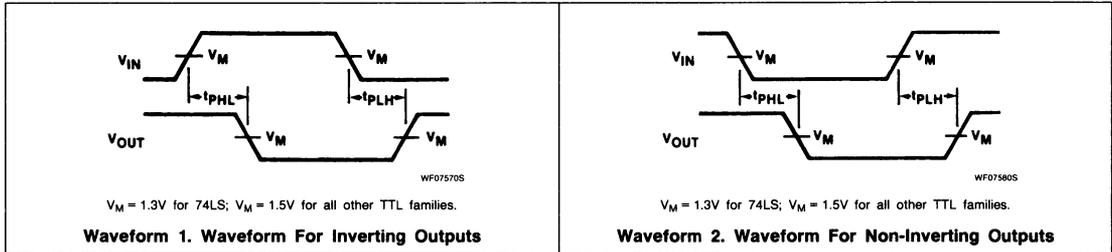
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Condition 1: Measure I_{CC} with I₇ grounded, other inputs and outputs open. Condition 2: Measure I_{CC} with all inputs and outputs open.

Encoder

74147

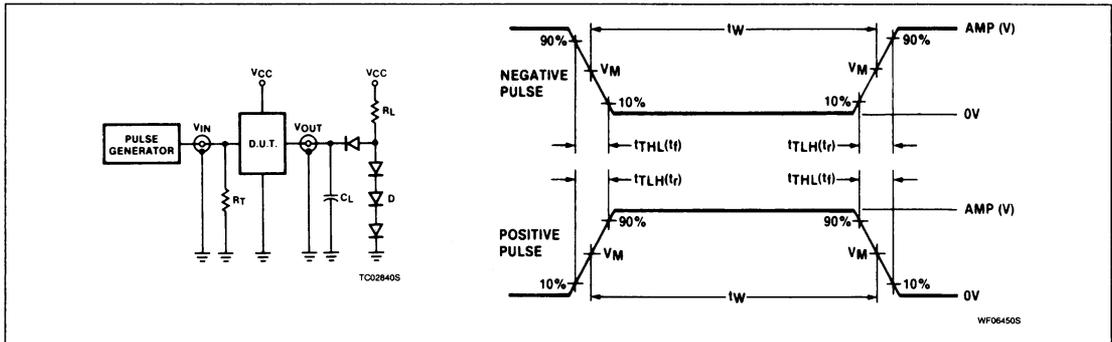
AC WAVEFORMS



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	74		UNIT
		$C_L = 15pF, R_L = 400\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Out-of-phase output	Waveform 1	19	ns
		Waveform 2	19	
t_{PLH} t_{PHL}	Propagation delay In-phase output	Waveform 2	14	ns
			11	

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74148 Encoder

8-Input Priority Encoder
Product Specification

Logic Products

FEATURES

- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N" bits
- Input Enable capability
- Priority encoding — automatic selection of highest priority input line
- Output Enable — active LOW when all inputs HIGH
- Group Signal output — active when any input is LOW

DESCRIPTION

The '148 8-input priority encoder accepts data from eight active-LOW inputs and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \bar{I}_7 having the highest priority.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74148	10ns	38mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74148N
Plastic SO	

NOTES:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

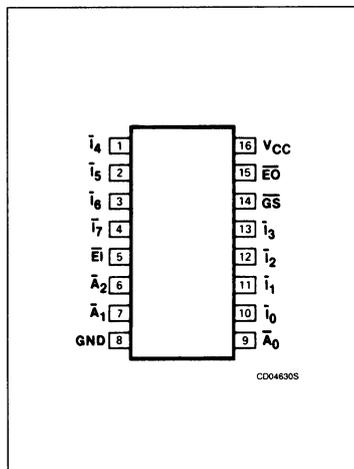
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
\bar{I}_0	Input	1ul
$\bar{I}_1 - \bar{I}_7$	Inputs	2ul
$\bar{E}I$	Input	2ul
All	Outputs	10ul

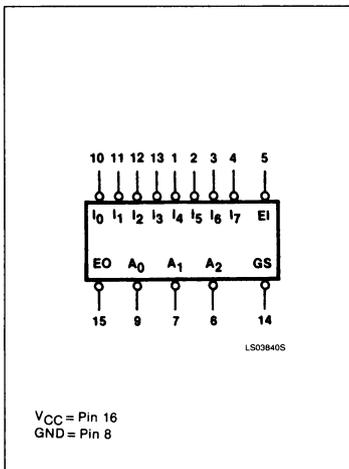
NOTE:

A 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

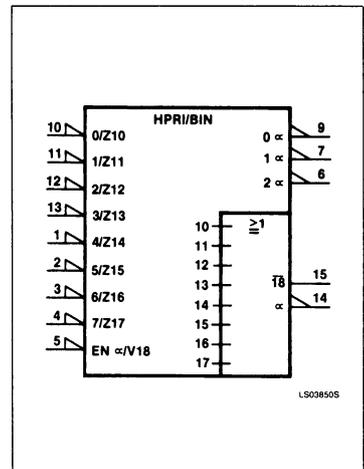
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Encoder

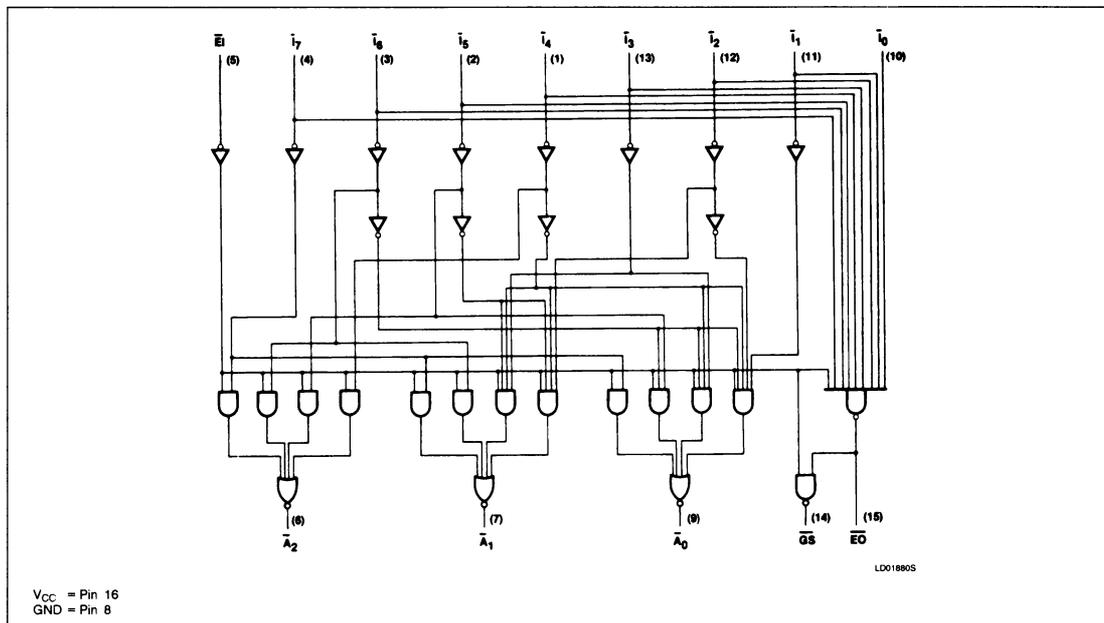
74148

A HIGH on the Enable Input (\bar{E}_1) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal (\bar{G}_S) output and an Enable Output (\bar{E}_0) are provided with the three data outputs. The \bar{G}_S is active-LOW when any input is LOW; this indicates when any input is active. The \bar{E}_0 is active-LOW when all inputs

are HIGH. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both \bar{E}_0 and \bar{G}_S are active-HIGH when the Enable input is HIGH.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS				
\bar{E}_1	\bar{I}_0	\bar{I}_1	\bar{I}_2	\bar{I}_3	\bar{I}_4	\bar{I}_5	\bar{I}_6	\bar{I}_7	\bar{G}_S	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{E}_0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	L	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Encoder

74148

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

Encoder

74148

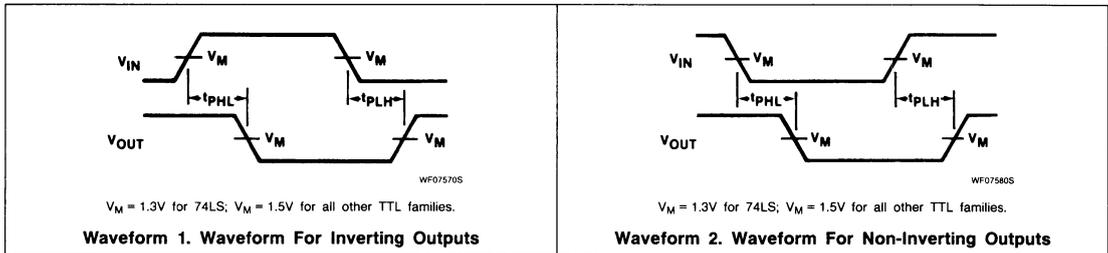
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74148			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.3		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	I _O input		40	μA	
		Other inputs		80	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	I _O input		-1.6	mA	
		Other inputs		-3.2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-35		-85	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		40	60	mA
		Condition 2		35	55	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX+0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Condition 1: Measure I_{CC} with I₇ (from I₀) and \bar{E} grounded, other inputs and outputs open. Condition 2: Measure I_{CC} with all inputs and outputs open.

AC WAVEFORMS



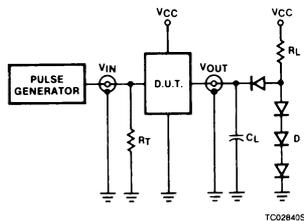
Encoder

74148

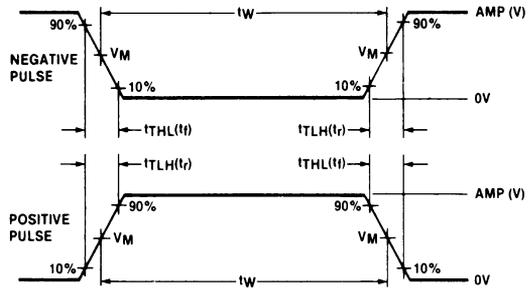
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT	
		$C_L = 15\text{pF}$, $R_L = 400\Omega$			
		Min	Max		
t_{PLH} t_{PHL}	Propagation delay I_n input to \bar{A}_n outputs	Waveform 2, in-phase output		15 14	ns
t_{PLH} t_{PHL}	Propagation delay I_n input to \bar{A}_n outputs	Waveform 1, out-of-phase output		19 19	ns
t_{PLH} t_{PHL}	Propagation delay I_n input to $\bar{E}O$ output	Waveform 1, out-of-phase output		10 25	ns
t_{PLH} t_{PHL}	Propagation delay I_n input to $\bar{G}S$ output	Waveform 2, in-phase output		30 25	ns
t_{PLH} t_{PHL}	Propagation delay EI input to \bar{A}_n outputs	Waveform 2, in-phase output		15 15	ns
t_{PLH} t_{PHL}	Propagation delay EI input to $\bar{E}O$ output	Waveform 2, in-phase output		15 30	ns
t_{PLH} t_{PHL}	Propagation delay EI input to $\bar{G}S$ output	Waveform 2, in-phase output		12 15	ns

TEST CIRCUITS AND WAVEFORMS



TC02840S



WF06450S

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74150 Multiplexer

16-Input Multiplexer
Product Specification

Logic Products

FEATURES

- Select data from 16 sources
- Demultiplexing capability
- Active-LOW enable or strobe
- Inverting data output

DESCRIPTION

The '150 is a logical implementation of a single-pole, 16-position switch with the switch position controlled by the state of four Select inputs. S_0, S_1, S_2, S_3 . The Multiplexer output (\bar{Y}) inverts the selected data. The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH the \bar{Y} output is HIGH regardless of all other inputs. In one package the '150 provides the ability to select from 16 sources of data or control information.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74150	17ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74150N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

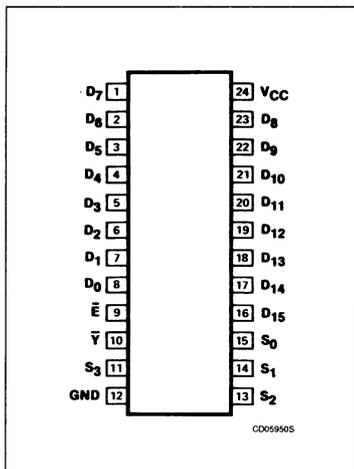
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1ul
\bar{Y}	Output	10ul

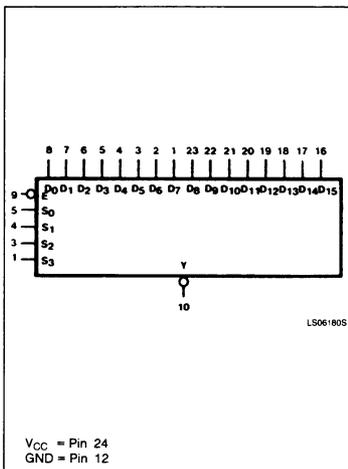
NOTE:

A 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

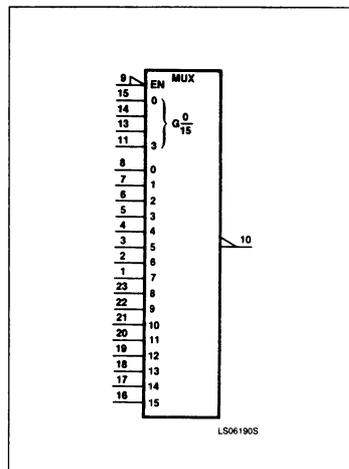
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Multiplexer

74150

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	HIGH-level output current			-800	μ A
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74150			UNIT
			Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}$		0.2	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μ A
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-18		-55	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		40	68	mA

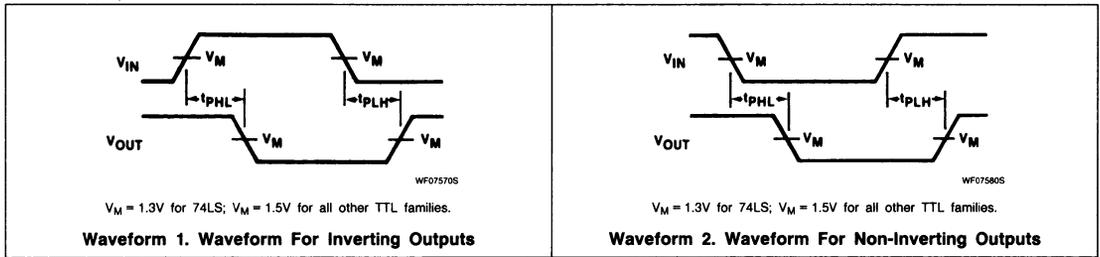
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with \bar{E} , $S_0 - S_3$ inputs at 4.5V, all other inputs and outputs open.

Multiplexer

74150

AC WAVEFORMS

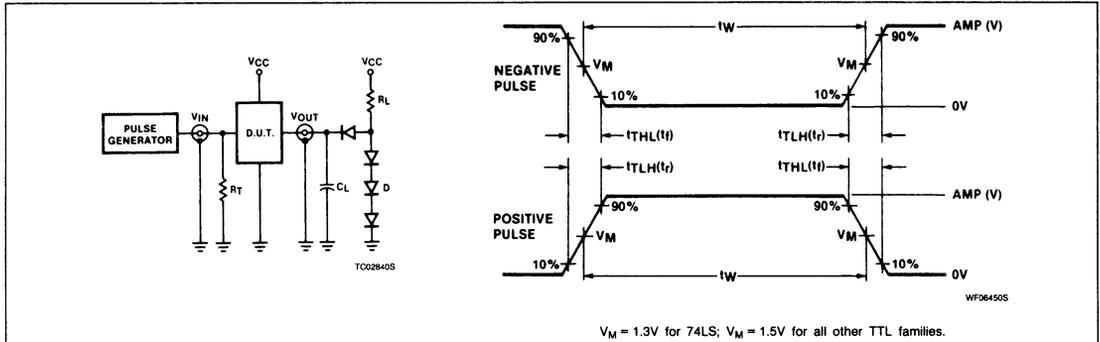


AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	74		UNIT
		$C_L = 15pF, R_L = 400\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to \bar{Y} output	Waveform 1	35 33	ns
t_{PLH} t_{PHL}	Propagation delay Enable to \bar{Y} output	Waveform 2	24 30	ns
t_{PLH} t_{PHL}	Propagation delay Data to \bar{Y} output	Waveform 1	14 20	ns

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TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74151, LS151, S151 Multiplexers

8-Input Multiplexer Product Specification

Logic Products

FEATURES

- Multifunction capability
- Complementary outputs
- See '251 for 3-state version

DESCRIPTION

The '151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2 . True (Y) and Complement (\bar{Y}) outputs are both provided. The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, the \bar{Y} output is HIGH and the Y output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Y = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

In one package the '151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

TYPE	TYPICAL PROPAGATION DELAY (ENABLE TO \bar{Y})	TYPICAL SUPPLY CURRENT (TOTAL)
74151	18ns	29mA
74LS151	12ns	6mA
74S151	9ns	45mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74151N, N74LS151N, N74S151N
Plastic SO	N74LS151D, N74S151D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

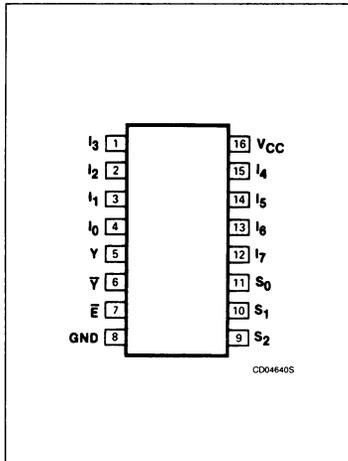
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

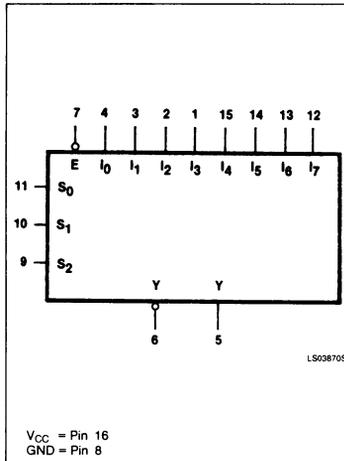
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION

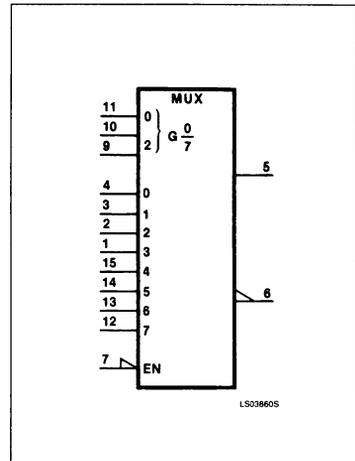


LOGIC SYMBOL



$V_{CC} = \text{Pin } 16$
 $GND = \text{Pin } 8$

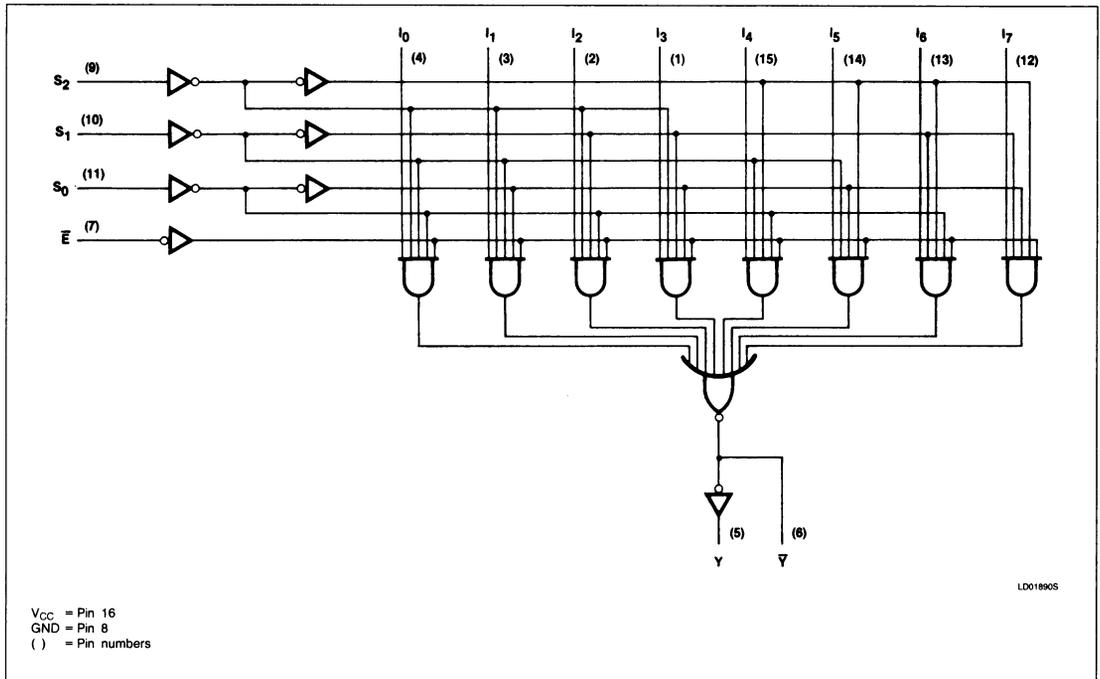
LOGIC SYMBOL (IEEE/IEC)



Multiplexers

74151, LS151, S151

LOGIC DIAGRAM



5

FUNCTION TABLE

				INPUTS								OUTPUTS	
\bar{E}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\bar{Y}	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	L	H	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

Multiplexers

74151, LS151, S151

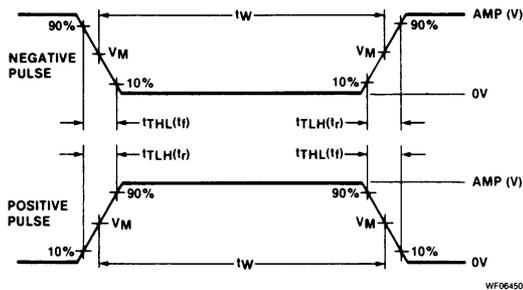
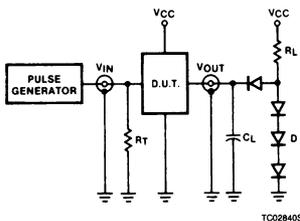
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Multiplexers

74151, LS151, S151

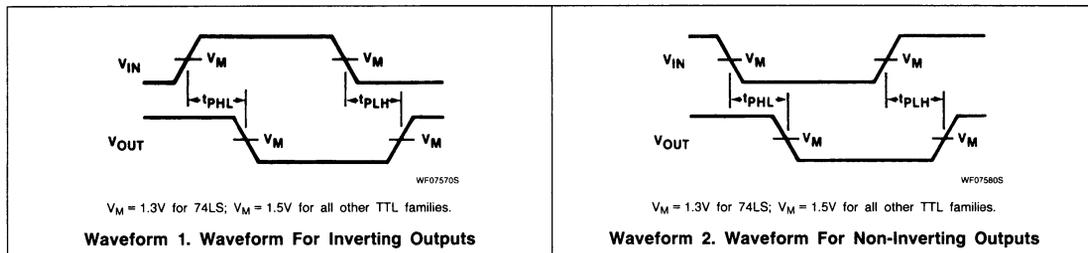
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74151			74LS151			74S151			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX			0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)						0.25	0.4			V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			-1.2	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V				1.0					1.0	mA
		V _I = 7.0V						0.1				mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V				40						μA
		V _I = 2.7V						20			50	μA
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V				-1.6			-0.4			mA
		V _I = 0.5V									-2.0	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-55	-20		-100	-40		-100	mA	
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		29	48		6	10		45	70	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} on the 74151 with \bar{E} and S₀ - S₂ at 4.5V, all other inputs and outputs open. Measure I_{CC} on the 74LS151 and 74S151 with all inputs at 4.5V and outputs open.

AC WAVEFORMS



Multiplexers

74151, LS151, S151

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT	
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		52 30		43 30		18 18	ns
t_{PLH} t_{PHL}	Propagation delay Select to \bar{Y} output	Waveform 1		35 33		23 32		15 13.5	ns
t_{PLH} t_{PHL}	Propagation delay Enable to Y output	Waveform 1		52 30		42 32		16.5 18	ns
t_{PLH} t_{PHL}	Propagation delay Enable to \bar{Y} output	Waveform 2		24 30		24 30		13 12	ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		29 24		32 26		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Data to \bar{Y} output	Waveform 1		20 14		21 20		7.0 7.0	ns

74153, LS153, S153 Multiplexers

Dual 4-Line To 1-Line Multiplexer
Product Specification

Logic Products

FEATURES

- Non-inverting outputs
- Separate enable for each section
- Common select inputs
- See '253 for 3-state version

DESCRIPTION

The '153 is a dual 4-input multiplexer that can select 2 bits of data from up to eight (8) sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables (\bar{E}_a, \bar{E}_b) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables (\bar{E}_a, \bar{E}_b) are HIGH.

$$Y_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74153	18ns	36mA
74LS153	18ns	6.2mA
74S153	9ns	45mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74153N, N74LS153N, N74S153N
Plastic SO	N74LS153D, N74S153D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

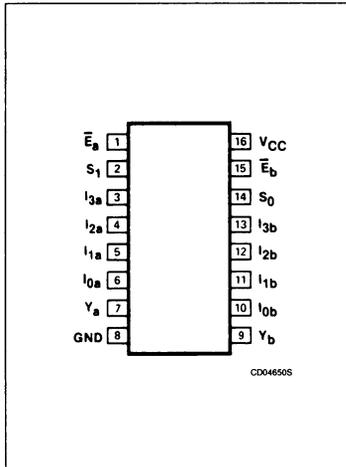
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

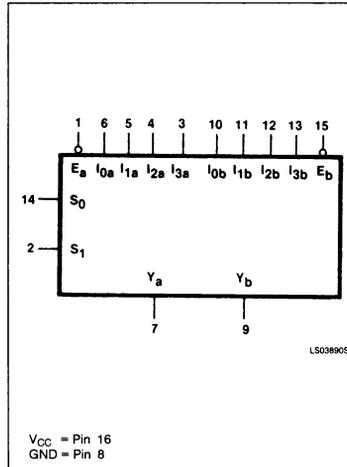
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

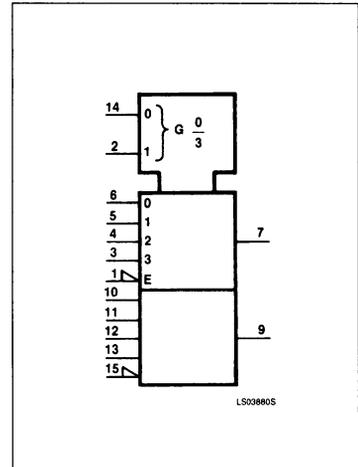
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

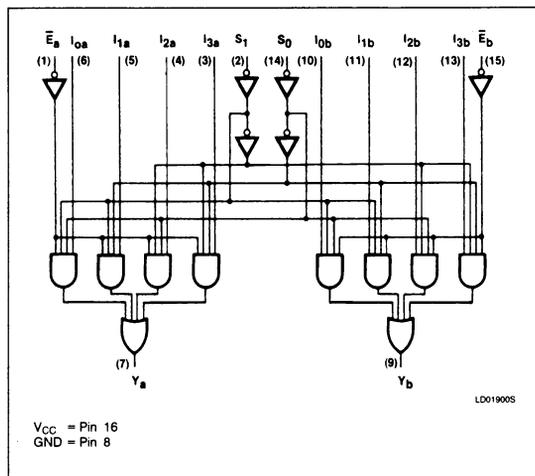


Multiplexers

74153, LS153, S153

The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S ₀	S ₁	\bar{E}	I ₀	I ₁	I ₂	I ₃	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

Multiplexers

74153, LS153, S153

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74153			74LS153			74S153			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4			V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5		-1.2	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA
		V _I = 7.0V					0.1				mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40						μA
		V _I = 2.7V					20		50		μA
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA
		V _I = 0.5V							-2.0		mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-57	-20		-100	-40		-100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		36	60		6.2	10		45	70	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all inputs grounded and all outputs open.

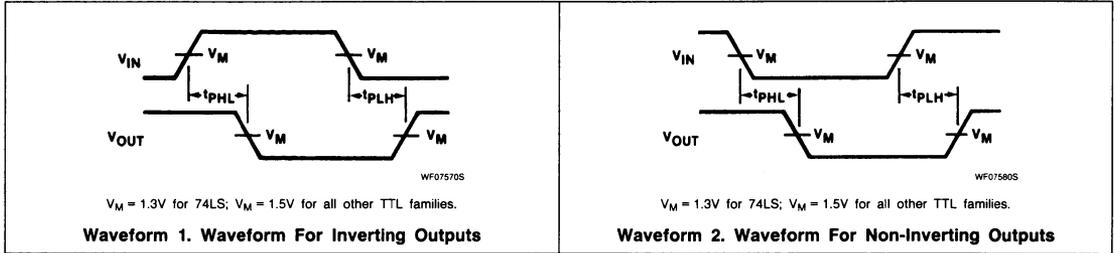
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 30pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay		34		29		18	ns
t _{PHL}	Select to output		34		38		18	
t _{PLH}	Propagation delay		30		24		15	ns
t _{PHL}	Enable to output		23		32		13.5	
t _{PLH}	Propagation delay		18		15		9.0	ns
t _{PHL}	Data to output		23		26		9.0	

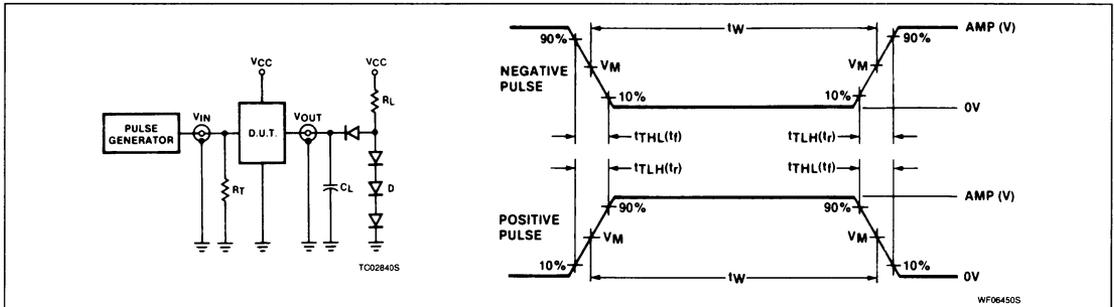
Multiplexers

74153, LS153, S153

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74154, LS154

Decoder/Demultiplexers

1-of-16 Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES

- 16-line demultiplexing capability
- Mutually exclusive outputs
- 2-input enable gate for strobing or expansion

DESCRIPTION

The '154 decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'd inputs which must be LOW to enable the outputs.

The '154 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74154	21ns	34mA
74LS154	15ns	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74154N, N74LS154N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

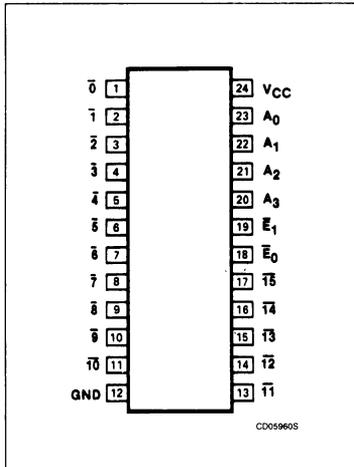
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	10LSuI

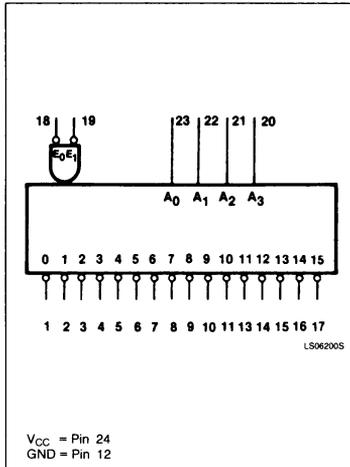
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

PIN CONFIGURATION

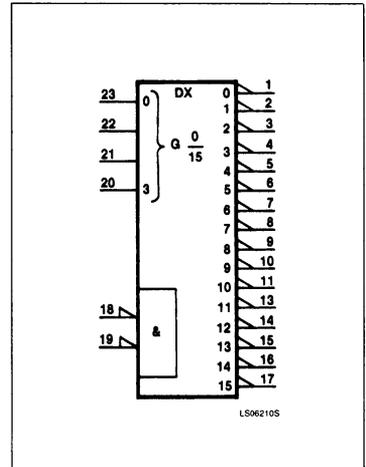


LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

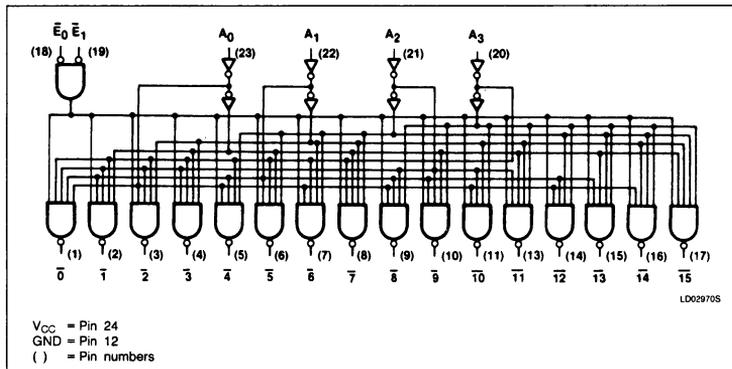
LOGIC SYMBOL (IEEE/IEC)



Decoder/Demultiplexers

74154, LS154

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUT																	
E ₀	E ₁	A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

Decoder/Demultiplexers

74154, LS154

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74154			74LS154			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0				mA
		V _I = 7.0V					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40				μA
		V _I = 2.7V					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-15		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		34	56		9	14	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all inputs grounded and all outputs open.

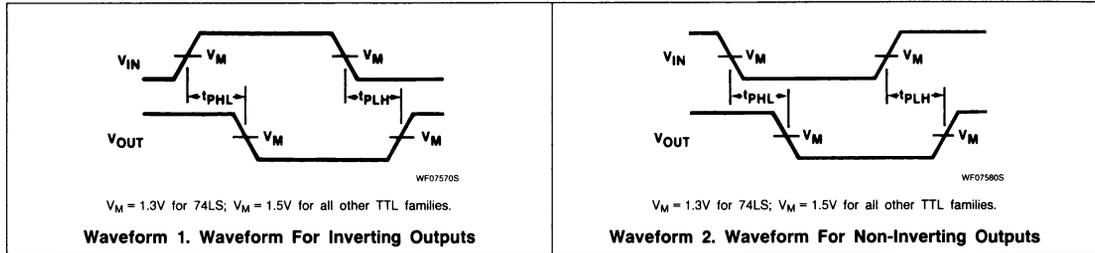
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Address to output Waveform 1		36 33		36 33	ns
t _{PLH} t _{PHL}	Propagation delay Enable to output Waveform 2		30 27		30 27	ns

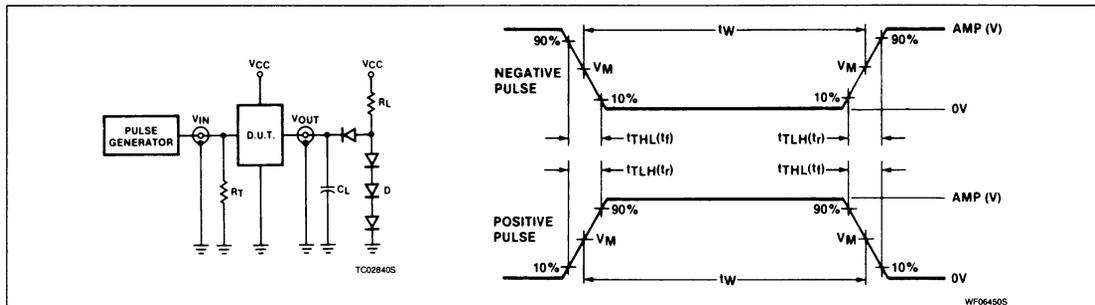
Decoder/Demultiplexers

74154, LS154

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74155, LS155

Decoders/Demultiplexers

Dual 2-Line To 4-Line Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES

- Common Address Inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications

DESCRIPTION

The '155 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address input (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\bar{0} - \bar{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74155	18ns	25mA
74LS155	17ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74155N, N74LS155N
Plastic SO	N74LS155D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

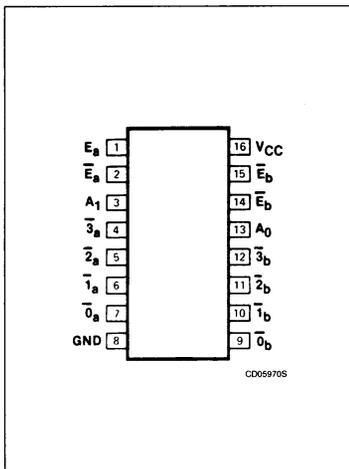
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	10LSuI

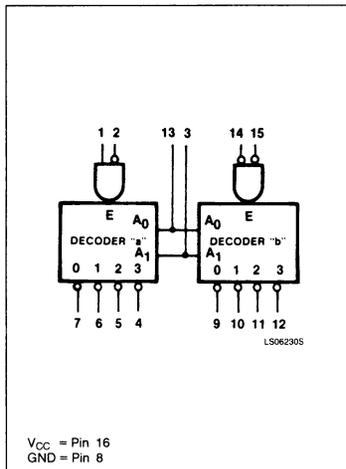
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

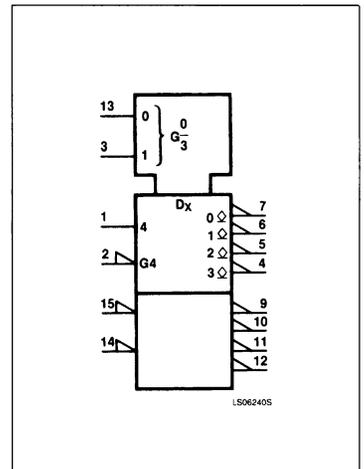
PIN CONFIGURATION



LOGIC SYMBOL



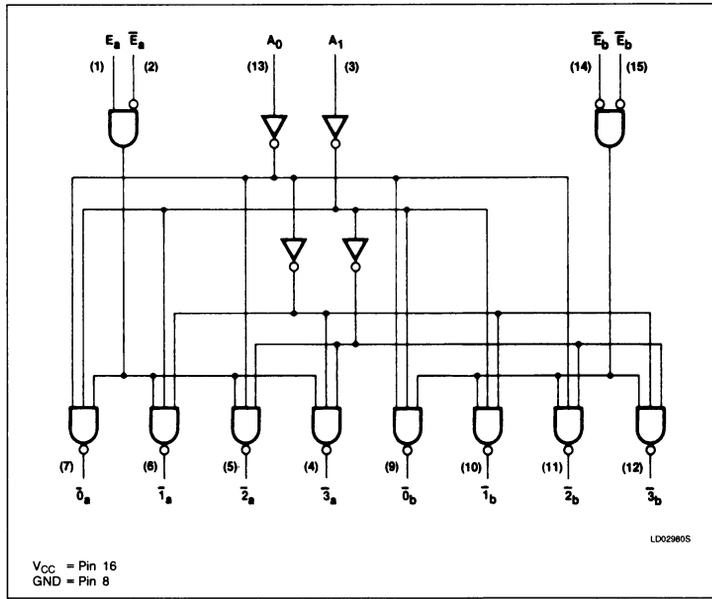
LOGIC SYMBOL (IEEE/IEC)



Decoders/Demultiplexers

74155, LS155

LOGIC DIAGRAM



Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \bar{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the \bar{E}_a or E_a inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\bar{E}_b \cdot \bar{E}_b$). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to \bar{E}_b and relabeling the common enable by connecting the remaining \bar{E}_b and \bar{E}_a .

FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	\bar{E}_a	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	\bar{E}_b	\bar{E}_b	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

Decoders/Demultiplexers

74155, LS155

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-800			-400	μA
I _{OL}	LOW-level output current			16			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74155			74LS155			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA
		V _I = 7.0V					0.1	mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40			μA
		V _I = 2.7V					20	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-57	-15		-100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		25	40		6.1	10	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with A₁, A₀ and E_a inputs at 4.5V, and E_b, E_a inputs grounded, and outputs open.

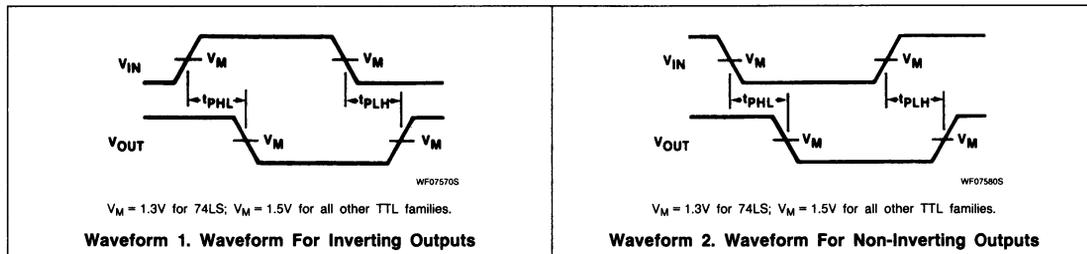
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Address to output Waveform 1		32 32		26 30	ns
t _{PLH} t _{PHL}	Propagation delay E _a or E _b to output Waveform 2		20 27		15 30	ns
t _{PLH} t _{PHL}	Propagation delay E _a to output Waveform 1		24 30		27 27	ns

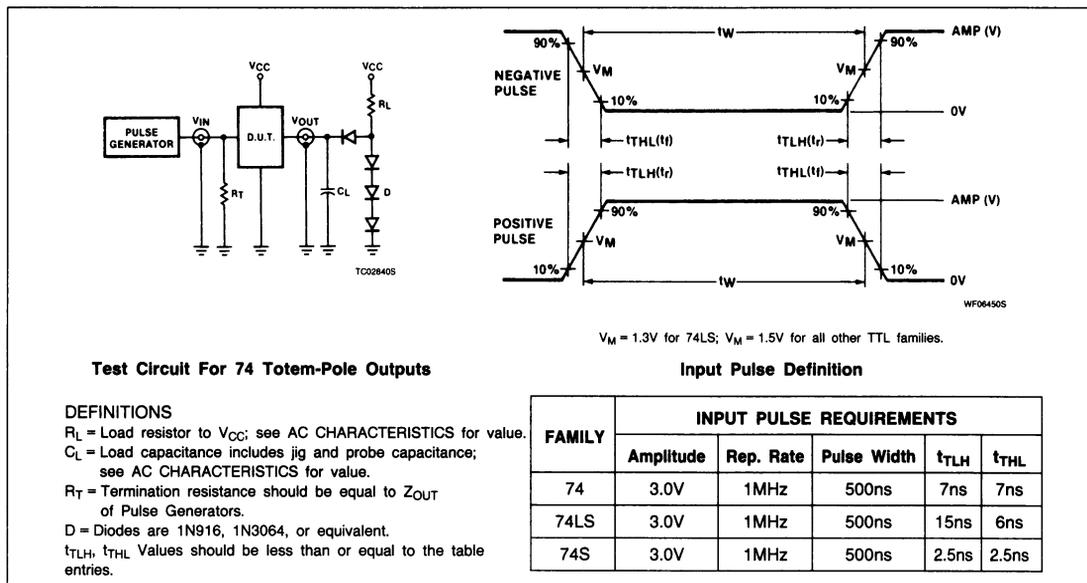
Decoders/Demultiplexers

74155, LS155

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74156, LS156

Decoders/Demultiplexers

Dual 2-Line To 4-Line Decoder/Demultiplexer (Open Collector)
Product Specification

Logic Products

FEATURES

- Common Address inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications
- Outputs can be tied together

DESCRIPTION

The '156 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address inputs (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\bar{0} - \bar{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74156	20ns	25mA
74LS156	31ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74156N, N74LS156N
Plastic SO	N74LS156D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

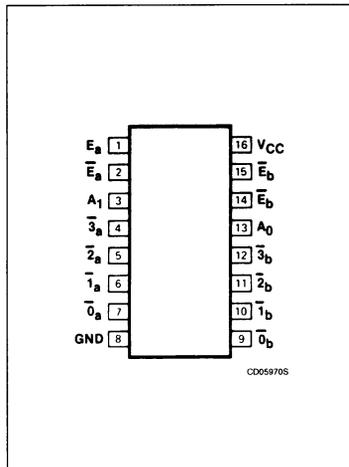
PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE:

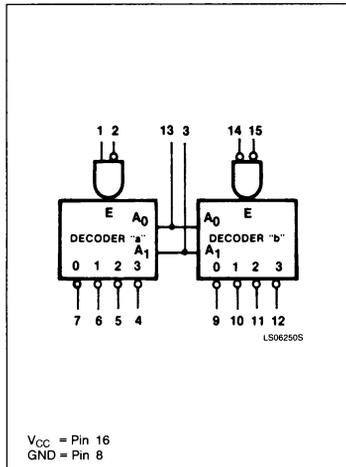
Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

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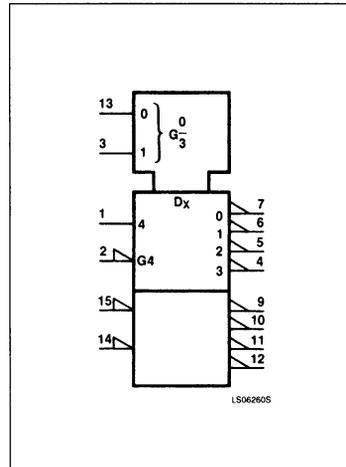
PIN CONFIGURATION



LOGIC SYMBOL



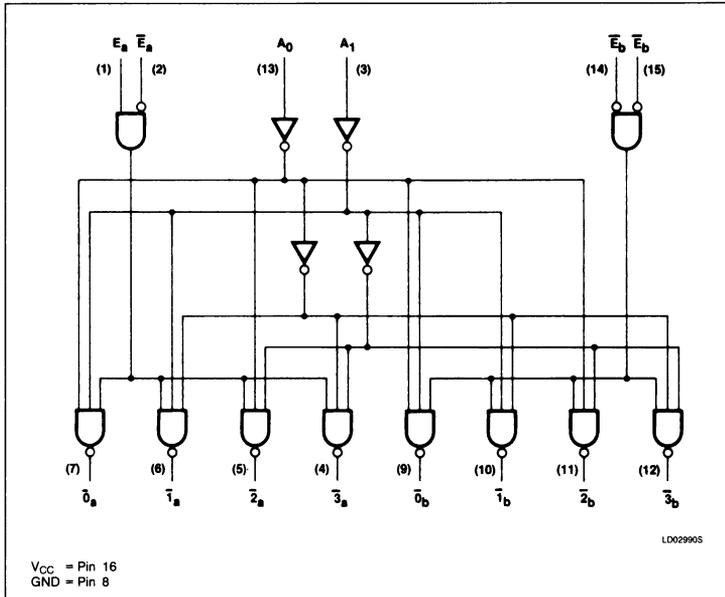
LOGIC SYMBOL (IEEE/IEC)



Decoders/Demultiplexers

74156, LS156

LOGIC DIAGRAM



Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \bar{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the \bar{E}_a or E_a inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\bar{E}_b \cdot \bar{E}_b$). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to \bar{E}_b and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining \bar{E}_b and \bar{E}_a .

The '156 can be used to generate all four minterms of two variables. The four minterms are useful to replace multiple gate functions in some applications. A further advantage of the '156 is being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown in the formula below:

$$f = (E + A_0 + A_1) \cdot (E + \bar{A}_0 + A_1) \cdot (E + A_0 + \bar{A}_1) \cdot (E + \bar{A}_0 + \bar{A}_1)$$

where $E = E_a + E_b$; $\bar{E} = \bar{E}_b + \bar{E}_a$.

FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	\bar{E}_a	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	\bar{E}_b	\bar{E}_b	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level

L = LOW voltage level

X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

Decoders/Demultiplexers

74156, LS156

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
V _{OH}	HIGH-level output voltage			5.5			5.5	V
I _{OL}	LOW-level output current			16			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74156			74LS156			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
I _{OH}	HIGH-level output current V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			250			100	μA
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA
		V _I = 7.0V					0.1	mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40			μA
		V _I = 2.7V					20	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{CC}	Supply current ³ (total) V _{CC} = MAX		25	40		6.1	10	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Measure I_{CC} with A₁, A₀ and E_a inputs at 4.5V, and E_b, E_a inputs grounded, and outputs open.

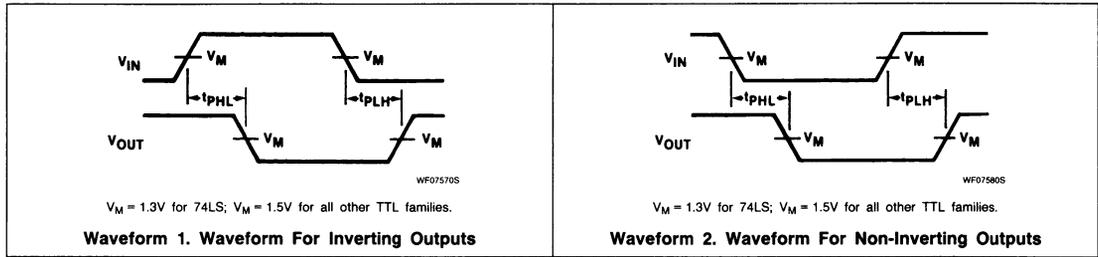
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Address to output Waveform 1		34 34		46 51	ns
t _{PLH} t _{PHL}	Propagation delay E _a or E _b to output Waveform 2		23 30		40 51	ns
t _{PLH} t _{PHL}	Propagation delay E _a to output Waveform 1		27 33		48 48	ns

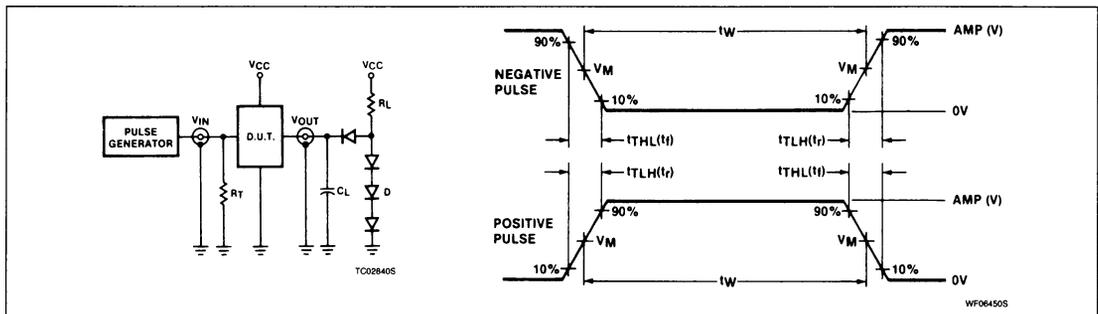
Decoders/Demultiplexers

74156, LS156

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74157, 74158, LS157, LS158, S157, S158 Data Selectors/Multiplexers

Logic Products

DESCRIPTION

The '157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the '157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

'157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
'158 Quad 2-Input Data Selector/Multiplexer (Inverted)

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74157	13ns	30mA
74LS157	13ns	9.7mA
74S157	7.4ns	50mA
74158	13ns	30mA
74LS158	13ns	4.8mA
74S158	6ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74157N, N74LS158N, N74S157N N74LS157N, N74S158N, N74LS158N
Plastic SO	N74LS157D, N74S158D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

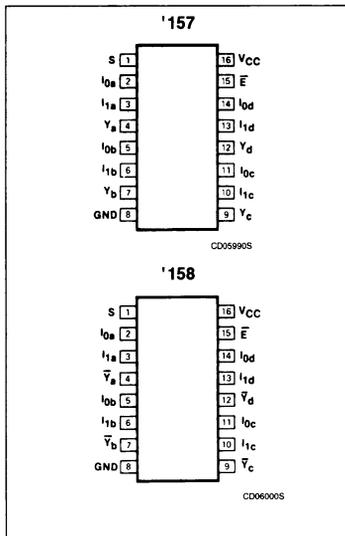
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
S, \bar{E}	Inputs	1ul	2Sul	2LSul
Data	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

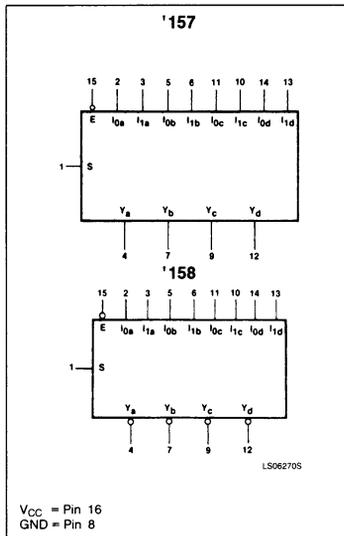
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

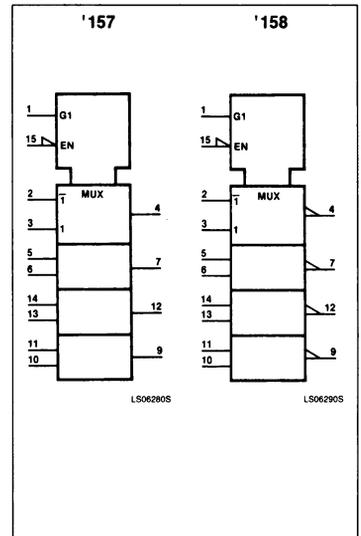
PIN CONFIGURATION



LOGIC SYMBOL



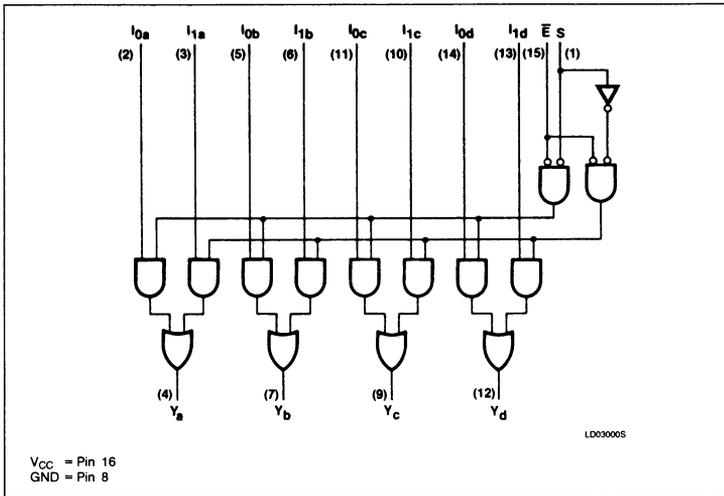
LOGIC SYMBOL (IEEE/IEC)



Data Selectors/Multiplexers

74157, 74158, LS157, LS158, S157, S158

LOGIC DIAGRAM, '157



The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Y_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Y_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Y_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

The '158 is similar but has inverting outputs:

$$\bar{Y}_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$\bar{Y}_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$\bar{Y}_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$\bar{Y}_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

FUNCTION TABLE, '157

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
		I_0	I_1	
\bar{E}	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level

L = LOW voltage level

X = Don't care

FUNCTION TABLE, '158

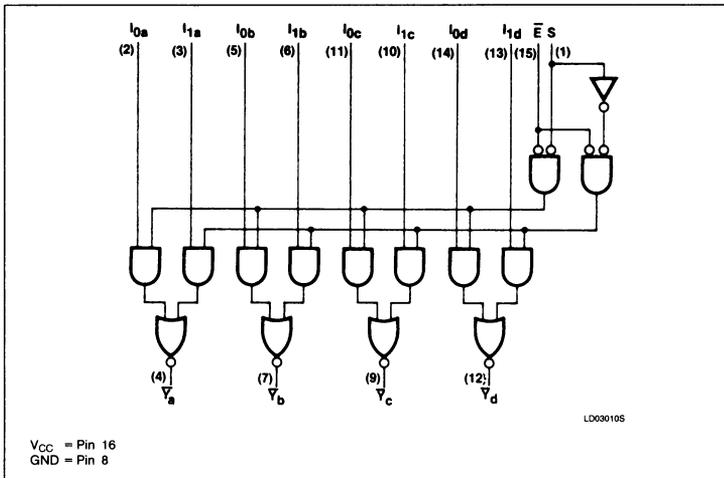
ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
		I_0	I_1	
\bar{E}	S	I_0	I_1	\bar{Y}
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level

L = LOW voltage level

X = Don't care

LOGIC DIAGRAM, '158



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70			°C

Data Selectors/Multiplexers

74157, 74158, LS157, LS158, S157, S158

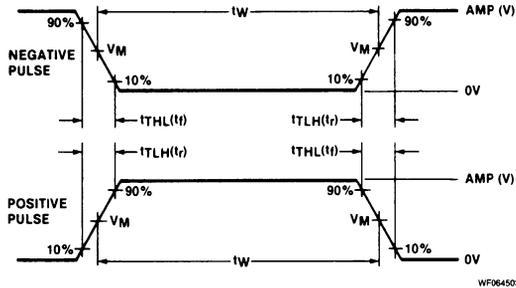
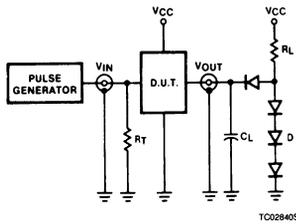
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

NOTE:

V_{IL} = +0.7V MAX for 54S at +125°C only.

TEST CIRCUITS AND WAVEFORMS



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Data Selectors/Multiplexers

74157, 74158, LS157, LS158, S157, S158

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74157, 158			74LS157, 158			74S157, 158			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5			0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4				V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA	
		V _I = 7.0V	S, E inputs					0.2					mA
			Data inputs					0.1					mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	S, E inputs		40							μA	
			Data inputs		40							μA	
		V _I = 2.7V	S, E inputs					40			100	μA	
			Data inputs					20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	S, E inputs		-1.6			-0.8				mA	
			Data inputs		-1.6			-0.4				mA	
		V _I = 0.5V	S, E inputs								-4	mA	
			Data inputs								-2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-55	-20		-100	-40		-100	mA	
I _{CC} Supply current ^{4, 5} (total)	V _{CC} = MAX	Note 4	'157 '158	30	48							mA	
		Note 4	'LS157				9.7	16				mA	
		Note 4	'LS158				4.8	8				mA	
		Note 5	'S157 All inputs = 4.5V							50	78	mA	
		Note 5	'S158 All inputs = 4.5V							39	61	mA	
		Note 5	'S158 I _{oa} , I _{ob} , I _{oc} , I _{od} at 4.5V, other inputs at 0V							41	81	mA	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

5. I_{CC} is measured with all outputs open.

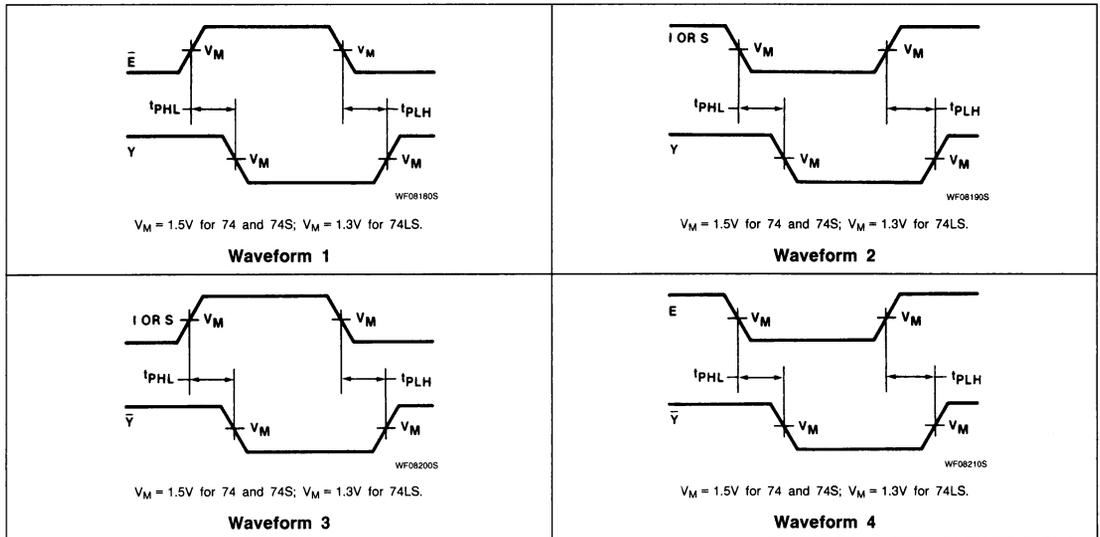
Data Selectors/Multiplexers

74157, 74158, LS157, LS158, S157, S158

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay Data to output	Waveform 2, '157		14 14	14 14	7.5 6.5	ns		
t_{PLH} t_{PHL} Propagation delay Enable to output	Waveform 1, '157		20 21	20 21	12.5 12	ns		
t_{PLH} t_{PHL} Propagation delay Select to output	Waveform 2, '157		23 27	23 27	15 15	ns		
t_{PLH} t_{PHL} Propagation delay Data to output	Waveform 3, '158		14 14	12 15	6.0 6.0	ns		
t_{PLH} t_{PHL} Propagation delay Enable to output	Waveform 4, '158		20 21	17 24	11.5 12	ns		
t_{PLH} t_{PHL} Propagation delay Select to output	Waveform 3, '158		23 27	20 24	12 12	ns		

AC WAVEFORMS



5

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A Counters

Logic Products

'160, '162 BCD Decade Counter
'161, '163 4-Bit Binary Counter
Product Specification

FEATURES

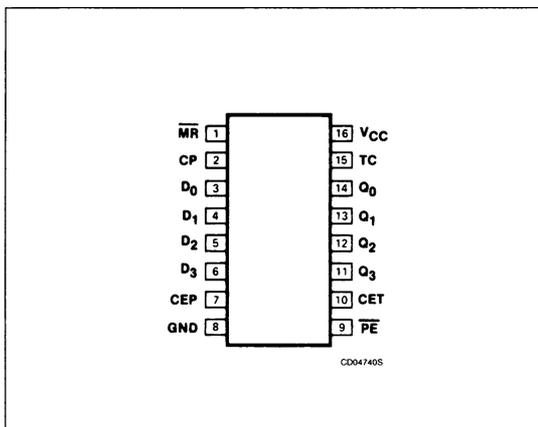
- Synchronous counting and loading
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset ('160, '161)
- Synchronous reset ('162, '163)
- Hysteresis on Clock input (LS only)

DESCRIPTION

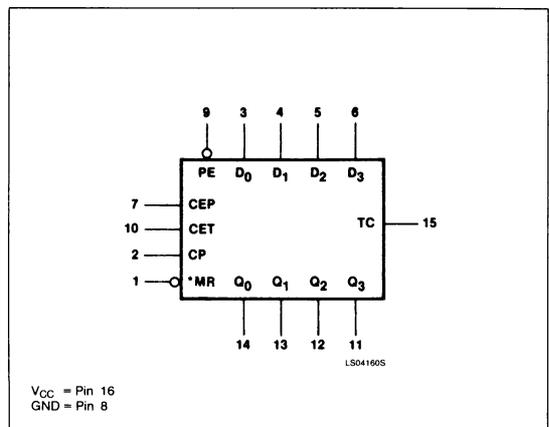
Synchronous presettable decade (74160, 74LS160A, 74LS162A) and 4-bit (74161, 74LS161A, 74163, 74LS163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to HIGH or LOW level. A LOW level at the Parallel Enable (\overline{PE}) input disables the counting action and causes the data at the $D_0 - D_3$ inputs to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold requirements for \overline{PE} are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

PIN CONFIGURATION



LOGIC SYMBOL



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74160 - 74163	32MHz	61mA
74LS160A - 74LS163A	32MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74160N, N74LS160AN, N74161N, N74LS161AN N74LS162AN, N74163N, N74LS163AN
Plastic SO	N74LS161AD, N74S163AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
CP, CET	Inputs	2ul	2LSul
D, CEP	Inputs	1ul	1LSul
\overline{PE}	Input	1ul	2LSul
All	Outputs	10ul	10LSul
\overline{MR}	Input ('160, '161)	1ul	1LSul
\overline{MR}	Input ('162, '163)	1ul	2LSul

NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

A LOW level at the Master Reset (\overline{MR}) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) in '160, 'LS160A, '161, and 'LS161A to LOW levels regardless of the levels at CP, \overline{PE} , CET and CEP inputs (thus providing an asynchronous clear function).

For the 'LS162A, '163, and LS163A, the clear function is synchronous. A LOW level at the Master Reset (\overline{MR}) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) to LOW levels after the next positive-going transition on the Clock (CP) input (providing that the set-up and hold requirements for \overline{MR} are met). This action occurs regardless of the levels at \overline{PE} , CET, and CEP inputs. This synchronous reset fea-

ture enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to the HIGH level output of Q_0 . This pulse can be used to enable the next cascaded stage (see Figure B).

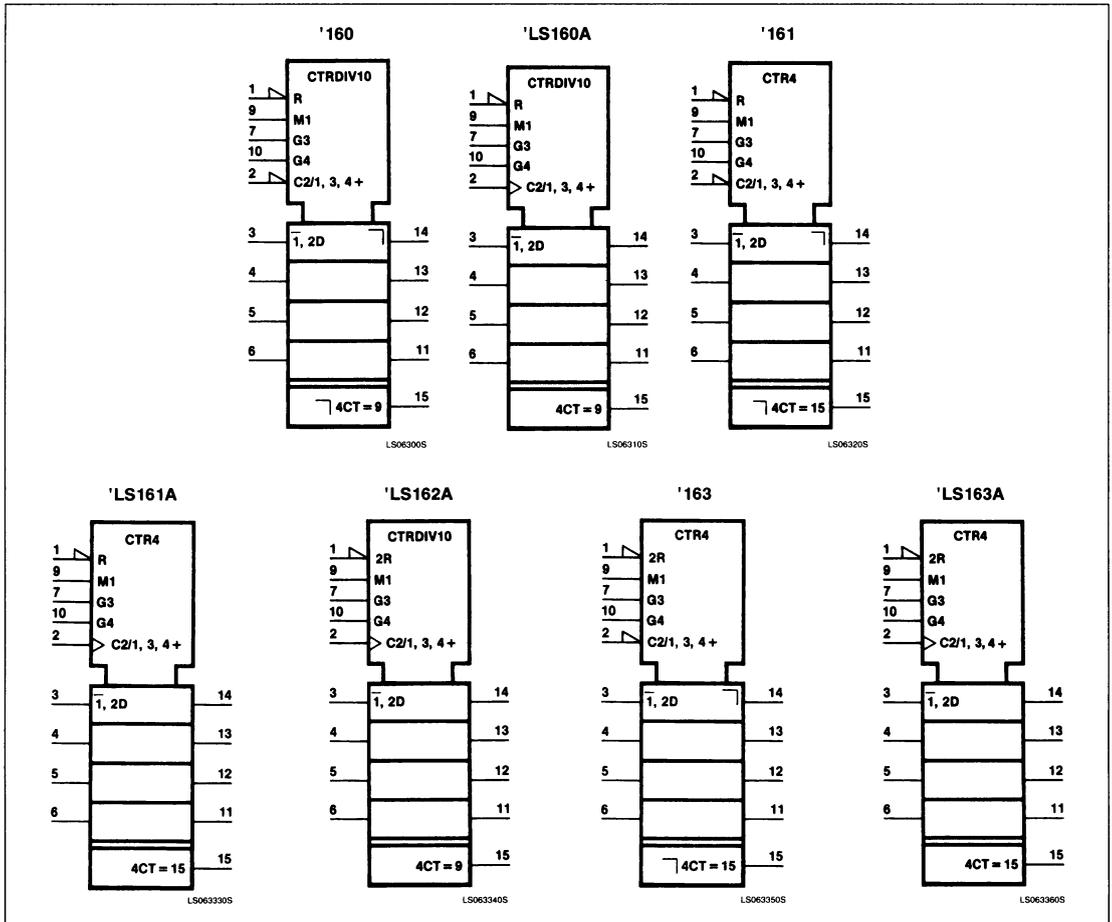
For conventional operation of 74160, 74161 and 74163, the following transitions should be avoided.

1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables and \overline{MR} are HIGH at or before the transition.
3. LOW-to-HIGH transition on the \overline{MR} input when clock is LOW, if the Enable and \overline{PE} inputs are HIGH at or before the transition.

For 74163 there is an additional transition to be avoided.

These restrictions are not applicable to 74LS160A, 74LS161A, 74LS162A and 74LS163A.

LOGIC SYMBOL (IEEE/IEC)



Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

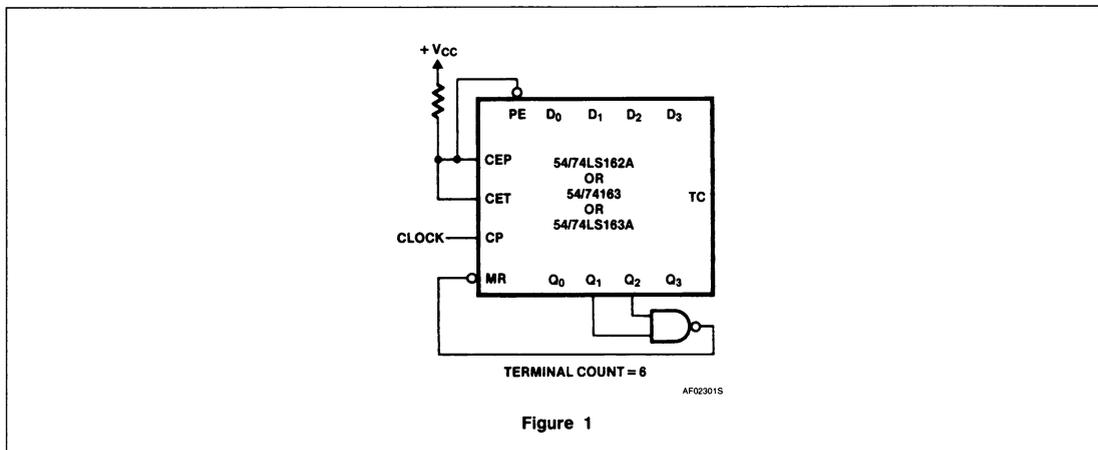


Figure 1

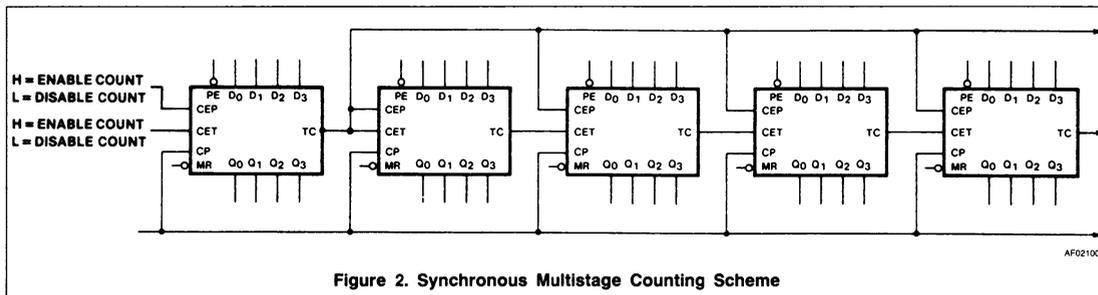
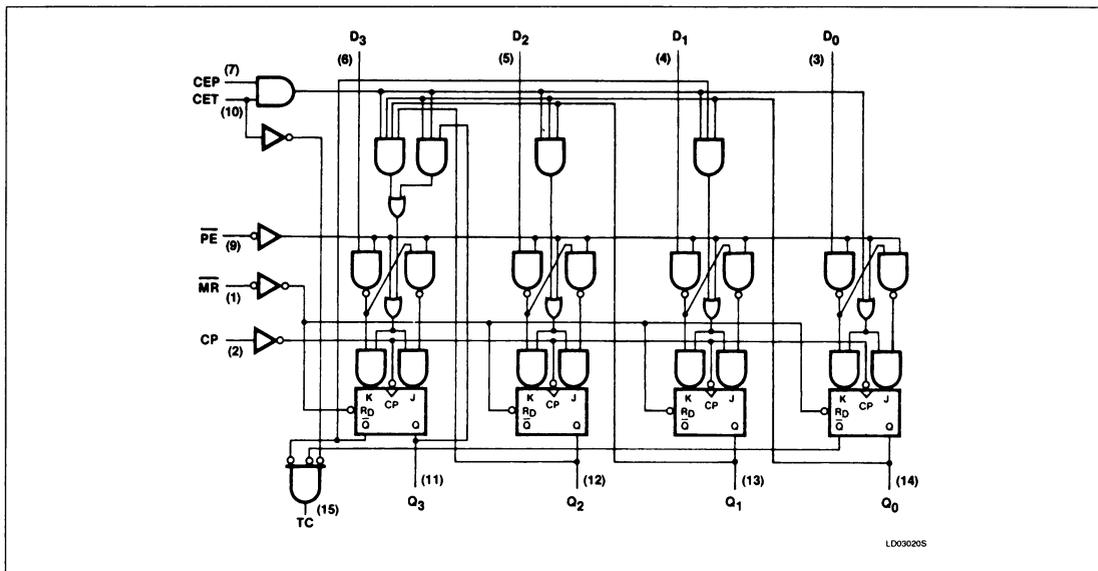


Figure 2. Synchronous Multistage Counting Scheme

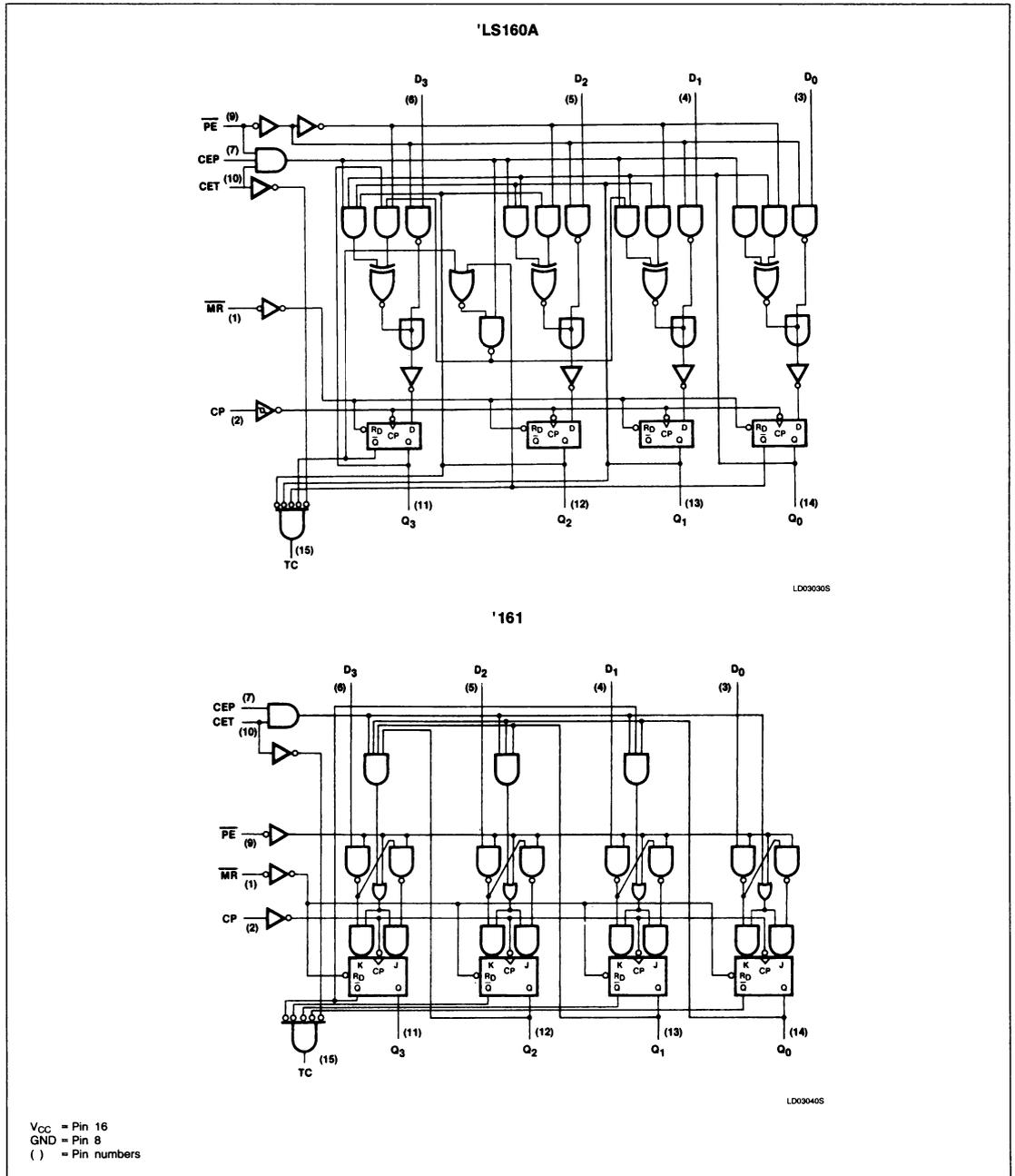
LOGIC DIAGRAM, 74160



Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS



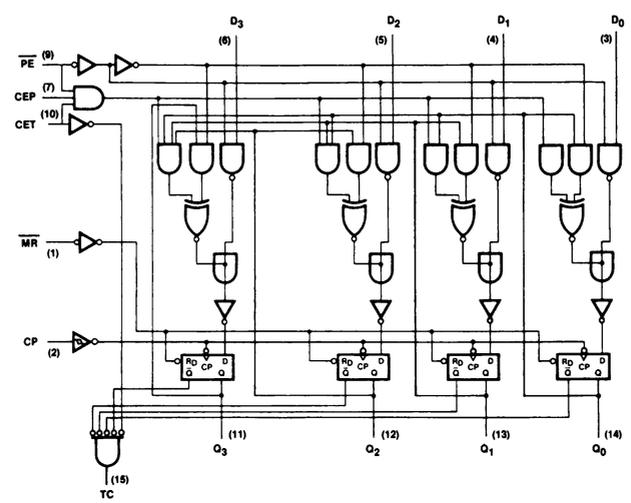
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Counters

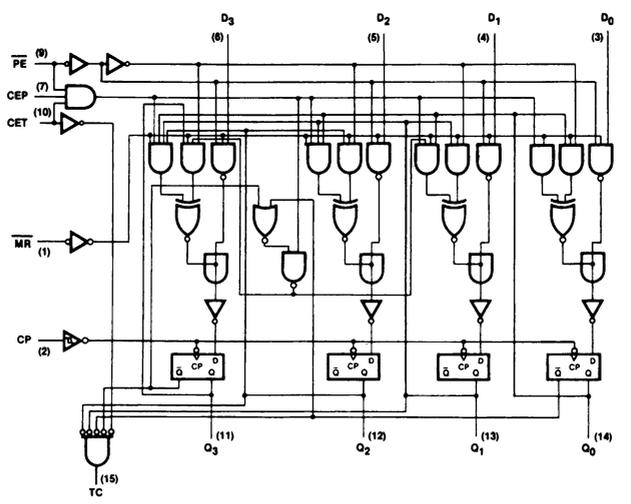
74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS

'LS161A



'LS162A

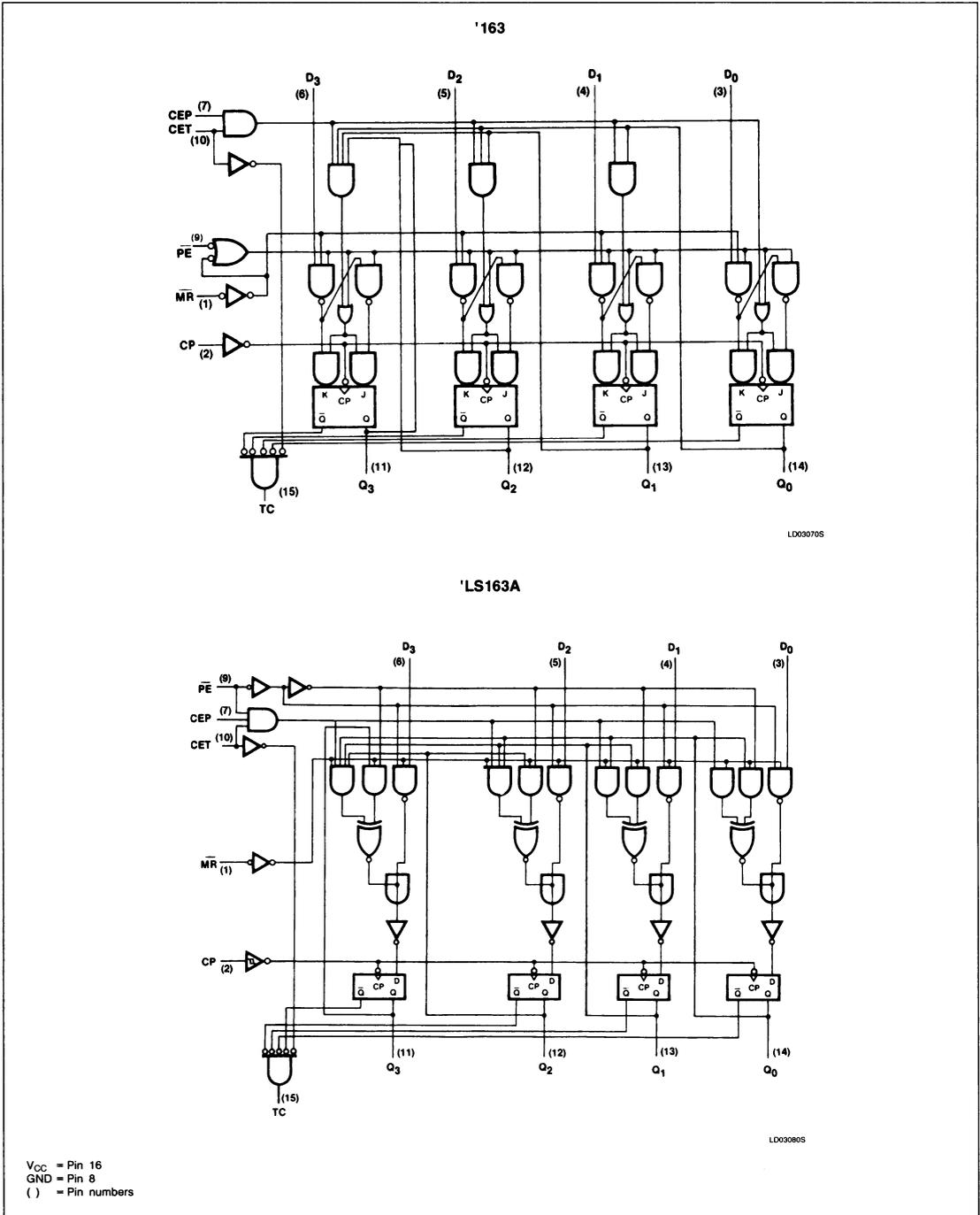


V_{CC} = Pin 16
 GND = Pin 8
 () = Pin numbers

Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS



Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

MODE SELECT — FUNCTION TABLE, '160, '161

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	\uparrow	X	X	l	l	L	L
	H	\uparrow	X	X	l	h	H	(a)
Count	H	\uparrow	h	h	$h^{(c)}$	X	count	(a)
Hold (do nothing)	H	X	$l^{(b)}$	X	$h^{(c)}$	X	q_n	(a)
	H	X	X	$l^{(b)}$	$h^{(c)}$	X	q_n	L

MODE SELECT — FUNCTION TABLE, '162, '163

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (clear)	l	\uparrow	X	X	X	X	L	L
Parallel load	$h^{(f)}$	\uparrow	X	X	l	l	L	L
	$h^{(f)}$	\uparrow	X	X	l	h	H	(d)
Count	$h^{(f)}$	\uparrow	h	h	$h^{(f)}$	X	count	(d)
Hold (do nothing)	$h^{(f)}$	X	$l^{(e)}$	X	$h^{(f)}$	X	q_n	(d)
	$h^{(f)}$	X	X	$l^{(e)}$	$h^{(f)}$	X	q_n	L

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

X = Don't care.

q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

\uparrow = LOW-to-HIGH clock transition.

NOTES:

(a) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for '161 and HLLH for '160).

(b) The HIGH-to-LOW transition of CEP or CET on the 74161 and 74160 should only occur while CP is HIGH for conventional operation.

(c) The LOW-to-HIGH transition of \overline{PE} on the 74161 and 74160 should only occur while CP is HIGH for conventional operation.

(d) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for '162 and HHHH for '163).

(e) The HIGH-to-LOW transition of CEP or CET on the 74163 should only occur while CP is HIGH for conventional operation.

(f) The LOW-to-HIGH transition of \overline{PE} or \overline{MR} on the 74163 should only occur while CP is HIGH for conventional operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

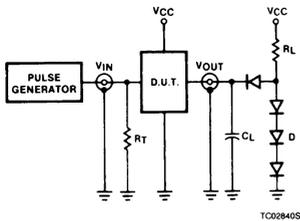
Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

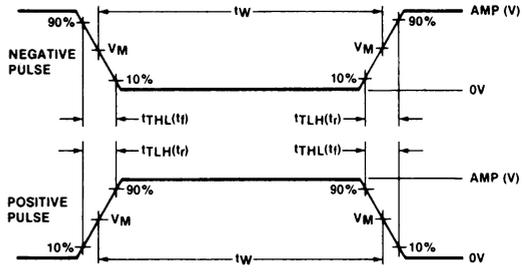
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



TC02840S



WF06450S

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Counters 74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74160, '161 '163			74LS160A, '161A '162A, '163A			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA
		V _I = 7.0V	D, CEP				0.1	mA
			PE, CP, CET				0.2	mA
			MR, ('LS160A, 'LS161A)				0.1	mA
			MR ('LS162A, 'LS163A)				0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	CP, CET		80			μA
			Other inputs		40			μA
		V _I = 2.7V	D, CEP				20	μA
			PE, CP, CET				40	μA
			MR ('LS160A, 'LS161A)				20	μA
			MR ('LS162A, 'LS163A)				40	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	CP, CET		-3.2			mA
			Other inputs		-1.6			mA
		V _I = 0.4V	D, CEP				-0.4	mA
			PE, CP, CET				-0.8	mA
			MR ('LS160A, 'LS161A)				-0.4	mA
			MR ('LS162A, 'LS163)				-0.8	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	I _{CC} H All outputs HIGH		59	94	18	31	mA
		I _{CC} L All outputs LOW		63	101	19	32	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX+0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC}H is measured with PE input HIGH, again with PE input LOW, all other inputs HIGH and outputs open. I_{CC}L is measured with Clock input HIGH, again with Clock input LOW, all other inputs low and outputs open.

Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2k\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to terminal count	Waveform 1		35 35		35 35	ns
t_{PLH} Propagation delay t_{PHL} Clock to Q outputs	Waveform 1, PE = HIGH		20 23		24 27	ns
t_{PLH} Propagation delay t_{PHL} Clock to Q outputs	Waveform 1, PE = LOW		25 29		24 27	ns
t_{PLH} Propagation delay t_{PHL} CET input to TC output	Waveform 2		16 16		14 14	ns
t_{PHL} Propagation delay, \overline{MR} to Q outputs ('160, '161)	Waveform 3		38		28	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	25		25		ns
t_W Master Reset pulse width ('160, '161)	Waveform 3	20		20		ns
t_W Master Reset pulse width ('162, '163)	Waveform 6	20		20		ns
t_s Set-up time, data to clock	Waveform 5	20		20		ns
t_h Hold time, data to clock ¹	Waveform 5	3		3		ns
t_s Set-up time, CEP or CET to clock	Waveform 4	20		20		ns
t_h Hold time, CEP or CET to clock	Waveform 4	0		0		ns
t_s Set-up time, \overline{PE} to clock	Waveform 5	25		20		ns
t_h Hold time, \overline{PE} to clock	Waveform 5	0		0		ns
t_s Set-up time, \overline{MR} to clock ('162, '163)	Waveform 6	20		20		ns
t_h Hold time, \overline{MR} to clock ('162, '163)	Waveform 6	0		0		ns
t_{rec} Recovery time, \overline{MR} to CP	Waveform 3	25		15		ns

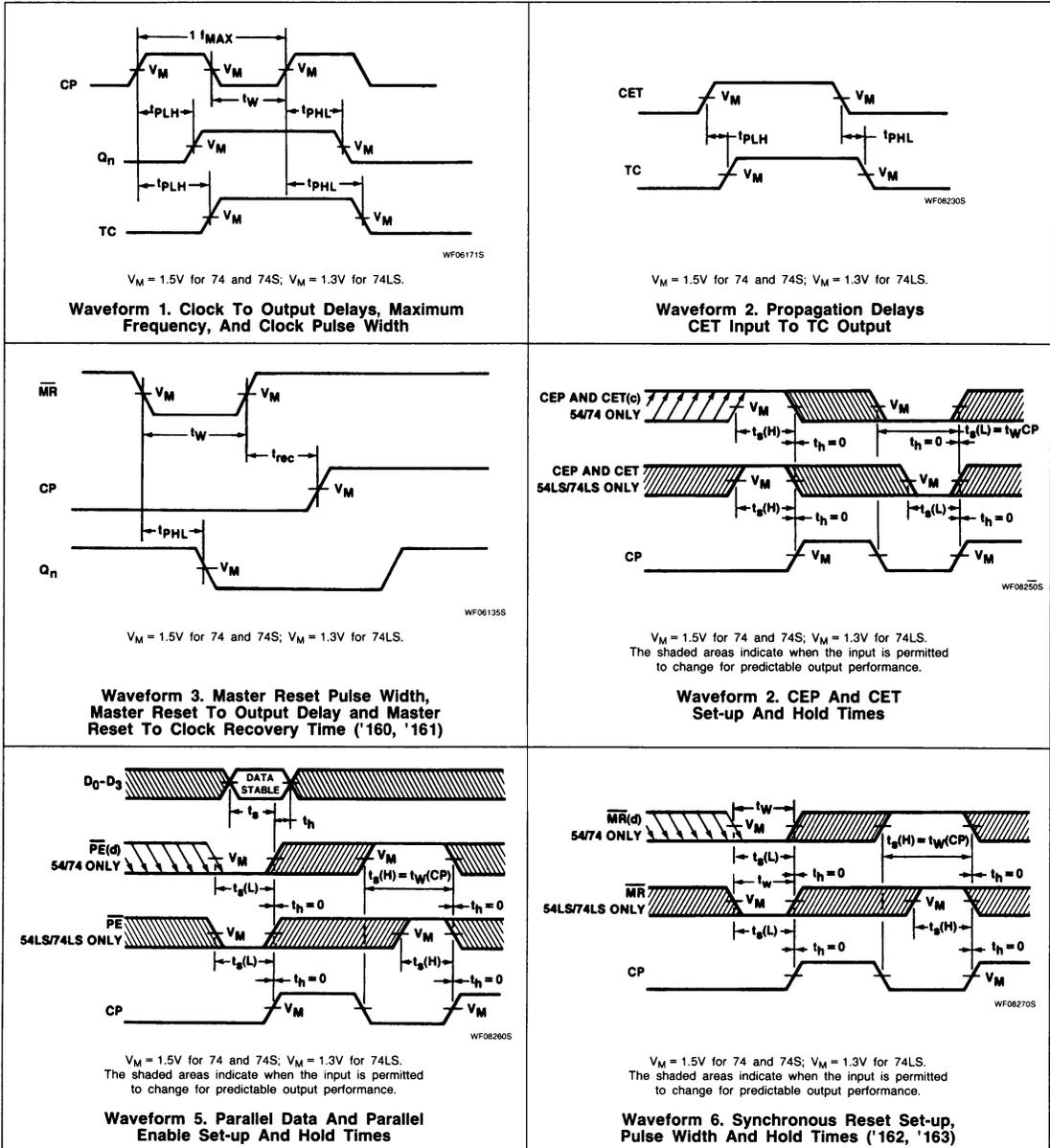
NOTE:

1. For 15ns rise time only, Hold time must be increased by 0.3ns for each nanosecond decrease in rise time.

Counters

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

AC WAVEFORMS



74164, LS164

Shift Registers

8-Bit Serial-In Parallel-Out Shift Register
Product Specification

Logic Products

FEATURES

- Gated serial Data inputs
- Typical shift frequency of 36MHz
- Asynchronous Master Reset
- Fully buffered Clock and Data inputs

DESCRIPTION

The '164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one set-up time before the rising clock edge. A LOW level on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74164	36MHz	37mA
74LS164	36MHz	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74164N, N74LS164N
Plastic SO	N74LS164D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

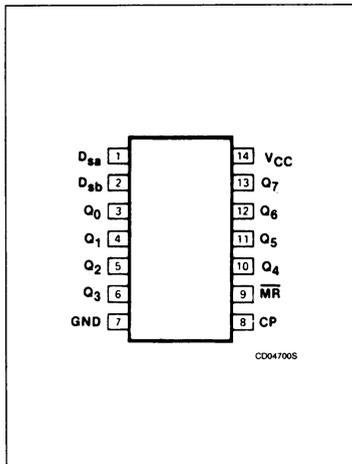
PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	5ul	10LSul

NOTE:

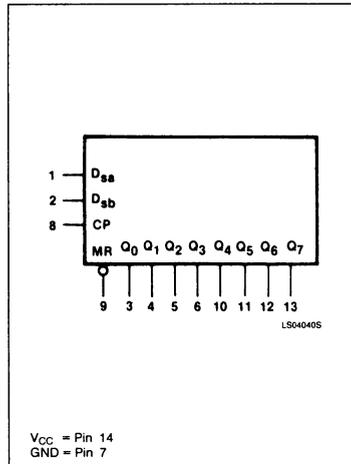
Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

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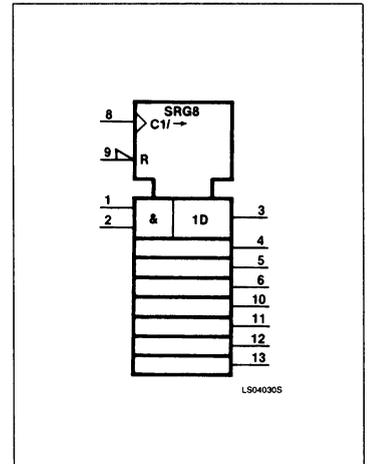
PIN CONFIGURATION



LOGIC SYMBOL



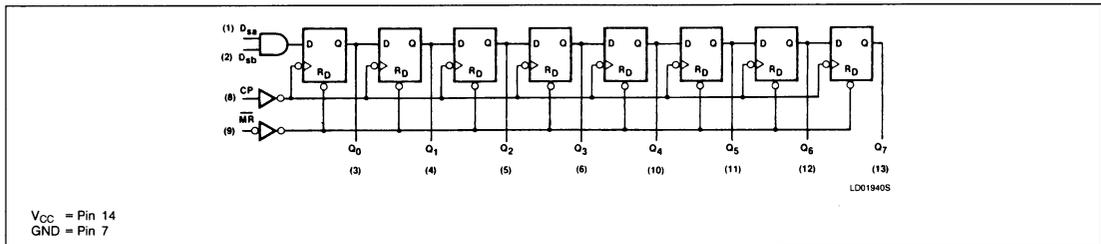
LOGIC SYMBOL (IEEE/IEC)



Shift Registers

74164, LS164

LOGIC DIAGRAM



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	MR	CP	D _{sa}	D _{sb}	Q ₀	Q ₁ — Q ₇	
Reset (clear)	L	X	X	X	L	L — L	
Shift	H	↑	l	l	L	q ₀ — q ₆	
	H	↑	l	h	L	q ₀ — q ₆	
	H	↑	h	l	L	q ₀ — q ₆	
	H	↑	h	h	H	q ₀ — q ₆	

- H = HIGH voltage level.
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
- q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH Clock transition.
- X = Don't care.
- ↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage				+0.8			V
I _{IK}	Input clamp current				-12			mA
I _{OH}	HIGH-level output current				-400			μA
I _{OL}	LOW-level output current				8			mA
T _A	Operating free-air temperature	0			70			°C

Shift Registers

74164, LS164

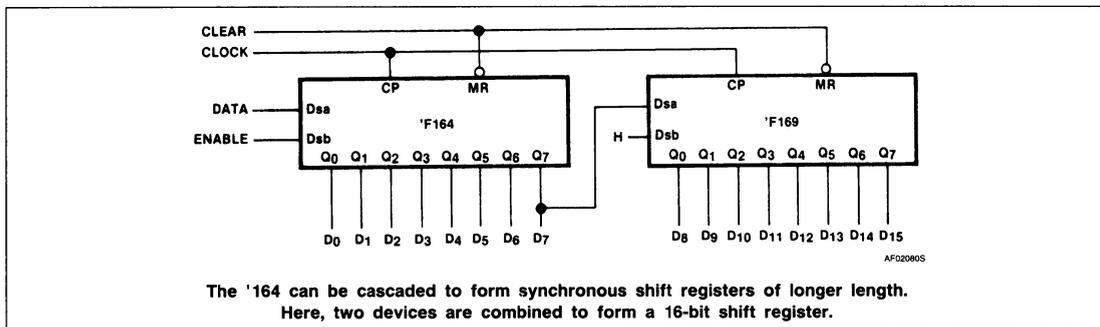
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74164			74LS164			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX I _{OH} = MAX	2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		0.2	0.4		0.35	0.5	V
						0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX			1.0				mA
							0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX			40				μA
							20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	9		-27.5	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		37	54		16	27	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION DIAGRAM



Shift Registers

74164, LS164

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 800\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum shift frequency	Waveform 1	25		25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		27 32		27 32	ns
t_{PHL} Propagation delay MR to output	Waveform 2		36		36	ns
t_{PLH} Propagation delay t_{PHL} Clock to output	$C_L = 50\text{pF}$ for these parameters	Waveform 1	30 37			ns
t_{PHL} Propagation delay MR to output		Waveform 2	42			ns

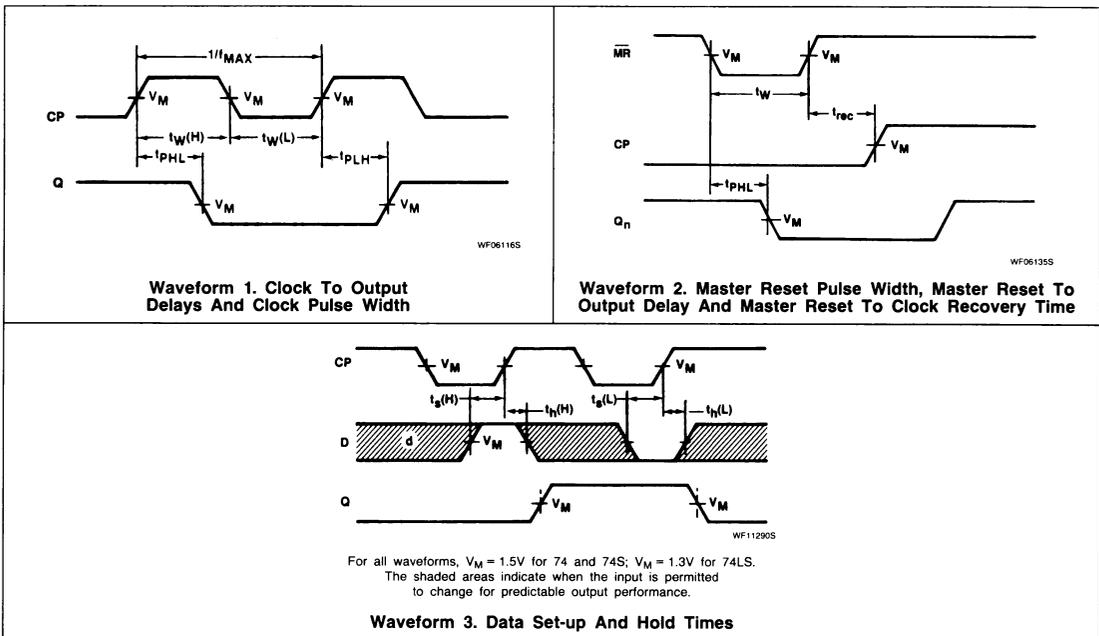
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W Clock pulse width	Waveform 1	20		20		ns
t_W MR pulse width	Waveform 2	20		20		ns
t_s Set-up time data to clock	Waveform 3	15		15		ns
t_h Hold time data to clock	Waveform 3	5.0		5.0		ns
t_{rec} MR to clock recovery time	Waveform 2	30		30		ns

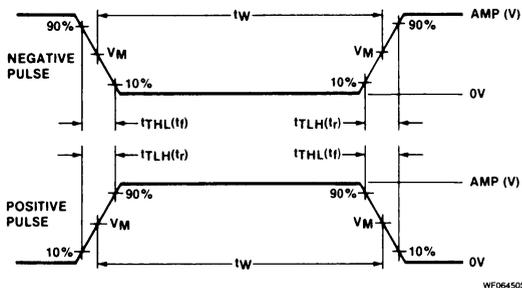
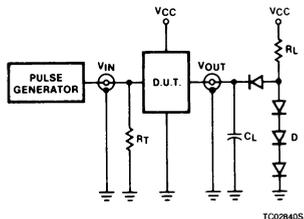
AC WAVEFORMS



Shift Registers

74164, LS164

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74165 Shift Register

8-Bit Serial/Parallel-In, Serial-Out Shift Register
Product Specification

Logic Products

- Asynchronous 8-bit parallel load
- Synchronous Serial input
- Clock Enable for "do nothing" mode
- See '166 for fully synchronous operation

DESCRIPTION

The '165 is an 8-bit parallel load or serial-in shift register with complementary Serial outputs (Q_7 and \bar{Q}_7) available from the last stage. When the Parallel Load ($\bar{P}L$) input is LOW, parallel data from the $D_0 - D_7$ inputs are loaded into the register asynchronously. When the $\bar{P}L$ input is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The Clock input is a gated-OR structure which allows one input to be used as an active LOW Clock Enable ($\bar{C}E$) input. The pin assignment for the CP and $\bar{C}E$

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74165	26MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74165N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
$\bar{P}L$	Input	2ul
Other	Inputs	1ul
All	Outputs	10ul

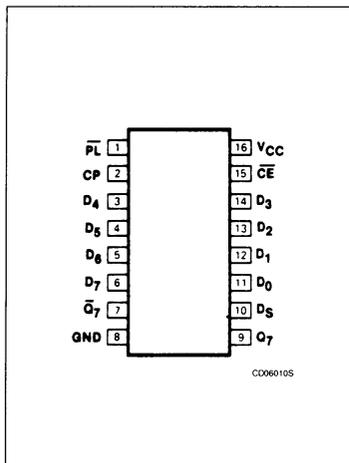
NOTE:

A 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

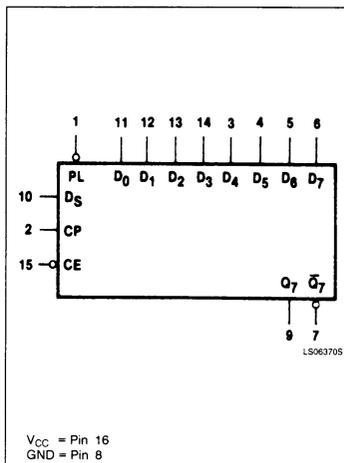
inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\bar{C}E$ input should only take place while the CP is HIGH for predictable operation. Also, the CP and

$\bar{C}E$ inputs should be LOW before the LOW-to-HIGH transition of $\bar{P}L$ to prevent shifting the data when $\bar{P}L$ is released.

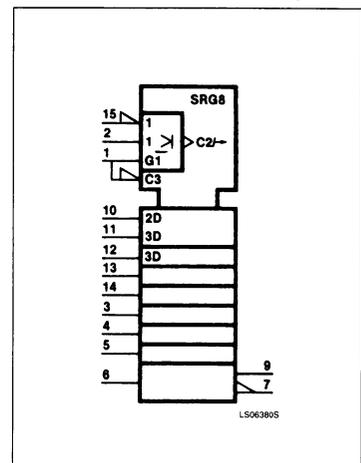
PIN CONFIGURATION



LOGIC SYMBOL



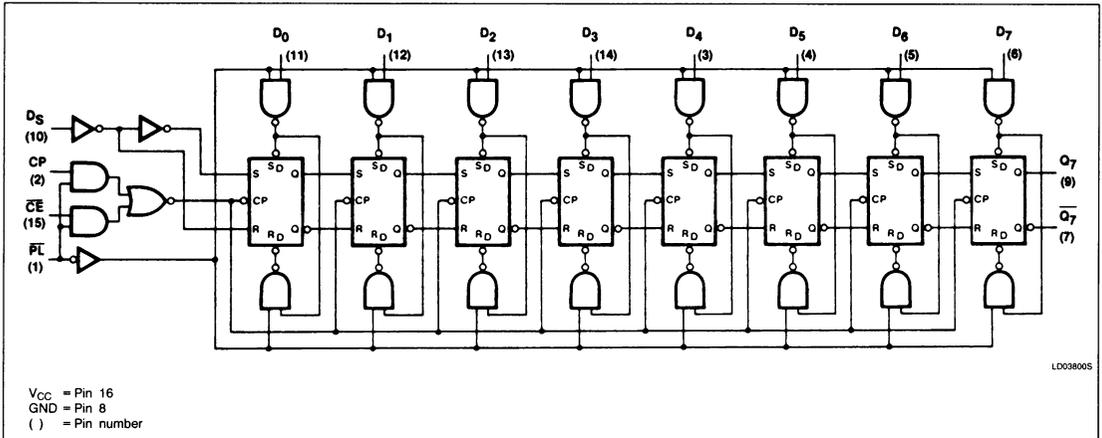
LOGIC SYMBOL (IEEE/IEC)



Shift Register

74165

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUTS	
	\overline{PL}	\overline{CE}	CP	D_S	$D_0 - D_7$	Q_0	$Q_1 - Q_6$	Q_7	$\overline{Q_7}$
Parallel load	L	X	X	X	L	L	L - L	L	H
	L	X	X	X	H	H	H - H	H	L
Serial shift	H	L	\uparrow	l	X	L	$q_0 - q_5$	q_6	$\overline{q_6}$
	H	L	\uparrow	h	X	H	$q_0 - q_5$	q_6	q_6
Hold "do nothing"	H	H	X	X	X	q_0	$q_1 - q_6$	q_7	$\overline{q_7}$

H = HIGH voltage level.

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

L = LOW voltage level.

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.

X = Don't care.

\uparrow = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70	°C

Shift Register

74165

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74165			UNIT
			Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OL} = MAX		0.2	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	PL input		80	μA
			Other inputs		40	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	PL input		-3.2	mA
			Other inputs		-1.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-18		-55	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX		42	63	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the outputs open, CE and CP at 4.5V, and a clock pulse applied to the PL input, I_{CC} is measured first with the Parallel Data inputs at 4.5V, then with the Parallel Data inputs grounded.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74		UNIT
			C _L = 15pF, R _L = 400Ω		
			Min	Max	
f _{MAX}	Maximum shift frequency	Waveform 1	20		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to output	Waveform 1		24 31	ns
t _{PLH} t _{PHL}	Propagation delay PL to output	Waveform 2		31 40	ns
t _{PLH} t _{PHL}	Propagation delay D ₇ to Q ₇	Waveform 3		17 36	ns
t _{PLH} t _{PHL}	Propagation delay D ₇ to Q ₇	Waveform 3		27 27	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Shift Register

74165

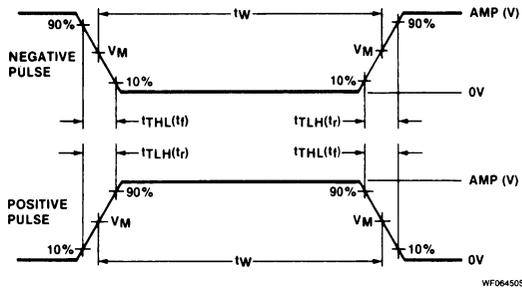
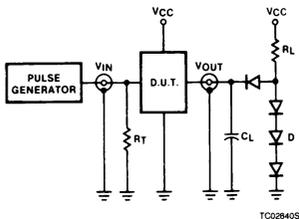
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t_w Clock pulse width	Waveform 1	25		ns
t_w $\overline{\text{PL}}$ pulse width	Waveform 2	15		ns
t_s Set-up time, D_S to clock	Waveform 4	20		ns
t_h Hold time, D_S to clock	Waveform 4	0		ns
$t_s(L)$ Set-up time, LOW $\overline{\text{CE}}$ to clock	Waveform 4	30		ns
t_h Hold time, $\overline{\text{CE}}$ to clock	Waveform 4	0		ns
t_s $\overline{\text{PL}}$ set-up time to clock	Waveform 2	45		ns
t_s Set-up time, D_5 and $D_7^{(1)}$ to $\overline{\text{PL}}$	Waveform 5	10		ns

NOTE:

1. The remaining six Data inputs and D_S are LOW. Prior to test, HIGH level data is loaded into D_7 input.

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

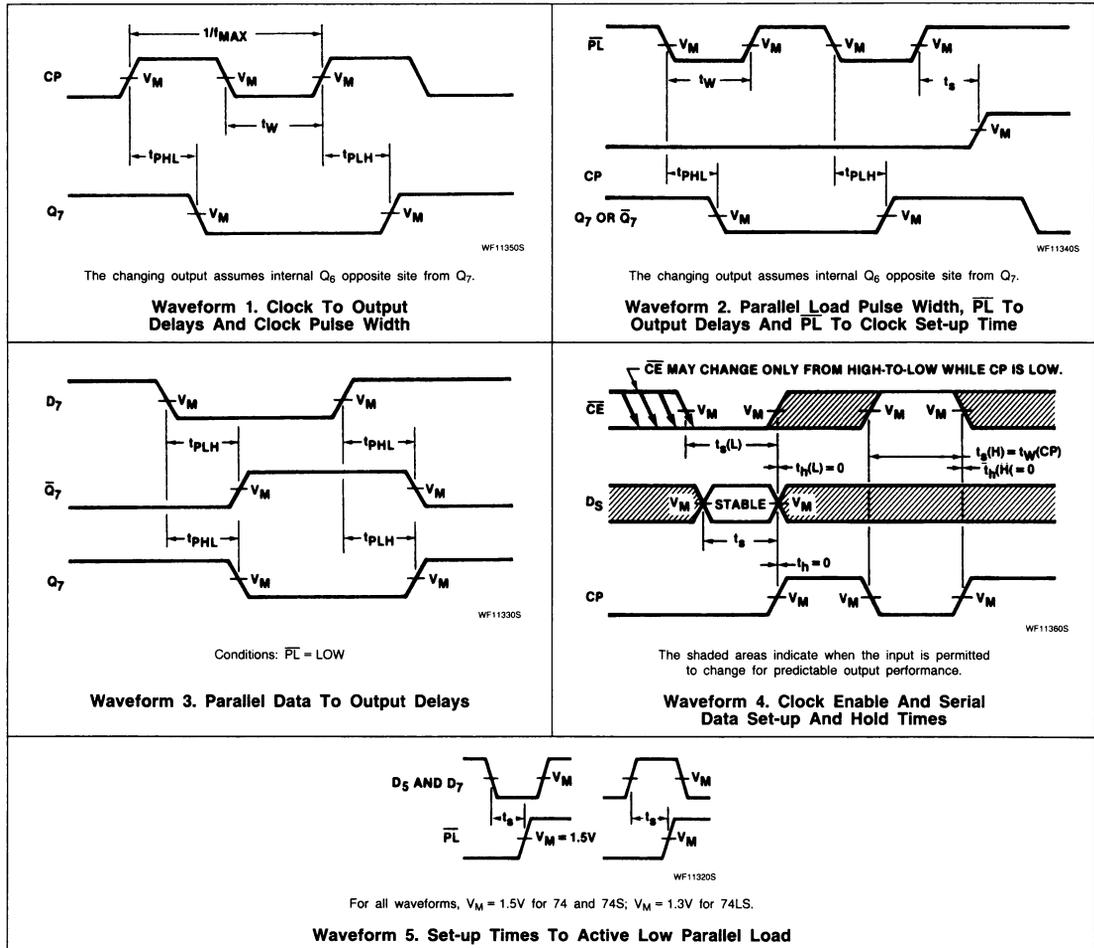
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

5

Shift Register

74165

AC WAVEFORMS



74166 Shift Register

8-Bit Serial/Parallel-In, Serial-Out Shift Register
Product Specification

Logic Products

FEATURES

- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous Master Reset
- See '165 for asynchronous parallel data load

DESCRIPTION

The '166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable (\overline{PE}) input. When the \overline{PE} is LOW one set-up time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When \overline{PE} is HIGH, data is entered into internal bit position Q_0 from Serial Data Input (D_S), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_S input of the succeeding stage.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74166	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74166N
Plastic SO	N74166D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1ul
Q_7	Output	10ul

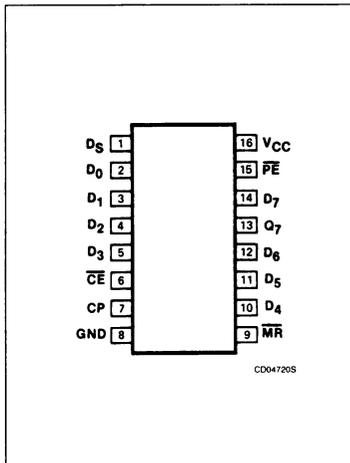
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

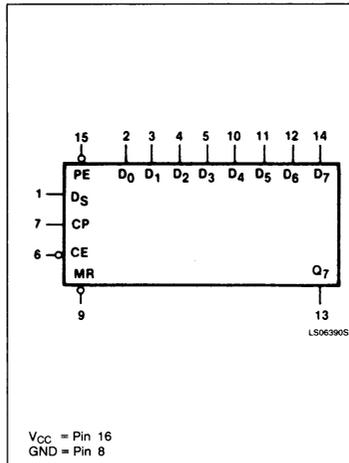
The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of \overline{CE} input should only

take place while the CP is HIGH for predictable operation. A LOW on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

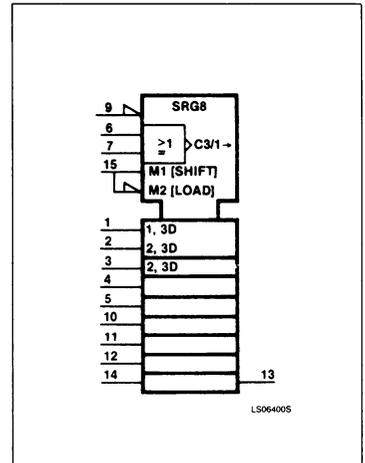
PIN CONFIGURATION



LOGIC SYMBOL



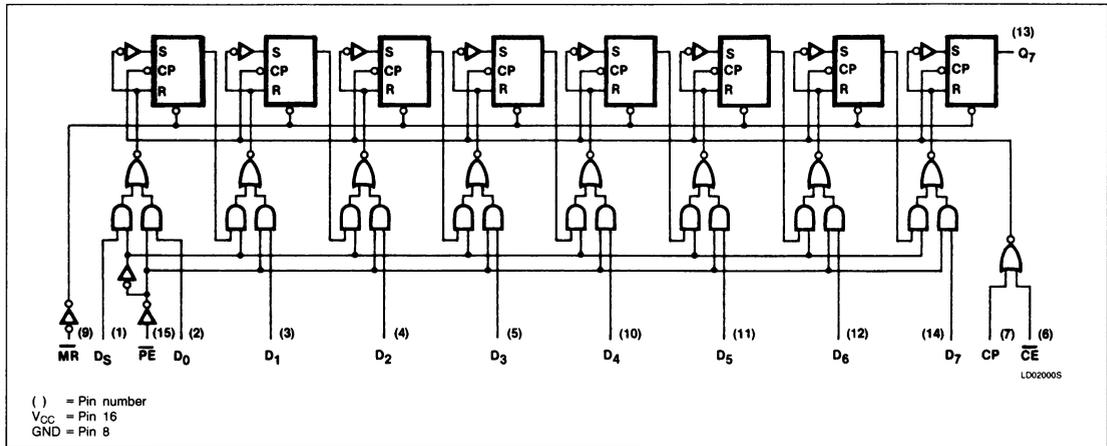
LOGIC SYMBOL (IEEE/IEC)



Shift Register

74166

LOGIC DIAGRAM

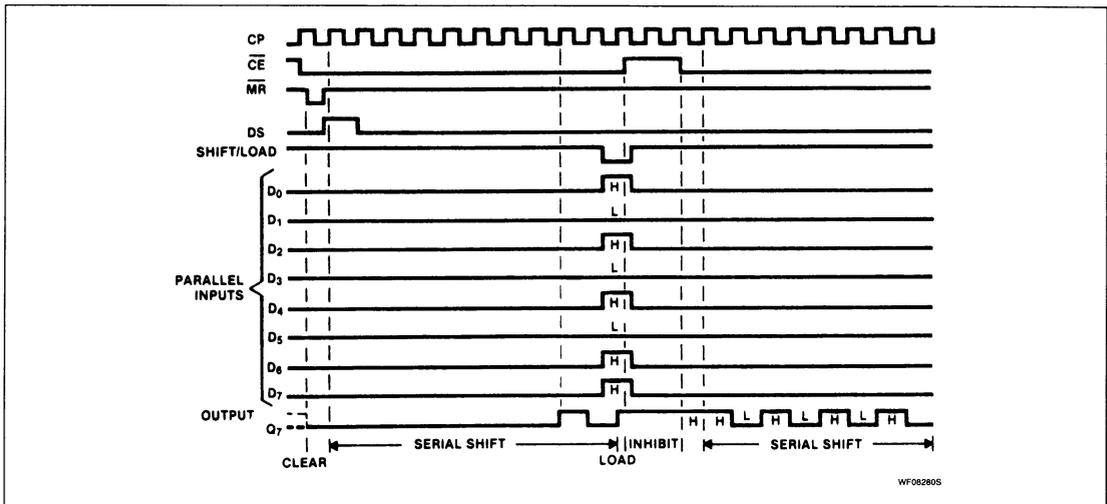


MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS						Q _n REGISTER		OUTPUT
	PE	CE	CP	D _S	D ₀ - D ₇	Q ₀	Q ₁ - Q ₆	Q ₇	
Parallel load	l	l	↑	X	l-h	L	L-L	L	
Serial shift	h	l	↑	l	X-X	L	Q ₀ -Q ₅	Q ₆	
Hold (do nothing)	X	h	X	X	X-X	Q ₀	Q ₁ -Q ₆	Q ₇	

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
 Q_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH Clock transition.

TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES



Shift Register

74166

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	HIGH-level output current			-800	μA
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74166			UNIT	
		Min	Typ ²	Max		
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}$		0.2	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-18		-57	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		90	127	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with 4.5V applied to the Serial input, a momentary ground, then 4.5V applied to Clock, all other inputs grounded and all outputs open.

Shift Register

74166

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		
		Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL} Propagation delay Clock to output	Waveform 1		26 30	ns ns
t_{PHL} Propagation delay \overline{MR} to output	Waveform 2		35	ns

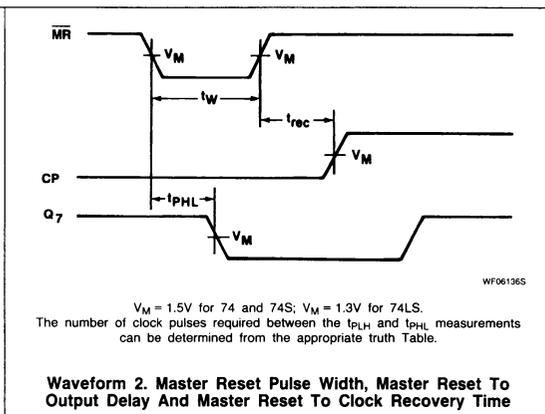
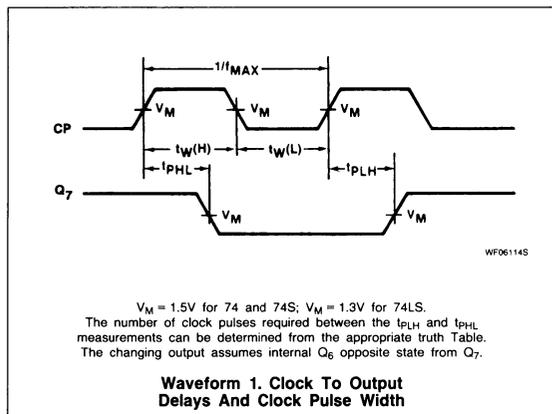
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t_w Clock pulse width	Waveform 1	20		ns
t_w \overline{MR} pulse width	Waveform 2	20		ns
t_s Set-up time data to clock	Waveform 3	20		ns
t_h Hold time data to clock	Waveform 3	0		ns
t_s Set-up time \overline{CE} to clock	Waveform 3	30		ns
t_h Hold time \overline{CE} to clock	Waveform 3	0		ns
t_s Set-up time \overline{PE} to clock	Waveform 3	30		ns
t_h Hold time \overline{PE} to clock	Waveform 3	0		ns
t_{rec} Recovery time \overline{MR} to clock	Waveform 2	30		ns

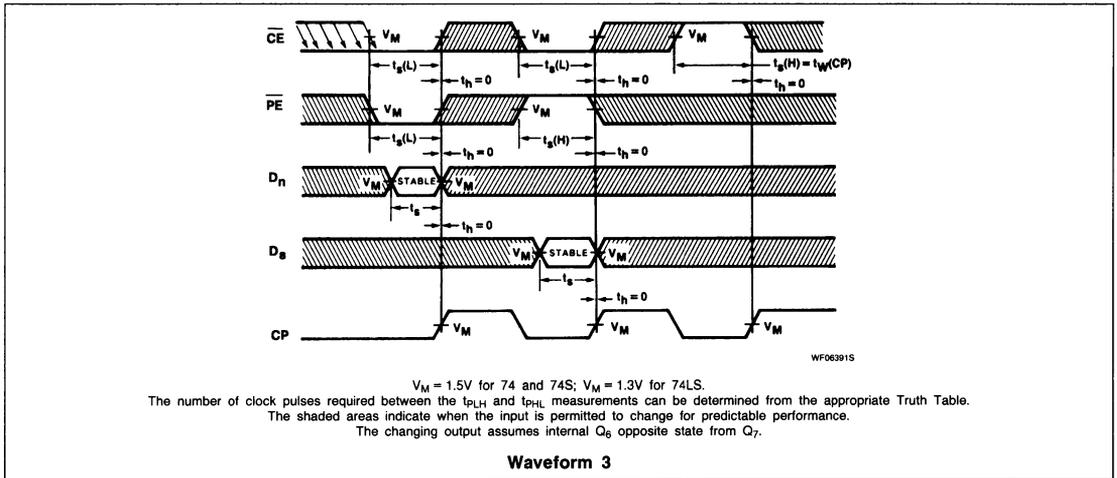
AC WAVEFORMS



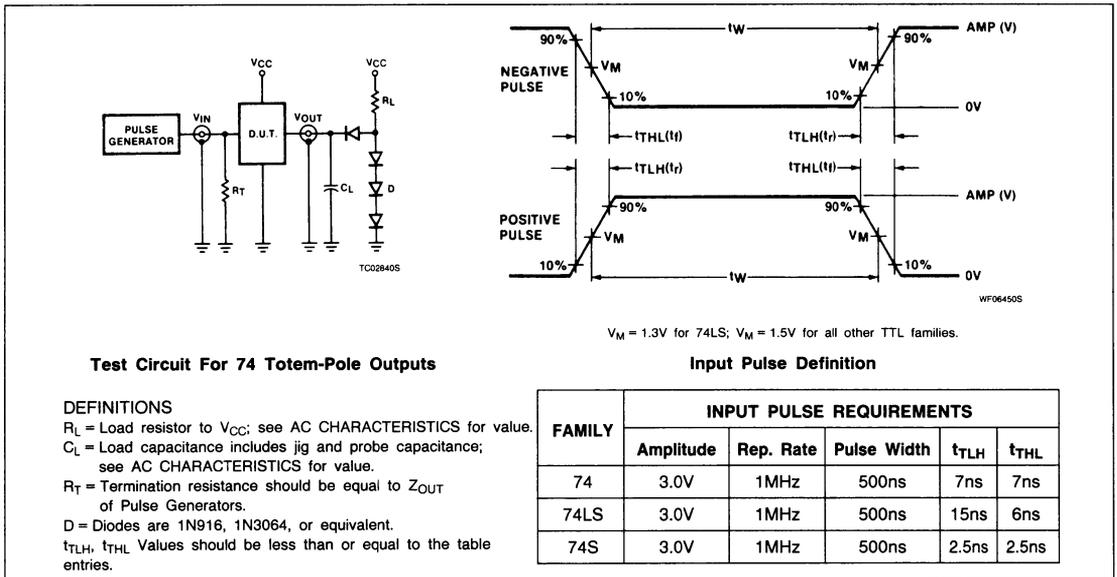
Shift Register

74166

AC WAVEFORMS (Continued)



TEST CIRCUITS AND WAVEFORMS



5

74LS168A, 74LS169A, S168A, S169A 4-Bit Bidirectional Counters

4-Bit Up/Down Synchronous Counter
Product Specification

Logic Products

FEATURES

- Synchronous counting and loading
- Up/down counting
- Modulo 16 binary counter — '169A
- BCD decade counter — '168A
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock

DESCRIPTION

The '168A is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS168A	32MHz	20mA
74S168A	70MHz	100mA
74LS169A	32MHz	20mA
74S169A	70MHz	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS168AN, N74S168AN N74LS169AN, N74S169AN
Plastic SO	N74LS169AD, N74S169AD, N74S169AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

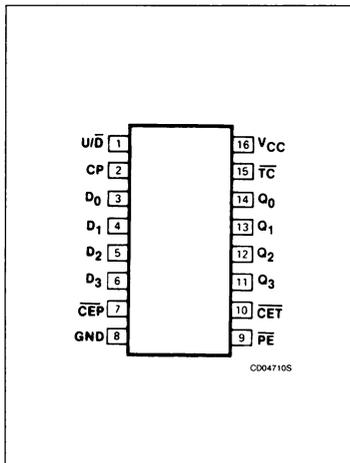
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
\overline{PE}	Input	1Sul	2LSul
\overline{CET}	Input	2Sul	1LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

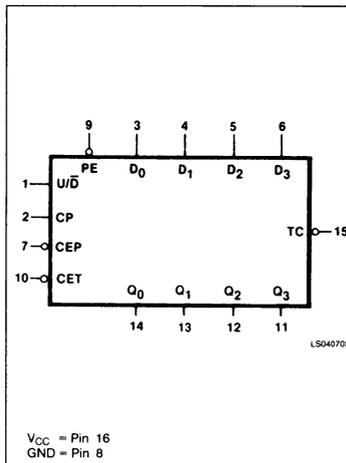
NOTE:

Where a 74S unit load (Sul) is understood to be $50\mu A I_{IH}$ and $-2.0mA I_{IL}$ and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

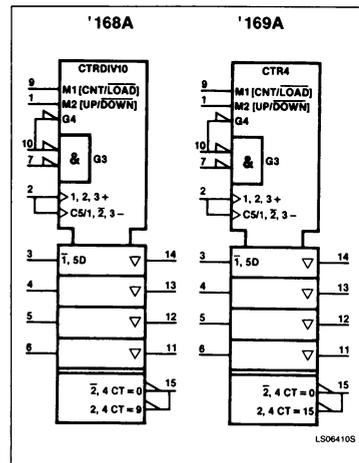
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down (U/\overline{D}) input; a HIGH will cause the

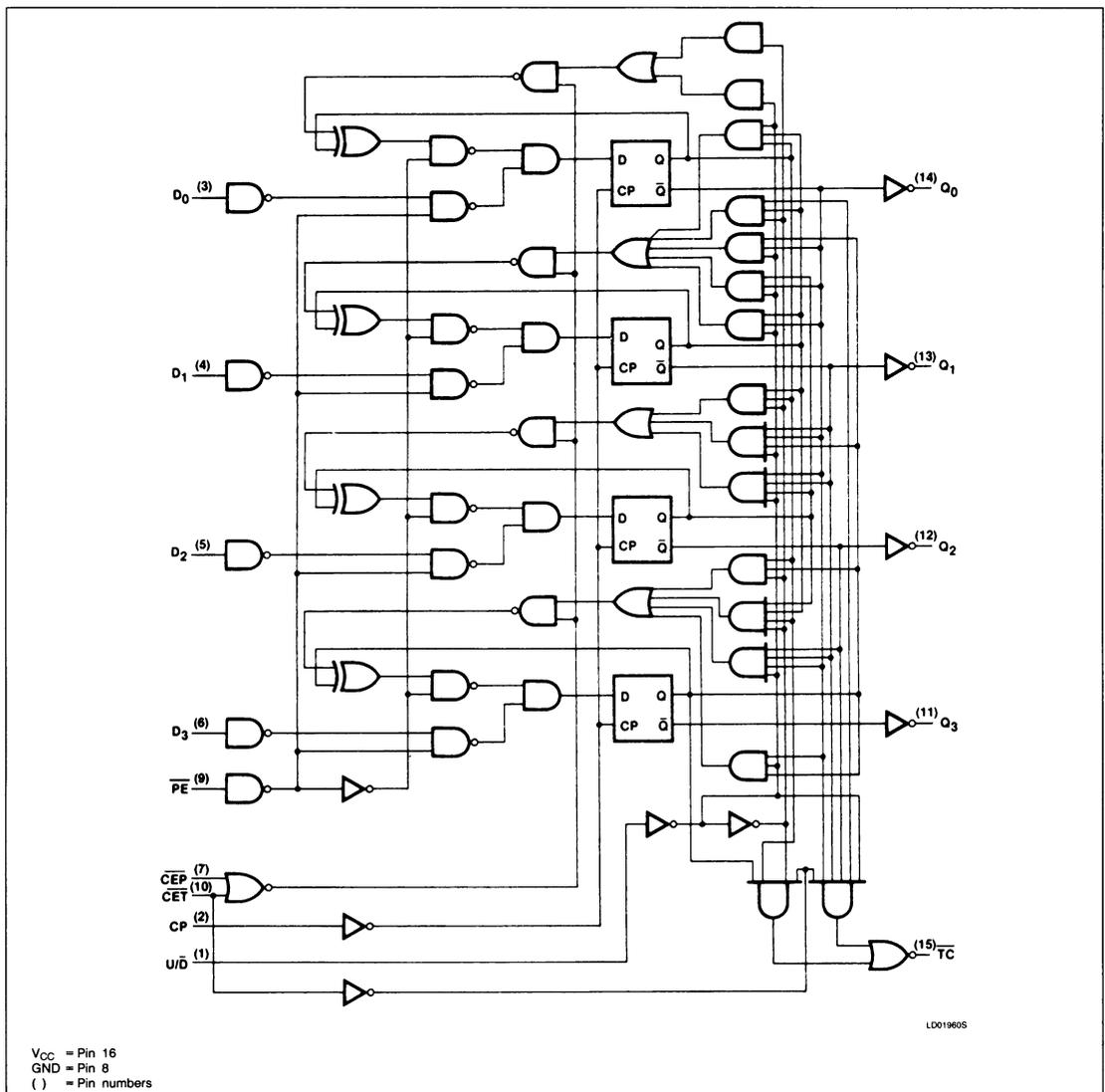
count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET} \cdot \overline{CEP}$) and a Terminal Count (\overline{TC}) output. Both Count Enable inputs must be LOW to count. The \overline{CET} input is fed forward to enable the \overline{TC} output. The \overline{TC} output thus enabled will produce a LOW

output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level \overline{TC} pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

The '169A is identical except that it is a Modulo 16 counter.

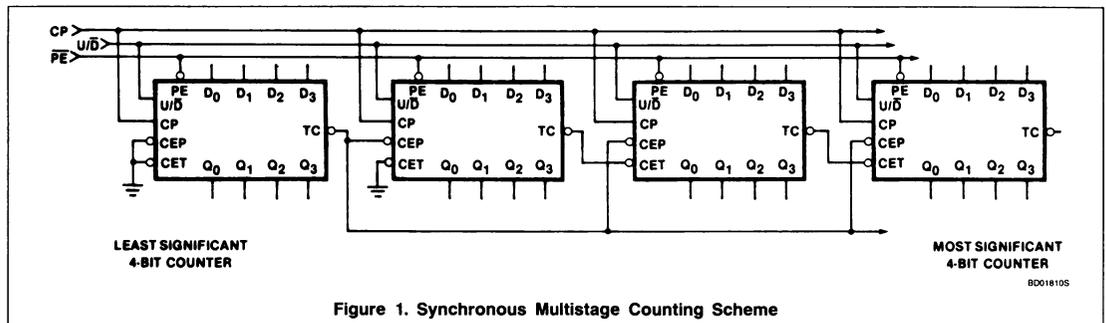
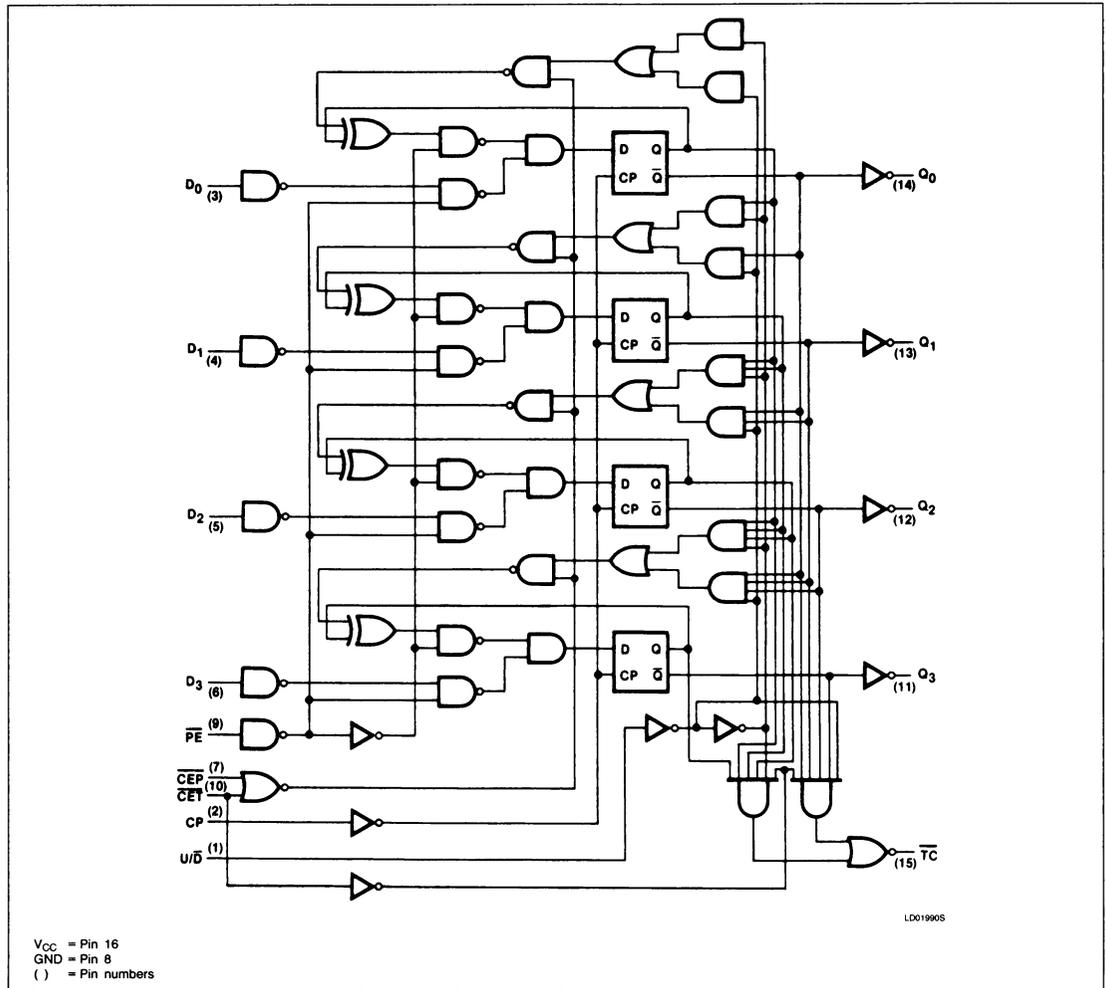
LOGIC DIAGRAM, '168A



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

LOGIC DIAGRAM, '169A



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS		
	CP	U/D	CEP	CET	PE	D _n	Q _n	TC	
Parallel Load	↑	X	X	X	l	i	L	(1)	
	↑	X	X	X	i	h	H	(1)	
Count Up	↑	h	l	l	h	X	Count Up	(1)	
Count Down	↑	l	l	l	h	X	Count Down	(1)	
Hold (do nothing)	↑	X	h	X	h	X	q _n	(1)	
	↑	X	X	h	h	X	q _n	H	

H = HIGH voltage level steady state
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level steady state
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
 ↑ = LOW-to-HIGH clock transition

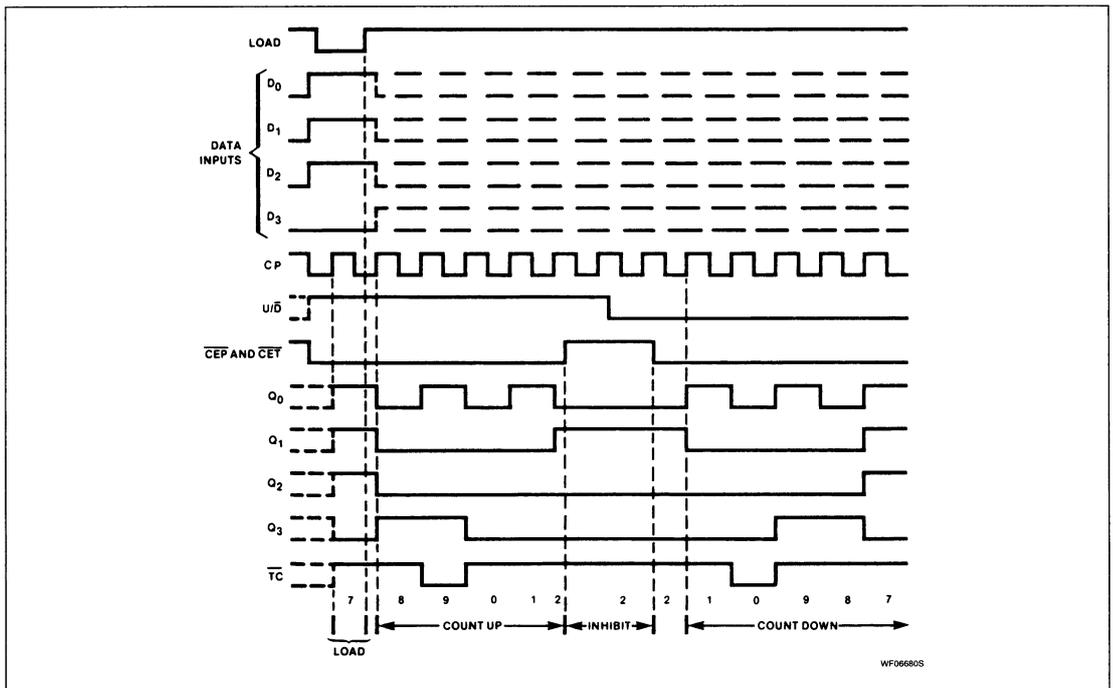
NOTE:

- The TC is LOW when \overline{CET} is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169A. The TC is LOW when \overline{CET} is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLL) and Terminal Count Down is (LLLL) for '168A.

WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the '168A. The operation of the '169A is similar.

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

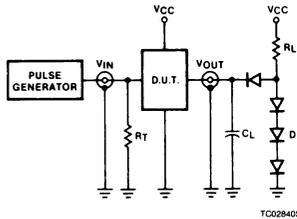
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

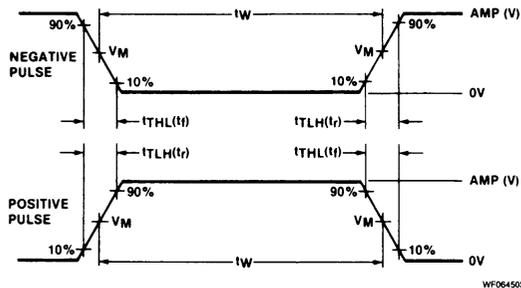
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-18			-18	mA
I _{OH} HIGH-level output current			-400			-1000	μA
I _{OL} LOW-level output current			8			20	mA
T _A Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS



TC02840S



WF06450S

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{PLH}, t_{PHL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{PLH}	t _{PHL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS168A, 169A			74S168A, 169A			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.35	0.5			0.5	V
		I _{OL} = 4mA (74LS)	0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA
		V _I = 7.0V	PE input		40			μA
			Other inputs		0.1			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	PE input		0.2		100	mA
			CET input		20		100	μA
			Other inputs		20		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	PE input		-0.8			mA
			Other inputs		-0.4			mA
		V _I = 0.5V	CET input					-4.0
Other inputs						-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		20	34		55	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after applying a momentary 4.5V, then ground to the Clock input with all other inputs grounded and outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S				UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω U/D = HIGH		C _L = 15pF, R _L = 280Ω U/D = LOW		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		40		40		MHz
t _{PLH} Propagation delay t _{PHL} Clock to Q output	Waveform 1		20 23		12 15		12 15	ns
t _{PLH} Propagation delay t _{PHL} Clock to TC	Waveform 1		35 35		17 15		15 25	ns
t _{PLH} Propagation delay t _{PHL} CET to TC	Waveform 2		14 14		11 15		11 15	ns
t _{PLH} Propagation delay t _{PHL} U/D control to TC ^(b)	Waveform 3		25 29		15 15		10 20	ns

NOTE:

- Propagation delay time from up/down to terminal count must be measured with the counter at either a minimum or a maximum count. As the logic level of the Up/Down input is changed, the Terminal Count output will follow. If the count is minimum (0), the Terminal Count output transition will be in phase. If the count is maximum (9 for '168A or 15 for 169A, the Terminal Count output will be out of phase.

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

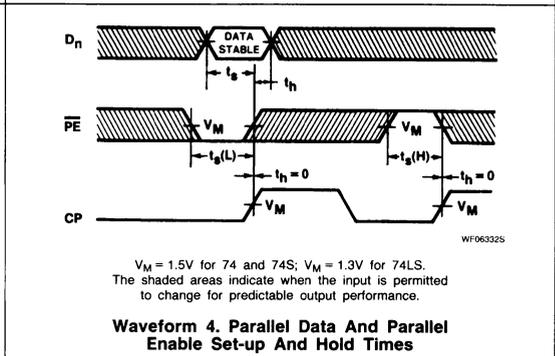
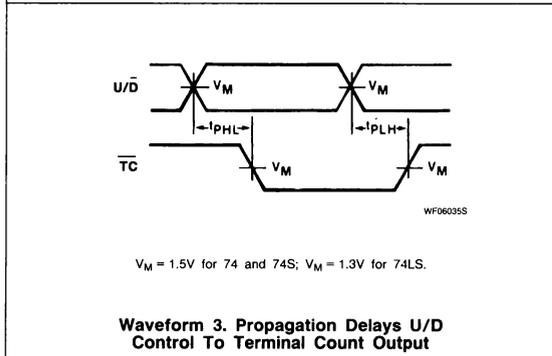
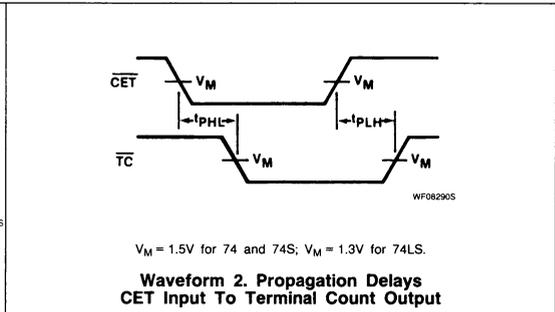
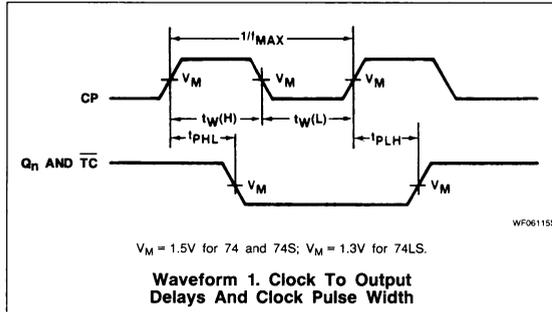
4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	25	10		ns
t_s	Setup time, data to clock	Waveform 4	20	6		ns
t_h	Hold time, data to clock	Waveform 4	0	1		ns
t_s	Setup time, \overline{PE} to clock	Waveform 4	25	9		ns
t_h	Hold time, \overline{PE} to clock	Waveform 4	0	0		ns
t_s	Setup time, \overline{CEP} & \overline{CET} to clock	Waveform 5	20	16		ns
t_h	Hold time, \overline{CEP} & \overline{CET} to clock	Waveform 5	0	0		ns
t_s	Setup time, U/\overline{D} to clock	Waveform 6	30	20		ns
t_h	Hold time, U/\overline{D} to clock	Waveform 6	0	0		ns

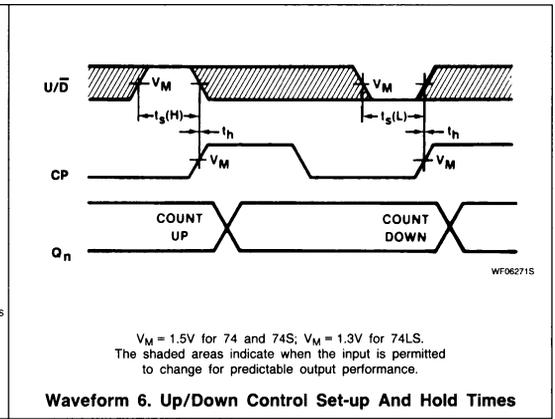
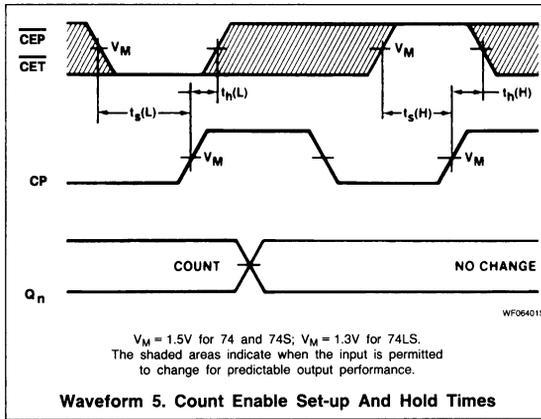
AC WAVEFORMS



4-Bit Bidirectional Counters

74LS168A, 74LS169A, S168A, S169A

AC WAVEFORMS (Continued)



74170, LS170 Register Files

4 x 4 Register File (Open Collector)
Product Specification

Logic Products

FEATURES

- Simultaneous and independent Read and Write operations
- Expandable to 1024 words by n-bits
- Open Collector outputs for wired-AND expansion
- See '670 for 3-State output version

DESCRIPTION

The '170 is a 16-bit register file organized as 4 words of 4 bits each, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable (WE) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the WE is LOW. Data supplied at the inputs will be read out in true (non-inverting) form. Data and Write Address inputs are inhibited when WE is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable (RE)

TYPE	TYPICAL PROPAGATION DELAY (RE to Q)	TYPICAL SUPPLY CURRENT (TOTAL)
74170	10ns (t_{PLH}) 20ns (t_{PHL})	127mA
74LS170	20ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74170N, N74LS170N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
D, W_A , W_B , R_A , R_B	Inputs	1uI	1LSuI
WE , RE	Inputs	1uI	2LSuI
All	Outputs	10uI	10LSuI

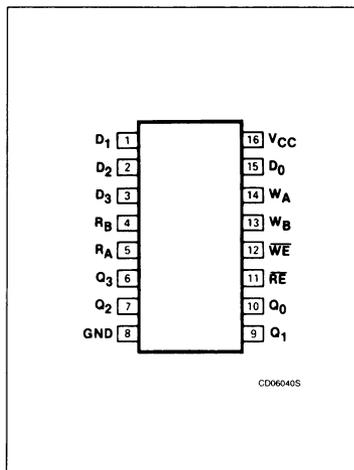
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} and a 74LS unit load (LSuI) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

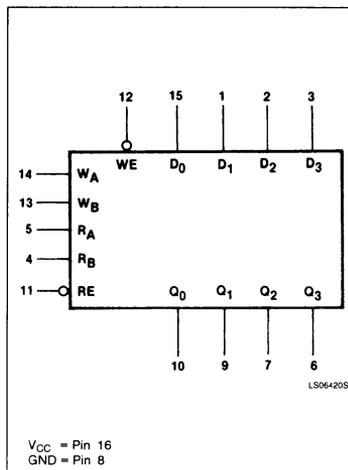
is LOW. Data outputs are inhibited and remain HIGH when the Read Enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times, and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the Open Collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

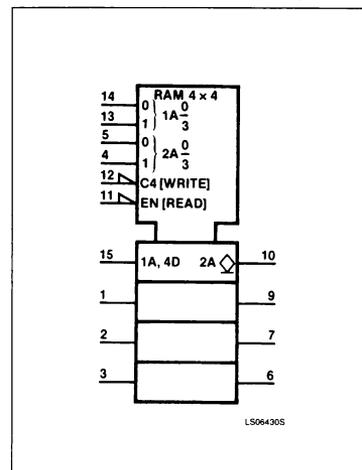
PIN CONFIGURATION



LOGIC SYMBOL



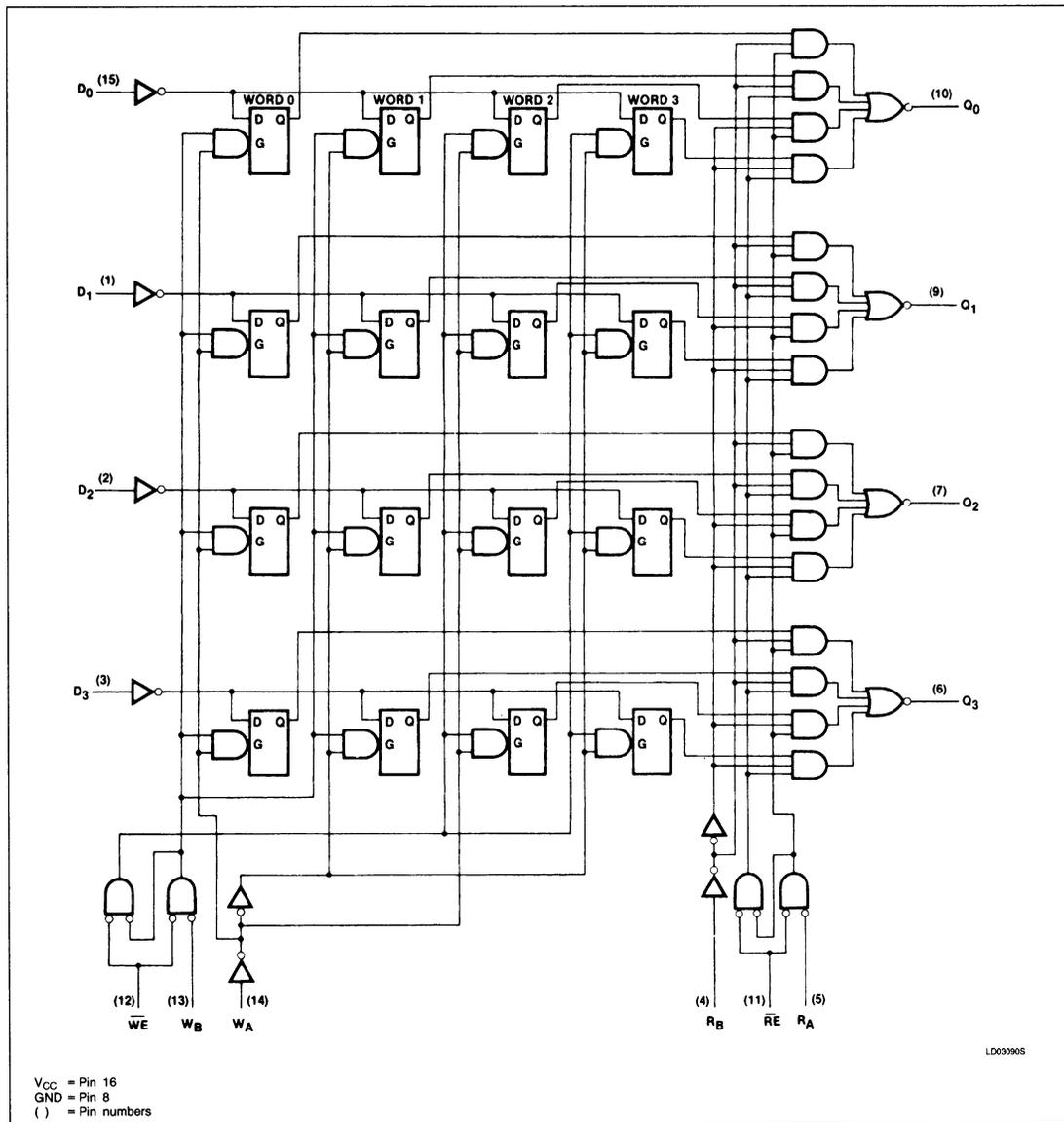
LOGIC SYMBOL (IEEE/IEC)



Register Files

74170, LS170

LOGIC DIAGRAM



Register Files

74170, LS170

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES ^(a)
	\overline{WE}	D_n	
Write data	L L	L H	L H
Data latched	H	X	no change

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	\overline{RE}	Internal Latches ^(b)	Q_n
Read	L L	L H	L H
Disabled	H	X	H

H = HIGH voltage level

L = LOW voltage level

X = Don't care.

NOTES:

a. The Write Address (W_A and W_C) to the "internal latches" must be stable while \overline{WE} is LOW for conventional operation.

b. The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by \overline{WE} or \overline{RE} operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-12			-18	mA
V_{OH}	HIGH-level output voltage			5.5			5.5	V
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

Register Files

74170, LS170

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74170			74LS170			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
I _{OH}	HIGH-level output current V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			30			100	μA	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	D, W _A , W _B , R _A , R _B inputs					0.1	mA
			WE, RE inputs					0.2	mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40			μA	
		V _I = 2.7V	D, W _A , W _B , R _A , R _B inputs					20	μA
			WE, RE inputs					40	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V	D, W _A , W _B , R _A , R _B inputs			-1.6		-0.4	mA	
		WE, RE inputs			-1.6		-0.8	mA	
I _{CC}	Supply current ³ (total) V _{CC} = MAX		127	150		25	40	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Measure I_{CC} with 4.5V applied to all Data and both Enable inputs, the Address inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Read Enable to output Waveform 1		15 30		30 30	ns
t _{PLH} t _{PHL}	Propagation delay Read Address to output Waveform 2		35 40		40 40	ns
t _{PLH} t _{PHL}	Propagation delay Write Enable to output Waveform 1		40 45		45 40	ns
t _{PLH} t _{PHL}	Propagation delay Data to output Waveform 1		30 45		45 35	ns

Register Files

74170, LS170

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

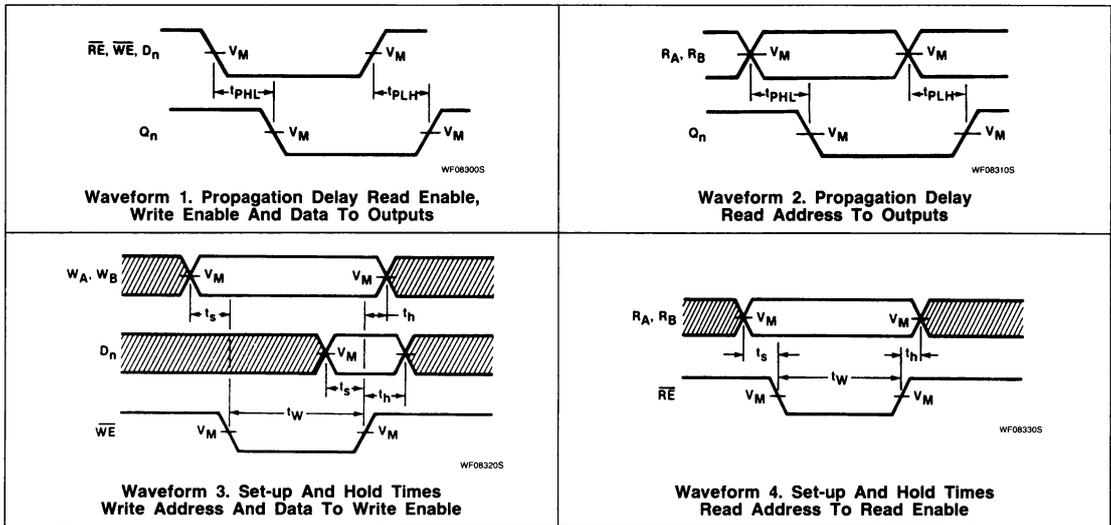
PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W	Write enable pulse width	25		25		ns
t_s	Set-up time, data to positive-going $\overline{WE}^{(c)}$	10		10		ns
t_h	Hold time, data to positive-going $\overline{WE}^{(c)}$	15		15		ns
t_s	Set-up time, read address to negative-going $\overline{WE}^{(c)}$	15		15		ns
t_h	Hold time, read address to positive-going $\overline{WE}^{(c)}$	5.0		5.0		ns
t_W	Read enable pulse width	25		25		ns
t_{latch}	Latch time for new data ^(d)	25		25		ns

NOTES:

c. Write Address set-up time will protect the data written into the previous address. If protection of data in the previous address is not required, t_s (Write Address to \overline{WE}) can be ignored, as any address selection sustained for the final 30ns of the \overline{WE} pulse and during t_h (Write Address to \overline{WE}) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of \overline{WE} to the rising edge of R_A or R_B . \overline{RE} must be LOW.

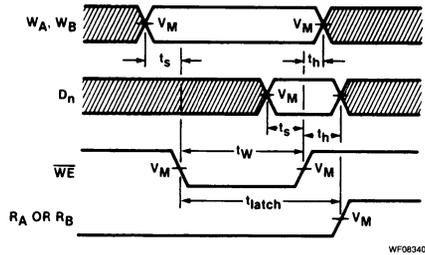
AC WAVEFORMS



Register Files

74170, LS170

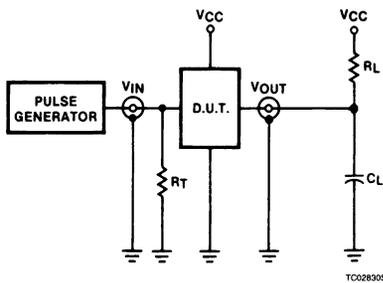
AC WAVEFORMS (Continued)



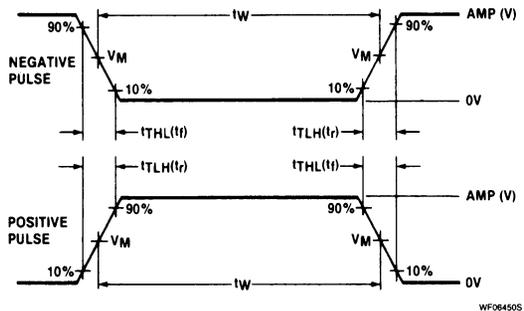
For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Set-up And Hold Times Write Address And Data To Write Enable

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74S172 Register File

16-Bit Multiple Port Register File (3-State)
Product Specification

Logic Products

FEATURES

- Simultaneous and independent Read and Write operations
- Expandable to 1024 words on n-bits
- 3-State outputs

DESCRIPTION

The '172 is a high-performance, 16-bit multiport register file with 3-State outputs organized as eight words of two bits each. Multiple address decoding circuitry is used so that the read and write operation can be performed independently on up to three word locations. Data can be written into two word locations through input Port "A" or input Port "C" while data is simultaneously read from both output Port "B" and output Port "C".

Port "A" is an input port which can be used to write two bits of data (D_{A0} , D_{A1}) into one of eight register locations selected by the Address inputs (A_{A0} , A_{A1} , A_{A2}). When the Write Enable (\overline{WE}_A) input is LOW one set-up time prior to the LOW-to-HIGH transition of the Clock (CP) input, the data is written into the selected location.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74S172	40MHz	160mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S172N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
All	Outputs	8Sul

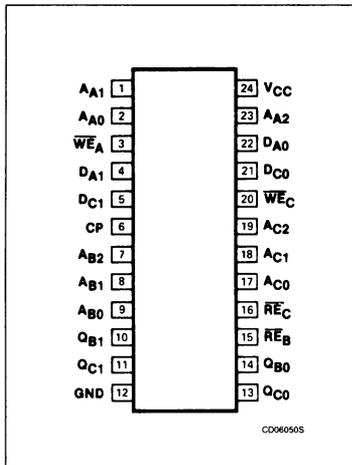
NOTE:

A 74S unit load (Sul) is $50\mu A$ and $I_{IH} = -2.0mA$.

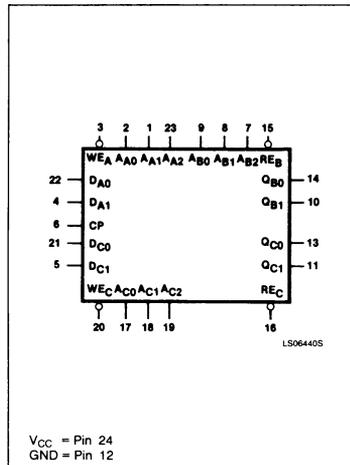
Port "B" is an output port which can be used to read two bits of data from one of eight register locations selected by the Address inputs (A_{B0} , A_{B1} , A_{B2}). When the Read Enable (\overline{RE}_B) is LOW, the selected 2-bit word appears on outputs Q_{B0} and Q_{B1} . When \overline{RE}_B is HIGH, the Q_{B0} and Q_{B1} outputs are in the HIGH impedance "off" state. The read operation is independent of the clock.

Port "C" is a read/write port that has separate Data input and Data output sections, but common Address inputs (A_{C0} , A_{C1} , A_{C2}). Data can be simultaneously written into and read from the same register location. Port "C" can be used to write data into one location while Port "A" is writing into a different location, but data cannot be written reliably into the same location simultaneously.

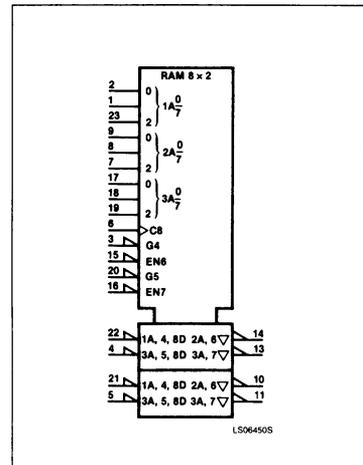
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Register File

74S172

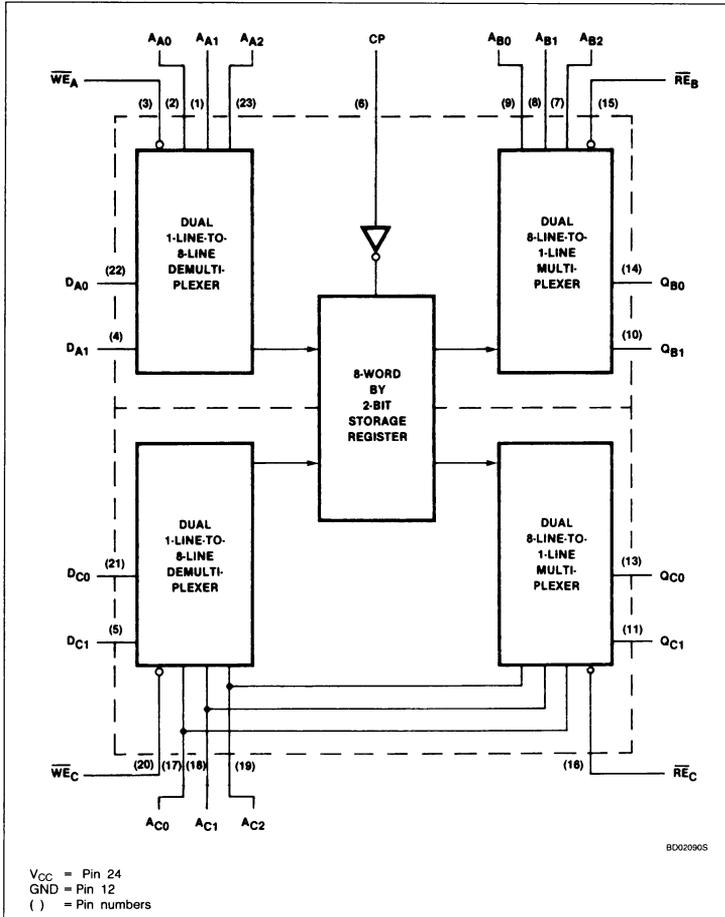
If both Ports "A" and "C" are enabled for writing into the same location during the same clock cycle, the LOW data will predominate if there is a conflict.

The register operation is essentially a master-slave flip-flop. Each master acts as a trans-

parent D latch when selected by the "A" or "C" address and the clock and applicable write enable are LOW. The data in the master is transferred to the slave (or output section) following the LOW-to-HIGH transition of the Clock (CP). The Address inputs must be stable while the Clock and Write Enable

inputs are LOW to ensure retention of data previously written into the other locations. Any number of masters can be altered while the clock and write enable are LOW, but the new data will not be loaded into the slaves, or be available at the outputs, until the clock goes HIGH.

BLOCK DIAGRAM



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS			ADDRESSED REGISTER
	CP	WE	D_n	
Write data ^(a)	↑	l	h	L H
Hold ^(b)	↓	h	X	no change

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	RE	Addressed Register	
Read	L L	L H	L H
Disabled	H	X	(Z)

- H = HIGH voltage level steady state.
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH or HIGH-to-LOW clock transition.
- L = LOW voltage level steady state.
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
- X = Don't care.
- (Z) = HIGH impedance (off) state.
- ↑ = LOW-to-HIGH clock transition.
- ↓ = HIGH-to-LOW clock transition.

NOTES:

- a. The Write Address (A_n and A_c) to the "internal register" must be stable while \overline{WE} and CP are LOW for conventional operation.
- b. The Write Enable must be HIGH before the HIGH-to-LOW clock transition to ensure that the data in the register is not changed.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

Register File

74S172

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74S			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-5.2	mA
I _{OL}	LOW-level output current			20	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		74S172			UNIT
				Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4			V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX				0.5	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V				40	μA
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.4V				-40	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V				1.0	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V				40	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	CP, WE _A , WE _C , AC ₀ - AC ₂			-1.6	mA
			Other inputs				-0.8
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-18		-55	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			160	190	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all inputs at 4.5V and all outputs open.

Register File

74S172

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74S		UNIT
		$C_L = 50\text{pF}$, $R_L = 400\Omega$		
		Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30	MHz
t_{PLH} t_{PHL}	Propagation delay Address (B or C) to output	Waveform 2	30 30	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	38 38	ns
t_{PZH}	Read enable time to HIGH	Waveform 3	30	ns
t_{PZL}	Read enable time to LOW	Waveform 4	30	ns
t_{PHZ}	Disable time from HIGH	Waveform 3, $C_L = 5\text{pF}$	20	ns
t_{PLZ}	Disable time from LOW	Waveform 4, $C_L = 5\text{pF}$	20	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

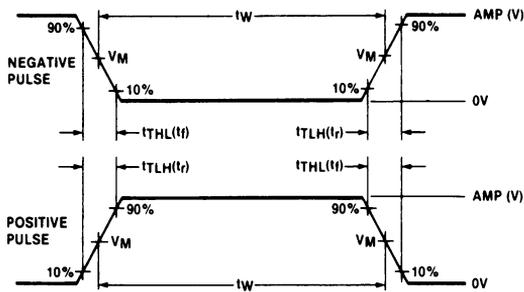
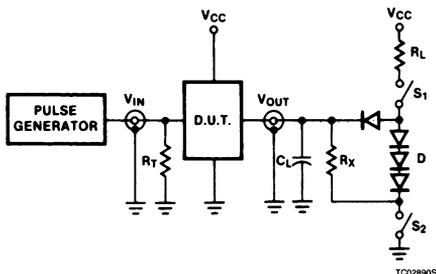
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74S		UNIT
		Min	Max	
t_w	Clock pulse width	Waveform 1	25	ns
t_s	Set-up time, write address (A or C) to negative-going clock and \overline{WE}	Waveform 5	15	ns
t_h	Hold time, write address (A or C) to positive-going clock and \overline{WE}	Waveform 5	0	ns
$t_s(\text{H})$	Set-up time, HIGH data to clock	Waveform 5	30	ns
$t_h(\text{H})$	Hold time, HIGH data to clock	Waveform 5	0	ns
$t_s(\text{L})$	Set-up time, LOW data to clock	Waveform 5	20	ns
$t_h(\text{L})$	Hold time, LOW data to clock	Waveform 5	0	ns
t_s	Set-up time, LOW \overline{WE} to positive-going clock	Waveform 6	35	ns
t_h	Hold time, LOW \overline{WE} to positive-going clock	Waveform 6	0	ns
t_s	Set-up time, HIGH \overline{WE} to negative-going clock	Waveform 6	10	ns
t_h	Hold time, HIGH \overline{WE} to positive-going clock	Waveform 6	0	ns

Register File

74S172

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

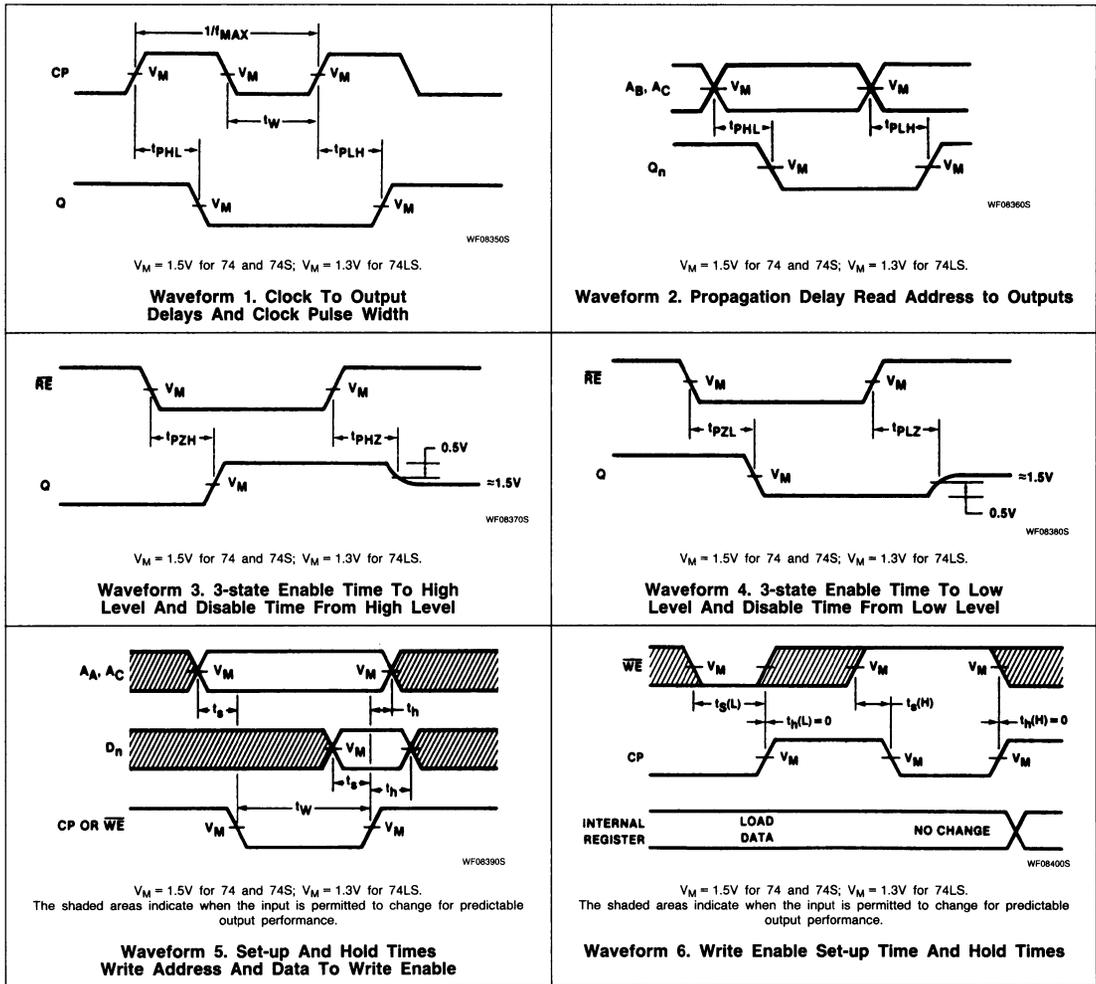
D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Register File

74S172

AC WAVEFORMS



74173, LS173 Flip-Flops

Quad D-Type Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- Edge-triggered D-type register
- Gated Input enable for hold "do nothing" mode
- 3-State output buffers
- Gated output enable control
- Pin compatible with the 8T10 and DM8551

DESCRIPTION

The '173 is a 4-bit parallel load register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable (\bar{E}_1 and \bar{E}_2) inputs are LOW, the data on the D inputs is loaded into the register synchronously with the LOW-to-HIGH Clock (CP) transition. When one or both \bar{E} inputs are HIGH one set-up time before the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and Clock Enable inputs are fully edge triggered and must be stable only one set-up time before the LOW-to-HIGH clock transition.

The Master Reset (MR) is an active HIGH asynchronous input. When the MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74173	35MHz	50mA
74LS173	50MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74173N, N74LS173N
Plastic SO-16	N74LS173D
Plastic SOL-16	CD7186D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	30LSul

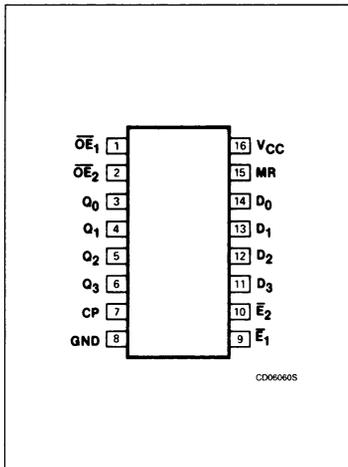
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$ and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

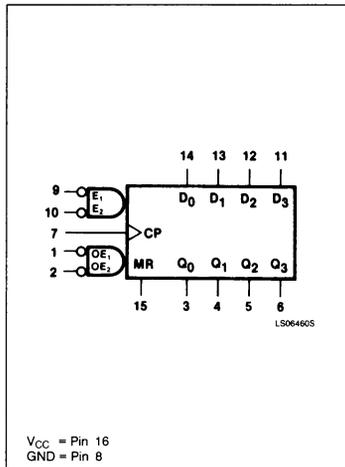
The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable (\bar{OE}_1 and \bar{OE}_2) inputs are LOW, the data in the register is presented at the Q outputs. When one or both \bar{OE} inputs is HIGH, the outputs are

forced to a HIGH impedance "off" state. The 3-State output buffers are completely independent of the register operation; the \bar{OE} transition does not affect the clock and reset operations.

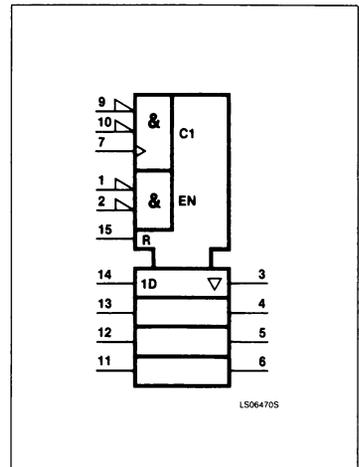
PIN CONFIGURATION



LOGIC SYMBOL



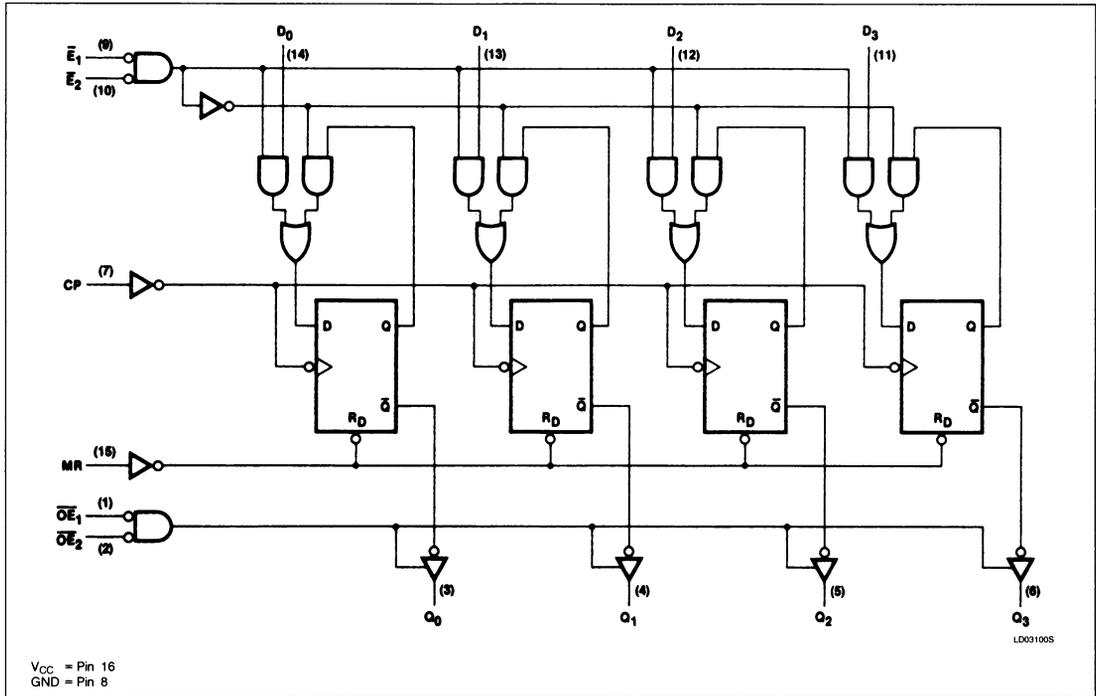
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74173, LS173

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	\bar{E}_1	\bar{E}_2	D _n	Q _n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (no change)	L	X	h	X	X	q _n
	L	X	X	h	X	q _n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS	
	Q _n (Register)		\bar{OE}_1	\bar{OE}_2	Q ₀ , Q ₁ , Q ₂ , Q ₃
Read	L	L	L	L	L
	H	L	L	L	H
Disabled	X	X	H	X	(Z)
	X	X	X	H	(Z)

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced input (or output) on set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
(Z) = HIGH impedance "off" state.
↑ = LOW-to-HIGH clock transition.

Flip-Flops

74173, LS173

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	HIGH-level output current			5.2			-2.6	mA
I_{OL}	LOW-level output current			16			24	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74173			74LS173			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4			2.4	3.1		V
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.4	0.35	0.5		V
		$I_{OL} = 12\text{mA}$ (74LS)			0.25	0.4		V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied $V_{CC} = \text{MAX}, V_{IH} = \text{MIN}$	$V_O = 2.4\text{V}$		40				μA
		$V_O = 2.7\text{V}$				20		μA
I_{OZL}	Off-state output current, LOW-level voltage applied $V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_O = 0.4\text{V}$			-40			-20	μA
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$		1.0				mA
		$V_I = 7.0\text{V}$				0.1		mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$		40				μA
		$V_I = 2.7\text{V}$				20		μA
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6			-0.4	mA
I_{OS}	Short-circuit output current ³ $V_{CC} = \text{MAX}$	-30		-70	-30		-130	mA
I_{CC}	Supply current ⁴ (total) $V_{CC} = \text{MAX}$		50	72	20	30		mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$, and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with MR grounded following momentary connection to 4.5V, $\overline{OE}_2, \overline{E}_1, \overline{E}_2$ and all Data inputs grounded, CP and \overline{OE}_1 at 4.5V, and all outputs open.

Flip-Flops

74173, LS173

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT	
		$C_L = 50\text{pF}$, $R_L = 400\Omega$		$C_L = 45\text{pF}$, $R_L = 667\Omega$			
		Min	Max	Min	Max		
f_{MAX}	Maximum clock frequency	Waveform 1		25		30	MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1			43 31	25 30	ns
t_{PHL}	Propagation delay, MR to output	Waveform 4			27	35	ns
t_{PZH}	Output enable to HIGH level	Waveform 2			30	23	ns
t_{PZL}	Output enable to LOW level	Waveform 3			30	27	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, $C_L = 5\text{pF}$			14	17	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, $C_L = 5\text{pF}$			20	17	ns

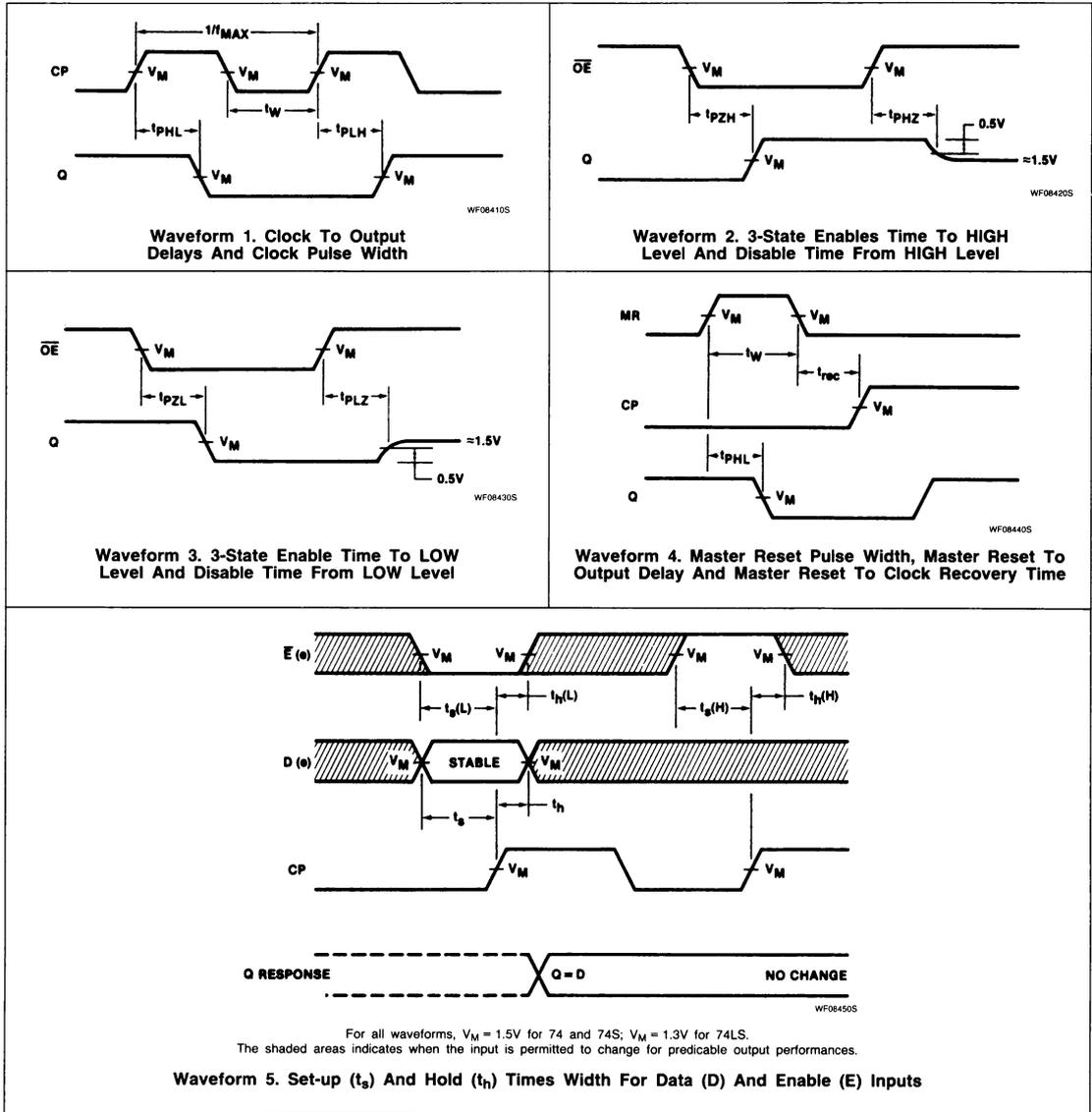
NOTE:Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.**AC SET-UP REQUIREMENTS** $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT	
		Min	Max	Min	Max		
$t_{\text{W}}(\text{CP})$	Clock pulse width	Waveform 1		20		20	ns
$t_{\text{W}}(\text{MR})$	MR pulse width	Waveform 4		20		20	ns
$t_s(\text{D})$	Set-up time, data to clock	Waveform 5		10		17	ns
$t_h(\text{D})$	Hold time, data to clock	Waveform 5		10		0	ns
$t_s(\bar{\text{E}})$	Set-up time, enable to clock	Waveform 5		17		35	ns
$t_h(\bar{\text{E}})$	Hold time, enable to clock	Waveform 5		2		0	ns
$t_{\text{rec}}(\text{MR})$	Recovery time, Master Reset to clock	Waveform 4		10		17	ns

Flip-Flops

74173, LS173

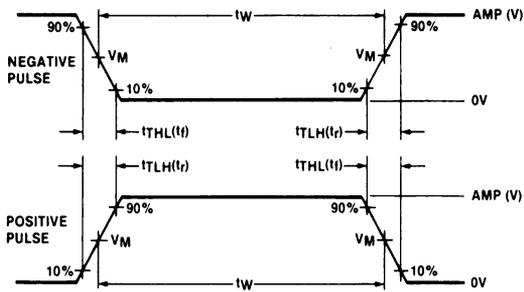
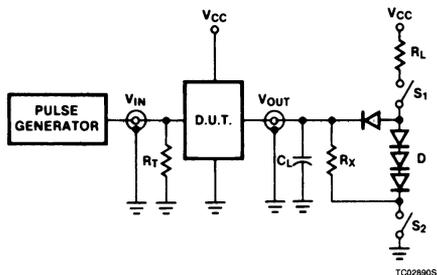
AC WAVEFORMS



Flip-Flops

74173, LS173

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

74174, LS174, S174 Flip-Flops

Hex D Flip-Flops
Product Specification

Logic Products

FEATURES

- Six edge-triggered D-type flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

DESCRIPTION

The '174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74174	35MHz	45mA
74LS174	40MHz	16mA
74S174	110MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74174N, N74LS174N, N74S174N
Plastic SO-16	N74LS174D, N74S174D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

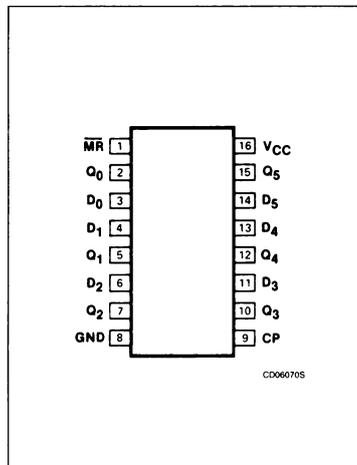
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
$Q_0 - Q_5$	Outputs	10ul	10Sul	10LSul

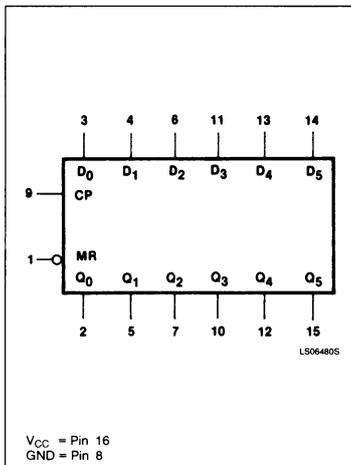
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

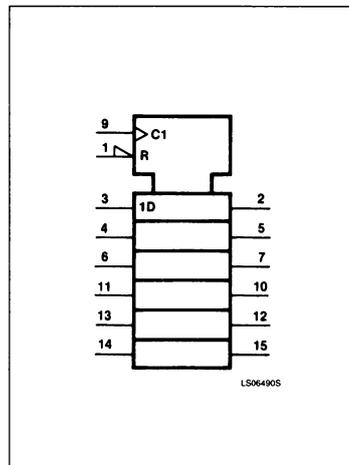
PIN CONFIGURATION



LOGIC SYMBOL



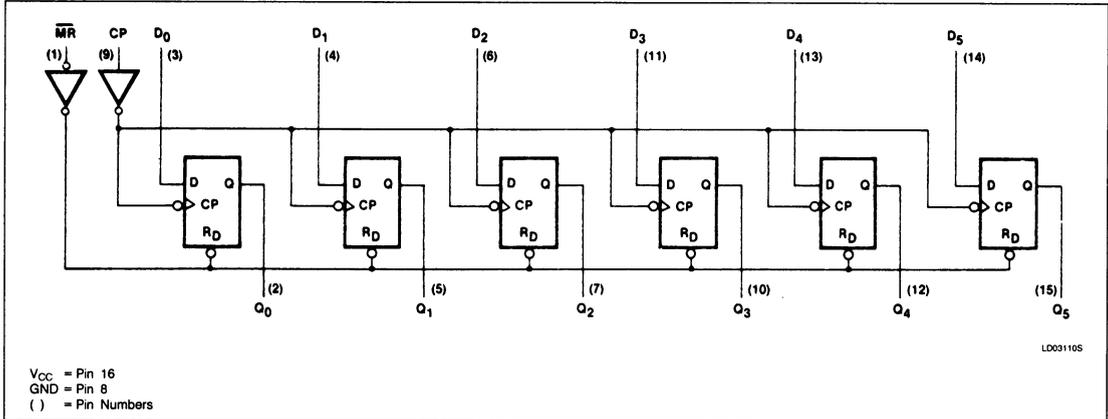
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74174, LS174, S174

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	\overline{MR}	CP	D _n	Q _n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18			-18	mA
I _{OH} HIGH-level output current			-800			-400			-1000	μA
I _{OL} LOW-level output current			16			8			20	mA
T _A Operating free-air temperature	0		70	0		70	0		70	°C

Flip-Flops

74174, LS174, S174

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74174			74LS174			74S174			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4			
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5		-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA
		V _I = 7.0V						0.1			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA
		V _I = 2.7V						20		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA
		V _I = 0.5V								-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		45	65		16	26		90	144	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after a momentary ground, then 4.5V is applied to Clock, with 4.5V applied to all Data and \overline{MR} inputs and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		30		75		MHz
t _{PLH} Propagation delay	Waveform 1		30		30		13	ns
t _{PHL} Clock to output			35		30		17	
t _{PHL} Propagation \overline{MR} delay to output	Waveform 3		35		35		22	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

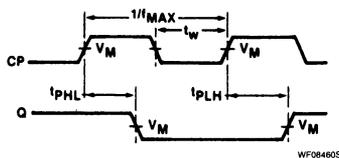
Flip-Flops

74174, LS174, S174

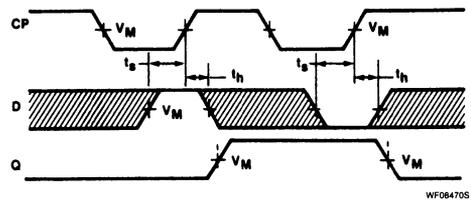
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 1	20		20		7.0		ns
t_w Master Reset pulse width	Waveform 3	20		20		10		ns
t_s Set-up time, data to CP	Waveform 2	20		20		5.0		ns
t_h Hold time, data to CP	Waveform 2	5		5		3.0		ns
t_{rec} Recovery time, \overline{MR} to CP	Waveform 3	25		25		5.0		ns

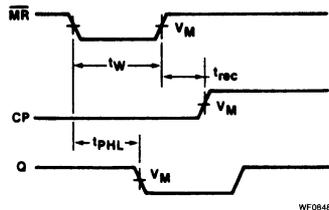
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



Waveform 2. Data Set-up And Hold Times



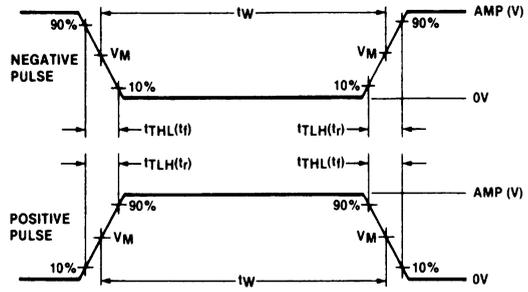
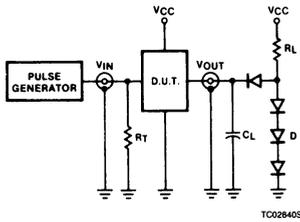
For all waveforms, $V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance

Waveform 3. Master Reset To Output Delay, Master Reset Pulse Width, And Master Reset Recovery Time

Flip-Flops

74174, LS174, S174

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74175, LS175, S175 Flip-Flops

Quad D Flip-Flop
Product Specification

Logic Products

FEATURES

- Four edge-triggered D flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

DESCRIPTION

The '175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and \bar{Q} outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74175	35MHz	30mA
74LS175	40MHz	11mA
74S175	110MHz	60mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74175N, N74LS175N, N74S175N
Plastic SO-16	N74LS175D, N74S175D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

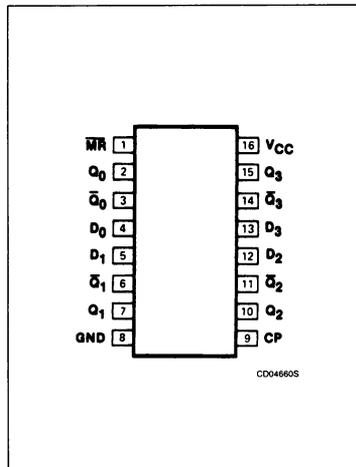
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

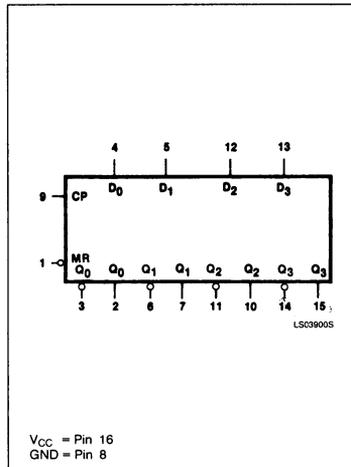
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

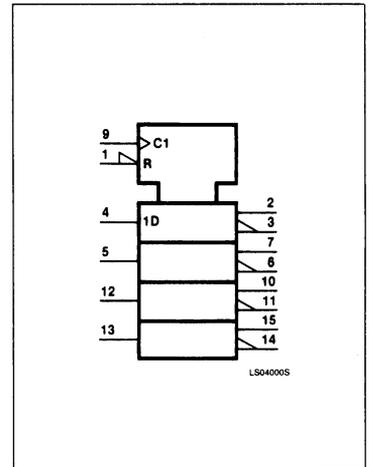
PIN CONFIGURATION



LOGIC SYMBOL



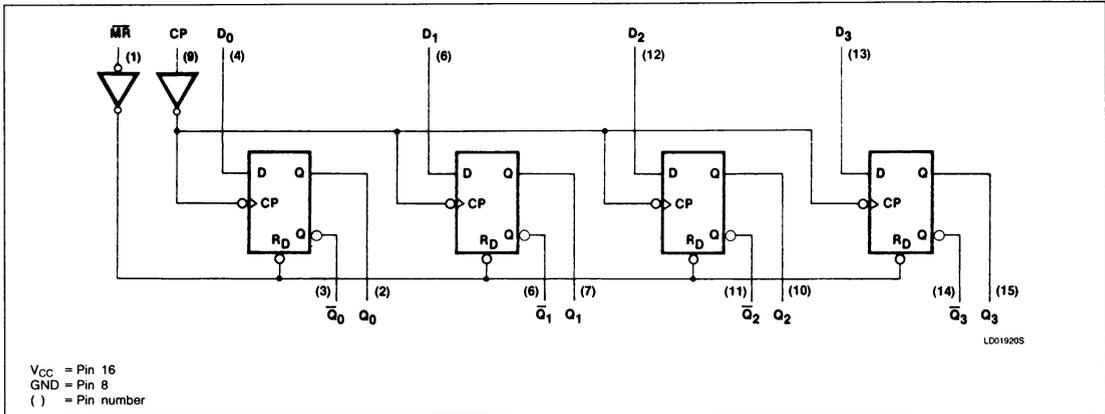
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74175, LS175, S175

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	MR	CP	D_n	Q_n	\bar{Q}_n
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	2.0			2.0			2.0			V
V_{IL}			+0.8			+0.8			+0.8	V
I_{IK}			-12			-18			-18	mA
I_{OH}			-800			-400			-1000	μA
I_{OL}			16			8			20	mA
T_A	0		70	0		70	0		70	°C

Flip-Flops

74175, LS175, S175

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74175			74LS175			74S175			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V						20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		30	45		11	18		60	96	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With all outputs open and 4.5V applied to all Data and Master Reset inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		30		75		MHz
t _{PLH} Propagation delay	Waveform 1		30		25		12	ns
t _{PHL} Clock to outputs			35		25		17	
t _{PLH} Propagation delay	Waveform 3		25		30		15	ns
t _{PHL} MR to outputs			35		30		22	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

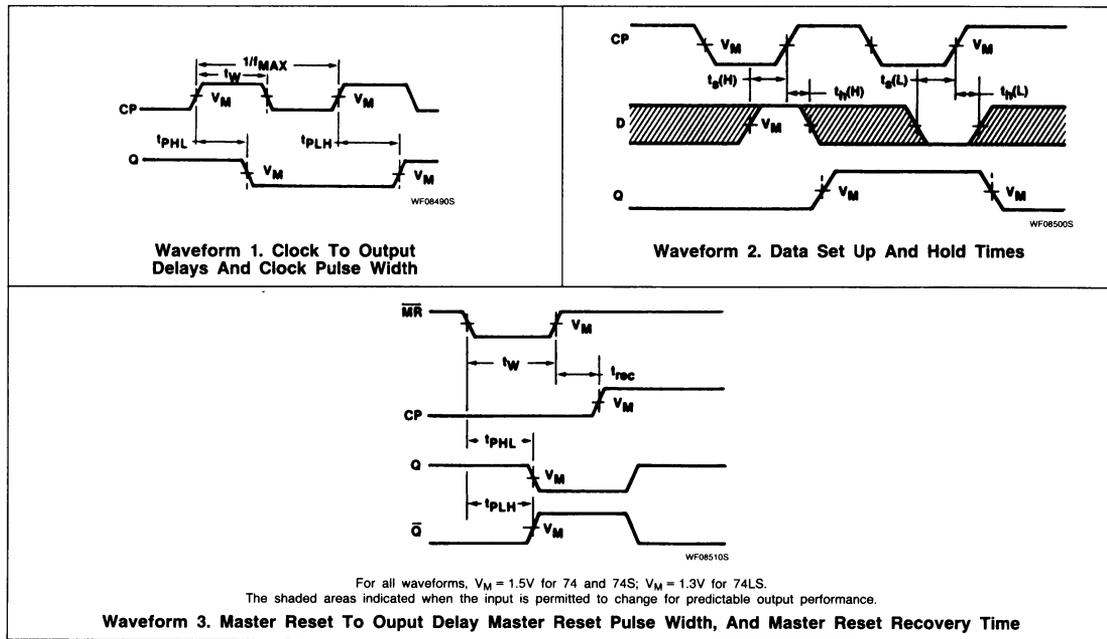
Flip-Flops

74175, LS175, S175

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT	
		Min	Max	Min	Max	Min	Max		
t_w	Clock pulse width	Waveform 1		20		20		7	ns
t_w	Master Reset pulse width	Waveform 3		20		20		10	ns
$t_s(H)$	Set-up time, HIGH data to CP	Waveform 2		20		20		5	ns
$t_h(H)$	Hold time, HIGH data to CP	Waveform 2		5		5		3	ns
$t_s(L)$	Set-up time, LOW data to CP	Waveform 2		20		20		5	ns
$t_h(L)$	Hold time, LOW data to CP	Waveform 2		5		5		3	ns
t_{rec}	Recovery time, \overline{MR} to CP	Waveform 3		25		25		5	ns

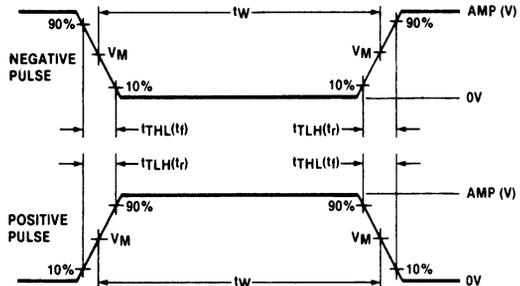
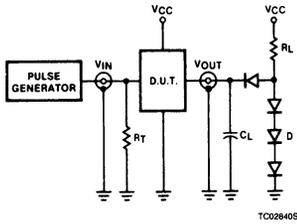
AC WAVEFORMS



Flip-Flops

74175, LS175, S175

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74180

Parity Generator/Checker

9-Bit Odd/Even Parity Generator/Checker
Product Specification

Logic Products

FEATURES

- Word length easily expanded by cascading
- Generate even or odd parity
- Checks for parity errors
- See '280 for faster parity checker

DESCRIPTION

The '180 is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even and Odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bits.

True active-HIGH or true active-LOW parity can be generated at both the Even and Odd outputs. True active-HIGH parity is established with Even Parity enable input (P_E) set HIGH and the Odd Parity enable input (P_O) set LOW. True active-LOW parity is established when P_E is LOW and P_O is HIGH. When both enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

Parity checking of a 9-bit word (8 bits plus parity) is possible by using the two

TYPE	TYPICAL PROPAGATION DELAY, $P_O = 0V$	TYPICAL SUPPLY CURRENT
74180	36ns	34mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74180N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
$I_0 - I_7$	Data inputs	1ul
P_E, P_O	Parity inputs	2ul
Σ_E, Σ_O	Parity outputs	10ul

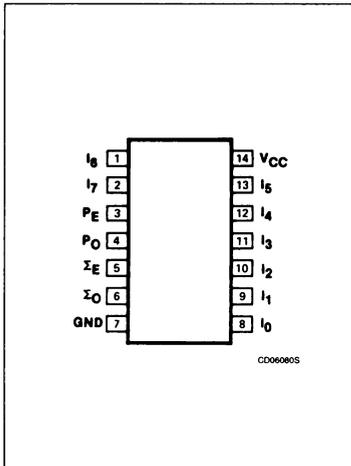
NOTE:

A 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

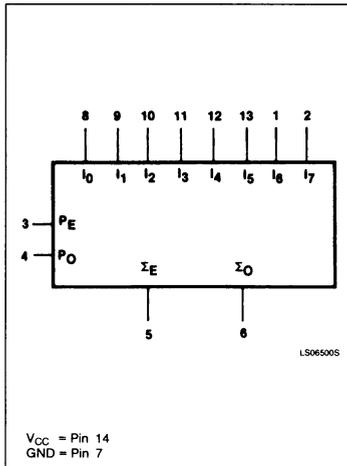
enable inputs plus an inverter as the ninth data input. To check for true active-HIGH parity, the ninth data input is tied to the P_O input and an inverter is connected between the P_O and P_E inputs. To check for true active-LOW parity, the ninth data input is tied to the P_E input and an inverter is connected between the P_E and P_O inputs.

Expansion to larger word sizes is accomplished by serially cascading the '180 in 8-bit increments. The Even and Odd parity outputs of the first stage are connected to the corresponding P_E and P_O inputs, respectively, of the succeeding stage.

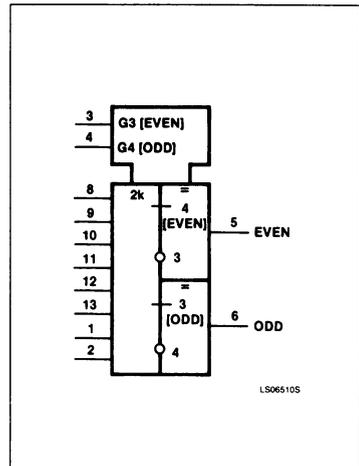
PIN CONFIGURATION



LOGIC SYMBOL



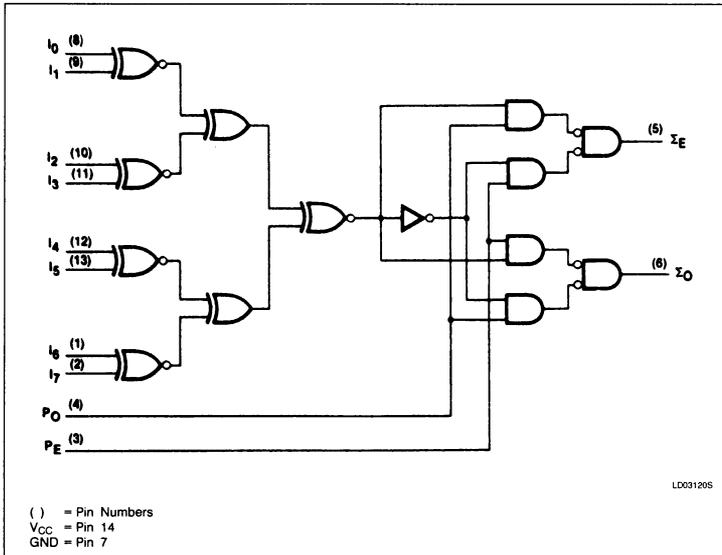
LOGIC SYMBOL (IEEE/IEC)



Parity Generator/Checker

74180

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS		
Number of HIGH Data Inputs (I ₀ - I ₇)	P _E	P _O	Σ _E	Σ _O
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
I _{OH} HIGH-level output current			-800	μA
I _{OL} LOW-level output current			16	mA
T _A Operating free-air temperature	0		70	°C

Parity Generator/Checker

74180

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74180			UNIT
		Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.3		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.4V	I _O - I ₇ inputs		40	μA
		P _E , P _O inputs		80	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V	I _O - I ₇ inputs		-1.6	mA
		P _{OE} , P _O inputs		-3.2	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-55	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		34	56	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with P_E and P_O inputs at 4.5V, all other inputs and outputs open.

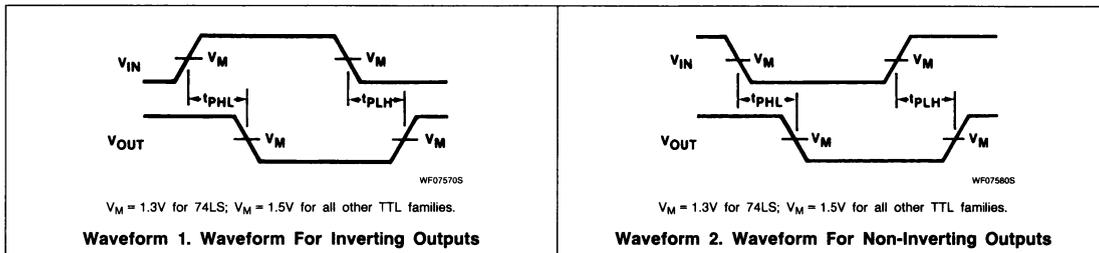
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to even output Waveforms 1 & 2, P _O = 0V		60 68	ns
t _{PLH} t _{PHL}	Propagation delay Data to odd output Waveforms 1 & 2, P _O = 0V		48 38	ns
t _{PLH} t _{PHL}	Propagation delay Data to even output Waveforms 1 & 2, P _E = 0V		48 38	ns
t _{PLH} t _{PHL}	Propagation delay Data to odd output Waveforms 1 & 2, P _E = 0V		60 68	ns
t _{PLH} t _{PHL}	Propagation delay P _E or P _O to output Waveform 1		20 10	ns

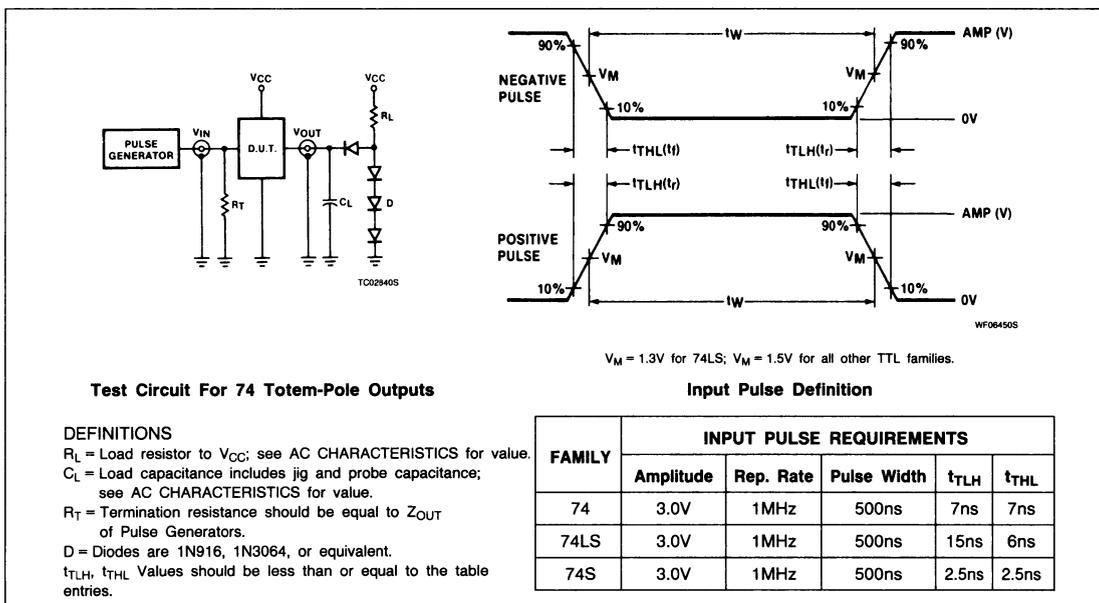
Parity Generator/Checker

74180

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74181, LS181, S181 Arithmetic Logic Units

4-Bit Arithmetic Logic Unit
Product Specification

Logic Products

FEATURES

- Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full lookahead carry for high-speed arithmetic operation on long words

DESCRIPTION

The '181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74181	22ns	91mA
74LS181	22ns	21mA
74S181	11ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74181N, N74LS181N, N74S181N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

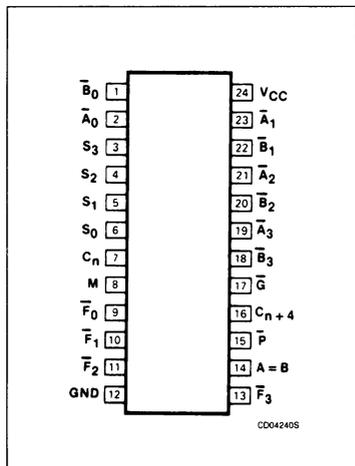
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
Mode	Input	1uI	1Sul	1LSul
\bar{A} or \bar{B}	Inputs	3uI	3Sul	3LSul
S	Inputs	4uI	4Sul	4LSul
Carry	Input	5uI	5Sul	5LSul
$F_0 - F_3, = B, C_{n+4}$	Outputs	10uI	10Sul	10LSul
\bar{G}	Output	10uI	10Sul	40LSul
\bar{P}	Output	10uI	10Sul	20LSul

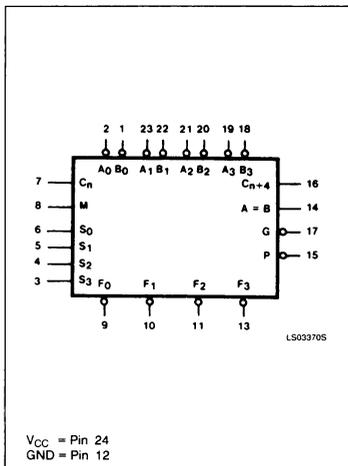
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION

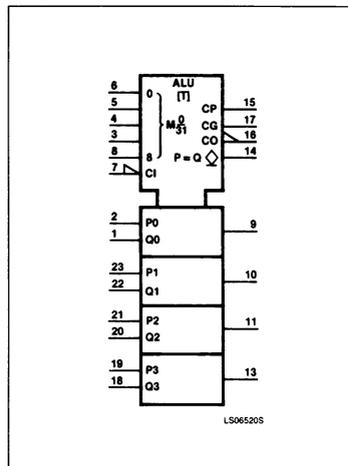


LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



Arithmetic Logic Units

74181, LS181, S181

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals \bar{P} (Carry Propagate) and \bar{G} (Carry Generate). \bar{P} and \bar{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the

'182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four \bar{F} outputs are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

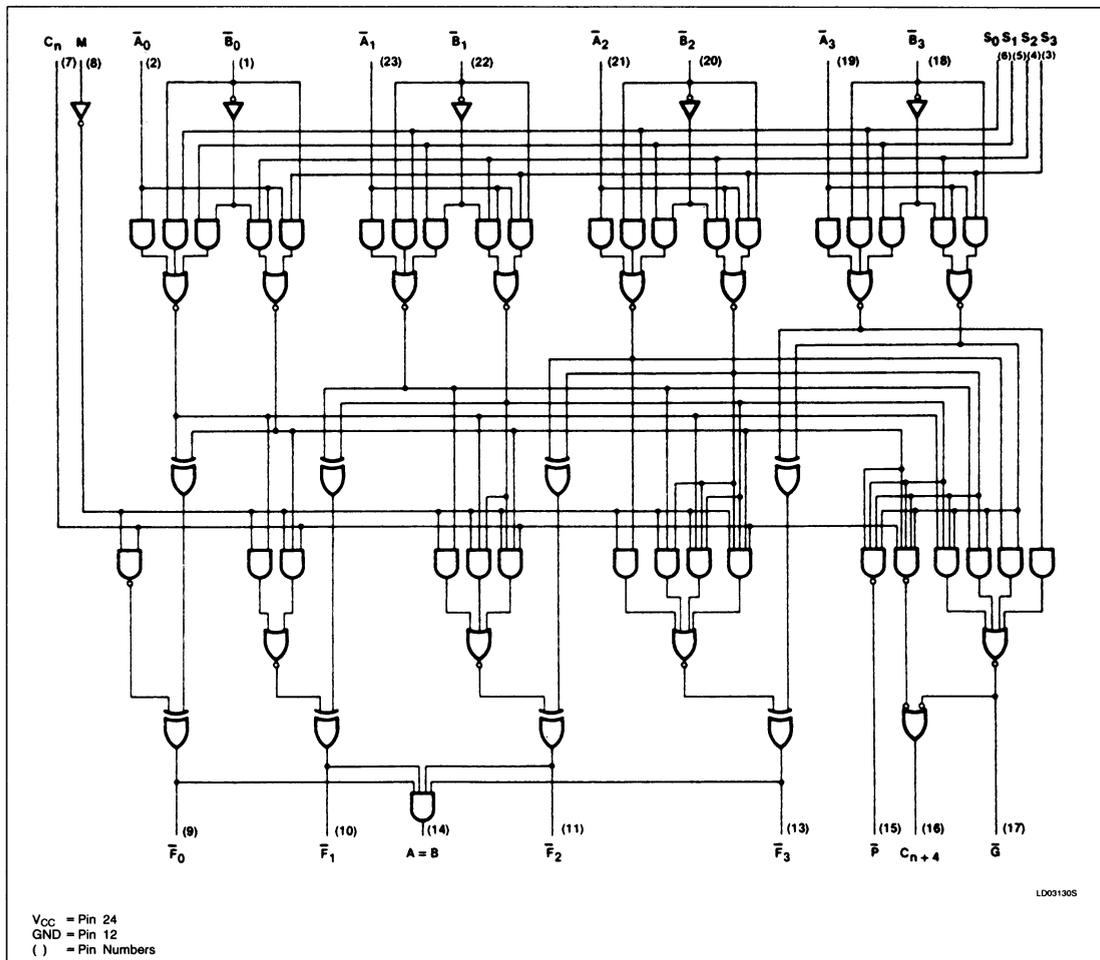
The Function Table lists the arithmetic operations that are performed without a carry in. An

incoming carry adds a one to each operation. Thus, select code LHHH generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM



Arithmetic Logic Units

74181, LS181, S181

MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	Logic (M = H)	Arithmetic** (M = L) (C _n = H)
L	L	L	L	\bar{A}	A
L	L	L	H	$\bar{A} + \bar{B}$	A + B
L	L	L	L	$\bar{A}B$	A + \bar{B}
L	L	H	H	Logical 0	minus 1
L	L	H	L	$\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$
L	H	L	L	\bar{B}	(A + B) plus $\bar{A}\bar{B}$
L	H	L	H	$A \bullet B$	A minus B minus 1
L	H	H	H	$\bar{A}B$	AB minus 1
H	L	L	L	$\bar{A} + B$	A plus AB
H	L	L	H	$\bar{A} \bullet \bar{B}$	A plus B
H	L	H	L	B	(A + \bar{B}) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	A + \bar{B}	(A + B) plus A
H	H	H	L	A + B	(A + \bar{B}) plus A
H	H	H	H	A	A minus 1

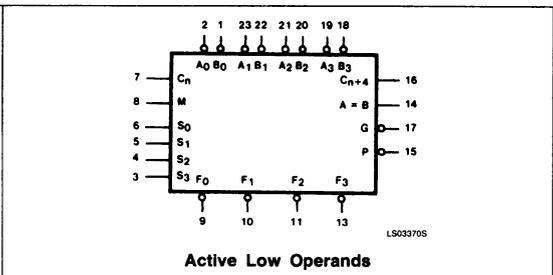
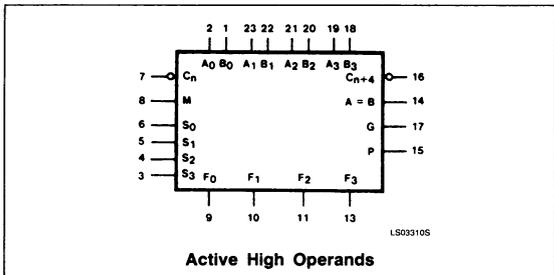
MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	Logic (M = H)	Arithmetic** (M = L) (C _n = L)
L	L	L	L	\bar{A}	A minus 1
L	L	L	H	$\bar{A}\bar{B}$	AB minus 1
L	L	L	H	$\bar{A} + B$	$\bar{A}\bar{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	L	H	L	$\bar{A} + \bar{B}$	A plus (A + \bar{B})
L	H	L	L	\bar{B}	AB plus (A + \bar{B})
L	H	L	H	$\bar{A} \bullet B$	A minus B minus 1
L	H	H	H	A + \bar{B}	A + \bar{B}
H	L	L	L	$\bar{A}\bar{B}$	A plus (A + B)
H	L	L	H	$\bar{A} \bullet \bar{B}$	A plus B
H	L	H	L	B	$\bar{A}\bar{B}$ (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$\bar{A}\bar{B}$	AB plus A
H	H	H	L	AB	$\bar{A}\bar{B}$ plus A
H	H	H	H	A	A

L = LOW voltage

H = HIGH voltage level

*Each bit is shifted to the next more significant position.

**Arithmetic operations expressed in 2s complement notation.



Arithmetic Logic Units

74181, LS181, S181

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18			-18	mA
I _{OH}	HIGH-level output current			-800			-400			-1000	μA
I _{OL}	LOW-level output current			16			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	0		70	°C



SUM MODE TEST TABLE I

FUNCTION INPUTS: S₀ = S₃ = 4.5V, S₁ = S₂ = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	C _n + 4
t _{PLH} t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	C _n + 4
t _{PLH} t _{PHL}	C _n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C _n + 4

Arithmetic Logic Units

74181, LS181, S181

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	$A = B$
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	$A = B$
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	C_{n+4}
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All \bar{A} and \bar{B}	None	Any \bar{F} or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

Arithmetic Logic Units

74181, LS181, S181

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74181			74LS181			74S181			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Any output except A = B	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX All outputs		0.2	0.4		0.35	0.5			0.5	V
		I _{OL} = 4mA					0.25	0.4				V
		I _{OL} = 16mA G output					0.47	0.7				V
		I _{OL} = 8mA P output					0.35	0.5				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	Mode input			1.0			0.1			1.0	mA
		A or B inputs			1.0			0.3			1.0	mA
		S inputs			1.0			0.4			1.0	mA
		Carry input			1.0			0.5			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	Mode input		40							μA
			A or B inputs		120							μA
			S inputs		160							μA
			Carry input		200							μA
	V _I = 2.7V	Mode input						20			50	μA
		A or B inputs						60			150	μA
		S inputs						80			200	μA
		Carry input						100			250	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	Mode input		-1.6			-0.4				mA
			A or B inputs		-4.8			-1.2				mA
			S inputs		-6.4			-1.6				mA
			Carry input		-8			-2				mA
	V _I = 0.5V	Mode input									-2	mA
		A or B inputs									-6	mA
		S inputs									-8	mA
		Carry input									-10	mA
I _{OH} HIGH-level output current	V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V, A = B only			250			100			250	μA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX Any output except A = B	-18		-57	-15		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Note 4a		88	140		20	34		120	220	mA
		Note 4b		94	150		21	37		120	220	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with the following conditions: a. S₀ through S₃, M, and A inputs are at 4.5V, other inputs grounded, all outputs open. b. S₀ through S₃ and M inputs are at 4.5V, other inputs grounded, all outputs open.

Arithmetic Logic Units

74181, LS181, S181

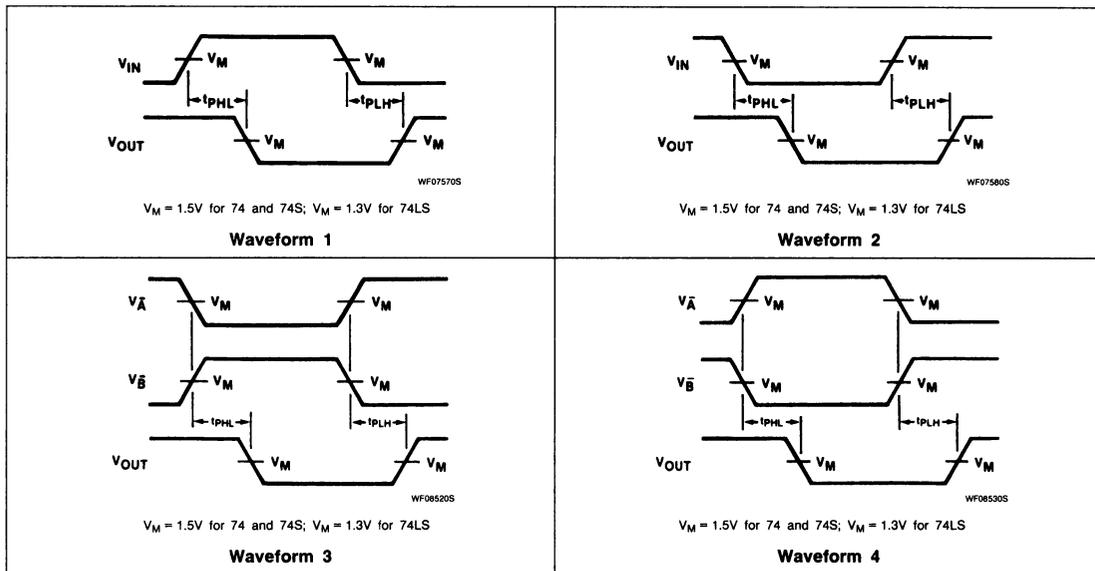
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74		74LS		74S		UNIT
			$C_L = 15\text{pF}$ $R_L = 400\Omega$		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	$M = 0\text{V}$, Sum or Diff Mode see Waveform 2 and Tables I & II		18 19		27 20		10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to \bar{F} outputs	$M = 0\text{V}$, Sum or Diff Mode see Waveform 2 and Tables I & II		19 18		26 20		12 12	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{G} output	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		19 19		29 23		12 12	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{G} output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		25 25		32 32		15 15	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{P} output	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		19 25		30 30		12 12	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{P} output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		25 25		30 33		15 15	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		42 32		32 20		16.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		48 34		32 32		20 22	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	$M = 4.5\text{V}$, Logic Mode see Waveform 2 and Table III		48 34		33 38		20 22	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to C_{n+4} output	$M = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$, $S_1 = S_2 = 0\text{V}$ Sum Mode, see Waveform 1 and Table I		43 41		38 38		18.5 18.5	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to C_{n+4} outputs	$M = 0\text{V}$, $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 4 and Table II		50 50		41 41		23 23	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to $A = B$ output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		50 48		50 62		23 30	ns

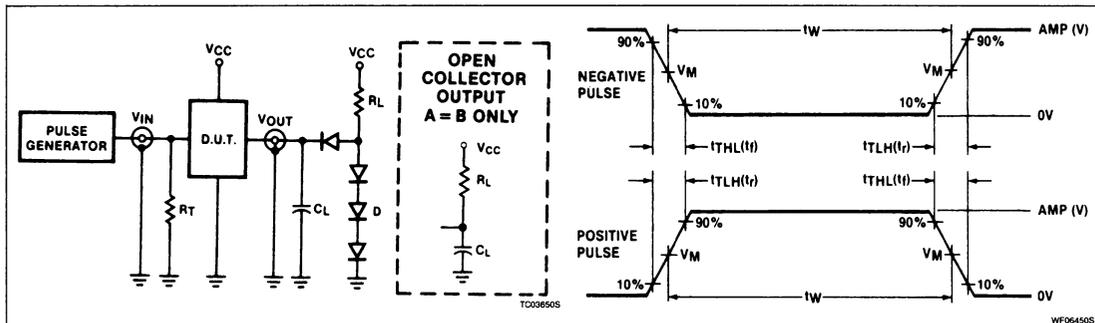
Arithmetic Logic Units

74181, LS181, S181

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74S182

Carry Generator

Lookahead Carry Generator
Product Specification

Logic Products

FEATURES

- Provides carry lookahead across a group of four ALU's
- Multi-level lookahead for high-speed arithmetic operation over long word lengths

DESCRIPTION

The '182 carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\bar{P}_0, \bar{P}_1, \bar{P}_2, \bar{P}_3$) and Carry Generate ($\bar{G}_0, \bar{G}_1, \bar{G}_2, \bar{G}_3$) signals and an active HIGH Carry input (C_n) and provides anticipated active HIGH carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The '182 also has active LOW Carry Propagate (\bar{P}) and Carry Generate (\bar{G}) outputs which may be used for further levels of lookahead.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S182	5.8ns	69mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S182N
Plastic SO-16	N74S182D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

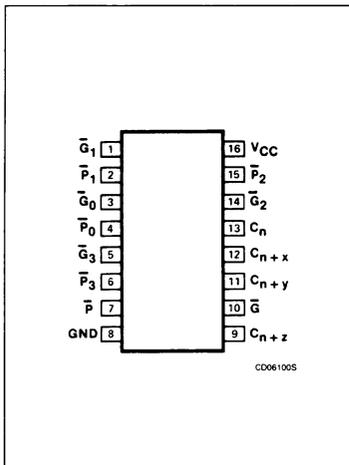
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
C_n	Input	1Sul
\bar{P}_3	Input	2Sul
\bar{P}_2	Input	3Sul
$\bar{P}_0, \bar{P}_1, \bar{G}_3$	Inputs	4Sul
\bar{G}_0, \bar{G}_2	Inputs	7Sul
\bar{G}_1	Input	8Sul
All	Outputs	10Sul

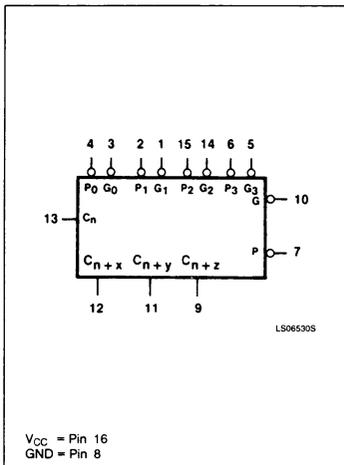
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

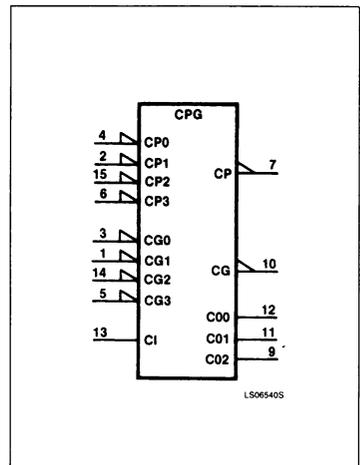
PIN CONFIGURATION



LOGIC SYMBOL



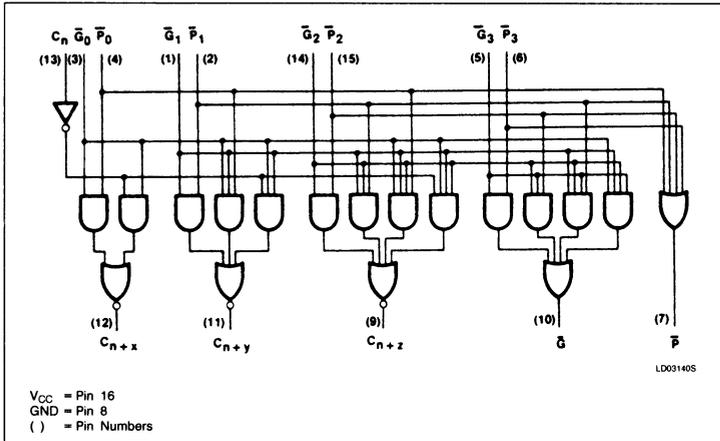
LOGIC SYMBOL (IEEE/IEC)



Carry Generator

74S182

LOGIC DIAGRAM



The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$

$$C_{n+y} = G_1 + P_1G_0 = P_1P_0C_n$$

$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0$$

$$\bar{G} = \bar{G}_3 + P_3\bar{G}_2 + P_3P_2\bar{G}_1 + P_3P_2P_1\bar{G}_0$$

$$\bar{P} = \bar{P}_3\bar{P}_2\bar{P}_1\bar{P}_0$$

The '182 can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	\bar{G}_0	\bar{P}_0	\bar{G}_1	\bar{P}_1	\bar{G}_2	\bar{P}_2	\bar{G}_3	\bar{P}_3	C_{n+x}	C_{n+y}	C_{n+z}	\bar{G}	\bar{P}
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X	H	X				L			
X	X	X	X	X	L	X				L			
X	X	X	L	X	X	L				H			
X	L	X	X	L	X	L				H			
H	X	L	X	L	X	L				H			
	X		X	X	X	X	H	H				H	
	X		X	X	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

Carry Generator

74S182

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74S			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-1000	μA
I _{OL}	LOW-level output current			20	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74S182			UNIT
			Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			0.5	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	C _n input		50	μA
			\bar{P}_3 input		100	μA
			\bar{P}_2 input		150	μA
			$\bar{P}_0, \bar{P}_1, \bar{G}_3$ inputs		200	μA
			\bar{G}_0, \bar{G}_2 inputs		350	μA
			\bar{G}_1 input		400	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.5V	C _n input		-2	mA
			\bar{P}_3 input		-4	mA
			\bar{P}_2 input		-6	mA
			$\bar{P}_0, \bar{P}_1, \bar{G}_3$ inputs		-8	mA
			\bar{G}_0, \bar{G}_2 inputs		-14	mA
			\bar{G}_1 input		-16	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-40		-100	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX		69	109	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

4. I_{CC} is measured with \bar{G}_0, \bar{G}_1 and \bar{G}_2 inputs at 4.5V, all other inputs grounded and all outputs open.

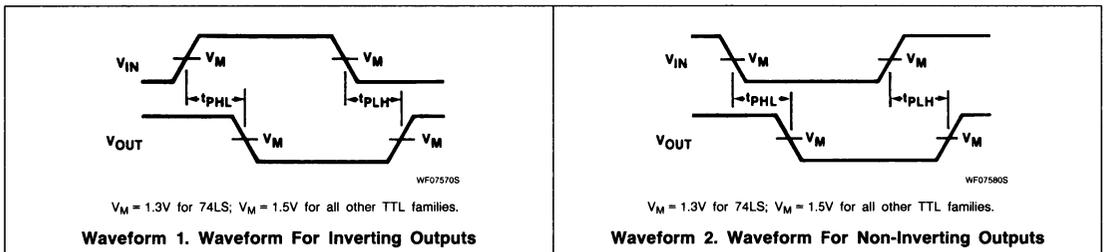
Carry Generator

74S182

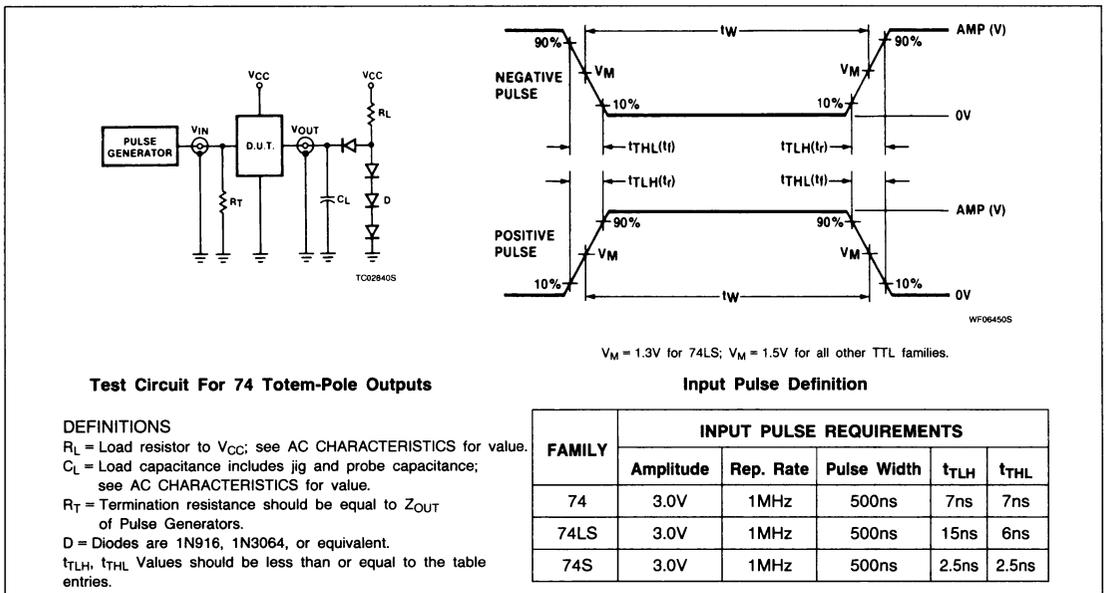
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay \bar{G}_n or \bar{P}_n to any C output	Waveform 1	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay \bar{G}_n or \bar{P}_n to \bar{G} output	Waveform 2	7.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay \bar{P}_n to \bar{P} output	Waveform 2	6.5 10	ns
t_{PLH} t_{PHL}	Propagation delay C_n to any C output	Waveform 2	10 10.5	ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74190, 191, LS191 Counters

'190 Presettable BCD/Decade Up/Down Counter
'191 Presettable 4-Bit Binary Up/Down Counter
Product Specification

Logic Products

FEATURES

- Synchronous, reversible counting
- BCD/decade—'190
4-bit binary—'191
- Synchronous, reversible counting
- Asynchronous parallel load capability
- Count enable control for synchronous expansion
- Single Up/Down control input

DESCRIPTION

The '190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The '191 is similar, but is a 4-bit binary counter.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74190	25MHz	65mA
74191	25MHz	65mA
74LS191	25MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74190N, N74191N, N74LS191N
Plastic SOL-16	N74LS191D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

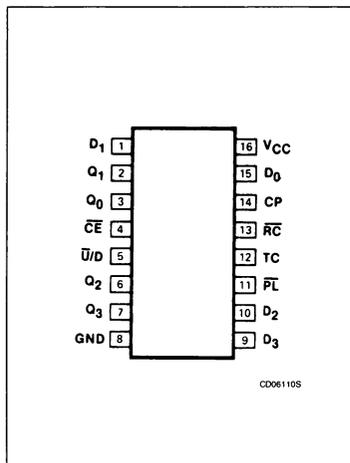
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S
\overline{CE}	Input	3ul	3LSul
Other	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

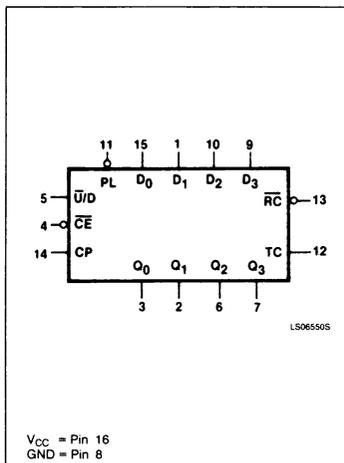
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

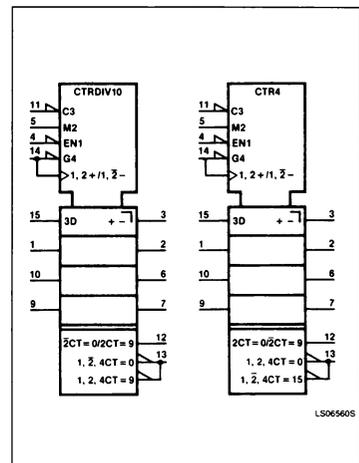
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Counters

74190, 191, LS191

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the Parallel Load (\overline{PL}) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable (\overline{CE}) input. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U/D}$) input signal determines the direction of counting as indicated in the Mode Select Table. The \overline{CE} input may go LOW when the clock is in either state, however, the LOW-to-HIGH \overline{CE} transition must occur only when the clock is HIGH. Also, the $\overline{U/D}$ input should be changed only when either \overline{CE} or CP is HIGH.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock (\overline{RC}). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode for 74190,

and reaches "15" in the count-up mode for 74191/74LS191. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U/D}$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the \overline{RC} output. When TC is HIGH and \overline{CE} is LOW, the RC follows the Clock Pulse (CP) delayed by two gate delays. The \overline{RC} output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multi-stage counters, as indicated in Figures A and B. In Figure A, each \overline{RC} output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it

ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The \overline{RC} outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the \overline{CE} input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own \overline{CE} , therefore, the simple inhibit scheme of Figure A and B does not apply.

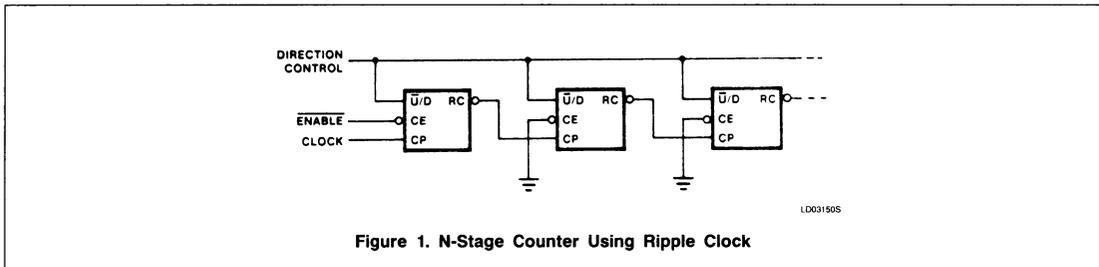


Figure 1. N-Stage Counter Using Ripple Clock

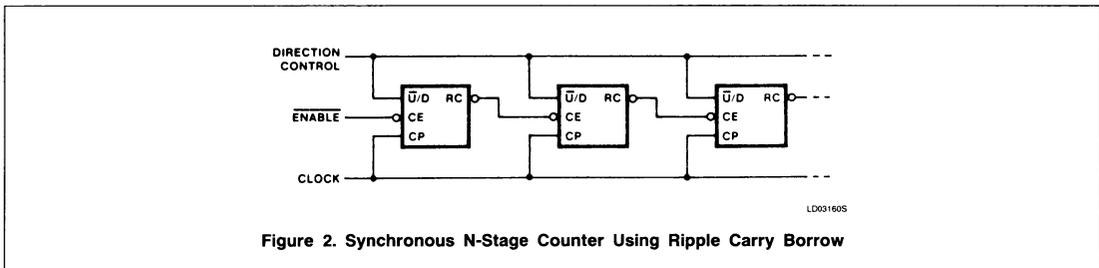


Figure 2. Synchronous N-Stage Counter Using Ripple Carry Borrow

Counters

74190, 191, LS191

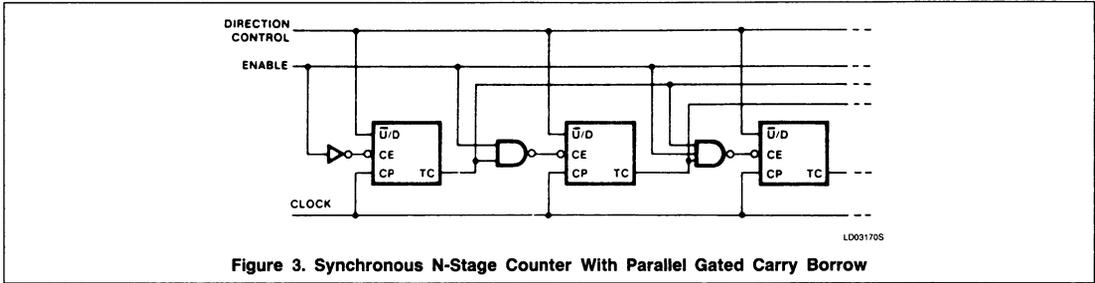
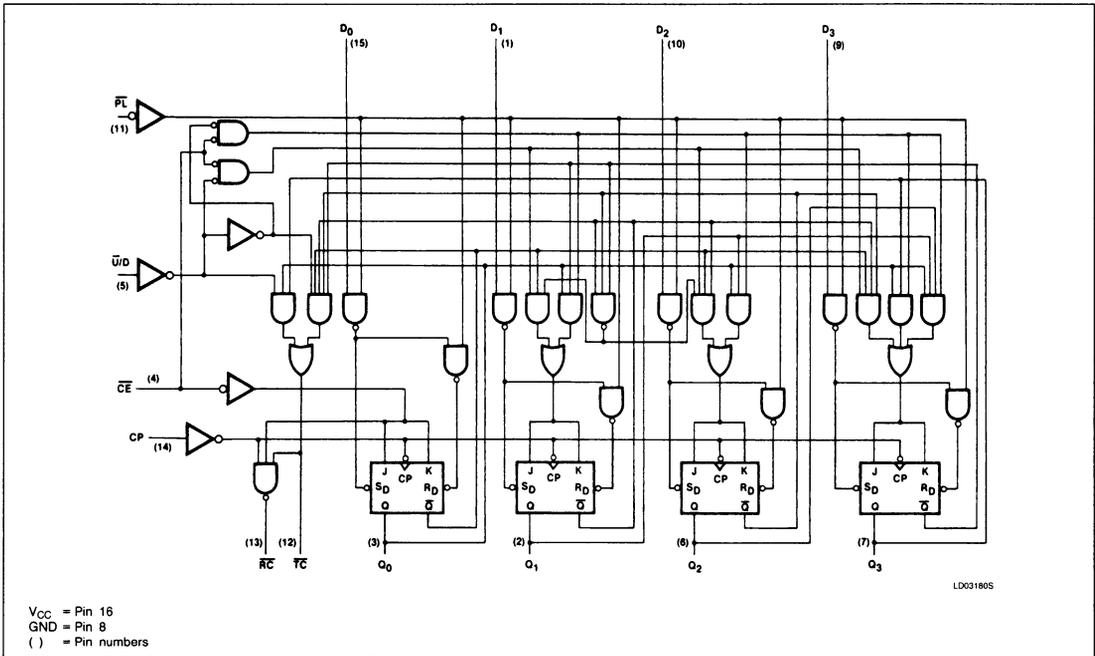


Figure 3. Synchronous N-Stage Counter With Parallel Gated Carry Borrow

LOGIC DIAGRAM '190

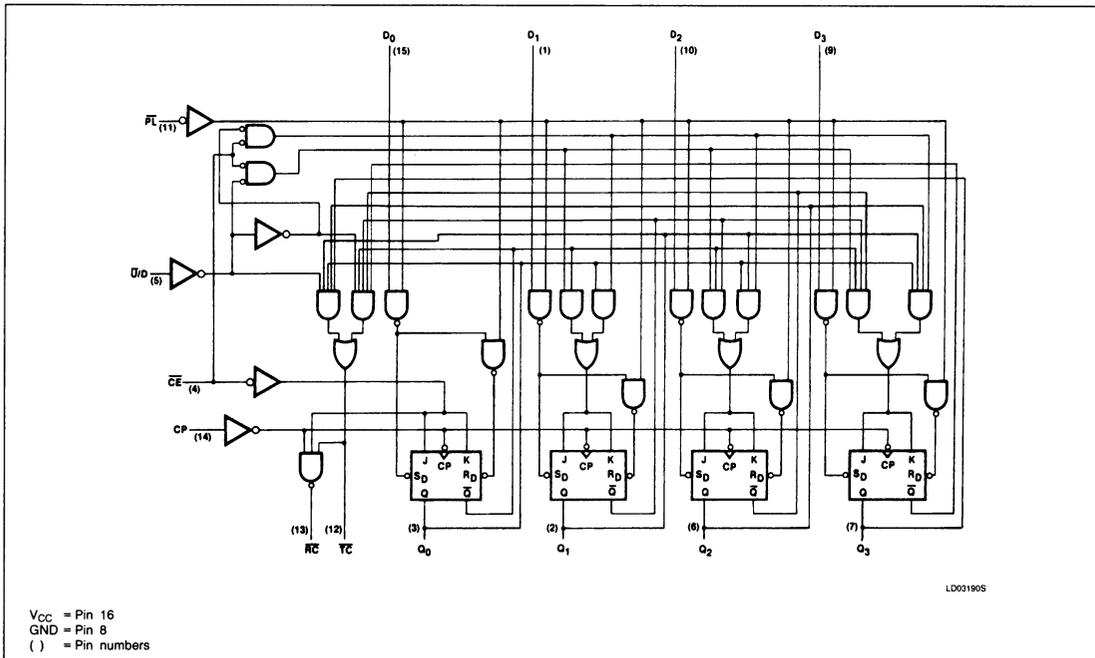


V_{CC} = Pin 16
 GND = Pin 8
 () = Pin numbers

Counters

74190, 191, LS191

LOGIC DIAGRAM '191



5

MODE SELECT — FUNCTION TABLE, '190, '191

OPERATING MODE	INPUTS					OUTPUTS
	P̄L	U/D	CĒ	CP	D _n	Q _n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	I	↑	X	count up
Count down	H	H	I	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND R̄C FUNCTION TABLE, '190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	CĒ	CP	Q ₀	Q ₁	Q ₂	Q ₃	TC	R̄C
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⌊	H	X	X	H	⌋	⌋
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌋	L	L	L	L	⌋	⌋

Counters

74190, 191, LS191

TC AND \overline{RC} FUNCTION TABLE, '191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	\overline{CE}	CP	Q ₀	Q ₁	Q ₂	Q ₃	TC	\overline{RC}
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	\downarrow	H	H	H	H	\downarrow	\downarrow
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	\downarrow	L	L	L	L	\downarrow	\downarrow

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

1 = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

X = Don't care.

 \uparrow = LOW-to-HIGH clock transition. \downarrow = LOW pulse. \downarrow = TC goes LOW on a LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-800			-400	μA
I _{OL}	LOW-level output current			16			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

Counters

74190, 191, LS191

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74190, 191			74LS191			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MIN, I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V	
		I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	C _E input					0.3	mA
			Other inputs					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	C _E input			120		μA	
			Other inputs			40		μA	
		V _I = 2.7V	C _E input					60	μA
			Other inputs					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	C _E input			-4.8		-1.2	mA
			Other inputs			-1.6		-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-65	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		65	105		20	35	mA	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

Counters

74190, 191, LS191

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum input count frequency	Waveform 1	20		20		MHz
t_{PLH} Propagation delay t_{PHL} Clock to Q output	Waveform 1		24 36		24 36	ns
t_{PLH} Propagation delay t_{PHL} Clock to $\overline{\text{RC}}$ output	Waveform 2		20 24		20 24	ns
t_{PLH} Propagation delay t_{PHL} Clock to TC output	Waveform 1		42 52		42 52	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{U/D}}$ to $\overline{\text{RC}}$ output	Waveform 7		45 45		45 45	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{U/D}}$ to TC output	Waveform 7		33 33		33 33	ns
t_{PLH} Propagation delay t_{PHL} Data to Q outputs	Waveform 3		22 50		32 40	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{PL}}$ to any output	Waveform 4		33 50		33 50	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CE}}$ to $\overline{\text{RC}}$ output	Waveform 2		33 33		33 33	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

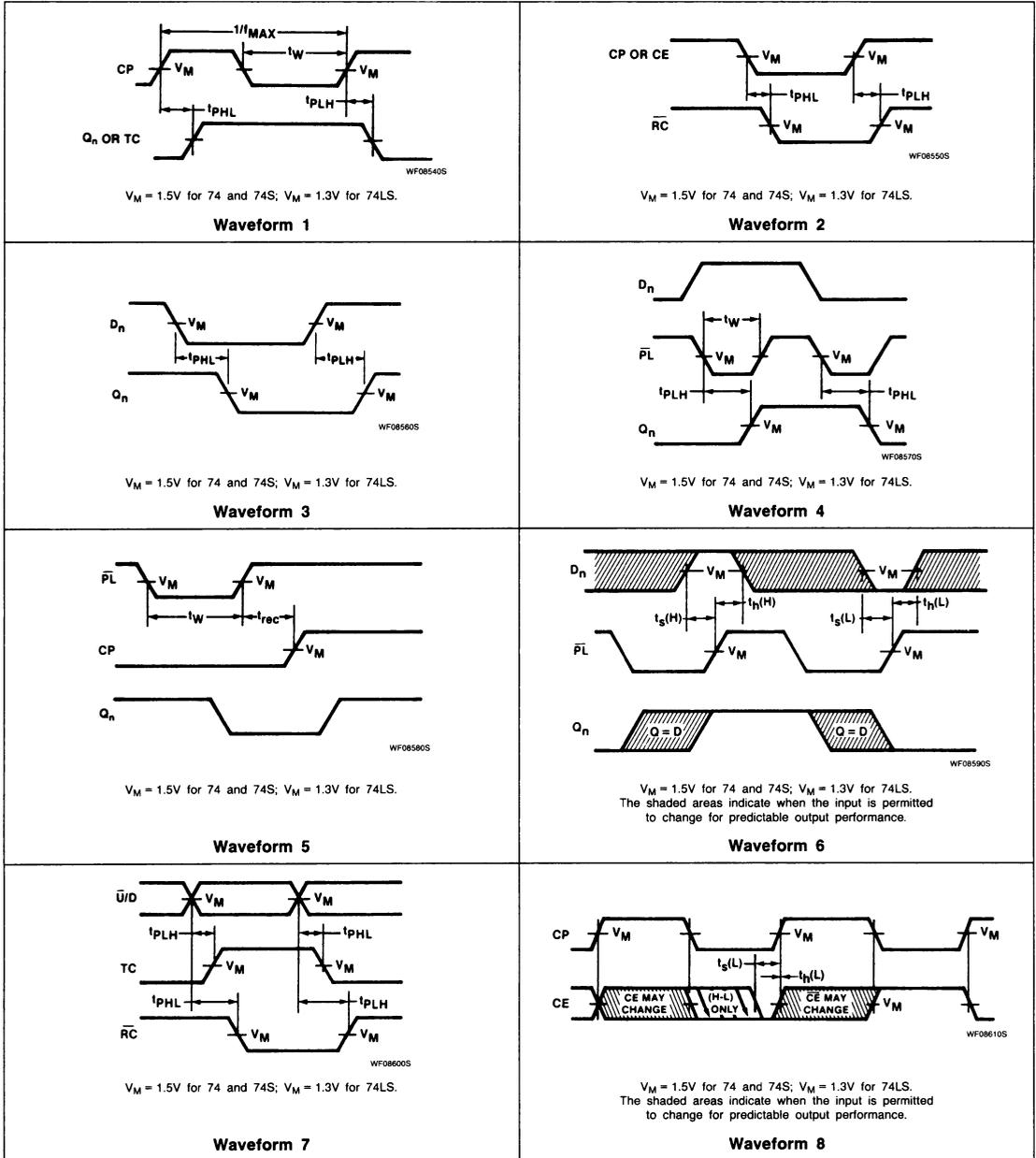
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W CP pulse width	Waveform 1	25		25		ns
t_W $\overline{\text{PL}}$ pulse width	Waveform 5	35		35		ns
t_s Set-up time, data to $\overline{\text{PL}}$	Waveform 6	20		20		ns
t_h Hold time, data to $\overline{\text{PL}}$	Waveform 6	4		5		ns
t_{rec} Recovery time, $\overline{\text{PL}}$ to CP	Waveform 5	40		40		ns
$t_s(\text{L})$ Set-up time, LOW $\overline{\text{CE}}$ to clock	Waveform 8	40		40		ns
$t_h(\text{L})$ Hold time, LOW $\overline{\text{CE}}$ to clock	Waveform 8	0		0		ns

Counters

74190, 191, LS191

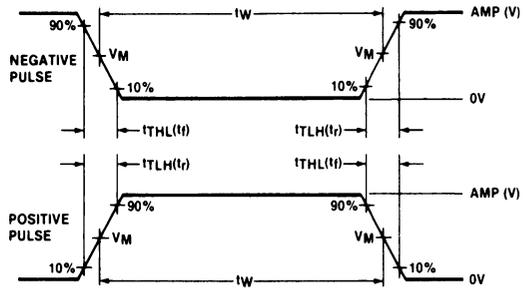
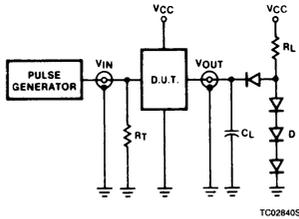
AC WAVEFORMS



Counters

74190, 191, LS191

TEST CIRCUITS AND WAVEFORMS



WF064505

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74192, 74193, LS192, LS193 Counters

'192 Presettable BCD Decade Up/Down Counter

'193 Presettable 4-Bit Binary Up/Down Counter

Product Specification

Logic Products

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset (clear)
- Expandable without external logic

DESCRIPTION

The '192 and '193 are 4-bit synchronous up/down counters — the '192 counts in BCD mode and the '193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up . . . if CP_D is pulsed while the CP_U is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74192	32MHz	65mA
74LS192	32MHz	19mA
74193	32MHz	65mA
74LS193	32MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74192N, N74LS192N, N74193N, N74LS193N
Plastic SO	N74LS193D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

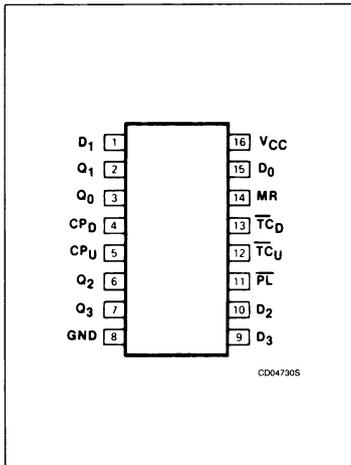
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

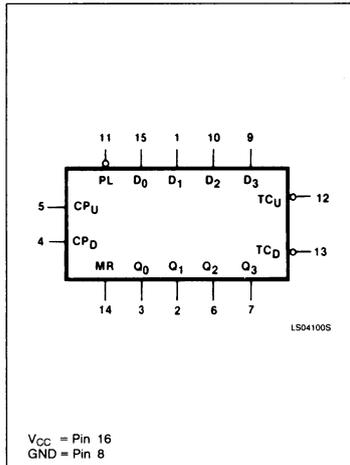
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION

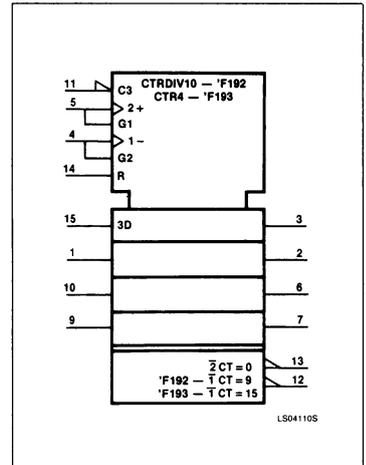


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



Counters

74192, 74193, LS192, LS193

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CPU_D input will advance the count by one.

One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the

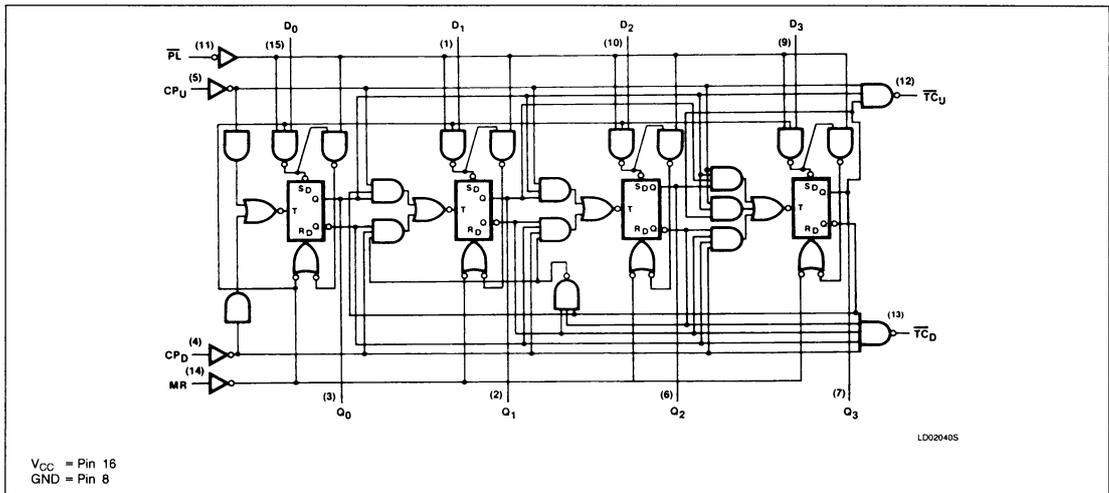
activating clock is HIGH to avoid erroneous counts.

The Terminal Count Up (\overline{TC}_U) and Terminal Count down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state of 9 (for the '192 and 15 for the '193), the next HIGH-to-LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, duplicating the count up clock, although delayed by two gate delays. Likewise, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The \overline{TC} outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-

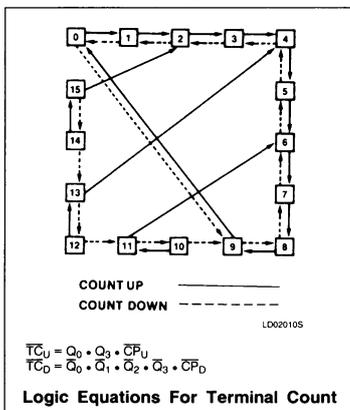
gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D₀ - D₃) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load (\overline{PL}) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs LOW. If one of the Clock input is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM, '192



STATE DIAGRAM, '192



MODE SELECT — FUNCTION TABLE, '192

OPERATING MODE	INPUTS								OUTPUTS					
	MR	PL	CP _U	CP _D	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q ₃	\overline{TC}_U	\overline{TC}_D
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	H	X	H	X	X	H	Q _n = D _n		L	L	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H ^(a)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H ^(b)

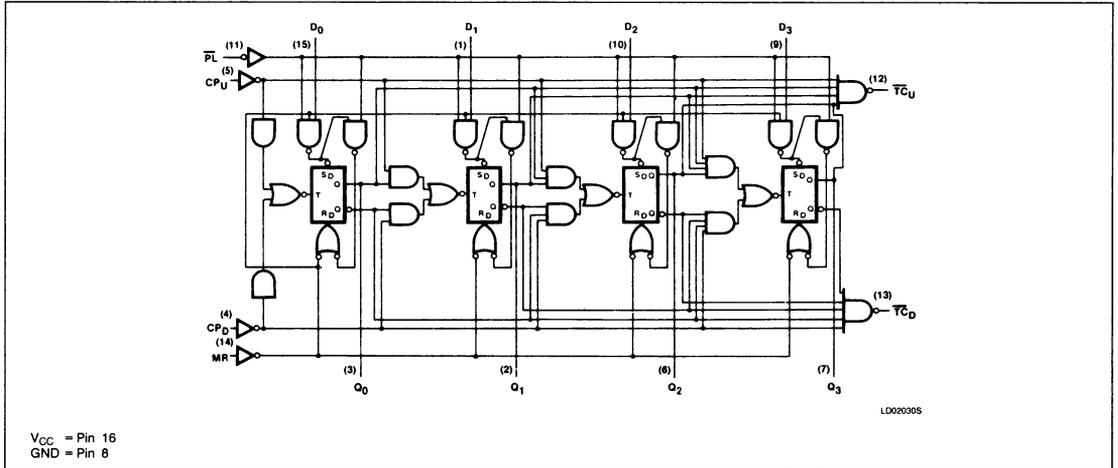
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

NOTES:
 a. $\overline{TC}_U = CP_U$ at terminal count up (HLLH).
 b. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

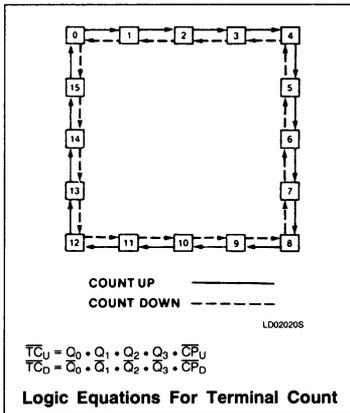
Counters

74192, 74193, LS192, LS193

LOGIC DIAGRAM, '193



STATE DIAGRAM, '193



MODE SELECT — FUNCTION TABLE, '193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	\overline{PL}	CP _U	CP _D	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q ₃	\overline{TC}_U	\overline{TC}_D
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	L	L	L	L	L	H
Count up	L	H	↑	H	X	X	X	X	Count up				H ^(c)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H ^(d)

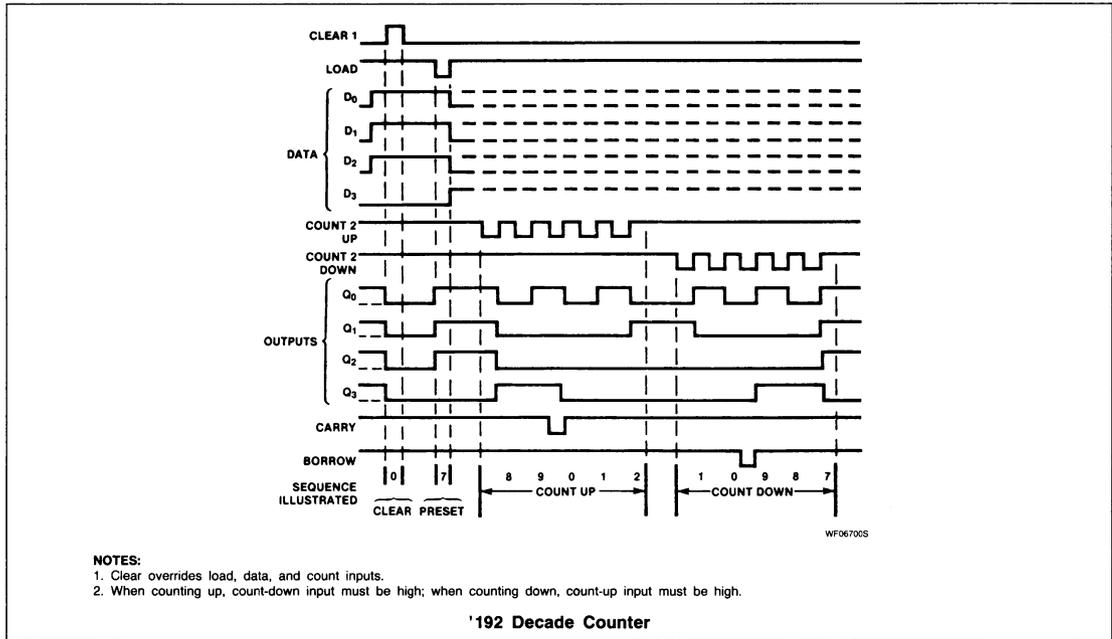
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES:
c. TC_U = CP_U at terminal count up (HHHH).
d. TC_D = CP_D at terminal count down (LLLL).

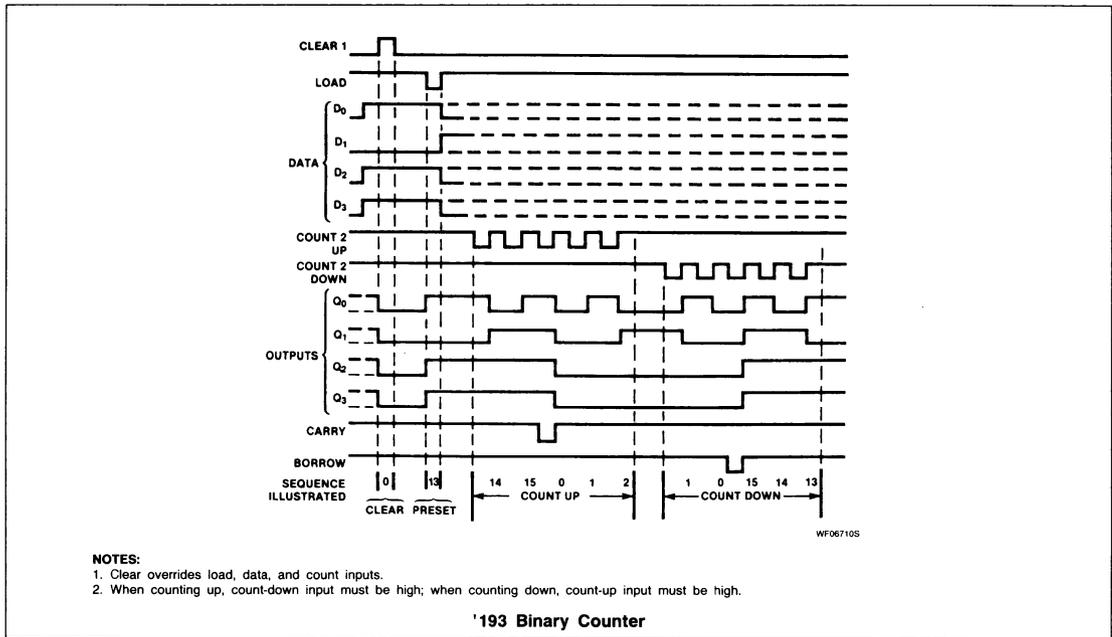
Counters

74192, 74193, LS192, LS193

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



Counters

74192, 74193, LS192, LS193

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-800			-400	mA
I _{OL}	LOW-level output current			16			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74192, '193			74LS192, '193			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4	V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX			0.2	0.4		0.35	0.5	V
		I _{OL} = MAX						0.25	0.4	V
I _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.5	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX				1.0			mA	
		V _I = 5.5V							0.1	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX				40			=mμA	
		V _I = 2.4V							20	=mμA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6		-0.4	mA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-18		-65	-20		mA	
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			65	102		19	34	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Parallel Load and Master Reset inputs grounded, all other outputs at 4.5V and all outputs open.

Counters

74192, 74193, LS192, LS193

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} Propagation delay t_{PHL} CP_U input to \overline{TC}_U output	Waveform 2		26 24		26 24	ns
t_{PLH} Propagation delay t_{PHL} CP_D input to \overline{TC}_D output	Waveform 2		24 24		24 24	ns
t_{PLH} Propagation delay t_{PHL} CP_U or CP_D to Q_n outputs	Waveform 1		38 47		38 47	ns
t_{PLH} Propagation delay t_{PHL} \overline{PL} input to Q_n output	Waveform 3		40 40		40 40	ns
t_{PHL} Propagation delay, MR to output	Waveform 4		35		35	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

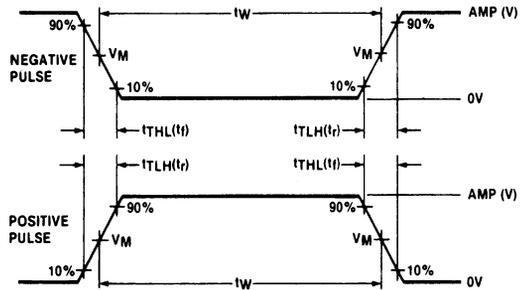
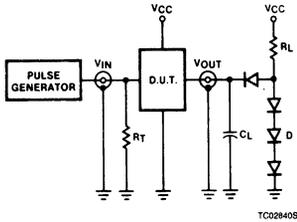
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W CP_U pulse width	Waveform 1	20		20		ns
t_W CP_D pulse width	Waveform 1	20		20		ns
t_W \overline{PL} pulse width	Waveform 3	20		20		ns
t_W MR pulse width	Waveform 4	20		20		ns
t_s Set-up time, data to \overline{PL}	Waveform 5	20		20		ns
t_h Hold time, data to \overline{PL}	Waveform 5	0		5		ns
t_{rec} Recovery time, \overline{PL} to CP	Waveform 3	40		40		ns
t_{rec} Recovery time, MR to CP	Waveform 4	40		40		ns

Counters

74192, 74193, LS192, LS193

TEST CIRCUITS AND WAVEFORMS



WF06450S

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

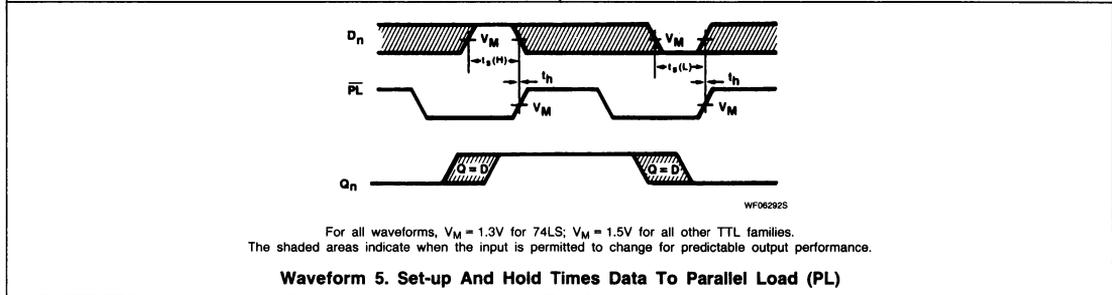
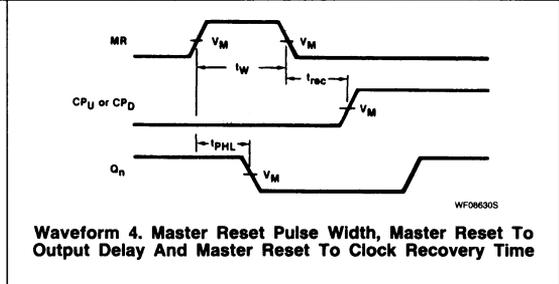
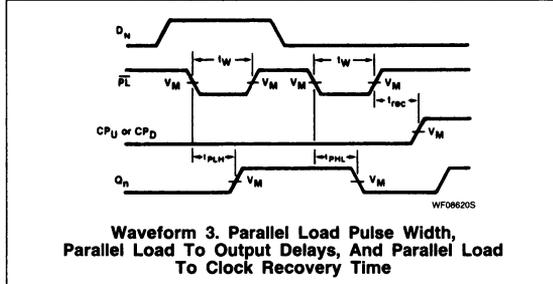
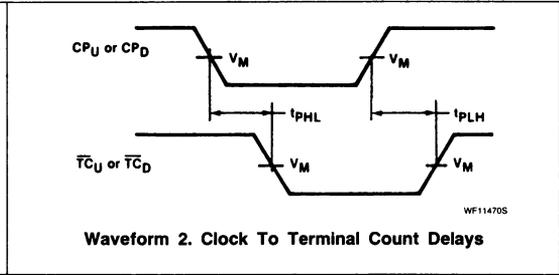
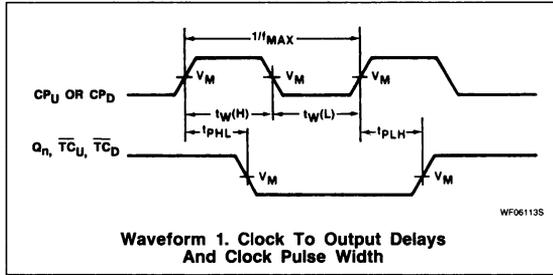
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

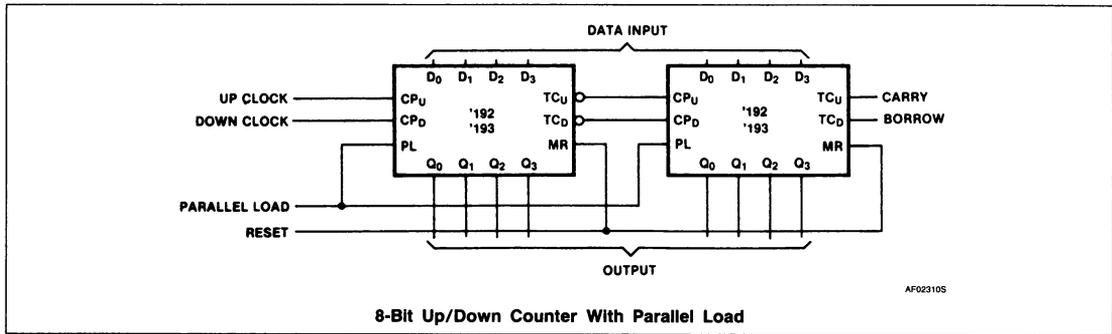
Counters

74192, 74193, LS192, LS193

AC WAVEFORMS



APPLICATION DIAGRAM



74194, LS194A, S194 Shift Registers

4-Bit Bidirectional Universal Shift Register
Product Specification

Logic Products

- Buffered clock and control inputs
- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the '194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74194	36MHz	39mA
74LS194A	36MHz	15mA
74S194	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74194N, N74LS194AN, N74S194N
Plastic SO-16	N74LS194AD, N74S194D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

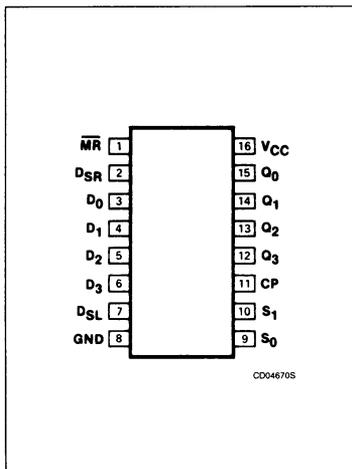
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
$Q_0 - Q_3$	Outputs	10ul	10Sul	10LSul

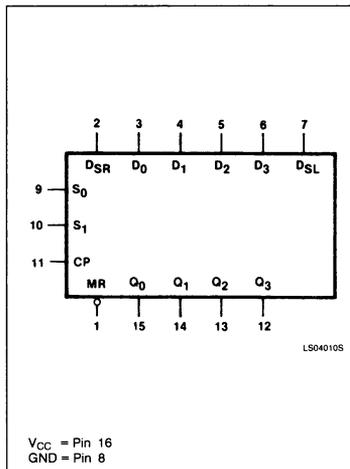
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

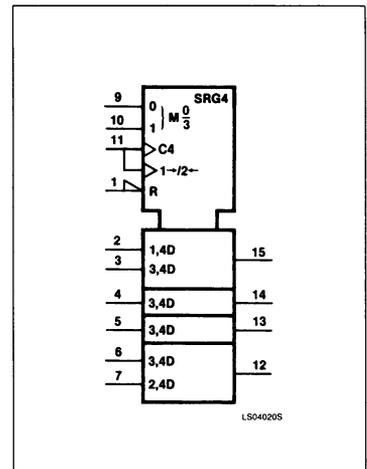
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Shift Registers

74194, LS194A, S194

MODE SELECT — FUNCTION TABLE

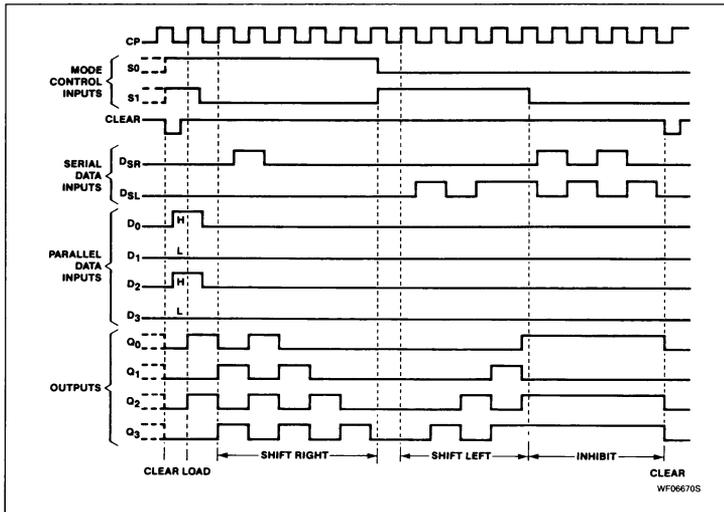
OPERATING MODE	INPUTS							OUTPUTS			
	CP	MR	S ₁	S	D _{SR}	D _{SL}	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	i(a)	i(a)	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift left	↑	H	h	i(a)	X	l	X	q ₁	q ₂	q ₃	L
	↑	H	h	i(a)	X	h	X	q ₁	q ₂	q ₃	H
Shift right	↑	H	i(a)	h	l	X	X	L	q ₀	q ₁	q ₂
	↑	H	i(a)	h	h	X	X	H	q ₀	q ₁	q ₂
Parallel load	↑	H	h	h	X	X	d _n	d ₀	d ₁	d ₂	d ₃

H = HIGH voltage level.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 d_n(q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

NOTE:

a. The HIGH-to-LOW transition of the S₀ and S₁ inputs on the 74194 should only take place while CP is HIGH for conventional operation.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



The '194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S₀ and S₁. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, Q₀ → Q₁, etc.) or, right to left (shift left, Q₃ → Q₂, etc.) or, parallel data can be entered, loading all 4 bits of the register simultaneously. When both S₀ and S₁ are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

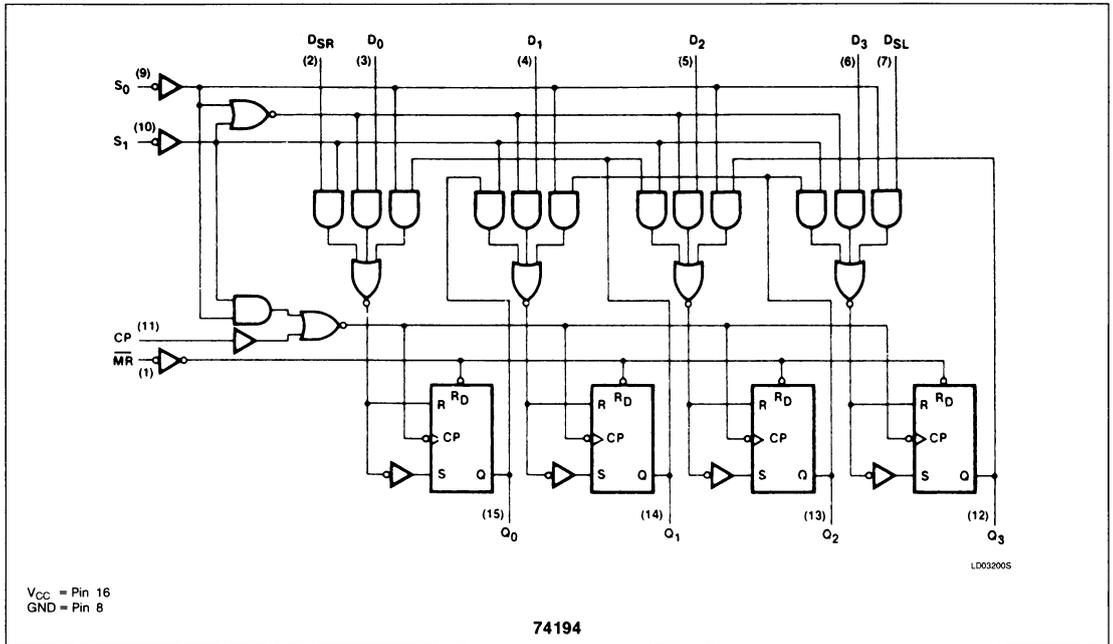
Mode Select and Data inputs on the 74S194 and 74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one set-up time prior to the positive transition of the clock pulse. The Mode Select inputs of the 74194 are gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH.

The four parallel data inputs (D₀ - D₃) are D-type inputs. Data appearing on D₀ - D₃ inputs when S₀ and S₁ are HIGH is transferred to the Q₀ - Q₃ outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset (MR) overrides all other input conditions and forces the Q outputs LOW.

Shift Registers

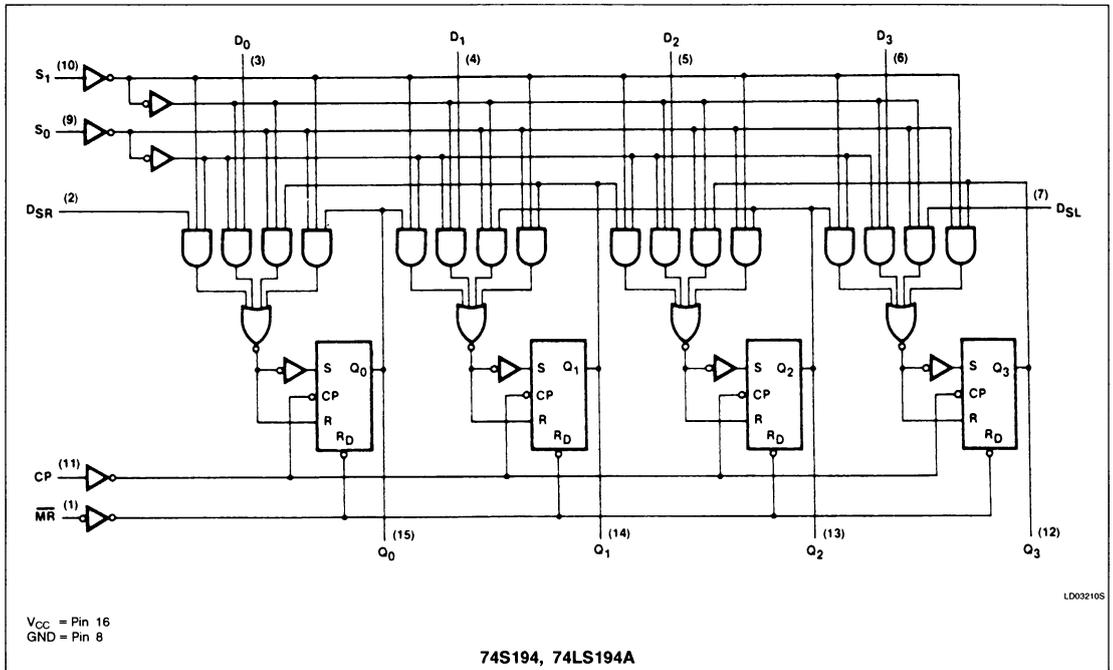
74194, LS194A, S194

LOGIC DIAGRAM



5

LOGIC DIAGRAM



Shift Registers

74194, LS194A, S194

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18			-18	mA
I _{OH}	HIGH-level output current			-800			-400			-1000	μA
I _{OL}	LOW-level output current			16			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74194			74LS194A			74S194			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.5		2.7	3.4		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4			
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA
		V _I = 7.0V					0.1				mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40						μA
		V _I = 2.7V					20			50	μA
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V			-1.6		-0.4				mA
		V _I = 0.5V								-2.0	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-57	-20		-100	-40		-100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		39	63		15	23		85	135	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With all outputs open, D_i inputs grounded and 4.5V applied to S₀, S₁, \overline{MR} and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

Shift Registers

74194, LS194A, S194

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	25		25		70		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		22 26		22 26	4.0 4.0	12 16.5	ns
t_{PHL} Propagation delay $\overline{\text{MR}}$ to output	Waveform 2		37		30		18.5	ns

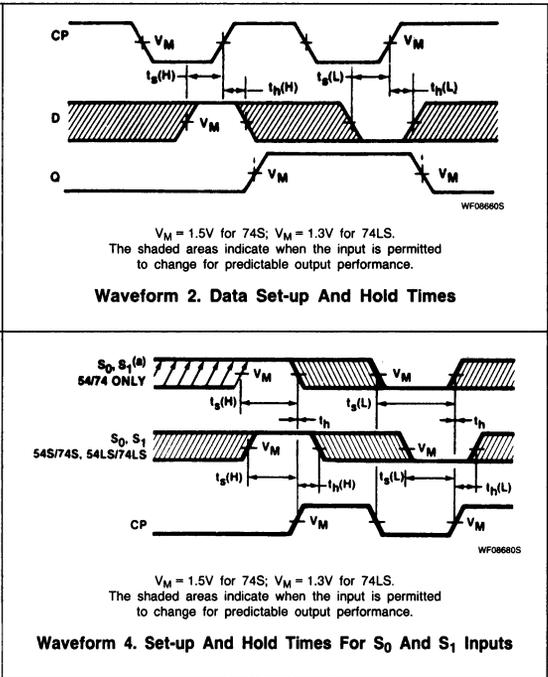
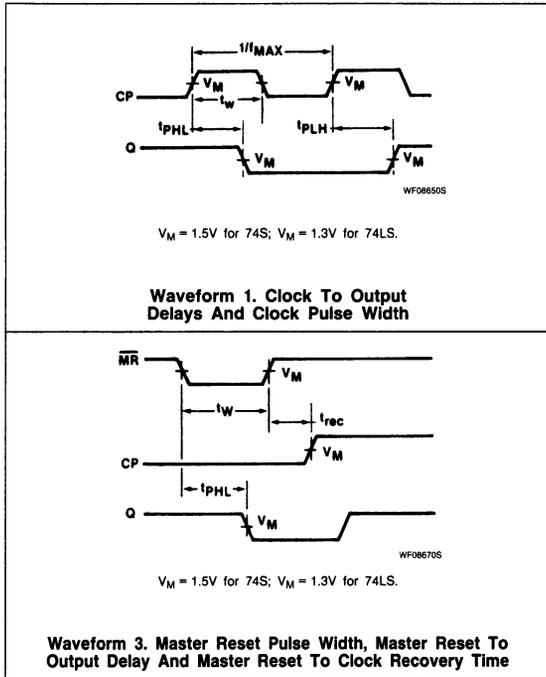
NOTE:Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.**AC SET-UP REQUIREMENTS** $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{\text{W(H)}}$ Clock pulse width HIGH	Waveform 1	20		20		7		ns
$t_{\text{W(L)}}$ $\overline{\text{MR}}$ pulse width, LOW	Waveform 2	20		20		12		ns
t_s Set-up time, data to clock	Waveform 3	20		20		5.0		ns
t_h Hold time, data to clock	Waveform 3	0		0		3.0		ns
$t_s(\text{L})$ Set-up time LOW, S_n to CP ^(a)	Waveform 4	30		30		11		ns
$t_s(\text{H})$ Set-up time HIGH, S_n to CP	Waveform 4	30		30		11		ns
t_h Hold time, S_n to CP	Waveform 4	0		0		3.0		ns
t_{rec} Recovery time, $\overline{\text{MR}}$ to CP	Waveform 2	25		25		9.0		ns

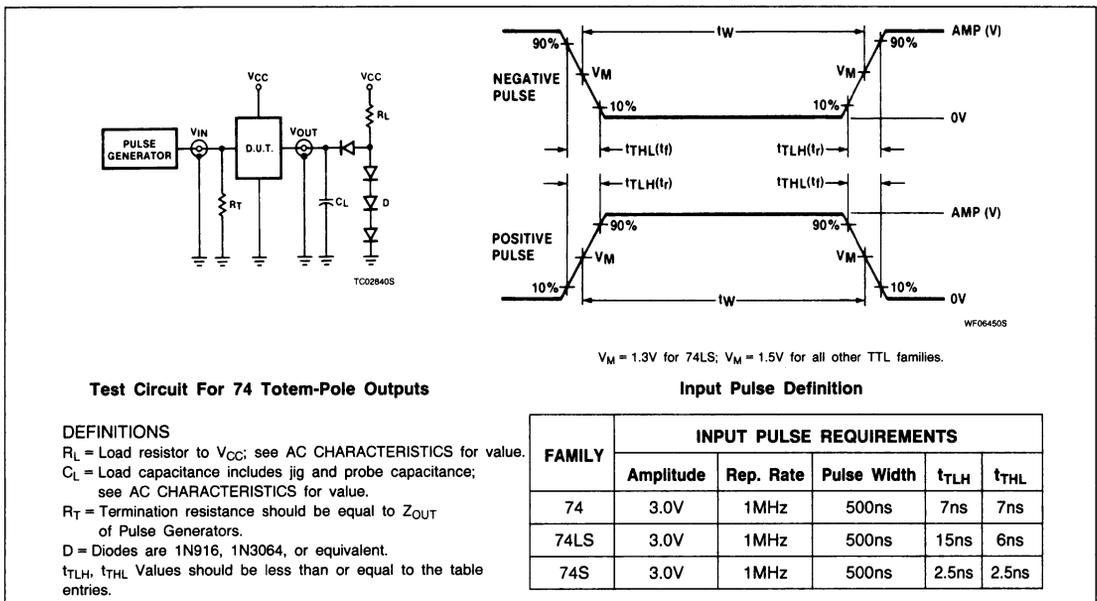
Shift Registers

74194, LS194A, S194

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74195, LS195A, S195 Shift Registers

4-Bit Parallel Access Shift Register
Product Specification

Logic Products

FEATURES

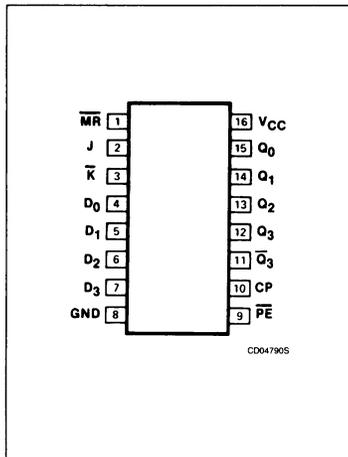
- Buffered Clock and Control inputs
- Shift right and parallel load capability
- J-K (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset

DESCRIPTION

The functional characteristics of the '195 4-Bit Parallel Access Shift register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The '195 operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74195	39MHz	39mA
74LS195A	39MHz	14mA
74S195	105MHz	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74195N, N74LS195N, N74S195N
Plastic SO-16	N74LS195AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1uI	1Sul	1LSul
All	Outputs	10uI	10Sul	10LSul

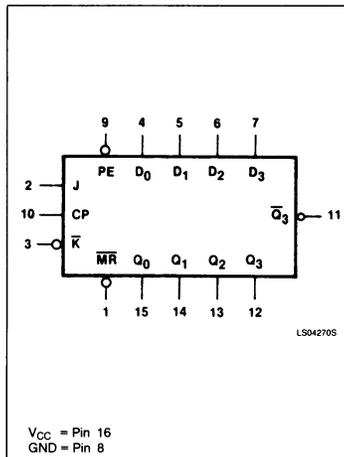
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

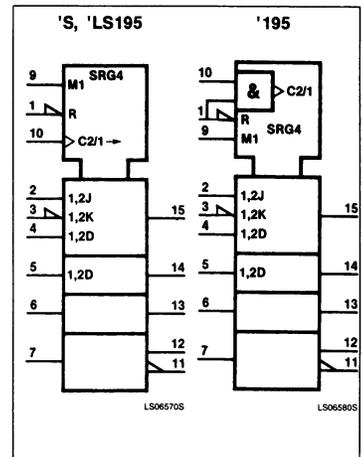
The J and \overline{K} inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four

common clocked D flip-flops when the \overline{PE} input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_3$) is transferred to the respective $Q_0 - Q_3$ outputs.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Shift Registers

74195, LS195A, S195

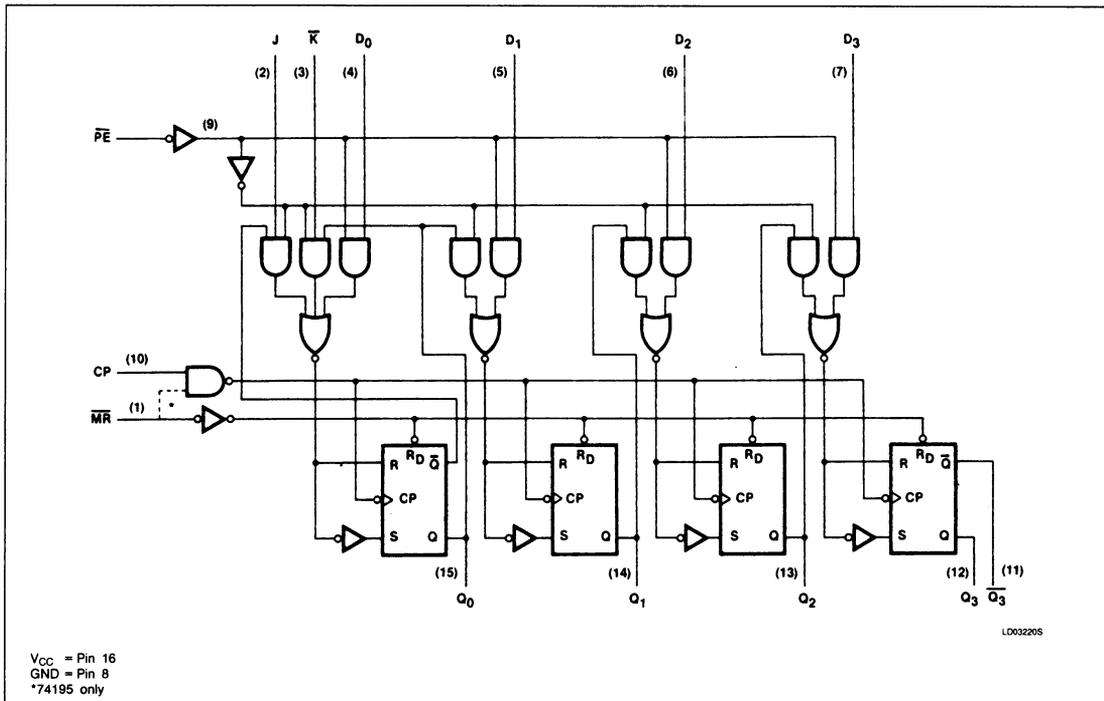
Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the \overline{PE} input low.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The '195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, \overline{K} , D_n , and \overline{PE} inputs for logic operation, other than the set-up and release time requirements.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition. The \overline{MR} on the 54/74195 is gated with the clock. Therefore, the LOW-to-HIGH \overline{MR} transition should only occur while the clock is LOW to avoid false clocking on the 54/74195.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	\overline{MR}	CP	\overline{PE}	J	\overline{K}	D_n	Q_0	Q_1	Q_2	Q_3	\overline{Q}_3
Asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
Shift, set first stage	H	\uparrow	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$
Shift, reset first stage	H	\uparrow	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$
Shift, toggle first stage	H	\uparrow	h	h	l	X	$\overline{q_0}$	q_0	q_1	q_2	$\overline{q_2}$
Shift, retain first stage	H	\uparrow	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
Parallel load	H	\uparrow	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d_3}$

H = HIGH voltage level.

L = LOW voltage level.

X = Don't care.

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.

\uparrow = LOW-to-HIGH clock transition.

Shift Registers

74195, LS195A, S195

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18			-18	mA
I _{OH}	HIGH-level output current			-800			-400			-1000	μA
I _{OL}	LOW-level output current			16			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74195			74LS195A			74S195			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, I _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4			V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V		1.0						1.0	mA
		V _I = 7.0V						0.1			mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V		40							μA
		V _I = 2.7V						20		50	μA
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V		-1.6				-0.4			mA
		V _I = 0.5V								-2	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-18		-57	-20		-100	-40		-100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX		39	63		14	21		70	109	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With all outputs open, \overline{PE} grounded, and 4.5V applied to the J, \overline{K} , and Data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to \overline{MR} , and then a momentary ground, followed by 4.5V to clock.

Shift Registers

74195, LS195A, S195

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	30		30		70		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		22 26		22 26		12 16.5	ns
t_{PHL} Propagation delay MR to output	Waveform 2		30		30		18.5	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Clock pulse width	Waveform 1	16		16		7		ns
t_W Master Reset pulse width	Waveform 2	12		12		12		ns
t_s Set-up time, J, \bar{K} and data to clock	Waveform 3	20		15		5.0		ns
t_h Hold time, J, \bar{K} and data to clock	Waveform 3	0		0		3.0		ns
t_s Set-up time, \bar{PE} to clock	Waveform 4	25		25		11		ns
t_h Hold time, \bar{PE} to clock	Waveform 4	0		0		0		ns
t_{rec} Recovery time, \bar{MR} to clock	Waveform 2	25		25		9.0		ns

AC WAVEFORMS

WF086905

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.5\text{V}$ for 74LS.

Waveform 1. Clock To Output Delays And Clock Pulse Width

WF087005

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.5\text{V}$ for 74LS.

Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay And Master Reset to Clock Recovery Time

WF087105

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.5\text{V}$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data Set-up And Hold Times

WF087205

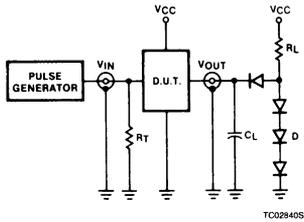
$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.5\text{V}$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4. Set-up And Hold Times Parallel Enable To Clock

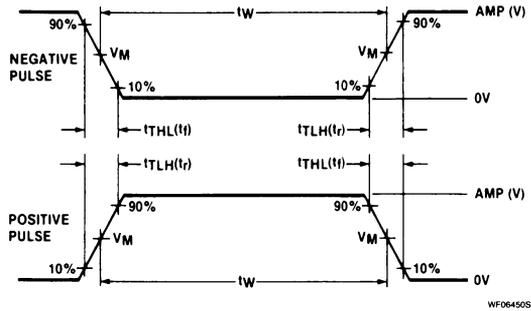
Shift Registers

74195, LS195A, S195

TEST CIRCUITS AND WAVEFORMS



TC029405



WF064505

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS197 Counter

Presetable 4-Bit Binary Ripple Counter
Product Specification

Logic Products

FEATURES

- High speed 4-bit binary counting
- Asynchronous parallel load for presetting counter
- Overriding Master Reset
- Buffered Q_0 output drives \overline{CP}_1 input plus standard fan-out

DESCRIPTION

The '197 is an asynchronously presetable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate Clock input. Stage changes are initiated in the counting modes by the HIGH-to-LOW transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock. The Q_0 flip-flop is triggered by the \overline{CP}_0 input while the \overline{CP}_1 input triggers the divide-by-8 section.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74LS197	40MHz	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS197N
Plastic SO-14	N74LS197D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
\overline{CP}_0	Clock input	6LSul
\overline{CP}_1	Clock input	3.5LSul
All	Other inputs	1LSul
$Q_0 - Q_3$	Outputs	10LSul

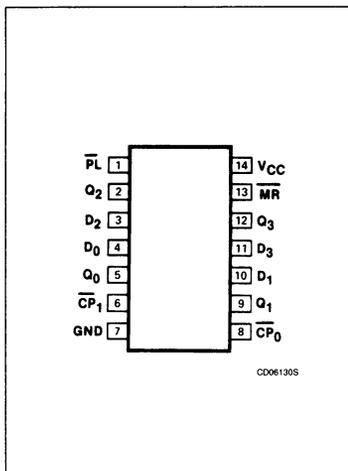
NOTE:

Where a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

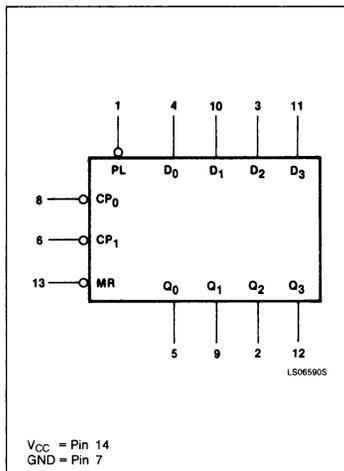
The device has an asynchronous active-LOW Master Reset (\overline{MR}) input which overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presetable. A LOW on the Parallel Load (\overline{PL}) input overrides the

Clock inputs and loads the data from parallel Data ($D_0 - D_3$) inputs into the flip-flops. The counter acts as a transparent latch while the \overline{PL} is LOW and any change in the D_n inputs will be reflected in the outputs.

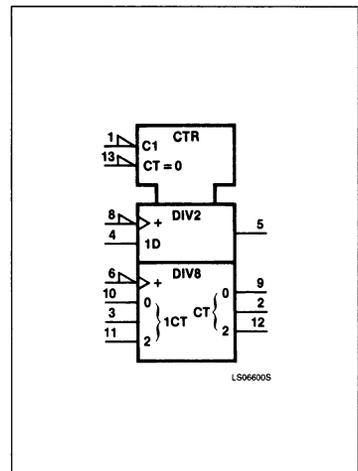
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Counter

74LS197

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS197			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.35	0.5	V
		I _{OL} = 4mA (74LS)	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V	D ₀ - D ₃ , $\overline{P}L$		0.1	mA
		$\overline{M}R$, $\overline{C}P_0$, $\overline{C}P_1$		0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	D ₀ - D ₃ , $\overline{P}L$		20	μ A
		$\overline{M}R$, $\overline{C}P_0$, $\overline{C}P_1$		40	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	D ₀ - D ₃ , $\overline{P}L$		-0.4	mA
		$\overline{M}R$ input		-0.8	mA
		$\overline{C}P_0$ input		-2.4	mA
		$\overline{C}P_1$ input		-1.3	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		16	27	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2k Ω		
		Min	Max	
f _{MAX} Maximum count frequency	Waveform 1	$\overline{C}P_0$	30	MHz
		$\overline{C}P_1$	15	MHz
t _{PLH} t _{PHL}	Propagation delay $\overline{C}P_0$ to Q ₀	Waveform 1	15 21	ns
t _{PLH} t _{PHL}	Propagation delay CP ₁ to Q ₁	Waveform 1	19 35	ns
t _{PLH} t _{PHL}	Propagation delay $\overline{C}P_1$ to Q ₂	Waveform 1	51 63	ns
t _{PLH} t _{PHL}	Propagation delay $\overline{C}P_1$ to Q ₃	Waveform 1	78 95	ns
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 2	27 44	ns
t _{PLH} t _{PHL}	Propagation delay $\overline{P}L$ to output	Waveform 3	39 45	ns
t _{PHL}	Propagation delay $\overline{M}R$ to output	Waveform 4	51	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

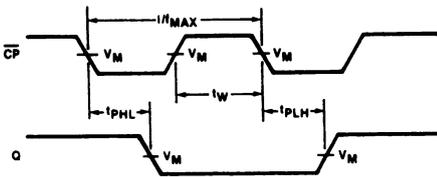
Counter

74LS197

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

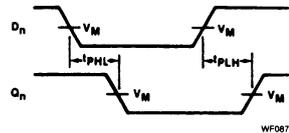
PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_w Clock pulse width	Waveform 1	\overline{CP}_0	20	ns
		\overline{CP}_1	30	ns
t_w \overline{MR} pulse width	Waveform 4	15		ns
t_w \overline{PL} pulse width	Waveform 3	20		ns
$t_s(H)$ Set-up time HIGH data to \overline{PL}	Waveform 5	10		ns
$t_h(H)$ Hold time HIGH data to \overline{PL}	Waveform 5	20		ns
$t_s(L)$ Set-up time LOW data to \overline{PL}	Waveform 5	15		ns
$t_h(L)$ Hold time LOW data to \overline{PL}	Waveform 5	20		ns
t_{rec} Recovery time \overline{MR} to \overline{CP}	Waveform 4	30		ns
t_{rec} Recovery time \overline{PL} to \overline{CP}	Waveform 3	30		ns

AC WAVEFORMS



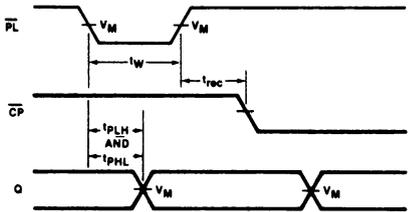
WF08730S

Waveform 1. Clock To Output Delays And Clock Pulse Width



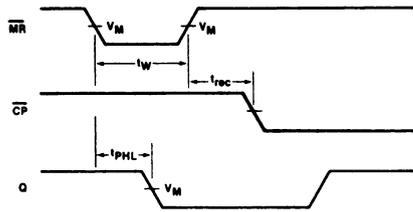
WF08740S

Waveform 2. Parallel Data To Output Delays



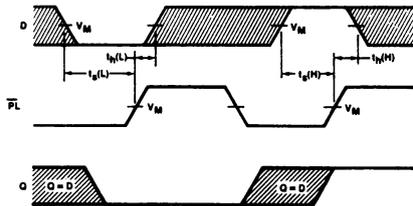
WF08750S

Waveform 3. Parallel Load Pulse Width, Parallel Load To Output Delay And Parallel Load To Clock Recovery Time



WF08760S

Waveform 4. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



WF08770S

For all waveforms, $V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

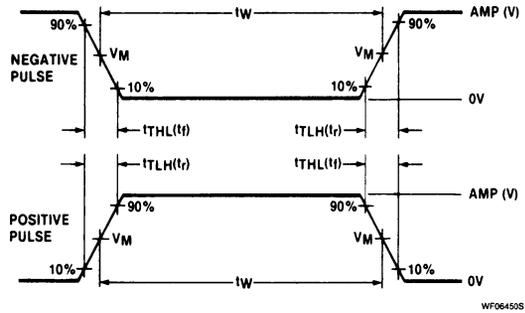
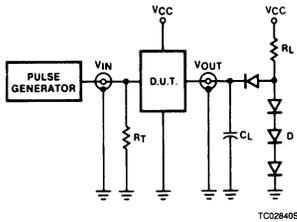
Waveform 5. Data Set-up And Hold Times

5

Counter

74LS197

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74199 Shift Register

8-Bit Parallel-Access Shift Register
Product Specification

Logic Products

FEATURES

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J-K (D) inputs to first stage
- Clock enable for hold (do nothing) mode
- Asynchronous Master Reset

DESCRIPTION

The functional characteristics of the '199 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74199	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74199N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

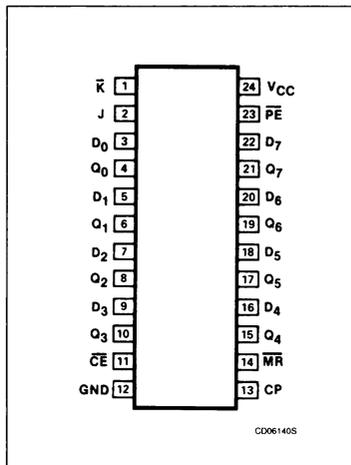
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1uI
$Q_0 - Q_7$	Parallel outputs	10uI

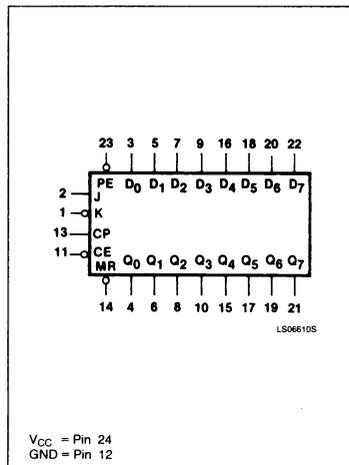
NOTE:

A 74 unit load (uI) is understood to be 40 μ A I_{IH} AND -1.6mA I_{IL} .

PIN CONFIGURATION

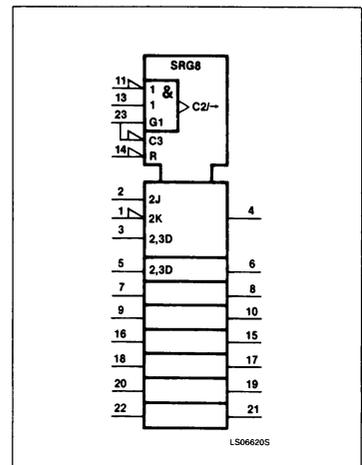


LOGIC SYMBOL



$V_{CC} = \text{Pin } 24$
 $GND = \text{Pin } 12$

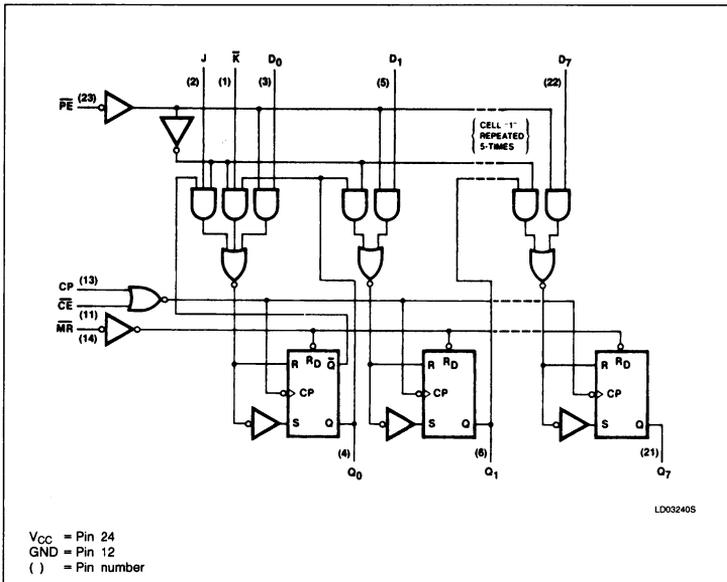
LOGIC SYMBOL (IEEE/IEC)



Shift Register

74199

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS							
	MR	CP	CE	PE	J	K	D _n	Q ₀	Q ₁	Q ₆	Q ₇			
Reset (clear)	L	X	X	X	X	X	X	L	L	L	L			
Shift, set first stage	H	↑	l	h	h	h	X	H	q ₀	q ₅	q ₆			
Shift, reset first stage	H	↑	l	h	l	l	X	L	q ₀	q ₅	q ₆			
Shift, toggle first stage	H	↑	l	h	h	l	X	\bar{q}_0	q ₀	q ₅	q ₆			
Shift, retain first stage	H	↑	l	h	l	h	X	q ₀	q ₀	q ₅	Q ₆			
Parallel load	H	↑	l	l	X	X	d _n	d ₀	d ₁	d ₆	d ₇			
Hold (do nothing)	H	↑	h ^(a)	X	X	X	X	q ₀	q ₁	q ₆	q ₇			

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care
 d_n(q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
 ↑ = LOW-to-HIGH clock transition.

NOTE:
 a. The LOW-to-HIGH transition of \bar{CE} should only occur while CP is HIGH for conventional operation.

The '199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable (PE) input. Serial data enters the first flip-flop (Q_0) via the J and \bar{K} inputs when the PE input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and \bar{K} inputs provide the flexibility of the J-K type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the PE input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_7$) is transferred to the respective $Q_0 - Q_7$ outputs.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The '199 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, \bar{K} , D_n , and PE inputs for logic operation, other than the set-up and release time requirements.

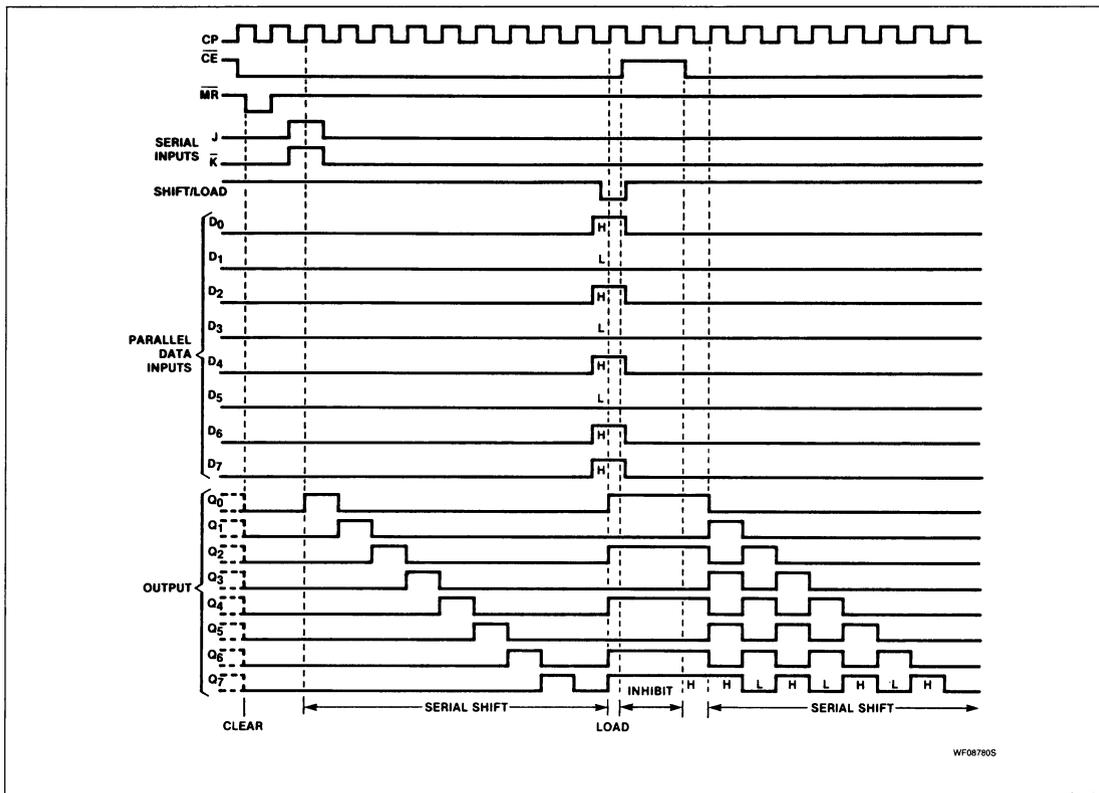
The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable (\bar{CE}) input. The pin assignment for the CP and \bar{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of \bar{CE} input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset (\bar{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

Shift Register

74199

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



5

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC}	4.75	5.0	5.25	V
V _{IH}	2.0			V
V _{IL}			+0.8	V
I _{IK}			-12	mA
I _{OH}			-800	V
I _{OL}			16	mA
T _A	0		70	°C

Shift Register

74199

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74199			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		90	127	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with \overline{K} , J and D inputs at 4.5V, momentary ground clock, then apply 4.5V, ground \overline{CE} , \overline{MR} and PE.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		26 30	ns
t _{PHL} Propagation delay MR to output	Waveform 2		35	ns

Per industry convention, f_{MAX} is the worst case of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

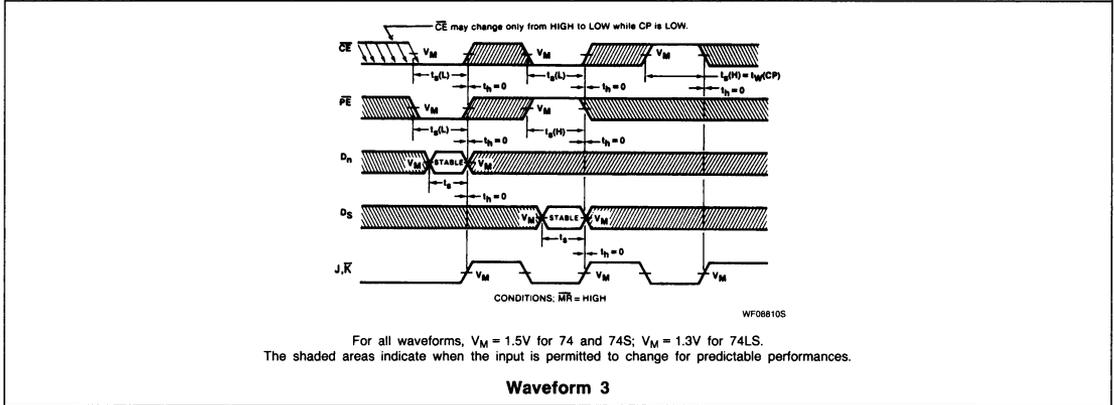
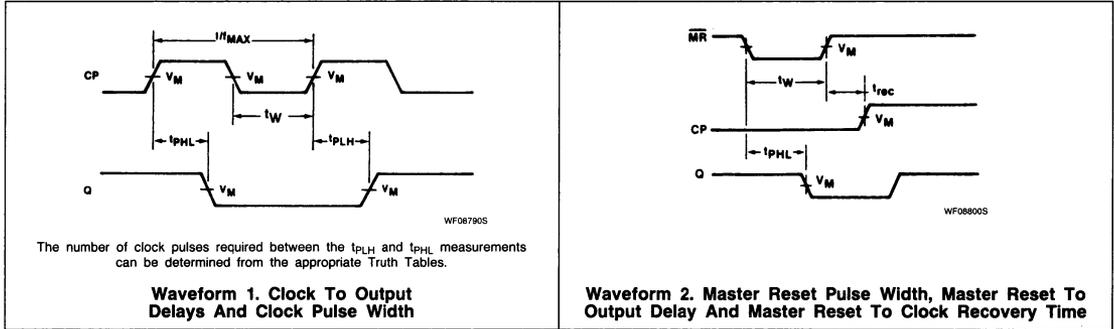
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t _W Clock pulse width	Waveform 1	20		ns
t _W \overline{MR} pulse width	Waveform 2	20		ns
t _s Set-up time, J, \overline{K} and data to clock	Waveform 3	20		ns
t _h Hold time, J, \overline{K} and data to clock	Waveform 3	0		ns
t _s Set-up time, \overline{CE} to clock	Waveform 3	30		ns
t _h Hold time, \overline{CE} to clock	Waveform 3	0		ns
t _s Set-up time, \overline{PE} to clock	Waveform 3	30		ns
t _h Hold time, \overline{PE} to clock	Waveform 3	0		ns
t _{rec} Recovery time, \overline{MR} to clock	Waveform 2	30		ns

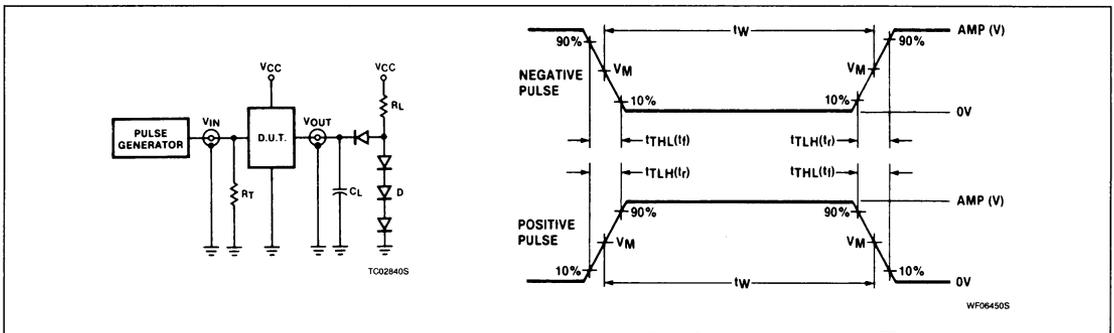
Shift Register

74199

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74221 Multivibrator

Dual Monostable Multivibrator Product Specification

Logic Products

FEATURES

- Pulse width variance is typically less than $\pm 0.5\%$ for 98% of the units
- The '221 demonstrates electrical and switching characteristics that are virtually identical to the '121 one-shots
- Pin-out is identical to the '123
- Overriding Reset terminates output pulse
- B input has hysteresis for improved noise immunity
- Maximum pulse width:
54221: 21 seconds
74221: 28 seconds

DESCRIPTION

The '221 is a dual monostable multivibrator with performance characteristics virtually identical to those of the '121. Each multivibrator features an active LOW going edge input (\bar{A}) and an active HIGH going edge input (B), either of which can be used as an Enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hys-

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74221	42ns	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74221N
Plastic SO-16	N74221D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

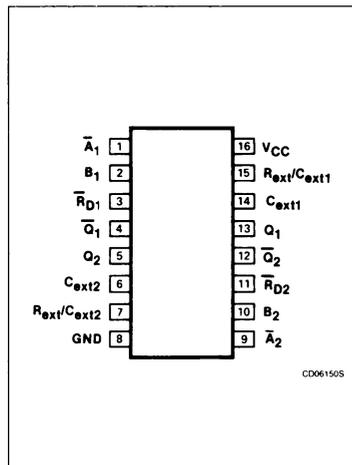
teresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the \bar{A} and B inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW Reset (\bar{R}_D). Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from

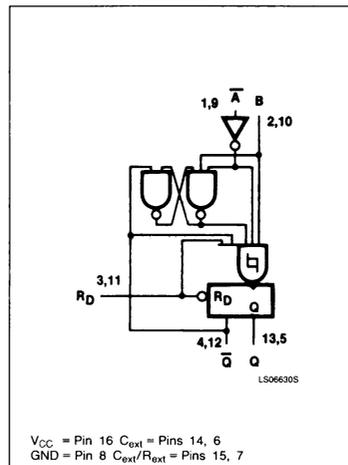
35 nanoseconds to the maximums shown in the FEATURES by choosing appropriate timing components. With $R_{ext} = 2k\Omega$ and $C_{ext} = 0$, an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

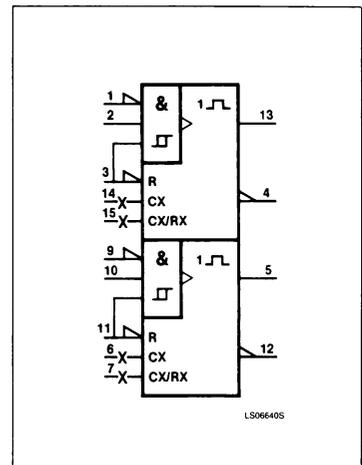
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Multivibrator

74221

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10 μ F) and more than one decade of timing resistance (2k Ω to 30k Ω for the 54221 and 2k Ω to 40k Ω for the 74221). Throughout these ranges, pulse width is defined by the following relationship: (see Figure A)

$$t_w(\text{out}) = C_{\text{ext}}R_{\text{ext}}\ln 2$$

$$t_w(\text{out}) \cong 0.7C_{\text{ext}}R_{\text{ext}}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4k Ω may be used.

Pin assignments for these devices are identical to those of the '123 so that the '221 can

be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext} .

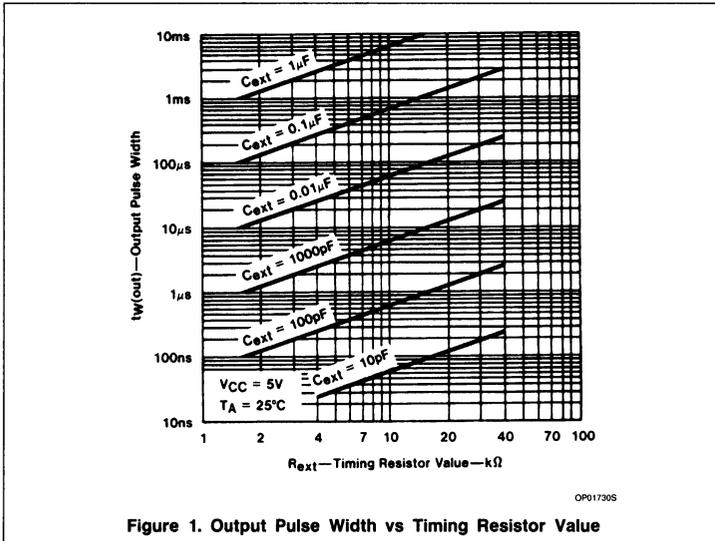


Figure 1. Output Pulse Width vs Timing Resistor Value

FUNCTION TABLE (Each monostable)

INPUTS			OUTPUTS	
\bar{R}_D	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow	\downarrow	\downarrow
H	\downarrow	H	\downarrow	\downarrow
\uparrow	L	H	\downarrow	\downarrow

In addition, see description and switching characteristics.

- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- \uparrow = LOW-to-HIGH transition
- \downarrow = HIGH-to-LOW transition
- \downarrow = one HIGH-level pulse
- \downarrow = one LOW-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
\bar{A}	Input	1uI
B, \bar{R}_D	Inputs	2uI
All	Outputs	10uI

NOTE:
A 74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70	$^{\circ}$ C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	V
I_{IK} Input clamp current			-12	mA
I_{OH} HIGH-level output current			-800	μ A
I_{OL} LOW-level output current			16	mA
T_A Operating free-air temperature	0		70	$^{\circ}$ C

Multivibrator

74221

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74221			UNIT	
			Min	Typ ²	Max		
V _{T+}	Positive-going threshold at \bar{A} and B	V _{CC} = MIN			2.0	V	
V _{T-}	Negative-going threshold at \bar{A} and B	V _{CC} = MIN	0.8			V	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = MAX	2.4	3.4		V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = MAX		0.2	0.4	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	\bar{A} input		40	μ A	
			B, \bar{R}_D inputs		80	μ A	
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	\bar{A} input		-1.6	mA	
			B, \bar{R}_D inputs		-3.2	mA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-18		-55	mA	
I _{CC}	Supply current (total)	V _{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74		UNIT
			C _L = 15pF, R _L = 400Ω		
			Min	Max	
t _{PLH}	Propagation delay	Waveform 1 C _{ext} = 80pF, R _{ext} = 2kΩ		70	ns
t _{PHL}	\bar{A} input to Q & \bar{Q} output			80	ns
t _{PLH}	Propagation delay	Waveform 2 C _{ext} = 80pF, R _{ext} = 2kΩ		55	ns
t _{PHL}	B input to Q & \bar{Q} output			65	ns
t _{PLH}	Propagation delay	Waveform 3 C _{ext} = 80pF, R _{ext} = 2kΩ		40	ns
t _{PHL}	\bar{R}_D input to Q & \bar{Q} output			27	ns
t _w	Minimum output pulse width	C _{ext} = 0pF, R _{ext} = 2kΩ		50	ns
t _w	Output pulse width	C _{ext} = 80pF, R _{ext} = 2kΩ	70	150	ns
		C _{ext} = 100pF, R _{ext} = 10kΩ	650	750	ns
		C _{ext} = 1μF, R _{ext} = 10kΩ	6.5	7.5	ms

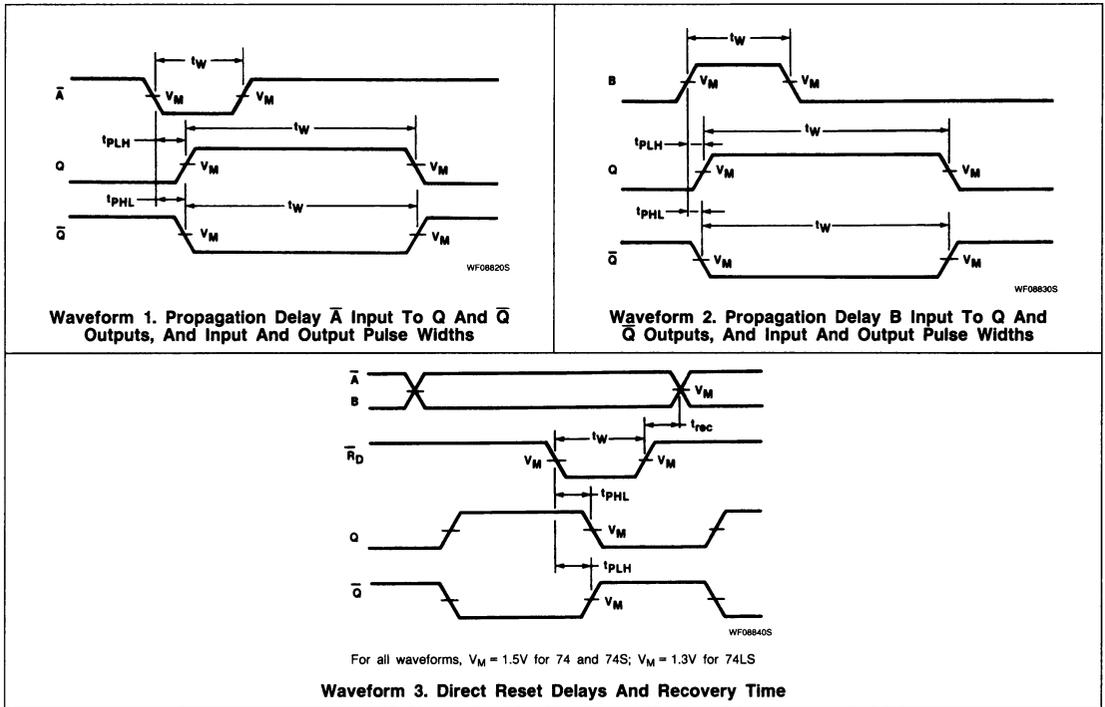
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74		UNIT
			Min	Max	
t _w	Minimum input pulse width to trigger	Waveforms 1 & 2	50		ns
t _w	Minimum reset pulse width	Waveform 3	20		ns
t _{rec}	Recovery time from reset to trigger input	Waveform 3	15		ns
R _{ext}	External timing resistor range		1.4	40	kΩ
C _{ext}	External timing capacitance range		0	1000	μF
Output duty cycle		R _{ext} = 2kΩ		67	%
		R _{ext} = R _{ext} (MAX)		90	%

Multivibrator

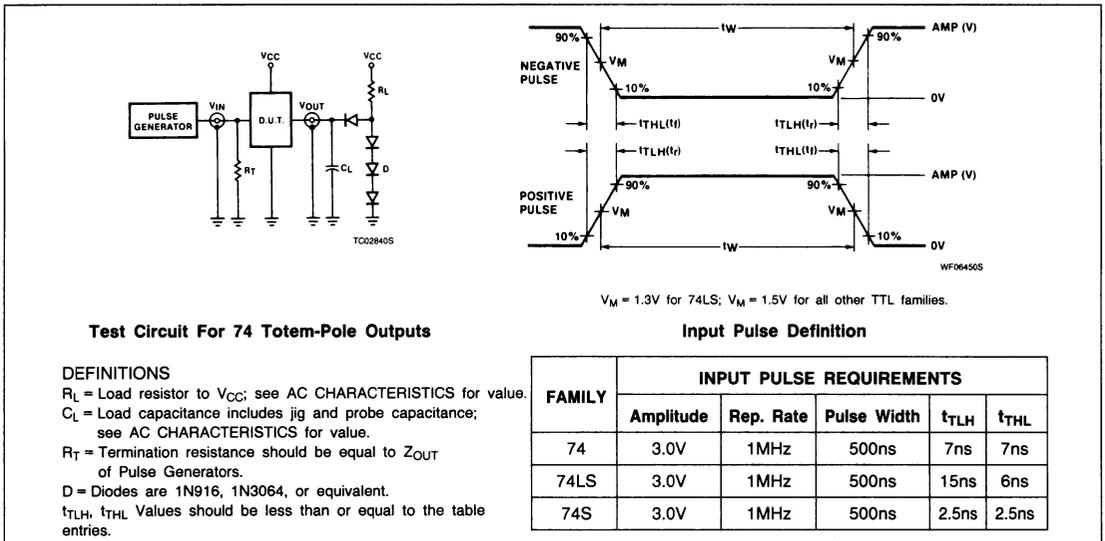
74221

AC WAVEFORMS



5

TEST CIRCUITS AND WAVEFORMS



74S225 16 x 5 FIFO

16 x 5 Asynchronous First-In/First-Out Memory (3-State)
Product Specification

Logic Products

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16-words of 5 bits
- DC to 10-MHz data rate
- 3-state outputs

DESCRIPTION

This 80-bit active element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words of five-bits each. A memory system using the 'S225 can easily be expanded in multiples of 16 words or of 5 bits as shown in Figure 2. The three-state outputs controlled by a single enable, \overline{OE} , make bus connection and multiplexing easy.

A FIFO is a memory storage device which allows data to be written into and/or read from its array at independent data rates. The 'S225 is a FIFO which will process data at any desired clock rate from DC to 10MHz. The data is processed in a parallel format, word by word.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S225	20MHz	80mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S225N
Plastic SOL-20	N74S225

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

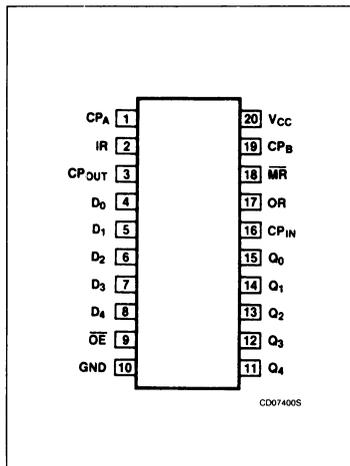
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
CP_A, CP_B	Load clock A, B inputs	0.1 SUL
$D_0 - D_4$	Data inputs	0.5 SUL
\overline{OE}	Output enable input	0.1 SUL
CP_{IN}	Unload clock input	0.1 SUL
\overline{MR}	Master reset input	0.1 SUL
IR	Input ready output	10 SUL
CP_{OUT}	Unload clock output	10 SUL
$Q_0 - Q_4$	Data outputs	10 SUL
OR	Output ready	10 SUL

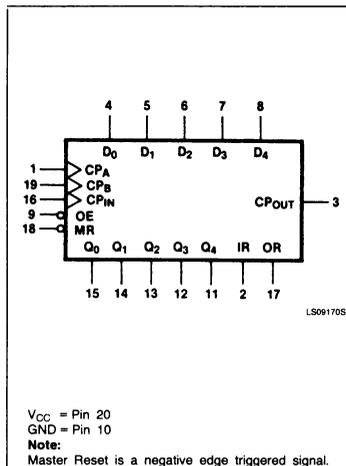
NOTE:

Where a 74S unit load (SUL) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

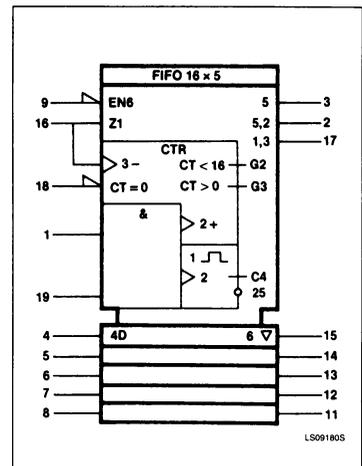
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



16 x 5 FIFO

74S225

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74S			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current	Data outputs		-6.5	mA
		Other outputs		-3.2	mA
I _{OL}	LOW-level output current	Data outputs		16	mA
		Other outputs		8	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S225			UNIT
		Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = MAX			V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			V
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V			μA
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.5V			μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			mA
I _{IH}	HIGH-level input current	Data inputs		40	μA
		Other inputs		25	μA
I _{IL}	LOW-level input current	Data inputs		-1	mA
		Other inputs		-250	μA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX			mA
I _{CC}	Supply current ⁴ (total)		80	120	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Measure I_{CC} with all outputs open and all possible inputs grounded.

16 x 5 FIFO

74S225

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS ¹	74S		UNIT
		$C_L = 30\text{pF}$ except where noted		
		Min	Max	
f_{MAX} Maximum clock frequency CP_A	Waveform 3	10		MHz
f_{MAX} Maximum clock frequency CP_B	Waveform 3	10		MHz
f_{MAX} Maximum clock frequency CP_{IN}	Waveform 2	10		MHz
t_W CP_{OUT}	Waveform 4	7		ns
t_{PLH} Propagation delay CP_{IN} to Q_n	Waveform 2		75 75	ns
t_{PLH} Propagation delay CP_A or CP_B to OR	Waveform 4		300	ns
t_{PLH} Propagation delay CP_{IN} to OR	Waveform 2		60 45	ns
t_{PHL} Propagation delay \overline{MR} to OR	Waveform 3		60	ns
t_{PHL} Propagation delay CP_A or CP_B to CP_{OUT}	Waveform 4		45	ns
t_{PHL} Propagation delay CP_A or CP_B to IR	Waveform 3		75	ns
t_{PLH} Propagation delay CP_{IN} to IR	Waveform 2		400	ns
t_{PLH} Propagation delay \overline{MR} to IR	Waveform 3		35	ns
t_{PLH} Propagation delay Q_n to OR \uparrow	Waveform 4		20 20	ns
t_{PZH} Output enable time to HIGH level	Waveform 5		40	ns
t_{PZL} Output enable time to LOW level	Waveform 5		40	ns
t_{PHZ} Output disable time from HIGH level	Waveform 5, $C_L = 5.0\text{pF}$		25	ns
t_{PLZ} Output disable time from LOW level	Waveform 5, $C_L = 5.0\text{pF}$		25	ns

NOTE:

- $R_1 = 300\Omega$, $R_2 = 600\Omega$ for data outputs.
 $R_1 = 600\Omega$, $R_2 = 1.2\text{k}\Omega$ for all other outputs.

AC SET-UP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$)

PARAMETER	TEST CONDITIONS	74S		UNIT
		Min	Max	
t_W (HIGH) Load clock CP_A or CP_B pulse width	Waveform 1	25		ns
t_W (LOW) Unload clock input CP_{IN} pulse width	Waveform 1	7		ns
t_W Master reset pulse width \overline{MR}	Waveform 1, 3 ⁽²⁾	40		ns
t_s Set-up time Data to CP_A to CP_B	Waveform 1	-20 \uparrow ⁽¹⁾		ns
t_s Set-up time \overline{MR} to CP_A or CP_B	Waveform 1	25 \uparrow		ns
t_h Hold time Data from CP_A or CP_B	Waveform 1	70 \uparrow		ns

NOTES:

- Data must be set up within 20ns after the load clock positive transition.
 \uparrow indicates that the LOW-to-HIGH transition of the load clock is used for reference.
- If a \uparrow occurs on the CP_A or CP_B signal generating a load clock input during \overline{MR} low, t_W is measured from $\uparrow CP_A$ or CP_B to $\uparrow \overline{MR}$, see waveform 3.

5

16 x 5 FIFO

74S225

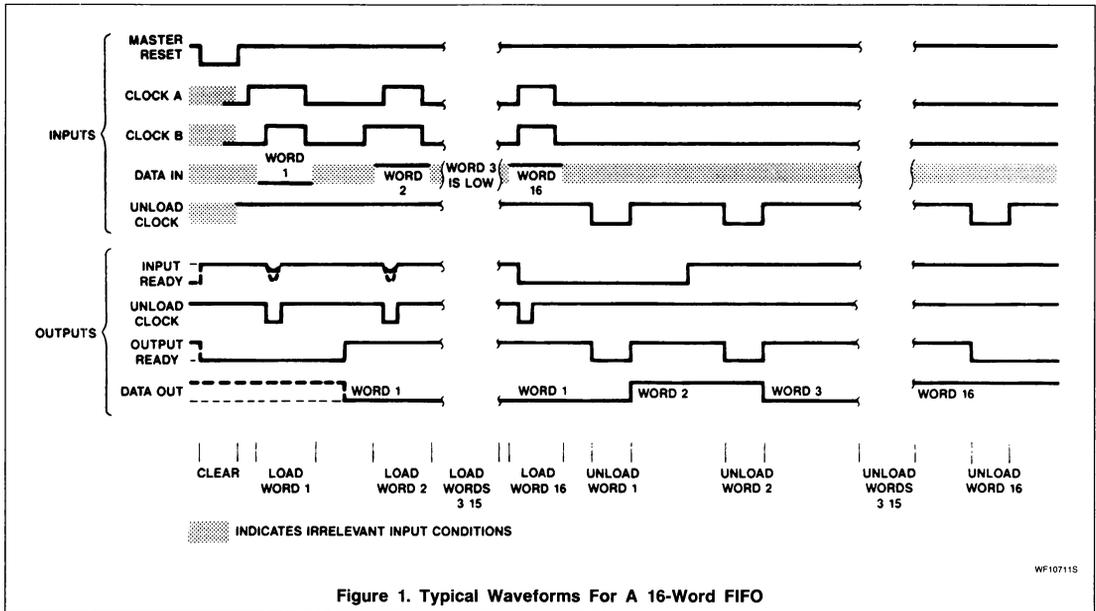


Figure 1. Typical Waveforms For A 16-Word FIFO

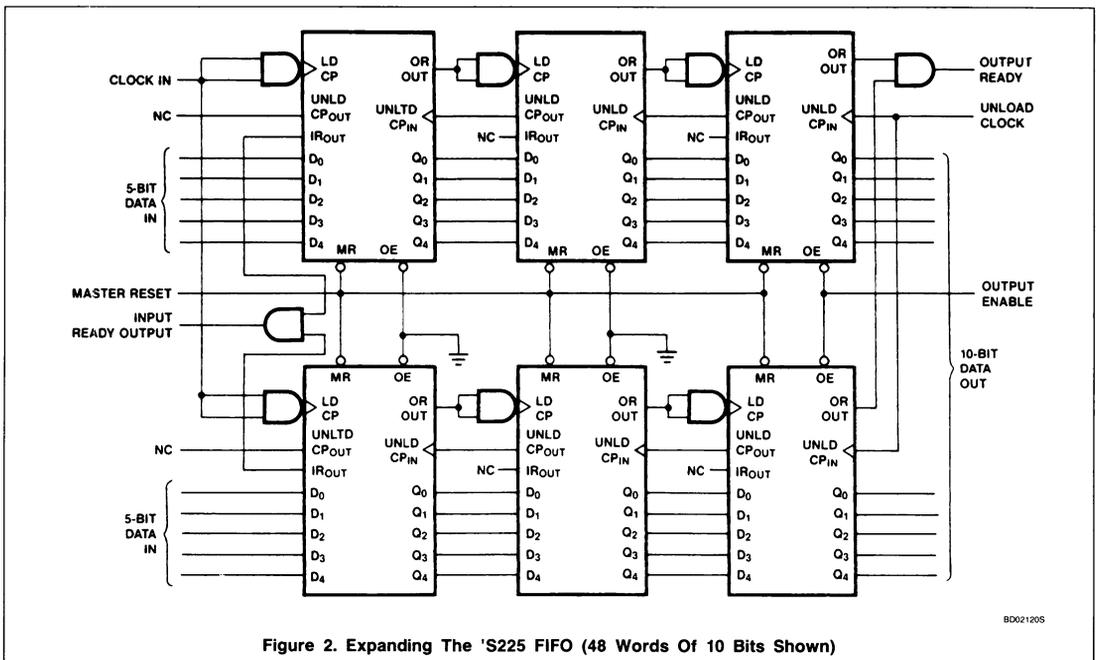
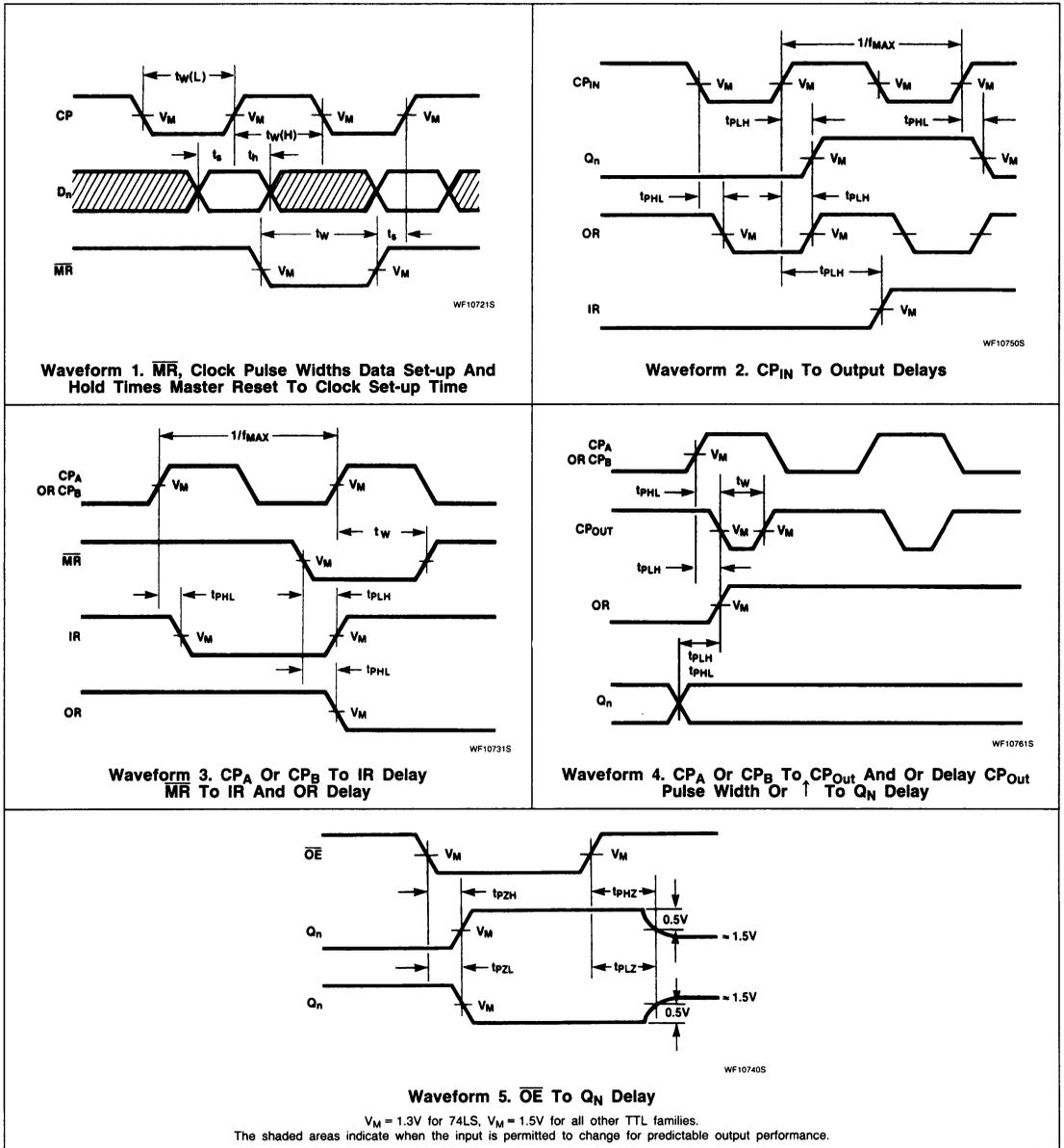


Figure 2. Expanding The 'S225 FIFO (48 Words Of 10 Bits Shown)

16 x 5 FIFO

74S225

AC WAVEFORMS

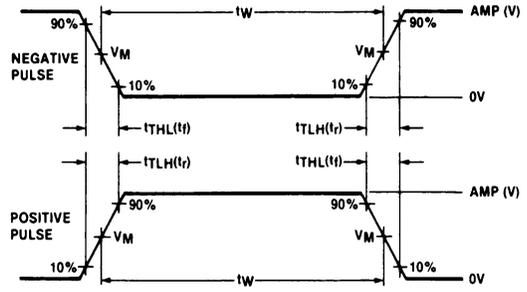
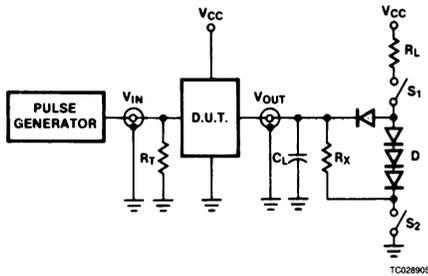


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16 x 5 FIFO

74S225

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PZH}, t_{PZH}	0.0V
All other	5.0V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

OUTPUTS	R_1	R_2
Data	300Ω	600Ω
All other	600Ω	1.2Ω

DEFINITIONS

- R_1, R_2 = Load resistors.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

74LS240, 74LS241, S240, S241 Buffers

Logic Products

'240 Octal Inverter Buffer (3-State)
'241 Octal Buffer (3-State)
Product Specification

FUNCTION TABLE, '240

INPUTS				OUTPUTS	
\overline{OE}_a	I_a	\overline{OE}_b	I_b	\overline{Y}_a	\overline{Y}_b
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE, '241

INPUTS				OUTPUTS	
\overline{OE}_a	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS240	11ns	24mA
74S240	4.5ns	93mA
74LS241	12ns	25mA
74S241	6ns	112mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS240N, N74S240N N74LS241N, N74S241N
Plastic SOL-20	N74LS240D, N74S240D N74LS241D, N74S241D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

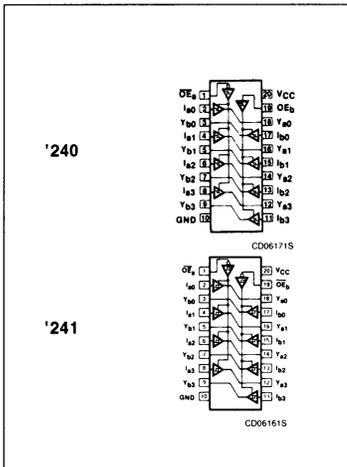
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
$I_{a0} - I_{a3}, I_{b0} - I_{b3}$	Inputs	1Sul	1LSul
$\overline{OE}_a, \overline{OE}_b, OE_b$	Inputs	1Sul	1LSul
All	Outputs	24Sul	32LSul

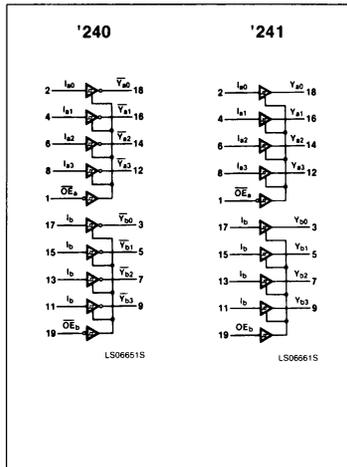
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

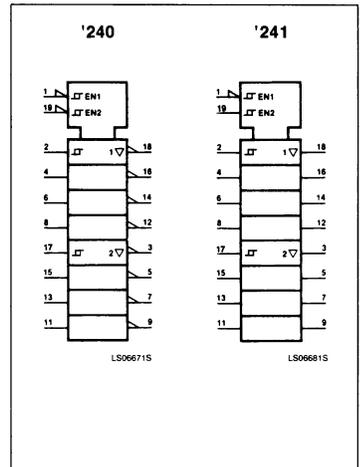
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffers

74LS240, 74LS241, S240, S241

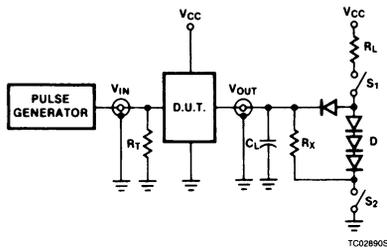
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

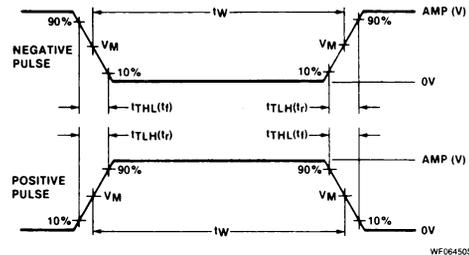
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	4.75	5.0	5.25	4.75	5.0	5.25	V	
V _{IH}	HIGH-level input voltage			2.0			V	
V _{IL}	LOW-level input voltage			+0.8			V	
I _{IK}	Input clamp current			-18			mA	
I _{OH}	HIGH-level output current			-15			mA	
I _{OL}	LOW-level output current			64			mA	
T _A	Operating free-air temperature			0			°C	
External resistance between any input or V _{CC} and ground							40	kΩ

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t _{pZH}	Open	Closed
t _{pZL}	Closed	Open
t _{pHZ}	Closed	Closed
t _{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffers

74LS240, 74LS241, S240, S241

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS240,241			74S240, 241			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4		V	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = 0.5V,$ $I_{OH} = \text{MAX}$	2.0			2.0			V	
	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OH} = -3\text{mA}$	2.4	3.4	2.4	3.4		V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$			$I_{OH} = -1\text{mA}$ (74S)	2.7			V	
		$I_{OL} = \text{MAX}$			0.5		0.55	V	
V_{OL} LOW-level output voltage		$I_{OL} = 12\text{mA}$ (74LS)			0.4			V	
	V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5		-1.2	V	
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$V_O = 2.4V$					50	μA	
		$V_O = 2.7V$			20			μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$V_O = 0.4V$			-20			μA	
		$V_O = 0.5V$					-50	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$					1.0	mA	
		$V_I = 7.0V$			0.1			mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$				20		50	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4V$					-0.2	mA	
		$V_I = 0.5V$	$I_{a0} - I_{a3}, I_{b0} - I_{b3}$ inputs					-400	μA
			$\overline{OE}_a, \overline{OE}_b, \overline{OE}_c$ inputs						-2
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$	-40		-130	-80		-180	mA	
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH}	'LS240		17	27			mA
		I_{CCL}			26	44			mA
		I_{CCZ}			29	50			mA
		I_{CCH}	'LS241		17	27			mA
		I_{CCL}			27	46			mA
		I_{CCZ}			32	54			mA
		I_{CCH}	'S240				80	135	mA
		I_{CCL}					100	150	mA
		I_{CCZ}					100	150	mA
		I_{CCH}	'S241				95	160	mA
I_{CCL}					120	180	mA		
I_{CCZ}					120	180	mA		

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with outputs open.

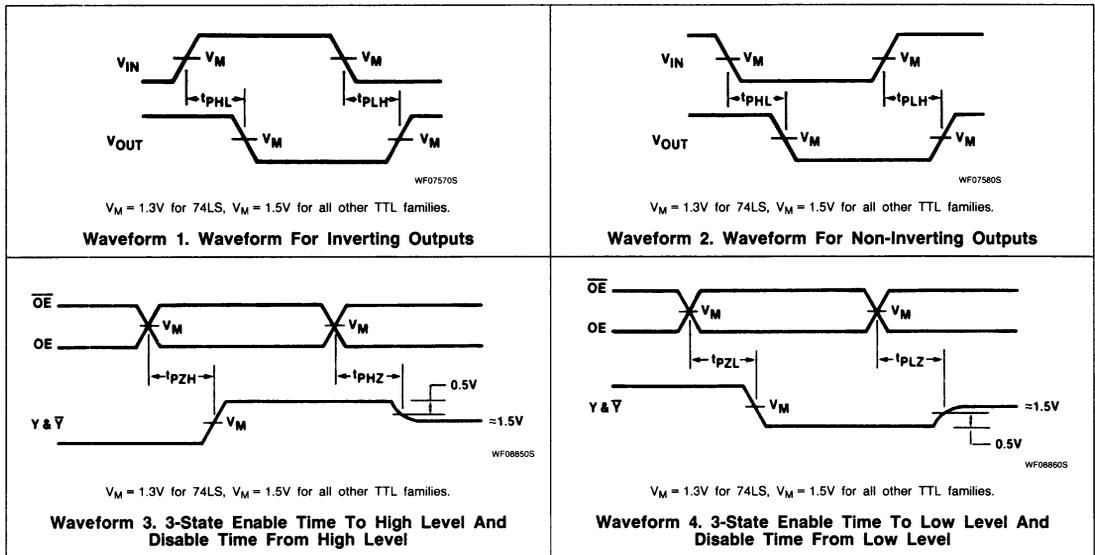
Buffers

74LS240, 74LS241, S240, S241

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 50\text{pF}$, $R_L = 90\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1, '240		14 18	7 7		ns
t_{PLH} t_{PHL}	Propagation delay Waveform 2, '241		18 18	9 9		ns
t_{PZH}	Enable to HIGH Waveform 3	LS	23			ns
		'S240			10	ns
		'S241			12	ns
t_{PZL}	Enable to LOW Waveform 4		30	15		ns
t_{PHZ}	Disable from HIGH Waveform 3, $C_L = 5\text{pF}$		18	9		ns
t_{PLZ}	Disable from LOW Waveform 4, $C_L = 5\text{pF}$		25	15		ns

AC WAVEFORMS



74LS242, LS243, S242, S243

Transceivers

'242 Quad Inverting Transceiver (3-State)

'243 Quad Transceiver (3-State)

Product Specification

FUNCTION TABLE, '242

INPUTS		INPUT/OUTPUT	
\overline{OE}_A	OE_B	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = \overline{B}$	INPUT

FUNCTION TABLE, '243

INPUTS		INPUT/OUTPUT	
\overline{OE}_A	OE_B	A_n	B_n
L	L	INPUT	$B = A$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = B$	INPUT

H = HIGH voltage level
 L = LOW voltage level
 (Z) = HIGH impedance (off) state
 (a) = This condition is not allowed due to excessive currents.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS242	10ns	27mA
74LS243	12ns	28mA
74S242	6.0ns	95mA
74S243	7.0ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS242N, N74LS243N, N74524N, N745243N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

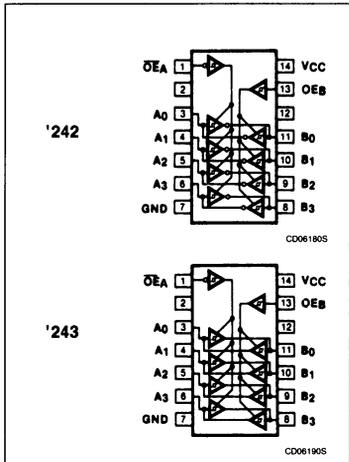
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS	74S
All	Inputs	1LSul	1Sul
A, B	Outputs	30LSul	10Sul

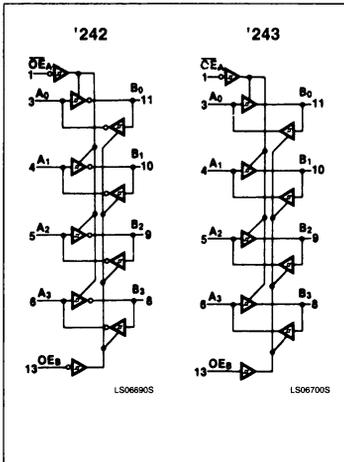
NOTE:

Where a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$ and 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

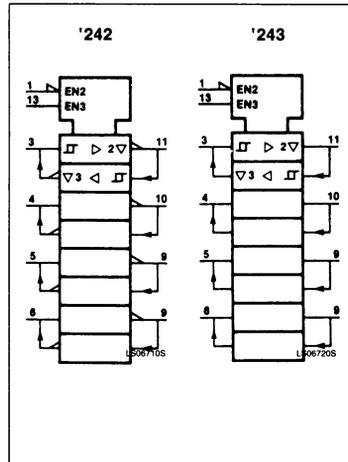
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceivers

74LS242, LS243, S242, S243

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			-0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	HIGH-level output current			-15			-15	mA
I _{OL}	LOW-level output current			24			64	mA
T _A	Operating free-air temperature	0		70	0		70	°C

Transceivers

74LS242, LS243, S242, S243

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74LS242 74LS243			74S242 74S243			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$		0.2	0.4		0.2	0.4		V
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = 0.5V, I_{OH} = \text{MAX}$		2.0			2.0			V
	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -3\text{mA}$		2.4	3.1		2.4	3.4		V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.35	0.5			0.55	
		$I_{OL} = 12\text{mA} (74\text{LS})$		0.25	0.4				V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5			-1.2	V
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_O = 2.7V$				40			50	μA
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_O = 0.4V$				-200			-400	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$	A, B inputs			0.1		1.0	mA
		$V_I = 7.0V$	$\overline{OE}_A, \overline{OE}_B$ inputs			0.1			mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$				20			50	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4V$	A inputs $\overline{OE}_A, \overline{OE}_B = V_{IL} = \text{MAX}$			-0.2			-0.4	mA
		B inputs $\overline{OE}_A, \overline{OE}_B = V_{IH} = \text{MIN}$			-0.2			-0.4	mA
		$\overline{OE}_A, \overline{OE}_B$ inputs			-0.2			-2	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$		-40		-130	-80		-180	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	'242	22	38		80	135	mA
		I_{CCL} Outputs LOW		29	50		100	150	mA
		I_{CCZ} Outputs OFF		29	50		100	150	mA
		I_{CCH} Outputs HIGH	'243	22	38		95	160	mA
		I_{CCL} Outputs LOW		29	50		120	180	mA
		I_{CCZ} Outputs OFF		32	54		120	180	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with outputs open and transceivers enabled in one direction only, or with all transceivers disabled.

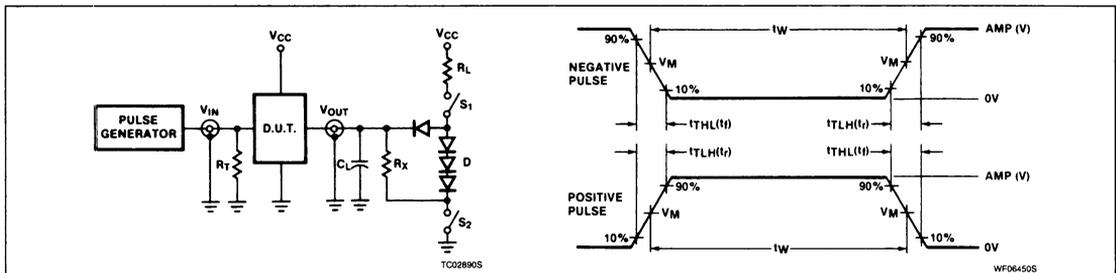
Transceivers

74LS242, LS243, S242, S243

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS242		74LS243		74S242		74S243		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 50\text{pF}$, $R_L = 90\Omega$		$C_L = 50\text{pF}$, $R_L = 90\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		14			7			ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2				18			9	ns
t_{PZH}	Enable to HIGH	Waveform 3		23	23		12		12	ns
t_{PZL}	Enable to LOW	Waveform 4		30	30		15		15	ns
t_{PHZ}	Disable from HIGH	Waveform 3, $C_L = 5\text{pF}$		18	18		9		9	ns
t_{PLZ}	Disable from LOW	Waveform 4, $C_L = 5\text{pF}$		25	25		15		15	ns

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

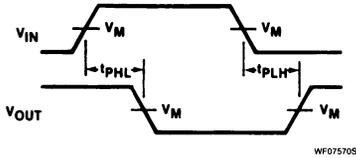
$R_X = 1\text{k}\Omega$ for 74, 74S. $R_X = 5\text{k}\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Transceivers

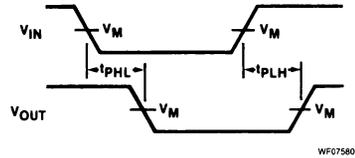
74LS242, LS243, S242, S243

AC WAVEFORMS



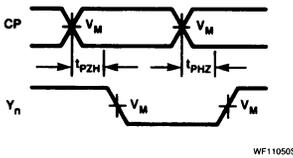
$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 1. Waveform For Inverting Outputs



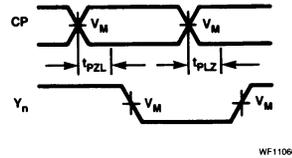
$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 2. Waveform For Non-Inverting Outputs



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 3. 3-State Enable Time To High Level and Disable Time From High Level



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 4. 3-State Enable Time To Low Level And Disable Time From Low Level

74LS244, S244

Buffers

Octal Buffers (3-State)
Product Specification

Logic Products

FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{OE}_a	I_a	\overline{OE}_b	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS244	12ns	25mA
74S244	6ns	112mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS244N, 74S244N
Plastic SOL-20	74LS244D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

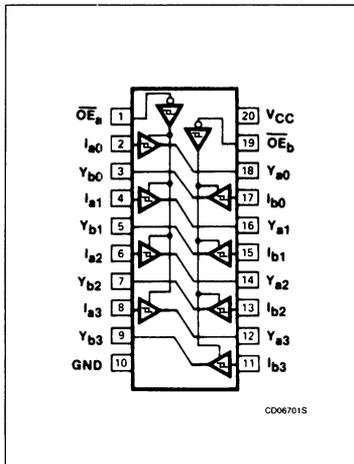
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	24Sul	30LSul

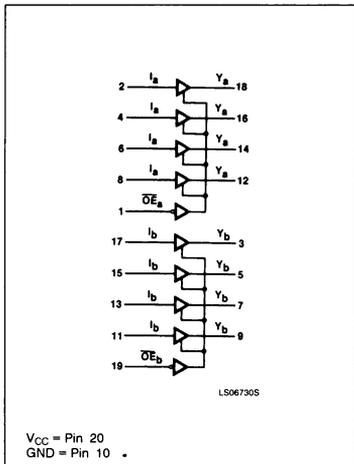
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

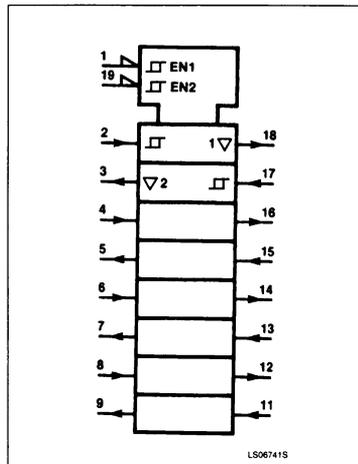
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffers

74LS244, S244

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

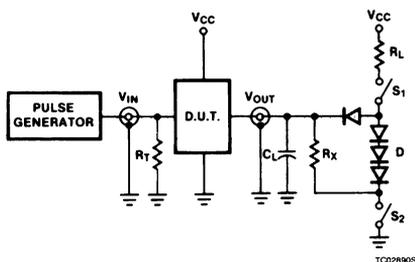
PARAMETER	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-18			-18	mA
I _{OH} HIGH-level output current			-15			-15	mA
I _{OL} LOW-level output current			24			64	mA
T _A Operating free-air temperature	0		70	0		70	°C

5

TEST CIRCUITS AND WAVEFORMS



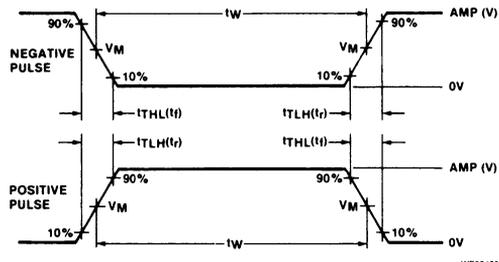
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t _{pZH}	Open	Closed
t _{pZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffers

74LS244, S244

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS244			74S244			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4		V
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = 0.5V$, $I_{OH} = \text{MAX}$	2.0			2.0			V
	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = \text{MAX}$	2.4	3.4		2.4			V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.5		0.55		V
		$I_{OL} = 12\text{mA}$ (74LS)		0.4				V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5			-1.2	V
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$V_O = 2.7V$		20				μA
		$V_O = 2.4V$				50		μA
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$V_O = 0.4V$		-20				μA
		$V_O = 0.5V$				-50		μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$					1.0	mA
		$V_I = 7.0V$		0.1				mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7V$			20			50	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4V$		-0.2				mA
		$V_I = 0.5V$	\overline{OE} inputs				-2.0	mA
			Other inputs				-0.4	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$	-40		-130	-80		-180	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		17	27	95	160	mA
		I_{CCL} Outputs LOW		27	46	120	180	mA
		I_{CCZ} Outputs OFF		32	54		120	180

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with outputs open.

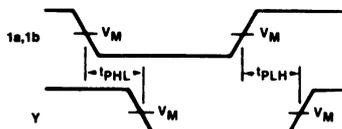
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 50\text{pF}$, $R_L = 90\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		18		9	ns
t_{PHL} Propagation delay	Waveform 1		18		9	ns
t_{PZH} Enable to HIGH	Waveform 2		23		12	ns
t_{PZL} Enable to LOW	Waveform 3		30		15	ns
t_{PHZ} Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$		18		9	ns
t_{PLZ} Disable from LOW	Waveform 3, $C_L = 5\text{pF}$		25		15	ns

Buffers

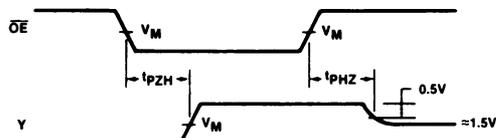
74LS244, S244

AC WAVEFORMS



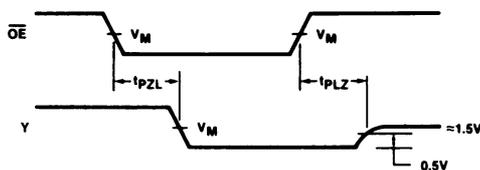
WF08670S

Waveform 1. Waveform For Non-Inverting Outputs



WF08680S

Waveform 2. 3-State Enable Time To High Level And Disable Time From High Level



WF08690S

For all waveforms, $V_M = 1.3V$ for 74LS, $V_M = 1.5V$ for all other TTL families.

Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

74LS245 Transceiver

Octal Transceiver (3-State)
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs

DESCRIPTION

The 'LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All data inputs have hysteresis built in to minimize AC noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS245	8ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS245N
Plastic SOL-20	N74LS245D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

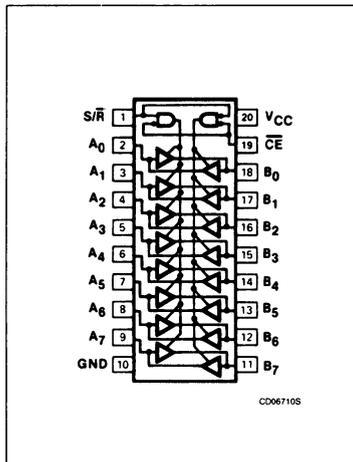
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

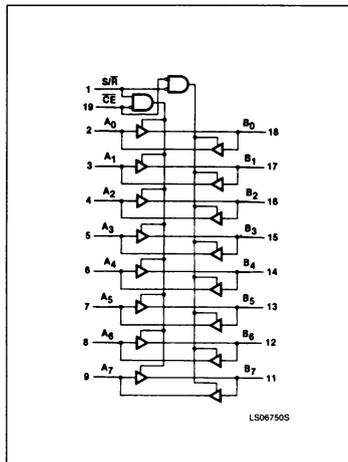
NOTE:

Where a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

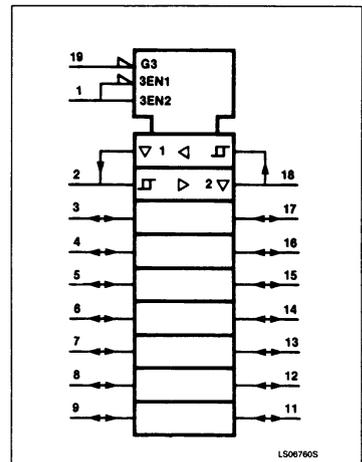
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceiver

74LS245

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/ \overline{R}	A _n	B _n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

NOTE
 V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V _{CC}	4.75	5.0	5.25	V
V _{IH}	2.0			V
V _{IL}			+0.8	V
I _{IK}			-18	mA
I _{OH}			-15	mA
I _{OL}			24	mA
T _A	0		70	°C

Transceiver

74LS245

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		74LS245			UNIT
				Min	Typ ²	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$		0.2	0.4		V
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_L = \text{MAX}$	$I_{OH} = \text{MAX}$	2.0			V
			$I_{OH} = -3\text{mA}$	2.4	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$			0.5	V
			$I_{OL} = 12\text{mA}$ (74LS)			0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, $V_O = 2.7\text{V}$, $\overline{CE} = 2.0\text{V}$				20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, $V_O = 0.4\text{V}$, $\overline{CE} = 2.0\text{V}$				-200	μA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$	A, B inputs		0.1	mA
			$V_I = 7.0\text{V}$	S/ \overline{R} , \overline{CE} inputs		0.1	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$				20	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$				-0.2	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-40		-130	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		48	70	mA
			I_{CCL} Outputs LOW		62	90	mA
			I_{CCZ} Outputs OFF		64	95	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with outputs open.

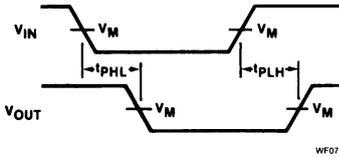
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS		74LS		UNIT
				$C_L = 4\text{pF}$, $R_L = 667\Omega$		
				Min	Max	
t_{PLH}	Propagation delay	Waveform 1			12	ns
t_{PHL}	Propagation delay	Waveform 1			12	ns
t_{PZH}	Enable to HIGH	Waveform 2			40	ns
t_{PZL}	Enable to LOW	Waveform 3		-	40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$			25	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5\text{pF}$			25	ns

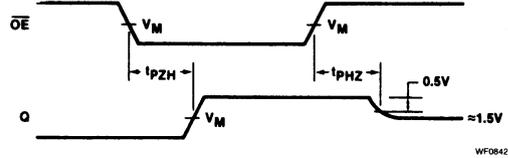
Transceiver

74LS245

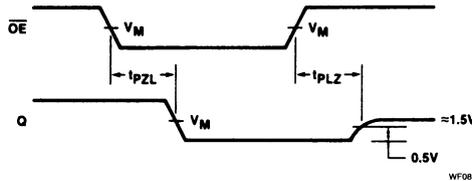
AC WAVEFORMS



Waveform 1. Waveform For Non-Inverting Outputs



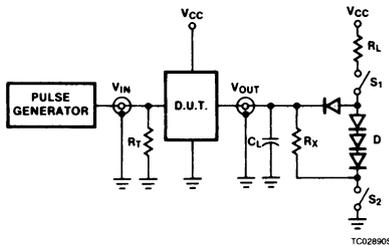
Waveform 2. 3-State Enable Time To High Level And Disable Time From High Level



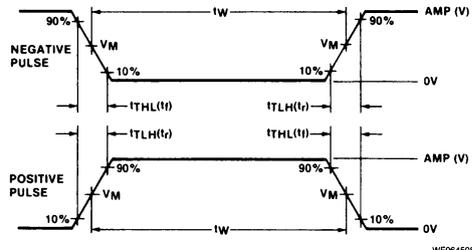
For all waveforms, $V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74LS, $R_X = 5k\Omega$ for 74ALS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS251, S251 Multiplexers

8-Input Multiplexer (3-State)
Product Specification

Logic Products

FEATURES

- High speed 8-to-1 multiplexing
- True and complement outputs
- Both outputs are 3-State for further multiplexer expansion
- 3-State outputs are buffer type with 12mA/24mA outputs for Military/Commercial applications

DESCRIPTION

The '251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and Negation (\bar{Y}) outputs are both provided. The Output Enable input (\bar{OE}) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \bar{OE} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

Both outputs are in the HIGH impedance (HIGH Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in

TYPE	TYPICAL PROPAGATION DELAY (DATA TO Y)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS251	18ns	9mA
74S251	8ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S251N, N74LS251AN

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

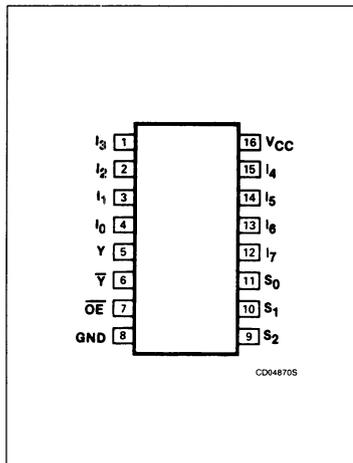
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

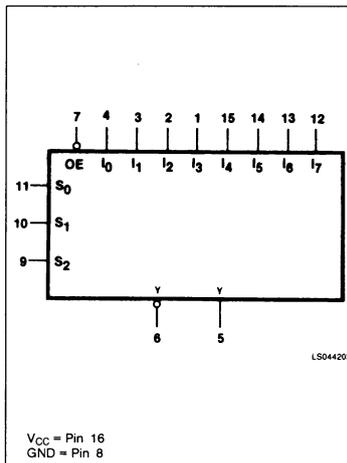
the HIGH impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design

of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

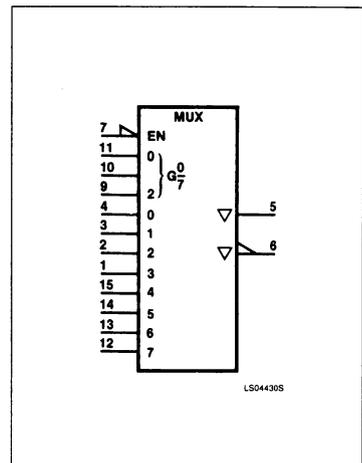
PIN CONFIGURATION



LOGIC SYMBOL



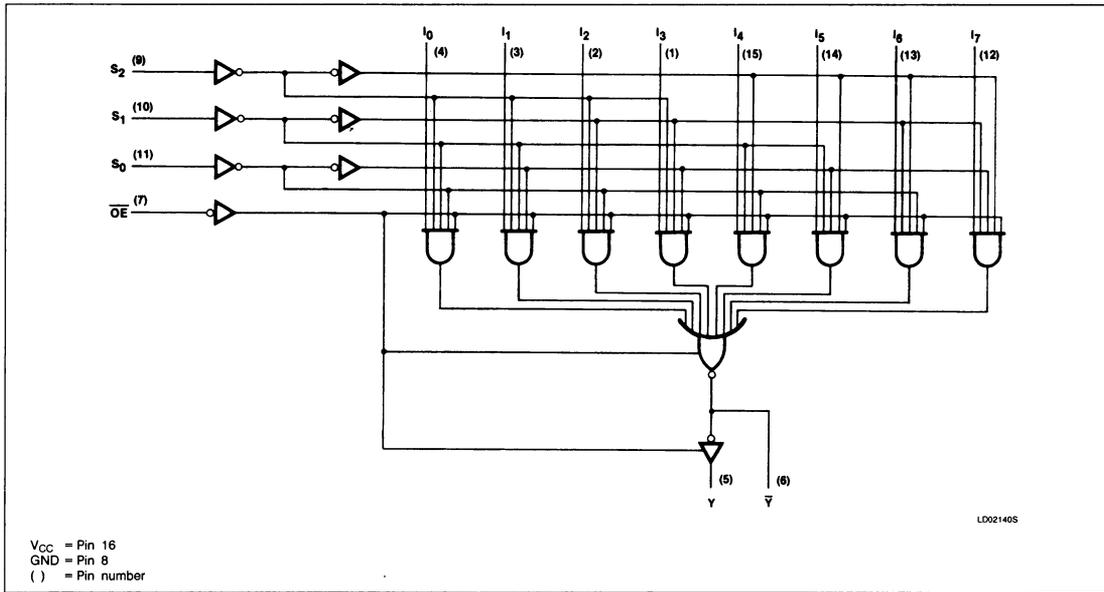
LOGIC SYMBOL (IEEE/IEC)



Multiplexers

74LS251, S251

LOGIC DIAGRAM



5

FUNCTION TABLE

INPUTS													OUTPUTS	
\overline{OE}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\overline{Y}	Y	
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)	
L	L	L	L	L	X	X	X	X	X	X	X	H	L	
L	L	L	L	L	H	X	X	X	X	X	X	L	H	
L	L	L	L	H	X	X	X	X	X	X	X	H	L	
L	L	L	H	X	X	X	X	X	X	X	X	L	H	
L	L	L	H	X	X	L	X	X	X	X	X	H	L	
L	L	L	H	X	X	X	L	X	X	X	X	L	H	
L	L	L	H	X	X	X	H	X	X	X	X	H	L	
L	L	H	L	L	X	X	X	L	X	X	X	L	H	
L	L	H	L	L	X	X	X	H	X	X	X	H	L	
L	L	H	L	H	X	X	X	X	L	X	X	L	H	
L	L	H	L	H	X	X	X	X	H	X	X	H	L	
L	L	H	H	L	X	X	X	X	X	L	X	L	H	
L	L	H	H	L	X	X	X	X	X	H	X	L	H	
L	L	H	H	H	X	X	X	X	X	X	L	H	L	
L	H	H	H	X	X	X	X	X	X	X	H	L	H	
L	H	H	H	X	X	X	X	X	X	X	L	H	L	
L	H	H	H	X	X	X	X	X	X	X	H	L	H	
L	H	H	H	X	X	X	X	X	X	X	L	H	L	
L	H	H	H	X	X	X	X	X	X	X	H	L	H	
L	H	H	H	X	X	X	X	X	X	X	L	H	L	

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output for HIGH output state	-0.5 to +5.5	-0.5 to +5.5	V
T_A Operating free-air temperature range	0 to 70		°C

Multiplexers

74LS251, S251

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	HIGH-level output current			-2.6			-6.5	mA
I _{OL}	LOW-level output current			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS251			74S251			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.1		2.4	3.2		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)		0.25	0.4			V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V
I _{OZH}	Off-state output current, HIGH-level voltage applied V _{CC} = MAX, V _{IH} = MIN	V _O = 2.4V					50	μA
		V _O = 2.7V			20			μA
I _{OZL}	Off-state output current, LOW-level voltage applied V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V			-20			μA
		V _O = 0.5V					-50	μA
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V					1.0	mA
		V _I = 7.0V			0.1			mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.7V			20		50	μA
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V			-0.4			mA
		V _I = 0.5V					-2	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-30		-130	-40		-100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX	Outputs LOW		6.1	10			mA
		Outputs HIGH		7.1	12		85	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} on the 74S251 with all inputs at 4.5V and all outputs open. Measure I_{CC} on the 74LS251A in the following manner: 1. *Outputs LOW*: Data and select inputs at 4.5V, output enable grounded and all outputs open. 2. *Outputs HIGH*: Data and select inputs at 4.5V, output enable at 4.5V and all outputs open.

Multiplexers

74LS251, S251

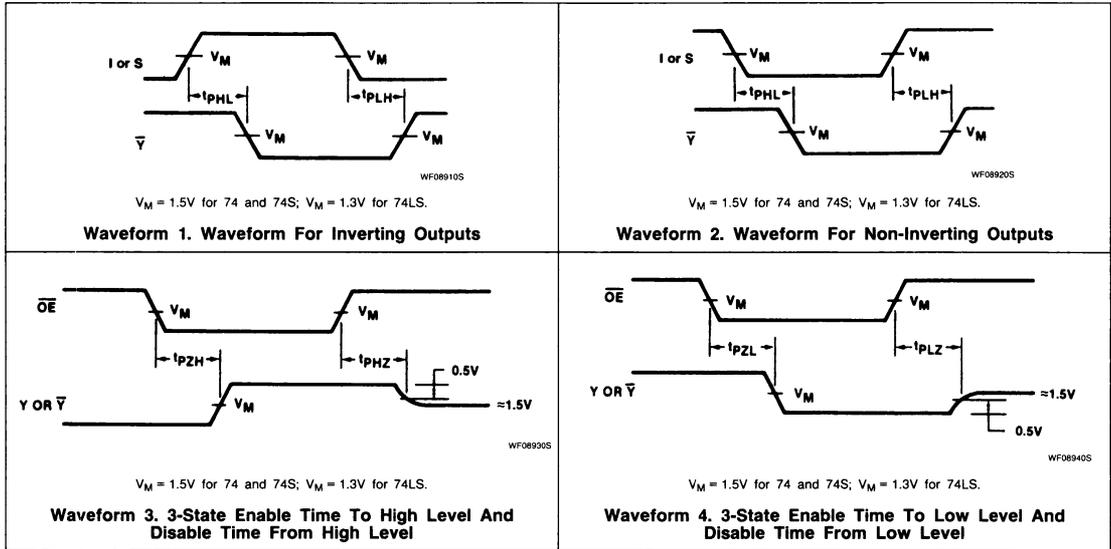
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2	45 45	18 19.5	ns	
t_{PLH} t_{PHL}	Propagation delay Select to \bar{Y} output	Waveform 1	33 33	15 13.5	ns	
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2	28 28	12 12	ns	
t_{PLH} t_{PHL}	Propagation delay Data to \bar{Y} output	Waveform 1	15 15	7.0 7.0	ns	
t_{PZH}	Output enable to HIGH level Y output	Waveform 3 $C_L = 50\text{pF}$ for 'S251	45	19.5	ns	
t_{PZL}	Output enable to LOW level Y output	Waveform 4 $C_L = 50\text{pF}$ for 'S251	40	21	ns	
t_{PZH}	Output enable to HIGH level \bar{Y} output	Waveform 3 $C_L = 50\text{pF}$ for 'S251	27	19.5	ns	
t_{PZL}	Output enable to LOW level \bar{Y} output	Waveform 4 $C_L = 50\text{pF}$ for 'S251	40	21	ns	
t_{PHZ}	Output disable from HIGH level	Waveform 3, $C_L = 5\text{pF}$	45	8.5	ns	
t_{PLZ}	Output disable from LOW level	Waveform 4, $C_L = 5\text{pF}$	25	14	ns	

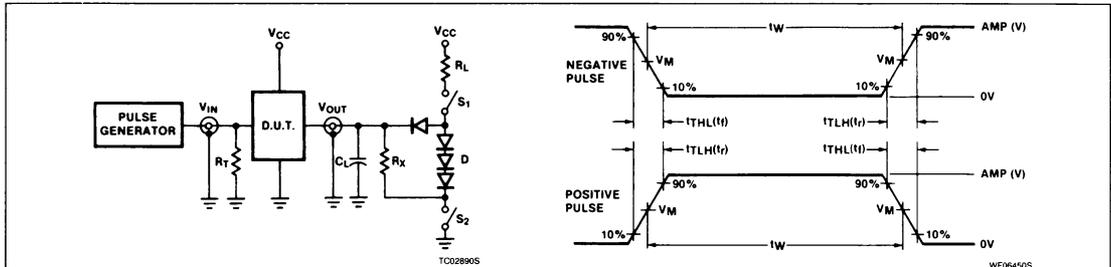
Multiplexers

74LS251, S251

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = $1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS253, S253 Multiplexers

Dual 4-Input Multiplexer (3-State)
Product Specification

Logic Products

FEATURES

- 3-State outputs for bus interface and multiplex expansion
- Common Select inputs
- Separate Output Enable inputs

DESCRIPTION

The '253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\bar{E}_{0a}, \bar{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

TYPE	TYPICAL PROPAGATION DELAY (From Data)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS253	15ns	8mA
74S253	8ns	48mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S253N, N74LS253N
Plastic SO-16	N74LS253D, N74S253D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

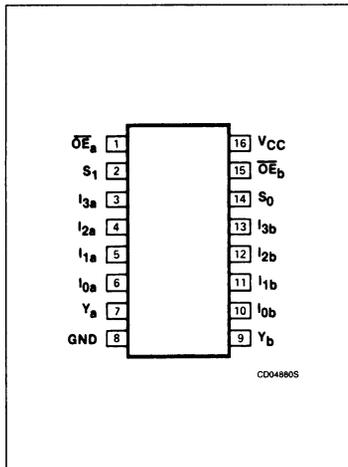
PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE:

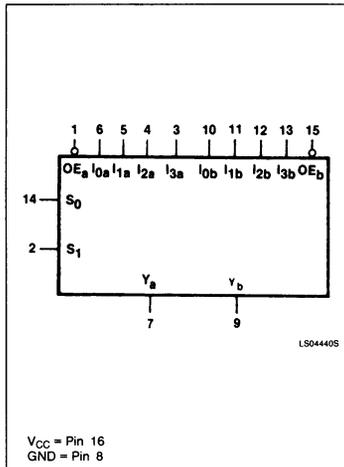
A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

5

PIN CONFIGURATION

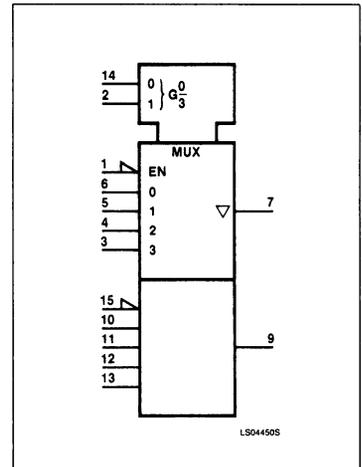


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

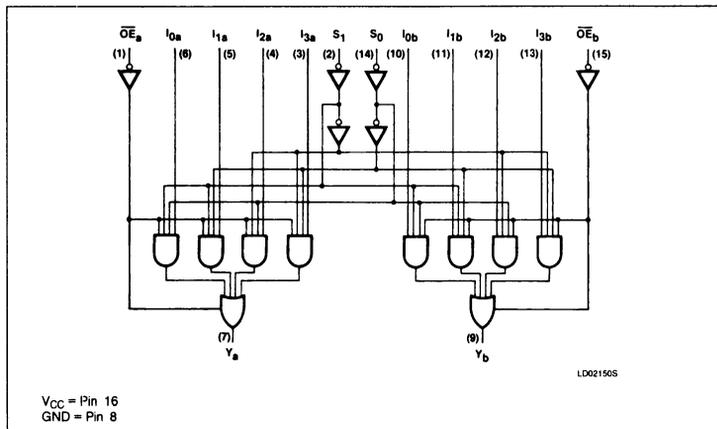
LOGIC SYMBOL (IEEE/IEC)



Multiplexers

74LS253, S253

LOGIC DIAGRAM



The '253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the two outputs are shown below:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S ₀	S ₁	I ₀	I ₁	I ₂	I ₃	\overline{OE}	\overline{Y}
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care.
 (Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	HIGH-level output current			-2.6			-6.5	mA
I _{OL}	LOW-level output current			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	°C

Multiplexers

74LS253, S253

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS253			74S253			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.1		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5		0.5	V
		I _{OL} = 4mA (74LS)		0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V			20			μA
		V _O = 2.4V					50	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V			-20			μA
		V _O = 0.5V					-50	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA
		V _I = 7.0V			0.1			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V			20		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-0.4			mA
		V _I = 0.5V					-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-15		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		7	12		70	mA
		Condition 2		8.5	14			mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured under the following conditions with the outputs open: *Condition 1*: All inputs grounded. *Condition 2*: \overline{OE} at 4.5V, all inputs grounded.

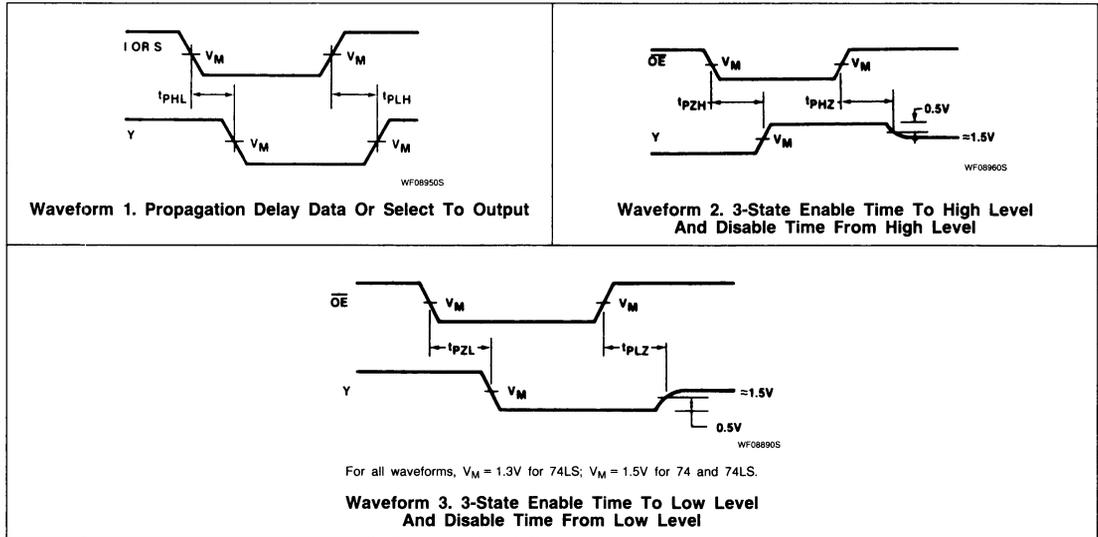
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay Data to Output	Waveform 1		25 20		9.0 9.0	ns
t _{PLH} t _{PHL} Propagation delay Select to output	Waveform 1		45 32		18 18	ns
t _{PZH} Output enable to HIGH level	Waveform 2		28		13	ns
t _{PZL} Output enable to LOW level	Waveform 3		23		14	ns
t _{PHZ} Output disable from HIGH level	Waveform 2, C _L = 5pF		41		8.5	ns
t _{PLZ} Output disable from LOW level	Waveform 3, C _L = 5pF		27		14	ns

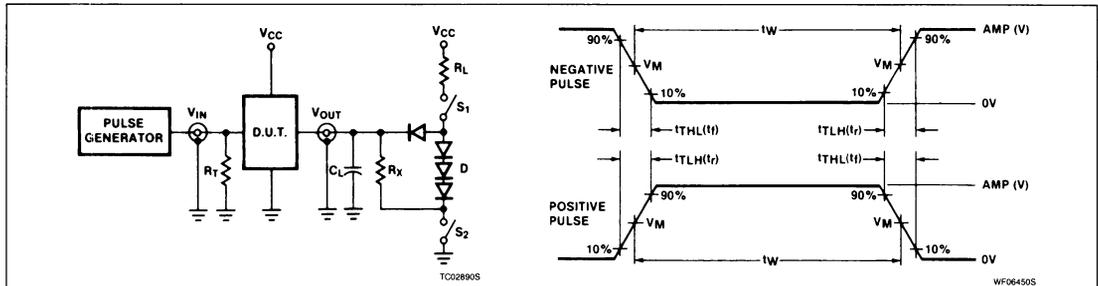
Multiplexers

74LS253, S253

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = $1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS256 Latch

Dual 4-Bit Addressable Latch
Product Specification

Logic Products

FEATURES

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-4 active HIGH decoder

DESCRIPTION

The '256 dual addressable latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS256	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS256N
Plastic SO-16	N74LS256D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
\bar{E}	Input	2LSul
Other	Inputs	1LSul
All	Outputs	10LSul

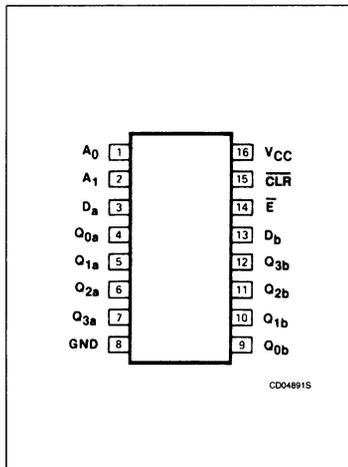
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

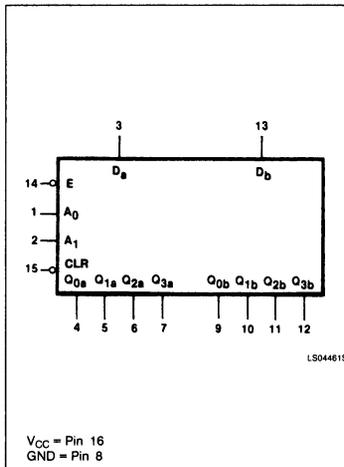
should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\bar{CLR} = \bar{E} = LOW$), addressed outputs will follow the level of the D inputs, with

all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

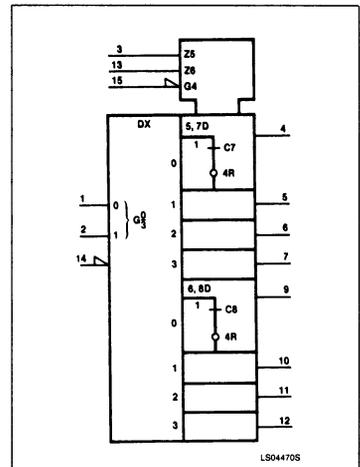
PIN CONFIGURATION



LOGIC SYMBOL



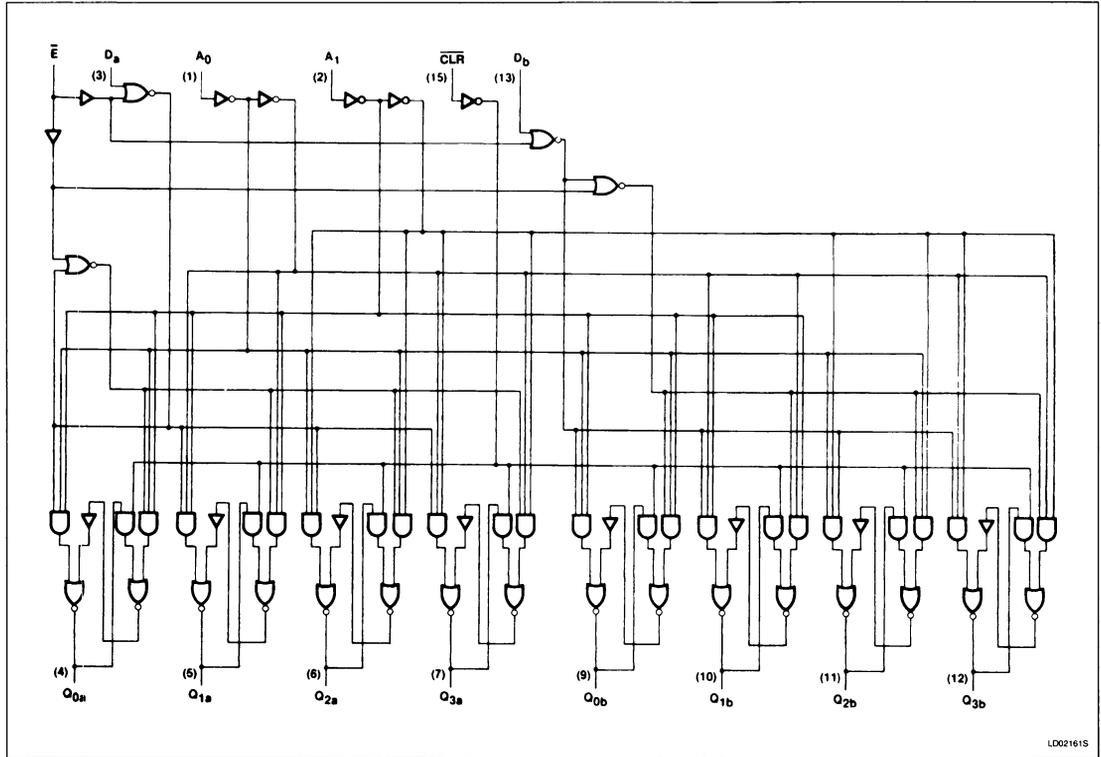
LOGIC SYMBOL (IEEE/IEC)



Latch

74LS256

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	CLR̄	Ē	D	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃
Clear	L	H	X	X	X	L	L	L	L
Demultiplex (active HIGH) decoder when D = H)	L	L	d	L	L	Q = d	L	L	L
	L	L	d	H	L	L	Q = d	L	L
	L	L	d	L	H	L	L	Q = d	L
	L	L	d	H	H	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	q ₀	q ₁	q ₂	q ₃
Addressable latch	H	L	d	L	L	Q = d	q ₁	q ₂	q ₃
	H	L	d	H	L	q ₀	Q = d	q ₂	q ₃
	H	L	d	L	H	q ₀	q ₁	Q = d	q ₃
	H	L	d	H	H	q ₀	q ₁	q ₂	Q = d

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

X = Don't care.

d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH Enable transition.

q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

Latch

74LS256

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74256			UNIT		
		Min	Typ ²	Max			
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$		2.7		V	
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.5	V	
			$I_{OL} = 4\text{mA}$		0.4	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			1.0	mA	
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$	\bar{E} input		40	μA	
			Other inputs		20	μA	
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	\bar{E} input		-0.8	mA	
			Other inputs		-0.4	mA	
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-15	-100	mA	
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$			22	36	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Latch

74LS256

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT	
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$			
		Min	Max		
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		35 24	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		32 21	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 3		38 29	ns
t_{PHL}	Propagation delay, Clear to output	Waveform 4		27	ns

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT	
		Min	Max		
t_W	Enable pulse width	Waveform 1	15		ns
t_W	Clear pulse width	Waveform 4	15		ns
$t_S(H)$	Set-up time HIGH, Data to Enable	Waveform 5	15		ns
$t_H(H)$	Hold time HIGH, Data to Enable	Waveform 5	0		ns
$t_S(L)$	Set-up time LOW, Data to Enable	Waveform 5	15		ns
$t_H(L)$	Hold time LOW, Data to Enable	Waveform 5	0		ns
t_S	Set-up time, Address to Enable ^(a)	Waveform 6	15		ns
t_H	Hold time, Address to Enable ^(b)	Waveform 6	0		ns

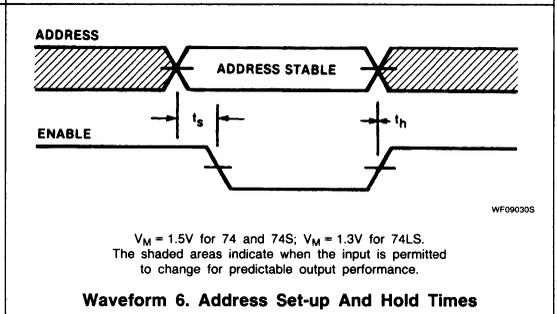
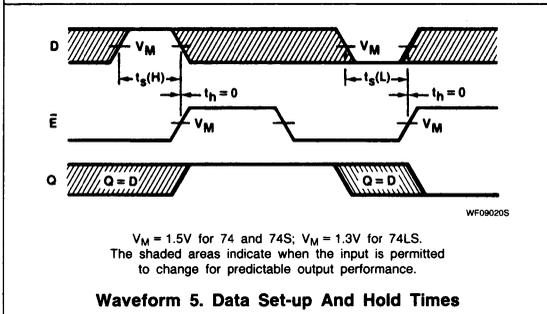
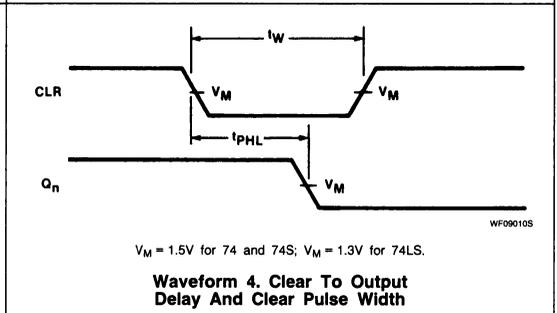
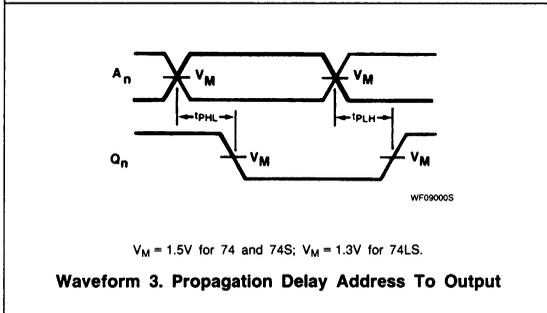
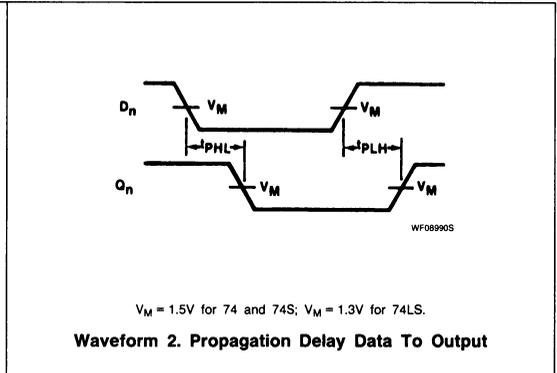
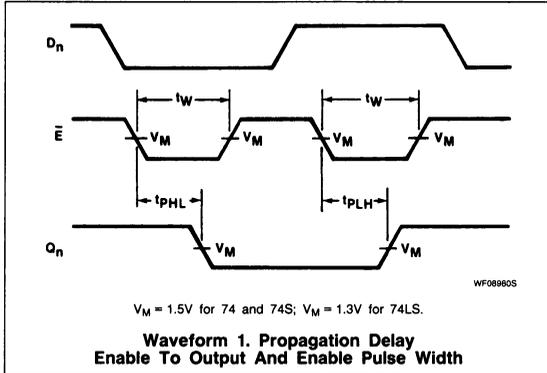
NOTE:

- a. The Address to Enable set-up time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

Latch

74LS256

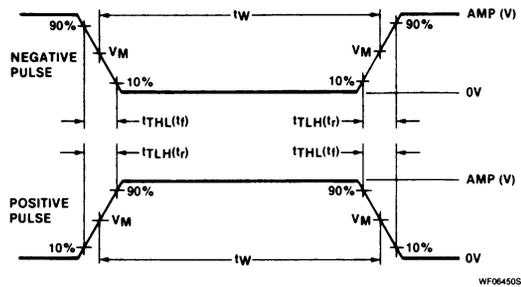
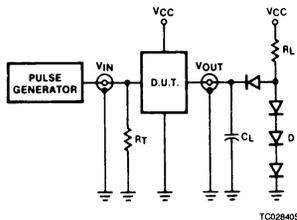
AC WAVEFORMS



Latch

74LS256

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS257A, S257 Data Selectors/Multiplexers

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)
Product Specification

Logic Products

FEATURES

- Multifunction capability
- Non-inverting data path
- 3-State outputs

DESCRIPTION

The '257 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The '257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS257A	13ns	9mA
74S257	6.6ns	56mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S257N, N74S257AN
Plastic SO-16	N74S257D
Plastic SOL-16	CD7193D
Plastic SOL-16	N74LS257D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

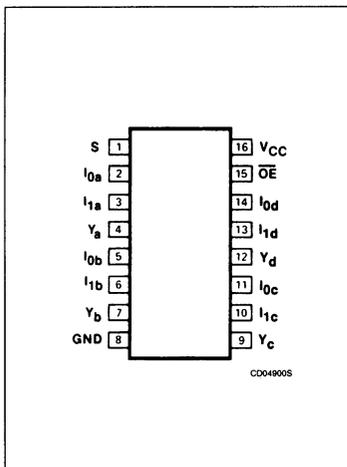
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S
S	Inputs	2Sul	2LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

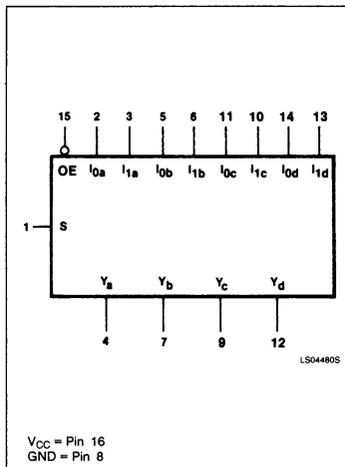
NOTE:

A 74S unit load (Sul) is understood to be $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

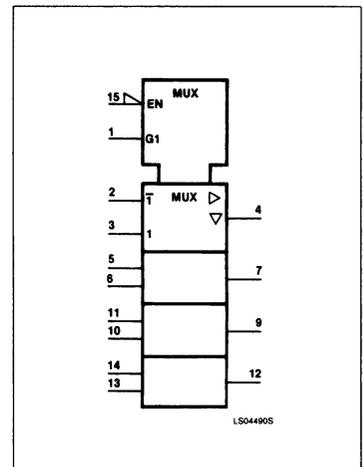
PIN CONFIGURATION



LOGIC SYMBOL



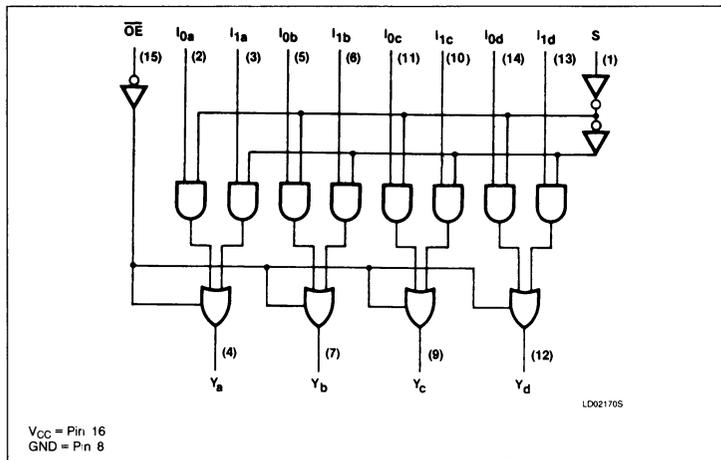
LOGIC SYMBOL (IEEE/IEC)



Data Selectors/Multiplexers

74LS257A, S257

LOGIC DIAGRAM



Outputs are forced to a HIGH impedance "off" state when the Output Enable input (\overline{OE}) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

FUNCTION TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
		I_0	I_1	
\overline{OE}	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	HIGH-level output current			-2.6			-6.5	mA
I _{OL}	LOW-level output current			24			20	mA
T _A	Operating free-air temperature	0		70	0		70	°C

Data Selectors/Multiplexers

74LS257A, S257

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74LS257A			74S257			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OH} = MAX	2.4	3.1		2.4	3.2		V
		I _{OH} = -1mA (74S)				2.7			V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5			0.5	V
		I _{OL} = 12mA (74LS)		0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _i = I _{IK}				-1.5			-1.2	V
I _{ozH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V			20				μA
		V _O = 2.4V						50	μA
I _{ozL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V			-20				μA
		V _O = 0.5V						-50	μA
I _i Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA
			S input		0.2				mA
		V _I = 7.0V	Other inputs		0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	S input		40			100	μA
			Other inputs		20			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	S input		-0.8				mA
			Other inputs		-0.4				mA
		V _I = 0.5V	S input					-4	mA
Other inputs						-2	mA		
I _{os} Short-circuit output current ³	V _{CC} = MAX		-30		-130	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH	6.2	10		44	68		mA
		I _{CC} L Outputs LOW	10	16		60	93		mA
		I _{CC} Z Outputs OFF	12	19		64	99		mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{os} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.

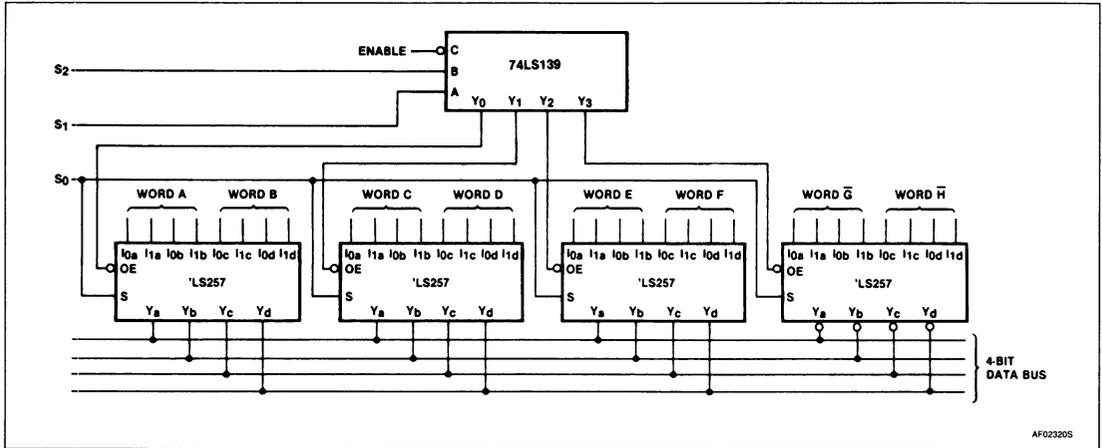
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C _L = 45pF, R _L = 667Ω		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 1		18 18	7.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay Select to output	Waveform 1		21 21	15 15	ns
t _{PZH}	Output enable to HIGH level	Waveform 2		30	19.5	ns
t _{PZL}	Output enable to LOW level	Waveform 3		30	21	ns
t _{PHZ}	Output disable from HIGH level	Waveform 2, C _L = 5pF		30	8.5	ns
t _{PLZ}	Output disable from LOW level	Waveform 3, C _L = 5pF		25	14	ns

Data Selectors/Multiplexers

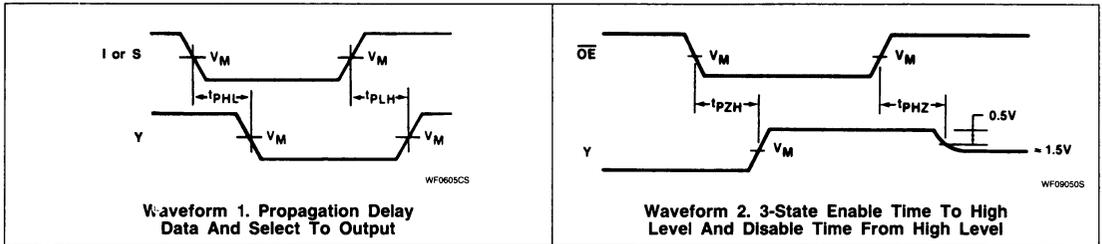
74LS257A, S257

APPLICATION DIAGRAM



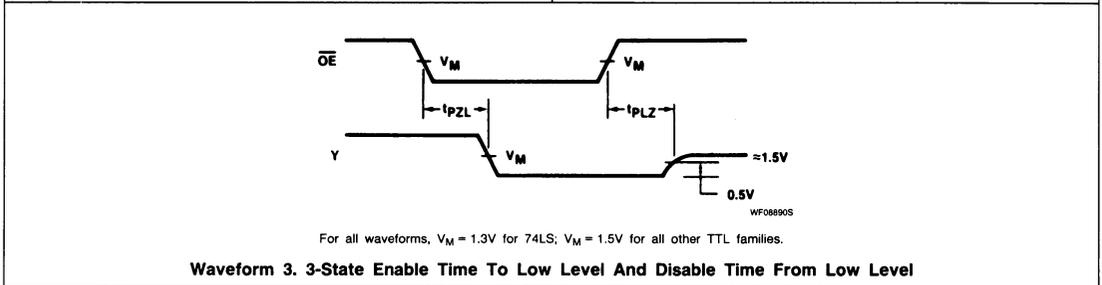
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AC WAVEFORMS



WF0605CS

WF090505



WF088905

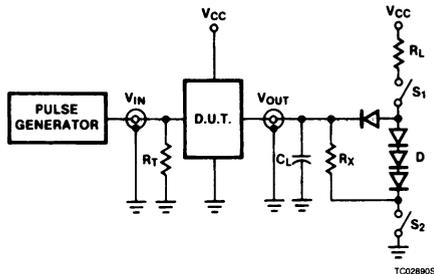
For all waveforms, $V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

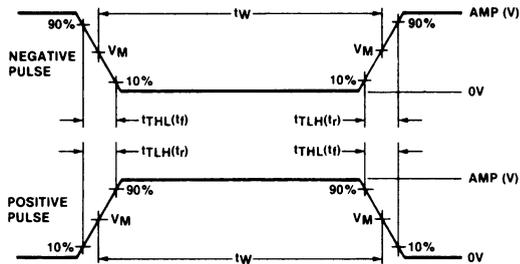
Data Selectors/Multiplexers

74LS257A, S257

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS258A, S258 Data Selectors/Multiplexers

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)
Product Specification

Logic Products

FEATURES

- Multifunction capability
- Inverting data path
- 3-State outputs
- See '257 for non-inverting version

DESCRIPTION

The '258 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in inverted (complementary) form.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS258A	13ns	9mA
74S258	6ns	48mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S258N, N74LS258AN
Plastic SOL-16	N74LS258AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

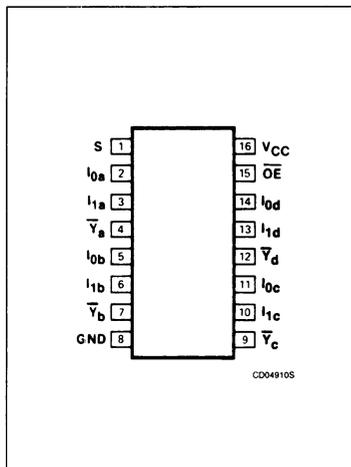
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
S	Input	2Sul	2LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

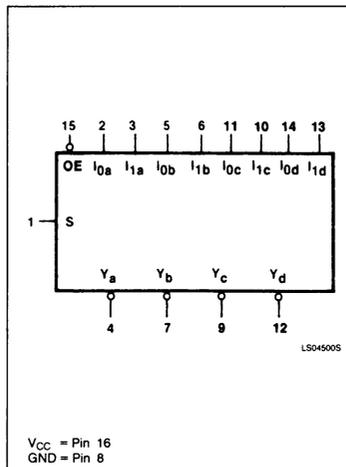
NOTE:

Where a 74S unit load (Sul) is to be $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

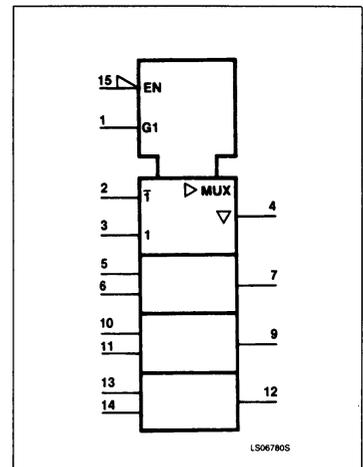
PIN CONFIGURATION



LOGIC SYMBOL



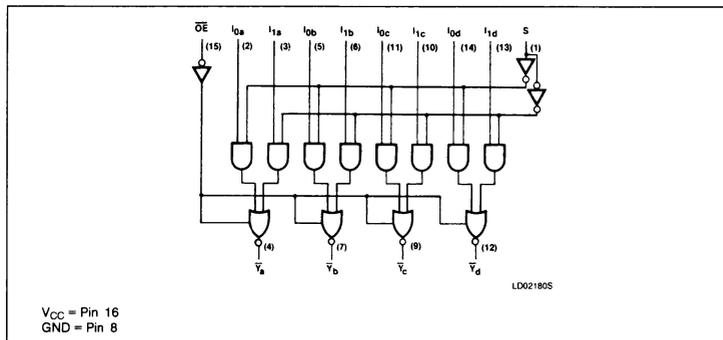
LOGIC SYMBOL (IEEE/IEC)



Data Selectors/Multiplexers

74LS258A, S258

LOGIC DIAGRAM



The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input (\overline{OE}) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-state devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
\overline{OE}	S	I_0	I_1	\overline{Y}
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74S	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8	V
I_{IK} Input clamp current			-18			-18	mA
I_{OH} HIGH-level output current			-2.6			-6.5	mA
I_{OL} LOW-level output current			24			20	mA
T_A Operating free-air temperature	0		70	0		70	°C

Data Selectors/Multiplexers

74LS258A, S258

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74LS258A			74S258			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OH} = MAX	2.4	3.1		2.4	3.2		V	
		I _{OH} = -1mA (74S)				2.7			V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5			0.5	V	
		I _{OL} = 12mA (74LS)		0.25	0.4				V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V			20				μA	
		V _O = 2.4V						50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V			-20				μA	
		V _O = 0.5V						-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA	
		V _I = 7.0V	S input		0.2				mA	
			Other inputs		0.1				mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	S input		40			100	μA	
			Other inputs		20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	S input		-0.8				mA	
			Other inputs		-0.4				mA	
		V _I = 0.5V	S input						-4	mA
			Other inputs						-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-30		-130	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH		4	7		36	56	mA	
		I _{CC} L Outputs LOW		8.8	14		52	81	mA	
		I _{CC} Z Outputs OFF		12	19		56	87	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.

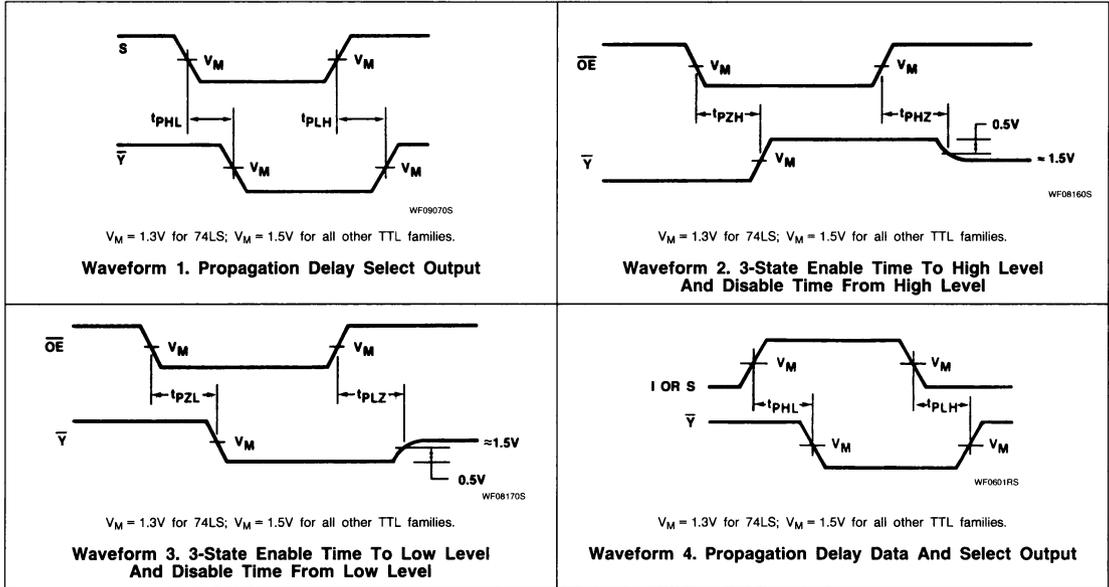
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT	
		C _L = 45pF, R _L = 667Ω		C _L = 15pF, R _L = 280Ω			
		Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 4			18 18	6.0 6.0	ns
t _{PLH} t _{PHL}	Propagation delay Select to output	Waveforms 1 & 4			21 21	12 12	ns
t _{PZH}	Output enable to HIGH level	Waveform 2			30	19.5	ns
t _{PZL}	Output enable to LOW level	Waveform 3			30	21	ns
t _{PHZ}	Output disable from HIGH level	Waveform 2, C _L = 5pF			30	8.5	ns
t _{PLZ}	Output disable from LOW level	Waveform 3, C _L = 5pF			25	14	ns

Data Selectors/Multiplexers

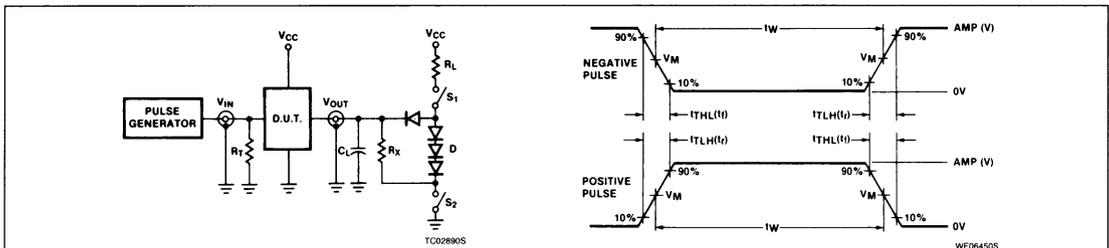
74LS258A, S258

AC WAVEFORMS



5

TEST CIRCUITS AND WAVEFORMS



SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- $R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS259 Latch

8-Bit Addressable Latch
Product Specification

Logic Products

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as a 1-of-8 active HIGH decoder

DESCRIPTION

The '259 addressable latch has four distinct modes of operation that are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS259	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS259N
Plastic SO-16	N74LS259D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	10LSul

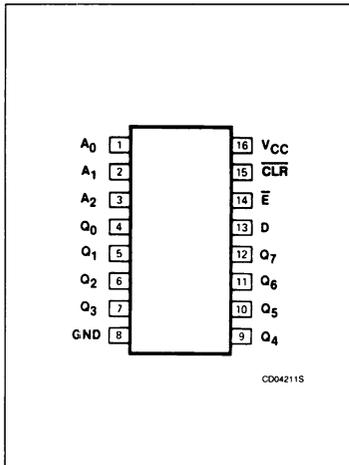
NOTE:

A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

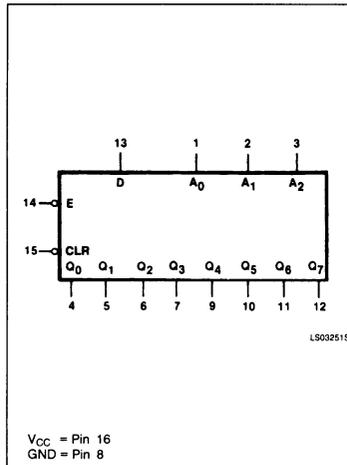
latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{CLR} = \overline{E} = LOW$), addressed outputs will follow the level of

the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

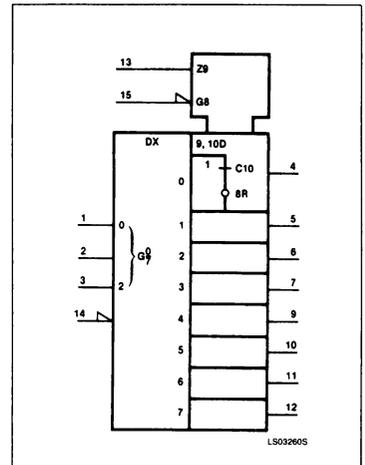
PIN CONFIGURATION



LOGIC SYMBOL



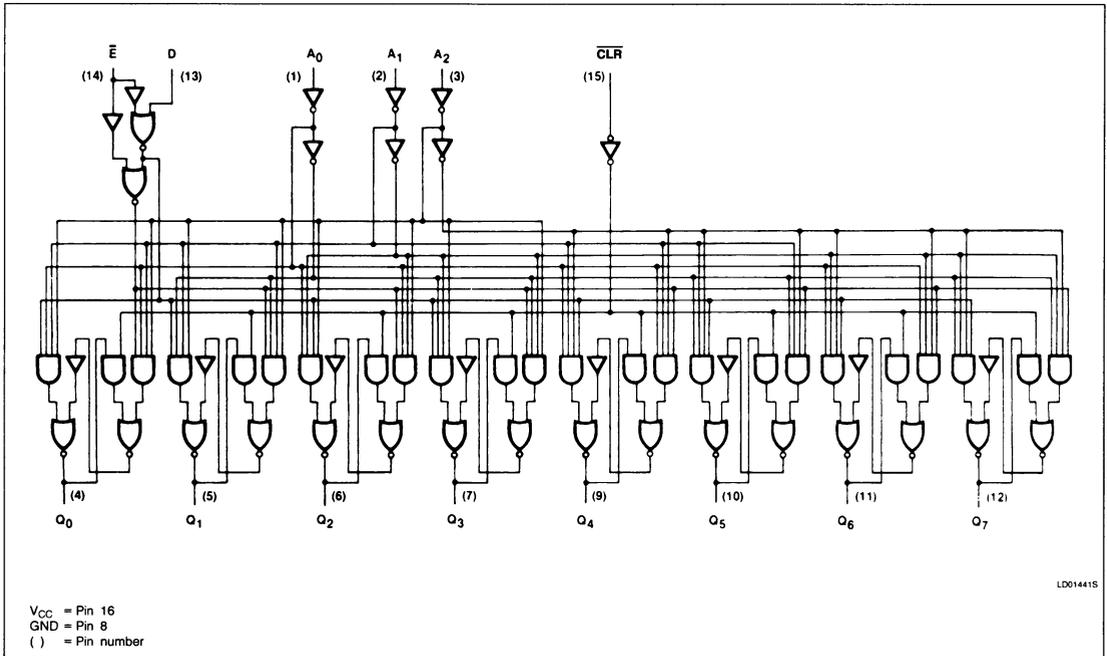
LOGIC SYMBOL (IEEE/IEC)



Latch

74LS259

LOGIC DIAGRAM



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MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	CLR	E-bar	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L

	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q = d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q = d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q = d	q ₃	q ₄	q ₅	q ₆	q ₇

	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q = d

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

X = Don't care.

d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH Enable transition.

q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

Latch

74LS259

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IH}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-400	μA
I _{OL}	LOW-level output current			8	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS259			UNIT		
		Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.7	3.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX			0.35	0.5	V
		I _{OL} = MAX			0.25	0.4	V
	I _{OL} = 4mA (74LS)						V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				0.1	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-0.4	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-20		-100	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			22	36	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the inputs grounded and the outputs open.

Latch

74LS259

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1	35 24	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2	32 21	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 3	38 29	ns
t_{PHL}	Propagation delay, clear to output	Waveform 4	27	ns

AC SET-UP REQUIREMENTS

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W	Enable pulse width	Waveform 1	15	ns
t_W	Clear pulse width	Waveform 4	15	ns
$t_s(H)$	Set-up time HIGH, data to enable	Waveform 5	15	ns
$t_h(H)$	Hold time HIGH, data to enable	Waveform 5	5	ns
$t_s(L)$	Set-up time LOW, data to enable	Waveform 5	15	ns
$t_h(L)$	Hold time LOW, data to enable	Waveform 5	5	ns
t_s	Set-up time, address to enable ^(a)	Waveform 6	15	ns
t_h	Hold time, address to enable ^(b)	Waveform 6	15	ns

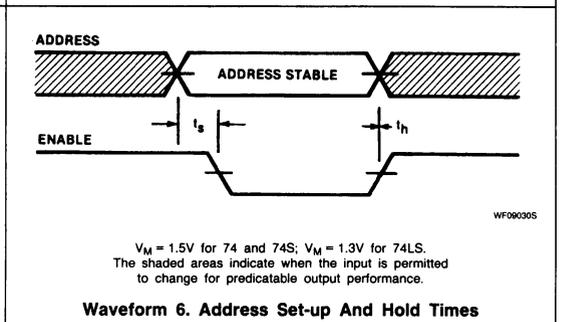
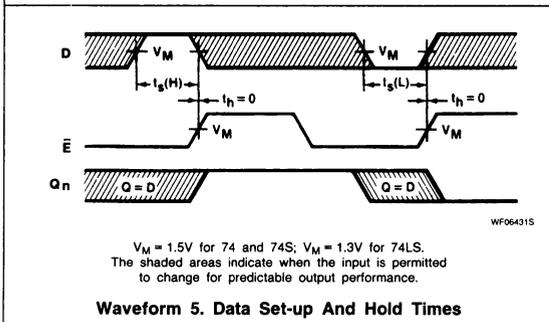
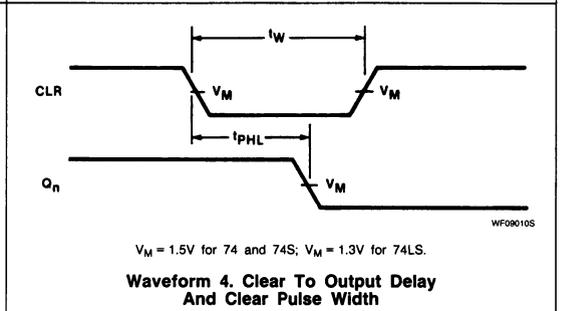
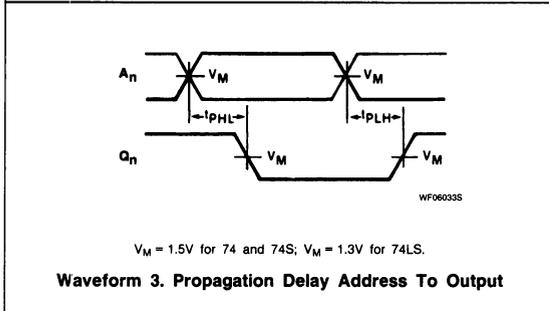
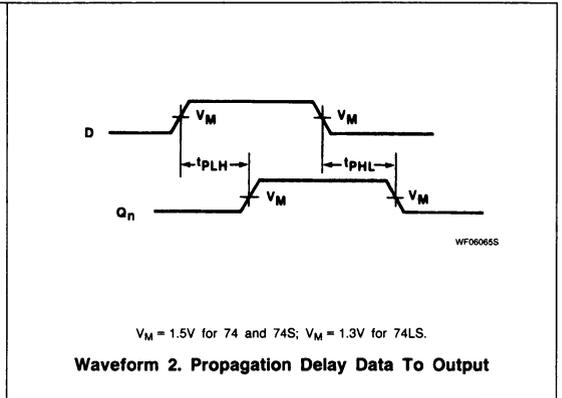
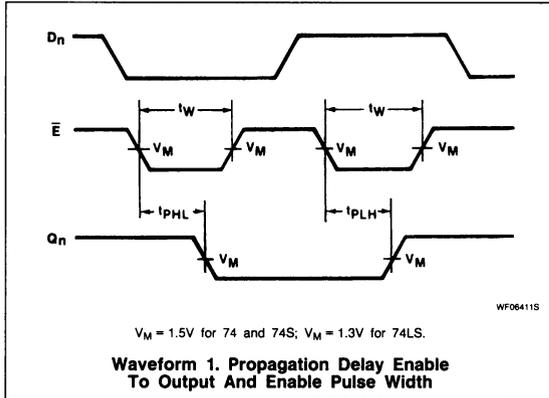
NOTES:

- a. The Address to Enable set-up time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

Latch

74LS259

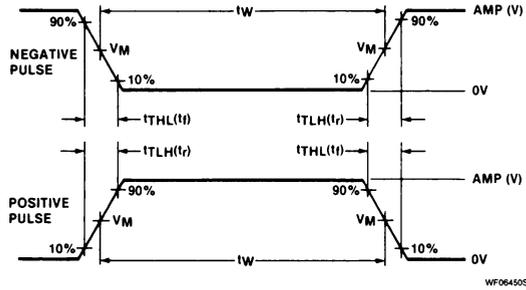
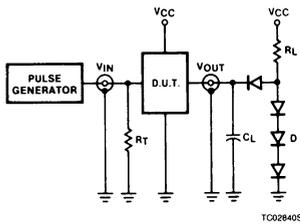
AC WAVEFORMS



Latch

74LS259

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS260, S260 Gates

Dual 5-Input NOR Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS260	9ns	4mA
74S260	4ns	22mA

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S260N, N74LS260N
Plastic SO-14	N74LS260D, N74S260D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

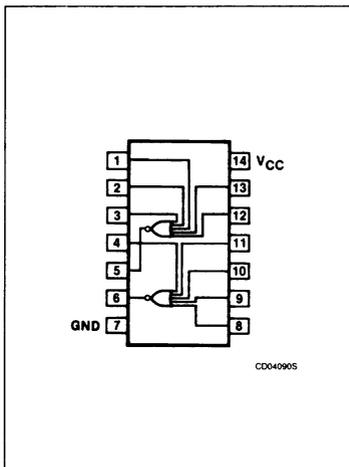
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
A - E	Inputs	1Sul	1LSul
Y	Outputs	10Sul	10LSul

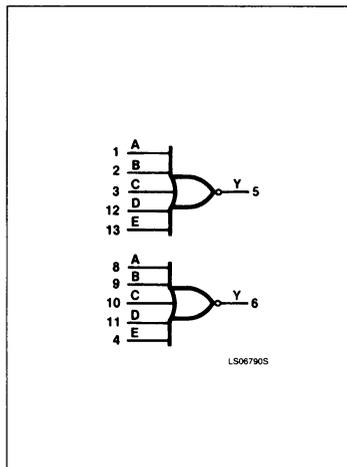
NOTE:

Where a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

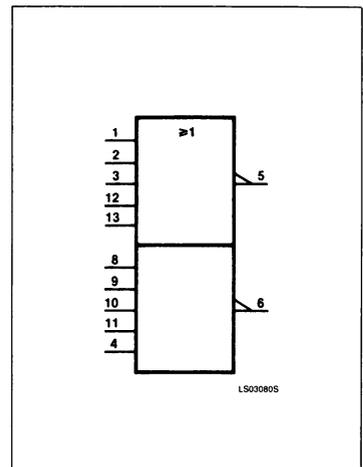
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gates

74LS260, S260

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	HIGH-level output current			-400			-1000	μA
I _{OL}	LOW-level output current			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS260			74S260			UNIT			
		Min	Typ ²	Max	Min	Typ ²	Max				
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX			2.7			2.7		V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN		I _{OL} = MAX				0.5		0.5	V
				I _{OL} = 4mA (74LS)				0.4			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}						-1.5		-1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX		V _I = 5.5V						1.0	mA
				V _I = 7.0V				0.1			mA
I _{IH}	HIGH-level Input current	V _{CC} = MAX		V _I = 2.7V				20		50	μA
I _{IL}	LOW-level input current	V _{CC} = MAX		V _I = 0.4V				-0.4			mA
				V _I = 0.5V						-2	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX			-15		-100	-40		-100	mA
I _{CC}	Supply current (total)	V _{CC} = MAX		I _{CCH} Outputs HIGH				4	17	29	mA
				I _{CCL} Outputs LOW				5.5	26	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

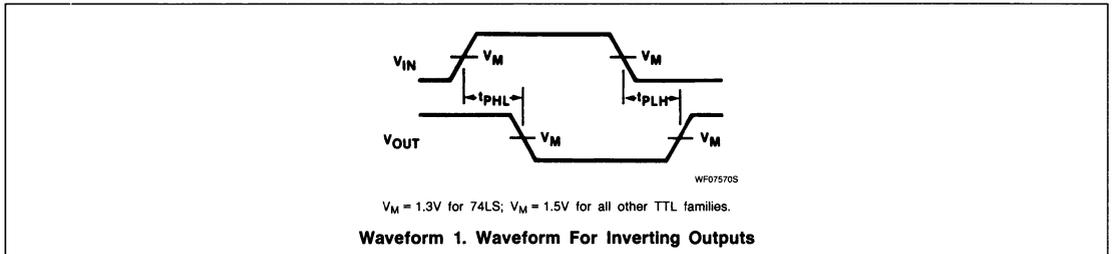
Gates

74LS260, S260

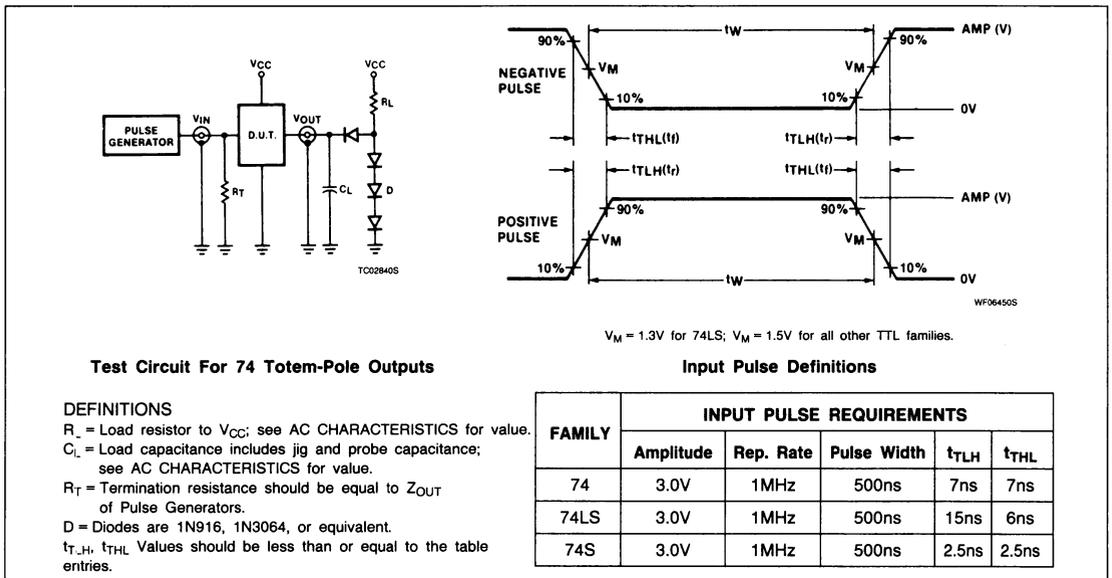
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		12 12		5.5 6.0	ns

AC WAVEFORM



TEST CIRCUITS AND WAVEFORMS



74LS266 Gate

Quad 2-Input Exclusive-NOR Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS266	18ns	8mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS266N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

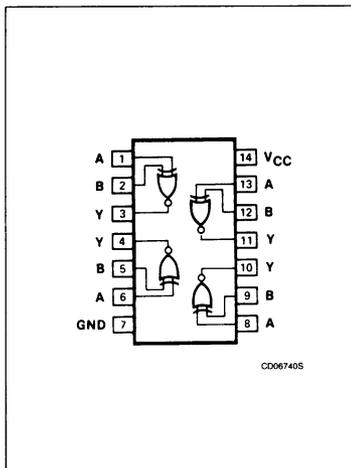
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
A, B	Inputs	2LSul
Y	Output	10LSul

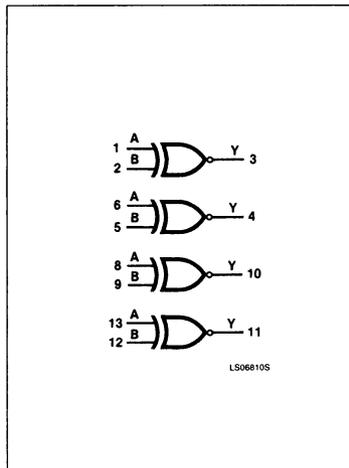
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{OL} .

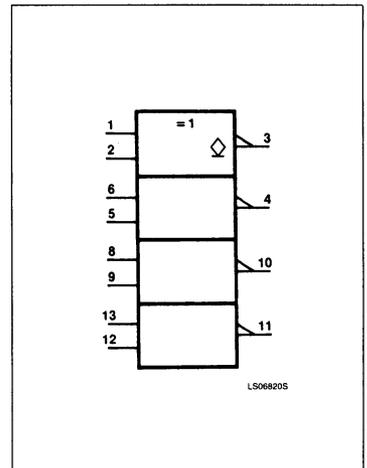
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74LS266

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	HIGH-level output voltage			5.5	V
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		74LS266			UNIT
				Min	Typ ²	Max	
I_{OH}	HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5V$				100	μA
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.35	0.5	V
			$I_{OL} = 4mA$		0.25	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$				0.2	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$				40	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4V$				-0.8	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$			8	13	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with one input of each gate at 4.5V, the other inputs grounded and the outputs open.

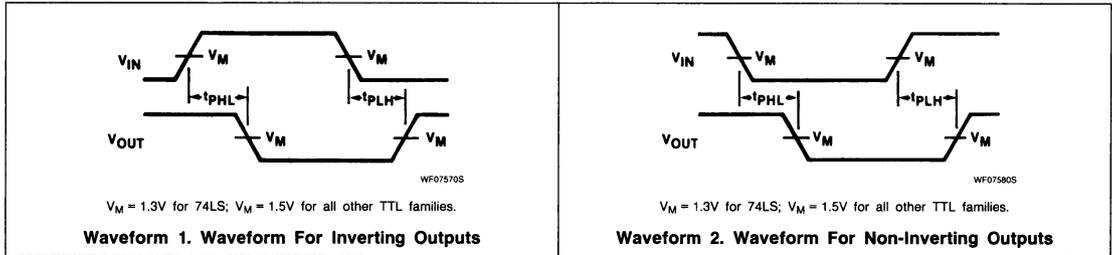
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		74LS		UNIT
				$C_L = 15pF, R_L = 2k\Omega$		
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 1, other input LOW			30 30	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 2, other input HIGH			30 30	ns

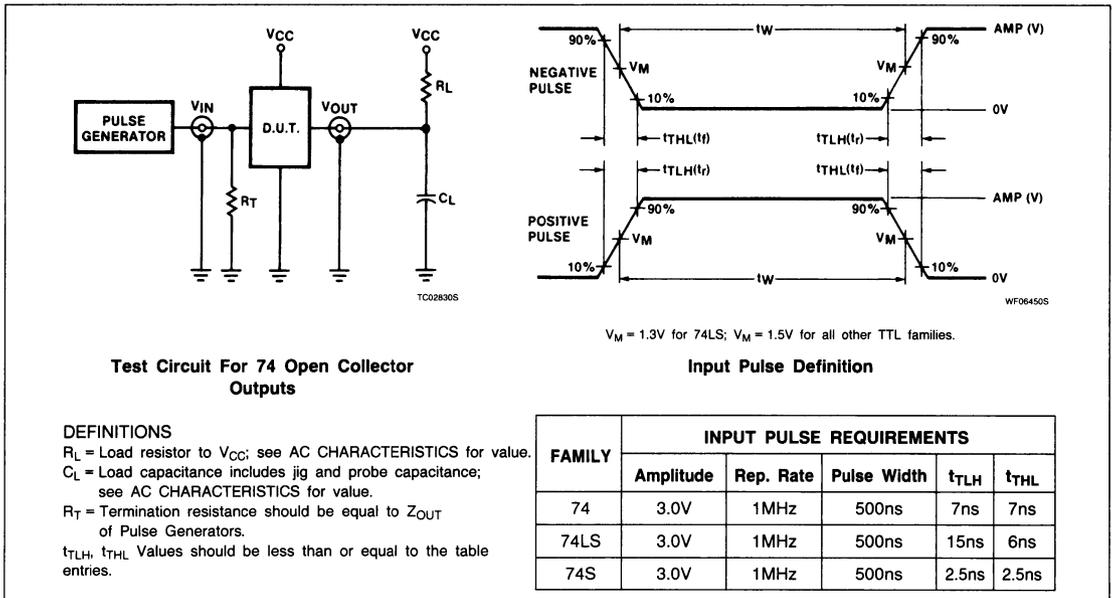
Gate

74LS266

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74LS273, S273 Flip-Flops

Octal D Flip-Flops
Product Specification

Logic Products

FEATURES

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- High speed Schottky version available
- Buffered common clock
- Buffered, asynchronous Master Reset
- Slim 20-pin plastic and ceramic DIP packages
- See '377 for Clock Enable version
- See '373 for transparent latch version
- See '374 for 3-state version

DESCRIPTION

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition,

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS273	40MHz	17mA
74S273	95MHz	109mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S273N, N74LS273N
Plastic SOL-20	N74LS273D, N74S273D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE:

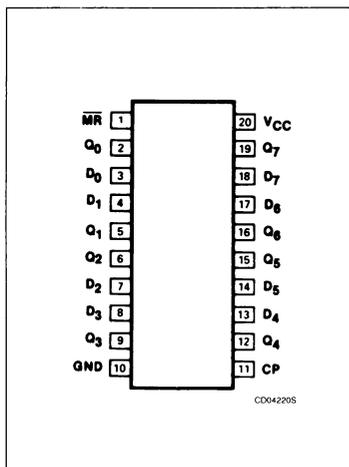
A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

tion, is transferred to the corresponding flip-flop's Q output.

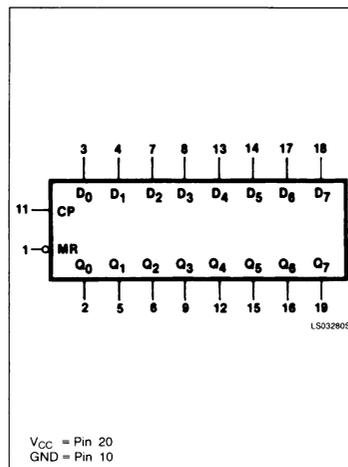
All outputs will be forced LOW independently of Clock or Data inputs by a LOW

voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

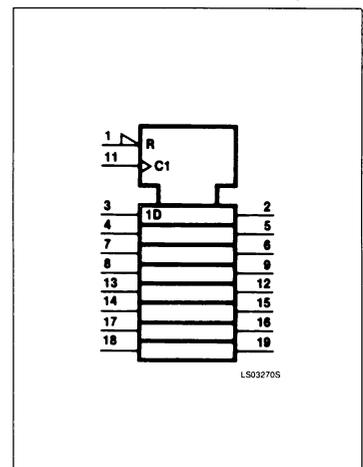
PIN CONFIGURATION



LOGIC SYMBOL



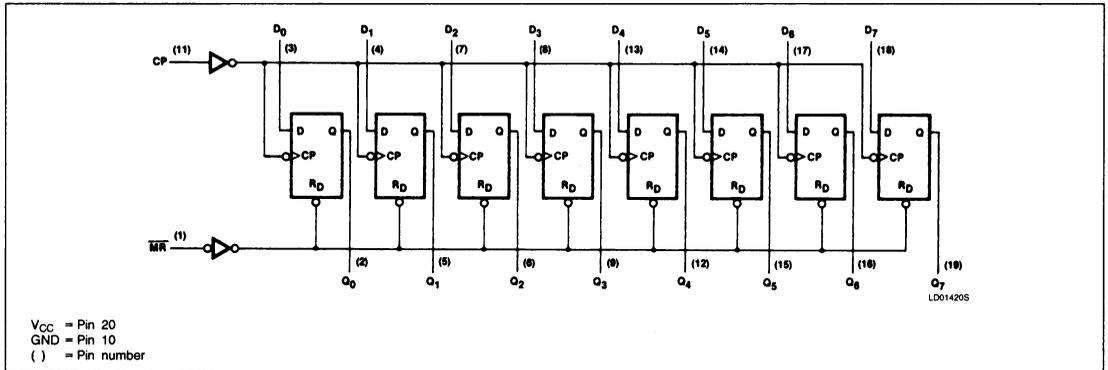
LOGIC SYMBOL (IEEE/IEC)



Flip-Flops

74LS273, S273

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	\overline{MR}	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8	V
I_{IK} Input clamp current			-18			-18	mA
I_{OH} HIGH-level output current			-400			-1000	μA
I_{OL} LOW-level output current			8			20	mA
T_A Operating free-air temperature	0		70	0		70	°C

Flip-Flops

74LS273, S273

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74LS273			74S273			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		2.7			V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5		0.5	V
			I _{OL} = 4mA (74LS)		0.25	0.4			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA
			V _I = 7.0V			0.1			mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20			50	μA
I _{IL}	LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-0.4			mA
			V _I = 0.5V					-2.0	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-20		-100	-40		-100	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX		17	27		109	150	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} after a momentary ground, then 4.5V is applied to clock with all outputs open and 4.5V applied to all Data inputs and the Master Reset input.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS		74S		UNIT
			C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
			Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t _{PLH}	Propagation delay	Waveform 1		27		15	ns
t _{PHL}	Clock to output			27		15	
t _{PHL}	Propagation delay, MR to output	Waveform 2		27		15	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

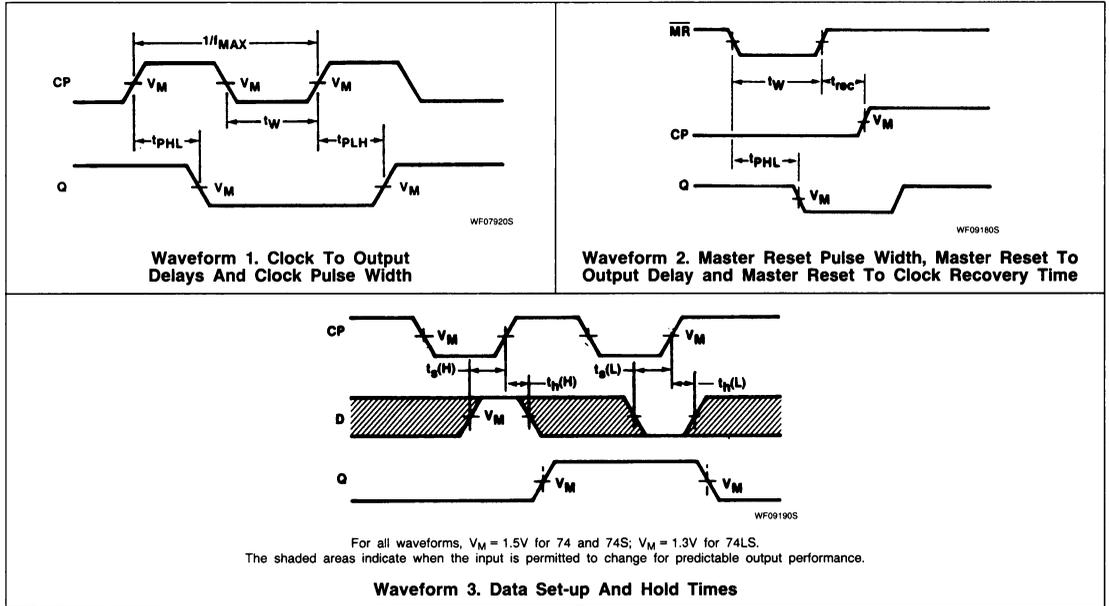
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0v

PARAMETER		TEST CONDITIONS	74LS		74S		UNIT
			Min	Max	Min	Max	
t _{w(L)}	Clock pulse width (LOW)	Waveform 1	20		7.0		ns
t _w	Master Reset pulse width	Waveform 2	20		10		ns
t _{s(H)}	Set-up time, HIGH data to CP	Waveform 3	20		5.0		ns
t _{h(H)}	Hold time, HIGH data to CP	Waveform 3	5.0		3.0		ns
t _{s(L)}	Set-up time, LOW data to CP	Waveform 3	20		5.0		ns
t _{h(L)}	Hold time, LOW data to CP	Waveform 3	5.0		3.0		ns
t _{rec}	Recovery time, MR to CP	Waveform 2	25		5.0		ns

Flip-Flops

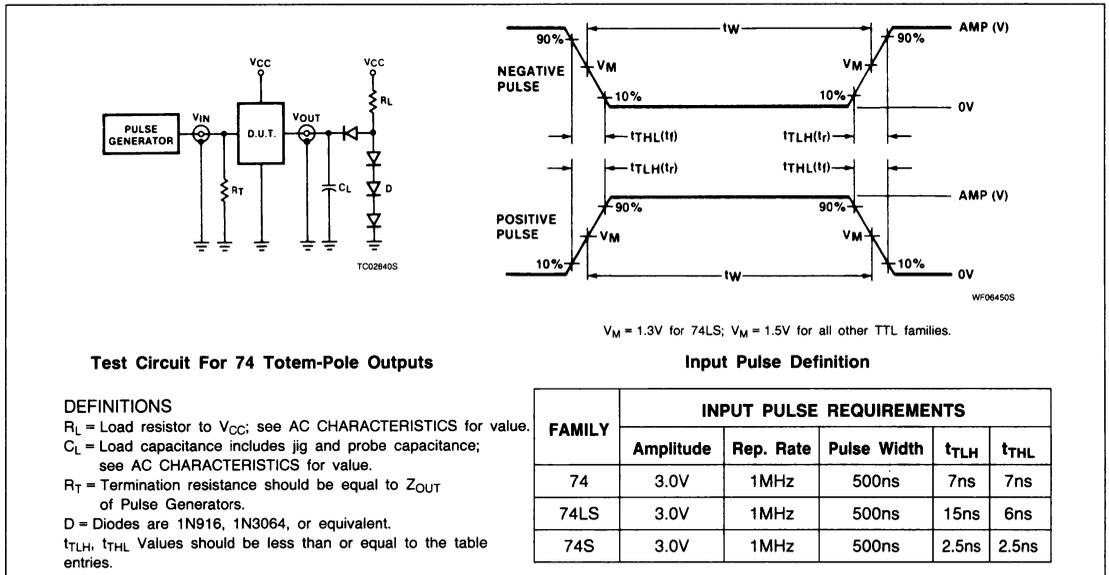
74LS273, S273

AC WAVEFORMS



5

TEST CIRCUITS AND WAVEFORMS



74279 Latch

Quad Set-Reset Latch
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74279	13ns	18mA

FUNCTION TABLE

INPUTS			OUTPUT
\bar{S}_1	\bar{S}_2	\bar{R}	Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No change

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.

h = The output is HIGH as long as \bar{S}_1 or \bar{S}_2 is LOW.
If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the truth table.

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74279N
Plastic SO-16	N74279D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

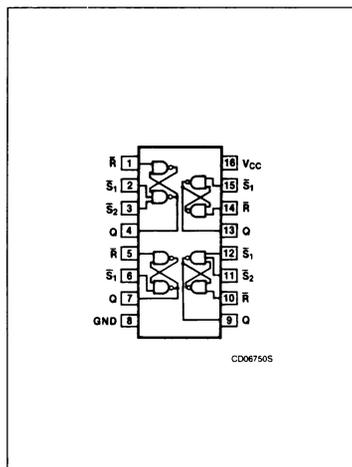
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1ul
Q	Output	10ul

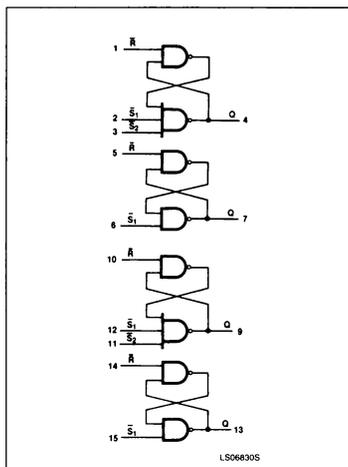
NOTE:

A 74 unit load (ul) is $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

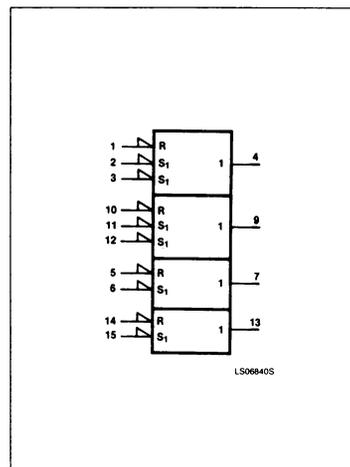
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Latch

74279

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74279			UNIT
			Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-18		-57	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX		18	30	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all \bar{R} inputs grounded, all \bar{S} inputs at 4.5V, and all outputs open.

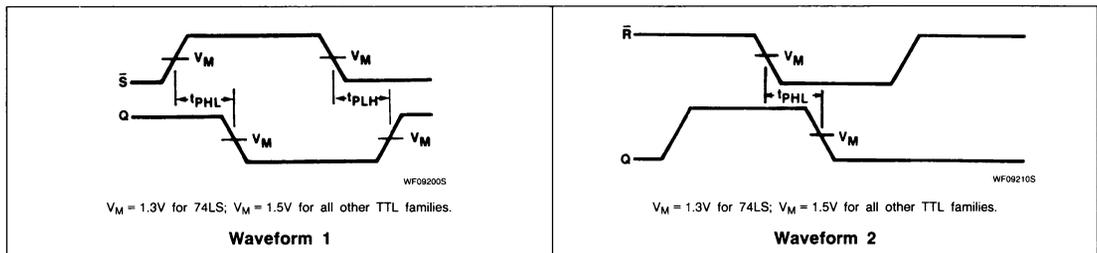
Latch

74279

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 1	22 15	ns
t_{PHL}	Propagation delay Reset to output	Waveform 2	27	ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

TC028405

WF064505

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

74S280

Parity Generator/Checker

9-Bit Odd/Even Parity Generator/Checker
Product Specification

Logic Products

FEATURES

- Buffered inputs — one normalized load
- Word-length easily expanded by cascading
- Similar pin configuration to '180 for easy system up-grading

DESCRIPTION

The '280 is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is HIGH when an even number of Data inputs ($I_0 - I_8$) are HIGH. The Odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S280	9.9ns	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S280N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
$I_0 - I_8$	Data inputs	1Sul
Σ_E, Σ_O	Parity outputs	10Sul

NOTE:

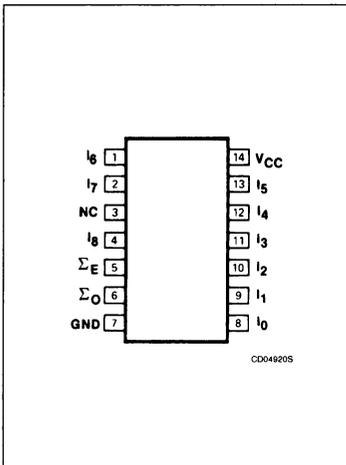
A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be

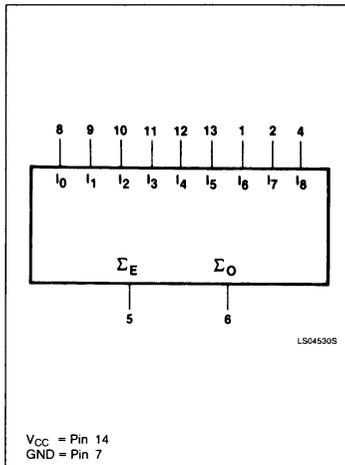
checked in less than 40ns with the 'S280.

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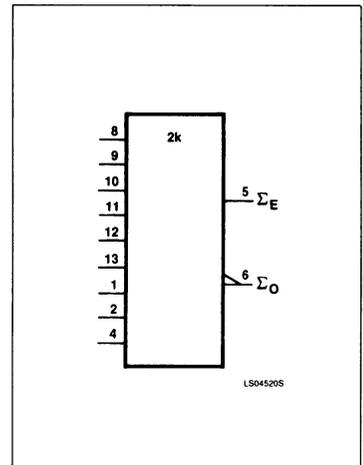
PIN CONFIGURATION



LOGIC SYMBOL



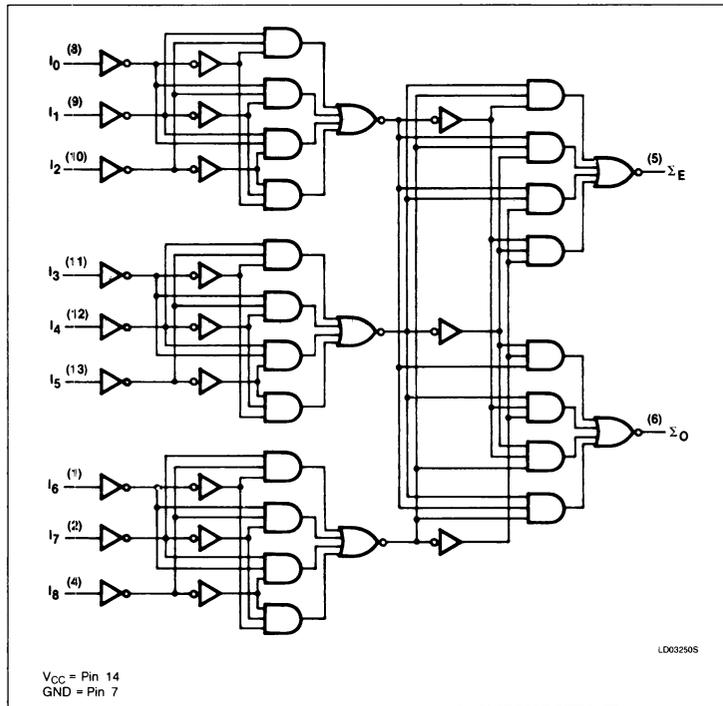
LOGIC SYMBOL (IEEE/IEC)



Parity Generator/Checker

74S280

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUTS	
	Σ_E	Σ_O
Number of HIGH data inputs ($I_0 - I_8$)		
Even	H	L
Odd	L	H

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74S	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70	°C

Parity Generator/Checker

74S280

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74S			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-1000	μ A
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	$^{\circ}$ C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74S280			UNIT
			Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}, V_{IH} = \text{MIN}$	2.7	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}, V_{IL} = \text{MAX}$			0.5	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			50	μ A
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-2	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		67	105	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all inputs grounded and all outputs open.

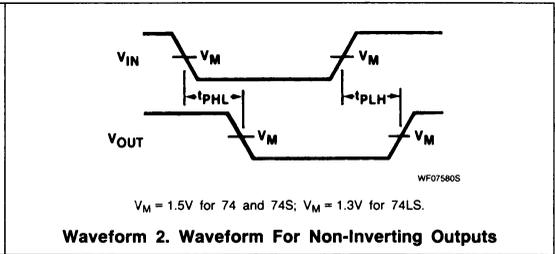
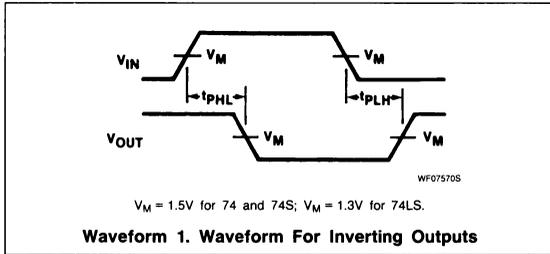
AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74S280		UNIT
			$C_L = 15\text{pF}, R_L = 280\Omega$		
			Min	Max	
t_{PLH}	Propagation delay	Waveforms 1 & 2	10	21	ns
t_{PHL}	Data to even output		11	18	
t_{PLH}	Propagation delay	Waveforms 1 & 2	9.6	21	ns
t_{PHL}	Data to odd output		9.3	18	

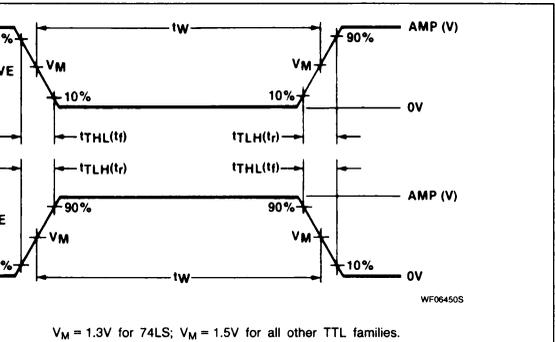
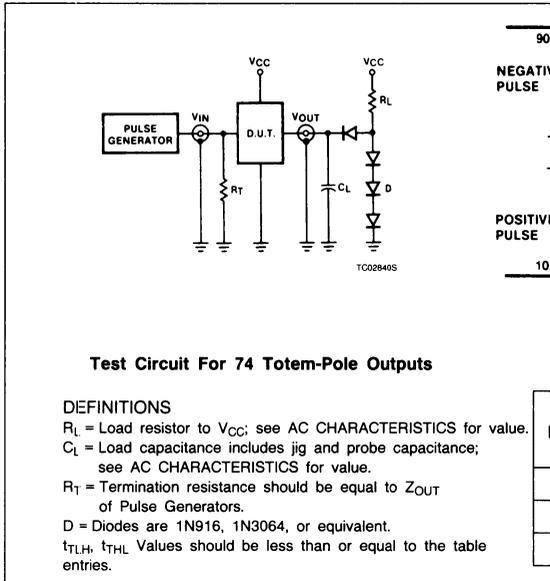
Parity Generator/Checker

74S280

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS283 Adder

4-Bit Full Adder With Fast Carry
Product Specification

Logic Products

FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal carry lookahead

DESCRIPTION

The '283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic) – see Function Table. In case of all active LOW operands the results $\Sigma_1 - \Sigma_4$ and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS283	13ns	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS283N
Plastic SO-16	N74LS283D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
A, B	Inputs	2LSul
C_{IN}	Input	1LSul
All	Outputs	10LSul

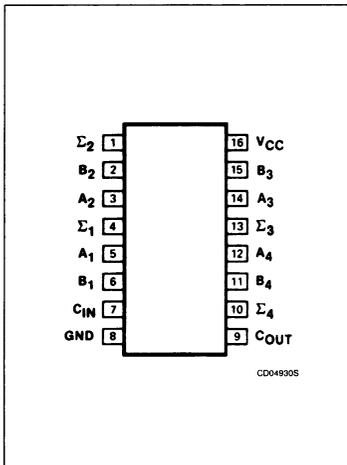
NOTE:

A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

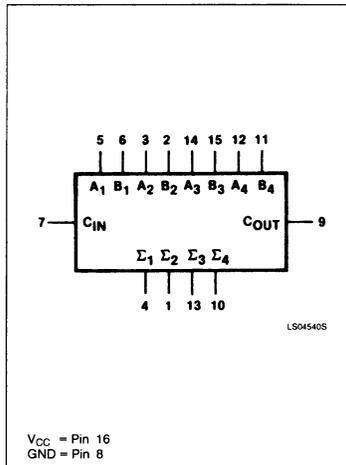
intended. Interchanging inputs of equal weight does not affect the operation,

thus C_{IN} , A_1 , B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

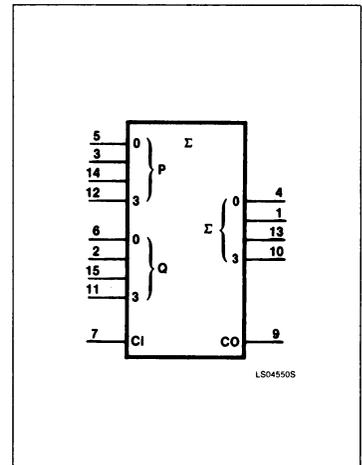
PIN CONFIGURATION



LOGIC SYMBOL



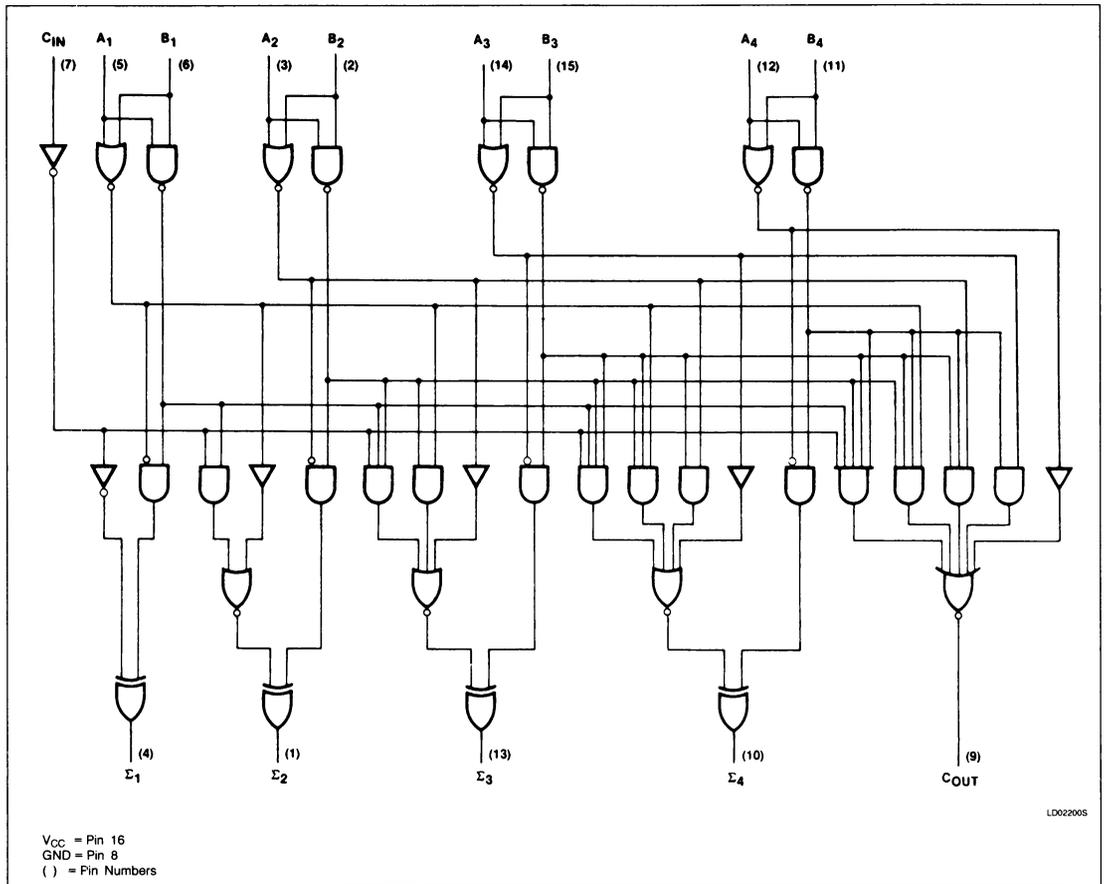
LOGIC SYMBOL (IEEE/IEC)



Adder

74LS283

LOGIC DIAGRAM



FUNCTION TABLE

PINS	C _{IN}	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C _{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Example:
 1001
 1010

 10011
 (10 + 9 = 19)
 (carry + 5 + 6 = 12)

H = HIGH voltage level
 L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

Adder

74LS283

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μ A
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	$^{\circ}$ C

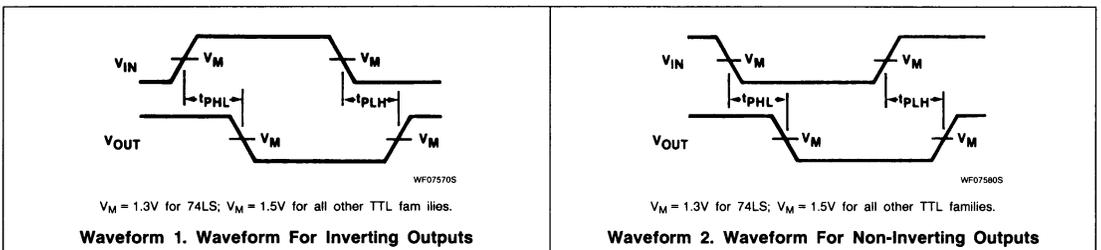
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS283			UNIT
		Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$			V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$			V
		$I_{OL} = \text{MAX}$			V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$			V
		$I_{OL} = 4\text{mA (74LS)}$			V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			mA
		A, B inputs			mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			μ A
		C_{IN} input			μ A
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			mA
		A, B inputs			mA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			mA
		C_{IN} input			mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$			mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$			mA
		Condition 1			mA
		Condition 2			mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$			mA
		Condition 3			mA
		Condition 2			mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} should be measured with all outputs open and the following conditions:
 Condition 1: All inputs grounded.
 Condition 2: All B inputs LOW, other inputs at 4.5V.
 Condition 3: All inputs at 4.5V.

AC WAVEFORMS



Adder

74LS283

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74LS		UNIT
			$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_1	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_2	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_3	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_4	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL}	Propagation delay A_1 or BV_1 to Σ_1	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2		17 22	ns
t_{PLH} t_{PHL}	Propagation delay A_1 or B_1 to C_{OUT}	Waveforms 1 & 2		17 17	ns

TEST CIRCUITS AND WAVEFORMS

TC02840S

WF06450S

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS290

Counter

Decade Counter
Product Specification

Logic Products

DESCRIPTION

The '290 is a 4-bit, ripple type decade counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the Clock and MR inputs, setting the outputs to nine (HLLH).

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS290	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS290N
Plastic SO-14	N74LS290D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

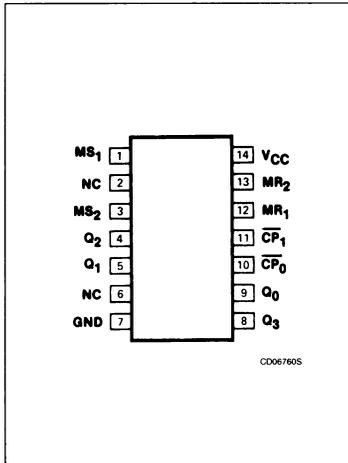
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
MR, MS	Inputs	1LSul
\overline{CP}_0	Input	4LSul
\overline{CP}_1	Input	8LSul
All	Outputs	10LSul

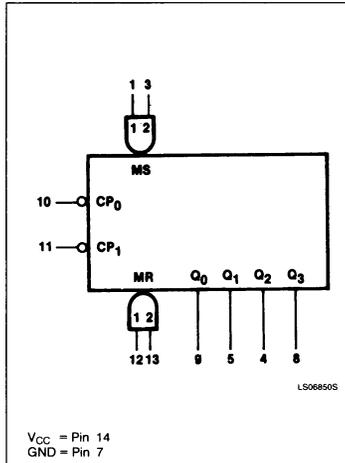
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

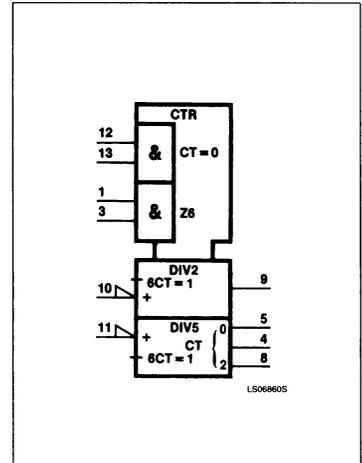
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Counter

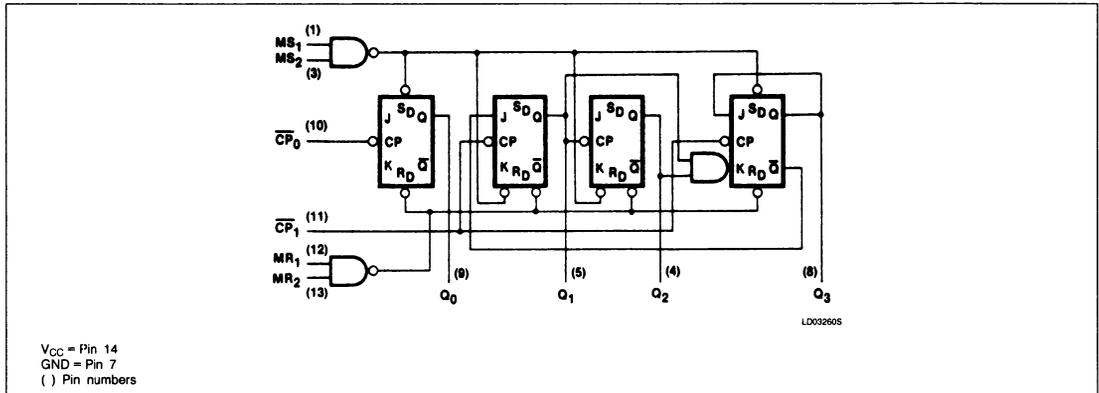
74LS290

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count, producing a

BCD count sequence. In a symmetrical binary divide-by-ten counter the Q_3 output must be connected externally to the \overline{CP}_0 input. The input count is then applied to the \overline{CP}_1 input and a divide-by-ten square wave is obtained at output Q_0 . To operate as a divide-by-two and a divide-by-five counter, no exter-

nal interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain divide-by-five operation at the Q_3 output.

LOGIC DIAGRAM



BCD COUNT SEQUENCE — FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE:
 Output Q_0 connected to input \overline{CP}_1 .

MODE SELECTION — FUNCTION TABLE

RESET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X			Count	
X	L	X	L			Count	
L	X	X	L			Count	
X	L	L	X			Count	

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

Counter

74LS290

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

NOTE: V_{IN} limited to +5.5V on CP_0 and CP_1 inputs only.**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μ A
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS290			UNIT		
		Min	Typ ²	Max			
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$		2.7	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$			0.35	0.5	V
		$I_{OL} = \text{MAX}$			0.25	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 7.0V$	MR, MS inputs		0.1	mA
			$V_I = 5.5V$	\overline{CP}_0 input		0.2	mA
				\overline{CP}_1 input		0.4	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$	MR, MS inputs		20	μ A	
			\overline{CP}_0 input ⁵		40	μ A	
			\overline{CP}_1 input ⁵		80	μ A	
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4V$	MR, MS inputs		-0.4	mA	
			\overline{CP}_0 input		-2.4	mA	
			\overline{CP}_1 input		-3.2	mA	
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-20		-100	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$			9	15	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.3. I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.5. The maximum limit for the 54LS290 is only 80 μ A for \overline{CP}_0 and 160 μ A for \overline{CP}_1 inputs.

Counter

74LS290

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
f_{MAX} $\overline{\text{CP}}_0$ input count frequency	Waveform 1	32		MHz
f_{MAX} $\overline{\text{CP}}_1$ input count frequency	Waveform 1	16		MHz
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_0$ input to Q_0 output	Waveform 1		16 18	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ input to Q_1 output	Waveform 1		16 21	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ input to Q_2 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ input to Q_3 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_0$ input to Q_3 output	Waveform 1		48 50	ns
t_{PHL} MR input to any output	Waveform 2		40	ns
t_{PLH} MS input to Q_0 and Q_3 outputs	Waveform 3		30	ns
t_{PHL} MS input to Q_1 and Q_2 outputs	Waveform 2		40	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

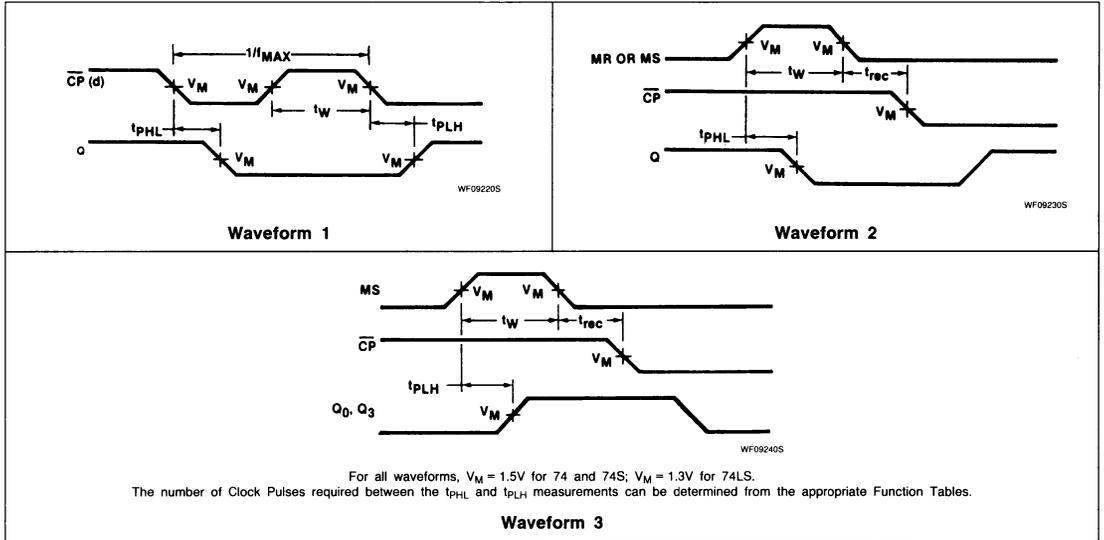
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W $\overline{\text{CP}}_0$ pulse width	Waveform 1	15		ns
t_W $\overline{\text{CP}}_1$ pulse width	Waveform 1	30		ns
t_W MR pulse width	Waveform 2	15		ns
t_{rec} Recovery time, MR to $\overline{\text{CP}}$	Waveform 2	25		ns
t_{rec} Recovery time, MS to $\overline{\text{CP}}$	Waveforms 2 and 3	25		ns

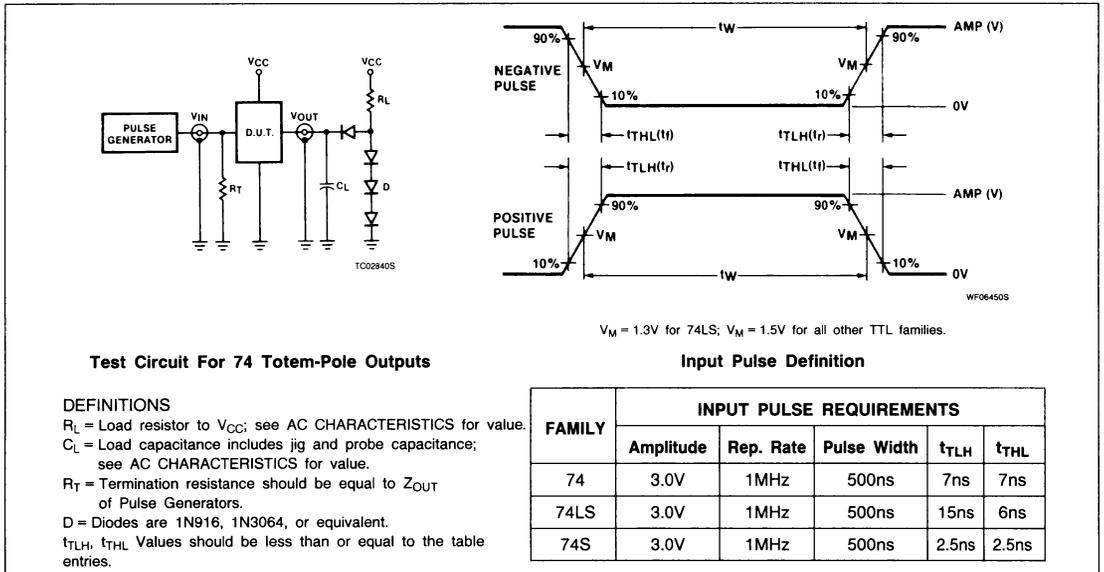
Counter

74LS290

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74LS293 Counter

4-Bit Binary Ripple Counter
Product Specification

Logic Products

DESCRIPTION

The '293 is a 4-bit ripple type binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR_1 MR_2) is provided which overrides both clocks and resets (clears) all the flip-flops.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS293	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS293N
Plastic SO-14	N74LS293D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

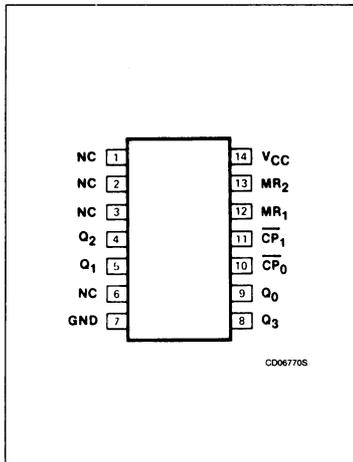
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
MR	Inputs	1LSul
\overline{CP}_0	Input	6LSul
\overline{CP}_1	Input	4LSul
All	Outputs	10LSul

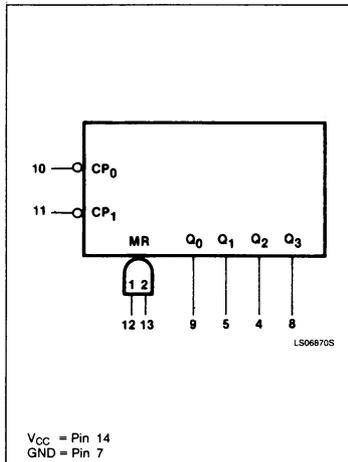
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

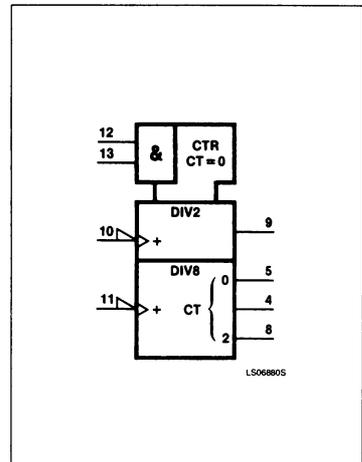
PIN CONFIGURATION



LOGIC SYMBOL



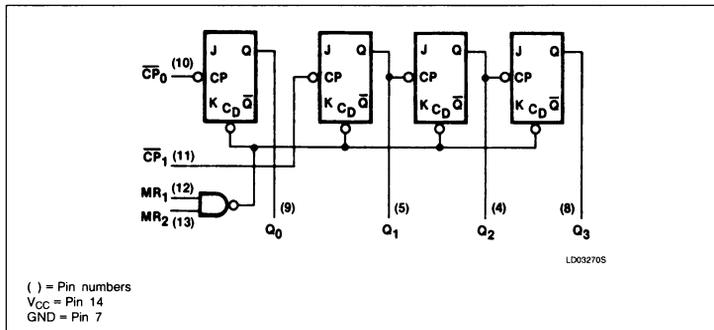
LOGIC SYMBOL (IEEE/IEC)



Counter

74LS293

LOGIC DIAGRAM



Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous divisions of 2, 4, 8 and 16 are preformed at the Q_0 , Q_1 , Q_2 and Q_3 outputs as shown in the function table. As a 3-bit counter the input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1 , Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE:
 Output Q_0 connected to input \overline{CP}_1 .

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H			Count	
H	L			Count	
L	L			Count	

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

Counter

74LS293

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

NOTE: V_{IN} limited to 5.5V on \overline{CP}_0 and \overline{CP}_1 inputs.**RECOMMENDED OPERATING CONDITIONS**

PARAMETER		74			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μ A
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS293			UNIT
		Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.7	3.4		V
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$			0.35	V
				0.25	V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$	$V_I = 7.0\text{V}$	MR inputs	0.1	mA
		$V_I = 5.5\text{V}$	\overline{CP} inputs	0.2	mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}, V_I = 2.7\text{V}$		MR inputs	20	μ A
			\overline{CP} inputs ⁵	40	μ A
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}, V_I = 0.4\text{V}$		MR inputs	-0.4	mA
			\overline{CP}_0 input	-2.4	mA
			\overline{CP}_1 input	-1.6	mA
I_{OS}	Short-circuit output current ³ $V_{CC} = \text{MAX}$	-20		-100	mA
I_{CC}	Supply current ⁴ (total) $V_{CC} = \text{MAX}$		9	15	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Clock inputs grounded, all outputs open, both MR inputs grounded following momentary connection to 4.5V.
- The maximum limit for the 54LS293 is 80 μ A for \overline{CP}_0 and \overline{CP}_1 inputs.

Counter

74LS293

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
f_{MAX} $\overline{\text{CP}}_0$ input count frequency	Waveform 1	32		MHz
f_{MAX} $\overline{\text{CP}}_1$ input count frequency	Waveform 1	16		MHz
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_0$ input to Q_0 output	Waveform 1		16 18	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ input to Q_1 output	Waveform 1		16 21	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ input to Q_2 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ input to Q_3 output	Waveform 1		51 51	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_0$ input to Q_3 output	Waveform 1		70 70	ns
t_{PHL} MR input to any output	Waveform 2		40	ns

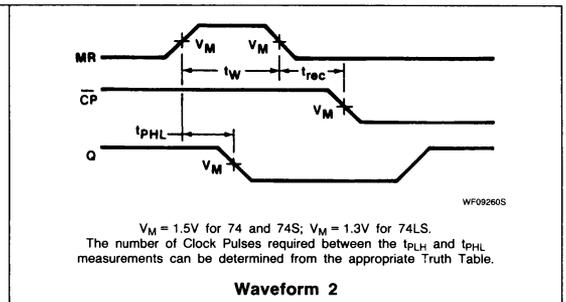
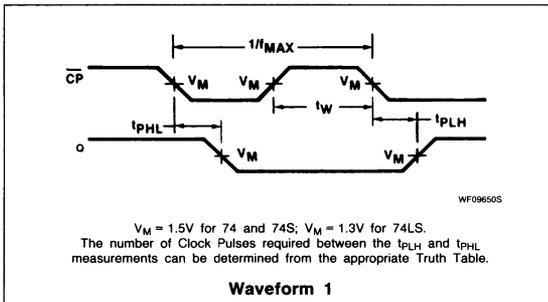
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W $\overline{\text{CP}}_0$ pulse width	Waveform 1	15		ns
t_W $\overline{\text{CP}}_1$ pulse width	Waveform 1	30		ns
t_W MR pulse width	Waveform 2	15		ns
t_{rec} Recovery time, MR to $\overline{\text{CP}}$	Waveform 2	25		ns

AC WAVEFORMS

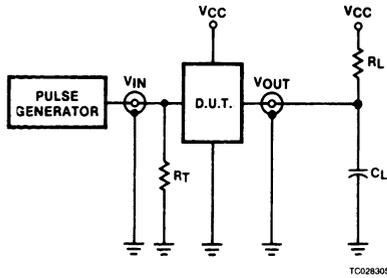


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Counter

74LS293

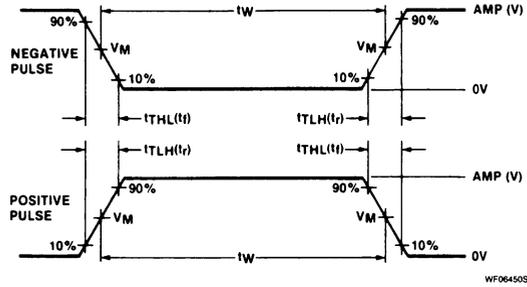
TEST CIRCUITS AND WAVEFORMS



**Test Circuit For 74
Open Collector Outputs**

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS295B Shift Register

4-Bit Shift Register With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 4-bit parallel load shift register
- Independent 3-State buffer outputs
- See '395 for serial expansion and Master Reset version

DESCRIPTION

The '295B is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data outputs ($D_0 - D_3$) into the register synchronous with the HIGH-to-LOW transition of the Clock input (CP). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative transition of the Clock. The PE and Data inputs are fully edge triggered and must be stable one set-up time

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS295B	45MHz	17mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS295BN

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE:

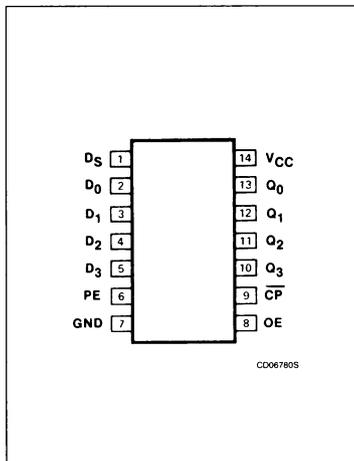
A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

prior to the HIGH-to-LOW transition of the Clock.

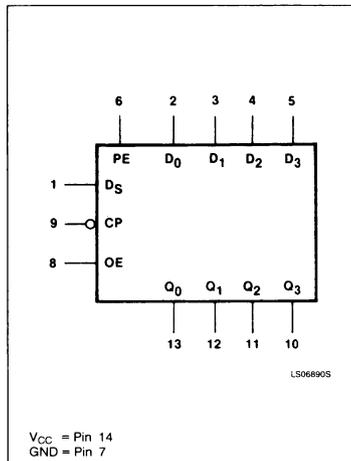
The 3-State output buffers are designed to drive heavily loaded 3-state buses or large capacitive loads. The active HIGH Output Enable (OE) controls all four 3-

state buffers independent of the register operation. When OE is HIGH the data in the register appears at the outputs. When OE is LOW the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

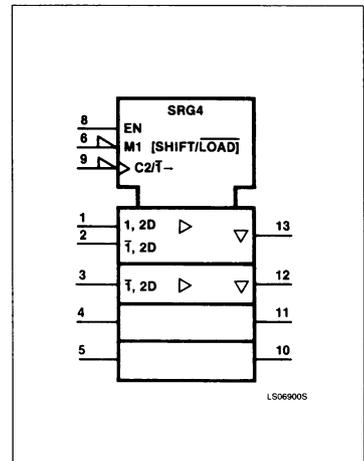
PIN CONFIGURATION



LOGIC SYMBOL



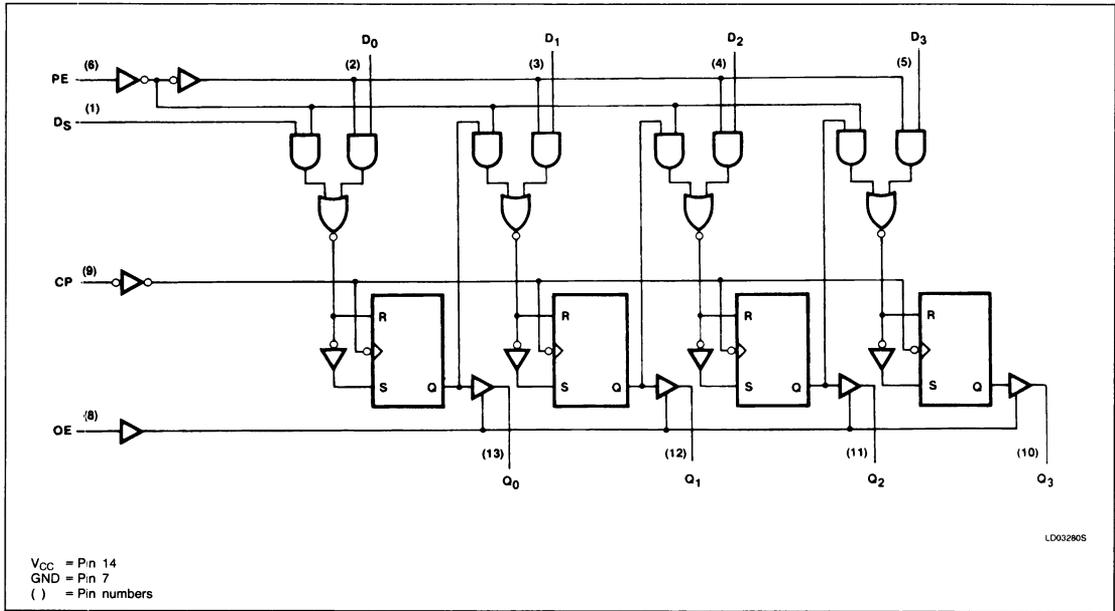
LOGIC SYMBOL (IEEE/IEC)



Shift Register

74LS295B

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS				REGISTER OUTPUTS			
	\overline{CP}	PE	D _S	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Shift right	↓	l	l	X	L	q ₀	q ₁	q ₂
	↓	l	h	X	H	q ₀	q ₁	q ₂
Parallel load	↓	h	X	l	L	L	L	L
	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q _n (Register)	Q ₀ , Q ₁ , Q ₂ , Q ₃
Read	H	L	L
	H	H	H
Disabled	L	X	(Z)

- H = HIGH voltage level.
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition.
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition.
- q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW clock transition.
- X = Don't care.
- (Z) = HIGH impedance "off" state.
- ↓ = HIGH-to-LOW clock transition.

Shift Register

74LS295B

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-2.6	mA
I _{OL}	LOW-level output current			24	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS295B			UNIT		
		Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.1		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5	V
			I _{OL} = 12mA (74LS)		0.25	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IL} = MAX, V _O = 2.7V				20	μA
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V				-20	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				0.1	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-0.4	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-30		-130	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		16	29	mA
			Condition 2		17	33	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the outputs open, D_S and PE at 4.5V, and the Data inputs grounded under the following conditions: *Condition 1* : OE at 4.5V and a momentary 3V, then ground, applied to the Clock input.
Condition 2 : OE and Clock input grounded.

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Shift Register

74LS295B

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT	
		$C_L = 45\text{pF}$, $R_L = 667\Omega$			
		Min	Max		
f_{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t_{PHL} t_{PLH}	Propagation delay Clock to output	Waveform 1		23 30	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		26	ns
t_{PZL}	Enable time to LOW level	Waveform 3		30	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5\text{pF}$		20	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5\text{pF}$		20	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT	
		Min	Max		
t_W	Clock pulse width	Waveform 1	16		ns
t_S	Set-up time, data to clock	Waveform 4	20		ns
t_H	Hold time, data to clock	Waveform 4	20		ns
t_S	Set-up time, PE to clock	Waveform 4	20		ns
t_H	Hold time, PE to clock	Waveform 4	10		ns

AC WAVEFORMS

WF09270S

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.

Waveform 1. Clock To Output Delays And Clock Pulse Width

WF09280S

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.

Waveform 2. 3-State Enable Time To High Level And Disable Time From High Level

WF09290S

$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.

Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

WF09300S

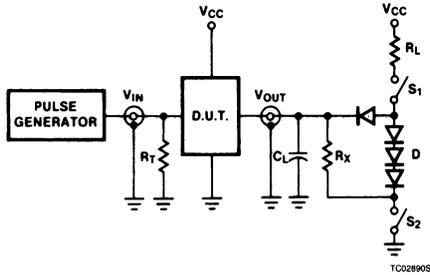
$V_M = 1.5\text{V}$ for 74 and 74S; $V_M = 1.3\text{V}$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4. Parallel Enable And Data Set-up And Hold Times

Shift Register

74LS295B

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t _{pZH}	Open	Closed
t _{pZL}	Closed	Open
t _{pHZ}	Closed	Closed
t _{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

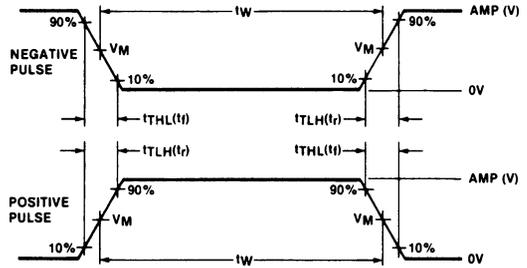
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74298, LS298 Registers

Quad 2-Port Register Product Specification

Logic Products

FEATURES

- Fully synchronous operation
- Select from two data sources
- Buffered, negative edge triggered clock

DESCRIPTION

This device is a high-speed Quad 2-Port Register. It selects 4 bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one set-up time prior to the HIGH-to-LOW transition of the clock for predictable operation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74298	19ns	39mA
74LS298	19ns	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74298N, N74LS298N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

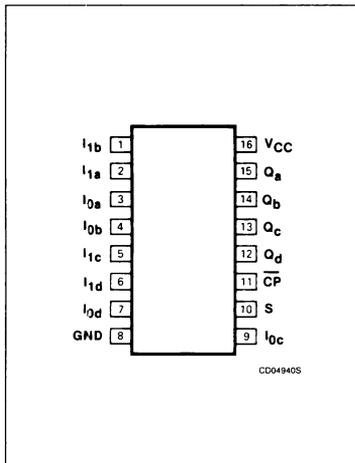
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

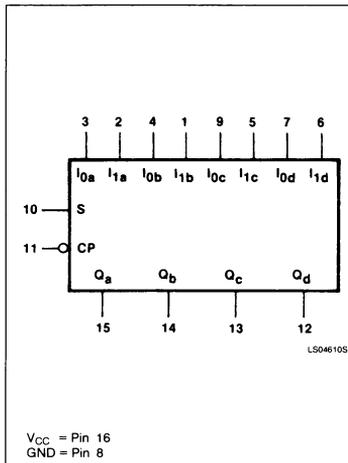
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

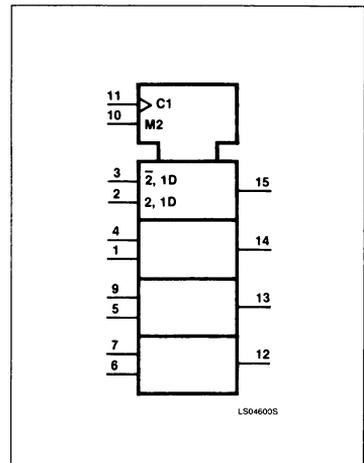
PIN CONFIGURATION



LOGIC SYMBOL



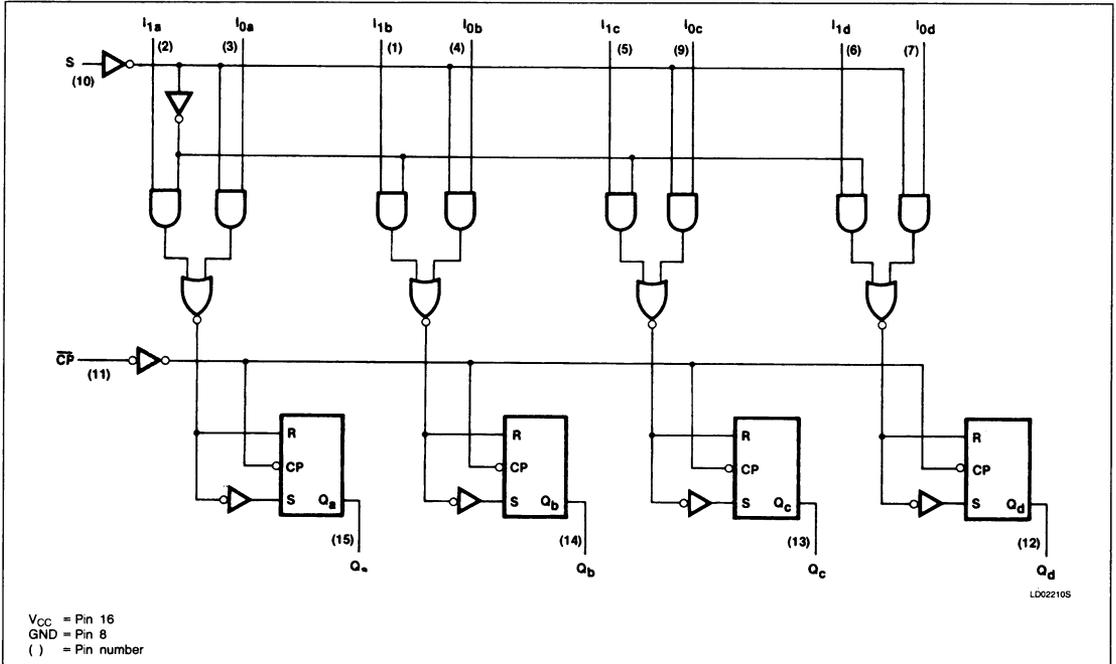
LOGIC SYMBOL (IEEE/IEC)



Registers

74298, LS298

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	\overline{CP}	S	I_0	I_1	Q_n
Load	↓	l	l	X	L
Source "0"	↓	l	h	X	H
Load	↓	h	X	l	L
Source "1"	↓	h	X	h	H

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition.
 X = Don't care
 ↓ = HIGH-to-LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70		°C

Registers

74298, LS298

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	HIGH-level output current			-800			-400	μ A
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	$^{\circ}$ C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74298			74LS298			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = \text{MAX}$	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.4	0.35	0.5		V
		$I_{OL} = 4\text{mA}$ (74LS)			0.25	0.4		V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5			-1.5	V
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$		1.0				mA
		$V_I = 7.0\text{V}$				0.1		mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$		40				μ A
		$V_I = 2.7\text{V}$				20		μ A
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$			-1.6			-0.4	mA
I_{OS}	Short-circuit output current ³ $V_{CC} = \text{MAX}$	-18		-57	-20		-100	mA
I_{CC}	Supply current ⁴ (total) $V_{CC} = \text{MAX}$		39	65		13	21	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after applying a momentary 4.5V, followed by ground to the Clock input, with all other inputs low and all outputs open.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
t_{PLH}	Propagation delay		27		27	ns
t_{PHL}	Clock to output		32		32	

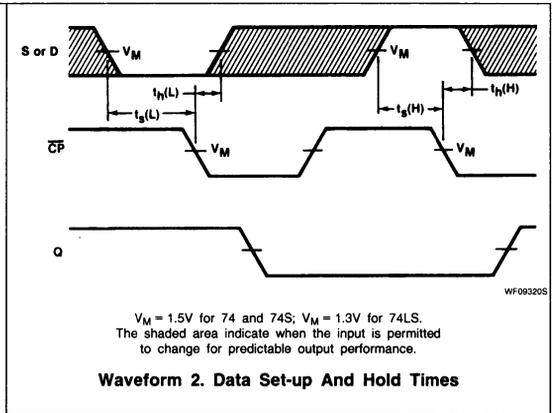
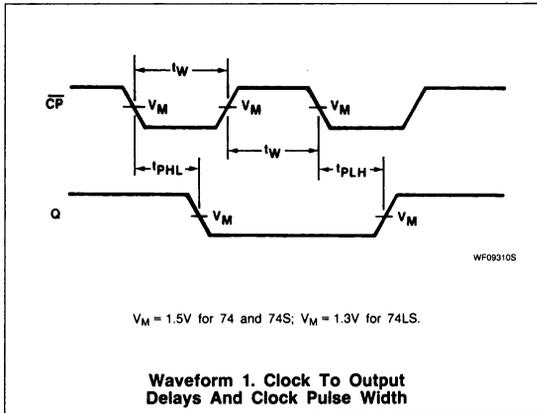
Registers

74298, LS298

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
t_W	Clock pulse width	20		20		ns
t_s	Set-up time, data to clock	15		15		ns
t_h	Hold time, data to clock	5		5		ns
t_s	Set-up time, select to clock	25		25		ns
t_h	Hold time, select to clock	0		0		ns

AC WAVEFORMS



5

TEST CIRCUITS AND WAVEFORMS

TC02840S

WF06450S

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74S350 Shifter

4-Bit Shifter With 3-State Outputs
Product Specification

Logic Products

FEATURES

- Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines
- 3-State outputs for bus organized systems
- Alternate source AM25S10

DESCRIPTION

The '350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The '350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical – with logic zeros filled in at either end of the shifting field.
2. Arithmetic – where the sign bit is extended during a shift down.
3. End around – where the data word forms a continuous loop.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S350	7ns	71mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S350N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
All	Outputs	10Sul

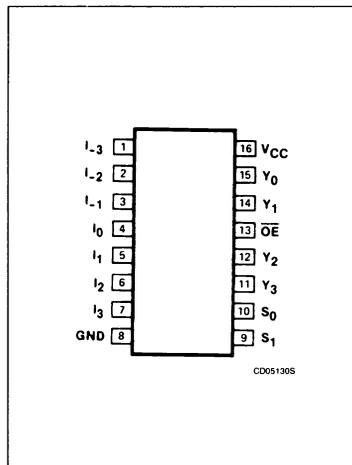
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

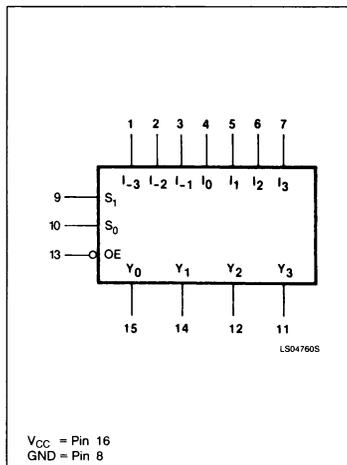
The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable (\overline{OE}) input controls the state of

the outputs. The outputs are in the HIGH impedance "off" state when \overline{OE} is HIGH, and they are active when \overline{OE} is LOW.

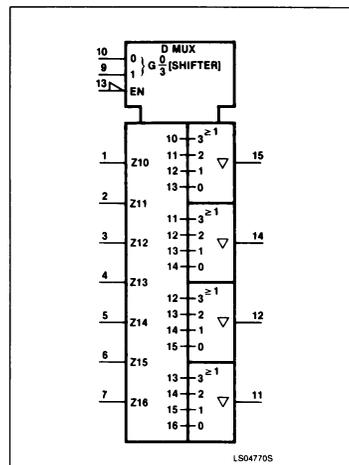
PIN CONFIGURATION



LOGIC SYMBOL



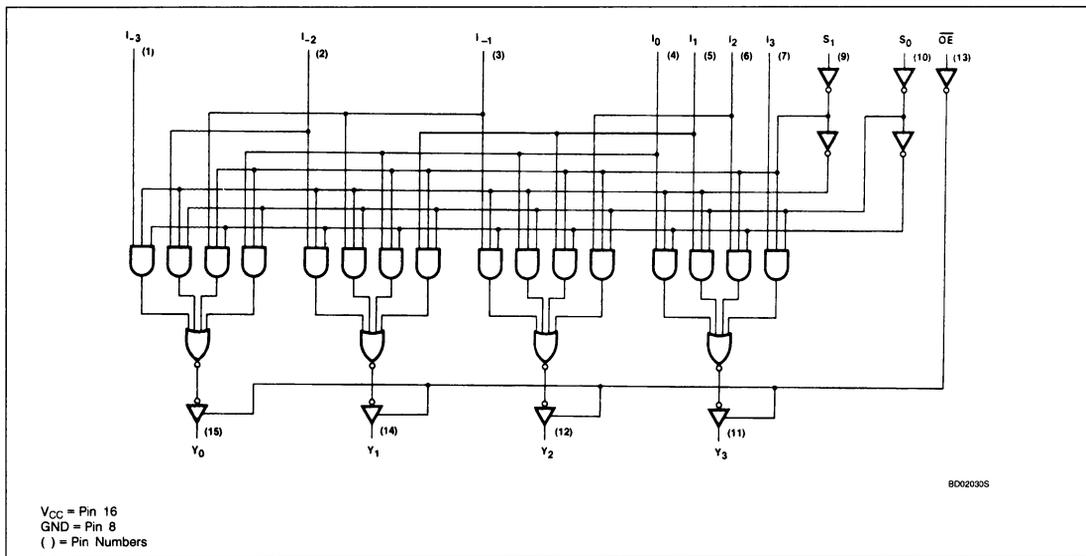
LOGIC SYMBOL (IEEE/IEC)



Shifter

74S350

LOGIC DIAGRAM



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FUNCTION TABLE

OE	S ₁	S ₀	I ₃	I ₂	I ₁	I ₀	I ₋₁	I ₋₂	I ₋₃	Y ₃	Y ₂	Y ₁	Y ₀
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D ₃	D ₂	S ₁	D ₀	X	X	X	D ₃	D ₂	D ₁	D ₀
L	L	H	H	X	D ₂	D ₁	D ₀	D ₋₁	X	X	D ₂	D ₁	D ₀
L	H	L	X	X	D ₁	D ₀	D ₋₁	D ₋₂	X	D ₁	D ₀	D ₋₁	D ₋₂
L	H	H	X	X	X	D ₀	D ₋₁	D ₋₂	D ₋₃	D ₀	D ₋₁	D ₋₂	D ₋₃

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance (off) state
 D_n = HIGH or LOW state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_0 + S_0 \cdot \bar{S}_1 \cdot I_{-1} + \bar{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$

$$Y_1 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_1 + S_0 \cdot \bar{S}_1 \cdot I_0 + \bar{S}_0 \cdot S_1 \cdot I_{-1} + S_0 \cdot S_1 \cdot I_{-2}$$

$$Y_2 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_2 + S_0 \cdot \bar{S}_1 \cdot I_1 + \bar{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1}$$

$$Y_3 = \bar{S}_0 \cdot \bar{S}_1 \cdot I_3 + S_0 \cdot \bar{S}_1 \cdot I_2 + \bar{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

Shifter

74S350

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74S			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IH}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-6.5	mA
I _{OL}	LOW-level output current			20	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S350			UNIT
		Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX			V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			V
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V			μA
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.5V			μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.5V			mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX			mA
I _{CC}	Supply current (total)	V _{CC} = MAX, V _{IN} = 0V			mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

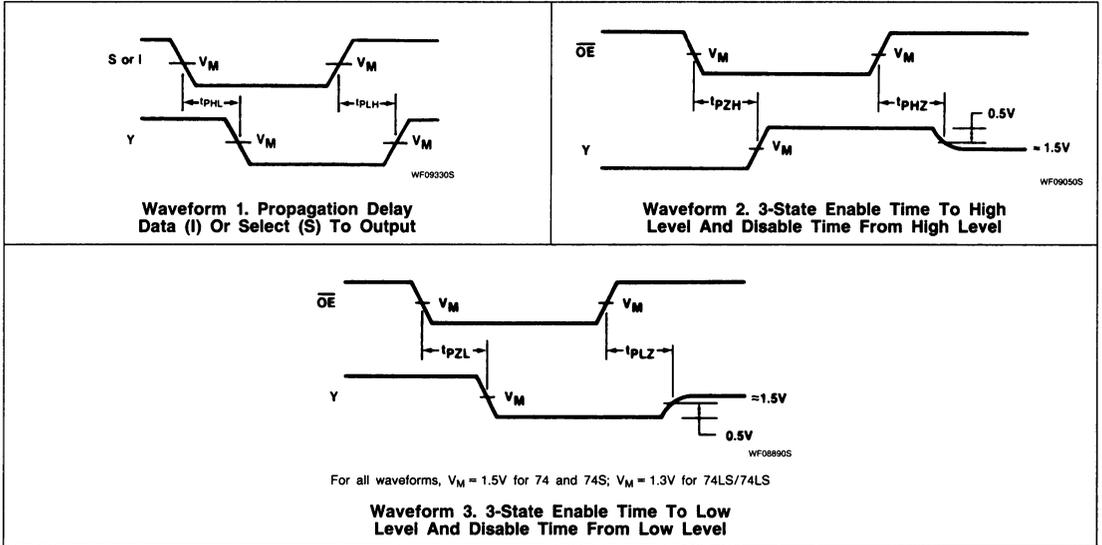
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 1	10.5 10.5	ns
t _{PLH} t _{PHL}	Propagation delay Select to output	Waveform 1	17 20	ns
t _{PZH}	Enable time to HIGH level	Waveform 2	19.5	ns
t _{PZL}	Enable time to LOW level	Waveform 3	21	ns
t _{PHZ}	Disable time from HIGH level	Waveform 2, C _L = 5pF	8.0	ns
t _{PLZ}	Disable time from LOW level	Waveform 3, C _L = 5pF	15	ns

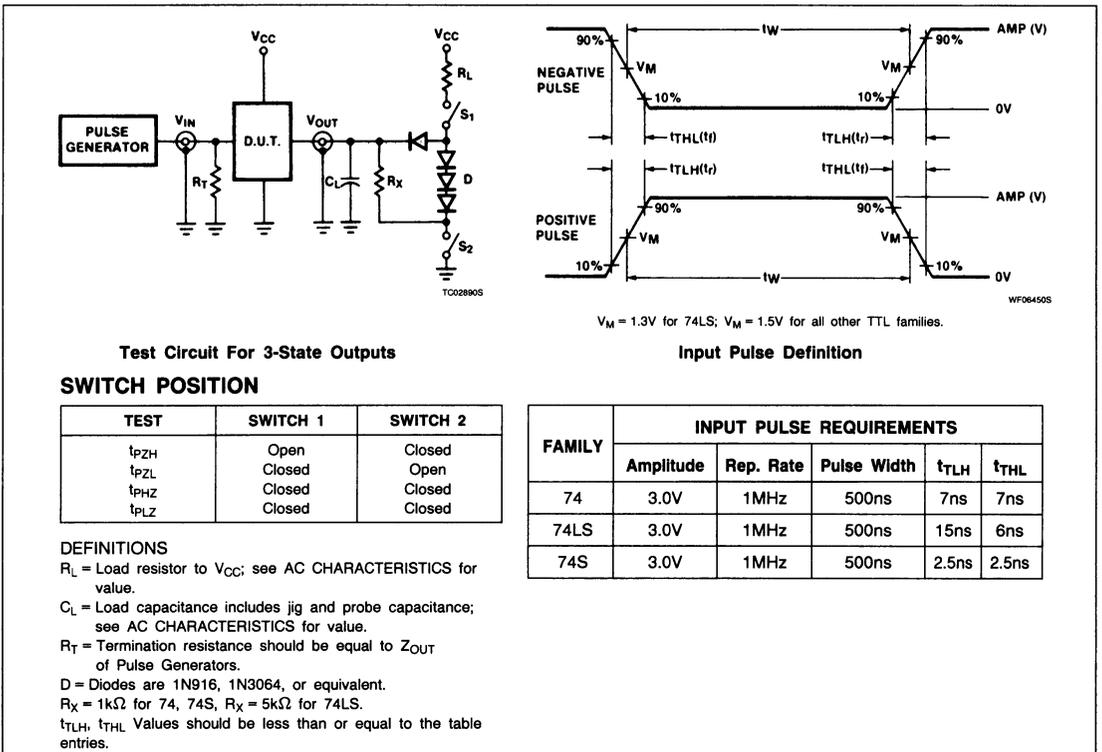
Shifter

74S350

AC WAVEFORMS



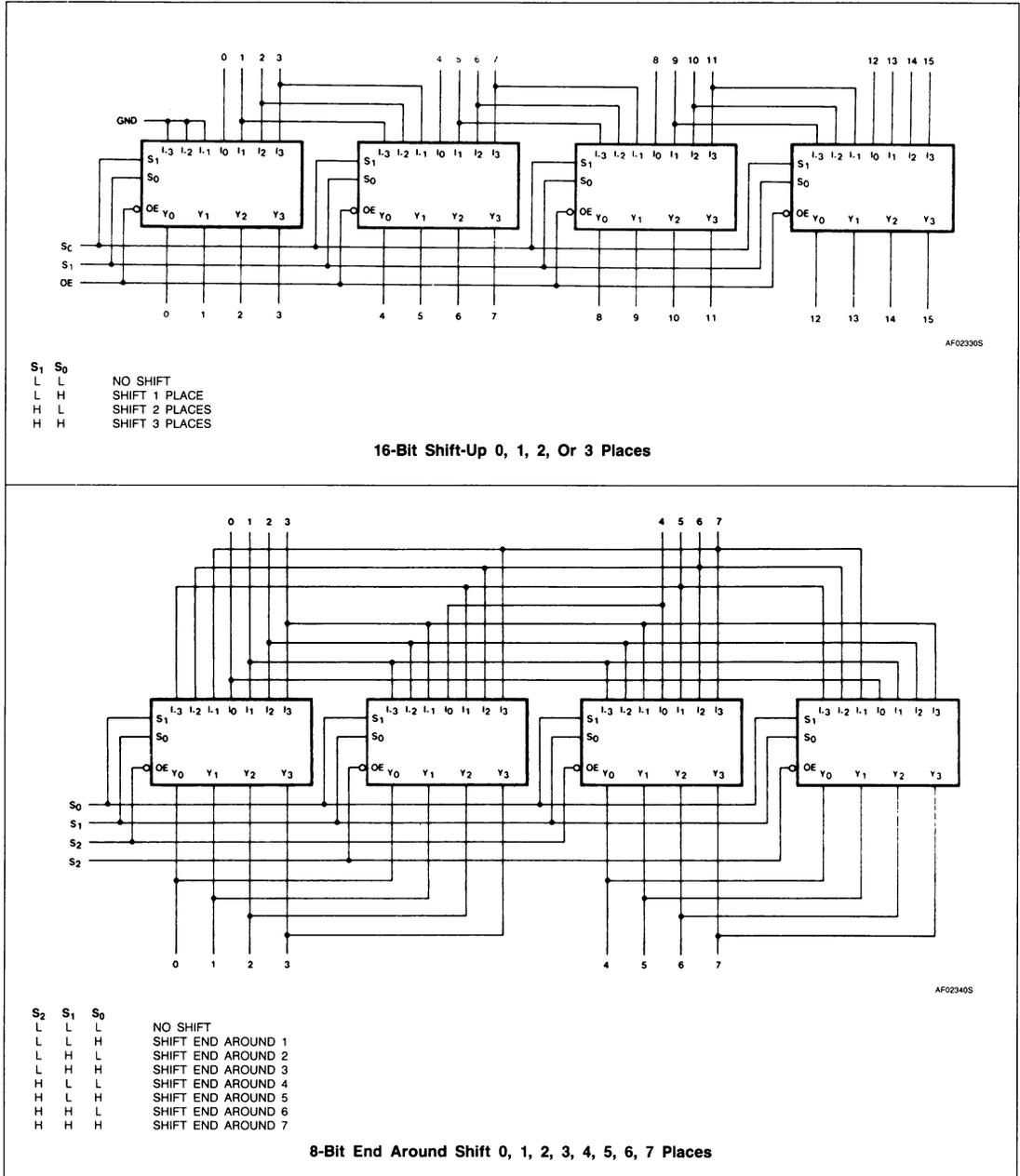
TEST CIRCUITS AND WAVEFORMS



Shifter

74S350

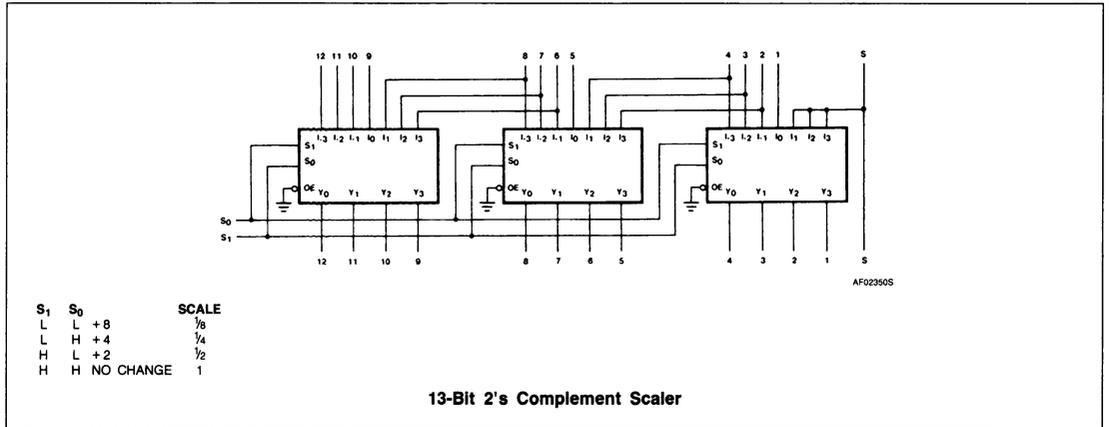
APPLICATIONS DIAGRAMS



Shifter

74S350

APPLICATIONS DIAGRAMS (Continued)



74LS352 Multiplexer

Dual 4-Line to 1-Line Multiplexer
Product Specification

Logic Products

FEATURES

- Inverting version of 'LS153
- Separate Enable for each section
- Common Select inputs
- See 'LS353 for 3-State version

DESCRIPTION

The 'LS352 is a dual 4-input multiplexer that can select 2 bits of data from up to eight sources under control of the common Select inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active LOW Enables (\bar{E}_a , \bar{E}_b) which can be used to strobe the outputs independently. Outputs (Y_a , Y_b) are forced HIGH when the corresponding Enables (\bar{E}_a , \bar{E}_b) are HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS352	15ns	6.2mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS352N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

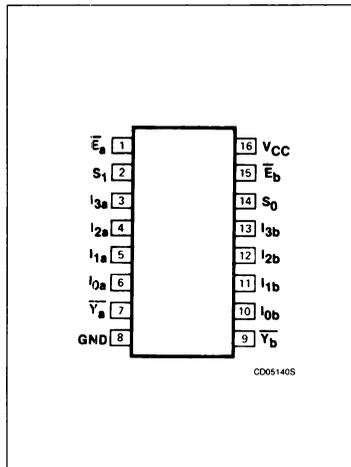
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	10LSul

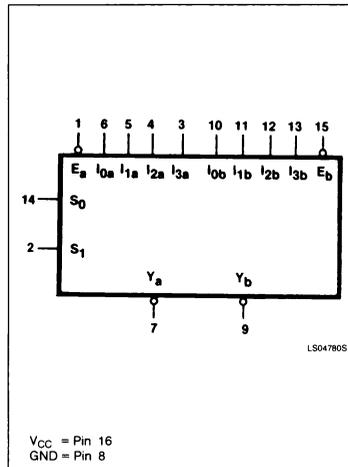
NOTE:

Where a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

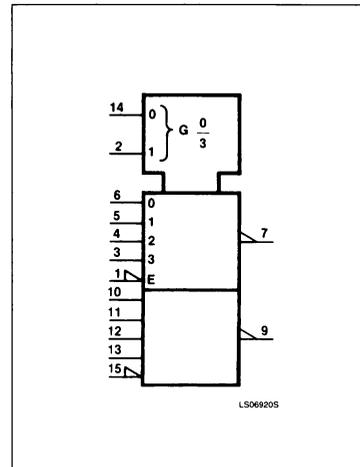
PIN CONFIGURATION



LOGIC SYMBOL



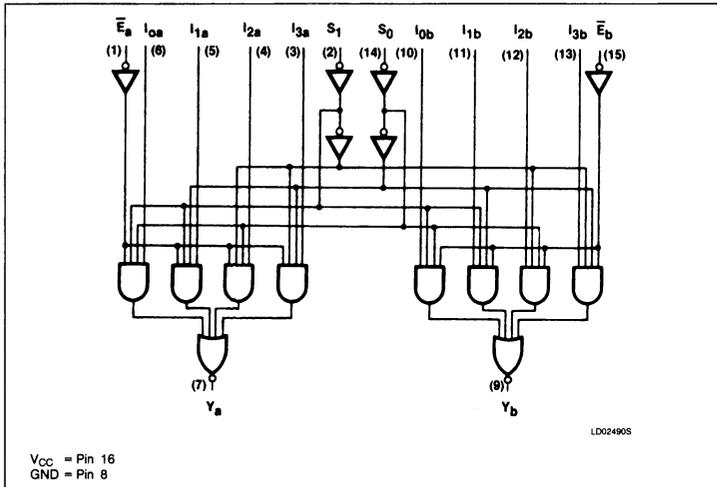
LOGIC SYMBOL (IEEE/IEC)



Multiplexer

74LS352

LOGIC DIAGRAM



The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$\bar{Y}_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\bar{Y}_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The 'LS352 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S ₀	S ₁	\bar{E}	I ₀	I ₁	I ₂	I ₃	Y
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

Multiplexer

74LS352

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μ A
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	$^{\circ}$ C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		74LS352			UNIT
				Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = \text{MAX}$		2.7	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.35	0.5	V
			$I_{OL} = 4\text{mA}$ (74LS)		0.25	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 7.0\text{V}$			0.1	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.7\text{V}$			20	μ A
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$			-0.4	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-20		-100	mA
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$			6.2	10	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

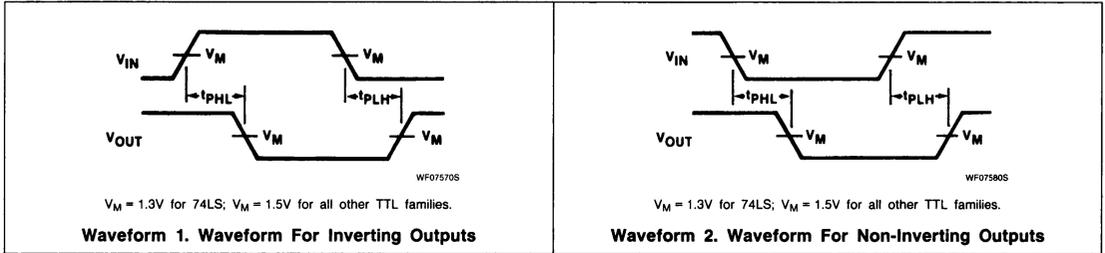
AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS		74LS		UNIT
				$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
				Min	Max	
t_{PLH}	Propagation delay	Waveform 1 or 2		29	ns	
t_{PHL}	Select to output			38		
t_{PLH}	Propagation delay	Waveform 2		24	ns	
t_{PHL}	Enable to output			32		
t_{PLH}	Propagation delay	Waveform 1		20	ns	
t_{PHL}	Data to output			26		

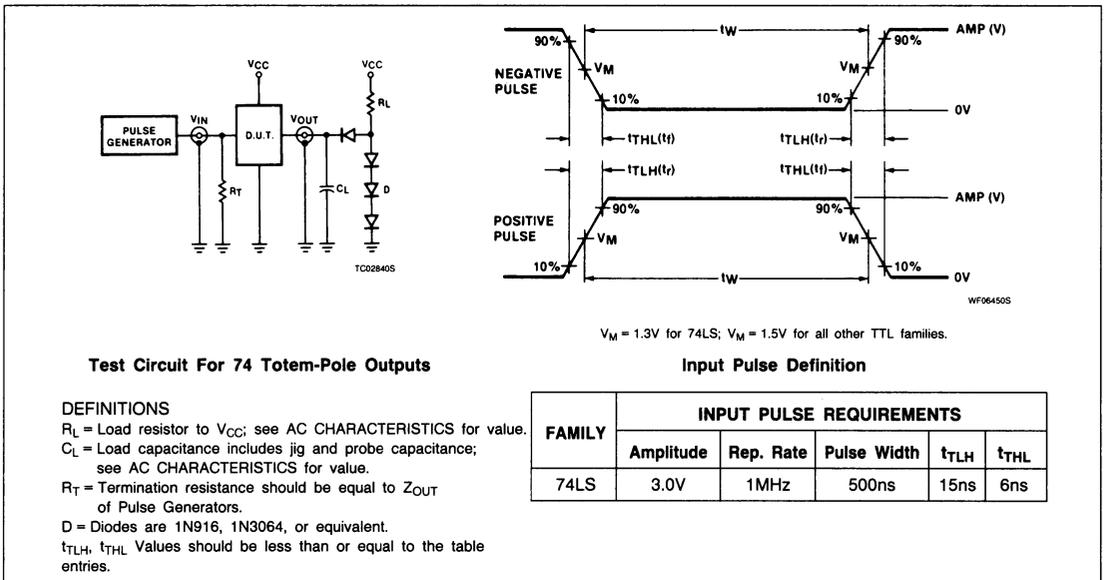
Multiplexer

74LS352

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74LS353 Multiplexer

Dual 4-Input Multiplexer (3-State)
Product Specification

Logic Products

FEATURES

- Inverting version of 'LS253
- 3-State outputs for bus interface and multiplex expansion
- Common Select inputs
- Separate Output Enable inputs

DESCRIPTION

The 'LS353 has two identical 4-input multiplexers with 3-State outputs which select two bits from eight sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\bar{E}_{0a}, \bar{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

TYPE	TYPICAL PROPAGATION DELAY (FROM DATA)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS353	12ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS353N
Plastic SO-16	N74LS353D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

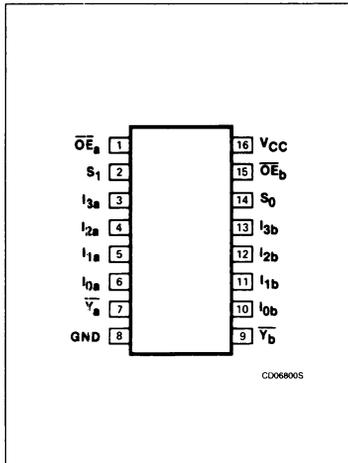
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	10LSul

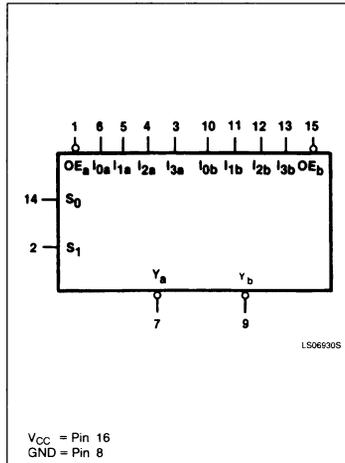
NOTE:

74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

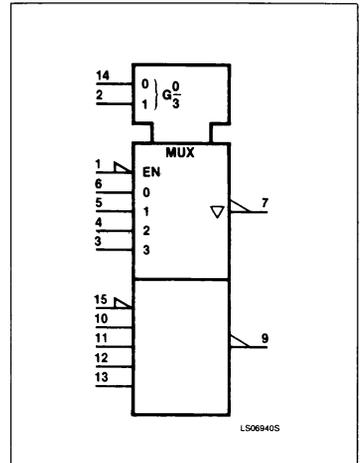
PIN CONFIGURATION



LOGIC SYMBOL



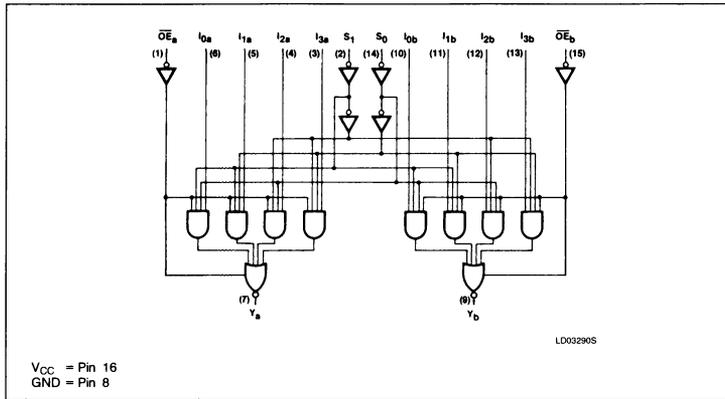
LOGIC SYMBOL (IEEE/IEC)



Multiplexer

74LS353

LOGIC DIAGRAM



The 'LS353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$\overline{Y}_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Y}_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S ₀	S ₁	I ₀	I ₁	I ₂	I ₃	OE	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER	74LS	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
I _{OH} HIGH-level output current			-2.6	mA
I _{OL} LOW-level output current			8	mA
T _A Operating free-air temperature	0		70	°C

Multiplexer

74LS353

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS353			UNIT	
		Min	Typ ²	Max		
I_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4	3.1		V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	0.35	0.5	V	
		$I_{OL} = 4\text{mA (74LS)}$	0.25	0.4	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}$	$V_O = 2.7\text{V}$		20	μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}$	$V_O = 0.4\text{V}$		-20	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 7.0\text{V}$		0.1	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$		-0.4	mA	
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$		-15	-100	mA	
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	Condition 1		7	12	mA
		Condition 2		8.5	14	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured under the following conditions with the outputs open: *Condition 1*: All inputs grounded. *Condition 2*: \overline{OE} at 4.5V, all inputs grounded.

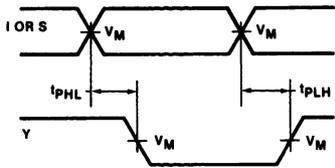
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL} Propagation delay Data to output	Waveform 1		25 20	ns
t_{PLH} t_{PHL} Propagation delay Select to output	Waveform 1		45 32	ns
t_{PZH} Output enable to HIGH level	Waveform 2		23	ns
t_{PZL} Output enable to LOW level	Waveform 3		23	ns
t_{PHZ} Output disable from HIGH level	Waveform 2, $C_L = 5\text{pF}$		41	ns
t_{PLZ} Output disable from LOW level	Waveform 3, $C_L = 5\text{pF}$		27	ns

Multiplexer

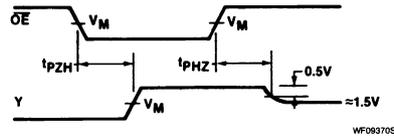
74LS353

AC WAVEFORMS



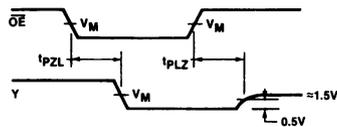
WF093605

Waveform 1. Propagation Delay Data Or Select To Input



WF093705

Waveform 2. 3-State Enable Time To High Level And Disable Time From High Level

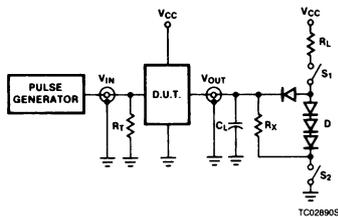


WF093805

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

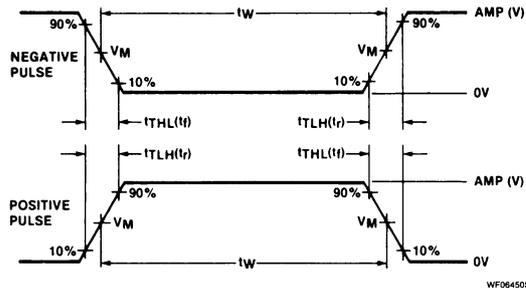
Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

TEST CIRCUITS AND WAVEFORMS



TC028905

Test Circuit For 3-State Outputs



WF064505

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS363 Latch

Octal Transparent Latch With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 8-bit transparent latch
- 3-state MOS compatible output buffers
- Common Latch Enable input with hysteresis
- Common 3-state Output Enable control
- Independent latch and 3-state buffer operation

DESCRIPTION

The '363 is an octal transparent latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs is transferred to the Latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the Data inputs while E is HIGH, and stores the data

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS363	19ns	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS363N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

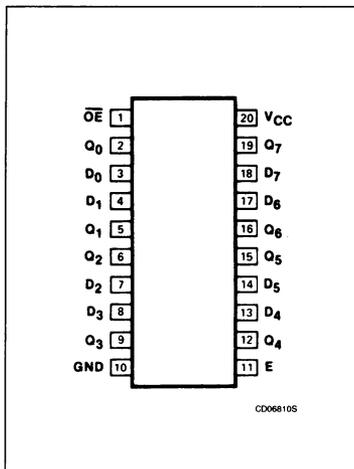
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

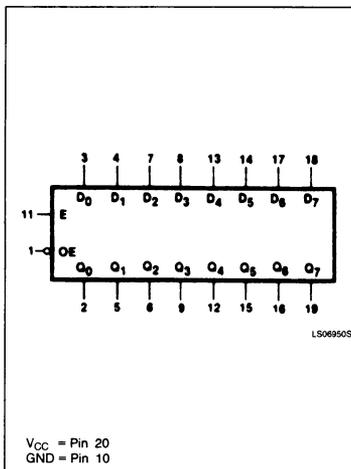
present one set-up time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis

built in to help minimize problems that signal and ground noise can cause on the latching operation.

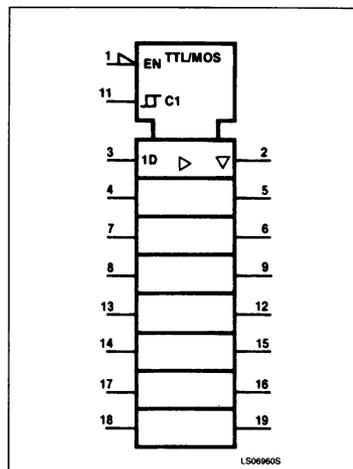
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Latch

74LS363

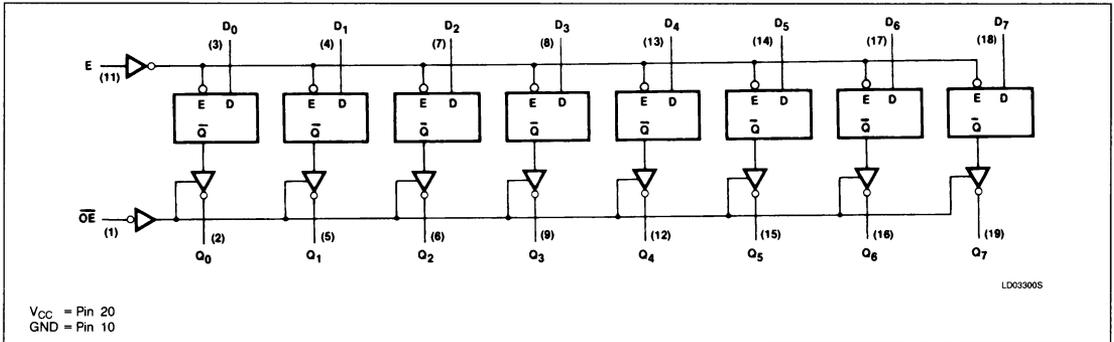
The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This

feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V.

The active LOW Output Enable (\overline{OE}) controls all eight 3-state buffers independent of the

latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	E	D_n		$Q_0 - Q_7$
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW enable transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW enable transition
 (Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	V
I_{IN} Input current	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to V_{CC}	V
T_A Operating free-air temperature range	0 to 70	°C

Latch

74LS363

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output voltage			-2.6	V
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS363			UNIT
		Min	Typ ²	Max	
V_{OH}	HIGH-level output current $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	3.65			V
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$		0.35	0.5	V
			0.25	0.4	V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied $V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_O = 3.65\text{V}$			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied $V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_O = 0.4\text{V}$			-20	μA
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			0.1	mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-0.4	mA
I_{OS}	Short-circuit output current ³ $V_{CC} = \text{MAX}$	-30		-130	mA
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}, \overline{OE} = 4.5\text{V}$		42	70	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Latch enable to output Waveform 1		30 36	ns
t_{PLH} t_{PHL}	Propagation delay Data to output Waveform 4		23 27	ns
t_{PZH}	Enable time to HIGH level Waveform 2		28	ns
t_{PZL}	Enable time to LOW level Waveform 3		36	ns
t_{PHZ}	Disable time from HIGH level Waveform 2, $C_L = 5\text{pF}$		20	ns
t_{PZL}	Disable time from LOW level Waveform 3, $C_L = 5\text{pF}$		25	ns

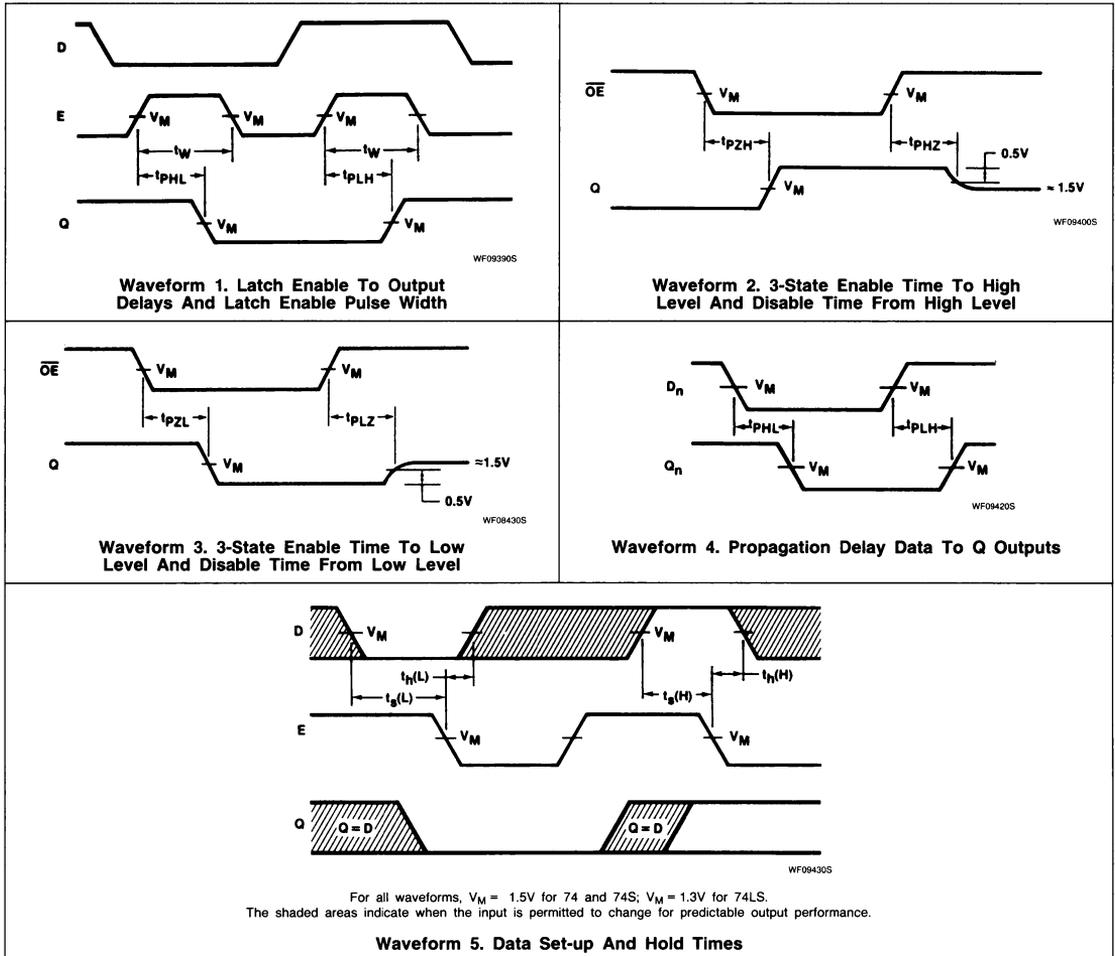
Latch

74LS363

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W	Latch enable pulse width	Waveform 1	15	ns
t_s	Set-up time, data to latch enable	Waveform 5	0	ns
t_h	Hold time, data to latch enable	Waveform 5	10	ns

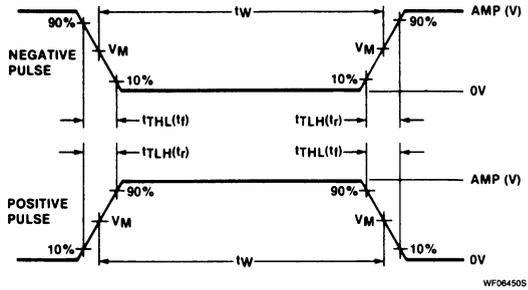
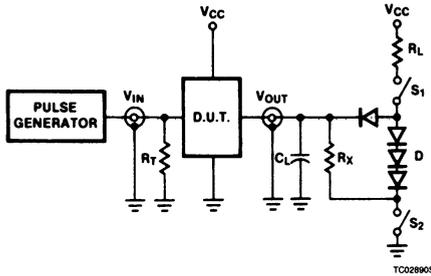
AC WAVEFORMS



Latch

74LS363

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
tpZH	Open	Closed
tpZL	Closed	Open
tpHZ	Closed	Closed
tpLZ	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS364 Flip-Flop

Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 8-bit positive edge-triggered register
- 3-State MOS compatible output buffers
- Common Clock input with hysteresis
- Common 3-State Output Enable control
- Independent register and 3-State buffer operation

DESCRIPTION

The '364 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transi-

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS364	50MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS364N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

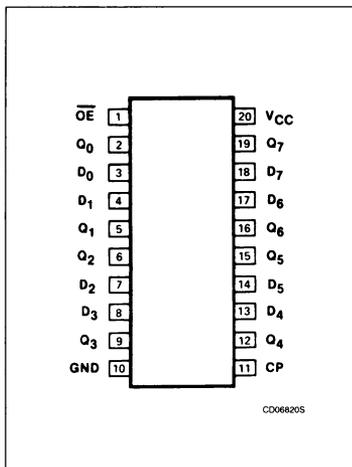
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

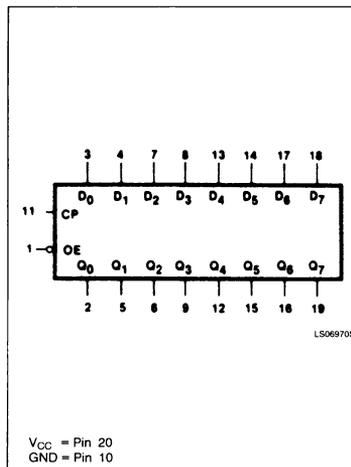
tion, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to

help minimize problems that signal and ground noise can cause on the clocking operation.

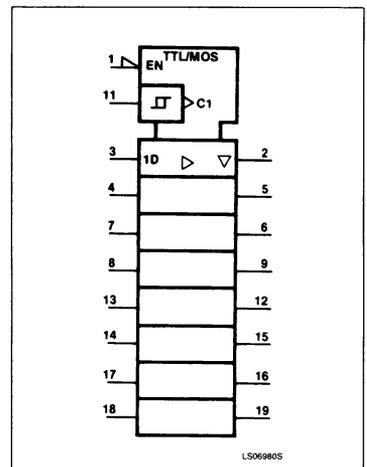
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Flip-Flop

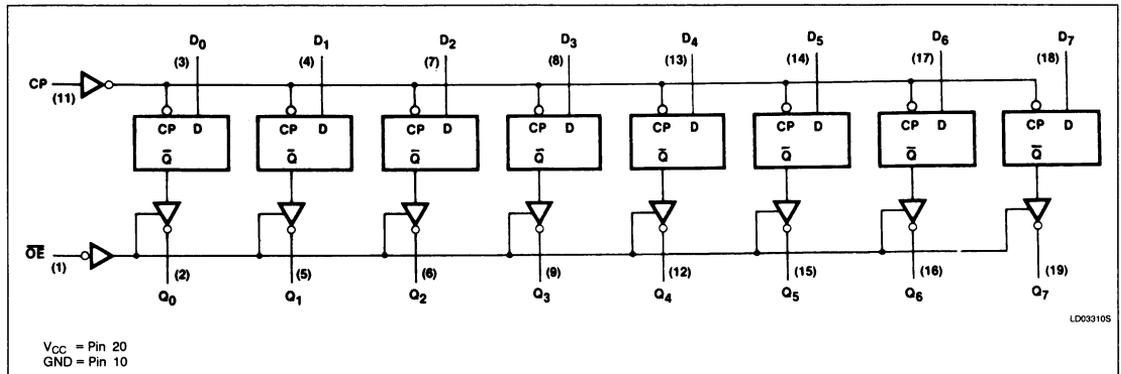
74LS364

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-State buffer by driving the output about 1V closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This

feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register

appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		$Q_0 - Q_7$
Load and read register	L	\uparrow	l	L	L
	L	\uparrow	h	H	H
Latch register and disable outputs	H	\uparrow	l	L	(Z)
	H	\uparrow	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
 \uparrow = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

Flip-Flop

74LS364

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IH}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-2.6	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		74LS364			UNIT
				Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$		3.65			V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$			0.35	0.5	V
				$I_{OL} = \text{MAX}$		0.25	0.4
	$I_{OL} = 12\text{mA (74LS)}$						
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_O = 3.65\text{V}$				20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_O = 0.4\text{V}$				-20	μA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				0.1	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$				-0.4	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-30		-130	mA
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}, \overline{OE} = 4.5\text{V}$			42	70	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Flip-Flop

74LS364

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	35	MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	33 34	ns
t_{PZH}	Enable time to HIGH level	Waveform 2	28	ns
t_{PZL}	Enable time to LOW level	Waveform 3	36	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5\text{pF}$	18	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5\text{pF}$	24	ns

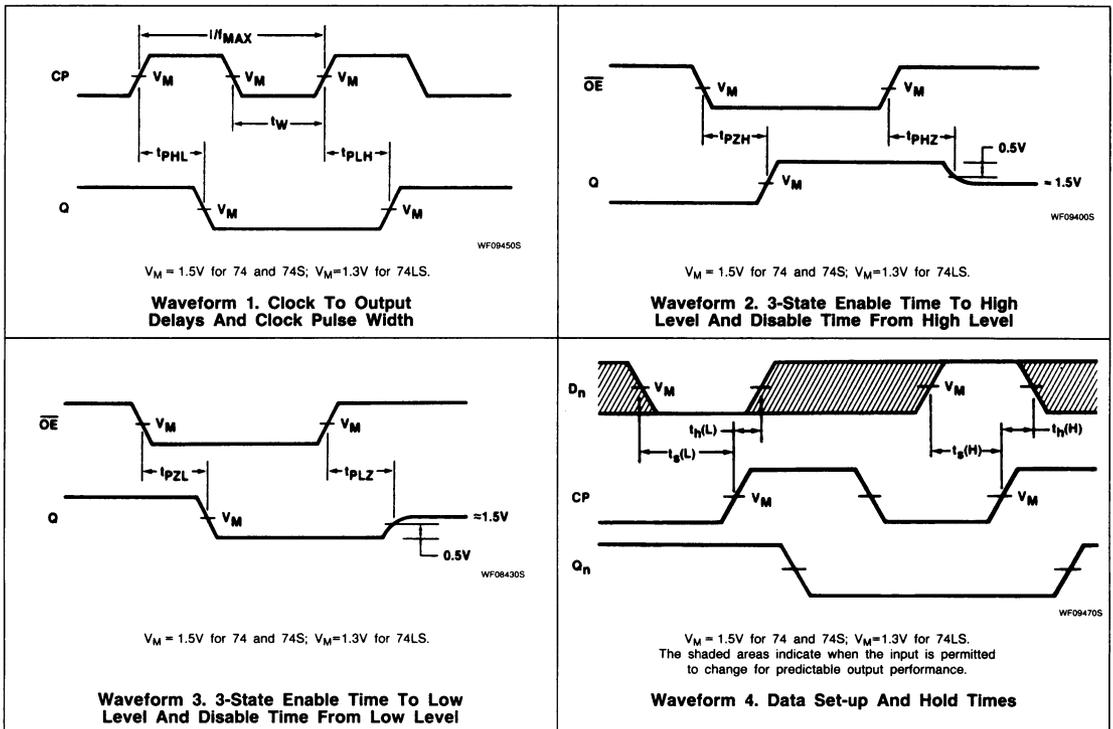
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_w	Clock pulse width	Waveform 1	15	ns
t_s	Set-up time, data to clock	Waveform 4	20	ns
t_h	Hold time, data to clock	Waveform 4	0	ns

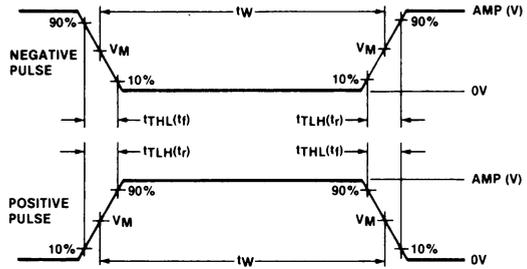
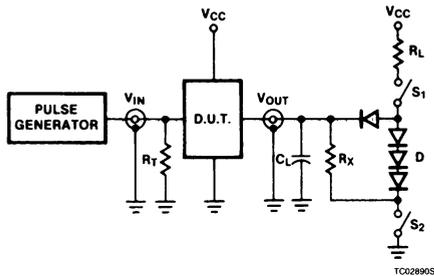
AC WAVEFORMS



Flip-Flop

74LS364

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74365A, 366A, 367A, 368A, LS365A, LS366A, LS367A, LS368A Buffers/Drivers

'365A, '367A Hex Buffer/Driver (3-State)
'366A, '368A Hex Inverter Buffer (3-State)
Product Specification

Logic Products

FUNCTION TABLE, '365A, '366A

INPUTS			OUTPUTS	
\overline{OE}_1	\overline{OE}_2	I	Y	\overline{Y}
L	L	L	L	H
L	L	L	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

FUNCTION TABLE, '367A, '368A

INPUTS		OUTPUTS	
\overline{OE}	I	Y	\overline{Y}
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74365A, 367A	10ns	65mA
74LS365A, 367A	10ns	14mA
74366A, 368A	9ns	59mA
74LS366A, 368A	10ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74365AN, N74LS365AN, N74366AN, N74LS366AN N74367AN, N74LS367AN, N74368AN, N74LS368AN
Plastic SO-16	N74LS365AD, N74LS367AD, N74LS368AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

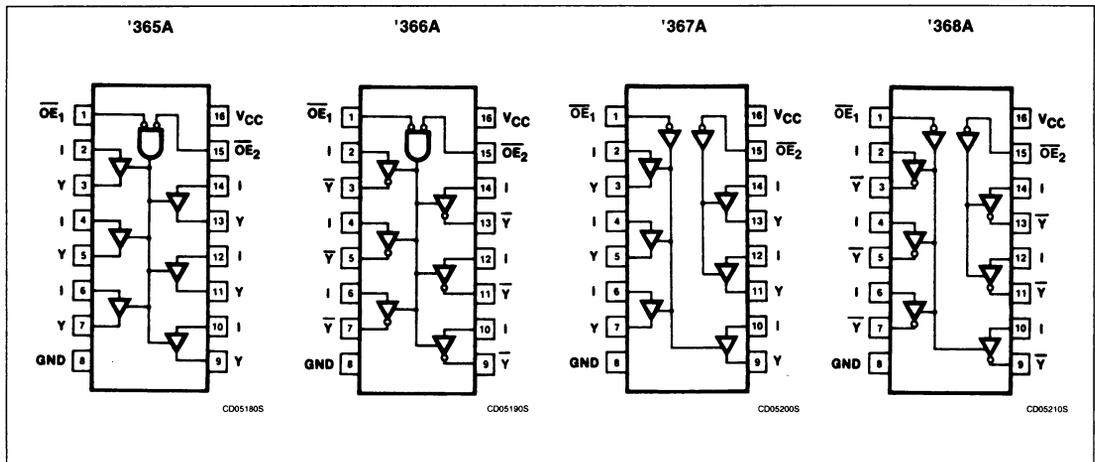
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	20ul	30LSul

NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

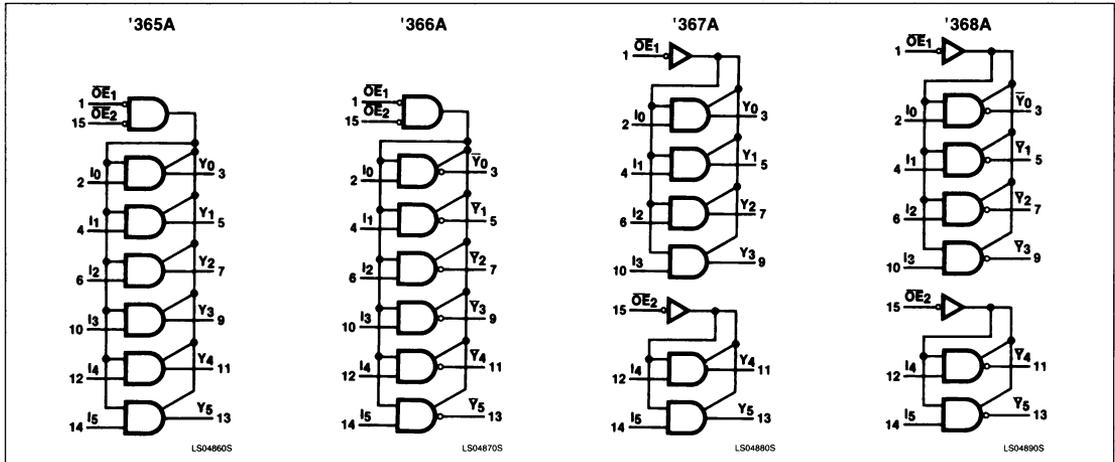
PIN CONFIGURATION



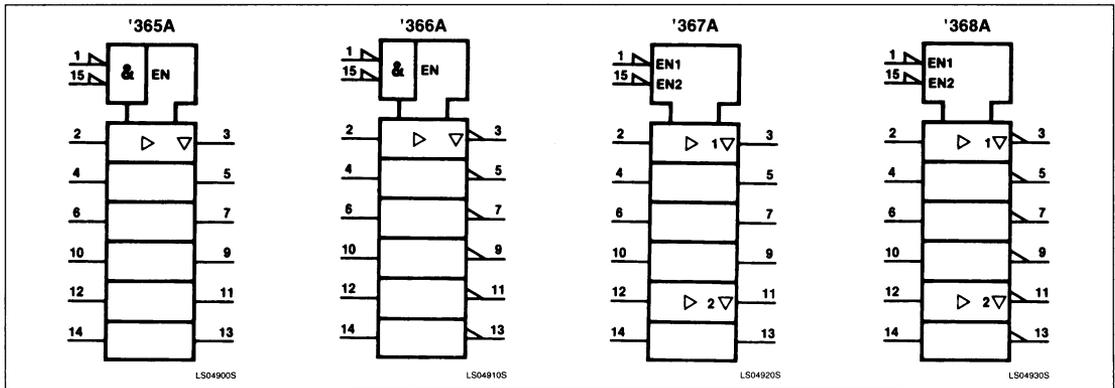
Buffers/Drivers

74365A, 366A, 367A, 368A,
LS365A, LS366A, LS367A, LS368A

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

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Buffers/Drivers

74365A, 366A, 367A, 368A,
LS365A, LS366A, LS367A, LS368A

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current			-5.2			-2.6	mA
I _{OL}	LOW-level output current			32			24	mA
T _A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74365A, '366A, '367A, '368A			74LS365A, '366A, '367A, '368A			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.1		2.4	3.1		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX			0.4	0.35	0.5	V	
		I _{OL} = 12mA (74LS)				0.25	0.4	V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _{OZH}	Off-state output current HIGH-level voltage applied V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V			40			20	μA	
I _{OZL}	Off-state output current, LOW-level voltage applied V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.4V			-40			-20	μA	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V					0.1	mA	
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40			μA	
		V _I = 2.7V					20	μA	
I _{IL}	LOW-level input current V _{CC} = MAX	I inputs, V _I = 0.5V Either OE input at 2.0V Does not apply to 'LS365A or 'LS367A			-40			-20	μA
		I inputs V _I = 0.4V Both OE inputs at 0.4V			-1.6			-0.4	mA
		OE inputs V _I = 0.4V			-1.6			-0.4	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-40		-130	-30		-130	mA	
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX	'365A, '367A			65	85	14	24	mA
		'366A, '368A			59	77	12	21	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Data inputs grounded and Output Enable inputs at 4.5V.

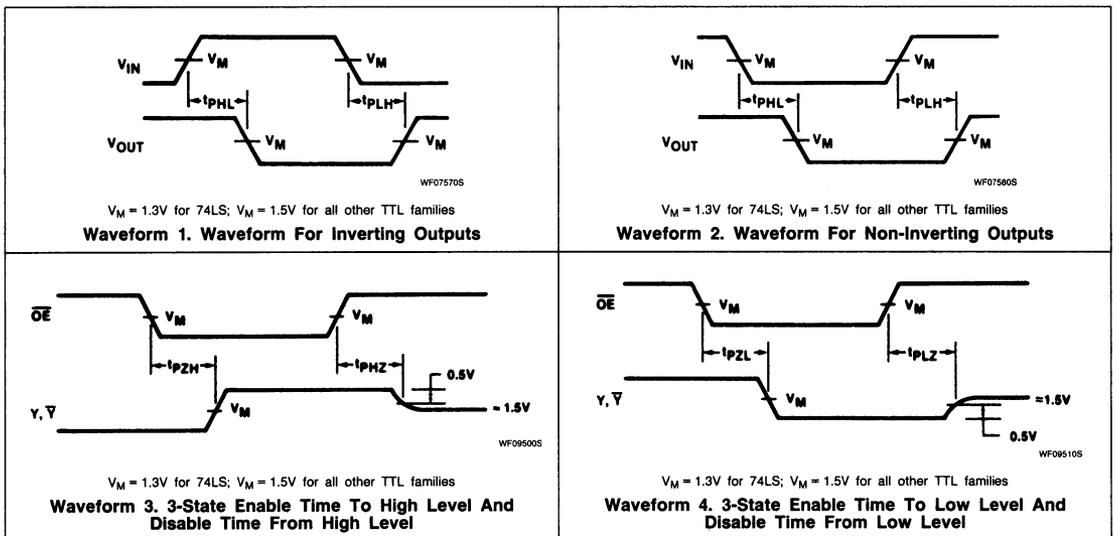
Buffers/Drivers

74365A, 366A, 367A, 368A,
LS365A, LS366A, LS367A, LS368A

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		$C_L = 50\text{pF}$, $R_L = 400\Omega$		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1, '366A, '368A		17 16		15 18	ns
t_{PLH} t_{PHL}	Propagation delay Waveform 2, '365A, '367A		16 22		16 22	ns
t_{PZH}	Enable to HIGH Waveform 3		35		35	ns
t_{PZL}	Enable to LOW Waveform 4	'365A, '367A	37		40	ns
		'366A, '368A	37		45	ns
t_{PHZ}	Disable from HIGH Waveform 3, $C_L = 5\text{pF}$	'365A, '367A	11		30	ns
		'366A, '368A	11		32	ns
t_{PLZ}	Disable from LOW Waveform 4, $C_L = 5\text{pF}$		27		35	ns

AC WAVEFORMS

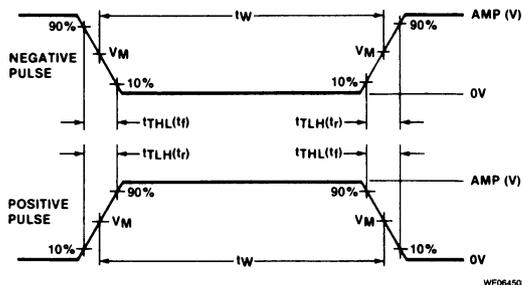
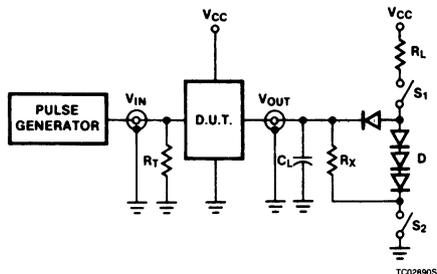


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Buffers/Drivers

74365A, 366A, 367A, 368A, LS365A, LS366A, LS367A, LS368A

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

74LS373, 74LS374, S373, S374

Latches/Flip-Flops

'373 Octal Transparent Latch With 3-State Outputs

'374 Octal D Flip-Flop With 3-State Outputs

Product Specification

FEATURES

- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS373	19ns	24mA
74S373	10ns	105mA
74LS374	19ns	27mA
74S374	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS373N, N74S373N, N74LS374N, N74S374N
Plastic SOL-20	N74LS373D, N74S373D, N74LS374D, N74S374D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

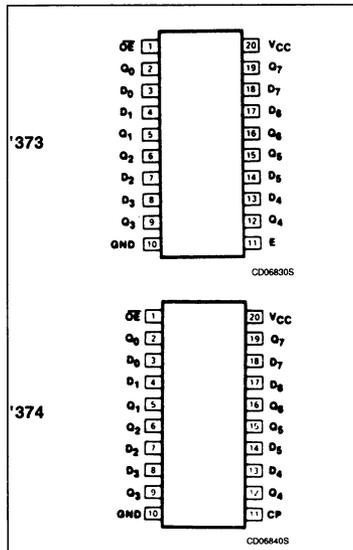
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

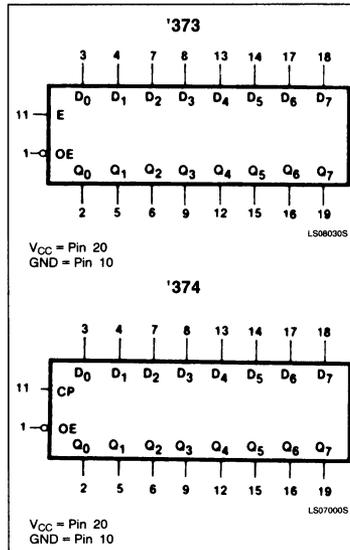
NOTE:

Where a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

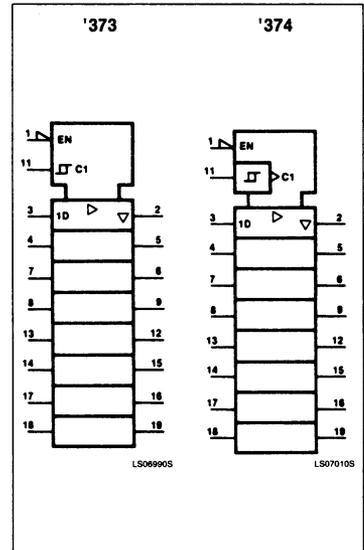
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/EC)



Latches/Flip-Flops

74LS373, 74LS374, S373, S374

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch

operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

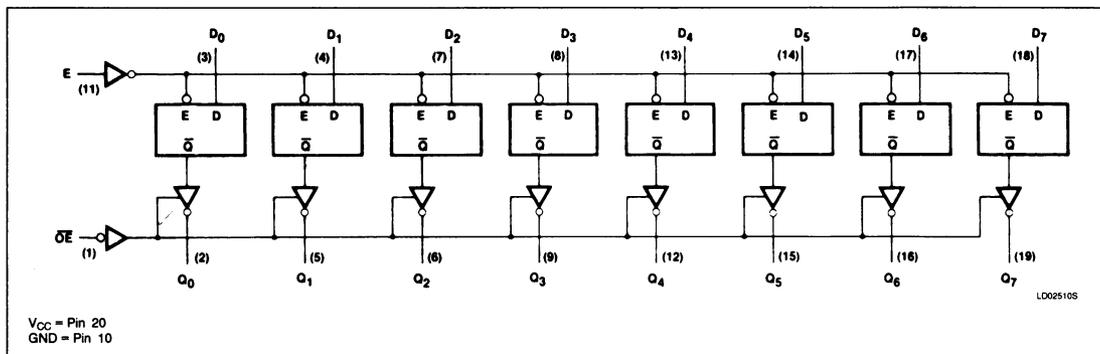
The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred

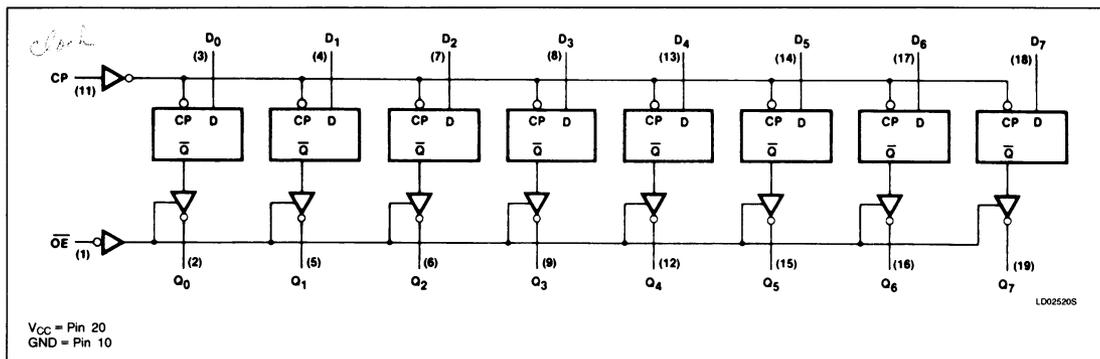
to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT — FUNCTION TABLE '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	E	D_n		$Q_0 - Q_7$
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

Latches/Flip-Flops

74LS373, 74LS374, S373, S374

MODE SELECT — FUNCTION TABLE '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		$Q_0 - Q_7$
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	(Z) (Z)

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW \overline{OE} transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW \overline{OE} transition

(Z) = HIGH impedance "off" state

↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	2.0			2.0			V
V_{IL}			+0.8			+0.8	V
I_{IK}			-18			-18	mA
I_{OH}			-2.6			-6.5	mA
I_{OL}			24			20	mA
T_A	0		70	0		70	°C

Latches/Flip-Flops

74LS373, 74LS374, S373, S374

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS373, 374			74S373, 374			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.1		2.4	3.1		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5		0.5	V	
		I _{OL} = 12mA (74LS)		0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V					20	μA	
		V _O = 2.4V					50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V					-20	μA	
		V _O = 0.5V					-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V					0.1	mA	
		V _I = 5.5V					1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V						20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V					-0.4	mA	
		V _I = 0.5V					-0.25	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-30		-130	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCZ} \overline{OE} = 4.5V 'LS373		24	40				mA
		I _{CCL} \overline{OE} = 0V 'S373					105	160	mA
		I _{CCZ} \overline{OE} = 4.5V 'LS374		27	40				mA
		I _{CCL} All inputs grounded 'S374					102	140	mA
		I _{CCZ} CP, \overline{OE} = 4.5V D inputs = GND 'S374					131	180	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C _L = 45pF, R _L = 667Ω		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 6, '374	35		75		MHz
t _{PLH} Propagation delay	Waveform 1, '373		30		14	ns
t _{PHL} Latch enable to output			30		18	
t _{PLH} Propagation delay	Waveform 4, '373		18		12	ns
t _{PHL} Data to output			18		12	
t _{PLH} Propagation delay	Waveform 6, '374		28		15	ns
t _{PHL} Clock to output			28		17	
t _{PZH} Enable time to HIGH level	Waveform 2		28		15	ns
t _{PZL} Enable time to LOW level	Waveform 3, '373 '374		36		18	ns
			28		18	
t _{PHZ} Disable time from HIGH level	Waveform 2, C _L = 5pF		20		9	ns
t _{PLZ} Disable time from LOW level	Waveform 3, C _L = 5pF		25		12	ns

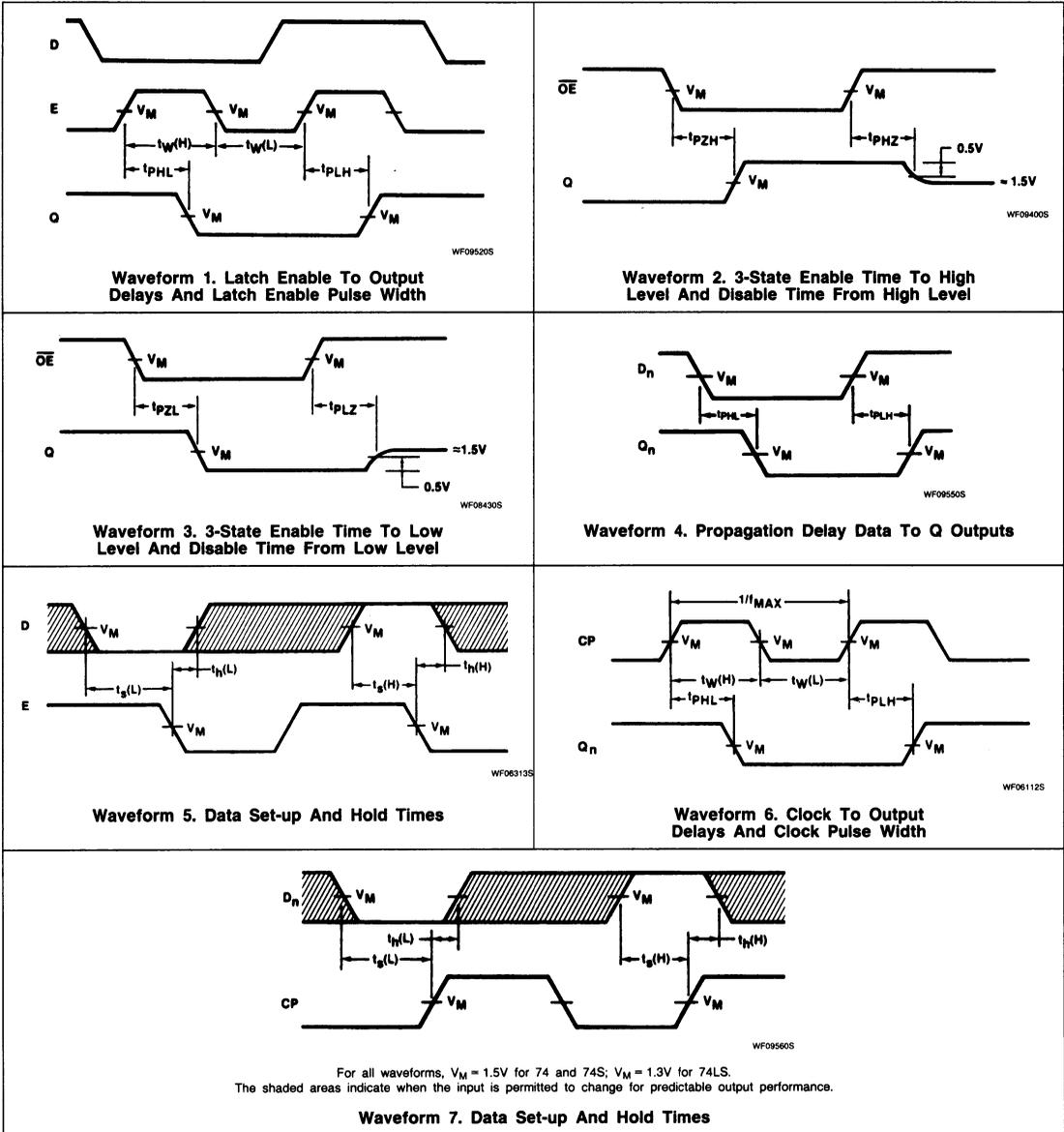
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Latches/Flip-Flops

74LS373, 74LS374, S373, S374

AC WAVEFORMS



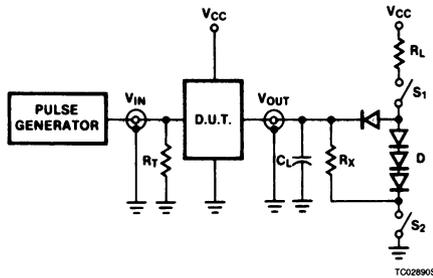
Latches/Flip-Flops

74LS373, 74LS374, S373, S374

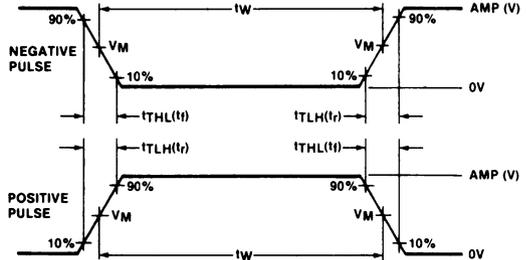
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$ $t_{w(L)}$	Latch enable pulse width	Waveform 1, '373	15 15		6 7.3	ns
t_s	Set-up time, data to latch enable	Waveform 5, '373	5		0	ns
t_h	Hold time, data to latch enable	Waveform 5, '373	20		10	ns
$t_{w(H)}$ $t_{w(L)}$	Clock pulse width	Waveform 6, '374	15 15		6 7.3	ns
t_s	Set-up time, data to clock	Waveform 7, '374	20		5	ns
t_h	Hold time, data to clock	Waveform 7, '374	0		2	ns

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1\text{k}\Omega$ for 74, 74S, $R_X = 5\text{k}\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS375 Latch

Quad Bistable Latch
Product Specification

Logic Products

FEATURES

- Quad transparent latch
- Complementary outputs

DESCRIPTION

The '375 has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one set-up time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched output remains stable as long as the enable is LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS375	12ns	6.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS375N
Plastic SO-16	N74LS375D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

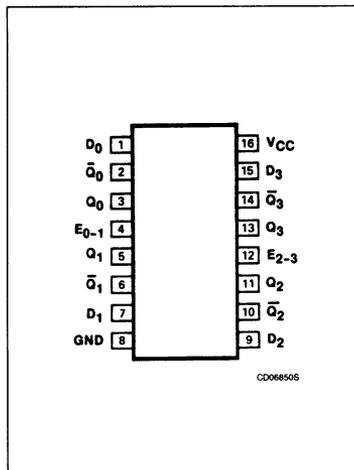
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$D_0 - D_3$	Inputs	1LSul
E_{0-1}, E_{2-3}	Inputs	4LSul
All	Outputs	10LSul

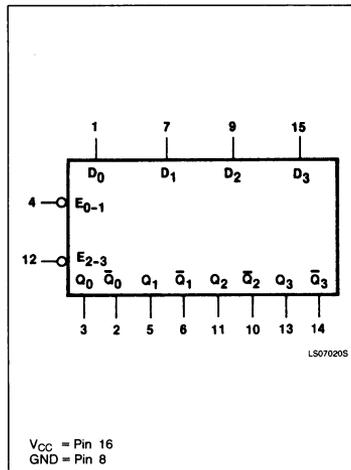
NOTE:

Where a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

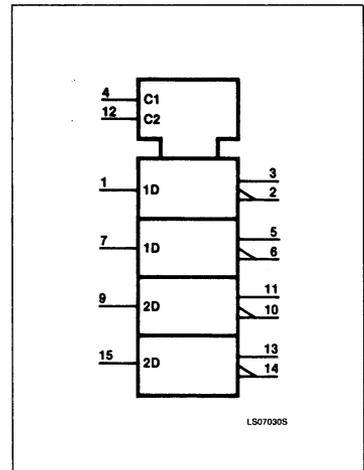
PIN CONFIGURATION



LOGIC SYMBOL



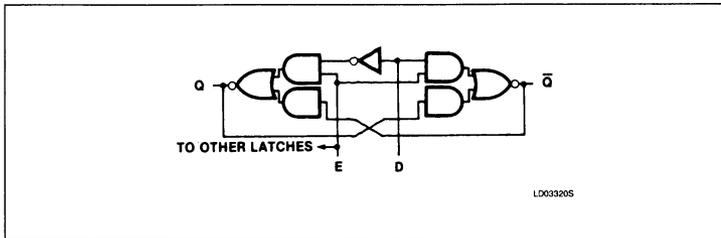
LOGIC SYMBOL (IEEE/IEC)



Latch

74LS375

LOGIC DIAGRAM (Each Latch)



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	\bar{Q}
Data Enabled	H	L	L	H
	H	H	H	L
Data Latched	L	X	q	\bar{q}

H = HIGH voltage level

L = LOW voltage level

X = Don't care.

q = Lower case letters indicate the state of referenced output one set-up time prior to the HIGH-to-LOW Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output voltage			-400	μ A
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

Latch

74LS375

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS375			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.5		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN V _{IL} = MAX	I _{OL} = MAX	0.35	0.5	V
		I _{OL} = 4mA	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V	D ₀ -D ₃ inputs		0.1	mA
		E ₀₋₁ , E ₂₋₃ Inputs		0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	D ₀ -D ₃ inputs		20	μA
		E ₀₋₁ , E ₂₋₃ Inputs		80	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	D ₀ -D ₃ inputs		-0.4	mA
		E ₀₋₁ , E ₂₋₃ inputs		-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		6.3	12	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} MAX +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Test I_{CC} with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to Q output	Waveform 1	27 17	ns
t _{PLH} t _{PHL}	Propagation delay Data to Q̄ output	Waveform 2	20 15	ns
t _{PLH} t _{PHL}	Propagation delay Enable to Q output	Waveform 3	27 25	ns
t _{PLH} t _{PHL}	Propagation delay Enable to Q̄ output	Waveform 3	30 15	ns

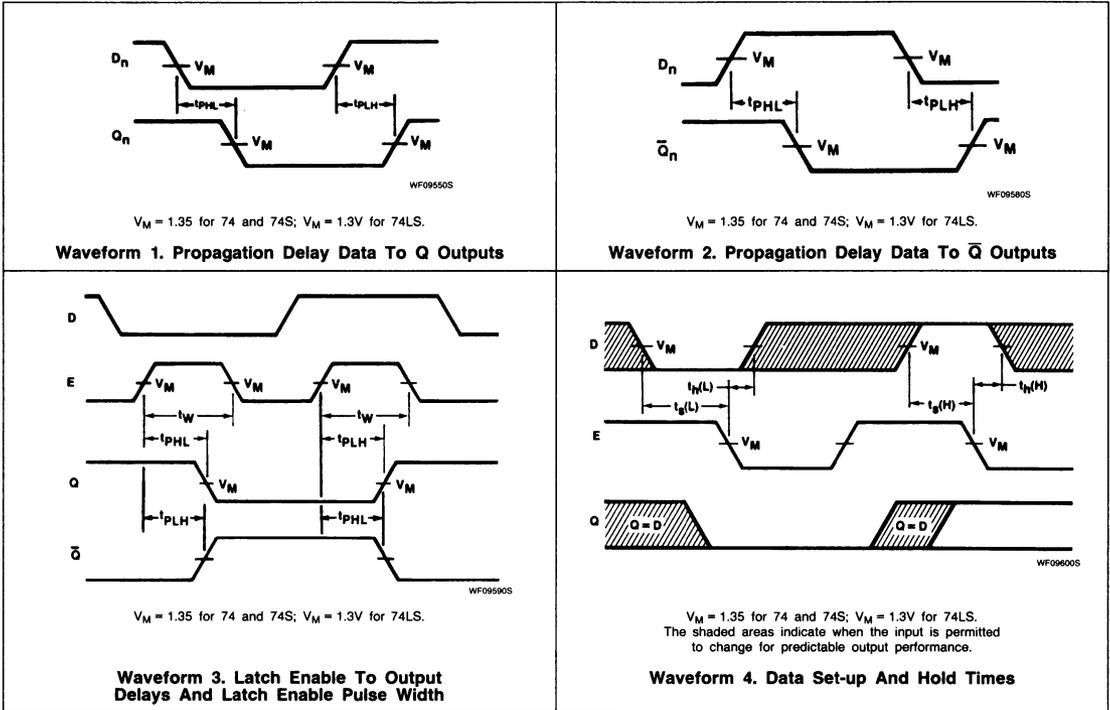
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t _w	Enable pulse width	Waveform 3	20	ns
t _s	Setup time, Data to Enable	Waveform 4	20	ns
t _h	Hold time, Data to Enable	Waveform 4	0	ns

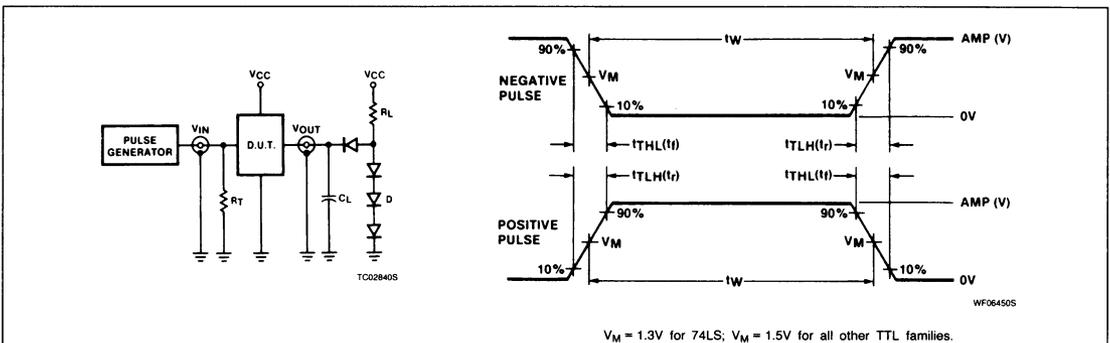
Latch

74LS375

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS377 Flip-Flop

Octal D Flip-Flop With Clock Enable
Product Specification

Logic Products

FEATURES

- Ideal for addressable register applications
- Clock Enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Slim 20-pin plastic and ceramic DIP packages
- See '273 for Master Reset version
- See '373 for transparent latch version
- See '374 for 3-state version

DESCRIPTION

The '377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

The register is fully edge triggered. The state of each D input, one set-up time

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS377	40MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS377N
Plastic SOL-20	N74LS377D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	10LSul

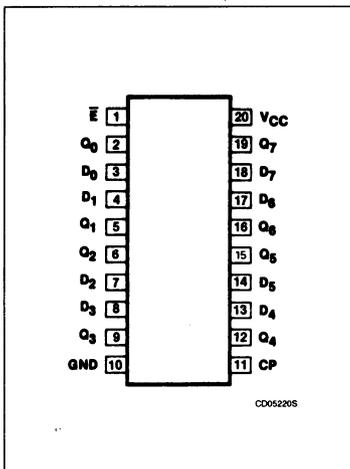
NOTE:

Where a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

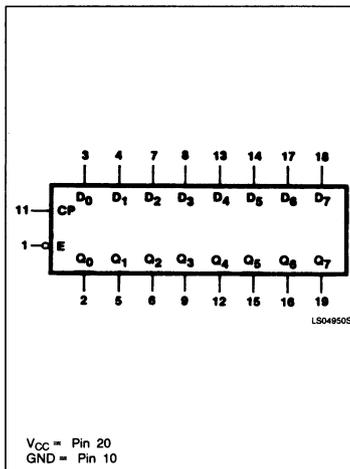
before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must

be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATION

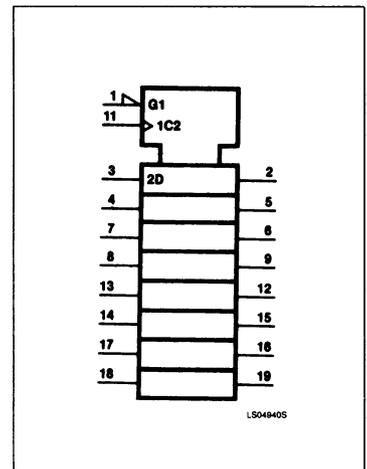


LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

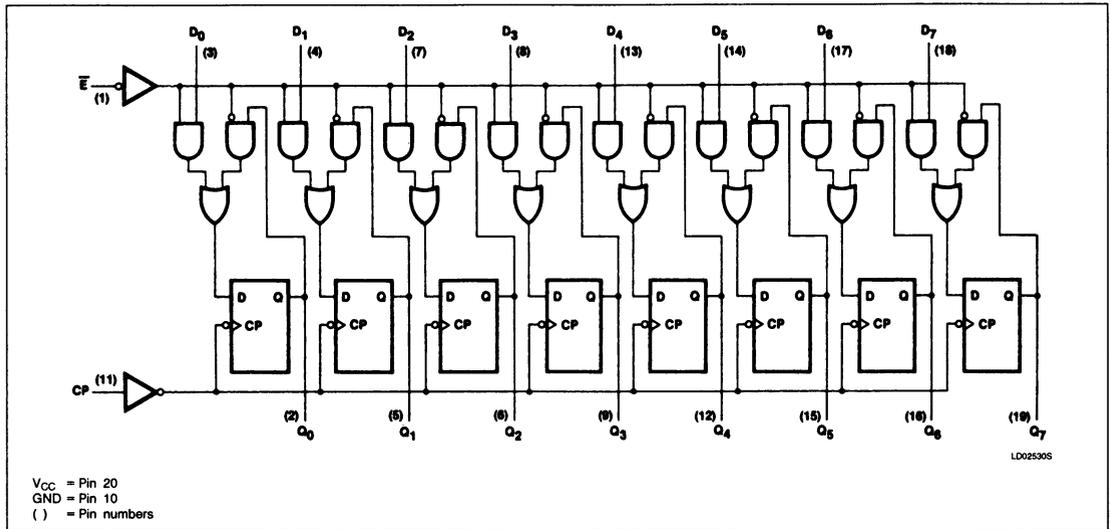
LOGIC SYMBOL (IEEE/IEC)



Flip-Flop

74LS377

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	\overline{CE}	D_n	Q_n
Load "1"	↑	L	h	H
Load "0"	↑	L	↑	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

Flip-Flop

74LS377

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output voltage			-400	μA
I _{OL}	LOW-level output current			8	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS377			UNIT
		Min	Typ ²	Max	
I _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.5		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.35	0.5	V
		I _{OL} = 4mA	0.25	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 7.0V			0.1	mA
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V			-0.4	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	-20		-100	mA
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CCH} Outputs HIGH	18	28	mA
		I _{CCL} Outputs LOW	22	35	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
f _{MAX}	Maximum clock frequency Waveform 1	30		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to output Waveform 1		27 27	ns

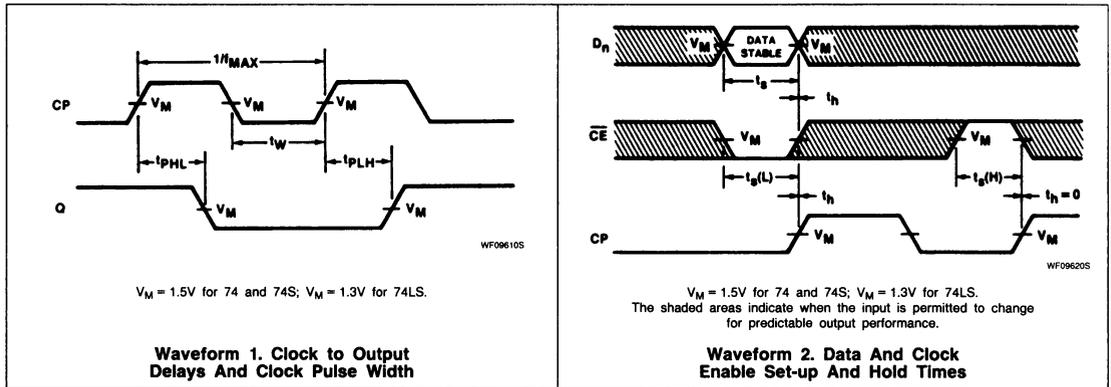
Flip-Flop

74LS377

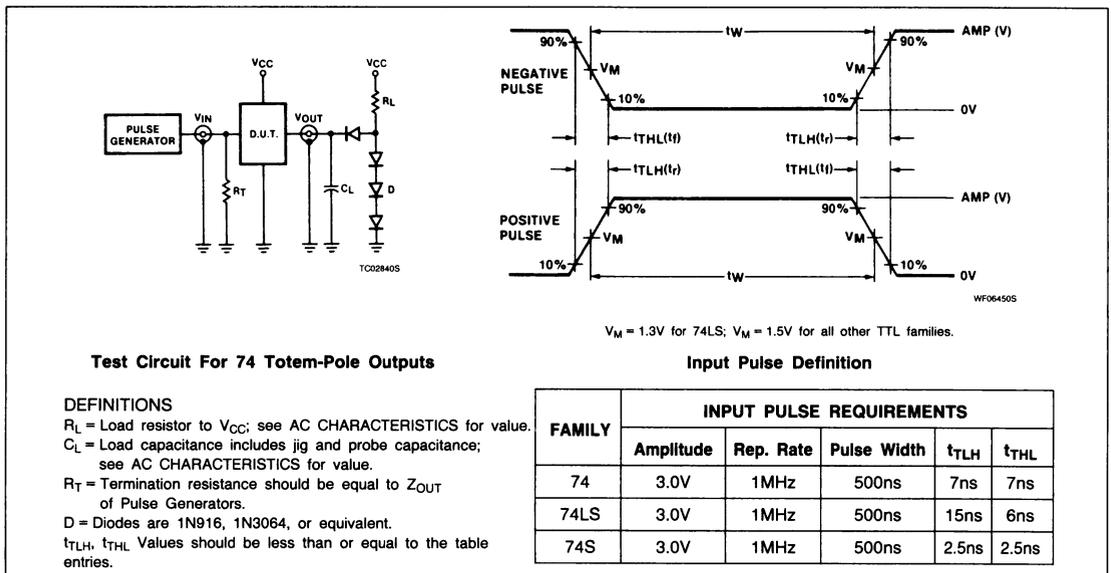
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
$t_{W(L)}$	Clock pulse width (LOW)	Waveform 1	20	ns
t_s	Setup, Data to CP	Waveform 2	20	ns
t_h	Hold time, Data to CP	Waveform 2	5	ns
t_s	Setup time, \overline{CE} to CP	Waveform 2	20	ns
t_h	Hold time, \overline{CE} to CP	Waveform 2	5	ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74LS378 Flip-Flop

Hex D Flip-Flop With Clock Enable
Product Specification

Logic Products

FEATURES

- Ideal for addressable register applications
- Six edge-triggered D flip-flops
- Buffered common clock
- Clock Enable for address and data synchronization applications
- See '174 for Master Reset version

DESCRIPTION

The '378 has six edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable (\overline{CE}) is low.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input is also

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS378	40MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS378N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	10LSul

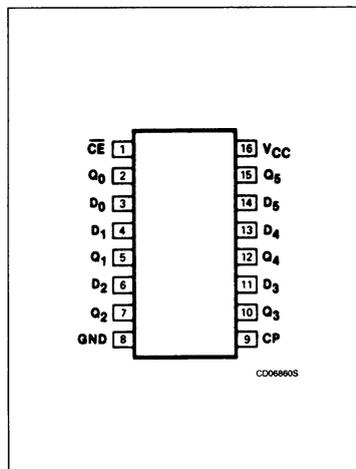
NOTE:

Where a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

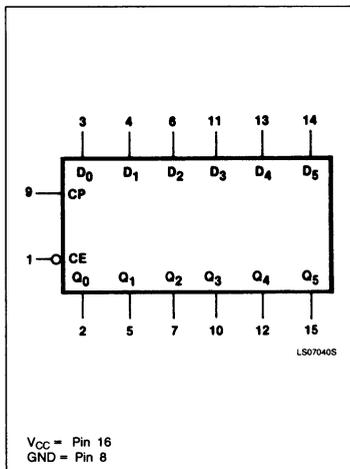
edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

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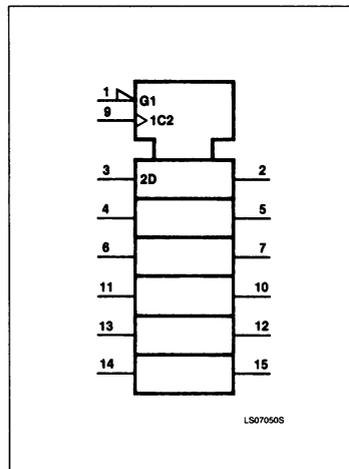
PIN CONFIGURATION



LOGIC SYMBOL



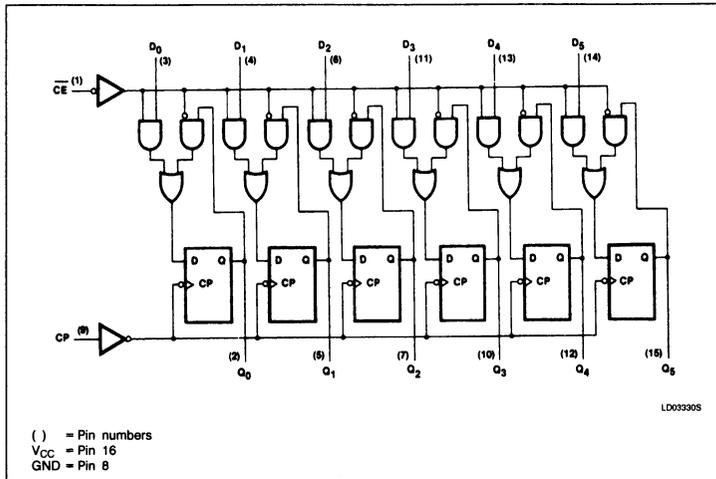
LOGIC SYMBOL (IEEE/IEC)



Flip-Flop

74LS378

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING	INPUTS			OUTPUTS
	CP	CE	D _n	Q _n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-400	μA
I _{OL}	LOW-level output current			8	mA
T _A	Operating free-air temperature	0		70	°C

Flip-Flop

74LS378

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS01			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.5		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN V _{IL} = MAX	I _{OL} = MAX	0.35	0.5	V
		I _{OL} = 4mA	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		15	24	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With ground to all data inputs and the Clock Enable input and all outputs open, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	30		MHz
t _{PLH} Propagation delay	Waveform 1		27	ns
t _{PHL} Clock to output			27	

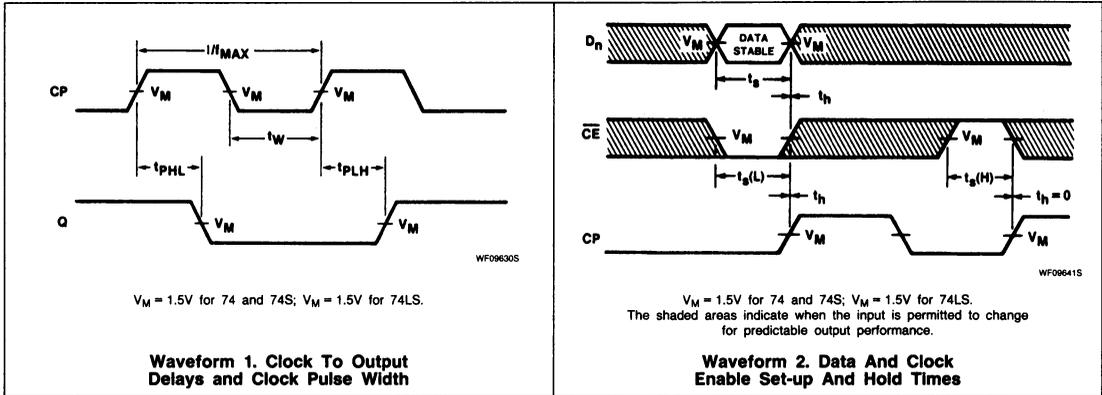
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t _{W(L)} Clock pulse width (LOW)	Waveform 1	20		ns
t _s Set-up time, Data to CP	Waveform 2	20		ns
t _h Hold time, Data to CP	Waveform 2	0		0
t _s Set-up time, \overline{CE} to CP	Active state	25		ns
	Inactive state	10		ns
t _h Hold time, \overline{CE} to CP	Waveform 2	5		ns

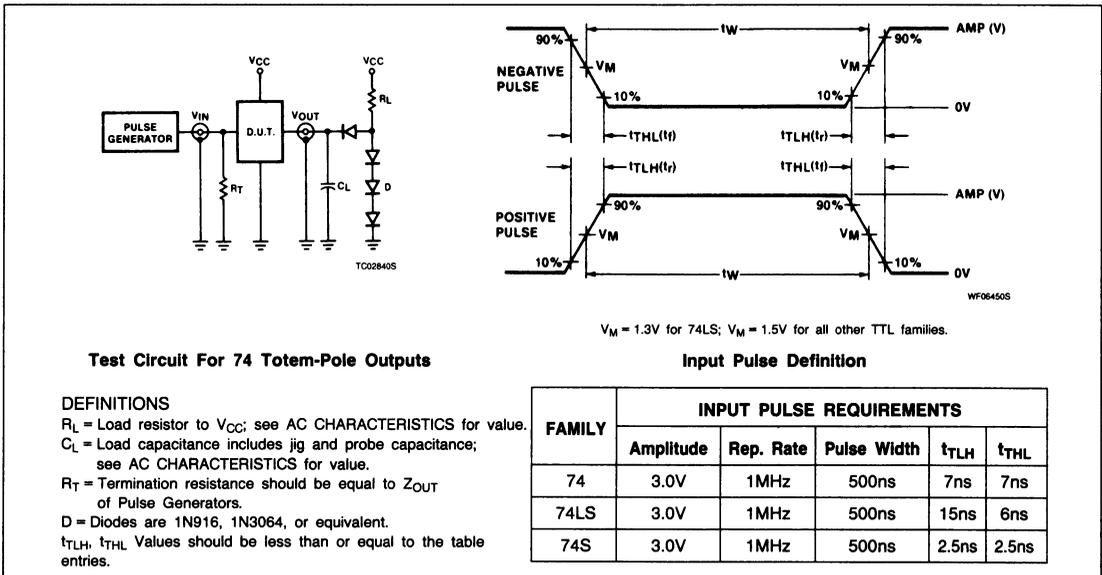
Flip-Flop

74LS378

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



74LS390 Counter

Dual Decade Ripple Counter
Product Specification

Logic Products

FEATURES

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two Master Resets to clear each decade counter individually

DESCRIPTION

The '390 is a dual 4-bit decade ripple counter divided into four separately clocked sections. The counter has two divide-by-two sections and two divide-by-five sections. These sections are normally used in a BCD decade or a bi-quinary configuration, since they share a common Master Reset input. If the two Master Resets can be used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS390	55MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS390N
Plastic SO-16	N74LS390D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

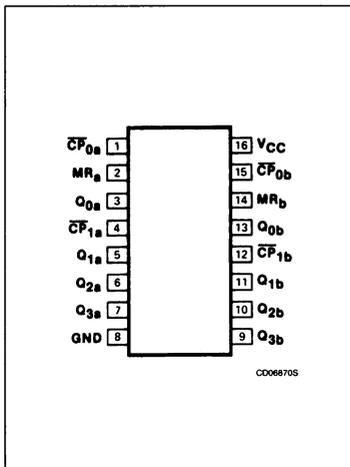
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
MR	Inputs	1LSul
CP ₀	Inputs	4LSul
CP ₁	Inputs	6LSul
All	Outputs	10LSul

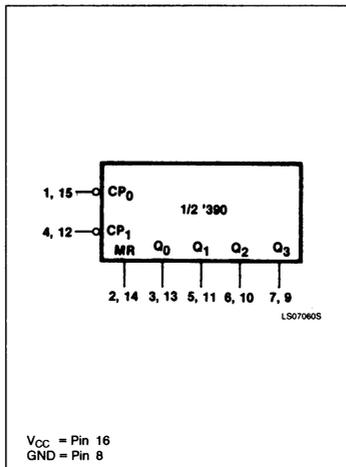
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

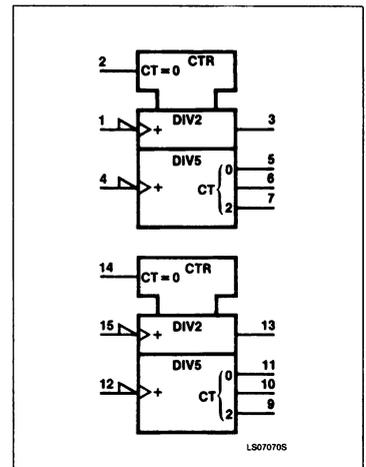
PIN CONFIGURATION



LOGIC SYMBOL



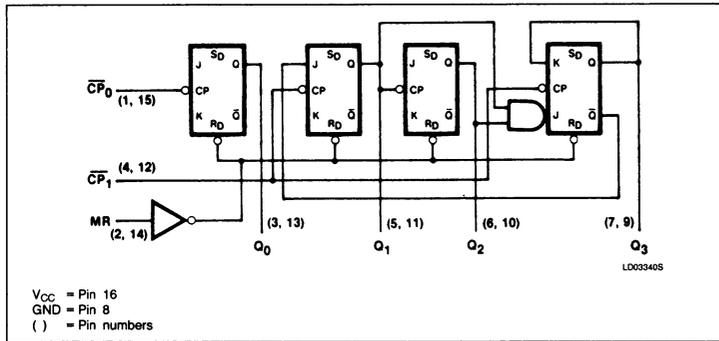
LOGIC SYMBOL (IEEE/IEC)



Counter

74LS390

LOGIC DIAGRAM



Each section is triggered by the HIGH-to-LOW transition of the Clock (\overline{CP}) inputs. For BCD decade operation, the Q_0 output is connected to the \overline{CP} input of the divide-by-five section. For bi-quinary decade operation (50% duty cycle output), the Q_3 output is connected to the CP_0 input, and Q_0 becomes the decade output.

The Master Resets (MR_a and MR_b) are active HIGH synchronous inputs to each decade counter which operate on the portion of the counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clocks and sets the four outputs LOW.

BCD COUNT SEQUENCE FOR 1/2 THE '390

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

H = HIGH voltage level
 L = LOW voltage level
NOTE:
 Output Q_0 is connected to input \overline{CP}_1 with Counter input on \overline{CP}_0 .

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE '390

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE:
 Output Q_3 is connected to input \overline{CP}_0 with Counter input on \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

NOTE:
 V_{IH} limited to 5.5V on \overline{CP}_0 and \overline{CP}_1 inputs.

Counter

74LS390

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μ A
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	$^{\circ}$ C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		74LS390			UNIT
				Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$		2.7	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.35	0.5	V
			$I_{OL} = 4\text{mA (74LS)}$		0.25	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_1 = I_{IK}$				-1.5	V
I_1	Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_1 = 7.0\text{V}$	MR inputs		0.1	mA
				\overline{CP}_0 inputs		0.2	mA
			$V_1 = 5.5\text{V}$	\overline{CP}_1 inputs		0.4	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_1 = 2.7\text{V}$	MR inputs		20	μ A	
			\overline{CP}_0 inputs		100	μ A	
			\overline{CP}_1 inputs		200	μ A	
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_1 = 0.4\text{V}$	MR inputs		-0.4	mA	
			\overline{CP}_0 inputs		-1.6	mA	
			\overline{CP}_1 inputs		-2.4	mA	
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-20		-100	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$			15	26	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with MR inputs grounded following momentary connection to 4.5V, all other inputs grounded and outputs open.

Counter

74LS390

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT	
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$			
		Min	Max		
f_{MAX}	$\overline{\text{CP}}_0$ input count frequency	Waveform 1	25		MHz
f_{MAX}	$\overline{\text{CP}}_1$ input count frequency	Waveform 1	12.5		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ to Q_0	Waveform 1		20 20	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ to Q_2	Waveform 1		60 60	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ to Q_1 or Q_3	Waveform 1		21 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ to Q_2	Waveform 1		39 39	ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		39	ns

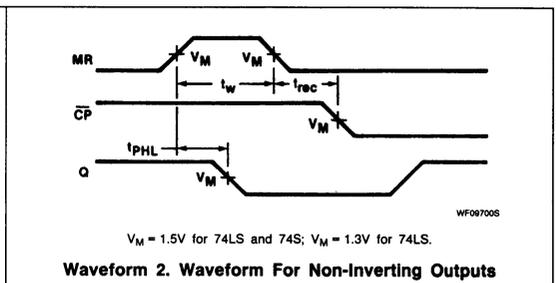
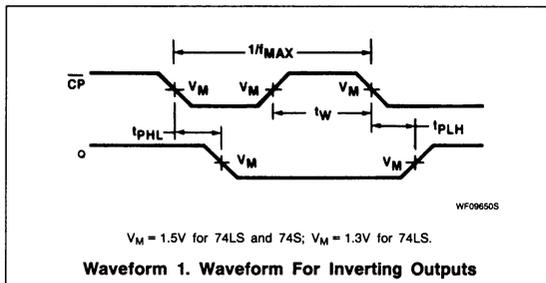
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT	
		Min	Max		
t_W	$\overline{\text{CP}}_0$ pulse width	Waveform 1	20		ns
t_W	$\overline{\text{CP}}_1$ pulse width	Waveform 1	40		ns
t_W	MR pulse width	Waveform 2	20		ns
t_{rec}	Recovery time, MR to $\overline{\text{CP}}$	Waveform 2	25		ns

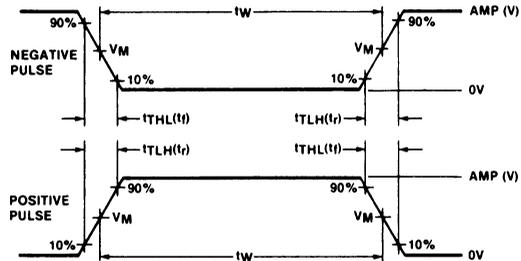
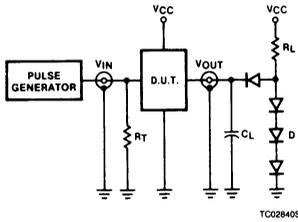
AC WAVEFORMS



Counter

74LS390

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS393 Counter

Dual 4-Bit Binary Ripple Counter
Product Specification

Logic Products

FEATURES

- Two 4-bit binary counters
- Divide-by any binary module up to 28 in one package
- Two Master Resets to clear each 4-bit counter individually

DESCRIPTION

The '393 is a Dual 4-bit Binary Ripple Counter with separate Clock and Master Reset inputs to each counter. The operation of each half of the '393 is the same as the '93 except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the Clock (\overline{CP}_a and \overline{CP}_b) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS393	35MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS393N
Plastic SO-14	N74LS393D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

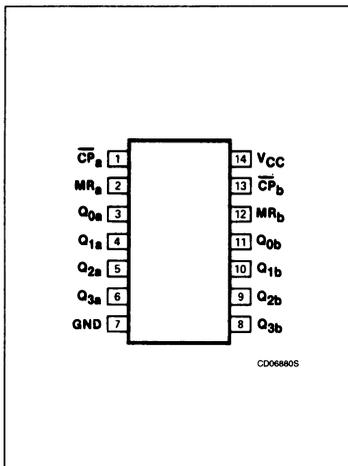
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
MR	Master Reset input	1LSul
\overline{CP}	Clock input	4LSul
Q	Output	10LSul

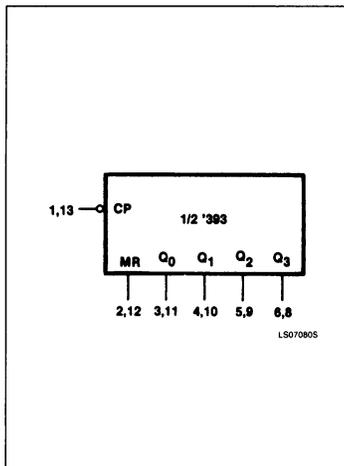
NOTE:

Where a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

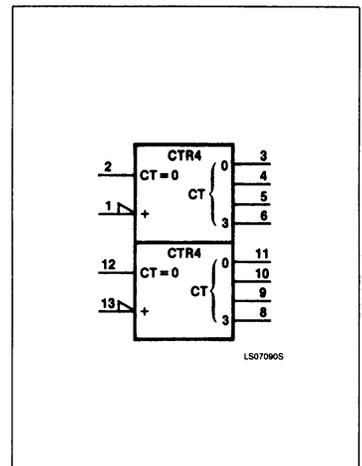
PIN CONFIGURATION



LOGIC SYMBOL



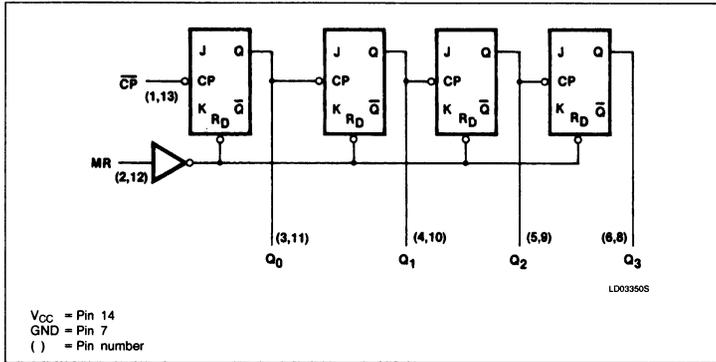
LOGIC SYMBOL (IEEE/IEC)



Counter

74LS393

LOGIC DIAGRAM



The Master Resets (MR_a and MR_b) are active-HIGH asynchronous inputs to each 4-bit counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clock and sets the outputs LOW.

COUNT SEQUENCE FOR 1/2 THE '393

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level
 L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	V
I_{IN} Input current	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to V_{CC}	V
T_A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			V
V_{IL} LOW-level input voltage			+0.8	V
I_{IK} Input clamp current			-18	mA
I_{OH} HIGH-level output current			-400	μA
I_{OL} LOW-level output current			8	mA
T_A Operating free-air temperature	0		70	°C

Counter

74LS393

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS393			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5	V
		I _{OL} = 4mA (74LS)		0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V	MR input		0.1	mA
		V _I = 5.5V	\overline{CP} input		0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	MR input			20	μ A
		\overline{CP} input			100	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	MR input			-0.4	mA
		\overline{CP} input			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		15	26	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with both MR inputs grounded following momentary connection to 4.5V, all other inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2k Ω		
		Min	Max	
f _{MAX} \overline{CP} input count frequency	Waveform 1	25		MHz
t _{PLH} t _{PHL} Propagation delay \overline{CP} to Q ₀	Waveform 1		20 20	ns
t _{PLH} t _{PHL} Propagation delay CP to Q ₃	Waveform 1		60 60	ns
t _{PHL} Propagation delay, MR to Q	Waveform 2		39	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

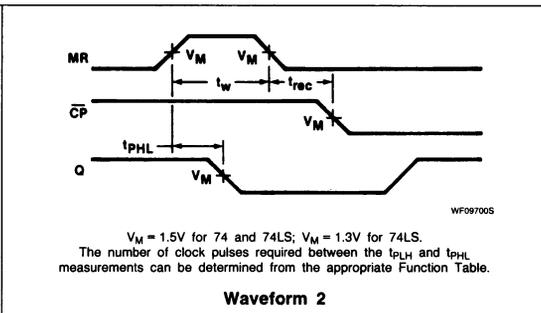
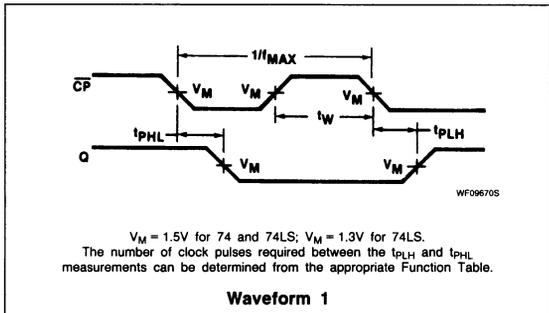
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t _w \overline{CP} pulse width	Waveform 1	20		ns
t _w MR pulse width	Waveform 2	20		ns
t _{rec} Recovery time, MR to \overline{CP}	Waveform 2	25		ns

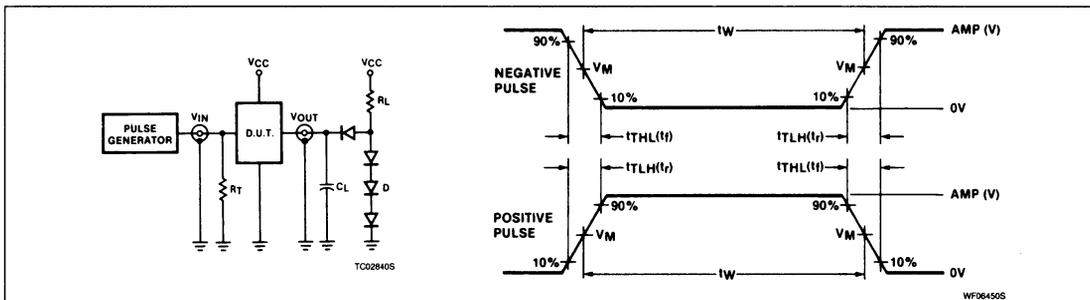
Counter

74LS393

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS395A Shift Register

4-Bit Cascadable Shift Register With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 4-bit parallel load shift register
- Independent 3-state buffer outputs
- Separate Q_3 output for serial expansion
- Asynchronous Master Reset

DESCRIPTION

The '395 is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs ($D_0 - D_3$) into the register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS395A	45MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS395AN

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
$Q_0 - Q_3$	Outputs	30LSul
Q_3	Output	10LSul

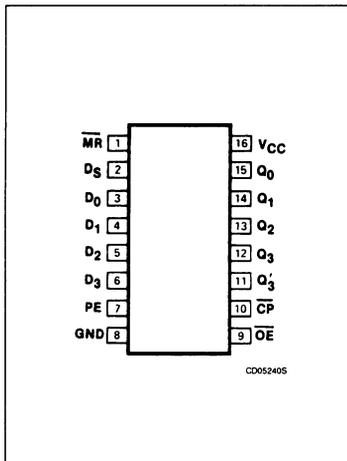
NOTE:

Where a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{L}$.

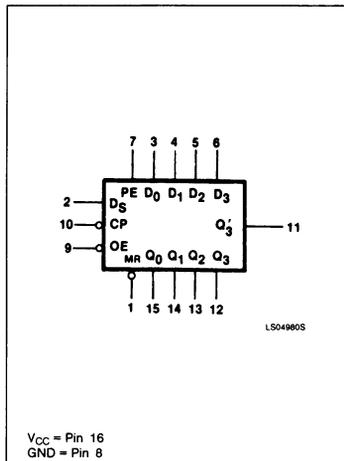
PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock.

The Master Reset (\overline{MR}) is an asynchronous active-LOW input. When LOW, the \overline{MR} overrides the clock and all other inputs and clears the register.

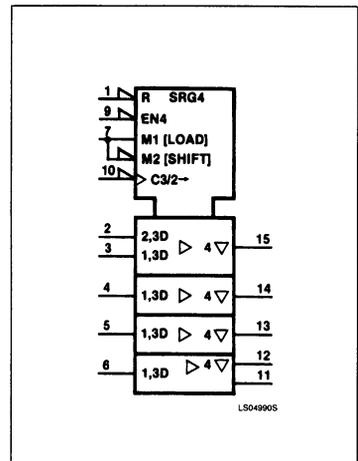
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Shift Register

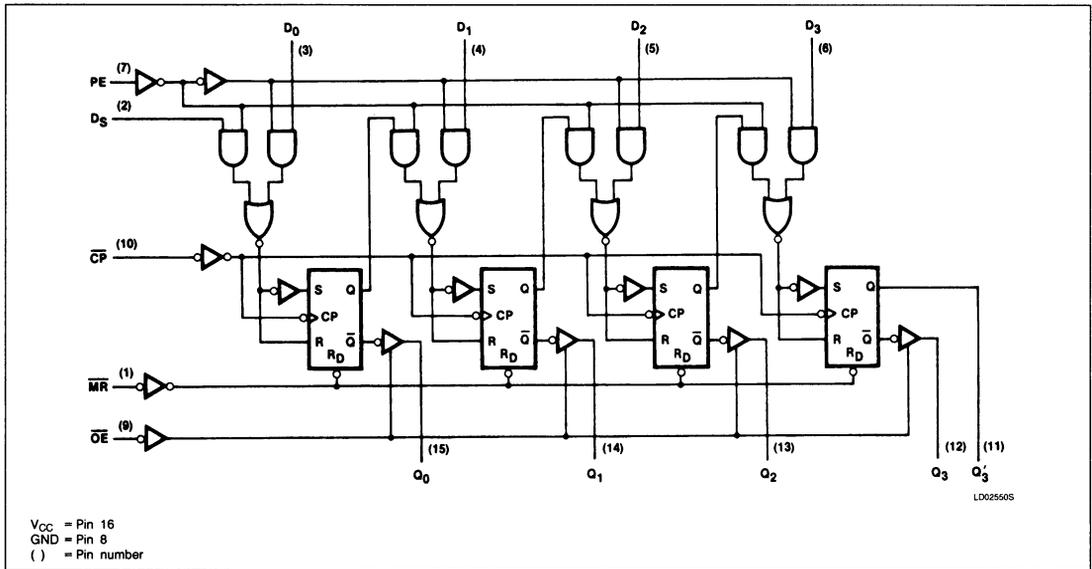
74LS395A

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The active-LOW Output Enable (\overline{OE}) controls all four 3-state buffers independent of the register operation. The

data in the register appears at the outputs when \overline{OE} is LOW. The outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus when \overline{OE} is HIGH. The output from the last stage is

brought out separately. This output (Q_3') is tied to the Serial Data input (D_5) of the next register for serial expansion applications. The Q_3 output is not affected by the 3-state buffer operation.

LOGIC DIAGRAM



FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS			
	MR	CP	PE	D _S	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q ₀	q ₁	q ₂
	H	↓	l	h	X	H	q ₀	q ₁	q ₂
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	\overline{OE}	Q _n (Register)	Q ₀ , Q ₁ , Q ₂ , Q ₃	Q ₃ '
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

- H = HIGH voltage level.
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition.
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition.
- q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW clock transition.
- X = Don't care.
- (Z) = HIGH impedance "off" state.
- ↓ = HIGH-to-LOW transition.

Shift Register

74LS395A

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current	Q ₃ '		-400	μA
		Q ₀ - Q ₃		-2.6	mA
I _{OL}	LOW-level output current	Q ₃ '		8	mA
		Q ₀ - Q ₃		24	mA
T _A	Operating free-air temperature	0		70	°C

Shift Register

74LS395A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS395A			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Q ₃	2.7	3.4	V	
		Q ₀ , Q ₁ , Q ₂ , Q ₃	2.4	3.1	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Q ₃	I _{OL} = MAX	0.35	0.5	V
			I _{OL} = 4mA (74LS)	0.25	0.4	V
		Q ₀ , Q ₁ , Q ₂ , Q ₃	I _{OL} = MAX	0.35	0.5	V
			I _{OL} = 12mA (74LS)	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MIN, V _{IH} = MIN, V _O = 2.7V	Q ₀ , Q ₁ , Q ₂ , Q ₃		20	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MIN, V _{IH} = MIN, V _O = 0.4V	Q ₀ , Q ₁ , Q ₂ , Q ₃		-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Q ₃	-20	-100	mA	
		Q ₀ , Q ₁ , Q ₂ , Q ₃	-30	-130	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1	19	34	mA	
		Condition 2	19	31	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with D_S and Master Reset at 4.5V. The Data inputs grounded and outputs open under the following conditions: *Condition 1*: \overline{OE} at 4.5V. A momentary 3V, then ground, applied to CP. *Condition 2*: Ground OE and CP inputs.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 45pF, R _L = 667Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	30		MHz
t _{PLH} Propagation delay	Waveform 1		30	ns
t _{PHL} Clock to buffer outputs			30	
t _{PLH} Propagation delay	Waveform 1, R _L = 2kΩ, C _L = 15pF		30	ns
t _{PHL} Clock to Q ₃ output			30	
t _{PHL} Propagation delay, \overline{MR} to output	Waveform 2		35	ns
t _{PZH} Enable time to HIGH level	Waveform 3		25	ns
t _{PZL} Enable time to LOW level	Waveform 4		25	ns
t _{PHZ} Disable time from HIGH level	Waveform 3, C _L = 5pF		17	ns
t _{PLZ} Disable time from LOW level	Waveform 4, C _L = 5pF		20	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

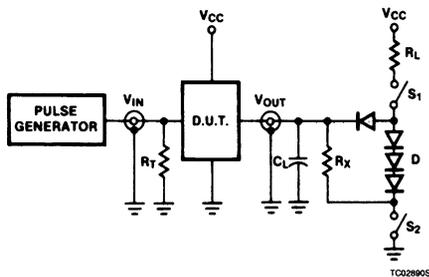
Shift Register

74LS395A

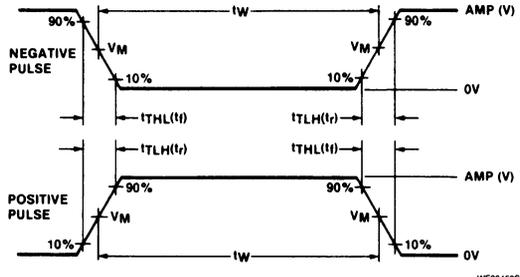
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W	Clock pulse width	Waveform 1	16	ns
t_W	Master Reset pulse width	Waveform 2	25	ns
t_s	Set-up time, data to clock	Waveform 5	20	ns
t_h	Hold time, data to clock	Waveform 5	10	ns
t_s	Set-up time, PE to clock	Waveform 5	40	ns
t_h	Hold time, PE to clock	Waveform 5	10	ns
t_{rec}	Recovery time, \overline{MR} to clock	Waveform 2	30	ns

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1\text{k}\Omega$ for 74, 74S, $R_X = 5\text{k}\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

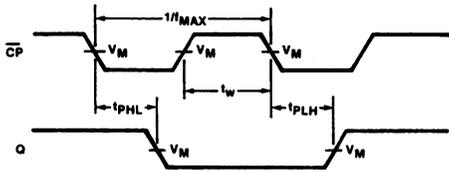
Q_3 is a standard totem-pole output.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Shift Register

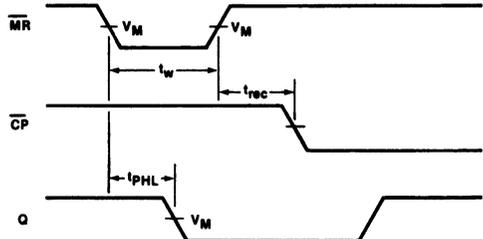
74LS395A

AC WAVEFORMS



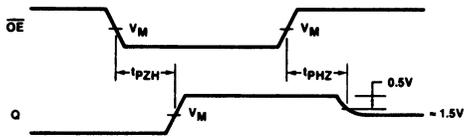
WF096905

Waveform 1. Clock To Output Delays And Clock Pulse Width



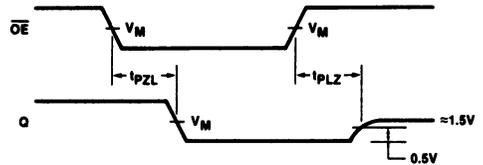
WF096905

Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



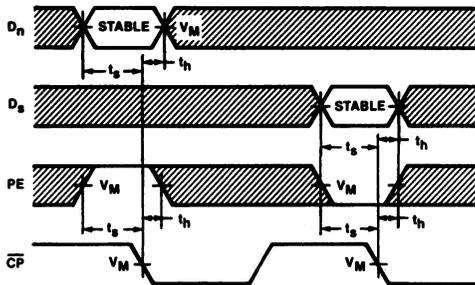
WF094005

Waveform 3. 3-State Enable Time To High Level And Disable Time From High Level



WF084305

Waveform 2. 3-State Enable Time To Low Level And Disable Time From Low Level



WF073205

For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Parallel Enable And Data Set-up And Hold Times

74LS445 Decoder/Driver

BCD-To-Decimal Decoder/Driver (Open Collector)
Product Specification

Logic Products

FEATURES

- 80mA output drive capability
- 7V output breakdown voltage
- See '45 for 30V output voltage
- See '42 for standard TTL outputs

DESCRIPTION

The '445 is a 1-of-10 decoder with open collector outputs. This decoder accepts BCD inputs on the A₀ to A₃ address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A₃ used as an active LOW enable.

The '445 features an output breakdown voltage of 7V. This device is ideal as a lamp or solenoid driver.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS445	39ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V ±5%; T _A = 0°C to +70°C
Plastic DIP	N74LS445N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

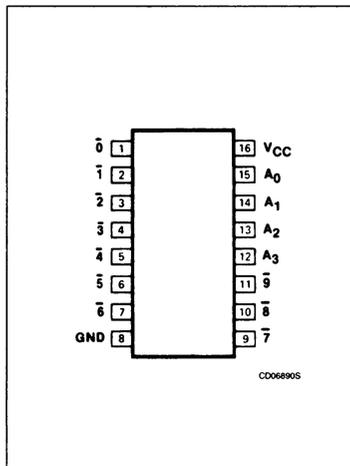
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

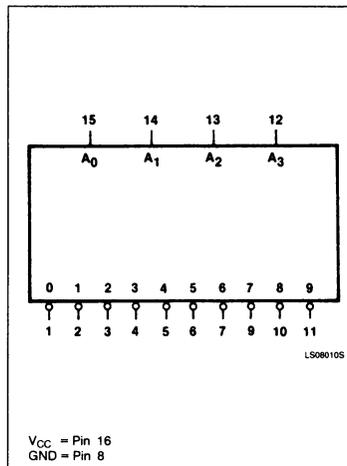
NOTE:

A 74LS unit load (LSul) is 20μA I_{IH} and -0.4mA I_{IL}.

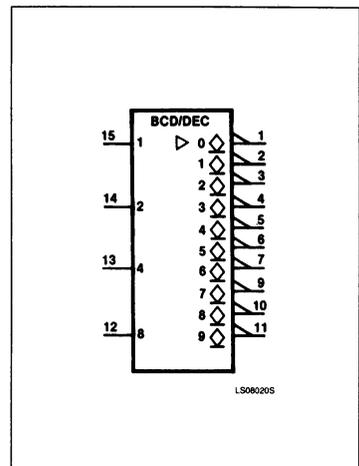
PIN CONFIGURATION



LOGIC SYMBOL



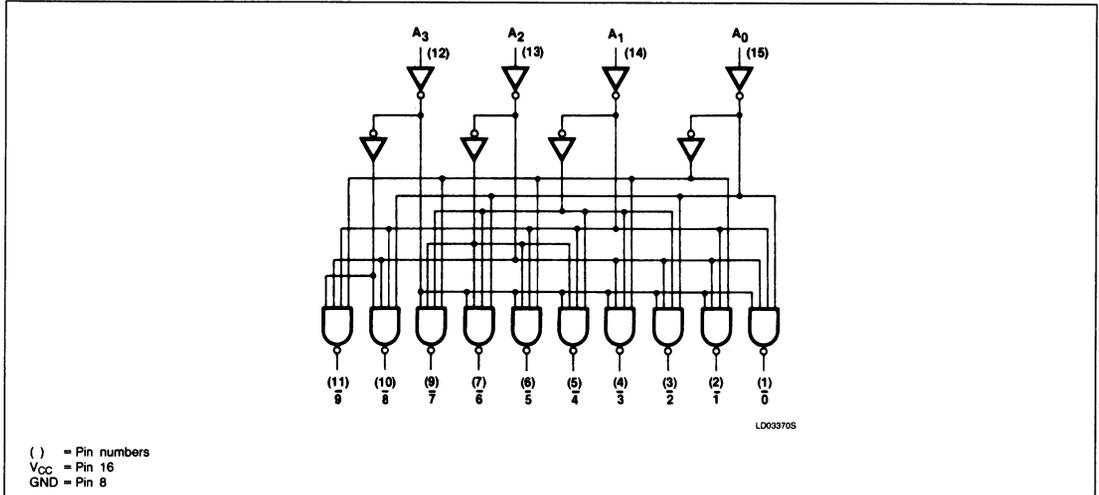
LOGIC SYMBOL (IEEE/IEC)



Decoder/Driver

74LS445

LOGIC DIAGRAM



FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
 L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

5

Decoder/Driver

74LS445

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
V _{OH} HIGH-level output voltage			7.0	V
I _{OL} LOW-level output current			24	mA
T _A Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS445			UNIT
		Min	Typ ²	Max	
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 7.0V			250	μA
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.35	0.5	V
		I _{OL} = 12mA (74LS)	0.25	0.4	V
		I _{OL} = 80mA (74LS)	1.6	3.0	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA
I _{CC} Supply current ³ (total)	V _{CC} = MAX		7	13	mA

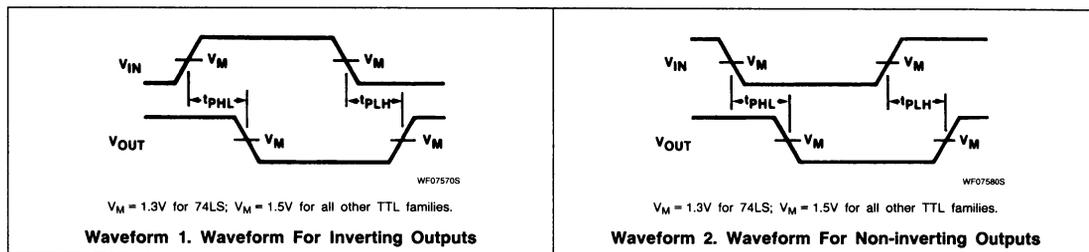
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Measure I_{CC} with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 45pF, R _L = 665Ω		
		Min	Max	
t _{PLH} t _{PHL}	Waveforms 1 & 2		50 50	ns

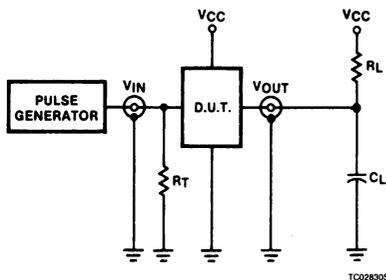
AC WAVEFORMS



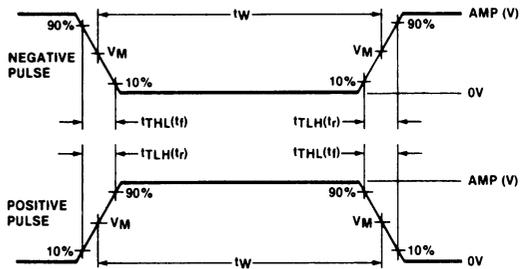
Decoder/Driver

74LS445

TEST CIRCUITS AND WAVEFORMS



TC028305



WF064505

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Open Collector Outputs

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS490 Counter

Dual BCD Decade Ripple Counter
Product Specification

Logic Products

FEATURES

- Two BCD decade counters
- Asynchronous Master Set (set-to-9)
- Asynchronous Master Reset (clear)

DESCRIPTION

The '490 is a Dual BCD Decade Ripple Counter with separate Clock, Master Set, and Master Reset inputs to each counter. The operation of each half of the '490 is the same as the '90 used in the BCD decade mode.

The counters are triggered by the HIGH-to-LOW transition of the Clock (\overline{CP}) inputs. No external connections are required to get the full BCD (8421) decade counting scheme from the counters. The counter outputs are internally connected as clocks or decoded inputs to succeeding stages. Since this is a ripple type counter, the outputs do not change synchronously and should not be used for high speed address decoding.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS490	55MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS490N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
\overline{CP}	Input	4LSul
MR, MS	Inputs	1LSul
$Q_0 - Q_3$	Outputs	10LSul

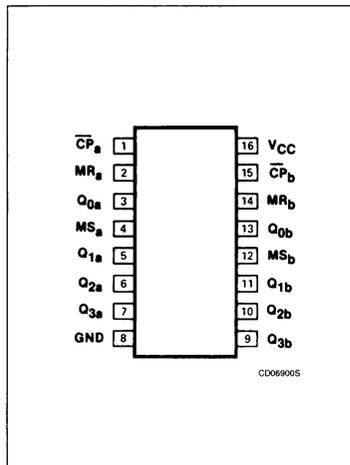
NOTE:

Where a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

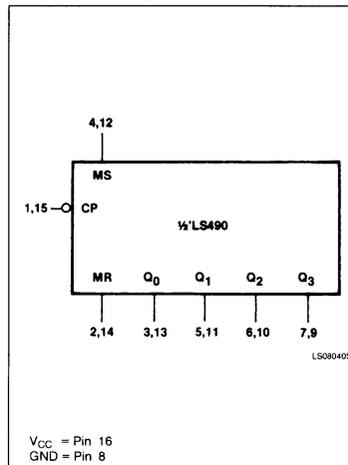
The Master Set (MS) and Master Reset (MR) are asynchronous active-HIGH inputs. The HIGH MR input overrides the clock and clears the associated 4 bits of

the counter. The HIGH MS input overrides the clock and MR inputs and sets the associated 4 bits to nine (HLLH).

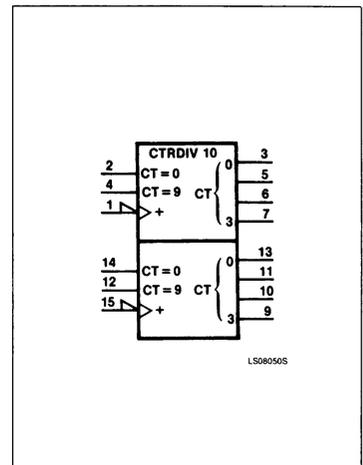
PIN CONFIGURATION



LOGIC SYMBOL



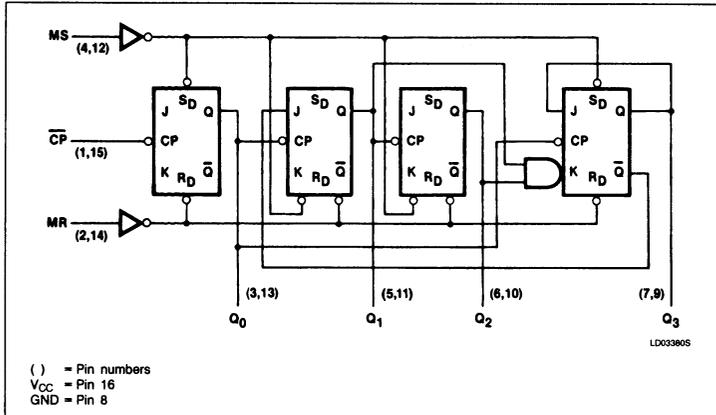
LOGIC SYMBOL (IEEE/IEC)



Counter

74LS490

LOGIC DIAGRAM



MODE SELECTION — FUNCTION TABLE FOR 1/2 THE '490

RESET/SET INPUTS		OUTPUTS			
MR	MS	Q ₀	Q ₁	Q ₂	Q ₃
H	L	L	L	L	L
L	H	H	L	L	H
L	L	Count			

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

BCD COUNT SEQUENCE FOR 1/2 THE '490

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE:
 Output Q₀ connected to input CP₁.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
I _{OH} HIGH-level output current			-400	μA
I _{OL} LOW-level output current			8	mA
T _A Operating free-air temperature	0		70	°C

Counter

74LS490

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS490			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5	V
		I _{OL} = 4mA (74LS)		0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V	MR, MS inputs		0.1	mA
		V _I = 5.5V	\overline{CP} input		0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	MR, MS inputs			20	μ A
		\overline{CP} input			100	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	MR, MS inputs			-0.4	mA
		\overline{CP} input			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		15	26	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all outputs open, MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2k Ω		
		Min	Max	
f _{MAX} \overline{CP} input count frequency	Waveform 1	35		MHz
t _{PLH} t _{PHL} Propagation delay \overline{CP} to Q ₀	Waveform 1		20 20	ns
t _{PLH} t _{PHL} Propagation delay \overline{CP} to Q ₁ or Q ₃	Waveform 1		39 39	ns
t _{PLH} t _{PHL} Propagation delay \overline{CP} to Q ₂	Waveform 1		54 54	ns
t _{PHL} Propagation delay, MR to Q	Waveform 2		39	ns
t _{PLH} t _{PHL} Propagation delay MS to Q	Waveforms 2 & 3		39 36	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

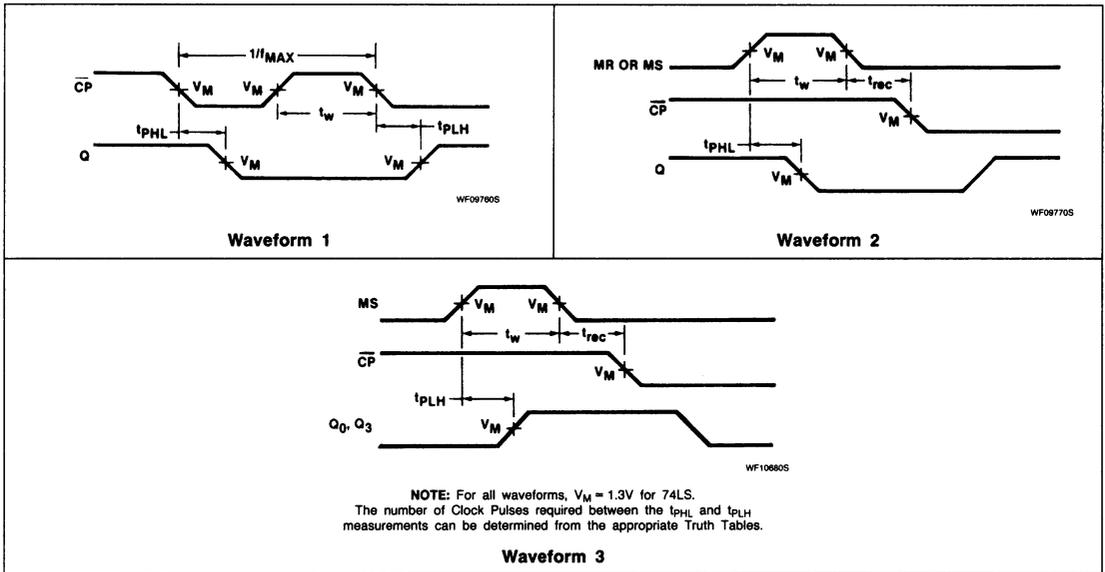
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t _W \overline{CP} pulse width	Waveform 1	20		ns
t _W MR pulse width	Waveform 2	20		ns
t _W MS pulse width	Waveforms 2 & 3	20		ns
t _{rec} Recovery time, MR to \overline{CP}	Waveform 2	25		ns
t _{rec} Recovery time, MS to \overline{CP}	Waveforms 2 & 3	25		ns

Counter

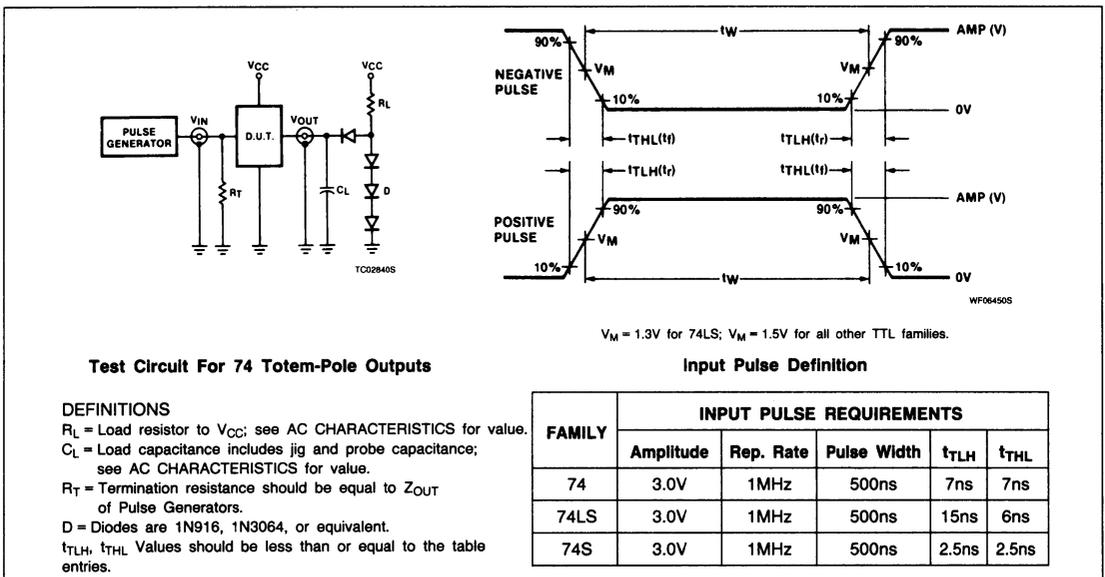
74LS490

AC WAVEFORMS



5

TEST CIRCUITS AND WAVEFORMS



74S534 Flip-Flop

Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 8-bit positive, edge-triggered register
- Inverting outputs
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION

The '534 is an 8-bit, edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's \overline{Q} output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S534	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S534N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
All	Outputs	10Sul

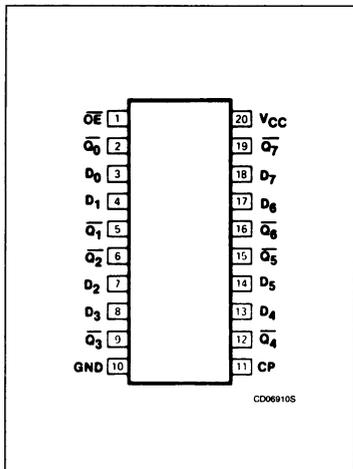
NOTE:

Where a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

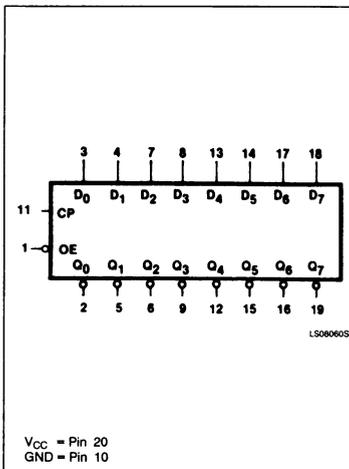
The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation.

When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

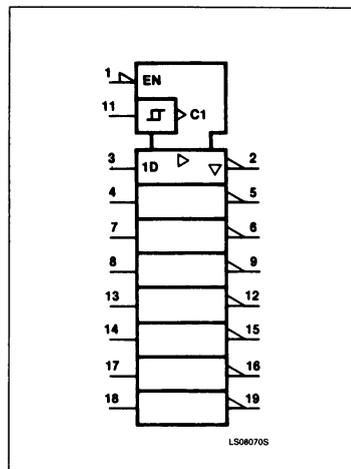
PIN CONFIGURATION



LOGIC SYMBOL



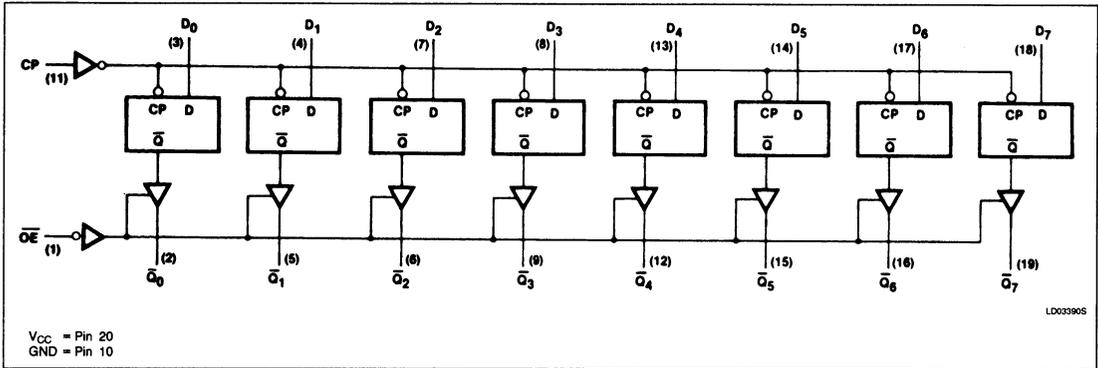
LOGIC SYMBOL (IEEE/IEC)



Flip-Flop

74S534

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		$Q_0 - Q_7$
Load and read register	L	\uparrow	l	L	H
	L	\uparrow	h	H	L
Load register and disable outputs	H	\uparrow	l	L	(Z)
	H	\uparrow	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one Set-up time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one Set-up time prior to the LOW-to-HIGH clock transition
 (Z) = HIGH impedance "off" state
 \uparrow = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74S			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-6.5	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	$^{\circ}C$

5

Flip-Flop

74S534

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74S534			UNIT	
			Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.1		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX				0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.4V			50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.5V			-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.5V			-0.25	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCL}	All inputs grounded		102	140	mA
		I _{CCZ}	CP, \overline{OE} = 4.5V D inputs = GND		131	180	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 3	75		MHz
t _{PLH} Propagation delay	Waveform 3		15	ns
t _{PHL} Clock to output			17	
t _{PZH} Enable time to HIGH level	Waveform 1		15	ns
t _{PZL} Enable time to LOW level	Waveform 2		18	ns
t _{PHZ} Disable time from HIGH level	Waveform 1, C _L = 5pF		9	ns
t _{PLZ} Disable time from LOW level	Waveform 2, C _L = 5pF		12	ns

AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74S		UNIT
		Min	Max	
t _{w(H)} Clock pulse width	Waveform 3	6		ns
t _{w(L)}		7.3		
t _S Set-up time, data to clock	Waveform 4	5		ns
t _H Hold time, data to clock	Waveform 4	2		ns

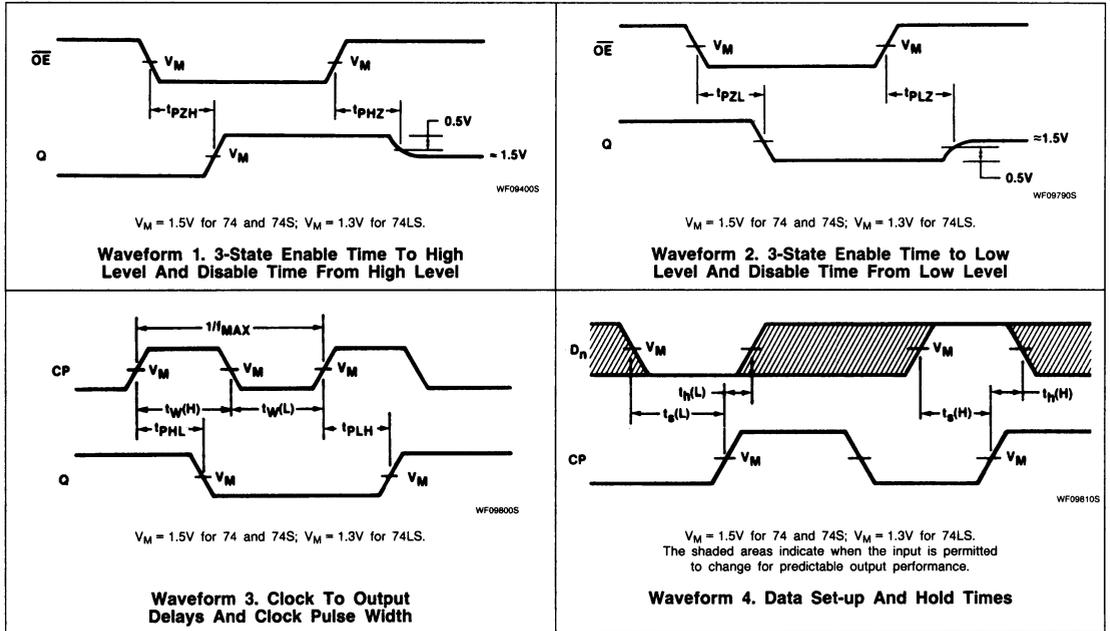
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Flip-Flop

74S534

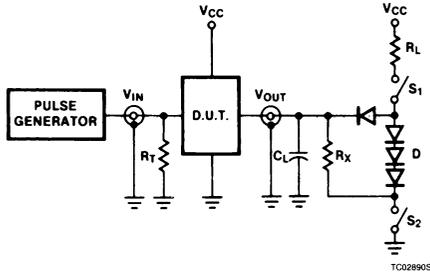
AC WAVEFORMS



Flip-Flop

74S534

TEST CIRCUITS AND WAVEFORMS



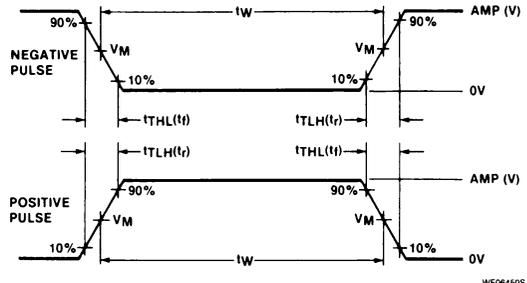
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- R_X = $1k\Omega$ for 74, 74S, R_X = $5k\Omega$ for 74LS.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS540, 74LS541

Buffers/Drivers

Octal Buffer/Line Driver (3-State)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS540	9ns	22mA
74LS541	10ns	23mA

FUNCTION TABLE

INPUTS			OUTPUTS	
\overline{OE}_1	\overline{OE}_2	I	Y	\overline{Y}
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS540N, N74LS541N
Plastic SOL-20	N74LS540D, N74LS541D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

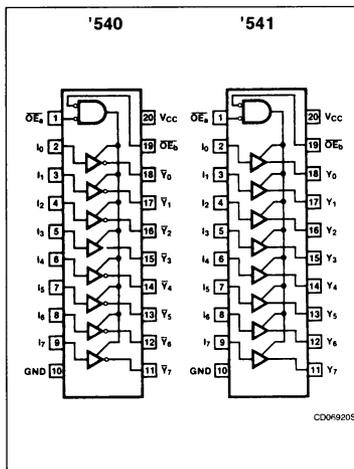
PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE:

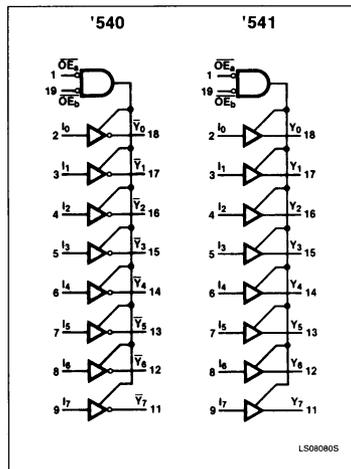
A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

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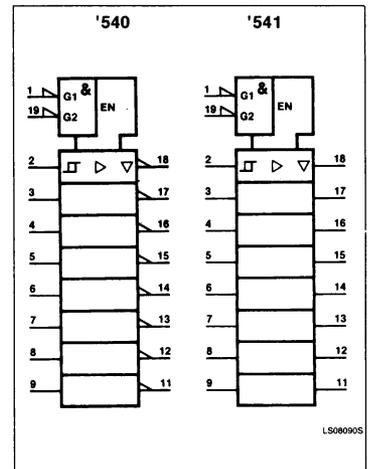
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Buffers/Drivers

74LS540, 74LS541

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-15	mA
I _{OL}	LOW-level output current			24	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS540, 541			UNIT	
		Min	Typ ²	Max		
ΔV _T	Hysteresis (V _{T+} - V _{T-})	V _{CC} = MIN	0.2	0.4	V	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = 0.5V, I _{OH} = MAX	2.0		V	
		V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = -3mA	2.4	3.4	V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		0.35	0.5	V
		I _{OL} = MAX I _{OL} = 12mA (74LS)		0.25	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _{ozH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.7V			20	μA
I _{ozL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.4V			-20	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.2	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-40		-130	mA
I _{CC}	Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH	16	25	mA
			I _{CC} L Outputs LOW	27	45	mA
			I _{CC} Z Outputs OFF	31	52	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

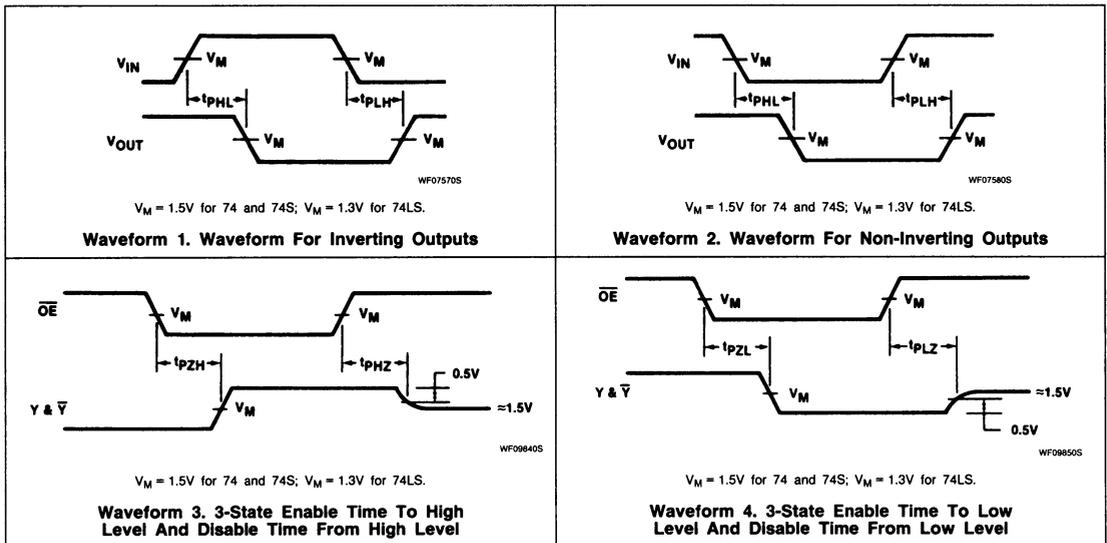
Buffers/Drivers

74LS540, 74LS541

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS540		74LS541		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveforms 1 & 2		15 15		15 18	ns
t_{PZH} Output enable time to HIGH level	Waveform 3		25		32	ns
t_{PZL} Output enable time to LOW level	Waveform 4		38		38	ns
t_{PHZ} Output disable time from HIGH level	Waveform 3, $C_L = 5\text{pF}$		18		18	ns
t_{PLZ} Output disable time from LOW level	Waveform 4, $C_L = 5\text{pF}$		25		29	ns

AC WAVEFORMS

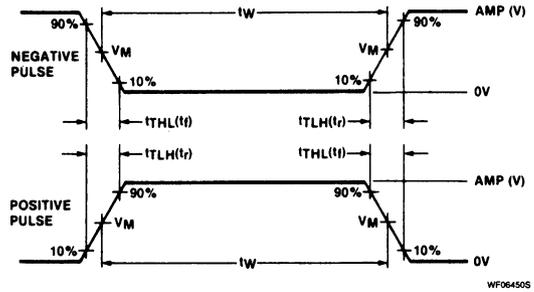
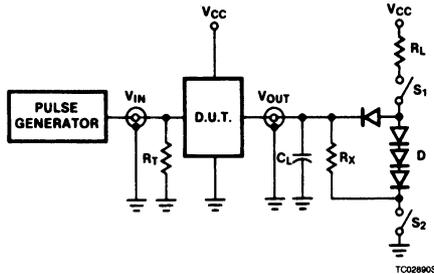


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Buffers/Drivers

74LS540, 74LS541

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS568A, 569A 3-State Bidirectional Counters

'568A BCD Decade Up/Down Synchronous Counter (3-State)
'569A 4-Bit Binary Up/Down Synchronous Counter (3-State)
Product Specification

Logic Products

FEATURES

- Speed improved over LS568/LS569
- Synchronous counting and loading
- UP/DOWN counting
- BCD decade counter - '568A
- Modulo 16 binary counter - '569A
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous Master Reset
- 3-State Counter outputs
- Gated Carry output

DESCRIPTION

The '568A and '569A are synchronous presettable UP/DOWN counters featuring an internal carry look-ahead for applications in high speed counting designs.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coin-

TYPE	TYPICAL f_{Max}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS568A	35MHz	28mA
74LS569A	35MHz	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS568AN, N74LS569AN

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
$Q_0 - Q_3$	Outputs	30LSul
\overline{TC} , GC	Outputs	10LSul

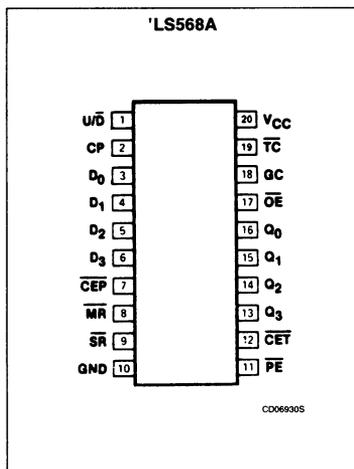
NOTE:

A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

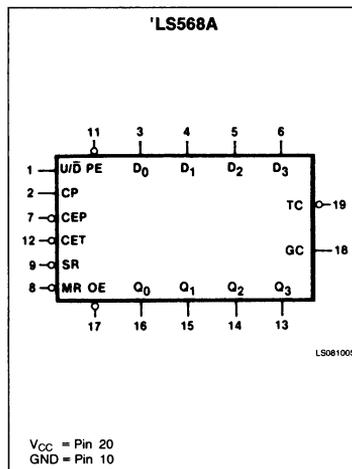
cident with each other when so instructed by the Count-Enable inputs and internal gating. This mode of operation eliminates the output spikes which are nor-

mally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the Clock.

PIN CONFIGURATION

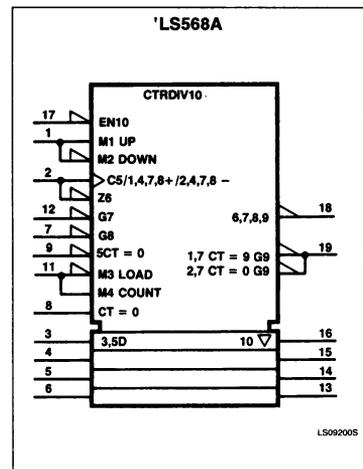


LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)

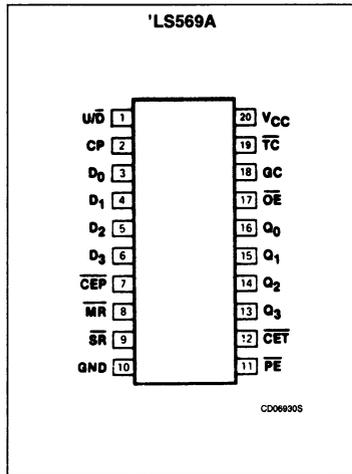


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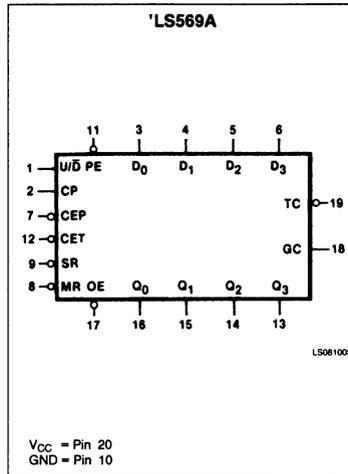
3-State Bidirectional Counters

74LS568A, 569A

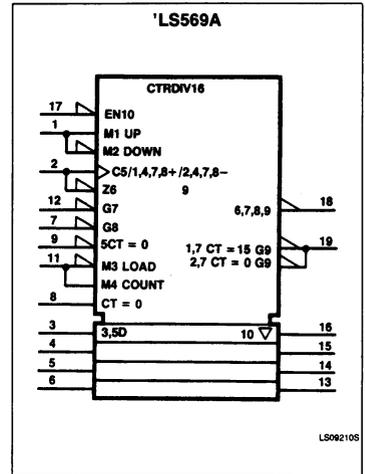
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the Clock, and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the Clock. The Synchronous Reset (\overline{SR}), when LOW one set-up time before the LOW-to-HIGH transition of the Clock, overrides the \overline{CEP} , \overline{CET} and \overline{PE} inputs, and causes the flip-flops to go LOW coincident with the positive Clock transition.

The Master Reset (\overline{MR}) is an asynchronous overriding clear function which forces all stages to a LOW state while the \overline{MR} input is LOW without regard to the Clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (\overline{CET} , \overline{CEP}) and a Terminal Count (\overline{TC}) output. Both Count Enable inputs must be LOW to count. The \overline{CET} input is fed forward to enable the \overline{TC} output. The \overline{TC} output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level \overline{TC} pulse is used to enable successive cascaded stages. See Figure A in '168/'169 data sheet for the fast synchronous multistage counting connections.

The Gated Clock output (GC) is a Terminal Count output which provides a HIGH-LOW-

HIGH pulse for a duration equal to the LOW time of the Clock pulse when \overline{TC} is LOW. The GC output can be used as a Clock input for the next stage in a simple ripple expansion scheme.

The direction of counting is controlled by the UP/DOWN (U/\overline{D}) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The active LOW Output Enable (\overline{OE}) input controls the 3-State buffer outputs independent of the counter operation. When \overline{OE} is LOW, the count appears at the buffer outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

3-State Bidirectional Counters

74LS568A, 569A

MODE SELECT — FUNCTION TABLE

COUNTER OPERATING MODES	INPUTS								COUNTER STATES			
	MR	CP	SR	U/D	PE	CEP	CET	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Asynchronous reset	L	X	X	X	X	X	X	X	L	L	L	L
Synchronous reset	H	↑	l	X	X	X	X	X	L	L	L	L
Parallel load	H	↑	h	X	l	X	X	l	L	L	L	L
	H	↑	h	X	l	X	X	h	H	H	H	H
Count up	H	↑	h	h	l	l	l	X	count up			
Count down	H	↑	h	l	h	l	l	X	count down			
Hold (do nothing)	H	↑	h	X	h	h	X	X	no change			
	H	↑	h	X	h	X	h	X	no change			

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q _n -Counter	Q ₀ , Q ₁ , Q ₂ , Q ₃
Read counter	L	L	L
	L	H	H
Disable outputs	H	L	(Z)
	H	H	(Z)

TERMINAL COUNT FUNCTION TABLE, '568A

INPUTS				COUNTER STATES				OUTPUTS	
CP	U/D	CEP	CET	Q ₀	Q ₁	Q ₂	Q ₃	TC	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	X	X	H	L	H
L	H	L	L	H	X	X	H	L	L
X	H	H	L	H	X	X	H	L	H
X	H	X	H	H	X	X	H	H	H

TERMINAL COUNT FUNCTION TABLE, '569A

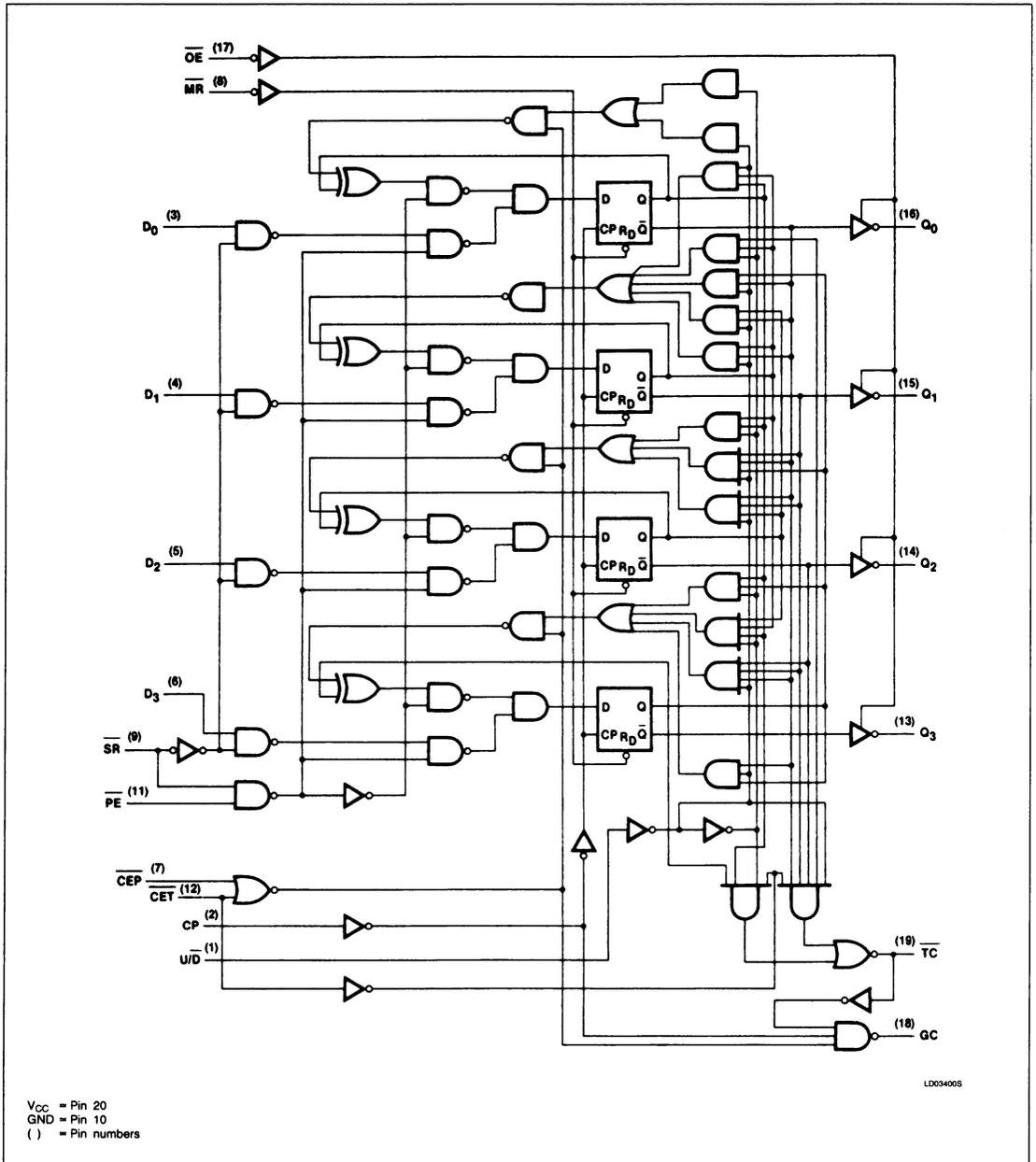
INPUTS				COUNTER STATES				OUTPUTS	
CP	U/D	CEP	CET	Q ₀	Q ₁	Q ₂	Q ₃	TC	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	L	L
X	H	H	L	H	H	H	H	L	H
X	H	X	H	H	H	H	H	H	H

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

3-State Bidirectional Counters

74LS568A, 569A

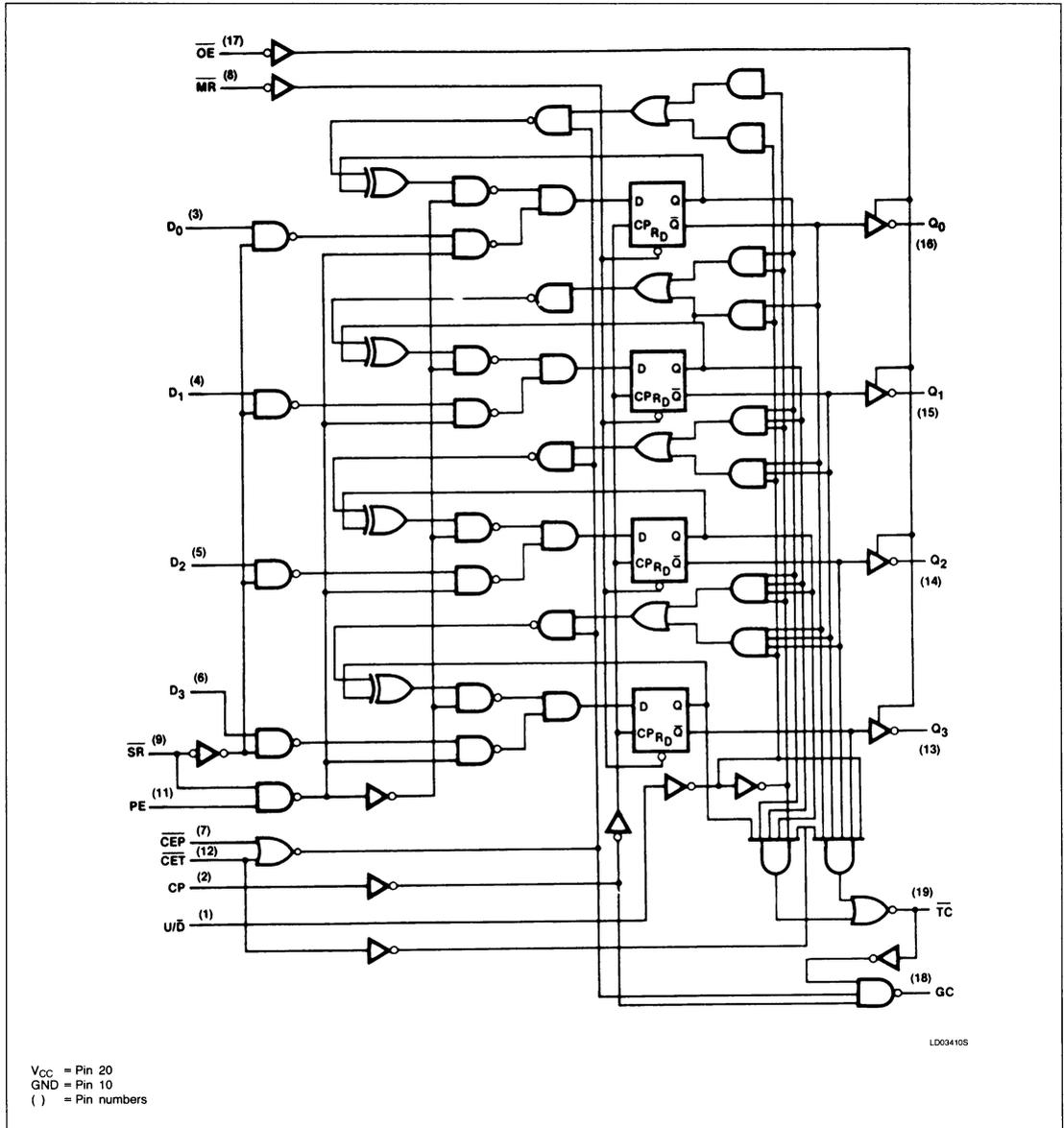
LOGIC DIAGRAM, '568A



3-State Bidirectional Counters

74LS568A, 569A

LOGIC DIAGRAM, '569A



3-State Bidirectional Counters

74LS568A, 569A

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-2.6	mA
				\overline{TC}, GC	-400
I _{OL}	LOW-level output current			24	mA
				\overline{TC}, GC	8
T _A	Operating free-air temperature	0		70	°C

3-State Bidirectional Counters

74LS568A, 569A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74LS568, 569			UNIT	
			Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Q ₀ - Q ₃	I _{OH} = MAX	2.4		V	
		\overline{TC} , GC	I _{OH} = MAX	2.4		V	
LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Q ₀ - Q ₃	I _{OL} = MAX		0.5	V	
			I _{OL} = 12mA (74LS)		0.5	V	
		\overline{TC} , GC	I _{OL} = MAX		0.5	V	
			I _{OL} = 4mA (74LS)		0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.7V				20	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.4V				-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Q ₀ - Q ₃		-30		-100	mA
		\overline{TC} , GC		-15		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX			28	43	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

3-State Bidirectional Counters

74LS568A, 569A

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		15 20	ns
t_{PLH} Propagation delay t_{PHL} Clock to $\overline{\text{TC}}$	Waveform 2		20 25	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CET}}$ to $\overline{\text{TC}}$	Waveform 3		14 15	ns
t_{PLH} Propagation delay t_{PHL} U/ $\overline{\text{D}}$ control to $\overline{\text{TC}}$	Waveform 4		20 25	ns
t_{PLH} Propagation delay t_{PHL} Clock to GC	Waveform 2		15 17	ns
t_{PLH} Propagation delay t_{PHL} CET or CEP to GC	Waveform 2		16 26	ns
t_{PHL} Propagation delay $\overline{\text{MR}}$ to output	Waveform 5		20	ns
t_{PZH} Output enable to HIGH level	Waveform 6		15	ns
t_{PZL} Output enable to LOW level	Waveform 7		15	ns
t_{PHZ} Output disable from HIGH level	Waveform 6, $C_L = 5\text{pF}$		20	ns
t_{PLZ} Output disable from LOW level	Waveform 7, $C_L = 5\text{pF}$		22	ns

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{\text{OUT}} = +0.5\text{V}$ and $V_{CC} = V_{CC \text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

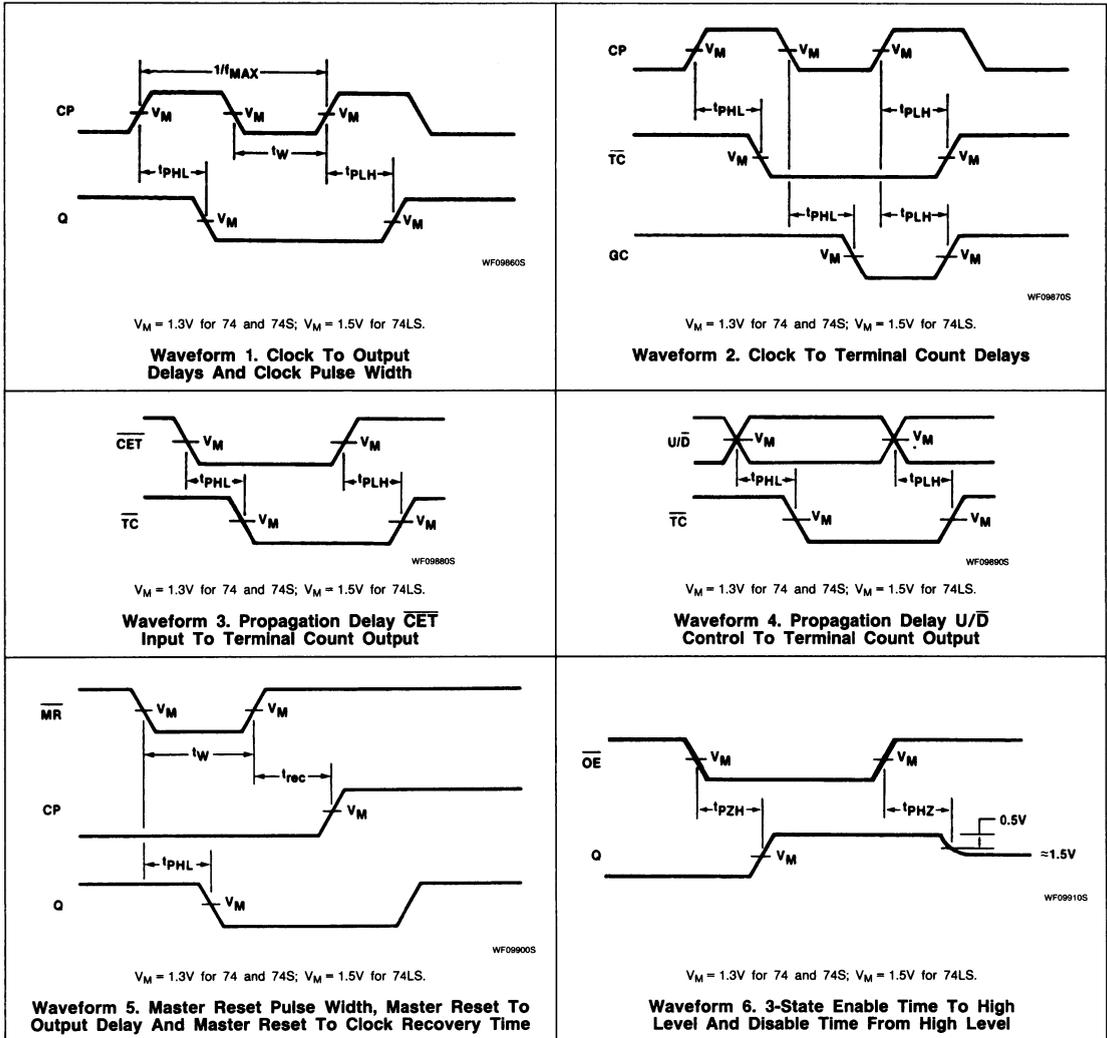
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t_W Clock pulse width	Waveform 1	20		ns
t_S Set-up time data to clock	Waveform 8	20		ns
t_H Hold time data to clock	Waveform 8	0		ns
t_S Set-up time $\overline{\text{PE}}$ to clock	Waveform 8	25		ns
t_H Hold time $\overline{\text{PE}}$ to clock	Waveform 8	0		ns
t_S Set-up time $\overline{\text{CEP}}$ & $\overline{\text{CET}}$ to clock	Waveform 9	20		ns
t_H Hold time $\overline{\text{CEP}}$ & $\overline{\text{CET}}$ to clock	Waveform 9	0		ns
t_S Set-up time U/ $\overline{\text{D}}$ to clock	Waveform 10	30		ns
t_H Hold time U/ $\overline{\text{D}}$ to clock	Waveform 10	0		ns
t_S Set-up time $\overline{\text{SR}}$ to clock	Waveform 11	30		ns
t_H Hold time $\overline{\text{SR}}$ to clock	Waveform 11	0		ns
t_{rec} Recovery time $\overline{\text{MR}}$ to clock	Waveform 5	20		ns

3-State Bidirectional Counters

74LS568A, 569A

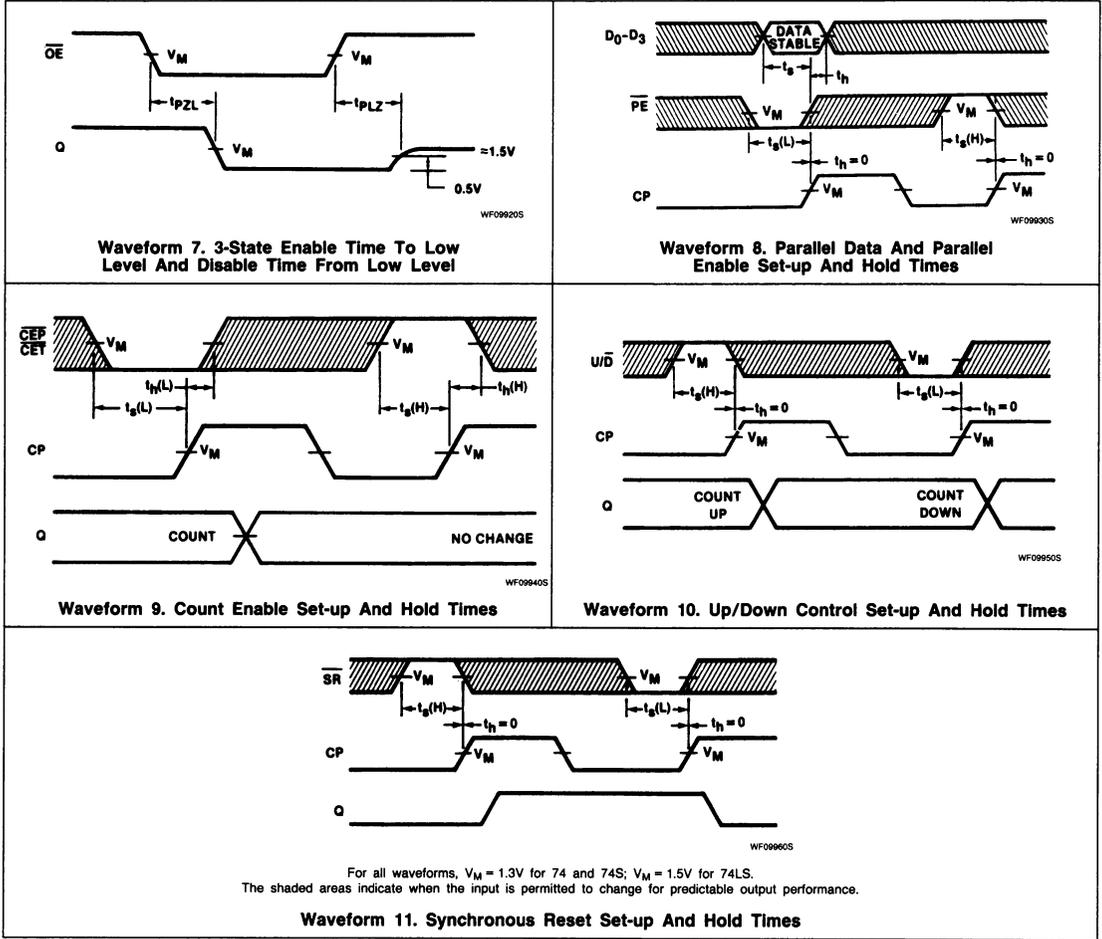
AC WAVEFORMS



3-State Bidirectional Counters

74LS568A, 569A

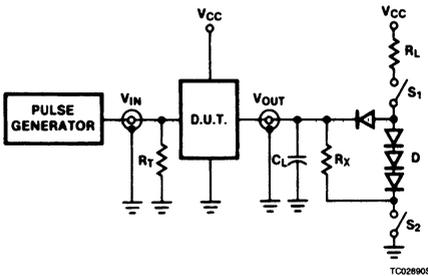
AC WAVEFORMS (Continued)



3-State Bidirectional Counters

74LS568A, 569A

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

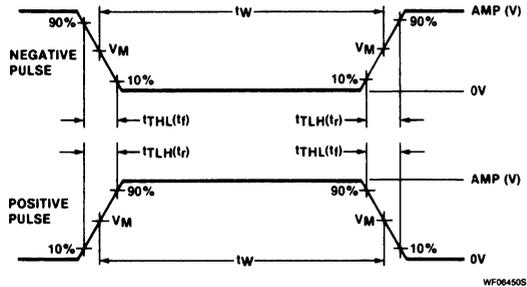
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS620, LS623 Transceivers

'LS620 Inverting Octal Bus Transceiver (3-State)
'LS623 Non-Inverting Octal Bus Transceiver (3-State)
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs
 - LS620, inverting
 - LS623, non-inverting
- Hysteresis on all Data inputs
- PNP inputs for reduced loading

DESCRIPTION

The 'LS623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The LS620 is an inverting version of the 'LS623. Both have built-in hysteresis to minimize ac noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS620	9ns	73.6mA
74LS623	9ns	73.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS620N, N74LS623N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

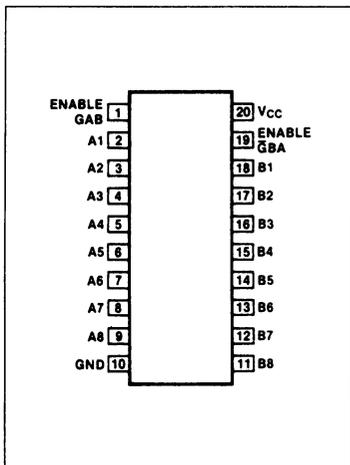
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

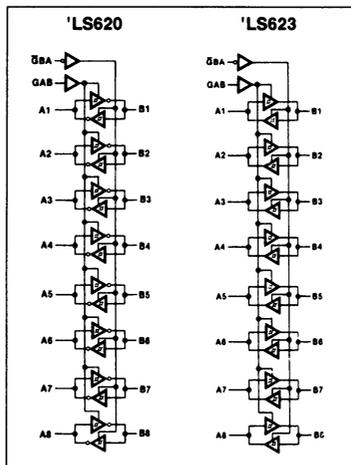
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

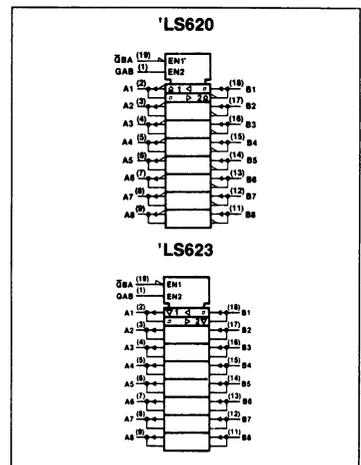
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceivers

74LS620, LS623

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
		'LS620	'LS623
$\bar{G}BA$	GAB		
L	L	\bar{B} data to A bus	B data to A bus
H	H	\bar{A} data to B bus	A data to B bus
H	L	(Z)	(Z)
L	H	\bar{B} data to A bus, \bar{A} data to B bus	B data to A bus, A data to B bus

H = HIGH voltage level

L = LOW voltage level

(Z) = HIGH impedance (off) state.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\bar{G}BA$ and GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620 and 'LS623 the capability to store data by simultaneous enabling of $\bar{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

NOTE:

 V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.6	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-15	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

Transceivers

74LS620, LS623

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS620, 74LS623			UNIT	
		Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input	0.2			V	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$	2.0		V	
		$I_{OH} = -3\text{mA}$	2.4	3.4	V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12\text{mA}$		0.25	0.4	V
		$I_{OL} = 24\text{mA}$ (74LS)		0.35	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5	V	
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, \bar{G} input = 2.0V, $V_O = 2.7\text{V}$			20	μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, \bar{G} input = 2.0V, $V_O = 0.4\text{V}$			-400	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ A or B input			0.1	mA
		$V_I = 7.0\text{V}$, \bar{G} BA or GAB input			0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$			20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$			-0.4	mA	
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$	-40		-130	mA	
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		63	70	mA
		I_{CCL} Outputs LOW		74	90	mA
		I_{CCZ} Outputs OFF		84	95	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with outputs open.

Transceivers

74LS620, LS623

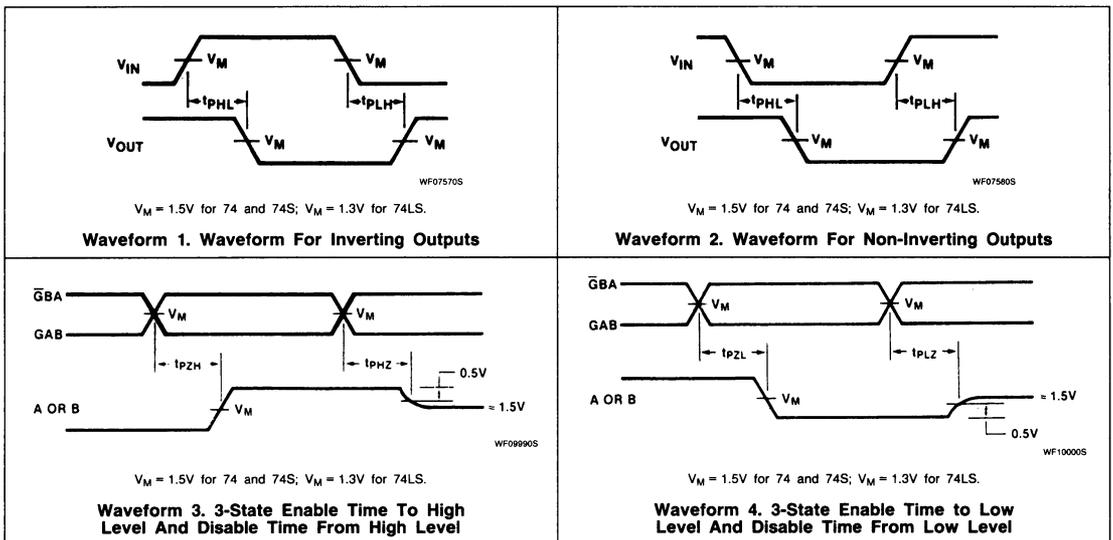
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS620		74LS623		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 1, '620 Waveform 2, '623	10 15		15 15	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 1, '620 Waveform 2, '623	10 15		15 15	ns
t_{PZH}	Enable to HIGH $\bar{G}BA$ input to A output	Waveform 3	40		40	ns
t_{PZH}	Enable to HIGH GAB input to B output	Waveform 3	40		40	ns
t_{PZL}	Enable to LOW $\bar{G}BA$ input to A output	Waveform 4	40		40	ns
t_{PZL}	Enable to LOW GAB input to B output	Waveform 4	40		40	ns
t_{PHZ}	Disable from HIGH $\bar{G}AB$ input to A output	Waveform 3, $C_L = 5\text{pF}$	25		25	ns
t_{PHZ}	Disable from HIGH GAB input to B output	Waveform 3, $C_L = 5\text{pF}$	25		25	ns
t_{PLZ}	Disable from LOW $\bar{G}BA$ input to A output	Waveform 4, $C_L = 5\text{pF}$	25		25	ns
t_{PLZ}	Disable from LOW GAB input to B output	Waveform 4, $C_L = 5\text{pF}$	25		25	ns

NOTE:

Test limits in screened columns are preliminary.

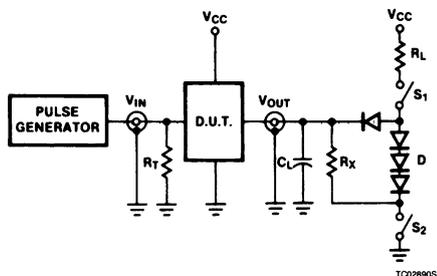
AC WAVEFORMS



Transceivers

74LS620, LS623

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t _{pZH}	Open	Closed
t _{pZL}	Closed	Open
t _{pHZ}	Closed	Closed
t _{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

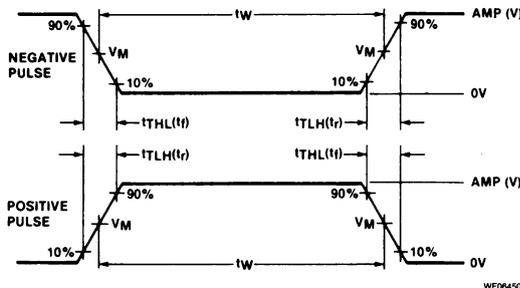
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS621, LS622 Transceivers

'LS621 Non-Inverting Octal Bus Transceiver (Open Collector)
'LS622 Inverting Octal Bus Transceiver (Open Collector)
Product Specification

Logic Products

FEATURES

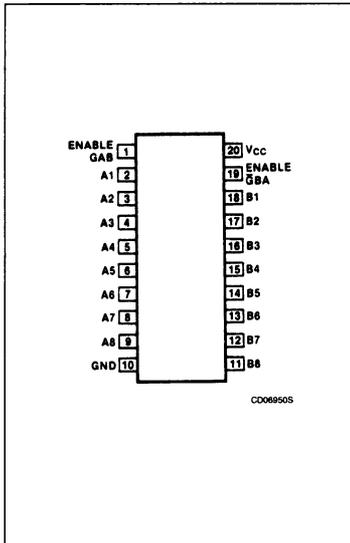
- Octal bidirectional bus interface
- Open-collector output
 - LS621, non-inverting
 - LS622, inverting
- Hysteresis on all Data inputs
- PNP inputs for reduced loading

DESCRIPTION

The 'LS621 is an octal transceiver featuring non-inverting open-collector bus compatible outputs in both send and receive directions. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'LS622 is an inverting version of the 'LS621. Both have built-in hysteresis to minimize ac noise effects.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS621	19.0ns	54.5ns
74LS622	19.0ns	54.5ns

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS621N, N74LS622N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

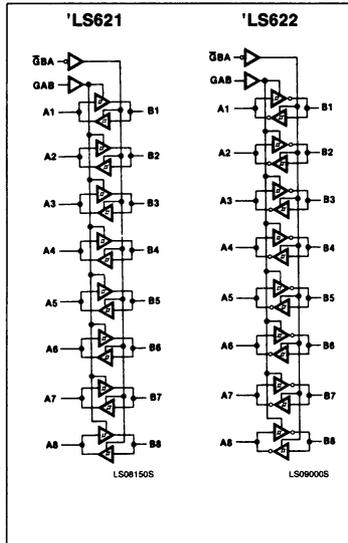
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

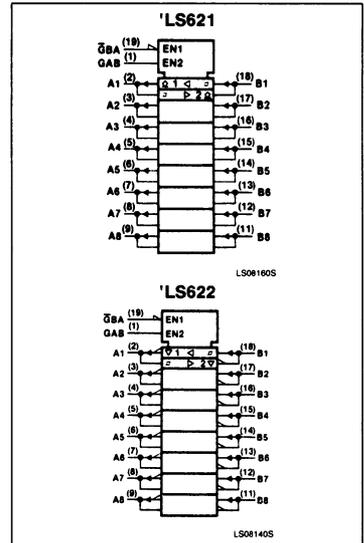
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the

logic levels at the enable inputs ($\overline{G}BA$ and GAB).

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceivers

74LS621, LS622

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
$\bar{G}BA$	GAB	'LS621	'LS622
L	L	B data to A bus	\bar{B} data to A bus
H	H	A data to B bus	\bar{A} data to B bus
H	L	(Z)	(Z)
L	H	B data to A bus, A data to B bus	\bar{B} data to A bus, \bar{A} data to B bus

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS621 and 'LS622 the capability to store data by simultaneous enabling of $\bar{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.6	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	HIGH-level output voltage			5.5	V
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

Transceivers

74LS621, LS622

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS621, 74LS622			UNIT
		Min	Typ ²	Max	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input	0.2	0.4		V
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{OH} = 5.5V$			100	μA
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12mA$	0.25	0.4	V
		$I_{OL} = 24mA$ (74LS)	0.35	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0V$			0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7V$			20	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4V$			-0.4	mA
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	42	70	mA
		I_{CCL} Outputs LOW	67	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

3. Measure I_{CC} with outputs open.

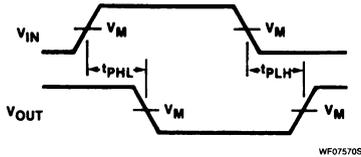
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	74LS621		74LS622		UNIT
		$C_L = 45pF$, $R_L = 667\Omega$		$C_L = 45pF$, $R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A input to B output	Waveform 2, '621		25		25	ns
	Waveform 1, '622		25		25	
t_{PLH} Propagation delay t_{PHL} B input to A output	Waveform 2, '621		25		25	ns
	Waveform 1, '622		25		25	
t_{PLH} Propagation delay $\bar{G}BA$ input to A output GAB input to B output	Waveform 1		40		40	ns
	Waveform 2		40		40	
t_{PHL} Propagation delay $\bar{G}BA$ input to A output GAB input to B output	Waveform 2		50		60	ns
	Waveform 1		50		60	

Transceivers

74LS621, LS622

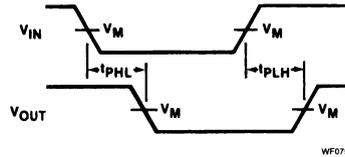
AC WAVEFORMS



WF07570S

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 1. Waveform For Inverting Outputs

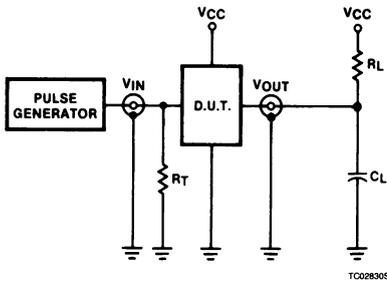


WF07580S

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 2. Waveform For Non-Inverting Outputs

TEST CIRCUITS AND WAVEFORMS



TC02830S

Test Circuit For 74 Open Collector Outputs

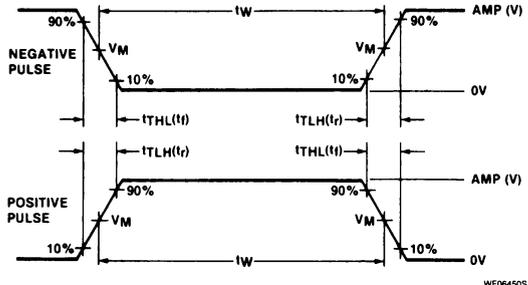
DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.



WF06450S

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS640, 74LS640-1 Transceiver

Inverting Octal Bus Transceiver (3-State)
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- Inverting 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS640-1)

DESCRIPTION

The 'LS640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS640-1 features a 48mA sink current capability. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS640 & -1	7ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS640N N74LS640-1N
Plastic SOL-20	N74LS640D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

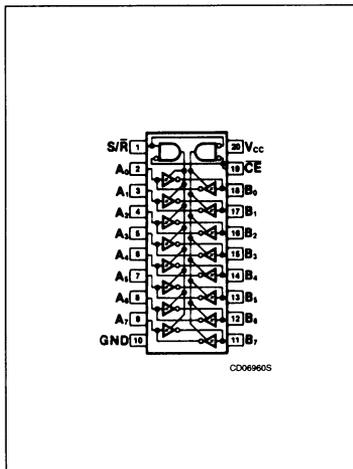
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

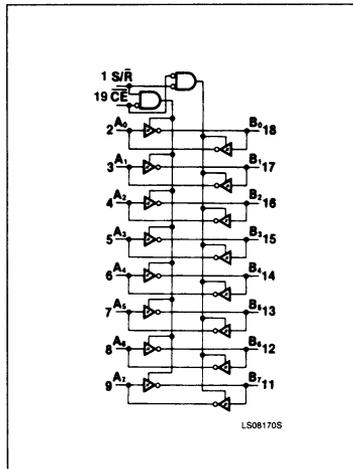
NOTE:

A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

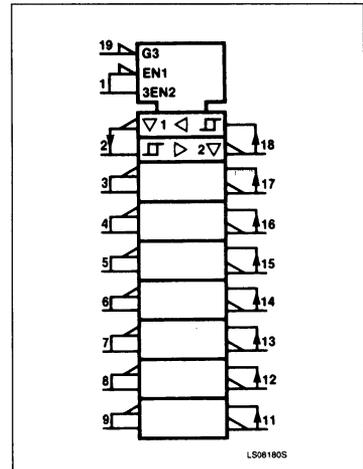
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceiver

74LS640, 74LS640-1

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/\overline{R}	A_n	B_n
L	L	$A = \overline{B}$	Inputs
L	H	Inputs	$B = \overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level

L = LOW voltage level

X = Don't care

(Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70	°C

NOTE

 V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS & -1			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.6	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-15	mA
I_{OL}	LOW-level output current			24	mA
		74LS-1 only		48	mA
T_A	Operating free-air temperature	0		70	°C

Transceiver

74LS640, 74LS640-1

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74LS640			74LS640-1			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input		0.2	0.4		0.2	0.4		V
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$	2.0			2.0			V
		$I_{OH} = -3\text{mA}$	2.4	3.4		2.4	3.4		V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12\text{mA}$		0.25	0.4	0.25	0.4		V
		$I_{OL} = 24\text{mA}$ (74LS)		0.35	0.5	0.35	0.5		V
		$I_{OL} = 48\text{mA}$ (74LS-1)					0.4	0.5	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-1.5			-1.5	V
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 2.7\text{V}$				20			20	μA
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 0.4\text{V}$				-400			-400	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ A or B input			0.1			0.1	mA
		$V_I = 7.0\text{V}$ S/\overline{R} or \overline{CE} input			0.1			0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$				20			20	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$				-0.4			-0.4	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$		-40		-130	-40		-130	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		48	70	48	70		mA
		I_{CCL} Outputs LOW		62	90	62	90		mA
		I_{CCZ} Outputs OFF		64	95	64	95		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
3. I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

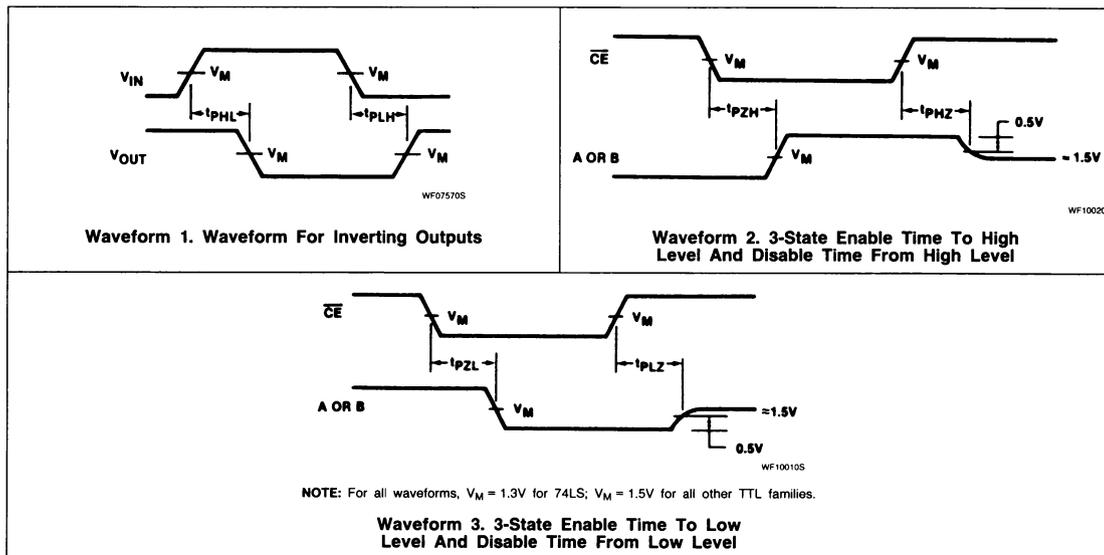
Transceiver

74LS640, 74LS640-1

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS & -1		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 1	10 15	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 1	10 15	ns
t_{PZH}	Enable to HIGH \overline{CE} , S/\overline{R} inputs to A output	Waveform 2	40	ns
t_{PZH}	Enable to HIGH \overline{CE} , S/\overline{R} inputs to B output	Waveform 2	40	ns
t_{PZL}	Enable to LOW \overline{CE} , S/\overline{R} inputs to A output	Waveform 3	40	ns
t_{PZL}	Enable to LOW \overline{CE} , S/\overline{R} inputs to B output	Waveform 3	40	ns
t_{PHZ}	Disable from HIGH \overline{CE} , S/\overline{R} inputs to A output	Waveform 2, $C_L = 5\text{pF}$	25	ns
t_{PHZ}	Disable from HIGH \overline{CE} , S/\overline{R} inputs to B output	Waveform 2, $C_L = 5\text{pF}$	25	ns
t_{PLZ}	Disable from LOW \overline{CE} , S/\overline{R} inputs to A output	Waveform 3, $C_L = 5\text{pF}$	25	ns
t_{PLZ}	Disable from LOW \overline{CE} , S/\overline{R} inputs to B output	Waveform 3, $C_L = 5\text{pF}$	25	ns

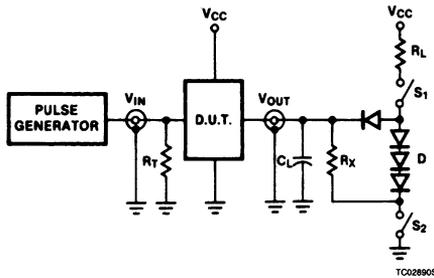
AC WAVEFORMS



Transceiver

74LS640, 74LS640-1

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

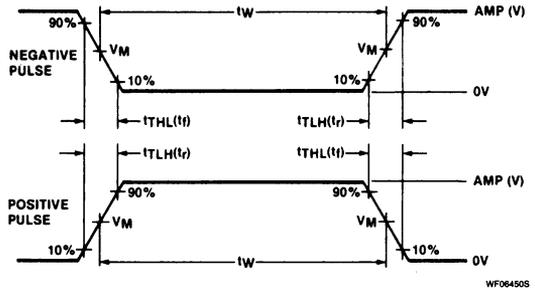
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = $1k\Omega$ for 74, 74S, R_X = $5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS641, LS642, 74LS641-1, LS642-1 Transceivers

Octal Bus Transceiver (Open Collector)
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- Open Collector Outputs
 - 'LS641, non-inverting
 - 'LS642, inverting
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS641-1, LS642-1)

FUNCTION TABLE, 'LS641

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/ \overline{R}	A _n	B _n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	(Z)	(Z)

FUNCTION TABLE, 'LS642

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/ \overline{R}	A _n	B _n
L	L	A = \overline{B}	Inputs
L	H	Inputs	B = \overline{A}
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

TYPE	TYPICAL PROPAGATION DELAY (A to B)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS641 & -1	17ns	58mA
74LS642 & -1	17ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V ±5%; T _A = 0°C to +70°C
Plastic DIP	N74LS641N N74LS641-1N N74LS642N N74LS642-1N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

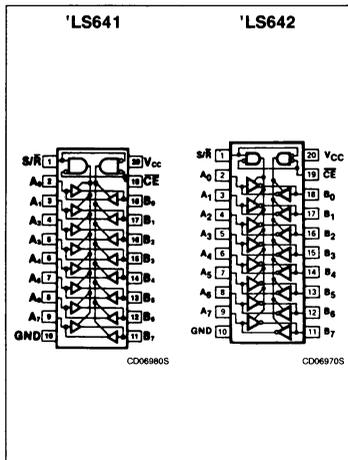
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

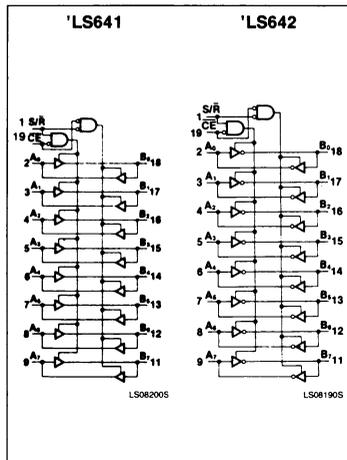
NOTE:

A 74LS unit load (LSul) is 20μA I_{IH} and -0.4mA I_{IL}.

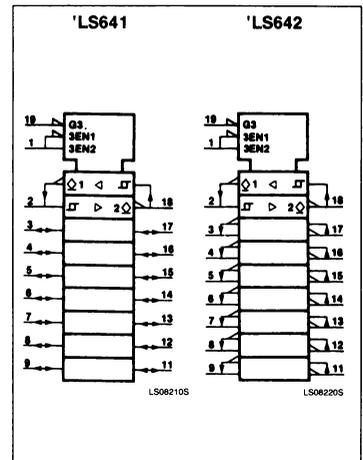
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceivers

74LS641, LS642, 74LS641-1, LS642-1

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS & -1	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS & -1			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.6	V
I _{IK}	Input clamp current			-18	mA
V _{OH}	HIGH-level output voltage			5.5	V
I _{OL}	LOW-level output current			24	mA
			74LS-1 only	48	mA
T _A	Operating free-air temperature	0		70	°C

5

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS641			74LS641-1			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
ΔV _T	Hysteresis (V _{T+} - V _{T-})	V _{CC} = MIN, A or B input		0.2	0.4		0.2	0.4	V
I _{OH}	HIGH-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V				100			100 μA
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = 12mA		0.25	0.4	0.25	0.4	V
			I _{OL} = 24mA (74LS)		0.35	0.5	0.35	0.5	V
			I _{OL} = 48mA (74LS-1)				0.4	0.5	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5		-1.5	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	A or B input			0.1	0.1	mA
			V _I = 7.0V	S/ \bar{R} or $\bar{C}\bar{E}$ input			0.1	0.1	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20		20	μA	
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4		-0.4	mA	
I _{CC}	Supply current ³ (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH		48	70	48	70	mA
			I _{CC} L Outputs LOW		62	90	62	90	mA
			I _{CC} Z Outputs OFF		64	95	64	95	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Measure I_{CC} with outputs open.

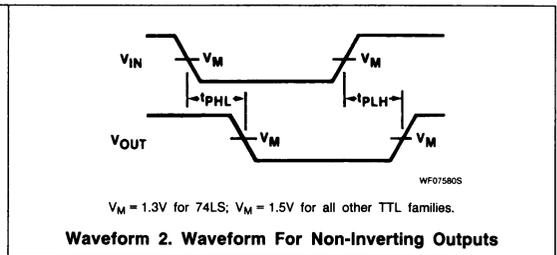
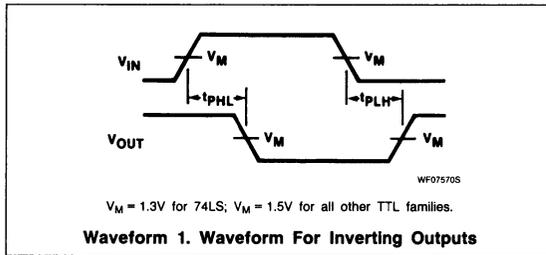
Transceivers

74LS641, LS642, 74LS641-1, LS642-1

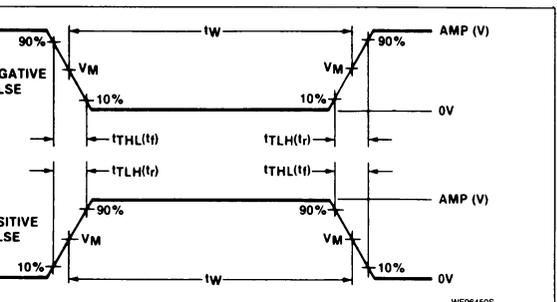
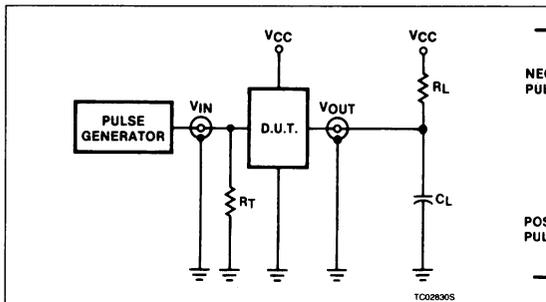
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	$C_L = 45\text{pF}$, $R_L = 667\Omega$		UNIT
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output Waveform 1		25	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output Waveform 1		25	ns
t_{PLH}	Propagation delay CE, S/R inputs to A output Waveform 1		40	ns
	CE input to B output Waveform 1		40	
	S/R input to B output Waveform 2		40	
t_{PHL}	Propagation delay CE, S/R inputs to A output Waveform 2		50	ns
	CE input to B output Waveform 2		50	
	S/R input to B output Waveform 1		50	

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS645, 74LS645-1 Transceiver

Octal Bus Transceiver (3-State)
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS645-1)

DESCRIPTION

The 'LS645 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS645-1 features a 48mA sink current capability. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS645 & -1	10ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS645N N74LS645-1N
Plastic SOL-20	N74LS645D N74LS645-1D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

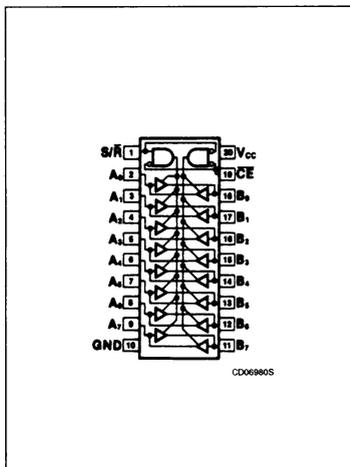
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

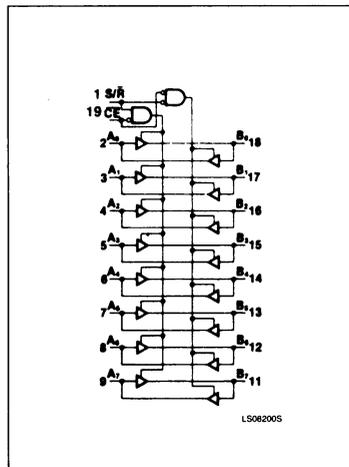
NOTE:

A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

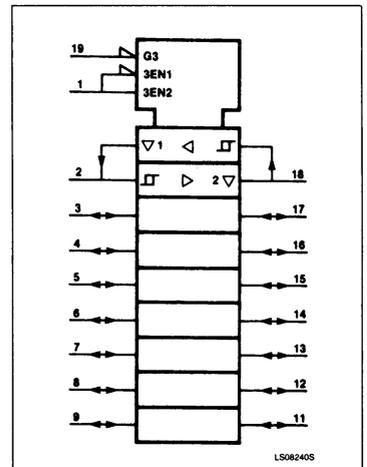
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceiver

74LS645, 74LS645-1

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/\overline{R}	A_n	B_n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	(Z)	(Z)

H = HIGH voltage level

L = LOW voltage level

X = Don't care

(Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

NOTE:

 V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS & -1			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.6	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-15	mA
I_{OL}	LOW-level output current			24	mA
		74LS-1 only		48	mA
T_A	Operating free-air temperature	0		70	°C

Transceiver

74LS645, 74LS645-1

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74LS645			74LS645-1			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input		0.2	0.4		0.2	0.4		V
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$	2.0			2.0			V
		$I_{OH} = -3\text{mA}$	2.4	3.4		2.4	3.4		V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12\text{mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 24\text{mA}$ (74LS)		0.35	0.5		0.35	0.5	V
		$I_{OL} = 48\text{mA}$ (74LS-1)					0.4	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-1.5			-1.5	V
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 2.7\text{V}$				20			20	μA
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 0.4\text{V}$				-400			-400	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ A or B input			0.1			0.1	mA
		$V_I = 7.0\text{V}$ S/ \overline{R} or \overline{CE} input			0.1			0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$				20			20	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$				-0.4			-0.4	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$		-40		-130	-40		-130	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		48	70		48	70	mA
		I_{CCL} Outputs LOW		62	90		62	90	mA
		I_{CCZ} Outputs OFF		64	95		64	95	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with outputs open.

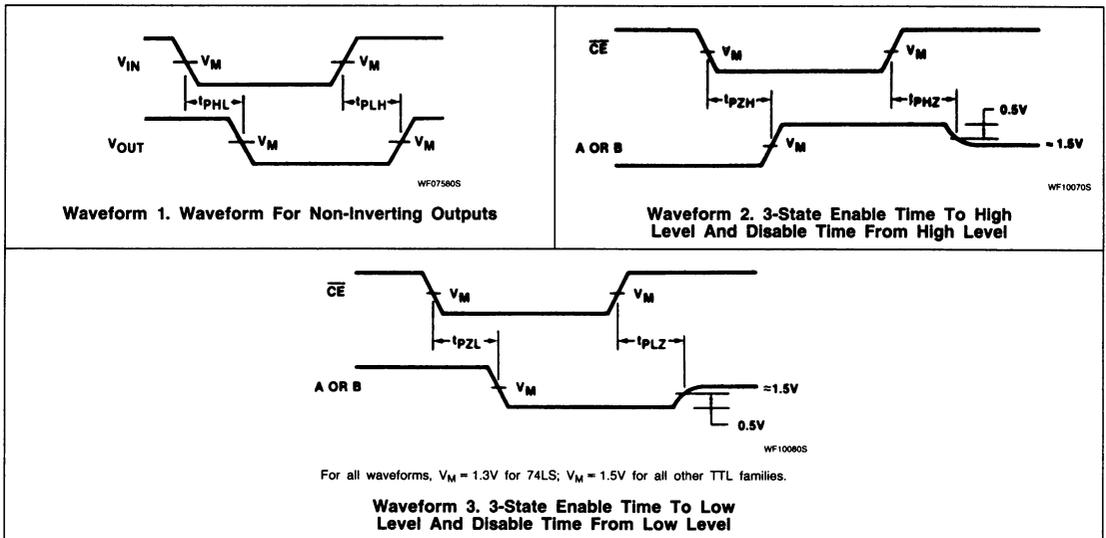
Transceiver

74LS645, 74LS645-1

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS & -1		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 1	15 15	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 1	15 15	ns
t_{pZH}	Enable to HIGH \overline{CE} , S/R inputs to A output	Waveform 2	40	ns
t_{pZH}	Enable to HIGH \overline{CE} , S/R inputs to B output	Waveform 2	40	ns
t_{pZL}	Enable to LOW \overline{CE} , S/R inputs to A output	Waveform 3	40	ns
t_{pZL}	Enable to LOW \overline{CE} , S/R inputs to B output	Waveform 3	40	ns
t_{pHZ}	Disable from HIGH \overline{CE} , S/R inputs to A output	Waveform 2, $C_L = 5\text{pF}$	25	ns
t_{pHZ}	Disable from HIGH \overline{CE} , S/R inputs to B output	Waveform 2, $C_L = 5\text{pF}$	25	ns
t_{pLZ}	Disable from LOW \overline{CE} , S/R inputs to A output	Waveform 3, $C_L = 5\text{pF}$	25	ns
t_{pLZ}	Disable from LOW \overline{CE} , S/R inputs to B output	Waveform 3, $C_L = 5\text{pF}$	25	ns

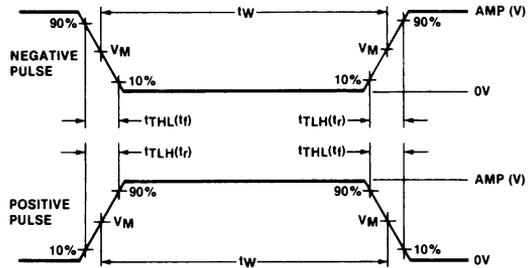
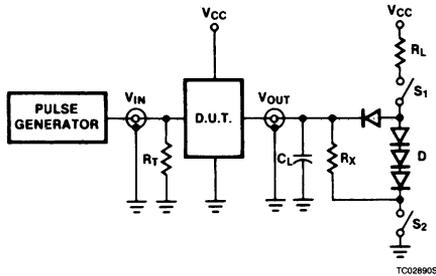
AC WAVEFORMS



Transceiver

74LS645, 74LS645-1

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

74LS670 Register File

4 x 4 Register File (3-State)
Product Specification

Logic Products

FEATURES

- Simultaneous and independent Read and Write operations
- Expandable to almost any word size and bit length
- 3-State outputs
- See '170 for open collector version

DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable ($\overline{W_E}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{W_E}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when $\overline{W_E}$ is HIGH.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS670	25ns	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS670N
Plastic SOL-16	N74LS670D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$D_0 - D_3, W_A, W_B, R_A, R_B$	Inputs	1LSul
$\overline{W_E}$	Input	2LSul
$\overline{R_E}$	Input	3LSul
$Q_0 - Q_3$	Outputs	10LSul

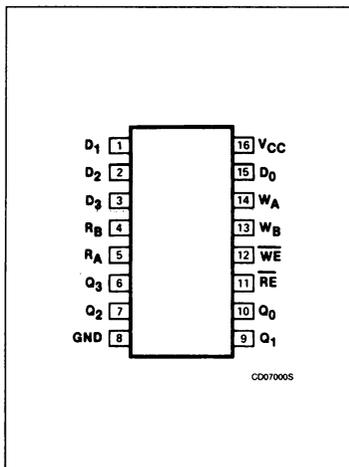
NOTE:

A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

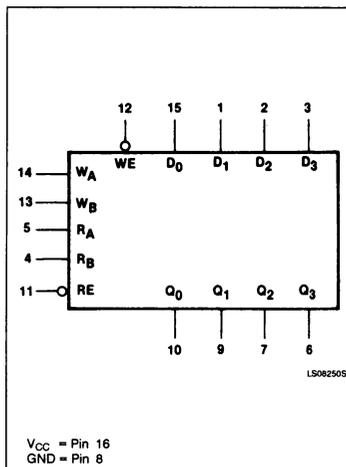
Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{R_E}$)

is LOW. Data outputs are in the HIGH impedance "off" state when the Read Enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

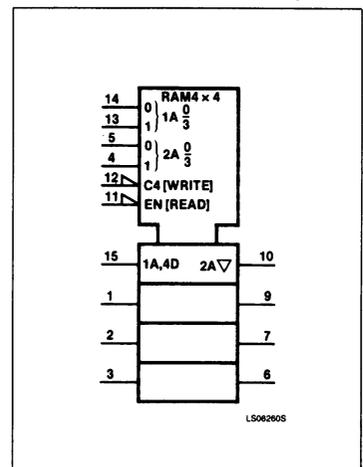
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Register File

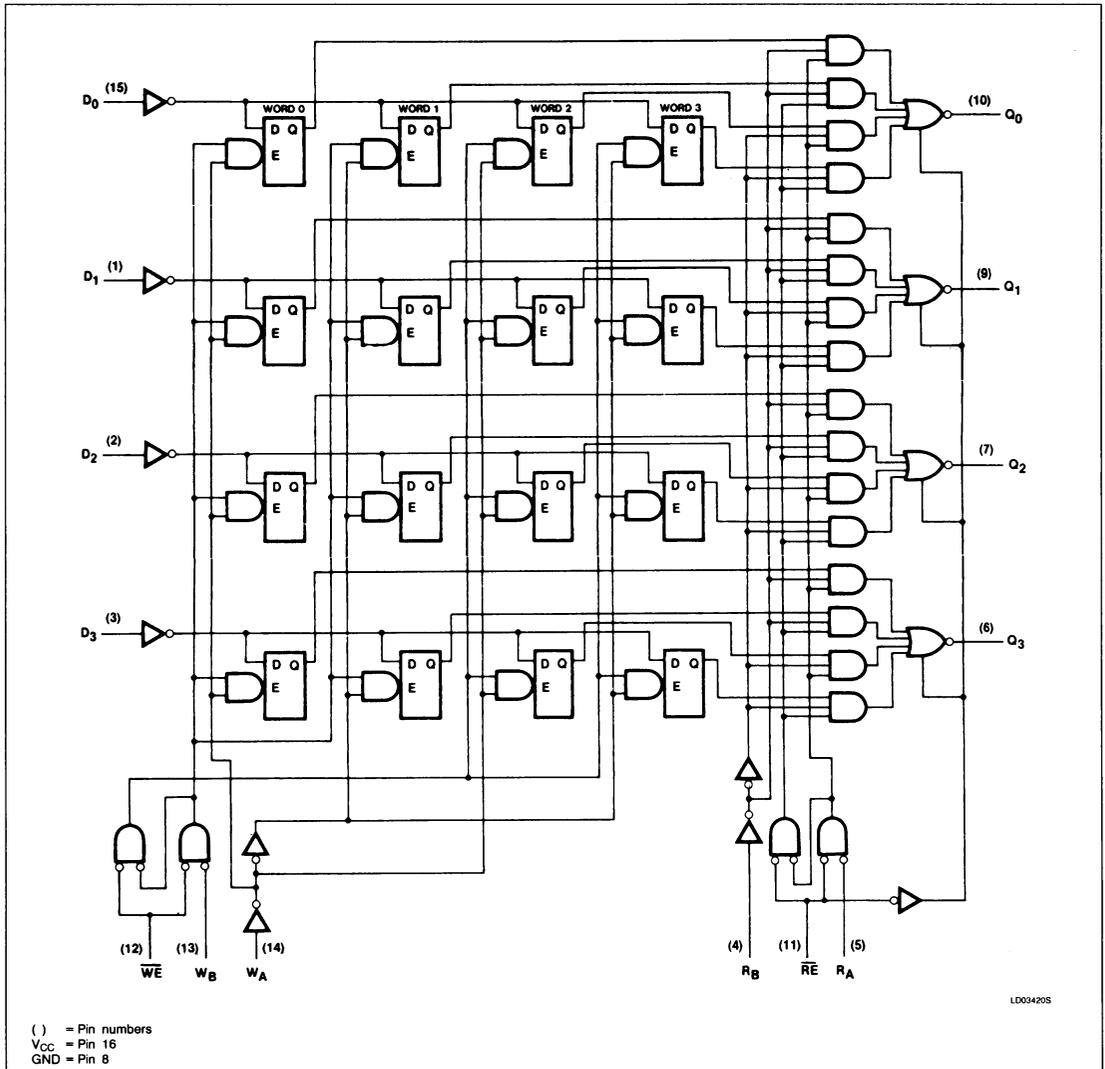
74LS670

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-

up resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to

be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

LOGIC DIAGRAM



Register File

74LS670

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES ^(a)
	\overline{WE}	D_n	
Write data	L	L	L
	L	H	H
Data latched	H	X	no change

NOTE:

a. The Write Address (W_A and W_B) to the "internal latches" must be stable while \overline{WE} is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT Q_n
	\overline{RE}	Internal Latches ^(b)	
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

NOTE:

b. The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by \overline{WE} or \overline{RE} operation.

H = HIGH voltage level

L = LOW voltage level

X = Don't care

(Z) = HIGH impedance "off" state.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-2.6	mA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

Register File

74LS670

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS670			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.1		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5	V
		I _{OL} = 4mA (74LS)		0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.7V			20	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V			-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V	D ₀ - D ₃ , W _A , W _B , R _A , R _B inputs		0.1	mA	
		\overline{WE} input		0.2	mA	
		\overline{RE} input		0.3	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	D ₀ - D ₃ , W _A , W _B , R _A , R _B inputs		20	μA	
		\overline{WE} input		40	μA	
		\overline{RE} input		60	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	D ₀ - D ₃ , W _A , W _B , R _A , R _B inputs		-0.4	mA	
		\overline{WE} input		-0.8	mA	
		\overline{RE} input		-1.2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		30	50	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with 4.5V applied to all Data inputs and Read Enable and Write Enable inputs, ground Read Address and Write Address inputs and leave all outputs open. This is a worse-case condition.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS670		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay Read address to output	Waveform 2		40 45	ns
t _{PLH} t _{PHL} Propagation delay Write enable to output	Waveform 1		45 50	ns
t _{PLH} t _{PHL} Propagation delay Data to output	Waveform 1		45 40	ns
t _{PZH} Enable time to HIGH level	Waveform 3		35	ns
t _{PZL} Enable time to LOW level	Waveform 3		40	ns
t _{PHZ} Disable time from HIGH level	Waveform 3, C _L = 5pF		50	ns
t _{PLZ} Disable time from LOW level	Waveform 3, C _L = 5pF		35	ns

Register File

74LS670

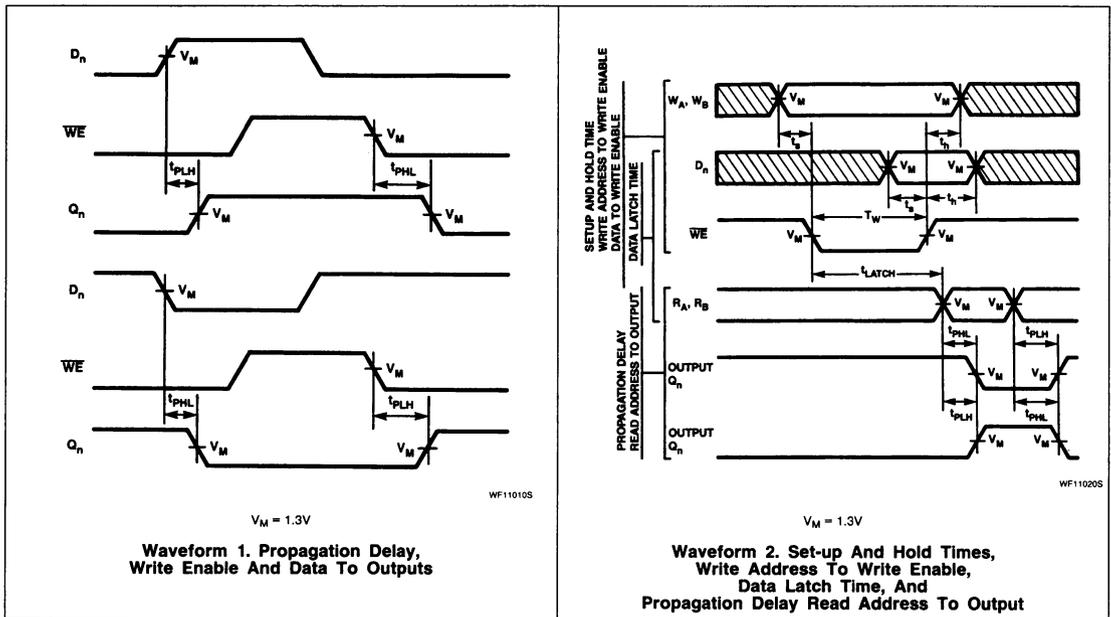
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS670		UNIT
		Min	Max	
t_W Read enable pulse width	Waveform 3	25		ns
t_W Write enable pulse width	Waveform 2, $\overline{RE} = \leq 0.8\text{V}$	25		ns
t_S Set-up time, data to positive-going \overline{WE}	Waveform 2	10		ns
t_H Hold time, data to positive-going \overline{WE}	Waveform 2	15		ns
t_S Set-up time, write address to negative-going $\overline{WE}^{(c)}$	Waveform 2	15		ns
t_H Hold time, write address to positive-going $\overline{WE}^{(c)}$	Waveform 2	5.0		ns
t_{latch} Latch time for new data ^(d)	Waveform 2	25		ns

NOTES:

- c. Write address set-up time will protect the data written into the previous address. If protection of data in the previous address is not required, t_S (write address to \overline{WE}) can be ignored, as any address selection sustained for the final 30ns of the \overline{WE} pulse and during t_H (write address to \overline{WE}) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
- d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of \overline{WE} to the rising or falling edge of R_A or R_B . \overline{RE} must be LOW.

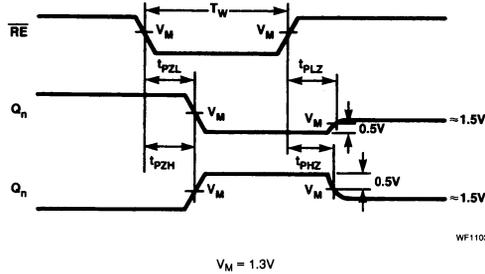
AC WAVEFORMS



Register File

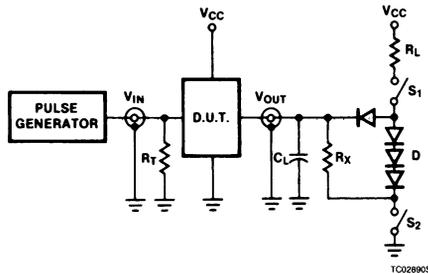
74LS670

AC WAVEFORMS (Continued)

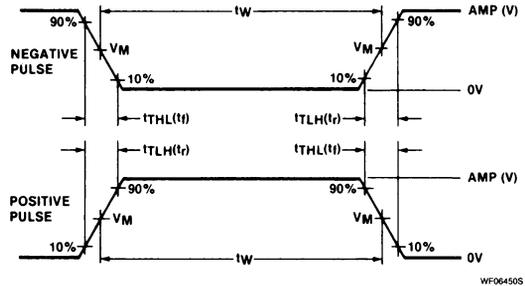


Waveform 3. 3-State Enable Time To High Or Low Level Disable Time From High Or Low Level

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = $1k\Omega$ for 74, 74S, $R_X = 5k\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Section 6
8T Series Data Sheets

Logic Products

8T09 Quad Bus Driver

3-State Quad Bus Driver
Product Specification

Logic Products

FEATURES

- High speed
- Quad bus driver
- 40mA Low-state drive
- 300pF load driving capability

DESCRIPTION

The 8T09 is a high speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The tri-state outputs present high impedance to the bus when disabled (control input '1'), and active drive when enabled (control input '0'). This eliminates the resistor pullup requirement while providing performance superior to open collector schemes. Each output can sink 40mA and drive 300pF loading with guaranteed propagation delay less than 20 nanoseconds.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T09	7ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T09N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
Data	Input	1ul
Disable	Input	1ul
3, 6, 8, 11	Output	10ul

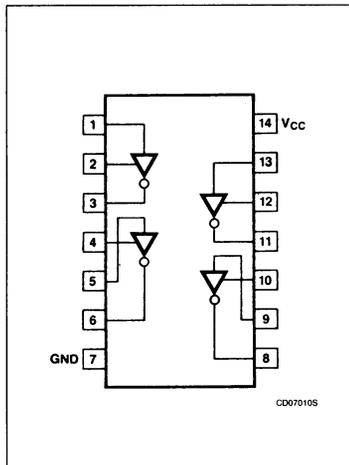
NOTE:

A unit load (ul) is $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

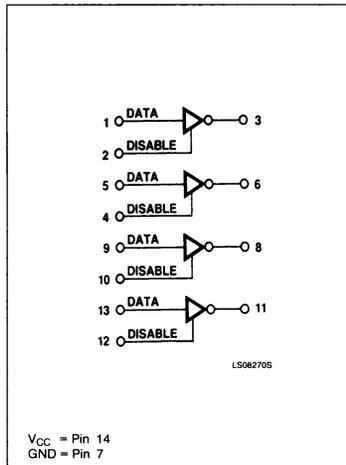
FUNCTION TABLE

DATA	DISABLE	OUTPUT
0	0	1
1	0	0
0	1	Hi-Z
1	1	Hi-Z

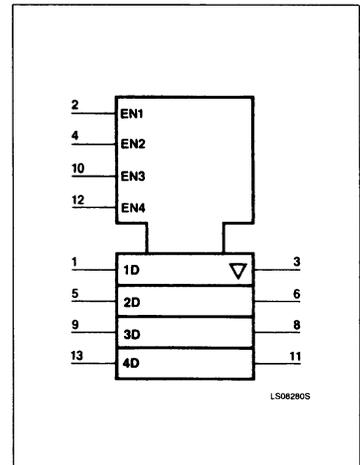
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Quad Bus Driver

8T09

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-5.2	mA
I _{OL}	LOW-level output current			40	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T09		UNIT
		Min	Max	
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -5.2mA		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 40mA		V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V		mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
t _{PLH} t _{PHL}	Propagation delay Data to output	Figure 1	C _L = 30pF C _L = 300pF	10 20	ns
t _{PZH}	Enable to HIGH	Figure 3	C _L = 30pF C _L = 300pF	14 22	ns
t _{PZL}	Enable to LOW	Figure 2	C _L = 30pF C _L = 300pF	14 22	ns
t _{PHZ}	Disable from LOW	Figure 3	C _L = 30pF C _L = 300pF	14 22	ns
t _{PLZ}	Disable from LOW	Figure 2	C _L = 30pF C _L = 300pF	14 22	ns

Quad Bus Driver

8T09

AC TEST CIRCUITS AND WAVEFORMS

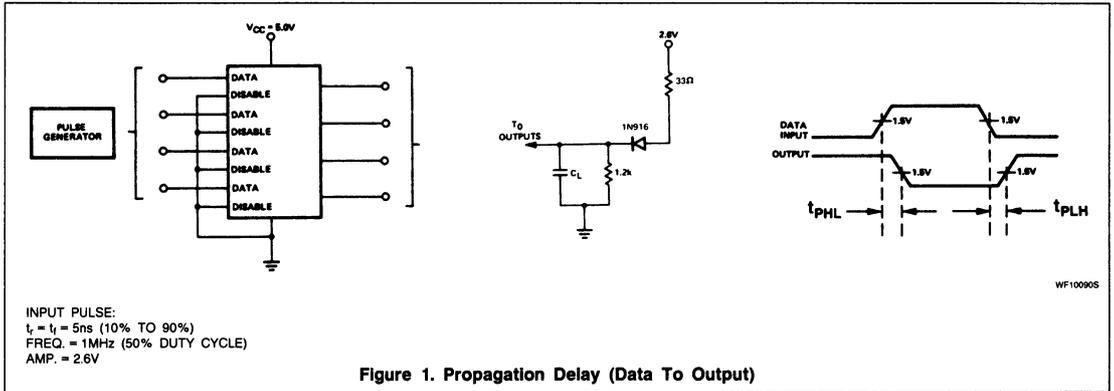


Figure 1. Propagation Delay (Data To Output)

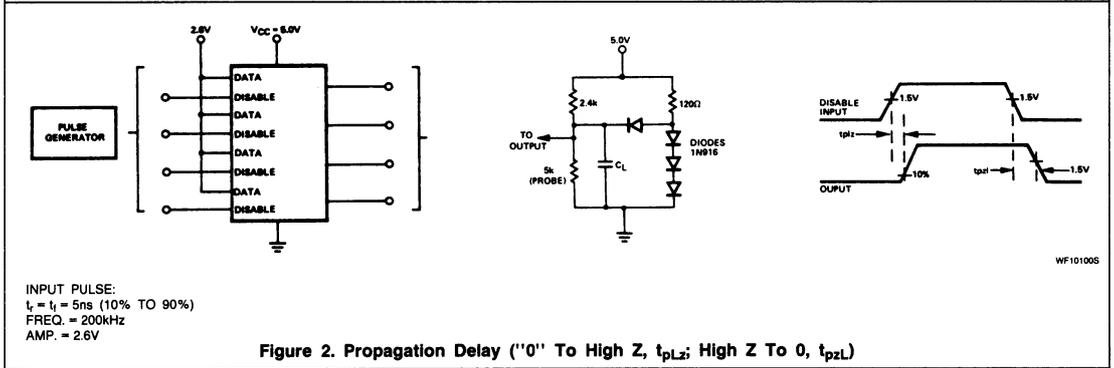


Figure 2. Propagation Delay ("0" To High Z, t_{PLz} ; High Z To 0, t_{PzL})

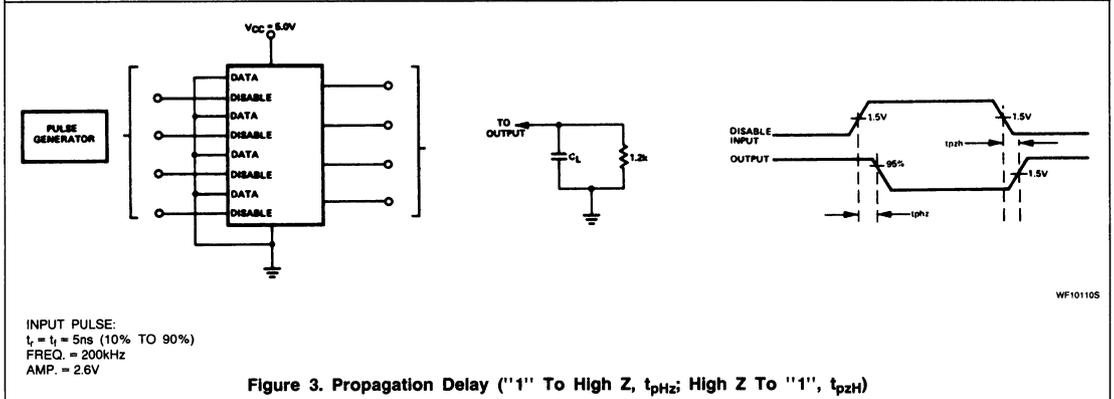


Figure 3. Propagation Delay ("1" To High Z, t_{PHz} ; High Z To "1", t_{PzH})

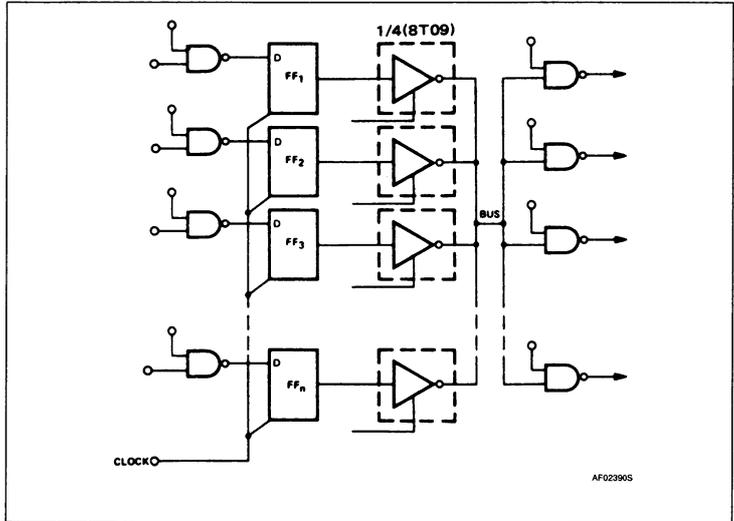
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Quad Bus Driver

8T09

The figure to right illustrates usage of the 8T09 in data processing logic. For example, FF₁ thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".

TYPICAL APPLICATIONS



AF023905

8T10 Bus Flip-Flop

3-State Quad D-Type Bus Flip-Flop Product Specification

Logic Products

DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A master reset input resets all flip-flops upon application of a logic "1" level.

Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T10	24ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^{\circ}C$ to $+70^{\circ}C$
Plastic DIP	N8T10N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

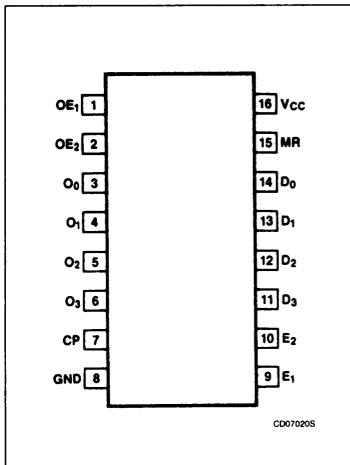
PINS	DESCRIPTION	8T
D_n , CP	Input	1ul
E_n , MR, OE_n	Input	1.2ul
Q_n	Output	10ul

NOTE:

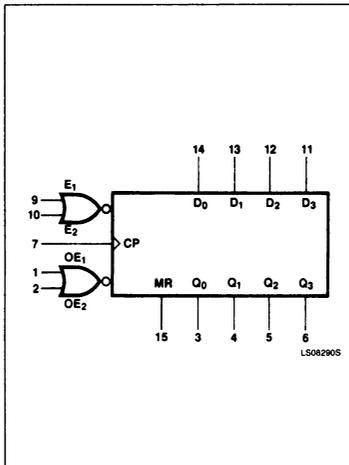
A unit load (ul) is $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

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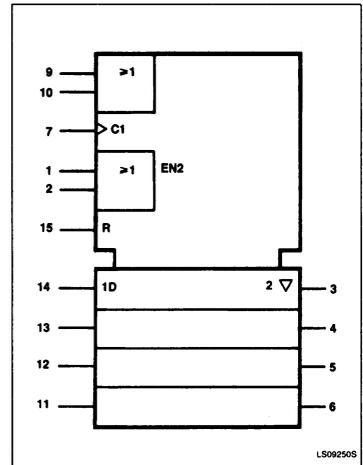
PIN CONFIGURATION



LOGIC SYMBOL



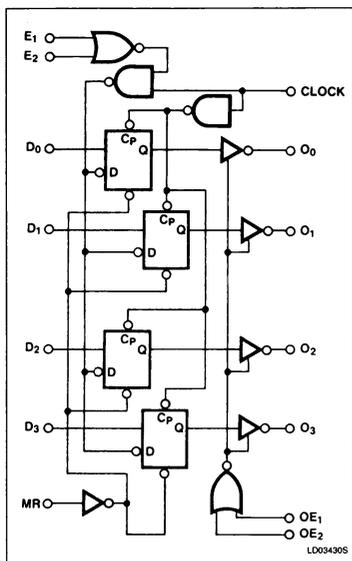
LOGIC SYMBOL (IEEE/IEC)



Bus Flip-Flop

8T10

LOGIC DIAGRAM



FUNCTION TABLE

D_n	E	OE	Q_{n+1}
0	0	0	0
1	0	0	1
X	1	0	Q_n
X	X	1	High Z

NOTES:

1. Q_n refers to the output state before a clock pulse.
2. Q_{n+1} refers to the output state after a clock pulse.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V_{CC}	4.75	5.0	5.25	V
V_{IH}	2.0			V
V_{IL}			0.8	V
I_{IK}			-12	mA
I_{OH}			-5.2	mA
I_{OL}			32	mA
T_A	0		70	°C

Bus Flip-Flop

8T10

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T10		UNIT
		Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		-1.5	V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -5.2mA	2.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, I _{OL} = 32mA		0.4	V
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 4.5V	Dn	40	μA
		Cp	40	μA
		Others	50	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	Dn	-3.2	mA
		Cp	-3.2	mA
		Others	-2.0	mA
I _{OS} Short-circuit output current ²	V _{CC} = MAX	-40	-120	mA
I _{CC} Supply current (total)	V _{CC} = 5.25V		118	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T		UNIT
		Min	Max	
t _{MAX} Maximum clock frequency	Figure 1	35		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Figure 1	C _L = 30pF	25	ns
		C _L = 300pF	35	
t _{PHL} Propagation delay, MR to output	Figure 2	C _L = 30pF	22	ns
		C _L = 300pF	30	
t _{PZH} Output enable to HIGH level				ns
t _{PZL} Output enable to LOW level	Figure 4	C _L = 300pF	30	ns
t _{PHZ} Output disable from HIGH level				ns
t _{PLZ} Output disable from LOW level	Figure 4	C _L = 300pF	30	ns

NOTE:

For industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T10		UNIT
		Min	Max	
t _{W(CP)} Clock pulse width	Figure 1		12	ns
t _{W(MR)} MR pulse width	Figure 2	15		ns
t _s Set-up time, data to clock	Figure 1	5		ns
t _h Hold time, data to clock	Figure 3		5	ns

Bus Flip-Flop

8T10

AC TEST CIRCUITS AND WAVEFORMS

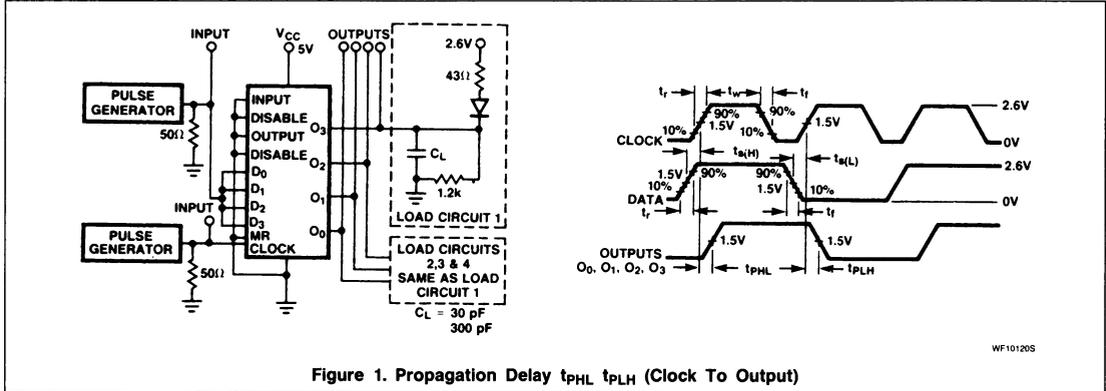


Figure 1. Propagation Delay t_{PHL} t_{PLH} (Clock To Output)

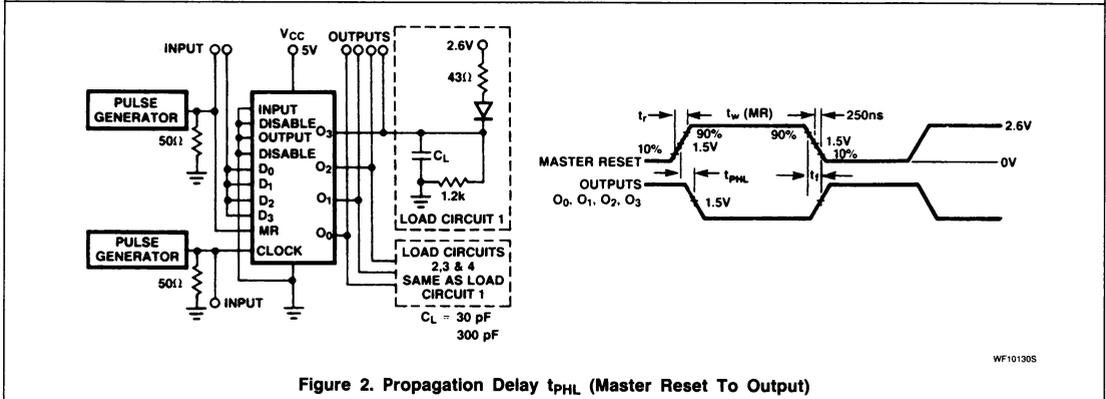


Figure 2. Propagation Delay t_{PHL} (Master Reset To Output)

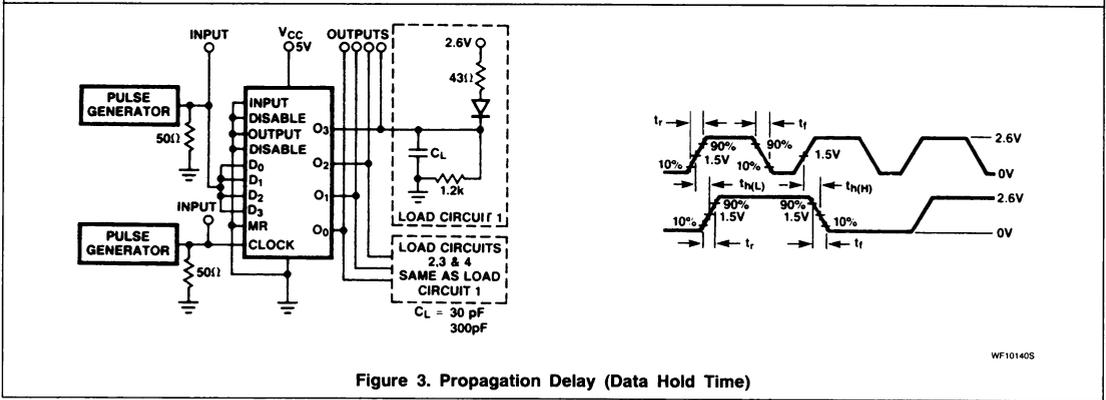


Figure 3. Propagation Delay (Data Hold Time)

Bus Flip-Flop

8T10

AC TEST CIRCUITS AND WAVEFORMS (Continued)

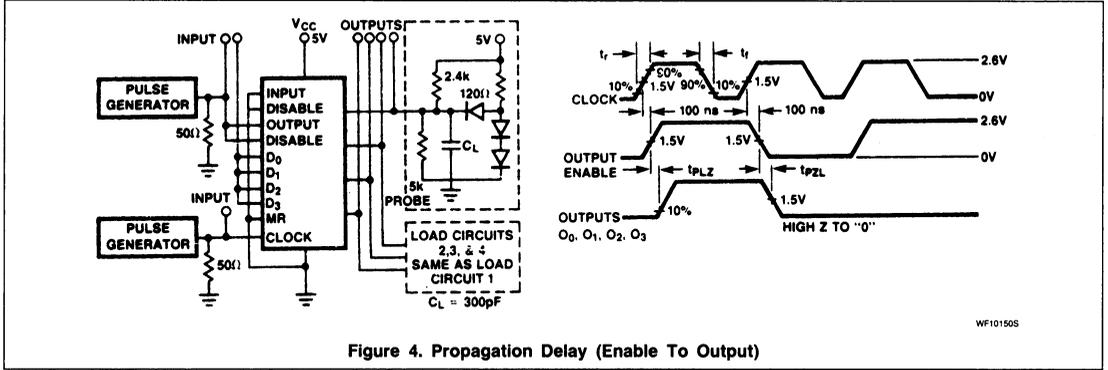
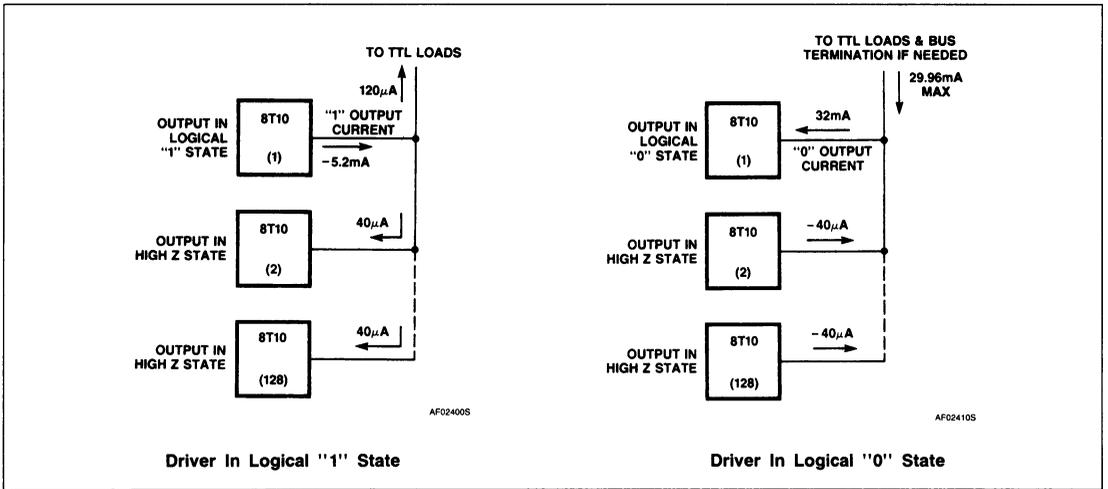


Figure 4. Propagation Delay (Enable To Output)

TYPICAL APPLICATIONS



8T13 Line Driver

Dual Line Driver
Product Specification

Logic Products

KEY DESIGN BENEFITS

- High-Power Drive Capability:
Specified at -75mA source current rating at 2.4 volts.
- Party-Line Operation:
Emitter-follower outputs enable two or more drivers to drive the same line. This permits multiple time-shared terminal connections since these drivers have no effect upon the transmission line unless activated.
- Input gating structure allows employment of the "OR" as well as the "AND" function.
- High Speed: Propagation Delay = 20ns (max).
- Input Clamp Diodes: Protects inputs from line ringing.
- Single 5 Volt power supply.
- Short Circuit Protection:
Incorporates a latch-back short circuit protection feature which protects the device by limiting the current it may source under conditions of zero load resistance.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
8T13	32ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$
Plastic DIP	N8T13N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
All inputs	Input	1ul
7, 9	Output	46ul

NOTE:

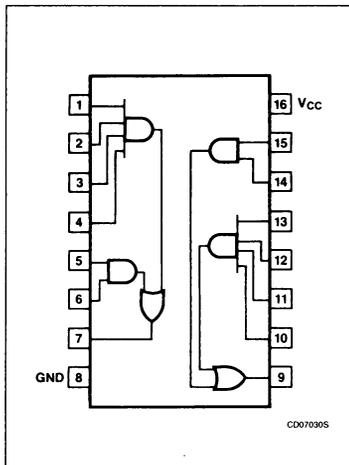
A unit load (ul) is $40\mu\text{A } I_{IH}$ and $-1.6\text{mA } I_{IL}$.

DESCRIPTION

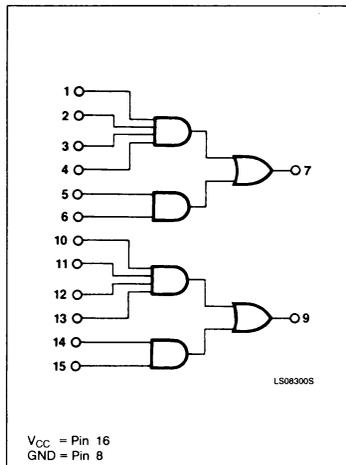
The 8T13 is a monolithic Dual Line Driver designed to drive 50Ω or 75Ω coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with stand- and TTL or DTL

systems. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50Ω to 500Ω .

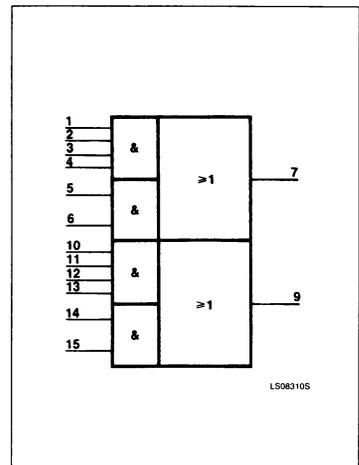
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Line Driver

8T13

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			75	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T13		UNIT	
		Min	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		-1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = 75mA	2.4		V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		40	μA
		V _{CC} = 0V, V _I = 4.5V			
I _{IL}	LOW-level input current	V _{CC} = MAX, V _{IN} = 0.4V		-1.6	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		-30	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		60	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

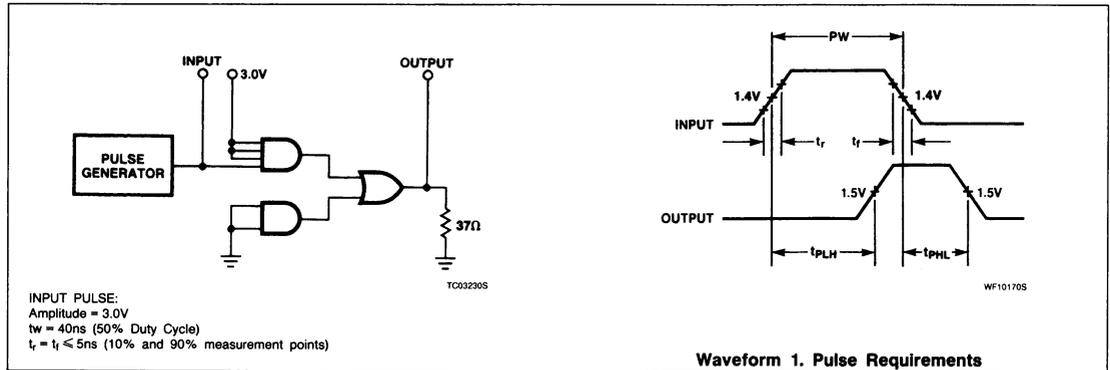
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T13		UNIT	
		R _L = 37Ω			
		Min	Max		
t _{PLH} t _{PHL}	Propagation delay	Waveform 1		20 20	ns

Line Driver

8T13

AC TEST CIRCUIT AND WAVEFORM



8T15 Line Driver

Dual Communications EIA/MIL Line Driver
Product Specification

Logic Products

DESCRIPTION

The 8T15 Dual Communications Line Driver provides line driving capability for data transmission between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, Mil STD-188B and CCITT V24.

This dual 4-input NAND driver will accept standard TTL logic level inputs and will drive interface lines with nominal data levels of $+6V$ and $-6V$. Output slew rate may be adjusted by attaching an external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as $\pm 25V$.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
8T15	4ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T15

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

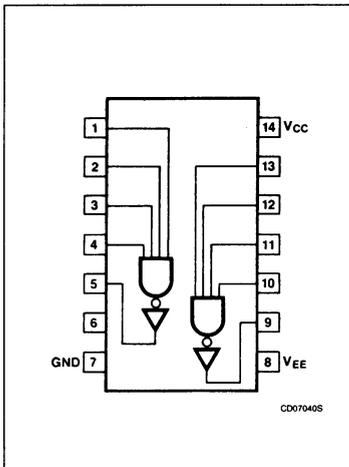
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
All	Inputs	1ul
All	Outputs	10ul

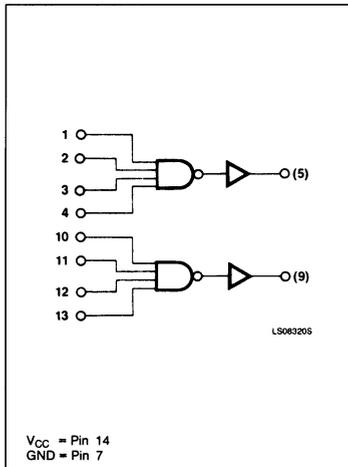
NOTE:

Where a unit load (ul) is $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

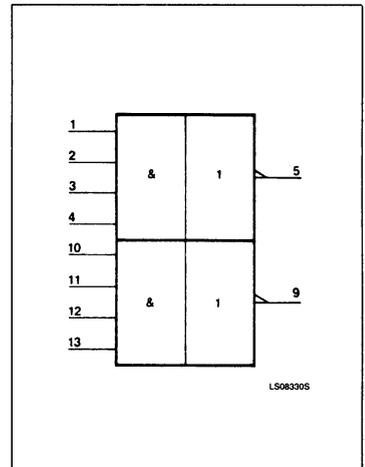
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Line Driver

8T15

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage, positive	+15	V
V _{EE}	Supply voltage, negative	-15	V
V _{IN}	Input voltage	-0.5 to +5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage, positive	11	12	13	V
V _{EE}	Supply voltage, negative	-11	-12	-13	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			12	mA
I _{OH}	HIGH-level output current			-4	mA
I _{OL}	LOW-level output current			4	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T15		UNIT		
		Min	Max			
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0	V	
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V	
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		1.5	V	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -4mA		-5.0	-7.0	V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 4mA		-5.0	-7.0	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		40	μA	
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V		-1.6	mA	
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		-25	+25	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		16	mA	
I _{EE}	Supply current (total)	V _{CC} = 5.25V		-28	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Line Driver

8T15

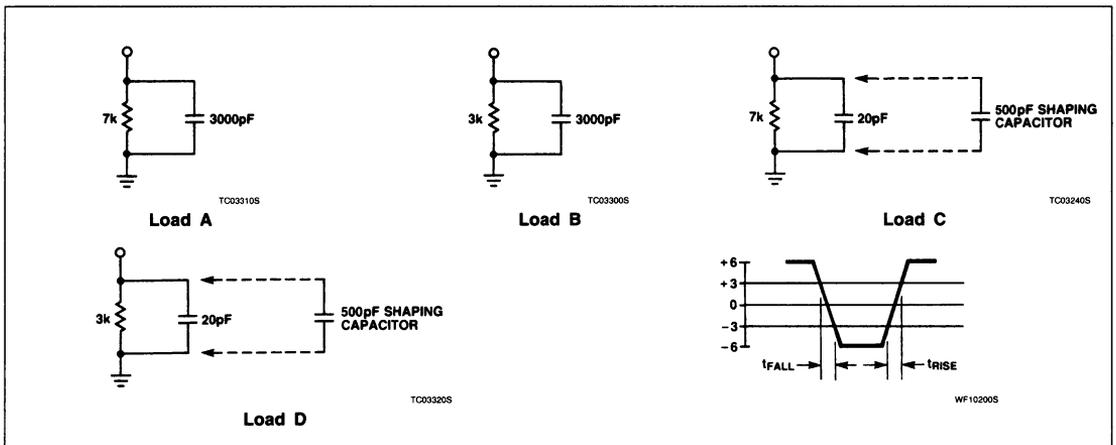
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TO	8T15			UNIT
		Min	Typ	Max	
Output rise time ¹	Load A			4	ns
	Load C	200			ns
Output fall time ¹	Load B			4	ns
	Load D	200			ns
Current ²	Positive supply			16	mA
	Negative supply			28	mA

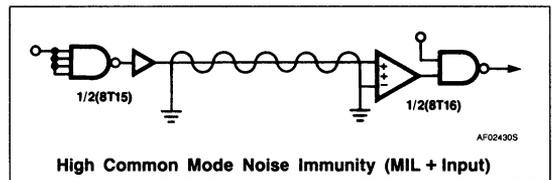
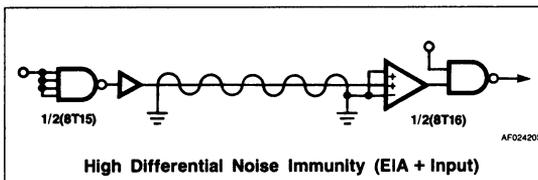
NOTES:

- Rise and fall times are measured between the $+3\text{V}$ and -3V points on the output waveform.
- $V_{CC} = 12.6\text{V}$, $V_{EE} = -12.6\text{V}$.

AC TEST CIRCUITS AND WAVEFORMS



TYPICAL APPLICATION



6

Line Driver

8T15

Table 1 provides a summary of the specific requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V24 for Communications Line Drivers along with the electrical characteristics of the Signetics 8T15.

Table 1

SPECIFICATION	EIA RS-232B, C	MIL-STD-188B	CCITT V24	SIGNETICS 8T15	
				(Limit)	(Typical)
Output voltage "1"	-5V min. ($R_L = 3000\Omega$) -15V max. ($R_L = 7000\Omega$)	-6 \pm 1V	-5V min. ($R_L = 3000\Omega$) -15V max. ($R_L = 7000\Omega$)	-5V min. -7V max. at 4mA	-6V at 4mA
Output voltage "0"	+5V min. ($R_L = 3000\Omega$) +15V max. ($R_L = 7000\Omega$)	+6 \pm 1V	+5V min. ($R_L = 3000\Omega$) +15V max. ($R_L = 7000\Omega$)	+5V min. 7V max. at -4mA	+6V at -4mA
Source impedance (power on)	Not specified	100 Ω max. for 1 < 10mA	Not specified		95 Ω for \pm (0.5 to 4.0mA)
Source impedance (power off)	300 min. at \pm 2V	N/A	300 min. at \pm 2V	300 min. at \pm 2V	2.5M Ω
Max. short circuit current	\pm 500mA max. to \pm 25V	100mA max. (to ground)	\pm 500mA max. (to \pm 25V)	\pm 25mA max. (to \pm 25V)	\pm 5mA (to \pm 25V)
Wave shape (rise and fall time)	\pm 4% of pulse interval (max.)	\pm 5% of pulse interval (min.)		4 μ s-3000pF 200ns-20pF	2 μ s-3000pF 25ns-20pF
Bit rate	0-20kHz	4kHz normal	20kHz max.		3MHz
Open circuit drive	\pm 25V max.	\pm 6V \pm 1V		\pm 6V \pm 1V	\pm 6V
Signal characteristics	1ms max. transition		1ms max. transition		2 μ s with $C_L = 3000$ pF
	30V/ μ s max. dV/dt		30V/ μ s max. dV/dt		20V/ μ s with $C_L = 500$ pF

8T16 Line Receiver

Dual Communications EIA/MIL Line Receiver with Hysteresis
Product Specification

Logic Products

DESCRIPTION

The 8T16 Dual Communications line Receiver provides receiving capability for data lines between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL-STD-188B and CCITT V24 and operates from a single 5 volt power supply.

The receivers accept single (EIA) or double ended (MIL) inputs and are provided with an output strobing control. Both EIA and MIL input standards are accommodated.

When using the EIA input terminal (with the Hysteresis terminal open), input voltage threshold levels are typically +2V and -2V with a guaranteed minimum Hysteresis of 2.4V. By grounding the "Hysteresis" terminal, the EIA input voltage threshold levels may be shifted to typically +1.0V and +2.1V with a minimum guaranteed Hysteresis of 0.75V. (Note that when using the EIA inputs, the MIL inputs—both positive and negative—must be grounded.)

The MIL input voltage threshold levels are typically +0.6V and -0.6V with a

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T16	100ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T16

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
MIL(+), MIL(-), EIA	Input	1ul
HYST, strobe	Input	1ul
2, 13	Output	10ul

NOTE:

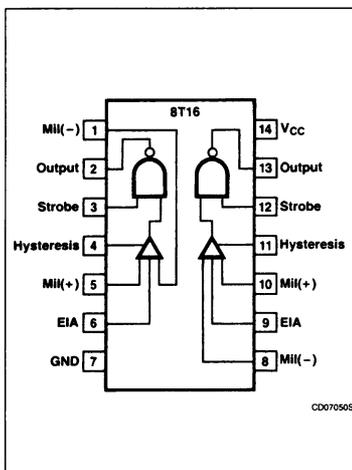
A unit load (ul) is $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

minimum guaranteed Hysteresis of 0.7V. A MIL negative terminal is provided on each receiver per specification MIL-STD-188B to provide for common mode noise rejection.

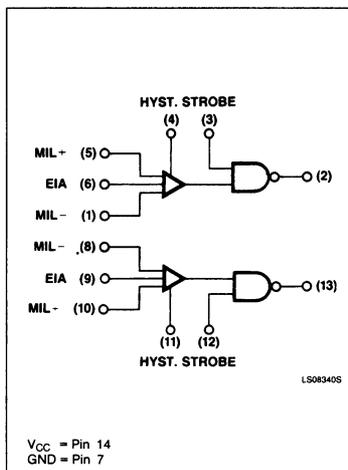
Each receiver includes a strobe input so that:

- A "1" on the strobe input allows data transfer.
- A "0" on the strobe input holds the output high.

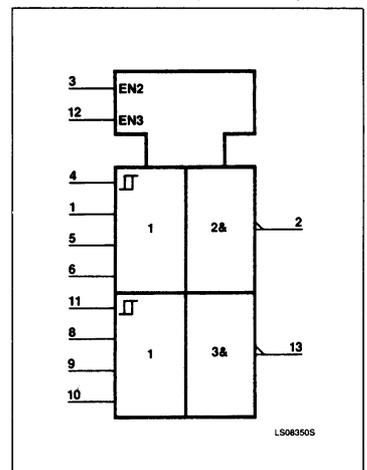
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Line Receiver

8T16

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0		2.5	V
V _{IL}	LOW-level input voltage	1.1		1.5	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	μA
I _{OL}	LOW-level output current			9.6	mA
T _A	Operating free-air temperature	0		70	°C

Line Receiver

8T16

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TO	FROM	TEST CONDITIONS	8T16			UNIT	
				Min	Typ	Max		
V _{OH} Output voltage (EIA) Hysteresis open ^{8, 12} Hysteresis open Hysteresis grounded ^{8, 10}	Outputs -800 μ A	EIA, MIL(+), MIL(-), STROBE	EIA = 3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V	2.6	3.5		V	
	Outputs -800 μ A	EIA, MIL(+), MIL(-), STROBE	EIA = +1.2V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V	2.8	3.5		V	
	Outputs -800 μ A	EIA, MIL(+), MIL(-), HYS, STROBE	EIA = +0.3V, MIL(+) = 0V, MIL(-) = 0V HYS = 0V, STROBE = 2.0V	2.6	3.5		V	
V _{OH} Output voltage (MIL) ^{8, 11} Output voltage (MIL) ^{8, 11} Output voltage (MIL) ^{8, 13}	Outputs -800 μ A	MIL(+), MIL(-), STROBE	MIL(+), -0.1mA, MIL(-) = 0V STROBE = 2.0V	2.6	3.5		V	
	Outputs -800 μ A	MIL(+), MIL(-), STROBE	MIL(+) = -0.9V, MIL(-) = 0V STROBE = 2.0V	2.6	3.5		V	
	Outputs -800 μ A	MIL(+), MIL(-), STROBE	MIL(+) = +0.35V, MIL(-) = 0V, STROBE = 2.0V	2.8	3.5		V	
V _{OH} Output voltage (STROBE) ⁸	Outputs -800 μ A	EIA, MIL(+), MIL(-), STROBE	EIA = 3.0V, MIL(+) = 0V MIL(-) = 0V, STROBE = 2.0V	2.6	3.5		V	
V _{OL} Output voltage (EIA) Hysteresis open ^{9, 12} Hysteresis open ^{9, 10} Hysteresis grounded ^{9, 12} Output voltage (MIL) ^{9, 13} Output voltage (MIL) Output voltage (MIL) ^{9, 11} Input resistance (EIA) Input resistance (MIL) Power consumption (per receiver) ¹⁷	Outputs 9.6mA	EIA, MIL(+), MIL(-), STROBE	EIA = +3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V			0.4	V	
	Outputs 9.6mA	EIA, MIL(+), MIL(-), STROBE	EIA = -1.2V, MIL(+) = 0V MIL(-) = 0V, STROBE = 2.0V		0.2	0.4	V	
	Outputs 9.6mA	EIA, MIL(+), MIL(-), HYS, STROBE	EIA = +3.0V, MIL(+) = 0V, MIL(-) = 0V HYS = 0V, STROBE = 2.0V			0.4	V	
	Outputs 9.6mA	MIL(+), MIL(-), STROBE	MIL(+) = +0.1mA, MIL(-) = 0V STROBE = 2.0V			0.4	V	
	Outputs 9.6mA	MIL(+), MIL(-), STROBE	MIL(+) = +0.9V, MIL(-) = 0V STROBE = 2.0V			0.4	V	
	Outputs 9.6mA	MIL(+), MIL(-), STROBE	MIL(+) = -0.35V, MIL(-) = 0V STROBE = 2.0V		0.2	0.4	V	
			EIA, MIL(+), MIL(-)	EIA = \pm 25V, MIL(+) = 0V MIL(-) = 0V	3	5	7	k Ω
			EIA, MIL(+), MIL(-)	EIA = 0V, MIL(+) = \pm 25V, MIL(-) = 0V	7.5	11.4		k Ω
			EIA, MIL(+), MIL(-)	EIA = 3.0V, MIL(+) = 0V, MIL(-) = 0V		44	75	mW
I _{OS} Output short circuit current ^{16, 17} Propagation delay ^{14, 15} Signal switching acceptance ¹⁵	Outputs 0V	EIA, MIL(+), MIL(-)	EIA = -3.0V, MIL(+) = 0V MIL(-) = 0V, STROBE = 5.0V	-10		-70	mA	
		STROBE	STROBE = 5.0V		100	150	ns	
		STROBE	STROBE = 5.0V	20			kHz	

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

2. All measurements are taken with ground pin tied to zero volts.

3. Positive current is defined as into the terminal referenced.

4. Positive logic definition: "UP" Level = H, "DOWN" Level = L.

5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.

6. Manufacturer reserves the right to make design and process changes and improvements.

7. This test guarantees operation free of latch-up over the specified input voltage range.

8. Output source current is supplied through a resistor to ground.

10. Previous EIA input: +3V (See hysteresis curve).

11. Previous MIL input: +0.9V (See hysteresis curve).

12. Previous EIA input: -3.0V (See hysteresis curve).

13. Previous MIL input: -0.9V (See hysteresis curve).

14. Reference AC Test Figures.

15. This test guarantees transfer of signals of up to 20kHz. Connect 1000pF between the output terminal and ground.

16. Each receiver to be tested separately.

17. V_{CC} = 5.25V.

Line Receiver

8T16

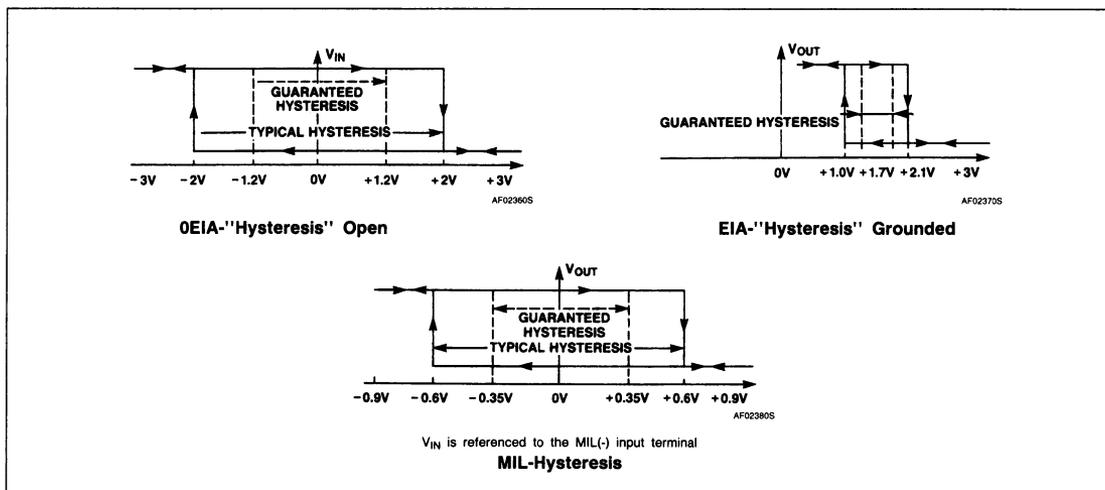
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	FROM	TEST CONDITIONS	8T16			UNIT
			Min	Typ	Max	
Input resistance						
EIA	EIA, MIL(+), MIL(-)	EIA = $\pm 25\text{V}$, MIL(+) = 0.0V , MIL(-) = 0.0V	3	5	7	$k\Omega$
MIL	EIA, MIL(+), MIL(-)	EIA = 0.0V , MIL(+) = $\pm 25\text{V}$, MIL(-) = 0.0V	7.5	11.4		$k\Omega$
Propagation delay	Strobe	Strobe = 5.00V		100	150	ns
Signal switching acceptance	Strobe	Strobe = 5.00V	20			kHz

NOTE:

This test guarantees transfer of signals of up to 20kHz. Correct 1000pF between the output terminal and ground.

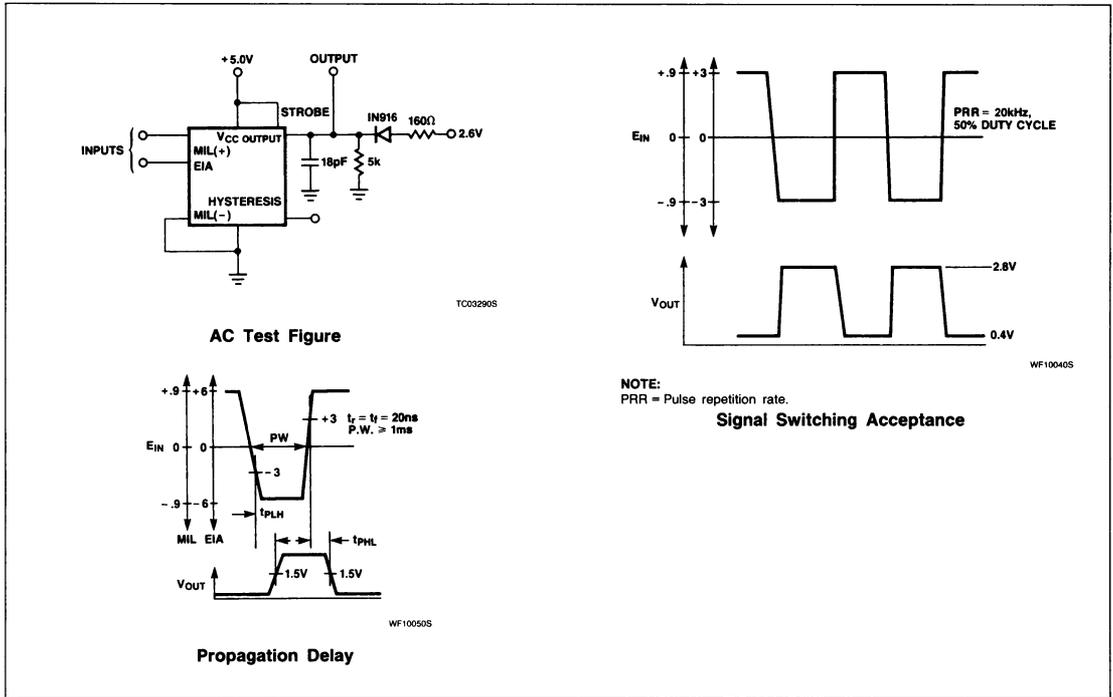
HYSTERESIS CURVES



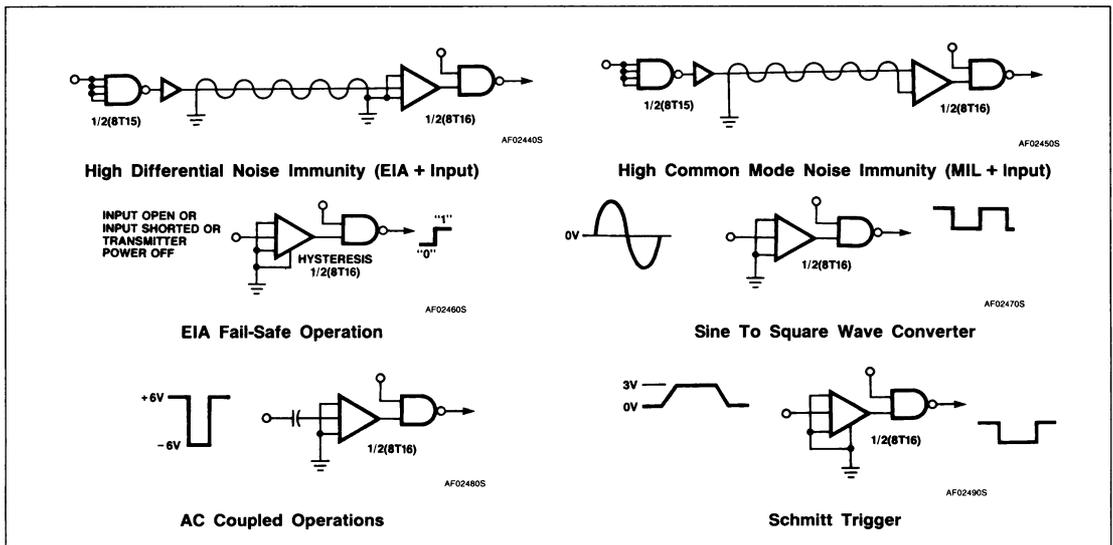
Line Receiver

8T16

AC TEST CIRCUITS AND WAVEFORMS



TYPICAL APPLICATIONS



6

8T20 Multivibrator

**Bidirectional One-Shot
Product Specification**

Logic Products

FEATURES

- Differential Input Threshold = $\pm 4\text{mV}$
- Pulse Position Error = Typically $< 3\text{ns}$
- Max. Input Frequency = 8MHz
- Triggers on Positive and/or Transitions

APPLICATIONS

- Disc, Tape and Drum Readers
- Digital Communications Receivers
- Signal Conditioners
- Transition Detectors

DESCRIPTION

The Bidirectional One Shot is intended for applications where high speed low level signal processing is required.

The 8T20 is a Monolithic Building Block, consisting of a high speed analog comparator, digital control circuitry, and a precision monostable multivibrator. The differential input threshold voltage is be-

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T20	30ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$
Plastic DIP	N8T20N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
PEC, NEC	Input	1ul
MR	Input	1ul
A, A; Q, Q	Output	10ul

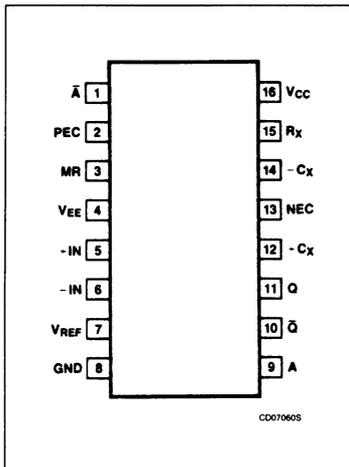
NOTE:

A unit load (ul) is $40\mu\text{A } I_{IH}$ and $-1.6\text{mA } I_{IL}$.

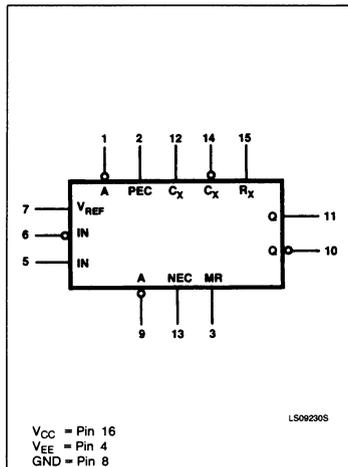
tween $\pm 4\text{mV}$ with respect to the input reference level which may range from -3.2V to $+4.2\text{V}$. For input frequencies up to 8MHz, the device may be condi-

tioned to act as a frequency doubler since it can trigger on both positive and negative input transitions.

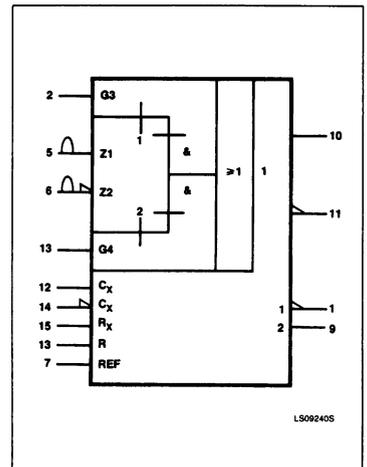
PIN CONFIGURATION



LOGIC SYMBOL



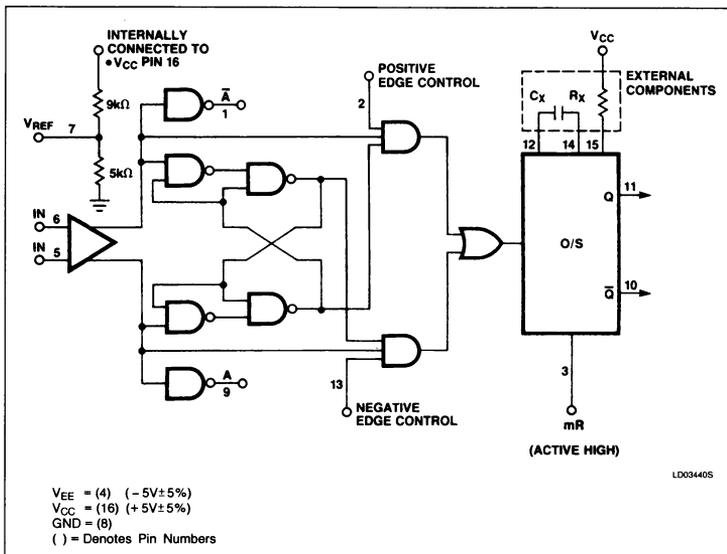
LOGIC SYMBOL (IEEE/IEC)



Multivibrator

8T20

LOGIC DIAGRAM



Timing pins permit using this device in a variety of applications where external control over pulse width is desirable. Pulse width (t^W) is defined by the relationship $t^W = C_x R_x \text{ Loge } 2$. Pulse width stability is internally compensated and virtually independent of temperature and V_{CC} variations, thus only limited by the accuracy of external timing components.

An internal resistive divider is available on the chip to provide a voltage of 1.4V (typ.). This output can be connected directly to either of the comparator inputs as a reference voltage when interfacing with TTL outputs.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	8T	UNIT
V_{CC} Supply voltage, positive	7.0	V
V_{EE} Supply voltage, negative	-7.0	V
V_{DIF} Differential input voltage	± 5.5	V
V_{IN} Input voltage	-0.5 to +5.5	V
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V_{CC} Supply voltage, positive	4.75	5.0	5.25	V
V_{EE} Supply voltage, negative	-4.75	5.0	-5.25	V
V_{IH} HIGH-level input voltage	2.0			V
V_{IL} LOW-level input voltage			0.8	V
I_{IK} Input clamp current			-12	mA
I_{OH} HIGH-level output current			-800	μA
I_{OL} LOW-level output current			16	mA
T_A Operating free-air temperature	0		70	$^{\circ}C$

Multivibrator

8T20

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T20		UNIT
		Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		-1.5	V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -800μA	2.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, I _{OL} = 16mA		0.4	V
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V PEC, NEC		-2.4	mA
I _{IL} Low level input current	V _{CC} = MAX, V _I = 0.4V mR		-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20	-70	mA
I _{CC} Supply current (total)	V _{CC} = 5.25V		55	mA
I _{EE} Supply current (total)	V _{CC} = 5.25V		-20	mA

DIFFERENTIAL INPUTS

V _T Input threshold voltage ⁴		±4		mV
I _B Input bias current ⁵	V _{CC} = +5V, V _{EE} = -5V		125	μA
I _{OS} Input offset current		2		μA
V _{CM} Common mode input volt, range ⁶		-3.2	+4.2	V

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- The differential input threshold voltage (V_T) is defined as the maximum DC voltage from the reference level necessary to trigger the one-shot.
- Refer to Figure 5.
- Common mode voltages that are confined within the dynamic range as specified will not cause false triggering of the one-shot.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min	Typ	Max	
Output frequency	Fig. 1, f _{in} = 8MHz	16			MHz
Propagation delay					
Input to Q, \bar{Q}	Fig. 2		30	50	ns
Input to A, \bar{A}	Fig. 4		30	50	ns
MR to Q, \bar{Q}			20	30	ns
Reference voltage (V _{REF})	Pin 7 tied to pin 6	0.8	1.4	2.0	V
Output pulse width, fig. 1	Rx = 10K, Cx = open	10		40	ns
Output pulse width, fig. 3	Rx = 10K, Cx = 100pF	600		800	ns

Multivibrator

8T20

AC TEST CIRCUITS AND WAVEFORMS

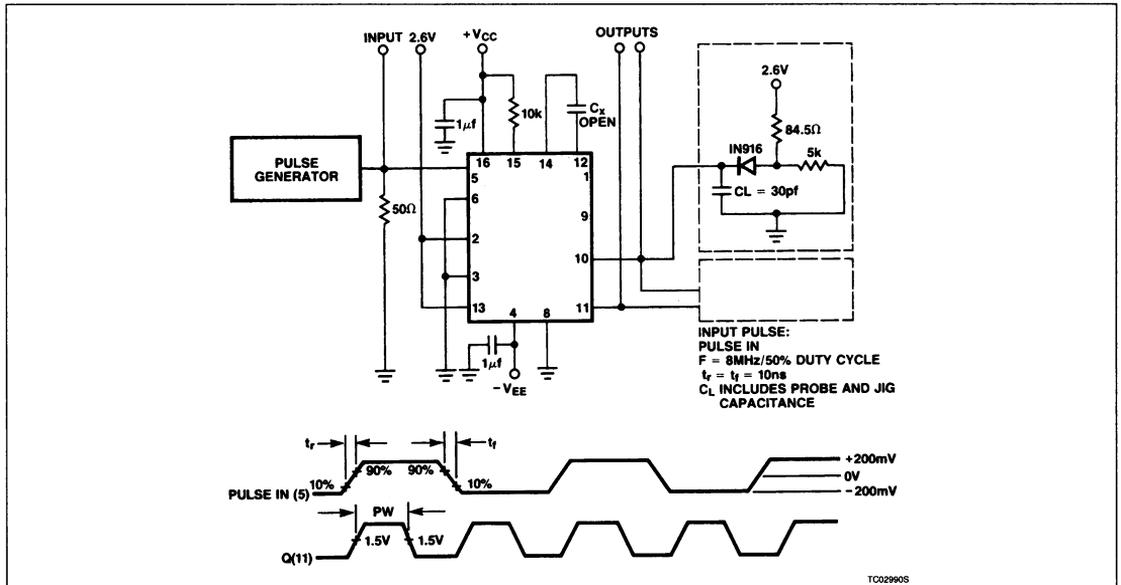


Figure 1. Minimum Output Pulse Width ($C_{x2} = OPEN$)

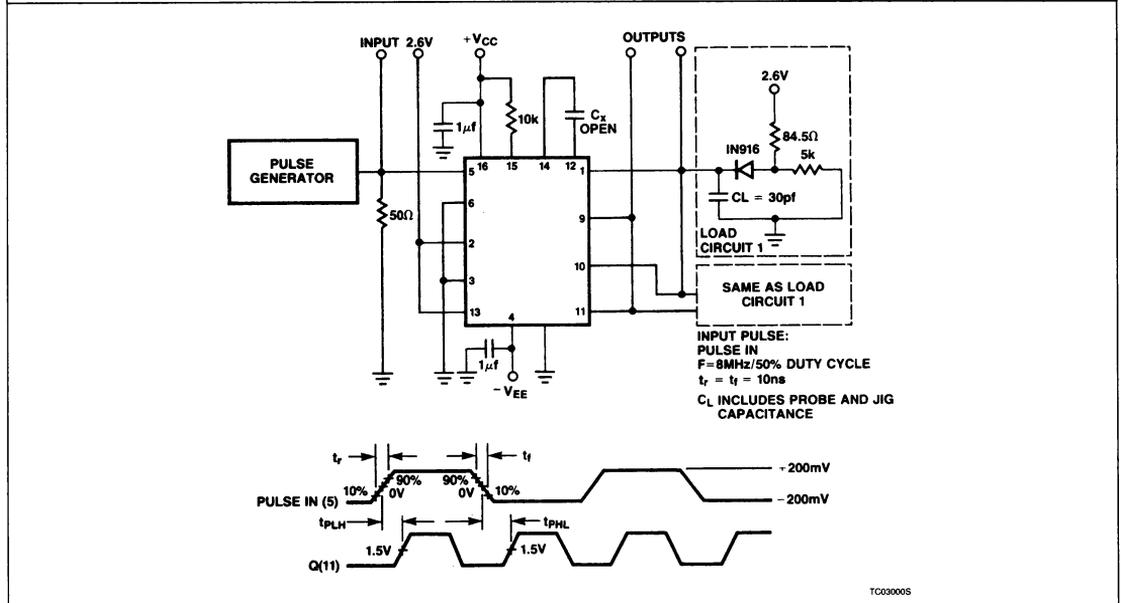


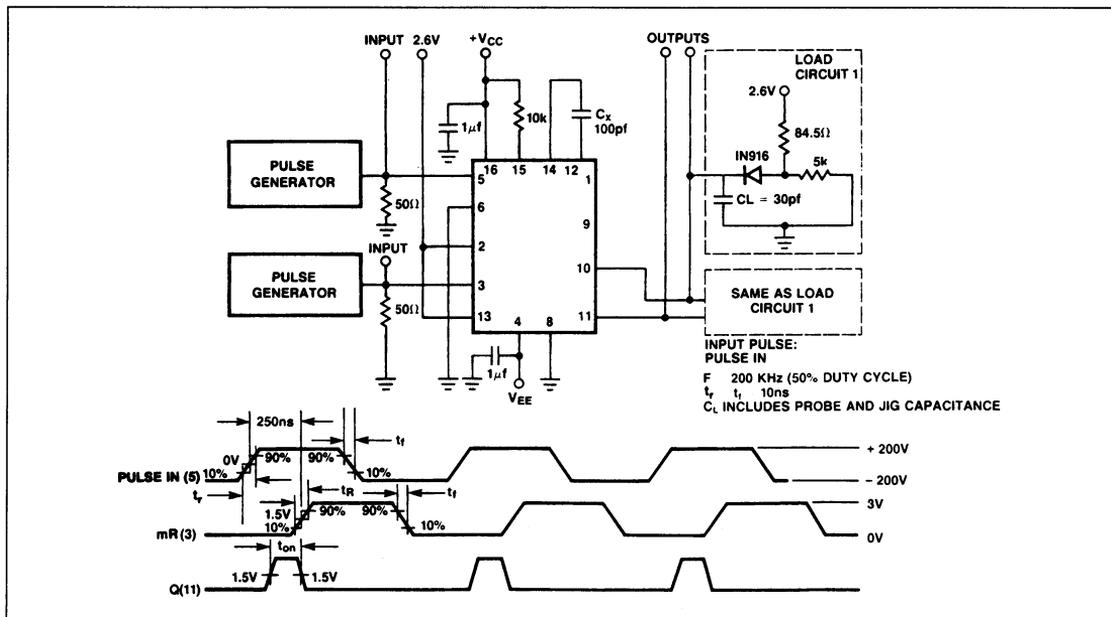
Figure 2. Propagation Delay (Input To Q, \bar{Q} Outputs)

6

Multivibrator

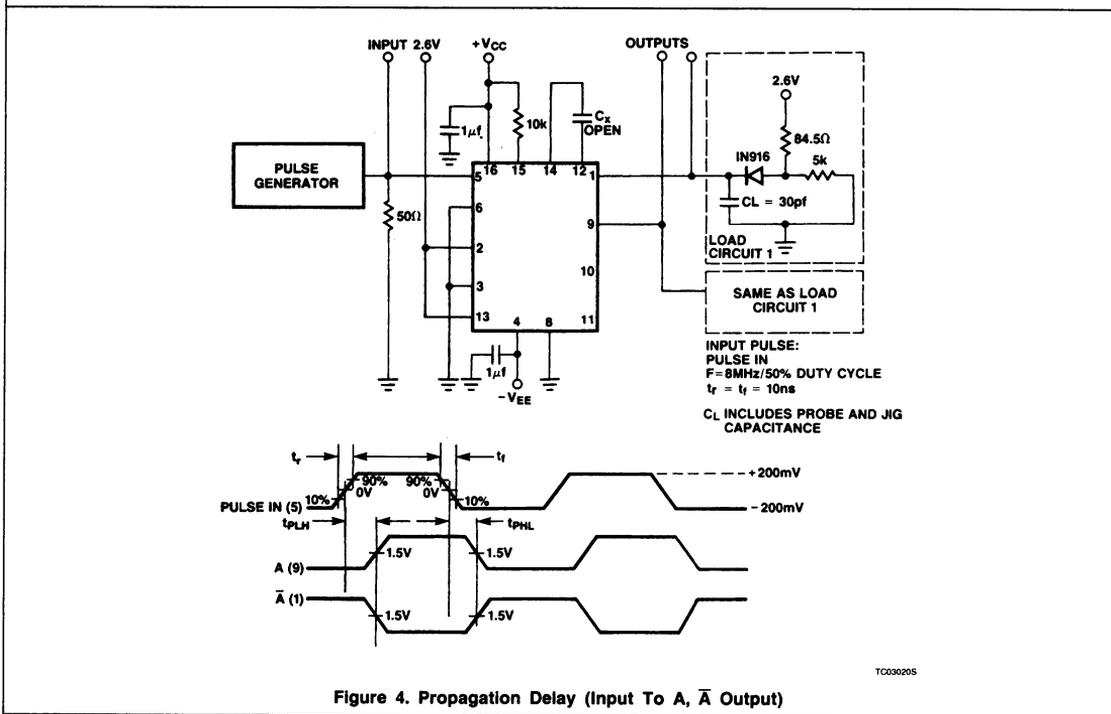
8T20

AC TEST CIRCUITS AND WAVEFORMS (Continued)



TC030105

Figure 3. Propagation Delay (MR To Q, \bar{Q})



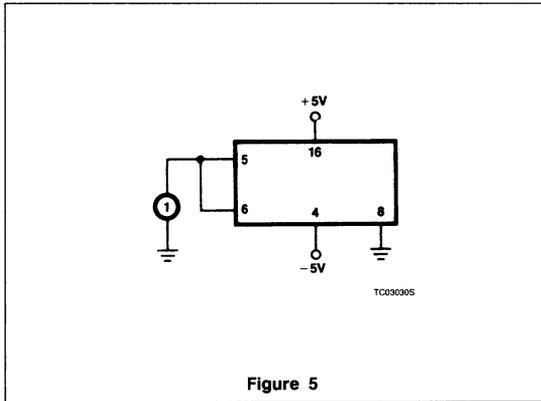
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Figure 4. Propagation Delay (Input To A, \bar{A} Output)

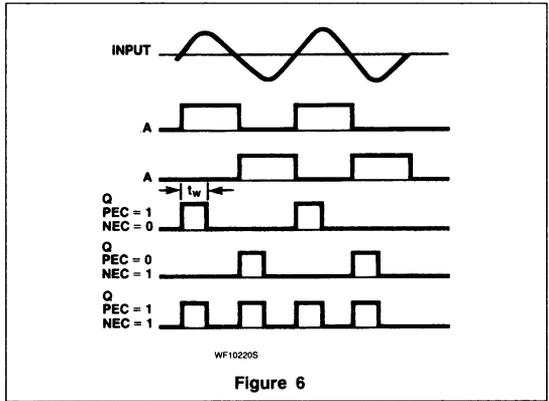
Multivibrator

8T20

INPUT BIAS CURRENT TEST CIRCUIT



INPUT/OUTPUT WAVEFORMS



8T22 Multivibrator

Retriggerable One Shot Product Specification

Logic Products

DESCRIPTION

The 8T22 is a direct pin-for-pin replacement for the 9601 retriggerable one-shot. Triggering can be performed on either the leading or falling edge of the input signal through selection of the proper input terminal.

The inputs are level-sensitive making triggering independent of signal transition times. Output pulse width is determined by external timing components (R_x and C_x) with each trigger pulse initiating a complete new-timing cycle.

For those applications where a dual retriggerable one-shot is required the Signetics 9602 should be considered.

FUNCTION TABLE

PIN NUMBER			
1	2	3	4
H → L	H	H	H
H	H → L	H	H
L	X	L → H	H
X	L	L → H	H
L	X	H	L → H
X	L	H	L → H

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T22	20ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T22N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

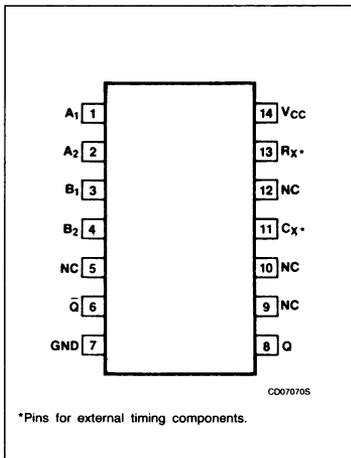
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
A_n, B_n	Input	1.5ul
C_x, R_x	Input	1.5ul
Q, \bar{Q}	Output	8ul

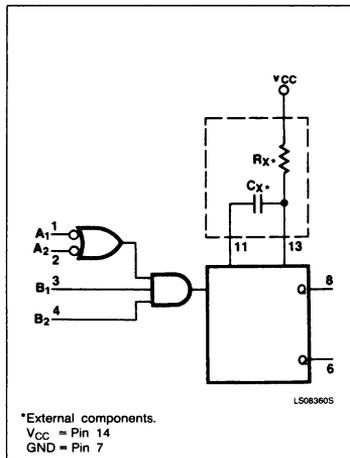
NOTE:

A unit load (ul) is $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

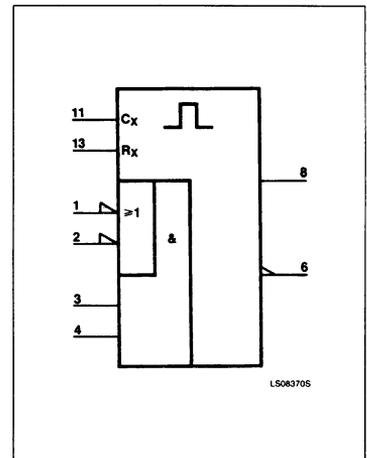
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Multivibrator

8T22

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	1.9		2.5	V
V _{IL}	LOW-level input voltage			0.9	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			960	μA
I _{OL}	LOW-level output current			12.8	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T22		UNIT	
		Min	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	1.9		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.9	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		-1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -960μA	2.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 12.8mA		0.4	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		60	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V		-1.6	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX, V _O = 0	-10	-40	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		25	mA
I _{EE}	Supply current (total)	V _{CC} = 5.25V		-28	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Multivibrator

8T22

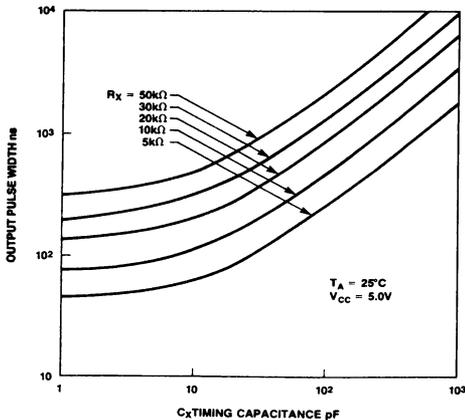
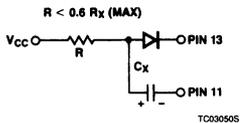
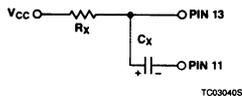
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T22			UNIT
		Min	Typ	Max	
Propagation delay Negative trigger input to true output (t_{PLH})	$R_x = 5.0\text{k}\Omega$, $C_x = 0$		25	40	ns
	$C_L = 15\text{pF}$		25	40	ns
Min. true output pulse width	$R_x = 5.0\text{k}\Omega$, $C_x = 0$ $C_L = 15\text{pF}$		45	65	ns
Pulse width variation	$R_x = 10\text{k}\Omega$, $C_x = 1000\text{pF}$	3.08	3.42	3.76	μs
Timing resistor		5.0		50	$\text{k}\Omega$
C_{Stray} - maximum allowable wiring capacitance	P13 to ground			50	pF

NOTES:

1. Positive current is defined as into the pin referenced.
2. Unless otherwise note, $10\text{k}\Omega$ resistor placed between Pin 13 and $V_{CC}(R_x)$.

OPERATION RULES



Typical Output Pulse Width Versus Timing Resistance And Capacitance For $C_x < 10^3\text{pF}$ Is Shown In The Above Graph.

1. An external resistor (R_x) and external capacitor (C_x) are required as shown in the Logic Diagram.
2. The value of R_x may vary from 5.0 to 10 $\text{k}\Omega$ (0 to 75°C).
3. C_x may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching $3.0\mu\text{A}$ or if stray capacitance from either terminal to ground is more than 50pF , the timing equations may not represent the pulse width obtained.
4. If electrolytic capacitors are to be used, the following configurations are recommended:
 - A. For use with low leakage electrolytic capacitors. The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than $3\mu\text{A}$, and the inverse capacitor leakage at 1.0 volt is less than $5\mu\text{A}$ over the operational temperature range, and Rule 3 above is satisfied.
 - B. Use with high inverse leakage current electrolytic capacitors. The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

$$t \approx 0.3 RC_x$$

The output pulse with (t) is defined as follows:

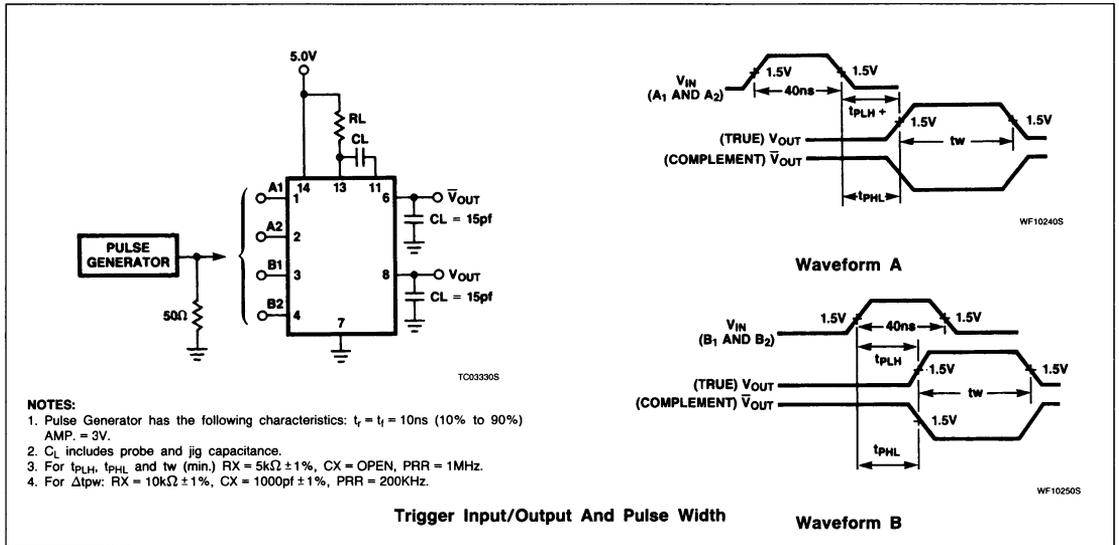
$$t = 0.32 R_x C_x \left[1 + \frac{0.7}{R_x} \right]$$

Where R_x is in $\text{k}\Omega$, C_x is in pF, t is in ns; for $C_x < 10^3\text{pF}$.

Multivibrator

8T22

AC TEST CIRCUITS AND WAVEFORMS



8T24 Line Receiver

Triple Line Receiver with Hysteresis
Product Specification

Logic Products

FEATURES

- Built-in input threshold hysteresis*
- High speed: $t_{PHL} = t_{PLH} = 20\text{ns}$ (typical)
- Each channel can be strobed independently
- Fanout of ten (10) with standard TTL integrated circuits
- Input gating is included with each line receiver for increased application flexibility
- Operation from a single +5V Power Supply

*Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System (360, System/370 I/O Interface Specification [IBM Specification GA 22-6974-0]): Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T24	20ns (t_{PLH})	
	20ns (t_{PHL})	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$
Plastic DIP	N8T24N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
R	Input	4.3ul
S, A, B	Input	1ul
f	Output	8ul

NOTE:

A unit load (ul) is $40\mu\text{A } I_{IH}$ and $-1.6\text{mA } I_{IL}$.

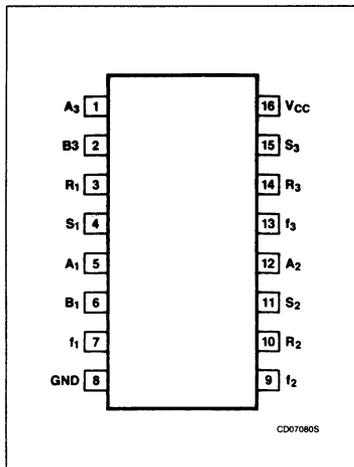
0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The

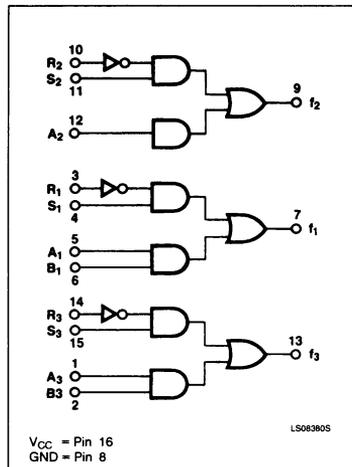
8T24 will also withstand an input of -0.15V with power on or off.

The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

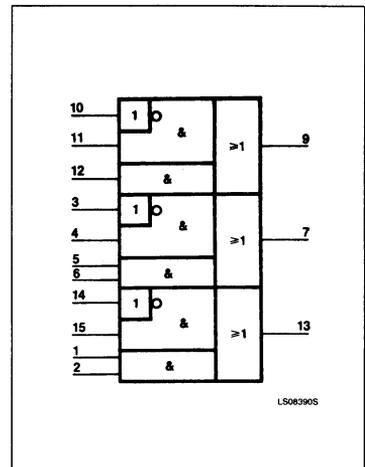
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Line Receiver

8T24

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	V
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0		2.5	V
V_{IL}	LOW-level input voltage	1.1		1.5	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	HIGH-level output current			-800	μ A
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T24		UNIT		
		Min	Max			
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		1.7	V	
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			0.7	V
V_{IK}	Input clamp diode voltage	$V_{CC} = \text{MIN}$, $I_{IK} = -12\text{mA}$			-1.5	V
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -800\mu\text{A}$		2.6		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16\text{mA}$			0.4	V
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 4.5\text{V}$, pins S, A, B			40	μ A
		$V_{CC} = \text{MAX}$, $V_I = 4.5\text{V}$, pin R			170	μ A
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$			-1.6	mA
I_{OS}	Short-circuit output current ²	$V_{CC} = \text{MAX}$		-50	-100	mA
I_{CC}	Supply current (total)	$V_{CC} = 5.25\text{V}$			80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS				LIMITS			UNITS
	R	S	A	B	Min	Typ	Max	
t_{PHL}						20	30	ns
t_{PLH}						20	30	ns
Hysteresis ¹		4.5V	0V	0V	0.2	0.4		V

NOTE:

- Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "0" to "1" state and the level at which the output begins to go from "1" to "0".

Line Receiver

8T24

AC TEST CIRCUIT AND WAVEFORMS

Input Pulse:
 Amplitude = 2.6V
 Pulse width = 200ns
 (50% Duty Cycle)
 $t_r = t_f = 5ns$ (10% to 90%)

WF102805

TC030605

3 Receivers in the package.
 Test each Receiver using switch positions as shown in Table 1.

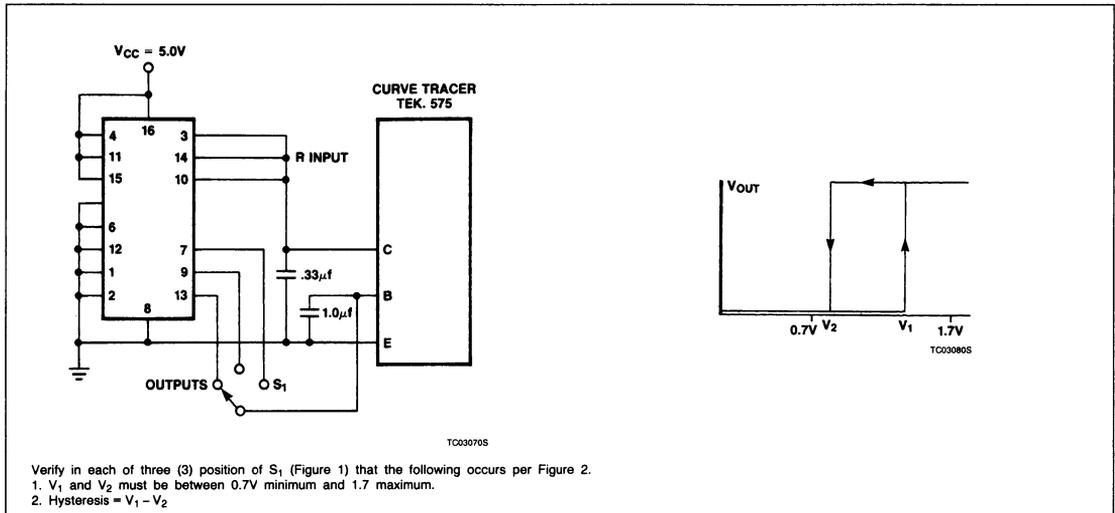
Table 1

RECEIVER NO.	POSITION	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

Line Receiver

8T24

HYSTERESIS TEST CIRCUIT



8T26A, 28 Bus Transceivers

3-State Quad Bus Transceiver Product Specification

Logic Products

FEATURES

- High speed Schottky quad transceivers
- 48mA LOW-state drive
- 200 μ A bus loading
- Ideal for:
 - Half-duplex data transmission
 - Memory interface buffers
 - Data routing in bus oriented systems
 - High current drivers
 - MOS/CMOS-to-TTL interface

DESCRIPTION

The 8T26A/28 consists of four pairs of 3-state logic elements configured as quad bus drivers/receivers, along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

Both the driver and receiver gates have 3-State outputs and low-current PNP

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T26A	7ns	48mA
N8T28	10ns	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T26AN, N8T28N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

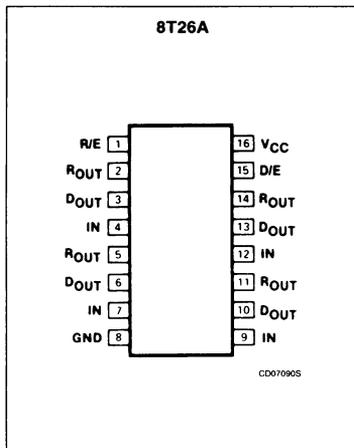
PINS	DESCRIPTION	N8T	S8T
I _N	Input	0.5Sul	0.5Sul
D/E, R/E	Inputs	0.5Sul	0.5Sul
D _{OUT}	Output	24Sul	16Sul
R _{OUT}	Output	10Sul	6Sul

NOTE:

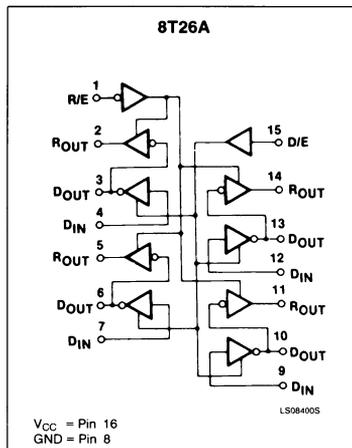
A unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} inputs. 3-State outputs provide the high switching speeds of totem-pole TTL circuits while offering the bus capability of

open collector gates. PNP inputs reduce input loading to 200 μ A maximum.

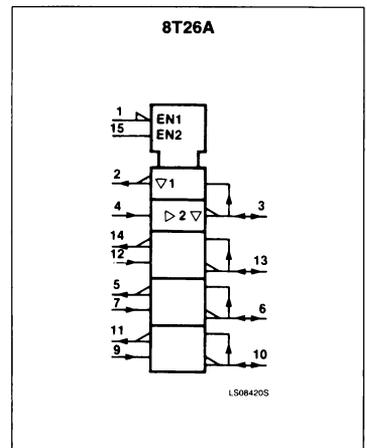
PIN CONFIGURATION



LOGIC SYMBOL



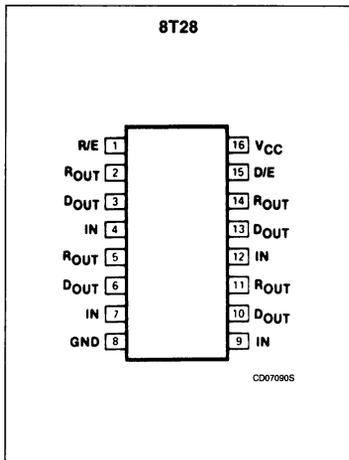
LOGIC SYMBOL (IEEE/IEC)



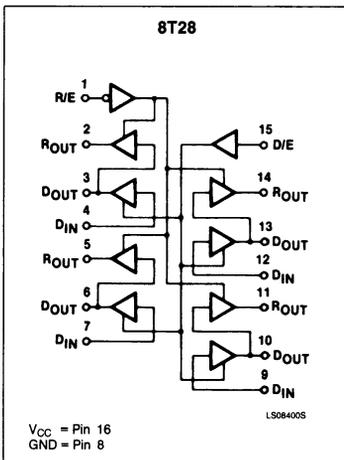
Bus Transceivers

8T26A, 28

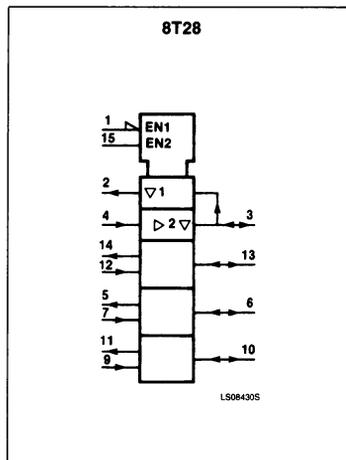
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	8T	N8T	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
I _{OL} Continuous	100	100	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

6

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-18	mA
I _{OH} HIGH-level output current			-10	mA
I _{OL} LOW-level output current			48	mA
			20	mA
T _A Operating free-air temperature	0		70	°C

Bus Transceivers

8T26A, 28

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	N8T26A, N8T28		S8T26A, S8T28		UNIT	
		Min	Max	Min	Max		
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		2.0		V	
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage		0.8		0.8	V	
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -18mA		-1.2		-1.2	V	
V _{BD} Input breakdown voltage	V _{CC} = MAX, I _I = 1mA	5.5		5.5		V	
V _{OH} HIGH-level output voltage, Driver outputs	V _{CC} = MIN	I _{OH} = -10mA	2.4			V	
		I _{OH} = -2mA			2.4	V	
V _{OH} HIGH-level output voltage, Receiver outputs	V _{CC} = MIN, I _{OH} = -100μA	3.25				V	
	V _{CC} = 5.0V, I _{OH} = -100μA			3.0		V	
V _{OL} LOW-level output voltage, Driver outputs	V _{CC} = MIN	I _{OL} = 48mA		0.5		V	
		I _{OL} = 32mA			0.5	V	
V _{OL} LOW-level output voltage, Receiver outputs	V _{CC} = MIN	I _{OL} = 20mA		0.5		V	
		I _{OL} = 12mA			0.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V		100		100	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.5V		-100		-100	μA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		25		25	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V	Driver, receiver	-200		-200	μA	
		Disabled	-25		-25	μA	
I _{OS} Short-circuit output current ²	V _{CC} = MAX	Driver	-50	-150	-50	-150	mA
		Receiver	-30	-100	-30	-100	mA
I _{CC} Supply current	V _{CC} = MAX	8T26A		87		87	mA
		8T28		110		110	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

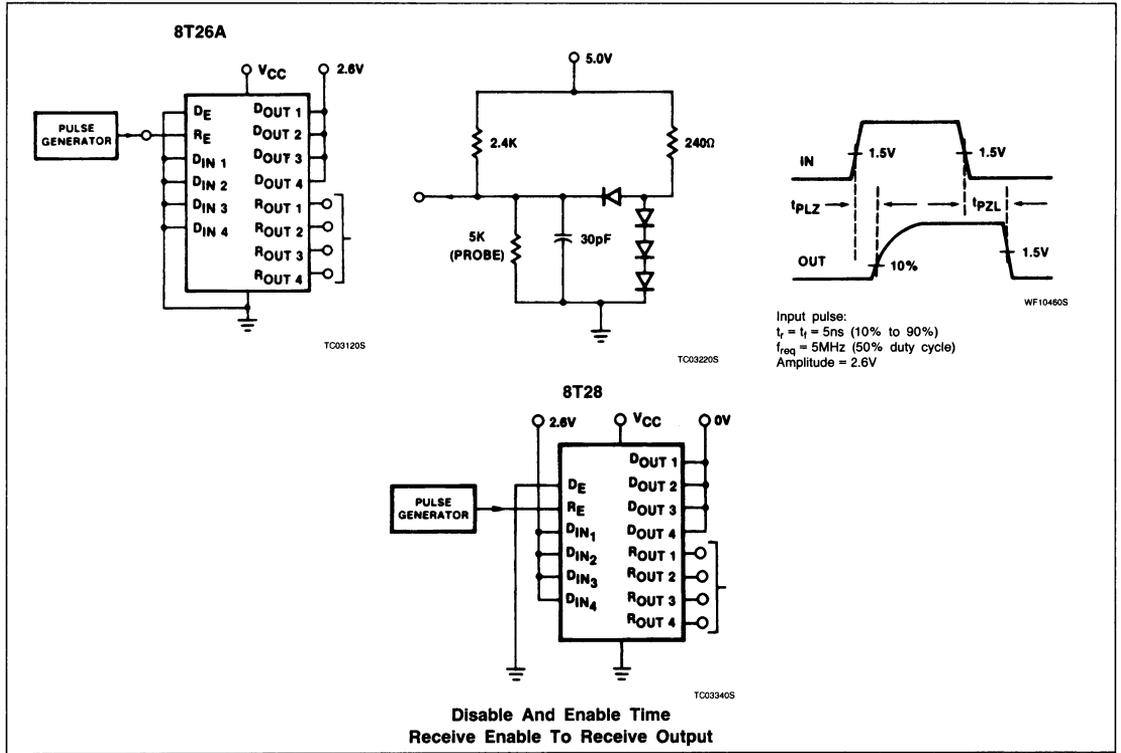
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T26A		8T28		UNIT
		Min	Max	Min	Max	
t _{PHL} Propagation delay, D _{OUT} to R _{OUT}	C _L = 30pF		14		17	ns
t _{PHL} Propagation delay, D _{IN} to D _{OUT}	C _L = 300pF		14		17	ns
t _{PLH} Propagation delay, D _{OUT} to R _{OUT}	C _L = 30pF		14		17	ns
t _{PLH} Propagation delay, D _{IN} to D _{OUT}	C _L = 300pF		14		17	ns
t _{PZL} Data enable to data output, high Z to 0	C _L = 300pF		25		28	ns
t _{PLZ} Data enable to data output, 0 to high Z	C _L = 300pF		20		23	ns
t _{PZL} Receive enable to receive output, high Z to 0	C _L = 30pF		20		23	ns
t _{PLZ} Receive enable to receive output, 0 to high Z	C _L = 30pF		15		18	ns

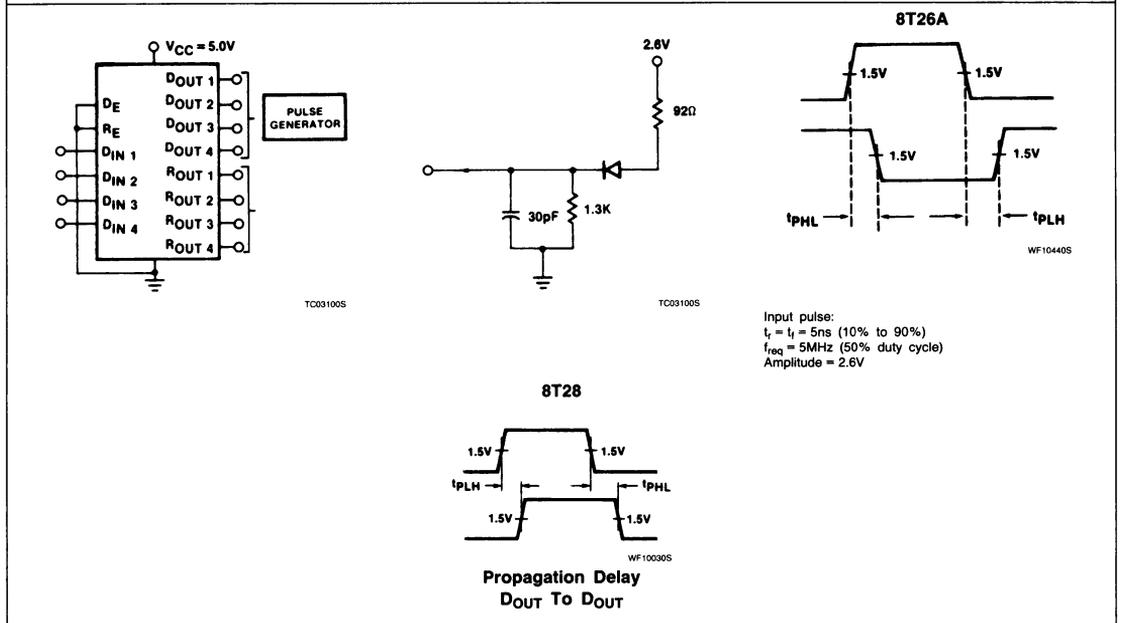
Bus Transceivers

8T26A, 28

TEST CIRCUITS AND WAVEFORMS



Disable And Enable Time
 Receive Enable To Receive Output



Bus Transceivers

8T26A, 28

TEST CIRCUITS AND WAVEFORMS (Continued)

8T26A

TC03210S

8T28

TC03200S

WF11450S

Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 $f_{req} = 5\text{MHz}$ (50% duty cycle)
 Amplitude = 2.6V

8T26A

TC03140S

8T28

TC03150S

WF10440S

Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 $f_{req} = 5\text{MHz}$ (50% duty cycle)
 Amplitude = 2.6V

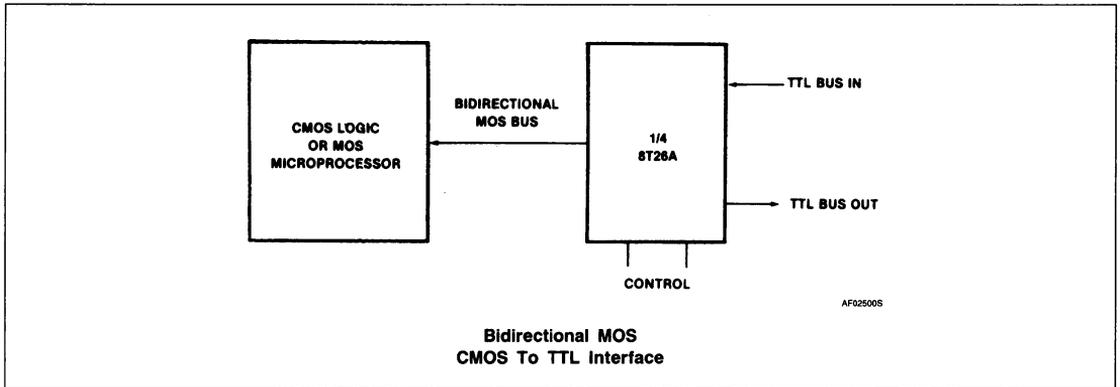
WF10030S

Propagation Delay
 D_{IN} To D_{OUT}

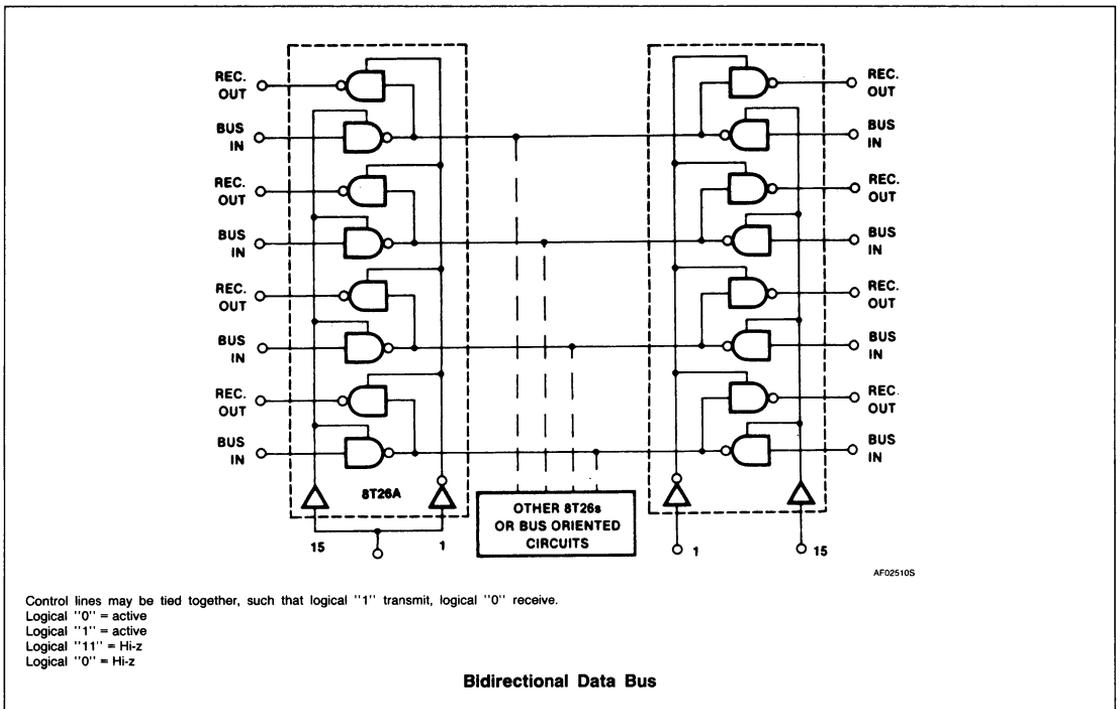
Bus Transceivers

8T26A, 28

TYPICAL APPLICATION



TYPICAL APPLICATION



6

8T37 Bus Receiver

Hex Bus Receiver with Hysteresis — Schmitt Trigger
Product Specification

Logic Products

DESCRIPTION

The 8T37 is a hex bus receiver with hysteresis organized as two triple receivers with separate disable lines for each group. Typically the devices may be used in bus organized data transmission systems interconnected by terminated lines. The low input current requirement allows several drivers and receivers to communicate over a common bus in "party line" fashion. A power-up or power-down sequence of the receiver will not affect the bus. Built in hysteresis provides maximum noise immunity and makes the 8T37 also an ideal Schmitt trigger in those applications where the non-linear input characteristics of standard TTL are undesirable.

Low input current requirements make the nex-inverter inputs compatible with MOS/CMOS in addition to DTL/TTL. All inputs have clamping diodes to simplify systems design. The receiver outputs as well as the disable inputs are TTL/DTL compatible.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T37	10ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T37N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

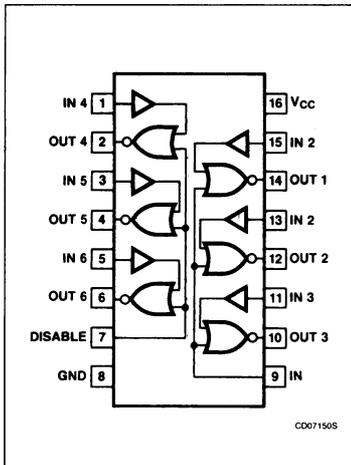
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
Disable	Input	2ul
IN (Receiver)	Input	1.3ul
OUT	Output	8ul

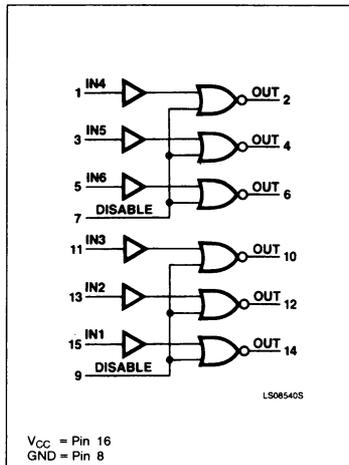
NOTE:

A unit load (ul) is $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} .

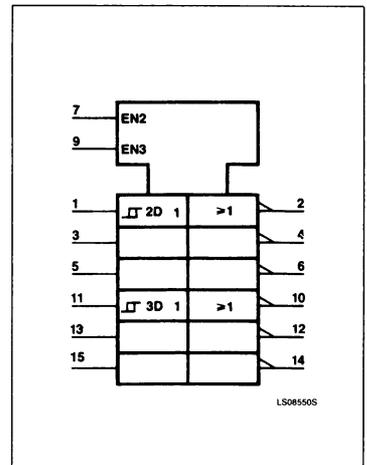
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Bus Receiver

8T37

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{OL}	Continuous		mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
HIGH-level input voltage, Receiver Disable	1.8 2.0		2.5	V
LOW-level input voltage, Receiver Disable	1.1		1.5 0.8	V
I _{IK} Input clamp current			-12	
I _{OH} HIGH-level output current			-400	μA
I _{OL} LOW-level output current			16	mA
T _A Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		8T37		UNIT
			Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	Receiver Disable	1.8 2.0	2.5	V
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	Receiver Disable	1.1	1.5 0.8	V
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		-1.5 1.5V	V	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -400μA		2.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, I _{OL} = 16mA			0.4	V
I _{IH} HIGH-level input current	V _{CC} = MAX V _{IN} = 2.4V V _{CC} = 0	Receiver		50	
		Disable		80	μA
		Others		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX V _{IN} = 0.4V	Receiver		-50	μA
		Disable		-3.2	mA
I _{OS} Short-circuit output current ²	V _{CC} = MAX		-18	-55	mA
I _{CC} Supply current (total)	V _{CC} = 5.25V			60	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

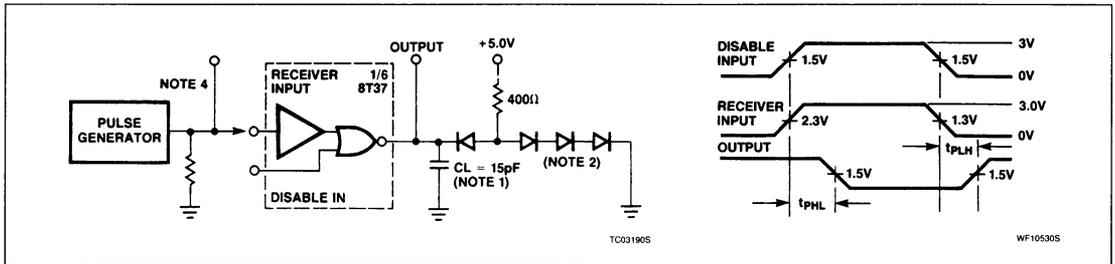
Bus Receiver

8T37

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITION	LIMITS			UNIT
		Min	Typ	Max	
Propagation delays					
Receiver	t_{PHL}		10	30	ns
	t_{PLH}		20	30	ns
Disable	t_{PHL}		9	15	ns
	t_{PLH}		11	15	ns

AC TEST CIRCUIT AND WAVEFORMS



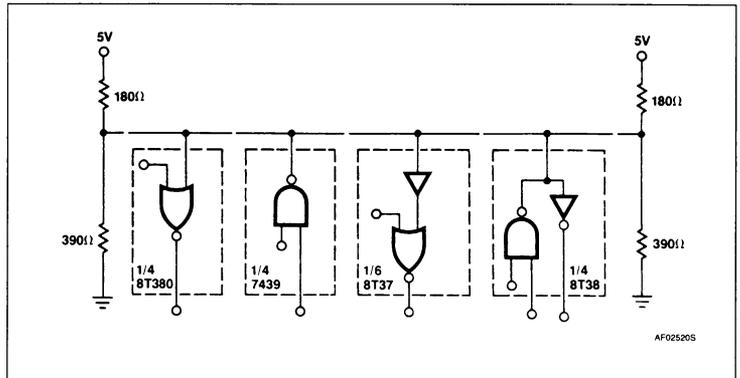
NOTES:

- Including probe and jig capacitance
- All diodes are 1N3064
Pulse generator characteristics
P.A. = 3.5V
- $Z_{OUT} = 50\Omega$ $P_{RR} = 1\text{MHz}$
 $t_r = t_f \leq 10\text{ns}$ (10% to 90%) Duty
Cycle = 50%
- When testing receiver, Disable = 0;
when testing disable, Receiver = 0.

*To be announced.

Each terminator is 120Ω the venins equivalent circuit. Using fl at ribbon a maximum reasonable length is 50 ft. from which the combined length of all taps or stubs should be subtracted.

TYPICAL APPLICATION



8T38 Bus Transceiver

Quad Bus Transceiver (Open Collector)
Product Specification

Logic Products

DESCRIPTION

The 8T38 is a quad bus transceiver with a common two input disable control for the drivers. Open collector driver outputs together with low input requirements for the receivers offer extreme versatility in low cost bus organized systems.

Busses may be terminated at both ends such that up to 100 driver/receiver pairs can utilize a common data bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus when $V_{CC} = 0$.

In those applications where only bus receiver are required the 8T380 quad bus receiver should be considered.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T38	19ns (t_{PHL})	
	23ns (t_{PLH})	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T38N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
Bus	Receiver input	1.2ul
Disable	Disable input	2.5ul
Bus	Driver output	31ul
Out	Receiver output	10ul

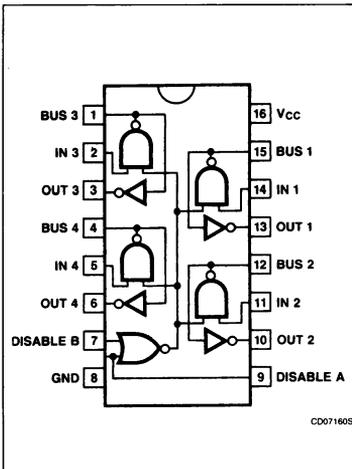
NOTE:

A unit load (ul) is $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

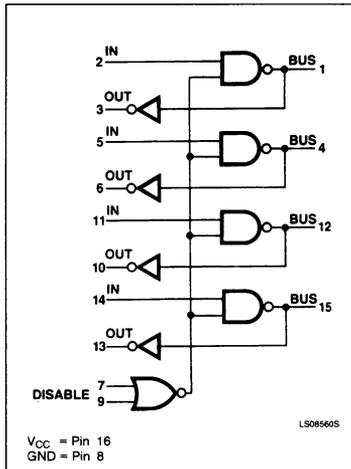
FUNCTION TABLE

MODE	DISABLE	DISABLE	DRIVER	BUS	RECEIVER
	A	B	In		Out
Receive	1	X	X	1	0
Receive	X	1	X	1	0
Drive	0	0	1	0	1
Drive	0	0	0	1	0

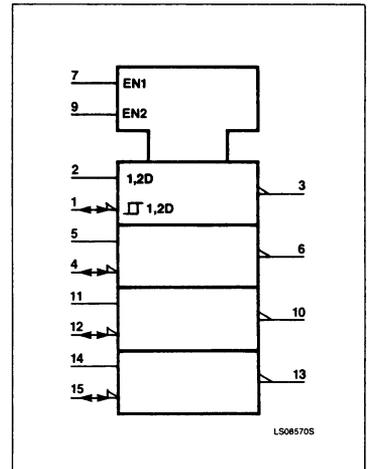
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Bus Transceiver

8T38

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage, disable	2.0		2.5	V
V _{IH}	HIGH-level input voltage, receiver	1.8		2.5	V
V _{IL}	LOW-level input voltage, disable			0.8	V
V _{IL}	LOW-level input voltage, receiver	1.1		1.5	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current, receiver			-100	mA
I _{OL}	LOW-level output current, driver			50	mA
I _{OL}	LOW-level output current, receiver			16	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T38		UNIT	
		Min	MAX		
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	Receiver	1.8	2.5	V
		Disable	2.0		
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	Receiver	1.1	1.5	V
		Disable		0.8	
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA			-1.5	V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -5.2mA		2.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN	I _{OL} = 50mA	Driver	0.5	V
		I _{OL} = 16mA	Receiver	0.4	
I _{IH} HIGH-level input current	V _{CC} = MAX V _{IH} = 2.4V	Receiver		100	μA
		Disable		50	
	V _{CC} = 0	Others		100	
I _{IL} LOW-level input current	V _{CC} = MAX V _{IN} = 0.4V	Receiver		50	μA
		Disable		-1.6	mA
I _{OS} Short-circuit output current ²	V _{CC} = MAX		18	55	mA
I _{CC} Supply current total	V _{CC} = 5.25V			60	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

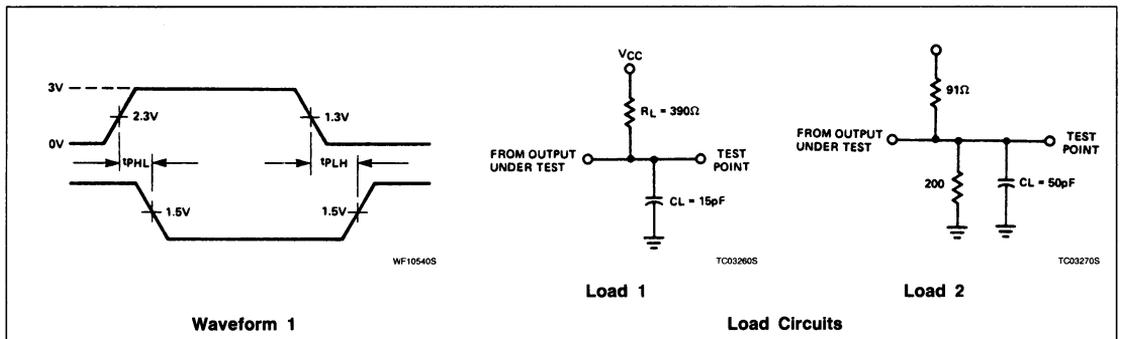
Bus Transceiver

8T38

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T			UNIT
		Min	Typ	Max	
t_{PHL} Propagation delay Disable bus	Load 2 $V_{IN} = 0\text{V to } 3\text{V}$ Measured from $V_{IN} = 1.5\text{V to } V_{BUS} = 1.5\text{V}$	11	19	30	ns
t_{PLH} Disable to bus		15	23	35	ns
t_{PHL} Driver to bus	Load 1 waveform 1	5	12	20	ns
t_{PLH} Driver to bus		5	12	25	ns
t_{PHL} Bus to receiver		5	14	25	ns
t_{PLH} Bus to receiver		12	27	40	ns

SWITCHING PARAMETERS MEASUREMENT INFORMATION



8T95, 96, 97, 98 Hex Buffers/Inverters

High Speed Hex 3-State Buffers
High Speed Hex 3-State Inverters
Product Specification

Logic Products

DESCRIPTION

Each of the 3-state bus interface elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL bus levels. For maximum systems flexibility, the 8T95 and 8T97 do so without logic inversion, whereas the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

FUNCTION TABLE — 8T95

INPUTS			OUTPUT
DIS ₁	DIS ₂	I	Y
L	L	L	L
L	L	H	H
X	H	X	(Z)
H	X	X	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

FUNCTION TABLE — 8T96

INPUTS			OUTPUT
DIS ₁	DIS ₂	I	\bar{Y}
L	L	L	H
L	L	H	L
X	H	X	(Z)
H	X	X	(Z)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T95	8ns	65mA
N8T96	6.5ns	59mA
N8T97	8ns	65mA
N8T98	6.5ns	59mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T95N, N8T96N N8T97N, N8T98N
Plastic SO	N8T97N, N8T98D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
DIS	Input	1Sul
I	Input	1Sul
Y	Output	24Sul

NOTE:

A unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{L} .

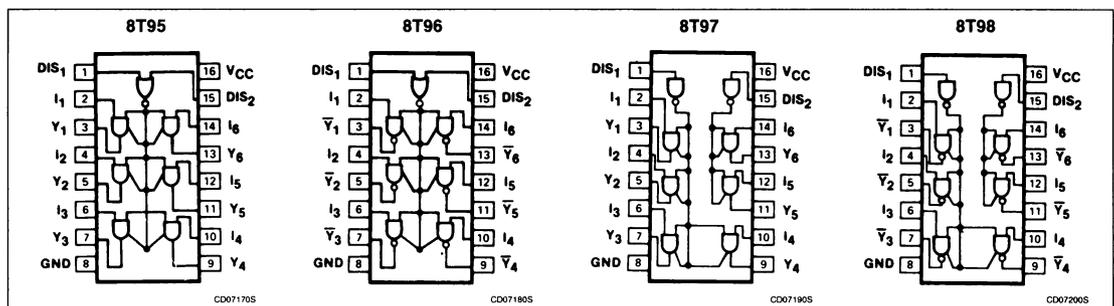
FUNCTION TABLE — 8T97

INPUTS		OUTPUT
DIS	I	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE — 8T98

INPUTS		OUTPUT
DIS	I	\bar{Y}
L	L	H
L	H	L
H	X	(Z)

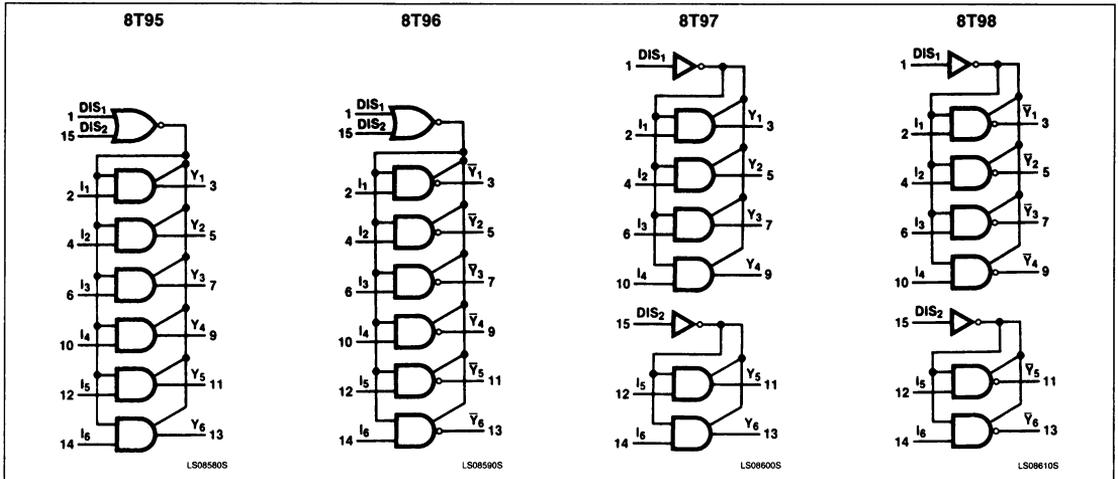
PIN CONFIGURATION



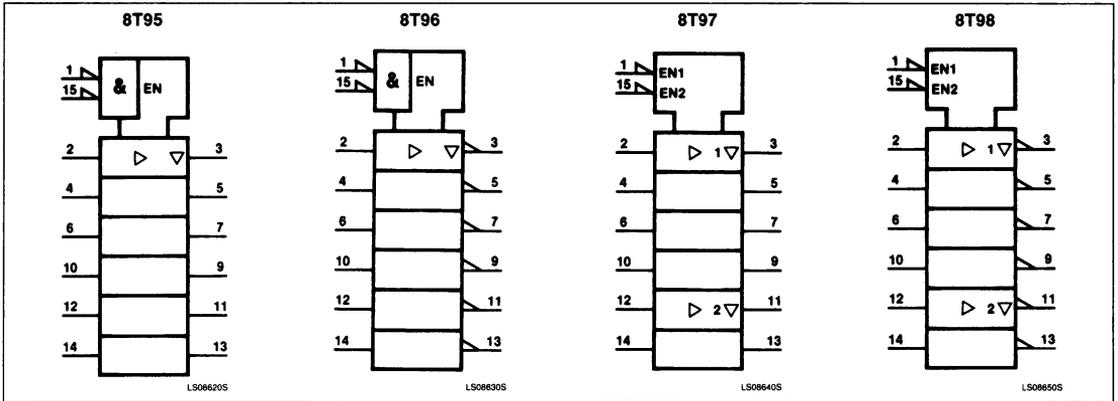
Hex Buffers/Inverters

8T95, 96, 97, 98

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8T	N8T	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +5	mA
I _{OL}	Continuous	100	100	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

6

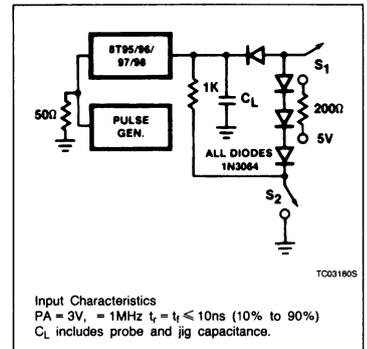
Hex Buffers/Inverters

8T95, 96, 97, 98

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IH}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-5.2	V
I _{OL}	LOW-level output current			48	mA
T _A	Operating free-air temperature	0		70	°C

TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T95/97		8T96/98		UNIT				
		Min	Max	Min	Max					
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage				2.0		2.0		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage					0.8		0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA					-1.5		-1.5	V
V _{BD}	Input breakdown voltage	V _{CC} = MAX, I _I = 1mA				5.5		5.5		V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -5.2mA				2.4		2.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 48mA					0.5 ³		0.5 ³	V
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V					40		40	μA
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.5V					-40		-40	μA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V					40		40	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.5V					Disable = 0.5V		-400	μA
							Disable = 2.0V		-40	μA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX				-40	-115	-40	-115	mA
I _{CC}	Supply current (total)	V _{CC} = MAX					98		89	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for S8T at T_A = +125°C only.

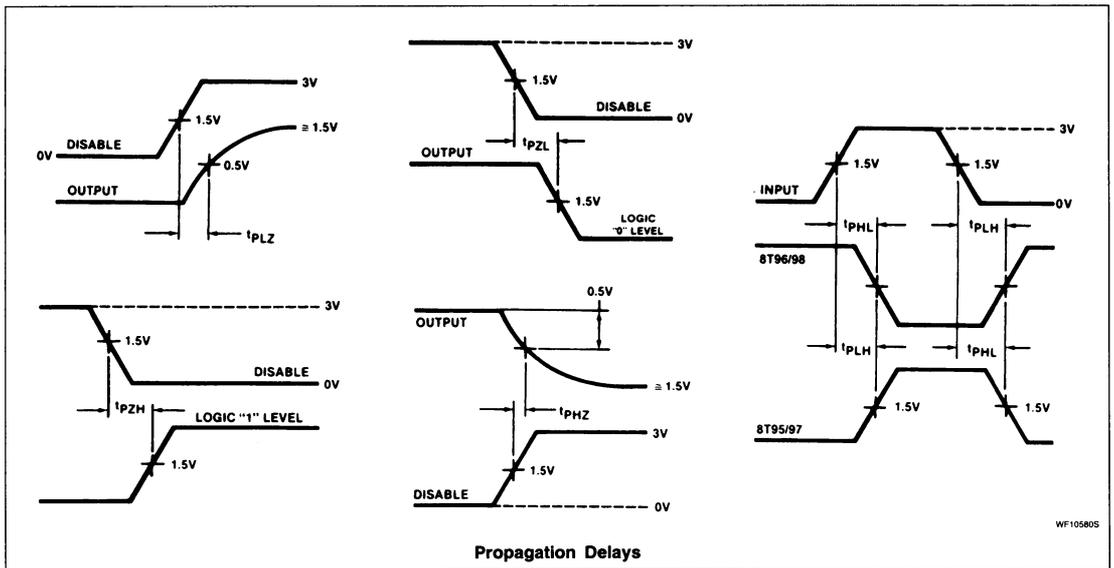
Hex Buffers/Inverters

8T95, 96, 97, 98

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T95/97		8T96/98		UNIT
		$R_L = 200\Omega$		$R_L = 200\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay Data inputs to data outputs	S_1, S_2 are closed, $C_L = 50\text{pF}$		12		11	ns
t_{PHL} Propagation delay Data inputs to data outputs	S_1, S_2 are closed, $C_L = 50\text{pF}$		13		10	ns
t_{PZH} Disable to outputs High Z to logic "1"	S_1 is open, S_2 is closed, $C_L = 50\text{pF}$		25		22	ns
t_{PZL} Disable to outputs High Z to logic "0"	S_1 is closed, S_2 is open, $C_L = 50\text{pF}$		25		24	ns
t_{PHZ} Disable to outputs Logic "1" to high Z	S_1, S_2 are closed, $C_L = 5\text{pF}$		10		10	ns
t_{PLZ} Disable to outputs Logic "0" to high Z	S_1, S_1 are closed, $C_L = 5\text{pF}$		12		16	ns

AC WAVEFORMS



8T125 Transceiver

Octal 3-State Transceiver
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- Pin compatible with 74LS245

DESCRIPTION

The 8T125 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable input for easy cascading and a Send/Receive input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T125	7.5ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T125N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

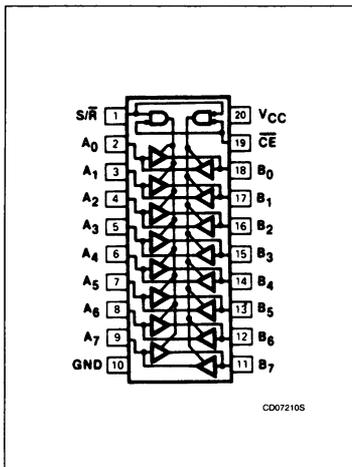
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T125
All	Inputs	1LSul
All	Outputs	30LSul

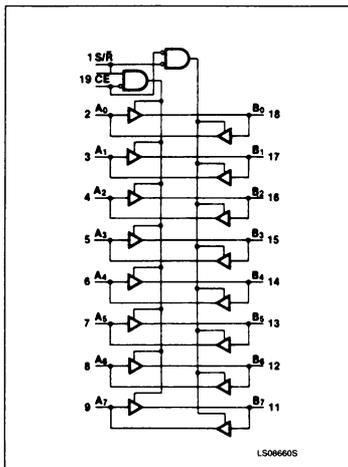
NOTE:

A unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

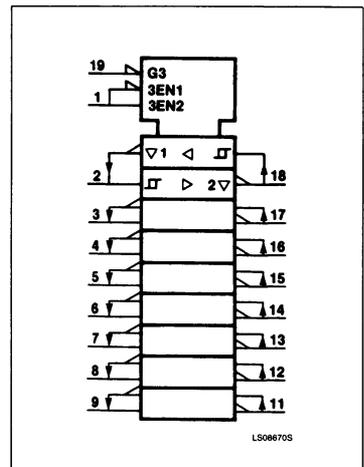
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceiver

8T125

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/\overline{R}	A_n	B_n
L	L	$A = \overline{B}$	INPUTS
L	H	INPUT	$B = \overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level

L = LOW voltage level

X = Don't care

(Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		N8T	UNIT		
V_{CC}	Supply voltage	7.0	7.0	V	
V_{IN}	Input voltage	Transceiver inputs	-0.5 to +5.5	-0.5 to +5.5	V
		Non-transceiver inputs	-0.5 to +7.0	-0.5 to +7.0	V
I_{OL}	Continuous	50	50	mA	
I_{IN}	Input current	-30 to +1	-30 to +1	mA	
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V	
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-15	mA
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

Transceiver

8T125

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	8T125		UNIT
			Min	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2		V
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V
V_{IK}	Input clamp diode voltage	$V_{CC} = \text{MIN}$, $I_{IK} = -18\text{mA}$		-1.5	V
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -3.0\text{mA}$	2.4	V
			$I_{OH} = -15\text{mA}$	2.0	V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 12\text{mA}$	0.4	V
			$I_{OL} = 24\text{mA}$	0.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, $V_O = 2.4\text{V}$		20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, $V_O = 0.4\text{V}$		-200	μA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4\text{V}$		20	μA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ transceiver inputs	100	μA
			$V_I = 7.0\text{V}$ non-transceiver inputs	100	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$		-200	μA
I_{OS}	Short-circuit output current ²	$V_{CC} = \text{MAX}$	-40	-120	mA
I_{CCH}	Supply current HIGH	$V_{CC} = \text{MAX}$, outputs HIGH		70	mA
I_{CCL}	Supply current LOW	$V_{CC} = \text{MAX}$, outputs LOW		90	mA
I_{CCZ}	Supply current 'off'	$V_{CC} = \text{MAX}$, outputs 'off'		95	mA

NOTE:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC \text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

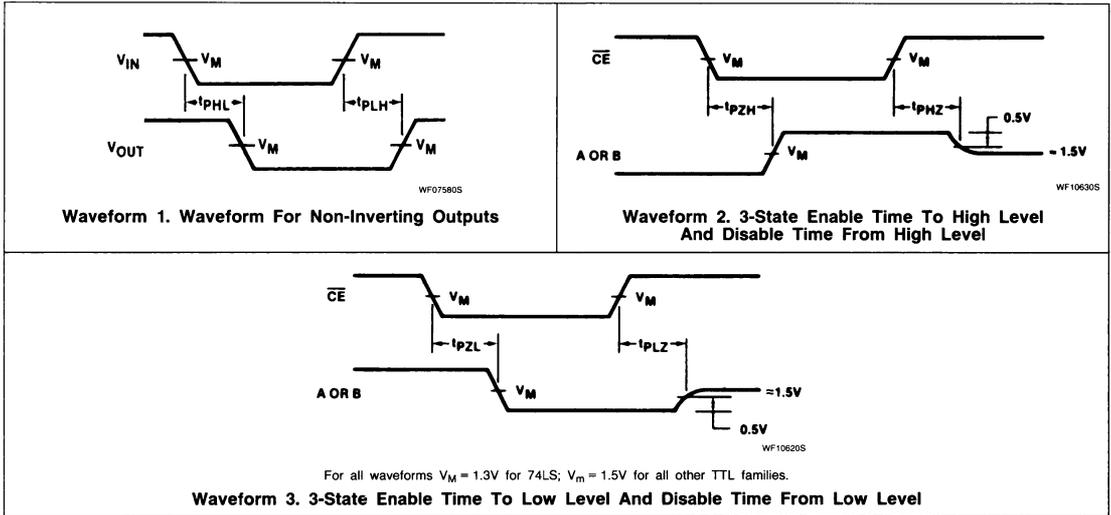
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	8T		UNIT
			$R_L = 667\Omega$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Input to output	Waveform 1, $C_L = 45\text{pF}$		12 12	ns
t_{PZH}	Enable to HIGH	Waveform 2, $C_L = 45\text{pF}$		40	ns
t_{PZL}	Enable to LOW	Waveform 3, $C_L = 45\text{pF}$		40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5\text{pF}$		25	ns

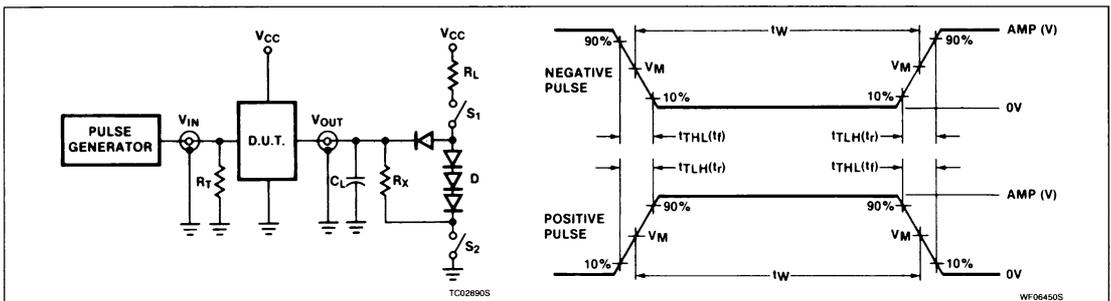
Transceiver

8T125

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



6

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

8T126, 127, 128, 129 Transceivers

Quad, 3-State Transceivers
Product Specification

Logic Products

DESCRIPTION

The 8T126 through 8T129 are quad transceivers designed to handle many bus interface applications. The devices feature 3-State outputs on both send and receive buffers, and pnp transistors on all inputs to reduce input LOW loading requirements.

The 8T126 and 8T128 feature a 3.4V minimum V_{OH} level on the receiver for MOS interface applications. The send and receive buffers have separate Enable inputs for independent control.

The 8T127 and 8T129 feature full 24mA drive in both send and receive buffers. These devices have a common Chip Enable input for easy cascading and a Send/Receive input for direction control.

FUNCTION TABLES

8T126

INPUTS			RECVR. OUT	BUS I/O
SE	RE	D_n	A_n	B_n
L	L	X	$A = \bar{B}$	Inputs
L	H	X	(Z)	(Z)
H	H	L	(Z)	H
H	H	H	(Z)	L
H	L	L	L	H
H	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(X) = HIGH impedance "off" state

8T127

INPUTS			RECVR. OUT	BUS I/O
SE	S/R	D_n	A_n	B_n
L	L	X	$A = \bar{B}$	Inputs
L	H	L	(Z)	H
L	H	H	(Z)	L
H	X	X	(Z)	(Z)

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T126N, N8T127N N8T128N, N8T129N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
All	Input	1ul
All	Output	60ul

NOTE:

A unit load (ul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

8T128

INPUTS			RECVR. OUT	BUS I/O
SE	RE	D_n	A_n	B_n
L	L	X	$A = B$	Inputs
L	H	X	(Z)	(Z)
H	H	L	(Z)	L
H	H	H	(Z)	H
H	L	L	L	L
H	L	H	H	H

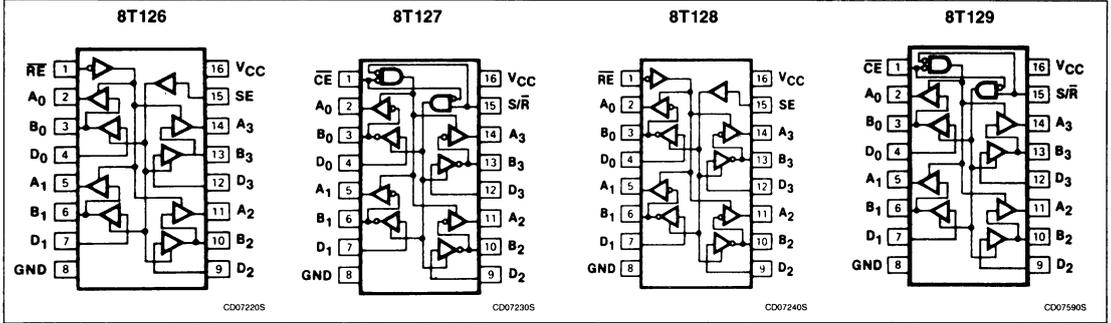
8T129

INPUTS			RECVR. OUT	BUS I/O
CE	S/R	D_n	A_n	B_n
L	L	X	$A = B$	Inputs
L	H	L	(Z)	L
L	H	H	(Z)	H
H	X	X	(Z)	(Z)

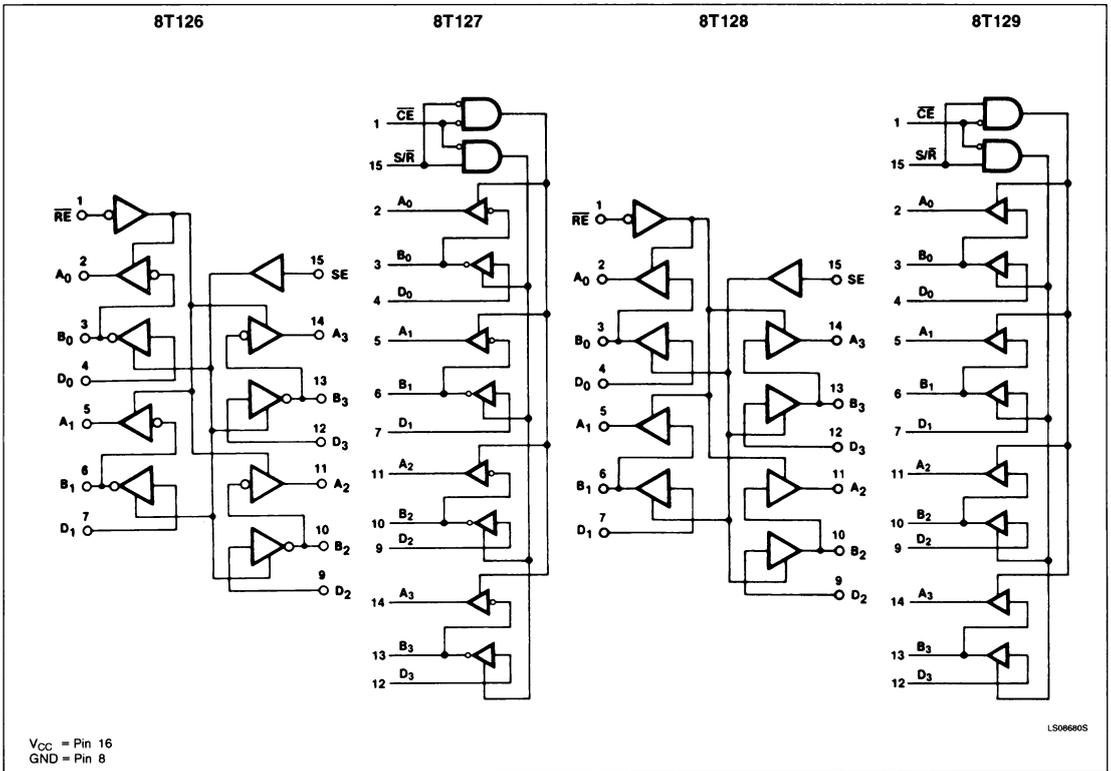
Transceivers

8T126, 127, 128, 129

PIN CONFIGURATION



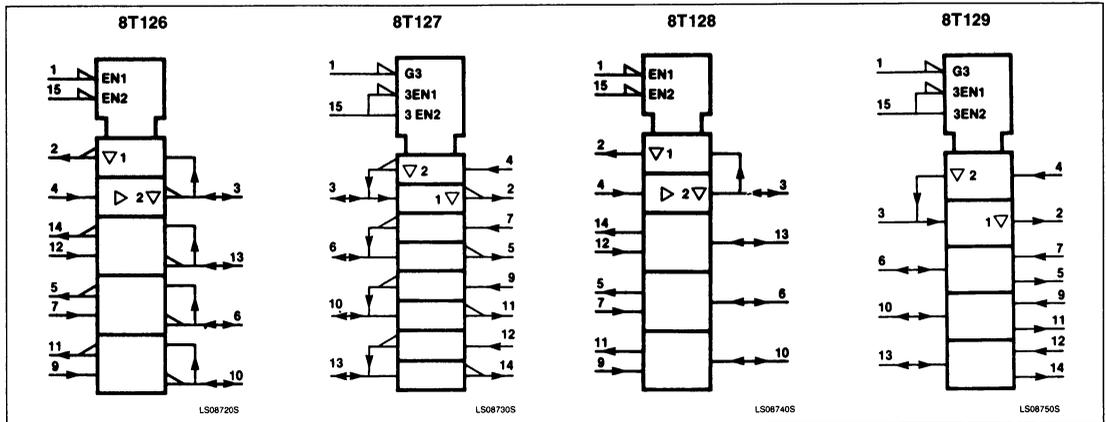
LOGIC SYMBOL



Transceivers

8T126, 127, 128, 129

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8T	N8T	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	Transceiver inputs	-0.5 to +5.5	V
		Non-transceiver inputs	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	-30 to +1	mA
I _{OL}	Continuous	50	50	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETERS		8T126/8T128			8T127/8T129			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			0.8			0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	HIGH-level output current	Bus		-5.2			-5.2	mA
		Receiver		-2.6			-5.2	mA
I _{OL}	LOW-level output current	Bus		24			24	mA
		Receiver		12			24	mA
T _A	Operating free-air temperature	0		70	0		70	°C

Transceivers

8T126, 127, 128, 129

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		8T126/8T128		8T127/8T129		UNIT
			Min	Max	Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0		V
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage			0.8		0.8	V
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -18mA			-1.5		-1.5	V
V _{OH} High-level output voltage, bus outputs	V _{CC} = MIN	I _{OH} = -5.2mA	2.4		2.4		V
V _{OH} HIGH-level output voltage, receiver outputs	V _{CC} = MIN, V _{IN} = V _{IL} , or V _{IH} per function table	I _{OH} = -100μA	3.4				V
		I _{OH} = -2.6mA	2.4				V
		I _{OH} = -5.2mA			2.4		V
V _{OL} LOW-level output voltage, bus outputs	V _{CC} = MIN	I _{OL} = 12mA		0.4		0.4	V
		I _{OL} = 24mA		0.5		0.5	V
V _{OL} LOW-level output voltage, receiver outputs	V _{CC} = MIN	I _{OL} = 6mA		0.4			V
		I _{OL} = 12mA				0.4	V
		I _{OL} = 12mA		0.5			V
		I _{OL} = 24mA				0.5	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V			20		20	μA
I _{OZL} Off-state output current, LOW-level voltage applied, receiver outputs	V _{CC} = MAX, V _O = 0.4V			-20		-20	μA
I _{OZL} Off-state output current, LOW-level voltage applied, bus outputs	V _{CC} = MAX, V _O = 0.4V			-100		-200	μA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20		20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	Bus inputs	V _I = 5.5V			100	μA
		Others	V _I = 7.0V			100	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-100		-200	μA
I _{OS} Short-circuit output current ²	V _{CC} = MAX		-40	-120	-40	-120	mA
I _{CCH} Supply current HIGH	V _{CC} = MAX, outputs HIGH			26		36	mA
I _{CCL} Supply current LOW	V _{CC} = MAX, outputs LOW			30		42	mA
I _{CCZ} Supply current "off"	V _{CC} = MAX, outputs "off"			36		44	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

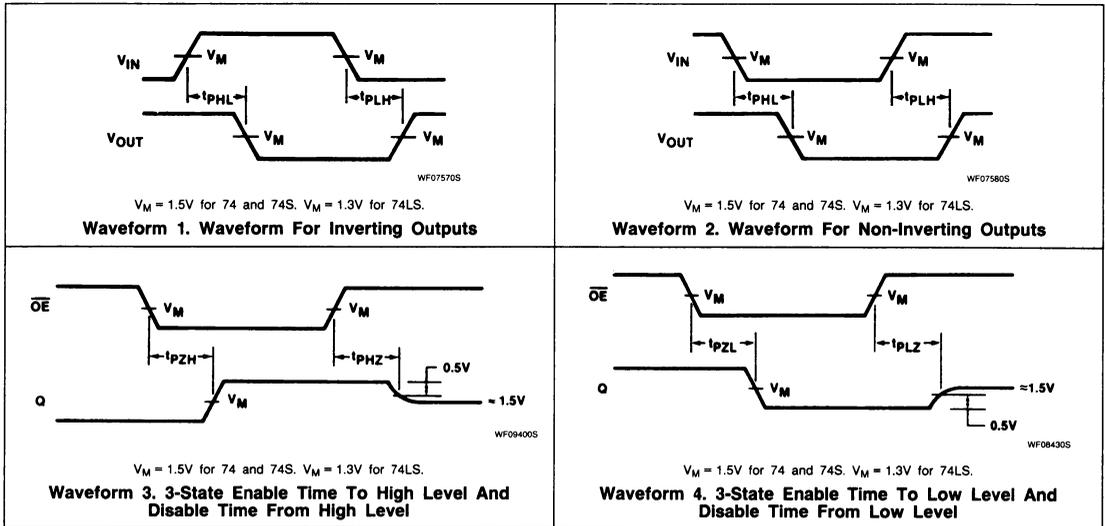
Transceivers

8T126, 127, 128, 129

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T126/8T128		8T127/8T129		UNIT
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to bus output Waveform 1 & 2, $C_L = 100\text{pF}$, $R_L = 667\Omega$		20 30		20 30	ns
t_{PLH} t_{PHL}	Propagation delay Bus to receiver output Waveform 1 & 2, $C_L = 50\text{pF}$, $R_L = 667\Omega$		20 30		20 25	ns
t_{PZH}	Enable to HIGH for bus output Waveform 3, $C_L = 100\text{pF}$, $R_L = 667\Omega$		30		35	ns
t_{PZH}	Enable to HIGH for receiver output Waveform 3, $C_L = 50\text{pF}$, $R_L = 667\Omega$		25		30	ns
t_{PZL}	Enable to LOW for bus output Waveform 4, $C_L = 100\text{pF}$, $R_L = 667\Omega$		35		35	ns
t_{PZL}	Enable to LOW for receiver output Waveform 4, $C_L = 50\text{pF}$, $R_L = 667\Omega$		30		30	ns
t_{PHZ}	Disable from HIGH Waveform 3, $C_L = 5\text{pF}$, $R_L = 667\Omega$ Waveform 3, $C_L = 50\text{pF}$, $R_L = 667\Omega$ Waveform 3, $C_L = 100\text{pF}$, $R_L = 667\Omega$		25		25	ns
			63		63	ns
			102		102	ns
t_{PLZ}	Disable from LOW Waveform 4, $C_L = 5\text{pF}$, $R_L = 667\Omega$ Waveform 4, $C_L = 50\text{pF}$, $R_L = 667\Omega$ Waveform 4, $C_L = 100\text{pF}$, $R_L = 667\Omega$		25		25	ns
			29		29	ns
			33		33	ns

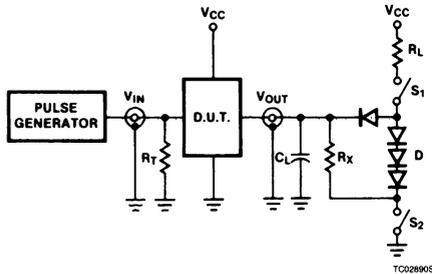
AC WAVEFORMS



Transceivers

8T126, 127, 128, 129

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t _{pZH}	Open	Closed
t _{pZL}	Closed	Open
t _{pHZ}	Closed	Closed
t _{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

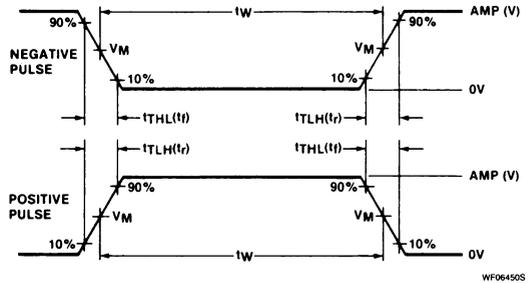
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_x = 1kΩ for 74, 74S, R_x = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

8T380 Bus Receiver

Quad Bus Receiver with Hysteresis-Schmitt Trigger
Product Specification

Logic Products

DESCRIPTION

The 8T380 is a quad 2-input bus receiver with hysteresis for use in I/O, data, and memory busses. Built-in hysteresis provides maximum noise immunity and a power-up or power-down sequence on the receiver will not affect the bus. LOW input current allows several drivers and receivers to communicate over a common bus in "Party line" fashion. The 8T380 is ideal as a Schmitt Trigger in analog interfaces that cannot tolerate the non-linear input impedance characteristics of standard TTL. Further, the LOW input requirements allow the 8T380 to be used as a CMOS to TTL interface. All inputs have clamping diodes to simplify systems design.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Out
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T380	20ns (t _{PLH}) 16ns (t _{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V ± 5%; T _A = 0°C to +70°C
Plastic DIP	N8T380N
Plastic SO	N8T380D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

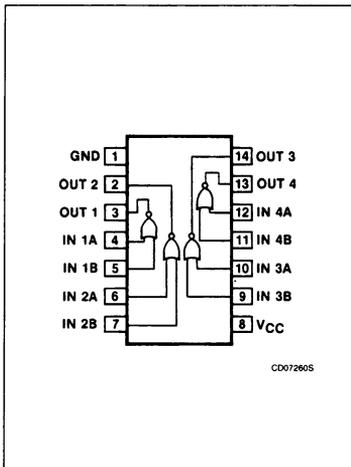
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
All	Input	1.2uI
All	Output	10uI

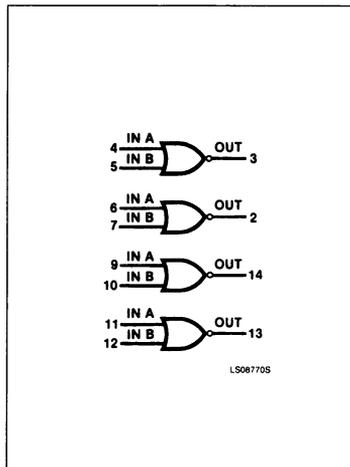
NOTE:

A unit load (uI) is 40μA I_{IH} and -1.6mA I_{IL}.

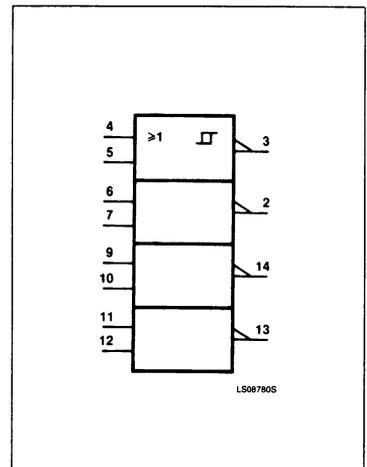
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Bus Receiver

8T380

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{OL}	Continuous	30	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0		2.5	V
V _{IL}	LOW-level input voltage	1.1		1.5	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-400	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T380		UNIT		
		Min	Max			
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0	2.5	V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		1.1	1.5	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA			-1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -400μA		2.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 16mA			0.4	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V			50	μA
		V _{CC} = 0V, V _I = 4.5V			50	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0V			-25	μA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		-18	-55	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V			40	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

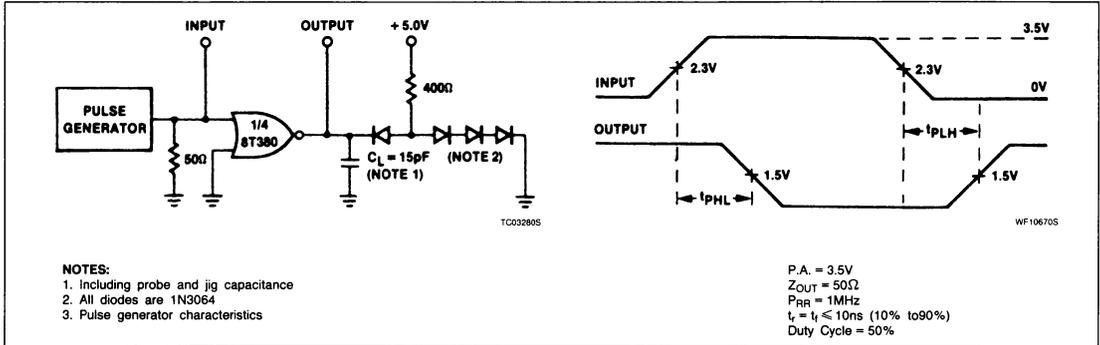
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH}	Propagation delay		35	ns
t _{PHL}	Input to output	See Test Circuits and Waveforms	35	

Bus Receiver

8T380

TEST CIRCUITS AND WAVEFORMS



Bus Receiver

8T380

TYPICAL APPLICATIONS

A generalized "Party Line" bus interface is shown in Figure 1. Each driver/receiver combination can communicate with any other pair of all. Open collector NAND Gates such as the Signetics 7439 have adequate driver capability for the bus terminations as well as 20 driver/receiver pairs. In addition the busing scheme is non-inverting as shown and bus drivers are activated by a logic "1" whereas bus receivers are activated by a Logic "0."

Each termination consisting of a 180Ω resistor to V_{CC} and 390Ω to ground is a 120Ω Thevenin's equivalent circuit. The maximum length of cable that can be driven is a complex relationship involving the type of cable used as well as the distribution of drivers and receivers on the bus. Using flat ribbon cable, a maximum reasonable length is 50 ft. minus the combined length of all taps or stubs.

SCHMITT TRIGGER

The receiver transfer curve shown in Figure 2a makes the 8T380 ideal in a variety of Schmitt Trigger and waveshaping applications such as Figure 2b.

MOS/CMOS INTERFACE

The input current which is only 50μA MAX in the logical "1" state and no current in the logical "0" state marks the 8T380 an ideal MOS/CMOS interface element.

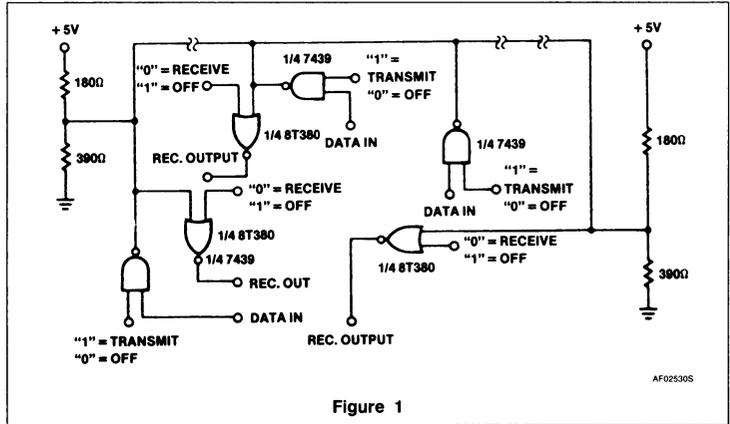


Figure 1

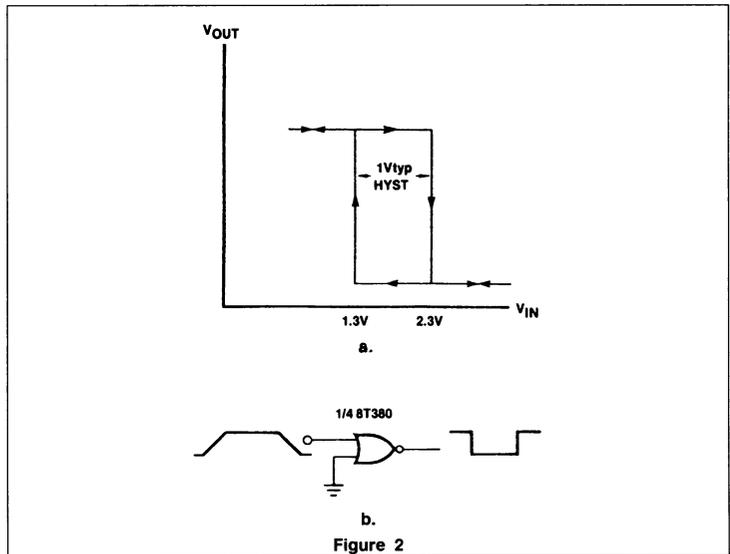


Figure 2

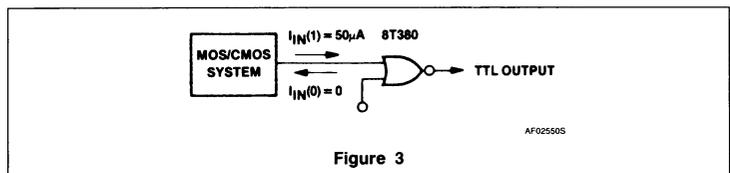


Figure 3

6

8T3404 Latch

High Speed 6-Bit Latch
Product Specification

Logic Products

FEATURES

- Low input load current: .25mA max., 1/6 standard TTL input load
- Minimum line reflection: low voltage diode input clamp
- Outputs sink 10mA min.
- 16-pin dual in-line package
- Simple expansion: enable inputs
- 12ns max. data to output delay over 0°C to 75°C temperature
- Directly compatible with DTL and TTL logic circuits

DESCRIPTION

The Signetics 8T3404 contains six high speed latches organized as independent 2-bit and 4-bit latches. They are designed for use as memory address registers, data registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low."

The 8T3404 is packaged in a standard 16-pin dual in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. To obtain fast switching speeds resulting in

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T3404	6ns (Data) 8ns (Write enable)	47mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T3404N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

MODE	INPUTS		OUTPUTS
	\bar{W}	D	\bar{Q}
Write latches	L	L	H
	L	H	L
Latch inputs	H	l	H
	H	h	L

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH \bar{W} transition.

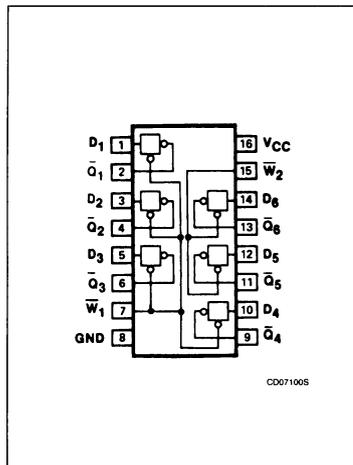
L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH \bar{W} transition.

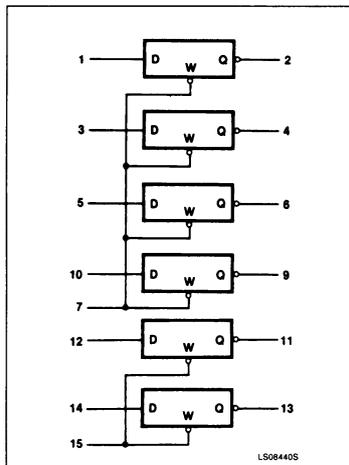
higher performance than equivalent devices made with a gold diffusion pro-

cess, Schottky barrier diode clamped transistors are used.

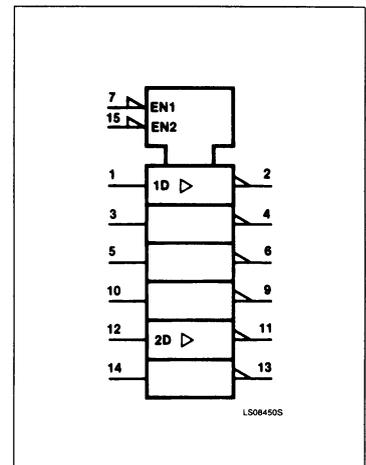
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Latch

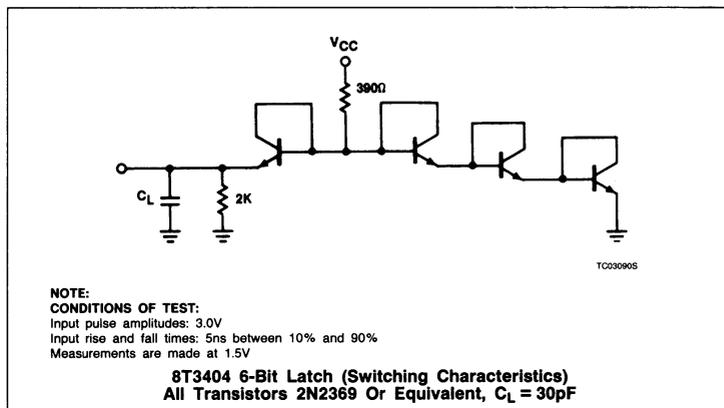
8T3404

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	N8T	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	V
I_{IN} Input current	-30mA to +100 μ A	
I_{OL} Continuous	100	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 5	$^{\circ}$ C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	V
V_{IH} High-level output voltage	2.0			V
V_{IL} LOW-level input voltage			+0.8	V
I_C Input clamp current			-5.0	mA
I_{OH} High-level output current			-1.5	mA
I_{OL} LOW-level output current			40	mA
T_A Operating free-air temperature	0		75	$^{\circ}$ C

TEST LOAD CIRCUIT

Latch

8T3404

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T3404			UNIT
		Min	Typ	Max	
V _{IL} Low level input current	V _{CC} = 5.25V, V _I = 0.45V			-0.25	mA
V _{IH} High level input current	V _{CC} = 5.25V, V _I = 5.25V			10	μA
V _{IK} Input clamp diode voltage	V _{CC} = 4.75V, I _C = -5.0mA			-1.0	V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 10.0mA			0.45	V
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -1.5mA	2.4			V
V _{IL} Input LOW voltage	V _{CC} = 5.0V			0.85	V
V _{IH} Input HIGH voltage	V _{CC} = 5.0V	2.0			V
I _{OS} Short-circuit output current ²	V _{CC} = 5.0V	-40		-120	mA
V _{OL} Output LOW voltage @ HIGH current	V _{CC} = 5.0V, I _{OL} = 40mA			0.8	V
I _{CC} Supply current (total)	V _{CC} = 5.25V			75	mA
I _{IL} Low level input current at pin 7	V _{CC} = 5.25V, V _I = 0.45V			-1.00	mA
I _{IL} Low level input current at pin 15	V _{CC} = 5.25V, V _I = 0.45V			-0.50	mA
I _{IH} High level input current at pin 7 and pin 15	V _I = 5.25V			10	μA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

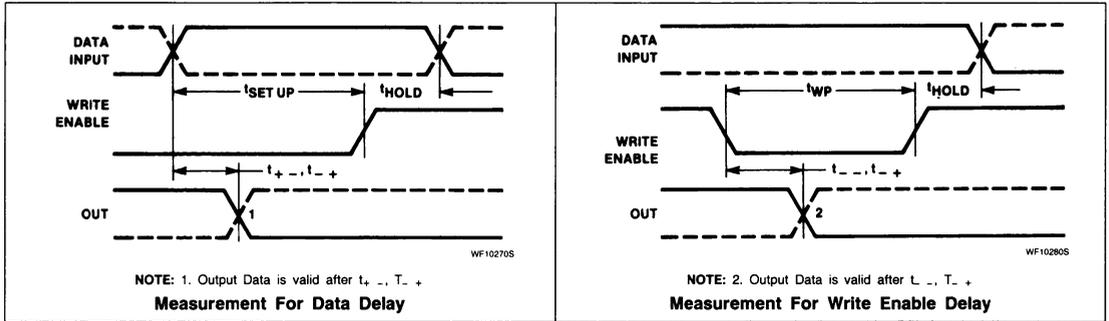
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T			UNIT
		Min	Typ	Max	
t _{+→} , t _{-→} Data to output delay				12	ns
t _{-→} , t ₋₊ Write enable to output delay				17	ns
t _{set-up} Time data must be present before rising edge of write enable		12			ns
t _{hold} Time data must remain after rising edge of write enable		8			ns
t _{WP} Write enable pulse width		15			ns
C _{IND} Data input capacitance	3404N f = 1MHz, V _{CC} = 0V 3404F V _{BIAS} = 2.0V, T _A = 25°C		4		pF
C _{INW} Write enable capacitance	3404N f = 1MHz, V _{CC} = 0V 3404F V _{BIAS} = 2.0V, T _A = 25°C		7		pF
			8		pF

Latch

8T3404

AC WAVEFORMS



8TS805, 806 Latches/Flip-Flops

8TS805 Octal Transparent Latch With 3-State Outputs
8TS806 Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 8-bit transparent latch – 8TS805
- 8-bit positive, edge-triggered register – 8TS806
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION

The 8TS805 is an octal, transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the High-to-Low enable transition. The enable gate has about 400mV of hysteresis built

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
8TS805	10ns	105mA
8TS806	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8TS805N, N8TS806N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

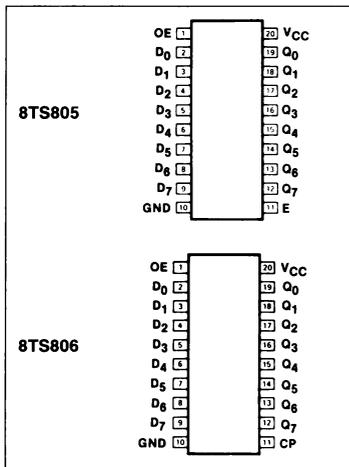
PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE:

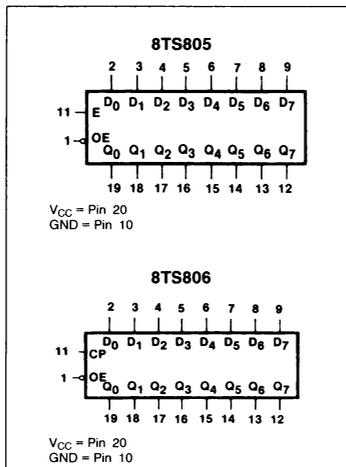
An 8TS unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

in to help minimize problems that signal and ground noise can cause on the latching operation.

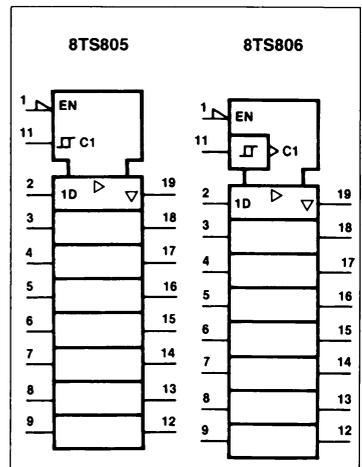
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Latches/Flip-Flops

8TS805, 806

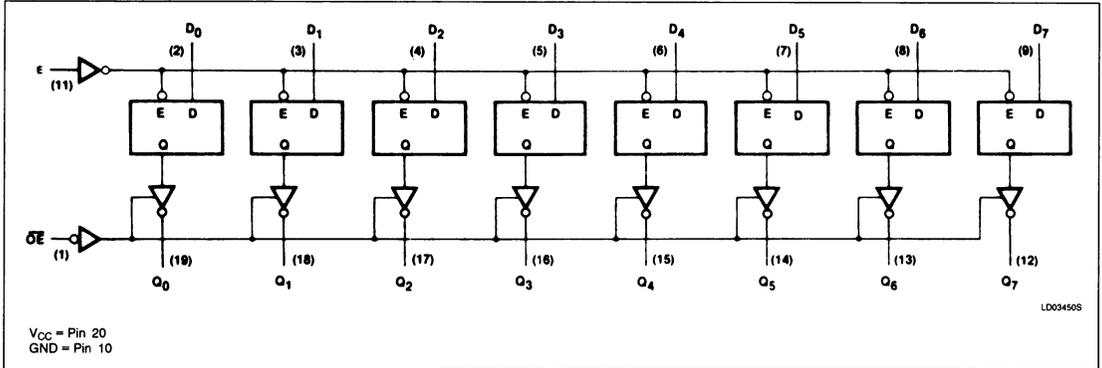
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the

HIGH impedance "off" state, which means they will neither drive nor load the bus.

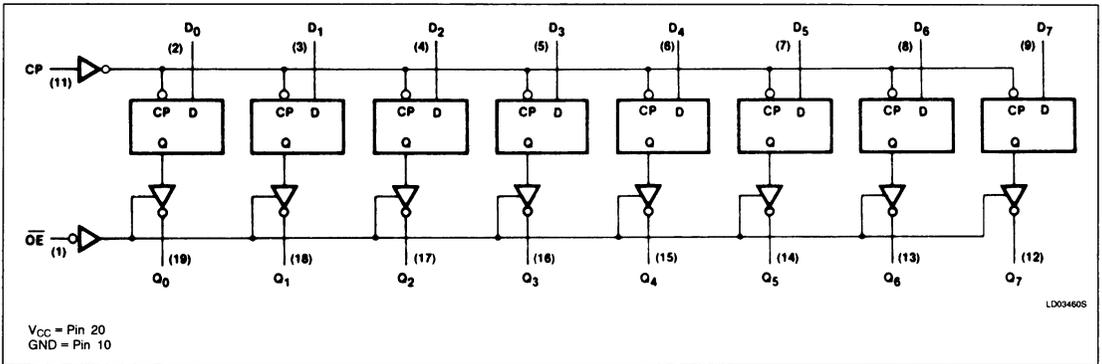
The 8TS806 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

LOGIC DIAGRAM, 8TS805



LOGIC DIAGRAM, 8TS806



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MODE SELECT — FUNCTION TABLE, 8TS805

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	E	D_n		$Q_0 - Q_7$
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Disable outputs	H	X	X	X	(Z)

Latches/Flip-Flops

8TS805, 806

MODE SELECT — FUNCTION TABLE, 8TS806

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	OE	CP	D _n		Q ₀ - Q ₇
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	X	X	X	(Z)

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition.

(Z) = HIGH impedance "off" state

↑ = LOW-to-HIGH clock transition

X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8TS			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	HIGH-level output current			-6.5	mA
I _{OL}	LOW-level output current			20	mA
T _A	Operating free-air temperature	0		70	°C

NOTE:

V_{IL} = +0.7V MAX for S8TS at T_A = +125°C only.

Latches/Flip-Flops

8TS805, 806

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		8TS805, 806			UNIT
			Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.1		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX			0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.2	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.4V				50	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.5V				-50	μA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V				1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				50	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V				-0.25	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-40		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCL} 8TS805		105	160	mA
		I _{CCL} All inputs grounded, 8TS806		102	140	mA
		I _{CCZ} CP, \overline{OE} = 4.5V D inputs = GND		131	180	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
- V_{OL} = +0.45V MAX for S8TS at T_A = +125°C only.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8TS		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 6, 8TS806	75		MHz
t _{PLH} Propagation delay t _{PHL} Latch enable to output	Waveform 1, 8TS805		14 18	ns
t _{PLH} Propagation delay t _{PHL} Data to output	Waveform 4, 8TS805		9 13	ns
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 6, 8TS806		15 17	ns
t _{PZH} Enable time to HIGH level	Waveform 2		15	ns
t _{PZL} Enable time to LOW level	Waveform 3 8TS805 8TS806		18 18	ns
t _{PHZ} Disable time from HIGH level	Waveform 2, C _L = 5pF		9	ns
t _{PLZ} Disable time from LOW level	Waveform 3, C _L = 5pF		12	ns

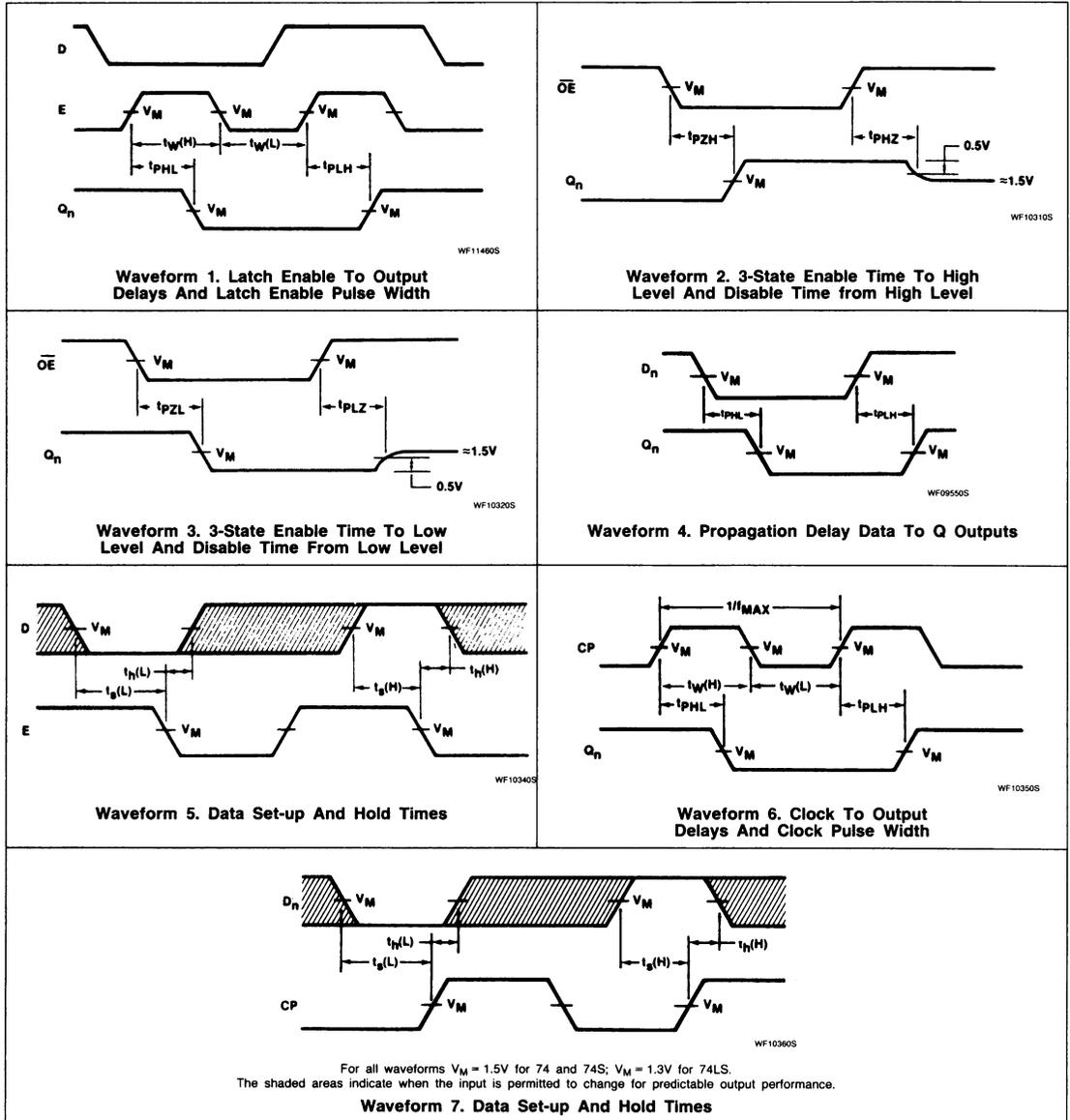
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Latches/Flip-Flops

8TS805, 806

AC WAVEFORMS



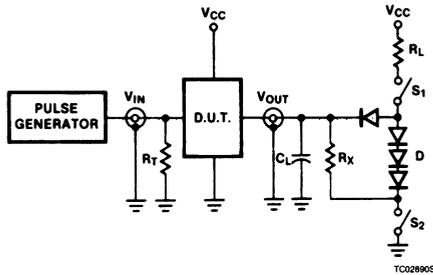
Latches/Flip-Flops

8TS805, 806

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8TS		UNIT
		Min	Max	
$t_{W(H)}$ $t_{W(L)}$ Latch enable pulse width	Waveform 1, 8TS805	6 7.3		ns
t_s Set-up time, data to latch enable	Waveform 5, 8TS805	5		ns
t_h Hold time, data to latch enable	Waveform 5, 8TS805	10		ns
$t_{W(H)}$ $t_{W(L)}$ Clock pulse width	Waveform 6, 8TS806	6 7.3		ns
t_s Set-up time, data to clock	Waveform 7, 8TS806	5		ns
t_h Hold time, data to clock	Waveform 7, 8TS806	4		ns

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

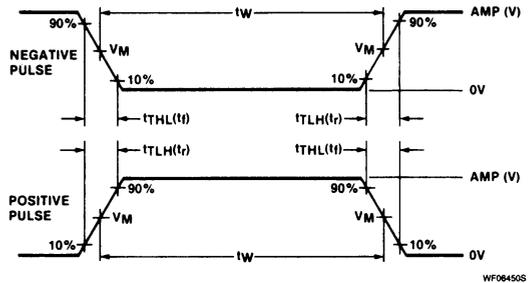
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = $1\text{k}\Omega$ for 74, 74S, R_X = $5\text{k}\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	2.5ns	2.5ns

8TS807, 808 Latches/Flip-Flops

8TS807 Octal Transparent Latch With 3-State Outputs
'808 Octal D Flip-Flop With 3-State Outputs
Product Specification

Logic Products

FEATURES

- 8-bit transparent latch – 8TS807
- 8-bit positive, edge-triggered register – 8TS808
- 3-State inverting output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION

The 8TS807 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
8TS807	10ns	105mA
8TS808	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8TS807N, N8TS808N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

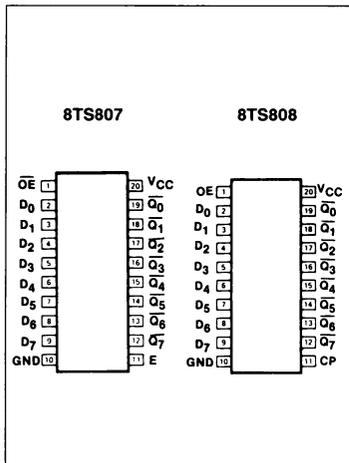
NOTE:

An 8TS unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

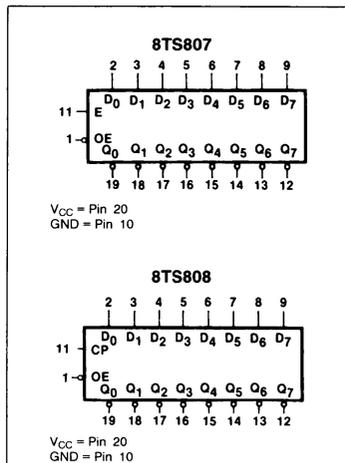
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation.

When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

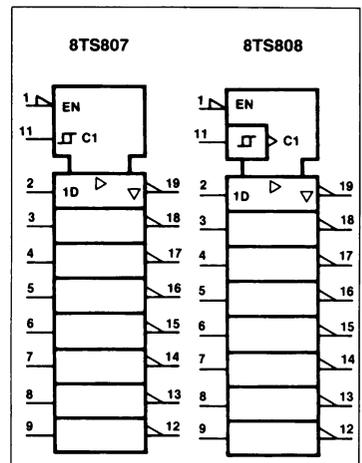
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Latches/Flip-Flops

8TS807, 808

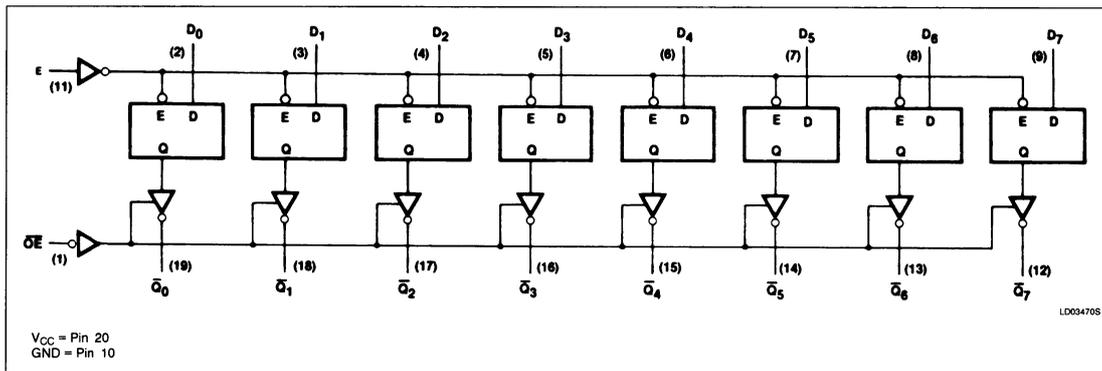
The 8TS808 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the

corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

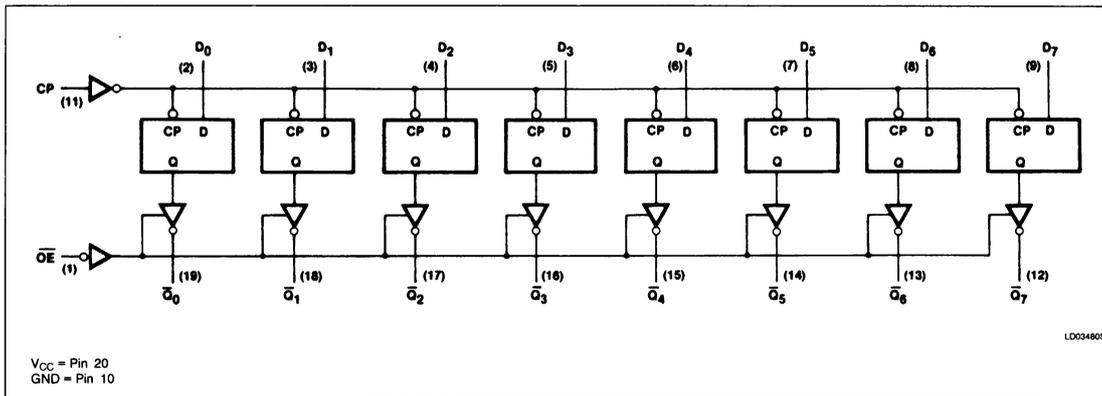
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS

memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 8TS807



LOGIC DIAGRAM, 8TS808



6

MODE SELECT — FUNCTION TABLE, 8TS807

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	E	D _n		Q ₀ - Q ₇
Enable and read register	L	H	L	H	H
	L	H	H	L	L
Latch and read register	L	L	l	L	H
	L	L	h	H	L
Disable outputs	H	X	X	X	(Z)

Latches/Flip-Flops

8TS807, 808

MODE SELECT — FUNCTION TABLE, 8TS808

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		$Q_0 - Q_7$
Load and read register	L	↑	l	H	L
	L	↑	h	L	H
Load register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

(Z) = HIGH impedance "off" state

↑ = LOW-to-HIGH clock transition

X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8TS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			6.5	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Latches/Flip-Flops

8TS807, 808

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8TS807, 808			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.1		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.4V			50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.5V			-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			-0.25	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCL} 8TS807		105	160	mA
		I _{CCL} All inputs grounded, 8TS808		102	140	mA
		I _{CCZ} CP, \overline{OE} = 4.5V D inputs = GND		131	180	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8TS		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 6, 8TS808	75		MHz
t _{PLH} Propagation delay	Waveform 1, 8TS807		14	ns
t _{PHL} Latch enable to output			18	
t _{PLH} Propagation delay	Waveform 4, 8TS807		9	ns
t _{PHL} Data to output			13	
t _{PLH} Propagation delay	Waveform 6, 8TS808		15	ns
t _{PHL} Clock to output			17	
t _{PZH} Enable time to HIGH level	Waveform 2		15	ns
t _{PZL} Enable time to LOW level	Waveform 3	8TS807 8TS808	18 18	ns
t _{PHZ} Disable time from HIGH level	Waveform 2, C _L = 5pF		9	ns
t _{PLZ} Disable time from LOW level	Waveform 3, C _L = 5pF		12	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

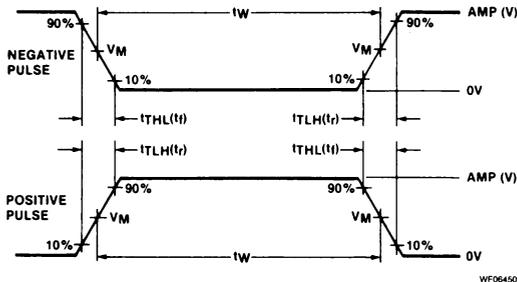
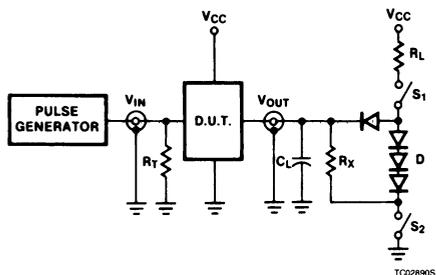
Latches/Flip-Flops

8TS807, 808

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8TS		UNIT
		Min	Max	
$t_{W(H)}$ $t_{W(L)}$ Latch enable pulse width	Waveform 1, 8TS807	6 7.3		ns
t_s Set-up time, data to latch enable	Waveform 5, 8TS807	5		ns
t_h Hold time, data to latch enable	Waveform 5, 8TS807	10		ns
$t_{W(H)}$ $t_{W(L)}$ Clock pulse width	Waveform 6, 8TS808	6 7.3		ns
t_s Set-up time, data to clock	Waveform 7, 8TS808	5		ns
t_h Hold time, data to clock	Waveform 7, 8TS808	4		ns

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

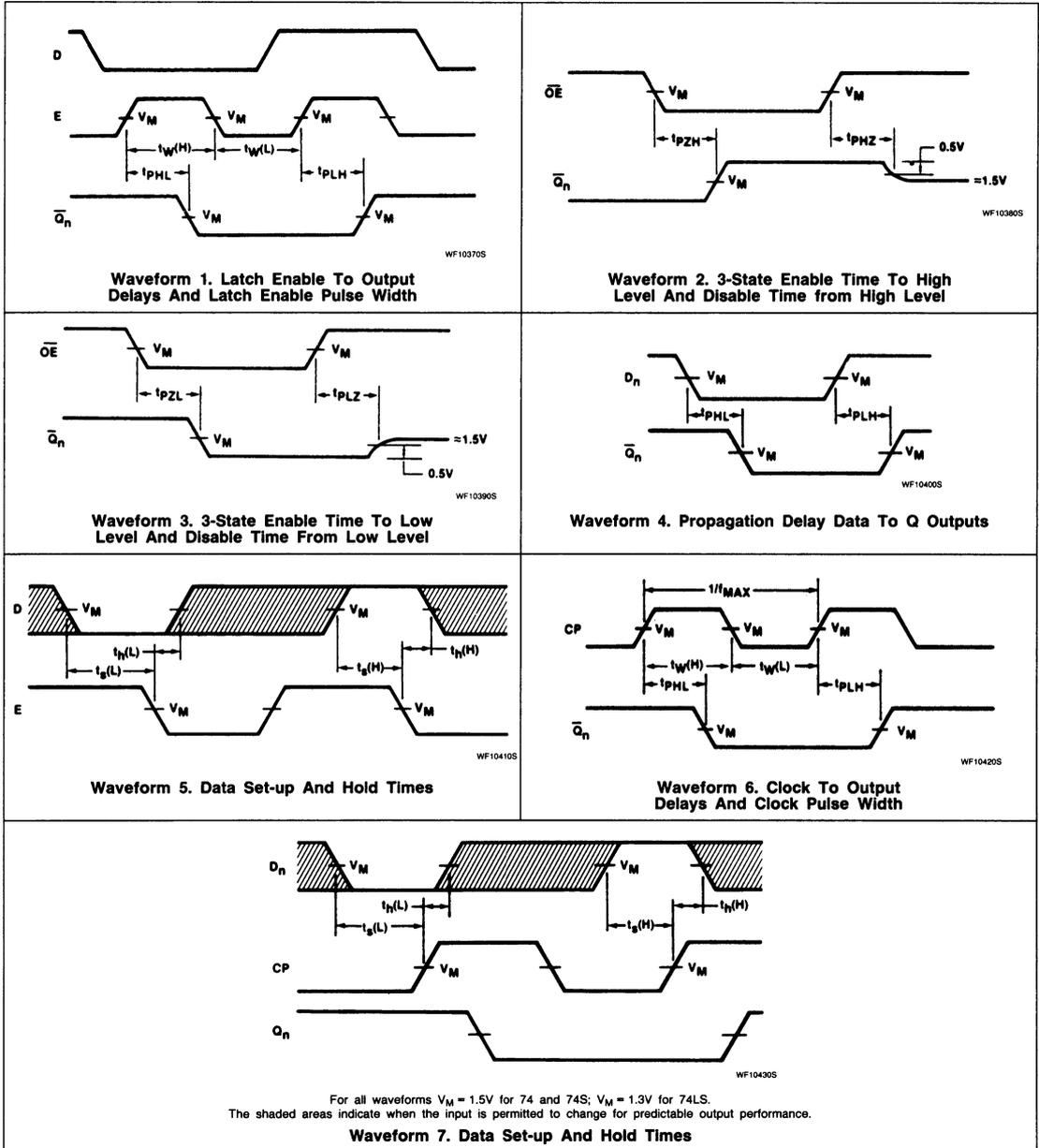
D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Latches/Flip-Flops

8TS807, 808

AC WAVEFORMS



74LS764 DRAM Controller

DRAM Dual-Ported Controller
Product Specification

Logic Products

FEATURES

- Allows two microprocessors to access the same bank of DRAM
- Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation
- 9 address output pins allow control of up to 256K DRAMS
- Separate refresh clock allows adjustable refresh timing
- On-board 18-bit address input latch
- 30MHz Maximum Clock rate

DESCRIPTION

The 74LS764 DRAM Dual-Ported Controller is a high-speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'LS764 contains an on-board 18-bit address input latch which latches the address inputs at the start of an access cycle.

The device is available in a 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS764	45ns	215mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS764N
PLCC-44	N74LS764A

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$\overline{REQ}_1, \overline{REQ}_2$	Request inputs (active LOW)	1LSUL
CP	Clock input	1LSUL
RCP	Refresh clock input	1LSUL
A1 - A18	Address inputs	1LSUL
GNT	Grant output	60LSUL
$\overline{SEL}_1, \overline{SEL}_2$	Select outputs (active LOW)	60LSUL
DTACK	Data transfer acknowledge output	60LSUL
\overline{RAS}	Row address strobe (output active LOW)	60LSUL
WG	Write gate output	60LSUL
\overline{CASEN}	Column address strobe enable output (active LOW)	60LSUL
MA0 - MA8	Address outputs	60LSUL

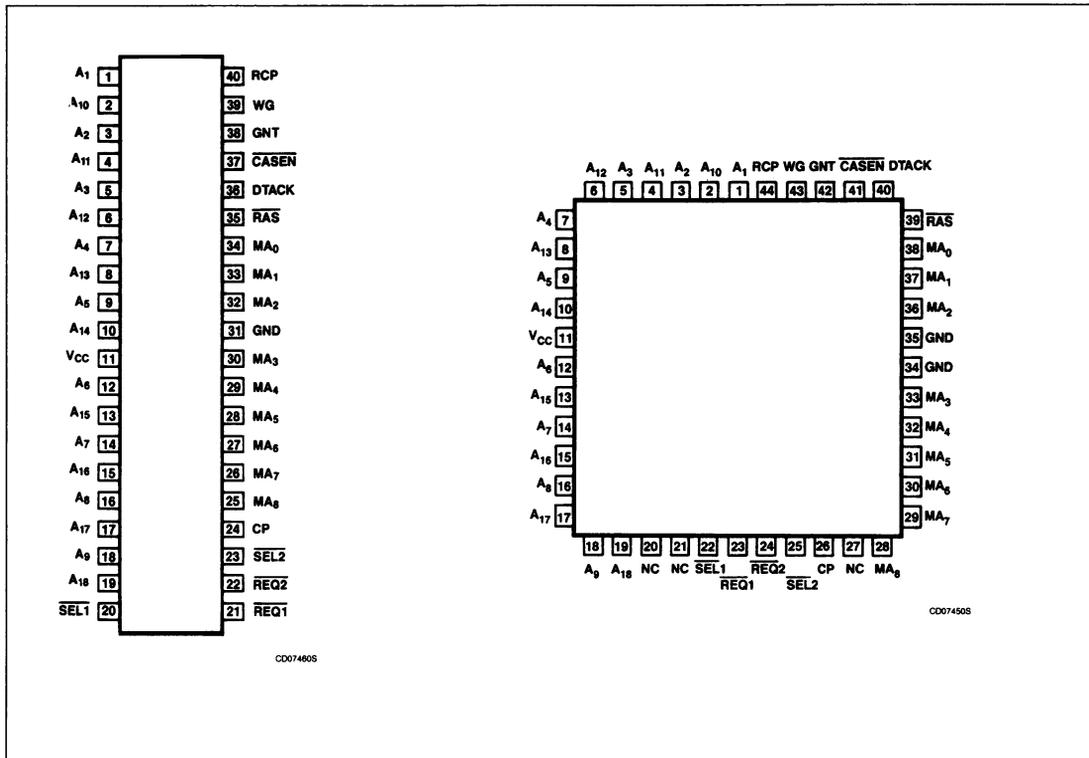
NOTE:

One 74LS Unit Load (LSUL) is defined as: 20 μ A in the HIGH state and 0.4mA in the LOW state.

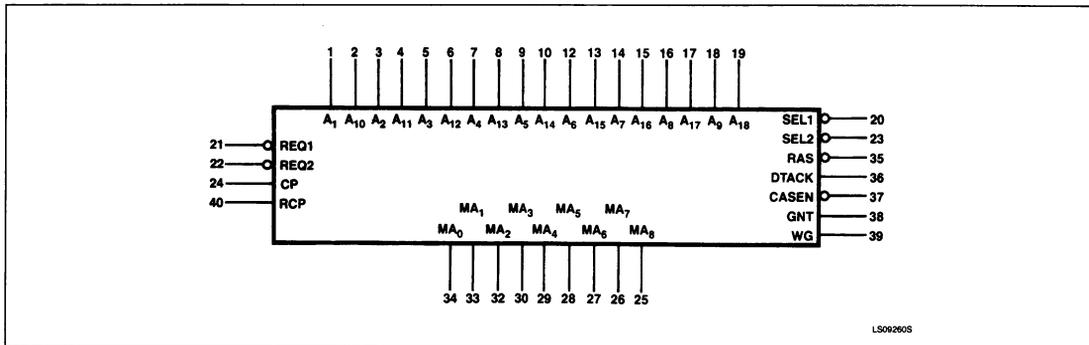
DRAM Controller

74LS764

PIN CONFIGURATION



LOGIC SYMBOL



DRAM Controller

74LS764

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1	1	1	I	Address inputs used to generate memory row address.
A2	3	3	I	
A3	5	5	I	
A4	7	7	I	
A5	9	9	I	
A6	11	12	I	
A7	13	14	I	
A8	15	16	I	
A9	17	18	I	
A10	2	2	I	Address inputs used to generate memory column address.
A11	4	4	I	
A12	6	6	I	
A13	8	8	I	
A14	10	10	I	
A15	12	13	I	
A16	14	15	I	
A17	16	17	I	
A18	18	19	I	
\overline{REQ}_1	21	23	I	Memory access request from microprocessor one.
\overline{REQ}_2	22	24	I	Memory access request from microprocessor two.
CP	24	26	I	Clock input which determines the master timing and arbitration rates.
RCP	40	44	I	Refresh Clock determines the period of refresh for each row after it is internally divided by 64.
\overline{SEL}_1	20	22	O	Select signal is activated in response to the active \overline{REQ}_1 input, indicating that access will be granted to microprocessor one.
V _{CC}	11	11		Power supply +5V ±5%
GND	31	34 35		Ground
\overline{SEL}_2	20	25	O	Select signal is activated in response to the active \overline{REQ}_2 input, indicating that access will be granted to microprocessor two.
MA0	34	38	O	Memory address output pins, designed to drive the address lines of a DRAM.
MA1	33	37	O	
MA2	32	36	O	
MA3	30	33	O	
MA4	29	32	O	
MA5	28	31	O	
MA6	27	30	O	
MA7	26	29	O	
MA8	25	28	O	
GNT	38	42	O	Grant output internally activated upon start of memory access cycle.
\overline{RAS}	35	39	O	Row address strobe is used to latch the row address into the bank of DRAM(to be connected directly to the \overline{RAS} inputs of the DRAMs).
WG	39	43	O	When activated, the "Write Gate" signal from the device could be gated with the microprocessor's write strobe to perform an "Early Write".
\overline{CASEN}	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs.
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has occurred.

DRAM Controller

74LS764

ARCHITECTURE

The 'LS764 arbitration logic is divided into two stages. The first stage controls which one of the two REQ inputs will be serviced by activating the corresponding SEL output. The SEL output signals have been provided for use as look-ahead enables for 3-state address lines from each of the microprocessors connected to the address inputs of the 'LS764.

The second arbitration stage controls arbitration between the SEL signals and refresh requests. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle via the GNT output signal. GNT is provided to indicate to the requesting microprocessor that its access cycle has begun. The GNT and SEL outputs can be used to generate wait states.

The 'LS764 has an 18-bit internal latch which latches the address inputs, A1 - A18, at the start of the access cycle. The latched address inputs are propagated to the MA0 - MA8 address outputs via an internal 18-bit MUX, which multiplexes the 18 address inputs to 9 row address and 9 column address signals, giving the 'LS764 the capability to interface 256K DRAMs to the masters.

The internal refresh row counter has 9 outputs, allowing the 'LS764 to refresh up to 512 row DRAMs.

The generation of RAS, CASEN, Write Gate (WG), and Data Transfer Acknowledge (DTACK) outputs are controlled by on chip timing logic.

FUNCTIONAL DESCRIPTION

The speed at which the 'LS764 operates is determined by the CP input, with a maximum limit of 30MHz. All internal signal timing and control is based on this input.

A microprocessor requests access to the DRAM by activating the appropriate REQ input. If a refresh cycle is not in process and the other request input is not active, the SEL output corresponding to the active REQ input will go LOW to indicate that access will be granted. The GNT output then goes HIGH (by the LOW-to-HIGH transition) indicating that a memory access cycle is now commencing. If an access or refresh cycle is in process, and the other microprocessor has not requested access, the SEL output corresponding to the active REQ input will go LOW to indicate that access will be granted, but GNT will not go HIGH until the current cycle is completed. After completion of current cycle, and followed by a synchronization period, GNT will automatically become active.

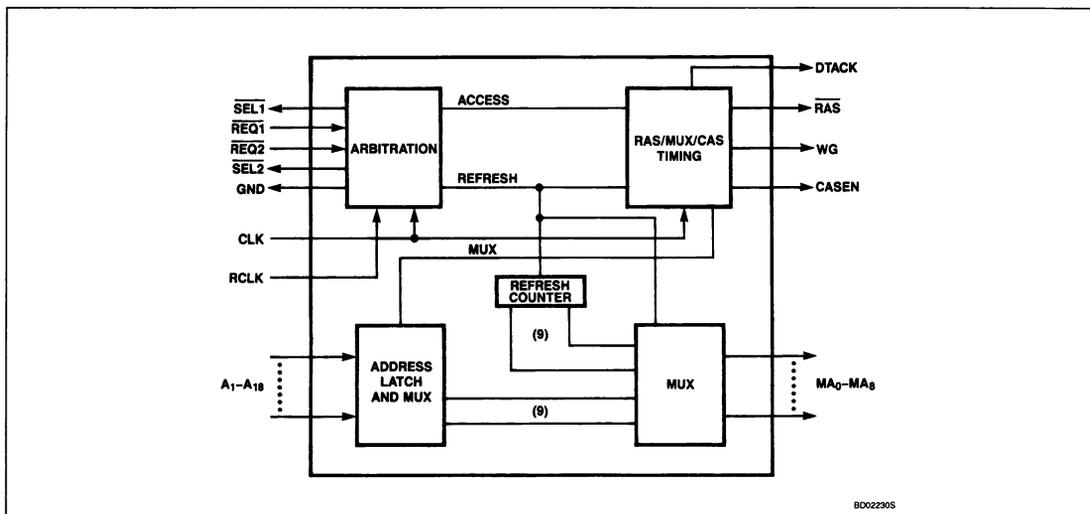
If access to the DRAM is requested by both microprocessors, the initial arbitration stage will determine which processor will be serviced by activating the corresponding SEL output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress at the time access is requested. REQ contention is arbitrated by internal circuitry sampling the REQ₁ and REQ₂ inputs on different edges of the CP input: REQ₁ is sampled on the rising edge of the clock and REQ₂ is sampled on the falling edge of the same clock. Specially designed CTL flip-flops have been used in this circuitry to eliminate meta-stable states. Again, if a refresh cycle is

in progress, the GNT output will not become active until the refresh cycle is completed.

When GNT becomes true on the 'LS764, the A1 - A18 address input signals are latched internally and the A1 - A9 signals are propagated to the MA0 - MA8 output pins. One-half clock cycle is allowed for the address signals to propagate through to the outputs, after which the RAS output is brought valid.

At the next half clock cycle, the A10 - A18 latch outputs on the 'LS764 are selected and propagated to the MA0 - MA9 outputs. The write gate (WG) output becomes valid at this time to indicate the proper time to gate the WRITE signal from the selected processor to the DRAM to perform an EARLY WRITE cycle. One-half clock cycle is again allowed for the A10 - A18 signals to propagate and stabilize. CASEN then becomes valid. CASEN can be used as a CAS output or decoded with higher-order address signals to produce multiple CAS signals. Once CASEN is valid, the controller will wait three clock cycles before negating RAS, making a total RAS pulse width of 4 clock cycles. At the time RAS becomes inactive, the DTACK output becomes true to indicate that data on the DRAM data lines is valid, or that the proper access time has been met. DTACK can be used to indicate a valid data transfer acknowledge for processors requiring this signal. All controller output signals will be held in this final state until the selected processor withdraws its request by driving its REQ input HIGH. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any

BLOCK DIAGRAM



8D022305

DRAM Controller

74LS764

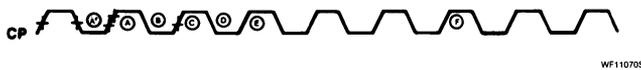
pending access or refresh cycles are serviced.

The refresh cycle commences from internally generated refresh requests. RCP is divided by 64 to produce a refresh request internally. Refresh requests are arbitrated with \overline{SEL} outputs in the second stage of arbitration. Refresh always has priority and will be serviced immediately or upon completion of the

current access cycle. At the start of a refresh grant, the 9 refresh counter address signals are allowed to propagate to the MA0 – MA8 outputs for one-half clock, at which time the \overline{RAS} signal becomes active for 4 clock cycles, then inactive for 3 clock cycles to meet the \overline{RAS} precharge requirement of the DRAMs, at which time the refresh cycle is terminated.

All signal outputs on the 'LS764 have 48mA drivers and proprietary positive edge rate controlling circuitry to reduce reflections when driving DRAMs on a PC board. The outputs are specified to handle up to 256pF without degradation of control and minimal degradation of access time, allowing any one pin to drive 32 devices (8pF load per input).

AC WAVEFORM FOR IMMEDIATE ACCESS (Sequence of events for \overline{REQ}_1 access when no refresh or \overline{REQ}_2 access)



WF11070S

- A' \overline{REQ}_2 sampled
- A \overline{REQ}_1 sampled
 \overline{SEL}_1 triggered (\overline{SEL}_1 triggered by \overline{REQ}_1 sample circuitry)
- B GNT triggered (\overline{SEL}_1 and GNT propagation paths are the same)
 A1 – A18 latched (Input address latch triggered by GNT circuitry)
 A1 – A9 propagate to MA outputs
- C \overline{RAS} triggered
- D WG triggered
 A10 – A18 selected and propagated to MA outputs
- E $\overline{C ASEN}$ triggered
- F \overline{RAS} negated
 DTACK triggered

DRAM Controller

74LS764

SYSTEM CYCLES

The 74LS764 is always in one of the following cycles.

A. IDLE There is no request pending and the refresh clock has not completed 64 clock cycles since the last refresh request.

B. REFRESH

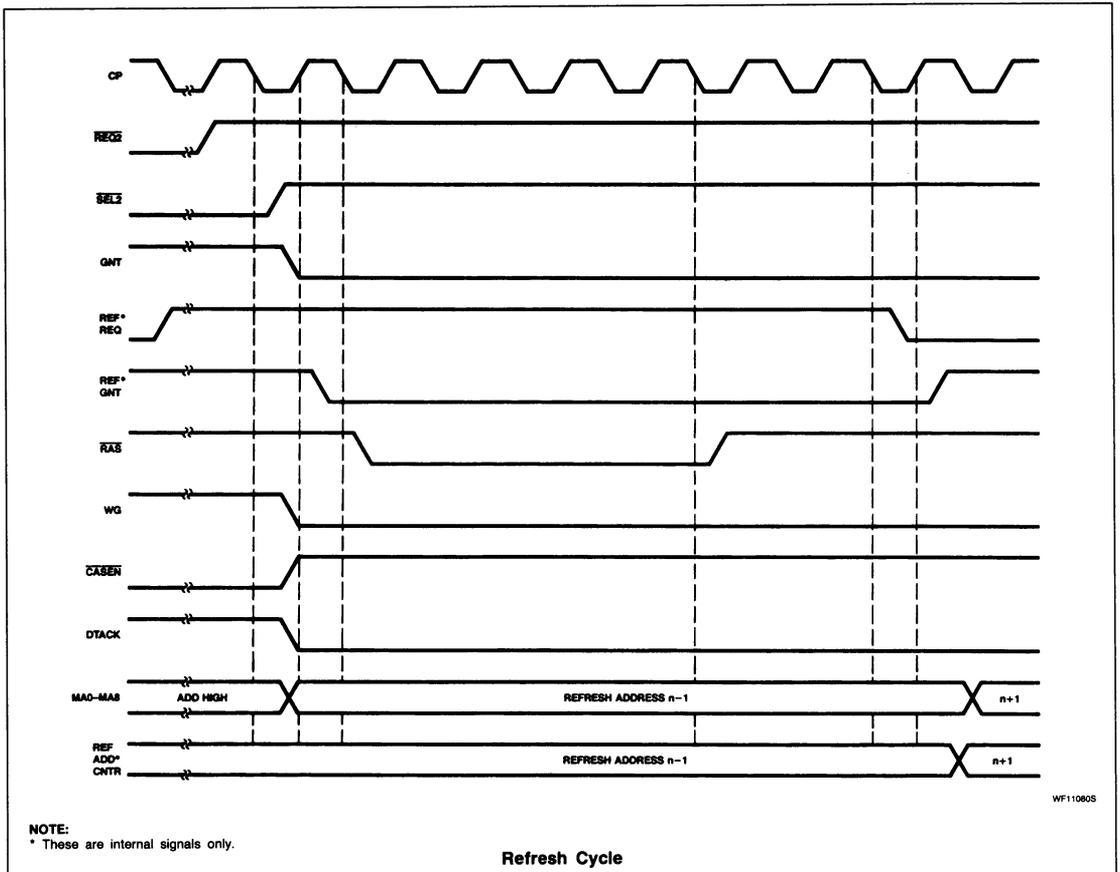
A refresh request is initiated every 64 refresh clock cycles, unless there is a refresh cycle already in progress. It is a \overline{RAS} only refresh cycle, derived from the clock (CP).

C. REQUEST₁

This is a memory access cycle for processor 1. It can only be initiated when there is no refresh or request 2 cycle in progress.

D. REQUEST₂

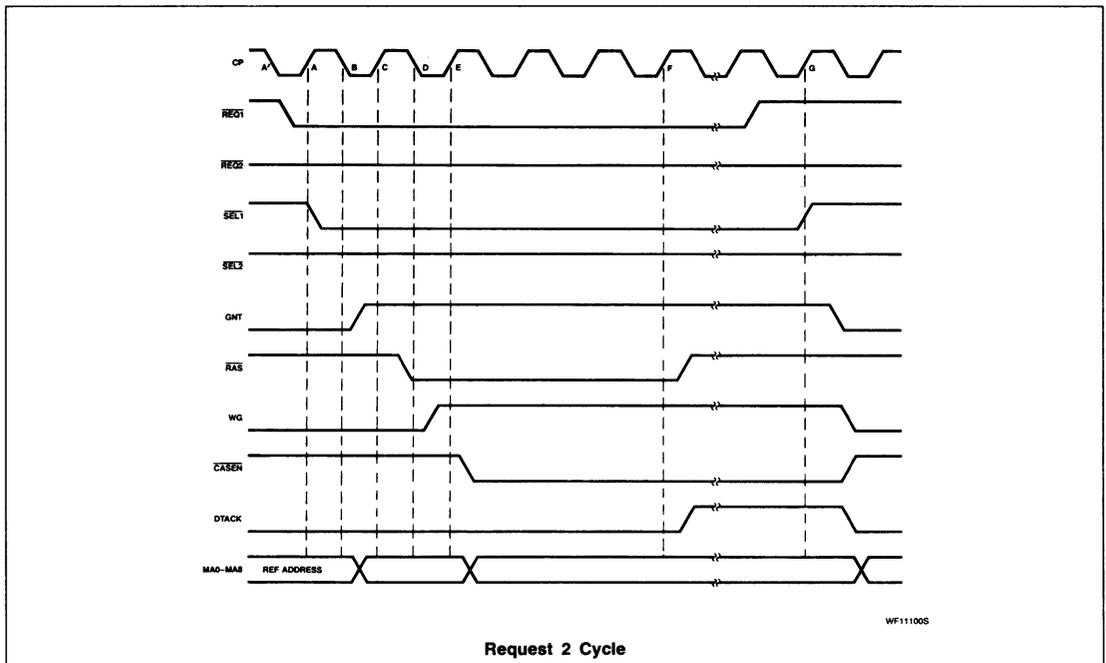
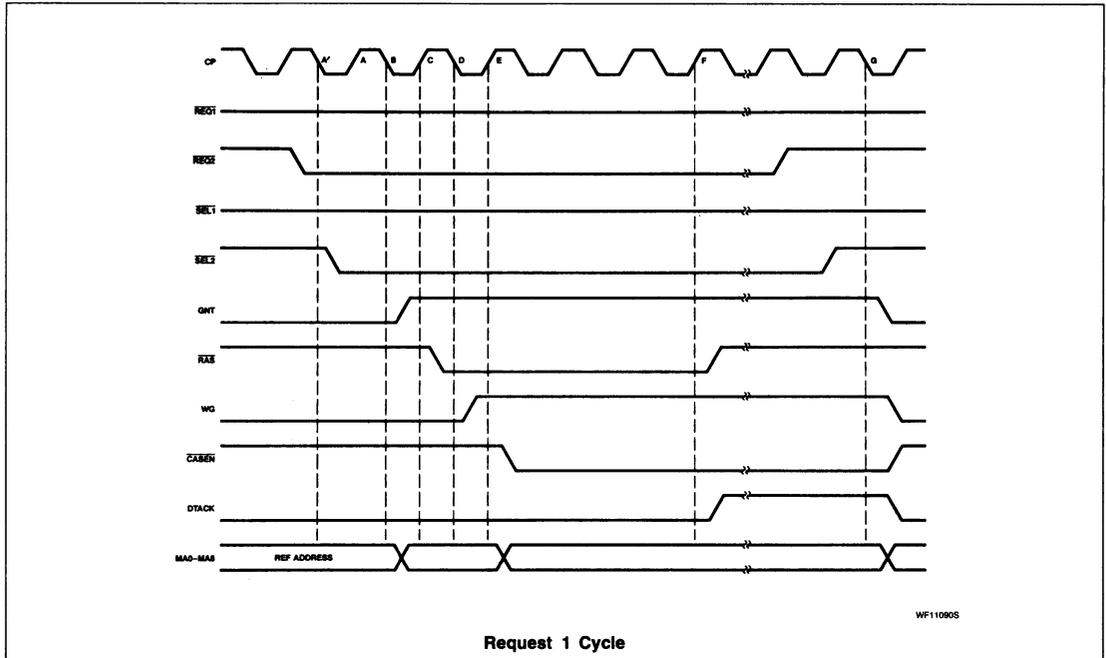
This is a memory access cycle for processor 2. It can only be initiated when there is no refresh or request 1 cycle in progress.



DRAM Controller

74LS764

SYSTEM CYCLES



7

DRAM Controller

74LS764

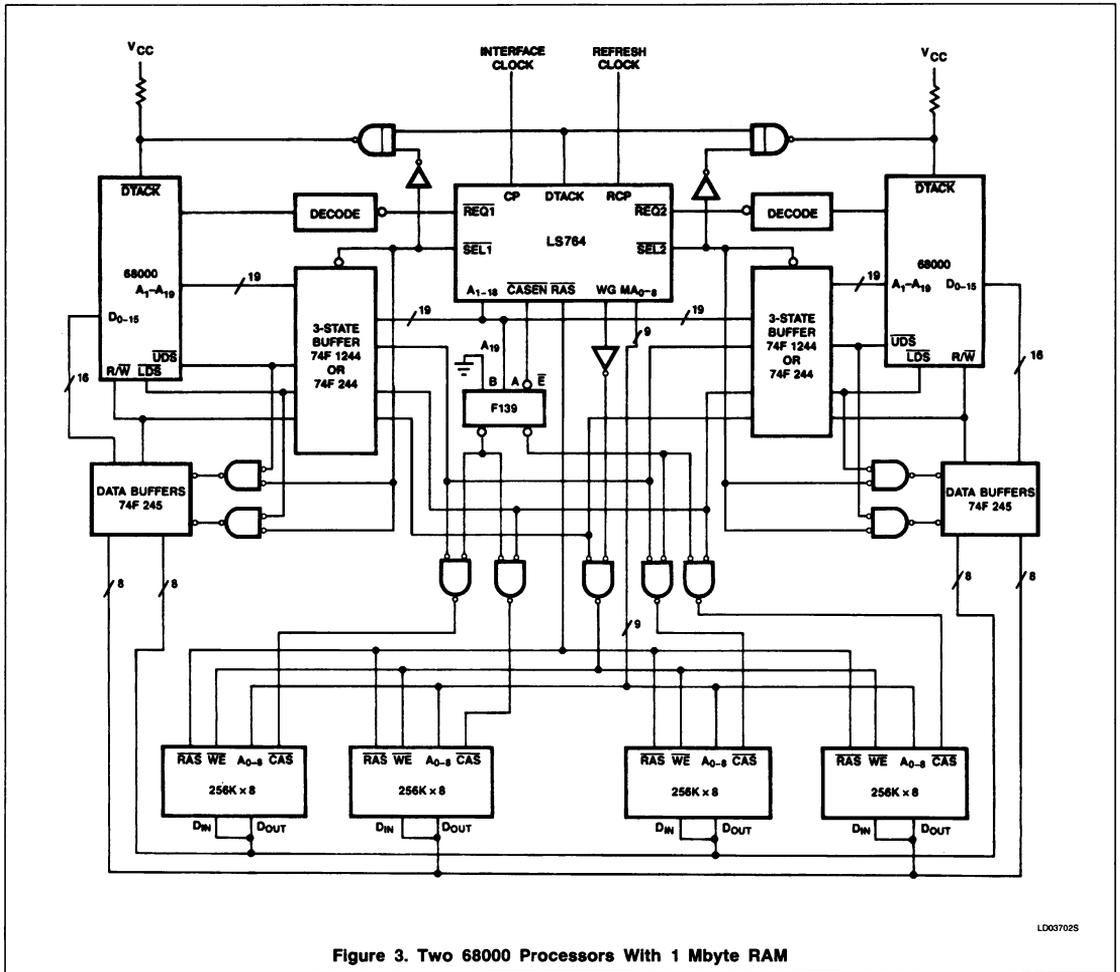


Figure 3. Two 68000 Processors With 1 Mbyte RAM

LD03702S

DRAM Controller

74LS764

ABSOLUTE MAXIMUM RATINGS (Over the operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS764	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	96	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS764			UNIT	
	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-400	μ A
I_{OL}	LOW-level output current	$V_{OL} = 450\text{mV}$		24	mA
		$V_{OL} = 650\text{mV}$		48	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS764			UNIT
		Min	Typ ²	Max	
V_{OH}	$V_{CC} = \text{Min}, V_{IL} = \text{Max}, V_{IH} = \text{Min}$ $I_{OH} = -35\text{mA}$	$\pm 10\%V_{CC}$	2.4	3.2	V
		$\pm 5\%V_{CC}$	2.7	3.4	V
V_{OL}	$V_{CC} = \text{Min}, V_{IL} = \text{Max}, V_{IH} = \text{Min}$ $I_{OL} = 60\text{mA}$	$\pm 10\%V_{CC}$.35	V
		$\pm 5\%V_{CC}$.35	V
V_{IK}	$V_{CC} = \text{Min}, I_I = I_{IK}$		-0.7	-1.5	V
I_I	$V_{CC} = 0.0\text{V}, V_I = 7.0\text{V}$			100	μ A
I_{IH}	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$			20	μ A
I_{IL}	$V_{CC} = \text{Max}, V_I = 0.5\text{V}$		-0.4	-0.6	mA
I_{RH} ³	$V_{CC} = \text{Min}, \text{force } 2.4\text{V}$			-35	mA
I_{RL} ⁴	$V_{CC} = \text{Min}, \text{force } 0.8\text{V}$	60			mA
I_{CC}	$V_{CC} = \text{Max}$		175	200	mA

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{RH} is the current necessary to guarantee the LOW to HIGH transition in a 70 Ω transmission line. This output condition results in a current that is approximately one half of the short circuit output current (I_{OS}).
- I_{RL} is the current necessary to guarantee the HIGH to LOW transition in a 70 Ω transmission line.

DRAM Controller

74LS764

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

PARAMETER	TEST CONDITIONS	74LS764			UNIT
		$C_L = 300\text{pF}$, $R_L = 70\Omega$			
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	32		MHz
t_{PLH} Propagation delay t_{PHL} CP(↑) to SEL_1		18	30	38	ns
t_{PLH} Propagation delay t_{PHL} CP(↓) to SEL_2		18	30	38	ns
t_{PLH} Propagation delay CP(B) to GNT		18	30	38	ns
t_{PHL} Propagation delay (Note 1)		18	35	45	ns
t_{PLH} Propagation delay t_{PHL} CP(B) to MA(Row Address)		15	32	40	ns
t_{PLH} Propagation delay CP(F) to $\overline{\text{RAS}}$	AC Waveforms	15	30	40	ns
t_{PHL} Propagation delay CP(C) to $\overline{\text{RAS}}$		15	32	42	ns
t_{PLH} Propagation delay CP(D) to WG		15	28	38	ns
t_{PHL} Propagation delay (Note 1)		32	52	62	ns
t_{PLH} Propagation delay t_{PHL} CP(D) to MA(Column Address)		15	30	42	ns
t_{PHL} Propagation delay (Note 1)		15	30	42	ns
t_{PLH} Propagation delay (Note 1)		30	48	60	ns
t_{PHL} Propagation delay CP(E) to $\overline{\text{CASEN}}$		15	32	42	ns
t_{PLH} Propagation delay CP(F) to DTACK		15	32	40	ns
t_{PHL} Propagation delay (Note 1)		34	50	62	ns
t_{PLH} Propagation delay t_{PHL} CP(transition) to MA(Refresh)		28	50	62	ns
		28	50	62	ns

NOTE:

These delays are with respect to clock edge "G" of the $\overline{\text{REQ}}_1$ or $\overline{\text{REQ}}_2$ access cycle shown on the AC Waveforms.

AC SET-UP REQUIREMENTS

PARAMETER	TEST CONDITIONS	74LS764		UNIT
		$C_L = 300\text{pF}$, $R_L = 70\Omega$		
		Min	Max	
$t_s(\text{H})$ Set-up time, HIGH or LOW $t_s(\text{L})$ $\overline{\text{REQ}}_1$, $\overline{\text{REQ}}_2$ to CP	AC Waveforms	3		ns
		3		
$t_h(\text{H})$ Hold time, HIGH or LOW $t_h(\text{L})$ CP to $\overline{\text{REQ}}_1$, $\overline{\text{REQ}}_2$		5		ns
		5		
$t_s(\text{H})$ Set-up time, HIGH or LOW $t_s(\text{L})$ $A_1 - A_{18}$ to CP(falling edge)		-8**		ns
		-8**		
$t_h(\text{H})$ Hold time, HIGH or LOW $t_h(\text{L})$ CP(falling edge) to $A_1 - A_{18}$		14		ns
		14		
$t_w(\text{H})$ CP pulse width, $t_w(\text{L})$ HIGH or LOW		19		ns
		18		
$t_w(\text{H})$ RCP pulse width, $t_w(\text{L})$ HIGH or LOW		10		ns
		12		

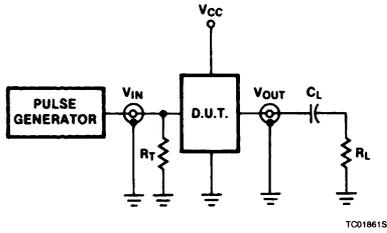
NOTES:

** These numbers indicate that the address inputs have a negative set-up time and could be valid 8ns after the falling edge of the CP clock. It is suggested that SEL_2 be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of SEL_1 to enable Address Bus 1. This will insure that set-up time for Address Bus 1 is not violated.

DRAM Controller

74LS764

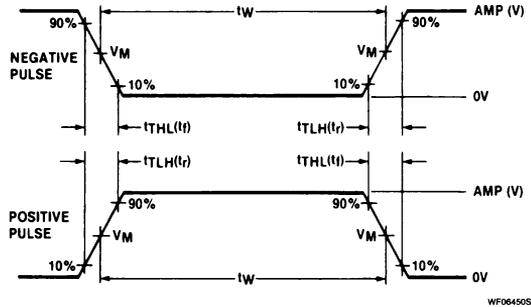
TEST CIRCUITS AND WAVEFORMS



Test Circuit Simulating RAM Boards

DEFINITIONS

- R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- D = DIODES are IN916, IN3064, or equivalent.
- t_{TLH} , t_{THL} values should be less than or equal to the table entries.



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74LS	3.0V	1MHz	500ns	15ns	6ns

74LS765 DRAM Controller

DRAM Dual-Ported Controller
Preliminary Specification

Logic Products

FEATURES

- Allows two microprocessors to access the same bank of DRAM
- Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation
- 9 address output pins allow control of up to 256K DRAMS
- Separate refresh clock allows adjustable refresh timing
- Same as LS764 but without input latch
- 30MHz Maximum Clock rate

DESCRIPTION

The 74LS765 DRAM Dual-Ported Controller is a high speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'LS765 unlatched option eliminates the address input latch to facilitate use with latched address outputs.

The device is available in a 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS765	45ns	215mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS765N*
PLCC-44	N74LS765A**

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
REQ_1, REQ_2	Request inputs (active LOW)	1LSUL
CP	Clock input	1LSUL
RCP	Refresh clock input	1LSUL
A1 - A18	Address inputs	1LSUL
GNT	Grant output	60LSUL
SEL_1, SEL_2	Select outputs (active LOW)	60LSUL
DTACK	Data transfer acknowledge output	60LSUL
\overline{RAS}	Row address strobe (output active LOW)	60LSUL
WG	Write gate output	60LSUL
\overline{CASEN}	Column address strobe enable output (active LOW)	
MA0 - MA8	Address outputs	60LSUL

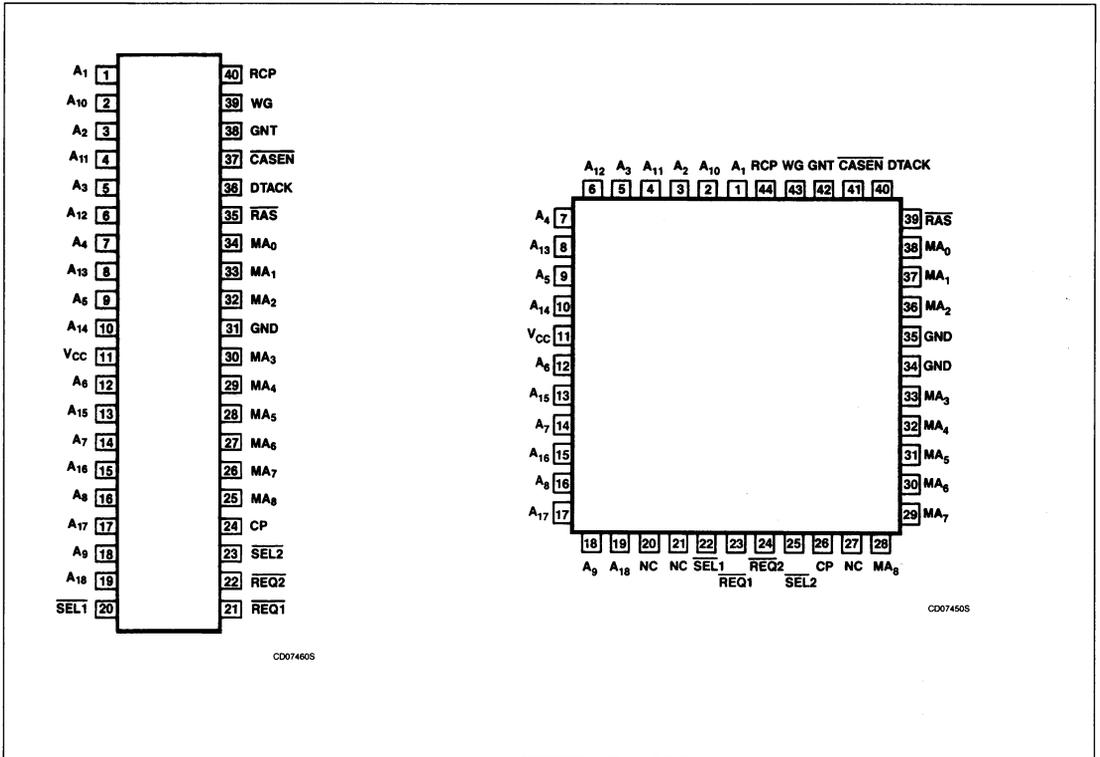
NOTE:

One 74LS Unit Load (LSUL) is defined as: 20 μ A in the HIGH state and 0.4mA in the LOW state.

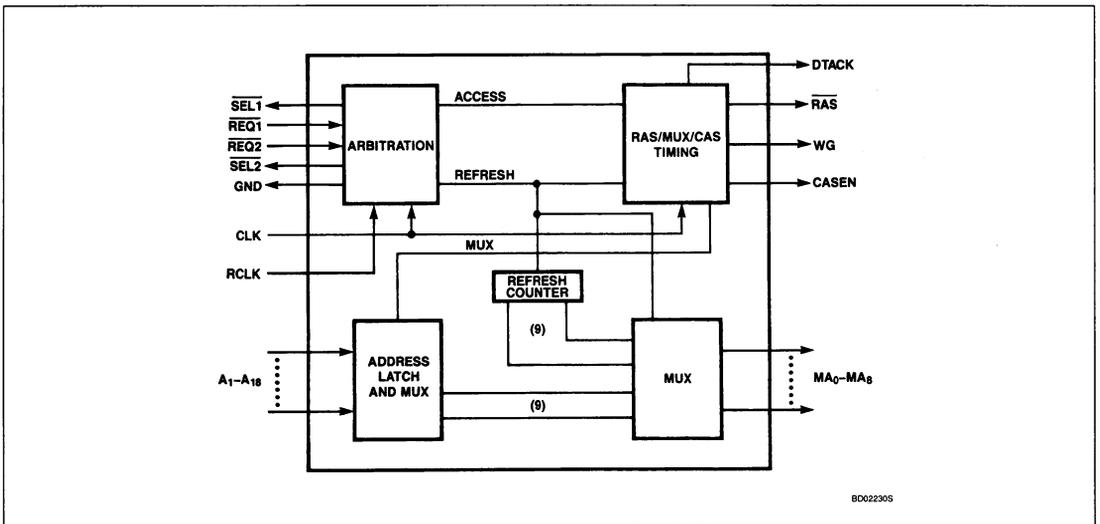
DRAM Controller

74LS765

PIN CONFIGURATION



BLOCK DIAGRAM



74LS1801 Bit Stream Manager

Encoder/Decoder
Product Specification

Logic Products

DESCRIPTION

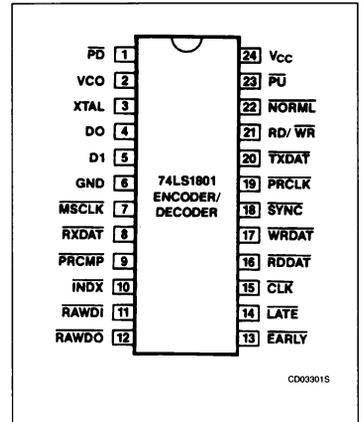
The 74LS1801 Encoder/Decoder (Figure 1) supports disk drive and data communications devices that require fast and reliable data separation capabilities. Although ideally suited for use with the 74LS1802 Serializer/Deserializer, the 74LS1801 is a flexible device which can be implemented in a variety of design applications.

Encoding is possible in FM, MFM, or Differential Manchester formats, making the 74LS1801 invaluable in designs requiring single density disk recording, double density disk recording, or in data communications applications. Included on-chip is a phase-comparator which can be bypassed; this feature is particularly useful in applications that use a complete external phase lock loop.

FEATURES

- Data rates up to 10MHz
- FM, MFM, and Differential Manchester encoding/decoding
- Precompensation in MFM write mode
- Built-in phase comparator
- Single 5V power supply
- Selectable encoding violation generation/detection formats

PIN CONFIGURATION



BLOCK DIAGRAM

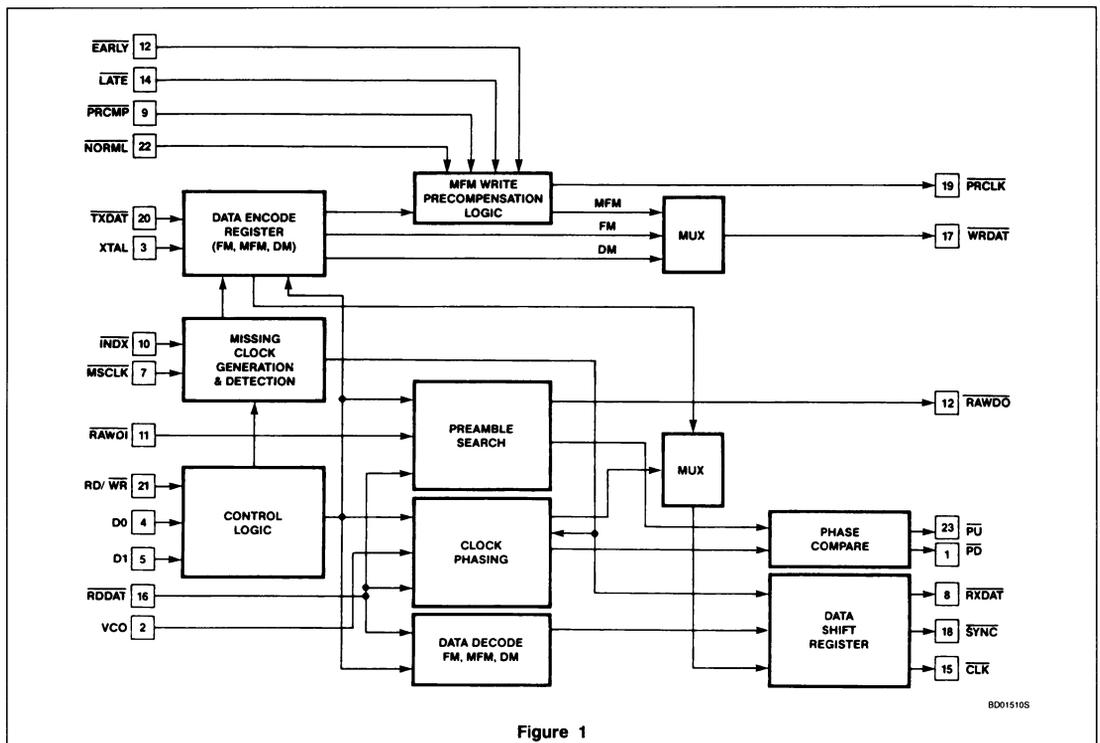
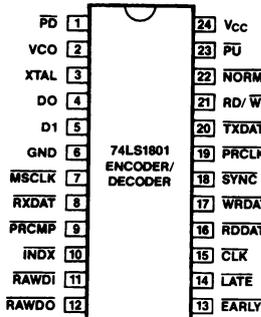


Figure 1

Bit Stream Manager

74LS1801

PIN CONFIGURATION



PIN NO.	IDENTIFIER	DESCRIPTION
10	$\overline{\text{INDX}}$	INDeX – an input that designates the missing clock pattern to be generated during the write mode; in the read mode, determines which data/clock pattern must be recognized as an address mark (Table 2, 3).
11	$\overline{\text{RAWDI}}$	RAW Data In – a shaped data pulse derived from $\overline{\text{RAWDO}}$. $\overline{\text{RAWDO}}$ is normally tied directly to $\overline{\text{RAWDI}}$.
12	$\overline{\text{RAWDO}}$	RAW Data Out – a shaped data pulse derived from $\overline{\text{RDDAT}}$ that can be processed through an external phase lock loop. $\overline{\text{RAWDO}}$ is normally tied directly to $\overline{\text{RAWDI}}$.
13	$\overline{\text{EARLY}}$	Modifies clock rate with respect to crystal reference when early precompensation is desired.
14	$\overline{\text{LATE}}$	Modifies clock rate with respect to crystal reference when late pre-compensation is desired.
15	$\overline{\text{CLK}}$	CLoCK – Clock input equal to the frequency of NRZ data.
16	$\overline{\text{RDDAT}}$	ReaD DATa – an input of encoded serial data (MFM, FM, or Differential Manchester) that is to be converted to NRZ data.
17	$\overline{\text{WRDAT}}$	WRite DATa – an output of encoded serial data (FM, MFM, or Differential Manchester) derived from NRZ data.
18	$\overline{\text{SYNC}}$	SYNChronization output – when active low, indicates recognition of valid encoding violation in the $\overline{\text{RDDAT}}$.
19	$\overline{\text{PRCLK}}$	PReCompensation CLoCK – an output used to excite an external delay line.
20	$\overline{\text{TXDAT}}$	Transmit Data – an input of NRZ data that is to be encoded to FM, MFM, or Differential Manchester data.
21	$\overline{\text{RD/WR}}$	ReaD/WRite – an input designating mode of operation: when high, a read is indicated; when low, a write is indicated.
22	$\overline{\text{NORML}}$	NORMaL – a clock input that is used when no precompensation is desired.
23	$\overline{\text{PU}}$	Pump UP – an output from the phase comparator that indicates the frequency of an external VCO is too low as compared to $\overline{\text{RDDAT}}$.
24	VCC	Supply voltage.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ\text{C to } +70^\circ\text{C}$
Hermetic DIP	N74LS1801I
Plastic DIP	N74LS1801N

Bit Stream Manager

74LS1801

FUNCTIONAL OPERATION

The 74LS1801 Encoder/Decoder serves to translate data between disk drive or data communications devices and the 74LS1802 Serializer/Deserializer (or comparable device). Information entering or leaving the Serializer/Deserializer interface is in the form of standard NRZ data and can be encoded to (or decoded from) one of three popular formats:

- Frequency Modulation (FM) — single density disk recordings.
- Modified Frequency Modulation (MFM) — double density disk recordings.
- Differential Manchester — data communications applications.

Read/Write and Format Control

The operational mode of the 74LS1801 is dictated by the RD/WR input: when low, a write (encode) is indicated; when high, a read (decode) is designated. In either mode, the format of data being decoded or encoded is controlled by the states of D0 and D1 inputs as shown below:

Table 1. Format Control

D0	D1	RESULTING FORMAT
L	L	MFM
H	L	FM
L	H	Differential Manchester

Following are discussions of the encoding and decoding functions of the 74LS1801, and the timing requirements necessary for accurate data transmittal.

Encoding Logic

When in the encode mode, NRZ data is input via the TXDAT input and, after about a three bit delay, is output on WRDAT. As described, output format is dependent on the states of D0 and D1. Address marks are distinguished from data by deleting clock pulses within the character.

These "missing clocks" are generated within the byte following a preamble of either all 0's (MFM and FM format) or all 1's (Differential Manchester format). As described in Table 2, clocks are eliminated according to inputs IND_X, MSCLK, and the specified encoding format.

When encoding data in the MFM format, MSCLK may be enabled during preamble generation and up to the beginning of an address mark. MSCLK can then be disabled during the byte following an address mark, or before the final bit of a four bit series in which the first two bits are 0's (e.g., before the final 0 in 0010). In applications utilizing consecutive A1 characters (such as in the case of floppy disk soft-sectored formats), MSCLK

Table 2. Missing Clocks

MSCLK	IND _X	FORMAT	RESULTING CLOCK PATTERN							
			Bit Cell Numbers:							
			0	1	2	3	4	5	6	7
L	H	FM			V	V	V			
L	L	FM			V		V			
L	H	Differential Manchester	V	V		V	V			
L	L	Differential Manchester	V	V			V			
L	X	MFM	2nd of 3 clocks missing							

NOTES:

- X = Don't care
- V = Missing Clock

Table 3. Address Mark Identification Requirements in Decode Mode

MSCLK	IND _X	CONDITIONS FOR ACTIVE SYNC OUTPUT
H	X	First '1' bit after preamble
L	H	A1 ₁₆ with missing clocks
L	L	Any byte with missing clocks

would remain active until the beginning of the byte following the A1 series.

The 74LS1801 also provides pre-compensation capabilities when encoding data in the MFM format. Activating the PRCMP signal (low) synchronizes output data according to a clock input provided on one of three inputs: EARLY — a clock shifted early in time, LATE — a clock shifted late in time, or NORML — a clock provided when no pre-compensation is needed. These inputs are supplied by an external delay line which, in turn, is excited by the PRCLK output (see Typical System Configuration, Figure 2.)

When encoding in FM or Differential Manchester formats, missing clocks are only generated in the first byte following a preamble of zeroes. The most significant bit of this byte must be a '1'; for example, address marks F8, FB, FC, or FE. MSCLK may be enabled up to the beginning of an address mark; once an address mark has been transmitted, it is not necessary to disable MSCLK.

Decoding Logic

In the decode mode, data (MFM, FM, or Differential Manchester) is input via the RDDAT input and, after an eleven bit delay, is output as NRZ data on RXDAT. As described above, input format is defined by the states of D0 and D1. In the MFM format, a minimum preamble length of 34 bits is required to allow for phase synchronization and location of an address mark; when in FM or Differential Manchester mode, a minimum length of 18 bits is required. After a preamble has been recognized, the 74LS1801 searches for an address mark. When an address mark is identified, the SYNC output becomes active low, and alerts the 74LS1802 of incoming data. Rules for positive address mark identifi-

cation are described below and summarized in Table 3.

When MSCLK is inactive, SYNC is activated on the first '1' data bit following a preamble of zeroes (MFM and FM) or 1's (Differential Manchester). Data is contained in the byte following this bit.

If MSCLK is active, the byte following a preamble of all zeroes is checked for the required missing clocks (Table 3) and if detected, SYNC is activated.

PHASE LOCK LOOP AND DATA SEPARATION LOGIC

Data/clock separation logic requires a clock pulse that is synchronous with read data (RDDAT); to create this signal, the 74LS1801 employs a Phase Lock Loop. In its simplest form, the PLL consists of an internal phase comparator, an external low pass filter and an external voltage controlled oscillator (VCO). Output from the VCO is continuously fed back to the phase compare circuit and contrasted with data read from the disk or communications device (RDDAT). A difference in phase is represented as one of two quantized output pulses: Pump Up indicates VCO frequency is too low, whereas Pump Down indicates that the VCO frequency is too high. The resulting output (PU or PD) is then processed by a low-pass filter which outputs a DC voltage proportional to the phase deviation. Accordingly, the VCO frequency is precisely serviced to the rate at which data was recorded. The 74LS1801 provides the capability to bypass internal phase compare logic; a typical application of this feature would be in designs implementing a complete external PLL.

Bit Stream Manager

74LS1801

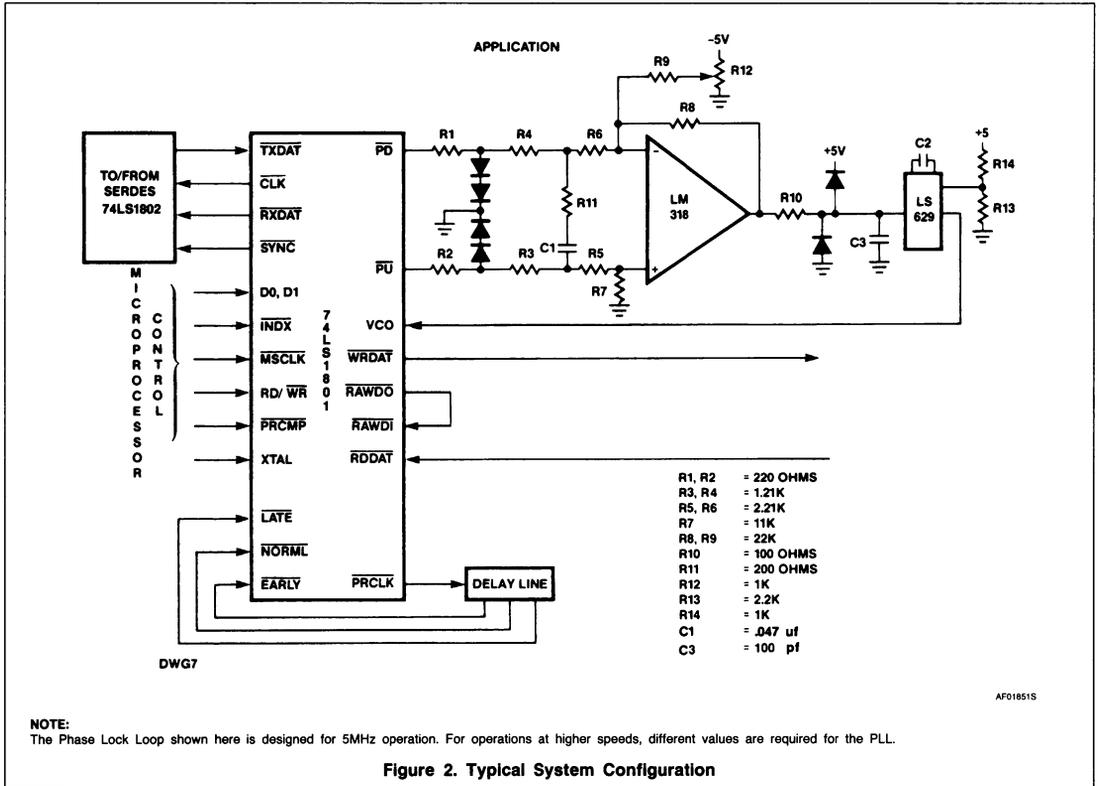


Figure 2. Typical System Configuration

Figure 3 illustrates this application and is discussed below.

RAW Data Out is a shaped data pulse derived directly from RDDAT. In MFM and FM modes, output is generated from the falling edge of RDDAT: in Differential Manchester mode, output is generated from both rising and falling edges. RAW Data In is a shaped data pulse derived from RAWDO and is used in internal data separation logic. The falling edge of RAWDI must be in phase with the falling edge of the VCO. RAWDI is normally tied directly to RAWDO.

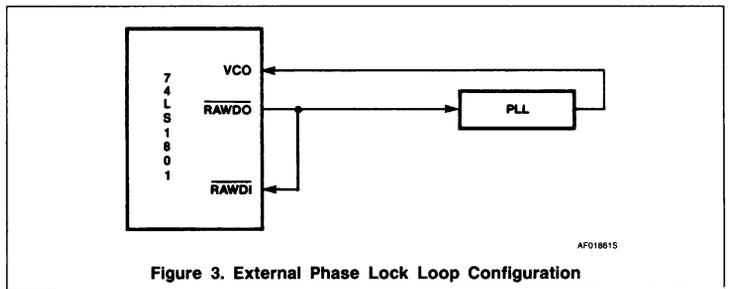
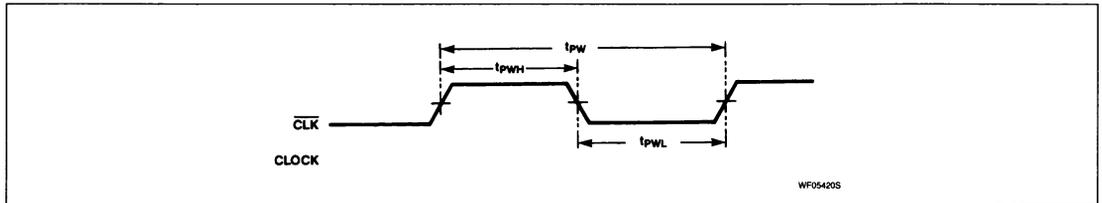


Figure 3. External Phase Lock Loop Configuration

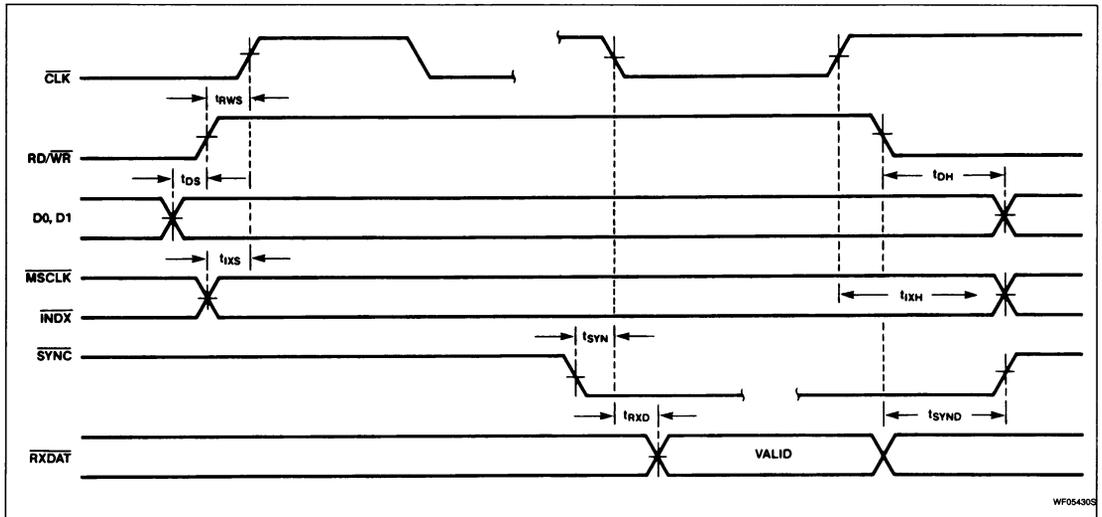
Bit Stream Manager

74LS1801

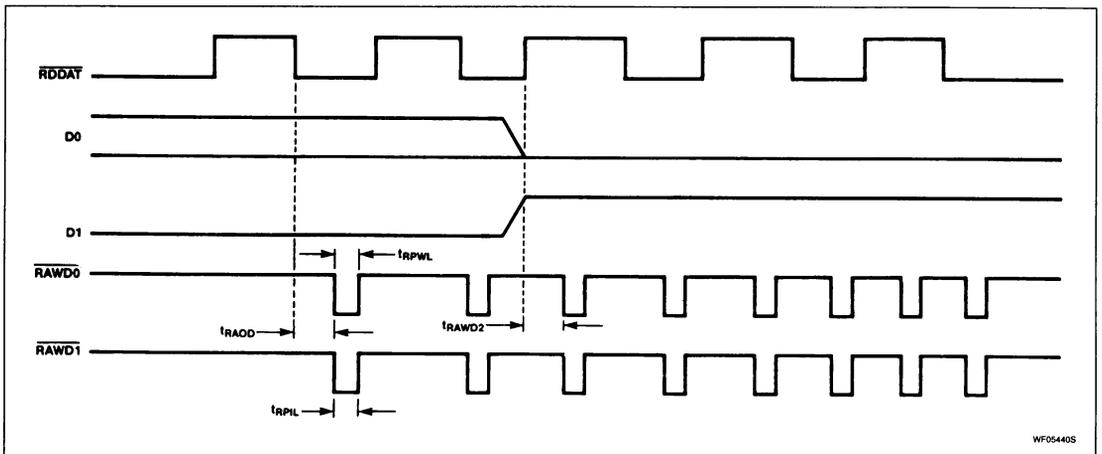
CLOCK CYCLE



READ CYCLE



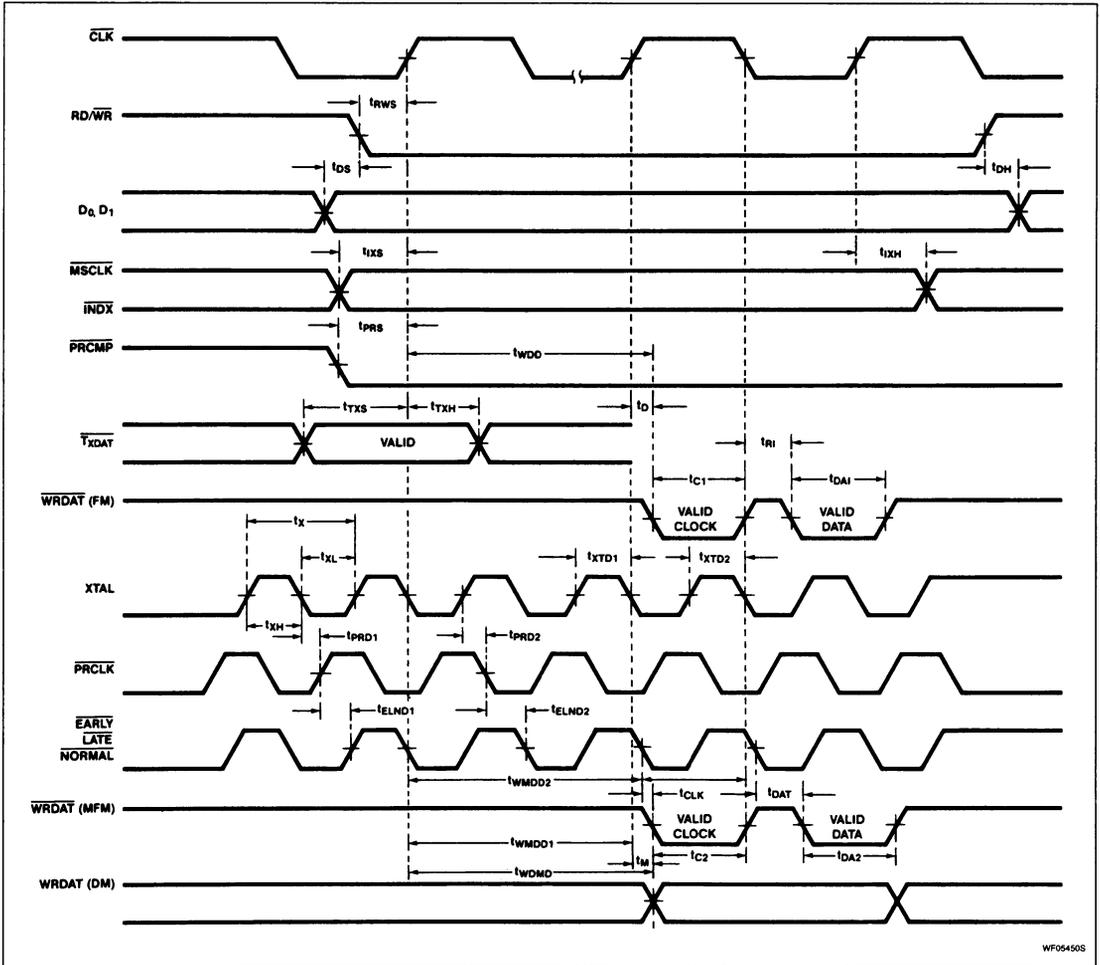
OTHER TIMING



Bit Stream Manager

74LS1801

WRITE CYCLE TIMING



WF054505

Bit Stream Manager

74LS1801

ABSOLUTE MAXIMUM RATINGS

PIN	DESCRIPTION	RATING	UNIT
V _{CC}	Supply voltage	+7.0	V
All other pins	Logic input pins	5.5	V

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V±5%; TA = 0°C to +70°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	COMMENTS
		Min	Typ	Max		
V _{TH}	Input threshold voltage	0.8		2.0	V	
V _{CD}	Input clamp diode voltage	I _N = -18mA		-1.2	V	
I _{IL}	Input low current	V _{IN} = 0.4V		-20	μA	
I _{IH}	Input high current	V _{IN} = 2.7V		20	μA	
I _I	Max input high current	V _{IN} = 5.5V		100	μA	
V _{OL}	Output voltage low	I _{OL} = 8mA		0.5	V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
		I _{OL} = 20mA		0.5	V	
V _{OH}	Output voltage high	V _{CC} = 4.5V	2.5		V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
		I _{OH} = 400μA I _{OH} = 1mA	2.5		V	
I _{OS}	Output short circuit current	V _{OUT} = 0	-15	-100	mA	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
		V _{OUT} = 1	-15	-100	mA	
I _{CC}	Supply current			184	mA	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t _{PW}	CLK pulse width	100		
t _{PWL}	CLK low time	50		
t _{PWH}	CLK high time	50		
t _X	XTAL cycle time	50		
t _{XH}	XTAL high time	25		
t _{XL}	XTAL low time	25		
t _{RWS}	RD/WR set-up to ↑CLK	0		
t _{DS}	D0, D1 set-up to RD/WR	0		
t _{IXS}	M _S CLK, I _N DX set-up to ↑CLK		35.2	
t _{SYN}	↓SYN _C to ↓CLK	2		
t _{RXD}	↓CLK to R _X DAT valid			4
t _{DH}	RD/WR to D0, D1 hold	0		
t _{SYND}	RD/WR to SYN _C inactive delay			36.4
t _{RAOD}	↓R _D DAT to ↓R _A W _D O delay		29.2	
t _{RPIL}	R _A W _D I pulse width	20*		
t _{RPWL}	R _A W _D O pulse width			40*
t _{WDMD}	T _X DAT to W _R DAT (DM)			t _{PW} + 41.2
t _M	↑CLK to W _R DAT delay		41.2	
t _{RAW_D2}	↑R _D DAT to ↓R _A W _D O delay		32.2	

Bit Stream Manager

74LS1801

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t _{DA2}	DATA bit duration		23.0	
t _{IXH}	↑CLK to MSCLK, IND _X hold		14.8	
t _{PRS}	PRC _{MP} set-up to ↑CLK			0
t _{TXS}	TXDAT set-up to ↑CLK		85.2	
t _{TXH}	TXDAT hold time		14.8	
t _{WDD}	TXDAT to WRDAT clock delay (FM data)		t _{PW} + 36.3	
t _P	↑CLK to clock delay (FM data)		36.3	
t _{C1}	Clock bit duration (FM)		19.0	
t _{R1}	Clock & data bit separation		31.0	
t _{DA1}	Data bit duration (FM)		19.0	
t _{XTD1}	↑XTAL to ↑CLK delay		35.2	
t _{XTD2}	↑XTAL to ↓CLK delay		32.2	
t _{PRD1}	↓XTAL to ↑PRCLK delay		26.3	
t _{PRD2}	↑XTAL to ↓PRCLK delay		28.3	
t _{ELND1}	↑PRCLK to Early, Late, Normal rising edge	1/2 t _{PW}		1/4 t _{PW}
t _{ELND2}	↓PRCLK to Early, Late, Normal falling edge	1/4 t _{PW}		0
t _{WMDD2}	TXDAT to WRDAT data delay (MFM)			3.5 x t _{PW}
t _{WMDD1}	TXDAT to WRDAT clock delay (MFM)			3.0 x t _{PW}
t _{CLK}	Early, Late, Normal falling edge to clock bit delay (MFM)		12.1	
t _{C2}	Clock bit duration (MFM)		23.0	
t _{DAT}	Early, Late, Normal falling edge to data bit delay (MFM)		12.1	

*Tabular entries with an asterisk are parameters that are guaranteed at the values listed; these values were determined either by system bench testing or by Signetics' characterization procedures. All other tabular entries are taken directly from simulation results run at range of operational frequencies; these values are not tested or guaranteed.

74LS1802 Bit Stream Manager

Serializer/Deserializer
Product Specification

Logic Products

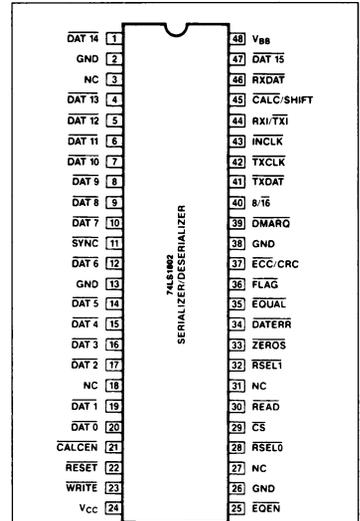
DESCRIPTION

The 74LS1802 Serializer/Deserializer (Figure 1) incorporates speed, flexibility, and proven ISL technology into a general-purpose device that performs many of the functions necessary for the implementation of a disk or communications controller. On-chip serializing/deserializing, programmable ECC and CRC operation, and bit comparison logic (useful for address-mark or header comparisons) make for a truly versatile device. A selectable 8- or 16-bit data bus and associated control lines allow for a DMA interface which requires little external hardware — a minimum system may be easily built with a microcontroller, a DMA controller, a RAM buffer, disk control lines and interface logic.

FEATURES

- Data rates up to 10MHz
- Selectable CRC-16 or CRC-CCITT polynomials
- Full Duplex operation with CRC/ECC on receive data
- Programmable ECC polynomial register
- Programmable control register
- On-chip bit comparator
- 8- or 16-bit selectable data bus
- 48-pin DIP

PIN CONFIGURATION



CD006315

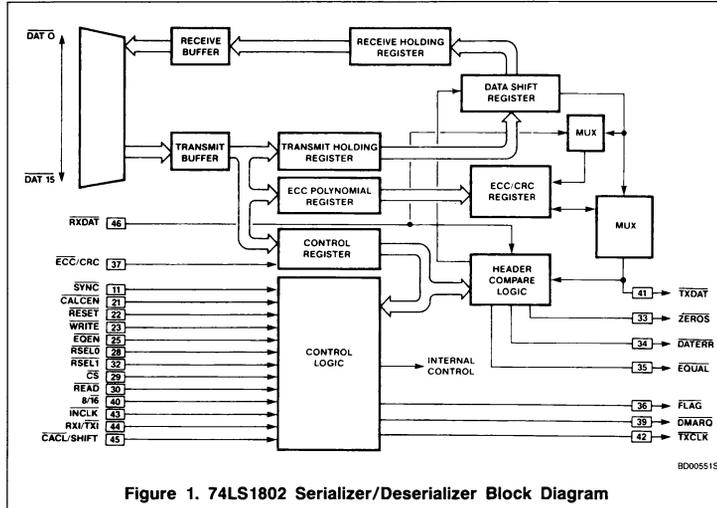
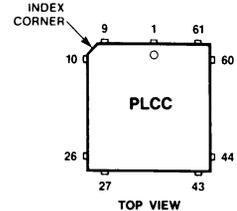


Figure 1. 74LS1802 Serializer/Deserializer Block Diagram



CD0068PS

PLCC	FUNCTION	PLCC	FUNCTION	PLCC	FUNCTION
1	VBB	24	DAT 2	47	ZEROS
2	DAT 14	25	NC	48	DATERR
3	GND	26	NC	49	EQUAL
4	NC	27	NC	50	FLAG
5	DAT 13	28	DAT 1	51	ECC/CRC
6	DAT 12	29	DAT 0	52	NC
7	DAT 11	30	CALCEN	53	GND
8	NC	31	NC	54	DMARQ
9	NC	32	RESET	55	NC
10	NC	33	NC	56	8/T6
11	NC	34	WRITE	57	TXDAT
12	DAT 10	35	VCC	58	TXCLK
13	DAT 9	36	EOEEN	59	NC
14	DAT 8	37	GND	60	NC
15	NC	38	NC	61	NC
16	DAT 7	39	RSEL0	62	NC
17	SYNC	40	CS	63	INCLK
18	DAT 6	41	READ	64	RXI/TXI
19	GND	42	NC	65	CALC/SHIFT
20	NC	43	NC	66	RXDAT
21	DAT 5	44	NC	67	NC
22	DAT 4	45	NC	68	DAT 15
23	DAT 3	46	RSEL1		

Bit Stream Manager

74LS1802

PIN DESCRIPTION

			PIN NO.	IDENTIFIER	DESCRIPTION	
1	DAT 14	48	V _{BB}	27	NC	Not connected.
2	GND	47	DAT 15	28	RSEL0	Register SELECT—inputs that designate which input register (Control Register, Transmit Hold Register or ECC Polynomial Register) is to be written into.
3	NC	46	RXDAT	32	RSEL1	
4	DAT 13	45	CALC/SHIFT	29	\overline{CS}	Chip Select—when active low, this input enables READ and WRITE lines for data transactions.
5	DAT 12	44	RXI/ \overline{TXI}	30	READ	When active low, this input enables data transfer from the Receive Hold Register onto the Data Bus.
6	DAT 11	43	INCLK	31	NC	Not connected.
7	DAT 10	42	TXCLK	33	ZEROS	When active low, this output indicates that both bits under comparison are in 0 state and vice versa.
8	DAT 9	41	TXDAT	34	DATERR	DATa ERRor—when active low, this output indicates that an ECC/CRC error has been detected.
9	DAT 8	40	8/ $\overline{16}$	35	EQUAL	When active low, this output indicates that both bits in the bit comparator are in the same state.
10	DAT 7	39	DMARQ	36	FLAG	An active low output pulse generated every 8- or 16-bits; FLAG indicates that data is available in receive mode or is requested in transmit mode.
11	SYNC	38	GND	37	ECC/CRC	When this input is low, the 32-bit ECC circuit is selected; when high, the 16-bit CRC circuit is selected.
12	DAT 6	37	ECC CRC	38	GND	Ground.
13	GND	36	FLAG	39	DMARQ	DMA ReQuest—when active low, this output indicates that data is available either in receive mode or is requested in transmit mode. (See control register description.)
14	DAT 5	35	EQUAL	40	8/ $\overline{16}$	When low, this input designates 16-bit operation; when high, 8-bit operation is selected.
15	DAT 4	34	DATERR	41	TXDAT	Transmit Data – NRZ transmit data.
16	DAT 3	33	ZEROS	42	TXCLK	Output clock with frequency equal to receive and transmit data.
17	DAT 2	32	RSEL1	43	INCLK	Input clock with frequency equal to receive and transmit data.
18	NC	31	NC	44	RXI/ \overline{TXI}	When low, this input designates transmit mode; when high, receive mode is selected.
19	DAT 1	30	READ	45	CALC/SHIFT	When low, this input causes the error detection circuit to generate the syndrome bytes. At the end of a data or ID field, CALC/SHIFT is forced high to shift out check bits (transmit mode), or compare these bits with received check bits (receive mode).
20	DAT 0	29	\overline{CS}	46	RXDAT	Receive data – NRZ receive data.
21	CALCEN	28	RSEL0	48	V _{BB}	Supply voltage for internal circuits.
22	RESET	27	NC			
23	WRITE	26	GND			
24	V _{CC}	25	EQEN			

Bit Stream Manager

74LS1802

FUNCTIONAL OPERATION

As shown in Figure 1, data I/O is facilitated by either an 8- or 16-bit bus. A high at 8/16 input puts the 74LS1802 into an 8-bit mode; when low, a 16-bit mode is indicated. Incoming data on the bus takes one of three forms: transmit data to be serialized, ECC polynomial specification data, or control register information. The 74LS1802 is informed of the type of input data through the RSELO and RSELT inputs, and as shown in Table 1, data is placed in one of three registers:

Table 1. Input Data Register Designations

RSELO	RSELT	REGISTER NAME
L	H	Cont Reg
H	L	Xmit Hold Reg
H	H	ECC Polyn Reg

Control Register

The Control Register shown in the accompanying diagram is a 5-bit register which can be programmed to implement the following modes/functions.

MSB				LSB	
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Where,

- Bit 0 = LEDGE/TEDGE
- Bit 1 = ECC PRESET
- Bit 2 = CRC PRESET
- Bit 3 = EQUAL/LATCH
- Bit 4 = CRC16/CRC-CCITT

Bit 0 (LEDE/TEDGE)

The falling edge of DMARQ indicates to an external DMA device to perform a Read or a Write. If the LEDGE/TEDGE bit is set to 0, DMARQ is terminated by the rising edge of READ or WRITE; when this bit is set to 1, DMARQ is terminated by the falling edge of READ or WRITE.

Bit 1 (ECC PRESET)

The ECC shift register must be preset to either all 0's or all 1's to be compatible with existing systems. When the ECC PRESET bit is set to 0, the ECC shift register is preset to 1's. When set to 1, the shift register is set to 0's.

Bit 2 (CRC PRESET)

To be compatible with existing systems, the CRC shift register must be preset to either all 0's or all 1's. For example, IBM 3740 and SYSTEM 34 compatible floppy disks require that the CRC shift register be preset to 1's, while Intel ISIS compatible disks require that this register be set to 0's. When the CRC PRESET bit is set to 0, the CRC shift register is preset to 1's; when set to 1, this register is set to 0's.

Bit 3 (EQUAL/LATCH)

The EQUAL output indicates the status of an internal bit-comparator. When the EQUAL/LATCH bit is set to 0, EQUAL reflects the status of the bit comparator on a per-bit basis. When set to 1, EQUAL is latched on the first mismatch between receive and transmit data - this condition is cleared (i.e., EQUAL is returned to a high state) when SYNC goes high.

Bit 4 (CRC16/CCITT)

When set to 0, the CRC circuit selects the standard CRC-16 polynomial ($X^{16} + X^{15} + X^2 + 1$); when set to 1, the standard CRC-CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$) is selected.

Transmit Hold Register

The main function of the Transmit Hold Register is to hold a byte/word in reserve, ready for transmission.

Before data is transmitted, it is loaded into the Transmit Hold Register. SYNC is externally activated to start the transmit process. This in turn activates FLAG, and DMARQ. Generation of FLAG and DMARQ indicates that the contents of the Transmit Hold Register have been loaded into the Data Shift Register. Hence, the next byte/word of data should be loaded into the Transmit-Hold Register.

ECC POLYNOMIAL REGISTER

This register is composed of 32 bits, each bit representing an X-term. It is selected by writing a one to the appropriate bit. An ECC polynomial is loaded by writing four consecutive bytes (least significant byte first) into the register. Thus the polynomial $X^{32} + X^{23} + X^{21} + X^{11} + X^8 + X^2 + 1$ would be programmed as follows:

BYTE NO.	DATA	
	MSB	LSB
	D7	D0
1	0 0 0 0 0 1 0 X	
2	0 0 0 0 1 0 0 1	
3	1 0 1 0 0 0 0 0	
4	0 0 0 0 0 0 0 0	

X = Don't care

The following would appear in the register as:

$$\begin{array}{cccccccc}
 X^{32} & & & & & & & X^{23} X^{21} \\
 1 & 00000000 & 10100000 & & & & & \\
 & & & X^{11} X^8 & & X^2 X^0 & & \\
 & 00001001 & 00000101 & & & & &
 \end{array}$$

with X^0 and X^{32} set to 1 by default.

ADDRESS MARK OR HEADER COMPARISONS

A bit comparator in the 74LS1802 compares one bit of received data with one bit of transmitted data; two status lines, EQUAL

and ZEROS, reflect the result of the comparison. When active low, EQUAL indicates both bits are in the same state, while ZEROS indicates the status of the bits under comparison. In this mode the chip is operating in a full duplex mode with CRC/ECC being performed on the receive data.

EQUAL can be used to detect a specific address mark or disk header. The expected header to be identified is loaded into the Transmit Hold Register, and RXI/TXI is set low for transmit mode. The SYNC input originates from the 74LS1801 Encoder/Decoder, and when active low, indicates that data following a preamble of 0's may be an address mark (see 74LS1801 Decoding Logic). Thus, EQUAL and ZEROS reflect the actual status of the bit comparator when SYNC is active low; when SYNC is inactive high, EQUAL and ZEROS are held active. Note that SYNC must be reset at the end of a header in preparation for a following read or write.

As specified by the EQUAL/LATCH Bit in the Control Register, the bit comparator operates in one of two modes. When the control bit is 0, EQUAL reflects the status of the bit comparator on a per-bit basis. When the control bit is 1, EQUAL is latched on the first mismatch between received and transmitted data and stays in this mode until SYNC becomes inactive high.

TRANSMITTING DATA

To transmit data, several initializations must take place: RXI/TXI must be held low to indicate a transmit operation, ECC/CRC is set to the appropriate state, and CALC/SHIFT must be held low to put the ECC/CRC circuit into "calculate mode." After the first byte/word of data has been loaded into the Transmit Hold Register, SYNC must be externally activated (low) to begin the transmit process. Activating SYNC forces the FLAG and DMARQ lines to go active, after which the next byte/word of data may be loaded into the device. Thereafter, FLAG and DMARQ will go active every 8 or 16 bits to request more data.

CALCEN may be activated to enable the ECC/CRC circuit before the start of the byte that is to be included in the ECC/CRC calculations. While the last byte of the data or header field is being shifted-out, CALC/SHIFT must be forced high, causing the ECC/CRC check bits to be shifted out after the data. As a result, SYNC must be held active low for at least 32 bits (ECC) or 16 bits (CRC) following the last bit of the data field. Typical timing for a transmit operation is shown in Figure 2.

Bit Stream Manager

74LS1802

RECEIVING DATA

Several conditions must be fulfilled before a receive operation takes place. RXI/TXI is held high to indicate a receive operation, ECC/CRC is set to the appropriate state, and CALC/SHIFT is held low to put the ECC/CRC circuit into "calculate mode." If the address mark is to be included in ECC/CRC calculations, CALCEN may be activated low at this time. Once these conditions have been fulfilled, receive data can be enabled.

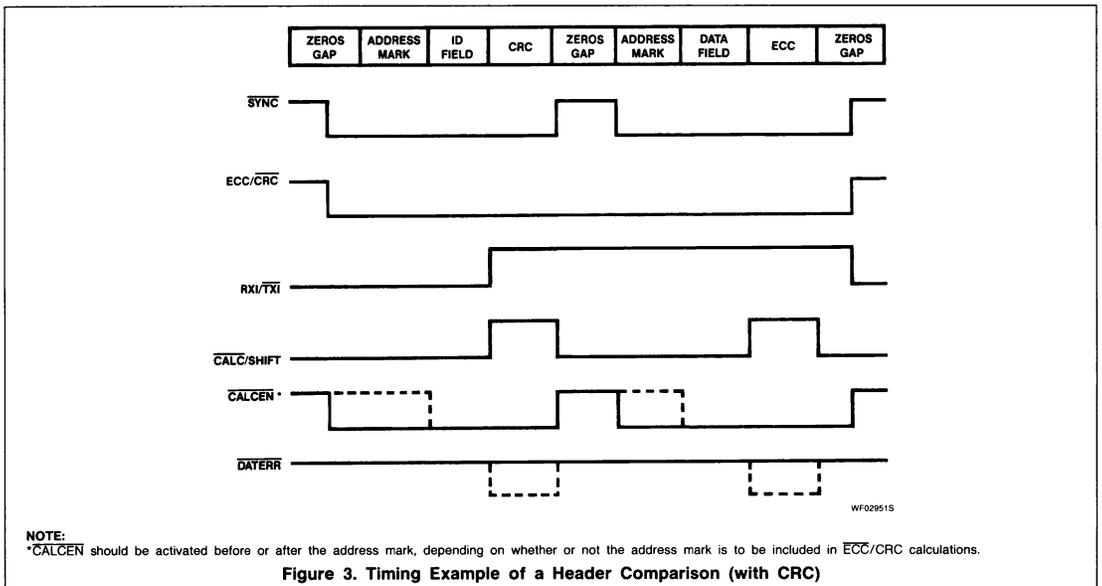
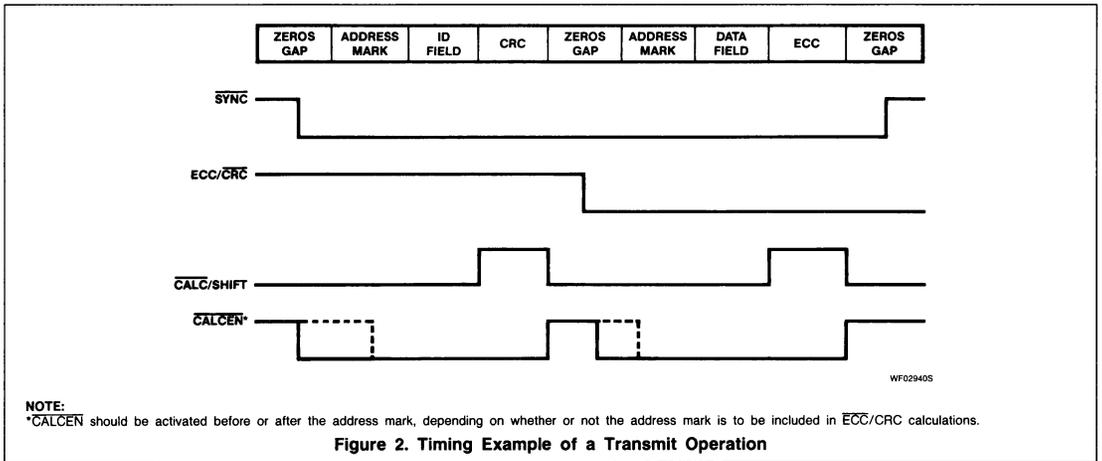
When SYNC is activated, a counter circuit sets up either 8- or 16-bits of data and generates active FLAG and DMARQ outputs to indicate data available in the Receive Hold Register. This continues until SYNC becomes high.

While the last byte of data is being received CALC/SHIFT must be forced high to put the ECC/CRC circuit into "checkmode" at the beginning of the next byte. At this time, check bits on receive data are compared to check bits appended to the end of the data field; if

the two groups of bits do not match, DATERR is activated. DATERR is latched internally and is cleared when SYNC goes inactive.

Note that SYNC must be held active until all check bits (32 for ECC, 16 for CRC) have been compared. The result of the bit comparison is held in the Receive Hold Register. If no error occurred, the Receive Hold Register will be set to 0's, otherwise these bytes are used in the correction process.

Typical timing for a header comparison (with CRC) is shown in Figure 3.

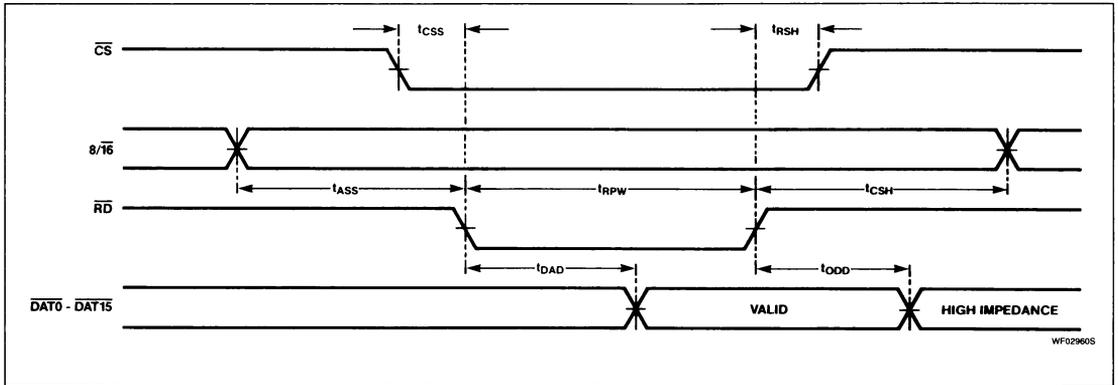


7

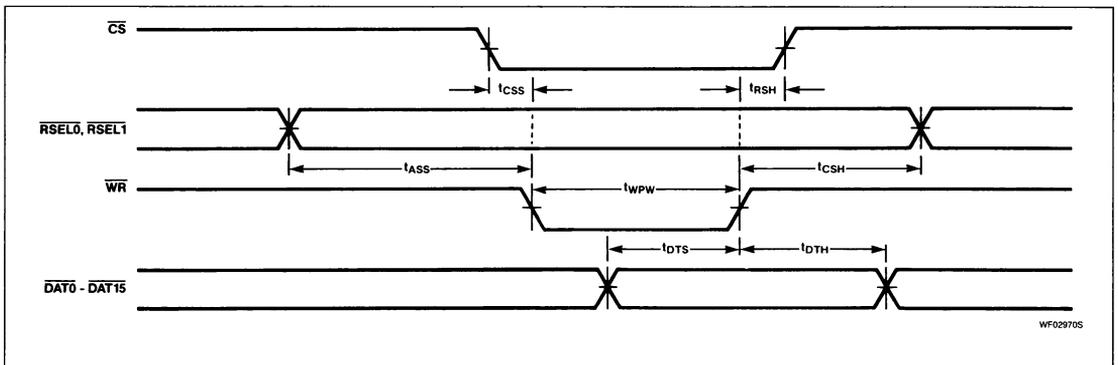
Bit Stream Manager

74LS1802

READ CYCLE TIMING



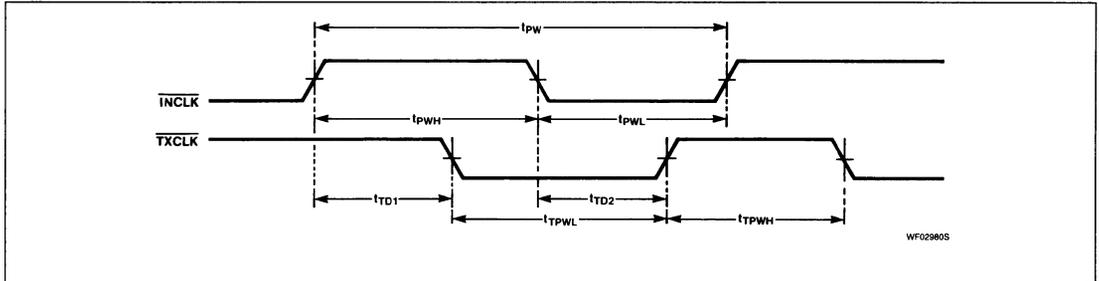
WRITE CYCLE TIMING



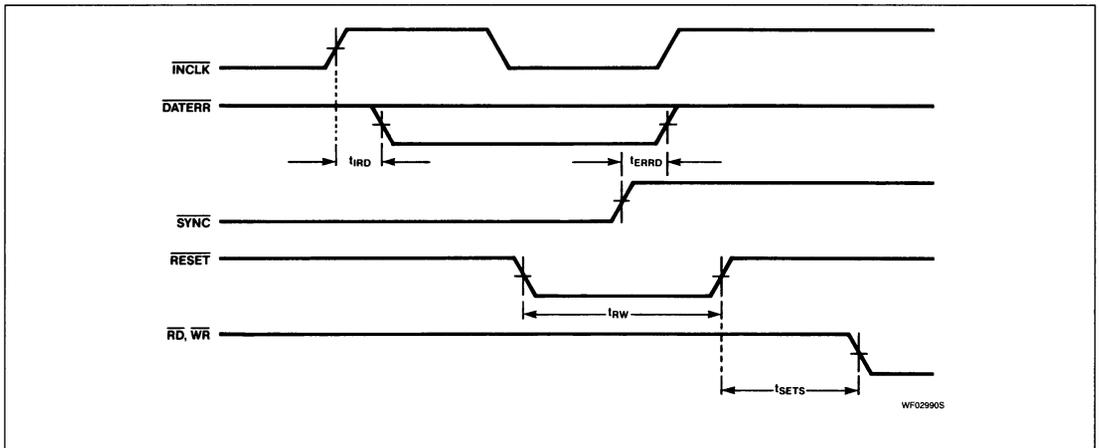
Bit Stream Manager

74LS1802

CLOCK CYCLE TIMING



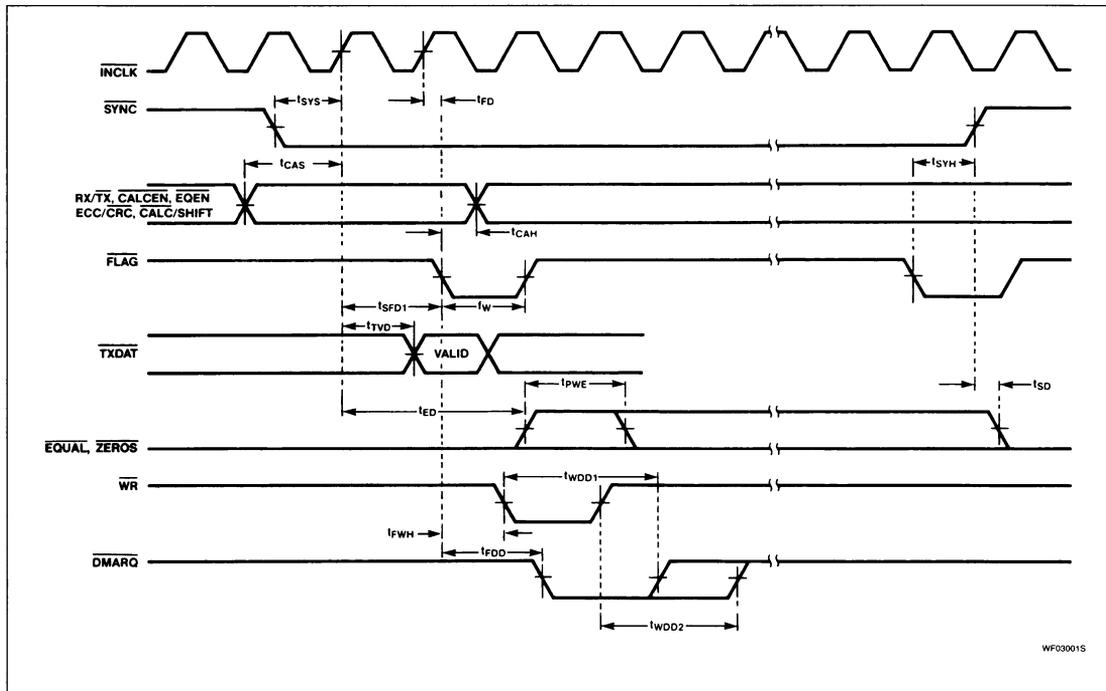
OTHER TIMING



Bit Stream Manager

74LS1802

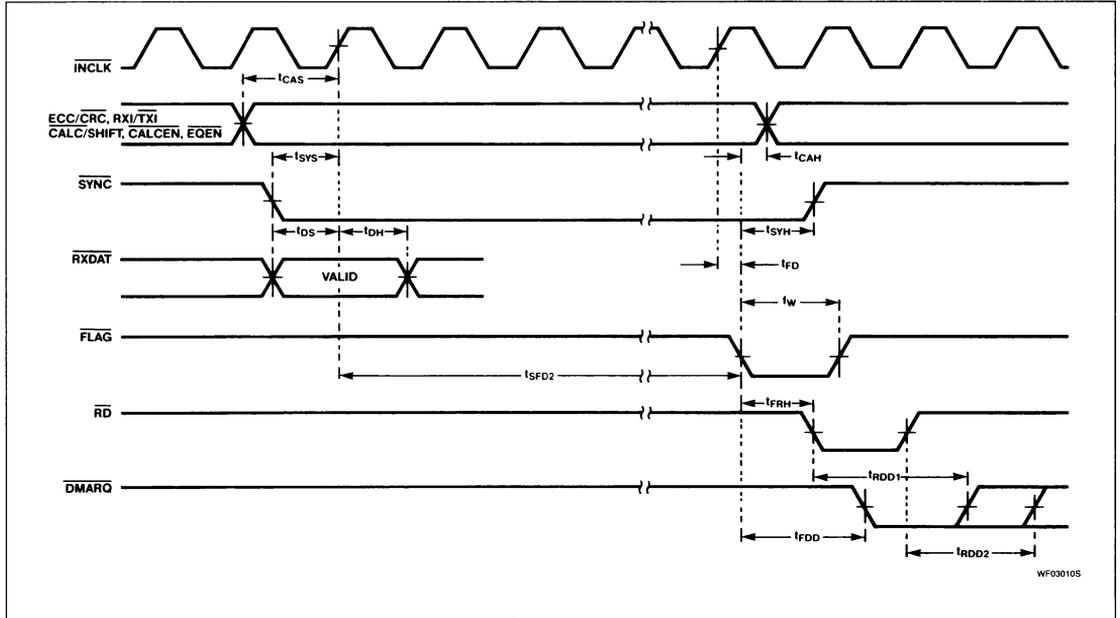
TRANSMIT, CRC/ECC CALCULATE AND SHIFT TIMING



Bit Stream Manager

74LS1802

RECEIVE, ECC/CRC CALCULATE AND RECEIVE TIMING



Bit Stream Manager

74LS1802

ABSOLUTE MAXIMUM RATINGS

PIN	DESCRIPTION	RATING	UNIT
V _{CC}	Supply voltage	+7.0	V
All other	Logic input pins	5.5	V

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	COMMENTS
		Min	Typ	Max		
V _{CD} Input clamp diode voltage	I _{IN} = 18mA			-1.5	V	
V _{TH} Input threshold voltage		0.8		2.0	V	
I _{IL} Input low current	V _{IN} = 0.4V			-20	μA	
I _{IH} Input high current	V _{IN} = 2.7V			20	μA	
I _I Max input high current	V _{IN} = 5.5V			100	μA	
V _{OL} Output low voltage	I _{OH} = 8mA			0.5	V	
V _{OH} Output high voltage	I _{OL} = -400μA	2.7			V	
I _{OS} Output short circuit current	V _{OUT} = 0V	-15		-100	mA	
I _{CC} Power supply current (buffers)				75	mA	
I _{BB} Power supply current (gates)				260	mA	

Bit Stream Manager

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AC ELECTRICAL CHARACTERISTICS (all time in nanoseconds)

PARAMETER	DESCRIPTION	LIMITS		
		Min	Typ	Max
t _{PDH}	INCLK High time	50		
t _{PWL}	INCLK Low time	50		
t _{PDH}	TXCLK High time	50		
t _{PWL}	TXCLK Low time	50		
t _{PWE}	EQUAL, ZEROS High time		t _{PW}	
t _W	FLAG Low time		98	
t _{RW}	RESET Low time		50	
t _{WPW}	WR Pulse width		50	
t _{RPW}	RD Pulse width		100	
t _{PW}	INCLK Cycle time	100		
t _{CSS}	CS set-up to ↓WR and ↓RD	0		
t _{ASS}	RSEL0, RSEL1 8/16 set-up to ↓RD and ↓WR		35	
t _{SETS}	RESET set-up to ↓RD, ↓WR		52	
t _{DTS}	DAT0 - DAT15 set-up to ↑WR		35	
t _{SYS}	SYNC set-up to ↑INCLK		1/2 t _{PW}	
t _{CAS}	RX/TX, ECC/CRC, CALC/SHIFT, CALCEN, EQEN set-up to ↑INCLK		t _{PW}	
t _{FD}	↑INCLK to ↓FLAG delay		2	
t _{DS}	RXDAT VALID TO ↑INCLK		1/2 t _{PW}	
t _{RDD1}	↓RD to ↑DMARQ		86	
t _{RDD2}	↑RD to ↑DMARQ		81	
t _{SFD1}	↑INCLK to ↓FLAG		t _{PW} + 2	
t _{ED}	↑INCLK to ↑EQUAL, ZEROS delay		t _{PW} + 91	
t _{TD1}	↑INCLK to ↓TXCLK		46	
t _{TD2}	↓INCLK to ↑TXCLK		33	
t _{RSH}	↑RD, ↑WR to CS hold	0		
t _{CSH}	↑RD, ↑WR to RSEL0, RSEL1, 8/16 hold		19	
t _{DTH}	↑WR to DAT0 - DAT15 hold		150	
t _{FWH}	↓FLAG to ↓WR	0		
t _{CAH}	↓FLAG to CALC/SHIFT, EQEN, CALCEN, ECC/CRC, RX/TX hold	0		
t _{DAD}	↓RD to DAT0 - DAT15 valid		59	
t _{IRD}	↑INCLK to ↓DATERR		7	
t _{TVD}	↑INCLK to TXDAT valid		49	
t _{ODD}	↑RD to DAT0 - DAT15 changing		50	
t _{ERRD}	↑SYNC to ↑DATERR		44	
t _{DH}	↑INCLK to RXDAT hold		1/2 t _{PW}	
t _{FRH}	↓FLAG to ↓RD	0		
t _{SYH}	↓FLAG to SYNC hold	0		
t _{SD}	↑SYNC to ↓EQUAL		76	
t _{FDD}	↓FLAG to ↓DMARQ delay		12	
t _{WDD1}	↓WR to ↑DMARQ delay		86	
t _{WDD2}	↑WR to ↑DMARQ delay		81	
t _{SFD2}	↑INCLK to ↓FLAG		9 t _{PW} + 2	

NOTE:

All tabular entries are taken directly from simulation. No values are tested or guaranteed.

74LS1811 Bit Stream Manager

Encoder/Decoder
Preliminary Specification

Logic Products

DESCRIPTION

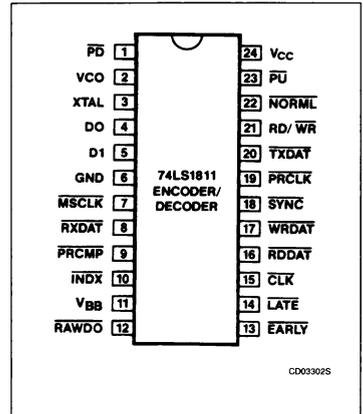
The 74LS1811 Encoder/Decoder (Figure 1) supports disk drive and data communications devices that require fast and reliable data separation capabilities. Although ideally suited for use with the 74LS1812 Serializer/Deserializer, the 74LS1811 is a flexible device which can be implemented in a variety of design applications.

Encoding is possible in FM, MFM, or Differential Manchester formats, making the 74LS1811 invaluable in designs requiring single density disk recording, double density disk recording, or in data communications applications. Included on-chip is a phase-comparator which can be bypassed; this feature is particularly useful in applications that use a complete external phase lock loop.

FEATURES

- FM, MFM, and Differential Manchester encoding/decoding
- Precompensation in MFM write mode
- Built-in phase comparator
- Single 5-volt power supply
- Selectable encoding violation generation/detection formats
- Data Rates:
 - FM 16MHz
 - MFM 20MHz
 - DM 20MHz

PIN CONFIGURATION



CD00302S

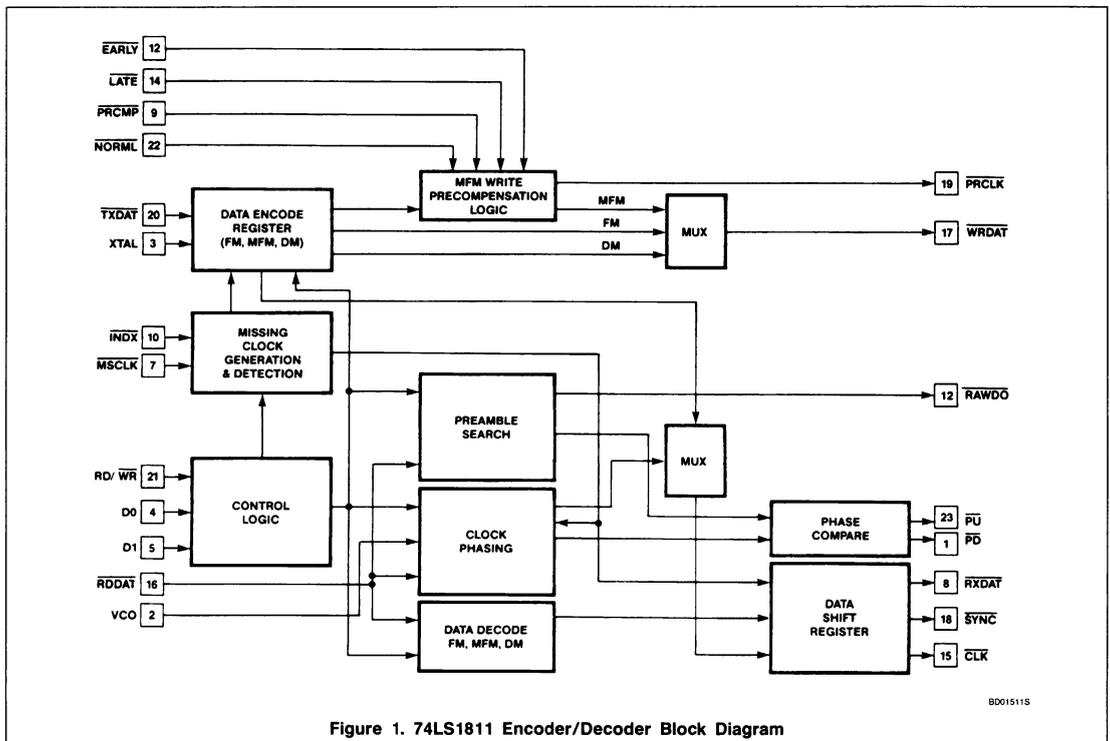


Figure 1. 74LS1811 Encoder/Decoder Block Diagram

B001511S

74LS1812 Bit Stream Manager

Serializer/Deserializer
Preliminary Specification

Logic Products

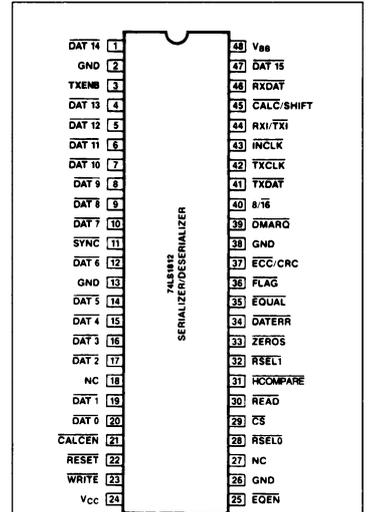
DESCRIPTION

The 74LS1812 Serializer/Deserializer (Figure 1) incorporates speed, flexibility, and proven ISL technology into a general-purpose device that performs many of the functions necessary for the implementation of a disk or communications controller. On-chip serializing/deserializing, programmable ECC and CRC operation, and bit comparison logic (useful for address-mark or header comparisons) make for a truly versatile device. A selectable 8- or 16-bit data bus and associated control lines allow for a DMA interface which requires little external hardware — a minimum system may be easily built with a microcontroller, a DMA controller, a RAM buffer, disk control lines and interface logic.

FEATURES

- Data rates up to 30MHz
- Selectable CRC-16 or CRC-CCITT polynomials
- Full Duplex operation with CRC/ECC on receive data
- Programmable ECC polynomial register
- Programmable control register
- On-chip bit comparator
- 8- or 16-bit selectable data bus
- 48-pin DIP or 68-pin PLCC

PIN CONFIGURATION



CD000325

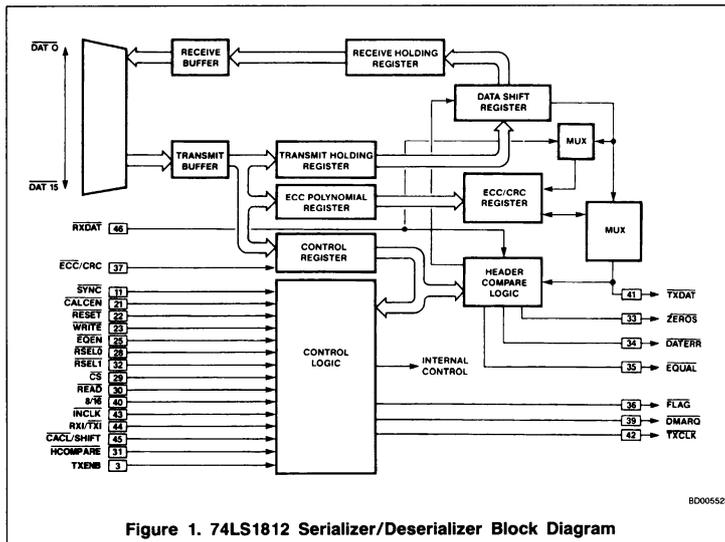
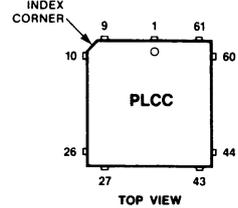


Figure 1. 74LS1812 Serializer/Deserializer Block Diagram

BD000552S



CD00068PS

PLCC FUNCTION	PLCC FUNCTION	PLCC FUNCTION
1 VBB	24 DAT 2	47 ZEROS
2 DAT 14	25 NC	48 DATERR
3 GND	26 NC	49 EQUAL
4 NC	27 NC	50 FLAG
5 DAT 13	28 DAT 1	51 ECC/CRC
6 DAT 12	29 DAT 0	52 NC
7 DAT 11	30 CALCEN	53 GND
8 NC	31 NC	54 DMARQ
9 TXENB	32 RESET	55 NC
10 NC	33 NC	56 8/16
11 NC	34 WRITE	57 TXDAT
12 DAT 10	35 VCC	58 TXCLK
13 DAT 9	36 EOEN	59 NC
14 DAT 8	37 GND	60 HCOMPARE
15 NC	38 NC	61 NC
16 DAT 7	39 RSEL0	62 NC
17 SYNC	40 CS	63 INCLK
18 DAT 6	41 READ	64 RXI/TXI
19 GND	42 NC	65 CALC/SHIFT
20 NC	43 NC	66 RXDAT
21 DAT 5	44 NC	67 NC
22 DAT 4	45 NC	68 DAT 15
23 DAT 3	46 RSEL1	

2960 Error Detection and Correction (EDC) Unit

Product Specification

Logic Products

FEATURES

- **Boosts Memory Reliability** — Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold.
- **Very High Speed** — Perfect for MOS microprocessor, minicomputer and mainframe systems.
 - Data in to error detect: 32ns worst case.
 - Data in to corrected data out: 65ns worst case.
- **High-performance systems can use the Signetics EDC in the check-only mode to avoid memory system slowdown.**
- **Replaces 25 to 50 MSI chips** — All necessary features are built-in to the Signetics 2960, including

diagnostics, data in, data out and check bit latches.

- **Handles Data Words From 8 to 64 Bits** — The Signetics 2960 is cascadable: 1 EDC for 8 or 16 bits, 2 for 32 bits, 4 for 64 bits.
- **Easy Byte Operations** — Separate byte enables on the data out latch simplify the steps and cuts the time required by byte writes.
- **Built-In Diagnostics** — The processor may completely exercise the EDC under software control to check for proper operation.

ing to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the EDC will correct any single-bit error and will detect all double- and some triple-bit errors. For 16-bit words, 6 check bits are used. The 2960 can be expanded to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Signetics 2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions.

The product is supplied in a 48-lead hermetic DIP package and a 48-pin plastic package.

DESCRIPTION

The Signetics 2960 Error Detection and Correction Unit (EDC) (Figure 1) contains the logic necessary to generate check bits on a 16-bit data field accord-

BLOCK DIAGRAM

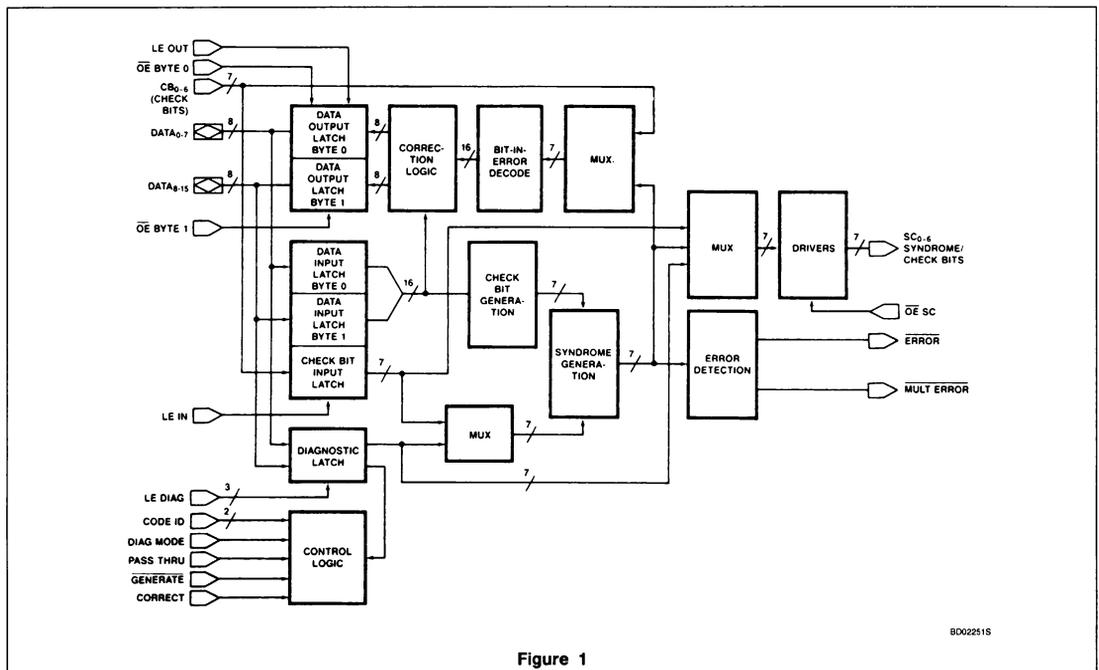
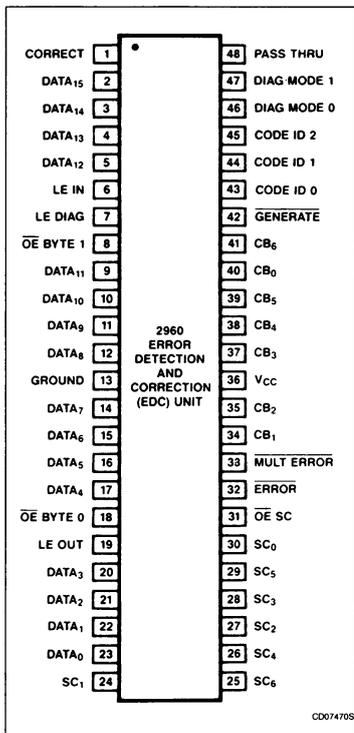


Figure 1

Error Detection and Correction (EDC) Unit

2960

PIN CONFIGURATION



ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N2960N
Hermetic DIP	N2960I

PIN DESCRIPTION

PIN NO.	IDENTIFIER	FUNCTION
1	Correct	Correct input: When HIGH this signal allows the correction network to correct any single-bit error in the Data input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDC will drive data directly from the Data input latch to the Data Output Latch without correction.
2-5 9-12 14-17 20-23	DATA ₁₅₋₁₂ DATA ₁₁₋₈ DATA ₇₋₄ DATA ₃₋₀	16 Bidirectional Data Lines: They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. DATA ₀ is the least significant bit; DATA ₁₅ is the most significant.
6	LE IN	Latch Enable: Data Input Latch. Controls latching of the input data. When HIGH the Data input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
7	LE DIAG	Latch Enable: Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID ₀₋₂ , DIAG MODE ₀₋₁ , CORRECT and PASS THRU.

Error Detection and Correction (EDC) Unit

2960

PIN DESCRIPTION (Continued)

PIN NO.	IDENTIFIER	FUNCTION
18, 8	OE BYTE 0, OE BYTE 1	Output Enable: Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.
13	GND	Ground.
19	LE OUT	Latch Enable: Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.
24, 25 – 30	SC ₁ SC ₆ – S ₀	Syndrome/Check Bit Outputs: These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.
31	OE SC	Output Enable: Syndrome/Check Bits. When LOW, the 3-state output lines SC ₀₋₆ are enabled. When HIGH, the SC outputs are in the high impedance state.
32	<u>ERROR</u>	Error Detected Output: When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, <u>ERROR</u> is forced HIGH. (In a 64-bit configuration, <u>ERROR</u> must be externally implemented.)
33	<u>MULT</u> <u>ERROR</u>	Multiple Errors Detected Output: When the EDC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate mode, <u>MULT ERROR</u> is forced HIGH (in a 64-bit configuration, <u>MULT ERROR</u> must be externally implemented.)
40, 34 – 35 37 – 39, 41	CB ₀₋₆	Seven Check Bit Input Lines: The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.
36	V _{CC}	+5V Power Supply.
42	<u>GENERATE</u>	Generate Check Bits Input: When this input is LOW the EDC is in the Check Bit Generate Mode. When HIGH the EDC is in the Detect Mode or Correct Mode. In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct Modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit input Latch. In Correct Mode, single-bit errors are also automatically corrected - corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.
43 – 45	Code ID ₀₋₂	Code Identification Inputs: These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32 and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID ₂ , ID ₁ , ID ₀) is also used to instruct the EDC that the signals, CODE ID ₀₋₂ , DIAG MODE ₀₋₁ , CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.
46, 47	DIAG MODE ₀₋₁	Diagnostic Mode Select: These two lines control the initialization and diagnostic operation of the EDC.
48	PASS THRU	Pass Thru Input: This line when HIGH forces the contents of the Check Bit Latch onto the Syndrome/Check Bit outputs (SC ₀₋₆) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

ARCHITECTURAL SUMMARY

The EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics.

As shown in Figure 1, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch

- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic

Error Detection and Correction (EDC) Unit

2960

Table 1. Hamming Code and Slice Identification

CODE ID ₂	CODE ID ₁	CODE ID ₀	HAMMING CODE AND SLICE SELECTED
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

Table 2. EDC Operating Modes

OPERATING MODE	DIAGNOSTIC MODE**		GENERATE	
	DM ₁	DM ₀	0	1
Normal	0	0	Generate	Correct*
Diagnostic Generate	0	1	Diagnostic Generate	Correct*
Diagnostic Correct	1	0	Generate	Diagnostic Correct*
Initialize	1	1	Initialize	Initialize
Pass Thru	When PASS THRU is asserted the Operating Mode is defaulted to the Pass Thru Mode.			

*Correct if the CORRECT Input is HIGH. Detect if the CORRECT Input is LOW.
 **In Code ID₂₋₀ 001 (ID₂, ID₁, ID₀) DM₁ and DM₀ are taken from the Diagnostic Latch.

- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

Data Input Latch

16 bits of data are loaded from the bidirectional DATA lines under control of the Latch Enable input, LE IN. Depending on the control mode the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch

Seven check bits are loaded under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

Check Bit Generation Logic

This block generates the appropriate check bit for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

Syndrome Generation Logic

In both Error Detection and Error Correction modes, this logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning

there are no errors) the syndrome bits will be all zeroes. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit-in-error.

Error Detection Logic

This section decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the ERROR and MULT ERROR outputs remain HIGH. If one or more errors are detected, ERROR goes LOW. If two or more errors are detected, both ERROR and MULT ERROR go LOW.

Error Correction Logic

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed the EDC must be switched to Generate Mode.

Data Output Latch

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.

The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

Diagnostic Latch

This is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

Control Logic

The control logic determines the specific operating mode of the device. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are read from the Diagnostic Latch.

FUNCTIONAL OPERATION

The EDC contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code (Table 1). Operating on data read from memory, the EDC will correct any single-bit error and will detect all double and some triple-bit errors. The EDC can be configured to operate on 16-bit data words (with 6 check bits), 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In fact, the EDC can be configured to work on data words from 8 to 64 bits. In all configurations, the device makes the error syndrome bits available on separate outputs for error data logging.

Code and Byte Specification

The EDC may be configured in several different ways and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with input lines CODE ID₀₋₂, as shown in Table 1; the three modified Hamming codes are defined below:

- 16/22 16 data bits
 6 check bits
 22 bits in total.
- 32/39 32 data bits
 7 check bits
 39 bits in total.
- 64/72 64 data bits
 8 check bits
 72 bits in total.

CODE ID input 001 (ID₂, ID₁, ID₀) is a special code, described later, used to operate the device in Internal Control Mode.

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Table 3. Diagnostic Mode Control

DIAG MODE ₁	DIAG MODE ₀	DIAGNOSTIC MODE SELECTED
0	0	Non-diagnostic mode: The EDC functions normally in all modes.
0	1	Diagnostic Generate: The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
1	0	Diagnostic Detect/Correct: In the Detect or Correct Mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	Initialize: The outputs of the Data Input Latch are forced to zeroes (and latched upon removal of the Initialize Mode) and the check bits generated correspond to the all-zero data.

Table 4. 16-Bit Modified Hamming Code

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X				X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X		X		X		X		X		X	X
C2	Odd (XNOR)	X	X				X	X	X			X		X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

Control Mode Selection

The device control lines are GENERATE, CORRECT, PASS THRU, DIAG MODE₀₋₁ and CODE ID₀₋₂. Table 2 indicates the operating modes selected by various combinations of the control line inputs.

Diagnostics

Table 3 shows specifically how DIAG MODE₀₋₁ select between normal operation, initialization and one of two diagnostic modes. The Diagnostic Modes allow the user to operate the EDC under software control in order to verify proper functioning of the device.

Check and Syndrome Bit Labelling

The check bits generated in the EDC are designed as follows:

- 16-bit configuration - CX, C0, C1, C2, C4, C8;
- 32-bit configuration - CX, C0, C1, C2, C4, C8, C16;

- 64-bit configuration - CX, C0, C1, C2, C4, C8, C16, C32.

Syndrome bits are similarly labeled SX through S32. There are only 6 syndrome bits in the 16-bit configuration, 7 for 32 bits and 8 syndrome bits in the 64-bit configuration.

The error correction code can be selected independent of the processor with the exception of diagnostic software.

Diagnostic software run by a processor to checkout the EDC system must know specifically which code is being used. This is only a problem when the EDC replaces an existing MSI implementation on an existing computer. In this case, the computer's software must first determine which of two codes (the old one used by the MSI implementation or the new one used by the EDC) is used by the computer's memory system.

This is easily determined by writing a test data word into memory and then examining whether the generated check bits are typical of the

old or the new code. From then on the software runs only the diagnostic appropriate for the code used on that particular computer's memory system.

Initialize Mode

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. ERROR and MULT ERROR are forced HIGH in the Initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDC may be placed in initialize mode and its outputs written in to all memory locations by the processor.

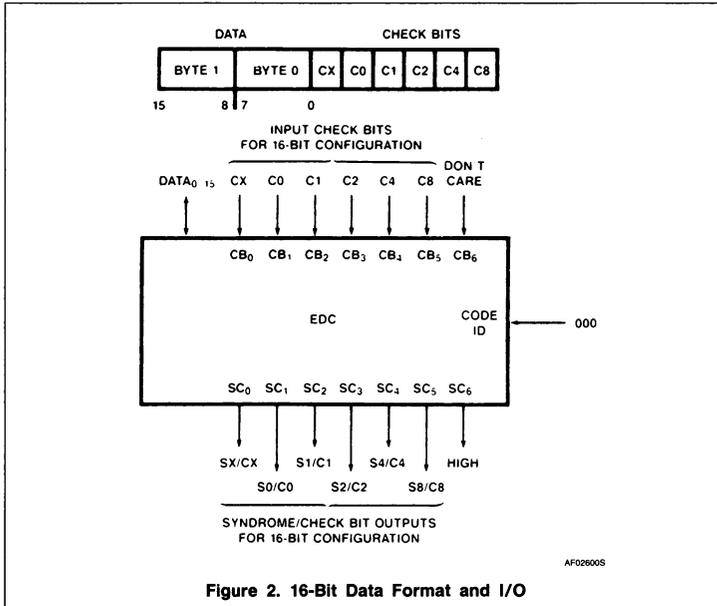
Code Selections

The Signetics 2960 EDC uses a modified Hamming Code which provides the following functions:

- Cascading of EDC Units
- Detection of all double-bit errors
- Detection of gross error conditions (all "0s" or all "1s").

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16-Bit Data Word Configuration

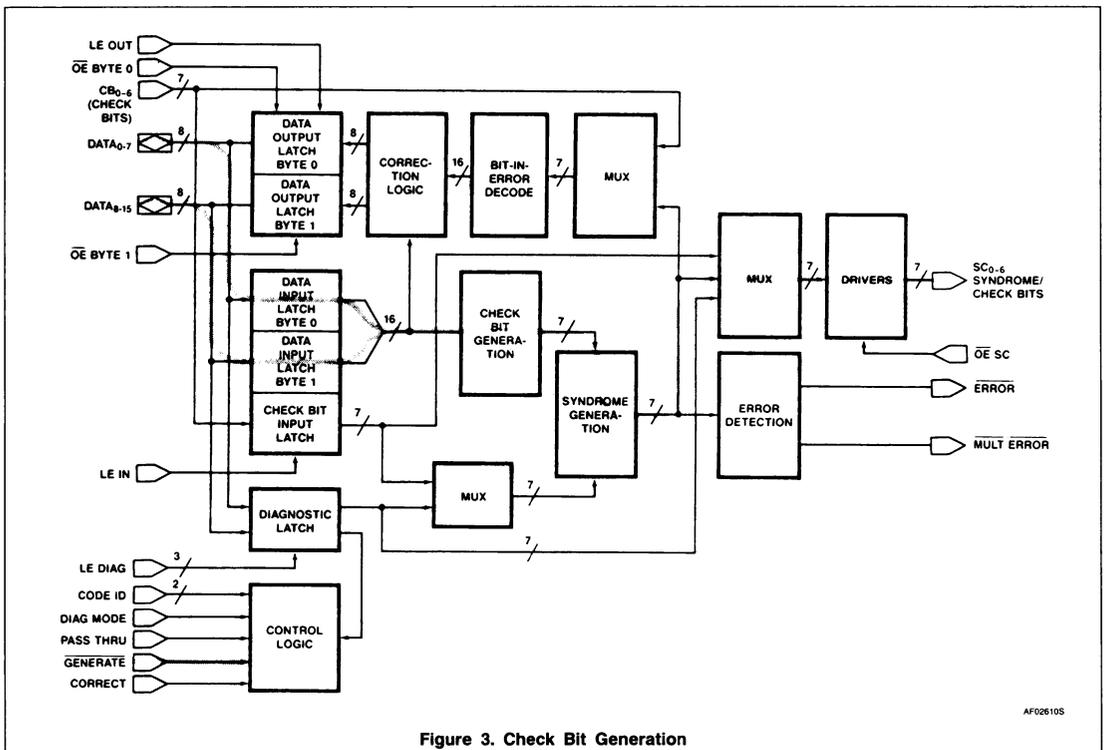
The 16-bit format consists of 16 data bits, six check bits and, as previously indicated, is designated as the 16/22 code. The data format and I/O configuration for a 16-bit word is shown in Figure 2.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC₀₋₅ (SC₆ is a logical one, or high).

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table 4.

Each check bit is generated as either an XOR or XNOR of eight of the 16 data bits as indicated in the table. The XOR function results in an even parity check bit; the XNOR is an odd parity check bit. Data flow for the Generate Mode is shown in Figure 3.



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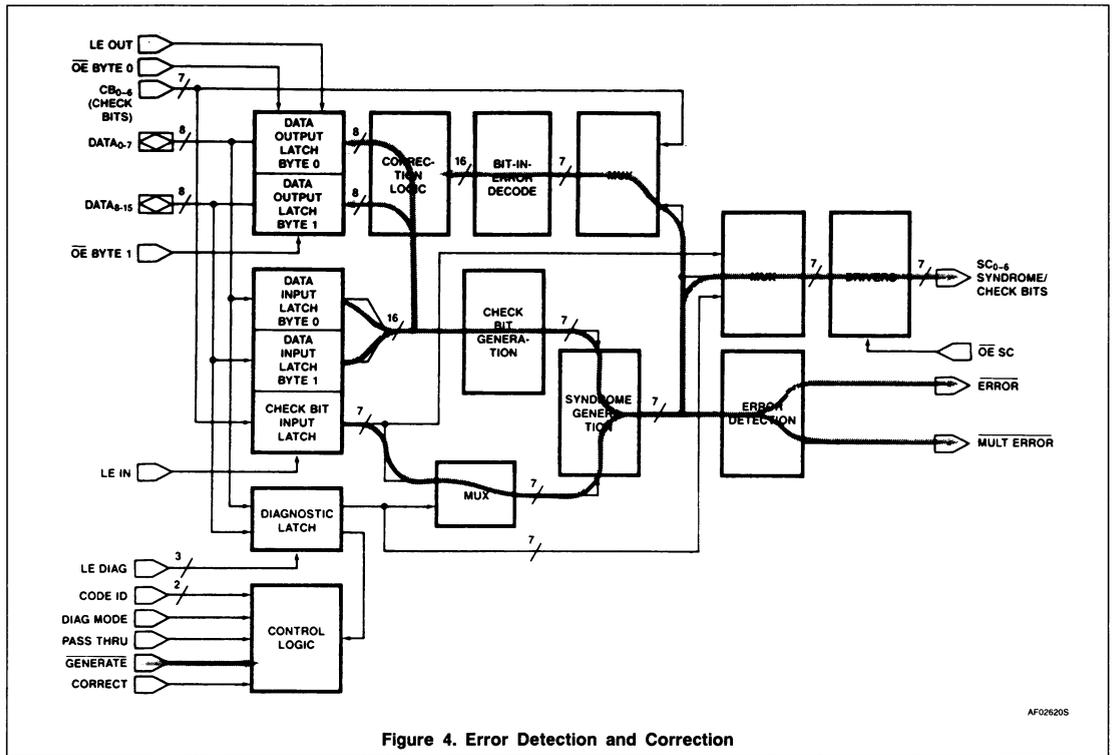


Figure 4. Error Detection and Correction

Table 5. Syndrome Decode to Bit-In-Error

SYNDROME BITS		S8	S4	S2	S1	S0	S1	S2	S4	S8
0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	1	0	1
0	1	0	1	1	0	0	1	1	0	1
0	1	0	0	0	0	1	1	1	1	1
1	0	0	*	C8	C4	T	C2	T	T	M
1	0	1	C1	T	T	15	T	13	7	T
1	1	0	C0	T	T	M	T	12	6	T
1	1	1	T	10	4	T	0	T	T	M
1	0	0	CX	T	T	14	T	11	5	T
1	0	1	T	9	3	T	M	T	T	M
1	1	0	T	8	2	T	1	T	T	M
1	1	1	M	T	T	M	T	M	M	T

* — no errors detected
 Number — the location of the single bit-in-error
 T — two errors detected
 M — three or more errors detected

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, ERROR goes LOW. If two or more errors are detected, MULT ERROR goes LOW. Both error indicators are HIGH if there are no errors.

Also available on device outputs SC₀₋₅ are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table 5 provides decoding data for the syndrome bits generated by the 16-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8 were 101001 this would be decoded to indicate that there is a single-bit error at data bit 9). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

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Table 6. Diagnostic Latch Loading

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE ID 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch — see Figure 4. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs SC₀₋₅. ERROR and MULT ERROR are forced HIGH in this mode.

Diagnostic Latch

The diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table 6 shows the loading definitions for the DATA lines.

Diagnostic Generate/Detect/Correct

These are special diagnostic modes selected by DIAG MODE₀₋₁ where either normal

check bit inputs or outputs are substituted for by check bits loaded into the Diagnostic Latch — See Table 2 for details. Figures 5 and 6 illustrate the flow of data during the two diagnostic modes.

Internal Control Mode

This mode is selected by CODE ID₀₋₂ input 001 (ID₂, ID₁, ID₀).

When in Internal Control Mode, the EDC takes the CODE ID₀₋₂, DIAG MODE₀₋₁, CORRECT, and PASS THRU control signals from the internal Diagnostic Latch rather than from the external input lines.

Table 6 gives the format for loading the Diagnostic Latch.

32-Bit Data Word Configuration

The 32-bit format consists of 32 data bits, seven check bits and, as previously indicated, is designated as the 32/39 code. The data format and I/O configuration for a 32-bit word is shown in Figure 7.

The upper EDC (Slice 0/1) handles the least significant bytes 0 and 1 — the external DATA lines 0 to 15 are connected to the same numbered inputs of the upper device. The lower EDC (Slice 2/3) handles the most significant bytes 2 and 3 — the external DATA lines for bits 16 to 31 are connected to inputs DATA₀ through DATA₁₅ respectively.

The valid syndrome and check bit outputs are those of Slice 2/3 as shown in the diagram. In Correct Mode these must be read into Slice 0/1 via the CB inputs and are selected by the MUX as inputs to the bit-in-error decoded (see block diagram), thus requiring external buffering and output enabling of the check bit lines as shown. The OE SC signal can be used to control enabling of check bit inputs — when syndrome outputs are enabled, the external check bit inputs will be disabled.

The valid ERROR and MULT ERROR outputs are those of the Slice 2/3. The ERROR and MULT ERROR outputs of Slice 0/1 are unspecified. All of the latch enables and control signals must be input to both of the devices.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC₀₋₆ of Slice 2/3.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table 7. Check bits are generated as either

an XOR or XNOR or 16 of the 32 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Code

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, ERROR goes LOW. If two or more errors are detected MULT ERROR goes LOW. Both error indicators are HIGH if there are no errors. The valid ERROR and MULT ERROR signals are those of Slice 2/3 — those of Slice 0/1 are undefined.

Also available on Slice 2/3 outputs SC_{0/6} are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table 8 gives the chart for decoding the syndrome bits generated for the 32-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8/S16 were 0010011 this would be decoded to indicate that there is a single-bit error at data bit 25). If no error is detected the syndrome bits will be all zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction — if desired this would be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

For data correction, both Slices 0/1 and 2/3 require access to the syndrome bits on Slice 2/3's outputs SC₀₋₆. Slice 2/3 has access to these syndrome bits through internal data paths, but for Slice 0/1 they must be read through the inputs CB₀₋₆. The device connections for this are shown in Figure 7. When in Correct Mode the SC outputs must be enabled so that they are available for reading in through the CB inputs.

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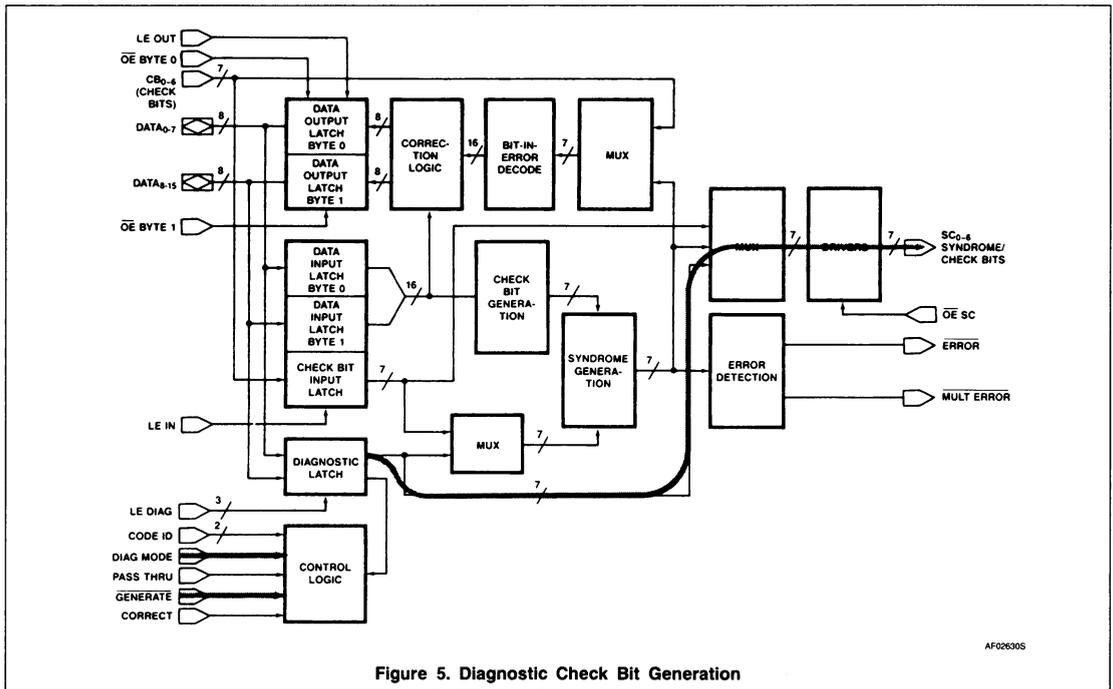


Figure 5. Diagnostic Check Bit Generation

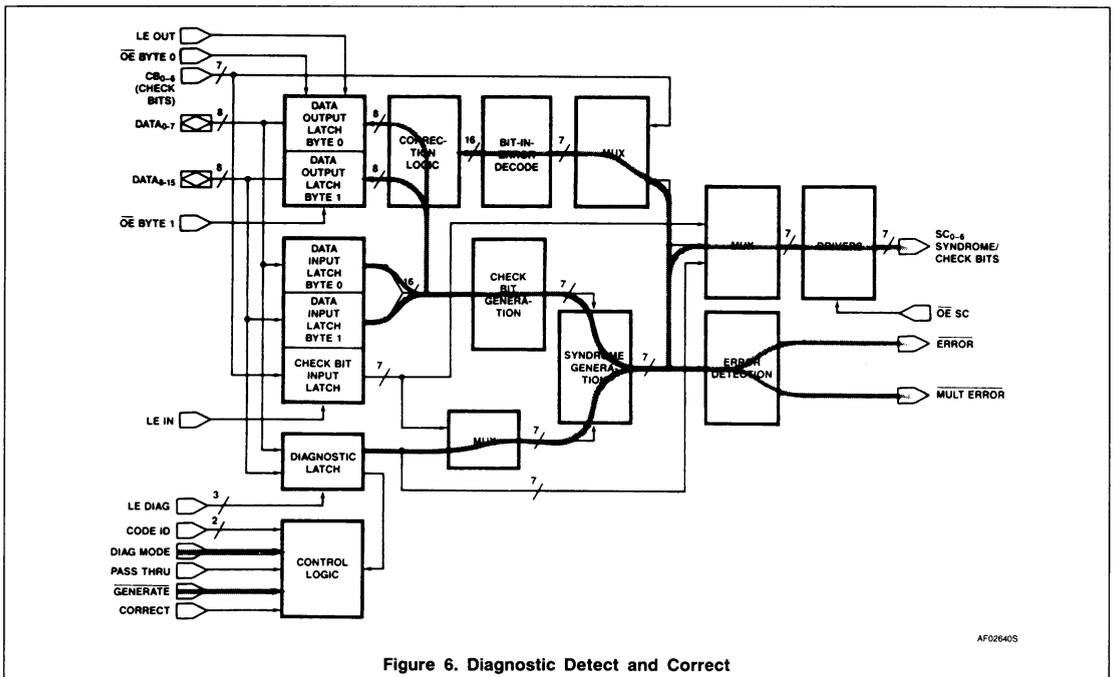


Figure 6. Diagnostic Detect and Correct

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Table 7. 32-Bit Modified Hamming Code

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CS	Even (XOR)	X				X		X	X	X		X	X			X	
C0	Even (XOR)	X	X	X		X		X			X		X			X	
C1	Odd (XNOR)	X			X	X			X			X	X			X	X
C2	Odd (XNOR)	X	X				X	X	X				X		X	X	
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CS	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X			X	X			X	X
C2	Odd (XNOR)	X	X				X	X	X				X		X	X	
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:

The check bit is generated as either an XOR or XNOR of the sixteen data bits noted by an "X" in the table.

Table 8. Syndrome Decode to Bit-In-Error

SYNDROME BITS				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
SX				S4	0	0	0	0	1	1	1	1
				S0	S1	S2						
0	0	0	0	*	C16	C8	T	C4	T	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* — no errors detected
 Number — the location of the single bit-in-error
 T — two errors detected
 M — three or more errors detected

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Table 9. Diagnostic Latch Loading

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 — CODE ID 0
9	Slice 0/1 — CODE ID 1
10	Slice 0/1 — CODE ID 2
11	Slice 0/1 — DIAG MODE 0
12	Slice 0/1 — DIAG MODE 1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASS THRU
15	Don't Care
16–23	Don't Care
24	Slice 2/3 — CODE ID 0
25	Slice 2/3 — CODE ID 1
26	Slice 2/3 — CODE ID 2
27	Slice 2/3 — DIAG MODE 0
28	Slice 2/3 — DIAG MODE 1
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASS THRU
31	Don't Care

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs SC₀₋₆ of Slice 2/3. ERROR and MULT ERROR are forced HIGH in this mode.

Diagnostic Latches/AC Calculations

Table 9 shows how the latches (Slice 1 and Slice 2) are loaded for code 32/39 (32-bit format). Table 10 shows key AC parameters for the 32-bit configuration.

64-Bit Data Word Configuration

The 64-bit format consists of 64 data bits, eight check bits and, as previously indicated, is designated as the 64/72 code. The data format and I/O configuration for a 64-bit word is shown in Figure 8.

The configuration to process the 64-bit format is similar to that shown in Figure 2. In this configuration a portion of the syndrome generation and error detection is implemented externally of the EDCs in MSI. For error correction the syndrome bits generated must be read back into all four EDCs through the CB inputs. This necessitates the check bit buffering shown in Figure 8. The OE SC signal can control the check bit enabling — when syndrome bit outputs are enabled the external check bit lines will be disabled so that the syndrome bits may be read onto the CB inputs.

The error detection signals for the 64-bit configuration differ from the 16 and 32-bit configurations. The ERROR signal functions the same: it is LOW if one or more errors are detected, and HIGH if no errors are detected.

The DOUBLE ERROR signal is HIGH if and only if a double-bit error is detected — it is LOW otherwise. All of the MULT ERROR outputs of the four devices are valid. MULT ERROR is LOW for all three ERROR cases and some DOUBLE ERROR combinations — See Table 15. It is HIGH if either zero or one errors are detected.

This is a different meaning for MULT ERROR than in other configurations.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated appear at the outputs of the XOR gates as indicated in Figure 8.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table 11. Check bits are generated as either an XOR or XNOR of 32 of the 64 bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Table 10. Key AC Calculations for the 32-Bit Configuration

32-BIT PROPAGATION DELAY		COMPONENT DELAY FROM 2960 AC SPECIFICATIONS, TABLE C
From	To	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA In	Corrected DATA Out	(DATA to SC) + (CB to SC, CODE ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	ERROR for 32 Bits	(DATA to SC) + (CB to ERROR, CODE ID 011)
DATA	MULT ERROR for 32 Bits	(DATA to SC) + (CB to MULT ERROR, CODE ID 011)

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Table 11. 64-Bit Modified Hamming Code Check Bit Encoding

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X			X		X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X	X				
C1	Odd (XNOR)	X			X	X				X	X			X		X	
C2	Odd (XNOR)	X	X				X	X	X			X	X				
C4	Even (XOR)			X	X	X	X	X							X	X	
C8	Even (XOR)					X	X	X	X	X			X	X	X	X	
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X			X		X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X	X				
C1	Odd (XNOR)	X			X	X				X	X			X		X	
C2	Odd (XNOR)	X	X				X	X	X			X	X				
C4	Even (XOR)			X	X	X	X	X							X	X	
C8	Even (XOR)					X	X	X	X	X			X	X	X	X	
C16	Even (XOR)									X	X	X	X	X	X	X	
C32	Even (XOR)									X	X	X	X	X	X	X	

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X				X	X			X		X	
C2	Odd (XNOR)	X	X				X	X	X			X	X				
C4	Even (XOR)			X	X	X	X	X							X	X	
C8	Even (XOR)					X	X	X	X	X			X	X	X	X	
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X	X			X	X	X	X	

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X				X	X			X		X	
C2	Odd (XNOR)	X	X				X	X	X			X	X				
C4	Even (XOR)			X	X	X	X	X							X	X	
C8	Even (XOR)					X	X	X	X	X			X	X	X	X	
C16	Even (XOR)									X	X	X	X	X	X	X	
C32	Even (XOR)	X	X	X	X	X	X	X	X	X			X	X	X	X	

NOTE:

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

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Table 12. Syndrome Decode to Bit-In-Error

SYNDROME BITS				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1		
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
SX S0 S1 S2				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	0	*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T	
0	0	0	1	C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M	
0	0	1	0	C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31	
0	0	1	1	T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T	
0	1	0	0	C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M	
0	1	0	1	T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T	
0	1	1	0	T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T	
0	1	1	1	16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M	
1	0	0	0	CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30	
1	0	0	1	T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T	
1	0	1	0	T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T	
1	0	1	1	M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M	
1	1	0	0	T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T	
1	1	0	1	17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M	
1	1	1	0	M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M	
1	1	1	1	T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T	

* — no errors detected
 Number — the location of the single bit-in-error
 T — two errors detected
 M — three or more errors detected

Detect Mode

In this mode the device compares the contents of the Data Input Latch against the contents of the Check Bit Input Latch and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, ERROR goes LOW. If exactly two errors are detected, DOUBLE ERROR goes HIGH. If three or more errors are detected, MULT ERROR goes LOW - the MULT ERROR output of any of the four EDCs may be used.

Available as XOR gate outputs are the generated syndrome bits — see Figure 8. The syndrome bits may be decoded to determine if a bit error was detected and for single-bit errors, which of the data or check bits is in error. Table 12 gives the chart for encoding the syndrome bits generated for the 64-bit configuration (as an example, if the syndrome bits SX/S1/S2/S4/S8/S16/S32 were 00100101 this would be decoded to indicate that there is a single-bit error at data bit 41). If no error is detected the syndrome bits will all be zeroes. In Detect Mode the contents of

the Data Input Latch are driven directly to the Inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified, if the single bit error is a check bit there is no automatic correction. Check bit correction can be done by placing the device in generate mode to produce a correct check bit sequence for the data in the Data Input Latch.

To perform the correction step, all four slices require access to the syndrome bits which are generated externally of the devices. This access is provided by reading the syndrome bits in through the CB inputs where they are selected as inputs to the bit-in-error decoded by the multiplexer (see block diagram). The device connections for this operation are

shown in Figure 8. When in Correct Mode the SC outputs must be enabled so that the syndrome bits are available at the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of the Check Bit Input Latch are passed through the external XOR network and appear inverted at the XOR gate outputs labeled CX to C32 — see Figure 8.

Diagnostic Latch

The Diagnostic Latch is used for both diagnostic and internal control of the EDC. Table 13 provides bit definitions and shows the 64-bit loading format.

Diagnostic Generate/Detect/Correct

These are special diagnostic modes selected by DIAG MODE₀₋₁ where either normal check bit inputs or outputs are substituted for by check bits from the Diagnostic Latch — see Table 2 for details.

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Table 13. Diagnostic Latch Loading

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 — CODE ID 0
9	Slice 0/1 — CODE ID 1
10	Slice 0/1 — CODE ID 2
11	Slice 0/1 — DIAG MODE 0
12	Slice 0/1 — DIAG MODE 1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASS THRU
15	Don't Care
16 – 23	Don't Care
24	Slice 2/3 — CODE ID 0
25	Slice 2/3 — CODE ID 1
26	Slice 2/3 — CODE ID 2
27	Slice 2/3 — DIAG MODE 0
28	Slice 2/3 — DIAG MODE 1
29	Slice 2/3 — CORRECT

DATA BIT	INTERNAL FUNCTION
30	Slice 2/3 — PASS THRU
31	Don't Care
32 – 37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 — CODE ID 0
41	Slice 4/5 — CODE ID 1
42	Slice 4/5 — CODE ID 2
43	Slice 4/5 — DIAG MODE 0
44	Slice 4/5 — DIAG MODE 1
45	Slice 4/5 — CORRECT
46	Slice 4/5 — PASS THRU
47	Don't Care
48 – 54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 — CODE ID 0
57	Slice 6/7 — CODE ID 1
58	Slice 6/7 — CODE ID 2
59	Slice 6/7 — DIAG MODE 0
60	Slice 6/7 — DIAG MODE 1
61	Slice 6/7 — CORRECT
62	Slice 6/7 — PASS THRU
63	Don't Care

Internal Control Mode

This mode is selected by CODE ID₀₋₂, input 001 (ID₂, ID₂, ID₀).

When in Internal Control Mode the EDC takes the CODE ID₀₋₂, DIAG MODE₀₋₁, CORRECT and PASS THRU signals from the internal Diagnostic Latch rather than from the external control lines — see Table 13 for latch loading.

AC Calculations

Table 14 shows key AC parameters for the 64-bit configuration.

Functional Equations

The following equations and tables describe in detail how the output values of the Signetics 2960 are determined as a function of input values and internal states of the chip. Before examining the tables, the following symbol definitions should be carefully studied.

Table 14. Key AC Calculations for the 64-Bit Configuration

64-BIT PROPAGATION DELAY		COMPONENT DELAYS FROM 2960 AC SPECIFICATIONS, TABLE C (PLUS MSI)
From	To	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA In	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	MULT ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to MULT ERROR, CODE ID 1xx)
DATA	DOUBLE ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

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Table 15. TOME (Three or More Errors)*

			S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
			**S6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
			S5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
			S4	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
S1	S2	S3																
0	0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0
0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

*S6, S5, ... S0 are internal syndromes except in Modes 010, 100, 101, 110, 111, (CODE ID₂, ID₁, ID₀). In these modes the syndromes are input over the Check-Bit lines S6 - C6, S5 - C5, S1 - C1, S0 - C0.

**The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC Outputs

Tables 16 through 20 show how outputs SC₀₋₆ are generated in each control mode for various CODE IDs (internal control mode not applicable).

DEFINITIONS

D _i	← (DATA _i if LE IN is HIGH or the output of bit i of the Data input Latch if LE IN is LOW)
C _i	← (CB _i if LE IN is HIGH or the output of bit i of the Check Bit Latch if LE IN is LOW)
DL _i	← Output of the bit i of the Diagnostic Latch
S _i	← Internally generated syndromes (same as outputs of SC _i if outputs enabled)
PA	← D0 ⊕ D1 ⊕ D2 ⊕ D4 ⊕ D6 ⊕ D8 ⊕ D10 ⊕ D12
PB	← D0 ⊕ D1 ⊕ D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7
PC	← D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15
PD	← D0 ⊕ D3 ⊕ D4 ⊕ D7 ⊕ D9 ⊕ D10 ⊕ D13 ⊕ D15
PE	← D0 ⊕ D1 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D11 ⊕ D12 ⊕ D13
PF	← D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D14 ⊕ D15
PG ₁	← D0 ⊕ D4 ⊕ D6 ⊕ D7
PG ₂	← D1 ⊕ D2 ⊕ D3 ⊕ D5
PG ₃	← D8 ⊕ D9 ⊕ D11 ⊕ D14
PG ₄	← D10 ⊕ D12 ⊕ D13 ⊕ D15

ERROR SIGNALS

ERROR	← (S6 · (ID ₁ + ID ₂)) · S5 · S4 · S3 · S2 · S1 · S0 + GENERATE + INITIALIZE + PASS THRU
MULT ERROR (16 and 32-Bit Modes)	← ((S6 · ID ₁) ⊕ S5 ⊕ S4 ⊕ S3 ⊕ S2 ⊕ S1 ⊕ S0) (ERROR) + TOME + GENERATE + PASS THRU + INITIALIZE
MULT ERROR (64-Bit Modes)	← TOME + GENERATE + PASS THRU + INITIALIZE

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Table 16. Syndrome/Check Bit Generation in GENERATE Mode

GENERATE MODE (CHECK BITS)	CODE ID ₂₋₀						
	000	010	011	100	101	110	111
SC ₀ *	PG ₂ ⊕ PG ₃	PG ₁ ⊕ PG ₃	PG ₂ ⊕ PG ₄	PG ₂ ⊕ PG ₃	PG ₂ ⊕ PG ₃	PG ₁ ⊕ PG ₄	PG ₁ ⊕ PG ₄
SC ₁ *	PA						
SC ₂ *	\overline{PD}	\overline{PD}	PD	\overline{PD}	PD	PD	PD
SC ₃ *	\overline{PE}	\overline{PE}	PE	\overline{PE}	PE	PE	PE
SC ₄ *	PF						
SC ₅ *	PC						
SC ₆ *	1	PB	PC	PB	PB	PB	PB

Table 17. Syndrome/Check Bit Generation in Detect/Correct Modes

DETECT AND CORRECT MODES (SYNDROMES)	CODE ID ₂₋₀						
	000	010	011*	100	101	110	111
SC ₀ *	PG ₂ ⊕ PG ₃ ⊕ C ₀	PG ₁ ⊕ PG ₃ ⊕ C ₀	PG ₂ ⊕ PG ₄ ⊕ CB ₀	PG ₂ ⊕ PG ₃ ⊕ C ₀	PG ₂ ⊕ PG ₃	PG ₁ ⊕ PG ₄	PG ₁ ⊕ PG ₄
SC ₁ *	PA ⊕ C ₁	PA ⊕ C ₁	PA ⊕ CB ₁	PA ⊕ C ₁	PA	PA	PA
SC ₂ *	\overline{PD} ⊕ C ₂	\overline{PD} ⊕ C ₂	PD ⊕ CB ₂	\overline{PD} ⊕ C ₂	PD	PD	PD
SC ₃ *	\overline{PE} ⊕ C ₃	\overline{PE} ⊕ C ₃	PE ⊕ CB ₃	\overline{PE} ⊕ C ₃	PE	PE	PE
SC ₄ *	PF ⊕ C ₄	PF ⊕ C ₄	PF ⊕ CB ₄	PF ⊕ C ₄	PF	PF	PF
SC ₅ *	PC ⊕ C ₅	PC ⊕ C ₅	PC ⊕ CB ₅	PC ⊕ C ₅	PC	PC	PC
SC ₆ *	1	PB ⊕ C ₆	PC ⊕ CB ₆	PB	PB	PB ⊕ C ₆	PB ⊕ C ₆

*In CODE ID₂₋₀ 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

Table 18. Syndrome/Check Bit Generation in Diagnostic Read Mode

DIAGNOSTIC READ MODE	CODE ID ₂₋₀						
	000	010	011*	100	101	110	111
SC ₀ *	PG ₂ ⊕ PG ₃ ⊕ DL ₀	PG ₁ ⊕ PG ₃ ⊕ DL ₀	PG ₂ ⊕ PG ₄ ⊕ CB ₀	PG ₂ ⊕ PG ₃ ⊕ DL ₀	PG ₂ ⊕ PG ₃	PG ₁ ⊕ PG ₄	PG ₁ ⊕ PG ₄
SC ₁ *	PA ⊕ DL ₁	PA ⊕ DL ₁	PA ⊕ CB ₁	PA ⊕ DL ₁	PA	PA	PA
SC ₂ *	\overline{PD} ⊕ DL ₂	\overline{PD} ⊕ DL ₂	PD ⊕ CB ₂	\overline{PD} ⊕ DL ₂	PD	PD	PD
SC ₃ *	\overline{PE} ⊕ DL ₃	\overline{PE} ⊕ DL ₃	PE ⊕ CB ₃	\overline{PE} ⊕ DL ₃	PE	PE	PE
SC ₄ *	PF ⊕ DL ₄	PF ⊕ DL ₄	PF ⊕ CB ₄	PF ⊕ DL ₄	PF	PF	PF
SC ₅ *	PC ⊕ DL ₅	PC ⊕ DL ₅	PC ⊕ CB ₅	PC ⊕ DL ₅	PC	PC	PC
SC ₆ *	1	PB ⊕ DL ₆	PC ⊕ CB ₆	PB	PB	PB ⊕ DL ₆	PB ⊕ DL ₆

*In CODE ID₂₋₀ 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

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Table 19. Syndrome/Check Bit Generation in Diagnostic Write Mode

DIAGNOSTIC WRITE MODE	CODE ID ₂₋₀						
	000	010	011*	100	101	110	111
SC ₀ ←	DL ₀	DL ₀	CB ₀	DL ₀	1	1	1
SC ₁ ←	DL ₁	DL ₁	CB ₁	DL ₁	1	1	1
SC ₂ ←	DL ₂	DL ₂	CB ₂	DL ₂	1	1	1
SC ₃ ←	DL ₃	DL ₃	CB ₃	DL ₃	1	1	1
SC ₄ ←	DL ₄	DL ₄	CB ₄	DL ₄	1	1	1
SC ₅ ←	DL ₅	DL ₅	CB ₅	DL ₅	1	1	1
SC ₆ ←	1	DL ₆	CB ₆	1	1	DL ₆	DL ₇

*In CODE ID₂₋₀ 011 the Check-Bit Latch is forced transparent; the Data Latch operates normally.

Table 20. Syndrome/Check Bit Generation in PASS THRU Mode

PASS THRU MODE	CODE ID ₂₋₀						
	000	010	011*	100	101	110	111
SC ₀ ←	C0	C0	CB ₀	C0	1	1	1
SC ₁ ←	C1	C1	CB ₁	C1	1	1	1
SC ₂ ←	C2	C2	CB ₂	C2	1	1	1
SC ₃ ←	C3	C3	CB ₃	C3	1	1	1
SC ₄ ←	C4	C4	CB ₄	C4	1	1	1
SC ₅ ←	C5	C5	CB ₅	C5	1	1	1
SC ₆ ←	1	C6	CB ₆	1	1	C6	C6

*In CODE ID₂₋₀ 011 the Check-Bit Latch is forced transparent; the Data Latch operates normally.

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Table 21. CODE ID₂₋₀ = 000*

		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
		S3	0	1	0	1	0	1	0	1
S2	S1									
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

*Unlisted S combinations are no correction.

Table 22. CODE ID₂₋₀ = 010*

		CB ₆	0	0	0	0	1	1	1	1
		CB ₅	1	1	1	1	0	0	0	0
		CB ₄	0	0	1	1	0	0	1	1
		CB ₃	0	1	0	1	0	1	0	1
CB ₂	CB ₁									
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

*Unlisted CB combinations are no correction.

Table 23. CODE ID₂₋₀ = 011*

		S6	0	0	0	0	1	1	1	1
		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
		S3	0	1	0	1	0	1	0	1
S2	S1									
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

*Unlisted S combinations are no correction.

Table 24. CODE ID₂₋₀ = 100*

		CB ₀	0	0	0	0	1	1	1	1
		CB ₆	0	0	0	0	1	1	1	1
		CB ₅	1	1	1	1	0	0	0	0
		CB ₄	0	0	1	1	0	0	1	1
		CB ₃	0	1	0	1	0	1	0	1
CB ₂	CB ₁									
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

*Unlisted CB combinations are no correction.

Data Correction

Tables 21 through 27 show which data output bits are corrected (inverted) depending upon the syndromes and the CODE ID position. Note that the syndromes that determine data correction are in some cases syndromes input externally via the CB inputs and in some cases syndromes generated internally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

The tables show the number of data bit inverted (corrected) if any for the CODE ID and syndrome combination.

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Table 25. CODE ID₂₋₀ = 101*

		CB₀	0	0	0	0	1	1	1	1
		CB₆	0	0	0	0	1	1	1	1
		CB₅	0	0	0	0	1	1	1	1
		CB₄	0	0	1	1	0	0	1	1
		CB₃	0	1	0	1	0	1	0	1
CB₂	CB₁									
0	0	—	—	—	5	—	11	14	—	—
0	1	—	1	2	6	8	12	—	—	—
1	0	—	—	3	7	9	13	15	—	—
1	1	—	0	4	—	10	—	—	—	—

*Unlisted CB combinations are no correction.

Table 26. CODE ID₂₋₀ = 110*

		CB₀	0	0	0	0	1	1	1	1
		CB₆	1	1	1	1	0	0	0	0
		CB₅	0	0	0	0	1	1	1	1
		CB₄	0	0	1	1	0	0	1	1
		CB₃	0	1	0	1	0	1	0	1
CB₂	CB₁									
0	0	—	—	—	5	—	11	14	—	—
0	1	—	1	2	6	8	12	—	—	—
1	0	—	—	3	7	9	13	15	—	—
1	1	—	0	4	—	10	—	—	—	—

*Unlisted CB combinations are no correction.

Table 27. CODE ID₂₋₀ = 111*

		CB₀	0	0	0	0	1	1	1	1
		CB₆	1	1	1	1	0	0	0	0
		CB₅	1	1	1	1	0	0	0	0
		CB₄	0	0	1	1	0	0	1	1
		CB₃	0	1	0	1	0	1	0	1
CB₂	CB₁									
0	0	—	11	14	—	—	—	—	5	—
0	1	8	12	—	—	—	1	2	6	—
1	0	9	13	15	—	—	—	3	7	—
1	1	10	—	—	—	—	0	4	—	—

*Unlisted CB combinations are no correction.

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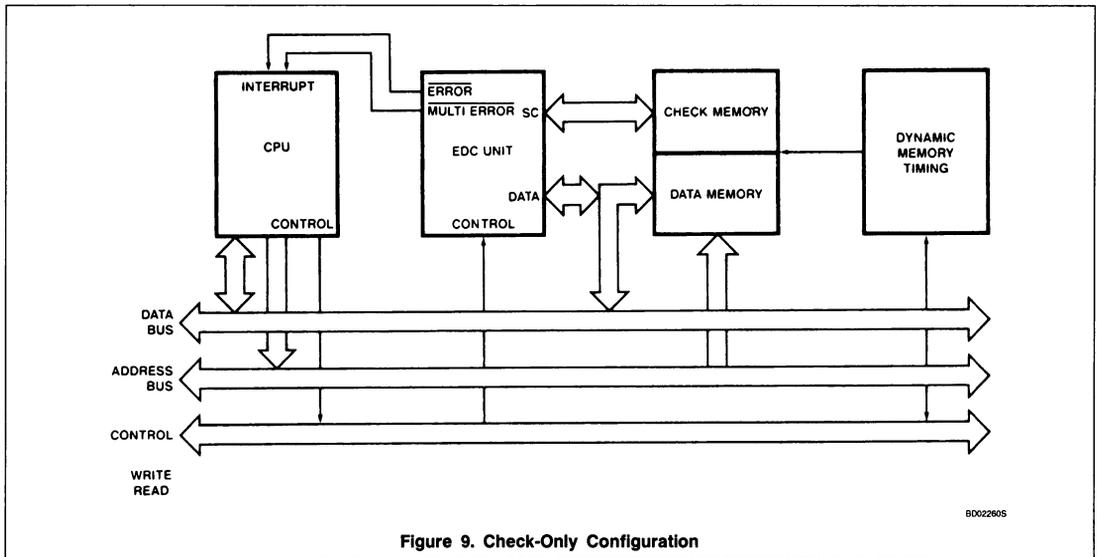


Figure 9. Check-Only Configuration

SYSTEM DESIGN CONSIDERATIONS

High-Performance Parallel Operation

For maximum memory system performance the EDC should be used in the Check-Only configuration shown in Figure 9. With this configuration the memory system operates as fast with EDC as it would without.

On reads from memory, data is read out from the RAMs directly to the data bus (same as in a non-EDC system). At the same time, the data is read into the EDC to check for errors.

If an error exists the EDC's error flags are used to interrupt the CPU and/or to stretch the memory cycle. If no error is detected, no slowdown is required.

If an error is detected, the EDC generates corrected data for the processor. At the designer's option the correct data may be written back into memory; error logging and diagnostic routines may also be run under processor control.

The Check-Only configuration allows data reads to proceed as fast with EDC as without. Only if an error is detected is there any slowdown. But even if the memory system had an error every hour this would mean only one error every 3-4 billion memory cycles. So even with a very high error rate, EDC in a Check-Only configuration has essentially zero impact on memory system speed.

On writes to memory, check bits must be generated before the full memory word can be written into memory. The data word is frequently buffered while the check bits are generated. This makes the check bit generate time transparent to the processor.

EDC in the Data Path

The simplest configuration for EDC is to have the EDC directly in the data path as shown in Figure 10. Correct-Always Configuration). In the configuration data read from memory is always corrected prior to putting the data on the data bus. The advantages are simpler operation and no need for mid-cycle interrupts. The disadvantages is that memory system speed is slowed by the amount of time it takes for error correction on every cycle.

Usually the Correct-Always Configuration will be used with MOS microprocessors which have ample memory timing budgets. Most high-performance processors will use the high-performance parallel configuration shown in Figure 9.

Scrubbing Avoids Double Errors

Single-bit errors are by far the most common in a memory system and are always correctable by the EDC.

Double-bit memory errors are far less frequent than single-bit errors (50 to 1, or 100 to 1) and are always detected by the EDC but not corrected.

In a memory system, soft errors occur only one at a time. A double-bit error in a data

word occurs when a single soft error is left uncorrected and is followed by another error in the data word hours, days, or weeks after the first.

"Scrubbing" memory periodically avoids almost all double-bit errors. In the scrubbing operation, every data word in a memory is periodically checked by the EDC for single-bit errors. If one is found, it is corrected and the data word written back into memory. Errors are not allowed to pile up and so most double-bit errors are avoided.

The scrubbing operation is generally done as a background routine when the memory is not being used by the processor.

If memory is scrubbed frequently, errors are detected and corrected during processor accesses need not be immediately written back into memory. Instead the error will be corrected in memory during scrubbing. This reduces the time delay involved in a processor access of an incorrect memory word.

Correction of Double-Bit Errors

In some cases, double-bit memory errors can be corrected. This is possible when one of the two bit errors is a hard error.

When a double-bit error is detected, the data word should be checked to determine if one of the errors is a hard error. If so, the hard error bit may be corrected by inverting it leaving only a single, correctable error. The time for this operation is negligible since it will occur infrequently.

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Error Detection and Correction (EDC) Unit

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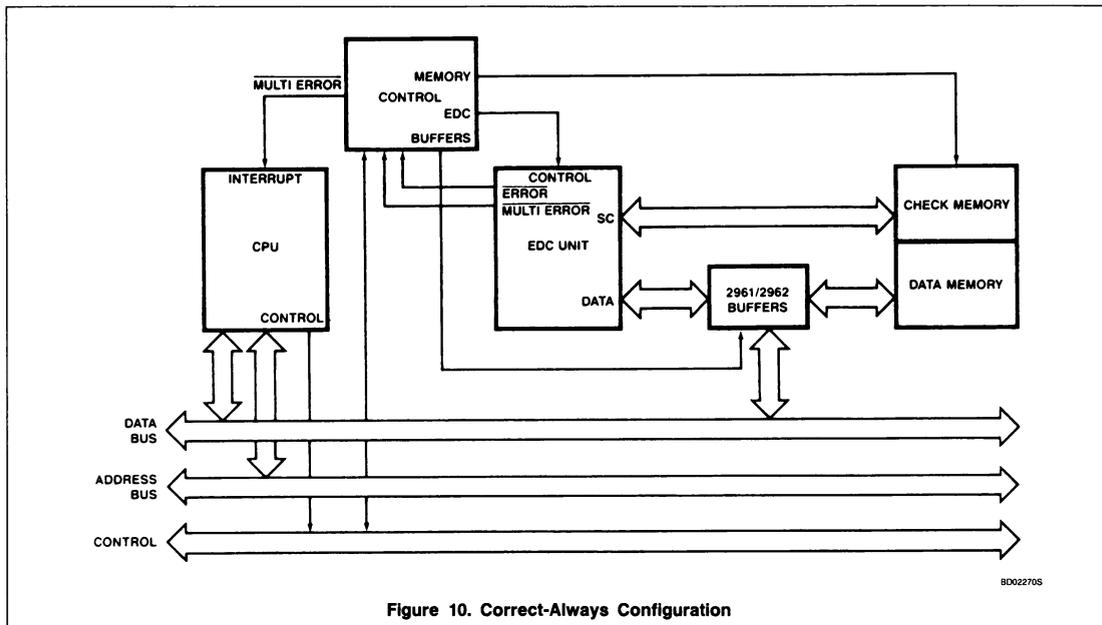


Figure 10. Correct-Always Configuration

The procedure after detection of a double error is as follows:

- Invert the data bits read from memory.
- Write the inverted data back into the same memory word.
- Re-read the memory location and XOR the newly read out value with the old. If there is no hard error then the XOR

result will be 1's. If there is a hard error, it will have the same bit value regardless of what was written in. So it will show as a 0 after the XOR operation.

- Invert the hard error bit (this will "correct" it) leaving only one error in the data.

- The EDC can then correct the single-bit error.
- Rewrite the correct data word into memory. This does not change the hard error but does eliminate the soft error. So the next memory access will find only a single-bit, correctable error.

An example helps to illustrate the procedure:

Example of Double Bit Error Correction When One is a Hard Error

	16 DATA BITS	6 CHECK BITS
1) Data read from memory (D ₂)	1111111100000011	011010
2) EDC detects a multiple error syndromes		011000
3) Syndrome decode indicates a double bit error		
4) Invert the bits read from memory (D ₁)	0000000011111100	100101
5) Write D ₁ back to the same memory location		
6) Read back the memory location (D ₂)	0000000011111101	100101
7) XOR D ₁ and D ₂	1111111100000010	111111
8) So the last data bit is the hard error. Use this to modify D ₁	1111111100000010	011010
9) Pass the modified D ₁ through the EDC. The EDC detects a single bit correctable error and outputs corrected data	1111111100000000	011010
10) Write the corrected data back to memory to fix the soft error		

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Error Logging and Preventative Maintenance

The effectiveness of preventative maintenance can be increased by logging information on errors detected by the EDC. This is called error logging.

The EDC provides syndromes when errors are detected. The syndromes indicate which bit is in error. In most memory systems, each individual RAM supplies only one bit of the memory word, so the syndrome and data word address specify which RAM was in error.

Typically a permanent/hard RAM failure is preceded by a period of time where the RAM displays an increasing frequency of intermittent, soft errors. Error logging statistics can be used to detect an increasing intermittent error frequency so that the RAM can be replaced before a permanent failure occurs.

Error logging also records the location of already hard failed RAMs. With EDC, a hard failure will not halt system operation. EDC always can correct single-bit errors even if it is a hard error. EDC can also correct double-bit errors where one is hard and one soft. The ability to continue operation despite hard errors can greatly reduce the need for emergency field maintenance. The hard-failed RAMs can be instead replaced at low cost during a regularly scheduled preventative maintenance session.

Reducing Check Bit Overhead

Memory word widths need not be the same as the data word width of the processor. There is a substantial reduction in check bit overhead if wider memory words are used. (See Table 28.)

This reduction in check-bit overhead lowers cost and increases the amount of data that can be packed on to each board.

The tradeoff is that when writing data pieces into memory that are narrower than the mem-

Table 28. Reducing Check Bit Overhead

MEMORY WORD		CHECK BIT OVERHEAD
# Data Bits	# Check Bits	
8	5	38%
16	6	27%
32	7	14%
64	8	11%

ory word width, more steps are required. These steps are exactly the same as those described in Byte Write in the Applications section. No penalty exists for reads from memory.

EDC per Board vs EDC per System

The choice of an EDC per system or per board depends on the economics and the architecture of the system.

Certainly the cheaper approach is to have only one EDC per system and this is a viable solution if only one memory location is accessed at a time.

This solution does require that the system have both data and check bit lines - see Figure 11. This makes retrofitting a system difficult and creates complications if static or ROM memory, which do not require check bits, are mixed in with dynamic RAM.

If the system has an advanced architecture, it is quite likely that it is necessary to simultaneously access memory locations on different memory boards — see Figure 12. Architectural features that require this are interleaved memory, cache memory, and DMA that is done simultaneously with processor memory accesses. EDC per board is a simpler system from a design standpoint.

The EDC is designed to work efficiently in either the per system or per board configurations.

Test Information

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5 – 8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. Signetics recommends using V_{IL} 0.4V and V_{IH} -2.4V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, Signetics offers documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Error Detection and Correction (EDC) Unit

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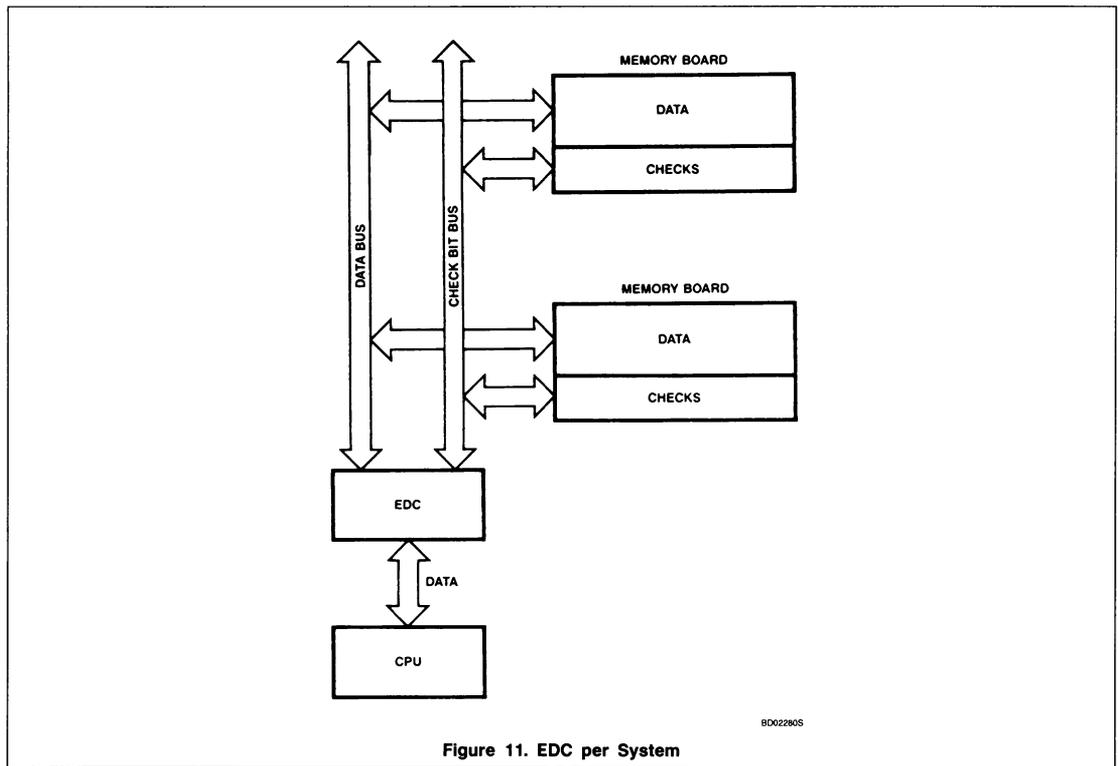


Figure 11. EDC per System

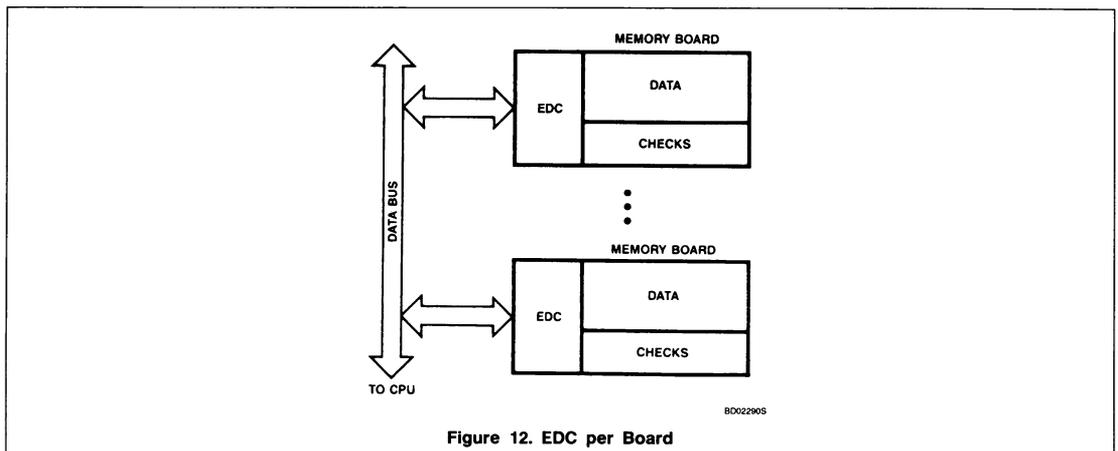


Figure 12. EDC per Board

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ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

PARAMETER	RATING	UNIT
Storage Temperature	-65 to +150	°C
Temperature (Case) Under Bias	-55 to +125	°C
Supply Voltage to Ground Potential	-0.5 to +7.0	V
DC Voltage Applied to Outputs for High Output State	-0.5 to V _{CC} MAX	V
DC Input Voltage	-0.5 to +5.5	V
DC Output Current, Into Outputs	30	mA
DC Input Current	-30 to +5.0	mA

OPERATING RANGE

PART NO.	TEMPERATURE	V _{CC}
N2960N N2960I	T _A = 0 to +70°C	5V (± 5%)

DC CHARACTERISTICS V_{CC} MIN = 4.75V, V_{CC} MAX = 5.25V

PARAMETER		TEST CONDITIONS ¹		2960			UNIT
				Min	Typ ²	Max	
V _{OH}	Output HIGH voltage	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -0.8mA	2.7			V
V _{OL}	Output LOW voltage	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 8mA			0.5	V
V _{IH}	Input HIGH voltage	Guaranteed input logical HIGH voltage for all inputs ⁶		2.0			V
V _{IL}	Input LOW voltage	Guaranteed input logical LOW voltage for all inputs ⁶				0.8	V
V _I	Input clamp voltage	V _{CC} = Min, I _{IN} = -18mA				-1.5	V
I _{IL}	Input LOW current	V _{CC} = Max V _{IN} = 0.5V	DATA ₀₋₁₅			-410	μA
			All other inputs			-360	
I _{IH}	Input HIGH current	V _{CC} = Max V _{IN} = 2.7V	DATA ₀₋₁₅			70	μA
			All other inputs			50	
I _I	Input HIGH current	V _{CC} = Max, V _{IN} = 5.5V				1.0	mA
I _{OZH} ⁴ I _{OZL} ⁴	Off state (high impedance) output current	V _{CC} = Max	DATA ₀₋₁₅	V _O = 2.4V		70	μA
				V _O = 0.5V		-410	
			SC ₀₋₆	V _O = 2.4V		50	
				V _O = 0.5V		-50	
I _{OS}	Output short circuit current ³	V _{CC} = V _{CC} Max + 0.5V, V _O = 0.5V		-25		-85	mA
I _{CC}	Power supply current ⁵	V _{CC} = Max	T _A = 25°C		315	340	mA
			T _A = 0 to +70°C			381	
			T _A = +70°C			335	

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
- Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
- These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
- Worst case I_{CC} is at minimum temperature.
- These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

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GUARANTEED PERFORMANCE OVER COMMERCIAL TEMPERATURE RANGE OF 0 TO +70°C

The tables that follow specify the guaranteed performance of the 2960 over the commercial

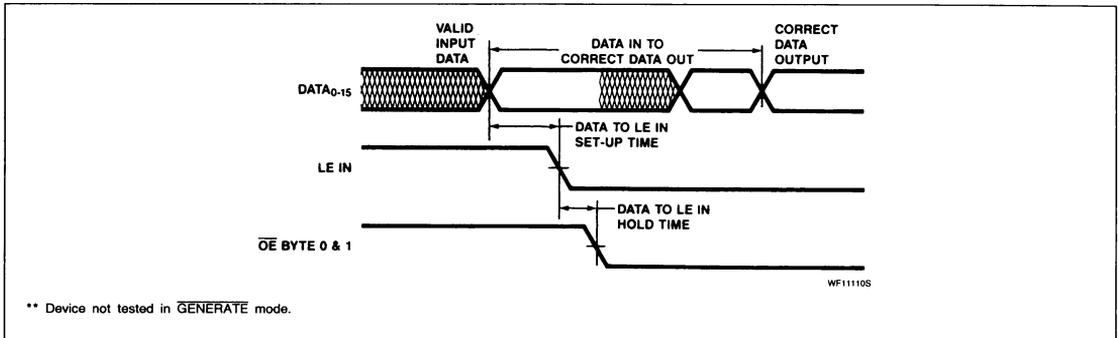
operating range of 0 to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: N2960N and N2960I.

COMBINATIONAL PROPAGATION DELAYS — $C_L = 50pF$

FROM INPUT	TO OUTPUT	SC ₀₋₆	DATA ₀₋₁₅	ERROR	MULT ERROR
DATA ₀₋₁₅		32	65*	32	50
CB ₀₋₆ (CODE ID ₂₋₀ 000, 011)		28	56	29	47
CB ₀₋₆ (CODE ID ₂₋₀ 010, 100, 101, 110, 111)		28	45	29	34
$\overline{\text{GENERATE}}$		35	63	36	55
CORRECT (Not internal control mode)		—	45	—	—
DIAG MODE (Not internal control mode)		50	78	59	75
PASS THRU (Not internal control mode)		36**	44	29	46
CODE ID ₂₋₀		61	90	60	80
LE IN (From latched to transparent)		39	72*	39	59
LE OUT (From latched to transparent)		—	31	—	—
LE DIAG (From latched to transparent; not internal control mode)		45	78	45	65
Internal control mode: LE DIAG (from latched to transparent)		67	96	66	86
Internal control mode: DATA ₀₋₁₅ (via diagnostic latch)		67	96	66	86

*Data In (or LE In) to Correct Data Out measurement requires timing as shown below.



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SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
DATA ₀₋₁₅	LE IN	6	7
CB ₀₋₆	LE IN	5	6
DATA ₀₋₁₅	LE OUT	44	5
CB ₀₋₆ (CODE ID 000, 011)	LE OUT	35	0
CB ₀₋₆ (CODE ID 010, 100, 101, 110, 111)	LE OUT	27	0
GENERATE	LE OUT	42	0
CORRECT	LE OUT	26	1
DIAG MODE	LE OUT	69	0
PASS THRU	LE OUT	26	0
CODE ID ₂₋₀	LE OUT	81	0
LE IN	LE OUT	51	5
DATA ₀₋₁₅	LE DIAG	6	8

MINIMUM PULSE WIDTHS

LE IN, LE OUT, LE DIAG	15
------------------------	----

OUTPUT ENABLE/DISABLE TIMES Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
\overline{OE} BYTE 0, \overline{OE} BYTE 1	DATA ₀₋₁₅	30	30
\overline{OE} SC	SC ₀₋₆	30	30

TEST LOADING

Three-State Outputs:

TC035405

Normal Outputs:

TC035505

TEST OUTPUT LOADS

PIN #	PIN LABEL	TEST CIRCUIT	R ₁	R ₂
—	D ₀ - D ₁₅	Fig. 11	430Ω	1kΩ
24 - 30	SC ₀ - SC ₆	Fig. 11	430Ω	1kΩ
32	ERROR	Fig. 12	470Ω	3kΩ
33	MULTERROR	Fig. 12	470Ω	3kΩ

PACKAGE DATA
 TYPE: Plastic and Ceramic
 Configuration: DIP
 Width: C = 0.6" P = 0.55"
 Length: 2.4"
 Pin Centers: 2.54 BSC

ORDERING INFORMATION
 Commercial:
 N2960N (Plastic)
 N2960I (Ceramic)

NOTES:

- C_L = 50pF includes scope probe, wiring and stray capacitances without devices in test fixture.
- S₁, S₂, S₃ are closed during function test and all AC tests, except output enable tests.
- S₁ and S₃ are closed while S₂ is open for t_{PZH} test.
S₁ and S₂ are closed while S₃ is open for t_{PZL} test.
- R₂ = 1K for three-state output.
- R₂ is determined by the I_{OH} at V_{OH} = 2.4V for non-three-state output.
- R₁ is determined by I_{OL} (MIL) with V_{CC} = 5.0V minus the current to ground through R₂.
- C_L = 5.0pF for output disable tests.

Error Detection and Correction (EDC) Unit

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APPLICATIONS

Byte Write

Byte operations are increasingly common for 16 and 32-bit processors. These complicate memory operations because check bits are generated for a complete 16 or 32 or 64-bit memory word, not for a single byte.

To write a byte into memory with EDC requires the following steps — See Figures 13 and 14.

- Latch the byte into the bus buffers
- Read the complete word from memory
- Correct the complete data word if necessary
- Insert the byte to be written into the data word
- Generate new check bits for the entire data word
- Store the data word back into memory.

(In fact these steps must be taken for any piece of data being written into memory that is not as wide as a full memory word).

The EDC is designed with the intent of keeping byte operations simple in error detection/correction systems. The EDC has separate output enables for each byte in the Data Output Latch. As shown in Figures 13 and 14, this allows the data word to be read from memory, the new byte to be inserted among the old, and new check bits to be generated using less time and less hardware than if separate byte enables were not available.

Diagnostics

EDC is used to boost the reliability of the overall system. It is necessary to also be able to check the operation of the EDC itself. For this reason the EDC has an internal control mode, a diagnostic latch, and two diagnostic modes.

To check that the EDC is functioning properly, the processor can put the EDC under software control by setting CODE ID₂₋₀ to 001. This puts the EDC into Internal Control Mode. In Internal Control Mode the EDC is controlled by the contents of the Diagnostic

DATA BITS	CHECK BITS REQUIRED	
	Single Error Corrections Only	Single Error Correct & Double Error Detect
8	4	5
16	5	6
32	6	7
64	7	8

Latch, which is loaded from the DATA inputs under processor control.

The EDC is set into CORRECT Mode. The processor loads in a known set of check bits into the Diagnostic Latch, a known set of data bits into the Data in Latch, and forces data errors. The output of the EDC (syndromes, error flags, corrected data) is then compared against the expected responses. By exercising the EDC with a string of data/check combinations and comparing the output against the expected responses, the EDC can be fully checked out.

Eight-Data Word

Eight-bit MOS microprocessors can use EDC too. Only five check bits are required. The EDC configuration for eight bits is shown in Figure 15. It operates as does the normal 16-bit configuration with the upper byte fixed at 0.

Other Word Widths

EDC on data words other than 8-, 16-, 32-, and 64-bits can be accomplished with the 2960. In most cases the extra data bits can be forced to a constant and EDC will proceed as normal. For example a 24-bit data word is shown in Figure 16.

Single Error Correction Only

The EDC normally corrects all single-bit errors and detects all double-bit and some triple-bit errors. To save one check bit per word the ability to detect double-bit errors can be sacrificed — single errors are still detected and corrected.

Figure 17 shows single error correction only configurations for 8-, 16-, 32-, and 64-bit data words respectively.

Check Bit Correction

The EDC detects single-bit errors whether the error is a data bit or a check bit. Data bit errors are automatically corrected by the EDC. To generate corrected check bits once a single check bit error is detected, the EDC need only be switched to GENERATE mode (data in the DATA INPUT LATCH is valid).

The syndromes generated by the EDC may be decoded to determine whether the single-bit error is a check bit.

In many memory systems, a check bit error will be ignored on the memory read and corrected during a periodic "scrubbing" of memory — see System Design Considerations).

Multiple Errors

The bit-in-error decode logic uses syndrome bits S0 through S32 to correct errors, SX is only used in developing the multiple error signal. This means that some multiple errors will cause a data bit to be inverted.

For example, in the 16-bit mode if data bits 8 and 13 are in error the syndrome 111100 (SX, S0, S1, S2, S4 S8) is produced. This is flagged a double error by the error detection logic, but the decoded bit-in-error only receives syndrome 11100 (S0, S1, S2, S4, S8) which it decodes as a single error in data bit 0 and inverts that bit. If it is desired to inhibit this inversion, the multiple error output may be connected to the correct input as in Figure 18. This will inhibit correction when a multiple error occurs. Extra time delay may be introduced in the data to correct data path when this is done.

Error Detection and Correction (EDC) Unit

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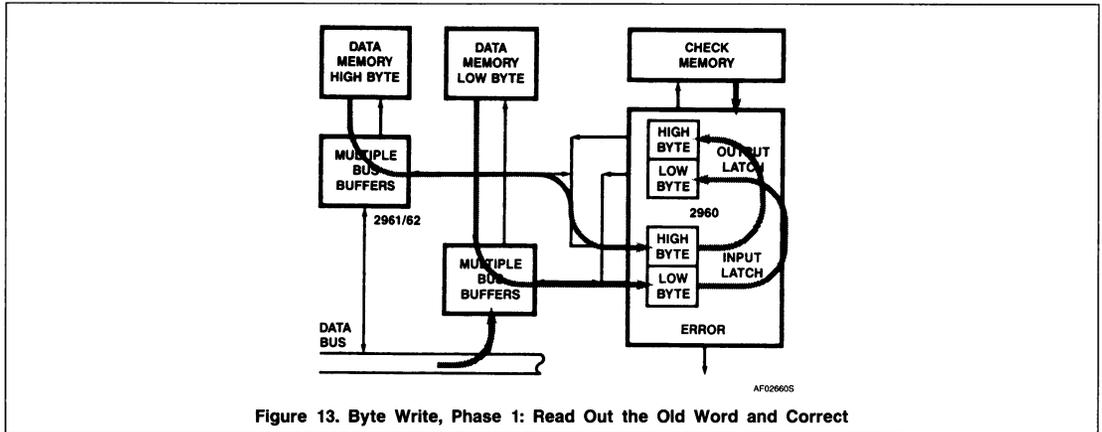


Figure 13. Byte Write, Phase 1: Read Out the Old Word and Correct

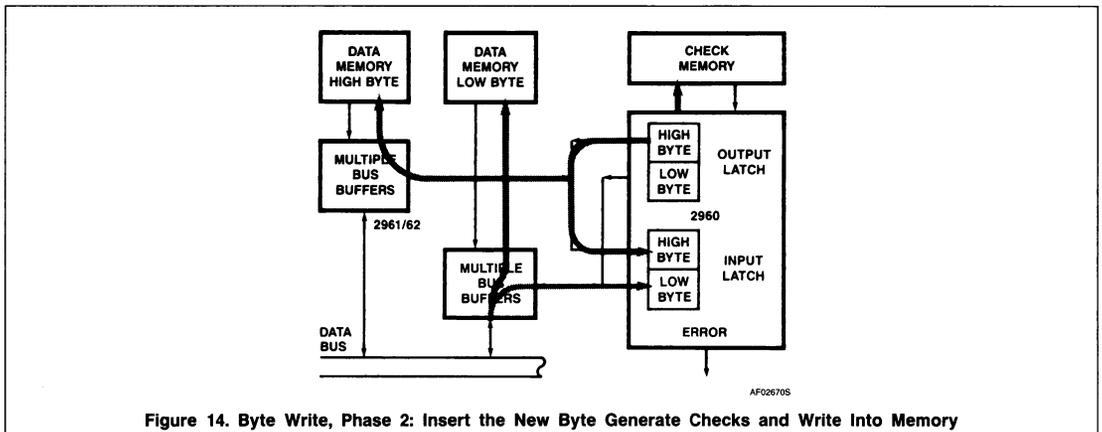


Figure 14. Byte Write, Phase 2: Insert the New Byte Generate Checks and Write Into Memory

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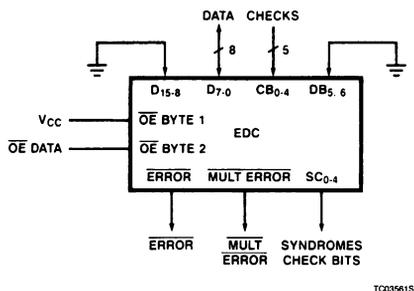


Figure 15. 8-Bit Configuration

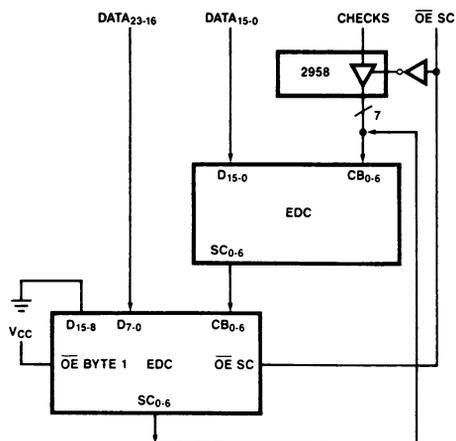
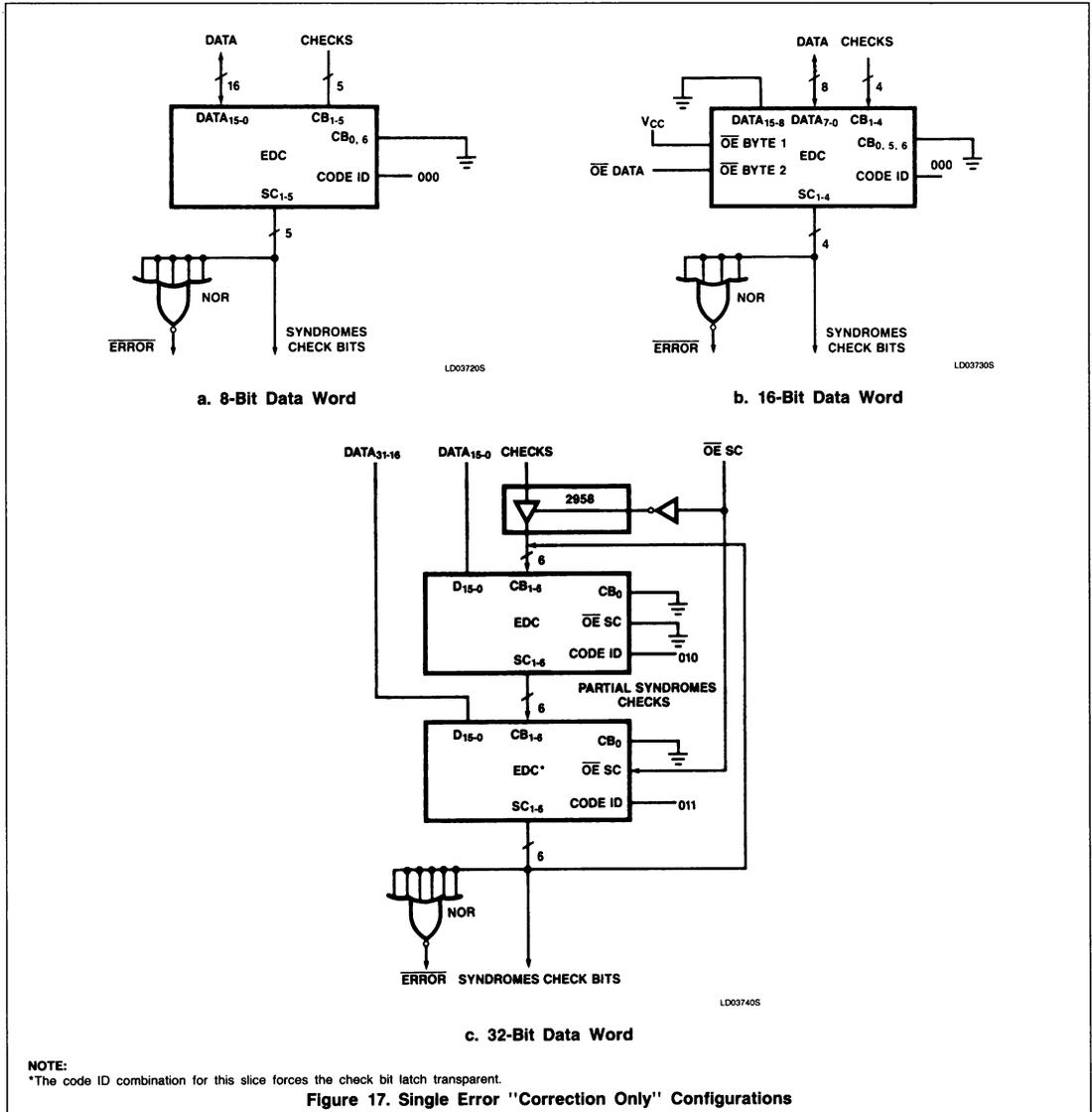


Figure 16. 24-Bit Configuration

Error Detection and Correction (EDC) Unit

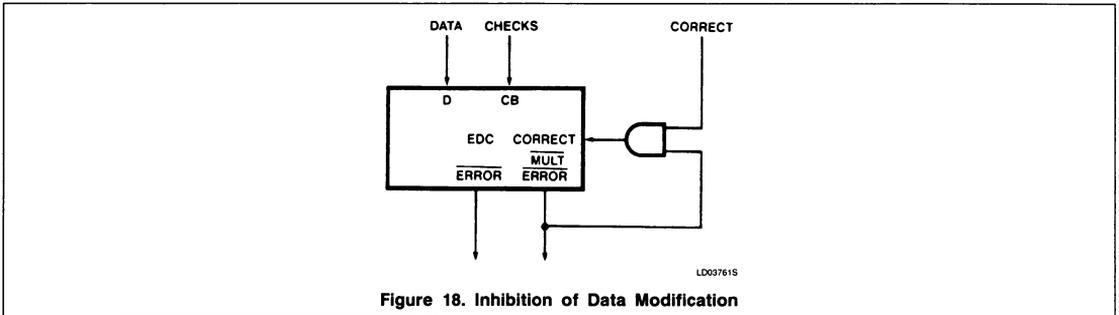
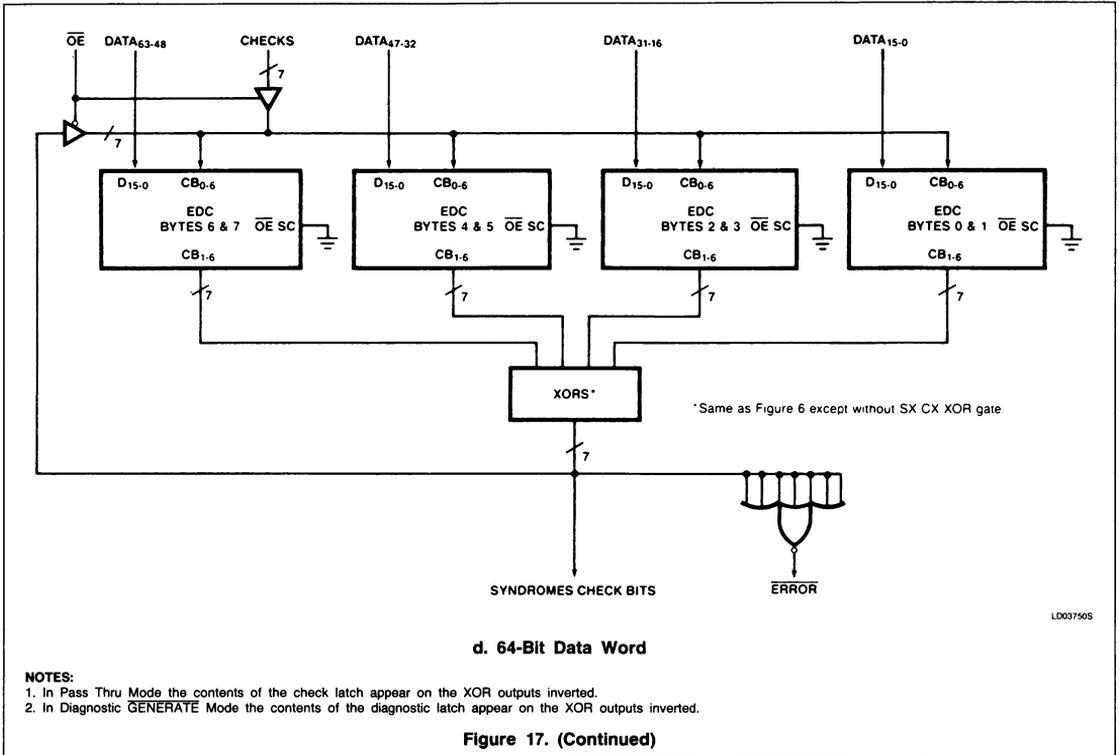
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Error Detection and Correction (EDC) Unit

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2964B Dynamic Memory Controller

Product Specification

Logic Products

FEATURES

- **Operating Options** — controls 16K or 64K DRAMs
- **8-Bit Refresh Counter** — refresh address generation, clear input, and selectable terminal count (128 or 256) output
- **Row Address Decoder** — four Active Row Address Select (RAS) outputs during refresh
- **On-Chip Latches** — dual 8-bit address latches and RAS decoder latches
- **User-Selectable Refresh Modes** — burst, distributed or transparent
- **3-port, 8-bit address multiplexer** with Schottky speed
- **Non-inverting address for RAS and CAS input paths**

PRODUCT DESCRIPTION

The Signetics 2964B Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation, and RAS/CAS control for dynamic RAMs of any data width. The eight-bit address path is designed for 64K DRAMs but can be used equally well with 16K DRAMs. Sixteen address input latches and two row address select latches (for higher order addresses) allow the DMC to control up to 256K words of memory (with 64K DRAMs) by using the internal RAS decoder to select from one-of-four banks of DRAMs.

FUNCTIONAL OPERATION

The Signetics 2964B Dynamic Memory Controller (Figure 1) replaces a dozen MSI devices by grouping several unique

functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the DRAM address lines.

The 2964B also includes a special RAS decoder and CAS buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

The RAS Decoder allows upper addresses to select one-of-four banks of DRAM by determining which bank receives an RAS input. During refresh (RFSH = LOW), the decoder mode is changed to four-of-four and all banks of

BLOCK DIAGRAM

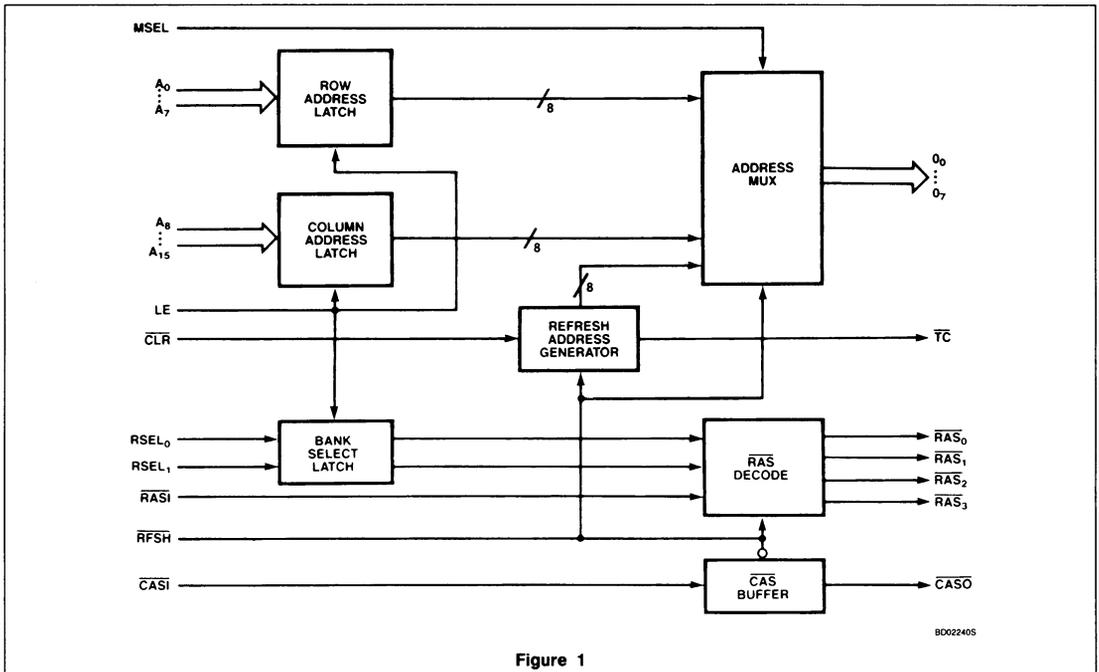


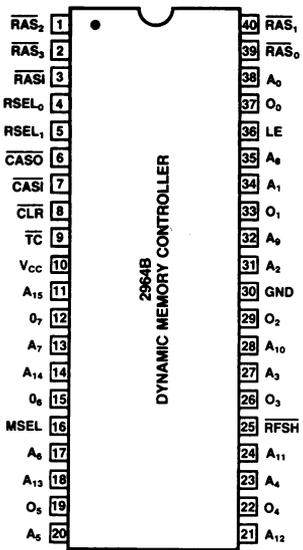
Figure 1

Dynamic Memory Controller

2964B

2964B PACKAGE/PIN DESIGNATIONS

PIN NO.	IDENTIFIER	FUNCTION
1, 2, 39 and 40	$\overline{RAS}_2, \overline{RAS}_3$ and $\overline{RAS}_0, \overline{RAS}_1$	Row Address Strobe outputs (\overline{RAS}_i). Each provides a Row Address Strobe for one of the four banks of memory. Each will go active LOW only when selected by $RSEL_0$ and $RSEL_1$ and only when \overline{RAS}_i goes active LOW. All \overline{RAS}_{0-3} outputs go active low in response to \overline{RAS}_i when \overline{RFSH} goes LOW.
3	\overline{RAS}_i	The Row Address Strobe input. During normal memory cycles, the selected \overline{RAS} Decoder output, $\overline{RAS}_0, \overline{RAS}_1, \overline{RAS}_2$ or \overline{RAS}_3 , will go active LOW in response to an active LOW input at \overline{RAS}_i . During refresh ($\overline{RFSH} = \text{LOW}$), all \overline{RAS} outputs go LOW in response to $\overline{RAS}_i = \text{LOW}$.
4 and 5	$RSEL_0$ and $RSEL_1$	The \overline{RAS} decoder Select inputs. Data (latched) at these inputs (normally higher-order addresses) is decoded by the \overline{RAS} Decoder to "RAS Select" one of four banks of memory with $\overline{RAS}_0, \overline{RAS}_1, \overline{RAS}_2$ or \overline{RAS}_3 .
6	\overline{CAS}_0	The Column Address Strobe output. The active LOW \overline{CAS}_0 output strobes the Column Address into the dynamic RAM. \overline{CAS}_0 is inhibited during refresh ($\overline{RFSH} = \text{LOW}$).
7	\overline{CAS}_i	The Column Address Strobe. An active LOW input at \overline{CAS}_i will result in an active LOW output at \overline{CAS}_0 , unless a refresh cycle is in progress ($\overline{RFSH} = \text{LOW}$).
8	\overline{CLR}	The refresh counter Clear input. An active LOW input at \overline{CLR} resets the refresh counter to all LOW (refresh address output to all HIGH).
9	\overline{TC}	The Terminal Count output. A LOW output at \overline{TC} indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on A_{15} . The \overline{TC} output remains active LOW until the refresh counter is advanced by the rising edge of \overline{RAS}_i or \overline{RFSH} .
10	V_{CC}	+5V power supply
11, 14, 18, 21, 24, 28, 32 and 35	$A_{15} - A_8$	The high-order Address inputs are used to latch eight Column Address inputs for the DRAM. These inputs drive the outputs $O_0 - O_7$ when $MSEL$ is LOW — see next paragraph.
12, 15, 19, 22, 26, 29, 33 and 37	$O_7 - O_0$	The DRAM address outputs. The eight-bit width is designed for DRAMs up to 64K.
13, 17, 20, 23, 27, 31, 34 and 38	$A_7 - A_0$	The low-order Address inputs are used to latch eight Row Address inputs for the DRAM. These inputs drive the outputs $O_0 - O_7$ when $MSEL$ is HIGH.
16	$MSEL$	The Multiplexer-SElect input determines whether low-order or high-order address inputs appear at the multiplexer outputs $O_0 - O_7$. When $MSEL$ is HIGH, the low-order address latches ($A_0 - A_7$) are connected to the outputs. When $MSEL$ is LOW, the high-order address latches are connected to the outputs.



Dynamic Memory Controller

2964B

2964B PACKAGE/PIN DESIGNATIONS (Continued)

PIN NO.	IDENTIFIER	FUNCTION	PIN NO.	IDENTIFIER	FUNCTION
25	RFSH	The Refresh control input. When active LOW, the $\overline{\text{RFSH}}$ input switches the address output multiplexer to output the inverted contents of the 8-bit refresh counter. $\overline{\text{RFSH}}$ LOW also inhibits the $\overline{\text{CAS}}$ buffer and changes the mode of the $\overline{\text{RAS}}$ decoder from one-of-four to four-of-four so that all four $\overline{\text{RAS}}$ decoder outputs, $\overline{\text{RAS}}_0$, $\overline{\text{RAS}}_1$, $\overline{\text{RAS}}_2$ and $\overline{\text{RAS}}_3$, go LOW in response to a LOW input at $\overline{\text{RAS}}_i$. This action refreshes one row address in each of the four $\overline{\text{RAS}}$ decoded memory banks. The refresh counter is advanced at the end of each cycle by the LOW-to-HIGH transition of $\overline{\text{RFSH}}$ or $\overline{\text{RAS}}_i$ (whichever occurs first). In burst mode refresh, $\overline{\text{RFSH}}$ may be held LOW and refresh accompanied by toggling $\overline{\text{RAS}}_i$.	30	GND	Ground.
			36	LE	The address latch enable input. An active HIGH input at LE causes the two 8-bit address latches and the 2-bit $\overline{\text{RAS}}$ Select input latch to go transparent, accepting new input data. A LOW input on LE latches the input data which meets set-up and hold time requirements.

memory receive an $\overline{\text{RAS}}$ input for refresh in response to an $\overline{\text{RAS}}_i$ active LOW input. $\overline{\text{CAS}}$ is inhibited during refresh.

Burst mode refresh is accomplished by holding $\overline{\text{RFSH}}$ low and toggling $\overline{\text{RAS}}_i$.

A_{15} is a dual function input which controls the refresh counter's range. For 64K DRAMS, it is

an address input. For 16K DRAMS, it can be pulled to +12V through 1K to terminate the refresh count at 128 instead of 256.

TRUTH TABLES: RAS OUTPUT FUNCTIONS

RFSH	RAS _i	RSEL ₁	RESEL ₀	RAS ₀	RAS ₁	RAS ₂	RAS ₃
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

CAS₀ FUNCTION

RFSH	CAS _i	CAS ₀
H	L	L
H	H	H
L	X	H

ADDRESS OUTPUT FUNCTIONS

MSEL	RFSH	0 ₀ - 0 ₇
H	H	A ₀ - A ₇
L	H	A ₈ - A ₁₅
X	L	Refresh Address

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Dynamic Memory Controller

2964B

REFRESH ADDRESS COUNTER FUNCTION

A ₁₅	CLR	RFSH	RAS _i	TC	REFRESH COUNT	FUNCTION
X	L	X	X	X	FF _H	Clear counter
X	H		X	X	NC	Output refresh address no change for counter
X	H		L	X	Count - 1	Return to memory cycle mode and decrement counter
X	H	L		X	NC	Output all RAS _i to RAM no change for counter
X	H	L		X	Count - 1	Return RAS _i to HIGH and decrement counter
L or H	H	X	X	L	00 _H	Terminal count for 256 line refresh
+12V*	H	X	X	L	00 _H and 80 _H	Terminal count for 128 line refresh

*Through 1K Ω resistor.

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage temperature	-65 to +150°C
Temperature (ambient) under bias	-55 to +125°C
Supply voltage to ground potential	-0.5 to +7.0V
DC voltage applied to outputs for high output state	+0.5V to +V _{CC} MAX
DC input voltage	-0.5 to 5.5V
DC output current, into outputs	30mA
DC input current	-30 to +5.0mA

Dynamic Memory Controller

2964B

DC ELECTRICAL CHARACTERISTICS Commercial: $T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V}$ ($\pm 5\%$), (Min = 4.75V), (Max = 5.25V)

DESCRIPTION	TEST CONDITIONS ¹		2964B			UNIT
			Min	Typ ²	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -1\text{mA}$	\overline{TC}	2.5			V
		Others	3.0			V
V_{OH} Output HIGH voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -15\text{mA}$	All outputs except \overline{TC}	2.0			V
V_{OL} Output LOW voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or I_{IL}	All outputs except \overline{TC} , $I_{OL} = 16\text{mA}$			0.5	V
		\overline{TC} , $I_{OL} = 8\text{mA}$			0.5	V
V_{IH} Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL} Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_{IN} = -18\text{mA}$				-1.5	V
I_{IL} Input LOW current	$V_{CC} = \text{MAX}$ $V_{IN} = 0.4\text{V}$	RAS \overline{I}			-3.2	mA
		$\overline{\text{CAS}}\overline{I}$, MSEL, $\overline{\text{RFSH}}$			-1.6	mA
		$A_0 - A_{15}$, $\overline{\text{CLR}}$ RSEL $_{0,1}$, LE			-0.4	mA
I_{IH} Input HIGH current	$V_{CC} = \text{MAX}$ $V_{IN} = 2.7\text{V}$	RAS \overline{I}			100	μA
		$\overline{\text{CAS}}\overline{I}$, MSEL, $\overline{\text{RFSH}}$			50	μA
		$A_0 - A_{15}$, $\overline{\text{CLR}}$ RSEL $_{0,1}$, LE			20	μA
I_I Input HIGH current	$V_{CC} = \text{MAX}$ $V_{IN} = -5.5\text{V}$	RAS \overline{I}			2.0	mA
		$\overline{\text{CAS}}\overline{I}$, MSEL, $\overline{\text{RFSH}}$			1.0	mA
	$V_{CC} = \text{MAX}$ $V_{IN} = 5.5\text{V}$	$A_0 - A_{15}$, $\overline{\text{CLR}}$ RSEL $_{0,1}$, LE			0.1	mA
I_{SC} Output short circuit current	$V_{CC} = \text{MAX}$ (note 3)		-40		-100	mA
I_{CC} Power supply current (note 4)	25°C, 5V	Com ¹		122		mA
	0 to 70°C				173	mA
	70°C				165	mA
I_T A_{15} Enable current	A_{15} connected to +12V through $1\text{K}\Omega \pm 10\%$				5	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under DC Electrical Characteristics for the applicable device type.
- Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
- Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
- I_{CC} is worst case when the Address inputs are latched HIGH, the refresh counter is at terminal count (255), RAS \overline{I} and $\overline{\text{CAS}}\overline{I}$ are HIGH and all other inputs are LOW.

Dynamic Memory Controller

2964B

AC ELECTRICAL CHARACTERISTICS

Tables 1 and 2 specify performance characteristics of the Signetics 2964B over the

operating range for capacitive loads of 50 and 150 picofarads, respectively. Note that the minimum specified limits for t_{PW} , t_S , and t_H are for minimum system operating require-

ments and that limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device. All AC parameters are specified at 1.5 volts.

Table 1. Performance Characteristics for Capacitive Loading of 50 Picofarads

PARAMETER — See Figure 2.	DESCRIPTION	$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	COMMERCIAL		UNIT
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$		
		Typ	Min	Max	
1 t_{PD}	A_i to O_i Delay	14		19	ns
2 t_{PHL}	\overline{RAS}_i to \overline{RAS}_i ($\overline{RFSH} = H$)	14		20	ns
3 t_{PHL}	\overline{RAS}_i to \overline{RAS}_i ($\overline{RFSH} = L$)	14		20	ns
4 t_{PD}	MSEL to O_i	17	9		ns
5 t_{PD}	MSEL to O_i	17		21	ns
6 t_{PHL}	\overline{CAS}_i to \overline{CAS}_i ($\overline{RFSH} = H$)	12		17	ns
7 t_{PHL}	$RSEL_i$ to \overline{RAS}_i ($LE = H, \overline{RAS}_i = L$)	15		20	ns
8 t_{PLH}	\overline{RFSH} to \overline{TC} ($\overline{RAS}_i = L$)	30		40	ns
9 t_{PLH}	\overline{RAS}_i to \overline{TC} ($\overline{RFSH} = L$)	25		35	ns
10 t_{PW}	$\overline{RAS}_i = L$ ($\overline{RFSH} = L$)	10	50		ns
11 t_{PW}	$\overline{RAS}_i = H$ ($\overline{RFSH} = L$)	10	50		ns
12 t_{PD}	\overline{RFSH} to O_i ($\overline{RAS}_i = X$)	17		21	ns
13 t_{PHL}	\overline{RFSH} to \overline{RAS}_i ($\overline{RAS}_i = L$)	19		26	ns
14 t_{PW}	$\overline{CLR} = L$	10	30		ns
15 t_{PLH}	\overline{RFSH} to \overline{CAS}_i ($\overline{RAS}_i = L, \overline{CAS}_i = L$, Note 1)	16		21	ns
16 t_{PD}	LE to O_i	25		35	ns
17 t_{PHL}	LE to \overline{RAS}_i	30		40	ns
18 t_{PLH}	\overline{CLR} to \overline{TC}	35		45	ns
19 t_{PLH}	\overline{CLR} to O_i ($\overline{RFSH} = L$)	31		44	ns
20 t_S	A_i to LE Set-up time	0	5		ns
21 t_H	A_i to LE Hold time	5	12		ns
22 t_S	$RSEL_i$ to LE Set-up time	0	5		ns
23 t_H	$RSEL_i$ to LE Hold time	10	17		ns
24 t_S	\overline{CLR} Recovery time	10	16		ns
25 t_{SKEW}	O_i to \overline{RAS}_i ($\overline{RFSH} = H$, Note 2)	2		5	ns
26 t_{SKEW}	O_i to \overline{CAS}_i (Note 2)	6		8	ns
27 t_{SKEW}	O_i to \overline{RAS}_i ($\overline{RFSH} = L$, Note 3)	6		8	ns
28 t_{SKEW}	O_i to \overline{RAS}_i (MSEL = Z, Note 4)	1		5	ns

Dynamic Memory Controller

2964B

AC ELECTRICAL CHARACTERISTICS (Continued)

Table 2. Performance Characteristics for Capacitive Loading of 150 Picofarads

PARAMETER — See Figure 2.	DESCRIPTION	$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	COMMERCIAL		UNIT
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$		
			Typ	Min	
1 t_{PD}	A_i to O_i Delay	20		25	ns
2 t_{PHL}	\overline{RAS}_i to \overline{RAS}_i (RFSH = H)	18		24	ns
3 t_{PHL}	\overline{RAS}_i to \overline{RAS}_i (RFSH = L)	18		24	ns
4 t_{PD}	MSEL to O_i	23	12		ns
5 t_{PD}	MSEL to O_i	23		27	ns
6 t_{PHL}	\overline{CAS}_i to \overline{CAS}_i (RFSH = H)	17		24	ns
7 t_{PHL}	RSEL _i to \overline{RAS}_i (LE = H, $\overline{RAS}_i = L$)	19		27	ns
8 t_{PLH}	RFSH to \overline{TC} ($\overline{RAS}_i = L$)	34		45	ns
9 t_{PLH}	\overline{RAS}_i to \overline{TC} (RFSH = L)	32		45	ns
10 t_{PW}	$\overline{RAS}_i = L$ (RFSH = L)	10	50		ns
11 t_{PW}	$\overline{RAS}_i = H$ (RFSH = L)	10	50		ns
12 t_{PD}	RFSH to O_i ($\overline{RAS}_i = X$)	21		27	ns
13 t_{PHL}	RFSH to \overline{RAS}_i ($\overline{RAS}_i = L$)	25		33	ns
14 t_{PW}	$\overline{CLR} = L$	10	30		ns
15 t_{PLH}	RFSH to \overline{CAS}_i ($\overline{RAS}_i = L$, $\overline{CAS}_i = L$, Note 1)	21		27	ns
16 t_{PD}	LE to O_i	30		40	ns
17 t_{PHL}	LE to \overline{RAS}_i	34		45	ns
18 t_{PLH}	\overline{CLR} to \overline{TC}	39		55	ns
19 t_{PLH}	\overline{CLR} to O_i (RFSH = L)	38		50	ns
20 t_S	A_i to LE Set-up time	0	5		ns
21 t_H	A_i to LE Hold time	5	12		ns
22 t_S	RSEL _i to LE Set-up time	0	5		ns
23 t_H	RSEL _i to LE Hold time	10	17		ns
24 t_S	\overline{CLR} Recovery time	10	16		ns
25 t_{SKEW}	O_i to \overline{RAS}_i (RFSH = H, Note 2)	3		6	ns
26 t_{SKEW}	O_i to \overline{CAS}_i (note 2)	6		8	ns
27 t_{SKEW}	O_i to \overline{RAS}_i (RFSH = L, Note 3)	6		9	ns
28 t_{SKEW}	O_i to \overline{RAS}_i (MSEL \overline{L} , Note 4)	1		5	ns

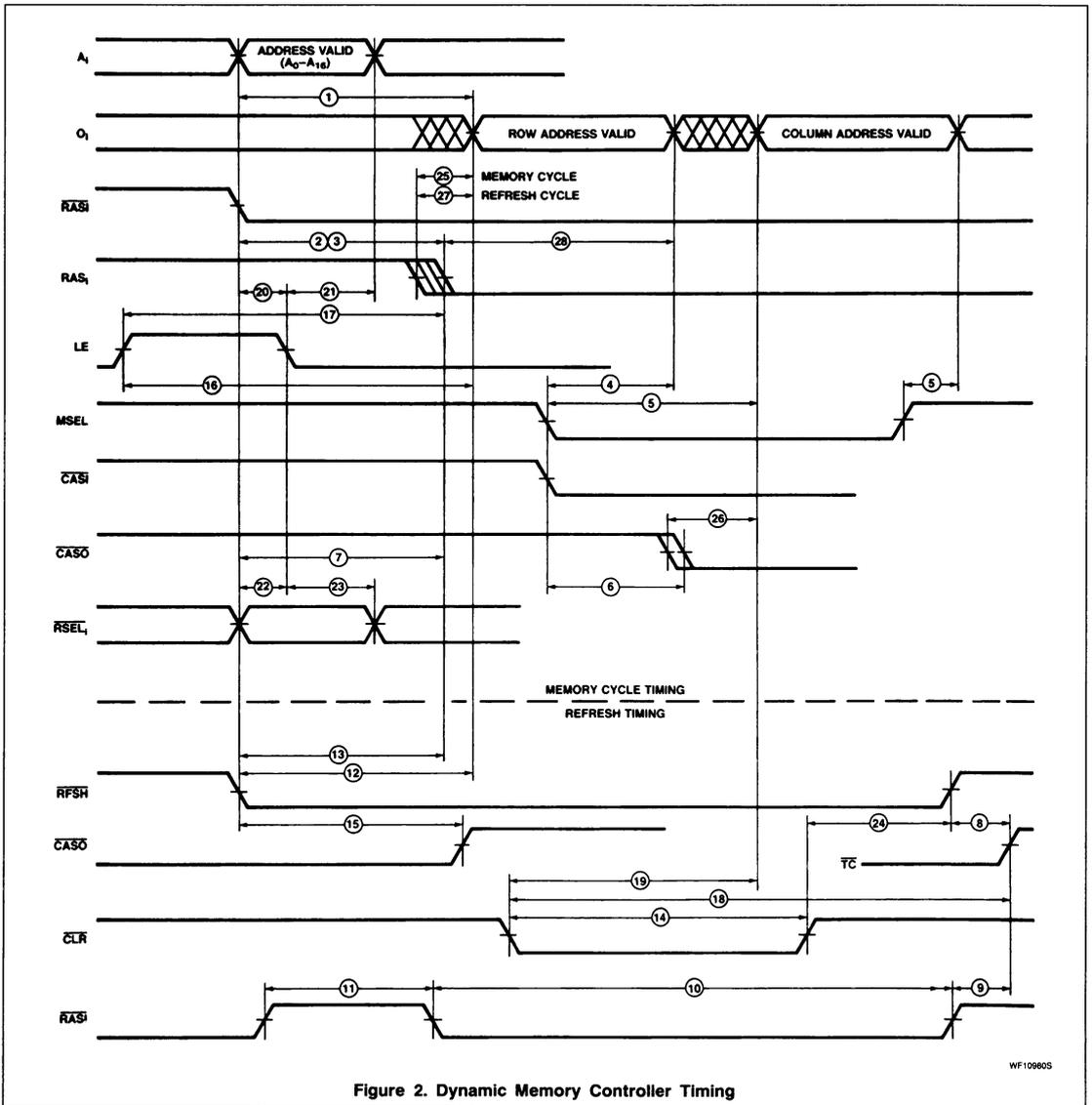
NOTES:

- RFSH inhibits \overline{CAS}_i during refresh. Specification is for \overline{CAS}_i inhibit time.
- O_i to \overline{RAS}_i (RFSH = HIGH) skew is guaranteed maximum difference between fastest \overline{RAS}_i to \overline{RAS}_i delay and slowest A_i to O_i delay within a single device. O_i to \overline{CAS}_i skew is maximum difference between fastest \overline{CAS}_i to \overline{CAS}_i delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.
- O_i to \overline{RAS}_i (RFSH = LOW) skew is guaranteed maximum difference between fastest \overline{RAS}_i to \overline{RAS}_i delay and slowest RFSH to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.
- O_i to \overline{RAS}_i (MSEL \overline{L}) skew is guaranteed maximum difference between fastest MSEL \overline{L} to O_i delay and slowest \overline{RAS}_i to \overline{RAS}_i delay within a single device.

Dynamic Memory Controller

2964B

TIMING DIAGRAM



Dynamic Memory Controller

2964B

MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 3. T_1 , T_2 , and T_3 represent the minimum timing requirements at the DMC inputs

to guarantee that DRAM timing requirements are met and that maximum system performance is achieved.

The minimum requirements for T_1 , T_2 , and T_3 are as follows:

$$T_1 \text{MIN} = t_{RAH} + t_{28}$$

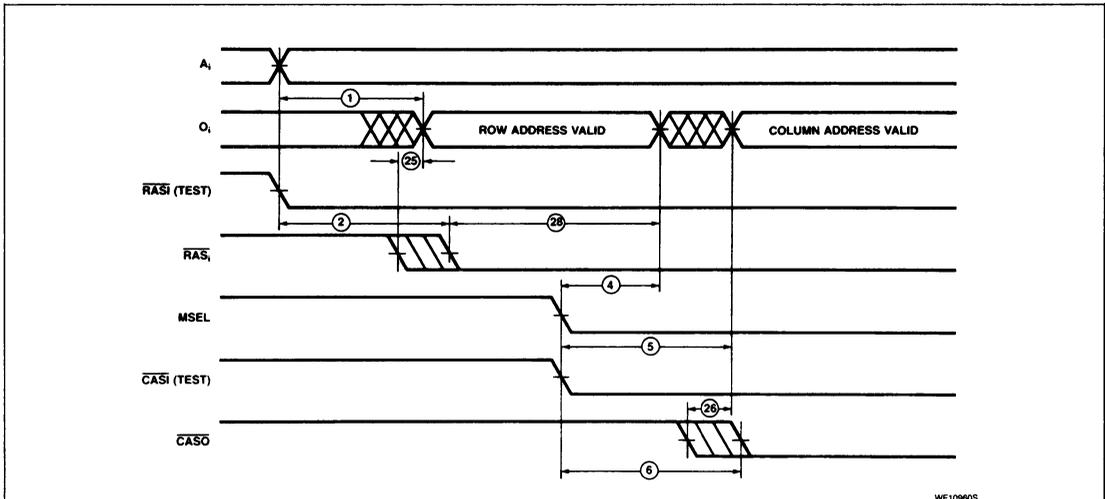
$$T_2 \text{MIN} = t_1 + t_{26} + t_{ASC}$$

$$T_3 \text{MIN} = t_{ASR} + t_{25} \text{ where,}$$

$$t_{RAH} = \text{Row Address Hold Time}$$

$$t_{ASC} = \text{Column Address Set-up Time}$$

$$t_{ASR} = \text{Row Address Set-up Time}$$

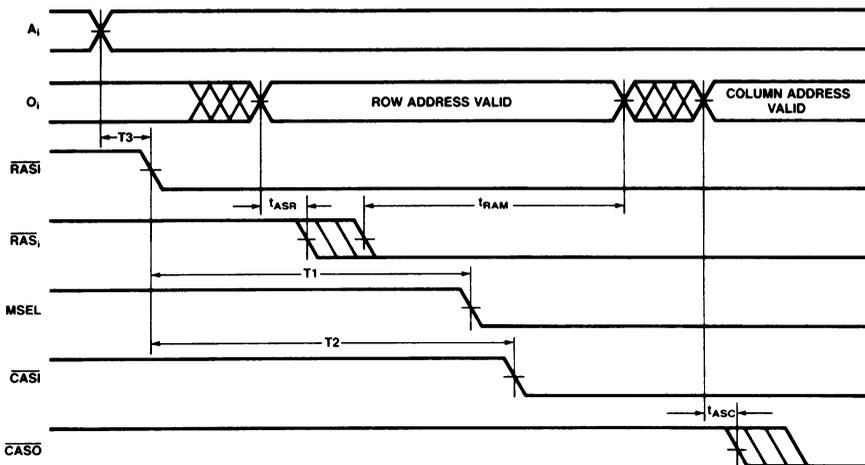


WF109605

Legend

- ⊗ = Guaranteed maximum difference between fastest \overline{RAS}_i to \overline{RAS}_i delay and the slowest A_1 to O_1 delay on any single device.
- ⊗ = Guaranteed maximum difference between fastest \overline{CAS}_i to \overline{CAS}_i delay and the slowest $MSEL$ to O_1 delay on any single device.
- ⊗ = Guaranteed maximum difference between fastest $MSEL$ to O_1 delay and the slowest \overline{RAS}_i to \overline{RAS}_i delay on any single device.

a. Specifications Applicable to Memory Cycle Timing



WF109705

b. Desired System Timing

Figure 3. Memory Cycle Timing

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Dynamic Memory Controller

2964B

ORDERING INFORMATION

Commercial:

N2964BN (Plastic)
N2964BI (Ceramic)

PACKAGE DATA

Type: Plastic or Ceramic
Configuration: DIP
Width: 0.6 in.
Length: 2.0 in.
Pin Centers: 0.1 in.

APPLICATIONS

Speed with Minimum Skew

The DMC provides Schottky speed in all of the critical paths. In addition, time skew between the Address, RAS and CAS paths is minimized (and specified) by placing these functions on the same chip. The inclusion of the CAS buffer allows matching of its propagation delay, and also provides the CAS inhibit function during RAS — only refresh.

Input Latches

The eighteen input latches are transparent when LE is HIGH and latch the input data, meeting the set-up and hold time requirements when LE goes LOW. In systems with separate address and data buses, LE may be permanently enabled HIGH.

Refresh Counter

The 8-bit refresh counter provides both 128 and 256 line refresh capability. Refresh con-

trol is external to allow maximum user flexibility. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counter is advanced at the LOW-to-HIGH transition of RFSH (or RASI). This assures a stable counter output for the next refresh cycle. The counter will continue to cycle through 256 addresses unless reset to zero by CLR. This actually causes all output to go HIGH since the output MUX is inverting. (Address inputs to outputs are non-inverting since both the input latches and output MUX are inverting.)

Refresh Terminal Count

The refresh counter also provides a Terminal Count output for burst mode refresh applications. TC normally occurs at count 255 (00₇ to 0₇ all LOW when RFSH is LOW). TC can be made to occur at count 127 for 128 line burst mode refresh by pulling A₁₅ up to +12V through a 1K Ω \pm 10% resistor. The counter actually cycles through 256 with TC determined by A₁₅. Otherwise A₁₅ functions as an address input when driven at normal TTL levels.

Three-Input 8-Bit Address Multiplexer

The address MUX is 8-bits wide (for 64K DRAMs) and has three data sources, the lower address input latch (A₀ to A₇), the upper address input latch (A₈ to A₁₅), and the internal refresh counter. The lower address latch is selected when MSEL is HIGH. This is

normally the Row address. The upper address latch is selected when MSEL is LOW. This is normally the Column address. The third source — the refresh counter is selected when RFSH is LOW and overrides MSEL.

When RFSH goes LOW, the MUX selects the refresh counter address and CASO is inhibited. Also, the RAS Decoder function is changed from one-of-four to four-of-four so all RAS outputs RAS₀ – RAS₃ go low to refresh all banks of memory when RASI goes LOW. When RFSH is HIGH, only one RAS output goes low, determined by the RAS Select inputs, RSEL₀ and RSEL₁. In either case the RAS Decoder output timing is controlled by RASI to make sure the refresh count appears at 00₀ – 0₇ before RAS₀ – RAS₃ goes LOW. This assures meeting Row address Set-up time requirement of the DRAM (t_{ASR}).

Maximum Performance System

The typical organization of a maximum performance 16-bit system including Error Detection and Correction is shown in Figure 6. Delay lines provide the most accurate timing and are recommended for RAS, MSEL, and CAS timing in this type of system.

Controlling 16K RAMS or Smaller Systems

16K DRAMs require seven address inputs and 128 line refresh. Also A₀ is often used to designate upper or lower byte transactions in 16-bit systems. These modifications are shown in Figure 7.

N3001 Microprogram Control Unit

Product Specification

Logic Products

FEATURES

- Schottky TTL process
- 45ns cycle time (typ.)
- Direct addressing of standard bipolar PROM or ROM
- 512 microinstruction addressability
- Advanced organization:
 - 9-bit microprogram address register and bus organized to address memory by row and column
 - 4-bit program latch
 - 2-flag registers
- 11 address control functions:
 - 3 jump and test latch functions
 - 16 way jump and test instructions
- 8 flag control functions:
 - 4 flag input functions
 - 4 flag output functions

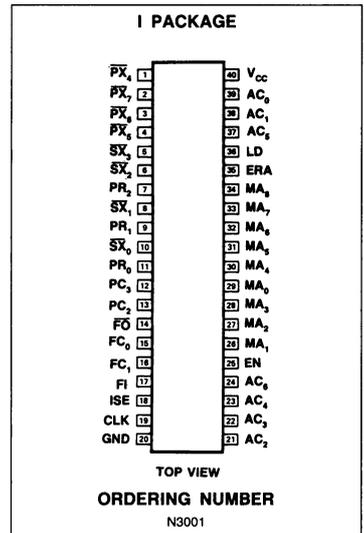
DESCRIPTION

The N3001 MCU is 1 element of a bipolar microcomputer set. When used with the N3002, 74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

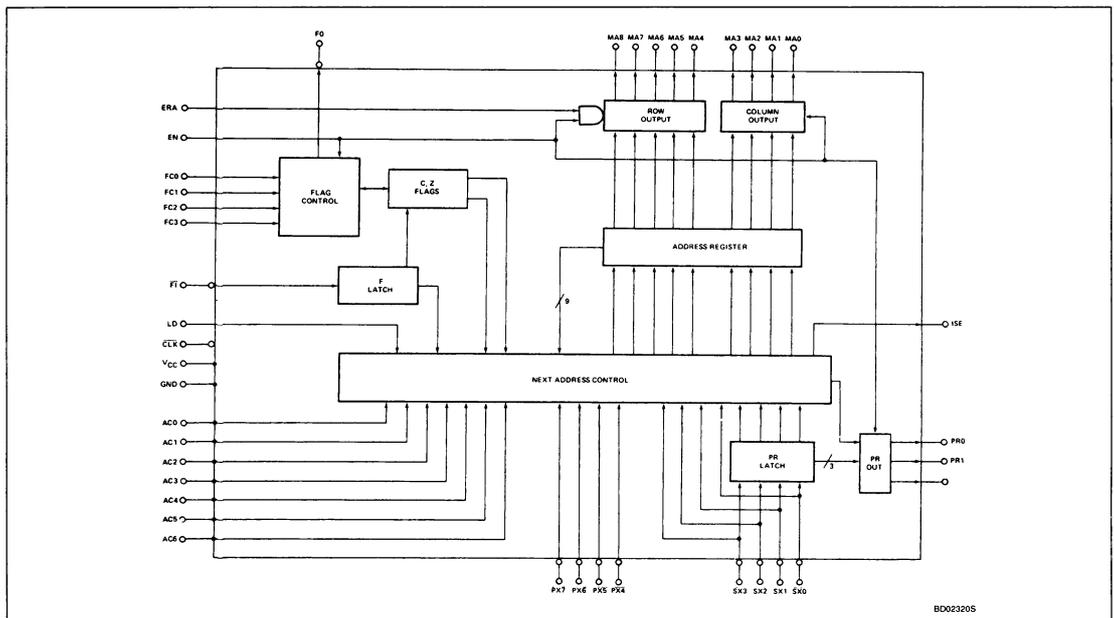
The N3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the N3001 include:

- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input buses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

PIN CONFIGURATION



BLOCK DIAGRAM



Microprogram Control Unit

N3001

PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1 - 4	$\overline{PX}_4 - \overline{PX}_7$	Primary Instruction Bus Inputs: Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active low
5, 6, 8, 10	$\overline{SX}_0 - \overline{SX}_3$	Secondary Instruction Bus Inputs: Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active low
7, 9, 11	PR ₀ - PR ₂	PR-Latch Outputs: The PR-latch outputs (SX ₀ - SX ₂) are synchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collector
12, 13 15, 16	FC ₀ - FC ₃	Flag Logic Control Inputs: The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active high
14	\overline{FO}	Flag Logic Output: The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	Active low Three-state
17	\overline{FI}	Flag Logic Input: The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active low
18	ISE	Interrupt Strobe Enable Output: The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active high
19	CLK	Clock Input	
20	GND	Ground	
21 - 24 37 - 39	AC ₀ - AC ₆	Next Address Control Function Inputs: All jump functions are selected by these control lines.	Active high
25	EN	Enable Input: When in the high state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26 - 29	MA ₀ - MA ₃	Microprogram Column Address Outputs	Three-state
30 - 34	MA ₄ - MA ₈	Microprogram Row Address Outputs	Three-state
35	ERA	Enable Row Address Input: When in the low state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilitate the implementation of priority interrupt systems.	Active high
36	LD	Microprogram Address Load Input: When the active high state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction buses into the microprogram address register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active high
40	V _{CC}	+5 Volt supply	

THEORY OF OPERATION

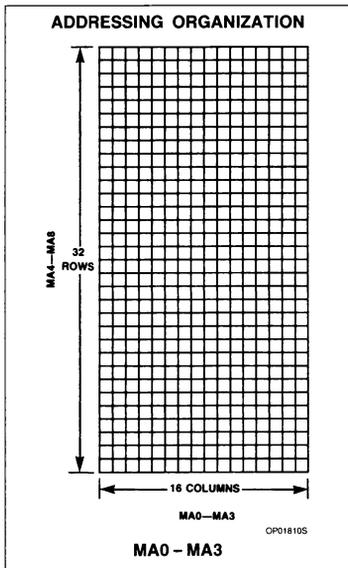
The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaneously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each instruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as a 5-bit row and 4-bit column address.

Microprogram Control Unit

N3001



FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and column addresses.

MNEMONIC	FUNCTION
row _n	5-bit next row address where n is the decimal row address.
col _n	4-bit next column address where n is the decimal column address.

Unconditional Address Control (Jump) Functions

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs (AC₀ - AC₆) to generate the next microprogram address.

JUMP FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JCC	Jump in current column. AC ₀ - AC ₄ are used to select 1 of 32 row addresses in the current column, specified by MA ₀ - MA ₃ , as the next address.
JZR	Jump to zero row. AC ₀ - AC ₃ are used to select 1 of 16 column addresses in row ₀ , as the next address.
JCR	Jump in current row. AC ₀ - AC ₃ are used to select 1 of 16 addresses in the current row, specified by MA ₄ - MA ₈ , as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC ₀ - AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ - MA ₈ , as the next row address. The current column is specified by MA ₀ - MA ₃ . The PR-latch outputs are asynchronously enabled.

JUMP/TEST FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JFL	Jump/test F-latch. AC ₀ - AC ₃ are used to select 1 of 16 row addresses in the current row group, specified by MA ₈ , as the next row address. If the current column group, specified by MA ₃ , is col ₀ - col ₇ , the F-latch is used to select col ₂ or col ₃ as the next column address. If MA ₃ specifies column group col ₈ - col ₁₅ , the F-latch is used to select col ₁₀ or col ₁₁ as the next column address.
JCF	Jump/test C-flag, AC ₀ - AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. If the current column group specified by MA ₃ is col ₀ - col ₇ , the C-flag is used to select col ₂ or col ₃ as the next column address. If MA ₃ specifies column group col ₈ - col ₁₅ , the C-flag is used to select col ₁₀ or col ₁₁ as the next column address. JZF
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.
JPR	Jump/test PR-latch. AC ₀ - AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. The 4 PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test rightmost PR-latch bits. AC ₀ - AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₂ and PR ₃ are used to select 1 of 4 column addresses in col ₄ through col ₇ as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC ₀ and AC ₁ are used to select 1 of 4 high-order row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₀ and PR ₁ are used to select 1 of 4 possible column addresses in col ₁₂ through col ₁₅ as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC ₀ and AC ₁ are used to select 1 of 4 row addresses in the current row group, specified by MA ₈ - MA ₈ , as the next row address. PX ₄ - PX ₇ are used to select 1 of 16 possible column addresses as the next column address. SX ₀ - SX ₃ data is locked in the PR-latch at the rising edge of the clock.

7

Microprogram Control Unit

N3001

Flag Conditional Address

Control (Jump Test) Functions

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

PX-Bus and PR-Latch

Conditional Address Control (Jump/Test) Functions

The PX-bus jump/test function uses the data on the primary instruction bus (PX₄ - PX₇), the current microprogram address control function to generate the next microprogram address. The PR-latch jump/test functions use the data in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Flag Control Functions

The flag control functions of the MCU are selected by the 4 input lines designated FC₀ - FC₃. Function code formats are given in "Flag Control Function summary".

The following is a detailed description of each of the 8 flag control functions.

Flag Input Control Functions

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line.

Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Flag Output Control Functions

The flag output control functions select the value to which the flag output (FO) line will be forced.

FLAG CONTROL FUNCTION

MNEMONIC	FUNCTION DESCRIPTION
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z-flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTION TABLE

MNEMONIC	FUNCTION DESCRIPTION
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC ₁	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	0
	STC	Set C-flag to f	1	1
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC ₃	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	1	0
	FFZ	Force FO to Z-flag	0	1
	FF1	Force FO to 1	1	1

LOAD FUNCTION	NEXT ROW				NEXT COL				
LD	MA ₈	7	6	5	4	MA ₃	2	1	0
0	See Address Control Function Summary								
1	0	X ₃	X ₂	X ₁	X ₀	X ₇	X ₆	X ₅	X ₄

NOTES:

f = Contents of the F-latch
 xn = Data on PX - or
 SX - bus line n (active low)

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION								NEXT ROW					NEXT COL			
		AC ₆	5	4	3	2	1	0	MA ₈	7	6	5	4	MA ₃	2	1	0	
JCC	Jump in current column	0	0	d ₄	d ₃	d ₂	d ₁	d ₀	d ₄	d ₃	d ₂	d ₁	d ₀	m ₃	m ₂	m ₁	m ₀	
JZR	Jump to zero row	0	1	0	d ₃	d ₂	d ₁	d ₀	0	0	0	0	0	d ₃	d ₂	d ₁	d ₀	
JCR	Jump in current row	0	1	1	d ₃	d ₂	d ₁	d ₀	m ₈	m ₇	m ₆	m ₅	m ₄	d ₃	d ₂	d ₁	d ₀	
JCE	Jump in column/enable	1	1	1	0	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	m ₃	m ₂	m ₁	m ₀	
JFL	Jump/test F-latch	1	0	0	d ₃	d ₂	d ₁	d ₀	m ₈	d ₃	d ₂	d ₁	d ₀	m ₃	0	1	f	
JCF	Jump/test C-flag	1	0	1	1	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	m ₃	0	1	c	
JZF	Jump/test Z-flag	1	0	1	1	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	m ₃	0	1	z	
JPR	Jump/test PR-latch	1	1	0	0	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	p ₂	p ₂	p ₁	p ₀	
JLL	Jump/test left PR bits	1	1	0	1	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	0	1	p ₃	p ₂	
JRL	Jump/test right PR bits	1	1	1	1	1	d ₁	d ₀	m ₈	m ₇	1	d ₁	d ₀	1	1	p ₁	p ₀	
JPX	Jump/test PX - bus	1	1	1	1	0	d ₁	d ₀	m ₈	m ₇	m ₆	d ₁	d ₀	X ₇	X ₆	X ₅	X ₄	

NOTES:

dn = Data on address control line n
 mn = Data in microprogram address register bit n

Pn = Data in PR-latch bit n
 xn = Data on PX - bus line n (active low)
 f, c, z = Contents of F-latch, C-flag, or Z-flag respectively

Microprogram Control Unit

N3001

STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active high at the rising edge of the clock, the data on the primary and secondary instruction buses, $PX_4 - PX_7$ and $SX_0 - SX_3$, is loaded into the microprogram address register. $PX_4 - PX_7$ are loaded into $MA_4 - MA_7$. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

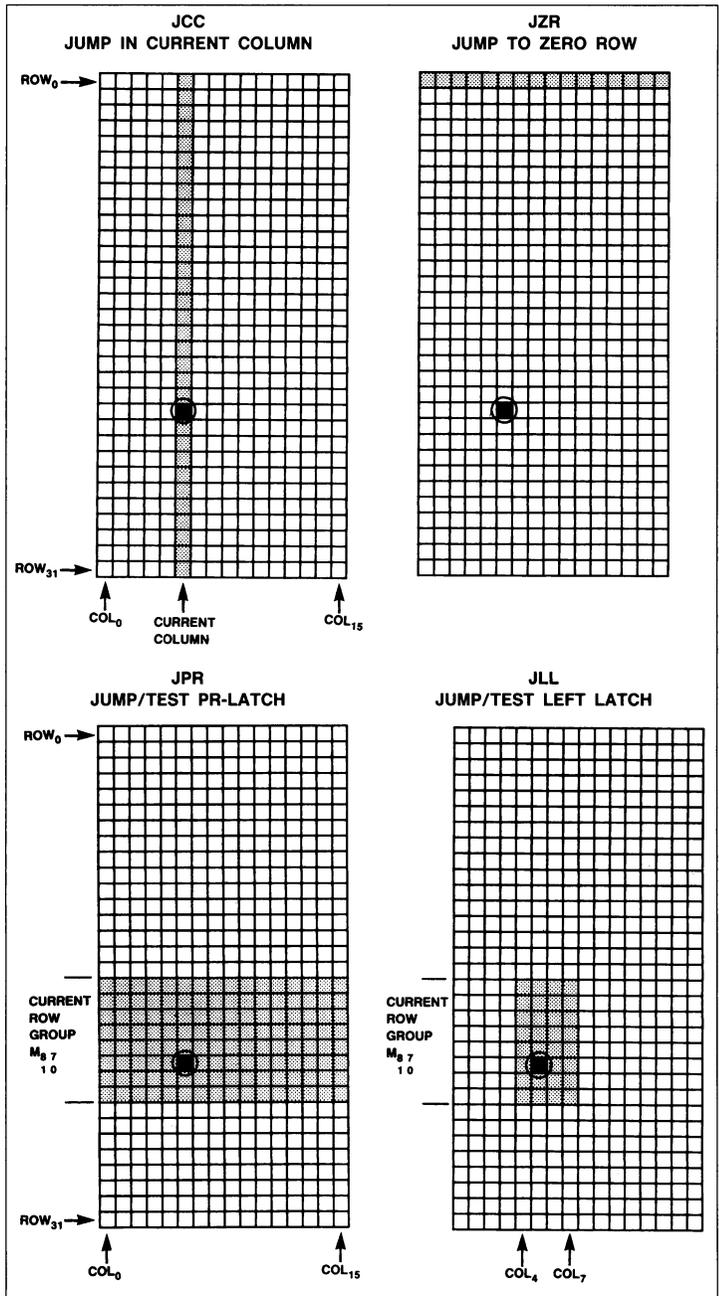
The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in active high state whenever a JZR is col_{15} is selected as the address control function. Generally, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so the interrupt control may be enabled at the beginning of the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on $AC_0 - AC_6$. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

JUMP SET DIAGRAMS

The following 10 diagrams illustrate the jump set for each of the 11 jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents 1 current row (row_{21}) and current column (col_6) address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

JUMP SET DIAGRAMS

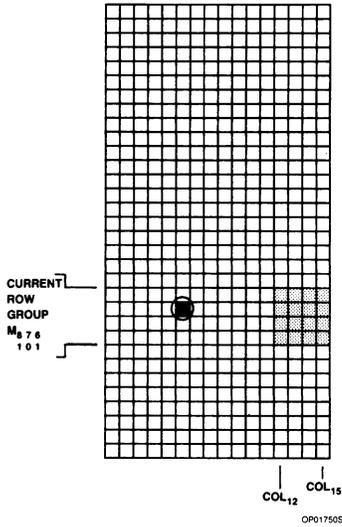


Microprogram Control Unit

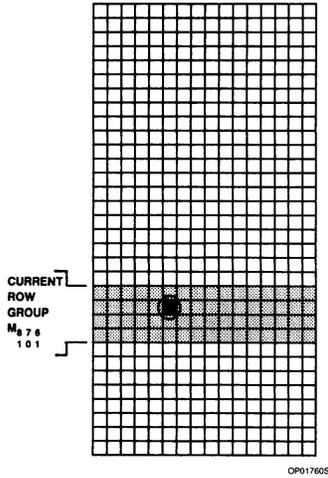
N3001

JUMP SET DIAGRAMS (Continued)

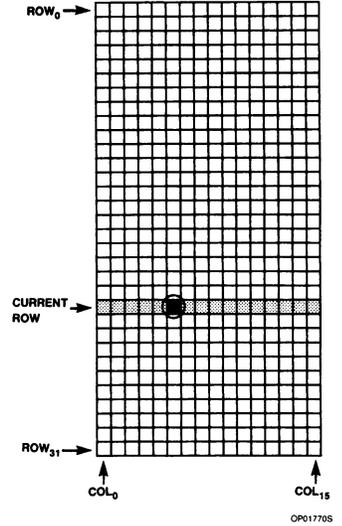
JRL
JUMP/TEST RIGHT LATCH



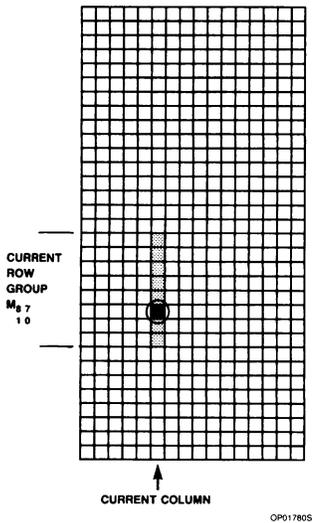
JPX
JUMP/TEST PX-BUS



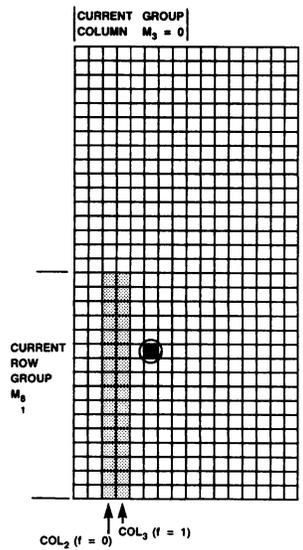
JCR
JUMP IN CURRENT ROW



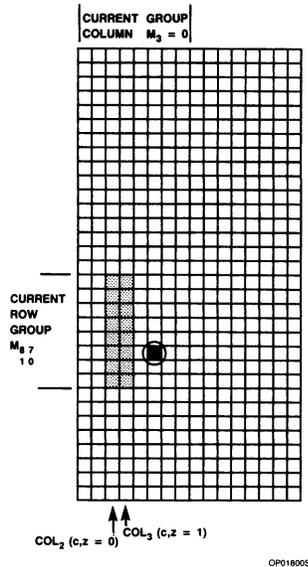
JCE
JUMP COLUMN/ENABLE



JFL
JUMP/TEST F-LATCH



JCF, JZF
JUMP/TEST C-FLAG
JUMP/TEST Z-FLAG



Microprogram Control Unit

N3001

AC ELECTRICAL CHARACTERISTICS N3001 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $\pm 5\%$ 10%

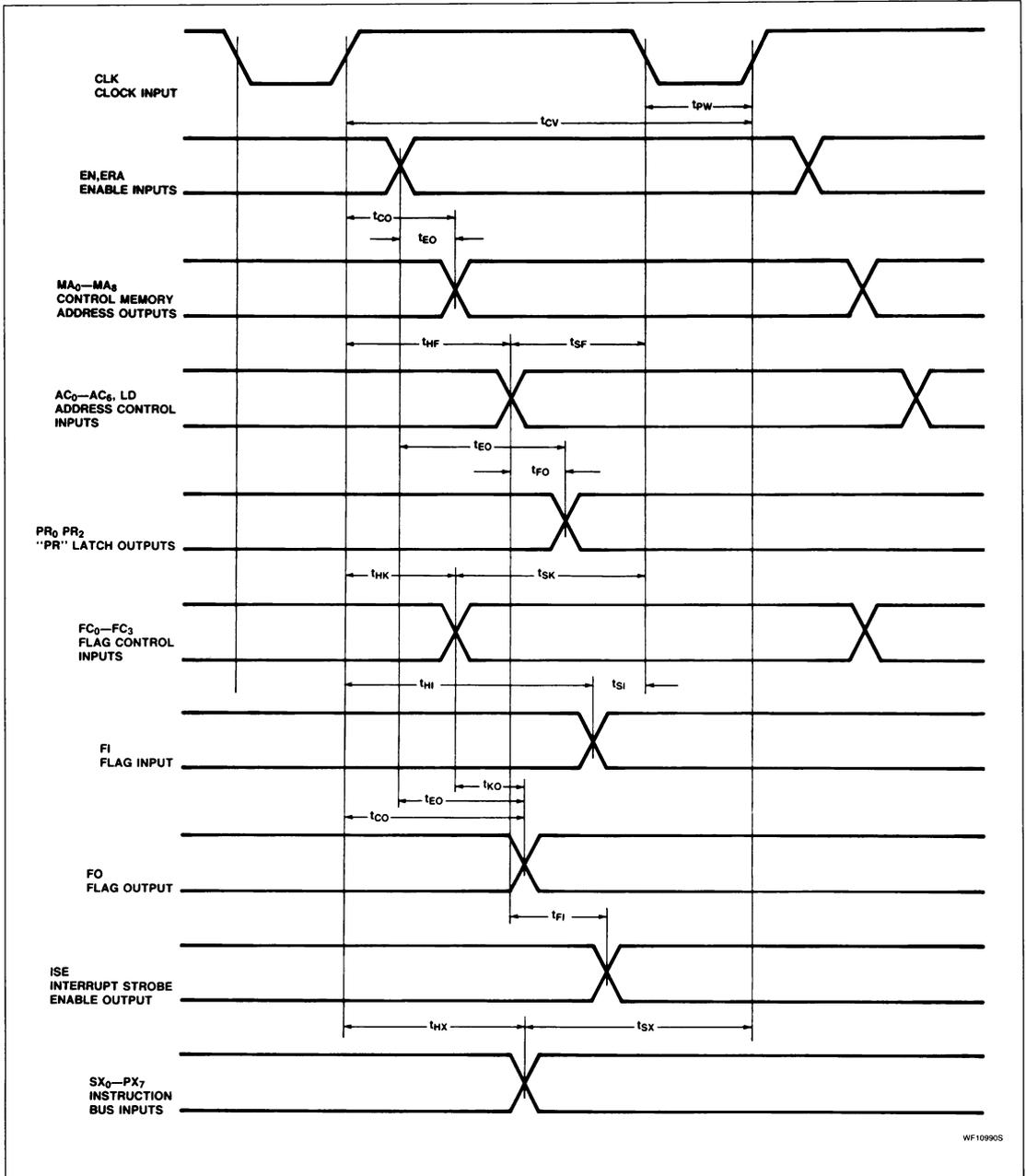
PARAMETER	N3001			UNIT
	Min	Typ ¹	Max	
t_{CY} Cycle time	60	45		ns
t_{PW} Clock pulse width	17	10		ns
t_{SF} Control and data input set-up times: LD, AC ₀ - AC ₆ (Set to "1"/"0")	20	3/14		ns
t_{SK} FC ₀ , FC ₁	7	5		ns
t_{SX} PX ₄ - PX ₇ (Set to "1"/"0")	28	4/13		ns
t_{SI} FI (Set to "1"/"0")	12	-6/0		ns
t_{SX} SX ₀ - SX ₃	15	5		ns
t_{HF} Control and data input hold times: LD, AC ₀ - AC ₆ (Hold to "1"/"0")	4	-3/-14		ns
t_{HK} FC ₀ , FC ₁	4	-5		ns
t_{HX} PX ₄ - PX ₇ (Hold to "1"/"0")	0	-4/-13		ns
t_{HI} FI (Hold to "1"/"0")	16	6.5/0		ns
t_{HX} SX ₀ - SX ₃	0	-5		ns
t_{CO} Propagation delay from clock input (CLK) to outputs (mA ₀ - mA ₈ , FO) (t_{PHL}/t_{PLH})		17/24	36	ns
t_{KO} Propagation delay from control inputs FC ₂ and FC ₃ to flag out (FO)		13	24	ns
t_{FO} Propagation delay from control inputs AC ₀ - AC ₆ to latch outputs (PR ₀ - PR ₂)		21	32	ns
t_{EO} Propagation delay from enable inputs EN and ERA to outputs (mA ₀ - mA ₈ , FO, PR ₀ - PR ₂)		17	26	ns
t_{FI} Propagation delay from control inputs AC ₀ - AC ₆ to interrupt strobe enable output (ISE)		20	32	ns

NOTES:1. Typical values are for $T_A = 25^\circ\text{C}$ and 5.0 supply voltage

Microprogram Control Unit

N3001

VOLTAGE WAVEFORMS



WF10990S

N3002 Central Processing Element

Product Specification

Logic Products

FEATURES

- 45ns cycle time (typ)
- Easy expansion to multiple of 2 bits
- 11 general purpose registers
- Full function accumulator
- Useful functions include:
 - 2's complement arithmetic
 - Logical AND, OR, NOT, exclusive-NOR
 - Increment, decrement
 - Shift left/shift right
 - Bit testing and zero detection
 - Carry look-ahead generation
 - Masking via K-bus conditioned locking allowing non-destructive testing of data in accumulator and scratchpad
- 3 input buses
- 2 output buses
- Control bus

DESCRIPTION

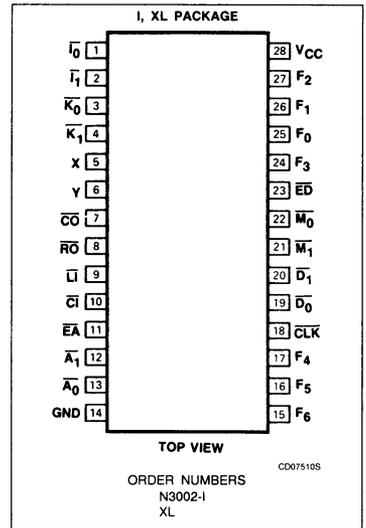
The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory.

FUNCTION TRUTH TABLE

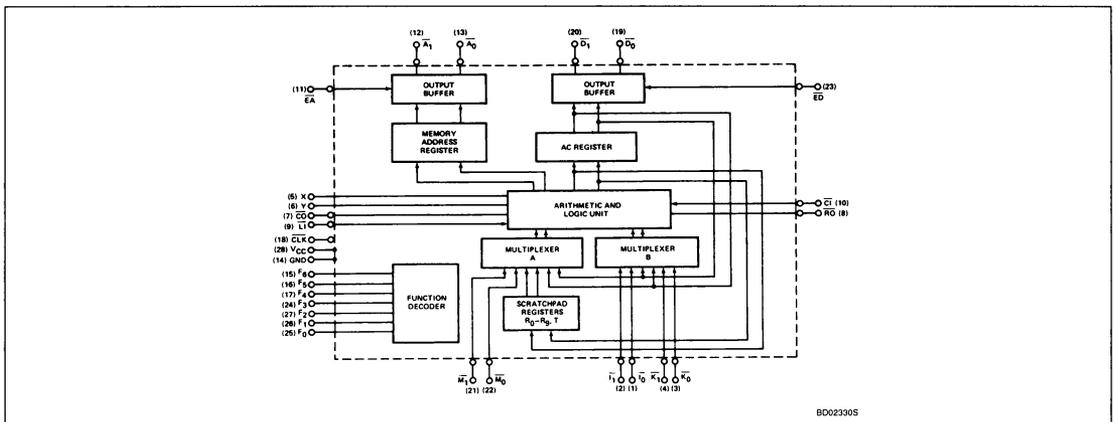
FUNCTION GROUP	F ₆	F ₅	F ₄
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F ₃	F ₂	F ₁	F ₀
I	R ₀	0	0	0	0
	R ₁	0	0	0	1
	R ₂	0	0	1	0
	R ₃	0	0	1	1
	R ₄	0	1	0	0
	R ₅	0	1	0	1
	R ₆	0	1	1	0
	R ₇	0	1	1	1
	R ₈	1	0	0	0
	R ₉	1	0	0	1
II	T	1	1	0	0
	AC	1	1	0	1
III	T	1	1	1	0
	AC	1	1	1	1

PIN CONFIGURATION



BLOCK DIAGRAM



Central Processing Element

N3002

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1, 2	$I_0 - I_1$	External Bus Input: The external bus inputs provide a separate input port for external input devices.	Active low
3, 4	$K_0 - K_1$	Mask Bus Inputs: The mask bus inputs provide a separate input port from the microprogram memory, to allow mask or constant entry	Active low
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs: The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator	Active high
7	CO	Ripple Carry Out: The ripple carry output is only disabled during shift right operations.	Active low Three-state
8	RO	Shift Right Output: The shift right output is only enabled during shift right operations.	Active low Three-state
9	LI	Shift Right Input	Active low
10	CI	Carry Input	Active low
11	EA	Memory Address Enable Input: When in the low state, the memory address enable input enables the memory address outputs ($A_0 - A_1$).	Active low
12 — 13	$A_0 - A_1$	Memory Address Bus Outputs: The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active low Three-state
14	GND	Ground	
14 — 17 24 — 27	$F_0 - F_6$	Micro-Function Bus Inputs: The micro-function bus inputs control ALU function and register selection.	Active high
18	CLK	Clock Input	
19 — 20	$D_0 - D_1$	Memory Data Bus Outputs: The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active low Three-state
21 — 22	$M_0 - M_1$	Memory Data Bus Inputs: The memory data bus inputs provide a separate input port for memory data.	Active low
23	ED	Memory Data Enable Input: When in the low state, the memory data enable input enables the memory data outputs ($D_0 - D_1$).	Active low
28	V_{CC}	+5 Volt Supply	

SYSTEM DESCRIPTION

Microfunction Decoder and K-Bus

Basic microfunctions are controlled by a 7-bit bus ($F_0 - F_6$) which is organized into 2 groups. The higher 3 bits ($F_4 - F_6$) are designated as F-Group and the lower 4 bits ($F_0 - F_3$) are designated as the R-Group. The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

The F-Bus instructs the microfunction decoder to:

- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:

- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction

- Bit masking
- Maintain program counter

A and B Multiplexers

A and B multiplexers select the proper 2 operands to the ALU.

A multiplexer selects inputs from one of the following:

- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:

- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

Scratchpad Registers

- Contains 11 registers ($R_0 - R_9, T$)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations

- Can be used as program counter

Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:

- 2's complement addition
- Incrementing
- Decrementing
- Shift left
- Shift right

Logical operations are:

- Transfer
- AND
- Inclusive-OR
- Exclusive-NOR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays carry look-ahead outputs (X and Y) and cascading shift inputs (LI, RO) are provided.

Central Processing Element

N3002

Accumulator

- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

Input Buses

M-bus: Data bus from main memory

- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus: Data bus from input/output devices

Accepts 2 bits of data from external input/output devices into CPE

- Is multiplexed into the ALU via the B multiplexer

K-bus: A special feature of the N3002 CPE

- During arithmetic operations, the K-bus can be used to **mask** portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

Output Buses

A-bus and Memory Address Register

- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/O instructions
- A-bus has Tri-State outputs

D-bus: Data bus from CPE to main memory or to I/O devices

- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I	XX	—	$R_n + (AC\ K) + CI \rightarrow R_n, AC$	Logically AND AC with K-bus. Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n .
		OO	ILR	$R_n + CI \rightarrow R, AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the results in AC.
		11	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	—	$M + (AC\ K) + CI \rightarrow AT$	Logically AND AC with the K-bus. Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AM + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	—	$AT_L \vee (\overline{LI} \wedge K_L) \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)]$ $[AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO$ $AT_H \rightarrow AT_L$ $L_I \rightarrow AT_H$	
1	I	XX	—	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	Logically OR R_n with the K-bus. Deposit the result in MAR. Add the K-bus to R_n and CI. Deposit the result in R_n .
		OO	LMI	$R_n \rightarrow MAR, R_n + CI \rightarrow R_n$	Load MAR to R_n . Conditionally increment R_n . Used to maintain a macro-instruction program counter.
		11	DSM	$11 \rightarrow MAR, R_n - 1 + CI \rightarrow R_n$	Set MAR to all ones. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement R_n .
1	II	XX	—	$K \vee M \rightarrow MAR$ $M + K + CI \rightarrow AT$	Logically OR the M-bus with the K-bus. Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR, M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		11	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.

Central Processing Element

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FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
1	III	XX	—	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	Logically OR the K-bus with the complement of AC or T, as specified. Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		11	DCA	$\overline{AT} - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	—	$(AC \wedge K) - 1 + CI \rightarrow R_n$	Logically AND the K-bus with AC. Subtract one from the result and add the difference to CI. Deposit the sum in R_n .
		OO	CSR	$CI - 1 \rightarrow R_n$ (See Note 1)	Subtract one from CI and deposit the difference in R_n . Used to conditionally clear or set R_n to all 0's or 1's, respectively.
		11	SDR	$AC - 1 + CI \rightarrow R_n$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in R_n . Used to store AC in R_n , or to store the decremented value of AC in R_n .
2	II	XX	—	$(AC \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	Logically AND the K-bus with AC. Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ (See Note 1)	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	SDA	$AC - 1 + CI \rightarrow AT$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.
2	III	XX	—	$(I \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	Logically AND the data of the K-bus with the data on the I-bus. Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	LDI	$I - 1 + CI \rightarrow AT$	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n$	Logically AND AC with the K-bus. Add R_n and CI to the result. Deposit the sum in R_n .
		OO	INR	$R_n + CI \rightarrow R_n$	Add CI to R_n and deposit the sum in R_n . Used to increment R_n .
		11	ADR	$AC + R_n + CI \rightarrow R_n$	Add AC to R_n . Add the result to CI and deposit the sum in R_n . Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.
3	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	Logically AND AC with the K-bus. Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.

Central Processing Element

N3002

FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
3	III	XX	—	$AT + (I \wedge K) + CI \rightarrow AT$	Logically AND the K-bus with the I-bus. Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	$AT + CI \rightarrow AT$	Conditionally increment AC or T. Used to increment AC or T.
		11	AIA	$I + AT + CI \rightarrow AT$	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.
4	I	XX	—	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \wedge (AC \wedge K) \rightarrow R_n$	Logically AND the K-bus with AC. Logically AND the result with the contents of R_n . Deposit the final result in R_n . Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
		OO	CLR	$CI \rightarrow CO, O \rightarrow R_n$	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	ANM	$CI \vee (R_n \wedge AC) \rightarrow CO$ $R_n \wedge AC \rightarrow R_n$	Logically AND AC with R_n . Deposit the result in R_n . Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	—	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \wedge (AC \wedge K) \rightarrow AT$	Logically AND the K-bus with AC. Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO, O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \wedge AC \rightarrow AT$	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND the M-bus data to the accumulator and test for a zero result.
4	III	XX	—	$CI \vee (AT \wedge 1 \wedge K) \rightarrow CO$ $AT \wedge (1 \wedge K) \rightarrow AT$	Logically AND the I-bus with the K-bus. Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO, O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANI	$CI \vee (AT \wedge 1) \rightarrow CO$ $AT \wedge 1 \rightarrow AT$	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	—	$CI \vee (R_n \wedge K) \rightarrow CO$ $K \wedge R_n \rightarrow R_n$	Logically AND the K-bus with R_n. Deposit the result in R_n . Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLR	$CI \rightarrow CO, O \rightarrow R_n$	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	TZR	$CI \vee R_n \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to one if R_n is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	—	$CI \vee (M \wedge K) \rightarrow CO$ $K \wedge M \rightarrow AT$	Logically AND the K-bus with the M-bus. Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO, O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	LTM	$CI \vee M \rightarrow CO$ $M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.

Central Processing Element

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FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
5	III	XX	—	$CI \vee (AT \wedge K) \rightarrow CO$ $K \wedge AT \rightarrow AT$	Logically AND the K-bus with AC or T, as specified. Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO, O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	TZA	$CI \vee AT \rightarrow CO$ $AT \rightarrow AT$	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.
6	I	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $R_n \vee (AC \wedge K) \rightarrow R_n$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n .
		OO	NOP	$CI \rightarrow CO, R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORR	$CI \vee AC \rightarrow CO$ $R_n \vee AC \rightarrow R_n$	Force CO to one if AC is non-zero. Logically OR AC with R_n . Deposit the result in R_n . Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $M \vee (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	$CI \rightarrow CO, M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		11	ORM	$CI \vee AC \rightarrow CO$ $M \vee AC \rightarrow AT$	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	—	$CI \vee (I \wedge K) \rightarrow CO$ $AT \vee (I \wedge I) \rightarrow AT$	Logical OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	$CI \rightarrow CO, AT \rightarrow AT$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORI	$CI \vee I \rightarrow CO$ $I \vee AT \rightarrow$	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC to T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.
7	I	XX	—	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \oplus (AC \vee K) \rightarrow R_n$	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n . Deposit the final result in R_n .
		OO	CMR	$CI \rightarrow CO, R_n \rightarrow R_n$	Complement the contents of R_n . Force CO to CI.
		11	XNR	$CI (R_n \vee AC) \rightarrow CO$ $R_n \oplus AC \rightarrow R_n$	Force CO to one if the logical AND of AC and R_n is non-zero. Exclusive-NOR AC with R_n . Deposit the result in R_n . Used to exclusive-NOR the accumulator with a register.

Central Processing Element

N3002

FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	II	XX	—	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \oplus (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	$CI \rightarrow CO, \bar{M} \rightarrow AT$	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		11	XNM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \oplus AC \rightarrow AT$	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	—	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$ $AT \oplus (I \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	$CI \rightarrow CO, \bar{AT} \rightarrow AT$	Complement AC or T, as specified. Force CO. to CI.
		11	XNI	$CI \vee (AT \wedge I) \rightarrow CO$ $I \oplus AT \rightarrow AT$	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

NOTE:

2's complement arithmetic adds 111 ... 11 to perform subtraction of 000 ... 01.

FUNCTION DESCRIPTION KEY

SYMBOL	MEANING
I, K, M	Data on the I, K, and M buses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R _n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L, H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
-	2's complement subtraction
^	Logical AND
v	Logical OR
⊕	Exclusive-NOR
→	Deposit into

Central Processing Element

N3002

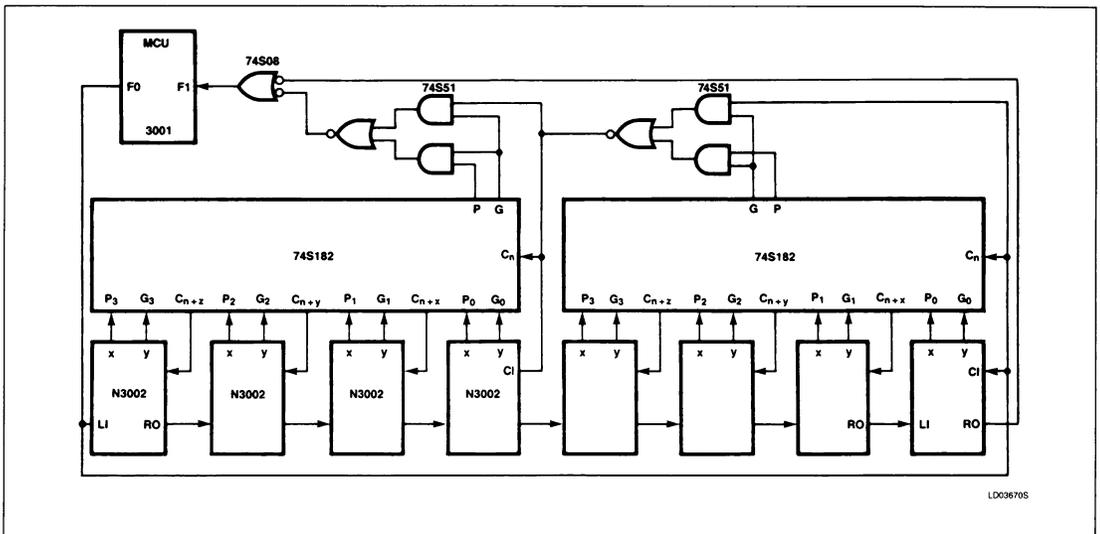
AC ELECTRICAL CHARACTERISTICS $N3001 = T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$

PARAMETER		N3002			UNIT
		Min	Typ*	Max	
tCY	Clock cycle time	70	45		ns
tWP	Clock pulse width	17	10		ns
tFS	Function input set-up time (F_0 through F_6)	48	-23 → 35		ns
Data set-up time:					
tDS	$I_0, I_1, M_0, M_1, K_0, K_1$	40	12 → 29		ns
tSS	L_i, Cl	21	0 → 7		30
Data and function hold time:					
tFH	F_0 through F_6	4	0		ns
tDH	$I_0, I_1, M_0, M_1, K_0, K_1$	4	-28 → -11		ns
tSH	L_i, Cl	12	-7 → 0		ns
Propagation Delay to X, Y, RO from:					
tXF	Any Function Input		28	52	ns
tXD	Any Data Input		16 → 20	33	ns
tXT	Trailing Edge of CLK		33	48	ns
tXL	Leading Edge of CLK	13	18 → 40	70	ns
Propagation delay to CO from:					
tCL	Leading Edge of CLK	16	25 → 44	70	ns
tCL	Trailing Edge of CLK		30 → 40	56	ns
tCF	Any Function Input		25 → 35	52	ns
tCD	Any Data Input		17 → 23	55	ns
tCC	Cl (Ripple Carry)		9 → 13	20	ns
Propagation delay to A_0, A_1, D_0, D_1 from:					
tDL	Leading Edge of CLK		17 → 25	40	ns
tDE	Enable Input ED, EA		10 → 12	20	ns

***NOTE:**

Typical values are for $T_A = 25^\circ\text{C}$ and typical supply voltage.

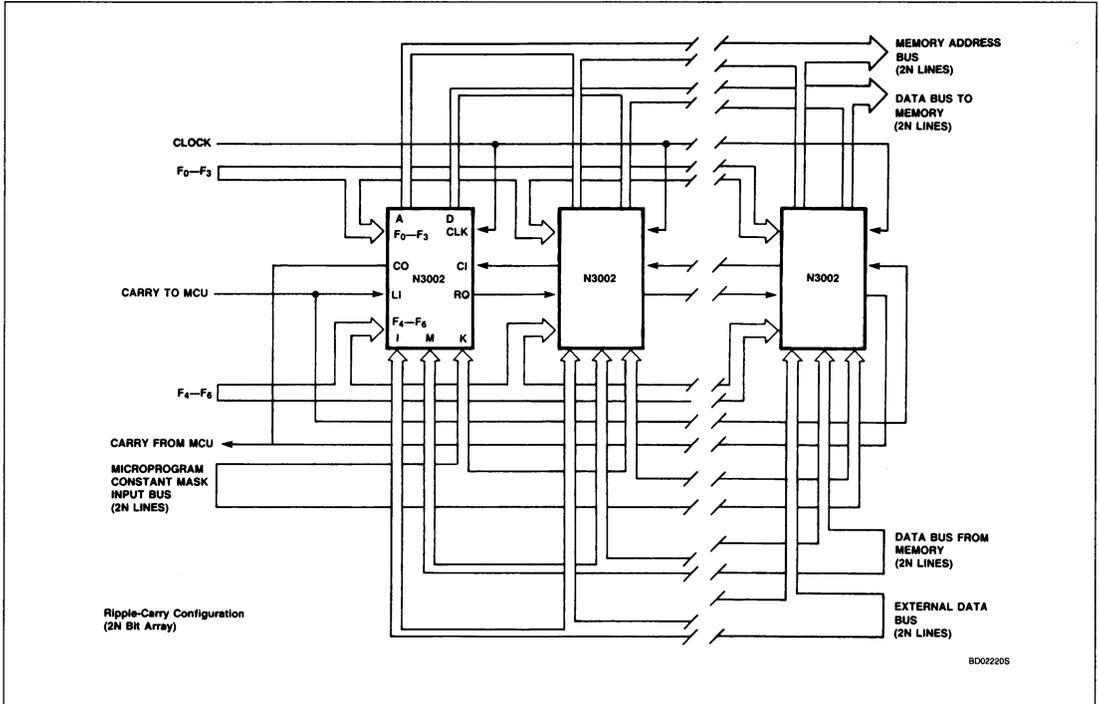
CARRY LOOK-AHEAD CONFIGURATION



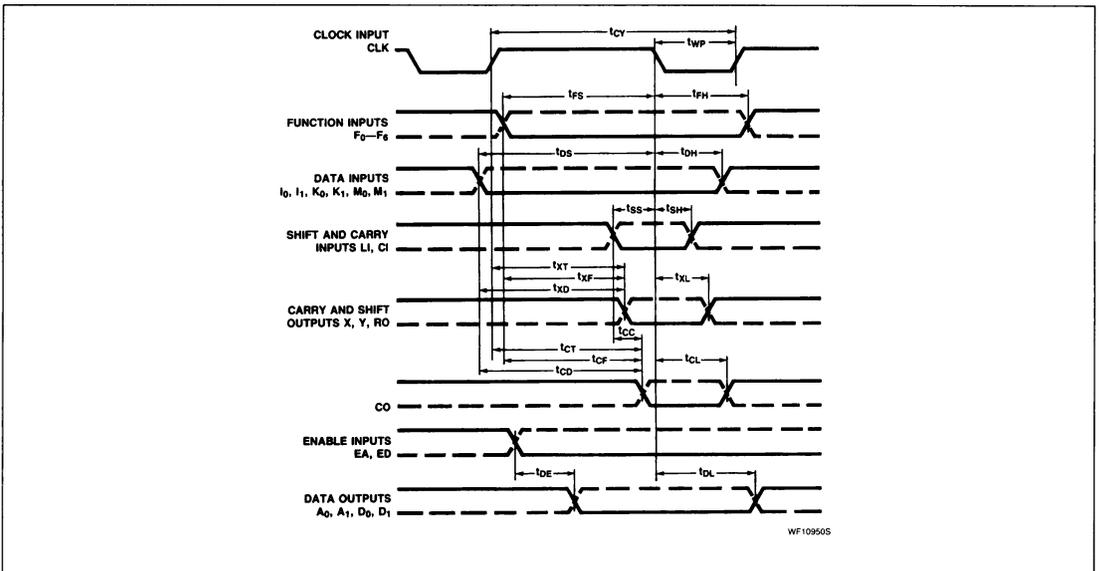
Central Processing Element

N3002

TYPICAL CONFIGURATIONS



VOLTAGE WAVEFORMS



7

9403 64-Bit FIFO Buffer Memory

Product Specification

Logic Products

FEATURES

- 10MHz Serial or Parallel Data Rate
- Serial or Parallel Input and Output
- Expandable Without External Logic
- Three-State Outputs
- Fully TTL-Compatible
- Slim (0.4 In.) 24-Pin DIP

PRODUCT DESCRIPTION

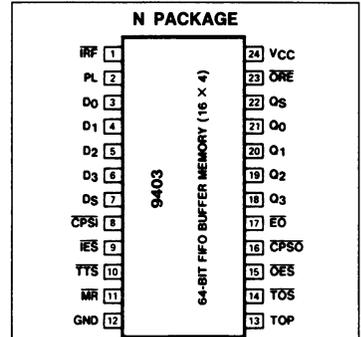
The 9403 is an expandable fall-through type First-In-First-Out (FIFO) Buffer Memory that is optimized for high-speed disc/tape controllers and communication-buffer applications. In multiples of four, the device can be expanded to any number of bits and subsequently, to any number of words. Serial or parallel data can be asynchronously entered or retrieved which makes the 9403 the cost-effective solution for implementing buffer memories.

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the 9403 consists of three parts which operate asynchronously and are virtually independent. These parts are:

- **Input Register** — with serial and parallel data inputs and control signals that permit easy expansion and a handshake interface.
- **FIFO Stack** — 4-bit wide, 14-word deep fall-through type with self-contained control logic.
- **Output Register** — with serial and parallel data outputs and control signals that permit easy expansion and a handshake interface.

PIN DESIGNATIONS & DESCRIPTIONS



ORDER NUMBER

N9403N

MNEMONIC AND FUNCTION	DESCRIPTION
IRF	Input register full output Low when input register is full
PL	Parallel load input High on PL enables $D_0 - D_3$; not edge-triggered, 1's catching
$D_0 - D_3$	Parallel data input
D_S	Serial data input
CPSI	Serial input clock Edge-triggered and activates on falling edge
IES	Serial input enable When low, serial input is enabled
TTS	Transfer to stack input When low, initiates fall-through
MR	Master Reset Active low
TOP	Transfer out parallel input When high and TOS is low, enables word transfer from stack to output register — not edge-triggered
TOS	Transfer out serial input When low and TOP is high, enables word transfer from stack to output register — not edge-triggered
OES	Serial output enable input When low, enables serial output
CPSO	Serial output clock input Edge-triggered and activates on falling edge
EO	Output enable Active low
$Q_0 - Q_3$	Parallel data output
Q_S	Serial data output
ORE	Output register empty output When high, output register contains valid data
GND	Ground
VCC	Supply voltage + 5 volts

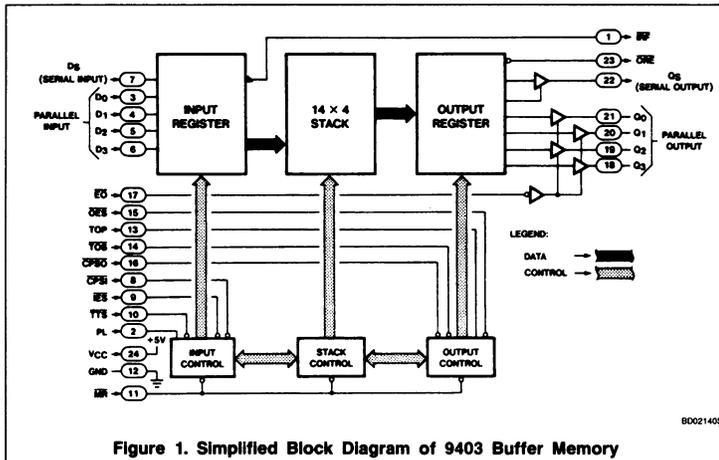


Figure 1. Simplified Block Diagram of 9403 Buffer Memory

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64-Bit FIFO Buffer Memory

9403

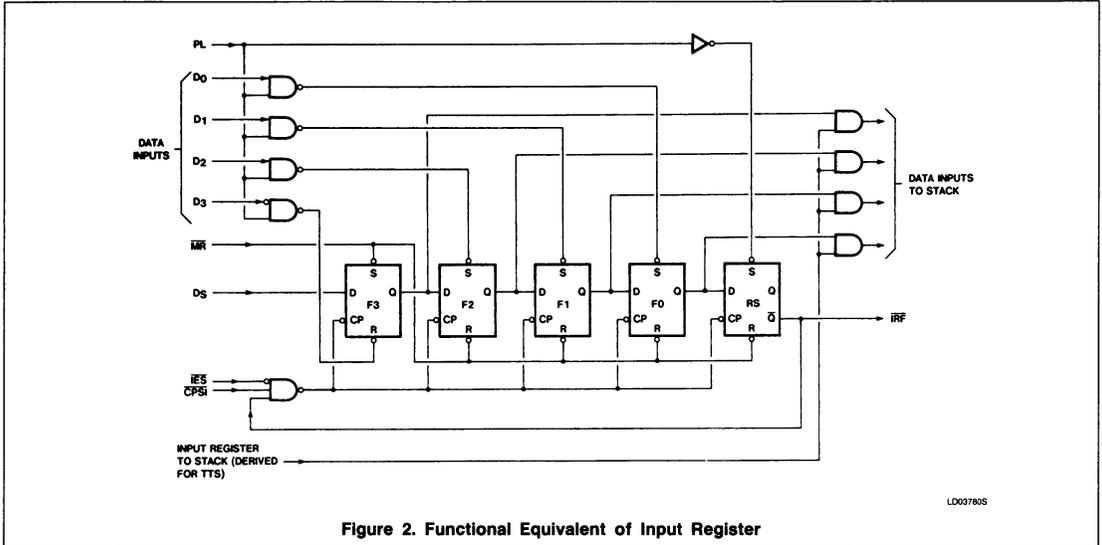


Figure 2. Functional Equivalent of Input Register

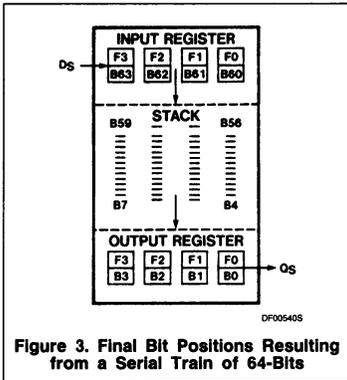


Figure 3. Final Bit Positions Resulting from a Serial Train of 64-Bits

INPUT REGISTER

Data can be entered serially or, using the parallel mode of operation, data is entered in 4-bit increments. In either case, the data is subsequently transferred to the fall-through stack; the functional equivalent of this register is shown in Figure 2. The Input Register Full (IRF) status signal is internally generated by the Register Status (RS) flip-flop; when initialized, the Q (IRF) output of this flip-flop is high.

Serial Entry (Input Register)

Serial data is entered via the D_S input and is handled by a 5-bit shift register consisting of flip-flops F3, F2, F1, F0, and RS. With IES and PL both low, each high-to-low transition of the serial input clock (CPS) shifts the input data in domino order from F3 to F2 to F1 to F0. After the fourth clock transition, the four bits of serial data are aligned in F3 through F0 and RS is set, forcing IRF low and inhibiting

CPS until contents of the input register are transferred to the stack. Figure 3 shows how a serial train of 64-bits would appear in the 9403 — four bits (B60 – B63) in the input register, 56 bits (B4 – B59) in the stack, and four bits (B0 – B3) in the output register.

Parallel Entry (Input Register)

When PL is high and CPS is low (Figure 2), flip-flops F0 – F3 are loaded with data and IRF is forced low. This condition remains until current data is transferred to the stack. Once the data is transferred, IRF is driven high and new data can again be clocked into the input flip-flops. If parallel expansion is not being implemented, IES must be low to establish row mastership — refer to discussion of parallel expansion.

STACK OPERATION

As shown in Figure 2, the outputs of F0 – F3 are applied to the stack under control of a signal derived from TTS. When TTS is low, an attempt to initiate a fall-through action is made. If the top location of stack is empty, data is loaded and the input register is re-initialized provided PL is low. Note that initialization is postponed until PL is again low. Thus, automatic FIFO action is achieved by connecting the TTS input to the IRF output.

The RS flip-flop (Figure 2) records the fact that data has been transferred to the stack; this flip-flop is not cleared until PL goes low. Therefore, if a particular data word is transferred to the stack and falls to the second location before PL goes low, the same word will not be re-transferred even though IRF and TTS are still low. Once data enters the stack, "fall-through" is automatic; a delay is

necessary only when waiting for the next stack location to empty. In the 9403, as in most modern FIFO designs, the MR input initializes the stack control section and does not clear the data.

OUTPUT REGISTER

This register receives and stores 4-bits of data from the bottom stack location and, on demand, outputs data onto a three-state 4-bit parallel data bus or a three-state serial data bus. The Output Register Full (ORE) status signal is internally-generated by the FX flip-flop; when data is transferred from the stack to the output register, ORE goes high. The functional equivalent of the output register is shown in Figure 4.

Retrieval of Serial Data

When the FIFO stack is empty and MR is driven low, the ORE output goes low to indicate that the output register is ready to accept new data from the stack. After new data is entered and falls through to the bottom stack location, it is transferred to the output register provided TOS is low and TOP is high. As a result of the data transfer, ORE goes high indicating valid data in the output register. Subsequently, the QS output is automatically enabled and the first data bit is transmitted to the three-state serial data bus. Henceforth, a serial shift of data occurs on each high-to-low transition of CPS. On the fourth transition, the register is emptied, ORE is forced low, and serial output QS is disabled. To request a new word from the stack, the TOS input can be connected to the ORE output.



64-Bit FIFO Buffer Memory

9403

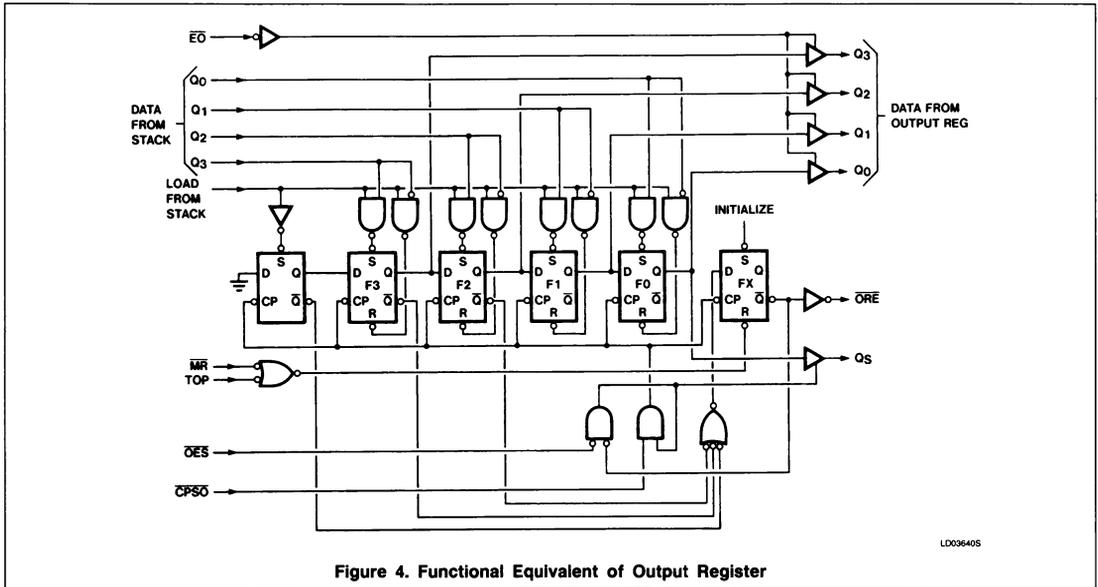


Figure 4. Functional Equivalent of Output Register

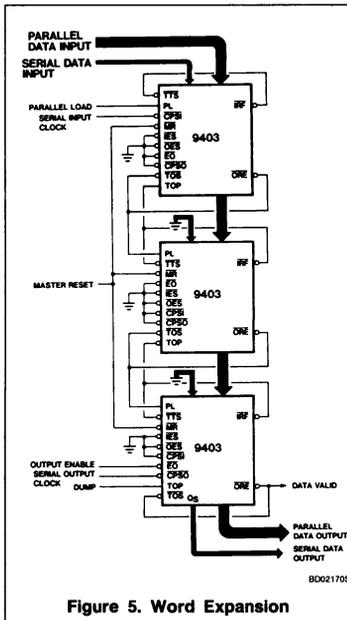


Figure 5. Word Expansion

Retrieval of Parallel Data

With the stack empty and MR in the active-low state, the ORE output goes low, signifying that the output register is also empty. When

new data is entered and has fallen through to bottom location of the stack, it is automatically transferred to the output register, provided the Transfer Out Parallel (TOP) input is high. When the data is transferred from stack-to-register, ORE goes high and valid data appears at Q₀ - Q₃ (Figure 4), provided the three-state buffers are enabled, that is, EOE is active-low. When TOP goes low, ORE is driven low which indicates that the data output cycle is complete; however, the original data remains latched in the flip-flops until the next word (if available) is transferred from the stack to the output register.

For parallel operation, CPSO must be low, whereas, TOS should be grounded for single-slice operation or connected to the appropriate ORE for expanded operation. The TOP input is not edge-triggered; therefore, if it goes high before data is available from stack but data becomes available before it goes low, the data will be transferred to the output register. However, internal control circuits prevent the same data from being transferred twice. If TOP goes high and returns to low before data is available from the stack, ORE will remain low, indicating the absence of valid output data.

VERTICAL EXPANSION

In a vertical structure, the 9403 can be expanded to achieve greater word capacity

without any external parts; a 46-word by 4-bit FIFO is shown in Figure 5. Using the same technique and similar connections, any FIFO of 15n + 1 words (where n is the number of devices) can be constructed. Observe that word expansion does not sacrifice flexibility of the 9403 FIFO as regards serial/parallel input and output.

HORIZONTAL EXPANSION

The 9403 can be horizontally expanded to store long words in multiples of 4-bits, again without external logic. Connections required to form a 16-word by 12-bit FIFO are shown in Figure 6, using similar techniques, any 16-word by 4n-bit FIFO (where n is the number of devices) can be constructed.

For horizontal or bit expansion, it is good practice to connect, respectively, the IRF and ORE outputs of the right-most device (most significant device) to the TTS and TOS inputs of all devices to the left (least significant devices) to guarantee that no operation is initiated before each and every device is ready. Word expansion does not affect the ability of the 9403 to handle serial/parallel inputs and outputs; however, the ripple form of expansion shown in Figure 6 does extract a penalty in speed of operation. Whereas a single 9403 is guaranteed to operate at 10MHz, an array of four FIFOs connected as shown is guaranteed to operate at 4.3MHz.

64-Bit FIFO Buffer Memory

9403

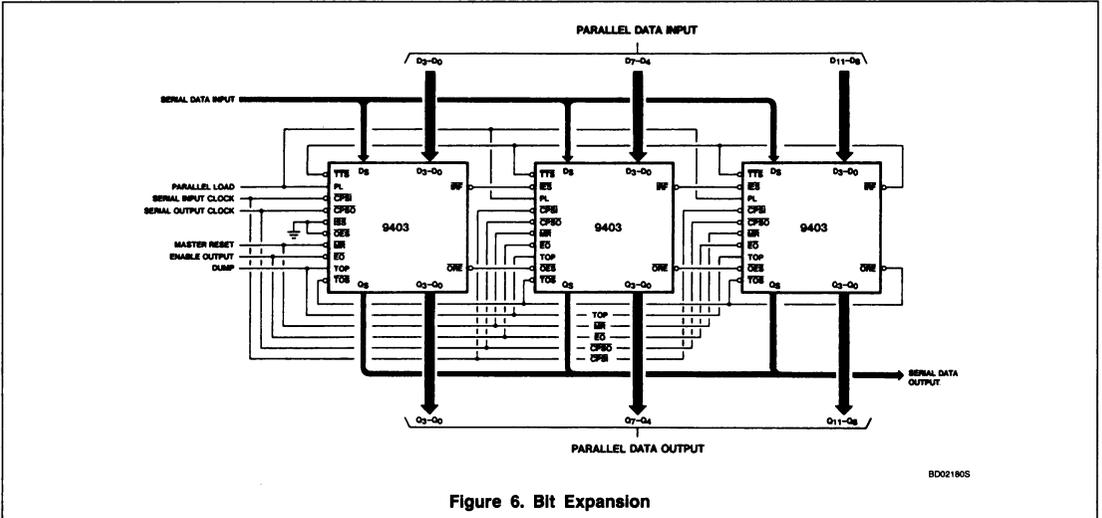
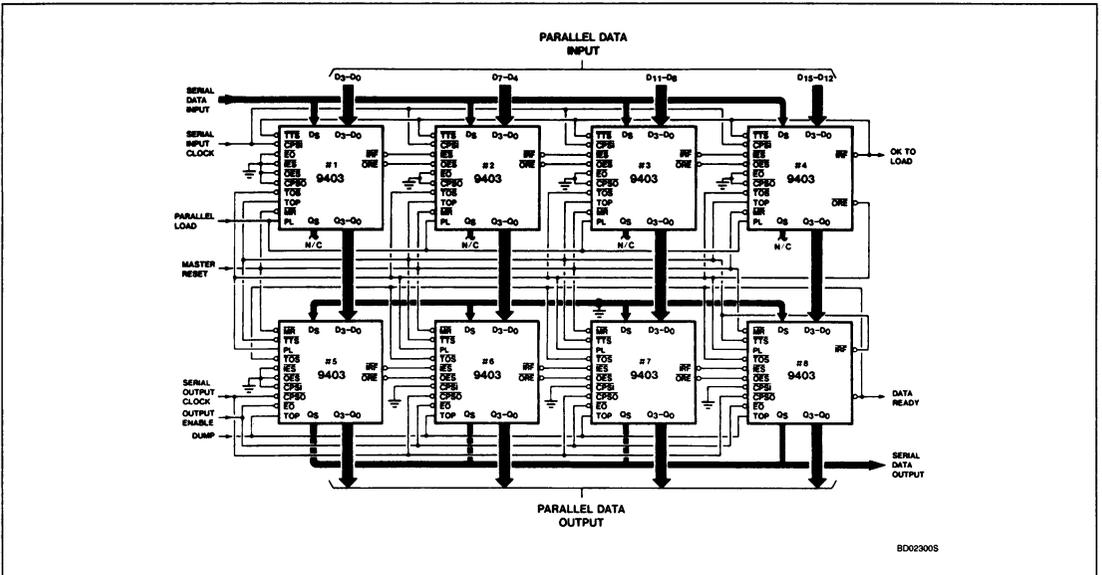


Figure 6. Bit Expansion



7

INPUT REGISTER	UNIT NUMBER & ORDER OF SERIAL BITS				OUTPUT REGISTER	UNIT NUMBER & ORDER OF SERIAL BITS			
	#1	#2	#3	#4		#5	#6	#7	#8
D ₃	BIT 483	BIT 487	BIT 491	BIT 495	Q ₃	BIT 3	BIT 7	BIT 11	BIT 15
D ₂	482	486	490	494	Q ₂	2	6	10	14
D ₁	481	485	489	493	Q ₁	1	5	9	13
D ₀	480	484	488	492	Q ₀	0	4	8	12

Figure 7. Horizontal and Vertical Expansion — 31 × 16 FIFO

64-Bit FIFO Buffer Memory

9403

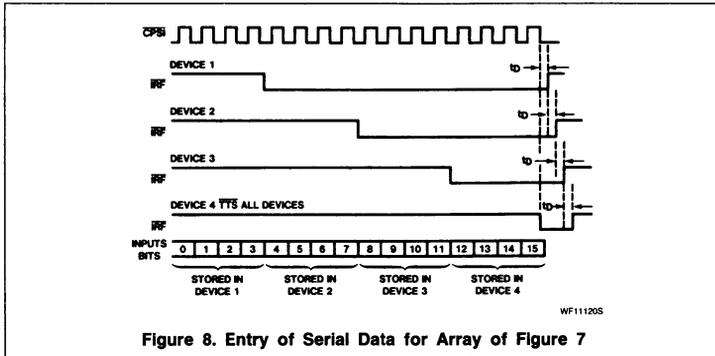


Figure 8. Entry of Serial Data for Array of Figure 7

HORIZONTAL AND VERTICAL EXPANSION

In addition to bit-or-word expansion, the 9403 can be used to expand in both the horizontal and vertical directions; a 31-word by 16-bit FIFO is shown in Figure 7. Using the same or similar techniques, any FIFO of $15m + 1$ words by $4n$ -bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row.

The chart appended to Figure 7 shows the final positions for a contiguous serial entry of 496 bits. Figures 8 and 9, respectively, show the timing relationships involved for data-entry and data-retrieval pertaining to the 31-word by 16-bit array.

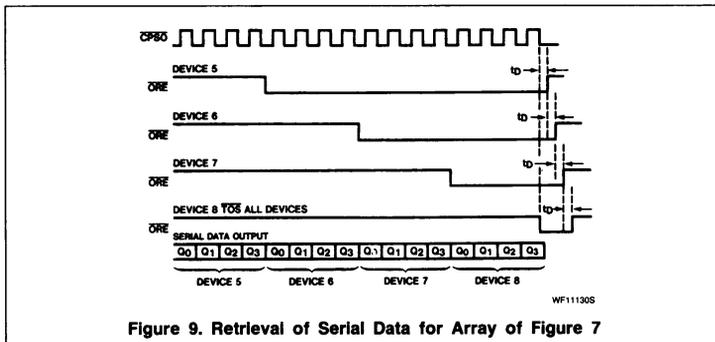


Figure 9. Retrieval of Serial Data for Array of Figure 7

INTERLOCKING CIRCUITS

Most conventional FIFO designs provide the status-signal counterparts of IRF and ORE. However, when these devices are used in arrays, variations in unit-to-unit operating speeds require the use of external gating to ensure that all devices have, in fact, completed the last operation. The 9403 incorporates simple but effective master/slave interlocking circuits to eliminate these gating requirements.

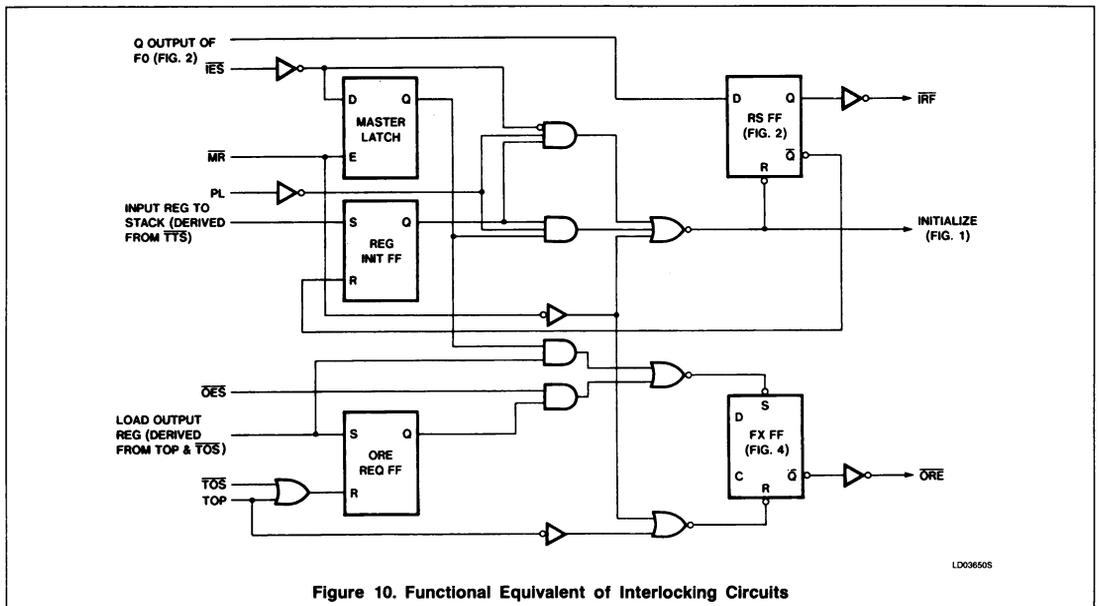


Figure 10. Functional Equivalent of Interlocking Circuits

64-Bit FIFO Buffer Memory

9403

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} Power supply voltage	+7	Vdc
V_{IN} Input voltage	+5.5	Vdc
V_O Off-state output voltage	+5.5	Vdc
T_A Operating temperature range	0 to +70	°C
T_{stg} Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS Over operating temperature range unless otherwise noted

PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
		Min	Typ	Max	
V_{IH} Input high voltage	Guaranteed input high voltage	2.0			V
V_{IL} Input low voltage	Guaranteed input low voltage			0.8	V
V_{CD} Input clamp diode voltage	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$		-0.9	-1.5	V
V_{OH} Output high voltage, $\overline{ORE}, \overline{IRF}$	$V_{CC} = \text{MIN}, I_{OH} = -400\mu\text{A}$	2.4	3.4		V
V_{OH} Output high voltage, $Q_0 - Q_3, Q_S$	$I_{OH} = -5.7\text{mA}, V_{CC} = \text{MIN}$	2.4	3.1		V
V_{OL} Output low voltage, $Q_0 - Q_3, Q_S$	$V_{CC} = \text{MIN}, I_{OL} = 16\text{mA}$		0.35	0.5	V
V_{OL} Output low voltage, $\overline{ORE}, \overline{IRF}$	$V_{CC} = \text{MIN}, I_{OL} = 8.0\text{mA}$		0.35	0.5	V
I_{OZH} Output off current high, $Q_0 - Q_3, Q_S$	$V_{CC} = \text{MAX}, V_{OUT} = 2.4\text{V}, V_E = 2\text{V}$			100	μA
I_{OZL} Output off current low, $Q_0 - Q_3, Q_S$	$V_{CC} = \text{MAX}, V_{OUT} = 0.5\text{V}, V_E = 2\text{V}$			-100	μA
I_{IH} Input high current	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$ $V_{CC} = \text{MAX}, V_{IN} = 5.5\text{V}$		1.0	40 1.0	μA mA
I_{IL} Input low current, all except \overline{OES} & \overline{IES}	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$			-0.36 -0.96	mA
I_{OS} Output short circuit current, $Q_0 - Q_3, Q_S, \overline{ORE}, \overline{OES}$	$V_{CC} = \text{MAX}, V_{OUT} = 0, (\text{Note } 3)$	-30		-130	mA
I_{CC} Supply Current	$V_{CC} \text{ MAX}, \text{Inputs open}$		115	170	mA

NOTES:

- Operating temperature ranges are guaranteed after terminal equilibrium has been reached.
- All voltages measured with respect to ground terminal.
- No more than one output should be shorted at a time.

64-Bit FIFO Buffer Memory

9403

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V, C_L = 15pF, T_A = 25^\circ C$

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS ^{1, 2, 3}	LIMITS			UNIT
				Min	Typ	Max	
Fall-through time: t_{DFT}	Positive going PL	$Q_0 - Q_3$	\overline{TTS} connected to \overline{IRF} , \overline{TOS} connected to \overline{ORE} , IES, OES, EO, \overline{CPSO} low. TOP high (f, Fig. 11)		450	600	ns
Propagation delay t_{PLH} Low-to-high t_{PHL} High-to-low	Negative going \overline{TTS} Negative going \overline{CPSI}	\overline{IRF} \overline{IRF}	Stack not full. PL low (a & b, Fig. 11)		48 18	64 25	ns
t_{PLH} Low-to-high t_{PHL} High-to-low	Negative going \overline{CPSO}	Q_5	Serial output \overline{OES} low. TOP high (c & d, Fig. 11)		30 17	40 28	ns
t_{PHL} High-to-low	Negative going \overline{CPSO}	\overline{ORE}				32	42
t_{PLH} Low-to-high t_{PHL} High-to-low	Positive going TOP	$Q_0 - Q_3$	\overline{EO} , \overline{CPSO} low (e, Fig 11)		40 31	56 45	ns
t_{PLH} Low-to-high t_{PHL} High-to-low	Positive going TOP Negative going TOP	\overline{ORE} \overline{ORE}	Parallel output. \overline{EO} , \overline{CPSO} low (e, Fig. 11)		51 40	68 54	ns
t_{PLH} Low-to-high	Negative going \overline{TOS}	Positive going \overline{ORE}	Data in stack. TOP high, (c & d, Fig. 11)		41	56	ns
t_{PHL} High-to-low	Positive going PL	Negative going \overline{IRF}	Stack not full (g & h, Fig. 11)		20	33	ns
t_{PLH} Low-to-high t_{PLH} Low-to-high t_{PLH} Low-to-high	Negative going PL Positive going OES Positive going IES	Positive going \overline{IRF} \overline{ORE} Positive going \overline{IRF}			33 26 31	46 44 40	ns
Enable delay: t_{PZH} High t_{PZL} Low	\overline{EO}	$Q_0 - Q_3$	Out of high impedance state		9	14 20	ns
t_{PZL} Low t_{PZH} High	Negative going \overline{OES}	Q_5				13	25 20
Disable delay: t_{PLZ} Low t_{PZH} High	\overline{EO}	$Q_0 - Q_3$	Into high impedance state		7	14	ns
t_{PLZ} Low t_{PHZ} High	Negative going \overline{OES}	Q_5				7	14
Appearance time: t_{AP} Parallel t_{AS} Serial	\overline{ORE} \overline{ORE}	$Q_0 - Q_3$ Q_5	Time elapsed between \overline{ORE} going high and valid data appearing at output, negative number indicates data available before \overline{ORE} goes high		-12 6	-5 10	ns
Pulse width: t_{PWL} \overline{CPSI} low t_{PWH} \overline{CPSI} high			Stack not full. PL low (a & b, Fig. 11)		20 33	11 19	ns
t_{PWL} TOP low t_{PWH} TOP high			\overline{CPSO} low, data available in stack (e, Fig. 11)		30 26	17 13	ns
t_{PWL} \overline{CPSO} low t_{PWH} \overline{CPSO} high			TOP high, data in stack, (c & d, Fig. 11)		30 32	16 18	ns
t_{PWH} PL high			Stack not full (g & h, Fig. 11)		40	29	ns
t_{PWL} \overline{TTS} low (serial or parallel mode)			Stack not full (a, b, g, & h, Fig. 11)		20	9	ns
t_{PWL} \overline{MR} low			(f, Fig. 11)		25	13	ns

64-Bit FIFO Buffer Memory

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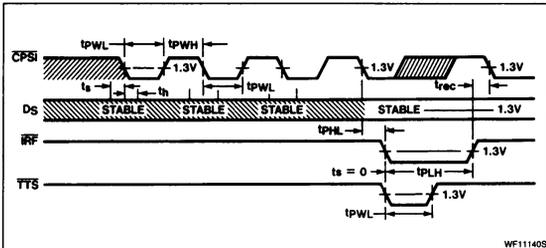
AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V, C_L = 15pF, T_A = 25^\circ C$ (Cont.)

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS ^{1, 2, 3}	LIMITS			UNIT
				Min	Typ	Max	
Set-up and hold time: t_s Set-up time t_h Hold time	D_S D_S	Negative $\overline{CP}SI$ $\overline{CP}SI$	PL low (a & b, Fig. 11)	28 0	17 -6		ns
t_s Set-up time	Parallel inputs	PL	Length of time parallel inputs must be applied prior to rising edge of PL	0	-22		ns
t_h Hold time	Parallel inputs	PL	Length of time parallel inputs must remain applied after falling edge of PL	2			ns
t_s Set-up time (serial or parallel mode)	$\overline{T}TS$	$\overline{I}RF$	(a, b, g, & h, Fig. 11)	0	-20		ns
t_s Set-up time	Negative going $\overline{O}RE$	Negative going $\overline{T}OS$	TOP high (c & d, Fig. 11)	0	-24		ns
t_s Set-up time t_s Set-up time	Negative going $\overline{I}ES$ Negative $\overline{T}TS$	$\overline{CP}SI$ $\overline{CP}SI$	(b, Fig. 11)	45 84	23 58		ns
Recovery time: t_{rec}	$\overline{M}R$	Any input	(f, Fig. 11)	15	5		ns

NOTES:

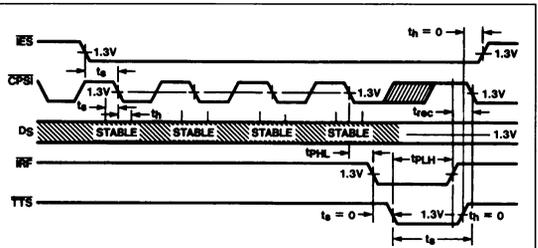
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{T}TS$ normally connected to $\overline{I}RF$.
3. If stack is full, $\overline{I}RF$ will stay low.

TEST CIRCUITS AND WAVEFORMS



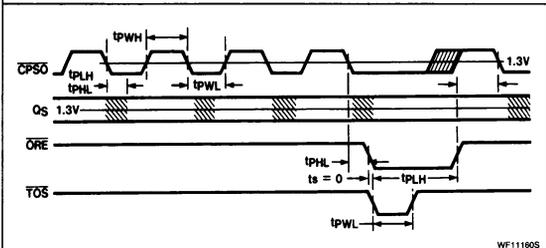
CONDITIONS:
Stack Not Full, $\overline{I}ES$, PL Low

a. Serial Input, Unexpanded or Master Operation



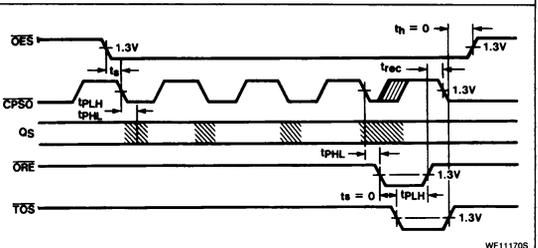
CONDITIONS:
Stack Not Full, $\overline{I}ES$ High When Initialized, PL Low

b. Serial Input, Expanded Slave Operation



CONDITIONS:
Data in Stack, Top High, $\overline{I}ES$ Low When Initialized, $\overline{O}ES$ Low

c. Serial Output, Unexpanded or Master Operation



CONDITIONS:
Data in Stack, Top High, $\overline{I}ES$ High When Initialized

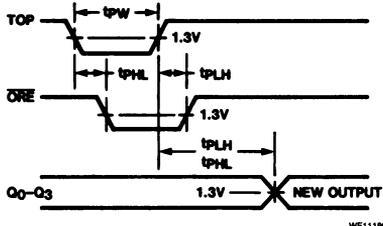
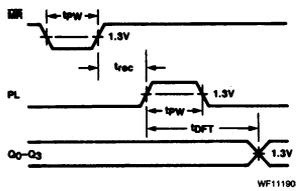
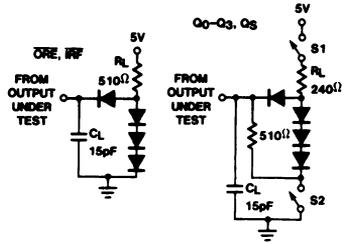
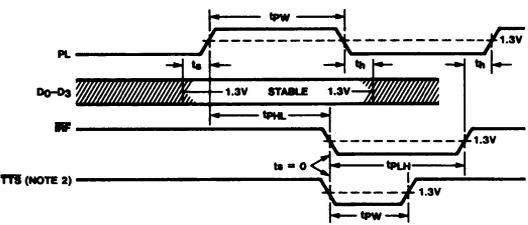
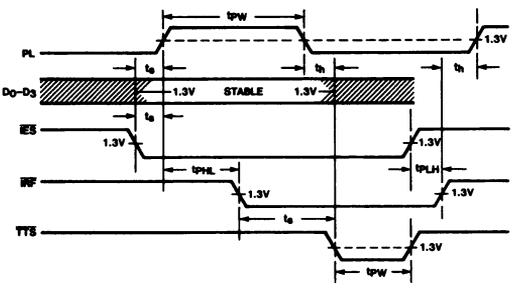
d. Serial Output, Slave Operation

7

64-Bit FIFO Buffer Memory

9403

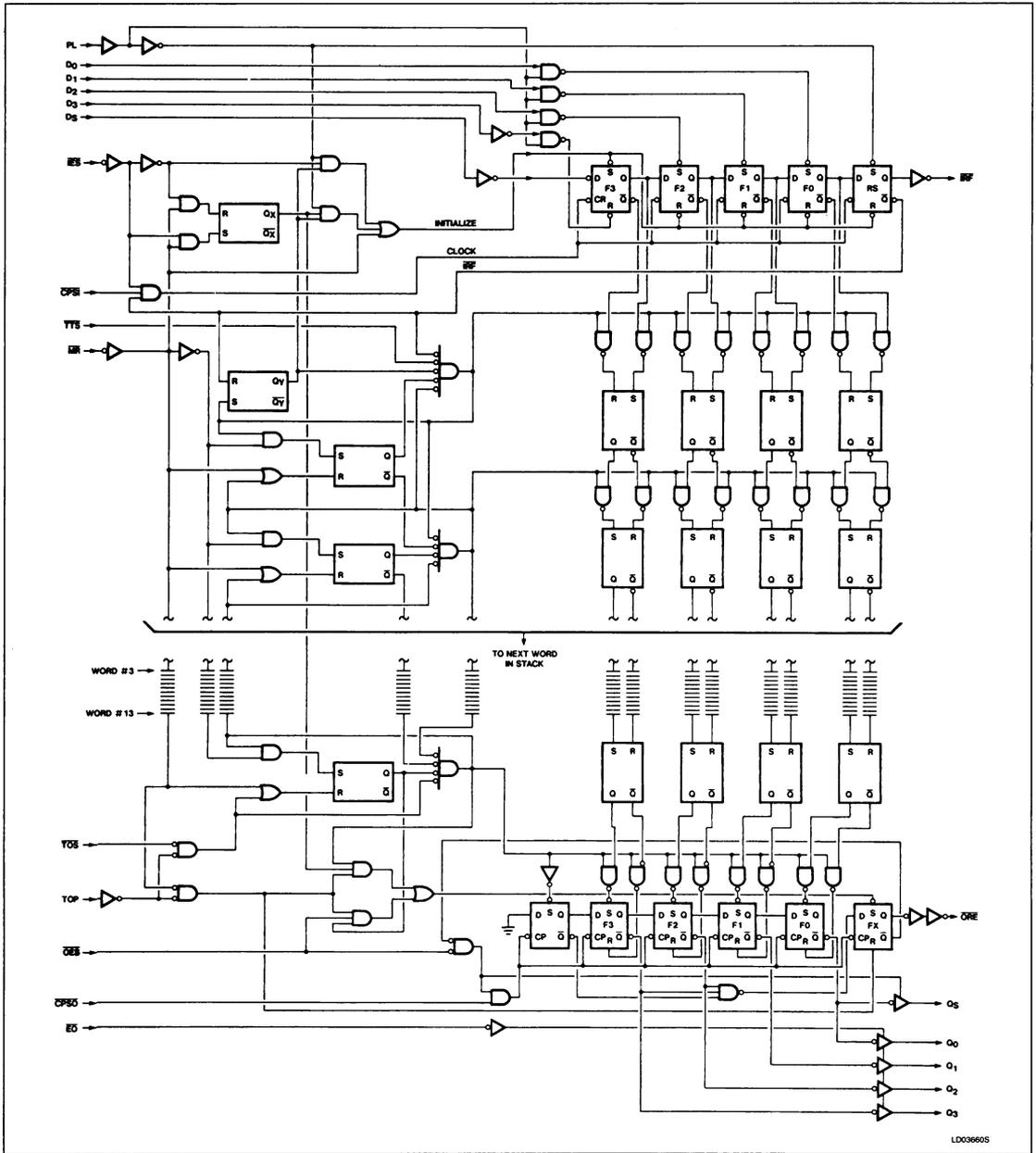
TEST CIRCUITS AND WAVEFORMS (Continued)

 <p style="text-align: right; font-size: small;">WF111805</p> <p>CONDITIONS: IES Low When Initialized, EO, CPSC Low, Data Available in Stack</p> <p style="text-align: center;">e. Parallel Output, 4-Bit Word or Master/Slave in Parallel Expansion</p>	 <p style="text-align: right; font-size: small;">WF111805</p> <p>CONDITIONS: TTS Connected to IRF, TOS Connected to ORE, IES, OES, EO, CPSC Low, Top High</p> <p style="text-align: center;">f. Fall-Through Time</p>
 <p style="text-align: right; font-size: small;">TC035805</p> <p>NOTES: 1. C_L includes jig and probe capacitance 2. All diodes are 1N3064 or equivalent</p> <p style="text-align: center;">g. Test Circuit for Measurement of AC Parameters</p>	 <p style="text-align: right; font-size: small;">WF107705</p> <p>CONDITIONS: Stack Not Full, IES Low When Initialized</p> <p style="text-align: center;">h. Parallel Load Mode, 4-BIT Word (Unexpanded) or Master/Slave Operation in Parallel Expansion</p>
 <p style="text-align: right; font-size: small;">WF107805</p> <p>CONDITIONS: Stack Not Full, Device Initialized With IES High</p> <p style="text-align: center;">j. Parallel Load, Slave Mode</p> <p style="text-align: center; font-size: small;">For all waveforms, $V_M = 1.3V$ for 74S; $V_M =$ for all other TTL families. The shaded areas indicate when the input is permitted to change for predictable output performance.</p> <p style="text-align: center;">Figure 11. 9403 Timing and Parameter-Measurement Information</p>	

64-Bit FIFO Buffer Memory

9403

LOGIC DIAGRAM



8X01A/9401 CRC Generator/Checker

Product Specification

Logic Products

FEATURES

- TTL inputs/outputs
- 12MHz (Max) data rate
- Separate preset/reset controls
- SDLC specified pattern match (8X01A only)
- Automatic right justification
- Pin-for-pin compatibility and functionally identical with 8X01 (8X01A only)
- $V_{CC} = 5V$
- 14-Pin DIP

APPLICATIONS

- Floppy and other disk systems
- Digital cassette and cartridge systems
- Data communication systems

DESCRIPTION

The CRC Generator/Checker (8X01A or 9401) provides error-correction capabilities for digital systems that handle serial data. The two parts differ in that the 8X01A provides Synchronous Data Link Control (SDLC).

The serial data stream is divided by a selected polynomial; the remainder resulting from this algebraic process is transmitted at the end of the data stream as a Cyclic Redundancy Check Character (CRCC). At the receiving end, the same calculation is performed on the data. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero; however, where SDLC protocols (8X01A only)

are used, the correct remainder is 1111000010111000 ($X^9 - X^{15}$).

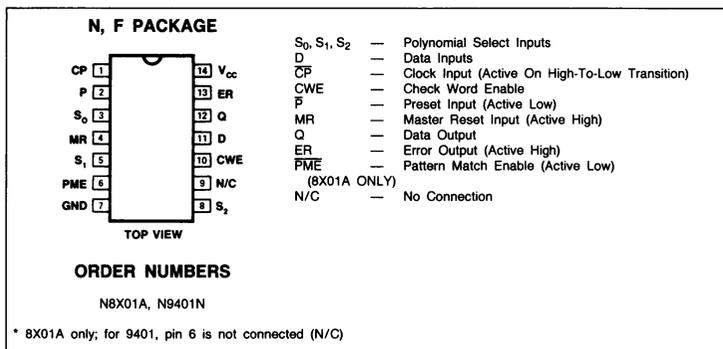
Eight polynomials are provided and any of these can be selected via a 3-bit control bus. Popular polynomials, such as CRC-16 and CCITT are implemented and the one selected can be programmed to start with all zeroes or all ones. Right justification for polynomials of degree less than 16 is automatic.

FUNCTIONAL OPERATION 8X01A and 9401

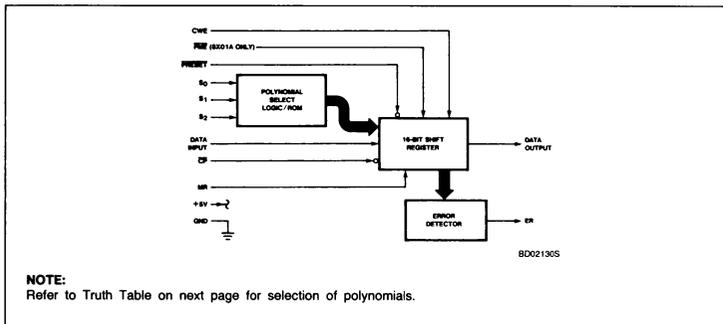
The CRC Generator/Checker circuit provides a means of detecting errors in a serial data communications environment. A binary message can be interpreted as a binary polynomial $H(x)$. This polynomial can be divided by a generator polynomial $P(x)$ such that $H(x) = P(x)Q(x) + R(x)$ whereby $Q(x)$ is the quotient and $R(x)$ is the remainder. During transmission, the remainder is appended to the end of the message as check bits. For a given message, a unique remainder is generated. Hardware implementation of division is simply a feedback shift register with Exclusive-OR gating. Subtraction and addition in modulo 2 is implemented by the Exclusive-OR function. The number of shift register stages is equal to the degree of the divisor polynomial.

The accompanying truth table defines the polynomials implemented in the CRC circuit. Each polynomial can be selected via control inputs S_0 , S_1 and S_2 . To generate the check bits, the data stream is entered via the Data (D) input, using the high to low transition of the Clock (\overline{CP}) input. This data is gated with the most significant output (Q) of the shift register which, in turn, controls the exclusive OR gates. The Check Word Enable (CWE) must be held high while the data is being entered. After the last data bit is entered, the CWE is brought low and the check bits are shifted out of the register and appended to the data bits using external gating — see Check Word Generation diagram.

8X01A & 9401 PACKAGE/PIN DESIGNATOR



BLOCK DIAGRAM OF 8X01A & 9401



CRC Generator/Checker

8X01A/9401

To check an incoming message for errors, both the data and check bits are entered through the "D" input with the \overline{CWE} input held high. The 8X01A while not in the data path, monitors the message. After the last check bit is entered, in the 8X01A, the \overline{ER} output is made valid by a high-to-low transition of \overline{CP} . If no error is detected during the data transmission, all bits of the internal register are low and the \overline{ER} output is also low; if an error is detected, it is reflected by the bit pattern and the \overline{ER} output is high. The \overline{ER} output status remains valid until the next high-to-low transition of \overline{CP} or until initialized by the preset (\overline{P}) or reset (\overline{MR}) functions. The \overline{PME} line must be high if the

\overline{ER} output is used to indicate an all-zero result.

A high level applied to the Master Reset (\overline{MR}) input asynchronously clears the shift register. A low level applied to the Preset (\overline{P}) input asynchronously sets all bits to the appropriate state if the control-code inputs (S_0 , S_1 , and S_2) specify a 16-bit polynomial. In the case of check polynomials that are 8-or-12 bits in length, only the most significant 8-or-12 bits of the shift register are set; all remaining bits are cleared.

8X01A ONLY

For data communications using the Synchronous Data Link Control (SDLC) protocol, the

8X01A is preset to an all-ones configuration before any accumulation is done; this applies to both transmitting and receiving modes of operation. Using SDLC, the check sum shifted out of the 8X01A must be inverted.

During the receiving mode, a special pattern of 1111000010111000 ($X^0 - X^{15}$) is used in place of all-zeroes to check for a valid message. The Pattern Match Enable pin allows the user to select this option. If \overline{PME} is low during the last bit time of the message, the \overline{ER} output is low providing the result matches the special pattern; if an error occurs, \overline{ER} is high.

TRUTH TABLE

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16} + X^{15} + X_2 + 1$	CRC-16
L	L	H	$X^{16} + X^{14} + X + 1$	CRC-16 REVERSE
L	H	L	$X^{16} + X^{15} + X^{13} + X^7 + X^4 + X^2 + X^1 + 1$	
L	H	H	$X^{12} + X^{11} + X^3 + X^2 + X + 1$	CRC-12
H	L	L	$X^8 + X^7 + X^5 + X^4 + X + 1$	
H	L	H	$X^8 + 1$	LRC-8
H	H	L	$X^{16} + X^{12} + X^5 + 1$	CRC-CCITT
H	H	H	$X^{16} + X^{11} + X^4 + 1$	CRC-CCITT REVERSE

RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
\overline{CP}	Clock input	0		12	MHz

CRC Generator/Checker

8X01A/9401

DC ELECTRICAL CHARACTERISTICS FOR 8X01A

PARAMETER	DESCRIPTION	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ	Max	
V _{IH}	Input high voltage		2.0			V
V _{IL}	Input low voltage				0.8	V
V _{IC}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.9	-1.5	V
V _{OH}	Output high voltage	V _{CC} = Min, I _{OH} = -400μA	2.7	3.4		V
V _{OL}	Output low voltage	V _{CC} = Min, I _{OL} = 4.0mA		0.35	0.4	V
		V _{CC} = Min, I _{OL} = 8.0mA		0.45	0.5	V
I _{IL}	Input low current	V _{CC} = Max, V _{IN} = 0.4V		-0.22	-0.36	mA
I _{IH}	Input high current	V _{CC} = Max, V _{IN} = 2.7V			20	μA
I _{IH}	Max input current	V _{CC} = Max, V _{IN} = 7V			0.1	mA
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V ²	-10		-42	mA
I _{CC}	Supply current	V _{CC} = Max, inputs open		60	110	mA

DC ELECTRICAL CHARACTERISTICS FOR 9401

PARAMETER	DESCRIPTION	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ	Max	
V _{IH}	Input high voltage	Guar. input high voltage	2.0			V
V _{IL}	Input low voltage	Guar. input low voltage			0.8	V
V _{IC}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.9	-1.5	V
V _{OH}	Output high voltage	V _{CC} = Min, I _{OH} = -400μA	2.4	3.4		V
V _{OL}	Output low voltage	V _{CC} = Min, I _{OL} = 4.0mA		0.35	0.4	V
		V _{CC} = Min, I _{OL} = 8.0mA		0.45	0.5	V
I _{IL}	Input low current	V _{CC} = Max, V _{IN} = 0.4V		-0.22	-0.36	mA
I _{IH}	Input high current	V _{CC} = Max, V _{IN} = 2.7V		1.0	40	μA
		V _{CC} = Max, V _{IN} = 5.5V			1.0	mA
I _{OS}	Output short circuit current ²	V _{CC} = Max, V _{OUT} = 0V	-15		-100	mA
I _{CC}	Supply current	V _{CC} = Max, inputs open		70	110	mA

NOTES:

- Commercial — V_{CC}(MIN) = 4.75V; V_{CC}(MAX) = 5.25V.
- No more than one output should be shorted at a time.

CRC Generator/Checker

8X01A/9401

AC ELECTRICAL CHARACTERISTICS FOR 8X01A $V_{CC} = 5V$, $T_A = +25^\circ C$

PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Max clock freq				12			MHz
Pulse widths: $t_w - \overline{CP}(L)$ $t_w - \overline{P}(L)$ $t_w - MR(H)$	Clock low Preset low Master reset high			See Figure 2 See Figure 3 See Figure 4	35 35 35			ns ns ns
Set-up/hold times: $t_s - D$ $t_s - \overline{CWE}(L)$ $t_h - D \& \overline{CWE}$	Set-up time Set-up time Hold time	Data CWE Data & CWE	Clock Clock Clock	See Figure 5	55 55 0			ns ns ns
Propagation delay: $t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{PRESET}	Data output	See Figures 1, 2, & 3			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Data output	See Figure 4			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{PRESET}	Error output	See Figure 3			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Error output	See Figure 4			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{CP}	Data output	See Figure 2			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{CP}	Error output	See Figure 2			55	ns
t_{REC}	Recovery time	Preset, MR	Clock	See Fig. 3 & 4	35			ns

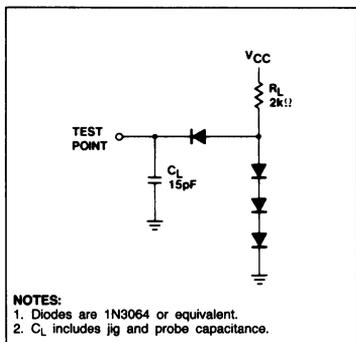
AC ELECTRICAL CHARACTERISTICS FOR 9401 $V_{CC} = 5V$, $T_A = +25^\circ C$

PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Max clock freq				12	20		MHz
Pulse widths: $t_w - \overline{CP}(L)$ $t_w - \overline{P}(L)$ $t_w - MR(H)$	Clock low Preset low Master reset high			See Figure 2 See Figure 3 See Figure 4	35 40 35	30 25		ns ns ns
Set-up/hold times: $t_s - D$ $t_s - \overline{CWE}$ $t_h - D \& \overline{CWE}$	Set-up time Set-up time Hold time	Data CWE Data & CWE	Clock Clock Clock	See Figure 5	55 55 0	35 35 -8		ns ns ns
Propagation delay: $t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{PRESET}	Data output	See Figures 1, 2, & 3		40 60		ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Data output	See Figure 4		30 55		ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{PRESET}	Error output	See Figure 3		40 60		ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Error output	See Figure 4		40 60		ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{CP}	Data output	See Figure 2		30 55		ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	\overline{CP}	Error output	See Figure 2		40 60		ns
t_{REC}	Recovery time	Preset, MR	Clock	See Fig. 3 & 4	35	25		ns

CRC Generator/Checker

8X01A/9401

TEST CIRCUIT



INPUT/OUTPUT STRUCTURES

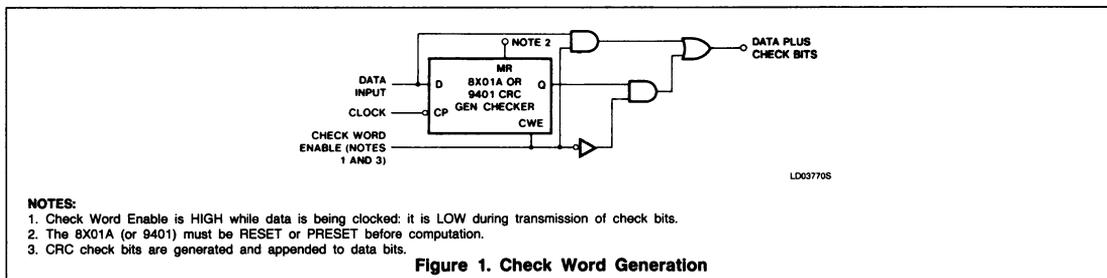
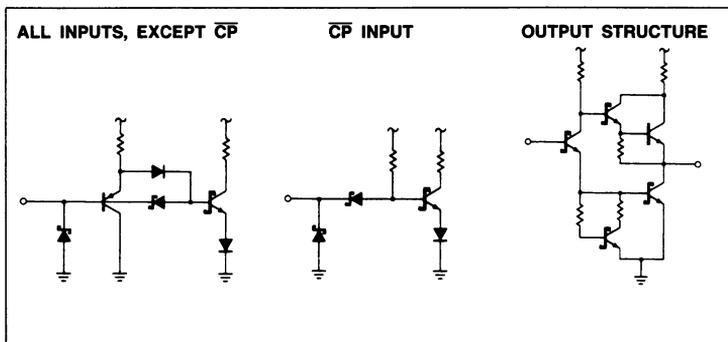
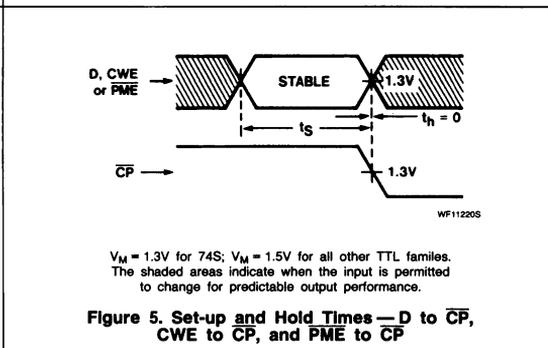
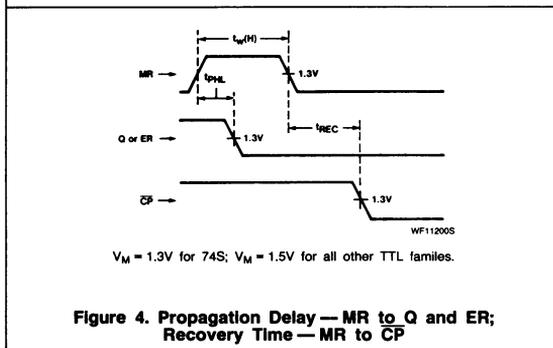
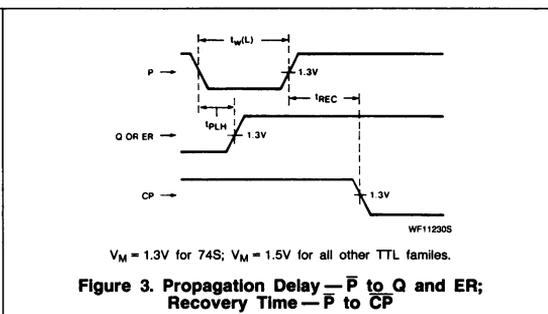
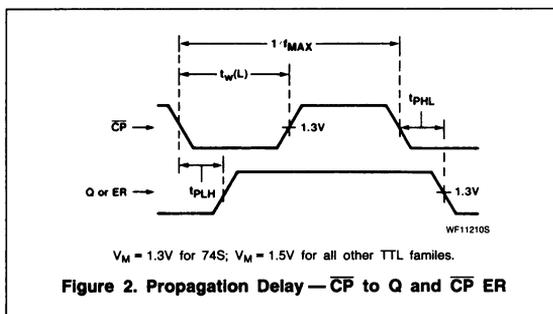


Figure 1. Check Word Generation

TEST CIRCUITS AND WAVEFORMS



8X02A Control Store Sequencer

Product Specification

Logic Products

FEATURES

- 10-Bit Address Generator (1024 Microinstruction Addressability)
- Operating Frequency Exceeding 12 MHz
- Direct Branching Over Full Address Range
- Conditional Branching
- Subroutine Branching Capability
- 4-Level Stack Register File

- Loop Control Facility Using Stack
- Three-State Address Outputs

PRODUCT DESCRIPTION

The Signetics 8X02A Control Store Sequencer generates addresses to access instructions from a microprogram memory (control store). This high-speed device provides an efficient means of controlling the flow through a microprogram

with a powerful set of sequencing functions. The 8X02A can directly address up to 1024 microinstructions; however, the total address space can be expanded by adding conventional paging techniques. Combined with memory, the 8X02A forms a powerful control section for CPU's, controllers, test equipment, and other microprogram-controlled systems.

8X02A PACKAGE AND PIN DESIGNATIONS

N PACKAGE

ORDER NUMBER

N8X02AN

PIN NO.	IDENTIFIER	FUNCTION
1, 28, 27	AC ₂ - AC ₀	Inputs used to select any one of eight Address Control Functions - see Table 1.
2	\overline{EN}	Enable three-state address outputs (A ₀ - A ₉); active-low input.
3 - 6, 8 - 13	A ₀ - A ₉	Three-state address outputs used to specify microprogram address; (A ₀ = LSB, A ₉ = MSB).
7	GND	Ground
14 - 21, 23, 24	B ₀ - B ₉	Branch address inputs: (B ₀ = LSB, B ₉ = MSB).
22	V _{CC}	Supply voltage.
25	CLK	Clock input (positive edge used for all triggering).
26	TEST	Active-high condition input used to determine conditional skips, branches, subroutine calls, and loop termination.

Control Store Sequencer

8X02A

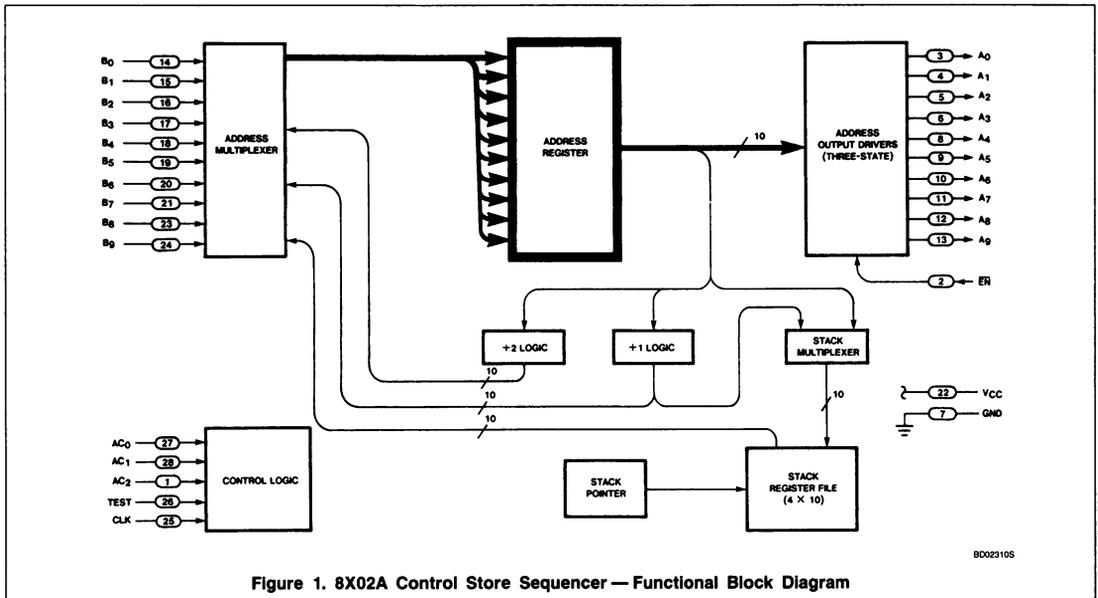


Figure 1. 8X02A Control Store Sequencer — Functional Block Diagram

FUNCTIONAL OPERATION

As shown in Figure 1, the data appearing on the address output pins ($A_0 - A_9$) is the contents of the 10-bit Address Register. On the rising edge of the clock input pulse (CLK), a new address is latched into the Address Register. This new address is supplied via the Address Multiplexer which selects one of five sources:

- Branch Address Input ($B_0 - B_9$)
- Current Address + 1
- Current Address + 2 (for the SKIP function)
- Stack Register File (most recent entry)
- All Zeroes (RESET)

The selection of the next address is determined by the "Address Control Function" specified by inputs $AC_0 - AC_2$ and the TEST input. Table 1 defines the eight Address Control Functions.

The "Reset" (RST) Address Control Function unconditionally forces all Address Register bits to zero on the rising edge of CLK. Sequential microprogram flow is provided by the "Increment" (INC) function which unconditionally increments the Address Register by one for each clock cycle. The Address Register automatically wraps around from the highest address (all "1s") to the lowest address (all "0s").

As shown in Table 1, the TEST input is used to conditionally execute four of the eight Address Control Functions. If the TEST input is **low** (false), the Address Register is simply

incremented by one — (for the BLT function, the Stack Pointer is also decremented). If the TEST input is **high** (true), the sequencer executes one of the following:

- Skip (TSK) — the Address Register is incremented by two.
- Branch (BRT) — the Address Register is loaded from the Branch Address Inputs.
- Branch-to-Subroutine (BSR).
- Branch-to-Loop (BLT).

The Stack Register File holds up to four 10-bit addresses and operates in the Last-In/First-Out (LIFO) mode. A Stack Pointer keeps track of the next register of the Stack File to be written into; the pointer is incremented after each "push" and decremented after each "pop" — see Table 1. When branching to a subroutine (BSR), the return address (current address + 1) is "pushed" onto the stack and the branch address input is loaded into the Address Register. To return from a subroutine, the "POP" function pops the return address off the stack and loads it into the Address Register.

The "Push-for-Looping" (PLP) function may be specified in the first instruction of a loop to "push" the current address onto the stack; the Address Register is incremented. A "Branch-to-Loop" (BLT) function placed at the end of the loop "pops" the stack and conditionally branches to the top-of-loop address, depending on the TEST input. If the test for repeating the loop is satisfied (TEST input **high**), the sequencer causes a branch

back to the first instruction of the loop in which the top-of-loop address is "pushed" back onto the stack. If the test fails (TEST input **low**), the top-of-loop address is discarded, the stack pointer is decremented and the Address Register is incremented. A combination of subroutines and loops may be nested up to four levels deep.

In abnormal circumstances, the Stack Pointer will wraparound from the fourth to the first register of the Stack File and vice-versa. If the stack is full (four addresses currently stored), an additional "push" causes the first (oldest) entry to be overwritten — (the four most recent entries are always maintained). If the stack is empty, a "pop" will access the fourth register of the Stack File; however, the contents of this register may be unpredictable.

The three-state address outputs ($A_0 - A_9$) are controlled by a common enable input (EN). When the enable input is **high**, the output drivers are placed in the high-impedance state allowing alternative access to the microprogram memory. Other circuit functions are unaffected by EN.

NOTE

To implement a RESET externally it is necessary to force all Address Control Inputs ($AC_0 - AC_2$) to the **high** state until at least one rising edge of CLK has occurred. If the AC inputs are supplied directly from the microprogram memory, a RESET may be accomplished by disabling the memory outputs. Pullup resistors should be provided to achieve the required high voltage level.

Control Store Sequencer

8X02A

Table 1. Address Control Functions

MNEMONIC AND DESCRIPTION	CONTROL LINES				NEXT ADDRESS	STACK OPERATION	STACK POINTER
	AC ₂	AC ₁	AC ₀	Test			
TSK – Test and skip	0	0	0	0	Current address + 1 Current address + 2	No change No change	No change No change
	0	0	0	1			
INC – Increment	0	0	1	X	Current address + 1	No change	No change
BLT – Branch to loop if test condition is true	0	1	0	0	Current address + 1 From stack register file	POP (ignore data) POP (read)	Decrement by 1 Decrement by 1
	0	1	0	1			
POP – Pop stack (return from subroutine)	0	1	1	X	From stack register file	POP (read)	Decrement by 1
BSR – Branch to subroutine if test condition is true	1	0	0	0	Current address + 1 Branch address inputs B ₀ – B ₉	No change PUSH (write current address + 1)	No change Increment by 1
	1	0	0	1			
PLP – Push for looping	1	0	1	X	Current address + 1	PUSH (write current address)	Increment by 1
BRT – Branch if test condition is true	1	1	0	0	Current address + 1 Branch address inputs B ₀ – B ₉	No change No change	No change No change
	1	1	0	1			
RST – Reset address to zero	1	1	1	X	All zeroes	No change	No change

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Off-state output voltage	+5.5	Vdc
T _{STG} Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS Conditions: Commercial – V_{CC} = 5.0V (±5%), 0°C ≤ T_A ≤ 70°C

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ ¹	Max	
V _{IH} V _{IL} V _{IC}	High level input voltage Low level input voltage Input clamp voltage	V _{CC} = Min	2			V
		V _{CC} = Min			0.8	
		V _{CC} = Min; I _I = -18mA			-1.5	
V _{OH} V _{OL}	High level output voltage Low level output voltage	V _{CC} = Min; I _{OH} = -2.6mA	2.4	3.4		
		V _{CC} = Min; I _{OL} = 8mA		0.42	0.5	
I _I	Input current at maximum input voltage	V _{CC} = Max; V _I = 5.5V		1	100	μA
I _{IH}	High level input current: AC ₂ – AC ₀ , TEST, CLK B ₉ – B ₀ , \overline{EN}	V _{CC} = Max; V _{IH} = 2.7V		< 0.1	40	μA
				< 0.1	20	
I _{IL}	Low level input current: AC ₂ – AC ₀ , TEST, CLK B ₉ – B ₀ , \overline{EN}	V _{CC} = Max; V _{IL} = 0.4V		-24	-800	μA
				-12	-400	
I _{OS}	Short circuit output current ²	V _{CC} = Max	-15	-60	-100	mA
I _{OZH}	High-Z state output current – high level	V _{CC} = Max; V _{OH} = 2.7V			20	μA
I _{OZL}	High-Z state output current – low level	V _{CC} = Max; V _{OL} = 0.4V			-20	μA
I _{CC}	Supply current	V _{CC} = Max		170	250	mA

NOTES:

1. Typical limits are: V_{CC} = 5.0V and T_A = 25°C.
2. For purposes of testing, not more than one output should be shorted at a time.

Control Store Sequencer

8X02A

AC ELECTRICAL CHARACTERISTICS Conditions: Commercial – $V_{CC} = 5.0V (\pm 5\%)$, $0^{\circ}C \leq T_A \leq 70^{\circ}C$
 Loading – See Test Loading Circuit

PARAMETERS ¹	REFERENCES		LIMITS ⁴			UNIT
	From	To	Min	Typ ²	Max	
Pulse width:						
t _{CW} Clock cycle time	↑ CLK	↑ CLK	80			ns
t _{PWH} Clock high	↑ CLK	↓ CLK	35	24		ns
t _{PWL} Clock low	↓ CLK	↑ CLK	15	9		ns
Propagation delay:						
t _{PLZ} Low to high-Z	↑ \overline{EN}	A ₀ – A ₉		14	20	ns
t _{PHZ} High to high-Z	↑ \overline{EN}	A ₀ – A ₉		35	42	ns
t _{PZL} High-Z to low	↓ \overline{EN}	A ₀ – A ₉		10	20	ns
t _{PZH} High-Z to high	↓ \overline{EN}	A ₀ – A ₉		20	30	ns
t _{PHL} High to low	↑ CLK	↓ A ₀ – A ₉		25	45	ns
t _{PLH} Low to high	↑ CLK	↑ A ₀ – A ₉		25	45	ns
t _{HA} Address output hold time ³	↑ CLK	A ₀ – A ₉	13			ns
Set-up/hold times:						
t _{SF} Function set-up time	AC ₀ – AC ₂	↑ CLK	20	18		ns
t _{SK} Branch set-up time	B ₀ – B ₉	↑ CLK	15	7		ns
t _{SI} Test set-up time	TEST	↑ CLK	20	15		ns
t _{HF} Function hold time	↑ CLK	AC ₀ – AC ₂	20	2		ns
t _{HK} Branch hold time	↑ CLK	B ₀ – B ₉	15	9		ns
t _{HI} Test hold time	↑ CLK	TEST	12	-2		ns

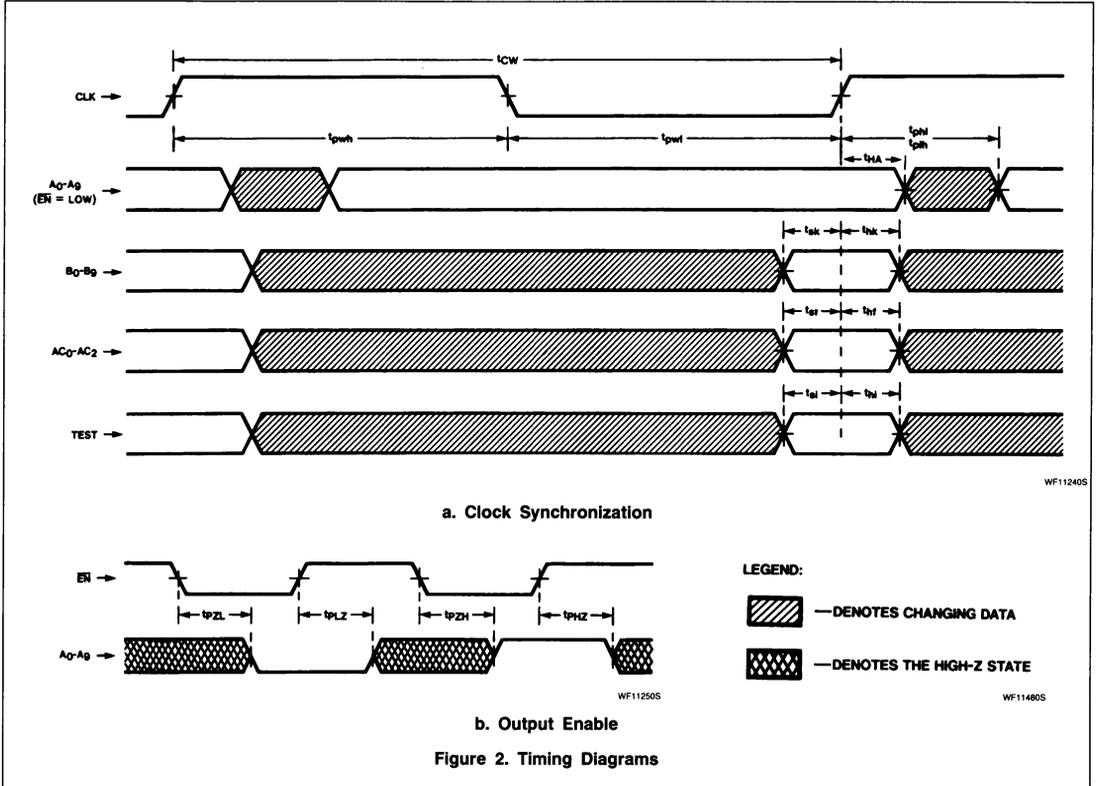
NOTES:

1. Parameter definitions are illustrated in the Timing Diagrams – See Figure 2.
2. Typical limits are: $V_{CC} = 5.0V$ and $T_A = 25^{\circ}C$.
3. t_{HA} is the minimum time the current address outputs remain stable before changing. This delay may be used to provide some of the hold times required for the AC, B, and TEST inputs, if these inputs are determined by the microprogram memory addressed by the 8X02A.
4. This data supercedes the November, 1980 edition of this data sheet.

Control Store Sequencer

8X02A

TIMING DIAGRAM

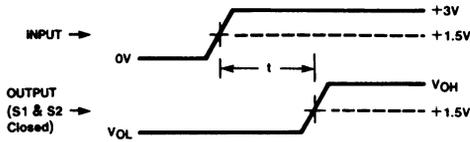


Control Store Sequencer

8X02A

AC VOLTAGE WAVEFORMS AND TEST LOADING

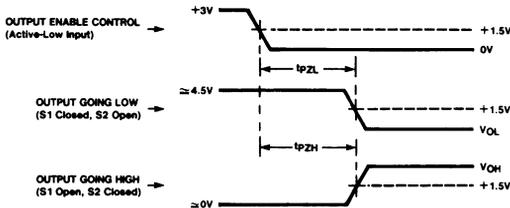
PROPAGATION DELAY (Typical Example):



WF11260S

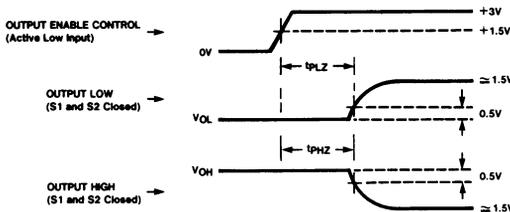
NOTE:
Pulse widths and setup/hold times are measured using the same reference points shown in the above waveforms.

OUTPUT ENABLE TIMES (Three-state outputs):

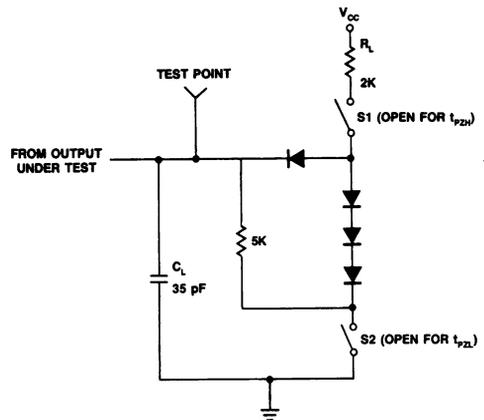


WF11270S

OUTPUT DISABLE TIMES (Three-state outputs):



WF11270S



TC03640S

NOTES:

1. C_L includes probe and jig capacitance.
2. All diodes are 1N3064 or equivalent.
3. Switches S1 and S2 are both closed for all measurements except Output Enable times — See AC VOLTAGE WAVEFORMS.

Control Store Sequencer

8X02A

APPLICATION

FUNCTIONAL DESCRIPTION

Figure 3 shows a typical configuration of an 8X02A-based control section in a CPU application. Microinstructions read from the memory are used to produce control signals for

the CPU and to determine the next microinstruction via the 8X02A Address Control inputs ($AC_0 - AC_2$). In the case of a conditional branch or skip, the status condition applied to the 8X02A TEST input is selected according to the microinstruction. In a branch-type microinstruction, a branch field typically supplies the 8X02A Branch Address inputs ($B_0 - B_9$). (In non-branching instructions, this field may

contain other CPU control information.) When a macroinstruction is presented to the CPU, the starting address of the microprogram routine which executes the macroinstruction is presented to the Branch Address inputs. Similar configurations may be used for other applications in which the Branch Address inputs are typically supplied directly from the microprogram memory.

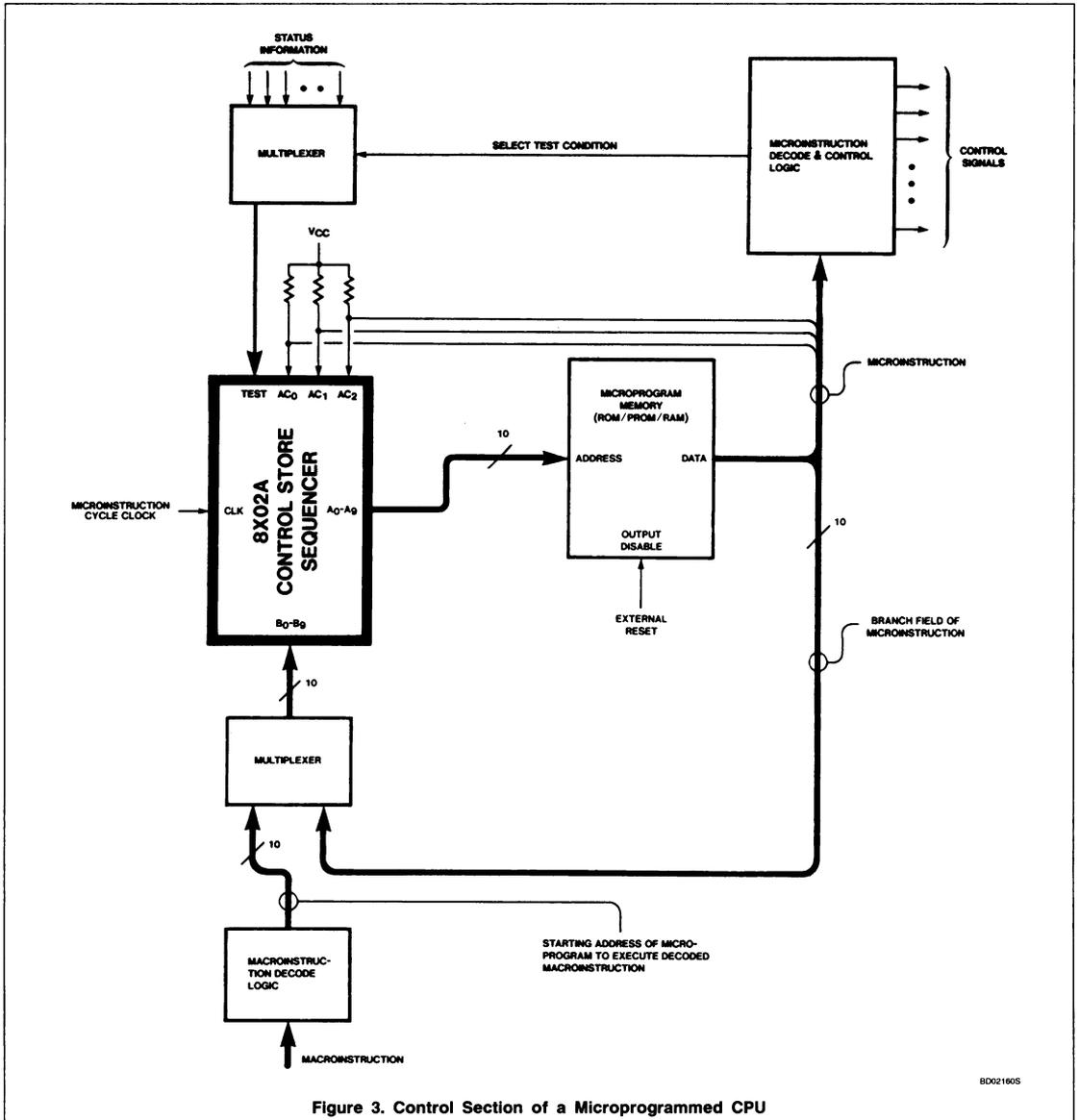


Figure 3. Control Section of a Microprogrammed CPU

8D02160S

8X41 Autodirectional Bus Transceiver

Product Specification

Logic Products

DESIGN FEATURE

- Intelligent bidirectional bus repeater with self-generating or external control
- Eight independent channels
- Open-collector outputs (meets DEC UNIBUS* specifications)
- TTL compatible
- High speed (30-nanoseconds max)
- Expandable to any number of bits
- High input impedance for every operating value of V_{CC}
- Low input current (less than 100-microamperes); high output current (up to 70-milliamperes)
- 0.6 in. 24-pin DIP
- +5V supply

USE AND APPLICATION

- Minicomputers
- Microcomputers MOS/Bipolar
- Communications
- Signal buffer
- Bus fan-out extensions
- Distributed processing
- Bidirectional bus connector/isolator

PRODUCT DESCRIPTION

The Signetics 8X41 Autodirectional Bus Transceiver is a general purpose asynchronous device ideal for system bus expansion applications. The 8X41 consists of eight data channels, each with one pair of terminals (A_i and B_i); each data channel can be operated independently.

The device requires no external controls since all intelligence is internally generated; thus, operation of the device is completely autonomous. The first logic

low signal that occurs on one channel terminal (A_i and B_i) will be repeated on the corresponding terminal (B_i or A_i) of the same channel.

The 8X41 is designed for use in open-collector bus systems where high speed and low-current inputs/high-current outputs are required. In system configurations, the discrete capabilities of the bus transceiver can be expanded by parallel connection to service any number of bits. To provide reliable operation and integrity of data transfers, all channels are disabled by an on-chip power monitor whenever V_{CC} falls below approximately 4V.

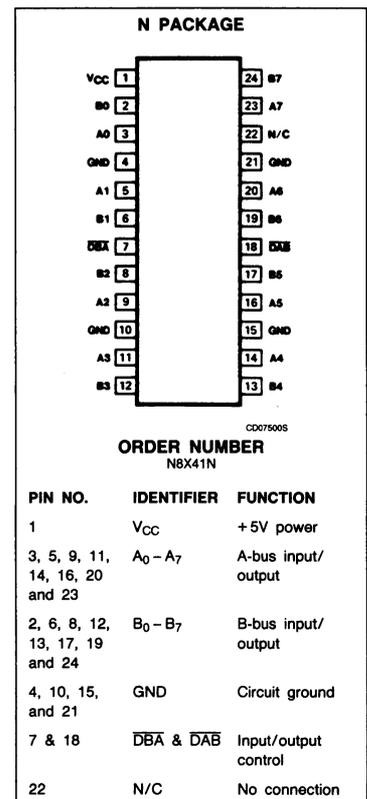
FUNCTIONAL OPERATION

The 8X41 (Figure 1) consists of eight functionally independent yet logically identical channels. Each channel consists of two bus terminals (A_i and B_i); each terminal is internally connected to an open-collector driver and a high-impedance receiver. The monitoring state of each channel is defined when both terminals (A_i and B_i) are "high"; in this state, the internal logic of the 8X41 continually examines the A and B bus signals to determine signal direction — A_i to B_i or B_i to A_i . A low signal occurring at either of the two terminals causes the open-collector driver on the opposite terminal to follow suit; hence, the signal is repeated by the 8X41. For each channel, latches L1 and L2 determine signal direction. As shown in the truth table for these latches, there is no transmission of data when both signals are low; however, this condition should never occur during normal system operation.

The internal automatic direction control can be overridden by either or both of the common disable inputs — \overline{DBA} and \overline{DAB} . When \overline{DBA} is driven low ($\overline{DAB} = \text{high}$), the B_i to A_i path is inter-

rupted and the device becomes a unidirectional repeater in the A_i to B_i direction only. With these conditions reversed ($\overline{DAB} = \text{low}$ and $\overline{DBA} = \text{high}$), the A_i to B_i path is interrupted and the chip functions as a unidirectional repeater in the B_i to A_i direction. When both control signals are low, data passage is inhibited in both directions. Refer to the I/O truth table for all possible input/output conditions.

8X41 PACKAGE/PIN DESIGNATIONS



Autodirectional Bus Transceiver

8X41

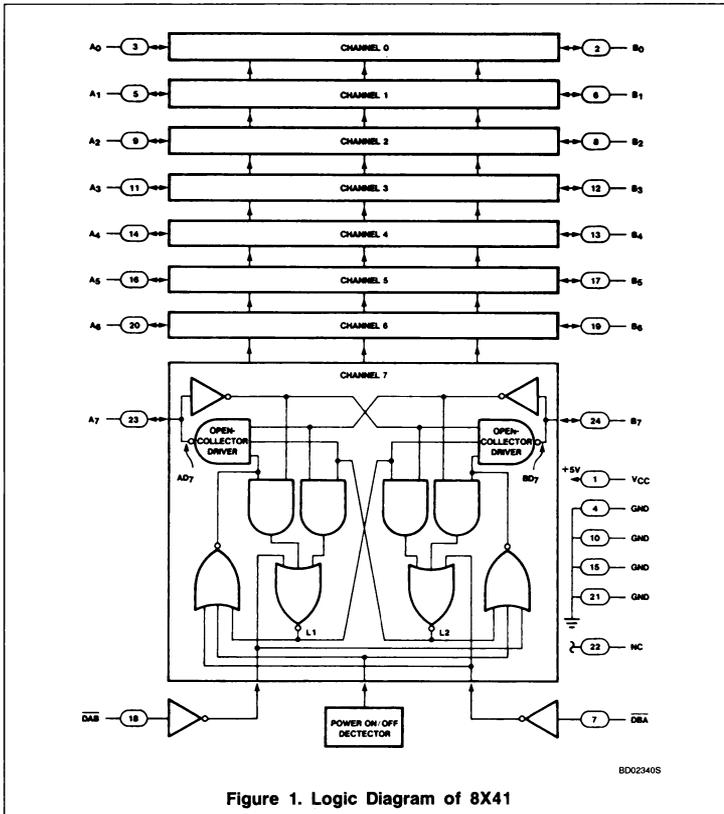


Figure 1. Logic Diagram of 8X41

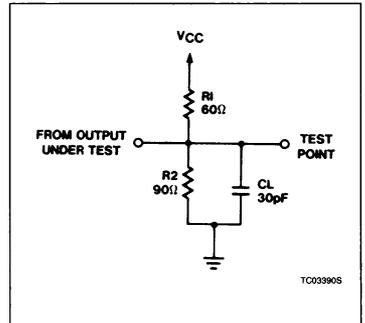
DBA	DAB	FUNCTION
0	0	Data transmission inhibited
0	1	$A_i \rightarrow B_i$
1	0	$A_i \leftarrow B_i$
1	1	$A_i \rightarrow B_i$ $A_i \leftarrow B_i$

i = Channel 0, 1, 2, 3, 4, 5, 6, or 7
 $A_i \rightarrow B_i$ = Data transmission from A_i to B_i
 $A_i \leftarrow B_i$ = Data transmission from B_i to A_i

TRUTH TABLE

LATCHES		DIRECTION OF DATA
L ₁	L ₂	
1	1	Monitoring state
1	0	A_i to B_i
0	1	B_i to A_i
0	0	No transmission

LOAD CIRCUIT FOR OUTPUTS



INPUT/OUTPUT TRUTH TABLE

EXTERNAL CONTROLS		INPUT SIGNALS		OUTPUT DRIVER SIGNALS	
DAB	DBA	A _i	B _i	AD _i	BD _i
H	H	L	L	H	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	H	H
H	L	L	L	H	L
H	L	L	H	H	L
H	L	H	L	H	H
H	L	H	H	H	H
L	H	L	L	L	H
L	H	L	H	H	H
L	H	H	L	L	H
L	H	H	H	H	H
L	L	X	X	H	H

NOTES:
 A_i = External signal
 AD_i = Output A driver
 B_i = External signal
 BD_i = Output B driver
 X = Don't care

Autodirectional Bus Transceiver

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DC CHARACTERISTICS $V_{CC} = 5V (\pm 5\%)$; $T_A = 0^\circ C$ to $70^\circ C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OL}	Bus output low voltage (driver ON)	$I_{OL} = 70mA$; $V_{CC} = MIN$			0.5	V
$*V_B$	Bus input threshold voltage (driver OFF)		1.3		1.7	V
V_{IH} (\overline{DBA} , DAB only)	High level input voltage		2.0			V
V_{IL} (\overline{DBA} , DAB only)	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = MIN$; $I_{IL} = -18mA$			-1.5	V
V_{PD}	Power ON/OFF detector threshold voltage		3.7		4.35	V
I_{IH} (DBA, \overline{DAB} only)	High level input current	$V_{CC} = Max$; $V_{IN} = 2.7V$			20	μA
I_{IL} (DBA, \overline{DAB} only)	Low level input current	$V_{CC} = Max$; $V_{IN} = 0.4V$			-0.4	mA
I_I	Bus input current (driver OFF)	$V_{CC} = Max$; $V_B = 2.5V^*$			100	μA
		$V_{CC} = Max$; $V_B = 0V^*$			-20	
I_{OFF}	Bus leakage current (power OFF)	$V_{CC} = 0V$; $V_B = 2.5V^*$			100	μA
I_{CC}	Supply current	$V_{CC} = Max$; $A_0 - A_7 = Low$ or $B_0 - B_7 = Low$ and $DBA = DAB = High$		145	180	mA

NOTE: $*V_B = V_{BUS}$ **AC CHARACTERISTICS** $V_{CC} = 5V (\pm 5\%)$; $T_A = 0^\circ C$ to $70^\circ C$

PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{PLL}	Propagation delay	Low A_i Low B_i	Low BD_i Low AD_i	$\overline{DBA} = \overline{DAB} = High$			30	ns
t_{PHH}	Propagation delay	High A_i High B_i	High BD_i High AD_i	$\overline{DBA} = \overline{DAB} = High$			30	ns
t_{DHH}	Propagation delay	High A_i	High BD_i	$\overline{DBA} = Low$; $\overline{DAB} = High$			25	ns
		High B_i	High AD_i	$\overline{DAB} = Low$; $\overline{DBA} = High$			25	
t_{DLL}	Propagation delay	Low A_i	Low BD_i	$\overline{DBA} = Low$; $\overline{DAB} = High$			25	ns
		Low B_i	Low AD_i	$\overline{DAB} = Low$; $\overline{DBA} = High$			25	
t_{DEH}	Propagation delay	Low \overline{DAB}	High AD_i	$\overline{DAB} = Low$; $A_i = Low$			30	ns
t_{DEL}	Propagation delay	High \overline{DBA}	Low AD_i	$\overline{DAB} = Low$; $B_i = Low$			30	ns
t_{DEH}	Propagation delay	Low \overline{DBA}	High BD_i	$\overline{DBA} = Low$; $B_i = Low$			30	ns
t_{DEL}	Propagation delay	High \overline{DAB}	Low BD_i	$\overline{DBA} = Low$; $A_i = Low$			30	ns
t_r	Recovery time (see timing diagram)	—	—	$\overline{DBA} = \overline{DAB} = High$		20		ns

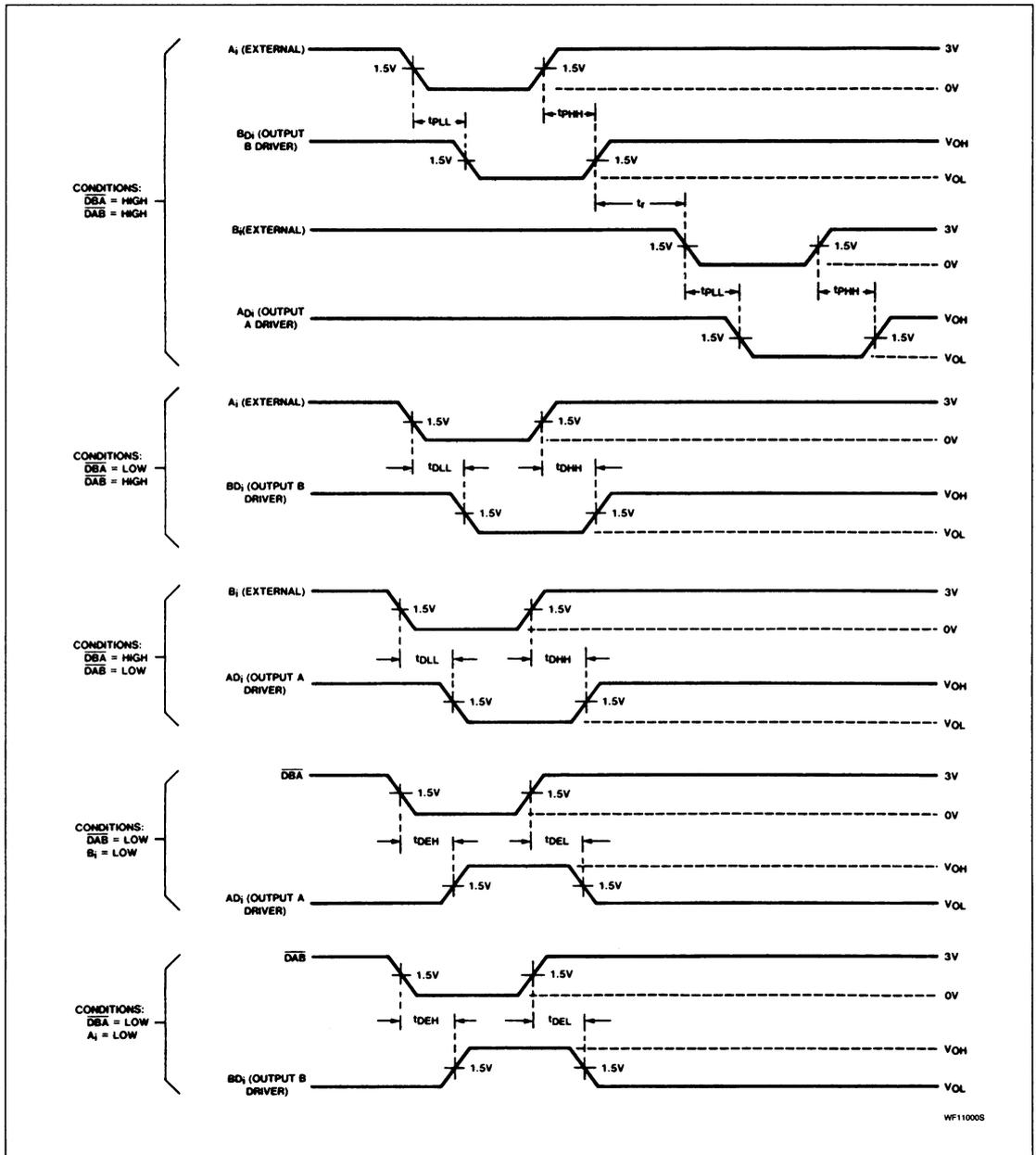
NOTES:

A_i = External signal
 AD_i = Output A driver
 B_i = External signal
 BD_i = Output B driver

Autodirectional Bus Transceiver

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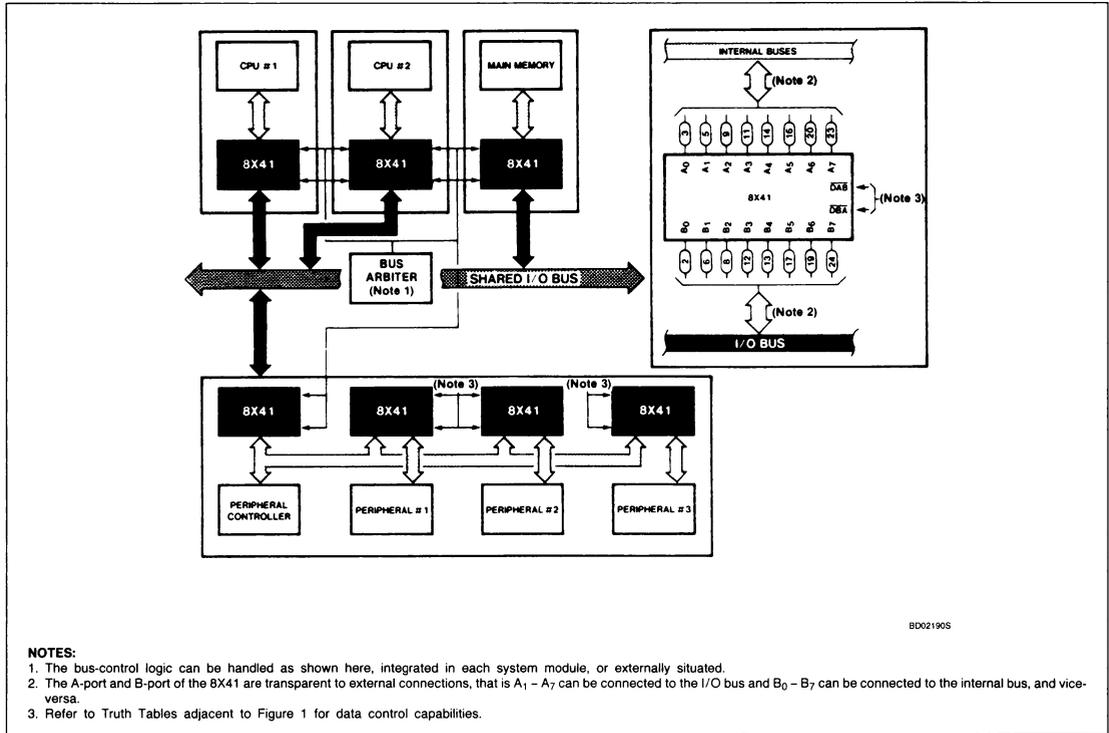
8X41 TIMING DIAGRAM



Autodirectional Bus Transceiver

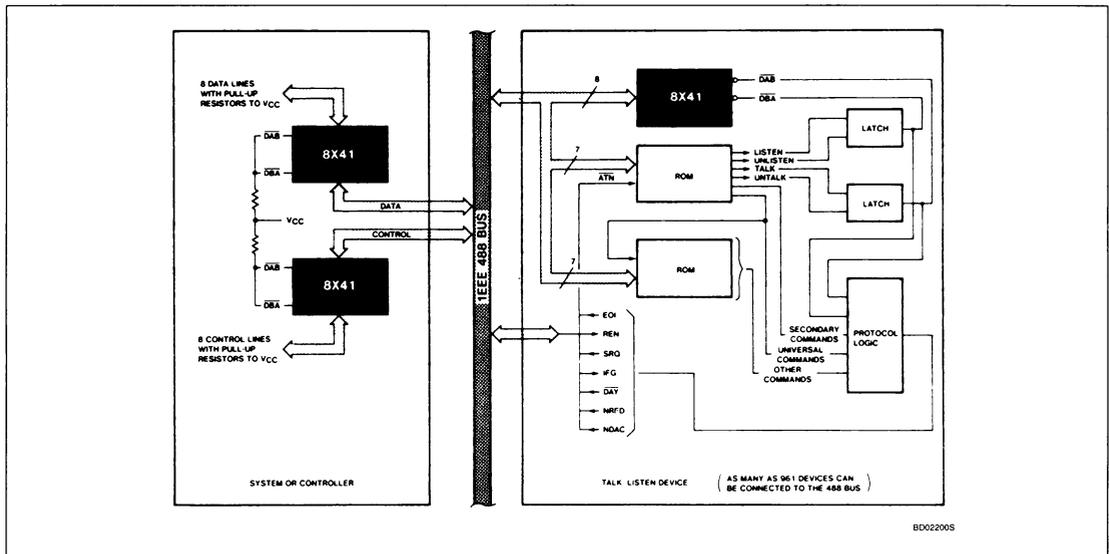
8X41

USING THE 8X41 IN A BUS-SHARED CONFIGURATION



BD021905

INTERFACING 8X41 TO IEEE 488 BUS



BD022005

8X60 FIFO RAM Controller (FRC)

Product Specification

Logic Products

FEATURES

- 12-Bit FIFO Address Generator
- Data Rate Exceeding 8MHz
- Asynchronous Read/Write Operations
- Three-State Address Outputs
- User-Defined Word Width
- Specifically Designed for Use with High-Speed Bipolar RAMs (Adaptable for Use with MOS RAMs)
- TTL Input and Output
- 16mA Address-Drive Capability

USE AND APPLICATION

- Interface Between Independently-Clocked Systems
- Buffer Memories for Disk and/or Tape
- Data Communication Concentrators
- CPU/Terminal Buffering
- DMA Applications
- CRT Terminals

PRODUCT DESCRIPTION

The Signetics 8 × 60 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed/high-capacity First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs — see **Applications** on the last page of this data sheet. The FRC can control up to 4096 words of buffer memory; intermediate buffer sizes can be selected — refer to the memory length table on the next page. Built-in arbitration logic handles read/write operations on a first-come/first-served basis.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8X60N
Hermetic CERDIP	N8X60F

As shown in Figure 1, the FRC consists of:

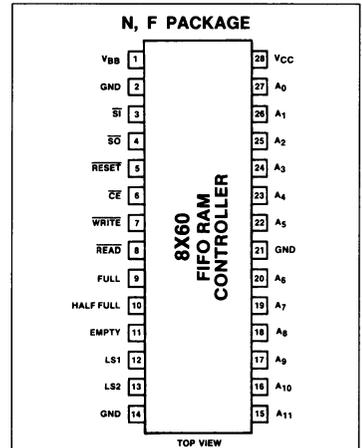
- A 12-Bit Write Address Generation Counter (Counter #1) and a 12-Bit Read Address Generation Counter (Counter #2).
- A 12-Bit Up/Down Status Counter (Counter #3).
- Twelve Three-State Address Drivers.
- Control Logic.

The two address counters, #1 and #2, respectively, are used to generate write and read addresses; the outputs of these counters are multiplexed to the three-state address drivers. Counter #3 generates **full**, **empty**, and **half full** status.

FUNCTIONAL OPERATION

The FRC operates in either of two basic modes — **write** into the FIFO buffer memory or **read** from the FIFO buffer memory. These two operations are described in subsequent paragraphs and the complete sequence is summarized in Table 1. Typical Write/Read timing relationships, arbitration logic, and chip-enable control are shown in the Timing Diagrams.

PIN CONFIGURATION



PIN NO.	IDENTIFIER	FUNCTION
1	V _{BB}	Supply voltage for internal circuits.
2, 14, 21	GND	Circuit ground.
3	S _I	Shift-In request for write cycle; active-low input.
4	S _O	Shift-Out request for read cycle; active-low input.
5	RESET	Active-low master reset input.
6	C _E	Active-low chip enable input.
7	WRITE	Write cycle address valid; active-low output.
8	READ	Read cycle address valid; active-low output.
9	FULL	Memory full status output; also, override input capability. Active when high.
10	HALF FULL	Memory half-full status output; active-high.
11	EMPTY	Memory empty status output; also, override input capability. Active when high.
12	LS1	Least significant bit (LSB) of the memory length select input.
13	LS2	Most significant bit (MSB) of the memory length select input.
15 - 20 22 - 27	A ₁₁ - A ₀	Three-state address outputs: A ₀ = LSB.
28	V _{CC}	Supply voltage.

FIFO RAM Controller (FRC)

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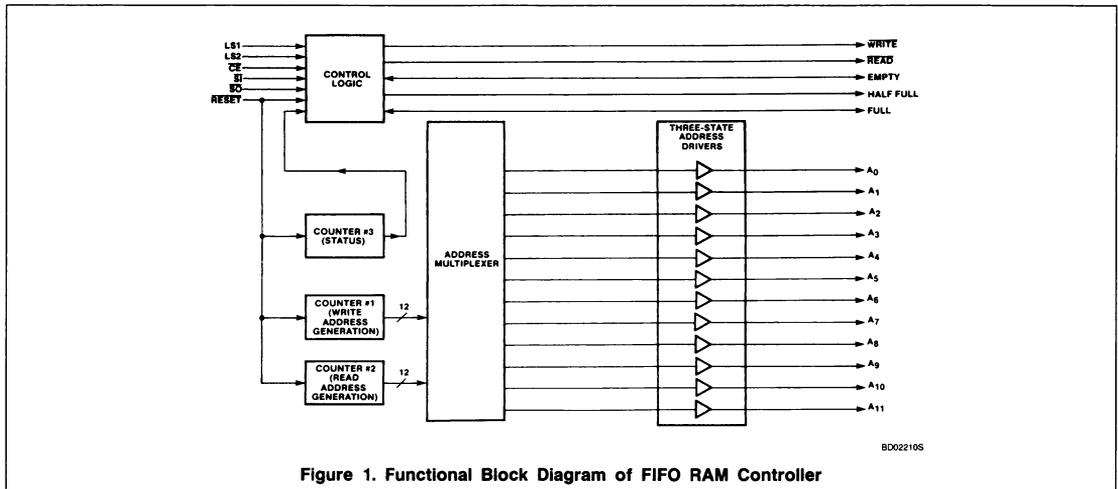


Figure 1. Functional Block Diagram of FIFO RAM Controller

FIFO BUFFER MEMORY — WRITE CYCLE

To perform a write operation, \overline{SO} must be **high** and \overline{SI} must be **low**. When these conditions exist and other control parameters (Table 1) are satisfied, the write address in Counter # 1 (Figure 1) is output to the address bus via the multiplexer and **WRITE** output goes **low**. (Note. Normally, the **WRITE** output goes **low** after the address output becomes state — refer to **WRITE Cycle Timing Diagram**. The **WRITE** output may then act as a **write** or **chip** enable for the RAMs that are used to implement the memory.

When the **write** cycle is ended (\overline{SI} is forced high), the **WRITE** output goes **high**, the address output buffers return to a high-impedance state. Counter # 1 (Write Address Generation) and Counter # 3 (Status) are both incremented, and Counter # 2 (Read Address Generation) remains unchanged.

FIFO BUFFER MEMORY — READ CYCLE

To perform a read operation, \overline{SI} must be **high** and \overline{SO} must be **low**. When these conditions exist and other control parameters (Table 1) are satisfied, the read address contained in Counter # 2 (Figure 1) is output to the address bus and the **READ** output goes **low**.

When the **read** cycle is ended (\overline{SO} is forced high) the **READ** output goes **high**, the output buffers return to a high-impedance state. Counter # 2 (Read Address Generation) is incremented. Counter # 3 (Status) is decremented, and Counter # 1 (Write Address Generation) remains unchanged.

MEMORY LENGTH

LS1	LS2	HALF LENGTH	FULL LENGTH
L	L	2048	4096
H	L	32	64
L	H	512	1024
H	H	128	256

CONTROL LOGIC

To prevent the possibility of operational conflicts, \overline{SI} and \overline{SO} are treated on a first-come/first-served basis; these two input signals are controlled by internal arbitration logic — refer to the applicable **Timing Diagrams** and **AC Characteristics** for functional and timing relationships. If one cycle is requested while the other cycle is in progress, the requested cycle will commence as soon as the current-cycle is complete (provided other control parameters are satisfied).

As shown in the accompanying diagram, the buffer length of the FIFO memory can be hardware-selected via the Length Select ($LS1, LS2$) Inputs. When less than the maximum length is selected, the unused high-order bits of the address outputs are held in the high-impedance state.

Generation of the status output signals (**HALF FULL**, **FULL** and **EMPTY**) is a function of the Length Select ($LS1, LS2$) inputs and the current state of Status Counter # 3. In general, the status outputs reflect the conditions that follow:

- **HALF FULL** — this status output signals goes **high** on the positive-going edge of \overline{SI} if the MSB of the selected length of Counter # 3 becomes a "1". The **HALF FULL** signal will go from **high-to-low** on the positive-going edge of \overline{SO} when,

after the **read** cycle, the selected length of Counter # 3 changes from "100 ... 00" to "011 ... 11". For example, if the selected memory length is 256 words (**FULL** = 256), then **HALF FULL** = 128 words; hence, on the positive-going edge of \overline{SO} when Counter # 3 reaches a count of 127, the **HALF FULL** output will go from **high-to-low**.

- **FULL** — this signal serves both as a status output and as an override input. The **FULL** signal goes **high** on the negative-going edge of \overline{SI} if all bits of Counter # 3 for selected length are equal to "1". The **FULL** output goes from **high-to-low** on the negative-going edge of \overline{SO} .
- **EMPTY** — this signal also serves as a status output and as an override input. On the negative-going edge of \overline{SO} , the **EMPTY** output is driven **high** if Status Counter # 3 contains a value of "1"; on the positive-going edge of \overline{SO} , the counter is decremented to "0". The **EMPTY** output goes from **high-to-low** on the negative-going edge of \overline{SI} .

Once the **FULL** signal is **high**, further Write Cycle Requests (\overline{SI} = low) are ignored; similarly, once the **EMPTY** signal is **high**, further Read Cycle requests (\overline{SO} = low) are ignored. However, to accommodate diversified applications, the **FULL** and **EMPTY** outputs are

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open-collector with on-chip 4.7K passive pull-up resistors. If either the FULL or EMPTY pins are forced **low** via external control, the corresponding **write** or **read** cycle may resume (provided the external FULL or EMPTY input is held **low** until the corresponding **WRITE** or **READ** output goes **low**) and the address/status counters will continue normal operation* — refer to Table 1.

The user must force the **RESET** input **low** to initialize the chip. (**Note.** If the **RESET** signal is driven **low** during a **write** or **read** cycle, the

address output may have a short period of uncertainty before assuming a high-impedance state.) The following actions occur when **RESET** is active:

- All internal counters are set to "0".
- All address output lines are forced to the high-impedance state.
- HALF FULL and FULL outputs are forced **low**.
- **WRITE**, **READ**, and **EMPTY** outputs are forced high.

When **CE** is **high**, the address output lines are forced to the high-impedance state, further **write** or **read** cycle requests are ignored, and all counters remain unchanged. If **CE** switches from **low-to-high** during a **write** or **read** cycle, the cycle in progress is always completed before the disabled state is entered. For details of these operations, refer to the timing information shown later in this data sheet.

*Refer to **Note** on inside back cover

Table 1. Summary of Operation

INPUTS				INITIAL CONDITIONS	RESULTING OUTPUTS			COMMENTS
RESET	CE	SI	SO		WRITE	READ	Address Bus	
L	X	X	X		H	H	Hi-Z	Reset all counters to 0.
H	X	H	H		H	H	Hi-Z	No action
H	L	L	H	FULL = L	L	H	Write address from Ctr #1	Shift into FIFO stack (Write Cycle)
H	L	L	H	FULL = H	H	H	Hi-Z	Stack full (write inhibited)
H	L	H	L	EMPTY = L	H	L	Read address from Ctr #2	Shift out of FIFO stack (Read Cycle)
H	L	H	L	EMPTY = H	H	H	Hi-Z	Stack empty (read inhibited)
H	L	L	↓	Write cycle in progress	L	H	Write address from Ctr #1	Continue write cycle (until \overline{SI} goes high)
H	L	↓	L	Read cycle in progress	H	L	Read Address from Ctr #2	Continue read cycle (until \overline{SO} goes high)
H	L	L	L	EMPTY = H	L	H	Write address from Ctr #1	Shift in (read inhibited)
H	L	L	L	FULL = H	H	L	Read address from Ctr #2	Shift out (write inhibited)
H	L	↑	H	Write cycle in progress	↑	H	Goes to Hi-Z	Increment write address counter #1 and status counter #3
H	L	H	↑	Read cycle in progress	H	↑	Goes to Hi-Z	Increment read address counter #2; decrement status counter #3
H	L	↑	L	Write cycle in progress ¹	↑	↓	Changes to read address from Ctr #2	Increment write address counter #1 and status counter #3
H	L	L	↑	Read cycle in progress ²	↓	↑	Changes to write address from Ctr #1	Increment read address counter #2; decrement status counter #3
H	H	↓	H		H	H	Hi-Z	Chip disabled
H	H	H	↓		H	H	Hi-Z	Chip disabled
H	↑	L	X	FULL = L; write cycle begun ¹	L	H	Write address from Ctr #1	Continue write cycle (until \overline{SI} goes high)
H	↑	X	L	EMPTY = L; read cycle begun ²	H	L	Read address from Ctr #2	Continue read cycle (until \overline{SO} goes high)
H	↓	L	L	FULL = L; EMPTY = L	-	-	-	This set of conditions should be avoided

NOTES:

1. Write cycle will occur if either \overline{SI} goes **low** before \overline{SO} goes **low** or EMPTY = H when \overline{SO} goes **low**.
2. Read cycle will occur if either \overline{SO} goes **low** before \overline{SI} goes **low** or FULL = H when \overline{SI} goes **low**.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power supply voltage	+7	V _{DC}
V _{BB} Supply voltage for internal circuits	+4	V _{DC}
V _{IN} Input voltage	+5.5	V _{DC}
V _O Off-state output voltage	+5.5	V _{DC}
T _{STG} Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS Conditions: Commercial — V_{CC} = 5.0V (±5%), V_{BB} = 1.5V (±5%)¹, 0°C ≤ T_A ≤ 70°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ²	Max	
V _{IH} High level input voltage ³		2.0			V
V _{IL} Low level input voltage				0.8	V
V _{OH} High level output voltage: All outputs except FULL and EMPTY	V _{CC} = MIN; I _{OH} = -2.6mA	2.7	3.5		V
V _{OL} Low level output voltage: Address Bus, WRITE, READ	V _{CC} = MIN; I _{OL} = 16mA		0.38	0.5	V
	HALF FULL, FULL, and EMPTY		0.35	0.5	V
V _{CD} Diode clamp voltage: All inputs except FULL and EMPTY	V _{CC} = MIN; I _{CD} = -18mA	-1.5	-0.8		V
I _{IH} High level input current: All inputs except FULL and EMPTY	V _{CC} = MAX; V _{IH} = 2.7V		0.1	20	μA
	FULL and EMPTY		-470	-750	μA
I _{IL} Low level input current: All inputs except FULL and EMPTY	V _{CC} = MAX; V _{IL} = 0.4V		-0.17	-0.4	mA
	FULL and EMPTY		-1.12	-1.8	mA
I _{OH} High level output current: FULL, EMPTY	V _{CC} = MIN; V _{OH} = V _{CC} (min)		15	100	μA
I _{OZH} High-Z output current (HIGH); address bus (Three-state)	V _{CC} = MAX; V _{OUT} = 2.4V		0.9	20	μA
I _{OZL} High-Z output current (LOW); address bus (Three-state)	V _{CC} = MAX; V _{OUT} = 0.5V		-0.6	-20	μA
I _I Input leakage current: All inputs except FULL and EMPTY	V _{CC} = MAX; V _{IN} = 5.5V		0.03	0.1	mA
I _{OS} Short-circuit output current: address bus and HALF FULL	V _{CC} = MAX; V _{OH} = 0V	-15	-68	-100	mA
	WRITE, READ	-40	-73	-100	mA
I _{CC} Supply current from V _{CC}	V _{CC} = MAX; Address 0°C → Bus = High-Z 70°C →		81	140	mA
			81	110	
I _{BB} Supply current from V _{BB}	V _{BB} = MAX 0°C → 70°C →		63	95	mA
			63	85	

NOTES:

1. V_{BB} can be obtained from a regulated 1.5V supply; alternately, proper supply current (I_{BB}) can be obtained by connecting a 56Ω (± 5%, 0.5W) resistor in series with V_{CC} as shown later in the APPLICATIONS diagram.

2. Typical limits are: V_{CC} = 5.0V; T_A = 25°C.

3. Because of the internal pull-up resistor on the FULL and EMPTY pins, a negative current is required to force the required voltage.

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AC ELECTRICAL CHARACTERISTICS Conditions: Commercial — $V_{CC} = 5.0V (\pm 5\%)$, $V_{BB} = 1.5V (\pm 5\%)$, $0^\circ C \leq T_A \leq 70^\circ C$

PARAMETERS	REFERENCES		TEST CONDITIONS	LIMITS			UNIT
	From	To		Min	Typ	Max	
Pulse widths:							
T_{LH} \overline{SI} high	$\uparrow \overline{SI}$	$\downarrow \overline{SI}$	Stack approaching FULL ¹	25	13		ns
T_{DH} \overline{SO} high	$\uparrow \overline{SO}$	$\downarrow \overline{SO}$	Stack approaching EMPTY ¹	30	16		ns
Write cycle timing:							
T_{LA} Address stable delay	$\downarrow \overline{SI}$	An	FULL = Low; \overline{SO} = High		40	55	ns
T_{AW} Address lead time	An	$\downarrow \overline{WRITE}$		3			ns
T_{LAW} \overline{WRITE} output active delay	$\downarrow \overline{SI}$	$\downarrow \overline{WRITE}$	FULL = Low; \overline{SO} = High	35	51	65	ns
T_{LW} \overline{WRITE} output inactive delay	$\uparrow \overline{SI}$	$\uparrow \overline{WRITE}$			3	10	ns
T_{WA} Address lag time	$\uparrow \overline{WRITE}$	An		20	34		ns
T_{LT} Address output disable	$\uparrow \overline{SI}$	An (Hi-Z)			37	60	ns
T_{LF} FULL status active delay	$\downarrow \overline{SI}$	$\uparrow \overline{FULL}$	Stack approaching FULL; \overline{SO} = High		39	65	ns
T_{LE} EMPTY status inactive delay	$\downarrow \overline{SI}$	$\downarrow \overline{EMPTY}$	Stack = EMPTY		40	65	ns
T_{HFH} HALF-FULL status active delay	$\uparrow \overline{SI}$	$\uparrow \overline{HALF FULL}$	Stack approaching HALF-FULL		30	45	ns
T_{DW} \overline{WRITE} output active after read	$\uparrow \overline{SO}$	$\downarrow \overline{WRITE}$	Both \overline{SI} & \overline{READ} = Low		74	95	ns
Read cycle timing:							
T_{DA} Address stable delay	$\downarrow \overline{SO}$	An	EMPTY = Low; \overline{SI} = High		40	55	ns
T_{AR} Address lead time	An	$\downarrow \overline{READ}$		-1			ns
T_{DAR} \overline{READ} output active delay	$\downarrow \overline{SO}$	$\downarrow \overline{READ}$	EMPTY = Low; \overline{SI} = High	30	48	65	ns
T_{DR} \overline{READ} output inactive delay	$\uparrow \overline{SO}$	$\uparrow \overline{READ}$			5	10	ns
T_{RA} Address lag time	$\uparrow \overline{READ}$	An		20	32		ns
T_{DT} Address output disable	$\uparrow \overline{SO}$	An (Hi-Z)			37	60	ns
T_{DE} EMPTY status active delay	$\downarrow \overline{SO}$	$\uparrow \overline{EMPTY}$	Stack approaching EMPTY; \overline{SI} = High		38	50	ns
T_{DF} FULL status inactive delay	$\downarrow \overline{SO}$	$\downarrow \overline{FULL}$	Stack = FULL		38	50	ns
T_{HFL} HALF-FULL status inactive delay	$\uparrow \overline{SO}$	$\downarrow \overline{HALF FULL}$	Stack exactly HALF-FULL		54	75	ns
T_{LR} \overline{READ} output active after write	$\uparrow \overline{SI}$	$\downarrow \overline{READ}$	Both \overline{SO} & \overline{WRITE} = Low		70	90	ns
Chip enable timing (write):							
T_{HEW} Chip enable hold time ²	$\downarrow \overline{SI}$	$\uparrow \overline{CE}$	FULL = Low; \overline{SO} = High	10	1		ns
T_{SEW} Chip disable set-up time ³	$\uparrow \overline{CE}$	$\downarrow \overline{SI}$	FULL = Low; \overline{SO} = High	10	1		ns
T_{PEW} Chip enable delay time	$\downarrow \overline{CE}$	$\downarrow \overline{WRITE}$	FULL = Low; \overline{SI} = Low; \overline{SO} = High		69	95	ns
Chip enable timing (read):							
T_{HER} Chip enable hold time ²	$\downarrow \overline{SO}$	$\uparrow \overline{CE}$	EMPTY = Low; \overline{SI} = High	10	1		ns
T_{SER} Chip disable set-up time ³	$\uparrow \overline{CE}$	$\downarrow \overline{SO}$	EMPTY = Low; \overline{SI} = High	10	1		ns
T_{PER} Chip enable delay time	$\downarrow \overline{CE}$	$\downarrow \overline{READ}$	EMPTY = Low; \overline{SO} = Low; \overline{SI} = High		64	95	ns
Reset timing:							
T_{RR} RESET recovery	$\uparrow \overline{RESET}$	$\downarrow \overline{WRITE}$	\overline{SI} = Low		57	75	ns
T_{RL} RESET pulse width (low)	$\downarrow \overline{RESET}$	$\uparrow \overline{RESET}$		25	8		ns
Full/empty override timing:							
T_{FW} Override Recovery for FULL	$\downarrow \overline{FULL}$	$\downarrow \overline{WRITE}$	Stack = Full; \overline{SI} = Low; \overline{SO} = High		70	95	ns
T_{ER} Override Recovery for EMPTY	$\downarrow \overline{EMPTY}$	$\downarrow \overline{READ}$	Stack = EMPTY; \overline{SO} = Low; \overline{SI} = High		65	90	ns

NOTES:

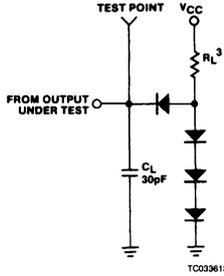
- Such that write/read request is inhibited after stack becomes full/empty.
- The earliest rising edge of \overline{CE} such that the \overline{WRITE} or \overline{READ} output always occurs.
- The latest rising edge of \overline{CE} such that the \overline{WRITE} or \overline{READ} output never occurs.

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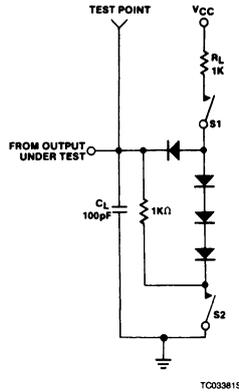
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TEST LOADING CIRCUITS

APPLICABLE PINS: WRITE (7),
READ (8), HALF FULL (10)



APPLICABLE PINS:
An (15 - 20, 22 - 27)

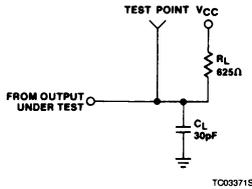


OUTPUT STATE		SWITCH POSITION	
FROM	TO	S1	S2
Low	High	Closed	Closed
High	Low	Closed	Closed
High	HI-Z	Closed	Closed
Low	HI-Z	Closed	Closed
HI-Z	High	Open	Closed
HI-Z	Low	Closed	Open

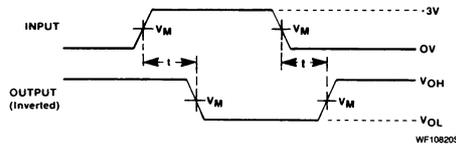
NOTES:

1. In all cases C_L includes probe and jig capacitance
2. All diodes are 1N916, 1N3064, or equivalent.
3. For READ and WRITE outputs, $R_L = 280$ ohms; for HALF FULL output, $R_L = 2K$ ohms.

APPLICABLE PINS: FULL (8)
AND EMPTY (11)



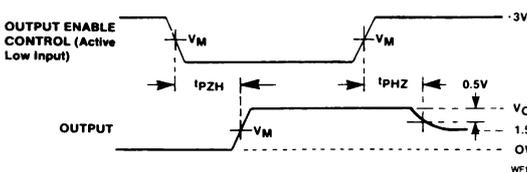
AC TEST WAVEFORMS



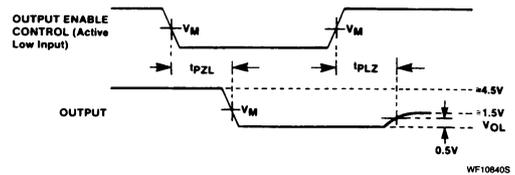
Propagation Delay
(Typical Example)

NOTE:

Pulse widths and Set-up/Hold times are measured using the same reference points as above waveform.



**3-State Enable Time to LOW Level
and Disable Time From LOW Level**



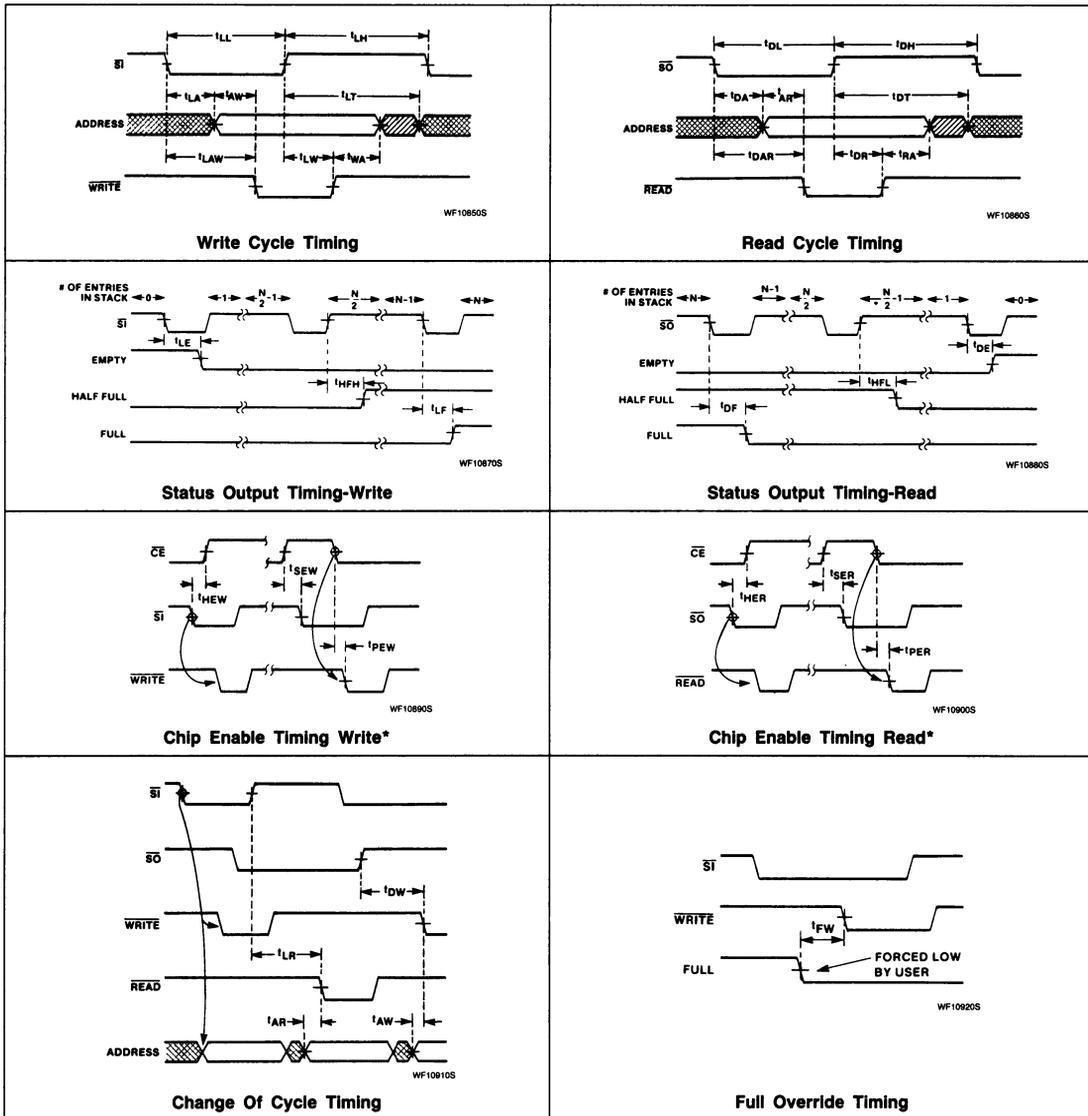
**3-State Enable Time to HIGH Level
and Disable Time From HIGH Level**

For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74LS.

FIFO RAM Controller (FRC)

8X60

TIMING DIAGRAMS

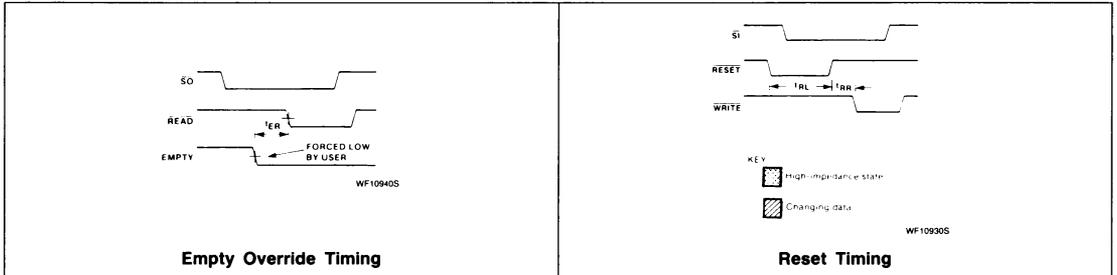


*The rising edge of \overline{CE} should not occur within 10-nanoseconds before or after a falling edge of \overline{SI} or \overline{SO} .

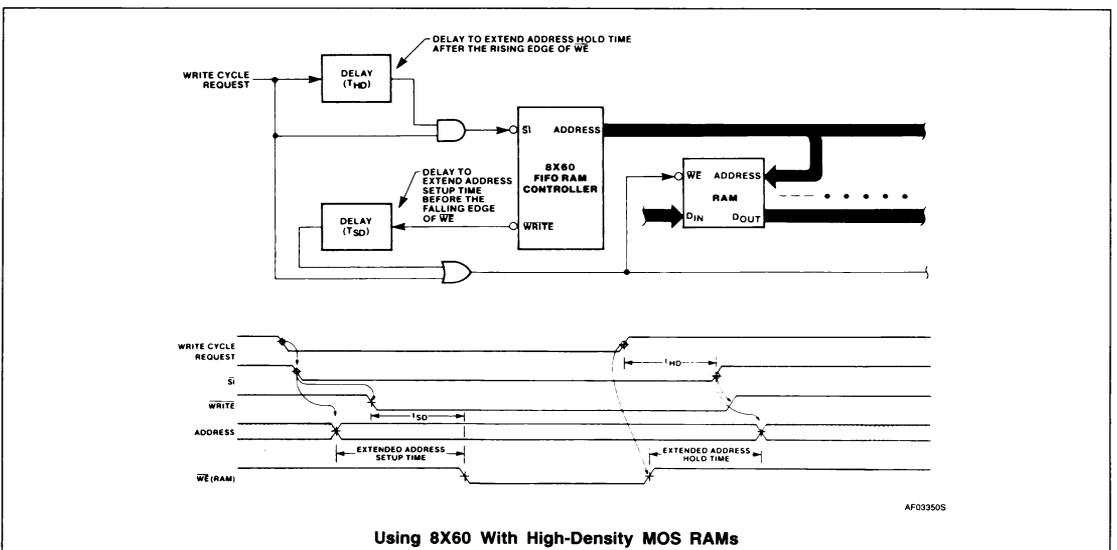
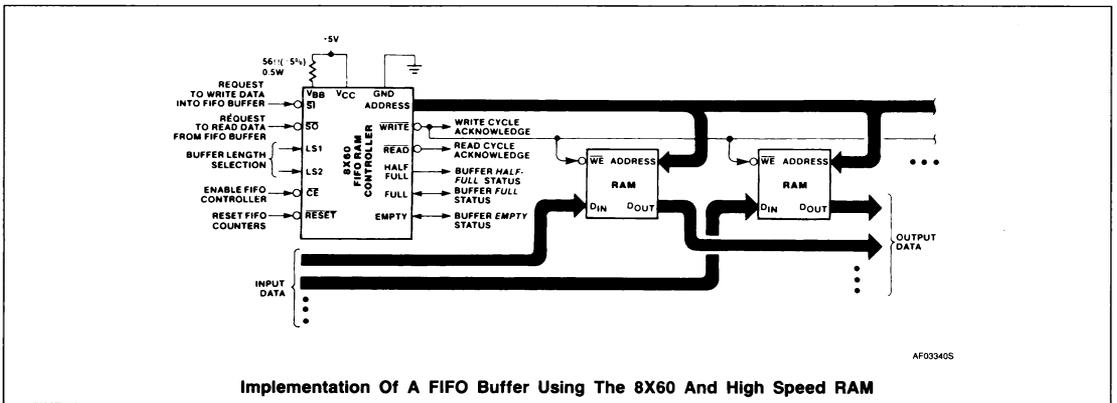
FIFO RAM Controller (FRC)

8X60

TIMING DIAGRAMS (Continued)



APPLICATIONS



Logic Products

INTRODUCTION

Economic survival is driving the electronics industry to use cheaper, faster, more reliable and more dense systems and components. Assembly technologies, such as SMD (Surface Mounted Device) technology, developed and used in hybrids and for military electronics for over two decades, is being adapted to commercial electronics as part of this evolution. With SMD technology, components are soldered directly to a metalized footprint on the surface of the board or substrate rather than being inserted through holes drilled in the board and then soldered. Because of this evolution, package styles specially designed to facilitate surface mounting are now in high demand.

The reasons for the change to SMD technology vary from one customer to another; but the primary motivator is higher profits through lower manufacturing and material costs, or an improved product, or both.

Improved Electrical Performance

Because SMD packages are much smaller than their DIP counterparts, they have much less capacitance and inductance, and provide improved AC performance, especially in high-speed environments. They help to minimize problems associated with ground bounce and multiple output switching found with standard DIP packages. The SO package is especially suitable for high-speed families such as FAST and High-Speed CMOS where package inductance can induce or compound problems not normally found in slower technologies.

Ease Of Automation

SMD pick-and-place machines offer higher yields, faster cycle rates (3 - 10x faster), and much higher throughput volumes than automatic insertion machines for DIP packages.

Greatly Increased Densities

Greatly increased densities can be achieved through surface mounting. The packages themselves are much smaller (as much as 70%) and can be placed much closer together. Furthermore, both sides of the board can be used with SMDs.

Reduced Board Costs

The number of layers, total size of the board and the number of plated through holes can be reduced, thus lowering the total cost of the board (many companies claim savings of 30 to 50%).

Easier Board Rework

In those instances where rework is necessary, it is much faster and cheaper with SMDs.

Improved Reliability

Not only are the components proving to be at least as reliable as their DIP counterparts, but surface mounted assemblies show fewer failures in stress tests than equivalent through hole assemblies.

Lower Shipping, Storage And Handling Costs

SMD components are up to 70% smaller and weigh up to 90% less than DIPs (up to 95% savings in storage area for Tape & Reel SMD components vs DIPs and up to 90% savings in component weight). Surface mount assemblies offer additional savings in both weight and space, both of which can be linked to increased profits.

SMD packages for integrated circuits fall into two categories: Swiss Outline also known as Small Outline (SO) and the Plastic Leaded Chip Carrier (PLCC).

SO PACKAGE

The SO package was developed by N.V. Philips Corp, originally for the Swiss watch industry. In the mid 1970s Signetics introduced linear ICs in SO packages to the US market (hybrid and telecommunications). As demand grew, other technologies such as FAST, Low Power Schottky, Schottky, TTL, CMOS, High-Speed CMOS (HC and HCT),

ECL, ROMs, RAMs, PROMs, were made available in SO packages.

The SO is a dual-in-line plastic package with leads spaced 0.050" apart and bent down and out in a Gull-Wing format. It comes in two widths: 0.150" SO, and 0.300" SOL (SO-Large) depending on the pin count.

As ICs became more complex and the number of pins grew, the standard dual-in-line packages grew longer and wider, presenting new electrical and mechanical problems. Some of these were resolved with the introduction of the ceramic leadless chip carrier (LCC). These were square, ceramic packages without leads which can be socketed or soldered directly to a substrate if the thermal coefficient of expansion of the chip carrier and the substrate are matched.

In 1980, the Plastic Leaded Chip Carrier (PLCC) was introduced as a cheaper alternative to the LCC. However, this was at the same time that SMD was winning acceptance in commercial electronics and the PLCC was seen as an ideal SMD package for the higher pin count devices (those with more than 28 leads). The PLCC is a square, plastic package with leads on four sides, spaced down and under in a J-Bend configuration. It is available in the higher pin counts: 20, 28, 44, 52, 68, 84 with even higher pin counts under development.

The smallest square PLCC is the 20 pin package. There are many reasons for this; the primary one is that below 20 pins, the package would be as thick as it is square,

Table 1

PIN COUNT	SO	SOL	PLCC
8	x		
14	x		
16	x	x	
18		x	x (rectangular)
20		x	x
24		x	
28		x	x
44			x
52			x
68			x
84			x

Surface Mounted ICs

Table 2. Maximum Thermal Resistance (θ_{JA}) Values for SMD Packages ($^{\circ}\text{C}/\text{W}$)

PINS	SO	SOL	PLCC
8	160		
14	115		
16	110	90	
20		85	70
24		75	
28		70	60
44			42
52			39
68			42
84			32

NOTE:

For more detailed information see Application Note SMD100 entitled "Thermal Considerations For Surface Mounted Devices" contained in the Application Note section of this data manual.

resulting in a cube-like package which would be very difficult to handle in an automated environment.

Logic and linear devices are available in SO while the more complex parts such as Micro-processors, Microcontrollers, Complex Peripherals, large memory devices, and other higher pin count integrated circuits will be found in the PLCC.

ASSEMBLY

The assembly of these SMD packages is virtually the same as for the older DIP packages using the same materials and most of the same equipment and assembly technologies.

The only differences in the process are the smaller lead frames, different lead bends (gull-wing for SO and J-Bend for the PLCC), and closer spacing resulting in a much smaller package for the same basic die.

RELIABILITY

Reliability studies of SMD components, conducted not only by Signetics and Philips, but many of our competitors and our customers have revealed that these packages are at least as reliable as the standard plastic DIP packages that have been used over the past 20 years. In several cases, test results of the SMD packages have been better than their DIP counterparts.

THERMAL CHARACTERISTICS

Thermal characteristics of ICs have always been a major consideration to producers and users of electronics products because an increase in junction temperature (T_J) can have an adverse effect on the long term operating life of an IC. The advantages realized by miniaturization have trade-offs in terms of increased junction temperatures. Some of the variables affecting T_J are controlled by the producer of the IC, while others are controlled by the user and the environment in which the device is used.

With the increased use of SMD, thermal management remains a valid concern because not only are the packages much smaller, but the thermal energy is concentrated much more densely on the PCB. For these reasons users of SMD must be more aware of all the variables affecting T_J .

Power Dissipation

Power dissipation (P_D) varies from one device to another depending on technology and complexity. It can be obtained by multiplying V_{CCmax} by the I_{CC} characterized at the maximum ambient temperature expected (in the case of TTL, 70°C).

- Junction temperature (T_J) is the temperature of a powered IC measured at the substrate diode. When the device is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A).
- All standard TTL, Schottky, Low Power Schottky, and FAST being built by Signetics use copper leadframes.
- The ability of the package to conduct heat from the chip to the environment is expressed in terms of thermal resistance, normally called Theta JA (θ_{JA}). θ_{JA} is the total resistance from the junction to ambient and is often separated into two components: θ_{JC} (junction to case) and θ_{CA} (case to ambient). $\theta_{JA} = \theta_{JC} + \theta_{CA}$. θ_{JA} values for SMD packages are listed in Table 2.
- All measurements are in still air.
- T_A max is $+70^{\circ}\text{C}$.
- I_{CC} characterized at nominal V_{CC} and $+70^{\circ}\text{C}$ ambient.
- Calculate power (P) by multiplying V_{CC} nominal x I_{CC} at $+70^{\circ}\text{C}$.
 $P = I_E$
- Calculate rise in (T_J) by multiplying Power by θ_{JA} .
 $T_J = P \times \theta_{JA}$
- Add $T_J + T_A$ max. If result is greater than 120°C , then thermal mounting or some other way to reduce the T_J must be used.

Factors Affecting Thermal Resistance

In addition to possible loading and duty cycle factors in some technologies, there are several factors which affect θ_{JA} of any IC package. Effective thermal management demands a sound understanding of all these variables.

Package variables include the leadframe design, leadframe material, the plastic used to encapsulate the device, and to a lesser extent, other variables such as the die size and die attach methods. While the thermal conductivity of the wire can be calculated, it is too insignificant to be considered as a factor.

Other factors that have a significant impact on the θ_{JA} include the substrate upon which the package is mounted, the density of the layout, the gap between the package and substrate, the number and length of traces on the surfaces of the board, the use of thermally conductive epoxies, and any external cooling methods.

STANDARDIZATION

The SO package is an industry standard format. In June 1985, the JEDEC (Joint Electronics Engineering Council) of the EIA (Electronics Industries Association) issued a Solid State Product Outlines Standard for each of the SO formats: MS-012 AA-AC for the 0.150" body width SO and MS-013 AA-AE for the 0.300" body width SOL. In addition to the JEDEC Standard, de facto standardization has been achieved in the industry in that most of the major US and European IC manufacturers (more than 15 companies currently) use this standard.

The PLCC is also a standardized format, with a JEDEC Registered Outline #MO-047 AA-AH. It also is multiple sourced with over 10 US IC manufacturers using this standard.

Points worth noting: ALL SO AND SOL PACKAGES HAVE 0.050" LEAD SPACING AND A GULL-WING LEAD BEND, WHILE ALL PLCC PACKAGES HAVE THE SAME LEAD SPACING AND A J-BEND LEAD BEND.

TAPE AND REEL

One revolutionary trend in SMD is the development of Tape and Reel for the IC packages. Philips and several other companies making automatic placement equipment recognized the need for a feed system which allows for positive indexing large volumes of components at high-speed in order to get maximum efficiency out of the new pick-and-place machines. Tubes are limited to a relatively small number of parts (dictated by tube length) and depend on gravity to feed components to the placement head. After several

Surface Mounted ICs

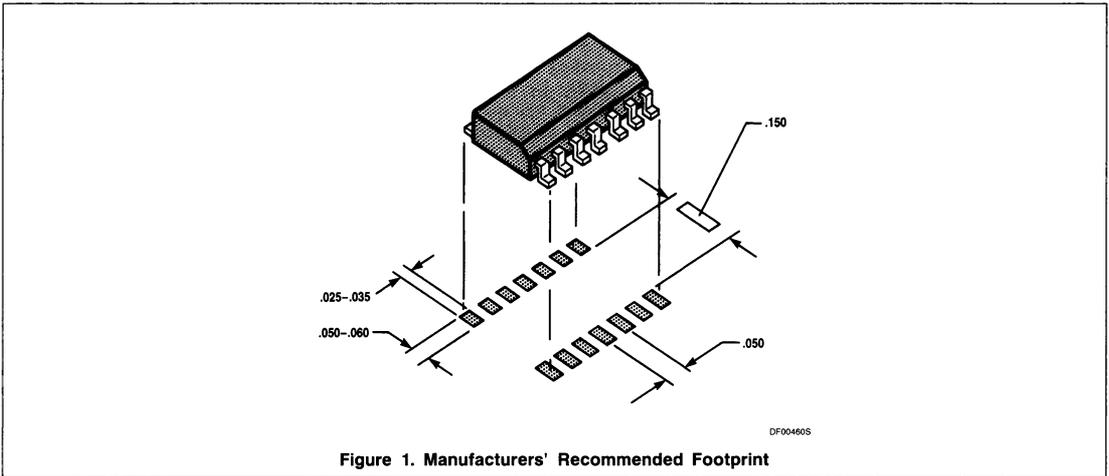


Figure 1. Manufacturers' Recommended Footprint

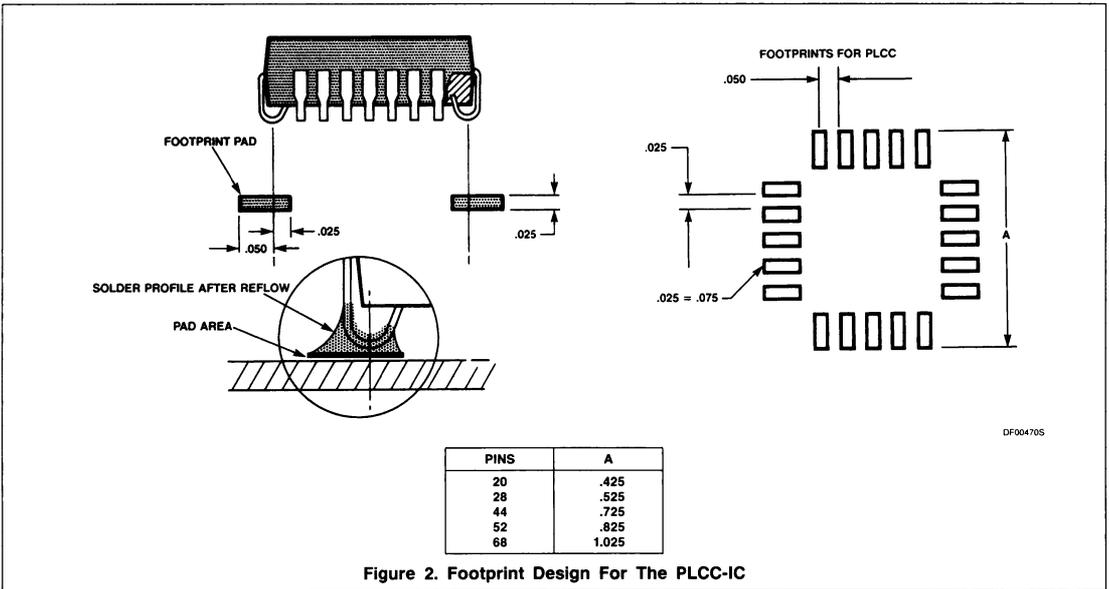


Figure 2. Footprint Design For The PLCC-IC

Surface Mounted ICs

proposed tape formats, Philips, Signetics, many of the component and placement equipment manufacturers, and board manufacturers convened under the auspices of EIA (Electronic Industries Association) and agreed on an industry standard specification for Tape and Reel for both SO and PLCC packages. The proposed EIA specification RS 481A is being used by Signetics and Philips, both of whom have shipped components on Tape and Reel since late 1984.

SUCCESS IN SURFACE MOUNTING BEGINS WITH THE DESIGNER

In addition to the different package configurations, surface mounting is done on a much smaller scale. Instead of the plated through holes, metallized footprints must be etched onto the substrate surface.

The designer will be using a more refined set of rules for layout of the surface mount PC board. Because the components can be spaced closer together with small contact spacing, a narrower conductor trace width is necessary. A common signal conductor can be 0.010" to 0.012" wide and 0.015" through 0.030" is adequate for power and ground bussing. The suggested footprint contact area has a generous tolerance. For the SO I.C., a rectangular pattern is used on 0.050" spacing. The length of the pad is 0.050" to 0.060" and the width can vary from 0.020" to 0.035". The 0.025" x 0.050" footprint pattern will work well using the grid placement system favored by most designers. The 0.012" conductor width spaced at 0.025" provides a reasonable 0.013" air gap between traces. However, if conductor traces are routed between contact pads, it will be necessary to neck down the trace width to 0.008" and still retain an equal airgap at each side. Because neck down traces require additional time in both hand taping or CAD/photo plot generation of artmasters, some compromises may be justified. By reducing the contact pad size

to 0.020" x 0.050", it is possible to route a consistent 0.010" conductor trace width and still maintain the desired clearances. However, some PC board shops may not maintain the consistent quality necessary when using this fine line approach over the entire board. It is important to discuss limitation and premium cost penalties with your supplier before full commitment to the 0.010", and smaller, trace widths.

Another very important consideration to be taken into account is the thermal concentration caused by miniaturization. The same die is being used in the SMD as in the DIP, thus the power dissipated is the same; however, the smaller packages are being placed much closer together, concentrating the thermal energy. The trade-offs between the increase in density and the concentration of thermal energy must be evaluated by the board manufacturer.

These factors may influence the choice of PCB material, the number of layers, and the thickness of the PCB board. New methods to transfer heat from the package to the board and then away from the board should be considered by the designer.

Other factors to be considered are the placement system, soldering method, post-assembly cleaning, inspection, test, and the availability of parts in SMD packages.

One of the first steps is to list all the devices needed and to determine which ones are available in SMD format. With the growth of popularity of SMD, the number of different functions offered by Signetics continues to grow rapidly. In addition to the SIGNETICS SMD POCKET GUIDE, there are several cross-reference lists available from design and assembly services. However, with the explosive growth of this market NONE OF THESE LISTS ARE NECESSARILY CURRENT. Please check with your local sales office because the parts availability lists are growing almost daily.

When choosing the type of footprints to use, it is very important that the designer considers the soldering method being used.

Basically there are two types of soldering in use today: flow soldering (wave, drag, or hot solder dip) and reflow soldering (vapor phase, infrared, thermal conduction through the PCB, and hot air).

The SO package can be soldered using a flow soldering method. The devices must be attached to the PCB by means of an adhesive because the device side of the board will be facing down as it goes through the solder wave. The orientation of the part as it goes through the solder wave can play an important role in the elimination of bridges. Experiments should be conducted by the user to determine the best footprints for use in a particular soldering system. Some users feel that the narrower footprints help to reduce solder bridges. Others have been experimenting with rounded footprints to reduce bridging during wave soldering and claim to have had very good results.

Reflow soldering has been done for many years in the hybrid industry. A solder paste or solder cream is applied to the footprint prior to placement of the component. These pastes and creams contain tiny spheres of solder suspended in a carrier which contains the flux. As the substrate temperature is raised, the flux, solvents, and carriers are driven off and the solder liquifies. Various melting point pastes and creams are available. As the liquid solder migrates to the metallized footprints, the surface tension is enough to move the leaded components. For SO packages, this can be an advantage because it acts as a self-positioning mechanism. However, it can be a problem for the smaller passive components if the solder paste isn't printed on evenly. If there is an uneven amount of solder paste on one end of one of these smaller devices, the surface tension can pull stronger on one side causing

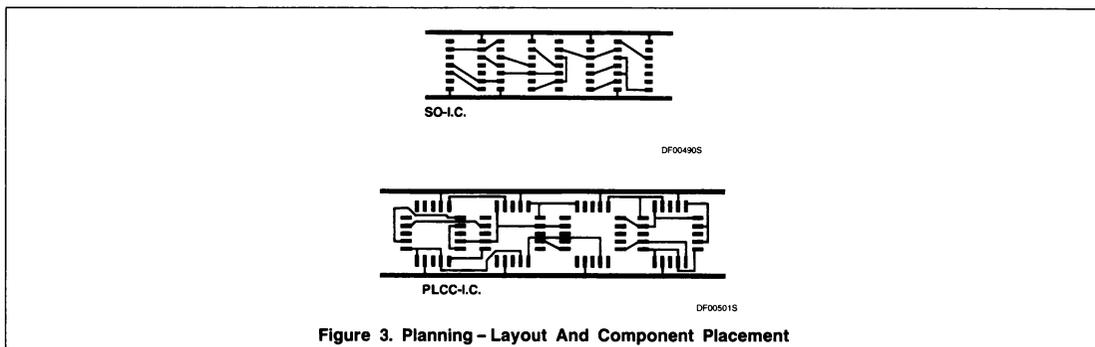
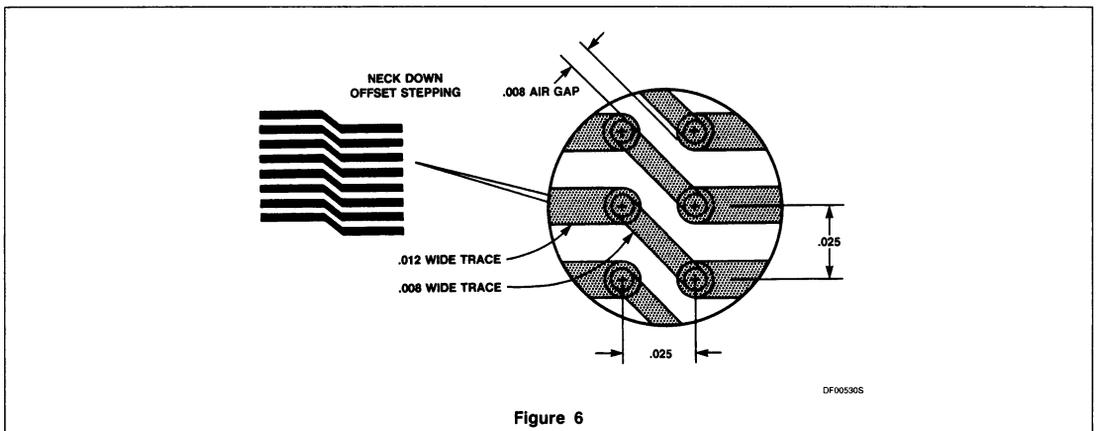
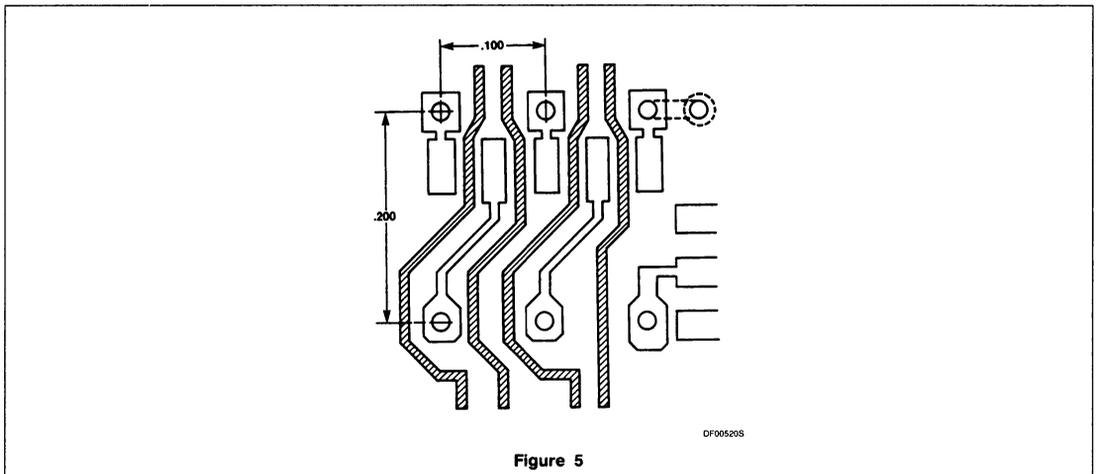
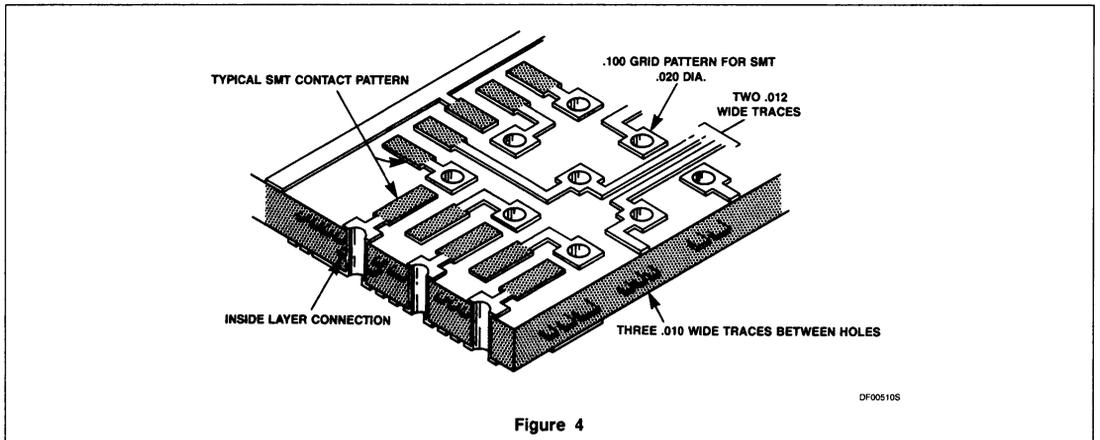


Figure 3. Planning - Layout And Component Placement

Surface Mounted ICs



Surface Mounted ICs

a "tombstoning" effect, i.e., one end of the device is lifted straight up.

Many variations of footprint patterns are possible. The formula shown in Figure 1 is applicable for both reflow and wave solder processes. Both configurations are possible and should be tried on an experimental basis before commitment to a large production run. Both time and development costs can be conserved by utilizing design and process consultants specializing in surface mount technology.

Figures 1 and 2 show some typical footprints used in reflow soldering. Note that the width of the footprint for the SO package varies from 0.025" to 0.035". Most users tend towards the narrow footprint. Further, the length of these prints should be kept as short as possible to prevent the part from swimming or sliding back and forth on the footprint while still allowing a good meniscus.

Another factor worth noting is that the footprint for PLCC should not extend too far under the package as this could promote solder bridges under the package where they can not be seen during inspection. The footprint for the PLCC should extend out further from the package than the lead itself to allow a good meniscus that will result in a strong, inspectable bond.

Careful placement of related components will allow a more effective use of a much smaller surface area. The interconnections that can be made on the substrate surface result in the elimination of feedthrough holes. Reduction of these holes and their associated pad areas further increase the density of the layout, and reduce total board cost as well. As indicated, the SO package has the same pinout on two parallel rows as found on the older DIP packages being replaced. Arranging related ICs in blocks or functional clusters with their associated discreet components can also help to maximize the use of the available surface area.

For several reasons, many users have expressed their preference for SO format through 28 pins. The SO is much smaller and lighter than the PLCC. The SOL, although a bit longer than the PLCC, still occupies about the same board space as you can see below.

Further, when using several packages and connecting them together, a given number of SO and SOL packages would take much less space than the same number of PLCCs, simply because of the interconnect geography. (See Figure 3).

Besides being smaller, the SO format is dual-in-line and has the same pinouts as those of a standard DIP (PLCC pinouts vary between devices as well as between manufacturers). The SO format is easier to handle and is much easier to visually inspect.

For devices over 28 pins, the PLCC is the package of choice, largely because it can hold a much larger die than the 0.300" wide SO packages.

In the early days of PCB technology when plated through holes were not possible, designers were forced to carefully plan component arrangements and connections. Using experience and ingenuity, they were able to eliminate crossovers while reducing the need for unwanted jumpers. With the advent of plated through holes and multilayer boards, the restriction to single sided boards was eliminated. Using the single sided concept the techniques used to interconnect the SMDs are as important as the footprint patterns. As noted before, the contact pads on 0.050" centers, range between 0.025" and 0.035" in width. Prior to choosing to add a feedthrough hole on the pad itself, two factors should be considered: 1) The hole diameter selected must allow for a reasonable location tolerance. A 0.010" to 0.015" diameter plated through hole in 0.062" thick FR4 material may increase the cost of your PCB. 2) Unless the feedthrough hole on the footprint area is either plugged or masked, in a reflow soldering situation, the solder will tend to migrate away from the IC contact resulting in a poor solder joint.

It is more desirable to add a separate pad for via or feedthrough requirements. To further provide for routing conductor traces while insuring an acceptable air gap, you may choose to use a 0.035" to 0.037" square pad for these feedthrough holes. The square configuration will furnish more than enough metal in the diagonal corners to compensate for the reduced annular cross section at the sides of the square. The 0.035" - 0.037" square feedthrough pad can be spaced at 0.050" when necessary or on the more traditional 0.100" pad. With this spacing it is possible to route two 0.012" wide conductor traces between pads, something only possible before with costly multilayer designs using leaded through hole technology.

The feedthrough pad is then connected to the component contact area with a narrow trace. This narrow trace reduces migration of the solder paste during the reflow process. To further reduce migration of the liquid solder,

application of solder mask coating over surface areas not requiring solder is recommended. This coating is applied with a wet screen process or photographically as a dry film and will act as a dam to contain solder to the contact area. (See Figures 4 and 5).

When using reflow soldering, the trace width should be about half the width of the footprint pattern. As noted before the signal carrying conductors are generally 0.012" to 0.015" wide. Supply voltages are carried on wider traces. When running traces between the device leads, it will be necessary to reduce the width to about 0.008" which provides an 0.008" gap between the trace and the edge of the pads when using 0.025" pads.

Because the SMDs are so much smaller than their leaded counterparts, the scale of the layout should be considered. On larger boards with a mix of SMDs and leaded devices, a 2:1 scale may be adequate. More complex layouts can be designed at 4:1 scale with excellent results. The larger scale will make it possible to increase density while assuring accuracy. If designing with a CAD system, accuracy and density can both be increased by increasing the grid resolution. Routing conductor traces will require careful planning, it is customary to use a 90° or 45° angle (Figure 6) when traces must divert from a continuous line.

Offset stepping several 0.012" wide conductor traces on 0.025" spacing will require necking down at the point of direction change to maintain the desired air gap. The start and stop points of photoplotter aperture runs must be carefully executed to reduce the chance of overlay and shorting. If outside services are used for digitizing or photoplotting, discuss your requirements for accuracy before proceeding. Some compromises may have to be made to ensure quality and control costs. Preparing artmasters on mylar using precision tape products and pre-printed footprint patterns may afford more flexibility during your entry into SMD technology. Changes can be made easily, and economical photo reduction processes will provide high quality working film. The technique used to prepare working film is a choice generally influenced by in-house capability or services available in a region.

Dramatic changes are taking place throughout this industry. Surface mount technology is key to an efficient transition into miniaturization and automation of electronic production.

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D Plastic Small Outline	9-6
N Plastic Standard Dual-In-Line	9-9

Logic Products

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

1. Dimensions are shown in Metric units (Millimeters) and English units (Inches).

2. Lead material: Copper Alloy, solder (63%Sn/37%Pb) dipped.
3. Body material: Plastic (Epoxy)
4. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated di-

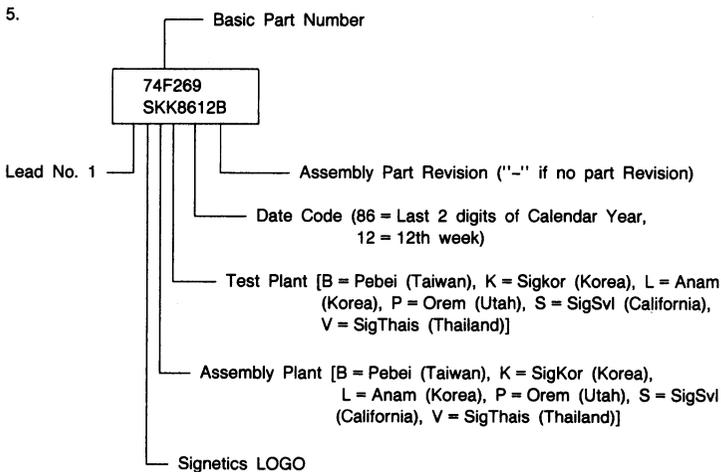
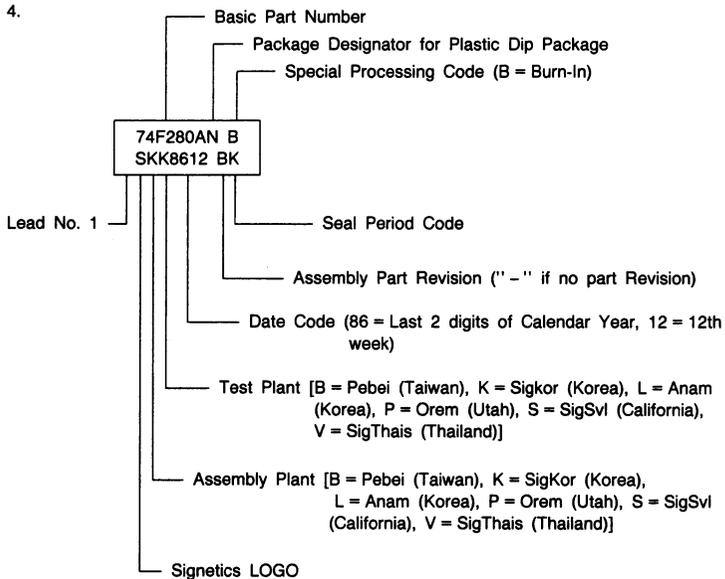
ode to measure the change in junction temperature due to a known power application. The substrate diode of a Bipolar technology device is generally the diode used in these tests. Die size and test environment have significant effects on thermal resistance values.

PLASTIC PACKAGES OUTLINES								
Package Type	Number of Leads	Package Feature	Package Ordering Code	Package Outline Code	Thermal Resistance $\theta_{JA/JC}$ ($^{\circ}C/W$)	Die Size (square mils)	Test Conditions	
							Test Ambient	Test Fixture
SO ¹ (Copper Leadframe)	14 pin (SO-14)	3.9mm (.15") Body width	D	DH1	124/37	2,500	Still air at room temperature	Device soldered to Philips glass epoxy test board (1.12" x .75" x .059") with .008 - .009" stand-off. Accuracy: $\pm 15\%$
	16 pin (SO-16)		D	DJ1	113/36			
	16 pin (SOL-16)	7.5mm (.30") Body width	D	DJ2	98/30	5,000		Device soldered to Philips glass epoxy test board (1.58" x .75" x .059") with .008 - .009" stand-off. Accuracy: $\pm 15\%$
	20 pin (SOL-20)		D	DL2	90/28			
	24 pin (SOL-24)		D	DN2	76/26			
	28 pin (SOL-28)		D	DQ2	70/24	10,000		
PLCC ² (Copper Leadframe)	44 pin (PLCC-44)	.650" Square body	A	AX1	50/20	15,000	Device soldered to Philips glass epoxy test board (2.24" x 2.24" x .062") with .008 - .009" stand-off. Accuracy: $\pm 15\%$	
DIP ³ (Copper Leadframe)	14 pin (DIP-14)	.300" Lead row centers	N	NH1	89/44	2,500	Still air at room temperature	Device in Textool ZIF socket with .040 inch, stand-off. Accuracy: $\pm 15\%$
	16 pin (DIP-16)		N	NJ1	86/43			
	20 pin (DIP-20)		N	NL1	74/32			
	24 pin SLIM DIP (DIP-24)	N	NN1	65/36	5,000	Device in Textool ZIF socket with .040 inch, stand-off. Accuracy: $\pm 15\%$		
	24 pin (DIP-24)	N	NN3	59/30				
	28 pin (DIP-28)	.600" Lead row centers	N	NQ3	52/27			10,000
	40 pin (DIP-40)		N	NW3	45/19			15,000

NOTES:

1. SO = Small Outline
2. PLCC = Plastic Leaded Chip Carrier
3. DIP = Dual-In-Line Package

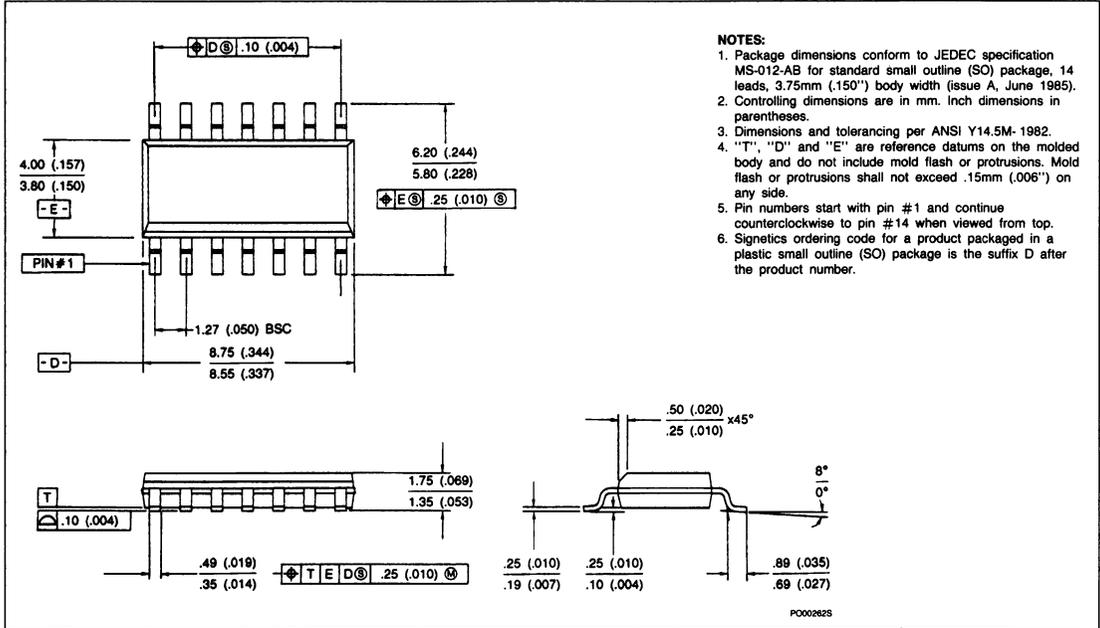
Package Outlines



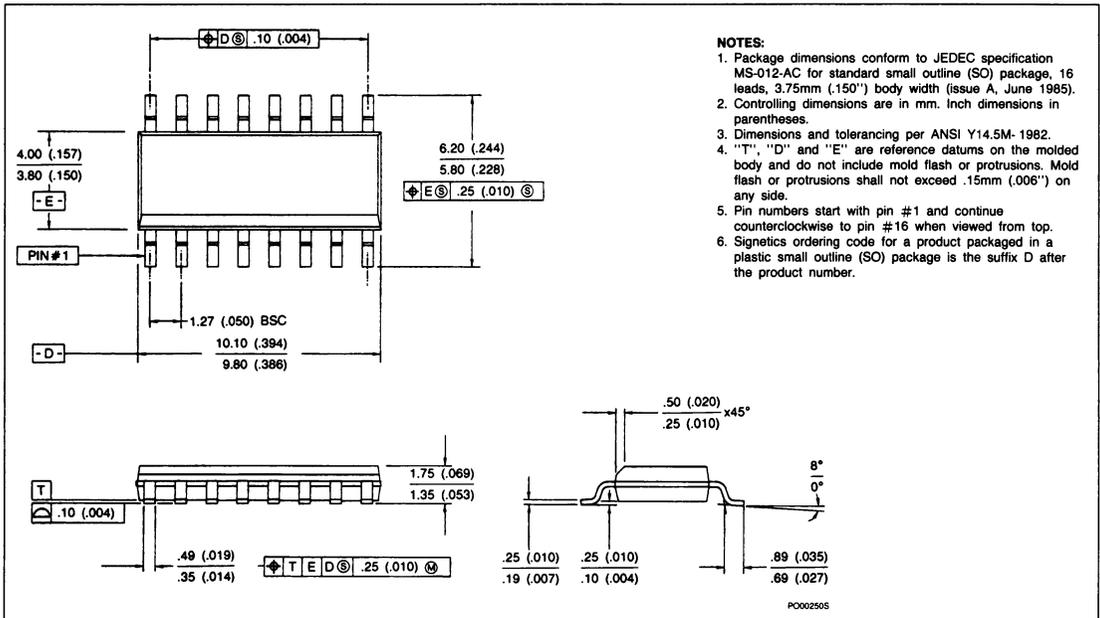
4. Package Symbolization for Plastic Dual-In-Line Package (DIP) Top Side
 5. Package Symbolization for Plastic Small Outline Package (SO) Top Side

Package Outlines

DH1/PLASTIC SO-14

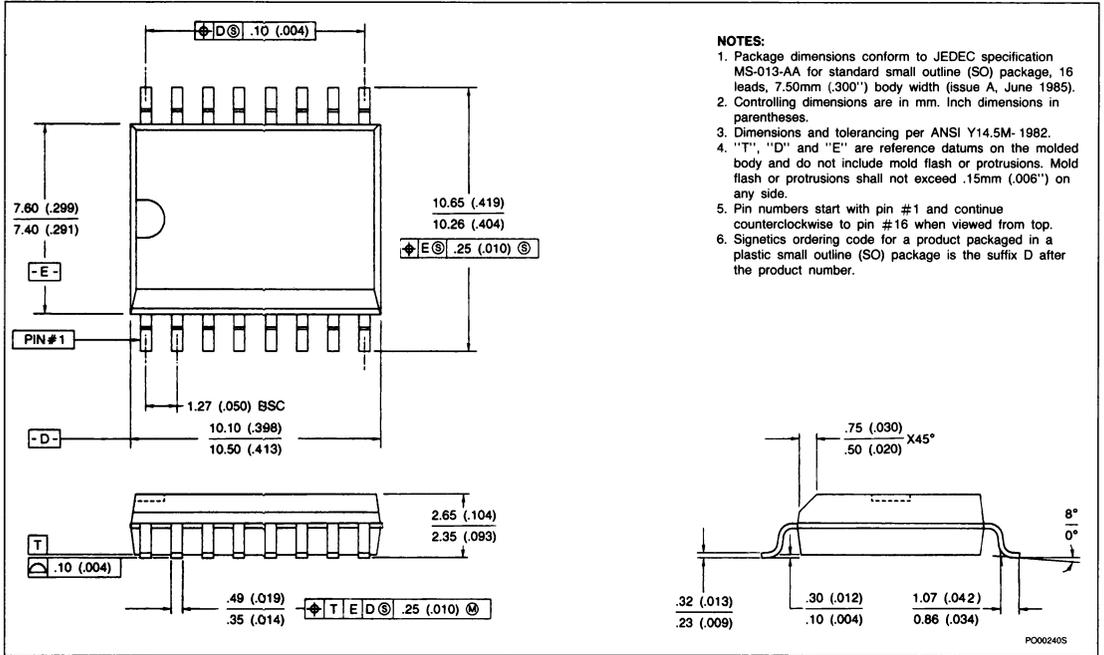


DJ1/PLASTIC SO-16

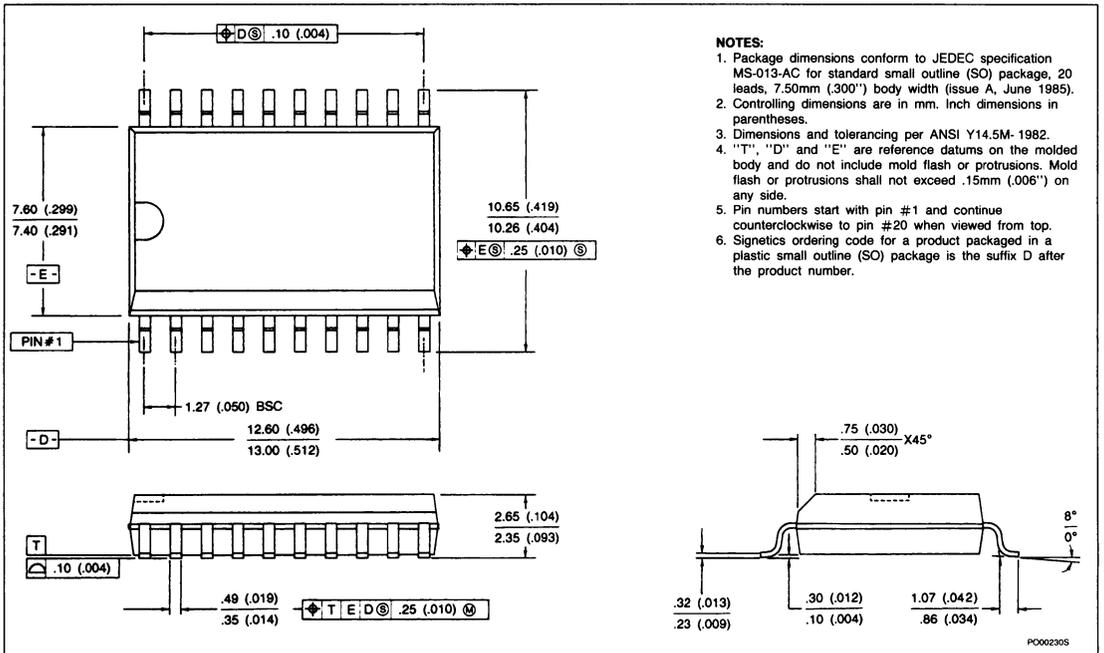


Package Outlines

DJ2/PLASTIC SOL-16

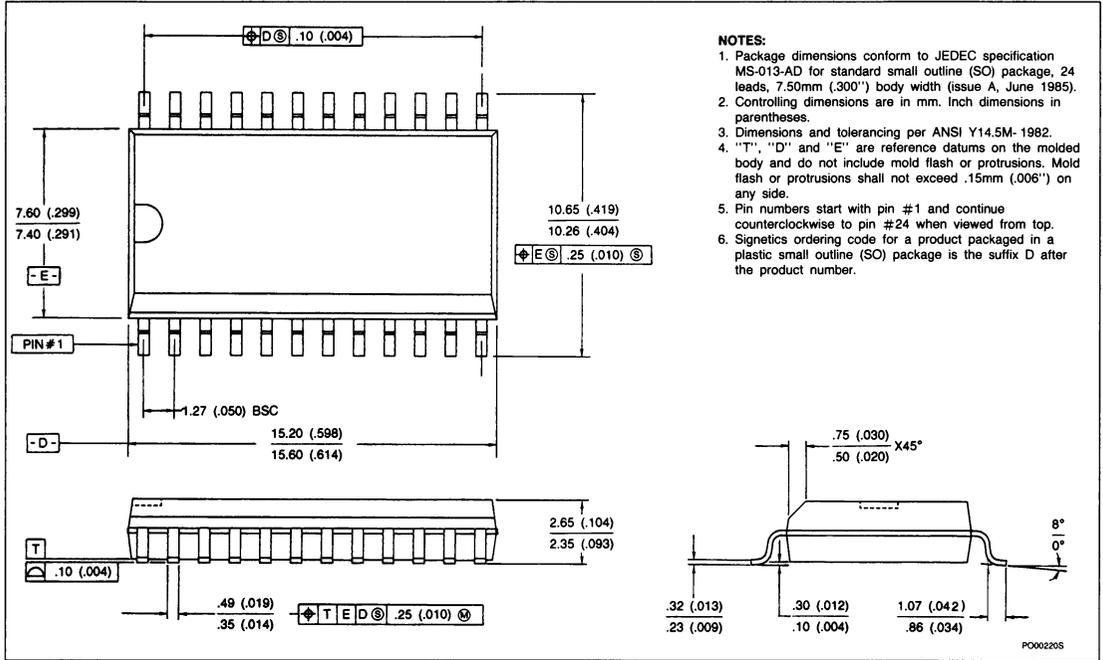


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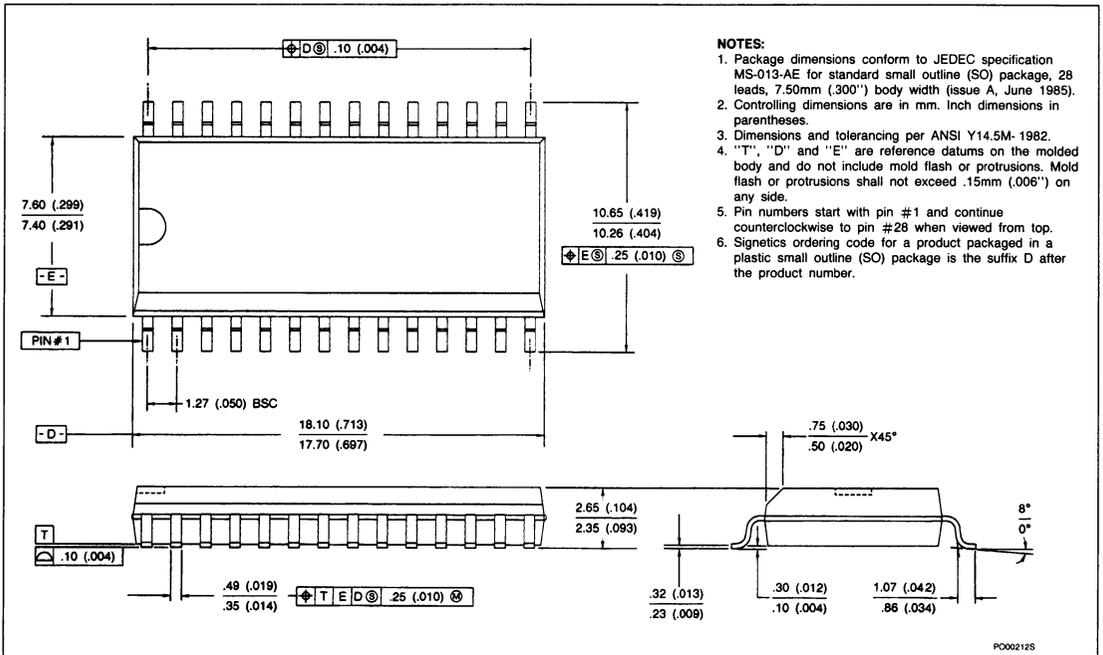


Package Outlines

DN2/PLASTIC SOL-24

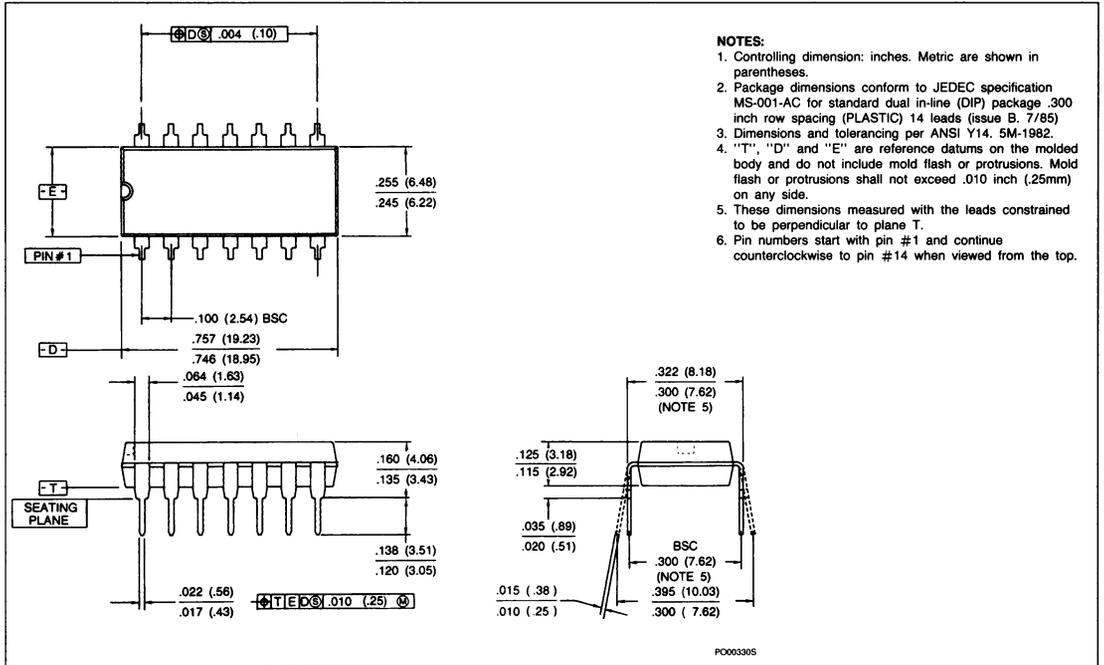


DQ2/PLASTIC SOL-28

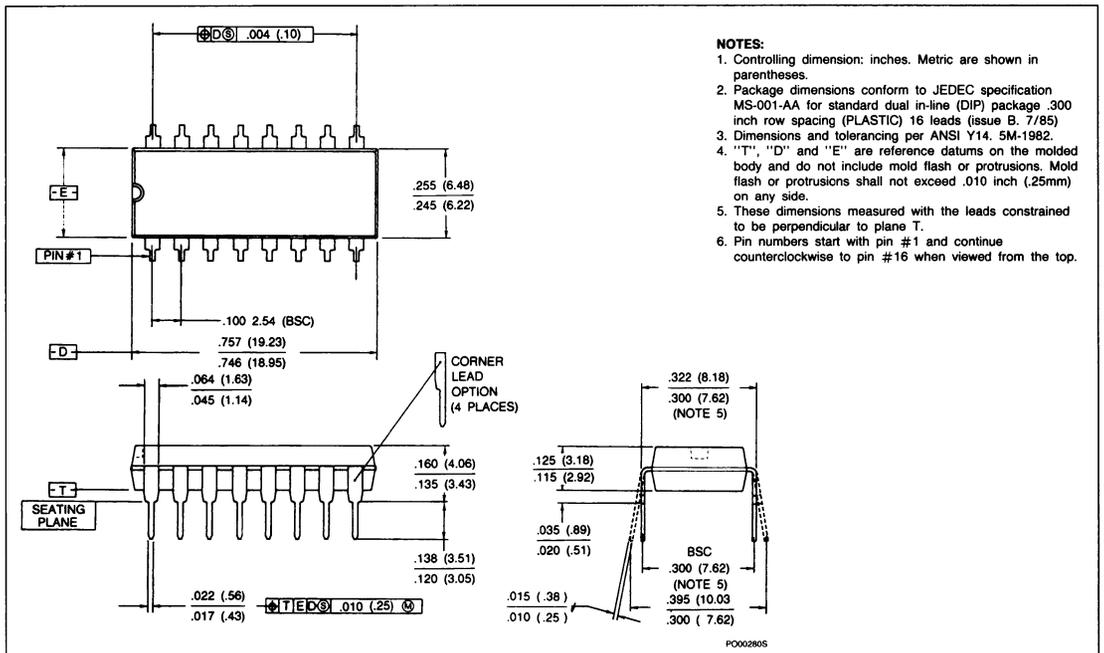


Package Outlines

NH1/PLASTIC DIP-14

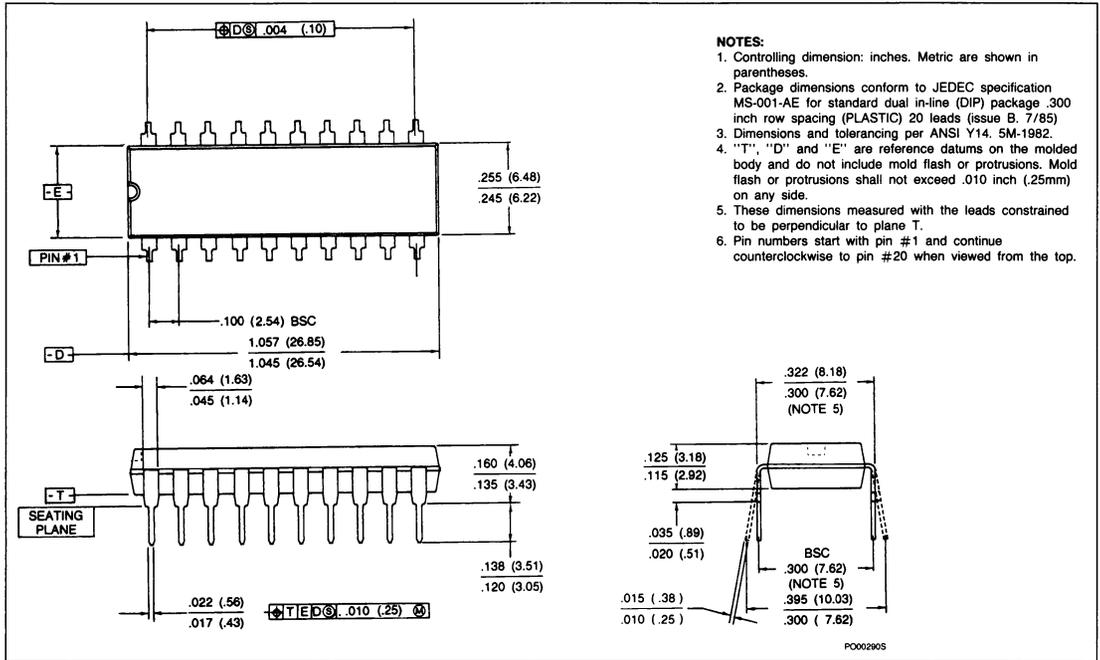


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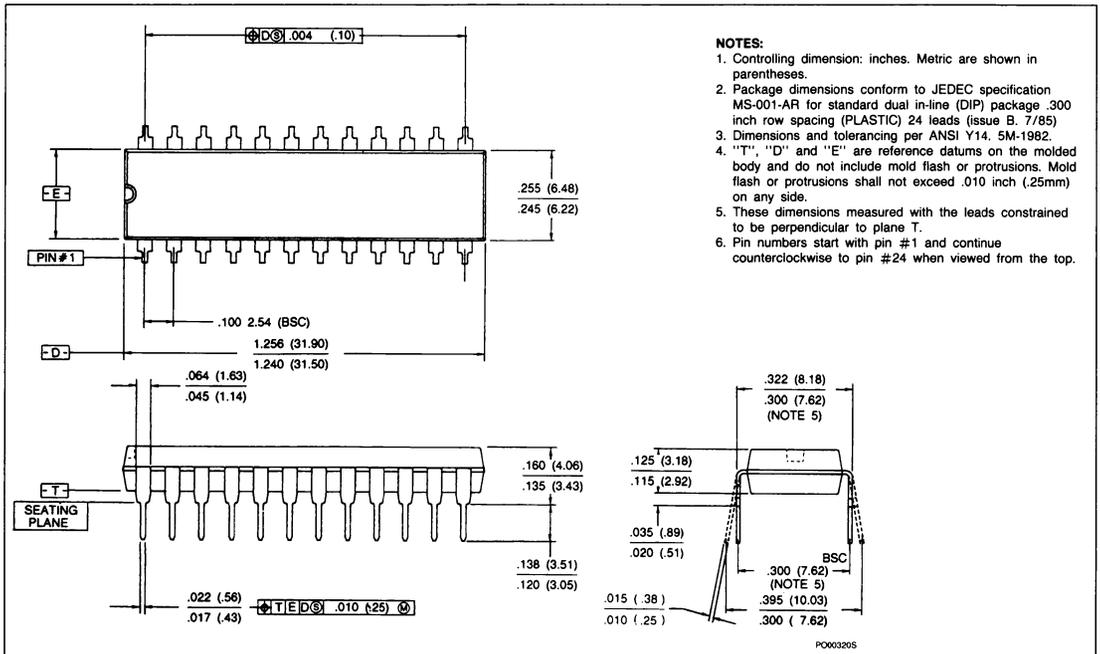


Package Outlines

NL1/PLASTIC DIP-20

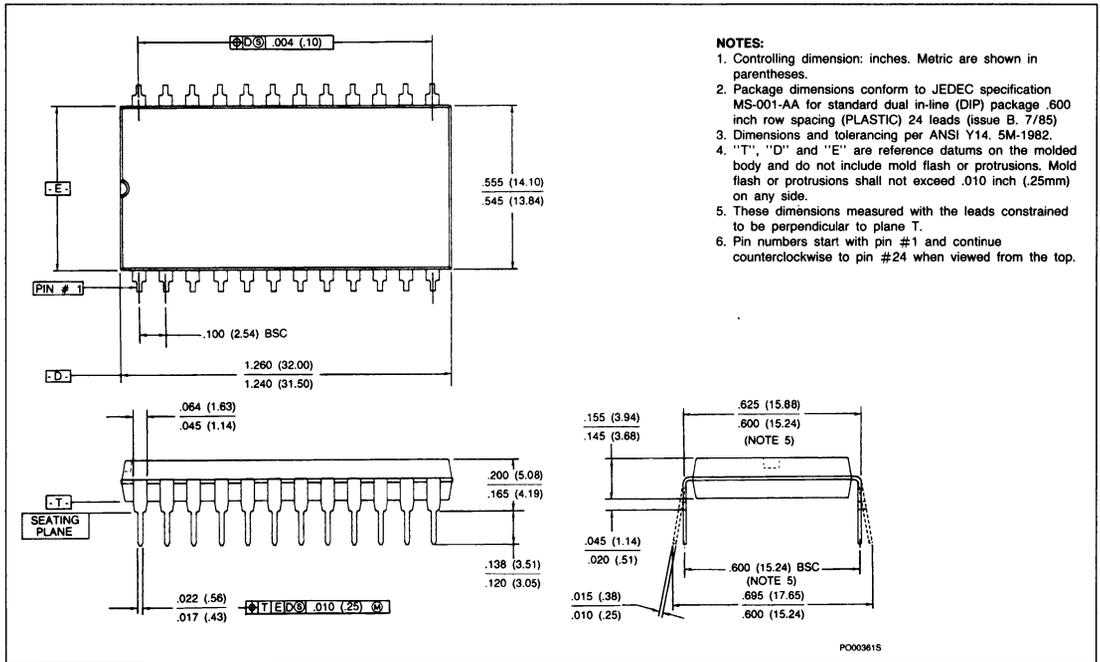


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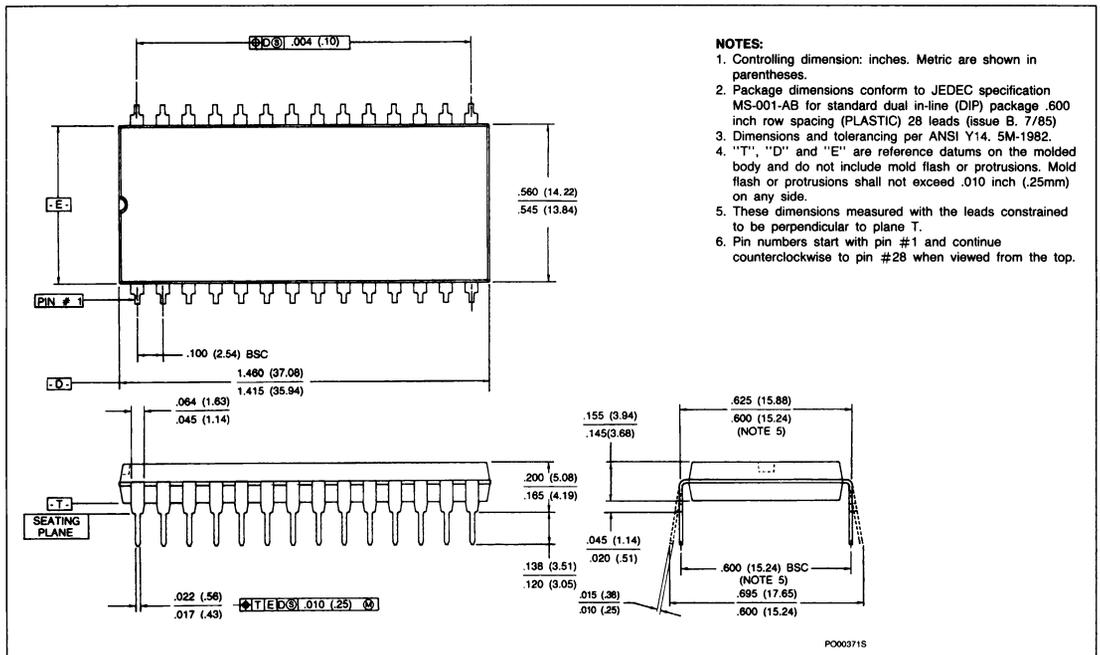


Package Outlines

NN3/PLASTIC DIP-24

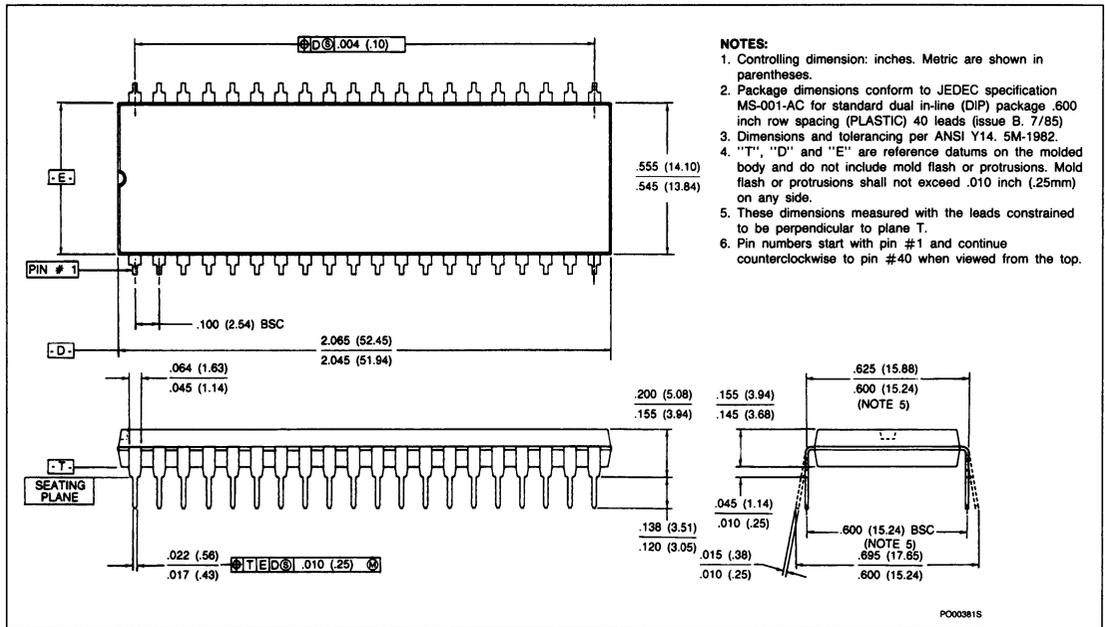


NQ3/PLASTIC DIP-28



Package Outlines

NW3/PLASTIC DIP-40



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