Signetics

PLD Data Manual

PHILIPS

Signetics Approach to Logic Flexibility: Programmable Logic Devices

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Preface

The continuing trend of system integration has created new challenges for Design Engineering. They must strive to consolidate higher complexity, and more feature intensive circuits into designs without sacrificing flexibility. Today's competitive electronic marketplace has created the need for logic devices, which can provide cost effective methods of reducing random logic requirements, interface with fixed and custom LSI logic, and maintain the flexible features required to make necessary system modifications prior to production. Signetics has responded to this need with Signetics Programmable Logic Devices (Signetics PLD).

The Signetics Programmable Logic family consists of devices which are designed to address logic needs ranging from random gates in the case of the Field Programmable Gate Arrays, to highly sophisticated state machines in the case of Field Programmable Logic Sequencers. Signetics pioneered the fully-programmable AND/OR/INVERT architecture in 1975. In 1987, Signetics introduced yet another new concept in PLD architectures. Moving away from an AND-OR array structure, the Signetics' Programmable Macro Logic architecture relies on a single NAND array concept. Signetics' novel architectural approach to Programmable Logic incorporates all the advantages associated with more dense complex gate arrays while retaining all the benefits of instantly programmable PLDs. By using the programmable features allowed by either powerful architecture, Signetics Programmable Logic can encompass wide-ranging levels of integration without the necessity of a multitude of devices, each with a different I/O configuration. The flexible programming structure allows the designer to "mold" the device architecture to the range of applications typically found in system design. In this way, one device can be used to perform several functions in the same design.

The 1988 – 1989 Signetics Programmable Logic Data Manual contains information that the designer will require in order to effectively utilize these products.

Signetics Application Specific Products Marketing

Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Selection Guide

Selection Guides

SIGNETICS PN	ARCHITECTURE	PACKAGE	TOTAL INPUTS (# Dedicated)	PRODUCT TERMS	INTERNAL STATE REGISTERS (# Dedicated)	OUTPUTS C, I/O, R/RI/O	T_{PD} (Max)	F_{MAX}	I_{CC} (Max)
PGA									
PLS103	16 × 9 × 9	28-Pin	16 (16)	9	0	9 C	35ns		170mA
PLS151	18 × 15 × 12	20-Pin	18 (6)	15	0	12 I/O	25ns		155mA
PAD									
PLS162	16 × 5	24-Pin	16 (16)	5	0	5 C	30ns		155mA
PLS163	12 × 9	24-Pin	12 (12)	9	0	9 C	30ns		155mA
PLA									
PLS100	16 × 48 × 8	28-Pin	16 (16)	48	0	8 C	50ns		170mA
PLC153-45/60	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	45/60ns		60mA*
PLS153	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	40ns		155mA
PLS153A	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	30ns		155mA
PLHS153	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	20ns		155mA
PLUS153B	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	15ns		200mA
PLUS153D	18 × 42 × 10	20-Pin	18 (8)	42	0	10 I/O	12ns		200mA
PLS161	12 × 48 × 8	24-Pin	12 (12)	48	0	8 C	50ns		170mA
PLS173	22 × 42 × 10	24-Pin	22 (12)	42	0	10 I/O	30ns		170mA
PLUS173B	22 × 42 × 10	24-Pin	22 (12)	42	0	10 I/O	15ns		200mA
PLUS173D	22 × 42 × 10	24-Pin	22 (12)	42	0	10 I/O	12ns		200mA
PLC473-60	20 × 24 × 11	24-Pin	20 (11)	24	0	2 C, 9 I/O	60ns		60mA*
PLHS473	20 × 24 × 11	24-Pin	20 (11)	24	0	2 C, 9 I/O	22ns		155mA
PAL®-TYPE									
PLHS18P8A	18 × 72 × 8	20-Pin	18 (10)	72	0	8 I/O	20ns		155mA
PLHS18P8B	18 × 72 × 8	20-Pin	18 (10)	72	0	8 I/O	15ns		155mA
PLHS16L8A	16 × 64 × 8	20-Pin	16 (10)	64	0	2 C, 6 I/O	20ns		155mA
PLHS16L8B	16 × 64 × 8	20-Pin	16 (10)	64	0	2 C, 6 I/O	15ns		155mA
PLUS16XXD**	16 × 64 × 8	20-Pin	Variable	64	0 – 8	Variable	10ns	56MHz	180mA
PLC16V8Q	16 × 72 × 8	20-Pin	16 (8)	72	8 (0)	8 RI/O	35, 45ns	18, 13MHz	50mA*
PLC16V8H	16 × 72 × 8	20-Pin	16 (8)	72	8 (0)	8 RI/O	35, 45ns	18, 13MHz	90mA*
PLC20V8Q	20 × 72 × 8	24-Pin	20 (12)	72	8 (0)	8 RI/O	35, 45ns	18, 13MHz	50mA*
PLC20V8H	20 × 72 × 8	24-Pin	20 (12)	72	8 (0)	8 RI/O	35, 45ns	18, 13MHz	90mA*
PLUS20XXD**	20 × 64 × 8	24-Pin	Variable	64	0 – 8	Variable	10ns	56MHz	210mA
PLS									
PLS105	16 × 48 × 8	28-Pin	16 (16)	48	6 (6)	8 R		13.9MHz	180mA
PLS105A	16 × 48 × 8	28-Pin	16 (16)	48	6 (6)	8 R		20MHz	180mA
PLUS405	16 × 64 × 8	28-Pin	16 (16)	64	8 (8)	8 R		33MHz	225mA
PLS155	16 × 45 × 12	20-Pin	16 (4)	45	4 (0)	8 I/O, 4 RI/O	50ns	14.3MHz	190mA
PLS157	16 × 45 × 12	20-Pin	16 (4)	45	6 (0)	6 I/O, 6 RI/O	50ns	14.3MHz	190mA
PLS159A	16 × 45 × 12	20-Pin	16 (4)	45	8 (0)	4 I/O, 8 RI/O	35ns	18MHz	190mA
PLS167	14 × 48 × 6	24-Pin	14 (14)	48	8 (6)	6 R		13.9MHz	180mA
PLS167A	14 × 48 × 6	24-Pin	14 (14)	48	8 (6)	6 R		20MHz	180mA
PLS168	12 × 48 × 8	24-Pin	12 (12)	48	10 (6)	8 R		13.9MHz	180mA
PLS168A	12 × 48 × 8	24-Pin	12 (12)	48	10 (6)	8 R		20MHz	180mA
PLS179	20 × 45 × 12	24-Pin	20 (8)	45	8 (0)	4 I/O and 8 RI/O	35ns	18MHz	210mA
PML									
PLHS501	32 × 116 × 24	52-Pin	32 (24)	72	0	16 C and 8 I/O	22ns		295mA
PLHS502	32 × 144 × 24	68-Pin	32 (24)	64	16 (0)	16 C or R, 8 I/O or RI/O	20ns	50MHz	370mA

OUTPUTS:
C = Combinatorial output
R = Registered output
I/O = Combinatorial I/O
R I/O = Registered I/O
* Measured at 15MHz (TTL input level)
** Under development

PGA = Programmable Gate Array
PAD = Programmable Address Decoder
PLA = Programmable Logic Array
PAL®–Type = Programmable Array Logic (Fixed OR Array)–Type
PLS = Programmable Logic Sequencer
PML = Programmable Macro Logic

NOTES:
$F_{MAX} = 1/(T_{IS} + T_{CKO})$ worst case
® PAL is a trademark of Monolithic Memories Inc., a wholly owned subsidiary of Advanced Micro Devices, Inc.

Signetics

Programmer Reference Guides

Application Specific Products

PART NUMBER	DEVICE CODES[2]		MODEL 29B			UNISITE 40			MODEL 60		
	FAMILY CODES	PIN CODES	SYSTEM REVISION	ADAPTOR REVISION		SYSTEM REVISION	ADAPTOR REVISION		SYSTEM REVISION	ADAPTOR REVISION	
				DIP	PLCC		DIP	PLCC		DIP	PLCC
PAL-TYPE DEVICES											
PLC16V8	86	3B	303A-V04	303A-011A; V05	303A-011B; V03	V2.1	SITE 40; 1.0	CHIPSITE; 1.0	TBA	TBA	TBA
PLC20V8	86	4E	303A-V04	303A-011A; V06	303A-011B; V03	V2.1	SITE 40; 1.0	CHIPSITE; 1.0	TBA	TBA	TBA
PLHS16L8A/B	1A	17	303A-V04	303A-012; V02	— —	V2.1	SITE 40; 1.0	CHIPSITE; 1.0	— —	— —	— —
PLHS18P8A/B	1A	33	303A-V04	303A-012; V01	— —	V2.1	SITE 40; 1.0	CHIPSITE; 1.0	— —	— —	— —
PLA DEVICES											
PLS100/101	96	01/61	303A-V04	303A-001; V01, V05	— —	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V01	360A003	TBA
PLS103	96	02/62	303A-V04	303A-001; V01, V05	— —	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V01	360A003	TBA
PLS151	96	64	303A-V04	303A-011A; V02 303A-001; V06	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	— —	— —	— —
PLC153	86	65	303A-V04	303A-011A; V05	303A-011B; V03	V2.1	SITE 40; 1.0	CHIPSITE; 1.0	TBA	TBA	TBA
PLS153/153A	96	65	303A-V04	303A-011A; V02 303A-001; V05	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V01	360A002	TBA
PLHS153	1A	65	303A-V04	303A-012; V02	— —	V2.1	SITE 40; 1.0	CHIPSITE; 1.0	— —	— —	— —
PLUS153B/D	1B	65	303A-V04	303A-011A; V07	303A-011B; V03	V2.1	SITE 40; 1.0	CHIPSITE; 1.0	TBA	TBA	TBA
PLS161	96	69	303A-V04	303A-001; V05 303A-011A; V02	NOT AVAILABLE IN PLCC	V1.5	SITE 40; 1.0	NOT AVAILABLE IN PLCC	60A/H; V01	360A002	NOT AVAILABLE IN PLCC
PLS162	96	73	— —	— —	"	V1.5	SITE 40; 1.0	"	60A/H; V05	306A004	"
PLS163	96	75	— —		"	V1.5	SITE 40; 1.0	"	60A/H; V05	360A004	"
PLS173[1]	96	76	303A-V04	303A-011A; V02	303A-011B; V02	V1.7	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V08	360A002	TBA
PLUS173B/D	1B	76	303A-V04	303A-011A; V07	303A-011B; V03	V2.1	SITE 40; 1.0	"	TBA	TBA	TBA
PLC473	86	78	303A-V04	303A-011A; V02	TBA	V2.1	SITE 40; 1.0	"	TBA	TBA	TBA
PLHS473	1A	78	303A-V04	303A-012; V01	— —	V2.1	SITE 40; 1.0	"	— —	— —	— —

PART NUMBER	DEVICE CODES[2]		MODEL 29B			UNISITE 40			MODEL 60		
	FAMILY CODES	PIN CODES	SYSTEM REVISION	ADAPTOR REVISION		SYSTEM REVISION	ADAPTOR REVISION		SYSTEM REVISION	ADAPTOR REVISION	
				DIP	PLCC		DIP	PLCC		DIP	PLCC
PLS DEVICES											
PLS105/105A	96	03/63	303A; V04	303A-011A; V02 303A-001; V01, 05	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V01	360A003	TBA
PLS155	96	67	303A; V04	303A-011A; V02 303A-001; V05	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V01	360A002	TBA
PLS157	96	68	303A; V04	303A-001; V05 303A-011A; V02	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V01	360A002	TBA
PLS159A	64	66	303A; V04	303A-011A; V02	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	TBA	TBA	TBA
PLS167/167A	96	60	303A; V04	303A-011A; V02	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V05	360A002	TBA
PLS168/168A[1]	96	74	303A; V04	303A-011A; V02	303A-011B; V02	V1.5	SITE 40; 1.0	CHIPSITE; 1.0	60A/H; V05	360A002	TBA
PLS179	96	77	303A; V04	303A-011A; V02	303A-011B; V02	V1.7	SITE 40; 1.0	CHIPSITE; 1.0	TBA	TBA	TBA
PLUS405	TBA	TBA	303A; V04	303A-011A; V07	303A-011B; V03	TBA	TBA	TBA	TBA	TBA	TBA
PML DEVICES											
PLHS501	010	707	— —	— —	— —	V1.7	— —	CHIPSITE; 1.0	— —	— —	— —
PLHS502	TBA	TBA	— —	— —	— —	TBA	— —	— —	— —	— —	— —

The software and hardware revisions listed are the earliest revisions that support these products. Later revisions can also be assumed to support these products.

NOTES:

1. Also supported on 303A-001; V06.
2. For Unisite model users only:
   - Family codes listed above must be preceeded with a "0" when programming PLCC packages.
   - Pin codes listed above must be preceeded with a "7" when programming PLCC packages.
3. "— —" indicates no support planned.

DEVICE PROGRAMMER REFERENCE GUIDE

STAG MICRO SYSTEMS, INC.
WESTERN AREA: 1600 WYATT DRIVE, SUITE 3, SANTA CLARA, CA. 95054 (408) 988-1118
EASTERN AREA: 3 NORTHERN BLVD., SUITE B4, AMHERST, N.H. 03031 (603) 673-4380

PART NUMBER	DEVICE CODES		MODEL ZL30	MODEL ZL30A		PPZ: ZM2200	
	FAMILY CODES	PIN CODES	(DIP ONLY)	DIP	PLCC	DIP	PLCC
PAL-TYPE DEVICES							
PLC16V8	12	154	30A27	30A27	30A001	30	**
PLC20V8	12	155	30A28	30A28	30A001	TBA	**
PLHS16L8A/B	10	029	NA	30A29[1]	30A101	TBA	**
PLHS18P8A/B	10	10	NA	30A23[1]	30A101	29	**
PLA DEVICES							
PLS100/101	13	00	30A01	30A01	30A001	17	**
PLS103	13	01	NA	30A01[2]	30A001	TBA	**
PLS151	14	04	30A01	30A01	30A001	26	**
PLC153	12	05	30A27	30A27	30A001	34	**
PLS153/153A	14	05	30A01	30A01	30A001	17	**
PLUS153B/D	11	05	30A27	30A27	30A001	34	**
PLS161	15	90	NA	30A01[2]	NOT AVAILABLE	24	NOT AVAILABLE
PLS162	15	94	NA	30A01[2]	IN PLCC	28[3]	IN PLCC
PLS163	15	95	NA	30A01[2]	"	26[4]	"
PLS173	15	96	30A01	30A01	30A001	23	**
PLUS173B/D	11	96	30A27	30A27	30A001	TBA	**
PLC473	12	132	30A24	30A24	30A001	32	**
PLHS473	10	132	NA	30A27[1]	30A101	30	**
PLS DEVICES							
PLS105/105A	13	02	30A01	30A01	30A001	17	**
PLS155	14	06	30A01	30A01	30A001	17	**
PLS157	14	07	30A01	30A01	30A001	17	**
PLS159A	13	08	30A25	30A25	30A001	27	**
PLS167/167A	15	91	30A01	30A01	30A001	TBA	**
PLS168/168A	15	97	30A01	30A01	30A001	23	**
PLS179	15	130	30A27	30A27	30A001	24	**
PML DEVICES							
PLHS501	10	133	NA	NA	30A22[1]	NA	NA
PLHS502	TBA	TBA	NA	NA	TBA	NA	NA

The software and hardware revisions listed are the earliest revisions that support these products. Lates revisions can also be assumed to support these products.

NOTES:

1. Requires 30A101 Adaptor; includes PLCC support.
2. Requires 30A100 Adaptor.
3. Requires 30-1594 Adaptor.
4. Requires 30-1595 Adaptor.

** Socket Adaptors required.

Signetics

Ordering Information

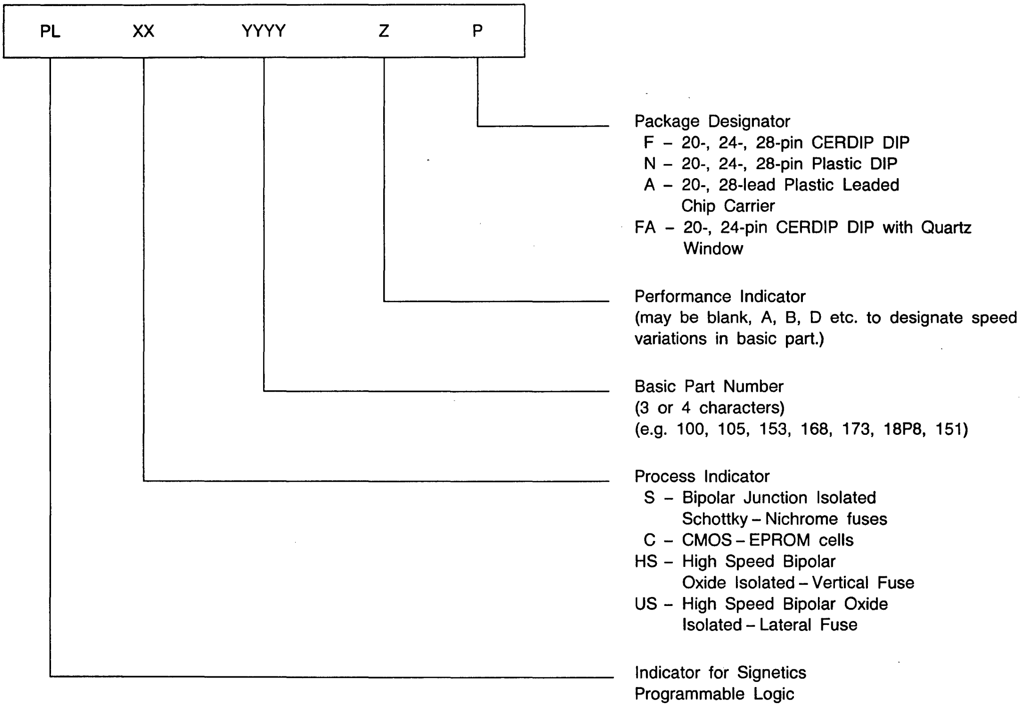
Application Specific Products

Signetics Programmable Logic Devices may be ordered by contacting either the local Signetics sales office, Signetics representatives or authorized distributors. A complete listing is located in the back of this manual.

Table 1 provides part number definition for Signetics PLD's. The Signetics part number system allows complete ordering information to be specified in the part number. The part number and product description is located on each data sheet.

Military versions of these commercial products may be ordered. Please refer to the military products data manual for complete ordering information.

New Signetics PLD Part Numbering System



PL XX YYYY Z P

Package Designator
F – 20-, 24-, 28-pin CERDIP DIP
N – 20-, 24-, 28-pin Plastic DIP
A – 20-, 28-lead Plastic Leaded Chip Carrier
FA – 20-, 24-pin CERDIP DIP with Quartz Window

Performance Indicator
(may be blank, A, B, D etc. to designate speed variations in basic part.)

Basic Part Number
(3 or 4 characters)
(e.g. 100, 105, 153, 168, 173, 18P8, 151)

Process Indicator
S – Bipolar Junction Isolated Schottky - Nichrome fuses
C – CMOS - EPROM cells
HS – High Speed Bipolar Oxide Isolated - Vertical Fuse
US – High Speed Bipolar Oxide Isolated - Lateral Fuse

Indicator for Signetics Programmable Logic

Signetics

Section 2
Introduction

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Signetics

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WHAT IS PROGRAMMABLE LOGIC

In 1975, Signetics Corporation developed a new product family by combining its expertise in semi-custom gate array products and fuse-link Programmable Read Only Memories (PROMs). Out of this marriage came Signetics Programmable Logic Family. The PLS100 Field-Programmable Logic Array (FPLA) was the first member of this family. The FPLA was an important industry first in two ways. First, the AND/OR/INVERT architecture allowed the custom implementations of Sum of Product logic equations. Second, the three-level fusing allows complete flexibility in the use of this device family. All logic interconnections from input to output are programmable.

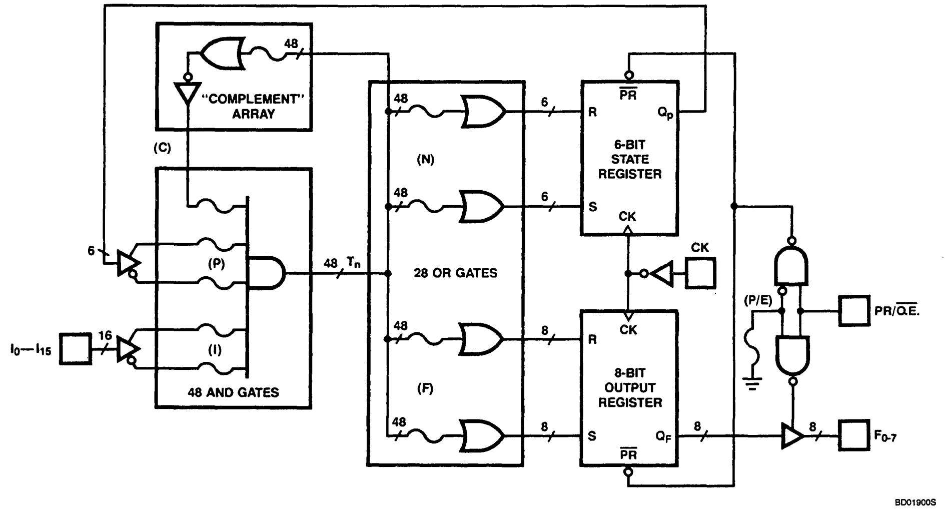
Development of this family did not stop with the PLS100. In 1977, the PLS103 Field-Programmable Gate Array (FPGA) and the PLS107 Field-Programmable ROM Patch (FPRP) were introduced.

The PLS105 Field-Programmable Logic Sequencer (FPLS) was announced in 1979. This device represents a significant step forward for PLD. The FPLS is a fully-implemented Mealy State Machine on a chip. Incorporated into its architecture are 48 P-terms, an 8-bit Output Register, and a 6-bit internal State Register. Reference Figure 1.

The FPLS can synchronously perform sequential routines at 20MHz. All of these products are now known as the Signetics PLD Series 28 Programmable Logic Family.

Signetics next innovation in this area was the Series 20 Programmable Logic Family. All members of this family are assembled in 20-pin packages. While reducing the number of pins in this family, Signetics has utilized controlled I/O in order to maintain the utility of the Series 20. Appropriate control terms have been included to allow active control of pin direction. Reference Figure 2.

The latest addition to the Signetics Programmable Logic families is the Series 24 devices. The PLS161 FPLA and the PLS167 FPLS are 24-pin devices comparable to the 28-pin PLS100 and PLS105 respectively. These devices have been followed by the PLS162/PLS163 Field-Programmable Address Decoder and the PLS168 FPLS.



NOTE:
I, P, C, N, F and P/E are user-programmable connections.

Figure 1. FPLS

Table 1. PLD Product Family

PART NUMBER	TYPE	CONFIGURATION
20-PIN		
PLS151	PGA	18-Input/12-Output
PLS153/153A/PLHS153	PLA	18-Input/10-Output - 42-Term
PLUS153B/153D/PLC153	PLA	18 input/10-Output - 42-Term
PLS155-159	PLS	16-Input/12-Output - 45-Term
PLS155	PLS	4 Registered Outputs
PLS157	PLS	6 Registered Outputs
PLS159	PLS	8 Registered Outputs
PLHS18P8A/B	PAL-Type	18-Input/10-Output - 72-Term
PLHS16L8A/B/D	PAL-Type	16-Input/8-Output - 64-Term
PLC16V8 Series	PAL-Type	18-Input/8-Output - 72-Term
24-PIN		
PLS161	PLA	12-Input/8-Output - 48-Term
PLS162	PGA	16-Input/5-Output
PLS163	PGA	12-Input/9-Output
PLS167/A	PLS	14-Input/6-Output - 48-Term 8-Bit State Registers 6-Output Registers
PLS168/A	PLS	12-Input/8-Output - 48-Term 10-Bit State Registers 8-Output Registers
PLS173/PLUS173B/D	PLA	22-Input/10-Output - 42-Term
PLS179	PLS	16-Input/12-Output - 42-Term 8-Bit State and Output Registers
PLHS473/PLC473	PLA	20-Inputs/11-Output - 24-Term
PLC20V8 Series	PAL-Type	22-Input/8-Output - 72-Term
28-PIN		
PLS100/101	PLA	16-Inputs/8-Output - 48-Term
PLS103	PGA	16-Inputs/9-Output
PLS105/105A/PLC105	PLS	16-Inputs/8-Output - 48-Term 6-Bit State Register 8-Output Registers
PLUS405	PLS	16-Inputs/8-Outputs - 64-Terms 8-Bit State and Output Registers
52-, 68-PIN		
PLHS501	PML	32-Input/24-Output - 116-Term
PLHS502	PML	32-Input/24-Output - 144-Term

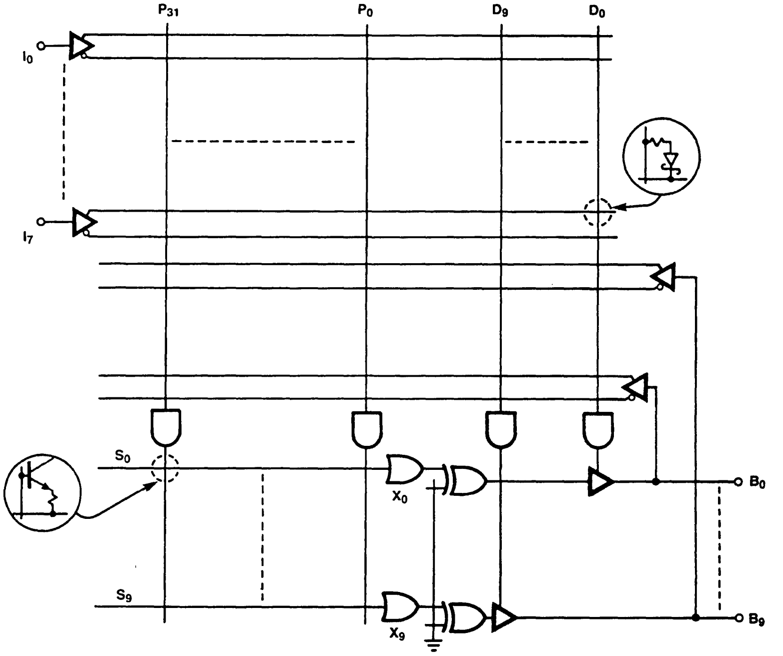
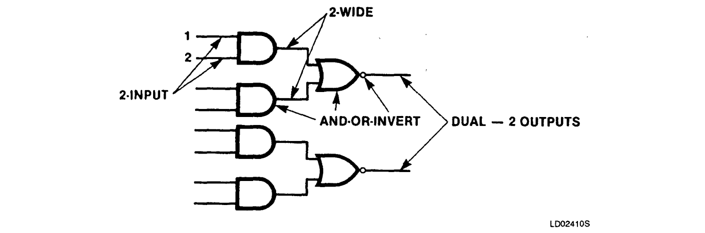
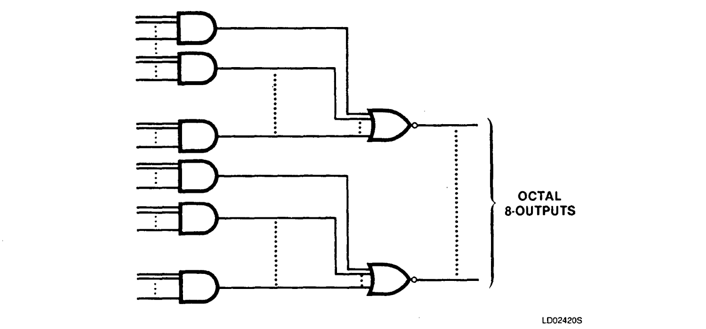


Figure 2. PLS153 20-Pin Functional Diagram



7450 2 × 2 × 2 Fixed Interconnections Dual, 2-Wide, 2-Input, AND/OR/INVERT



PLS100 16 × 48 × 8 Octal, 48-Wide, 16-Input, AND/OR/INVERT

Table 2. Gate Replacement (All Terms Used)

	Gates	I.C.s
Each P-Term = 2 8-Input AND Gates & 1 2-Input AND Gate =	144	108
OR Matrix = 16 4-Input OR Gates =	128	32
	272	140

Table 3. Typical Application

4 Variables/P-Term	40 Gates
4 P-Terms/Output	15-20 I.C.s

PRODUCT DESCRIPTION

While all PLD devices are architecturally similar, the Field-Programmable Logic Array is most representative of the concepts involved. The FPLA is an AND/OR/INVERT device, with all internal interconnections programmable via fuse links. If we compare the PLS100 FPLS to the familiar 7450 AOI gate, the similarity of function becomes apparent.

Package-Gate Replacement Potential

All Signetics PLD devices are capable of replacing multiple discrete logic devices. The number of packages is dependent on the application and the device used.

If all product terms and inputs on the PLS100 are utilized, a total of 272 gates and 140 I.C.s can theoretically be replaced. (See Table 2.) Since the PLS100 is made up of logic structures which are not available as commercial logic devices, such as 32 input AND gates and 48 input OR gates, these numbers are based on breakdowns of these high complexity logic structures into structures which are available as discrete logic.

The typical application does not fully utilize the FPLA, however. We can assume that the typical application is as defined in Table 3.

The replacement of 15-20 I.C.s with one PLS100 is not unusual.

PLD ECONOMICS

The reason any product line exists is because it solves a problem in a cost-effective manner.

PLD is no different in this respect. Let's assume that one PLS100 is replacing only 10 TTL logic packages.

If we assume that the average selling price of an SSI level device is $0.25, then we have a basis for comparison.

10 I.C.s @ 0.35 = $3.50
1 PLS100 FPLA = $7.00

Considering piece-part cost alone does not fare well for the PLS100 FPLA. **But**, part cost is one of the smaller costs in systems manufacturing. Let's next consider PC board costs.

PC BOARD

The purchase price of a PCB is calculated on a per square inch basis. Typical costs at the 5K level are $0.23/in^2, the cost for LS is 1.2in^2 = $0.23/in^2 = $0.28. For a 28-pin FPLA device, the packing density is 1-PLS100 per 2.5in^2, giving a cost of 2.5in^2 × $0.23/in^2 = $0.58.

PCB FABRICATION

Now let's consider the cost of building the board. The primary cost for PCB fabrication is parts preparation and stuffing.

Estimates by PCB manufacturers indicate a nominal cost of $0.14 per device for LS TTL and $0.16 for 28-pin FPLA. There is also a basic cost of $0.02 per in^2 for handling, soldering, and inspecting.

The cost of incoming inspection and inventory/usage must also be considered in any fair comparison.

INCOMING INSPECTION

The cost of incoming inspection can be calculated on a per-pin basis. Assuming an equal mix of 14- and 16-pin SSI parts and a testing cost of $0.01 per pin, the LS TTL cost is $0.15 per I.C. The corresponding cost for the PLS100 would be $0.01 × 28 or $0.28 total.

COMPONENT INVENTORY/ USAGE

The inventory cost for LS TTL parts is dominated by inventory maintenance, while the LSI type parts, the piece price dominates. Assuming a 2% usage rate due to parts breakage, burnout, etc., in the manufacturing process, the parts cost for LS TTL is 2% × $0.25 = $0.005. Adding $0.02 per device for inventory maintenance, the total LS cost $0.03. For FPLA, 2% = $7.00± $0.02 = $0.16.

Consideration must also be given to testing the completed PCB and Rework costs.

PCB TESTING

Testing costs are generally figured on a PCB basis and are usually go-no-go tests using a "bed of nails". For this comparison, assume a PCB of 5" × 7". The cost for testing the completed PCB is estimated to be $3.60 for 20 I.C.s. This breaks down as $0.18 per LS TTL device or about $0.45 per FPLA device.

PCB REWORK

The main causes of rework are poorly plated holes, solder bridges, and parts inserted incorrectly. The "bed of nails" test can usually detect all of the faults. Rework costs about 50% of test costs. The result is $1.80 per PCB, or $0.09 per device for LS TTL and $0.18 for the 28-pin FPLA.

System manufacturing costs are harder to define. For this comparison we estimated $0.28 for each LS device and about $0.65 for the FPLA. These costs include backplane wiring, final system assembly and test costs.

Now using these figures, the comparison in Table 4 can be made.

Table 4. Cost Analysis

	LS TTL	FPLA
IC COMPONENTS	.35	7.00
PCB MANUFACTURING		
Incoming Inspection	.15	.28
Component Inventory/Usage	.03	.16
PC Board	.28	.58
Fabrication	.14	.16
Test	.18	.45
Rework	.09	.18
ASSEMBLY LABOR	.28	.65
COST PER COMPONENT	1.50	9.46
NUMBER OF COMPONENTS	× 10	× 1
TOTAL	15.00	9.46

CONCLUSION:
THE FPLA is a 37% savings over the LS TTL DESIGN.

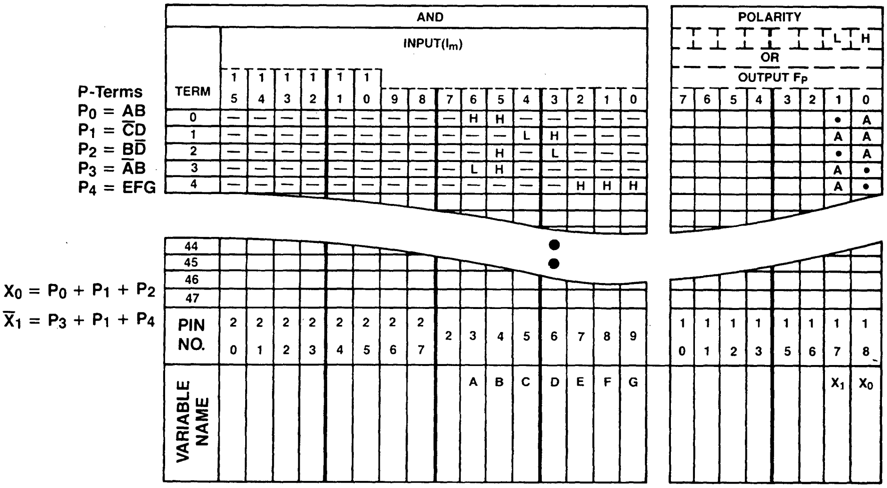
PLD LOGIC SYNTHESIS

28-PIN

PLD is capable of Logic Synthesis. No intermediate step is required to implement Boolean Logic Equations with PLD. Each term in each equation simply becomes a direct entry into the Logic Program Table. The following example illustrates this straightforward concept:

$X_0 = AB + \overline{C}D + B\overline{D}$

$\overline{X}_1 = \overline{A}B + \overline{C}D + EFG$



P-Terms

$P_0 = AB$

$P_1 = \overline{C}D$

$P_2 = B\overline{D}$

$P_3 = \overline{A}B$

$P_4 = EFG$

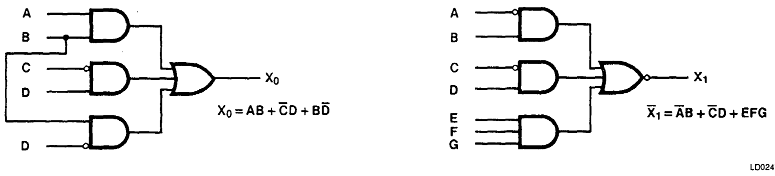
$X_0 = P_0 + P_1 + P_2$

$\overline{X}_1 = P_3 + P_1 + P_4$

	AND																POLARITY							
	INPUT(I_m)																						L	H
																	OR OUTPUT F_P							
TERM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	—	—	—	—	—	—	—	—	—	H	H	—	—	—	—	—							•	A
1	—	—	—	—	—	—	—	—	—	—	—	L	H	—	—	—							A	A
2	—	—	—	—	—	—	—	—	—	—	H	—	L	—	—	—							•	A
3	—	—	—	—	—	—	—	—	—	L	H	—	—	—	—	—							A	•
4	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	H							A	•
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G							X_1	X_0

TB01910S

Figure 3. Field-Programmable Logic Array (16 × 48 × 8) PLS100/PLS101


A
B
C
D
D
X_0
$X_0 = AB + \overline{C}D + B\overline{D}$
A
B
C
D
E
F
G
X_1
$\overline{X}_1 = \overline{A}B + \overline{C}D + EFG$

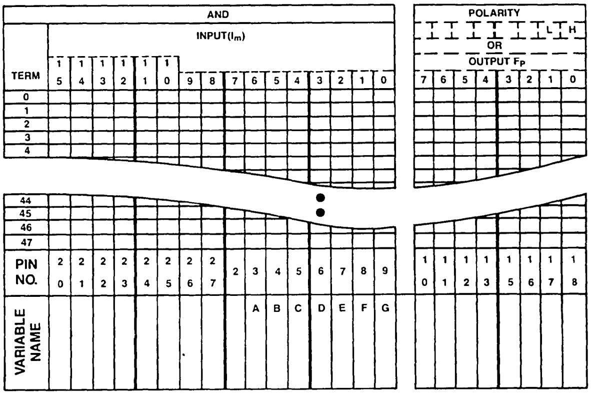
LD02471S

Figure 4. Equivalent Fixed Logic Diagram

In the previous example, the two Boolean Logic equations were broken into Product terms. Each P-term was then programmed into the P-term section of the PLS100 FPLA Program Table. This was accomplished in the following manner:

Step 1

Select which input pins $I_0 - I_{15}$ will correspond to the input variables. In this case A – G are the input variable names. I_6 through I_0 were selected to accept inputs A – G respectively.



TERM	AND INPUT(I_m) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POLARITY / OR OUTPUT F_P 7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
4																								
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G								

Figure 5

Step 2

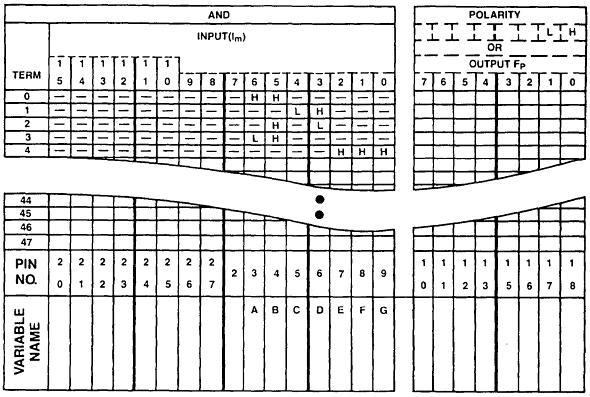
Transfer the Boolean Terms to the FPLA Program Table. This is done simply by defining each term and entering it on the Program Table.

e.g., $P_0 = AB$

This P-term translates to the Program Table by selecting $A = I_6 = H$ and $B = I_5 = H$ and entering the information in the appropriate column.

$P_1 = \overline{C}D$

This term is defined by selecting $C = I_4 = L$ and $D = I_3 = H$, and entering the data into the Program Table. Continue this operation until all P-terms are entered into the Program Table.

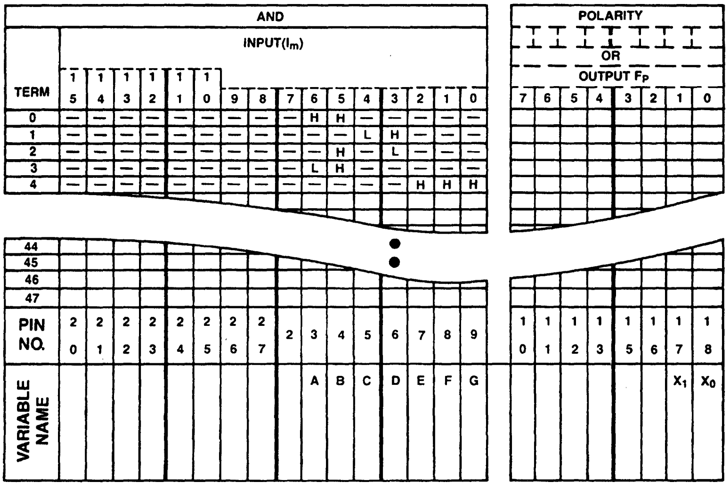


TERM	AND INPUT(I_m) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POLARITY / OR OUTPUT F_P 7	6	5	4	3	2	1	0
0	—	—	—	—	—	—	—	—	—	H	H	—	—	—	—	—								
1	—	—	—	—	—	—	—	—	—	—	—	L	H	—	—	—								
2	—	—	—	—	—	—	—	—	—	—	H	—	L	—	—	—								
3	—	—	—	—	—	—	—	—	—	L	H	—	—	—	—	—								
4	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	H								
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G								

Figure 6

Step 3

Select which output pins correspond to each output function. In this case F_0 = Pin 18 = X_0, and F_1 = Pin 17 = X_1.



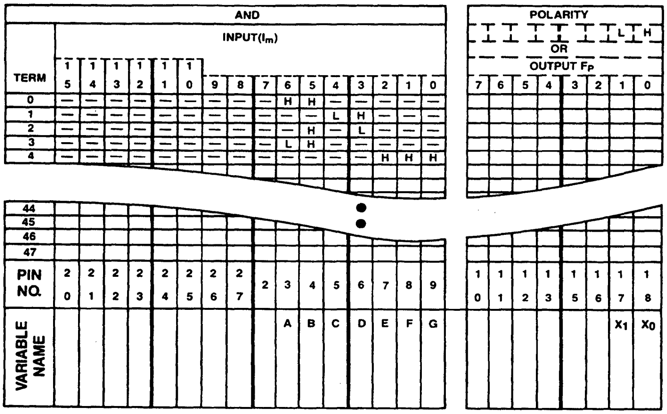
	AND																POLARITY							
	INPUT(I_m)																OR OUTPUT F_P							
TERM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	—	—	—	—	—	—	—	—	—	H	H	—	—	—	—	—								
1	—	—	—	—	—	—	—	—	—	—	—	L	H	—	—	—								
2	—	—	—	—	—	—	—	—	—	—	H	—	L	—	—	—								
3	—	—	—	—	—	—	—	—	—	L	H	—	—	—	—	—								
4	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	H								
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G							X_1	X_0

TB01882S

Figure 7

Step 4

Select the Output Active Level desired for each Output Function. For X_0 the active level is high for a positive logic expression of this equation. Therefore, it is only necessary to place an (H) in the Active Level box above Output Function 0, (F_0). Conversely, X_1 can be expressed as $\overline{X}_1$ by placing an (L) in the Active Level box above Output Function 1, (F_1).



	AND																POLARITY							
																							L	H
	INPUT(I_m)																OR OUTPUT F_P							
TERM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	—	—	—	—	—	—	—	—	—	H	H	—	—	—	—	—								
1	—	—	—	—	—	—	—	—	—	—	—	L	H	—	—	—								
2	—	—	—	—	—	—	—	—	—	—	H	—	L	—	—	—								
3	—	—	—	—	—	—	—	—	—	L	H	—	—	—	—	—								
4	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	H								
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G							X_1	X_0

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Figure 8

Step 5

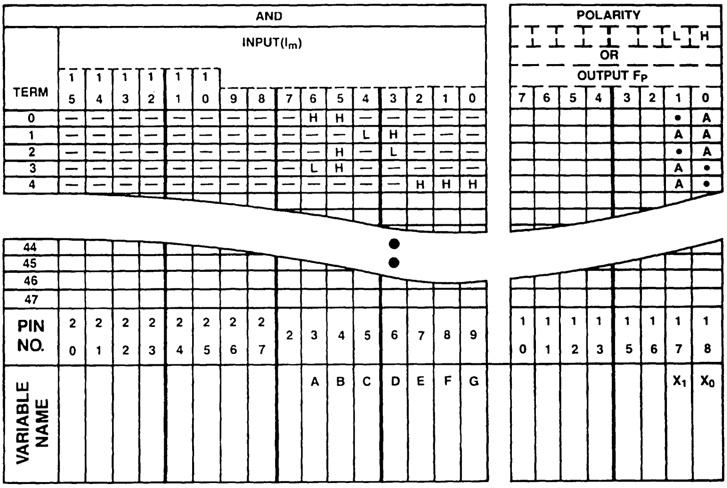
Select the P-Terms you wish to make active for each Output Function. In this case $X_0 = P_0 + P_1 + P_2$, so an A has been placed in the intersection box for P_0 and X_0, P_1 and X_0 and P_2 and X_0.

Terms which are not active for a given output are made inactive by placing a (●) in the box under that P-term. Leave all unused P-terms unprogrammed.

Continue this operation until all outputs have been defined in the Program Table.

Step 6

Enter the data into a Signetics approved programmer. The input format is identical to the Signetics Program Table. You specify the P-terms, Output Active Level, and which P-terms are active for each output .exactly the way it appears on the Program Table.



$X_0 = P_0 + P_1 + P_2$

$\overline{X}_1 = P_3 + P_1 + P_4$

	AND																POLARITY							
	INPUT(I_m)																						L	H
																	OR OUTPUT F_P							
TERM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	—	—	—	—	—	—	—	—	—	H	H	—	—	—	—	—							•	A
1	—	—	—	—	—	—	—	—	—	—	—	L	H	—	—	—							A	A
2	—	—	—	—	—	—	—	—	—	—	H	—	L	—	—	—							•	A
3	—	—	—	—	—	—	—	—	—	L	H	—	—	—	—	—							A	•
4	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	H							A	•
44																								
45																								
46																								
47																								
PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME										A	B	C	D	E	F	G							X_1	X_0

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Figure 9

PLD LOGIC SYNTHESIS

20-PIN

When fewer inputs and outputs are required in a logic design and low cost is most important, the Signetics 20-pin PLD should be considered first choice. The PLS153 is an FPLA with 8 inputs, 10 I/O pins, and 42 product terms. The user can configure the device by defining the direction of the I/O pins. This is easily accomplished by using the direction control terms $D_0 - D_9$ to establish the direction of pins $B_0 - B_9$. The D-terms control the Tri-state buffers found on the outputs of the EX-OR gates. Figures 10 and 11 show how the D-term configures each B_x pin.

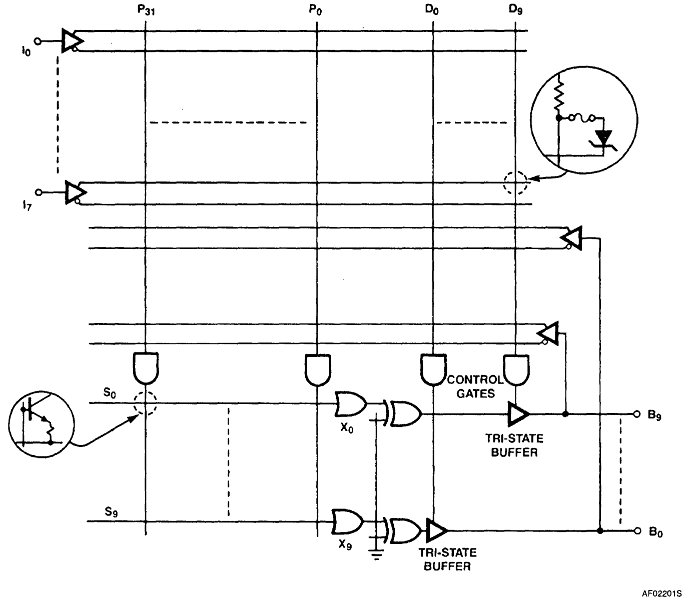
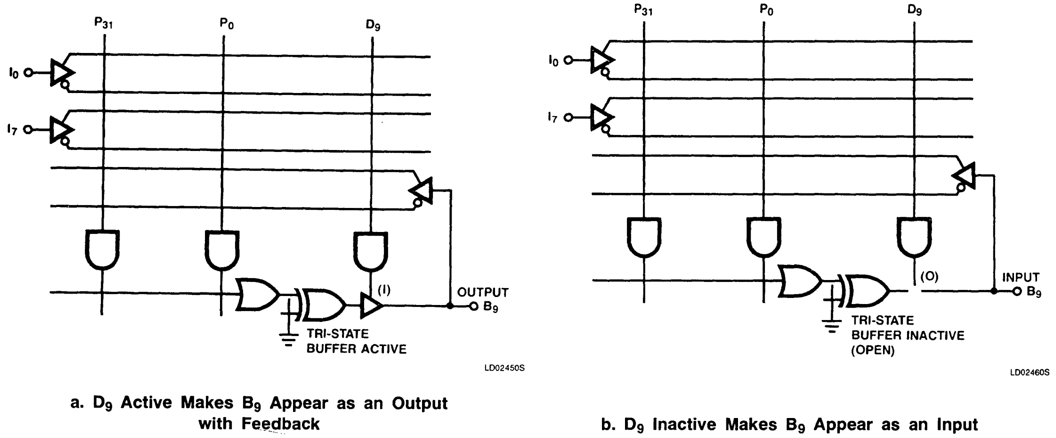


Figure 10. PLS153 Functional Diagram



a. D_9 Active Makes B_9 Appear as an Output with Feedback

b. D_9 Inactive Makes B_9 Appear as an Input

Figure 11

To control each D-term, it is necessary to understand that each control gate is a 36-input AND gate. To make the Tri-state buffer active (B_X pin an output), the output of the control gate must be at logic HIGH (1). This can be accomplished in one of two ways. A HIGH can be forced on all control gate input nodes, or fuses can be programmed. When a fuse is programmed, that control gate input node is internally pulled up to HIGH (1). See Figure 12 and Figure 13.

Programming the fuse permanently places a HIGH (1) on the input to the control gate. The input pin no longer has any effect on that state.

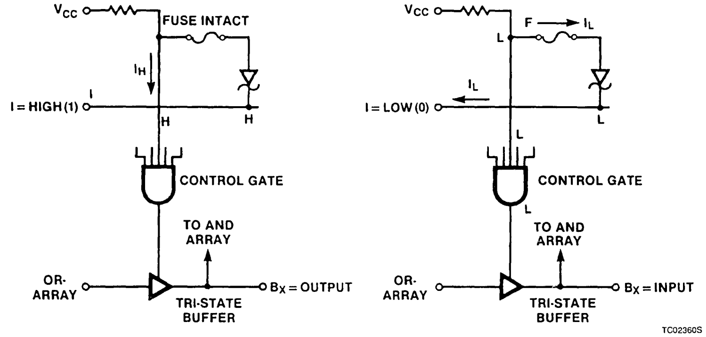


Figure 12. Input Effect on Control Gates (Fuse Intact)

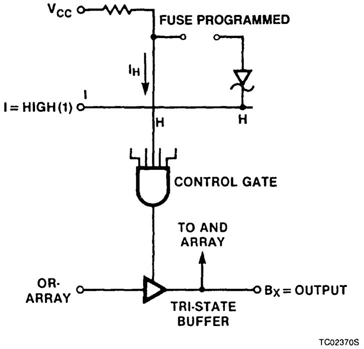
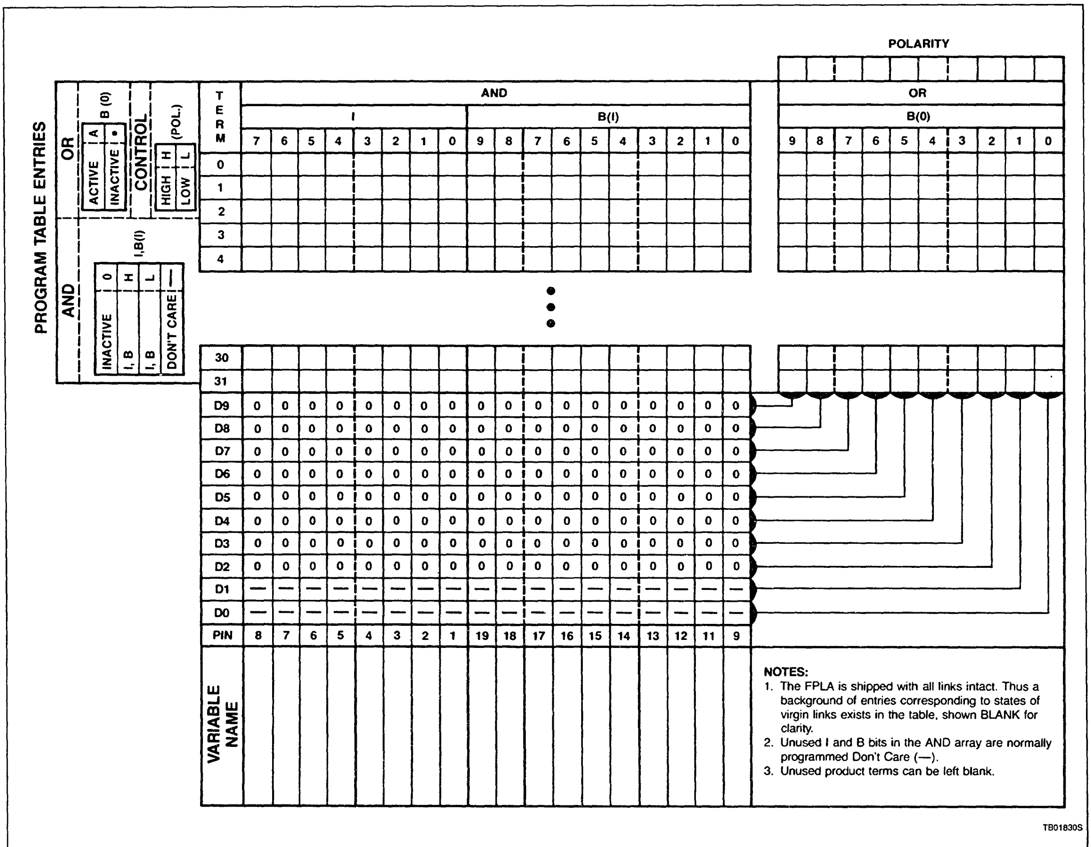


Figure 13. Effect on Control Gate if Fuse is Programmed

DEDICATING B_X PIN DIRECTION

Since each input to the D-terms is true and complement buffered (see Figure 11), when the device is shipped with all fuses intact, all control gates have half of the 36 input lines at logic low (0). The result of this is all Control Gate outputs are low (0) and the Tri-state buffers are inactive. This results in all B_X pins being in the input condition. The resultant device is, therefore, an 18-input, 0-output FPLA. While useful as a bit bucket or Write-Only-Memory (WOM), most applications require at least one output. Clearly, the first task is to determine which of the B_x pins are to be outputs. The next step is to condition the control gate to make the Tri-state buffer for those gates active. To dedicate B_0 and B_1 as outputs, it is necessary to program all fuses to the inputs to Control Gates D_0 and D_1. This internally pulls all inputs to those gates to HIGH (1) permanently. Since all inputs to the Control Gates are HIGH (1), the output is HIGH (1) and the Tri-state buffers for B_0 and B_1 are active. This permanently enables B_0 and B_1 as outputs. Note that even though B_0 and B_1 are outputs, the output data is available to the AND array via the internal feedback (see Figure 11a).

To program this data, the PLS153 Program Table is used as shown in Figure 14.


PROGRAM TABLE ENTRIES
OR
ACTIVE A
INACTIVE •
B (0)
CONTROL
HIGH H
LOW L
(POL.)
AND
INACTIVE 0
I, B H
I, B L
DON'T CARE —
I,B(I)

																			POLARITY									
TERM	AND																		OR									
	I								B(I)										B(O)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0																												
1																												
2																												
3																												
4																												
• • •																												
30																												
31																												
D9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9										
VARIABLE NAME																												

NOTES:
1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I and B bits in the AND array are normally programmed Don't Care (—).
3. Unused product terms can be left blank.

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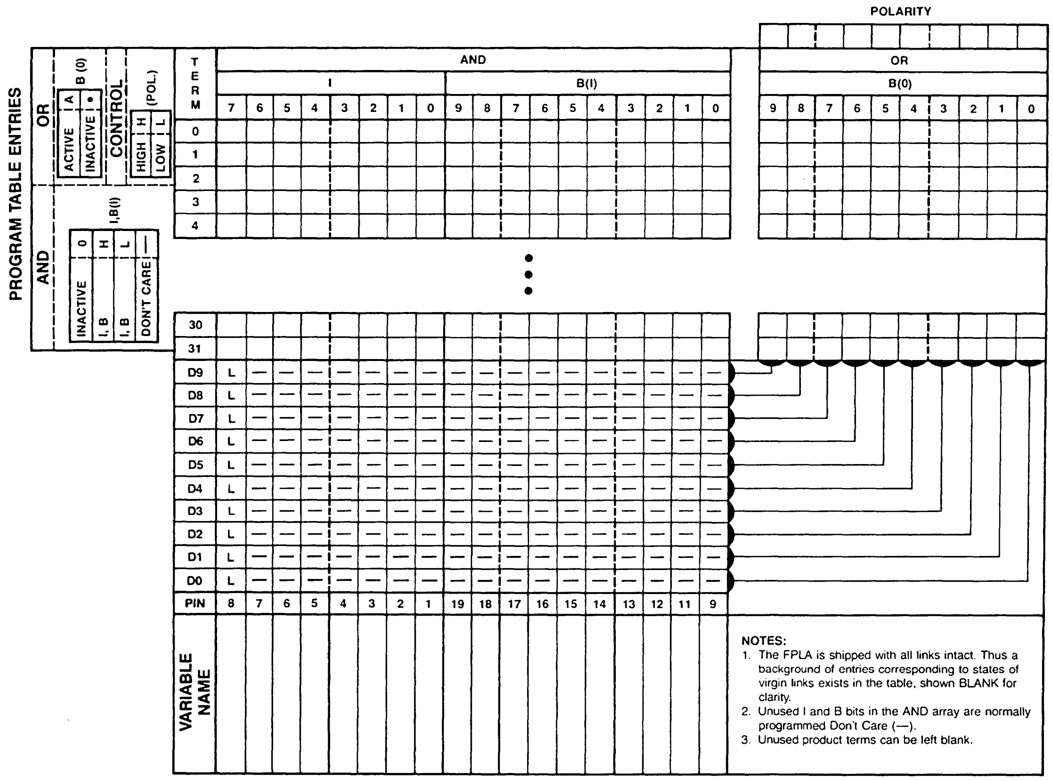
Figure 14. Dedicating B_0 and B_1 as Outputs and B_2 Through B_9 as Inputs

By placing a (—) Don't Care in each input box you are specifying that the True and Complement fuses are programmed on each Control Gate, thus permanently dedicating the B_0 and B_1 pins as outputs. By placing a (0) in all input boxes for B_2-B_9, you are specifying that both True and Complement fuses are intact. This causes a low (0) to be forced on half of the Control Gate inputs, guaranteeing the output of the Control Gate will be low (0). When the Control Gate outputs are low (0), the Tri-state buffer is inactive and the B_2-B_9 pins are enabled as inputs. All B_x pin directions can be controlled in this manner.

ACTIVE DIRECTION CONTROL

Sometimes it is necessary to be able to actively change the direction of the B_x pins without permanently dedicating them. Some applications which require this include Tri-state bus enable, multi-function decoding, etc. This can easily be done by programming the Control Gate to respond to one or more input pins. It is only necessary to select which I_x and B_x pins will control the pin directions and the active level HIGH (H) or LOW (L) that will be used. The PLS153 Program Table in Figure 15 shows the method of controlling B_0-B_9 with I_7. When I_7 is LOW (L), pins B_0-B_9 are outputs when I_7 is HIGH (H), pins B_0-B_9 are inputs. Note that by programming all other I_x and B_x pins as DON'T CARE (—), they are permanently discqnnected from control of B_x pin direction.


PROGRAM TABLE ENTRIES
OR
ACTIVE A
INACTIVE •
B (0)
CONTROL
HIGH H
LOW L
(POL.)
AND
INACTIVE 0
I, B H
I, B L
DON'T CARE —
I,B(I)
VARIABLE NAME
TB01840S

	AND																		OR									
POLARITY																												
	I								B(I)										B(0)									
TERM	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0																												
1																												
2																												
3																												
4																												
• • •																												
30																												
31																												
D9	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D8	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D7	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D6	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D5	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D4	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D3	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D2	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D1	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D0	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9										
VARIABLE NAME																												

NOTES:
1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I and B bits in the AND array are normally programmed Don't Care (—).
3. Unused product terms can be left blank.

Figure 15. Active Control of B_0-B_9 Using I_7 Active Low (L)

The previous 28-pin logic synthesis example (Page 2-5) could be done on the PLS153 as follows:

$X_0 = AB + \overline{C}D + B\overline{D}$

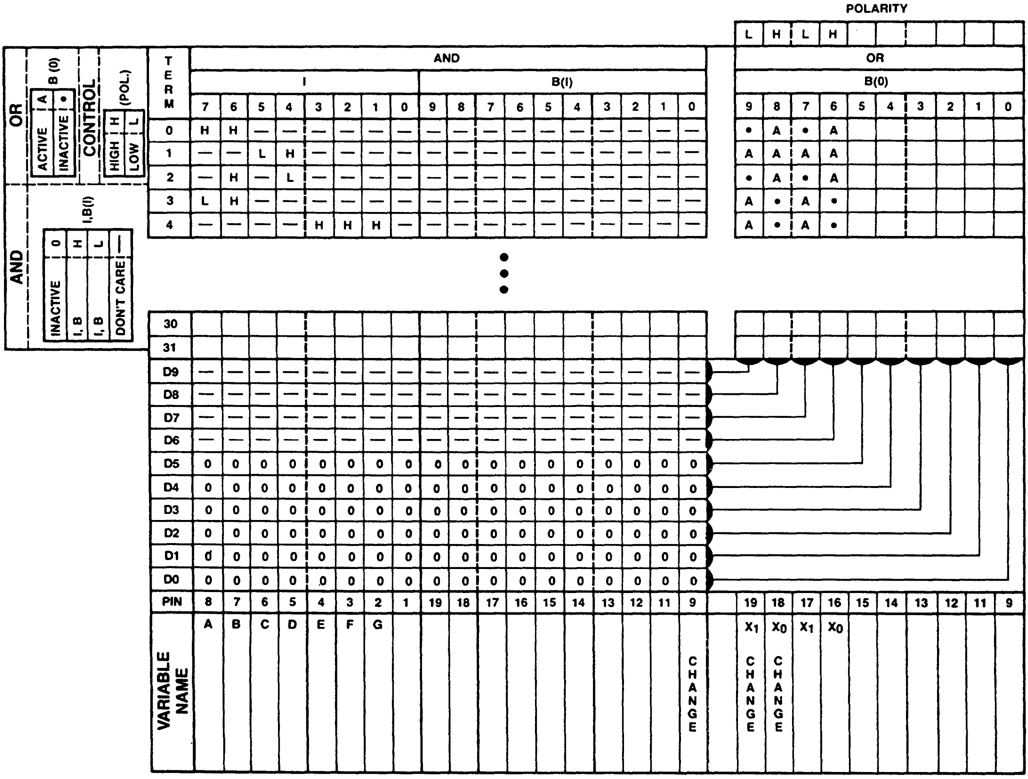
$\overline{X}_1 = \overline{A}B + \overline{C}D + EFG$

Note that B_0 was used as a CHANGE input. When B_0 is HIGH (H) the outputs appear on B_8 and B_9. When B_0 is LOW (L), the outputs appear on B_6 and B_7. B_1 through B_5 are not used and therefore left unprogrammed.

THE ROLE OF AMAZE (AUTOMATIC MAP AND ZAP ENTRY) IN LOGIC DEVELOPMENT

AMAZE is a software development package which provides the logic designer with a multimode data input capability. This software package, which has been developed for both mainframe and microcomputer environments, allows data entry in the program table format previously described, or on one of two equation formats. Both Boolean Logic Equations and State Variable Equations are supported on AMAZE. In addition to the flexible input formats offered, AMAZE also provides full device documentation, and a functional simulator. The simulator features manual and automatic modes. In the automatic mode, the software generates a set of input vectors which can be used as functional test vectors. The manual mode is an interactive procedure which allows the designer to input vectors to the simulator. The AMAZE simulator then responds with the appropriate output vector. In both modes, the simulator uses the functional model generated by the user's input data.

For more information on AMAZE refer to Section 8 of the 1987 Signetics Programmable Logic Data Manual.



PROGRAM TABLE ENTRIES

OR: B (0) — ACTIVE A, INACTIVE •

CONTROL (POL.) — HIGH H, LOW L

AND: I,B(I) — INACTIVE 0, I,B H, I,B L, DON'T CARE —

POLARITY																		L	H	L	H						
TERM	AND																	OR									
	I								B(I)									B(0)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0	H	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	•	A	•	A						
1	—	—	L	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A	A	A	A						
2	—	H	—	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	•	A	•	A						
3	L	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A	•	A	•						
4	—	—	—	—	H	H	H	—	—	—	—	—	—	—	—	—	—	—	A	•	A	•						
											• • •																	
30																												
31																												
D9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—										
D5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D1	d	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
D0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	19	18	17	16	15	14	13	12	11	9
VARIABLE NAME	A	B	C	D	E	F	G											CHANGE	X1 CHANGE	X0 CHANGE	X1	X0						

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Figure 16. PLS153 Example

SEQUENTIAL LOGIC CONSIDERATIONS

The PLS105 and PLS155 – PLS159 represent significant increases in complexity when compared to the combinatorial logic devices previously discussed. By combining the AND/OR combinatorial logic with clocked output flip-flops and appropriate feedback, Signetics has created the first family of totally flexible sequential logic machines.

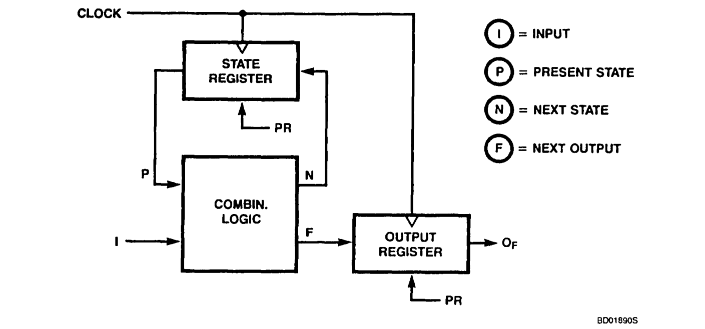


Figure 17. Basic Architecture of PLS105 FPLS. I, P, N, and F are Multi-line Paths Denoting Groups of Binary Variables Programmed by The User.

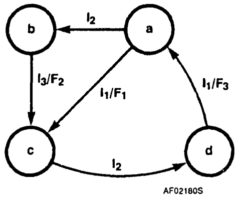


Figure 18. Typical State Diagram. I_{1-3} Are Jump Conditions Which Must be Satisfied Before Any Transitions Take Place. F_r Are Changes in Output Triggered by I_m, and Stored in The Output Register. State Transitions a → b and c → d Involve No Output Change.

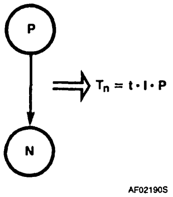


Figure 19. Typical State Transition Between Any Two States of Figure 18. The Arrow Connecting the Two States Gives Rise to a Transition Term T_n. I is the Jump Condition.

The PLS105 FPLS (Field-Programmable Logic Sequencer) is an example of a high-order machine whose applications are manifold. Application areas for this device include high-speed data controllers, microprocessor and minicomputer bus arbitration, industrial controls, timing generation, multi-function counters and shift registers, and microprocessor-driven microcontrollers. The PLS105 is fully capable of performing fast sequential operations in relatively low-speed processor systems. By placing repetitive sequential operations on the PLS105, processor overhead is reduced. Each PLS105 can be viewed as a high-speed, 48-state subroutine.

The following pages summarize the PLS105 architecture and features.

FPLS Architecture

The PLS105 Logic Sequencer is a programmable state machine of the Mealy type, in which the output is a function of the present state and the present input.

With the FPLS a user can program any logic sequence expressed as a series of jumps between stable states, triggered by a valid input condition (I) at clock time (t). All stable states are arbitrarily assigned and stored in the State Register. The logic output of the machine is also programmable, and is stored in the Output Register.

Clocked Sequence

A synchronous logic sequence can be represented as a group of circles interconnected with arrows. The circles represent stable states, labeled with an arbitrary numerical code (binary, hex, etc.) corresponding to discrete states of a suitable register. The arrows represent state transitions, labeled with symbols denoting the jump condition and the required **change** in output. The number of states in the sequence depends on the length and complexity of the desired algorithm.

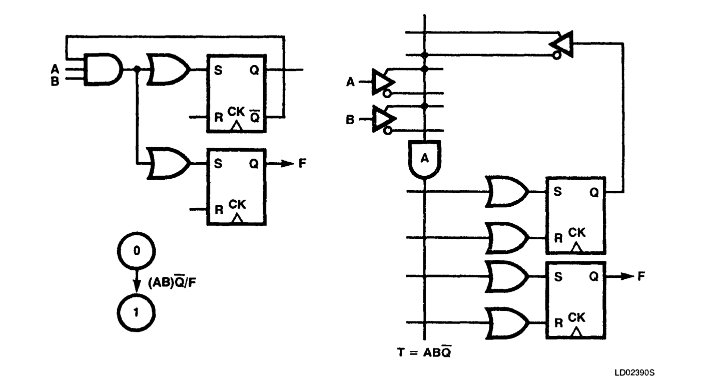


Figure 20. Typical State Jump From State (0) to State (1), if Inputs A = B = "1". The Jump Also Forces F = "1", as Required.

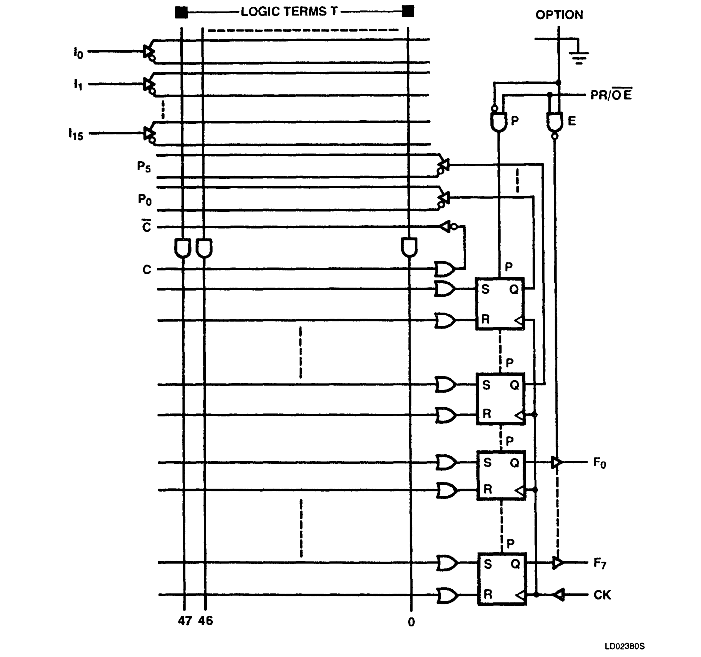


Figure 21. Simplified Logic Diagram of PLS105 FPLS

State Jumps

The state from which a jump originates is referred to as the Present state (P), and the state to which a jump terminates is defined as the Next state (N). A state jump always causes a change in state, but may or may not cause a change in machine output (F).

State jumps can occur only via "transition terms" T_n. These are logical AND functions of the clock (t), the Present state (P), and a valid input (I). Since the clock is actually applied to the State Register, $T_n = I \bullet P$. When T_n is "true", a control signal is generated and used at clock time (t) to force the contents of the State Register from (P) to (N), and to change the contents of the Output Register (if necessary). The simple state jump in Figure 20, involving 2 inputs, 1 state bit, and 1 output bit, illustrates the equivalence of discrete and programmable logic implementations.

FPLS Logic Structure

The FPLS consists of programmable AND and OR gate arrays which control the Set and Reset inputs of a State Register, as well as monitor its output via an internal feedback path. The arrays also control an independent Output Register, added to store output commands generated during state transitions, and to hold the output constant during state sequences involving no output changes. If desired, any number of bits of the Output Register can be used to extend the width of the State Register, via external feedback.

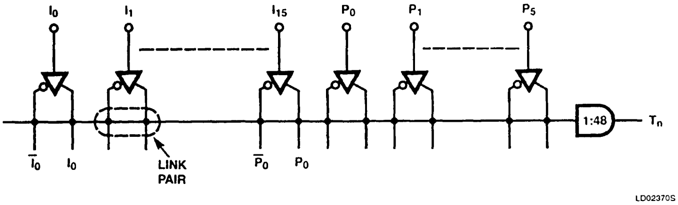


Figure 22. Typical AND Gate Coupled to (I) and (P) Inputs. If at Least One Link Pair Remains Intact, T_n is Unconditionally Forced Low.

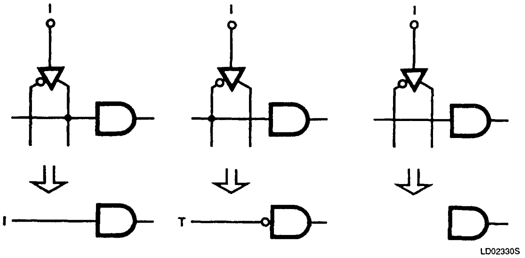


Figure 23. Choice of Input Polarity Coupling to a Typical AND Gate. With Both Links Open, (I) is Logically Don't Care.

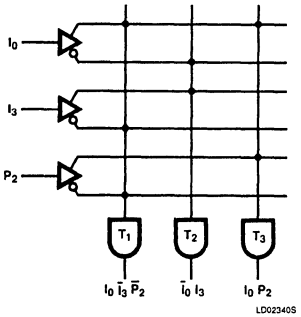


Figure 24. Typical Transition Terms Involving Arbitrary Inputs and State Variables. All Remaining Gate Inputs Are Programmed Don't Care. Note That T_2 Output Is State Independent.

Input Buffers

16 external inputs (I_m) and 6 internal inputs (P_s), fed back from the State Register, are combined in the AND array through two sets of True/Complement (T/C) buffers. There are a total of 22 T/C buffers, all connected to multi-input AND gates via fusible links which are initially intact.

Selective fusing of these links allows coupling either True, Complement, or Don't Care values of (I_m) and (P_s).

"AND" Array

State jumps and output changes are triggered at clock time by valid transition terms T_n. These are logical AND functions of the present state (P) and the present input (I).

The FPLS AND Array contains a total of 48 AND gates. Each gate has 45 inputs — 44 connected to 22 T/C input buffers, and 1 dedicated to the Complement Array. The outputs of all AND gates are propagated through the OR Array, and used at clock time (t) to force the contents of the State Register from (P) to (N). They are also used to control the Output Register, so that the FPLS 8-bit output F_r is a function of the inputs and present state.

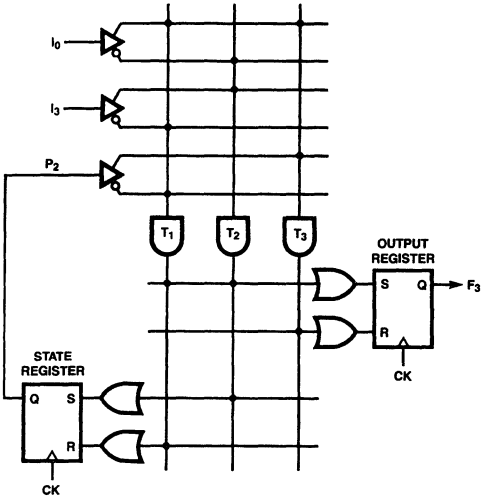


Figure 25. Typical OR Array Gating of Transition Terms $T_{1,2,3}$ Controlling Arbitrary State and Output Register Stages.

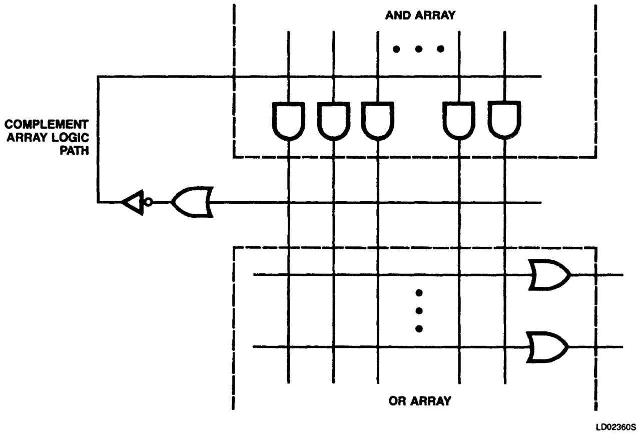


Figure 26. The COMPLEMENT Array is Logically Constructed from a 48-Input Programmable OR Gate Followed by an Inverter. All AND Terms Coupled to the OR Gate are Complemented at the Inverter Output, and Can be Fed Back as Inputs to the AND Array.

"OR" Array

In general, a clocked sequence will consist of several stable states and transitions, as determined by the complexity of the desired algorithm. All state and output changes in the state diagram imply changes in the contents of State and Output Registers.

Thus, each flip-flop in both registers may need to be conditionally set or reset several times with T_n commands. This is accomplished by selectively ORing through a programmable OR Array all AND gate outputs T_n necessary to activate the proper flip-flop control inputs.

The FPLS OR Array consists of 14 pairs of OR gates, controlling the S/R inputs of 14 State and Output Register stages, and a single OR gate for the Complement Array. All gates have 48 inputs for connecting to all 48 AND gates.

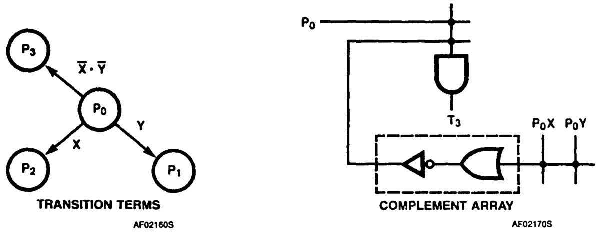
Complement Array

The COMPLEMENT Array provides an asynchronous feedback path from the OR Array back to the AND Array.

This structure enables the FPLS to perform both direct and complement sequential state jumps with a minimum of transition (AND) terms.

Typically direct jumps, such as T_1 and T_2 in Figure 27 require only a single AND gate each.

But a complement jump such as T_3 generally requires many AND gates if implemented as a direct jump. However, by using the Complement Array, the logic requirements for this type of jump can be handled with just one more gate from the AND Array.



DIRECT $\begin{cases} T_1 = P_0X \\ T_2 = P_0Y \end{cases}$

COMPLEMENT $\{$ $T_3 = P_0(\overline{X} \bullet \overline{Y}) = P_0(\overline{T_1 + T_2})$

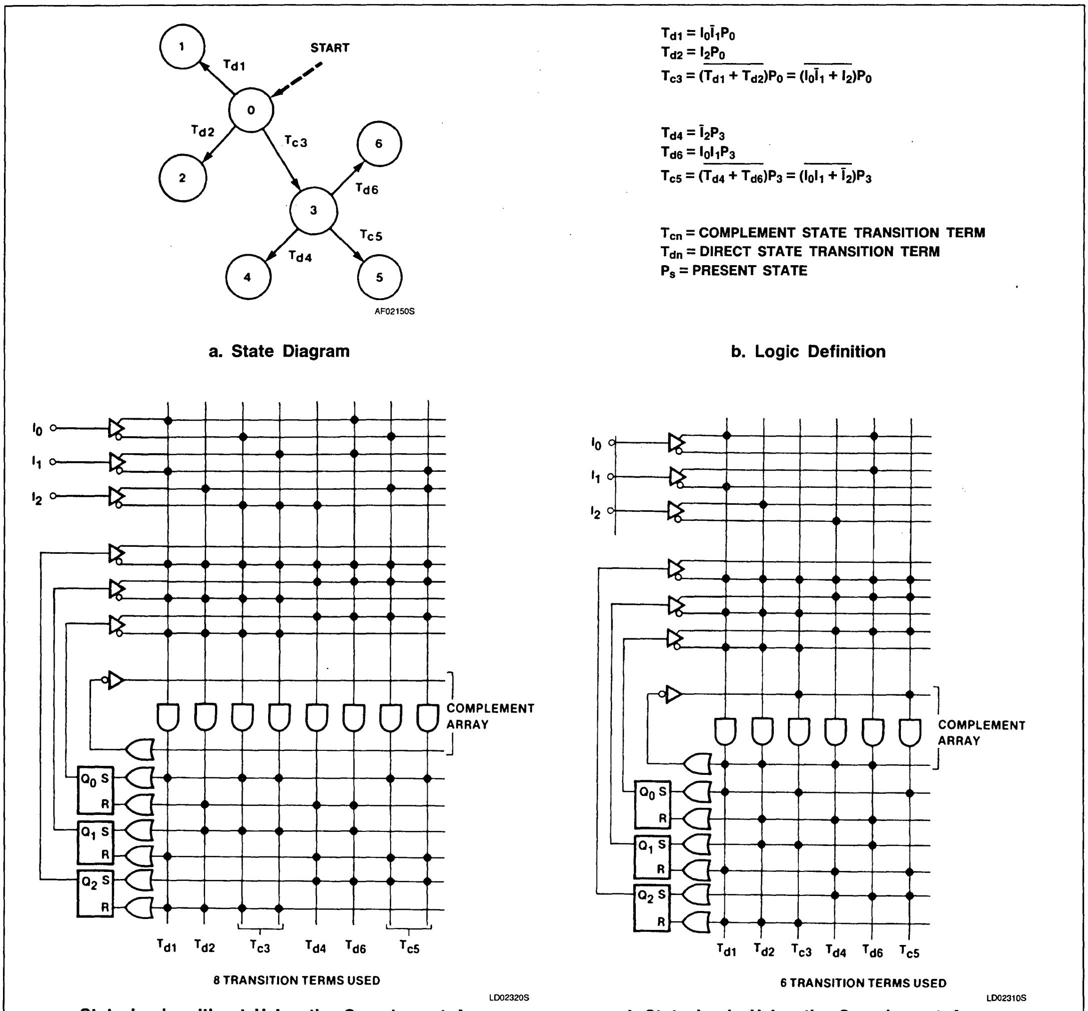
$$T_3 = P_0(\overline{P_0X + P_0Y})$$
$$T_3 = P_0\overline{[P_0(X + Y)]}$$
$$T_3 = P_0[\overline{P}_0 + \overline{(X + Y)}]$$
$$T_3 = 0 + P_0\overline{(X + Y)}$$
$$T_3 = P_0(\overline{X} \bullet \overline{Y})$$

a. Typical State Sequence

b. Complement Jump

Figure 27. a. X And Y Specify the Conditional Logic for Direct Jump Transition Terms T_1 and T_2. The Complement Jump Term T_3 is True Only When Both T_1 and T_2 are False. b. Note that the Complementary Logic Expression for T_3, $\overline{T_1 + T_2}$, Corresponds Exactly to the Logic Structure of the Complement Array.

As indicated in Figure 28, the single Complement Array gate may be used for many states of the state diagram. This happens because all transition terms linked to the OR gate include the present state as a part of their conditional logic. In any particular state, only those transition terms which are a function of that state are enabled; all other terms coupled to different states are disabled and do not influence the output of the Complement Array. As a general rule of thumb, the Complement Array can be used as many times as there are states.



$T_{d1} = I_0\bar{I}_1P_0$
$T_{d2} = I_2P_0$
$T_{c3} = \overline{(T_{d1} + T_{d2})}P_0 = \overline{(I_0\bar{I}_1 + I_2)}P_0$

$T_{d4} = \bar{I}_2P_3$
$T_{d6} = I_0I_1P_3$
$T_{c5} = \overline{(T_{d4} + T_{d6})}P_3 = \overline{(I_0I_1 + \bar{I}_2)}P_3$

T_{cn} = COMPLEMENT STATE TRANSITION TERM
T_{dn} = DIRECT STATE TRANSITION TERM
P_s = PRESENT STATE

a. State Diagram

b. Logic Definition

c. State Logic without Using the Complement Array

d. State Logic Using the Complement Array

Figure 28. Logic Reduction with the Complement Array. The Logic State Diagram in (a) Includes Complement Jumps T_{C3} and T_{C5} Defined in (b). When Using the Complement Array, a Savings of 2 Transition Terms Results, as Shown in (c) and (d).

Table 5. 20-Pin PLD Sequential Family Summary

DEVICE	REGISTERED OUTPUTS	OUTPUT TYPE
PLS155	4-Bit Register	T.S.
PLS157	6-Bit Register	T.S.
PLS159	8-Bit Register	T.S.

PLD-20 SEQUENTIAL DEVICES

The 20-pin PLD family also includes sequential devices. These devices are all similar in architecture. The major difference consists of the number of outputs which are registered.

FEATURES

The PLD-20 sequencers have been designed with a maximum of flexibility in mind. Each element of the architecture contributes to the ease of use the PLD-20 family provides. Each part has the features listed:

- **J/K flip-flop Output Register**
- **Dynamic control of flip-flop type (J/K or D)**
- **Parallel bus load**
- **Asynchronous preset and reset capability**
- **Combinational I/O pins**
- **Programmable enable pins**
- **Output feedback to AND Array available**

OUTPUT REGISTER

The Output Register of the PLD-20 sequential devices are comprised of fully implemented J/K flip-flops. Each flip-flop is positive edge-triggered from a common clock.

In addition, a dynamically controllable "fold-back" buffer between the J and K inputs to the flip-flop allows the designer to change the function of the flip-flop from J/K to D-type under the control of the flip-flop control term (F). A fuse allows the designer to dedicate the flip-flop as a permanent D-type by programming the fuse.

By leaving the fuse intact, the flip-flop control line (F) is maintained as the active mode control. If the output of F is logic Low (0), then the flip-flop is configured as a D-type. If the output of F is a logic High (1), then the flip-flop is configured as a J/K type. Term F is programmed in the same manner as the 32 logic transition terms (T). It is well to note at this time that when the flip-flop is configured as a D-type, the OR-term driving the K input of the flip-flop must not be active.

During all modes of operation, the output register data is fed back to the AND Array. This feedback is used to establish present-state to next-state jumps.

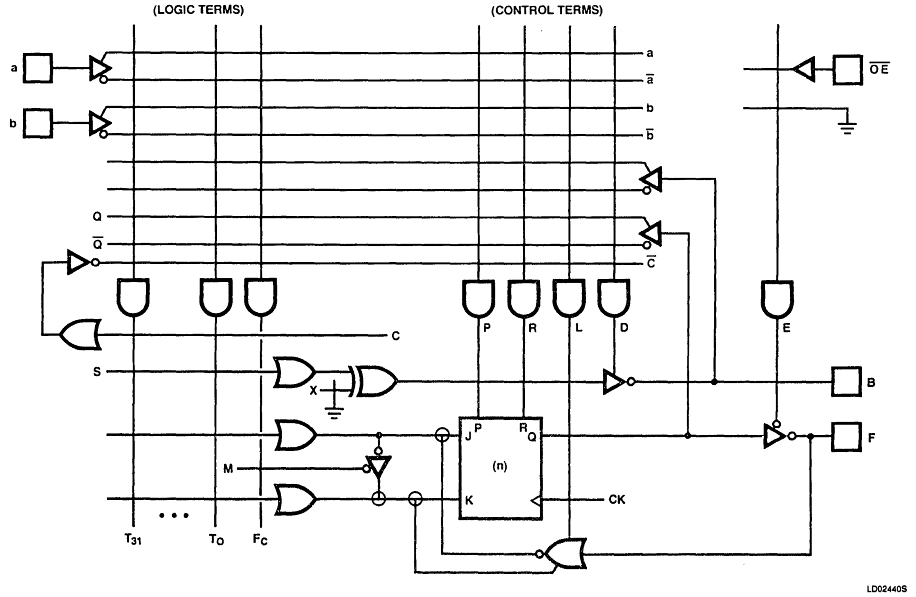


Figure 29

PARALLEL BUS LOADING

The Output Register may be loaded from the bus via the load control term (L). This feature forces the data contained on the F_0 pin into the J/K flip-flop. It operates synchronously with the rising edge of the clock. This feature can be used to preload a state into the machine, or to latch input data into the AND Array.

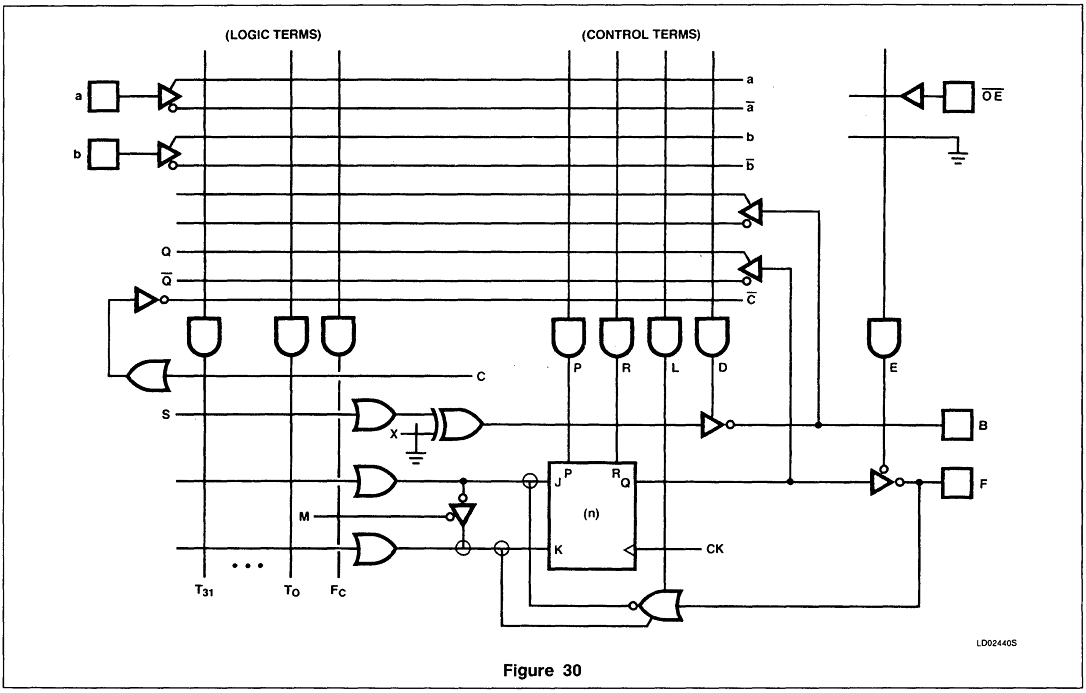


Figure 30

PRESET AND RESET

Asynchronous preset and reset capability has been provided on the PLD-20 sequential devices. This feature is controlled in the AND-Array on the PLS159. However, the preset and reset function on the PLS155 is controlled via the OR Array. The PLS157 preset and reset controls are split between the two arrays. See the individual data sheets for details.

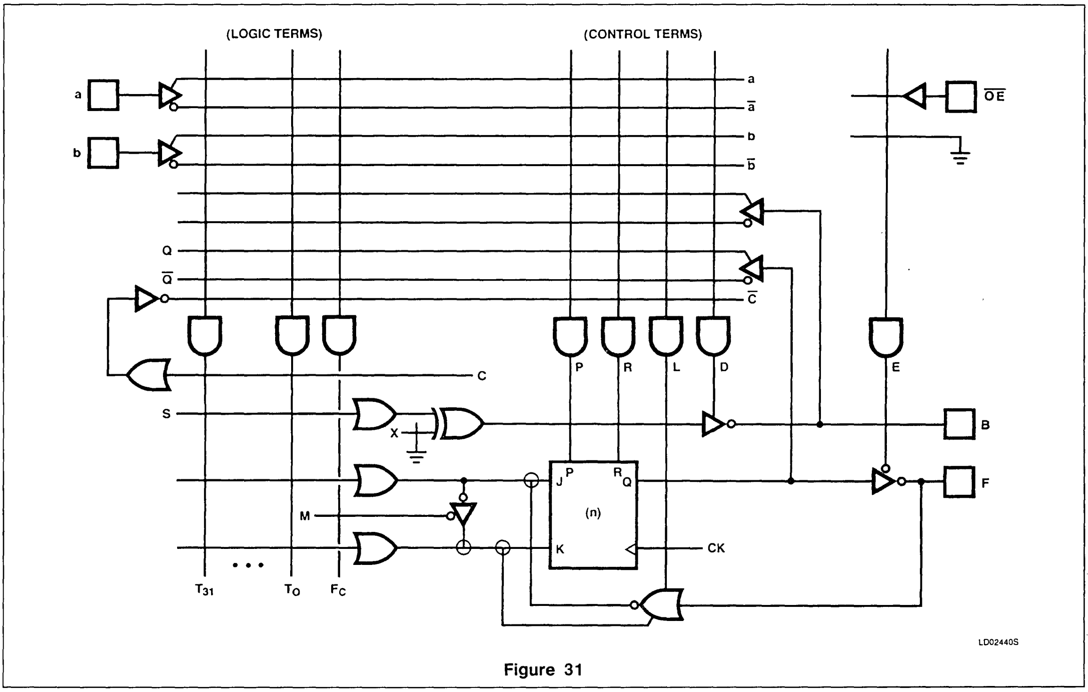


Figure 31

COMBINATIONAL I/O PINS

Each PLD-20 sequential device has a number of combinational pins (B_n) which can be programmed and used exactly as the B pins on the PLS153 FPLA. The direction control term (D) establishes the data flow on these pins. The individual data sheet should be consulted for the quantity and pin number assignment for each device.

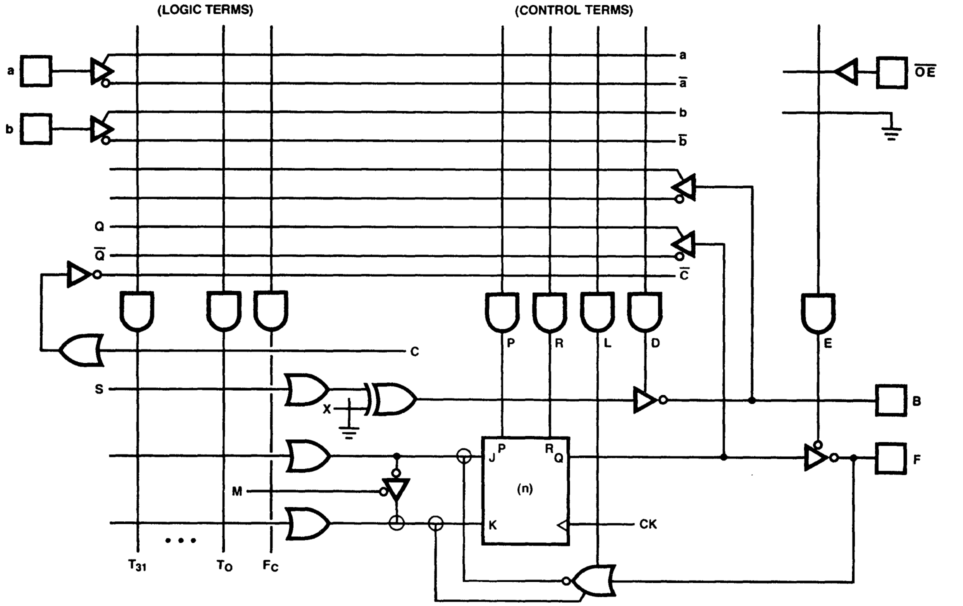
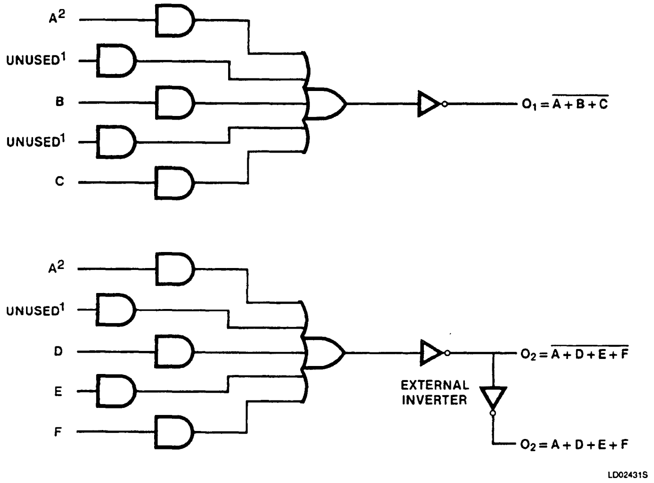


Figure 32

PLA vs. PAL® ARRAYS

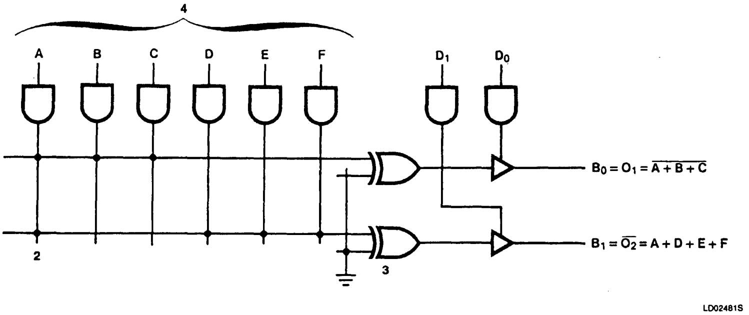
The PLA architecture provides the most efficient means of implementing logic. The 28-pin devices, PLS100/101 and PLS103 are unique in their ability to directly implement logic. They offer the most useable P-terms, the highest number of inputs and outputs, and the most straightforward programming of any logic device in the industry. The following diagrams illustrate the relative ease of programming the flexible PLA structure against the fixed OR Array of the PAL.

The Signetics approach to programmable logic gives the designer the flexibility he needs where he needs it — in the device itself. The combination of totally flexible architecture, more useable product terms, and ease of logic implementation make Signetics Programmable Logic Family the obvious choice.



NOTES:
1. Unused P-terms lost to designer.
2. Common P-term to 2 or more outputs requires 2 or more P-terms; one on each output.
3. External inverter required to change active level of output.
4. 10 P-terms used.

Figure 33. Application Example PAL Approach


4
A
B
C
D
E
F
D₁
D₀
B₀ = O₁ = $\overline{A+B+C}$
B₁ = $\overline{O_2}$ = A + D + E + F
2
3
LD02481S

NOTES:
1. All P-terms usable.
2. Common P-terms available to all outputs.
3. Programmable outputs eliminate need for external component.
4. 6 P-terms used.

Figure 34. PLD Approach

Quality and Reliability

SIGNETICS PROGRAMMABLE LOGIC QUALITY

Signetics has put together winning processes for manufacturing Programmable Logic. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The PLD's produced in the Application Specific Products Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from −55°C to +125°C and at +10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 - QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Bipolar Memory and Programmable Logic products, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: $T_J = 150°C$, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: $T_J = 150°C$, 1000 hours
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): -65°C to +150°C, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C, 100% saturated steam) and 300 cycles of thermal shock (-65°C to +150°C).

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality and Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the Programmable Logic SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100PPM (parts per million), down from an industry practice of 10,000PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

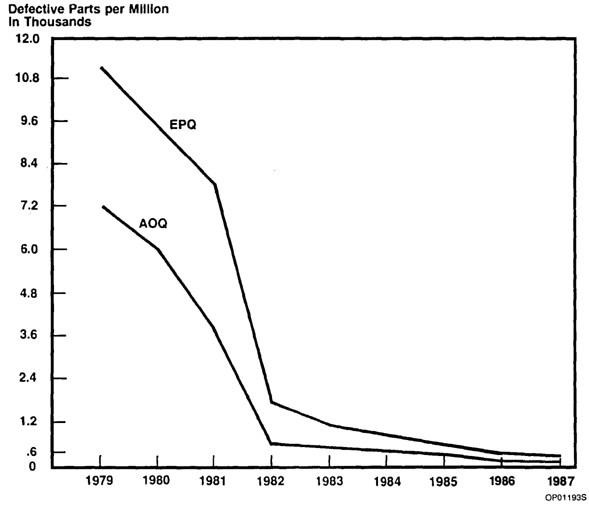


Figure 1. Signetics Quality Progress

Quality and Reliability

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed upon price. Signetics considers Performance to Customer Request and Performance to Original Schedule Date to be key Quality issues. Employees treat delinquencies as quality defects. They analyze the cause for the delinquency and seek corrective action to prevent future occurance. Continuous effort is given to try to acheive the ultimate goal of zero delinquencies.

ONGOING QUALITY PROGRAM

The quality improvement program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" – ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

PRODUCT QUALITY PROGRAM

To reduce defects in outgoing products, we created the Product Quality Program. This is managed by the Product Engineering Council, composed of the top product engineering and test professionals in the company. This group:

1. Sets aggressive product quality improvement goals;
2. provides corporate-level visibility and focus on problem areas;
3. serves as a corporate resource for any group requiring assistance in quality improvement; and
4. drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Quality and Reliability

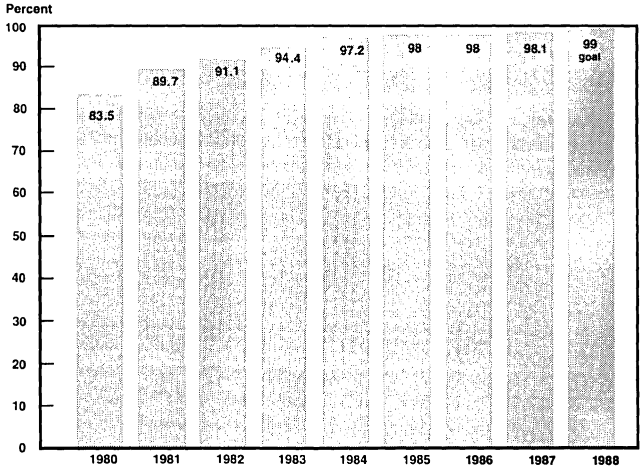


Figure 3. Lot Acceptance Rate From Signetics Vendors

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

MATERIAL WAIVERS

1988 - STD =	0 Waivers
1987 -	0
1986 -	0
1985 -	0
1984 -	0
1983 -	0
1982 -	2
1981 -	134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities – failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letter-head directly to the corporate V.P. of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. During the development of the program many profound changes were made. Figure 4, *Programmable Logic Process Flow*, shows the result. Key changes included such things as implementing 100% temperature testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of Programmable Logic. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

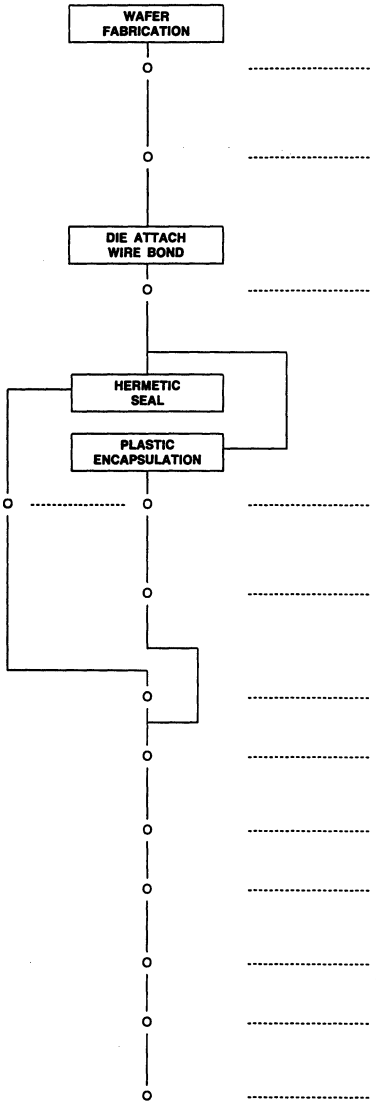
OUR GOAL: 100% PROGRAMMING YIELD

Our original goal back in the early 1970s was to develop a broad line of programmable products which would be recognized as having the best programming yield in the industry. Within the framework of a formal quality program, our efforts to improve circuit designs and refine manufacturing controls have resulted in major advances toward that goal.

Also within the framework of our formal quality program we have now established a stated goal of 100% programming yield. Through the increasing effectiveness of a quality attitude of "Do It Right The First Time" we're moving ever closer to that target.

Signetics PLD programming yields have been shown in collected data from internal audits and customer reporting to be consistently higher than comparable devices produced by our competition. We use systematic methods involving publication of exacting specifications of our programming algorithms, and through evaluation of those algorithms as implemented in industry standard programming equipment. Because of this we can assure our customers who program Signetics PLD's on such qualified equipment they will see consistently high yields. Our data base shows that average lot programming yield exceeds 97%.

Quality and Reliability



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

STABILIZATION BAKE PRECONDITIONING

Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance. Hermetic devices are baked to ensure the elimination of any remaining cavity moisture.

TEMPERATURE CYCLING (Monitor)

Using MIL-STD-883 Method 1010.1 Condition C devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during 100% electrical tests.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% gross leak testing.

100% PRODUCTION ELECTRICAL TEST

Every device is tested for functional and AC/DC parameters at high temperature with guard bands to assure performance to data sheet limits.

BURN IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum junction temperature.

SYMBOL

Devices are marked with the Signetics logo, device number and date code or custom symbol per individual specification requirements.

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics or customer documents.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested for functional and AC/DC parameters at 25°C with guard bands to assure performance to data sheet limits.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees that the specified mechanical and electrical tests have met Signetics Zero Defect Requirements. Every shipment is sealed and identified by QA personnel.

Figure 3. Application Specific Products Programmable Logic Process Flow

Quality and Reliability

As time goes on the drive for a product line that has Zero Defects will grow in intensity. These efforts will provide both Signetics and our customers with the ability to achieve the mutual goal of improved product quality.

The Application Specific Quality Assurance department has monitored PPM progress, which can be seen in Figure 4. We are pleased with the progress that has been made, and expect to achieve even more impressive results as the procedures for accomplishing these tasks are fine tuned.

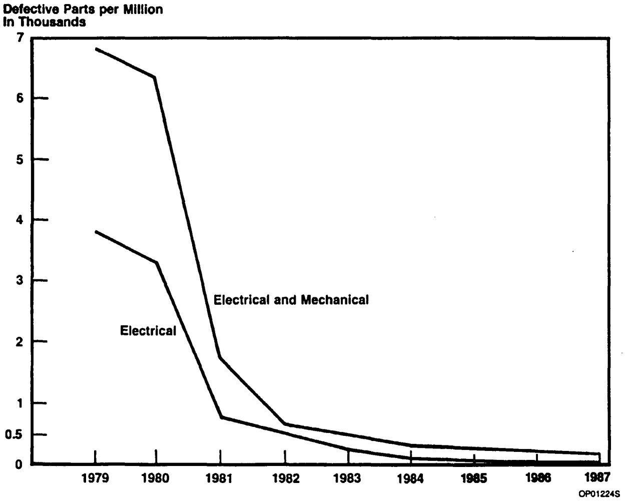


Figure 4. Programmable Logic EPQ (Estimated Process Quality)

Quality and Reliability

The Application Specific Reliability Department has established an ongoing Infant Mortality Monitor, the results of which can be seen in Figure 5. This monitor is used to determine and drive ongoing Corrective Action for the purposes of continuously improving product reliability.

The real measure of any quality improvement program is the result that our customers see. The meaning of *Quality* is more than just working circuits. It means commitment to *On Time Delivery* at the *Right Place* of the *Right Quantity* of the *Right Product* at the *Agreed Upon Price.*

Product Programmability, as illustrated in Figure 6, is continously monitored to assure that the highest performance possible is attained.

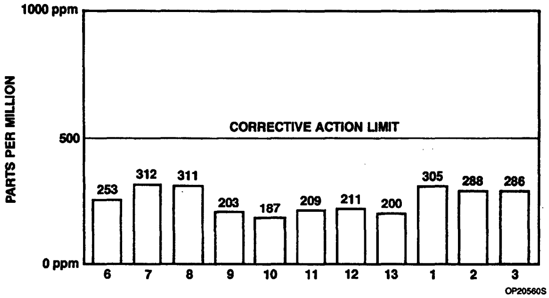


Figure 5. EPROM/EPLD Infant Mortality Monitor

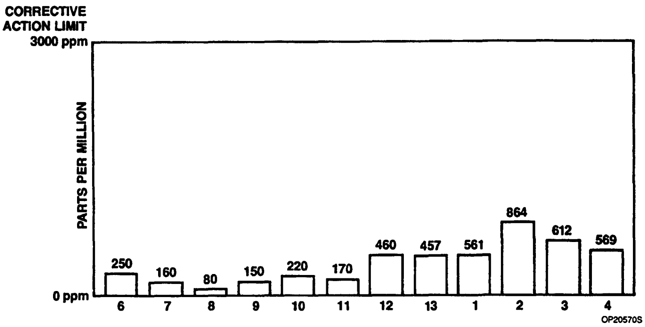


Figure 6. EPROM/EPLD Programmability Monitor

Quality and Reliability

CMOS RELIABILITY INFORMATION

All Signetics' EPROM die are designed as low power UV light erasable and electrically programmable read only memories. They have been designed to perform over military and commercial temperature ranges. These die are assembled in EPROM packages that comply with industry standard packages: Cerdip (Quartz window), Plastic DIP (One Time Programmable) and Plastic Leaded Chip Carrier (One Time Programmable).

The following descriptions are of the tests and calculations performed on each device organization and package type to validate the quality and reliability of the CMOS design and technology. All described tests are performed on each package type, with the exception of the 'Program-erase cycling' test for the One Time Programmable devices.

ELECTROSTATIC DISCHARGE PROTECTION (ESD)

This test is performed to validate the product's tolerance to electrostatic discharge damage.

Both MIL-STD-883 criteria (human body model) and mechanical model charged device test are performed.

HIGH TEMPERATURE STORAGE LIFE TEST (HTSL)

Another popular name for this test is data retention bake. This process is used to thermally accelerate charge loss from the floating gate. The test is performed by subjecting devices that contain a 100% programmed data pattern to a 250°C bake with no applied electrical bias or clocks.

In addition to charge loss, this test is used to detect mechanical reliability (i.e., bond integrity) and process instability.

DYNAMIC LOW TEMPERATURE LIFE TEST (DLTL)

This test is performed at −10°C to detect the effects of hot electron injection into the gate oxide as well as package-related failures (i.e., metal corrosion). The biasing and clocking conditions for this test are identical to the DHTL #1 test.

TEMPERATURE CYCLE (TMCL)

This test consists of performing 200 cycles of ambient air temperature of the chamber and housing the unbiased subject devices from −65°C to +150°C and back. The 200 cycles are performed at 20 minutes per cycle.

DYNAMIC HIGH TEMPERATURE LIFE TEST (DHTL #1)

This test is used to accelerate failure mechanisms by operating the devices at 125°C ambient temperature with worst-case specified power supply voltages of V_{CC} and V_{PP} at 5.5V. The memory is sequentially addressed to exercise the fully-loaded outputs. A checkerboard complement data pattern is used to simulate random patterns expected during actual use.

DYNAMIC HIGH TEMPERATURE LIFE TEST (DHTL #2)

This test is used to accelerate oxide breakdown failures and to further accelerate the failure mechanisms of DHTL #1. The test setup is identical to the one used for the DHTL #1 test except the temperature is 150°C and the V_{CC} and V_{PP} power supply voltages are 6.5V, resulting in a 20% increase over the specified operational electrical field across the gate oxides of the device (1.25mV/cm for 325Å oxide thickness). This represents a 55 × electrical field induced acceleration in addition to the thermal acceleration at 150°C.

PROGRAM-ERASE CYCLING AND PROGRAMMABILITY

All four power supply voltage combinations for V_{CC} and V_{PP} are tested for programmability ($V_{CC} = 6.0V \pm 0.25V$ and $V_{PP} = 12.5V \pm 0.5V$ in program mode). The number of possible program/erase cycles is then tested to establish program-erase cycling expectations.

FAILURE RATE PREDICTIONS

In preparation for the various life tests, a 168 hour, 125°C, 5.5V production burn-in is performed on the devices. The infant mortality rejects are removed from the population in order to develop long-term failure rate information during the random failure rate portion of the device life cycle.

The failure rate calculation combines all failure mechanisms by activation energies and associated device hours for the 125°C, 5.5V Dynamic Life Test (DHTL #1), the 150°C, 6.5V Dynamic Life Test (DHTL #2), the 150°C, 7.5V Static Life Test and the 250°C Bake.

The activation energies for the various EPROM failure mechanisms are:

Defective bit charge gain/loss (electron hopping conduction)	0.6eV
Oxide breakdown	0.3eV
Silicon defects	0.3eV
Contamination	1.0 – 1.2eV
Intrinsic charge loss	1.4eV

NOTE:
The combined failure rate for the stresses is the sum of failure rates by activation energies.

METHODS OF FAILURE RATE CALCULATIONS

Actual Device Hours = Number of Devices × Number of Hours. In order to determine the Equivalent Hours derated to a given operating temperature, the junction temperatures of the devices should be calculated using the known thermal resistance of the package (θ_{JA}) and the power dissipation of the devices:

$$T_{1,\,2} = \theta_{JA}\ (IV)_{1,\,2} + T_{A1,\,2} \qquad (1)$$

Using the Arrhenius relation, the test temperature and the derated operating temperature will yield the thermal acceleration factor from T_1 to T_2:

$$\frac{R_1}{R_2} = \frac{A \cdot \exp\left[\frac{E_A}{kT_1}\right]}{A \cdot \exp\left[\frac{E_A}{kT_2}\right]} = \exp\left[\frac{E_A}{k}\right]\left[\frac{1}{T_1} - \frac{1}{T_2}\right] \qquad (2)$$

k = 8.617 × 10^{-5} eV/Kelvin (Boltzmann's constant)

A = proportionality constant for a given failure mechanism

R_1 = mean time to failure @ T_1

R_2 = mean time to failure @ T_2

E_A = activation energy for the failure mechanism

T_1 = operating temperature

T_2 = life test temperature

An additional 55 × acceleration factor should be added for the 150°C/6.5V dynamic life test due to the time-dependent oxide failure acceleration (20% higher than specified power supply voltage).

Multiplying the actual device hours by the acceleration factor for each failure mechanism will result in the equivalent hours.

Poisson statistics are applied to estimate the performance of the population from the life test results of a sample test. This is useful when the probability of failures is small and the failures occur randomly in time. A commonly used formula for estimating the failure rate is the "chi-squared" equation:

$$F_C = \frac{\chi^2}{2nt} \times 100\% \qquad (3)$$

F_C = calculated failure rate estimate (in %/1000 hrs) at upper confidence limit

χ^2 = "chi-squared" value for $2F_A + 2$ degrees of freedom for α where F_A is the number of actual failures (χ^2 comes from available tables for a known α)

α = 1−B, where B is the confidence limit (B is stated in %).

n = number of units in test

t = test time in thousands of hours (equivalent)

Equation 3 will calculate the estimated failure rates/1000 hrs for 60% confidence level (industry standard) for each failure mechanism.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Memory products, samples are selected that represent product groups from all wafer fabrication and assembly locations.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Signetics

Application Specific Products

Section 3
PAL®-Type Device Data Sheets

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Series 20

PLC16V8 Erasable and OTP PAL®-Type Device 3-3
PLHS16L8A PAL®-Type Device 3-13
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PLUS16R8D PAL®-Type Devices 3-27
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Signetics

PLC16V8 Series
Erasable and OTP PAL®-Type Device

Signetics Programmable Logic
Product Specification

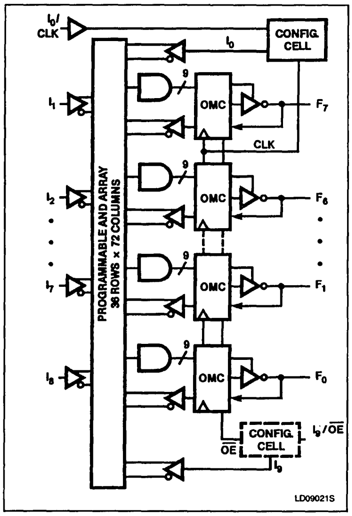
Application Specific Products
• Series 20

DESCRIPTION

The PLC16V8 Programmable Array Logic device is a 20-pin CMOS PLD designed to replace full-power as well as quarter-power and half-power Series 20 PAL® devices. Available in four speed/power configurations, the generic PLC16V8 device can be configured to emulate 22 different PAL devices in multiple speed/power configurations. The more complex AND/OR logic functions can be easily implemented with the PLC16V8 because of the flexibility inherent to its generic Output Macro Cell architecture.

The PLC16V8 is a two-level logic element comprised of 10 inputs, 72 AND gates and 8 Output Macro Cells (OMC). Each Output Macro Cell can be individually configured as a dedicated input, a dedicated output, a bidirectional I/O or as a registered output with feedback. This generic architecture provides a means of reducing documentation, inventory and manufacturing related costs. Furthermore, the PLC16V8 series devices are designed to accept both TTL and CMOS input levels to facilitate logic integration in almost any system environment.

FUNCTIONAL DIAGRAM



FEATURES

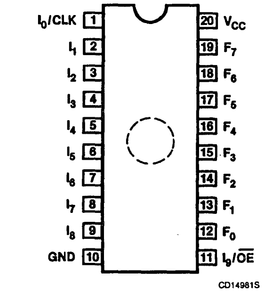
- **100% functional replacement for Series 20 PAL devices**
  $-I_{OL}$ = 24mA
- **Low power performance: 50 and 90mA max**
  - **All inputs and outputs switching at 15MHz**
- **Equivalent bipolar performance**
  - **35 and 45ns t_{PD}**
  - **28.5 and 22.2MHz f_{MAX} (async)**
- **EPROM cell technology**
  - **Erasable**
  - **100% testable**
  - **Reconfigurable (quartz window package only)**
- **TTL and CMOS compatible**
- **Security fuse**
- **Available in 300mil-wide DIP with quartz window, plastic DIP (OTP), or PLCC (OTP)**

PIN LABEL DESCRIPTIONS

I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)

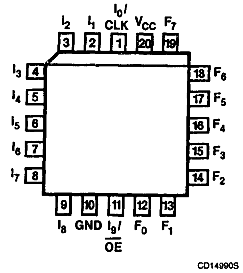
PIN CONFIGURATIONS

N and FA Packages



N = Plastic
FA = Ceramic with Quartz Window

A Package



A = Plastic Leaded Chip Carrier

PAL DEVICE TO PLC16V8 OUTPUT PIN CONFIGURATION CROSS REFERENCE

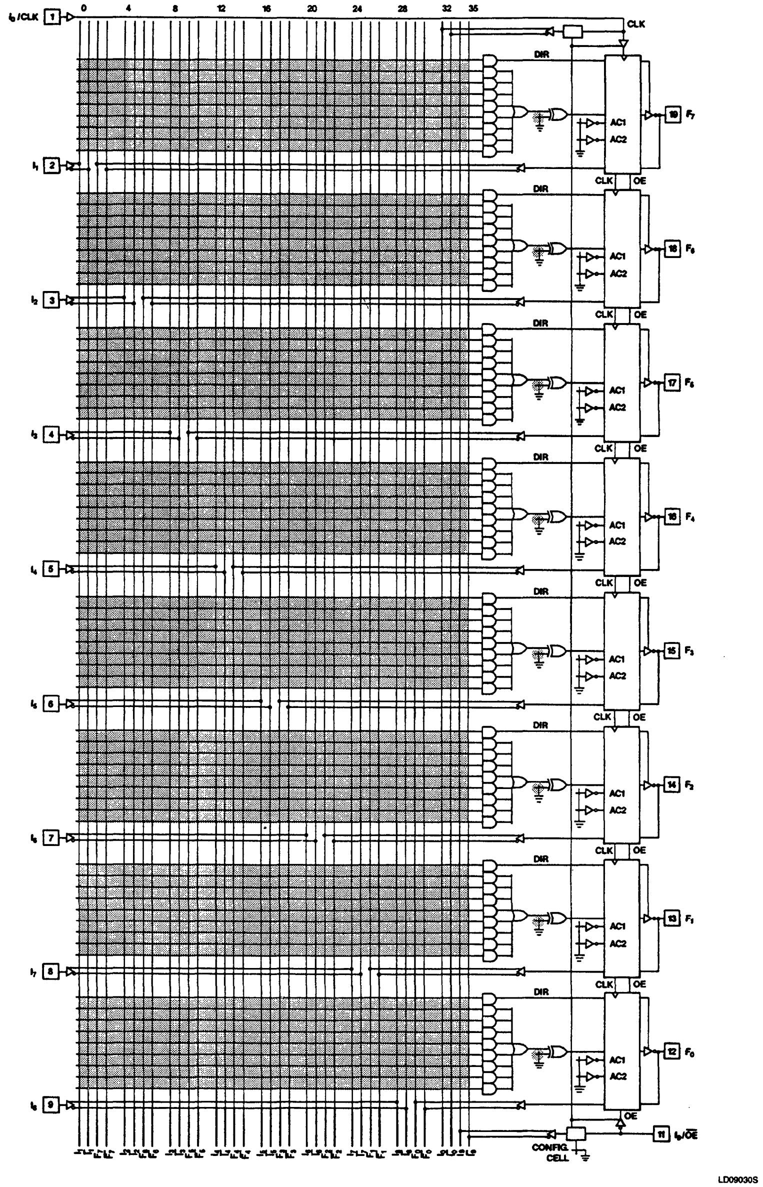
PIN NO.	PLC 16V8	16L8 16H8 16P8 18P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	$I_9/\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

® PAL is a registered trademark of Monolithic Memories, Inc., a wholly owned subsidiary of Advanced Micro Devices, Inc.

Erasable and OTP PAL®-Type Device

PLC16V8 Series

LOGIC DIAGRAM



NOTES:

In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is non-inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
⊕ Denotes a programmable cell location.

Erasable and OTP PAL®-Type Device

PLC16V8 Series

The Signetics state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at one-quarter to one-half the power consumption. The erasable nature of the EPROM process enables Signetics to functionally test the devices prior to shipment to the customer. Additionally, this allows Signetics to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

Signetics' AMAZE PLD design software supports all aspects of design, simulation and programming. For simple conversion of existing PAL device codes into the PLC16V8 series format, a PAL-to-V8 Converter is also available. This stand-alone, single-disk software package translates a PAL device code (from a device or a JEDEC standard fuse map) into an equivalent PLC16V8 series JEDEC format. The PAL-to-V8 converter, which runs on an IBM PC or compatible, includes the necessary programmer interface software for most commercially available programmers.

THE OUTPUT MACRO CELL (OMC)

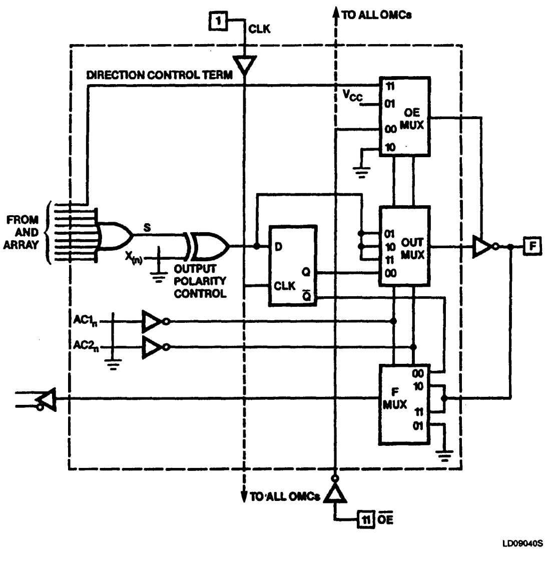
The PLC16V8 has 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the table, 4 different configurations may be implemented.

FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_n$	$AC2_n$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registered OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

OUTPUT MACRO CELL (OMC)



NOTE:
□ Denotes a programmable cell location.

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common — from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follow:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

Erasable and OTP PAL®-Type Device

PLC16V8 Series

ORDERING INFORMATION

DESCRIPTION			ORDER CODE
Propagation Delay (Max)		I_{CC} (Active at 15MHz)	
t_{PD} = 35ns	f_{MAX} = 18.1MHz (Synchronous)	50mA	PLC16V8Q35
		90mA	PLC16V8H35
t_{PD} = 45ns	f_{MAX} = 13.3MHz (Synchronous)	50mA	PLC16V8Q45
		90mA	PLC16V8H45
Package Type			PACKAGE[1]
20-pin Plastic DIP (one time programmable; OTP)			N
20-pin Plastic Leaded Chip Carrier			A
20-pin Ceramic DIP with quartz window (reprogrammable)			FA

NOTE:
1. The package order code directly follows the device order code, i.e., PLC16V8Q35N for Plastic DIP (OTP).

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V_{DC}
V_{IN}	Input voltage	-0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	-0.5 to V_{CC} +0.5	V_{DC}
I_{IN}	Input currents	-10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

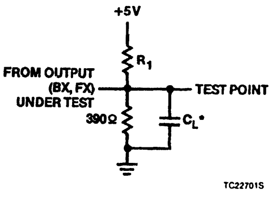
NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLC16V8 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

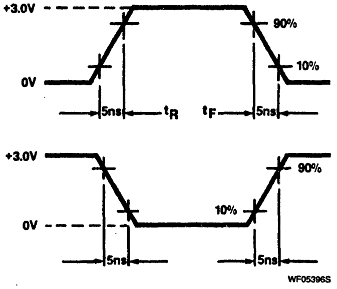
AC TEST CONDITIONS



*CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Erasable and OTP PAL®-Type Device

PLC16V8 Series

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min	−0.3		0.8	V
V_{IH}	High	V_{CC} = Max	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = Min I_{OL} = 24mA			0.5	V
V_{OH}	High	I_{OH} = −3.2mA	2.4			V
Input current						
I_{IL}	Low[6]	V_{IN} = GND			−10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 −10	µA µA
I_{OS}	Short-circuit[3, 7]	V_{OUT} = GND			−130	mA
I_{CC}	V_{CC} supply current (Active)[4]	I_{OUT} = 0mA f = 15MHz[5] Quarter power (Q)			50	mA
		Half power (H)			90	mA
Capacitance						
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all inputs and outputs switching.
5. Refer to Figure 1, ΔI_{CC} vs Frequency (worst case). (Referenced from 15MHz)
6. I_{IL} for Pin 1 (I_0/CLK) is ±10µA with V_{IN} = 0.4V.
7. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.

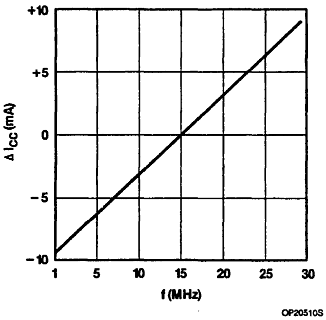


Figure 1. ΔI_{CC} **vs Frequency (Worst Case) (Referenced from 15MHz)**

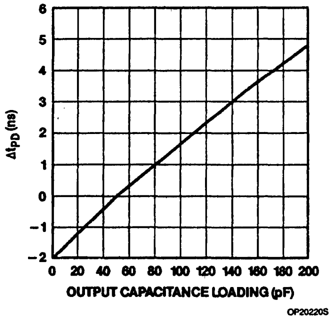


Figure 2. Δt_{PD} **vs Output Capacitance Loading (Typical)**

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$ $R_2 = 390\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION[1]		PLC16V8Q-35 PLC16V8H-35		PLC16V8Q-45 PLC16V8H-45		UNIT
				R_1 (Ω)	C_L (pF)	Min	Max	Min	Max	
Pulse width										
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +			55		75		ns
t_{CKH}	Clock width High	CLK –	CLK +			20		25		ns
t_{CKL}	Clock width Low	CLK +	CLK –			20		25		ns
Hold time										
t_{IH}	Input or feedback data hold time	Input ±	CLK +			0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	CLK +	I ±, F ±			30		40		ns
Propagation delay										
t_{PD}	Delay from input to active output	F ±	I ±, F ±	200	50		35		45	ns
t_{CKO}	Clock High to output valid access Time	F ±	CLK +	200	50		25		35	ns
t_{OE1}[3]	Product term enable to active output	F ±	I ±, F ±	Active-High R = 1.5k Active-Low R = 550	50		35		45	ns
t_{OD1}[2]	Product term disable to outputs off	F ±	I ±, F ±	From V_{OH} R = ∞ From V_{OL} R = 200	5		35		45	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	F ±	OE –	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		30	ns
t_{OE2}[3]	Pin 11 output enable to active output	F ±	OE +	Active-High R = 1.5k Active-Low R = 550	50		25		30	ns
t_{PPR}	Power-up reset	F +	V_{CC} +				35		45	ns
Frequency of operation ($t_{IS} + t_{CKO}$)										
f_{MAX}	Maximum frequency	Synch. Asynch.		200	50		18.1 28.5		13.3 22.2	MHz

NOTES:

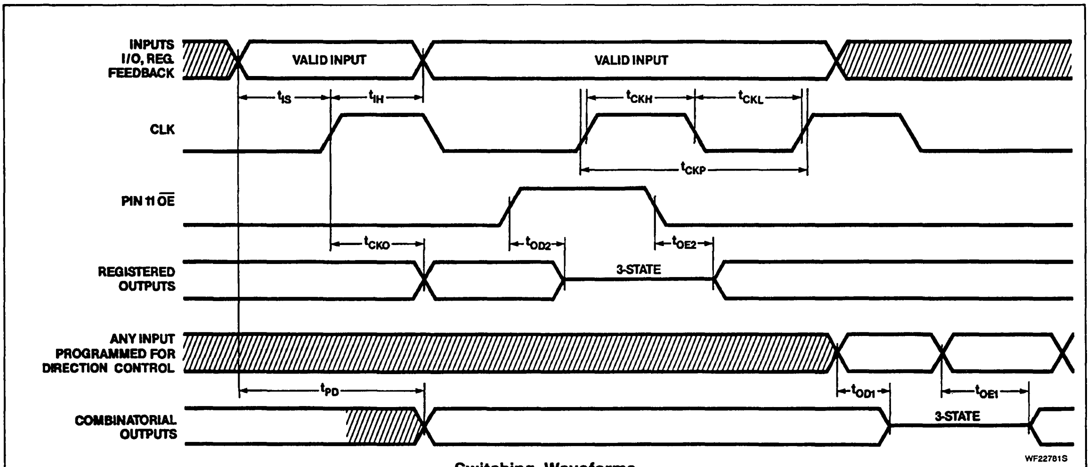
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. 3-State levels are measured ±0.5V from the active steady-state level.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.

POWER-UP RESET

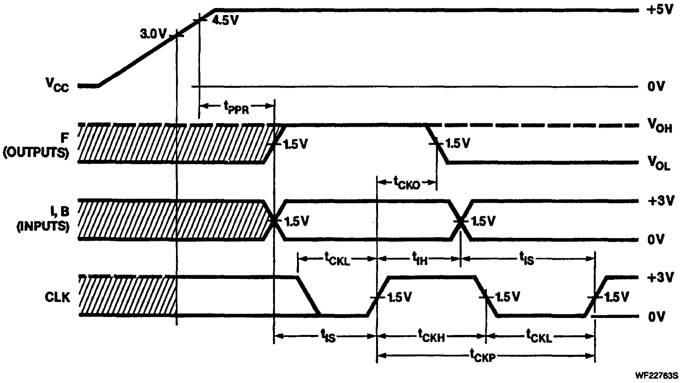
In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC16V8. All internal registers will reset to active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an active-High on the associated output pin because of the inverted output buffer. The internal feedback ($\overline{Q}$) of a registered OMC will also be set High. The programmed polarity of OMC will not affect the active-High output condition during a system power-up condition.

The following conditions must be considered when the asynchronous power-up reset occurs. V_{CC} rise to 4.5V (90%) must be monotonic. The clock input must stabilize to a valid TTL level prior to the V_{CC} rise to 60% (3.0V). All input setup and hold times (t_{IS} and t_{IH}) must be adhered to prior to clocking the device.

TIMING DIAGRAMS



Switching Waveforms



NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output conditon (enabled or disabled).

Power-Up Reset

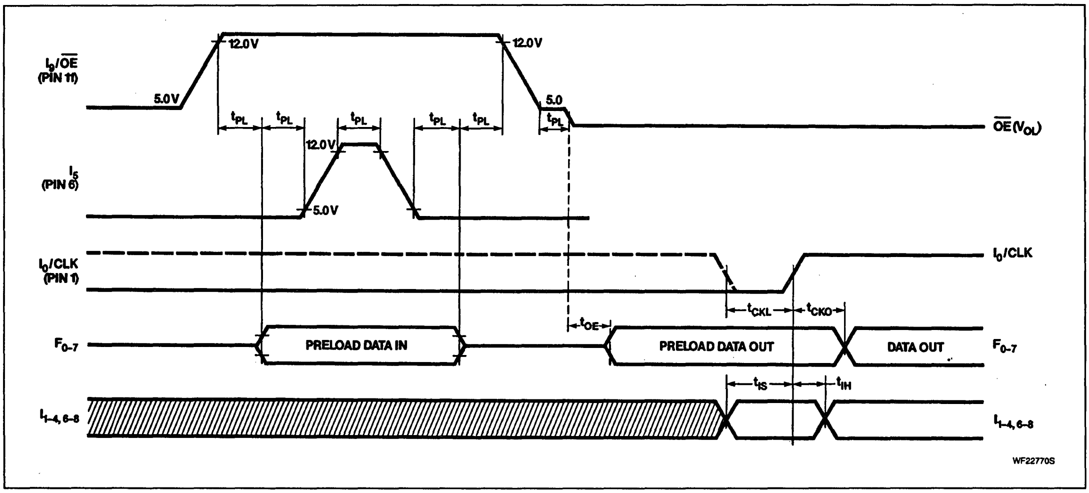
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC16V8 series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_9/\overline{OE}$ and I_5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register $\overline{Q}$ output via the feedback path will reflect the complement of the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references.

REGISTER PRELOAD (DIAGNOSTIC MODE)



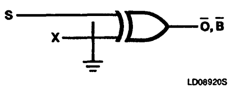
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic Programming equipment.

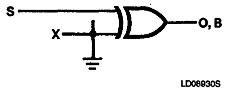
With Logic programming, the AND/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2, as shown below. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY — (O, B)

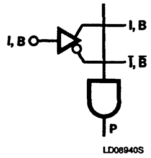


ACTIVE LEVEL	CODE
INVERTING	L

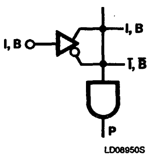


ACTIVE LEVEL	CODE
NON-INVERTING	H

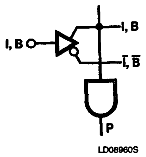
"AND" ARRAY — (I, B)



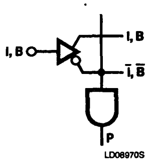
STATE	CODE
DON'T CARE	-



STATE	CODE
INACTIVE[1]	O

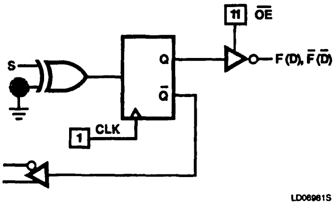


STATE	CODE
I, B	H

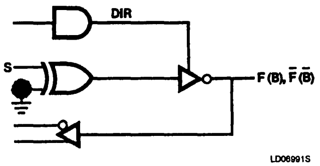


STATE	CODE
Ī, B̄	L

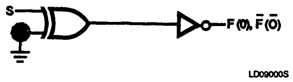
ARCHITECTURE CONTROL — AC1 and AC2



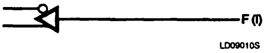
OMC CONFIGURATION	CODE
REGISTERED (D-TYPE)	D



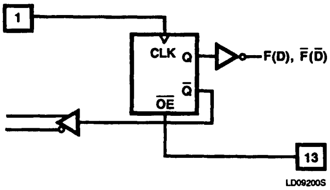
OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B



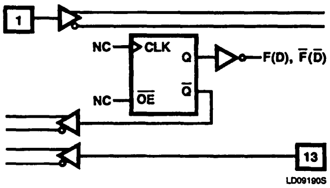
OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I



CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = OE	L



CONFIGURATION CELL	CODE
PIN 1 = INPUT 11 = INPUT	H[6]

NOTE:

A factory shipped unprogrammed device is configured such that:

1. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is non-inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and ŌE functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC16V8 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 - 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC16V8 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC16V8 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC16V8 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage:

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAM TABLE

CONFIGURATION CELL (CLK/$\overline{OE}$ CONTROL) □

ARCH. CONTROL BITS □□□□□□□□

OUTPUT POLARITY □□□□□□□□

NOTES:
In the unprogrammed or virgin state:
- All AND gate locations are pulled to a logic "0" (Low).
- Output polarity is non-inverting.
- Pins 1 and 11 are configured as inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
- All output macro cells (OMC) are configured as combinatorial I/O, with the outputs disabled via the direction control term.

CUSTOMER NAME ____________

PURCHASE ORDER # ____________

SIGNETICS DEVICE # ____________ CF (XXXX) ____________

CUSTOMER SYMBOLIZED PART # ____________

TOTAL NUMBER OF PARTS ____________

PROGRAM TABLE # ____________ REV. ________ DATE ________

TERM	AND																		OR (FIXED)							
	I										F (I)								F (B, O, D)							
	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																			D	/	/	/	/	/	/	/
1																			A	/	/	/	/	/	/	/
2																			A	/	/	/	/	/	/	/
3																			A	/	/	/	/	/	/	/
4																			A	/	/	/	/	/	/	/
5																			A	/	/	/	/	/	/	/
6																			A	/	/	/	/	/	/	/
7																			A	/	/	/	/	/	/	/
8																			A	/	/	/	/	/	/	/
9																			/	D	/	/	/	/	/	/
10																			/	A	/	/	/	/	/	/
11																			/	A	/	/	/	/	/	/
12																			/	A	/	/	/	/	/	/
13																			/	A	/	/	/	/	/	/
14																			/	A	/	/	/	/	/	/
15																			/	A	/	/	/	/	/	/
16																			/	A	/	/	/	/	/	/
17																			/	A	/	/	/	/	/	/
18																			/	/	D	/	/	/	/	/
19																			/	/	A	/	/	/	/	/
20																			/	/	A	/	/	/	/	/
21																			/	/	A	/	/	/	/	/
22																			/	/	A	/	/	/	/	/
23																			/	/	A	/	/	/	/	/
24																			/	/	A	/	/	/	/	/
25																			/	/	A	/	/	/	/	/
26																			/	/	A	/	/	/	/	/
27																			/	/	/	D	/	/	/	/
28																			/	/	/	A	/	/	/	/
29																			/	/	/	A	/	/	/	/
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35																			/	/	/	A	/	/	/	/
36																			/	/	/	/	D	/	/	/
37																			/	/	/	/	A	/	/	/
38																			/	/	/	/	A	/	/	/
39																			/	/	/	/	A	/	/	/
40																			/	/	/	/	A	/	/	/
41																			/	/	/	/	A	/	/	/
42																			/	/	/	/	A	/	/	/
43																			/	/	/	/	A	/	/	/
44																			/	/	/	/	A	/	/	/
45																			/	/	/	/	/	D	/	/
46																			/	/	/	/	/	A	/	/
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51																			/	/	/	/	/	A	/	/
52																			/	/	/	/	/	A	/	/
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58																			/	/	/	/	/	/	A	/
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60																			/	/	/	/	/	/	A	/
61																			/	/	/	/	/	/	A	/
62																			/	/	/	/	/	/	A	/
63																			/	/	/	/	/	/	/	D
64																			/	/	/	/	/	/	/	A
65																			/	/	/	/	/	/	/	A
66																			/	/	/	/	/	/	/	A
67																			/	/	/	/	/	/	/	A
68																			/	/	/	/	/	/	/	A
69																			/	/	/	/	/	/	/	A
70																			/	/	/	/	/	/	/	A
71																			/	/	/	/	/	/	/	A
PIN	11	9	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	19	18	17	16	15	14	13	12
VARIABLE NAME																										

AND ARRAY

INACTIVE	O
I, F (I, B)	H
I, F ($\overline{I}$, $\overline{B}$)	L
DON'T CARE	—

CONTROL

OMC ARCH.

REGISTERED (D-TYPE)	D
FIXED INPUT	I
FIXED OUTPUT	O
BIDIRECTIONAL I/O	B

OUTPUT POLARITY

NON-INVERTING	H
INVERTING	L

CONFIG. CELL*

PIN 1 = CLK; PIN 11 = $\overline{OE}$	L
PIN 1, PIN 11 = INPUT	H

OR ARRAY (FIXED)

DATA CANNOT BE ENTERED INTO THE OR ARRAY FIELD DUE TO THE FIXED NATURE OF THE DEVICE ARCHITECTURE.

DIRECTION CONTROL	D
ACTIVE OUTPUT	A
NOT USED	/

* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.

TB03610S

Signetics

PLHS16L8A
PAL®-Type Device

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLHS16L8A is a high-speed "A" version PAL®-type device. The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 OR gates. The Signetics PLHS16L8A offers 100% functional compatibility with other PAL 16L8 devices. Specified at a tpd of 20ns (maximum), the PLHS16L8A is 20% faster than other "A" version PAL 16L8 devices. And, the PLHS16L8A consumes 20% less power than most other "A" speed 16L8 devices.

All AND gates are linked to 10 dedicated inputs, 6 bidirectional I/O and 2 dedicated outputs. On-chip buffers couple either true (I, B) or complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates. The 64 AND gates are separated into eight groups of eight product terms each. Within each group, seven of the AND terms are OR'ed together, while the eighth is used to control the 3-State function of the bidirectional I/O. All outputs (bidirectional and dedicated) are inverting.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs, which act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

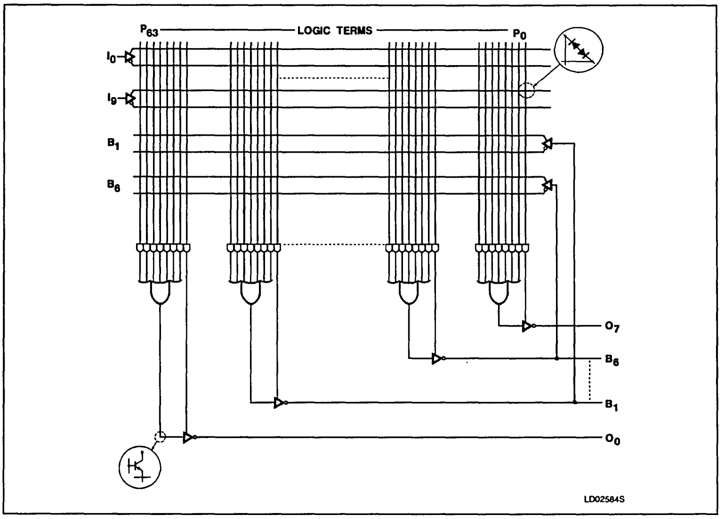
The PLHS16L8A is field-programmable, allowing the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

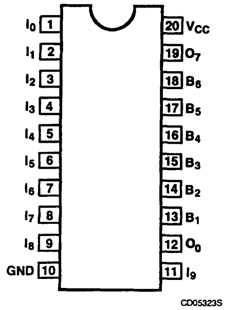
- **20% faster than other "A" version PAL devices**
  - **t_{pd} = 20ns (MAX)**
- **I_{CC} supply current: 155mA (worst-case)**
- **100% functionally and pin-for-pin compatible with AmPAL16L8A, MMI PAL16L8A, TIBPAL16L8-25 and NSC PAL16L8A devices**
- **Field-programmable**
- **10 dedicated inputs**
- **8 outputs**
  - **6 bidirectional I/O**
  - **2 dedicated outputs**
- **Individual 3-State control of all outputs**
- **64 AND gates/product terms**
- **Security Fuse**

FUNCTIONAL DIAGRAM

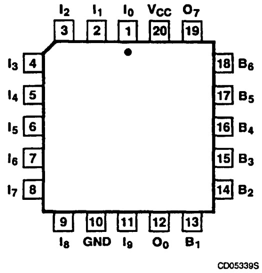


PIN CONFIGURATIONS

N Package



A Package



APPLICATIONS

- **100% functional replacement for 20-pin 16L8 combinatorial PAL devices**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping/decoding**
- **Multiplexing**

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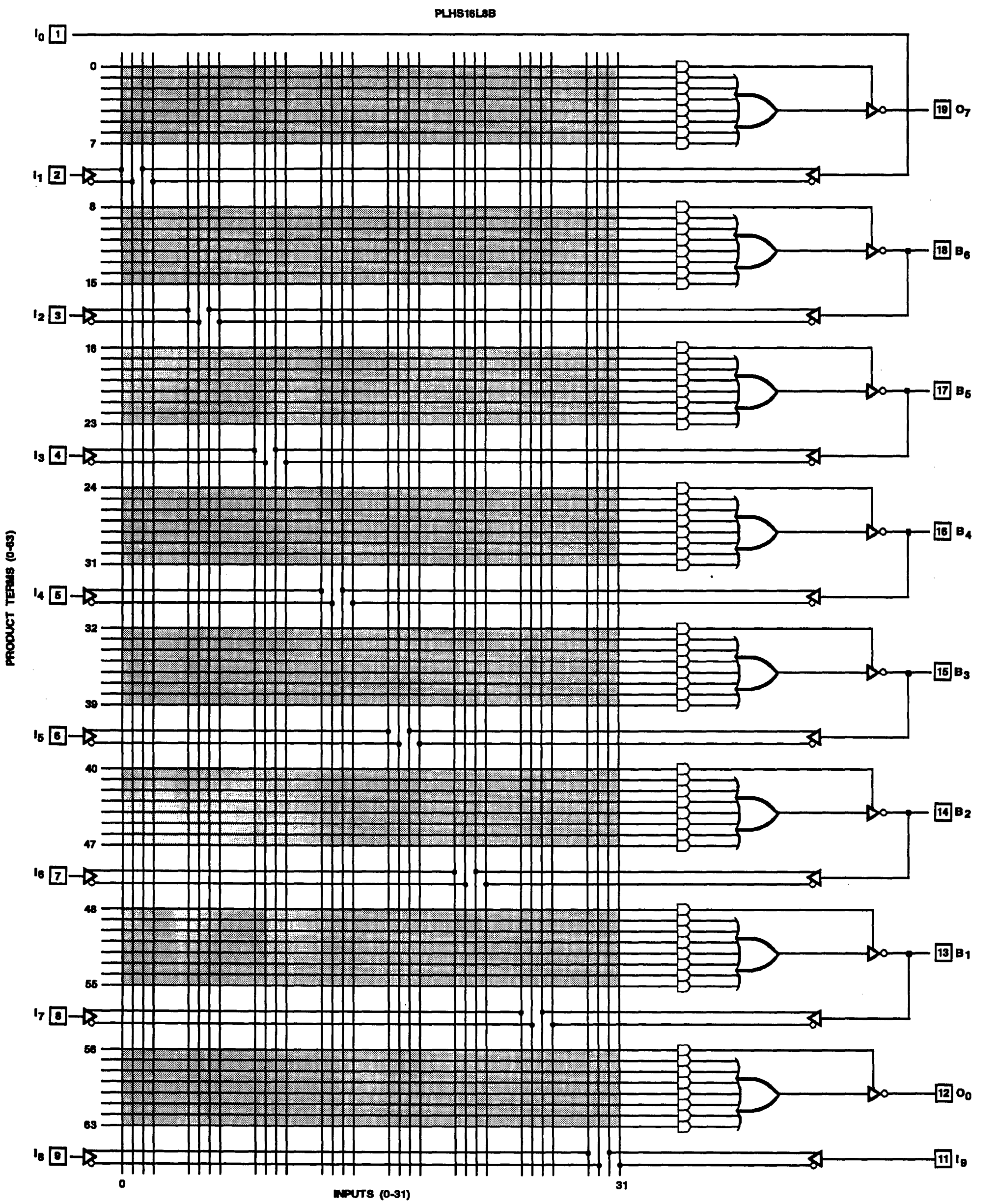
FPLA LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. Programmable connections.

PAL®-Type Device PLHS16L8A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP (300mil-wide)	PLHS16L8AN
20-pin Plastic Leaded Chip Carrier	PLHS16L8AA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V_{DC}
V_{IN}	Input voltage	−0.5 to +5.5	V_{DC}
V_{OUT}	Output voltage	−0.5 to V_{CC} Max	V_{DC}
V_{OUTPRG}	Output voltage (programming)	+21	V_{DC}
I_{IN}	Input current	−30 to +5	mA
I_{OUT}	Output current	+100	mA
I_{OUTPRG}	Output current (programming)	+170	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ 75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			+0.8	V
V_{IH}	High	V_{CC} = Max	+2.0			V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −18mA		−0.9	−1.2	V
Output voltage						
		V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = +24mA			+0.50	V
V_{OH}	High	I_{OH} = −3.2mA	+2.4	+3.5		V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = +0.40V		−20	−100	μA
I_{IH}	High	V_{IN} = +2.7V			+25	μA
I_I	High	V_{IN} = +5.5V			+1.0	mA
Output current						
		V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2.0V				
I_{OZH}	Output leakage	V_{OUT} = +2.7V			+100	μA
I_{OZL}	Output leakage	V_{OUT} = +0.40V			−50	μA
I_{OS}	Short circuit[3]	V_{OUT} = +0.5V	−30	−60	−90	mA
I_{CC}	V_{CC} current	V_{CC} = Max, All inputs = GND		100	155	mA
Capacitance[4]						
		V_{CC} = +5V				
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		6		pF
C_{OUT}	I/O	V_{OUT} = 2.0V @ f = 1MHz		9		pF

NOTES:

[1] Typical limits are at V_{CC} = 5.0V and T_A = +25°C.

[2] These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

[3] Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

[4] These parameters are not 100% tested, but are periodically sampled.

AC ELECTRICAL CHARACTERISTICS $R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Input ±	Output ±	$C_L = 50pF$		14	20	ns
t_{EA}	Output enable	Input ±	Output −	$C_L = 50pF$		14	20	ns
t_{ER}	Output disable	Input ±	Output +	$C_L = 5pF$		14	20	ns

NOTES:

1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.
2. T_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_{OH} = -0.5V$ with S_1 open, and Low-to-High impedance tests are made to the $V_{OL} = +0.5V$ level with S_1 closed.

VIRGIN STATE

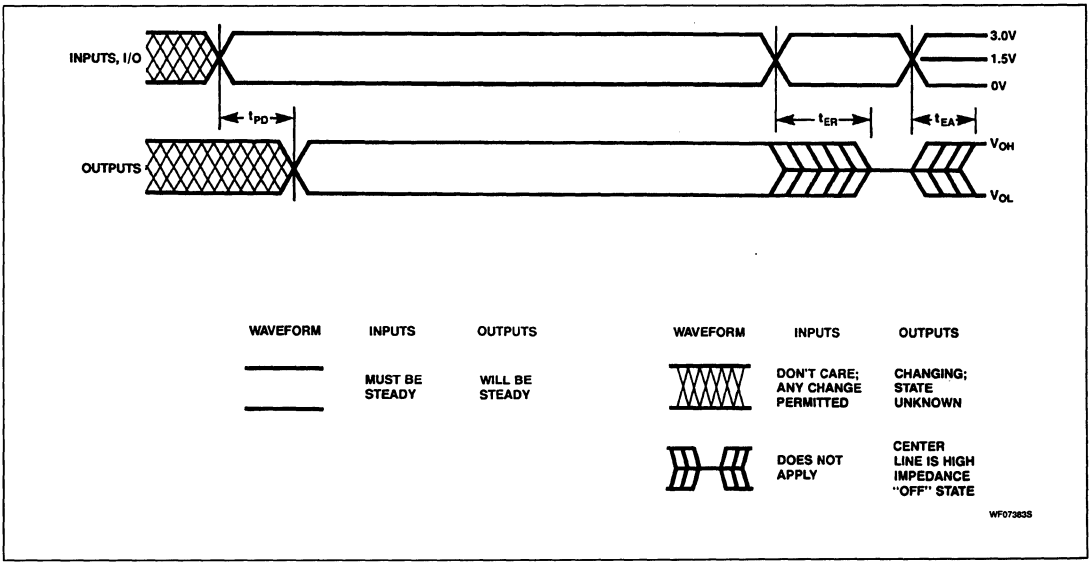
A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are enabled.
2. All p-terms are enabled in the AND array.

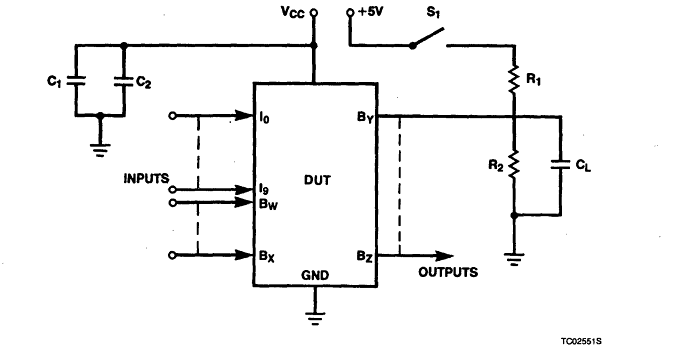
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Input to output progagation delay.
t_{ER}	Input to output disable (3-State) delay (Output Disable).
t_{EA}	Input to Output Enable delay (Output Enable).

TIMING DIAGRAMS

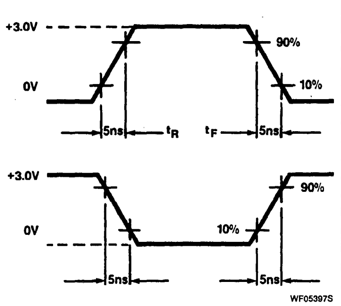


AC TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

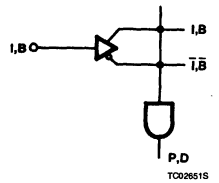
LOGIC PROGRAMMING

PLHS16L8A logic designs can be generated using any commercially available, JEDEC standard design software that supports the 16L8 architecture. No JEDEC fuse map conversion or translation is necessary when using the PLHS16L8A.

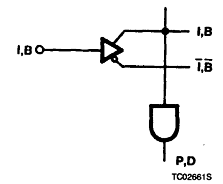
PLHS16L8A designs can also be generated using the program table format, detailed on the following page. This program table entry (PTE) format is supported on the Signetics AMAZE PLD design software. AMAZE is available free of charge to qualified users.

To implement the desired logic functions, each logic variable (I, B, P and D) from the logic equations is assigned a symbol. TRUE (High), COMPLEMENT (Low), DON'T CARE and INACTIVE symbols are defined below.

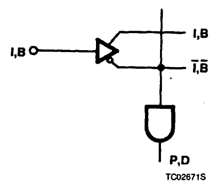
"AND" ARRAY—(I, B)



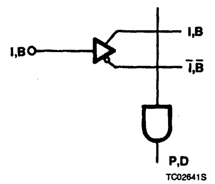
STATE	CODE
INACTIVE[2]	O



STATE	CODE
TRUE	H



STATE	CODE
COMPLEMENT	L



STATE	CODE
DON'T CARE[1]	-

NOTES:

[1] This is the initial state of all diodes pairs.

[2] All unused product terms must be programmed with all pairs of diodes in the INACTIVE state (all fuses on an unused p-term must be programmed).

PAL®-Type Device PLHS16L8A

PROGRAM TABLE

Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All p-terms are active until programmed otherwise.
4. All unused product terms must be programmed with all pairs of fuses in the INACTIVE state (all fuses on an unused p-term must be programmed).
5. Data cannot be entered into the OR array field due to the fixed nature of the device architecture.

OR (FIXED)

DIRECTION	D
ACTIVE OUTPUT	A
NOT USED	▨

AND

INACTIVE	O
I, B	H
Ī, B̄	L
DON'T CARE	—

I,B(I)

CUSTOMER NAME________

PURCHASE ORDER #________

SIGNETICS DEVICE #________ CF (XXXX)________

CUSTOMER SYMBOLIZED PART #________

TOTAL NUMBER OF PARTS________

PROGRAM TABLE #________ REV________ DATE________

TERM	AND																	OR (FIXED)							
	INPUT (I)										INPUTS (B)							OUTPUTS (B, O)							
	9	8	7	6	5	4	3	2	1	0	6	5	4	3	2	1		7	6	5	4	3	2	1	0
0																		D	▨	▨	▨	▨	▨	▨	▨
1																		A	▨	▨	▨	▨	▨	▨	▨
2																		A	▨	▨	▨	▨	▨	▨	▨
3																		A	▨	▨	▨	▨	▨	▨	▨
4																		A	▨	▨	▨	▨	▨	▨	▨
5																		A	▨	▨	▨	▨	▨	▨	▨
6																		A	▨	▨	▨	▨	▨	▨	▨
7																		A	▨	▨	▨	▨	▨	▨	▨
8																		▨	D	▨	▨	▨	▨	▨	▨
9																		▨	A	▨	▨	▨	▨	▨	▨
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11																		▨	A	▨	▨	▨	▨	▨	▨
12																		▨	A	▨	▨	▨	▨	▨	▨
13																		▨	A	▨	▨	▨	▨	▨	▨
14																		▨	A	▨	▨	▨	▨	▨	▨
15																		▨	A	▨	▨	▨	▨	▨	▨
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56																		▨	▨	▨	▨	▨	▨	▨	D
57																		▨	▨	▨	▨	▨	▨	▨	A
58																		▨	▨	▨	▨	▨	▨	▨	A
59																		▨	▨	▨	▨	▨	▨	▨	A
60																		▨	▨	▨	▨	▨	▨	▨	A
61																		▨	▨	▨	▨	▨	▨	▨	A
62																		▨	▨	▨	▨	▨	▨	▨	A
63																		▨	▨	▨	▨	▨	▨	▨	A
PIN	11	9	8	7	6	5	4	3	2	1	18	17	16	15	14	13		19	18	17	16	15	14	13	12
VARIABLE NAME																									

TB02024S

Signetics

PLHS16L8B
PAL®-Type Device

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLHS16L8B is a very high-speed "B" version PAL®-type device. The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 OR gates. The Signetics PLHS16L8B offers 100% functional compatibility with other PAL 16L8 devices. Specified at 155mA I_{CC} (maximum), the PLHS16L8B consumes 20% less power than other "B" version PAL 16L8 devices.

All AND gates are linked to 10 dedicated inputs, 6 bidirectional I/O and 2 dedicated outputs. On-chip buffers couple either true (I, B) or complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates. The 64 AND gates are separated into eight groups of eight product terms each. Within each group, seven of the AND terms are OR'ed together, while the eighth is used to control the 3-State function of the bidirectional I/O. All outputs (bidirectional and dedicated) are inverting.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

The PLHS16L8B is field-programmable, allowing the user to quickly generate custom patterns using standard programming equipment.

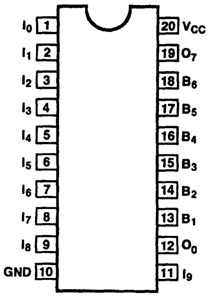
Order codes are listed in the Ordering Information Table.

FEATURES

- **Consumes 20% less power than other "B" version PAL devices**
  - **155mA I_{CC} (worst-case)**
- **I/O propagation delay: 15ns (MAX)**
- **100% functionally and pin-for-pin compatible with AmPAL16L8B, MMI PAL16L8B, TIBPAL16L8-15 and NSC PAL16L8B devices**
- **Field-programmable**
- **10 dedicated inputs**
- **8 outputs**
  - **6 bidirectional I/O**
  - **2 dedicated outputs**
- **Individual 3-State control of all outputs**
- **64 AND gates/product terms**
- **Security Fuse**

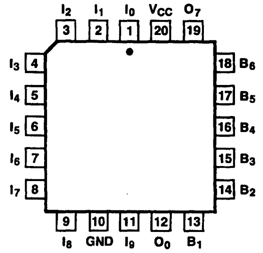
PIN CONFIGURATIONS

N Package



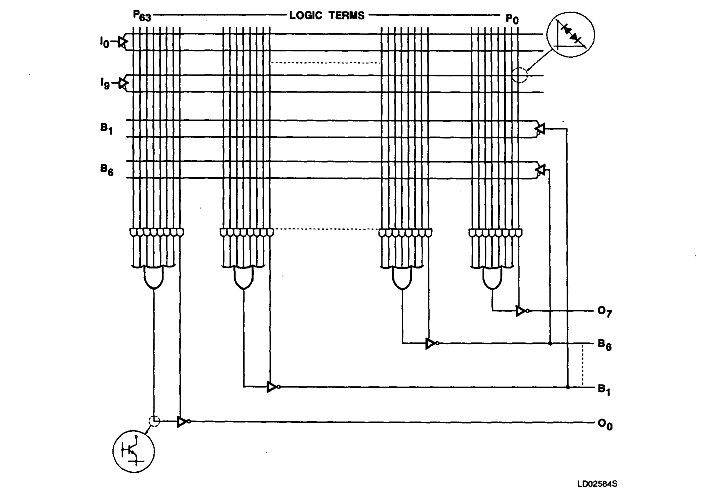
CD05323S

A Package



CD05339S

FUNCTIONAL DIAGRAM



LD02584S

APPLICATIONS

- **100% functional replacement for 20-pin 16L8 combinatorial PAL devices**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping/decoding**
- **Multiplexing**

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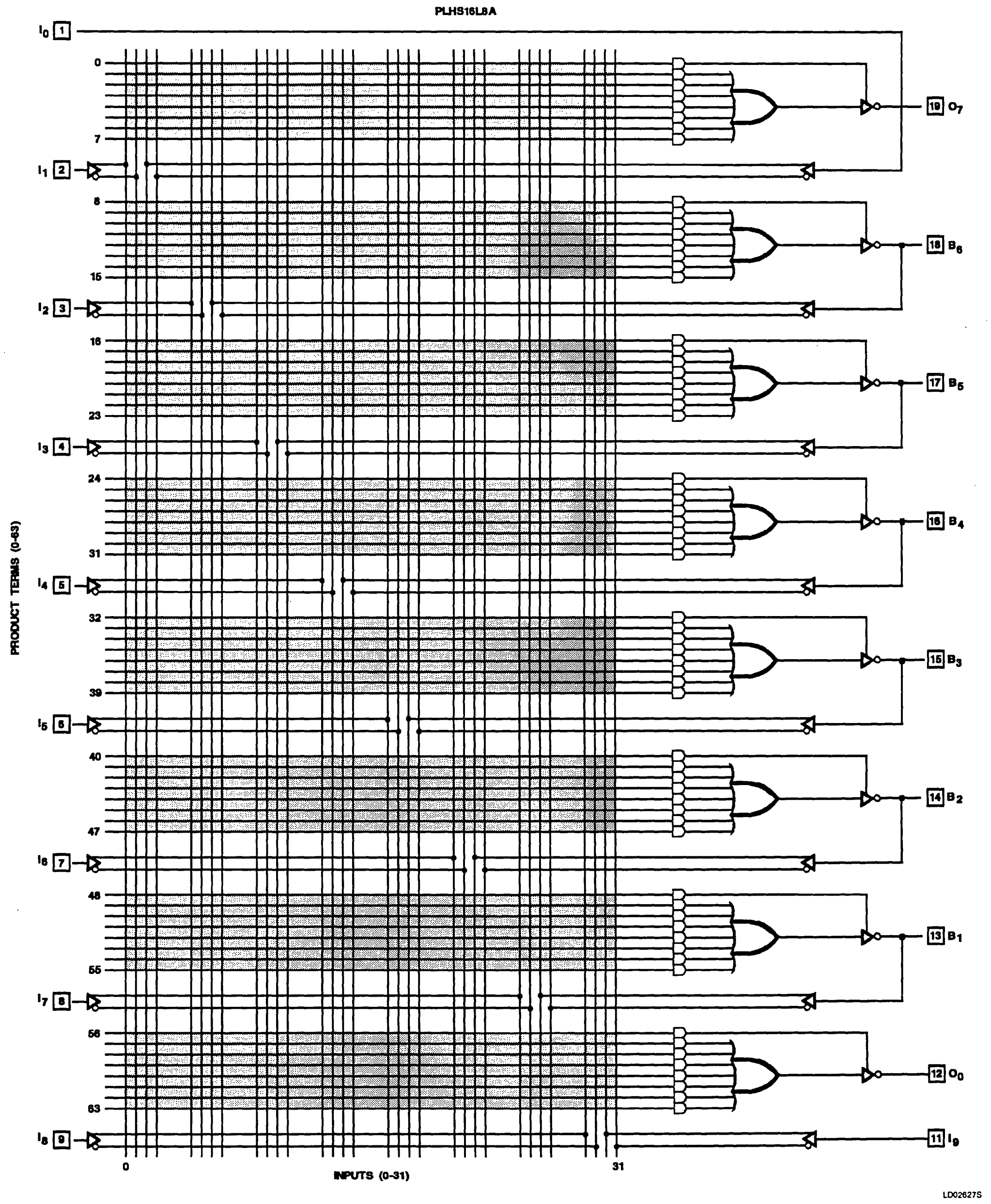
FPLA LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. ▨ Programmable connections.

PAL®-Type Device PLHS16L8B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP (300mil-wide)	PLHS16L8BN
20-pin Plastic Leaded Chip Carrier	PLHS16L8BA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V_{DC}
V_{IN}	Input voltage	-0.5 to +5.5	V_{DC}
V_{OUT}	Output voltage	-0.5 to V_{CC} Max	V_{DC}
V_{OUTPRG}	Output voltage (programming)	+21	V_{DC}
I_{IN}	Input current	-30 to +5	mA
I_{OUT}	Output current	+100	mA
I_{OUTPRG}	Output current (programming)	+170	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. **Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.**

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			+0.8	V
V_{IH}	High	V_{CC} = Max	+2.0			V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −18mA		-0.9	-1.2	V
Output voltage						
		V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = +24mA			+0.50	V
V_{OH}	High	I_{OH} = −3.2mA	+2.4	+3.5		V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = +0.40V		-20	-100	µA
I_{IH}	High	V_{IN} = +2.7V			+25	µA
I_I	High	V_{IN} = +5.5V			+1.0	mA
Output current						
		V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2.0V				
I_{OZH}	Output leakage	V_{OUT} = +2.7V			+100	µA
I_{OZL}	Output leakage	V_{OUT} = +0.40V			-50	µA
I_{OS}	Short circuit[3]	V_{OUT} = +0.5V	-30	-60	-90	mA
I_{CC}	V_{CC} current	V_{CC} = Max, All inputs = GND		100	155	mA
Capacitance[4]						
		V_{CC} = +5V				
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		6		pF
C_{OUT}	I/O	V_{OUT} = 2.0V @ f = 1MHz		9		pF

NOTES:

1. Typical limits are at V_{CC} = 5.0V and T_A = + 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.

AC ELECTRICAL CHARACTERISTICS $R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Input ±	Output ±	$C_L = 50pF$		12	15	ns
t_{EA}	Output enable	Input ±	Output –	$C_L = 50pF$		12	15	ns
t_{ER}	Output disable	Input ±	Output +	$C_L = 5pF$		12	15	ns

NOTES:

1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.
2. T_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_{OH} = -0.5V$ with S_1 open, and Low-to-High impedance tests are made to the $V_{OL} = +0.5V$ level with S_1 closed.

VIRGIN STATE

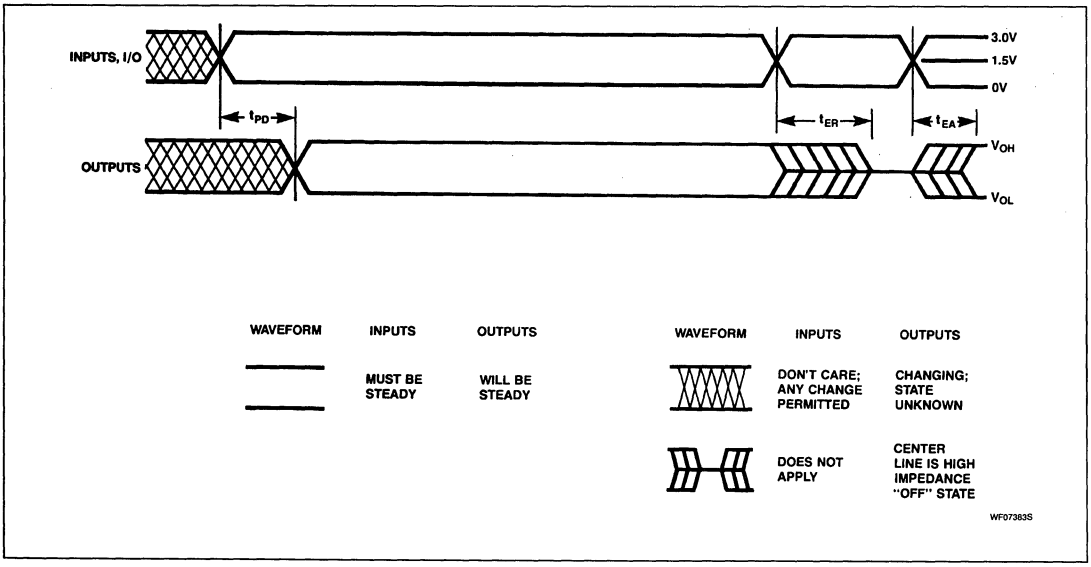
A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are enabled.
2. All p-terms are enabled in the AND array.

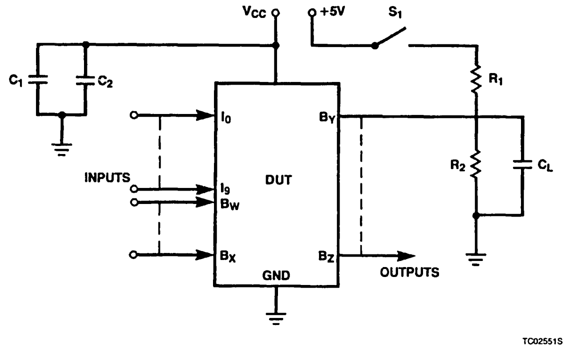
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Input to output progagation delay.
t_{ER}	Input to output disable (3-State) delay (Output Disable).
t_{EA}	Input to Output Enable delay (Output Enable).

TIMING DIAGRAMS

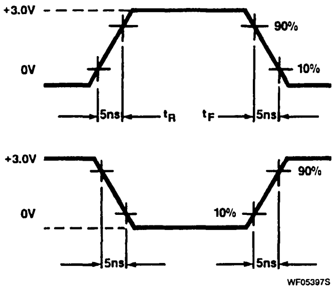


AC TEST LOAD CIRCUIT



NOTE:
C1 and C2 are to bypass VCC to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

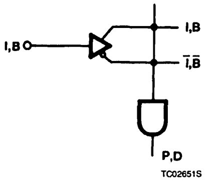
LOGIC PROGRAMMING

PLHS16L8B logic designs can be generated using any commercially available, JEDEC standard design software that supports the 16L8 architecture. No JEDEC fuse map conversion or translation is necessary when using the PLHS16L8B.

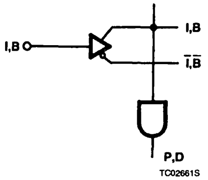
PLHS16L8B designs can also be generated using the program table format, detailed on the following page. This program table entry (PTE) format is supported on the Signetics AMAZE PLD design software. AMAZE is available free of charge to qualified users.

To implement the desired logic functions, each logic variable (I, B, P and D) from the logic equations is assigned a symbol. TRUE (High), COMPLEMENT (Low), DON'T CARE and INACTIVE symbols are defined below.

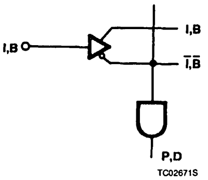
"AND" ARRAY—(I, B)



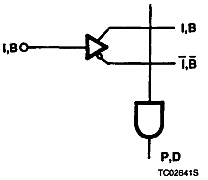
STATE	CODE
INACTIVE[2]	O



STATE	CODE
TRUE	H



STATE	CODE
COMPLEMENT	L



STATE	CODE
DON'T CARE[1]	-

NOTES:
1. This is the initial state of all diodes pairs.
2. All unused product terms must be programmed with all pairs of diodes in the INACTIVE state (all fuses on an unused p-term must be programmed).

PAL®-Type Device PLHS16L8B

PROGRAM TABLE

Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All p-terms are active until programmed otherwise.
4. All unused product terms must be programmed with all pairs of fuses in the INACTIVE state (all fuses on an unused p-term must be programmed).
5. Data cannot be entered into the OR array field due to the fixed nature of the device architecture.

OR (FIXED)

DIRECTION	D
ACTIVE OUTPUT	A
NOT USED	/

AND

INACTIVE	O
I, B	H
Ī, B̄	L
DON'T CARE	—

I,B(I)

CUSTOMER NAME______

PURCHASE ORDER #______

SIGNETICS DEVICE #______ CF (XXXX)______

CUSTOMER SYMBOLIZED PART #______

TOTAL NUMBER OF PARTS______

PROGRAM TABLE #______ REV______ DATE______

TERM	AND																	OR (FIXED)							
	INPUT (I)										INPUTS (B)							OUTPUTS (B, O)							
	9	8	7	6	5	4	3	2	1	0	6	5	4	3	2	1		7	6	5	4	3	2	1	0
0																		D	/	/	/	/	/	/	/
1																		A	/	/	/	/	/	/	/
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49																		/	/	/	/	/	/	A	/
50																		/	/	/	/	/	/	A	/
51																		/	/	/	/	/	/	A	/
52																		/	/	/	/	/	/	A	/
53																		/	/	/	/	/	/	A	/
54																		/	/	/	/	/	/	A	/
55																		/	/	/	/	/	/	A	/
56																		/	/	/	/	/	/	/	D
57																		/	/	/	/	/	/	/	A
58																		/	/	/	/	/	/	/	A
59																		/	/	/	/	/	/	/	A
60																		/	/	/	/	/	/	/	A
61																		/	/	/	/	/	/	/	A
62																		/	/	/	/	/	/	/	A
63																		/	/	/	/	/	/	/	A
PIN	11	9	8	7	6	5	4	3	2	1	18	17	16	15	14	13		19	18	17	16	15	14	13	12
VARIABLE NAME																									

TB02024S

Signetics

PLUS16R8D Series
PAL®-Type Devices

Signetics Programmable Logic
Preliminary Specification

Application Specific Products
- **Series 20**

FEATURES

- **Ultra high-speed:**
  - **t_{PD} = 10ns**
  - **f_{MAX} = 55.5MHz (with feedback)**
  - **t_{IS} = 10ns (worst case)**
  - **t_{CKO} = 8ns (worst case)**
- **100% functionally and pin-for-pin compatible with industry standard 20-pin PAL ICs**
- **Power-up reset function to enhance state machine design and testability**
- **Design support provided via AMAZE and other CAD tools for Series 20 PAL devices**
- **Field-programmable on industry standard programmers**
- **Security fuse**
- **Individual 3-State control of all outputs**

DESCRIPTION

The Signetics PLUS16XXD family is an ultra high-speed 10ns version of existing Series 20 PAL devices.

The PLUS16XXD family is 100% functional and pin-compatible with the 16L8, 16R8, 16R6, and 16R4 Series devices.

The sum of products (AND/OR) architecture is comprised of 64 AND gates and 8 OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided.

The PLUS16R8D, R6D, and R4D have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

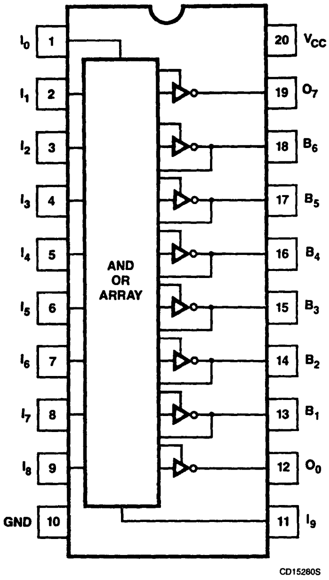
In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

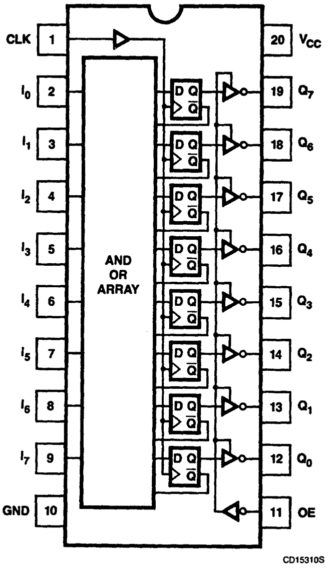
The PLUS16XXD family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS	t_{PD}	I_{CC}	f_{MAX} WITHOUT FEEDBACK	f_{MAX} WITH FEEDBACK
PLUS16L8D	10	8(6 I/O)	0	10ns	180mA		
PLUS16R8D	8	0	8		180mA	62.5MHz	55.5MHz
PLUS16R6D	8	2 I/O	6	10ns	180mA	62.5MHz	55.5MHz
PLUS16R4D	8	4 I/O	4	10ns	180mA	62.5MHz	55.5MHz

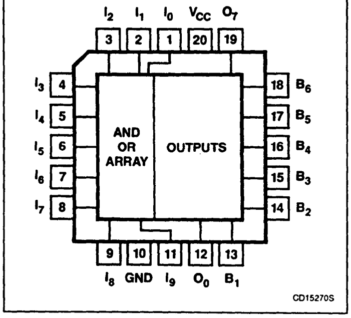
PLUS16L8D



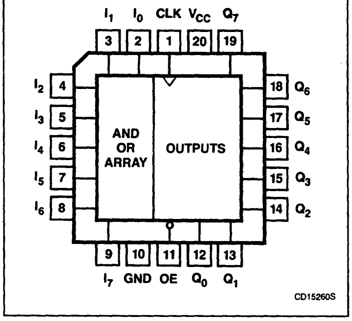
PLUS16R8D



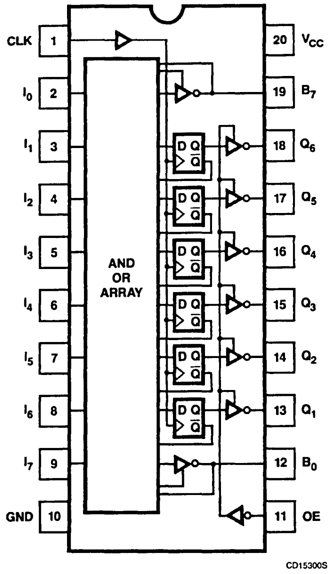
PLUS16L8D



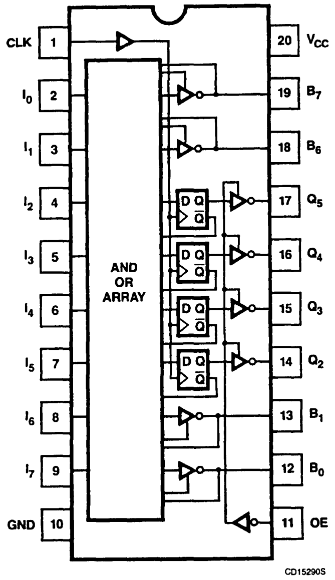
PLUS16R8D



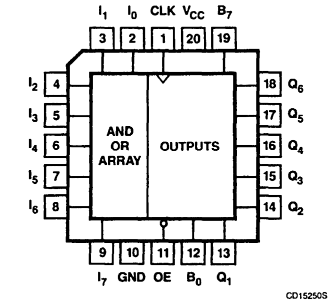
PLUS16R6D



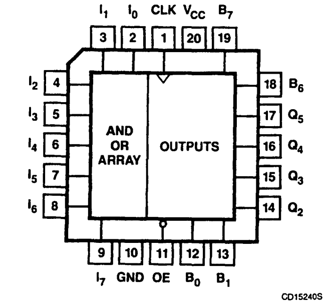
PLUS16R4D



PLUS16R6D



PLUS16R4D



Signetics

PLHS18P8A
PAL®-Type Device

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLHS18P8A is a two-level logic element consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 direction control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an Ex-OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

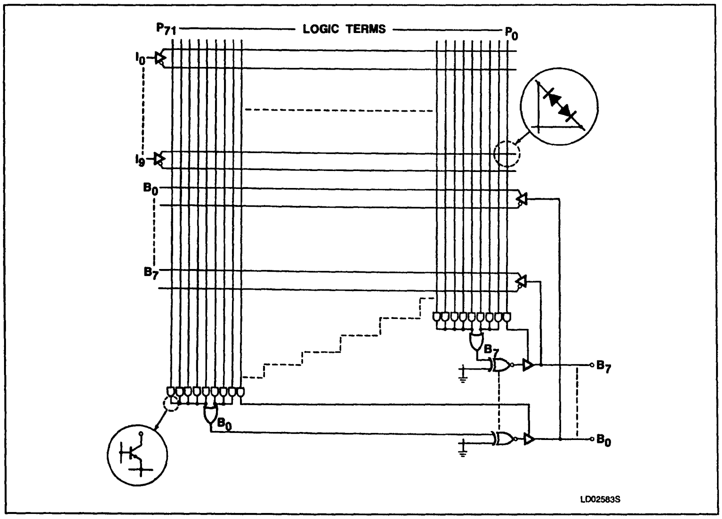
The PLHS18P8A is field-programmable, allowing the user to quickly generate custom pattern using standard programming equipment.

Order codes are listed in the Ordering Information Table.

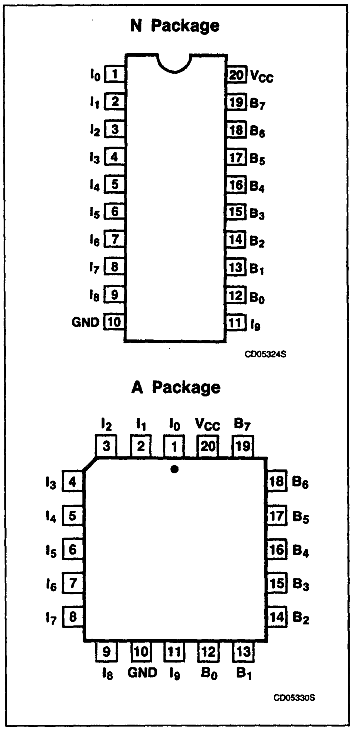
FEATURES

- **100% functionally compatible with AmPAL18P8A and all 16L8, 16P8, 16H8, 16L2, 16H2, 14L4, 14H4, 12L6, 12H6, 10L8, 10H8, 16LD8 and 16HD8 PAL type products**
- **Field-Programmable**
- **10 inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms**
  - **configured into eight groups of nine**
- **Programmable output polarity (3-State output)**
- **I/O propagation delay: 20ns (max)**
- **Power dissipation: 500mW (typ)**
- **TTL compatible**
- **Security Fuse**

FUNCTIONAL DIAGRAM



PIN CONFIGURATIONS


N Package

A Package

APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PAL devices**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

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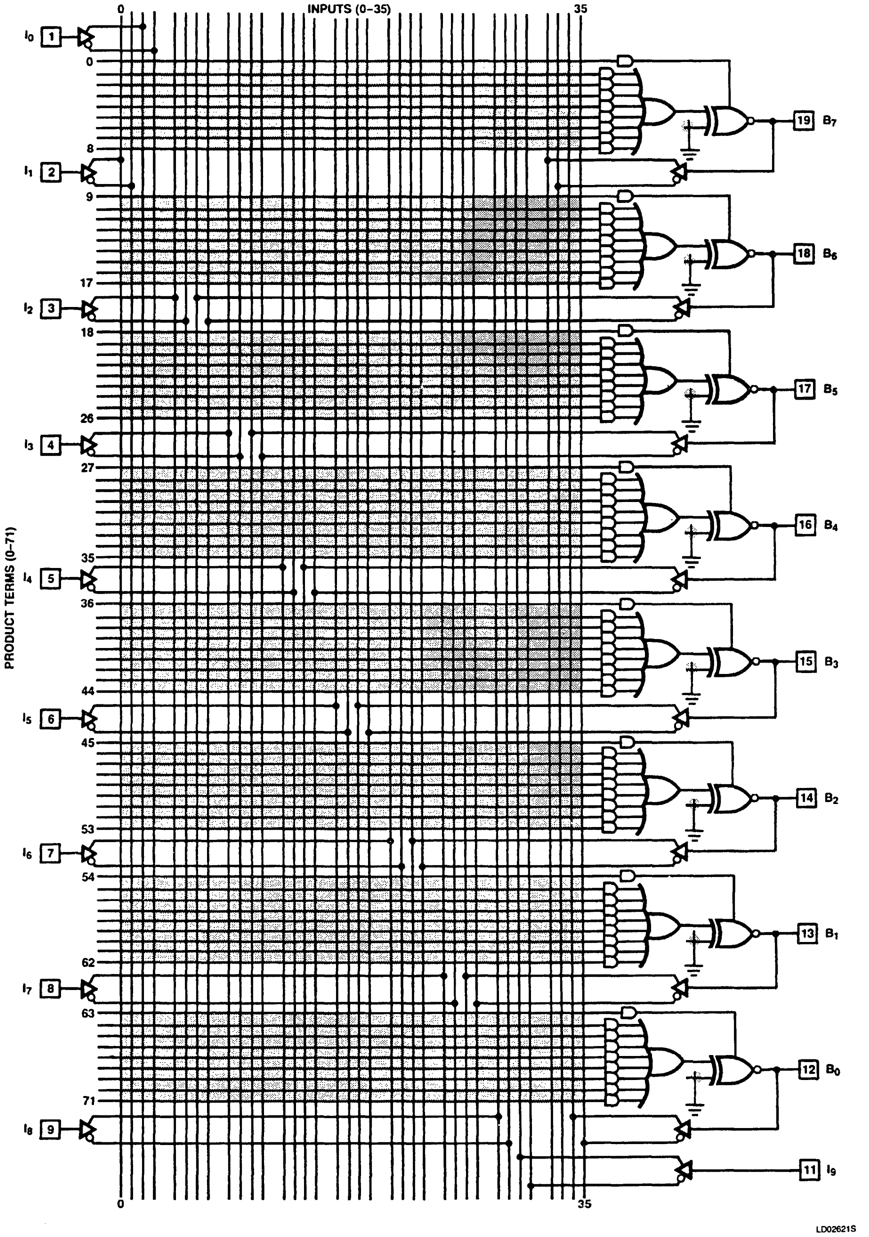
FPLA LOGIC DIAGRAM



NOTES:

1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. ▨ Programmable connections.

PAL®-Type Device PLHS18P8A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP (300mil-wide)	PLHS18P8AN
20-pin Plastic Leaded Chip Carrier	PLHS18P8AA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V_{DC}
V_{IN}	Input voltage	-0.5 to +5.5	V_{DC}
V_{OUT}	Output voltage	-0.5 to V_{CC} Max	V_{DC}
V_{OUTPRG}	Output voltage (programming)	+21	V_{DC}
I_{IN}	Input current	-30 to +5	mA
I_{OUT}	Output current	+100	mA
I_{OUTPRG}	Output current (programming)	+170	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			+0.8	V
V_{IH}	High	V_{CC} = Max	+2.0			V
V_I	Clamp	V_{CC} = Min, I_{IN} = –18mA		–0.9	–1.2	V
Output voltage						
		V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = +24mA			+0.50	V
V_{OH}	High	I_{OH} = –3.2	+2.4	+3.5		V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = +0.40V		-20	-100	μA
I_{IH}	High	V_{IN} = +2.7V			+25	μA
I_I	High	V_{IN} = +5.5V			+1.0	mA
Output current						
		V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2.0V				
I_{OZH}	Output leakage	V_{OUT} = +2.7V			+100	μA
I_{OZL}	Output leakage	V_{OUT} = +0.40V			-250	μA
I_{SC}	Short circuit[3]	V_{OUT} = +0.5V	-25	-60	-90	mA
I_{CC}	V_{CC} current	V_{CC} = Max, All inputs = GND		100	155	mA
Capacitance[4]						
		V_{CC} = +5V				
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		6		pF
C_{OUT}	I/O	V_{OUT} = 2.0V @ f = 1MHz		9		pF

NOTES:

[1] Typical limits are at V_{CC} = 5.0V and T_A = +25°C.

[2] These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

[3] Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

[4] These parameters are not 100% tested, but are periodically sampled.

AC ELECTRICAL CHARACTERISTICS $R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Input ±	Output ±	$C_L = 50pF$		14	20	ns
t_{EA}	Output enable	Input ±	Output −	$C_L = 50pF$		14	20	ns
t_{ER}	Output disable	Input ±	Output +	$C_L = 5pF$		14	20	ns

NOTES:

1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.
2. T_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_{OH} = -0.5V$ with S_1 open, and Low-to-High impedance tests are made to the $V_{OL} = +0.5V$ level with S_1 closed.

VIRGIN STATE

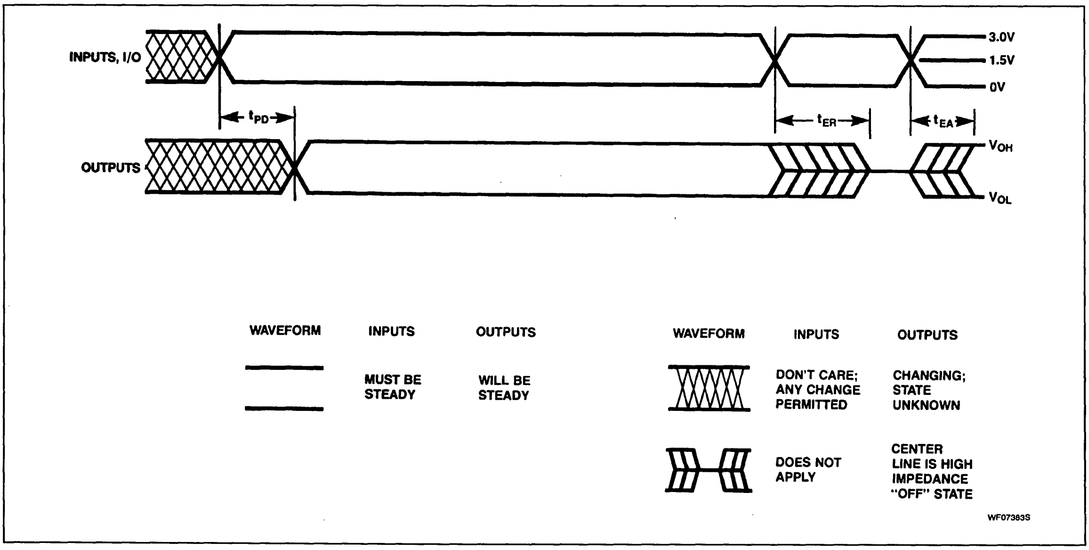
A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are at "H" polarity.
2. All outputs are enabled.
3. All p-terms are enabled.

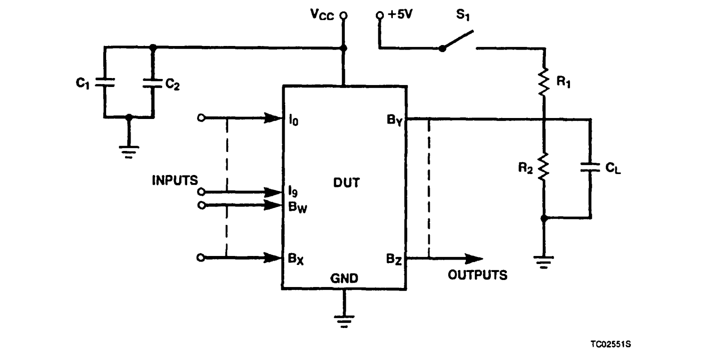
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Input to output progagation delay.
t_{ER}	Input to output disable (3-State) delay (Output Disable).
t_{EA}	Input to Output Enable delay (Output Enable).

TIMING DIAGRAMS

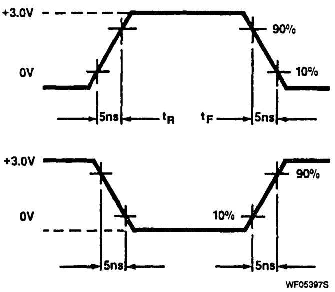


AC TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

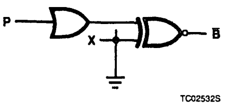
LOGIC PROGRAMMING

PLHS18P8A logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

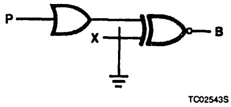
PLHS18P8A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY — (B)

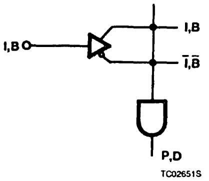


ACTIVE LEVEL	CODE
LOW	L

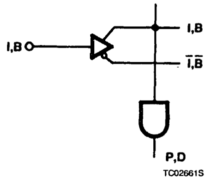


ACTIVE LEVEL	CODE
HIGH[1]	H

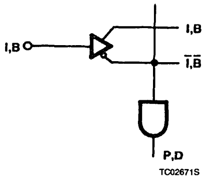
"AND" ARRAY — (I, B)



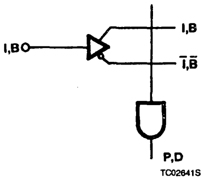
STATE	CODE
INACTIVE[2]	O



STATE	CODE
I, B	H



STATE	CODE
$\overline{I}$, $\overline{B}$	L



STATE	CODE
DON'T CARE[1]	-

NOTES:
1. This is the initial state of all link pairs.
2. All unused product terms must be programmed with all pairs of fuses in the INACTIVE state (all fuses on an unused p-term must be programmed).

PAL®-Type Device | PLHS18P8A

PROGRAM TABLE

Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All p-terms are active until programmed otherwise.
4. All unused product terms must be programmed with all pairs of fuses in the INACTIVE state (all fuses on an unused p-term must be programmed).
5. Data cannot be entered into the OR array field due to the fixed nature of the device architecture.

CONTROL

HIGH	H	(POL)
LOW	L	

OR (FIXED)

DIRECTION	D
ACTIVE OUTPUT	A
NOT USED	—

AND

INACTIVE	O	I,B(I)
I, B	H	
Ī, B̄	L	
DON'T CARE	—	

CUSTOMER NAME ____________________

PURCHASE ORDER # ____________________

SIGNETICS DEVICE # ____________________ CF (XXXX) ____________________

CUSTOMER SYMBOLIZED PART # ____________________

TOTAL NUMBER OF PARTS ____________________

PROGRAM TABLE # ____________ REV ____________ DATE ____________

																			POLARITY							
TERM	AND																		OR (FIXED)							
	I										B (I)								B (O)							
	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																			D							
1																			A							
2																			A							
3																			A							
4																			A							
5																			A							
6																			A							
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65																										A
66																										A
67																										A
68																										A
69																										A
70																										A
71																										A
PIN	11	9	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	19	18	17	16	15	14	13	12
VARIABLE NAME																										

TB02023S

Signetics

PLHS18P8B
PAL®-Type Device

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLHS18P8B is a two-level logic element consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 direction control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an Ex-OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

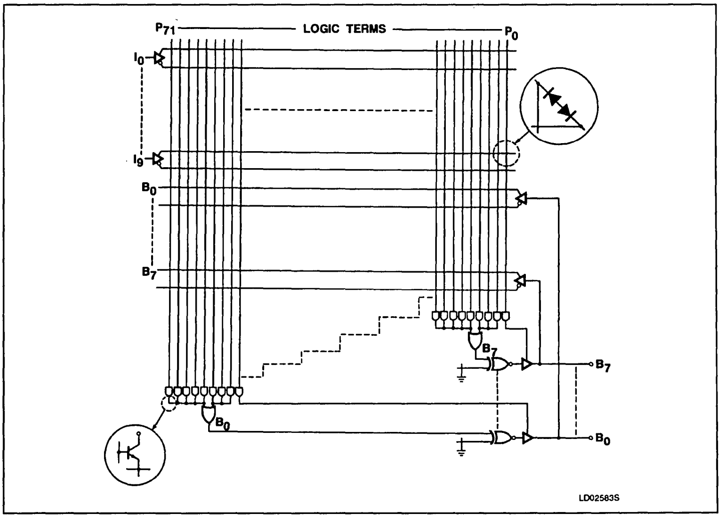
The PLHS18P8B is field-programmable, allowing the user to quickly generate custom pattern using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

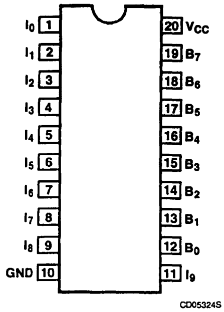
- **100% functionally compatible with AmPAL18P8B and all 16L8, 16P8, 16H8, 16L2, 16H2, 14L4, 14H4, 12L6, 12H6, 10L8, 10H8, 16LD8 and 16HD8 PAL type products**
- **Field-Programmable**
- **10 inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms**
  - **configured into eight groups of nine**
- **Programmable output polarity (3-State output)**
- **I/O propagation delay: 15ns (max)**
- **Power dissipation: 500mW (typ)**
- **TTL compatible**
- **Security Fuse**

FUNCTIONAL DIAGRAM

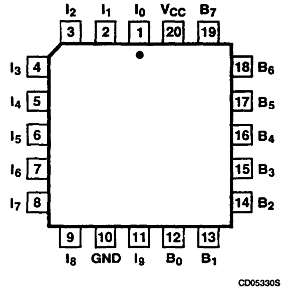


PIN CONFIGURATIONS

N Package



A Package



APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PAL devices**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

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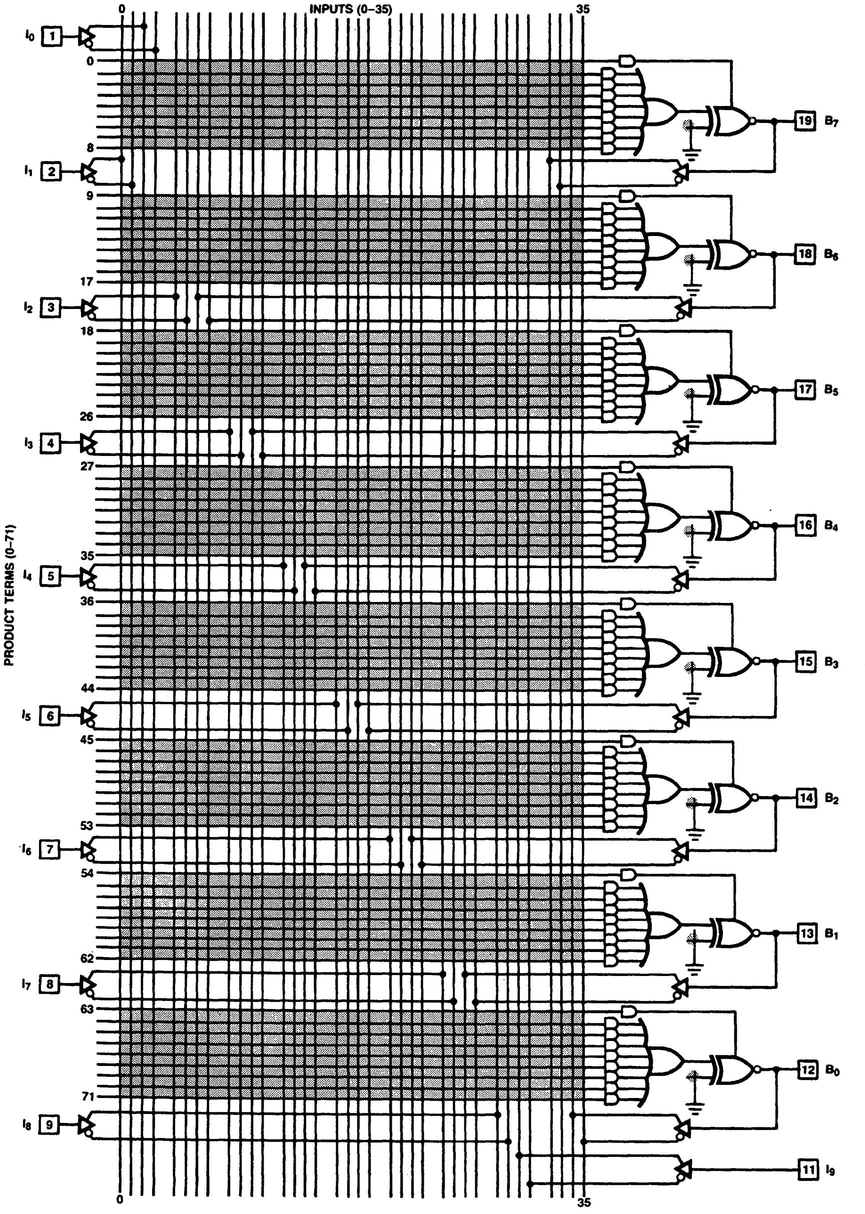
FPLA LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. Programmable connections.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP (300mil-wide)	PLHS18P8BN
20-pin Plastic Leaded Chip Carrier	PLHS18P8BA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]*

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V_{DC}
V_{IN}	Input voltage	-0.5 to +5.5	V_{DC}
V_{OUT}	Output voltage	-0.5 to V_{CC} Max	V_{DC}
V_{OUTPRG}	Output voltage (programming)	+21	V_{DC}
I_{IN}	Input current	-30 to +5	mA
I_{OUT}	Output current	+100	mA
I_{OUTPRG}	Output current (programming)	+170	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS 0°C ⩽ T_A ⩽ 75°C, 4.75V ⩽ V_{CC} ⩽ 5.25V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			+0.8	V
V_{IH}	High	V_{CC} = Max	+2.0			V
V_I	Clamp	V_{CC} = Min, I_{IN} = –18mA		-0.9	-1.2	V
Output voltage						
		V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = +24mA			+0.50	V
V_{OH}	High	I_{OH} = –3.2	+2.4	+3.5		V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = +0.40V		-20	-100	μA
I_{IH}	High	V_{IN} = +2.7V			+25	μA
I_I	High	V_{IN} = +5.5V			+1.0	mA
Output current						
		V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2.0V				
I_{OZH}	Output leakage	V_{OUT} = +2.7V			+100	μA
I_{OZL}	Output leakage	V_{OUT} = +0.40V			-250	μA
I_{SC}	Short circuit[3]	V_{OUT} = +0.5V	-30	-60	-90	mA
I_{CC}	V_{CC} current	V_{CC} = Max, All inputs = GND		100	155	mA
Capacitance[4]						
		V_{CC} = +5V				
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		6		pF
C_{OUT}	I/O	V_{OUT} = 2.0V @ f = 1MHz		9		pF

NOTES:

1. Typical limits are at V_{CC} = 5.0V and T_A = + 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.

AC ELECTRICAL CHARACTERISTICS $R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Input ±	Output ±	$C_L = 50pF$		12	15	ns
t_{EA}	Output enable	Input ±	Output –	$C_L = 50pF$		12	15	ns
t_{ER}	Output disable	Input ±	Output +	$C_L = 5pF$		12	15	ns

NOTES:

1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.
2. T_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_{OH} = -0.5V$ with S_1 open, and Low-to-High impedance tests are made to the $V_{OL} = +0.5V$ level with S_1 closed.

VIRGIN STATE

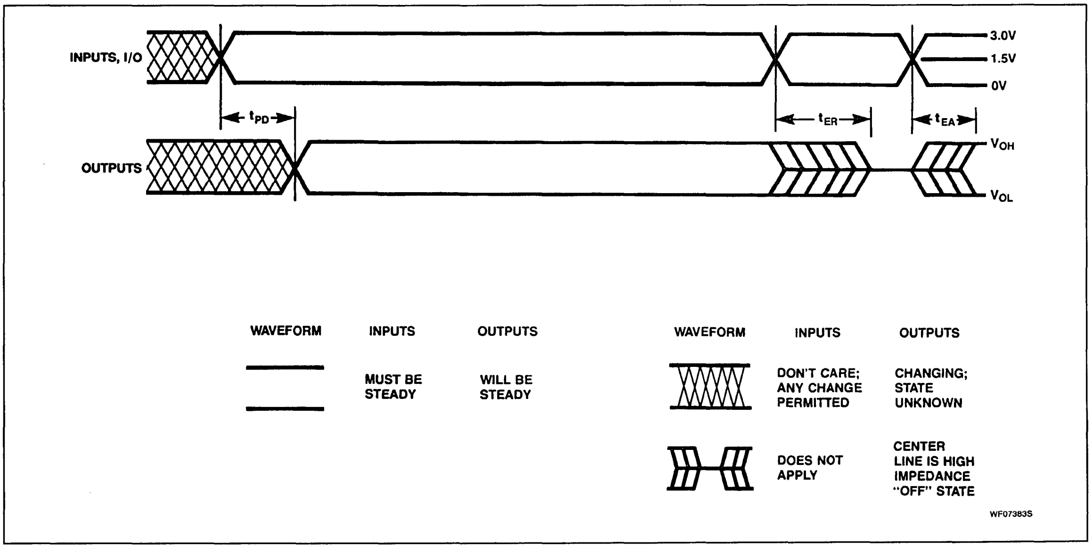
A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are at "H" polarity.
2. All outputs are enabled.
3. All p-terms are enabled.

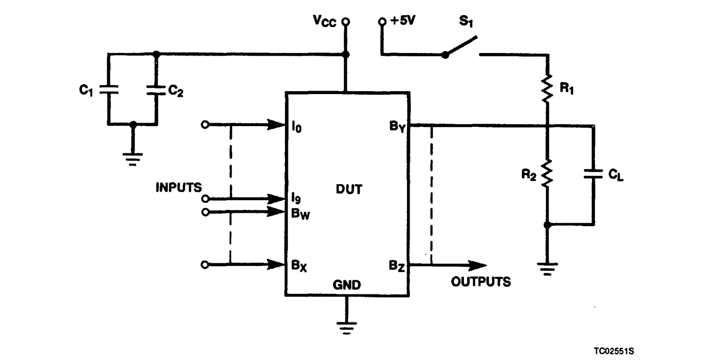
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Input to output progagation delay.
t_{ER}	Input to output disable (3-State) delay (Output Disable).
t_{EA}	Input to Output Enable delay (Output Enable).

TIMING DIAGRAMS

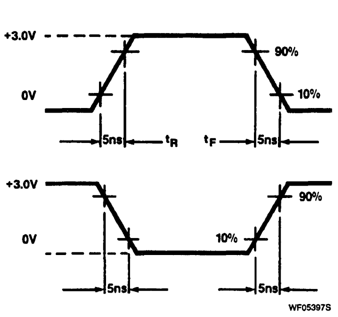


AC TEST LOAD CIRCUIT



NOTE:
C1 and C2 are to bypass VCC to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

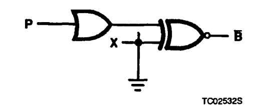
LOGIC PROGRAMMING

PLHS18P8B logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

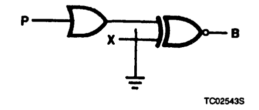
PLHS18P8B logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY — (B)

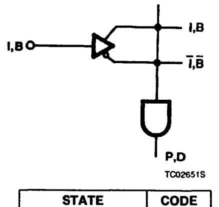


ACTIVE LEVEL	CODE
LOW	L

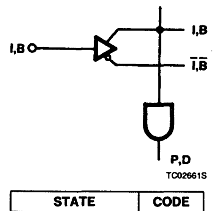


ACTIVE LEVEL	CODE
HIGH[1]	H

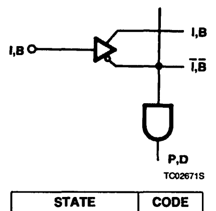
"AND" ARRAY — (I, B)



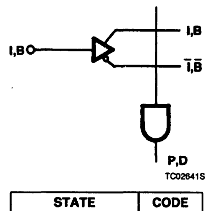
STATE	CODE
INACTIVE[2]	O



STATE	CODE
I, B	H



STATE	CODE
Ī, B̄	L



STATE	CODE
DON'T CARE[1]	-

NOTES:
1. This is the initial state of all link pairs.
2. All unused product terms must be programmed with all pairs of fuses in the INACTIVE state (all fuses on an unused p-term must be programmed).

PAL®-Type Device PLHS18P8B

PROGRAM TABLE

Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All p-terms are active until programmed otherwise.
4. All unused product terms must be programmed with all pairs of fuses in the INACTIVE state (all fuses on an unused p-term must be programmed).
5. Data cannot be entered into the OR array field due to the fixed nature of the device architecture.

CONTROL

HIGH	H	(POL)
LOW	L	

OR (FIXED)

DIRECTION	D
ACTIVE OUTPUT	A
NOT USED	

AND

INACTIVE	O	I,B(I)
I, B	H	
Ī, B̄	L	
DON'T CARE	—	

CUSTOMER NAME____________

PURCHASE ORDER #____________

SIGNETICS DEVICE #____________ CF (XXXX)____________

CUSTOMER SYMBOLIZED PART #____________

TOTAL NUMBER OF PARTS____________

PROGRAM TABLE #____________ REV________ DATE________

																			POLARITY							
TERM	AND																		OR (FIXED)							
	I										B (I)								B (O)							
	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																			D							
1																			A							
2																			A							
3																			A							
4																			A							
5																			A							
6																			A							
7																			A							
8																			A							
9																				D						
10																				A						
11																				A						
12																				A						
13																				A						
14																				A						
15																				A						
16																				A						
17																				A						
18																					D					
19																					A					
20																					A					
21																					A					
22																					A					
23																					A					
24																					A					
25																					A					
26																					A					
27																						D				
28																						A				
29																						A				
30																						A				
31																						A				
32																						A				
33																						A				
34																						A				
35																						A				
36																							D			
37																							A			
38																							A			
39																							A			
40																							A			
41																							A			
42																							A			
43																							A			
44																							A			
45																								D		
46																								A		
47																								A		
48																								A		
49																								A		
50																								A		
51																								A		
52																								A		
53																								A		
54																									D	
55																									A	
56																									A	
57																									A	
58																									A	
59																									A	
60																									A	
61																									A	
62																									A	
63																										D
64																										A
65																										A
66																										A
67																										A
68																										A
69																										A
70																										A
71																										A
PIN	11	9	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	19	18	17	16	15	14	13	12
VARIABLE NAME																										

TB02023S

Signetics

PLC20V8 Series
Erasable and OTP PAL®-Type Device

Signetics Programmable Logic
Product Specification

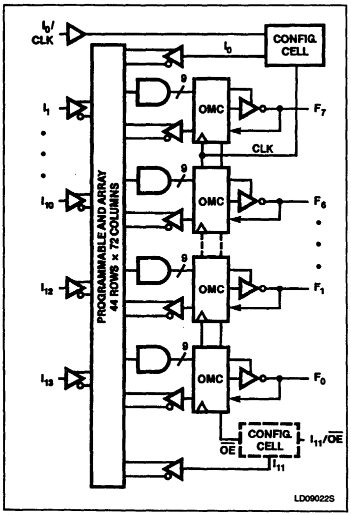
Application Specific Products
- **Series 24**

DESCRIPTION

The PLC20V8 Programmable Array Logic device is a 24-pin CMOS PLD designed to replace full-power as well as quarter-power and half-power Series 24 PAL® devices. Available in four speed/power configurations, the generic PLC20V8 device can be configured to emulate 21 different PAL devices in multiple speed/power configurations. The more complex AND-OR logic functions can be easily implemented with the PLC20V8 because of the flexibility inherent to its generic Output Macro Cell architecture.

The PLC20V8 is a two-level logic element comprised of 14 inputs, 72 AND gates and 8 Output Macro Cells (OMC). Each Output Macro Cell can be individually configured as a dedicated input, a dedicated output, a bidirectional I/O or as a registered output with feedback. This generic architecture provides a means of reducing documentation, inventory and manufacturing related costs. Furthermore, the PLC20V8 series devices are designed to accept both TTL and CMOS input levels to facilitate logic integration in almost any system environment.

FUNCTIONAL DIAGRAM



FEATURES

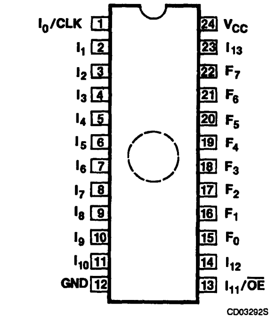
- **100% functional replacement for Series 24 PAL devices**
  $-I_{OL} = 24mA$
- **Low power performance: 50 and 90mA max**
  - **All inputs and outputs switching at 15MHz**
- **Equivalent bipolar performance**
  - **35 and 45ns t_{PD}**
  - **28.5 and 22.2MHz f_{MAX} (async)**
- **EPROM cell technology**
  - **Erasable**
  - **100% testable**
  - **Reconfigurable (quartz window package only)**
- **TTL and CMOS compatible**
- **Security fuse**
- **Available in 300mil-wide DIP with quartz window, plastic DIP (OTP), or PLCC (OTP)**

PIN LABEL DESCRIPTIONS

I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)

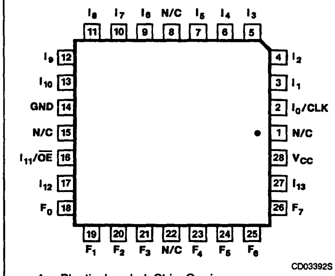
PIN CONFIGURATIONS

N Package



N = Plastic
FA = Ceramic with Quartz Window

A Package



A = Plastic Leaded Chip Carrier

PAL DEVICE TO PLC20V8 OUTPUT PIN CONFIGURATION CROSS REFERENCE (DIP Packages Only)

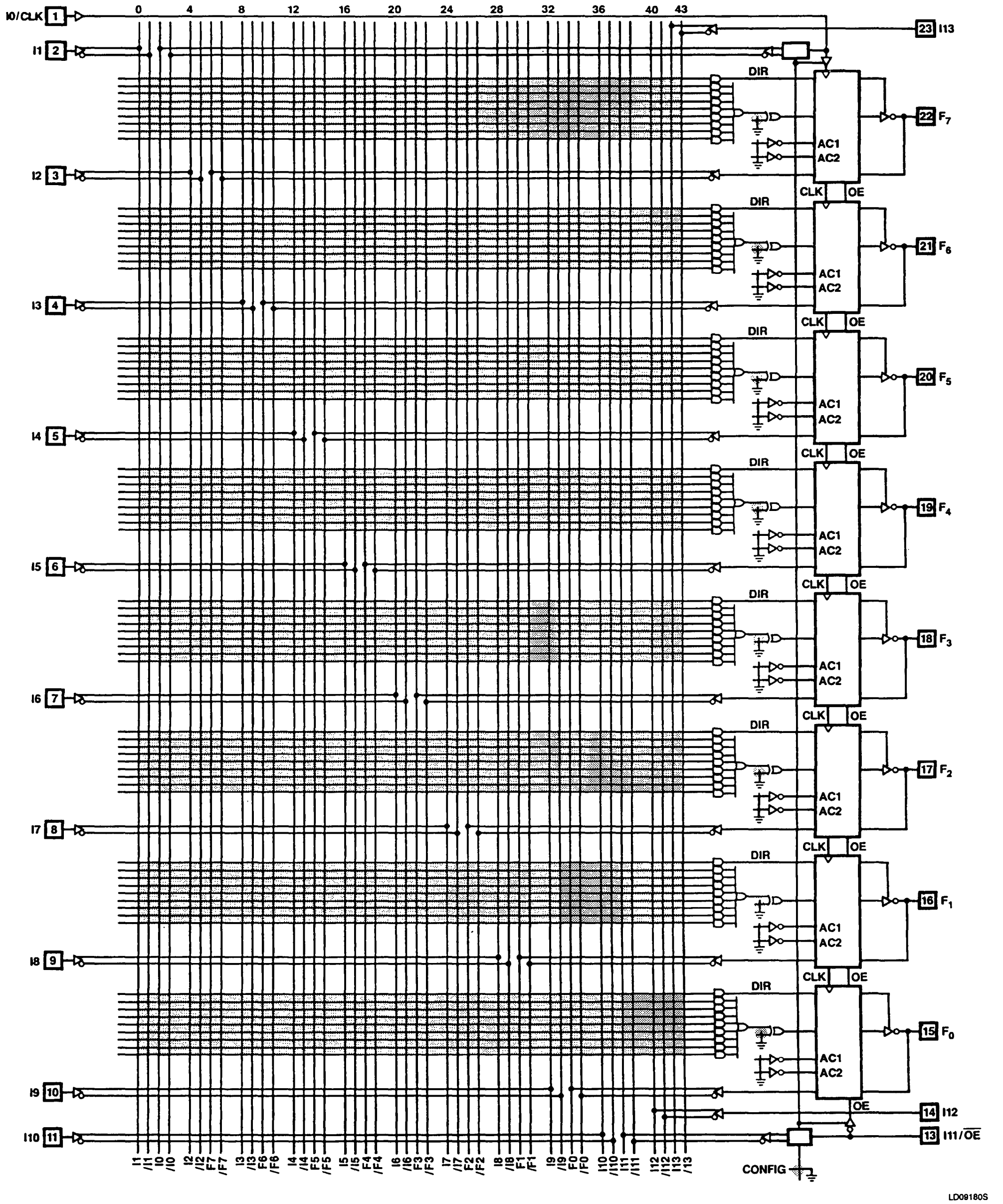
PIN NO.	PLC 20V8	20R8 20RP8	20R6 20RP6	20R4 20RP4	20L8 20H8 20P8	20L2 20H2 20P2	18L4 18H4 18P4	16L6 16H6 16P6	14L8 14H8 14P8
1	I_0/CLK	CLK	CLK	CLK	I	I	I	I	I
13	I_{11}/$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I	I
14	I_{12}	I	I	I	I	I	I	I	I
15	F0	D	B	B	O	I	I	I	O
16	F1	D	D	B	B	I	I	O	O
17	F2	D	D	D	B	I	O	O	O
18	F3	D	D	D	B	O	O	O	O
19	F4	D	D	D	B	O	O	O	O
20	F5	D	D	D	B	I	O	O	O
21	F6	D	D	B	B	I	I	O	O
22	F7	D	B	B	O	I	I	I	O
23	I13	I	I	I	I	I	I	I	I

® PAL is a registered trademark of Monolithic Memories, Inc., a wholly owned subsidiary of Advanced Micro Devices, Inc.

Erasable and OTP PAL®-Type Device

PLC20V8 Series

LOGIC DIAGRAM


I0/CLK 1
I1 2
I2 3
I3 4
I4 5
I5 6
I6 7
I7 8
I8 9
I9 10
I10 11
0
4
8
12
16
20
24
28
32
36
40
43
DIR
AC1
AC2
CLK
OE
23 I13
22 F7
21 F6
20 F5
19 F4
18 F3
17 F2
16 F1
15 F0
14 I12
13 I11/OE
I1 /I1 I0 /I0 I2 /I2 F7 /F7 I3 /I3 F6 /F6 I4 /I4 F5 /F5 I5 /I5 F4 /F4 I6 /I6 F3 /F3 I7 /I7 F2 /F2 I8 /I8 F1 /F1 I9 /I9 F0 /F0 I10 /I10 I11 /I11 I12 /I12 I13 /I13
CONFIG
LD09180S

NOTES:

In the unprogrammed or virgin state:

All cells are in a conductive state.

All AND gate locations are pulled to a logic "0" (Low).

Output polarity is non-inverting.

Pins 1 and 13 are configured as inputs 0 and 11, respectively, via the configuration cell. The clock and $\overline{\text{OE}}$ functions are disabled.

All output macro cells (OMC) are configured as bidrectional I/O, with the outputs disabled via the direction term.

⊕ Denotes a programmable cell location.

Erasable and OTP PAL®-Type Device

PLC20V8 Series

The Signetics state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at one-quarter to one-half the power consumption. The erasable nature of the EPROM process enables Signetics to functionally test the devices prior to shipment to the customer. Additionally, this allows Signetics to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

Signetics' AMAZE PLD design software supports all aspects of design, simulation and programming. For simple conversion of existing PAL device codes into the PLC20V8 series format, a PAL-to-V8 converter is also available. SimPal, (sim'pal), a stand-alone, single-disk software package translates a PAL device code (from a device or a JEDEC standard fuse map) into an equivalent PLC20V8 series JEDEC format. The SimPal PAL-to-V8 converter, which runs on an IBM PC or compatible, includes the necessary programmer interface software for most commercially available programmers.

THE OUTPUT MACRO CELL (OMC)

The PLC20V8 has 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the table, 4 different configurations may be implemented.

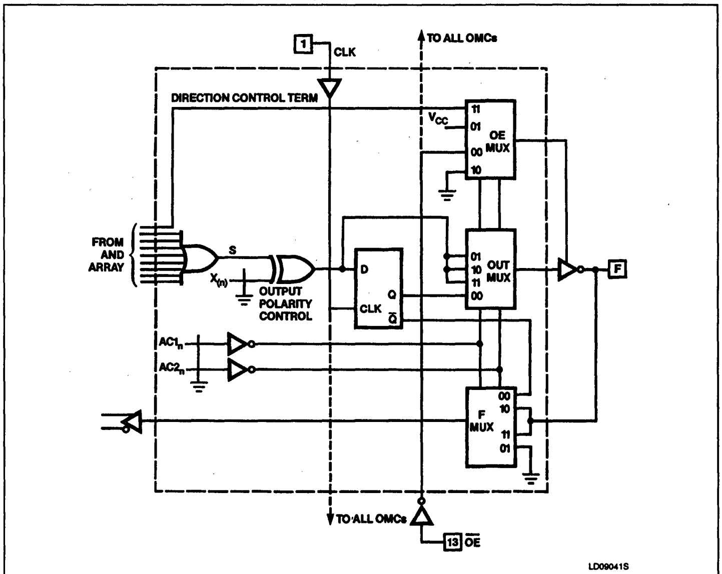
CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 13. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 13 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 13 are both dedicated inputs. Note that the output enable for all registered OMCs is common — from Pin 13 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_n$	$AC2_n$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registered OMCs from Pin 13 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 13 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 13 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 13 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

OUTPUT MACRO CELL (OMC)



NOTE:
□ Denotes a programmable cell location.

If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 13, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 13 are dedicated inputs. The programming codes are as follow:

Pin 1 = CLK, Pin 13 = $\overline{OE}$	L
Pin 1 and Pin 13 = Input	H

Erasable and OTP PAL®-Type Device

PLC20V8 Series

ORDERING INFORMATION

DESCRIPTION			ORDER CODE
Propagation Delay (Max)		I_{CC} (Active at 15MHz)	
t_{PD} = 35ns	f_{MAX} = 18.1MHz (Synchronous)	50mA	PLC20V8Q35
		90mA	PLC20V8H35
t_{PD} = 45ns	f_{MAX} = 13.3MHz (Synchronous)	50mA	PLC20V8Q45
		90mA	PLC20V8H45
Package Type			PACKAGE[1]
24-pin Plastic DIP (one time programmable; OTP)			N
24-pin Plastic Leaded Chip Carrier (one time programmable; OTP)			A
24-pin Ceramic DIP with quartz window (reprogrammable)			FA

NOTE:

1. The package order code directly follows the device order code, i.e., PLC20V8Q35N for Plastic DIP (OTP).

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V_{DC}
V_{IN}	Input voltage	-0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	-0.5 to V_{CC} +0.5	V_{DC}
I_{IN}	Input currents	-10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature rnage	-65 to +150	°C

NOTE:

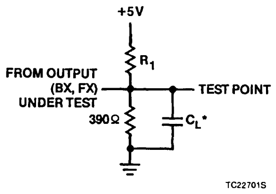
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLC20V8 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

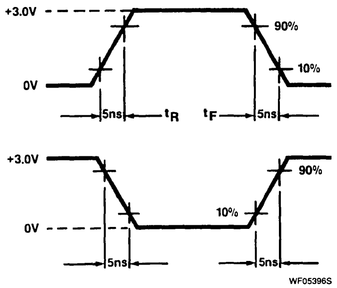
AC TEST CONDITIONS



*C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Erasable and OTP PAL®-Type Device

PLC20V8 Series

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION		LIMITS			UNIT
				Min	Typ[1]	Max	
Input voltage[2]							
V_{IL}	Low	V_{CC} = Min		−0.3		0.8	V
V_{IH}	High	V_{CC} = Max		2.0		V_{CC} + 0.3	V
Output voltage[2]							
V_{OL}	Low	V_{CC} = Min I_{OL} = 24mA				0.5	V
V_{OH}	High	I_{OH} = −3.2mA		2.4			V
Input current							
I_{IL}	Low[6]	V_{IN} = GND				−10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND				10 −10	µA µA
I_{OS}	Short-circuit[3, 7]	V_{OUT} = GND				−130	mA
I_{CC}	V_{CC} supply current (Active)[4]	I_{OUT} = 0mA f = 15MHz[5]	Quarter power (Q)			50	mA
			Half power (H)			90	mA
Capacitance							
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V			12		pF
C_B	I/O	V_B = 2.0V			15		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all inputs and outputs switching.
5. Refer to Figure 1, ΔI_{CC} vs Frequency (worst case). (Referenced from 15MHz)
6. I_{IL} for Pin 1 (I_0/CLK) is ±10µA with V_{IN} = 0.4V.
7. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.

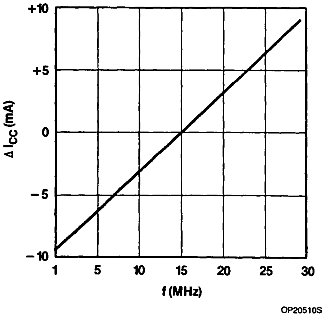


Figure 1. ΔI_{CC} **vs Frequency (Worst Case) (Referenced from 15MHz)**

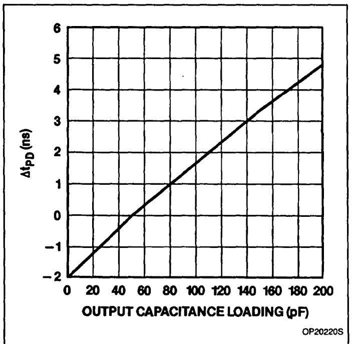


Figure 2. Δt_{PD} **vs Output Capacitance Loading (Typical)**

AC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$ $R_2 = 390\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION[1]		PLC20V8Q-35 PLC20V8H-35		PLC20V8Q-45 PLC20V8H-45		UNIT
				R_1 (Ω)	C_L (pF)	Min	Max	Min	Max	
Pulse width										
t_{CKP}	Clock period (Minimum t_{IS} + t_{CKO})	CLK +	CLK +			55		75		ns
t_{CKH}	Clock width High	CLK –	CLK +			20		25		ns
t_{CKL}	Clock width Low	CLK +	CLK –			20		25		ns
Hold time										
t_{IH}	Input or feedback data hold time	Input ±	CLK +			0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	CLK +	I ±, F ±			30		40		ns
Propagation delay										
t_{PD}	Delay from input to active output	F ±	I ±, F ±	200	50		35		45	ns
t_{CKO}	Clock High to output valid access Time	F ±	CLK +	200	50		25		35	ns
t_{OE1}[3]	Product term enable to active output	F ±	I ±, F ±	Active-High R = 1.5k Active-Low R = 550	50		35		45	ns
t_{OD1}[2]	Product term disable to outputs off	F ±	I ±, F ±	From V_{OH} R = ∞ From V_{OL} R = 200	5		35		45	ns
t_{OD2}[2]	Pin 13 output disable High to outputs off	F ±	OE –	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		30	ns
t_{OE2}[3]	Pin 13 output enable to active output	F ±	OE +	Active-High R = 1.5k Active-Low R = 550	50		25		30	ns
t_{PPR}	Power-up reset	F +	V_{CC} +				35		45	ns
Frequency of operation (t_{IS} + t_{CKO})										
f_{MAX}	Maximum frequency	Synch. Asynch.		200	50		18.1 28.5		13.3 22.2	MHz

NOTES:

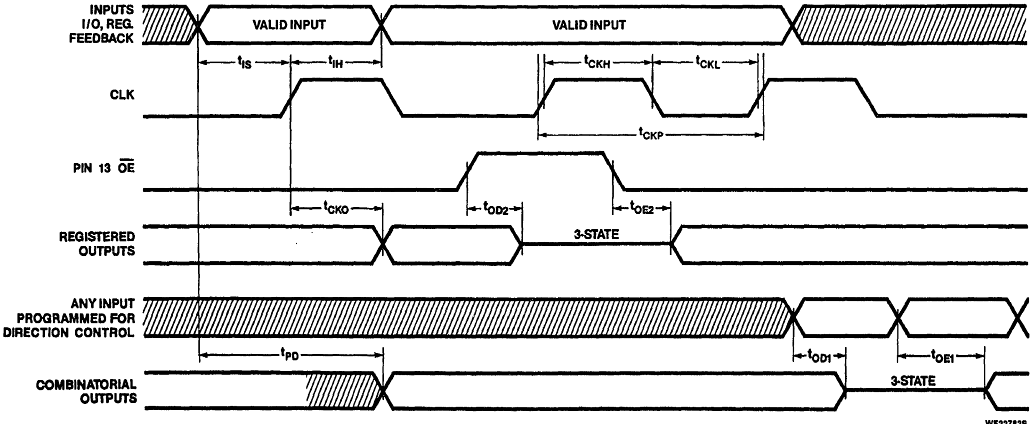
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. 3-State levels are measured ±0.5V from the active steady-state level.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.

POWER-UP RESET

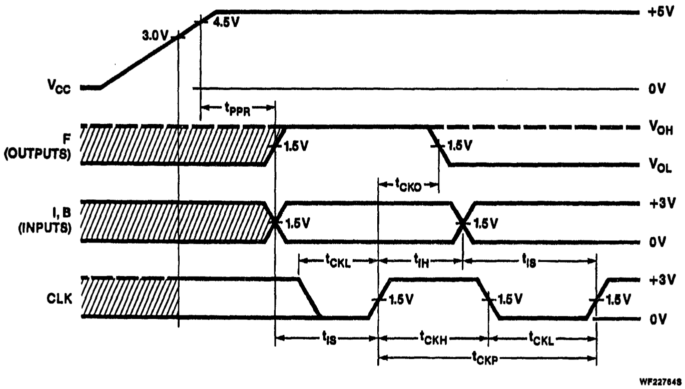
In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC20V8. All internal registers will reset to active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an active-High on the associated output pin because of the inverted output buffer. The internal feedback ($\overline{Q}$) of a registered OMC will also be set High. The programmed polarity of OMC will not affect the active-High output condition during a system power-up condition.

The following conditions must be considered when the asynchronous power-up reset occurs. V_{CC} rise to 4.5V (90%) must be monotonic. The clock input must stabilize to a valid TTL level prior to the V_{CC} rise to 60% (3.0V). All input setup and hold times (t_{IS} and t_{IH}) must be adhered to prior to clocking the device.

TIMING DIAGRAMS



Switching Waveforms



NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output conditon (enabled or disabled).

Power-Up Reset

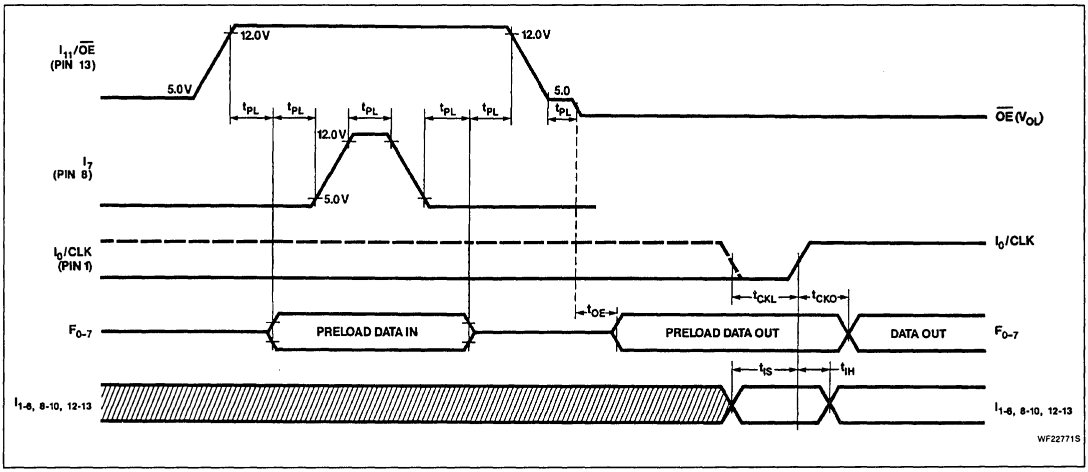
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC20V8 series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 13 and 8 ($I_{11}/\overline{OE}$ and I_7). (See diagram for timing and sequence.)

To read the data out, Pins 13 and 8 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register $\overline{Q}$ output via the feedback path will reflect the complement of the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references.

REGISTER PRELOAD (DIAGNOSTIC MODE)



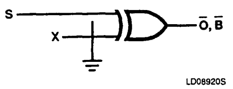
LOGIC PROGRAMMING

The EPLD can be programmed by means of Logic Programming equipment.

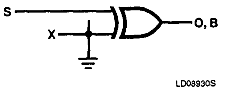
With Logic programming, the AND/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2, as shown below. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY — (O, B)

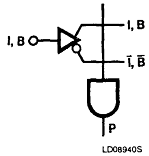


ACTIVE LEVEL	CODE
INVERTING	L

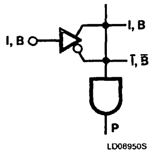


ACTIVE LEVEL	CODE
NON-INVERTING	H

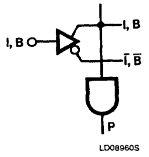
"AND" ARRAY — (I, B)



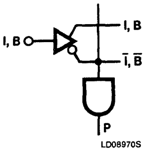
STATE	CODE
DON'T CARE	-



STATE	CODE
INACTIVE	O

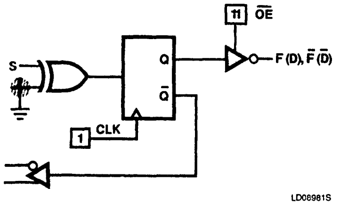


STATE	CODE
I, B	H

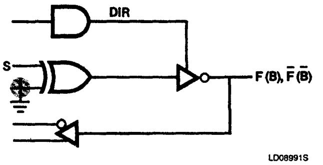


STATE	CODE
I̅, B̅	L

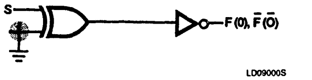
ARCHITECTURE CONTROL — AC1 and AC2



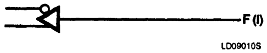
OMC CONFIGURATION	CODE
REGISTERED (D-TYPE)	D



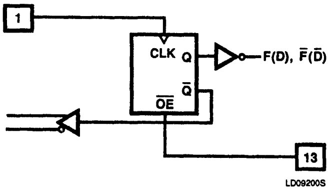
OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O (COMBINATORIAL)	B



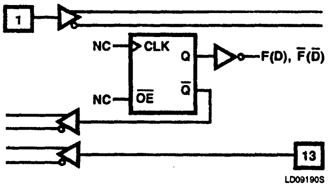
OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I



CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 13 = $\overline{OE}$	L



CONFIGURATION CELL	CODE
PIN 1 = INPUT 13 = INPUT	H[6]

NOTE:

A factory shipped unprogrammed device is configured such that:

1. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is non-inverting.
4. Pins 1 and 13 are configured as inputs 0 and 11. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 13, respectively, if any one OMC is programmed as registered.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC20V8 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 - 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC20V8 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC20V8 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC20V8 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

Erasable and OTP PAL®-Type Device

PLC20V8 Series

PROGRAM TABLE

NOTES:
In the unprogrammed or virgin state:
- All AND gate locations are pulled to a logic "0" (Low).
- Output polarity is non-inverting.
- Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and OE functions are disabled.
- All output macro cells (OMC) are configured as combinatorial I/O, with the outputs disabled via the direction control term.

CUSTOMER NAME ____________________

PURCHASE ORDER # ____________________

SIGNETICS DEVICE # ____________ CF (XXXX) ____________

CUSTOMER SYMBOLIZED PART # ____________________

TOTAL NUMBER OF PARTS ____________________

PROGRAM TABLE # ____________ REV. ____________ DATE ____________

CONFIGURATION CELL (CLK/$\overline{OE}$ CONTROL) □

ARCH. CONTROL BITS □□□□□□□□

OUTPUT POLARITY □□□□□□□□

TERM	AND																						OR (FIXED)							
	I														F (I)								F (B, O, D)							
	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																							D	/	/	/	/	/	/	/
1																							A	/	/	/	/	/	/	/
2																							A	/	/	/	/	/	/	/
3																							A	/	/	/	/	/	/	/
4																							A	/	/	/	/	/	/	/
5																							A	/	/	/	/	/	/	/
6																							A	/	/	/	/	/	/	/
7																							A	/	/	/	/	/	/	/
8																							A	/	/	/	/	/	/	/
9																							/	D	/	/	/	/	/	/
10																							/	A	/	/	/	/	/	/
11																							/	A	/	/	/	/	/	/
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71																							/	/	/	/	/	/	/	A
PIN	23	14	13	11	10	9	8	7	6	5	4	3	2	1	22	21	20	19	18	17	16	15	22	21	20	19	18	17	16	15
VARIABLE NAME																														

AND ARRAY		CONTROL				OR ARRAY (FIXED)	
		OMC ARCH.		OUTPUT POLARITY		DATA CANNOT BE ENTERED INTO THE OR ARRAY FIELD DUE TO THE FIXED NATURE OF THE DEVICE ARCHITECTURE.	
INACTIVE	O	REGISTERED (D-TYPE)	D	NON-INVERTING	H	DIRECTION CONTROL	D
I, F (I, B)	H	FIXED INPUT	I	INVERTING	L	ACTIVE OUTPUT	A
$\overline{\text{I, F (I, B)}}$	L	FIXED OUTPUT	O	CONFIG. CELL*		NOT USED	/
DON'T CARE	—	BIDIRECTIONAL I/O	B	PIN 1 = CLK; PIN 13 = $\overline{OE}$	L		
				PIN 1, PIN 13 = INPUT	H		

* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.

TB03620S

Signetics

PLUS20R8D Series
PAL®-Type Devices

Signetics Programmable Logic
Preliminary Specification

Application Specific Products
- **Series 24**

FEATURES

- **Ultra high-speed:**
  - **t_{PD} = 10ns**
  - **f_{MAX} = 55.5MHz (with feedback)**
  - **t_{IS} = 10ns (worst case)**
  - **t_{CKO} = 8ns (worst case)**
- **100% functionally and pin-for-pin compatible with industry standard 24-pin PAL ICs**
- **Power-up reset function to enhance state machine design and testability**
- **Design support provided via AMAZE and other CAD tools for Series 24 PAL devices**
- **Field-programmable on industry standard programmers**
- **Security fuse**
- **Individual 3-State control of all outputs**

DESCRIPTION

The Signetics PLUS20XXD family is an ultra high-speed 10ns version of existing Series 24 PAL devices.

The PLUS20XXD family is 100% functional and pin-compatible with the 20L8, 20R8, 20R6, and 20R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided.

The PLUS20R8D, R6D, and R4D have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

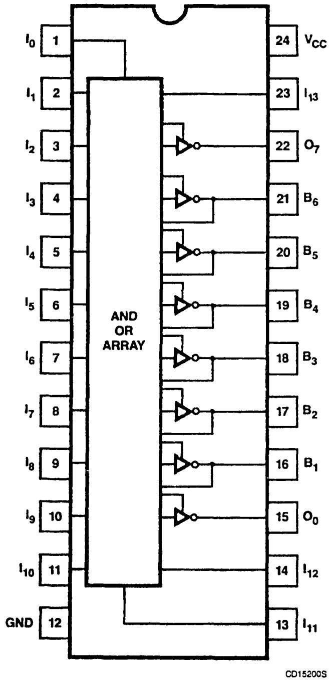
In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

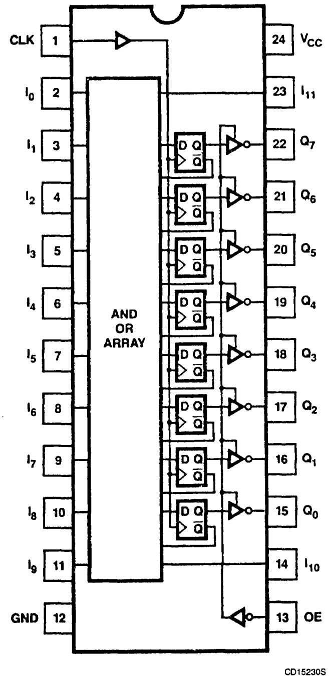
The PLUS20XXD family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS	t_{PD}	I_{CC}	f_{MAX} WITHOUT FEEDBACK	f_{MAX} WITH FEEDBACK
PLUS20L8D	14	8(6 I/O)	0	10ns	210mA		
PLUS20R8D	12	0	8		210mA	62.5MHz	55.5MHz
PLUS20R6D	12	2 I/O	6	10ns	210mA	62.5MHz	55.5MHz
PLUS20R4D	12	4 I/O	4	10ns	210mA	62.5MHz	55.5MHz

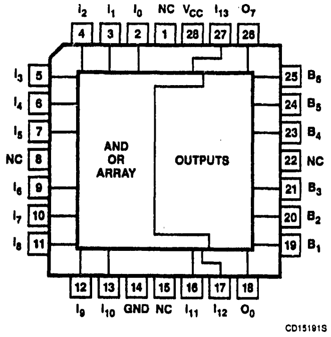
PLUS20L8D



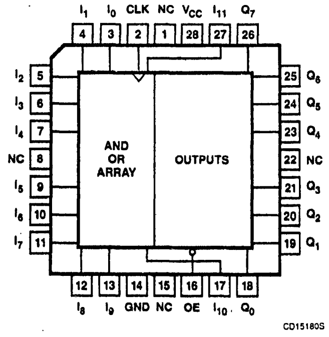
PLUS20R8D



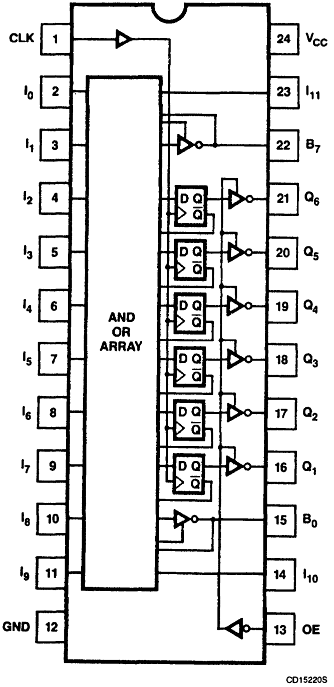
PLUS20L8D



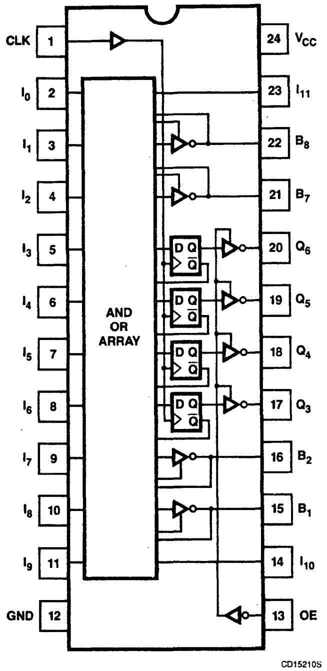
PLUS20R8D



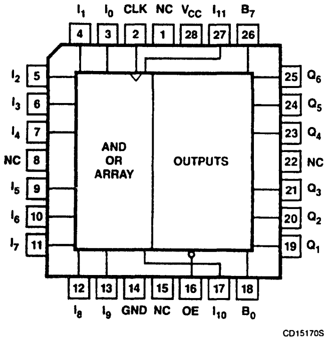
PLUS20R6D



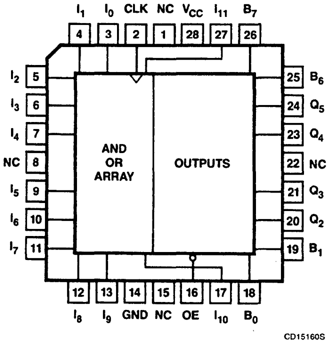
PLUS20R4D



PLUS20R6D



PLUS20R4D



Signetics

Section 4 Programmable Logic Array Device Data Sheets

Application Specific Products

INDEX

Series 20

PLS151 Field-Programmable Gate Array (18 × 15 × 12); 25ns 4-3
PLC153 Erasable and OTP Programmable Logic Array (18 × 32 × 10); 45/60ns 4-9
PLS153 Field-Programmable Logic Array (18 × 42 × 10); 40ns 4-16
PLS153A Field-Programmable Logic Array (18 × 42 × 10); 30ns 4-22
PLHS153 Field-Programmable Logic Array (18 × 42 × 10); 20ns 4-28
PLUS153B Field-Programmable Logic Array (18 × 42 × 10); 15ns 4-34
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Series 24

PLS161 Field-Programmable Logic Array (12 × 48 × 8); 50ns 4-46
PLS162 Field-Programmable Address Decoder (16 × 5); 30ns 4-52
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PLC473-60 Erasable and OTP Programmable Logic Array (20 × 24 × 11); 60ns . 4-82
PLHS473 Field-Programmable Logic Array (20 × 24 × 11); 22ns 4-89

Series 28

PLS100/101 Programmable Logic Array (16 × 48 × 8); 50ns 4-95
PLS103 Programmable Gate Array (16 × 9 × 9); 35ns 4-102

Signetics

PLS151

Field-Programmable Gate Array (18 × 15 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLS151 is a single level logic element, consisting of 15 AND gates with fusible link connections for programming I/O polarity, I/O direction and output enable control.

All gates are linked to 6 inputs (I) and 12 bidirectional I/O lines (B). These yield variable I/O gate configurations via 3 direction control gates (D), ranging from 18 inputs to 12 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to each AND gate. The polarity of all gate outputs is individually programmable through a set of EX-OR gates for implementing AND/NAND logic functions. Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its inputs and outputs (DeMorgan's Theorem).

The PLS151 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

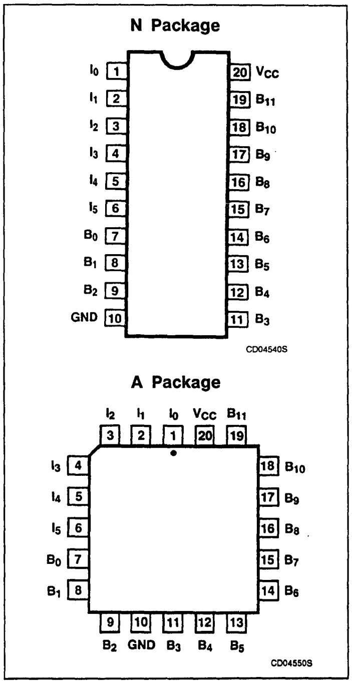
FEATURES

- **Field-Programmable (Ni-Cr link)**
- **6 inputs**
- **15 product terms:**
  - **12 logic terms**
  - **3 control terms**
- **12 bidirectional I/O lines**
- **Programmable output polarity**
  - **Active-High or -Low outputs**
- **Programmable output enable**
- **Power dissipation: 575mW (typ.)**
- **I/O propagation delay: 25ns (max.)**
- **Input loading: −100μA (max.)**
- **TTL compatible**
- **3-State outputs**

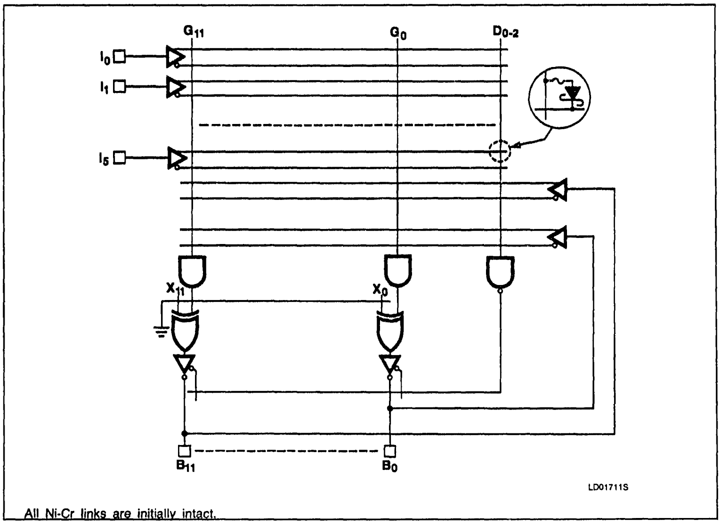
APPLICATIONS

- **Random gating functions**
- **Address decoding**
- **Code detectors**
- **Memory mapped I/O**
- **Fault monitors**
- **I/O port decoders**

PIN CONFIGURATIONS



FUNCTIONAL DIAGRAM



All Ni-Cr links are initially intact.

LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$X = A \cdot \overline{B} \cdot C \cdot \ldots$

ACTIVE-LOW

$X = \overline{A \cdot \overline{B} \cdot C \cdot} \ldots$

$X = \overline{A} + B + \overline{C} + \ldots$

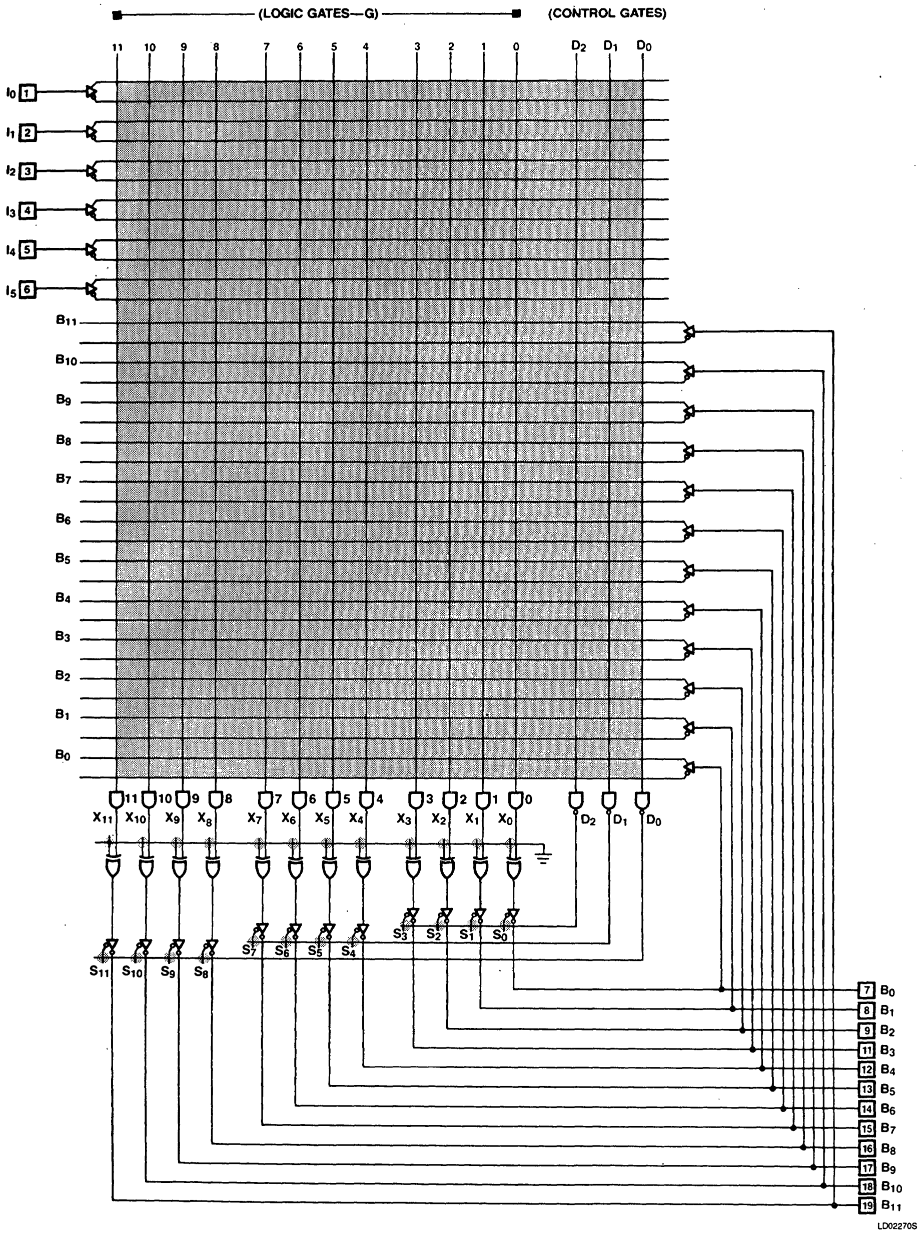
NOTES:

1. For each of the 12 outputs, either function X (Active-High) or $\overline{X}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

Field-Programmable Gate Array (18 × 15 × 12)

PLS151

FPGA LOGIC DIAGRAM



NOTES:
1. All gato inputs with a blown link float to a logic "1".
2. Programmable connection.

Field-Programmable Gate Array (18 × 15 × 12)

PLS151

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLS151N
20-pin Plastic Leaded Chip Carrier	PLS151A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS[1]		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[2, 3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OL}	Low	I_{OL} = 10mA			0.5	V
V_{OH}	High	I_{OH} = −2mA	2.4			V
Input current[6]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			−100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			−140	
I_{OS}	Short circuit[3, 4]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		115	155	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

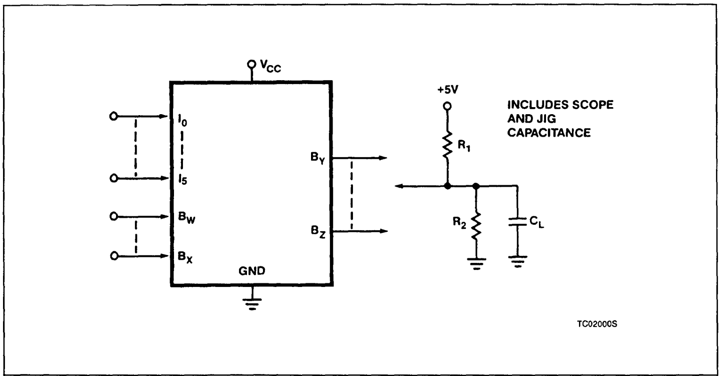
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[1]	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		16	25	ns
t_{OE}	Output enable	Output −	Input ±			17	25	ns
t_{OD}	Output disable[5]	Ouput +	Input ±	$C_L = 5pF$		17	25	ns

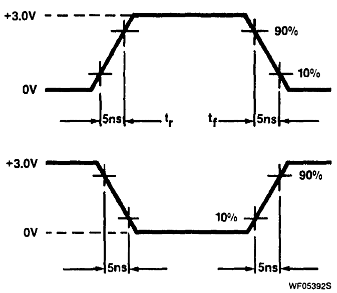
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one pin at a time.
4. Duration of short circuit should not exceed 1 second.
5. Measured at $V_T = V_{OL} + 0.5V$.
6. I_{IL} and I_{IH} limits are for dedicated inputs only (I_O–I_5).

TEST LOAD CIRCUITS



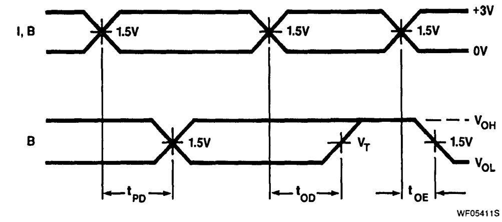
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAM



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

Field-Programmable Gate Array (18 × 15 × 12)

PLS151

LOGIC PROGRAMMING

In a virgin device all Ni-Cr links are intact. PLS151 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLS151 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

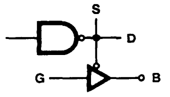
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

VIRGIN STATE

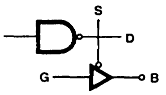
A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at 'H' polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.
4. All B terms are I/O unless otherwise programmed.

I/O DIRECTION – (B)

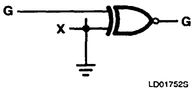


DIRECTION	CODE
I/O[1]	A

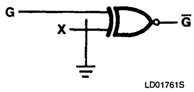


DIRECTION	CODE
INPUT	•

OUTPUT POLARITY – (B)

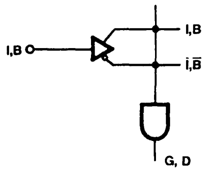


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

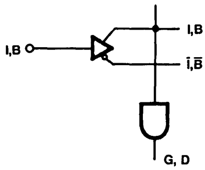


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

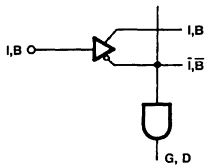
"AND" ARRAY – (I, B)



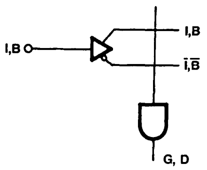
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H



STATE	CODE
$\bar{I}$, $\bar{B}$	L



STATE	CODE
DON'T CARE	-

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the True and Complement of an input (either I or B) are left intact.

Field-Programmable Gate Array (18 × 15 × 12)

PLS151

FPGA PROGRAM TABLE

CUSTOMER NAME ____________

PURCHASE ORDER # ____________

SIGNETICS DEVICE # ____________ CF (XXXX)

CUSTOMER SYMBOLIZED PART # ____________

TOTAL NUMBER OF PARTS ____________

PROGRAM TABLE # ________ REV ________ DATE ________

D2 = ____________

G0 = ____________

G1 = ____________

G2 = ____________

G3 = ____________

D1 = ____________

G4 = ____________

G5 = ____________

G6 = ____________

G7 = ____________

D0 = ____________

G8 = ____________

G9 = ____________

G10 = ____________

G11 = ____________

NOTES

1. The FPGA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I and B bits are normally programmed Don't Care (–).
3. Unused Gates can be left blank.
4. Disregard Polarity for Gates used only as inputs.

CONTROL

HIGH	H	(POL.)
LOW	L	
I/O	A	(DIR.)
INPUT	●	

AND

I, B

INACTIVE	0
I, B	H
$\bar{I}, \bar{B}$	L
Don't Care	–

PIN	GATE	DIR.	POL.	AND																	
				I						B (I)											
				5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0
■	D2	■	■																		
7	00																				
8	01																				
9	02																				
11	03																				
■	D1	■	■																		
12	04																				
13	05																				
14	06																				
15	07																				
■	D0	■	■																		
16	08																				
17	09																				
18	10																				
19	11																				
■	■	PIN		6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	8	7
VARIABLE NAME																					

TB01720S

Signetics

PLC153
Erasable and OTP Programmable Logic Array (18 × 42 × 10)

Application Specific Products
• Series 20

Signetics Programmable Logic
Product Specification

DESCRIPTION

The PLC153 CMOS devices are two-level logic Erasable and OTP (One Time Programmable) Programmable Logic Arrays. The PLC153 devices are low power versions of the Signetics PLS153/153A and PLHS153 Bipolar Programmable Logic devices. EPROM cells provide the connections for the programmable AND array, the programmable OR array and the Ex-OR output polarity gates.

On-chip buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) inputs to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of Ex-OR gates for implementing AND/OR or AND/NOR logic functions.

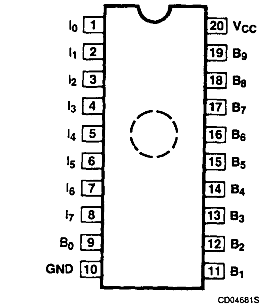
The PLC153 is field-programmable, using Floating-Gate EPROM cells. This enables the generation of custom logic patterns using standard programming equipment.

FEATURES

- **Low power, 100% functional replacement for PLS153 Series PLAs**
- **EPROM cell technology**
  - **Erasable (quartz window package only)**
  - **100% Testable**
  - **Reconfigurable**
- **8 dedicated inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 45 and 60ns (max.)**
- **Input loading: – 10μA (max)**
- **Power dissipation: 60mA at 15MHz (max)**
- **3-State outputs**
- **CMOS and TTL compatible**

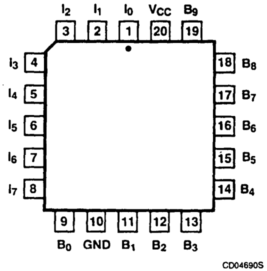
PIN CONFIGURATIONS

N and FA Packages



N = Plastic
FA = Ceramic with Quartz Window

A Package

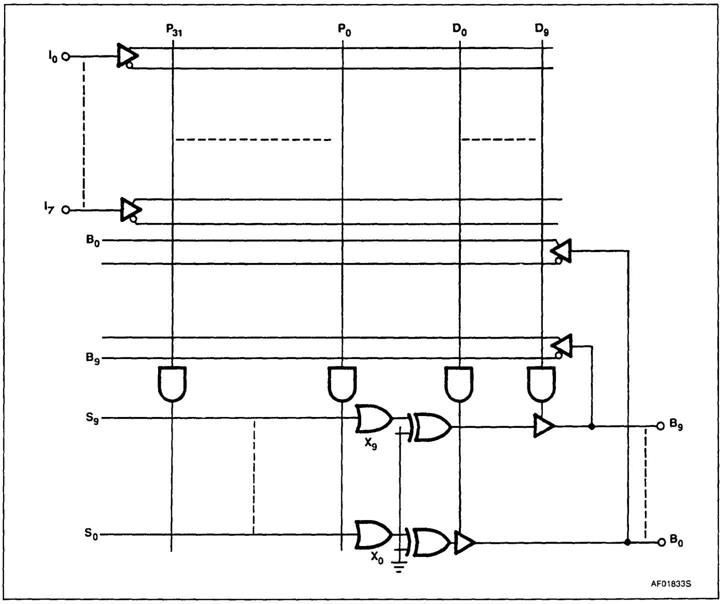


A = Plastic Leaded Chip Carrier

APPLICATIONS

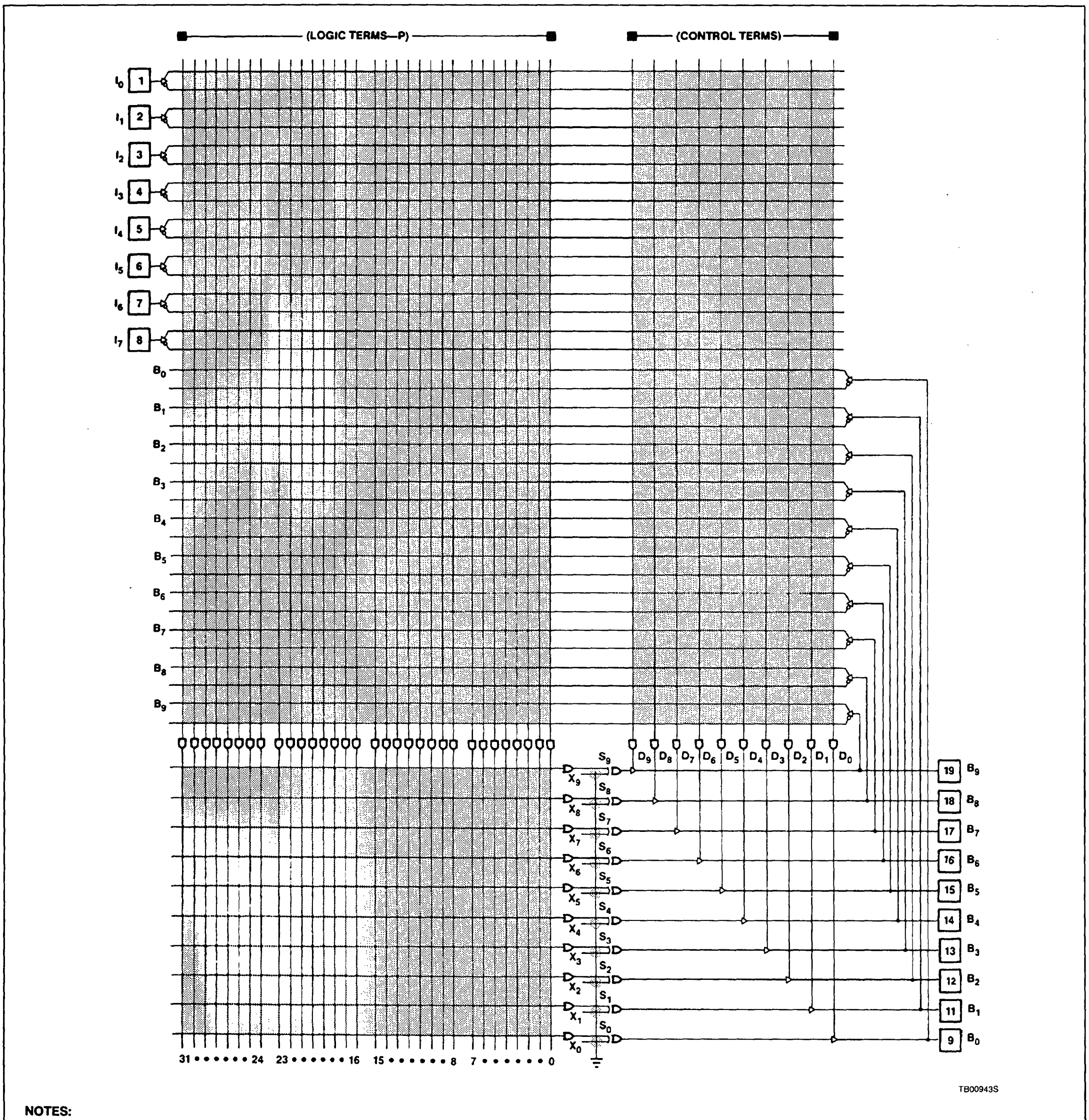
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

FUNCTIONAL DIAGRAM



Programmable Logic Array (18 × 42 × 10) PLC153

FPLA LOGIC DIAGRAM



NOTES:

1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Programmable Logic Array (18 × 42 × 10) PLC153

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP with Window (300mil-wide)	PLC153-45FA
	PLC153-60FA
20-Pin Plastic DIP (300mil-wide)	PLC153-45N
	PLC153-60N
20-Pin Plastic Leaded Chip Carrier	PLC153-45A
	PLC153-60A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	70°C
Allowable thermal rise ambient to junction	70°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	-30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +70°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min	-0.3		0.8	V
V_{IH}	High	V_{CC} = Max	2.0		V_{CC} + 0.3	V
Output voltage[2]						
		V_{CC} = Min				
V_{OL}	Low	I_{OL} = 8mA			0.45	V
V_{OH}	High	I_{OH} = -3mA	2.4			V
Input current[10]						
I_{IL}	Low	V_{IN} = GND			-10	μA
I_{IH}	High	V_{IN} = V_{CC}			10	μA
Output current						
$I_{O(OFF)}$	Hi-Z state[7]	V_{OUT} = V_{CC}			10	μA
		V_{OUT} = GND			-10	μA
I_{OS}	Short circuit[3, 6]	V_{OUT} = GND	-15		-70	mA
I_{CC}	V_{CC} supply current (Active)[4, 5, 9]	No load f = 15MHz TTL inputs		48	60	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		6		pF
C_B	I/O (bidirectional)	V_B = 2.0V		12		pF

Notes on following page.

Programmable Logic Array (18 × 42 × 10) PLC153

AC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +70°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	PLC153-45		PLC153-60		UNIT
					Min	Max	Min	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		45		60	ns
t_{OE}	Output enable	Output −	Input ±	$C_L = 30pF$		45		60	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		45		60	ns

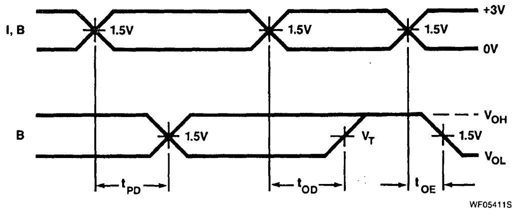
NOTES:

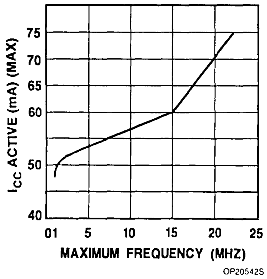
1. All typical values are at $V_{CC} = 5V$. $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. TTL inputs: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
5. Measured with all inputs and outputs switching.
6. Duration of short circuit should not exceed 1 second.
7. Leakage values are a combination of input and output leakage.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Refer to Figure 1 for worst case I_{CC} vs frequency specifications.
10. Pin 1 (V_{pp}) has an input leakage current of 100μA.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM

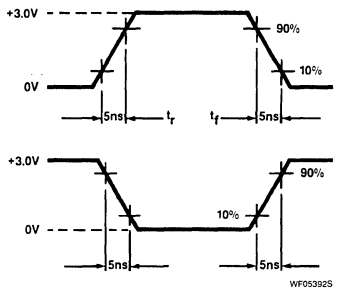




NOTES:
1. Tested with all outputs switching.
2. Tested with TTL inputs.

Figure 1. (Worst-case) I_{CC} vs Frequency

VOLTAGE WAVEFORMS

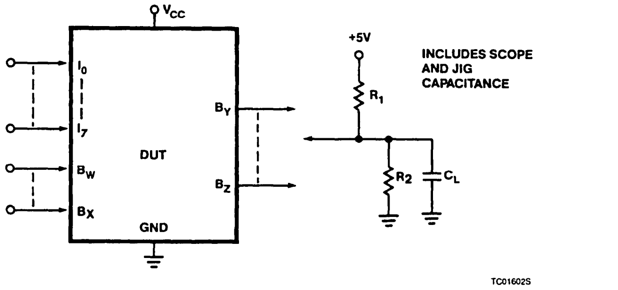


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Programmable Logic Array (18 × 42 × 10) PLC153

TEST LOAD CIRCUITS



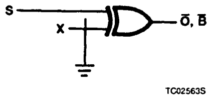
LOGIC PROGRAMMING

The EPLA can be programmed by means of Logic programming equipment.

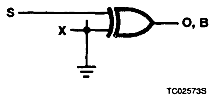
With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table, the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY — (O, B)

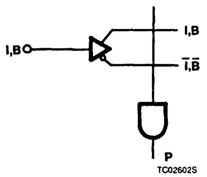


ACTIVE LEVEL	CODE
INVERTING	L

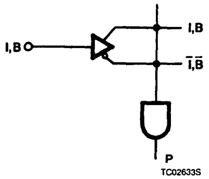


ACTIVE LEVEL	CODE
NON-INVERTING[1]	H

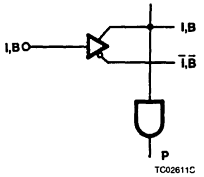
"AND" ARRAY — (I, B)



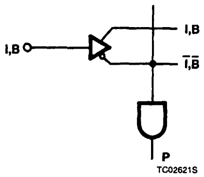
STATE	CODE
DON'T CARE	-



STATE	CODE
INACTIVE[1,2]	O

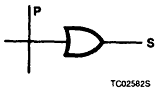


STATE	CODE
I, B	H

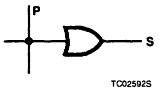


STATE	CODE
$\bar{I}, \bar{B}$	L

"OR" ARRAY — (O, B)



P_n STATUS	CODE
INACTIVE	•



P_n STATUS	CODE
ACTIVE[1]	A

NOTES:

1. This is the initial unprogrammed state of all link pairs.
2. Any Product Term (P_n) will always be inactive if one of its input pairs (I, B) is left unprogrammed as shown.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are inactive.
3. All P_n terms are active in the OR array.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC153 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC153 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC153 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC153 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a $12{,}000\mu\text{W/cm}^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ $12000\mu\text{W/cm}^2$). Exposure of these CMOS to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

Programmable Logic Array (18 × 42 × 10) PLC153

FPLA PROGRAM TABLE

CUSTOMER NAME ____________

PURCHASE ORDER # ____________

SIGNETICS DEVICE # ____________ CF (XXXX)

CUSTOMER SYMBOLIZED PART # ____________

TOTAL NUMBER OF PARTS ____________

PROGRAM TABLE # ______ REV ______ DATE ______

NOTES:

In the unprogrammed state:

- All AND gates are pulled to a logic '0' (Low).
- Output polarity is non-inverting.
- Unused I and B bits in the AND array should be programmed as Don't Care (-).
- Unused product terms in the OR array should be programmed as INACTIVE (o).

OR

B(O): ACTIVE A; INACTIVE •

CONTROL (POL): HIGH H; LOW L

AND

I, B (I): INACTIVE 0; I, B H; $\bar{I}$, $\bar{B}$ L; DON'T CARE —

																				POLARITY									
T E R M	AND																			OR									
	I								B(I)											B(O)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0																												
1																												
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D3																												
D2																												
D1																												
D0																												
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	19	18	17	16	15	14	13	12	11	9
VARIABLE NAME																												

TB00959S

Signetics

PLS153
Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLS153 is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

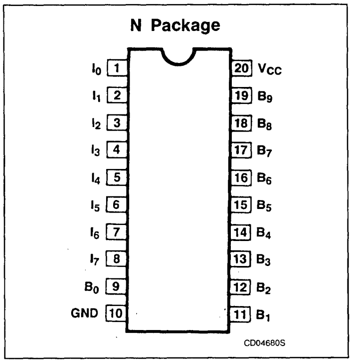
FEATURES

- **Field-Programmable (Ni-Cr links)**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 40ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 650mW (typ.)**
- **3-State outputs**
- **TTL compatible**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

PIN CONFIGURATION



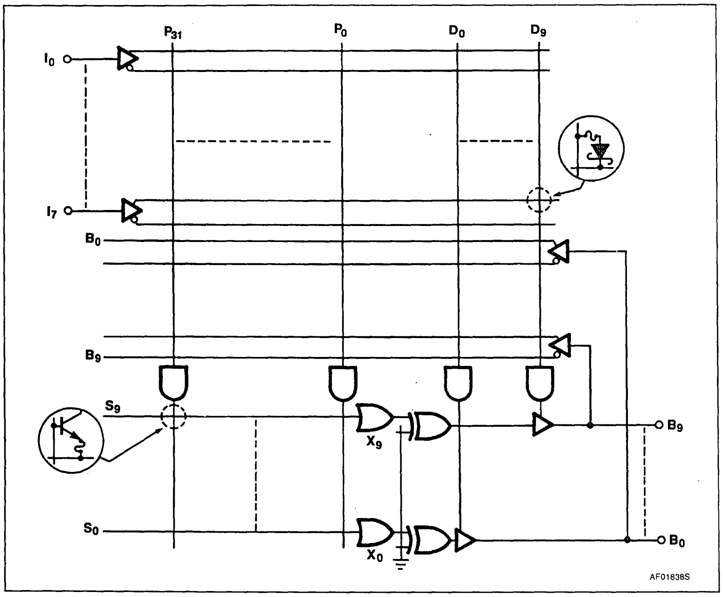
LOGIC FUNCTION

TYPICAL PRODUCT TERM:
Pn = A · B · C · D · . . .
TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
Z = P0 + P1 + P2 . . .

AT OUTPUT POLARITY = L
$Z = \overline{P0 + P1 + P2 +} \ . . .$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot . . .$

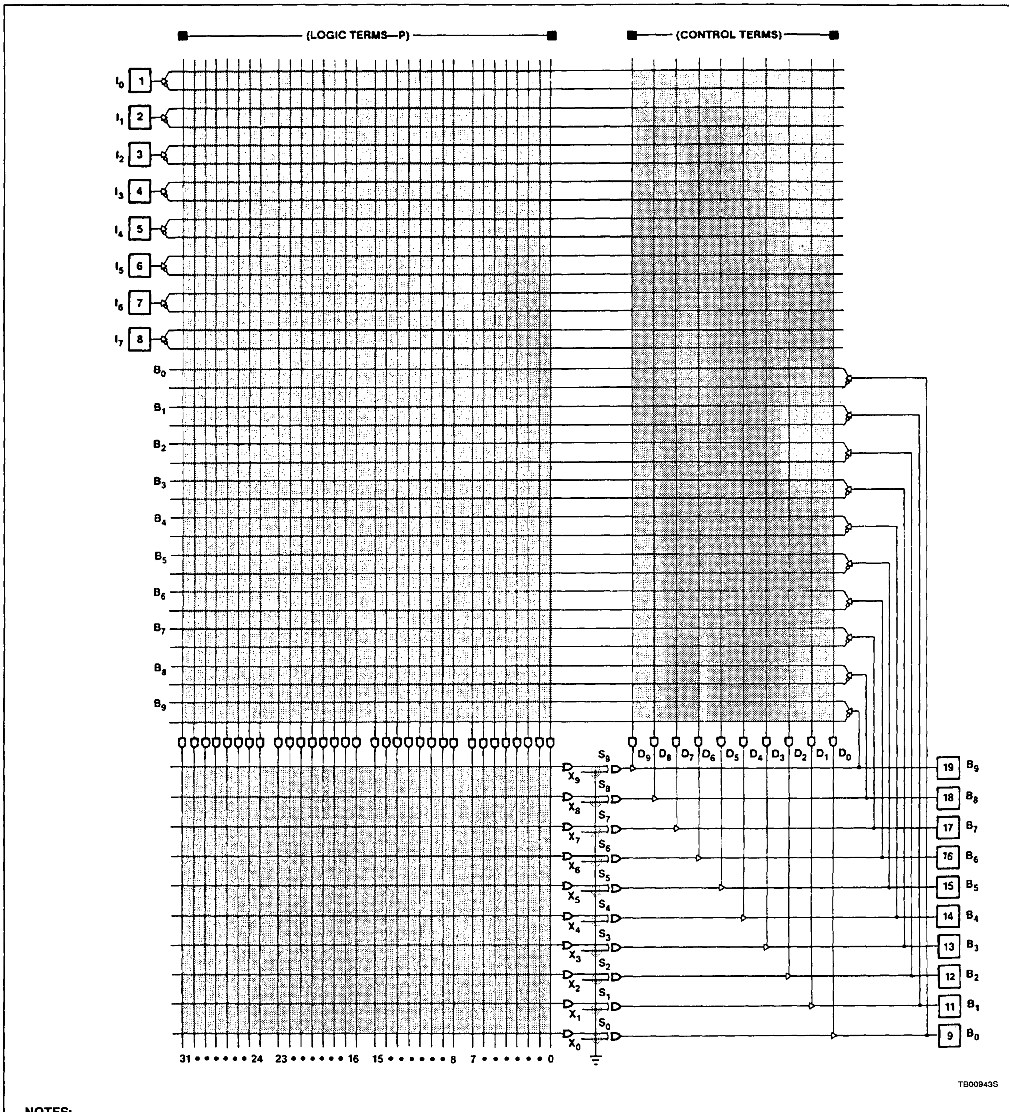
NOTES:
1. For each of the 10 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



Field-Programmable Logic Array (18 × 42 × 10) PLS153

FPLA LOGIC DIAGRAM



NOTES:

1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Array (18 × 42 × 10) PLS153

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLS153N

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS153 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[2, 3]	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = Min				
V_{OL}	Low[2, 4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[2, 5]	I_{OH} = -2mA	2.4			V
Input current[10]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		130	155	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

Field-Programmable Logic Array (18 × 42 × 10) PLS153

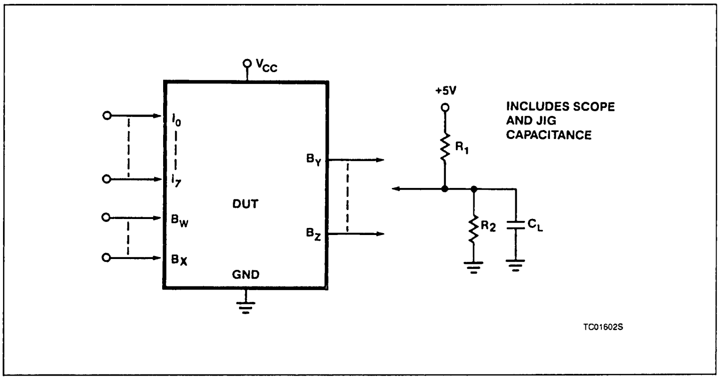
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[1]	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		30	40	ns
t_{OE}	Output enable	Output −	Input ±	$C_L = 30pF$		25	35	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		25	35	ns

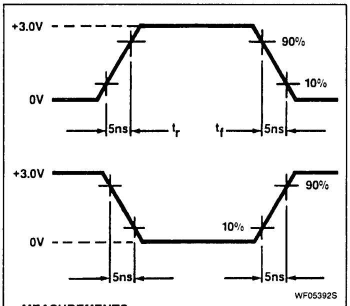
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with +10V applied to I_7.
5. Measured with +10V applied to I_{0-7}. Output sink current is supplied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with I_0, I_1 at 0V, $I_2 - I_7$ and B_{0-9} at 4.5V.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IL} and I_{IH} limits are for dedicated inputs only (I_0-I_7).

TEST LOAD CIRCUITS



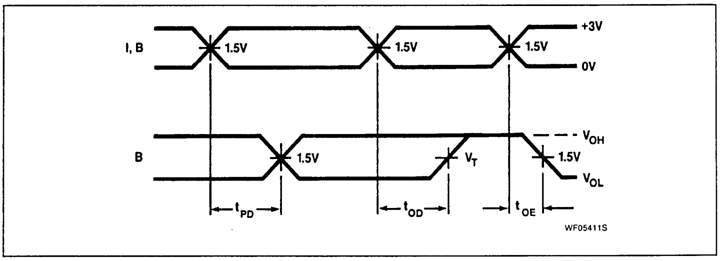
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAM



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

Field-Programmable Logic Array (18 × 42 × 10) PLS153

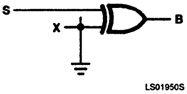
LOGIC PROGRAMMING

PLS153 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

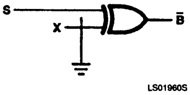
PLS153 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (B)

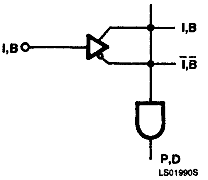


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

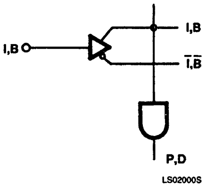


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

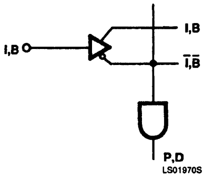
"AND" ARRAY – (I, B)



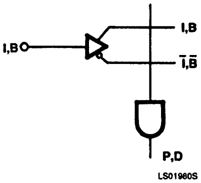
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H

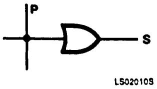


STATE	CODE
$\bar{I}$, $\bar{B}$	L

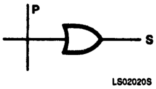


STATE	CODE
DON'T CARE	-

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

[1] This is the initial unprogrammed state of all links.

[2] Any gate P_n will be unconditionally inhibited if both the True and Complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

Field-Programmable Logic Array (18 × 42 × 10) PLS153

FPLA PROGRAM TABLE

CUSTOMER NAME ______
PURCHASE ORDER # ______
SIGNETICS DEVICE # ______ CF (XXXX)
CUSTOMER SYMBOLIZED PART # ______
TOTAL NUMBER OF PARTS ______
PROGRAM TABLE # ______ REV ______ DATE ______

Notes
1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (–).
3. Unused product terms can be left blank.

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

AND

INACTIVE	0	I, B(I)
I, B	H	
Ī, B̄	L	
DON'T CARE	–	

																			POLARITY									
TERM	AND																		OR									
	I								B(I)										B(O)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0																												
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D0																												
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	19	18	17	16	15	14	13	12	11	9
VARIABLE NAME																												

TB00955S

Signetics

PLS153A
Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLS153A is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS153A is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed int the Ordering Information Table.

FEATURES

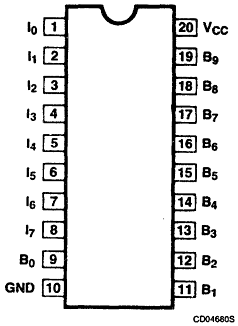
- **Field-Programmable (Ni-Cr links)**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 30ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 650mW (typ.)**
- **3-State outputs**
- **TTL compatible**

APPLICATIONS

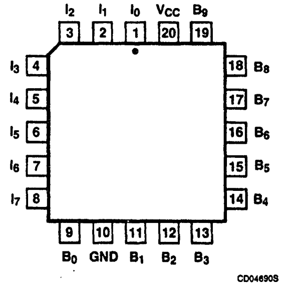
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

PIN CONFIGURATIONS

N Package



A Package



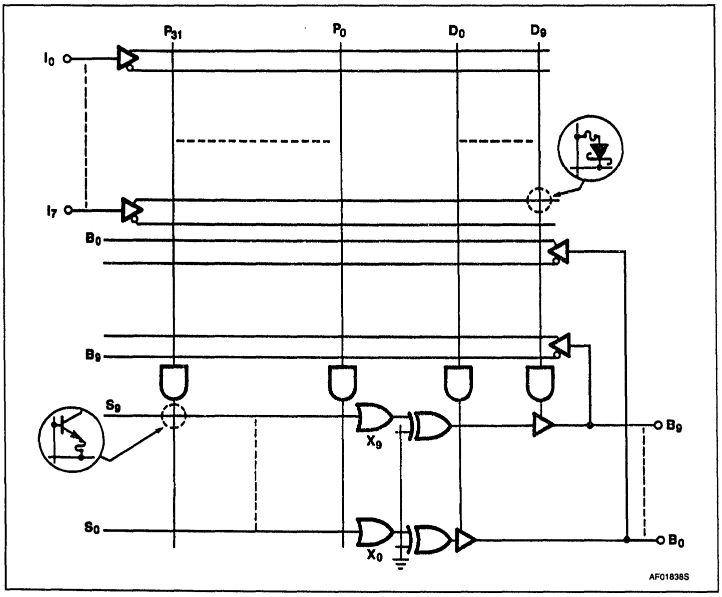
LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$P_n = A \cdot B \cdot C \cdot D \cdot \ldots$
TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

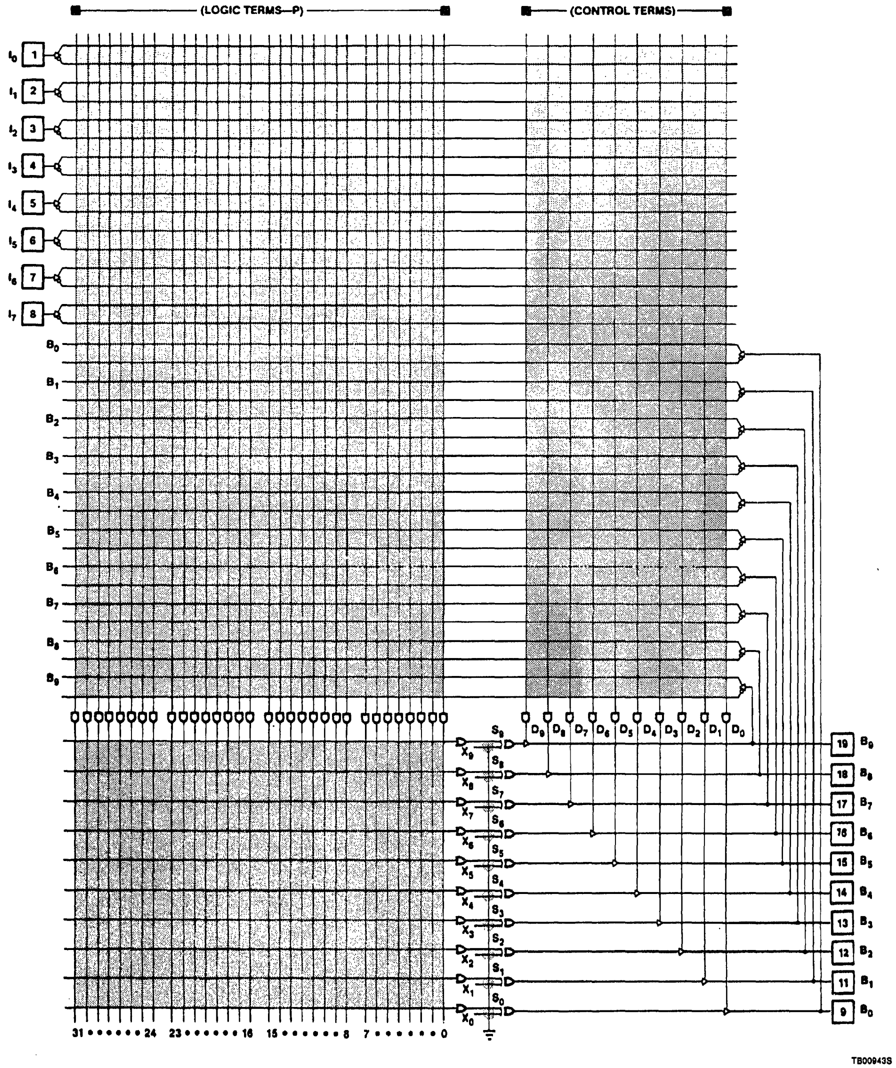
AT OUTPUT POLARITY = L
$Z = \overline{P0 + P1 + P2 +} \ldots$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \ldots$

NOTES:
1. For each of the 10 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



FPLA LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ◎ Programmable connection.

Field-Programmable Logic Array (18 × 42 × 10) PLS153A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLS153AN
20-pin Plastic Leaded Chip Carrier	PLS153AA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[2, 3]	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = Min				
V_{OL}	Low[2, 4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[2, 5]	I_{OH} = -2mA	2.4			V
Input current[10]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		130	155	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

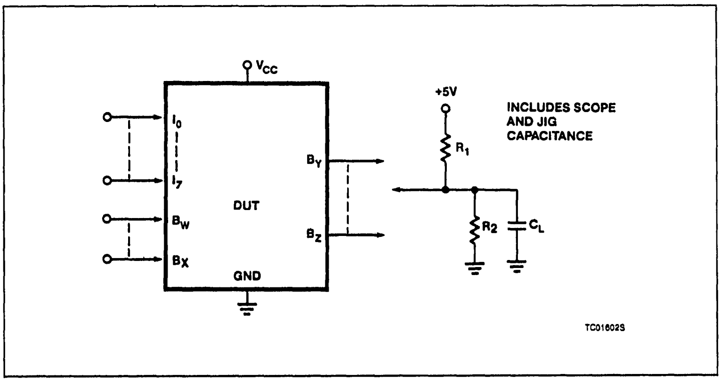
Field-Programmable Logic Array (18 × 42 × 10) PLS153A

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

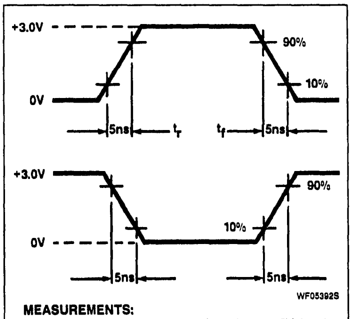
SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[1]	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		20	30	ns
t_{OE}	Output enable	Output ±	Input ±	$C_L = 30pF$		20	30	ns
t_{OD}	Output disable[8]	Output ±	Input ±	$C_L = 5pF$		20	30	ns

NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with +10V applied to I_7.
5. Measured with +10V applied to I_{0-7}. Output sink current is supplied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with $I_{0, 1}$ at 0V and I_{2-7} and B_{0-9} at 4.5V.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IH} and I_{IL} limits are for dedicated inputs only (I_0-I_9).

TEST LOAD CIRCUITS



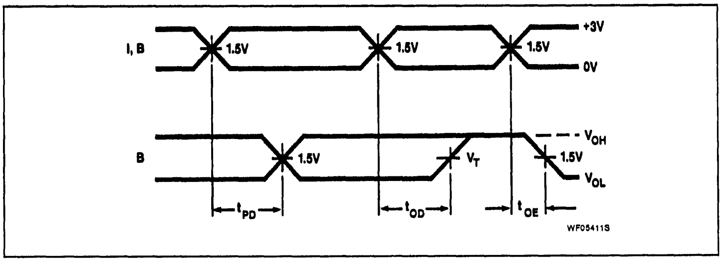
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAM



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

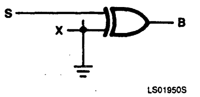
LOGIC PROGRAMMING

PLS153A logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

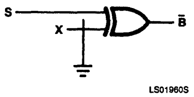
PLS153A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY - (B)

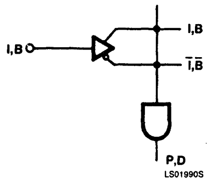


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

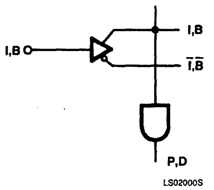


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

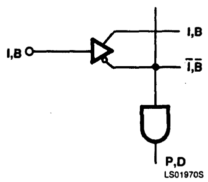
"AND" ARRAY - (I, B)



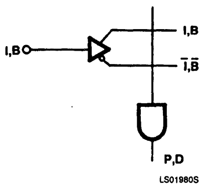
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H

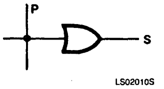


STATE	CODE
$\overline{I}$, $\overline{B}$	L

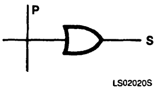


STATE	CODE
DON'T CARE	-

OR ARRAY - (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the True and Complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

CAUTION: PLS153A TEST COLUMNS

The PLS153A incorporates two columns not shown in the logic block diagram. These columns are used for in-house testing of the device in the unprogrammed state. These columns must be disabled prior to using the PLS153A in your application. If you are using a Signetics-approved programmer the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.

Furthermore, because of these test columns, the PLS153A cannot be programmed using the programmer algorithm for the PLS153.

Field-Programmable Logic Array (18 × 42 × 10) PLS153A

FPLA PROGRAM TABLE

CUSTOMER NAME ____

PURCHASE ORDER # ____

SIGNETICS DEVICE # ____ CF (XXXX)

CUSTOMER SYMBOLIZED PART # ____

TOTAL NUMBER OF PARTS ____

PROGRAM TABLE # ____ REV ____ DATE ____

Notes

1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (–).
3. Unused product terms can be left blank.

OR

B(O)	
ACTIVE	A
INACTIVE	•

CONTROL

(POL)	
HIGH	H
LOW	L

AND

I, B(I)	
INACTIVE	0
I, B	H
Ī, B̄	L
DON'T CARE	–

																				POLARITY									
TERM	AND																			OR									
									B(I)											B(O)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0
0																													
1																													
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D6																													
D5																													
D4																													
D3																													
D2																													
D1																													
D0																													
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9
VARIABLE NAME																													

TB00955S

Signetics

PLHS153
Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLHS153 is a high-speed version of the PLS153 and PLS153A FPLAs.

The PLHS153 is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

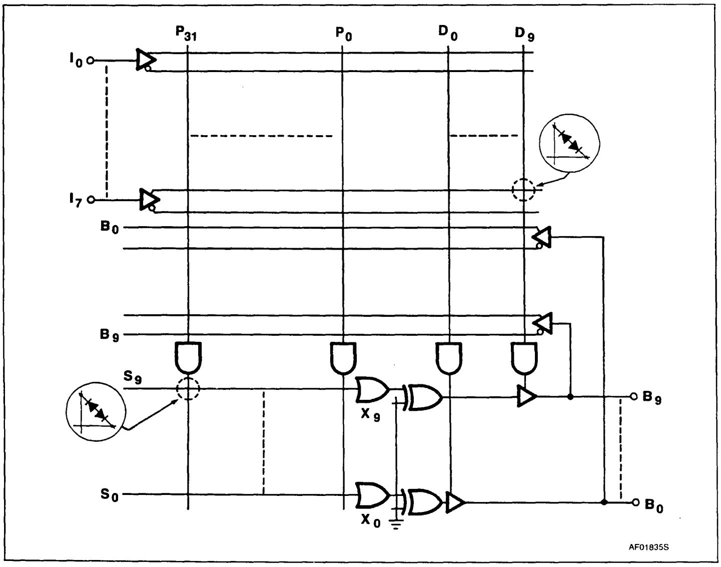
On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

FEATURES

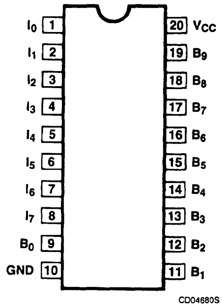
- **Field-Programmable**
- **Functionally identical to PLS153/153A**
- **8 inputs**
- **10 bidirectional I/O lines**
- **42 AND gates**
- **10 OR gates**
- **Programmable output polarity**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 20ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 650mW (typ.)**
- **3-State outputs**
- **TTL compatible**
- **Security fuse**

FUNCTIONAL DIAGRAM



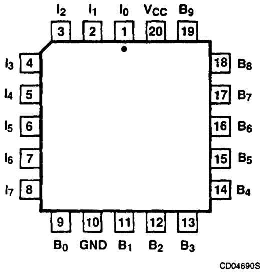
PIN CONFIGURATIONS

N Package



TOP VIEW

A Package

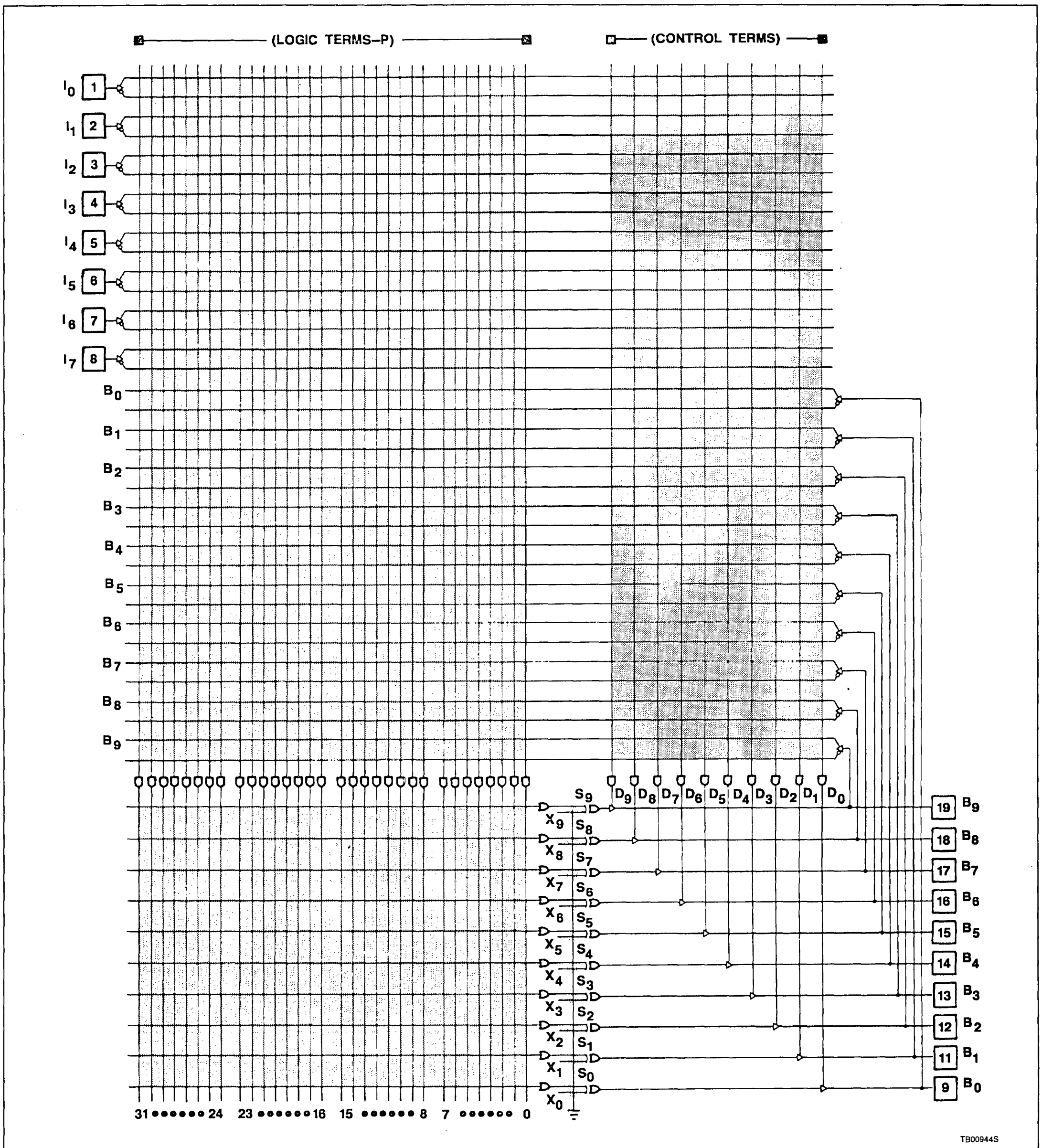


APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

Field-Programmable Logic Array (18 × 42 × 10) PLHS153

FPLA LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. All unprogrammed or virgin "EX-OR" gate locations are pulled to logic "0" .
3. ▨ Programmable connection.

Field-Programmable Logic Array (18 × 42 × 10) PLHS153

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLHS153N
20-pin Plastic Leaded Chip Carrier	PLHS153A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	-30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_A	Operating free-air temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLHS153 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = –2mA	2.4			V
Input current[10]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	µA
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0.5V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		130	155	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

Field-Programmable Logic Array (18 × 42 × 10) PLHS153

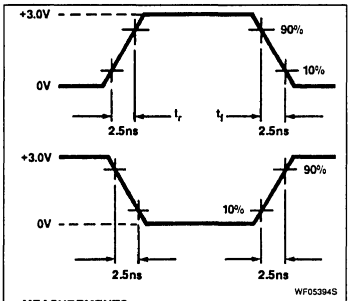
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[1]	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		14	20	ns
t_{OE}	Output enable	Output −	Input ±	$C_L = 30pF$		16	20	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		14	20	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with +10V applied to I_5.
5. Output sink current is supplied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with all pins = open or 4.5V.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IL} and I_{IH} limits are for dedicated inputs only (I_0-I_7).

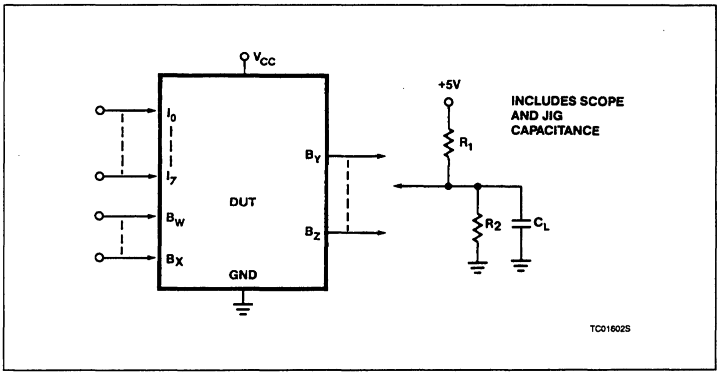
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

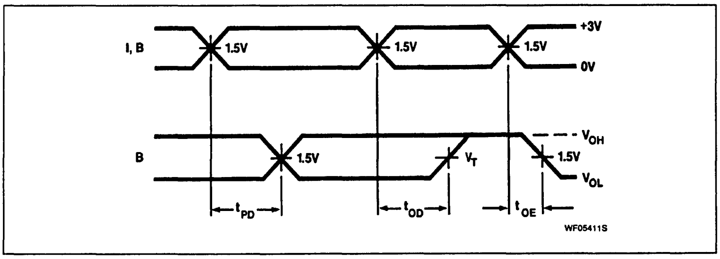
TEST LOAD CIRCUITS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Field-Programmable Logic Array (18 × 42 × 10) PLHS153

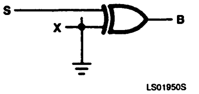
LOGIC PROGRAMMING

PLHS153 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

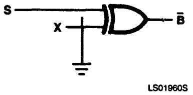
PLHS153 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY - (B)

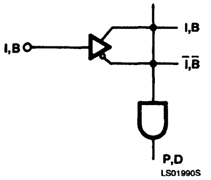


ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H

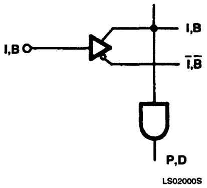


ACTIVE LEVEL	CODE
LOW[1] (INVERTING)	L

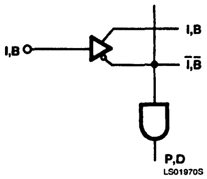
"AND" ARRAY - (I, B)



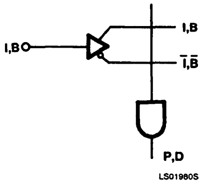
STATE	CODE
INACTIVE[2]	O



STATE	CODE
I, B	H

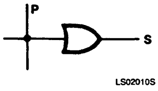


STATE	CODE
$\overline{I}$, $\overline{B}$	L

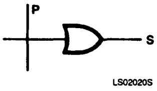


STATE	CODE
DON'T CARE[1]	-

OR ARRAY - (B)



P_n STATUS	CODE
ACTIVE	A



P_n STATUS	CODE
INACTIVE[1]	•

NOTES:

[1] This is the initial unprogrammed state of all links. All unused P_n and D_n terms must be programmed as INACTIVE.

[2] Any gate P_n will be unconditionally inhibited if both the True and Complement of an input (either I or B) are programmed for a connection.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "L" polarity.
2. All P_n terms are enabled in the AND array.
3. All P_n terms are inactive in the OR array.

Field-Programmable Logic Array (18 × 42 × 10) PLHS153

FPLA PROGRAM TABLE

CUSTOMER NAME ____________

PURCHASE ORDER # ____________

SIGNETICS DEVICE # ____________ CF (XXXX)

CUSTOMER SYMBOLIZED PART # ____________

TOTAL NUMBER OF PARTS ____________

PROGRAM TABLE # ________ REV ________ DATE ________

Notes

1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (-) in the virgin state.
3. All P-terms are active until programmed otherwise.
4. Unused product terms must be programmed as INACTIVE.

AND	
INACTIVE	0
I, B	H
Ī, B̄	L
DON'T CARE	–

I, B (I)

OR	
ACTIVE	A
INACTIVE	•

B(O)

CONTROL	
HIGH	H
LOW	L

(POL)

POLARITY

TERM	AND																		OR									
									B(I)										B(O)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
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D4																												
D3																												
D2																												
D1																												
D0																												
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	19	18	17	16	15	14	13	12	11	9
VARIABLE NAME																												

TB00950S

Signetics

PLUS153B

Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLUS153B is a 15ns version of the Signetics PLS153 FPLA architecture. The Signetics state-of-the-art Oxide isolated Bipolar fabrication process is employed to produce performance levels not yet achieved in devices of this complexity.

The PLUS153B is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of Ex-OR gates for implementing AND/OR or AND/NOR logic functions.

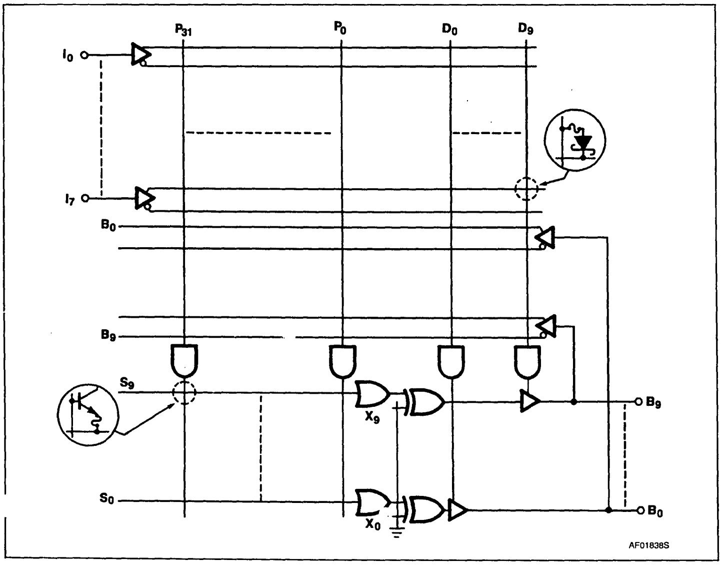
The PLUS153B is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

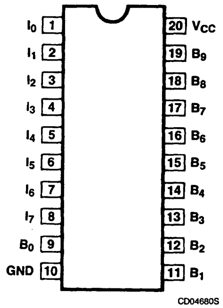
- **Field-Programmable (Ti-W links)**
- **Functionally identical to, and pin-for-pin compatible with, the PLS153/153A, PLHS153, and the PLUS153D**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Programmable output polarity**
  - **active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 15ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **3-State outputs**
- **TTL compatible**
- **Security fuse**

FUNCTIONAL DIAGRAM



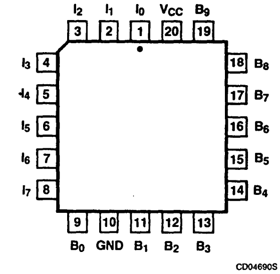
PIN CONFIGURATIONS

N Package



TOP VIEW

A Package

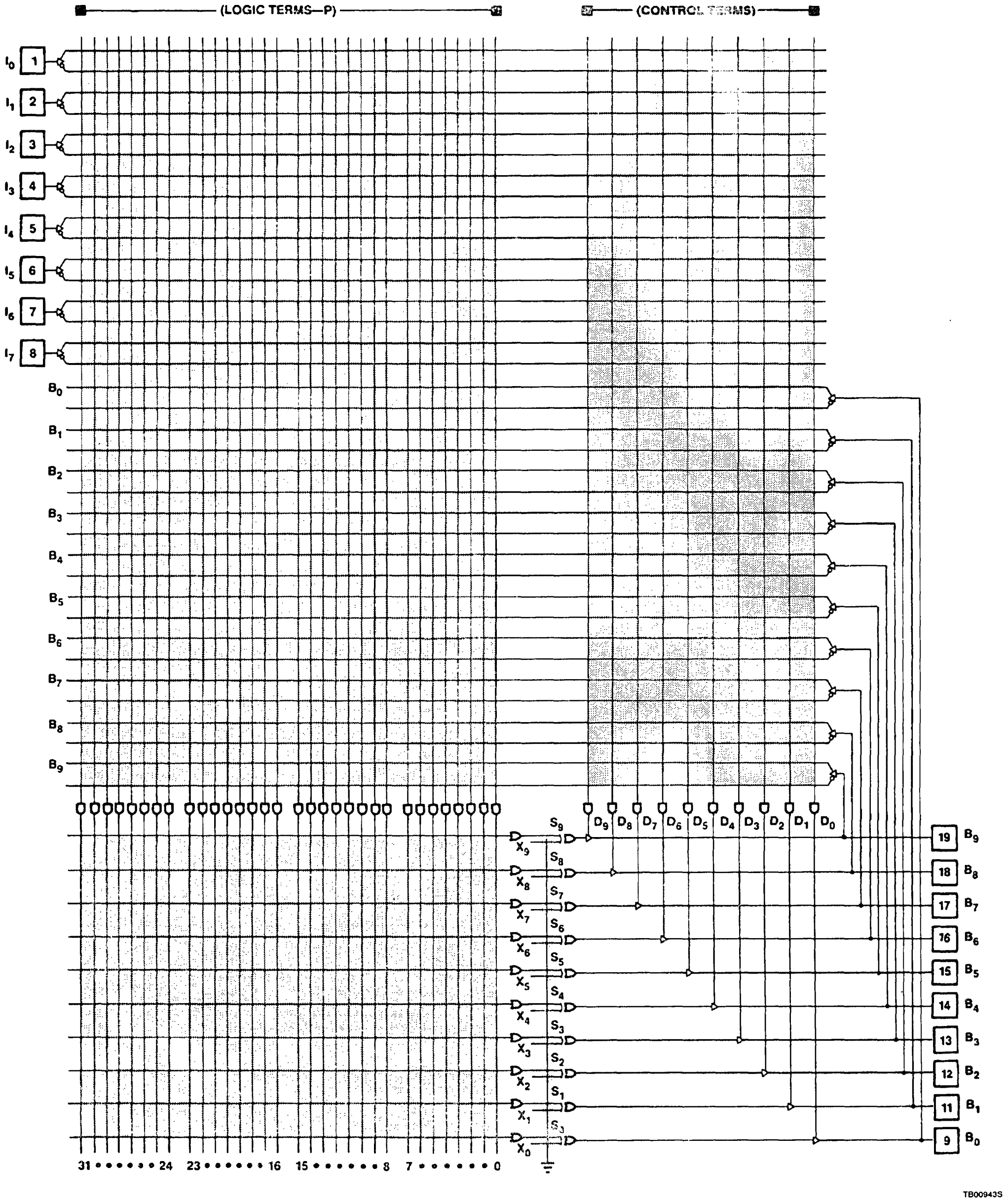


APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

Field-Programmable Logic Array (18 × 42 × 10) PLUS153B

FPLA LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Array (18 × 42 × 10) PLUS153B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLUS153BN
20-pin Plastic Leaded Chip Carrier	PLUS153BA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating free-air temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLUS153B device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage						
		V_{CC} = Min				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = −2mA	2.4			V
Input current[10]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			−100	
I_{IH}	High	V_{IN} = 5.5V			40	μA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	μA
		V_{OUT} = 0.45V			−140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		150	200	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

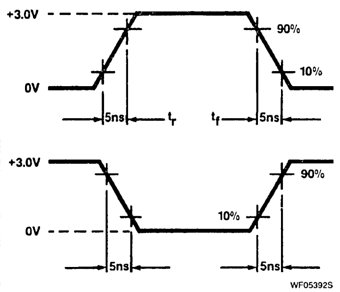
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[1]	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		11	15	ns
t_{OE}	Output enable	Output –	Input ±	$C_L = 30pF$		11	15	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		11	15	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs $I_0–I_2 = 0V$, inputs $I_3–I_5 = 4.5V$, inputs $I_7 = 4.5V$ and $I_6 = 10V$. For outputs $B_0–B_4$ and for outputs $B_5–B_9$ apply the same conditions, except $I_7 = 0V$.
5. Same conditions as Note 5, except $I_7 = +10V$.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs $I_0–I_7$ and $B_0–B_9 = 0V$.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IL} and I_{IH} limits are for dedicated inputs only (I_0-I_7).

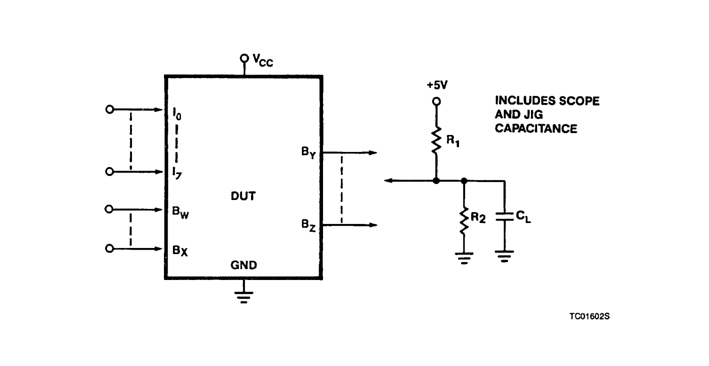
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

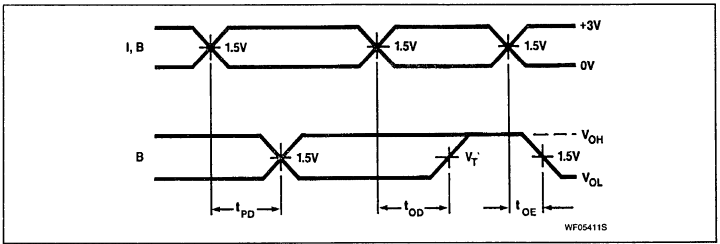
TEST LOAD CIRCUITS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



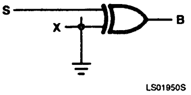
LOGIC PROGRAMMING

PLUS153B logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

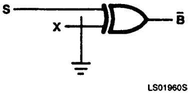
PLUS153B logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (B)

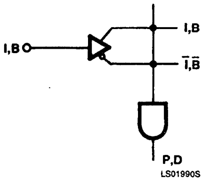


ACTIVE LEVEL	CODE
HIGH^1 (NON-INVERTING)	H

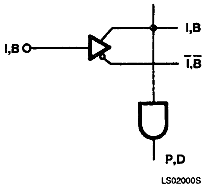


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

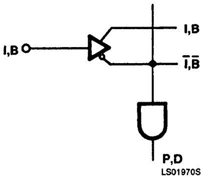
AND ARRAY – (I, B)



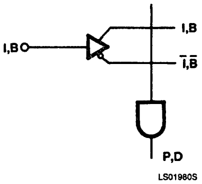
STATE	CODE
INACTIVE^{1,2}	O



STATE	CODE
I, B	H

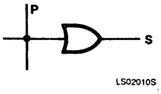


STATE	CODE
$\overline{I}$, $\overline{B}$	L

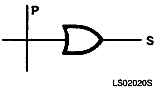


STATE	CODE
DON'T CARE	-

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE^1	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the true and complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

Field-Programmable Logic Array (18 × 42 × 10) PLUS153B

FPLA PROGRAM TABLE

CUSTOMER NAME ________________

PURCHASE ORDER # ________________

SIGNETICS DEVICE # ________ CF (XXXX)

CUSTOMER SYMBOLIZED PART # ________________

TOTAL NUMBER OF PARTS ________________

PROGRAM TABLE # ______ REV ______ DATE ______

Notes

1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (–).
3. Unused product terms can be left blank.

AND

INACTIVE	0	I, B(I)
I, B	H	
Ī, B̄	L	
DON'T CARE	–	

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

																				POLARITY									
TERM	AND																		OR									
	I								B(I)										B(O)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0																												
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D1																												
D0																												
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	19	18	17	16	15	14	13	12	11	9
VARIABLE NAME																												

TB00955S

Signetics

PLUS153D
Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

The PLUS153D is a 12ns version of the Signetics PLS153 FPLA architecture. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce performance levels not yet achieved in devices of this complexity.

The PLUS153D is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of Ex-OR gates for implementing AND/OR or AND/NOR logic functions.

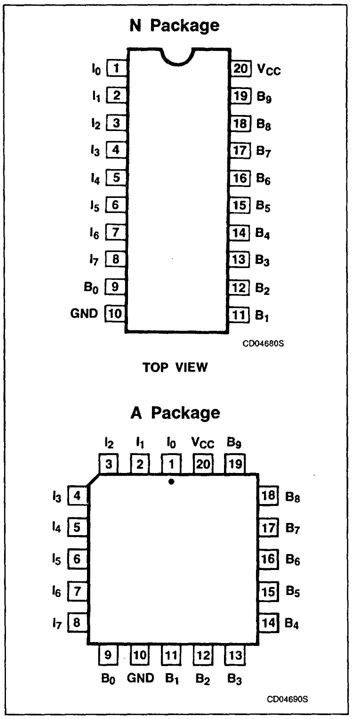
The PLUS153D is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

- **Field-Programmable (Ti-W links)**
- **Functionally identical to, and pin-for-pin compatible with, the PLS153/153A, PLHS153 and PLUS153B**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Programmable output polarity**
  - **active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 12ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **3-State outputs**
- **TTL compatible**
- **Security fuse**

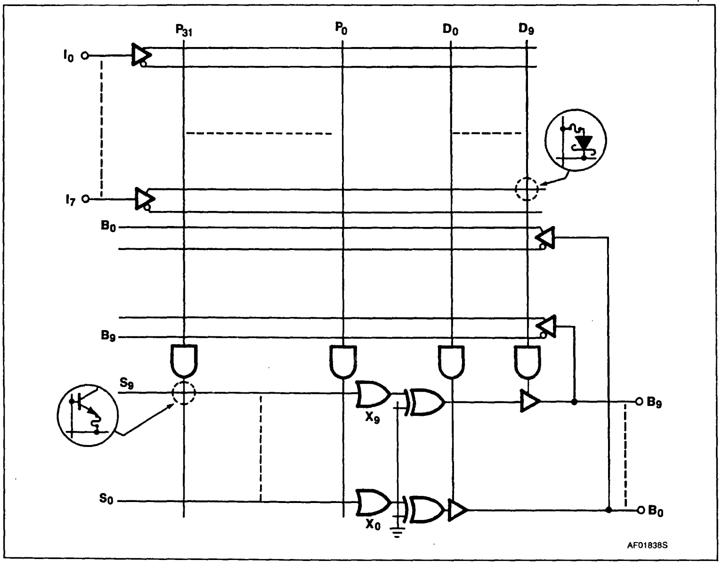
PIN CONFIGURATIONS



APPLICATIONS

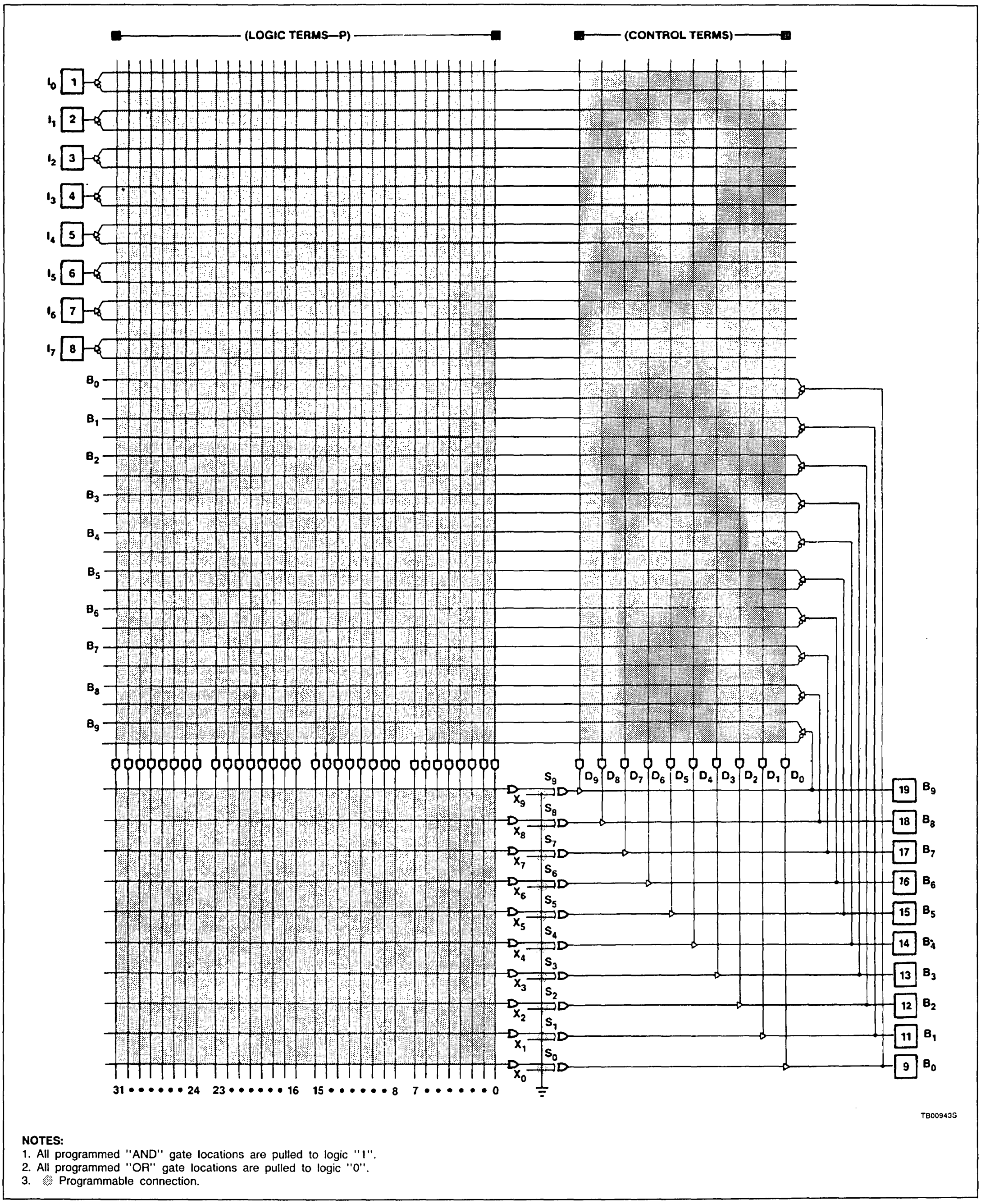
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

FUNCTIONAL DIAGRAM



Field-Programmable Logic Array (18 × 42 × 10) PLUS153D

FPLA LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Array (18 × 42 × 10) PLUS153D

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLUS153DN
20-pin Plastic Leaded Chip Carrier	PLUS153DA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating free-air temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
Input current[11]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		150	200	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

Field-Programmable Logic Array (18 × 42 × 10) PLUS153D

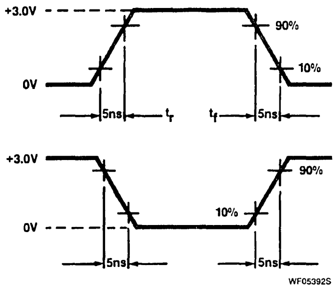
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[1]	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		10	12	ns
t_{OE}	Output enable	Output −	Input ±	$C_L = 30pF$		10	12	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		10	12	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs I_0–I_2 = 0V, inputs I_3–I_5 = 4.5V, inputs I_7 = 4.5V and I_6 = 10V. For outputs B_0–B_4 and for outputs B_5–B_9 apply the same conditions, except I_7 = 0V.
5. Same conditions as Note 5, except $I_7 = +10V$.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs I_0–I_7 and B_0–B_9 = 0V.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IL} and I_{IH} limits are for dedicated inputs only (I_0-I_7).

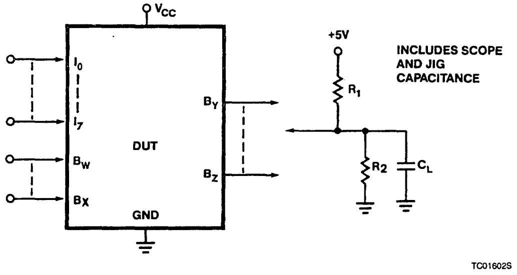
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

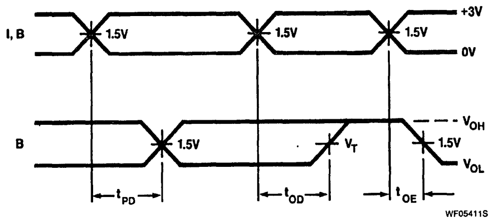
TEST LOAD CIRCUITS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Field-Programmable Logic Array (18 × 42 × 10) PLUS153D

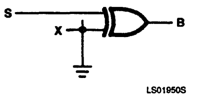
LOGIC PROGRAMMING

PLUS153D logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

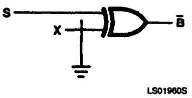
PLUS153D logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY - (B)

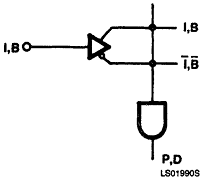


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

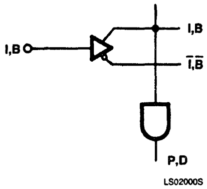


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

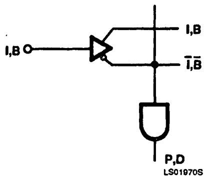
AND ARRAY - (I, B)



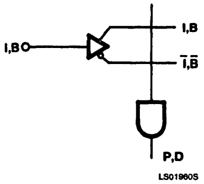
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H

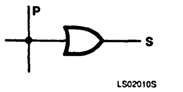


STATE	CODE
$\bar{I}$, $\bar{B}$	L

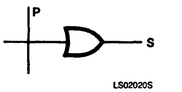


STATE	CODE
DON'T CARE	-

OR ARRAY - (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the true and complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

Field-Programmable Logic Array (18 × 42 × 10) PLUS153D

FPLA PROGRAM TABLE

CUSTOMER NAME ____________
PURCHASE ORDER # ____________
SIGNETICS DEVICE # ____________ CF (XXXX)
CUSTOMER SYMBOLIZED PART # ____________
TOTAL NUMBER OF PARTS ____________
PROGRAM TABLE # ______ REV ______ DATE ______

Notes

1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (–).
3. Unused product terms can be left blank.

OR

B(0)

ACTIVE	A
INACTIVE	•

CONTROL

(POL)

HIGH	H
LOW	L

AND

I, B(I)

INACTIVE	0
I, B	H
$\bar{I}, \bar{B}$	L
DON'T CARE	–

																			POLARITY									
	AND																		OR									
	I								B(I)										B(0)									
TERM	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
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D5																												
D4																												
D3																												
D2																												
D1																												
D0																												
PIN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9	19	18	17	16	15	14	13	12	11	9
VARIABLE NAME																												

TB00955S

Signetics

PLS161
Field-Programmable Logic Array (12 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
● Series 24

DESCRIPTION

The PLS161 is a bipolar, Field-Programmable Logic Array (FPLA). The device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

This device consists of 12 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 12 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-terms will activate an output by disconnecting terms which do not affect the output. In addition each output can be fused as active-High (H) or active-Low (L).

The PLS161 is fully TTL compatible, and includes a chip enable input for output inhibit control and expansion of input variables.

Order codes are listed in the Ordering Information Table.

FEATURES

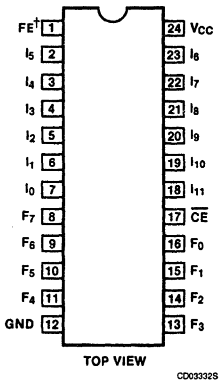
- Field-Programmable (Ni-Cr Link)
- Input variables: 12
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 50ns (max.)
- Power dissipation: 600mW (typ.)
- Input loading: −100µA (max.)
- Chip Enable input
- Output disable function
- Separate I/O architecture
- 3-State outputs

APPLICATIONS

- CRT display systems
- Random logic
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Sequential controllers
- Data security encoders
- Fault detectors
- Frequency synthesizers

PIN CONFIGURATION

N Package



† Fuse Enable Pin: It is recommended that this pin either be left open or tied to ground during normal operation.

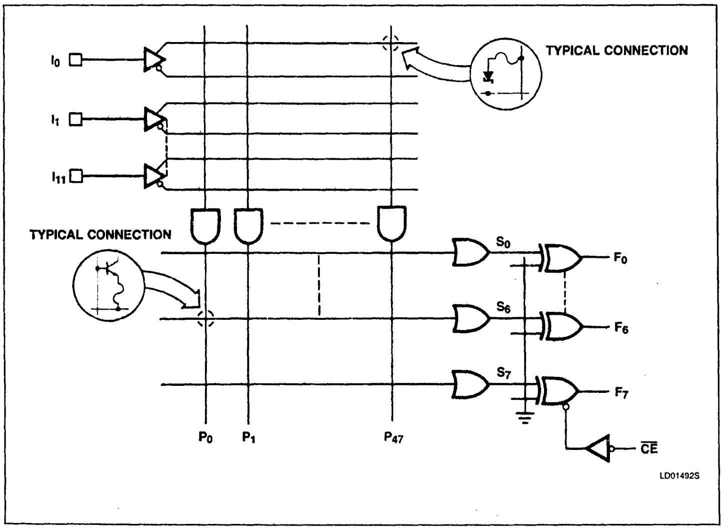
LOGIC FUNCTION

TYPICAL PRODUCT TERM
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{11}}$

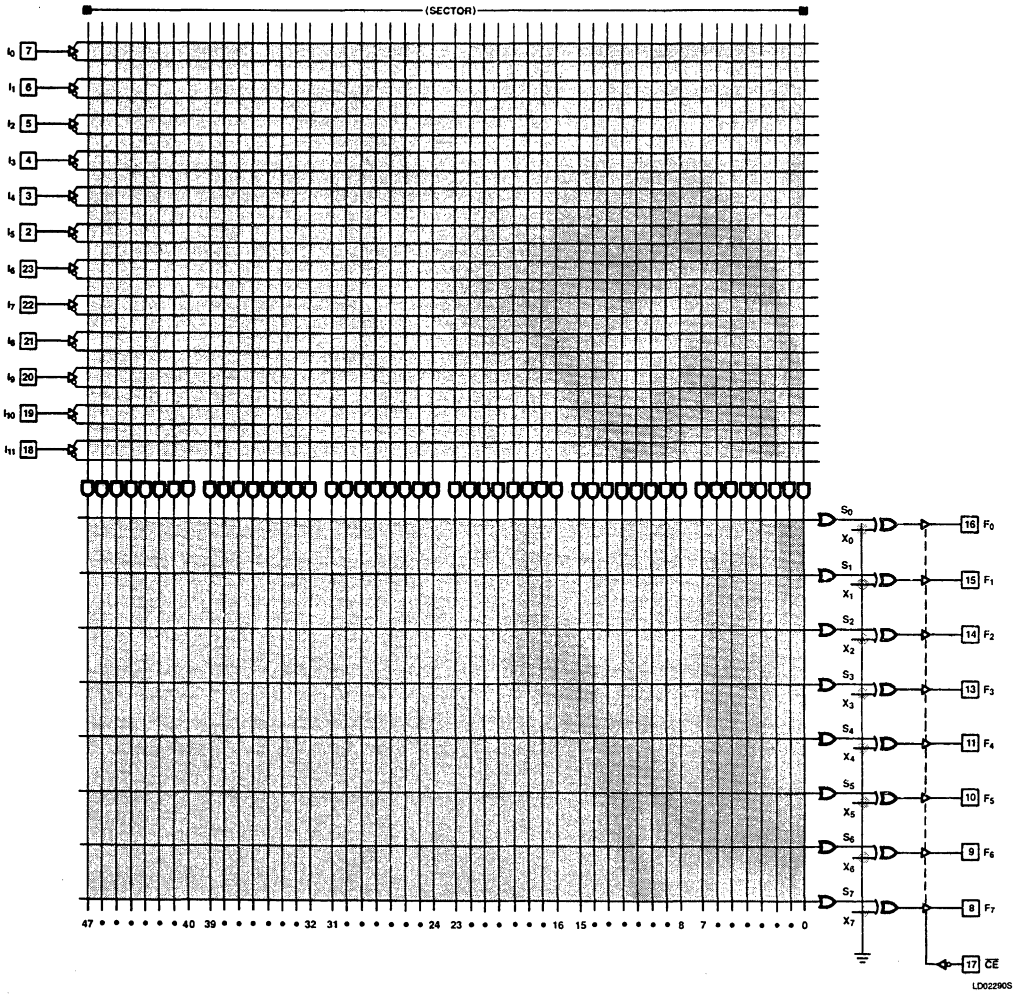
TYPICAL OUTPUT FUNCTIONS:
$@\ \overline{CE} = 0$:
$F_0 = (P_0 + P_1 + P_2)$ @ L = CLOSED
$F_0 = (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ L = OPEN

NOTE:
For each of the 8 outputs either the function F_p (active-High) or $\overline{F_p}$ (active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.

FUNCTIONAL DIAGRAM



FPLA LOGIC DIAGRAM



NOTES:
1. All AND/EX-OR gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown link float to a logic "0".
3. ◎ Programmable connection.

Field-Programmable Logic Array (12 × 48 × 8) PLS161

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS161N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High[4]	I_{OH} = -2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
		V_{CC} = Max				
I_{IH}	High	V_{IN} = 5.5V		< 1	40	µA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100	µA
Output current						
		$\overline{CE}$ = High, V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		-1	-40	
I_{OS}	Short circuit[3, 6]	$\overline{CE}$ = Low, V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		120	170	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2V		8		pF
C_{OUT}	Output	V_{OUT} = 2V		17		pF

Notes on following page.

Field-Programmable Logic Array (12 × 48 × 8) PLS161

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Propagation delay							
t_{PD}	Input	Output	Input		35	50	ns
t_{CE}	Chip enable	Output	Chip enable		15	30	ns
Disable time							
t_{CD}	Chip disable	Output	Chip enable		15	30	ns

NOTES:

1. All values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one pin at a time.
4. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
5. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

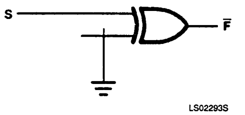
LOGIC PROGRAMMING

PLS161 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

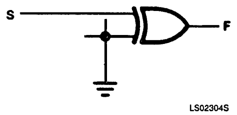
PLS161 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

EX-OR ARRAY – (F)

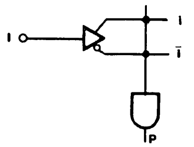


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

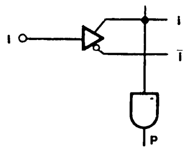


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

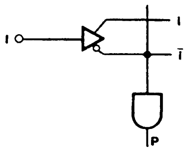
"AND" ARRAY – (I)



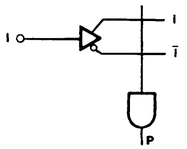
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I	H

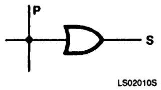


STATE	CODE
Ī	L

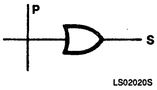


STATE	CODE
DON'T CARE	—

"OR" ARRAY - (F)



P_n STATUS	CODE
ACTIVE	A



P_n STATUS	CODE
INACTIVE	●

NOTES:

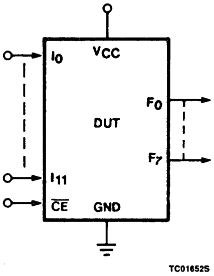
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

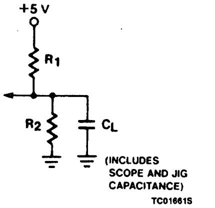
VIRGIN STATE

The PLS161 virgin device is factory shipped in an unprogrammed state, with all fuses intact, such that:

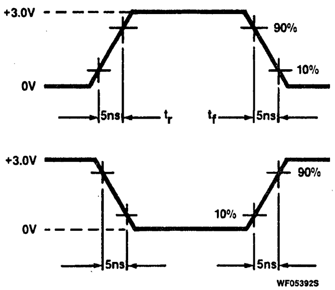
1. All P_n terms are disabled. (Inactive).
2. All P_n terms are active on all outputs.
3. All outputs are active-High.

TEST LOAD CIRCUITS





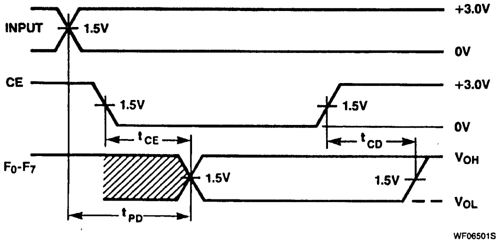
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAM



Read Cycle

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Input valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off state (Hi-Z or High).
t_{PD}	Delay between beginning of valid Input (with Chip Enable Low) and when Data Output becomes valid.

FPLA PROGRAM TABLE

CUSTOMER NAME ______________________

PURCHASE ORDER # ______________________

SIGNETICS DEVICE # ________ CF (XXXX) ________

CUSTOMER SYMBOLIZED PART # ______________________

TOTAL NUMBER OF PARTS ______________________

PROGRAM TABLE # ______________ REV_____ DATE _____

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	$\overline{I_m}$	Don't Care	Prod Term Present in F_p	Prod Term Not Present in F_p	Active High	Active Low
H	L	—(dash)	A	• (period)	H	L
NOTE Enter (-) for unused inputs of used P-terms.			NOTES 1. Entries independent of output polarity. 2. Enter (A) for unused outputs of used P-terms.		NOTES 1. Polarity programmed once only. 2. Enter (H) for all unused outputs.	

VARIABLE NAME	PIN NO.	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	TERM	AND
	18																																																	11	INPUT (I_m)
	19																																																	10	
	20																																																	9	
	21																																																	8	
	22																																																	7	
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	4																																																	3	
	5																																																	2	
	6																																																	1	
	7																																																	0	

																																																			OR	POLARITY
	8																																																	7	OUTPUT (F_P)
	9																																																	6	
	10																																																	5	
	11																																																	4	
	13																																																	3	
	14																																																	2	
	15																																																	1	
	16																																																	0	

TB01540S

Signetics

PLS162

Field-Programmable Address Decoder (16 × 5)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLS162 is a bipolar, Field-Programmable Address Decoder. The device consists of five AND/NAND gates which share 16 common inputs. The type of gate is selected by programming the output as active-High (H) or active-Low (L). Each of the 16 inputs $I_0 - I_{15}$ can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the five AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS162 includes chip-enable control for output strobing and inhibit. It features 3-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

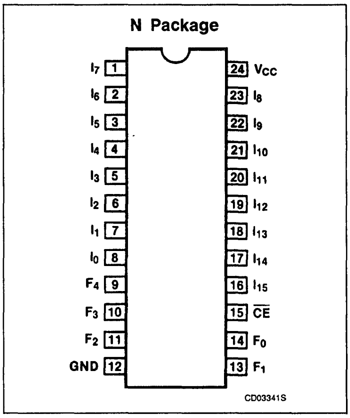
FEATURES

- **Field-Programmable (Ni-Cr link)**
- **16 input variables**
- **5 output functions**
- **Chip Enable input**
- **I/O propagation delay: 30ns (max.)**
- **Power dissipation: 500mW (typ.)**
- **Input loading: $-100\mu A$ (max.)**
- **3-State outputs**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION



LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:
ACTIVE-HIGH

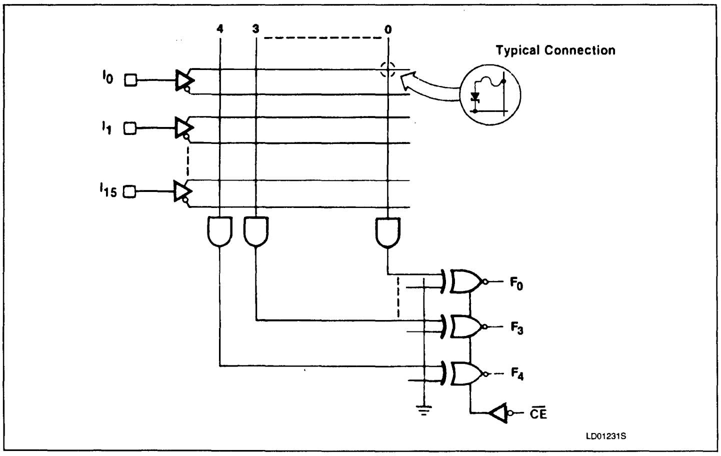
$X = A \cdot \overline{B} \cdot C \cdot \ldots$

ACTIVE-LOW

$X = \overline{A \cdot \overline{B} \cdot C \cdot \ldots}$
$X = \overline{A} + B + \overline{C} + \ldots$

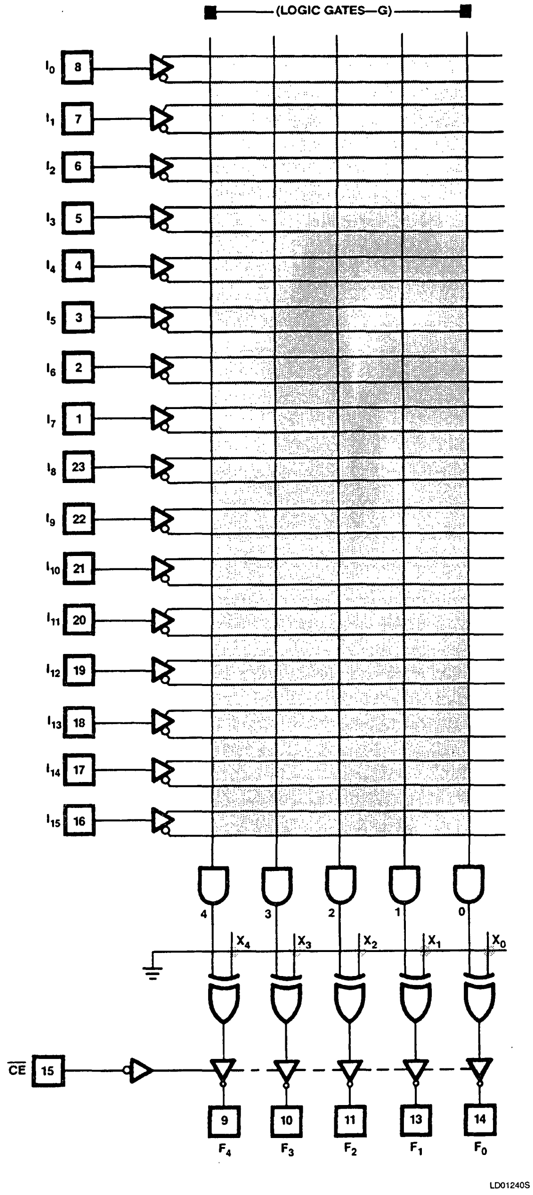
NOTES:
1. For each of the 5 outputs, either function X (active-High) or $\overline{X}$ (active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (F).

FUNCTIONAL DIAGRAM



Field-Programmable Address Decoder (16 × 5) PLS162

FPAD LOGIC DIAGRAM



NOTE:
1. All gate inputs with a blown link float to a logic "1".
2. ▨ Programmable connection.

Field-Programmable Address Decoder (16 × 5) PLS162

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS162N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temporature range	−65 to +150	°C

NOTE:

1. Stresses above those listed may causo malfunction or permanent damage to the device. This is a stress rating only. Functional operation at thoso or any other conditions above those indicated in the operational and programming specification of tho dovico is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[2]	Max	
Input voltage[1]						
V_{IH} V_{IL} V_{IC}	High Low Clamp[3]	V_{CC} = Max V_{CC} = Min V_{CC} = Min, I_{IN} = −12mA	2.0	 −0.8	 0.8 −1.2	V V V
Output voltage[1]						
 V_{OH} V_{OL}	 High[5] Low[4]	V_{CC} = Min I_{OH} = −2mA I_{OL} = 15mA	 2.4	 0.35	 0.5	 V V
Input current						
 I_{IH} I_{IL}	 High Low	V_{CC} = Max V_{IN} = 5.5V V_{IN} = 0.45V		 <1 −10	 40 −100	 μA μA
Output current						
 $I_{O\ (OFF)}$ I_{OS}	 Hi-Z state[6] Short circuit[3, 7]	V_{CC} = Max V_{OUT} = 5.5V V_{OUT} = 0.45V V_{OUT} = 0V	 −15	 1 −1	 40 −40 −70	 μA mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		100	155	mA
Capacitance						
 C_{IN} C_{OUT}	 Input Output[6]	V_{CC} = 5.0V V_{IN} = 2.0V V_{OUT} = 2.0V		 8 15		 pF pF

Notes on following page.

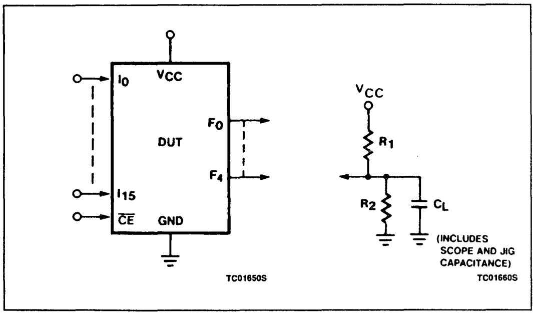
AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[1]	Max	
t_{PD}	Propagation delay	Output	Input	$C_L = 30pF$		20	30	ns
t_{CE}	Chip enable	Output	Chip enable	$C_L = 30pF$		20	30	ns
t_{CD}	Chip disable	Output	Chip enable	$C_L = 5pF$		20	30	ns

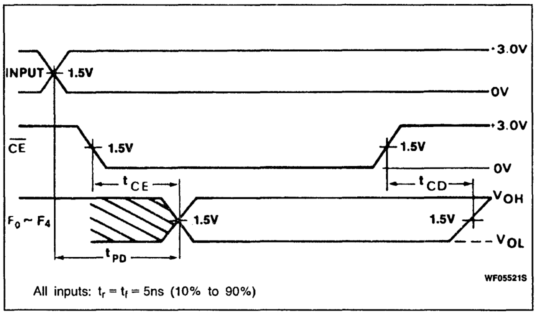
NOTES:

1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. Test each pin one at a time.
4. Measure with a programmed logic condition for which the output under test is at low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the outputs open.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

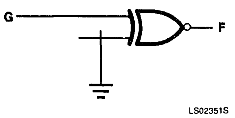
LOGIC PROGRAMMING

PLS162 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

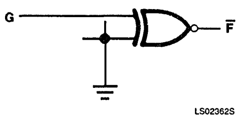
PLS162 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (F)

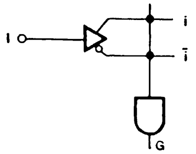


ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H

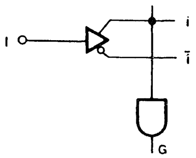


ACTIVE LEVEL	CODE
LOW[1] (INVERTING)	L

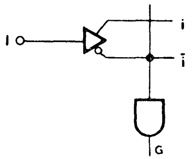
"AND" ARRAY – (I)



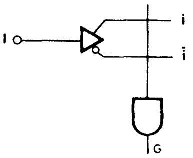
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I	H



STATE	CODE
I	L



STATE	CODE
DON'T CARE	—

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate G_n will be unconditionally inhibited if both the True and Complement of any input (either I or B) are left intact.

VIRGIN DEVICE

The PLS162 is shipped in an unprogrammed state, in which:

1. All P_n terms are disabled. (Inactive).
2. All P_n terms are active on all outputs.
3. All outputs are active-Low.

FPAD PROGRAM TABLE

CUSTOMER NAME ______________	*THIS PORTION TO BE COMPLETED BY SIGNETICS*
PURCHASE ORDER # ______________	*CF (XXXX)* ______________
SIGNETICS DEVICE # ______________	*CUSTOMER SYMBOLIZED PART #* ______________
TOTAL NUMBER OF PARTS ______________	*DATE RECEIVED* ______________
PROGRAM TABLE # ______________	*COMMENTS* ______________

F_0 (14) ______________ = ______________

F_1 (13) ______________ = ______________

F_2 (11) ______________ = ______________

F_3 (10) ______________ = ______________

F_4 (9) ______________ = ______________

GATE		**INPUT**															
POLARITY		I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
F_0																	
F_1																	
F_2																	
F_3																	
F_4																	
PIN NO.		16	17	18	19	20	21	22	23	1	2	3	4	5	6	7	8
VARIABLE NAME																	

NOTES
1. The FPAD is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I bits are normally programmed Don't Care (—).
3. Unused Gates can be left blank.

PROGRAM TABLE ENTRIES

AND	
INACTIVE	0
I	H
$\bar{I}$	L
Don't Care	—

(I)

CONTROL	
HIGH	H
LOW	L

(POL.)

TB01281S

4

Signetics

PLS163

Field-Programmable Address Decoder (12 × 9)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLS163 is a bipolar, Field-Programmable Address Decoder. The device consists of nine AND/NAND gates which share 12 common inputs. The type of gate is selected by programming the output as active-High (H) or active-Low (L). Each of the 12 inputs $I_0 - I_{11}$ can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the nine AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS163 includes chip-enable control for output strobing and inhibit. It features 3-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

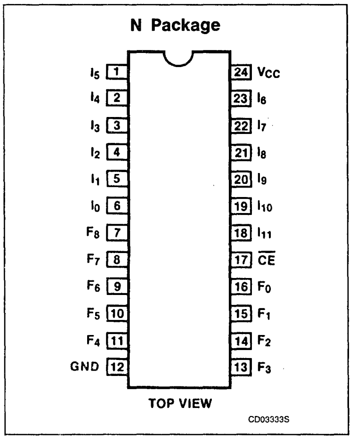
FEATURES

- **Field-Programmable (Ni-Cr link)**
- **12 input variables**
- **9 output functions**
- **Chip Enable input**
- **I/O propagation delay: 30ns (max.)**
- **Power dissipation: 600mW (typ.)**
- **Input loading: −100μA (max.)**
- **3-State outputs**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

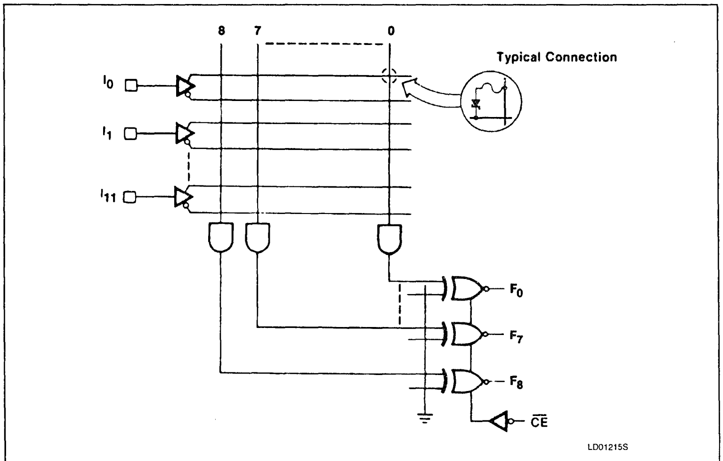
APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$X = A \cdot \overline{B} \cdot C \cdot \; . . .$

ACTIVE-LOW

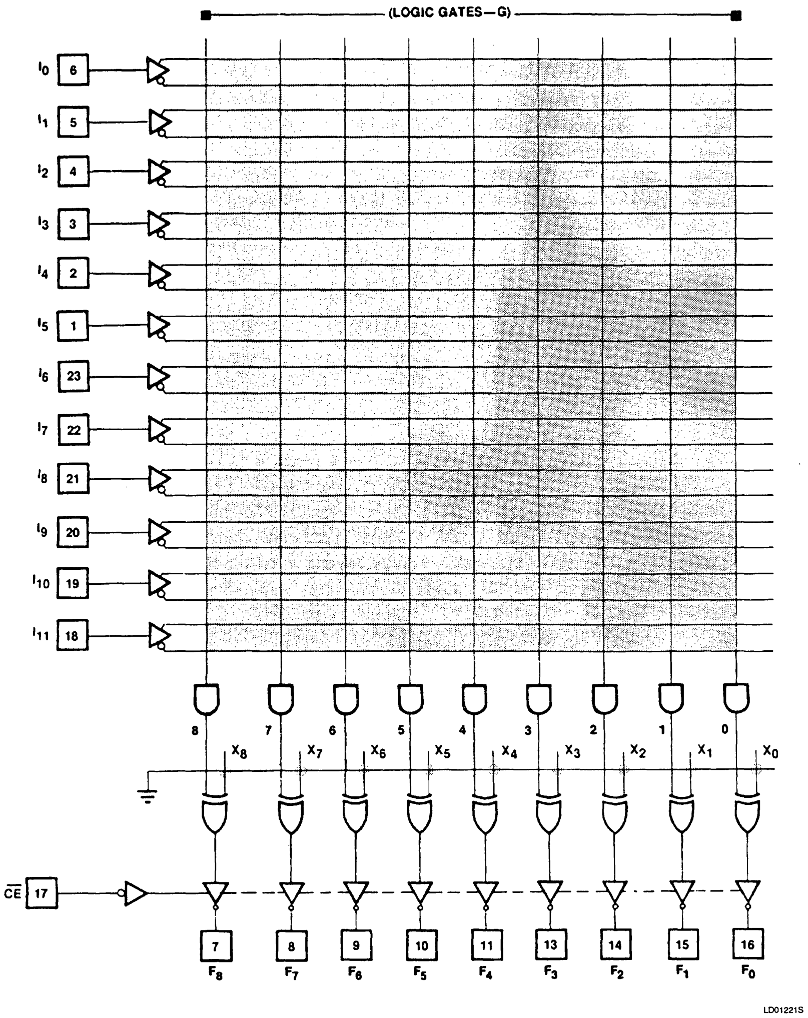
$X = \overline{A \cdot \overline{B} \cdot C \cdot} \; . . .$
$X = \overline{A} + B + \overline{C} + \; . . .$

NOTES:

1. For each of the 9 outputs, either function X (active-High) or $\overline{X}$ (active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (F).

Field-Programmable Address Decoder (12 × 9) PLS163

FPAD LOGIC DIAGRAM



NOTES:
1. All gate inputs with a blown link float to a logic "1".
2. ⁘ Programmable connection.

Field-Programmable Address Decoder (12 × 9) PLS163

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS163N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[2]	Max	
Input voltage						
V_{IH}	High[1]	V_{CC} = Max	2.0			V
V_{IL}	Low[1]	V_{CC} = Min			0.8	V
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage						
		V_{CC} = Min				
V_{OH}	High[1,5]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[1,4]	I_{OL} = 15mA		0.35	0.5	V
Input current						
		V_{CC} = Max				
I_{IH}	High	V_{IN} = 5.5V		< 1	40	µA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100	µA
Output current						
		V_{CC} = Max				
$I_{O\ (OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		-1	-40	µA
I_{OS}	Short circuit[3,7]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	155	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15		pF

Notes on following page.

AC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

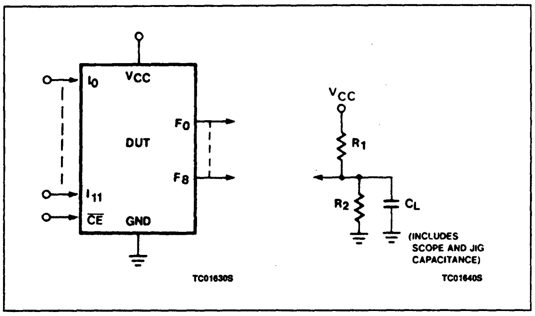
SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[2]	Max	
t_{PD}	Propagation delay	Output	Input	$C_L = 30pF$		20	30	ns
t_{CE}	Chip enable	Output	Chip enable	$C_L = 30pF$		20	30	ns
t_{CD}	Chip disable	Output	Chip enable	$C_L = 5pF$		20	30	ns

NOTES:

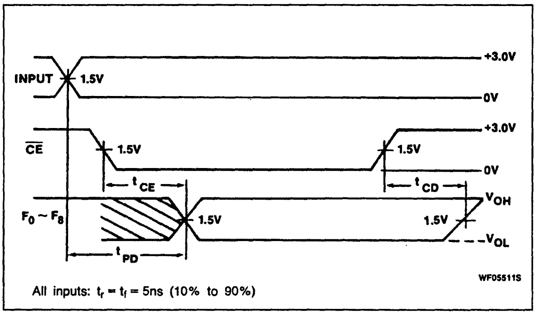
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. Test each pin one at a time.
4. Measure with a programmed logic condition for which the output under test is at low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the outputs open.

4

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

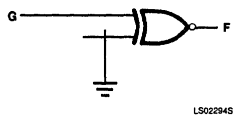
LOGIC PROGRAMMING

PLS163 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

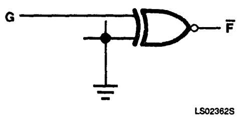
PLS163 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY - (F)

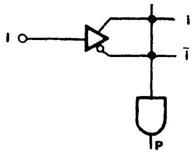


ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H

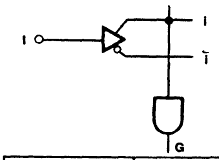


ACTIVE LEVEL	CODE
LOW[1] (INVERTING)	L

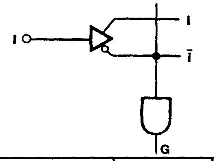
"AND" ARRAY - (I)



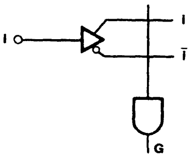
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I	H



STATE	CODE
Ī	L



STATE	CODE
DON'T CARE	—

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate G_n will be unconditionally inhibited if both the True and Complement fuses of any input (I) are left intact.

VIRGIN DEVICE

The PLS163 is shipped in an unprogrammed state, in which:

1. All P_n terms are disabled. (Inactive).
2. All P_n terms are active on all outputs.
3. All outputs are active-Low.

Field-Programmable Address Decoder (12 × 9) PLS163

FPAD PROGRAM TABLE

CUSTOMER NAME ____________________

PURCHASE ORDER # ____________________

SIGNETICS DEVICE # ____________________

TOTAL NUMBER OF PARTS ____________________

PROGRAM TABLE # ____________________

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) ____________________

CUSTOMER SYMBOLIZED PART # ____________________

DATE RECEIVED ____________________

COMMENTS ____________________

F_0 (16) __________ = ____________________

F_1 (15) __________ = ____________________

F_2 (14) __________ = ____________________

F_3 (13) __________ = ____________________

F_4 (11) __________ = ____________________

F_5 (10) __________ = ____________________

F_6 (9) __________ = ____________________

F_7 (8) __________ = ____________________

F_8 (7) __________ = ____________________

GATE		INPUT											
POLARITY		I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
F_0													
F_1													
F_2													
F_3													
F_4													
F_5													
F_6													
F_7													
F_8													
PIN NO.		18	19	20	21	22	23	1	2	3	4	5	6
VARIABLE NAME													

NOTES
1. The FPAD is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I bits are normally programmed Don't Care (—).
3. Unused Gates can be left blank.

PROGRAM TABLE ENTRIES

AND		CONTROL	
INACTIVE	0	HIGH	H
I	H	LOW	L
$\overline{I}$	L		
Don't Care	—		
(I)		(POL.)	

TB01271S

Signetics

PLS173
Field-Programmable Logic Array (22 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

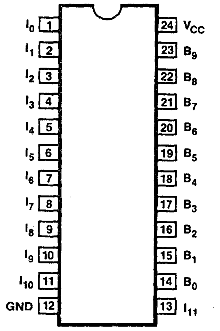
- **Field-Programmable (Ni-Cr links)**
- **12 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 30ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **3-State outputs**
- **TTL compatible**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

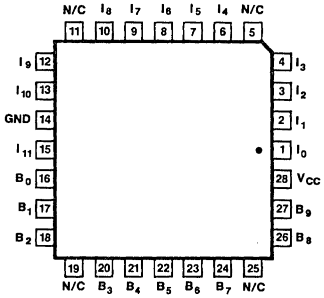
PIN CONFIGURATIONS

N Package



CD03293S

A Package



CD03390S

LOGIC FUNCTION

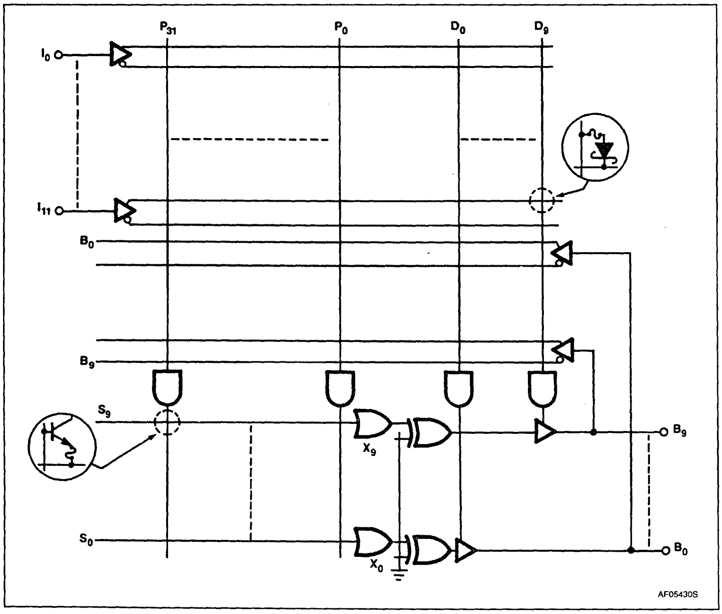
TYPICAL PRODUCT TERM:
Pn = A·$\overline{B}$·C·D· . . .

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
Z = P0 + P1 + P2 . . .

AT OUTPUT POLARITY = L
Z = $\overline{P0 + P1 + P2 +}$ . . .
Z = $\overline{P0}$·$\overline{P1}$·$\overline{P2}$· . . .

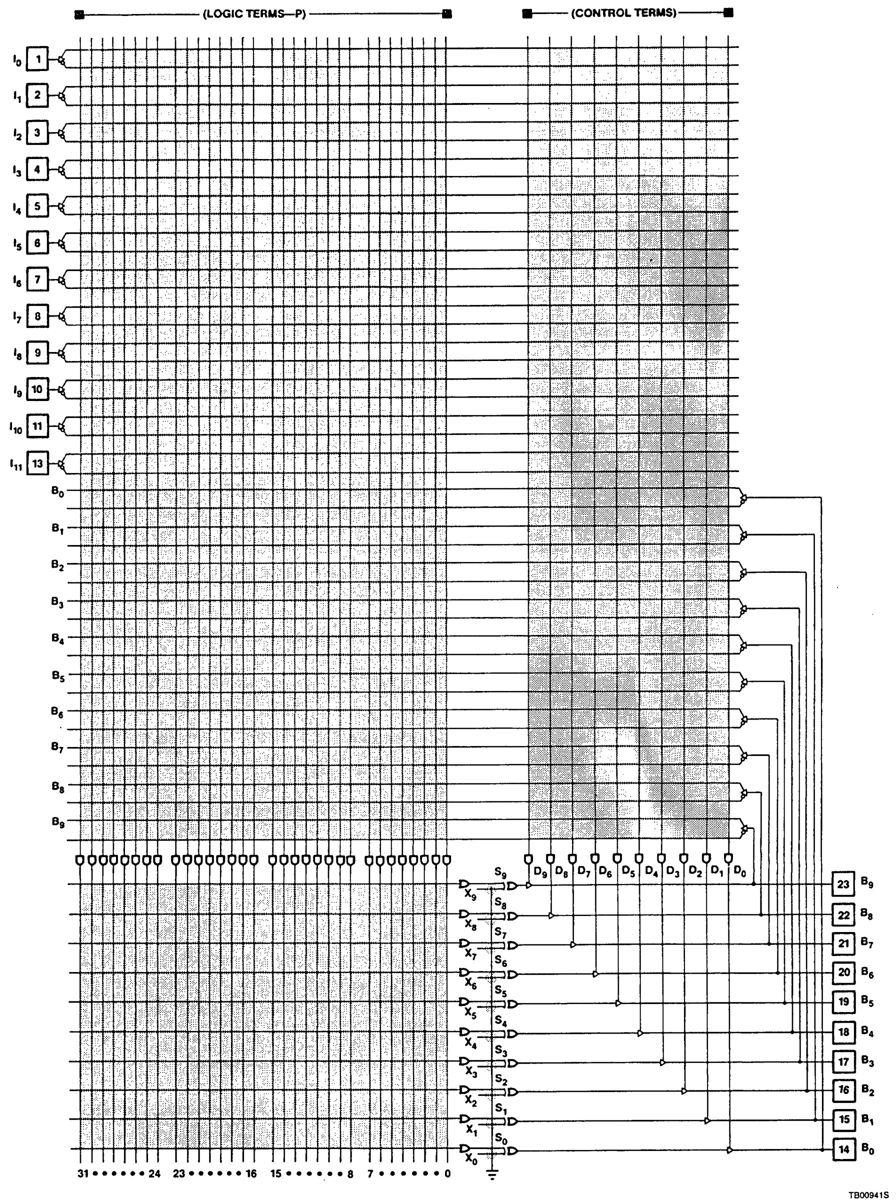
NOTES:
1. For each of the 10 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I), and bidirectional pins (B).

FUNCTIONAL DIAGRAM



Field-Programmable Logic Array (22 × 42 × 10) PLS173

FPLA LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Array (22 × 42 × 10) PLS173

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS173N
28-pin Plastic Leaded Chip Carrier	PLS173A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0^\circ C \leqslant T_A \leqslant +75^\circ C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[2, 3]	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = Min				
V_{OL}	Low[2, 4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[2, 5]	I_{OH} = -2mA	2.4			V
Input current[10]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		150	170	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notos on following page.

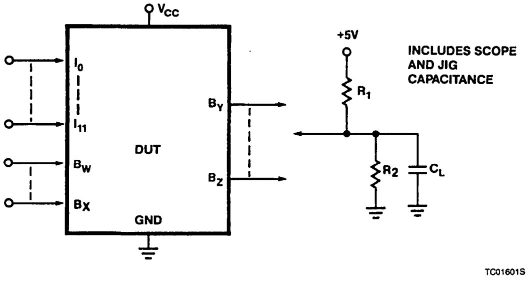
AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		20	30	ns
t_{OE}	Output enable	Output –	Input ±	$C_L = 30pf$		20	30	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		20	30	ns

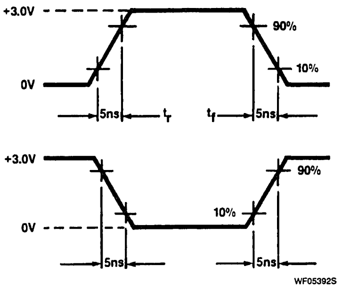
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to I_{11}. Pins 1 – 5 = 0V, Pins 6 – 10 = 4.5V, Pin 11 = 0V and Pin 13 = 10V.
5. Same conditions as Note 5 except Pin 11 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with I_0 and I_1 = 0V and $I_2 - I_{11}$ and $B_0 - B_9$ = 4.5V. Part in Virgin State.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 - I_{11}$).

TEST LOAD CIRCUITS



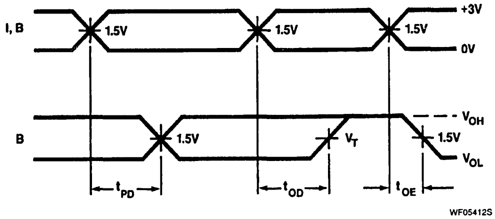
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAM



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

Field-Programmable Logic Array (22 × 42 × 10) PLS173

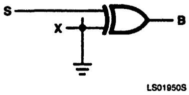
LOGIC PROGRAMMING

PLS173 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

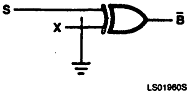
PLS173 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY - (B)

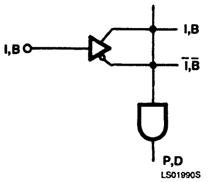


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

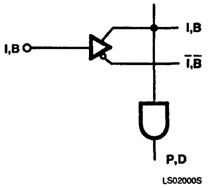


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

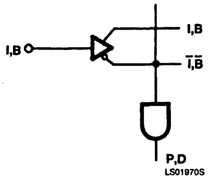
"AND" ARRAY - (I, B)



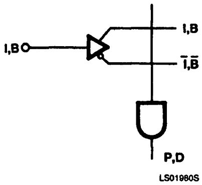
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H

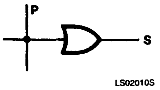


STATE	CODE
$\overline{I}$, $\overline{B}$	L

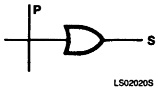


STATE	CODE
DON'T CARE	-

OR ARRAY - (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the True and Complement of any input (I, B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

Field-Programmable Logic Array (22 × 42 × 10) PLS173

FPLA PROGRAM TABLE

CUSTOMER NAME ____________

SIGNETICS DEVICE # ____________

PROGRAM TABLE # ______ REV______ DATE______

Notes

1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (–).
3. Unused product terms can be left blank.

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

AND

INACTIVE	0	I, B (I)
I, B	H	
$\bar{I}$, $\bar{B}$	L	
DON'T CARE	–	

																								POLARITY									
TERM	AND																							OR									
													B(I)											B(O)									
	11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0
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PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14		23	22	21	20	19	18	17	16	15	14
VARIABLE NAME																																	

TB00956S

Signetics

PLUS173B
Field-Programmable Logic Array (22 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLUS173B is a 15ns version of the PLS173 FPLA architecture. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce performance levels not yet achieved in devices of this complexity.

The PLUS173B is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

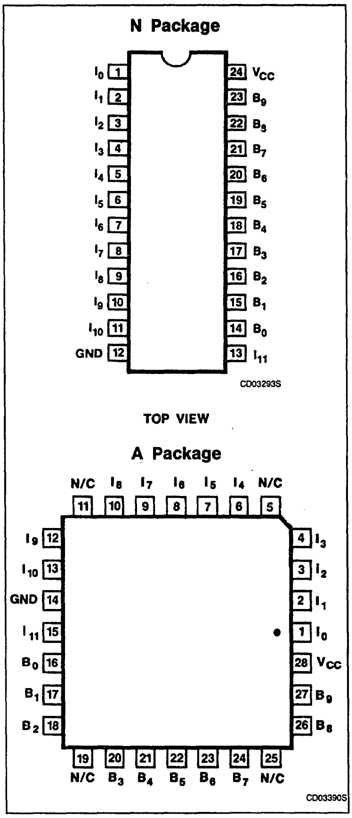
On chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of Ex-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLUS173B is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

FEATURES

- **Field-Programmable (Ti-W links)**
- **Functionally identical to, and pin-for-pin compatible with, the PLS173 and the PLUS173D**
- **12 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Programmable output polarity**
  - **active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 15ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **3-State outputs**
- **TTL compatible**
- **Security fuse**

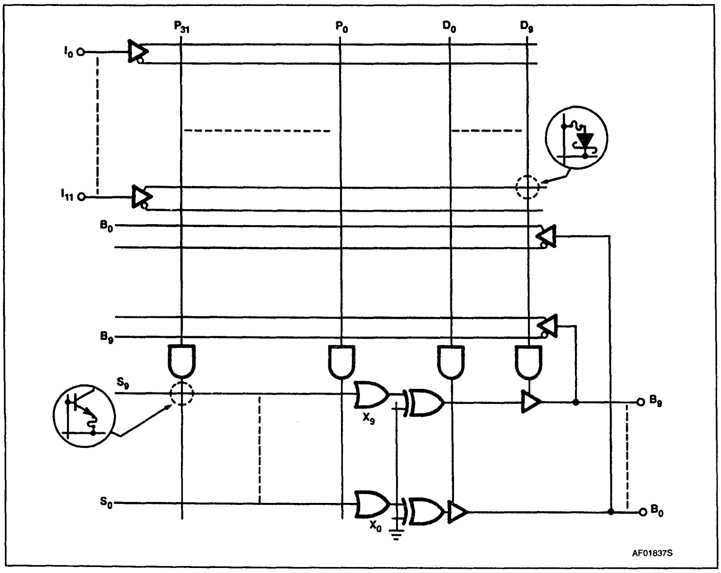
PIN CONFIGURATIONS



APPLICATIONS

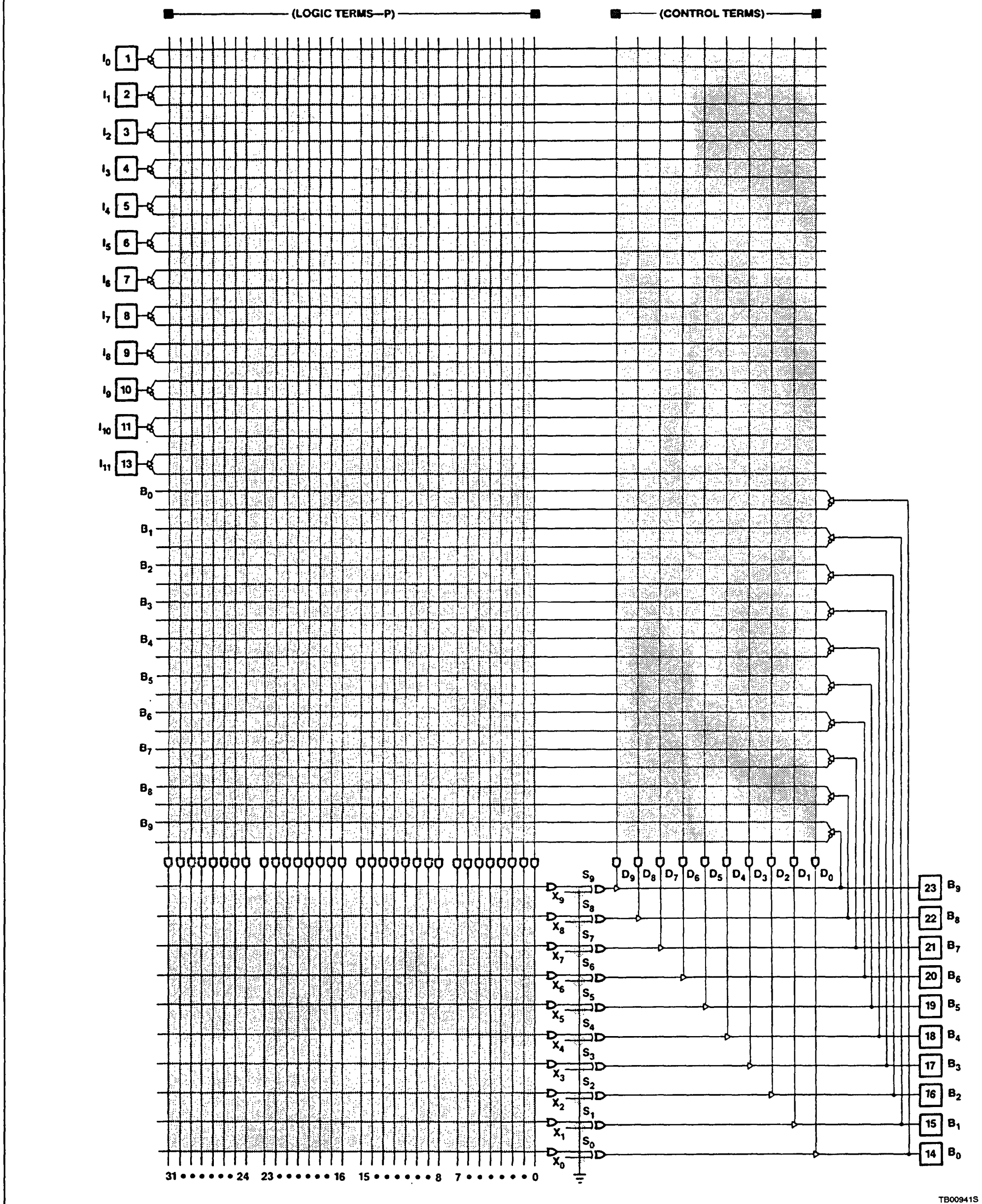
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

FUNCTIONAL DIAGRAM



Field-Programmable Logic Array (22 × 42 × 10) PLUS173B

FPLA LOGIC DIAGRAM



NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Array (22 × 42 × 10) PLUS173B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLUS173BN
28-pin Plastic Leaded Chip Carrier	PLUS173BA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating free-air temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLUS173B device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
Input current[10]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		150	200	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

Field-Programmable Logic Array (22 × 42 × 10) PLUS173B

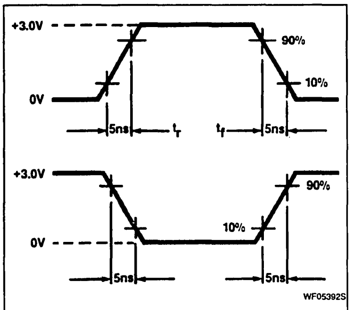
AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		11	15	ns
t_{OE}	Output enable	Output −	Input ±	$C_L = 30pF$		11	15	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		11	15	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs $I_0 - I_4 = 0V$, inputs $I_5 - I_9 = 4.5V$, $I_{11} = 4.5V$ and $I_{10} = 10V$. For outputs $B_0 - B_4$ and for outputs $B_5 - B_9$ apply the same conditions except $I_{11} = 0V$.
5. Same conditions as Note 4 except input $I_{11} = +10V$.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs $I_0 - I_{11}$ and $B_0 - B_9 = 0V$. Part in Virgin State.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 - I_{11}$).

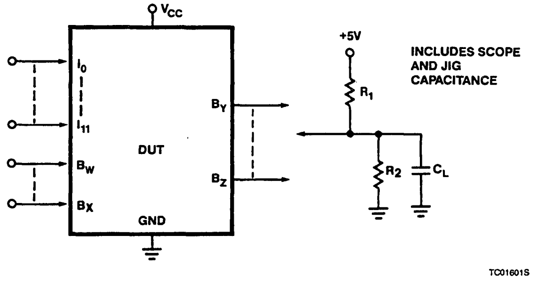
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

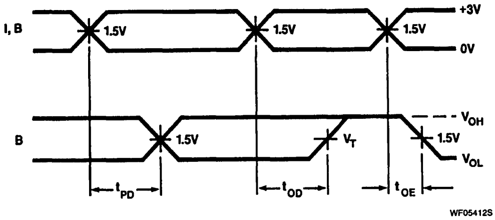
TEST LOAD CIRCUITS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Field-Programmable Logic Array (22 × 42 × 10) PLUS173B

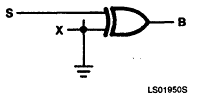
LOGIC PROGRAMMING

PLUS173B logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

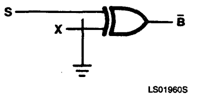
PLUS173B logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (B)

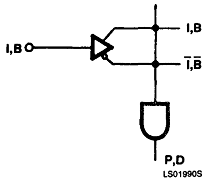


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

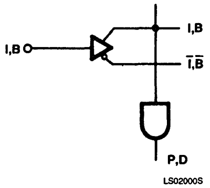


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

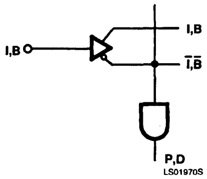
AND ARRAY – (I, B)



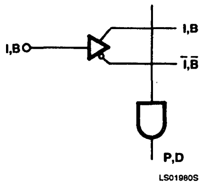
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H

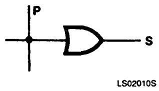


STATE	CODE
Ī, B̄	L

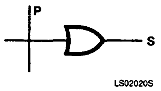


STATE	CODE
DON'T CARE	-

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the True and Complement of any input (I, B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

Field-Programmable Logic Array (22 × 42 × 10) PLUS173B

FPLA PROGRAM TABLE

CUSTOMER NAME ______________________

SIGNETICS DEVICE # ______________________

PROGRAM TABLE # ______ REV______ DATE ______

Notes
1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (—).
3. Unused product terms can be left blank.

AND

INACTIVE	0	I, B (I)
I, B	H	
$\bar{I}$, $\bar{B}$	L	
DON'T CARE	—	

OR

ACTIVE	A	B(0)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

POLARITY

	AND																						OR									
													B(I)										B(0)									
TERM	11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
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D4																																
D3																																
D2																																
D1																																
D0																																
PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14	23	22	21	20	19	18	17	16	15	14
VARIABLE NAME																																

TB00956S

Signetics

PLUS173D Field-Programmable Logic Array (22 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLUS173D is a 12ns version of the PLS173 FPLA architecture. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce performance levels not yet achieved in devices of this complexity.

The PLUS173D is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of Ex-OR gates for implementing AND/OR or AND/NOR logic functions.

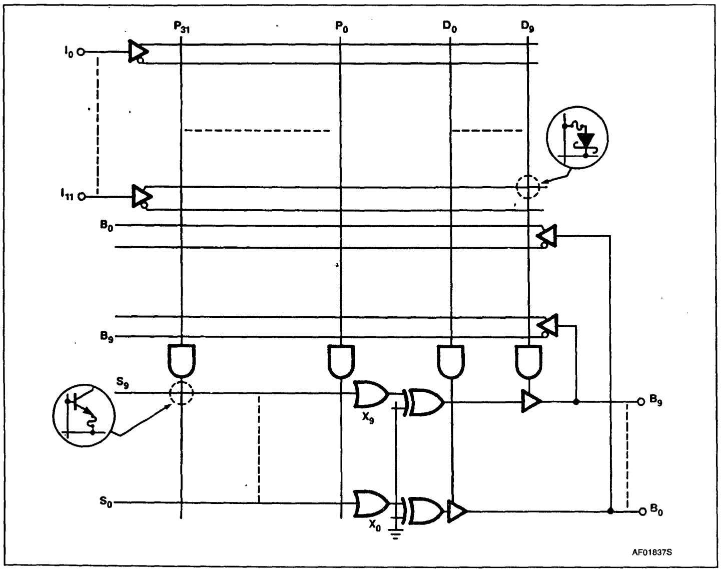
The PLUS173D is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

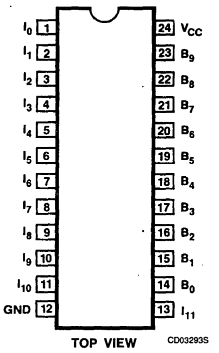
- **Field-Programmable (Ti-W links)**
- **Functionally identical to, and pin-for-pin compatible with, the PLS173 and the PLUS173B**
- **12 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Programmable output polarity**
  - **active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 12ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **3-State outputs**
- **TTL compatible**
- **Security fuse**

FUNCTIONAL DIAGRAM

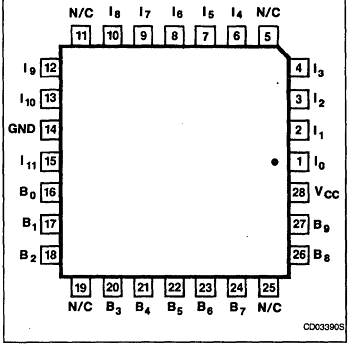


PIN CONFIGURATIONS

N Package



A Package

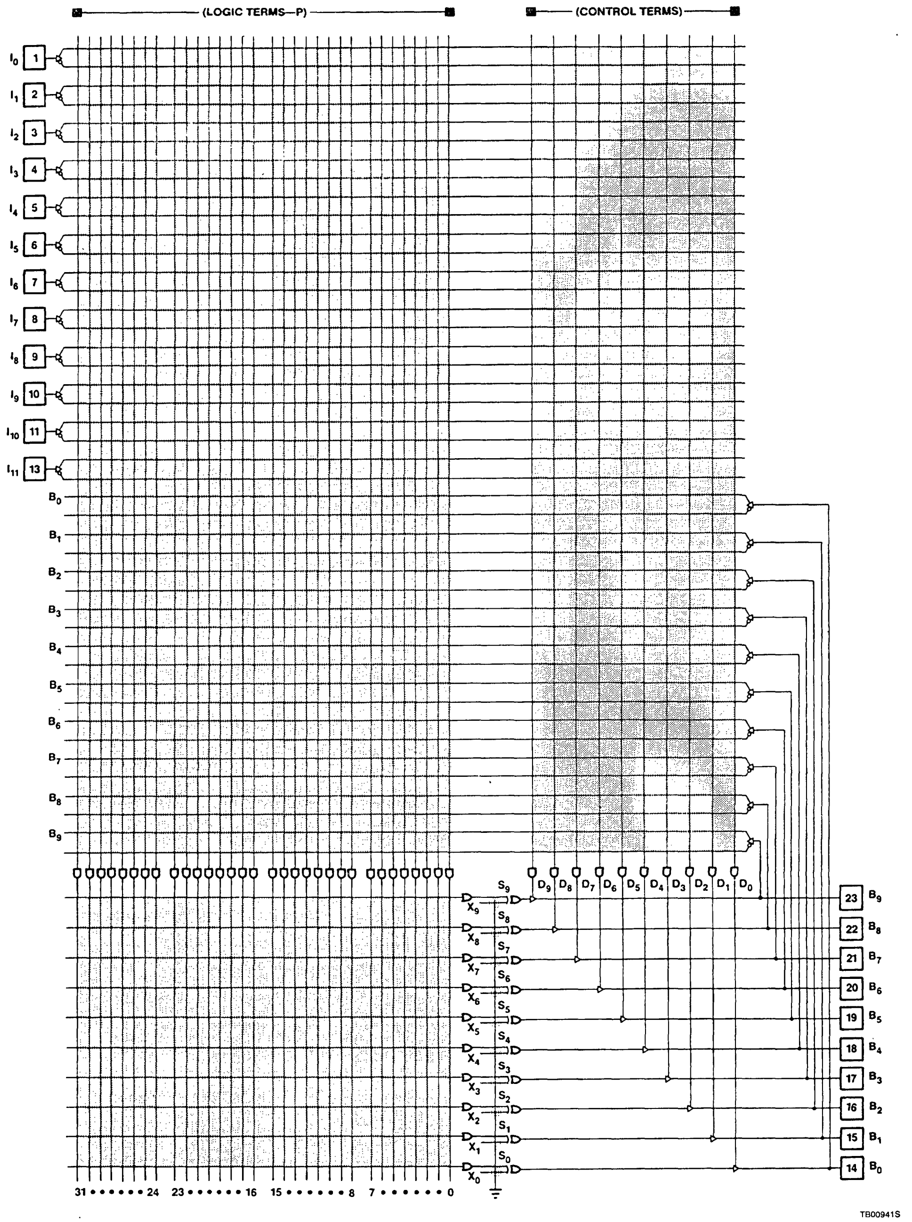


APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

Field-Programmable Logic Array (22 × 42 × 10) PLUS173D

FPLA LOGIC DIAGRAM



NOTES:

1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Array (22 × 42 × 10) PLUS173D

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLUS173DN
28-pin Plastic Leaded Chip Carrier	PLUS173DA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating free-air temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

[1] Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
Input current[10]						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		150	200	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on following page.

Field-Programmable Logic Array (22 × 42 × 10) PLUS173D

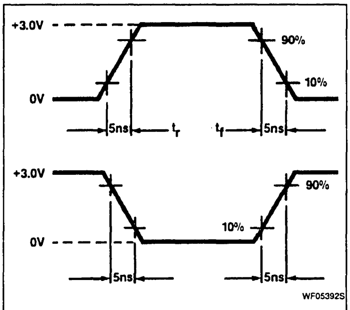
AC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		10	12	ns
t_{OE}	Output enable	Output −	Input ±	$C_L = 30pF$		10	12	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		10	12	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs $I_0 - I_4 = 0V$, inputs $I_5 - I_9 = 4.5V$, $I_{11} = 4.5V$ and $I_{10} = 10V$. For outputs $B_0 - B_4$ and for outputs $B_5 - B_9$ apply the same conditions except $I_{11} = 0V$.
5. Same conditions as Note 4 except input $I_{11} = +10V$.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs $I_0 - I_{11}$ and $B_0 - B_9 = 0V$. Part in Virgin State.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 - I_{11}$).

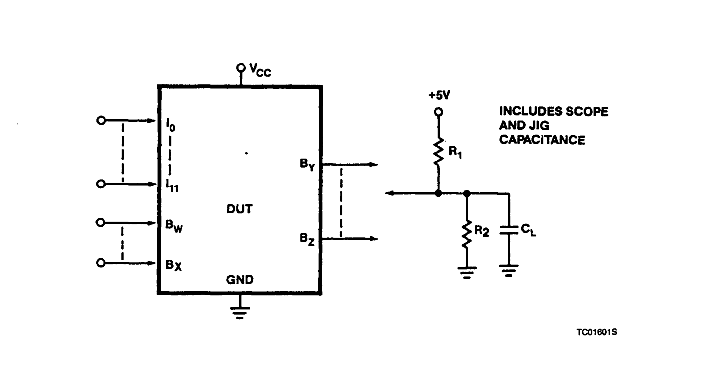
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

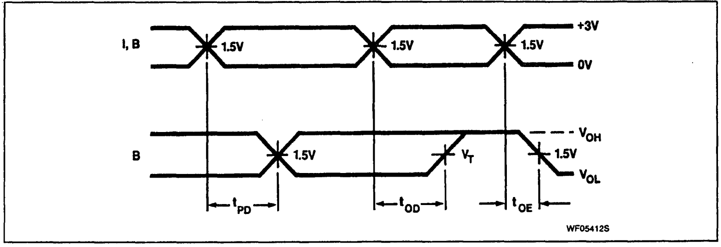
TEST LOAD CIRCUITS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Field-Programmable Logic Array (22 × 42 × 10) PLUS173D

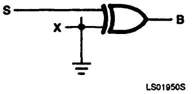
LOGIC PROGRAMMING

PLUS173D logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

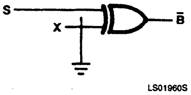
PLUS173D logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (B)

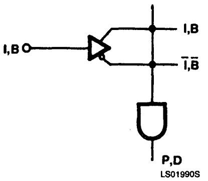


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

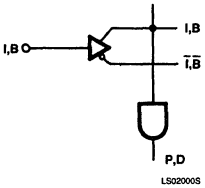


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

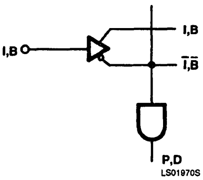
AND ARRAY – (I, B)



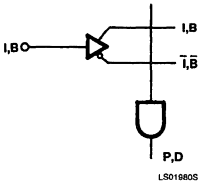
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H

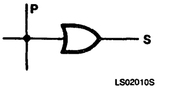


STATE	CODE
$\bar{I}$, $\bar{B}$	L

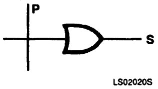


STATE	CODE
DON'T CARE	-

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the True and Complement of any input (I, B) are left intact.

Field-Programmable Logic Array (22 × 42 × 10) PLUS173D

FPLA PROGRAM TABLE

CUSTOMER NAME ____________

SIGNETICS DEVICE # ____________

PROGRAM TABLE # ______ REV ______ DATE ______

Notes

1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (–).
3. Unused product terms can be left blank.

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

AND

INACTIVE	0	I, B(I)
I, B	H	
$\bar{I}$, $\bar{B}$	L	
DON'T CARE	–	

																							POLARITY									
TERM	AND																						OR									
													B(I)										B(O)									
	11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
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PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14	23	22	21	20	19	18	17	16	15	14
VARIABLE NAME																																

TB00056S

Signetics

PLC473-60
Erasable and O.T.P. Programmable Logic Array (20 X 24 X 11)

Application Specific Products
- **Series 24**

Signetics Programmable Logic
Product Specification

DESCRIPTION

The PLC473-60 is a two-level logic CMOS Erasable Programmable Logic Device (EPLD) consisting of 24 AND gates and 22 OR gates with EPROM cell connections for programming I/O polarity and direction. The Signetics state-of-the-art Floating-Gate CMOS process is used to produce UV erasable and One Time Programmable (O.T.P.) versions of the PLC473.

All AND gate inputs are linked to 11 dedicated input pins ($I_0 - I_{10}$) and 9 bidirectional I/O pins ($B_0 - B_8$). These bidirectional pins are controlled via the OR array. Employing the 2 dedicated outputs ($O_A - O_B$) and the programmable I/O direction feature, the PLC473 can be configured with up to 20 inputs — and as many as 11 outputs.

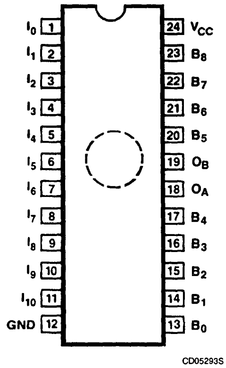
The AND array input buffers provide both the True and Complement of the inputs (I_X) and the bidirectional signals (B_X) as programmable connections to

FEATURES

- **Electrically Programmable; UV erasable and One Time Programmable (O.T.P.) versions available**
- **11 dedicated inputs**
- **2 dedicated outputs**
- **9 bidirectional I/O lines**
- **24 product terms**
- **I/O direction decoded in OR array**
- **I/O propagation delay: 60ns (max.)**
- **Input loading: −10μA (max.)**
- **Power dissipation:**
  - **CMOS inputs: 53mA max at 15MHz**
  - **TTL inputs: 60mA max at 15MHz**
- **Output: 3-State condition decoded in OR array**
- **TTL and CMOS compatible**

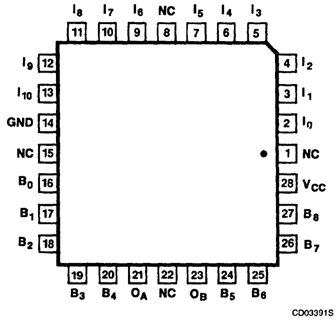
PIN CONFIGURATIONS

FA and N Packages



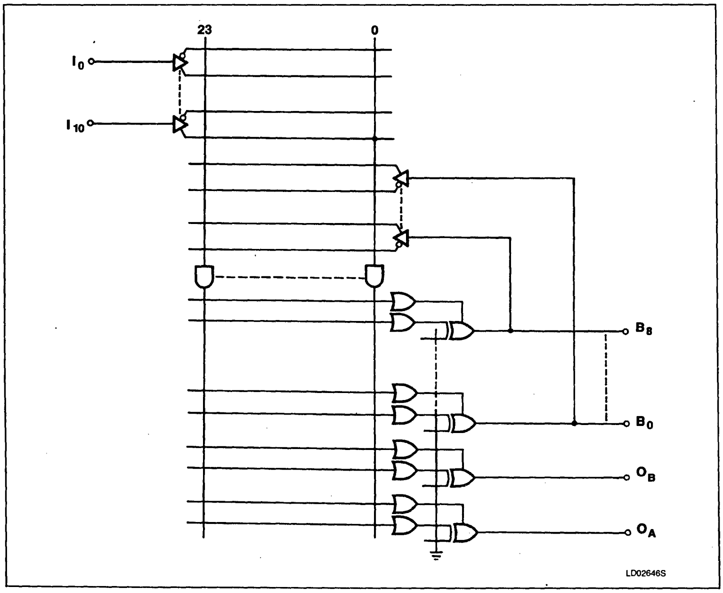
FA = Ceramic with window (erasable)
N = Plastic (O.T.P.)

A Package



NOTE:
A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



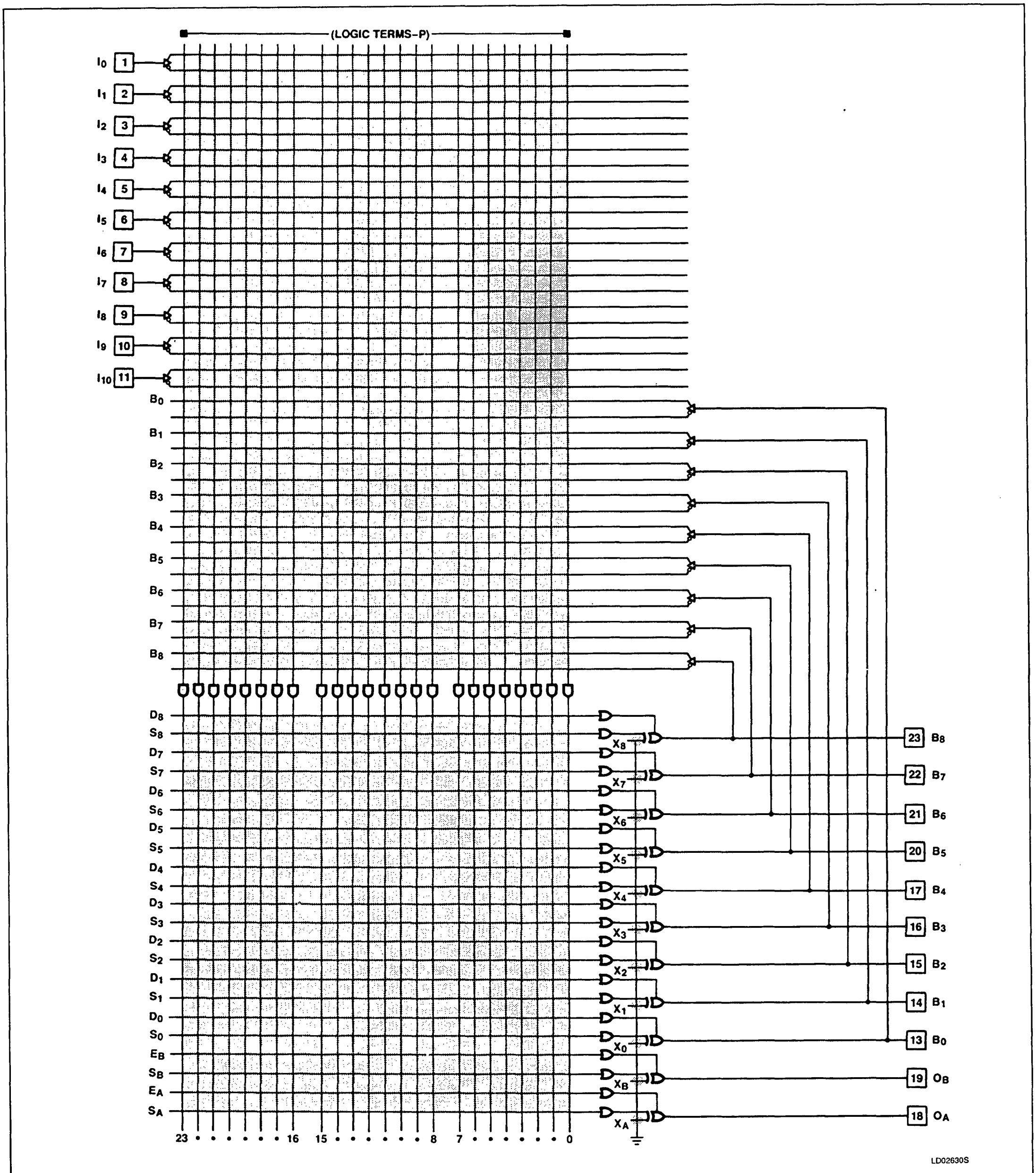
APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

Erasable and O.T.P. Programmable Logic Array (20 × 24 × 11)

PLC473-60

FPLA LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

the AND gates. All 24 AND gates can then be optionally linked to all 22 OR gates (a feature known as Product Term sharing not found in PALs[1] or most macrocell architectures). The OR array drives 11 output buffers which can be programmed as active-High for AND-OR functions or active-Low for AND-NOR functions. In addition, the I/O configuration of each bidirectional pin is individually controlled by a sum-of-products (AND-OR) function which may also contain any of the 24 AND gate outputs. This allows dynamic I/O configuration of all 9 bidirectional pins.

The PLC473-60 is field programmable using Floating-Gate Ultraviolet Erasable Cells. The UV erasable version is available in a ceramic DIP (300mil-wide) with a quartz window. One Time Programmable versions are available in plastic DIP and PLCC.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic DIP with Window (300mil-wide)	PLC473-60FA
24-pin Plastic DIP (300mil-wide)	PLC473-60N
28-pin Plastic Leaded Chip Carrier (PLCC)	PLC473-60A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	-30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$Z = \overline{P0 + P1 + P2 +} \ldots$

$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:

1. For each of the 11 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I), fixed output pins (O) and bidirectional pins (B).

Erasable and O.T.P. Programmable Logic Array (20 X 24 X 11)

PLC473-60

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +70°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION		LIMITS			UNIT
				Min	Typ[1]	Max	
Input voltage[2]							
V_{IL}	Low	V_{CC} = Min		-0.3		0.8	
V_{IH}	High	V_{CC} = Max		2.0		V_{CC} + 0.3	V
Output voltage[2]							
		V_{CC} = Min					
V_{OL}	Low	I_{OL} = 8mA				0.45	V
V_{OH}	High	I_{OH} = -3mA		2.4			
Input current[9]							
I_{IL}	Low	V_{IN} = GND				-10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	
Output current							
$I_{O(OFF)}$	Hi-Z state[7]	V_{OUT} = V_{CC}				10	µA
		V_{OUT} = GND				-10	µA
I_{OS}	Short circuit[3, 6]	V_{OUT} = GND		-15		-70	mA
I_{CC}	V_{CC} supply current (Active)[4, 5, 8]	No load, f = 15MHz, V_{CC} = Max	CMOS inputs			53	mA
			TTL inputs			60	mA
Capacitance							
		V_{CC} = 5V					
C_{IN}	Input	V_{IN} = 2.0V			6		
C_B	I/O (bidirectional)	V_B = 2.0V			12		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. CMOS inputs: V_{IL} = GND, V_{IH} = V_{CC}
   TTL inputs: V_{IL} = 0.45V, V_{IH} = 2.4V
5. Measured with all inputs and outputs switching.
6. Duration of short circuit should not exceed 1 second.
7. Leakage values are a combination of input and output leakage.
8. Refer to Figure 1 for I_{CC} vs frequency specifications (worst case).
9. Pin 1 (V_{PP}) has a leakage current of ±100µA.

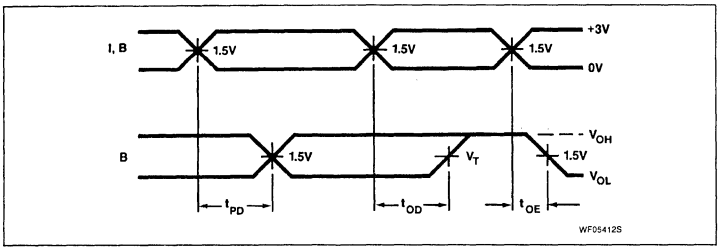
AC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +70°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS		UNIT
					Min	Max	
t_{PD}	Propagation delay	Output ±	Input ±	C_L = 30pF		60	ns
t_{OE}	Output enable	Output -	Input ±	C_L = 30pF		60	ns
t_{OD}	Output disable[1]	Output +	Input ±	C_L = 5pF		60	ns

NOTE:

1. Measured at V_T = V_{OL} + 0.5V.

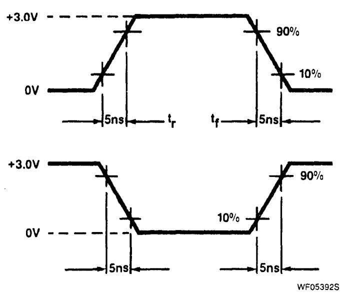
TIMING DIAGRAM



TIMING DEFINITIONS

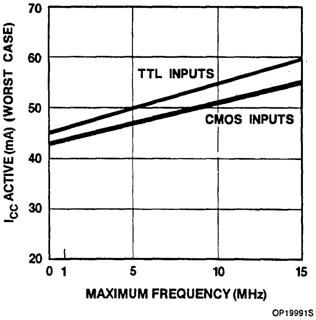
SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

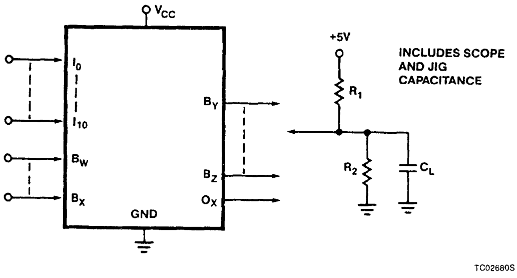
Input Pulses



NOTES:
1. Tested with all outputs switching.
2. Tested with TTL inputs (worst case).

Figure 1. Dynamic I_{CC} vs Frequency

TEST LOAD CIRCUITS



LOGIC PROGRAMMING

PLC473-60 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

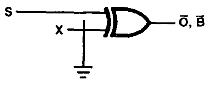
PLC473-60 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

Erasable and O.T.P. Programmable Logic Array (20 X 24 X 11)

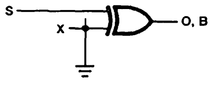
PLC473-60

OUTPUT POLARITY - (O, B)



ACTIVE LEVEL	CODE
LOW	L

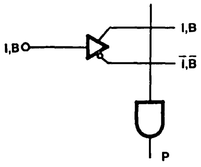
TC02561S



ACTIVE LEVEL	CODE
HIGH[1]	H

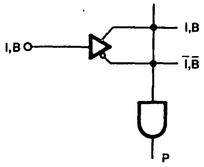
TC02571S

"AND" ARRAY - (I, B)



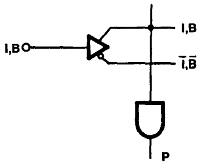
STATE	CODE
DON'T CARE	-

TC02601S



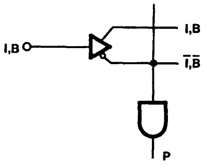
STATE	CODE
INACTIVE[1]	O

TC02632S



STATE	CODE
I, B	H

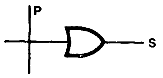
TC02610S



STATE	CODE
$\bar{I}$, $\bar{B}$	L

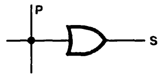
TC02620S

"OR" ARRAY - (O, B)



P_n STATUS	CODE
INACTIVE	•

TC02581S



P_n STATUS	CODE
ACTIVE[1]	A

TC02590S

NOTES:

1. This is the initial unprogrammed state of all link pairs.
2. Any Product Term (P_n) will always be False (logic low) if at least one of its (I,B) link pairs is unprogrammed as shown.

VIRGIN STATE

A factory shipped virgin device is configured such that:

1. All outputs are at "H" polarity.
2. All P_n terms are inactive in the AND array.
3. All P_n terms are active in the OR array.

ERASURE CHARACTERISTICS (FOR FA PACKAGE ONLY)

The PLC473 is erased by exposure to ultraviolet light. The recommended erasure procedure is exposure to short-wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^3. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12,000μW/cm^2 power rating.

The PLC473 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a PLC473 can be exposed to without damage is 7258Wsec/cm^2 (1week @ 12,000μW/cm^2). Exposure of this CMOS EPROM to high-intensity UV light for longer periods may cause permanent damage. Some erasure may occur with exposure to light sources having wavelengths shorter than 4,000Å such as sunlight or fluorescent light. For maximum system reliability, precautions should be taken by placing opaque labels over the quartz window when used in these environments.

Erasable and O.T.P. Programmable Logic Array (20 × 24 × 11)

PLC473-60

FPLA PROGRAM TABLE

CUSTOMER NAME ______________________
PURCHASE ORDER # ______________________
SIGNETICS DEVICE # ____________ CF (XXXX) ____________
CUSTOMER SYMBOLIZED PART # ______________________
TOTAL NUMBER OF PARTS ______________________
PROGRAM TABLE # ________ REV ________ DATE ________

AND

INACTIVE	0	I,B(I)
I, B	H	
$\bar{I}$, $\bar{B}$	L	
DON'T CARE	—	

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

																																	POLARITY										
	AND																					OR																					
TERM	I											B (I)									TERM	E		D									O		B (O)								
	10	9	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0		B	A	8	7	6	5	4	3	2	1	0	B	A	8	7	6	5	4	3	2	1	0
0																					0																						
1																					1																						
2																					2																						
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PIN	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	17	16	15	14	13													19	18	23	22	21	20	17	16	15	14	13
VARIABLE NAME																																											

Notes:
1. The EPLA is shipped with all links intact.
2. Unused I and B bits in the AND array should be programmed as Don't Care (–).
3. Unused product terms should be programmed in the OR array.
4. All product terms are active in the OR array in the virgin state.

TB01981S

Signetics

PLHS473
Field-Programmable Logic Array (20 × 24 × 11)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLHS473 is a two level logic device consisting of 24 AND gates and 22 OR gates with fusible link connections for programming I/O polarity and direction. The Signetics state of the art Oxide-Isolated Bipolar process is used to produce performance not yet achieved in devices of this complexity.

All AND gates are linked to 11 input pins, 9 bidirectional I/O pins, and 2 dedicated output pins. The bidirectional pins are controlled via the OR array. Using these features, the PLHS473 can be configured with up to 20 inputs and as many as 11 outputs.

The AND array input buffers provide both the True and Complement of the inputs (I_X) and the bidirectional signals (B_X) as programmable connections to the AND gates. All 24 AND gates can then be optionally linked to all 22 OR gates (a feature known as Product Term sharing not found in PAL® device architectures or most macrocell architectures). The OR array drives 11 output buffers which can be programmed as active-High for AND-OR functions or active-Low for AND-NOR functions. In addition, the I/O configuration of each bidirectional pin is individually controlled by a sum-of-products (AND-OR) function which may also contain any of the 24 AND gate outputs. This allows dynamic I/O configuration of all 9 bidirectional pins.

The PLHS473 contains two new features of significance. A code verification lock has been incorporated to improve user security. The addition of three test columns and one test row enables the user to test the device in an unprogrammed state.

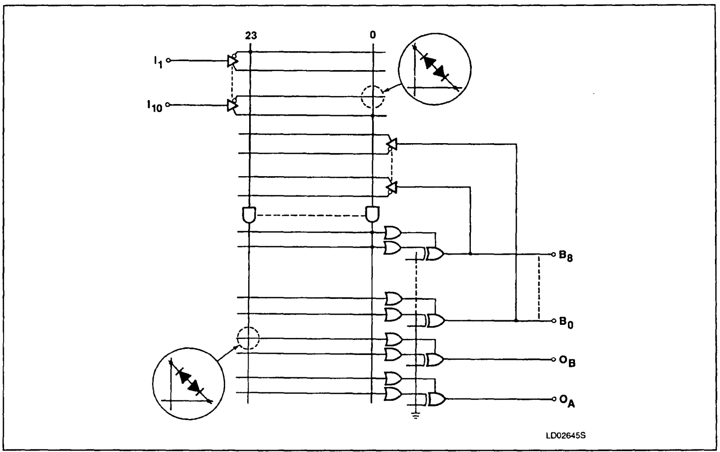
The PLHS473 is field programmable using Vertical Avalanche Migration Programmed (VAMP™) fuses to program the cells. This enables the generation of custom logic patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

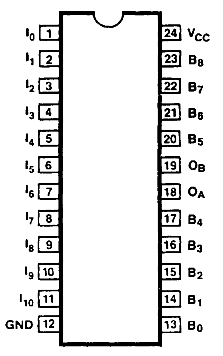
- **Field-Programmable**
- **11 dedicated inputs**
- **2 dedicated outputs**
- **9 bidirectional I/O lines**
- **24 product terms**
- **22 OR gates**
- **I/O direction decoded in OR array**
- **Output Enable decoded in OR array**
- **Security fuse**
- **I/O propagation delay: 22ns (max.)**

FUNCTIONAL DIAGRAM



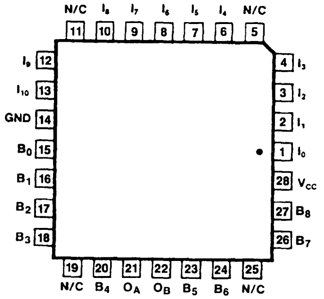
PIN CONFIGURATIONS

N Package



CD05294S

A Package



CD05300S

- **Input loading: −100μA (max.)**
- **Power dissipation: 700mW (typ.)**
- **Security fuse**
- **Testable in unprogrammed state**
- **Programmable as 3-State or Open-Collector outputs**
- **TTL compatible**
- **Programmable output polarity**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

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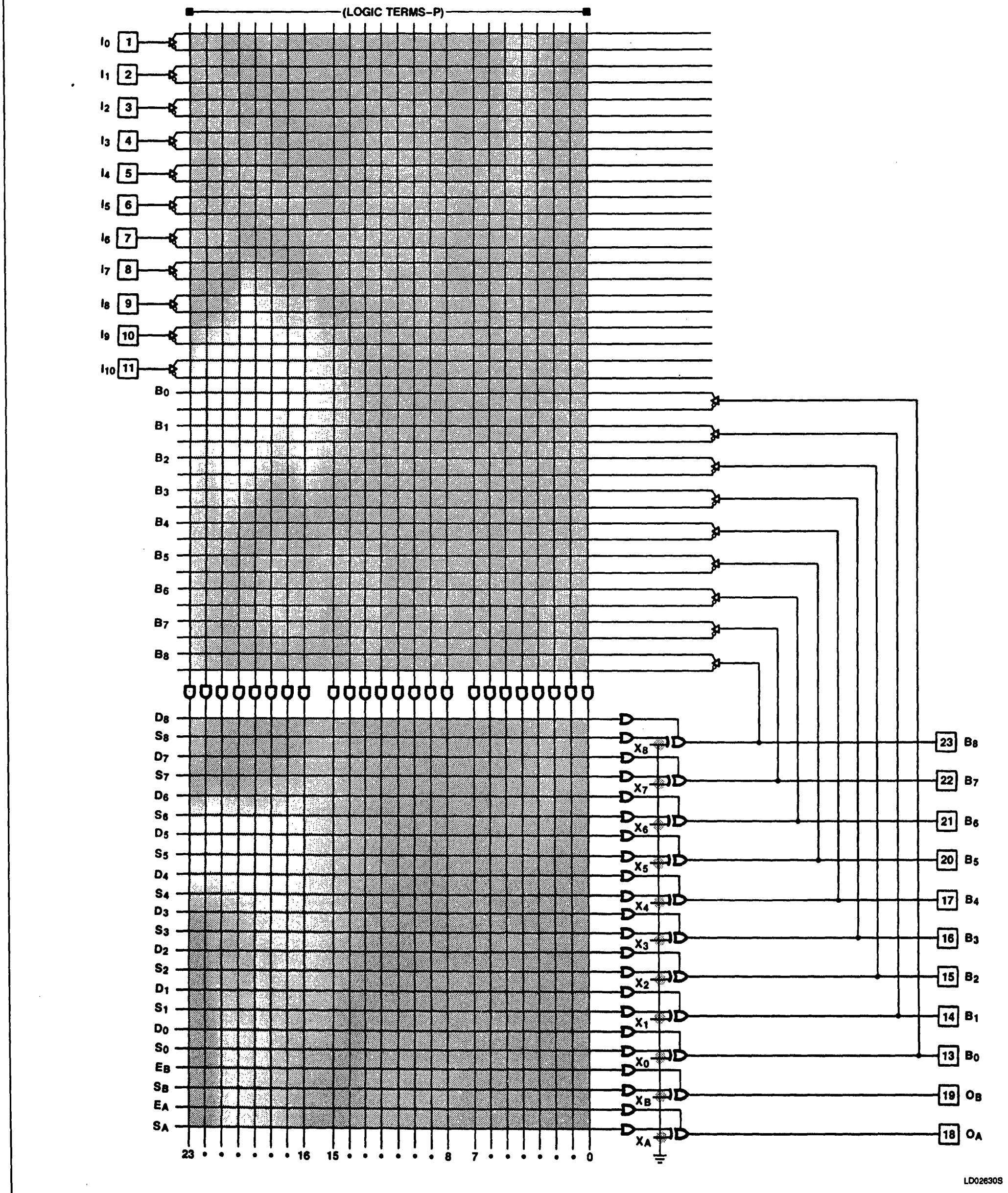
FPLA LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. All unprogrammed or virgin "OR" gate locations are pulled to logic "0".
3. ◌ Programmable connection.

Field-Programmable Logic Array (20 × 24 × 11) PLHS473

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLHS473N
28-pin Plastic Leaded Chip Carrier	PLHS473A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	-30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_A	Operating free-air temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ ...$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ ...$

AT OUTPUT POLARITY = L

$Z = \overline{P0 + P1 + P2 +} \ ...$

$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ ...$

NOTES:

1. For each of the 11 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I), fixed output pins (0) and bidirectional pins (B).

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[3]						
		V_{CC} = Min				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			40	µA
		V_{OUT} = 0.45V			-100	µA
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0.5V	-15		-70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		140	155	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

Notes on the following page.

Field-Programmable Logic Array (20 × 24 × 11) PLHS473

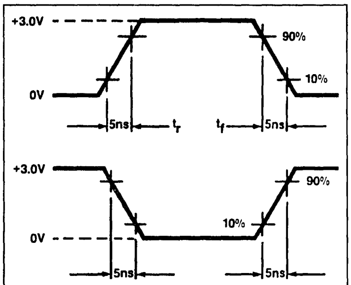
AC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 30pF$		15	22	ns
t_{OE}	Output enable	Output –	Input ±	$C_L = 30pF$		15	22	ns
t_{OD}	Output disable[8]	Output +	Input ±	$C_L = 5pF$		15	22	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs 0 – 4 = 0V, inputs 5, 7 = 4.5V, and inputs 6, 8 – 10 = 10V.
5. Same conditions as Note 5 except input 8 = 4.5V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with all inputs and bidirectional pins at 4.5V. Part in Virgin State.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.

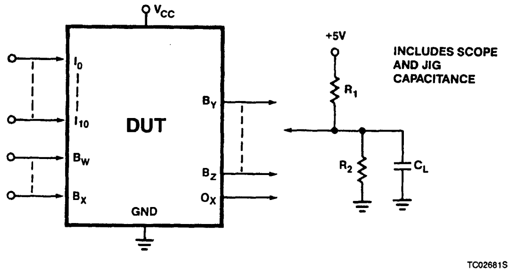
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

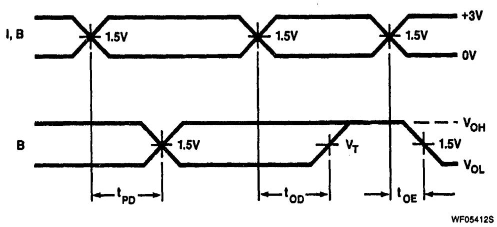
TEST LOAD CIRCUITS



TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Field-Programmable Logic Array (20 × 24 × 11) PLHS473

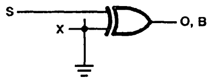
LOGIC PROGRAMMING

PLHS473 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLHS473 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

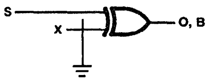
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (O, B)



TC02574S

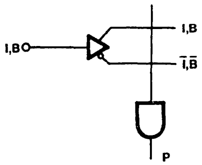
ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H



TC02564S

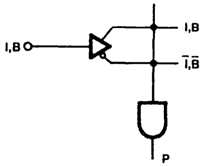
ACTIVE LEVEL	CODE
LOW[1] (INVERTING)	L

"AND" ARRAY – (I, B)



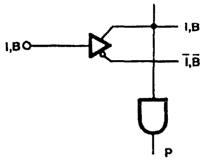
STATE	CODE
DON'T CARE[1]	-

TC02600S



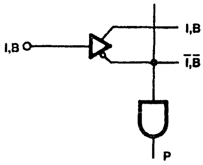
STATE	CODE
INACTIVE[2]	O

TC02630S



STATE	CODE
I, B	H

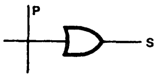
TC02610S



STATE	CODE
$\overline{I}$, $\overline{B}$	L

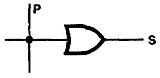
TC02620S

OR ARRAY – (O, B)



P_n STATUS	CODE
INACTIVE[1]	•

TC02580S



P_n STATUS	CODE
ACTIVE	A

TC02591S

NOTES:

1. This is the initial unprogrammed state of all links. All unused P_n and D_n terms must be programmed as INACTIVE.
2. Any gate P_n will be unconditionally inhibited if the True and Complement of either input (I or B) are both programmed for a connection.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "L" polarity.
2. All P_n terms are enabled in the AND array. (Don't Cares)
3. All P_n terms are inactive in the OR array.

Field-Programmable Logic Array (20 × 24 × 11) PLHS473

FPLA PROGRAM TABLE

CUSTOMER NAME ____________
PURCHASE ORDER # ____________
SIGNETICS DEVICE # ________ CF (XXXX) ________
CUSTOMER SYMBOLIZED PART # ____________
TOTAL NUMBER OF PARTS ____________
PROGRAM TABLE # ______ REV ______ DATE ______

AND

INACTIVE	0	I,B(I)
I, B	H	
Ī, B̄	L	
DON'T CARE	—	

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

POLARITY										

TERM	AND																				TERM	OR																					
	I											B (I)										E		D									O		B (O)								
	10	9	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0		B	A	8	7	6	5	4	3	2	1	0	B	A	8	7	6	5	4	3	2	1	0
0																					0																						
1																					1																						
2																					2																						
3																					3																						
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VARIABLE NAME																																											

Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All P-terms are inactive on all outputs (B, O) in the virgin array.
4. Unused product terms can be left blank.

TB01980S

Signetics

PLS100/PLS101
Field-Programmable Logic Array (16 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLS100 (3-state) and PLS101 (Open-Collector) are bipolar, fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs can be ANDed together to comprise one P-term. All 48 P-terms can be selectively ORed to each output.

The PLS100 and PLS101 are fully TTL compatible, and chip enable control for expansion of input variables and output inhibit. They feature either Open-Collector or 3-state outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

FEATURES

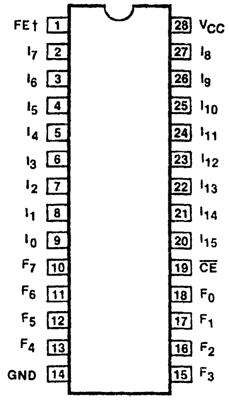
- **Field-Programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **I/O propagation delay: 50ns (max.)**
- **Power dissipation: 600mW (typ.)**
- **Input loading: −100μA (max.)**
- **Chip Enable input**
- **Output option:**
  - **PLS100: 3-State**
  - **PLS101: Open-Collector**
- **Output disable function:**
  - **3-State: Hi-Z**
  - **Open-Collector: High**

APPLICATIONS

- **CRT display systems**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**
- **16-bit to 8-bit bus interface**
- **Random logic replacement**

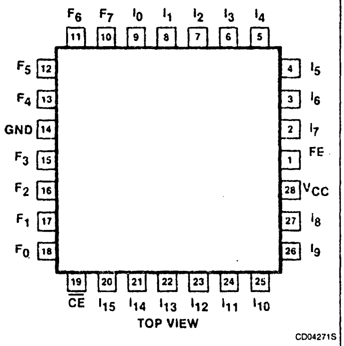
PIN CONFIGURATIONS

N Package

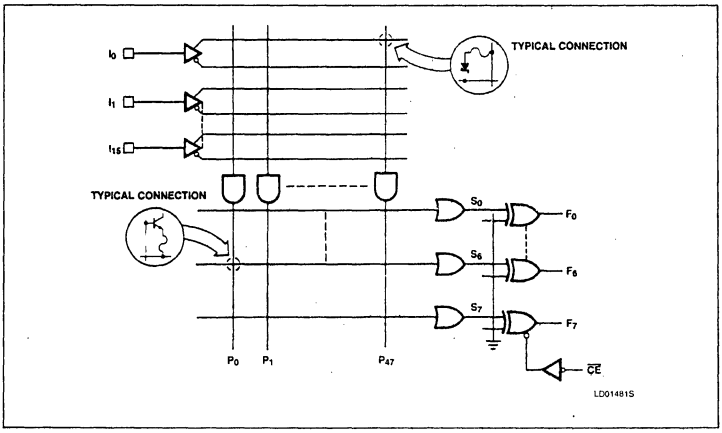


† Fuse Enable Pin: It is recommended that this pin either be left open or connected to ground during normal operation.

A Package



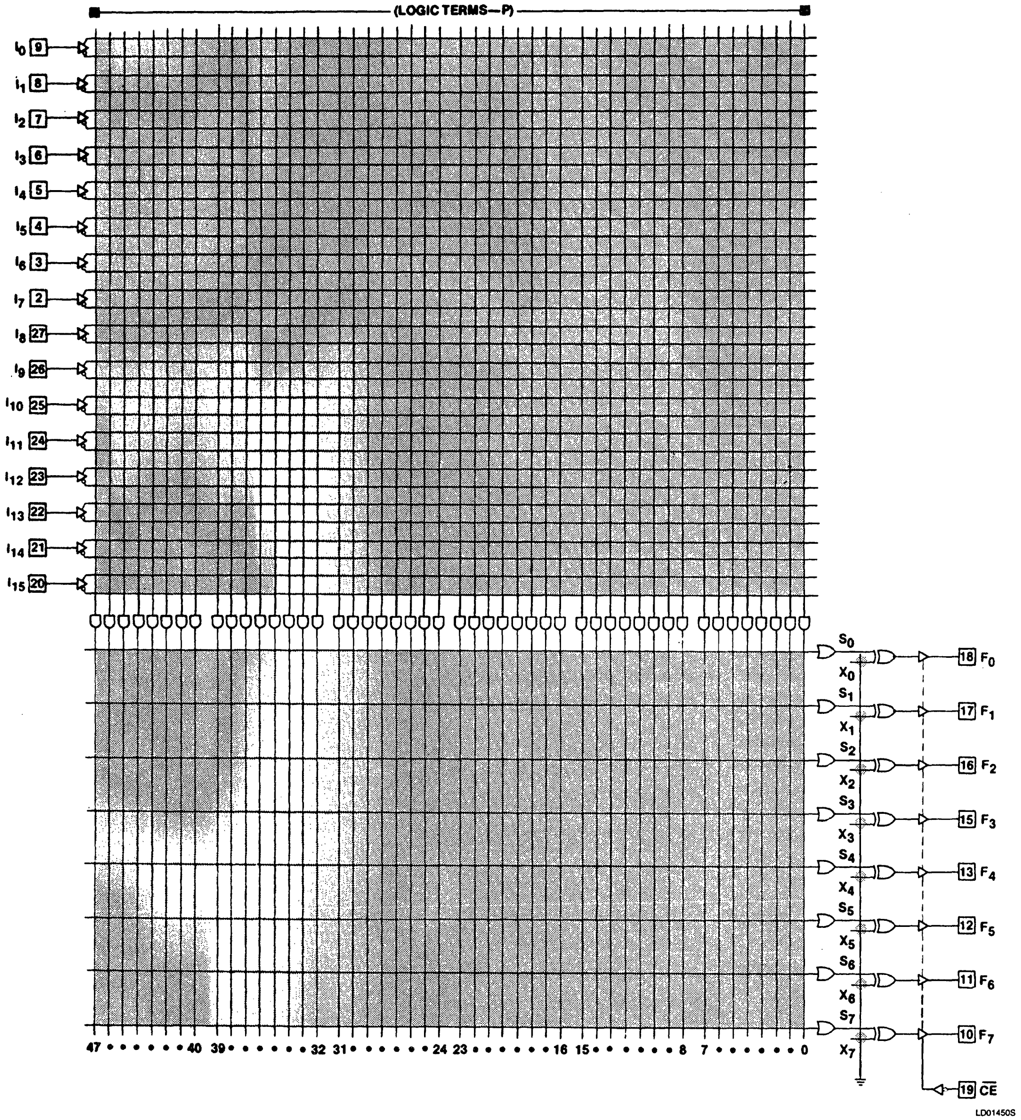
FUNCTIONAL DIAGRAM



Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

FPLA LOGIC DIAGRAM



NOTES:

1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

ORDERING INFORMATION

DESCRIPTION	TRI-STATE	OPEN-COLLECTOR
28-pin Plastic DIP 600mil-wide	PLS100N	PLS101N
28-pin Plastic Leaded Chip Carrier	PLS100A	PLS101A

The PLS100 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[2, 3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High (PLS100)[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
Output current						
$I_{O(OFF)}$	Hi-Z state (PLS100)	$\overline{CE}$ = High, V_{CC} = Max				
		V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit (PLS100)[3, 6]	$\overline{CE}$ = Low, V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		120	170	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		17		pF

Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Propagation delay							
t_{PD}	Input	Output	Input		35	50	ns
t_{CE}	Chip enable	Output	Chip enable		15	30	ns
Disable time							
t_{CD}	Chip disable	Output	Chip enable		15	30	ns

NOTES:

1. All values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test one pin at a time.
4. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
5. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

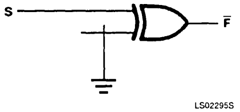
LOGIC PROGRAMMING

PLS100/PLS101 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

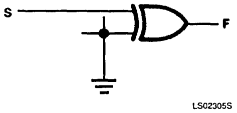
PLS100/PLS101 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY - (F)

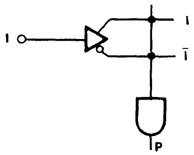


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

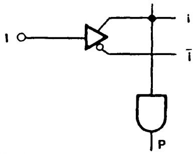


ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

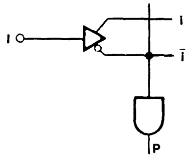
"AND" ARRAY - (I)



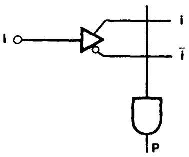
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I	H

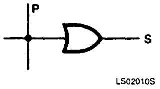


STATE	CODE
Ī	L

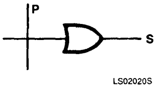


STATE	CODE
DON'T CARE	—

"OR" ARRAY - (F)



P_n STATUS	CODE
ACTIVE[1]	A

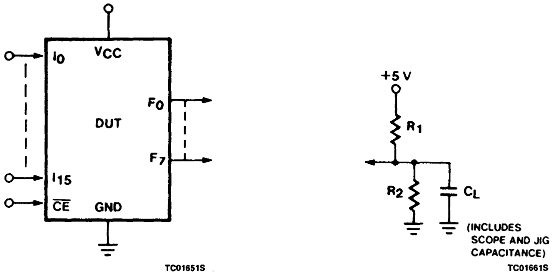


P_n STATUS	CODE
INACTIVE	•

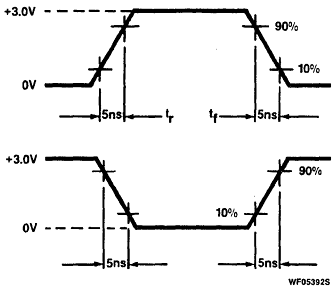
NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

TEST LOAD CIRCUITS



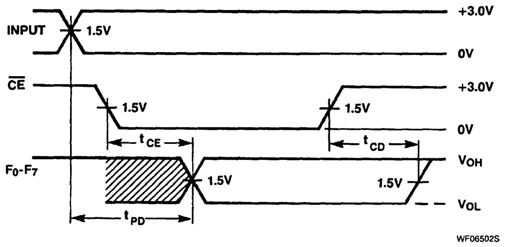
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAM



Read Cycle

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable low (with Input valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off state (Hi-Z or High).
t_{PD}	Delay between beginning of valid Input (with Chip Enable Low) and when Data Output becomes valid.

VIRGIN STATE

The PLS100/101 virgin devices are factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All P_n terms are disabled (inactive), in the AND array.
2. All P_n terms are active in the OR array.
3. All outputs are active-High.

Field-Programmable Logic Array (16 × 48 × 8)

PLS100/PLS101

FPLA PROGRAM TABLE

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	Im	Don't Care	Prod. Term Present in F_P	Prod. Term Not Present in F_P	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L

NOTE
Enter (—) for unused inputs of used P-terms.

NOTES
1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

NOTES
1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

CUSTOMER NAME __________

PURCHASE ORDER # __________

SIGNETICS DEVICE # __________ CF (XXXX)

CUSTOMER SYMBOLIZED PART # __________

TOTAL NUMBER OF PARTS __________

PROGRAM TABLE # __________ REV __________ DATE __________

	AND																POLARITY							
	INPUT (I_m)																OR							
																	OUTPUT (F_P)							
TERM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
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PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	12	13	15	16	17	18
VARIABLE NAME																								

TB01560S

Signetics

PLS103 Field-Programmable Gate Array (16 × 9 × 9)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 28

DESCRIPTION

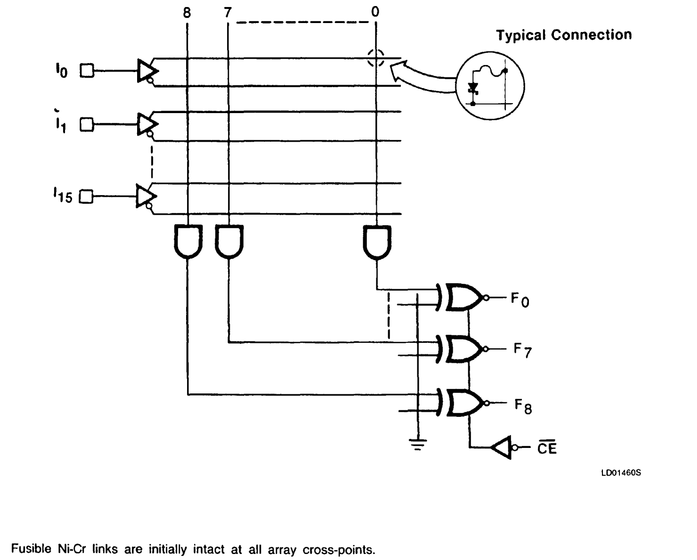
The PLS103 is a bipolar, fuse Programmable Gate Array. The device consists of nine AND/NAND gates which share 16 common inputs. The type of gate is selected by programming the output as active-High (H) or active-Low (L). Each of the 16 inputs $I_0 - I_{15}$ can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the nine AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS103 includes chip-enable control for output strobing and inhibit. It features 3-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

FUNCTIONAL DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

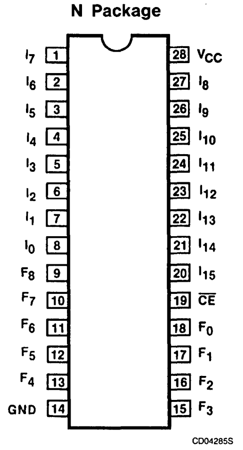
FEATURES

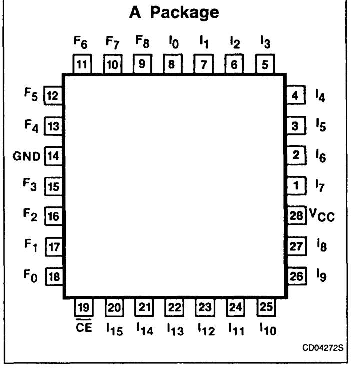
- Field-Programmable (Ni-Cr link)
- 16 input variables
- 9 output functions
- Chip Enable input
- I/O propagation delay: 35ns (max.)
- Power dissipation: 600mW (typ.)
- Input loading: $-100\mu A$ (max.)
- 3-State outputs
- Output disable function: Hi-Z
- Fully TTL compatible

APPLICATIONS

- Random logic
- Address decoders
- Code detectors
- Peripheral selectors
- Fault monitors
- Machine state decoders

PIN CONFIGURATIONS





LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$X = A \cdot \overline{B} \cdot C \cdot \ \ldots$

ACTIVE-LOW

$X = \overline{A \cdot \overline{B} \cdot C \cdot} \ \ldots$
$X = \overline{A} + B + \overline{C} + \ \ldots$

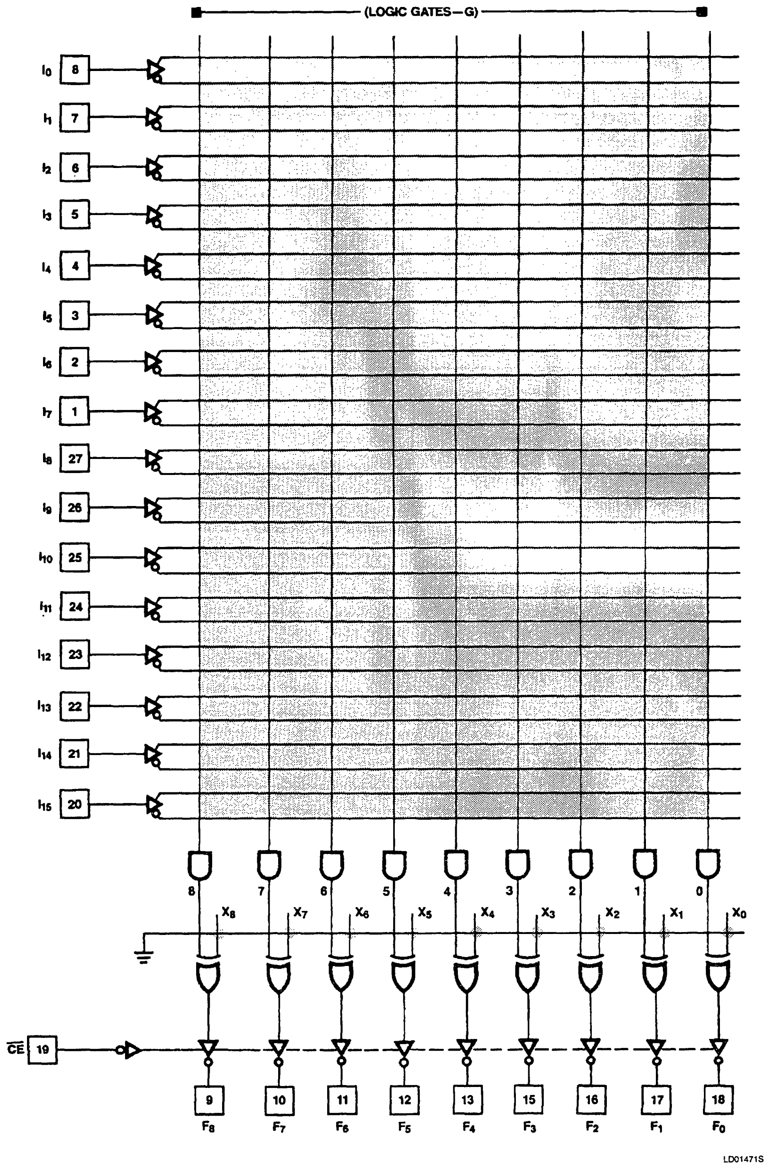
NOTES:

1. For each of the 9 outputs, either function X (active-High) or $\overline{X}$ (active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (O).

Field-Programmable Gate Array (16 × 9 × 9)

PLS103

FPGA LOGIC DIAGRAM



NOTES:
1. All gate inputs when a blown link float to a logic "1".
2. ▨ Programmable connection.

Field-Programmable Gate Array (16 × 9 × 9)

PLS103

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	PLS103N
28-pin Plastic Leaded Chip Carrier	PLS103A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[2]	Max	
Input voltage[1]						
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[1]						
		V_{CC} = Min				
V_{OH}	High[5]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[4]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
Output current						
		$\overline{CE}$ = High, V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[3,6]	$\overline{CE}$ = Low, V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		120	170	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

Notes on following page.

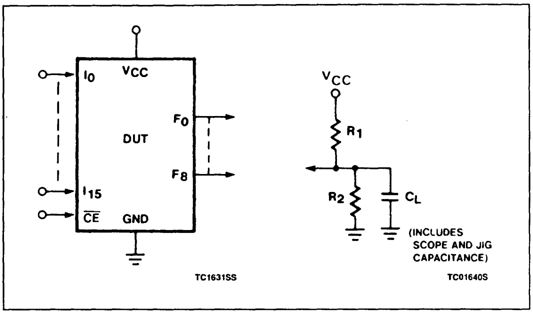
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
Propagation delay							
t_{PD}	Input	Output	Input		20	35	ns
t_{CE}	Chip enable	Output	Chip enable		15	30	ns
Disable time							
t_{CD}	Chip disable	Output	Chip enable		15	30	ns

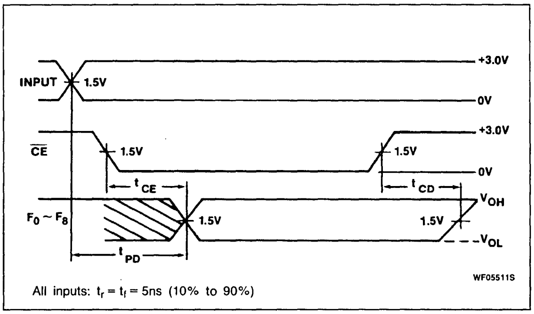
NOTES:

1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. Test one pin at a time.
4. Measure with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the outputs open.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

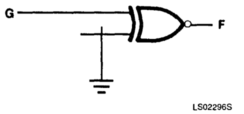
LOGIC PROGRAMMING

In a virgin device all Ni-Cr links are intact. PLS013 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

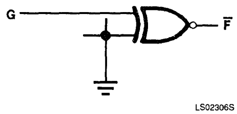
PLS013 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY - (F)

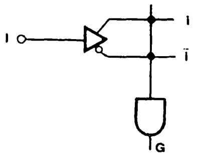


ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H

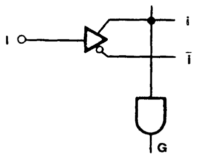


ACTIVE LEVEL	CODE
LOW[1] (INVERTING)	L

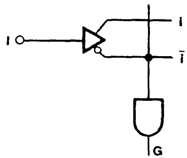
"AND" ARRAY - (I), (P)



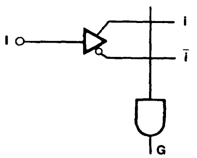
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I	H



STATE	CODE
Ī	L



STATE	CODE
DON'T CARE	—

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate G_n will be unconditionally inhibited if both the True and Complement fuses of any input (I) are left intact.

VIRGIN STATE

The PLS103 virgin device is factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All P_n terms are disabled (inactive).
2. All P_n terms are active on all outputs.
3. All outputs are active-Low.

FPGA PROGRAM TABLE

CUSTOMER NAME ________	*THIS PORTION TO BE COMPLETED BY SIGNETICS*
PURCHASE ORDER # ________	*CF (XXXX)* ________
SIGNETICS DEVICE # ________	*CUSTOMER SYMBOLIZED PART #* ________
TOTAL NUMBER OF PARTS ________	*DATE RECEIVED* ________
PROGRAM TABLE # ________	*COMMENTS* ________

F_0 (18) ________ = ________

F_1 (17) ________ = ________

F_2 (16) ________ = ________

F_3 (15) ________ = ________

F_4 (13) ________ = ________

F_5 (12) ________ = ________

F_6 (11) ________ = ________

F_7 (10) ________ = ________

F_8 (9) ________ = ________

GATE		INPUT															
POLARITY		I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
F_0																	
F_1																	
F_2																	
F_3																	
F_4																	
F_5																	
F_6																	
F_7																	
F_8																	
PIN NO.		20	21	22	23	24	25	26	27	1	2	3	4	5	6	7	8
VARIABLE NAME																	

NOTES:
1. The FPGA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused Inputs are normally programmed Don't Care (—).
3. Unused Gates can be left blank.

PROGRAM TABLE ENTRIES

AND

INACTIVE	0
I	H
$\bar{I}$	L
Don't Care	—

(I)

CONTROL

HIGH	H
LOW	L

(POL.)

LD02260S

Signetics

Application Specific Products

Section 5 Programmable Logic Sequencer Device Data Sheets

INDEX

Series 20

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PLS157 Field-Programmable Logic Sequencer (16 × 45 × 12); 18.2MHz. 5-14
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Series 24

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Signetics

PLS155

Field-Programmable Logic Sequencer (16 × 45 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

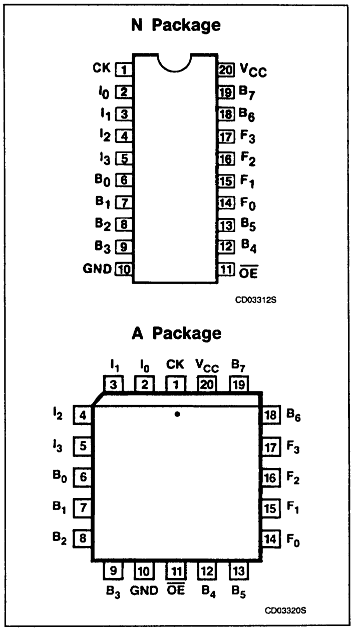
The PLS155 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 4 registered I/O outputs (F) in conjunction with 8 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- f_{MAX} = 14MHz
  - 18.2MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 8 bidirectional I/O lines
- 4 bidirectional registers
- J-K, T, or D-type flip-flops
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: −100μA (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible
- 3-State outputs

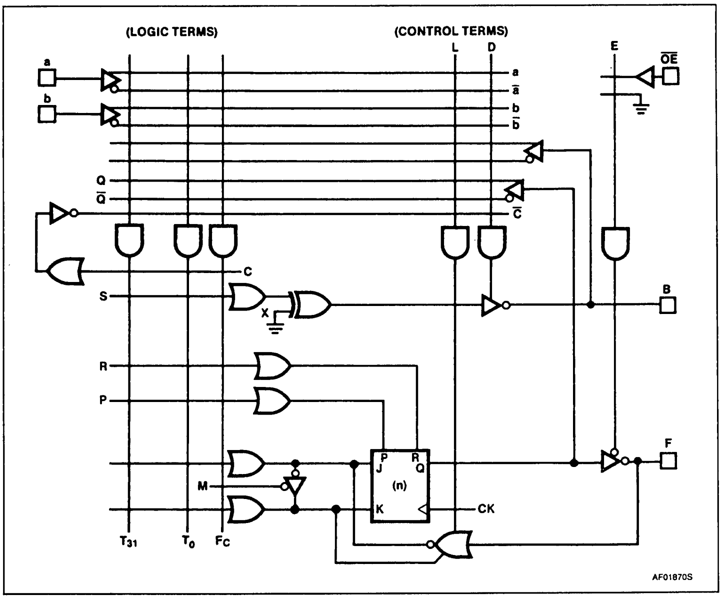
PIN CONFIGURATIONS



APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

FUNCTIONAL DIAGRAM



Field-Programmable Logic Sequencer (16 × 45 × 12) PLS155

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops. The Asynchronous Preset and Reset lines (P, R), are driven from the OR matrix.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS155 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

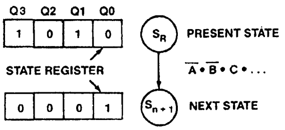
Order codes are listed in the Ordering Information Table.

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J/K only or J/K or D (controlled).
5. All B pins, are inputs and all F pins are outputs unless otherwise programmed.

LOGIC FUNCTION



SET Q_0: $J_0 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

TOGGLE Q_3: $J_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

TB00901S

NOTES:
Similar logic functions are applicable for D and T mode flip-flops.

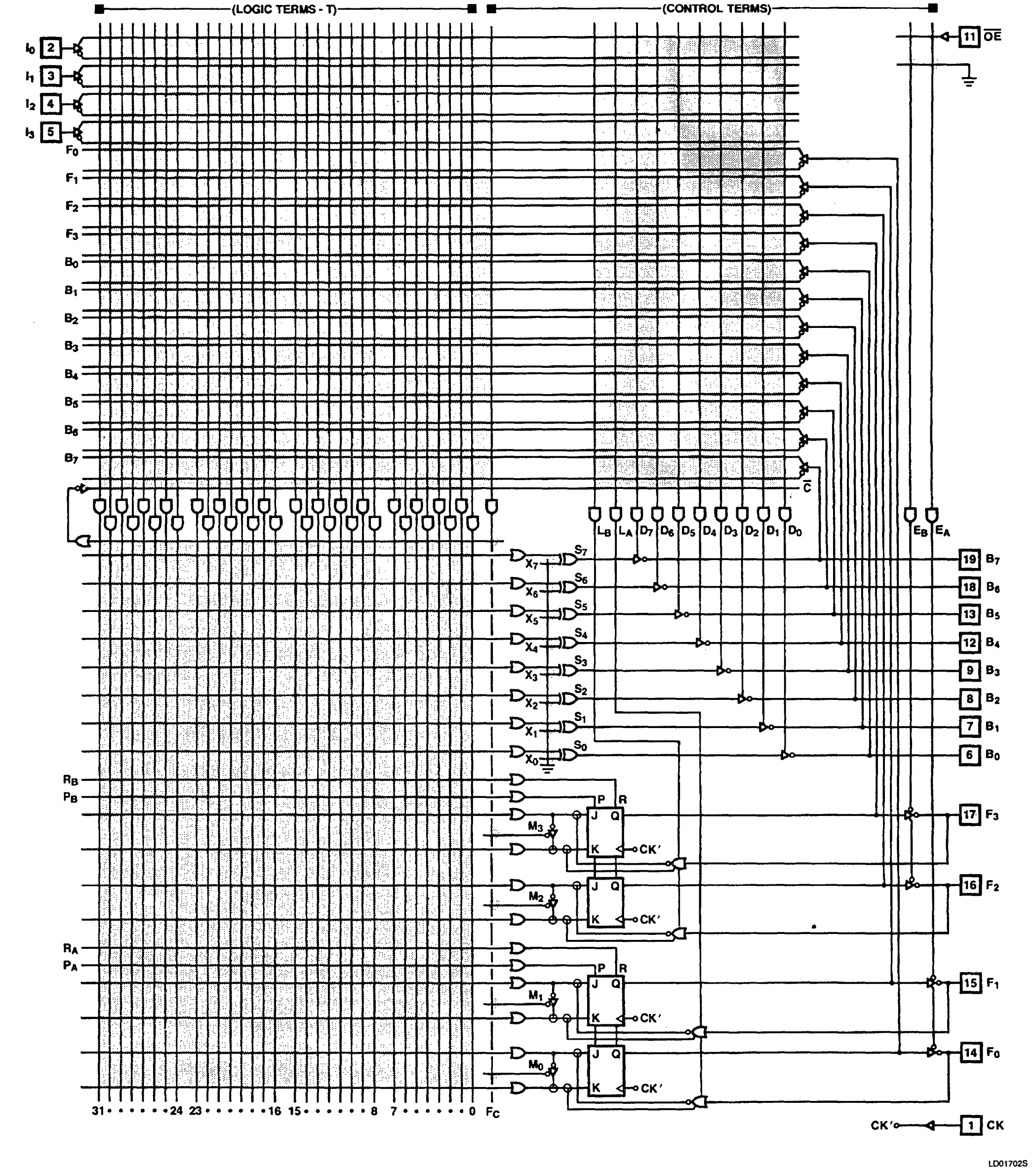
FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:
1. Positive Logic:
$J/K = T_0 + T_1 + T_2$ .... T_{31}
$T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (Q_0 \bullet Q_1 \ldots) \bullet (B_0 \bullet B_1 \bullet \ldots)$
2. ↑denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active T_n disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. * * = Forced at F_n pin to load J/K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS155

FPLS LOGIC DIAGRAM



NOTES:

1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ▨ Programmable connection.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS155

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLS155N
20-pin Plastic Leaded Chip Carrier	PLS155A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High	I_{OH} = −2mA	2.4			V
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5	V
Input current[5]						
		V_{CC} = Max				
I_{IH}	High	V_{IN} = 5.5V		< 1	80	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
Output current						
		V_{CC} = Max				
$I_{O\ (OFF)}$	Hi-Z state[5, 6]	V_{OUT} = 5.5V		1	80	µA
		V_{OUT} = 0.45V		−1	−140	µA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[4]	V_{CC} = Max		150	190	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = + 25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
5. Leakage values are a combination of input and output leakage.
6. Measured with V_{IH} applied to $\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

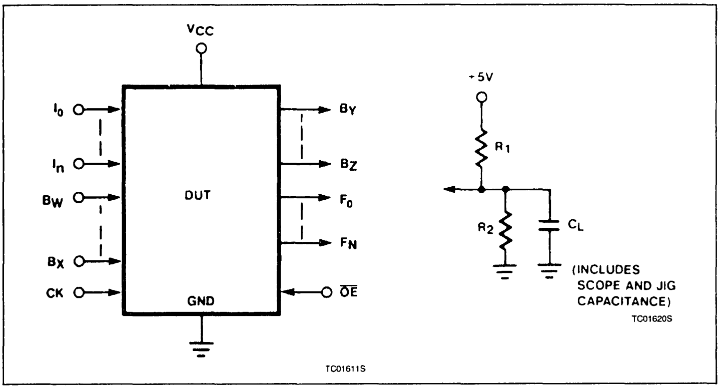
SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min[5]	Typ[1]	Max	
Pulse width								
t_{CKH}	Clock[2] High	CK −	CK +	$C_L = 30pF$	25	20		ns
t_{CKL}	Clock Low	CK +	CK −		30	20		
t_{CKP}	Period	CK +	CK +		70	50		
t_{PRH}	Preset/Reset pulse	(I,B) +	(I,B) −		40	30		
Setup time								
t_{IS1}	Input	CK +	(I,B) ±	$C_L = 30pF$	40	30		ns
t_{IS2}	Input (through F_n)	CK +	F ±		20	10		
t_{IS3}	Input (through Complement Array)[4]	CK +	(I,B) ±		65	40		
Hold time								
t_{IH1}	Input	CK +	(I,B) ±	$C_L = 30pF$	0	−10		ns
t_{IH2}		CK +	F ±		15	10		
Propagation delays								
t_{CKO}	Clock	F ±	CK +	$C_L = 30pF$		25	30	ns
t_{OE1}	Output enable	F −	$\overline{OE}$ −	$C_L = 30pF$		20	30	
t_{OD1}	Output disable[3]	F +	$\overline{OE}$ +	$C_L = 5pF$		20	30	
t_{PD}	Output	B ±	(I,B) ±	$C_L = 30pF$		40	50	
t_{OE2}	Output enable	B ±	(I,B) +	$C_L = 30pF$		35	55	
t_{OD2}	Output disable[3]	B +	(I,B) −	$C_L = 5pF$		30	35	
t_{PRO}	Preset/Reset	F ±	(I,B) +	$C_L = 30pF$		50	55	

NOTES:

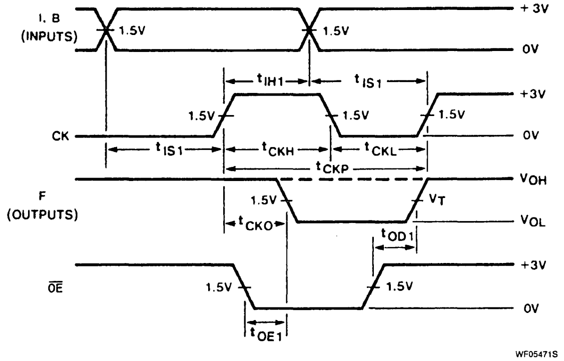
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ≤ 10ns.
3. Measured at $V_T = V_{OL} + 0.5V$.
4. When using the Complement Array $T_{CKP} = 95ns$ (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.
6. For test circuits, waveforms and timing diagrams see the following pages.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS155

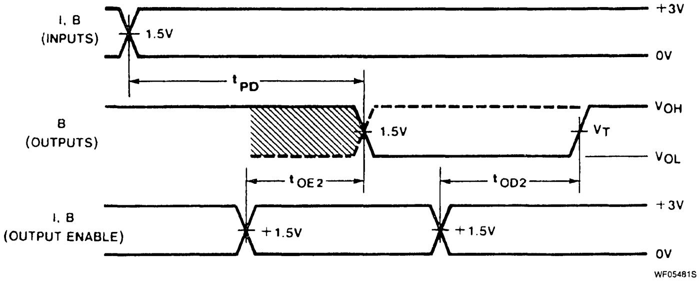
TEST LOAD CIRCUITS



TIMING DIAGRAMS



Flip-Flop Outputs

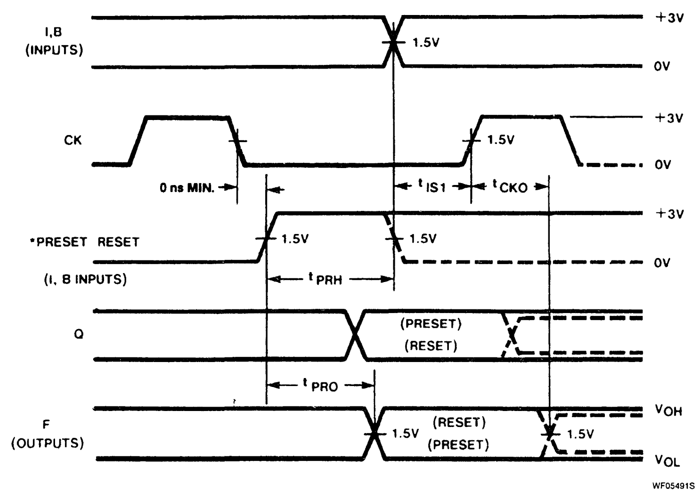


Gate Outputs

TIMING DEFINITIONS

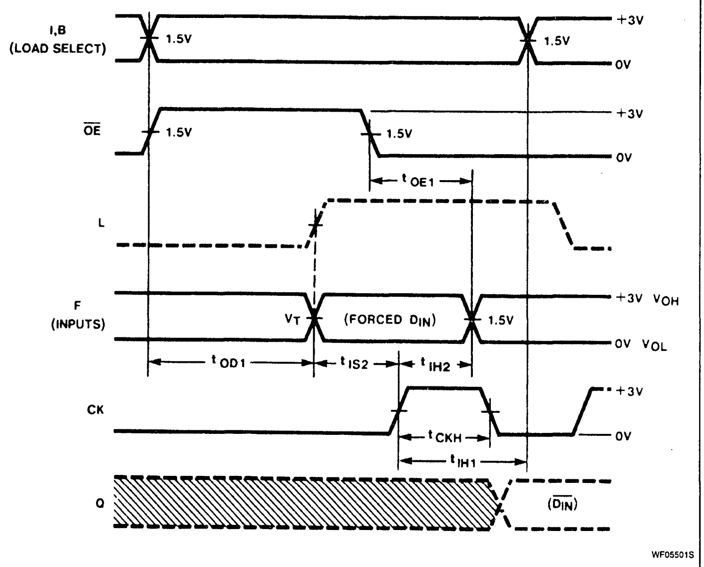
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational Outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low, and when combinational Outputs are in the OFF-state.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



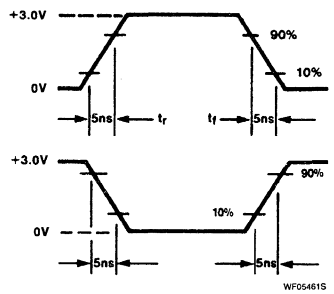
* The leading edge of preset/reset must occur only when the input clock is "low", and must remain "high" as long as required to override clock. The falling edge of preset/reset can never go "low" when the input clock is "high".

Asynchronous Preset/Reset



Flip-Flop Input Mode

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS155

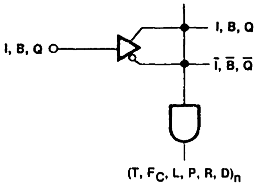
LOGIC PROGRAMMING

PLS155 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLS155 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

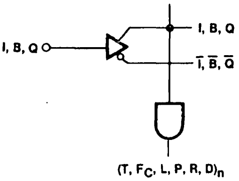
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (B), (Q_p)



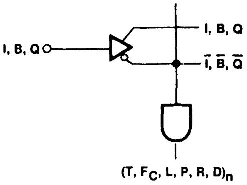
STATE	CODE
INACTIVE[1,2]	O

LS02030S



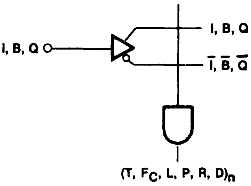
STATE	CODE
I, B, Q	H

LS02040S



STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

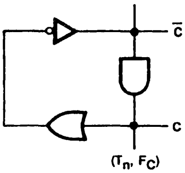
LS02050S



STATE	CODE
DON'T CARE	–

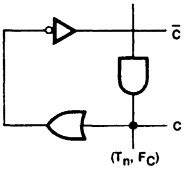
LS02060S

"COMPLEMENT" ARRAY – (C)



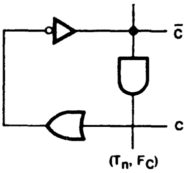
ACTION	CODE
INACTIVE[1,3,5]	O

LS02070S



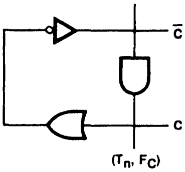
ACTION	CODE
GENERATE[5]	A

LS02080S



ACTION	CODE
PROPAGATE	•

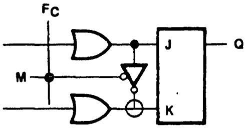
LS02090S



ACTION	CODE
TRANSPARENT	–

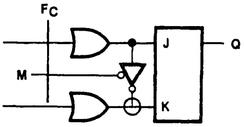
LS02100S

"OR" ARRAY – (F-F CONTROL MODE)



ACTION	CODE
J/K OR D (CONTROLLED)	A

LS02130S



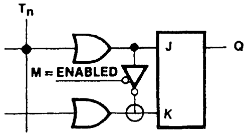
ACTION	CODE
J·K	•

LS02140S

Notes on following page.

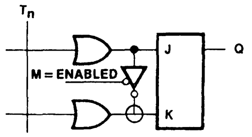
Field-Programmable Logic Sequencer (16 × 45 × 12) PLS155

"OR" ARRAY – (Q_n = D-Type)



T_n STATUS	CODE
ACTIVE (Set)	A

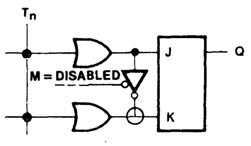
LS02150S



T_n STATUS	CODE
INACTIVE (Reset)	●

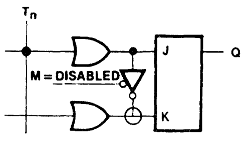
LS02160S

"OR" ARRAY – (Q_n = J-K Type)



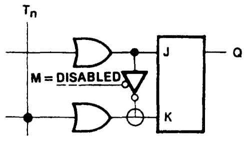
ACTION	CODE
TOGGLE	O

LS02170S



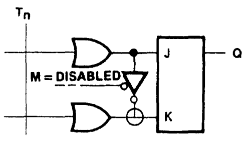
ACTION	CODE
SET	H

LS02180S



ACTION	CODE
RESET	L

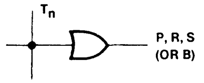
LS02190S



ACTION	CODE
HOLD	–

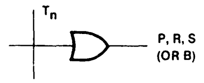
LS02200S

"OR" ARRAY – (S or B), (P), (R)



T_n STATUS	CODE
ACTIVE	A

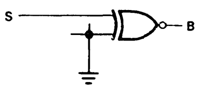
LS02210S



T_n STATUS	CODE
INACTIVE	●

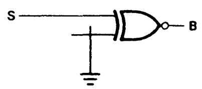
LS02220S

"EX-OR" ARRAY – (B)



POLARITY	CODE
LOW	L

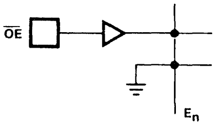
LS02230S



POLARITY	CODE
HIGH	H

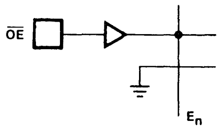
LS02240S

"$\overline{OE}$" ARRAY – (E)



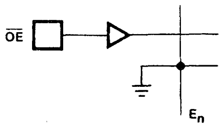
ACTION	CODE
IDLE[4]	O

LS02250S



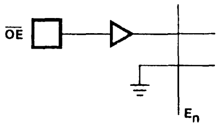
ACTION	CODE
CONTROL	A

LS02260S



ACTION	CODE
ENABLE[4]	●

LS02270S



ACTION	CODE
DISABLE	–

LS02280S

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)$_n$ will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)$_n$ due to their lack of "OR" array links.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS155

FPLS PROGRAM TABLE

AND

INACTIVE	O
I, B, Q	H
$\overline{I}, \overline{B}, \overline{Q}$	L
DON'T CARE	–

I, B (I), Q (P)

INACTIVE	O
GENERATE	A
PROPAGATE	•
TRANSPARENT	–

C

OR

ACTIVE	A
INACTIVE	•

P, R, B (O), (Q = D)

TOGGLE	O
SET	H
RESET	L
HOLD	–

(Q = J/K)

CONTROL

J/K	•
J/K or D (controlled)	A

F/F MODE

IDLE	O
CONTROL	A
ENABLE	•
DISABLE	–

$E_{A, B}$

HIGH	H
LOW	L

(POL)

NOTES

1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (—). Program unused Q, B, P, and R bits in the OR array as (—) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) ____________

CUSTOMER SYMBOLIZED PART # ____________

DATE RECEIVED ____________

COMMENTS ____________

CUSTOMER NAME ____________

PURCHASE ORDER # ____________

SIGNETICS DEVICE # ____________

TOTAL NUMBER OF PARTS ____________

PROGRAM TABLE # ________ REV ________ DATE ________

																		F/F MODE				E_B	E_A			POLARITY							
		AND																OR															
	C	I				B(I)								Q(P)				Q(N)				P		R		B(O)							
TERM		3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0	3	2	1	0	B	A	B	A	7	6	5	4	3	2	1	0
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D5																																	
D4																																	
D3																																	
D2																																	
D1																																	
D0																																	
PIN		5	4	3	2	19	18	13	12	9	8	7	6	17	16	15	14																

TB01211S

Signetics

PLS157
Field-Programmable Logic Sequencer (16 × 45 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLS157 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 6 registered I/O outputs (F) in conjunction with 6 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

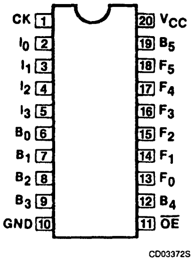
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

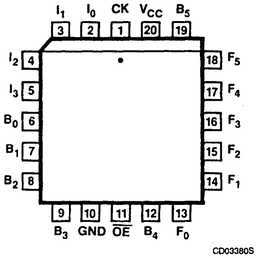
- f_{MAX} = 14MHz
  - 18.2MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 6 bidirectional I/O lines
- 6 bidirectional registers
- J-K, T, or D-type flip-flops
- 3-State outputs
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: −100μA (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible

PIN CONFIGURATIONS

N Package



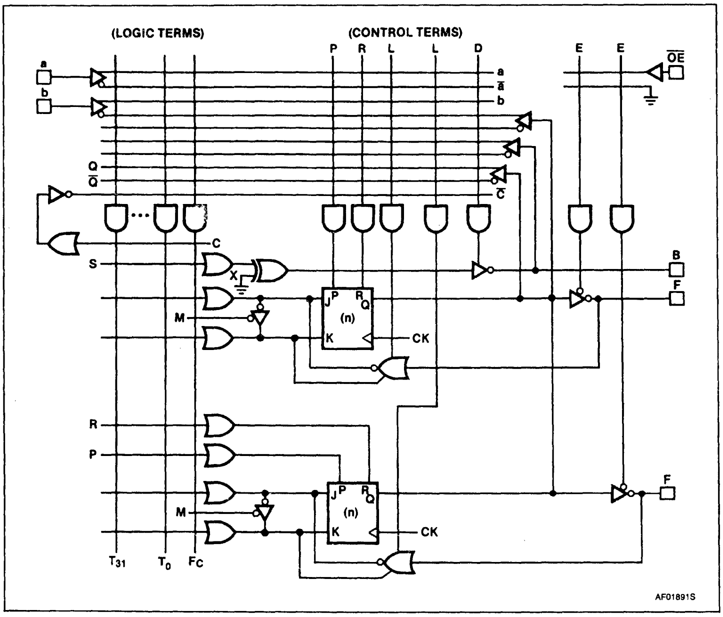
A Package



APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

FUNCTIONAL DIAGRAM



Field-Programmable Logic Sequencer (16 × 45 × 12) PLS157

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops. The Asynchronous Preset and Reset lines (P, R), for two of the registers are driven from the AND matrix. The Preset and Reset lines (P, R) controlling the lower four registers are driven from the OR matrix.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS157 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

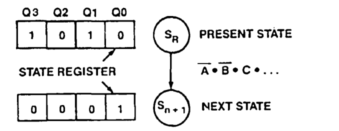
Order codes are listed in the Ordering Information Table.

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J/K only or J/K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

LOGIC FUNCTION



SET Q_0: $J_0 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 - (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

TOGGLE Q_3: $J_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

TB00901S

NOTES:
Similar logic functions are applicable for D and T mode flip-flops.

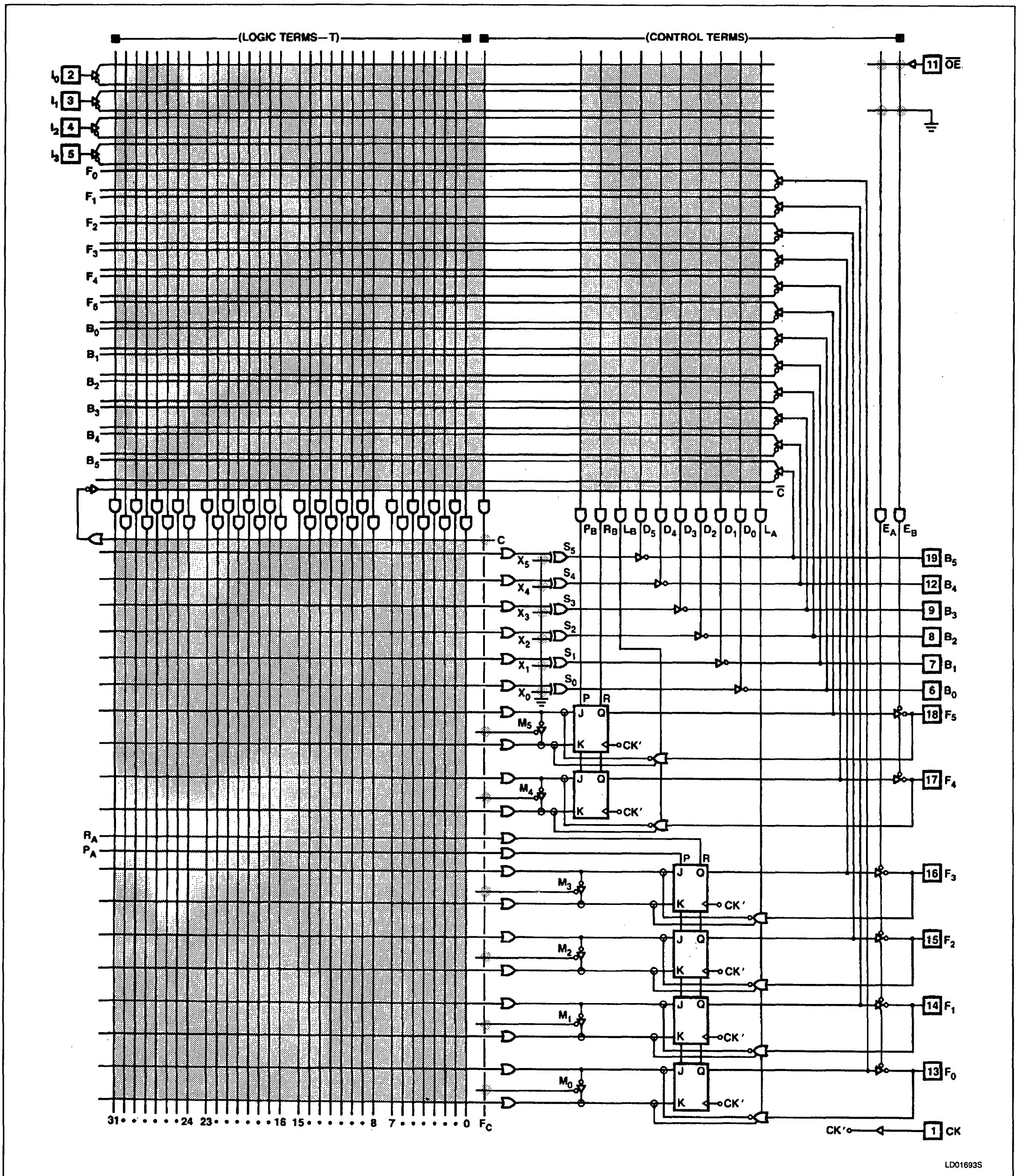
FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:
1. Positive Logic:
   $J/K = T_0 + T_1 + T_2$ .... T_{31}
   $T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (Q_0 \bullet Q_1 \ldots) \bullet (B_0 \bullet B_1 \bullet \ldots)$
2. ↑denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active T_n disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. * * = Forced at F_n pin to load J/K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS157

FPLS LOGIC DIAGRAM



NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. Programmable connection.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS157

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLS157N
20-pin Plastic Leaded Chip Carrier	PLS157A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High	I_{OH} = −2mA	2.4			V
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	80	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
Output current						
		V_{CC} = Max				
$I_{O\ (OFF)}$	Hi-Z state[5, 6]	V_{OUT} = 5.5V		1	80	µA
		V_{OUT} = 0.45V		−1	−140	µA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[4]	V_{CC} = Max		150	190	mA
Capacitance						
		V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
5. Leakage values are a combination of input and output leakage.
6. Measured with V_{IH} applied to $\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.

AC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

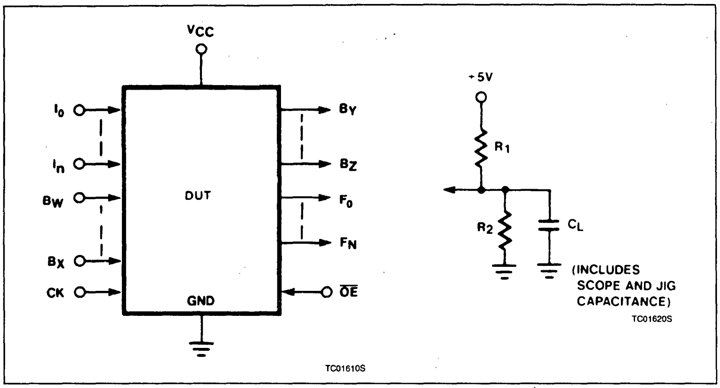
SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min[5]	Typ[1]	Max	
Pulse width								
t_{CKH}	Clock[2] High	CK −	CK +	$C_L = 30pF$	25	20		ns
t_{CKL}	Clock Low	CK +	CK −		30	20		
t_{CKP}	Period	CK +	CK +		70	50		
t_{PRH}	Preset/Reset pulse	(I,B) +	(I,B) −		40	30		
Setup time								
t_{IS1}	Input	CK +	(I,B) ±	$C_L = 30pF$	40	30		ns
t_{IS2}	Input (through F_n)	CK +	F ±		20	10		
t_{IS3}	Input (through Complement Array)[4]	CK +	(I,B) ±		65	40		
Hold time								
t_{IH1}	Input	CK +	(I,B) ±	$C_L = 30pF$	0	−10		ns
t_{IH2}		CK +	F ±		15	10		
Propagation delays								
t_{CKO}	Clock	F ±	CK +	$C_L = 30pF$		25	30	ns
t_{OE1}	Output enable	F −	$\overline{OE}$ −	$C_L = 30pF$		20	30	
t_{OD1}	Output disable[3]	F +	$\overline{OE}$ +	$C_L = 5pF$		20	30	
t_{PD}	Output	B ±	(I,B) ±	$C_L = 30pF$		40	50	
t_{OE2}	Output enable	B ±	(I,B) +	$C_L = 30pF$		35	55	
t_{OD2}	Output disable[3]	B +	(I,B) −	$C_L = 5pF$		30	35	
t_{PRO}	Preset/Reset	F ±	(I,B) +	$C_L = 30pF$		50	55	

NOTES:

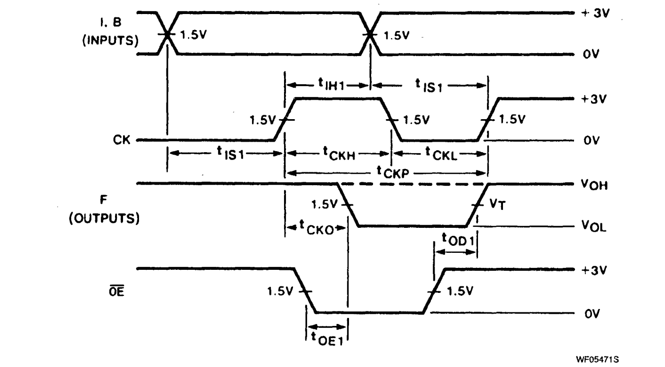
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) $\leqslant$ 10ns.
3. Measured at $V_T = V_{OL} + 0.5V$.
4. When using the Complement Array $T_{CKP} = 95ns$ (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.
6. For test circuits, waveforms and timing diagrams see the following pages.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS157

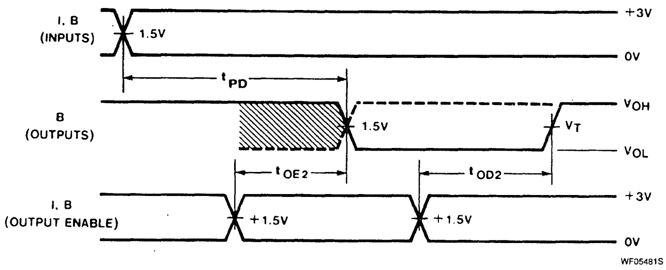
TEST LOAD CIRCUITS



TIMING DIAGRAMS



Flip-Flop Outputs

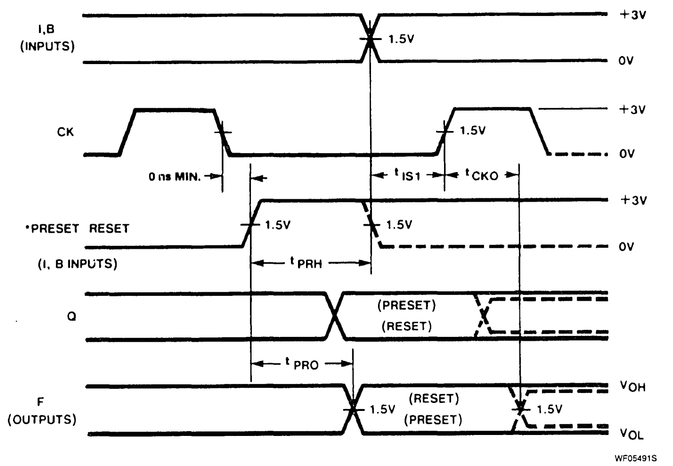


Gate Outputs

TIMING DEFINITIONS

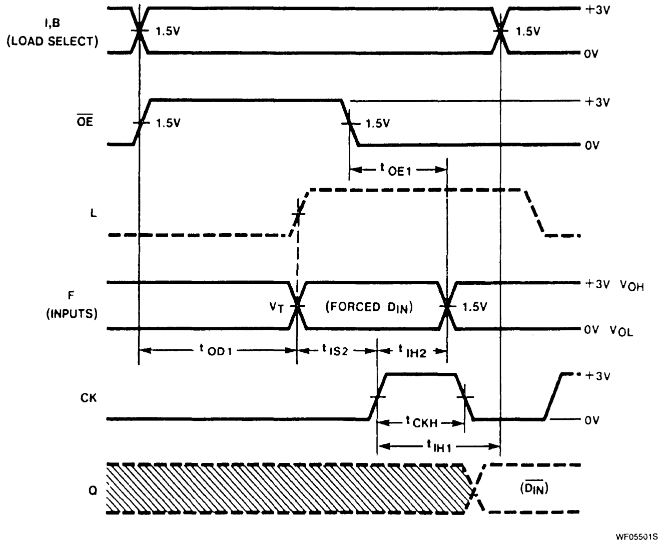
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational Outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low, and when combinational Outputs are in the OFF-state.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



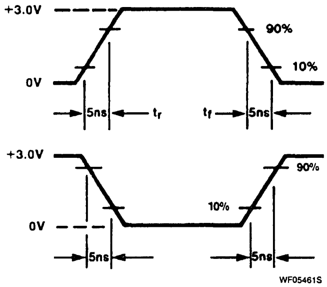
* The leading edge of preset/reset must occur only when the input clock is "low", and must remain "high" as long as required to override clock. The falling edge of preset/reset can never go "low" when the input clock is "high".

Asynchronous Preset/Reset



Flip-Flop Input Mode

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

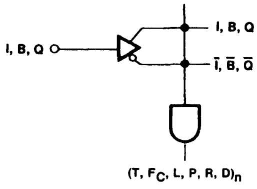
LOGIC PROGRAMMING

PLS157 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLS157 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

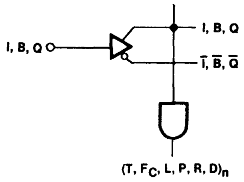
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (B), (Q_p)



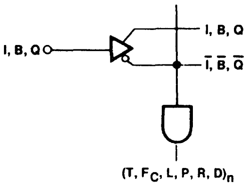
STATE	CODE
INACTIVE[1,2]	O

LS02030S



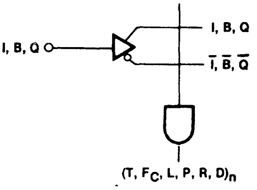
STATE	CODE
I, B, Q	H

LS02040S



STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

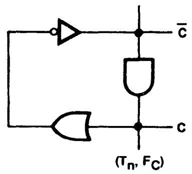
LS02050S



STATE	CODE
DON'T CARE	–

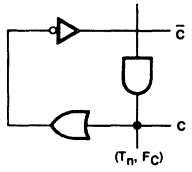
LS02060S

"COMPLEMENT" ARRAY – (C)



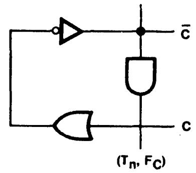
ACTION	CODE
INACTIVE[1,3,5]	O

LS02070S



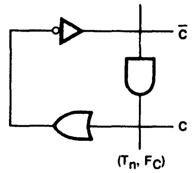
ACTION	CODE
GENERATE[5]	A

LS02080S



ACTION	CODE
PROPAGATE	•

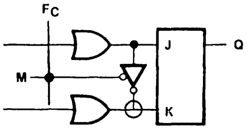
LS02090S



ACTION	CODE
TRANSPARENT	–

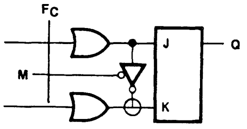
LS02100S

"OR" ARRAY – (F-F CONTROL MODE)



ACTION	CODE
J/K OR D (CONTROLLED)	A

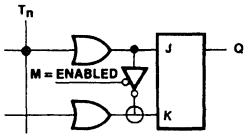
LS02130S



ACTION	CODE
J-K	•

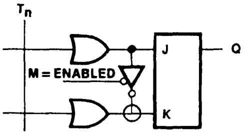
LS02140S

"OR" ARRAY – (Q_n = D-Type)



T_n STATUS	CODE
ACTIVE (Set)	A

LS02150S

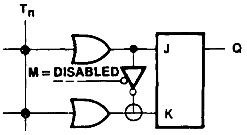


T_n STATUS	CODE
INACTIVE (Reset)	•

LS02160S

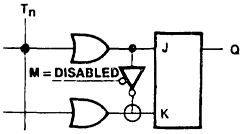
Notes on following page.

"OR" ARRAY – (Q_n = J-K Type)



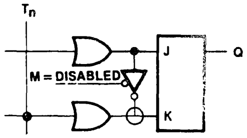
ACTION	CODE
TOGGLE	O

LS02170S



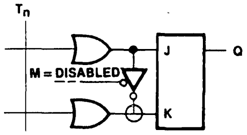
ACTION	CODE
SET	H

LS02180S



ACTION	CODE
RESET	L

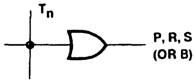
LS02190S



ACTION	CODE
HOLD	–

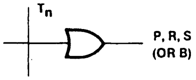
LS02200S

"OR" ARRAY – (S or B), (P), (R)



T_n STATUS	CODE
ACTIVE	A

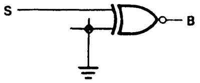
LS02210S



T_n STATUS	CODE
INACTIVE	•

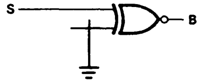
LS02220S

"EX-OR" ARRAY – (B)



POLARITY	CODE
LOW	L

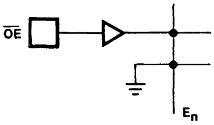
LS02230S



POLARITY	CODE
HIGH	H

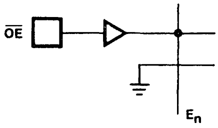
LS02240S

"$\overline{OE}$" ARRAY – (E)



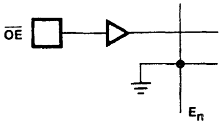
ACTION	CODE
IDLE[4]	O

LS02250S



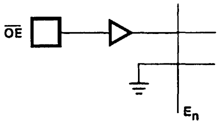
ACTION	CODE
CONTROL	A

LS02260S



ACTION	CODE
ENABLE[4]	•

LS02270S



ACTION	CODE
DISABLE	–

LS02280S

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)$_n$ will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)$_n$ due to their lack of "OR" array links.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS157

FPLS PROGRAM TABLE

AND

INACTIVE	O	
I, B, Q	H	I, B (I), Q (P)
$\overline{I}, \overline{B}, \overline{Q}$	L	
DON'T CARE	–	

INACTIVE	O	
GENERATE	A	C
PROPAGATE	•	
TRANSPARENT	–	

OR

ACTIVE	A	P, R, B (O), (Q = D)
INACTIVE	•	

TOGGLE	O	
SET	H	(Q = J/K)
RESET	L	
HOLD	–	

CONTROL

J/K	•	F/F MODE
J/K or D (controlled)	A	

IDLE	O	
CONTROL	A	$E_{A, B}$
ENABLE	•	
DISABLE	–	

HIGH	H	(POL.)
LOW	L	

F/F MODE					

NOTES
1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (—). Program unused Q, B, P, and R bits in the OR array as (—) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

E_B	E_A

POLARITY					

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) ____

CUSTOMER SYMBOLIZED PART # ____

DATE RECEIVED ____

COMMENTS ____

CUSTOMER NAME ____

PURCHASE ORDER # ____

SIGNETICS DEVICE # ____

TOTAL NUMBER OF PARTS ____

PROGRAM TABLE # ____ REV ____ DATE ____

TERM	AND																	OR													
	C	I				B(I)						Q (P)						Q (N)						P	R	B(O)					
		3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	A	A	5	4	3	2	1	0
0																															
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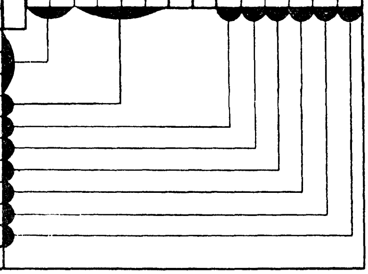
31																															
F_C																															
P_B																															
R_B																															
L_B																															
L_A																															
D5																															
D4																															
D3																															
D2																															
D1																															
D0																															
PIN		5	4	3	2	19	12	9	8	7	6	18	17	16	15	14	13														



TB01350S

Signetics

PLS159A
Field-Programmable Logic Sequencer (16 × 45 × 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 20

DESCRIPTION

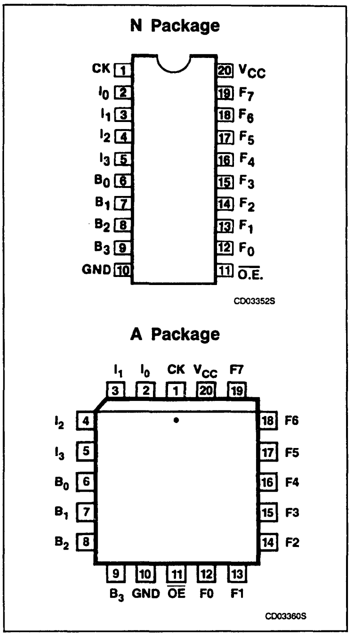
The PLS159A is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- High-speed version of PLS159
- f_{MAX} = 18MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J-K, T, or D-type flip-flops
- Power-on reset feature on all flip-flops ($F_n = 1$)
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: $-100\mu A$ (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible
- 3-State outputs

PIN CONFIGURATIONS

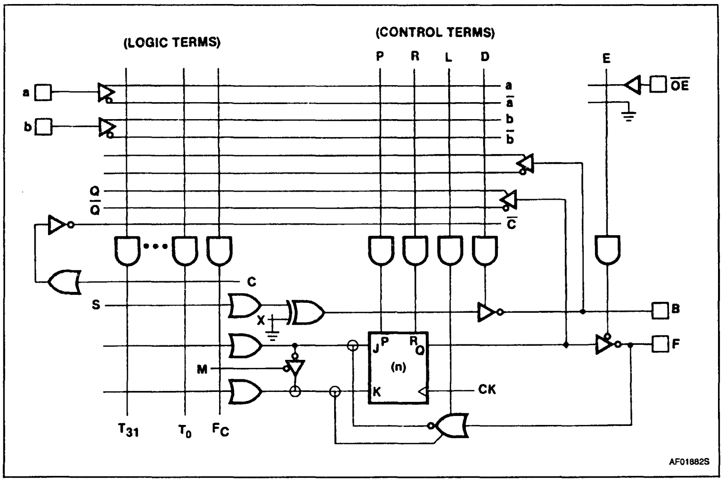

N Package

A Package

APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

FUNCTIONAL DIAGRAM



Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of Ex-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R).

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS159A is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

VIRGIN STATE

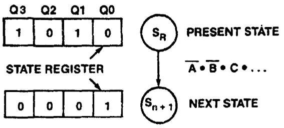
The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

CAUTION: PLS159A PROGRAMMING ALGORITHM

The programming voltage required to program the PLS159A is higher (17.5V) then that required to program the PLS159 (14.5V). Consequently, the PLS159 programming algorithm will not program the PLS159A. Please exercise caution when accessing programmer device codes to insure that the correct algorithm is used.

LOGIC FUNCTION



SET Q_0: $J_0 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

TOGGLE Q_3: $J_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

TB00901S

NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

FLIP-FLOP TRUTH TABLE

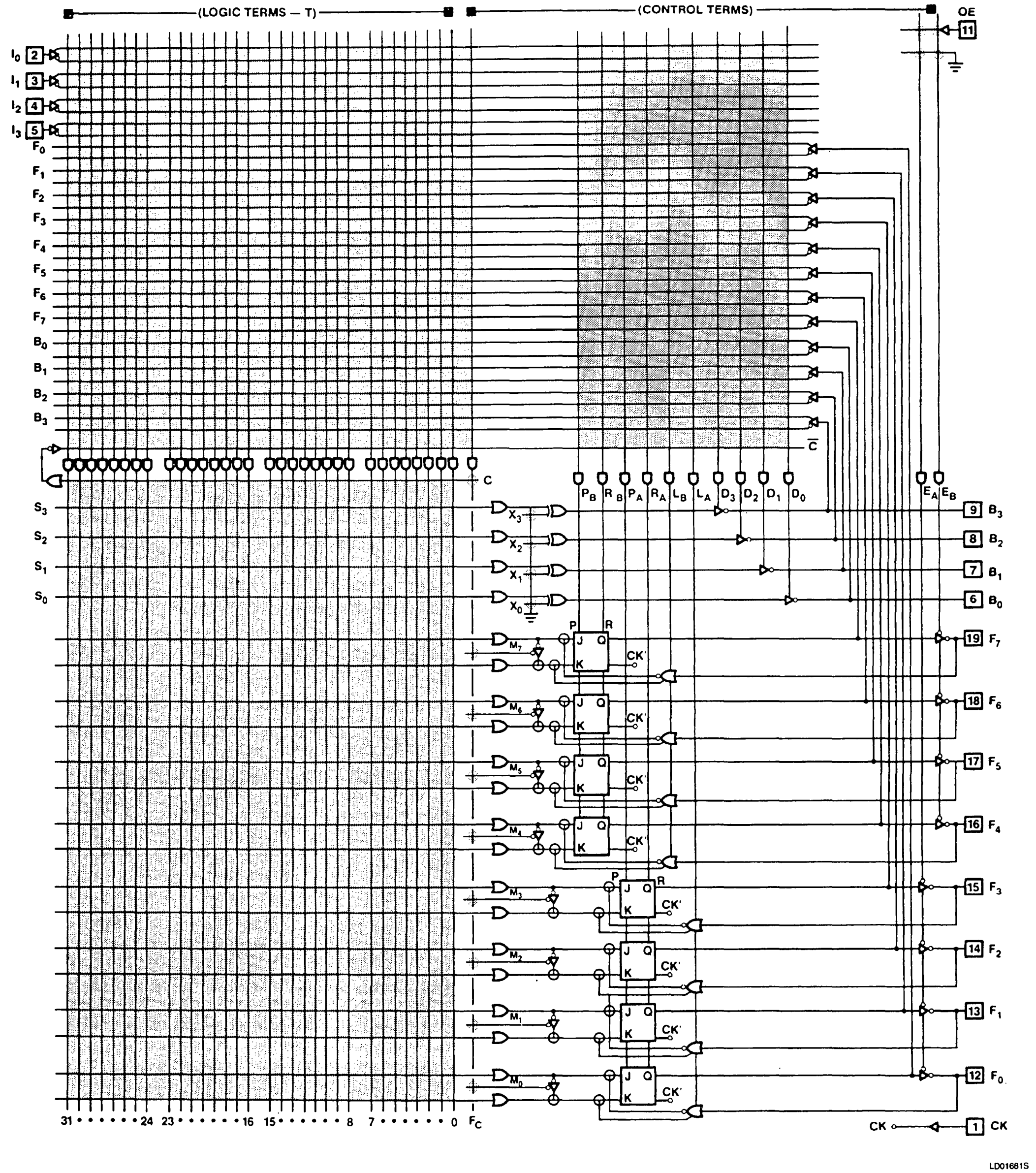
$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	L	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:

1. Positive Logic:
   J-K = $T_0 + T_1 + T_2$ .... T_{31}
   $T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (Q_0 \bullet Q_1 \ldots) \bullet (B_0 \bullet B_1 \bullet \ldots)$
2. ↑denotes transition from Low to High level.
3. X = Don't Care
4. * = Forced at F_n pin for loading J-K flip-flop in I/O mode. L must be enabled, and other active T_n disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. * * = Forced at F_n pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

FPLS LOGIC DIAGRAM



NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ◌ Programmable connection.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLS159AN
20-pin Plastic Leaded Chip Carrier	PLS159AA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = Min, I_{OH} = −2mA	2.4			V
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{CC} = Max, V_{IN} = 5.5V		< 1	40	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
Output current						
$I_{O(OFF)}$	Hi-Z state[4, 7]	V_{CC} = Max, V_{OUT} = 5.5V		1	80	μA
		V_{OUT} = 0.45V		−1	−140	μA
I_{OS}	Short circuit[3, 5]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[6]	V_{CC} = Max		150	190	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IH} applied to $\overline{OE}$.
5. Duration of short circuit should not exceed 1 second.
6. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
7. Leakage values are a combination of input and output leakage.

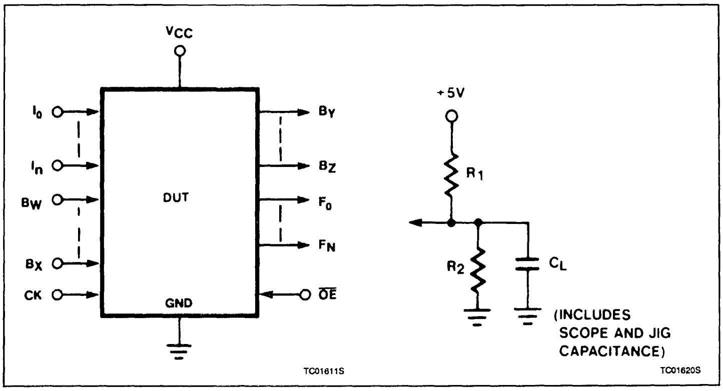
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min[5]	Typ[1]	Max	
Pulse width								
t_{CKH}	Clock[2] High	CK −	CK +	$C_L = 30pF$	20	15		ns
t_{CKL}	Clock Low	CK +	CK −	$C_L = 30pF$	20	15		
t_{CKP}	Period	CK +	CK +	$C_L = 30pF$	55	45		
t_{PRH}	Preset/Reset pulse	(I, B) +	(I, B) −	$C_L = 30pF$	35	30		
Setup time								
t_{IS1}	Input	CK +	(I, B) ±	$C_L = 30pF$	35	30		ns
t_{IS2}	Input (through F_n)	CK +	F ±	$C_L = 30pF$	15	10		
t_{IS3}	Input (through Complement Array)[4]	CK +	(I, B) ±	$C_L = 30pF$	55	45		
Hold time								
t_{IH1}	Input	CK +	(I, B) ±	$C_L = 30pF$	0	−5		ns
t_{IH2}	Input (through F_n)	CK +	F ±	$C_L = 30pF$	15	10		
Propagation delay								
t_{CKO}	Clock	F ±	CK +	$C_L = 30pF$		15	20	ns
t_{OE1}	Output enable	F −	$\overline{OE}$ −	$C_L = 30pF$		20	30	
t_{OD1}	Output disable[3]	F +	$\overline{OE}$ +	$C_L = 5pF$		20	30	
t_{PD}	Output	B ±	(I, B) ±	$C_L = 30pF$		25	35	
t_{OE2}	Output enable	B ±	(I, B) +	$C_L = 30pF$		20	30	
t_{OD2}	Output disable[3]	B +	(I, B) −	$C_L = 5pF$		20	30	
t_{PRO}	Preset/Reset	F ±	(I, B) +	$C_L = 30pF$		35	45	
t_{PPR}	Power-on/preset	F −	V_{CC}+	$C_L = 30pF$		0	10	

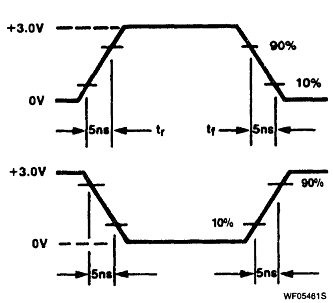
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ≤ 10ns.
3. Measured at $V_T = V_{OL} + 0.5V$.
4. When using the Complement Array $T_{CKP} = 75ns$ (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS

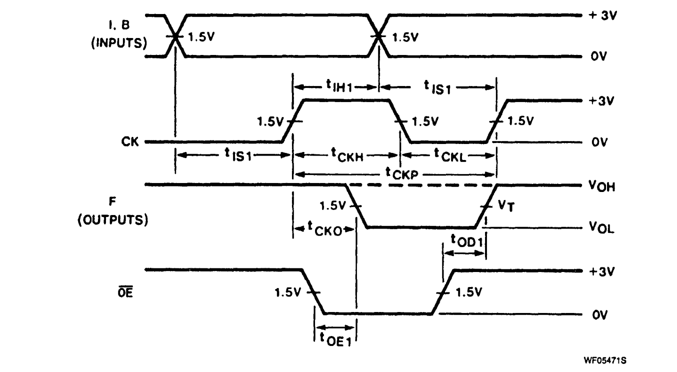


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

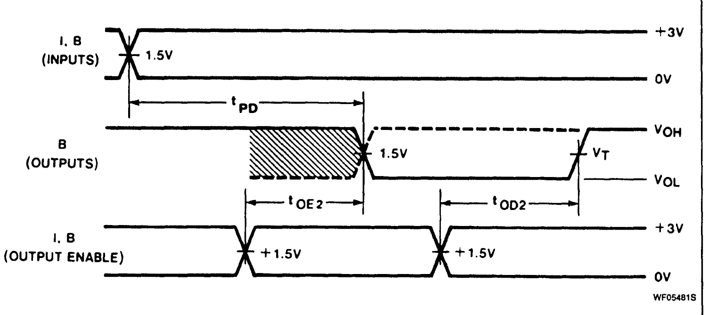
Input Pulses

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

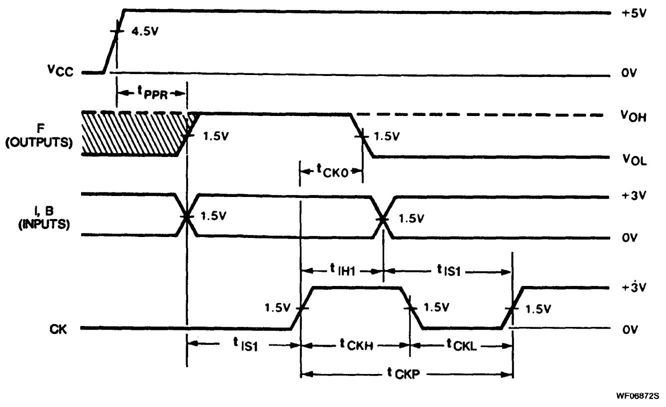
TIMING DIAGRAMS



Flip-Flop Outputs



Gate Outputs

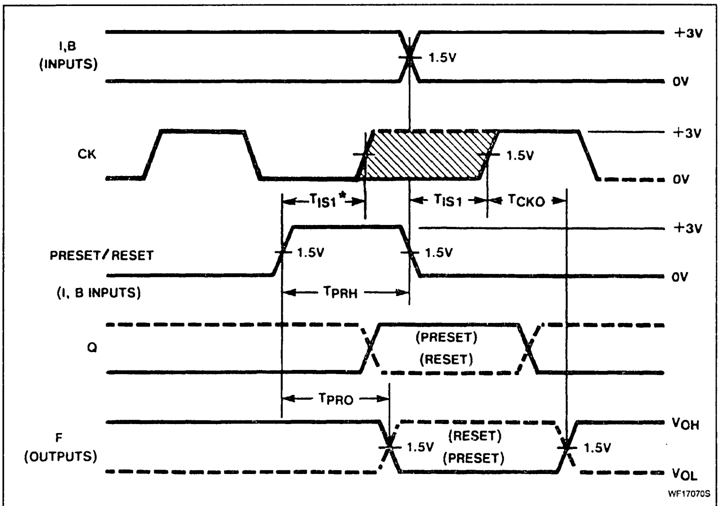


Power-On Reset

TIMING DEFINITIONS

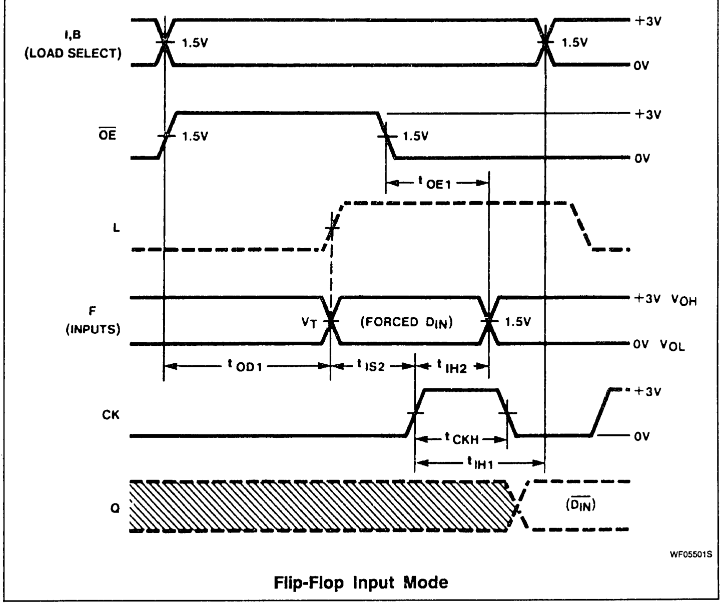
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the OFF-state.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the OFF-state.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



* Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if T_{IS1} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Flip-Flop Input Mode

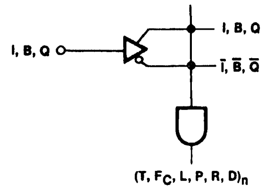
LOGIC PROGRAMMING

PLS159A logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLS159A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

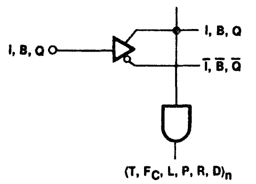
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY — (I), (B), (Qp)



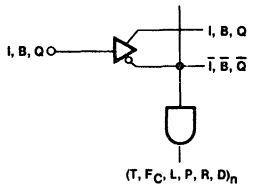
STATE	CODE
INACTIVE[1, 2]	O

LS02032S



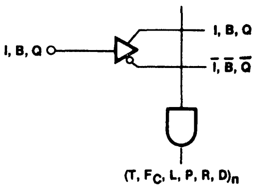
STATE	CODE
I, B, Q	H

LS02040S



STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

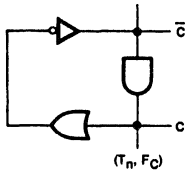
LS02050S



STATE	CODE
DON'T CARE	–

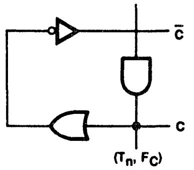
LS02060S

"COMPLEMENT" ARRAY — (C)



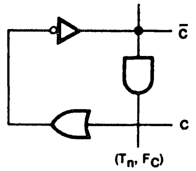
ACTION	CODE
INACTIVE[1, 3, 5]	O

LS02072S



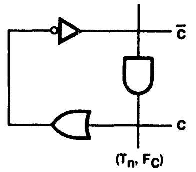
ACTION	CODE
GENERATE[5]	A

LS02080S



ACTION	CODE
PROPAGATE	●

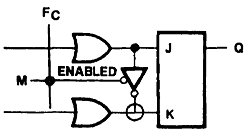
LS02090S



ACTION	CODE
TRANSPARENT	–

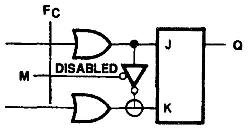
LS02100S

"OR" ARRAY — (F-F CONTROL MODE)



ACTION	CODE
J-K OR D (CONTROLLED)[1]	A

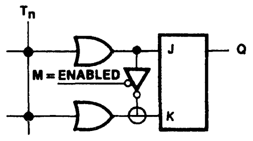
LS02131S



ACTION	CODE
J-K ONLY	●

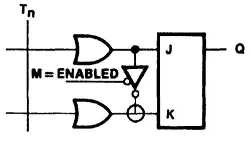
LS02141S

"OR" ARRAY — (Q_n = D - Type)



T_n STATUS	CODE
ACTIVE (Set)[1]	A

LS02151S



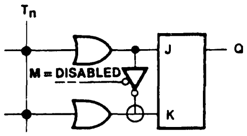
T_n STATUS	CODE
INACTIVE (Reset)	●

LS02160S

CAUTION:
The PLS159A Programming Algorithm is different from the PLS159.

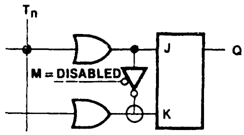
Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

"OR" ARRAY — (Q_n = J - K Type)



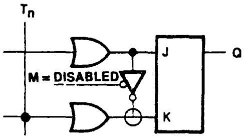
ACTION	CODE
TOGGLE	O

LS02170S



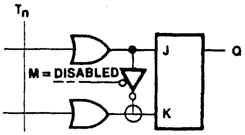
ACTION	CODE
SET	H

LS02180S



ACTION	CODE
RESET	L

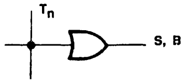
LS02190S



ACTION	CODE
HOLD	–

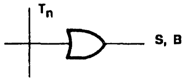
LS02200S

"OR" ARRAY — (S or B)



T_n STATUS	CODE
ACTIVE[1]	A

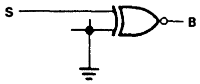
LS02211S



T_n STATUS	CODE
INACTIVE	•

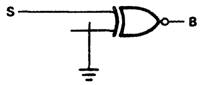
LS02221S

"EX-OR" ARRAY — (B)



POLARITY	CODE
LOW	L

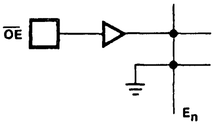
LS02230S



POLARITY	CODE
HIGH	H

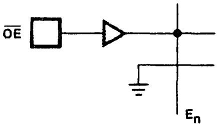
LS02240S

"OE " ARRAY — (E)



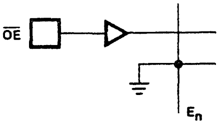
ACTION	CODE
IDLE[1, 4]	O

LS02252S



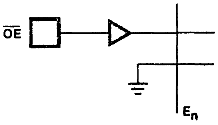
ACTION	CODE
CONTROL	A

LS02260S



ACTION	CODE
ENABLE[4]	•

LS02270S



ACTION	CODE
DISABLE	–

LS02280S

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)$_n$ will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link, pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)$_n$ due to their lack of "OR" array links.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

FPLS PROGRAM TABLE

AND

INACTIVE	O	I, B (I), Q (P)
I, B, Q	H	
Ī, B̄, Q̄	L	
DON'T CARE	—	
INACTIVE	O	C
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

OR

ACTIVE	A	P, R, B (O), (Q = D)
INACTIVE	•	
TOGGLE	O	(Q = J/K)
SET	H	
RESET	L	
HOLD	—	

CONTROL

J/K	•	F/F MODE
J/K or D (controlled)	A	
HIGH	H	(POL.)
LOW	L	

IDLE	O	$E_{A,B}$
CONTROL	A	
ENABLE	•	
DISABLE	—	

NOTES
1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and Q bits in the AND array as (—). Program unused Q, B, P, and R bits in the OR array as (—) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

F/F MODE	E_B	E_A	POLARITY

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) ____

CUSTOMER SYMBOLIZED PART # ____

DATE RECEIVED ____

COMMENTS ____

CUSTOMER NAME ____

PURCHASE ORDER # ____

SIGNETICS DEVICE # ____

TOTAL NUMBER OF PARTS ____

PROGRAM TABLE # ____ REV ____ DATE ____

TERM	C	AND																(OR)											
		I				B(I)				Q (P)								Q (N)								B(O)			
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0
0																													
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F_C																													
P_B																													
R_B																													
L_B																													
P_A																													
R_A																													
L_A																													
D3																													
D2																													
D1																													
D0																													
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12												

TB01291S

Signetics

PLS167
Field-Programmable Logic Sequencer (14 × 48 × 6)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLS167 is a bipolar, programmable state machine of the Mealy type. The Field Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 8 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND Array combines 14 external inputs, I_{0-13}, with 8 internal inputs, P_{0-7}, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P_0 and P_1 of the internal State Register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR Array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse.

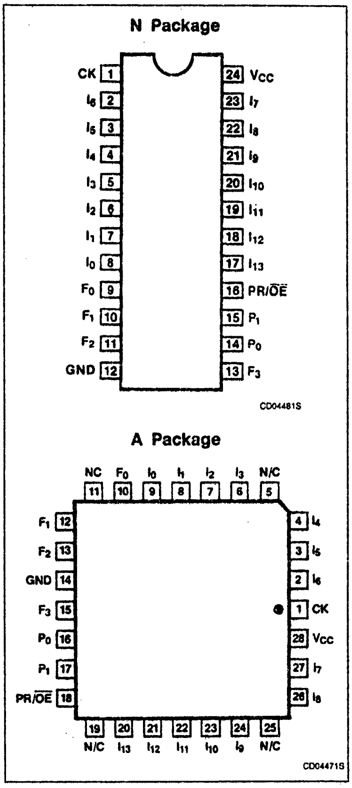
Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to Output-Enable function, as an additional user programmable option.

Order codes are listed in the Ordering Information Table.

FEATURES

- **f_{MAX}: 13.9MHz**
  - **- 20MHz clock rate**
- **Field-Programmable (Ni-Cr link)**
- **14 True/Complement buffered inputs**
- **48 programmable AND gates**
- **25 programmable OR gates**
- **8-bit State Register**
- **2-bit shared State/Output Register**
- **4-bit Output Register**
- **Transition Complement Array**
- **Programmable Asynchronous Preset/Output Enable**
- **Positive edge-triggered clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On-chip Test Array**
- **Power: 600mW (typ.)**
- **TTL compatible**
- **3-State outputs**
- **Single +5V supply**
- **300mil-wide 24-pin DIP**

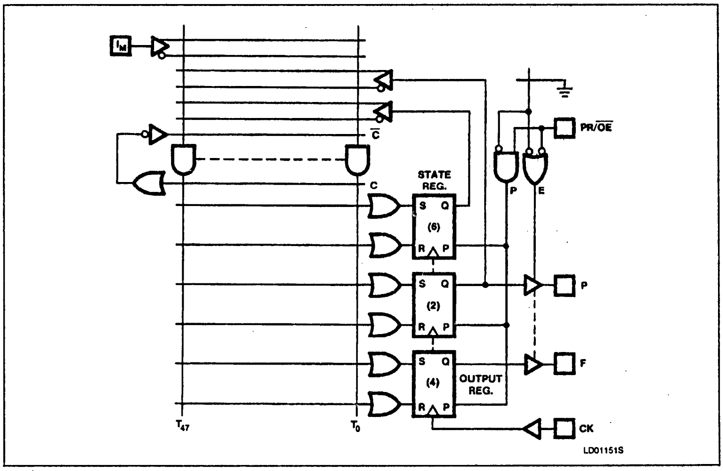
PIN CONFIGURATIONS



APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Security locking systems**

FUNCTIONAL DIAGRAM



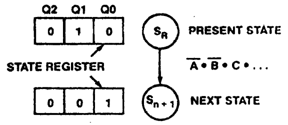
Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2–7 17–23	I_{1-13}	**Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
8	I_0	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-3} and P_{0-1} reflect the contents of State Register bits P_{2-7} (see Diagnostic Output Mode diagram). The contents of flip-flops P_{0-1} and F_{0-3} remain unaltered.	Active-High/Low
9–11 13	F_{0-3}	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of Output Register bits Q_{0-3}, when enabled. When I_0 is held at +10V, $F_{0-3} = (P_{2-5})$.	Active-High
14–15	P_{0-1}	**Logic/Diagnostic Outputs:** Two register bits with shared function as least significant State Register bits, or most significant Output Register bits. When I_0 is held at +10V, $P_{0-1} = (P_{6-7})$.	Active-High
16	PR/$\overline{\text{OE}}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and P_{0-1} and F_{0-3} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.	Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers.	Active-Low (L)

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

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TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION		I_O	CK	S	R	$Q_{P/F}$	F
	PR	$\overline{\text{OE}}$						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:

1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I_0\ I_1\ I_2 \ldots)\ (P_0\ P_1 \ldots P_7)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V
6. X = Don't Care (≤5.5V)

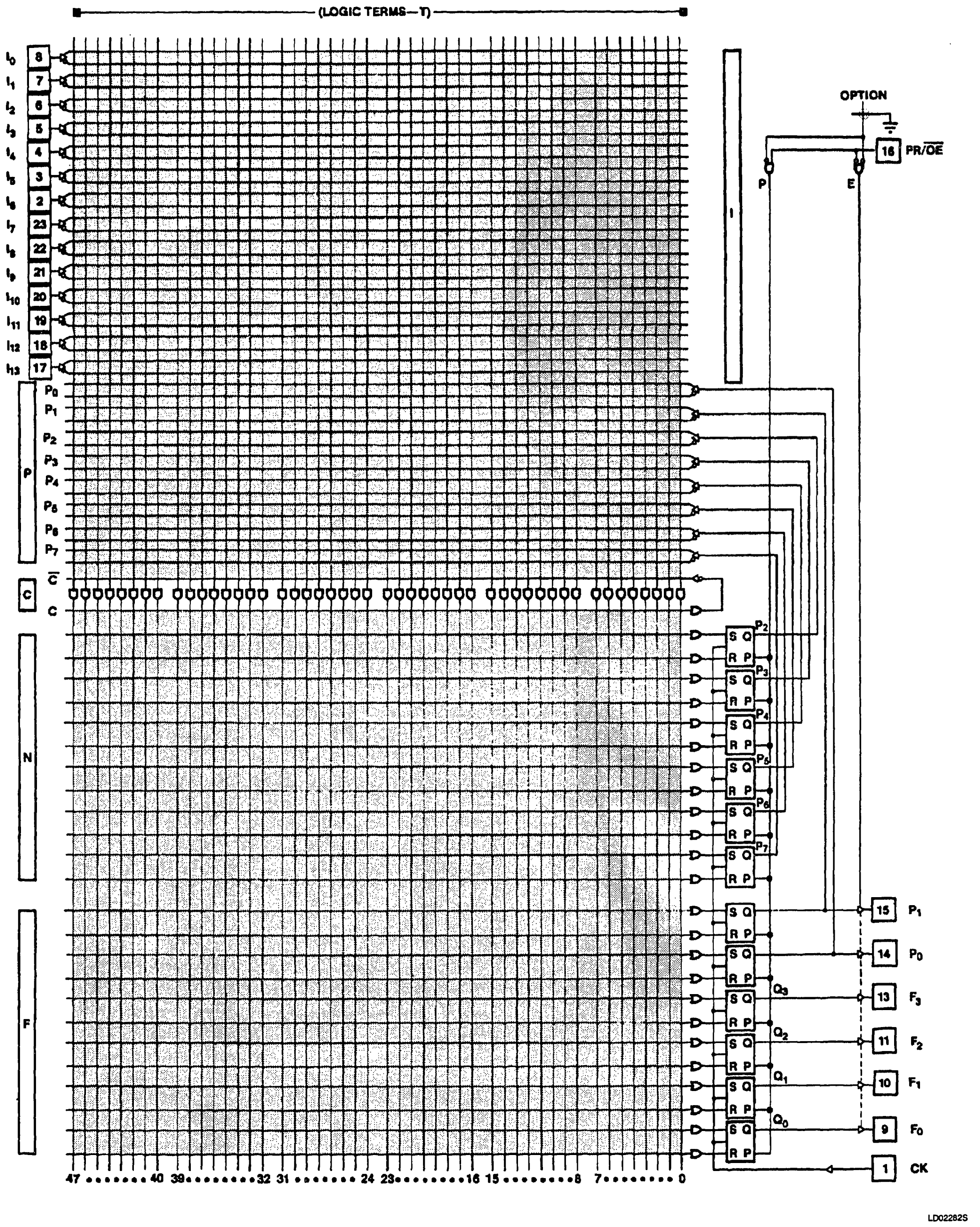
VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{\text{OE}}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.
   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

FPLS LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS167N
28-pin Plastic Leaded Chip Carrier	PLS167A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the dovico is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250	μA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	μA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = + 25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

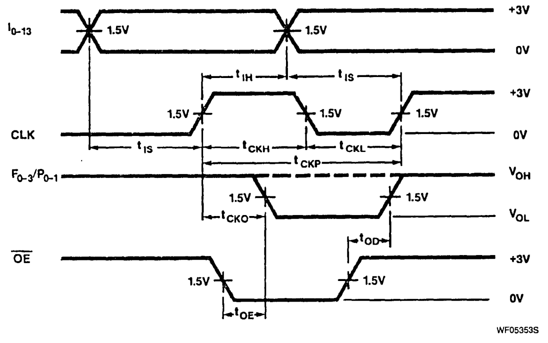
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Pulse width[3]							
t_{CKH}	Clock[2] High	CK −	CK +	25	15		ns
t_{CKL}	Clock Low	CK +	CK −	25	15		
$t_{CKP1}B$	Period (without Complement Array)	CK +	CK +	80	40		
$t_{CKP2}B$	Period (with Complement Array)	CK +	CK +	120	60		
t_{PRH}	Preset pulse	PR −	PR +	25	15		
Setup time[3]							
$t_{IS1}A$	Input	CK +	Input ±	60			ns
$t_{IS1}B$	Input	CK +	Input ±	50			
$t_{IS1}C$	Input	CK +	Input ±	42			
$t_{IS2}A$	Input (through Complement Array)	CK +	Input ±	90			
$t_{IS2}B$	Input (through Complement Array)	CK +	Input	80			
$t_{IS2}C$	Input (through Complement Array)	CK +	Input	72			
t_{VS}	Power-on preset	CK −	V_{CC} +	0	−10		
t_{PRS}	Preset	CK −	PR −	0	−10		
Hold time							
t_{IH}	Input	Input ±	CK +	5	−10		ns
Propagation delay							
t_{CKO}	Clock	Output ±	CK +		15	30	ns
t_{OE}	Output enable	Output −	OE −		20	30	
t_{OD}	Output disable	Output +	OE +		20	30	
t_{PR}	Preset	Output +	PR +		18	30	
t_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	
Frequency of operation[3]							
$f_{MAX}C$	Without Complement Array					13.9	MHz
$f_{MAX}C$	With Complement Array					9.8	

NOTES:

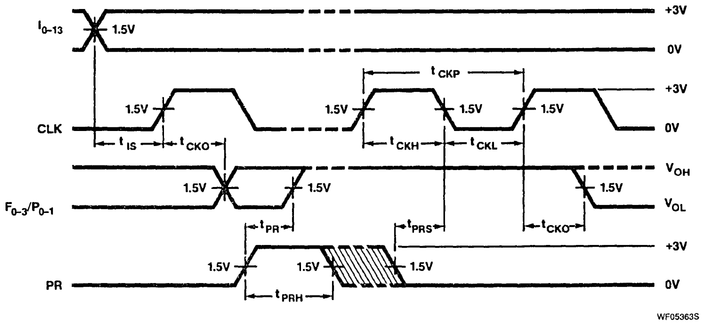
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ⩽ 30ns.
3. Soo "Speed vs. OR Loading" diagrams.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

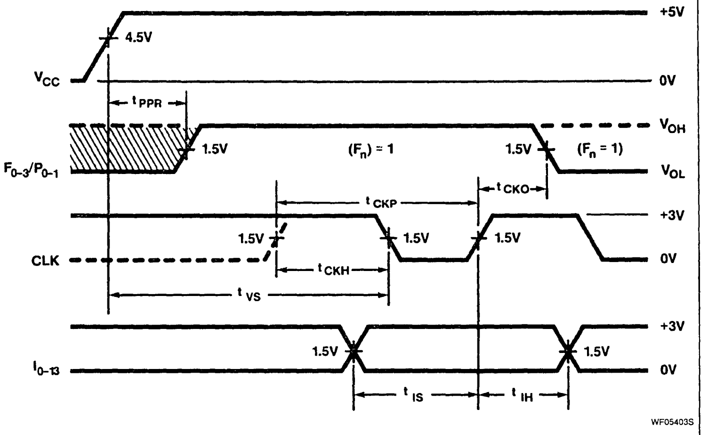
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset



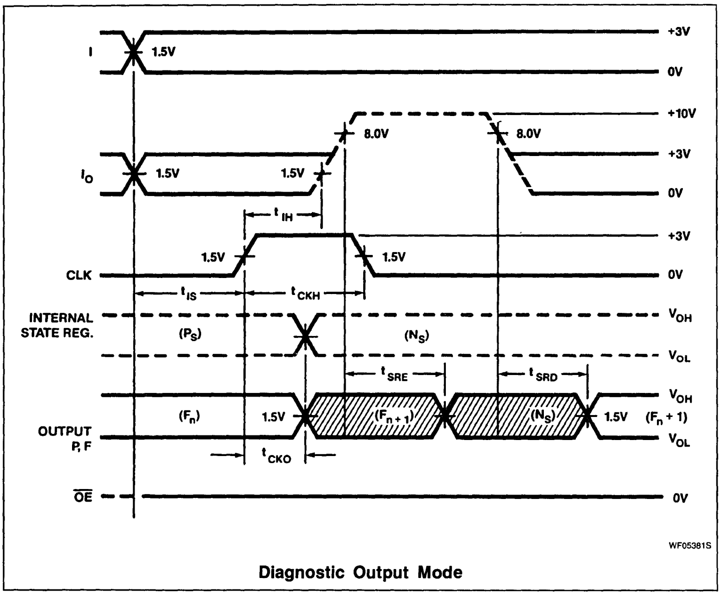
Power-On Preset

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Clock period – when not using Complement array.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{CKP2}	Clock period – when using complement array.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid Input data.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{SRE}	Delay between input I_0 transition to Diagnostic mode and when the Outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

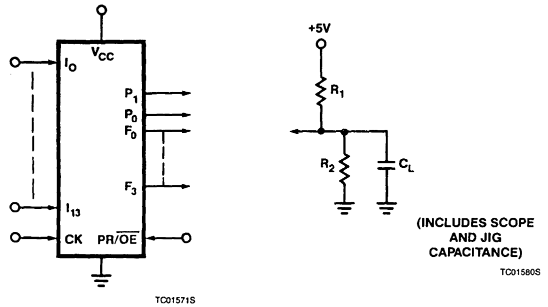
Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

TIMING DIAGRAMS (Continued)

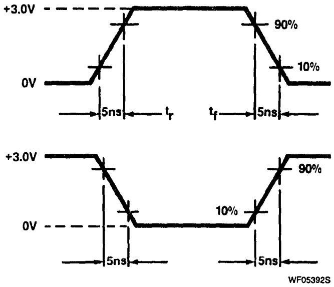


Diagnostic Output Mode

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

SPEED VS. "OR" LOADING

The maximum frequency at which the FPLS can be clocked while operating in *sequential mode* is given by:

$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The AC electrical characteristics contain three limits for the parameters t_{IS1} and t_{IS2}. The first, t_{IS1A} is guaranteed for a device with 48 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 32 terms connected to any OR line. And t_{IS1C} is guaranteed for a device with 24 terms connected to any OR line.

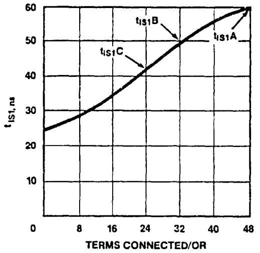


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Figure 1. t_{IS1} vs. Terms/OR Connected

The Three other entries in the AC table, t_{IS2} A, B, and C are corresponding 48, 32, and 24 term limits when using the on-chip Complement Array.

The worst case t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the FPLS logic diagram, typically illustrated in Figure 2, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

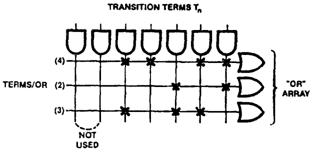

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Figure 2. Typical OR Array Interconnect Pattern

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

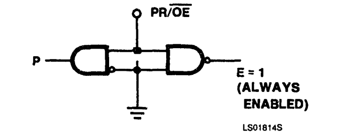
LOGIC PROGRAMMING

PLS167 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

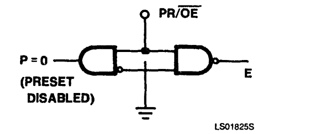
PLS167 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION – (P/E)



OPTION	CODE
PRESET[1]	H

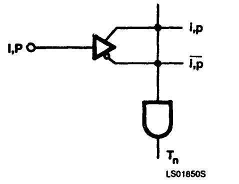


OPTION	CODE
$\overline{OE}$	L

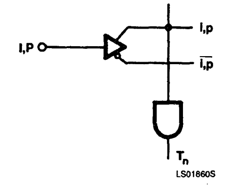
PROGRAMMING:

The PLS167 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

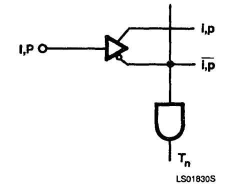
"AND" ARRAY – (I), (P)



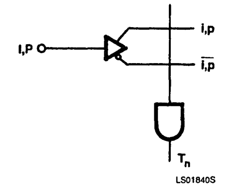
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, P	H

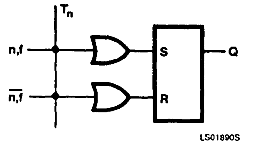


STATE	CODE
$\overline{I}$, $\overline{P}$	L

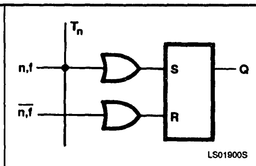


STATE	CODE
DON'T CARE	–

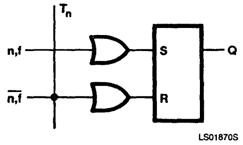
"OR" ARRAY – (N), (F)



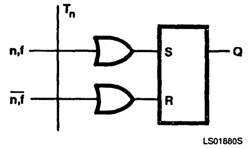
ACTION	CODE
INACTIVE[1,3]	O



ACTION	CODE
SET	H

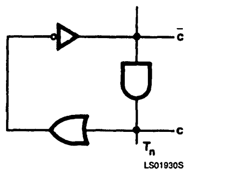


ACTION	CODE
RESET	L

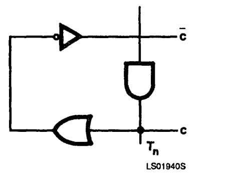


ACTION	CODE
NO CHANGE	–

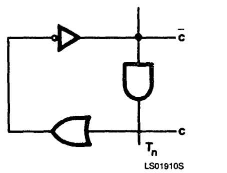
"COMPLEMENT" ARRAY – (C)



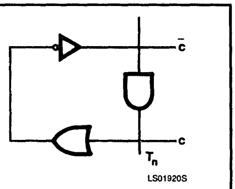
ACTION	CODE
INACTIVE[1,4]	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	–

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement of any input (I, P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To provent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

FPLS PROGRAM TABLE

CUSTOMER NAME ______________________

PURCHASE ORDER # ______________________

SIGNETICS DEVICE # CF (XXXX)

CUSTOMER SYMBOLIZED PART # ______________________

TOTAL NUMBER OF PARTS ______________________

PROGRAM TABLE # ______________________

REV ______________________

DATE ______________________

PROGRAM TABLE ENTRIES

AND

INACTIVE	0	Cn
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

INACTIVE	0	Im, Ps
I, P	H	
$\overline{I}$, $\overline{P}$	L	
DON'T CARE	—	

OR

INACTIVE	0	Ns, Fr
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
$\overline{OE}$	L	

	AND																								OPTION (P/E) OR											
TERM	Cn	INPUT (I_M)														PRESENT STATE (P_S)								REMARKS	NEXT STATE (N_S)								OUTPUT (Fr)			
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0
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PIN NO.		17	18	19	20	21	22	23	2	3	4	5	6	7	8																15	14	13	11	10	9
VARIABLE NAME																																				

TB01622S

NOTES:
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exits in the table, shown BLANK instead for clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (—).
3. Unused Transition Terms can be left for future code modification or programmed as (—) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

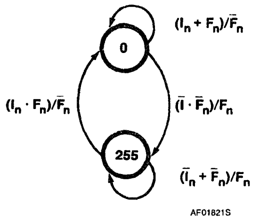
Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

TEST ARRAY

The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

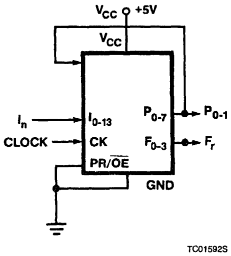
The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-13} as shown in the test circuit timing diagram.



0
255
$(I_n + F_n)/\bar{F}_n$
$(I_n \cdot F_n)/\bar{F}_n$
$(\bar{I} \cdot \bar{F}_n)/F_n$
$(\bar{I}_n + \bar{F}_n)/F_n$
AF01821S

State Diagram



FPLS Under Test

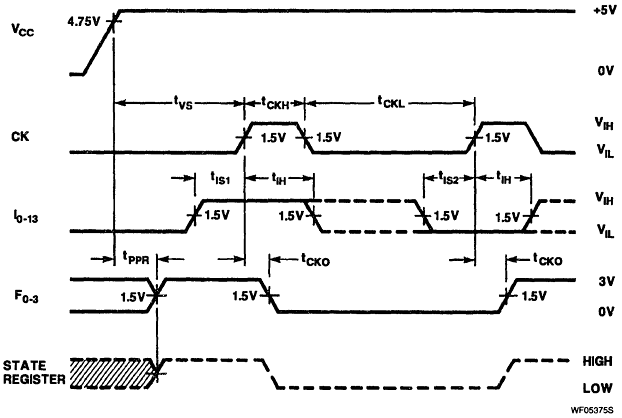
TERM	C	AND																					
		INPUT (Im)														PRESENT STATE (Ps)							
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)											H
OR											
NEXT STATE (Ns)								OUTPUT (Fr)			
7	6	5	4	3	2	1	0	3	2	1	0
L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H	H	H

TB01600S

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.



Test Circuit Timing Diagram

TERM	C	AND																					
		INPUT (Im)														PRESENT STATE (Ps)							
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)											H
OR											
NEXT STATE (Ns)								OUTPUT (Fr)			
7	6	5	4	3	2	1	0	3	2	1	0
–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–

TB01610S

Test Array Deleted

Signetics

PLS167A
Field-Programmable Logic Sequencer (14 × 48 × 6)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS167A is a bipolar, programmable state machine of the Mealy type.The Field-Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 8 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset Option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 14 external inputs, I_{0-13}, with 8 internal inputs, P_{0-7}, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P_0 and P_1 of the internal State Register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse.

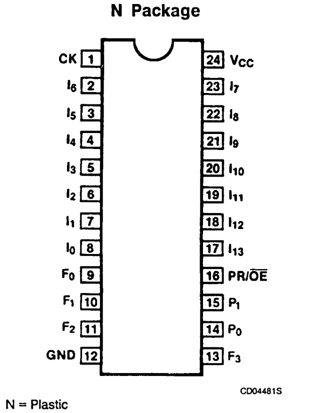
Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes are listed in the Ordering Information Table.

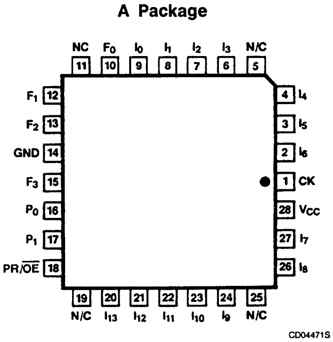
FEATURES

- **f_{MAX}: 20MHz**
  - **25MHz clock rate**
- **Field-Programmable (Ni-Cr link)**
- **14 True/Complement buffered inputs**
- **48 programmable AND gates**
- **25 programmable OR gates**
- **8-bit State Register**
- **2-bit shared State/Output Register**
- **4-bit Output Register**
- **Transition Complement Array**
- **Programmable Asynchronous Preset/Output Enable**
- **Positive edge-triggered clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On-chip Test Array**
- **Power: 600mW (typ.)**
- **TTL compatible**
- **3-State outputs**
- **Single +5V supply**
- **300mil-wide 24-pin DIP**

PIN CONFIGURATIONS



N = Plastic

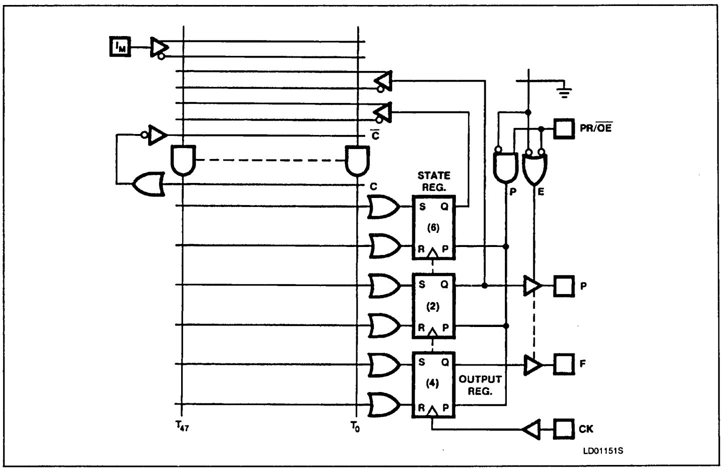


A = Plastic Leaded Chip Carrier

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Security locking systems**

FUNCTIONAL DIAGRAM



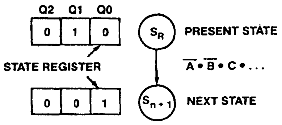
Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167A

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A low-to-high transition on this line is necessary to update the contents of both registers.	Active-High
2 – 7 17 – 23	I_{1-13}	**Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
8	I_0	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-3} and P_{0-1} reflect the contents of state register bits P_{2-7} (see Diagnostic Output Mode diagram). The contents of flip-flops P_{0-1} and F_{0-3} remain unaltered.	Active-High/Low
9 – 11 13	F_{0-3}	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of Output Register bits Q_{0-3}, when enabled. When I_0 is held at +10V, $F_{0-3} = (P_{2-5})$.	Active-High
14 – 15	P_{0-1}	**Logic/Diagnostic Outputs:** Two register bits with shared function as least significant State Register bits, or most significant Output Register bits. When I_0 is held at +10V, $P_{0-1} = (P_{6-7})$.	Active-High
16	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and P_{0-1} and F_{0-3} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.	Active High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers.	Active-Low (L)

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

TB00900S

TRUTH TABLE[1, 2, 3, 4, 5, 6]

V_{CC}	OPTION		I_0	CK	S	R	$Q_{P/F}$	F
	PR	$\overline{OE}$						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		I	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:

1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I_0\ I_1\ I_2 \ldots)\ \overline{(P_0\ P_1 \ldots P_7)}$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low-to-High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V
6. X = Don't care (⩽ 5.5V)

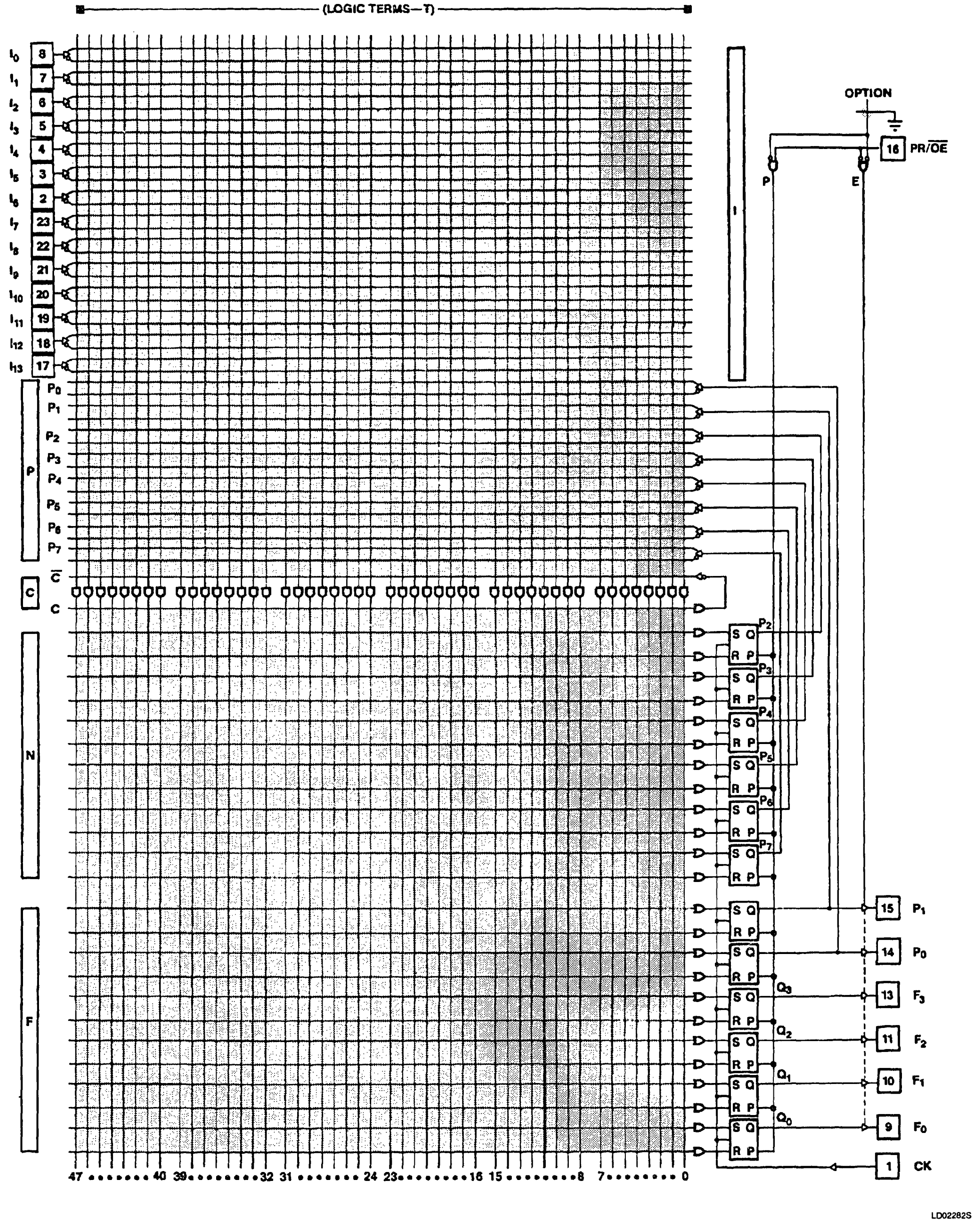
VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

FPLS LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown link float to a logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS167AN
28-pin Plastic Leaded Chip Carrier	PLS167AA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167A

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		−1	−40	µA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_A = + 25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167A

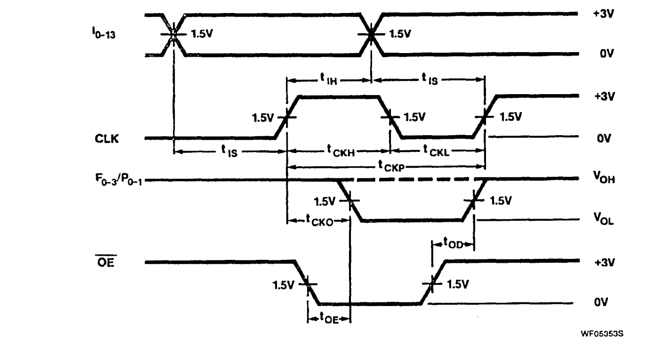
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Pulse width[3]							
t_{CKH}	Clock[2] High	CK −	CK +	20	15		ns
t_{CKL}	Clock Low	CK +	CK −	20	15		
$t_{CKP1}B$	Period (without Complement Array)	CK +	CK +	50	40		
$t_{CKP2}B$	Period (with Complement Array)	CK +	CK +	80	50		
t_{PRH}	Preset pulse	PR −	PR +	25	15		
Setup time[3]							
$t_{IS1}A$	Input	CK +	Input ±	40			ns
$t_{IS1}B$	Input	CK +	Input ±	30			
$t_{IS2}A$	Input (through Complement Array)	CK +	Input ±	70			
$t_{IS2}B$	Input (through Complement Array)	CK +	Input	60			
t_{VS}	Power-on preset	CK −	V_{CC} +	0	−10		
t_{PRS}	Preset	CK −	PR −	0	−10		
Hold time							
t_{IH}	Input	Input ±	CK +	5	−10		ns
Propagation delay							
t_{CKO}	Clock	Output ±	CK +		15	20	ns
t_{OE}	Output enable	Output −	OE −		20	30	
t_{OD}	Output disable	Output +	OE +		20	30	
t_{PR}	Preset	Output +	PR +		18	30	
t_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	
Frequency of operation[3]							
$f_{Max}B$	Without Complement Array					20.0	MHz
$f_{Max}B$	With Complement Array					12.5	

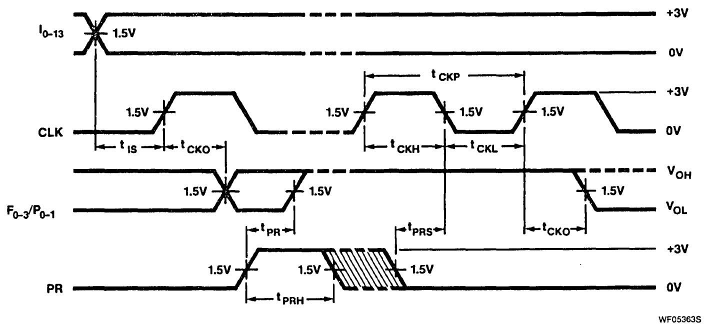
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ⩽ 30ns.
3. See "Speed vs. OR Loading" diagrams.

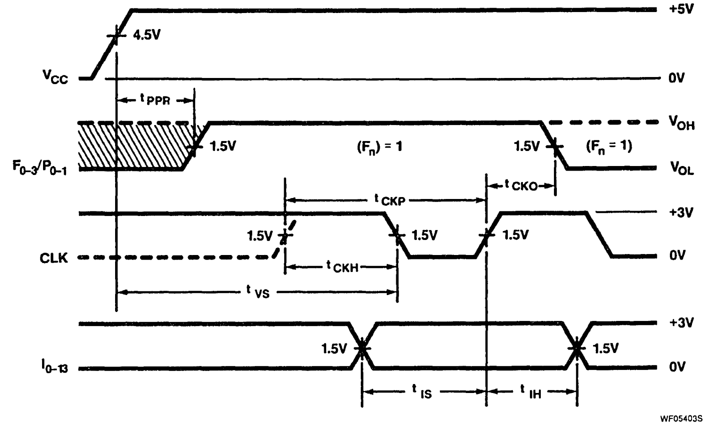
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset

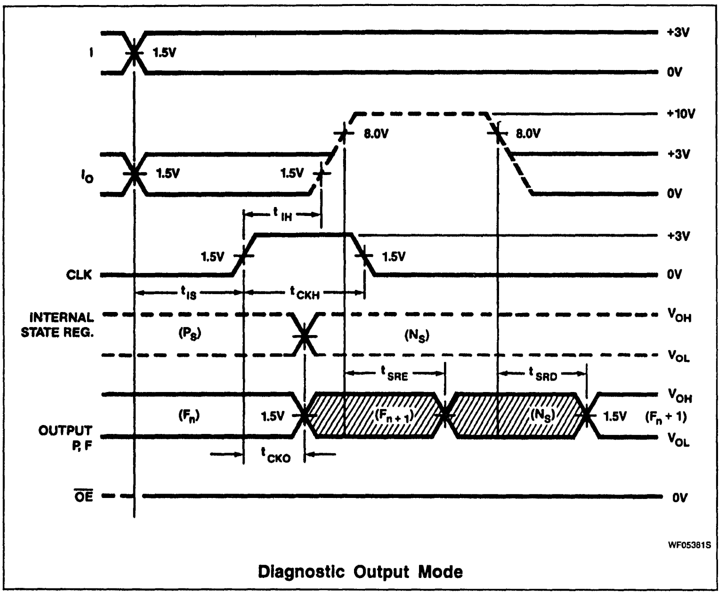


Power-On Preset

TIMING DEFINITIONS

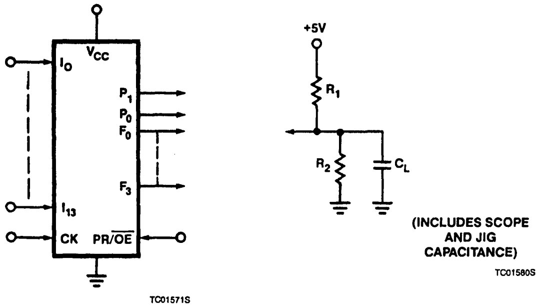
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Clock period – when not using Complement array.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{CKP2}	Clock period – when using complement array.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid Input data.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{SRE}	Delay between input I_0 transition to Diagnostic mode and when the Outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

TIMING DIAGRAMS (Continued)

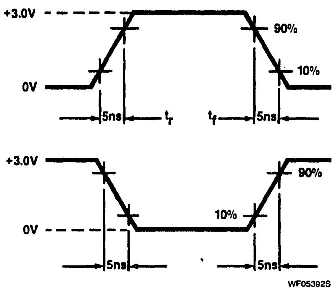


Diagnostic Output Mode

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167A

SPEED VS. "OR" LOADING

The maximum frequency at which the FPLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The AC electrical characteristics contain two limits for the parameters t_{IS1} and t_{IS2}. The first, t_{IS1A} is guaranteed for a device with 24 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 16 terms connected to any OR line.

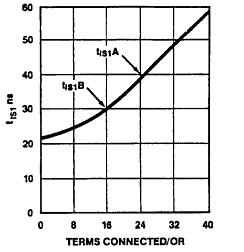


Figure 1. t_{IS1} vs. Terms/OR Connected

The three other entries in the AC table, t_{IS2} A and B are corresponding 24 and 16 term limits when using the on-chip Complement Array.

The worst case of t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the FPLS logic diagram, typically illustrated in Figure 2, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

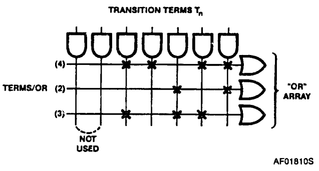


Figure 2. Typical OR Array Interconnect Pattern

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167A

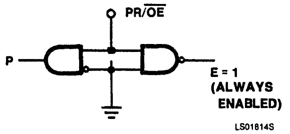
LOGIC PROGRAMMING

PLS167A logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

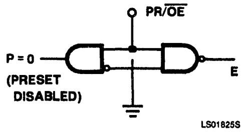
PLS167A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION – (P/E)



OPTION	CODE
PRESET[1]	H

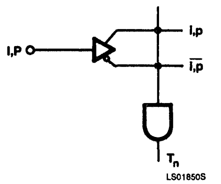


OPTION	CODE
$\overline{OE}$	L

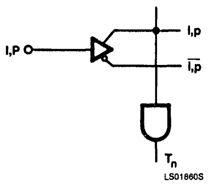
PROGRAMMING:

The PLS167A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

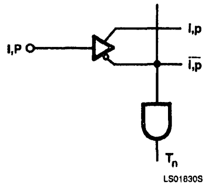
"AND" ARRAY – (I), (P)



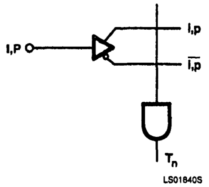
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, P	H

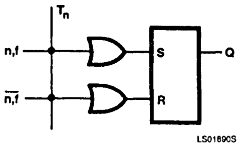


STATE	CODE
$\bar{I}$, $\bar{P}$	L

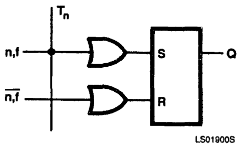


STATE	CODE
DON'T CARE	-

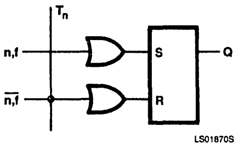
"OR" ARRAY – (N), (F)



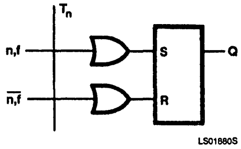
ACTION	CODE
INACTIVE[1,3]	O



ACTION	CODE
SET	H

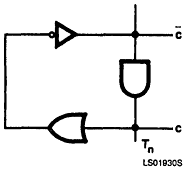


ACTION	CODE
RESET	L

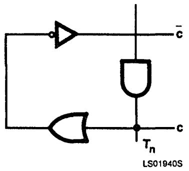


ACTION	CODE
NO CHANGE	-

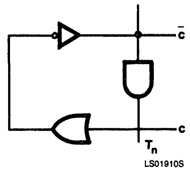
"COMPLEMENT" ARRAY – (C)



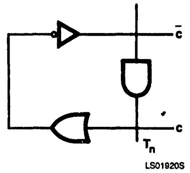
ACTION	CODE
INACTIVE[1,4]	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	-

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement of any input (I, P) are left intact.
3. To provont simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To provont oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167A

FPLS PROGRAM TABLE

CUSTOMER NAME ____________________

PURCHASE ORDER # ____________________

SIGNETICS DEVICE # CF (XXXX)

CUSTOMER SYMBOLIZED PART # ____________________

TOTAL NUMBER OF PARTS ____________________

PROGRAM TABLE # ____________________

REV ____________________

DATE ____________________

PROGRAM TABLE ENTRIES

AND

INACTIVE	0	C_n
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

INACTIVE	0	I_m, P_s
I, P	H	
$\bar{I}$, $\bar{P}$	L	
DON'T CARE	—	

OR

INACTIVE	0	N_s, F_r
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
$\overline{OE}$	L	

AND																									OPTION (P/E) OR											
TERM	C_n	INPUT (I_M)														PRESENT STATE (P_S)								REMARKS	NEXT STATE (N_S)								OUTPUT (F_r)			
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0
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47																																				
PIN NO.		17	18	19	20	21	22	23	2	3	4	5	6	7	8																15	14	13	11	10	9
VARIABLE NAME																																				

TB01622S

NOTES:

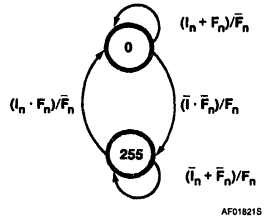
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused C_n, I_m, and P_s bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic programmers.

TEST ARRAY

The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

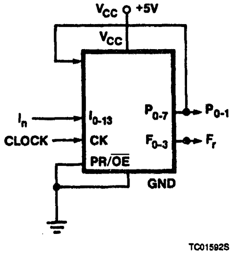
The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-13} as shown in the test circuit timing diagram.



$(I_n + F_n)/\bar{F}_n$
0
$(I_n \cdot F_n)/\bar{F}_n$
$(\bar{I} \cdot \bar{F}_n)/F_n$
255
$(\bar{I}_n + \bar{F}_n)/F_n$
AF01821S

State Diagram



FPLS Under Test

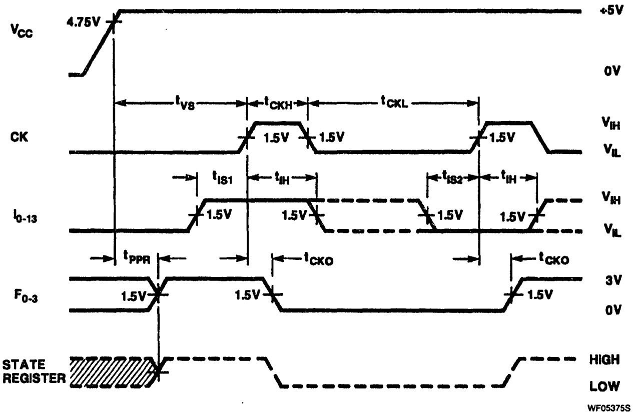
TERM	C	INPUT (Im)														PRESENT STATE (Ps)							
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)											H
OR											
NEXT STATE (Ns)								OUTPUT (Fr)			
7	6	5	4	3	2	1	0	3	2	1	0
L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H	H	H

TB01600S

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.



Test Circuit Timing Diagram

TERM	C	INPUT (Im)														PRESENT STATE (Ps)							
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)											H
OR											
NEXT STATE (Ns)								OUTPUT (Fr)			
7	6	5	4	3	2	1	0	3	2	1	0
–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–

TB01610S

Test Array Deleted

Signetics

PLS168
Field-Programmable Logic Sequencer (12 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLS168 is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 10 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, I_{0-11}, with 10 internal inputs, P_{0-9}, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P_0-P_3 of the internal State Register are brought off-chip to allow extending the Output Register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse.

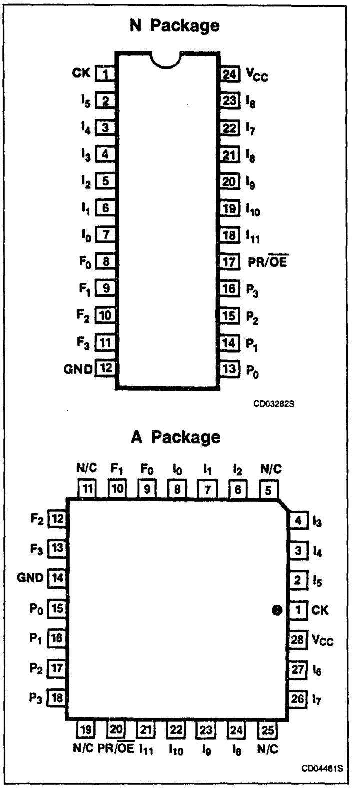
Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes are listed in the Ordering Information Table.

FEATURES

- f_{MAX}: 13.9MHz
  - 20MHz clock rate
- Field-Programmable (Ni-Cr link)
- 12 True/Complement buffered inputs
- 48 programmable AND gates
- 29 programmable OR gates
- 10-bit State Register
- 4-bit shared State/Output Register
- 4-bit Output Register
- Transition Complement Array
- Programmable Asynchronous Preset/Output Enable
- Positive edge-triggered clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip Test Array
- Power: 600mW (typ.)
- TTL compatible
- 3-State outputs
- Single +5V supply
- 300mil-wide 24-pin DIP

PIN CONFIGURATIONS

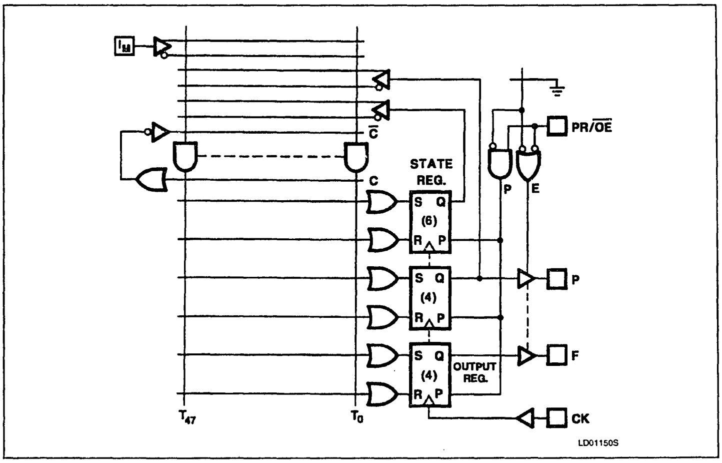

N Package

A Package

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

FUNCTIONAL DIAGRAM



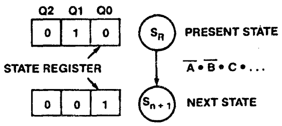
Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2-6 18-23	I_{1-11}	**Logic Inputs:** The 11 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
7	I_0	**Logic/Diagnostic Input:** A 12th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{2-3} and P_{0-3} reflect the contents of State Register bits P_{4-9} (see Diagnostic Output Mode diagram). The contents of flip-flops P_{0-1} and F_{0-3} remain unaltered.	Active-High/Low
13- 16	P_{0-3}	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of State Register bits P_{0-3}. When I_0 is held at +10V these pins reflect ($P_6 - P_9$).	Active-High
10-11	$F_2 - F_3$	**Logic/Diagnostic Outputs:** Two register bits ($F_2 - F_3$) which normally reflect Output Register bits ($Q_2 - Q_3$). When I_0 is held at +10V these pins reflect ($P_4 - P_5$).	Active-High
17	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held high, clocking is inhibited and P_{0-9} and F_{0-3} are high. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes low. • **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers.	 Active-High (H) Active-Low (L)
8, 9	$F_0 - F_1$	**Logic Output:** Two device outputs which reflect Output Registers $Q_0 - Q_1$. When I_0 is held at +10V $F_0 - F_1$ = Logic "1".	

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

TB00900S

TRUTH TABLE[1, 2, 3, 4, 5, 6]

V_{CC}	OPTION		I_0	CK	S	R	$Q_{P/F}$	F
	PR	$\overline{OE}$						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:

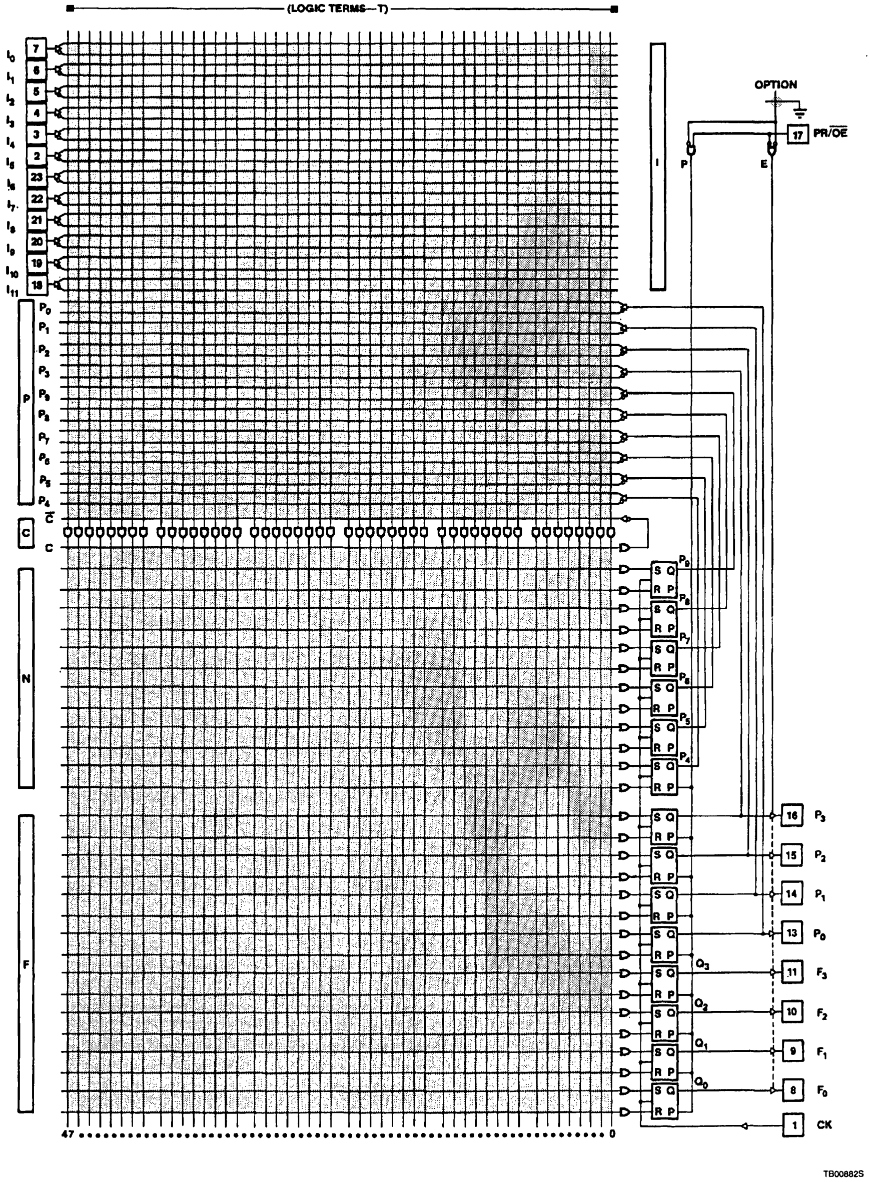
1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I_0\ I_1\ I_2 \ldots)\ (P_0\ P_1 \ldots P_9)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V
6. X = Don't care (≤5.5V)

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.
   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

FPLS LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ◍ Programmable connection.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS168N
28-pin Plastic Leaded Chip Carrier	PLS168A

THERMAL RATING

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{IN}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Pulse width[3]							
t_{CKH}	Clock[2] High	CK −	CK +	25	15		ns
t_{CKL}	Clock Low	CK +	CK −	25	15		
$t_{CKP1}B$	Period (without Complement Array)	CK +	CK +	80	40		
$t_{CKP2}B$	Period (with Complement Array)	CK +	CK +	120	60		
t_{PRH}	Preset pulse	PR −	PR +	25	15		
Setup time[3]							
$t_{IS1}A$	Input	CK +	Input ±	60			ns
$t_{IS1}B$	Input	CK +	Input ±	50			
$t_{IS1}C$	Input	CK +	Input ±	42			
$t_{IS2}A$	Input (through Complement Array)	CK +	Input ±	90			
$t_{IS2}B$	Input (through Complement Array)	CK +	Input	80			
$t_{IS2}C$	Input (through Complement Array)	CK +	Input	72			
t_{VS}	Power-on preset	CK −	V_{CC} +	0	−10		
t_{PRS}	Preset	CK −	PR −	0	−10		
Hold time							
t_{IH}	Input	Input ±	CK +	5	−10		ns
Propagation delay							
t_{CKO}	Clock	Output ±	CK +		15	30	ns
t_{OE}	Output enable	Output −	OE −		20	30	
t_{OD}	Output disable	Output +	OE +		20	30	
t_{PR}	Preset	Output +	PR +		18	30	
t_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	
Frequency of operation[3]							
$f_{MAX}C$	Without Complement Array					13.9	MHz
$f_{MAX}C$	With Complement Array					9.8	

NOTES:

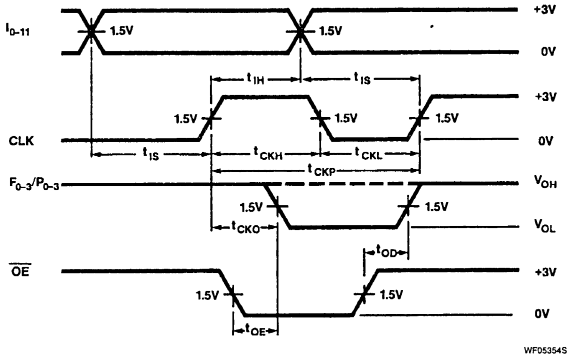
[1] All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.

[2] To prevent spurious clocking, clock rise time (10% − 90%) ≤ 30ns.

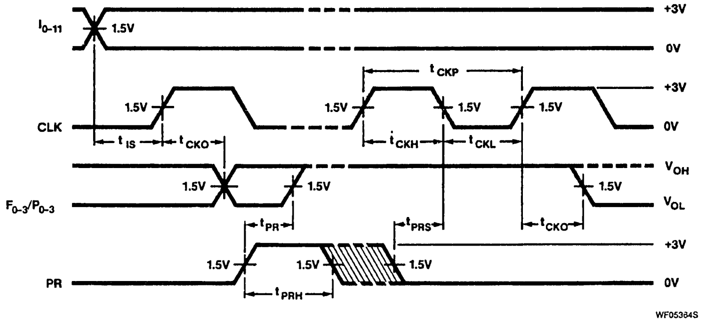
[3] See "Speed vs. OR Loading" diagrams.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

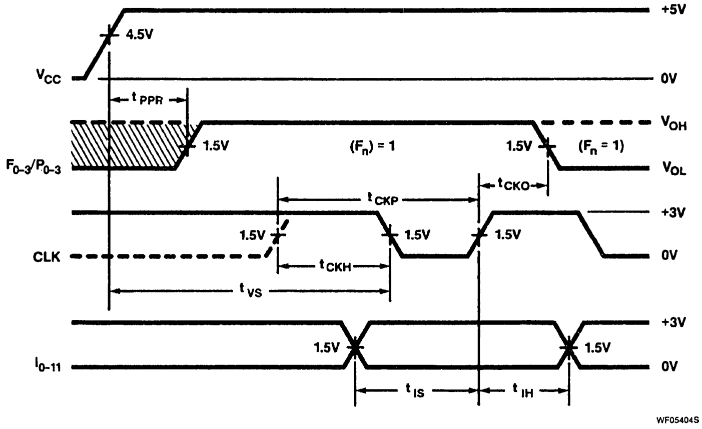
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset

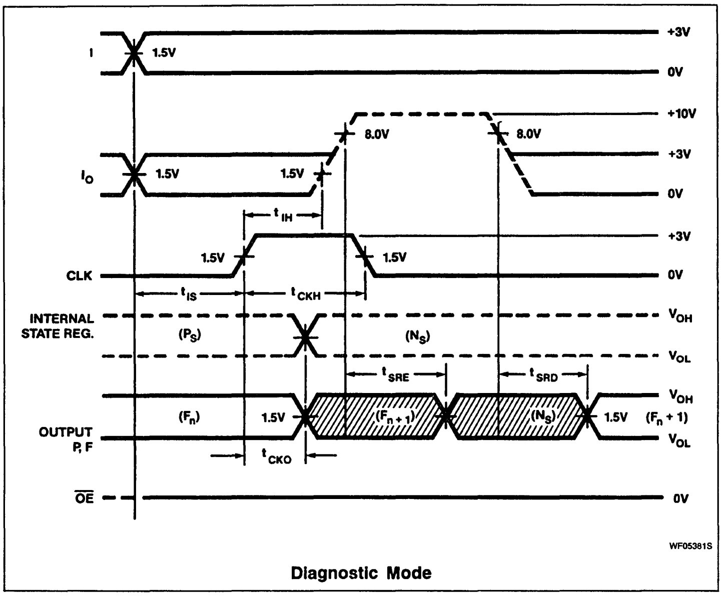


Power-On Preset

TIMING DEFINITIONS

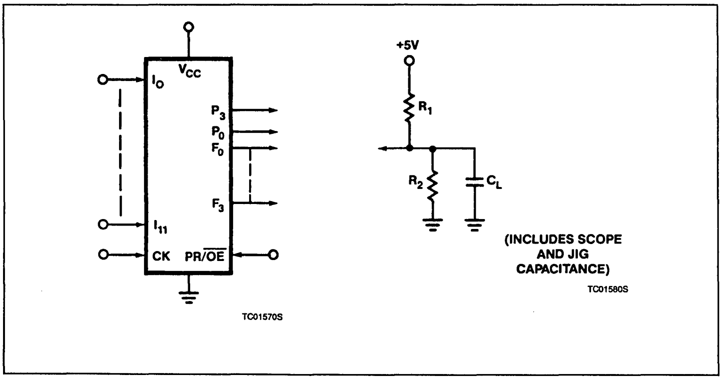
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Clock period – when not using Complement array.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{CKP2}	Clock period – when using complement array.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{SRE}	Delay between input I_0 transition to Diagnostic mode and when the Outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

TIMING DIAGRAMS (Continued)

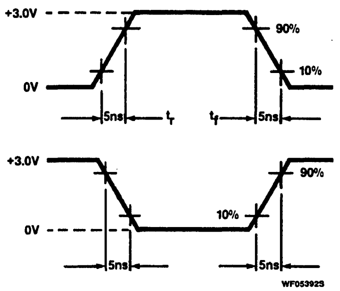


Diagnostic Mode

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and output, unless otherwise specified.

Input Pulses

SPEED VS. "OR" LOADING

The maximum frequency at which the FPLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The AC electrical characteristics contain three limits for the parameters t_{IS1} and t_{IS2}. The first, t_{IS1A} is guaranteed for a device with 48 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 32 terms connected to any OR line. And t_{IS1C} is guaranteed for a device with 24 terms connected to any OR line.

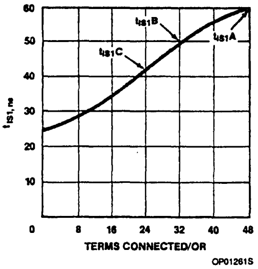


Figure 1. t_{IS1} vs. Terms/OR Connected

The three other entries in the AC table, t_{IS2} A, B and C are corresponding 48, 32 and 24 term limits when using the on-chip Complement Array.

The worst case of t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the FPLS logic diagram, typically illustrated in Figure 2, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

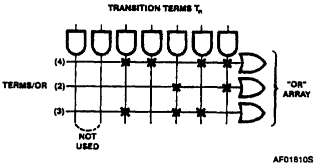


Figure 2. Typical OR Array Interconnect Pattern

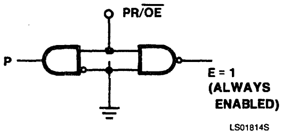
LOGIC PROGRAMMING

PLS168 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

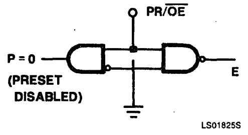
PLS168 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION - (P/E)



OPTION	CODE
PRESET[1]	H

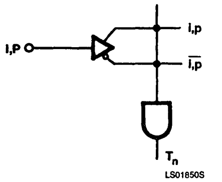


OPTION	CODE
$\overline{OE}$	L

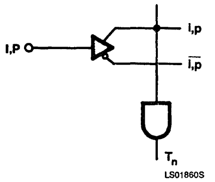
PROGRAMMING:

The PLS168 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

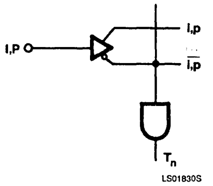
"AND" ARRAY - (I), (P)



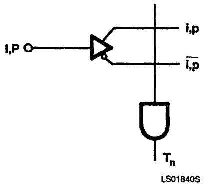
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, P	H

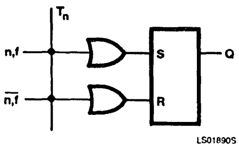


STATE	CODE
$\overline{I}$, $\overline{P}$	L

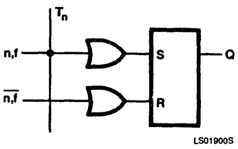


STATE	CODE
DON'T CARE	-

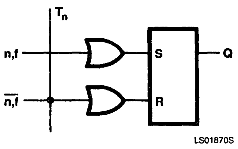
"OR" ARRAY - (N), (F)



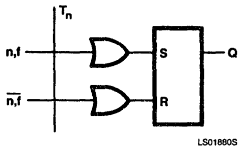
ACTION	CODE
INACTIVE[1,3]	O



ACTION	CODE
SET	H

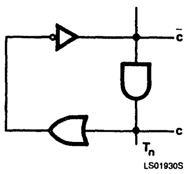


ACTION	CODE
RESET	L

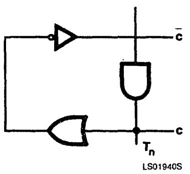


ACTION	CODE
NO CHANGE	-

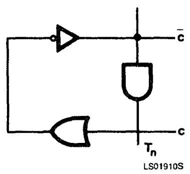
"COMPLEMENT" ARRAY - (C)



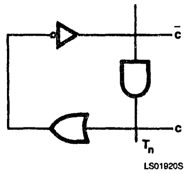
ACTION	CODE
INACTIVE[1,4]	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	-

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement of any input (I or P) are left intact.
3. To prevont simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To provent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

FPLS PROGRAM TABLE PLS168

CUSTOMER NAME ______________________
PURCHASE ORDER # ______________________
SIGNETICS DEVICE # CF (XXXX) ______________________
CUSTOMER SYMBOLIZED PART # ______________________
TOTAL NUMBER OF PARTS ______________________
PROGRAM TABLE # ______________________
REV ______________________
DATE ______________________

AND

INACTIVE	O	C_n
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

INACTIVE	O	I_m P_s
I, P	H	
Ī, P̄	L	
DON T CARE	—	

OR

INACTIVE	O	$N_s \cdot F_r$
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
OE	L	

AND																									OPTION (P/E) OR													
TERM	C_n	INPUT(Im)												PRESENT STATE (Ps) (Px)										REMARKS	NEXT STATE (Ns) (Px)										OUTPUT (Fr)			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	3	2	1	0
0																																						
1																																						
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45																																						
46																																						
47																																						
PIN NO.		18	19	20	21	22	23	2	3	4	5	6	7																		16	15	14	13	11	10	9	8
VARIABLE NAME																																						

TB02030S

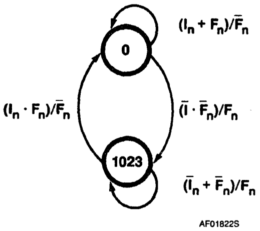
Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

TEST ARRAY

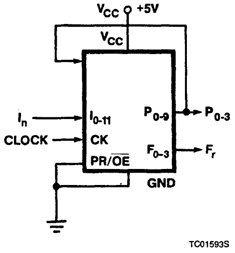
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-11} as shown in the test circuit timing diagram.


0
1023
$(I_n + F_n)/\overline{F}_n$
$(I_n \cdot F_n)/\overline{F}_n$
$(\overline{I} \cdot \overline{F}_n)/F_n$
$(\overline{I}_n + \overline{F}_n)/F_n$
AF01822S

State Diagram

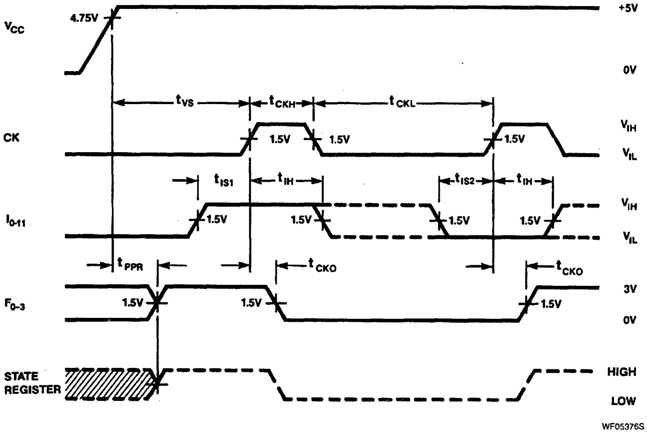


FPLS Under Test

AND																									OPTION (P E)													H
																									OR													
TERM	C_n	INPUT(Im)												PRESENT STATE (Ps) (Px)										REMARKS	NEXT STATE (Ns) (Px)										OUTPUT (Fr)			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L		H	H	H	H	H	H	H	H	H	H	H	H	H	H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.



Test Circuit Timing Diagram

AND																									OPTION (P E)													H
																									OR													
TERM	C_n	INPUT(Im)												PRESENT STATE (Ps) (Px)										REMARKS	NEXT STATE (Ns) (Px)										OUTPUT (Fr)			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	3	2	1	0
48	-	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		-	-	-	-	-	-	-	-	-	-	-	-	-	-
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L		-	-	-	-	-	-	-	-	-	-	-	-	-	-

Test Array Deleted

Signetics

PLS168A
Field-Programmable Logic Sequencer (12 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

The PLS168A is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 10 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, I_{0-11}, with 10 internal inputs, P_{0-9}, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P_0-P_3 of the internal State Register are brought off-chip to allow extending the Output Register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

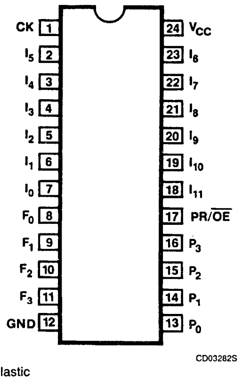
Order codes are listed in the Ordering Information Table.

FEATURES

- f_{MAX}: 20MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 12 True/Complement buffered inputs
- 48 programmable AND gates
- 29 programmable OR gates
- 10-bit State Register
- 4-bit shared State/Output Register
- 4-bit Output Register
- Transition Complement Array
- Programmable Asynchronous Preset/Output Enable
- Positive edge-triggered clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip Test Array
- Power: 600mW (typ.)
- TTL compatible
- 3-State outputs
- Single +5V supply
- 300mil-wide 24-pin DIP

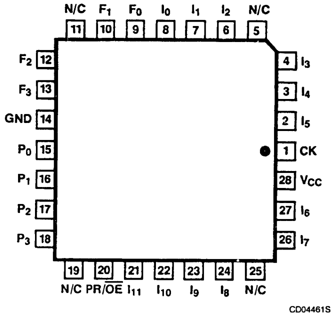
PIN CONFIGURATIONS

N Package



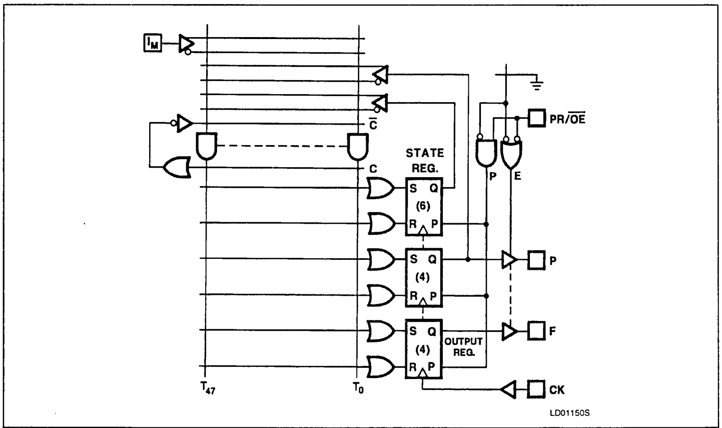
N = Plastic

A Package



A = Plastic Leaded Chip Carrier

FUNCTIONAL DIAGRAM



APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

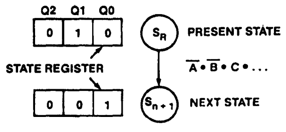
Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2-6 18-23	I_{1-11}	**Logic Inputs:** The 11 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
7	I_0	**Logic/Diagnostic Input:** A 12th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_2-F_3 and P_0-P_3 reflect the contents of State Register bits P_{4-9} (see Diagnostic Output Mode diagram). The contents of flip-flops P_{0-1} and F_{0-3} remain unaltered.	Active-High/Low
13- 16	P_{0-3}	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of State Register bits P_{0-3}. When I_0 is held at +10V these pins reflect (P_6-P_9).	Active-High
10-11	F_2-F_3	**Logic/Diagnostic Outputs:** Two register bits (F_2-F_3) which reflect Output Register bits (Q_2-Q_3). When I_0 is held at +10V these pins reflect (P_4-P_5).	Active-High
17	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held high, clocking is inhibited and P_{0-9} and F_{0-3} are high. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes low.	 Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers.	Active-Low (L)
8, 9	F_0-F_1	**Logic Output:** Two device outputs which reflect Output Registers Q_0-Q_1. When I_0 is held at +10V F_0-F_1 = Logic "1"	

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

TD00900S

TRUTH TABLE[1, 2, 3, 4, 5, 6]

V_{CC}	OPTION		I_0	CK	S	R	$Q_{P/F}$	F
	PR	$\overline{OE}$						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:

1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I_0\ I_1\ I_2\ldots)\ (P_0\ P_1 \ldots P_9)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V
6. X = Don't Care (⩽5.5V)

VIRGIN STATE

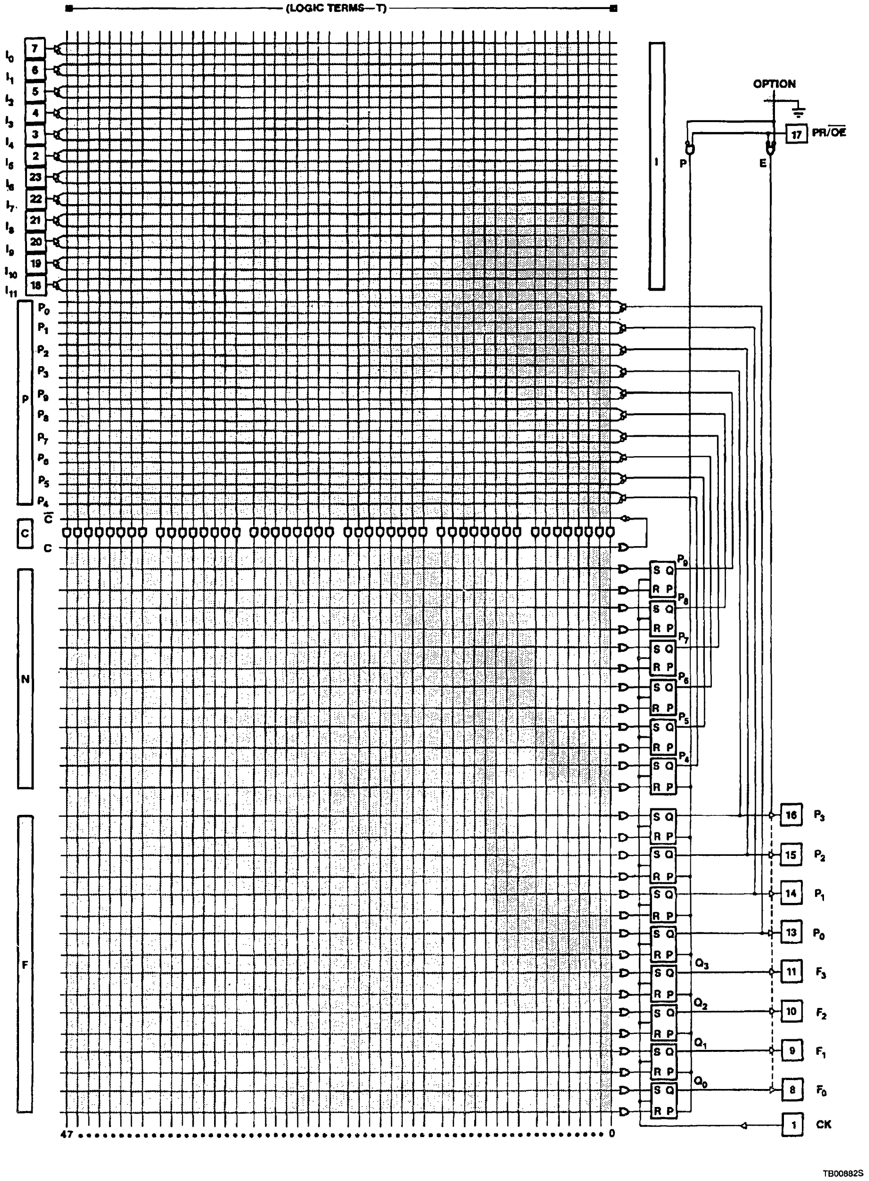
A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

   NOTE: The Test Array pattern MUST be deleted before incorporating a user program.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

FPLS LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ░ Programmable connection.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS168AN
28-pin Plastic Leaded Chip Carrier	PLS168AA

THERMAL RATING

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{IN}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250	μA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	μA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = + 25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

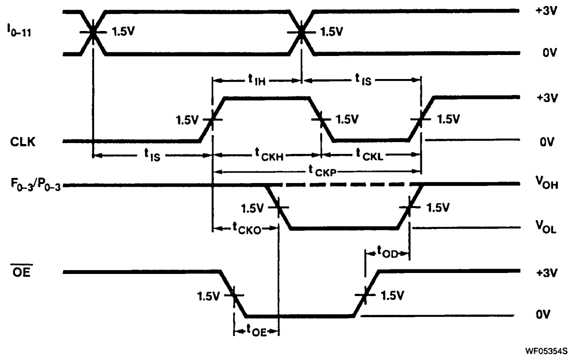
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Pulse width[3]							
t_{CKH}	Clock[2] High	CK −	CK +	20	15		ns
t_{CKL}	Clock Low	CK +	CK −	20	15		
t_{CKP1}B	Period (without Complement Array)	CK +	CK +	50	40		
t_{CKP2}B	Period (with Complement Array)	CK +	CK +	80	50		
t_{PRH}	Preset pulse	PR −	PR +	25	15		
Setup time[3]							
t_{IS1}A	Input	CK +	Input ±	40			ns
t_{IS1}B	Input	CK +	Input ±	30			
t_{IS2}A	Input (through Complement Array)	CK +	Input ±	70			
t_{IS2}B	Input (through Complement Array)	CK +	Input	60			
t_{VS}	Power-on preset	CK −	V_{CC} +	0	−10		
t_{PRS}	Preset	CK −	PR −	0	−10		
Hold time							
t_{IH}	Input	Input ±	CK +	5	−10		ns
Propagation delay							
t_{CKO}	Clock	Output ±	CK +		15	20	ns
t_{OE}	Output enable	Output −	OE −		20	30	
t_{OD}	Output disable	Output +	OE +		20	30	
t_{PR}	Preset	Output +	PR +		18	30	
t_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	
Frequency of operation[3]							
f_{MAX}B	Without Complement Array					20	MHz
f_{MAX}B	With Complement Array					12.5	

NOTES:

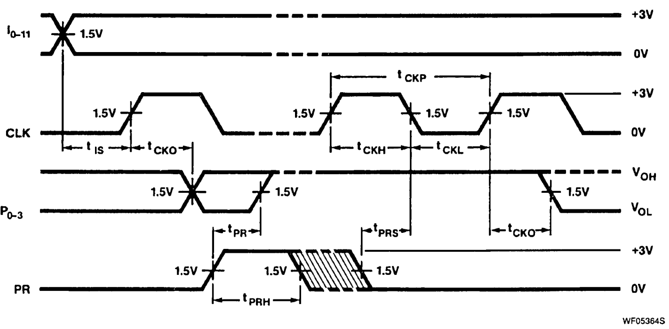
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ⩽ 30ns.
3. See "Speed vs. OR Loading" diagrams.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

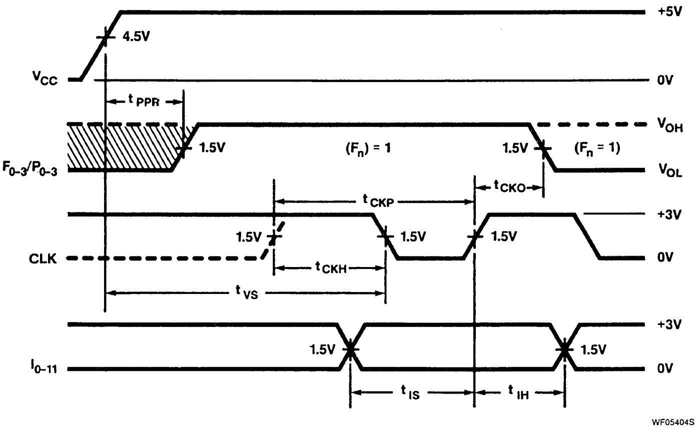
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset



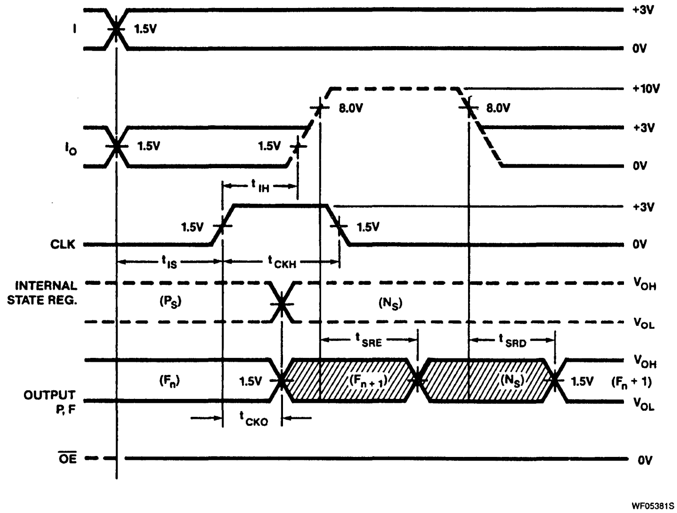
Power-On Preset

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Clock period – when not using Complement array.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{CKP2}	Clock period – when using complement array.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{SRE}	Delay between input I_0 transition to Diagnostic mode and when the Outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

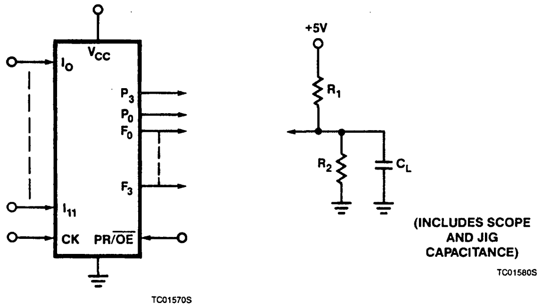
5

TIMING DIAGRAMS (Continued)

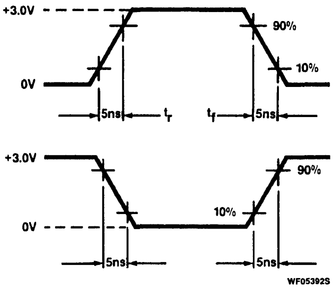


Diagnostic Mode

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and output, unless otherwise specified.

Input Pulses

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

SPEED VS. "OR" LOADING

The maximum frequency at which the FPLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The AC electrical characteristics contain two limits for the parameters t_{IS1} and t_{IS2}. The first, t_{IS1A} is guaranteed for a device with 24 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 16 terms connected to any OR line.

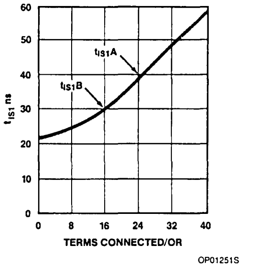


Figure 1. t_{IS1} vs. Terms/OR Connected

The three other entries in the AC table, t_{IS2} A and B are corresponding 24 and 16 term limits when using the on-chip Complement Array.

The worst case of t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the FPLS logic diagram, typically illustrated in Figure 2, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

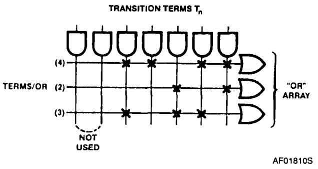


Figure 2. Typical OR Array Interconnect Pattern

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

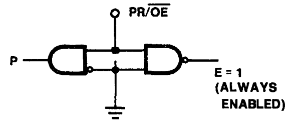
LOGIC PROGRAMMING

PLS168A logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLS168A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

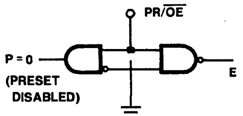
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION – (P/E)



LS01814S

OPTION	CODE
PRESET[1]	H



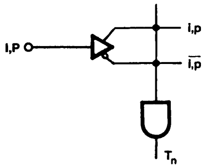
LS01825S

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING:

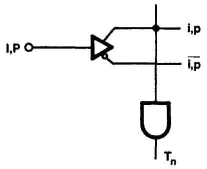
The PLS168A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY – (I), (P)



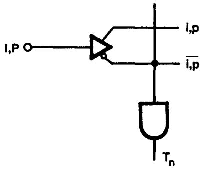
LS01850S

STATE	CODE
INACTIVE[1,2]	O



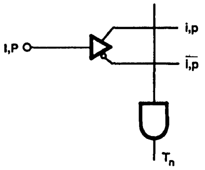
LS01860S

STATE	CODE
I, P	H



LS01830S

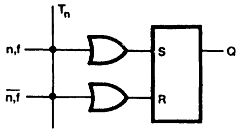
STATE	CODE
$\overline{I}$, $\overline{P}$	L



LS01840S

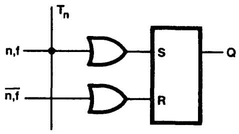
STATE	CODE
DON'T CARE	–

"OR" ARRAY – (N), (F)



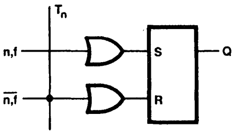
LS01890S

ACTION	CODE
INACTIVE[1,3]	O



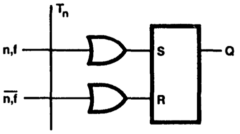
LS01900S

ACTION	CODE
SET	H



LS01870S

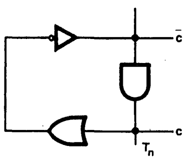
ACTION	CODE
RESET	L



LS01880S

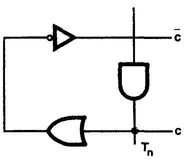
ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY – (C)



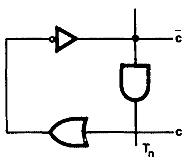
LS01930S

ACTION	CODE
INACTIVE[1,4]	O



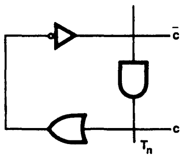
LS01940S

ACTION	CODE
GENERATE	A



LS01910S

ACTION	CODE
PROPAGATE	•



LS01920S

ACTION	CODE
TRANSPARENT	–

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To provont simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To provont oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

FPLS PROGRAM TABLE PLS168A

CUSTOMER NAME ____________________

PURCHASE ORDER # ____________________

SIGNETICS DEVICE # CF (XXXX)

CUSTOMER SYMBOLIZED PART # ____________________

TOTAL NUMBER OF PARTS ____________________

PROGRAM TABLE # ____________________

REV ____________________

DATE ____________________

AND

INACTIVE	O	C_n
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	
INACTIVE	O	I_m, P_s
I, P	H	
$\bar{I}$, $\bar{P}$	L	
DON'T CARE	—	

OR

INACTIVE	O	N_s, F_r
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
OE	L	

AND																									OPTION (P/E)													
																									OR													
TERM	C_n	INPUT(Im)												PRESENT STATE (Ps) (Px)										REMARKS	NEXT STATE (Ns) (Px)						OUTPUT (Fr)							
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	3	2	1	0
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PIN NO.		18	19	20	21	22	23	2	3	4	5	6	7																		16	15	14	13	11	10	9	8
VARIABLE NAME																																						

TB02031S

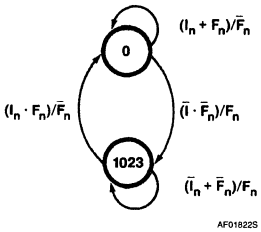
Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168A

TEST ARRAY

The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

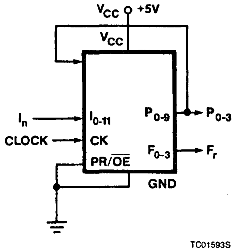
The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to $I_{0\text{-}11}$ as shown in the test circuit timing diagram.



0
1023
$(I_n + F_n)/\bar{F}_n$
$(I_n \cdot F_n)/\bar{F}_n$
$(\bar{I} \cdot \bar{F}_n)/F_n$
$(\bar{I}_n + \bar{F}_n)/F_n$
AF01822S

State Diagram

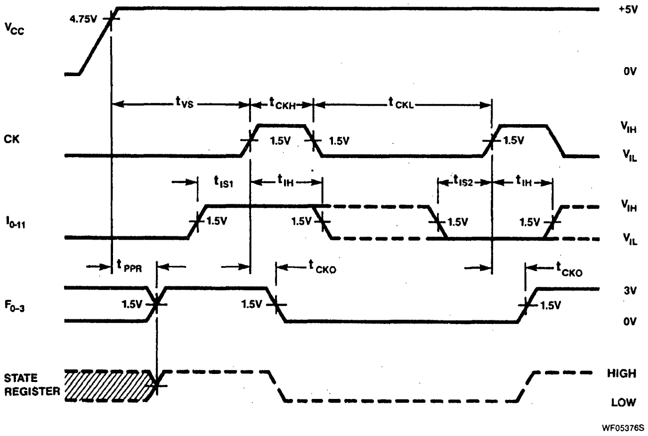


FPLS Under Test

AND																									OPTION (P E)													H
																									OR													
TERM	Cn	INPUT(Im)												PRESENT STATE (Ps) (Px)										REMARKS	NEXT STATE (Ns) (Px)										OUTPUT (Fr)			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L		H	H	H	H	H	H	H	H	H	H	H	H	H	H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.



Test Circuit Timing Diagram

AND																									OPTION (P E)													H
																									OR													
TERM	Cn	INPUT(Im)												PRESENT STATE (Ps) (Px)										REMARKS	NEXT STATE (Ns) (Px)										OUTPUT (Fr)			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	3	2	1	0
48	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H		–	–	–	–	–	–	–	–	–	–	–	–	–	–
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L		–	–	–	–	–	–	–	–	–	–	–	–	–	–

Test Array Deleted

Signetics

PLS179
Field-Programmable Logic Sequencer (20 X 45 X 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 24

DESCRIPTION

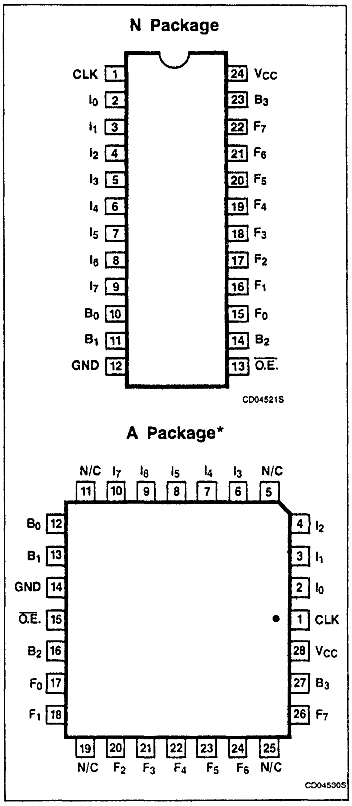
The PLS179 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 20 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 8 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- **f_{MAX} = 18.2MHz**
  - **25MHz clock rate**
- **Field-Programmable (Ni-Cr link)**
- **8 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active-High or -Low outputs**
- **Programmable $\overline{OE}$ control**
- **Positive edge-triggered clock**
- **Power-on reset on flip-flop (F_n = "1")**
- **Input loading: PLS179: − 100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **TTL compatible**
- **3-State option**

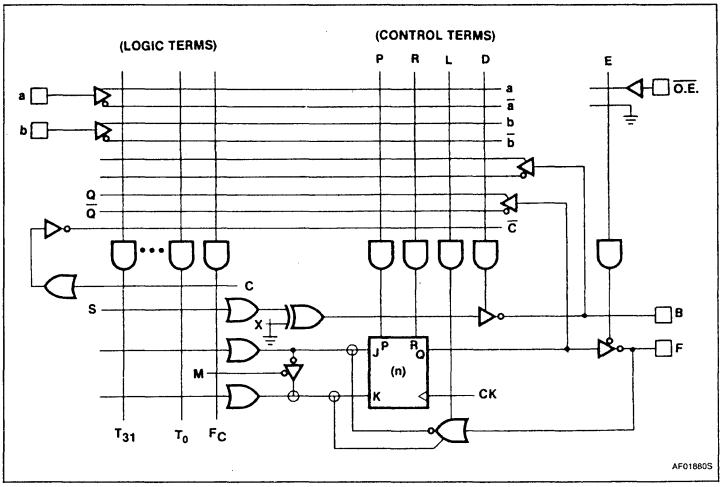
PIN CONFIGURATIONS



APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

FUNCTIONAL DIAGRAM



Field-Programmable Logic Sequencer (20 X 45 X 12) PLS179

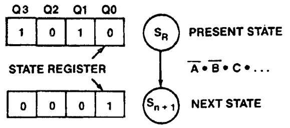
On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R).

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS179 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

LOGIC FUNCTION



SET Q_0: $J_0 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

TOGGLE Q_3: $J_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

TB00901S

NOTES:
Similar logic functions are applicable for D and T mode flip-flops.

FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								H/Hi-Z
L	X	X	X	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

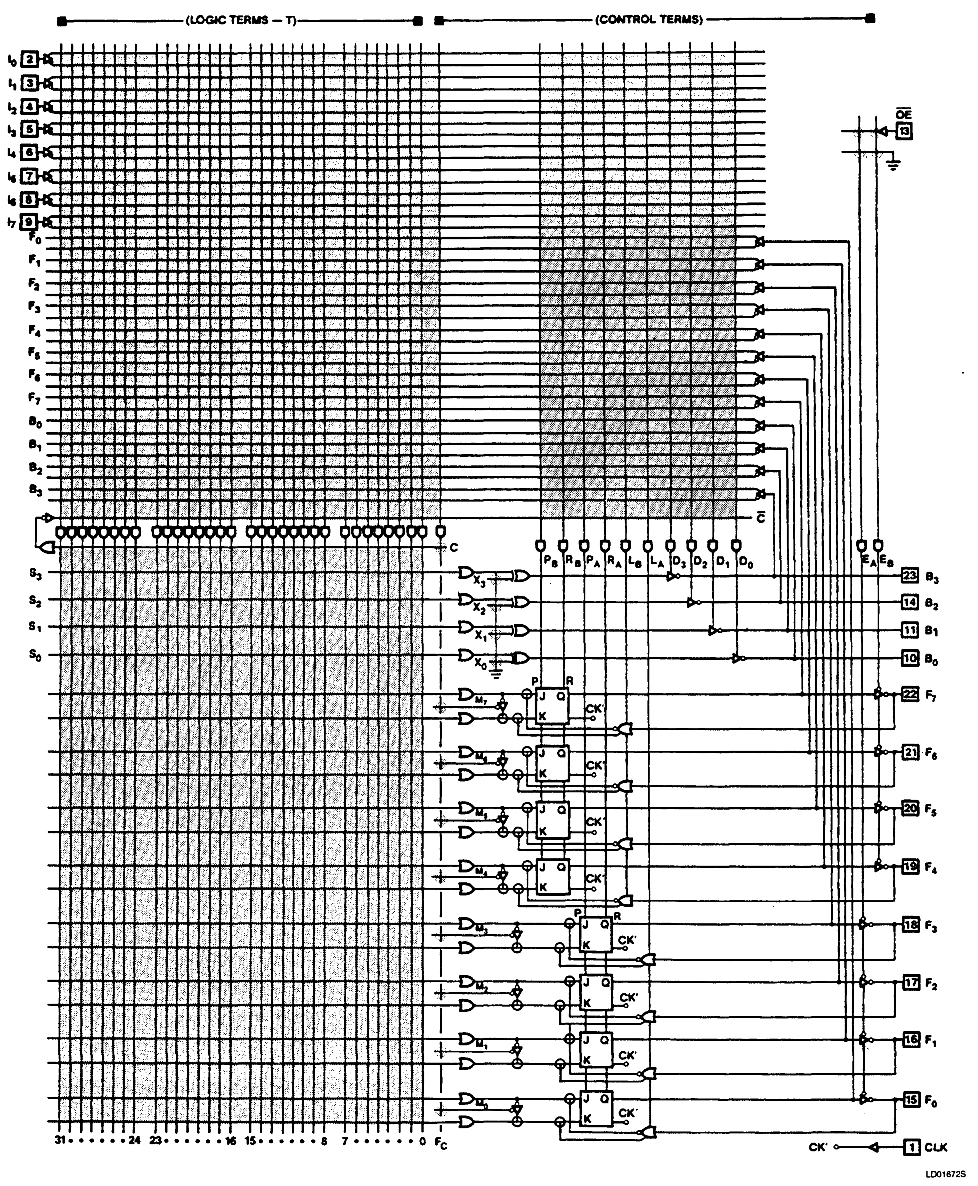
NOTES:
1. Positive Logic:
   $J/K = T_0 + T_1 + T_2 + \ldots + T_{31}$
   $T_n = \overline{C} \cdot (I_0 \cdot I_1 \cdot I_2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B_0 \cdot B_1 \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't Care
4. * = Forced at F_n pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active T_n disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J/K only or J/K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

FPLS LOGIC DIAGRAM



1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ▨ Programmable connection.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS179N
28-pin Plastic Leaded Chip Carrier	PLS179A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = Min, I_{OH} = -2mA	2.4			V
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{CC} = Max, V_{IN} = 5.5V		< 1	40	μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100	μA
Output current						
$I_{O(OFF)}$	Hi-Z state[4, 7]	V_{CC} = Max, V_{OUT} = 5.5V		1	80	μA
		V_{OUT} = 0.45V			-140	μA
I_{OS}	Short circuit[3, 5]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[6]	V_{CC} = Max		150	210	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3 Test one at a time.
4. Moasured with V_{IH} applied to $\overline{OE}$.
5. Duration of short circuit should not exceed 1 second.
6. I_{CC} is moasured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
7. Leakago values are a combination of input and output leakage.

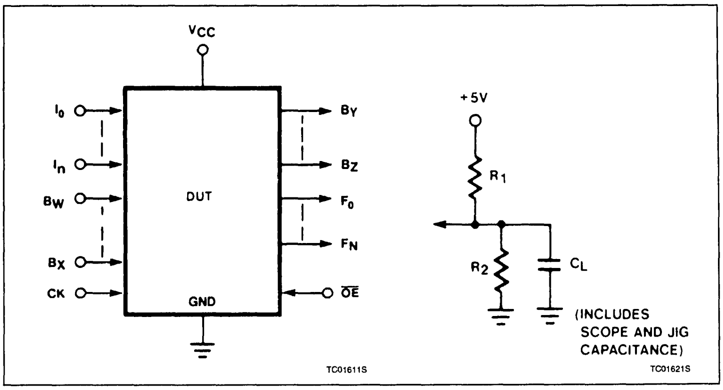
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min[5]	Typ[1]	Max	
Pulse width				$C_L = 30pF$				
t_{CKH}	Clock[2] High	CK −	CK +		20	15		ns
t_{CKL}	Clock Low	CK +	CK −		20	15		
t_{CKP}	Period	CK +	CK +		55	45		
t_{PRH}	Preset/Reset pulse	(I,B) +	(I,B) −		35	30		
Setup time								
t_{IS1}	Input	CK +	(I,B) ±		35	30		ns
t_{IS2}	Input (through F_n)	CK +	F ±		15	10		
t_{IS3}	Input (through Complement Array)[4]	CK +	(I,B) ±		55	45		
Hold time								
t_{IH1}	Input	CK +	(I,B) ±		0	-5		ns
t_{IH2}	Input (through F_n)	CK +	F ±		15	10		
Propagation delay								
t_{CKO}	Clock	F ±	CK ±			15	20	ns
t_{OE1}	Output enable	F −	$\overline{OE}$ −			20	30	
t_{OD1}	Output disable[3]	F +	$\overline{OE}$ +	$C_L = 5pF$		20	30	
t_{PD}	Output	B ±	(I,B) ±	$C_L = 30pF$		25	35	
t_{OE2}	Output enable	B ±	(I,B) +			20	30	
t_{OD2}	Output disable[3]	B +	(I,B) −	$C_L = 5pF$		20	30	
t_{PRO}	Preset/Reset	F ±	(I,B) +	$C_L = 30pF$		35	45	
t_{PPR}	Power-on preset	F −	V_{CC} +			0	10	

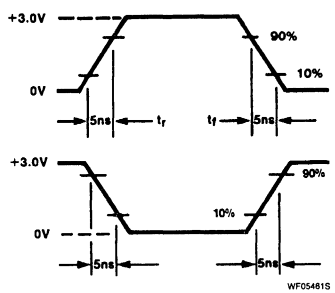
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ≤ 10ns.
3. Measured at $V_T = V_{OL} + 0.5V$.
4. When using the Complement Array $T_{CKP} = 75ns$ (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS

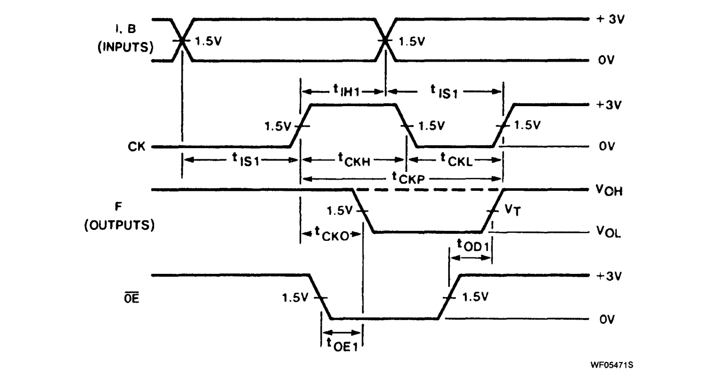


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

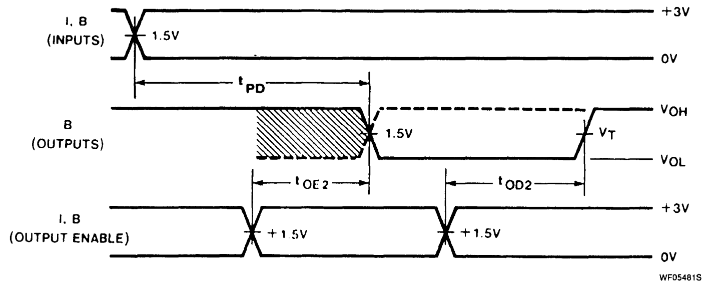
Input Pulses

Field-Programmable Logic Sequencer (20 X 45 X 12) PLS179

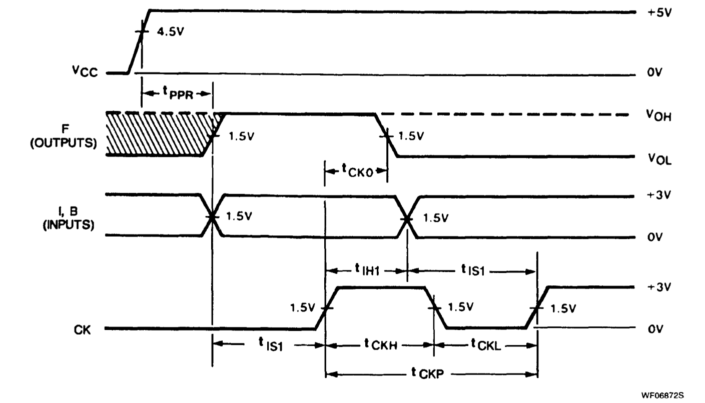
TIMING DIAGRAMS



Flip-Flop Outputs



Gate Outputs

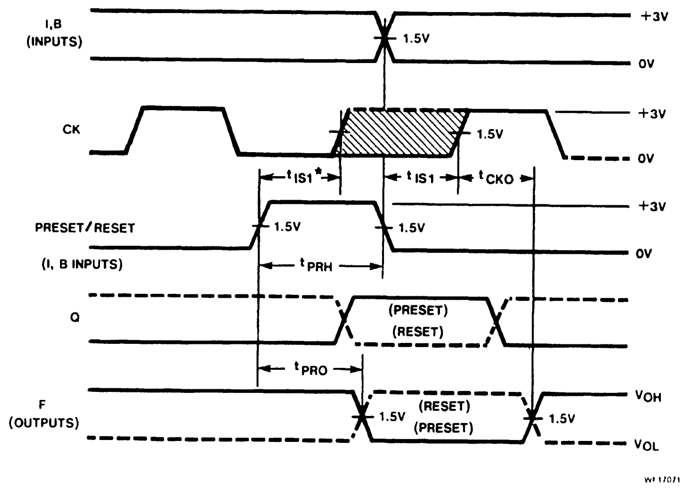


Power-On Reset

TIMING DEFINITIONS

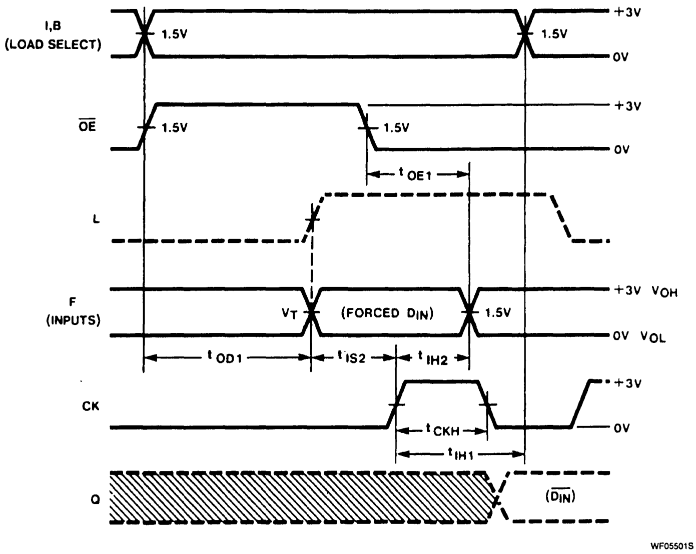
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational Outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational Outputs are in the off state.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



*Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if T_{IS1} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Flip-Flop Input Mode

Field-Programmable Logic Sequencer (20 X 45 X 12) PLS179

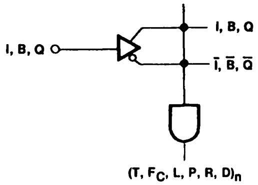
LOGIC PROGRAMMING

PLS179 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLS179 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

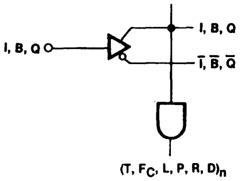
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY - (I), (B), (Qp)



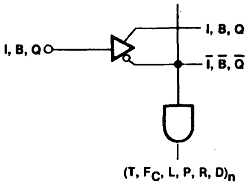
STATE	CODE
INACTIVE[1,2]	O

LS02030S



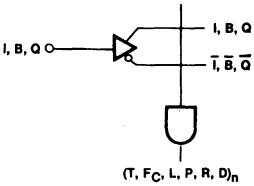
STATE	CODE
I, B, Q	H

LS02040S



STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

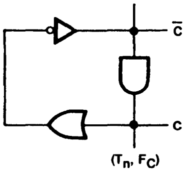
LS02050S



STATE	CODE
DON'T CARE	–

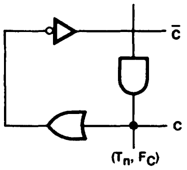
LS02060S

"COMPLEMENT" ARRAY - (C)



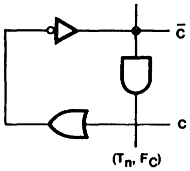
ACTION	CODE
INACTIVE[1,3,5]	O

LS02070S



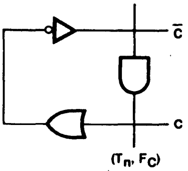
ACTION	CODE
GENERATE[5]	A

LS02080S



ACTION	CODE
PROPAGATE	●

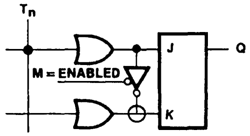
LS02090S



ACTION	CODE
TRANSPARENT	–

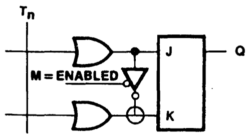
LS02100S

"OR" ARRAY — (Q_N = D - Type)



T_n STATUS	CODE
ACTIVE (Set)	A

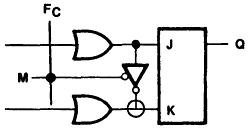
LS02150S



T_n STATUS	CODE
INACTIVE (Reset)	●

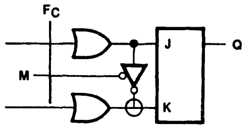
LS02160S

"OR" ARRAY — (F-F CONTROL MODE)



ACTION	CODE
J/K OR D (CONTROLLED)	A

LS02130S



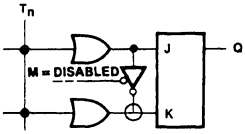
ACTION	CODE
J-K	●

LS02140S

Notes on following page.

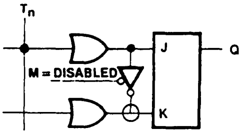
Field-Programmable Logic Sequencer (20 X 45 X 12) PLS179

"AND" ARRAY — (Q_N = J - K Type)



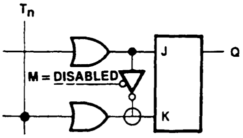
ACTION	CODE
TOGGLE	O

LS02170S



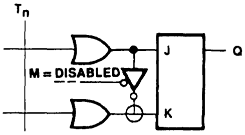
ACTION	CODE
SET	H

LS02180S



ACTION	CODE
RESET	L

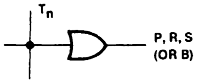
LS02190S



ACTION	CODE
HOLD	–

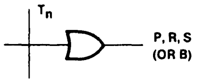
LS02200S

"OR" ARRAY — (S or B)



T_n STATUS	CODE
ACTIVE	A

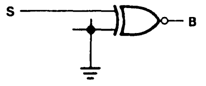
LS02210S



T_n STATUS	CODE
INACTIVE	•

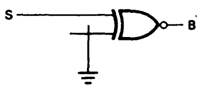
LS02220S

"EX-OR" ARRAY — (B)



POLARITY	CODE
LOW	L

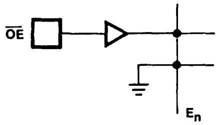
LS02230S



POLARITY	CODE
HIGH	H

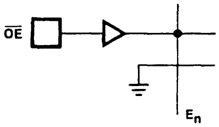
LS02240S

"OE " ARRAY — (E)



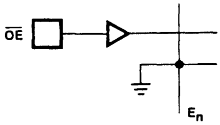
ACTION	CODE
IDLE[4]	O

LS02250S



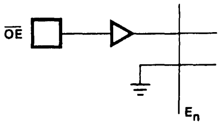
ACTION	CODE
CONTROL	A

LS02260S



ACTION	CODE
ENABLE[4]	•

LS02270S



ACTION	CODE
DISABLE	–

LS02280S

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)$_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link, pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)$_n$ due to their lack of "OR" array links.

Field-Programmable Logic Sequencer (20 × 45 × 12) PLS179

FPLS PROGRAM TABLE

AND

INACTIVE	0	I, B, (I), Q (P)
I, B, Q	H	
Ī, B̄, Q̄	L	
DON'T CARE	—	

INACTIVE	0	C
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

OR

ACTIVE	A	P, R, B (O) (Q = D)
INACTIVE	•	

TOGGLE	0	(Q = J/K)
SET	H	
RESET	L	
HOLD	—	

CONTROL

J/K	•	F/F MODE
J/K or D (CONTROLLED)	A	

IDLE	0	E_A, B
CONTROL	A	
ENABLE	•	
DISABLE	—	

HIGH	H	(POL.)
LOW	L	

NOTES

1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and O bits in the AND array as (—). Program unused Q, B, R, and P bits in the OR array as (—) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) ____________

CUSTOMER SYMBOLIZED PART # ____________

DATE RECEIVED ____________

COMMENTS ____________

														F/F MODE								E_B				E_A				POLARITY			
TERM	C	AND																				(OR)											
		I								B (I)				Q (P)								Q (N)								B (O)			
		7	6	5	4	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0
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P_B																																	
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L_B																																	
P_A																																	
R_A																																	
L_A																																	
D3																																	
D2																																	
D1																																	
D0																																	
PIN		9	8	7	6	5	4	3	2	23	14	11	10	22	21	20	19	18	17	16	15												

CUSTOMER NAME ____________

PURCHASE ORDER # ____________

SIGNETICS DEVICE # ____________

TOTAL NUMBER OF PARTS ____________

PROGRAM TABLE # ________ REV ________ DATE ________

TB01711S

Signetics

PLS105

Field-Programmable Logic Sequencer (16 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 28

DESCRIPTION

The PLS105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_P, and 8 Q_F edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs I_{0-15} with six internal inputs P_{0-5}, which are fed back from the State Registers to form up to 48 transition terms (AND terms). All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output Enable}}$ function, as an additional user-programmable option.

Order codes are listed in the Ordering Information Table.

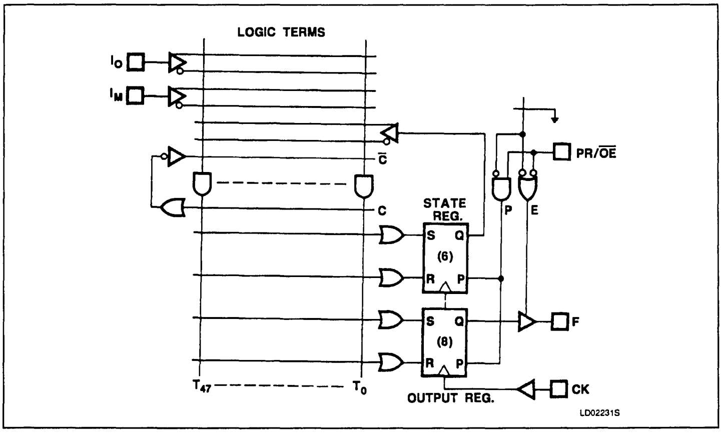
FEATURES

- f_{MAX} = 13.9MHz
  - 20MHz clock rate
- Field-Programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition Complement Array
- Positive edge-triggered clocked flip-flops
- Programmable Asynchronous Preset or Output Enable
- Power-on preset to all "1" of internal registers
- Power dissipation: 600mW (typ.)
- TTL compatible
- Single +5V supply
- 3-State outputs

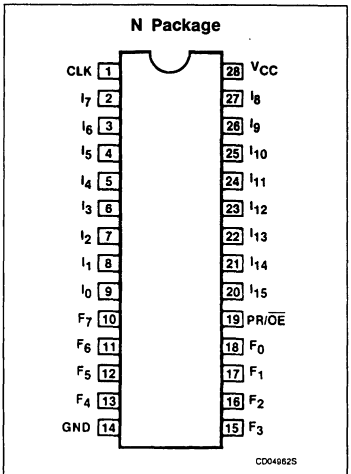
APPLICATIONS

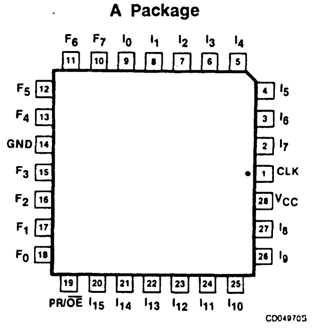
- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

FUNCTIONAL DIAGRAM



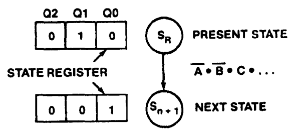
PIN CONFIGURATIONS





LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

TB00900S

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 – 8 20 – 27	I_{1-15}	**Logic Inputs:** The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
9	I_0	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-5} reflect the contents of State Register bits P_{0-5}. The contents of each Output Register remains unaltered.	Active-High/Low
10 – 13 15 – 18	F_{0-7}	**Logic/Diagnostic Outputs:** Eight device outputs which normally reflect the contents of Output Register bits Q_{0-7}, when enabled. When I_0 is held at +10V, $F_{0-5} = (P_{0-5})$, and $F_{6,7}$ = Logic "1".	Active-High
19	PR/$\overline{\text{OE}}$	**Preset or $\overline{\textbf{Output Enable}}$ Input:** A user programmable function:	
		• **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F_{0-7} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.	Active-High (H)
		• $\overline{\textbf{Output Enable}}$: Provides an Output Enable function to all output buffers F_{0-7} from the Output Register.	Active-Low (L)

TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION		I_0	CK	S	R	$Q_{P/F}$	F
	PR	$\overline{\text{OE}}$						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:

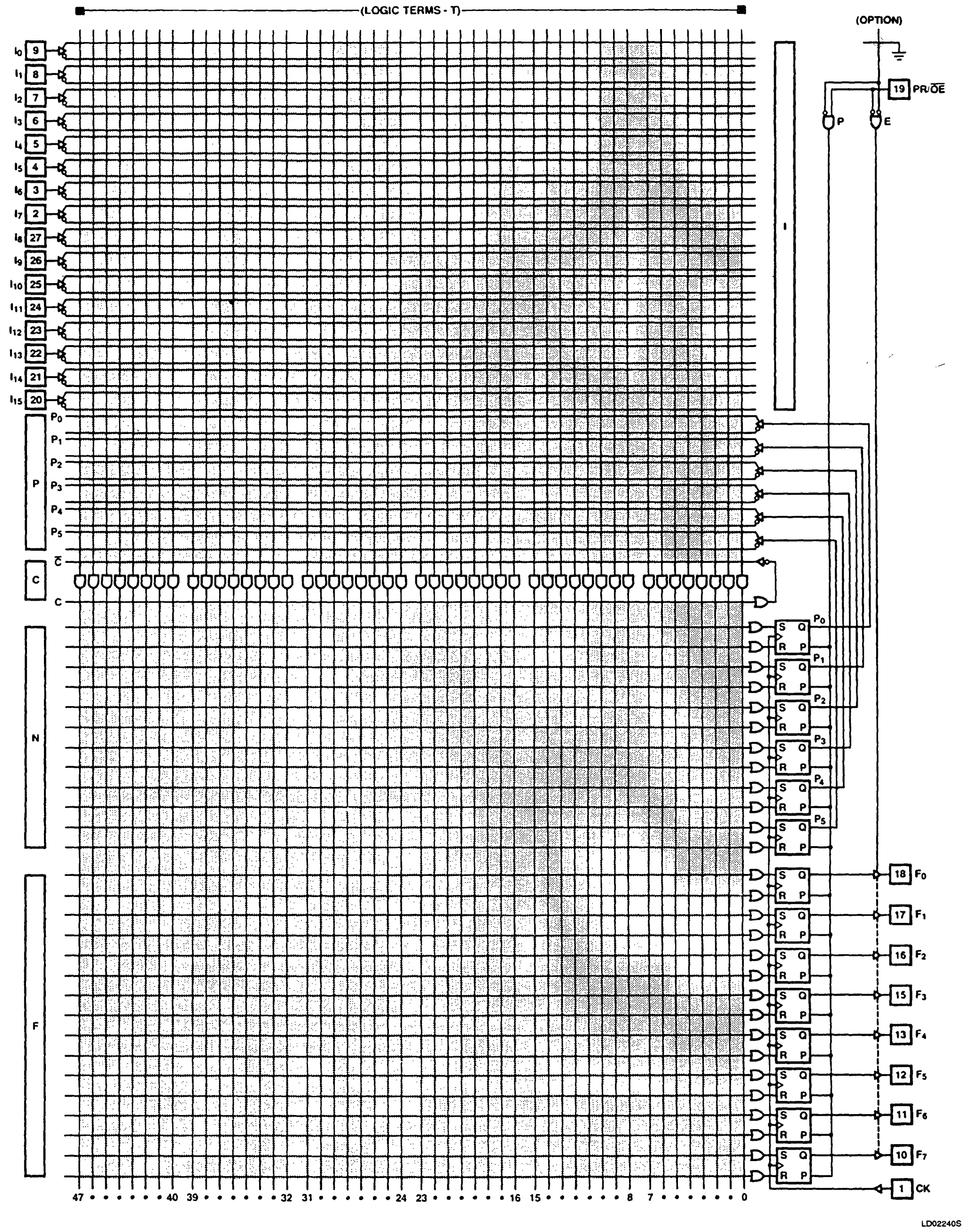
1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + ... + T_{47}$
   $T_n = C(I_0\ I_1\ I_2...)\ (P_0\ P_1...P_5)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V
6. X = Don't Care ($\leqslant$5.5V)

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{\text{OE}}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.
   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically when using Signetics qualified programming equipment.

FPLS LOGIC DIAGRAM



NOTES:
1. All AND inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown link float to logic "0".
3. ▨ Programmable connection.

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	PLS105N
28-pin Plastic Leaded Chip Carrier	PLS105A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	µA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105

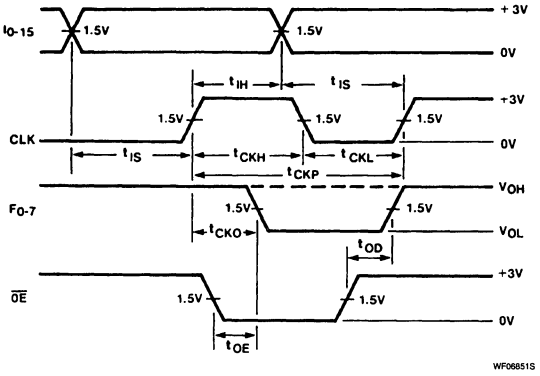
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Pulse width							
t_{CKH}	Clock[2] High	CK −	CK +	25	15		ns
t_{CKL}	Clock Low	CK +	CK −	25	15		
$t_{CKP1}B$	Period (without Complement Array)	CK +	CK +	80	40		
$t_{CKP2}B$	Period (with Complement Array)	CK +	CK +	120	60		
t_{PRH}	Preset pulse	PR −	PR +	25	15		
Setup time[3]							
$t_{IS1}A$	Input	CK +	Input ±	60			ns
$t_{IS1}B$	Input	CK +	Input ±	50			
$t_{IS1}C$	Input	CK +	Input ±	42			
$t_{IS2}A$	Input (through Complement Array)	CK +	Input ±	90			
$t_{IS2}B$	Input (through Complement Array)	CK +	Input	80			
$t_{IS2}C$	Input (through Complement Array)	CK +	Input	72			
t_{VS}	Power-on preset	CK −	V_{CC} +	0	−10		
t_{PRS}	Preset	CK −	PR −	0	−10		
Hold time							
t_{IH}	Input	Input ±	CK +	5	−10		ns
Propagation delay							
t_{CKO}	Clock	Output ±	CK +		15	30	ns
t_{OE}	Output enable	Output −	OE −		20	30	
t_{OD}	Output disable	Output +	OE +		20	30	
t_{PR}	Preset	Output +	PR +		18	30	
t_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	
Frequency of operation[3]							
$f_{MAX}C$	Without Complement Array					13.9	MHz
$f_{MAX}C$	With Complement Array					9.8	

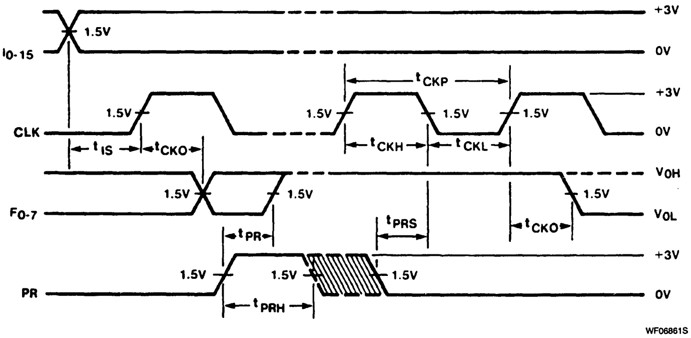
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ⩽ 30ns.
3. Soo "Speed vs. OR Loading" diagrams.

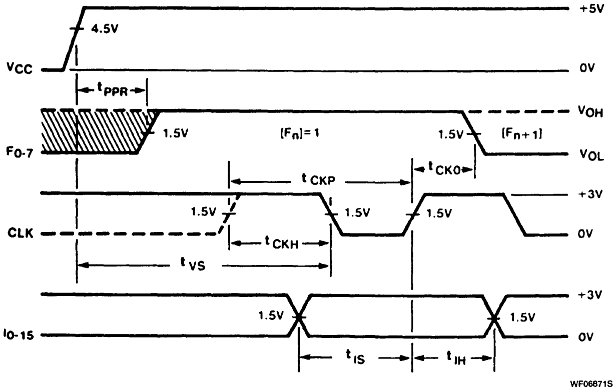
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset



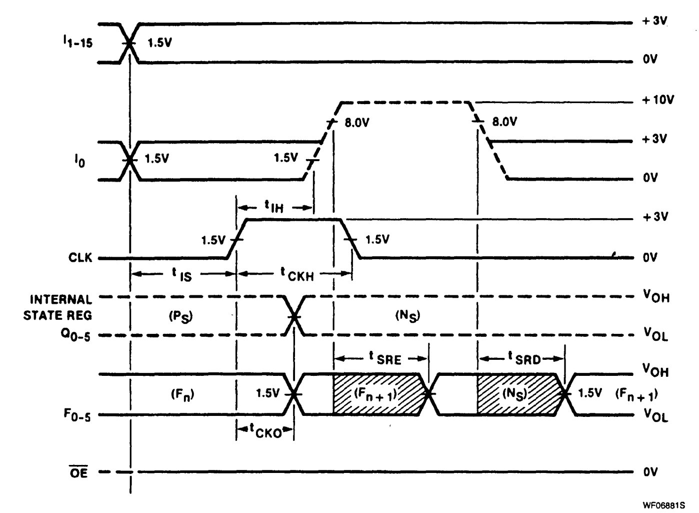
Power-On Preset

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Clock period - when not using Complement Array.
t_{IS1} t_{CKP2}	Required delay between beginning of valid input and positive transition of Clock. Clock period - when using Complement Array.
t_{IS2}	Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with ' PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{SRE}	Delay between input I_0 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after .power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

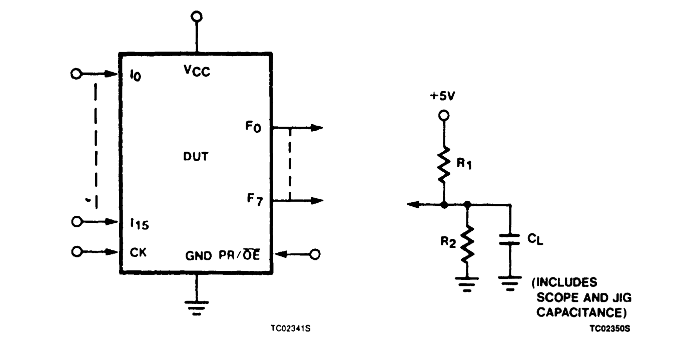
5

TIMING DIAGRAMS (Continued)

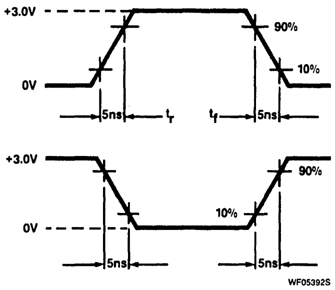


Diagnostic Mode

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105

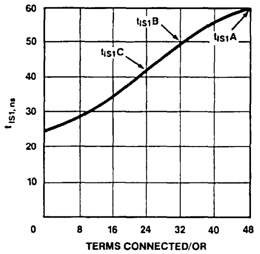
SPEED VS. "OR" LOADING

The maximum frequency at which the FPLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS}, due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The AC electrical characteristics contain three limits for the parameters t_{IS1} and t_{IS2}. The first, t_{IS1A} is guaranteed for a device with 48 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 32 terms connected to any OR line. And t_{IS1C} is guaranteed for a device with 24 terms connected to any OR line.



OP01261S

Figure 1. t_{IS1} vs. Terms/OR Connected

The three other entries in the AC table, t_{IS2} A, B, and C are corresponding 48, 32, and 24 term limits when using the on-chip Complement Array.

The worst case t_{IS} for a given application can be determined by identifying the OR line with the maximum number of t_n connections. This can be done by referring to the interconnect pattern in the FPLS logic diagram, typically illustrated in Figure 2, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

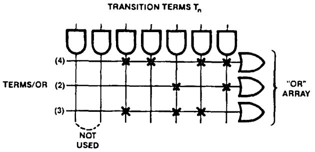


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Figure 2. Typical OR Array Interconnect Pattern

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105

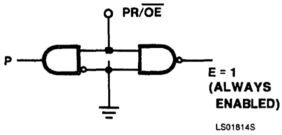
LOGIC PROGRAMMING

PLS105 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

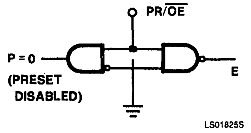
PLS105 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{\text{OE}}$ OPTION – (P/E)



OPTION	CODE
PRESET[1]	H

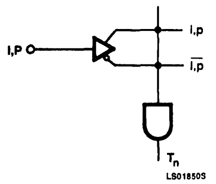


OPTION	CODE
$\overline{\text{OE}}$	L

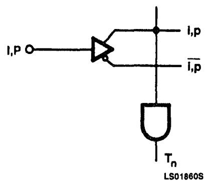
PROGRAMMING THE PLS105:

The PLS105 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

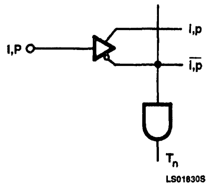
"AND" ARRAY – (I), (P)



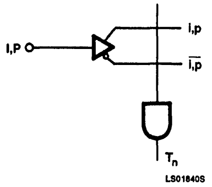
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, P	H

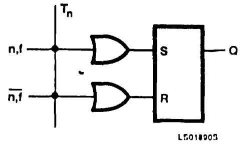


STATE	CODE
$\overline{\text{I}}$, $\overline{\text{P}}$	L

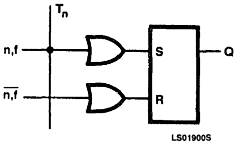


STATE	CODE
DON'T CARE	–

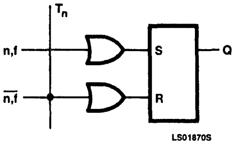
"OR" ARRAY – (N), (F)



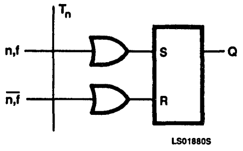
ACTION	CODE
INACTIVE[1,3]	O



ACTION	CODE
SET	H

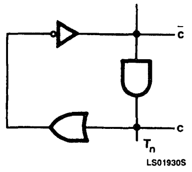


ACTION	CODE
RESET	L

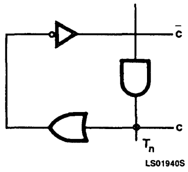


ACTION	CODE
NO CHANGE	–

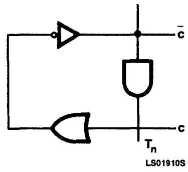
"COMPLEMENT" ARRAY – (C)



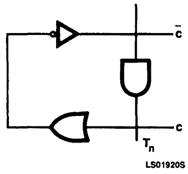
ACTION	CODE
INACTIVE[1,4]	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	–

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement fuses of any input (I,P) are left intact.
3. To provent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To provent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105

FPLS PROGRAM TABLE

CUSTOMER NAME ____________________
PURCHASE ORDER # ____________________
SIGNETICS DEVICE # ____CF (XXXX)____
CUSTOMER SYMBOLIZED PART # ____________________
TOTAL NUMBER OF PARTS ____________________
PROGRAM TABLE ____________________
REV ____________________
DATE ____________________

PROGRAM TABLE ENTRIES

AND

INACTIVE	0	Cn
GENERATE	A	
PROPAGATE	●	
TRANSPARENT	—	

INACTIVE	0	Im, Ps
I, P	H	
$\overline{I}, \overline{P}$	L	
DON'T CARE	—	

OR

INACTIVE	0	Ns, Fr
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
$\overline{OE}$	L	

AND																									OPTION (P/E) OR													
TERM	Cn	INPUT (Im)																PRESENT STATE (Ps)						REMARKS	NEXT STATE (Ns)						OUTPUT (Fr)							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0
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PIN NO.		20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9														10	11	12	13	15	16	17	18
VARIABLE NAME																																						

LD02251S

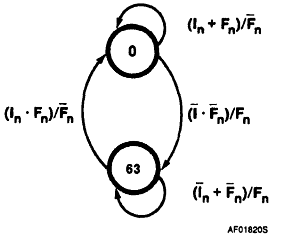
NOTES:
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exits in the table, shown BLANK instead for clarity.
2. Unused Cn Im, and Ps bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmed.

TEST ARRAY

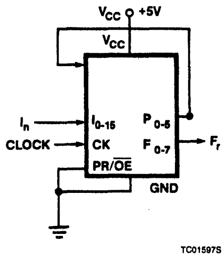
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-15} as shown in the test circuit timing diagram.


0
63
$(I_n + F_n)/\bar{F}_n$
$(I_n \cdot F_n)/\bar{F}_n$
$(\bar{I} \cdot \bar{F}_n)/F_n$
$(\bar{I}_n + \bar{F}_n)/F_n$
AF01820S

State Diagram



FPLS Under Test

TEST ARRAY PROGRAM

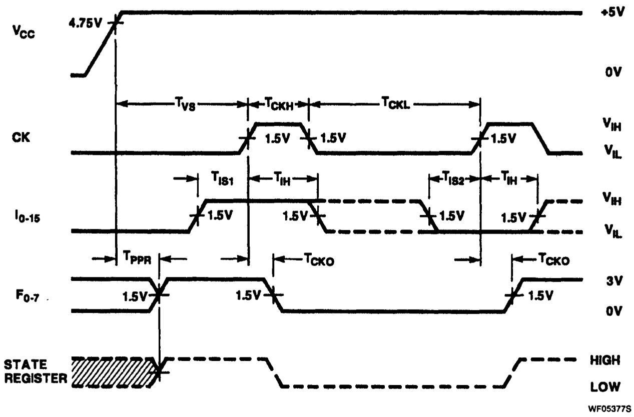
TERM	C	AND																					
		INPUT (Im)																PRESENT STATE (Ps)					
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)													H
OR													
NEXT STATE (Ns)						OUTPUT (Fr)							
5	4	3	2	1	0	7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

TB01760S

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.



Test Circuit Timing Diagram

TEST ARRAY DELETED

TERM	C	AND																					
		INPUT (Im)																PRESENT STATE (Ps)					
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0
48	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)													H
OR													
NEXT STATE (Ns)						OUTPUT (Fr)							
5	4	3	2	1	0	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—	—	—

TB01750S

Test Array Deleted

Signetics

PLS105A
Field-Programmable Logic Sequencer (16 × 48 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 28

DESCRIPTION

The PLS105A is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_P, and 8 Q_F edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs I_{0-15} with 6 internal inputs P_{0-5}, which are fed back from the State Registers to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output-Enable}}$ function, as an additional user programmable option.

Order codes are listed in the Ordering Information Table.

FEATURES

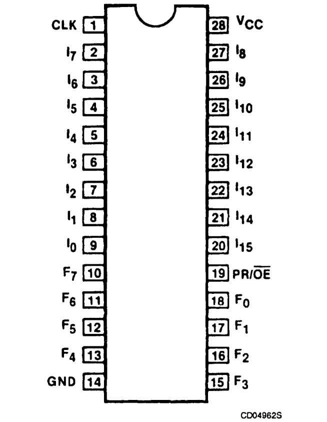
- f_{MAX} = 20MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition complement array
- Positive edge-triggered clocked flip-flops
- Programmable Asynchronous Preset or Output Enable
- Power-on preset to all "1" of internal registers
- Power dissipation: 600mW (typ.)
- TTL compatible
- Single +5V supply
- 3-State outputs

APPLICATIONS

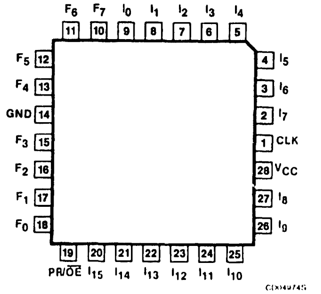
- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

PIN CONFIGURATIONS

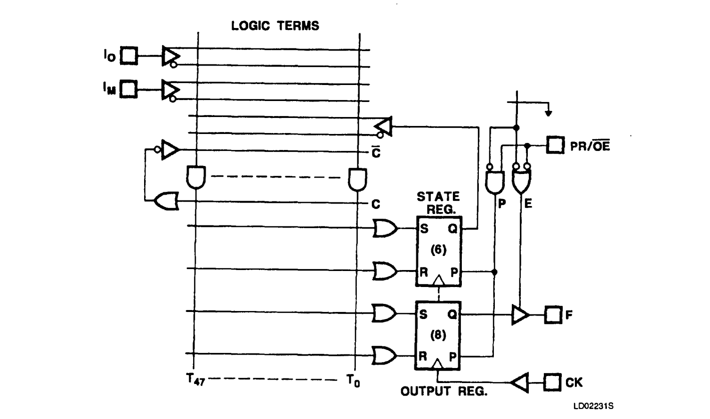
N Package



A Package

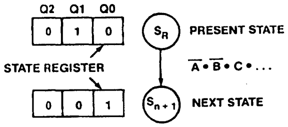


FUNCTIONAL DIAGRAM



LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$R_0 = 0$

RESET Q_1: $S_1 = 0$

$R_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$

$R_2 = 0$

TB00000S

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 – 8 20 – 27	I_{1-15}	**Logic Inputs:** The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
9	I_0	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-5} reflect the contents of State Register bits P_{0-5}. The contents of each Output Register remains unaltered.	Active-High/Low
10 – 13 15 – 18	F_{0-7}	**Logic/Diagnostic Outputs:** Eight device outputs which normally reflect the contents of Output Register bits Q_{0-7}, when enabled. When I_0 is held at +10V, F_{0-5} = (P_{0-5}), and $F_{6,\,7}$ = Logic "1".	Active-High
19	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F_{0-7} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low.	 Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an output enable function to buffers F_{0-7} from the Output Register.	Active-Low (L)

TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION		I_0	CK	S	R	$Q_{P/F}$	F
	PR	$\overline{OE}$						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:

1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + ... + T_{47}$
   $T_n = C(I_0\ I_1\ I_2...)\ (P_0\ P_1...P_5)$
2. Either Preset (Active-High) or $\overline{\text{Output}}$ $\overline{\text{Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V
6. X = Don't Care ($\leqslant$5.5V)

VIRGIN STATE

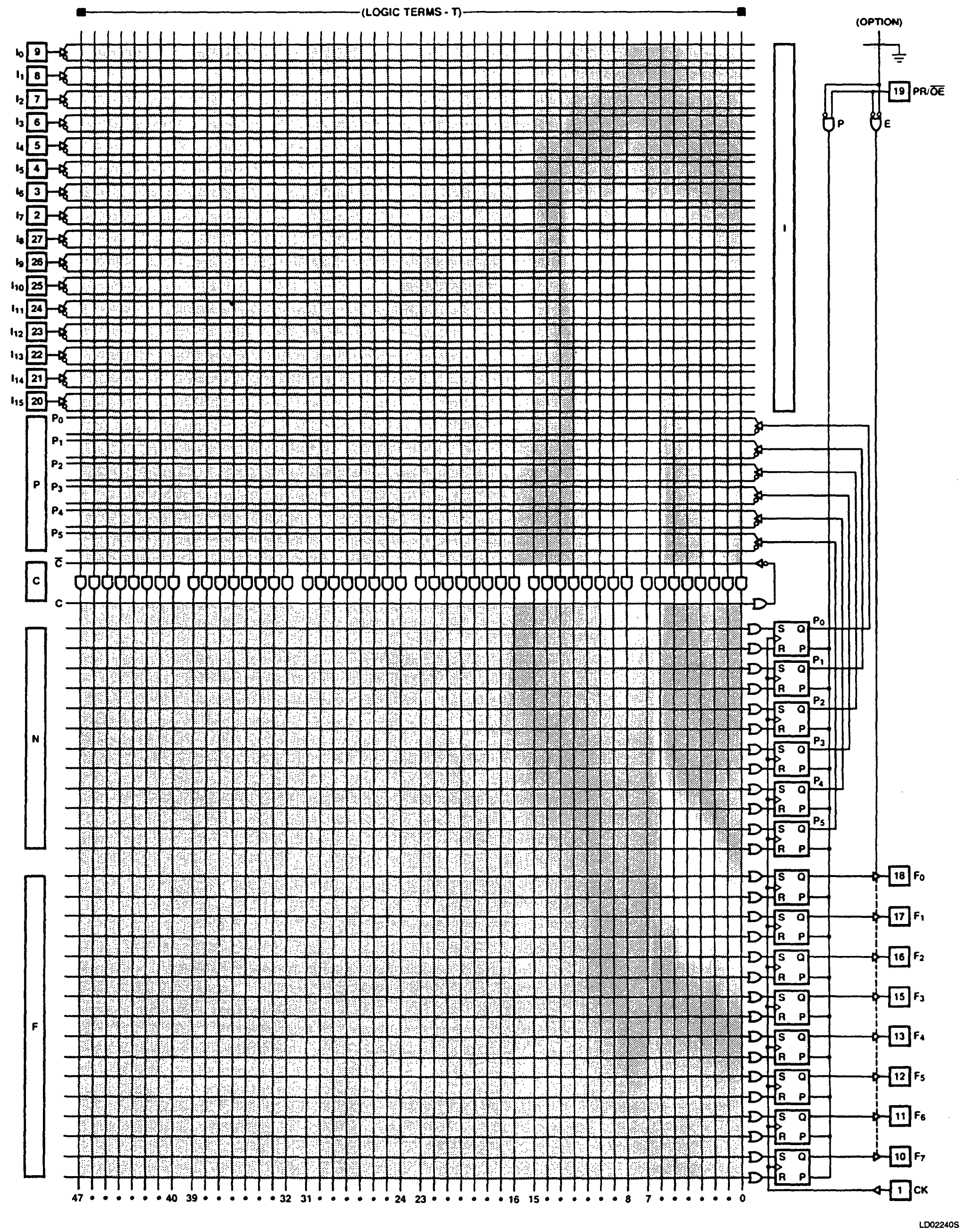
A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

   NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically when using any of Signetics' qualified programming equipment.

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

FPLS LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ◈ Programmable connection.

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	PLS105AN
28-pin Plastic Leaded Chip Carrier	PLS105AA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

[1] Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High[4]	I_{OH} = −2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250	μA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	μA
I_{OS}	Short circuit[3, 7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	180	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
5. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to PR/$\overline{OE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

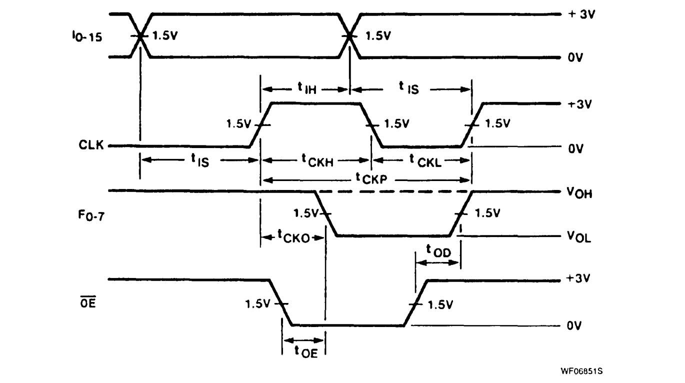
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Pulse width							
t_{CKH}	Clock[2] High	CK −	CK +	20	15		ns
t_{CKL}	Clock Low	CK +	CK −	20	15		
$t_{CKP1}B$	Period (without Complement Array)	CK +	CK +	50	40		
$t_{CKP2}B$	Period (with Complement Array)	CK +	CK +	80	50		
t_{PRH}	Preset pulse	PR −	PR +	25	15		
Setup time[3]							
$t_{IS1}A$	Input	CK +	Input ±	40			ns
$t_{IS1}B$	Input	CK +	Input ±	30			
$t_{IS2}A$	Input (through Complement Array)	CK +	Input ±	70			
$t_{IS2}B$	Input (through Complement Array)	CK +	Input	60			
t_{VS}	Power-on preset	CK −	V_{CC} +	0	−10		
t_{PRS}	Preset	CK −	PR −	0	−10		
Hold time							
t_{IH}	Input	Input ±	CK +	5	−10		ns
Propagation delay							
t_{CKO}	Clock	Output ±	CK +		15	20	ns
t_{OE}	Output enable	Output −	OE −		20	30	
t_{OD}	Output disable	Output +	OE +		20	30	
t_{PR}	Preset	Output +	PR +		18	30	
t_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	
Frequency of operation							
$f_{MAX}B$	Without Complement Array					20	MHz
$f_{MAX}B$	With Complement Array					12.5	

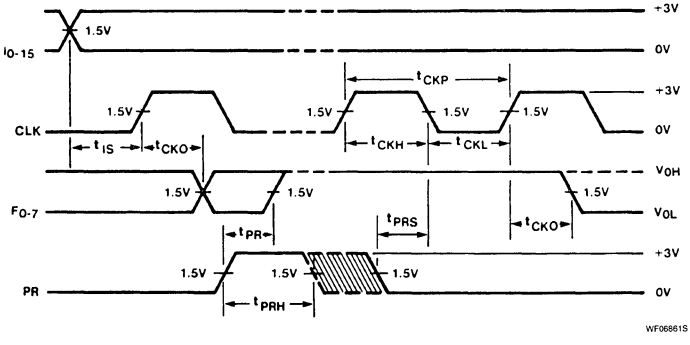
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. To prevent spurious clocking, clock rise time (10% − 90%) ⩽ 30ns.
3. See "Speed vs. OR Loading" diagrams.

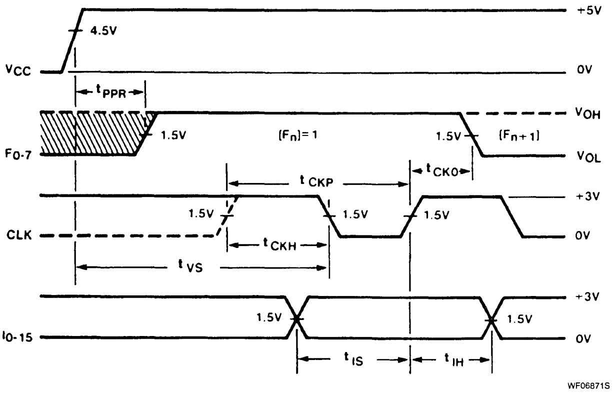
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset

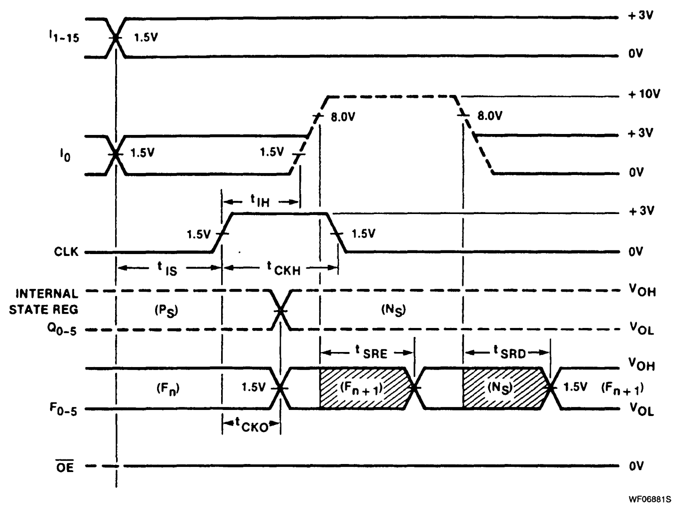


Power-On Preset

TIMING DEFINITIONS

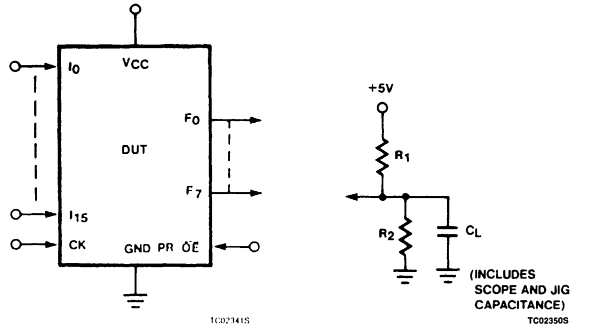
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period — when not using Complement Array.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{CKP2}	Clock period — when using Complement Array.
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{SRE}	Delay between input I_0 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{SRD}	Delay between input I_0 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

TIMING DIAGRAMS (Continued)

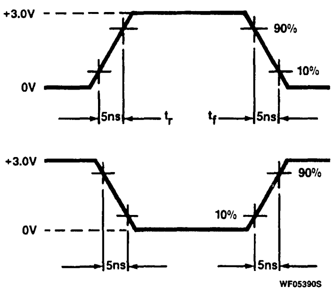


Diagnostic Mode

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

SPEED VS. "OR" LOADING

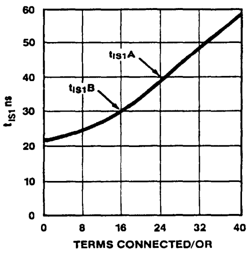
The maximum frequency at which the FPLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects $t_{IS,}$ due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The AC electrical characteristics contain two limits for the parameters t_{IS1} and t_{IS2}. The first, t_{IS1A} is guaranteed for a device with 24 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 16 terms connected to any OR line.

The two other entries in the AC table, t_{IS2} A and B are corresponding 24 and 16 term limits when using the on-chip Complement array.



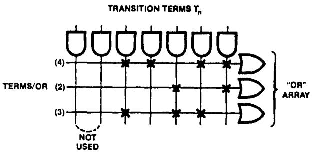
OP01251S

Figure 1. t_{IS1} vs. Terms/OR Connected

The worst case of t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to the interconnect pattern in the FPLS logic diagram, typically illustrated in Figure 2, or by counting the maximum number of "H" *or* "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.



AF01810S

Figure 2. Typical OR Array Interconnect Pattern

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

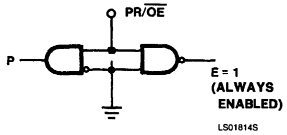
LOGIC PROGRAMMING

PLS105A logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

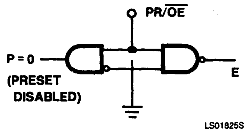
PLS105A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PRESET/$\overline{OE}$ OPTION – (P/E)



OPTION	CODE
PRESET^1	H

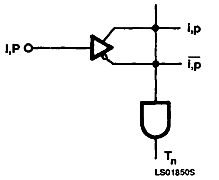


OPTION	CODE
$\overline{OE}$	L

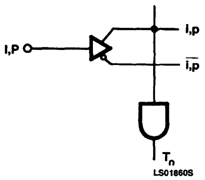
PROGRAMMING THE PLS105A:

The PLS105A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

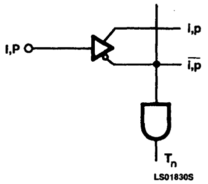
"AND" ARRAY – (I), (P)



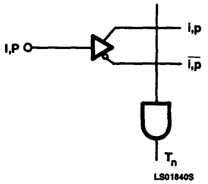
STATE	CODE
INACTIVE^{1,2}	O



STATE	CODE
I, P	H

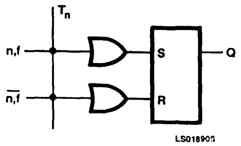


STATE	CODE
$\overline{I}$, $\overline{P}$	L

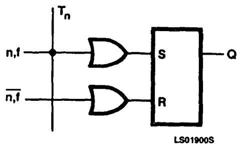


STATE	CODE
DON'T CARE	-

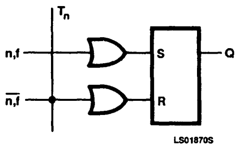
"OR" ARRAY – (N), (F)



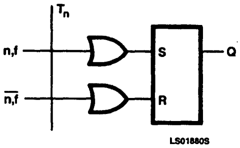
ACTION	CODE
INACTIVE^{1,3}	O



ACTION	CODE
SET	H

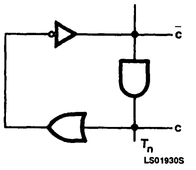


ACTION	CODE
RESET	L

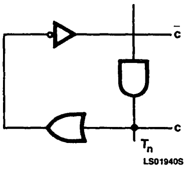


ACTION	CODE
NO CHANGE	-

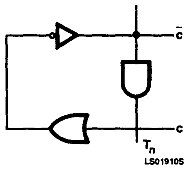
"COMPLEMENT" ARRAY – (C)



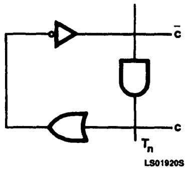
ACTION	CODE
INACTIVE^{1,4}	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	-

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
2. Any gate T_n will be unconditionally inhibited if both the true and complement fuses of any input (I,P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Field-Programmable Logic Sequencer (16 × 48 × 8) PLS105A

FPLS PROGRAM TABLE

CUSTOMER NAME ____________

PURCHASE ORDER # ____________

SIGNETICS DEVICE # CF (XXXX)

CUSTOMER SYMBOLIZED PART # ____________

TOTAL NUMBER OF PARTS ____________

PROGRAM TABLE ____________

REV ____________

DATE ____________

PROGRAM TABLE ENTRIES

AND

Cn

INACTIVE	0
GENERATE	A
PROPAGATE	●
TRANSPARENT	—

Im, Ps

INACTIVE	0
I, P	H
$\overline{I}, \overline{P}$	L
DON'T CARE	—

OR

Ns, Fr

INACTIVE	0
SET	H
RESET	L
NO CHANGE	—

OPTION

P/E

PRESET	H
$\overline{OE}$	L

AND																									OPTION (P/E)													
																									OR													
TERM	Cn	INPUT (Im)																PRESENT STATE (Ps)						REMARKS	NEXT STATE (Ns)						OUTPUT (Fr)							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																																						
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46																																						
47																																						
PIN NO.		20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9														10	11	12	13	15	16	17	18
VARIABLE NAME																																						

LD02251S

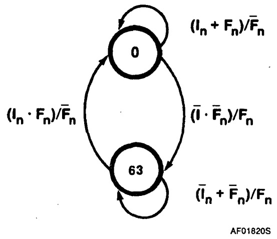
NOTES:
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exits in the table, shown BLANK instead for clarity.
2. Unsed C_n, I_m, and P_s bits are normally programmed Don't Care (-).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (-) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

TEST ARRAY

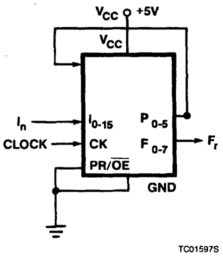
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-15} as shown in the test circuit timing diagram.


0
63
$(I_n + F_n)/\bar{F}_n$
$(I_n \cdot F_n)/\bar{F}_n$
$(\bar{I} \cdot \bar{F}_n)/F_n$
$(\bar{I}_n + \bar{F}_n)/F_n$
AF01820S

State Diagram



FPLS Under Test

TEST ARRAY PROGRAM

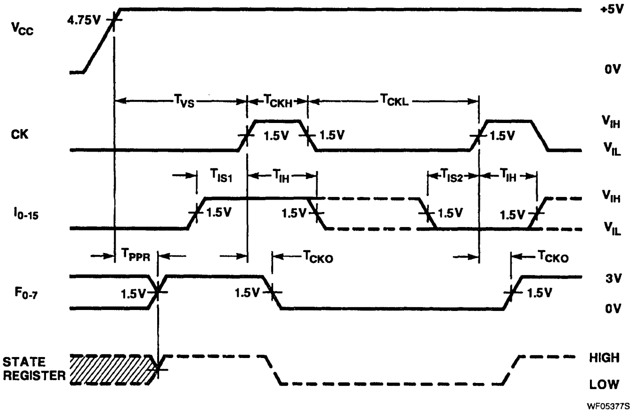
TERM	AND																						
	C	INPUT (Im)																PRESENT STATE (Ps)					
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)													H
OR													
NEXT STATE (Ns)						OUTPUT (Fr)							
5	4	3	2	1	0	7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

TB01760S

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.



Test Circuit Timing Diagram

TEST ARRAY DELETED

TERM	AND																						
	C	INPUT (Im)																PRESENT STATE (Ps)					
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0
48	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)													H
OR													
NEXT STATE (Ns)						OUTPUT (Fr)							
5	4	3	2	1	0	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—	—	—

TB01750S

Test Array Deleted

Signetics

PLUS405
Field-Programmable Logic Sequencer (16 × 64 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
• Series 28

DESCRIPTION

The PLUS405 is a bipolar, programmable state machine of the Mealy type. Both the AND and the OR array are user-programmable. All 64 AND gates are connected to the 16 external dedicated inputs ($I_0 - I_{15}$) and to the feedback paths of the 8 on-chip State Registers ($Q_{P0} - Q_{P7}$). Complement transition terms can be generated via optional use of the two internal Complement Arrays (input variables C_0, C_1).

All state transition terms can include True, False and Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective registers. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the State and Output Registers.

All state ($Q_{P0} - Q_{P7}$) and output ($Q_{F0} - Q_{F7}$) registers are edge-triggered, clocked J-K flip-flops, with Asynchronous Preset and Reset options. The PLUS405 architecture provides the added flexibility of the J-K toggle function which is indeterminate on S-R flip-flops. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "1". This feature allows the state machine to be asynchronously initialized to known internal state and output conditions prior to proceeding through a sequence of state transitions. Upon power-up, all registers are unconditionally preset to "1". If desired, the initialization input pin (INIT) can be converted to an $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) function as an additional user-programmable feature.

Availability of two user-programmable clocks allows the user to design two independently clocked state machine functions consisting of four state and four output bits each.

Order codes are listed in the Ordering Information Table.

FEATURES

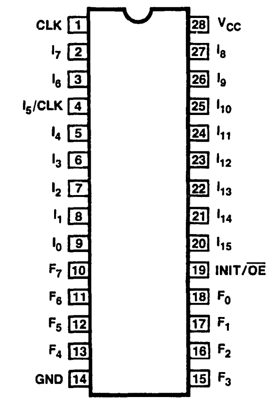
- Functional superset of PLS105/105A
- 50MHz clock rate
- f_{MAX} = 33MHz ($1/(t_{IS} + t_{CKO}) = f_{MAX}$)
- Field-programmable (Ti-W fusible link)
- 16 input variables
- 8 output functions
- 64 transition terms
- 8-bit State Register
- 8-bit Output Register
- 2 transition Complement Array terms
- Multiple clocks
- Programmable Asynchronous Initialization or $\overline{\text{Output Enable}}$
- Power-on preset of all registers to "1"
- 950mW power dissipation (typ.)
- TTL compatible
- J-K or S-R flip-flop functions
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

PIN CONFIGURATIONS

N Package

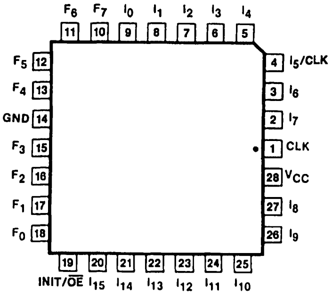


TOP VIEW

CD11463S

NOTE:
N = Plastic

A Package



CD04975S

NOTE:
A = Plastic Leaded Chip Carrier

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. Pin 1 only clocks P_{0-3} and F_{0-3} if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5-9, 26-27 20-22	$I_0 - I_4$, I_7, I_6 $I_8 - I_9$ $I_{13} - I_{15}$	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	I_5/CLK	**Logic Input/Clock:** A user programmable function: • **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P_{4-7} and Output Registers F_{4-7}, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I_{12}	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{12} is held at +10V, device outputs $F_0 - F_7$ reflect the contents of State Register bits $P_0 - P_7$. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I_{11}	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{11} is held at +10V, device outputs $F_0 - F_7$ become direct inputs for State Register bits $P_0 - P_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0 - F_7$ into the State Register bits $P_0 - P_7$. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I_{10}	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{10} is held at +10V, device outputs $F_0 - F_7$ become direct inputs for Output Register bits $Q_0 - Q_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0 - F_7$ into the Output Register bits $Q_0 - Q_7$. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10-13 15-18	$F_0 - F_7$	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits $Q_0 - Q_7$, when enabled. When I_{12} is held at +10V, $F_0 - F_7 = (P_0 - P_7)$. When I_{11} is held at +10V, $F_0 - F_7$ become inputs to State Register bits $P_0 - P_7$. When I_{10} is held at +10V, $F_0 - F_7$ become inputs to Output Register bits $Q_0 - Q_7$.	Active-High (H)
19	INIT/$\overline{\text{OE}}$	**Initialization or $\overline{\text{Output Enable}}$ Input:** **A user-programmable function:** • **Initialization:** Provides an asynchronous preset to logic "1" or reset to logic "0" of all State and Output Register bits, determined individually for each register bit through user programming. INIT overrides Clock, and when held High, clocking is inhibited and $F_0 - F_7$ are in their initialization state. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after INIT goes Low. See timing definition for t_{VCK} and t_{NVCK}.	Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an output enable function to buffers $F_0 - F_7$ from the Output Registers.	Active-Low (L)

Field-Programmable Logic Sequencer (16 × 64 × 8)

PLUS405

TRUTH TABLE [1, 2, 3, 4, 5, 6, 7]

V_{CC}	OPTION		I_{10}	I_{11}	I_{12}	CK	J	K	Q_P	Q_F	F
	INIT	$\overline{OE}$									
+5V	H		*	*	*	X	X	X	H/L	H/L	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L^9
	L		+10V	X	X	↑	X	X	Q_P	H	H^9
	L		X	+10V	X	↑	X	X	L	Q_F	L^9
	L		X	+10V	X	↑	X	X	H	Q_F	H^9
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
		X	+10V	X	X	↑	X	X	Q_P	L	L^9
		X	+10V	X	X	↑	X	X	Q_P	H	H^9
		X	X	+10V	X	↑	X	X	L	Q_F	L^9
		X	X	+10V	X	↑	X	X	H	Q_F	H^9
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	X	X	H

NOTES:

1. Positive Logic:
   $S/R \text{ (or } J/K) = T_0 + T_1 + T_2 + \ldots T_{63}$
   $T_n = (C_0, C_1)(I_0, I_1, I_2, \ldots)\ (P_0, P_1, \ldots P_7)$
2. Either Initialization (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H/L/+10V
5. X = Don't Care (⩽5.5V)
6. H/L implies that either a High or a Low can occur, depending upon user-programmed selection (each State and Output Register individually programmable).
7. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-stated and the indicated levels on the output pins are forced by the user.

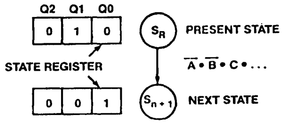
VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$ option is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All S/R (or J/K) flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array preprogrammed with a standard test pattern.

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

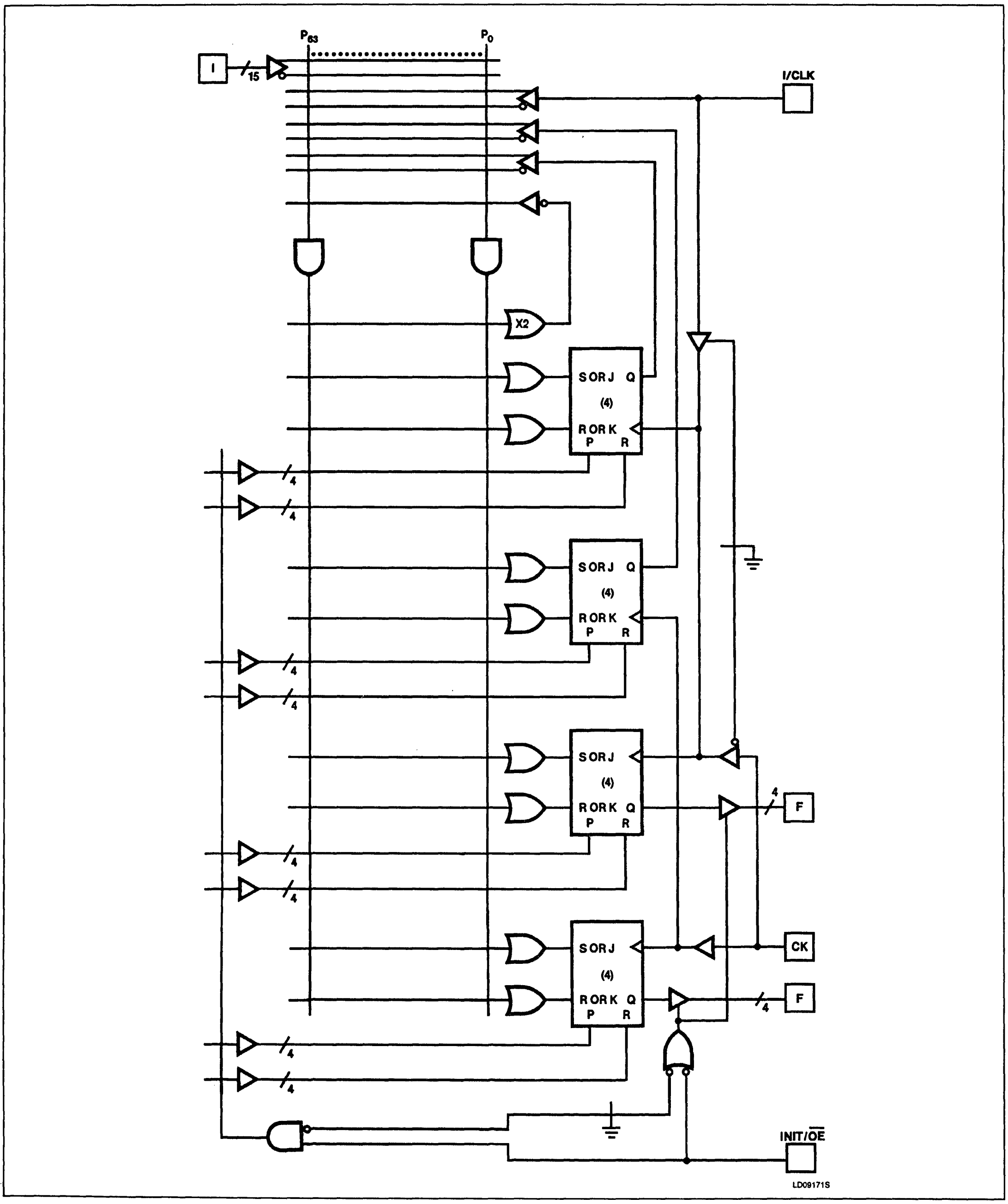
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

TB00900S

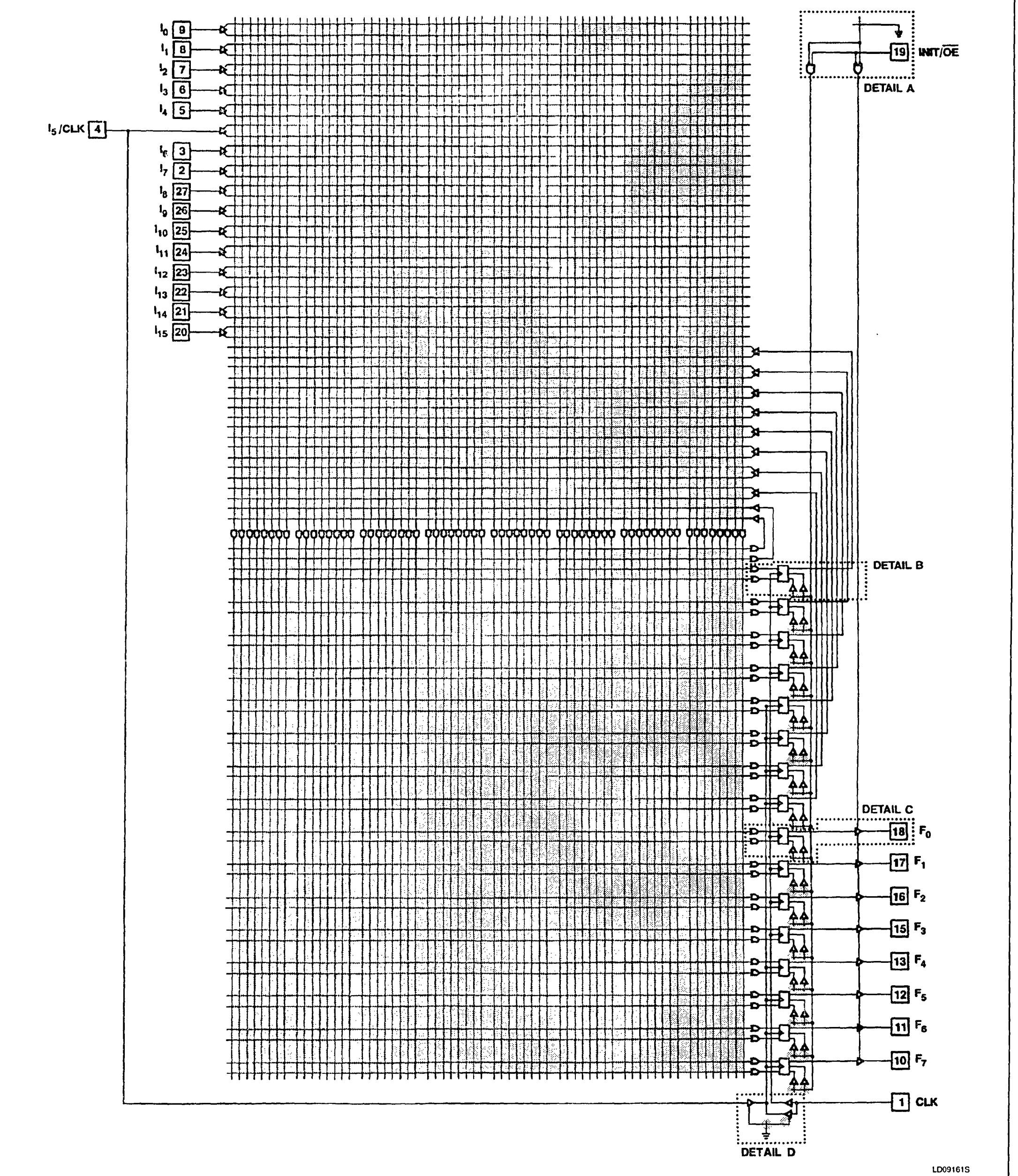
FUNCTIONAL DIAGRAM



Field-Programmable Logic Sequencer (16 × 64 × 8)

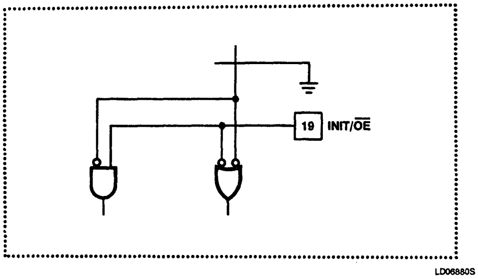
PLUS405

FPLS LOGIC DIAGRAM

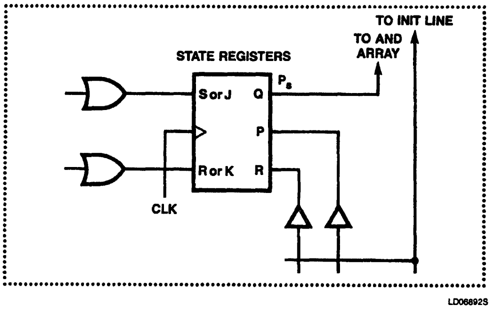


NOTE:
Denotes a programmable fuse location.

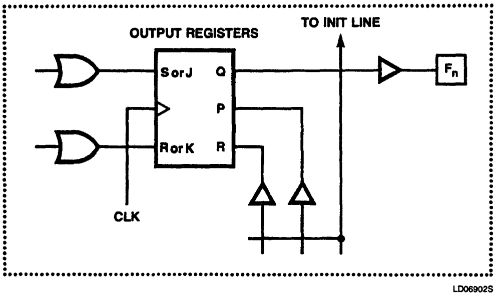
DETAILS FOR REGISTERS FOR PLUS405



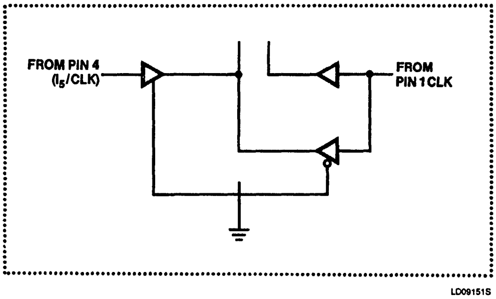
Detail A



Detail B



Detail C



Detail D

Field-Programmable Logic Sequencer (16 × 64 × 8)

PLUS405

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Plastic DIP (600mil-wide)	PLUS405N
28-Pin Plastic Leaded Chip Carrier	PLUS405A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	-30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

[1] Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		-0.8	-1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = Min, I_{OH} = −2mA	2.4			V
V_{OL}	Low	V_{CC} = Min, I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		-20	-250	μA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{CC} = Max, V_{OUT} = 5.5V		1	40	μA
		V_{CC} = Max, V_{OUT} = 0.45V		-1	-40	μA
I_{OS}	Short circuit[3, 4]	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = Max		190	225	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{CC} = 5.0V, V_{OUT} = 2.0V		10		pF

NOTES:

[1] All typical values are at V_{CC} = 5V, T_A = +25°C.

[2] All voltage values are with respect to network ground terminal.

[3] Test one at a time.

[4] Duration of short circuit should not exceed 1 second.

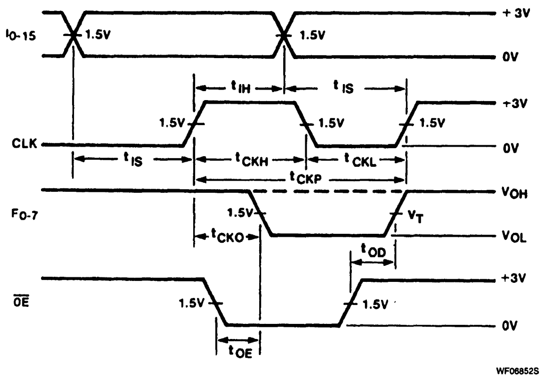
[5] I_{CC} is measured with the INIT/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75°CV \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Pulse width							
t_{CKH}	Clock High	CK –	CK +	10	8		ns
t_{CKL}	Clock Low	CK +	CK –	10	8		ns
t_{CKP1}	Period (without Complement Array)	CK +	CK +	30	25		ns
t_{CKP2}	Period (with Complement Array)	CK +	CK +	40	35		ns
t_{INITH}	Initialization pulse	INIT +	INIT –	15	8		ns
Setup time[2]							
t_{IS1}	Input	CK +	Input ±	15	12		ns
t_{IS2}	Input (through Complement Array)	CK +	Input ±	25	20		ns
t_{VS}	Power-on preset	CK –	V_{CC} +	0	–10		ns
t_{VCK}	Clock resume (after initiallization)	CK –	INIT –	0	–5		ns
t_{NVCK}	Clock lockout (before Initialization)	INIT –	CK –	15	5		ns
Hold time							
t_{IH}	Input	Input ±	CK +	0	–5		ns
Propagation delay							
t_{CKO}	Clock	Output ±	CK +		10	15	ns
t_{OE}	Output enable	Output –	OE –		12	15	ns
t_{OD}	Output disablo[3]	Output +	OE +		12	15	ns
t_{INIT}	Initialization	Output +	INIT +		15	20	ns
t_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	ns
Frequency of operation							
f_{MAX}	Without Complement Array With Complement Array					33 25	MHz

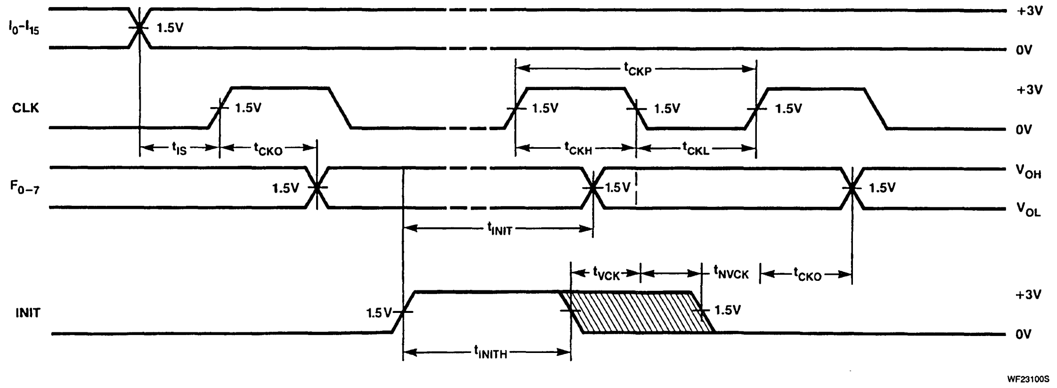
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. Product term loading considorations: Connecting more than 8 toggle mode registers to only one product term by itself may compromise the setup time performance. This restriction does not apply if toggle mode function is not used.
3. $C_L = 5pF$; $V_T = V_{OL} + 0.5V$.

TIMING DIAGRAMS

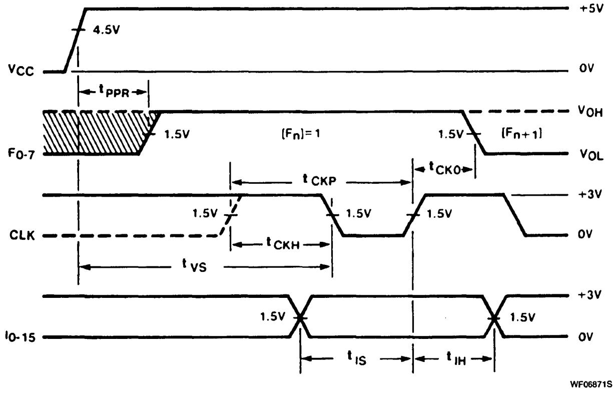


Sequential Mode

TIMING DIAGRAMS (Continued)

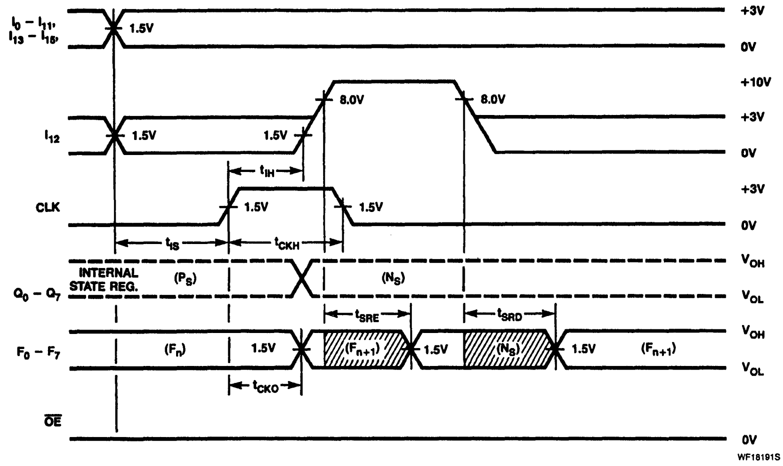


Asynchronous Initialization

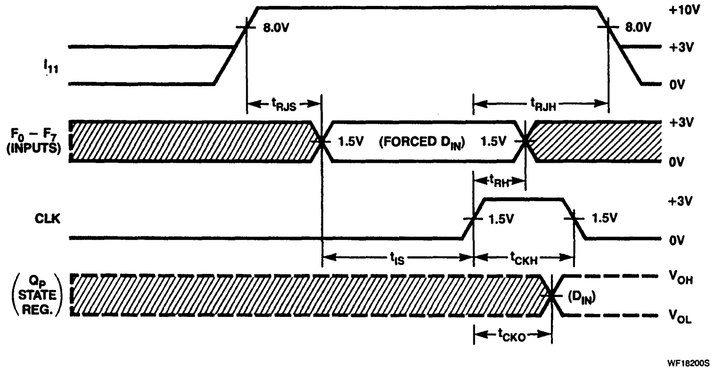


Power-On Preset

TIMING DIAGRAMS (Continued)

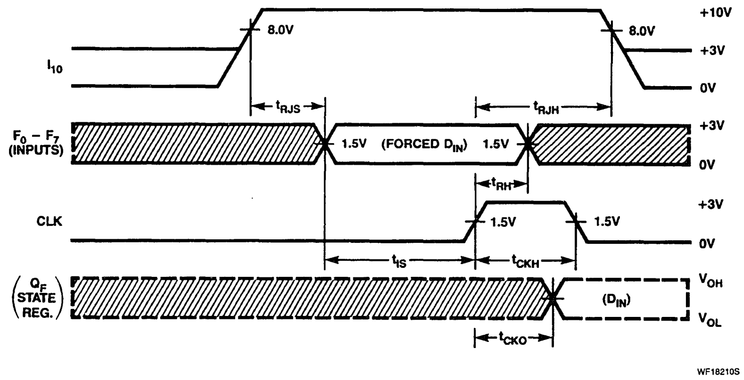


Diagnostic Mode — State Register Outputs



Diagnostic Mode — State Register Input Jam

TIMING DIAGRAMS (Continued)



Diagnostic Mode — Output Register Input Jam

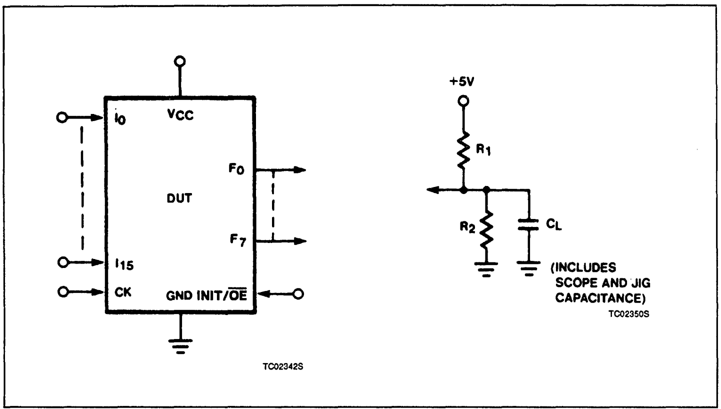
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKP}	Clock period — when not using Complement Array.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with INIT/$\overline{OE}$ Low).
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{RJH}	Required delay between positive transition of Clock and end of inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively.
f_{MAX}	Maximum clock frequency.

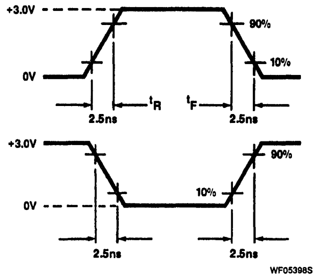
SYMBOL	PARAMETER
t_{CKL}	Interval between clock pulses.
t_{CKP2}	Clock period — when using Complement Array.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{SRE}	Delay between input I_{12} transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{RJS}	Required delay between inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively, and when the ouput pins become available as inputs.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization to guarantee that the clock edge is not detected as a valid negative transition.

SYMBOL	PARAMETER
t_{INITH}	Width of initialization input pulse.
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{INIT}	Delay between positive transition of Initialization and when Outputs become valid.
t_{SRD}	Delay between input I_{12} transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jaming data into State or Output Registers in diagnostic mode.
t_{VCK}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding first reliable clock pulse.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

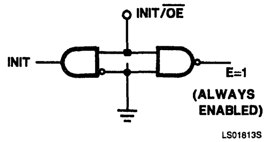
LOGIC PROGRAMMING

PLUS405 Logic designs can be generated using Signetics' AMAZE design software or several other commercially availabe, JEDEC standard PLD design software packages. Boolean and/or state equation entry format is accepted.

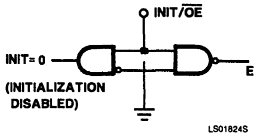
PLUS405 logic designs can also be generated using the program table format detailed on the following page(s). This Program Table Entry Format (PTE) is supported by the Signetics' AMAZE PLD design software. AMAZE is available free of charge to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations is assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION/$\overline{OE}$ OPTION — (INIT/$\overline{OE}$)



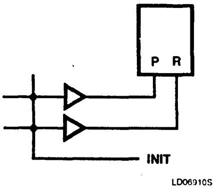
OPTION	CODE
INITIALIZATION[1]	H



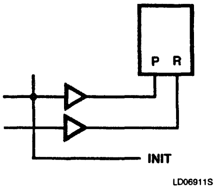
OPTION	CODE
$\overline{OE}$	L

PROGRAMMING THE PLUS405:
The PLUS405 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

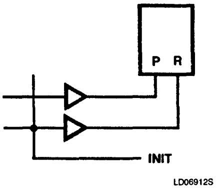
PRESET/RESET OPTION — (P/R)



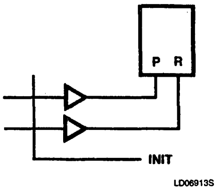
ACTION	CODE
INDETERMINATE[4]	O



ACTION	CODE
PRESET	H

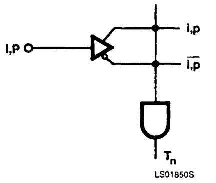


ACTION	CODE
RESET	L

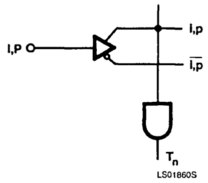


ACTION	CODE
INDETERMINATE[4]	-

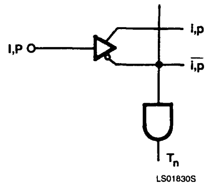
"AND" ARRAY — (I), (P)



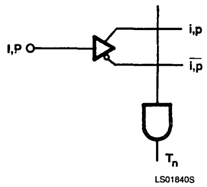
STATE	CODE
INACTIVE[1, 2]	O



STATE	CODE
I, P	H

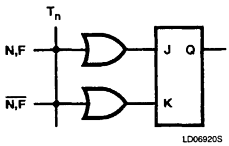


STATE	CODE
$\bar{I}$, $\bar{P}$	L

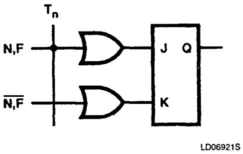


STATE	CODE
DON'T CARE	-

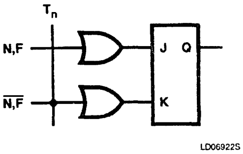
"OR" ARRAY — J-K FUNCTION — (N), (F)



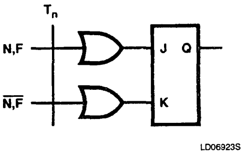
ACTION	CODE
TOGGLE[6]	O



ACTION	CODE
SET	H

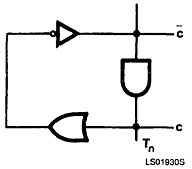


ACTION	CODE
RESET	L

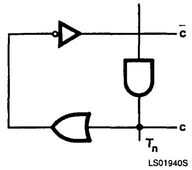


ACTION	CODE
NO CHANGE	-

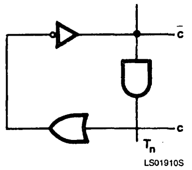
"COMPLEMENT" ARRAY — (C)



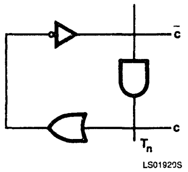
ACTION	CODE
INACTIVE[1, 3]	O



ACTION	CODE
GENERATE	A

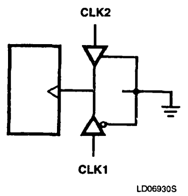


ACTION	CODE
PROPAGATE	•

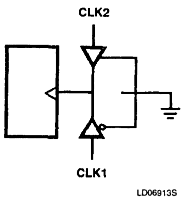


ACTION	CODE
TRANSPARENT	-

CLOCK OPTION — (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY	L



OPTION	CODE
CLK1 and CLK2[5]	H

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. These states are not allowed when using PRESET/RESET option.
5. Input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6. A single product term cannot drive more than 8 registers by itself when used in TOGGLE mode.

PLUS405 FPLS PROGRAM TABLE

AND

INACTIVE	0
I, P	H
Ī, P̄	L
DON'T CARE	–

Im, Ps

INACTIVE	0
GENERATE	A
PROPAGATE	•
TRANSPARENT	–

Cn

OR

INACTIVE OR TOGGLE	0
SET	H
RESET	L
NO CHANGE	–

Ns, Fr

OPTIONS

INIT	H
$\overline{OE}$	L

INIT/$\overline{OE}$

CLK1 ONLY	L
CLK1 AND 2	H

CLK1/CLK2

CUSTOMER NAME ____________

SIGNETICS DEVICE # ____________ CF (XXXX) ____________

CUSTOMER SYMBOLIZED PART # ____________

REV ____________ DATE ____________

PROGRAM TABLE ____________

																			CLOCK 1/2								INITIALIZATION/OUTPUT ENABLE															
	AND																										OR															
	COMP. ARRAY		INPUT (Im)																PRESENT STATE (Ps)								NEXT STATE (Ns)								OUTPUT (Fr)							
	C1	C0	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	P7	P6	P5	P4	P3	P2	P1	P0	N7	N6	N5	N4	N3	N2	N1	N0	F7	F6	F5	F4	F3	F2	F1	F0
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PIN NO.			20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9																	10	11	12	13	15	16	17	18
PIN LABELS																																										

TB03142S

NOTES:
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the IN/E and H for the clock option, exits in the table, shown BLANK instead for clarity.
2. Unused Cn Im, and Ps bits are normally programmed Don't Care (—).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (—) for maximum speed.

Signetics

Section 6
PML Data Sheets

Application Specific Products

INDEX

PLHS501 Programmable Macro Logic 6-3

PLHS502 Programmable Macro Logic 6-13

Signetics

PLHS501
Programmable Macro Logic

Product Specification

Applied Specific Application Products • PML Series

FEATURES

- Programmable instant gate array
- SNAP development system:
  - Supports third-party schematic entry formats
  - Macro library
  - Versatile netlist format for design portability
  - Logic, timing, and fault simulation
- AMAZE development system:
  - Supports third-party schematic entry formats
  - Boolean equation entry
  - Logic, timing, and fault simulation
- TTL compatible
- Power dissipation = 1.12W (typ.)

PROPAGATION DELAYS

- Single level (excluding the internal core) = 22ns (max)
- Two level (through the internal core) = 30ns (max)
- Delay per internal NAND function = 8ns (max)

STRUCTURE

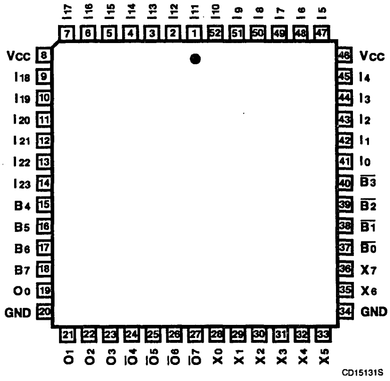
- NAND gate based architecture:
  - 72 foldback NAND terms
- 24 dedicated inputs (I0 - I23)
- 8 bidirectional I/Os with individual 3-State enable:
  - 4 active-High (B4 - B7)
  - 4 active-Low (/B0 - /B3)
- 16 dedicated outputs:
  - 4 active-High outputs:
    O0, O1 with common 3-State enable
    O2, O3 with common 3-State enable
  - 4 active-Low outputs:
    $\overline{O4}$, $\overline{O5}$ with common 3-State enable
    $\overline{O6}$, $\overline{O7}$ with common 3-State enable
  - 8 Exclusive-OR outputs:
    X0 - X3 with common 3-State enable
    X4 - X7 with common 3-State enable
- Security fuse allows protection of proprietary designs
- Testable in unprogrammed state

DESCRIPTION

The PLHS501 is a high-density Bipolar Programmable Macro Logic device. PML incorporates a programmable NAND structure. The NAND architecture is an efficient method for implementing any logic function. The SNAP software development system provides a user friendly environment for design entry. SNAP eliminates the need for a detailed understanding of the PLHS501 architecture and makes it transparent to the user. PLHS501 is also supported on the Signetics AMAZE software development system.

PIN CONFIGURATION

A Package
(52-pin PLCC)



ARCHITECTURE

The core of the PLHS501 is a programmable fuse array of 72 NAND gates. The output of each gate folds back upon itself and all other NAND gates. In this manner total interconnectivity of all logic functions is achieved in the PLHS501. Any logic function can be created within the core of the device without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers.

DESIGN DEVELOPMENT TOOLS

SNAP

The SNAP Software Development System provides the necessary tools for designing with PML. SNAP provides the following:

- Schematic entry netlist generation from third party schematic design packages such as OrCAD/STD^{TM} and FutureNet^{TM}.
- Macro library for standard PLHS501 functions and user defined functions
- Boolean equation entry
- State equation entry
- Syntax and design entry checking
- Simulator includes logic simulation, fault simulation, automatic test vector generation, and timing simulation.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. The minimum system configuration for SNAP is 640K bytes of RAM and a hard disk.

SNAP provides primitive PML function libraries for third-party schematic design packages. Custom macro function libraries can be defined in schematic or equation form.

After the completion of a design, the software compiles the design for syntax and completeness. Complete simulation can be carried out using the different simulation tools available.

The programming data is generated in JEDEC format. Using the Device Programmer Interface (DPI) module of SNAP, the JEDEC fusemap is sent from the host computer to the device programmer.

AMAZE

The AMAZE PLD Design Software development system also supports the PLHS501. AMAZE provides the following capabilities for the PLHS501:

- Schematic entry netlist conversion from third-party schematic software
- Boolean equation entry
- Logic and timing simulation
- Automatic test vector generation

AMAZE operates on an IBM PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.0 or higher. The minimum system configuration for AMAZE is 640K bytes of RAM and a hard disk.

AMAZE compiles the design after completion for syntax and completeness. Programming data is generated in JEDEC format.

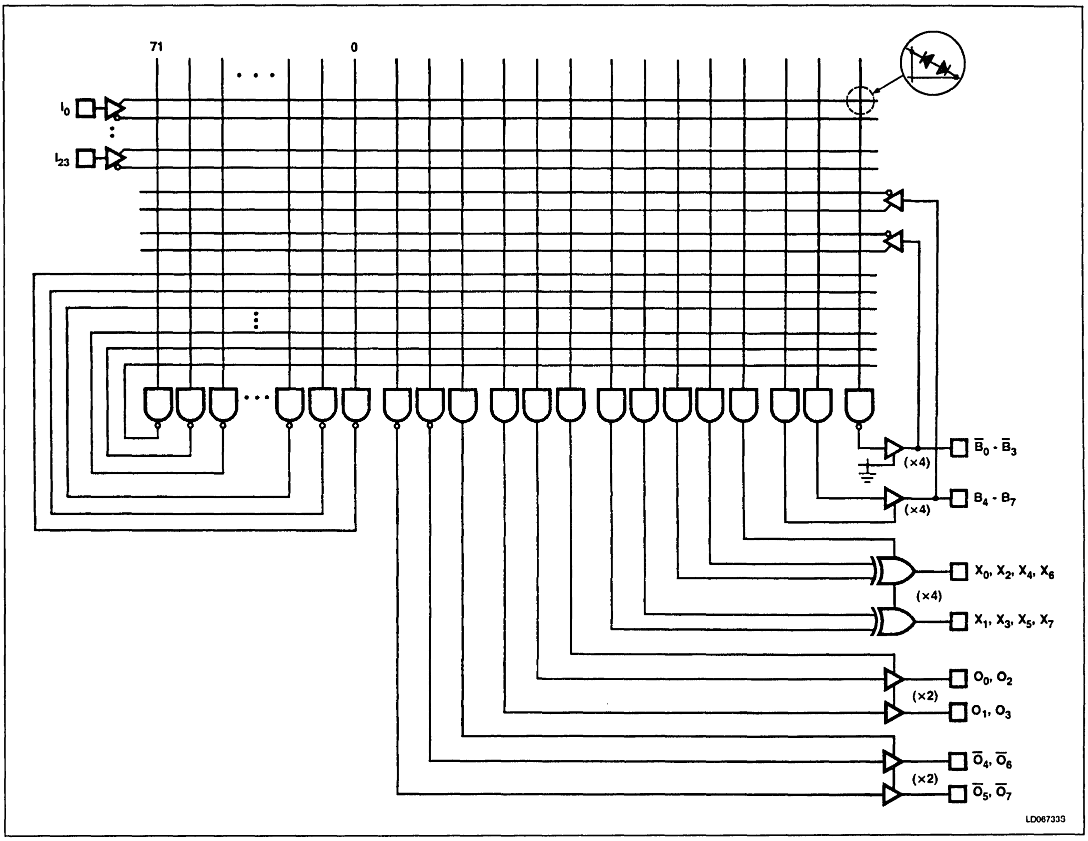
DESIGN SECURITY

The PLHS501 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

FutureNet is a trademark of FutureNet Corporation.
OrCAD/STD is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

Programmable Macro Logic | PLHS501

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
52-Pin Plastic Leaded Chip Carrier	PLHS501A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

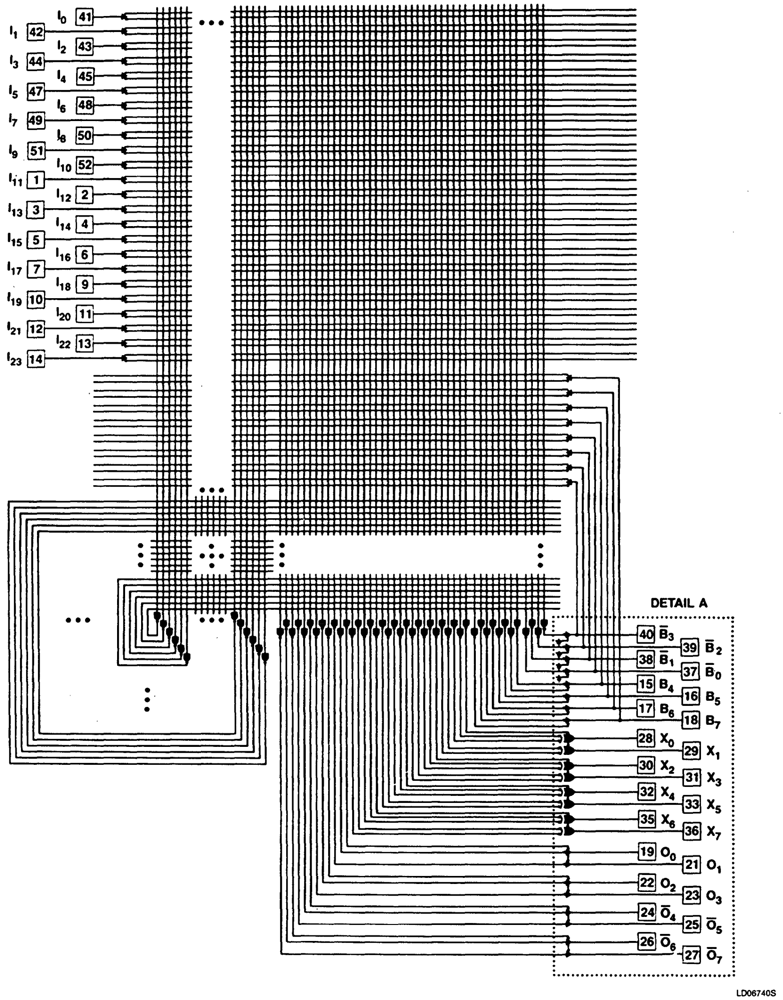
TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

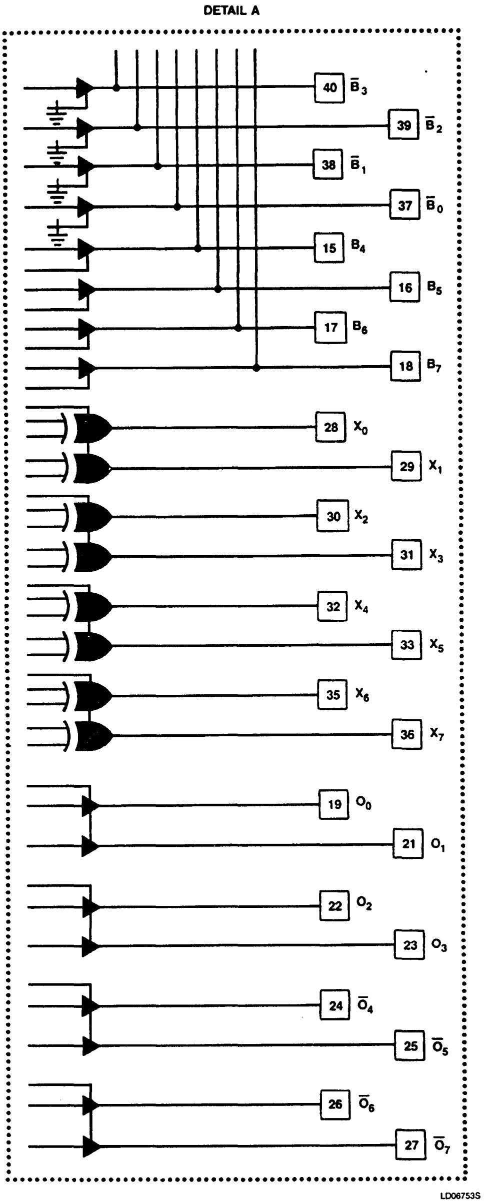
VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:

1. All product terms are enabled.
2. All bidirectional (B) pins are outputs.
3. All outputs are enabled.
4. All outputs are active-High **except** $\overline{B}_0 - \overline{B}_3$ (fusable I/O) and $\overline{O}_4 - \overline{O}_7$ which are active-Low.

LOGIC DIAGRAM




DETAIL A
40 B̄3
39 B̄2
38 B̄1
37 B̄0
15 B4
16 B5
17 B6
18 B7
28 X0
29 X1
30 X2
31 X3
32 X4
33 X5
35 X6
36 X7
19 O0
21 O1
22 O2
23 O3
24 Ō4
25 Ō5
26 Ō6
27 Ō7
LD06753S

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[2, 3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage						
		V_{CC} = Min				
V_{OL}	Low[2, 4]	I_{OL} = 10mA			0.45	V
V_{OH}	High[2, 5]	I_{OH} = −2mA	2.4			V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[9]	V_{OUT} = 5.5V			80	μA
		V_{OUT} = 0.45V			−140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		225	295	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_{OUT} = 2.0V		15		pF

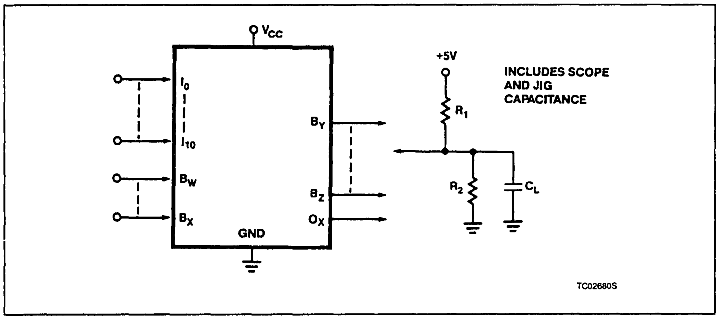
AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+75°C$, $4.75 < V_{CC} < 5.25V$, $R_1 = 470\Omega$, $R_2 = 1000\Omega$

SYMBOL	PARAMETER		TEST CONDITION	LIMITS			UNIT
	TO	FROM		Min	Typ	Max	
t_{PD1}	Output ±	Input ±	C_L = 30pF			25	ns
t_{PD2}	Output ±	Input ±				25	ns
t_{PD3}	Output ±	Input ±				22	ns
t_{PD4}[10]	Output ±	Input ±				30	ns
t_{PD5}[10]	Output ±	Input ±				30	ns
t_{PD6}[10]	Output ±	Input ±				28	ns
t_{PD7}	Internal					8	ns
t_{OE}	Output −	Input ±				26	ns
t_{OD}[8]	Output +	Input ±	C_L = 5pF			26	ns

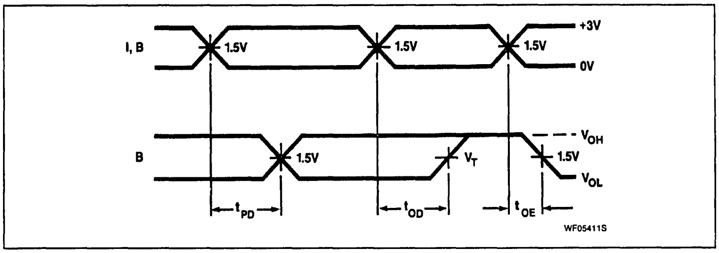
NOTES:

1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. For Pins 15-19, 21-27 and 37-40, V_{OL} is measured with Pins 5 and 41 = 8.75V, Pin 43 = 0V and Pins 42 and 44 = 4.5V. For Pins 28-33 and 35-36, V_{OL} is measured under same conditions EXCEPT Pin 44 = 0V.
5. V_{OH} is measured with Pins 5 and 41 = 8.75V, Pins 42 and 43 = 4.5V and Pin 44 = 0V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with all dedicated inputs at 0V and bidirectional and output pins open.
8. Measured at $V_T = V_{OL} + 0.5V$.
9. Leakage values are a combination of input and output leakage.
10. Limits are guaranteed with internal feedback buffers simultaneously switching cumulative maximum of eight outputs.

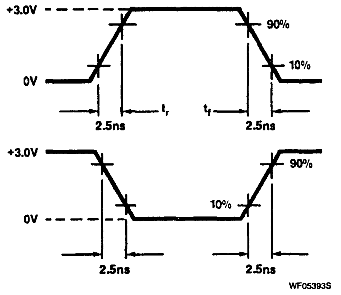
TEST LOAD CIRCUITS



TIMING DIAGRAMS



VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

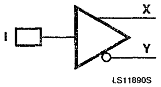
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD1}	Input to Output delay, one pass, through X outputs.
t_{PD2}	Input to Output delay, one pass, through $\overline{B}$ outputs.
t_{PD3}	Input to Output delay, one pass, through O, $\overline{O}$ and B outputs.
t_{PD4}	Input to Output delay, two passes, through X outputs.
t_{PD5}	Input to Output delay, two passes, through $\overline{B}$ outputs.
t_{PD6}	Input to Output delay, two passes, through O, $\overline{O}$ and B outputs.
t_{PD7}	Feedback delay per internal NAND function performed.
t_{OD}	Delay between output change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when the output reflects specified output level.

Programmable Macro Logic PLHS501

MACRO CELL SPECIFICATIONS

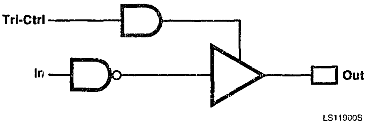
Input Buffer



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	X X	I I		6 7		ns
t_{PHL} t_{PLH}	Y Y	I I		4.5 6		ns

Input Pins: 1 – 7, 9 – 14, 41 – 45, 48 – 52
Bidirectional Pins: 15 – 18, 37 – 40

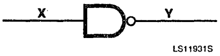
NAND Output Buffer with 3-State Control



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Out Out	In In		10.5 9.0		ns
t_{OE} t_{OD}	Out Out	Tri-Ctrl Tri-Ctrl		9.5 9.5		ns

Output Pins: 24 – 27

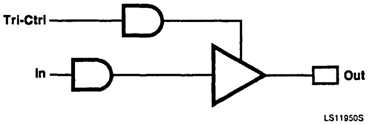
Internal Fold Back NAND



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Y Y	X X		5.5 6.5		ns

MACRO CELL SPECIFICATIONS (Continued)

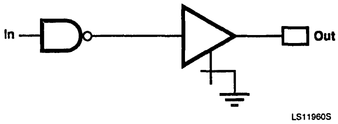
AND Output Buffer with 3-State Control



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Output Output	In In		10 8.5		ns
t_{OE} t_{OD}	Out Out	Tri-Ctrl Tri-Ctrl		9.5 9.5		ns

Bidirectional and Output Pins: 19, 21, 22, 23, 15 – 18

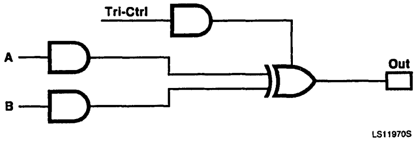
NAND Output Buffer



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}				10.5 9		

Bidirectional Pins: 37 – 40

Ex-OR Output Buffer



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Out Out	A or B A or B		10 12		ns
t_{OE} t_{OD}	Out Out	Tri-Ctrl Tri-Ctrl		9.5 9.5		ns

Ex-OR Output Pins: 28 – 33

PLHS501 GATE COUNT EQUIVALENTS

FUNCTION	PLHS501 INTERNAL NAND EQUIVALENT	COMMENTS
Gates:		
NANDs	1	For 1 to 32 input variables.
ANDs	1	For 1 to 32 input variables.
NORs	1	For 1 to 32 input variables.
ORs	1	For 1 to 32 input variables.
Decoders:		
3 to 8	8	Inverted inputs available.
4 to 16	16	Inverted inputs available.
5 to 32	32	Inverted inputs available (24 chip outputs only).
Encoders:		
8 to 3	15	Inverted inputs, 2 logic levels.
16 to 4	32	Inverted inputs, 2 logic levels.
32 to 5	41	Inverted inputs, 2 logic levels, factored solution.
Multiplexers:		
4 to 1	5	Inverted inputs available.
8 to 1	9	
16 to 1	17	
27 to 1	28	Can address only 27 external inputs – more if internal.
Flip-Flops:		
D – FF	6	With asynch S – R.
T – FF	6	With asynch S – R.
J – K – FF	10	With asynch S – R.
Adders:		
8-bit	45	Full carry-lookahead (four levels of logic).
Barrel Shifters:		
8-bit	72	2 levels of logic.
Latches		
D-latch	3	2 levels of logic with one shared gate.

Signetics

PLHS502
Programmable Macro Logic

Preliminary Specification

Application Specific Products

FEATURES

- Programmable instant gate array
- SNAP development system
  - Supports third-party schematic entry formats
  - Macro library
  - Versatile netlist format for design portability
  - Logic, timing, and fault simulation
- TTL compatible
- Power dissipation = 1.25W (typ.)

PROPAGATION DELAYS

- Single level (excluding the internal core) = 22ns (max)
- Two level (through the internal core) = 30ns (max)
- Delay per internal NAND function = 8ns (max)
- Maximum operating frequency = 50MHz (internal flip-flop)

STRUCTURE

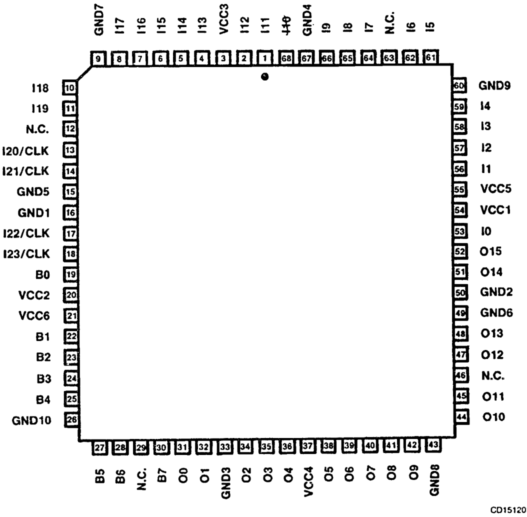
- NAND gate based architecture
  - 64 foldback NAND terms
- 20 dedicated inputs
- 4 programmable input/clock inputs
- 8 independent clocks
  - 4 from input/clock pins
  - 4 from NAND array
- 8 bidirectional I/Os
- 16 dedicated outputs
  - 8 active-High outputs
  - 4 outputs with programmable polarity
  - 4 3-State outputs with programmable polarity
- 16 buried flip-flops
  - 8 D type
  - 8 S-R type
- Security fuse allows protection of proprietary designs
- Testable in unprogrammed state

DESCRIPTION

The PLHS502 is a high-density Bipolar Programmable Macro Logic device. PML incorporates a programmable NAND structure. The NAND architecture is an efficient method for implementing any logic function. The SNAP software development system provides a user friendly environment for design entry. SNAP eliminates the need for a detailed understanding of the PLHS502 architecture and makes it transparent to the user.

PIN CONFIGURATION

A Package
(68-pin PLCC)



Programmable Macro Logic PLHS502

ARCHITECTURE

The core of the PLHS502 is a programmable fuse array of 64 NAND gates and 16 buried flip-flops. The output of each gate and flip-flop folds back upon itself and all other NAND gates and flip-flops. In this manner, total interconnectivity of all logic functions is achieved in the PLHS502. Any logic function can be created within the core of the device without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers.

- Buried Flip-Flops
  The 16 buried flip-flops can be connected to the input or output structures through the NAND array. Intricate state machine designs can be implemented within the core without any unnecessary delays from the input or output buffers. Each flip-flop can be realized as an input or output register with no constraints.
- The Clock Array
  The 16 buried flip-flops (8-D and 8 S-R) can be clocked individually through the 'Clock Array'. The Clock Array consists of 8 individual clocks, 4 directly from the input pins and 4 from the NAND array. The clock inputs from the NAND array enable the user to create different functions for clocking the flip-flops. This, together with the fully interconnectivity of the device, offers the capability to implement a variety of synchronous and asynchronous state machines as well as multi-phase design, such as pipelined processing.

DESIGN DEVELOPMENT TOOLS

The SNAP Software Development System provides the necessary tools for designing with PML. SNAP provides the following:

- Schematic entry netlist generation from third-party schematic design packages such as OrCAD/STD^{TM} and FutureNet^{TM}.
- Macro library for standard PLHS502 functions and user defined functions
- Boolean equation entry
- State equation entry
- Syntax and design entry checking
- Simulator includes logic simulation, fault simulation, automatic test generation, and timing simulation.

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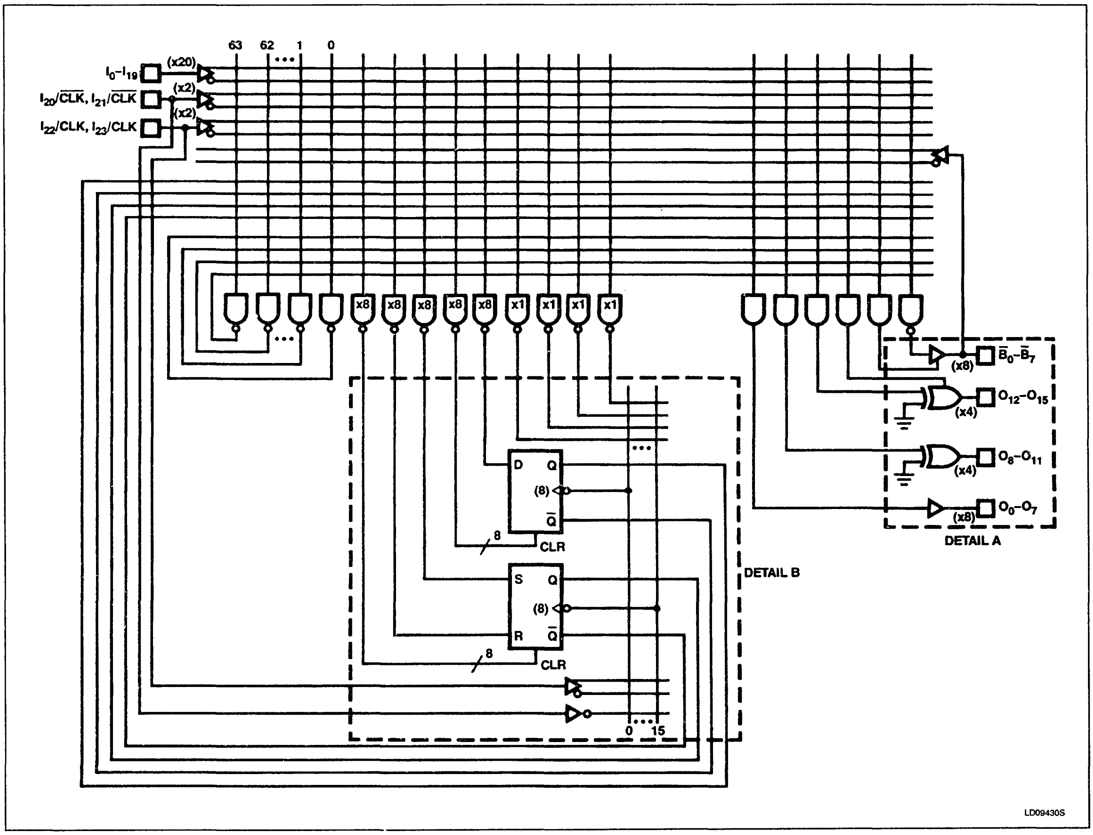
The programming data is generated in JEDEC format. Using the Device Programmer Interface (DPI) module of SNAP, the JEDEC fusemap is sent from the host computer to the device programmer.

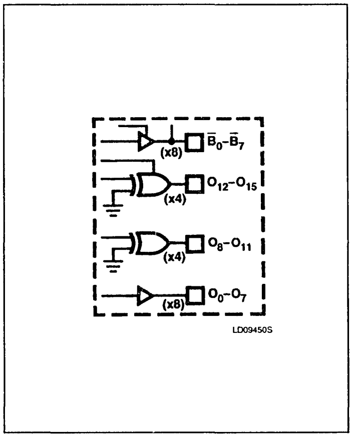
DESIGN SECURITY

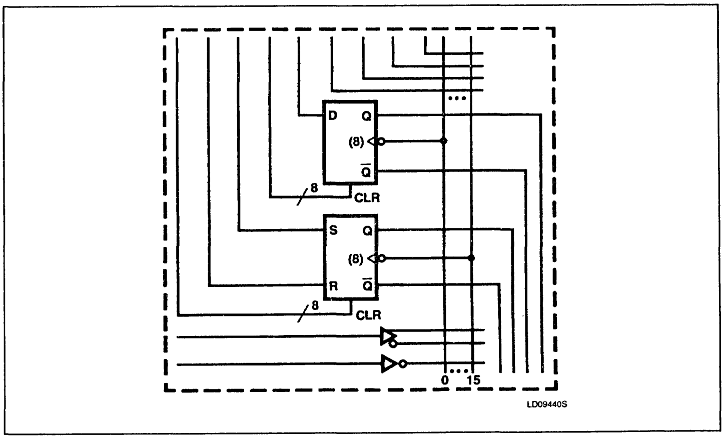
The PLHS502 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

FutureNet is a trademark of FutureNet Corporation.
OrCAD/STD is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

FUNCTIONAL DIAGRAM







Programmable Macro Logic

PLHS502

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
68-Pin Plastic Leaded Chip Carrier	PLHS502A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_A	Operating temperature range	0	+75	°C
T_{STG}	Storage temperature range	-65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:

1. All bidirectional (B) pins are outputs.
2. All outputs are enabled.
3. All outputs are active-Low **except** $O_0 - O_7$, which are active-High.

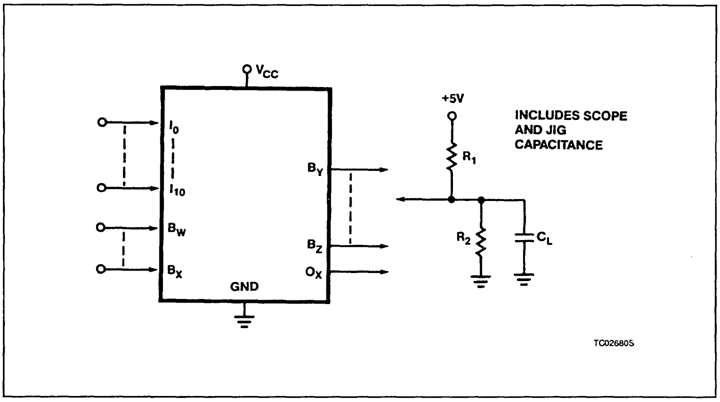
DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[2]	V_{CC} = Min, I_{IN} = -12mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = Min				
V_{OL}	Low[2]	I_{OL} = 10mA			0.45	V
V_{OH}	High[2]	I_{OH} = -2mA	2.4			V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			-140	
I_{OS}	Short circuit	V_{OUT} = 0V	-15		-70	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max			375	mA
Capacitance						
		V_{CC} = 5V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_{OUT} = 2.0V		15		pF

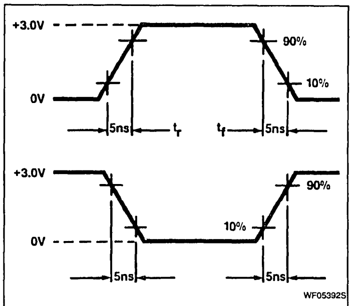
NOTES:

1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.

TEST LOAD CIRCUITS



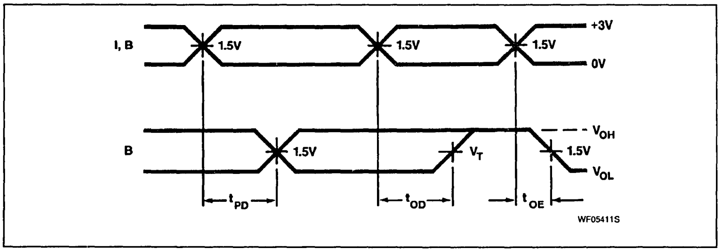
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the + 1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAMS



AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+75°C$, $4.75 < V_{CC} < 5.25V$, $R_1 = 470\Omega$, $R_2 = 1000\Omega$

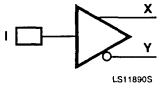
SYMBOL	PARAMETER	LIMITS		
		Min	Typ	Max
Non registered operations				
t_{PD1}	Input to output delay — no NAND feedback w/Ex-OR buffer		17ns	22ns
t_{PD2}	Input to output delay — no NAND feedback w/NAND buffer		15ns	20ns
t_{PD3}	Input to output delay — no NAND feedback w/AND buffer		15ns	20ns
t_{PD4}	Input to output delay — w/1 NAND feedback w/Ex-OR buffer		22ns	30ns
t_{PD5}	Input to output delay — w/1 NAND feedback w/NAND buffer		20ns	28ns
t_{PD6}	Input to output delay — w/1 NAND feedback w/AND buffer		20ns	28ns
t_{PD7}	Feedback delay per internal NAND function performed		5ns	8ns
t_{OE}	Output enable time — no NAND feedback		20ns	25ns
t_{OD}	Output disable time — no NAND feedback		18ns	22ns

AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 0°C$ to $+75°C$, $4.75 < V_{CC} < 5.25V$, $R_1 = 470\Omega$, $R_2 = 1000\Omega$

SYMBOL	PARAMETER	LIMITS		
		Min	Typ	Max
Registered operations from dedicated clock inputs				
t_{IS1}	Input to clock setup time	10ns	6ns	
t_{IS2}	NAND feedback to clock setup time (not including t_{D7})	5ns	3ns	
t_{IH1}	Input hold time	4ns	3ns	
t_{IH2}	NAND feedback to clock hold time	7ns	5ns	
t_{CK0}	Clock to output (includes NAND output buffer delay)		20ns	25ns
t_{CK1}	Clock to output (includes AND output buffer delay)		20ns	25ns
t_{CK2}	Clock to output (includes Ex-OR output buffer delay)		22ns	27ns
t_{CK3}	Clock to output (includes NAND output buffer delay +1 feedback)		23ns	30ns
t_{CK4}	Clock to output (includes AND output buffer delay +1 feedback)		23ns	30ns
t_{CK5}	Clock to output (includes Ex-OR output buffer delay +1 feedback)		25ns	32ns
t_{CK6}	Clock to feedback matrix (not including buffer delay)		15ns	20ns
t_{CKH1}	Width of input clock pulse	15ns	10ns	
t_{CKL1}	Interval between clock pulses	15ns	10ns	
t_{CLR1}	Clear input to output (includes NAND output buffer delay)		23ns	30ns
t_{CLR2}	Clear input to output (includes AND output buffer delay)		23ns	30ns
t_{CLR3}	Clear input to output (includes Ex-OR output buffer delay)		25ns	32ns
t_{CLRQ}	Clear input to register output		15ns	20ns
t_{CLH}		20ns	15ns	
t_{PPR}			0ns	10ns
Operations from P-term clocks (abbreviated as P-CK)				
t_{IS4}	Input to P-CK setup time	8ns	6ns	
t_{IS5}	NAND feedback to P-CK setup time	5ns	3ns	
t_{HOLD3}	Input hold time for P-CK	13ns	8ns	
t_{HOLD4}	NAND feedback hold time for P-CK	18ns	11ns	
t_{CK7}	P-CK to output (includes NAND output buffer delay)		25ns	35ns
t_{CK8}	P-CK to output (includes AND output buffer delay)		25ns	35ns
t_{CK9}	P-CK to output (includes Ex-OR output buffer delay)		27ns	38ns
t_{CK10}	P-CK to output (includes NAND output buffer delay +1 feedback)		32ns	42ns
t_{CK11}	P-CK to output (includes AND output buffer delay +1 feedback)		32ns	42ns
t_{CK12}	P-CK to output (includes Ex-OR output buffer delay +1 feedback)		34ns	44ns
t_{CK13}	P-CK to feedback matrix (not including output buffer delay)		18ns	25ns
t_{CKH2}	Width of P-CK pulse	20ns	15ns	
t_{CKL2}	Interval between P-CK pulses	20ns	15ns	

MACRO CELL A.C. SPECIFICATIONS

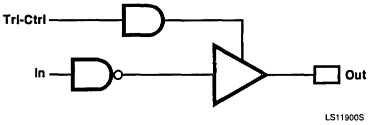
Input Buffer



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{HL} t_{LH}	X X	I I			TBD	ns
t_{HL} t_{LH}	Y Y	I I			TBD	ns

Input Pins: 1, 2, 4 – 8, 10, 11, 13, 14, 17, 18, 53, 56 – 59, 61, 62, 64 – 66, 68
Bidirectional Pins: 19, 22 – 25, 27, 28, 30

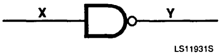
NAND Output Buffer with 3-State Control



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Out Out	In In			TBD	ns ns
t_{OE} t_{OD}	Out Out	Tri-Ctrl Tri-Ctrl			TBD	ns ns

Bidirectional and Output Pins: 19, 22 – 25, 27, 28, 30

Internal Foldback NAND

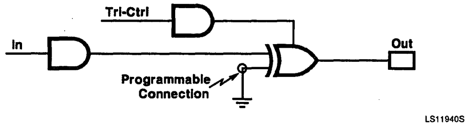


SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL}	Y	X			TBD	ns
t_{PLH}	Y	X			TBD	ns

Programmable Macro Logic PLHS502

MACRO CELL A.C. SPECIFICATIONS (Continued)

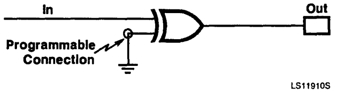
3-State Output with Programmable Polarity



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Out Out	In In			TBD	ns
t_{OE} t_{OD}	Out Out	Tri-Ctrl Tri-Ctrl			TBD	ns

Output Pins: 47, 48, 51, 52

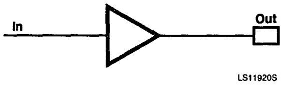
Output with Programmable Polarity



SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Out Out	In In			TBD	ns

Output Pins: 41, 42, 44, 45

Output Buffer



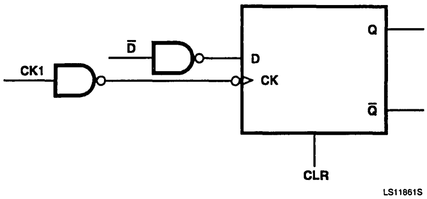
SYMBOL	PARAMETER		LIMITS			UNIT
	To (Output)	From (Input)	Min	Typ	Max	
t_{PHL} t_{PLH}	Out Out	In In			TBD	ns

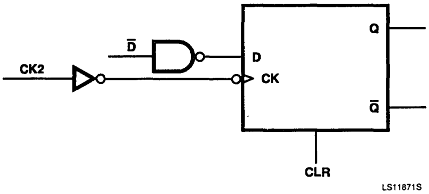
Output Pins: 31, 32, 34 – 36, 38 – 40

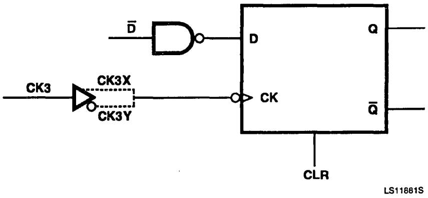
D FLIP-FLOP

INPUTS			OUTPUTS	
CLR	CK	$\overline{D}$	Q	$\overline{Q}$
H	X	X	H	L
L	L	Q_0	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H

NOTE:
Q_0, $\overline{Q}_0$ represent previous stable condition of Q, $\overline{Q}$







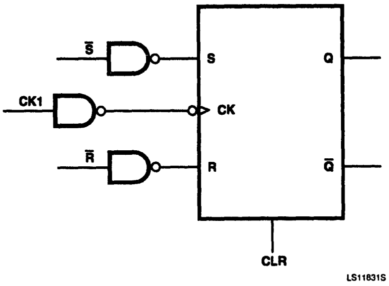
SYMBOL	LIMITS			UNIT
	Min	Typ	Max	
f_{CK1}			TBD	MHz
f_{CK2}			TBD	MHz
f_{CK3X}			TBD	MHz
f_{CK3Y}			TBD	MHz
$t_{W\ CK1}$ High			TBD	ns
$t_{W\ CK1}$ Low			TBD	ns
$t_{W\ CK2}$ High			TBD	ns
$t_{W\ CK2}$ Low			TBD	ns
$t_{W\ CK3X}$ High			TBD	ns
$t_{W\ CK3Y}$ Low			TBD	ns
t_{SETUP} D			TBD	ns
t_{HOLD} D			TBD	ns
$t_{W\ CLR}$ High			TBD	ns

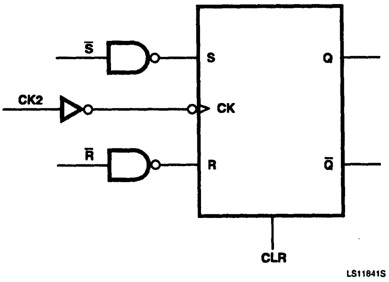
SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS			UNIT
			Min	Typ	Max	
t_{PLH}	CK1	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK1	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CK2	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK2	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CK3X	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK3X	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CK3Y	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK3Y	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CLR	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CLR	Q, $\overline{Q}$			TBD	ns

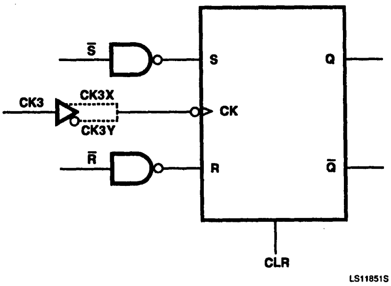
S-R FLIP-FLOP

INPUTS				OUTPUTS	
CLR	CK	$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
H	X	X	X	H	L
L	L	X	X	Q_0	$\overline{Q}_0$
L	↑	H	L	L	H
L	↑	L	H	H	L
L	↑	L	L	Q_0	$\overline{Q}_0$
L	↑	H	H	Not allowed	

NOTE:
Q_0, $\overline{Q}_0$ represent previous stable condition of Q, $\overline{Q}$

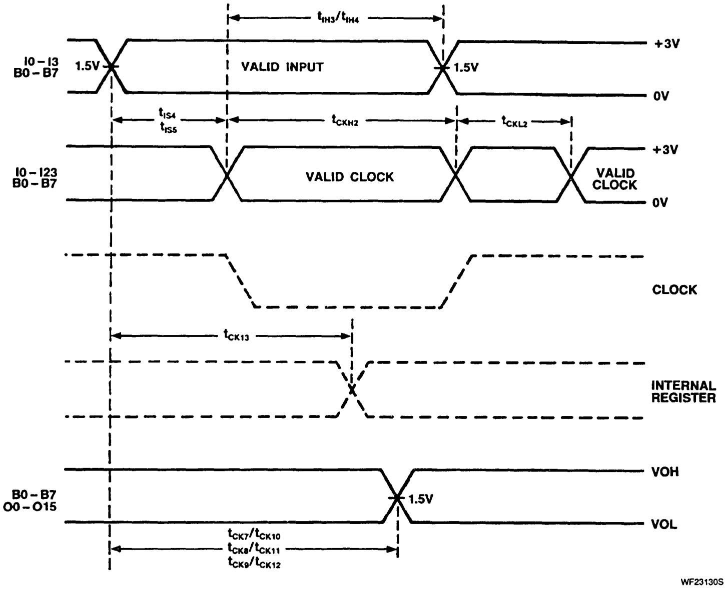




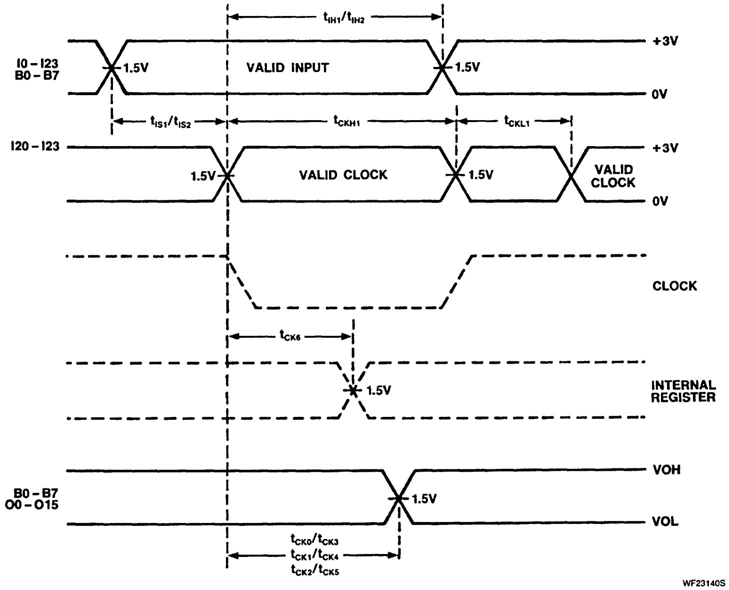


SYMBOL	LIMITS			UNIT
	Min	Typ	Max	
f_{CK1}			TBD	MHz
f_{CK2}			TBD	MHz
f_{CK3X}			TBD	MHz
f_{CK3Y}			TBD	MHz
$t_{W\ CK1}$ High			TBD	ns
$t_{W\ CK1}$ Low			TBD	ns
$t_{W\ CK2}$ High			TBD	ns
$t_{W\ CK2}$ Low			TBD	ns
$t_{W\ CK3X}$ High			TBD	ns
$t_{W\ CK3X}$ Low			TBD	ns
$t_{W\ CK3Y}$ High			TBD	ns
$t_{W\ CK3Y}$ Low			TBD	ns
t_{SETUP} S, R			TBD	ns
t_{HOLD} S, R			TBD	ns
$t_{W\ CLR}$ High			TBD	ns

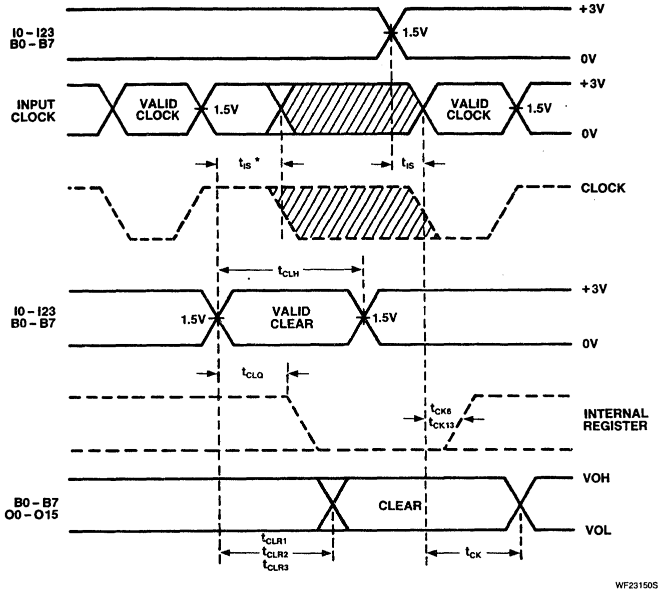
SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS			UNIT
			Min	Typ	Max	
t_{PLH}	CK1	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK1	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CK2	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK2	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CK3X	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK3X	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CK3Y	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CK3Y	Q, $\overline{Q}$			TBD	ns
t_{PLH}	CLR	Q, $\overline{Q}$			TBD	ns
t_{PHL}	CLR	Q, $\overline{Q}$			TBD	ns



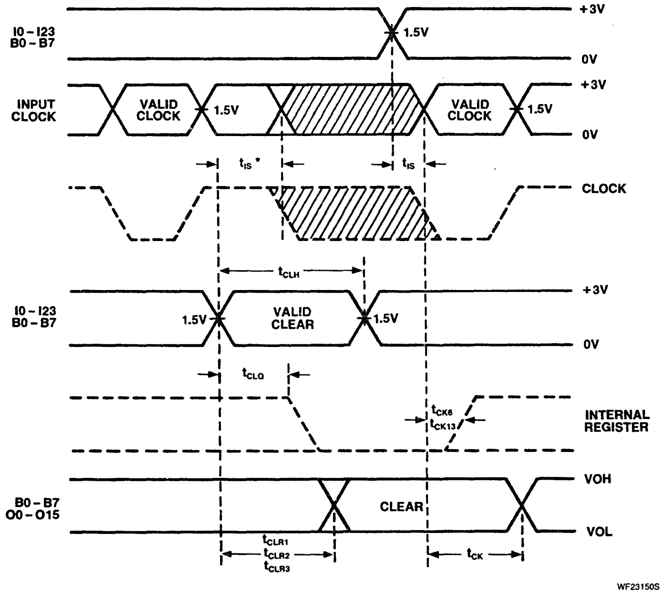
Register Output — P-Term Clock Inputs



Register Outputs — Dedicated Clock Inputs



Asynchronous Clear



Asynchronous Clear

Signetics

Application Specific Products

Section 7
Military Errata

Effective October 1986, this section has been superseded by the Military Products Data Manual. Information regarding this manual can be obtained from the Military Division in Sacramento, (916) 925-6700.
Electrical specifications herein do not necessarily describe the performance characterization of military processed products.

Signetics

Section 8 Development Software

Application Specific Products

INDEX

AMAZE – Automatic Map and Zap Equations Design Software 8-3

8

AMAZE
Programmable Logic Development Software

Application Specific Products

SOFTWARE SUPPORT FOR USER PROGRAMMABLE LOGIC

Computer Aided Design (CAD) support is becoming necessary to address the time-consuming details required by the more complex programmable logic devices available today. The design effort can include the manipulation of Boolean equations, truth tables, state diagrams, flowcharts etc, to create the binary fuse map required to program such devices.

For many years, design engineers have used programmable read-only memories (PROMs) to replace conventional logic. The architecture of the PROM can be described as a programmable logic device containing a **fixed** AND array followed by a **programmable** OR array. The fixed structure of the PROM requires a full assignment of output words to be programmed for every input combination. Therefore, little use can be made of programmable logic software programs for logic minimization or other compiling efforts when using PROMs.

Signetics Programmable Logic Devices are the most advanced approach to solving the inherent limitations of PROMs. Their architecture consists of a **programmable** AND array, followed by a **programmable** OR array - with the addition of a **programmable** invert function for flexible output control.

A Signetics PLD device can implement **any** set of Boolean expressions, provided that they are first put into the standard sum of products form. The logical ANDs are implemented at the first gate level of the programmable logic device and the logical ORs are implemented by the second gate level within the PLD. The only limitations on the expressions are those imposed by the number of inputs, outputs, and internal product terms provided by the particular PLD circuit selected. The efficiency of implementing the set of equations can be increased significantly by applying DeMorgan's theorem, and utilizing the programmable invert function on each output.

If there seems to be too few product terms to handle a relatively large equation set, one of several minimization methods can be pursued.

The probability of reducing such equations to manageable size is enhanced through the flexibility of shared AND terms for each output function, the accessibility of all AND terms to each output, and having a programmable invert function on each output. All of these features can be utilized by applying the manual manipulation of Venn Diagrams or Karnaugh Maps. However, the time and effort to accomplish these tasks as well as document the effort for procurement specification purposes increase the need and desire to have software programs to automatically perform such manipulations.

Many types of software programs are being developed to provide this assistance for operation on a wide range of computer hardware. This list of software is expanding rapidly, consisting of both Signetics generated software and some independent software houses' contributions.

This discussion is intended to outline the Signetics developed software program called AMAZE (**A**utomatic **M**ap **A**nd **Z**ap **E**quation **E**ntry) The AMAZE software program currently consists of five modules, BLAST ('**B**oolean **L**ogic **A**nd **S**tate **T**ransfer' entry program), PTP ('**PAL To** **P**LD' conversion program), DPI ('**D**evice **P**rogrammer **I**nterface' program), PLD SIM ('**PLD Sim**ulator'' program) and the PTE ('**P**rogram **T**able **E**ditor' program). Other modules will be added when product developments require additional software tools.

It must be noted that the AMAZE program is not by any means the total extent of software available for use in designing with PLD (Programmable Logic Devices). Several other commercially available PLD Design Software packages support Signetics' PLD product line. Please contact your local Signetics representative for the latest word on the most currently available software.

Programmable Logic Development Software AMAZE

AMAZE Version 1.65

Description

The AMAZE software program, **A**utomatic **M**ap **A**nd **Z**ap **E**quation **E**ntry software, consists of the following five modules:

- **BLAST** ('**B**oolean **L**ogic **A**nd **S**tate **T**ransfer' entry program)
- **PTE** ('**P**rogram **T**able **E**ditor')
- **PTP** ('**P**AL **T**o **P**LD' conversion program)
- **DPI** ('**D**evice **P**rogrammer **I**nterface' program)
- **PLD SIM** ('**PLD** **S**imulator' program)

Each module performs specific tasks as outlined in the following section.

Features

- **Multiple modules allowing expansion for future requirements**
- **Each module designed to be user friendly**
- **Both HELP and ERROR messages**
- **Document printout: Header, Pin diagram, Boolean equation and Fuse map**
- **Interface with most commercial programmers**
- **SIMULATOR programs provide applications assistance and Automatic Test Vector Generation**

Equipment Requirements (for Version 1.65)

- **Platform 1: IBM-PC, XT, AT, PS-2 and compatibles**
  - **Memory: Minimum of 640K bytes**
  - **Operating system: PC-DOS version 2.0 or higher**
  - **Disk Drive: One hard disk drive and one double sided floppy disk drive**
- **Platform 2: DEC VAX/VMS**
  - **Version 4.0 or higher**

Please contact your Signetics Sales Representative for availability and ordering information.

Products Supported

AMAZE Version 1.65 supports the following products:

20-Pin PLDs
PLS151 PLS153 PLS153A PLHS153 PLUS153B PLUS153D PLC153 PLS155 PLS157 PLS159 PLS159A PLC16V8 Series PLHS18P8A PLHS18P8B
24-Pin PLDs
PLS161 PLS162 PLS163 PLS167 PLS167A PLS168 PLS168A PLS173 PLUS173B PLUS173D PLS179 PLHS473 PLC473 PLC20V8 Series
28-Pin PLDs
PLS100 PLS101 PLS103 PLS105 PLS105A PLUS405
52-pin PLDs
PLHS501[1]

NOTE:

[1] The PLHS501 and other Programmable Macro Logic devices will also be supported on a separate PML Development System (scheduled to be available in 1989).

BLAST

Boolean Logic And State Transfer program is a menu driven software package that supports the engineer in implementing logic designs into Signetics Programmable Logic Devices. It checks design data and automatically compiles a program table from Boolean and State Machine equations. Data from the program table is then used to produce a Standard File which contains the fusing codes in a form acceptable to all the AMAZE modules (i.e. PLD-SIM and DPI).

BLAST reports the logic and syntax errors, and lists the equations in a Sum of Products form, which can help the user to minimize the entered logic equations. It will automatically partition State machine designs into specified devices, and then delete redundant terms during compilation.

BLAST also provides the capability of modifying a current logic set programmed into a device by overlaying new data onto unused fuses.

BOOLEAN LOGIC AND STATE TRANSFER FEATURES

- **User friendly interactive pinlist editor**
- **Boolean equation or state vector entry**
- **Schematic entry (with external schematic capture package)****
- **On-line error checking, minimization, and design overlay**
- **Capable of partitioning single designs into multiple PLDs**
- **Generates standard PLD fusemap files**
- **Supports all Signetics' PLDs and PLEs**
- **User definable device files for support of PALs and other PLD devices**

PTE

Program Table Entry is an interactive editor which allows the logic designer to enter data into AMAZE in the form of SIGNETICS APPROVED PROGRAM TABLES. Each Signetics PLD data sheet has the program table format which applies to that device. In addition, PTE can be used to document completed designs and to make changes in logic functions which have been previously defined in the BLAST module.

PROGRAM TABLE EDITOR FEATURES

- **Allows easy creation and editing of new and existing PLD designs**
- **Truth-table representation of PLD fusemap in High/Low format**
- **On-line editor provides automatic cursor control and prevents syntax errors**
- **On-line help screen and print facility**
- **Operates on standard PLD fusemap files**

PTP

PAL To PLD is a conversion program to allow easy transfer of the various PAL 20 and 24 pin circuits to the Signetics PLD 20 and 24 pin series devices.

PTP can automatically upload the PAL pattern from a Commercial programmer, convert the pattern into a PLD pattern, and then download the PLD pattern into the programmer. The PAL pattern and it's corresponding PLD pattern are documented, and the PLD pattern can be directed to other AMAZE modules.

PTP can also convert the PAL fuse file in a HEXPLOT format.

PAL-TO-PLD CONVERSION FEATURES

- **Menu-driven fusemap conversion of 20- and 24-pin PAL devices to pin and functional equivalent Signetics' PLDs and PAL-type devices**
- **Automatic assembler removes duplicated p-terms providing efficient PLD mapping (PLD conversions only)**
- **Accepts JEDEC, fuseplot files or direct PAL master input via commercial PLD programmer**
- **User selectable RS-232 programmable interface parameters**
- **Provides fusemap conversion documentation**
- **Generates standard PLD fusemap files compatible with other AMAZE modules**

The PTP module supports the conversion of the following device types:

PLS153 PLHS18P8 PLC16V8	10H8, 10L8, 12H6, 12L6, 14H4, 14L4, 16H2, 16L2, 16C1, 16H8, 16L8, 16P8
PLC16V8	18P8, 16RP8
PLS155 PLC16V8	16R4
PLS157 PLC16V8	16R6
PLS159 PLC16V8	16R8
PLS173 PLC20V8	14L8, 16L6, 18L4, 20C1, 20L2, 20L8
PLS173	12L10, 20L10
PLS179 PLC20V8	20R8
PLC20V8	20R4, 20R6

Signetics also provides a stand-alone version of the PTP module, SimPal, which supports the conversion of PAL device fuse maps into equivalent Signetics PAL-type PLDs.

SimPal operates on an IBM-PC/AT/XT/PS-2 or compatible platform (PC-DOS Version 2.0 or higher). SimPal supports the conversion of the following PAL JEDEC fuse maps:

PLC16V8 PLHS18P8	10H8, 10L8, 12H6, 12L6, 14H4, 14L4, 16H2, 16L2, 16C1, 16H8, 16L8, 16P8
PLC16V8	16R4, 16R6, 16R8, 16RP8, 18P8
PLC20V8	14L8, 16L6, 18L4, 20C1, 20L2, 20L8, 20R8, 20R4, 20R6

DPI

Device Programmer Interface is the software module that provides the interface between the Standard File created by the AMAZE modules and a commercial programmer. This module allows both download (sending from host to programmer) and upload (sending from programmer into the host) operations.

DPI supports both JEDEC and Signetics High/Low formats to convey fusing information to and from several commercial programmers.

(** AMAZE accepts TTL schematics generated with DATA-I/O FUTURENET DASH and OrCAD's OrCAD STD design software packages).

DEVICE PROGRAMMER INTERFACE FEATURES

- **Supports standard JEDEC and Signetics High/Low fusemap file formats**
- **RS-232 interface to commercial PLD programmers**
- **Screen menus for easy upload and download of fusemaps**
- **User selectable RS-232 parameters for programmer flexibility**
- **Test vectors automatically transferred to programmer along with fusemap file**
- **Operates with standard PLD fusemap files**

PLD SIMULATOR

The **PLD Simulator** program is a software package that simulates the operation of the logic that has been defined for Signetics PLD products. The input to the program is the Standard File generated by other AMAZE modules. The simulator has the capability of running manually or automatically. In the automatic mode the simulator creates a file of test vectors that can be used to test the programmed devices. In the manual mode the program will allow the operator to assign an input vector and observe the resultant output.

PLD FUNCTIONAL SIMULATOR FEATURES

- **Functional simulation of designs created from equations, program tables, or existing programmed devices**
- **Automatic test vector generation from standard or JEDEC PLD fusemap files**
- **Interactive keyboard entry or batch file input of test vectors**
- **Detects illegal State Machine transitions and flags affected p-terms**
- **On-line help screen**

Signetics

Section 9
Application Notes

Application Specific Products

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Signetics

AN7
Single Chip Multiprocessor Arbiter

Application Note

Application Specific Products

INTRODUCTION

In multiprocessor environments there is considerable savings to be made through sharing system resources. If each processor must support its own bus structure, I/O devices, and bulk storage medium, system cost could be very high. In the configuration shown in Figure 1, all processors share a common communication bus, and a number of system resources.

Since every processor must use the common system bus to communicate with its peripherals, a priority structure that resolves simultaneous processor bus requests into a single bus grant must be integrated into the system. In addition to making request-grant transactions, transient bus contention due to grant switching must be removed by inserting precise guard band times between bus grants.

Signetics' Field Programmable Logic Sequencer provides a convenient and cost-effective means for implementing a synchronous arbiter to perform these tasks within a single chip.

ARBITER STRUCTURE

Within a multiprocessor system, two general classes of processors can be recognized: Priority A and Priority b. Priority A processors have the highest request priority and must only compete with other Priority A processors for bus control. The arbiter must issue "A" grants in manner that prevents any high priority "A" processor from locking out another Priority A processor. To enable this, the Priority A rules implemented here use a Last Granted Lowest Priority (LGLP) ring structure. After an "A" processor has completed a bus-related task, its next arbitrated request priority will be lowest in the "A" request group. The previously second highest priority "A" processor will then become highest priority requester. The net effect of the "round robin" exchange is that every Priority A processor will have a turn at being highest priority processor. Priority A processors are typically ones that perform real-time operations or vital system tasks.

Priority b processors are lower in priority than the "A's" and may only be granted system control when no "A" requests are pending. "b" processors usually perform background tasks. Within the Priority b group, further priority ordering exists such that each "b" processor has a fixed priority position.

Plumber[1], Pearce[2], and Hojberg[3] present asynchronous techniques of arbiter implementation. These methods all have hard-wired priority rules and imprecise guard band times during grant switching. As pointed out by Hojberg, a synchronous state machine can be configured as a Mealy-type controller to provide not only precise guard band times and programmable priority rules, but also programmable input/output polarity. The state machine in Figure 2 is made from a control PROM array and an edge-triggered latch. The "A" and "b" requests and the machine's present state are used by the control PROM to determine the next "A" and "b" grants and the next state.

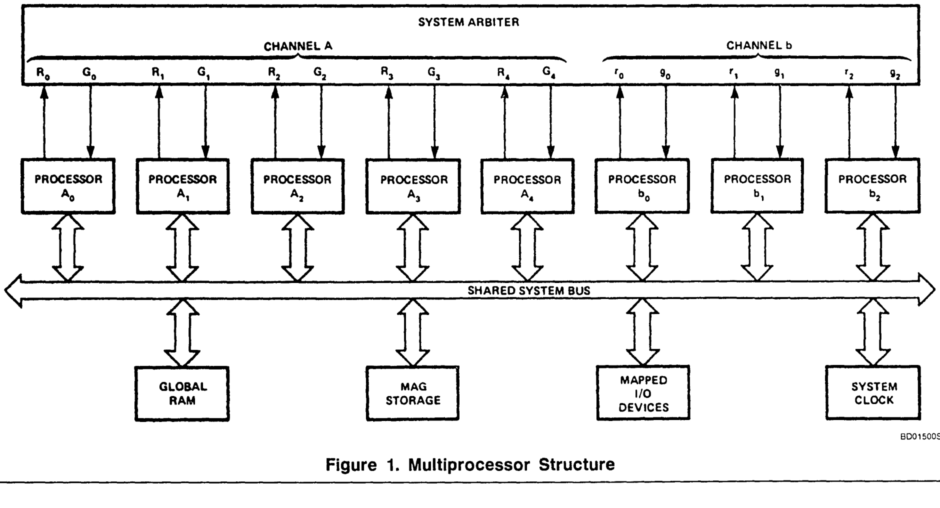
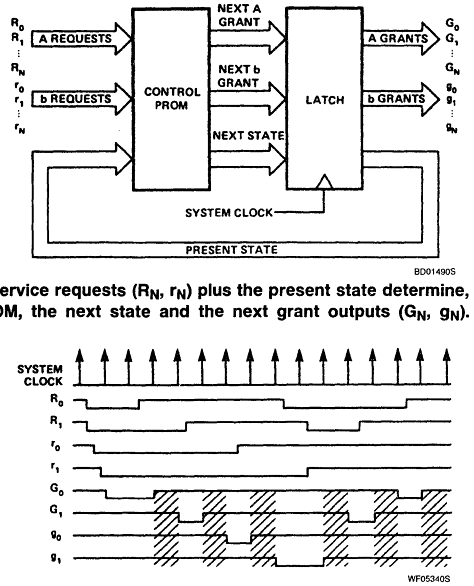


Figure 1. Multiprocessor Structure

Single Chip Multiprocessor Arbiter AN7



a. A and b service requests (R_N, r_N) plus the present state determine, through the control PROM, the next state and the next grant outputs (G_N, g_N).

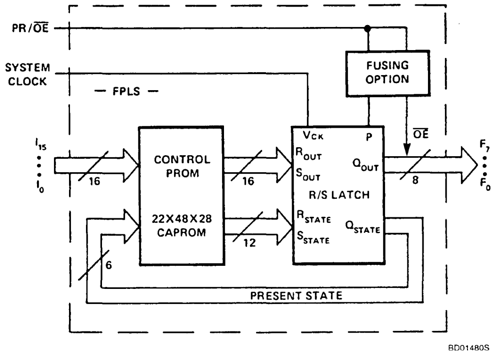
b. Requests R_0, R_1, r_0, and r_1 are asserted low in the same clock sample period. The priority rules that determine the order in which the grants are issued and the shaded guard-band areas are programmed into the control PROM. Note that the A and b request lines and the present state input to the PROM must have a set-up time equal or greater than the latch set-up time plus the PROM access time.

Figure 2. Arbiter Constructed from a Mealy-Type State Machine

SYSTEM OPERATION

Two machine states can be identified by inspection: a wait state and a grant state. The state machine enters a grant state as a response to a system request on either R_N or r_N. The machine will remain in this state with a single grant line asserted as long as the request remains asserted. Upon releasing the request line, the machine will pass through a single wait state before considering other pending requests. This provides a single state guard band time. The requests received must meet the set-up requirement of the edge-triggered latch after propagating through the control PROM. If these time considerations do not fit within a given multiprocessor structure, an input latch may be added such that the R_N and r_N lines are clocked through the latch by the system clock, thereby removing asynchronous set-up time considerations. On the basis of a state machine approach, two techniques of implementation are feasible: 1) using an architecturally advanced single IC controller, the FPLS, and, 2) a traditional PROM/LATCH configuration.

Single Chip Multiprocessor Arbiter AN7



a. FPLS Single Chip System

																								OPTION(P/Ē)													
		TRANSITION TERM																						OUTPUT TERM													
		INPUT VARIABLE (Im)																PRESENT STATE (Ps)						NEXT STATE (Ns)						OUTPUT FUNCTION (Fn)							
NO.	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																																					
1																																					
2																																					
3																																					
4																																					
5																																					
46																																					
47																																					

TB00800S

b. FPLS Standard Program Table

CK	S	R	Q
↑	0	0	Q
↑	0	1	0
↑	1	0	1
↑	1	1	Undefined

NOTE:
(↑) denotes positive clock transition. S = R = 1 is an illegal input condition.

c. Transition Table of Clocked S/R Flip-Flop

Figure 3

FPLS ARBITER IMPLEMENTATION

A five Priority "A" and three Priority "b" arbiter will be constructed such that all grant outputs will be asserted low for grants and all request inputs will be asserted low for system requests.

Brief FPLS Description

The FPLS block diagram shown in Figure 3(a) consists of a control PLA and 14 clocked S/R flip-flops. The control PLA is actually an AND-OR logic array that functions as a Content Addressable PROM. The PLA is organized as 48 words of 28 bits with 16 external input lines, and six internal inputs fed back from the State Register. The 28 PLA outputs drive the S/R inputs of the six-bit State Register and eight-bit Output Register. Note that the state feedback path is made inside the FPLS.

I_N and present state inputs, P_S, represent 2^{22} possible input codes; 48 of these codes may be mapped in the PLA to provide a 14 bit register control word. As shown in Figure 3(b) each input code may be specified by assigning to the variables either Low "L", High "H", or Don't Care "-" logic states. If any input code falls logically outside the programmed codes, the PLA asserts a Low on all its 28 internal outputs, thereby issuing a "no change" command to the R/S flip-flops.

This is an important architectural feature because it requires that only state or output transition terms be programmed. Looping terms that change neither state nor output need not be programmed in the FPLS, owing to the functional characteristics of S/R flip-flops tabulated in Figure 3(c). An example of this is shown in Figure 4.

The S/R inputs of both state and output registers are specified by using PLA outputs ("AND" functions of request inputs and present state) in the program table of Figure 3(c).

The corresponding next state of each bit will be set to 0 for "L", 1 for "H", and No Change for "-". The FPLS's PR/OE line may be assigned either Asynchronous Preset or Output Enable functions, via a user programmable option.

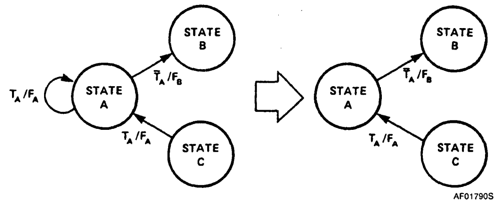
The entire function is integrated into a single 28-pin package designated as PLS105.

State Algorithm

Figure 5(a) displays the circular state form and all possible state transitions of the LGLP priority structure. Hex states 3F, 3E, 3D, 3C, and 3B are arbiter wait states W_{0-4}. In these states, processor "A" and "b" requests are monitored. Figure 5(b) illustrates a typical grant to processor A_1 in hex state 07. As long as A_1 asserts its request line low, the next state will be 07_{16} and the next output will remain with G_1 asserted low and all the other grant outputs asserted high. Since no change in state or grant output results from this transition, no PLA resources are required.

As soon as processor A_1 returns its request line, R_1, to 1, a state transition is made to 3D, and an output transition is made to set all grant outputs to 1. Since processor A_1 was the last to be granted system resources, it will now have the lowest A level request priority (LGLP). In wait state W_2, the highest priority processor will be A_2, second A_3, third A_4, and fourth A_0. To maintain the LGLP rule, grant transitions must follow the state rule $G_N \rightarrow W_{(N+1)}$, and wait states, W_M, must set their "A" priorities so that processor A_M is highest priority. Priority decreases as one proceeds clockwise around the state ring to the lowest priority processor, $A_{(m-1)}$.

When no "A" requests are pending, "b" requests may be granted. To avoid upsetting the LGLP priority rule, a "b" grant must leave and return to the same wait state. Since the "b" priority structure is the same regardless of the wait state, only a single set of "b" transition terms are required.



NOTE:
T_N/F_N = Inputs/outputs.
The FPLS requires that only two out of the three transition terms be programmed.

Figure 4. FPLS State and Output Transitions

For example, a grant transition to g_2 (Hex 20 - 25) can be issued only if there are no "A", "b_0", or "b_1" requests pending. Given the binary wait state code 111XXX, where "X's" represent Don't Cares, a request code of 01111111 will transfer the arbiter to the grant state g_2 from any of the wait states, W_{0-4}.

It is important to realize that in making this transition, the lower three-state bits will not be changed — they provide the wait state return address. When r_2 returns high, 1XXXXXXX, a transition back to the previously exited wait state is made by forcing a "1" in the three most significant state bits and leaving the lower three-state bits unchanged.

All output and state bits are initially preset to "1" through the use of the optional preset function. Grant output lines are only forced low when transitions are made to grant states and are returned to "1" when jumping back to a wait state.

Table 1 provides the complete arbiter program. The complete arbiter circuit diagram is shown in Figure 6. The AMAZE equations are shown in Figure 7.

PROM/LATCH IMPLEMENTATION

The same five "A" processor and three "b" processor arbiter can be implemented with discrete PROM's and Latches using the same state diagrams for the FPLS, except that now looping transition terms must be programmed. Coding of all state and output transitions requires programming of two memory fields: the "A" request PROM's (2KX6) and the "b" request PROM (64 × 3). The complete circuit diagram is shown in Figure 6(b).

The "A" request PROM's determine the next machine state (N_{0-5}) at all times, except when there are no "A" requests pending and there is a "b" request, or if the machine is presently in a "b" grant state. In these cases, the "b" request PROM controls the machine's next state.

The grant control lines are decoded from the next state lines and latched in two quad output latches. This PROM/LATCH organization is conceptually the same as that shown in Figure 2.

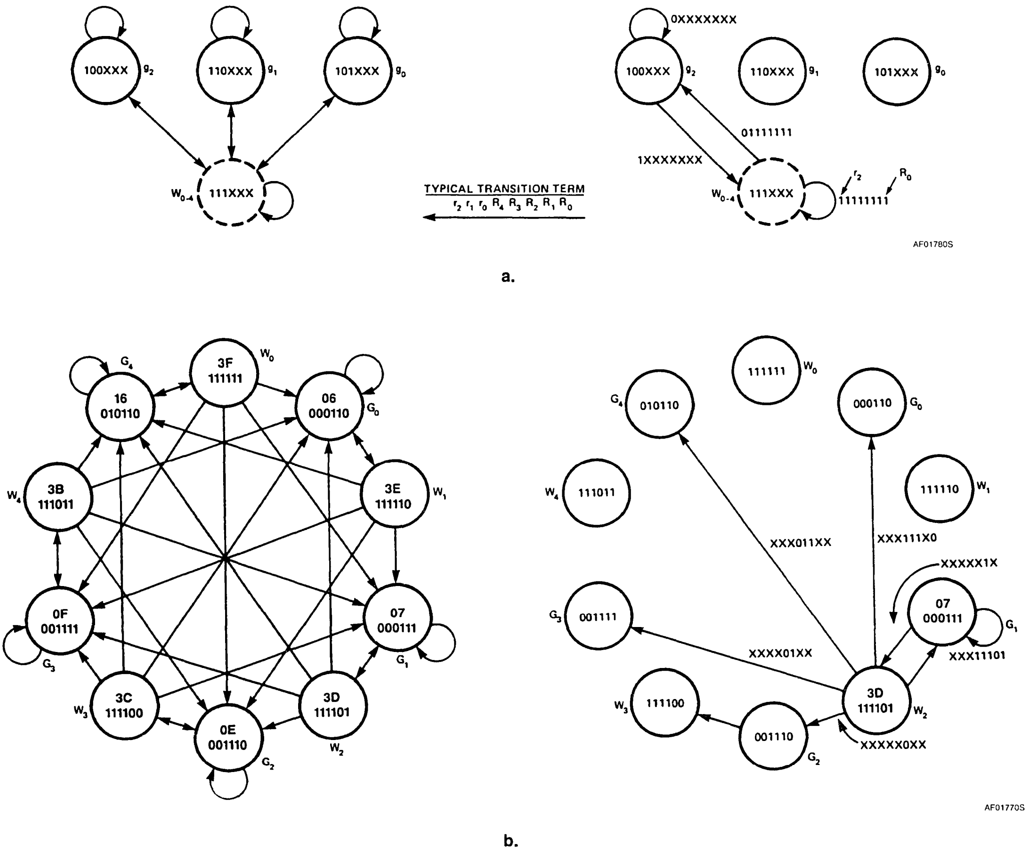
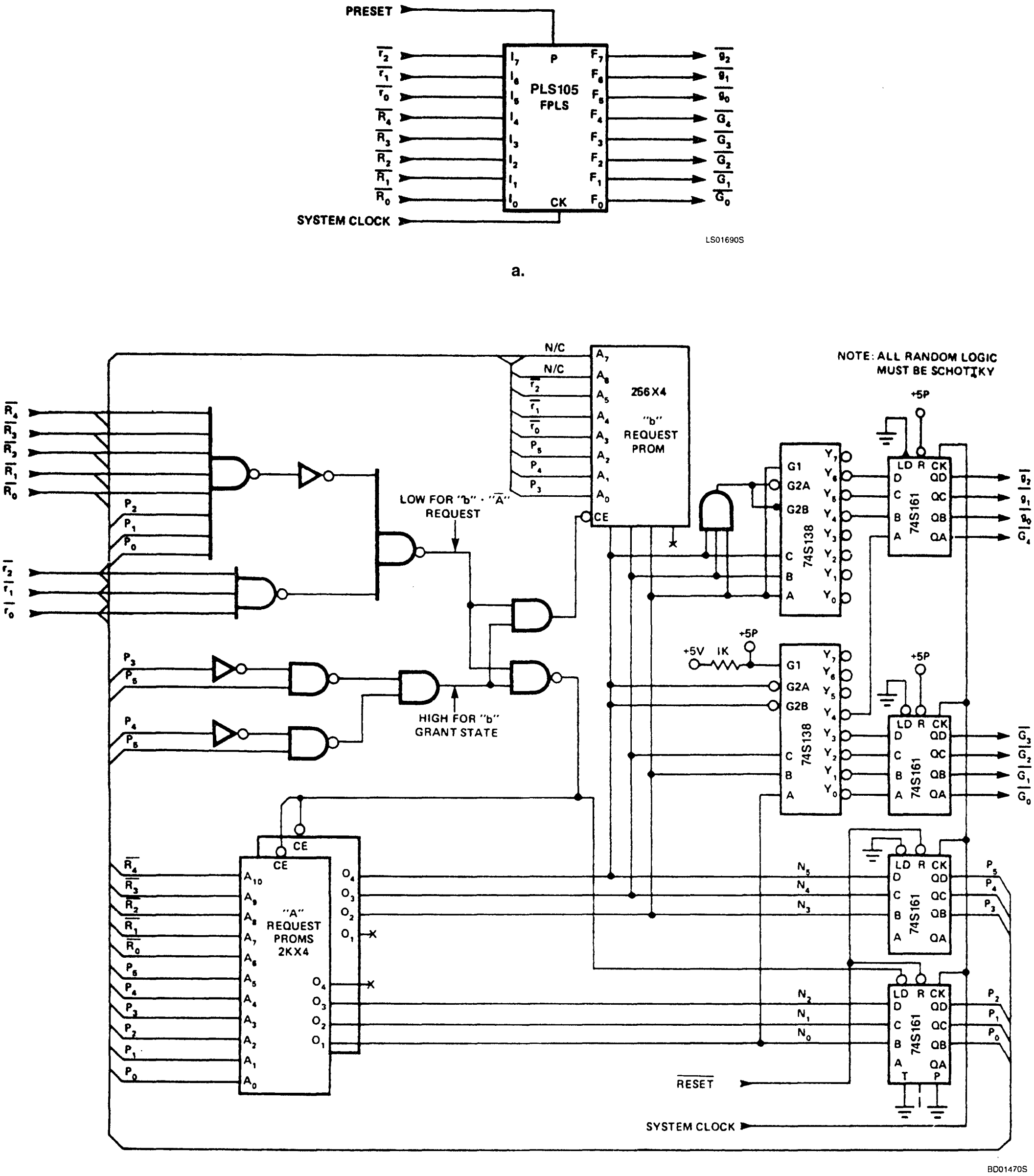


Figure 5. Arbiter State Transition Diagram



a.

b.

Figure 6. Arbiter Circuit Diagram Summary

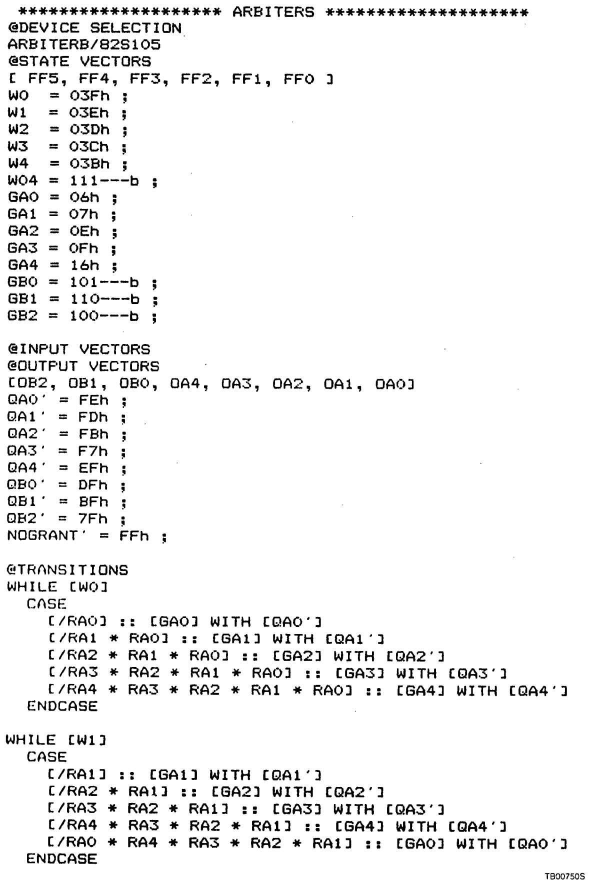
Single Chip Multiprocessor Arbiter

Table 1. FPLS Program Table for Priority Arbiter

No.	TRANSITION TERM																						OUTPUT TERM														
	INPUT VARIABLE (Im)																PRESENT STATE (Ps)						NEXT STATE (Ns)						OUTPUT FUNCTION (Fn)								
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	L	W_0
1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L	H	
2	—	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	H	H	L	L	H	H	H	L	H	H	H	H	H	L	H	H	
3	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	L	H	H	H	
4	—	—	—	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H	H	L	H	H	H	H	
5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	—	H	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	W_1
6	—	—	—	—	—	—	—	—	—	—	—	—	—	L	H	—	H	H	H	H	H	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	
7	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H	—	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	
8	—	—	—	—	—	—	—	—	—	—	—	L	H	H	H	—	H	H	H	H	H	L	L	H	L	H	H	L	H	H	H	L	H	H	H	H	
9	—	—	—	—	—	—	—	—	—	—	—	H	H	H	H	L	H	H	H	H	H	L	L	L	L	H	H	L	H	H	H	H	H	H	H	L	
10	—	—	—	—	—	—	—	—	—	—	—	—	—	L	—	—	H	H	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	L	H	H	W_2
11	—	—	—	—	—	—	—	—	—	—	—	—	L	H	—	—	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	L	H	H	H	
12	—	—	—	—	—	—	—	—	—	—	—	L	H	H	—	—	H	H	H	H	L	H	L	H	L	H	H	L	H	H	H	L	H	H	H	H	
13	—	—	—	—	—	—	—	—	—	—	—	H	H	H	—	L	H	H	H	H	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H.	L	
14	—	—	—	—	—	—	—	—	—	—	—	H	H	H	L	H	H	H	H	H	L	H	L	L	L	H	H	H	H	H	H	H	H	H	L	H	
15	—	—	—	—	—	—	—	—	—	—	—	—	L	—	—	—	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	W_3
16	—	—	—	—	—	—	—	—	—	—	—	L	H	—	—	—	H	H	H	H	L	L	L	H	L	H	H	L	H	H	H	L	H	H	H	H	
17	—	—	—	—	—	—	—	—	—	—	—	H	H	—	—	L	H	H	H	H	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	L	
18	—	—	—	—	—	—	—	—	—	—	—	H	H	—	L	H	H	H	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	
19	—	—	—	—	—	—	—	—	—	—	—	H	H	L	H	H	H	H	H	H	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	
20	—	—	—	—	—	—	—	—	—	—	—	L	—	—	—	—	H	H	H	L	H	H	L	H	L	H	H	L	H	H	H	L	H	H	H	H	W_4
21	—	—	—	—	—	—	—	—	—	—	—	H	—	—	—	L	H	H	H	L	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	L	
22	—	—	—	—	—	—	—	—	—	—	—	H	—	—	L	H	H	H	H	L	H	H	L	L	L	H	H	L	H	H	H	H	H	H	L	H	
23	—	—	—	—	—	—	—	—	—	—	—	H	—	L	H	H	H	H	H	L	H	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	
24	—	—	—	—	—	—	—	—	—	—	—	H	L	H	H	H	H	H	H	L	H	H	L	L	H	H	H	H	H	H	H	H	L	H	H	H	
25	—	—	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	H	H	—	—	—	H	L	H	—	—	—	H	H	L	H	H	H	H	H	W_{0-4}
26	—	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	H	H	H	—	—	—	H	H	L	—	—	—	H	L	H	H	H	H	H	H	
27	—	—	—	—	—	—	—	—	L	H	H	H	H	H	H	H	H	H	H	—	—	—	H	L	L	—	—	—	L	H	H	H	H	H	H	H	
28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	G_0
29	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	G_1
30	—	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	L	L	H	H	H	L	H	H	H	H	L	L	H	H	H	H	H	H	H	H	G_2
31	—	—	—	—	—	—	—	—	—	—	—	—	H	—	—	—	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	G_3
32	—	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	G_4
33	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	H	L	H	—	—	—	H	H	H	—	—	—	H	H	H	H	H	H	H	H	g_0
34	—	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	H	H	L	—	—	—	H	H	H	—	—	—	H	H	H	H	H	H	H	H	g_1
35	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—	H	L	L	—	—	—	H	H	H	—	—	—	H	H	H	H	H	H	H	H	g_2
36																																					
									$\overline{r_2}$	$\overline{r_1}$	$\overline{r_0}$	$\overline{R_4}$	$\overline{R_3}$	$\overline{R_2}$	$\overline{R_1}$	$\overline{R_0}$													$\overline{g_2}$	$\overline{g_1}$	$\overline{g_0}$	$\overline{G_4}$	$\overline{G_3}$	$\overline{G_2}$	$\overline{G_1}$	$\overline{G_0}$	

TB00790S

Single Chip Multiprocessor Arbiter AN7



```
 ******************** ARBITERS ********************
@DEVICE SELECTION
ARBITERB/82S105
@STATE VECTORS
[ FF5, FF4, FF3, FF2, FF1, FF0 ]
W0  = 03Fh ;
W1  = 03Eh ;
W2  = 03Dh ;
W3  = 03Ch ;
W4  = 03Bh ;
W04 = 111---b ;
GA0 = 06h ;
GA1 = 07h ;
GA2 = 0Eh ;
GA3 = 0Fh ;
GA4 = 16h ;
GB0 = 101---b ;
GB1 = 110---b ;
GB2 = 100---b ;

@INPUT VECTORS
@OUTPUT VECTORS
[OB2, OB1, OB0, OA4, OA3, OA2, OA1, OA0]
QA0' = FEh ;
QA1' = FDh ;
QA2' = FBh ;
QA3' = F7h ;
QA4' = EFh ;
QB0' = DFh ;
QB1' = BFh ;
QB2' = 7Fh ;
NOGRANT' = FFh ;

@TRANSITIONS
WHILE [W0]
  CASE
    [/RA0] :: [GA0] WITH [QA0']
    [/RA1 * RA0] :: [GA1] WITH [QA1']
    [/RA2 * RA1 * RA0] :: [GA2] WITH [QA2']
    [/RA3 * RA2 * RA1 * RA0] :: [GA3] WITH [QA3']
    [/RA4 * RA3 * RA2 * RA1 * RA0] :: [GA4] WITH [QA4']
  ENDCASE

WHILE [W1]
  CASE
    [/RA1] :: [GA1] WITH [QA1']
    [/RA2 * RA1] :: [GA2] WITH [QA2']
    [/RA3 * RA2 * RA1] :: [GA3] WITH [QA3']
    [/RA4 * RA3 * RA2 * RA1] :: [GA4] WITH [QA4']
    [/RA0 * RA4 * RA3 * RA2 * RA1] :: [GA0] WITH [QA0']
  ENDCASE
```

TB00750S

a. Arbiter State Equations

Figure 7

```
WHILE [W2]
  CASE
    [/RA2] :: [GA2] WITH [QA2']
    [/RA3 * RA2] :: [GA3] WITH [QA3']
    [/RA4 * RA3 * RA2] :: [GA4] WITH [QA4']
    [/RA0 * RA4 * RA3 * RA2] :: [GA0] WITH [QA0']
    [/RA1 * RA0 * RA4 * RA3 * RA2] :: [GA1] WITH [QA1']
  ENDCASE

WHILE [W3]
  CASE
    [/RA3] :: [GA3] WITH [QA3']
    [/RA4 * RA3] :: [GA4] WITH [QA4']
    [/RA0 * RA4 * RA3] :: [GA0] WITH [QA0']
    [/RA1 * RA0 * RA4 * RA3] :: [GA1] WITH [QA1']
    [/RA2 * RA1 * RA0 * RA4 * RA3] :: [GA2] WITH [QA2']
  ENDCASE

WHILE [W4]
  CASE
    [/RA4] :: [GA4] WITH [QA4']
    [/RA0 * RA4] :: [GA0] WITH [QA0']
    [/RA1 * RA0 * RA4] :: [GA1] WITH [QA1']
    [/RA2 * RA1 * RA0 * RA4] :: [GA2] WITH [QA2']
    [/RA3 * RA2 * RA1 *RA1 * RA4] :: [GA3] WITH [QA3']
  ENDCASE

WHILE [W04]
  CASE
    [/RB0 * RA4 * RA3 * RA2 * RA1 * RA0] :: [GB0] WITH [QB0']
    [/RB1 * RB0 * RA4 * RA3 * RA2 * RA1 * RA0] :: [GB1] WITH [QB1']
    [/RB2 * RB1 * RB0 * RA4 * RA3 * RA2 * RA1 * RA0] :: [GB2] WITH [QB2']
  ENDCASE

WHILE [GA0]
  IF [RA0] THEN [W1] WITH [NOGRANT']

WHILE [GA1]
  IF [RA1] THEN [W2] WITH [NOGRANT']

WHILE [GA2]
  IF [RA2] THEN [W3] WITH [NOGRANT']

WHILE [GA3]
  IF [RA3] THEN [W4] WITH [NOGRANT']

WHILE [GA4]
  IF [RA4] THEN [W0] WITH [NOGRANT']

WHILE [GB0]
  IF [RB0] THEN [GB1] WITH [NOGRANT']

WHILE [GB1]
  IF [RB1] THEN [GB2] WITH [NOGRANT']

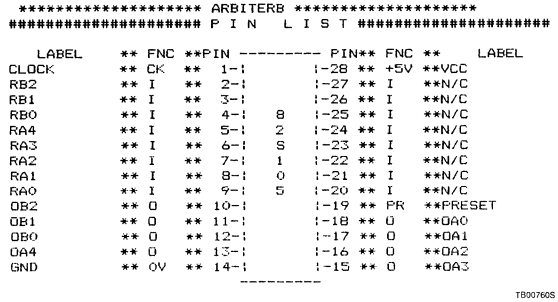
WHILE [GB2]
  IF [RB2] THEN [GB0] WITH [NOGRANT']
```

TB00751S

a. Arbiter State Equations (Continued)

Figure 7 (Continued)

9



```
 ******************** ARBITERB ********************
###################### P I N   L I S T ######################

   LABEL      ** FNC **PIN --------- PIN** FNC **     LABEL
CLOCK         ** CK  **   1-|       |-28 ** +5V **VCC
RB2           ** I   **   2-|       |-27 ** I   **N/C
RB1           ** I   **   3-|       |-26 ** I   **N/C
RB0           ** I   **   4-|   8   |-25 ** I   **N/C
RA4           ** I   **   5-|   2   |-24 ** I   **N/C
RA3           ** I   **   6-|   S   |-23 ** I   **N/C
RA2           ** I   **   7-|   1   |-22 ** I   **N/C
RA1           ** I   **   8-|   0   |-21 ** I   **N/C
RA0           ** I   **   9-|   5   |-20 ** I   **N/C
OB2           ** O   **  10-|       |-19 ** PR  **PRESET
OB1           ** O   **  11-|       |-18 ** O   **OA0
OB0           ** O   **  12-|       |-17 ** O   **OA1
OA4           ** O   **  13-|       |-16 ** O   **OA2
GND           ** OV  **  14-|       |-15 ** O   **OA3
                             ---------
```

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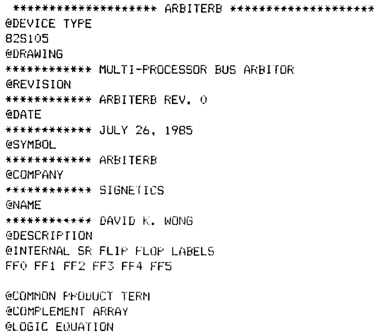
b. Arbiter Pin List



```
 ******************** ARBITERB ********************
@DEVICE TYPE
82S105
@DRAWING
************ MULTI-PROCESSOR BUS ARBITOR
@REVISION
************ ARBITERB REV. 0
@DATE
************ JULY 26, 1985
@SYMBOL
************ ARBITERB
@COMPANY
************ SIGNETICS
@NAME
************ DAVID K. WONG
@DESCRIPTION
@INTERNAL SR FLIP FLOP LABELS
FF0 FF1 FF2 FF3 FF4 FF5

@COMMON PRODUCT TERM
@COMPLEMENT ARRAY
@LOGIC EQUATION
```

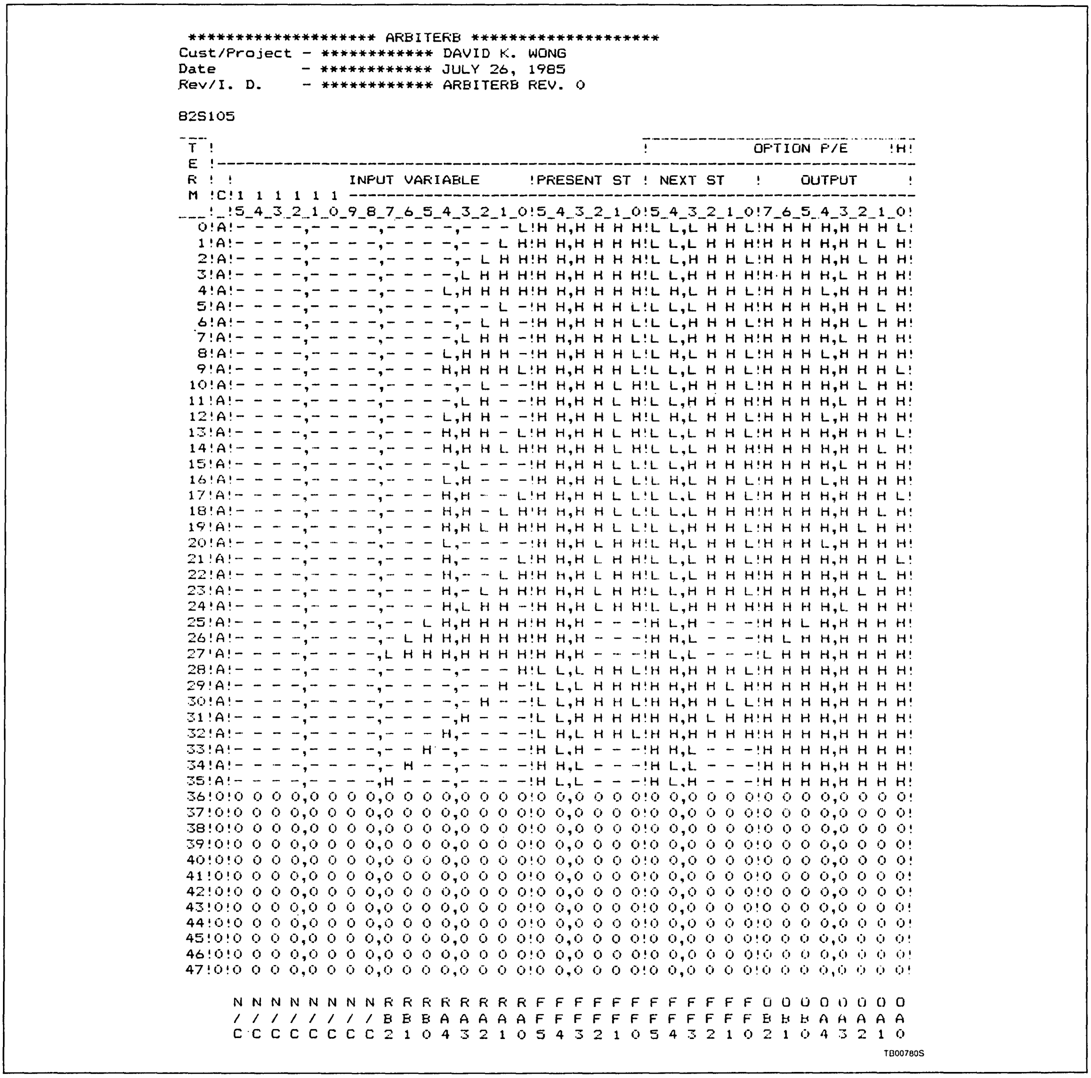
TB00770S

c. Arbiter Boolean Equations

Figure 7 (Continued)

Single Chip Multiprocessor Arbiter

Table 2. Arbiter Program Table



```
 ********************* ARBITERB *********************
Cust/Project - ************ DAVID K. WONG
Date         - ************ JULY 26, 1985
Rev/I. D.    - ************ ARBITERB REV. 0

82S105

---                                              ----------------------------
 T !                                             !           OPTION P/E   !H!
 E !--------------------------------------------------------------------------
 R ! !            INPUT VARIABLE      !PRESENT ST ! NEXT ST   !    OUTPUT     !
 M !C!1 1 1 1 1 1 ------------------------------------------------------------
___!_!5_4_3_2_1_0_9_8_7_6_5_4_3_2_1_0!5_4_3_2_1_0!5_4_3_2_1_0!7_6_5_4_3_2_1_0!
  0!A!- - - -,- - - -,- - - -,- - - L!H H,H H H H!L L,L H H L!H H H H,H H H L!
  1!A!- - - -,- - - -,- - - -,- - L H!H H,H H H H!L L,L H H H!H H H H,H H L H!
  2!A!- - - -,- - - -,- - - -,- L H H!H H,H H H H!L L,H H H L!H H H H,H L H H!
  3!A!- - - -,- - - -,- - - -,L H H H!H H,H H H H!L L,H H H H!H H H H,L H H H!
  4!A!- - - -,- - - -,- - - L,H H H H!H H,H H H H!L H,L H H L!H H H L,H H H H!
  5!A!- - - -,- - - -,- - - -,- - L -!H H,H H H L!L L,L H H H!H H H H,H H L H!
  6!A!- - - -,- - - -,- - - -,- L H -!H H,H H H L!L L,H H H L!H H H H,H L H H!
  7!A!- - - -,- - - -,- - - -,L H H -!H H,H H H L!L L,H H H H!H H H H,L H H H!
  8!A!- - - -,- - - -,- - - L,H H H -!H H,H H H L!L H,L H H L!H H H L,H H H H!
  9!A!- - - -,- - - -,- - - H,H H H L!H H,H H H L!L L,L H H L!H H H H,H H H L!
 10!A!- - - -,- - - -,- - - -,- L - -!H H,H H L H!L L,H H H L!H H H H,H L H H!
 11!A!- - - -,- - - -,- - - -,L H - -!H H,H H L H!L L,H H H H!H H H H,L H H H!
 12!A!- - - -,- - - -,- - - L,H H - -!H H,H H L H!L H,L H H L!H H H L,H H H H!
 13!A!- - - -,- - - -,- - - H,H H - L!H H,H H L H!L L,L H H L!H H H H,H H H L!
 14!A!- - - -,- - - -,- - - H,H H L H!H H,H H L H!L L,L H H H!H H H H,H H L H!
 15!A!- - - -,- - - -,- - - -,L - - -!H H,H H L L!L L,H H H H!H H H H,L H H H!
 16!A!- - - -,- - - -,- - - L,H - - -!H H,H H L L!L H,L H H L!H H H L,H H H H!
 17!A!- - - -,- - - -,- - - H,H - - L!H H,H H L L!L L,L H H L!H H H H,H H H L!
 18!A!- - - -,- - - -,- - - H,H - L H!H H,H H L L!L L,L H H H!H H H H,H H L H!
 19!A!- - - -,- - - -,- - - H,H L H H!H H,H H L L!L L,H H H L!H H H H,H L H H!
 20!A!- - - -,- - - -,- - - L,- - - -!H H,H L H H!L H,L H H L!H H H L,H H H H!
 21!A!- - - -,- - - -,- - - H,- - - L!H H,H L H H!L L,L H H L!H H H H,H H H L!
 22!A!- - - -,- - - -,- - - H,- - L H!H H,H L H H!L L,L H H H!H H H H,H H L H!
 23!A!- - - -,- - - -,- - - H,- L H H!H H,H L H H!L L,H H H L!H H H H,H L H H!
 24!A!- - - -,- - - -,- - - H,L H H -!H H,H L H H!L L,H H H H!H H H H,L H H H!
 25!A!- - - -,- - - -,- - L H,H H H H!H H,H - - -!H L,H - - -!H H L H,H H H H!
 26!A!- - - -,- - - -,- L H H,H H H H!H H,H - - -!H H,L - - -!H L H H,H H H H!
 27!A!- - - -,- - - -,L H H H,H H H H!H H,H - - -!H L,L - - -!L H H H,H H H H!
 28!A!- - - -,- - - -,- - - -,- - - H!L L,L H H L!H H,H H H L!H H H H,H H H H!
 29!A!- - - -,- - - -,- - - -,- - H -!L L,L H H H!H H,H H L H!H H H H,H H H H!
 30!A!- - - -,- - - -,- - - -,- H - -!L L,H H H L!H H,H H L L!H H H H,H H H H!
 31!A!- - - -,- - - -,- - - -,H - - -!L L,H H H H!H H,H L H H!H H H H,H H H H!
 32!A!- - - -,- - - -,- - - H,- - - -!L H,L H H L!H H,H H H H!H H H H,H H H H!
 33!A!- - - -,- - - -,- - H -,- - - -!H L,H - - -!H H,L - - -!H H H H,H H H H!
 34!A!- - - -,- - - -,- H - -,- - - -!H H,L - - -!H L,L - - -!H H H H,H H H H!
 35!A!- - - -,- - - -,H - - -,- - - -!H L,L - - -!H L,H - - -!H H H H,H H H H!
 36!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 37!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 38!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 39!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 40!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 41!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 42!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 43!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 44!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 45!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 46!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!
 47!0!0 0 0 0,0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0 0 0,0 0 0 0!

      N N N N N N N N R R R R R R R R F F F F F F F F F F F F 0 0 0 0 0 0 0 0
      / / / / / / / / B B B A A A A A F F F F F F F F F F F F B B B A A A A A
      C C C C C C C C 2 1 0 4 3 2 1 0 5 4 3 2 1 0 5 4 3 2 1 0 2 1 0 4 3 2 1 0
                                                                       TB00780S
```

Single Chip Multiprocessor Arbiter

SUMMARY

As can be seen from the circuit diagrams, the FPLS can offer significant advantages over discrete MSI arrays in the design of state machines. The tradeoff in both design alternatives for the Priority Arbiter is shown in Table 2. Clearly, the FPLS approach uses fewer parts, with savings in PC board space and power requirements.

Table 3. Design Alternatives for the Priority Arbiter

PARAMETER	F.P.L.S.	PROM/LATCH
Parts count	1 IC	≈19IC's
PCB space	.84 in^2	7.92 in^2
Power	.65W	2.85W
Voltage	+5V	+5V

REFERENCES

1. W.W. Plumber: "Asynchronous Arbiters"; *IEEE Transactions on Computers,* January 1972, pp. 37 – 42.
2. R.C. Pearce, J.A. Field, and W.D. Little: "Asynchronous Arbiter Module"; *IEEE Transactions on Computers,* September 1975, pp. 931 – 933.
3. K. Soe Hojberg: "An Asynchronous Arbiter Resolves Resource Allocation Conflicts on a Random Priority Basis"; *Computer Design,* August 1977, pp. 120 – 123.
4. K. Soe Hojberg: "One-Step Programmable Arbiter for Multiprocessors"; *Computer Design,* April 1978, pp. 154 – 158.

Signetics

Application Specific Products

AN8
Introduction To Signetics Programmable Logic

Application Note

Author: K. A. H. Noach

INTRODUCTION

Custom logic is expensive – too expensive if your production run is short. 'Random logic' is cheaper but occupies more sockets and board space. Signetics Programmable Logic bridges the gap. Using PLD, you can configure an off-the-shelf chip to perform just the logic functions you need. Design and development times are much shorter, and risk much lower than for custom logic. Connections are fewer than for random logic, and, for all but the simplest functions, propagation delay is usually shorter. Yet another advantage that PLD has over custom logic is that it allows you to redesign the functions without redesigning the chip – giving you an invaluable margin not only for cut-and-try during system development, but also for later revision of system design. You're not tied down by the need to recover capital invested in a custom chip.

A PLD chip is an array of logic elements – gates, inverters, and flip-flops, for instance. In the virgin state, everything is connected to everything else by nichrome fuses, and although the chip has the capacity to perform an extensive variety of logic functions, it doesn't have the ability to. What gives it that is programming: selectively blowing undesired fuses so that those that remain provide the interconnections necessary for the required functions.

Signetics Series 20 PLD, named for the number of pins, supplements the well-known Series 28. The package is smaller – little more than a third the size, in fact – but the improved architecture, with user-programmable shared I/O. compensates for the fewer pins. The series comprises the following members, in order of increasing complexity:

- **PLS151 – field-programmable gate array**
- **PLS153 – field-programmable logic array**
- **PLS155 – field-programmable logic sequencer**
- **PLS157 – field-programmable logic sequencer**
- **PLS159 – field-programmable logic sequencer**

Entry to all the devices is via a product matrix, an array of input and shared I/O lines fuse-connected to the multiple inputs of an array of AND gates (see Figures 1, 2 and 5). To exploit the capacity of any device, it is important to make the most economical use of tho AND gates it has available. Application of de Morgan's theorem can help in this. For example, inputs for the function

$$F = A + B + C + D$$

would occupy four of the AND gates of the product matrix. However, the same function rewritten as

$$\overline{F} = \overline{A}\ \overline{B}\ \overline{C}\ \overline{D}$$

would occupy only one. Moreover, the second function could be done on the simplest of the Series 20 devices (*and* leave eleven gates over for other functions), whereas the first could not. The fact that all inputs of the Series 20 devices, including the shared ones, incorporate double buffers that make the true and complement forms of all input variables equally accessible, greatly facilitates the use of de Morgan's theorem for logic minimization.

To convert the minimized logic equations to the pattern of fuses to be blown, you can use either a programming sheet (see e.g. Table 1) or Boolean equation program-entry software that lets you enter the equations via the keyboard of a terminal. The direct programmability of logic equations makes system design with PLD simple and sure. Functional changes can be made by replacing one PLD chip by another differently programmed. In many cases you can even remove the original one, reprogram it on the spot, and re-insert it. Programming machines qualified for the Series 20 are at present available from DATA I/O, KONTRON, and STAG.

FPGA PLS151

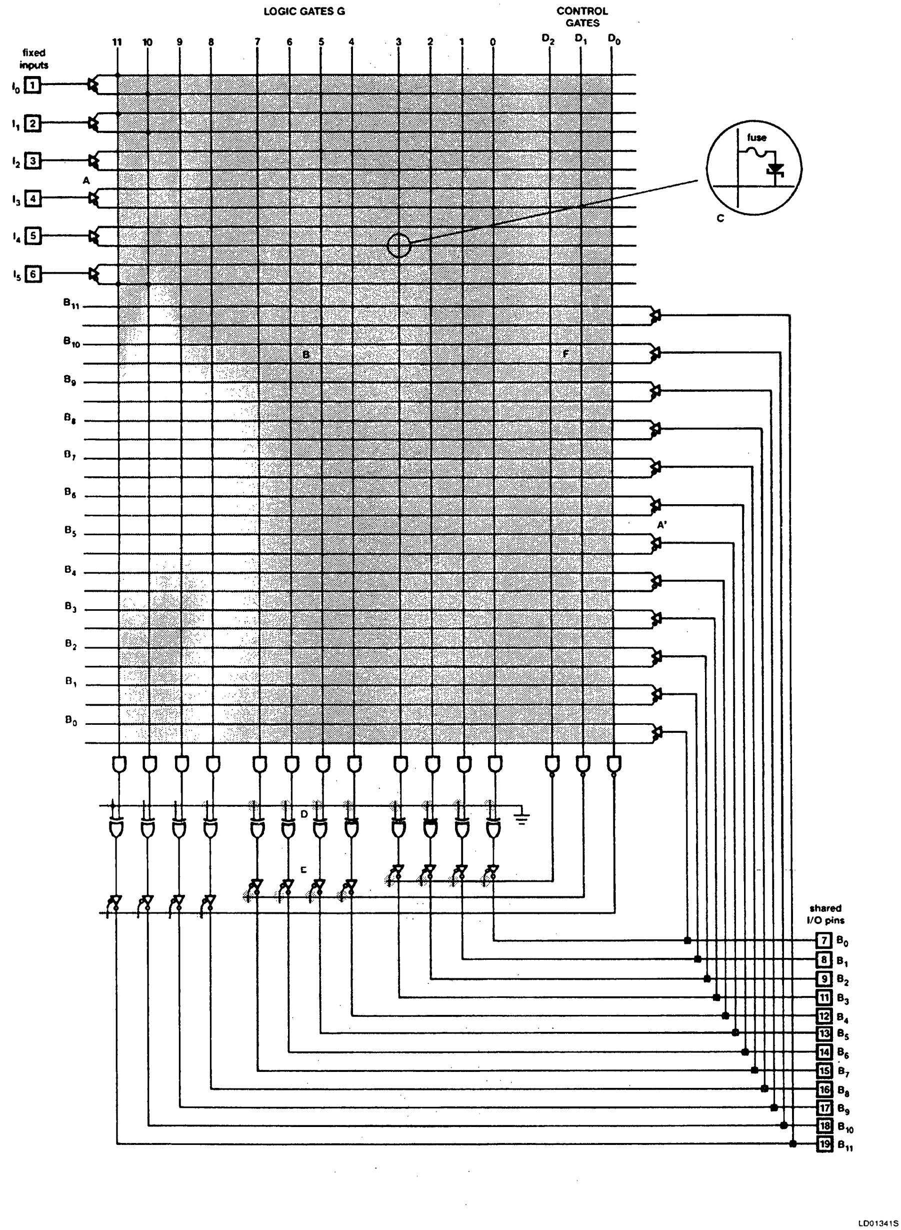
The field-programmable gate array is the simplest of the Series 20 PLD devices; Figure 1 shows the functional diagram. The array can accept up to 18 inputs. There are six dedicated input pins (A) and twelve (A') that can be programmed as inputs, outputs, or bidirectional I/O. All input variables, whether on dedicated or programmed input pins, are available in both true and complement form in the product matrix (B), and both forms are buffered: either form can drive all 12 product lines if required. In the virgin state, all the input variables and their complements are connected to all the product lines via a diode and a fuse (C), and the product matrix is effectively inoperative. To enable it to generate the required functions, unrequired connections between individual input lines and product lines are severed by blowing the connecting fuses.

At the output of the product matrix are 12 NAND gates, each with 36 inputs to accommodate the 18 possible input variables and their complements. Each of the product terms is normally active-Low, but a unique feature of Signetics PLD is that any or all of them can be independently programmed active-High. This is done by means of an array of exclusive-OR gates (D) at the NAND-gate outputs; when the fuse that grounds the second input of each OR gate is blown, the output of that gate is inverted.

The product matrix and exclusive OR-gate connections shown in Figure 1 illustrate the flexibility conferred by having buffered complements of all input variables internally available, together with independently programmable output polarities. Output B_{11}, shown with its exclusive OR-gate fuse intact, is programmed

$$\overline{B_{11}} = I_0 I_1 \overline{I_5}$$

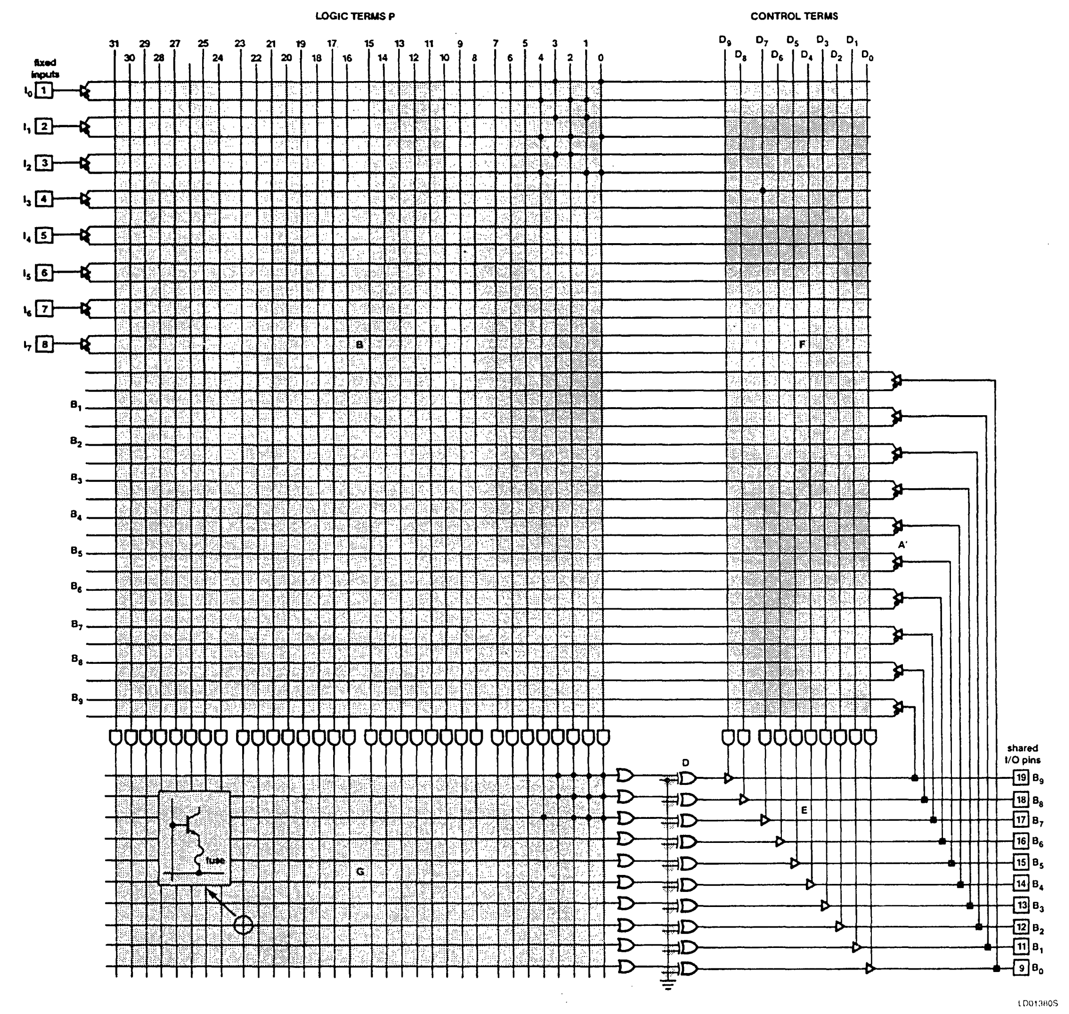
Introduction To Signetics Programmable Logic AN8



NOTE:
A, dedicated inputs; A', programmable I/O. B, product (NAND) matrix with fused connections C; each of the vertical lines in the matrix represents 36 inputs to the terminating NAND gated. D, exclusive-OR array with inputs grounded via fuses for polarity control. E, programmable Tri-state output buffers. F, fuse-programmable control matrix. Square dots (■) represent permanent connections; round dots (●) intact fuse connections. Connected as shown, the array is programmed for the functions $\overline{B}_{11} = I_0\ I_1\ \overline{I}_5$ and $B_{10} = \overline{I}_0\ \overline{I}_1\ \overline{I}_5$.

Figure 1. Field-Programmable Gate Array PLS151A

Introduction To Signetics Programmable Logic



NOTE:
A to F, as in Figure 1. G, sum (OR) matrix. Connected as shown, the array is programmed as a single-bit adder with Carry Enable.

Figure 2. Field-Programmable Logic Array PLS153

At the same time, and without using any additional inputs, output B_{10} (fuse blown) is programmed

$$B_{10} = \overline{I_0}\,\overline{I_1}\,\overline{I_5}$$

Each of the exclusive-OR gates drives a three-state output buffer. In the virgin state all the buffers (E) are disabled and therefore in the high-impedance state. The function of the programmable I/O pins (A') is then determined by the I/O control matrix (F). The three AND gates at the control-matrix output are Active-High, and when one of them is in the High state, the four output buffers it controls are enabled; the corresponding I/O pins then act as outputs. conversely, when a control-matrix AND-gate output is Low and the control fuse for the corresponding Tri-state buffer is intact, the pins controlled by that gate act as inputs. Thus, these pins can be programmed in groups of up to four to act as inputs or outputs according to the state of selected input variables. If required, any of the programmable I/O pins can be made a dedicated output by blowing the control fuse of the output buffer associated with it.

The speed of the FPGA compares favorably with TTL, although its propagation delay is longer than the individual gate delay of TTL. When the number of inputs required is large, however, the FPGA more than makes up for this. When more than eight inputs are required, for example, the FPGA has a distinct advantage. Then, the overall propagation delay of TTL often amounts to two or three gate delays, but that of the FPGA to only one.

FPLA PLS153

Architecture

With two levels of logic embodied in a product matrix terminating in 32 AND gates coupled to a ten-output OR matrix (Figure 2), the FPLA is a step up in complexity from the FPGA. Again, there is provision for 18 input variables, internally complemented and buffered, but here divided between eight dedicated input pins and ten individually programmable I/O pins. As before, exclusive-OR gates grounded by fuses provide output polarity control, and any of the programmable I/O pins can be made a dedicated output by blowing the control fuse of the output buffer associated with it.

Programming

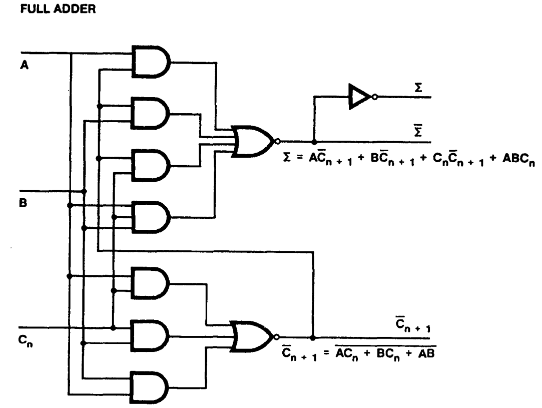
When the required functions have been defined, corresponding programming instructions are entered in a programming table, the layout of which reflects the FPLA architecture. (A Signetics computer program named AMAZE, which accepts Boolean equations as input and generates an FPLA programming table as output, is also available.) The programming machine blows the FPLA fuses in the pattern prescribed by the table.

As an illustration of FPLA programming, consider a full adder. Figure 3 shows a TTL version (74LS80) and the corresponding logic equations. Note that the feedback of $\overline{C}_{n+1}$ introduces a second propagation delay. In the FPLA this is eliminated by redefining Σ in terms of A, B, and C_n, as shown in Figure 4, and using the right side of the equation for $\overline{C}_{n+1}$ instead of the term itself. At first glance this would appear to require a minimum of three product terms for $\overline{C}_{n+1}$ plus four for Σ, or a total of seven. The Karnaugh maps, however, show considerable overlap between the two functions: the map for $\overline{C}_{n+1}$ differs from that for Σ only by having A B C_n instead of $\overline{A}$ $\overline{B}$ $\overline{C_n}$. Rewriting the equation for $\overline{C}_{n+1}$ to introduce $\overline{A}$ $\overline{B}$ $\overline{C_n}$ and eliminate A B C_n,

$$\overline{C}_{n+1} = A\,\overline{B}\,\overline{C_n} + \overline{A}\,B\,\overline{C_n} + \overline{A}\,\overline{B}\,C_n + \overline{A}\,\overline{B}\,\overline{C_n}$$

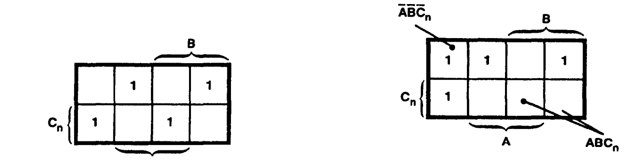
increases the number of product terms by one, but now $\overline{C}_{n+1}$ and Σ have three terms in common. Therefore, since the FPLA allows multiple use of product terms, it is sufficient to program each of the common terms only once; thus, the original seven product terms are effectively reduced to five.

To fill in the programming table (Table 1), first allocate inputs and outputs.


FULL ADDER
A
B
C_n
Σ
$\overline{\Sigma}$
$\Sigma = A\overline{C}_{n+1} + B\overline{C}_{n+1} + C_n\overline{C}_{n+1} + ABC_n$
$\overline{C}_{n+1}$
$\overline{C}_{n+1} = \overline{AC_n + BC_n + AB}$

LD01370S

Figure 3. Single-Bit Full Adder in TTL (e.g. 74LS80)



$$\Sigma = A\overline{C}_{n+1} + B\overline{C}_{n+1} + \overline{C}_n\overline{C}_{n+1} + ABC_n$$
$$= A\overline{B}\overline{C}_n + \overline{A}B\overline{C}_n + \overline{A}\overline{B}C_n + ABC_n$$

LD01320S

$$\overline{C}_{n+1} = \overline{AC_n + BC_n + AB}$$
$$= \overline{A}\overline{B} + \overline{A}\overline{C}_n + \overline{B}\overline{C}_n$$
$$= A\overline{B}\overline{C}_n + \overline{A}B\overline{C}_n + \overline{A}\overline{B}C_n + \overline{A}\overline{B}\overline{C}_n$$

LD01330S

Figure 4. Karnaugh Maps and Logic Equations for the Full Adder of Figure 3, Illustrating how the Equations are Reduced for the FPLA Implementation Shown in Figure 2 and Table 1

Inputs:	A $= I_0$	Outputs:	$\overline{C}_{n+1} = B_7$
	B $= I_1$		$\overline{\Sigma} = B_8$
	$C_n = I_2$		$\Sigma = B_9$

Next, enter the product terms of Σ in the product-matrix (AND) part of the table, using H to indicate a true input and L a false one.

- Term 0 is A $\overline{B}$ $\overline{C_n}$: mark H, L, L in columns I_0, I_1, I_2 of row 0
- Term 1 is $\overline{A}$ B $\overline{C_n}$: mark L, H, L in columns I_0, I_1, I_2 of row 1
- Term 2 is $\overline{A}$ $\overline{B}$ C_n: mark L, L, H in columns I_0, I_1, I_2 of row 2
- Term 3 is A B C_n: mark H, H, H in columns I_0, I_1, I_2 of row 3.

Fill the rest of rows 0, 1, 2, and 3 with dashes to indicate that all other inputs are to be disconnected from Terms 0, 1, 2, and 3 (fuses blown).

The product terms of Σ must be added to form the sum-of-products required at output B_9. Indicate the required addition by putting an A (for Attached, i.e. fuse unblown) in the Term 0, 1, 2, and 3 spaces of column $B(O)_9$; Term 4 is not required for Σ, so put a dot in the Term 4 space to indicate that it is to be disconnected (fuse blown). To indicate that the output is to be Active-High, put an H in the polarity square above the $B(O)_9$ column. Finally, fill row D_9 with dashes to indicate that all fuses on line D_9 of the control matrix are to be blown and B_9 is to be a dedicated output. This completes the programming of Σ.

The $\overline{\Sigma}$ output on B_8 is programmed in just the same way, except that the polarity square above the $B(O)_8$ column is marked L to indicate Active-Low. (Note that in the FPLA, the Σ and $\overline{\Sigma}$ outputs change simultaneously, because all output signals traverse the exclusive-OR array (D), whether they are Active-High or Active-Low. In the TTL full adder shown in Figure 3, the output inverter delays the change of Σ with respect to $\overline{\Sigma}$.)

Table 1. FPLA Programming Table Filled in for the Full Adder of Figure 2

PROGRAM TABLE ENTRIES:

I, B(I)	
INACTIVE	0
I, B	H
$\overline{I}, \overline{B}$	L
DON'T CARE	–

(AND)

B(O)	
ACTIVE	A
INACTIVE	•

B(O)	
HIGH	H
LOW	L

(POL.)

																			POLARITY									
																			H	L	L							
TERM	AND																		OR									
	I								B(I)										B(O)									
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0	–	–	–	–	–	L	L	H	–	–	–	–	–	–	–	–	–	–	A	A	A							
1	–	–	–	–	–	L	H	L	–	–	–	–	–	–	–	–	–	–	A	A	A							
2	–	–	–	–	–	H	L	L	–	–	–	–	–	–	–	–	–	–	A	A	A							
3	–	–	–	–	–	H	H	H	–	–	–	–	–	–	–	–	–	–	A	A	•							
4	–	–	–	–	–	L	L	L	–	–	–	–	–	–	–	–	–	–	•	•	A							
5																												
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D9	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–										
D8	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–										
D7	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–										
D6																												
D5																												
D4																												
D3																												
D2																												
D1																												
D0																												
PIN NO.	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9										
VARIABLE NAME					ENABLE	C_n	B	A	Σ	$\overline{\Sigma}$	$\overline{C_{n+1}}$																	

TB01480S

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The output C_{n+1} on B_7 contains three of the same terms as Σ, plus the term $\overline{A}\ \overline{B}\ \overline{C_n}$. Only this last term needs to be additionally programmed in the product matrix: mark L, L, L in columns I_0, I_1, I_2 of the Term 4 row. Indicate the addition

$$A\ \overline{B}\ \overline{C_n} + \overline{A}\ B\ \overline{C_n} + \overline{A}\ \overline{B}\ C_n + \overline{A}\ \overline{B}\ \overline{C_n}$$

by putting an A in rows 0, 1, 2, and 4 of column $B(O)_7$, and show that Term 3 ($A\ B\ C_n$) is not required by putting a dot in the Term 3 row to indicate disconnection (fuse blown). Put an L in the $B(O)_7$ polarity square to indicate Active-Low.

Identifying B_7 as a dedicated output by indicating that all the fuses to control term D_7 are to be blown, would now complete the programming of the full adder. However, a useful supplementary feature would be a Carry Enable function to keep the B_7 output buffer in the high-impedance state except when the enable input I_3 is true. The output buffer is enabled when both the fuses of a control term are blown, or when one is blown and the term that controls the output buffer is true. Thus, a Carry Enable can be provided via the I_3 input by leaving intact the fuse for Active-High operation of the enable signal to control term D_7. To indicate this, put an H in the I_3 column of row D_7 and fill the rest of the row with dashes.

The full adder with output Carry Enable uses only four of the eight dedicated inputs, three of the ten programmable I/O pins, and five of the 32 AND gates. The remaining capacity can be used for programming other functions which may, if required, also make use of AND-gate outputs already programmed for the full adder.

All fuses not indicated as blown in the programming table are normally left intact to preserve capacity for later program revisions or the addition of supplementary functions. If it is essential to minimize propagation delay, however, the finalized program should include instructions for blowing all unused fuses to minimize load capacitance.

FPLS PLS155 - PLS157 - PLS159 Architecture

The FPLS (Figure 5) is the most complex of the Series 20 PLD devices. Like the FPLA, it has a 32-term product matrix followed by an OR matrix. In the FPLS, however, the OR matrix is larger and comprises three distinct parts, with architecture differing in detail from type to type. In the PLS155, for instance, the first part consists of eight 32-input gates coupled, like those of the FPLA, to an output-polarity-controlling exclusive-OR array. The second consists of twelve additional gates which control four flip-flops. These are what give the FPLS its sequential character, enabling it to dictate its next state as a function of its present state. The third part is the deceptively simple Complement Array (I in Figure 5): a single OR gate with its output inverted and fed back into the product matrix. This enables a chosen sum-of-products to become a common factor of any or all the product terms and makes it possible to work factored sum-of-products equations. it is also useful for handshaking control when interfacing with a processor and for altering the sequence of a state machine without resorting to a large number of product terms.

PLS155 has four dedicated inputs and eight programmable I/O pins that can be allocated in the same way as in the FPLA. It also has four shared I/O pins (L) whereby the flip-flops can be interfaced with a bidirectional data bus. Two product terms, L_A and L_B in the control matrix F, control the loading of the flip-flops, in pairs, synchronized with the clock.

Figure 6 shows the architecture of the flip-flop circuitry in the PLS155. The flip-flops are positive-edge–triggered and can be dynamically changed to J-K, T, or D types according to the requirements of the function being performed; this considerably lessens the demands on the logic. The Tri-state inverter between the J and K inputs governs the mode of operation, under the control of the product term F:

- When the inverter is in the high-impedance state, the flip-flop is a J-K type, or a T type when J = K.
- When the inverter is active, K = $\overline{J}$ and the flip-flop is a D type; the K input must then be disconnected from the OR matrix.

All the product terms from the product matrix (T_0 to T_{31} in Figure 5) are fuse-connected to the J and K input OR gates. if both fuses of any one product term are left intact, J = K and the flip-flop is a T type.

The flip-flops of the PLS155 have asynchronous Preset and Reset controlled by terms in the OR matrix that take priority over the clock. Their three-state output buffers can be controlled from the enable pin OE or permanently enabled or disabled by blowing fuses or leaving them intact in the enable array (K in Figure 5).

The PLS157 and PLS159 sequencers have, respectively, six and eight flip-flops. The architecture differs in detail but is similar in principle to that of PLS155.

Programming

The FPLS is programmed in much the same way as the FPLA, using a table to instruct the machine that blows the undesired fuses. It is not necessary to work with a circuit diagram; in fact, it is even undesirable to do so, since applying the necessary logic reduction techniques would in most cases make the diagram difficult to read and more a hindrance than a help. An example of how to program the FPLS as a universal counter/shift-register is given in the Appendix.

DEVELOPMENT AND PRODUCTION ECONOMY WITH PLD

Underlying the design philosophy of the Signetics Series 20 PLD is the concept of programmable arrays whose architecture emulates logic equation formats rather than mere aggregations of gates. The unique combination of features which support this philosophy includes:

- double-buffered true and complement inputs
- programmable-polarity outputs
- programmable I/O for internal feedback and maximum freedom in allocating inputs and outputs
- truth-table programming format

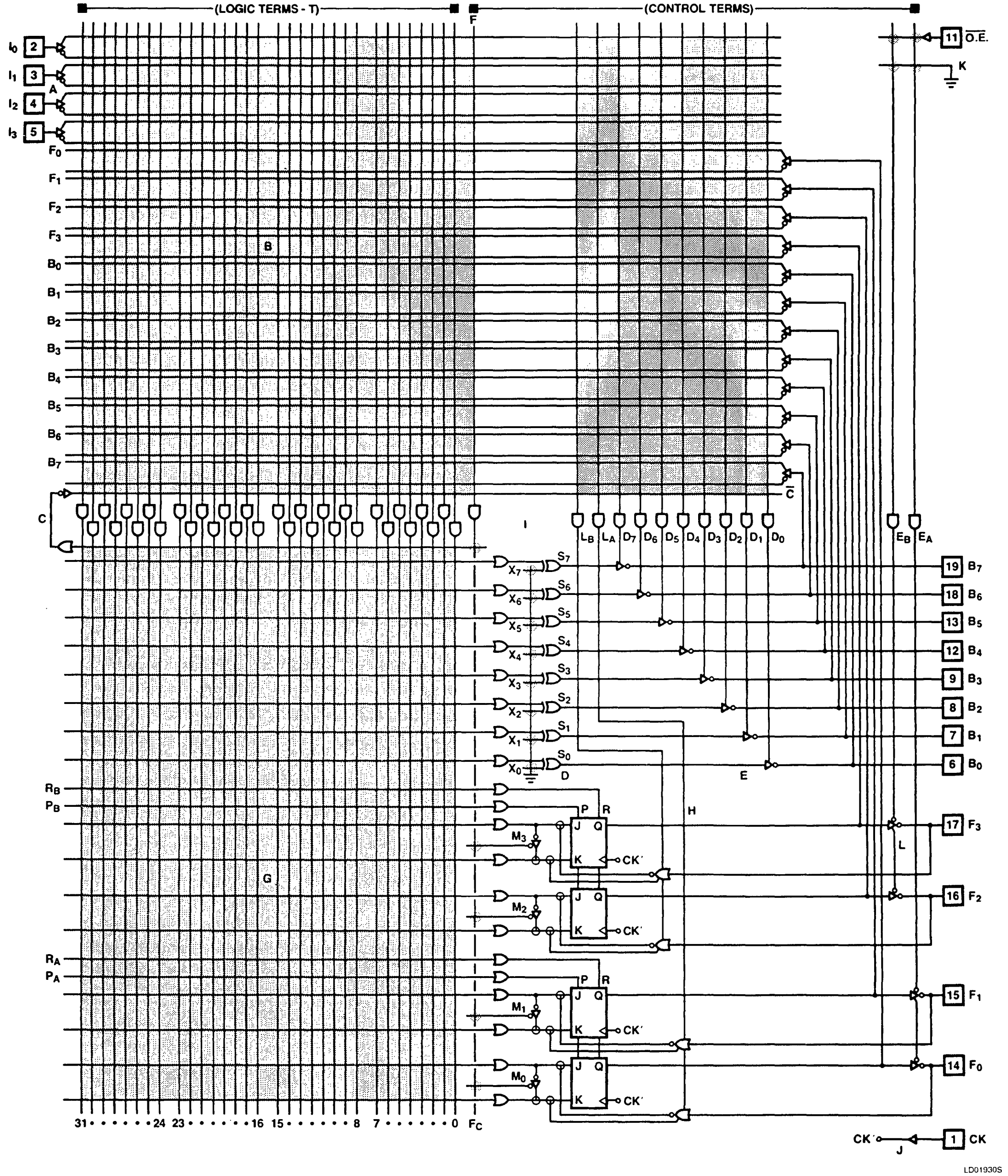
These features are common to all the PLD devices. In the field-programmable logic sequencers they are further supported by:

- flip-flops with dynamically alterable operating modes
- a complement array for simplified handshaking control

From the development engineer's point of view an important advantage of PLD is that it eliminates breadboarding. Once the functions required in terms of minimized logic equations are worked out, a PLD can be programmed accordingly. Once programmed, it will perform those functions.

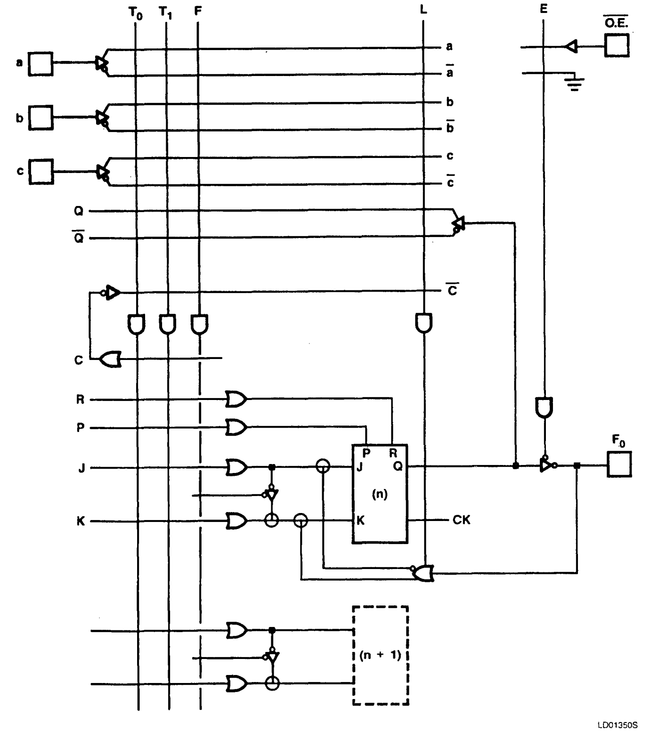
Loading the instructions into the programming machine usually takes no more than a couple of hours; after that, the machine can program the devices at a rate of 100 an hour. Moreover, since any PLD can be programmed in many different ways, PLD has considerable potential for simplifying purchasing and stock control. One type of device can be programmed to perform a diversity of tasks for which it would otherwise be necessary to purchase and stock many different devices.

Series 20 PLD is second-sourced by Harris Semiconductor.



NOTE:
A to G, As In Figure 2. H, Flip-Flops And Bus-Load Buffer. J, Clock Input. K, Output-Buffer Enable. L, Tri-state Flip-Flop Output Buffers.

Figure 5. Field-Programmable Logic Sequencer PLS155



-⊕- denotes wire-OR

● denotes fixed connection

Figure 6. Architecture of the PLS155 Flip-Flop Circuitry

APPENDIX

Programming an FPLS as a Counter/Shift-Register

Objective: to program a PLS155 FPLS as a count-up, count-down, shift-right, shift-left machine governed by three control terms - COUNT/$\overline{\text{SHIFT}}$, RIGHT/UP, LEFT/DOWN. Direct implementation would result in a machine with 64 state transitions (see Table A-1), which is beyond the scope of the PLS155 or even the 28-pin PLS105. Logic reduction is therefore necessary.

As there are only four feedback variables (D, C, B, A), you can do the reduction by hand, one mode at a time; the control terms need not be included till the summary equations are written. Using the transition mapping method suggested here, you can examine the excitation equations for all types of flip-flops (R-S, J-K, D, T) and choose those types that will perform the required functions using the fewest product terms. Table A-2 summarizes the rules for flip-flop implementation using transition maps; the transition symbols used in the table mean:

PRESENT STATE	NEXT STATE	TRANSITION SYMBOL
0	0	0
0	1	α
1	0	β
1	1	1

Using these symbols, construct Table A-3 from Table A-1 to enable you to examine the excitation equations for all types of flip-flops. Proceeding one mode at a time, transfer the state conditions from Table A-3 to Karnaugh maps, as in Figure A-1. Following the rules in Table A-2, derive the excitation equations for the different types of flip-flops (the examples shown in Figure A-1 omit the T type because it is the same as the J-K type when J = K). In deciding which types of flip-flop to use, remember that logic minimization with PLD is different from logic minimization with 'random logic': with random logic you seek to reduce the number of standard packages required; with PLD you seek to reduce the number of product terms.

From Figure A-1 it is evident that you should choose J-K or T flip-flops for the counter mode and D flip-flops for the shift mode, for you then require only one product term per flip-flop per mode. Table A-4 summarizes the number of product terms per mode the various types of flip-flops would require.

Table A-5 shows the completed programming table for the counter/shift-register. The programming of Terms 0 to 15 reflects the flip-flop excitation equations and illustrates the value of being able to switch the flip-flops dynamically from one type of operation to another. Terms 16, 17 and 18, respectively, provide for INITIALIZE, asynchronous RESET, and STOP functions.

The programming of the two additional inputs $\overline{\text{HALT}}$ and $\overline{\text{BUSY}}$ illustrates the value of the complementary, which is made active when $\overline{\text{HALT}}$ and $\overline{\text{BUSY}}$ are Low (A in the Complement square of Term 18) and propagated into all the other terms (dot in the Complement squares of Terms 0 to 17). This means that unless the $\overline{\text{HALT}}$ and $\overline{\text{BUSY}}$ inputs are High, none of the product terms will be true and the state of the machine will not change. If the Complement Array were not used, twice the number of product terms would be required, even if one of the additional inputs were omitted.

As it is, the design uses only 19 of the 32 product terms available, so there is ample capacity for extending its capabilities. For example, the shift-left function can be augmented by a binary multiplication capability, using a D type flip-flop to make it shift one, two, or three places according to the state of two extra inputs, X and Y. Table A-6 shows the revised programming table. The binary multiplication function occupies nine additional product terms.

ACKNOWLEDGEMENT

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Table A-1. Present-State/Next-State Table for Counter/Shift-Register

STATE NO.	PRESENT STATE				NEXT STATE															
					Count Down				Count Up				Shift Left				Shift Right			
	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A
0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0
2	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	1
3	0	0	1	1	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1
4	0	1	0	0	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0
5	0	1	0	1	0	1	0	0	0	1	1	0	1	0	1	0	1	0	1	0
6	0	1	1	0	0	1	0	1	0	1	1	1	1	1	0	0	0	0	1	1
7	0	1	1	1	0	1	1	0	1	0	0	0	1	1	1	0	1	0	1	1
8	1	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	0	1	0	0
9	1	0	0	1	1	0	0	0	1	0	1	0	0	0	1	1	1	1	0	0
10	1	0	1	0	1	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1
11	1	0	1	1	1	0	1	0	1	1	0	0	0	1	1	1	1	1	0	1
12	1	1	0	0	1	0	1	1	1	1	0	1	1	0	0	1	0	1	1	0
13	1	1	0	1	1	1	0	0	1	1	1	0	1	0	1	1	1	1	1	0
14	1	1	1	0	1	1	0	1	1	1	1	1	1	1	0	1	0	1	1	1
15	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1
CONTROL TERMS																				
COUNT/$\overline{\text{SHIFT}}$					1				1				0				0			
RIGHT/UP					0				1				0				1			
LEFT/DOWN					1				0				1				0			

Table A-2. Rules for Flip-Flop Implementation Using Transition Maps

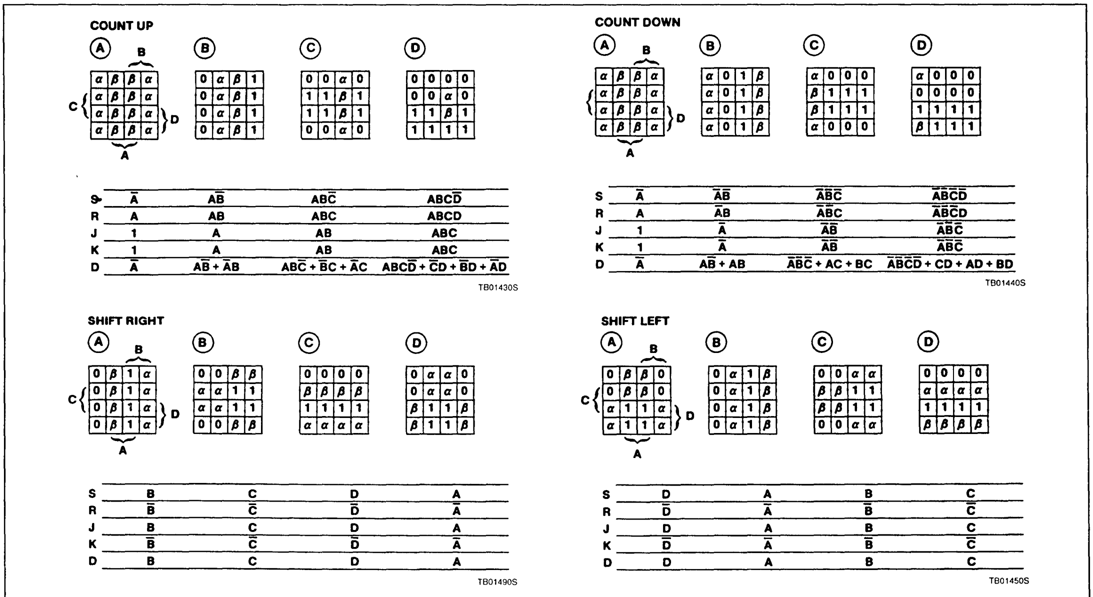
FLIP-FLOP TYPE	INPUT	MUST INCLUDE	MUST EXCLUDE	REDUNDANT
R-S	S	α	β,0	1,x
	R	β	α,1	0,x
D	D	α,1	β,0	x
T	T	α,β	0,1	x
J-K	J	α	0	1,β,x
	K	β	1	0,α,x

Table A-3. Transition Table for Counter/Shift-Register

STATE NO.	PRESENT STATE				TRANSITION															
					Count Down				Count Up				Shift Left				Shift Right			
	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A
0	0	0	0	0	α	α	α	α	0	0	0	α	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	β	0	0	α	β	0	0	α	β	α	0	0	β
2	0	0	1	0	0	0	β	α	0	0	1	α	0	α	β	0	0	0	β	α
3	0	0	1	1	0	0	1	β	0	α	β	β	0	α	1	β	α	0	β	1
4	0	1	0	0	0	β	α	α	0	1	0	α	α	β	0	0	0	β	α	0
5	0	1	0	1	0	1	0	β	0	1	α	β	α	β	α	β	α	β	α	β
6	0	1	1	0	0	1	β	α	0	1	1	α	α	1	β	0	0	β	1	α
7	0	1	1	1	0	1	1	β	α	β	β	β	α	1	1	β	α	β	1	1
8	1	0	0	0	β	α	α	α	1	0	0	α	β	0	0	α	β	α	0	0
9	1	0	0	1	1	0	0	β	1	0	α	β	β	0	α	1	1	α	0	β
10	1	0	1	0	1	0	β	α	1	0	1	α	β	α	β	α	β	α	β	α
11	1	0	1	1	1	0	1	β	1	α	β	β	β	α	1	1	1	α	β	1
12	1	1	0	0	1	β	α	α	1	1	0	α	1	β	0	α	β	1	α	0
13	1	1	0	1	1	1	0	β	1	1	α	β	1	β	α	1	1	1	α	β
14	1	1	1	0	1	1	β	α	1	1	1	α	1	1	β	α	β	1	1	α
15	1	1	1	1	1	1	1	β	β	β	β	β	1	1	1	1	1	1	1	1

Table A-4. Number of Product Terms Required for Counter/Shift-Register Flip-Flop Excitation

FLIP-FLOP TYPE	COUNT UP	COUNT DOWN	SHIFT RIGHT	SHIFT LEFT	TOTAL
SR only	8	8	8	8	32
JK only	4	4	8	8	24
D only	10	10	4	4	28
FPLS	4(J-K)	4(J-K)	4(D)	4(D)	16


COUNT UP
A
B
C
D
B
C
D
A
α β β α / α β β α / α β β α / α β β α
0 α β 1 / 0 α β 1 / 0 α β 1 / 0 α β 1
0 0 α 0 / 1 1 β 1 / 1 1 β 1 / 0 0 α 0
0 0 0 0 / 0 0 α 0 / 1 1 β 1 / 1 1 1 1
COUNT DOWN
A
B
C
D
α β β α / α β β α / α β β α / α β β α
α 0 1 β / α 0 1 β / α 0 1 β / α 0 1 β
α 0 0 0 / β 1 1 1 / β 1 1 1 / α 0 0 0
α 0 0 0 / 0 0 0 0 / 1 1 1 1 / β 1 1 1
SHIFT RIGHT
A
B
C
D
0 β 1 α / 0 β 1 α / 0 β 1 α / 0 β 1 α
0 0 β β / α α 1 1 / α α 1 1 / 0 0 β β
0 0 0 0 / β β β β / 1 1 1 1 / α α α α
0 α α 0 / 0 α α 0 / β 1 1 β / β 1 1 β
SHIFT LEFT
A
B
C
D
0 β β 0 / 0 β β 0 / α 1 1 α / α 1 1 α
0 α 1 β / 0 α 1 β / 0 α 1 β / 0 α 1 β
0 0 α α / β β 1 1 / β β 1 1 / 0 0 α α
0 0 0 0 / α α α α / 1 1 1 1 / β β β β

COUNT UP

S	$\overline{A}$	$A\overline{B}$	$AB\overline{C}$	$ABC\overline{D}$
R	A	AB	ABC	ABCD
J	1	A	AB	ABC
K	1	A	AB	ABC
D	$\overline{A}$	$A\overline{B} + \overline{A}B$	$AB\overline{C} + \overline{B}C + \overline{A}C$	$ABC\overline{D} + \overline{C}D + \overline{B}D + \overline{A}D$

TB01430S

COUNT DOWN

S	$\overline{A}$	$\overline{A}\overline{B}$	$\overline{A}\overline{B}\overline{C}$	$\overline{A}\overline{B}\overline{C}\overline{D}$
R	A	$\overline{A}B$	$\overline{A}\overline{B}C$	$\overline{A}\overline{B}\overline{C}D$
J	1	$\overline{A}$	$\overline{A}\overline{B}$	$\overline{A}\overline{B}\overline{C}$
K	1	$\overline{A}$	$\overline{A}\overline{B}$	$\overline{A}\overline{B}\overline{C}$
D	$\overline{A}$	$A\overline{B} + AB$	$\overline{A}\overline{B}\overline{C} + AC + BC$	$\overline{A}\overline{B}\overline{C}\overline{D} + CD + AD + BD$

TB01440S

SHIFT RIGHT

S	B	C	D	A
R	$\overline{B}$	$\overline{C}$	$\overline{D}$	$\overline{A}$
J	B	C	D	A
K	$\overline{B}$	$\overline{C}$	$\overline{D}$	$\overline{A}$
D	B	C	D	A

TB01490S

SHIFT LEFT

S	D	A	B	C
R	$\overline{D}$	$\overline{A}$	$\overline{B}$	$\overline{C}$
J	D	A	B	C
K	$\overline{D}$	$\overline{A}$	$\overline{B}$	$\overline{C}$
D	D	A	B	C

TB01450S

Figure A-1 Karnaugh Maps and Flip-Flop Excitation Functions for the Counter/Shift-Register

Table A-5. PLS155 FPLS Programming Table for the Counter/Shift-Register

PROGRAM TABLE ENTRIES

C

INACTIVE	O
GENERATE	A
PROPAGATE	•
TRANSPARENT	–

AND

I, B(I), Q(P)

INACTIVE	O
I, B, Q	H
$\overline{I}, \overline{B}, \overline{Q}$	L
DON'T CARE	–

(AND)

(Q = J/K)

TOGGLE	O
SET	H
RESET	L
HOLD	–

(OR)

P, R, B(O), (Q = D)

ACTIVE	A
INACTIVE	•

(OR)

E_A, E_B

IDLE	O
CONTROL	A
ENABLE	•
DISABLE	–

F/F TYPE

J/K	•
D OR J/K	A

(OR)

HIGH	H
LOW	L

(POL.)

														F/F TYPE				E_B = A		E_A = A						POLARITY							
														A	A	A	A	A	A	A	A												H
	AND																	OR															
TERM	C	I				B(I)								Q(P)				Q(N)				P				B(O)							
		3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0	3	2	1	0	B	A	B	A	7	6	5	4	3	2	1	0
0	•	L	H	L	H	L		–	–	–	–	–	–	–	–	–	–	–	–	–	O	–	–	–	–	–	–	–	–	–	–	–	A
1	•	L	H	L	H	L		C	OU	N	T	–	–	–	–	–	L	–	–	O	–	–	–	–	–	–	–	–	–	–	–	–	A
2	•	L	H	L	H	L		–	D	O	W	N	–	–	–	L	L	–	O	–	–	–	–	–	–	–	–	–	–	–	–	–	A
3	•	L	H	L	H	L		–	–	–	–	–	–	–	L	L	L	O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	A
4	•	L	L	H	H	L		–	–	–	–	–	–	–	–	–	–	–	–	–	O	–	–	–	–	–	–	–	–	–	–	–	A
5	•	L	L	H	H	L		CO	UN	T	–	–	–	–	–	–	H	–	–	O	–	–	–	–	–	–	–	–	–	–	–	–	A
6	•	L	L	H	H	L			U	P	–	–	–	–	–	H	H	–	O	–	–	–	–	–	–	–	–	–	–	–	–	–	A
7	•	L	L	H	H	L		–	–	–	–	–	–	–	H	H	H	O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	A
8	•	L	H	L	L	L		–	–	–	–	–	–	H	–	–	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	A
9	•	L	H	L	L	L		SH	IF	T	–	–	–	–	–	–	H	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	A
10	•	L	H	L	L	L		–	LE	FT	–	–	–	–	–	H	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	A
11	•	L	H	L	L	L		–	–	–	–	–	–	–	H	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	A
12	•	L	L	H	L	L		–	–	–	–	–	–	–	–	H	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	A
13	•	L	L	H	L	L		SH	IF	T	–	–	–	–	H	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	A
14	•	L	L	H	L	L		–	RI	GHT	–	–	–	H	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	A
15	•	L	L	H	L	L		–	–	–	–	–	–	–	–	–	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	A
16	•	H	–	–	–	L	–	INI	TI	AL	IZE	–	–	–	–	–	–	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	•
17	•	–	–	–	–	H	–	R	E	SE	T	–	–	–	–	–	–	–	–	–	–	–	–	A	A	–	–	–	–	–	–	–	•
18	A	–	–	–	–	–	L	L	–	S	TO	P	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	•
19																																	
20																																	
21																																	
22																																	
23																																	
24																																	
25																																	
26																																	
27																																	
28																																	
29																																	
30																																	
31																																	
F_C	–	–	–	–	L	–	–	–	–	–	–	–	–	–	–	–	–																
L_B																																	
L_A																																	
D_7	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
D_6	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
D_5	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
D_4																																	
D_3																																	
D_2																																	
D_1																																	
D_0	–	–	–	–	–	–	–	L	–	–	–	–	–	–	–	–	–																
		5	4	3	2	19	18	13	12	9	8	7	6	17	16	15	14																
VARIABLE NAME		INIT	LEFT\DOWN	RIGHT\UP	COUNT\\$\overline{SHIFT}$	RESET	$\overline{HALT}$	$\overline{BUSY}$					ACTIVE	D	C	B	A																

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Table A-6. Modified PLS155 FPLS Programming Table for the Counter/Shift-Register With the Addition of a Binary Multiplier

														F/F TYPE				E_B = A		E_A = A						POLARITY							
														A	A	A	A	A	A	A	A												H
		AND																OR															
TERM	C	I				B(I)								Q(P)				Q(N)				P				B(O)							
		3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0	3	2	1	0	B	A	B	A	7	6	5	4	3	2	1	0
0	•	L	H	L	H	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	O	-	-	-	-	-	-	-	-	-	-	-	A
1	•	L	H	L	H	L	-	-	-	-	-	-	-	-	-	-	L	-	-	O	-	-	-	-	-	-	-	-	-	-	-	-	A
2	•	L	H	L	H	L	-	-	-	-	-	-	-	-	-	L	L	-	O	-	-	-	-	-	-	-	-	-	-	-	-	-	A
3	•	L	H	L	H	L	-	-	-	-	-	-	-	-	L	L	L	O	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A
4	•	L	L	H	H	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	O	-	-	-	-	-	-	-	-	-	-	-	A
5	•	L	L	H	H	L	-	-	-	-	-	-	-	-	-	-	H	-	-	O	-	-	-	-	-	-	-	-	-	-	-	-	A
6	•	L	L	H	H	L	-	-	-	-	-	-	-	-	-	H	H	-	O	-	-	-	-	-	-	-	-	-	-	-	-	-	A
7	•	L	L	H	H	L	-	-	-	-	-	-	-	-	H	H	H	O	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A
8	•	L	H	L	L	L	-	-	L	H	-	-	-	H	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	A
9	•	L	H	L	L	L	-	-	H	L	-	-	-	-	H	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	A
10	•	L	H	L	L	L	-	-	H	H	-	-	-	-	-	H	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	A
11	•	L	H	L	L	L	-	-	L	H	-	-	-	-	-	-	H	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	A
12	•	L	H	L	L	L	-	-	H	L	-	-	-	H	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	A
13	•	L	H	L	L	L	-	-	H	H	-	-	-	-	H	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	A
14	•	L	H	L	L	L	-	-	L	H	-	-	-	-	-	H	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	A
15	•	L	H	L	L	L	-	-	H	L	-	-	-	-	-	-	H	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	A
16	•	L	H	L	L	L	-	-	H	H	-	-	-	H	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	A
17	•	L	H	L	L	L	-	-	L	H	-	-	-	-	H	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A
18	•	L	H	L	L	L	-	-	H	L	-	-	-	-	-	H	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A
19	•	L	H	L	L	L	-	-	H	H	-	-	-	-	-	-	H	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A
20	•	L	L	H	L	L	-	-	-	-	-	-	-	-	-	H	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	A
21	•	L	L	H	L	L	-	-	-	-	-	-	-	-	H	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	A
22	•	L	L	H	L	L	-	-	-	-	-	-	-	H	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	A
23	•	L	L	H	L	L	-	-	-	-	-	-	-	-	-	-	H	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A
24	•	H	-	-	-	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	•
25	•	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	•
26	A	-	-	-	-	-	L	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	•
27																																	
28																																	
29																																	
30																																	
31																																	
F_C	-	-	-	-	L	-	-	-	-	-	-	-	-	-	-	-	-																
L_B																																	
L_A																																	
D_7	•	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O																
D_6	•	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O																
D_5	•	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O																
D_4	•	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O																
D_3	•	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O																
D_2																																	
D_1																																	
D_0	-	-	-	-	-	-	-	L	-	-	-	-	-	-	-	-	-																
		5	4	3	2	19	18	13	12	9	8	7	6	17	16	15	14																
VARIABLE NAME		INIT	LEFT\DOWN	RIGHT\UP	COUNT\$\overline{SHIFT}$	RESET	$\overline{HALT}$	$\overline{BUSY}$					ACTIVE	D	C	B	A																

PROGRAM TABLE ENTRIES

I, B(I), Q(P)	
INACTIVE	O
I, B, Q	H
$\overline{I}, \overline{B}, \overline{Q}$	L
DON'T CARE	–

(AND)

C	
INACTIVE	O
GENERATE	A
PROPAGATE	•
TRANSPARENT	–

AND

P, R, B(O), (Q = D)	
ACTIVE	A
INACTIVE	•

(OR)

(Q = J/K)	
TOGGLE	O
SET	H
RESET	L
HOLD	–

(OR)

HIGH	H
LOW	L

(POL.)

E_A, E_B	
IDLE	O
CONTROL	A
ENABLE	•
DISABLE	–

F/F TYPE	
J/K	•
D OR J/K	A

(OR)

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Signetics

AN10
4-Bit Binary-To-7 Segment Decoder

Application Note

Application Specific Products

INTRODUCTION

Using the PLS153 or PLS153A, a 4-bit binary-to-7 segment decoder may be easily constructed. This paper will cover Hex-to-7 segment decoder, BCD-to-7 segment decoder, decoder with latches, and decoder with multiplexer. The architecture of PLS153/153A is basically an AND-OR matrix. The large number of inputs of each AND term is ideal for decoder applications, and the ability to drive the entire OR array makes possible the efficient use of AND terms such that, together with the programmable output polarity, a minimum number of AND terms is needed to implement the decoder function. Another important feature of the PLS153/153A architecture is the 10 bidirectional I/O pins. The bidirectionality of these pins provides internal feedback to the AND matrix, which eliminates the need for external wiring and, more importantly, it saves I/O pin requirements. All I/O pins of the PLS153/153A have tri-state output buffers, each may be enabled or disabled by its own controlling AND terms. In applications where high current drive is necessary but low power consumption is still desirable, the AND term controlled tri-state buffers are ideal for multiplexing. The LED display may be driven at a higher current and lower duty cycle to get better brightness/current efficiency and reduce the overall power dissipation.

DESCRIPTION

Hex-To-7 Segment Decoder

A 7 segment display (Figure 1) may be used to represent a hexadecimal number as shown in Table 1. The format serves merely as an example. Some designers may prefer other configurations, particularly for letters B and D. Before implementing the truth table with programmable logic devices, one has to decide whether the outputs should be Active-High or Active-Low. If a moderate drive current of 15mA or less is needed, and if a common anode LED display is used, then an Active-Low output configuration is sufficient. On the other hand, if only a common cathode LED display is available and the current drive requirement is not very critical, an Active-High output configuration may be used. The change of output polarity may be easily affected by putting in the POLARITY section 'H' for Active-High and 'L' for Active-Low. Since the output polarity is programmable, one may choose to describe the logic in terms of outputs equal to '1's or outputs equal to '0's.

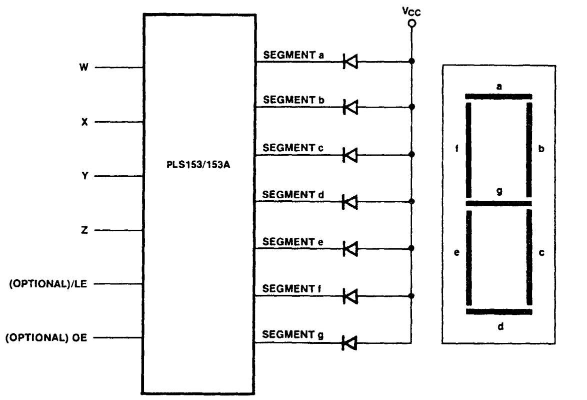

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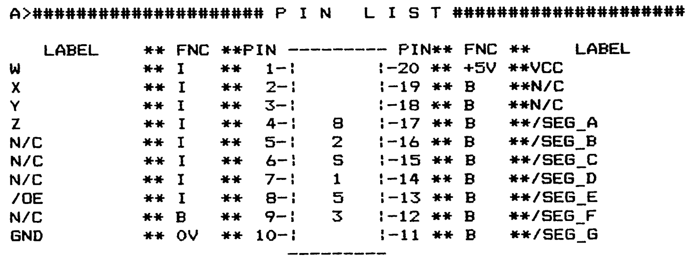
Figure 1. 7 Segment Decoder Driving a Common Anode LED Display



```
A>######################## P I N   L I S T #######################

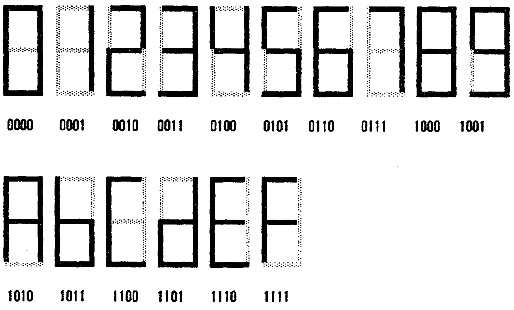
   LABEL      ** FNC **PIN ---------- PIN** FNC **     LABEL
W             ** I   **  1-¦         ¦-20 ** +5V **VCC
X             ** I   **  2-¦         ¦-19 ** B   **N/C
Y             ** I   **  3-¦         ¦-18 ** B   **N/C
Z             ** I   **  4-¦    8    ¦-17 ** B   **/SEG_A
N/C           ** I   **  5-¦    2    ¦-16 ** B   **/SEG_B
N/C           ** I   **  6-¦    S    ¦-15 ** B   **/SEG_C
N/C           ** I   **  7-¦    1    ¦-14 ** B   **/SEG_D
/OE           ** I   **  8-¦    5    ¦-13 ** B   **/SEG_E
N/C           ** B   **  9-¦    3    ¦-12 ** B   **/SEG_F
GND           ** OV  ** 10-¦         ¦-11 ** B   **/SEG_G
                            ----------
```

TB00981S

Figure 2. Pin List of Binary-to-7 Segment Decoder

NOTE:
PLSXXX and 82SXXX are interchangeable part numbers.

Table 1. Truth Table of Hex–to–7–Segment Decoder



ZYXW	a	b	c	d	e	f	g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	1	0	1	1
1010	1	1	1	0	1	1	1
1011	0	0	1	1	1	1	1
1100	1	0	0	1	1	1	0
1101	0	1	1	1	1	0	1
1110	1	0	0	1	1	1	1
1111	1	0	0	0	1	1	1

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Table 2. H/L Programming Table for Binary-to-7-Segment Decoder

82S153/153A PROGRAMMING TABLE DRAWING ID: B TO 7 SEG DECODER REV. –

DESIGNER: D.K. WONG DATE: 12/15/84

																			POLARITY											
																			H	H	L	L	L	L	L	L	L	H	COMMENTS	
	AND																		OR											
	I								B(I)										B(O)											
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	INPUT	OUTPUT
0	-	-	-	-	L	L	L	L	-	-	-	-	-	-	-	-	-	-	•	•	A	A	A	A	A	A	•	•	0	0
1	-	-	-	-	L	L	L	H	-	-	-	-	-	-	-	-	-	-	•	•	•	A	A	•	•	•	•	•	1	1
2	-	-	-	-	L	L	H	L	-	-	-	-	-	-	-	-	-	-	•	•	A	A	•	A	A	•	A	•	2	2
3	-	-	-	-	L	L	H	H	-	-	-	-	-	-	-	-	-	-	•	•	A	A	A	A	•	•	A	•	3	3
4	-	-	-	-	L	H	L	L	-	-	-	-	-	-	-	-	-	-	•	•	•	A	A	•	•	A	A	•	4	4
5	-	-	-	-	L	H	L	H	-	-	-	-	-	-	-	-	-	-	•	•	A	•	A	A	•	A	A	•	5	5
6	-	-	-	-	L	H	H	L	-	-	-	-	-	-	-	-	-	-	•	•	A	•	A	A	A	A	A	•	6	6
7	-	-	-	-	L	H	H	H	-	-	-	-	-	-	-	-	-	-	•	•	A	A	A	•	•	•	•	•	7	7
8	-	-	-	-	H	L	L	L	-	-	-	-	-	-	-	-	-	-	•	•	A	A	A	A	A	A	A	•	8	8
9	-	-	-	-	H	L	L	H	-	-	-	-	-	-	-	-	-	-	•	•	A	A	A	A	•	A	A	•	9	9
10	-	-	-	-	H	L	H	L	-	-	-	-	-	-	-	-	-	-	•	•	A	A	A	•	A	A	A	•	10	A
11	-	-	-	-	H	L	H	H	-	-	-	-	-	-	-	-	-	-	•	•	•	•	A	A	A	A	A	•	11	b
12	-	-	-	-	H	H	L	L	-	-	-	-	-	-	-	-	-	-	•	•	A	•	•	A	A	A	A	•	12	C
13	-	-	-	-	H	H	L	H	-	-	-	-	-	-	-	-	-	-	•	•	•	A	A	A	A	•	A	•	13	d
14	-	-	-	-	H	H	H	L	-	-	-	-	-	-	-	-	-	-	•	•	A	•	•	A	A	A	A	•	14	E
15	-	-	-	-	H	H	H	H	-	-	-	-	-	-	-	-	-	-	•	•	A	•	•	•	A	A	A	•	15	F
16																														
17																														
18																														
19																														
20																														
21																														
22																														
23																														
24																														
25																														
26																														
27																														
28																														
29																														
30																														
31																														
D9																														
D8																														
D7	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ENABLE B7 FOR OUTPUT (SEG A)											
D6	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	" B6 " " " B											
D5	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	" B5 " " " C											
D4	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	" B4 " " " D											
D3	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	" B3 " " " E											
D2	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	" B2 " " " F											
D1	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	" B1 " " " G											
D0																														
NAME	/OE				Z	Y	X	W													A	B	C	D	E	F	G			

TB01001S

4-Bit Binary-To-7 Segment Decoder AN10

Table 3. H/L Programming Table for Binary-to-7 Segment Decoder

82S153/153A PROGRAMMING TABLE DRAWING ID: B TO 7 SEG DECODER REV. A
DESIGNER: D. K. Wong DATE: 12/15/84

	AND																		OR										
POLARITY																			H	H	H	H	H	H	H	H	H	H	
	I								B(I)										B(O)										
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	COMMENTS
0	-	-	-	-	L	L	L	L	-	-	-	-	-	-	-	-	-	-	•	•	•	•	•	•	•	•	A	•	0
1	-	-	-	-	L	L	L	H	-	-	-	-	-	-	-	-	-	-	•	•	A	•	-	A	A	A	A	•	1
2	-	-	-	-	L	L	H	L	-	-	-	-	-	-	-	-	-	-	•	•	•	•	A	•	•	A	•	•	2
3	-	-	-	-	L	L	H	H	-	-	-	-	-	-	-	-	-	-	•	•	•	•	•	•	A	A	•	•	3
4	-	-	-	-	L	H	L	L	-	-	-	-	-	-	-	-	-	-	•	•	A	•	•	A	A	•	•	•	4
5	-	-	-	-	L	H	L	H	-	-	-	-	-	-	-	-	-	-	•	•	•	A	•	•	A	•	•	•	5
6	-	-	-	-	L	H	H	L	-	-	-	-	-	-	-	-	-	-	•	•	•	A	•	•	•	•	•	•	6
7	-	-	-	-	L	H	H	H	-	-	-	-	-	-	-	-	-	-	•	•	•	•	-	A	A	A	A	•	7
8	-	-	-	-	H	L	L	L	-	-	-	-	-	-	-	-	-	-	•	•	•	•	•	•	•	•	•	•	8 (*)
9	-	-	-	-	H	L	L	H	-	-	-	-	-	-	-	-	-	-	•	•	•	•	•	•	A	•	•	•	9
10	-	-	-	-	H	L	H	L	-	-	-	-	-	-	-	-	-	-	•	•	•	•	•	A	•	•	•	•	A
11	-	-	-	-	H	L	H	H	-	-	-	-	-	-	-	-	-	-	•	•	A	A	•	•	•	•	•	•	b
12	-	-	-	-	H	H	L	L	-	-	-	-	-	-	-	-	-	-	•	•	•	A	A	•	•	•	A	•	C
13	-	-	-	-	H	H	L	H	-	-	-	-	-	-	-	-	-	-	•	•	A	•	•	•	•	A	•	•	d
14	-	-	-	-	H	H	H	L	-	-	-	-	-	-	-	-	-	-	•	•	•	A	A	•	•	•	•	•	E
15	-	-	-	-	H	H	H	H	-	-	-	-	-	-	-	-	-	-	•	•	•	A	A	A	•	•	•	•	F
16																													
17																													
18																													
19																													
20																													
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22																													
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25																													
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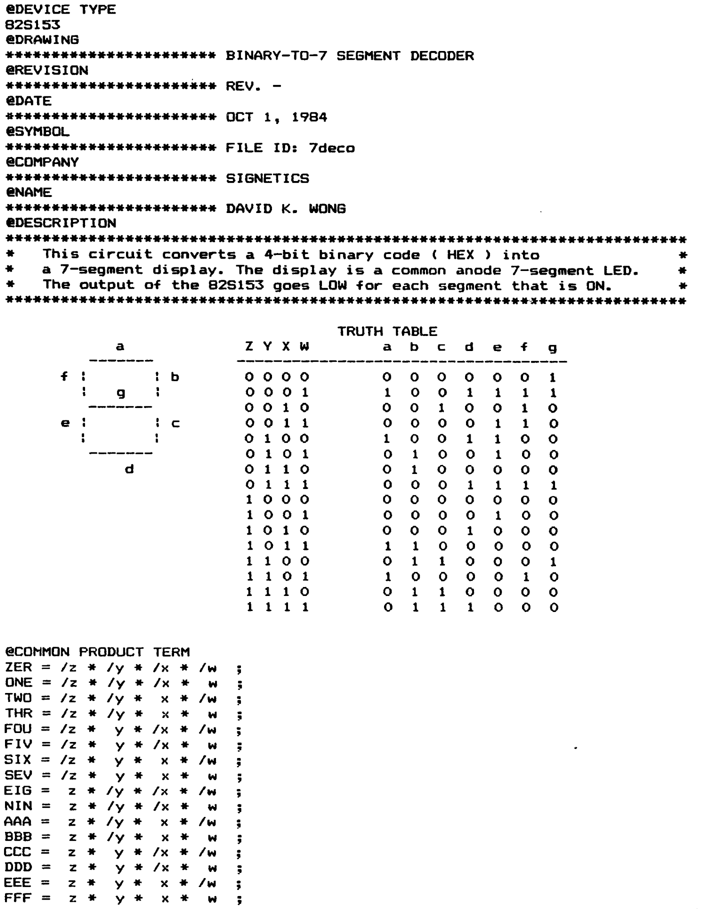
27																													
28																													
29																													
30																													
31																													
D9																													
D8																													
D7	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D6	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D5	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D4	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D3	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D2	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D1	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D0																													
NAME	OE				Z	Y	X	W													A	B	C	D	E	F	G		

(*) SINCE THIS TERM IS "INACTIVE", IT MAY BE DELETED. THEREFORE, THE TOTAL # OF TERMS REQUIRED IS 15.

TB01011S

4-Bit Binary-To-7 Segment Decoder AN10



```
@DEVICE TYPE
82S153
@DRAWING
************************ BINARY-TO-7 SEGMENT DECODER
@REVISION
************************ REV. -
@DATE
************************ OCT 1, 1984
@SYMBOL
************************ FILE ID: 7deco
@COMPANY
************************ SIGNETICS
@NAME
************************ DAVID K. WONG
@DESCRIPTION
**************************************************************************
*   This circuit converts a 4-bit binary code ( HEX ) into               *
*   a 7-segment display. The display is a common anode 7-segment LED.    *
*   The output of the 82S153 goes LOW for each segment that is ON.       *
**************************************************************************

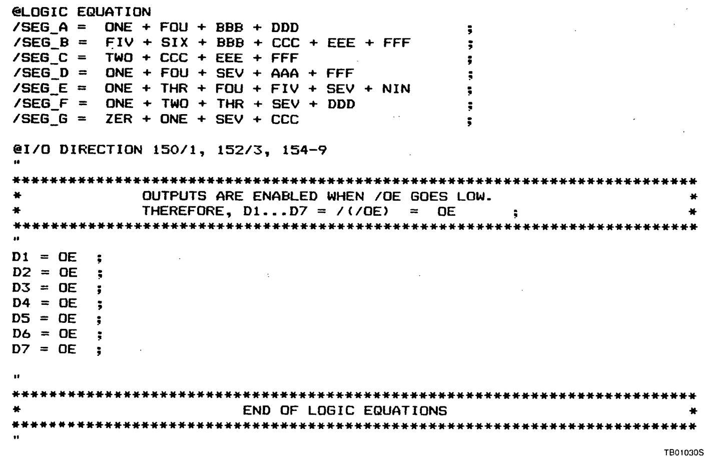
                                        TRUTH TABLE
           a            Z Y X W         a  b  c  d  e  f  g
        -------         --------------------------------------
     f :       : b      0 0 0 0         0  0  0  0  0  0  1
       :   g   :        0 0 0 1         1  0  0  1  1  1  1
        -------         0 0 1 0         0  0  1  0  0  1  0
     e :       : c      0 0 1 1         0  0  0  0  1  1  0
       :       :        0 1 0 0         1  0  0  1  1  0  0
        -------         0 1 0 1         0  1  0  0  1  0  0
           d            0 1 1 0         0  1  0  0  0  0  0
                        0 1 1 1         0  0  0  1  1  1  1
                        1 0 0 0         0  0  0  0  0  0  0
                        1 0 0 1         0  0  0  0  1  0  0
                        1 0 1 0         0  0  0  1  0  0  0
                        1 0 1 1         1  1  0  0  0  0  0
                        1 1 0 0         0  1  1  0  0  0  1
                        1 1 0 1         1  0  0  0  0  1  0
                        1 1 1 0         0  1  1  0  0  0  0
                        1 1 1 1         0  1  1  1  0  0  0


@COMMON PRODUCT TERM
ZER = /z * /y * /x * /w  ;
ONE = /z * /y * /x *  w  ;
TWO = /z * /y *  x * /w  ;
THR = /z * /y *  x *  w  ;
FOU = /z *  y * /x * /w  ;
FIV = /z *  y * /x *  w  ;
SIX = /z *  y *  x * /w  ;
SEV = /z *  y *  x *  w  ;
EIG =  z * /y * /x * /w  ;
NIN =  z * /y * /x *  w  ;
AAA =  z * /y *  x * /w  ;
BBB =  z * /y *  x *  w  ;
CCC =  z *  y * /x * /w  ;
DDD =  z *  y * /x *  w  ;
EEE =  z *  y *  x * /w  ;
FFF =  z *  y *  x *  w  ;
```

TB01020S

Figure 3. Boolean Equation for Binary-to-7 Segment Decoder

4-Bit Binary-To-7 Segment Decoder AN10



```
@LOGIC EQUATION
/SEG_A =  ONE + FOU + BBB + DDD                       ;
/SEG_B =  FIV + SIX + BBB + CCC + EEE + FFF           ;
/SEG_C =  TWO + CCC + EEE + FFF                       ;
/SEG_D =  ONE + FOU + SEV + AAA + FFF                 ;
/SEG_E =  ONE + THR + FOU + FIV + SEV + NIN           ;
/SEG_F =  ONE + TWO + THR + SEV + DDD                 ;
/SEG_G =  ZER + ONE + SEV + CCC                       ;

@I/O DIRECTION 150/1, 152/3, 154-9
"
****************************************************************************
*              OUTPUTS ARE ENABLED WHEN /OE GOES LOW.                      *
*              THEREFORE, D1...D7 = /(/OE)  =  OE      ;                   *
****************************************************************************
"
D1 = OE  ;
D2 = OE  ;
D3 = OE  ;
D4 = OE  ;
D5 = OE  ;
D6 = OE  ;
D7 = OE  ;

"
****************************************************************************
*                         END OF LOGIC EQUATIONS                           *
****************************************************************************
"
```

TB01030S

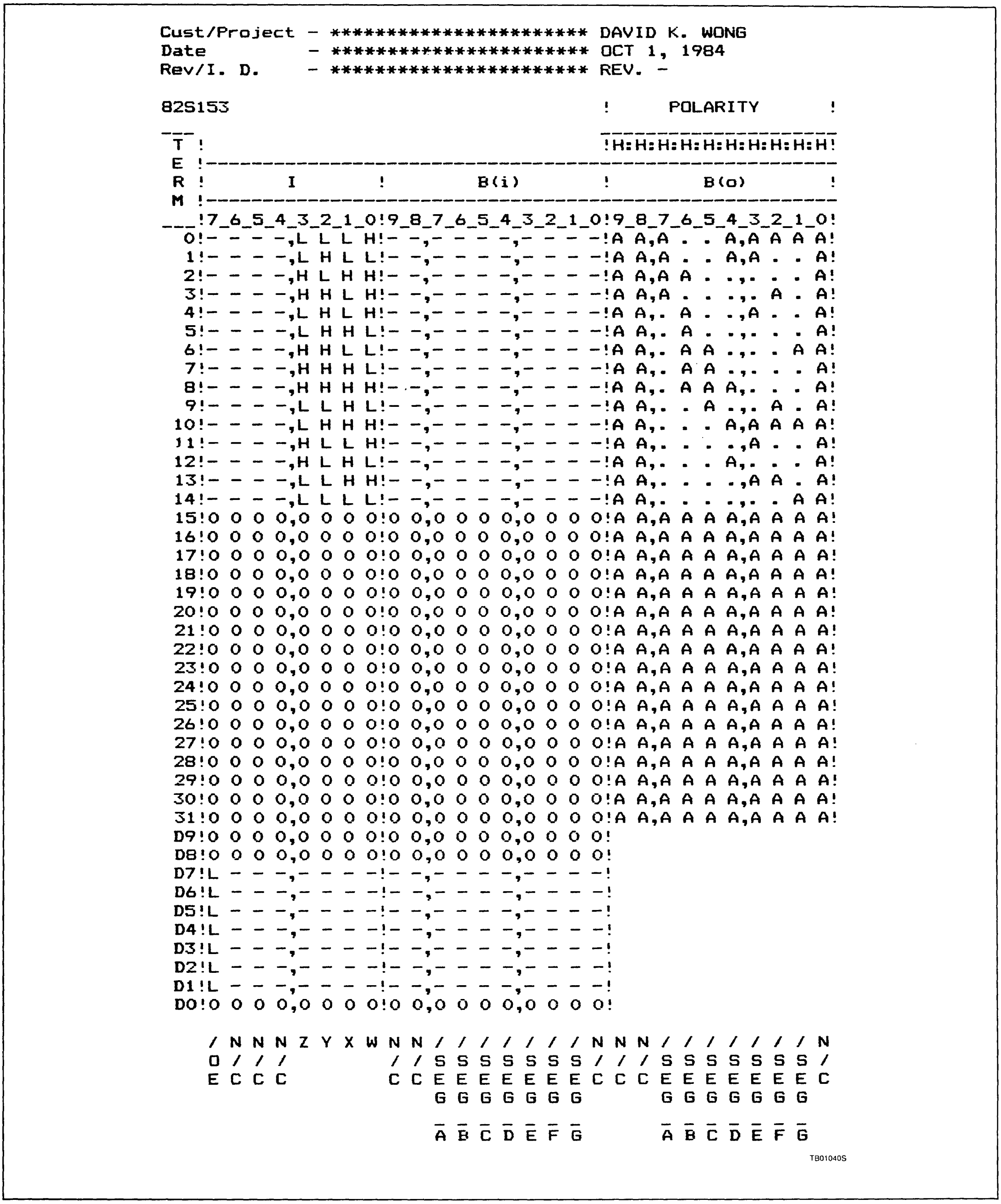
Figure 3 (Continued)

In this example, an Active-Low output goes Low when a segment is to be turned on. The truth table shown in Table 1 is translated into an H/L programming table as shown in Table 2. Since the LED display used here is common anode, the output polarity of each output pin is programmed "L" so that an output goes low when a segment is to be turned on. The decoder takes 16 AND terms. Notice that all outputs go Low when input equals "8". If the logic is written for "0s" instead of "1s", one AND term could be saved. Table 3 shows that the same circuit may be implemented by using only 15 AND terms. Notice that the polarity is the reverse of that of Table 2. The outputs may be turned on and off by I_7, /OE, which controls the 7 tri-state output buffers through control terms (AND terms D_1 to D_7). The same design is also implemented using Boolean equations with AMAZE. Figures 2 through 4 are, respectively, pin list, logic equations, and logic simulation results of the hex-to-7 segment decoder circuit generated by AMAZE. Table 4 is the H/L table generated by AMAZE. In the process of generating Boolean equations for the decoder, common product terms are used to economize the usage of AND terms.

4-Bit Binary-To-7 Segment Decoder

AN10

Table 4. H/L Table Generated by AMAZE for Binary-to-7 Segment Decoder



```
Cust/Project - ************************ DAVID K. WONG
Date         - ************************ OCT 1, 1984
Rev/I. D.    - ************************ REV. -

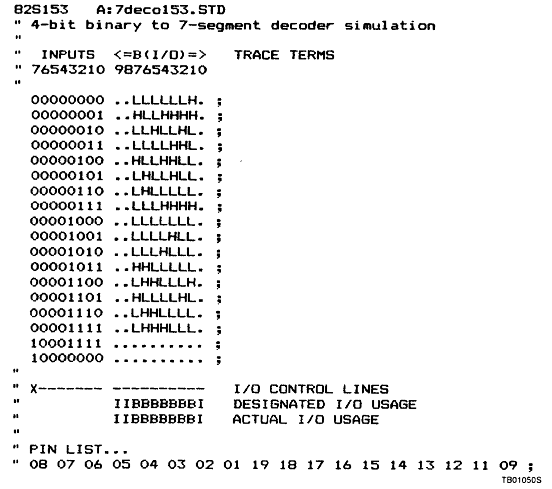
82S153                                 !     POLARITY      !
___                                    ---------------------
 T !                                   !H:H:H:H:H:H:H:H:H:H!
 E !--------------------------------------------------------
 R !       I       !        B(i)       !        B(o)       !
 M !--------------------------------------------------------
___!7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!- - - -,L L L H!- -,- - - -,- - - -!A A,A . . A,A A A A!
  1!- - - -,L H L L!- -,- - - -,- - - -!A A,A . . A,A . . A!
  2!- - - -,H L H H!- -,- - - -,- - - -!A A,A A . .,. . . A!
  3!- - - -,H H L H!- -,- - - -,- - - -!A A,A . . .,. A . A!
  4!- - - -,L H L H!- -,- - - -,- - - -!A A,. A . .,A . . A!
  5!- - - -,L H H L!- -,- - - -,- - - -!A A,. A . .,. . . A!
  6!- - - -,H H L L!- -,- - - -,- - - -!A A,. A A .,. . A A!
  7!- - - -,H H H L!- -,- - - -,- - - -!A A,. A A .,. . . A!
  8!- - - -,H H H H!- -,- - - -,- - - -!A A,. A A A,. . . A!
  9!- - - -,L L H L!- -,- - - -,- - - -!A A,. . A .,. A . A!
 10!- - - -,L H H H!- -,- - - -,- - - -!A A,. . . A,A A A A!
 11!- - - -,H L L H!- -,- - - -,- - - -!A A,. . . .,A . . A!
 12!- - - -,H L H L!- -,- - - -,- - - -!A A,. . . A,. . . A!
 13!- - - -,L L H H!- -,- - - -,- - - -!A A,. . . .,A A . A!
 14!- - - -,L L L L!- -,- - - -,- - - -!A A,. . . .,. . A A!
 15!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 16!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 17!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 18!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 19!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 23!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 25!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 27!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 31!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 D9!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D8!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D7!L - - -,- - - -!- -,- - - -,- - - -!
 D6!L - - -,- - - -!- -,- - - -,- - - -!
 D5!L - - -,- - - -!- -,- - - -,- - - -!
 D4!L - - -,- - - -!- -,- - - -,- - - -!
 D3!L - - -,- - - -!- -,- - - -,- - - -!
 D2!L - - -,- - - -!- -,- - - -,- - - -!
 D1!L - - -,- - - -!- -,- - - -,- - - -!
 D0!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!

    / N N N Z Y X W N N / / / / / / / N N N / / / / / / / N
    O / / /         / / S S S S S S S / / / S S S S S S S /
    E C C C         C C E E E E E E E C C C E E E E E E E C
                      G G G G G G G           G G G G G G G

                      - - - - - - -           - - - - - - -
                      A B C D E F G           A B C D E F G
```

TB01040S

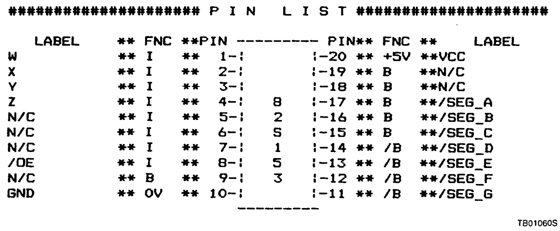
4-Bit Binary-To-7 Segment Decoder | AN10



```
82S153    A:7deco153.STD
" 4-bit binary to 7-segment decoder simulation
"
"  INPUTS  <=B(I/O)=>   TRACE TERMS
" 76543210 9876543210
"
  00000000 ..LLLLLLH. ;
  00000001 ..HLLHHHH. ;
  00000010 ..LLHLLHL. ;
  00000011 ..LLLLHHL. ;
  00000100 ..HLLHHLL. ;
  00000101 ..LHLLHLL. ;
  00000110 ..LHLLLLL. ;
  00000111 ..LLLHHHH. ;
  00001000 ..LLLLLLL. ;
  00001001 ..LLLLHLL. ;
  00001010 ..LLLHLLL. ;
  00001011 ..HHLLLLL. ;
  00001100 ..LHHLLLH. ;
  00001101 ..HLLLLHL. ;
  00001110 ..LHHLLLL. ;
  00001111 ..LHHHLLL. ;
  10001111 .......... ;
  10000000 .......... ;
"
" X------- ----------   I/O CONTROL LINES
"          IIBBBBBBBI   DESIGNATED I/O USAGE
"          IIBBBBBBBI   ACTUAL I/O USAGE
"
" PIN LIST...
" 08 07 06 05 04 03 02 01 19 18 17 16 15 14 13 12 11 09 ;
```

TB01050S

Figure 4



```
###################### P I N   L I S T ######################

   LABEL     ** FNC **PIN --------- PIN** FNC **    LABEL
W            ** I   **  1-¦         ¦-20 ** +5V **VCC
X            ** I   **  2-¦         ¦-19 ** B   **N/C
Y            ** I   **  3-¦         ¦-18 ** B   **N/C
Z            ** I   **  4-¦    8    ¦-17 ** B   **/SEG_A
N/C          ** I   **  5-¦    2    ¦-16 ** B   **/SEG_B
N/C          ** I   **  6-¦    S    ¦-15 ** B   **/SEG_C
N/C          ** I   **  7-¦    1    ¦-14 ** /B  **/SEG_D
/OE          ** I   **  8-¦    5    ¦-13 ** /B  **/SEG_E
N/C          ** B   **  9-¦    3    ¦-12 ** /B  **/SEG_F
GND          ** OV  ** 10-¦         ¦-11 ** /B  **/SEG_G
                            ---------
```

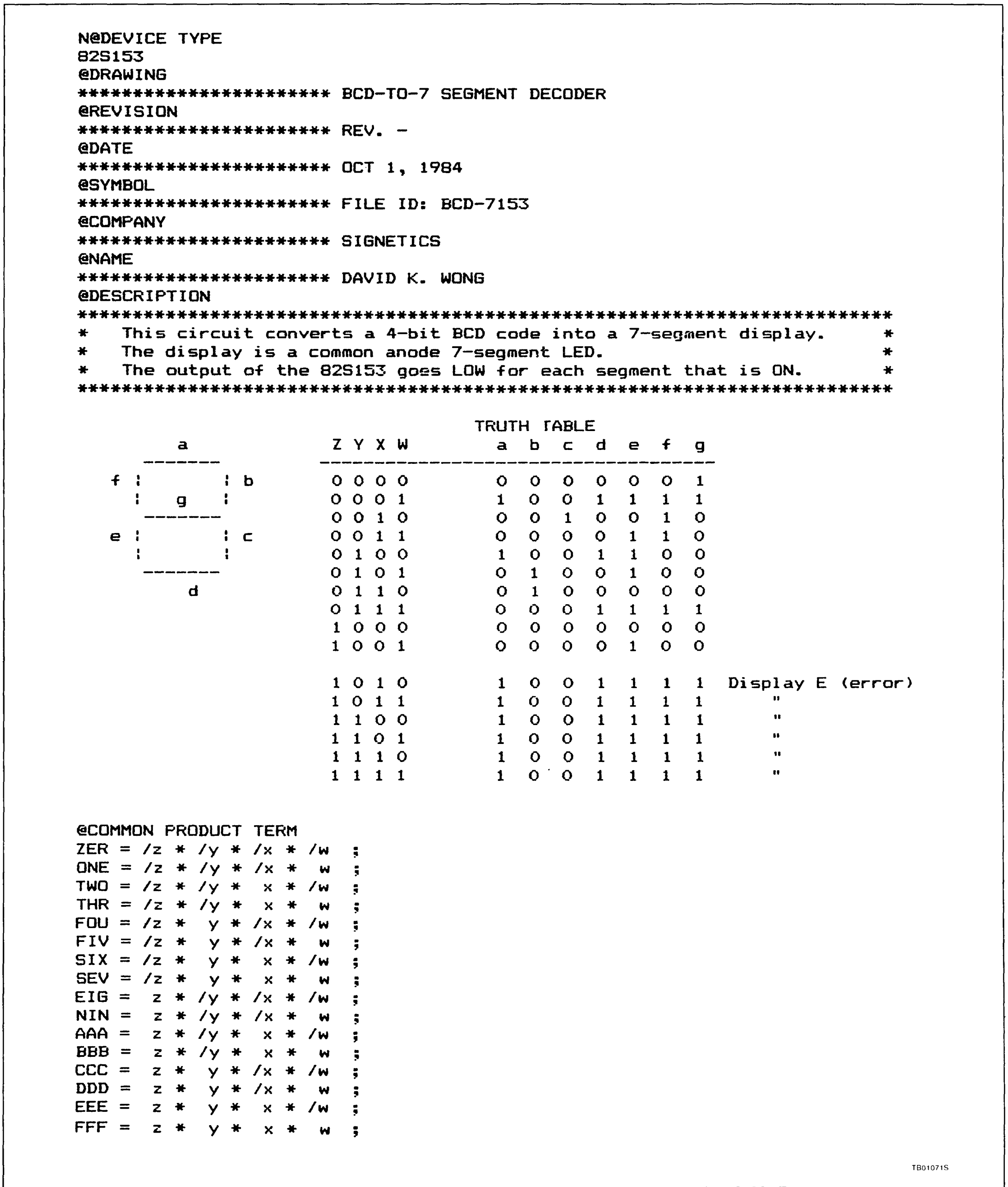
TB01060S

Figure 5. Pin List of Binary-to-7 Segment Decoder Generated by AMAZE

BCD-To-7 Segment Decoder

Using the same principle as in the previous example, a BCD input may be converted to a 7 segment display. If the input will always be within the range of 0000B to 1001B, the design will take ten AND terms to implement the decoding function. But if the display of an error message is desired when input exceeds 1001B, the design shown in Figures 5 and 6 and Table 5, may be used. Alternatively, the error message "E" will be displayed if the input does not equal anything between 0000B and 1001B inclusively. The circuit used to detect that none of the ten AND terms being true is shown in Figure 7 where if the input is outside of the range of 0000B to 1001B, none of the terms ZER to NIN will be active, which in turn causes the output of the NOR term to be High. The High output then causes the "E" term to be active and thus an output "E" is displayed. This scheme takes two propagation delays before "E" is displayed but only one delay for "0" to "9" to be displayed. The circuit shown in Figure 7 is implemented as shown in Table 4, column $B(O)_0$ of terms 0 to 9, and term #11. The output $B(O)_0$ becomes High when terms 0 to 9 are inactive, $(T_0 + T_1 + T_2 + T_3 + T_4 + T_5 + T_6 + T_7 + T_8 + T_9) = 0$ where T_0 is term #0, T_1 is term #1, T_2 is . . ., etc. $B(O)_0$ is then fed back to the input of term #11 which, when active, causes outputs B and C to be High, segments B and C to turn off and the other segments to turn on. Term #10 is left blank to separate the main decoding function and the feedback function for the sake of clarity of this demonstration. A similar feature (the COMPLEMENT ARRAY) may be found in PLS155/157/159 where the feedback path is buried inside the chip without having to use up one I/O pin. Notice that this feature greatly reduces the number of AND terms needed. But for device architectures which do not allow common AND terms, this logic minimization will not be possible. Figure 8 and Table 6 implement design with AMAZE. The circuit is then simulated as shown in Figure 9.

4-Bit Binary-To-7 Segment Decoder AN10



```
N@DEVICE TYPE
82S153
@DRAWING
************************ BCD-TO-7 SEGMENT DECODER
@REVISION
************************ REV. -
@DATE
************************ OCT 1, 1984
@SYMBOL
************************ FILE ID: BCD-7153
@COMPANY
************************ SIGNETICS
@NAME
************************ DAVID K. WONG
@DESCRIPTION
**************************************************************************
*   This circuit converts a 4-bit BCD code into a 7-segment display.     *
*   The display is a common anode 7-segment LED.                         *
*   The output of the 82S153 goes LOW for each segment that is ON.       *
**************************************************************************

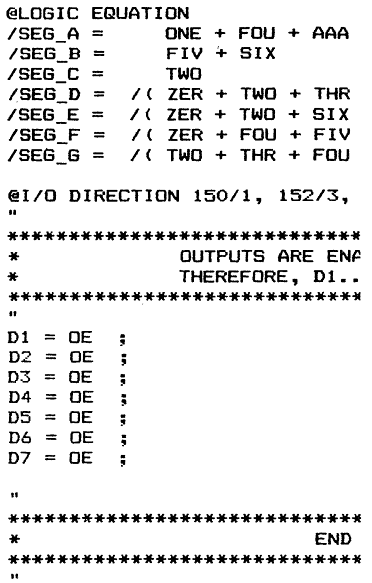
                                          TRUTH TABLE
          a              Z Y X W         a  b  c  d  e  f  g
       -------           ----------------------------------------
   f :         : b       0 0 0 0         0  0  0  0  0  0  1
     :    g    :         0 0 0 1         1  0  0  1  1  1  1
       -------           0 0 1 0         0  0  1  0  0  1  0
   e :         : c       0 0 1 1         0  0  0  0  1  1  0
     :         :         0 1 0 0         1  0  0  1  1  0  0
       -------           0 1 0 1         0  1  0  0  1  0  0
          d              0 1 1 0         0  1  0  0  0  0  0
                         0 1 1 1         0  0  0  1  1  1  1
                         1 0 0 0         0  0  0  0  0  0  0
                         1 0 0 1         0  0  0  0  1  0  0

                         1 0 1 0         1  0  0  1  1  1  1   Display E (error)
                         1 0 1 1         1  0  0  1  1  1  1       "
                         1 1 0 0         1  0  0  1  1  1  1       "
                         1 1 0 1         1  0  0  1  1  1  1       "
                         1 1 1 0         1  0  0  1  1  1  1       "
                         1 1 1 1         1  0  0  1  1  1  1       "


@COMMON PRODUCT TERM
ZER = /z * /y * /x * /w  ;
ONE = /z * /y * /x *  w  ;
TWO = /z * /y *  x * /w  ;
THR = /z * /y *  x *  w  ;
FOU = /z *  y * /x * /w  ;
FIV = /z *  y * /x *  w  ;
SIX = /z *  y *  x * /w  ;
SEV = /z *  y *  x *  w  ;
EIG =  z * /y * /x * /w  ;
NIN =  z * /y * /x *  w  ;
AAA =  z * /y *  x * /w  ;
BBB =  z * /y *  x *  w  ;
CCC =  z *  y * /x * /w  ;
DDD =  z *  y * /x *  w  ;
EEE =  z *  y *  x * /w  ;
FFF =  z *  y *  x *  w  ;
```

TB01071S

Figure 6. Boolean Equations for BCD-to-7 Segment Decoder for AMAZE



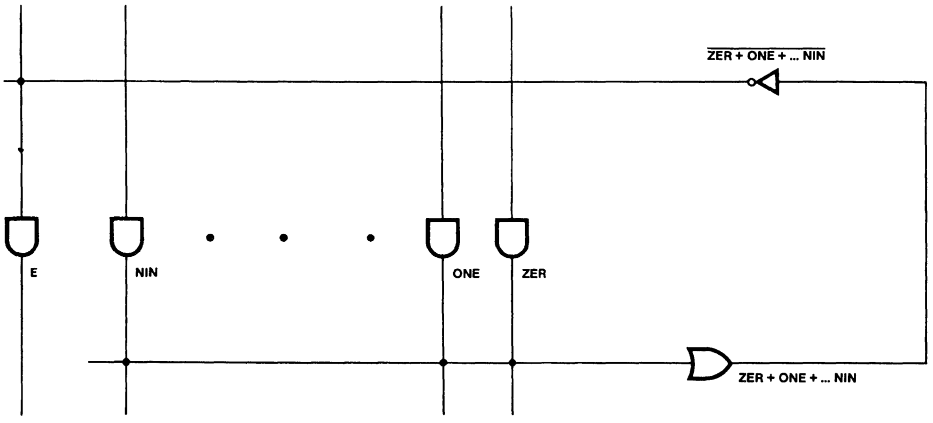
```
@LOGIC EQUATION
/SEG_A =      ONE + FOU + AAA
/SEG_B =      FIV + SIX
/SEG_C =      TWO
/SEG_D =   /( ZER + TWO + THR
/SEG_E =   /( ZER + TWO + SIX
/SEG_F =   /( ZER + FOU + FIV
/SEG_G =   /( TWO + THR + FOU

@I/O DIRECTION 150/1, 152/3,
"
*****************************
*              OUTPUTS ARE ENA
*              THEREFORE, D1..
*****************************
"
D1 = OE  ;
D2 = OE  ;
D3 = OE  ;
D4 = OE  ;
D5 = OE  ;
D6 = OE  ;
D7 = OE  ;

"
*****************************
*                         END
*****************************
"
```

TB01081S

Figure 6 (Continued)



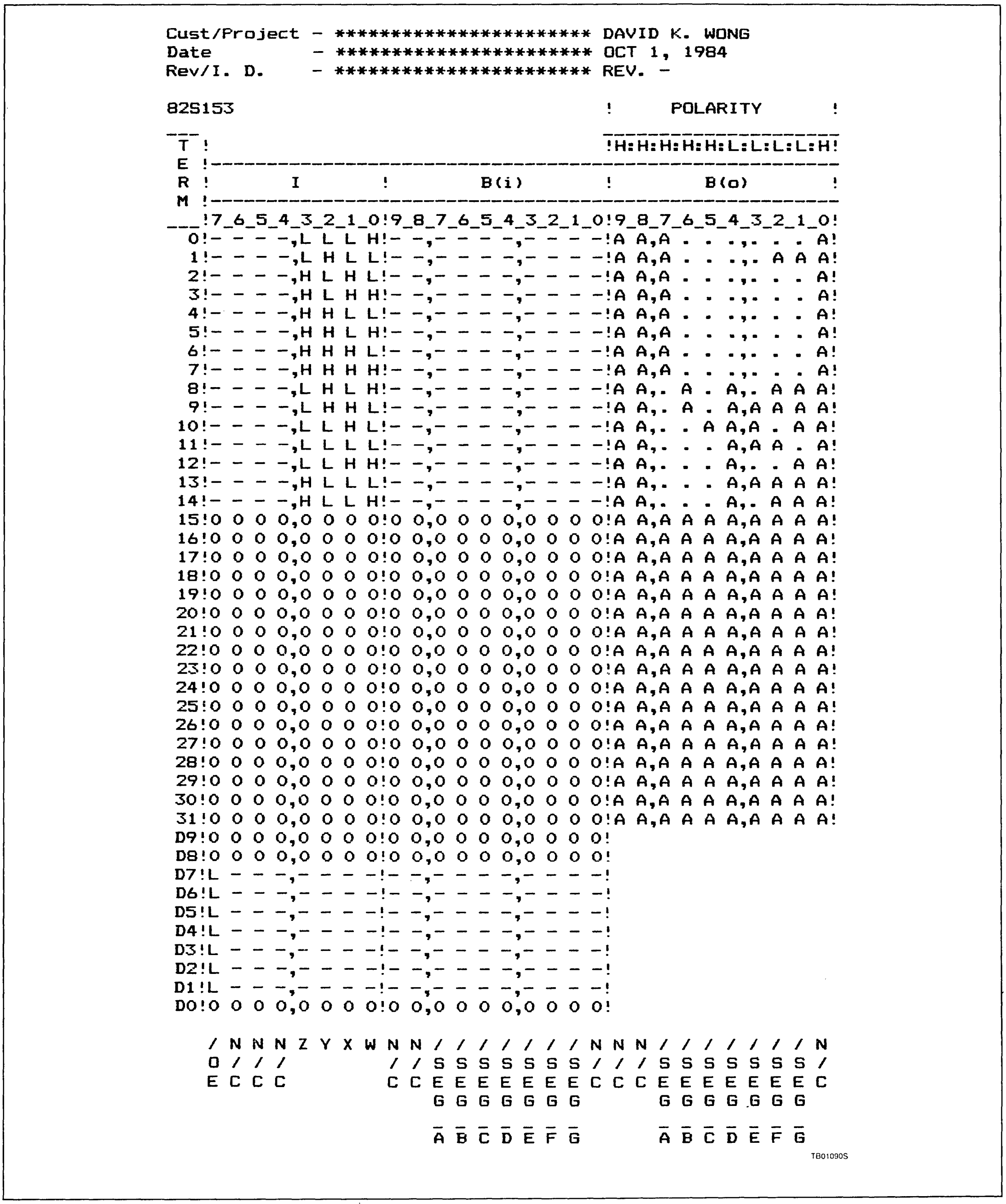
LD01160S

Figure 7. Complement Array — "None of the Above" Detection Circuit

4-Bit Binary-To-7 Segment Decoder

AN10

Table 5. H/L Table for BCD-to-7 Segment Decoder Generated by AMAZE



```
Cust/Project - ************************ DAVID K. WONG
Date         - ************************ OCT 1, 1984
Rev/I. D.    - ************************ REV. -

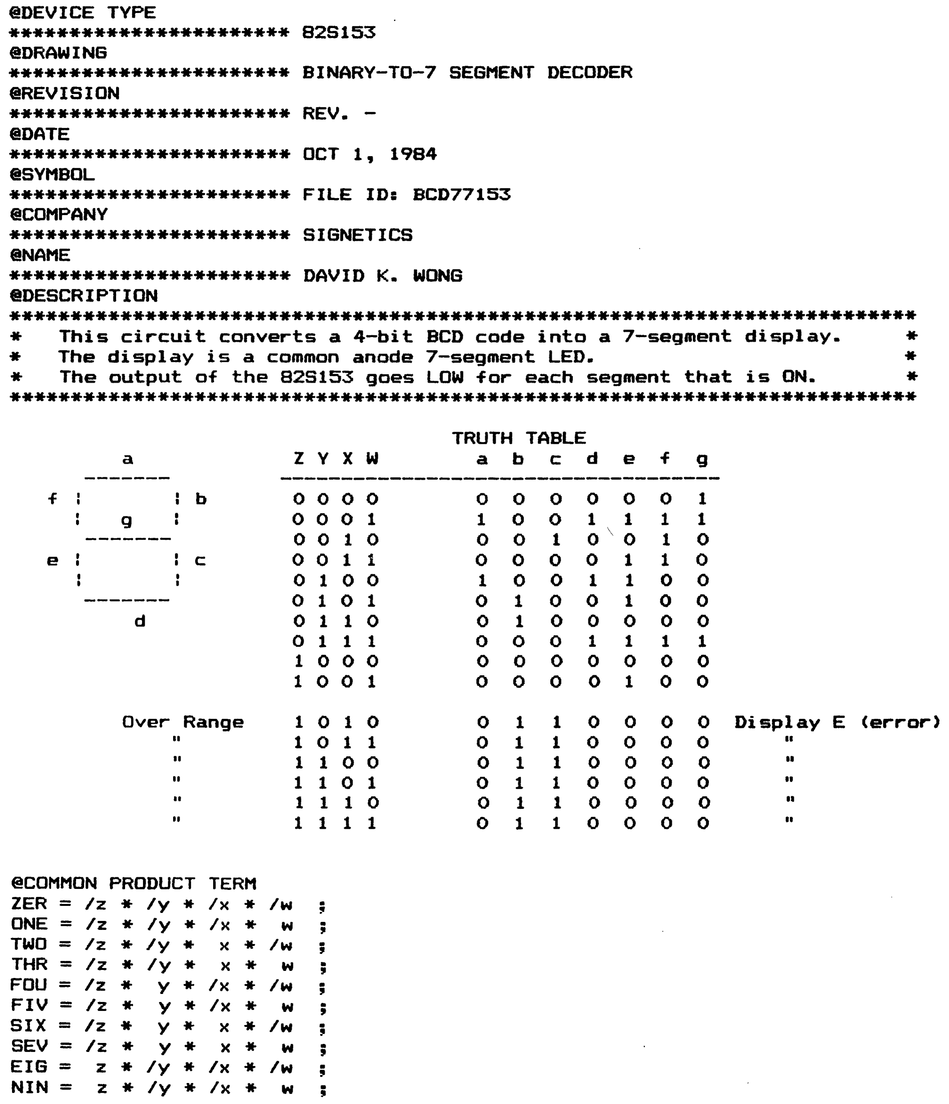
82S153                                 !     POLARITY      !

---                                     ---------------------
 T !                                   !H:H:H:H:H:L:L:L:L:H!
 E !--------------------------------------------------------
 R !       I       !        B(i)        !        B(o)        !
 M !--------------------------------------------------------
___!7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!- - - -,L L L H!- -,- - - -,- - - -!A A,A . . .,. . . A!
  1!- - - -,L H L L!- -,- - - -,- - - -!A A,A . . .,. A A A!
  2!- - - -,H L H L!- -,- - - -,- - - -!A A,A . . .,. . . A!
  3!- - - -,H L H H!- -,- - - -,- - - -!A A,A . . .,. . . A!
  4!- - - -,H H L L!- -,- - - -,- - - -!A A,A . . .,. . . A!
  5!- - - -,H H L H!- -,- - - -,- - - -!A A,A . . .,. . . A!
  6!- - - -,H H H L!- -,- - - -,- - - -!A A,A . . .,. . . A!
  7!- - - -,H H H H!- -,- - - -,- - - -!A A,A . . .,. . . A!
  8!- - - -,L H L H!- -,- - - -,- - - -!A A,. A . A,. A A A!
  9!- - - -,L H H L!- -,- - - -,- - - -!A A,. A . A,A A A A!
 10!- - - -,L L H L!- -,- - - -,- - - -!A A,. . A A,A . A A!
 11!- - - -,L L L L!- -,- - - -,- - - -!A A,. . . A,A A . A!
 12!- - - -,L L H H!- -,- - - -,- - - -!A A,. . . A,. . A A!
 13!- - - -,H L L L!- -,- - - -,- - - -!A A,. . . A,A A A A!
 14!- - - -,H L L H!- -,- - - -,- - - -!A A,. . . A,. A A A!
 15!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 16!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 17!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 18!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 19!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 23!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 25!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 27!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 31!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 D9!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D8!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D7!L - - -,- - - -!- -,- - - -,- - - -!
 D6!L - - -,- - - -!- -,- - - -,- - - -!
 D5!L - - -,- - - -!- -,- - - -,- - - -!
 D4!L - - -,- - - -!- -,- - - -,- - - -!
 D3!L - - -,- - - -!- -,- - - -,- - - -!
 D2!L - - -,- - - -!- -,- - - -,- - - -!
 D1!L - - -,- - - -!- -,- - - -,- - - -!
 D0!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!

    / N N N Z Y X W N N / / / / / / / N N N / / / / / / / N
    O / / /         / / S S S S S S S / / / S S S S S S S /
    E C C C         C C E E E E E E E C C C E E E E E E E C
                        G G G G G G G       G G G G G G G

                        ‾ ‾ ‾ ‾ ‾ ‾ ‾       ‾ ‾ ‾ ‾ ‾ ‾ ‾
                        A B C D E F G       A B C D E F G
                                                         TB01090S
```

4-Bit Binary-To-7 Segment Decoder AN10



```
@DEVICE TYPE
************************ 82S153
@DRAWING
************************ BINARY-TO-7 SEGMENT DECODER
@REVISION
************************ REV. -
@DATE
************************ OCT 1, 1984
@SYMBOL
************************ FILE ID: BCD77153
@COMPANY
************************ SIGNETICS
@NAME
************************ DAVID K. WONG
@DESCRIPTION
******************************************************************************
*   This circuit converts a 4-bit BCD code into a 7-segment display.        *
*   The display is a common anode 7-segment LED.                            *
*   The output of the 82S153 goes LOW for each segment that is ON.          *
******************************************************************************

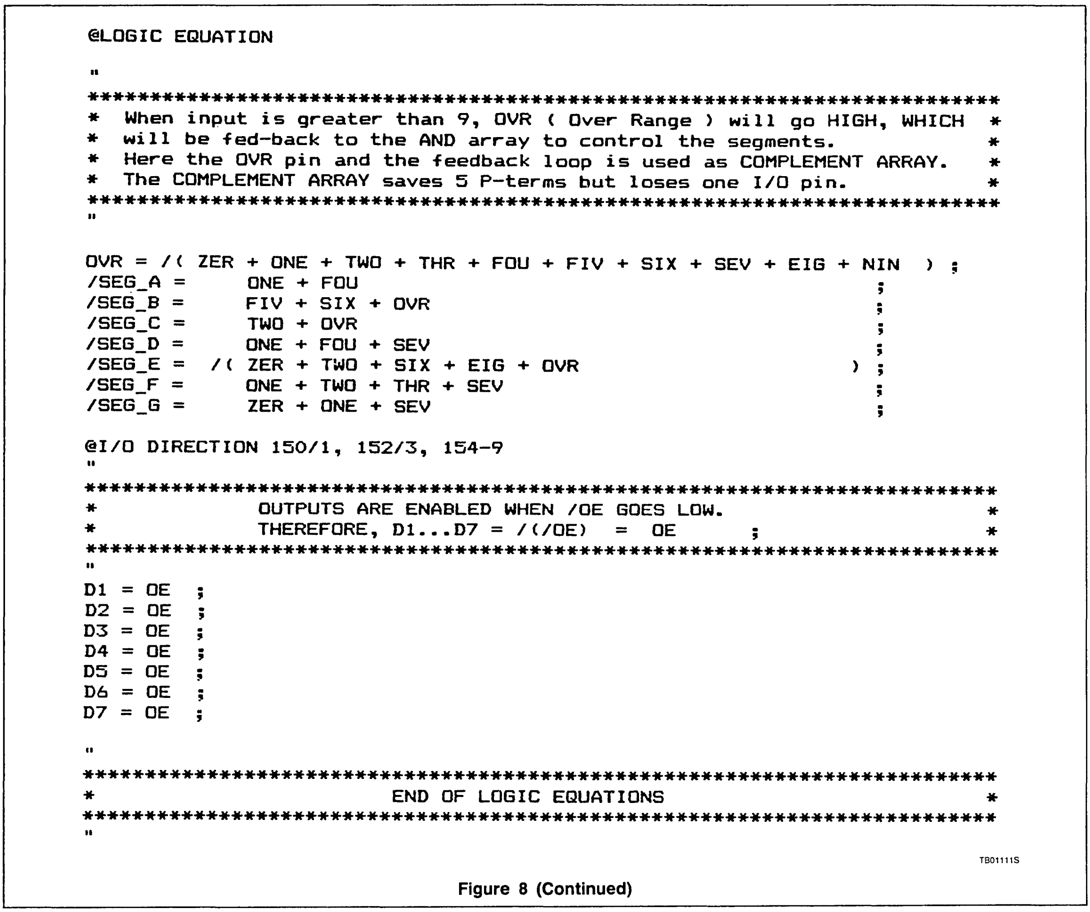
                                            TRUTH TABLE
         a              Z Y X W           a  b  c  d  e  f  g
      -------           ------------------------------------
   f :       : b        0 0 0 0           0  0  0  0  0  0  1
     :   g   :          0 0 0 1           1  0  0  1  1  1  1
      -------           0 0 1 0           0  0  1  0  0  1  0
   e :       : c        0 0 1 1           0  0  0  0  1  1  0
     :       :          0 1 0 0           1  0  0  1  1  0  0
      -------           0 1 0 1           0  1  0  0  1  0  0
         d              0 1 1 0           0  1  0  0  0  0  0
                        0 1 1 1           0  0  0  1  1  1  1
                        1 0 0 0           0  0  0  0  0  0  0
                        1 0 0 1           0  0  0  0  1  0  0

           Over Range   1 0 1 0           0  1  1  0  0  0  0   Display E (error)
                "       1 0 1 1           0  1  1  0  0  0  0          "
                "       1 1 0 0           0  1  1  0  0  0  0          "
                "       1 1 0 1           0  1  1  0  0  0  0          "
                "       1 1 1 0           0  1  1  0  0  0  0          "
                "       1 1 1 1           0  1  1  0  0  0  0          "


@COMMON PRODUCT TERM
ZER = /z * /y * /x * /w  ;
ONE = /z * /y * /x *  w  ;
TWO = /z * /y *  x * /w  ;
THR = /z * /y *  x *  w  ;
FOU = /z *  y * /x * /w  ;
FIV = /z *  y * /x *  w  ;
SIX = /z *  y *  x * /w  ;
SEV = /z *  y *  x *  w  ;
EIG =  z * /y * /x * /w  ;
NIN =  z * /y * /x *  w  ;
```

TB01101S

Figure 8. Boolean Equation for BCD-to-7 Segment Decoder



```
@LOGIC EQUATION

"
*************************************************************************
*  When input is greater than 9, OVR ( Over Range ) will go HIGH, WHICH  *
*  will be fed-back to the AND array to control the segments.           *
*  Here the OVR pin and the feedback loop is used as COMPLEMENT ARRAY.   *
*  The COMPLEMENT ARRAY saves 5 P-terms but loses one I/O pin.          *
*************************************************************************
"

OVR = /( ZER + ONE + TWO + THR + FOU + FIV + SIX + SEV + EIG + NIN  ) ;
/SEG_A =     ONE + FOU                                              ;
/SEG_B =     FIV + SIX + OVR                                        ;
/SEG_C =     TWO + OVR                                              ;
/SEG_D =     ONE + FOU + SEV                                        ;
/SEG_E =  /( ZER + TWO + SIX + EIG + OVR                          ) ;
/SEG_F =     ONE + TWO + THR + SEV                                  ;
/SEG_G =     ZER + ONE + SEV                                        ;

@I/O DIRECTION 150/1, 152/3, 154-9
"
*************************************************************************
*              OUTPUTS ARE ENABLED WHEN /OE GOES LOW.                   *
*              THEREFORE, D1...D7 = /(/OE)  =  OE      ;                *
*************************************************************************
"
D1 = OE  ;
D2 = OE  ;
D3 = OE  ;
D4 = OE  ;
D5 = OE  ;
D6 = OE  ;
D7 = OE  ;

"
*************************************************************************
*                           END OF LOGIC EQUATIONS                      *
*************************************************************************
"
```

TB01111S

Figure 8 (Continued)

Table 6. H/L Table of BCD-to-7 Segment Decoder Generated by AMAZE

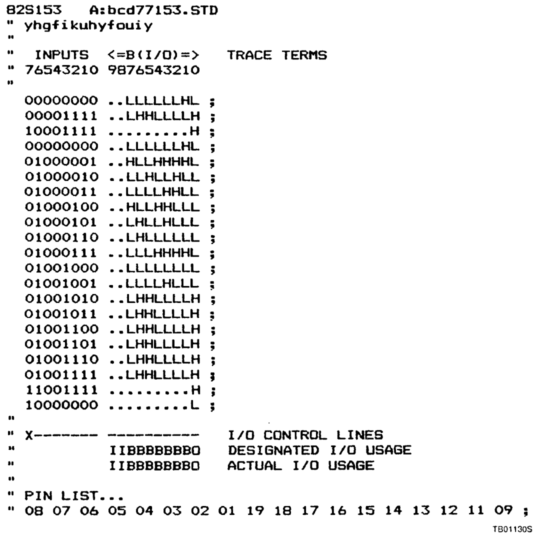
```
Cust/Project - ************************ DAVID K. WONG
Date         - ************************ OCT 1, 1984
Rev/I. D.    - ************************ REV. -

82S153                                 !     POLARITY      !
___                                    _____________________
 T !                                   !H:H:H:H:H:H:L:H:H:L!
 E !--------------------------------------------------------
 R !       I       !        B(i)       !        B(o)       !
 M !--------------------------------------------------------
___!7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!- - - -,L L L L!- -,- - - -,- - - -!A A,. . . .,A . A A!
  1!- - - -,L L L H!- -,- - - -,- - - -!A A,A . . A,. A A A!
  2!- - - -,L L H L!- -,- - - -,- - - -!A A,. . A .,A A . A!
  3!- - - -,L L H H!- -,- - - -,- - - -!A A,. . . .,. A . A!
  4!- - - -,L H L L!- -,- - - -,- - - -!A A,A . . A,. . . A!
  5!- - - -,L H L H!- -,- - - -,- - - -!A A,. A . .,. . . A!
  6!- - - -,L H H L!- -,- - - -,- - - -!A A,. A . .,A . . A!
  7!- - - -,L H H H!- -,- - - -,- - - -!A A,. . . A,. A A A!
  8!- - - -,H L L L!- -,- - - -,- - - -!A A,. . . .,A . . A!
  9!- - - -,H L L H!- -,- - - -,- - - -!A A,. . . .,. . . A!
 10!- - - -,- - - -!- -,- - - -,- - - H!A A,. A A .,A . . .!
 11!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 12!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 13!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 14!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 15!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 16!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 17!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 18!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 19!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 23!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 25!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 27!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 31!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 D9!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D8!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D7!L - - -,- - - -!- -,- - - -,- - - -!
 D6!L - - -,- - - -!- -,- - - -,- - - -!
 D5!L - - -,- - - -!- -,- - - -,- - - -!
 D4!L - - -,- - - -!- -,- - - -,- - - -!
 D3!L - - -,- - - -!- -,- - - -,- - - -!
 D2!L - - -,- - - -!- -,- - - -,- - - -!
 D1!L - - -,- - - -!- -,- - - -,- - - -!
 D0!- - - -,- - - -!- -,- - - -,- - - -!

    / N N N Z Y X W N N / / / / / / / O N N / / / / / / / O
    O / / /         / / S S S S S S S V / / S S S S S S S V
    E C C C         C C E E E E E E E R C C E E E E E E E R
                        G G G G G G G       G G G G G G G

                        _ _ _ _ _ _ _       _ _ _ _ _ _ _
                        A B C D E F G       A B C D E F G
```

TB01120S



```
82S153    A:bcd77153.STD
" yhgfikuhyfouiy
"
"  INPUTS  <=B(I/O)=>   TRACE TERMS
" 76543210 9876543210
"
  00000000 ..LLLLLLHL ;
  00001111 ..LHHLLLLH ;
  10001111 .........H ;
  00000000 ..LLLLLLHL ;
  01000001 ..HLLHHHHL ;
  01000010 ..LLHLLHLL ;
  01000011 ..LLLLHHLL ;
  01000100 ..HLLHHLLL ;
  01000101 ..LHLLHLLL ;
  01000110 ..LHLLLLLL ;
  01000111 ..LLLHHHHL ;
  01001000 ..LLLLLLLL ;
  01001001 ..LLLLHLLL ;
  01001010 ..LHHLLLLH ;
  01001011 ..LHHLLLLH ;
  01001100 ..LHHLLLLH ;
  01001101 ..LHHLLLLH ;
  01001110 ..LHHLLLLH ;
  01001111 ..LHHLLLLH ;
  11001111 .........H ;
  10000000 .........L ;
"
" X------- ----------   I/O CONTROL LINES
"          IIBBBBBBBO   DESIGNATED I/O USAGE
"          IIBBBBBBBO   ACTUAL I/O USAGE
"
" PIN LIST...
" 08 07 06 05 04 03 02 01 19 18 17 16 15 14 13 12 11 09 ;
```

TB01130S

Figure 9. Simulation Results of H/L Table

BCD-To-7 Segment Decoder with Output Latches

Output latches may be constructed by using the bidirectional I/Os of PLS153/153A as shown in Figure 10. When /LE (latch enable) is High, the output equals the input. But when /LE is Low, the output is latched. Changing the input will not effect the output. Segments a and e are used to illustrate the decoding and latch circuit as shown in Figures 11 and 12 which are expressed in H/L format as shown in Table 8. The complete design of the decoder is shown in Figures 13 and 14 and Table 7. With the output latches, the circuit cannot be tri-stated since the tri-state condition will interrupt the feedback path. An alternative approach is shown in Figure 15 where the display is a common cathode, the segment drivers are always on and the duty cycling is implemented with a digit driver which pulls the common cathode of the display to ground as the input "Duty Cycle" goes High. A common practice is to drive the segments with 10 time the desired DC current and drive the digit with a 10% duty cycle pulse. The H/L implementation is as shown in Tables 9 and 10. The "Duty Cycle" control input is generated externally.

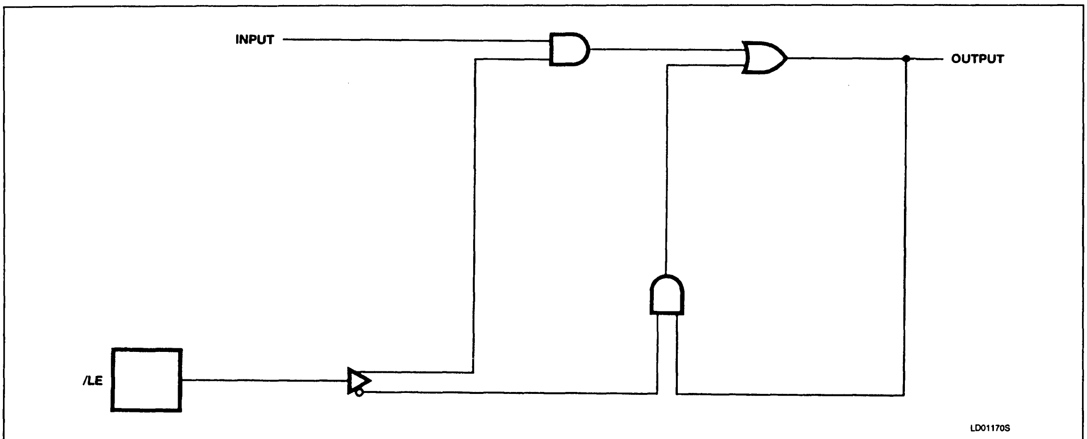


Figure 10. Block Diagram of a Simple D-Latch

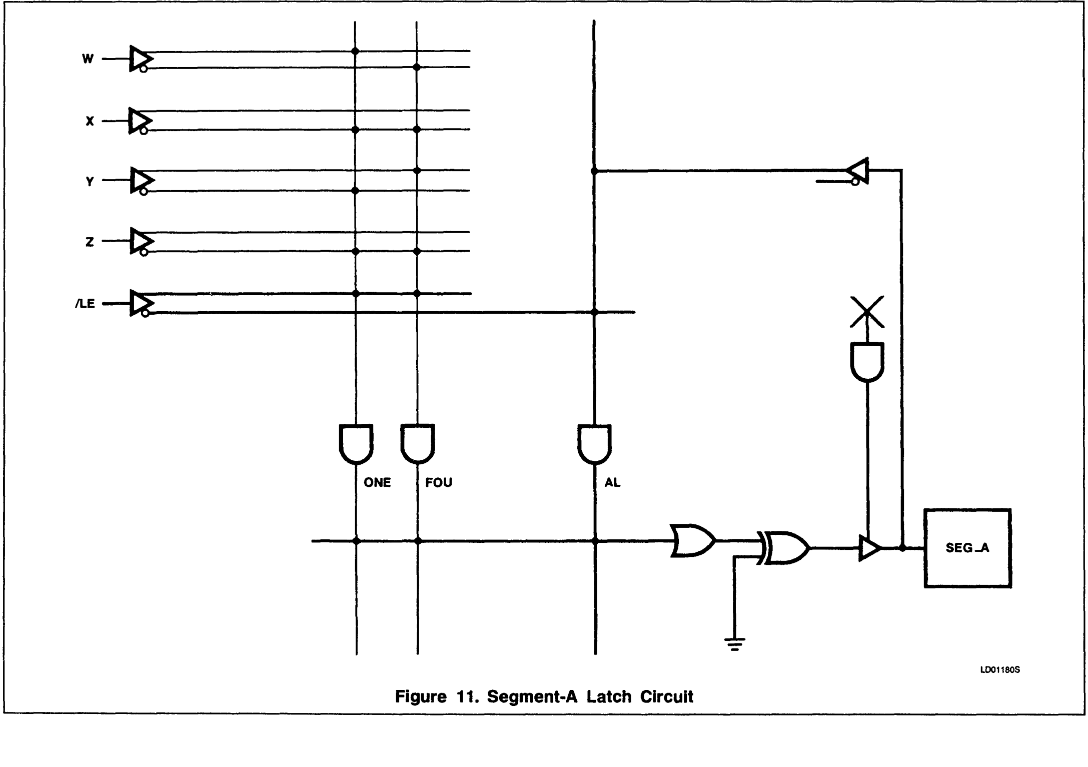


Figure 11. Segment-A Latch Circuit

4-Bit Binary-To-7 Segment Decoder AN10

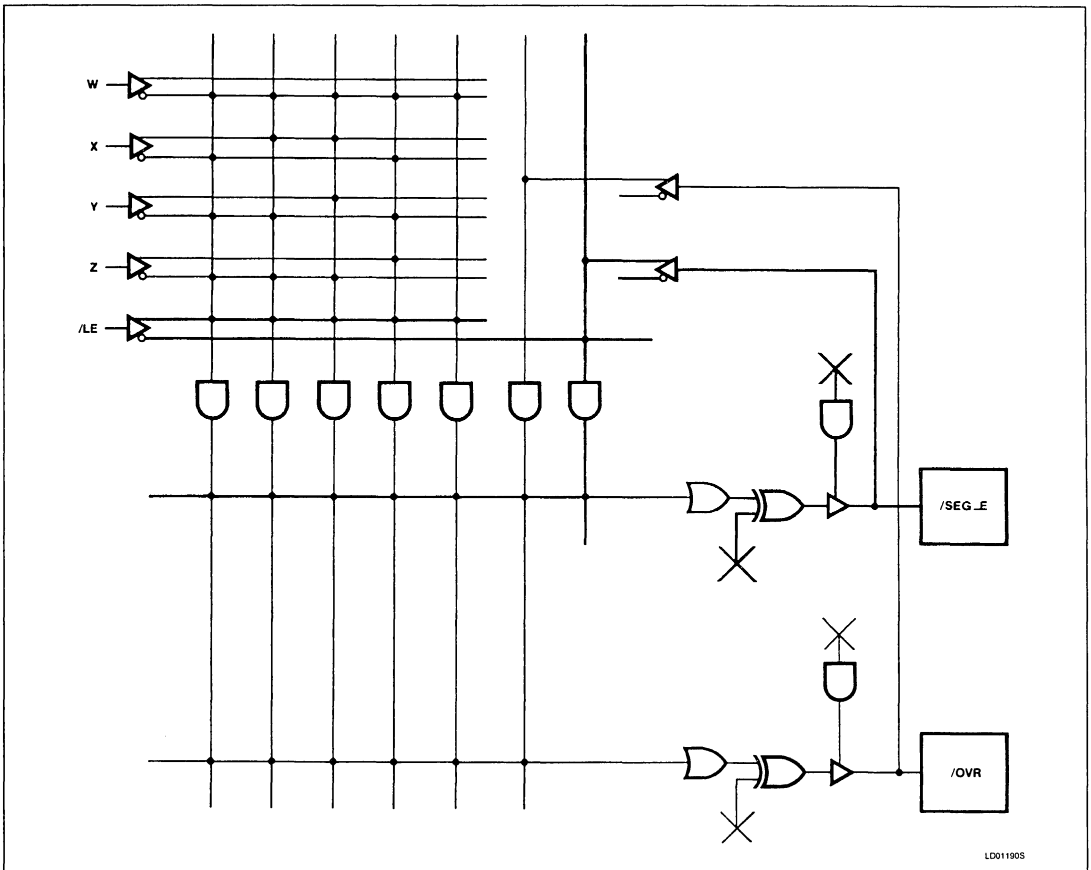
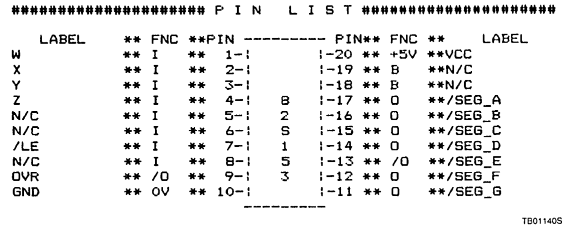


Figure 12. Segment-E Latch



```
####################### P I N   L I S T #######################

   LABEL      ** FNC **PIN ---------- PIN** FNC **     LABEL
W             ** I   **  1-!         !-20 ** +5V **VCC
X             ** I   **  2-!         !-19 ** B   **N/C
Y             ** I   **  3-!         !-18 ** B   **N/C
Z             ** I   **  4-!    8    !-17 ** O   **/SEG_A
N/C           ** I   **  5-!    2    !-16 ** O   **/SEG_B
N/C           ** I   **  6-!    S    !-15 ** O   **/SEG_C
/LE           ** I   **  7-!    1    !-14 ** O   **/SEG_D
N/C           ** I   **  8-!    5    !-13 ** /O  **/SEG_E
OVR           ** /O  **  9-!    3    !-12 ** O   **/SEG_F
GND           ** OV  ** 10-!         !-11 ** O   **/SEG_G
                           ----------
```

TB01140S

Figure 13. Pin List of BCD-to-7 Segment Decoder with Latches

```
@DEVICE TYPE
82S153
@DRAWING
************************ BCD-TO-7 SEGMENT DECODER
@REVISION
************************ REV. -
@DATE
************************ OCT 1, 1984
@SYMBOL
************************ FILE ID: BCD7L153
@COMPANY
************************ SIGNETICS
@NAME
************************ DAVID K. WONG
@DESCRIPTION
*****************************************************************************
*   This circuit converts a 4-bit BCD code into a 7-segment display.      *
*   The display is a common anode 7-segment LED.                           *
*   The output of the 82S153 goes LOW for each segment that is ON.         *
*   The outputs are latched when /LE goes LOW.                             *
*****************************************************************************

                                          TRUTH TABLE
          a               Z Y X W        a   b   c   d   e   f   g
       -------            ---------------------------------------
   f :       : b          0 0 0 0        0   0   0   0   0   0   1
     :   g   :            0 0 0 1        1   0   0   1   1   1   1
       -------            0 0 1 0        0   0   1   0   0   1   0
   e :       : c          0 0 1 1        0   0   0   0   1   1   0
     :       :            0 1 0 0        1   0   0   1   1   0   0
       -------            0 1 0 1        0   1   0   0   1   0   0
          d               0 1 1 0        0   1   0   0   0   0   0
                          0 1 1 1        0   0   0   1   1   1   1
                          1 0 0 0        0   0   0   0   0   0   0
                          1 0 0 1        0   0   0   0   1   0   0

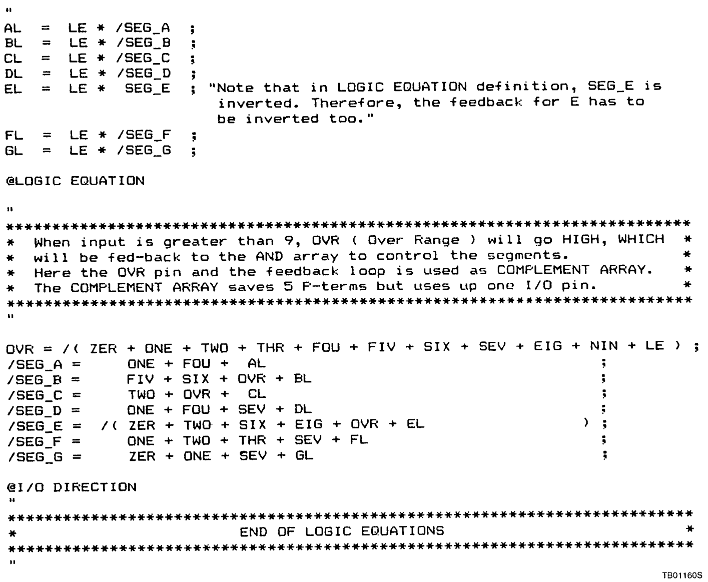
         Over Range       1 0 1 0        0   1   1   0   0   0   0   Display E (error)
             "            1 0 1 1        0   1   1   0   0   0   0        "
             "            1 1 0 0        0   1   1   0   0   0   0        "
             "            1 1 0 1        0   1   1   0   0   0   0        "
             "            1 1 1 0        0   1   1   0   0   0   0        "
             "            1 1 1 1        0   1   1   0   0   0   0        "


@COMMON PRODUCT TERM
ZER = /z * /y * /x * /w * /LE  ;
ONE = /z * /y * /x *  w * /LE  ;
TWO = /z * /y *  x * /w * /LE  ;
THR = /z * /y *  x *  w * /LE  ;
FOU = /z *  y * /x * /w * /LE  ;
FIV = /z *  y * /x *  w * /LE  ;
SIX = /z *  y *  x * /w * /LE  ;
SEV = /z *  y *  x *  w * /LE  ;
EIG =  z * /y * /x * /w * /LE  ;
NIN =  z * /y * /x *  w * /LE  ;

"
*****************************************************************************
*              Feedback circuits to form D-latches.                          *
*****************************************************************************
```

TB01150S

Figure 14. Boolean Equation of BCD-to-7 Segment Decoder with Latches



```
"
AL   =  LE * /SEG_A  ;
BL   =  LE * /SEG_B  ;
CL   =  LE * /SEG_C  ;
DL   =  LE * /SEG_D  ;
EL   =  LE *  SEG_E  ; "Note that in LOGIC EQUATION definition, SEG_E is
                        inverted. Therefore, the feedback for E has to
                        be inverted too."
FL   =  LE * /SEG_F  ;
GL   =  LE * /SEG_G  ;

@LOGIC EQUATION

"
***************************************************************************
*  When input is greater than 9, OVR ( Over Range ) will go HIGH, WHICH  *
*  will be fed-back to the AND array to control the segments.            *
*  Here the OVR pin and the feedback loop is used as COMPLEMENT ARRAY.   *
*  The COMPLEMENT ARRAY saves 5 P-terms but uses up one I/O pin.         *
***************************************************************************
"

OVR = /( ZER + ONE + TWO + THR + FOU + FIV + SIX + SEV + EIG + NIN + LE ) ;
/SEG_A =      ONE + FOU +  AL                                       ;
/SEG_B =      FIV + SIX + OVR + BL                                  ;
/SEG_C =      TWO + OVR +  CL                                       ;
/SEG_D =      ONE + FOU + SEV + DL                                  ;
/SEG_E =  /( ZER + TWO + SIX + EIG + OVR + EL                     ) ;
/SEG_F =      ONE + TWO + THR + SEV + FL                            ;
/SEG_G =      ZER + ONE + SEV + GL                                  ;

@I/O DIRECTION
"
***************************************************************************
*                          END OF LOGIC EQUATIONS                         *
***************************************************************************
"
```

TB01160S

Figure 14 (Continued)

Table 7. H/L Table of BCD-to-7 Segment Decoder with Latches

```
Cust/Project - *********************** DAVID K. WONG
Date         - *********************** OCT 1, 1984
Rev/I. D.    - *********************** REV. -

82S153                                 !      POLARITY       !
___                                     ---------------------
 T !                                   !H:H:H:H:H:H:L:H:H:L!
 E !---------------------------------------------------------
 R !       I       !        B(i)       !        B(o)        !
 M !---------------------------------------------------------
___!7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!- H - -,L L L L!- -,- - - -,- - - -!A A,. . . .,A . A A!
  1!- H - -,L L L H!- -,- - - -,- - - -!A A,A . . A,. A A A!
  2!- H - -,L L H L!- -,- - - -,- - - -!A A,. . A .,A A . A!
  3!- H - -,L L H H!- -,- - - -,- - - -!A A,. . . .,. A . A!
  4!- H - -,L H L L!- -,- - - -,- - - -!A A,A . . A,. . . A!
  5!- H - -,L H L H!- -,- - - -,- - - -!A A,. A . .,. . . A!
  6!- H - -,L H H L!- -,- - - -,- - - -!A A,. A . .,A . . A!
  7!- H - -,L H H H!- -,- - - -,- - - -!A A,. . . A,. A A A!
  8!- H - -,H L L L!- -,- - - -,- - - -!A A,. . . .,A . . A!
  9!- H - -,H L L H!- -,- - - -,- - - -!A A,. . . .,. . . A!
 10!- L - -,- - - -!- -,- - - -,- - - -!A A,. . . .,. . . A!
 11!- L - -,- - - -!- -,H - - -,- - - -!A A,A . . .,. . . .!
 12!- - - -,- - - -!- -,- - - -,- - - H!A A,. A A .,A . . .!
 13!- L - -,- - - -!- -,- H - -,- - - -!A A,. A . .,. . . .!
 14!- L - -,- - - -!- -,- - H -,- - - -!A A,. . A .,. . . .!
 15!- L - -,- - - -!- -,- - - H,- - - -!A A,. . . A,. . . .!
 16!- L - -,- - - -!- -,- - - -,L - - -!A A,. . . .,A . . .!
 17!- L - -,- - - -!- -,- - - -,- H - -!A A,. . . .,. A . .!
 18!- L - -,- - - -!- -,- - - -,- - H -!A A,. . . .,. . A .!
 19!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 23!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 25!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 27!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 31!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 D9!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D8!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!
 D7!- - - -,- - - -!- -,- - - -,- - - -!
 D6!- - - -,- - - -!- -,- - - -,- - - -!
 D5!- - - -,- - - -!- -,- - - -,- - - -!
 D4!- - - -,- - - -!- -,- - - -,- - - -!
 D3!- - - -,- - - -!- -,- - - -,- - - -!
 D2!- - - -,- - - -!- -,- - - -,- - - -!
 D1!- - - -,- - - -!- -,- - - -,- - - -!
 D0!- - - -,- - - -!- -,- - - -,- - - -!

    N / N N Z Y X W N N / / / / / / / O N N / / / / / / / O
    / L / /         / / S S S S S S S V / / S S S S S S S V
    C E C C         C C E E E E E E E R C C E E E E E E E R
                        G G G G G G G       G G G G G G G

                        _ _ _ _ _ _ _       _ _ _ _ _ _ _
                        A B C D E F G       A B C D E F G
```

TB01170S

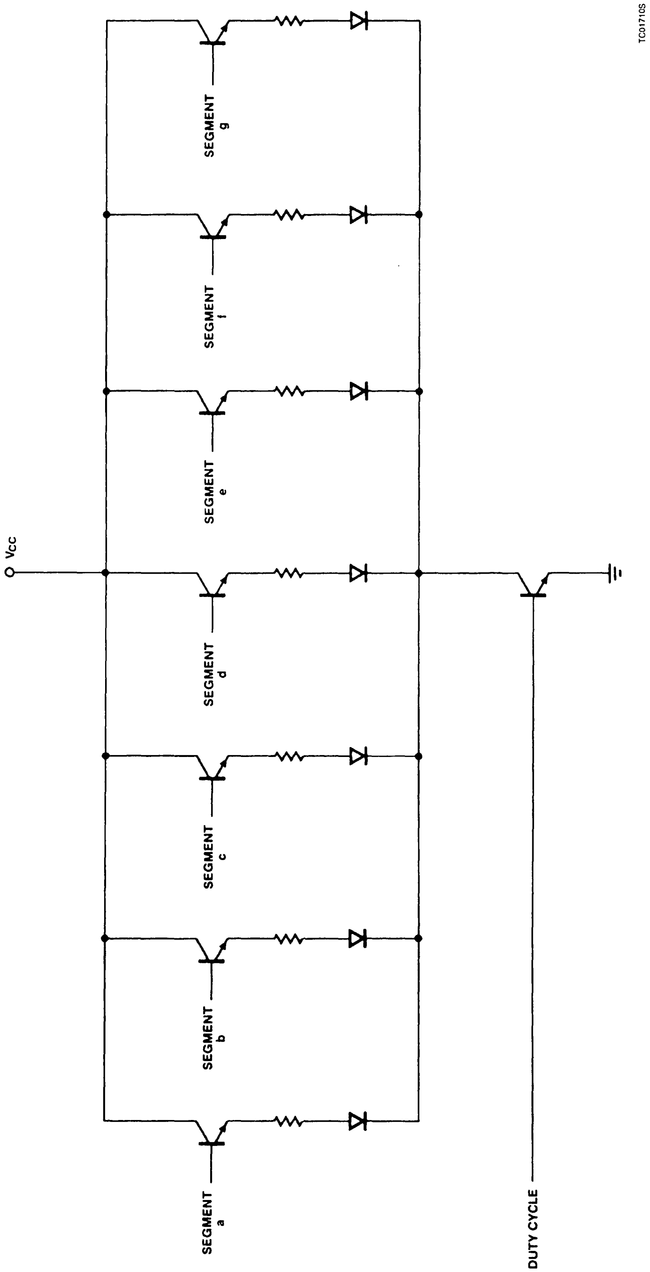
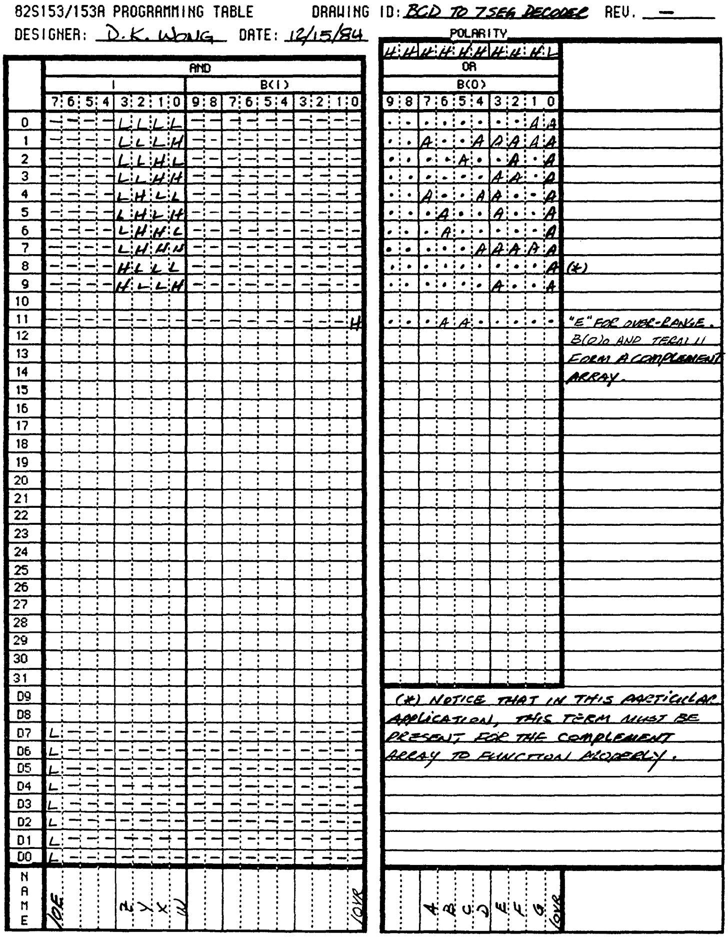


Figure 15. Segment Drivers and Digit Driver

4-Bit Binary-To-7 Segment Decoder

AN10

Table 8. BCD-to-7 Segment Decoder Using Complement Array



82S153/153A PROGRAMMING TABLE DRAWING ID: BCD TO 7SEG DECODER REV. —

DESIGNER: D.K. WONG DATE: 12/15/84

																				POLARITY									
																			H	H	H	H	H	H	H	H	H	L	
	AND																		OR										
	I								B(I)										B(O)										
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	
0	-	-	-	-	L	L	L	L	-	-	-	-	-	-	-	-	-	-	·	·	·	·	·	·	·	·	A	A	
1	-	-	-	-	L	L	L	H	-	-	-	-	-	-	-	-	-	-	·	·	A	·	·	A	A	A	A	A	
2	-	-	-	-	L	L	H	L	-	-	-	-	-	-	-	-	-	-	·	·	·	·	A	·	·	A	·	A	
3	-	-	-	-	L	L	H	H	-	-	-	-	-	-	-	-	-	-	·	·	·	·	·	·	A	A	·	A	
4	-	-	-	-	L	H	L	L	-	-	-	-	-	-	-	-	-	-	·	·	A	·	·	A	A	·	·	A	
5	-	-	-	-	L	H	L	H	-	-	-	-	-	-	-	-	-	-	·	·	·	A	·	·	A	·	·	A	
6	-	-	-	-	L	H	H	L	-	-	-	-	-	-	-	-	-	-	·	·	·	A	·	·	·	·	·	A	
7	-	-	-	-	L	H	H	H	-	-	-	-	-	-	-	-	-	-	·	·	·	·	·	A	A	A	A	A	
8	-	-	-	-	H	L	L	L	-	-	-	-	-	-	-	-	-	-	·	·	·	·	·	·	·	·	·	A	(*)
9	-	-	-	-	H	L	L	H	-	-	-	-	-	-	-	-	-	-	·	·	·	·	·	·	A	·	·	A	
10																													
11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	·	·	·	A	A	·	·	·	·	·	"E" FOR OVER-RANGE.
12																													B(O)0 AND TERM 11
13																													FORM A COMPLEMENT
14																													ARRAY.
15																													
16																													
17																													
18																													
19																													
20																													
21																													
22																													
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26																													
27																													
28																													
29																													
30																													
31																													
D9																													(*) NOTICE THAT IN THIS PARTICULAR
D8																													APPLICATION, THIS TERM MUST BE
D7	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											PRESENT FOR THE COMPLEMENT
D6	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											ARRAY TO FUNCTION PROPERLY.
D5	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D4	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D3	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D2	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D1	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D0	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
NAME	/OE				Z	Y	X	W										/OVR			A	B	C	D	E	F	G	/OVR	

TB01180S

4-Bit Binary-To-7 Segment Decoder

Table 9. Segments A and E with Latches

82S153/153A PROGRAMMING TABLE DRAWING ID:________ REV. ____

DESIGNER: ________ DATE: ________

																				POLARITY									
																						H	H	H	H	L	H	H	L	
	AND																			OR									
	I								B(I)										B(O)										
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	
0	H	-	-	-	L	L	L	H	-	-	-	-	-	-	-	-	-	-			A								$\overline{A}$ = LE * W * $\overline{X}$ * $\overline{Y}$ * $\overline{Z}$
1	H	-	-	-	L	H	L	L	-	-	-	-	-	-	-	-	-	-			A								+ LE * $\overline{W}$ * $\overline{X}$ * Y * $\overline{Z}$
2	L	-	-	-	-	-	-	-	-	-	H	-	-	-	-	-	-	-			A								+ $\overline{LE}$ * A
3																													
4																													
5	H	-	-	-	L	L	L	L	-	-	-	-	-	-	-	-	-	-							A				E = LE * $\overline{W}$ * $\overline{X}$ * $\overline{Y}$ * $\overline{Z}$
6	H	-	-	-	L	L	H	L	-	-	-	-	-	-	-	-	-	-							A				+ LE * $\overline{W}$ * $\overline{X}$ * Y * $\overline{Z}$
7	H	-	-	-	L	H	H	L	-	-	-	-	-	-	-	-	-	-							A				+ LE * $\overline{W}$ * X * Y * $\overline{Z}$
8	H	-	-	-	H	L	L	L	-	-	-	-	-	-	-	-	-	-							A				+ LE * W * $\overline{X}$ * $\overline{Y}$ * $\overline{Z}$
9	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H							A				+ LE * OVR
10	L	-	-	-	-	-	-	-	-	-	-	-	-	-	L	-	-	-							A				+ $\overline{LE}$ * $\overline{E}$
11																													
12																												A	OVR = 1 IF INPUT ≠ 0-9
13																													
14																													
15																													
16																													
17																													
18																													
19																													
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30																													
31																													
D9																													
D8																													
D7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D6																													
D5																													
D4																													
D3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
D2																													
D1																													
D0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-											
NAME	LE				Z	Y	X	W			A				E			OVR			A				E			OVR	

TB01191S

4-Bit Binary-To-7 Segment Decoder

Table 10. H/L Table of BCD-to-7 Segment Decoder with Latches with Outputs Active-High

82S153/153A PROGRAMMING TABLE DRAWING ID: BCD7LM REV. –

DESIGNER: D.K. WONG DATE: 12/26/84

	AND																		OR										
	I								B(I)										B(O)										
																			POLARITY		L	L	L	L	L	L	L	L	
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	
0	–	H	–	–	L	L	L	L	–	–	–	–	–	–	–	–	–	–			·	·	·	·	·	·	A	A	0
1	–	H	–	–	L	L	L	H	–	–	–	–	–	–	–	–	–	–			A	·	·	A	A	A	A	A	1
2	–	H	–	–	L	L	H	L	–	–	–	–	–	–	–	–	–	–			·	·	A	·	·	A	·	A	2
3	–	H	–	–	L	L	H	H	–	–	–	–	–	–	–	–	–	–			·	·	·	·	A	A	·	A	3
4	–	H	–	–	L	H	L	L	–	–	–	–	–	–	–	–	–	–			A	·	·	A	A	·	·	A	4
5	–	H	–	–	L	H	L	H	–	–	–	–	–	–	–	–	–	–			·	A	·	·	A	·	·	A	5
6	–	H	–	–	L	H	H	L	–	–	–	–	–	–	–	–	–	–			·	A	·	·	·	·	·	A	6
7	–	H	–	–	L	H	H	H	–	–	–	–	–	–	–	–	–	–			·	·	·	A	A	A	A	A	7
8	–	H	–	–	H	L	L	L	–	–	–	–	–	–	–	–	–	–			·	·	·	·	·	·	·	A	8
9	–	H	–	–	H	L	L	H	–	–	–	–	–	–	–	–	–	–			·	·	·	·	A	·	·	A	9
10																													
11	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	H			·	A	A	·	·	·	·	·	E (ERROR)
12																													
13	–	L	–	–	–	–	–	–	–	–	L	–	–	–	–	–	–	–			A	·	·	·	·	·	·	·	SEG A LATCH
14	–	L	–	–	–	–	–	–	–	–	–	L	–	–	–	–	–	–			·	A	·	·	·	·	·	·	" B "
15	–	L	–	–	–	–	–	–	–	–	–	–	L	–	–	–	–	–			·	·	A	·	·	·	·	·	" C "
16	–	L	–	–	–	–	–	–	–	–	–	–	–	L	–	–	–	–			·	·	·	A	·	·	·	·	" D "
17	–	L	–	–	–	–	–	–	–	–	–	–	–	–	L	–	–	–			·	·	·	·	A	·	·	·	" E "
18	–	L	–	–	–	–	–	–	–	–	–	–	–	–	–	L	–	–			·	·	·	·	·	A	·	·	" F "
19	–	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–	L	–			·	·	·	·	·	·	A	·	" G "
20																													
21																													
22																													
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28																													
29																													
30																													
31																													
D9																													
D8																													
D7	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
D6	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
D5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
D4	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
D3	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
D2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
D1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
D0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–											
NAME		/LE			Z	Y	X	W										OVR			A	B	C	D	E	F	G	OVR	

ALL OUTPUT POLARITIES ARE INVERTED SO THAT AN "A" CAUSES A "LOW" OUTPUT, A "·" CAUSES A "HIGH" OUTPUT.

SINCE ALL OUTPUTS ARE INVERTED, THE FEEDBACK CIRCUITS FOR THE LATCHES ARE ALSO INVERTED

THE OVR OUTPUT CREATES THE "ERROR" DISPLAY IF INPUT ≠ (0 TO 9)

TB01200S

Signetics

Application Specific Products

AN11
PLD Programmable Retriggerable One-Shot

Application Note

Author: David Wong

FEATURES

- **Programmable pulse-width/delay**
- **Maximum 256 clock cycles**
- **Asynchronous TRIGGER input**
- **Active-High and Active-Low outputs**
- **Asynchronous RESET**
- **20-pin package**

THEORY OF OPERATION

The one-shot consists of an FPLS PLS159 and an external clock which may be part of the system in which this one-shot is to work. As shown in Figure 1 and Table 1 the FPLS is configured to have a latch and an eight-bit binary up counter which is presettable by input data to any number less than 256. Since the input data is inverted before it is loaded into the registers, counting from the complements of the input to FF will give the correct number of counts as counting from the input down to 00.

Pulse-width/delay inputs may be the outputs of another device or switches. When /RESET goes Low, flip-flops are set to all 1's (terms PB and PA). At the rising edge of the next clock, data is latched into the registers (terms LB and LA). When /TRIG goes Low, it is latched into the input latch formed by term # 0, 1, 2 and 13. The output O_1 of the latch goes High and O_2 goes Low which enables the 8-bit counting cycle. The O_1 and $/O_1$ will maintain their output levels until the end of the counting cycle at which time the counter reaches the count FF, resets the latch by term # 13, and sets O_2 High. At the rising edge of the next clock, terms LA and LB cause data to be loaded again into the registers, and the device is ready for another /TRIG input. The output wave-forms are illustrated in Figure 2.

If the /TRIG pulse-width is longer than the desired pulse-width of the one-shot, the device will react as mentioned above, and at the end of the count cycle new data will be loaded, another count cycle begins while the outputs remain set by the /TRIG input without changing throughout the change-over of one count cycle to another. O_{1a}, on the other hand, will go Low for one clock period at the change-over. As long as the /TRIG is Low, O_{1a} will continue to pulse Low for one clock period at the change-over of one count cycle to another. The output O_2 will pulse High for one clock cycle at the change-over. Figure 2 illustrates output wave-forms for both cases. The output wave-forms are as illustrated in Figure 2.

The one-shot is implemented by programming the PLS159 as shown in Table 1. The logic representation of the program is shown in Figure 3.

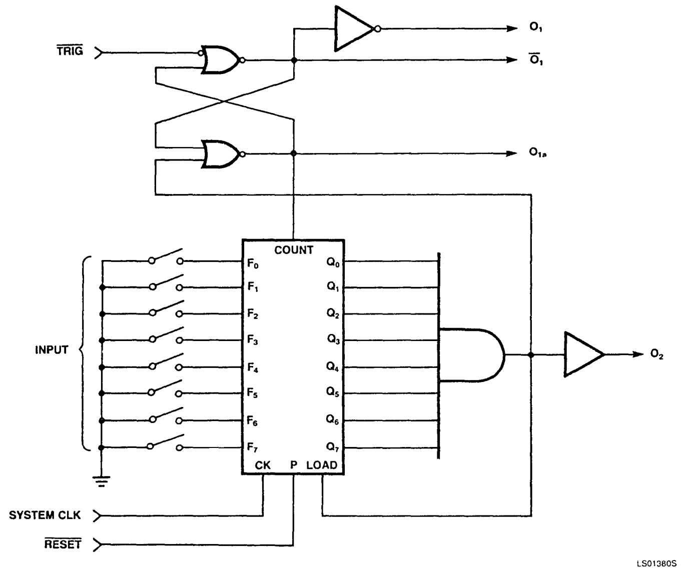

Figure 1. Programmable Retriggerable One-Shot

PLD Programmable Retriggerable One-Shot — AN11

Table 1. PLS159 FPLS Program Table

PROGRAMMABLE RETRIGGERABLE ONE-SHOT

											FF MODE									E								POLARITY				
											A	A	A	A	A	A	A	A		—				—				L	L	H	H	
	TERM	AND																	REMARK	(OR)												REMARK
		C	I				B(I)				Q(P)									Q(N)								B(O)				
			3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
	0	–	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	LATCH	–	–	–	–	–	–	–	–	A	●	●	A	$B_0 = \overline{B_3}$
	1	–	–	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	"	–	–	–	–	–	–	–	–	A	●	●	A	
	2	–	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	"	–	–	–	–	–	–	–	–	●	A	●		
	3																															
	4	–	–	–	H	–	–	H	–	–	–	–	–	–	–	–	–	–	COUNT CYCLE	–	–	–	–	–	–	–	0	●	●	●	●	
	5	–	–	–	H	–	–	H	–	–	–	–	–	–	–	–	–	H		–	–	–	–	–	–	0	–	●	●	●	●	
	6	–	–	–	H	–	–	H	–	–	–	–	–	–	–	–	H	H		–	–	–	–	–	0	–	–	●	●	●	●	
	7	–	–	–	H	–	–	H	–	–	–	–	–	–	–	H	H	H		–	–	–	–	0	–	–	–	●	●	●	●	
	8	–	–	–	H	–	–	H	–	–	–	–	–	–	H	H	H	H		–	–	–	0	–	–	–	–	●	●	●	●	
	9	–	–	–	H	–	–	H	–	–	–	–	–	H	H	H	H	H		–	–	0	–	–	–	–	–	●	●	●	●	
	0	–	–	–	H	–	–	H	–	–	–	–	H	H	H	H	H	H		–	0	–	–	–	–	–	–	●	●	●	●	
	11	–	–	–	H	–	–	H	–	–	–	H	H	H	H	H	H	H		0	–	–	–	–	–	–	–	●	●	●	●	
	12																															
	13	–	–	–	–	–	–	–	–	–	H	H	H	H	H	H	H	H	LATCH	–	–	–	–	–	–	–	–	●	A	A	●	
	14																															
	15																															
	16																															
	17																															
	18																															
	19																															
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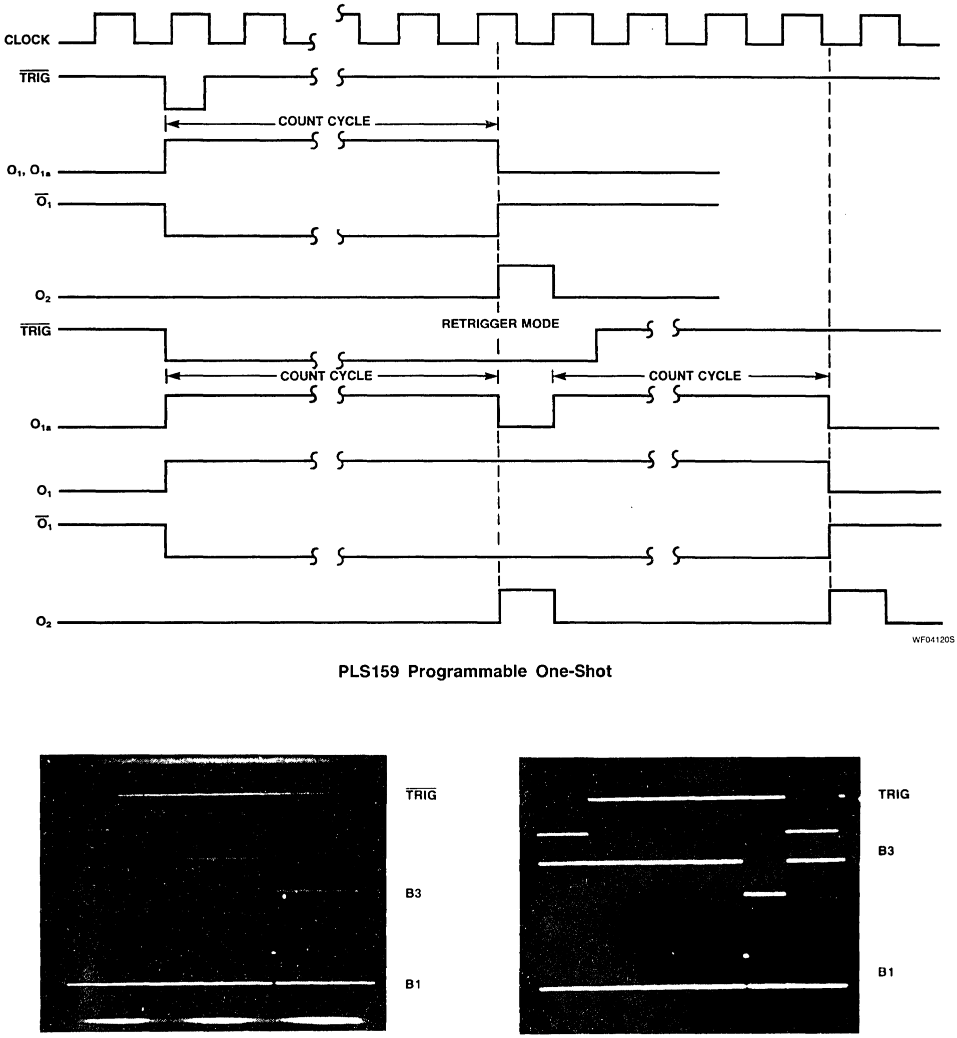
	25																															
	26																															
	27																															
	28																															
	29																															
	30																															
	31																															
2	F_C																															
3	P_B	–	–	–	L	–	–	–	–	–	–	–	–	–	–	–	–	–	SET Q4 TO Q7 HIGH													
4	R_B																															
5	L_B	–	–	–	–	–	–	–	–	–	H	H	H	H	H	H	H	H	LOAD DATA AT NEXT CK													
6	P_A	–	–	–	L	–	–	–	–	–	–	–	–	–	–	–	–	–	SET Q0 TO Q3 HIGH													
7	R_A																															
8	L_A	–	–	–	–	–	–	–	–	–	H	H	H	H	H	H	H	H	LOAD DATA AT NEXT CK													
9	D3	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
0	D2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
1	D1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
2	D0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
	PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12														
	NAMES		/TRIG		/RESET		O1a	/O1	O2	O1																						

TB00421S

COMMENTS:
This one-shot will load data at the end of the count cycle. If $\overline{\text{TRIG}}$ pulse-width is longer than the count cycle, output B3 will go Low for one clock period and go High again for another count cycle. Outputs B_2 and B_0 stay Low and High respectively until $\overline{\text{TRIG}}$ goes High and count cycle is completed without interruption.



PLS159 Programmable One-Shot

Figure 2. Timing Diagram of Programmable Retriggerable One-Shot

PLD Programmable Retriggerable One-Shot

AN11

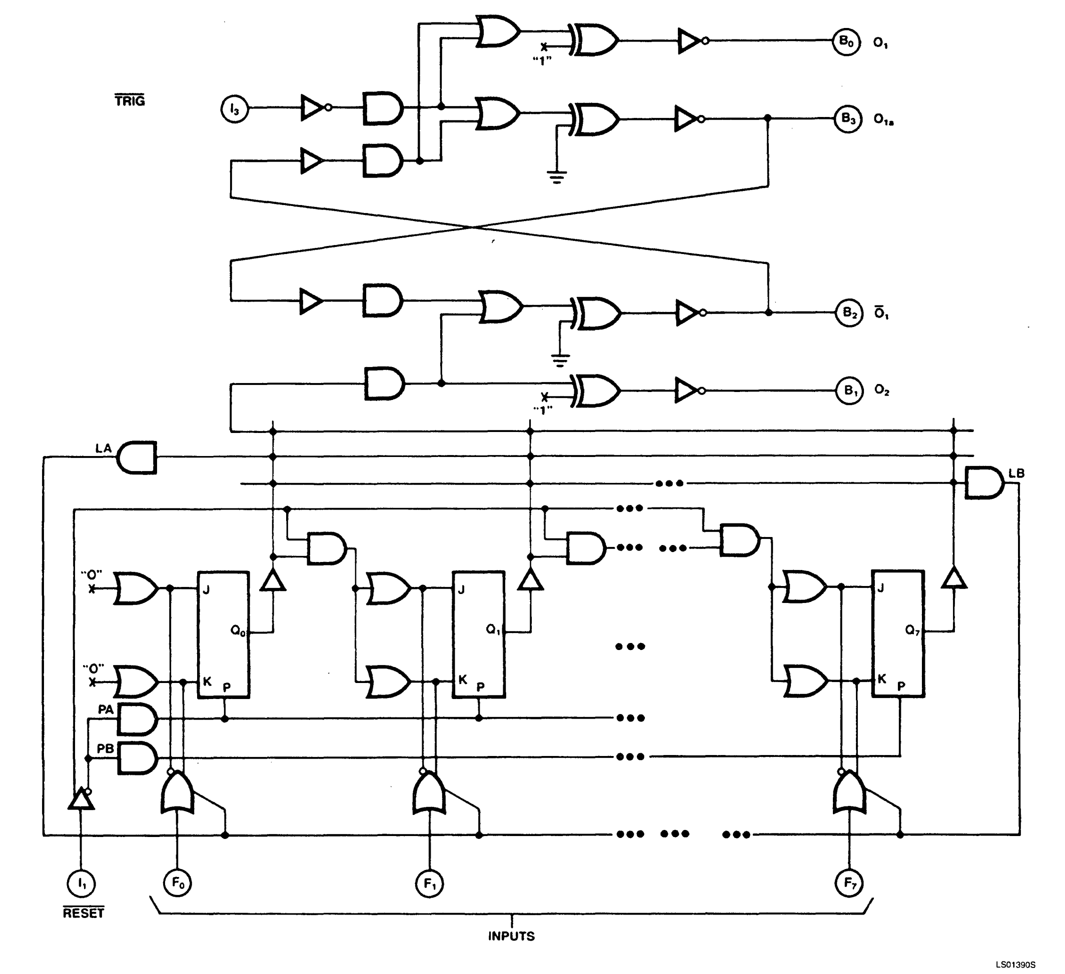


Figure 3. Logic Representation of Table 1

Signetics

AN13
Oscillator With PLS159

Application Note

Application Specific Products

INTRODUCTION

The Field-Programmable Logic Sequencer PLS159 may be a self-contained system except that it requires a system clock which is generally provided by an external source. Using a simple R-C network, two bidirectional I/O pins, one can make a simple oscillator which can provide a clock frequency up to 7MHz (typical) with a pulse width of about 75ns. The frequency of oscillation is set by adjusting the RC network, or by adjusting a reference voltage, V. The circuit is shown in Figure 1. This circuit may be used to clock the flip flops on the same chip, or provide a clock for a bigger system. While this circuit uses only two AND-terms and one control term, the rest of the chip may be used for other circuits.

Initially, the capacitor has zero charge and thus is at zero volt. Output is also at a Low, which disables the tri-state buffer. As the capacitor is being charged up, its voltage increases. At about 1.6V, the non-inverting input buffer begins to turn on. One propagation delay later, the output goes High, which enables the tri-state buffer after another propagation delay. Since the tri-state buffer is unconditionally programmed to a Low, it begins to discharge the capacitor at a fast rate. As the input voltage to the non-inverting buffer drops below 1.6V, the buffer begins to change state. One propagation delay later, output goes Low, which disables the tri-state buffer after another propagation delay. The R-C network is ready to start all over again.

To implement this circuit, we first choose B_1 to input voltage from the RC network and B_0 to be the output pin. As shown in Table 1, we enable the output $B(O)_0$ by "dashing out" the AND-term D_0, make the output non-inverting by programming POLARITY "H" and connect it to term-0 by entering an A in column $B(O)_0$ term-0. We then program an H in $B(I)_1$, term-0 to connect the non-inverting input of B_1 to term-0. Since we don't need the rest of the inputs and outputs, we "dash out" all other input entries and "dot out" all unused outputs in term-0. To create a Low output on $B(O)_1$, we may either have a Low input on the OR and have the output non-inverted, or have a High on the input of OR and have the output inverted to produce a Low. We will arbitrarily use the second method. Here we dash out all inputs and outputs in term-1 except $B(O)_1$ which is programmed an A. We then program the POLARITY of $B(O)_1$ "L" to be inverting.

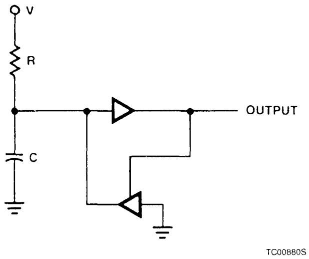


Figure 1. R-C Network Circuit

Finally we program an H in $B(I)_0$ and term-D_1 and dash out all unused inputs so that when $B(O)_0$ becomes High, D_1 will enable the output buffer $B(O)_1$. The program is further illustrated by Figure 2.

Since the High output pulsewidth is about two propagation delays of B_1 to B_0, it is wide enough to drive the clock input of the PLS159. If a square wave is desired, one of the flip flops may be programmed to toggle, as shown in Table 1, term-4, in which case the output frequency of the square wave is half that of $B(O)_0$.

The stability of the output frequency can be controlled by:

1. Making V a stable voltage source,
2. making the charging current of the RC network much greater than the input current of $B(I)_1$ (see Figure 4 for input current characteristics),
3. making the period of oscillation much greater than four times the internal propagation delay (typical $t_{PD} = 35ns$).

Recommendations:

a) Use capacitance less than 500pf.

b) Choose R such that $V/R >> I_{IL}$ (since $I_{IL} = -100\mu A$, worst case, over temperature range, V/R may be 1mA, for example).

The recommendations above put a limit to the range of frequency which the PLS159 may operate in exchange for stable operating frequency. One may extend its range by reducing C to zero (remove the capacitor) and thus operate the circuit at its maximum frequency, or increase the resistance to infinite (remove the resistor), and let the external capacitor be charged by the input current I_{IL}, which gives a much lower frequency.

Table 1. PLS159 FPLS Program Table

CODE NO.										FF MODE									E_B				E_A				POLARITY				
																													L	H	
TERM	AND																	REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	–	–	–	–	–	–	–	H	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	•	•	•	A	$B_0 = B_I$
1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	•	•	A	•	$B_{(0)-I}$ =LOW
2																															
3																															
4	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	O	•	•	•	•	SQUARE WAVE
5																															SEE COMMENT #2
6																															
7																															
8																															
9																															
10																															
11																															
12																															
13																															
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28																															
29																															
30																															
31																															
FC																															
PB																															
RB																															
LB																															
PA																															
RA																															
LA																															
D3																															
D2																															
D1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
D0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS																													SEE COMMENT #1	B(O)-∅ ENABLED	PLS159

TB00510S

COMMENTS:

1. D_1 is controlled by $B(1)_0$, which enables $B(O)_1$ when $B(O)_0$ outputs a High.
2. $Q(N)_{-0}$ is programmed as J-K flip-flop, and will toggle automatically at each rising-edge of the clock.

NOTE:

1. In order for the flip-flop to work the clock out (B_O) must be externally connected to pin 1.

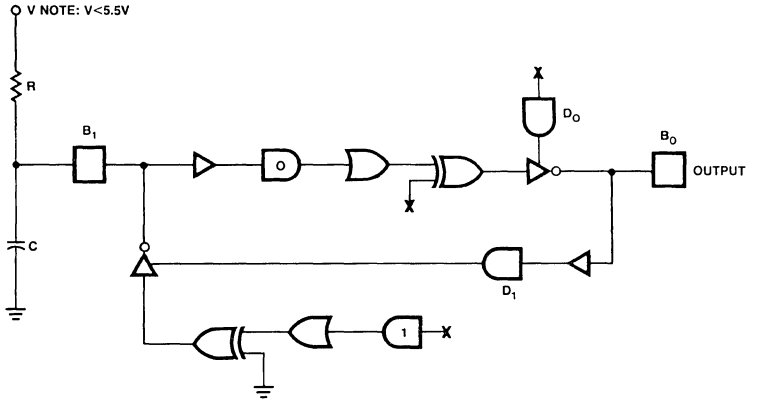
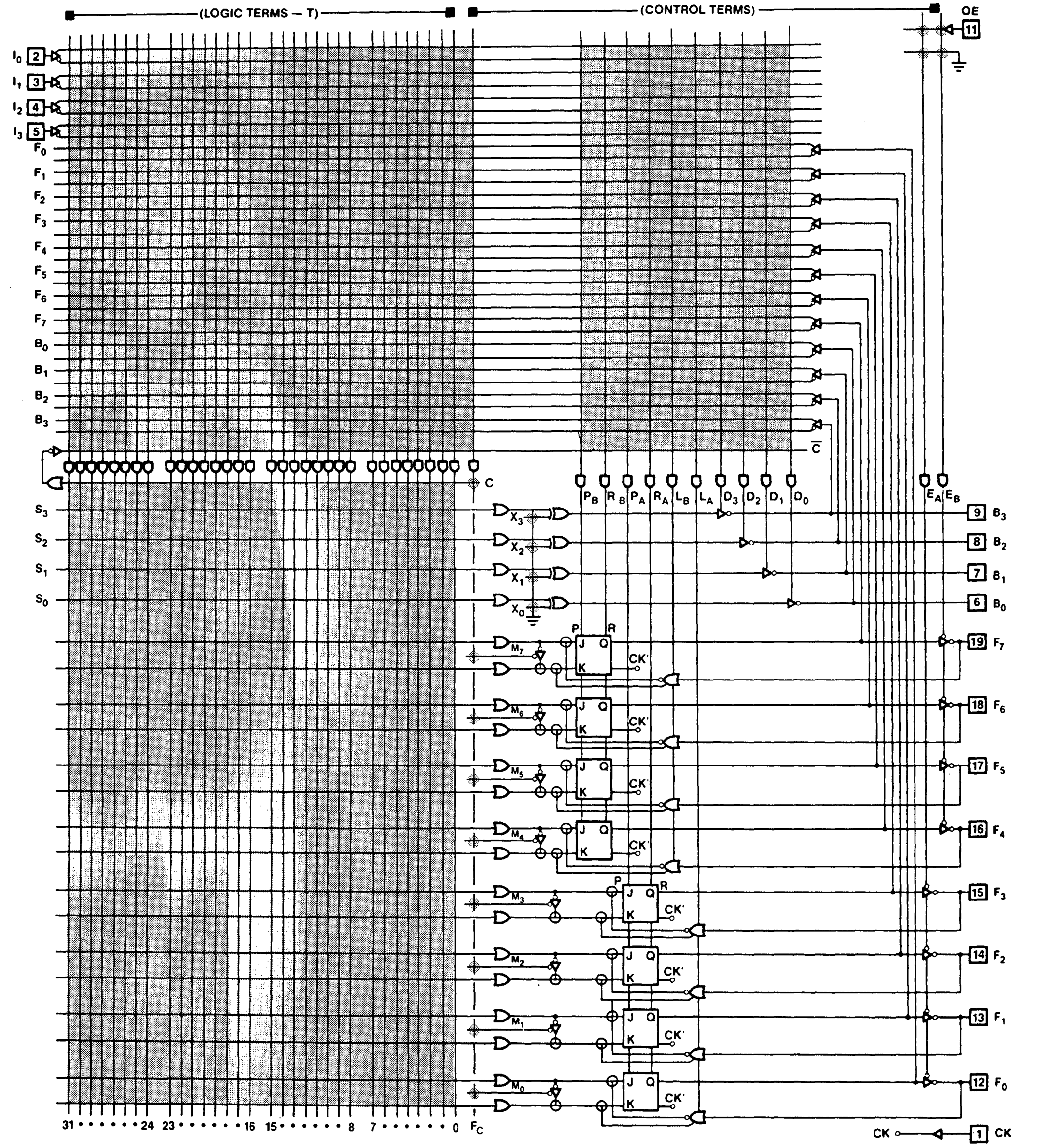


Figure 2. Logic Diagram of Oscillator Circuit



NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.

Figure 3. Logic Diagram of PLS159 FPLS

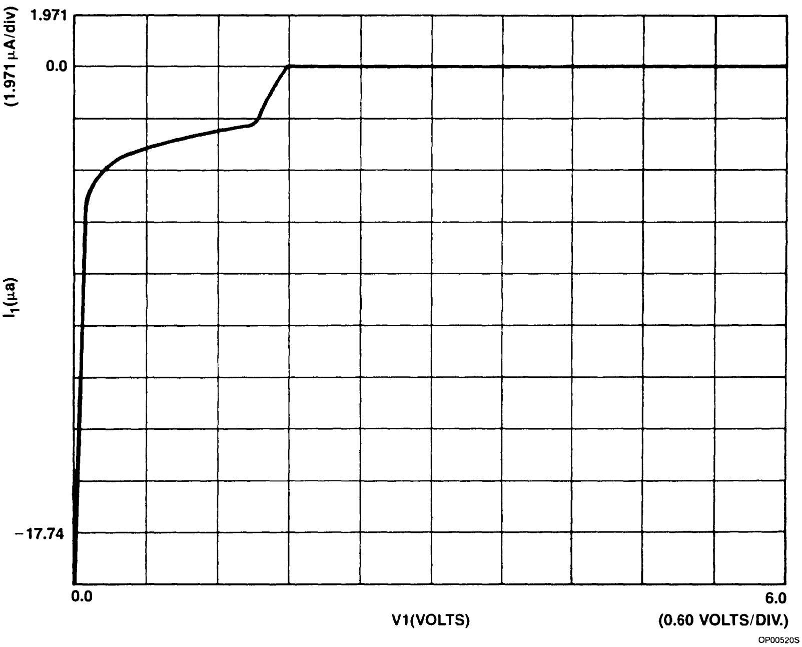


Figure 4. Input Current vs Input Voltage Characteristics of I/O Pins

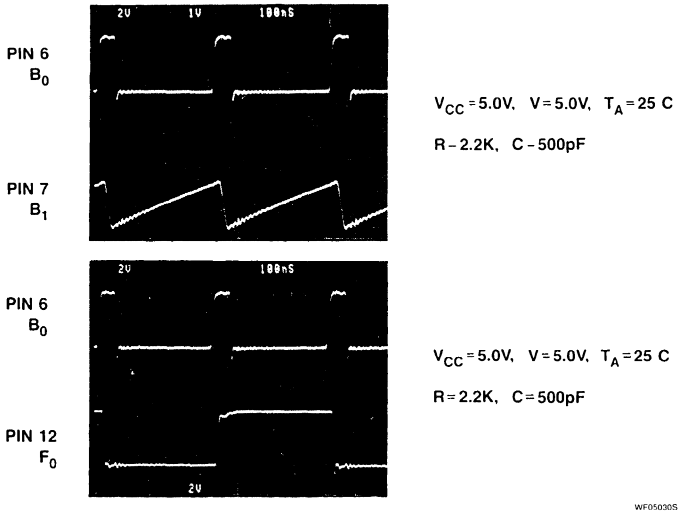


Figure 5. Output Waveforms of Oscillator Circuit

Signetics

AN14
Latches and Flip-Flops With PLS153

Application Note

Application Specific Products

DESCRIPTION

Using the simple AND, OR and INVERT logic functions of the PLS153, memory functions such as latches and edge-triggered flip-flops may be implemented with a relatively small part of the chip and without external wiring. In this application note, we will discuss the implementation of two R-S latches, a D-latch, an edge-triggered R-S flip-flop, and an edge-triggered D flip-flop.

INTRODUCTION TO PLS153

To implement this function, let's first take a look at the PLS153 logic diagram and its programming table as shown in Appendices A and B. On the left side of the logic diagram (Appendix A) are eight dedicated inputs, I_0 to I_7, each of which has a true and a complement output. Each output is connected to the inputs of 32 AND functions (we will call them AND-terms from now on), the outputs of which are, in turn, connected to the inputs of ten OR functions. The output of each OR function is connected to one input of an Exclusive-OR function, which is in turn connected to a non-inverting output buffer. The function of the XOR is to control the output polarity. The output, in its virgin state, is non-inverting, since one side of the XOR is connected to ground by the fuse X_n, where n = 0, 1, 3...9. To have the output inverted, one needs only to blow fuse X_n open so that the X_n input is unconditionally High. The output buffers are all three-state buffers which may be enabled or disabled by their corresponding AND gates. The output buffers are disabled in their virgin state. All pins labeled "B" are bidirectional. Input buffers of the "B" pins are identical to those of the "I" pins.

The programming table shown in Appendix B emulates a truth table. All the inputs to the device are positioned on the left side, and all the outputs are on the right side. Each row in the table corresponds to an 18-input AND-term with up to ten outputs. On the left side, or the input side of the table, each column represents an input. The 18 columns represent input buffers I_0 to I_7, B_0 to B_9. To distinguish between inputs and outputs of the bidirectional pin, B(I) is used for input and B(O) is used for outputs as shown in the programming table. On the right side of the table, each column represents an output circuit $(B(O)_{0-9})$ which consists of an OR gate, an XOR, and a non-inverting three-state buffer. The output buffers are controlled by AND-terms D_0 to D_9, the inputs of which may be connected to any number of the 18 inputs.

The polarity of the outputs is defined by the POLARITY entries which are on the upper right corner of the programming table.

To program the inputs to the AND-terms, an "H" will cause the fuse of the inverting input buffer to be blown, leaving the non-inverting buffer connected to the AND-term; an "L" will do the opposite. A " – " will cause both fuses to be blown, and therefore the programmed input is a "Don't care". A "0", the virgin state of the device, has both fuses intact, which causes the output of the AND-term to be unconditionally Low.

To program the outputs, a "." causes the fuse that connects the output of AND-term to the input of an OR to be blown and thus renders the output inactive. An "A" causes the fuse to remain intact and thus the output is active.

The output polarity of each output buffer may be programmed by entering an "H" or an "L" in the POLARITY section. An "L" causes the XOR to blow its grounding fuse and become inverted, whereas an "H" leaves the fuse intact and the output is non-inverted.

To AND several inputs, we put them in a row; to OR several inputs, we put them in different rows, as shown in illustrations in Appendix B.

SIMPLE R-S LATCH

A simple R-S latch may be formed by cross-coupling two NAND functions together as shown in Figure 1.

As an illustration, let's assign the input R to I_0 of the PLS153, input S to I_1, output Q to B_0, and output $\overline{Q}$ to B_1. As shown in Table 1, to form the NAND gates we need to program the POLARITY Low on $B(O)_0$ and $B(O)_1$. To unconditionally enable the output buffers, we "dash" out all inputs to D_0 and D_1. As for the inputs, we put an "H" on I_0, term-0 for the input R, non-inverted; another "H" on $B(I)_1$, term-0 for the feedback from Q. In the same manner, we program I_1, term-1 and $B(O)_0$ "H". The POLARITY, rows 0, 1, D_0 and D_1, forms a "truth table" with which one can analyze his own or someone else's design. The program in Table 1 may be illustrated as shown in Figure 2.

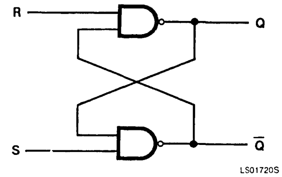


Figure 1. RS Latch

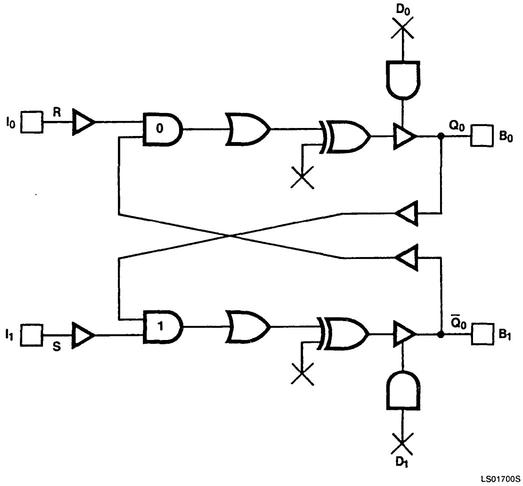


Figure 2. RS Latch

Latches and Flip-Flops With PLS153 AN14

Table 1. PLS153/153A Programming Table

CODE NO.																				POLARITY										
																												L	L	
	AND																			OR										
	I								B(I)											B(O)										
TERM	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	-	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	H	-		●	●	●	●	●	●	●	●	●	A	$Q=/(R \cdot \overline{Q})$
1	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	H		●	●	●	●	●	●	●	●	A	●	$\overline{Q}=/(S \cdot Q)$
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PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS							S	R									$\overline{Q_0}$	Q_0										$B(O)_1$ ($\overline{Q_0}$)	$B(O)_0$ (Q_0)	

PLS153

TB00860S

ANOTHER SIMPLE R-S LATCH

Another way to implement a simple latch is shown in Figure 3, in which two NOR functions are cross-coupled to form a latch.

As with the previous example, we first define the input and output pins. For this example, we use I_2 for the R input, I_3 for the S input, B_2 for the Q output, and B_3 for the $\overline{Q}$ output. We program B_2 and B_3 to have inverted outputs by programming POLARITY of B_2 and B_3 Low, as shown in Table 2. Terms 6 and 7 are ORed together by $B(O)_2$, rows 6 and 7. In the same manner $B(O)_3$ ORs Terms 8 and 9. The programmed table of this design may be represented as shown in Figure 4.

Since each AND-term of the PLS153 can accommodate up to 18 inputs (true or inverting inputs of eight from I_0 to I_7 and ten from B_0 to B_9), and each OR circuit can be connected to up to thirty-two AND-terms, we can add additional features such as those shown in Figure 5.

The programming of this design is left to the reader as an exercise.

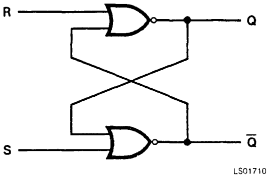

Figure 3. RS Latch

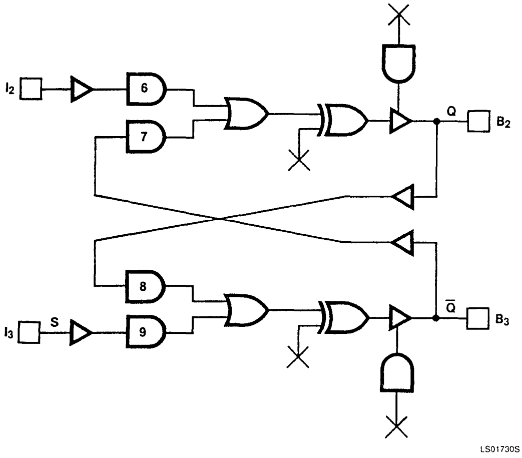

Figure 4. RS Latch

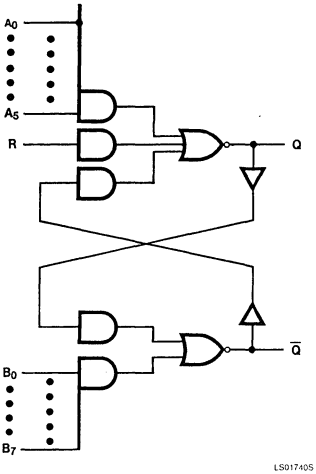

Figure 5. RS Latch

Latches and Flip-Flops With PLS153

Table 2. PLS153/153A Programming Table

CODE NO.																				POLARITY										
																										L	L	L	L	
TERM	AND																			OR										
	I								B(I)											B(O)										
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	-	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	H	-	$R\cdot\overline{Q}$	•	•	•	•	•	•	•	•	•	A	$Q=/(R\cdot\overline{Q})$
1	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	H	$S\cdot Q$	•	•	•	•	•	•	•	•	A	•	$\overline{Q}=/(S\cdot Q)$
2																														
3																														
4																														
5																														
6	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	R	•	•	•	•	•	•	•	A	•	•	$Q=/(R+\overline{Q})$
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	-	$\overline{Q}$	•	•	•	•	•	•	•	A	•	•	$Q=/(R+\overline{Q})$
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	Q	•	•	•	•	•	•	A	•	•	•	$\overline{Q}=/(Q+S)$
9	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	S	•	•	•	•	•	•	A	•	•	•	$\overline{Q}=/(Q+S)$
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PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS					S	R	S	R							$\overline{Q}$	Q	$\overline{Q}$	Q								B_3 ($\overline{Q}_1$)	B_2 (Q_1)	B_2	B_0	PLS153

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Latches and Flip-Flops With PLS153 AN14

D-LATCH

A simple D-latch can be constructed with an PLS153 as shown in Figure 6.

This circuit may be easily programmed into the PLS153 as shown in Table 3. The program may, in turn, be represented as shown in Figure 7.

This circuit may be expanded to have multiple D-latches using the same latch enable (LE).

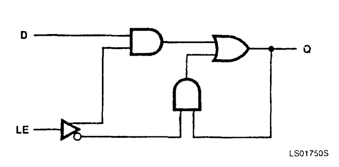

Figure 6. D Latch

R-S FLIP-FLOP

Two R-S latches may be combined to form a master-save flip-flop that is triggered at the rising-edge of the clock (or the falling-edge of the clock, if the designer so desires). Figure 8 shows a combination of two sets of cross-coupled NOR gates concatenated to form the flip-flop. The implementation of this circuit using PLS153 is as illustrated in Table 4 and Figure 9.

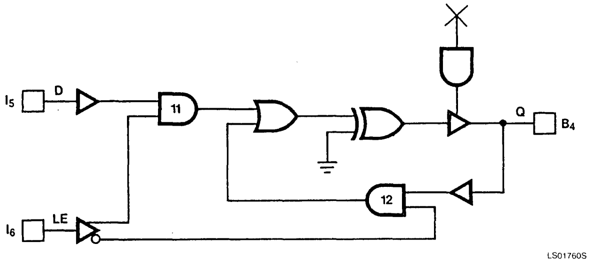

Figure 7. D-Latch

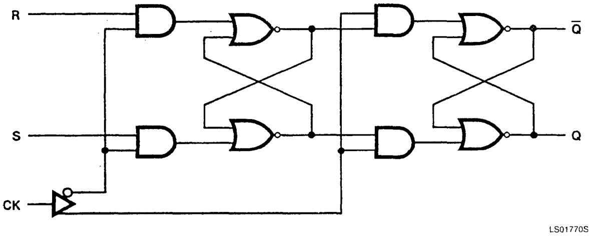

Figure 8. RS Flip-Flop

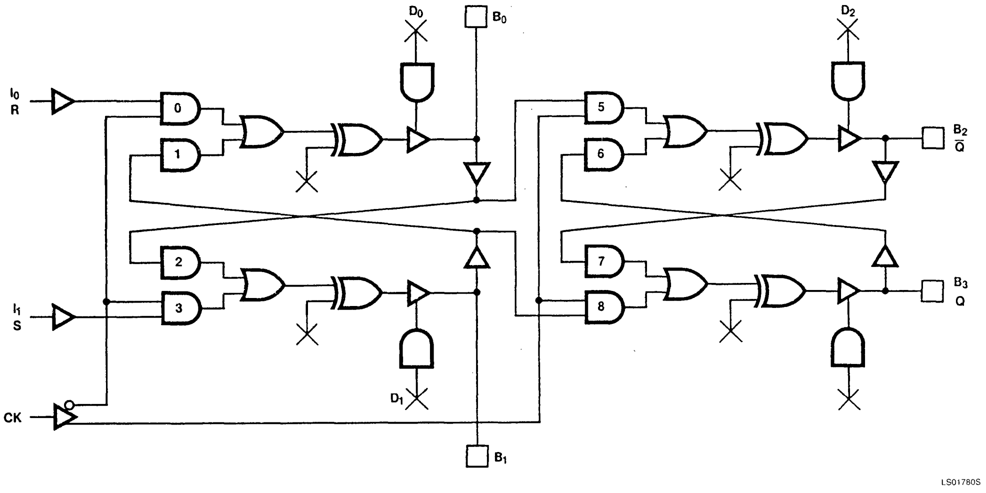

Figure 9. RS Flip-Flop

Latches and Flip-Flops With PLS153 AN14

Table 3. PLS153/153A Programming Table

CODE NO.																				POLARITY										
																									H	L	L	L	L	
	AND																			OR										
	I								B(I)											B(O)										
TERM	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	-	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	H	-	R·$\overline{Q}$	•	•	•	•	•	•	•	•	•	A	/(R·$\overline{Q}$)
1	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	H	S·Q	•	•	•	•	•	•	•	•	A	•	/(S·Q)
2																														
3																														
4																														
5																														
6	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	R	•	•	•	•	•	•	•	A	•	•	}/(R+$\overline{Q}$)
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	-	$\overline{Q}$	•	•	•	•	•	•	•	A	•	•	)
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	Q	•	•	•	•	•	•	A	•	•	•	}/(Q+S)
9	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	-	-	S	•	•	•	•	•	•	A	•	•	•	)
10																														
11	-	H	H	-	-	-	-	·	-	-	-	-	-	-	-	-	-	-	LE·D	•	•	•	•	•	A	•	•	•	•	}(LE·D+
12	-	L	-	-	-	-	-	-	-	-	-	-	-	H	-	-	-	-	$\overline{LE}$·Q	•	•	•	•	•	A	•	•	•	•	) $\overline{LE}$·Q)
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D2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS		LE	D		S	R	S	R						Q	$\overline{Q}$	Q	$\overline{Q}$	Q							B_4	B_3	B_2	B_1	B_0	

PLS153

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Latches and Flip-Flops With PLS153 AN14

Table 4. PLS153/153A Programming Table

CODE NO.																				POLARITY										
																											L	L	L	L	
TERM	AND																			OR										
	I								B(I)											B(O)										
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	-	-	-	-	-	L	-	H	-	-	-	-	-	-	-	-	-	-	$\overline{CK} \cdot R$	●	●	●	●	●	●	●	●	●	A	}/($R \cdot \overline{CK} + B_1$)
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	B_1	●	●	●	●	●	●	●	●	●	A	)
2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	B_0	●	●	●	●	●	●	●	●	A	●	}/($S \cdot \overline{CK} + B_0$)
3	-	-	-	-	-	L	H	-	-	-	-	-	-	-	-	-	-	-	$\overline{CK} \cdot S$	●	●	●	●	●	●	●	●	A	●	)
4																														
5	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	H	$CK \cdot B_0$	●	●	●	●	●	●	●	A	●	●	}/($B_0 \cdot CK + B_3$)
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	-	B_3	●	●	●	●	●	●	●	A	●	●	)
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	B_2	●	●	●	●	●	●	A	●	●	●	}/($B_1 \cdot CK + B_2$)
8	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	H	-	$CK \cdot B_1$	●	●	●	●	●	●	A	●	●	●	)
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D0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS						CK	S	R							$Q = B_3$	$\overline{Q} = B_2$	B_1	B_0								$B_3 = Q$	$B_2 = \overline{Q}$	B_1	B_0	

PLS153

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D FLIP-FLOP

An edge-triggered master-slave D flip-flop may be constructed with two D-latches in the manner shown in Figure 10.

An PLS153 may be programmed as shown in Figure 11 to implement the D flip-flop which is equivalent to the circuit shown in Table 5 in the PLS153 logic representation.

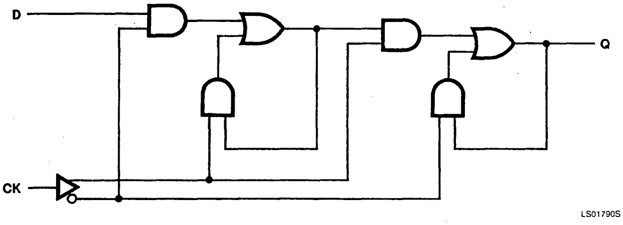

Figure 10. D Flip-Flop

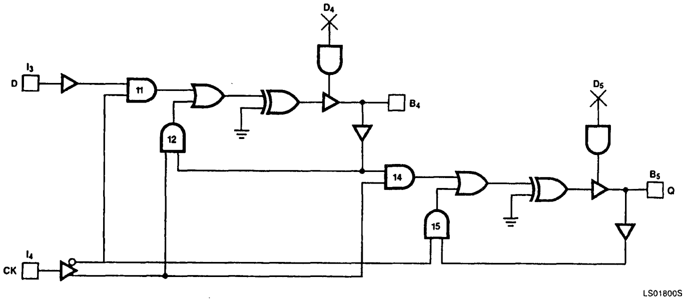

Figure 11. D Flip-Flop

Latches and Flip-Flops With PLS153

AN14

Table 5. PLS153/153A Programming Table

CODE NO.

TERM	AND																				OR										
	POLARITY																								H	H	L	L	L	L	
	I								B(I)												B(O)										
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	-	-	-	-	-	L	-	H	-	-	-	-	-	-	-	-	-	-	R·$\overline{CK}$	●	●	●	●	●	●	●	●	●	A	}/(R·$\overline{CK}$+B_1)
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	B_1	●	●	●	●	●	●	●	●	●	A	)
2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	B_0									A		
3	-	-	-	-	-	L	H	-	-	-	-	-	-	-	-	-	-	-	S·$\overline{CK}$									A		
4																														
5	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	-	H	CK·B_0								A			}/(B_0·CK+Q)
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	-	Q								A			)
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	B_2							A				}/(B_1·CK+B_2)
8	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	H	-	B_1·CK							A				)
9																														
10																														
11	-	-	-	L	H	-	-	-	-	-	-	-	-	-	-	-	-	-	$\overline{CK}$·D						A					}($\overline{CK}$·D+CK·
12	-	-	-	H	-	-	-	-	-	-	-	-	-	H	-	-	-	-	CK·B_4						A					} B_4)
13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
14	-	-	-	H	-	-	-	-	-	-	-	-	-	H	-	-	-	-	CK·B_4					A						}(CK·B_4+$\overline{CK}$·
15	-	-	-	L	-	-	-	-	-	-	-	-	H	-	-	-	-	-	$\overline{CK}$·Q					A						) Q)
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D4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS				CK	D	$\overline{CK}$	S	R					B_5 (Q)	B_4	Q = B_3	$\overline{Q}$ = B_2	B_1	B_0						B_5 (Q)	B_4	B_3	B_2	B_1	B_0	PLS153

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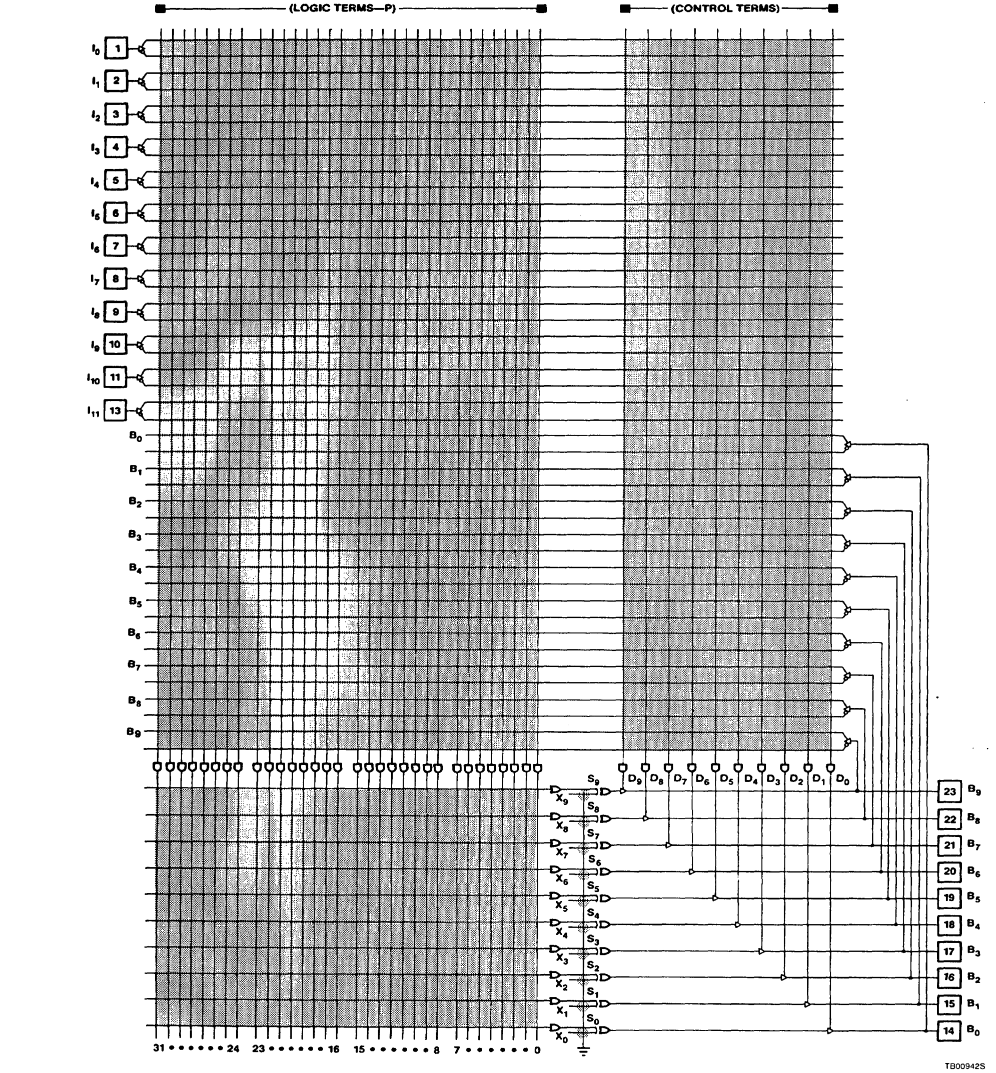
APPENDIX A



NOTES:

1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Figure A-1. FPLA Logic Diagram

Appendix B. PLS153/153A Programming Table

CODE NO.																				POLARITY										
																				H	H	H	H	L	L	L	H	H	H	
TERM	AND																			OR										
	I								B(I)											B(O)										
	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	H	H	H	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	$A \cdot B \cdot C \cdot D$	A	●	●	●	A	●	●	●	●	●	$X = A \cdot B \cdot C \cdot D$
1																														$T = /(A \cdot B \cdot C \cdot D)$
2																														
3																														
4	L	L	L	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	$\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$	●	A	●	●	●	A	●	●	●	●	$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$
5																														$U = /(\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D})$
6																														
7																														
8																														
9	-	H	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-		$B \cdot \overline{C}$	●	●	A	●	●	●	A	●	●	●	$Z = (B \cdot \overline{C} + B \cdot \overline{D} +$
10	-	H	-	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	$B \cdot \overline{D}$	●	●	A	●	●	●	A	●	●	●	$\overline{C} \cdot \overline{D})$
11	-	-	L	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	$\overline{C} \cdot \overline{D}$	●	●	A	●	●	●	A	●	●	●	$V = /(B \cdot \overline{C} + B \cdot \overline{D}$
12																														$+ \overline{C} \cdot \overline{D})$
13																														
14																														
15																														
16																														
17																														
18																														
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25																														
26																														
27																														
28																														
29																														
30																														
31																														
D9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D6																														
D5		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D4			-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D3	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-												
D2																														
D1																														
D0																														
PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS	A	B	C	D					X	Y	Z		T	U	V					X	Y	Z		T	U	V				

PLS153

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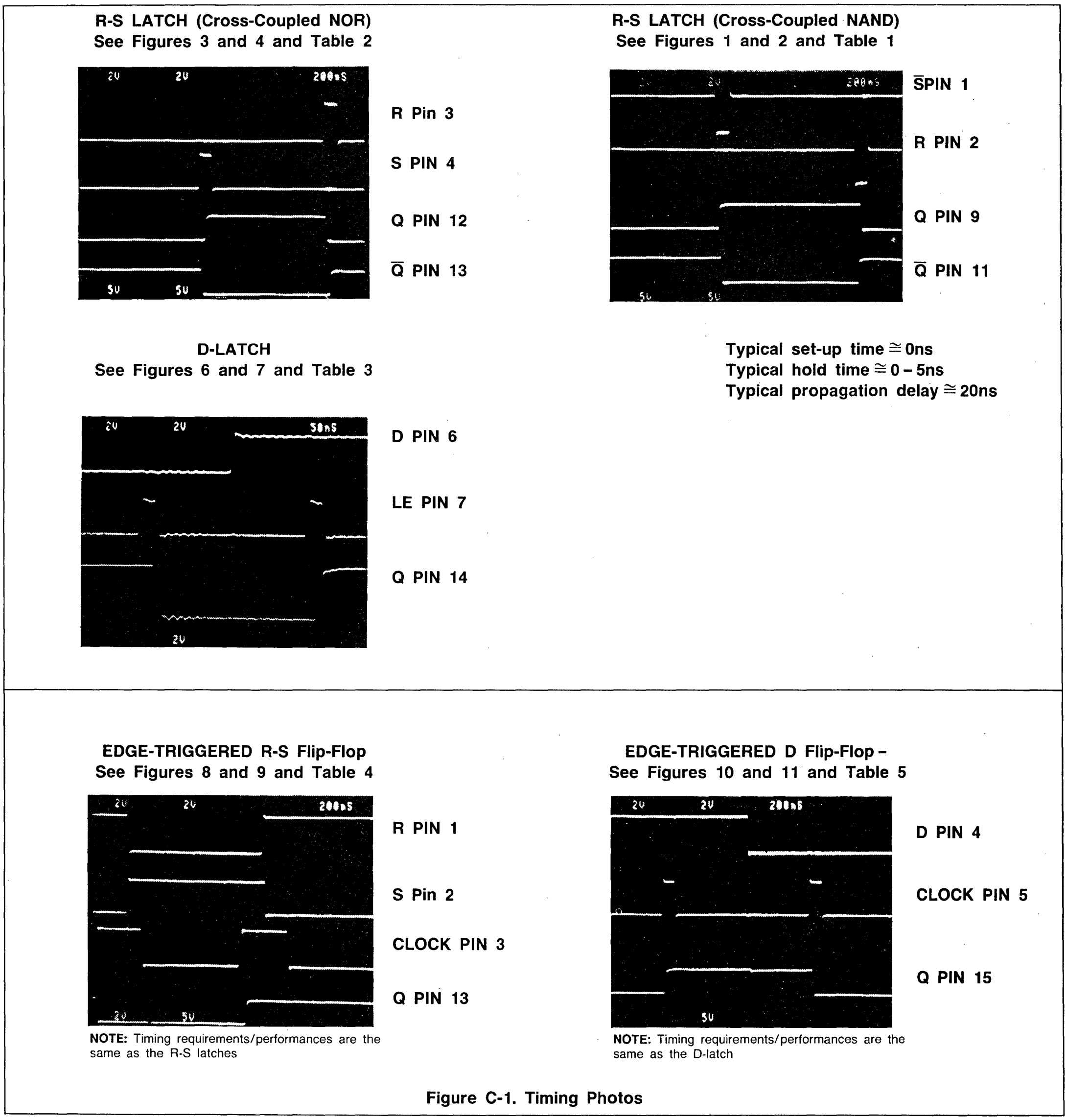
APPENDIX C



R-S LATCH (Cross-Coupled NOR)
See Figures 3 and 4 and Table 2

R-S LATCH (Cross-Coupled NAND)
See Figures 1 and 2 and Table 1

D-LATCH
See Figures 6 and 7 and Table 3

Typical set-up time ≅ 0ns
Typical hold time ≅ 0 - 5ns
Typical propagation delay ≅ 20ns

EDGE-TRIGGERED R-S Flip-Flop
See Figures 8 and 9 and Table 4

NOTE: Timing requirements/performances are the same as the R-S latches

EDGE-TRIGGERED D Flip-Flop -
See Figures 10 and 11 and Table 5

NOTE: Timing requirements/performances are the same as the D-latch

Figure C-1. Timing Photos

Signetics

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Application Note

Application Specific Products

INTRODUCTION

The PLS159 is a field programmable logic sequencer which consists of four dedicated inputs, four bidirectional I/O's, eight flip-flops, thirty two 16-input AND gates, twenty 32-input OR gates, and a complement array. Each flip-flop has a bidirectional I/O and may be individually programmed as J-K or D flip-flop, or switch between the two types dynamically. The flip-flops will accept data from the internal logic array or from the bidirectional I/O, or they may be set or reset asynchronously from the AND array. The output polarity of the four bidirectional I/O's are programmable and the direction is controlled by the AND array. Figure 1 is the logic diagram of PLS159.

PROGRAMMING THE PLS159

The programming table is shown in Table 1 where there is a place for everything that is shown in Figure 1. The program table is basically divided into two main sections. The left hand side of the table, section A, represents the input side of the AND gates, while the right hand side, section B, represents the OR gates sections which includes the flip-flops and the combinatorial outputs B(0) to B(3). The flip-flops modes are defined in section C and the output polarities of the combinatorial outputs are defined in section E. The programming symbols are detailed in Figure 2.

As shown in Table 1, the programming table is very similar to a truth table. Each column in section A represents an input to the 32 AND gates, and each row represents an AND gate connecting to 17 inputs. Columns I_0 to I_3 represent the 4 dedicated inputs, I_0 to I_3. Columns $B(I)_0$ to $B(I)_3$ represent the inputs of the 4 bidirectional I/O, B_0 to B_3. Columns $Q(P)_0$ to $Q(P)_7$ represent the feedback, F_0 to F_7, from the flip-flops (the present state). Column "C" represents the complement array.

As shown in Figure 1, the outputs of the AND gates are connected to an array of OR gates which, in turn, are connected to either flip-flops or output circuits. Columns $Q(N)_0$ to $Q(N)_7$ represent the next state which the flip-flops will be in. Columns $B(O)_0$ to $B(O)_3$ represent the combinatorial outputs B_0 to B_3.

Each row represents an AND gate with 17 inputs each of which may be true and/or complement and is, therefore, a perfect decoder. Referring to the programming symbols in Figure 2, to implement the equation

$$Z = A * B * C * D,$$

all one has to do is to enter one line as shown in Table 2, term−0.

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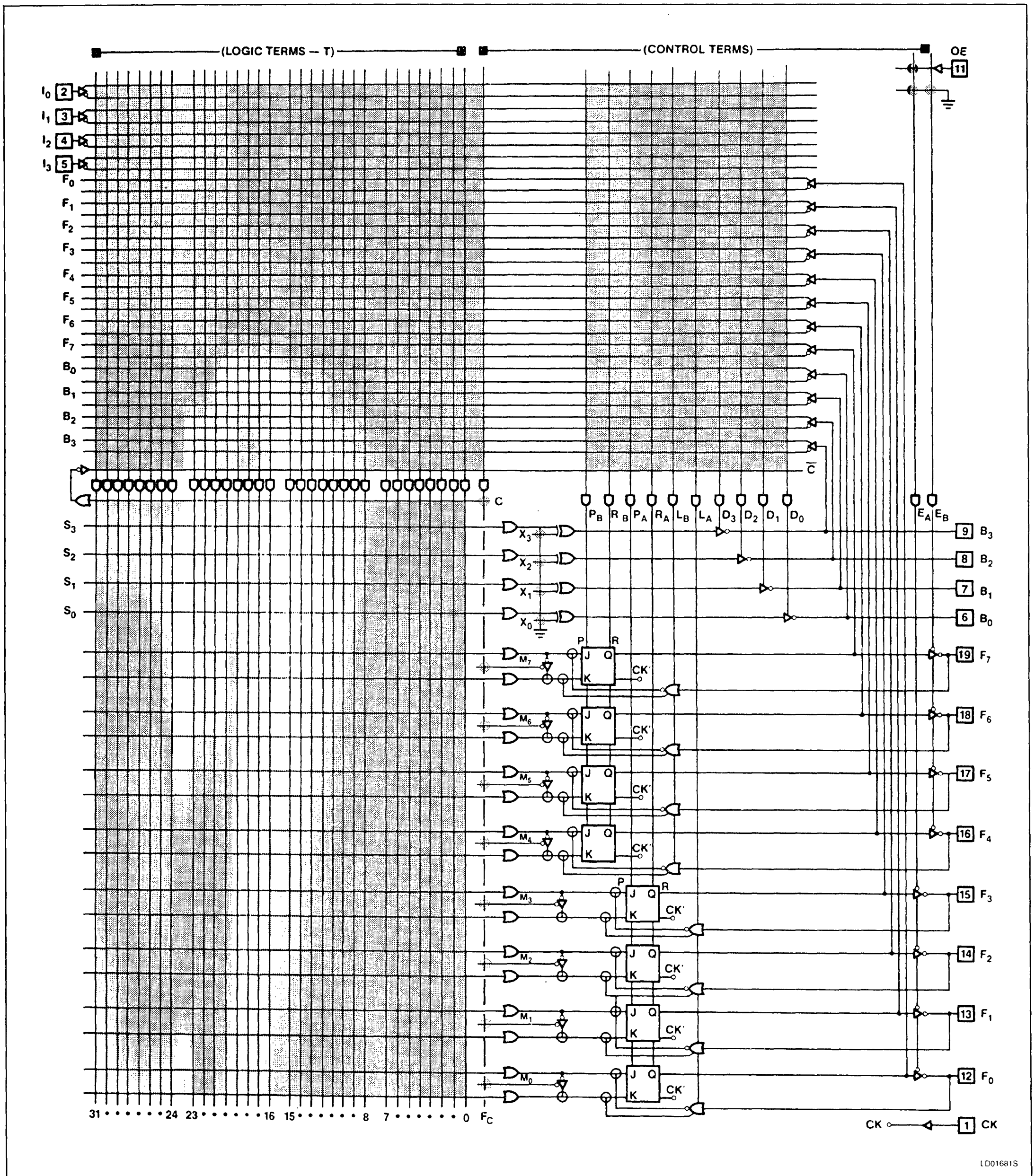
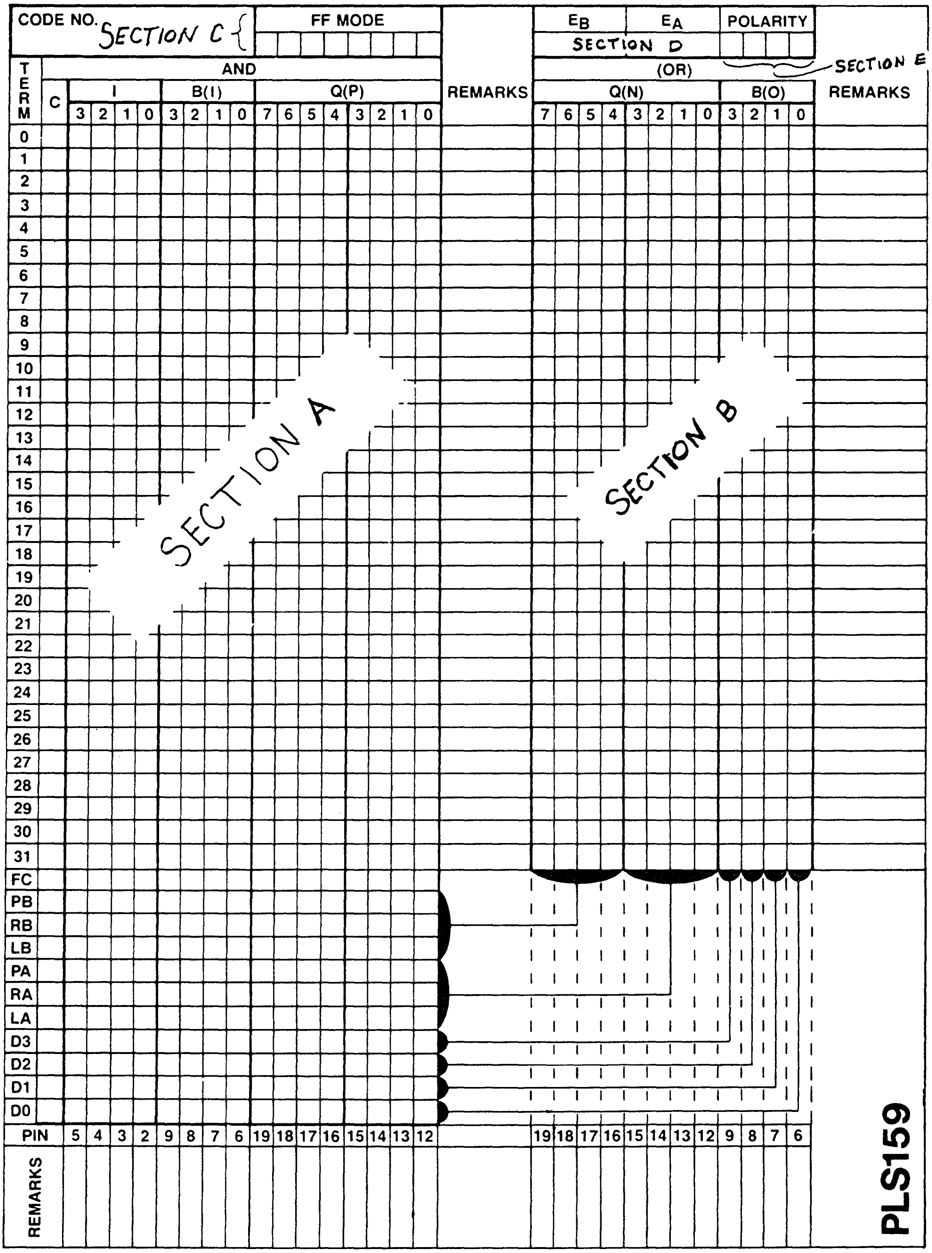


NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.

Figure 1. FPLS Logic Diagram

Table 1. FPLS Program Table



CODE NO. SECTION C {

FF MODE

EB | EA | POLARITY

SECTION D

SECTION E

TERM	C	AND																REMARKS	(OR)												REMARKS
		I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0																															
1																															
2																															
3																															
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FC																															
PB																															
RB																															
LB																															
PA																															
RA																															
LA																															
D3																															
D2																															
D1																															
D0																															
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS																															

SECTION A

SECTION B

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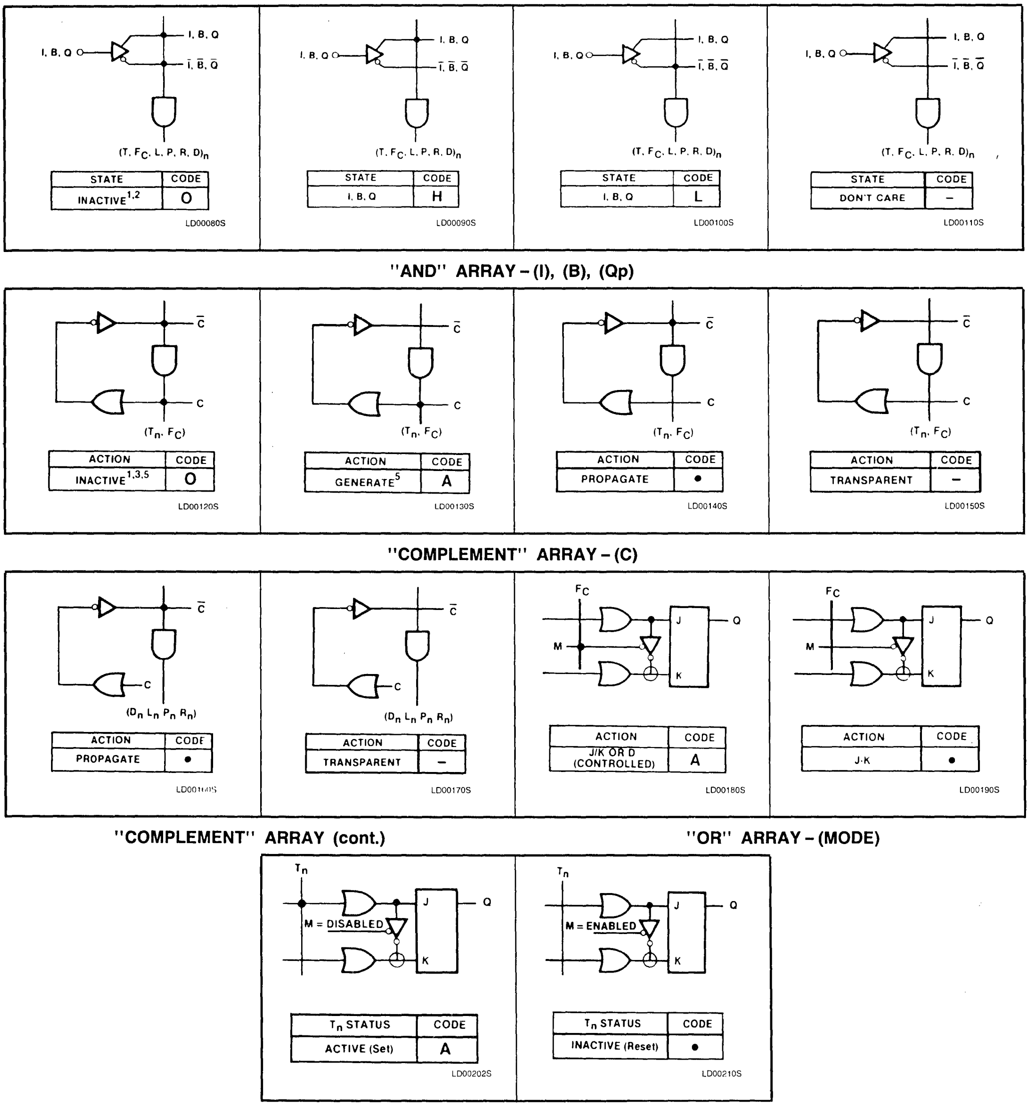
The FPLS can be programmed by means of Logic Programming equipment.

With Logic programming, the AND/OR-EX-OR input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Tables on the following pages.

In these Tables, the logic state or action of all I/O, control, and state variables is assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:



"AND" ARRAY – (I), (B), (Qp)

STATE	CODE
INACTIVE[1,2]	O

STATE	CODE
I, B, Q	H

STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)

ACTION	CODE
INACTIVE[1,3,5]	O

ACTION	CODE
GENERATE[5]	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

"COMPLEMENT" ARRAY (cont.)

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

"OR" ARRAY – (MODE)

ACTION	CODE
J/K OR D (CONTROLLED)	A

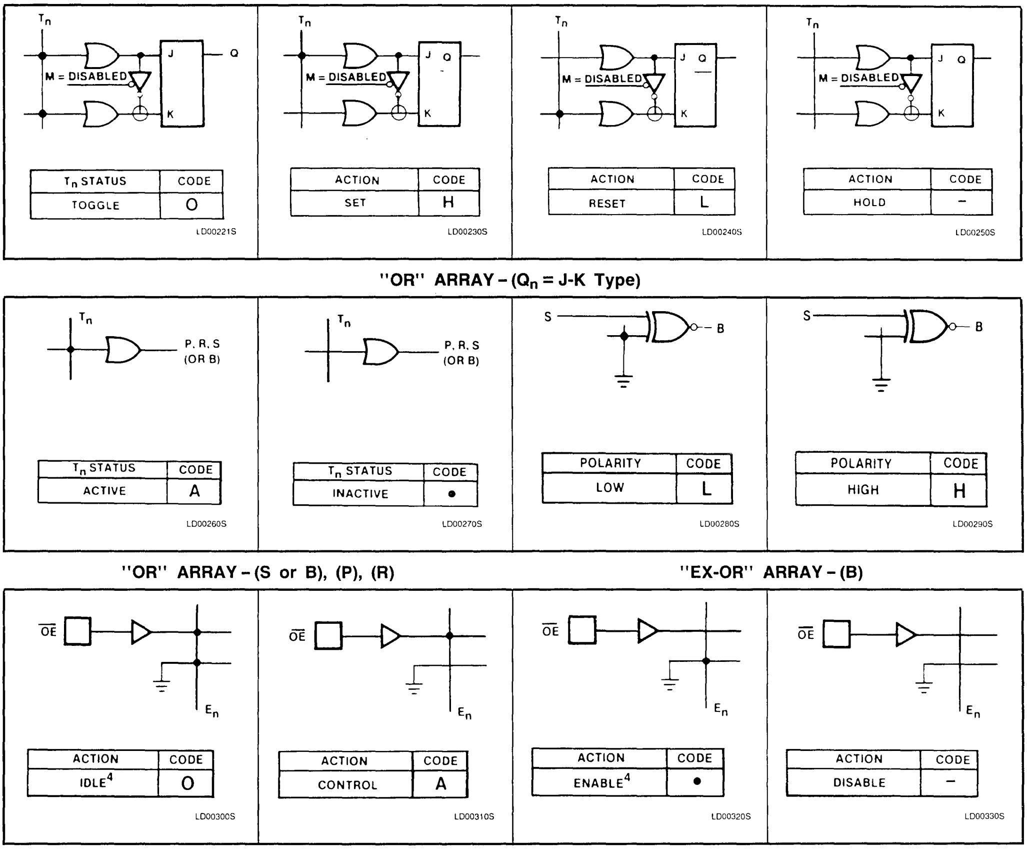
ACTION	CODE
J-K	•

"OR" ARRAY – (Q_N = D-Type)

T_n STATUS	CODE
ACTIVE (Set)	A

T_n STATUS	CODE
INACTIVE (Reset)	•

Figure 2



T_n STATUS	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

"OR" ARRAY – (Q_n = J-K Type)

T_n STATUS	CODE
ACTIVE	A

T_n STATUS	CODE
INACTIVE	•

POLARITY	CODE
LOW	L

POLARITY	CODE
HIGH	H

"OR" ARRAY – (S or B), (P), (R)

"EX-OR" ARRAY – (B)

ACTION	CODE
IDLE[4]	O

ACTION	CODE
CONTROL	A

ACTION	CODE
ENABLE[4]	•

ACTION	CODE
DISABLE	–

"$\overline{OE}$" ARRAY – (E)

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T, F_C, L, P, R, D)$_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n, F_C.
4. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L, P, R, D)$_n$ due to their lack of "OR" array links.

Figure 2 (continued)

Table 2. FPLS Program Table

CODE NO.	FF MODE	E_B	E_A	POLARITY			
				H	H	H	H

TERM	AND																	REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	-	H	H	H	H	-	-	-	-	-	-	-	-	-	-	-	-	A*B*C*D	-	-	-	-	-	-	-	-	•	•	•	A	z=A*B*C*D
1																															
2	-	L	H	L	-	-	-	-	-	-	-	-	-	-	-	-	-	/A* B*/C	-	-	-	-	-	-	-	-	•	•	A	•	Y=/A*B*/C
3																															
4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	"1"	-	-	-	-	-	-	-	-	•	A	•	•	X= 1
5																															
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	"0"	0	0	0	0	0	0	0	0	A	A	A	A	VIRGIN CONDITION
7	-	-	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-	"0"	-	-	-	-	-	-	-	-	A	•	•	•	W=0
8																															
9	-	H	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A*/B	-	-	-	-	-	-	-	-	A	•	•	•	W=A*/B
10	-	-	-	H	L	-	-	-	-	-	-	-	-	-	-	-	-	C*/D	-	-	-	-	-	-	-	-	A	•	•	•	W=C*/D
11																															
12																															
13																															
14																															
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LB																															
PA																															
RA																															
LA																															
D3																															
D2																															
D1																															
D0																															
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS		A	B	C	D																						W	X	Y	Z	

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Notice that only I_0 to I_3 on the left hand side and $B(O)_4$ on the right hand side have entries to implement the equation. All unused columns are dashed out or dotted out.

To implement the equation

Y = /A * B * /C,

enter one line as shown in Table 2, term-2 where the entry "H" represents the non-inverting input buffer while the entry "L" represents the inverting buffer. To have the AND gate to be unconditionally "High", dash out all the inputs of that particular AND gate as shown in Table 2, term-4. The virgin condition of the device, as shipped from the factory, has all connections intact, which means that the inverting and the non-inverting buffers of the same inputs are connected together. Such connection will cause the AND gate to be unconditionally "Low" as shown in Table 2, terms 6 and 7. The unconditional High and Low states are normally useful only internally and seldom brought out to the output pins.

To implement the equation

W = A * /B + C * /D,

enter one line for A * /B and another line for C * /D as shown in Table 2, terms 9 and 10. Use one line to AND something together; use different lines to OR something together — one line per item to be OR'ed.

All the pins which are labelled B's are bidirectional I/O pins. Their input buffers are represented by the B(I) columns on the left hand side of the programming table. An "H" entry represents the non-inverting buffer and an "L" entry represents the inverting buffer. Their output buffers are represented by the B(O) columns on the right hand side of the table. An "A" entry means that the output is active (connected to the AND gates); a "." entry means that the output is inactive (not connected). The outputs may be programmed to be inverting or noninverting. The polarity of each output is determined by its exclusive OR gate (Figure 1 and Figure 2). To have a non-inverting output, enter an "H" in the section labelled "POLARITY" (Table 1, Section E). To have an inverting output, enter an "L". For example, Table 3, terms-0 and-2 implement the equation

Z = /(A * B) and Y = A * B

respectively. The above two equations may also be implement by term-4 which uses the same AND gate to drive two OR gates.

Besides being able to have programmable Active-High or Active-Low output, the programmable output polarity feature also low output, the programmable output polarity feature also allows the user to minimize his AND term utilization by converting his logic equation into other forms such as conversion by De Morgan Theorem.

For example, the equation

X = A + B + C + D

takes four AND terms to implement as shown in Table 3, terms 6 to 9. By using De Morgan Theorem, the same equation is changed to

/W = /A * /B * /C * /D

The result is as shown in term 11 – a saving of three AND terms. The output buffers are disabled in their virgin states so that they all behave as inputs. The buffers are enabled or disabled by their corresponding Control AND terms D_0 to D_3 (see Figure 1). The Control AND terms are represented in the programming table on the last four rows on the left hand side. Dashing out all the inputs will cause the output buffer to be unconditionally enabled, whereas a "0" (zero) will cause the buffer to be unconditionally disabled. The buffers may also be controlled by a logical condition, e.g. A * /B * /C, etc.

There are eight flip-flops on the chip each of which may be programmed as a J/K or a D flip-flop, or they may be programmed to switch dynamically. As shown in Figure 1, each flip-flop is a J/K to begin with. A tri-state inverter is connected in between the J and K inputs of each flip-flop, which when enabled by the AND gate F_C, will cause the flip-flop to function as a D flip-flop. The inverters are enabled by F_C through fuses M_0 to M_7. A "." in the F/F Mode entry of the programming table means that particular fuse is to be disconnected and that particular flip-flop is to be J/K. An "A" entry will leave the M fuses intact, which allow the flip-flop to be D or J/K as controlled by the output of F_C (see Figure 2, "OR" ARRAY-(MODE)). The inputs to the flip-flops are represented by the programming table as the next state, $Q(N)_{0 \text{ to } 7}$ since their inputs are from the OR array. The outputs of these registers are connected to their respective tri-state inverting output buffers, four of which are controlled by EA and the other four by EB. A "." in EA will enable outputs F_0 to F_3, whereas a "-" will disable them. An "A" will allow the output buffers to be controlled by /OE, pin 11. Table 4, terms 0, 1 and 3 represent the following equations

Q_0: J = A * C + /B * /E eq. 1

Q_0: K = A * /C eq. 2

Notice that the J input in equation 1 is represented by the "H" entry in terms-0 and 1, column $Q(N)_0$ while the K input in equation 2 is represented by the "L" entry in term-3, column $Q(N)_0$. An undefined input, J or K, is considered "Low".

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Table 3. FPLS Program Table

CODE NO.	FF MODE	E_B	E_A	POLARITY
				L H H L

TERM	AND																	REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	–	–	–	H	H	–	–	–	–	–	–	–	–	–	–	–	–	A*B	–	–	–	–	–	–	–	–	•	•	•	A	z=/(A*B)
1																															
2	–	–	–	H	H	–	–	–	–	–	–	–	–	–	–	–	–	A*B	–	–	–	–	–	–	–	–	•	•	A	•	Y= A*B
3																															
4	–	–	–	H	H	–	–	–	–	–	–	–	–	–	–	–	–	A*B	–	–	–	–	–	–	–	–	•	•	A	A	z = /(A*B)
5																															Y = A*B
6	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	A	–	–	–	–	–	–	–	–	•	A	•	•	
7	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	B	–	–	–	–	–	–	–	–	•	A	•	•	
8	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	C	–	–	–	–	–	–	–	–	•	A	•	•	x=A+B+C+D
9	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	D	–	–	–	–	–	–	–	–	•	A	•	•	
10																															
11	–	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	/A*/B*/C*/D	–	–	–	–	–	–	–	–	A	•	•	•	W=/(/A*/B*/C
12																															*/D)
13																															
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D1																															
D0																															
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS			B	A																							W	X	Y	Z	

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Table 4. FPLS Program Table

CODE NO.										FF MODE									E_B				E_A				POLARITY				
										●	●	●				A	●		●				●								
TERM	AND																	REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	–	H	–	H	–	–	–	–	–	–	–	–	–	–	–	–	–	A*C	–	–	–	–	–	–	–	H					J= A*C
1	–	–	L	–	L	–	–	–	–	–	–	–	–	–	–	–	–	/B*/E	–	–	–	–	–	–	–	H					+/B*/E
2																															
3	–	H	–	L	–	–	–	–	–	–	–	–	–	–	–	–	–	A*/C	–	–	–	–	–	–	–	L					K= A*/C
4																															
5	–	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	/A*/B*/C	●	●	●	●	●	●	A	●					D=/A*/B*/C
6	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	E	●	●	●	●	●	●	A	●					+E
7																															
8	–	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	/A*/B*/C	–	–	–	–	–	–	H	–					D=/A*/B*/C
9	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–	–	–	E	–	–	–	–	–	–	H	–					+E
10																															
11	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	O	–	–	–	–	–					
12	–	–	–	–	–	–	–	–	–	–	–	H	–	–	–	–	–		–	O	–	–	–	–	–	–					T=1
13	–	–	–	–	–	–	–	–	–	–	H	H	–	–	–	–	–		O	–	–	–	–	–	–	–					T= Q_5
14																															T= Q_5*Q_6
15																															
16																															
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FC	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
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PA																															
RA																															
LA																															
D3																															
D2																															
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D0																															
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS		A	B	C	D																										

PLS159

TB00411S

PLS159 Primer

AN15

A D flip-flop may be implemented by first entering an "A" in F/F MODE. Then enter "0" in the row F_C, which will unconditionally enable the tri-state inverter between the J and K inputs. The following logic equation may be implemented as shown in Table 4, term 5

Q_1: D = /A * /B * /C + E.

Notice that the entries in term 5, columns $Q(N)_{0 \text{ to } 7}$ are "A" and "." instead of "H" and "L" as in the case of J/K flip-flops. The entry "A" will cause the fuse connecting to the "K" input to be disconnected and the "J" fuse to be intact. Whereas the entry "." will cause both fuses to be disconnected. This feature enables the user to quickly recognize the mode in which the flip-flops are operating without having to go through the control terms. Some commercially available device programmers in the market may not have the software capability to implement this feature, in which case an "H" and a "-" may be used in place of "A" and "." respectively as shown in Table 4, terms 8 and 9.

Of course, the term F_C may have inputs instead of zeros and dashes, in which case the flip-flop modes are controlled dynamically.

When both the J and K inputs are "1's", the flip-flop will toggle. A simple 3-bit counter may be implemented using only AND terms as shown in Table 4 terms 11, 12 and 13. The logic equations for the three flip-flops are as the following:

Q_5: T = 1; (Q_5 toggles unconditionally)
Q_6: T = Q_5; (Q_6 toggles when Q_5 = 1)
Q_7: T = $Q_5 * Q_6$; (Q_7 toggles when Q_5 * Q_6 = 1)

The above equations represent an octal up-counter. However, since the outputs of the flip-flops are inverted, the counting sequence of the outputs is that of a down-counter.

The flip-flops may be asynchronously set and reset by the Control AND terms PA/PB and RA/RB respectively. As shown in Figure 1, PA and RA controls flip-flops F_0 to F_3, while PB and RB control F_4 to F_7.

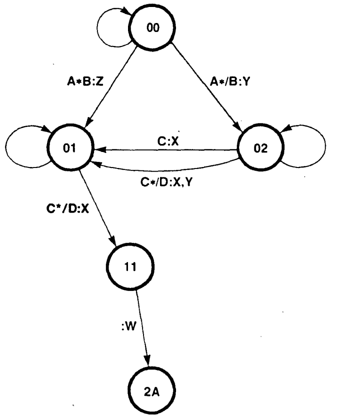

Figure 3

In order to save the number of input pins, the eight flip-flops may be synchronously loaded directly from their own output pins. To use this feature, EA and/or EB must be programmed "A" or "-" so that the output buffers may be disabled before loading. As shown in Figure 1, every flip-flop has an OR/NOR gate the input of which is directly connected to the output pin and the outputs of the OR/NOR are connected to the K and J inputs respectively. This OR/NOR gate inverts the input and feeds it to the flip-flop in a "wire-OR" fashion. Therefore, when loading data directly into the flip-flops from the output pins, caution must be exercised to insure that the inputs from the OR array does not interfere with the data being loaded. For example, if the data being loaded is a "1" on the output pin, the J input will be a "0" and the K input will be a "1". If, at the same time, a "1" is present at the J-input from the OR array, the flip-flop will see "1's" in both J and K inputs. It will toggle as a result. The OR/NOR gates are enabled by the Control AND terms LA and LB. LA controls flip-flops F_0 to F_3 and LB controls F_4 to F_7.

All Control AND terms function and are programmed in the same manner as the other AND terms. The only difference is that the Control AND terms are not connected to the OR array.

The outputs of the flip-flops may be fed back into the AND array as the present state, Q(P). The output of the AND array into the OR array and the inputs to the flip-flops is the next state, Q(N). As an example, Figure 3 is a state machine implemented in a PLS159 as shown in Table 5, terms 0 to 6.

Table 5. FPLS Program Table

CODE NO.										FF MODE									E_B				E_A				POLARITY				
										●	●	●	●	●	●	●	●		●				●				H	H	H	H	
TERM	AND																	REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	–	H	H	–	–	–	–	–	–	L	L	L	L	L	L	L	L		L	L	L	L	L	L	L	H	•	•	•	A	
1	–	–	–	H	L	–	–	–	–	L	L	L	L	L	L	L	H		L	L	L	H	L	L	L	H	•	A	•	•	
2	–	–	–	–	–	–	–	–	–	L	L	L	H	L	L	L	H		L	L	H	L	H	L	H	L	A	•	•	•	
3																															
4	–	H	L	–	–	–	–	–	–	L	L	L	L	L	L	L	L		L	L	L	L	L	L	H	L	•	•	A	•	
5	–	–	–	H	–	–	–	–	–	L	L	L	L	L	L	H	L		L	L	L	L	L	L	L	H	•	A	•	•	
6	–	–	–	H	L	–	–	–	–	L	L	L	L	L	L	H	L		L	L	L	L	L	L	L	H	•	A	A	•	
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D3	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
D2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
D1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
D0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS		A	B	C	D																						W	X	Y	Z	PLS159

TB00091S

Signetics

AN16
PLS159 As Modulo Counters

Application Note

Application Specific Products

DESCRIPTION

The field-programmable logic sequencer (FPLS) PLS159 has eight edge-triggered flip-flops which may be individually programmed to be J/K, D, or toggle flip-flops. The detail logic diagram of the device is shown in Figure 2.

A counter may be constructed by having individual flip-flops toggle when they are at certain states. Implementing such counters requires one toggle flip-flop per bit and an associating AND gate as a decoder for each flip-flop. Such a method allows the PLS159 to be a counter from modulo 2 to 256 or from one bit to 8 bits.

MODULO-8 UP/DOWN COUNTER

The Up-Counter

The PLS159 has an inverting output buffer for each flip-flop. Therefore the counting sequence of the flip-flops is from 7 to 0 so that the outputs will count from 0 to 7. Table 1 is the truth table of the internal counting sequence.

Table 1

COUNT	Q_2	Q_1	Q_0
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0

From Table 1, logic equations for the flip-flops may be generated as the following:

Q_0: T = 1;	(Q_0 unconditionally toggles)
Q_1: T = $/Q_0$;	(Q_1 toggles if $Q_0 = 0$)
Q_2: T = $/Q_0 * /Q_1$;	(Q_2 toggles if both Q_0 and $Q_1 = 0$)

The equations are implemented as shown in Table 2, terms 0, 1, and 2. E_A is enabled, and the mode for the three flip-flops is set to J/K. All unused flip-flops and outputs (the B(0)'s) associating to AND-terms are "dashed" or "dotted" out. The event to be counted is connected to the clock input, pin 1 of the device.

The Down-Counter

The down-counter is constructed in the same manner as the up-counter except that the counting sequence is reversed. The down-counter is implemented in Table 2, terms 4 to 6 with the corresponding flip-flop mode set to J/K and E_B enabled.

Modulo-16 Counter

Expanding the modulo-8 counter to 4-bit, the counter becomes modulo-16, Table 3, terms 0 to 3 and the associating F/F MODE and E_A implement a modulo-16 up-counter, while terms 5 to 8 and the associating F/F MODE and E_B implement the modulo-16 down-counter.

PLS159 As Modulo Counters

AN16

Table 2

CODE NO.	FF MODE								E_B	E_A	POLARITY			
	•	•	•	•	•	•	•	•	•	•				

TERM	C	AND																REMARKS	(OR)												REMARKS
		I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	—	—	—	—	O	•	•	•	•	
1		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L		—	—	—	—	—	—	O	—	•	•	•	•	
2		—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	L		—	—	—	—	—	O	—	—	•	•	•	•	
3																															
4		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	O	—	—	—	—	•	•	•	•	
5		—	—	—	—	—	—	—	—	—	—	—	H	—	—	—	—		—	—	O	—	—	—	—	—	•	•	•	•	
6		—	—	—	—	—	—	—	—	—	—	H	H	—	—	—	—		—	O	—	—	—	—	—	—	•	•	•	•	
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PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS																															

PLS159

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PLS159 As Modulo Counters

Table 3

CODE NO.	FF MODE								E					

CODE NO.	FF MODE								E_B	E_A	POLARITY			
	●	●	●	●	●	●	●	●	●	●				

TERM		AND																REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	O	•	•	•	•	
1		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	L		–	–	–	–	–	–	O	–	•	•	•	•	
2		–	–	–	–	–	–	–	–	–	–	–	–	–	–	L	L		–	–	–	–	–	O	–	–	•	•	•	•	
3		–	–	–	–	–	–	–	–	–	–	–	–	–	L	L	L		–	–	–	–	O	–	–	–	•	•	•	•	
4																															
5		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	O	–	–	–	–	•	•	•	•	
6		–	–	–	–	–	–	–	–	–	–	–	H	–	–	–	–		–	–	O	–	–	–	–	–	•	•	•	•	
7		–	–	–	–	–	–	–	–	–	–	H	H	–	–	–	–		–	O	–	–	–	–	–	–	•	•	•	•	
8		–	–	–	–	–	–	–	–	–	H	H	H	–	–	–	–		O	–	–	–	–	–	–	–	•	•	•	•	
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PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS																															PLS159

TB00011S

DECADE COUNTER

The Decade Up-Counter

The truth table of a decade counter is as shown in Table 4.

Table 4

COUNT	Q_3	Q_2	Q_1	Q_0
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
0	1	1	1	1

Logic equations may be generated from Table 4 as the following:

Q_0: T = 1;
Q_1: T = $/Q_0$ * Q_3;
Q_2: T = $/Q_0$ * $/Q_1$ * Q_3;
Q_3: T = $/Q_0$ * $/Q_1$ * $/Q_2$ * Q_3 +
$/Q_0$ * Q_1 * Q_2 * $/Q_3$;

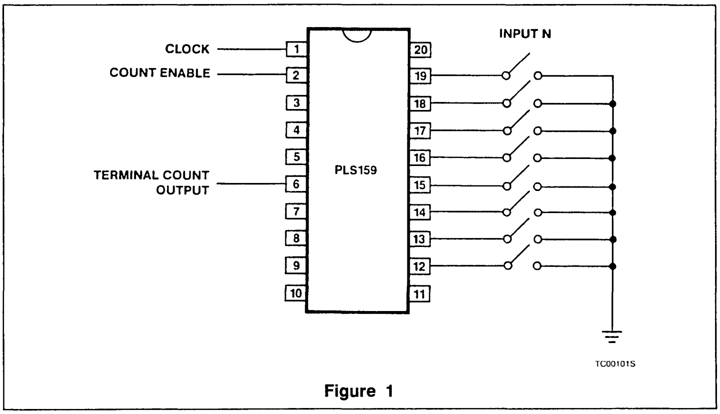

Figure 1

The equations are implemented as shown in Table 5, terms 0 to 4 and the associating flip-flop mode and E_A settings.

Decade Down-Counter

The decade down-counter is similar to the decade up-counter except that the counting sequence is reversed from 0 to 9 as shown in Table 5, terms 6 to 11 with the associating F/F MODE set to J/K and E_B to ENABLE.

Decade Down Counter

COUNT	Q_7	Q_6	Q_5	Q_4
9	0	1	1	0
8	0	1	1	1
7	1	0	0	0
6	1	0	0	1
5	1	0	1	0
4	1	0	1	1
3	1	1	0	0
2	1	1	0	1
1	1	1	1	0
0	1	1	1	1
9	0	1	1	0

Q_4: T = 1;
Q_5: T = Q_4 * Q_5 * Q_6 * $/Q_7$ +
Q_4 * $/Q_5$ * $/Q_6$ * Q_7 +
Q_4 * Q_5 * $/Q_6$ * Q_7 +
Q_4 * $/Q_5$ * Q_6 * Q_7 ;
Q_6: T = Q_4 * Q_5 * Q_6 * $/Q_7$ +
Q_4 * Q_5 * $/Q_6$ * Q_7 ;
Q_7: T = Q_4 * Q_5 * Q_6 * $/Q_7$ +
Q_4 * Q_5 * Q_6 * Q_7 ;

DIVIDE-BY-N COUNTER

This counter, shown in Figure 1 and Table 6, takes an input (maximum = 8 bits for each device), complements it, and counts until all flip-flops become 1, then a terminal count is sent out at $B(O)_0$ (divide-by-N). At the end of the count, where all flip-flops are 1's, terms LA and LB are activated which causes the flip-flops to load data from F_0 to F_7, and the cycle starts again. Since there are 8 flip-flops, the maximum count is 256.

PLS159 As Modulo Counters

Table 5

CODE NO.	FF MODE								EB	EA	POLARITY			
	•	•	•	•	•	•	•	•	●	●				

TERM	AND																	REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		-	-	-	-	-	-	-	O	•	•	•	•	
1	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	-	L		-	-	-	-	-	-	O	-	•	•	•	•	
2	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	L	L		-	-	-	-	-	O	-	-	•	•	•	•	
3	-	-	-	-	-	-	-	-	-	-	-	-	-	H	L	L	L		-	-	-	-	O	-	-	-	•	•	•	•	
4	-	-	-	-	-	-	-	-	-	-	-	-	-	L	H	H	L		-	-	-	-	O	-	-	-	•	•	•	•	
5																															
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		-	-	-	O	-	-	-	-	•	•	•	•	
7	-	-	-	-	-	-	-	-	-	L	H	H	H	-	-	-	-		O	O	O	-	-	-	-	-	•	•	•	•	
8	-	-	-	-	-	-	-	-	-	H	L	L	H	-	-	-	-		-	-	O	-	-	-	-	-	•	•	•	•	
9	-	-	-	-	-	-	-	-	-	H	L	H	H	-	-	-	-		-	O	O	-	-	-	-	-	•	•	•	•	
10	-	-	-	-	-	-	-	-	-	H	H	L	H	-	-	-	-		-	-	O	-	-	-	-	-	•	•	•	•	
11	-	-	-	-	-	-	-	-	-	H	H	H	H	-	-	-	-		O	-	-	-	-	-	-	-	•	•	•	•	
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PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS																															

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PLS159 As Modulo Counters

Table 6

CODE NO.	FF MODE								E_B	E_A	POLARITY			
	•	•	•	•	•	•	•	•	—	—				H

TERM	C	AND																REMARKS	(OR)												REMARKS
		I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0		—	—	—	L	—	—	—	L	—	—	—	—	—	—	—	—		—	—	—	—	—	—	—	O	•	•	•	•	
1		—	—	—	L	—	—	—	L	—	—	—	—	—	—	—	H		—	—	—	—	—	—	O	—	•	•	•	•	
2		—	—	—	L	—	—	—	L	—	—	—	—	—	—	H	H		—	—	—	—	—	O	—	—	•	•	•	•	
3		—	—	—	L	—	—	—	L	—	—	—	—	—	H	H	H		—	—	—	—	O	—	—	—	•	•	•	•	
4		—	—	—	L	—	—	—	L	—	—	—	—	H	H	H	H		—	—	—	O	—	—	—	—	•	•	•	•	
5		—	—	—	L	—	—	—	L	—	—	—	H	H	H	H	H		—	—	O	—	—	—	—	—	•	•	•	•	
6		—	—	—	L	—	—	—	L	—	—	H	H	H	H	H	H		—	O	—	—	—	—	—	—	•	•	•	•	
7		—	—	—	L	—	—	—	L	—	H	H	H	H	H	H	H		O	—	—	—	—	—	—	—	•	•	•	•	
8		—	—	—	L	—	—	—	—	H	H	H	H	H	H	H	H		—	—	—	—	—	—	—	—	•	•	•	A	
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PB																															
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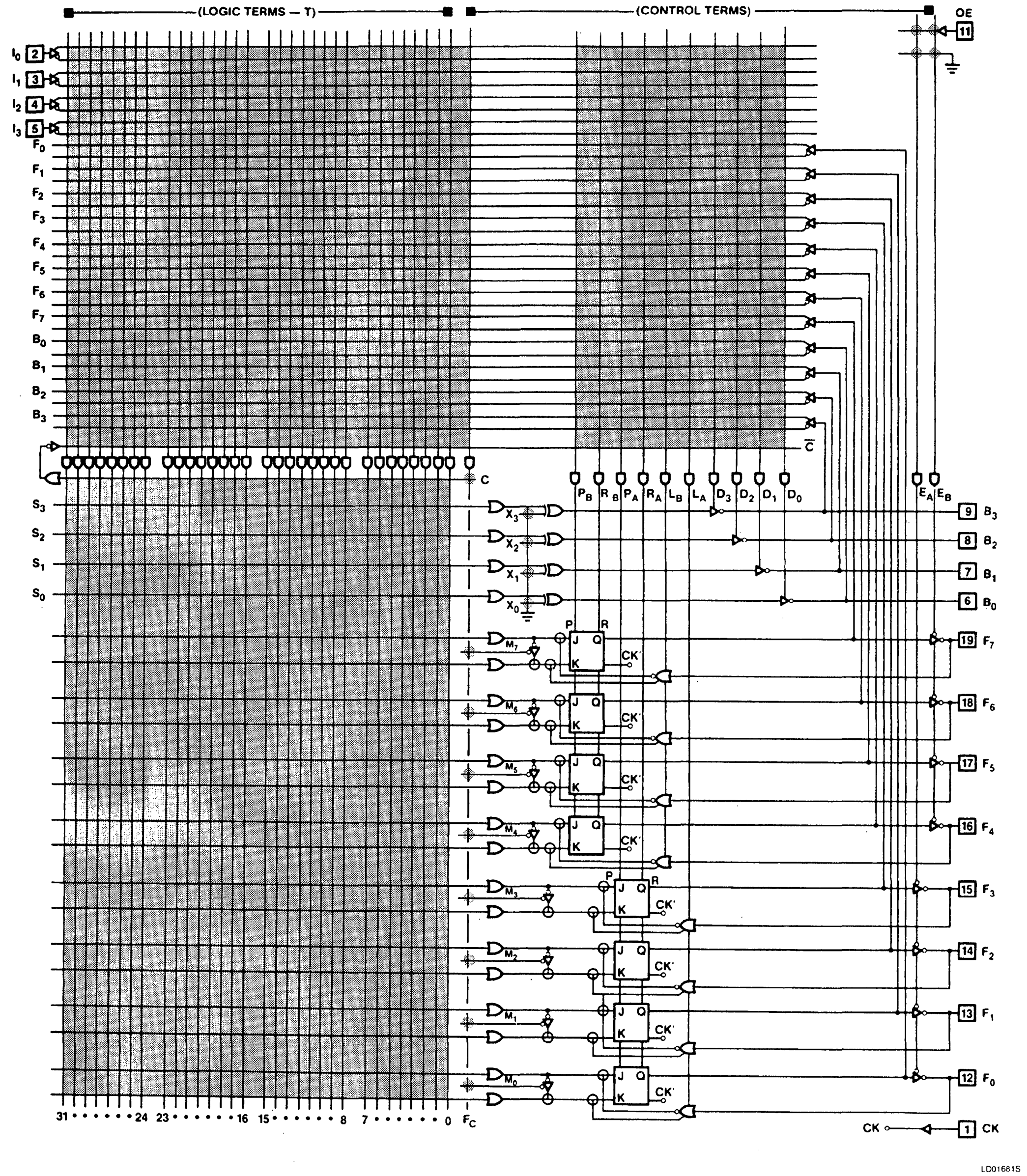
LB	—	—	—	—	—	—	—	—	—	H	H	H	H	H	H	H	H														
PA																															
RA																															
LA	—	—	—	—	—	—	—	—	—	H	H	H	H	H	H	H	H														
D3																															
D2																															
D1																															
D0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—														
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS					/ENABLE																										PLS159

TB00043S



NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.

Figure 2

Signetics

AN17
Electronic Combination Lock

Application Note

Application Specific Products

INTRODUCTION

A combination lock may be opened by entering the correct numbers which match the preset security code that may be of any number of digits. Using a PLS157, an electronic combination lock with user settable security code may be constructed. The security code may be one to five hexadecimal digits that can be preset by the user. The lock takes a 4-bit binary input as the "combination" and a "Data Valid" input, which means that the combination may be five digits long and each digit may be from 0 to F. If the input matches the preset digit of the security code, the lock will wait for the next digit. If the input does not match the corresponding digit of the security code, the lock will reset itself to the first digit position again. The user may use as many as five digits for the combination which may be set by using five DIP switches or other means. The lock may be used in conjunction with a 4-bit binary encoded rotary switch, or an encoded push button key pad, or an optical card reader, or a magnetic strip reader. The design takes advantage of the six JK flip-flops of the PLS157, the bidirectional I/O's, the complement array, and the general architecture of common product terms.

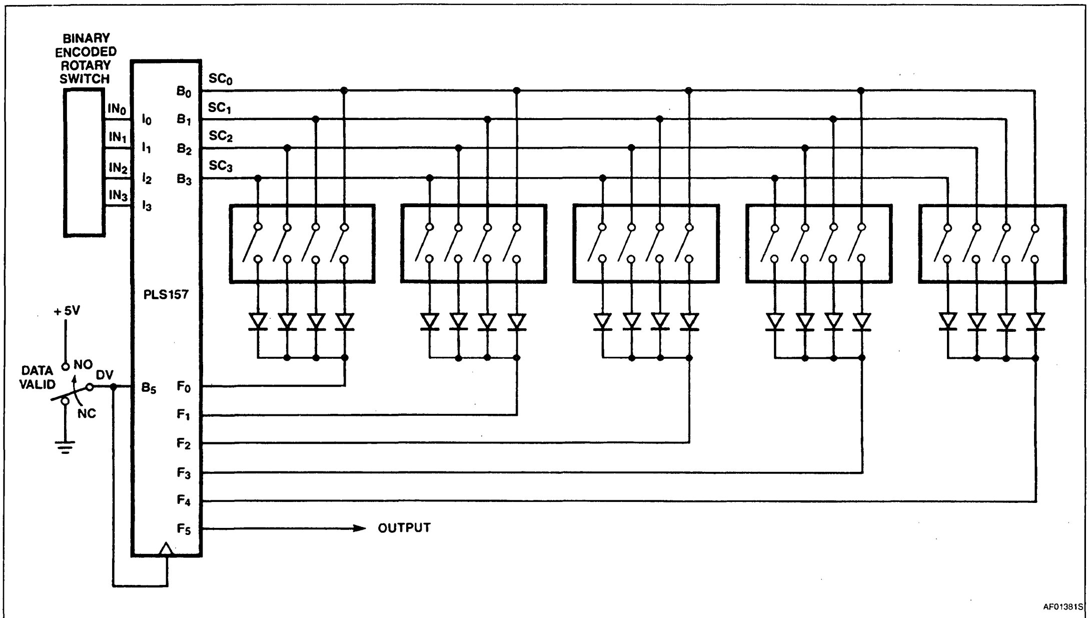
DESCRIPTION

Figure 1 shows an example of an electronic lock which uses five DIP switches to set the security code (hexadecimal 0 to E, F is reserved for reset), a 4-bit binary encoded rotary switch to enter the combination at I_0 to I_3, and a single pole double throw push button switch, "Data Valid", as the clock which is debounced by the associated circuitry of pin B_5. The security code is set with five DIP switches which are connected to a four line input ($B(I)_0$ to $B(I)_3$). The five DIP switches are multiplexed by the outputs of the flip-flops, F_0 to F_4. In normal operation, one of the F/F outputs is Low (the content of the register being a "1") while the other five are High. The operation is actually a shift register with a zero bit shifting through five one's. Therefore only one DIP switch is pulled Low (selected) at any one time while the rest is deselected. The pin named "MATCH", $B(O)_4$, is an I/O which outputs a High if the input matches the corresponding digit of the security code, otherwise it outputs a Low. A High output of $B(O)_4$ enables the shift register to shift one position while a Low causes the shift register to reset to the starting position which is a "1" in F/F_0 (flip-flop 0) (F_0 is Low due the output inverter) and "0's" in the other five (F_1 to F_5 = High). The state diagram of the design is as shown in Figure 2 where the state numbers are expressed in two hexadecimal digits. The least significant digit consists of F_3, F_2, F_1, and F_0; whereas the most significant digit consists of F_5, and F_4. At the top of the state diagram, the power-up and reset state is 00 hex. When the outputs have more than one Low, as sometimes happens during power-up, the circuit automatically resets the registers to 00 hex which causes all outputs to be High in order to prevent more than one DIP switch being enabled. After power-up or reset, pushing the "Data Valid" button will initialize the circuit to have the first digit of the security code enabled. Subsequently, any false entry will cause the circuit to go back to the initialized state of 01 hex. When the first digit is correctly set and the "Data Valid" button pressed, the circuit goes to 02 hex and the second DIP switch is enabled while the first DIP switch is disabled. The circuit is now ready for the second digit. By repeating the process, the circuit keeps shifting the "1" in the shift register until it reaches F/F_5 at which time the Low output may be used to trigger a solenoid. If at any time of the sequence, an incorrect digit is entered, the circuit reverts back to the initialized state of 01 hex.

Notice that any of the five outputs from F_1 to F_5 may be used as an output. Therefore, if, for example, a two digit security code is used, only two DIP switches are needed and the output is taken from F_2 to trigger a solenoid. After the last digit has been entered, all DIP switches are deselected and the inputs $B(I)_0$ to $B(I)_3$ become 1111 binary, or F hex. Therefore, the hex number F is not used as a valid code but as an initialization input entered at I_0 to I_3. When the hex number F is entered, the circuit initializes itself to the 01 hex state. After the last digit of the security code has been entered, if the "Data Valid" button is pressed again, the circuit sees a false entry and reinitializes itself.

The design is implemented using a PLS157 as shown in Table 1, H/L Programming Table of Electronic Lock. P-terms 0 to 14 are programmed as decoders. If an input matches the corresponding digit of the security code, one of the p-terms will be active which causes $B(O)_4$ to output a High which, in turn, enables the registers to shift to the next digit by terms 16 to 20. In the event that an incorrect input is entered, $B(O)_4$ outputs a Low which, in turn, causes the registers to be set 000001 binary by term 21. If an input of F is entered, term 15 causes the registers to be 000001. Terms 22 to 29 and RB ensure that no more than one register is "1" at a time. Terms 22 to 28 are connected to the complement array, which in turn, drives terms 29 and RB to set the registers to 000000 when terms 22 to 28 are inactive.

Electronic Combination Lock | AN17



NOTES:
1. All diodes are Philips BAT81 Schottky diodes or equivalent.
2. Single pole double throw momentary switch.

Figure 1. Simple Block Diagram of Electronic Lock

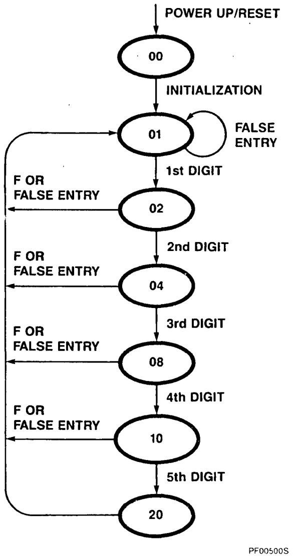


Figure 2. State Diagram of Electronic Lock

Table 1. PLS157 H/L Programming Table

				F/F MODE		EA : EB		POLARITY	
				• • • • • •				H H H H H H	
	AND				REMARKS	OR			REMARKS
		I	B(I)	Q(P)		Q(N)	P R	B(O)	
T#	C	3 2 1 0	5 4 3 2 1 0	5 4 3 2 1 0		5 4 3 2 1 0	A A	5 4 3 2 1 0	
00	-	L L L L	- - L L L L	- - - - - -	0	- - - - - -	• •	• A • • • •	B4 = 1 IF
01	-	L L L H	- - L L L H	- - - - - -	1	- - - - - -	• •	• A	INPUT MATCHES
02	-	L L H L	- - L L H L	- - - - - -	2	- - - - - -	• •	• A	SECURITY CODE:
03	-	L L H H	- - L L H H	- - - - - -	3	- - - - - -	• •	• A	
04	-	L H L L	- - L H L L	- - - - - -	4	- - - - - -	• •	• A	
05	-	L H L H	- - L H L H	- - - - - -	5	- - - - - -	• •	• A	
06	-	L H H L	- - L H H L	- - - - - -	6	- - - - - -	• •	• A	
07	-	L H H H	- - L H H H	- - - - - -	7	- - - - - -	• •	• A	
08	-	H L L L	- - H L L L	- - - - - -	8	- - - - - -	• •	• A	
09	-	H L L H	- - H L L H	- - - - - -	9	- - - - - -	• •	• A	
10	-	H L H L	- - H L H L	- - - - - -	A	- - - - - -	• •	• A	
11	-	H L H H	- - H L H H	- - - - - -	B	- - - - - -	• •	• A	
12	-	H H L L	- - H H L L	- - - - - -	C	- - - - - -	• •	• A	
13	-	H H L H	- - H H L H	- - - - - -	D	- - - - - -	• •	• A	
14	-	H H H L	- - H H H L	- - - - - -	E	- - - - - -	• •	• A	
15	-	H H H H	- - - - - -	- - - - - -	F	L L L L L H	• •	• •	INITIALIZE TO 000001
16	-	- - - -	- H - - - -	L L L L L H		L L L L H L	• •	• •	SHIFT RIGHT
17	-	- - - -	- H - - - -	L L L L H L		L L L H L L	• •	• •	
18	-	- - - -	- H - - - -	L L L H L L		L L H L L L	• •	• •	
19	-	- - - -	- H - - - -	L L H L L L		L H L L L L	• •	• •	
20	-	- - - -	- H - - - -	L H L L L L		H L L L L L	• •	• •	
21	-	- - - -	- L - - - -	- - - - - -	B4=0, FALSE ENTRY	L L L L L H	• •	• •	INITIALIZE
22	A	- - - -	- - - - - -	L L L L L L	IF ALL F/F = 0	- - - - - -	• •	• •	
23	A	- - - -	- - - - - -	L L L L L H	or more than 1	- - - - - -	• •	• •	
24	A	- - - -	- - - - - -	L L L L H L	F/F = 1	- - - - - -	• •	• •	
25	A	- - - -	- - - - - -	L L L H L L		- - - - - -	• •	• •	
26	A	- - - -	- - - - - -	L L H L L L		- - - - - -	• •	• •	
27	A	- - - -	- - - - - -	L H L L L L		- - - - - -	• •	• •	
28	A	- - - -	- - - - - -	H L L L L L		- - - - - -	• •	• •	
29	•	- - - -	- - - - - -	- - - - - -	/C = 1	- - - - - -	• A	• •	RESET F0-F3
30									
31	-	- - - -	H - - - - -	- - - - - -		- - - - - -	• •	A •	"DV" DEBOUNCE
FC									ALL F/F = JK
PB									
RB	•	- - - -	- - - - - -	- - - - - -	/C = 1	RESET F4-F5			
LB									
LA									
D5	-	- - - -	- - - - - -	- - - - - -	ENABLE B(O)5				
D4	-	- - - -	- - - - - -	- - - - - -	ENABLE B(O)4				
D3									
D2									
D1									
D0									
PIN	*	5 4 3 2	19 12 9 8 7 6	18 17 16 15 14 13		18 17 16 15 14 13		19 12 9 8 7 6	
NAME		IN3 IN2 IN1 IN0	DV - - SC3 SC2 SC1 SC0			SW5 SW4 SW3 SW2 SW1 SW0		- MATCH	

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Signetics

Application Specific Products

AN18
Schmitt Trigger Using PLS153 and PLS159

Application Note

INTRODUCTION

One of the many features of the PLS153 to 159 series is the availability of individually controlled Tri-state I/O pins. Taking advantage of this feature, a Schmitt trigger may be constructed using one input pin, two bidirectional I/O pins and additional components of three resistors. The two threshold voltages, as well as the hysterisis, are determined by the values of the three resistors and the parameters of the PLS153/159 device, which are 1) input threshold voltage, V_{TH}, 2) High output voltage, V_{OH}, and 3) Low output voltage, V_{OL}. The circuit may be simplified if Schmitt function is needed only on Low going High or High going Low, and if the hysterisis and threshold voltages are not important.

DESCRIPTION

A simplified block diagram of a non-inverting Schmitt trigger is shown in Figure 1 where R_1, R_2, and R_1, R_3, form two pairs of voltage dividers one of which get into action at input voltage direction of High going Low and the other Low going High. Assuming that input voltage starts at zero volt, the output voltage is therefore at V_{OL} which causes Q_2 to pull R_3 towards ground. As the input voltage increases, only a fraction of the voltage is impressed upon the input buffer due to the dividing network R_1 and R_3. As soon as the input voltage reaches a point where $V_1 = V_{TH}$ (V_{TH} = 1.38V typical), the output switches to V_{OH} which, in turn, turns off Q_2 and turns on Q_1. V_1 will jump to a value greater than V_{TH} and Q_1 then pulls the input pin, through R_2, towards V_{OH}, which in turn locks the output to a High state even if the input voltage fluctuates, as long as it does not fluctuate outside of the designed hysterisis. When the input voltage goes from a High to a Low, the Schmitt function repeats itself except that Q_1 and Q_2 reverse their roles.

The triggering voltages, V_H (Low going High) and V_L (High going Low) are:
$V_H = V_{TH}\ [(R_1 + R_3)/R_3] - V_{OL}\ (R_1/R_3)$;
$V_L = V_{TH}\ [(R_1 + R_2)/R_2] - V_{OH}\ (R_1/R_2)$;
where, at room temperature, V_{CC} = 5.0V, I_{OH}/I_{OL} < 1mA. V_{TH} is the threshold voltage of the device, typically 1.38V; V_{OL} is the output Low voltage of the device, typically 0.36V at $|I_{OL}|$ < 1mA; V_{OH} is the output High voltage of the device, typically 3.8V at $|I_{OH}|$ < 1mA.

The implementation of Figure 1 using PLS153/153A is as shown in Table 1, and Figure 2a. A scope photo of the operation of the circuit is shown in the Appendix. The implementation using PLS159 is shown in Table 2 and Figure 2b. In Tables 1 & 2, V_1 is the input pin, V_0 is the output pin, V_2 is the output which pulls down V_1 and V_3 is the output pin that pulls up V_1. The Schmitt output is available at pin B_0 for external use, and is available internally at the input buffers of I_0 and $B(I)_0$. However, there is a propagation delay between the two signals from the I_0 buffer and the $B(I)_0$ buffer.

An inverting Schmitt triggered buffer may be constructed using the same principle. A simple block diagram of such inverter is shown in Figure 3a. The circuit is implemented using H/L programming table as shown in Table 3 for PLS153 and Table 4 for PLS159. Table 3 is also represented in logic symbols in Figure 3b. If the voltage levels (V_L and V_H) and the hysterisis are not critical, one I/O pin may be used to pull the input pin High and Low. Therefore one I/O pin and a resistor may be saved. The drawback is that the range of V_H and V_L is quite limited. The circuit is as shown in Figure 4.

If Schmitt function is needed only in one direction, one of the resistor/output circuit may be eliminated. The circuit is as shown in Figure 5.

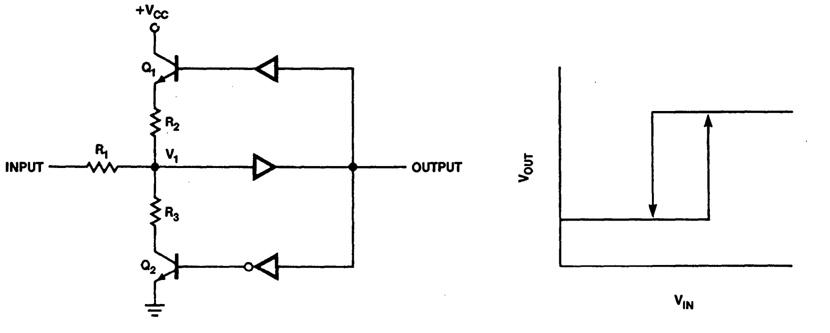

Figure 1. Simplified Block Diagram of a Schmitt Trigger

Schmitt Trigger Using PLS153 and PLS159 AN18

Table 1. PLS153/153A Programming Table

CODE NO.																				POLARITY										
																								L	H		H	H	H	
	AND																			OR										
	I								B(I)											B(O)										
TERM	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	–	–	–	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–									•	•	A	NON-INV. BUFFER
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									•	A	•	OUTPUT V_{OL}
2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–									A	•	•	OUTPUT V_{OH}
3																														
4																														
5																														
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						A	A					SAME AS
7																														TERMS 1 + 2
8																														WITH
9																														B(O)4 = V_2
10																														B(O)5 = V_3
11																														
12																														
13																														
14																														
15																														
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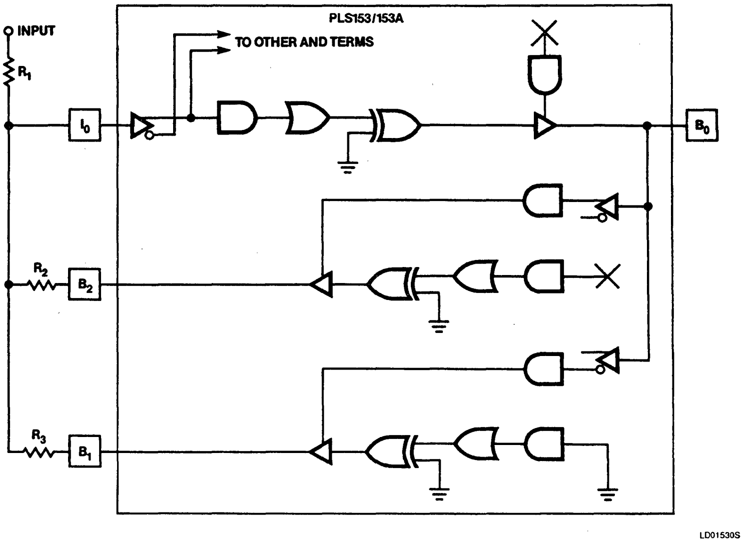
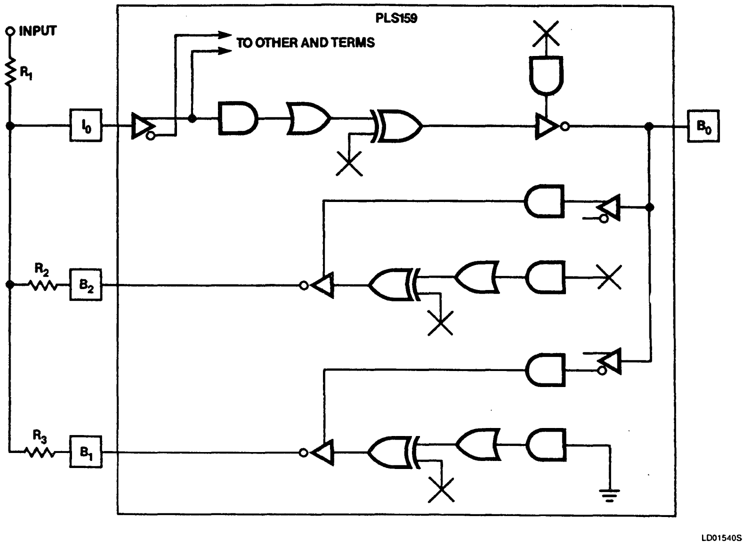
27																														
28																														
29																														
30																														
31																														
D9																														
D8																														
D7																														
D6																														
D5																														
D4																														
D3																														
D2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	H												
D1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	L												
D0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–												
PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS								V_1																			V_3	V_2	V_0	PLS153

TB01730S

NOTE:
Schmitt trigger output may be obtained from both I_0 and $B(I)_0$ to drive the AND-ARRAY.



a. Using PLS153/153A



b. Using PLS159

Figure 2. Schmitt Trigger

Schmitt Trigger Using PLS153 and PLS159

Table 2. PLS159 FPLS Programming Table

CODE NO.										FF MODE									E_B				E_A				POLARITY				
																												H	H	H	
TERM	AND																		(OR)												
	C	I				B(I)				Q(P)								REMARKS	Q(N)								B(O)				REMARKS
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	—	—	—	—	H	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—	•	•	•	A	NON-INV. BUFR
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		—	—	—	—	—	—	—	—	•	•	A	•	OUTPUT V_{OL}
2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—	•	A	•	•	OUTPUT V_{OH}
3																															
4																															
5																															
6																															
7																															
8																															
9																															
10																															
11																															
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28																															
29																															
30																															
31																															
FC																															
PB																															
RB																															
LB																															
PA																															
RA																															
LA																															
D3																															
D2	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—	—														
D1	—	—	—	—	—	—	—	—	L	—	—	—	—	—	—	—	—														
D0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—														
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS					V_1		V_3	V_2	V_0																						PLS159

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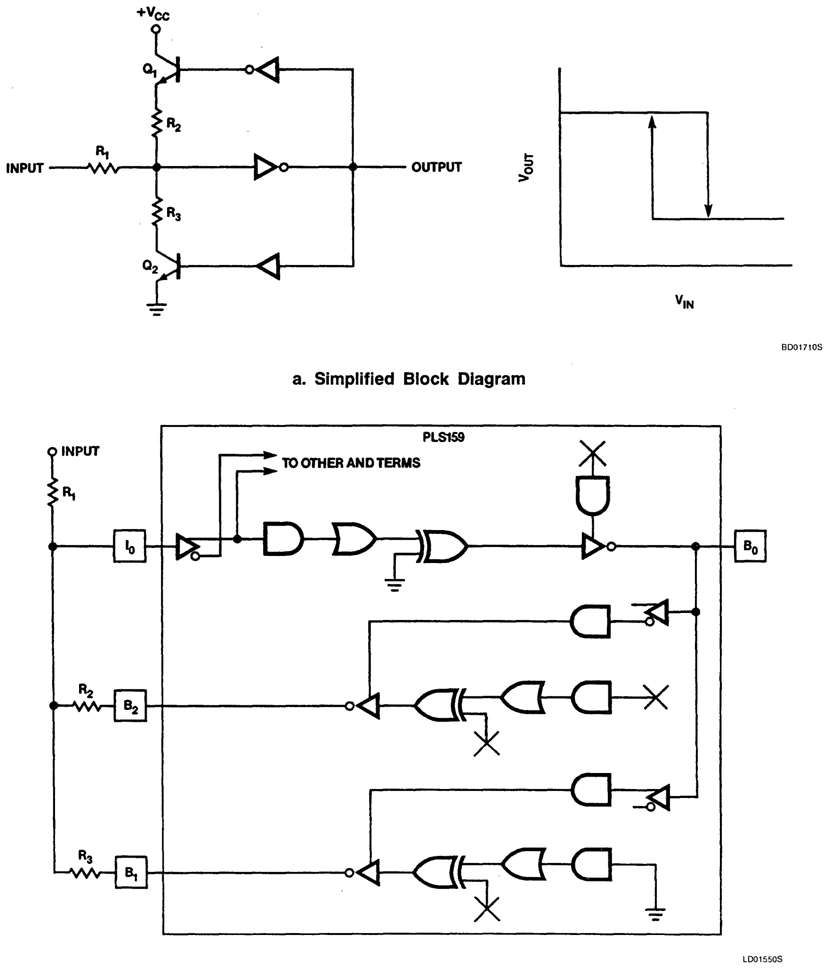
Schmitt Trigger Using PLS153 and PLS159

AN18



a. Simplified Block Diagram

b. Using PLS159

Figure 3. Inverting Schmitt Trigger

Schmitt Trigger Using PLS153 and PLS159

AN18

Table 3. PLS153/153A Programming Table

CODE NO.																				POLARITY										
																											L	L	L	
	AND																			OR										
	I								B(I)											B(O)										
TERM	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	REMARKS	9	8	7	6	5	4	3	2	1	0	REMARKS
0	–	–	–	–	–	–	–	H	–	–	–	–	–	–	–	–	–	–									•	•	A	INV. BUFFER
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									•	A	•	OUTPUT V_{OH}
2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–									A	•	•	OUTPUT V_{OL}
3																														
4																														
5																														
6																														
7																														
8																														
9																														
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30																														
31																														
D9																														
D8																														
D7																														
D6																														
D5																														
D4																														
D3																														
D2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	H												
D1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	L												
D0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–												
PN	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	11	9		19	18	17	16	15	14	13	12	11	9	
REMARKS								V_1																			V_3	V_2	V_0	PLS153

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Table 4. PLS159 FPLS Program Table

CODE NO.	FF MODE	EB	EA	POLARITY
				H H L

TERM	AND																	REMARKS	(OR)												REMARKS
	C	I				B(I)				Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	—	—	—	—	H	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—	•	•	•	A	INV. BUFFER
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		—	—	—	—	—	—	—	—	•	•	A	•	OUTPUT V_{OL}
2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—	•	A		•	OUTPUT V_{OH}
3																															
4																															
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FC																															
PB																															
RB																															
LB																															
PA																															
RA																															
LA																															
D3																															
D2	—	—	—	—	—	—	—	—	L	—	—	—	—	—	—	—	—														
D1	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—	—														
D0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—														
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	PLS159
REMARKS					V_1		V_3	V_2	V_0																						

TB01590S

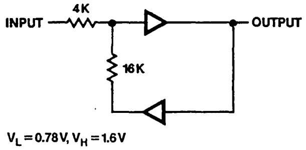
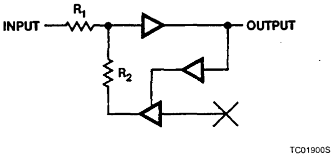
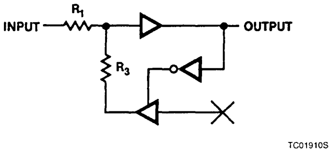


Figure 4. Schmitt Trigger Using One I/O Pin



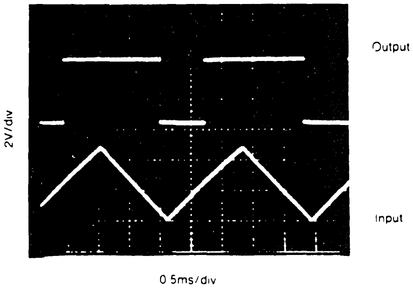
a. High Going Low Direction



b. Low Going High Direction

Figure 5. Schmitt Trigger

APPENDIX A



NOTE:
R_1 = 3.9kΩ, R_2 = 10.8kΩ, R_3 = 2.0kΩ, V_{CC} = 5.0V, Ambient temperature ≈ 25°C

Figure A-1. A Non-Inverting Schmitt Triggered Buffer

Signetics

AN19
Electronic Dice

Application Note

Application Specific Products

DESCRIPTION

A PLS159 is used to implement a pair of dice. Each die is represented by a series of six different state transitions. Two push button switches are used to "roll" the dice; in other words start/stop the state transitions. Each push button controls one die. When the switches are held low, the state transitions take place for each die and the result is displayed when a push button is released.

Each die is made up of seven LED's which are connected to the outputs of the PLS159. The system also contains its own oscillator which generates the clock cycle necessary for the state transitions.

The random release of the push button provides a random output. The high frequency of the internal oscillator and the fact that the switches are not debounced, add more "randomness" to each event.

The overall system configuration is shown in Figure 3.

LOGIC IMPLEMENTATION

The configuration of each die is shown in Figure 1, with each letter representing an LED.

To represent the numbers one through six the LED's are turned on as shown in Figure 2.

Table 1 is the truth table generated from Figure 2.

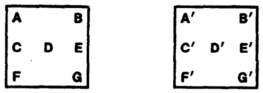


Figure 1. Dice Configuration

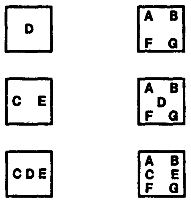


Figure 2. Number Representation

Table 1. Truth Table for Dice

	A	B	C	D	E	F	G
One	0	0	0	1	0	0	0
Two	0	0	1	0	1	0	0
Three	0	0	1	1	1	0	0
Four	1	1	0	0	0	1	1
Five	1	1	0	1	0	1	1
Six	1	1	1	0	1	1	1

The result of Table 1 is the following logic equations:

A = Four + Five + Six;
B = Four + Five + Six;
C = Two + Three + Six;
D = One + Three + Five;
E = Two + Three + Six;
F = Four + Five + Six;
G = Four + Five + Six;

As can be seen from the above logic equations:

A≡B≡F≡G;
C≡E;

Table 2 is the result of Table 1 and the above common terms.

Table 2. Truth Table for PLS159 Outputs

	A, B, F, G	C, E	D
One	0	0	1
Two	0	1	0
Three	0	1	1
Four	1	0	0
Five	1	0	1
Six	1	1	0

For each die, three outputs of the PLS159 are needed to implement the logic in Table 2. These outputs are connected to the LED's as follows:

F0: A, B, F, G;
F1: C, E;
F2: D;

Similarly for the second die:

F3: A', B', F', G';
F4: C', E';
F5: D';

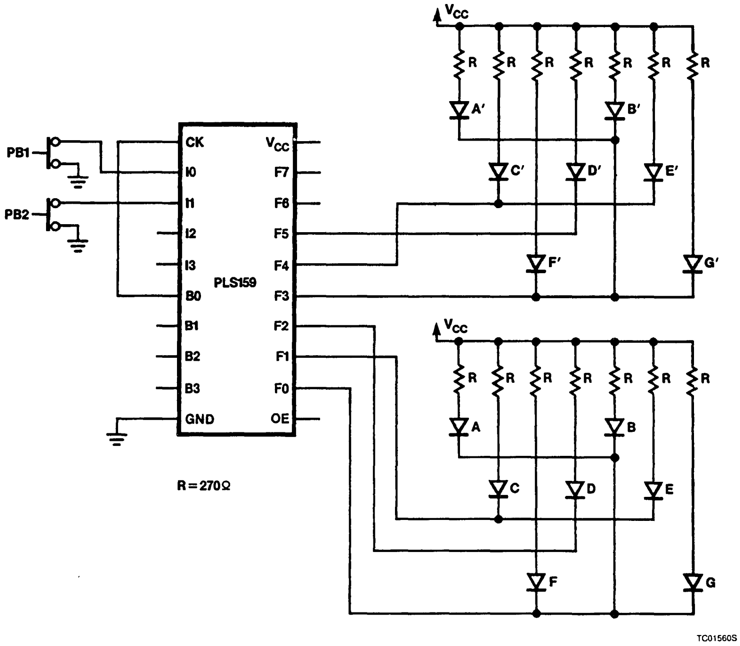


Figure 3. Dice Implementation Using the PLS159

Electronic Dice

STATE TRANSITIONS

Figure 4 shows two arbitrary state transition sequences which are used to implement each die.

These state transitions are implemented in the program table of the PLS159.

INTERNAL OSCILLATOR

An internal oscillator is also implemented for the system. The internal configuration of the oscillator is shown in Figure 5. For a detailed explanation of the implementation of this oscillator see AN13: Oscillator with the PLS159. B0 is connected externally to the clock input of the PLS159.

EXPLANATION OF PROGRAM TABLE

The program table for the two dice is shown in Table 3.

Terms 0 – 5 and 7 – 12 represent the state transitions for each die.

Terms 14 – 15 and 17 – 18 reset the flip-flops to HLL and HLH if undefined states occur, such as during power up.

Terms 20 and 21 and output controls terms D1 and D2 are used to implement the internal oscillator (see AN13).

Inputs I0 and I1 are connected to the two push button switches which roll the dice. These inputs are programmed to be Active-Low. When the push button is closed the state transitions take place, and upon release of the push button, the current states are displayed on the outputs.

The outputs of the PLS159 are inverted and this must be taken into consideration when assigning "H" and "L"s to the F0, F1, F2, F3, F4, and F5. These assignments are shown in Table 4. All the flip-flops are set to be of the J – K type.

Table 4. H And L Assignment

	F2, F5	F1, F4	F0, F3
One	H	L	L
Two	L	H	L
Three	H	H	L
Four	L	L	H
Five	H	L	H
Six	L	H	H

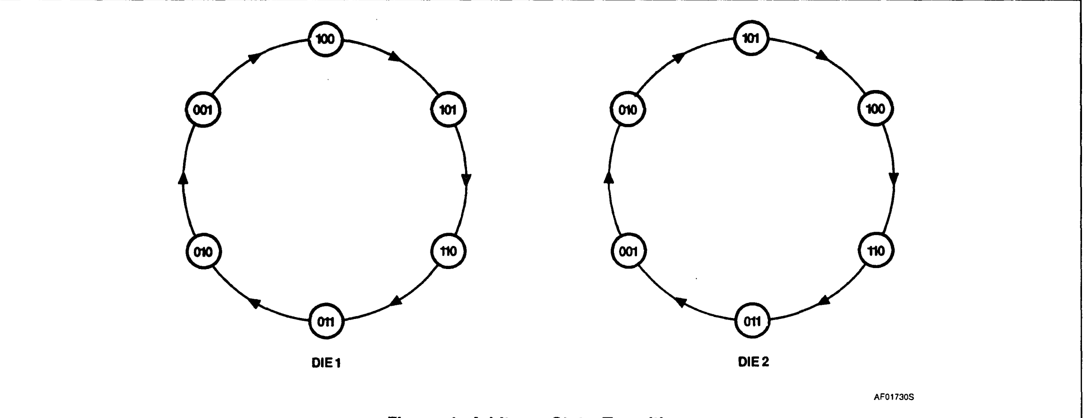


Figure 4. Arbitrary State Transitions

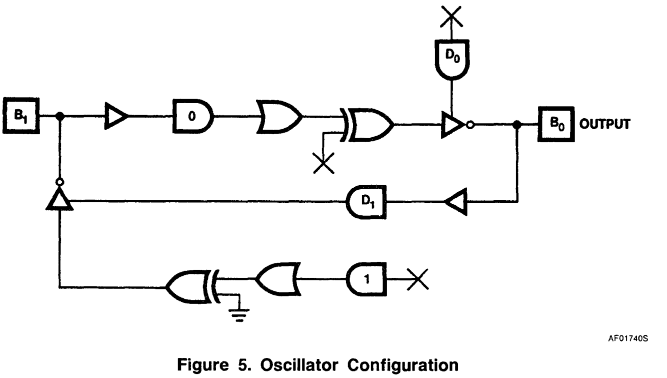


Figure 5. Oscillator Configuration

Table 3. Program Table for 2 Dice

CODE NO.										FF MODE									EB				EA				POLARITY				
										A	A	•	•	•	•	•	•		•				•				L	L	H	L	
TERM	AND																		(OR)												
	C	I				B(I)				Q(P)								REMARKS	Q(N)								B(O)				REMARKS
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	—	—	—	—	L	—	—	—	—	—	—	—	—		H	L	L	100→101	—	—	—	—	—	H	L	H	•	•	•	•	
1	—	—	—	—	L	—	—	—	—	—	—	—	—		H	L	H	101→110	—	—	—	—	—	H	H	L	•	•	•	•	
2	—	—	—	—	L	—	—	—	—	—	—	—	—		H	H	L	110→011	—	—	—	—	—	L	H	H	•	•	•	•	DIE 1
3	—	—	—	—	L	—	—	—	—	—	—	—	—		L	H	H	011→010	—	—	—	—	—	L	H	L	•	•	•	•	
4	—	—	—	—	L	—	—	—	—	—	—	—	—		L	H	L	010→001	—	—	—	—	—	L	L	H	•	•	•	•	
5	—	—	—	—	L	—	—	—	—	—	—	—	—		L	L	H	001→100	—	—	—	—	—	H	L	L	•	•	•	•	
6																															
7	—	—	—	L	—	—	—	—	—	—	—	H	L	H	—	—	—	101→100	—	—	H	L	L	—	—	—	•	•	•	•	
8	—	—	—	L	—	—	—	—	—	—	—	H	L	L	—	—	—	100→110	—	—	H	H	L	—	—	—	•	•	•	•	
9	—	—	—	L	—	—	—	—	—	—	—	H	H	L	—	—	—	110→011	—	—	L	H	H	—	—	—	•	•	•	•	DIE 2
10	—	—	—	L	—	—	—	—	—	—	—	L	H	H	—	—	—	011→001	—	—	L	L	H	—	—	—	•	•	•	•	
11	—	—	—	L	—	—	—	—	—	—	—	L	L	H	—	—	—	001→010	—	—	L	H	L	—	—	—	•	•	•	•	
12	—	—	—	L	—	—	—	—	—	—	—	L	H	L	—	—	—	010→101	—	—	H	L	H	—	—	—	•	•	•	•	
13																															
14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	L	L	Undefined	—	—	—	—	—	H	L	L	•	•	•	•	Go to 100
15	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	H	H	states for DIE 1	—	—	—	—	—	H	L	L	•	•	•	•	
16																															
17	—	—	—	—	—	—	—	—	—	—	—	L	L	L	—	—	—	Undefined	—	—	—	H	L	H	—	—	•	•	•	•	Go to 101
18	—	—	—	—	—	—	—	—	—	—	—	H	H	H	—	—	—	states for DIE 2	—	—	—	H	L	H	—	—	•	•	•	•	
19																															
20	—	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—	—	Oscillator	—	—	—	—	—	—	—	—	•	•	A	•	$B_0 = B_1$
21	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—	•	•	•	A	$B(O)_1$ = Low
22																															
23																															
24																															
25																															
26																															
27																															
28																															
29																															
30																															
31																															
FC																															
PB																															
RB																															
LB																															
PA																															
RA																															
LA																															
D3																															
D2																															
D1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Enable $B(O)1$													
D0	—	—	—	—	—	—	—	H	—	—	—	—	—	—	—	—	—	Enable $B(O)0$ for term 20													
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS																															

PLS159

TB00622S

Signetics

Application Specific Products

AN21
9-Bit Parity Generator/Checker With 82S153/153A

Application Note

INTRODUCTION

This application note presents the design of a parity generator using Signetics PLD, 82S153 or 82S153A, which enables the designers to customize their circuits in the form of "sum-of-products". The PLA architecture and the 10 bi-directional I/O's make it possible to implement the 9-bit parity generator/checker in one chip without any external wiring between pins. A logic diagram of the device is shown in Appendix A.

The parity of an 8-bit word is generated by counting the number of "1's" in the word. If the number is odd, the word has odd parity. If the number is even, the word has even parity. Thus, a parity generator designed for even parity, for example, will generate a "0" if the parity is even, or a "1" if parity is odd. Conversely, an odd parity generator will generate a "0" if the parity of the word is odd, or a "1" if the parity is even. This bit is then concatinated to the word making it 9-bits long. When the word is used elsewhere, its parity may be checked for correctness.

FEATURES

- **Generates even and odd parities (SUM_E and SUM_O)**
- **SUM_E = "1" for even parity, "0" for odd parity**
- **SUM_O = "1" for odd parity, "0" for even parity**
- **Generate parity or check for parity errors**
- **Cascaded to expand word length**

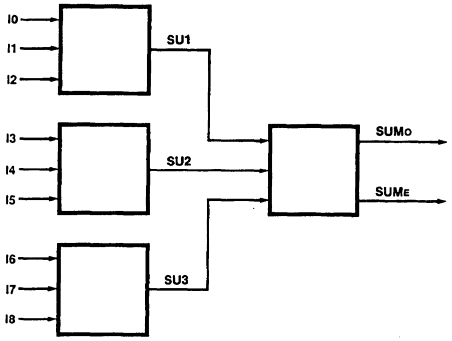
DESCRIPTION

The most straight forward way of implementing the parity generator/checker is to take the 9-input truth table (8 inputs for the 8-bit word, and 1 input for cascading the previous stage) and put it in a 256 × 4 PROM. Since there are 2^9 combinations and half of them is odd, the other half is even, the circuit will take 256 terms. An alternative is to divide the 9-bits into 3 groups of 3-bits as shown in Figure 1. If the sum of the 3-bits is odd, then the intermediate output SU1, or SU2, or SU3 equals 1. Otherwise it equals 0. The intermediate results are grouped together and SUM_O becomes "1" if the sum is odd, otherwise SUM_O equals "0". The circuit is implemented using AMAZE as shown in Figure 3. SU1 is an intermediate output for inputs I_0, I_1 and I_2. In the same manner, SU2 and SU3 are intermediate outputs for I_3, I_4, I_5 and I_6, I_7, I_8. The design uses up 16 product terms and 5 control terms leaving 16 product terms and 4 bi-directional I/O's to implement other logic designs.

The design is tested by using the logic simulator provided by AMAZE. The input test vector is chosen to exhaustively test for all 8 input combinations at all 4 sections of the circuit.

9-Bit Parity Generator/Checker With 82S153/153A

AN21



BD01670S

I_0	I_1	I_2	SU1
0	0	0	0
0	0	1	1
0	1	1	0
0	1	0	1
1	0	1	0
1	0	0	1
1	1	0	0
1	1	1	1

I_3	I_4	I_5	SU2
0	0	0	0
0	1	1	0
0	0	1	1
0	1	0	1
1	0	1	0
1	1	0	0
1	0	0	1
1	1	1	1

I_6	I_7	I_8	SU3
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	0
0	0	1	1
0	1	0	1
1	0	0	1
1	1	1	1

SU1	SU2	SU3	SUM_O	SUM_E
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Figure 1. Block Diagram of 9-Bit Parity Generator/Checker

```
 ******************** PARGEN ********************
###################### P I N   L I S T ######################

      LABEL     ** FNC **PIN ---------- PIN** FNC **     LABEL
I0              ** I    **   1-:         :-20 ** +5V **VCC
I1              ** I    **   2-:         :-19 ** /O  **SUME
I2              ** I    **   3-:         :-18 ** O   **SUMO
I3              ** I    **   4-:    8    :-17 ** B   **N/C
I4              ** I    **   5-:    2    :-16 ** B   **N/C
I5              ** I    **   6-:    S    :-15 ** B   **N/C
I6              ** I    **   7-:    1    :-14 ** B   **N/C
I7              ** I    **   8-:    5    :-13 ** O   **SU3
I8              ** I    **   9-:    3    :-12 ** O   **SU2
GND             ** OV   **  10-:         :-11 ** O   **SU1
                              ----------
```

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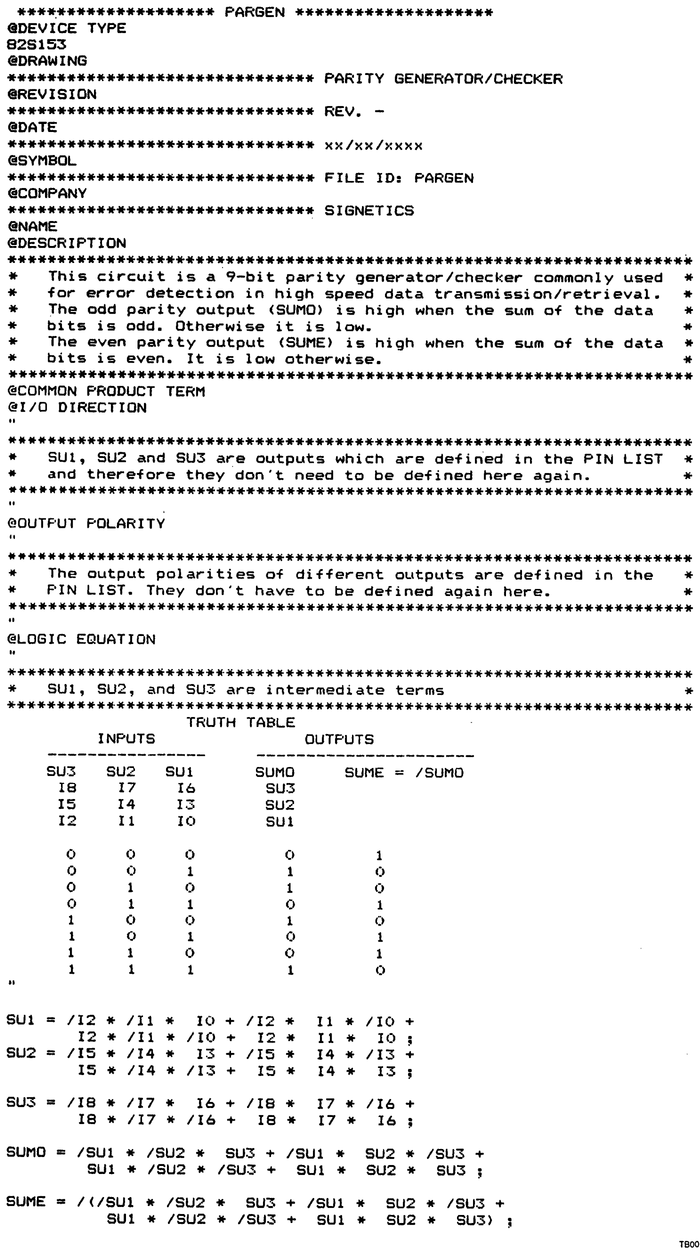
Figure 2. Pin List

9-Bit Parity Generator/Checker With 82S153/153A — AN21



```
 ******************** PARGEN ********************
@DEVICE TYPE
82S153
@DRAWING
******************************** PARITY GENERATOR/CHECKER
@REVISION
******************************** REV. -
@DATE
******************************** xx/xx/xxxx
@SYMBOL
******************************** FILE ID: PARGEN
@COMPANY
******************************** SIGNETICS
@NAME
@DESCRIPTION
*********************************************************************
*   This circuit is a 9-bit parity generator/checker commonly used  *
*   for error detection in high speed data transmission/retrieval.  *
*   The odd parity output (SUMO) is high when the sum of the data   *
*   bits is odd. Otherwise it is low.                               *
*   The even parity output (SUME) is high when the sum of the data  *
*   bits is even. It is low otherwise.                              *
*********************************************************************
@COMMON PRODUCT TERM
@I/O DIRECTION
"
*********************************************************************
*   SU1, SU2 and SU3 are outputs which are defined in the PIN LIST  *
*   and therefore they don't need to be defined here again.         *
*********************************************************************
"
@OUTPUT POLARITY
"
*********************************************************************
*   The output polarities of different outputs are defined in the   *
*   PIN LIST. They don't have to be defined again here.             *
*********************************************************************
"
@LOGIC EQUATION
"
*********************************************************************
*   SU1, SU2, and SU3 are intermediate terms                        *
*********************************************************************
                  TRUTH TABLE
         INPUTS                    OUTPUTS
    ---------------          ---------------------
    SU3    SU2    SU1        SUMO     SUME = /SUMO
    I8     I7     I6         SU3
    I5     I4     I3         SU2
    I2     I1     I0         SU1

     0      0      0          0         1
     0      0      1          1         0
     0      1      0          1         0
     0      1      1          0         1
     1      0      0          1         0
     1      0      1          0         1
     1      1      0          0         1
     1      1      1          1         0
"

SU1 = /I2 * /I1 *  I0 + /I2 *  I1 * /I0 +
       I2 * /I1 * /I0 +  I2 *  I1 *  I0 ;
SU2 = /I5 * /I4 *  I3 + /I5 *  I4 * /I3 +
       I5 * /I4 * /I3 +  I5 *  I4 *  I3 ;

SU3 = /I8 * /I7 *  I6 + /I8 *  I7 * /I6 +
       I8 * /I7 * /I6 +  I8 *  I7 *  I6 ;

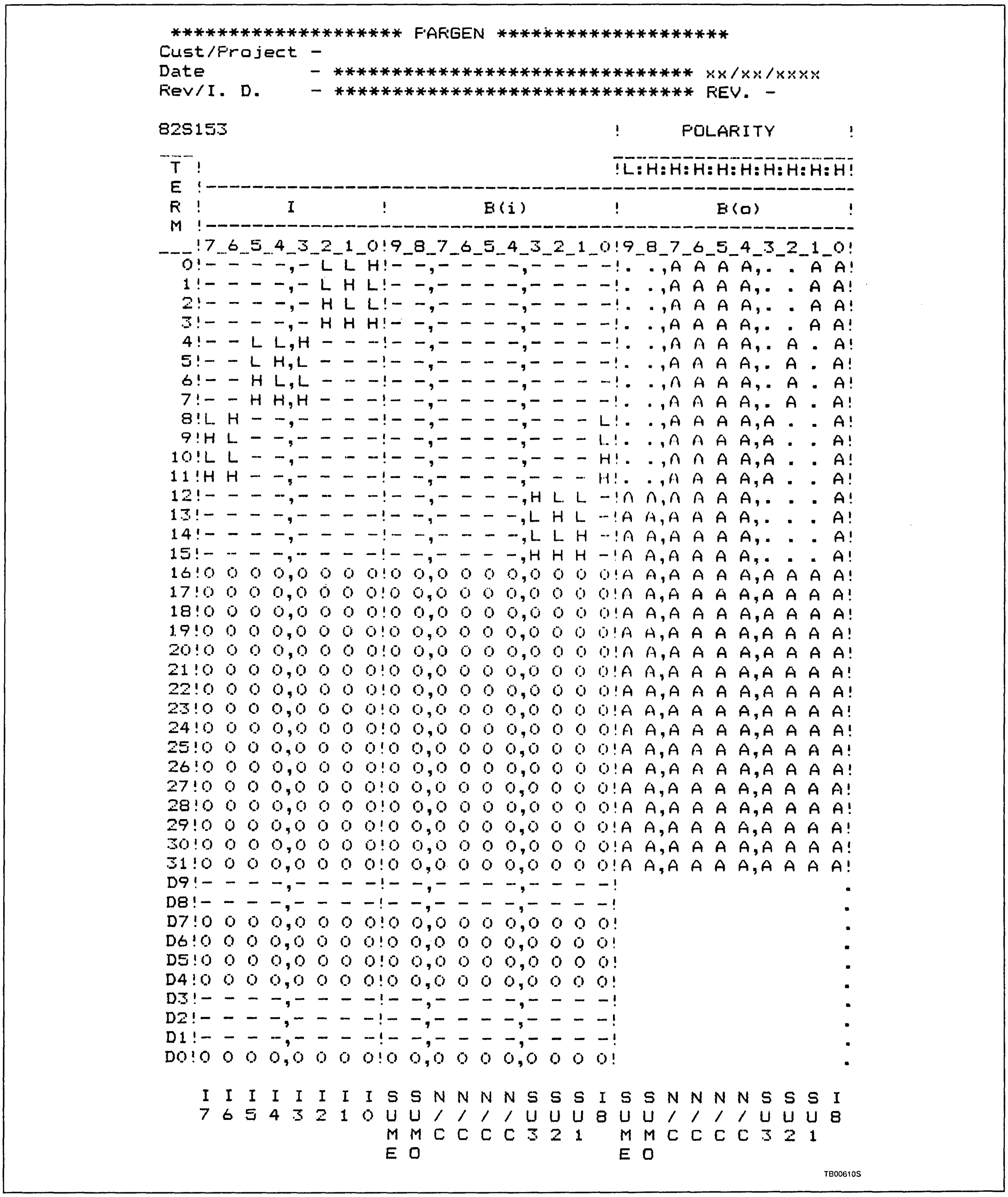
SUMO = /SU1 * /SU2 *  SU3 + /SU1 *  SU2 * /SU3 +
        SU1 * /SU2 * /SU3 +  SU1 *  SU2 *  SU3 ;

SUME = /(/SU1 * /SU2 *  SU3 + /SU1 *  SU2 * /SU3 +
          SU1 * /SU2 * /SU3 +  SU1 *  SU2 *  SU3) ;
```

TB00580S

Figure 3. AMAZE Implementation of the Parity Generator/Checker Circuit

Table 1. Programming Table

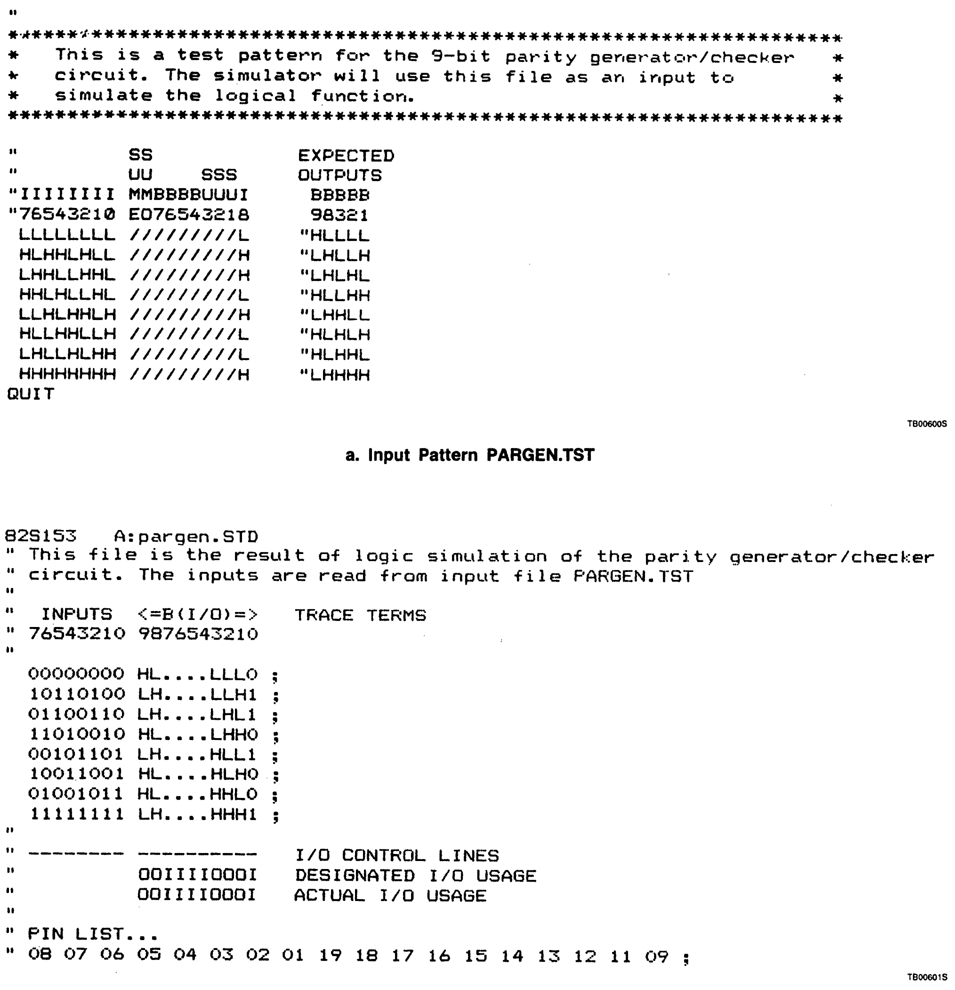


```
    ******************** FARGEN ********************
Cust/Project -
Date         - ******************************** xx/xx/xxxx
Rev/I. D.    - ******************************** REV. -

82S153                                 !     POLARITY      !
---                                     -------------------
 T !                                   !L:H:H:H:H:H:H:H:H:H!
 E !---------------------------------------------------------
 R !       I       !        B(i)       !       B(o)        !
 M !---------------------------------------------------------
___!7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!- - - -,- L L H!- -,- - - -,- - - -!. .,A A A A,. . A A!
  1!- - - -,- L H L!- -,- - - -,- - - -!. .,A A A A,. . A A!
  2!- - - -,- H L L!- -,- - - -,- - - -!. .,A A A A,. . A A!
  3!- - - -,- H H H!- -,- - - -,- - - -!. .,A A A A,. . A A!
  4!- - L L,H - - -!- -,- - - -,- - - -!. .,A A A A,. A . A!
  5!- - L H,L - - -!- -,- - - -,- - - -!. .,A A A A,. A . A!
  6!- - H L,L - - -!- -,- - - -,- - - -!. .,A A A A,. A . A!
  7!- - H H,H - - -!- -,- - - -,- - - -!. .,A A A A,. A . A!
  8!L H - -,- - - -!- -,- - - -,- - - L!. .,A A A A,A . . A!
  9!H L - -,- - - -!- -,- - - -,- - - L!. .,A A A A,A . . A!
 10!L L - -,- - - -!- -,- - - -,- - - H!. .,A A A A,A . . A!
 11!H H - -,- - - -!- -,- - - -,- - - H!. .,A A A A,A . . A!
 12!- - - -,- - - -!- -,- - - -,H L L -!A A,A A A A,. . . A!
 13!- - - -,- - - -!- -,- - - -,L H L -!A A,A A A A,. . . A!
 14!- - - -,- - - -!- -,- - - -,L L H -!A A,A A A A,. . . A!
 15!- - - -,- - - -!- -,- - - -,H H H -!A A,A A A A,. . . A!
 16!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 17!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 18!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 19!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 23!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 25!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 27!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 31!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 D9!- - - -,- - - -!- -,- - - -,- - - -!                  .
 D8!- - - -,- - - -!- -,- - - -,- - - -!                  .
 D7!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D6!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D5!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D4!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D3!- - - -,- - - -!- -,- - - -,- - - -!                  .
 D2!- - - -,- - - -!- -,- - - -,- - - -!                  .
 D1!- - - -,- - - -!- -,- - - -,- - - -!                  .
 D0!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .

    I I I I I I I I S S N N N N S S S I S S N N N N S S S I
    7 6 5 4 3 2 1 0 U U / / / / U U U 8 U U / / / / U U U 8
                    M M C C C C 3 2 1   M M C C C C 3 2 1
                    E O                 E O
```

TB00610S



```
"
*********************************************************************
*   This is a test pattern for the 9-bit parity generator/checker   *
*   circuit. The simulator will use this file as an input to        *
*   simulate the logical function.                                  *
*********************************************************************

"          SS            EXPECTED
"          UU    SSS     OUTPUTS
"IIIIIIII MMBBBBUUUI      BBBBB
"76543210 E076543218      98321
 LLLLLLLL /////////L     "HLLLL
 HLHHLHLL /////////H     "LHLLH
 LHHLLHHL /////////H     "LHLHL
 HHLHLLHL /////////L     "HLLHH
 LLHLHHLH /////////H     "LHHLL
 HLLHHLLH /////////L     "HLHLH
 LHLLHLHH /////////L     "HLHHL
 HHHHHHHH /////////H     "LHHHH
QUIT
```

TB00600S

a. Input Pattern PARGEN.TST

```
82S153    A:pargen.STD
" This file is the result of logic simulation of the parity generator/checker
" circuit. The inputs are read from input file PARGEN.TST
"
"  INPUTS  <=B(I/O)=>   TRACE TERMS
" 76543210 9876543210
"
  00000000 HL....LLLO ;
  10110100 LH....LLH1 ;
  01100110 LH....LHL1 ;
  11010010 HL....LHHO ;
  00101101 LH....HLL1 ;
  10011001 HL....HLHO ;
  01001011 HL....HHLO ;
  11111111 LH....HHH1 ;
"
" -------- ----------   I/O CONTROL LINES
"          OOIIIIOOOI   DESIGNATED I/O USAGE
"          OOIIIIOOOI   ACTUAL I/O USAGE
"
" PIN LIST...
" 08 07 06 05 04 03 02 01 19 18 17 16 15 14 13 12 11 09 ;
```

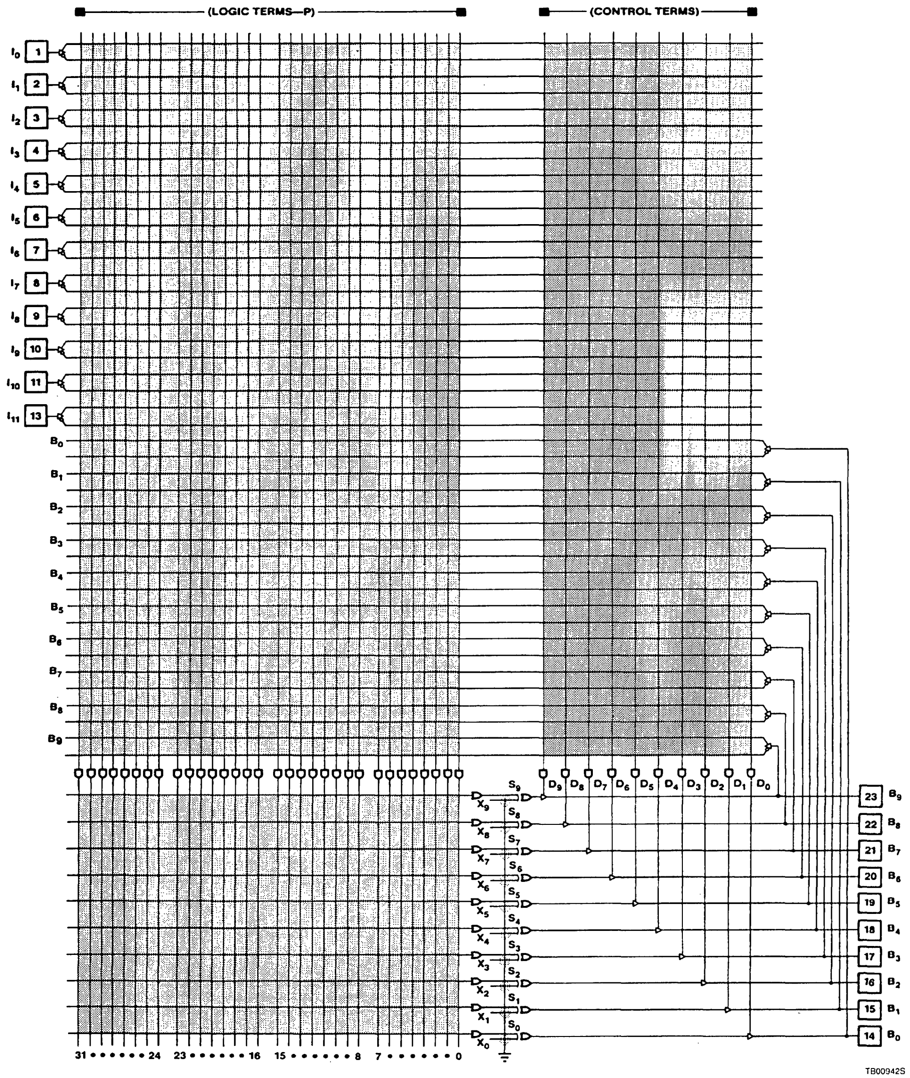
TB00601S

b. Output File From SIMULATOR

Figure 4. Test Vectors

9-Bit Parity Generator/Checker With 82S153/153A AN21

APPENDIX A



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

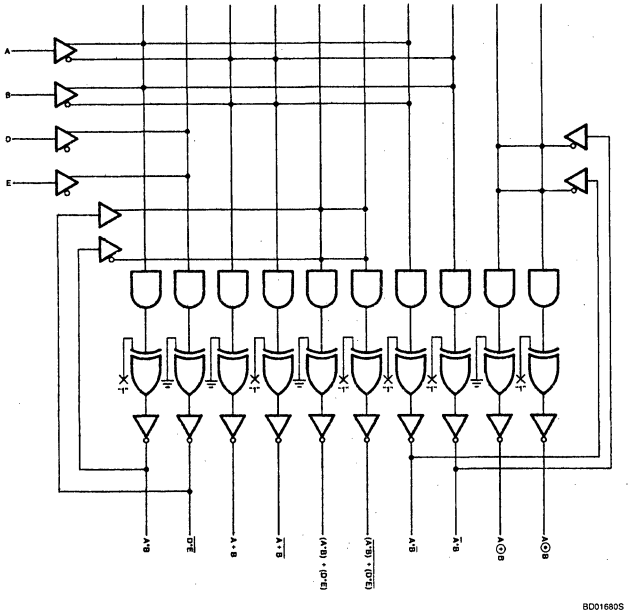
Figure A-1. FPLA Logic Diagram

Signetics

Application Specific Products

AN22
PLS151 Toolkit

Application Note



a. Basic Gates Configuration

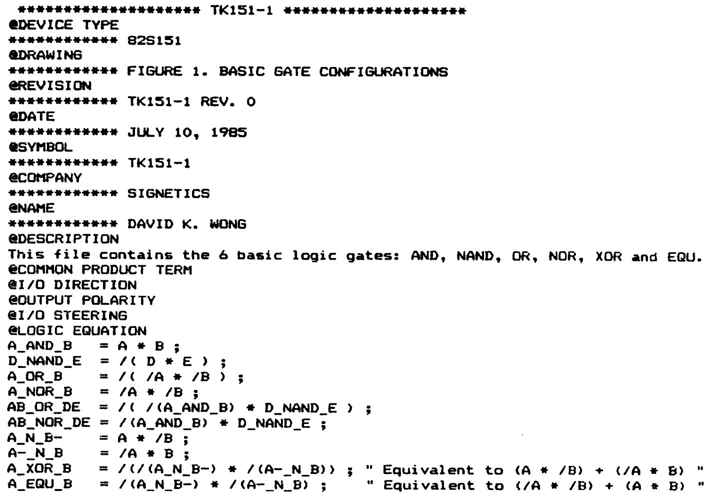
```
 ******************** TK151-1 ********************
####################### P I N   L I S T #######################

   LABEL      ** FNC **PIN ---------- PIN** FNC **     LABEL
A             ** I   **  1-:          :-20 ** +5V **VCC
B             ** I   **  2-:          :-19 ** O   **A_NOR_B
D             ** I   **  3-:          :-18 ** /O  **A_OR_B
E             ** I   **  4-:    8     :-17 ** /O  **D_NAND_E
N/C           ** I   **  5-:    2     :-16 ** O   **A_AND_B
N/C           ** I   **  6-:    S     :-15 ** /O  **AB_OR_DE
N/C           ** /B  **  7-:    1     :-14 ** O   **AB_NOR_DE
N/C           ** /B  **  8-:    5     :-13 ** /O  **A_XOR_B
A-_N_B        ** O   **  9-:    1     :-12 ** O   **A_EQU_B
GND           ** OV  ** 10-:          :-11 ** O   **A_N_B-
                         ----------
```

TB00640S

b. Pin List

Figure 1



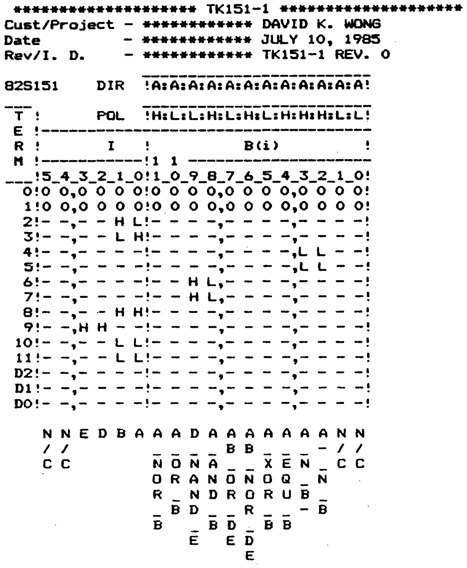
```
******************** TK151-1 ********************
@DEVICE TYPE
************ 82S151
@DRAWING
************ FIGURE 1. BASIC GATE CONFIGURATIONS
@REVISION
************ TK151-1 REV. 0
@DATE
************ JULY 10, 1985
@SYMBOL
************ TK151-1
@COMPANY
************ SIGNETICS
@NAME
************ DAVID K. WONG
@DESCRIPTION
This file contains the 6 basic logic gates: AND, NAND, OR, NOR, XOR and EQU.
@COMMON PRODUCT TERM
@I/O DIRECTION
@OUTPUT POLARITY
@I/O STEERING
@LOGIC EQUATION
A_AND_B    = A * B ;
D_NAND_E   = /( D * E ) ;
A_OR_B     = /( /A * /B ) ;
A_NOR_B    = /A * /B ;
AB_OR_DE   = /( /(A_AND_B) * D_NAND_E ) ;
AB_NOR_DE  = /(A_AND_B) * D_NAND_E ;
A_N_B-     = A * /B ;
A-_N_B     = /A * B ;
A_XOR_B    = /(/(A_N_B-) * /(A-_N_B)) ; " Equivalent to (A * /B) + (/A * B) "
A_EQU_B    = /(A_N_B-) * /(A-_N_B) ;    " Equivalent to (/A * /B) + (A * B) "
```

TB00630S

c. Boolean Equations of Basic Gate Configurations

Figure 1 (Continued)

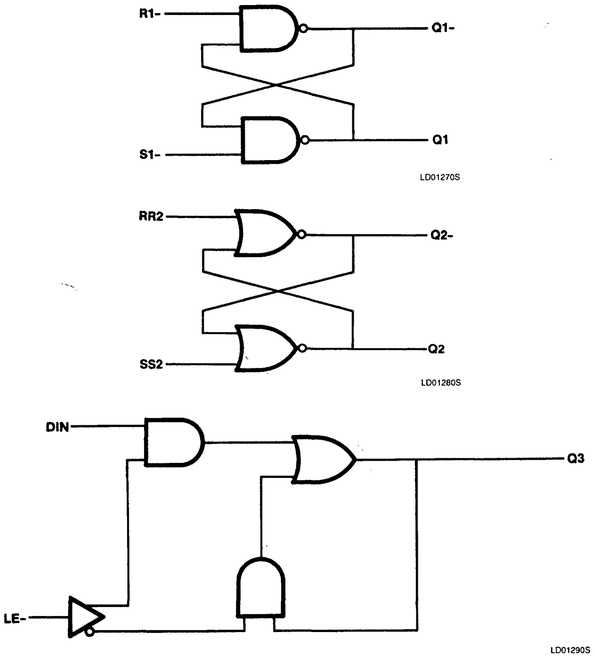
Table 1. Program Table of Basic Gate Configurations



```
******************** TK151-1 ********************
Cust/Project - ************ DAVID K. WONG
Date         - ************ JULY 10, 1985
Rev/I. D.    - ************ TK151-1 REV. 0
                        _______________________
82S151    DIR      !A:A:A:A:A:A:A:A:A:A:A:A!
___                _______________________
 T !      POL      !H:L:L:H:L:H:L:H:H:H:L:L!
 E !-----------------------------------------
 R !      I      !            B(i)          !
 M !-------------!1 1 -----------------------
___!5_4_3_2_1_0!1_0_9_8_7_6_5_4_3_2_1_0!
  0!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  1!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  2!- -,- - H L!- - - -,- - - -,- - - -!
  3!- -,- - L H!- - - -,- - - -,- - - -!
  4!- -,- - - -!- - - -,- - - -,L L - -!
  5!- -,- - - -!- - - -,- - - -,L L - -!
  6!- -,- - - -!- - H L,- - - -,- - - -!
  7!- -,- - - -!- - H L,- - - -,- - - -!
  8!- -,- - H H!- - - -,- - - -,- - - -!
  9!- -,H H - -!- - - -,- - - -,- - - -!
 10!- -,- - L L!- - - -,- - - -,- - - -!
 11!- -,- - L L!- - - -,- - - -,- - - -!
 D2!- -,- - - -!- - - -,- - - -,- - - -!
 D1!- -,- - - -!- - - -,- - - -,- - - -!
 DO!- -,- - - -!- - - -,- - - -,- - - -!

     N N E D B A A A D A A A A A A A N N
     / /         _ _ _ _ B B _ _ _ - / /
     C C         N O N A _ _ X E N _ C C
                 O R A N O N O Q _ N
                 R _ N D R O R U B _
                 _ B D _ _ R _ _ - B
                 B   _ B D _ B B
                     E   E D
                           E
```

TB00680S



a. Basic Latches Configuration

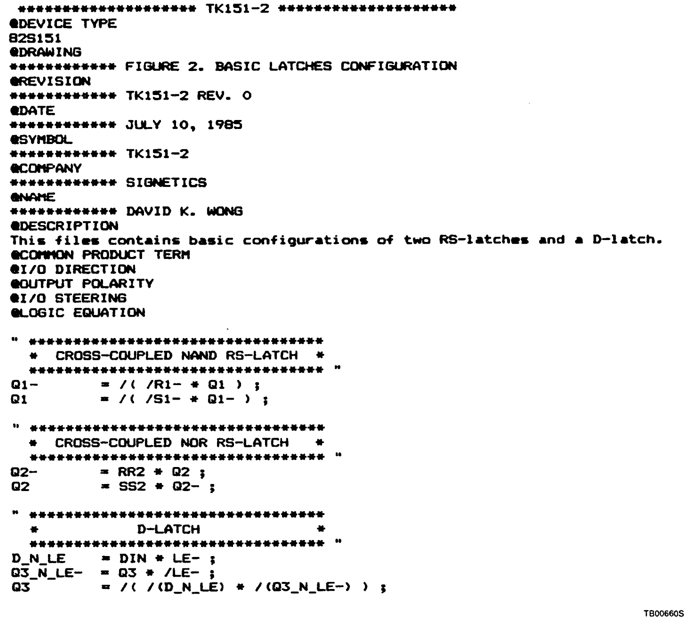
```
 ********************** TK151-2 *********************
######################## P I N   L I S T ########################

   LABEL      ** FNC **PIN ---------- PIN** FNC **     LABEL
R1-           ** I   **   1-!        !-20 ** +5V **VCC
S1-           ** I   **   2-!        !-19 ** /O  **Q1
RR2           ** I   **   3-!        !-18 ** /O  **Q1-
SS2           ** I   **   4-!   8    !-17 ** O   **Q2
DIN           ** I   **   5-!   2    !-16 ** O   **Q2-
LE-           ** I   **   6-!   S    !-15 ** /O  **Q3
N/C           ** /B  **   7-!   1    !-14 ** O   **D_N_LE
N/C           ** /B  **   8-!   5    !-13 ** O   **Q3_N_LE-
N/C           ** /B  **   9-!   1    !-12 ** /B  **N/C
GND           ** OV  **  10-!        !-11 ** /B  **N/C
                            ----------
```

TB00670S

b. Pin List

Figure 2



```
******************** TK151-2 ********************
@DEVICE TYPE
82S151
@DRAWING
************ FIGURE 2. BASIC LATCHES CONFIGURATION
@REVISION
************ TK151-2 REV. 0
@DATE
************ JULY 10, 1985
@SYMBOL
************ TK151-2
@COMPANY
************ SIGNETICS
@NAME
************ DAVID K. WONG
@DESCRIPTION
This files contains basic configurations of two RS-latches and a D-latch.
@COMMON PRODUCT TERM
@I/O DIRECTION
@OUTPUT POLARITY
@I/O STEERING
@LOGIC EQUATION

" ********************************
  *  CROSS-COUPLED NAND RS-LATCH  *
  ******************************** "
Q1-         = /( /R1- * Q1 ) ;
Q1          = /( /S1- * Q1- ) ;

" ********************************
  *  CROSS-COUPLED NOR RS-LATCH   *
  ******************************** "
Q2-         = RR2 * Q2 ;
Q2          = SS2 * Q2- ;

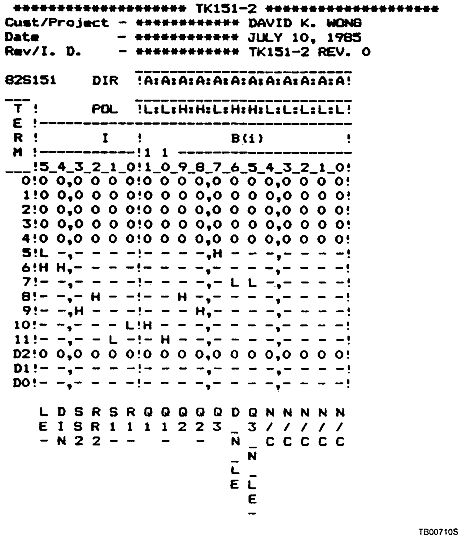
" ********************************
  *           D-LATCH             *
  ******************************** "
D_N_LE      = DIN * LE- ;
Q3_N_LE-    = Q3 * /LE- ;
Q3          = /( /(D_N_LE) * /(Q3_N_LE-) ) ;
```

TB00660S

c. Boolean Equations of Basic Latches Configuration

Figure 2 (Continued)

Table 2. Program Table of Basic Latches

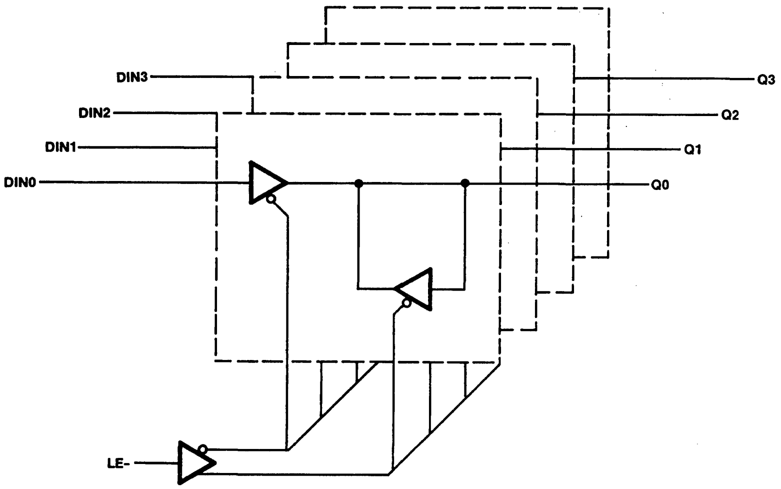


```
******************** TK151-2 ********************
Cust/Project - ************ DAVID K. WONG
Date         - ************ JULY 10, 1985
Rev/I. D.    - ************ TK151-2 REV. 0

                  -----------------------
82S151    DIR    !A:A:A:A:A:A:A:A:A:A:A:A!
___               -----------------------
 T !      POL    !L:L:H:H:L:H:H:L:L:L:L:L!
 E !-------------------------------------
 R !      I     !          B(i)         !
 M !-----------!1 1 --------------------
___!5_4_3_2_1_0!1_0_9_8_7_6_5_4_3_2_1_0!
  0!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  1!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  2!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  3!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  4!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  5!L -,- - - -!- - - -,H - - -,- - - -!
  6!H H,- - - -!- - - -,- - - -,- - - -!
  7!- -,- - - -!- - - -,- L L -,- - - -!
  8!- -,- H - -!- - H -,- - - -,- - - -!
  9!- -,H - - -!- - - H,- - - -,- - - -!
 10!- -,- - - L!H - - -,- - - -,- - - -!
 11!- -,- - L -!- H - -,- - - -,- - - -!
 D2!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
 D1!- -,- - - -!- - - -,- - - -,- - - -!
 D0!- -,- - - -!- - - -,- - - -,- - - -!

    L D S R S R Q Q Q Q Q D Q N N N N N
    E I S R 1 1 1 1 2 2 3 _ 3 / / / / /
    - N 2 2 - -   -   -   N _ C C C C C
                          _ N
                          L _
                          E L
                            E
                            -
```

TB00710S



LD01300S

a. 4-Bit D-Latch

```
 ********************** TK151-3 **********************
************************ P I N   L I S T ************************

   LABEL     ** FNC **PIN ---------- PIN** FNC **    LABEL
DIN0         ** I   **   1-!          !-20 ** +5V **VCC
DIN1         ** I   **   2-!          !-19 ** B   **Q0
DIN2         ** I   **   3-!          !-18 ** B   **Q1
DIN3         ** I   **   4-!    8     !-17 ** B   **Q2
LE-          ** I   **   5-!    2     !-16 ** B   **Q3
N/C          ** I   **   6-!    S     !-15 ** B   **FB0
N/C          ** /B  **   7-!    1     !-14 ** B   **FB1
N/C          ** /B  **   8-!    5     !-13 ** B   **FB2
N/C          ** /B  **   9-!    1     !-12 ** B   **FB3
GND          ** 0V  **  10-!          !-11 ** /B  **N/C
                            ----------
```

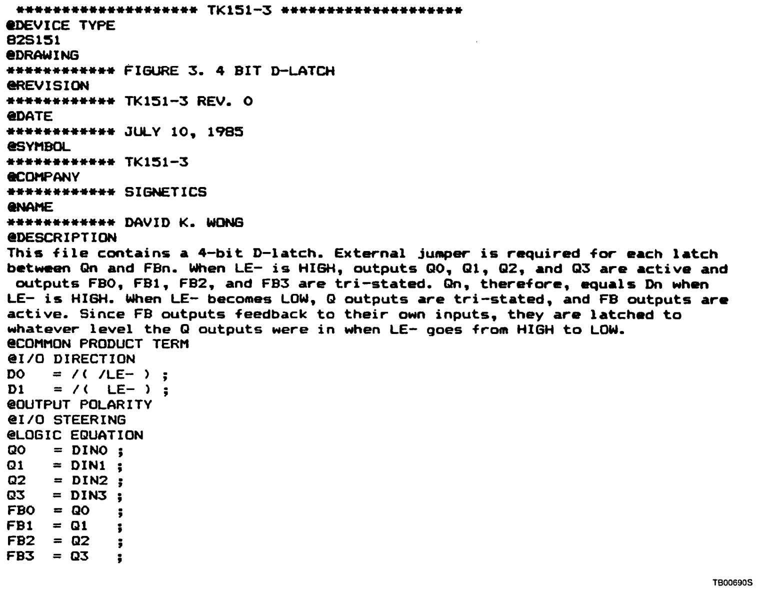
TB00700S

b. Pin List

Figure 3

PLS151 Toolkit

AN22



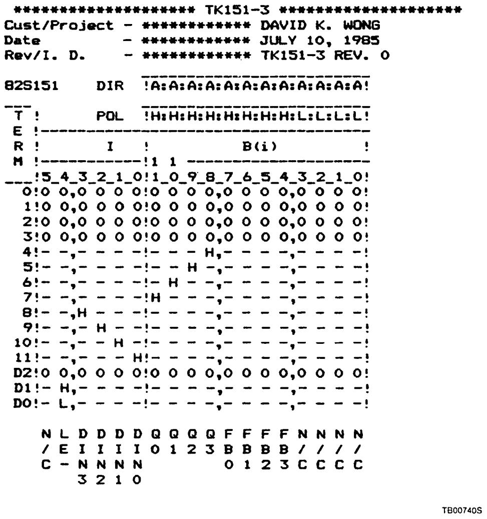
```
 ******************** TK151-3 ********************
@DEVICE TYPE
82S151
@DRAWING
************ FIGURE 3. 4 BIT D-LATCH
@REVISION
************ TK151-3 REV. 0
@DATE
************ JULY 10, 1985
@SYMBOL
************ TK151-3
@COMPANY
************ SIGNETICS
@NAME
************ DAVID K. WONG
@DESCRIPTION
This file contains a 4-bit D-latch. External jumper is required for each latch
between Qn and FBn. When LE- is HIGH, outputs Q0, Q1, Q2, and Q3 are active and
 outputs FB0, FB1, FB2, and FB3 are tri-stated. Qn, therefore, equals Dn when
LE- is HIGH. When LE- becomes LOW, Q outputs are tri-stated, and FB outputs are
active. Since FB outputs feedback to their own inputs, they are latched to
whatever level the Q outputs were in when LE- goes from HIGH to LOW.
@COMMON PRODUCT TERM
@I/O DIRECTION
D0    = /( /LE- ) ;
D1    = /(  LE- ) ;
@OUTPUT POLARITY
@I/O STEERING
@LOGIC EQUATION
Q0    = DIN0 ;
Q1    = DIN1 ;
Q2    = DIN2 ;
Q3    = DIN3 ;
FB0   = Q0   ;
FB1   = Q1   ;
FB2   = Q2   ;
FB3   = Q3   ;
```

TB00690S

c. Boolean Equations of 4-Bit D-Latch

Figure 3 (Continued)

Table 3. Program Table of 4-Bit D-Latch

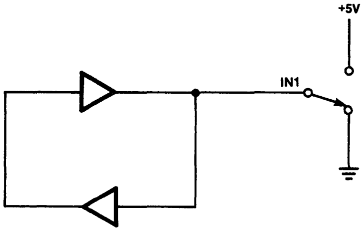


```
 ******************** TK151-3 ********************
Cust/Project - ************ DAVID K. WONG
Date         - ************ JULY 10, 1985
Rev/I. D.    - ************ TK151-3 REV. 0

               _________________________
82S151   DIR   !A:A:A:A:A:A:A:A:A:A:A:A!
---            _________________________
 T !      POL  !H:H:H:H:H:H:H:H:L:L:L:L!
 E !------------------------------------
 R !         I     !          B(i)         !
 M !-----------!1 1 --------------------
___!5_4_3_2_1_0!1_0_9_8_7_6_5_4_3_2_1_0!
  0!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  1!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  2!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  3!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  4!- -,- - - -!- - - H,- - - -,- - - -!
  5!- -,- - - -!- - H -,- - - -,- - - -!
  6!- -,- - - -!- H - -,- - - -,- - - -!
  7!- -,- - - -!H - - -,- - - -,- - - -!
  8!- -,H - - -!- - - -,- - - -,- - - -!
  9!- -,- H - -!- - - -,- - - -,- - - -!
 10!- -,- - H -!- - - -,- - - -,- - - -!
 11!- -,- - - H!- - - -,- - - -,- - - -!
 D2!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
 D1!- H,- - - -!- - - -,- - - -,- - - -!
 DO!- L,- - - -!- - - -,- - - -,- - - -!

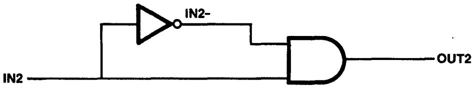
    N L D D D D Q Q Q Q F F F F N N N N
    / E I I I I 0 1 2 3 B B B B / / / /
    C - N N N N         0 1 2 3 C C C C
        3 2 1 0
```

TB00740S



TC01800S

Switch Debouncer



LD01310S

Pulse Shaper

a. Single Pin Switch Debouncer and Pulse Shaper

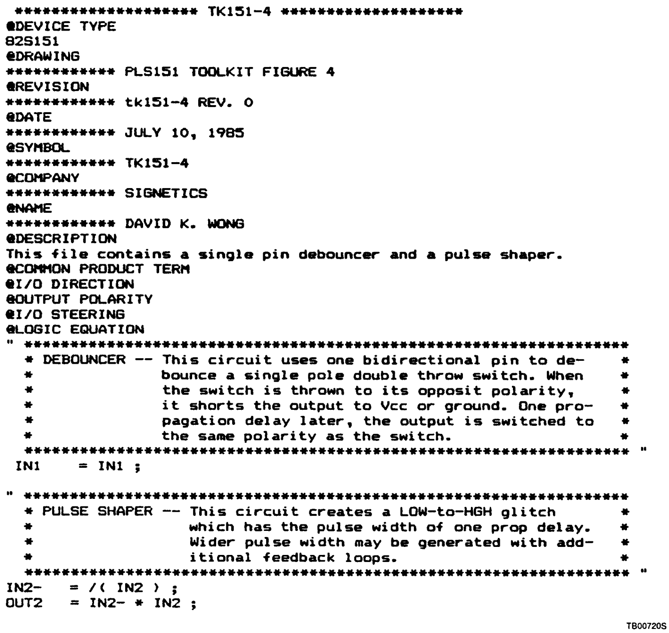
```
 ******************** TK151-4 ********************
********************** P I N   L I S T **********************

   LABEL      ** FNC **PIN ---------- PIN** FNC **    LABEL
 IN2          ** I    **   1-|         |-20 ** +5V **VCC
 N/C          ** I    **   2-|         |-19 ** O   **IN1
 N/C          ** I    **   3-|         |-18 ** /O  **IN2-
 N/C          ** I    **   4-|    8    |-17 ** O   **OUT2
 N/C          ** I    **   5-|    2    |-16 ** /B  **N/C
 N/C          ** I    **   6-|    S    |-15 ** /B  **N/C
 N/C          ** /B   **   7-|    1    |-14 ** /B  **N/C
 N/C          ** /B   **   8-|    5    |-13 ** /B  **N/C
 N/C          ** /B   **   9-|    1    |-12 ** /B  **N/C
 GND          ** OV   **  10-|         |-11 ** /B  **N/C
                             ----------
```

TB00730S

b. Pin List

Figure 4



```
******************** TK151-4 ********************
@DEVICE TYPE
82S151
@DRAWING
************ PLS151 TOOLKIT FIGURE 4
@REVISION
************ tk151-4 REV. 0
@DATE
************ JULY 10, 1985
@SYMBOL
************ TK151-4
@COMPANY
************ SIGNETICS
@NAME
************ DAVID K. WONG
@DESCRIPTION
This file contains a single pin debouncer and a pulse shaper.
@COMMON PRODUCT TERM
@I/O DIRECTION
@OUTPUT POLARITY
@I/O STEERING
@LOGIC EQUATION
" ***************************************************************
  * DEBOUNCER -- This circuit uses one bidirectional pin to de-    *
  *              bounce a single pole double throw switch. When    *
  *              the switch is thrown to its opposit polarity,     *
  *              it shorts the output to Vcc or ground. One pro-   *
  *              pagation delay later, the output is switched to   *
  *              the same polarity as the switch.                  *
  *************************************************************** "
 IN1    = IN1 ;

" ***************************************************************
  * PULSE SHAPER -- This circuit creates a LOW-to-HGH glitch      *
  *                 which has the pulse width of one prop delay.  *
  *                 Wider pulse width may be generated with add-  *
  *                 itional feedback loops.                       *
  *************************************************************** "
IN2-    = /( IN2 ) ;
OUT2    = IN2- * IN2 ;
```

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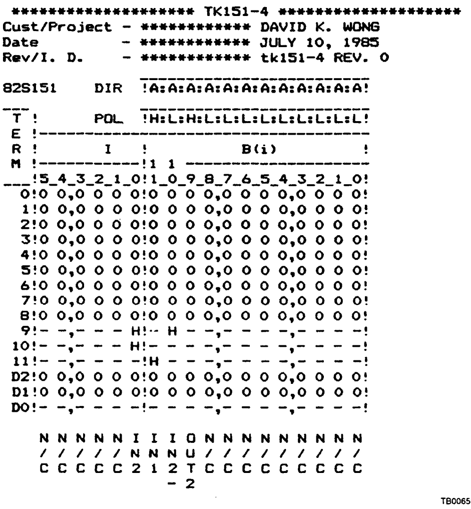
c. Boolean Equations of Single Pin and Pulse Shaper

Figure 4 (Continued)

Table 4. Program Table of Single Pin Debouncer and Shaper



```
 ******************** TK151-4 ********************
Cust/Project - ************ DAVID K. WONG
Date         - ************ JULY 10, 1985
Rev/I. D.    - ************ tk151-4 REV. 0

               _________________________
82S151    DIR  !A:A:A:A:A:A:A:A:A:A:A:A!
___            _________________________
 T !      POL  !H:L:H:L:L:L:L:L:L:L:L:L!
 E !------------------------------------
 R !      I    !         B(i)          !
 M !-----------!1 1 --------------------
___!5_4_3_2_1_0!1_0_9_8_7_6_5_4_3_2_1_0!
  0!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  1!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  2!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  3!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  4!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  5!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  6!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  7!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  8!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
  9!- -,- - - H!- H - -,- - - -,- - - -!
 10!- -,- - - H!- - - -,- - - -,- - - -!
 11!- -,- - - -!H - - -,- - - -,- - - -!
 D2!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
 D1!0 0,0 0 0 0!0 0 0 0,0 0 0 0,0 0 0 0!
 DO!- -,- - - -!- - - -,- - - -,- - - -!

    N N N N N I I I O N N N N N N N N N
    / / / / / N N N U / / / / / / / / /
    C C C C C 2 1 2 T C C C C C C C C C
                  - 2
```

TB00650S

Signetics

AN23
PLS168/168A Primer

Application Note

Application Specific Products

INTRODUCTION

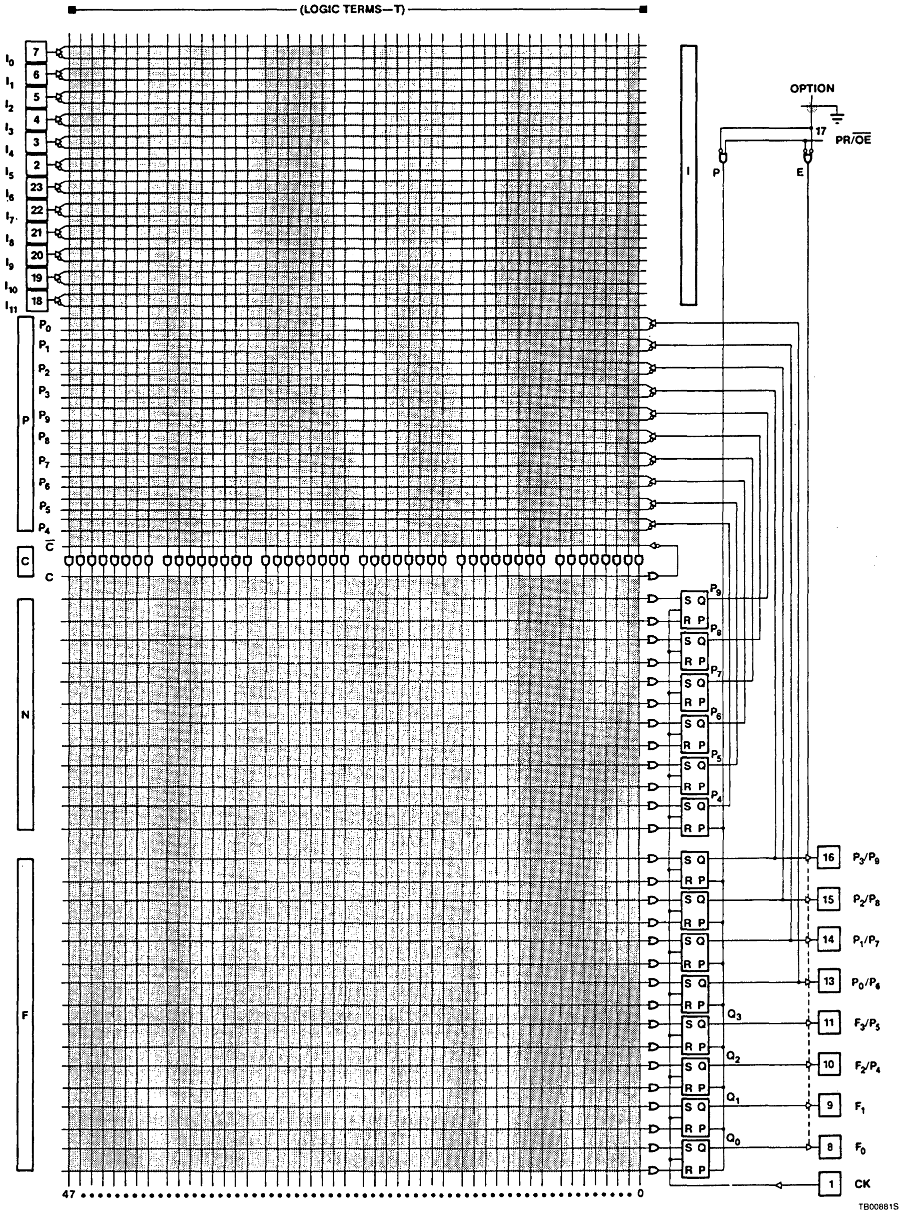
THE PLS168/168A is a bipolar Field-Programmable Logic Sequencer as shown in Figure 1, which consists of 12 inputs, a 48 product term PLA and 14 R/S flip-flops. Out of the 14 flip-flops, six are buried State Registers ($P_4 - P_9$), four Output Registers ($F_0 - F_3$), and four Dual-purpose Registers ($P_0 - P_3$), which may be used as Output or State Registers. All flip-flops are positive edge-triggered. They are preset to "1" at power-up, or may be asynchronously set to "1" by an optional PR/OE pin, which may be programmed either as a preset pin or as an Output Enable pin. Additional features includes the Complement Array and diagnostics features.

ARCHITECTURE

As shown in Figure 2, the device is organized as a decoding AND-OR network which drives a set of registers some of which, in turn, feedbacks to the AND/OR decoder while the rest serve as outputs. Outputs P_0 to P_3 may be programmed to feedback to the AND/OR decoder as State Registers and, at the same time, used as outputs. The user now can design a 10-bit state machine without external wiring. The AND/OR array is the classical PLA structure in which the outputs of all the AND gates can be programmed to drive all the OR gates. The schematic diagram of the AND-OR array is shown in Figure 3. This structure provides the user a very structured design methodology which can be automated by CAD tools, such as Signetics AMAZE software package. The output of the PLA is in the form of sum-of-products which, together with the RS flip-flops, is the ideal structure for implementation of state machines. (Refer to Appendix A for a brief description of synchronous finite state machines.)

Design Tools

A direct approach to implement a design using the PLS168/168A is the H/L table supplied in the data sheet as shown in Table 1. The table is organized according to input and output of the PLA decoding network. The lefthand side of the table represent the inputs to the AND-array, which includes input from input pins and present state information from the feedback buffers which feedback the contents of the State Register. The righthand side of the table represents the output of the OR-array, which drives the State and Output Registers as the next state and output. Each column in the lefthand side of the table represents an input buffer, which may be inverting, non-inverting, disconnected or unprogrammed. Each column in the righthand side of the table represents a pair of outputs to the flip-flops, which may be set, reset, disconnected, or unprogrammed. The programming symbols are H, L, –, and 0. (See Figure 4 for details.) For inputs buffers, "H" means that the non-inverting buffer is connected, "L" means that the inverting buffer is connected, "–" means that both inverting and non-inverting buffers are disconnected, and "0" means that both inverting and non-inverting buffers are connected which causes that particular AND-term to be unconditionally Low. On the output side of the table, "H" means that the particular AND-term is connected to the OR-term on the "S" input of the particular flip-flop, "L" means that the AND-term is connected to the "R" side, "–" means that the AND-term is not connected to the flip-flop at all, and "0" means that the AND-term is connected to both the "S" and "R" sides. More details of the symbols and their meanings are shown in Appendix B. Each row in the table represents an AND-term. There are 48 AND-terms in the device. Therefore, there are 48 rows in the table. An example of implementing a transition from one state to another is shown in Figure 4a. The state diagram can be implemented by the PLS168 as shown in Figure 4b. The state diagram is translated into H/L format as shown in Figure 4c. The first column on the lefthand side of the table is for the Complement Array which will be discussed in detail in the next section.



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ▨ Programmable connection.

Figure 1. Logic Diagram of PLS168/168A

PLS168/168A Primer

AN23

Table 1. PLS168/168A Programming Table

CUSTOMER NAME ______________________

PURCHASE ORDER # ______________________

SIGNETICS DEVICE # CF (XXXX)

CUSTOMER SYMBOLIZED PART # ______________________

TOTAL NUMBER OF PARTS ______________________

PROGRAM TABLE # ______________________

REV ______________________

DATE ______________________

AND

INACTIVE	O	C_n
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

INACTIVE	O	$I_m \cdot P_s$
I, P	H	
I, $\bar{P}$	L	
DON'T CARE	—	

OR

INACTIVE	O	$N_s \cdot F_r$
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
OE	L	

		AND																							OPTION (P/E)													
																									OR													
TERM	C_n	INPUT(Im)												PRESENT STATE (Ps) (Px)										REMARKS	NEXT STATE (Ns) (Px)										OUTPUT (Fr)			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	3	2	1	0
0																																						
1																																						
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42																																						
43																																						
44																																						
45																																						
46																																						
47																																						
PIN NO.		18	19	20	21	22	23	2	3	4	5	6	7																		16	15	14	13	11	10	9	8
VARIABLE NAME																																						

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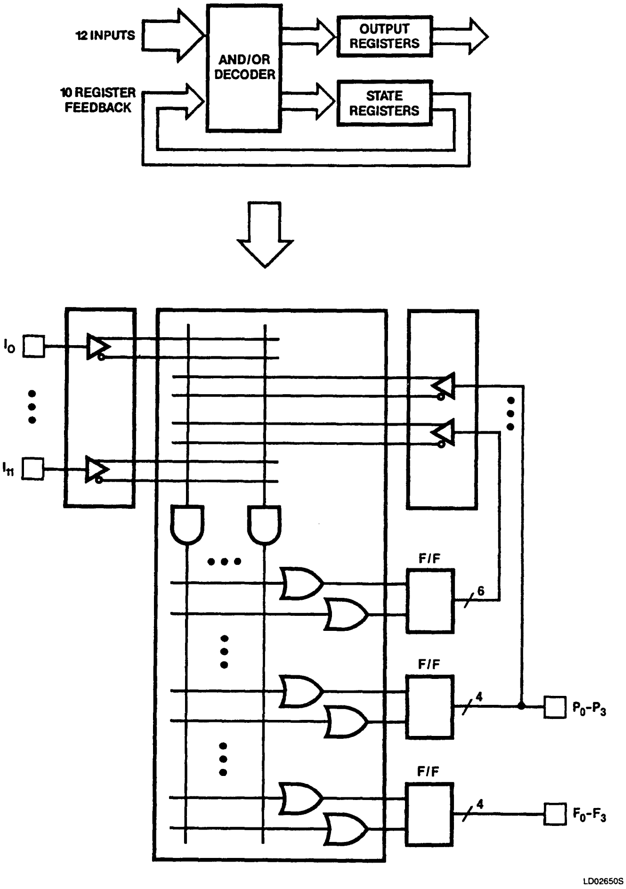


Figure 2. The Architecture of PLS168/168A

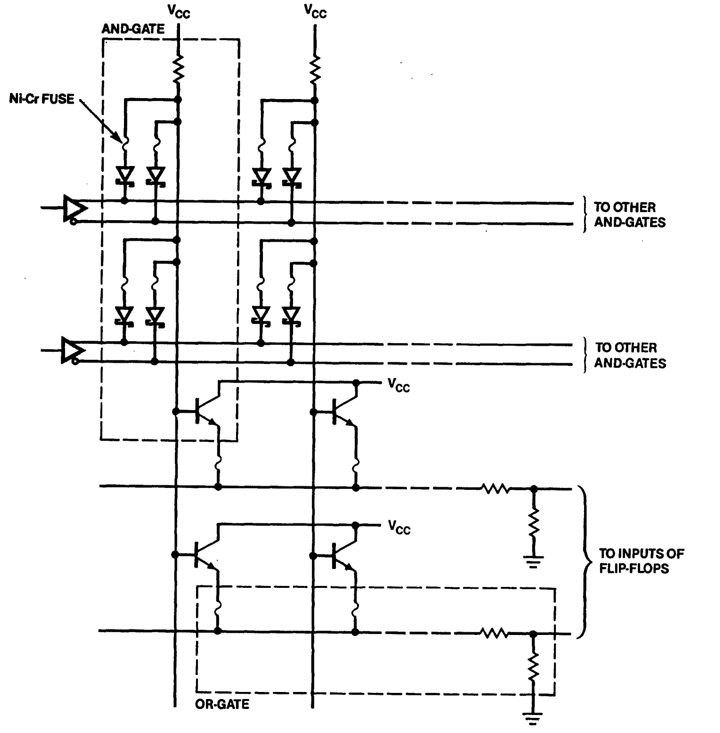
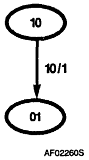
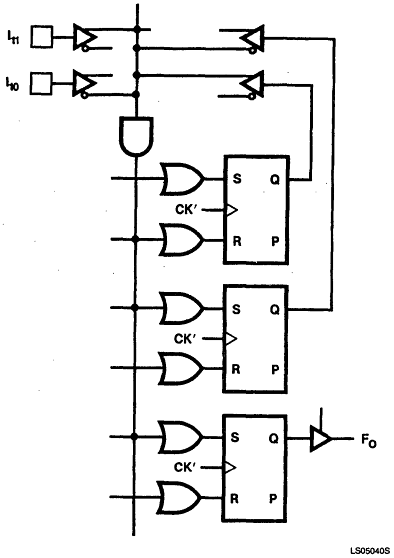


Figure 3. Schematic Diagram of AND-OR Array



a. State Diagram



b. Implementation of State Diagram (a) With PLS168

TERM	AND																							OPTION (PR/OE)													
																								OR													
	C	INPUT												PRESENT STATE										NEXT STATE										OUTPUT			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	3	2	1	0
00	–	H	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–	H	L	–	–	–	–	–	–	–	–	L	H	–	–	–	–	H	–	–	–
01																																					
PIN NO.		18	19	20	21	22	23	2	3	4	5	6	7																	16	15	14	13	11	10	9	8
NAME		IN1	INØ																															OUTØ			

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c. PLS168 Programming Table

Figure 4. Implementing State Machine with PLS168

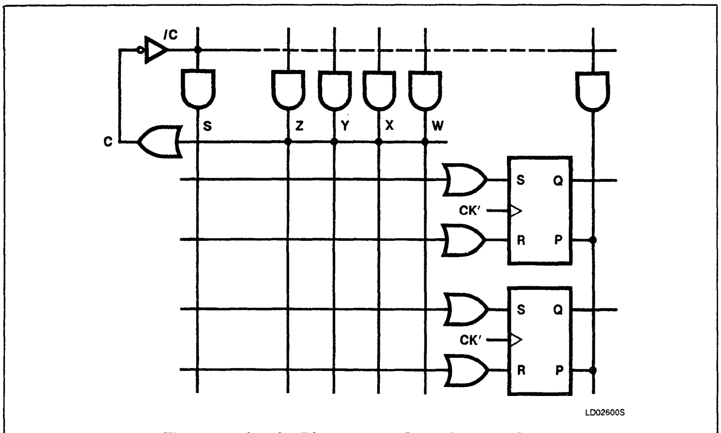
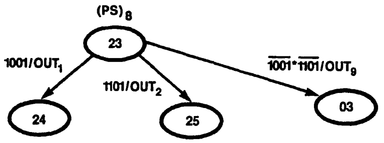


Figure 5. Logic Diagram of Complement Array

Complement Array

An additional feature is tho Complement Array, which is often usod to provide escape vectors in case the stato machines get into undefined states during powor-up or a timing violation due to asynchronous inputs. A logic diagram of the Complement Array is shown in Figure 5. The output of the Complement Array is normally Low when one or more AND-terms are High. If all of the AND-terms are Low, then the output of the Complement Array will be High. In this example, if each AND-term is a decoder for a particular state and input combination, and if the circuit gets into an undefined state, none of the AND-terms will be High. Therefore, the output /C will be High, which will then enable the AND-term S which in turn may be used to reset all registers to Low or High as predefined. The state machine thus escapes from being in an undefined state by using the Complement Array and one AND-term. Without the Complement Array an alternate way of escaping from being in an undefined state is by defining all possible states which are not being defined. This method may require quite a few AND-terms depending on the design. Another application for the Complement Array is illustrated by the following example. As shown in Figure 6, when the machine is in state 23, if input vector equals 1001, it will go to next state 24. If the input is 1101, then go to state 25. But if the input is neither 1001 nor 1101, then go to state 03. It takes only two terms to implement the first two transition vectors. To implement the third vector "go to state 03 if input is neither 1001 nor 1101", the Complement Array accepts the outputs of the first two AND-terms as inputs. If the input vector is neither 1001 nor 1101, then both terms will be Low, which causes the output of the Complement Array (/C) to be High. A third AND-term is used to AND state 24 and /C together to set the registers to state 03. The State Diagram is translated into AMAZE syntex as shown in Figure 6b, where all vectors are in square brackets and the Complement Array is represented by the ELSE statement. The State diagram Figure 6a can also be expressed in the format of a program table as shown in Figure 6c. The complement array may be used to exit from different present states to different next states. It can be used many times in one state machine design as shown in Figures 7a, b, and c where the state diagram is implemented using the AMAZE state equation syntex and the H/L format.



NOTE: $\overline{1001}\cdot\overline{1101} = \overline{1001+1101}$

AF02241S

a. State Diagram

```
WHILE [23]
  IF [1001] THEN [24] WITH
[OUT1]
  IF [1101] THEN [25] WITH
[OUT2]
  ELSE: [03] WITH [OUT9]
```

b. AMAZE State Equation Syntex

TERM	AND																							OPTION (PR/OE) OR													
	C	INPUT												PRESENT STATE										NEXT STATE										OUTPUT			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	3	2	1	0
00	A	H	L	L	H	–	–	–	–	–	–	–	–	H	L	L	L	H	H	–	–	–		H	L	L	H	L	L	–	–	–		L	L	L	H
01	A	H	H	L	H	–	–	–	–	–	–	–	–	H	L	L	L	H	H	–	–	–		H	L	L	H	L	H	–	–	–		L	L	H	L
02	•	–	–	–	–	–	–	–	–	–	–	–	–	H	L	L	L	H	H	–	–	–		L	L	L	L	H	H	–	–	–		H	L	L	H
03																																					
04																																					
05																																					
PIN NO.		18	19	20	21	22	23	2	3	4	5	6	7																	16	15	14	13	11	10	9	8
NAME		IN3	IN2	IN1	INØ																													OP3	OP2	OP1	OPØ

COMPLEMENT ARRAY

PRESENT STATE=23(HEX)

NEXT STATE: 24(HEX)
25(HEX)
03(HEX)

OUT1=0001
OUT2=0010
OUTG=1001

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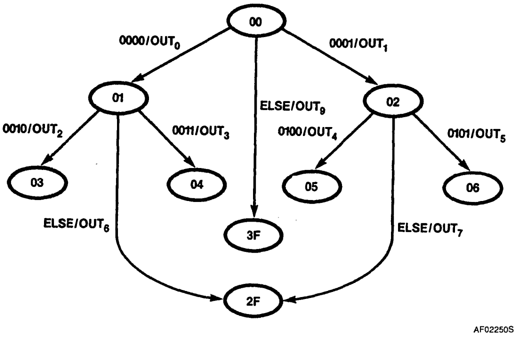
c. H/L Format

Figure 6. Application of Complement Array



a. State Diagram

```
WHILE [00]
  IF [0000] THEN [01] WITH [OUT0]
  IF [0001] THEN [02] WITH [OUT1]
  ELSE: [3F] WITH [OUT9]
WHILE [01]
  IF [0010] THEN [03] WITH [OUT2]
  IF [0011] THEN [04] WITH [OUT3]
  ELSE: [2F] WITH [OUT6]
WHILE [02]
  IF [0100] THEN [05] WITH [OUT4]
  IF [0101] THEN [06] WITH [OUT5]
  ELSE: [2F] WITH [OUT7]
```

b. AMAZE State Equation

T E R M	AND																						OPTION (PR/OE)													
																							OR													
	C	INPUT												PRESENT STATE										NEXT STATE										OUTPUT			
		11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	3	2	1	0
00	A	L	L	L	L	–	–	–	–	–	–	–	–	L	L	L	L	L	L	–	–	–	–	L	L	L	L	L	H	–	–	–	–	L	L	L	L
01	A	L	L	L	H	–	–	–	–	–	–	–	–	L	L	L	L	L	L	–	–	–	–	L	L	L	L	H	L	–	–	–	–	L	L	L	H
02	•	–	–	–	–	–	–	–	–	–	–	–	–	L	L	L	L	L	L	–	–	–	–	H	H	H	H	H	H	–	–	–	–	H	L	L	H
03																																					
04	A	L	L	H	L	–	–	–	–	–	–	–	–	L	L	L	L	L	H	–	–	–	–	L	L	L	L	H	H	–	–	–	–	L	L	H	L
05	A	L	L	H	H	–	–	–	–	–	–	–	–	L	L	L	L	L	H	–	–	–	–	L	L	L	H	L	L	–	–	–	–	L	L	H	H
06	•	–	–	–	–	–	–	–	–	–	–	–	–	L	L	L	L	L	H	–	–	–	–	H	L	H	H	H	H	–	–	–	–	L	H	H	L
07																																					
08	A	L	H	L	L	–	–	–	–	–	–	–	–	L	L	L	L	H	L	–	–	–	–	L	L	L	H	L	H	–	–	–	–	L	H	L	L
09	A	L	H	L	H	–	–	–	–	–	–	–	–	L	L	L	L	H	L	–	–	–	–	L	L	L	H	H	L	–	–	–	–	L	H	L	H
10	•	–	–	–	–	–	–	–	–	–	–	–	–	L	L	L	L	H	L	–	–	–	–	H	L	H	H	H	H	–	–	–	–	L	H	H	H
11																																					
PIN NO.		18	19	20	21	22	23	2	3	4	5	6	7																	16	15	14	13	11	10	9	8
NAME		IN3	IN2	IN1	INØ																													OP3	OP2	OP1	OPØ

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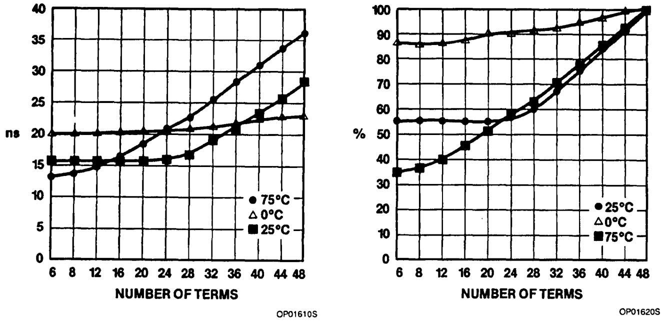
c. PLS168 Programming Table

Figure 7. Applications of Complement Array



a. PLS168 Setup Time vs P-Term Loading

b. PLS168 Setup Time vs P-Term Loading

Figure 8

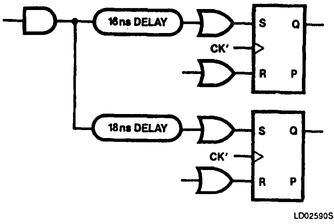


Figure 9. Difference in Propagation Delay Due to Different P-Term Loading

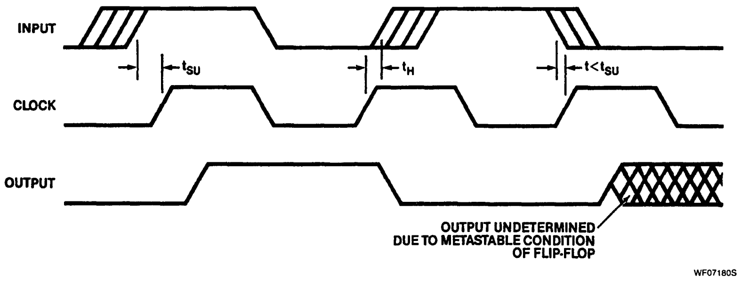

INPUT
t_{SU}
t_H
$t<t_{SU}$
CLOCK
OUTPUT
OUTPUT UNDETERMINED DUE TO METASTABLE CONDITION OF FLIP-FLOP
WF07180S

Figure 10. Change of t_{CKO} Due to Metastable Condition of Flip-Flop

Optional Preset/Output Enable

The PR/OE pin provides the user with the option of either using that pin to control the Tri-state output buffers of the Output Registers, or have that pin to asynchronously preset all registers to High. The purpose of the preset function is to provide the system a way to set the PLS168 to a known state, all Highs. The output enable function are sometimes used where the state machine is connected to a bus which is shared by other output circuits. It is also used during power-up sequence to keep the PLS168 from sending power glitches to other circuits which it drives. By programming the PR/OE pin to control the Tri-state output buffers, the preset function is permanently disabled. By programming the PR/OE pin to control the asynchronous preset of the registers, the output buffers are permanently enabled. While using the preset function to asynchronously preset the register, if a rising edge of the clock occurs while the preset input is High, the registers will remain preset. Normal flip-flop operation will resume only after the preset input is Low and the rising edge of the next clock. Setting the registers to a predefined pattern other than all Highs may be accomplished by using a dedicated p-term, which is activated by an input pin which will also inhibit all other p-terms which are being used. The inhibiting of other p-terms eliminates the problem of undetermined state of an RS flip-flop caused by having Highs on both R and S inputs.

Diagnostic Features

In debugging a state machine, sometimes it is necessary to know what is the content of the state register. The buried State Register may be read by applying +10V on I_0, which will cause the contents of register bits P_4 to P_5, P_6 to P_9 to be displayed on output pins F_2 to F_3 and P_0 and P_3 respectively. While the device can handle the +10V on pin I_0, prolonged and continuous use will cause the chip to heat up since more power is being dissipated at +10V. To facilitate more expedient functional tests, synchronous preset vectors as described above may be used to set the State Register to different states without having to go through the entire sequence.

Timing Requirements

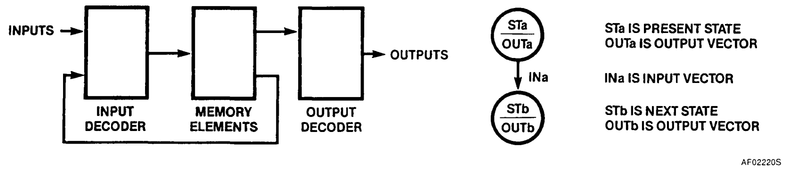
Since the PLS168 is intended to be a synchronous finite state machine, the inputs are expected to be synchronous to the clock and set-up and hold time requirements are expected to be met. In general, the set-up time requirement is measured at its worst case as having the entire AND-array connected to the OR-term being measured and there is only one active AND-term to drive the entire line. The set-up time decreases from there as less p-terms are used. This is due to the capacitance of the unused AND-terms being removed from the line. Figure 8a shows the typical set-up time requirement of a PLS168A device. Figure 8b shows the normalized set-up time as a percentage of the worst case, which is with 48 terms connected. In a typical state machine design, some flip-flops will change states more frequently than others. Those that change more frequently will have more p-term loading on its OR gates than those that change states less frequently. The different loadings on the OR-terms cause different delay on the inputs of the flip-flops as shown in Figure 9. If an input fails to meet the set-up time specification, it is possible that the resultant of the input change gets to one set of flip-flops before the rising edge of the clock while it gets to other flip-flops during or after the clock's rising edge. The result is that some flip-flops have changed states and some have not, or some get into metastable condition as shown in Figure 10. The state machine is now either out of sequence or is in an undefined state. This problem often occurs with asynchronous inputs which is generated totally independent of the clock on the system. A common remedy for the problem of asynchronous inputs is to use latches or flip-flops to catch the input and then synchronously feed it to the state machine. This minimizes the problem with the different propagation delays due to different p-term loading. But there is still a finite probability that the external latches or flip-flops will get into metastable condition, which may be propagated into the state machine. Nevertheless, the window for the flip-flops in state machine to get into undefined states or metastable condition is narrowed by a great extent.

APPENDIX A

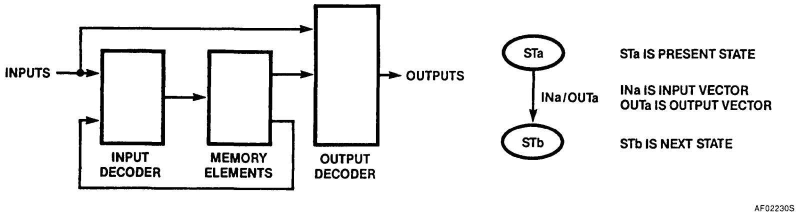
INTRODUCTION TO STATE MACHINE

A state machine is a synchronous sequential circuit which interprets inputs and generates outputs in accordance with a predetermined logic sequence. It is analogous to running a computer program with a computer. The state machine, with its sequence coded in hardware, can run much faster than a computer running the sequence in software. Therefore, it is often used in controller applications where speed is important.

Generally, state machines may be classified as Mealy or Moore machines as shown in Figures 1a and 1b. The fundamental difference of the two types are: the output of a Moore machine is a dependent of only the state of the memory elements whereas the output of a Mealy machine is a dependent of both the state of the memory elements and the inputs to the state machine. The figures also show graphic representations of the logic sequence in the form of state diagram in which the bubbles represent state vectors, and the arrows represent transitions from present states to next states.



Appendix A-1. Moore Machine Model



Appendix A-2. Mealy Machine Model

APPENDIX B

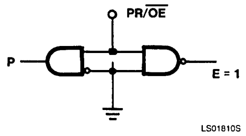
LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

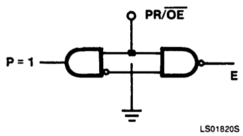
With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

In this table, the logic state or action of control variables C, I, P, N, and F, associated with each Transition Term T_n, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

PRESET/$\overline{\text{OE}}$ OPTION – (P/E)



OPTION	CODE
PRESET	H

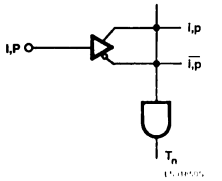


OPTION	CODE
$\overline{\text{OE}}$	L

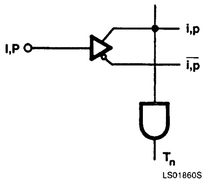
PROGRAMMING:

The PLS168A has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic high (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all highs (H) as the present state.

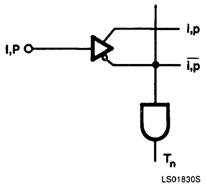
"AND" ARRAY – (I), (P)



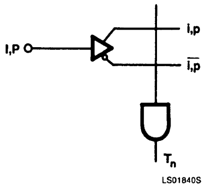
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, P	H

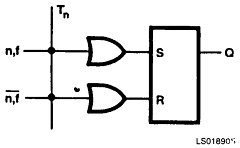


STATE	CODE
$\overline{\text{I}}$, $\overline{\text{P}}$	L

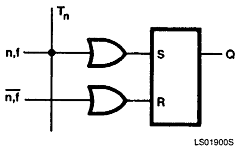


STATE	CODE
DON'T CARE	–

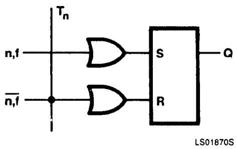
"OR" ARRAY – (N), (F)



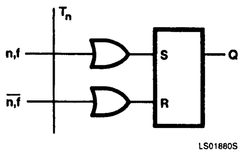
ACTION	CODE
INACTIVE[1,3]	O



ACTION	CODE
SET	H

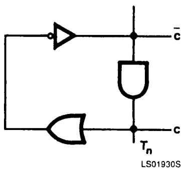


ACTION	CODE
RESET	L

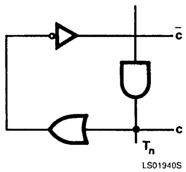


ACTION	CODE
NO CHANGE	–

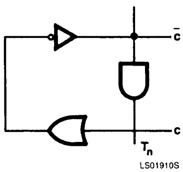
"COMPLEMENT" ARRAY – (C)



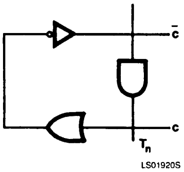
ACTION	CODE
INACTIVE[1,4]	O



ACTION	CODE
GENERATE	A



ACTION	CODE
PROPAGATE	•



ACTION	CODE
TRANSPARENT	–

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Signetics

AN24
PLS173 as a 10-Bit Comparator, 74LS460

Application Note

Application Specific Products

DESCRIPTION

The PLS173 is a 24-pin PLA device which has 10 bidirectional outputs and 12 dedicated inputs. The output of the device is the sum of products of the inputs. The polarity of each output may be individually programmed as Active-High or Active-Low. A logic diagram of the device is shown in Appendix A. A 10-bit comparator similar to the 74LS460 compares two 10-bit data inputs to establish if EQUIVALENCE or NOT EQUIVALENCE exists. The output has True and Complement comparison status outputs. The logic diagram of the comparator is shown in Figure 1.

The truth table is as shown in Table 1 where vectors a and b are 10-bit inputs to A9 to A0 and B9 to B0. If the input to A9-A0 is bit-to-bit equivalent to the input to B9-B0, the two input vectors are considered EQUIVALENT, and output EQ goes High and NE goes Low. If the two input vectors are not bit-to-bit equivalent, then EQ goes Low and NE goes High. The circuit is implemented with AMAZE as shown in Figures 2a, 2b and 2c. The result of logic simulation of the circuit is shown in Figure 2d.

Notice that on the OR side of the program table in Figure 5, all the fuses in the OR-term are intact, which means that all the AND-terms are still connected to all the OR-terms. This feature provides for future modification. But if all the unused AND-terms are deleted, the device will run faster. There are also many unused AND-terms which will provide for future modification. But if they are deleted (both on the AND and OR side), it will amount to about 450μA per term power saving. Figure 3 is the program table with all unused terms deleted.

Table 1. Function Table

$A_9 - A_0$	$B_9 - B_0$	EQ	NE
a	a	H	L
b	b	H	L
a	b	L	H
b	a	L	H

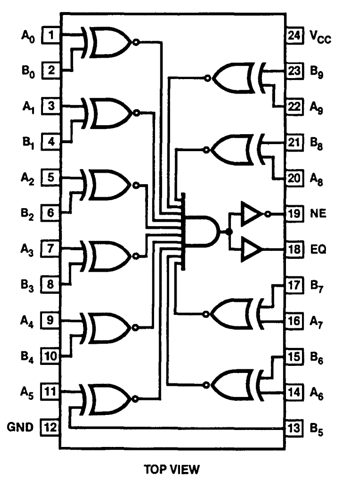
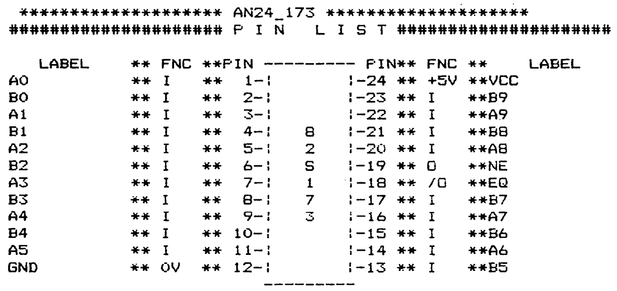


Figure 1. Logical Equivalent Circuit of 10-Bit Comparator



```
    ******************** AN24_173 ********************
   ###################### P I N   L I S T ######################

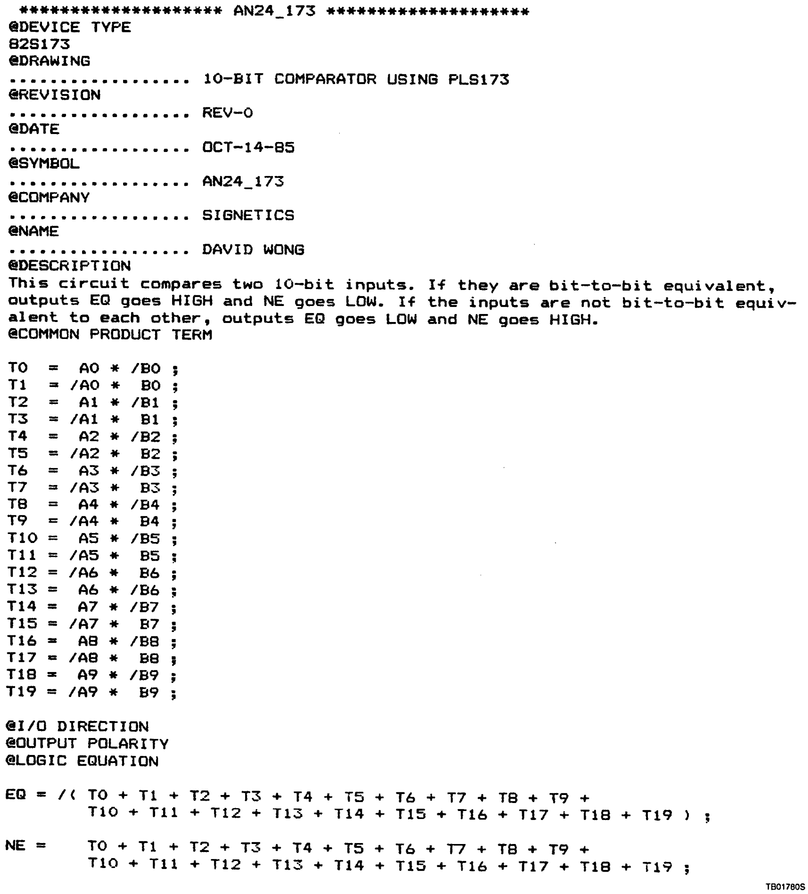
      LABEL       ** FNC **PIN ---------- PIN** FNC **     LABEL
   A0             ** I    **  1-!         !-24 ** +5V **VCC
   B0             ** I    **  2-!         !-23 ** I   **B9
   A1             ** I    **  3-!         !-22 ** I   **A9
   B1             ** I    **  4-!   8     !-21 ** I   **B8
   A2             ** I    **  5-!   2     !-20 ** I   **A8
   B2             ** I    **  6-!   S     !-19 ** O   **NE
   A3             ** I    **  7-!   1     !-18 ** /O  **EQ
   B3             ** I    **  8-!   7     !-17 ** I   **B7
   A4             ** I    **  9-!   3     !-16 ** I   **A7
   B4             ** I    ** 10-!         !-15 ** I   **B6
   A5             ** I    ** 11-!         !-14 ** I   **A6
   GND            ** OV   ** 12-!         !-13 ** I   **B5
                                ----------
```

TB01770S

a. Pin List of 10-Bit Comparator

Figure 2

PLS173 as a 10-Bit Comparator, 74LS460 AN24



```
********************* AN24_173 *********************
@DEVICE TYPE
82S173
@DRAWING
.................. 10-BIT COMPARATOR USING PLS173
@REVISION
.................. REV-0
@DATE
.................. OCT-14-85
@SYMBOL
.................. AN24_173
@COMPANY
.................. SIGNETICS
@NAME
.................. DAVID WONG
@DESCRIPTION
This circuit compares two 10-bit inputs. If they are bit-to-bit equivalent,
outputs EQ goes HIGH and NE goes LOW. If the inputs are not bit-to-bit equiv-
alent to each other, outputs EQ goes LOW and NE goes HIGH.
@COMMON PRODUCT TERM

T0  =  A0 * /B0 ;
T1  = /A0 *  B0 ;
T2  =  A1 * /B1 ;
T3  = /A1 *  B1 ;
T4  =  A2 * /B2 ;
T5  = /A2 *  B2 ;
T6  =  A3 * /B3 ;
T7  = /A3 *  B3 ;
T8  =  A4 * /B4 ;
T9  = /A4 *  B4 ;
T10 =  A5 * /B5 ;
T11 = /A5 *  B5 ;
T12 = /A6 *  B6 ;
T13 =  A6 * /B6 ;
T14 =  A7 * /B7 ;
T15 = /A7 *  B7 ;
T16 =  A8 * /B8 ;
T17 = /A8 *  B8 ;
T18 =  A9 * /B9 ;
T19 = /A9 *  B9 ;

@I/O DIRECTION
@OUTPUT POLARITY
@LOGIC EQUATION

EQ = /( T0 + T1 + T2 + T3 + T4 + T5 + T6 + T7 + T8 + T9 +
        T10 + T11 + T12 + T13 + T14 + T15 + T16 + T17 + T18 + T19 ) ;

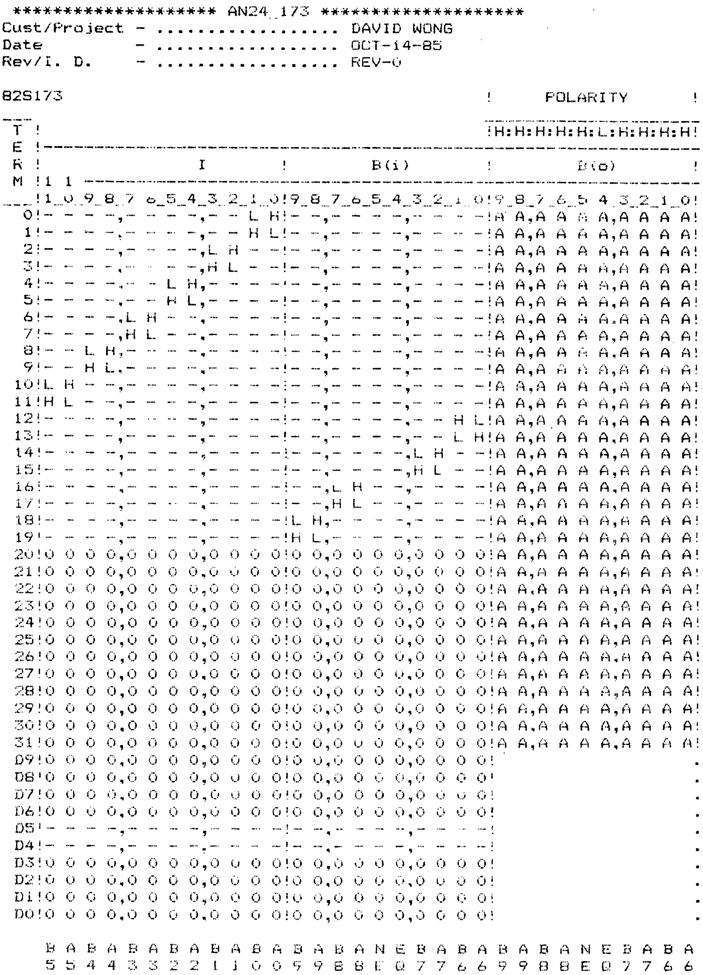
NE =    T0 + T1 + T2 + T3 + T4 + T5 + T6 + T7 + T8 + T9 +
        T10 + T11 + T12 + T13 + T14 + T15 + T16 + T17 + T18 + T19 ;
```

TB01780S

b. Boolean Equations of 10-Bit Comparator

Figure 2 (Continued)

PLS173 as a 10-Bit Comparator, 74LS460　AN24



```
******************** AN24_173 ********************
Cust/Project  - .................. DAVID WONG
Date          - .................. OCT-14-85
Rev/I. D.     - .................. REV-0

82S173                                         !    POLARITY       !
---                                            ---------------------
 T !                                           !H:H:H:H:H:L:H:H:H:H!
 E !---------------------------------------------------------------
 R !               I       !        B(i)       !        B(o)       !
 M !1 1 -----------------------------------------------------------
___!1_0_9_8_7 6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5 4_3_2_1_0!
  0!- - - -,- - - -,- - L H!- -,- - - -,- - - -!A A,A A A A,A A A A!
  1!- - - -,- - - -,- - H L!- -,- - - -,- - - -!A A,A A A A,A A A A!
  2!- - - -,- - - -,L H - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
  3!- - - -,- - - -,H L - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
  4!- - - -,- - L H,- - - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
  5!- - - -,- - H L,- - - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
  6!- - - -,L H - -,- - - -!- -,- - - -,- - - -!A A,A A A A.A A A A!
  7!- - - -,H L - -,- - - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
  8!- - L H,- - - -,- - - -!- -,- - - -,- - - -!A A,A A A A.A A A A!
  9!- - H L,- - - -,- - - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
 10!L H - -,- - - -,- - - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
 11!H L - -,- - - -,- - - -!- -,- - - -,- - - -!A A,A A A A,A A A A!
 12!- - - -,- - - -,- - - -!- -,- - - -,- - H L!A A,A A A A,A A A A!
 13!- - - -,- - - -,- - - -!- -,- - - -,- - L H!A A,A A A A.A A A A!
 14!- - - -,- - - -,- - - -!- -,- - - -,L H - -!A A,A A A A,A A A A!
 15!- - - -,- - - -,- - - -!- -,- - - -,H L - -!A A,A A A A,A A A A!
 16!- - - -,- - - -,- - - -!- -,L H - -,- - - -!A A,A A A A.A A A A!
 17!- - - -,- - - -,- - - -!- -,H L - -,- - - -!A A,A A A A,A A A A!
 18!- - - -,- - - -,- - - -!L H,- - - -,- - - -!A A,A A A A,A A A A!
 19!- - - -,- - - -,- - - -!H L,- - - -,- - - -!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A.A A A A,A A A A!
 23!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A.A A A A,A A A A!
 25!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A.A A A A!
 27!0 0 0 0,0 0 0 0.0 0 0 0!0 0,0 0 0 0.0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0.0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A.A A A A,A A A A!
 31!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A.A A A A!
 D9!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D8!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D7!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D6!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D5!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D4!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D3!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D2!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D1!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D0!0 0 0 0.0 0 0 0.0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .

     B A B A B A B A B A B A B A B A N E B A B A B A B A N E B A B A
     5 5 4 4 3 3 2 2 1 1 0 0 9 9 8 8 E 0 7 7 6 6 9 9 8 8 E 0 7 7 6 6
```

TB01790S

c. Program Table of 10-Bit Comparator After Assembly of Boolean Equation File

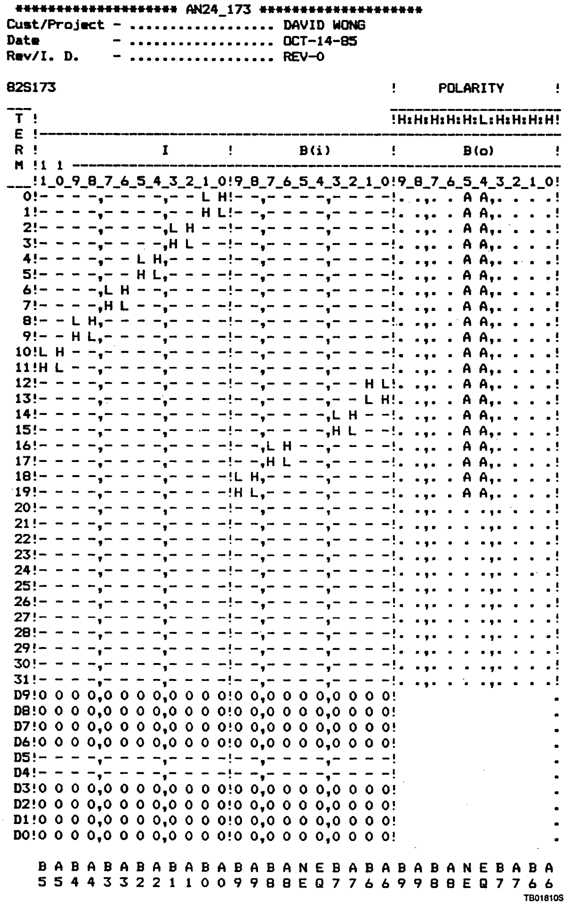
Figure 2 (Continued)

```
82S173    A:AN24_173.STD
" AMAZE FILE ID: AN24_173
" LOGIC SIMULATION OF 10-BIT COMPARATOR
"
" <==INPUTS==> <=B(I/O)=>   TRACE TERMS
" 11
" 109876543210 9876543210
"
  000000000000 0000LH0000 ;
  010000000000 0000HL0000 ;
  100000000000 0000HL0000 ;
  110000000000 0000LH0000 ;
  000100000000 0000HL0000 ;
  001000000000 0000HL0000 ;
  001100000000 0000LH0000 ;
  000001000000 0000HL0000 ;
  000010000000 0000HL0000 ;
  000011000000 0000LH0000 ;
  000000010000 0000HL0000 ;
  000000100000 0000HL0000 ;
  000000110000 0000LH0000 ;
  000000000100 0000HL0000 ;
  000000001000 0000HL0000 ;
  000000001100 0000LH0000 ;
  000000000001 0000HL0000 ;
  000000000010 0000HL0000 ;
  000000000011 0000LH0000 ;
  000000000000 0100HL0000 ;
  000000000000 1000HL0000 ;
  000000000000 1100LH0000 ;
  000000000000 0001HL0000 ;
  000000000000 0010HL0000 ;
  000000000000 0011LH0000 ;
  000000000000 0000HL0100 ;
  000000000000 0000HL1000 ;
  000000000000 0000LH1100 ;
  000000000000 0000HL0001 ;
  000000000000 0000HL0010 ;
  000000000000 0000LH0011 ;
"
" ------------ ----------   I/O CONTROL LINES
"              IIIIOOIIII   DESIGNATED I/O USAGE
"              IIIIOOIIII   ACTUAL I/O USAGE
"
" PINLIST...
" 13 11 10 09 08 07 06 05 04 03 02 01
" 23 22 21 20 19 18 17 16 15 14 ;
```

TB01800S

d. Test Vectors Generated by AMAZE After Logic Simulation

Figure 2 (Continued)



```
********************* AN24_173 *********************
Cust/Project - .................. DAVID WONG
Date         - .................. OCT-14-85
Rev/I. D.    - .................. REV-0

82S173                                         !     POLARITY      !

---                                            ---------------------
 T !                                           !H:H:H:H:H:L:H:H:H:H!
 E !----------------------------------------------------------------
 R !           I           !       B(i)        !       B(o)        !
 M !1 1 ------------------------------------------------------------
___!1_0_9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!- - - -,- - - -,- - L H!- -,- - - -,- - - -!. .,. . A A,. . . .!
  1!- - - -,- - - -,- - H L!- -,- - - -,- - - -!. .,. . A A,. . . .!
  2!- - - -,- - - -,L H - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
  3!- - - -,- - - -,H L - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
  4!- - - -,- - L H,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
  5!- - - -,- - H L,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
  6!- - - -,L H - -,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
  7!- - - -,H L - -,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
  8!- - L H,- - - -,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
  9!- - H L,- - - -,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
 10!L H - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
 11!H L - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . A A,. . . .!
 12!- - - -,- - - -,- - - -!- -,- - - -,- - H L!. .,. . A A,. . . .!
 13!- - - -,- - - -,- - - -!- -,- - - -,- - L H!. .,. . A A,. . . .!
 14!- - - -,- - - -,- - - -!- -,- - - -,L H - -!. .,. . A A,. . . .!
 15!- - - -,- - - -,- - - -!- -,- - - -,H L - -!. .,. . A A,. . . .!
 16!- - - -,- - - -,- - - -!- -,L H - -,- - - -!. .,. . A A,. . . .!
 17!- - - -,- - - -,- - - -!- -,H L - -,- - - -!. .,. . A A,. . . .!
 18!- - - -,- - - -,- - - -!L H,- - - -,- - - -!. .,. . A A,. . . .!
 19!- - - -,- - - -,- - - -!H L,- - - -,- - - -!. .,. . A A,. . . .!
 20!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 21!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 22!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 23!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 24!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 25!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 26!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 27!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 28!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 29!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 30!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 31!- - - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,. . . .!
 D9!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D8!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D7!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D6!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D5!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                  .
 D4!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                  .
 D3!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D2!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D1!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .
 D0!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                  .

      B A B A B A B A B A B A B A B A N E B A B A B A B A N E B A B A
      5 5 4 4 3 3 2 2 1 1 0 0 9 9 8 8 E Q 7 7 6 6 9 9 8 8 E Q 7 7 6 6
```

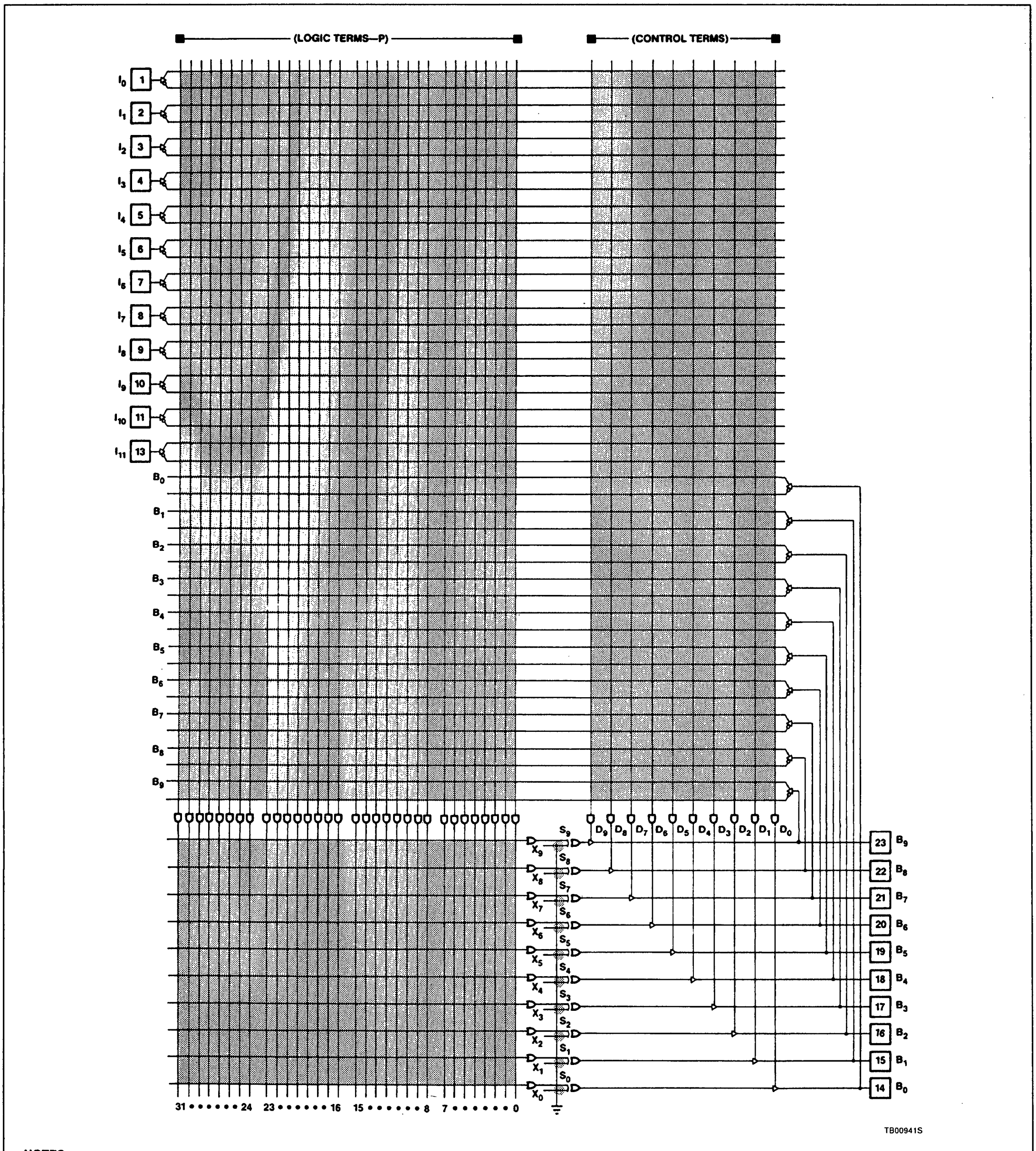
TB01810S

Figure 3. Program Table of 10-Bit Comparator with All Unused Terms Deleted

PLS173 as a 10-Bit Comparator, 74LS460 AN24

APPENDIX A

FPLA LOGIC DIAGRAM FOR PLS173



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ⬭ Programmable connection.

Signetics

AN25
A Simple Entry/Exit Metering Device

Application Note

Application Specific Products

DESCRIPTION

The following is the implementation of a counter/controller using a PLS157. This system counts and controls the number of entries to a certain media. For example, it can be used as a parking-lot controller to keep track of the number of cars entering a parking lot, and restricting any entries when the parking lot is full.

The design utilizes the six registers, six bi-directional I/O lines and the general architecture of the PLS157. In this design, the user can set the maximum number of entries using external switches. Since the six registers in the device are used as a six-bit counter, the maximum number that can be set is 2^6. However, the design can be cascaded to increase the number of entries.

SYSTEM OPERATION

The basic system configuration is shown in Figure 1. As can be seen from this figure, the system can be expanded indefinitely. All the devices in cascade are identical to each other. Whenever there is a need for expanding the maximum number of counts, a device can be programmed identical to the device(s) already in the system and added in cascade.

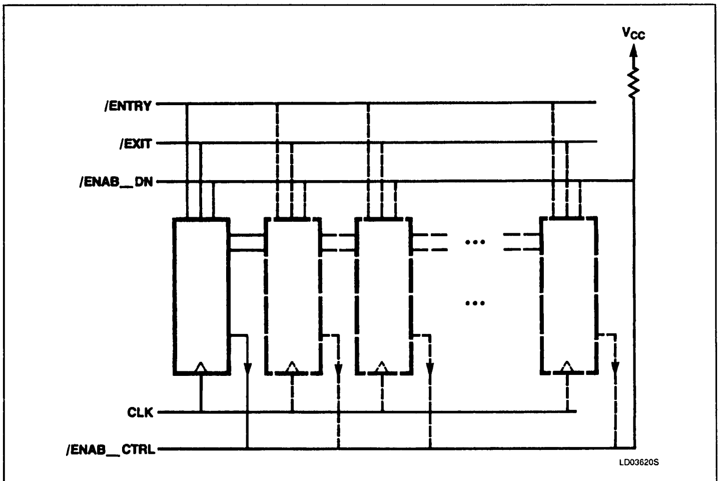


Figure 1. System Configuration

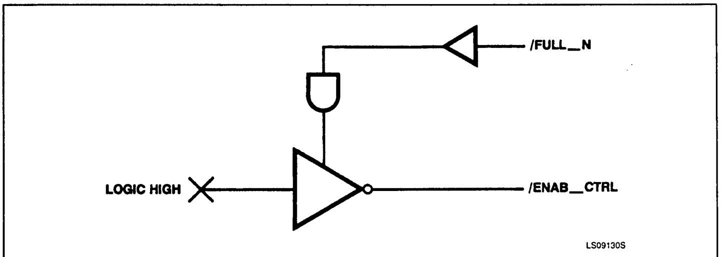


Figure 2. /ENAB_CTRL Output Configuration

There are external switches connected to the bi-directional inputs of the flip-flops. The user sets the maximum count in binary with the switches and loads the value into the registers. If the maximum count necessary exceeds the number available in one device, then another device is cascaded to the existing device. For example, in a system with two devices, the maximum available increases to 2^{12} or 4096.

When the maximum count is set, the control circuitry is used to keep track of the number of entries and exits. In the case of a parking lot, a pressure sensor can be used at the entrance and exit to generate a pulse which triggers the control circuitry. An alternative could be light beam sensors to generate the necessary pulses.

The operation of the system is such that each entry decreases the maximum count stored in the registers by one. When the count is zero, it means that the media is full and the control circuitry generates a signal to disable any further entries to the system. On the other hand, each exit increases the count by one. Since it is assumed that the media is empty when the maximum count is set, it is, therefore, impossible to physically count past the maximum set number. This is due to the fact that there cannot be more exits from the system than the actual number of objects residing in the system. If there are objects in the system when the maximum number is set, these objects should also be taken into consideration when setting the maximum count.

CONTROL SIGNALS

The following is the explanation of the control signals shown in Figure 1.

The /ENTRY and /EXIT inputs signify an entrance or exit to or from the respective media and are triggered from the sensors at the entrance and exit. Each entry causes a count-down from the maximum set number until all the flip-flops are low. This means that the system is full and the count-down should be disabled.

A Simple Entry/Exit Metering Device AN25

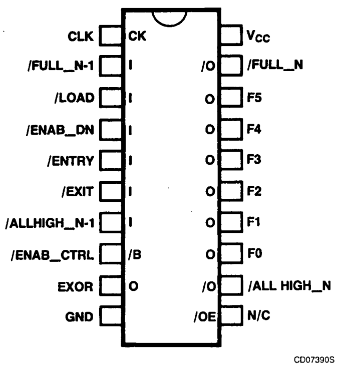


Figure 3. Single Device Configuration

When all the flip-flops are low, the /FULL_N signal which is an Active-Low output is activated. The count-down is enabled by the /ENAB_DN input, which is connected externally to the /ENAB_CTRL line. The /ENAB_CTRL is a Tri-state output which is controlled by the /FULL_N signal. When all the flip-flops are low, the /FULL_N signal deactivates the /ENAB_CTRL output as shown in Figure 2.

All of the /ENAB_CTRL outputs are connected to the /ENAB_CTRL bus as shown in Figure 1. When the media is full, all the /ENAB_CTRL signals are deactivated which cause the count-down to be disabled.

An exit causes a count up. As mentioned before, the total number of exits from the system cannot exceed the total number of entries.

The /ALLHIGH_N signal is an Active-Low output which becomes low when all the flip-flops are high. Figure 3 shows the configuration of a single device.

The /FULL_N and /ALLHIGH_N signals are used to activate the /FULL_N-1 and /ALLHIGH_N-1 of a cascaded device. These signals will be explained in detail shortly. The /FULL_N signal is also used to trigger any control circuitry used to restrict any further entries to the system. In the case of a parking lot, the /FULL_N can be used to activate a light or close the entrance gate.

The EXOR output is used to clock the system and is externally connected to the CLK input of the device. The EXOR generates a clock pulse when either an exit or entry take place. This restricts the system from counting if a simultaneous entry and exit takes place.

To set the maximum count, the user can use switches connected to inputs F0-F5 of the device(s). Then by bringing the /LOAD input low and triggering the /ENTRY or /EXIT inputs to generate a clock pulse, the data from these switches can be latched into the registers.

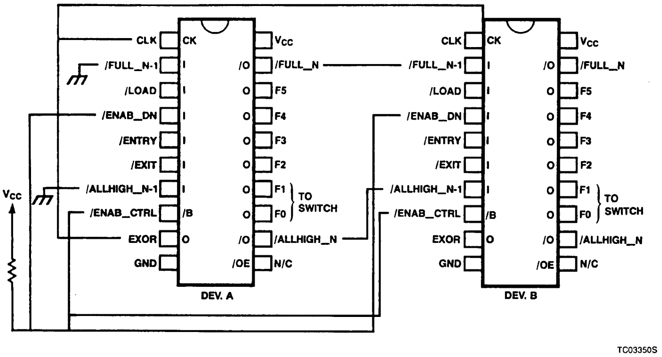


Figure 4. Cascaded Configuration

CASCADE DEVICE EXAMPLE

This is an example of two cascaded devices. Figure 4 shows the cascade configuration of devices 'A' and 'B'. For the sake of simplicity, it is assumed that each device contains only two registers. This assumption gives clarity to the explanation, and can be extended to cover the six registers contained in each device.

As an example, it is assumed that the maximum count to be implemented in this example is 1001 in binary. In other words, the maximum number of entries is set to be 'ten'. F0A and F1A are the registers in device A, and F0B and F1B are the registers in device B. 10 is the input sequence to device B and 01 is input sequence to device A.

The count-up and count-down sequences are shown in Table 1.

Table 1. An Up/Down Count Sequence Example

DEV. B		DEV. A		DEV. B		DEV. A	
F0B	F1B	F0A	F1A	F0B	F1B	F0A	F1A
1	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1
0	1	1	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	0	0	0	1	0	1
0	0	1	1	0	1	1	0
0	0	1	0	0	1	1	1
0	0	0	1	1	0	0	0
0	0	0	0	1	0	0	1
COUNT DOWN				COUNT UP			

TB02080S

Table 2. Count Sequence

NO.	F5	F4	F3	F2	F1	F0
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
4	0	0	0	1	0	0
	⋮	⋮	⋮	⋮	⋮	⋮
7	0	0	0	1	1	1
8	0	0	1	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮
15	0	0	1	1	1	1
16	0	1	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮
31	0	1	1	1	1	1
32	1	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮
62	1	1	1	1	1	0
63	1	1	1	1	1	1
0	0	0	0	0	0	0

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A Simple Entry/Exit Metering Device | AN25

In the 1001 example, F0B is the MSB (Most Significant Bit) and F1A is the LSB (Least Significant Bit). As can be seen in Table 1, a count-down occurs in device 'B', when F0A and F1A are both low. When F0A and F1A are low, this means that the /FULL_N signal is active. The /FULL_N-1 input of device 'B' is connected to the FULL_N output of device 'A'. Therefore, a count down occurs in device 'B' only when the input to /FULL_N-1 goes low. In this manner, the count-down sequence in Table 1 can be implemented.

Similarly, for the count-up sequence, a count-up occurs in device 'B' only when both F0A and F1A are high. At this point, the /ALLHIGH_N signal becomes active. Therefore, a count-up occurs in device 'B' only when /ALLHIGH_N of device 'A' is active.

UP/DOWN COUNTERS

An up-down counter is implemented in each device to keep track of the number of entries and exits. To implement these counters the flip-flops are set in the toggle mode. Table 2 shows the count sequence.

The following conditions are true for the count-up sequence:

Table 3a

REGISTER	TRUE CONDITION FOR TOGGLE
F0	Unconditionally Toggle
F1	F0
F2	F0*F1
F3	F0*F1*F2
F4	F0*F1*F2*F3
F5	F0*F1*F2*F3*F4

Similarly, for the count-down sequence:

Table 3b

REGISTER	TRUE CONDITION FOR TOGGLE
F0	Unconditionally Toggle
F1	/F0
F2	/F0*/F1
F3	/F0*/F1*/F2*
F4	/F0*/F1*/F2*/F3
F5	/F0*/F1*/F2*/F3*/F4*

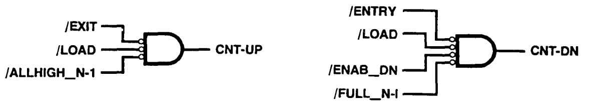


Figure 5. CNT-UP and CNT-DN Signals

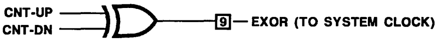
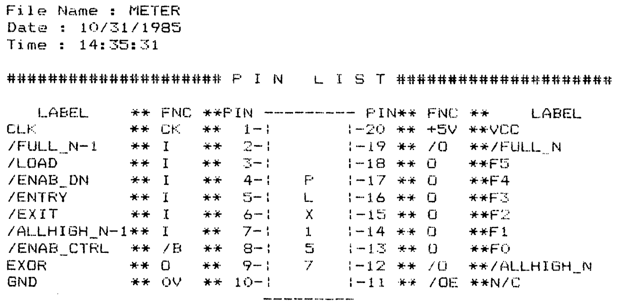


Figure 6. System Clock



```
File Name : METER
Date : 10/31/1985
Time : 14:35:31

###################### P I N   L I S T ######################

   LABEL      ** FNC **PIN ---------- PIN** FNC **     LABEL
CLK           ** CK  **  1-|          |-20 ** +5V **VCC
/FULL_N-1     ** I   **  2-|          |-19 ** /O  **/FULL_N
/LOAD         ** I   **  3-|          |-18 ** O   **F5
/ENAB_DN      ** I   **  4-|    P     |-17 ** O   **F4
/ENTRY        ** I   **  5-|    L     |-16 ** O   **F3
/EXIT         ** I   **  6-|    X     |-15 ** O   **F2
/ALLHIGH_N-1** I   **  7-|    1     |-14 ** O   **F1
/ENAB_CTRL    ** /B  **  8-|    5     |-13 ** O   **F0
EXOR          ** O   **  9-|    7     |-12 ** /O  **/ALLHIGH_N
GND           ** OV  ** 10-|          |-11 ** /OE **N/C
                            ----------
```

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Figure 7

CONTROL SIGNALS

The following are the control signals used to control the operation of the devices:

The logic diagram for generating the 'CNT-UP' and 'CNT-DN' signals is shown in Figure 5.

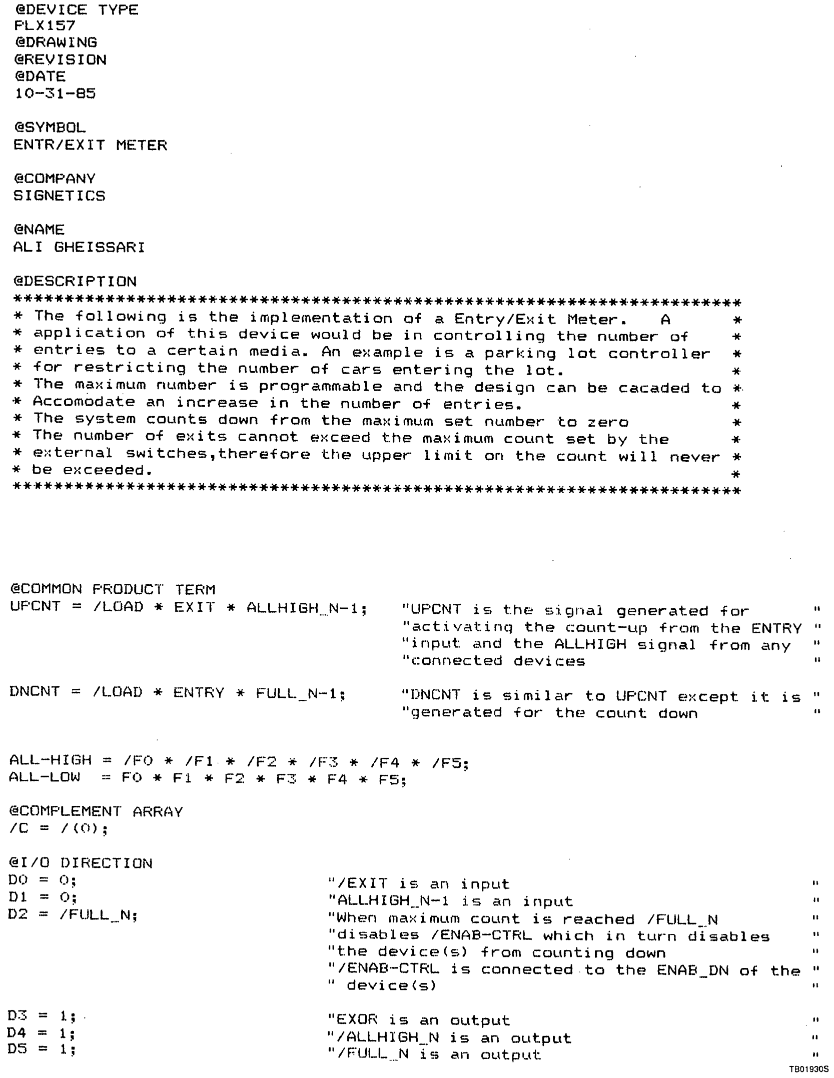
As can be seen from this figure, a count-up occurs when the following is true:
a) An exit takes place and,
b) the system is not loading in any data and,
c) the previous stage has generated the /ALLHIGH_N-1 signal.

A count-down occurs when:
a) An entry takes place and,
b) the system is not loading in any data and,
c) the previous stage has generated the /FULL_N-1 signal and,
d) the media is not full, thus /ENAB_DN signal is low.

The system clock is generated using the CNT-UP and CNT-DN signals. The system is to be clocked only when an exit or entry takes place. In order to prevent the system from being clocked when a simultaneous entry and exit takes place, these two signals are exclusive-OR'ed (Figure 6).

The equations shown in (Tables 3a and 3b) are generated using Signetics AMAZE software (Figures 7 and 8). The resulting program table is shown in Table 4.

A Simple Entry/Exit Metering Device AN25



```
@DEVICE TYPE
PLX157
@DRAWING
@REVISION
@DATE
10-31-85

@SYMBOL
ENTR/EXIT METER

@COMPANY
SIGNETICS

@NAME
ALI GHEISSARI

@DESCRIPTION
***********************************************************************
* The following is the implementation of a Entry/Exit Meter.   A      *
* application of this device would be in controlling the number of   *
* entries to a certain media. An example is a parking lot controller *
* for restricting the number of cars entering the lot.                *
* The maximum number is programmable and the design can be cacaded to *
* Accomodate an increase in the number of entries.                    *
* The system counts down from the maximum set number to zero          *
* The number of exits cannot exceed the maximum count set by the      *
* external switches,therefore the upper limit on the count will never *
* be exceeded.                                                        *
***********************************************************************



@COMMON PRODUCT TERM
UPCNT = /LOAD * EXIT * ALLHIGH_N-1;    "UPCNT is the signal generated for      "
                                       "activating the count-up from the ENTRY "
                                       "input and the ALLHIGH signal from any  "
                                       "connected devices                      "

DNCNT = /LOAD * ENTRY * FULL_N-1;      "DNCNT is similar to UPCNT except it is "
                                       "generated for the count down           "


ALL-HIGH = /F0 * /F1 * /F2 * /F3 * /F4 * /F5;
ALL-LOW  = F0 * F1 * F2 * F3 * F4 * F5;

@COMPLEMENT ARRAY
/C = /(0);

@I/O DIRECTION
D0 = 0;                         "/EXIT is an input                              "
D1 = 0;                         "ALLHIGH_N-1 is an input                        "
D2 = /FULL_N;                   "When maximum count is reached /FULL_N          "
                                "disables /ENAB-CTRL which in turn disables     "
                                "the device(s) from counting down               "
                                "/ENAB-CTRL is connected to the ENAB_DN of the "
                                " device(s)                                     "

D3 = 1;                         "EXOR is an output                              "
D4 = 1;                         "/ALLHIGH_N is an output                        "
D5 = 1;                         "/FULL_N is an output                           "
```

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Figure 8

A Simple Entry/Exit Metering Device

AN25

```
@OUTPUT POLARITY

X2 = 0;                          "/ENAB_CTRL is active low                     "
X3 = 1;                          "EXOR is active high                          "
X4 = 0;                          "/ALLHIGH_N is active low                     "
X5 = 0;                          "/FULL_N is active low                        "

@FLIP FLOP CONTROL
FC = 1;                           "All flip flops are J-K                      "

@OUTPUT ENABLE
"NOT USED"

@REGISTER LOAD
LA = LOAD;                        "Load the registers with the number set      "
LB = LOAD;                        "by the input switches                       "

@ASYNCHRONOUS PRESET/RESET
"NOT USED"

@FLIP FLOP MODE
"NOT USED"

@LOGIC EQUATION
EXOR = UPCNT*/DNCNT + DNCNT*/UPCNT;  "Output count pulse only if there is not  "
                                     "a simultaneous entry and exit            "
/FULL_N = /( ALL-LOW * /LOAD);       "indicates when maximum count is reached  "
/ALLHIGH_N = /( ALL-HIGH * /LOAD);   "shows when empty                         "
/ENAB_CTRL = /(1);                   "puts low on the ENAB_CTRL bus            "

"The following is the implementation of the counter together with the        "
"necessary logic."

/F0: T = (ENAB_DN * DNCNT) + UPCNT;


/F1: T = (ENAB_DN * F0 * DNCNT) + (/F0 * UPCNT);


/F2: T = (ENAB_DN * F0 * F1 * DNCNT) + (/F0 * /F1 * UPCNT);


/F3: T = (ENAB_DN * F0 * F1 * F2 * DNCNT) +
         (/F0 * /F1 * /F2 * UPCNT);

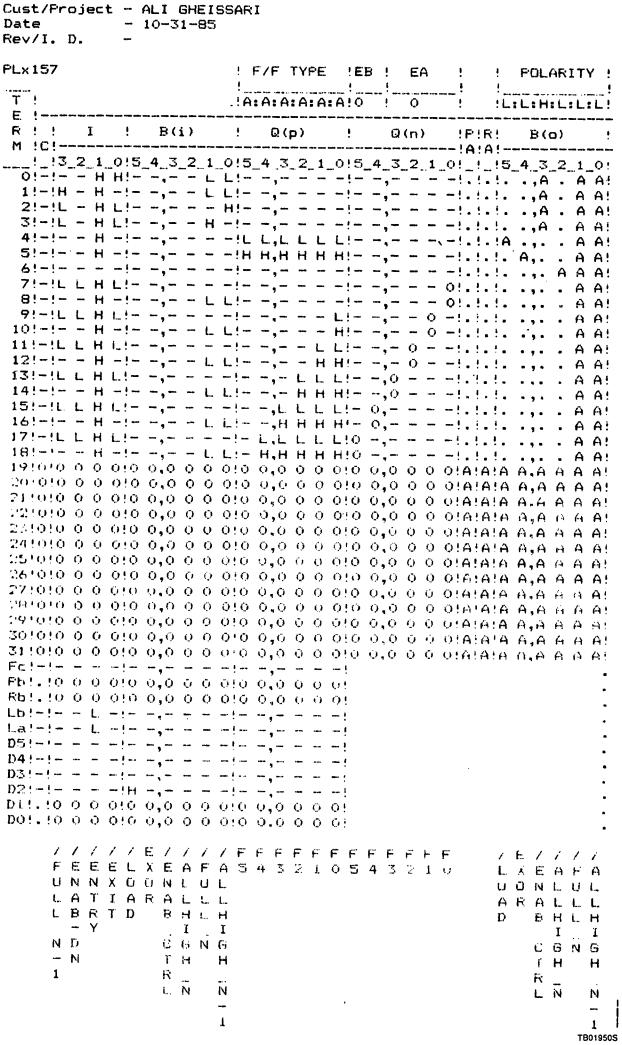

/F4: T = (ENAB_DN * F0 * F1 * F2 * F3 * DNCNT) +
         (/F0 * /F1 * /F2 * /F3 * UPCNT);


/F5: T = (ENAB_DN * F0 * F1 * F2 * F3 * F4 * DNCNT) +
         (/F0 * /F1 * /F2 * /F3 * /F4 * UPCNT);
```

TB01940S

Figure 8 (Continued)

Table 4. Program Table for Entry/Exit Meter



```
Cust/Project  - ALI GHEISSARI
Date          - 10-31-85
Rev/I. D.     -

PLx157                   ! F/F TYPE  !EB !  EA   !   !  POLARITY !
                         !___________!___!_______!   !___________!
 T !                    .!A:A:A:A:A:A!O  !  O    !   !L:L:H:L:L:L!
 E !--------------------------------------------------------------
 R ! !   I   !   B(i)  !   Q(p)   !   Q(n)   !F!R!  B(o)     !
 M !C!-------------------------------------------!A!A!------------
___!_!3_2_1_0!5_4_3_2_1_0!5_4_3_2_1_0!5_4_3_2_1_0!_!_!5_4_3_2_1_0!
  0!-!- - H H!- -,- - L L!- -,- - - -!- -,- - - -!.!.!. .,A . A A!
  1!-!H - H -!- -,- - L L!- -,- - - -!- -,- - - -!.!.!. .,A . A A!
  2!-!L - H L!- -,- - - H!- -,- - - -!- -,- - - -!.!.!. .,A . A A!
  3!-!L - H L!- -,- - H -!- -,- - - -!- -,- - - -!.!.!. .,A . A A!
  4!-!- - H -!- -,- - - -!L L,L L L L!- -,- - - -!.!.!A .,. . A A!
  5!-!- - H -!- -,- - - -!H H,H H H H!- -,- - - -!.!.!. A,. . A A!
  6!-!- - - -!- -,- - - -!- -,- - - -!- -,- - - -!.!.!. .,. A A A!
  7!-!L L H L!- -,- - - -!- -,- - - -!- -,- - - O!.!.!. .,. . A A!
  8!-!- - H -!- -,- - L L!- -,- - - -!- -,- - - O!.!.!. .,. . A A!
  9!-!L L H L!- -,- - - -!- -,- - - L!- -,- - O -!.!.!. .,. . A A!
 10!-!- - H -!- -,- - L L!- -,- - - H!- -,- - O -!.!.!. .,. . A A!
 11!-!L L H L!- -,- - - -!- -,- - L L!- -,- O - -!.!.!. .,. . A A!
 12!-!- - H -!- -,- - L L!- -,- - H H!- -,- O - -!.!.!. .,. . A A!
 13!-!L L H L!- -,- - - -!- -,- L L L!- -,O - - -!.!.!. .,. . A A!
 14!-!- - H -!- -,- - L L!- -,- H H H!- -,O - - -!.!.!. .,. . A A!
 15!-!L L H L!- -,- - - -!- -,L L L L!- O,- - - -!.!.!. .,. . A A!
 16!-!- - H -!- -,- - L L!- -,H H H H!- O,- - - -!.!.!. .,. . A A!
 17!-!L L H L!- -,- - - -!- L,L L L L!O -,- - - -!.!.!. .,. . A A!
 18!-!- - H -!- -,- - L L!- H,H H H H!O -,- - - -!.!.!. .,. . A A!
 19!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 20!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 21!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 22!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 23!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 24!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 25!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 26!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 27!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 28!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 29!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 30!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 31!0!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!A!A!A A,A A A A!
 Fc!-!- - - -!- -,- - - -!- -,- - - -!                           .
 Fb!.!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!                           .
 Rb!.!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!                           .
 Lb!-!- - L -!- -,- - - -!- -,- - - -!                           .
 La!-!- - L -!- -,- - - -!- -,- - - -!                           .
 D5!-!- - - -!- -,- - - -!- -,- - - -!                           .
 D4!-!- - - -!- -,- - - -!- -,- - - -!                           .
 D3!-!- - - -!- -,- - - -!- -,- - - -!                           .
 D2!-!- - - -!H -,- - - -!- -,- - - -!                           .
 D1!.!0 0 0 0!0 0,0 0 0 0!0 0,0 0 0 0!                           .
 D0!.!0 0 0 0!0 0,0 0 0 0!0 0.0 0 0 0!                           .

      / / / / / E / / / / F F F F F F F F F F F F     / E / / / /
      F E E E L X E A F A 5 4 3 2 1 0 5 4 3 2 1 0     L X E A F A
      U N N X O O N L U L                             U O N L U L
      L A T I A R A L L L                             A R A L L L
      L B R T D   B H L H                             D   B H L H
        - Y         I   I                                   I   I
      N D         C G N G                                 C G N G
      - N         T H   H                                 T H   H
      1           R _   _                                 R _
                  L N   N                                 L N   N
                        -                                       -
                        1                                       1
                                                          TB01950S
```

Signetics

AN26
PLHS18P8A Primer

Application Note

Application Specific Products

FEATURES

- **100% functional replacement for all 20-pin PALs**
- **I/O propagation delay: 20ns (max)**
- **Security fuse lock**
- **10 inputs**
- **8 bidirectional I/O lines**
- **Tri-state outputs have programmable polarity**
- **Architecture: 8 groups of nine AND gates. Total of 72 product terms**
- **Software support on Signetics AMAZE**
- **Complete TTL compatibility**
- **Each bidirectional I/O has individually controllable output enable**

ARCHITECTURE

The PLHS18P8A is an oxide-isolated, bipolar field-programmable logic array. This device is configured as a decoding two-level AND-OR (sum of products) structure. The PLHS18P8A block diagram is shown in Figure 1. All the AND gates are linked to ten inputs ($I_0 - I_9$) and eight bidirectional I/O lines ($B_{(0)} - B_{(7)}$). These links can be made via the on-chip true/complement buffers. The 72 AND gates are configured in 8 groups which contain 9 AND gates each. In every group, eight AND gates are used for user-defined logic functions and the ninth AND gate is used as a tri-state output enable control. This gives the user capability to control the output enable by means of a product term. The outputs of the eight logical product terms are ORed together (see Figure 1). The output polarity of each OR gate is individually programmable via an Exclusive-OR gate. The user has a choice of Active-Low or Active-High on each of the eight outputs. Figure 2 shows the logic diagram of the PLHS18P8A.

HOW A DEVICE IS PROGRAMMED

There are three main programmable sections on the PLHS18P8A:
A. The AND array.
B. The output polarity.
C. The security fuse.

A. The AND Array — The AND array fuses are back-to-back diode pairs which act as open connections in a virgin device. These open connections are configured as 'Don't Cares' (' – ') in an unprogrammed device. The open connections are pulled to a logic High ('1') (see Figure 3). Consequently, all unprogrammed AND locations are pulled to a logic High ('1') state. This means that in an unprogrammed device, all the product terms are active. During fusing, current is avalanched across individual diode pairs. This essentially short circuits the diode and provides a connection for the associated product term. Figure 3 shows how a typical connection is made to the AND array (see Appendix B for a description of the vertical fuses).

The inputs to the AND array consist of 10 dedicated inputs (I0 – I9) and 8 bidirectional I/Os (B(0) – B(7)). Initially, all these inputs are configured as 'Don't Cares' (' – '). These inputs can be connected to the AND array through an inverting or non-inverting buffer. The AND gate can be connected to the inverting buffer by programming the inverting fuse. Similarly, a connection can be made to the non-inverting buffer by programming the non-inverting fuse. Disabling an AND term is achieved by implementing a logical Low ('0') on the output of the specified AND gate. When both fuses of an input (e.g. I0 and $\overline{\text{I0}}$) are programmed, both the inverting and non-inverting buffers are connected to the inputs of the AND gate. To achieve this a '0' should be entered on the program table under the specified input. This will in turn create a logical Low ('0') on the output. To avoid any glitches on the output, it is a good practice to program all inputs to force a logical Low ('0').

In each block of nine AND gates, one gate is used as an output enable control for the tri-state output (Terms 0, 9, 18, 27, 36, 45, 54, 63, designated as D on Table 2). The remaining eight gates are connected to a fixed OR gate. Since in the unprogrammed state the outputs of all the AND gates are at logic High ('1'), the output of the OR gate also acquires a logic High state. Therefore the user is responsible for deactivating any unwanted product terms. This is done by creating a logic Low ('0') on the outputs of the unwanted product terms as previously explained. Moreover, the output buffer is always enabled since the product term controlling the tri-state output buffer also has a logic High state. If any of the bidirectional pins are to be defined as inputs, the product term controlling the specified bidirectional pin must be disabled. The bidirectional pin can also be configured as a dynamic I/O by defining the required logic for the output-enable-control product term.

The actual programming of the PLHS18P8A is carried out according to JEDEC[1] standards and the specific programming algorithm developed for the part.

According to JEDEC standards on data preparation for the PLD programmer, a "1" specifies a high impedance for the specified fuse and "0" a low impedance for the designated fuse.

For the AND array, the programming algorithm leaves the fuse intact (open-circuited) when a JEDEC "1" is specified. Consequently, a JEDEC "0" programs and short circuits the specified fuse. The programming algorithm is different for the output polarity and will be explained in the next paragraph on Special Conditions for the Output Polarity.

B. Special Conditions For The Output Polarity — In an unprogrammed device, all the output polarities are configured as inverting buffers. In this state, the device will have logic Low on all its outputs. The outputs of the PLHS18P8A are configured as tri-state buffers. The two inputs of each Ex-OR gate are connected as follows: one input is connected to the output of the fixed OR gate. The second input is a connection to ground (logic Low) through a fusible link.

As mentioned earlier, an unprogrammed fuse acts as an open connection which is pulled to a logic High. Therefore the output of the Ex-OR gate acts as an inverting buffer. When the fuse is programmed, there is a connection between ground (logic Low) and the input of the Ex-OR gate. This will cause the Ex-OR gate to act as a non-inverting buffer.

[1] For more information on standard data transfer format between the data preparation system and PLD programmer, refer to JEDEC — Solid State Engineering Council publications.

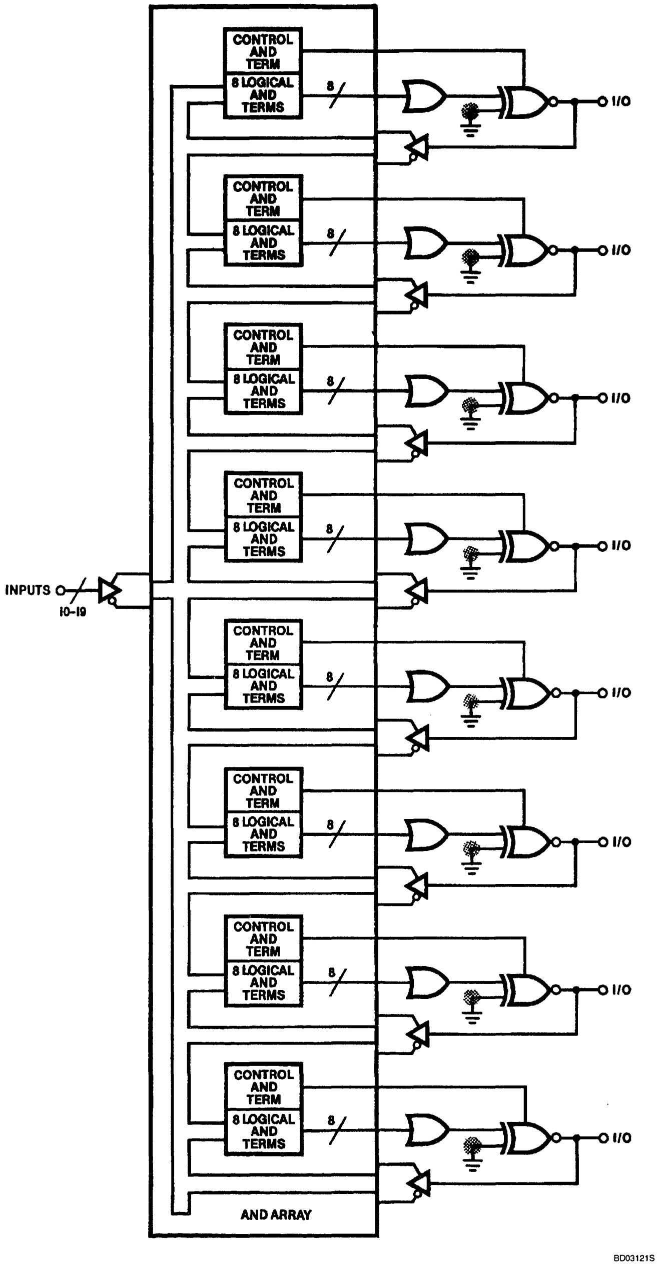
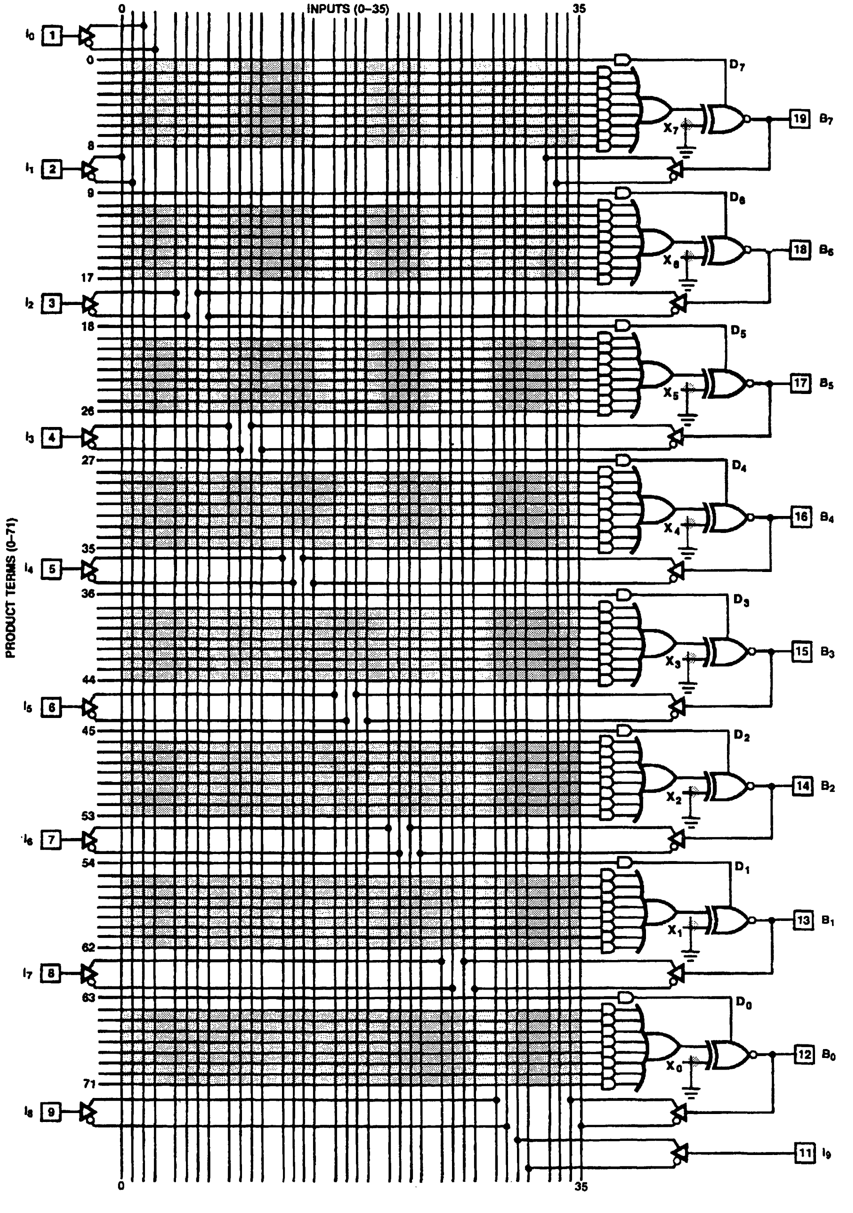
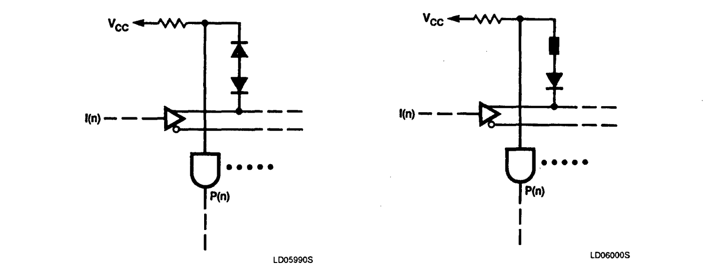


Figure 1. Block Diagram of the PLHS18P8A



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. All unprogrammed or virgin "OR" gate locations are pulled to logic "1".
3. ▨ Programmable corrections.

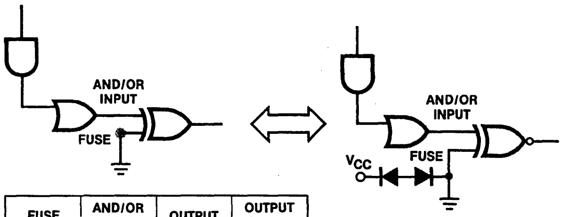
Figure 2. Logic Diagram of the PLHS18P8A



a. Unprogrammed Connection

b. Programmed. The Non-Inverting Buffer is Connected to the AND Gate

Figure 3. How a Fuse is Programmed



FUSE	AND/OR INPUT	OUTPUT	OUTPUT POLARITY
U	O	I	▷○
U	I	O	
P	O	O	▷
P	I	I	

P = PROGRAMMED
U = UNPROGRAMMED

Figure 4. Output Polarity Definition

Table 1. Programming Algorithm

JEDEC SPECIFICATION	AND ARRAY FUSE PROGRAMMING ALGORITHM	OUTPUT POLARITY FUSE PROGRAMMING ALGORITHM
1 — High impedance	Fuse unprogrammed (open circuit)	Fuse programmed (short circuit)
0 — Low impedance	Fuse programmed (short circuit)	Fuse unprogrammed (open circuit)

Figure 4 shows the definition of the output polarity for the PLHS18P8A. As can be seen, the output configuration of the PLHS18P8A is equivalent to an Ex-OR gate.

The programming algorithm for the output polarity section of the PLHS18P8A is different from that of the AND array. For the output polarity a JEDEC "1" (high impedance) programs (short circuits) the Ex-OR gate fuse, whereas a "0" (low impedance) leaves the fuse intact (open circuit).

The programming specifications are transparent to the user and do not need to be taken into consideration when designing with the PLHS18P8A. Table 1 shows the resulting programming algorithm from the JEDEC specification.

C. The Security Fuse — Programming equipment used to program the PLHS18P8A are capable of determining the logic pattern stored in this device (see Appendix A). The security fuse can be blown to disable the programmer from reading the pattern in a programmed device. This feature adds a measure of protection for proprietary designs.

The procedure for programming this fuse depends on the programmer manufacturer and is explained in the manufacturer's operations manual.

DESIGN TOOLS FOR THE PLHS18P8A

Many CAD tools such as Signetics' AMAZE software[2] are available to implement designs using the PLHS18P8A. The AMAZE software enables the user to enter the design in the form of Boolean equations or via the program table shown in Table 2. This program table is a one-to-one map of all the programmable links of Figure 2. The following explains the implementation of designs using the program table. Also, an example on using the Boolean Logic Entry program of the AMAZE software is given.

Using PTE (Program Table Entry) — Assume that Z is a typical logic function with the following equation:

Z = P0 + P1

Where P0 and P1 are product terms with the following equations:

P0 = A * /B * C

P1 = /A * B * /D

The program table in Table 2 is used to implement this equation. Table 3 shows the implementation of the logic function using the PTE. The first group of AND terms is used to implement this function. B(7) is used for the output, I0, I1, and I2 as inputs.

— Term 0 is the direction control term. It is the tri-state output enable control term. Since Z is configured as an output, leaving Term 0 in its unprogrammed state causes the output to be unconditionally enabled.

— Term 1 is the P-term labeled P0, where A*/B*C is designated by HLH in columns I0, I1, and I2.

— Term 2 is the P-term labeled P1, where /A*B*/D is designated by LHL in columns I0, I1, and I2.

— Terms 3, 4, 5, 6, 7. At least one input (or all the inputs) *must be set to zero* to disconnect these terms from the OR gate.

— The output polarity for B(7) is H, and this is entered in the 'Polarity' section.

Using BLAST (Boolean Logic And State Transfer) — The BLAST module in AMAZE can be used to implement the above equation. Figures 5 and 6 show the pin list and logic equation format. Table 4 is the program table generated from these equations.

[2] Refer to Signetics Programmable Logic Data Manual for a complete description of the AMAZE programmable logic development software.

PLHS18P8A Primer

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Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All p-terms are active until programmed otherwise.
4. Unused p-terms must be disabled or programmed with at least one pair of fuses.

CONTROL

HIGH	H	(POL)
LOW	L	

AND

INACTIVE	O	I,B(I)
I, B	H	
Ī, B̄	L	
DON'T CARE	—	

CUSTOMER NAME__________

PURCHASE ORDER # __________

SIGNETICS DEVICE # __________ CF (XXXX)

CUSTOMER SYMBOLIZED PART # __________

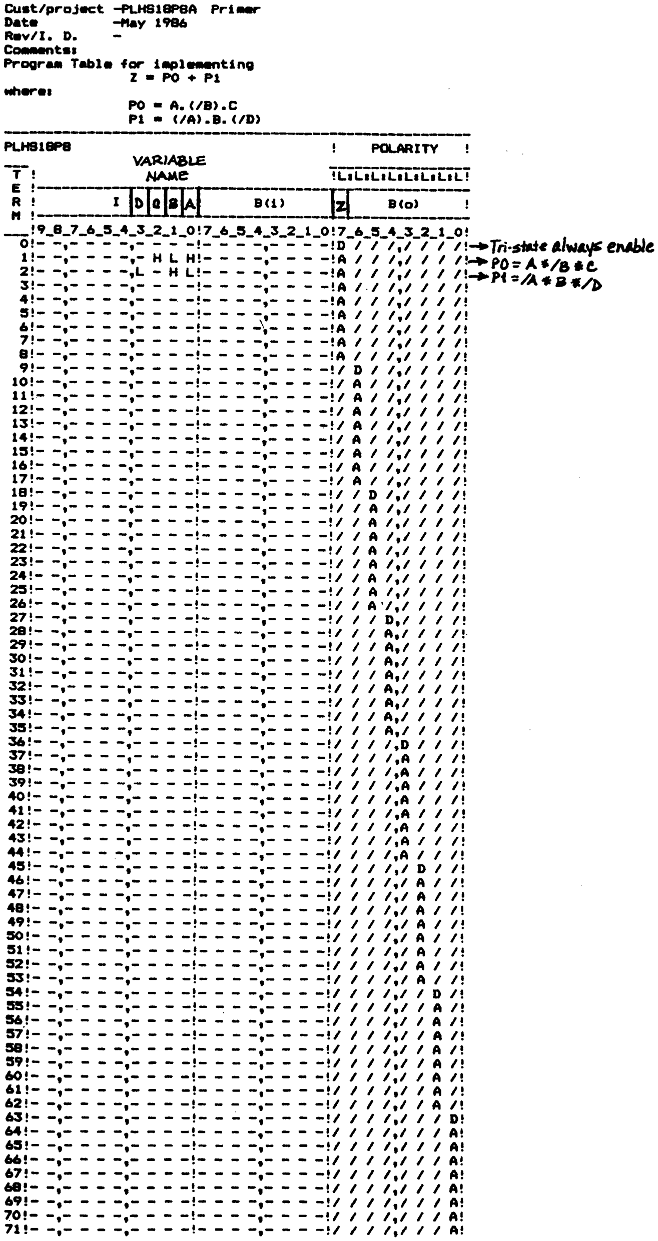
TOTAL NUMBER OF PARTS __________

PROGRAM TABLE # __________ REV __________ DATE __________

TERM	AND																		POLARITY OR (FIXED)							
	I										B (I)								B (O)							
	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																			D							
1																			A							
2																			A							
3																			A							
4																			A							
5																			A							
6																			A							
7																			A							
8																			A							
9																				D						
10																				A						
11																				A						
12																				A						
13																				A						
14																				A						
15																				A						
16																				A						
17																				A						
18																					D					
19																					A					
20																					A					
21																					A					
22																					A					
23																					A					
24																					A					
25																					A					
26																					A					
27																						D				
28																						A				
29																						A				
30																						A				
31																						A				
32																						A				
33																						A				
34																						A				
35																						A				
36																							D			
37																							A			
38																							A			
39																							A			
40																							A			
41																							A			
42																							A			
43																							A			
44																							A			
45																								D		
46																								A		
47																								A		
48																								A		
49																								A		
50																								A		
51																								A		
52																								A		
53																								A		
54																									D	
55																									A	
56																									A	
57																									A	
58																									A	
59																									A	
60																									A	
61																									A	
62																									A	
63																										D
64																										A
65																										A
66																										A
67																										A
68																										A
69																										A
70																										A
71																										A
PIN	11	9	8	7	6	5	4	3	2	1	19	18	17	16	15	14	13	12	19	18	17	16	15	14	13	12
VARIABLE NAME																										

TB02020S

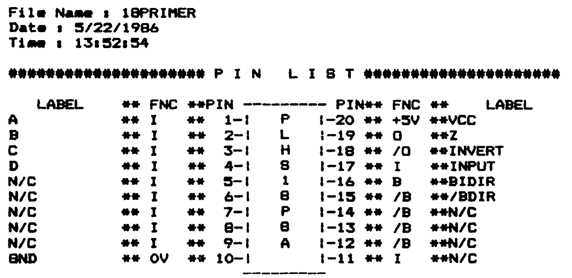
Table 2. Program Table



```
Cust/project -PLHS18P8A  Primer
Date         -May 1986
Rev/I. D.    -
Comments:
Program Table for implementing
                Z = PO + P1
where:
                PO = A.(/B).C
                P1 = (/A).B.(/D)
----------------------------------------------------------
PLHS18P8                                !   POLARITY   !
                VARIABLE
---               NAME                  ----------------
 T !                                    !L:L:L:L:L:L:L:L!
 E !-----------------------------------------------------
 R !          I |D|C|B|A|     B(i)     |Z|    B(o)      !
 M !-----------------------------------------------------
___!9_8_7_6_5_4_3_2_1_0!7_6_5_4_3_2_1_0!7_6_5_4_3_2_1_0!
  0!- -,- - - -,- - - -!- - - -,- - - -!D / / /,/ / / /!→Tri-state always enable
  1!- -,- - - -,- H L H!- - - -,- - - -!A / / /,/ / / /!→PO = A */B *C
  2!- -,- - - -,L - H L!- - - -,- - - -!A / / /,/ / / /!→P1 = /A * B */D
  3!- -,- - - -,- - - -!- - - -,- - - -!A / / /,/ / / /!
  4!- -,- - - -,- - - -!- - - -,- - - -!A / / /,/ / / /!
  5!- -,- - - -,- - - -!- - - -,- - - -!A / / /,/ / / /!
  6!- -,- - - -,- - - -!- - - -,- - - -!A / / /,/ / / /!
  7!- -,- - - -,- - - -!- - - -,- - - -!A / / /,/ / / /!
  8!- -,- - - -,- - - -!- - - -,- - - -!A / / /,/ / / /!
  9!- -,- - - -,- - - -!- - - -,- - - -!/ D / /,/ / / /!
 10!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 11!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 12!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 13!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 14!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 15!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 16!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 17!- -,- - - -,- - - -!- - - -,- - - -!/ A / /,/ / / /!
 18!- -,- - - -,- - - -!- - - -,- - - -!/ / D /,/ / / /!
 19!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 20!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 21!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 22!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 23!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 24!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 25!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 26!- -,- - - -,- - - -!- - - -,- - - -!/ / A /,/ / / /!
 27!- -,- - - -,- - - -!- - - -,- - - -!/ / / D,/ / / /!
 28!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 29!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 30!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 31!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 32!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 33!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 34!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 35!- -,- - - -,- - - -!- - - -,- - - -!/ / / A,/ / / /!
 36!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,D / / /!
 37!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 38!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 39!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 40!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 41!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 42!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 43!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 44!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,A / / /!
 45!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ D / /!
 46!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 47!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 48!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 49!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 50!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 51!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 52!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 53!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 54!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / D /!
 55!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 56!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 57!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 58!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 59!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 60!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 61!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 62!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 63!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / D!
 64!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 65!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 66!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 67!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 68!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 69!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 70!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 71!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
```

TB03071S

Table 3. Implementation of the Function "Z" Using PTE



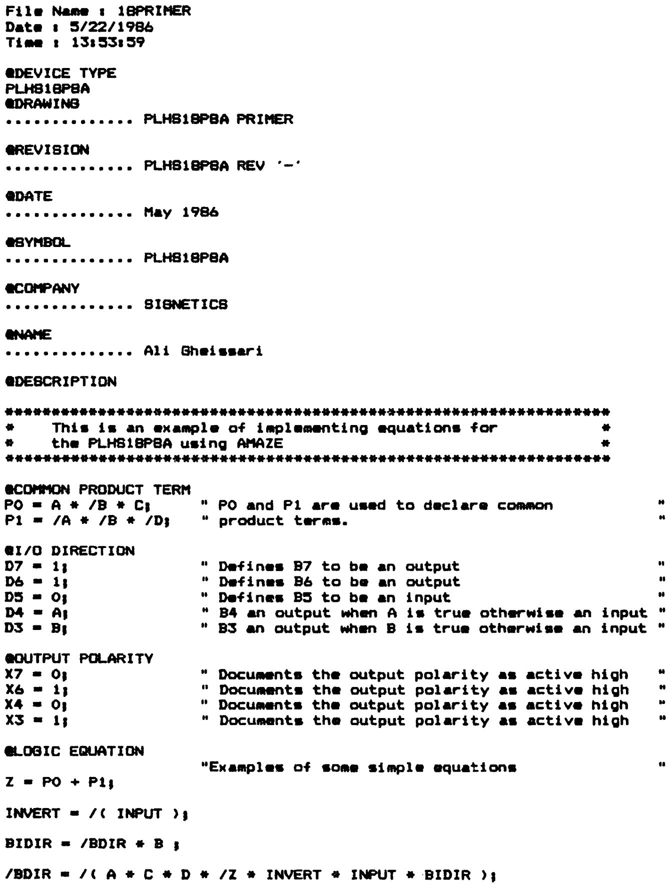
```
File Name : 18PRIMER
Date : 5/22/1986
Time : 13:52:54

######################## P I N   L I S T ########################

    LABEL      ** FNC **PIN ---------- PIN** FNC **     LABEL
A              ** I    **   1-|    P    |-20 ** +5V **VCC
B              ** I    **   2-|    L    |-19 ** O   **Z
C              ** I    **   3-|    H    |-18 ** /O  **INVERT
D              ** I    **   4-|    S    |-17 ** I   **INPUT
N/C            ** I    **   5-|    1    |-16 ** B   **BIDIR
N/C            ** I    **   6-|    8    |-15 ** /B  **/BDIR
N/C            ** I    **   7-|    P    |-14 ** /B  **N/C
N/C            ** I    **   8-|    8    |-13 ** /B  **N/C
N/C            ** I    **   9-|    A    |-12 ** /B  **N/C
GND            ** OV   ** 10-|          |-11 ** I   **N/C
                              ----------
```

TB03051S

Figure 5



```
File Name : 18PRIMER
Date : 5/22/1986
Time : 13:53:59

@DEVICE TYPE
PLHS18P8A
@DRAWING
.............. PLHS18P8A PRIMER

@REVISION
.............. PLHS18P8A REV '-'

@DATE
.............. May 1986

@SYMBOL
.............. PLHS18P8A

@COMPANY
.............. SIGNETICS

@NAME
.............. Ali Gheissari

@DESCRIPTION

*****************************************************************
*    This is an example of implementing equations for           *
*    the PLHS18P8A using AMAZE                                  *
*****************************************************************

@COMMON PRODUCT TERM
P0 = A * /B * C;         " P0 and P1 are used to declare common         "
P1 = /A * /B * /D;       " product terms.                               "

@I/O DIRECTION
D7 = 1;                  " Defines B7 to be an output                   "
D6 = 1;                  " Defines B6 to be an output                   "
D5 = 0;                  " Defines B5 to be an input                    "
D4 = A;                  " B4 an output when A is true otherwise an input "
D3 = B;                  " B3 an output when B is true otherwise an input "

@OUTPUT POLARITY
X7 = 0;                  " Documents the output polarity as active high   "
X6 = 1;                  " Documents the output polarity as active high   "
X4 = 0;                  " Documents the output polarity as active high   "
X3 = 1;                  " Documents the output polarity as active high   "

@LOGIC EQUATION
                         "Examples of some simple equations             "
Z = P0 + P1;

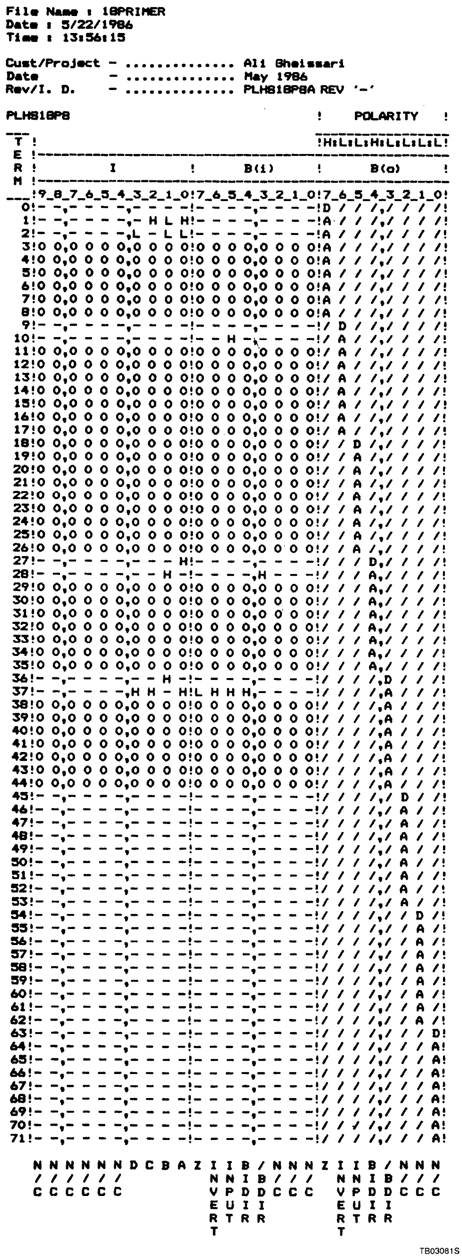
INVERT = /( INPUT );

BIDIR = /BDIR * B ;

/BDIR = /( A * C * D * /Z * INVERT * INPUT * BIDIR );
```

TB03061S

Figure 6. Boolean Equation File



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File Name : 18PRIMER
Date : 5/22/1986
Time : 13:56:15

Cust/Project - ............... Ali Gheissari
Date         - ............... May 1986
Rev/I. D.    - ............... PLHS18P8A REV '-'

PLHS18P8                               !    POLARITY     !
---                                     ------------------
 T !                                   !H:L:L:H:L:L:L:L!
 E !-----------------------------------------------------
 R !         I         !      B(i)     !      B(o)      !
 M !-----------------------------------------------------
___!9_8_7_6_5_4_3_2_1_0!7_6_5_4_3_2_1_0!7_6_5_4_3_2_1_0!
  0!- -,- - - -,- - - -!- - - -,- - - -!D / / /,/ / / /!
  1!- -,- - - -,- H L H!- - - -,- - - -!A / / /,/ / / /!
  2!- -,- - - -,L - L L!- - - -,- - - -!A / / /,/ / / /!
  3!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A / / /,/ / / /!
  4!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A / / /,/ / / /!
  5!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A / / /,/ / / /!
  6!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A / / /,/ / / /!
  7!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A / / /,/ / / /!
  8!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A / / /,/ / / /!
  9!- -,- - - -,- - - -!- - - -,- - - -!/ D / /,/ / / /!
 10!- -,- - - -,- - - -!- - H -,- - - -!/ A / /,/ / / /!
 11!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ A / /,/ / / /!
 12!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ A / /,/ / / /!
 13!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ A / /,/ / / /!
 14!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ A / /,/ / / /!
 15!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ A / /,/ / / /!
 16!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ A / /,/ / / /!
 17!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ A / /,/ / / /!
 18!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / D /,/ / / /!
 19!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 20!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 21!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 22!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 23!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 24!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 25!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 26!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / A /,/ / / /!
 27!- -,- - - -,- - - H!- - - -,- - - -!/ / / D,/ / / /!
 28!- -,- - - -,- - H -!- - - -,H - - -!/ / / A,/ / / /!
 29!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / A,/ / / /!
 30!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / A,/ / / /!
 31!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / A,/ / / /!
 32!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / A,/ / / /!
 33!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / A,/ / / /!
 34!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / A,/ / / /!
 35!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / A,/ / / /!
 36!- -,- - - -,- - H -!- - - -,- - - -!/ / / /,D / / /!
 37!- -,- - - -,H H - H!L H H H,- - - -!/ / / /,A / / /!
 38!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / /,A / / /!
 39!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / /,A / / /!
 40!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / /,A / / /!
 41!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / /,A / / /!
 42!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / /,A / / /!
 43!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / /,A / / /!
 44!0 0,0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!/ / / /,A / / /!
 45!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ D / /!
 46!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 47!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 48!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 49!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 50!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 51!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 52!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 53!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ A / /!
 54!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / D /!
 55!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 56!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 57!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 58!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 59!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 60!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 61!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 62!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / A /!
 63!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / D!
 64!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 65!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 66!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 67!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 68!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 69!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 70!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!
 71!- -,- - - -,- - - -!- - - -,- - - -!/ / / /,/ / / A!

    N N N N N N D C B A Z I I B / N N N Z I I B / N N N
    / / / / / /           N N I B / / /   N N I B / / /
    C C C C C C           V P D D C C C   V P D D C C C
                          E U I I         E U I I
                          R T R R         R T R R
                          T               T
```

TB03081S

Table 4. Programming Table Generated by AMAZE

APPENDIX A

Programmers

The PLHS18P8A can be programmed by means of logic programming equipment. With Logic Programming, the AND/Ex-OR gate input connections necessary to implement the desired logic are coded directly from the logic equations using the program table shown in Table 2.

The symbols used in the program table correspond to the fusing pattern of the corresponding link pairs, defined in Figure 6.

To program the device, the address of every fuse to be programmed must be entered in the programmer. This is a tedious and error-prone method of implementing the required logic pattern. Using CAD software, such as Signetics' AMAZE software, enables users to go directly from program table or logic equations to a fuse plot. The fuse plot can be downloaded to a programmer through a serial port. The downloaded fuse plot is in JEDEC format.

APPENDIX B

The vertical fuse is the latest in programmable logic technology. It combines reliability, low capacitance and testability in an incredibly small space.

The vertical fuse takes advantage of the properties of silicon and aluminum. The virgin fuse is a three-layer device: a shallow layer of N-type silicon on top, a layer of P-type silicon in the middle, and a layer of N-type silicon on the bottom. This forms a pair of PN diodes, back-to-back, which will not allow current to pass under normal circumstances.

There is a cap of aluminum on top of this structure. During programming, high current conditions (50 to 100 times what is seen during normal operation) is induced by avalanche breakdown of the reverse-biased diode. The aluminum will "spike" through the shallow N-type layer. Once the aluminum has spiked through, the top diode in the pair is shorted out. The whole vertical fuse will then look like a pure PN diode. Before programming, the fuse is an excellent blocking element, having current leakages in the order of nanoamps. After programming, the fuse is set as a small, well-defined diode.

QUALITY

Besides the AC and DC parametrics, each and every fuse goes through three tests for forward characteristics, reverse characteristics, and programmability. Extensive on-chip test circuitry ensures full AC parametric testing before and after the part is programmed. This insures that the customer receives the highest possible fusing yield which is made possible by vertical fuses. Vertical fuses also offer the smallest and fastest array structure together with the highest reliability possible.

APPENDIX C

Test Array

The PLHS18P8A may be subjected to AC and DC parametric tests prior to programming via an on-chip test array. Table C1 shows the test columns in the part. The test sequence is as follows.

Test column 1 is connected to B(O)0, 2, 4, 6 while test column 2 is connected to B(O)1, 3, 5, 7. Applying 10V to Pin 11 will put all the outputs in the Active-High mode and tri-state its associated input buffer.

Applying 10V to Pin 8 will disable B(O) 0 – 3, enable B(O) 4 – 7, tri-state B(I) 4 – 7, tri-state its associated input buffer, disable the AND array and enable test columns 1 and 2. The test columns are defined during programming by the PLD programmer.

Table C1. Test Columns of PLHS18P8A

TEST COLUMN	INPUTS																	
	Is										B(Is)							
	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

Signetics

AN27
PLHS473 Primer

Application Note

Application Specific Products

INTRODUCTION

The PLHS473 is a 24-pin field- programmable logic array (FPLA) which has 11 dedicated inputs, 2 dedicated outputs and 9 bidirectional I/Os. The logic array consists of 24 programmable product terms which are connected to 22 programmable OR terms in the classical PLA architecture. A functional diagram is shown in Figure 1. The shaded areas represent programmable interconnects between vertical and horizontal lines. Eleven dedicated inputs, I_0 to I_{10}, are located on the upper lefthand corner of the diagram, and the 9 bidirectional I/Os, B_0 to B_8 are located on the lower righthand corner. All inputs to the AND array have true and inverting input buffers. The output portion of the 9 bidirectional I/Os and 2 outputs may be programmed to be Active-High or Active-Low by altering fuses X_0 to X_8, X_A and X_B which are connected to one leg of the Exclusive-OR gates. Each output is connected to two OR-terms, one of which provides the logic function OR to the output while the other provides the ENABLE function for the tri-state output buffer. Alternatively, each output may be configured to emulate an open-collector output by programming the output to an unconditional LOW and apply the logic function on the tri-state controlling OR-term as shown in Figure 2. In addition, the PLHS473 has a security fuse which may be programmed to lock out unauthorized access to the fuse map of the design.

This device is fabricated with an oxide-isolation process for the best speed/power performance. The programmable element is a "vertical fuse" which is actually two PN diodes connected back-to-back (anode-to-anode stacked on top of one another) as shown in the insets of Figure 1. The fuses are normally open-circuited. To program a fuse, a sufficiently high voltage is applied across the two diodes such that one diode breaks down which induces metal migration across the PN junction of the avalanched diode. This technology allows smaller chip size and faster speed performance. The guaranteed propagation delay may be tested by using the two factory-programmed test columns and a test row as a test vehicle for speed testing. These test columns are to be deleted automatically in the process of programming.

The vertical fuses of an unprogrammed device, being normally open-circuited, set all AND terms to a High state and disconnected to all OR terms. The OR terms are normally Low when they are not connected to the AND terms. Once an AND term is programmed to make connections with the OR array, it cannot be disconnected. However, AND terms may be disabled by having the true and inverting input buffers (e.g., A * /A, B * /B, etc.) of all inputs connected to the AND term which is to be disabled.

While even a single input, (A * /A), will hold the AND term to a Low, glitches may develop if the input voltage changes state. Therefore, it is recommended that the complementary buffers of all inputs in the disabled AND term be connected.

Programming the PLHS473

The programming table and symbols of the PLHS473 are shown in Table 1 where there is a place for every function that is shown in Figure 1. The table is divided into two main sections. The left side of the table, sections A and B, represents the input side of the AND array (section A has all dedicated inputs I_0 to I_{10}, section B has inputs from the bidirectional I/Os B_0 to B_8), whereas the right side, sections C, D, and E, represents the outputs of the OR array. Section C represents the OR array which controls the tri-state output buffers of the bidirectional I/Os B_0 to B_8 and outputs O_A and O_B, while section D represents the OR array which drives the outputs. Section E controls the output polarity of each output. As shown in Table 1, the program table is very similar to a truth table. Each row represents one of the 24 product terms, while each column in sections A and B represents an input to the 24 product terms and in sections C and D, each column represents an output. The intersection of a column and a row in sections A and B represents four possible fuse configurations, namely, 1) both inverting and non-inverting input buffers are connected to the AND term, 2) only the inverting buffer is connected, 3) only the non-inverting input buffer is connected, and 4) both inverting and non-inverting buffers are disconnected. These four configurations are represented as "0", "L", "H", and " – ", respectively. Each intersection of a row and a column in sections C and D involves only two fuse configurations, either connected or disconnected. Therefore, the entry there is either "A" or " – ", respectively. In the polarity control section (section E), each square represents the configuration of the fuse connected to the Exclusive-OR, which is connected to a particular output pin. An "H" represents an Active-High or non-inverting output, an "L" represents an Active-Low or inverting output. See Table 1 for further details.

PLHS473 Primer

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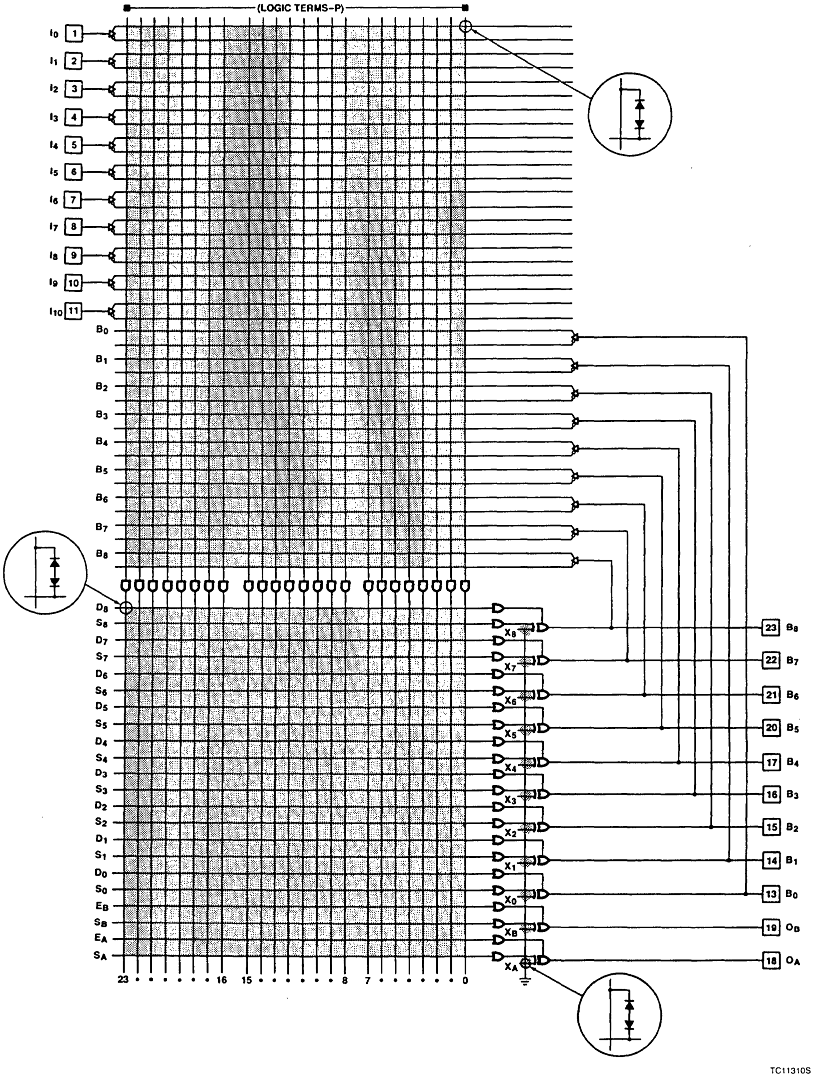

NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. All unprogrammed or virgin "OR" gate locations are pulled to logic "0".
3. ◍ Programmable connections.

Figure 1. PLHS473 Logic Diagram

PLHS473 Primer

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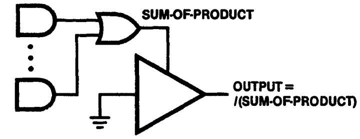


Figure 2. Emulation of Open-Collector Output

Notice that as shown in Figure 1, all fuses in their unprogrammed state are normally open-circuited. This means that all product terms are initially disconnected to the OR array, all OR gates are initially at a logic LOW, and all output pins are initially in High-Z state. Therefore, if anys of the outputs are to be enabled, its controlling OR term must be set to a logic HIGH. An example is shown in Table 2, term 0 where pins O_A, O_B $B(O)_8$ are programmed as dedicated outputs. The input section of term 0 is entirely "dashed out" (this is actually its unprogrammed state) which causes the AND term to be unconditionally HIGH. OR terms E_A, E_B, and D_8 are connected to product term 0 by the "A" entries in their respective squares. The rest of the D section and the B(O) section are "dotted out" (left unconnected) since we are not concerned with them for the moment. If more outputs are needed later on, their corresponding squares may be changed to "As" from "dots" as the need arises.

Table 1. PLHS473 Programming Table

CUSTOMER NAME ____________________
PURCHASE ORDER # ____________________
SIGNETICS DEVICE # __________ CF (XXXX) __________
CUSTOMER SYMBOLIZED PART # ____________________
TOTAL NUMBER OF PARTS ____________________
PROGRAM TABLE # ________ REV ________ DATE ________

AND

INACTIVE	0	I,B(I)
I, B	H	
$\bar{I}$, $\bar{B}$	L	
DON'T CARE	—	

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

HIGH	H	(POL)
LOW	L	

SECTION E

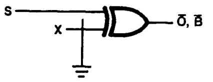
POLARITY										

TERM	AND																			
	I											B (I)								
	10	9	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
0																				
1																				
2																				
3																				
4																				
5																				
6																				
7																				
8																				
9																				
10																				
11																				
12						SECTION A										SECTION B				
13																				
14																				
15																				
16																				
17																				
18																				
19																				
20																				
21																				
22																				
23																				
PIN	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	17	16	15	14	13
VARIABLE NAME																				

TERM	OR																					
	E		D									O		B (O)								
	B	A	8	7	6	5	4	3	2	1	0	B	A	8	7	6	5	4	3	2	1	0
0																						
1																						
2																						
3																						
4																						
5																						
6																						
7																						
8																						
9																						
10																						
11																						
12							SECTION C											SECTION D				
13																						
14																						
15																						
16																						
17																						
18																						
19																						
20																						
21																						
22																						
23																						
												19	18	23	22	21	20	17	16	15	14	13

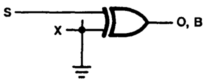
Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All P-terms are inactive on all outputs (B, O) in the virgin array.
4. Unused product terms can be left blank.

OUTPUT POLARITY — (0, B)



ACTIVE LEVEL	CODE
LOW[1]	L

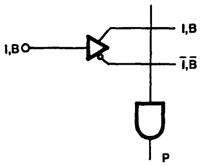
TC02560S



ACTIVE LEVEL	CODE
HIGH	H

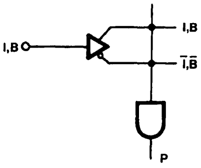
TC02570S

AND ARRAY — (I, B)



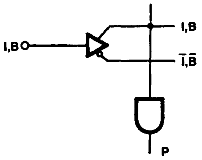
STATE	CODE
DON'T CARE[1]	-

TC02600S



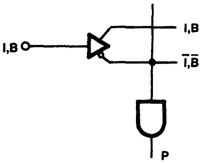
STATE	CODE
INACTIVE[2]	O

TC02630S



STATE	CODE
I, B	H

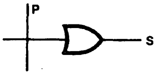
TC02610S



STATE	CODE
$\bar{I}, \bar{B}$	L

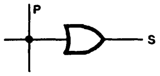
TC02620S

OR ARRAY — (O, B)



P_n STATUS	CODE
INACTIVE[1]	•

TC02580S

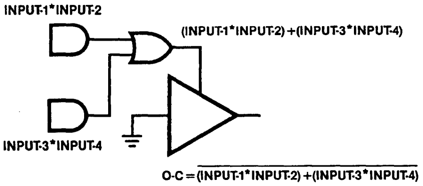


P_n STATUS	CODE
ACTIVE[1]	A

TC02590S

NOTES:

1. This is the initial unprogrammed state of all link pairs.
2. Any gate P_n will be unconditionally inhibited if any one of its (I, B) link pairs is programmed for a connection.


INPUT-1*INPUT-2
(INPUT-1*INPUT-2)+(INPUT-3*INPUT-4)
INPUT-3*INPUT-4
O-C = $\overline{(INPUT-1*INPUT-2)+(INPUT-3*INPUT-4)}$

TC11330S

Figure 3. Emulation of Open-Collector Output

VIRGIN STATE

A factor shipped virgin device contains all fusible links.

1. All output at "L" polarity.
2. All P_n terms are enable.
3. All P_n terms are active on all outputs.

Once we have determined the outputs, we can proceed with defining the logic functions. As an example, the logic function

OUT-0 = INPUT-1* /INPUT-2

is shown in Table 2, term #2 where in the column labeled "INPUT-1", an "H" is entered to represent a connection of the non-inverting input buffer of INPUT-1 and the AND term 2. In the column labelled "INPUT-2", an "L" is entered to represent the connection of the inverting input buffer of INPUT-1 and the AND term 2. On the output side of the table, O_B in term 0 is programmed "A" to make a connection between term 2 and the OR term which is connected to the output pin O_B: The output polarity of O_B is arbitrarily set to Active-High by programming an "H" in the O_B column of the polarity section.

A sum of several product terms (AND-OR) is implemented by connecting multiple AND terms to the same OR term. An example is shown in Table 2, terms 4 and 5, which implement the logic function

OUT-1 = (INPUT-1 */INPUT-2) +
(INPUT-3 * INPUT-4)

The logic function

OUT-2 = /((INPUT-1 * INPUT-2) +
(INPUT-3 * INPUT-4))

is shown in terms 9 and 10. The output is Active-Low as programmed "L" in the polarity section of OUT-2. As a rule, the AND function is implemented in a row, whereas the OR function is implemented in a column. Since the AND portions of terms 2 and 4 are the same, they may be combined as shown in term 7, which saves a duplicated term.

Table 2 terms 12 and 13 together emulate an open-collector output as an example. The logic equation

O-C = /((INPUT-1 * INPUT-2) +
(INPUT-3 * INPUT-4))

is implemented by first programming O-C Active-High in the polarity section. Terms 12 and 13 implement the sum of product function. Notice that the B(O) of O-C is programmed as a "dot" in both terms 12 and 13, which, together with the polarity control, causes it to be unconditionally Low, since a disconnected OR term is unconditionally Low. The intersections of column D_7 and terms 12 and 13 are programmed "A" so that the tri-state output buffer of $B(O)_7$ is enabled at input conditions (INPUT-1 * INPUT-2) = 1 or (INPUT-3 * INPUT-4) = 1. Terms 10 and 11 may be represented as shown in Figure 3.

Signetics produces a software package, AMAZE, as a design tool which assists implementation of logic design and documentation. For further information on AMAZE software, refer to the AMAZE User's Manual. Two simple circuits shown as examples are implemented using AMAZE. The first circuit is a simple cross-coupled RS latch. The second circuit is a multiplexer/demultiplexer which multiplexes four inputs to one output or demultiplexes one input into four outputs. Both circuits are put into the same PLHS473 device.

Table 2. Examples of Programming PLHS473

CUSTOMER NAME ____
PURCHASE ORDER # ____
SIGNETICS DEVICE # ____ CF (XXXX) ____
CUSTOMER SYMBOLIZED PART # ____
TOTAL NUMBER OF PARTS ____
PROGRAM TABLE # ____ REV ____ DATE ____

AND

INACTIVE	0	
I, B	H	I,B(I)
Ī, B̄	L	
DON'T CARE	—	

OR

ACTIVE	A	B(O)
INACTIVE	•	

CONTROL

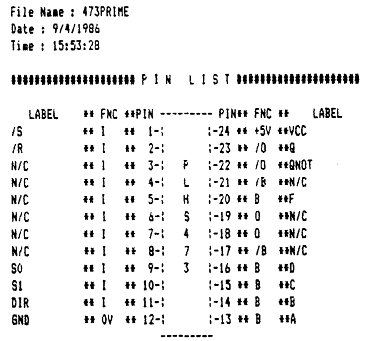
HIGH	H	(POL)
LOW	L	

TERM	AND																			
	I											B (I)								
	10	9	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
0	—	—	—	—	—	—	—	—	—	—			—	—	—	—	—	—	—	—
1																				
2	H	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3																				
4	H	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	—	—	H	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6																				
7	H	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8																				
9	H	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	H	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11																				
12	H	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	H	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14																				
15																				
16																				
17																				
18																				
19																				
20																				
21																				
22																				
23																				
PIN	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	17	16	15	14	13
VARIABLE NAME	INPUT-1	INPUT-2	INPUT-3	INPUT-4																

TERM	OR																					
POLARITY												H	H	L								
	E		D									O		B (O)								
	B	A	8	7	6	5	4	3	2	1	0	B	A	8	7	6	5	4	3	2	1	0
0	A	A	A	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
1																						
2	•	•	•	•	•	•	•	•	•	•	•	A	•	•	•	•	•	•	•	•	•	•
3																						
4	•	•	•	•	•	•	•	•	•	•	•	•	A	•	•	•	•	•	•	•	•	•
5	•	•	•	•	•	•	•	•	•	•	•	•	A	•	•	•	•	•	•	•	•	•
6																						
7	•	•	•	•	•	•	•	•	•	•	•	A	A	•	•	•	•	•	•	•	•	•
8																						
9	•	•	•	•	•	•	•	•	•	•	•	•	•	A	•	•	•	•	•	•	•	•
10	•	•	•	•	•	•	•	•	•	•	•	•	•	A	•	•	•	•	•	•	•	•
11																						
12	•	•	•	A	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
13	•	•	•	A	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
14																						
15																						
16																						
17																						
18																						
19																						
20																						
21																						
22																						
23																						
PIN												19	18	23	22	21	20	17	16	15	14	13
VARIABLE NAME												OUT-Ø	OUT-1	OUT-2	O-C							

Notes
1. The FPLA is shipped with all links open.
2. Unused I and B bits in the AND array exist as Don't Care (–) in the virgin state.
3. All P-terms are inactive on all outputs (B, O) in the virgin array.
4. Unused product terms can be left blank.

TB03100S



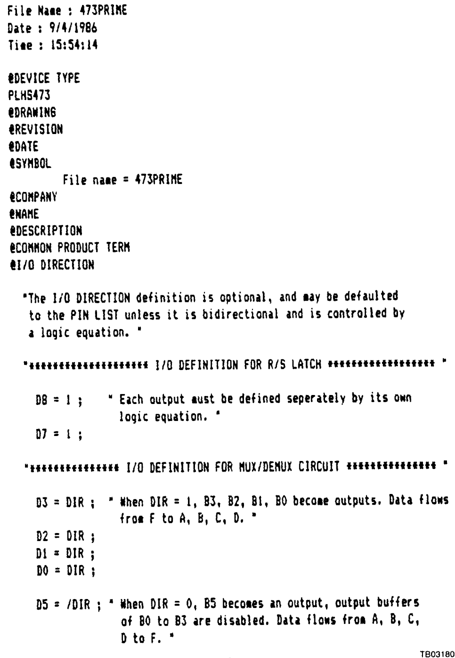
```
File Name : 473PRIME
Date : 9/4/1986
Time : 15:53:28

####################### P I N   L I S T #######################

   LABEL     ** FNC **PIN --------- PIN** FNC **    LABEL
/S           ** I   **  1-:       :-24 ** +5V **VCC
/R           ** I   **  2-:       :-23 ** /O  **Q
N/C          ** I   **  3-:  P    :-22 ** /O  **QNOT
N/C          ** I   **  4-:  L    :-21 ** /B  **N/C
N/C          ** I   **  5-:  H    :-20 ** B   **F
N/C          ** I   **  6-:  S    :-19 ** O   **N/C
N/C          ** I   **  7-:  4    :-18 ** O   **N/C
N/C          ** I   **  8-:  7    :-17 ** /B  **N/C
S0           ** I   **  9-:  3    :-16 ** B   **D
S1           ** I   ** 10-:       :-15 ** B   **C
DIR          ** I   ** 11-:       :-14 ** B   **B
GND          ** 0V  ** 12-:       :-13 ** B   **A
                          ---------
```

TB03170S

Figure 4. Pin List



```
File Name : 473PRIME
Date : 9/4/1986
Time : 15:54:14

@DEVICE TYPE
PLHS473
@DRAWING
@REVISION
@DATE
@SYMBOL
        File name = 473PRIME
@COMPANY
@NAME
@DESCRIPTION
@COMMON PRODUCT TERM
@I/O DIRECTION

  "The I/O DIRECTION definition is optional, and may be defaulted
   to the PIN LIST unless it is bidirectional and is controlled by
   a logic equation. "

  "******************** I/O DEFINITION FOR R/S LATCH ****************** "

    D8 = 1 ;    " Each output must be defined seperately by its own
                  logic equation. "
    D7 = 1 ;

  "*************** I/O DEFINITION FOR MUX/DEMUX CIRCUIT *************** "

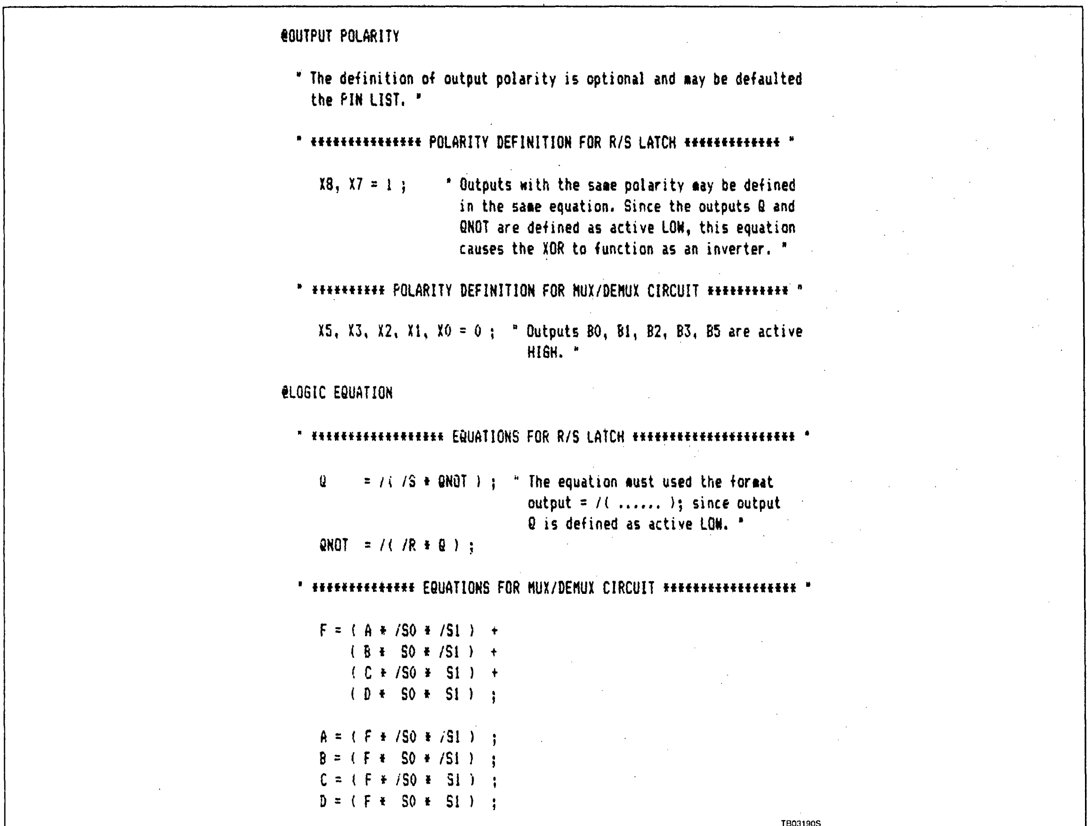
    D3 = DIR ;  " When DIR = 1, B3, B2, B1, B0 become outputs. Data flows
                  from F to A, B, C, D. "
    D2 = DIR ;
    D1 = DIR ;
    D0 = DIR ;

    D5 = /DIR ; " When DIR = 0, B5 becomes an output, output buffers
                  of B0 to B3 are disabled. Data flows from A, B, C,
                  D to F. "
```

TB03180S

Figure 5. Boolean Equations

9



```
@OUTPUT POLARITY

  " The definition of output polarity is optional and may be defaulted
    the PIN LIST. "

  " *************** POLARITY DEFINITION FOR R/S LATCH ************* "

     X8, X7 = 1 ;      " Outputs with the same polarity may be defined
                         in the same equation. Since the outputs Q and
                         QNOT are defined as active LOW, this equation
                         causes the XOR to function as an inverter. "

  " ********** POLARITY DEFINITION FOR MUX/DEMUX CIRCUIT *********** "

     X5, X3, X2, X1, X0 = 0 ;  " Outputs B0, B1, B2, B3, B5 are active
                                 HIGH. "

@LOGIC EQUATION

  " ****************** EQUATIONS FOR R/S LATCH ********************** "

     Q    = /( /S * QNOT ) ;  " The equation must used the format
                                output = /( ...... ); since output
                                Q is defined as active LOW. "
     QNOT = /( /R * Q ) ;

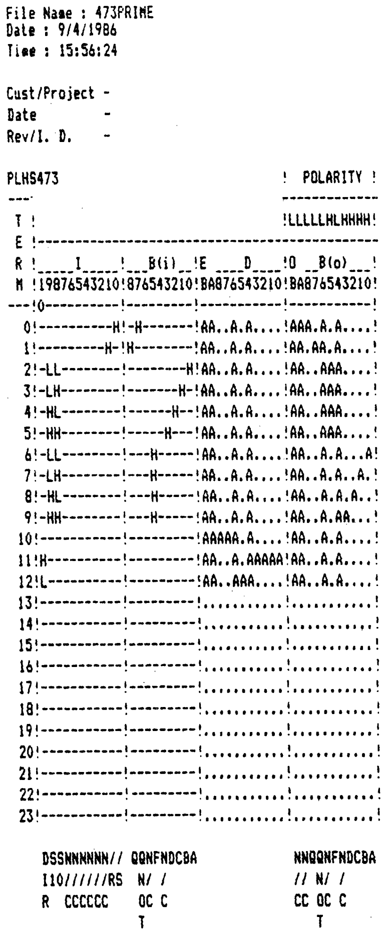
  " ************** EQUATIONS FOR MUX/DEMUX CIRCUIT ****************** "

     F = ( A * /S0 * /S1 )  +
         ( B *  S0 * /S1 )  +
         ( C * /S0 *  S1 )  +
         ( D *  S0 *  S1 )  ;

     A = ( F * /S0 * /S1 )  ;
     B = ( F *  S0 * /S1 )  ;
     C = ( F * /S0 *  S1 )  ;
     D = ( F *  S0 *  S1 )  ;
```

TB03190S

Figure 5. Boolean Equations (Continued)



```
File Name : 473PRIME
Date : 9/4/1986
Time : 15:56:24

Cust/Project -
Date         -
Rev/I. D.    -

PLHS473                              !  POLARITY !
---                                  -------------
 T !                                 !LLLLLHLHHHH!
 E !----------------------------------------------
 R !_____I_____!___B(i)__!E ____D____!O __B(o)___!
 M !19876543210!876543210!BA876543210!BA876543210!
---!0----------!---------!-----------!-----------!
  0!----------H!-H-------!AA..A.A....!AAA.A.A....!
  1!---------H-!H--------!AA..A.A....!AA.AA.A....!
  2!-LL--------!--------H!AA..A.A....!AA..AAA....!
  3!-LH--------!-------H-!AA..A.A....!AA..AAA....!
  4!-HL--------!------H--!AA..A.A....!AA..AAA....!
  5!-HH--------!-----H---!AA..A.A....!AA..AAA....!
  6!-LL--------!---H-----!AA..A.A....!AA..A.A...A!
  7!-LH--------!---H-----!AA..A.A....!AA..A.A..A.!
  8!-HL--------!---H-----!AA..A.A....!AA..A.A.A..!
  9!-HH--------!---H-----!AA..A.A....!AA..A.AA...!
 10!-----------!---------!AAAAA.A....!AA..A.A....!
 11!H----------!---------!AA..A.AAAAA!AA..A.A....!
 12!L----------!---------!AA..AAA....!AA..A.A....!
 13!-----------!---------!...........!...........!
 14!-----------!---------!...........!...........!
 15!-----------!---------!...........!...........!
 16!-----------!---------!...........!...........!
 17!-----------!---------!...........!...........!
 18!-----------!---------!...........!...........!
 19!-----------!---------!...........!...........!
 20!-----------!---------!...........!...........!
 21!-----------!---------!...........!...........!
 22!-----------!---------!...........!...........!
 23!-----------!---------!...........!...........!

    DSSNNNNNN// QQNFNDCBA             NNQQNFNDCBA
    I10//////RS  N/ /                 // N/ /
    R  CCCCCC    OC C                 CC OC C
                 T                       T
```

TB03160S

Figure 6. Program Table

Signetics

Application Specific Products

AN28
High-Speed 12-Bit Tracking A/D Converter Using PLS179

Application Note

INTRODUCTION

The general technique underlying the operation of this A/D converter is illustrated by the fuctional block diagram in Figure 1. The system consists of a D/A converter, a comparator circuit, and digital logic circuitry. The digital logic circuitry outputs a digital vaue which is converted to analog by the D/A converter.

The comparator senses when the output is greater or less than the input and causes the digital circuit to decrement or increment its digital output respectively. The initial conversion is completed in 13 clock cycles. If tracking mode is used, the A/D converter then tracks the input voltage as it changes by incrementing or decrementing 1-LSB per clock. The tracking function makes it possible to make an A/D conversion in one clock cycle if the input changes less than the value of 1-LSB per clock period. The conversion may be halted and the digital output, as well as the converted analog output from DAC, will hold their output constant indefinitely. This feature works well as sample-and-hold since its output voltage will not decay over time whereas the output of an analog sample/hold will decay due to charge leakages.

In order to avoid the violation of setup time by the output of the comparator, its output is latched. There is a built-in 2-phase clock in U2 which may be used to drive the logic circuitry and the latch of the comparator (see Signetics NE5105 data sheet for details on output latches of voltage comparators).

The analog input voltage may be sampled and held by an analog sample/hold circuit to keep the input to the ADC from changing. The DONE output may be used to control the sample-and-hold if needed.

This paper discusses only the digital circuit which contains the SAR and the Up/Down Counter. The analog circuits are not within the scope of this paper.

SAR

Two PLS179s are connected together to form a 12-bit shift register and up/down counter. The schematic diagram of the A/D converter is shown in Figure 2. U2 contains bits 0 to 4 and U1 contains Bits 5 to 11. Interconnects are made as shown in the diagram. The digital output to the DAC is in natural binary format (e.g. 0000 0000 0000 equal zero, and 1111 1111 1111 is full scale or 4095). After the/ST input becomes 0, at the rising edge of the next clock, the SAR is initialized to half-scale (1000 0000 0000) and the DONE flip-flop is reset to output 0 which causes the open-collector output /DONE_OC to become high impedance. The digital output is converted by the DAC and is compared to the analog input voltage by the comparator. If the digital output is greater than the analog input, the SAR shifts the 1 to next MSB on the right. The content of the SAR becomes (0100 0000 0000). If the digital output is still greater than the input, the SAR shifts right one bit again. The content of the SAR then becomes (0010 0000 0000). The shifting of 1 to the next MSB in equivalent to reducing by half the value of the bit under consideration. If the output is still too large, the SAR reduces it by half again by shifting to the right one more time. The SAR keeps shifting to the right until the digital output is less than the input. When the output is less than the input, the SAR adds one bit to the next MSB while keeping all the higher order bits unchanged. For example, if the current output is 0001 0000 0000 and the output is less than the input, the SAR adds one bit to the right at the next clock. The output becomes 0001 1000 0000. The output is again compared to the input. If the addition of that one bit is too much, it will be shifted to the right until the output becomes less than the input. When that happens, that SAR will again add one bit to the right. The algorithm of the SAR may be summarized as the following: If the output is greater than the input, shift to the right; otherwise add one bit to the right. This process continues until all 12 bits have been operated on. The last bit (Bit 0) is always changed from 0 to 1, which is used as the condition to set DONE to 1 which, in turn, sets open-collector output, /DONE_OC, to 0.

UP/DOWN COUNTER

After DONE becomes 1, if /ST and /HOLD are 1 and /TRACK is 0, the SAR turns into a 12-bit up/down counter. If the analog input voltage increases, the counter will increment by 1 at every clock until it matches the input. If the input decreases, the counter will decrement by 1. When /HOLD becomes 0, the counter is inhibited and the output is held indefinitely. The counters consist of 12 toggle flip-flops and 2 p-terms per flip-flop for directional control. The counter will operate only

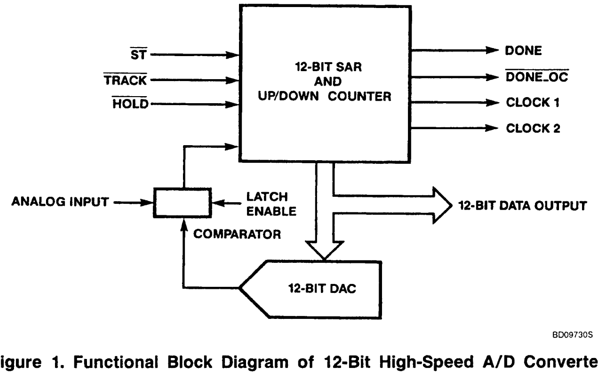


Figure 1. Functional Block Diagram of 12-Bit High-Speed A/D Converter

High-Speed 12-Bit Tracking A/D Converter Using PLS179

AN28

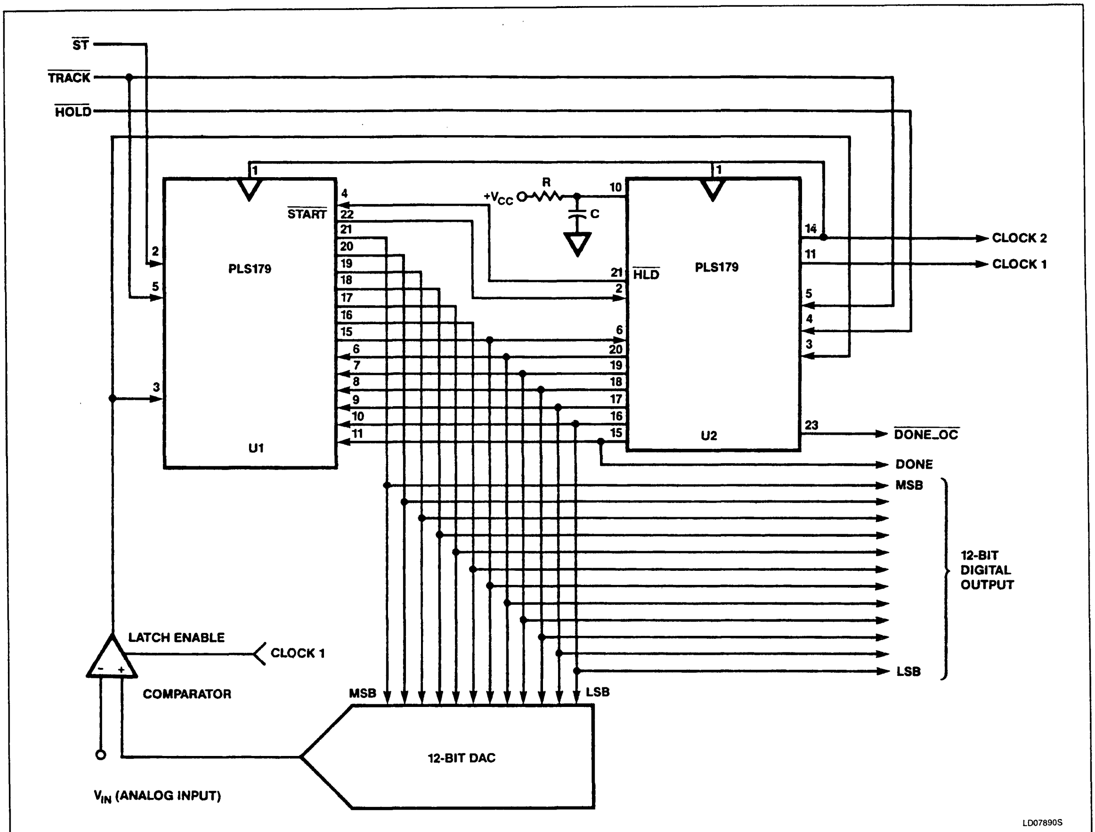


Figure 2. Schematic Diagram of 12-Bit High-Speed A/D Converter

after the approximation cycle is completed and DONE is 1.

Since the /ST and /HOLD inputs may be asynchronous with the clock, in order to minimize the possibilities of having a metastable condition from happening, these inputs close-up are latched by flip-flops /START of U1 and /HLD of U2 respectively. Once they are latched, subsequent operation begins at the rising-edge of the next clock. The output of the comparator may be latched to prevent setup time violation. (Signetics NE5105 is a high-speed comparator with an output latch. External latch may be used with other comparators.)

CLOCKS

U2 generates an optional 2-phase clock which may be used to control the latch of the comparator. The two clocks are basically 180° out of phase and CLOCK2 has an additional 25ns propagation delay behind CLOCK1. CLOCK2 is used to drive the clock-inputs of the PLS179 devices.

The clock frequency is controlled by R and C. Those who want to use the built-in clock should experiment with RC time constants for the best value. It is recommended that the capacitance should be less than 1000pF for best results (see Ap Note AN13 for more detail).

DONE AND /DONE_OC

The output DONE is reset to 0 when /ST is 0. It remains 0 until the approximation cycle is completed. After the least significant bit becomes 1, the DONE bit becomes 1 at the next clock. It remains 1 until it is reset again by input /ST.

The /DONE_OC output is configured to emulate an open-collector output. The output is programmed to have a logic 0. When DONE is 0, the Tri-state output buffer is set to Hi-Z condition. As soon as DONE equals 1, the Tri-state buffer is enabled and /DONE_OC becomes 0.

In the initial phase of A/D conversion, 13 clock cycles are required. It is essential that the input voltage to the comparator remains unchanged while the SAR is converting. It may be necessary to have a sample/hold at the front end. The DONE output may be used to control the analog sample/hold circuit.

INPUT LATCHES

Flip-flop /START and 2 p-terms in U1 are configured as a non-inverting D flip-flop. The input, /ST, and the output /START have the same polarities. Flip-flop /HLD and 2 p-terms in U2 also form a non-inverting D flip-flop. The output /HLD and the input /HOLD have the same polarities.

AMAZE INPLEMENTATION

The implementation of the logic circuit using AMAZE is as shown in the appendices. The SAR circuit is first designed as a state machine (file name: ADCS.SEE). It is then partitioned into two PLS179s after proper pin assignments are made. Then the up/down counter, input latches, 2-phase clocks and the open-collector output, are implemented by using Boolean equations in their respective .BEE files (file names: ADCB1.BEE and ADCB2.BEE) in AMAZE. The files are then assembled to produce the fuse-maps of PLS179 (ADCB1.STD and ADCB2.STD).

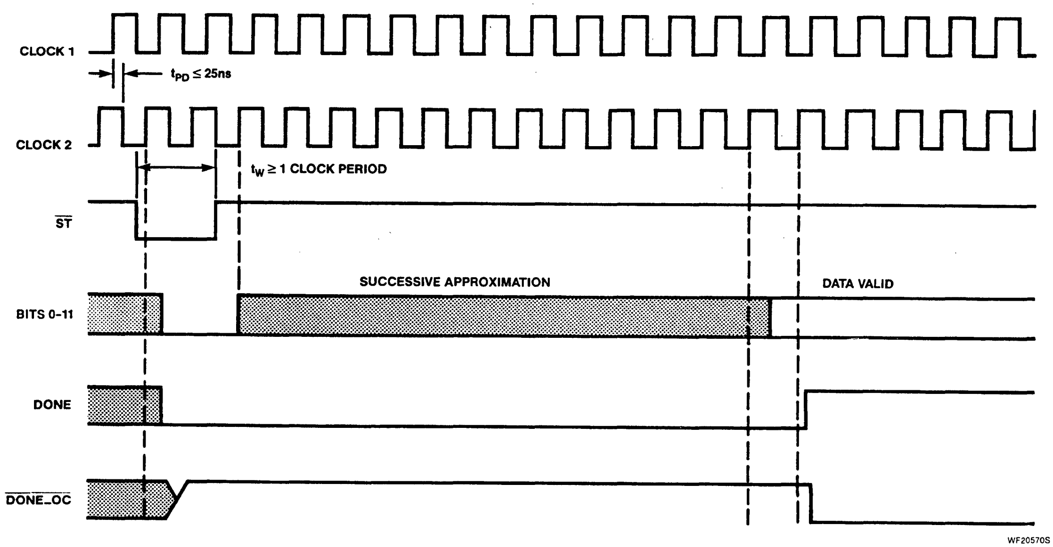
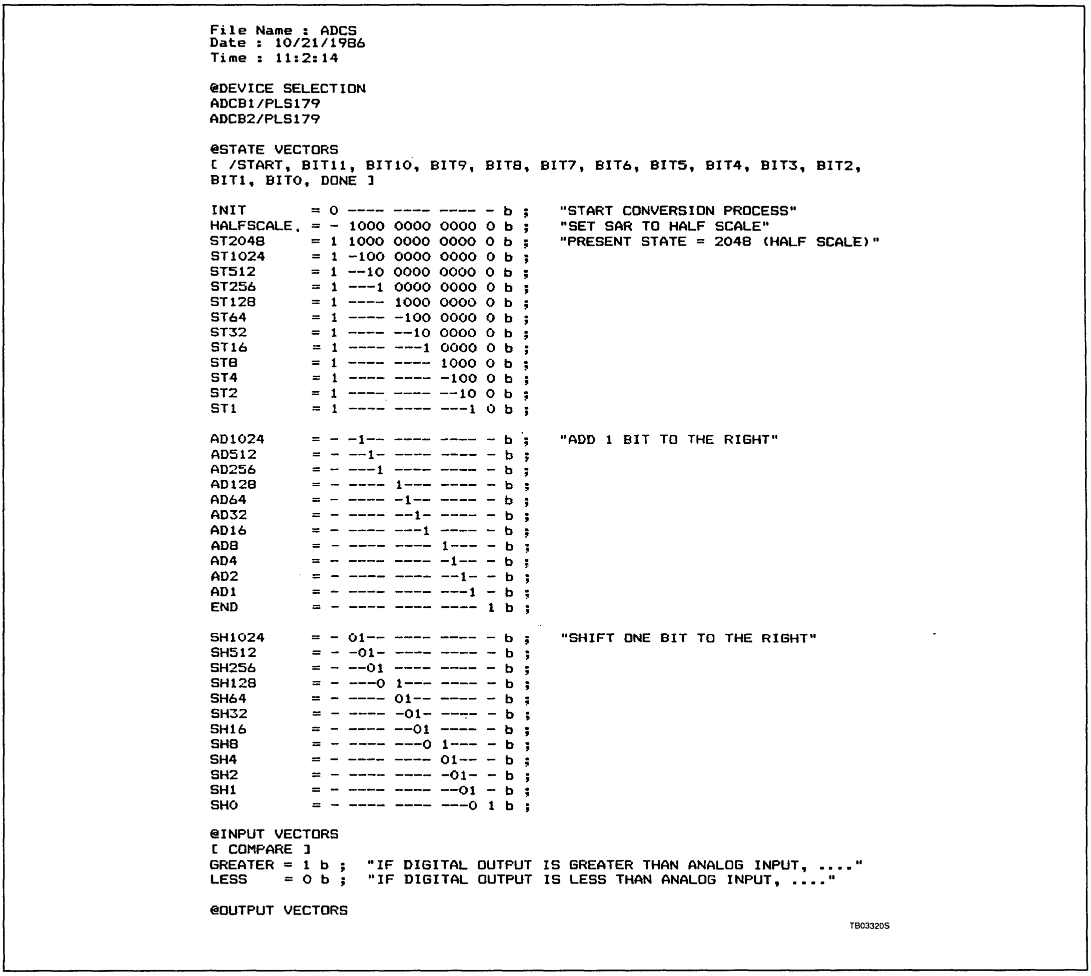


Figure 3. Timing Diagram of Successive Approximation Cycle

APPENDIX A: STATE EQUATIONS OF SAR



```
File Name : ADCS
Date : 10/21/1986
Time : 11:2:14

@DEVICE SELECTION
ADCB1/PLS179
ADCB2/PLS179

@STATE VECTORS
[ /START, BIT11, BIT10, BIT9, BIT8, BIT7, BIT6, BIT5, BIT4, BIT3, BIT2,
BIT1, BIT0, DONE ]

INIT        = 0 ---- ---- ---- - b ;   "START CONVERSION PROCESS"
HALFSCALE.  = - 1000 0000 0000 0 b ;   "SET SAR TO HALF SCALE"
ST2048      = 1 1000 0000 0000 0 b ;   "PRESENT STATE = 2048 (HALF SCALE)"
ST1024      = 1 -100 0000 0000 0 b ;
ST512       = 1 --10 0000 0000 0 b ;
ST256       = 1 ---1 0000 0000 0 b ;
ST128       = 1 ---- 1000 0000 0 b ;
ST64        = 1 ---- -100 0000 0 b ;
ST32        = 1 ---- --10 0000 0 b ;
ST16        = 1 ---- ---1 0000 0 b ;
ST8         = 1 ---- ---- 1000 0 b ;
ST4         = 1 ---- ---- -100 0 b ;
ST2         = 1 ---- ---- --10 0 b ;
ST1         = 1 ---- ---- ---1 0 b ;

AD1024      = - -1-- ---- ---- - b ;   "ADD 1 BIT TO THE RIGHT"
AD512       = - --1- ---- ---- - b ;
AD256       = - ---1 ---- ---- - b ;
AD128       = - ---- 1--- ---- - b ;
AD64        = - ---- -1-- ---- - b ;
AD32        = - ---- --1- ---- - b ;
AD16        = - ---- ---1 ---- - b ;
AD8         = - ---- ---- 1--- - b ;
AD4         = - ---- ---- -1-- - b ;
AD2         = - ---- ---- --1- - b ;
AD1         = - ---- ---- ---1 - b ;
END         = - ---- ---- ---- 1 b ;

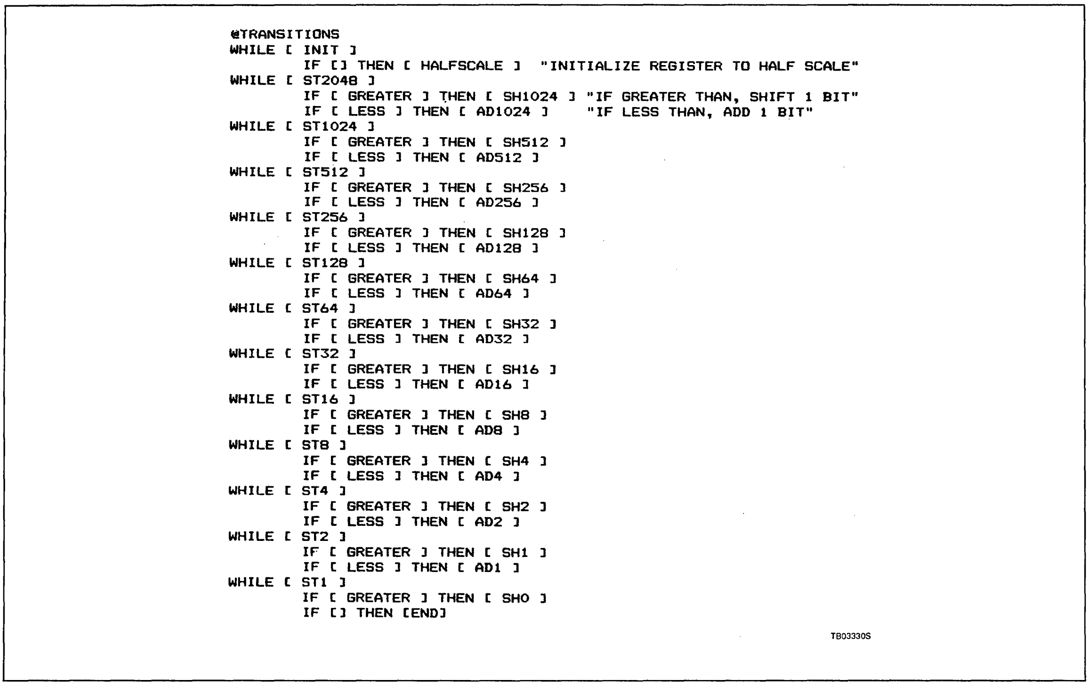
SH1024      = - 01-- ---- ---- - b ;   "SHIFT ONE BIT TO THE RIGHT"
SH512       = - -01- ---- ---- - b ;
SH256       = - --01 ---- ---- - b ;
SH128       = - ---0 1--- ---- - b ;
SH64        = - ---- 01-- ---- - b ;
SH32        = - ---- -01- ---- - b ;
SH16        = - ---- --01 ---- - b ;
SH8         = - ---- ---0 1--- - b ;
SH4         = - ---- ---- 01-- - b ;
SH2         = - ---- ---- -01- - b ;
SH1         = - ---- ---- --01 - b ;
SH0         = - ---- ---- ---0 1 b ;

@INPUT VECTORS
[ COMPARE ]
GREATER = 1 b ;  "IF DIGITAL OUTPUT IS GREATER THAN ANALOG INPUT, ...."
LESS    = 0 b ;  "IF DIGITAL OUTPUT IS LESS THAN ANALOG INPUT, ...."

@OUTPUT VECTORS
```

TB03320S

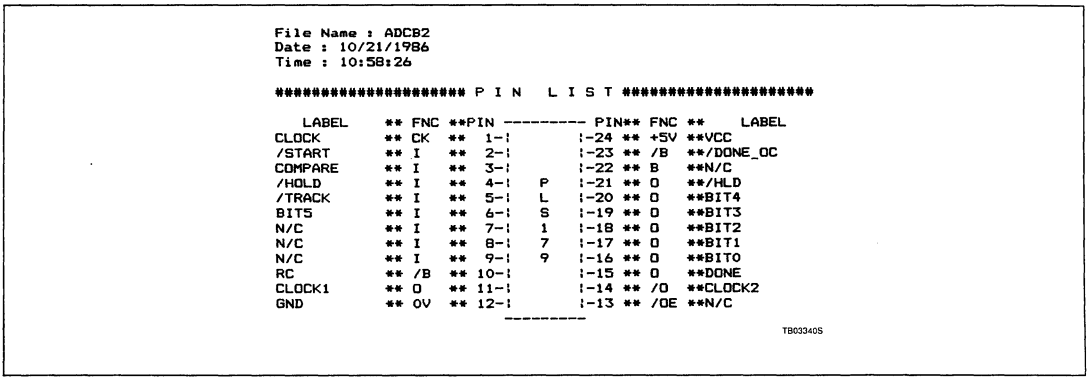
APPENDIX A: STATE EQUATIONS OF SAR (Continued)



```
@TRANSITIONS
WHILE [ INIT ]
        IF [] THEN [ HALFSCALE ]  "INITIALIZE REGISTER TO HALF SCALE"
WHILE [ ST2048 ]
        IF [ GREATER ] THEN [ SH1024 ] "IF GREATER THAN, SHIFT 1 BIT"
        IF [ LESS ] THEN [ AD1024 ]    "IF LESS THAN, ADD 1 BIT"
WHILE [ ST1024 ]
        IF [ GREATER ] THEN [ SH512 ]
        IF [ LESS ] THEN [ AD512 ]
WHILE [ ST512 ]
        IF [ GREATER ] THEN [ SH256 ]
        IF [ LESS ] THEN [ AD256 ]
WHILE [ ST256 ]
        IF [ GREATER ] THEN [ SH128 ]
        IF [ LESS ] THEN [ AD128 ]
WHILE [ ST128 ]
        IF [ GREATER ] THEN [ SH64 ]
        IF [ LESS ] THEN [ AD64 ]
WHILE [ ST64 ]
        IF [ GREATER ] THEN [ SH32 ]
        IF [ LESS ] THEN [ AD32 ]
WHILE [ ST32 ]
        IF [ GREATER ] THEN [ SH16 ]
        IF [ LESS ] THEN [ AD16 ]
WHILE [ ST16 ]
        IF [ GREATER ] THEN [ SH8 ]
        IF [ LESS ] THEN [ AD8 ]
WHILE [ ST8 ]
        IF [ GREATER ] THEN [ SH4 ]
        IF [ LESS ] THEN [ AD4 ]
WHILE [ ST4 ]
        IF [ GREATER ] THEN [ SH2 ]
        IF [ LESS ] THEN [ AD2 ]
WHILE [ ST2 ]
        IF [ GREATER ] THEN [ SH1 ]
        IF [ LESS ] THEN [ AD1 ]
WHILE [ ST1 ]
        IF [ GREATER ] THEN [ SHO ]
        IF [] THEN [END]
```

TB03330S

APPENDIX B: PIN LISTS

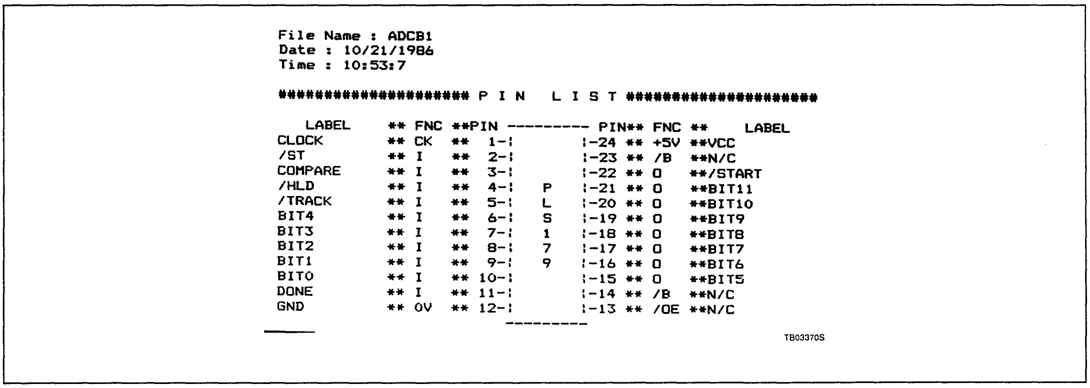


```
File Name : ADCB2
Date : 10/21/1986
Time : 10:58:26

###################### P I N   L I S T ######################

   LABEL     ** FNC **PIN --------- PIN** FNC **     LABEL
CLOCK        ** CK  **   1-!       !-24 ** +5V **VCC
/START       ** I   **   2-!       !-23 ** /B  **/DONE_OC
COMPARE      ** I   **   3-!       !-22 ** B   **N/C
/HOLD        ** I   **   4-!   P   !-21 ** O   **/HLD
/TRACK       ** I   **   5-!   L   !-20 ** O   **BIT4
BIT5         ** I   **   6-!   S   !-19 ** O   **BIT3
N/C          ** I   **   7-!   1   !-18 ** O   **BIT2
N/C          ** I   **   8-!   7   !-17 ** O   **BIT1
N/C          ** I   **   9-!   9   !-16 ** O   **BIT0
RC           ** /B  **  10-!       !-15 ** O   **DONE
CLOCK1       ** O   **  11-!       !-14 ** /O  **CLOCK2
GND          ** OV  **  12-!       !-13 ** /OE **N/C
                           ---------
```

TB03340S



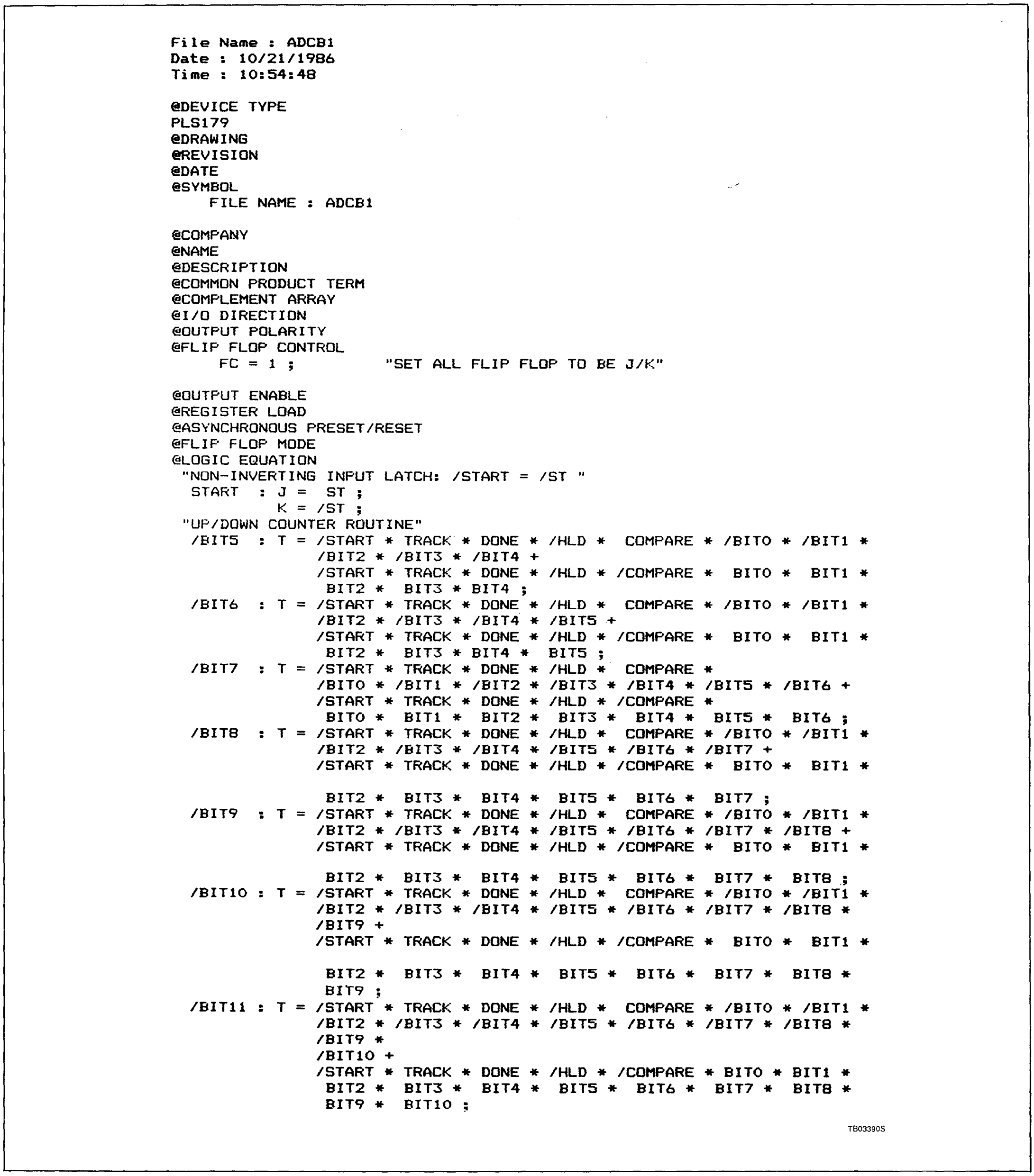
```
File Name : ADCB1
Date : 10/21/1986
Time : 10:53:7

###################### P I N   L I S T ######################

   LABEL     ** FNC **PIN --------- PIN** FNC **     LABEL
CLOCK        ** CK  **   1-!       !-24 ** +5V **VCC
/ST          ** I   **   2-!       !-23 ** /B  **N/C
COMPARE      ** I   **   3-!       !-22 ** O   **/START
/HLD         ** I   **   4-!   P   !-21 ** O   **BIT11
/TRACK       ** I   **   5-!   L   !-20 ** O   **BIT10
BIT4         ** I   **   6-!   S   !-19 ** O   **BIT9
BIT3         ** I   **   7-!   1   !-18 ** O   **BIT8
BIT2         ** I   **   8-!   7   !-17 ** O   **BIT7
BIT1         ** I   **   9-!   9   !-16 ** O   **BIT6
BIT0         ** I   **  10-!       !-15 ** O   **BIT5
DONE         ** I   **  11-!       !-14 ** /B  **N/C
GND          ** OV  **  12-!       !-13 ** /OE **N/C
                           ---------
```

TB03370S

APPENDIX C: BOOLEAN EQUATIONS OF UP/DOWN COUNTER AND INPUT LATCH



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File Name : ADCB1
Date : 10/21/1986
Time : 10:54:48

@DEVICE TYPE
PLS179
@DRAWING
@REVISION
@DATE
@SYMBOL
    FILE NAME : ADCB1

@COMPANY
@NAME
@DESCRIPTION
@COMMON PRODUCT TERM
@COMPLEMENT ARRAY
@I/O DIRECTION
@OUTPUT POLARITY
@FLIP FLOP CONTROL
     FC = 1 ;         "SET ALL FLIP FLOP TO BE J/K"

@OUTPUT ENABLE
@REGISTER LOAD
@ASYNCHRONOUS PRESET/RESET
@FLIP FLOP MODE
@LOGIC EQUATION
 "NON-INVERTING INPUT LATCH: /START = /ST "
  START  : J =  ST ;
           K = /ST ;
 "UP/DOWN COUNTER ROUTINE"
  /BIT5  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
                BIT2 *  BIT3 * BIT4 ;
  /BIT6  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
                BIT2 *  BIT3 * BIT4 *  BIT5 ;
  /BIT7  : T = /START * TRACK * DONE * /HLD *  COMPARE *
               /BIT0 * /BIT1 * /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 +
               /START * TRACK * DONE * /HLD * /COMPARE *
                BIT0 *  BIT1 *  BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 ;
  /BIT8  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *

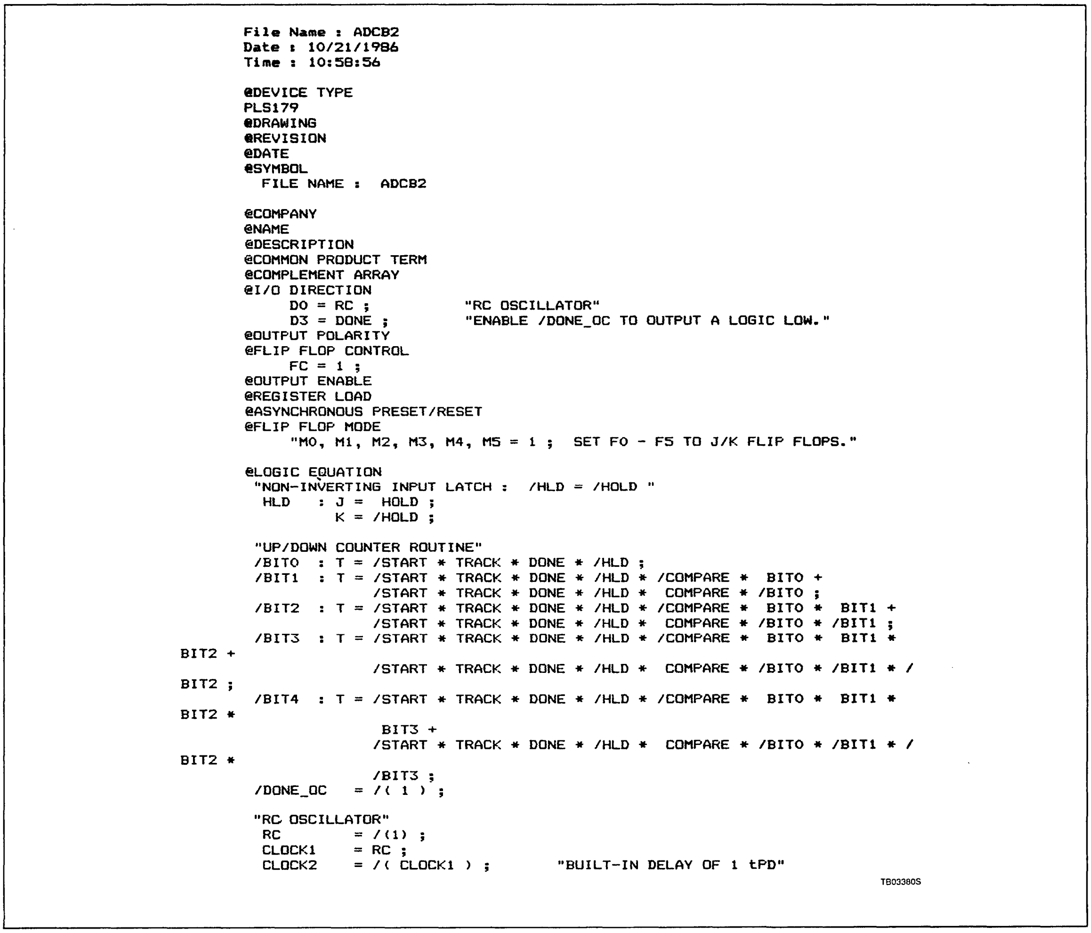
                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 ;
  /BIT9  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 * /BIT8 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *

                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 *  BIT8 ;
  /BIT10 : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 * /BIT8 *
               /BIT9 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *

                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 *  BIT8 *
                BIT9 ;
  /BIT11 : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 * /BIT8 *
               /BIT9 *
               /BIT10 +
               /START * TRACK * DONE * /HLD * /COMPARE * BIT0 * BIT1 *
                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 *  BIT8 *
                BIT9 *  BIT10 ;
```

TB03390S

APPENDIX C: BOOLEAN EQUATIONS OF UP/DOWN COUNTER AND INPUT LATCH (Continued)



```
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       Date : 10/21/1986
       Time : 10:58:56

       @DEVICE TYPE
       PLS179
       @DRAWING
       @REVISION
       @DATE
       @SYMBOL
         FILE NAME :  ADCB2

       @COMPANY
       @NAME
       @DESCRIPTION
       @COMMON PRODUCT TERM
       @COMPLEMENT ARRAY
       @I/O DIRECTION
            D0 = RC ;           "RC OSCILLATOR"
            D3 = DONE ;         "ENABLE /DONE_OC TO OUTPUT A LOGIC LOW."
       @OUTPUT POLARITY
       @FLIP FLOP CONTROL
            FC = 1 ;
       @OUTPUT ENABLE
       @REGISTER LOAD
       @ASYNCHRONOUS PRESET/RESET
       @FLIP FLOP MODE
            "M0, M1, M2, M3, M4, M5 = 1 ;  SET F0 - F5 TO J/K FLIP FLOPS."

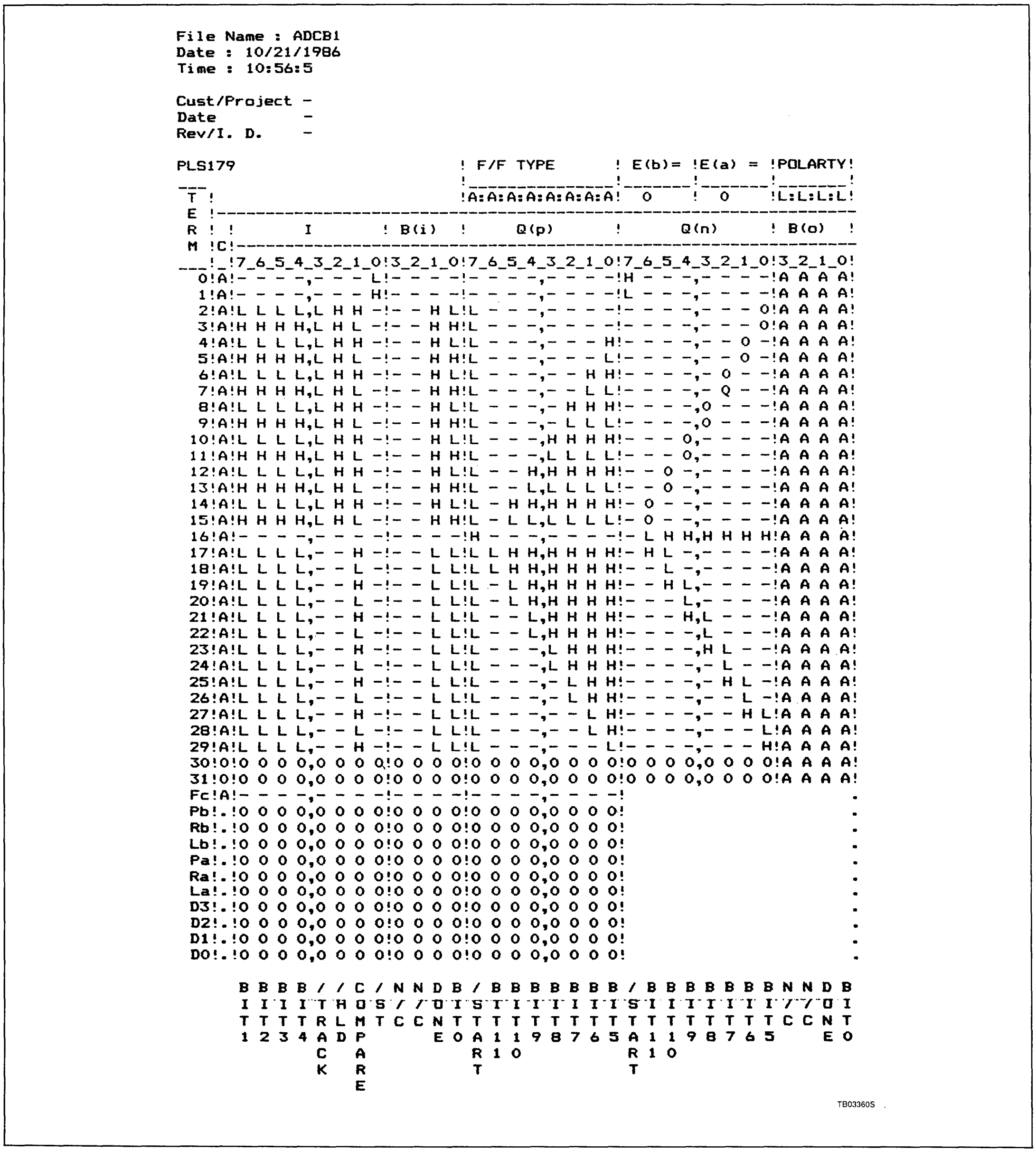
       @LOGIC EQUATION
        "NON-INVERTING INPUT LATCH :  /HLD = /HOLD "
         HLD   : J =  HOLD ;
                   K = /HOLD ;

        "UP/DOWN COUNTER ROUTINE"
        /BIT0  : T = /START * TRACK * DONE * /HLD ;
        /BIT1  : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 +
                     /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 ;
        /BIT2  : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 +
                     /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 ;
        /BIT3  : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
BIT2 +
                     /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 * /
BIT2 ;
        /BIT4  : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
BIT2 *
                      BIT3 +
                     /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 * /
BIT2 *
                     /BIT3 ;
        /DONE_OC    = /( 1 ) ;

        "RC OSCILLATOR"
         RC         = /(1) ;
         CLOCK1     = RC ;
         CLOCK2     = /( CLOCK1 ) ;       "BUILT-IN DELAY OF 1 tPD"
```

TB03380S

APPENDIX D: U1 ADCB1 FUSE MAP



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File Name : ADCB1
Date : 10/21/1986
Time : 10:56:5

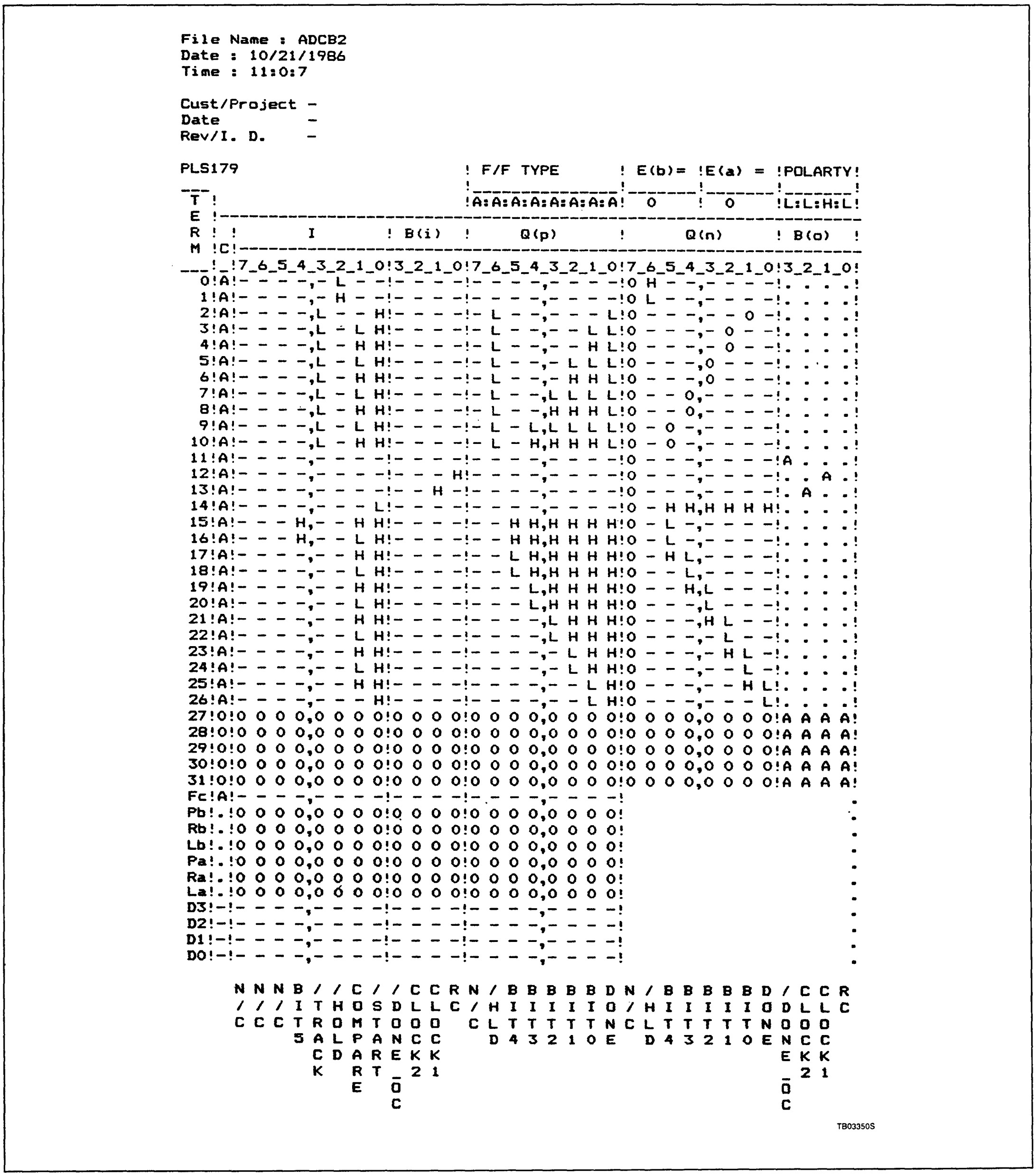
Cust/Project -
Date         -
Rev/I. D.    -

PLS179                       ! F/F TYPE       ! E(b)= !E(a) = !POLARTY!
                             !_______________!_______!_______!_______!
___
 T !                         !A:A:A:A:A:A:A:A!   0   !   0   !L:L:L:L!
 E !------------------------------------------------------------------
 R ! !      I        ! B(i) !     Q(p)      !      Q(n)     ! B(o)  !
 M !C!----------------------------------------------------------------
___!_!7_6_5_4_3_2_1_0!3_2_1_0!7_6_5_4_3_2_1_0!7_6_5_4_3_2_1_0!3_2_1_0!
  0!A!- - - -,- - - L!- - - -!- - - -,- - - -!H - - -,- - - -!A A A A!
  1!A!- - - -,- - - H!- - - -!- - - -,- - - -!L - - -,- - - -!A A A A!
  2!A!L L L L,L H H -!- - H L!L - - -,- - - -!- - - -,- - - 0!A A A A!
  3!A!H H H H,L H L -!- - H H!L - - -,- - - -!- - - -,- - - 0!A A A A!
  4!A!L L L L,L H H -!- - H L!L - - -,- - - H!- - - -,- - 0 -!A A A A!
  5!A!H H H H,L H L -!- - H H!L - - -,- - - L!- - - -,- - 0 -!A A A A!
  6!A!L L L L,L H H -!- - H L!L - - -,- - H H!- - - -,- 0 - -!A A A A!
  7!A!H H H H,L H L -!- - H H!L - - -,- - L L!- - - -,- Q - -!A A A A!
  8!A!L L L L,L H H -!- - H L!L - - -,- H H H!- - - -,0 - - -!A A A A!
  9!A!H H H H,L H L -!- - H H!L - - -,- L L L!- - - -,0 - - -!A A A A!
 10!A!L L L L,L H H -!- - H L!L - - -,H H H H!- - - 0,- - - -!A A A A!
 11!A!H H H H,L H L -!- - H H!L - - -,L L L L!- - - 0,- - - -!A A A A!
 12!A!L L L L,L H H -!- - H L!L - - H,H H H H!- - 0 -,- - - -!A A A A!
 13!A!H H H H,L H L -!- - H H!L - - L,L L L L!- - 0 -,- - - -!A A A A!
 14!A!L L L L,L H H -!- - H L!L - H H,H H H H!- 0 - -,- - - -!A A A A!
 15!A!H H H H,L H L -!- - H H!L - L L,L L L L!- 0 - -,- - - -!A A A A!
 16!A!- - - -,- - - -!- - - -!H - - -,- - - -!- L H H,H H H H!A A A A!
 17!A!L L L L,- - H -!- - L L!L L H H,H H H H!- H L -,- - - -!A A A A!
 18!A!L L L L,- - L -!- - L L!L L H H,H H H H!- - L -,- - - -!A A A A!
 19!A!L L L L,- - H -!- - L L!L - L H,H H H H!- - H L,- - - -!A A A A!
 20!A!L L L L,- - L -!- - L L!L - L H,H H H H!- - - L,- - - -!A A A A!
 21!A!L L L L,- - H -!- - L L!L - - L,H H H H!- - - H,L - - -!A A A A!
 22!A!L L L L,- - L -!- - L L!L - - L,H H H H!- - - -,L - - -!A A A A!
 23!A!L L L L,- - H -!- - L L!L - - -,L H H H!- - - -,H L - -!A A A A!
 24!A!L L L L,- - L -!- - L L!L - - -,L H H H!- - - -,- L - -!A A A A!
 25!A!L L L L,- - H -!- - L L!L - - -,- L H H!- - - -,- H L -!A A A A!
 26!A!L L L L,- - L -!- - L L!L - - -,- L H H!- - - -,- - L -!A A A A!
 27!A!L L L L,- - H -!- - L L!L - - -,- - L H!- - - -,- - H L!A A A A!
 28!A!L L L L,- - L -!- - L L!L - - -,- - L H!- - - -,- - - L!A A A A!
 29!A!L L L L,- - H -!- - L L!L - - -,- - - L!- - - -,- - - H!A A A A!
 30!0!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A A A A!
 31!0!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A A A A!
 Fc!A!- - - -,- - - -!- - - -!- - - -,- - - -!                       .
 Pb!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Rb!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Lb!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Pa!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Ra!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 La!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 D3!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 D2!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 D1!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 D0!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .

      B B B B / / C / N N D B / B B B B B B B / B B B B B B B N N D B
      I I I I T H O S / / O I S I I I I I I I S I I I I I I I / / O I
      T T T T R L M T C C N T T T T T T T T T T T T T T T T T C C N T
      1 2 3 4 A D P       E 0 A 1 1 9 8 7 6 5 A 1 1 9 8 7 6 5       E 0
              C   A           R 1 0           R 1 0
              K   R           T               T
                  E
```

TB03360S

APPENDIX D: U2 ADCB2 FUSE MAP (Continued)



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File Name : ADCB2
Date : 10/21/1986
Time : 11:0:7

Cust/Project -
Date         -
Rev/I. D.    -

PLS179                             ! F/F TYPE       ! E(b)= !E(a) = !POLARTY!
___                                !________________!_______!_______!_______!
 T !                               !A:A:A:A:A:A:A:A!   0    !   0    !L:L:H:L!
 E !------------------------------------------------------------------------
 R ! !          I          ! B(i)  !      Q(p)       !       Q(n)     ! B(o)  !
 M !C!------------------------------------------------------------------------
___!_!7_6_5_4_3_2_1_0!3_2_1_0!7_6_5_4_3_2_1_0!7_6_5_4_3_2_1_0!3_2_1_0!
  0!A!- - - -,- L - -!- - - -!- - - -,- - - -!0 H - -,- - - -!. . . .!
  1!A!- - - -,- H - -!- - - -!- - - -,- - - -!0 L - -,- - - -!. . . .!
  2!A!- - - -,L - - H!- - - -!- L - -,- - - L!0 - - -,- - 0 -!. . . .!
  3!A!- - - -,L - L H!- - - -!- L - -,- - L L!0 - - -,- 0 - -!. . . .!
  4!A!- - - -,L - H H!- - - -!- L - -,- - H L!0 - - -,- 0 - -!. . . .!
  5!A!- - - -,L - L H!- - - -!- L - -,- L L L!0 - - -,0 - - -!. . . .!
  6!A!- - - -,L - H H!- - - -!- L - -,- H H L!0 - - -,0 - - -!. . . .!
  7!A!- - - -,L - L H!- - - -!- L - -,L L L L!0 - - 0,- - - -!. . . .!
  8!A!- - - -,L - H H!- - - -!- L - -,H H H L!0 - - 0,- - - -!. . . .!
  9!A!- - - -,L - L H!- - - -!- L - L,L L L L!0 - 0 -,- - - -!. . . .!
 10!A!- - - -,L - H H!- - - -!- L - H,H H H L!0 - 0 -,- - - -!. . . .!
 11!A!- - - -,- - - -!- - - -!- - - -,- - - -!0 - - -,- - - -!A . . .!
 12!A!- - - -,- - - -!- - - H!- - - -,- - - -!0 - - -,- - - -!. . A .!
 13!A!- - - -,- - - -!- - H -!- - - -,- - - -!0 - - -,- - - -!. A . .!
 14!A!- - - -,- - - L!- - - -!- - - -,- - - -!0 - H H,H H H H!. . . .!
 15!A!- - - H,- - H H!- - - -!- - H H,H H H H!0 - L -,- - - -!. . . .!
 16!A!- - - H,- - L H!- - - -!- - H H,H H H H!0 - L -,- - - -!. . . .!
 17!A!- - - -,- - H H!- - - -!- - L H,H H H H!0 - H L,- - - -!. . . .!
 18!A!- - - -,- - L H!- - - -!- - L H,H H H H!0 - - L,- - - -!. . . .!
 19!A!- - - -,- - H H!- - - -!- - - L,H H H H!0 - - H,L - - -!. . . .!
 20!A!- - - -,- - L H!- - - -!- - - L,H H H H!0 - - -,L - - -!. . . .!
 21!A!- - - -,- - H H!- - - -!- - - -,L H H H!0 - - -,H L - -!. . . .!
 22!A!- - - -,- - L H!- - - -!- - - -,L H H H!0 - - -,- L - -!. . . .!
 23!A!- - - -,- - H H!- - - -!- - - -,- L H H!0 - - -,- H L -!. . . .!
 24!A!- - - -,- - L H!- - - -!- - - -,- L H H!0 - - -,- - L -!. . . .!
 25!A!- - - -,- - H H!- - - -!- - - -,- - L H!0 - - -,- - H L!. . . .!
 26!A!- - - -,- - - H!- - - -!- - - -,- - L H!0 - - -,- - - L!. . . .!
 27!0!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A A A A!
 28!0!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A A A A!
 29!0!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A A A A!
 30!0!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A A A A!
 31!0!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!0 0 0 0,0 0 0 0!A A A A!
 Fc!A!- - - -,- - - -!- - - -!- - - -,- - - -!                       .
 Pb!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Rb!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Lb!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Pa!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 Ra!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 La!.!0 0 0 0,0 0 0 0!0 0 0 0!0 0 0 0,0 0 0 0!                       .
 D3!-!- - - -,- - - -!- - - -!- - - -,- - - -!                       .
 D2!-!- - - -,- - - -!- - - -!- - - -,- - - -!                       .
 D1!-!- - - -,- - - -!- - - -!- - - -,- - - -!                       .
 D0!-!- - - -,- - - -!- - - -!- - - -,- - - -!                       .

     N N N B / / C / / C C R N / B B B B B D N / B B B B B D / C C R
     / / / I T H O S D L L C / H I I I I I O / H I I I I I O D L L C
     C C C T R O M T O O O   C L T T T T T N C L T T T T T N O O O
           5 A L P A N C C     D 4 3 2 1 0 E   D 4 3 2 1 0 E N C C
             C D A R E K K                                   E K K
             K   R T _ 2 1                                   _ 2 1
                 E   Ō                                       Ō
                     C                                       C
```

TB03350S

Signetics

AN29
PLHS501 Programmable Macro Logic Primer

Application Note

Application Specific Products

SUMMARY

The evolution of Programmable Logic Devices (PLD's) has led to the birth of a new generation of programmable devices designated as PML (Programmable Macro Logic). The immense versatility of these devices brings them closer as plausible alternatives to semicustom design approaches in low-to-medium ranges of applications. The following paper begins with a background on PML and a brief description of the PML basic architecture (See Reference 1.) Next, the first PML devices are introduced with a detailed discussion of the PLHS501. The implementation of PML in the AMAZE software package is presented. A system level example intends to demonstrate the capabilities of PML as an eloquent and efficient design alternative.

THE EMERGENCE OF THE THIRD GENERATION PLD ARCHITECTURE

PML was introduced at WESCON '85 by Signetics Corporation. The unique architecture of PML breaks away into a new era of programmable logic devices. The purpose of the PML architecture is to overcome the two level AND-OR bottleneck and provide the user with a higher level of logic integration. Current PLD's rely on two levels of logic transformation to implement combinational logic in Sum-Of-Products (SOP) form. In addition various PLD's make use of higher level macros such as flip-flops to form sequential logic functions. These macros connect the AND-OR chain to dedicated I/O pins.

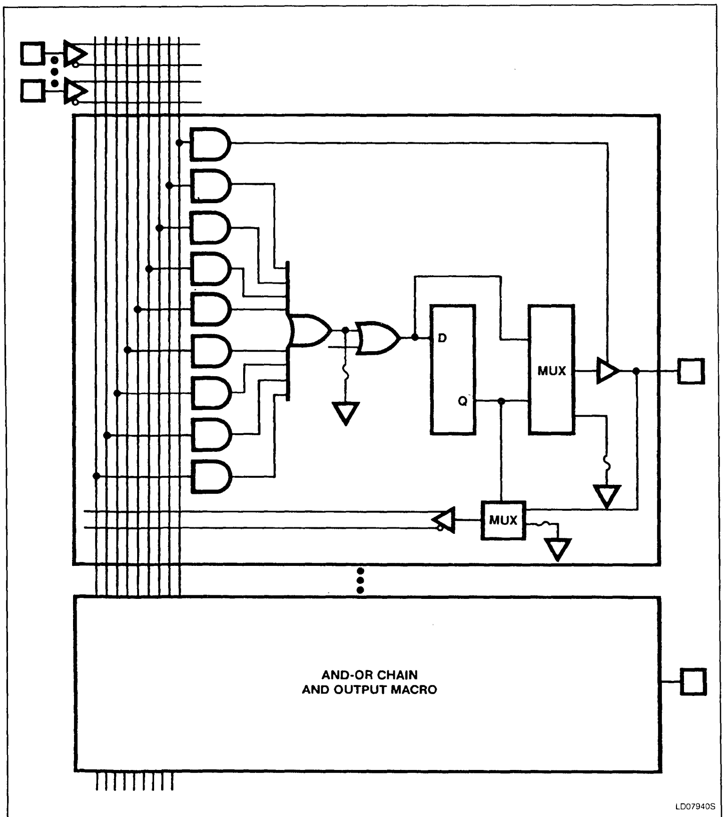


Figure 1. One of the Latest Registered PALs^{TM}

Figure 1 show the basic architecture of one of the most recent PAL^{TM} devices. It is clear that this architecture is inefficient in making full use of the available on-chip resources. This is due to the fact that an unused I/O macro will be wasted and remains futile.

For example, if an I/O pin is used as an input, the output macros are all wasted. Obviously, such an architecture cannot provide the user with an increase in the levels of logic integration. The PML device takes advantage of the fundamental architecture shown in Figure 2 to overcome these deficiencies and waste of on-chip resources. As shown in Figure 2, PML incorporates the NAND-NAND gate equivalence to break the AND-OR bottleneck.

The core of the PML is the programmable NAND-NAND network which connects the input and output macros to each other. Thus the inputs, outputs, and function macros are all connected by a single array.

At the present, two devices are under development which employ the above architecture. Both devices are fabricated by the Signetics state-of-the-art oxide isolation process and are packaged in 52-pin PLCC.

The first device available will be the PLHS501. The seemingly simple structure of this device can implement every logic function furnished by the current PAL^{TM}/PLA devices. Although the PLHS501 is principally a combinational logic device, its unique architecture makes it an ideal tool for applications involving asynchronous state machines (See Reference 2.)

The PLHS502 is a sequential logic device. It supplements the PLHS501 features with sixteen edge-triggered flip-flops. The device çan provide diverse applications encompassing synchronous and asynchronous state machine designs.

PAL^{TM} is a Trademark of Monolithic Memories, Inc.

Table 1. Functional Description of PLHS501 I/O Pins

PIN NO.	IDENTIFIER	FUNCTION
41-45, 47-52, 1-7, 9-14	I0-I23	Dedicated inputs
37-40	/B0-/B3	Fuse-programmable bidirectional I/Os with Active-Low outputs. Can be configured as open-collector outputs.
15-18	B4-B7	Logic controlled bidirectional I/Os with Active-High Tri-state outputs.
28-29 30-31 32-33 35-36	X0-X1 X2-X3 X4-X5 X6-X7	Pairs of Tri-state Exclusive-OR outputs that have common Output Enable.
19, 21 22-23	O0-O1 O2-O3	Pairs of dedicated Active-Low Tri-state output buffers. Each pair has common Output Enable control.
24-25 26-27	O4-O5 O6-O7	Pairs of dedicated Active-High Tri-state output buffers. Each pair has common Output Enable control.

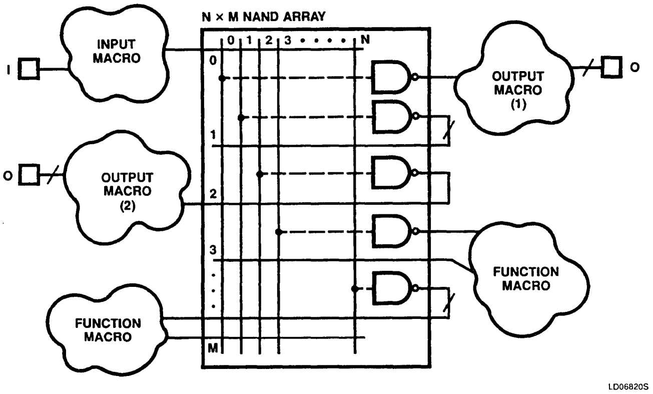


Figure 2. PML Fundamental Architecture

THE PLHS501 PML

The PLHS501 architecture in Figure 3 exhibits an exquisite logic tool. The device provides a combination of 72 NAND terms, 24 dedicated inputs (I0-I23), eight bidirectional I/O's (B0-B7), eight exclusive-OR outputs (X0-X7), and eight dedicated outputs (O0-O7). Figure 4 shows the PLHS501 logic diagram and Table 1 illustrates the functional breakdown of the PLHS501 I/O pins.

Since the output of each NAND term feeds back to the inputs of the NAND array, intricate logic functions can be implemented without wasting valuable I/O pins. For example, in order to implement an internal 'RS' latch in a combinational PAL^{TM}/PLD, at least two inputs and two outputs are required. The same internal latch can be configured by the PLHS501 without using any I/O pins.

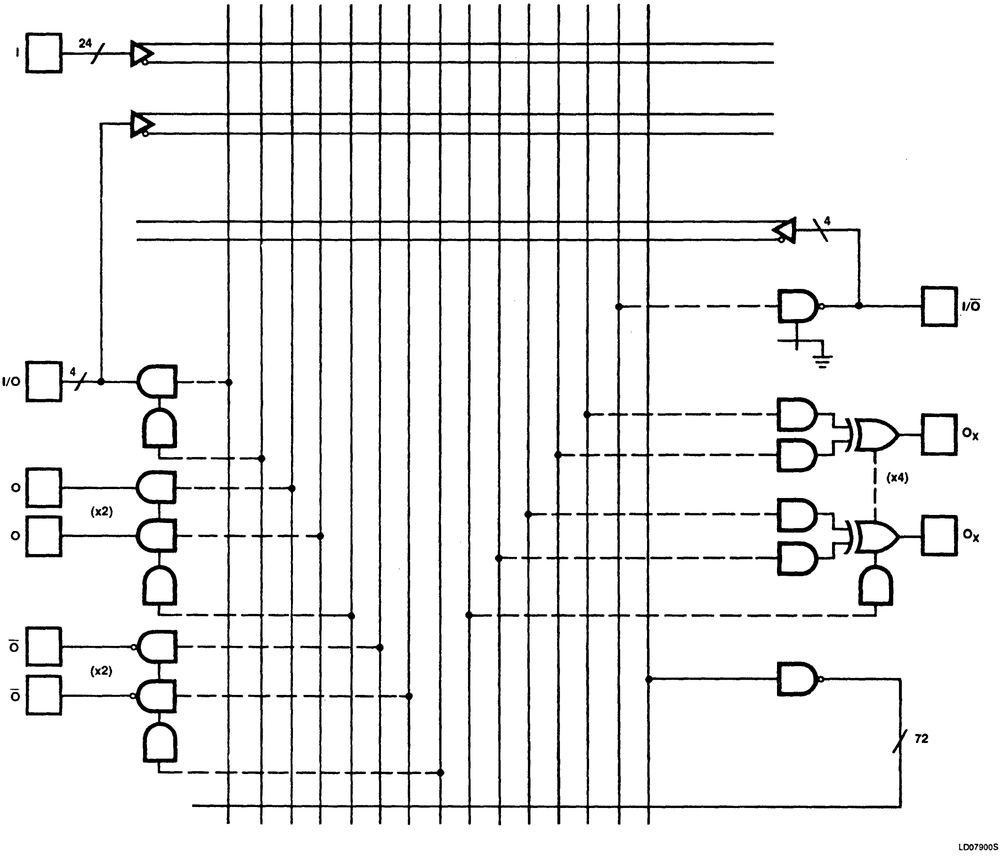


Figure 3. PLHS501 Logic Diagram

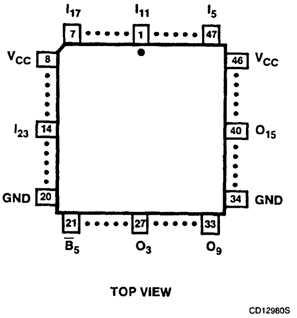
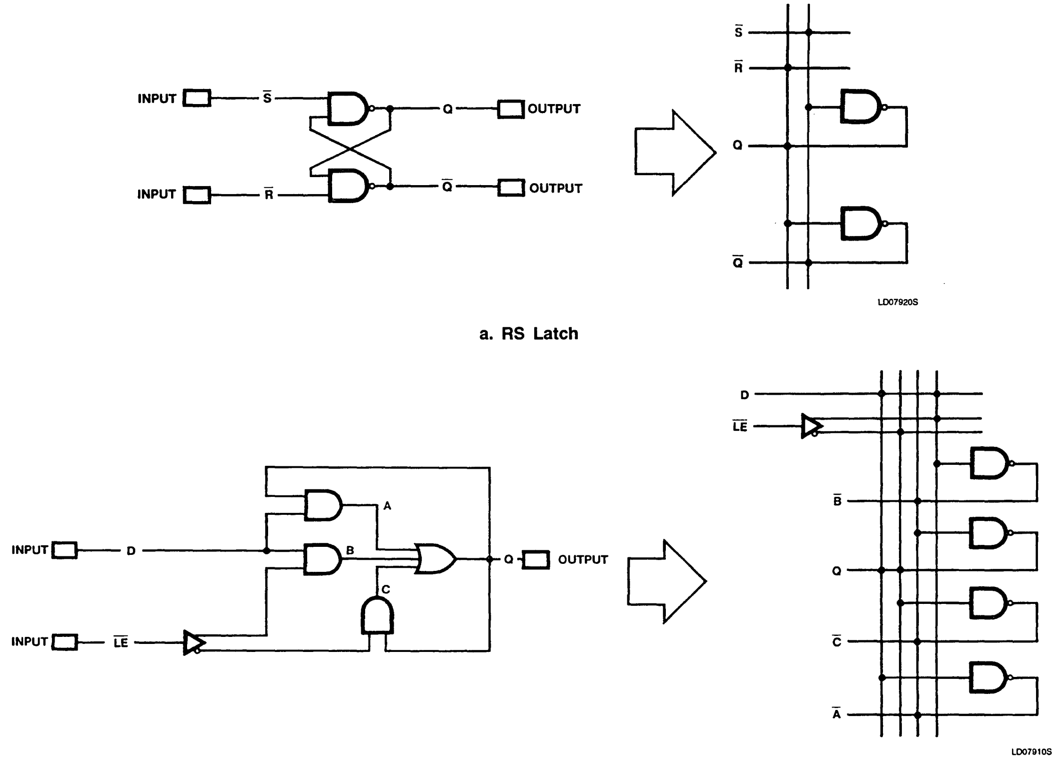


Figure 4. PLHS501 Pin Assignments

Figure 5 illustrates how 'RS' and 'D' latches are implemented in the PLHS501.

Another eminent application of the PLHS501 is in generating asynchronous state machines.

The blend of internal feedback paths together with the abundant number of gates makes this device suitable for designing asynchronous state machines which employ propagation delays of feedback paths as memory elements as shown in Figure 6. (See Reference 2.)



a. RS Latch

b. D Latch

Figure 5. R/S and D Latch Implementation with PML

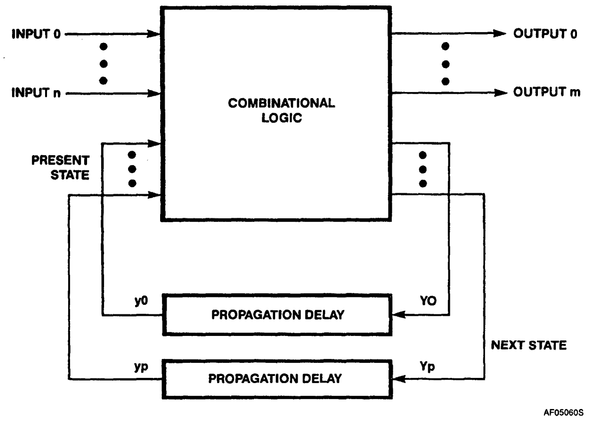


Figure 6. Model of Asynchronous State Machines Using Propagation Delays of the Feedback Path as Memory Elements

PML DEVELOPMENT SOFTWARE

Programmable logic development software has become an integral part of the PLD design process. Without software tools PLDs become perplexing devices which are inconvenient to use. Development software enables the user to take full advantage of the programmable logic's resources. The complexity of the PML devices makes software an indispensable element in the design process.

The AMAZE PLD design software, as noted in Reference 3, has been developed for Signetics programmable logic devices. PML design and development will be fully supported by AMAZE. Figure 7 shows the AMAZE configuration for supporting PML. The structure of the software is based on the following modules:

.BLAST	(Boolean Logic And State Transfer entry)
.DPI	(Device Programmer Interface)
.SIM	(PLD functional SIMulator)
.PI	(PML Integrator)

The foundation for the above modules is an AMAZE standard fuse file (STD). The STD file is the common means of communication between all the modules. The following paragraphs briefly explain the implementation of PML in the AMAZE structure.

BLAST

The basic elements of BLAST are:

1. Boolean Equation Entry (BEE).
2. State Equation Entry (SEE).
3. Schematic To Boolean Converter (STBC).

1. BEE accepts user defined logic in the form of boolean equations and produces an AMAZE standard fuse file. The boolean notation in BEE will account for the following PML features.

a. The single array architecture provides an option to specify the number of logic (gate) levels that accommodate a specified function. The number of gate levels dictate the delay between the inputs and outputs. The number of logic levels for each function can be specified using the following notation:

LABEL [number of logic levels] = equation; where LABEL is the user designated name of the output pin.

b. Some outputs have more than one gate associated with them (for example, registered or EXOR outputs). The input SIDE of these outputs can be specifically defined. For example:

Pin Label: R = eqn;
S = eqn;

c. User definable CLOCK Logic (e.g. as in the PLHS502) can be specified.

d. For PML devices the Sum-of-Products (SOP) can be defined as common terms.

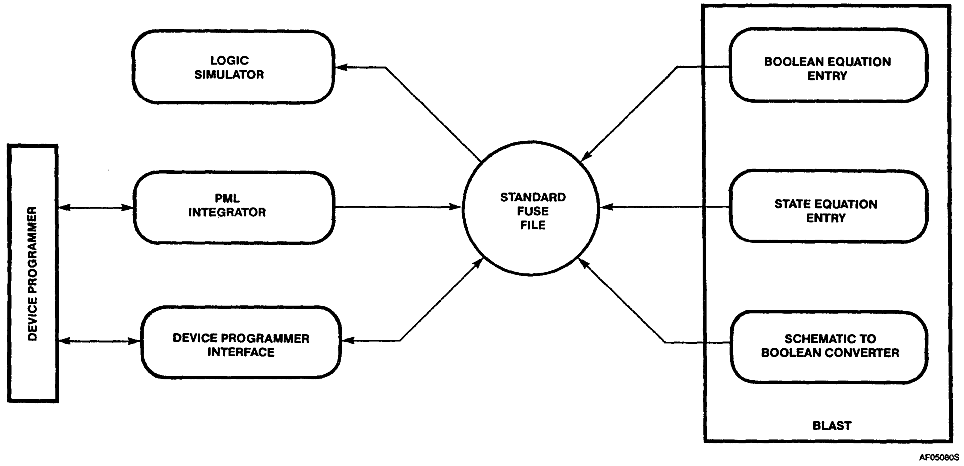


Figure 7. AMAZE Configuration for PML

2. SEE accepts state machine definitions and produces the AMAZE standard fuse file. Particularly, SEE will include asynchronous state machine implementations utilizing the PLHS501.

3. STBC converst schematic netlists produced by CAD systems such as Futurenet^{TM}, Daisy, and Mentor into an AMAZE BEE file. STBC will fully embody the PML in the following manner:

a. De Morgan's theorem is applied to produce equations in SOP form. All the functions in SOP form are then converted into their NAND- NAND equivalent.

b. The converter will determine the polarity and the number of levels in each equation and will automatically determine the correct output polarity.

DPI

Device Programmer Interface provides the interface between the AMAZE standard fuse file and a commercial programmer. It allows the transmission of data to and from the device programmer.

SIM

The functional simulator uses the AMAZE standard fuse file in the following manner:

a. An event driven simulator will assess the delays within the PML in order to properly simulate the pattern.

b. Automatically generates test vectors for the pattern simulation.

PI

The PML Integrator is a conversion that transforms various PAL^{TM} or PLD circuits into a PML device. It will automatically fit multiple PAL^{TM}/PLD devices into a single PML. It is capable of automatically receiving patterns from a commercial device programmer and downloading it back to the programmer after the PML transformation. The implementation of an 'Integrator' will allow the automatic conversion of numerous PAL^{TM}/PLDs into a single PML device.

AMAZE will not be the total extent of development software available for the PML devices. The task of implementing PML design software is already underway by a number of different vendors of CAD software.

PLHS501 DESIGN EXAMPLE

The following example intends to manifest the capabilities of the PLHS501. Figure 8 shows a system formed with TTL logic. The system requirements make it imperative only to use discrete asynchronous latches. Thus, none of the 7 latches in the system can be directly replaced by registers. The system diagram is drafted using Futurenet^{TM} DASH-2 Schematic Designer. The system is partitioned into two PLS173s and one PLS153. In order to convert the system into its targeted PLD's, the PINLIST (see Figures 9a-9c) has to be defined. Using the AMAZE PIN-LIST editor, the specified PLD's are labeled with the same labels as those on the system schematic (Figure 8). After the declaration of labels, AMAZE automatically converts the system to the designated PLDs. The AMAZE generated boolean equation files are shown in Figures 9a, 9b, and 9c. Figure 10 shows the overall system implemented with PLDs. The logic condensation capabilities of PML makes it feasible to replace the whole system by a single PLHS501 (Figure 11). The PLHS501 in this design will still have ample space for any future additions.

The above example demonstrates only part of the PLHS501 capabilities. The introduction of PML devices and their immense logic power will pave the way for a new generation of efficient and elegant systems.

REFERENCES

1. Cavlan, Napoleone 1985. "Third Generation PLD Architecture Breaks AND-OR Bottleneck", WESCON 1985 Conference Proceedings.

2. Wong, David K. "Third Generation PLS Architecture and its Applications", Electro 1986 Conference Proceedings.

3. "1986 PLD Data Manual", Signetics Corporation.

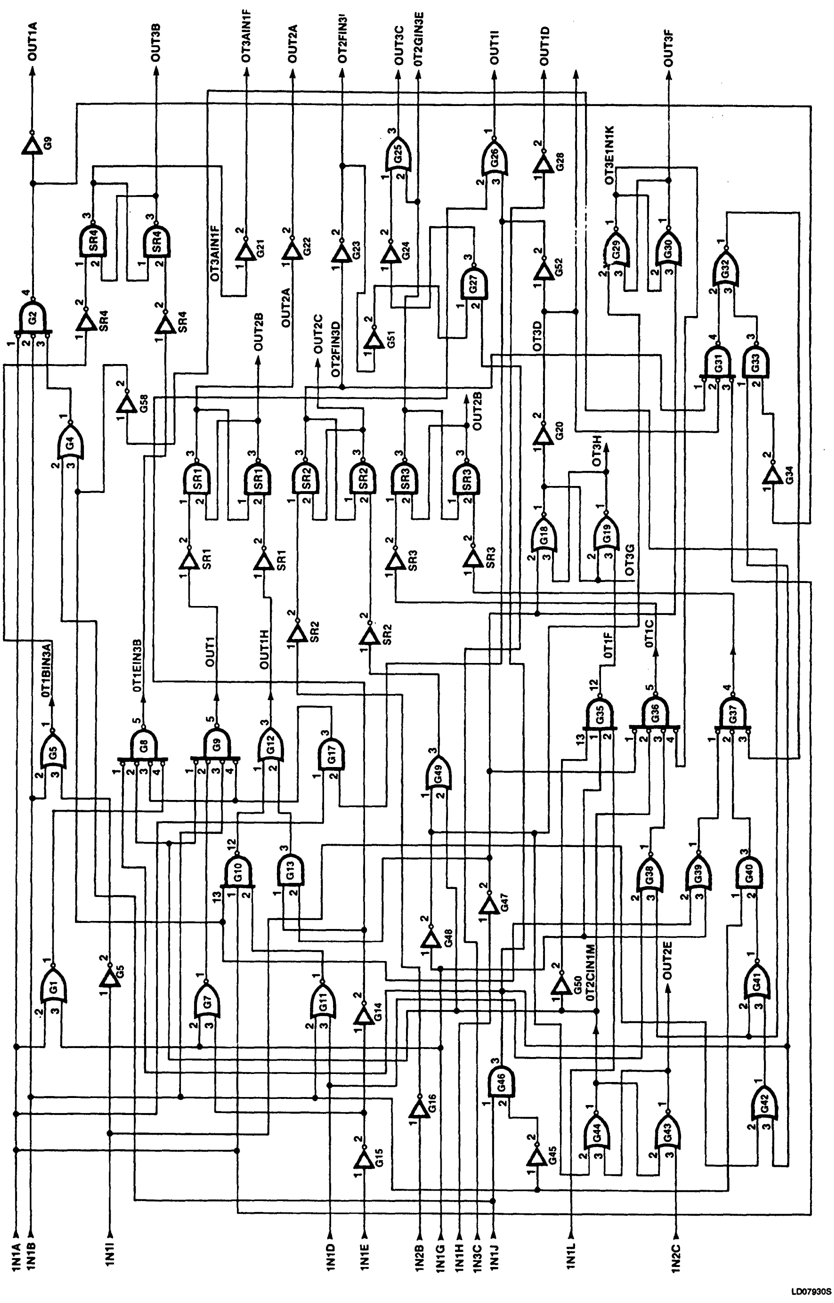
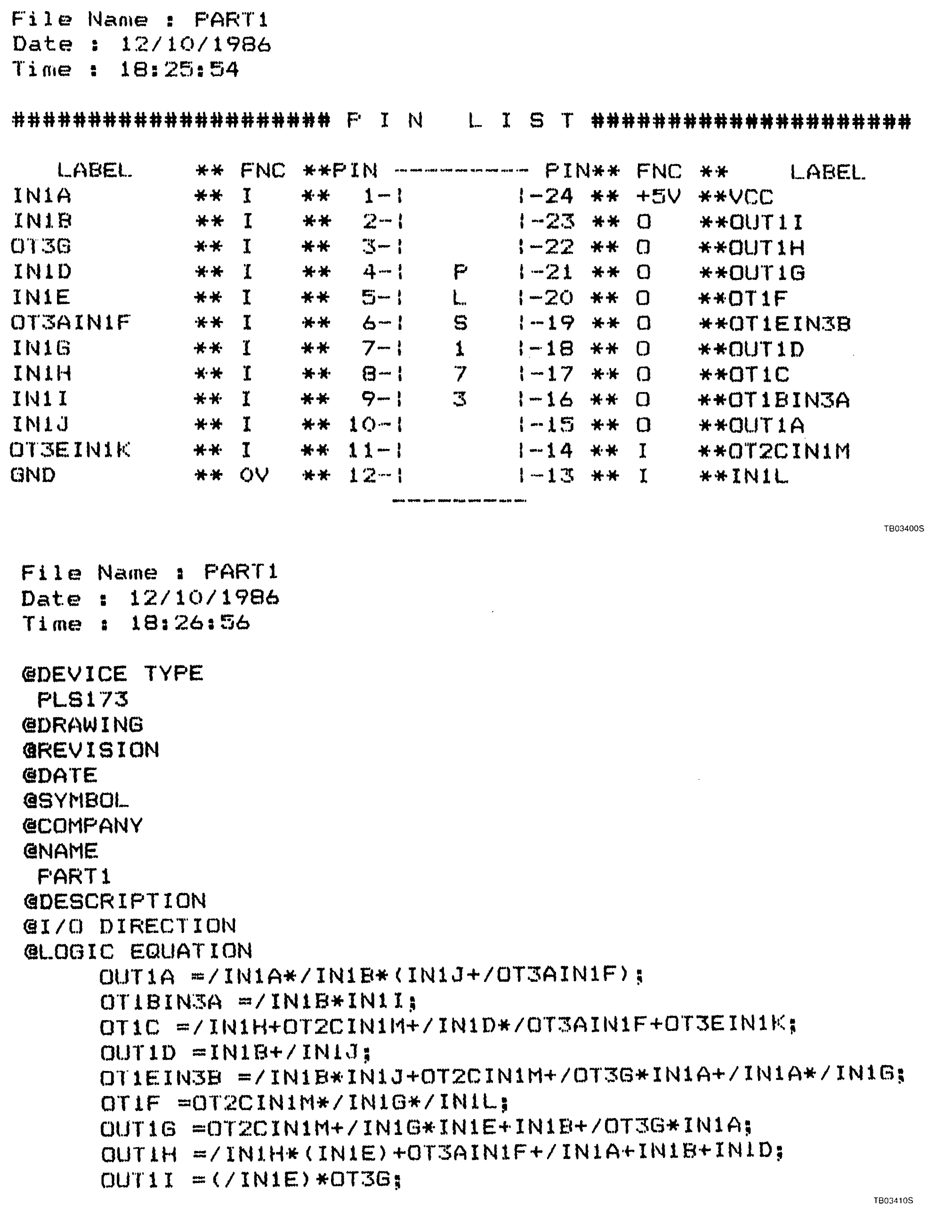


Figure 8. System Implemented with TTL Logic



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IN1A          ** I   **  1-!        !-24 ** +5V **VCC
IN1B          ** I   **  2-!        !-23 ** O   **OUT1I
OT3G          ** I   **  3-!        !-22 ** O   **OUT1H
IN1D          ** I   **  4-!   P    !-21 ** O   **OUT1G
IN1E          ** I   **  5-!   L    !-20 ** O   **OT1F
OT3AIN1F      ** I   **  6-!   S    !-19 ** O   **OT1EIN3B
IN1G          ** I   **  7-!   1    !-18 ** O   **OUT1D
IN1H          ** I   **  8-!   7    !-17 ** O   **OT1C
IN1I          ** I   **  9-!   3    !-16 ** O   **OT1BIN3A
IN1J          ** I   ** 10-!        !-15 ** O   **OUT1A
OT3EIN1K      ** I   ** 11-!        !-14 ** I   **OT2CIN1M
GND           ** OV  ** 12-!        !-13 ** I   **IN1L
                             ----------
```

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@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
 PART1
@DESCRIPTION
@I/O DIRECTION
@LOGIC EQUATION
     OUT1A =/IN1A*/IN1B*(IN1J+/OT3AIN1F);
     OT1BIN3A =/IN1B*IN1I;
     OT1C =/IN1H+OT2CIN1M+/IN1D*/OT3AIN1F+OT3EIN1K;
     OUT1D =IN1B+/IN1J;
     OT1EIN3B =/IN1B*IN1J+OT2CIN1M+/OT3G*IN1A+/IN1A*/IN1G;
     OT1F =OT2CIN1M*/IN1G*/IN1L;
     OUT1G =OT2CIN1M+/IN1G*IN1E+IN1B+/OT3G*IN1A;
     OUT1H =/IN1H*(IN1E)+OT3AIN1F+/IN1A+IN1B+IN1D;
     OUT1I =(/IN1E)*OT3G;
```

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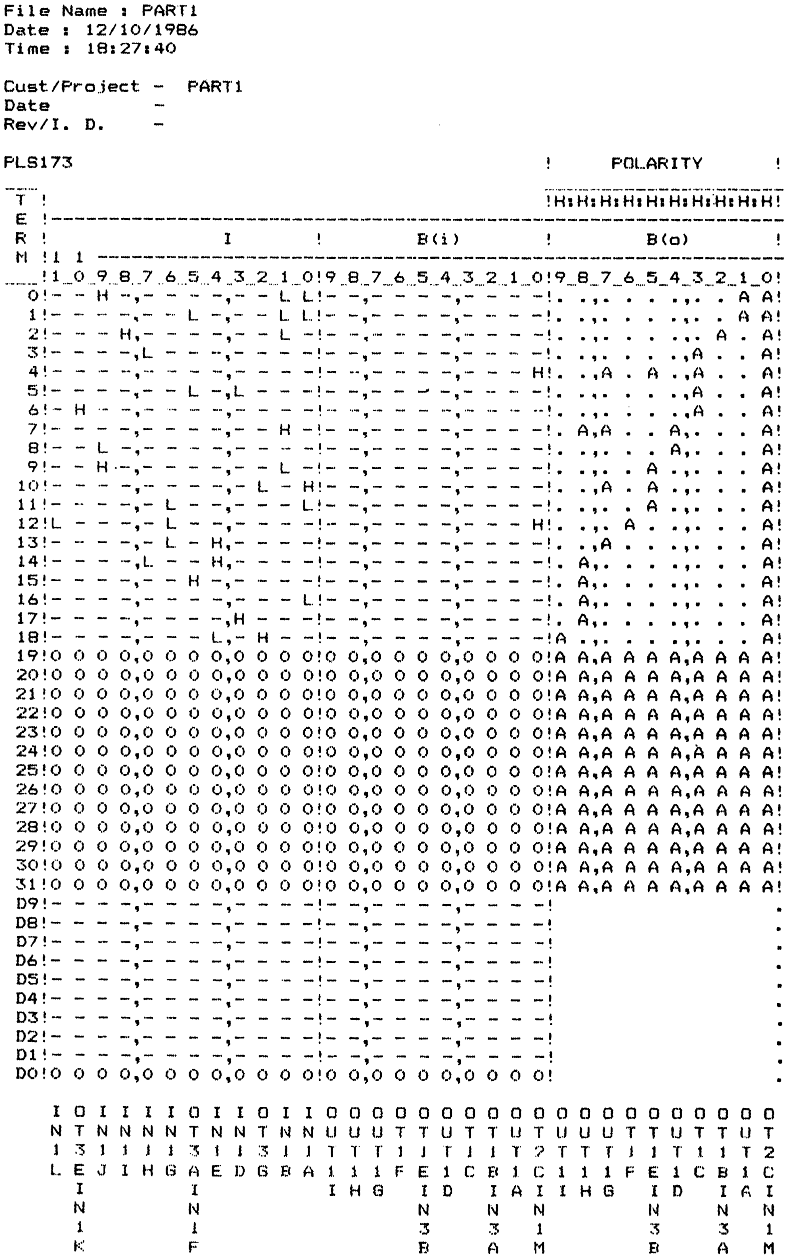
Figure 9a. Part 1: PLS173



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Cust/Project -  PART1
Date         -
Rev/I. D.    -

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----                                            ---------------------
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  E !----------------------------------------------------------------
  R !           I           !       B(i)        !       B(o)        !
  M !1 1 ------------------------------------------------------------
____!1_0_9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
   0!- - H -,- - - -,- - L L!- -,- - - -,- - - -!. .,. . . .,. . A A!
   1!- - - -,- - L -,- - L L!- -,- - - -,- - - -!. .,. . . .,. . A A!
   2!- - - H,- - - -,- - L -!- -,- - - -,- - - -!. .,. . . .,. A . A!
   3!- - - -,L - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,A . . A!
   4!- - - -,- - - -,- - - -!- -,- - - -,- - - H!. .,A . A .,A . . A!
   5!- - - -,- - L -,L - - -!- -,- - - -,- - - -!. .,. . . .,A . . A!
   6!- H - -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . .,A . . A!
   7!- - - -,- - - -,- - H -!- -,- - - -,- - - -!. A,A . . A,. . . A!
   8!- - L -,- - - -,- - - -!- -,- - - -,- - - -!. .,. . . A,. . . A!
   9!- - H -,- - - -,- - L -!- -,- - - -,- - - -!. .,. . A .,. . . A!
  10!- - - -,- - - -,- L - H!- -,- - - -,- - - -!. .,A . A .,. . . A!
  11!- - - -,- L - -,- - - L!- -,- - - -,- - - -!. .,. . A .,. . . A!
  12!L - - -,- L - -,- - - -!- -,- - - -,- - - H!. .,. A . .,. . . A!
  13!- - - -,- L - H,- - - -!- -,- - - -,- - - -!. .,A . . .,. . . A!
  14!- - - -,L - - H,- - - -!- -,- - - -,- - - -!. A,. . . .,. . . A!
  15!- - - -,- - H -,- - - -!- -,- - - -,- - - -!. A,. . . .,. . . A!
  16!- - - -,- - - -,- - - L!- -,- - - -,- - - -!. A,. . . .,. . . A!
  17!- - - -,- - - -,H - - -!- -,- - - -,- - - -!. A,. . . .,. . . A!
  18!- - - -,- - - L,- H - -!- -,- - - -,- - - -!A .,. . . .,. . . A!
  19!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  20!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  21!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  22!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  23!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
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  25!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  26!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  27!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  28!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  29!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  30!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  31!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  D9!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D8!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D7!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D6!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D5!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D4!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D3!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D2!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D1!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
  D0!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .

     I O I I I I O I I O I I O O O O O O O O O O O O O O O O O O O O
     N T N N N N T N N T N N U U U T T U T T U T U U U T T U T T U T
     1 3 1 1 1 1 3 1 1 3 1 1 T T T 1 1 T 1 1 T ? T T T 1 1 T 1 1 T 2
     L E J I H G A E D G B A 1 1 1 F E 1 C B 1 C 1 1 1 F E 1 C B 1 C
       I         I           I H G   I D   I A I I H G   I D   I A I
       N         N                   N     N   N         N     N   N
       1         1                   3     3   1         3     3   1
       K         F                   B     A   M         B     A   M
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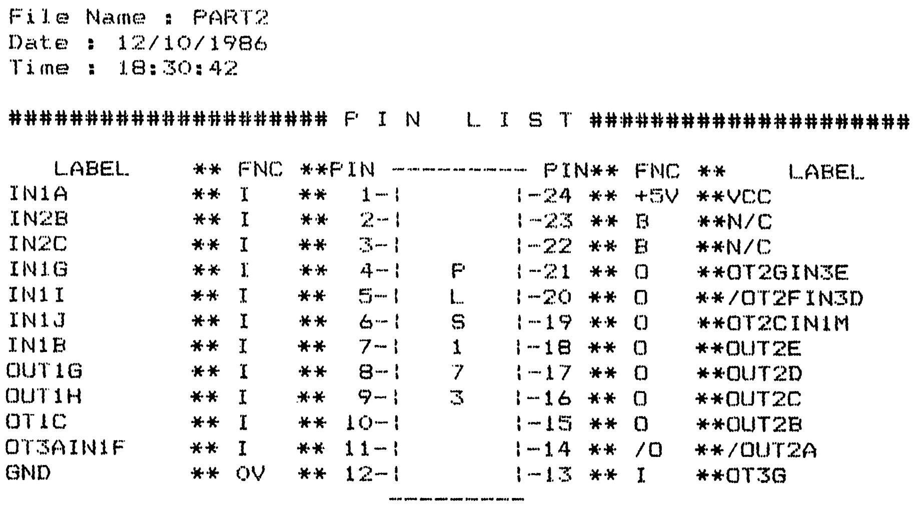
Figure 9a. Part 1: PLS173 (Continued)



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IN1A         ** I   **  1-|         |-24 ** +5V **VCC
IN2B         ** I   **  2-|         |-23 ** B   **N/C
IN2C         ** I   **  3-|         |-22 ** B   **N/C
IN1G         ** I   **  4-|    P    |-21 ** O   **OT2GIN3E
IN1I         ** I   **  5-|    L    |-20 ** O   **/OT2FIN3D
IN1J         ** I   **  6-|    S    |-19 ** O   **OT2CIN1M
IN1B         ** I   **  7-|    1    |-18 ** O   **OUT2E
OUT1G        ** I   **  8-|    7    |-17 ** O   **OUT2D
OUT1H        ** I   **  9-|    3    |-16 ** O   **OUT2C
OT1C         ** I   ** 10-|         |-15 ** O   **OUT2B
OT3AIN1F     ** I   ** 11-|         |-14 ** /O  **/OUT2A
GND          ** OV  ** 12-|         |-13 ** I   **OT3G
                           ----------
```

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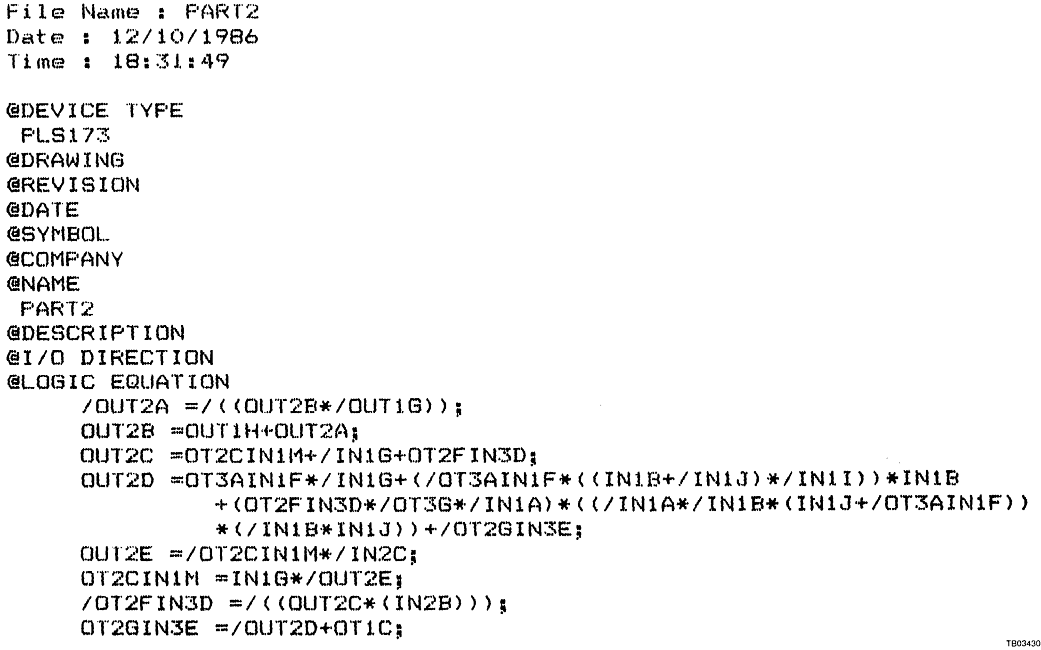

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 PLS173
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
 PART2
@DESCRIPTION
@I/O DIRECTION
@LOGIC EQUATION
     /OUT2A =/((OUT2B*/OUT1G));
     OUT2B =OUT1H+OUT2A;
     OUT2C =OT2CIN1M+/IN1G+OT2FIN3D;
     OUT2D =OT3AIN1F*/IN1G+(/OT3AIN1F*((IN1B+/IN1J)*/IN1I))*IN1B
              +(OT2FIN3D*/OT3G*/IN1A)*((/IN1A*/IN1B*(IN1J+/OT3AIN1F))
              *(/IN1B*IN1J))+/OT2GIN3E;
     OUT2E =/OT2CIN1M*/IN2C;
     OT2CIN1M =IN1G*/OUT2E;
     /OT2FIN3D =/((OUT2C*(IN2B)));
     OT2GIN3E =/OUT2D+OT1C;
```

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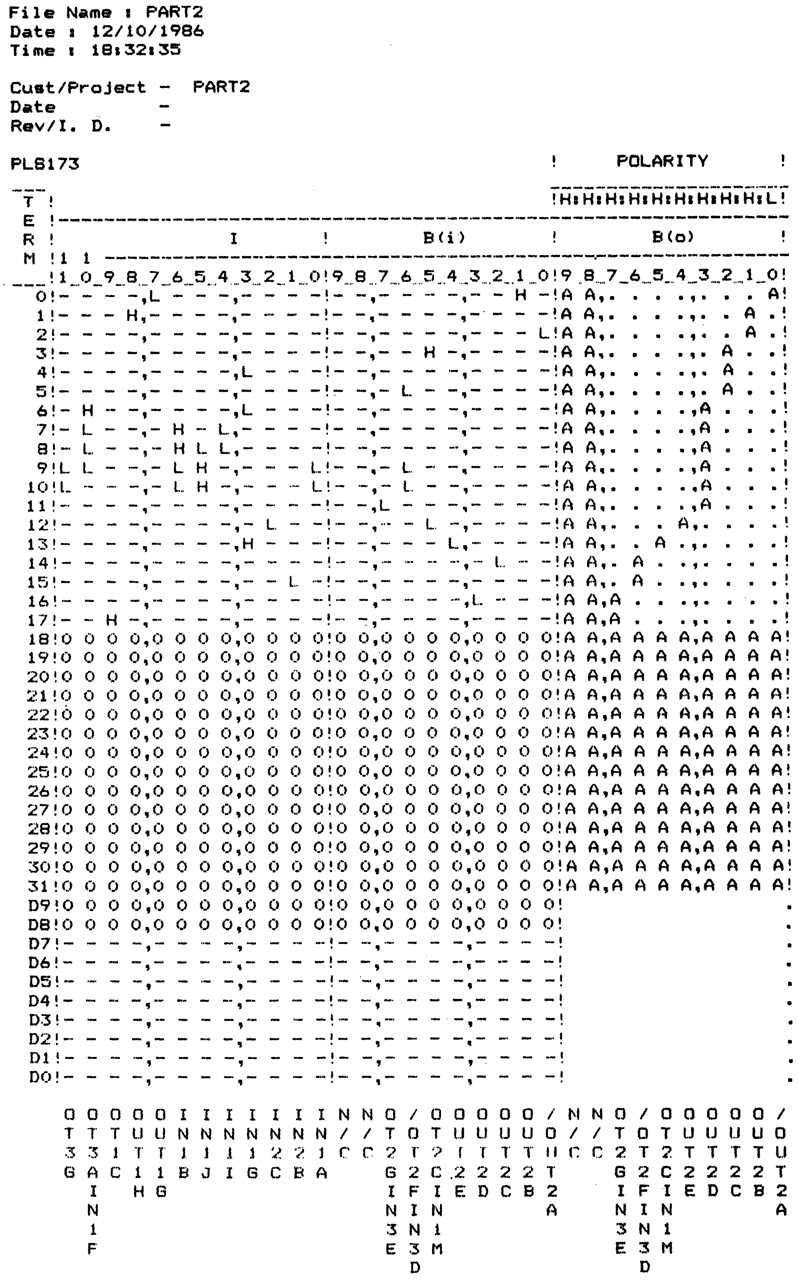
Figure 9b. Part 2: PLS173



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Cust/Project -  PART2
Date         -
Rev/I. D.    -

PLS173                                         !      POLARITY     !
---                                            ---------------------
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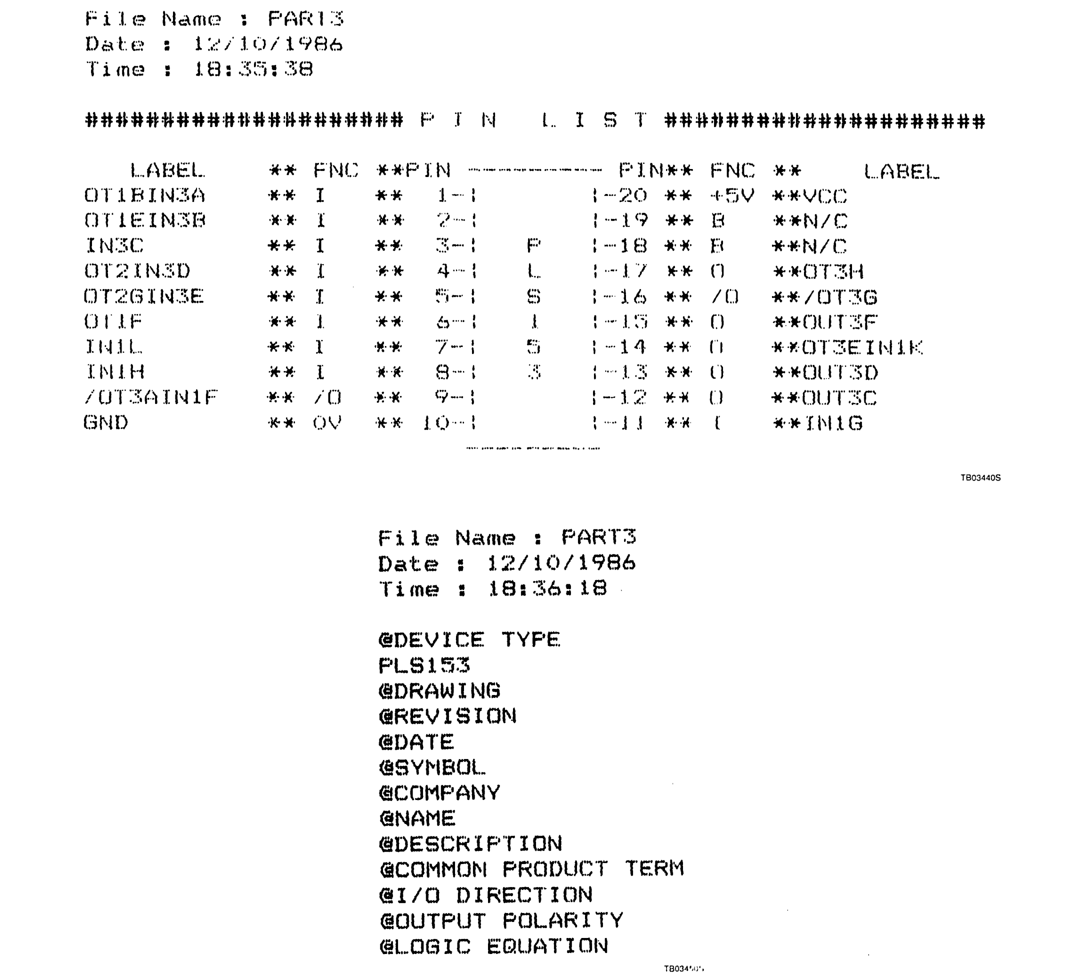
 E !----------------------------------------------------------------
 R !           I           !        B(i)       !        B(o)       !
 M !1 1 ------------------------------------------------------------
___!1_0_9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!- - - -,L - - -,- - - -!- -,- - - -,- - H -!A A,. . . .,. . . A!
  1!- - - H,- - - -,- - - -!- -,- - - -,- - - -!A A,. . . .,. . A .!
  2!- - - -,- - - -,- - - -!- -,- - - -,- - - L!A A,. . . .,. . A .!
  3!- - - -,- - - -,- - - -!- -,- - H -,- - - -!A A,. . . .,. A . .!
  4!- - - -,- - - -,L - - -!- -,- - - -,- - - -!A A,. . . .,. A . .!
  5!- - - -,- - - -,- - - -!- -,- L - -,- - - -!A A,. . . .,. A . .!
  6!- H - -,- - - -,L - - -!- -,- - - -,- - - -!A A,. . . .,A . . .!
  7!- L - -,- H - L,- - - -!- -,- - - -,- - - -!A A,. . . .,A . . .!
  8!- L - -,- H L L,- - - -!- -,- - - -,- - - -!A A,. . . .,A . . .!
  9!L L - -,- L H -,- - - L!- -,- L - -,- - - -!A A,. . . .,A . . .!
 10!L - - -,- L H -,- - - L!- -,- L - -,- - - -!A A,. . . .,A . . .!
 11!- - - -,- - - -,- - - -!- -,L - - -,- - - -!A A,. . . .,A . . .!
 12!- - - -,- - - -,- L - -!- -,- - L -,- - - -!A A,. . . A,. . . .!
 13!- - - -,- - - -,H - - -!- -,- - - L,- - - -!A A,. . A .,. . . .!
 14!- - - -,- - - -,- - - -!- -,- - - -,- L - -!A A,. A . .,. . . .!
 15!- - - -,- - - -,- - L -!- -,- - - -,- - - -!A A,. A . .,. . . .!
 16!- - - -,- - - -,- - - -!- -,- - - -,L - - -!A A,A . . .,. . . .!
 17!- - H -,- - - -,- - - -!- -,- - - -,- - - -!A A,A . . .,. . . .!
 18!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 19!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 23!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 25!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 27!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 31!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 D9!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D8!0 0 0 0,0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D7!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D6!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D5!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D4!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D3!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D2!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D1!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .
 D0!- - - -,- - - -,- - - -!- -,- - - -,- - - -!                   .

    O O O O O I I I I I I I N N O / O O O O O / N N O / O O O O O /
    T T T U U N N N N N N N / / T O T U U U U O / / T O T U U U U O
    3 3 1 T T 1 1 1 1 2 2 1 C C 2 T ? I T T T U C C 2 T 2 T T T T U
    G A C 1 1 B J I G C B A     G 2 C 2 2 2 2 T     G 2 C 2 2 2 2 T
      I   H G                   I F I E D C B 2     I F I E D C B 2
      N                         N I N         A     N I N         A
      1                         3 N 1               3 N 1
      F                         E 3 M               E 3 M
                                  D                   D
```

TB03470S

Figure 9b. Part 2: PLS173 (Continued)



```
File Name : PART3
Date : 12/10/1986
Time : 18:35:38

##################### P I N   L I S T #####################

   LABEL      ** FNC **PIN ------------ PIN** FNC **    LABEL
OT1BIN3A      ** I   **  1-|           |-20 ** +5V **VCC
OT1EIN3B      ** I   **  2-|           |-19 ** B   **N/C
IN3C          ** I   **  3-|     P     |-18 ** B   **N/C
OT2IN3D       ** I   **  4-|     L     |-17 ** O   **OT3H
OT2GIN3E      ** I   **  5-|     S     |-16 ** /O  **/OT3G
OT1F          ** I   **  6-|     1     |-15 ** O   **OUT3F
IN1L          ** I   **  7-|     5     |-14 ** O   **OT3EIN1K
IN1H          ** I   **  8-|     3     |-13 ** O   **OUT3D
/OT3AIN1F     ** /O  **  9-|           |-12 ** O   **OUT3C
GND           ** OV  ** 10-|           |-11 ** I   **IN1G
                           -------------
```

TB03440S

```
File Name : PART3
Date : 12/10/1986
Time : 18:36:18

@DEVICE TYPE
PLS153
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION
@COMMON PRODUCT TERM
@I/O DIRECTION
@OUTPUT POLARITY
@LOGIC EQUATION
```

TB034[illegible]

Figure 9c. Part 3: PLS153

```
File Name : PART3
Date : 12/10/1986
Time : 18:36:47

Cust/Project -
Date         -
Rev/I. D.    -

PLS153                                 !      POLARITY     !
---                                    ---------------------
 T !                                   !H:H:H:L:H:H:H:H:H:L!
 E !--------------------------------------------------------
 R !       I       !       B(i)        !       B(o)        !
 M !--------------------------------------------------------
___!7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!9_8_7_6_5_4_3_2_1_0!
  0!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  1!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  2!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  3!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  4!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  5!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  6!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  7!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  8!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
  9!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 10!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 11!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 12!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 13!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 14!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 15!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 16!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 17!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 18!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 19!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 20!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 21!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 22!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 23!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 24!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 25!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 26!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 27!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 28!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 29!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 30!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 31!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!A A,A A A A,A A A A!
 D9!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D8!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D7!- - - -,- - - -!- -,- - - -,- - - -!                   .
 D6!- - - -,- - - -!- -,- - - -,- - - -!                   .
 D5!- - - -,- - - -!- -,- - - -,- - - -!                   .
 D4!- - - -,- - - -!- -,- - - -,- - - -!                   .
 D3!- - - -,- - - -!- -,- - - -,- - - -!                   .
 D2!- - - -,- - - -!- -,- - - -,- - - -!                   .
 D1!0 0 0 0,0 0 0 0!0 0,0 0 0 0,0 0 0 0!                   .
 D0!- - - -,- - - -!- -,- - - -,- - - -!                   .

    I I O O O I O O N N O / O O O O I / N N O / O O O O I /
    N N T T T N T T / / T O U T U U N O / / T O U T U U N O
    1 1 1 2 2 3 1 1 C C 3 T T 3 T T 1 T C C 3 T T 3 T T 1 T
    H L F G I C E B     H 3 3 E 3 3 G 3     H 3 3 E 3 3 G 3
          I N   I I       G F I D C   A       G F I D C   A
          N 3   N N           N       I           N       I
          3 D   3 3           1       N           1       N
          E     B A           K       1           K       1
                                      F                   F
```

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Figure 9c. Part 3: PLS153 (Continued)

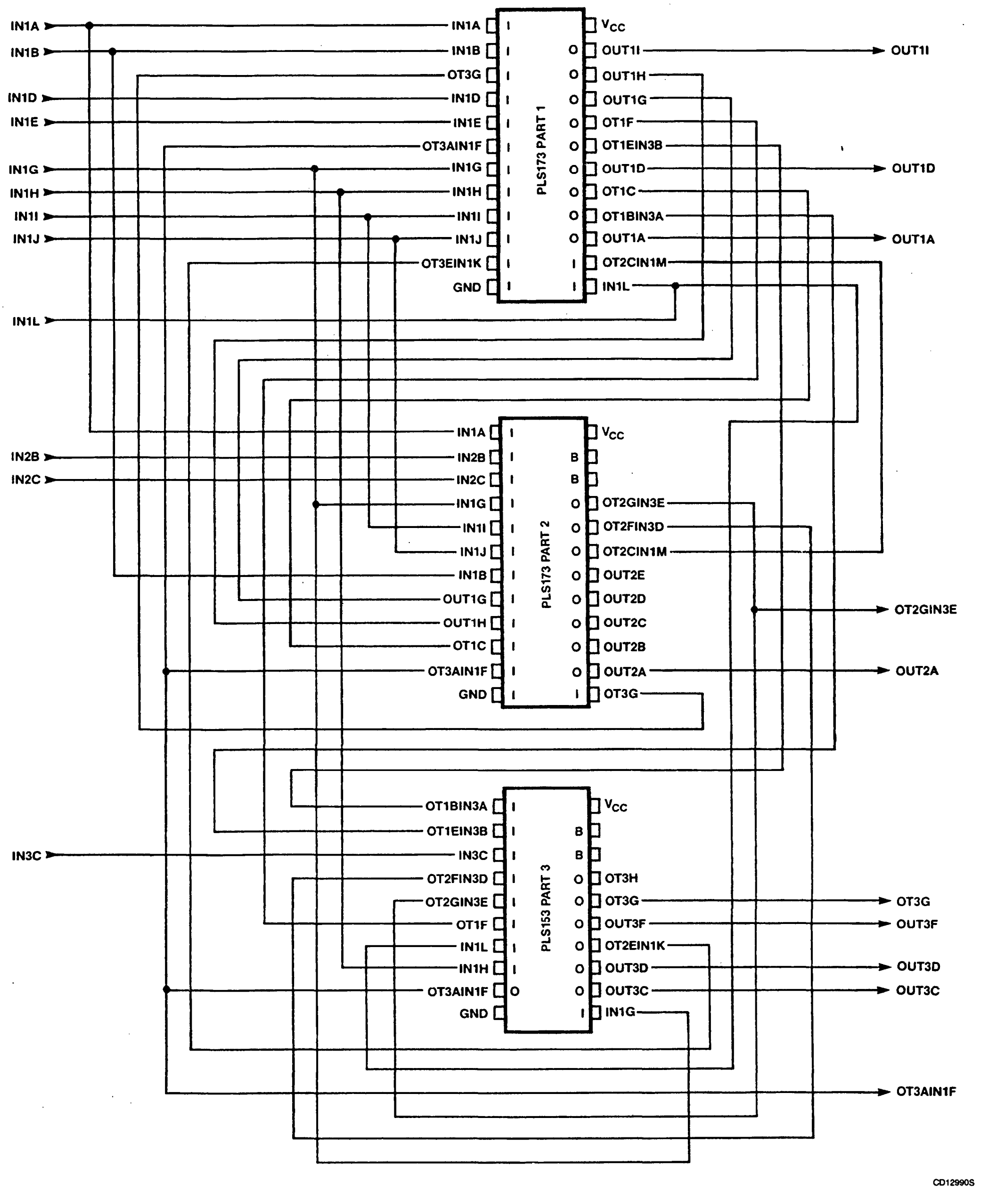


Figure 10. System in Figure 8 Implemented with PLD's

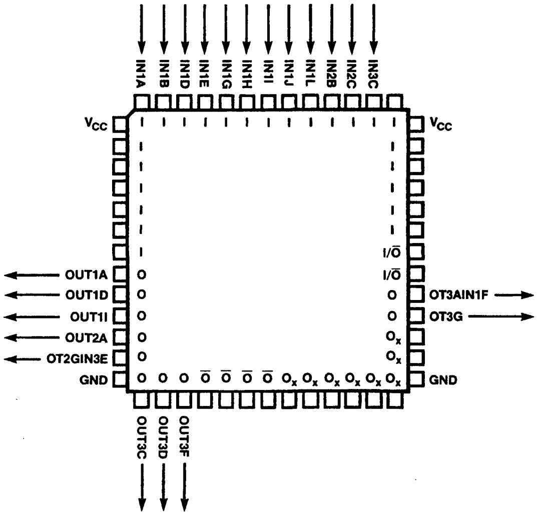


Figure 11. System in Figure 10 Implemented with PLHS501

Signetics

Designing with Programmable Macro Logic

Application Specific Products

INTRODUCTION TO PML DESIGN CONCEPTS

Programmable Macro Logic, an extension of the Programmable Logic Array (PLA) concept combines a programming or fuse array with an array of wide input NAND gates wherein each gate folds back upon itself and all other such NAND gates. This is called a foldback NAND structure and its basic elements have been outlined previously (Cavlan[1], Wong[2], Gheissari and Safari[3]).

The choice of an internal NAND logic cell is appropriate because the cell is functionally complete, requiring but a single cell type to generate any Boolean function. A cell within the PLHS501 may be configured to accommodate from one to 32 inputs from the outside world, and up to 72 inputs from within the chip. Because the user can select either direct or inverted input variables, and either a direct or complemented output, the NAND function can generate, with a single pass through the programming array, the basic four logic functions of AND, OR, NAND, NOR. All these basic functions, can be extremely wide, of course (see Figure 1.1). This convenient structure allows efficient exploitation of all widely used minimization techniques (Karnaugh Maps, Quine-McCluskey, Boolean Algebra, etc.).

The obvious extensions to additional combinational functions for decoding, multiplexing and general Boolean functions is straightforward. Adding feedback to the system expands the range of realizeable functions to include sequential as well as combinational functions. Figure 1.2 illustrates the basic arrangement of the PLHS501. Because of the large number of inputs each NAND gate has available, logic functions that require several levels of conventional 4 or 8 input gates may be able to be reduced to 1 or 2 levels. However, it is important to realize that unlike AND-OR PLD architectures, more than 2 levels of logic may be implemented in the PLHS501 without wasting output or input pins. Up to 72 levels of logic may be implemented due to each of the 72 foldback NAND gates.

So far, the concept of a "macro" is still not evident. Two ways for the generation of a macro exist — namely, hard and soft. Borrowing from the concept in computer programming wherein a section of code (called a macro) is repeated every time its use is required, we can establish subfunctions which can be repeated each time required. The user defined or soft macro can be one which will generate a function by fused interconnect. When a fixed design function is provided, it is a hard macro. This may be an optimized structure like a flip-flop or an adder, or some other function which is generated on the foundation, by the manufacturer. Soft macros are seldom optimized or precisely consistent, but hard macros are both optimized and unalterable.

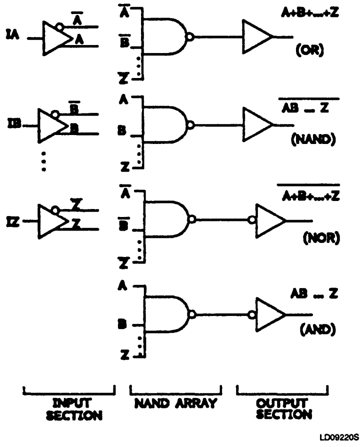


Figure 1.1 PML Basic Functions

When a user function for a particular use is isolated, defined and repetition of the function is required, special software constructs are provided which will allow it to be defined as a soft macro and efficiently replicated. For higher performance and functional density, an array of choices which contain optimized functions or hard macros will be offered in successor chips. In particular, the PLHS502 (described in Section 4) will include an array of flip-flops for high performance state machine design.

Optimizing combinational functions in PML consists largely in making choices and tradeoffs. For single output logic functions, the choice is obvious from the truth table. If a particular function's truth table has fewer entries that are logical zeroes than logical ones, product of sums should be chosen and the appropriate OR-AND structure generated. Otherwise, the usual sum of products should be chosen, minimizing as usual, before dropping into the two level AND-OR structure (using the NAND-NAND realization). Combining the availability of inversion at the input and output of the chip, the NAND-NAND structure can perform either the OR-AND or the AND-OR rendition of a function with equal ease, using precisely the same number of logic levels. The designer needs only to choose the optimal rendition to suit his needs (see Table 1.1). Truth tables with 50% ones can use either version at the designers whim unless other uses arise.

PERFORMANCE

The PLHS501 (Figure 1.2) is a high speed, oxide isolated, vertically fused PML device containing 72 internal NAND functions which are combined with 24 dedicated inputs, 8 bidirectionals and 16 dedicated outputs. A large collection of applications, both combinational and sequential, may be configured using this part which looks roughly like a small, user definable gate array. For the sake of clarity, worst case passing a signal from an input, making one pass through the NAND array (output terms) and exiting an output takes around 25 nanoseconds with each incremental pass through the NAND foldback array taking about 8 nanoseconds.

TABLE 1.1 EXAMPLE DEMONSTRATION

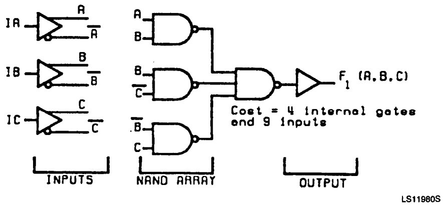
F1 (A, B, C) $\overline{=}$ ¯ABC¯ + ¯ABC¯ + ABC¯ + ABC + ABC

A	B	C	f1
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

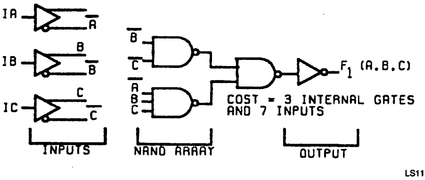
\ AB C\	00	01	11	10
0	0	1	1	0
1	1	0	1	1

The optimal choice would be to generate the zero entries.

If we group on the <u>one</u> entries we shall get: F_1 = AB¯ + $\overline{B}$C + BC



If we group on the <u>zero</u> entries we get instead: F_1 = (B + C) (A + B + C)



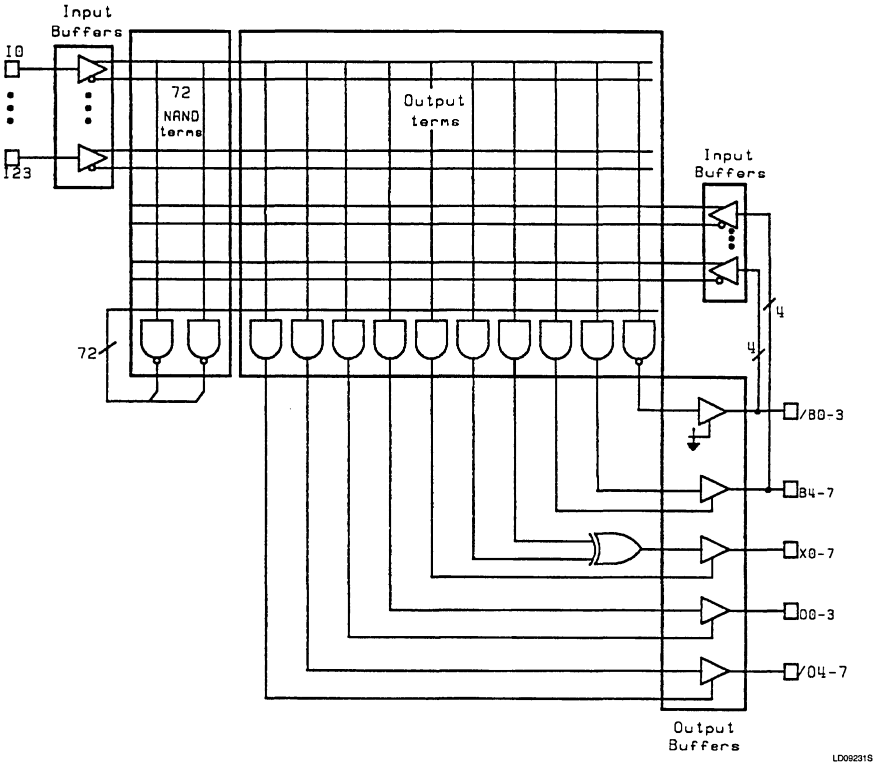


Figure 1.2 PLHS501 Logic Diagram

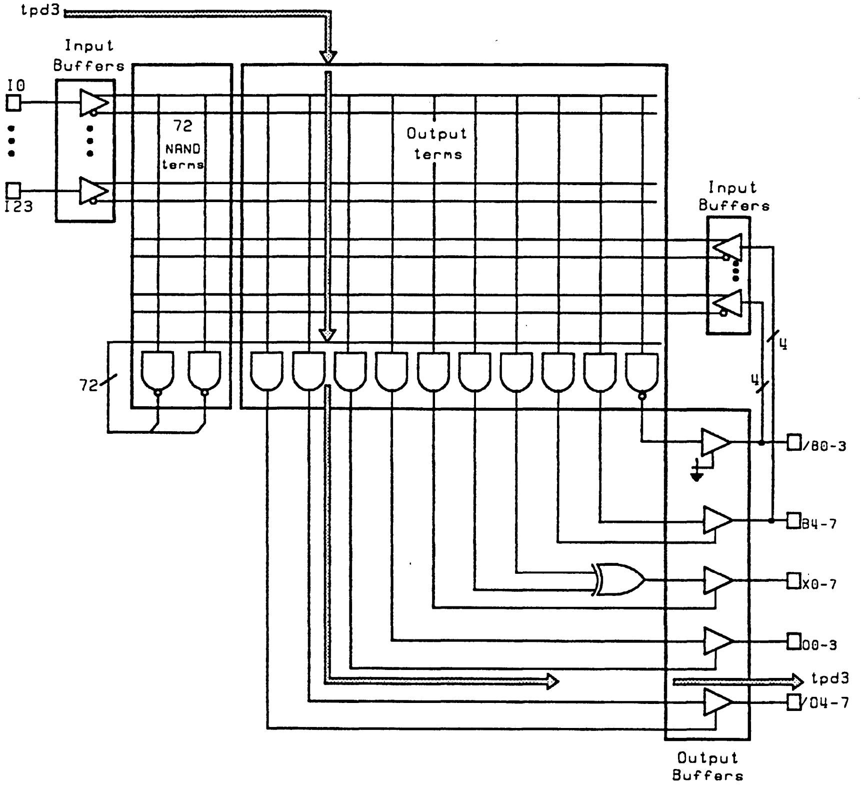
Designing with Programmable Macro Logic

The data sheet first lists some maximum propagation delays from an input, through a NAND output term and out through various output gates. Secondly, it lists maximum propagation delays from an input, through a NAND foldback term, through a NAND output term and out through the different output gates.

It is intriguing that subtracting one from the other yields a NAND foldback gate delay of 5 to 6ns when the worst case gate delay of an internal foldback gate is listed as 8ns. This is due to the fact that a gate has less of a delay when it's output is falling (tPHL) than when it's output is rising (tPLH). When passing a signal through two NAND gates one gate will have less of a delay than the other, and since the individual rise and fall delays are not specified, this causes the apparent discrepancy between the two delays.

Figure 1.3, Figure 1.4, Figure 1.5 and Figure 1.6 show graphically the timing paths listed in the PLHS501 data sheet.

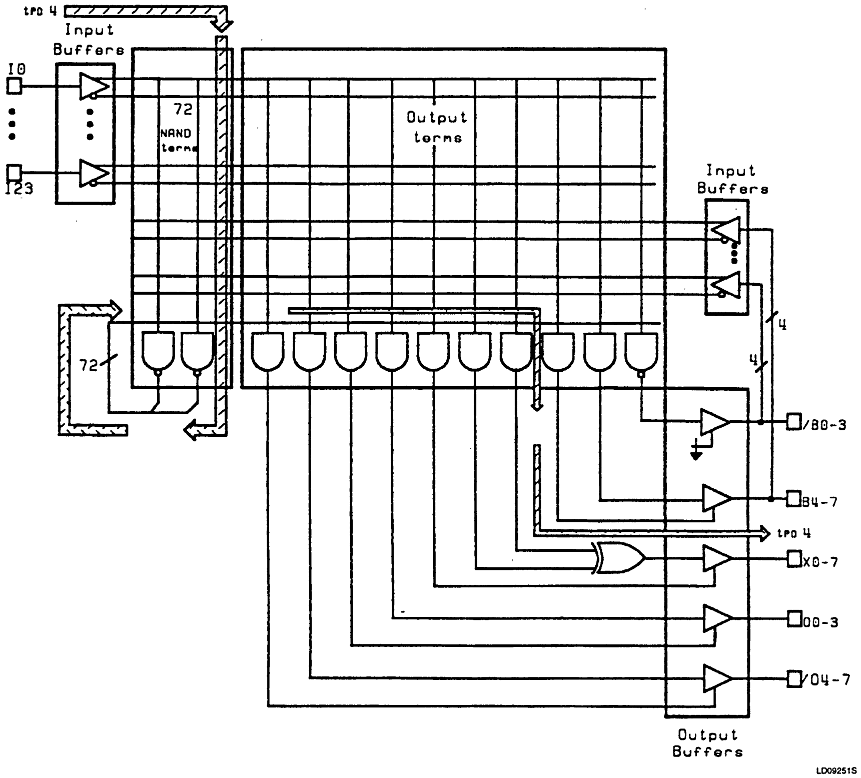
PLHS501 TIMING



NOTES:
tpd3 = 22ns maximum.
Input Buffer + 1 NAND gate + Output Buffer (0, /0,B).

Figure 1.3 tpd3 –22ns Maximum

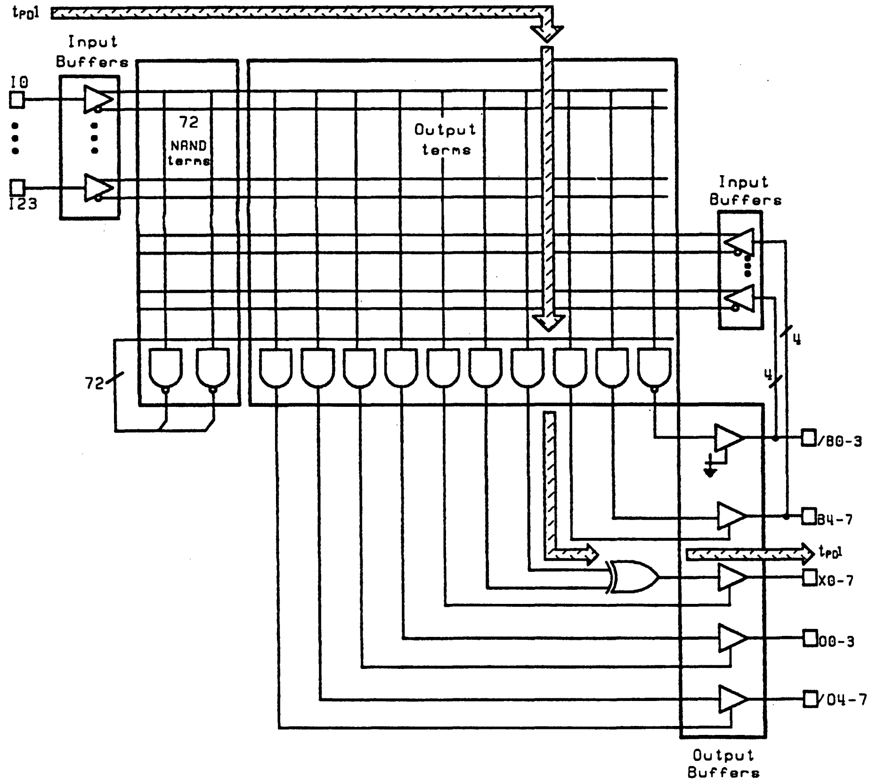
PLHS501 TIMING (Continued)



NOTES:
$t_{PD}4 = 30ns$ maximum.
Input Buffer + 2 NAND gate + XOR gate + Output Buffer.

Figure 1.4 $t_{PD}4$ –30ns Maximum

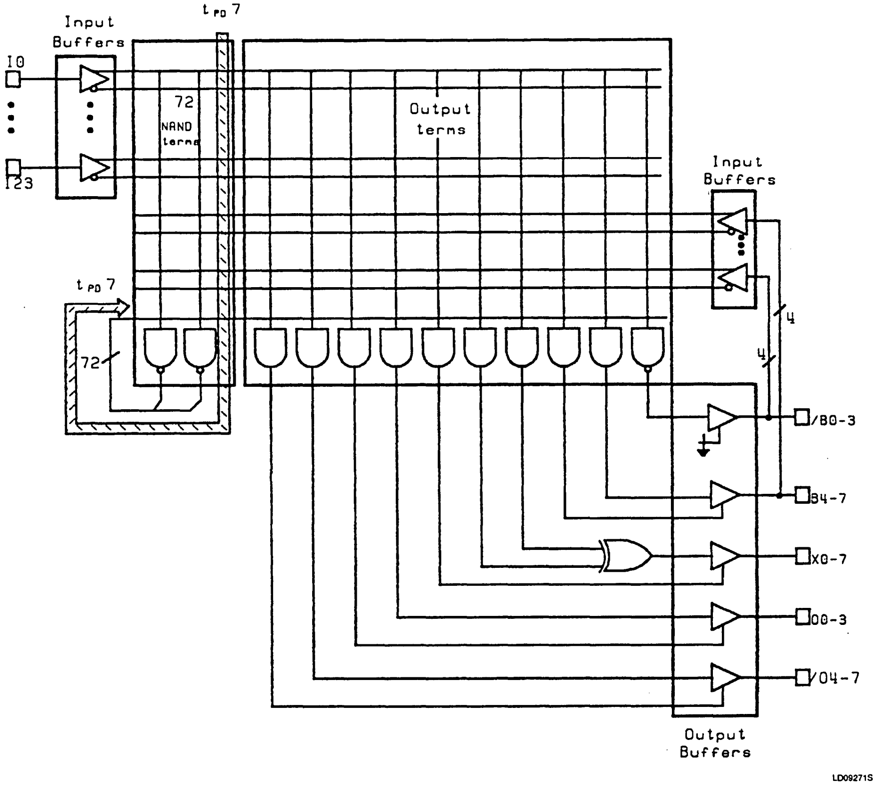
PLHS501 TIMING (Continued)



NOTES:
$t_{PD}1$ = 25ns maximum.
Input Buffer + 1 NAND gate + XOR gate + Output Buffer.

Figure 1.5 $t_{PD}1$ –25ns Maximum

PLHS501 TIMING INTERNAL



NOTE:
$t_{PD}7$ = 8ns maximum.

Figure 1.6 $t_{PD}7$ –8ns Maximum

NAND GATE FLIP-FLOPS

Various types of flip-flops and latches may be constructed using the NAND gate building blocks of the PLHS501. A typical 7474 type of edge-triggered D flip-flop requires 6 NAND gates as shown in Figure 1.7.

No additional gates are required to implement asynchronous set and reset functions to the flip-flop. The equations necessary for AMAZE to implement the D flip-flop are shown in Figure 1.8. However, please note that the equations of Figure 1.8 define a D flip-flop configured as a divide by 2 (i.e., QN is connected to the data input) whereas Figure 1.7 shows a general case. Also note that flip-flops with some additional features may be constructed without using more than the six NAND gates. This is possible because of the large number of inputs associated with each NAND gate. For instance, a flip- flop may be required to have a clock gated by one or more signals. Using the PLHS501, it may be implemented by adding additional input signal names to NAND gate equations of gates #2 and #3 of Figure 1.7. If the data input is to the AND of several signals, extra inputs to NAND gate #4 may be used. Or if additional set or reset lines are required, they may be added simply by using more of the inputs of each NAND gate connected to the main set or reset.

Figure 1.10 shows two simulations of the same flip-flop. The first one is at a little less than maximum frequency, for clarity in following the waveforms, and the second is at the maximum toggling frequency. For these simulations each NAND gate has a maximum tpHL or tpLH of 8nsec (which is the gate delay of a NAND gate in the PLHS501's foldback array). First of all, it can be seen from these simulations that for proper simulation or testing of such a device a set or reset input is mandatory. Both Q and QN outputs are unknown no matter what the inputs do, until they are put into a known state by either a set or reset input. Secondly, various timing parameters such as propagation delay, as well as setup and hold times may be determined. For the general case, referring to Figure 1.7:

Tsetup = tpd4 + tpd1, Thold = tpd3 + tpd4 and Clock to Q = tpd3 + tpd6 + tpd5.

Therefore, performance of the flip-flop depends a great deal on which gates in the PLHS501 are used, either NAND gates in the foldback array or output NAND gates, connected to bidirectional pins. As a test of the simulation, a D flip-flop connected as a divide by 2 was constructed using only the foldback NAND terms (see Figure 1.8). An output NAND term was used to invert the QN output and drive an output buffer. The only inputs were the clock and a reset. The data input to the flop was driven internally by the QN output. According to the simulation, it was possible to drive the clock at a frequency of 25Mhz and this small circuit also functioned at that frequency.

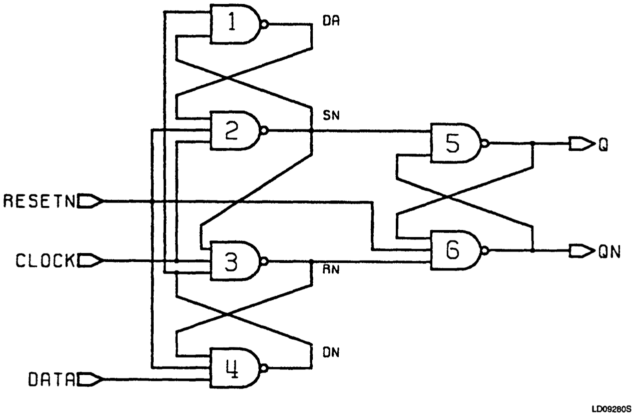
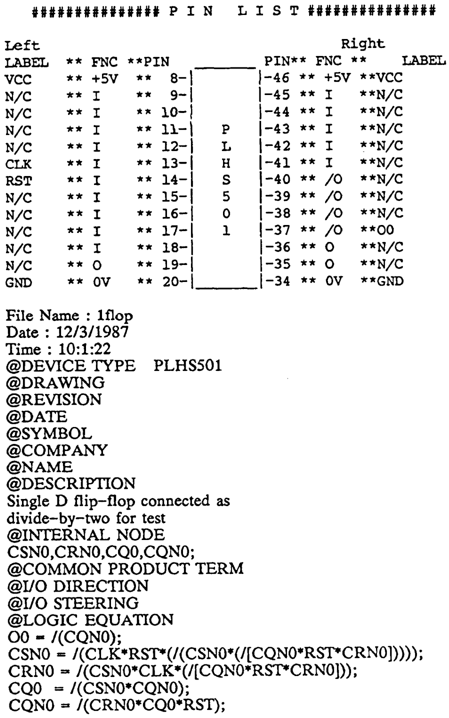


Figure 1.7 Edge Triggered D Flip-Flop



```
############### P I N   L I S T ###############

Left                                        Right
LABEL   ** FNC **PIN   _______  PIN** FNC **    LABEL
VCC     ** +5V  **  8-|       |-46 ** +5V **VCC
N/C     ** I    **  9-|       |-45 ** I   **N/C
N/C     ** I    ** 10-|       |-44 ** I   **N/C
N/C     ** I    ** 11-|   P   |-43 ** I   **N/C
N/C     ** I    ** 12-|   L   |-42 ** I   **N/C
CLK     ** I    ** 13-|   H   |-41 ** I   **N/C
RST     ** I    ** 14-|   S   |-40 ** /O  **N/C
N/C     ** I    ** 15-|   5   |-39 ** /O  **N/C
N/C     ** I    ** 16-|   0   |-38 ** /O  **N/C
N/C     ** I    ** 17-|   1   |-37 ** /O  **O0
N/C     ** I    ** 18-|       |-36 ** O   **N/C
N/C     ** O    ** 19-|       |-35 ** O   **N/C
GND     ** 0V   ** 20-|_______|-34 ** 0V  **GND

File Name : 1flop
Date : 12/3/1987
Time : 10:1:22
@DEVICE TYPE   PLHS501
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION
Single D flip-flop connected as
divide-by-two for test
@INTERNAL NODE
CSN0,CRN0,CQ0,CQN0;
@COMMON PRODUCT TERM
@I/O DIRECTION
@I/O STEERING
@LOGIC EQUATION
O0 = /(CQN0);
CSN0 = /(CLK*RST*(/(CSN0*(/[CQN0*RST*CRN0]))));
CRN0 = /(CSN0*CLK*(/[CQN0*RST*CRN0]));
 CQ0  = /(CSN0*CQN0);
CQN0 = /(CRN0*CQ0*RST);
```

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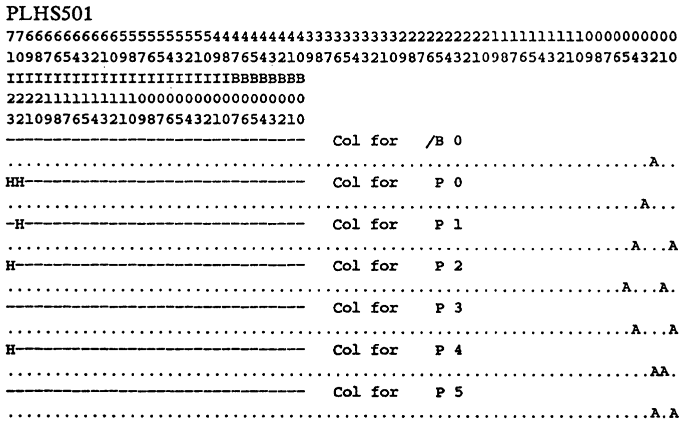
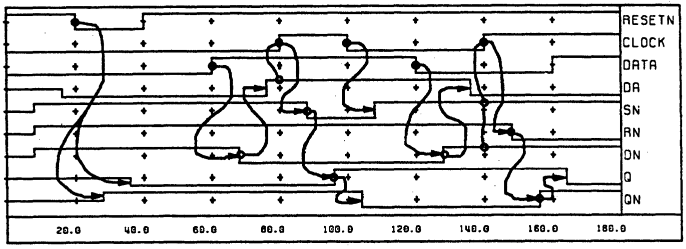
Figure 1.8 PLHS501 Test Flip-Flop



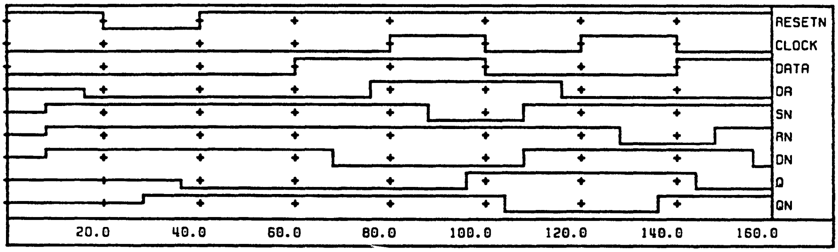
```
PLHS501
776666666666555555555544444444443333333333222222222211111111110000000000
109876543210987654321098765432109876543210987654321098765432109876543210
IIIIIIIIIIIIIIIIIIIIIIIIBBBBBBBB
22221111111111000000000000000000
32109876543210987654321076543210
--------------------------------   Col for   /B 0
.....................................................................A..
HH------------------------------   Col for    P 0
....................................................................A...
-H------------------------------   Col for    P 1
...................................................................A...A
H-------------------------------   Col for    P 2
..................................................................A...A.
--------------------------------   Col for    P 3
...................................................................A...A
H-------------------------------   Col for    P 4
.....................................................................AA.
--------------------------------   Col for    P 5
.....................................................................A.A
```

TB03640S

Figure 1.9 Partial PLHS501 Fusemap Showing Test Flip-Flop Fusing



WF23160S



WF23170S

Figure 1.10 Waveforms of Test Flip-Flop

Designing with Programmable Macro Logic

FUNCTIONAL FIT

In the late 1960's and early 1970's designers used SSI, MSI and small amounts of early LSI to generate logic solutions. Frustrated by the lack of wide input gates to accommodate a lot of product terms for two level solutions, they turned toward the budding ROM and PROM products. These devices relied on literally realizing a function by generating its truth table in silicon. The logic function had to have each logical one and zero realized distinctly as an entry for a particular combination of input variables, usually supplied on the address lines of the memory. Observing that many such truth tables were dense in ones or zeroes and sparse in the remainder, a cadre of initial manufacturers emerged with focus on supplying a programmable product with a few AND gates and OR gates which were versatile enough to compete against the ROM/PROM parts. The gimmick supplied by these PLA manufacturers was to illustrate the functional equivalency of the PLA to the PROM by comparing the number of product terms (to be shortened to "p-terms") the PLA supplied and comparing this to the width and depth of available PROMs. P-terms became the "currency" of the PLA world and a designer only had to assess the equivalent number of Boolean product terms required by his function to determine whether a particular PLA was a suitable candidate for his design.

Almost in parallel, gate arrays became available. These provided an array of identical, fixed input gates (usually two input NANDs or NORs). These were generated in a regular fashion on a substrate which had a fixed input/output pin arrangement. Also recognizing that all logic functions could be built from the appropriate two input gates, when interconnected correctly, manufacturers offered these devices to customers who required increased density. The designer's responsibility was to generate what would ultimately be a metal interconnect pattern of his design. Special tools were required to allow an untrained system designer to do this successfully. Flip-flops, decoders, registers, adders, etc., could all be generated from the low level gate building blocks.

The currency of gate arrays became known as gate equivalent functions. That is, with a limited number of available gates on a substrate, the user needed to know precisely how many gates were used up, on a function by function basis, to generate each piece of his design. A D flip-flop requires about six gates, a D latch four, a 3 to 8 decoder takes about 14 gates and so forth. This allowed estimation regarding whether the function could conceivably be fit onto a particular substrate or not. Manufacturers had to offer multiple foundations so that a designer could be assured that his design would result in a working I.C.

The classic method of estimating whether a logic function would fit into a PLA was to determine the number of I/O pads required and the number of product terms required to generate the logical function, then select the PLA. For a gate array, the required measure included the I/O pad arrangement but substituted the number of available gates to generate the logical function (usually by table lookup). In an attempt to reconcile the two measures, Hartman[4] has evolved a formula for his product line. A calculation using this method and developing an appropriate "exchange rate" is shown in Table 2.1 for the PLHS501 and PLHS502. An alternate method of generating an estimate is to consider the gate equivalent of generating, say for the PLHS501, a gate equivalent of the part in an optimistic functional configuration (72 occurrences of a 32 input NAND gate). Figure 2.1 shows how this will result in over 2000 equivalent gates. Conversely, by stacking the NAND gates into D flip-flops, its least efficient function, the PLHS501 will have a gate equivalent of only about 100 gates.

The most rational method of assessing fit is to isolate functions and identify the correct configuration in terms of gates, to allow direct tally of the gates used, to generate the proposed configuration. Table 2.2 may assist in doing this analysis. Note that all basic gates require precisely one gate to generate the function. Also note the occurrence of functions in the table which could never be generated as standard I.C.'s previously. The procedure is to tally the design against a total budget of 72 multiple input NAND gates.

Table 2.2 is illustrative only, and should by no means be taken as complete. It may be simply expanded by designing the proposed function with disregard to the usual restrictions on the number of inputs to a gate, realize the function as one, two, three, or more levels of interconnected logic and count the number of gate ocurrences required. Special software has been provided to allow pyramided logic structures to be generated under the designer's control. These structures may, however, be no deeper than 72 levels for the PLHS501. Functions should be generated in accord with the guidelines mentioned before, for selecting an optimal 2 level logical solution.

It is an interesting observation that manufacturers of gate arrays and standard cell products which offer embedded PROMS, ROMS or RAMS have not successfully described these embedded functions in terms of equivalent gates, but rather resort to other means (such as divulging their relative area with respect to the area of a basic gate). There is, as yet, no standard in this arena.

TABLE 2.1 EQUIVALENCY RATIO

Hartman's method is based on a CMOS gate array equivalency wherein 4 transistors constitute a 2 input NAND or NOR gate, equal to one gate. Thus, his "exchange rate" is as follows:

E.R. = 4 × # inputs
+9 × # FFs
+7 × # 3-State outputs
+(15 to 30) × # OR outputs from the AND/OR array.

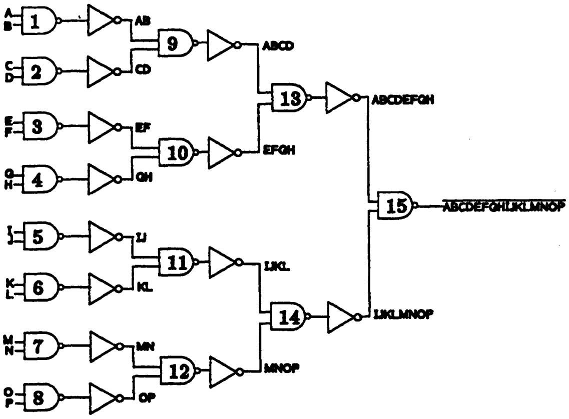
For the PLHS501: (using CMOS numbers which may be inappropriate)

E.R. = 4 × 32
+9 × 0
+7 × 24
+(15 to 30) × 50% of 72 feedbacks = 836 to 1376 gates

For the PLHS502:

E.R. = 4 × 32
+9 × 16
+7 × 12
+(15 to 30) × 50% of 64 feedback = 962 to 1502 gates

Being for two bipolar I.C.'s, in this case, the method may be inappropriate, but may be taken as an estimating procedure.



NOTE:
Double this and add one for a 32 input NAND.

Figure 2.1 16 Input NAND Formed from 2 Input Gates

TABLE 2.2 PLHS501 GATE COUNT EQUIVALENTS

FUNCTION	PLHS501 INTERNAL NAND EQUIVALENT	COMMENTS
Gates		
NANDs	1	For 1 to 32 input variables.
ANDs	1	For 1 to 32 input variables.
NORs	1	For 1 to 32 input variables.
ORs	1	For 1 to 32 input variables.
Decoders		
3 to 8	8	Inverted inputs available.
4 to 16	16	Inverted inputs available.
5 to 32	32	Inverted inputs available (24 chip outputs only).
Encoders		
8 to 3	15	Inverted inputs, 2 logic levels.
16 to 4	32	Inverted inputs, 2 logic levels.
32 to 5	41	Inverted inputs, 2 logic levels, factored solution.
Multiplexers		
4 to 1	5	Inverted inputs available.
8 to 1	9	
16 to 1	17	
27 to 1	28	Can address only 27 external inputs — more if internal.
Flip-Flops		
D-FF	6	With asynch S-R
T-FF	6	With asynch S-R
J-K-FF	8	With asynch S-R
Adders		
8-bit	45	Full carry look-ahead (four levels of logic)
Barrel Shifters		
8-bit	72	2 levels of logic

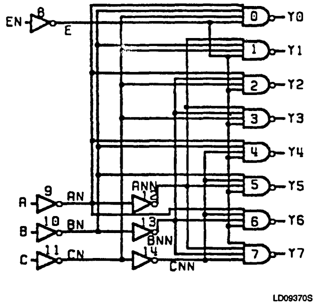
Designing with Programmable Macro Logic

DESIGN EXAMPLES

Most designers tend to view a PLD as a mechanism for collecting logical glue within a system. That is, those pieces which tie together the larger LSI microprocessors, controllers, RAMs, ROMs, UARTs, etc. However, there is a tendency of viewing a gate array as an entire system on a chip. PML based products will fit well in either casting as will be demonstrated by a series of small but straightforward examples. For starters, we shall examine how the fusing process embeds functions, progress to glue-like decoding operations and finally demonstrate some coprocessor like functions as well as homemade "standard products".

The method of associating gates within the NAND foldback structure is depicted in Figure 3.1 wherein a simple three to eight decoder is fused into the array. The corresponding inputs are on the left and outputs at the top. This figure shows inputs and their inverse formed in the array resulting in a solution that requires 6 inverting NANDs that would probably be best generated at the input receivers. Hence, this diagram could be trimmed by six gates, down to eight to achieve the function. Figure 3.2 shows two consecutive D-flip-flop fusing images. Note that asynchronous sets and resets may be achieved for free, in this version. In both Figures 3.1 and 3.2 the gates are numbered in a one-to-one arrangement. As well, the accompanying equations are in the format used by Signetics AMAZE design software. For clarity, consider the gate labeled 2A in Figure 3.1. Schematically, this is shown as a 3 input NAND. However, in the fused depiction, it combines from three intermediate output points with the dot intersect designation. Hence, all gates are drawn as single input NANDs whose inputs span the complete NAND gate foldback structure.

1 OF 8 DECODER/DEMULTIPLEXER



©LOGIC EQUATION

AN = /A;
BN = /B;
CN = /C;
ANN = /AN;
BNN = /BN;
CNN = /CN;
E = /EN;
Y0 = / (AN * BN * CN * E);
Y1 = / ANN * BN * CN * E);
Y2 = / AN * BNN * CN * E);
Y3 = / ANN * BNN * CN * E);
Y4 = / AN * BN * CNN * E);
Y5 = / ANN * BN * CNN * E);
Y6 = / AN * BNN * CNN * E);
Y7 = / ANN * BNN * CNN * E);

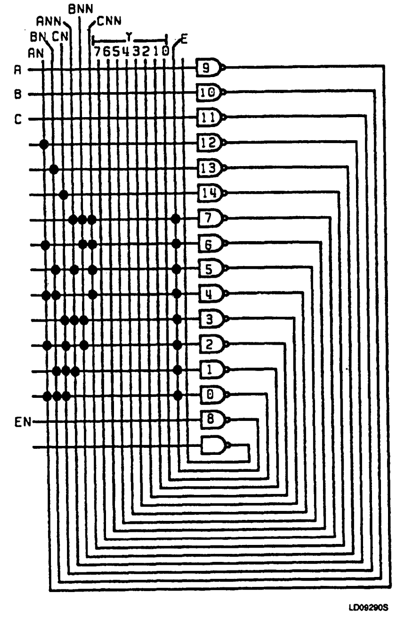
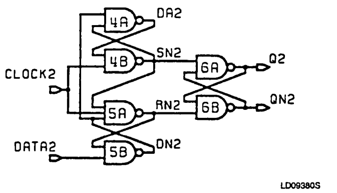
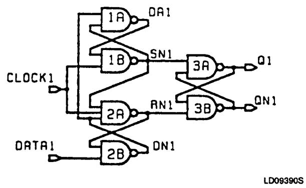


Figure 3.1 Decoder Implementation in NAND Foldback Structure

TWO EDGE-TRIGGERED FLIP-FLOPS





©LOGIC EQUATION

DA1 = / (DN1 • SN1);
SN1 = / (DA • CLOCK1)
RN1 = / (SN1 • CLOCK1 • DN1);
DN1 = / (DATA1 • RN1);
Q1 = / (SN1 • QN1);
QN1=/ (RN1 • Q1);

DA2 = / (DN2 • SN2);
SN2 = / (DA2 • CLOCK2)
RN2 = / (SN2 • CLOCK2 • DN2);
DN2 = / (DATA2 • RN2);
Q2 = / (SN2 • QN1);
QN2 = / (RN2 • Q2);

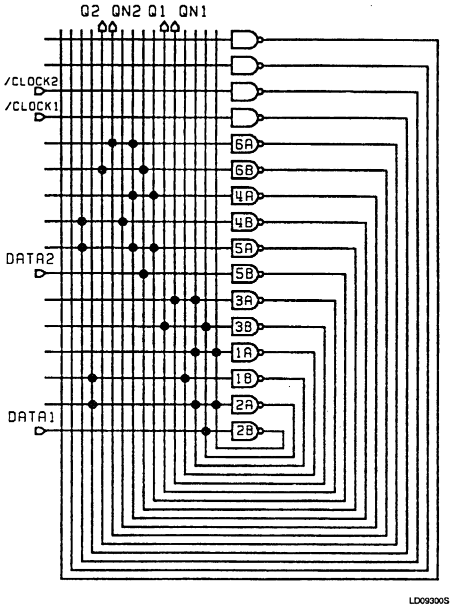


Figure 3.2 Two Flip-Flops Implemented in the NAND Foldback Structure

One straightforward example of using a PLHS501 is shown in Figure 3.3. Here, the device is configured to accept the 23 upper address lines generated by a 68000 microprocessor. By selecting the direct and complemented variables, at least 16 distinct address selections can be made using only the dedicated outputs. The designer can combine additional VME bus strobes, or other control signals to qualify the decode or, define 8 additional outputs for expanded selection. As well, the designer could transform the bidirectionals to inputs and decode over a 32 bit space, selecting combinations off of a 32 bit wide address bus. Because this simple level of design requires only NAND output terms plus 4 NAND gates in the foldback array (for inversion of signals connected to O3.O0), there may be as many as 68 remaining gates to accomplish additional handshaking or logical operations on the input variables.

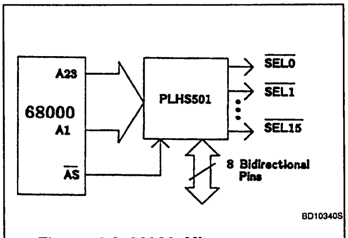


Figure 3.3 68000 Microprocessor Address Decode

Designing with Programmable Macro Logic

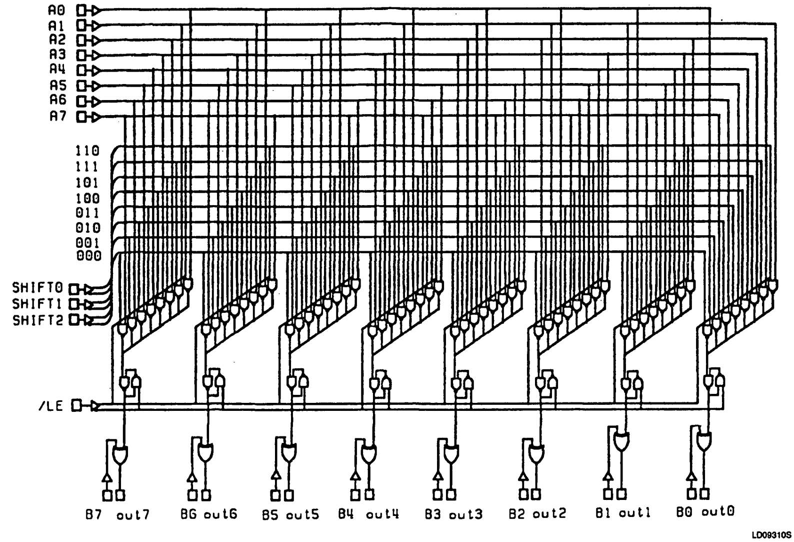


Figure 3.4 8-Bit Barrel Shifter Implemented with the PLHS501

An eight bit barrel shifter exploits most of the PLHS501 as depicted in Figure 3.4. This implementation utilizes all 72 internal foldback NANDs in a relatively brute force configuration as well as 8 output NANDs to generate transparent latched and shifted results. The shift position here is generated by the shift 0, shift 1 and shift 2 inputs which are distinguished and selected from the input cells. Variations on this idea of data manipulation could include direct passing data, mirror imaged data (bit reversal) or byte swapping to name a few.

Part of an eight bit, look-ahead parallel adder is shown in Figure 3.5. Gates necessary to form the level-0 generate and propagate, as well as the XOR output gates generating the resulting sum are not shown. The reader should be aware that this solution exploits four layers of pyramided gates and only utilizes a total of about 58 gates. Additional comparison or Boolean operations could still be generated with remaining NAND functions to achieve additional arithmetic operations. This application should make the reader aware of a new class of applications achieveable with third generation PLDs — user defineable I/O coprocessors. The approach of increasing microprocessor performance by designing dedicated task coprocessors is now within the grasp of user defineable single chip solutions.

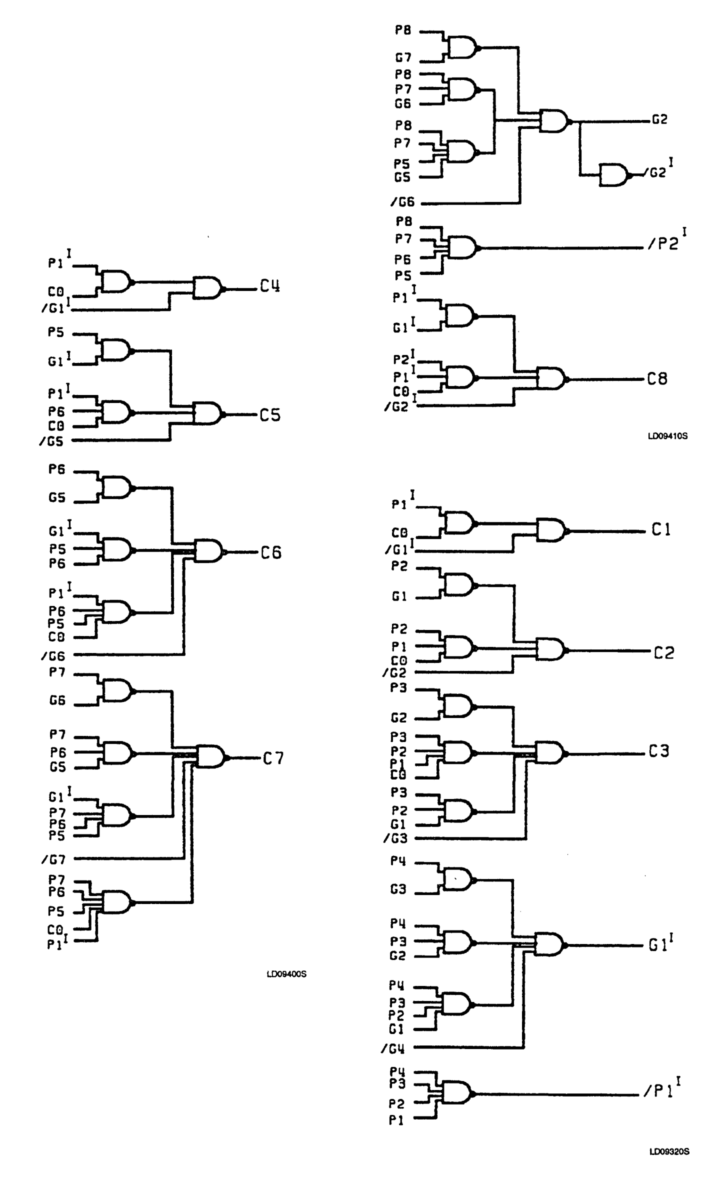


Figure 3.5 Partial NAND Gate Equivalence of the 8-Bit Look-Ahead Adder

An example of one of the least efficient structures realizeable on the PLHS501 is shown in Figure 3.6. Here, a cascade of 12 D-flip-flops are formed into a toggle chain that uses all available NAND gates in the main logic array. In the PLHS501 simple cross coupled latches or transparent D latches are preferred over edge triggered flip flops simply because they conserve NAND gates. Applications for structures like this include timing generators, rate multiplication, etc. Additional output gates exist on the output terms as shown in Figure 1.2, which could gate the output in multiple state detection configurations. As well, rearranging Figure 3.6 as a 12-bit shifter, picking off states at the output terms could result in a general purpose sequence recognizer capable of recognizing binary string sequences. These strings could be up to 13 bits long (in a Mealy configuration) and 24 distinct sequences could be sensed and detected.

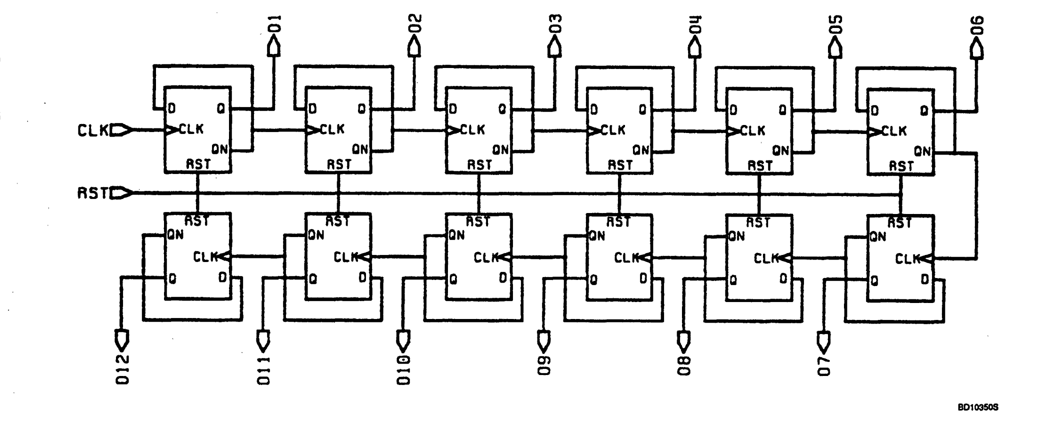


Figure 3.6 12-Bit Ripple Counter

Figure 3.7 shows a 32 to 5-bit priority encoder. This sort of device could generate encoded vector interrupts for 32 contending devices. Of particular interest is the fact that ordinary encoders are not this wide. The designer is, of course, not constrained to generating combinational functions in even powers of two. Thus, the PLHS501 can easily perform customized functions like a 5 to 27 decoder or a 14 to 4 encoder or, even an 18 to 7 multiplexor. For the sake of optimization, the designer is encouraged to implement precisely the function he needs, no more and no less!

The design examples given are illustrative of some typical operations used in ordinary systems. In each case, the example could be thought of as simply an "off the shelf" standard solution to an every day problem (i.e., a de facto standard product).

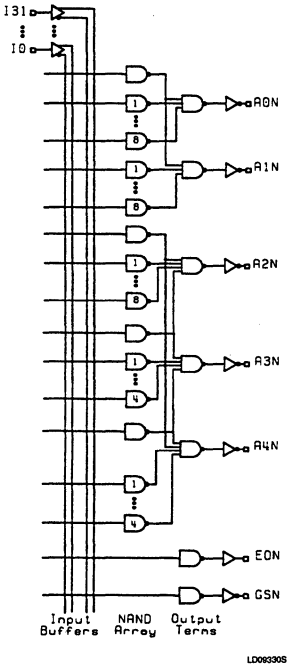


Figure 3.7 Encoder

Designing with Programmable Macro Logic

SUCCESSOR ARCHITECTURES

The design examples described and Table 2.2 illustrate the combinational power and the sequential limitations of the PLHS501 – Signetics first PML entry. Clearly, the next family members must address the flip-flop issue, and they do. The PLHS502 (Figure 4.1) shows a similar NAND function array of 64 gates with the vital addition of 8 buried D-flip-flops and 8 buried S – R flip-flops. Again, 16 pins are devoted to dedicated outputs, 20 straight inputs, 4 clock or general inputs and 8 bidirectionals can be configured to expand input or output capabilities. Slated to operate in the middle 30MHz clocking range, this part greatly expands the sequencer capability beyond the initial PLHS501. The PLHS502 application range will include state machines like CRC generation/detection, Bus handshakers, LAN handshaking, arithmetic coprocessors, single chip systems and a complete bevy of general sequencer operations such as sequence generation and detection. It should be emphasized that the NAND array is fully connected and circumvents limitations on connectivity as found in other PLD products.

Almost simultaneous with the arrival of the PLHS502 (a bipolar part) will be the first CMOS PML entry. Expanding on the functional capabilities of the PLHS502, the CMOS part will offer 52 flip-flops in a variety of natural configurations with a NAND array near 200 gates. Due to complexity and density, the part will combine a distinctive power-save option and the benefits of scan-design.

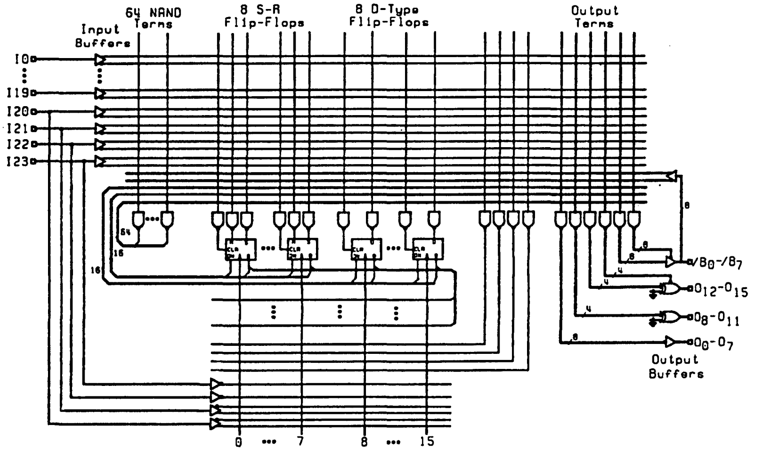


Figure 4.1 PLHS502 Diagram

SUPPORT ISSUES

The current PML architecture, the PLHS501, is adequately supported by Signetics AMAZE software. Offered free to qualified users, AMAZE can generate the required design files, fusemaps and simulations within the appropriate modules of AMAZE. From a simple menu driven environment on an IBM personal computer (or compatible under MS/DOS), the user can generate a design with logic equations, state equations or schematic entry (using FutureNet Dash or ORCAD SDT software). Once the design is entered, the user must "assemble" it prior to fusing the PML product. If required, the user may simulate the assembled file to determine the accuracy and functional operation of his design. Iteration between design entry, assembly and simulation may be required, depending on the users expectations and the completeness of design. Automatic test vector generation is a simulation option. Currently, the designer may fuse his design using either a DATA I/O Unisite programmer, a Stag ZL-30A or a STREBOR fusing system with corresponding configuration modules.

The AMAZE product is fully contained and complete except for the schematic capture program. Although it is used for the complete line of Signetics PLD products (PLAs, Sequencers and PROMs), it has undergone additional modification to support special features required by the nature of the PML products. These include the following:

- **Internal Nodes** — the ability to define and refer to nodes completely within the array and isolated from direct contact with the device I/O pins.
- **Bracket Freezing** — the ability to tag (with square brackets) a Boolean subfunction which is not to be optimized by the AMAZE assembler but is to be realized within the design explicitly as described by equation.

Both features are key to the AMAZE approach to macro generation. In particular, "bracket freezing" allows the designer to make tradeoffs between wide and shallow combinational paths and long, narrow combinational paths.

In the current rendition of AMAZE, automatic placement and interconnect of the fused Boolean functions is the recommended approach. Should the user decide to intervene, a special fuse table editor exists for manual alteration of the design file. This is not the recommended approach, but it also serves as a diagnostic tool to review design placement and interconnect.

Future directions for software support include enhanced simulation, exhaustive automatic Boolean optimization, the development of a full library of macros, automatic design partitioning and a wide assortment of bells and whistles.

PLHS501 EXAMPLES USING AMAZE REVISION 1.6

- **Simple gate implementations**
- **8-bit barrel shifter**
- **12-bit comparator with dual 1 of 8 decoders**
- **8-bit carry look-ahead adder**
- **32 to 5 priority encoder**
- **8-bit shift register with 3-bit counter and sequence detector**
- **4-bit synchronous counter**

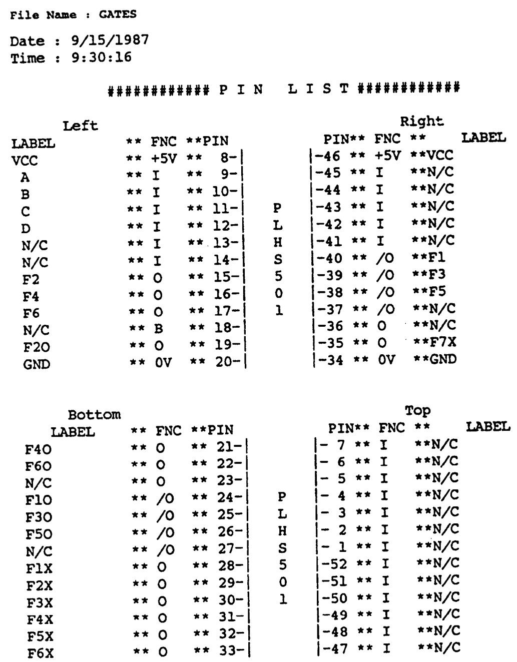
Following are six example applications for the PLHS501 using AMAZE Rev. 1.6. They should not be viewed as showing all possible capabilities of the device. They have been designed to demonstrate some of the PLHS501 features, syntax of AMAZE, and to give the reader some ideas for possible circuit implementations.

Note that these examples were written using AMAZE Rev. 1.6. Although Signetics will try to keep succeeding versions of AMAZE compatible, it may be necessary to change some syntax rules. Therefore, please refer to your AMAZE manual for any notes on differences, if using a revision later than Rev. 1.6.

SIMPLE GATE IMPLEMENTATIONS

In this example six functions were implemented for each of the three major types of output structures. The six functions are AND/OR, AOI, NAND, AND, OR and NOR. A requirement for the AND/OR and AOI gates was to use only two gates each from the foldback array and to combine these product terms in one NAND output gate. To achieve this result, it was necessary for the /B and /O outputs to write equations using internal nodes and brackets around the equation. Refer to Figures 6.1 and 6.2.

For the simulation (Figures 6.3 and 6.4) a binary count of 0 through 15 hex was applied to the input D-A. Each output of the log file was checked against anticipated and other device outputs of the same function for correct operation.



```
File Name : GATES

Date : 9/15/1987
Time : 9:30:16

            ############ P I N   L I S T ############

     Left                                           Right
LABEL          ** FNC **PIN               PIN** FNC **     LABEL
VCC            ** +5V **  8-|           |-46 ** +5V **VCC
 A             ** I   **  9-|           |-45 ** I   **N/C
 B             ** I   ** 10-|           |-44 ** I   **N/C
 C             ** I   ** 11-|     P     |-43 ** I   **N/C
 D             ** I   ** 12-|     L     |-42 ** I   **N/C
 N/C           ** I   ** 13-|     H     |-41 ** I   **N/C
 N/C           ** I   ** 14-|     S     |-40 ** /O  **F1
 F2            ** O   ** 15-|     5     |-39 ** /O  **F3
 F4            ** O   ** 16-|     0     |-38 ** /O  **F5
 F6            ** O   ** 17-|     1     |-37 ** /O  **N/C
 N/C           ** B   ** 18-|           |-36 ** O   **N/C
 F2O           ** O   ** 19-|           |-35 ** O   **F7X
 GND           ** OV  ** 20-|           |-34 ** OV  **GND


      Bottom                                        Top
    LABEL      ** FNC **PIN               PIN** FNC **     LABEL
 F4O           ** O   ** 21-|           |- 7 ** I   **N/C
 F6O           ** O   ** 22-|           |- 6 ** I   **N/C
 N/C           ** O   ** 23-|           |- 5 ** I   **N/C
 F1O           ** /O  ** 24-|     P     |- 4 ** I   **N/C
 F3O           ** /O  ** 25-|     L     |- 3 ** I   **N/C
 F5O           ** /O  ** 26-|     H     |- 2 ** I   **N/C
 N/C           ** /O  ** 27-|     S     |- 1 ** I   **N/C
 F1X           ** O   ** 28-|     5     |-52 ** I   **N/C
 F2X           ** O   ** 29-|     0     |-51 ** I   **N/C
 F3X           ** O   ** 30-|     1     |-50 ** I   **N/C
 F4X           ** O   ** 31-|           |-49 ** I   **N/C
 F5X           ** O   ** 32-|           |-48 ** I   **N/C
 F6X           ** O   ** 33-|           |-47 ** I   **N/C
```

TB03650S

Figure 6.1 Gates Pin List

```
File Name : GATES
Date : 9/15/1987
Time : 9:30:35

@DEVICE TYPE
PLHS501
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION

Various single and two level gate implementations using
different output structures

@INTERNAL NODE
@COMMON PRODUCT TERM
@I/O DIRECTION
@I/O STEERING
@LOGIC EQUATION

"AND-OR using /B output"
f1 = /(/[a*b] * /[c*d]) ;
"AND-OR-INVERT using B output"
f2 = /[(a*b) + (c*d)];
"NAND using /B output"
f3 = /(a*b*c*d);
"AND using B output"
f4 = a*b*c*d;
"OR using /B output"
f5 = /(/a*/b*/c*/d);
"NOR using B output"
f6 = /a*/b*/c*/d;
```

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```
"AND-OR using XOR output"
f1x = (a*b)+(c*d);
"AND-OR-INVERT using XOR output"
f2x = /[(a*b) + (c*d)];
"NAND using XOR output"
f3x = /(a*b*c*d);
"AND using XOR output"
f4x = a*b*c*d;
"OR using XOR output"
f5x = /(/a*/b*/c*/d);
"NOR using XOR output"
f6x = /a*/b*/c*/d;
"XOR using XOR output"
f7x : xr1 = a;
      xr2 = b;

"AND-OR using /O output"
f1o = /(/[a*b] * /[c*d]) ;
"AND-OR-INVERT using O output"
f2o = /[(a*b) + (c*d)];
"NAND using /O output"
f3o = /(a*b*c*d);
"AND using O output"
f4o = a*b*c*d;
"OR using /O output"
f5o = /(/a*/b*/c*/d);
"NOR using O output"
f6o = /a*/b*/c*/d;
```

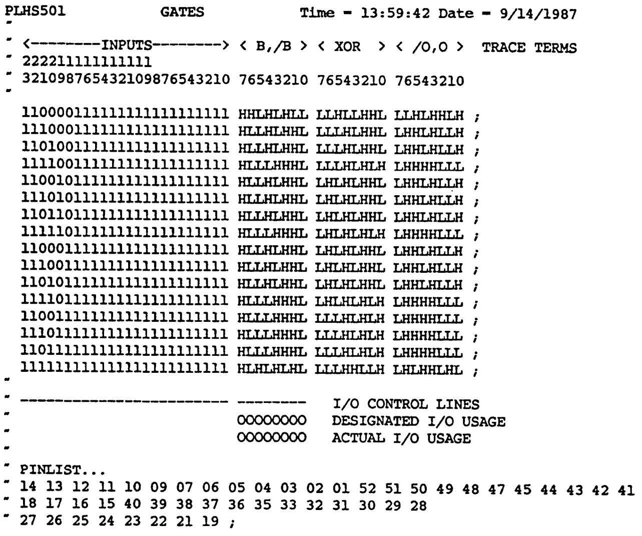
TB03670S

Figure 6.2 Gates Boolean Equations

```
" Simulation input file for GATES
"
" <--------INPUTS--------> < B,/B >
" 222211111111111
" 321098765432109876543210 76543210
"
"   DCBA   A is MSB, D is LSB
"
  HHLLLLHHHHHHHHHHHHHHHHHH -------- "Input all 0's A-D"
  HHHLLLHHHHHHHHHHHHHHHHHH -------- "Input count 1"
  HHLHLLHHHHHHHHHHHHHHHHHH -------- "Through...
  HHHHLLHHHHHHHHHHHHHHHHHH --------
  HHLLHLHHHHHHHHHHHHHHHHHH --------
  HHHLHLHHHHHHHHHHHHHHHHHH --------
  HHLHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHLLLHHHHHHHHHHHHHHHHHHH --------
  HHHLLHHHHHHHHHHHHHHHHHHH --------
  HHLHLHHHHHHHHHHHHHHHHHHH --------
  HHHHLHHHHHHHHHHHHHHHHHHH --------
  HHLLHHHHHHHHHHHHHHHHHHHH --------
  HHHLHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "Count 15 hex"
QUIT
```

TB03680S

Figure 6.3 Gates Simulation Input File



```
PLHS501            GATES            Time - 13:59:42 Date - 9/14/1987
"
" <--------INPUTS--------> < B,/B > < XOR  > < /O,O >  TRACE TERMS
" 22221111111111
" 321098765432109876543210 76543210 76543210 76543210
"
  110000111111111111111111 HHLHLHLL LLHLLHHL LLHLHHLH ;
  111000111111111111111111 HLLHLHHL LLLHLHHL LHHLHLLH ;
  110100111111111111111111 HLLHLHHL LLLHLHHL LHHLHLLH ;
  111100111111111111111111 HLLLHHHL LLLHLHLH LHHHHLLL ;
  110010111111111111111111 HLLHLHHL LHLHLHHL LHHLHLLH ;
  111010111111111111111111 HLLHLHHL LHLHLHHL LHHLHLLH ;
  110110111111111111111111 HLLHLHHL LHLHLHHL LHHLHLLH ;
  111110111111111111111111 HLLLHHHL LHLHLHLH LHHHHLLL ;
  110001111111111111111111 HLLHLHHL LHLHLHHL LHHLHLLH ;
  111001111111111111111111 HLLHLHHL LHLHLHHL LHHLHLLH ;
  110101111111111111111111 HLLHLHHL LHLHLHHL LHHLHLLH ;
  111101111111111111111111 HLLLHHHL LHLHLHLH LHHHHLLL ;
  110011111111111111111111 HLLLHHHL LLLHLHLH LHHHHLLL ;
  111011111111111111111111 HLLLHHHL LLLHLHLH LHHHHLLL ;
  110111111111111111111111 HLLLHHHL LLLHLHLH LHHHHLLL ;
  111111111111111111111111 HLHLHLHL LLLHHLLH LHLHHLHL ;
"
" ------------------------ --------   I/O CONTROL LINES
"                          00000000   DESIGNATED I/O USAGE
"                          00000000   ACTUAL I/O USAGE
"
" PINLIST...
" 14 13 12 11 10 09 07 06 05 04 03 02 01 52 51 50 49 48 47 45 44 43 42 41
" 18 17 16 15 40 39 38 37 36 35 33 32 31 30 29 28
" 27 26 25 24 23 22 21 19 ;
```

TB03690S

Figure 6.4 Gates Simulation Log File

8 BIT BARREL SHIFTER

This 8-bit shifter will shift to the right, data applied to A7 – A0 with the result appearing on OUT7 – OUT0. Data may be shifted by 1 to 7 places by indicating the desired binary count on pins SHIFT2 – SHIFT0. Data applied to the OUT0 position for a shift of 1. For a shift of 0, A7 will appear on OUT7.

Also included is a transparent latch for the output bits. The input 'COMPLMTO' will invert all output bits simultaneously and input /OE will 3-State all outputs.

```
File Name : BRLSHFT
Date : 9/15/1987
Time : 9:31:58

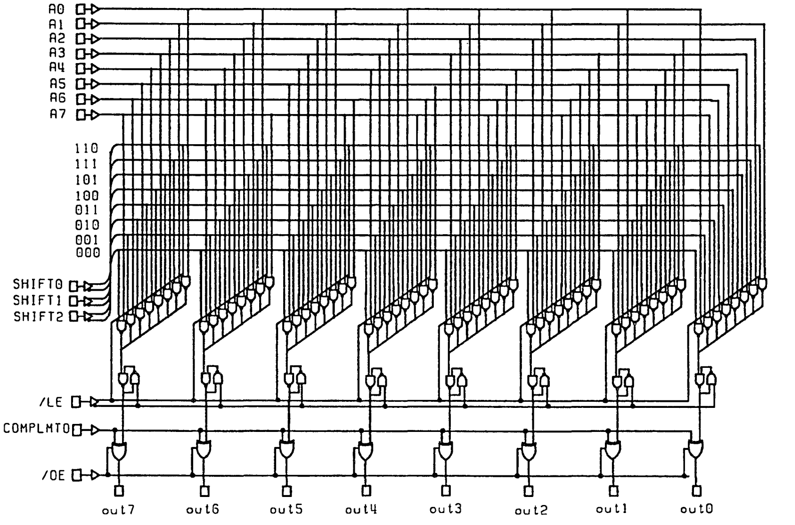
##################### P I N   L I S T #####################

         Left                                      Right
   LABEL      ** FNC **PIN             PIN** FNC **    LABEL
VCC           ** +5V **  8-|          |-46 ** +5V **VCC
A2            ** I   **  9-|          |-45 ** I   **N/C
A3            ** I   ** 10-|          |-44 ** I   **N/C
A4            ** I   ** 11-|   P      |-43 ** I   **N/C
A5            ** I   ** 12-|   L      |-42 ** I   **N/C
A6            ** I   ** 13-|   H      |-41 ** I   **N/C
A7            ** I   ** 14-|   S      |-40 ** /O  **L0
L4            ** O   ** 15-|   5      |-39 ** /O  **L1
L5            ** O   ** 16-|   0      |-38 ** /O  **L2
L6            ** O   ** 17-|   1      |-37 ** /O  **L3
L7            ** O   ** 18-|          |-36 ** O   **OUT7
N/C           ** O   ** 19-|          |-35 ** O   **OUT6
GND           ** 0V  ** 20-|          |-34 ** 0V  **GND


         Bottom                                    Top
   LABEL      ** FNC **PIN             PIN** FNC **    LABEL
N/C           ** O   ** 21-|          |- 7 ** I   **A1
N/C           ** O   ** 22-|          |- 6 ** I   **A0
N/C           ** O   ** 23-|          |- 5 ** I   **SHIFT2
N/C           ** /O  ** 24-|   P      |- 4 ** I   **SHIFT1
N/C           ** /O  ** 25-|   L      |- 3 ** I   **SHIFT0
N/C           ** /O  ** 26-|   H      |- 2 ** I   **COMPLMTO
N/C           ** /O  ** 27-|   S      |- 1 ** I   **/LE
OUT0          ** O   ** 28-|   5      |-52 ** I   **/OE
OUT1          ** O   ** 29-|   0      |-51 ** I   **N/C
OUT2          ** O   ** 30-|   1      |-50 ** I   **N/C
OUT3          ** O   ** 31-|          |-49 ** I   **N/C
OUT4          ** O   ** 32-|          |-48 ** I   **N/C
OUT5          ** O   ** 33-|          |-47 ** I   **N/C
```

TB03700S

Figure 6.5 Barrel Shifter Pin List



LD09360S

Figure 6.6 8-Bit Barrel Shifter Schematic

```
File Name : BRLSHFT
Date : 9/15/1987
Time : 9:32:14

@DEVICE TYPE
PLHS501
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION

8 Bit Barrel Shifter
with 3-state latched outputs

@INTERNAL NODE
nod1,nod2,nod3,nod4,nod5,nod6,nod7,nod8;
nod9,nod10,nod11,nod12,nod13,nod14,nod15,nod16;
nod17,nod18,nod19,nod20,nod21,nod22,nod23,nod24;
nod25,nod26,nod27,nod28,nod29,nod30,nod31,nod32;
i3,i2,i1,i0;
@COMMON PRODUCT TERM
rot0 = /shift2 * /shift1 * /shift0;
rot1 = /shift2 * /shift1 *  shift0;
rot2 = /shift2 *  shift1 * /shift0;
rot3 = /shift2 *  shift1 *  shift0;
rot4 =  shift2 * /shift1 * /shift0;
rot5 =  shift2 * /shift1 *  shift0;
rot6 =  shift2 *  shift1 * /shift0;
rot7 =  shift2 *  shift1 *  shift0;
@I/O DIRECTION
xe0 = oe;
xe1 = oe;
xe2 = oe;
xe3 = oe;
@I/O STEERING
@LOGIC EQUATION

17 = /[a7 * rot0 * /le +
       a6 * rot1 * /le +
       a5 * rot2 * /le +
       a4 * rot3 * /le +
       a3 * rot4 * /le +
       a2 * rot5 * /le +
       a1 * rot6 * /le +
```

TB03710S

Figure 6.7 Barrel Shifter Boolean Equations

```
         a0 * rot7 * /le +
         le * /l7];

  l6 = /[a6 * rot0 * /le +
         a5 * rot1 * /le +
         a4 * rot2 * /le +
         a3 * rot3 * /le +
         a2 * rot4 * /le +
         a1 * rot5 * /le +
         a0 * rot6 * /le +
         a7 * rot7 * /le +
         le * /l6];

  l5 = /[a5 * rot0 * /le +
         a4 * rot1 * /le +
         a3 * rot2 * /le +
         a2 * rot3 * /le +
         a1 * rot4 * /le +
         a0 * rot5 * /le +
         a7 * rot6 * /le +
         a6 * rot7 * /le +
         le * /l5];

  l4 = /[a4 * rot0 * /le +
         a3 * rot1 * /le +
         a2 * rot2 * /le +
         a1 * rot3 * /le +
         a0 * rot4 * /le +
         a7 * rot5 * /le +
         a6 * rot6 * /le +
         a5 * rot7 * /le +
         le * /l4];

  nod1 = [a3 * rot0 * /le];
  nod2 = [a2 * rot1 * /le];
  nod3 = [a1 * rot2 * /le];
  nod4 = [a0 * rot3 * /le];
  nod5 = [a7 * rot4 * /le];
  nod6 = [a6 * rot5 * /le];
  nod7 = [a5 * rot6 * /le];
  nod8 = [a4 * rot7 * /le];
  i3 = [le * l3];

  l3 = /([/nod1*/nod2*/nod3*/nod4*/nod5*/nod6*/nod7*/nod8*/i3]);

nod9 = [a2 * rot0 * /le];
nod10= [a1 * rot1 * /le];
```

TB03720S

Figure 6.7 Barrel Shifter Boolean Equations (Continued)

```
       nod11= [a0 * rot2 * /le];
       nod12= [a7 * rot3 * /le];
       nod13= [a6 * rot4 * /le];
       nod14= [a5 * rot5 * /le];
       nod15= [a4 .* rot6 * /le];
       nod16= [a3 * rot7 * /le];
       i2 = [le * l2];

l2 = /([/nod9*/nod10*/nod11*/nod12*/nod13*/nod14*/nod15*/nod16*/i2]);

       nod17= [a1 * rot0 * /le];
       nod18= [a0 * rot1 * /le];
       nod19= [a7 * rot2 * /le];
       nod20= [a6 * rot3 * /le];
       nod21= [a5 * rot4 * /le];
       nod22= [a4 * rot5 * /le];
       nod23= [a3 * rot6 * /le];
       nod24= [a2 * rot7 * /le];
       i1 = [le * l1];

l1 = /([/nod17*/nod18*/nod19*/nod20*/nod21*/nod22*/nod23*/nod24*/i1]);

       nod25= [a0 * rot0 * /le];
       nod26= [a7 * rot1 * /le];
       nod27= [a6 * rot2 * /le];
       nod28= [a5 * rot3 * /le];
       nod29= [a4 * rot4 * /le];
       nod30= [a3 * rot5 * /le];
       nod31= [a2 * rot6 * /le];
       nod32= [a1 * rot7 * /le];
       i0 = [le * l0];

l0 = /([/nod25*/nod26*/nod27*/nod28*/nod29*/nod30*/nod31*/nod32*/i0]);

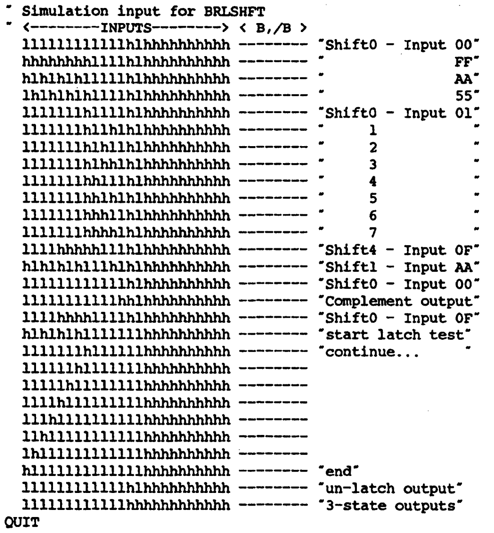
       out7 : xr1 = /l7;
              xr2 = complmto;
       out6 : xr1 = /l6;
              xr2 = complmto;
       out5 : xr1 = /l5;
              xr2 = complmto;
       out4 : xr1 = /l4;
              xr2 = complmto;
       out3 : xr1 = l3;
              xr2 = complmto;
       out2 : xr1 = l2;
              xr2 = complmto;
       out1 : xr1 = l1;
```

TB03730S

```
       xr2 = complmto;
out0 : xr1 = l0;
       xr2 = complmto;
```

TB03740S

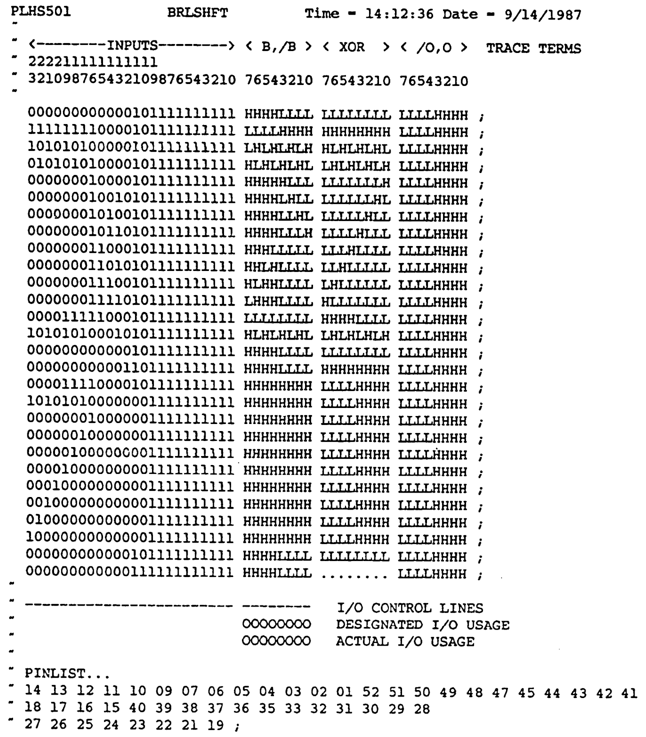
Figure 6.7 Barrel Shifter Boolean Equations (Continued)



```
" Simulation input for BRLSHFT
" <--------INPUTS--------> < B,/B >
  llllllllllllhlhhhhhhhhhh -------- "Shift0 - Input 00"
  hhhhhhhhllllhlhhhhhhhhhh -------- "               FF"
  hlhlhlhlllllhlhhhhhhhhhh -------- "               AA"
  lhlhlhlhllllhlhhhhhhhhhh -------- "               55"
  lllllllhllllhlhhhhhhhhhh -------- "Shift0 - Input 01"
  lllllllhllhlhlhhhhhhhhhh -------- "     1           "
  lllllllhlhllhlhhhhhhhhhh -------- "     2           "
  lllllllhlhhlhlhhhhhhhhhh -------- "     3           "
  lllllllhhlllhlhhhhhhhhhh -------- "     4           "
  lllllllhhlhlhlhhhhhhhhhh -------- "     5           "
  lllllllhhhllhlhhhhhhhhhh -------- "     6           "
  lllllllhhhhlhlhhhhhhhhhh -------- "     7           "
  llllhhhhhlllhlhhhhhhhhhh -------- "Shift4 - Input 0F"
  hlhlhlhlllhlhlhhhhhhhhhh -------- "Shift1 - Input AA"
  llllllllllllhlhhhhhhhhhh -------- "Shift0 - Input 00"
  lllllllllllhhlhhhhhhhhhh -------- "Complement output"
  llllhhhhllllhlhhhhhhhhhh -------- "Shift0 - Input 0F"
  hlhlhlhlllllllhhhhhhhhhh -------- "start latch test"
  lllllllhllllllhhhhhhhhhh -------- "continue...     "
  llllllhlllllllhhhhhhhhhh --------
  lllllhllllllllhhhhhhhhhh --------
  llllhlllllllllhhhhhhhhhh --------
  lllhllllllllllhhhhhhhhhh --------
  llhlllllllllllhhhhhhhhhh --------
  lhllllllllllllhhhhhhhhhh --------
  hlllllllllllllhhhhhhhhhh -------- "end"
  llllllllllllhlhhhhhhhhhh -------- "un-latch output"
  llllllllllllhhhhhhhhhhhh -------- "3-state outputs"
QUIT
```

TB03750S

Figure 6.8 Barrel Shifter Simulation Input File



```
PLHS501            BRLSHFT         Time - 14:12:36 Date - 9/14/1987
"
" <--------INPUTS--------> < B,/B > < XOR  > < /O,O >  TRACE TERMS
" 2222111111111111
" 321098765432109876543210 76543210 76543210 76543210
"
  000000000000101111111111 HHHHLLLL LLLLLLLL LLLLHHHH ;
  111111110000101111111111 LLLLHHHH HHHHHHHH LLLLHHHH ;
  101010100000101111111111 LHLHLHLH HLHLHLHL LLLLHHHH ;
  010101010000101111111111 HLHLHLHL LHLHLHLH LLLLHHHH ;
  000000010000101111111111 HHHHHLLL LLLLLLLH LLLLHHHH ;
  000000010010101111111111 HHHHLHLL LLLLLLHL LLLLHHHH ;
  000000010100101111111111 HHHHLLHL LLLLLHLL LLLLHHHH ;
  000000010110101111111111 HHHHLLLH LLLLHLLL LLLLHHHH ;
  000000011000101111111111 HHHLLLLL LLLHLLLL LLLLHHHH ;
  000000011010101111111111 HHLHLLLL LLHLLLLL LLLLHHHH ;
  000000011100101111111111 HLHHLLLL LHLLLLLL LLLLHHHH ;
  000000011110101111111111 LHHHLLLL HLLLLLLL LLLLHHHH ;
  000011111000101111111111 LLLLLLLL HHHHLLLL LLLLHHHH ;
  101010100010101111111111 HLHLHLHL LHLHLHLH LLLLHHHH ;
  000000000000101111111111 HHHHLLLL LLLLLLLL LLLLHHHH ;
  000000000001101111111111 HHHHLLLL HHHHHHHH LLLLHHHH ;
  000011110000101111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  101010100000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  000000010000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  000000100000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  000001000000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  000010000000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  000100000000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  001000000000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  010000000000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  100000000000001111111111 HHHHHHHH LLLLHHHH LLLLHHHH ;
  000000000000101111111111 HHHHLLLL LLLLLLLL LLLLHHHH ;
  000000000000111111111111 HHHHLLLL ........ LLLLHHHH ;
"
" ------------------------ --------   I/O CONTROL LINES
"                          00000000   DESIGNATED I/O USAGE
"                          00000000   ACTUAL I/O USAGE
"
" PINLIST...
" 14 13 12 11 10 09 07 06 05 04 03 02 01 52 51 50 49 48 47 45 44 43 42 41
" 18 17 16 15 40 39 38 37 36 35 33 32 31 30 29 28
" 27 26 25 24 23 22 21 19 ;
```

TB03760S

Figure 6.9 Barrel Shifter Simulation Log File

```
File Name : 12BITCMP
Date : 9/15/1987
Time : 9:36:0

###################### P I N   L I S T ######################

         Left                                     Right
   LABEL        ** FNC **PIN            PIN** FNC **     LABEL
VCC             ** +5V **  8-|          |-46 ** +5V **VCC
B6              ** I   **  9-|          |-45 ** I   **A4
B7              ** I   ** 10-|          |-44 ** I   **A3
B8              ** I   ** 11-|    P     |-43 ** I   **A2
B9              ** I   ** 12-|    L     |-42 ** I   **A1
B10             ** I   ** 13-|    H     |-41 ** I   **A0
B11             ** I   ** 14-|    S     |-40 ** /O  **CMPOUT
ENCOMP          ** I   ** 15-|    5     |-39 ** I   **DA2
DCDREN          ** I   ** 16-|    0     |-38 ** I   **DA1
RW              ** I   ** 17-|    1     |-37 ** I   **DA0
N/C             ** B   ** 18-|          |-36 ** O   **R7
W0              ** O   ** 19-|          |-35 ** O   **R6
GND             ** 0V  ** 20-|          |-34 ** 0V  **GND


         Bottom                                   Top
   LABEL        ** FNC **PIN            PIN** FNC **     LABEL
W1              ** O   ** 21-|          |- 7 ** I   **B5
W2              ** O   ** 22-|          |- 6 ** I   **B4
W3              ** O   ** 23-|          |- 5 ** I   **B3
W4              ** /O  ** 24-|    P     |- 4 ** I   **B2
W5              ** /O  ** 25-|    L     |- 3 ** I   **B1
W6              ** /O  ** 26-|    H     |- 2 ** I   **B0
W7              ** /O  ** 27-|    S     |- 1 ** I   **A11
R0              ** O   ** 28-|    5     |-52 ** I   **A10
R1              ** O   ** 29-|    0     |-51 ** I   **A9
R2              ** O   ** 30-|    1     |-50 ** I   **A8
R3              ** O   ** 31-|          |-49 ** I   **A7
R4              ** O   ** 32-|          |-48 ** I   **A6
R5              ** O   ** 33-|          |-47 ** I   **A5
```

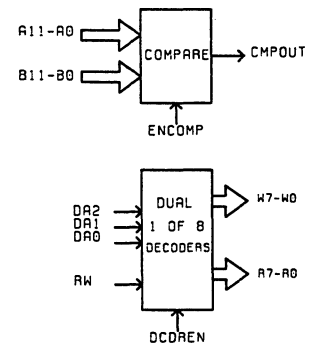
TB03770S

Figure 6.10 12-Bit Comparator Pin List

12 BIT COMPARATOR WITH DUAL 1 OF 8 DECODERS

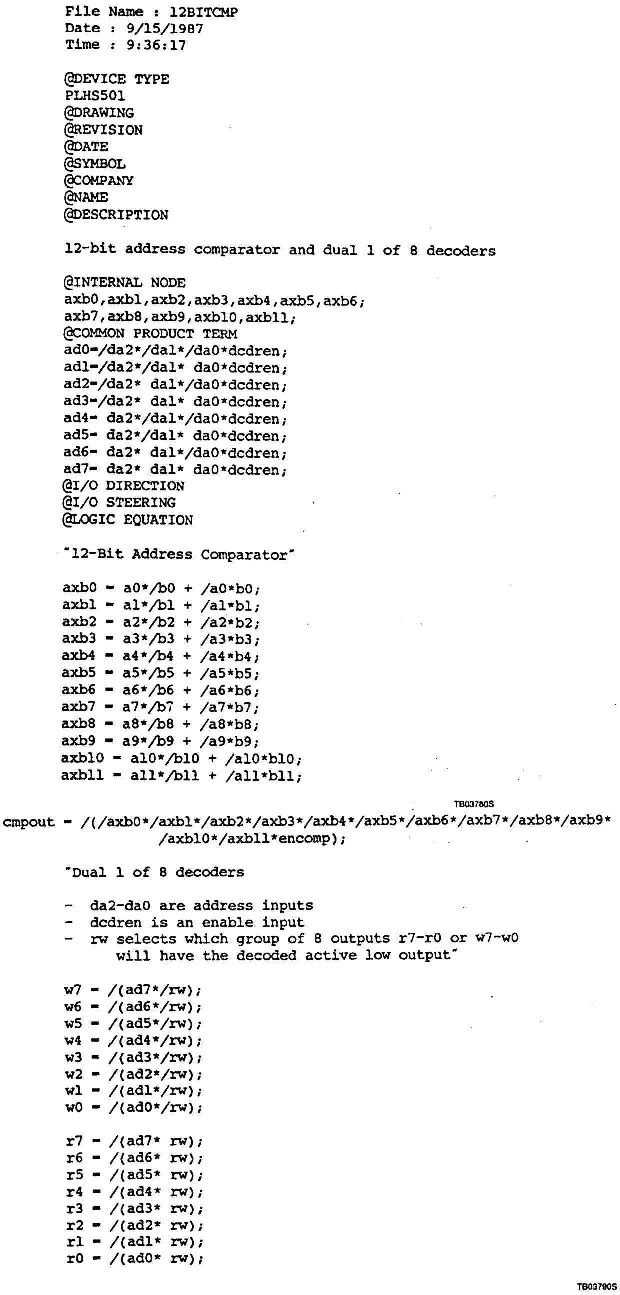
Two functions that are very often associated with controlling I/O parts are address comparison and address decoding. In this example, both functions are programmed into a PLHS501 using 52 out of the 72 foldback NAND terms.

The comparator compares 12 bits on inputs A11 – A0 to inputs B11 – B0 when the input 'ENCMP" is High. Output 'CMPOUT' will become active-Low when all 12 bits of the A input match the B. Selection between the two decoders is done with input 'R/W'. Only one output may be active (Low) at a time. Although currently separate functions, the decoder enable may be derived internally from 'CMPOUT' freeing 2 bidirectional pins which together with available foldback NAND terms, may be used to incorporate a third function.



BD10360S

Figure 6.11 12-Bit Comparator with Dual 1 – 8 Decoders Block Diagram



```
       File Name : 12BITCMP
       Date : 9/15/1987
       Time : 9:36:17

       @DEVICE TYPE
       PLHS501
       @DRAWING
       @REVISION
       @DATE
       @SYMBOL
       @COMPANY
       @NAME
       @DESCRIPTION

       12-bit address comparator and dual 1 of 8 decoders

       @INTERNAL NODE
       axb0,axb1,axb2,axb3,axb4,axb5,axb6;
       axb7,axb8,axb9,axb10,axb11;
       @COMMON PRODUCT TERM
       ad0=/da2*/da1*/da0*dcdren;
       ad1=/da2*/da1* da0*dcdren;
       ad2=/da2* da1*/da0*dcdren;
       ad3=/da2* da1* da0*dcdren;
       ad4= da2*/da1*/da0*dcdren;
       ad5= da2*/da1* da0*dcdren;
       ad6= da2* da1*/da0*dcdren;
       ad7= da2* da1* da0*dcdren;
       @I/O DIRECTION
       @I/O STEERING
       @LOGIC EQUATION

       "12-Bit Address Comparator"

       axb0 = a0*/b0 + /a0*b0;
       axb1 = a1*/b1 + /a1*b1;
       axb2 = a2*/b2 + /a2*b2;
       axb3 = a3*/b3 + /a3*b3;
       axb4 = a4*/b4 + /a4*b4;
       axb5 = a5*/b5 + /a5*b5;
       axb6 = a6*/b6 + /a6*b6;
       axb7 = a7*/b7 + /a7*b7;
       axb8 = a8*/b8 + /a8*b8;
       axb9 = a9*/b9 + /a9*b9;
       axb10 = a10*/b10 + /a10*b10;
       axb11 = a11*/b11 + /a11*b11;
```

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```
cmpout = /(/axb0*/axb1*/axb2*/axb3*/axb4*/axb5*/axb6*/axb7*/axb8*/axb9*
                  /axb10*/axb11*encomp);

       "Dual 1 of 8 decoders

       -  da2-da0 are address inputs
       -  dcdren is an enable input
       -  rw selects which group of 8 outputs r7-r0 or w7-w0
             will have the decoded active low output"

       w7 = /(ad7*/rw);
       w6 = /(ad6*/rw);
       w5 = /(ad5*/rw);
       w4 = /(ad4*/rw);
       w3 = /(ad3*/rw);
       w2 = /(ad2*/rw);
       w1 = /(ad1*/rw);
       w0 = /(ad0*/rw);

       r7 = /(ad7* rw);
       r6 = /(ad6* rw);
       r5 = /(ad5* rw);
       r4 = /(ad4* rw);
       r3 = /(ad3* rw);
       r2 = /(ad2* rw);
       r1 = /(ad1* rw);
       r0 = /(ad0* rw);
```

TB03790S

Figure 6.12 12-Bit Comparator Boolean Equations

```
" Simulation inputs for 12BITCMP
" <--------INPUTS--------> < B,/B >
" 222211111111111
" 32HL98765432HL98765432HL 765432HL
"
  LLLLLLLLLLLLLLLLLLLLLLLL -LLL-LLL "disable comp"
  LLLLLLLLLLLLLLLLLLLLLLLL -LLH-LLL "enable comp"
  HLHLHLHLHLHLHLHLHLHLHLHL -LLH-LLL "comp AA"
  LHLHLHLHLHLHLHLHLHLHLHLH -LLH-LLL "comp 55"
  HHHHHHHHHHHHHHHHHHHHHHHH -LLH-LLL "comp FF"
  HHHHHHHHHHHHLHHHHHHHHHHH -LLH-LLL "A not equal B"
  LLLLLLLLLLLLLLLLLLLLLLLL -LHL-LLL "enable decoder W"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-LLL "enable decoder R"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-LLH "count 1"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-LHL "      2"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-LHH "      3"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-HLL "      4"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-HLH "      5"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-HHL "      6"
  LLLLLLLLLLLLLLLLLLLLLLLL -HHL-HHH "      7"
  LLLLLLLLLLLLLLLLLLLLLLLL -LHL-HHH "enable decoder W"
QUIT
```

TB03800S

Figure 6.13 12-Bit Comparator Simulation Input File

```
PLHS501          12BITCMP        Time = 15:0:58 Date = 9/14/1987
"
" <--------INPUTS--------> < B,/B > < XOR   > < /O,O >  TRACE TERMS
" 222211111111111
" 321098765432109876543210 76543210 76543210 76543210
"
  000000000000000000000000 H000H000 HHHHHHHH HHHHHHHH ;
  000000000000000000000000 H001L000 HHHHHHHH HHHHHHHH ;
  101010101010101010101010 H001L000 HHHHHHHH HHHHHHHH ;
  010101010101010101010101 H001L000 HHHHHHHH HHHHHHHH ;
  111111111111111111111111 H001L000 HHHHHHHH HHHHHHHH ;
  111111111111011111111111 H001H000 HHHHHHHH HHHHHHHH ;
  000000000000000000000000 H010H000 HHHHHHHH HHHHHHHL ;
  000000000000000000000000 H110H000 HHHHHHHL HHHHHHHH ;
  000000000000000000000000 H110H001 HHHHHHLH HHHHHHHH ;
  000000000000000000000000 H110H010 HHHHHLHH HHHHHHHH ;
  000000000000000000000000 H110H011 HHHHLHHH HHHHHHHH ;
  000000000000000000000000 H110H100 HHHLHHHH HHHHHHHH ;
  000000000000000000000000 H110H101 HHLHHHHH HHHHHHHH ;
  000000000000000000000000 H110H110 HLHHHHHH HHHHHHHH ;
  000000000000000000000000 H110H111 LHHHHHHH HHHHHHHH ;
  000000000000000000000000 H010H111 HHHHHHHH LHHHHHHH ;
"
" ------------------------ --------   I/O CONTROL LINES
"                          OIIIOIII   DESIGNATED I/O USAGE
"                          OIIIOIII   ACTUAL I/O USAGE
"
" PINLIST...
" 14 13 12 11 10 09 07 06 05 04 03 02 01 52 51 50 49 48 47 45 44 43 42 41
" 18 17 16 15 40 39 38 37 36 35 33 32 31 30 29 28
" 27 26 25 24 23 22 21 19 ;
```

TB03810S

Figure 6.14 12-Bit Comparator Simulation Log File

8-BIT CARRY LOOK-AHEAD ADDER

This function may be used as part of an ALU design or simply to off-load a microprocessor. Figure 6.16 is a block diagram showing the individual components needed for each bit.

A carry input (C0) is provided along with a carry output (C8). The result of an addition between the inputs A7 – A0 and B7 – B0 occurs on outputs SUM7 – SUM0.

```
File Name : 8BITADDR
Date : 9/15/1987
Time : 9:37:21

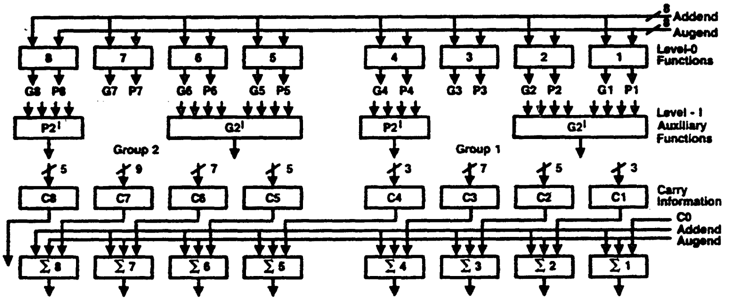
##################### P I N   L I S T #####################

          Left                                    Right
   LABEL        ** FNC **PIN             PIN** FNC **     LABEL
VCC             ** +5V **  8-|           |-46 ** +5V **VCC
A2              ** I   **  9-|           |-45 ** I   **N/C
A3              ** I   ** 10-|           |-44 ** I   **N/C
A4              ** I   ** 11-|     P     |-43 ** I   **N/C
A5              ** I   ** 12-|     L     |-42 ** I   **N/C
A6              ** I   ** 13-|     H     |-41 ** I   **N/C
A7              ** I   ** 14-|     S     |-40 ** /O  **N/C
N/C             ** B   ** 15-|     5     |-39 ** /O  **N/C
N/C             ** B   ** 16-|     0     |-38 ** /O  **N/C
N/C             ** B   ** 17-|     1     |-37 ** /O  **N/C
N/C             ** B   ** 18-|           |-36 ** O   **SUM7
C8              ** O   ** 19-|           |-35 ** O   **SUM6
GND             ** 0V  ** 20-|           |-34 ** 0V  **GND


          Bottom                                   Top
   LABEL        ** FNC **PIN             PIN** FNC **      LABEL
N/C             ** O   ** 21-|           |- 7 ** I   **A1
N/C             ** O   ** 22-|           |- 6 ** I   **A0
N/C             ** O   ** 23-|           |- 5 ** I   **B7
N/C             ** /O  ** 24-|     P     |- 4 ** I   **B6
N/C             ** /O  ** 25-|     L     |- 3 ** I   **B5
N/C             ** /O  ** 26-|     H     |- 2 ** I   **B4
N/C             ** /O  ** 27-|     S     |- 1 ** I   **B3
SUM0            ** O   ** 28-|     5     |-52 ** I   **B2
SUM1            ** O   ** 29-|     0     |-51 ** I   **B1
SUM2            ** O   ** 30-|     1     |-50 ** I   **B0
SUM3            ** O   ** 31-|           |-49 ** I   **C0
SUM4            ** O   ** 32-|           |-48 ** I   **N/C
SUM5            ** O   ** 33-|           |-47 ** I   **N/C
```

TB03820S

Figure 6.15 8-Bit Adder Pin List



BD10370S

NOTES:

G1' = G4 + P4 * G3 + P4 * P3 * G2 + P4 * P3 * P2 * G1;
P1' = P4 * P3 * P2 * P1
G2' = G8 + P8 * G7 + P8 * P7 * G6 + P8 * P7 * P6 * G5;
P2' = P8 * P7 * P6 * P5

C1 = G1 + P1 * C0;
C2 = G2 + P2 * G1 + P2 * P1 * C0;
C3 = G3 + P3 * G2 + P3 * P2 * G1 + P3 * P2 * P1 * C0;
C4 = G1' + P1' * C0;
C5 = G5 + P5 * G1' + P5 * P1' * C0;
C6 = G6 + P6 * G5 + P6 * P5 * G1' + P6 * P5 * P1' * C0;
C7 = G7 + P7 * G6 + P7 * P6 * G5 + P7 * P6 * P5 * G1' + P7 * P6 * P5 * P1' * C0;
C8 = G2' + P2' * G1' + P2' * P1' * C0;

Figure 6.16 8-Bit Carry Look-Ahead Adder Block Diagram and Equations

Designing with Programmable Macro Logic

```
File Name : 8BITADDR
Date : 9/15/1987
Time : 9:37:36
@DEVICE TYPE
PLHS501
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION
8 Bit Carry Look-Ahead Adder

@INTERNAL NODE
 g8, gl, g2, g3, g4, g5, g6, g7;
 p8, pl, p2, p3, p4, p5, p6, p7;
gn8,gnl,gn2,gn3,gn4,gn5,gn6,gn7;
cl,c2,c3,c4,c5,c6,c7;
gl_1,g2_1;
@COMMON PRODUCT TERM
@I/O DIRECTION
@I/O STEERING
@LOGIC EQUATION

"level-0 functions"
gnl = /(a0*b0);
pl = /(/a0*/b0);
gl = /gnl;

gn2 = /(al*bl);
p2 = /(/al*/bl);
g2 = /gn2;

gn3 = /(a2*b2);
p3 = /(/a2*/b2);
g3 = /gn3;

gn4 = /(a3*b3);
p4 = /(/a3*/b3);
g4 = /gn4;

gn5 = /(a4*b4);
p5 = /(/a4*/b4);
g5 = /gn5;

gn6 = /(a5*b5);
```

TB03830S

Figure 6.17 8-Bit Adder Boolean Equations

```
p6 = /(/a5*/b5);
g6 = /gn6;

gn7 = /(a6*b6);
p7 = /(/a6*/b6);
g7 = /gn7;

gn8 = /(a7*b7);
p8 = /(/a7*/b7);
g8 = /gn8;


"level-1 functions"
gl_1 = g4 + p4*g3 + p4*p3*g2 + p4*p3*p2*gl;
g2_1 = g8 + p8*g7 + p8*p7*g6 + p8*p7*p6*g5;

"carry information"
cl = gl + pl*c0;
c2 = g2 + p2*gl + p2*pl*c0;
c3 = g3 + p3*g2 + p3*p2*gl + p3*p2*pl*c0;
c4 = gl_1 + p4*p3*p2*pl*c0;
c5 = g5 + p5*gl_1 + p5*p4*p3*p2*pl*c0;
c6 = g6 + p6*g5 + p6*p5*gl_1 + p6*p5*p4*p3*p2*pl*c0;
c7 = g7 + p7*g6 + p7*p6*g5 + p7*p6*p5*gl_1 +
          p7*p6*p5*p4*p3*p2*pl*c0;
c8 = g2_1 + p8*p7*p6*p5*gl_1 + p8*p7*p6*p5*p4*p3*p2*pl*c0;

"addition functions"
sum0 : xrl = c0;
       xr2 = pl * gnl;
suml : xrl = cl;
       xr2 = p2 * gn2;
sum2 : xrl = c2;
       xr2 = p3 * gn3;
sum3 : xrl = c3;
       xr2 = p4 * gn4;
sum4 : xrl = c4;
       xr2 = p5 * gn5;
sum5 : xrl = c5;
       xr2 = p6 * gn6;
sum6 : xrl = c6;
       xr2 = p7 * gn7;
sum7 : xrl = c7;
       xr2 = p8 * gn8;
```

TB04070S

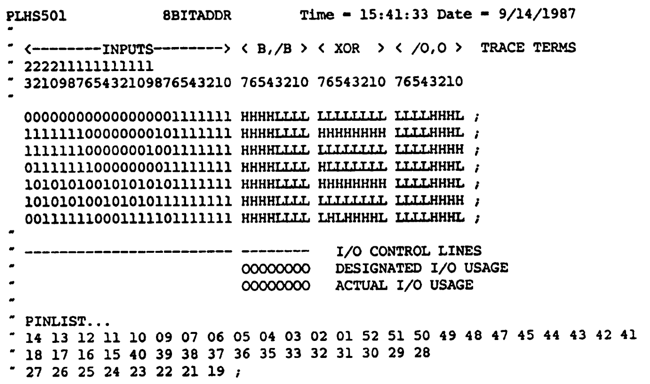
Figure 6.17 8-Bit Adder Boolean Equations (Continued)

```
" 8 Bit Adder Simulation input
"
" <--------INPUTS--------> < B,/B >
" 2222HHHHHHHHHHl
" 321098765432109876543210 76543210
"
  LLLLLLLLLLLLLLLLLHHHHHHH -------- "0 + 0"
  HHHHHHHLLLLLLLLHLHHHHHHH -------- "0 + FF"
  HHHHHHHLLLLLLLLHLLHHHHHH -------- "1 + FF"
  LHHHHHHHLLLLLLLLLHHHHHHH -------- "0 + 7F + CARRY IN"
  HLHLHLHLLHLHLHLHLHHHHHHH -------- "AA + 55"
  HLHLHLHLLHLHLHLHHHHHHHHH -------- "AA + 55 + CARRY IN"
  LLHHHHHHLLLHHHHHLHHHHHHH -------- "3F + 1F"
QUIT
```

TB03840S

Figure 6.18 8-Bit Adder Simulation Input File

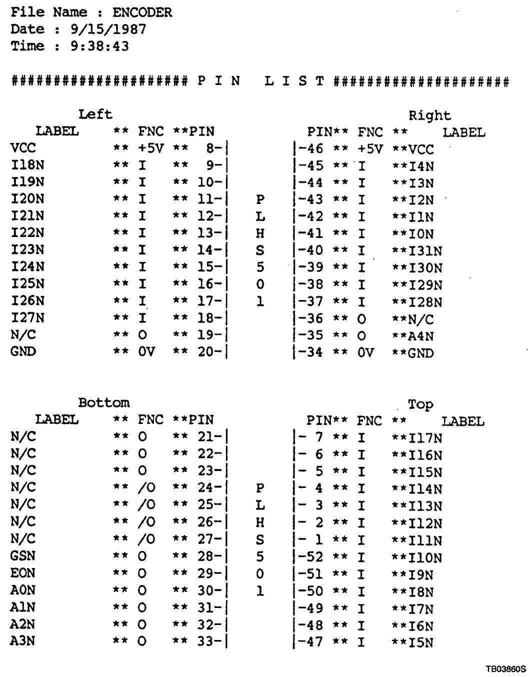
Designing with Programmable Macro Logic



```
PLHS501          8BITADDR        Time = 15:41:33 Date = 9/14/1987
"
" <--------INPUTS--------> < B,/B > < XOR  > < /O,O >  TRACE TERMS
" 2222111111111111
" 321098765432109876543210 76543210 76543210 76543210
"
  000000000000000001111111 HHHHLLLL LLLLLLLL LLLLHHHL ;
  111111100000000101111111 HHHHLLLL HHHHHHHH LLLLHHHL ;
  111111100000001001111111 HHHHLLLL LLLLLLLL LLLLHHHH ;
  011111110000000011111111 HHHHLLLL HLLLLLLL LLLLHHHL ;
  101010100101010101111111 HHHHLLLL HHHHHHHH LLLLHHHL ;
  101010100101010111111111 HHHHLLLL LLLLLLLL LLLLHHHH ;
  001111110001111101111111 HHHHLLLL LHLHHHHL LLLLHHHL ;
"
" ------------------------ --------   I/O CONTROL LINES
"                          00000000   DESIGNATED I/O USAGE
"                          00000000   ACTUAL I/O USAGE
"
" PINLIST...
" 14 13 12 11 10 09 07 06 05 04 03 02 01 52 51 50 49 48 47 45 44 43 42 41
" 18 17 16 15 40 39 38 37 36 35 33 32 31 30 29 28
" 27 26 25 24 23 22 21 19 ;
```

TB03850S

Figure 6.19 8-Bit Adder Simulation Log File



```
File Name : ENCODER
Date : 9/15/1987
Time : 9:38:43

##################### P I N   L I S T #####################

        Left                                        Right
   LABEL     ** FNC **PIN              PIN** FNC **    LABEL
VCC          ** +5V **  8-|          |-46 ** +5V **VCC
I18N         ** I   **  9-|          |-45 ** I   **I4N
I19N         ** I   ** 10-|          |-44 ** I   **I3N
I20N         ** I   ** 11-|    P     |-43 ** I   **I2N
I21N         ** I   ** 12-|    L     |-42 ** I   **I1N
I22N         ** I   ** 13-|    H     |-41 ** I   **I0N
I23N         ** I   ** 14-|    S     |-40 ** I   **I31N
I24N         ** I   ** 15-|    5     |-39 ** I   **I30N
I25N         ** I   ** 16-|    0     |-38 ** I   **I29N
I26N         ** I   ** 17-|    1     |-37 ** I   **I28N
I27N         ** I   ** 18-|          |-36 ** O   **N/C
N/C          ** O   ** 19-|          |-35 ** O   **A4N
GND          ** OV  ** 20-|          |-34 ** OV  **GND

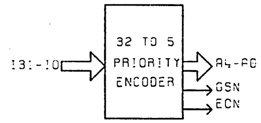

        Bottom                                       Top
   LABEL     ** FNC **PIN              PIN** FNC **    LABEL
N/C          ** O   ** 21-|          |- 7 ** I   **I17N
N/C          ** O   ** 22-|          |- 6 ** I   **I16N
N/C          ** O   ** 23-|          |- 5 ** I   **I15N
N/C          ** /O  ** 24-|    P     |- 4 ** I   **I14N
N/C          ** /O  ** 25-|    L     |- 3 ** I   **I13N
N/C          ** /O  ** 26-|    H     |- 2 ** I   **I12N
N/C          ** /O  ** 27-|    S     |- 1 ** I   **I11N
GSN          ** O   ** 28-|    5     |-52 ** I   **I10N
EON          ** O   ** 29-|    0     |-51 ** I   **I9N
A0N          ** O   ** 30-|    1     |-50 ** I   **I8N
A1N          ** O   ** 31-|          |-49 ** I   **I7N
A2N          ** O   ** 32-|          |-48 ** I   **I6N
A3N          ** O   ** 33-|          |-47 ** I   **I5N
```

TB03860S

Figure 6.20 Encoder Pin List

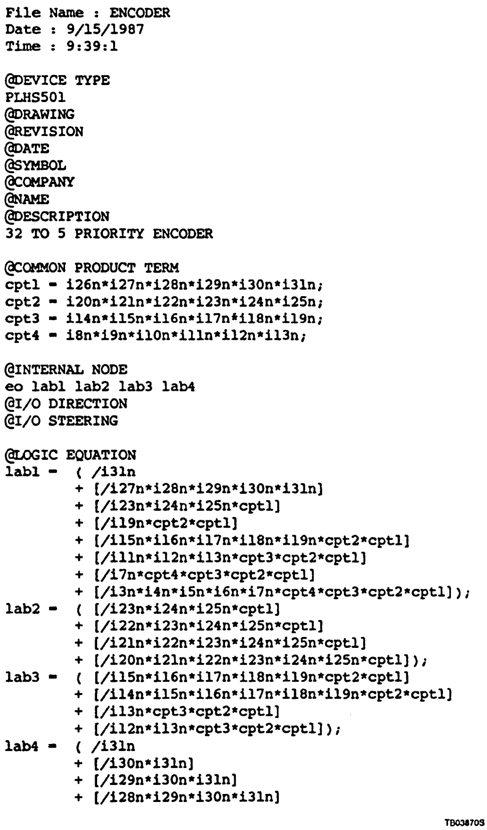
32- to 5-BIT PRIORITY ENCODER

This relatively simple example demonstrates the capability of the PLHS501 to be programmed with functions that are not available in 'standard' device libraries. The equations may look difficult at first glance. However, there is a pattern to the encoding. Referring to Figure 6.21 Lab4 – Lab1 are terms that are common to several outputs (A4n – A0n). Separating them from the main equations allows a total reduction in the numbers of gates used.



BD10380S

Figure 6.21 32 to 5 Priority Encoder Block Diagram



```
File Name : ENCODER
Date : 9/15/1987
Time : 9:39:1

@DEVICE TYPE
PLHS501
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION
32 TO 5 PRIORITY ENCODER

@COMMON PRODUCT TERM
cpt1 = i26n*i27n*i28n*i29n*i30n*i31n;
cpt2 = i20n*i21n*i22n*i23n*i24n*i25n;
cpt3 = i14n*i15n*i16n*i17n*i18n*i19n;
cpt4 = i8n*i9n*i10n*i11n*i12n*i13n;

@INTERNAL NODE
eo lab1 lab2 lab3 lab4
@I/O DIRECTION
@I/O STEERING

@LOGIC EQUATION
lab1 =  ( /i31n
        + [/i27n*i28n*i29n*i30n*i31n]
        + [/i23n*i24n*i25n*cpt1]
        + [/i19n*cpt2*cpt1]
        + [/i15n*i16n*i17n*i18n*i19n*cpt2*cpt1]
        + [/i11n*i12n*i13n*cpt3*cpt2*cpt1]
        + [/i7n*cpt4*cpt3*cpt2*cpt1]
        + [/i3n*i4n*i5n*i6n*i7n*cpt4*cpt3*cpt2*cpt1]);
lab2 =  ( [/i23n*i24n*i25n*cpt1]
        + [/i22n*i23n*i24n*i25n*cpt1]
        + [/i21n*i22n*i23n*i24n*i25n*cpt1]
        + [/i20n*i21n*i22n*i23n*i24n*i25n*cpt1]);
lab3 =  ( [/i15n*i16n*i17n*i18n*i19n*cpt2*cpt1]
        + [/i14n*i15n*i16n*i17n*i18n*i19n*cpt2*cpt1]
        + [/i13n*cpt3*cpt2*cpt1]
        + [/i12n*i13n*cpt3*cpt2*cpt1]);
lab4 =  ( /i31n
        + [/i30n*i31n]
        + [/i29n*i30n*i31n]
        + [/i28n*i29n*i30n*i31n]
```

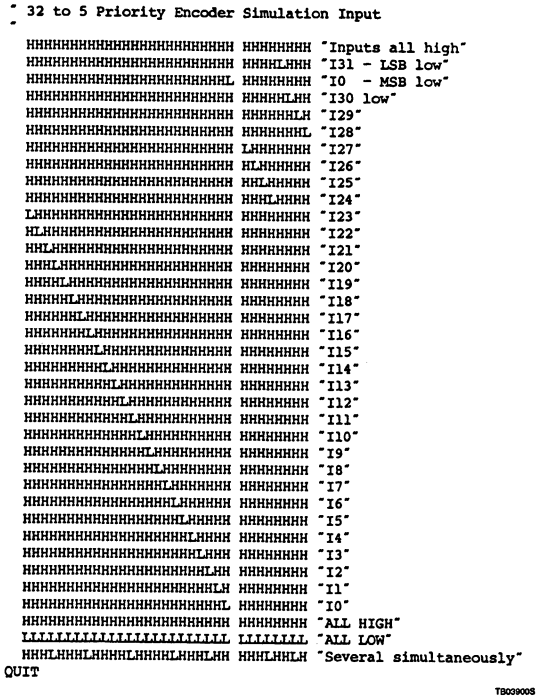
TB03870S

Figure 6.22 Encoder Boolean Equations

```
             + [/i27n*i28n*i29n*i30n*i31n]
             + [/i26n*i27n*i28n*i29n*i30n*i31n]
             + [/i25n*cpt1]
             + [/i24n*i25n*cpt1]);
eo   = /(i0n*i1n*i2n*i3n*i4n*i5n*i6n*i7n
             *i8n*i9n*i10n*i11n*i12n*i13n*i14n*i15n
             *i16n*i17n*i18n*i19n*i20n*i21n*i22n*i23n
             *i24n*i25n*cpt1);
gsn = /eo;
eon = eo;
a0n =  /( lab1
            + [/i29n*i30n*i31n]
            + [/i25n*cpt1]
            + [/i21n*i22n*i23n*i24n*i25n*cpt1]
            + [/i17n*i18n*i19n*cpt2*cpt1]
            + [/i13n*cpt3*cpt2*cpt1]
            + [/i9n*i10n*i11n*i12n*i13n*cpt3*cpt2*cpt1]
            + [/i5n*i6n*i7n*cpt4*cpt3*cpt2*cpt1]
            + [/i1n*i2n*i3n*i4n*i5n*i6n*i7n*cpt4*cpt3*cpt2*cpt1]);
a1n =  /( lab1
            + [/i30n*i31n]
            + [/i26n*i27n*i28n*i29n*i30n*i31n]
            + [/i22n*i23n*i24n*i25n*cpt1]
            + [/i18n*i19n*cpt2*cpt1]
            + [/i14n*i15n*i16n*i17n*i18n*i19n*cpt2*cpt1]
            + [/i10n*i11n*i12n*i13n*cpt3*cpt2*cpt1]
            + [/i6n*i7n*cpt4*cpt3*cpt2*cpt1]
            + [/i2n*i3n*i4n*i5n*i6n*i7n*cpt4*cpt3*cpt2*cpt1]);
a2n =  /(  /i31n
            + [/i30n*i31n]
            + [/i29n*i30n*i31n]
            + [/i28n*i29n*i30n*i31n]
            + lab2
            + lab3
            + [/i7n*cpt4*cpt3*cpt2*cpt1]
            + [/i6n*i7n*cpt4*cpt3*cpt2*cpt1]
            + [/i5n*i6n*i7n*cpt4*cpt3*cpt2*cpt1]
            + [/i4n*i5n*i6n*i7n*cpt4*cpt3*cpt2*cpt1]);
a3n =  /( lab4
            + lab3
            + [/i11n*i12n*i13n*cpt3*cpt2*cpt1]
            + [/i10n*i11n*i12n*i13n*cpt3*cpt2*cpt1]
            + [/i9n*i10n*i11n*i12n*i13n*cpt3*cpt2*cpt1]
            + [/i8n*i9n*i10n*i11n*i12n*i13n*cpt3*cpt2*cpt1]);
a4n =  /( lab4
            + lab2                                          TB03880S
            + [/i19n*cpt2*cpt1]
            + [/i18n*i19n*cpt2*cpt1]
            + [/i17n*i18n*i19n*cpt2*cpt1]
            + [/i16n*i17n*i18n*i19n*cpt2*cpt1]);
```

TB03890S

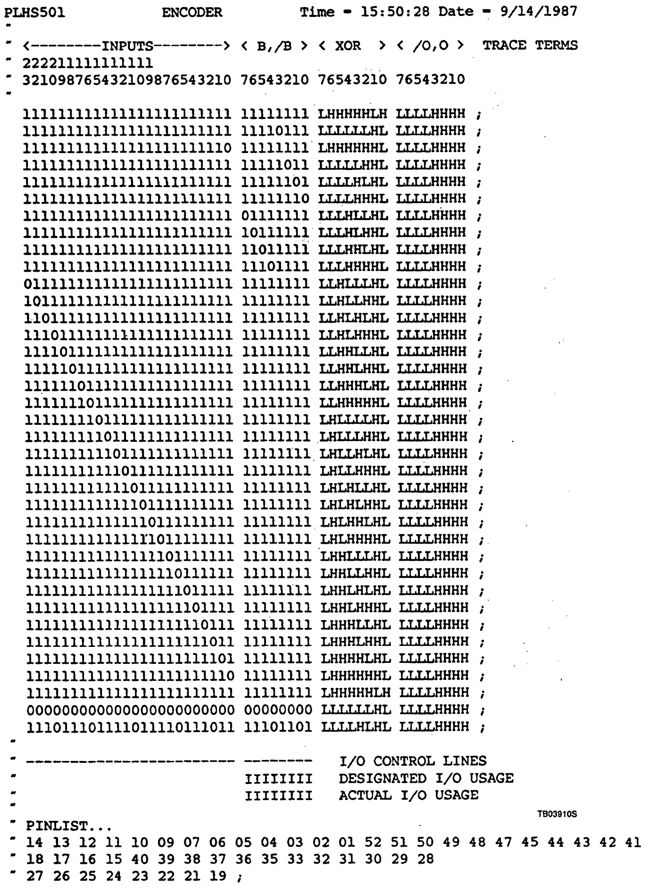
Figure 6.22 Encoder Boolean Equations (Continued)



```
" 32 to 5 Priority Encoder Simulation Input
"
  HHHHHHHHHHHHHHHHHHHHHHHH HHHHHHHH "Inputs all high"
  HHHHHHHHHHHHHHHHHHHHHHHH HHHHLHHH "I31 - LSB low"
  HHHHHHHHHHHHHHHHHHHHHHHL HHHHHHHH "I0  - MSB low"
  HHHHHHHHHHHHHHHHHHHHHHHH HHHHHLHH "I30 low"
  HHHHHHHHHHHHHHHHHHHHHHHH HHHHHHLH "I29"
  HHHHHHHHHHHHHHHHHHHHHHHH HHHHHHHL "I28"
  HHHHHHHHHHHHHHHHHHHHHHHH LHHHHHHH "I27"
  HHHHHHHHHHHHHHHHHHHHHHHH HLHHHHHH "I26"
  HHHHHHHHHHHHHHHHHHHHHHHH HHLHHHHH "I25"
  HHHHHHHHHHHHHHHHHHHHHHHH HHHLHHHH "I24"
  LHHHHHHHHHHHHHHHHHHHHHHH HHHHHHHH "I23"
  HLHHHHHHHHHHHHHHHHHHHHHH HHHHHHHH "I22"
  HHLHHHHHHHHHHHHHHHHHHHHH HHHHHHHH "I21"
  HHHLHHHHHHHHHHHHHHHHHHHH HHHHHHHH "I20"
  HHHHLHHHHHHHHHHHHHHHHHHH HHHHHHHH "I19"
  HHHHHLHHHHHHHHHHHHHHHHHH HHHHHHHH "I18"
  HHHHHHLHHHHHHHHHHHHHHHHH HHHHHHHH "I17"
  HHHHHHHLHHHHHHHHHHHHHHHH HHHHHHHH "I16"
  HHHHHHHHLHHHHHHHHHHHHHHH HHHHHHHH "I15"
  HHHHHHHHHLHHHHHHHHHHHHHH HHHHHHHH "I14"
  HHHHHHHHHHLHHHHHHHHHHHHH HHHHHHHH "I13"
  HHHHHHHHHHHLHHHHHHHHHHHH HHHHHHHH "I12"
  HHHHHHHHHHHHLHHHHHHHHHHH HHHHHHHH "I11"
  HHHHHHHHHHHHHLHHHHHHHHHH HHHHHHHH "I10"
  HHHHHHHHHHHHHHLHHHHHHHHH HHHHHHHH "I9"
  HHHHHHHHHHHHHHHLHHHHHHHH HHHHHHHH "I8"
  HHHHHHHHHHHHHHHHLHHHHHHH HHHHHHHH "I7"
  HHHHHHHHHHHHHHHHHLHHHHHH HHHHHHHH "I6"
  HHHHHHHHHHHHHHHHHHLHHHHH HHHHHHHH "I5"
  HHHHHHHHHHHHHHHHHHHLHHHH HHHHHHHH "I4"
  HHHHHHHHHHHHHHHHHHHHLHHH HHHHHHHH "I3"
  HHHHHHHHHHHHHHHHHHHHHLHH HHHHHHHH "I2"
  HHHHHHHHHHHHHHHHHHHHHHLH HHHHHHHH "I1"
  HHHHHHHHHHHHHHHHHHHHHHHL HHHHHHHH "I0"
  HHHHHHHHHHHHHHHHHHHHHHHH HHHHHHHH "ALL HIGH"
  LLLLLLLLLLLLLLLLLLLLLLLL LLLLLLLL "ALL LOW"
  HHHLHHHLHHHHLHHHHLHHHLHH HHHLHHLH "Several simultaneously"
QUIT
```

TB03900S

Figure 6.23 Encoder Simulation Input File



```
PLHS501          ENCODER         Time = 15:50:28 Date = 9/14/1987
"
" <--------INPUTS--------> < B,/B > < XOR  > < /O,O >  TRACE TERMS
" 222211111111111
" 321098765432109876543210 76543210 76543210 76543210
"
  111111111111111111111111 11111111 LHHHHHLH LLLLHHHH ;
  111111111111111111111111 11110111 LLLLLLHL LLLLHHHH ;
  111111111111111111111110 11111111 LHHHHHHL LLLLHHHH ;
  111111111111111111111111 11111011 LLLLLHHL LLLLHHHH ;
  111111111111111111111111 11111101 LLLLHLHL LLLLHHHH ;
  111111111111111111111111 11111110 LLLLHHHL LLLLHHHH ;
  111111111111111111111111 01111111 LLLHLLHL LLLLHHHH ;
  111111111111111111111111 10111111 LLLHLHHL LLLLHHHH ;
  111111111111111111111111 11011111 LLLHHLHL LLLLHHHH ;
  111111111111111111111111 11101111 LLLHHHHL LLLLHHHH ;
  011111111111111111111111 11111111 LLHLLLHL LLLLHHHH ;
  101111111111111111111111 11111111 LLHLLHHL LLLLHHHH ;
  110111111111111111111111 11111111 LLHLHLHL LLLLHHHH ;
  111011111111111111111111 11111111 LLHLHHHL LLLLHHHH ;
  111101111111111111111111 11111111 LLHHLLHL LLLLHHHH ;
  111110111111111111111111 11111111 LLHHLHHL LLLLHHHH ;
  111111011111111111111111 11111111 LLHHHLHL LLLLHHHH ;
  111111101111111111111111 11111111 LLHHHHHL LLLLHHHH ;
  111111110111111111111111 11111111 LHLLLLHL LLLLHHHH ;
  111111111011111111111111 11111111 LHLLLHHL LLLLHHHH ;
  111111111101111111111111 11111111 LHLLHLHL LLLLHHHH ;
  111111111110111111111111 11111111 LHLLHHHL LLLLHHHH ;
  111111111111011111111111 11111111 LHLHLLHL LLLLHHHH ;
  111111111111101111111111 11111111 LHLHLHHL LLLLHHHH ;
  111111111111110111111111 11111111 LHLHHLHL LLLLHHHH ;
  111111111111111011111111 11111111 LHLHHHHL LLLLHHHH ;
  111111111111111101111111 11111111 LHHLLLHL LLLLHHHH ;
  111111111111111110111111 11111111 LHHLLHHL LLLLHHHH ;
  111111111111111111011111 11111111 LHHLHLHL LLLLHHHH ;
  111111111111111111101111 11111111 LHHLHHHL LLLLHHHH ;
  111111111111111111110111 11111111 LHHHLLHL LLLLHHHH ;
  111111111111111111111011 11111111 LHHHLHHL LLLLHHHH ;
  111111111111111111111101 11111111 LHHHHLHL LLLLHHHH ;
  111111111111111111111110 11111111 LHHHHHHL LLLLHHHH ;
  111111111111111111111111 11111111 LHHHHHLH LLLLHHHH ;
  000000000000000000000000 00000000 LLLLLLHL LLLLHHHH ;
  111011101111011110111011 11101101 LLLLHLHL LLLLHHHH ;
"
" ------------------------ --------   I/O CONTROL LINES
"                          IIIIIIII   DESIGNATED I/O USAGE
"                          IIIIIIII   ACTUAL I/O USAGE
"
" PINLIST...
" 14 13 12 11 10 09 07 06 05 04 03 02 01 52 51 50 49 48 47 45 44 43 42 41
" 18 17 16 15 40 39 38 37 36 35 33 32 31 30 29 28
" 27 26 25 24 23 22 21 19 ;
```

TB03910S

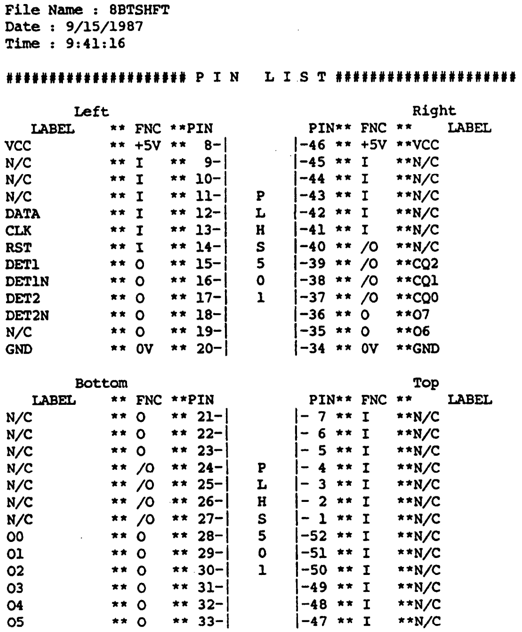
TB03920S

Figure 6.24 Encoder Simulation Log File

8-BIT SHIFT REGISTER WITH SEQUENCE DETECTOR

This example demonstrates an application using D type edge-triggered flip-flops. Six NAND gates are used for each flip-flop (Figure 3.2). Note that to add an asynchronous reset and/or set to any flip-flop requires no additional gates. Also, every flip-flop must have a reset or set line to initialize it. Without being initialized, the simulator will not be able to determine the output states as it could power-up in either a set or reset condition. An uninitialized flip-flop will cause AMAZE 1.6 to display a message indicating the outputs are not stabilized within a certain time period.

As can be seen from the block diagram (Figure 6.26) this design consists of an 8-bit shift register, 3-bit ripple counter and 2 flip-flops that are set only upon detection of specific patterns. The patterns are read from the Q and QN outputs of the shift register. Since the input to the second flip-flop has the output of the first flip-flop as a product term, detection of the first pattern is a requirement for the detection of the second.



```
File Name : 8BTSHFT
Date : 9/15/1987
Time : 9:41:16

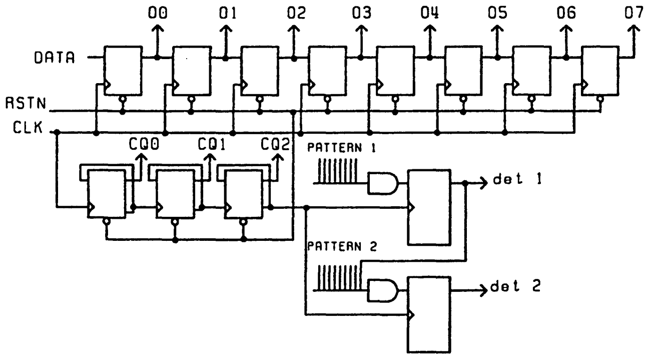
###################### P I N   L I S T ######################

            Left                                        Right
    LABEL       ** FNC **PIN              PIN** FNC **     LABEL
VCC             ** +5V **  8-|           |-46 ** +5V **VCC
N/C             ** I   **  9-|           |-45 ** I   **N/C
N/C             ** I   ** 10-|           |-44 ** I   **N/C
N/C             ** I   ** 11-|   P       |-43 ** I   **N/C
DATA            ** I   ** 12-|   L       |-42 ** I   **N/C
CLK             ** I   ** 13-|   H       |-41 ** I   **N/C
RST             ** I   ** 14-|   S       |-40 ** /O  **N/C
DET1            ** O   ** 15-|   5       |-39 ** /O  **CQ2
DET1N           ** O   ** 16-|   0       |-38 ** /O  **CQ1
DET2            ** O   ** 17-|   1       |-37 ** /O  **CQ0
DET2N           ** O   ** 18-|           |-36 ** O   **O7
N/C             ** O   ** 19-|           |-35 ** O   **O6
GND             ** OV  ** 20-|           |-34 ** OV  **GND

            Bottom                                      Top
    LABEL       ** FNC **PIN              PIN** FNC **     LABEL
N/C             ** O   ** 21-|           |- 7 ** I   **N/C
N/C             ** O   ** 22-|           |- 6 ** I   **N/C
N/C             ** O   ** 23-|           |- 5 ** I   **N/C
N/C             ** /O  ** 24-|   P       |- 4 ** I   **N/C
N/C             ** /O  ** 25-|   L       |- 3 ** I   **N/C
N/C             ** /O  ** 26-|   H       |- 2 ** I   **N/C
N/C             ** /O  ** 27-|   S       |- 1 ** I   **N/C
O0              ** O   ** 28-|   5       |-52 ** I   **N/C
O1              ** O   ** 29-|   0       |-51 ** I   **N/C
O2              ** O   ** 30-|   1       |-50 ** I   **N/C
O3              ** O   ** 31-|           |-49 ** I   **N/C
O4              ** O   ** 32-|           |-48 ** I   **N/C
O5              ** O   ** 33-|           |-47 ** I   **N/C
```

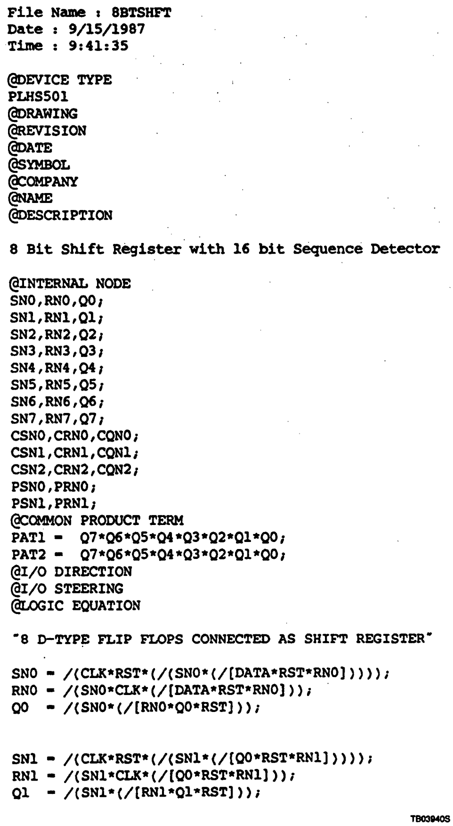
TB03930S

Figure 6.25 8-Bit Shifter Pin List



BD10390S

Figure 6.26 Shift Register with Sequence Detector Block Diagram



```
File Name : 8BTSHFT
Date : 9/15/1987
Time : 9:41:35

@DEVICE TYPE
PLHS501
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION

8 Bit Shift Register with 16 bit Sequence Detector

@INTERNAL NODE
SN0,RN0,Q0;
SN1,RN1,Q1;
SN2,RN2,Q2;
SN3,RN3,Q3;
SN4,RN4,Q4;
SN5,RN5,Q5;
SN6,RN6,Q6;
SN7,RN7,Q7;
CSN0,CRN0,CQN0;
CSN1,CRN1,CQN1;
CSN2,CRN2,CQN2;
PSN0,PRN0;
PSN1,PRN1;
@COMMON PRODUCT TERM
PAT1 =  Q7*Q6*Q5*Q4*Q3*Q2*Q1*Q0;
PAT2 =  Q7*Q6*Q5*Q4*Q3*Q2*Q1*Q0;
@I/O DIRECTION
@I/O STEERING
@LOGIC EQUATION

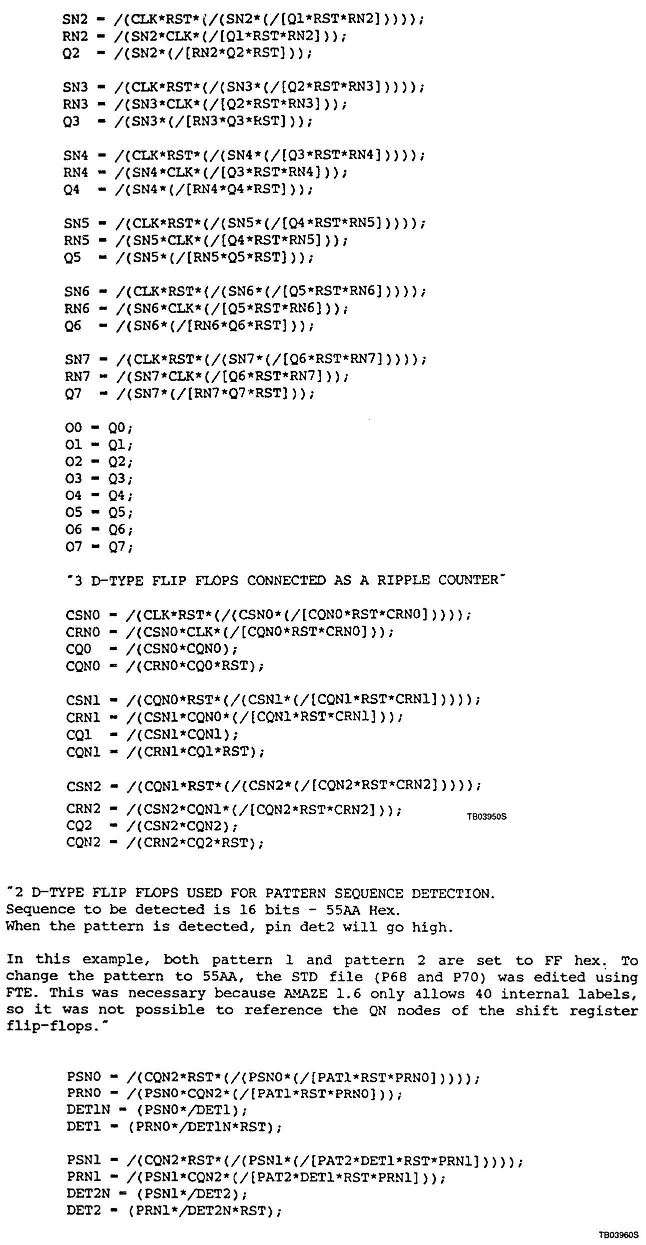
"8 D-TYPE FLIP FLOPS CONNECTED AS SHIFT REGISTER"

SN0 = /(CLK*RST*(/(SN0*(/[DATA*RST*RN0]))));
RN0 = /(SN0*CLK*(/[DATA*RST*RN0]));
Q0  = /(SN0*(/[RN0*Q0*RST]));


SN1 = /(CLK*RST*(/(SN1*(/[Q0*RST*RN1]))));
RN1 = /(SN1*CLK*(/[Q0*RST*RN1]));
Q1  = /(SN1*(/[RN1*Q1*RST]));
```

TB03940S

Figure 6.27 8-Bit Shifter Boolean Equations



```
        SN2 = /(CLK*RST*(/(SN2*(/[Q1*RST*RN2]))));
        RN2 = /(SN2*CLK*(/[Q1*RST*RN2]));
        Q2  = /(SN2*(/[RN2*Q2*RST]));

        SN3 = /(CLK*RST*(/(SN3*(/[Q2*RST*RN3]))));
        RN3 = /(SN3*CLK*(/[Q2*RST*RN3]));
        Q3  = /(SN3*(/[RN3*Q3*RST]));

        SN4 = /(CLK*RST*(/(SN4*(/[Q3*RST*RN4]))));
        RN4 = /(SN4*CLK*(/[Q3*RST*RN4]));
        Q4  = /(SN4*(/[RN4*Q4*RST]));

        SN5 = /(CLK*RST*(/(SN5*(/[Q4*RST*RN5]))));
        RN5 = /(SN5*CLK*(/[Q4*RST*RN5]));
        Q5  = /(SN5*(/[RN5*Q5*RST]));

        SN6 = /(CLK*RST*(/(SN6*(/[Q5*RST*RN6]))));
        RN6 = /(SN6*CLK*(/[Q5*RST*RN6]));
        Q6  = /(SN6*(/[RN6*Q6*RST]));

        SN7 = /(CLK*RST*(/(SN7*(/[Q6*RST*RN7]))));
        RN7 = /(SN7*CLK*(/[Q6*RST*RN7]));
        Q7  = /(SN7*(/[RN7*Q7*RST]));

        O0 = Q0;
        O1 = Q1;
        O2 = Q2;
        O3 = Q3;
        O4 = Q4;
        O5 = Q5;
        O6 = Q6;
        O7 = Q7;

        "3 D-TYPE FLIP FLOPS CONNECTED AS A RIPPLE COUNTER"

        CSN0 = /(CLK*RST*(/(CSN0*(/[CQN0*RST*CRN0]))));
        CRN0 = /(CSN0*CLK*(/[CQN0*RST*CRN0]));
        CQ0  = /(CSN0*CQN0);
        CQN0 = /(CRN0*CQ0*RST);

        CSN1 = /(CQN0*RST*(/(CSN1*(/[CQN1*RST*CRN1]))));
        CRN1 = /(CSN1*CQN0*(/[CQN1*RST*CRN1]));
        CQ1  = /(CSN1*CQN1);
        CQN1 = /(CRN1*CQ1*RST);

        CSN2 = /(CQN1*RST*(/(CSN2*(/[CQN2*RST*CRN2]))));
        CRN2 = /(CSN2*CQN1*(/[CQN2*RST*CRN2]));          TB03950S
        CQ2  = /(CSN2*CQN2);
        CQN2 = /(CRN2*CQ2*RST);


"2 D-TYPE FLIP FLOPS USED FOR PATTERN SEQUENCE DETECTION.
Sequence to be detected is 16 bits - 55AA Hex.
When the pattern is detected, pin det2 will go high.

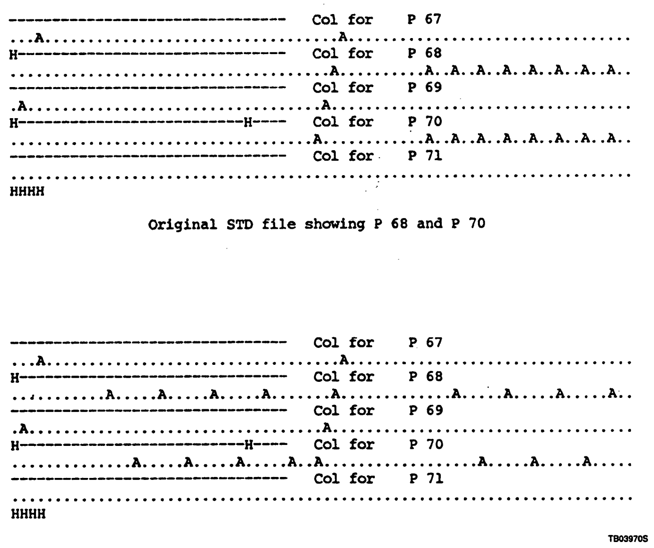
In this example, both pattern 1 and pattern 2 are set to FF hex. To
change the pattern to 55AA, the STD file (P68 and P70) was edited using
FTE. This was necessary because AMAZE 1.6 only allows 40 internal labels,
so it was not possible to reference the QN nodes of the shift register
flip-flops."


        PSN0 = /(CQN2*RST*(/(PSN0*(/[PAT1*RST*PRN0]))));
        PRN0 = /(PSN0*CQN2*(/[PAT1*RST*PRN0]));
        DET1N = (PSN0*/DET1);
        DET1 = (PRN0*/DET1N*RST);

        PSN1 = /(CQN2*RST*(/(PSN1*(/[PAT2*DET1*RST*PRN1]))));
        PRN1 = /(PSN1*CQN2*(/[PAT2*DET1*RST*PRN1]));
        DET2N = (PSN1*/DET2);
        DET2 = (PRN1*/DET2N*RST);

                                                                TB03960S
```

Figure 6.27 8-Bit Shifter Boolean Equations (Continued)



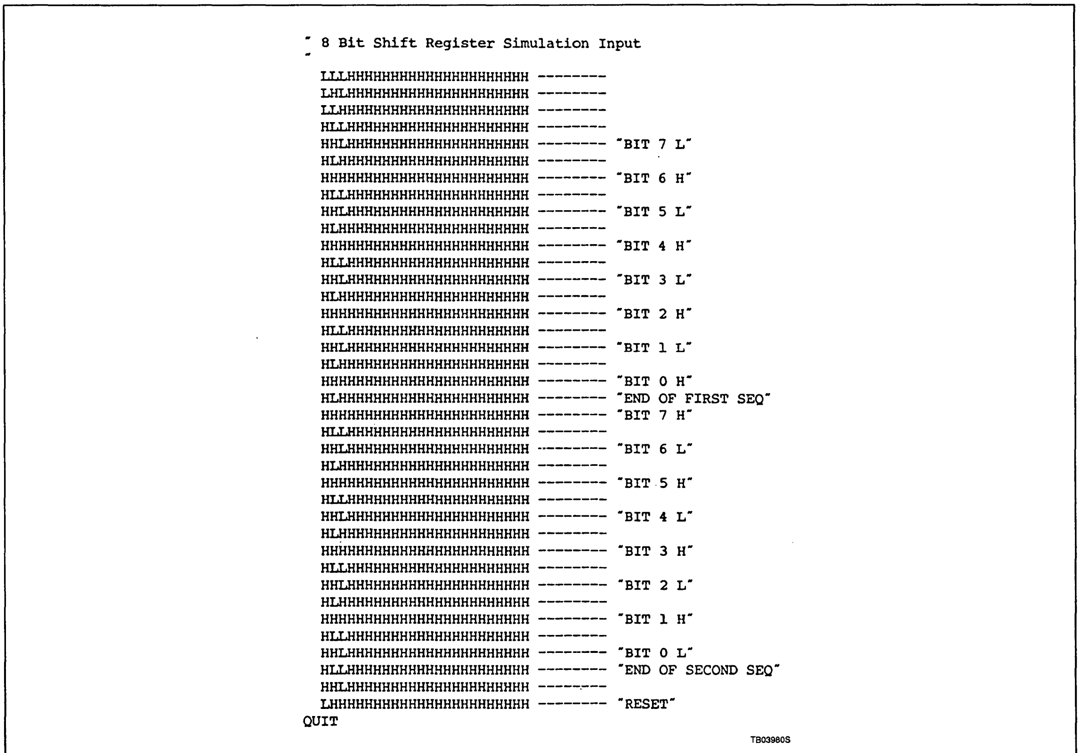
```
--------------------------------   Col for    P 67
...A..................................A.................................
H-------------------------------   Col for    P 68
.....................................A..........A..A..A..A..A..A..A..A..
--------------------------------   Col for    P 69
.A..................................A...................................
H--------------------------H----   Col for    P 70
...................................A............A..A..A..A..A..A..A..A..
--------------------------------   Col for    P 71
........................................................................
HHHH
```

Original STD file showing P 68 and P 70

```
--------------------------------   Col for    P 67
...A..................................A.................................
H-------------------------------   Col for    P 68
...........A.....A.....A.....A.......A.............A.....A.....A.....A..
--------------------------------   Col for    P 69
.A..................................A...................................
H--------------------------H----   Col for    P 70
..............A.....A.....A.....A..A..................A.....A.....A.....
--------------------------------   Col for    P 71
........................................................................
HHHH
```

TB03970S

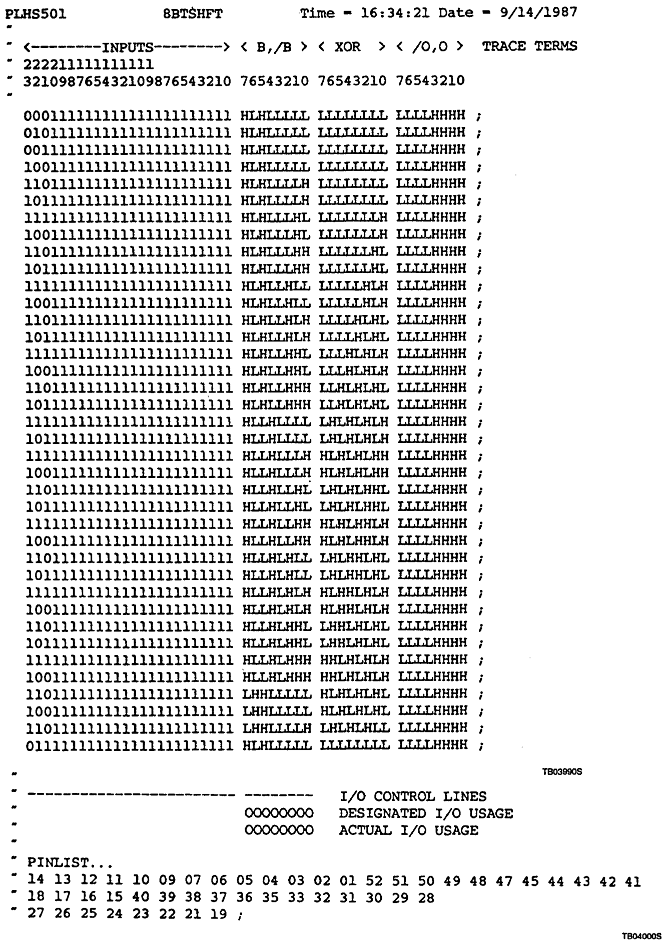
Figure 6.28 Portion of STD Files



```
" 8 Bit Shift Register Simulation Input
"
  LLLHHHHHHHHHHHHHHHHHHHHH --------
  LHLHHHHHHHHHHHHHHHHHHHHH --------
  LLHHHHHHHHHHHHHHHHHHHHHH --------
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 7 L"
  HLHHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 6 H"
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 5 L"
  HLHHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 4 H"
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 3 L"
  HLHHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 2 H"
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 1 L"
  HLHHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 0 H"
  HLHHHHHHHHHHHHHHHHHHHHHH -------- "END OF FIRST SEQ"
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 7 H"
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 6 L"
  HLHHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 5 H"
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 4 L"
  HLHHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 3 H"
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 2 L"
  HLHHHHHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "BIT 1 H"
  HLLHHHHHHHHHHHHHHHHHHHHH --------
  HHLHHHHHHHHHHHHHHHHHHHHH -------- "BIT 0 L"
  HLLHHHHHHHHHHHHHHHHHHHHH -------- "END OF SECOND SEQ"
  HHLHHHHHHHHHHHHHHHHHHHHH --------
  LHHHHHHHHHHHHHHHHHHHHHHH -------- "RESET"
QUIT
```

TB03980S

Figure 6.29 8-Bit Shifter Simulation Input File



```
PLHS501          8BT$HFT        Time - 16:34:21 Date - 9/14/1987
"
" <--------INPUTS--------> < B,/B > < XOR  > < /O,O >  TRACE TERMS
" 222211111111111
" 321098765432109876543210 76543210 76543210 76543210
"
  000111111111111111111111 HLHLLLLL LLLLLLLL LLLLHHHH ;
  010111111111111111111111 HLHLLLLL LLLLLLLL LLLLHHHH ;
  001111111111111111111111 HLHLLLLL LLLLLLLL LLLLHHHH ;
  100111111111111111111111 HLHLLLLL LLLLLLLL LLLLHHHH ;
  110111111111111111111111 HLHLLLLH LLLLLLLL LLLLHHHH ;
  101111111111111111111111 HLHLLLLH LLLLLLLL LLLLHHHH ;
  111111111111111111111111 HLHLLLHL LLLLLLLH LLLLHHHH ;
  100111111111111111111111 HLHLLLHL LLLLLLLH LLLLHHHH ;
  110111111111111111111111 HLHLLLHH LLLLLLHL LLLLHHHH ;
  101111111111111111111111 HLHLLLHH LLLLLLHL LLLLHHHH ;
  111111111111111111111111 HLHLLHLL LLLLLHLH LLLLHHHH ;
  100111111111111111111111 HLHLLHLL LLLLLHLH LLLLHHHH ;
  110111111111111111111111 HLHLLHLH LLLLHLHL LLLLHHHH ;
  101111111111111111111111 HLHLLHLH LLLLHLHL LLLLHHHH ;
  111111111111111111111111 HLHLLHHL LLLHLHLH LLLLHHHH ;
  100111111111111111111111 HLHLLHHL LLLHLHLH LLLLHHHH ;
  110111111111111111111111 HLHLLHHH LLHLHLHL LLLLHHHH ;
  101111111111111111111111 HLHLLHHH LLHLHLHL LLLLHHHH ;
  111111111111111111111111 HLLHLLLL LHLHLHLH LLLLHHHH ;
  101111111111111111111111 HLLHLLLL LHLHLHLH LLLLHHHH ;
  111111111111111111111111 HLLHLLLH HLHLHLHH LLLLHHHH ;
  100111111111111111111111 HLLHLLLH HLHLHLHH LLLLHHHH ;
  110111111111111111111111 HLLHLLHL LHLHLHHL LLLLHHHH ;
  101111111111111111111111 HLLHLLHL LHLHLHHL LLLLHHHH ;
  111111111111111111111111 HLLHLLHH HLHLHHLH LLLLHHHH ;
  100111111111111111111111 HLLHLLHH HLHLHHLH LLLLHHHH ;
  110111111111111111111111 HLLHLHLL LHLHHLHL LLLLHHHH ;
  101111111111111111111111 HLLHLHLL LHLHHLHL LLLLHHHH ;
  111111111111111111111111 HLLHLHLH HLHHLHLH LLLLHHHH ;
  100111111111111111111111 HLLHLHLH HLHHLHLH LLLLHHHH ;
  110111111111111111111111 HLLHLHHL LHHLHLHL LLLLHHHH ;
  101111111111111111111111 HLLHLHHL LHHLHLHL LLLLHHHH ;
  111111111111111111111111 HLLHLHHH HHLHLHLH LLLLHHHH ;
  100111111111111111111111 HLLHLHHH HHLHLHLH LLLLHHHH ;
  110111111111111111111111 LHHLLLLL HLHLHLHL LLLLHHHH ;
  100111111111111111111111 LHHLLLLL HLHLHLHL LLLLHHHH ;
  110111111111111111111111 LHHLLLLH LHLHLHLL LLLLHHHH ;
  011111111111111111111111 HLHLLLLL LLLLLLLL LLLLHHHH ;
```

TB03990S

```
"
" ------------------------ --------   I/O CONTROL LINES
"                          OOOOOOOO   DESIGNATED I/O USAGE
"                          OOOOOOOO   ACTUAL I/O USAGE
"
" PINLIST...
" 14 13 12 11 10 09 07 06 05 04 03 02 01 52 51 50 49 48 47 45 44 43 42 41
" 18 17 16 15 40 39 38 37 36 35 33 32 31 30 29 28
" 27 26 25 24 23 22 21 19 ;
```

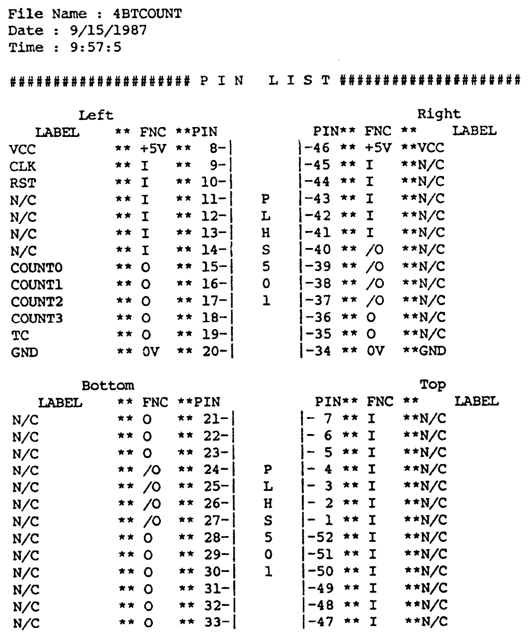
TB04000S

Figure 6.30 8-Bit Shifter Simulation Log File

4-BIT SYNCHRONOUS COUNTER

This counter produces a binary count on outputs Count3 – Count0. Note the required reset (RST) input to initialize all of the flip-flops. The inputs for each flip-flop were first determined by drawing the desired output waveforms. Next, Karnaugh maps were used to reduce the number of terms and determine the logic equations for the input to each flip-flop. This technique could be used to construct a counter whose outputs produce some count other than binary.

The simulation only consists of a reset, followed by a number of clocks to count from 0 through 15 and back to 0.



```
File Name : 4BTCOUNT
Date : 9/15/1987
Time : 9:57:5

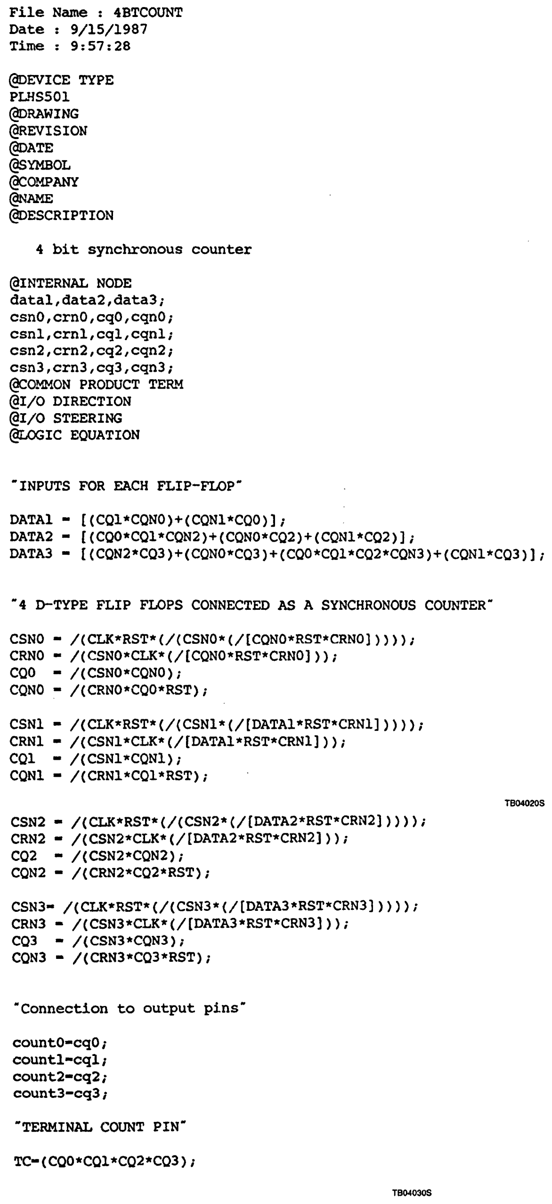
##################### P I N   L I S T #####################

        Left                                           Right
  LABEL      ** FNC **PIN               PIN** FNC **      LABEL
VCC          ** +5V **  8-|            |-46 ** +5V **VCC
CLK          ** I   **  9-|            |-45 ** I   **N/C
RST          ** I   ** 10-|            |-44 ** I   **N/C
N/C          ** I   ** 11-|    P       |-43 ** I   **N/C
N/C          ** I   ** 12-|    L       |-42 ** I   **N/C
N/C          ** I   ** 13-|    H       |-41 ** I   **N/C
N/C          ** I   ** 14-|    S       |-40 ** /O  **N/C
COUNT0       ** O   ** 15-|    5       |-39 ** /O  **N/C
COUNT1       ** O   ** 16-|    0       |-38 ** /O  **N/C
COUNT2       ** O   ** 17-|    1       |-37 ** /O  **N/C
COUNT3       ** O   ** 18-|            |-36 ** O   **N/C
TC           ** O   ** 19-|            |-35 ** O   **N/C
GND          ** OV  ** 20-|            |-34 ** OV  **GND

        Bottom                                         Top
  LABEL      ** FNC **PIN               PIN** FNC **      LABEL
N/C          ** O   ** 21-|            |- 7 ** I   **N/C
N/C          ** O   ** 22-|            |- 6 ** I   **N/C
N/C          ** O   ** 23-|            |- 5 ** I   **N/C
N/C          ** /O  ** 24-|    P       |- 4 ** I   **N/C
N/C          ** /O  ** 25-|    L       |- 3 ** I   **N/C
N/C          ** /O  ** 26-|    H       |- 2 ** I   **N/C
N/C          ** /O  ** 27-|    S       |- 1 ** I   **N/C
N/C          ** O   ** 28-|    5       |-52 ** I   **N/C
N/C          ** O   ** 29-|    0       |-51 ** I   **N/C
N/C          ** O   ** 30-|    1       |-50 ** I   **N/C
N/C          ** O   ** 31-|            |-49 ** I   **N/C
N/C          ** O   ** 32-|            |-48 ** I   **N/C
N/C          ** O   ** 33-|            |-47 ** I   **N/C
```

TB04010S

Figure 6.31 4-Bit Counter Pin List



```
File Name : 4BTCOUNT
Date : 9/15/1987
Time : 9:57:28

@DEVICE TYPE
PLHS501
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION

   4 bit synchronous counter

@INTERNAL NODE
data1,data2,data3;
csn0,crn0,cq0,cqn0;
csn1,crn1,cq1,cqn1;
csn2,crn2,cq2,cqn2;
csn3,crn3,cq3,cqn3;
@COMMON PRODUCT TERM
@I/O DIRECTION
@I/O STEERING
@LOGIC EQUATION


"INPUTS FOR EACH FLIP-FLOP"

DATA1 = [(CQ1*CQN0)+(CQN1*CQ0)];
DATA2 = [(CQ0*CQ1*CQN2)+(CQN0*CQ2)+(CQN1*CQ2)];
DATA3 = [(CQN2*CQ3)+(CQN0*CQ3)+(CQ0*CQ1*CQ2*CQN3)+(CQN1*CQ3)];


"4 D-TYPE FLIP FLOPS CONNECTED AS A SYNCHRONOUS COUNTER"

CSN0 = /(CLK*RST*(/(CSN0*(/[CQN0*RST*CRN0]))));
CRN0 = /(CSN0*CLK*(/[CQN0*RST*CRN0]));
CQ0  = /(CSN0*CQN0);
CQN0 = /(CRN0*CQ0*RST);

CSN1 = /(CLK*RST*(/(CSN1*(/[DATA1*RST*CRN1]))));
CRN1 = /(CSN1*CLK*(/[DATA1*RST*CRN1]));
CQ1  = /(CSN1*CQN1);
CQN1 = /(CRN1*CQ1*RST);
```

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```
CSN2 = /(CLK*RST*(/(CSN2*(/[DATA2*RST*CRN2]))));
CRN2 = /(CSN2*CLK*(/[DATA2*RST*CRN2]));
CQ2  = /(CSN2*CQN2);
CQN2 = /(CRN2*CQ2*RST);

CSN3= /(CLK*RST*(/(CSN3*(/[DATA3*RST*CRN3]))));
CRN3 = /(CSN3*CLK*(/[DATA3*RST*CRN3]));
CQ3  = /(CSN3*CQN3);
CQN3 = /(CRN3*CQ3*RST);


"Connection to output pins"

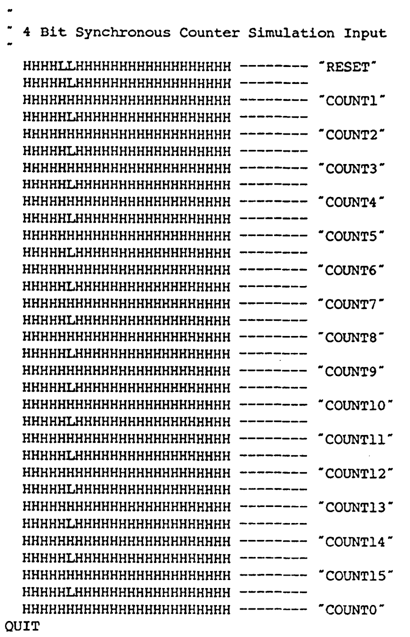
count0=cq0;
count1=cq1;
count2=cq2;
count3=cq3;

"TERMINAL COUNT PIN"

TC=(CQ0*CQ1*CQ2*CQ3);
```

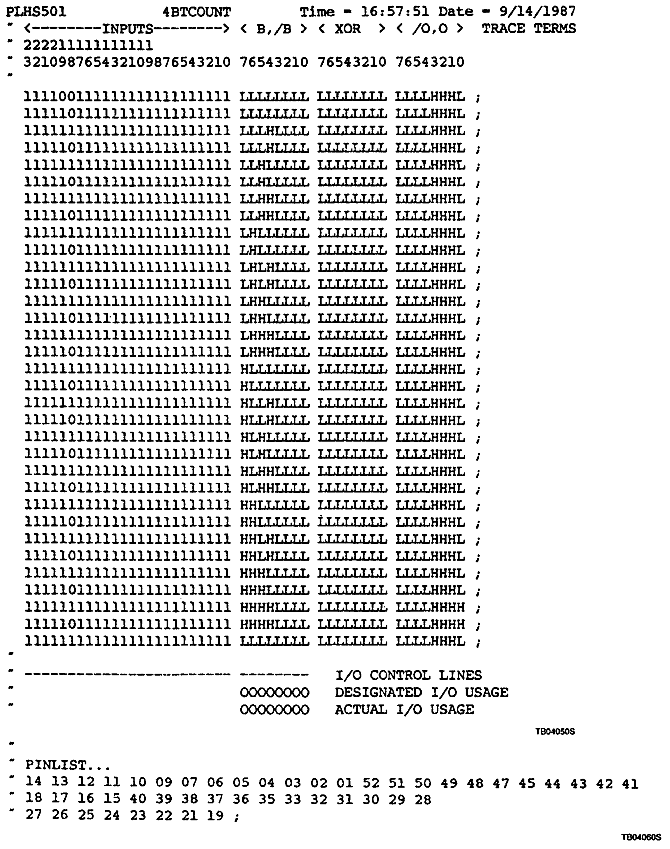
TB04030S

Figure 6.32 4-Bit Counter Boolean Equations



```
"
" 4 Bit Synchronous Counter Simulation Input
"
  HHHHLLHHHHHHHHHHHHHHHHHH -------- "RESET"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT1"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT2"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT3"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT4"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT5"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT6"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT7"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT8"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT9"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT10"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT11"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT12"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT13"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT14"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT15"
  HHHHHLHHHHHHHHHHHHHHHHHH --------
  HHHHHHHHHHHHHHHHHHHHHHHH -------- "COUNT0"
QUIT
```

Figure 6.33 4-Bit Counter Simulation Input File



```
PLHS501          4BTCOUNT        Time = 16:57:51 Date = 9/14/1987
" <--------INPUTS--------> < B,/B > < XOR  > < /O,O >  TRACE TERMS
" 222211111111111
" 321098765432109876543210 76543210 76543210 76543210
"
  111100111111111111111111 LLLLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LLLLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 LLLHLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LLLHLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 LLHLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LLHLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 LLHHLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LLHHLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 LHLLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LHLLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 LHLHLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LHLHLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 LHHLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LHHLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 LHHHLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 LHHHLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HLLLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 HLLLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HLLHLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 HLLHLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HLHLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 HLHLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HLHHLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 HLHHLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HHLLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 HHLLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HHLHLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 HHLHLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HHHLLLLL LLLLLLLL LLLLHHHL ;
  111110111111111111111111 HHHLLLLL LLLLLLLL LLLLHHHL ;
  111111111111111111111111 HHHHLLLL LLLLLLLL LLLLHHHH ;
  111110111111111111111111 HHHHLLLL LLLLLLLL LLLLHHHH ;
  111111111111111111111111 LLLLLLLL LLLLLLLL LLLLHHHL ;
"
" ------------------------ --------   I/O CONTROL LINES
"                          00000000   DESIGNATED I/O USAGE
"                          00000000   ACTUAL I/O USAGE
```

TB04050S

```
"
" PINLIST...
" 14 13 12 11 10 09 07 06 05 04 03 02 01 52 51 50 49 48 47 45 44 43 42 41
" 18 17 16 15 40 39 38 37 36 35 33 32 31 30 29 28
" 27 26 25 24 23 22 21 19 ;
```

TB04060S

Figure 6.34 4-Bit Counter Simulation Log File

Bibliography

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Section 10
Package Outlines

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A PLASTIC: Leaded Chip Carrier 10-3
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FA CERAMIC: Dual-In-Line With Quartz Window 10-8
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Package Outlines

PLASTIC PLCC

1. Package dimensions conform to JEDEC specifications for standard Leaded Chip Carrier outline (PLCC) package.
2. Controlling dimensions are given in inches with dimensions in millimeters contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M - 1982.
4. "D-E" and "F-G" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006″) on any side.
5. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
6. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
7. Body material: Plastic (Epoxy).
8. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test condition for these values follow:

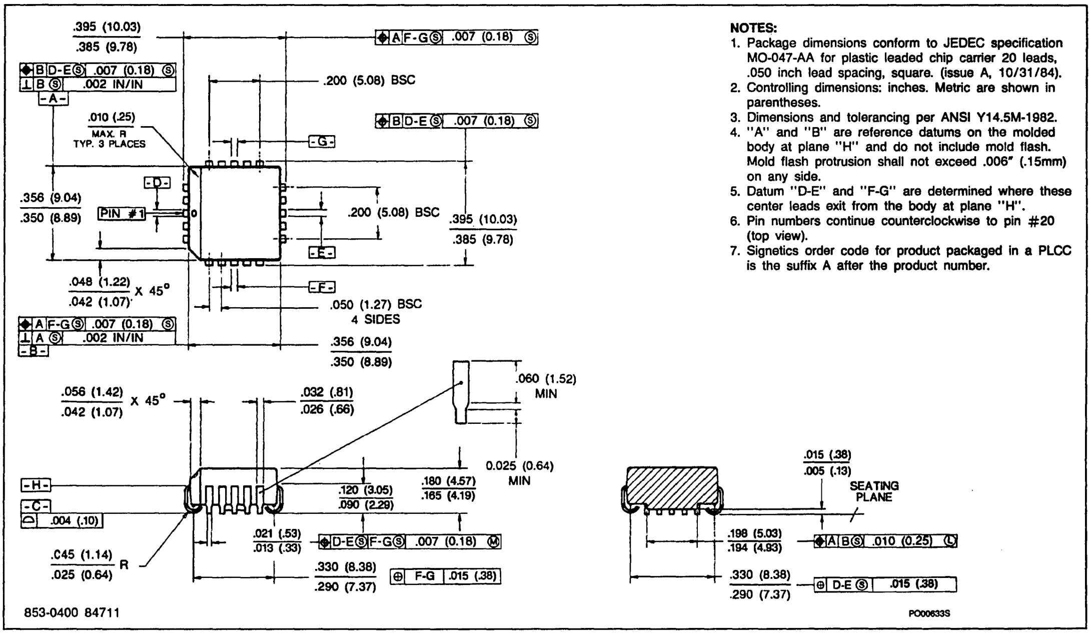
   Test Ambient — Still Air
   Test Fixture — θ_{JA} - Glass epoxy test board (2.24″ × 2.24″ × 0.062″.)
   θ_{JC} - Water cooled heat sink

PLASTIC LEADED CHIP CARRIER (PLCC)

NO. OF LEADS	PACKAGE CODE	DESCRIPTION
20	A	350mil-wide
28	A	450mil-wide
52	A	750mil-wide
68	A	950mil-wide

TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)			
Die Size	Power Dissipation (W)	Average θ_{JA}	Average θ_{JC}
20K	.75	70	30
25K	1.0	61	23
50K	1.0	42	15

20-PIN PLASTIC PLCC (A PACKAGE)

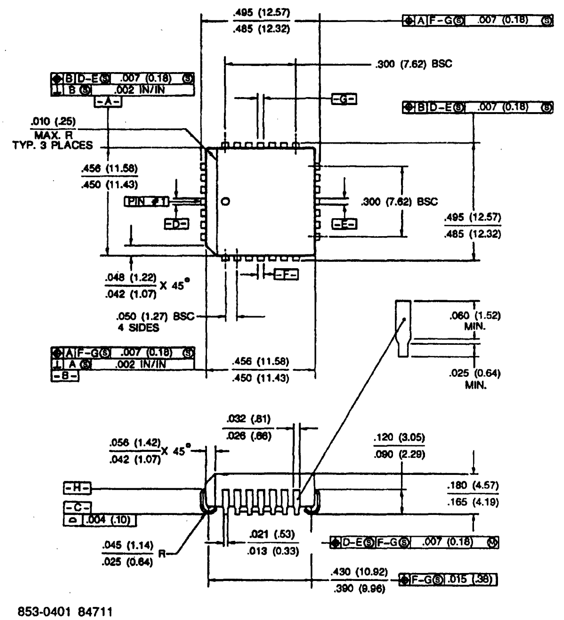


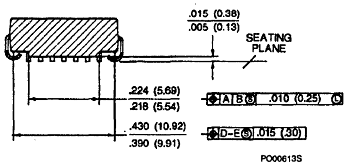
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006″ (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #20 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

Package Outlines

28-PIN PLASTIC PLCC (A PACKAGE)



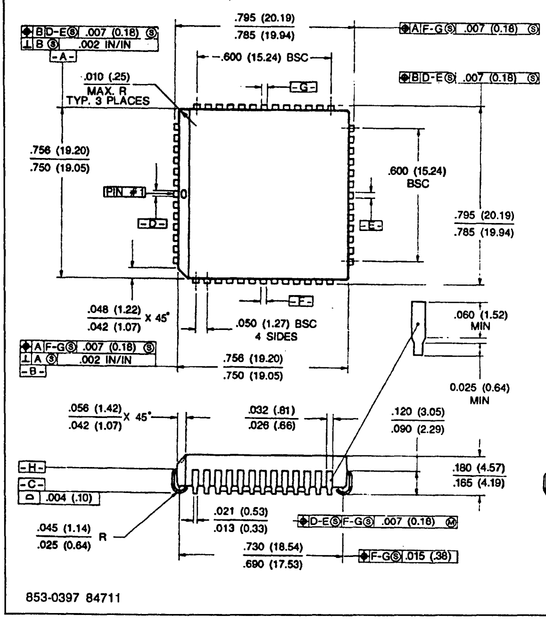


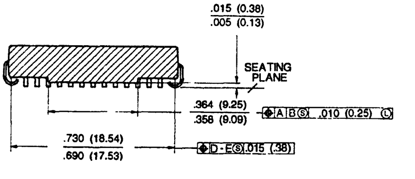
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #28 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0401 84711

52-PIN PLASTIC PLCC (A PACKAGE)





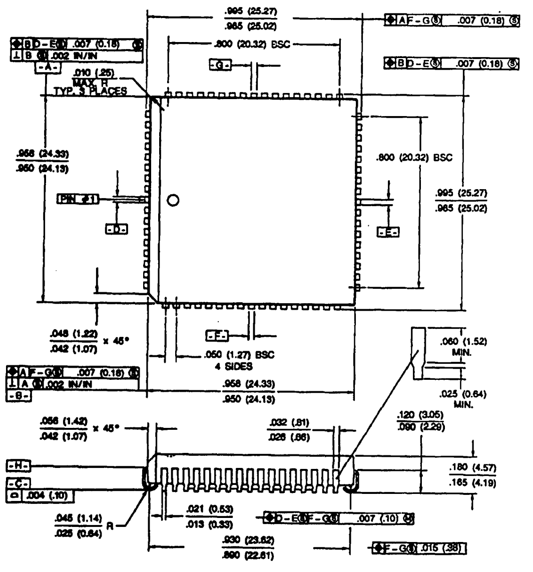
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #20 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0397 84711

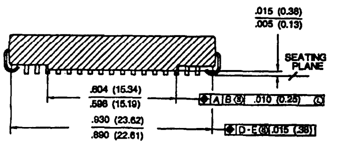
Package Outlines

68-PIN PLASTIC LEADED CHIP CARRIER



NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AE for plastic leaded chip carrier 68 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #68 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.



853-0398 84711

PO00623S

Package Outlines

HERMETIC CERDIP

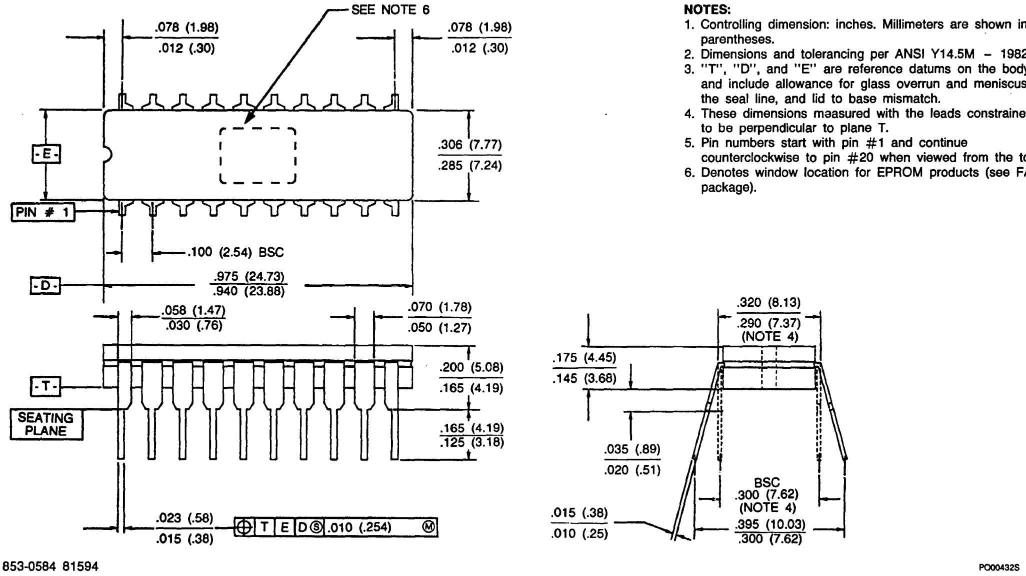
1. Package dimensions conform to JEDEC specifications for standard Ceramic Dual Inline (Cerdip) package.
2. Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M - 1982.
4. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Lead material: ASTM alloy F-30 (Alloy 42) or equivalent – tin plated or solder dipped.
7. Body Material: Ceramic with glass seal at leads.
8. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test condition for these values follow:
   Test Ambient — Still Air
   Test Fixture — θ_{JA} – Textool ZIF socket with 0.04″ stand-off
   θ_{JC} – Water cooled heat sink

HERMETIC DUAL-IN-LINE PACKAGES

NO. OF LEADS	PACKAGE CODE	DESCRIPTION
20	F	300mil-wide
24	F	300mil-wide
28	F	600mil-wide

TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)			
Die Size	Power Dissipation (W)	Average θ_{JA}	Average θ_{JC}
20K	.75	70	7.8
25K	1.0	62	6.9
30K	1.0	48	6.3

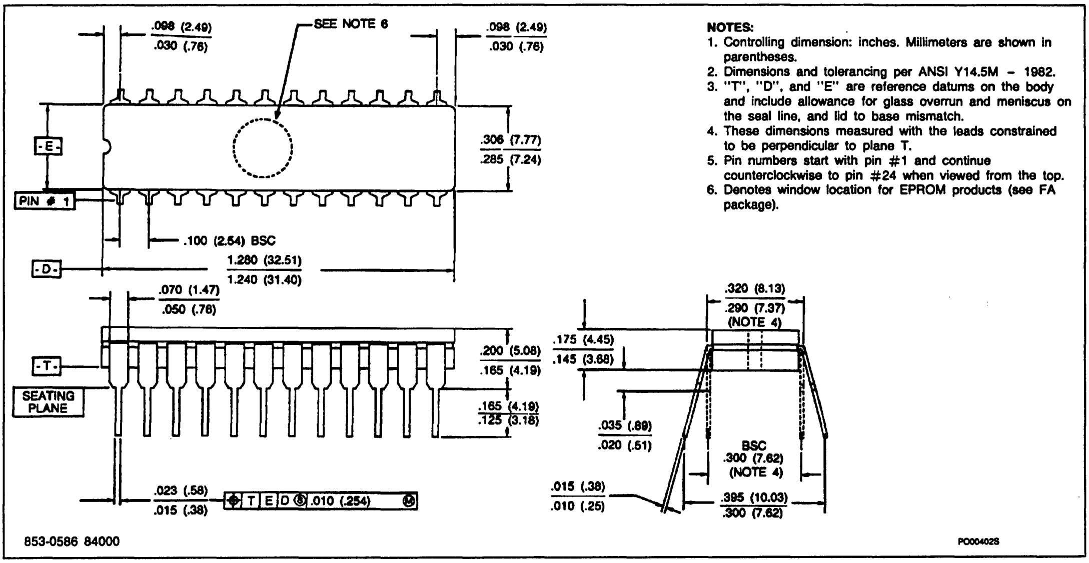
20-PIN CERAMIC DIP (F PACKAGE)



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.
6. Denotes window location for EPROM products (see FA package).

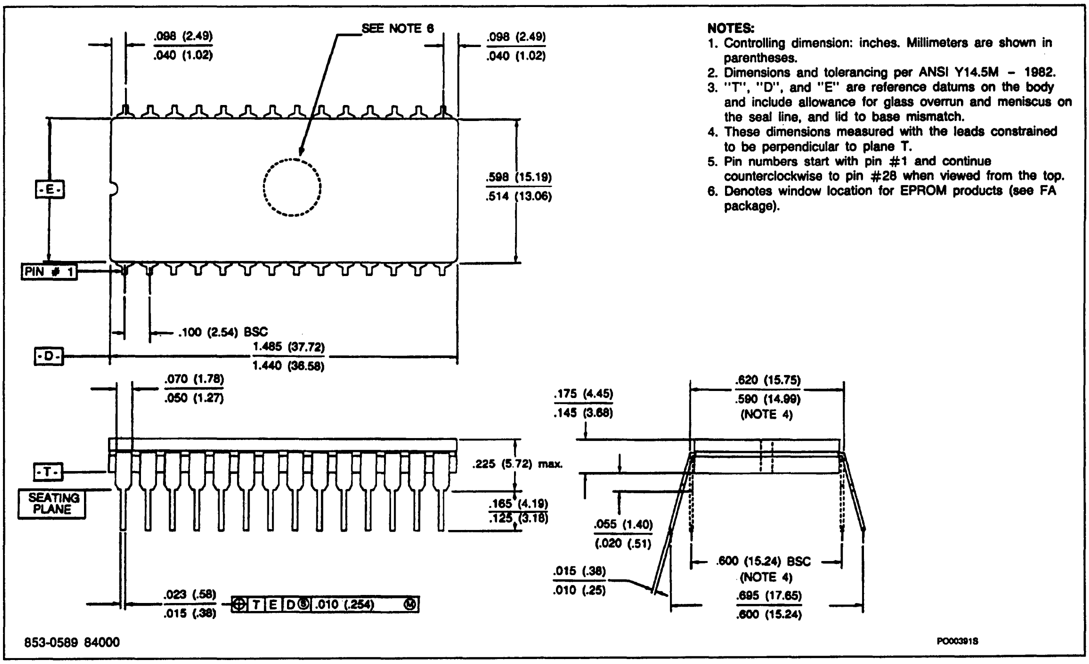
Package Outlines

24-PIN CERAMIC DIP (F PACKAGE)



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products (see FA package).

28-PIN CERAMIC DIP (F PACKAGE)



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM products (see FA package).

Package Outlines

HERMETIC CERDIP WITH QUARTZ WINDOW

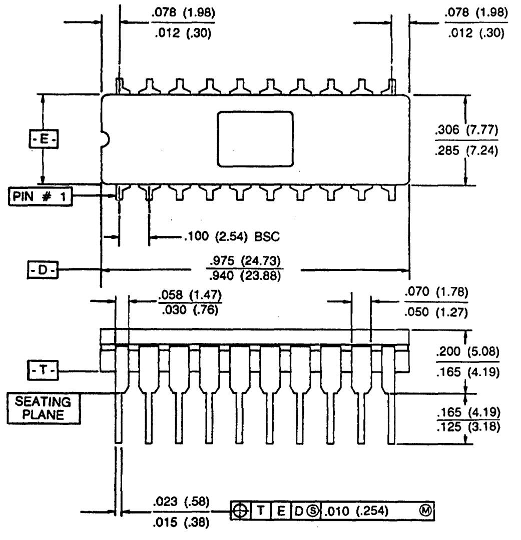
1. Package dimensions conform to JEDEC specifications for standard Ceramic Dual Inline (Cerdip) package.
2. Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M - 1982.
4. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Lead material: ASTM alloy F-30 (Alloy 42) or equivalent - tin plated or solder dipped.
7. Body Material: Ceramic with glass seal at leads.
8. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test condition for these values follow:
   Test Ambient — Still Air
   Test Fixture — θ_{JA} - Textool ZIF socket with 0.04" standoff
   θ_{JC} - Water cooled heat sink

HERMETIC DUAL-IN-LINE PACKAGES WITH QUARTZ WINDOW

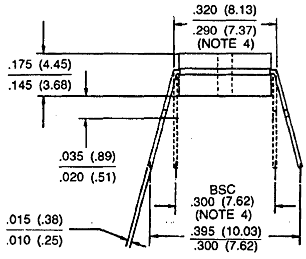
NO. OF LEADS	PACKAGE CODE	DESCRIPTION
20	FA	300mil-wide
24	FA	300mil-wide
28	FA	600mil-wide

TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)			
Die Size	Power Dissipation (W)	Average θ_{JA}	Average θ_{JC}
25K	.5	67	7.8
30K	.5	52	7.0

20-PIN CERAMIC DIP WITH QUARTZ WINDOW (FA PACKAGE)



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

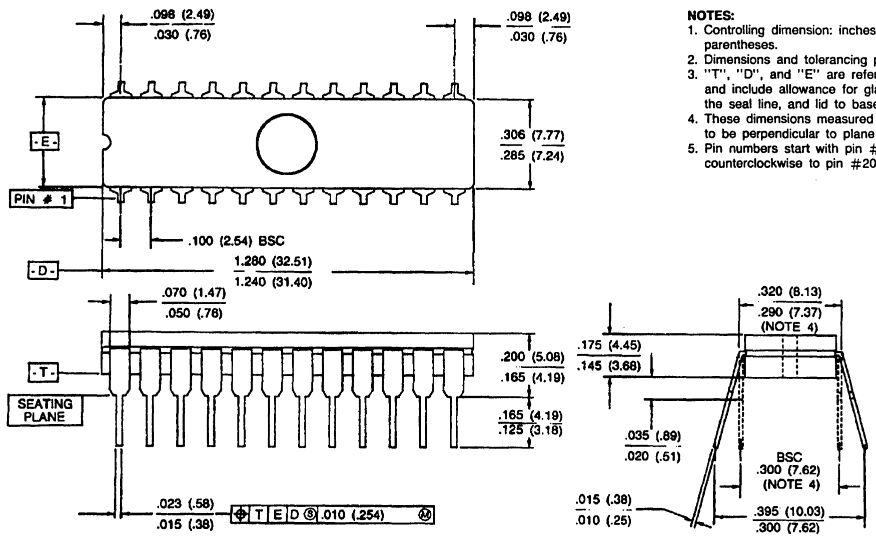


853-0584 81594

PO00433S

Package Outlines

24-PIN CERAMIC DIP WITH QUARTZ WINDOW (FA PACKAGE)

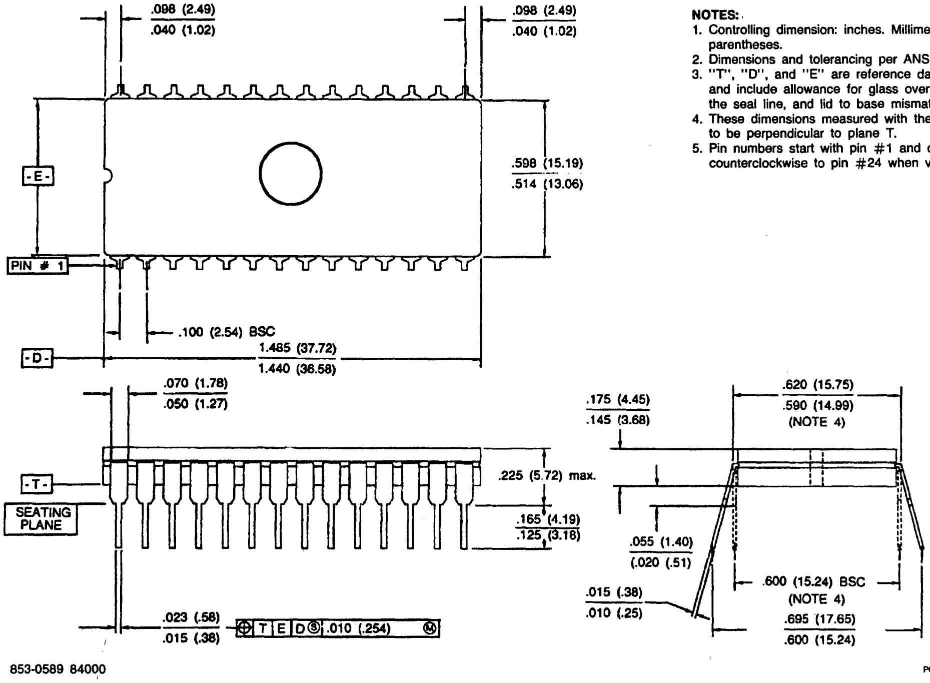


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0586 84000

PO00403S

28-PIN CERAMIC DIP WITH QUARTZ WINDOW (FA PACKAGE)



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0589 84000

PO00392S

Package Outlines

PLASTIC DIP

1. Package dimensions conform to JEDEC specification MS-001-AA for standard Plastic Dual Inline (DIP) package.
2. Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M - 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.01 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
7. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
8. Body material: Plastic (Epoxy)
9. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test condition for these values follow:

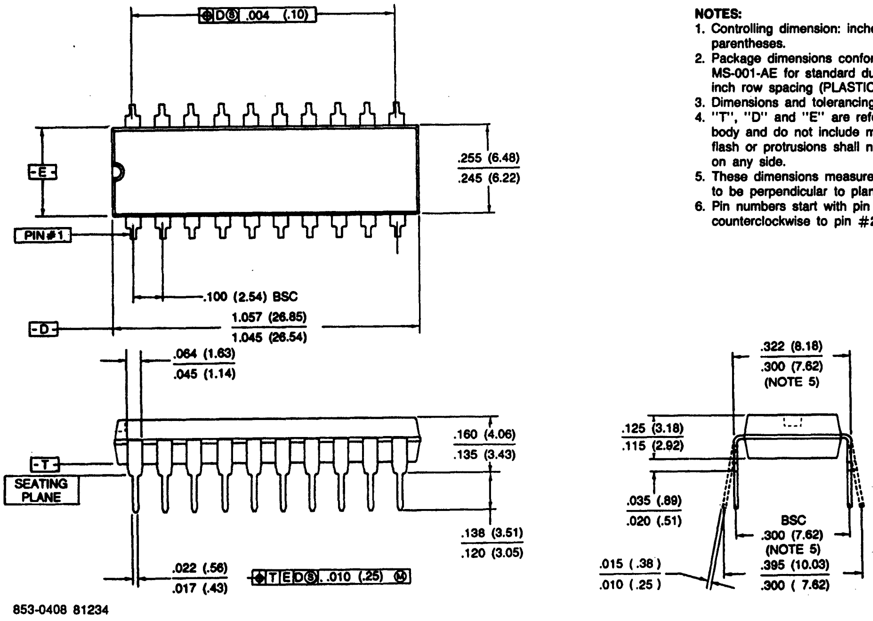
   Test Ambient — Still Air
   Test Fixture — θ_{JA} – Textool ZIF socket with 0.04" standoff
   θ_{JC} – Water cooled heat sink

PLASTIC DUAL-IN-LINE PACKAGES

NO. OF LEADS	PACKAGE CODE	DESCRIPTION
20	N	Cu. Lead Frame 300mil-wide
24	N	Cu. Lead Frame 300mil-wide
28	N	Cu. Lead Frame 600mil-wide

TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)			
Die Size	Power Dissipation (W)	Average θ_{JA}	Average θ_{JC}
20K	.75	61	25
25K	1.0	55	25
50K	1.0	46	18

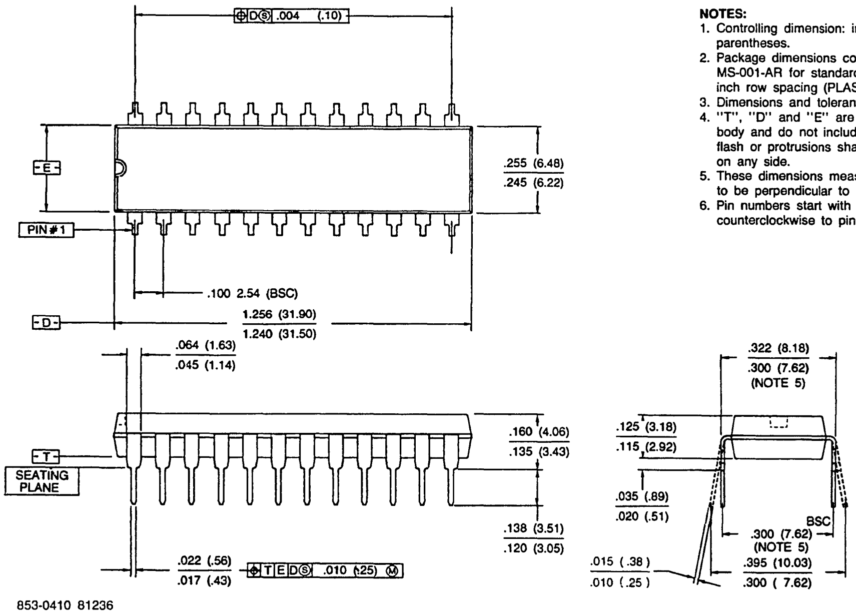
20-PIN PLASTIC (N PACKAGE)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

Package Outlines

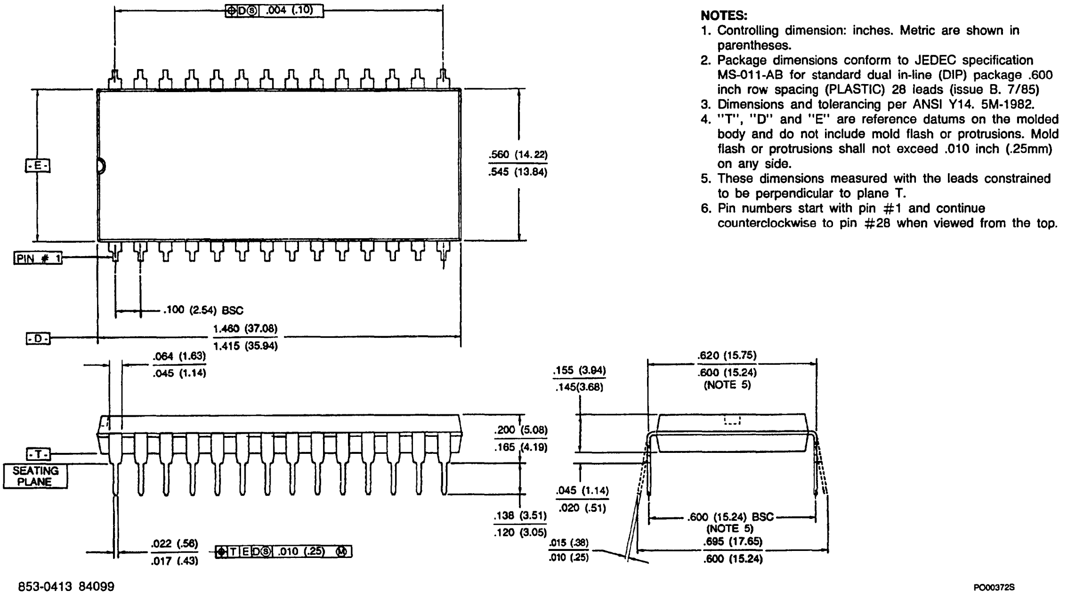
24-PIN PLASTIC (N PACKAGE)



NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AR for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

28-PIN PLASTIC (N PACKAGE)



NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

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