Interface Products Catalog

Sipex

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

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For information on any of the following SIPEX Data Conversion Products, please contact the SIPEX Literature Department at (508) 667-8700.

Model **Description**

Sampling Analog-to-Digital Converters

HS574A ... 12-Bit, 25µs
SP574B ... 12-Bit, 25µs; 20kHz Nyquist Frequency
SP674A ... 12-Bit, 15µs
SP674B ... 12-Bit, 15µs; 33kHz Nyquist Frequency
SP774B ... 12-Bit, 8µs; 62.5kHz Nyquist Frequency
SP1674B . 12-Bit, 10µs; 50kHz Nyquist Frequency
SP7800A . 12-Bit, 3µs; Single +5V Supply
SP8503 .... 12-Bit, 3µs; Bipolar Input
SP8505 .... 12-Bit, 5µs; Bipolar Input
SP8510 .... 12-Bit, 10µs; Bipolar Input
SP8603 .... 12-Bit, 3µs; Unipolar Input
SP8605 .... 12-Bit, 5µs; Unipolar Input
SP8610 .... 12-Bit, 10µs; Unipolar Input

Digital-to-Analog Converters

HS3120 ... 12-Bit, 2µs, Latched, 4-Quadrant Multiplying, Current Output
HS3140 ... 14-Bit, 2µs, 4-Quadrant Multiplying, Current Output
HS3160 ... 16-Bit, 2µs, 4-Quadrant Multiplying, Current Output
SP7512 .... 12-Bit, 2µs, Double-Buffered, 4-Quadrant Multiplying, Current Output
SP7514 .... 14-Bit, 2µs, 4-Quadrant Multiplying, Current Output
SP7516 .... 16-Bit, 2µs, 4-Quadrant Multiplying, Current Output
HS7541A . 12-Bit, 2µs, 4-Quadrant Multiplying, Current Output
SP7545 .... 12-Bit, 2µs, Buffered, 4-Quadrant Multiplying, Current Output
HS7584 ... 12-Bit, 2µs, Quad, Double-Buffered, 4-Quadrant Multiplying, Current Output with Independent Reference Inputs
SP9316 .... 16-Bit, 2µs, Latched, 4-Quadrant Multiplying, Current Output
SP9502 .... 12-Bit, 4µs, Dual, 4-Quadrant Multiplying, Voltage Output
SP9504 .... 12-Bit, 4µs, Quad, 4-Quadrant Multiplying, Voltage Output
SP9602 .... 12-Bit, 4µs, Low-Power; Dual, 4-Quadrant Multiplying, Voltage Output
SP9604 .... 12-Bit, 4µs, Low-Power; Quad, 4-Quadrant Multiplying, Voltage Output
SP9841 .... 8-Bit, 0.7µs; Octal, 2-Quadrant Multiplying, Current Output with 8 Independent Reference Inputs
SP9842 .... 8-Bit, 0.7µs; Octal, Multiplying, Current Output with 4 pair of Reference Inputs

Data Acquisition Systems

SP8120 .... 8-Channel, 12-Bit, 100KHz, Parallel Out, Monolithic DAS
SP8121 .... 8-Channel, 12-Bit, 100KHz, Parallel Out, Monolithic DAS
SP8480 .... 8-Channel, 12-Bit, 100KHz, 8/4 Nibble Out, Monolithic DAS
SP8481 .... 8-Ch., 12-Bit, 100KHz, Latched MUX, Nibble Out, Monolithic DAS

Advanced Information

SP9840 .... 8-Bit, 1µs; Octal, Multiplying, Voltage Output with 3-Wire Serial Interface and 8 Independent Reference Inputs
SP9843 .... 8-Bit, 1µs; Octal, Multiplying, Voltage Output with 3-Wire Serial Interface and 4 Pair of Reference Inputs

For information on any of the following SIPEX ASIC (Custom) Monolithics Products, please contact the SIPEX Literature Department at (508) 667-8700.

Model **Description**

SP2000 Analog Array Products

General Information
Introduction
Array General Description
Array Structure
Tiles
SP2000 Array Se**lection Guide**
SP2101 2x2 Analog Array
SP2103 4x2 Analog Array
SP2104 4x3 Analog Array
SP2105 4x4 Analog Array
SP2107 4x5 Analog Array
SP2000 Series Analog Array Components
20 Volt Process Specifications
35 Volt Process Specifications
General Process Specifications
Standard Package Options
SP2000 MacroCell Se**lection Guide**

Amplifiers

OPA1 ..... General Purpose OpAmp
OPA2 ..... General Purpose OpAmp
OPA3 ..... Precision OpAmp
OPA5 ..... Clamped–Output OpAmp
OPA6 ..... Video OpAmp
OPA8 ..... Low Voltage OpAmp
JOP27 ..... High Precision JFET OpAmp
JOP28 ..... Precision JFET OpAmp
JOP34 ..... General Purpose JFET OpAmp
JOP35 ..... Low Power JFET OpAmp

Multiplexing Amplifiers

MXA2 ..... 2–Channel Multiplexing Amplifier

Low Voltage OpAmps

LVA1 ..... Wide CMR, Low–Voltage OpAmp
LVA2 ..... Low–Voltage OpAmp

Buffers

BUF1 ..... Buffer/Operational Amplifier
JBF1 ..... JFET Buffer

Sample–and–Hold Amplifiers

SHA1 ..... Sample–and–Hold Amplifier & Switch

Tran**simpedance Amplifiers**

TZA1 ..... Transimpedance Amplifier

For information on any of the following SIPEX ASIC (Custom) Monolithics Products, please contact the SIPEX Literature Department at (508) 667-8700.

Model	Description
Comparators	
CMP1	..... Single–Supply TTL Comparator
CMP2	..... Split–Supply TTL Comparator
CMP4	..... Two–Input Window Comparator
Multipliers	
MLT1	..... Current Out, 4–Quadrant VCA
MLT2	..... Current Out, 4–Quadrant Multiplier
MLT3	..... Voltage Out, 4–Quadrant Multiplier
MLT4	..... Current Out, TTL In, 4–Quad. Multi.
Full–Wave Rectifiers	
FWR1	..... Current Source Out, F–W Rectifier
FWR2	..... Current Sink Out, F–W Rectifier
Bias **Generators**	
BAS1	..... IP and IPT Cell Bias Source
Logic **Gates**	
LBS1	..... CML Logic Bias Source
LBF1	..... CML Logic Input Buffer
NOR1	..... NOR/OR Gate, CML
Function Blocks	
CHP1	..... Charge Pump, Bipolar Output
Voltage References	
RBZ10	..... 10V Buried–Zener Reference
RBG10	.... 10V Band–Gap Reference
Analog Switch	
SWA2SP	. Precision Single–Pole, SIngle–Throw Analog Switch

SIPEX... EXCELLENCE IN SIGNAL PROCESSING

Sipex Corporation designs and manufactures Analog Signal Processing Circuits. Utilizing a broad range of technologies including CMOS, Bipolar and BiCMOS, **Sipex** has developed a wide range of monolithic products. **Sipex**'s Standard Products are focused primarily in two areas: Data Converters and Interface Circuits. The Interface Circuits consist of industry standard as well as proprietary products. Data Converter products cover a full range of D/A's, A/D's, and DAS' with primary focus on high speed, high resolution circuits. In addition to Sipex's broad standard product offering, the company designs and manufactures custom circuits for unique signal processing needs.

This catalog covers our standard Interface Product offering. If you would like our Data Conversion Products catalog or our ASIC (Custom) Monolithic Products catalog, please contact the **Sipex** Literature Department at 508–667–8700.

SIPEX INTERFACE PRODUCTS:

Single Interface

Sipex has been serving the +5V Only RS232 market since 1988. This product line does represent our core product offering and is enhanced and improved as needed to keep pace with the rigorous requirements of industry. In 1993 **Sipex** released the first product in a family of RS485 transceivers. The SP485 which is a half duplex RS485 transceiver was the first in a series of RS485 transceivers.

Multi-Mode Interface

Sipex entered the multimode serial interface market with the industry's first programmable RS232/422 transceiver in 1990. Based on this technology the 300 series was expanded to support RS232, RS422, and AppleTalk™. Single-chip transceivers supporting two interface modes gave us the entree into our newest series — the 500 series supports up to eleven (11) programmable interface standards integrated into easy to use, space saving, single chip solutions.

Whether it's our multimode transceivers or one of our many single interface products, Sipex is delivering affordable, reliable solutions to the market today.

RELIABILITY

Quality and reliability have long been inherent to our company. While the majority of our sales today are to Industrial customers, our roots were in the military markets, including demanding space applications.

The disciplines required to successfully service these markets have been carried into all **Sipex**'s products. Quality has always been a 'way of life' at **Sipex**. Outgoing quality levels of our monolithic products are better than 200ppm with our more mature products better than 100ppm. We are proud of our outgoing quality level and are continually striving to improve upon it.

Ordering Information

North America: Orders may be placed through our North American Sales office located at 22 Linnell Circle, Billerica, MA 01821 USA by telephone at 508–667–8700 or by fax at 508–670–9001. Product information may be obtained, and orders placed through **Sipex**'s representatives or distributors whose addresses and telephone numbers are listed in this catalog.

International: Customers outside North America are served by **Sipex** direct sales offices in France, Germany and Japan. **Sipex** is also represented throughout the world by international representatives and distributors whose offices are listed in this catalog.

Terms and Conditions of Sale

Prices and delivery information of any item in this catalog is available from our sales representatives or direct from the Company. Quotations are F.O.B. factory of origin, and are subject to change without notice. On all orders, payment is net 30 days following date of shipment.

Applications Engineering

Sipex maintains a support staff of technical sales engineers, both domestically and internationally, who are expert in specific areas of analog, digital, and microelectronics technology. Staff engineers provide further technical support, as needed, on advanced circuit designs or application problems.

Shipping Instruments

Shipping will be via United Parcel Service or Parcel Post unless other instructions are indicated. For rush service, we will ship by Air Freight, Air Express or Air Parcel Post on request.

Warranty

Sipex warrants its products to be free from defects in material and workmanship for a period of one year from the date of shipment. This warranty shall not apply to any product which has been abused or misused physically or electrically or whose leads have been clipped or soldered. Sipex's sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective components. Sipex shall not be liable for consequential damages under any circumstances.

Returns

When returning material for repair or replacement, it is necessary first to contact Customer Service. Upon acceptance of the request, a return material authorization (RMA#) will be issued. We require a detailed description of the reason for the return; the date and purchase order number on which it was obtained, and the date of receipt.

Specifications

Sipex reserves the right to discontinue items and change specifications without notice.

INTRODUCTION

Sipex Corporation recognizes that the quality and reliability of our products are of primary importance to our customers. **Sipex**'s Quality Assurance System has been designed to meet the needs of our customers and to evolve as new requirements are defined.

Corporate Mission and Quality Policy

Sipex Corporation has a "World Class" Quality Assurance System, incorporating the highest product and service standards in use today. In addition, it is the **Corporation**'s policy to meet or exceed each and every customer's product and service expectations.

Quality Commitment Statement

Maintaining **Sipex**'s Quality Assurance System requires the commitment and participation of all **Sipex** employees. At **Sipex**, effective and timely training, coupled with good communication, fosters an environment where all employees understand and are integral members of the Quality Assurance System. To ensure continued focus on Quality, **Sipex** Senior management has overall responsibility for Quality management.

Quality Assurance System

Sipex Corporation has in place a Quality Assurance System that achieves product "fitness for use" by performing three quality functions simultaneously:

- Quality Planning
- Quality Control
- Quality Improvement

The functional implementation of **Sipex**'s Total Quality Management (TQM) philosophy is indicated in *Figure 1*.

A key element in **Sipex**'s TQM philosophy is it's Quality Improvement Council. The **Sipex** Quality Council receives inputs from various sources inside and outside the Corporation. Information received from the **Sipex** Manufacturers Representative Council, factory operations, and endusers is used to direct, control, and assess **Sipex's** company wide efforts to manage for quality.

Quality Planning

Planning For Quality at **Sipex** involves all aspects of developing processes and products that meet the customer's requirements. **Sipex** performs the Quality Planning Function by ensuring that the customer's expectations are accurately communicated to the design, development and production departments. These requirements are, in turn, relayed to **Sipex** vendors to ensure a consistent quality standard from raw material to finished product.

Quality and Reliability Assessment play an important role in the Quality Planning Function at **Sipex**. Process and Product qualification flows are indicated in *Figure 2*.

Sipex's Reliability Assessment and monitoring program relies on accelerated environmental and stress tests to determine process/product reliability.

Sipex has divided its Wafer Fabrication and Assembly processes by Vendor and Process Family. Units are randomly selected from each process family on a periodic basis and exposed to a full range of environmental and stress testing. These tests include Temperature Cycle, Thermal Shock, Pressure Pot, High Temperature Operational Life Tests, Biased Temperature/Humidity Testing, HAST, Power Cycling and various mechanical integrity tests. In addition, **Sipex** performs Vapor Phase Stressing prior to environmental stressing to assess the integrity of the plastic molding compounds used on non–hermetic packages.

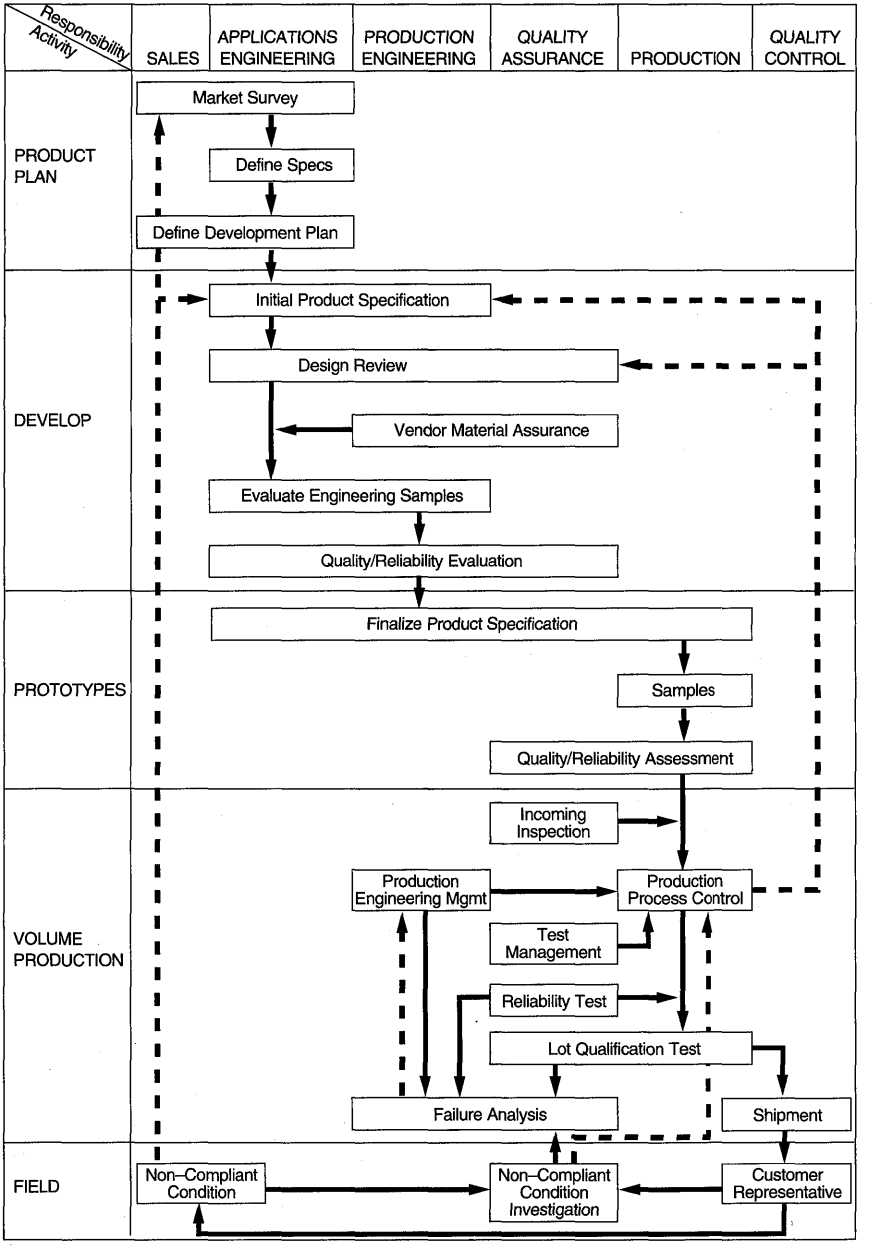


Figure 1. Sipex Corporation Quality Assurance System

Quality Management of Vendors

As part of the **Sipex** Vendor Partnership program, this data is shared with **Sipex** vendors and together, Process Improvement programs are defined and executed. Further, **Sipex** performs routine environmental stressing failure analysis as a service to our vendors. This service is provided for production processes as well as process improvements still in development.

Quality Management of Design

Sipex uses various computerized design verification tools to detect connection errors and layout violations. Design rules have been defined with sufficient margin so that even Class "S" current densities can be met under worst case process and manufacturing tolerances. **Sipex** has also developed extensive transistor level models, used to verify "worst case" performance, during the design phase.

Quality Control

The Quality Control (QC) at **Sipex** continuously assesses product and process performance relative to process/product goals. **Sipex**'s Quality Control Function uses a "feedback" loop that compares the actual performance to plan and takes action to address deficiencies when they occur. The Quality Control function extends to many areas in **Sipex** and includes **Sipex**'s vendors, manufacturing facilities, as well as customers.

The QC Function is implemented in the following main areas:

- QCI Monitoring
- In–Line Monitoring
- Quality/Reliability Assessment
- Statistical Quality Control
- Vendor/Source Control

QCI Monitoring

Sipex Corporation's Quality Conformance Inspection (QCI) data collection program follows the general practices and intent of MIL–M–38510 and MIL–STD–883. This is done for commercial (predominately non–hermetic packages) as well as military (presently limited to hermetic packages) products.

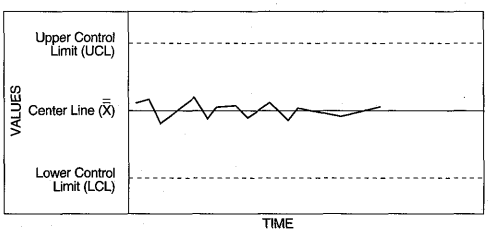
Table I summarizes the Quality Control general requirements/data collection performed by **Sipex** for the various process classification in place at **Sipex**. A comparison of corresponding **Sipex** manufacturing flows, including QCI gates, can be found in *Figure* 3.

In–Line Monitoring

Sipex utilizes in–line monitoring in conjunction with Statistical Process Control (SPC) Analysis techniques to monitor key process parameters in real time. This data allows the manufacturing personnel to react to process variations quickly, as well as serving as a database for process trend analysis.

Additionally, **Sipex** performs numerous QC checks in–line to ensure process consistency. Process Control Charts are in use at virtually every process operation.

Near real time monitoring techniques such as X–Ray analysis (eutectic die attach process monitoring), wire sweep (plastic packages), and SEM Analysis for metallization step coverage



In–Line Process Control Chart

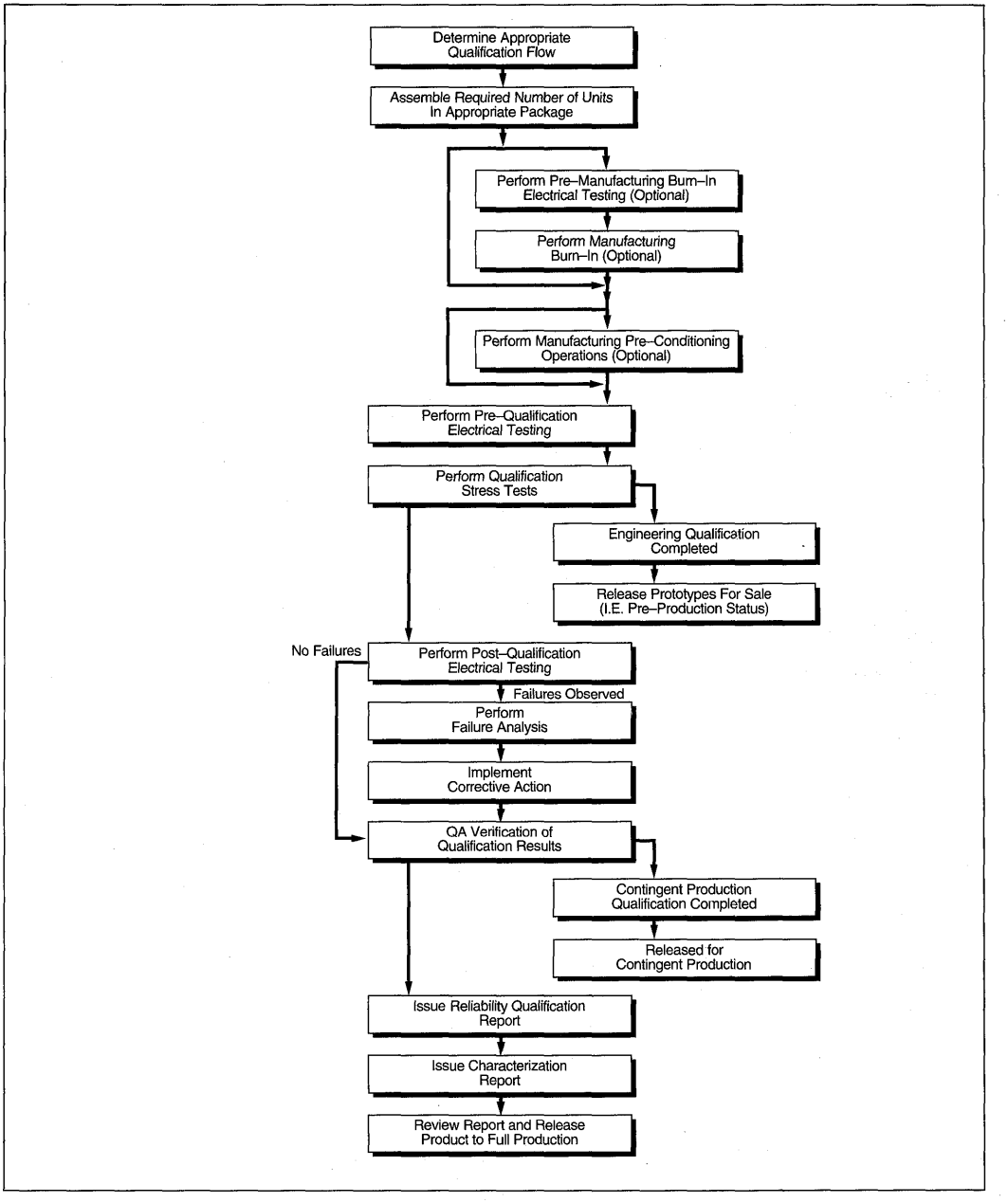


Figure 2. Generic Reliability Assessment and Product/Process Qualification Control Flow Chart

Description of Requirements and Screens	MIL–I–38535 Appendix A MIL–M–38510, MIL–STD–883 Requirements, Methods and Test Conditions	Processing Level						
		Requirements	JAN B (1)	SMD(1)	883 Class S	883 Class B	Hermetic Comm.	Non–Herm. Comm.
1. General MIL–M–38510: A. Pre–Certification B. Qualification Test Plan C. Product Assurance Program Plan	The manufacturer shall establish and implement a product assurance plan and submit to qualifying activity.	---	X	X	X	X	X	X
2. Certification	A. DESC survey B. Manufacturer's Q.A. Survey	---	X N/A	N/A X	N/A X	N/A X	N/A X	N/A X
3. Traceability	Traceability to wafer production lots	---	X	X	X	X	X	X
4. Country of Origin	Devices must be manu–factured, assembled and tested within U.S. or its territories.	---	X	N/A	X	X	N/A	N/A
MIL–STD–883, Method 5004 Screening								
5. Internal Visual	Method 2010 cond. B	100%	X	X	Method 2010 A	X	X(2) (Comm.)	X(2) (Comm.)
6. Stabilization Bake	Method 1008 cond. B	100%	X	X	X	X	X	N/A
7. Temperature Cycle	Method 1010 cond. C (10 Cycles,–65°C to +150°C)	100%	X	X	X	X	X	N/A
8. Constant Acceleration Y1 (30 kg in Y1 axis)	Method 2001 cond. E	100%	X	X	X	X	X	N/A
9. Visual Inspection	Method 2009 4th Optical	100%	X	X	X	X	X (2) (Comm.)	X (2)Criteria (Comm.)
10. Hermeticity A. Fine Leak B. Gross Leak	A. Method 1014 cond A or B B. Method 1014 cond. C	100%	X	X	X	X	X	N/A
11. Interim Electricals (initial class test)	Per applicable slash sheet for JAN of manufacturers documented data sheet.	100%	X	X	X	X	N/A	N/A
12. Burn–In	Method 1015, condition as specified. Minimum 160 hrs. at +125°C.	100%	X	X	240 Hrs minimum at +125°C	X	N/A	N/A
13. Final Electrical Post Burn–In Test	100% at +25°C with 5% PDA and in–line Group A. Also 100% at	100%	X	X	X	X	N/A	N/A
14. Lead Finish	Hot Solder dip, if necessary	100%	X	X	X	X	X	X
15. Mark	Fungus inhibiting ink includes ESD and Part Nomenclature	100% JM38510/ XXXXXX	X 5962 XXXXXX	X JEDEC 101B	X	X	X	X
16. Quality Conformance Inspection	Method 5005 in–line Group B Sub–Groups as indicated	Sub–Groups B2, B3, B5	x	X	X	X	N/A	N/A
17. Lead Scan/Straighten	---	100%	X	X	X	X	X	X
18. Post Mark/Final Electrical Test	100% at other temperature extreme and in–line Group A	100%	X	X	X	X	X 25°C. only	X 25°C. only
19. Lead Scan/Straighten	---	100%	X	X	X	X	X	X
20. 100% Hermeticity Test A. Fine Leak B. Gross Leak	A. Method 1014 cond. A or B B. Method 1014 condition C	100%	X	X	X	X	N/A	N/A

Table 1a. Comparison of Various Screening and Lot Conformance Requirements

Description of Requirements and Screens	MIL-I-38535 Appendix A MIL-M-38510, MIL-STD-883 Requirements, Methods and Test Conditions	Processing Level						
		Requirements	JAN B(1)	SMD(1)	883 Class S	883 Class B	Hermetic Comm.	Non-Herm. Comm.
21. QA Hermeticity Test A Fine Leak B Gross Leak	A. Method 1014 cond. A or B B. Method 1014 condition C	---	X	X	X	X	N/A	N/A
22. Visual/Mechanical Paperwork review in-line QA	100% Method 2009 review sample	---	X	X	X	X	X	X
23. Pack/Ship	Verify P.O. Requirement Includes C of C * No C of C issued	100%	X	X	X	X	X *	X *
Quality Conformance Inspection per Method 5005 of MIL-STD-883 (attributes data only)								
24. Group A[4]	Electrical per slash sheet or manufacturer's data sheets; subgroups 1-11 as specified.	Each lot/sublot	X	In-line	Each Lot	In-line	In-line 25°C only	In-Line 25°C only
25. Group B[4]	Packages functional and constructional related test	Each package[3] type on each lot	Each Lot	Each Lot	Each Lot	Each Package[5]	N/A	N/A
26. Group C[4]	Die related test (1,000 hrs Steady State Life)	Each microcircuit group	Every Quarter	Generic Every 52 Weeks	Every Quarter	Generic Every 52 wks per internal Sipex spec.	Reliability Qualification per internal Sipex spec.	Reliability Qualification per internal Sipex spec.
27. Group D[4]	Package related test group	Each package	Every Six Months	Generic Every 52 weeks	Every Six Months	Generic Every 52 Weeks	Reliability Qualification per internal Sipex spec.	Reliability Qualification per internal Sipex spec.

Notes:
1. Sipex Corporation does not perform JAN Class B or SMD Processing. These are included in this table for comparison purposes only.
2. Commercial visual screening is performed per Method 5004, Condition B (Class B) with minor relaxations allowed.
3. This performed for each log, package type, date code and assembly plant.
4. Quality Conformance inspections are done prior to shipment.
5. Per Seal-Week

Table 1b. Comparison of Various Screening and Lot Conformance Requirements

are employed on a periodic basis to monitor process integrity. These can also provide early detection of process variations that are not observable using conventional In-Line Monitoring practices.

Statistical Quality Control

Sipex utilizes various Statistical Quality Control Methods, including:

- SPC Analysis
- Pereto Graphs
- Process/Defect
- Histograms
- Cause/Effect Analysis
- Design of Experiments (DOE)
- Failure Mode Analysis

to analyze process and product performance data. In addition, **Sipex** has established working partnerships with each of its Vendors that involves periodic exchanges of process control data and Failure Analysis data.

Quality Improvement

Quality Improvement at **Sipex** involves improving both fitness for use as well as reducing process defects. Improvement is categorized as attaining new levels of performance that are consistently superior to all previous levels.

Sipex employs the technique of Continuous Process Improvement (CPI) to execute the Quality Improvement function. **Sipex**'s Quality

Improvement Council directs the CPI program.

Product Reliability Assessment

Product Reliability Assessment is an effort whereby statistical methods are employed to ascertain, control, predict and ultimately improve the failure rates of products.

The IC industry has evolved a method of reliability assessment and prediction based on MIL–HDBK–217 that considers both the chemical and physical sources of the failure mechanisms, as well as the inherently dynamic nature of the failure rates. **Sipex Corporation** subscribes to, supports, and aggressively utilizes these industry accepted practices.

Failure Rate and MTBF

The Mean Time Between Failures (MTBF) and the Failure Rate (FR) are two parameters used when Product Reliability Data is presented. These two parameters are inverses of each other. For example, if 200 units are tested for 1000 hours during which 4 failures occur, then

$$MTBF = \frac{\text{total device - hours}}{\text{total \# of failures}} = \frac{200x1000}{4} = 50,000\ hrs$$

$$FR = \frac{1}{MTBF} = \frac{\text{total \# of failures}}{\text{total device hours}} = 0.00002 = 2x10^{-5}$$

As manufacturing operations become more and more reliable, the Failure Rates associated with them begin to approach zero. This situation is highly desirable but can cause problems; an increasing number of leading zeroes (or, alternatively, larger negative powers of ten) are required to express the FR value. Reliability Engineers have developed a shorthand notation called Failure In Time (FIT) that simplifies writing the FR value. Failure In Time is related to Failure Rate by the expression:

$$FR \times 10^9 = FIT$$

Essentially, 1 FIT = 1 Failure in one billion device–hours of operation.

Continuing with the data in the above example:

$$FIT = FRx10^9$$
$$= 2x10^{-5}x10^9$$
$$= 2x10^4$$

The calculated MTBF and FR are called point estimates because they represent values obtained from data collected from one test (in this case, of 1000 hours in duration). If a second group of 200 units were tested for 1000 hrs, it is likely that the observed number of failures would be different.

IC unit failures occur in discrete quantities (i.e. 0,1,2,—n failures per lot). Each lot tested will have a number of failures that may or may not be the same as previous (or future) lots tested (or to be tested). This type of failure occurrence can be modeled by a discrete Probability Distribution Function called a Binomial Probability Function. When the number of observed failures is small, and the total number of units tested is large, the Poisson Probability Function becomes a close approximation to the Binomial Probability Function. The Poisson Probability function is useful as a first order failure rate model.

Continuous Probability Distribution Functions, such as Log–Normal and Weibull Functions, have also been used by the IC industry to model failures. The Poisson, Log–Normal and Weibull Distribution Functions are all negative exponentials. As such, these functions have several unique and mathematically desirable features that have been successfully exploited

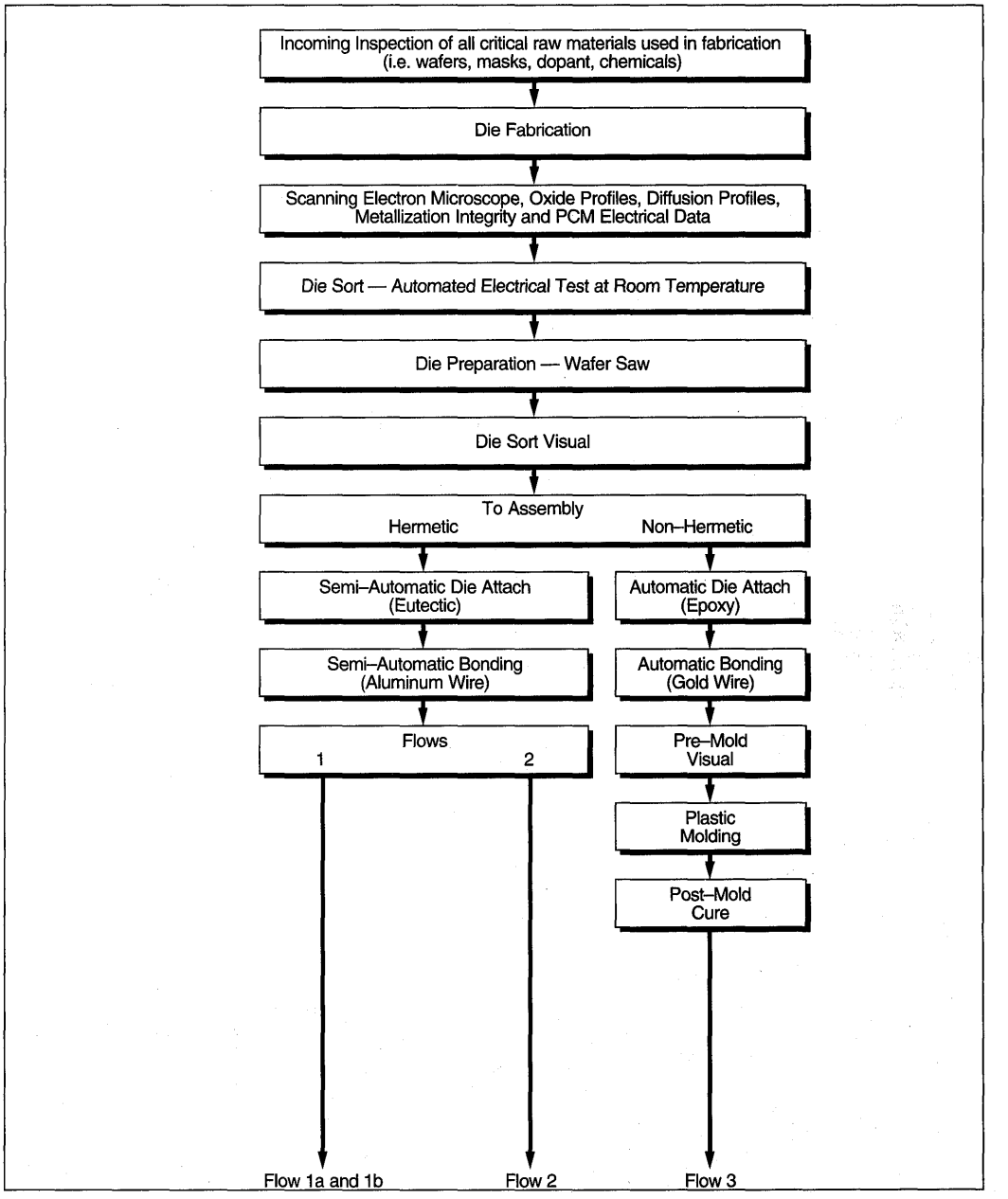


Figure 3a. Standard Manufacturing Flows

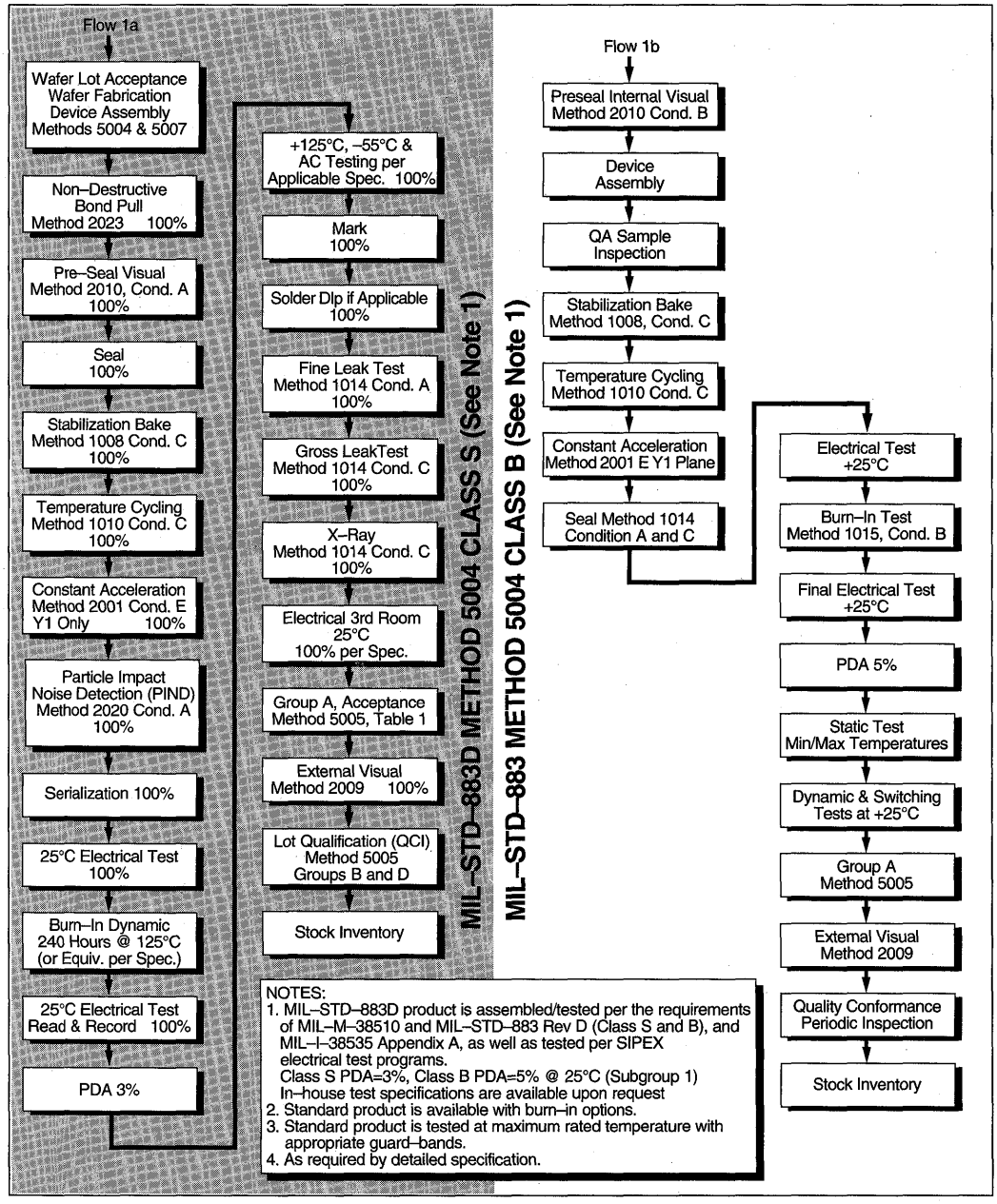


Figure 3b. Standard Manufacturing Flows

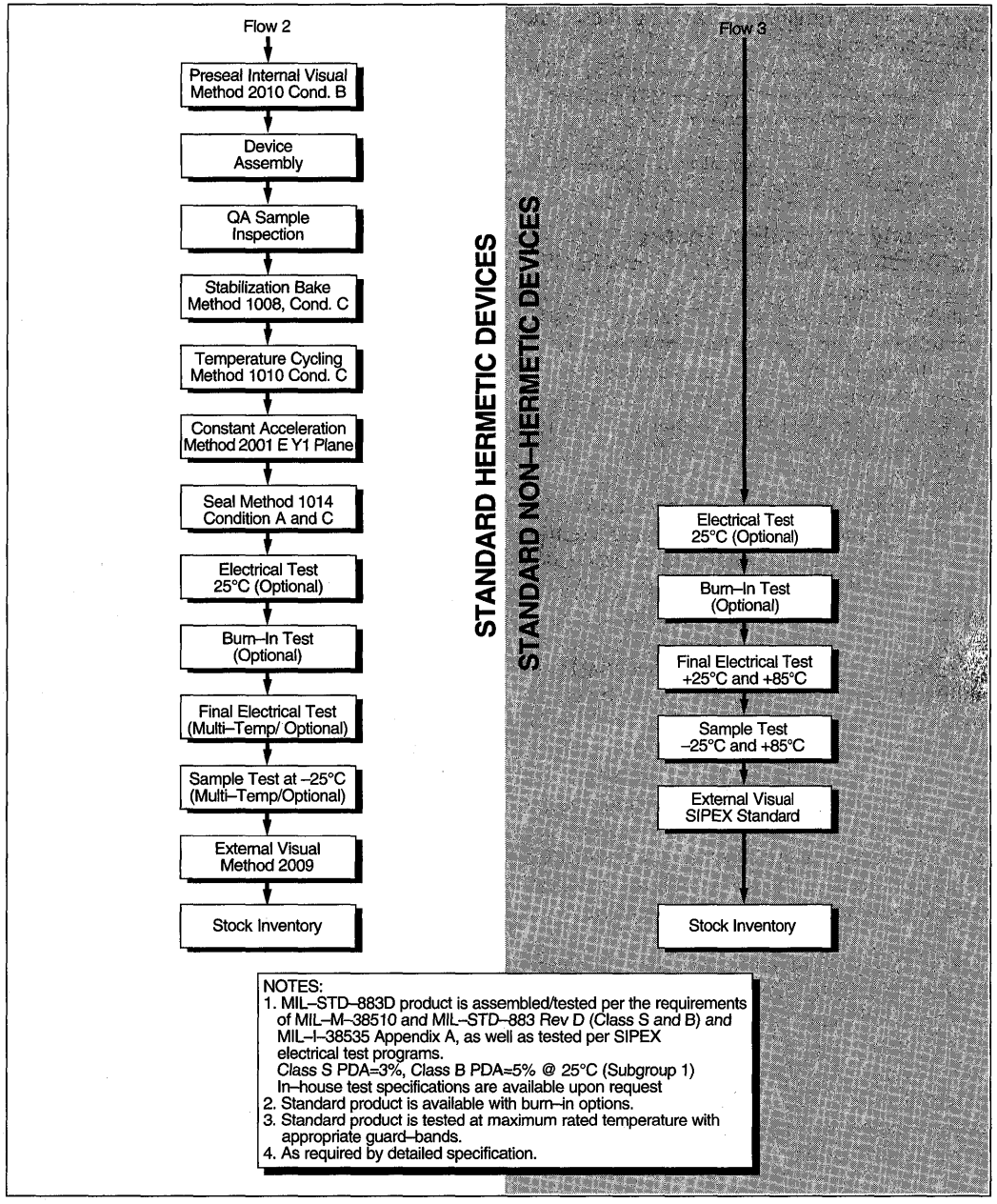


Figure 3c. Standard Manufacturing Flows

by Reliability Engineers. Among these, the most important are:

- The inverse relationship between MTBF and FR as illustrated in the above example
- The Failure Rate is independent of time (due to the exponential characteristic)

Reliability Distribution Theory

The" bathtub" distribution in *Figure 4* has historically been the most common failure rate distribution observed in the IC industry. As IC manufacturing techniques have improved, however, the total number of failures observed in the Infant Mortality and Random Failure regions has steadily declined to levels that are often too low to measure.

Consequently, much effort has been devoted to developing methods for accelerating component aging so that the failure rates associated with latent defects in the Wearout Region of the failure rate curve can be determined.

As mentioned previously, the exponential Probability Distribution Functions chosen by the IC Industry have the very convenient property of being independent of time. This feature allows reliability data to be collected in an almost infinite combination of devices and hours. Consequently, data collected using 5 devices for 10,000 hours is equivalent to data collected using 500 devices for 100 hours, assuming all other conditions of the tests are identical.

Taking this concept one step further, the Semiconductor Industry collects data representing hundreds of years of device performance at room temperature (25°C) by testing modest sample sizes (50–500 units) for 1000 hours at elevated temperatures (125–175°C). This is accomplished by using a relationship called the Arrhenius equation:

$$\text{Reaction Rate} = \text{Failure Rate} = Ae^{\left(\frac{-E_a}{kT}\right)}$$

k = Boltzmans Constant, 8.61423 x 10^{-5} eV/°K
E_a = Activation Energy of the Failure Mechanism
T = Temperature (°K)
A = Constant, independent of temperature

This relationship has been demonstrated to govern the failure rates of many mechanisms found to be responsible for IC failures. Assuming Ea is independent of Temperature, the Arrhenius Relationship can be rewritten so as to define an Acceleration Factor:

$$\frac{FR_{T2}}{FR_{T1}} = \text{Acceleration Factor} = \alpha = e^{\frac{E_a}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}$$

In the above equation, the Acceleration Factor acts as a multiplier that converts data collected at temperature T_2 to its equivalent at temperature T_1.

By way of example, using an Activation Energy of 0.8 eV, the conversion factors in *Table 2* result when data collected at 125°C is "converted" to its equivalent value at a lower temperature.

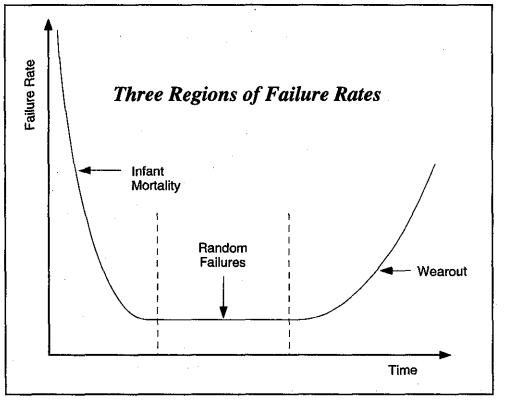


Figure 4. "Bathtub" Historical IC Failure Rate

A routine application of the Acceleration Factor is in the computation of equivalent device-hours. This is necessary when FR or MTBF values are required for a temperature other than the temperature at which the actual data was collected. Using the FR and MTBF relationships previously defined, inclusion of the Acceleration Factor results in the following modified expressions:

$$MTBF = \frac{(\text{total device - hours}) \times (\text{Acceleration Factor})}{\text{Total number of failures}}$$

$$FR = \frac{1}{MTBF} = \frac{\text{Total number of failures}}{(\text{total device - hours}) \times (\text{Acceleration Factor})}$$

On Accelerated Aging and Life Testing

Caution must be exercised when a specific stress condition is chosen for an Accelerated Life Test. The goal of the Accelerated Test is to expose the latent defects that are in some way responsible for failures in the Wearout Region without inducing additional unrelated failures.

Accelerated Life Tests are specifically designed to be of short duration, high stress. To be an effective tool in identifying potential device failure modes, these tests must produce failures similar to those observed in the field. Accelerated Life Testing can generate either unrelated failures or cause minor failure mechanisms that overwhelm the actual failure mechanisms.

An Accelerated Life Test considers the circuit design, fabrication/manufacturing technology, packaging methods and field failure rate histories collected on devices produced with similar manufacturing characteristics.

Data Collected At	Multiply By	Equivalent To Data At
125°C	2479.81	25°C
125°C	133.13	55°C
125°C	41.88	70°C

Table 2. Data Conversion to Equivalent Temperature

Activation Energy

The Arrhenius Activation Energy is the amount of molecular energy required for a particular failure mechanism to take place. This Activation Energy has no relationship to the semiconductor Energy Band Theory.

Industry practice is to empirically determine the Activation Energy of a particular failure mechanism by using an Arrhenius Plot, as in *Figure 5. The* Activation Energy associated with a specific failure mechanism is an average of the observed activation energies attributed to that particular failure mechanism. The slope of the line is given as:

$$\text{Slope} = \frac{-E_a}{k}$$

and the Activation Energy is given as:

$$E_a = -k \times (\text{Slope})$$

The Activation Energy is then compared to previous process history and industry published Activation Energies to ascertain the associated failure mechanism.

Typical Activation Energies associated with common IC failure mechanisms are listed in *Table 3.*

As can be seen from this table, Activation Energies associated with a specific failure mechanism often overlap observed Ea ranges of other failure mechanisms. In this case more than one failure analysis is required to determine the exact failure mechanism. By examining the MTBF equation and the Arrhenius Plot in *Fig-*

ure 5, it can be seen that decreasing values of Ea will predict decreasing MTBFs with corresponding increases in the FR. Stated another way, Ea and FR are inversely related.

Sipex Corporation tracks both the Relative Failure Rate and the Specific Failure Rate. *Table 3* contains a typical Relative Failure Rate distribution. Using an analysis method based on Relative Failure Rates, **Sipex** has determined that a weighted Activation Energy of 0.8eV is representative of the failure mechanisms observed to date on **Sipex** products. This activation energy provides a prediction of expected failure rates.

What Is A Failure?

Stresses including Accelerated Life Testing, cause two types of Failures:

- Parametric or Soft Failures
- Catastrophic or Hard Failures

Device Parametric Failures are units that are fully functional, but contain electrically measured failures to a published specification.

A Catastrophic Failure is categorized by **Sipex** as any device that is incapable of performing all of its specified functions.

Additionally, a Parametric Failure that exhibits measured values that are either 2x the maximum or 1/2x the minimum required value are classified as Catastrophic Failures by **Sipex Corporation**.

Sipex takes a conservative approach and considers all failures (whether Parametric or Catastrophic) and includes both types of failures when reporting Failure Rate, Failure In Time or Mean Time Between Failure Data.

The Implications of Sampling On Reliability Statistics

The statistics and examples discussed up to this point have relied on determination of the Failure Rates by direct measurements of all units within the population. Physical environmental test system size limits the number of devices that can be exposed to an environmental stress at any one time. Additionally, the use of Accelerated Testing to generate failures "consumes" a portion of the useful life of each device tested.

These and other practical constraints force the use of random samples to determine Failure Rates. This complicates the overall Failure Rate Determination effort because the uncertainty associated with the random sampling activity must be accounted for in the Failure Rate calculations.

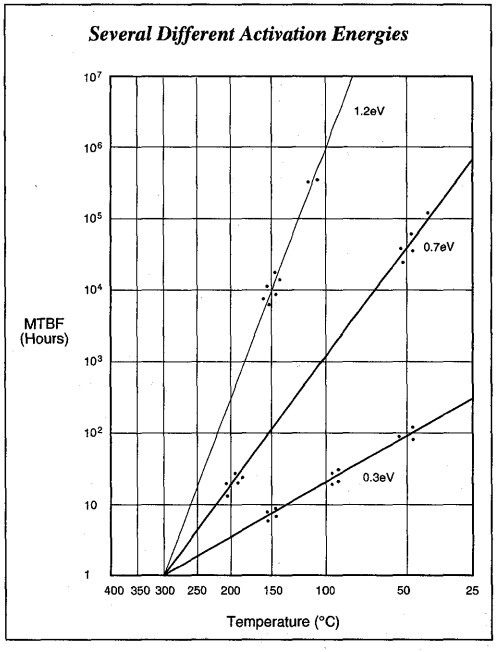


Figure 5. Arrhenius Plot

Based on historical knowledge of the distributions of IC failures and the relationship (or correlation) of one failure to another, it is possible to quantify a level of certainty associated with Failure Rates calculated from random samples.

Using Chi–Squared statistics, device failure data collected from random samples are used to predict the worst–case field failure rates likely to be experienced for the remainder of the devices in that lot. As data is collected from samples taken from independent lots (usually three separate lots, as a minimum), a cumulative Failure Rate can be calculated that represents the anticipated field failure rates for all lots. The Chi–Squared function is mathematically related to the Binomial and Poisson Functions (and is a special case of the Gamma Function). Graphically, the Chi–Squared function is similar in shape to the Normal or Gaussian distribution when a sufficiently large sample size is chosen (see *Figure 6*).

Failure Rate calculations incorporating the Chi–Squared statistical function are given as:

$$FR = \frac{(\chi^2)}{2DH\alpha}$$

χ^2 = Chi - Squared Value
DH = Device Hours
α = Acceleration Factor

The Chi–Squared value is typically determined by using mathematical tables where the indices into the table are the parameters:

– Confidence Level, CL
– Degrees of Freedom, DF

The Confidence Level is a means of statistically stating the possibility that the calculated Failure Rate will not be exceeded. For example, a Confidence Level of 0.60 means that in 60% of the cases the observed Failure Rate will be less than or equal to the predicated Failure Rate.

Failure Mode	Activation Energy	Primary Detection Method
Oxide Defect	0.3eV	HTDB
Silicon Defect	0.3	HTDB
Ionic Contamination		
Bulk	1.0	HTSB
Surface (Bipolar)	1.0–1.1	HTSB
Surface (MOS)	1.2–1.4	HTSB
Metallization		
Electromigration	0.6–1.2	HTSB
Corrosion	0.7–1.0	HTSB, HH
Microcracks	—	TC
Contact Metal Migration	0.6	HTDB
Stress Voids	0.3–0.5	HTDB, HH, TC, TS
Surface Inversion	0.5–1.0	HTDB
Charge Injection/Loss	1.4	HTSB
Slow Trapping	1.0–1.3	HTSB
Bond Related		
Intermetallic Growth	1.0–1.1	HTSB
Fatigue	—	TC, TS
Masking Defect		
Metal To Poly	0.3	HTSB
Metal To Metal	0.3	HTSB, TC, TS
Diffusion	0.5	HTSB
Packaging Related	—	HTSB, TC, TS, HH

NOTES:
1. HTSB is High Temperature Static Burn–In
2. HTDB is High Temperature Dynamic Burn–In
3. TC is Temperature Cycling
4. HH is High Humidity
5. TS is Thermal Shock

Table 3. Common Silicon Integrated Circuit Failure Modes

Failure Mode/ Mechanism	Relative Failure Rate	Weighted Avg. E_a
Wire Bond/Assembly/ Packaging	45%	1.1eV
Metallization	25	0.8
Ionic Contamination/ Surface Inversion	20	1.2
Oxide/Silicon Poly	5	0.3
Masking	8	0.4
Other	2	0.6

NOTE: Although reflective of Relative Failure Rate data collected by Sipex, Table II also includes data presented by numerous Government and Industry sources. As such, Table II does not reflect the attributes of any single Sipex Product or Product family, but should be considered an average for all Sipex Corporation Products.

Table 4. Typical Relative Failure Rate By Failure Mode Mechanism

Degrees of Freedom is a measure of the amount of dependence a given failure has on all other failures. The total number of observed failures also influences the DF value. The Degrees of Freedom parameter is calculated using the expression:

DF = 2r =Degrees of Freedom

r = total number of observed failures during random sampling

Sample Calculations For Failure Rate Using Random Samples

The concepts concerning Failure Rate calculations based on random sampling as described in previous sections of this report are employed below to demonstrate a typical application.

Assume the following data has been collected for a hypothetical Sipex Corporation part SP999–CT:

TEST 1
Number of units tested: 1250
Number of failures: 1
Test Temperature: 125°C
Number of Hours Tested: 3000 Hr

TEST 2
Number of units tested: 775
Number of failures: 0
Test Temperature: 55°C
Number of Hours Tested: 5000 Hr

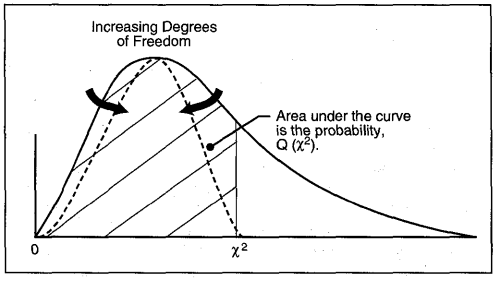


Figure 6. Chi–Squared Distribution

TEST 3
Number of units tested: 2753
Number of failures: 2
Test Temperature: 25°C
Number of Hours Tested: 462,504 Hr

Statement of Requirements: It is desired to calculate the Failure Rate (expressed in FITs) using a Confidence Level of 60% for an anticipated component field application at 55°C.

Table I contains Acceleration Factors for converting from 125°C to 75°C, 55°C or 25°C but does not contain an Acceleration Factor for converting from 25°C to 55°C. This factor is calculated using:

$$\alpha = e^{\frac{E_a}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}$$

where:

$E_a = 0.8V$

$T_1 = 55°C + 273°K = 320°C$

$T_2 = 25°C + 273°C = 298°K$

$K = 8.63X10^{-5} eV/°K$

Now, substituting these values back into the expression for α:

$$\alpha = e^{\frac{0.8eV}{8.63x10^{-5}V/°K}\left(\frac{1}{328°K}-\frac{1}{298°K}\right)}$$

for 25°C data conversion to 55°C data

$= e^{-2.845}$

$= 0.0581$

The Acceleration Factor appropriate for converting the data collected in this example from 25°C to 55°C is a= 0.0581.

Using this additional Acceleration Factor, it is now possible to calculate the total number of Device–Hours at 55°C:

DH = (Device–Hours Test 1)x (Acceleration Factor) + (Device–Hours Test 2) x (Acceleration Factor)+ (Device–Hours Test 3) x (Acceleration Factor)
= (1250 x 3000) x 133.13 + (775x5000) x 1 + (2753 x 462,504) x 0.0581
= 4.992 x 108 + 3.875 x 10^6 + 7.401 x 10^7 Device–Hours
= 5.809 x 10^8 Device–Hours @ 55°C

The total number of failures observed is given by:

r = (Number Failures Test 1 + Number Failures Test 2 + Number Failures Test 3)
= 1 + 0 + 2
= 3

The Degrees of Freedom value is calculated using:

DF = 2r
= 2 x 3
= 6

A Confidence Level of 60% must be restated as a fractional value not greater than 1.0. This is given as:

$$CL = \frac{CL(\%)}{100} = \frac{60\%}{100} = 0.6$$

Recalling the Failure Rate expression containing Chi–squared:

$$FR = \frac{\chi^2}{2D}$$

Using DF=6, CL=0.6 (as required per this example), χ^2 = 7.68 is obtained from mathematical tables. Substituting back into the FR expression:

$$FR = \frac{7.68}{2x5.809x10^8} = 6.61 \times 10^{-9}$$

Converting Failure Rate to FITs:

$$FIT = FRx10^9$$
$$= 6.61x10^{-9}x10^9$$
$$= 6.61 \text{ FITs}$$

Therefore, in this example, a Failure Rate not to exceed 6.61 FITs at an operating temperature of 55°C is expected in 60% of all lots of **Sipex Corporation** SP999–CT product.

SUMMARY OF TERMS

Accelerated Aging
Short duration environmental stresses specifically designed to induce latent defects to manifest themselves as device failures.

Accelerated Life Testing
Same as Accelerated Aging.

Acceleration Factor
The ratio of two Failure Rates involving the same Failure Modes obtained from identical units exposed to similar Environmental Stress conditions but differing in only one or two variables (e.g., temperature or voltage).

Activation Energy
The molecular energy required for a specific failure mechanism to take place.

AQL
Average Quality Level. This is a measure of quality that reflects the number of units rejected at Incoming Inspection.

Catastrophic Failure
Any device that is incapable of performing all of its specified functions.

Also known as a Hard Failure or a Functional Failure.

Compliance
An affirmative indication or judgment that the supplier of a product or service has met the requirements of the relevant specifications, contract, or regulation; also the state of meeting the requirements.

Confidence Level
A statistical term that quantifies the probability that a specified value, parameter, or attribute will occur in a given population of units.

Conformance
An affirmative indication or judgment that a product or service has met the requirements of the relevant specifications, contract, or regulation; also the state of meeting the requirements.

Defect
An attribute that is judged to be noncompliant to specification requirements.

Degrees Of Freedom
A statistical term that is used to quantify the dependence of a specific failure occurrence to all other failure occurrences. The Degrees of Freedom value is related to the number of failures observed.

Environmental Stress
Any physical or chemical influence that a device is exposed to and/or operated under.

Failure
The cessation of a device to perform a function (or functions) as required or specified.

Failure In Time (FIT)
A shorthand method for expressing Failure Rate. One FIT is defined as 1 failure in 10^9 device hours.

Failure Mechanism:
The chemical or physical cause of the failure.

Failure Rate
The Failure Rate at which device failures occur. Failure Rate may be measured, calculated based on random samples, or predicted based on previous historical data/trends.

Parametric Failure
Any device that is fully functional, but fails one or more parametric limits. Also known as a Soft Failure.

Quality
The collective characteristics (physical, electrical, mechanical, etc.) that make a device what it is. Quality is inherent and is the summation of all characteristics of the device.

Quality Assurance
All those planned or systematic actions necessary to provide adequate confidence that a product or service will satisfy given requirements for quality.

Quality Control
The operational techniques and the activities used to fulfill requirements of quality.

Quality Management
That aspect of the overall management function that determines and implements the quality policy.

Quality Measure
A quantitative measure of the features and characteristics of a product or service.

Quality Plan
A document setting out the specific quality practices, resources, and activities relevant to a particular product, process, service, contract or project.

Quality Policy
The overall intentions and direction of an organization as regards quality, as formally expressed by top management.

Quality Surveillance
The continuing monitoring and verification of the status of procedures, methods, conditions, products, processes, and services, and analysis of records in relation to stated references to ensure that requirements for quality are being met.

Quality System
The organizational structure, responsibilities,

procedures, processes, and resources for implementing quality management.

Reliability
Reliability is the ability of a device to perform stated functions over a specific period of time.

Specification
The document that prescribes the requirements with which the product or service has to conform.

Statistical Process Control
The application of statistical techniques to the control of processes.

Statistical Quality Control
The application of statistical techniques to the control of quality.

Testing
A means of determining the capability of an item to meet specified requirements by subjecting the item to a set of physical, chemical, environmental or operating actions and conditions.

Verification
The act of reviewing, inspecting, testing, checking, auditing, or otherwise establishing and documenting whether items, processes, services, or documents conform to specified requirements.

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INTERFACE PRODUCTS

INTERFACE PRODUCT SELECTION TABLE

+5V High–Speed RS232 Transceiver with 0.1µF Capacitors

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP200	5	0	4	Yes (0)	No	No	1
SP204	4	0	4	No	No	No	1
SP205	5	5	None	Yes(0)	No	Yes	1
SP205B	5	5	None	Yes (5)	Yes	Yes	1
SP206	4	3	4	Yes (0)	No	Yes	1
SP206B	4	3	4	Yes (3)	Yes	Yes	1
SP207	5	3	4	No	No	No	1
SP207B	5	3	4	Yes (3)	Yes	Yes	1
SP208	4	4	4	No	No	No	1
SP211	4	5	4	Yes (0)	No	Yes	1
SP211B	4	5	4	Yes (5)	Yes	Yes	1
SP213	4	5	4	Yes (2)	Yes	Yes	1

+5V/+12V Powered, Enhanced RS232 Drivers/Receivers

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP231A	2	2	2	No	No	No	33
SP239A	3	5	2	No	No	Yes	17

+5V Powered, Enhanced RS232 Drivers/Receivers

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP232A	2	2	4	No	No	No	33
SP233A	2	2	None	No	No	No	33
SP310A	2	2	4	Yes (0)	No	No	33

+5V Powered, Enhanced RS232 Drivers/Receivers, with Receiver Enable, Shutdown and Wakeup

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP241C	3	5	4	Yes (0)	Yes	Yes	41
SP312A	2	2	4	Yes (2)	Yes	Yes	33

+5V Powered RS232 Drivers/Receivers

Model	No. Drivers	No. Receivers	Ext. Caps.	Shutdown (No.*)	Wakeup	TTL Tri–State	Page
SP230A	5	0	4	Yes (0)	No	No	17
SP234A	4	0	4	No	No	No	17
SP235A	5	5	None	Yes (0)	No	Yes	17
SP235B	5	5	None	Yes (5)	Yes	Yes	17
SP236A	4	3	4	Yes (0)	No	Yes	17
SP236B	4	3	4	Yes (3)	Yes	Yes	17
SP237A	5	3	4	No	No	No	17
SP238A	4	4	4	No	No	No	17
SP240A	5	5	4	Yes (0)	No	Yes	17
SP240B	5	5	4	Yes (5)	Yes	Yes	17
SP241A	4	5	4	Yes (0)	No	Yes	17
SP241B	4	5	4	Yes (5)	Yes	Yes	17

* Number of active receivers in Shutdown mode.

INTERFACE PRODUCT SELECTION TABLE

RS232/RS422 Line Drivers/Receivers

Model	No. RS232 Ch.	No. RS422 Ch.	Mode Select	Loopback Test	Page
SP301	2	2	Software	Yes	49
SP302	4	2	Software	Yes	49

Enhanced RS232/RS422 Line Drivers/Receivers

Model	No. RS232 Ch.	No. RS422 Ch.	Mode Select	Loopback Test	Page
SP304	4	2	Software	Yes	75

RS232/AppleTalk™ Serial Transceiver

Model	No. RS232 Drivers.	No. RS232 Receivers	Macintosh™ Port	Mode Select	Page
SP303	4	4	1	Software	67

RS422/RS423 Line Drivers/Receivers

Model	No. RS422 Ch.	No. RS423 Ch.	Mode Select	Loopback Test	Page
SP306	2	2	Software	Yes	87

+3.3V Powered EIA562 Line Drivers/Receivers

Model	No. Drivers.	No. Receivers	Shutdown (No.*)	WakeUp	TTL Tri-State	Page
SP341	3	5	Yes (0)	Yes	Yes	93

RS485/RS422 Half-Duplex Interface Transceiver

Model	No. Drivers.	No. Receivers	Shutdown (No.*)	Low Power	Driver Enable	Rcvr Enable	Page
SP481	1	1	Yes	Yes	Yes	Yes	97
SP485	1	1	No	Yes	Yes	Yes	97

RS485/RS422 Line Drivers

Model	No. Drivers.	Driver Enable	Page
SP486	4	Common	105
SP487	4	Independent	105

RS485/RS422 Line Receivers

Model	No. Receivers.	Receiver Enable	Page
SP488	4	Common	111
SP489	4	Dual Pair	111

Multi-Protocol/Multi-Mode Serial Line Drivers/Receivers

Model	Protocols.	Drivers	Receivers	Page
SP501	11	6	7	117
SP502	6	6	7	159
SP503	6	7	7	189

CMOS Asynchronous to Synchronous Converter

Model	Page
MAS7838	217

* Number of active receivers in Shutdown mode.

EIA STANDARDS

Specification		RS-232D	RS-423A	RS-422	RS-485	RS-562
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential	Single-Ended
Number of Drivers and Receivers Allowed on One Line		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers	1 Driver 1 Receiver
Maximum Cable Length		50 feet	4,000 feet	4,000 feet	4,000 feet	C≤2500pF @ ≤20kb/s C≤1000pF @ ≥20kb/s
Maximum Data Rate		20kb/s	100kb/s	10Mb/s	10Mb/s	64kb/s
Driver Output Maximum Voltage		±25V	±6V	-0.25V to +6V	-7V to +12V	-3.7 to +13.2V
Driver Output Signal Level	Loaded	±5V	±3.6V	±2V	±1.5V	±3.7V
	Unloaded	±15V	±6V	±5V	±5V	±13.2V
Driver Load Impedance		3kΩ to 7kΩ	450Ω min.	100Ω	54Ω	3kΩ to 7kΩ
Maximum Driver Output Current (High Impedance State)	Power On	— —	— —	— —	±100µA	— —
	Power Off	V_{MAX} /300	100µA	±100µA	±100µA	— —
Slew Rate		30V/µs max.	Controls Provided	— —	— —	30V/µs max.
Receiver Input Voltage Range		±15V	±12V	-7V to +7V	-7V to +12V	±15V
Receiver Input Sensistivity		±3V	±200mV	±200mV	±200mV	±3V
Receiver Input Resistance		3kΩto 7kΩ	4kΩ min.	4kΩ min.	12kΩ min.	3kΩ to 7kΩ

Commonly–Used Data Communications Interfaces††

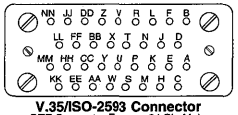
		RS-232		EIA-530		RS-449		EIA-561		EIA-574		V.35	
Signal Name	*Source*	*Mnemonic*	*Pin*	*Mnemonic*	*Pin*	*Mnemonic*	*Pin*	*Mnemonic*	*Pin*	*Mnemonic*	*Pin*	*Mnemonic*	*Pin*
Shield	—	—	1	—	1	—	1	—	—	—	—	—	A
Transmitted Data	DTE	BA	2	BA (A)	2	SD (A)	4	103	6	103	3	103	P
				BA (B)	14	SD (B)	22					103	S
Received Data	DCE	BB	3	BB (A)	3	RD (A)	6	104	5	104	2	104	R
				BB (B)	16	RD (B)	24					104	T
Request To Send	DTE	CA	4	CA (A)	4	RS (A)	7	105/133†	8	105/133†	7	105	C
				CA (B)	19	RS (B)	25						
Clear To Send	DCE	CB	5	CB (A)	5	CS (A)	9	106	7	106	8	106	D
				CB (B)	13	CS (B)	27						
DCE Ready (DSR)	DCE	CC	6	CC (A)	6	DM (A)	11	—	—	107	6	107	E
				CC (B)	22	DM (B)	29						
DTE Ready (DTR)	DTE	CD	20	CD (A)	20	TR (A)	12	108	3	108	4	108	H *
				CD (B)	23	TR (B)	30						
Signal Ground	—	AB	7	AB	7	SG	19	102	4	102	5	102	B
Recv. Line Sig. Det. (DCD)	DCE	CF	8	CF (A)	8	RR (A)	13	109	2	109	1	109	F
				CF (B)	10	RR (B)	31						
Trans. Sig. Elemt. Timing	DCE	DB	15	DB (A)	15	ST (A)	5	—	—	—	—	114	Y
				DB (B)	12	ST (B)	23					114	AA
Recv. Sig. Elemt. Timing	DCE	DD	17	DD (A)	17	RT (A)	8	—	—	—	—	115	V
				DD (B)	9	RT (B)	26					115	X
Local Loopback	DTE	LL	18	LL	18	LL	10	—	—	—	—	141	L *
Remote Loopback	DTE	RL	21	RL	21	RL	14	—	—	—	—	140	N *
Ring Indicator	DCE	CE	22	—	—	—	—	125	1	125	9	125	J *
Trans. Sig. Elemt. Timing	DTE	DA	24	DA (A)	24	TT (A)	17	—	—	—	—	113	U *
				DA (B)	11	TT (B)	35					113	W *
Test Mode	DCE	TM	25	TM	25	TM	18	—	—	—	—	142	NN *

METACOMP

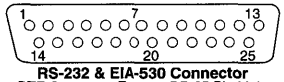
** Pins are specified in ISO 2593 but are not included in CCITT v.35*

† When hardware flow control is required, Circuit 105 may take on the functionality of Circuit 133.

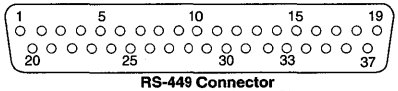
†† Some less–commonly used signals are not shown. METACOMP and SIPEX make no representation as to the accuracy or reliability of the information provided herein.



V.35/ISO-2593 Connector
DTE Connector Face — 34 Pin Male

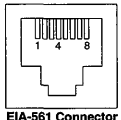


RS-232 & EIA-530 Connector
DTE Connector Face — DB-25 Pin Male

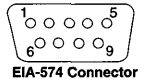


RS-449 Connector
DTE Connector Face — DB-37 Pin Male

Interchange Voltage States		
Notation	***Negative***	***Positive***
BinaryState	1	0
Signal Condition	Marking	Spacing
Function	Off	On



EIA-561 Connector
Equip. Connector Face
RJ-45 8 Pin Female



EIA-574 Connector
DTE Connector Face
DB-9 Pin Male

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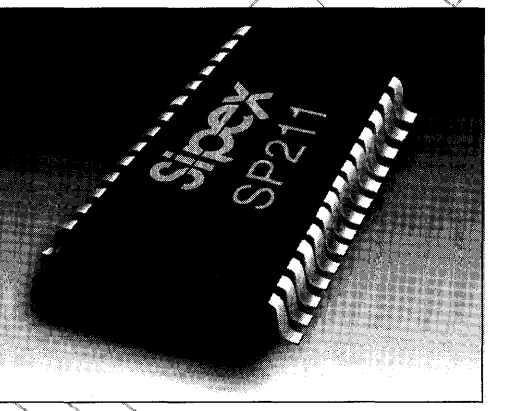
SP200/204/205/206/207/208/211/213

+5V High–Speed RS232 Transceivers with 0.1µF Capacitors

- 0.1µF External Charge Pump Capacitors
- 120Kbps Data Rate
- Standard SOIC and SSOP Packages
- Multiple Drivers and Receivers
- Single 5V Supply Operation
- 1µA Shutdown Mode
- WakeUp Feature in Shutdown Mode
- Tri–State Receiver Outputs
- Meets All RS232 and V.28 Specifications
- Improved Driver Output Capacity for Mouse Applications



DESCRIPTION...

The **SP200 Series** are multi–channel RS232 line transceivers in a variety of configurations to fit most communication needs. All models in this Series feature low–power CMOS construction and **Sipex**–patented (5,306,954) on-board charge pump circuitry to generate the ±10V RS232 voltage levels, using 0.1µF charge pump capacitors to save board space and reduce circuit cost. The **SP200**, **SP205**, **SP206**, **SP207B**, **SP211** and **SP213** models feature a low–power shutdown mode, which reduces power supply drain to 1µA. A WakeUp function keeps the receivers active in the shutdown mode.

Model	Number of RS232 Drivers	Number of RS232 Receivers	No. of Receivers Active in Shutdown	No. of External 0.1µF Capacitors	Shutdown	WakeUp	TTL Tri–State
SP200	5	0	0	4	Yes	No	No
SP204	4	0	0	4	No	No	No
SP205	5	5	0	None	Yes	No	Yes
SP205B	5	5	5	None	Yes	Yes	Yes
SP206	4	3	0	4	Yes	No	Yes
SP206B	4	3	3	4	Yes	Yes	Yes
SP207	5	3	0	4	No	No	No
SP207B	5	3	3	4	Yes	Yes	Yes
SP208	4	4	0	4	No	No	No
SP211	4	5	0	4	Yes	No	Yes
SP211B	4	5	5	4	Yes	Yes	Yes
SP213	4	5	2	4	Yes	Yes	Yes

Table 1. Model Selection Table

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +6V
V^+ ..... (V_{CC} – 0.3V) to +13.2V
V^- 13.2V
Input Voltages
T_{IN} ..... –0.3V to (V_{CC} +0.3V)
R_{IN} ..... ±20V
Output Voltages
T_{OUT} ..... (V^+, +0.3V) to (V^-, –0.3V)
R_{OUT} ..... –0.3V to (V_{CC} +0.3V)
Short Circuit Duration on T_{OUT} ..... Continuous
Power Dissipation
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

SPECIFICATIONS

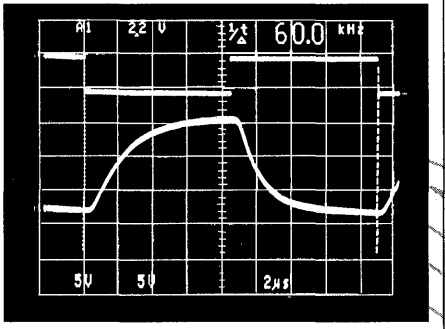
V_{CC} at nominal ratings; 0.1µF charge pump capacitors; T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
TTL INPUTS					T_{IN}, EN, SD
Logic Threshold					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Logic Pullup Current		15	200	µA	T_{IN} = 0V
Data Rate			120	Kbps	C_L = 2,500pF, R_L = 3KΩ
TTL OUTPUTS					
Compatibility		TTL/CMOS			
V_{OL}			0.4	Volts	I_{OUT} = 3.2mA; V_{CC} = +5V
V_{OH}	3.5			Volts	I_{OUT} = –1.0mA
Leakage Current		0.05	±10	µA	EN = V_{CC}; 0V ≤ R_{OUT} ≤ V_{CC}; T_A = +25°C
RS232 OUTPUT					
Output Voltage Swing	±5	±7		Volts	All transmitter outputs loaded with 3KΩ to ground
Output Resistance	300			Ohms	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±25		mA	Infinite duration
RS232 INPUT					
Voltage Range	–15		+15	Volts	
Voltage Threshold					
Low	0.8	1.2		Volts	V_{CC} = 5V, T_A = +25°C
High		1.7	2.4	Volts	V_{CC} = 5V, T_A = +25°C
Hysteresis	0.2	0.5	1.0	Volts	V_{CC} = +5V
Resistance	3	5	7	KΩ	±15V; T_A = +25°C
DYNAMIC CHARACTERISTICS					
Propagation Delay		1.5		µs	RS232–to–TTL
Instantaneous Slew Rate			30	V/µs	C_L = 50pF, R_L = 3–7KΩ; T_A = +25°C
Transition Region Slew Rate		5		V/µs	C_L = 2,500pF, R_L = 3KΩ; measured from +3V to –3V or –3V to +3V
Output Enable Time		400		ns	
Output Disable Time		250		ns	

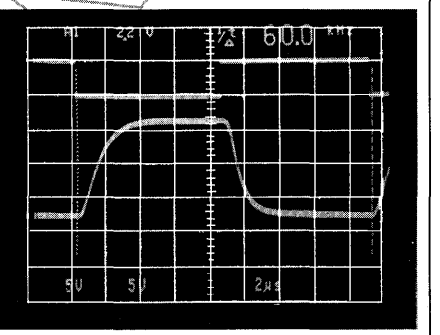
SPECIFICATIONS

V_{CC} at nominal ratings; 0.1µF charge pump capacitors; T_{MIN} to T_{MAX}, unless otherwise noted.

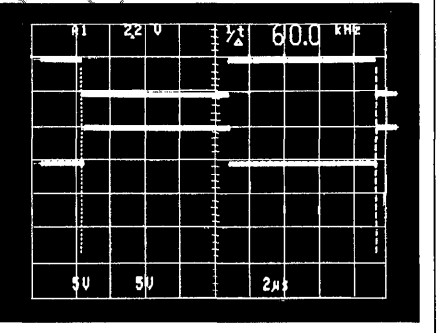
PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
POWER REQUIREMENTS					
V_{CC}					
SP200, SP205, SP207 and SP207B	4.75	5.00	5.25	Volts	
All other parts	4.50	5.00	5.50	Volts	
I_{CC}					T_A = +25°C
		4	10	mA	No load; V_{CC} = ±10%
		20		mA	All transmitters R_L = 3KΩ
Shutdown Current		1	10	µA	T_A = +25°C
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial, –C	0		+70	°C	
Extended, –E	–40		+85	°C	
Storage Temperature	–65		+125	°C	
Package					
–A	Shrink (SSOP) small outline				
–T	Wide (SOIC) small outline				



Transmitter Output
R_L=3KΩ, C_L=5,000pF

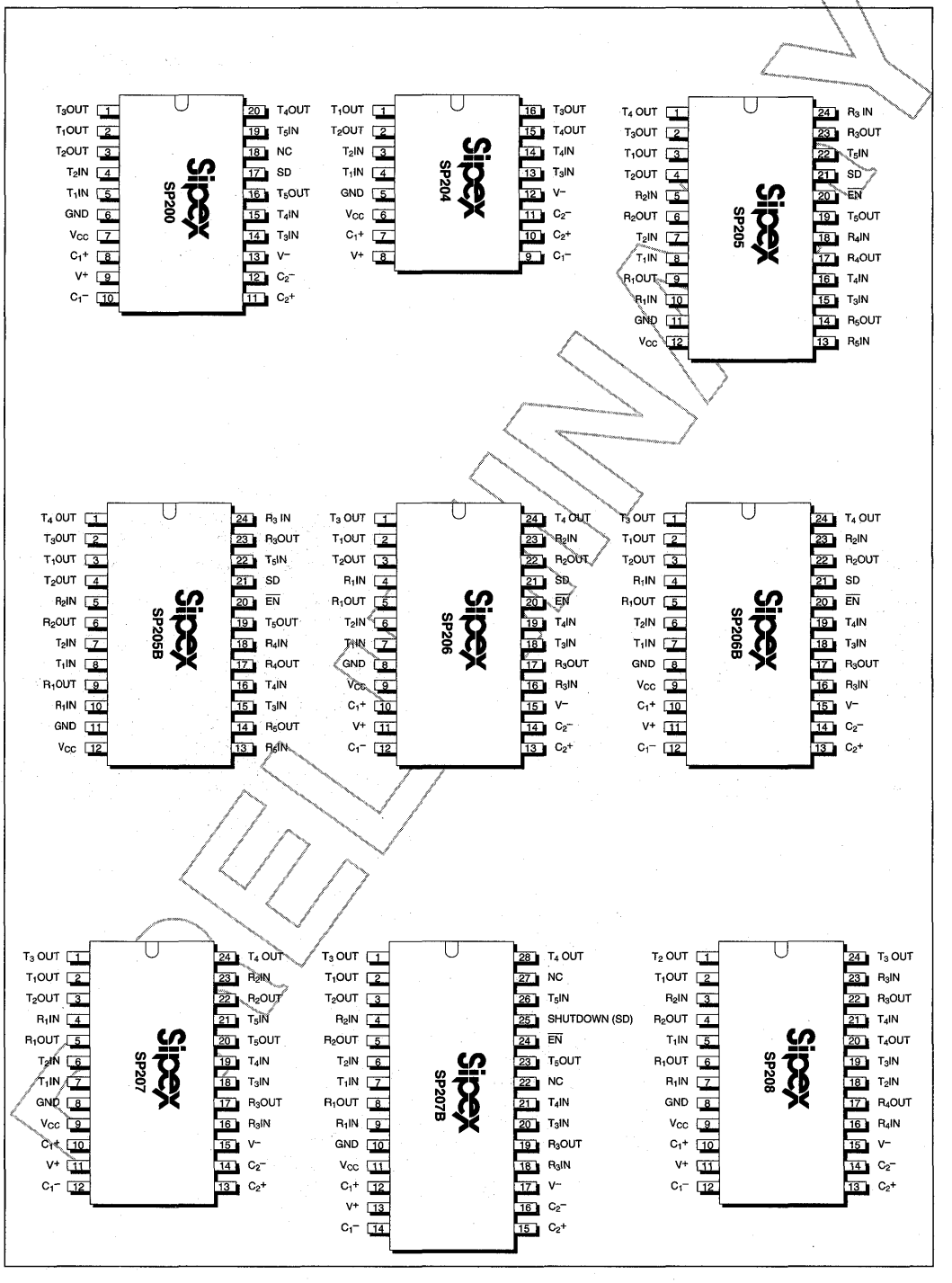


Transmitter Output
R_L=3KΩ, CL=2,500pF

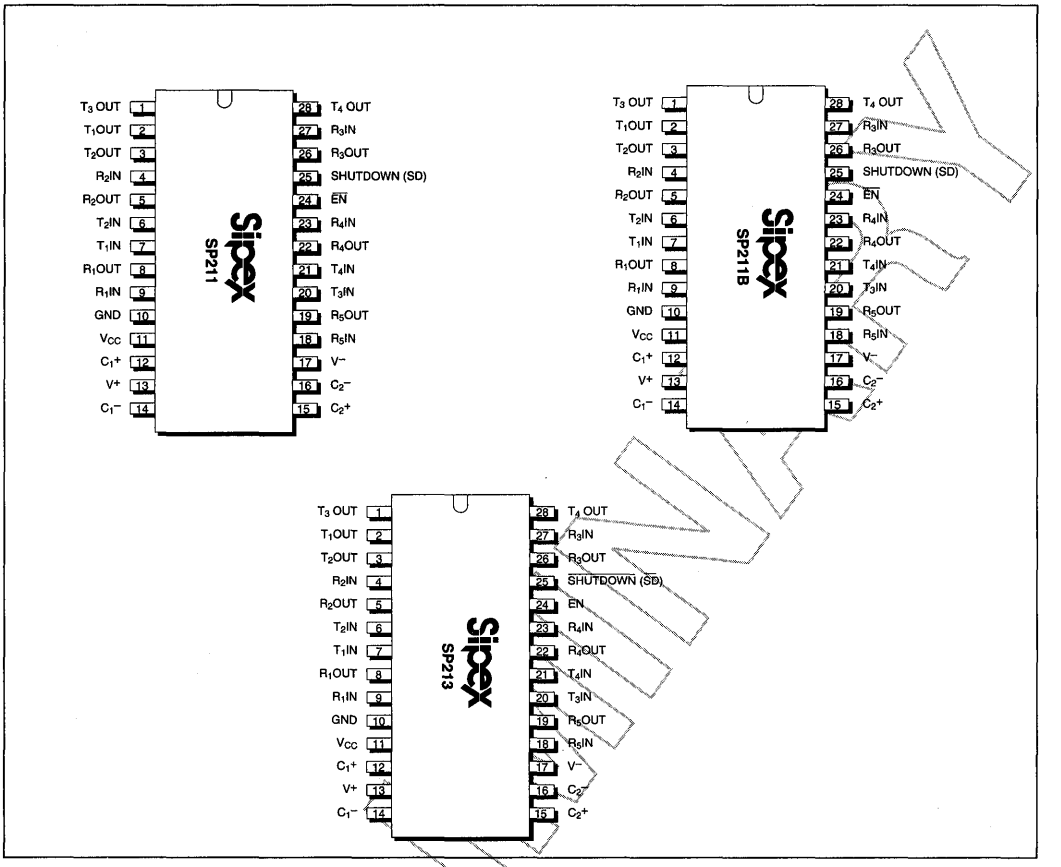


Receiver Output

PINOUT



PINOUT



FEATURES...

The **SP200 Series** multi–channel RS232 line transceivers provide a variety of configurations to fit most communication needs, especially those applications where ±12V is not available. All models in this Series feature low–power CMOS construction and **SIPEX**–proprietary on-board charge pump circuitry to generate the ±10V RS232 voltage levels. The ability to use 0.1µF charge pump capacitors saves board space and reduces circuit cost. Different models within the Series provide different driver/receiver combinations to match any application requirement.

The **SP200**, **SP205**, **SP206**, **SP207B**, **SP211** and **SP213** models feature a low–power shutdown mode, which reduces power supply drain to 1µA. The WakeUp function keeps the receivers active in the shutdown mode, unless disabled by the EN pin. Models with –B suffix are equipped with the WakeUp function.

Models in the Series are available in 28–pin SO (wide) and SSOP (shrink) small outline packages. Devices can be specified for commercial (0°C to +70°C) and industrial/extended (–40°C to +85°C) operating temperatures.

THEORY OF OPERATION

Charge–Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to

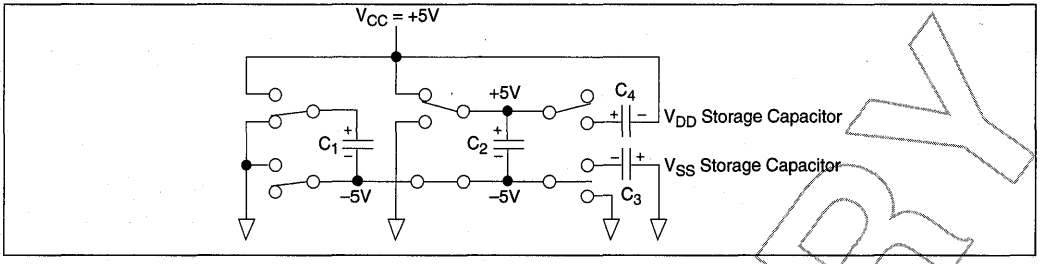


Figure 1. Charge Pump — Phase 1

attain symmetrical 10V power supplies. *Figure 3a* shows the waveform found on the positive side of capcitor C_2, and *Figure 3b* shows the negative side of capcitor C_2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –10V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated 10V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

The **SP200 Series** devices are made up of three basic circuit blocks — 1) transmitter/driver, 2) receiver and 3) the **SIPEX**–proprietary charge

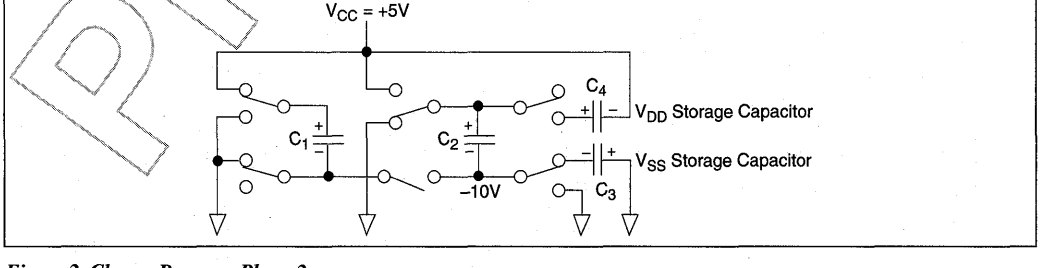


Figure 2. Charge Pump — Phase 2

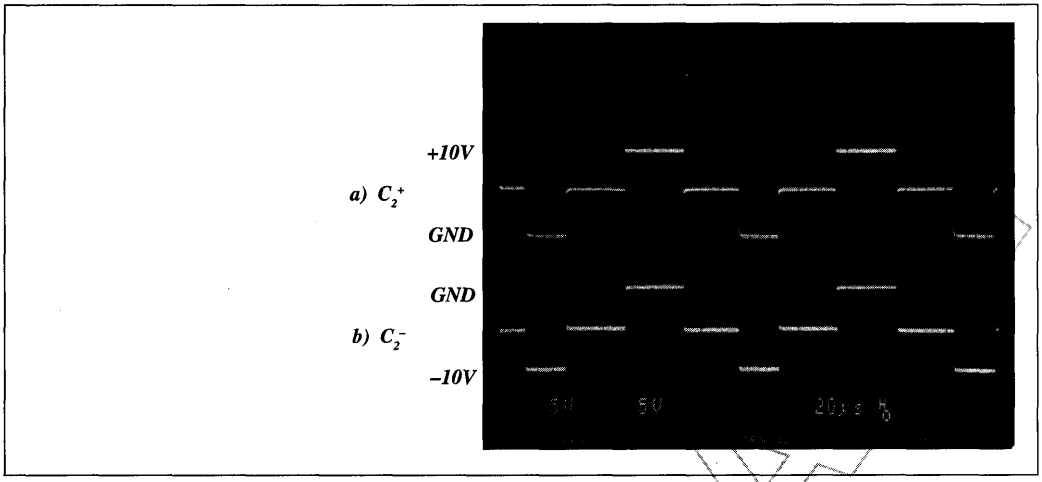


Figure 3. Charge Pump Waveforms

pump. Each model within the Series incorporates variations of these circuits to achieve the desired configuration and performance.

Transmitter/Driver

The drivers are inverting transmitters, which accept either TTL or CMOS inputs and output the RS232 signals with an inverted sense relative to the input logic levels. Typically, the RS232 output voltage swing is ±9V with no load, and ±5V minimum with full load. The transmitter outputs are protected against infinite short–circuits to ground without degradation in reliability. The drivers of the **SP200**, **SP205**, **SP205B**, **SP206**, **SP206B**, **SP207B, SP211**, **SP211B** and **SP213** can be tri–stated by using the SHUTDOWN function.

In the "power off" state, the output impedance will remain greater than 300 ohms, again satisfying the RS232 specifications. Should the input of the driver be left open, an internal 400Kohm pullup resistor to V_{CC} forces the input high, thus committing the output to a low state. The slew rate of the transmitter output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS232D 2.1.7, Paragraph 5). The transition of the loaded output from high to low also meets the monotonicity requirements of the standard.

Receivers

The receivers convert RS232 input signals to inverted TTL signals. Since the input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5Kohm pulldown resistor to ground will commit the output of the receiver to a high state.

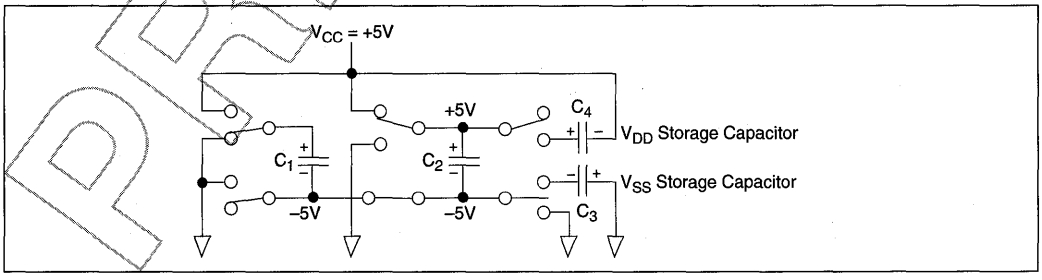


Figure 4. Charge Pump — Phase 3

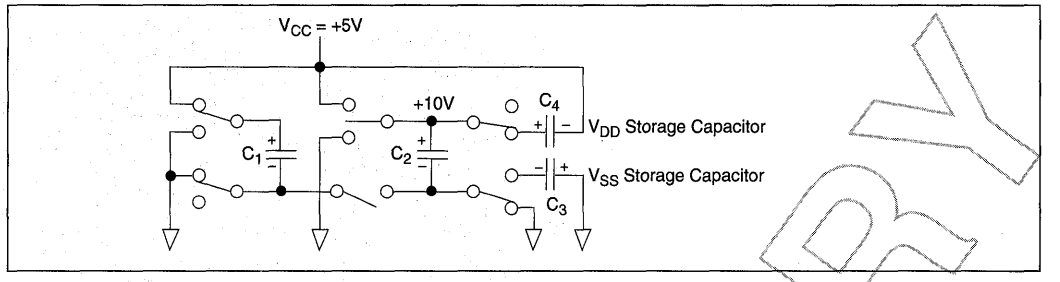


Figure 5. Charge Pump — Phase 4

SHUTDOWN MODE

The **SP200**, **SP205**, **SP205B**, **SP206**, **SP206B**, **SP207B**, **SP211**, **SP211B** and **SP213** all feature a control input which will disable the device and reduce the power supply current to less than 10µA, making the parts ideal for battery–powered systems. In the "shutdown" mode the receivers and transmitters will both be tri–stated. The V^+ output of the charge pump will discharge to V_{CC}, and the V^- output will discharge to ground. Products with the WakeUp function can enable or disable the receivers during shutdown.

For complete shutdown to occur and the 10µA power drain to be realized, the following conditions must be met:

SP200, **SP205/B**, **SP206/B**, **SP207B** and **SP211/B**:

- +5V must be applied to the SD pin
- ENABLE must be either 0V, +5.0V or not connected
- the transmitter inputs must be either +5.0V or not connected
- V_{CC} must be +5V
- Receiver inputs must be >0V and <+5V

SP213:

- 0V must be applied to the SD pin
- ENABLE must be either 0V, +5.0V or not connected
- the transmitter inputs must be either +5.0V or not connected
- V_{CC} must be +5V
- Receiver inputs must be >0V and <+5V

SD	EN	SP213 Only $\overline{SD}$	SP213 Only EN	Power Up/Down	Receiver Outputs
0	0	1	1	Up	Enable
0	1	1	0	Up	Tri–state
1	0	0	1	Down	Enable
1	1	0	0	Down	Tri–state

Table 2. Wake–Up Truth Table

ENABLE

The **SP205/B**, **SP206/B**, **SP207/B**, **SP211** and **SP213** all feature an enable input, which allows the receiver outputs to be either tri–stated or enabled. This can be especially useful when the receiver is tied directly to a microprocessor data bus. For the **SP205/B**, **SP206/B**, **SP207/B** and **SP211**, enable is active low; that is, 0V applied to the ENABLE pin will enable the receiver outputs. For the **SP213**, enable is active high; that is, +5V applied to the ENABLE pin will enable the receiver outputs.

WAKEUP FUNCTION

The **SP205B**, **SP206B**, **SP207B**, **SP211B** and **SP213** have a wake–up feature that keeps two or more receivers in an enabled state when the device is in the shutdown mode. The **SP213** has two receivers active (R_4 and R_5), while the **SP205B**, **SP207B** and **SP211B** have all receivers active during shutdown. With only the receivers active during shutdown, the devices draw 5–10µA of supply current.

A typical application of this function would be where a modem is interfaced to a computer in a power–down mode. The ring indicator signal from the modem could be passed through an active receiver in the **SP2XXB/SP213** that is itself in the shutdown mode. The ring indicator signal would propagate through the **SP2XXB/SP213** to the power management circuitry of the computer to power up the microprocessor and the **SP2XXB/SP213** drivers. After the supply voltage to the **SP2XXB/SP213** reaches +5.0V, the SHUTDOWN pin can be disabled, taking the **SP2XXB/SP213** out of the shutdown mode.

All receivers that are active during shutdown maintain 500mV (typ.) of hysteresis.

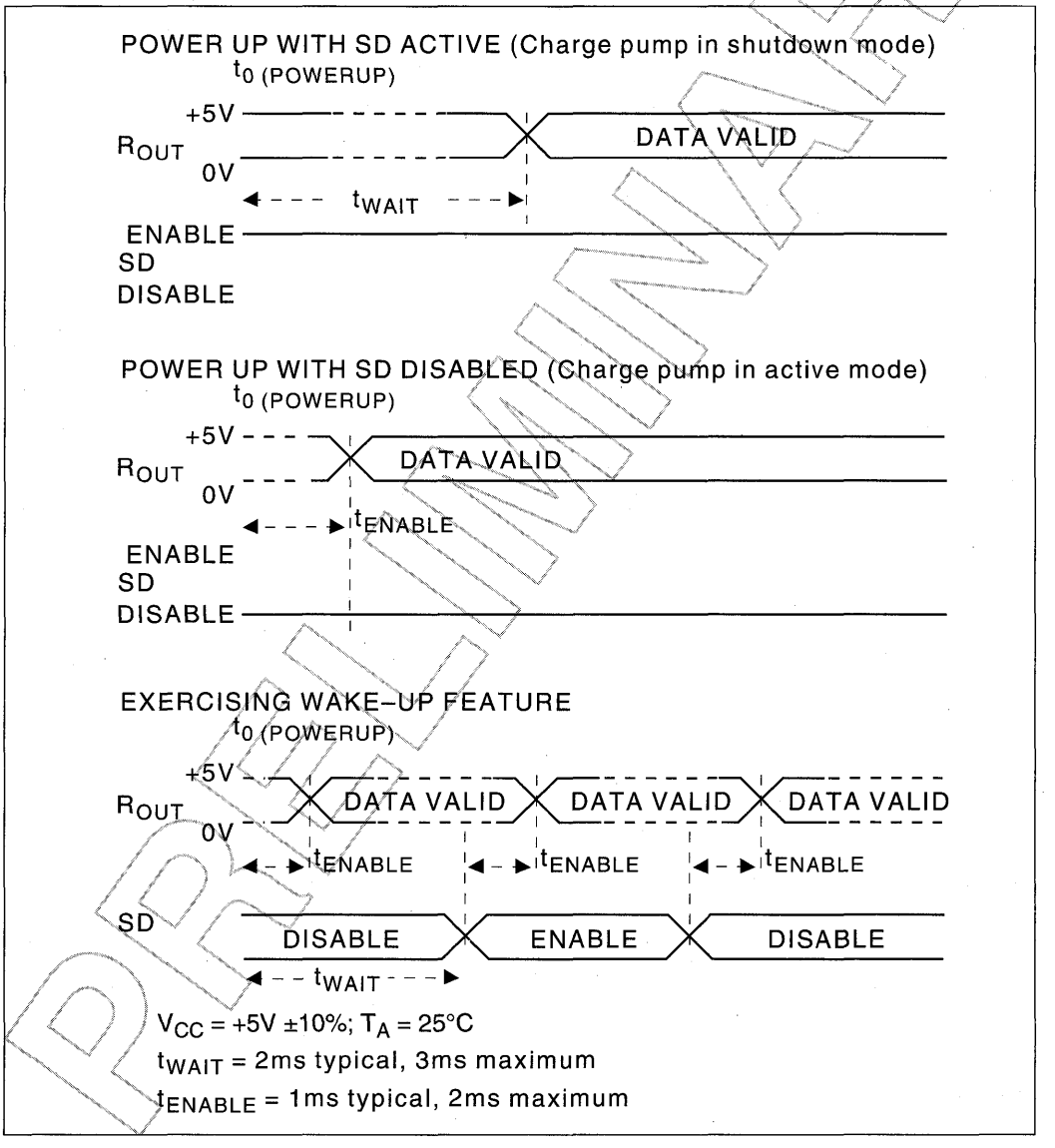


Figure 6. Wake–Up Timing

Specification	RS–232D	RS–423A	RS–422	RS–485	RS–562
Mode of Operation	Single–Ended	Single–Ended	Differential	Differential	Single–Ended
No. of Drivers and Receivers Allowed on One Line	1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers	1 Driver 1 Receiver
Maximum Cable Length	50 feet	4,000 feet	4,000 feet	4,000 feet	C ≤ 2,500pF @ <20Kbps; C ≤1,000pF @ >20Kbps
Maximum Data Rate	20Kb/s	100Kb/s	10Mb/s	10Mb/s	64Kb/s
Driver output Maximum Voltage	±25V	±6V	–0.25V to +6V	–7V to +12V	–3.7V to +13.2V
Driver Output Signal Level Loaded Unloaded	 ±5V ±15V	 ±3.6V ±6V	 ±2V ±5V	 ±1.5V ±5V	 ±3.7V ±13.2V
Driver Load Impedance	3 – 7Kohm	450 ohm	100 ohm	54 ohm	3–7Kohm
Max. Driver Output Current (High Impedance State) Power On Power Off	 V_{MAX}/300	 100µA	 ±100µA	 ±100µA ±100µA	
Slew Rate	30V/µs max.	Controls Provided			30V/µs max.
Receiver Input Voltage Range	±15V	±12V	–7V to +7V	–7V to +12V	±15V
Receiver Input Sensitivity	±3V	±200mV	±200mV	±200mV	±3V
Receiver Input Resistance	3–7Kohm	4Kohm min.	4Kohm min.	12Kohm min.	3–7Kohm

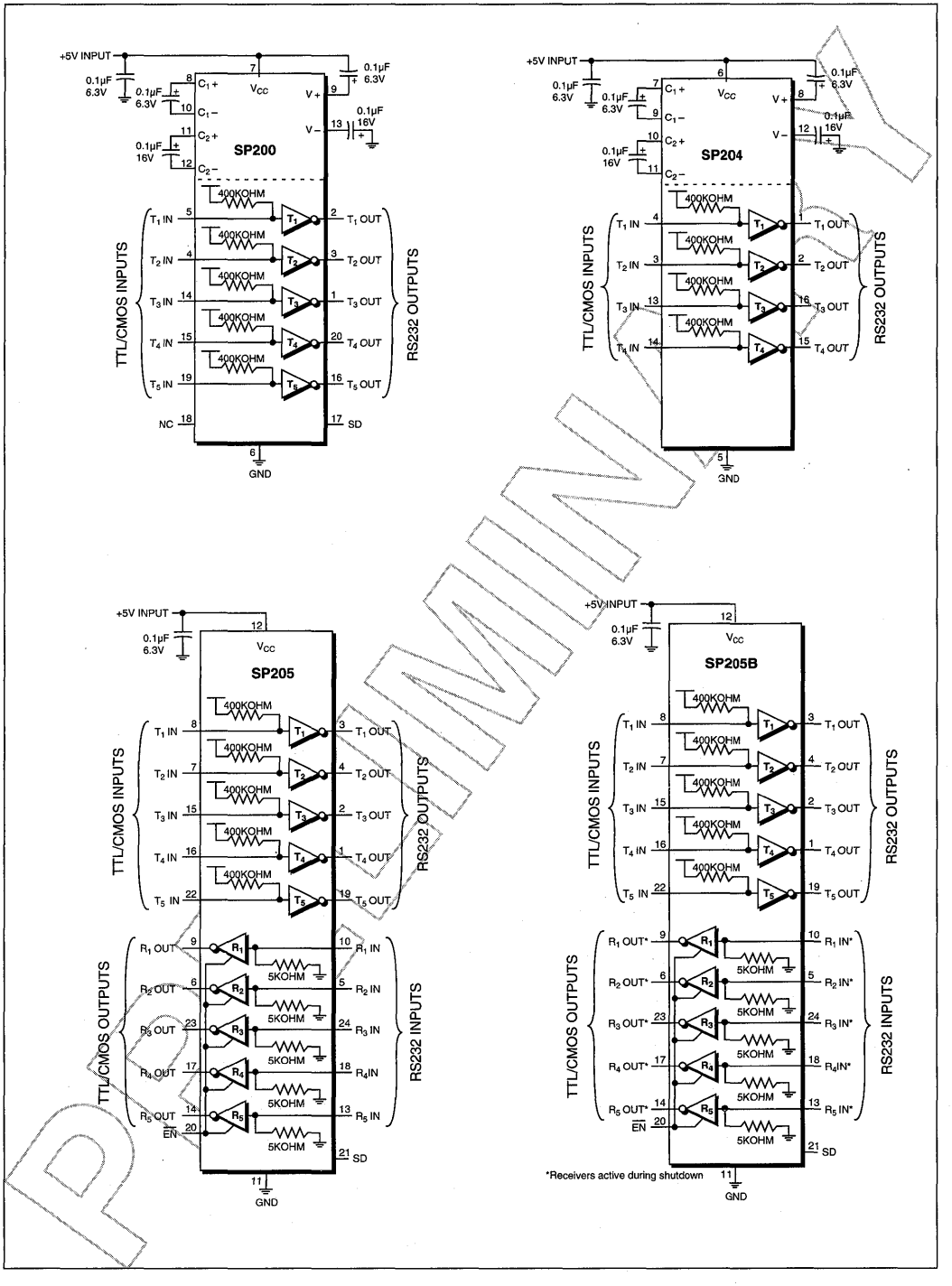
Table 3. EIA Standard Definitions

EIA STANDARDS

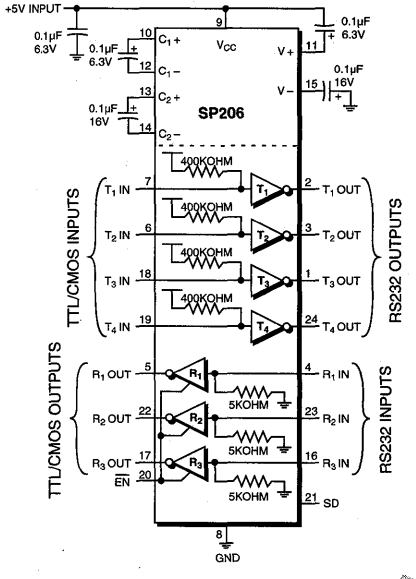
The Electronic Industry Association (EIA) developed several standards of data transmission which are revised and updated in order to meet the requirements of the industry. In data processing, there are two basic means of communicating between systems and components. The RS232 standard was first introduced in 1962 and, since that time, has become an industry standard.

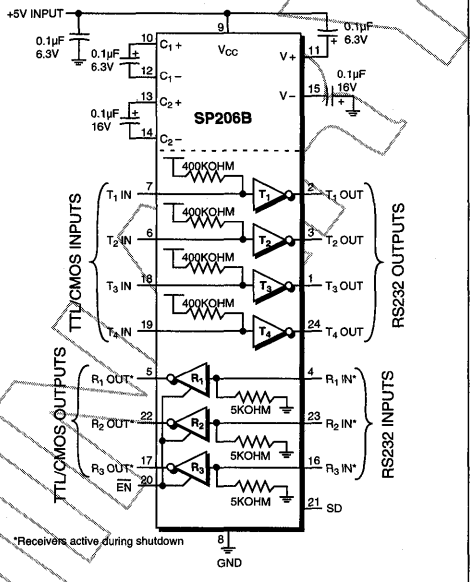
The RS232 is a relatively slow data exchange protocol, with a maximum baud rate of only 20Kbaud, which can be transmitted over a maximum copper wire cable length of 50 feet. The SP200 through SP213 Series of data communications interface products have been designed to meet both the EIA protocol standards, and the needs of the industry.

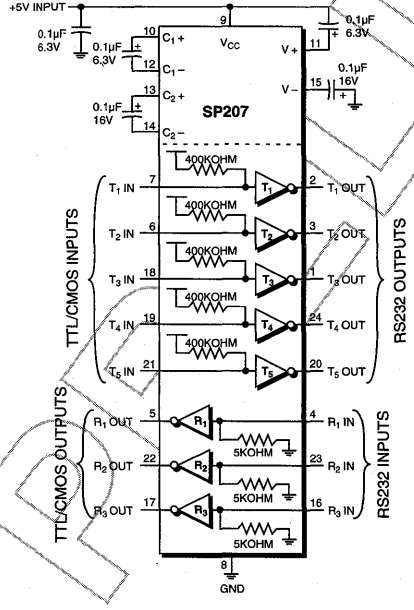
TYPICAL APPLICATION CIRCUITS

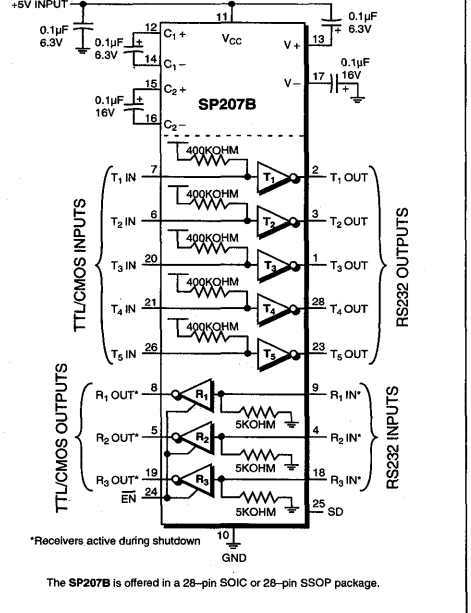


TYPICAL APPLICATION CIRCUITS



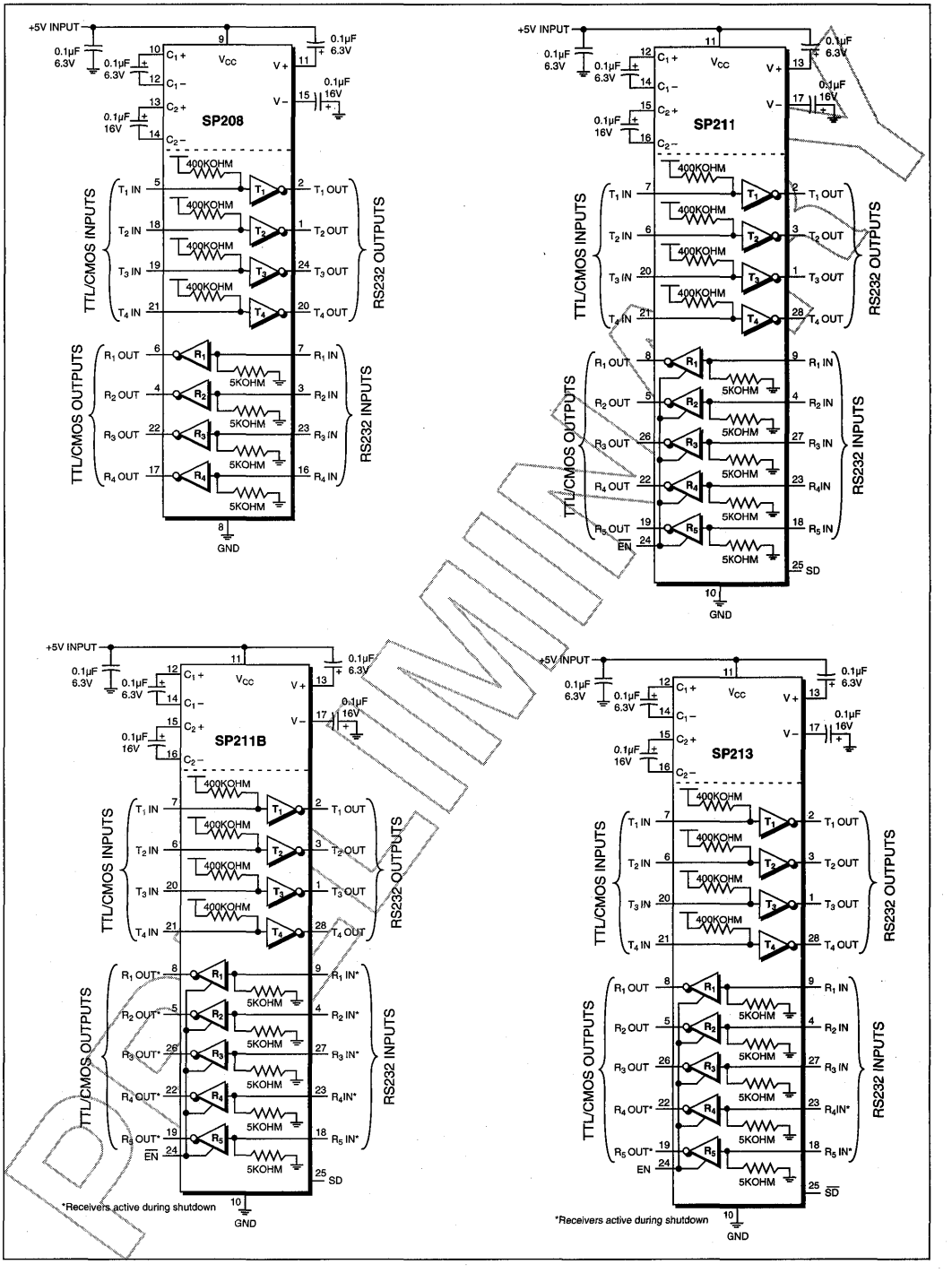






The **SP207B** is offered in a 28–pin SOIC or 28–pin SSOP package.

TYPICAL APPLICATION CIRCUITS



ORDERING INFORMATION

RS232 Transceivers:

Model	Drivers	Receivers	Temperature Range	Package Type
SP207CA	5	3	0°C to +70°C	24–pin SSOP
SP207CP	5	3	0°C to +70°C	24–pin Plastic DIP
SP207CT	5	3	0°C to +70°C	24–pin SOIC
SP207EA	5	3	–40°C to +85°C	24–pin SSOP
SP207EP	5	3	–40°C to +85°C	24–pin Plastic DIP
SP207ET	5	3	–40°C to +85°C	24–pin SOIC
SP208CA	4	4	0°C to +70°C	24–pin SSOP
SP208CP	4	4	0°C to +70°C	24–pin Plastic DIP
SP208CT	4	4	0°C to +70°C	24–pin SOIC
SP208EA	4	4	–40°C to +85°C	24–pin SSOP
SP208EP	4	4	–40°C to +85°C	24–pin Plastic DIP
SP208ET	4	4	–40°C to +85°C	24–pin SOIC

RS232 Transmitters:

Model	Drivers	Receivers	Temperature Range	Package Type
SP204CP	4	0	0°C to +70°C	16–pin Plastic DIP
SP204CT	4	0	0°C to +70°C	16–pin SOIC
SP204EP	4	0	–40°C to +85°C	16–pin Plastic DIP
SP204ET	4	0	–40°C to +85°C	16–pin SOIC

RS232 Transmitters with Low–Power Shutdown:

Model	Drivers	Receivers	Temperature Range	Package Type
SP200CP	5	0	0°C to +70°C	20–pin Plastic DIP
SP200CT	5	0	0°C to +70°C	20–pin SOIC
SP200EP	5	0	–40°C to +85°C	20–pin Plastic DIP
SP200ET	5	0	–40°C to +85°C	20–pin SOIC

RS232 Transceivers with Low–Power Shutdown and Tri–state Enable:

Model	Drivers	Receivers	Temperature Range	Package Type
SP205CP	5	5	0°C to +70°C	24–pin Plastic Double–Width DIP
SP205EP	5	5	–40°C to +85°C	24–pin Plastic Double–Width DIP
SP206CA	4	3	0°C to +70°C	24–pin SSOP
SP206CP	4	3	0°C to +70°C	24–pin Plastic DIP
SP206CT	4	3	0°C to +70°C	24–pin SOIC
SP206EA	4	3	–40°C to +85°C	24–pin SSOP
SP206EP	4	3	–40°C to +85°C	24–pin Plastic DIP
SP206ET	4	3	–40°C to +85°C	24–pin SOIC
SP211CA	4	5	0°C to +70°C	28–pin SSOP
SP211CT	4	5	0°C to +70°C	28–pin SOIC
SP211EA	4	5	–40°C to +85°C	28–pin SSOP
SP211ET	4	5	–40°C to +85°C	28–pin SOIC

ORDERING INFORMATION

RS232 Transceivers with Low–Power Shutdown, Tri–state Enable, and Wake–Up Function:

Model	Drivers	Receivers	Temperature Range	Package Type
SP205BCP	5	5, with 5 active in Shutdown	0°C to +70°C	24–pin Plastic Double–Width DIP
SP205BEP	5	5, with 5 active in Shutdown	–40°C to +85°C	24–pin Plastic Double–Width DIP
SP206BCA	4	3, with 3 active in Shutdown	0°C to +70°C	24–pin SSOP
SP206BCP	4	3, with 3 active in Shutdown	0°C to +70°C	24–pin Plastic DIP
SP206BCT	4	3, with 3 active in Shutdown	0°C to +70°C	24–pin SOIC
SP206BEA	4	3, with 3 active in Shutdown	–40°C to +85°C	24–pin SSOP
SP206BEP	4	3, with 3 active in Shutdown	–40°C to +85°C	24–pin Plastic DIP
SP206BET	4	3, with 3 active in Shutdown	–40°C to +85°C	24–pin SOIC
SP207BCA	5	3, with 3 active in Shutdown	0°C to +70°C	28–pin SSOP
SP207BCT	5	3, with 3 active in Shutdown	0°C to +70°C	28–pin SOIC
SP207BEA	5	3, with 3 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP207BET	5	3, with 3 active in Shutdown	–40°C to +85°C	28–pin SOIC
SP211BCA	4	5, with 5 active in Shutdown	0°C to +70°C	28–pin SSOP
SP211BCT	4	5, with 5 active in Shutdown	0°C to +70°C	28–pin SOIC
SP211BEA	4	5, with 5 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP211BET	4	5, with 5 active in Shutdown	–40°C to +85°C	28–pin SOIC
SP213CA	4	5, with 2 active in Shutdown	0°C to +70°C	28–pin SSOP
SP213CT	4	5, with 2 active in Shutdown	0°C to +70°C	28–pin SOIC
SP213EA	4	5, with 2 active in Shutdown	–40°C to +85°C	28–pin SSOP
SP213ET	4	5, with 2 active in Shutdown	–40°C to +85°C	28–pin SOIC

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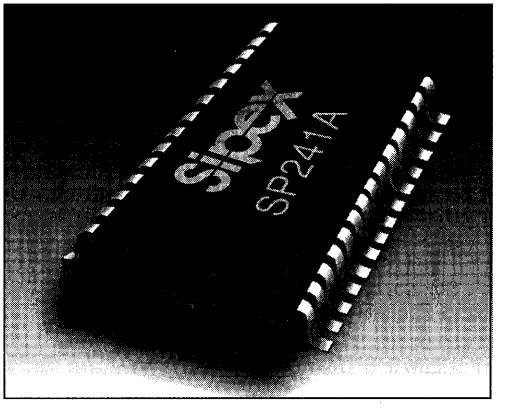
SP230A/234A/235A/236A/237A/238A/239A/241A
SP235B/236B/240A/240B/241A/241B

+5V Powered Multi–Channel RS232 Drivers/Receivers

- Operates from Single +5V Power Supply (+5V and +12V — SP239A)
- Meets All RS232D and V.28 Specifications
- ±9V Output Swing with +5V Supply
- Improved Driver Output Capacity for Mouse Applications
- Low Power Shutdown — 1µA
- Wake Up Feature in Shutdown Mode
- 3–State TTL/CMOS Receiver Outputs
- ±30V Receiver Input Levels
- Low Power CMOS — 5mA Operation
- Wide Charge Pump Capacitor Value Range — 1–10µF



DESCRIPTION...

The **SP230A** Series are multi–channel RS232 line drivers/receivers that provide a variety of configurations to fit most communication needs, especially where ±12V is not available. Some models feature a shutdown mode to conserve power in battery–powered systems. Some require no external components. All, except one model, feature a built–in charge pump voltage converter, allowing them to operate from a single +5V power supply. All drivers and receivers meet all EIA RS232D and CCITT V.28 requirements. The Series is available in plastic and ceramic DIP and SOIC packages.

SELECTION TABLE

Model	Power Supplies	No. of RS232 Drivers	No. of RS232 Rcvrs	External Components	Low Power Shutdown	TTL 3–State	Wake-Up	No. of Pins
SP230A	+5V	5	0	4 Capacitors	Yes	No	No	20
SP234A	+5V	4	0	4 Capacitors	No	No	No	16
SP235A	+5V	5	5	None	Yes	Yes	No	24
SP235B	+5V	5	5	None	Yes	Yes	Yes	24
SP236A	+5V	4	3	4 Capacitors	Yes	Yes	No	24
SP236B	+5V	4	3	4 Capacitors	Yes	Yes	Yes	24
SP237A	+5V	5	3	4 Capacitors	No	No	No	24
SP238A	+5V	4	4	4 Capacitors	No	No	No	24
SP239A	+5V/+8.5 to +13.2V	3	5	2 Capacitors	No	Yes	No	24
SP240A	+5V	5	5	4 Capacitors	Yes	Yes	No	44
SP240B	+5V	5	5	4 Capacitors	Yes	Yes	Yes	44
SP241A	+5V	4	5	4 Capacitors	Yes	Yes	No	28
SP241B	+5V	4	5	4 Capacitors	Yes	Yes	Yes	28

ABSOLUTE MAXIMUM RATINGS

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

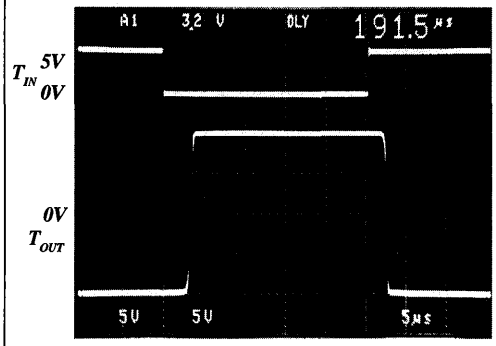
V_{CC} ..... +6V
V^+ ..... (Vcc–0.3V) to +13.2V
V^- 13.2V
Input Voltages:
T_{IN} ..... –0.3 to (Vcc +0.3V)
R_{IN} ..... ±30V
Output Voltages:
T_{OUT} ..... (V+, +0.3V) to (V–, –0.3V)
R_{OUT} ..... –0.3V to (Vcc +0.3V)
Short Circuit Duration:
T_{OUT} ..... Continuous
Power Dissipation:
CERDIP 675mW
(derate 9.5mW/°C above +70°C)
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

SPECIFICATIONS

All units Vcc=+5V±10%; except SP235A/B, Vcc=+5V±5%; SP239A only, V+ = +8.5 to +13.2V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
POWER REQUIREMENTS					
Vcc Power Supply Current		5	10	mA	No load, T_A= +25°C
SP239A only		0.4	1.0	mA	
V+ Power Supply Current					
SP239A only		8	15	mA	No load, V^+ = 12V
Shutdown Supply Current		1	10	µA	T_A = +25°C
LOGIC INPUTS					
Input Logic Threshold					
Low			0.8	Volts	T_{IN} ; EN, SD
High	2.0			Volts	T_{IN} ; EN, SD
Logic Pullup Current		15	200	µA	T_{IN} = 0V
RS232 INPUTS					
RS232 Input Voltage Range	-30		+30	Volts	
RS232 Input Threshold					
Low	0.8	1.2		Volts	Vcc = 5V, T_A = +25°C
High		1.7	2.4	Volts	Vcc = 5V, T_A = +25°C
RS232 Input Hysteresis	0.2	0.5	1.0	Volts	Vcc = 5V
RS232 Input Resistance	3	5	7	Kohms	T_A = +25°C
LOGIC OUTPUTS					
Output Voltage					
Low			0.4	Volts	I_{OUT} = 3.2mA
High	3.5			Volts	I_{OUT} = 1.0mA
Output Leakage Current		0.05	±10	µA	EN = V_{CC}, 0V≤R_{OUT} ≤Vcc
RS232 OUTPUTS					
Output Enable Time		400		nS	SP235A/B, SP236A/B, SP241A/B
SP239A &					
Output Disable Time		250		nS	SP235A/B, SP236A/B, SP241A/B
SP239A &					
Propagation Delay		1.5		µS	RS232 to TTL
Instantaneous Slew Rate			30	V/µS	C_L = 10pF, R_L= 3—7KΩ; T_A = +25°C
RS232 OUTPUTS					
Transition Region Slew Rate		3		V/µs	C_L = 2500pF, R_L= 3KΩ; measured from +3V to -3V or -3V to +3V
Output Voltage Swing	±5	±9		Volts	All transmitter outputs loaded with 3KΩ to Ground
Output Resistance	300			Ohms	V_{CC}= 0V; V_{OUT} = ±2V
RS232 Output Short Circuit Current		±10		mA	Infinite duration

Transmitter Output Waveforms



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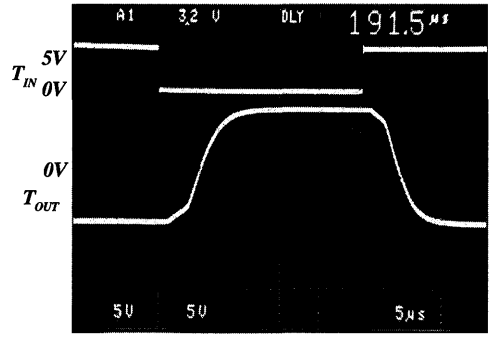
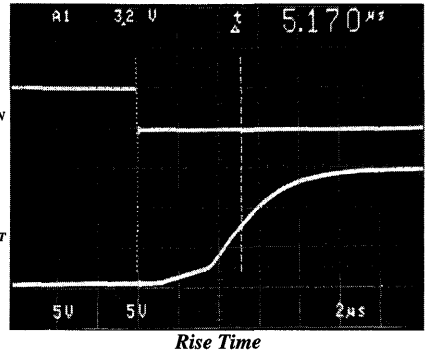
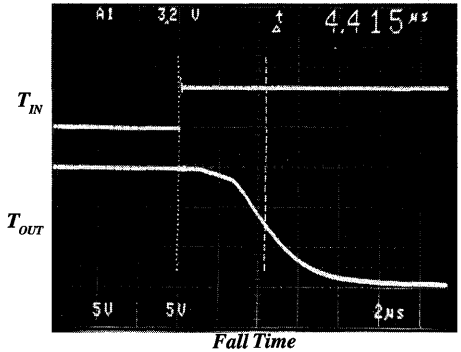


$R_L = 3K\Omega$, $C_L = 2{,}500pF$

Transmitter Propagation Delay

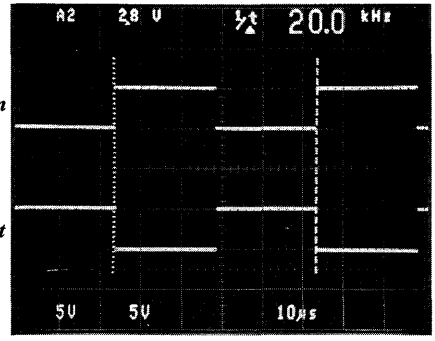


Rise Time
$R_L = 3K\Omega$; $C_L = 2{,}500pF$
All inputs = 20KHz

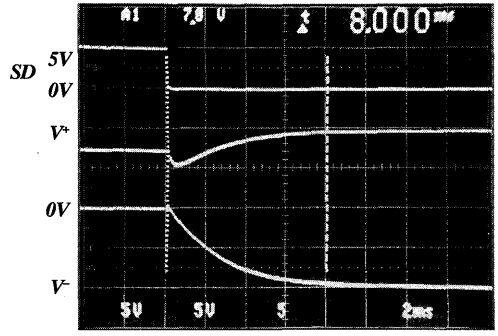


Fall Time
$R_L = 3K\Omega$; $C_L = 2{,}500pF$

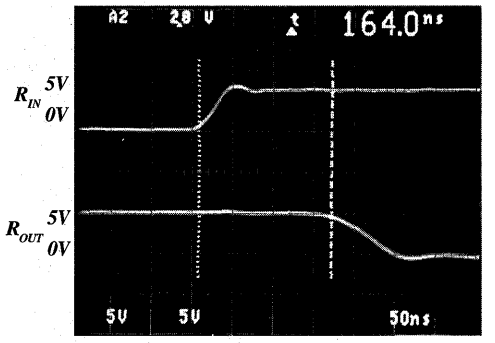
Receiver Output Waveform



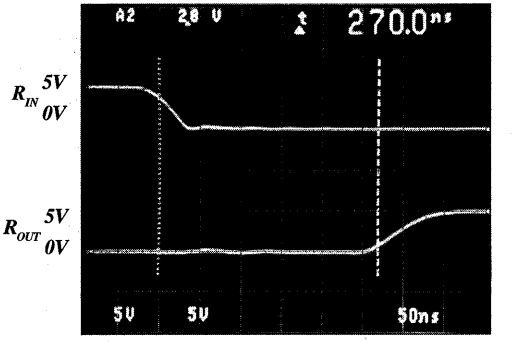
Shutdown to V+, V– Rise Time



Receiver Propagation Delay

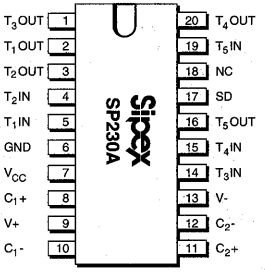


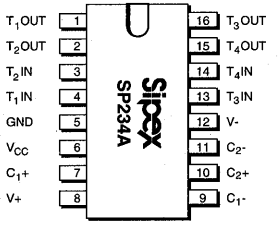
Fall Time

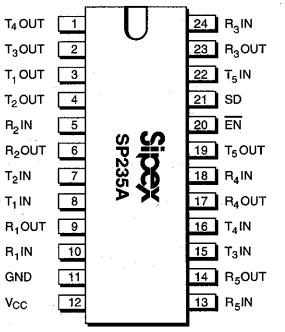


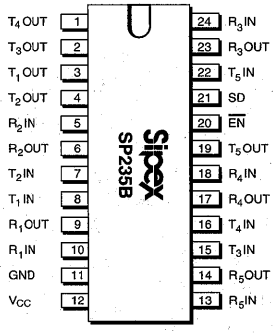
Rise Time

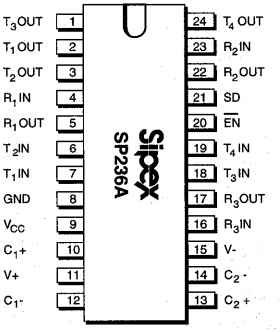
PINOUT

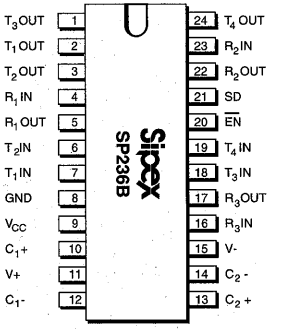




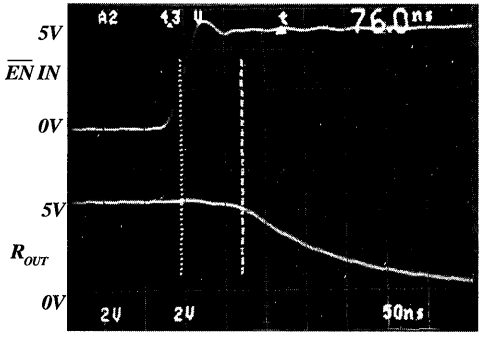




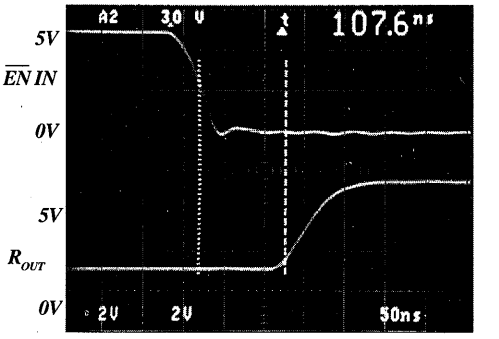




Receiver Output Enable/Disable Times

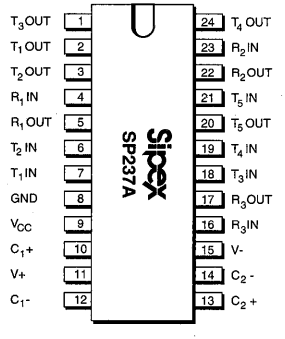


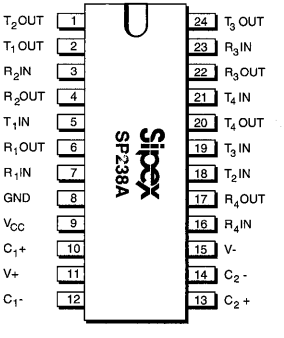
Disable

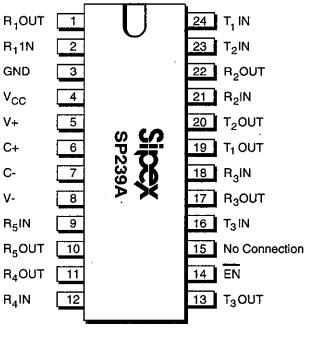


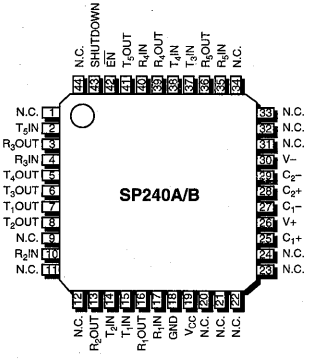
Enable

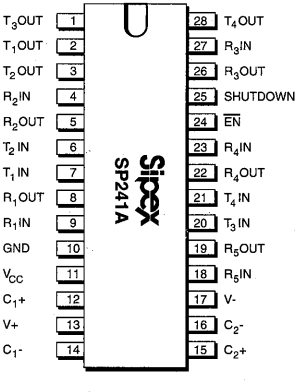
PINOUT

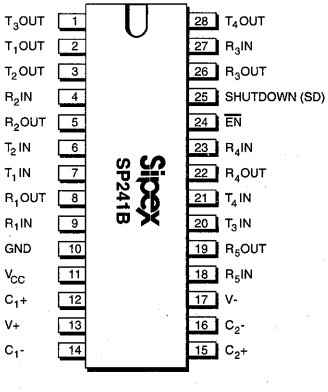












FEATURES...

The multi–channel RS232 line drivers/receivers provides a variety of configurations to fit most communication needs, especially those applications where ±12V is not available. The **SP230A**, **SP235A/B**, **SP236A/B, SP240A/B**, and **SP241A/B** feature a shutdown mode which reduces device power dissipation to less than 5µW. All feature low power CMOS operation, which is particularly beneficial in battery–powered systems. The **SP235A/B** use no external components and are ideally suited where printed circuit board space is limited.

All products in the Series, except the **SP239A**, include two charge pump voltage converters which allow them to operate from a single +5V supply. These converters convert the +5V input power to the ±10V needed to generate the RS232 output levels. The **SP239A** is designed to operate from +5V and +12V supplies. An internal charge pump converter produces the necessary –12V supply. All drivers and receivers meet all EIA RS232D and CCITT V.28 specifications.

The Series are available for use over the commercial, industrial and military temperature ranges. They are packaged in plastic and ceramic DIP, and SOIC packages. For product processed and screened to MIL–M–38510 and MIL–STD–883C requirements, please consult the factory.

THEORY OF OPERATION

The **SP230A/B–241A/B** series devices are made up of three basic circuit blocks — 1) transmitter, 2) receiver and 3) charge pump. Each model within the series incorporates variations of these circuits to achieve the desired configuration and performance.

Driver/Transmitter

The drivers are inverting transmitters, which accept TTL or CMOS inputs and output the RS232 signals with an inverted sense relative to the input logic levels. Typically the RS232 output voltage swing is ±9V. Even under worst-case loading conditions of 3kΩ and 2500pF, the output is guaranteed to be ±5V, which is consistent with the RS232 standard specifications. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

The drivers of the **SP230A, SP235A/B, SP236A/B, SP240A/B** and **SP241A/B** can be tri-stated by using the SHUTDOWN function. In this "power–off" state, the output impedance will remain greater than 300 ohms, again satisfying the RS232 specifications. Should the input of the driver be left open, an internal 400kΩ pull–up resistor to V_{CC} forces the input high, thus committing the output to a low state.

The slew rate of the transmitter output is internally limited to a maximum of 30V/µs in order to meet the

Specification		RS-232D	RS-423A	RS-422	RS-485	RS-562
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential	Single–Ended
Number of Drivers and Receivers Allowed on One Line		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers	1 Driver 1 Receiver
Maximum Cable Length		50 feet	4,000 feet	4,000 feet	4,000 feet	C≤2500pF @ ≤20kb/s C≤1000pF @ ≥20kb/s
Maximum Data Rate		20kb/s	100kb/s	10Mb/s	10Mb/s	64kb/s
Driver Output Maximum Voltage		±25V	±6V	-0.25V to +6V	-7V to +12V	-3.7 to +13.2V
Driver Output Signal Level	Loaded	±5V	±3.6V	±2V	±1.5V	±3.7V
	Unloaded	±15V	±6V	±5V	±5V	±13.2V
Driver Load Impedance		3kΩ to 7kΩ	450Ω min.	100Ω	54Ω	3kΩ to 7kΩ
Maximum Driver Output Current (High Impedance State)	Power On	— —	— —	— —	±100µA	— —
	Power Off	V_{MAX} /300	100µA	±100µA	±100µA	— —
Slew Rate		30V/µs max.	Controls Provided	— —	— —	30V/µs max.
Receiver Input Voltage Range		±15V	±12V	-7V to +7V	-7V to +12V	±15V
Receiver Input Sensistivity		±3V	±200mV	±200mV	±200mV	±3V
Receiver Input Resistance		3kΩto 7kΩ	4kΩ min.	4kΩ min.	12kΩ min.	3kΩ to 7kΩ

Table 1. EIA Standards Definition

standards [EIA 232–D 2.1.7, Paragraph (5)]. The transition of the loaded output from V_{OL} to V_{OH} clearly meets the monotonicity requirements of the standard [EIA 232–D 2.1.7, Paragraphs (1) & (2)].

Receivers

The receivers convert RS232 input signals to inverted TTL signals. Since the input is usually from a transmission line, where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines.

The input thresholds are 0.8V minimum and 2.4V maximum, again well within the ±3V RS232 requirements. The receiver inputs are also protected against voltages up to ±30V. Should an input be left unconnected, a 5kΩ pulldown resistor to ground will commit the output of the receiver to a high state.

In actual system applications, it is quite possible for signals to be applied to the receiver inputs before power is applied to the receiver circuitry. This occurs for example when a PC user attempts to print only to realize the printer wasn't turned on. In this case an RS232 signal from the PC will appear on the receiver input at the printer. When the printer power is turned on, the receiver will operate normally. All series devices are fully protected. Again to facilitate use in "real-world" applications, the receiver outputs can be tri–stated by bringing the ENABLE ($\overline{EN}$) pin high, with the driver remaining full active.

Charge Pump

The charge pump section of the **SP230A** series allows the circuit to operate from a single +5V, ±10% power

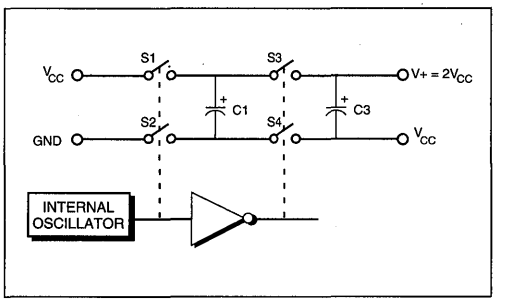


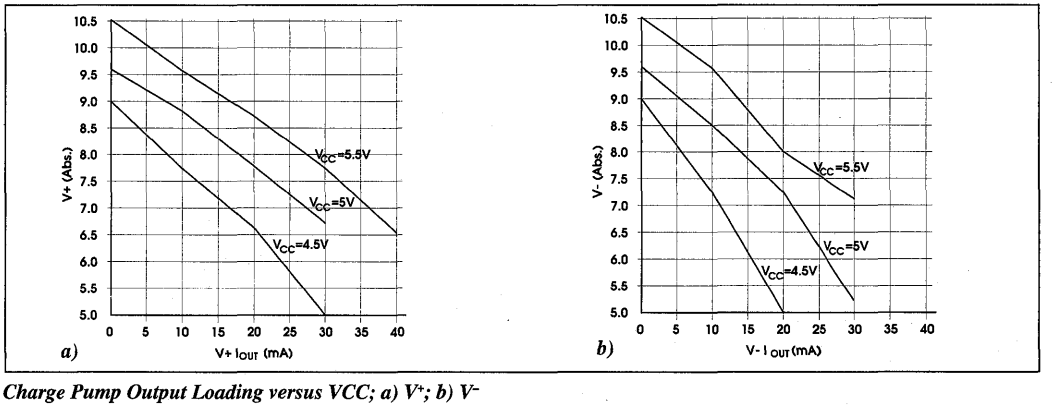
Figure 1. Charge Pump Voltage Doubler

supply by generating the required operating voltages internal to the devices. The charge pump consists of two sections — 1) a voltage doubler and 2) a voltage inverter.

As shown in *Figure 1*, an internal oscillator triggers the charge accumulation and voltage inversion. The voltage doubler momentarily stores a charge on capacitor C_1 equal to V_{CC}, referenced to ground. During the next transition of the oscillator this charge is boot–strapped to transfer charge to capacitor C_3. The voltage across C_3 is now from V_{CC} to V^+.

In the inverter section (Figure 2), the voltage across C_3 is transferred to C_2 forcing a range of 0V to V^+ across C_2. Boot–strapping of C_2 will then transfer charge to C_4 to generate V^-.

The values of the capacitors are somewhat non-critical and can be varied, however the performance will be affected. As C_3 and C_4 are reduced, higher levels of ripple will appear. Lower values of C_1 and C_2 will increase the



Charge Pump Output Loading versus VCC; a) V+; b) V-

SD	$\overline{EN}$	Power Up/Down	Receiver Outputs
0	0	Up	Enable
0	1	Up	Tri–state
1	0	Down	Enable
1	1	Down	Tri–state

Table 2. Wake–Up Truth Table

output impedance of V^+ and V^-, which will degrade V_{OH} and V_{OL}. Capacitor values can be as low as 1.0µF.

Shutdown (SD)

The **SP230A**, **SP235A/B**, **SP236A/B**, **SP240A/B** and **SP241A/B** all feature a control input which will disable the part and reduce V_{CC} current typically to less than 5µA, which is especially useful to designers of battery–powered systems. In the "power–off" mode the receiver and transmitter will both be tri-stated. V^+ will discharge to V_{CC}, and V^- will discharge to ground.

For complete shutdown to occur and the 10µA current drain to be realized, the following conditions must be met:

- +5.00V must be applied to the SD pin;
- ENABLE must either 0V, +5.0V or not connected;
- the transmitter inputs must be either +5.0V or not connected; and
- V_{CC} must be +5V
- Receiver inputs must be >0V and <+5V

Please note that for proper operation, the SD input pin must never be left floating.

ENABLE Input ($\overline{EN}$)

The **SP235A/B**, **SP236A/B**, **SP239A**, **SP240A/B**, and **SP241A/B** all feature an enable input ($\overline{EN}$), which allows the receiver outputs to be either tri–stated or enabled. The enable input is active low; 0V applied to $\overline{EN}$ will enable the receiver outputs. This can be especially useful when the receiver is tied directly to a microprocessor data bus.

Protection From Shorts to >±15V

The driver outputs are protected against shorts to ground, other driver outputs, and V^+ or V^-. For protection against voltages exceeding ±15V, two back–to–back zener diodes connected to clamp the outputs to an acceptable voltage level are recommended. (Refer to *Figure 3.*)

Improved Drive Capability for Mouse Applications

Each of the devices in this data sheet have improved drive capability for non-standard applications. Although the EIA RS232D standards specify the maximum loading to be 3kΩ and 2500pF, the **SP230A**, **SP234A**, **SP235A/B**, **SP236A/B**, **SP237A**, **SP238A**, **SP239**, **SP240A/B**, and **SP241A/B** can typically drive loads as low as 1kΩ and still maintain ±5V outputs. This feature is especially useful when the serial port is intended to be used for a "self-powered" mouse. In this case the voltage necessary to operate the circuits in the mouse can be derived from the RS232 driver output as long as the loading is ≥1kΩ (refer to *Figure 4*). For applications which even exceed this requirement, drivers can be connected in parallel, increasing the drive capability to 750Ω, while maintaining the ±5V V_{OH} and V_{OL} levels (refer to *Figure 5*).

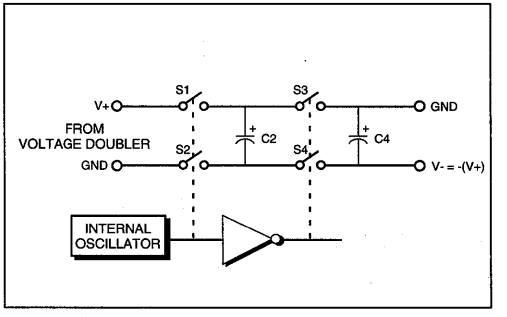


Figure 2. Charge Pump Voltage Inverter

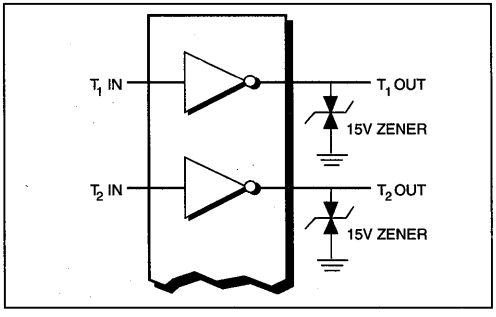


Figure 3. High Voltage Short Circuit Protection

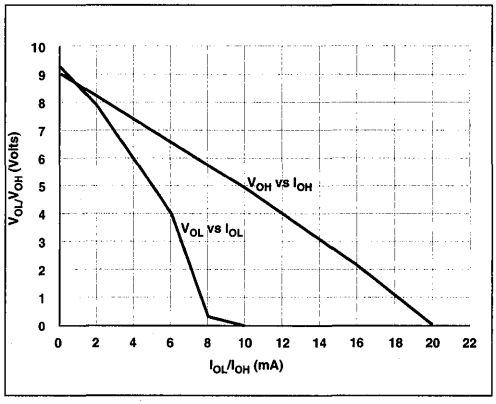


Figure 4. Mouse Application Drive Capability

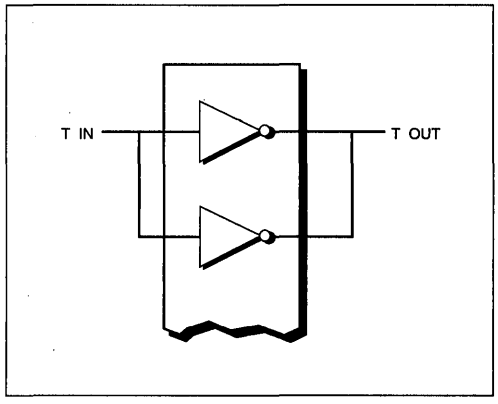
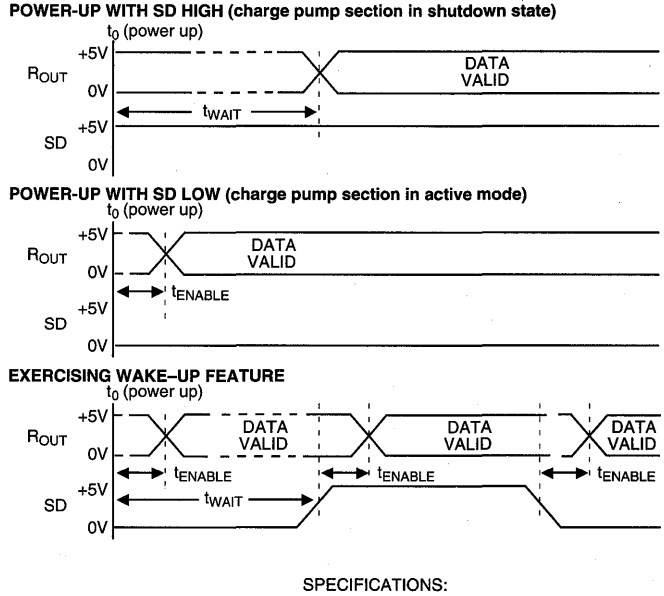


Figure 5. Parallel Drivers

Wake-Up Feature

The **SP235B**, **SP236B**, **SP240B** and **SP241B** have a wake-up feature that keeps all receivers in an enabled state when the device is in the shutdown mode. *Table 2* defines the truth table for the wake-up function. Timing for the wake-up function is shown in *Figure 6*.

If the **SP235B**, **SP236B**, **SP240B** and **SP241B** are powered up in the shutdown state (SD driven high during V_{CC} power up), the part must remain in a powered on state for a minimum of 3ms before the wake-up function can be used. After the 3ms wait time, there is a 2ms delay time before data is valid for both enable and disable



SPECIFICATIONS:
(V_{CC} =+5V±10%, T_A=25°C)

PARAMETER	MIN.	TYP.	MAX.
t_{WAIT}		2ms	3ms
t_{ENABLE}		1ms	2ms

Figure 6. Wake–Up and Shutdown Timing

of the charge pump. If the **SP2XXB** is powered up with SD low, then only the 2ms delay time will apply (refer to *Figure 6*). Under normal operation, both the wait time and delay time should be transparent to the user.

With only the receivers activated, the device typically draws less than 5µA (10µA max) supply current. In the case of a modem interfaced to a computer in power-down mode, the RI (ring indicator) signal from the modem would be used to "wake up" the computer, allowing it to accept the data transmission.

After the ring indicator signal has propagated through the **SP2XXB** receiver, it can be used to trigger the power management circuitry of the computer to power up the microprocessor and bring the SD pin to the **SP2XXB** low, taking it out of shutdown. The receiver propagation delay is typically 1µs. The enable time for V+ and V- is typically 2ms. After V+ and V- have settled to their final values, a signal can be sent back to the modem on the DTR (Data Terminal Ready) pin signifying that the computer is ready to accept and transmit data.

All receivers that are active during shutdown maintain 500m V (typ.) of hystersis.

Varying Capacitor Values

As stated earlier, the capacitor values are somewhat non-critical. Since they are an actual component of the charge pump circuitry, their value will affect its performance, which in turn affects the V_{OH} and V_{OL} levels. There is no upper limit for the value of any of the four capacitors; lower values will impact performance. C_1 and C_2 are responsible for the charge accumulation and can be reduced to 1µF; this will increase the output impedance of V^+ and V^-. Reducing these capacitor values will limit the ability of the **SP2XXA/B** to maintain the dc voltages needed to generate the RS232 output levels. Capacitors C_3 and C_4 can also be reduced to 1µF; doing so will increase the ripple on V^+ and V–.

Typically each driver will require 1µF of capacitance as a minimum to operate within all specified parameters; if five drivers are active in the circuit, then C_3 and C_4 should be 5µF. In order to operate at these minimum values, the supply voltage must be maintained at +5.0V ±5%. Also, the ambient operating temperature must be less than 60°C.

The capacitor values must be chosen to suit the particular application. The designer must balance board space, cost and performance to maximize the design. The capacitors can be polarized or non–polarized, axial-leaded or surface-mount. As the size and value decrease, so does the cost; however, the value should be chosen to accommodate worst-case load conditions.

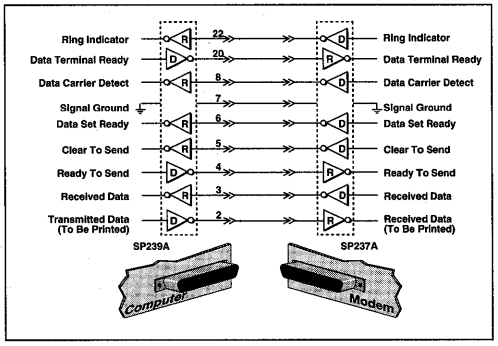
INTERFACE EXAMPLE — A MODEM ON THE IBM PC SERIAL PORT

The RS232 standard defines 22 serial interface signals. These signals consist of ground lines, timing, data, control and test signals, plus a set of signals rarely used for a second data channel. Many of these signal lines are not used in typical RS232 applications; in fact, the IBM® PC serial port is implemented using only nine pins.

For example, consider the case of a PC using this nine pin port to communicate with a peripheral device such as a modem. We see the following activity on each of the RS232 lines as the computer and modem are activated and communicate with each other as well as the remote modem at the other end of the phone line.

Signal Ground (GND)

The Signal Ground pin acts as a reference for all the other signals. This pin is simply maintained at a 0V level to serve as a level to which all other signals are referenced. Both the PC and the modem will have this line connected to their respective internal ground lines.



IBM Modem Port Interconnections

Data Terminal Ready (DTR)
This is the pin the computer uses to tell peripheral devices that it is on–line and ready to communicate.

Data Set Ready (DSR)
Peripheral devices use this line to tell the computer that they are on–line and ready to communicate. When the modem is turned on and has completed its self–test routine (assuming it does one), it will send a signal to the PC by asserting this line.

Request To Send (RTS)
The computer activates this line to notify the peripheral device that it is ready to send data. In this example, the computer notifies the modem that it is ready to send data to be transmitted by the modem.

Clear To Send (CTS)
This is the line on which the peripheral device tells the computer that it is ready to receive data from the computer. If the modem was not ready, i.e. it was performing a loop–back self–test, for example, it would not assert this line. Once the modem was ready to receive data from the PC, it would assert this line. When it receives the **CTS** signal from the modem, the PC knows that a data transmission path has been established between itself and the modem.

Transmitted Data (TD or TX)
This is the pin on which the computer sends the actual data signal to be transmitted, i.e. a positive voltage (+3V to +15V) to represent a logic "0", and a negative voltage (–3V to –15V) to represent a logic "1". The PC would send the data on this line to be transmitted by the modem.

Ring Indicator (RI)
This line is used by the peripheral device to tell the computer that a remote device wants to start communicating. The modem would activate the **RI** line to tell the computer that the remote modem was calling, i.e. the phone is ringing.

Data Carrier Detect (DCD)
This line is used by the modem to tell the computer that it has completed a transmission path with the remote modem, and to expect to start receiving data at any time.

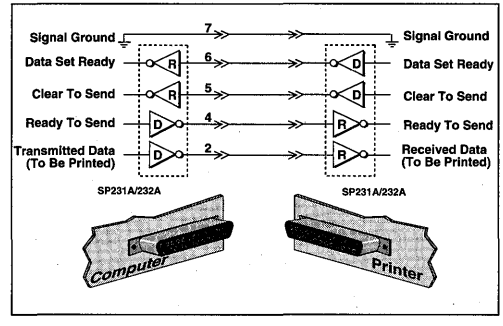
Received Data (RD or RX)
This is the pin on which the modem sends the computer the incoming data signal, i.e. a positive voltage (+3V to +15V) to represent a logic "0", and a negative voltage (-3V to -15V) to represent a logic "1".

INTERFACE EXAMPLE — A PRINTER ON THE IBM PC SERIAL PORT
The RS232 standard defines 22 serial interface signals. These signals consist of ground lines, timing, data, control and test signals, plus a set of signals rarely used for a second data channel. Many of these signal lines are not used in typical RS232 applications; in fact, the IBM® PC serial port is implemented using only nine pins.

For example, consider the case of a PC using this nine pin port to communicate with a peripheral device such as a printe. We see the following activity on each of the RS232 lines as the computer and printer are activated and communicate.

Signal Ground (GND)
The Signal Ground pin acts as a reference for all the other signals. This pin is simply maintained at a 0V level to serve as a level to which all other signals are referenced. Both the PC and the printer will have this line connected to their respective internal ground lines.

Data Terminal Ready (DTR)
This is the pin the computer uses to tell peripheral devices that it is on–line and ready to communi-



IBM Printer Port Interconnections

cate. Once the comuter is powered–up and ready, it will send out a signal on the **DTR** to inform the printer that it is powered–up and ready to go. The printer really doesn't care, since it will simply print data as it is received. Accordingly, this pin is not needed at the printer.

Data Set Ready (DSR)

Peripheral devices use this line to tell the computer that they are on–line and ready to communicate. When the printer is turned on and has completed its self–test routine (assuming it does one), it will send a signal to the PC by asserting this line.

Request To Send (RTS)

The computer activates this line to notify the peripheral device that it is ready to send data. In this example, the computer notifies the printer that it is ready to send data to be printed by the printer.

Clear To Send (CTS)

This is the line on which the peripheral device tells the computer that it is ready to receive data from the computer. If the printer was not ready, i.e. it was out of paper, for example, it would not assert this line. Once the printer was ready to receive data from the PC, it would assert this line. When it receives the **CTS** signal from the printer, the PC knows that a data transmission path has been established between itself and the printer.

Transmitted Data (TD or TX)

This is the pin on which the computer sends the actual data signal representing the actual information to be printed, i.e. a positive voltage (+3V to +15V) to represent a logic "0", and a negative voltage (-3V to -15V) to represent a logic "1".

Ring Indicator (RI)

This line is used by the peripheral device to tell the computer that a remote device wants to start communicating. A modem would activate the **RI** line to tell the computer that a remote modem was calling, i.e. the phone is ringing. In the case of a printer, this line is unused.

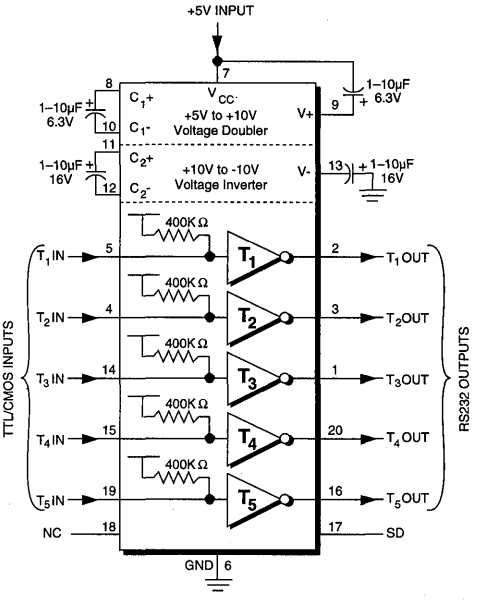
Data Carrier Detect (DCD)

This line is used by a peripheral device to tell the computer to expect to start receiving data at any time. Since the printer would not be sending data to the PC in this case this line is not needed.

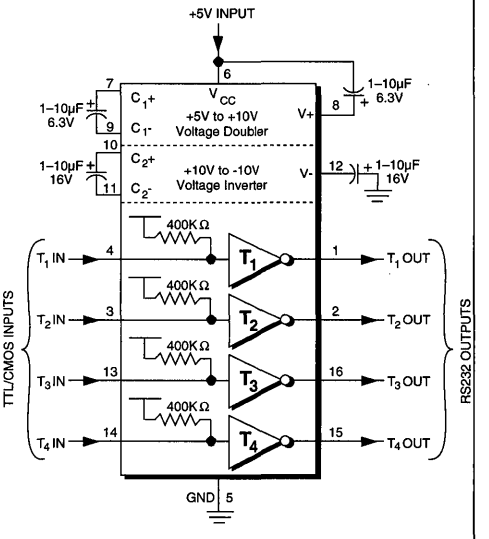
Received Data (RD or RX)

This is the pin on which the computer receives the incoming data signal, i.e. a positive voltage (+3V to +15V) to represent a logic "0", and a negative voltage (-3V to -15V) to represent a logic "1". Again, in this instance, since the printer will not be sending the PC any data, this line is not needed.

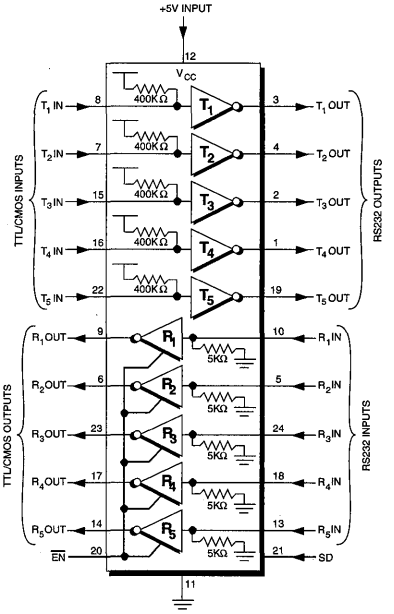
TYPICAL CIRCUITS



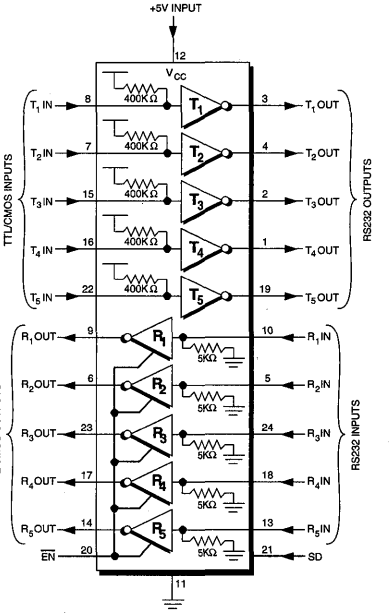
230A



234A

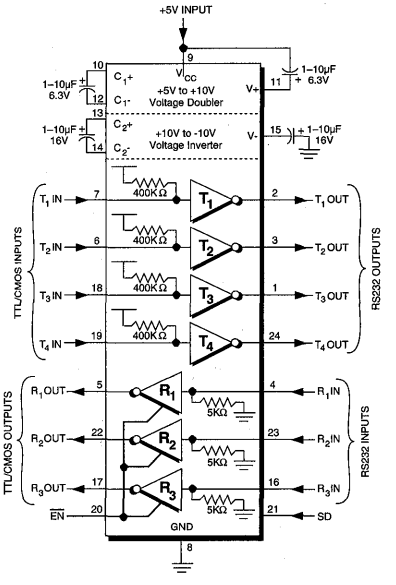


235A

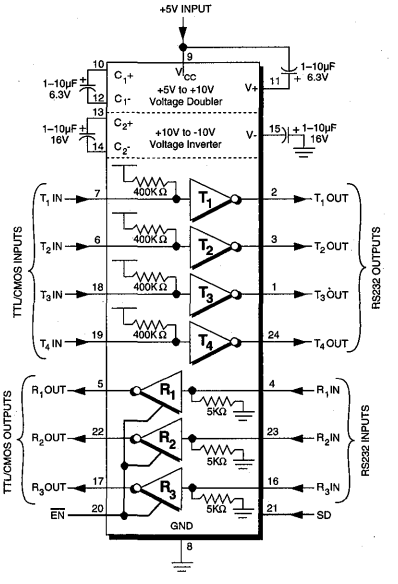


235B

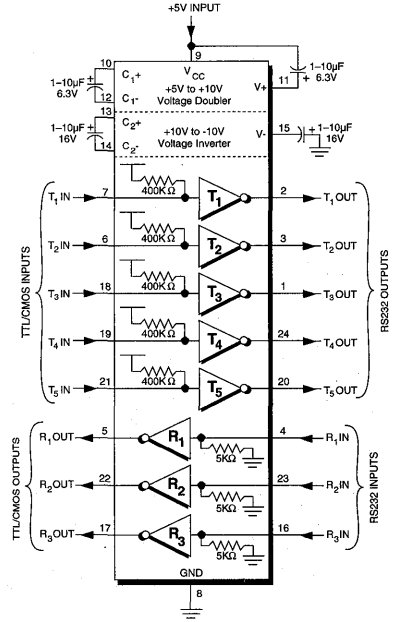
TYPICAL CIRCUITS



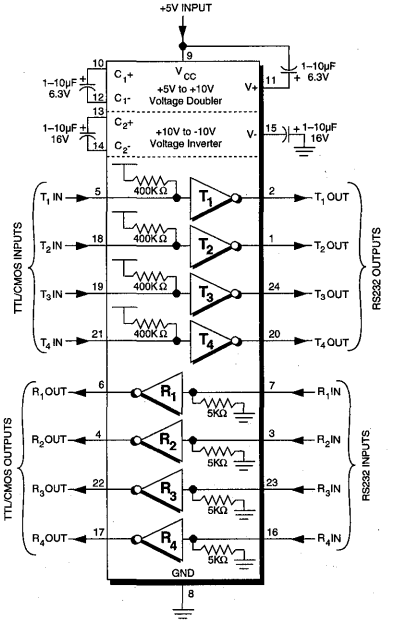
236A



236B

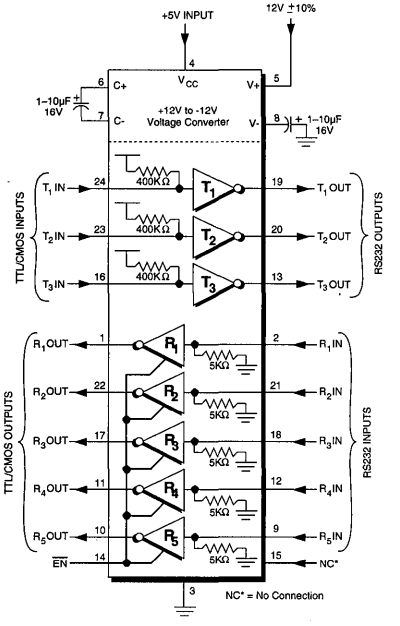


237A

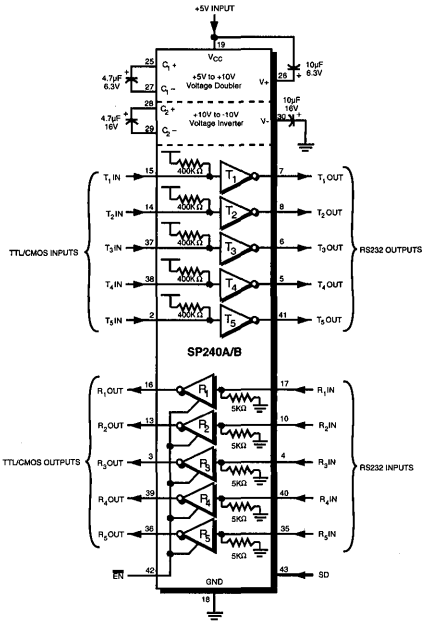


238A

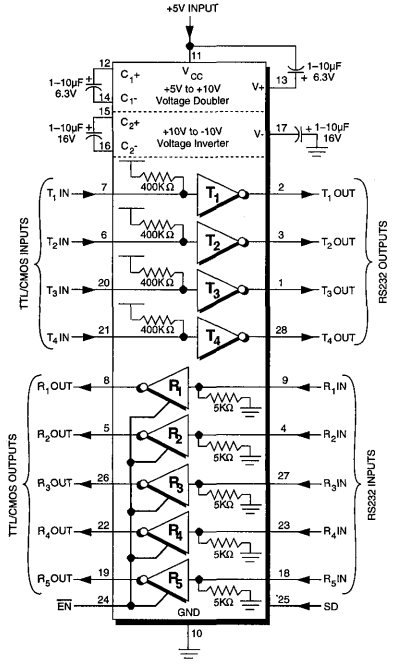
TYPICAL CIRCUITS



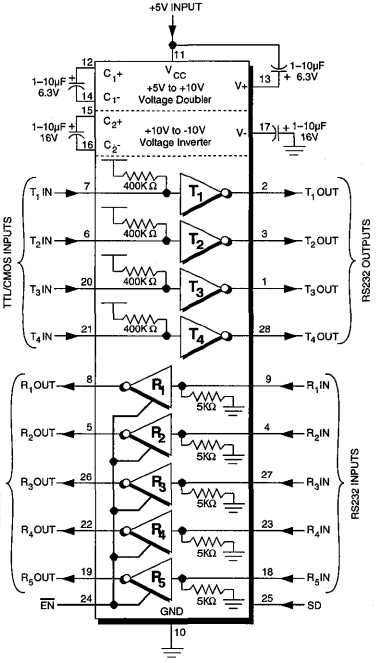
239A



240A/B



241A



241B

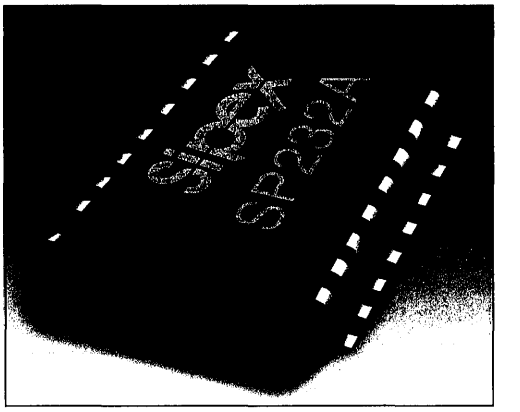
ORDERING INFORMATION

Model	Temperature Range	Package
SP230ACP	0°C to +70°C	20–pin Plastic DIP
SP230ACT	0°C to +70°C	20–pin SOIC
SP230ACX	0°C to +70°C	Dice
SP230AEP	–40°C to +85°C	20–pin Plastic DIP
SP230AET	–40°C to +85°C	20–pin SOIC
SP234ACP	0°C to +70°C	16–pin Plastic DIP
SP234ACT	0°C to +70°C	16–pin SOIC
SP234ACX	0°C to +70°C	Dice
SP234AEP	–40°C to +85°C	16–pin Plastic DIP
SP234AET	–40°C to +85°C	16–pin SOIC
SP235ACP	0°C to +70°C	24–pin Plastic Double–width DIP
SP235AEP	–40°C to +85°C	24–pin Plastic Double–width DIP
SP235BCP	0°C to +70°C	24–pin Plastic Double–width DIP
SP235BEP	–40°C to +85°C	24–pin Plastic Double–width DIP
SP236ACS	0°C to +70°C	24–pin Plastic DIP
SP236ACT	0°C to +70°C	24–pin SOIC
SP236ACX	0°C to +70°C	Dice
SP236AES	–40°C to +85°C	24–pin Plastic DIP
SP236AET	–40°C to +85°C	24–pin SOIC
SP236BCS	0°C to +70°C	24–pin Plastic DIP
SP236BCT	0°C to +70°C	24–pin SOIC
SP236BCX	0°C to +70°C	Dice
SP236BES	–40°C to +85°C	24–pin Plastic DIP
SP236BET	–40°C to +85°C	24–pin SOIC
SP237ACS	0°C to +70°C	24–pin Plastic DIP
SP237ACT	0°C to +70°C	24–pin SOIC
SP237ACX	0°C to +70°C	Dice
SP237AES	–40°C to +85°C	24–pin Plastic DIP
SP237AET	–40°C to +85°C	24–pin SOIC
SP238ACS	0°C to +70°C	24–pin Plastic DIP
SP238ACT	0°C to +70°C	24–pin SOIC
SP238ACX	0°C to +70°C	Dice
SP238AES	–40°C to +85°C	24–pin Plastic DIP
SP238AET	–40°C to +85°C	24–pin SOIC
SP239ACS	0°C to +70°C	24–pin Plastic DIP
SP239ACT	0°C to +70°C	24–pin SOIC
SP239ACX	0°C to +70°C	Dice
SP239AES	–40°C to +85°C	24–pin Plastic DIP
SP239AET	–40°C to +85°C	24–pin SOIC
SP240ACF	0°C to +70°C	44–pin Quad Flatpack
SP240BCF	0°C to +70°C	44–pin Quad Flatpack
SP241ACT	0°C to +70°C	28–pin SOIC
SP241AET	–40°C to +85°C	28–pin SOIC
SP241BCT	0°C to +70°C	28–pin SOIC
SP241BET	–40°C to +85°C	28–pin SOIC

Some –CT and –ET packages available Tape–on–Reel; please consult the factory.

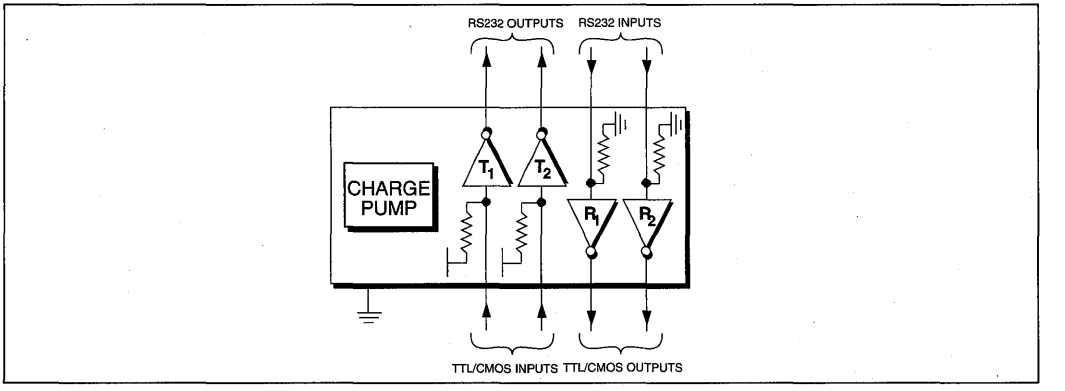
Enhanced RS232 Line Drivers/Receivers

- Operates from Single 5V Power Supply
- Meets All RS232D and V.28 Specifications
- Multiple Drivers and Receivers
- Small Charge Pump Capacitors — 0.1µF
- Operates with 0.1µF and 100µF Capacitors
- High Data Rate — 120Kbps Under Load
- High Output Slew Rate — 10V/µs Under Load
- Low Power Shutdown ≤1µA
- 3-State TTL/CMOS Receiver Outputs
- ±30V Receiver Input Levels
- Low Power CMOS — 15mA Operation



DESCRIPTION...

The **Sipex SP231A**, **SP232A** and **SP233A** are enhanced versions of the **Sipex SP231**, **SP232** and **SP233** RS232 line drivers/receivers. They are pin-for-pin replacements for these earlier versions and will operate in their sockets. Performance enhancements include 10V/µs slew rate, 120K bits per second guaranteed transmission rate, and increased drive current for longer and more flexible cable configurations. Ease of use enhancements include smaller, 0.1µF charge pump capacitors, enhanced ESD protection, low power dissipation and overall ruggedized construction for commercial environments. The Series is available in plastic and ceramic DIP and SOIC packages operating over the commercial, industrial and military temperature ranges.



ABSOLUTE MAXIMUM RATINGS

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +6V
V^+ ..... (Vcc-0.3V) to +13.2V
V^- 13.2V
Input Voltages
T_{IN} ..... -0.3 to (Vcc +0.3V)
R_{IN} ..... ±30V

Output Voltages
T_{OUT} ..... (V+, +0.3V) to (V-, -0.3V)
R_{OUT} ..... -0.3V to (Vcc +0.3V)
Short Circuit Duration
T_{OUT} ..... Continuous
Power Dissipation
CERDIP 675mW
(derate 9.5mW/°C above +70°C)
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

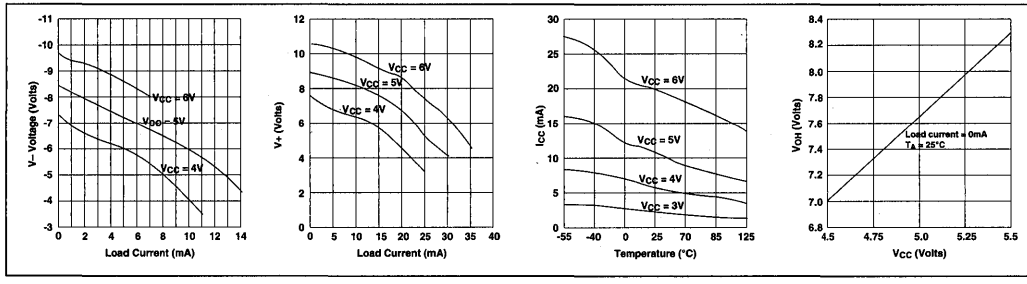
SPECIFICATIONS

V_{CC}=+5V±10%; V+=+8.5V to +13.2V (SP231A only) 0.1µF charge pump capacitors; T_{MIN} to T_{MAX} unless otherwise noted.

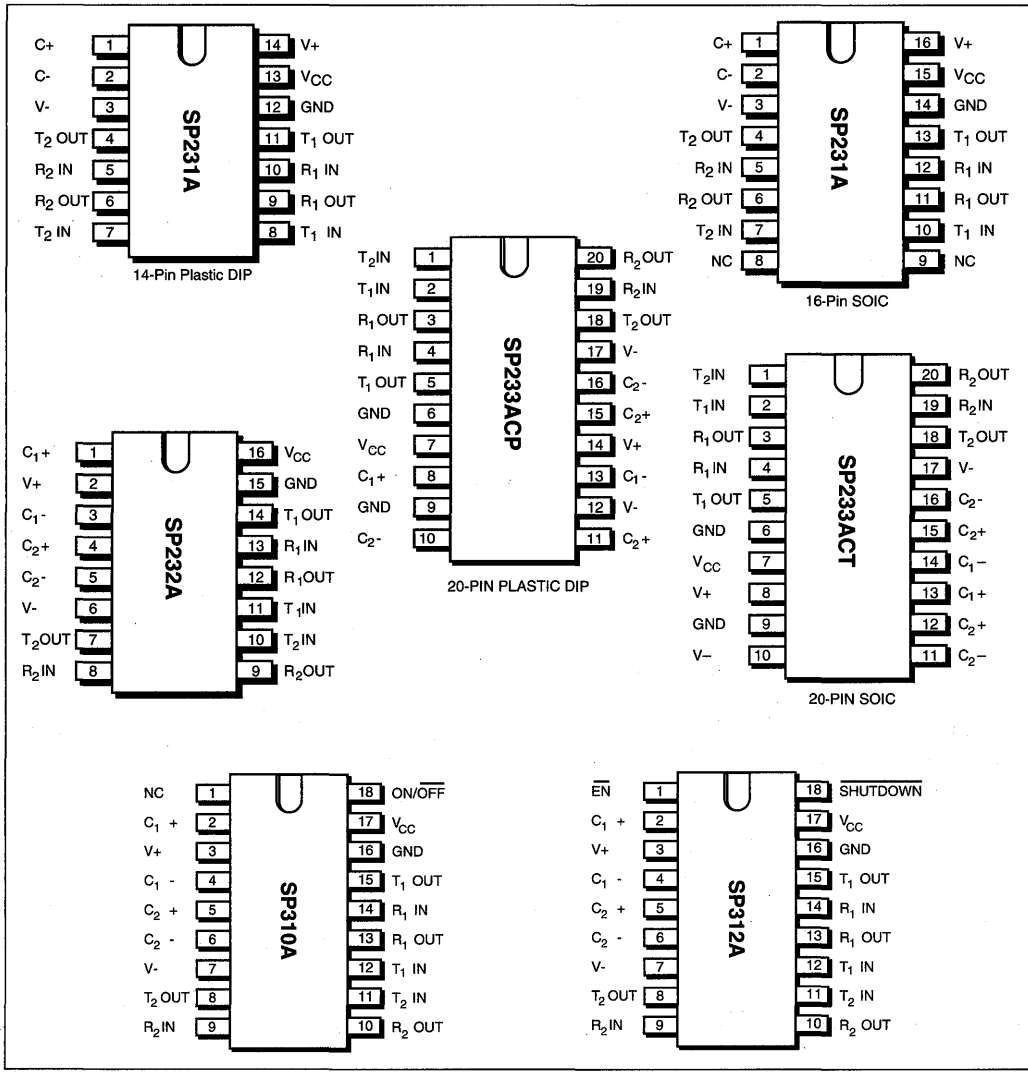
PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TTL INPUT					
Logic Threshold					
Low			0.8	Volts	T_{IN} ; EN, SD
High	2.0			Volts	T_{IN} ; EN, SD
Logic Pullup Current		15	200	µA	T_{IN} = 0V
Data Rate			120	Kbps	C_L = 2500pF, R_L= 3KΩ
TTL OUTPUT					
TTL/CMOS Output					
Voltage, Low			0.4	Volts	I_{OUT} = 3.2mA; Vcc = +5V
Voltage, High	3.5			Volts	I_{OUT} = -1.0mA
Leakage Current **; T_A = +25°		0.05	±10	µA	$\overline{EN}$ = V_{CC}, 0V≤R_{OUT} ≤V_{CC}
RS232 OUTPUT					
Output Voltage Swing	±5	±9		Volts	All transmitter outputs loaded with 3KΩ to Ground
Output Resistance	300			Ohms	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±18		mA	Infinite duration
RS232 INPUT					
Voltage Range	-30		+30	Volts	
Voltage Threshold					
Low	0.8	1.2		Volts	V_{CC} = 5V, T_A = +25°C
High		1.7	2.4	Volts	V_{CC} = 5V, T_A = +25°C
Hysteresis	0.2	0.5	1.0	Volts	V_{CC} = 5V, T_A = +25°C
Resistance	3	5	7	KΩ	
DYNAMIC CHARACTERISTICS					
Propagation Delay, RS232 to TTL		1.5		µS	
Instantaneous Slew Rate			30	V/µS	C_L = 10pF, R_L= 3 - 7KΩ; T_A =+25°C
Transition Region Slew Rate		10		V/µs	C_L = 2500pF, R_L= 3KΩ; measured from +3V to -3V or -3V to +3V
Output Enable Time **		400		ns	SP310A and SP312A only
Output Disable Time **		250		ns	SP310A and SP312A only
POWER REQUIREMENTS					
V_{CC} Power Supply Current		10	15	mA	No load, T_A= +25°C; V_{CC} = 5V
		25		mA	All transmitters R_L = 3KΩ; T_A = +25°C
V+ Power Supply Current ***		5	10	mA	No load, V+ = 12V
Shutdown Supply Current **		1	10	µA	V_{CC} = 5V, T_A = +25°C

SP310A and **SP312A** only; *** **SP231A** only

PERFORMANCE CURVES



PINOUT...



FEATURES...

The **Sipex SP231A**, **SP232A** and **SP233A** are enhanced versions of the **Sipex SP231**, **SP232** and **SP233** RS232 line drivers/receivers. They are pin-for-pin replacements for these earlier versions, will operate in their sockets with capacitors ranging from 0.1 to 100µF, either polarized or non–polarized, and feature several improvements in both performance and ease of use. Performance enhancements include 10V/µs slew rate, 120K bits per second guaranteed transmission rate, and increased drive current for longer and more flexible cable configurations. Ease of use enhancements include smaller, 0.1µF charge pump capacitors, enhanced ESD protection, low power dissipation and overall ruggedized construction for commercial environments.

The **SP232A**, **SP233A**, **SP310A** and **SP312A** include charge pump voltage converters which allow them to operate from a single +5V supply. These converters convert the +5V input power to the ±10V needed to generate the RS232 output levels. Both meet all EIA RS232D and CCITT V.28 specifications. The **SP231A** has provisions for external V+ supplies. With this power supplied externally, the current drain due to charge pump operation is considerably reduced, typically to 400µA.

The **SP310A** provides identical features as the **SP232A**. The **SP310A** has a single control line which simultaneously shuts down the internal DC/DC converter and puts all transmitter and receiver outputs into a high impedance state. The **SP312A** is identical to the **SP310A** with separate tri-state and shutdown control lines.

The **SP231A** is available in 14-pin plastic DIP, CERDIP and 16-pin SOIC packages for operation over commercial, industrial and military temperature ranges. The **SP232A** is available in 16-pin plastic DIP, SOIC and CERDIP packages, operating over the commercial, industrial and military temperature ranges. The **SP233A** is available in a 20-pin plastic DIP and 20–pin SOIC package for operation over the commercial and industrial temperature ranges. The **SP310A** and **SP312A** are available in 18-pin plastic, CERDIP and SOIC packages for operation over the commercial and industrial temperature ranges. Please consult the factory for DIP and surface-mount packaged parts supplied on tape-on-reel, as well as parts screened to MIL-M-38510.

THEORY OF OPERATION

The **SP231A**, **SP232A, SP233A**, **SP310A** and **SP312A** devices are made up of three basic circuit blocks — 1) a driver/transmitter, 2) a receiver and 3) a charge pump. Each block is described below.

Driver/Transmitter

The drivers are inverting transmitters, which accept TTL or CMOS inputs and output the RS232 signals with an inverted sense relative to the input logic levels. Typically the RS232 output voltage swing is ±9V. Even under worst case loading conditions of 3kohms and 2500pF, the output is guaranteed to be ±5V, which is consistent with the RS232 standard specifications. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

The instantaneous slew rate of the transmitter output is internally limited to a maximum of 30V/µs in order to meet the standards [EIA 232-D 2.1.7, Paragraph (5)]. However, the transition region slew rate of these enhanced products is typically 10V/µs. The smooth transition of the loaded output from V_{OL} to V_{OH} clearly meets the monotonicity requirements of the standard [EIA 232-D 2.1.7, Paragraphs (1) & (2)].

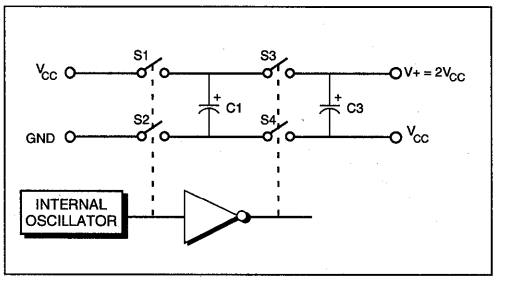


Figure 1. Charge Pump Voltage Doubler

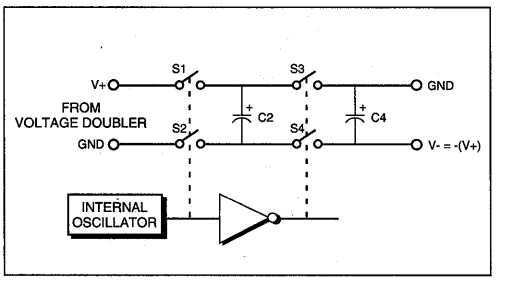


Figure 2. Charge Pump Voltage Inverter

Receivers

The receivers convert RS232 input signals to inverted TTL signals. Since the input is usually from a transmission line, where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines.

The input thresholds are 0.8V minimum and 2.4V maximum, again well within the ±3V RS232 requirments. The receiver inputs are also protected against voltages up to ±30V. Should an input be left unconnected, a 5kohm pulldown resistor to ground will commit the output of the receiver to a high state.

In actual system applications, it is quite possible for signals to be applied to the receiver inputs before power is applied to the receiver circuitry. This occurs for example when a PC user attempts to print only to realize the printer wasn't turned on. In this case an RS232 signal from the PC will appear on the receiver input at the printer. When the printer power is turned on, the receiver will operate normally. All of these enhanced devices are fully protected.

Charge Pump

The charge pump section of the these devices allows the circuit to operate from a single +5V ±10% power supply by generating the required operating voltages internal to the devices. The charge pump consists of two sections — 1) a voltage doubler and 2) a voltage inverter.

As shown in *Figure 1*, an internal oscillator triggers the charge accumulation and voltage inversion. The voltage doubler momentarily stores a charge on capacitor C_1 equal to V_{cc}, referenced to ground. During the next transition of the oscillator this charge is boot-strapped to transfer charge to capacitor C_3. The voltage across C_3 is now from V_{cc} to V^+.

In the inverter section *(Figure 2)*, the voltage across C_3 is transferred to C_2 forcing a range of 0V to V^+ across C_2. Boot-strapping of C_2 will then transfer charge to C_4 to genrate V^-.

One of the significant enhancements over previous products of this type is that the values of the capacitors are no longer critical and have been decreased in size considerably to 0.1µF. Because the charge pump runs at a much higher frequency, the 0.1µF capacitors are sufficient to transfer and sustain charges to the two transmitters.

APPLICATION HINTS

Protection From Shorts to ±15V

The driver outputs are protected against shorts to ground, other driver outputs, and V^+ or V^-. If the possibility exists that the outputs could be inadvertently connected to voltages higher than ±15V, then it is recommended that external protection be provided. For protection against voltages exceeding ±15V, two back-to-back zener diodes connected from each output to ground will clamp the outputs to an acceptable voltage level.

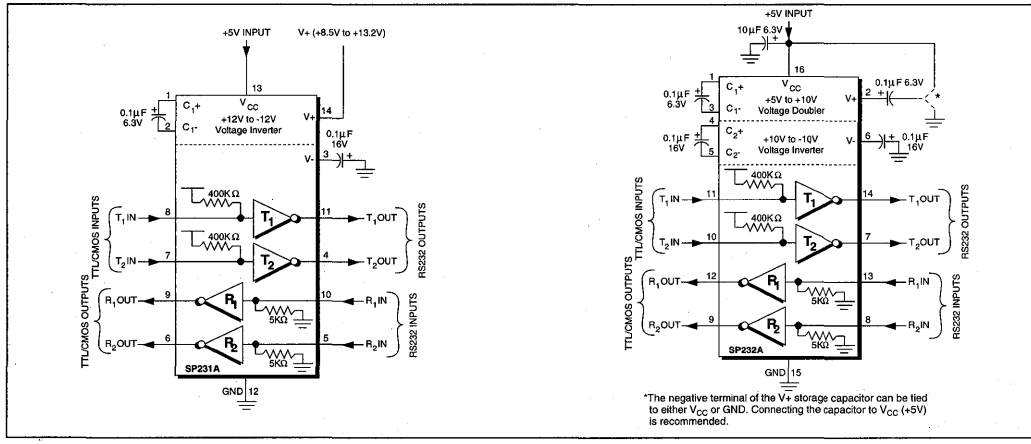


Figure 3. Typical Circuits using the SP231A and 232A.

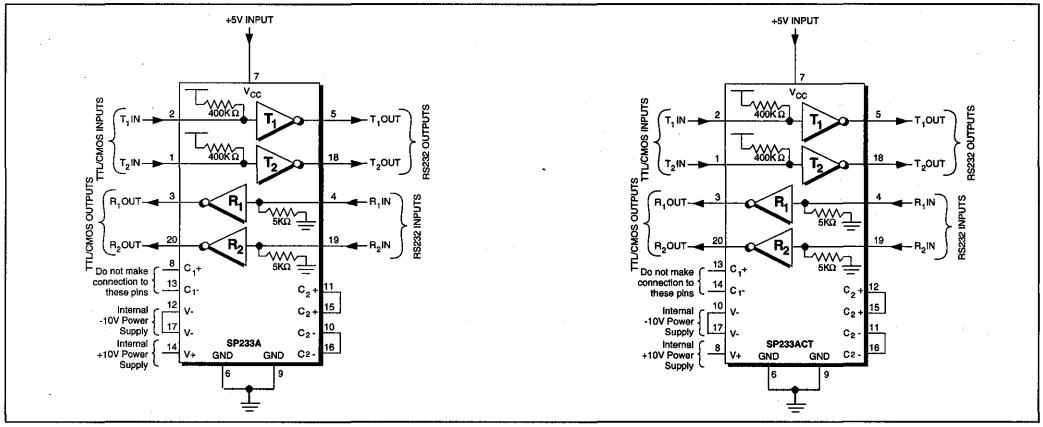


Figure 4. Typical Circuits using the SP233ACP and SP233ACT

Shutdown ($\overline{SD}$) and Enable ($\overline{EN}$) — SP310A/SP312A Only

Both the **SP310A** and **SP312A** have a shut-down/ standby mode to conserve power in battery-powered systems. To activate the shutdown mode, which stops the operation of the charge pump, a logic "0" is applied to the appropriate control line. For the **SP310A**, this control line is ON/OFF (pin 18). Activating the shutdown mode also puts the **SP310A** transmitter and receiver outputs in a high impedance condition (tri-stated). The shutdown mode is controlled on the **SP312A** by a logic "0" on the $\overline{SHUTDOWN}$ control line (pin 18); this also puts the transmitter outputs in a tri–state mode. The receiver outputs can be tri–stated separately during normal operation or shutdown by a logic "1" on the ENABLE line (pin 1).

Wake–Up Feature (SP312A Only)

The **SP312A** has a wake–up feature that keeps all the receivers in an enabled state when the device is in the shutdown mode. *Table 1* defines the truth table for the wake–up function.

With only the receivers activated, the **SP312A** typically draws less than 5µA supply current (10µA maximum). In the case of a modem interfaced to a computer in power down mode, the Ring Indicator (RI) signal from the modem would be used to "wake up" the computer, allowing it to accept data transmission.

After the ring indicator signal has propagated through the **SP312A** receiver, it can be used to trigger the power management circuitry of the computer to power up the microprocessor, and bring the $\overline{SD}$ pin of the **SP312A** to a logic high, taking it out of the shutdown mode. The receiver propagation delay is typically 1µs. The enable time for V^+ and V^- is typically 2ms. After V^+ and V^- have settled to their final values, a signal can be sent back to the modem on the data terminal ready (DTR) pin signifing that the computer is ready to accept and transmit data.

Pin Strapping — SP233ACT Only

The **SP233A** packaged in the 20–pin SOIC package (**SP233ACT**) has a slightly different pinout than the **SP233A** in other package configurations. To operate properly, the following pairs of pins must be externally wired together:

the two V– pins (pins 10 and 17)
the two C_2+ pins (pins 12 and 15)
the two C_2– pins (pins 11 and 16)

All other connections, features, functions and performance are identical to the **SP233A** as specified elsewhere in this data sheet.

$\overline{SD}$	$\overline{EN}$	Power Up/Down	Receiver Outputs
1	0	Down	Enable
1	1	Down	Tri–state
0	0	Up	Enable
0	1	Up	Tri–state

Table 1. Wake-up Function Truth Table.

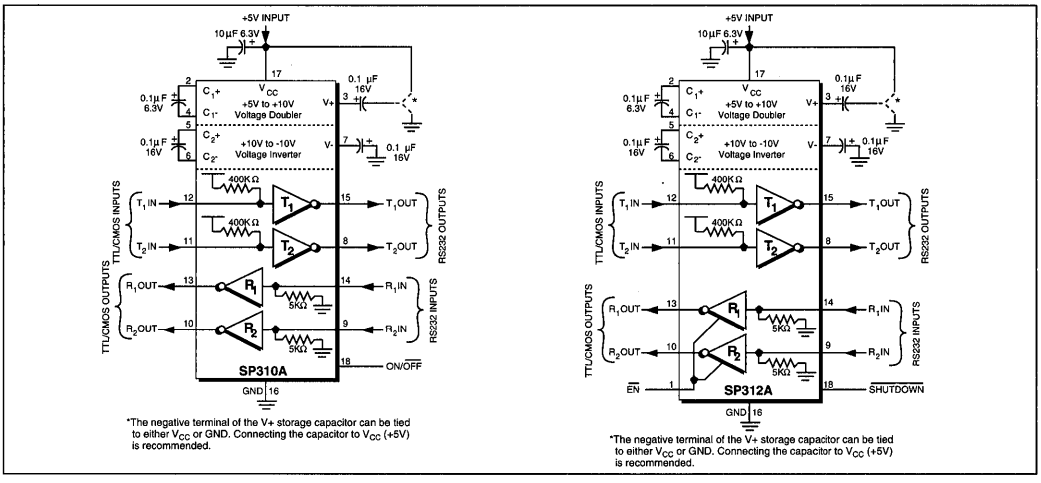


Figure 5. Typical Circuits using the SP310A and SP312A

ORDERING INFORMATION

Model	Temperature Range	Package
SP231ACP	0°C to +70°C	14–pin Plastic DIP
SP231ACT	0°C to +70°C	16–pin SOIC
SP231ACX	0°C to +70°C	Dice
SP231AEP	–40°C to +85°C	14–pin Plastic DIP
SP231AET	–40°C to +85°C	16–pin SOIC
SP232ACN	0°C to +70°C	16–pin N–SOIC
SP232ACP	0°C to +70°C	16–pin Plastic DIP
SP232ACT	0°C to +70°C	16–pin SOIC
SP232ACX	0°C to +70°C	Dice
SP232AEP	–40°C to +85°C	16–pin Plastic DIP
SP232AET	–40°C to +85°C	16–pin SOIC
SP233ACP	0°C to +70°C	20–pin Plastic DIP
SP233ACT	0°C to +70°C	20–pin SOIC
SP233AEP	–40°C to +85°C	20–pin Plastic DIP
SP233AET	–40°C to +85°C	20–pin SOIC
SP310ACP	0°C to +70°C	18–pin Plastic DIP
SP310ACT	0°C to +70°C	18–pin SOIC
SP310ACX	0°C to +70°C	Dice
SP310AEP	–40°C to +85°C	18–pin Plastic DIP
SP310AET	–40°C to +85°C	18–pin SOIC
SP312ACP	0°C to +70°C	18–pin Plastic DIP
SP312ACT	0°C to +70°C	18–pin SOIC
SP312ACX	0°C to +70°C	Dice
SP312AEP	–40°C to +85°C	18–pin Plastic DIP
SP312AET	–40°C to +85°C	18–pin SOIC

CT and ET packages available Tape–on–Reel. Please consult the factory for pricing and availability for this option, and for parts screened to MIL–STD–883.

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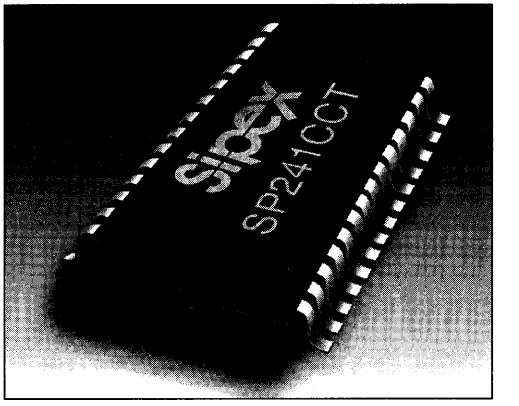
SP241C

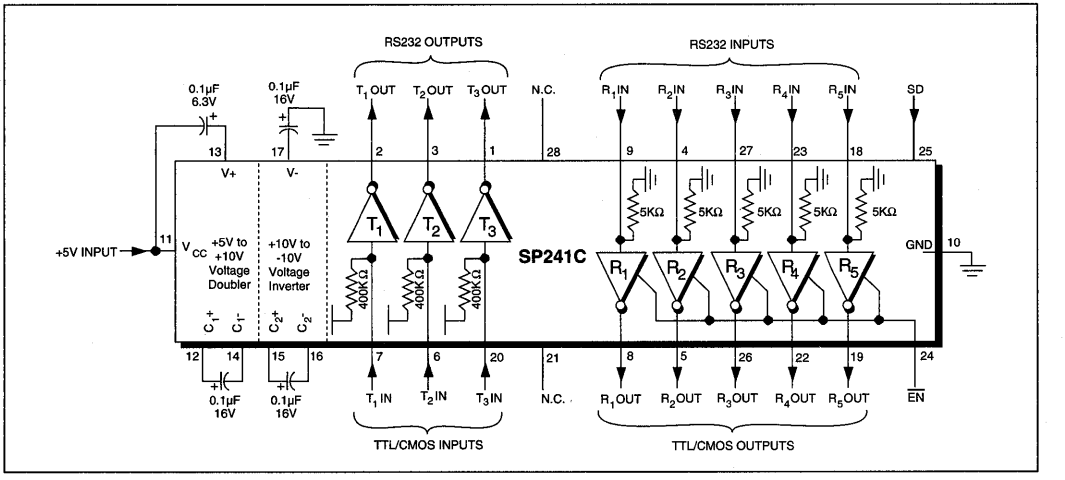
Enhanced +5V Powered Multi–Channel RS232 Drivers/Receivers

- Operate From Single +5V Power Supply
- Meets all RS232D and V.28 Specifications
- 3 Drivers and 5 Receivers
- High Data Rate:
  120 Kbits/sec @ 2,500 pF Load
- Small Charge Pump Capacitors; 0.1µF
- ±30V Receiver Input Levels
- 3-State TTL/CMOS Receiver Outputs with Wake-up Feature
- Power Management Circuit to Optimize Power Consumption/Performance
- Low Power CMOS: 4 mA Operation
- Low Power Shutdown Current: <1µA



DESCRIPTION...

The Sipex **SP241C** is an enhanced version of Sipex **SP241** line drivers/receivers which operate at +5V. The **SP241C** is pin–compatible with the older **SP241** except that operation has been optimized by incorporating only three (3) drivers. Performance enhancements include 120 Kbits/sec guaranteed transmission rate, 10V/µS slew rate, and long cable drive capability. The **SP241C** includes charge pump voltage converters which allow it to operate from a single +5V power supply, with charge pump and decoupling capacitors of 0.1µF minimum.



ABSOLUTE MAXIMUM RATINGS

This is a stress rating only and functional operation of the device at these or any other above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{cc} ..... +6 V
V+ ..... (Vcc–0.3V) to +13.2V
V- 13.2V
Input Voltages
T_{IN} ..... –0.3V to (Vcc +0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+, +0.3V) to (V–, –0.3V)
R_{OUT} ..... –0.3V to (Vcc +0.3V)
Short Circuit Duration
T_{OUT} ..... Continuous
Power Dissipation
CERDIP 675mW
(derate 9.5mW/°C above +70°C)
Plastic Dip 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

SPECIFICATIONS

V_{CC} = 5V ± 10%, 0.1µF charge pump capacitors; T_{MIN} to T_{MAX} unless otherwise noted.

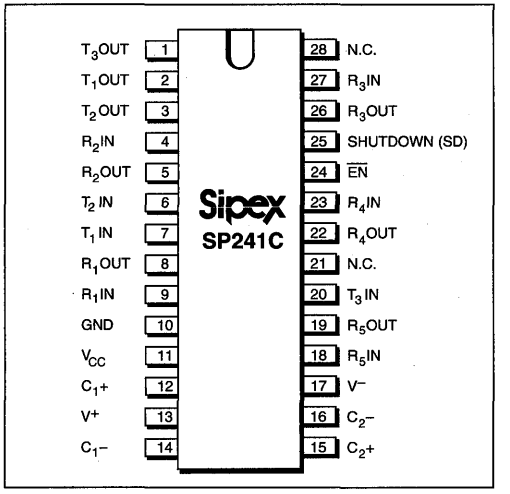
PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TTL INPUT					
Logic Threshold					
Low			0.8	Volts	T_{IN}; $\overline{EN}$, SD
High	2.0			Volts	T_{IN}; $\overline{EN}$, SD
Logic Pullup Current		15	200	µA	T_{IN} = 0V
Data Rate			120	Kbits/sec	C_L = 2500pF, R_L = 3KΩ,
TTL OUTPUT					
TTL CMOS Output Voltage					
Low			0.4	Volts	I_{OUT} = 3.2mA; V_{CC} = +5V
High	3.5			Volts	I_{OUT} = –1.0mA
Leakage Current		0.05	±10	µA	$\overline{EN}$=V_{CC}, 0V≤R_{OUT}≤V_{CC}; T_A=+25°C
RS232 OUTPUT					
Output Voltage Swing	±5	±7		Volts	All transmitter outputs loaded with 3KΩ to Ground
Output Resistance	300			Ohms	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±25		mA	Infinite duration
RS232 INPUT					
Voltage Range	-30		+30	Volts	
Voltage Threshold					
Low	0.8	1.2		Volts	V_{CC} = 5V, T_A = +25°C
High		1.7	2.4	Volts	V_{CC} = 5V, T_A = +25°C
Hysteresis	0.2	0.5	1.0	Volts	Vcc = 5V
Resistance	3	5	7	KΩ	T_A = +25°C
DYNAMIC CHARACTERISTICS					
Propagation Delay		1.5		µs	RS232 to TTL
Instantaneous Slew Rate			30	V/µs	C_L = 10pF, R_L = 3-7KΩ; T_A = +25°C
Transition Region Slew Rate		10		V/µs	C_L = 2500pF, R_L=3KΩ; measured from +3V to –3V or –3V to +3V
Output Enable Time		400		ns	
Output Disable Time		250		ns	

SPECIFICATIONS

V_{CC} = 5V ± 10%, 0.1µF charge pump capacitors; T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
POWER REQUIREMENTS					
Vcc Power Supply Current		4	10	mA	No load, T_A = +25°C; V_{CC} = +5V
		20		mA	All transmitters R_L=3KΩ; T_A=+25°C
Shutdown Supply Current		1	10	µA	T_A = +25°C
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range					
Commercial; –_C	0		+70	°C	
Industrial; –_E	–40		+85	°C	
Storage Temperature Range	–55		+125	°C	
Package					
–__T		28–pin SOIC			
–__A		28–pin SSOP			

SP241C PINOUT



EIA RS232 STANDARDS

The Electronic Industry Association (EIA) developed several standards of data transmission which are revised and updated in order to meet the requirements of the industry. In data processing, there are two basic means of communicating between systems and components. The RS232 standard defines a single-ended communication method, while the RS422 standard defines a differential method. The RS232 standard was first introduced in 1962, and since that time has become an industry standard.

RS232 is a relatively slow data exchange protocol, with a maximum baud rate of only 20kbaud, which can be transmitted over a maximum copper wire cable length of 50 feet. The **SP241C** has been designed to meet both the EIA protocol standards and the needs of the industry.

THEORY OF OPERATION

The **SP241C** is made up of three basic circuit blocks — 1) a driver/transmitter, 2) a receiver and 3) a charge pump. All three circuit blocks have been designed with enhanced performance of earlier designs.

Driver/Transmitter

The drivers are inverting transmitters, which accept TTL or CMOS inputs and output the RS232 signals with an inverted sense relative to the input logic levels. Typically the RS232 output voltage swing is ±9V. Even under worst case loading conditions of 3kohms and 2500pF, the output is guaranteed to be ±5V, which is consistent with the RS232 standard specificaitons. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

The drivers of the **SP241C** can be tri-stated by using the SHUTDOWN function. In the "power-off" state, the output impedance will remain greater than 300 ohms, again satisfying the RS232 specifications.

Should the input of the driver be left open, an internal 400kohm pull-up resistor to Vcc forces the input high, thus committing the output to a low state.

The slew rate of the transmitter output is internally limited to a maximum of 30V/µs in order to meet the standards [EIA 232-D 2.1.7, Paragraph (5)]. The smooth transition of the loaded output from V_{OL} to V_{OH} clearly meets the monotonicity requirements of the standard [EIA 232-D 2.1.7, Paragraphs (1) & (2)].

Enhanced Driver Performance

Enhancements to the standard requirements of the RS232 drivers include high data rate, and high current drive. Because the drivers can typically achieve a 10V/µS slew rate, the data rate is guaranteed to 120 Kbits/sec even under full load conditions of 3KΩ and 2500pF. For applications that exceed the EIA RS232 standards for loading, the SP241C can maintain ±5V swings at loads as low as 750Ω, see *Figure 1*.

Receivers

The receivers convert RS232 input signals to inverted TTL signals. Since the input is usually from a transmission line, where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines.

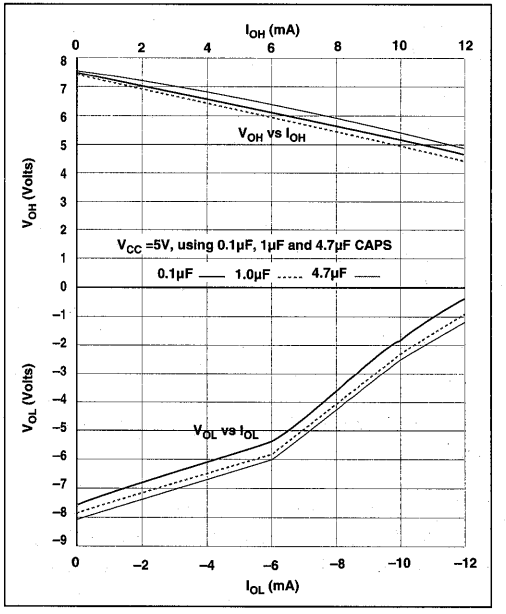


Figure 1. Enhanced Driver Performance

The input thresholds are 0.8V minimum and 2.4V maximum, again well within the ±3V RS232 requirements. The receiver inputs are also protected against voltages up to ±30V. Should an input be left unconnected, a 5kohm pulldown resistor to ground will commit the output of the receiver to a high state.

In actual system applications, it is quite possible for signals to be applied to the receiver inputs before power is applied to the receiver circuitry. This occurs for example when a PC user attempts to print only to realize the printer wasn't turned on. In this case an RS232 signal from the PC will appear on the receiver input at the printer. When the printer power is turned on, the receiver will operate normally. The **SP241C** is fully protected. Again to facilitate use in "real-world" applications, the receiver outputs can be tri-stated by bringing the ENABLE (EN) pin low, with the drivers remaining full active.

Enhanced Receiver Performance

The receivers also have been designed to surpass the EIA RS232 standard data requirements. Although the standard RS232 data rate is 20Kbaud, the **SP241C** can accept data up to a guaranteed rate of 120 Kbits/sec.

The receivers have been designed to operate with very low power. This allows all the receivers to remain active while the part is in shutdown mode, and still keep Icc<10µA. This feature is called "wake-up" and is explained in detail under Key Features on page 4.

Charge Pump

The charge pump section of the **SP241C** allows the circuit to operate from a single +5V ±10% power supply by generating the required operating voltages internal to the devices. The charge pump consists of two sections — 1) a voltage doubler and 2) a voltage inverter.

As shown in *Figure 2*, an internal oscillator triggers the charge accumulation and voltage inversion. The voltage doubler momentarily stores a charge on capacitor C_1 equal to V_{CC}, referenced to ground. During the next transition of the oscillator this charge is bootstrapped to transfer charge to capacitor C_3. The voltage across C_3 is now from Vcc to V+.

In the inverter section *Figure 3*, the voltage across C_3 is transferred to C_2 forcing a range of 0V to V^+ across

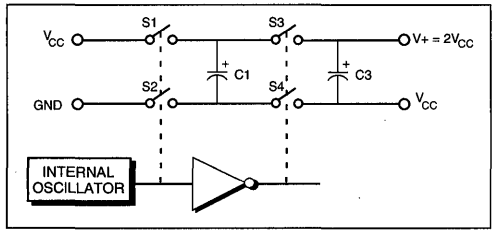


Figure 2. Charge Pump Voltage Doubler

C_2. Boot-strapping of C_2 will then transfer charge to C_4 to generate V^-.

The values of the capacitors are somewhat non-critical and can be varied, however the performance will be affected. As C_3 and C_4 are reduced, higher levels of ripple will appear. Lower values of C_1 and C_2 will increase the output impedance of V^+ and V^-, which will degrade V_{OH} and V_{OL}.

Enhanced Charge Pump Performance

The charge pump of the **SP241C** is an improved version of the original design. Although the basic operation is similar the capacitor requirements have been reduced to 0.1µF for both the charging and storage capacitors, and the current drive has been greatly increased; Icc however is still a guaranteed 10mA.

The **SP241C** is final tested at all appropriate temperatures using four 0.1µF ceramic capacitors. This guaranteed performance with the small capacitors minimizes board space while maximizing performance. Even with the small caps the drivers can typicaly drive loads as low as 750Ω. Figure 1, shows V_{OH} and V_{OL} vs load current.

KEY FEATURES

Shutdown (SD)

The **SP241C** features a control input which will disable the part and reduce Vcc current typically to less than 10µA, which is especially useful to designers of battery-powered systems. In the "power-off" mode the receiver and transmitter will both be tri-stated. V^+ will discharge to V_{CC}, and V^- will discharge to ground.

For complete shutdown to occur and the 10µA current drain to be realized, the following conditions must be met:

- +5.00V must be applied to the SD pin;
- $\overline{\text{ENABLE}}$ must either 0V, +5.0V or not connected;
- the receiver inputs must be either 0V or +5V
- the transmitter inputs must be either +5.0V or not connected; and
- Vcc must be +5V

For proper operation, the SD input pin must not be left floating.

New Feature: Wake-up

The **SP241C** has a wake-up feature that keeps all receivers in an ENABLED state when the device is in the shutdown (power down) mode; *Table 1* defines the truth table for the wake-up function. With only the receivers activated, the device typically draws less than 5µA, (10µA max) supply current. In the case of a modem interfaced to a computer in power down mode, the RI (ring indicator) signal from the modem would be used to "wake-up" the computer allowing it to accept the data transmission.

After the ring indicator signal has propagated through the **SP241C** receiver, it can be used to trigger the power management ciruitry of the computer to power up the the microprocessor and bring the SD pin low, taking it out of shutdown mode. The receiver propagation time for the **SP241C** is typically 1µs. The enable time for V^+ and V^- is typically 2ms. At this point a signal can be sent to the modem on the DTR (data terminal ready) pin signifying that the computer is ready to accept and transmit data.

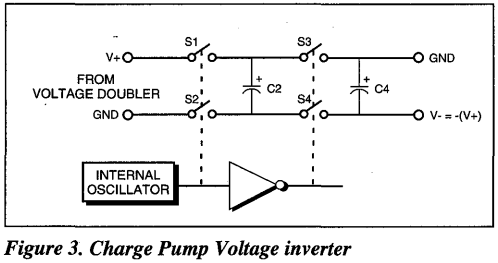


Figure 3. Charge Pump Voltage inverter

SD	$\overline{\text{EN}}$	Power Up/Down	Receiver Outputs
0	0	Up	Enable
0	1	Up	Tri–state
1	0	Down	Enable
1	1	Down	Tri–state

Table 1. Wake–Up Function Truth Table

New Feature: Power Management

The **SP241C** has internal circuitry that constantly monitors driver loading and Icc. Under no load conditions the power management circuitry slows the charge pump oscillator, minimizing the Icc current drain to typically 4mA (10mA maximum). While under full load conditions, the charge pump operates at the full speed oscillator frequency, and I_{CC} increases to around 20mA.

ENABLE Input (EN)

The **SP241C** features an ENABLE input (EN), which allows the receiver outputs to be either tri-stated or enabled. The enable input is active low; 0V applied to EN will enable the receiver outputs. This can be especially useful when the receiver is tied directly to a microprocessor data bus. The EN function remains fully active during shutdown (see *Table 1*).

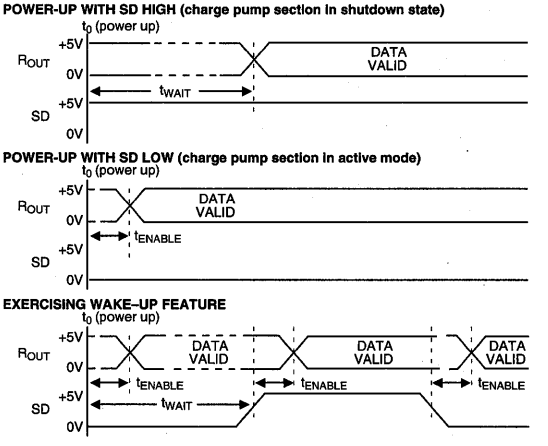
APPLICATION HINTS

Over-Voltage Protection

The driver outputs are protected against shorts to ground, other driver outputs, and V^+ or V^-. If the possibility exists that the outputs could be inadvertently connected to voltages greater than ±15V, then it is recommended that external protection be provided. Back to back Zener diodes or transient voltage surpressors can be used to clamp the driver outputs to safe levels. Receiver inputs are protected to ±30V signal levels, and should not require external voltage clamps, unless transient situations may produce signals greater than ±30V.

Enhanced Drive Capability for Mouse Applications

The **SP241C** has been designed with improved drive capability for non-standard applications. Although the EIA RS232D standards specify the maximum loading to be 3KΩ and 2500pF, the **SP241C** can typically drive loads as low as 750Ω and still maintain ±5V outputs. This feature is especially useful when the serial port is intended to be used for a "self-powered" mouse. In this case the voltage necessary to operate the circuits in the mouse can be derived from the RS232 driver output as long as the loading is ≥ 750Ω. For applications which even exceed this requirement, drivers can be paralleled, increasing the drive capability to 500Ω, again keeping the ±5V V_{OH} and V_{OL} levels (*Figure 1*).



SPECIFICATIONS:
(V_{CC} =+5V±10%, T_A=25°C)

PARAMETER	MIN.	TYP.	MAX.
t_{WAIT}		2ms	3ms
t_{ENABLE}		1ms	2ms

Figure 4. Wake–Up Timing

ORDERING INFORMATION

Model	**Package**
0°C to +70°C:	
SP241CCT	28–pin SOIC
SP241CCA	28–pin (Shrink Small Outline) SSOP
–40°C to +85°C	
SP241CET	28–pin SOIC
SP241CEA	28–pin (Shrink Small Outline) SSOP

CT, CA, ET and EA packages available Tape–on–Reel; please consult the factory

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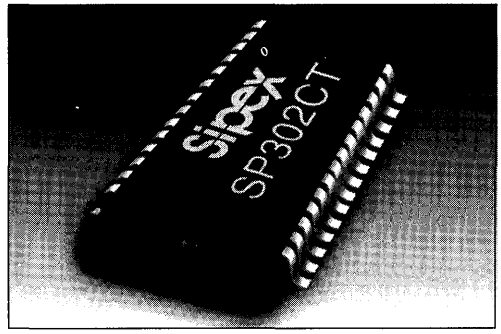
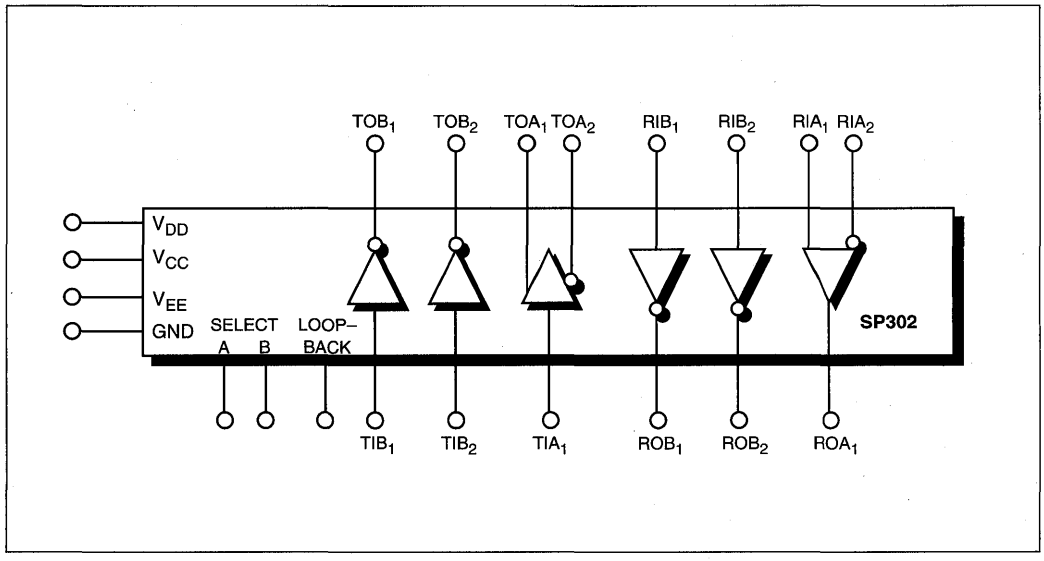
RS232/RS422 Line Drivers/Receivers

- RS232 and RS422 on One Chip
- Multiple Drivers and Receivers
- Software-selectable Modes
- Loopback for Self-Testing
- Short-circuit Protected
- 24-pin Single-width DIP or SOIC Package



DESCRIPTION...

The **SP301** and **SP302** are proprietary single-chip devices that contain both RS232 and RS422 protocol line drivers and receivers. Their configuration may be changed at any time by logic levels on two control lines. In any configuration, both the **SP301** and **SP302** fully meet the requirements of the EIA RS232D and RS422 data communication standards. A loopback test mode is provided.The **SP301** and **SP302** are available in 24-pin single width plastic, and 28-pin SOIC packages for commercial and industrial temperature range operation.



SPECIFICATIONS

($T_{MIN} \leq T_A \leq T_{MAX}$ and nominal supply voltages unless otherwise noted)

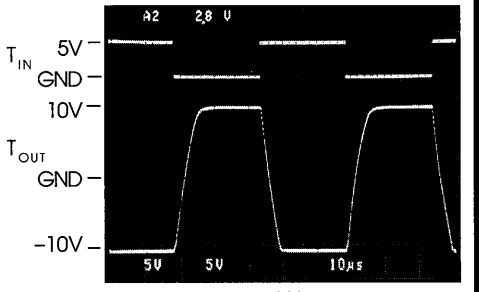
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS232 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	+5.0			V	R_L = 3kΩ, V_{IN} = 0.8V
Low Level Output			-5.0	V	R_L = 3kΩ, V_{IN} = 2.0V
Short Circuit Current			±30	mA	V_{OUT} = 0V
Loopback Output Voltage		-1.5		V	R_L = 3kΩ, V_{EE} = -12.0V; Note 1
Slew rate			30	V/µs	C_L = 50pF, R_L = 3kΩ; T_A = 25°C
Transition Time		3		µs	V_{OUT} from +3V to -3V or -3V to +3V
Transmission Rate			200	kbps	
RS232 RECEIVER					
Input Voltage Range	-15		+15	V	Note 6
Input High Threshold	+1.75		+2.5	V	Positive-going
Input Low Threshold	+0.75		+1.35	V	Negative-going
Input Impedance	3		7	kΩ	$V_{SS} \leq V_{IN} \leq V_{DD}$
TTL Output Level					
V_{OL}			0.4	V	V_{CC} = +4.75V, I_{OUT} = +1.6mA
V_{OH}	2.4			V	V_{CC} = +4.75V, I_{OUT} = -0.5mA
Receiving Rate			200	kbps	
RS422 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	2.75		6.0	V	I_{OH} = -20mA
Low Level Output			1.0	V	I_{OL} = +20mA
Differential Output	±2			V	R_L = 100Ω
			±6	V	R_L = ∞
Short Circuit Current			±100	mA	Note 2
Output Current			±500	µA	-0.25V < V_o < 6V; power off
Transition Time			400	ns	R_L = 100Ω, C_L = 15pF; Note 3
Transmission Rate			1,000	Kbps	
RS422 RECEIVER					
Common Mode Range			±7	V	Note 4
Differential Input			±15	V	Note 4 and 6
Differential Input Threshold	-0.2		+0.2	V	T_A = 25°C
Input Voltage Hysteresis	30			mV	V_{CM} = 0V; T_A = 25°C
Input Resistance	3			kΩ	-7V < V_{CM} < +7V
TTL Output Level					
V_{OL}			0.4	V	V_{CC} = +4.75V, I_{OUT} = +1.6mA
V_{OH}	2.4			V	V_{CC} = +4.75V, I_{OUT} = -0.5mA
Receiving Rate			1,000	Kbps	
Short Circuit Output Current			±120	mA	V_{OUT} = 0V
POWER REQUIREMENTS					
V_{DD} = +12V, ±10%		7	15	mA	Note 5
V_{CC} = +5V; ±10%		5	7	mA	Note 5
V_{EE} = -12V, ±10%		11	20	mA	Note 5
ENVIRONMENTAL					
Operating Temperature					
-CS, –CT	0		+70	°C	
-MR	-55		+125	°C	
Storage Temperature	-65		+150	°C	

Notes:

1. In Loop-back mode
2. Only one output drive pin per package will be shorted at any time
3. From 10% to 90% of steady-state
4. This is an absolute maximum rating; normal operating levels are $V_{in} < 5V$
5. Outputs unloaded; Inputs tied to GND; $T_A = +25°C$; $V_{IL} = 0V$; LB=0
   Typical SP302 current drains under full load are:
   18mA (+12V), 10mA (-12V) and 7mA (+5V) in RS232 mode only;
   5mA (+12V), 7mA (-12V) and 56mA (+5V) in RS422 mode only;
   12mA (+12V), 14mA (-12V) and 31mA (+5V) in RS232 and RS422 modes;
   RS232 loads 3KΩ, 2500pF, 20kHz; RS422 outputs across 100Ω, 500kHz.
6. In Loopback mode, the external voltage input to the receiver must not exceed ±10V, otherwise the loopback test may be adversely affected.

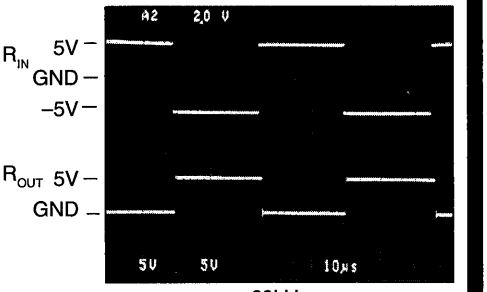
TYPICAL PERFORMANCE CURVES

RS232 Driver



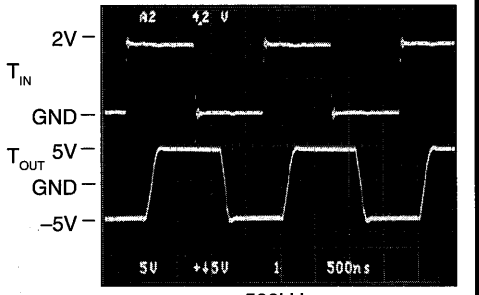
20kHz

RS232 Receiver



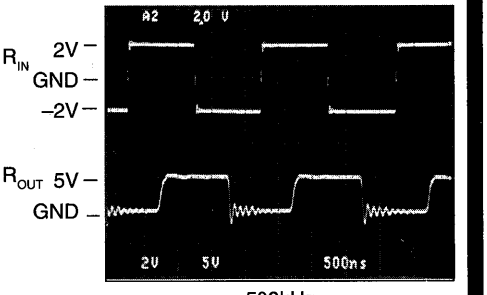
20kHz

RS422 Driver



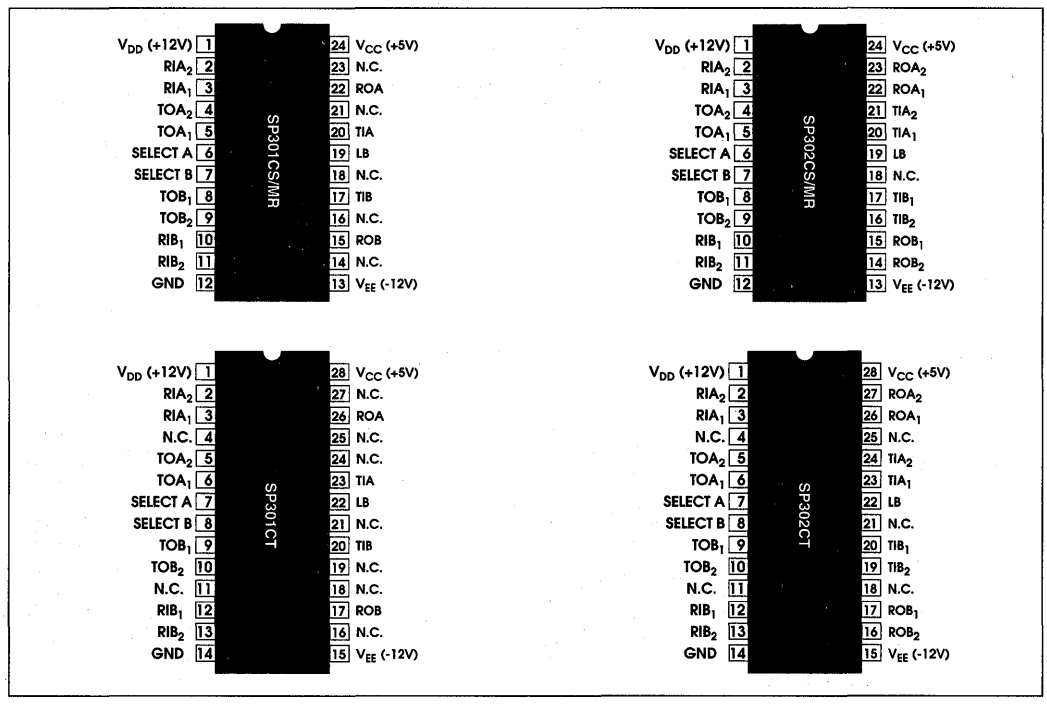
500kHz

RS422 Receiver



500kHz

PIN ASSIGNMENTS



FEATURES...

The **SP301** and **SP302** are proprietary single-chip devices that contain both RS232 and RS422 protocol line drivers and receivers. They differ only in the total number of line drivers and receivers of each protocol that may be active at any given time. Their configuration may be changed at any time by logic levels on two control lines. In any configuration, both the **SP301** and **SP302** fully meet the requirements of the EIA RS232D and RS422 data communication standards.

The RS232 line driver circuits convert TTL logic level inputs into inverted RS232 output signals. The RS422 line drivers convert TTL logic levels into RS422 differential output signals. The RS422 line driver outputs feature high source and sink current capability. All line drivers are internally protected against short circuits on their outputs.

The RS232 receivers convert the EIA RS232 input signals to inverted TTL output logic levels. The RS422 receivers convert the EIA RS422 differential input signals into non-inverted TTL output logic levels. Receiver input filtering provides excellent high frequency noise immunity. Input pulses with widths less than 1µs are completely ignored. The RS232 receivers have the additional feature of voltage hysteresis, which helps eliminate spurious output transitions that might result from low amplitude noise voltages during slower-speed signal transitions.

A loopback test mode is provided that puts the driver outputs to a high impedance tri-state level, and routes the driver outputs to their associated receiver inputs. In this configuration, the signal path is non-inverting from the TTL driver input to the receiver TTL output. This operating mode allows the controlling system to perform diagnostic self-test of the RS232/RS422 driver/receiver circuitry at speeds up to 3,000 bits per second.

The **SP301** and **SP302** are available in 24-pin single–width (0.300") plastic DIP and 28-pin

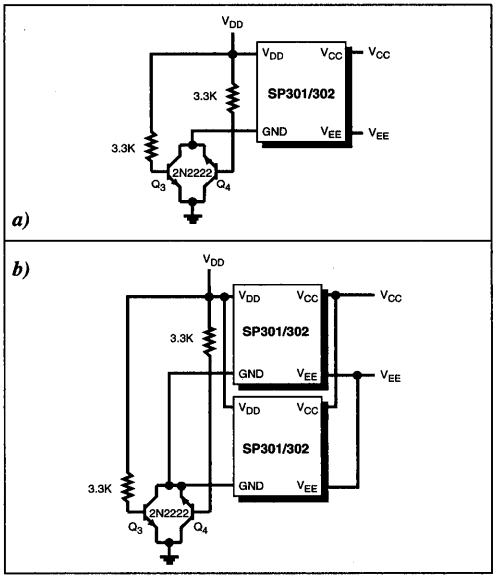


Figure 1. Isolating SP301/302 From Ground; a) Single SP301/302; b) Multiple SP301/302

SOIC packages for operation over the commercial temperature range.

USING THE SP301/302 POWER SUPPLIES

The **SP301/SP302** require ±12V and +5V for full RS232 and RS422 operation. The ±12V supplies set up the RS232 ±9V voltage swings, and the +5V is used for the interal logic that formats the communications mode and controls the loopback function. The supply voltages can be decreased to as low as ±7V for V_{DD} and V_{EE}, and 4.0V for V_{CC}. Under these supply conditions, derated performance can be expected.

POWER SUPPLY SEQUENCING

There are two requirements for power supply sequencing for the **SP301/302**. The first is that V_{DD} is always greater than V_{CC}. The second is that when the part is powered up, V_{DD} must be applied 20ms before V_{CC}.

GENERAL USAGE

RS232 Operation

The **SP301** and **SP302** are fully compliant RS232 devices. Their outputs are fully protected against shorts to ±20V with no external circuitry. If the potential exists for momentary shorts to voltages greater than ±20V, it is recommended that a 220Ω resistor be wired in series with each driver output. This will limit any damage from the higher short-circuit current from these higher voltage potentials. Voltage clamps such as back-to- back Zener diodes can be used to clamp the driver outputs to "safe" levels. Short circuit current to ground is internally limited, and can therefore be sustained infinitely. Under normal operating conditions, the drivers can typically source 7mA at ±5V output, which exceeds the minimum RS232 standards requirement.

If an **SP301/302** transmitter output occupies a data transmission line with other RS232 devices which are not powered by the same power supplies, it is possible that a device that is not powered will have a low impedance path to ground at its driver output. The RS232 standards require that with no power applied to the device, the impedance from a transmitter output to ground must be greater than 300Ω. This can be easily achieved as shown in *Figure 1a*, where an external transistor is used as a switch to isolate an **SP301/302** from ground in the power

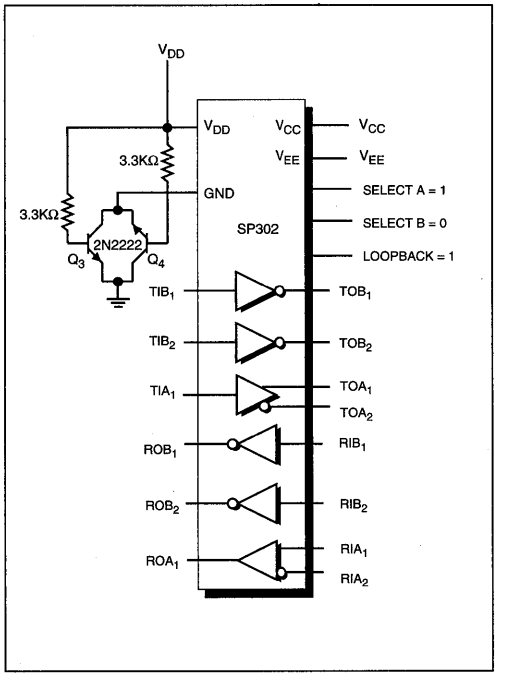


Figure 2. Typical Circuit

off condition. With V_{DD} turned on, the transistor switch is on, connecting ground (GND) for the device to the circuit ground. In a power off condition, this transistor is switched off, thus isolating the unit from circuit ground, and thereby leaving the driver in a high impedance state. Multiple **SP301/302s** can be connected as shown in *Figure 1b*.

RS422 OPERATION

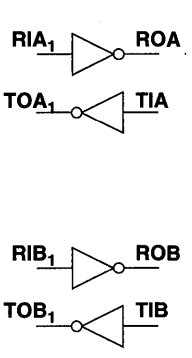
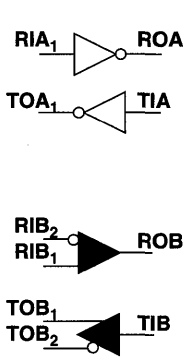
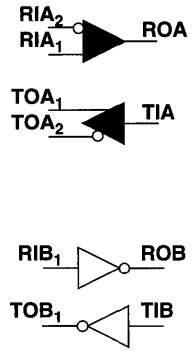
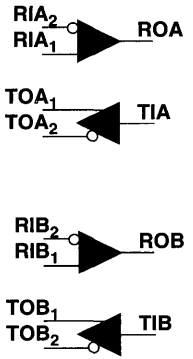
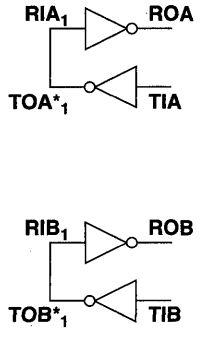
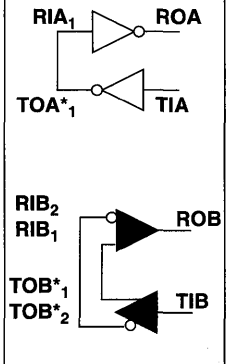
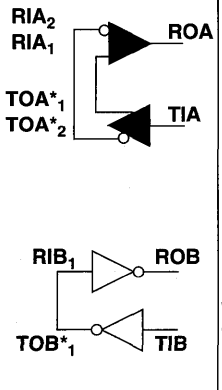
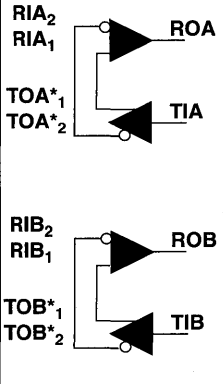
The **SP301** and **SP302** are fully compliant RS422 devices when operating in the RS422 mode. Baud rate and drive capability have been balanced to provide as much versatility as possible. The **SP301** and **SP302** are both guaranteed for a 1Mbps data rate, supplying ±2V minimum into a 100Ω load. Short circuit protection for the RS422 operating mode is the same as in the RS232 mode. The driver outputs can be shorted to ground for an infinite duration, with a maximum current of ±100mA.

The RS422 receivers accept differential signals at a 1Mbps rate, and translate them to a non-inverted TTL output. The receivers are specified with a ±15V differential input voltage, which means that to operate normally, the difference betweeen the voltages at the inputs cannot exceed ±15V. The common mode voltage is specified as ±7V. This identifies the midpoint of the range about which the differential input must lie so that the receiver can detect a change of state. Within this ±7V range, the receivers will recognize a change in state with a ±200mV differential threshold voltage. Since the RS232 and RS422 inputs are shared, all receiver inputs are protected to ±30V to guard against inadvertently applying an RS232 signal to an input that is configured for RS422.
Figure 2 shows a typical circuit for the **SP301/302**. In this case the **SP302** is shown configured for one (1) duplex RS422 and two (2) duplex RS232 communication paths.

CONFIGURING THE SP301/302

The Figures on pages 7 and 8 show the various combinations of simultaneous RS232 and RS422 operation that can be achieved with the **SP301**. Similarly, the figures on pages 9 and 10 show the various combinations for the **SP302**. Each of these configurations are software selectable by logic level on the SELECT A and SELECT B control lines. Configuration can be changed "on-the-fly".

SP301 CONTROL LOGIC CONFIGURATION

SELECTION	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE
SELECT A: SELECT B:	0 0	0 1	1 0	1 1
NON–LOOPBACK (LB = 1)				
LOOPBACK (LB=0)				

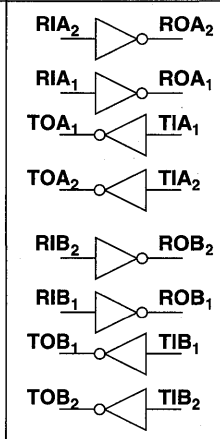
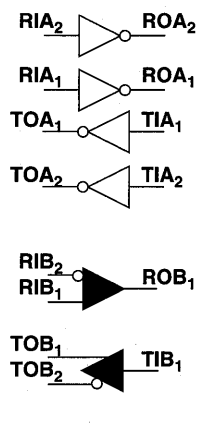
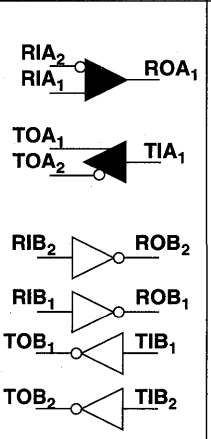
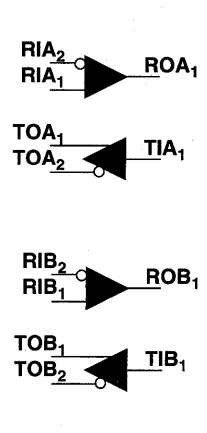
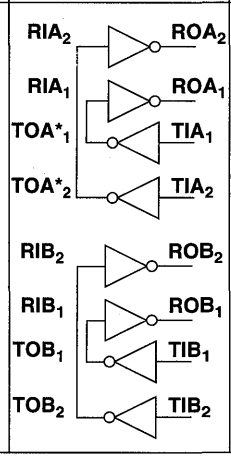
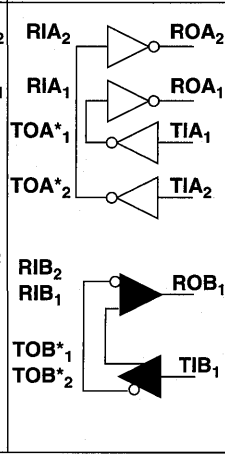
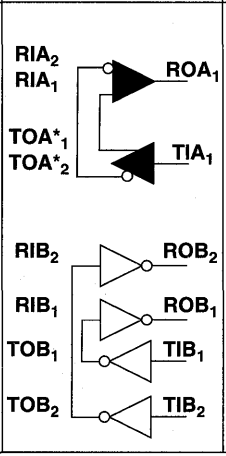
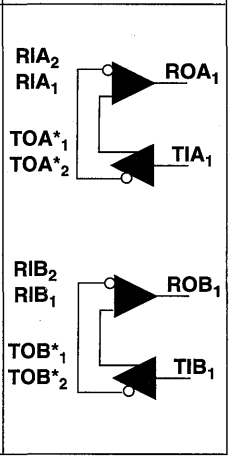
RS232 DRIVER
* Tri–state Output

RS232 RECEIVER

RS422 RECEIVER

RS422 DRIVER

SP302 CONTROL LOGIC CONFIGURATION

SELECTION	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE
SELECT A: SELECT B:	0 0	0 1	1 0	1 1
NON–LOOPBACK (LB = 1)				
LOOPBACK (LB=0)				

RS232 DRIVER
* Tri–state Output

RS232 RECEIVER

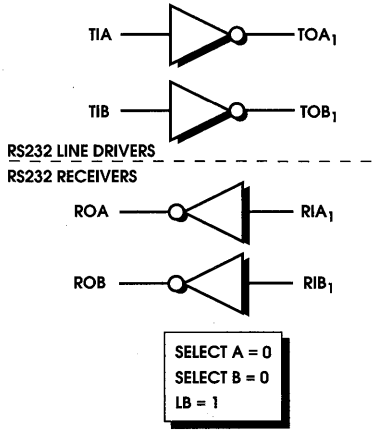
RS422 RECEIVER

RS422 DRIVER

SP301 CONFIGURATIONS

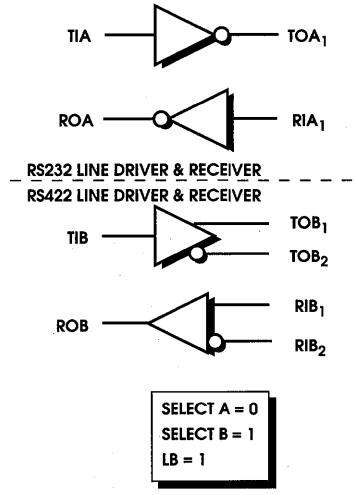
Two-Channel Full Duplex RS232

Two independent channels of RS232 line driver and two channels of RS232 receiver.



One-Channel Full Duplex RS232 & One-Channel Full Duplex RS422

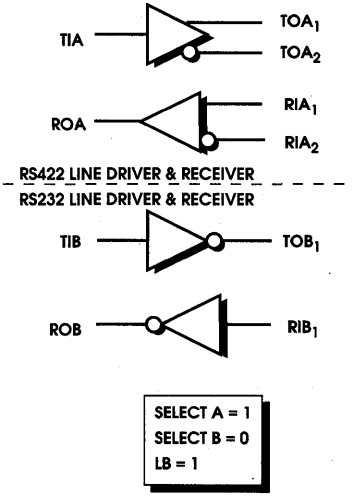
A single RS232 line driver and receiver, and a single RS422 line driver and receiver.



SP301 CONFIGURATIONS

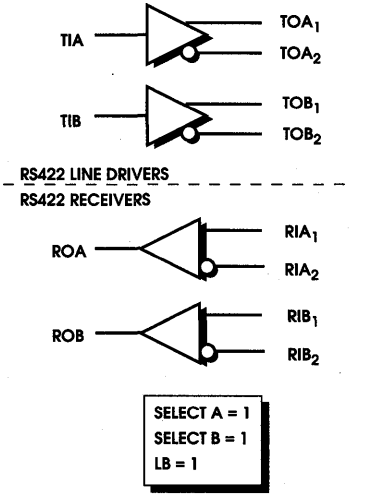
One-Channel Full Duplex RS232 & One-Channel Full Duplex RS422 Opposite Drivers

A single RS232 line driver and receiver, and a single RS422 line driver and receiver. At first glance, this is the same configuration as that in the figure immediately to the left. Note however that functions are activated on the opposite channels as that of those in *Figure 1b*.



Two-Channel Full Duplex RS422

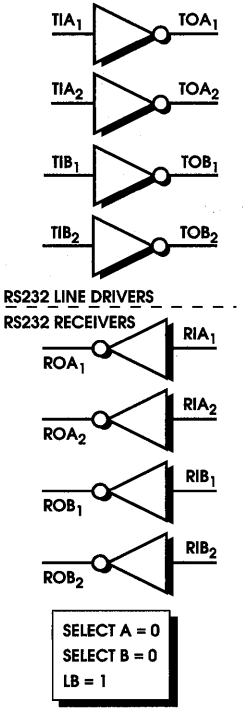
Two RS422 line drivers and two RS422 receivers.



SP302 CONFIGURATIONS

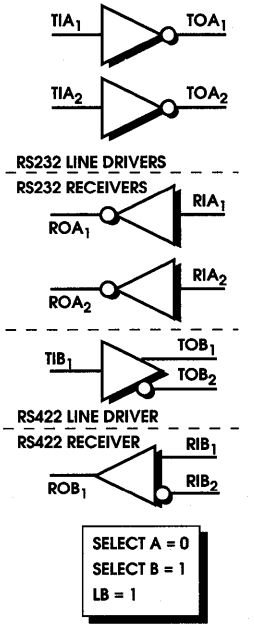
Four-Channel Duplex RS232

Four independent channels of RS232 line driver and four channels of RS232 receiver.



Two-Channel Duplex RS232 & One-Channel Duplex RS422

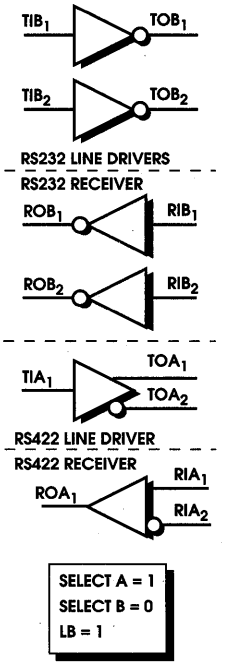
Two RS232 line drivers and receivers, and a single RS422 line driver and receiver.



SP302 CONFIGURATIONS

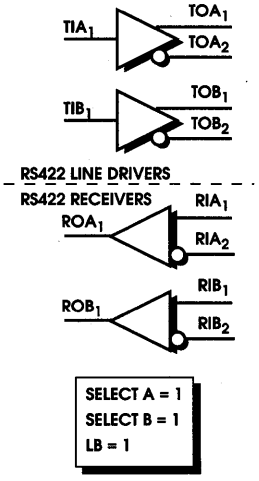
Two-Channel Duplex RS232 & One-Channel Duplex RS422 Opposite Drivers

Two RS232 line drivers and receivers, and a single RS422 line driver and receiver. At first glance, this is the same configuration as that immediately to the left. Note however that functions are activated on the opposite channels.



Two-Channel Duplex RS422

Two RS422 line drivers and two RS422 receivers.

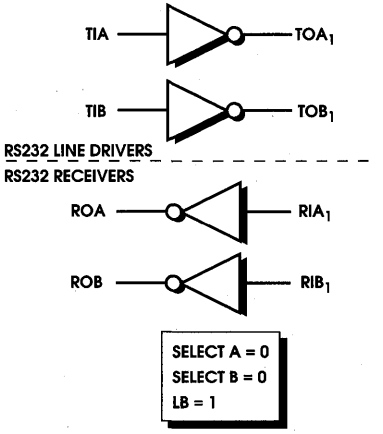


LOOPBACK

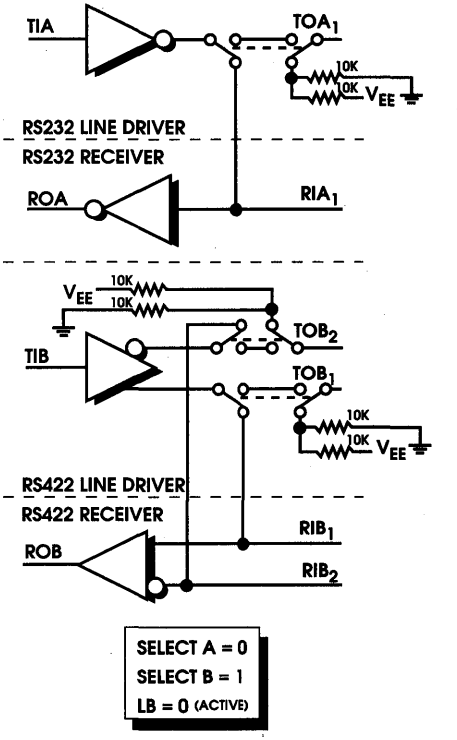
Both the **SP301** and **SP302** have a function called loopback, which is essentially a chip self-test. However, by connecting system test loops with the inputs and outputs of the **SP301/302**, a system-level diagnostic can be run on power-up or on command. The test loops can be enabled and disabled allowing both system test and operation with the same components. A maximum data rate for loopback of 3Kbps is recommended. Loopback is a pin-programmable function, activated by a logic low on the **LB** pin (19). As

SP301 CONFIGURATIONS IN LOOPBACK MODE

Two -Channel Full Duplex RS232



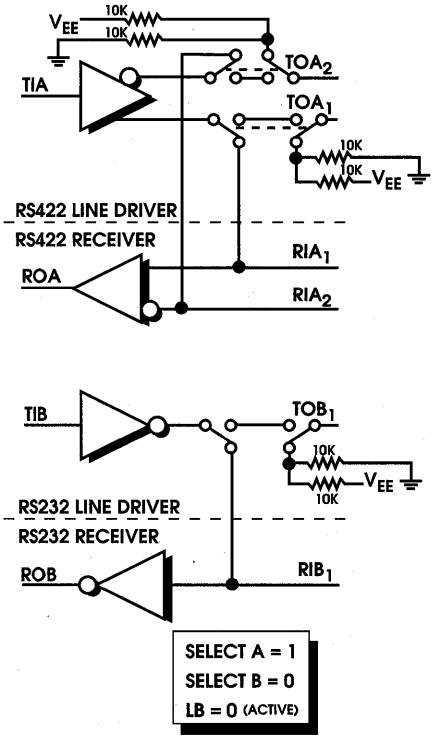
One-Channel Full Duplex RS232 & One-Channel Full Duplex RS422



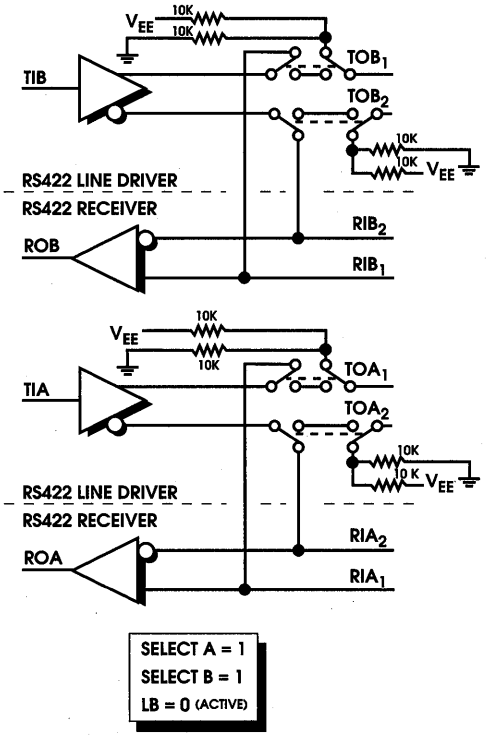
shown in these figures, the loopback function internally connects the driver outputs to the corresponding receiver inputs, and switches the output pin to a resistive divider of 10KΩ nominal impedance from V_{EE} to ground. Receiver outputs are left active for signal verification. During loopback, the receiver inputs are tied to ground via a 5kΩ pulldown resistor. To minimize loopback errors, the receiver inputs must be limited to ±10V swings.

SP301 CONFIGURATIONS IN LOOPBACK MODE

One-Channel Full Duplex RS232 & One-Channel Full Duplex RS422 Opposite Drivers

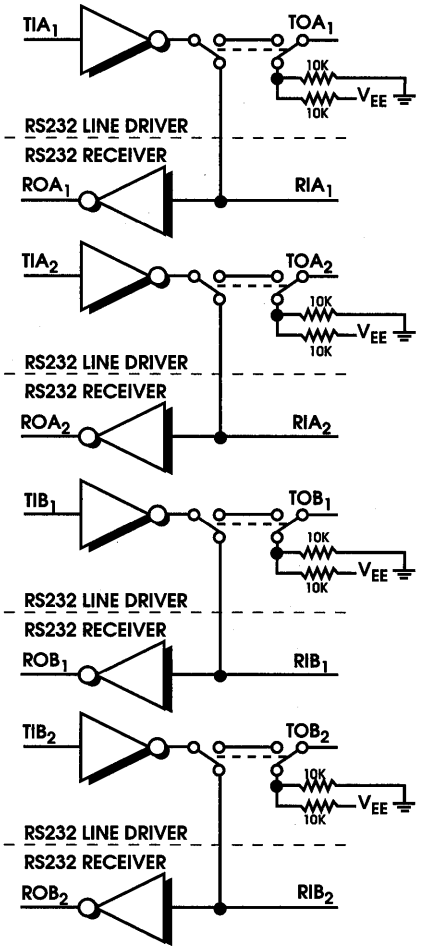


Two-Channel Full Duplex RS422



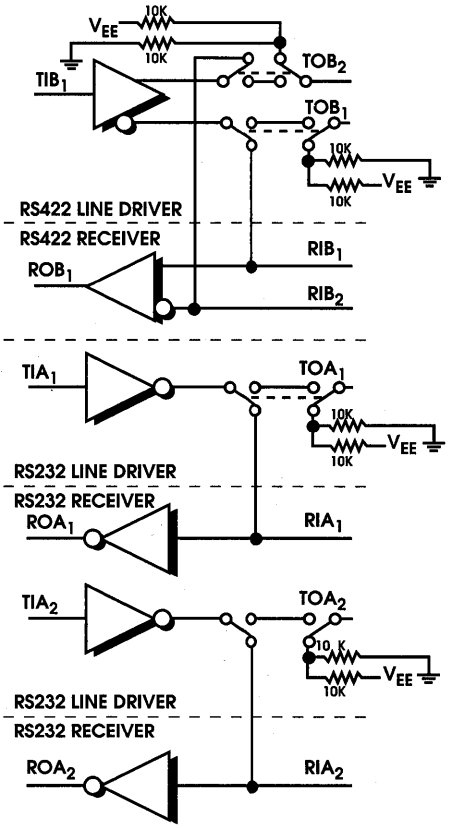
SP302 CONFIGURATIONS IN LOOPBACK MODE

Four-Channel Duplex RS232



SELECT A = 0
SELECT B = 0
LB = 0 (ACTIVE)

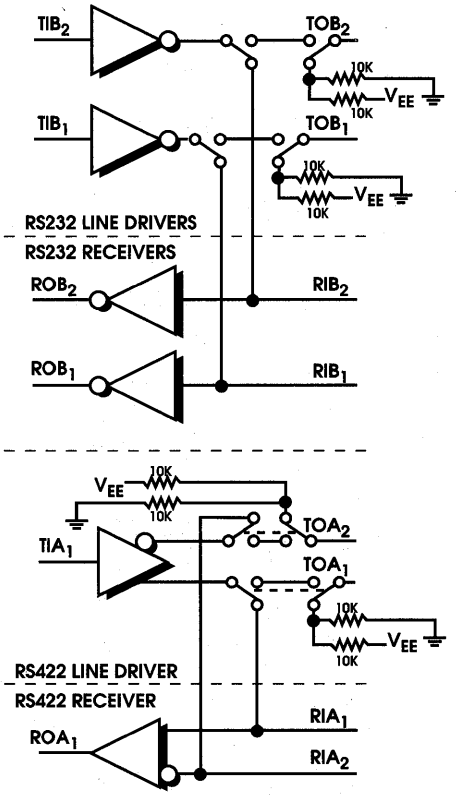
Two-Channel Duplex RS232 & One-Channel Duplex RS422



SELECT A = 0
SELECT B = 1
LB = 0 (ACTIVE)

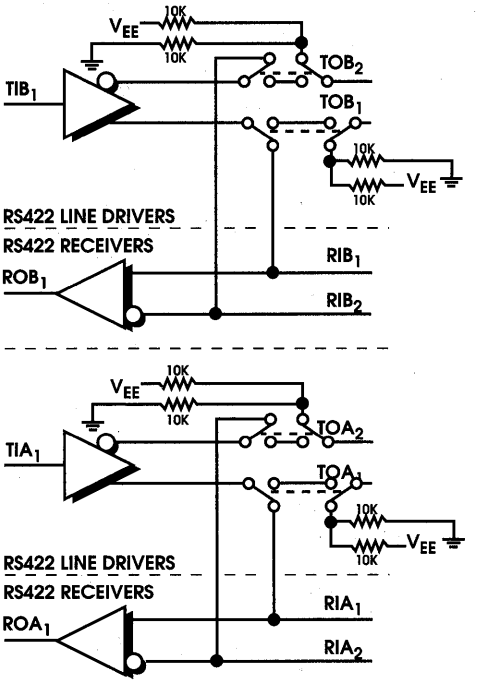
SP302 CONFIGURATIONS IN LOOPBACK MODE

Two-Channel Duplex RS232 & One-Channel Duplex RS422 Opposite Drivers



SELECT A = 1
SELECT B = 0
LB = 0 (ACTIVE)

Two-Channel Duplex RS422



SELECT A = 1
SELECT B = 1
LB = 0 (ACTIVE)

ORDERING INFORMATION

Model	Max # of Duplex Channels RS232	RS422	Temperature	Package
SP301CS	2	2	0°C to +70°C	24-pin single-width plastic DIP
SP301CT	2	2	0°C to +70°C	28-pin SOIC
SP301ES	2	2	-40°C to +85°C	24-pin single-width plastic DIP
SP301ET	2	2	-40°C to +85°C	28-pin SOIC
SP302CS	4	2	0°C to +70°C	24-pin single-width plastic DIP
SP302CT	4	2	0°C to +70°C	28-pin SOIC
SP302ES	4	2	-40°C to +85°C	24-pin single-width plastic DIP
SP302ET	4	2	-40°C to +85°C	28-pin SOIC

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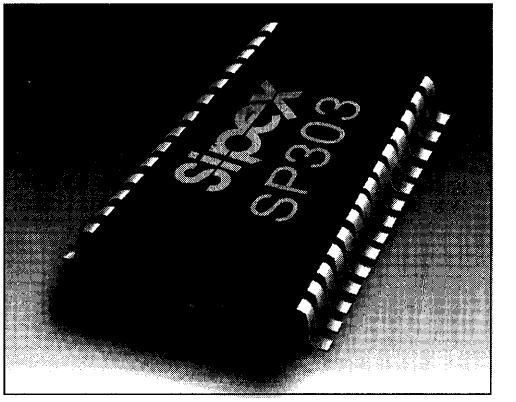
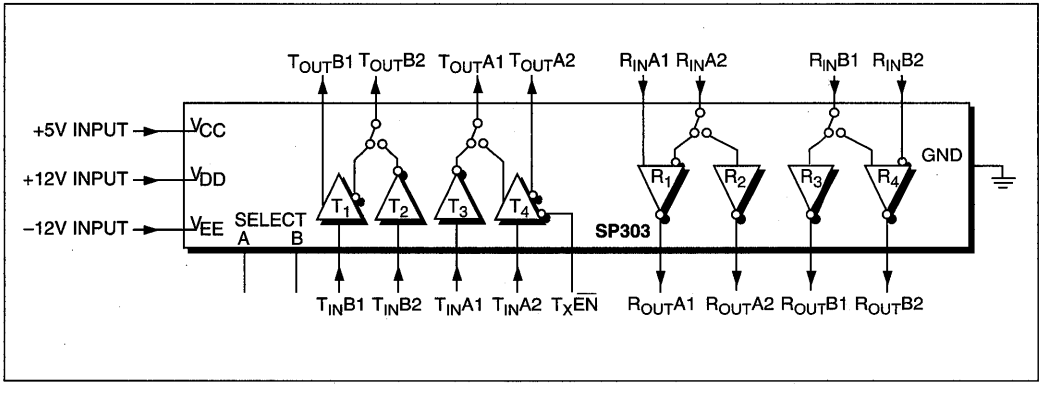
RS232/AppleTalk™ Serial Transceiver

- Single chip serial transceiver supports AppleTalk™ or RS232 interface
- Programmable Selection of Interface
- 4 RS232 Drivers and 4 RS232 Receivers
- Provides Macintosh™ type interface
- ±30V Receiver Input Levels
- Surface Mount Packaging



DESCRIPTION...

The **SP303** is a single chip device that offers both RS232 and Apple–Talk interfaces. When configured for RS232 mode the **SP303** has 4 drivers and 4 receivers. When the part is programmed for Apple–Talk mode, the **SP303** supports Macintosh–type ports. All drivers and receivers can operate at data rates up to 1 Mbps. The differential driver used for transmitting data signals is equipped with a tri-state function. The **SP303** is available in a 28–pin SOIC package for operation over the commercial temperature range.



SPECIFICATIONS

($T_{MIN} \leq T_A \leq T_{MAX}$ and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RS232 DRIVER					Note 1
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	+5.0			V	R_L = 3KΩ, V_{IN} = 0.8V
Low Level Output			-5.0	V	R_L = 3KΩ, V_{IN} = 2.0V
Short Circuit Current			±30	mA	V_{OUT} = 0V
Slew Rate			30	V/µs	C_L = 50pF, R_L = 3kΩ; T_A = 25°C
Transition Time		3		µs	Note 2
Transmission Rate			200	Kbps	
RS232 RECEIVER					Note 1
Input Voltage Range	–15		+15	V	
Input High Threshold	+1.75		+2.5	V	Positive-going
Input Low Threshold	+0.75		+1.35	V	Negative-going
Input Impedance	3		7	KΩ	C_L <2,500pF; $V_{SS} \leq V_{IN} \leq V_{DD}$
TTL Output Level					
V_{OL}			0.4	V	V_{CC} =+4.75V, I_{OUT} =+1.6mA
V_{OH}	2.4			V	V_{CC} =+4.75V, I_{OUT} =-0.5mA
Receiving Rate			200	Kbps	
DIFFERENTIAL DRIVER					Note 3
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	+3.6	+6		V	I_{OH} = 8mA
Low Level Output	-3.6	-6		V	I_{OL} = –8mA
Differential Output	±3.6			V	R_L = 450Ω
	(V_{EE}+0.7V)		(V_{DD}–0.7V)	V	RL = ∞
Short Circuit Current			40	mA	
Output Current			±500	µA	–0.25V < V_O < 6V; Power off
Leakage Current		0.05	±10	µA	TxEN=V_{cc}, 0≤TxDO≤6V, Note 4
Transition Time		720		ns	R_L=450Ω, C_L=50pF; Note 5
Transmission Rate			1000	Kbps	
DIFFERENTIAL RECEIVER					Note 3
Common Mode Range			±7	V	Note 6
Differential Input			±15	V	Note 6
Differential Input Threshold	–0.2		+0.2	V	T_A=25°C
Input Voltage Hysteresis	30			mV	V_{CM}=0V;T_A=25°C
Input Resistance	3			KΩ	–7V<V_{CM}<+7V
TTL Output Level					
V_{OL}			0.4	V	V_{CC}=+4.75V, I_{OUT}=+1.6mA
V_{OH}	2.4			V	V_{CC}=+4.75V, I_{OUT}=–0.5mA
Receiving Rate			1000	Kbps	
Short Circuit Output Current			±120	mA	V_{OUT}=0V
SINGLE–ENDED RECEIVER					Note 3
Input Threshold	–200		+200	mV	T_A=25°C
Input Voltage Hysteresis	30			mV	V_{CM}=0V; T_A=25°C
Input Impedance	3		7	KΩ	
TTL Output Level					
V_{OL}			0.4	V	$V_{CC=}$+4.75; I_{OUT}=+1.6mA
V_{OH}	2.4			V	V_{CC}=+4.75; $I_{OUT=}$–0.5mA
Transmission Rate			1000	Kbps	
POWER REQUIREMENTS					
V_{DD} = +12V, ±10%		7	15	mA	All Transmitter outputs R_L=∞
V_{CC} = +5V, ±10%		5	7	mA	T_A=25°C
V_{EE} = –12V, ±10%		11	20	mA	

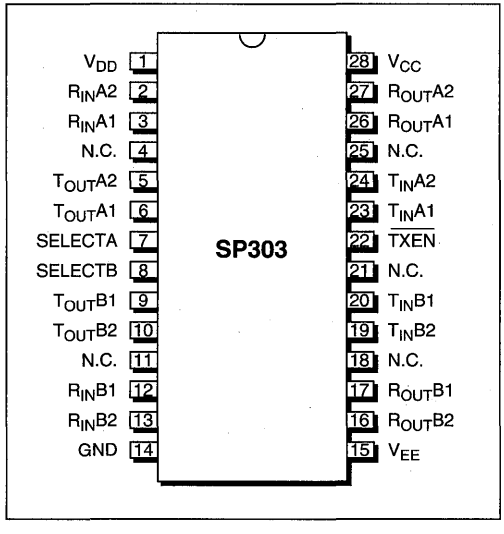
SPECIFICATIONS

($T_{MIN} \leq T_A \leq T_{MAX}$ and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature	0		+70	°C	
Storage Temperature	–65		+150	°C	
Package		28–pin SOIC			

Note:
1. RS232 Mode, SELA = SELB = GND.
2. V_{OUT} from +3V to –3V or –3V to +3V.
3. Macintosh™ AppleTalk™ Mode, SELA = SELB = +5V.
4. Leakage current specification applies to both TxDO– and TxDO+; T_A=+25°C only.
5. From 10% to 90% of steady state.
6. This is an absolute maximum rating. Normal operating levels are $V_{IN} \leq 5V$.

PINOUT



PIN ASSIGNMENTS – RS232 MODE

Pin 1 — V_{DD} — +12V Power Supply.

Pin 2 — $R_{IN}A2$ — DSR; RS232 input.

Pin 3 — $R_{IN}A1$ — RXD; RS232 input.

Pin 4 — N.C. — No Connection.

Pin 5 — $T_{OUT}A2$ — RTS; RS232 output.

Pin 6 — $T_{OUT}A1$ — TXD; RS232 output.

Pin 7 — SEL A — Select A; used with Select B (pin 8) to select operating mode. Logic "0" on both SEL A and SEL B selects RS232 mode; logic "1" on both SEL A and SEL B selects AppleTalk™ mode.

Pin 8 — SEL B — Select B; used with Select A (pin 7) to select operating mode. Logic "0" on both SEL A and SEL B selects RS232 mode; logic "1" on both SEL A and SEL B selects AppleTalk™ mode.

Pin 9— $T_{OUT}B1$— DTR; RS232 output.

Pin 10 — $T_{OUT}B2$ — RI; RS232 output.

Pin 11 — N.C. — No Connection.

Pin 12— $R_{IN}B1$— CTS; RS232 input.

Pin 13 — N.C. — No Connection.

Pin 14 — GND — Signal ground. Connected to logic and chasis ground.

Pin 15 — V_{EE} — –12V Power Supply.

Pin 16 — N.C. — No Connection.

Pin 17 — $R_{OUT}B1$ — CTS; TTL Output to UART.

Pin 18 — N.C. — No Connection.

Pin 19 — $T_{OUT}B2$ — RI; TTL input from UART.

Pin 20 — $T_{IN}B1$ — DTR; TTL input from UART.

Pin 21 — N.C. — No Connection.

Pin 22 — TxEN — Transmit Enable; Only functional in Mac Mode.

Pin 23 — $T_{IN}A1$ — TXD; TTL input from UART.

Pin 24 — N.C. — No Connection.

Pin 25 — N.C. — No Connection.

Pin 26 — $R_{OUT}A1$ — RXD; TTL output to UART.

Pin 27 — N.C. — No Connection.

Pin 28 — V_{CC} — +5V Power Supply.

PIN ASSIGNMENTS — MACINTOSH™ APPLETALK™ MODE

Pin 1 — V_{DD} — +12V Power Supply.

Pin 2 — $R_{IN}A2$ — Receive data; received at UART's RxD (non–inverted); V_{IH} = 0.2V; V_{IL} = –0.2V; R_{IN} =3KW minimum.

Pin 3 — $R_{IN}A1$ — Receive data; received at UART's RxD (inverted); V_{IH} = 0.2V; V_{IL} = –0.2V; R_{IN} =3KΩ minimum.

Pin 4 — N.C. — No Connection.

Pin 5 — $T_{OUT}A2$ — Transmit data; driven from UART's TxD (non–inverted); tri–stated when UART's RTS is not asserted; V_{OH} = 3.6V min; V_{OL} = –3.6V min; R_L = 450Ω.

Pin 6 — $T_{OUT}A1$ — Transmit data; driven from UART's TxD (inverted); tri–stated when RTS is not asserted; V_{OH} = 3.6V min; V_{OL} = –3.6V min; R_L = 450Ω

Pin 7 — SEL A — Select A; used with Select B (pin 8) to select operating mode. Logic "0" on both SEL A and SEL B selects RS232 mode; logic "1" on both SEL A and SEL B selects AppleTalk™ mode.

Pin 8 — SEL B — Select B; used with Select A (pin 7) to select operating mode. Logic "0" on both SEL A and SEL B selects RS232 mode; logic "1" on both SEL A and SEL B selects AppleTalk™ mode.

Pin 9— $T_{OUT}B1$— Handshake output; driven from UART's DTR (inverted) ; V_{OH} = 3.6V min; V_{OL} = –3.6V min; R_L = 450Ω

Pin 10 — $T_{OUT}B2$ — Handshake output; driven from UART's DTR (non–inverted); V_{OH} = 3.6V min; V_{OL} = –3.6V min; R_L = 450Ω

Pin 11 — N.C. — No Connection.

Pin 12— $R_{IN}B1$— Handshake input or extemal clock; received non–inverted at UART's CTS and TRxC; V_{IH} = 0.2V; V_{IL} = –0.2V; R_{IN} =3KΩ minimum.

Pin 13 — N.C. — No Connection.

Pin 14 — GND — Signal ground. Connected to logic and chasis ground.

Pin 15 — V_{EE} — –12V Power Supply.

Pin 16 — N.C. — No Connection.

Pin 17 — $R_{OUT}B1$ — Receive handshake output; connects to UART's CTS and TRxC.

Pin 18 — N.C. — No Connection.

Pin 19 — $T_{OUT}B2$ — Not used in AppleTalk™ mode.

Pin 20 — $T_{IN}B1$ — Transmit handshake input; connects to UART's DTR output.

Pin 21 — N.C. — No Connection.

Pin 22 — $T\overline{xEN}$ — Transmit data driver enable; connects to UART's RTS; transmit data driver is enabled when this pin is low.

Pin 23 — $T_{IN}A1$ — Transmit data input; connects to UART's TxD output.

Pin 24 — N.C. — No Connection.

Pin 25 — N.C. — No Connection.

Pin 26 — $R_{OUT}A1$ — Receive data output: connects to UART's RxD input.

Pin 27 — N.C. — No Connection.

Pin 28 — V_{CC} — +5V Power Supply.

FEATURES...

The **SP303** is a single chip device that offers both RS232 and Apple–Talk interfaces. When configured for RS232 mode the **SP303** provides 4 drivers and 4 receivers. When the part is programmed for Apple–Talk mode, the SP303 supports Macintosh–type ports. The mode can be changed at any time by bringing both the SEL A and the SEL B pins high for Mac mode, or low for RS232 mode.

The RS232 line driver circuits convert TTL–logic level inputs into inverted RS232 output signals. The RS232 receivers convert the EIA RS232 input signals to inverted TTL output logic levels. The receivers have voltage hysteresis, which helps eliminate spurious output transitions that might result from low–amplitude noise voltages during slower-speed signal transitions.

When the **SP303** is programmed for Mac mode, the transmit data and receive data signals are

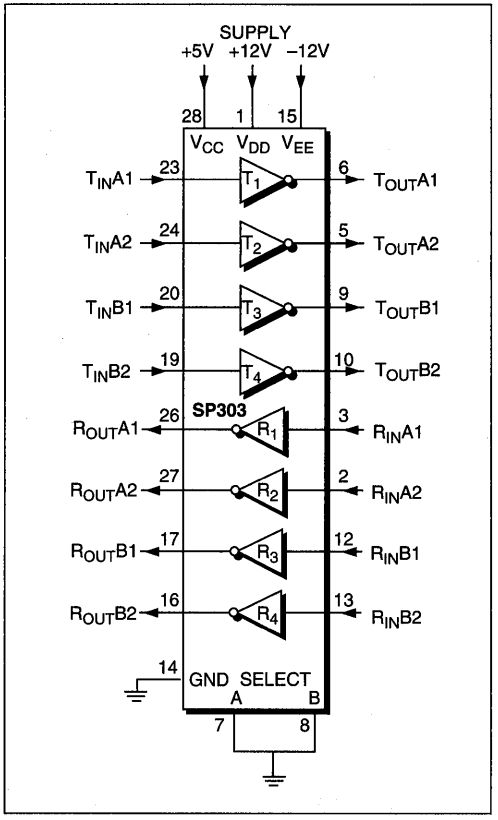


Figure 1. RS232 Operating Mode

differential, while the handshake out and handshake in signals are single–ended. The **SP303** does not have the extra GPI (general purpose input). All drivers and receivers can operate at data rates up to 1 Mbps. The differential driver used for transmitting data signals is equipped with a tri-state function. When the TxEN pin is brought low the differential driver is enabled; when it is high, the driver outputs are tri–stated. The tri–state function does not affect any other driver in either mode of operation.

One **SP303** can significantly reduce the board space necessary for a similar discrete solution offering both RS232 and Apple–Talk interfaces. Due to the space savings, the **SP303** can provide multi-mode interfacing to equipment such as printers or modems without sacrificing additional board space, or cost. This allows the OEM to offer more flexible interface capabilities without additional material costs.

The **SP303** is available in a 28–pin SOIC package for operation over the commercial temperature range.

APPLICATION EXAMPLE
RS232 MODE SERIAL INTERFACE

Figure 3 shows the **SP303CT** used in a dual serial port application which allows both RS232 and Macintosh™ AppleTalk™ Mode interfaces. With SEL A and SEL B low, the port can be configured for RS232. In this mode, the SP303CT is set up for 4 drivers and 4 receivers. The transmitter enable pin (pin22) has no effect in this mode.

The RFI filters shown are optional depending upon the FCC requirements of the system. The **SP303CT** has internal slew rate limiting, which keeps the RS232 slew rate <30V/µS. Since the

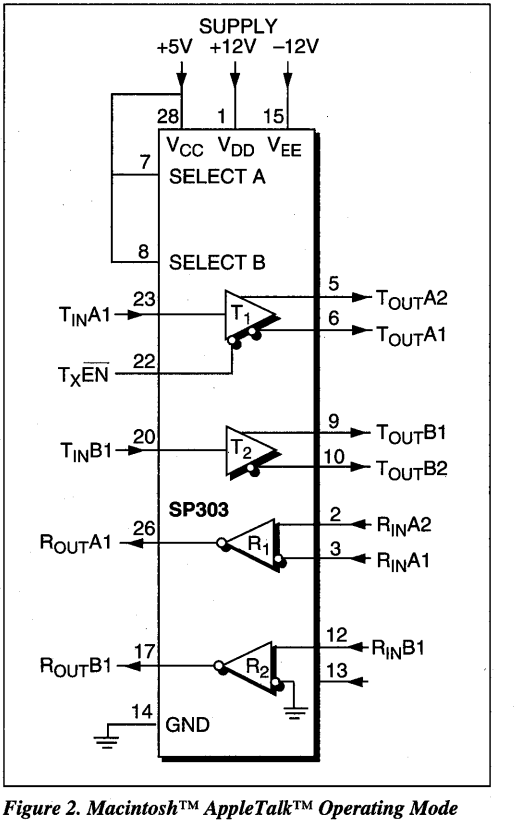


Figure 2. Macintosh™ AppleTalk™ Operating Mode

SP303CT is usually connected to the outside world, it is suggested that the user place transient voltage suppression devices on each of the I/O lines to ensure up to ±25KV ESD protection.

While the part is programmed for RS232 mode, the drivers and receivers can operate up to 200Kbps. The RS232 receiver inputs are capable of receiving signals up to ±30V. The Macintosh™ AppleTalk™ mode inputs and outputs are protected to guard against the situation where an RS232 cable is connected to the port while it is configured for Macintosh™ AppleTalk™ mode.

APPLICATION EXAMPLE MACINTOSH™ APPLETALK™ SERIAL INTERFACE

The schematic below (*Figure 4*) shows the **SP303CT** programmed for Macintosh™ AppleTalk™ operating mode. In this mode the **SP303CT** offers one differential driver used for transmitting data, one differential receiver used for receiving data, one single–ended, non–inverting receiver used to receive a handshake signal, and one single–ended inverting driver used to transmit a handshake signal.

The differential driver used for transmitting data can be put into tri–state mode by bringing the TxEN line high; a low on this pin will enable

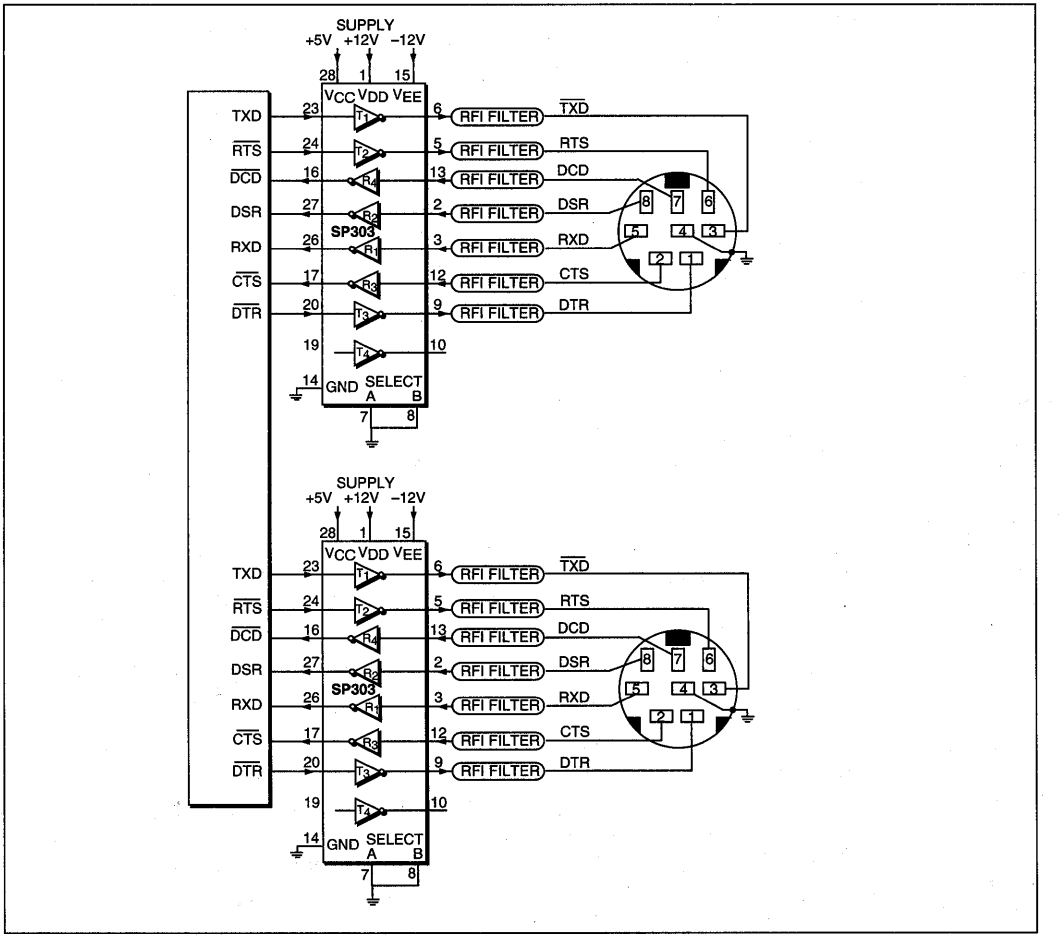


Figure 3. RS232 Interface.

the driver output. This function only applies to the transmit data driver in AppleTalk™ mode. Both differential drivers have output signals on each pin that typically swing ±6V. The peak to peak differential voltage swing is typically ±12V.

The second driver is used for transmitting the handshake output signal and can be used as either a differential driver or single ended. This particular application required a single–ended inverting signal for the handshake output signal.

Some Macintosh equipment requires an extra single–ended inverting receiver which is called a general purpose input. The GPI receiver is normally connected to pin 7 on the external 8 pin connector. This receiver is not available on the SP303CT.

Since the SP303CT is usually connected to the outside world, it is suggested that the user place transient voltage suppression devices on each of the 1/0 lines to ensure up to ±25KV ESD protection.

POWER SUPPLY SEQUENCING

There are two requirements for power supply sequencing for the **SP303**. The first is that V_{DD} is always greater than V_{CC}. The second is that when the part is powered up, V_{DD} must be applied 20ms before V_{CC}.

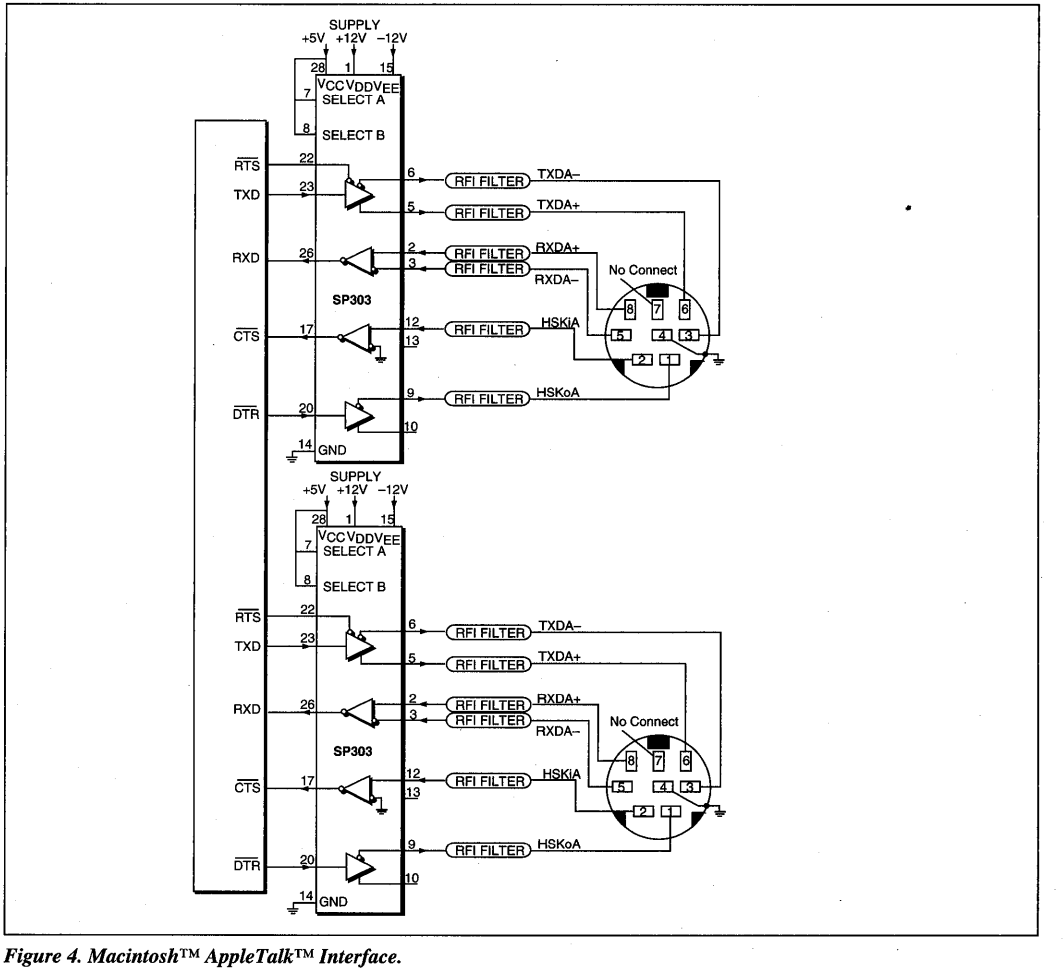


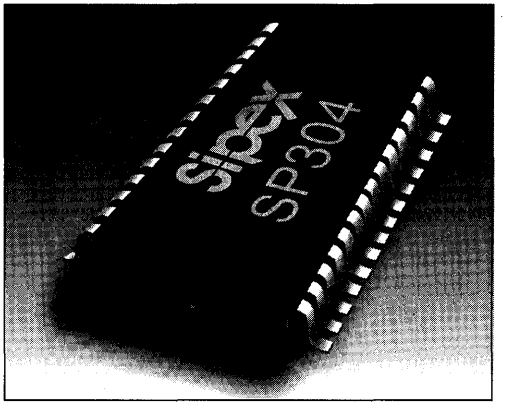
Figure 4. Macintosh™ AppleTalk™ Interface.

ORDERING INFORMATION

Model	Temperature Range	Package
SP303CT	0°C to +70°C	28–pin SOIC
SP303CT/TR	0°C to +70°C	28–pin SOIC/Tape–on–reel

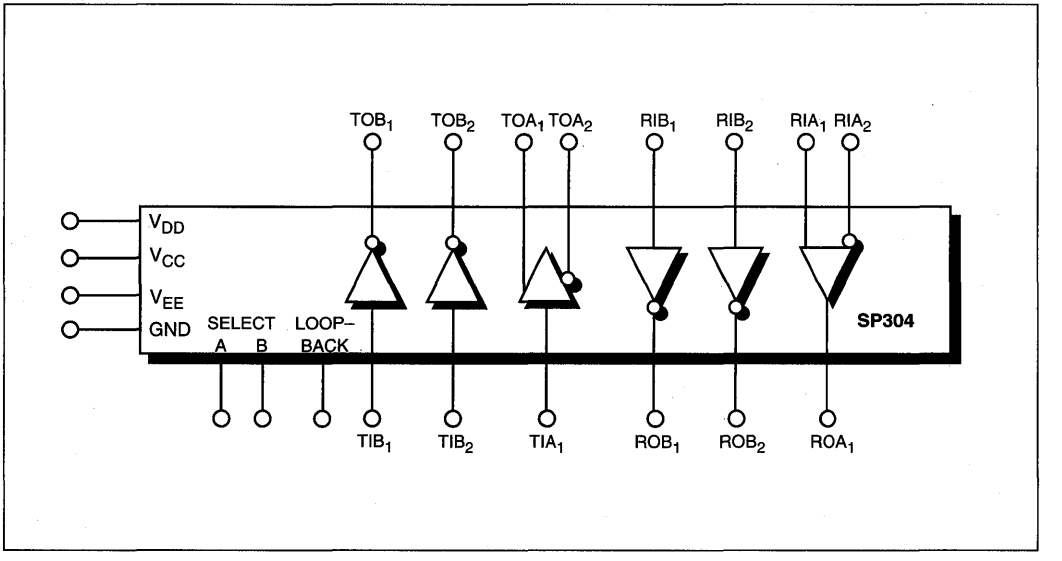
RS232/RS422 Line Drivers/Receivers

- RS232 and RS422 on One Chip
- Multiple Drivers and Receivers
- Software-selectable Modes
- Loopback for Self-Testing
- Short-circuit Protected
- Single-width 24-pin DIP and 28–pin SOIC Packages



DESCRIPTION...

The **SP304** is an enhanced-performance version of the **Sipex SP302** RS232 and RS422 protocol line drivers and receivers. It is pin-for-pin compatible with the **SP302**, and in any configuration, fully meets the requirements of the EIA RS232D and RS422 data communication standards. A loopback test mode is provided. The **SP304** is available in 24-pin single width plastic DIP, and 28-pin SOIC packages for commercial and industrial temperature range operation.



SPECIFICATIONS

($T_{MIN} \le T_A \le T_{MAX}$ and nominal supply voltages unless otherwise noted)

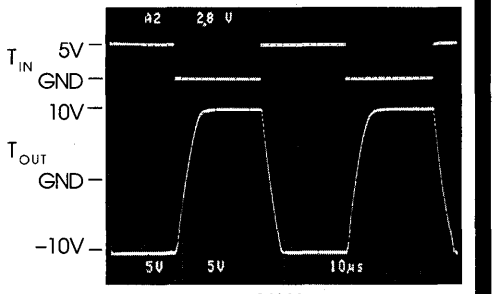
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS232 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	+5.0			V	R_L = 3kΩ, V_{IN} = 0.8V
Low Level Output			-5.0	V	R_L = 3kΩ, V_{IN} = 2.0V
Short Circuit Current			±30	mA	V_{OUT} = 0V
Loopback Output Voltage		-1.5		V	R_L = 3kΩ, V_{EE} = -12.0V; Note 1
Slew rate			30	V/µs	C_L = 50pF, R_L = 3kΩ; T_A = 25°C
Transition Time		3		µs	V_{OUT} from +3V to -3V or -3V to +3V
Transmission Rate			200	kbps	
RS232 RECEIVER					
Input Voltage Range	-15		+15	V	Note 6
Input High Threshold	+1.75		+2.5	V	Positive-going
Input Low Threshold	+0.75		+1.35	V	Negative-going
Input Impedance	3		7	kΩ	
TTL Output Level					
V_{OL}			0.4	V	V_{CC} = +4.75V, I_{OUT} = +1.6mA
V_{OH}	2.4			V	V_{CC} = +4.75V, I_{OUT} = -0.5mA
Receiving Rate			200	kbps	
RS422 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	2.75		6.0	V	I_{OH} = -20mA
Low Level Output			1.0	V	I_{OL} = +20mA
Differential Output	±2			V	R_L = 100Ω
			±6	V	R_L = ∞
Short Circuit Current			±100	mA	Note 2
Output Current			±500	µA	-0.25V < V_o < 6V; power off
Transition Time			400	ns	R_L = 100Ω, C_L = 15pF; Note 3
Transmission Rate			1,000	Kbps	
RS422 RECEIVER					
Common Mode Range			±7	V	Note 4
Differential Input			±15	V	Note 4
Differential Input Threshold	-0.2		+0.2	V	T_A = 25°C
Input Voltage Hysteresis	30			mV	V_{CM} = 0V; T_A = 25°C
Input Resistance	3			kΩ	-7V < V_{CM} < +7V
TTL Output Level					
V_{OL}			0.4	V	V_{CC} = +4.75V, I_{OUT} = +1.6mA
V_{OH}	2.4			V	V_{CC} = +4.75V, I_{OUT} = -0.5mA
Receiving Rate			1,000	Kbps	
Short Circuit Output Current			±120	mA	V_{OUT} = 0V
POWER REQUIREMENTS					
V_{DD} = +12V, ±10%		7	15	mA	Note 5
V_{CC} = +5V, ±10%		5	7	mA	Note 5
V_{EE} = -12V, ±10%		11	20	mA	Note 5
ENVIRONMENTAL					
Operating Temperature					
-CS	0		+70	°C	
-MR	-55		+125	°C	
Storage Temperature	-65		+150	°C	

Notes:

1. In Loopback mode
2. Only one output drive pin per package will be shorted at any time
3. From 10% to 90% of steady-state
4. This is an absolute maximum rating; normal operating levels are V_{in} < 5V
5. Outputs unloaded; Inputs tied to GND; T_A = +25°C; V_L = 0V; LB=0
   Typical SP304 current drains under full load are:
   18mA (+12V), 10mA (-12V) and 7mA (+5V) in RS232 mode only;
   5mA (+12V), 7mA (-12V) and 56mA (+5V) in RS422 mode only;
   12mA (+12V), 14mA (-12V) and 31mA (+5V) in RS232 and RS422 modes;
   RS232 loads 3KΩ, 2500pF, 20kHz; RS422 outputs across 100Ω, 500kHz.

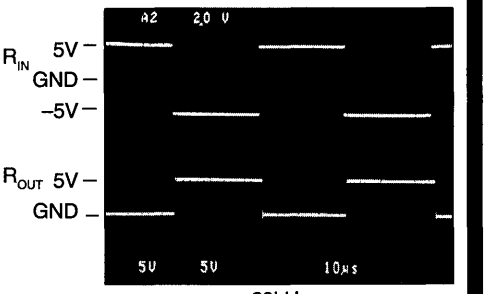
TYPICAL PERFORMANCE CURVES

RS232 Driver



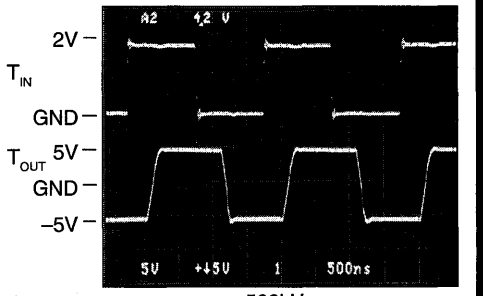
20kHz

RS232 Receiver



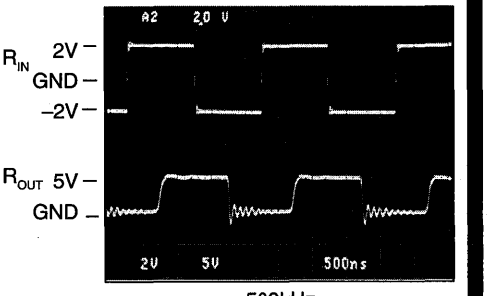
20kHz

RS422 Driver



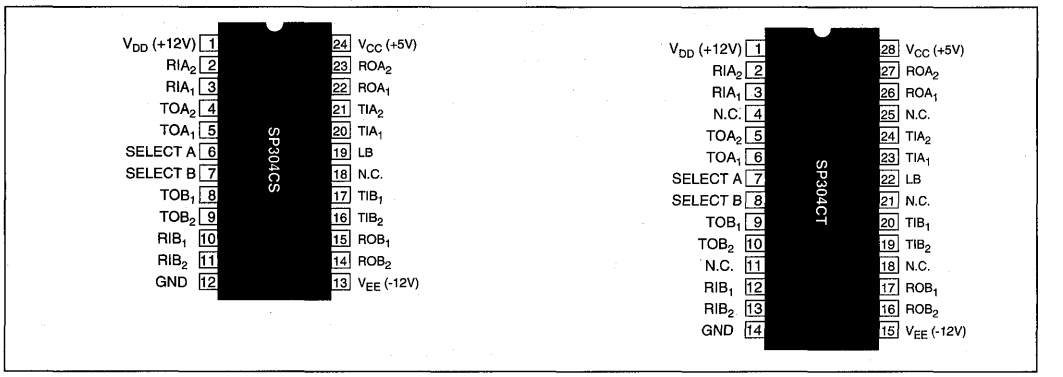
500kHz

RS422 Receiver



500kHz

PIN ASSIGNMENTS



FEATURES...

The **SP304** is a proprietary single-chip device that contain both RS232 and RS422 protocol line drivers and receivers. It is pin–for–pin compatible with the **Sipex SP302**. Like the **SP302**, its configuration may be changed at any time by logic levels on two control lines. In any configuration, the **SP304** fully meets the requirements of both the EIA RS232D and RS422 data communication standards. The **SP304** enhancements include improved isolation from external signals and a true high–impedance driver output in the loopback test mode, and no power–up sequence requirements.

The RS232 line driver circuits convert TTL logic level inputs into inverted RS232 output signals. The RS422 line drivers convert TTL logic levels into RS422 differential output signals. The RS422 line driver outputs feature high source and sink current capability. All line drivers are internally protected against short circuits on their outputs.

The RS232 receivers convert the EIA RS232 input signals to inverted TTL output logic levels. The RS422 receivers convert the EIA RS422 differential input signals into non-inverted TTL output logic levels. Receiver input filtering provides excellent high frequency noise immunity. Input pulses with widths less than 1µs are completely ignored. The RS232 receivers have the additional feature of voltage hysteresis, which helps eliminate spurious output transitions that might result from low amplitude noise voltages during slower-speed signal transitions.

A loopback test mode is provided that puts the driver outputs to a high impedance tri-state level, and routes the driver outputs to their associated receiver inputs. In this configuration, the signal path is non-inverting from the TTL driver input to the receiver TTL output. This operating mode allows the controlling system to perform diagnostic self-test of the RS232/RS422 driver/receiver circuitry at speeds up to 3,000 bits per second. In the loopback mode, a ±13.2V input range may be applied to the receiver inputs with no interference to the loopback test. In addition, the driver outputs are in a true high–impedance state during loopback.

The **SP304** is available in 24-pin singlewidth (0.300") plastic DIP and 28-pin SOIC packages, for operation over the commercial and industrial temperature ranges.

USING THE SP304

POWER SUPPLIES

The **SP304** requires ±12V and +5V for full RS232 and RS422 operation. The ±12V supplies set up the RS232 ±9V voltage swings, and the +5V is used for the internal logic that formats the communications mode and controls the loopback function. The supply voltages can be decreased to as low as ±7V for V_{DD} and V_{EE}, and

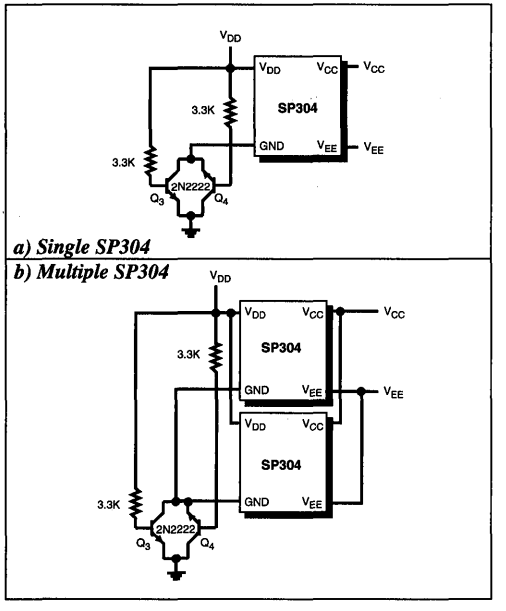


Figure 1. Isolating the SP304 from Ground.

4.0V for V_{CC}. Under these supply conditions, derated performance can be expected.

POWER SUPPLY SEQUENCING

There are no special power–up sequencing requirements for the **SP304**.

GENERAL USAGE

RS232 Operation

The **SP304** is a fully compliant RS232 device. Its outputs are fully protected against shorts to ±20V with no external circuitry. If the potential exists for momentary shorts to voltages greater than ±20V, it is recommended that a 220Ω resistor be wired in series with each driver output. This will limit any damage from the higher short-circuit current from these higher voltage potentials. Voltage clamps such as back-to- back Zener diodes can be used to clamp the driver outputs to "safe" levels. Short circuit current to ground is internally limited, and can therefore be sustained infinitely. Under normal operating conditions, the drivers can typically source 7mA at ±5V output, which exceeds the minimum RS232 standards requirement.

If an **SP304** transmitter output occupies a data transmission line with other RS232 devices which are not powered by the same power supplies, it is possible that a device that is not powered will have a low impedance path to ground at its driver output. The RS232 standards require that with no power applied to the device, the impedance from a transmitter output to ground must be greater than 300Ω. This can be easily achieved as shown in *Figure 1a*, where an external transistor is used as a switch to isolate an **SP304** from ground in the power off condition. With V_{DD} turned on, the transistor switch is on, connecting ground (GND) for the device to the circuit ground. In a power off condition, this transistor is switched off, thus isolating the unit from circuit ground, and thereby leaving the driver in a high impedance state. Multiple **SP304s** can be connected as shown in *Figure 1b.*

RS422 OPERATION

The **SP304** is fully compliant RS422 devices when operating in the RS422 mode. Baud rate and drive capability have been balanced to provide as much versatility as possible. The **SP304** are both guaranteed for a 1Mbps data rate,

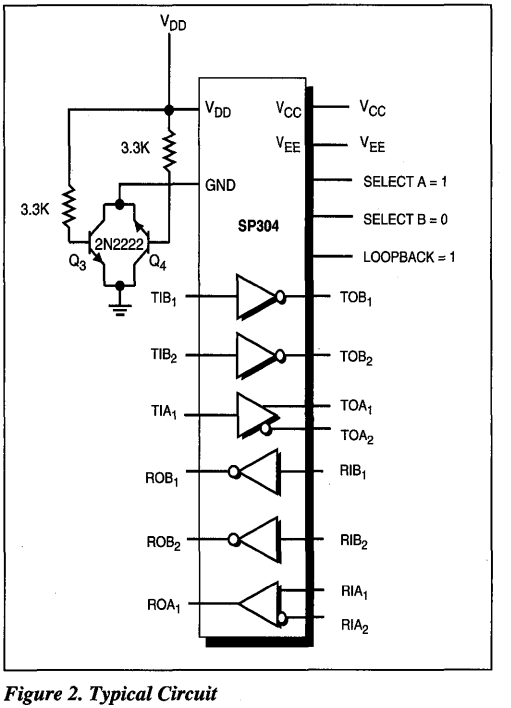


Figure 2. Typical Circuit

supplying ±2V minimum into a 100Ω load. Short circuit protection for the RS422 operating mode is the same as in the RS232 mode. The driver outputs can be shorted to ground for an infinite duration, with a maximum current of ±100mA.

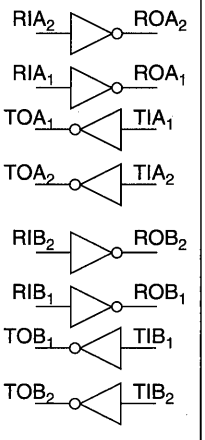
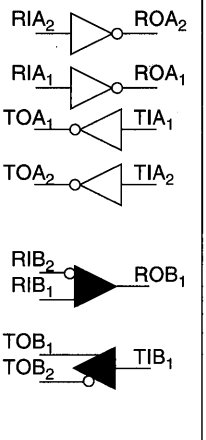
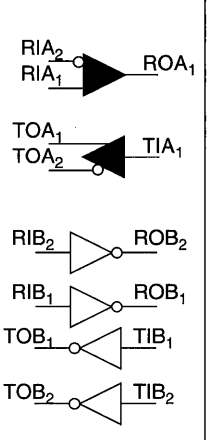
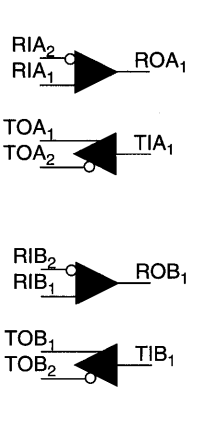
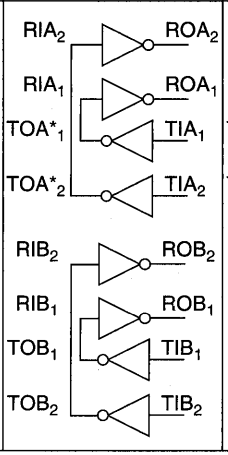
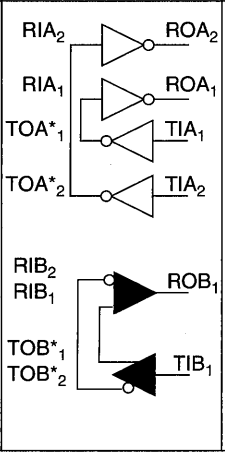
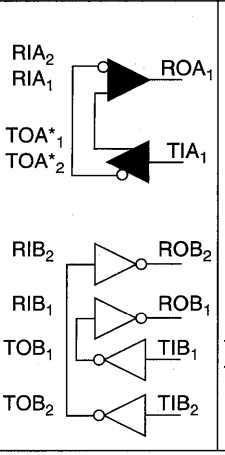
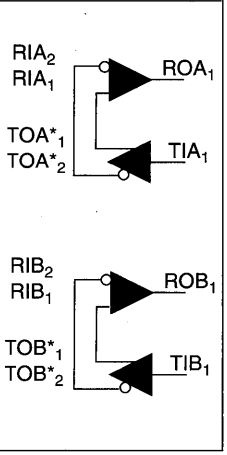
The RS422 receivers accept differential signals at a 1Mbps rate, and translate them to a non-inverted TTL output. The receivers are specified with a ±15V differential input voltage, which means that to operate normally, the difference betweeen the voltages at the inputs cannot exceed ±15V. The common mode voltage is specified as ±7V. This identifies the midpoint of the range about which the differential input must lie so that the receiver can detect a change of state. Within this ±7V range, the receivers will recognize a change in state with a ±200mV differential threshold voltage. Since the RS232 and RS422 inputs are shared, all receiver inputs are protected to ±30V to guard against inadvertently applying an RS232 signal to an input that is configured for RS422.

Figure 2 shows a typical circuit for the **SP304**. In this case the **SP304** is shown configured for one (1) duplex RS422 and two (2) duplex RS232 communication paths.

CONFIGURING THE SP304

The Figures on pages 7 and 8 show the various combinations of simultaneous RS232 and RS422 operation that can be achieved with the **SP304**. Each of these configurations are software selectable by logic level on the SELECT A and SELECT B control lines. Configuration can be changed "on-the-fly".

SP304 CONTROL LOGIC CONFIGURATION

SELECTION	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE
SELECT A: SELECT B:	0 0	0 1	1 0	1 1
NON– LOOPBACK (LB = 1)				
LOOPBACK (LB=0)				

RS232 DRIVER
* Tri–state Output

RS232 RECEIVER

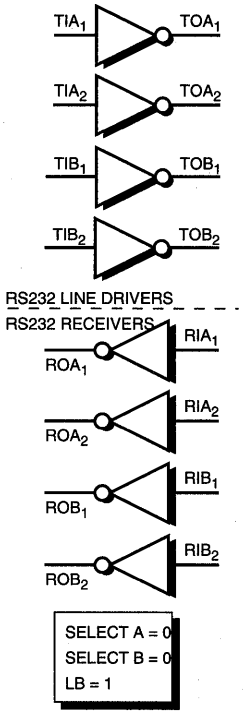
RS422 RECEIVER

RS422 DRIVER

SP304 CONFIGURATIONS

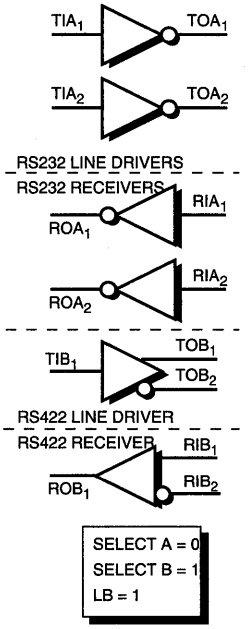
Four-Channel Duplex RS232

Four independent channels of RS232 line driver and four channels of RS232 receiver.



Two-Channel Duplex RS232 & One-Channel Duplex RS422

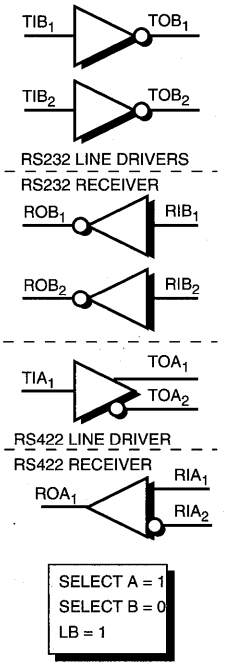
Two RS232 line drivers and receivers, and a single RS422 line driver and receiver.



SP304 CONFIGURATIONS

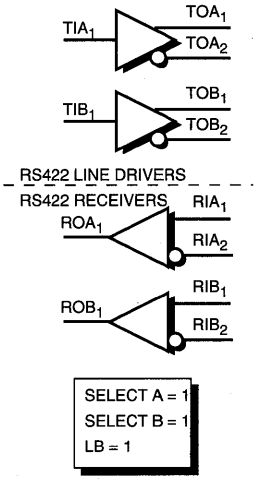
Two-Channel Duplex RS232 & One-Channel Duplex RS422 Opposite Drivers

Two RS232 line drivers and receivers, and a single RS422 line driver and receiver. At first glance, this is the same configuration as that immediately to the left. Note however that functions are activated on the opposite channels.



Two-Channel Duplex RS422

Two RS422 line drivers and two RS422 receivers.

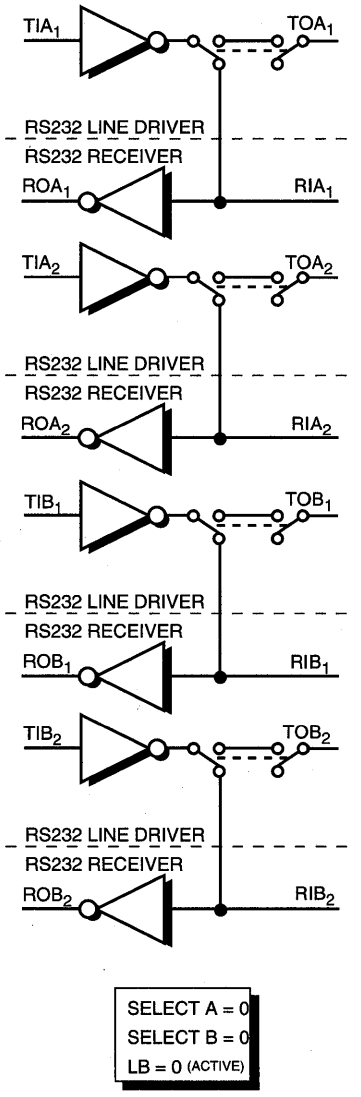


LOOPBACK

The **SP304** has a function called loopback, which is essentially a chip self-test. However, by connecting system test loops with the inputs and outputs of the **SP304**, a system-level diagnostic can be run on power-up or on command. The test loops can be enabled and disabled allowing both system test and operation with the same components. A maximum data rate for loopback of 3Kbps is recommended. Loopback is a pin-programmable function, activated by a logic low on the **LB** pin (19). As shown in these figures, the loopback function internally con-

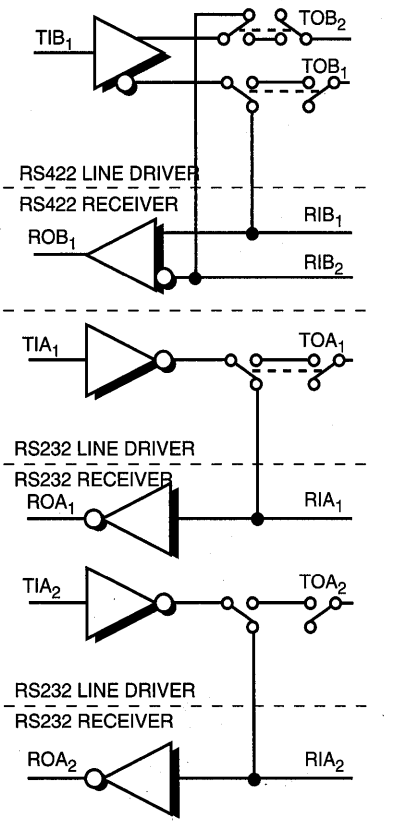
SP304 CONFIGURATIONS IN LOOPBACK MODE

Two -Channel Full Duplex RS232



SELECT A = 0
SELECT B = 0
LB = 0 (ACTIVE)

One-Channel Full Duplex RS232 & One-Channel Full Duplex RS422



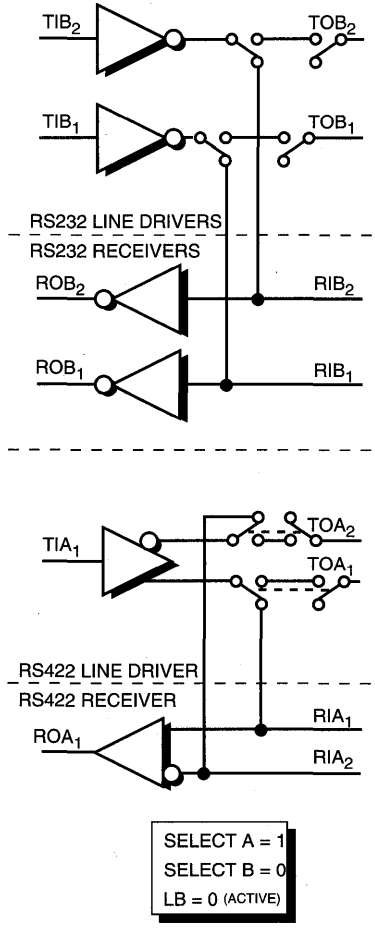
SELECT A = 0
SELECT B = 1
LB = 0 (ACTIVE)

necting the driver outputs to the corresponding receiver inputs, and switches the output pin to a high impedance from V_{EE} to ground. Receiver outputs are left active for signal verification.

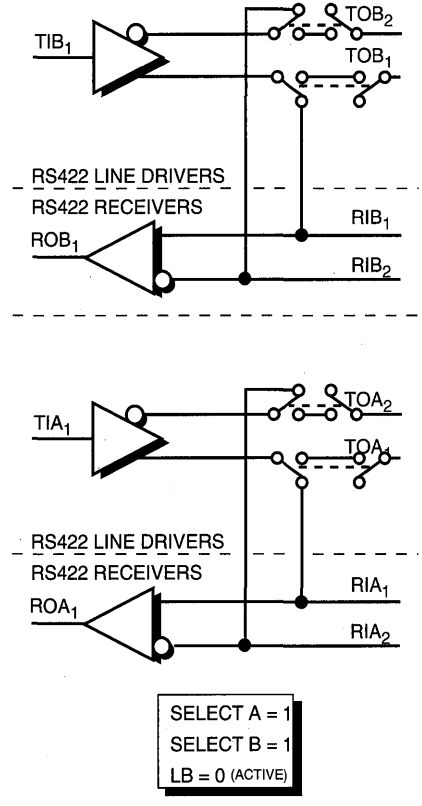
During loopback, the receiver inputs are tied to ground via a 5kΩ pulldown resistor. The receiver inputs can accept the full ±15V swings with no interference to the loopback function.

SP304 CONFIGURATIONS IN LOOPBACK MODE

One-Channel Full Duplex RS232 & One-Channel Full Duplex RS422 Opposite Drivers



Two-Channel Full Duplex RS422

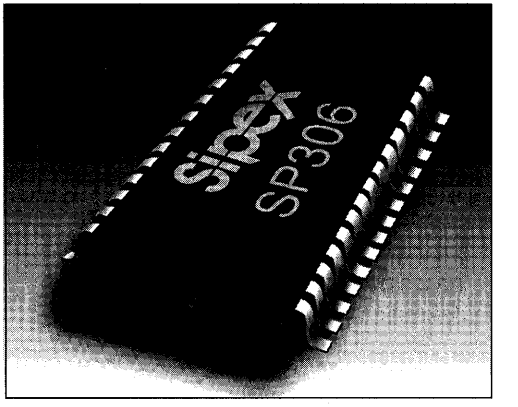


ORDERING INFORMATION

Model	Max # of Duplex Channels RS232	RS422	Temperature	Package
SP304CS	4	2	0°C to +70°C	24-pin Single–Width Plastic DIP
SP304CT	4	2	0°C to +70°C	28-pin SOIC
SP304ES	4	2	-40°C to +85°C	24-pin Single–Width Plastic DIP
SP304ET	4	2	-40°C to +85°C	28-pin SOIC

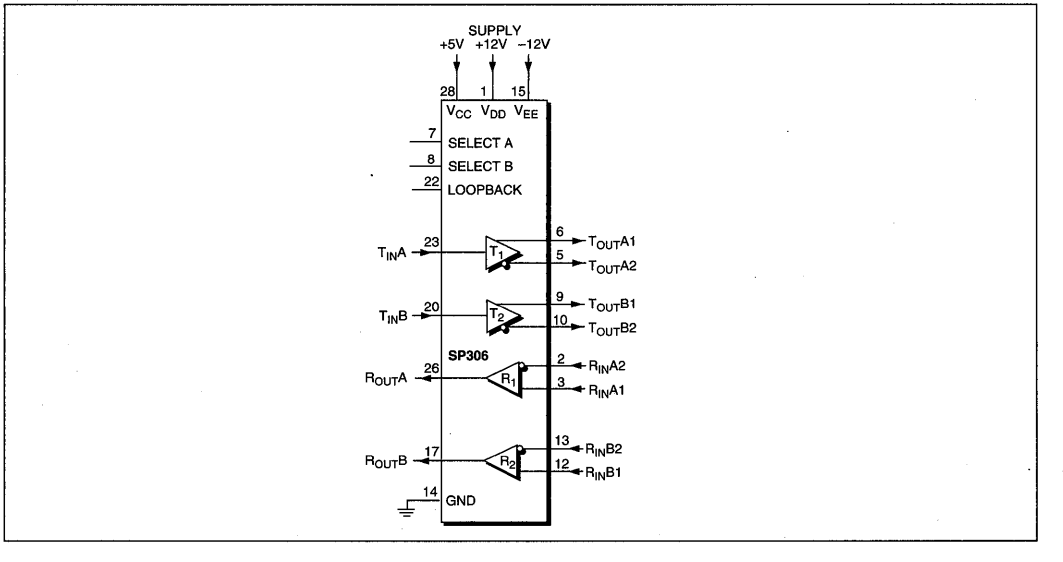
RS422/RS423 Line Drivers/Receivers

- Single chip serial transceiver supports RS422 or RS423 interfaces
- Programmable Selection of Interface
- Two Full–Duplex Channels of Either Interface
- Software–Selectable Mode
- Loopback for Self–Testing
- Short–Circuit Protected
- Surface Mount Packaging



DESCRIPTION...

The **SP306** is a single chip device that offers both RS422 and RS423–type serial interfaces. The device can be programmed to provide two full–duplex channels of either RS422 or RS423 via two mode control pins. The **SP306** also features a loopback function that can be activated in any operating mode. The **SP306** is available in a 28–pin SOIC package for operation over the commercial temperature range.



SPECIFICATIONS

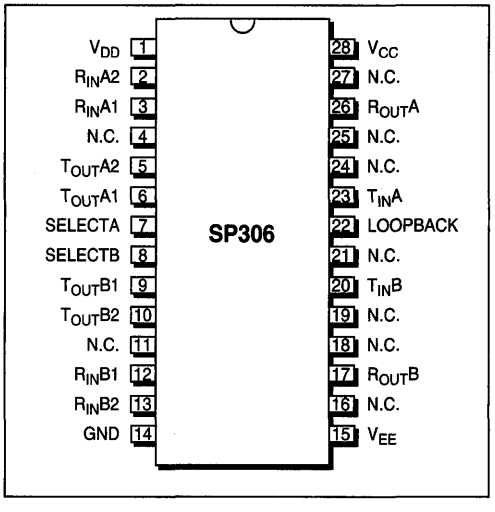
($T_{MIN} \leq T_A \leq T_{MAX}$ and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RS423 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	+3.0		+6.0	V	R_L = 450Ω, V_{IN} = 0.8V; Note 6
			(V_{DD} – 0.7V)	V	R_L = ∞
Low Level Output	–3.0		–6.0	V	R_L = 450Ω, V_{IN} = 2.0V; Note 6
			(V_{EE} +0.7V)	V	R_L = ∞
Short Circuit Current			±40	mA	V_{OUT} = 0V; Note 2
Transition Time		720		ns	R_L = 450Ω, C_L = 50pF; Note 3
Transmission Rate			100	Kbps	
RS423 RECEIVER					
Input Threshold	–200		+200	mV	Common–mode = ±7V; Note 1
Input Impedance	4			KΩ	R_{IN} = ±10V
TTL Output Level					
V_{OL}			0.4	V	V_{CC} =+4.75V, I_{OUT} =+1.6mA
V_{OH}	2.4			V	V_{CC} =+4.75V, I_{OUT} =-0.5mA
Receiving Rate			100	Kbps	
RS422 DRIVER					Note 3
TTL Input Level					
V_{IL}	0		0.8	V	
V_{IH}	2.0			V	
High Level Output	+2.75		+6	V	I_{OH} = –20mA
Low Level Output			+1.0	V	I_{OL} = 20mA
Differential Output	±2.0			V	R_L = 100Ω
			±6.0	V	RL = ∞
Short Circuit Current			±100	mA	
Output Current			±500	µA	–0.25V < V_O < 6V; Power off
Transition Time			400	ns	R_L=450Ω, C_L=15pF; Note 3
Transmission Rate			500	Kbps	
RS422 RECEIVER					
Common Mode Range			±7	V	Note 4
Differential Input			±15	V	Note 4
Differential Input Threshold	–0.2		+0.2	V	T_A=25°C
Input Voltage Hysteresis	30			mV	V_{CM}=0V;T_A=25°C
Input Resistance	3			KΩ	–7V<V_{CM}<+7V
TTL Output Level					
V_{OL}			0.4	V	V_{CC}=+4.75V, I_{OUT}=+1.6mA
V_{OH}	2.4			V	V_{CC}=+4.75V, I_{OUT}=–0.5mA
Receiving Rate			500	Kbps	
Short Circuit Output Current			±120	mA	V_{OUT}=0V
POWER REQUIREIMENTS					
V_{DD} = +12V		7	15	mA	All Transmitter outputs R_L=∞
V_{CC} = +5V		5	7	mA	T_A=25°C
V_{EE} = –12V		11	20	mA	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
–C	0		+70	°C	
–M	–55		+125	°C	
Storage Temperature	–65		+150	°C	
Package					
–C	28–pin SOIC				
–F	28–pin Ceramic Flatpack				

Note:

1. The common mode voltage is defined as the algebraic mean of the two voltages appearing at the receiver input terminals with respect to the receiver circuit ground.
2. Only one output drive pin per package will be shorted at any time.
3. From 10% to 90% of steady state.
4. This is an absolute maximum rating. Normal operating levels are $V_{IN} \leq 5V$.
5. Outputs unloaded. Inputs tied to GND; T_A=+25°C; V_{IL} = 0V; LB = 0.
6. V_{OL}/V_{OH} will typically be ±3V over –55°C to +125°C with 450Ω loads.

PINOUT



PIN ASSIGNMENTS

Pin 1 — V_{DD} — +12V Power Supply.

Pin 2 — $R_{IN}A2$ — RS422 input.

Pin 3 — $R_{IN}A1$ — RS422/RS423 input.

Pin 4 — N.C. — No Connection.

Pin 5 — $T_{OUT}A2$ —RS422 output.

Pin 6 — $T_{OUT}A1$ — RS422/RS423 output.

Pin 7 — SEL A — Select A; used with Select B (pin 8) to select operating mode; please refer to ***SP306** Control Logic Configuration* section for truth table.

Pin 8 — SEL B — Select B; used with Select A (pin 7) to select operating mode; please refer to ***SP306** Control Logic Configuration* section for truth table.

Pin 9— $T_{OUT}B1$— RS422/RS423 output.

Pin 10 — $T_{OUT}B2$ — RS422 output.

Pin 11 — N.C. — No Connection.

Pin 12— $R_{IN}B1$— RS422/RS423 input.

Pin 13 — $R_{IN}B2$— RS422 input

Pin 14 — GND — Signal ground. Connected to logic and chasis ground.

Pin 15 — V_{EE} — –12V Power Supply.

Pin 16 — N.C. — No Connection.

Pin 17 — $R_{OUT}B$ — TTL output.

Pin 18 — N.C. — No Connection.

Pin 19 — N.C. — No Connection.

Pin 20 — $T_{IN}B$ — TTL input.

Pin 21 — N.C. — No Connection.

Pin 22 — LOOPBACK — Active low; logic "1" selects operating mode controlled by SELECT A and SELECT B; logic "0" selects loopback configuration for whatever operating mode is selected by states of SELECT A and SELECT B.

Pin 23 — $T_{IN}A$ — TTL input.

Pin 24 — N.C. — No Connection.

Pin 25 — N.C. — No Connection.

Pin 26 — $R_{OUT}A$ — TTL output.

Pin 27 — N.C. — No Connection.

Pin 28 — V_{CC} — +5V Power Supply.

FEATURES...

The **SP306** is a single chip device that offers both RS422 and RS423 serial interfaces. The device can be programmed via two control mode pins (7 and 8). In either operating mode, the **SP306** provides two full–duplex channels. A loopback function is also provided for chip self–test, which connects driver outputs to receiver inputs with no external circuitry.

The RS422 drivers convert TTL logic levels into RS422 differential output signals. The RS422 line driver outputs feature high source

and sink current capability. The RS423 line drivers convert TTL logic levels into inverted RS423 output signals. All line drivers are internally protected against short circuits on their outputs.

The RS422 receivers convert the RS422 differential input signals into non–inverted TTL logic levels. Receiver input thresholds are ±200mV. The RS422 receivers can receive input data up to 1Mbps. The RS423 receivers convert the RS423 input signals into inverted TTL output logic levels. The RS423 receivers have an input threshold of ±200mV, and can receive data up to 100Kbps.

A loopback test mode is provided that puts the driver outputs into a high impedance tri–state level, and routes the driver outputs to their associated receiver inputs. In this configuration, the signal path is non–inverting from the TTL driver inputs to the receiver TTL outputs. This operating mode allows the controlling system to perform diagnostic self–test of the RS422/423 transceiver circuitry at speeds up to 3Kbps.

APPLICATION INFORMATION

Control Logic Configuration

Software control of the **SP306** is via two select pins (7 and 8) and a loopback control pin (22). SELECT A and SELECT B allow the user to program the **SP306** for four different interface modes. Loopback mode can be selected in any of these interface modes. The figures that follow outline the various operating modes that are supported by the **SP306**.

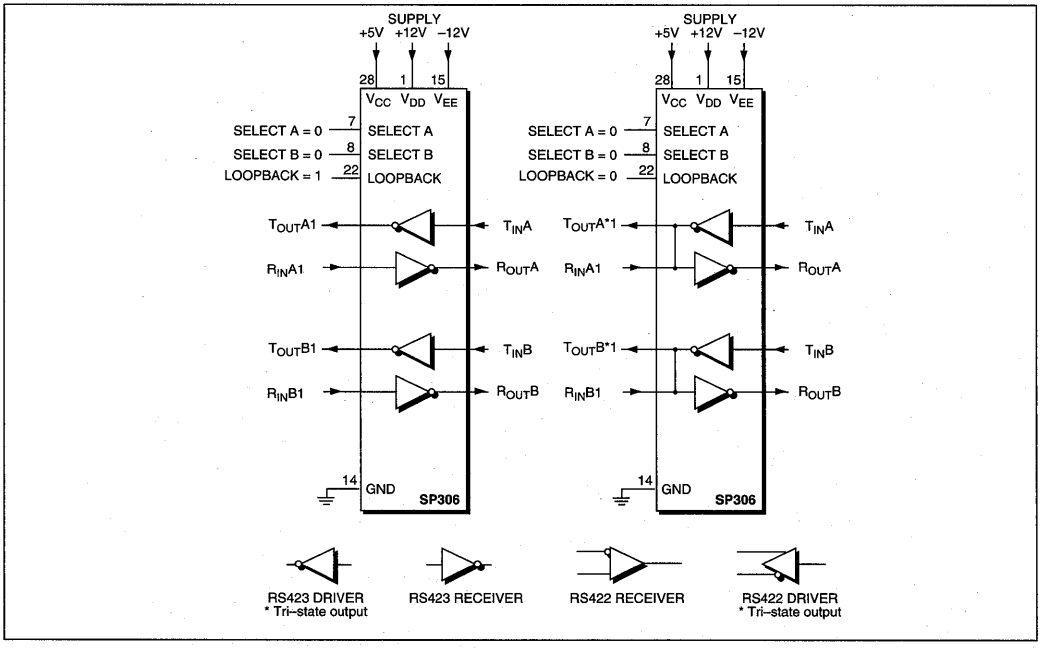


Figure 1. Control Input Configuration — SELECT A = 0, SELECT B = 0

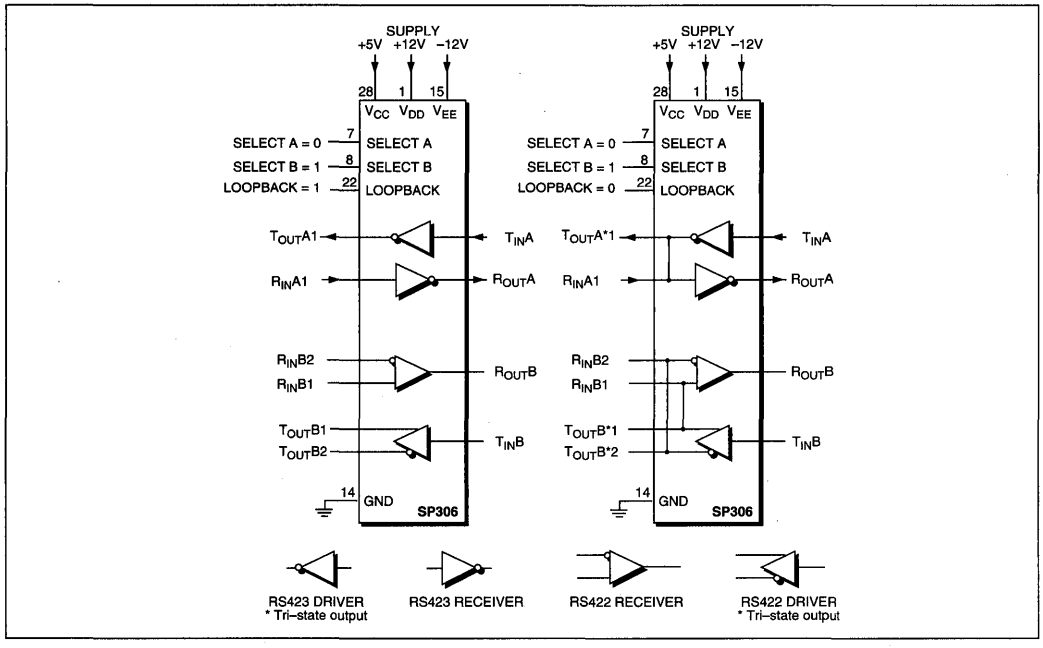


Figure 2. Control Input Configuration — SELECT A = 0, SELECT B = 1

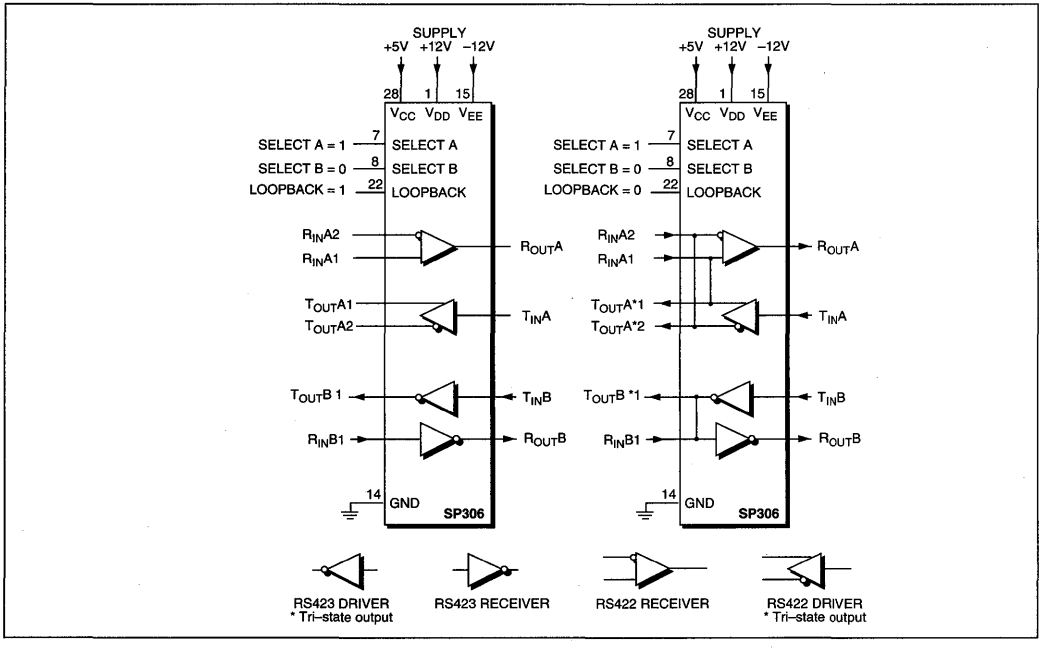


Figure 3. Control Input Configuration — SELECT A = 1, SELECT B = 0

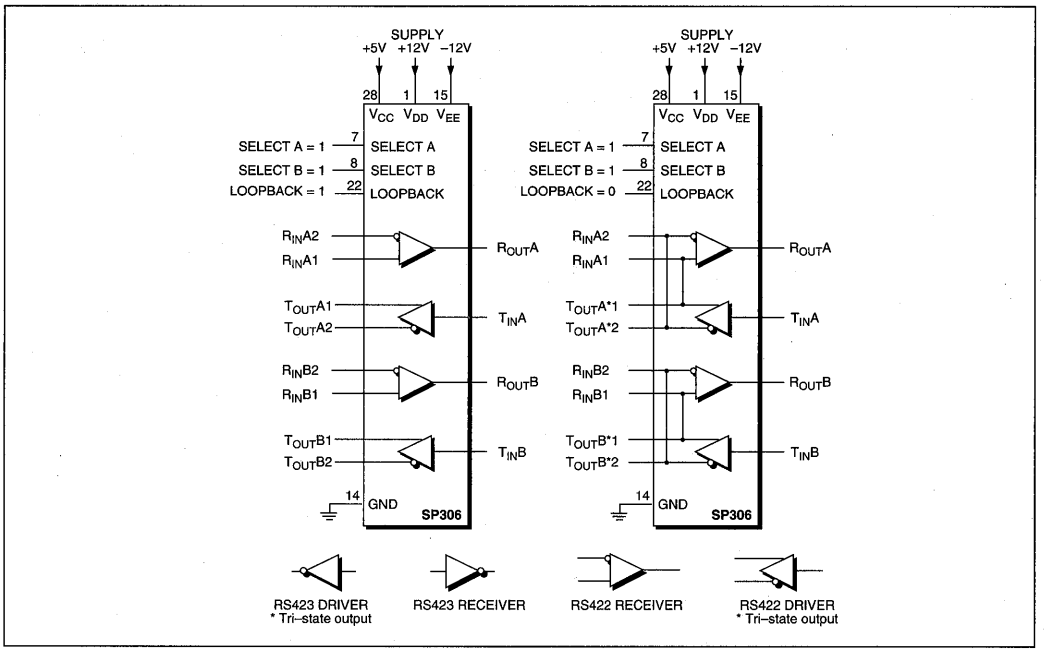


Figure 4. Control Input Configuration — SELECT A = 1, SELECT B = 1

ORDERING INFORMATION

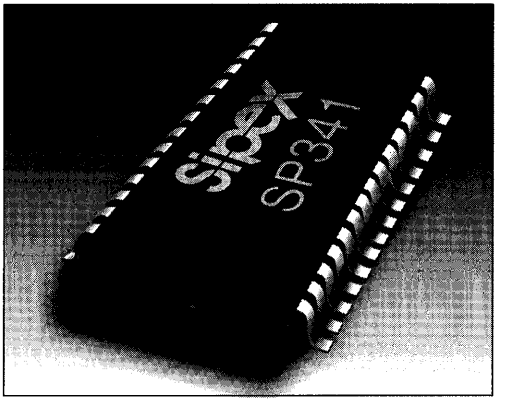
Model	Temperature Range	Package
Two full–duplex channels RS422/423		
SP306CT	0°C to +70°C	28–pin SOIC
SP306MF	–55°C to +125°C	28–pin Ceramic Flatpack

SP341

+3.3V Powered Multi-Channel EIA/TIA 562 Drivers/Receivers

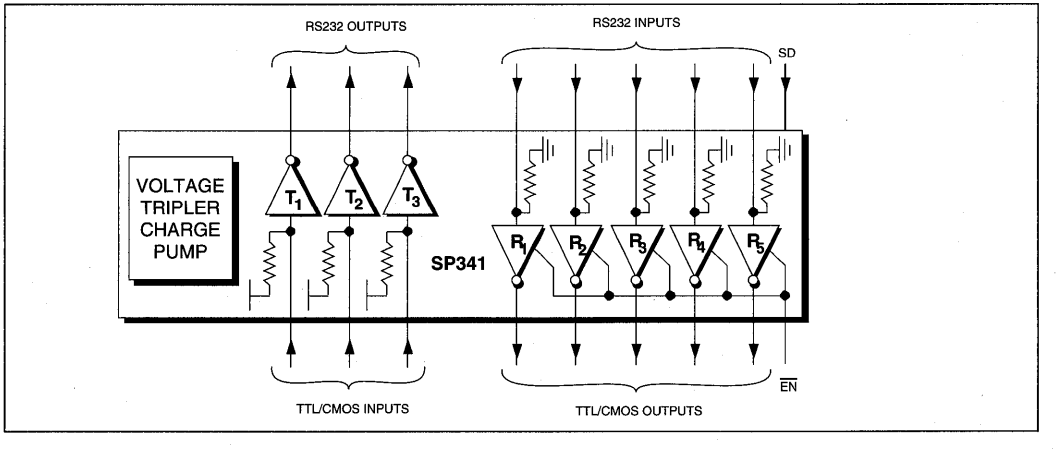
FEATURES

- Operate From Single +3.3V Power Supply
- Meet all EIA/TIA 562 Specifications
- 3 Drivers and 5 Receivers
- ±30V Receiver Input Levels
- 3-State TTL/CMOS Receiver Outputs with Wake-up Feature
- Power Management Circuit to Optimize Power Consumption/Performance
- Low Power CMOS: 4 mA Operation
- Low Power Shutdown Current: <1µA
- Output Over–Voltage Protection: ±15V



DESCRIPTION

The Sipex **SP341** is an enhanced version of Sipex SP241 line drivers/receivers which operates at +3.3V. The **SP341** is pin compatible with **SP241** except one driver has been removed to provide two pins necessary for +3.3V operation. The **SP341** meets EIA/TIA 562 specifications, which guarantees inter–operability with RS232 interfaces. The **SP341** includes a **Sipex** patent–pending voltage–tripler charge pump, which allows the **SP341** to operate from a single +3.3V power supply. A 1µF capacitor should be connected between the "2 V_{CC}" pin and ground. The other charge pump and decoupling capacitors should be at least 1µF. The charge pump capacitors can be either polarized or non–polarized.



ABSOLUTE MAXIMUM RATINGS

* This is a stress rating only and functional operation of the device at these or any other above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

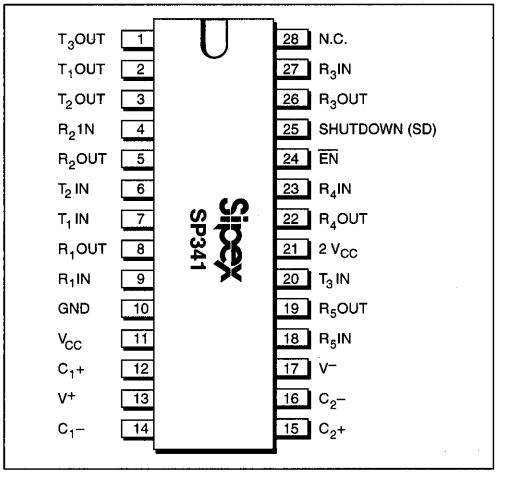
V_{cc} ..... +6 V
V+ ..... (Vcc-0.3V) to +13.2V
V- 13.2V
Input Voltages
T_{IN} ..... -0.3V to (Vcc +0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+, +0.3V) to (V-, -0.3V)
R_{OUT} ..... -0.3V to (Vcc +0.3V)
Short Circuit Duration T_{OUT} ..... Continuous
Power Dissipation
CERDIP 675mW
(derate 9.5mW/°C above +70°C)
Plastic Dip 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

SPECIFICATIONS

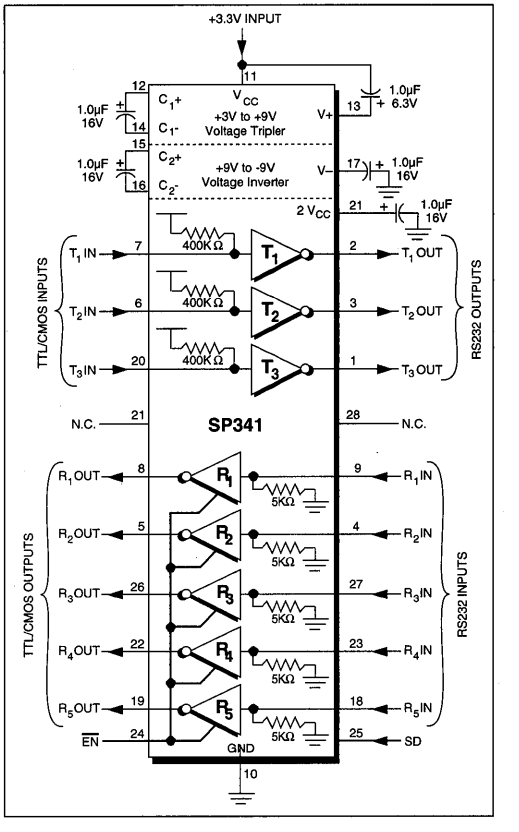
V_{CC} = +3.3V ± 10%, 1µF charge pump capacitors; T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TTL INPUT					
Logic Threshold					
Low			0.8	Volts	T_{IN}
High	2.0			Volts	T_{IN}
Logic Pullup Current		15	200	µA	T_{IN} = 0V
Data Rate			20	Kbits/sec	C_L = 2500pF, R_L = 3KΩ
			120	Kbits/sec	C_L = 1000pF, R_L = 3KΩ
TTL OUTPUT					
TTL CMOS Output Voltage					
Low			0.4	Volts	I_{OUT} = 3.2mA; V_{CC} = +3.3V
High	2.8			Volts	I_{OUT} = –40µA; V_{CC} = +3.3V
Leakage Current		0.05	±10	µA	$\overline{EN}$=V_{CC}; 0V≤R_{OUT}≤V_{CC}; T_A=+25°C
RS232 OUTPUT					
Output Voltage Swing	±3.7	±4.2		Volts	All transmitter outputs loaded with 3KΩ to Ground
Output Resistance	300			Ohms	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±10		mA	Infinite duration
RS232 INPUT					
Voltage Range	-30		+30	Volts	
Voltage Threshold					
Low	0.7	1.2		Volts	V_{CC} = 3.3V, T_A = +25°C
High		1.7	2.4	Volts	V_{CC} = 3.3V, T_A = +25°C
Hysteresis	0.2	0.5	1.0	Volts	Vcc = 3.3V
Resistance	3	5	7	KΩ	T_A = +25°C
DYNAMIC CHARACTERISTICS					
Propagation Delay		1.5		µs	RS232 to TTL
Instantaneous Slew Rate			30	V/µs	C_L=10pF, R_L=3-7KΩ; T_A=+25°C
Transition Region Slew Rate		4		V/µs	C_L = 2500pF, R_L=3KΩ; measured from +2V to –2V or –2V to +2V
Output Enable Time		400		ns	
Output Disable Time		250		ns	
POWER REQUIREMENTS					
Vcc Power Supply Current		4	10	mA	No load, T_A = +25°C
		13		mA	All transmitters R_L=3KΩ; T_A=+25°C
Shutdown Supply Current		1	10	µA	T_A = +25°C

SP341 PINOUT



SP341 TYPICAL CIRCUIT



SHUTDOWN FEATURE (SD)

Since power consumption is critical, especially in +3.3V battery operation, the **SP341** has a built-in intelligent power management circuit which constantly optimizes its power-consumption/performance. To further save power, the **SP341** can be shut-down by applying V_{CC} to the SD pin to stop the charge pump and reduce I_{CC} to around 1µA. In shutdown mode, all receivers are in a high impedance three-state mode.

WAKE-UP FEATURE

The **SP341** has a wake-up feature that keeps all the receivers in an enabled state when the device is in the shutdown mode, unless explicitly disabled by the $\overline{EN}$ pin. With only the receivers activated, the **SP341** typically draws less than 1µA supply current (10µA maximum). In the case of a modem interfaced to a computer in power down mode, the Ring Indicator (RI) signal from the modem would be used to "wake up" the computer, allowing it to accept data transmission.

After the ring indicator signal had propagated through the **SP341** receiver, it can be used to trigger the power management circuitry of the computer to power up the microprocessor and bring the SD pin of the **SP341** to a logic low, taking it out of the shutdown mode. The receiver propagation delay is typically 1µs. The enable time for V^+ and V^- is typically 2ms. After V^+ and V^- have settled to their final values, a signal can be sent back to the modem on the data terminal ready (DTR) pin signifying that the computer is ready to accept and transmit data.

SD	$\overline{EN}$	Power Up/Down	Receiver Outputs
0	0	Up	Enable
0	1	Up	Tri–state
1	0	Down	Enable
1	1	Down	Tri–state

Table 1. Wake–Up Function Truth Table

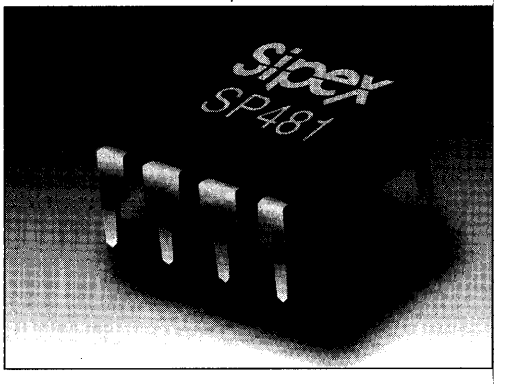
ORDERING INFORMATION

Model	Temperature Range	Package
SP341CT	0°C to +70°C	28–pin SOIC
SP341ET	–40°C to +85°C	28–pin SOIC

CT and ET packages available Tape–on–Reel; please consult the factory

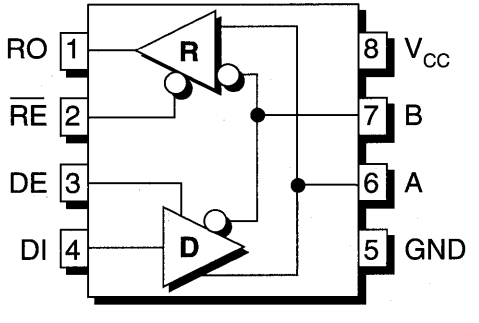
Low–Power RS485/RS422 Interface Transceiver

- Low Power: I_{CC} = 300µA Typical
- Single +5V Supply
- Power Up/Down Glitch-Free Driver Outputs - Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or With the Power Off
- Combined Impedance of a Driver Output and Receiver Allows Up to 32 Transceivers on the Bus
- SP481 Provides SHUTDOWN mode
- Pin Compatible with the MAX481, MAX485 and LTC485



DESCRIPTION...

The Sipex **SP481/485** are low power half–duplex transceivers designed for RS485 and RS422 applications with extended common mode range (+12V to -7V). The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. The **SP481** features a SHUTDOWN mode for <1µA standby power consumption. The **SP481/485** are fully specified over the commercial and industrial temperature ranges.



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC}) ..... +12 V
Control Input Voltages ..... -0.5V to V_{CC} +0.5V
Driver Input Voltage ..... -0.5V to V_{CC} +0.5V
Driver Input Voltage ..... ±14V
Receiver Input Voltages. ..... ±14V
Receiver Output Voltage ..... -0.5V to V_{CC} +0.5V

* This is a stress rating only and functional operation of the device at these or any other above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

SPECIFICATIONS

V_{CC} = 5V ± 5%, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DIFFERENTIAL DRIVER					
Output Voltage			5	Volts	Unloaded; $R_L = \infty$
	2			Volts	with load; R = 50Ω; (RS422)
	1.5		5	Volts	with load; R = 27Ω; (RS485); *Fig. 1*
Magnitude Change of Output			0.2	Volts	R = 27Ω of R = 50Ω; *Fig. 1*
					Voltage for Complementary Output States
Common Mode Output			3	Volts	R = 27Ω or R = 50Ω; *Fig. 1*
Magnitude Change of Driver Common Mode Output			0.2	Volts	R = 27Ω or R = 50Ω; *Fig. 1*
					Voltage for Complementary Output States
Input High Voltage	2.0			Volts	DE, DI, $\overline{RE}$
Input Low Voltage			0.8	Volts	DE, DI, $\overline{RE}$
Input Current			±2	µA	DE, DI, $\overline{RE}$
Input Current (A, B)					DE = 0, V_{CC} = 0V or 5.25V
			+1.0	mA	V_{IN} = 12V
			-0.8	mA	V_{IN} = -7V
Driver Short-Circuit Current					-7V ≤ V_O ≤ +10V
V_{OUT} = HIGH	35		250	mA	
V_{OUT} = LOW	35		250	mA	
Driver Data Rate			5	Mbps	
Driver Input to Output	20	30	60	ns	R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pf;
Driver Input to Output	20	30	60	ns	*Figures 3 and 5*
Driver Output to Output		5	10	ns	
Driver Rise or Fall Time	3	15	40	ns	
Driver Enable to Output High		40	70	ns	C_L = 100pF; *Fig. 4 & 7*; S_2 closed
Driver Enable to Output Low		40	70	ns	C_L = 100pF; *Fig. 4 & 7*; S_1 closed
Driver Disable Time from Low		40	70	ns	C_L = 15pF; *Fig. 4 & 7*; S_1 closed
Driver Disable Time from High		40	70	ns	C_L = 15pF; *Fig. 4 & 7*; S_2 closed
RECEIVER					
Diff. Input Threshold Voltage	-0.2		+0.2	Volts	-7V ≤ V_{CM} ≤ +12V
Input Hysteresis		70		mV	V_{CM} = 0V
Output High Voltage	3.5			Volts	I_O = -4mA, V_{ID} = +200mV
Output Low Voltage			0.4	Volts	I_O = +4mA, V_{ID} = -200mV
Three-State (High Impedance) Output Current			±1	µA	V_{CC} = Max. 0.4V ≤ V_O ≤ 2.4V
Input Resistance	12			kΩ	-7V ≤ V_{CM} ≤ +12V
Short-circuit Current	7		85	mA	0V ≤ V_O ≤ V_{CC}
Receiver Data Rate			5	Mbps	
Receiver Input to Output	60	90	200	ns	R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pf
Receiver Input to Output	60	90	200	ns	*Figures 3 & 8*
Diff. Rcvr Skew $\lvert t_{PLH} - t_{PHL} \rvert$		13		ns	

SPECIFICATIONS (continued)

V_{CC} = 5V ± 5%, 0°C<T_A<70°C unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER					
Receiver Enable to Output Low		20	50	ns	C_{RL} = 15pF; *Fig. 2 & 9*; S_1 closed
Receiver Enable to Output High		20	50	ns	C_{RL} = 15pF; *Fig. 2 & 9*; S_2 closed
Receiver Disable from Low		20	50	ns	C_{RL} = 15pF; *Fig. 2 & 9*; S_1 closed
Receiver Disable from High		20	50	ns	C_{RL} = 15pF; *Fig. 2 & 9*; S_2 closed
POWER REQUIREMENTS					
Supply Voltage	+4.5		+5.5	Volts	V_{CC}
Supply Current					I_{CC}
SP485					
No load		500	900	µA	$\overline{RE}$, DI = 0V or V_{CC}; DE = 5V
		300	500	µA	$\overline{RE}$, DI = 0V or V_{CC}; DE = 0V
SP481					
No load		500	900	µA	$\overline{RE}$, DI = 0V or 5V; DE = 5V
		300	500	µA	$\overline{RE}$=0V, DI = 0V or 5V; DE = 0V
Shutdown Mode		0.1	10	µA	DE = 0V, $\overline{RE}$=V_{CC}
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (–C_)	0		+70	°C	
Industrial (–E_)	–40		+85	°C	
Storage Temperature	–65		+150	°C	
Package					
–CS, –ES	8–pin plastic DIP				
–CN, –EN	8–pin narrow body SOIC				

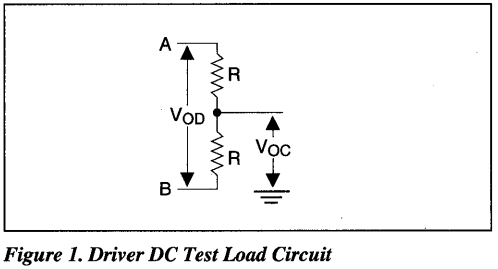


Figure 1. Driver DC Test Load Circuit

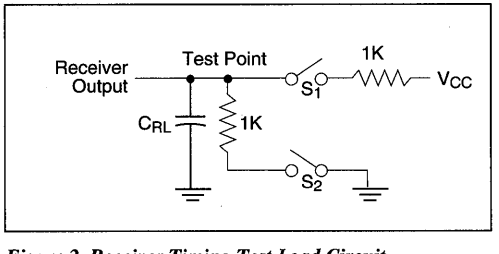


Figure 2. Receiver Timing Test Load Circuit

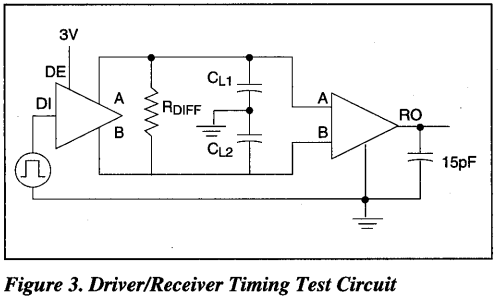


Figure 3. Driver/Receiver Timing Test Circuit

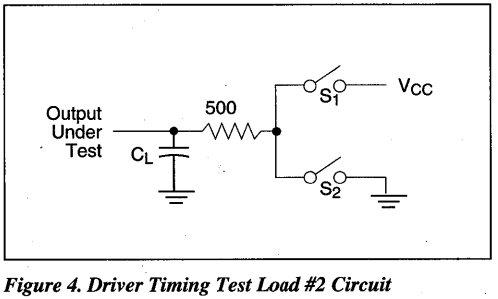


Figure 4. Driver Timing Test Load #2 Circuit

PIN FUNCTION...

PIN #	NAME	DESCRIPTION
1	RO	Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A>B by 200mV, RO will be high. If A<B by 200mV, then RO will be low.
2	$\overline{RE}$	Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.
3	DE	Driver Outputs Enable. A high on DE enables the driver output. A and B, and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver.
4	DI	Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.
5	GND	Ground Connection.
6	A	Driver Output/Receiver Input.
7	B	Driver Output/Receiver Input.
8	V_{cc}	Positive Supply; $4.75V < V_{cc} < 5.25V$

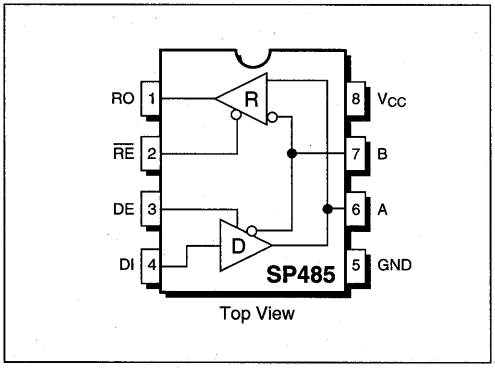


Figure 5. SP485/481 Pinout

FEATURES...

The **Sipex SP481** and **SP485** are half–duplex transceivers designed for RS485 and RS422 applications. BiCMOS design offers significant power savings over their bipolar counterparts without sacrificing ruggedness against overload of ESD damage or other performance parameters.

The **SP481** and **SP485** are pin–for–pin replacements for each other and the MAX481 and MAX485 products. The **SP485** has an operating current of only 300µA, making it ideal as a replacement for older bipolar products. The **SP481**features a shutdown mode that reduces standby operating current to less than 1µA maximum.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a current limiting circuit at the driver outputs. The receiver has a fail safe feature which guarantees a high output state when the inputs are left open.

The **SP481** and **SP485** are fully specified over the commercial temperature range.

SHUTDOWN MODE...

The SHUTDOWN mode is accessed simply by disabling both the DE and $\overline{RE}$ control lines simultaneously. In the SHUTDOWN mode, standby power dissipation is reduced to <1µA.

INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	LINE CONDITION	B	A
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

Table 1. Transmit Function Truth Table

INPUTS			OUTPUTS
$\overline{RE}$	DE	A - B	R
0	0	+0.2V	1
0	0	-0.2V	0
0	0	Inputs Open	1
1	0	X	Z

Table 2. Receive Function Truth Table

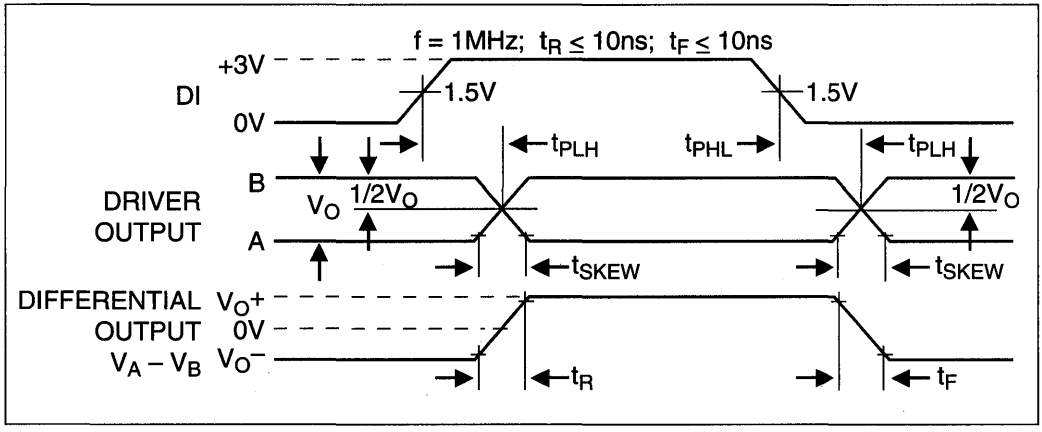


Figure 6. Driver Propagation Delays

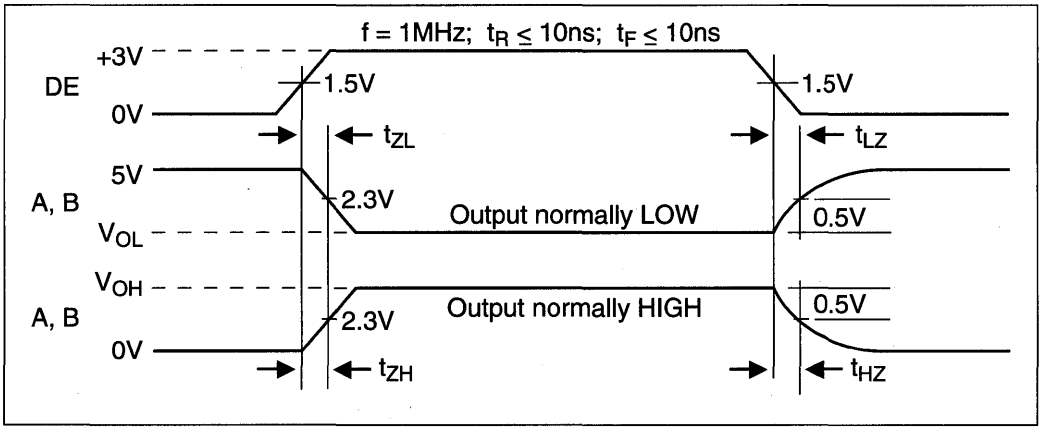


Figure 7. Driver Enable and Disable Times

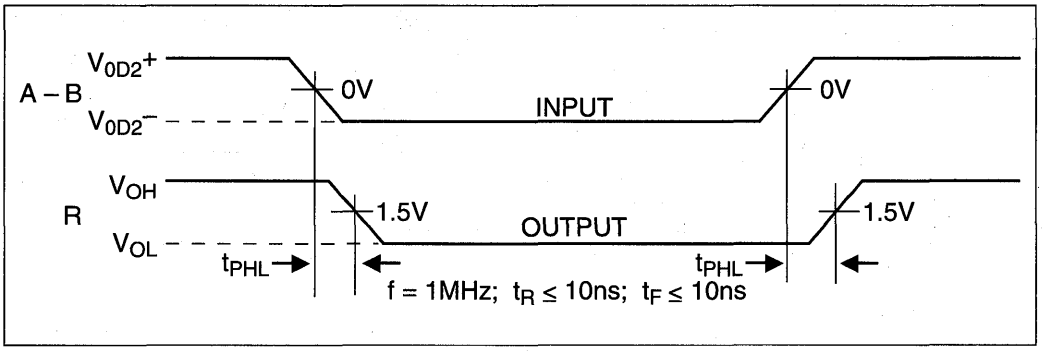


Figure 8. Receiver Propagation Delays

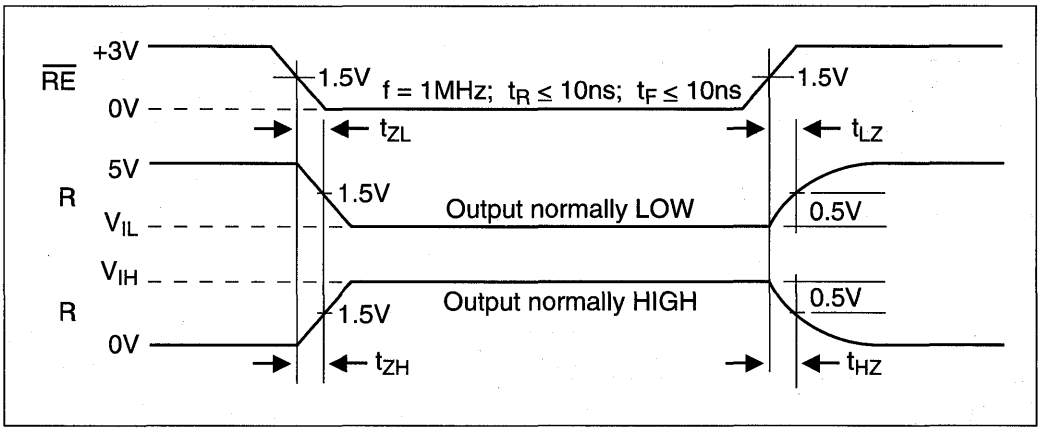


Figure 9. Receiver Enable and Disable Times

ORDERING INFORMATION

Model	Temperature Range	Package
SP481CN	0°C to +70°C	8-pin narrow SOIC
SP481CS	0°C to +70°C	8-pin Plastic DIP
SP485CN	0°C to +70°C	8-pin narrow SOIC
SP485CS	0°C to +70°C	8-pin Plastic DIP
SP481EN	-40°C to +85°C	8-pin narrow SOIC
SP481ES	-40°C to +85°C	8-pin Plastic DIP
SP485EN	-40°C to +85°C	8-pin narrow SOIC
SP485ES	-40°C to +85°C	8-pin Plastic DIP

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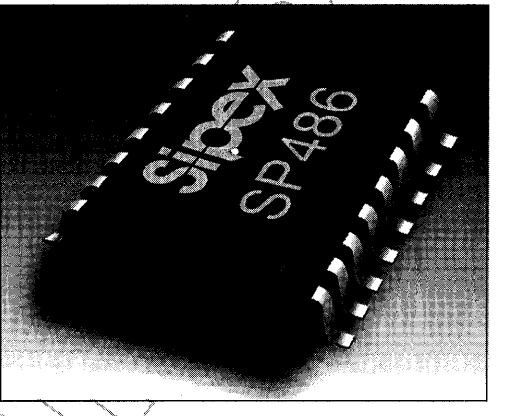
SP486 and SP487

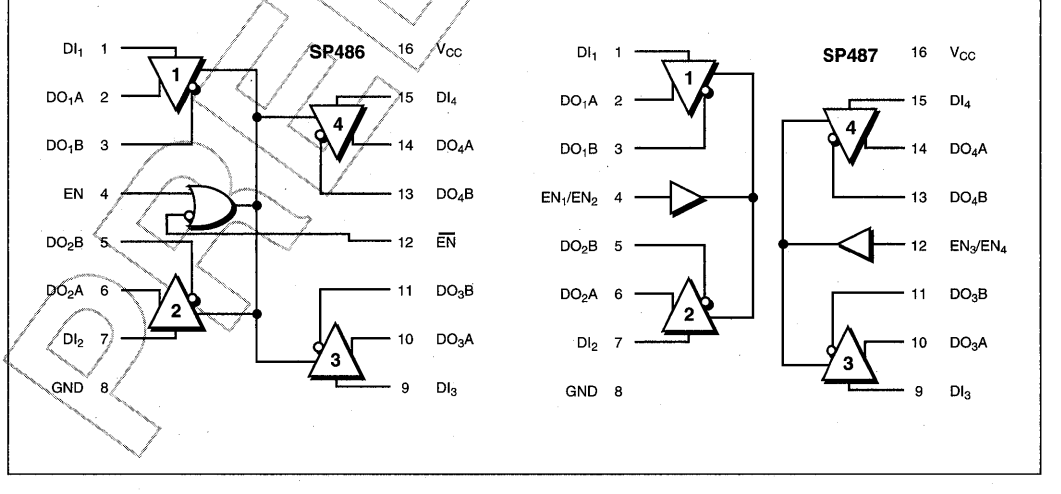
Quad RS485/422 Line Drivers

- RS485 or RS422 Applications
- Quad Differential Line Drivers
- Tri–state Output Control
- 40ns Typical Driver Propagation Delays
- 5ns Skew
- –7V to +12V Common Mode Output Range
- 100µA Supply Current
- Single +5V Supply Operation
- Pin Compatible with SN75172, SN75174, LTC486 and LTC487



DESCRIPTION...

The **SP486** and **SP487** are low–power quad differential line drivers meeting RS485 and RS422 standards. The **SP486** features a common driver enable control; the **SP487** provides independent driver enable controls for each pair of drivers. Both feature tri–state outputs and wide common–mode input range. Both are available in 16–pin plastic DIP and SOIC packages.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

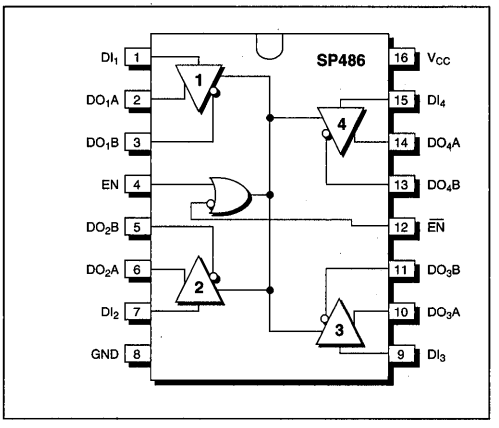
V_{CC} ..... +12V
Input Voltages
  Logic ..... –0.5V to (V_{CC} +0.5V)
  Drivers ..... –0.5V to (V_{CC} +0.5V)
Driver Output Voltage ..... ±14V
Input Currents
  Logic ..... ±25mA
  Driver ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Power Dissipation
  Plastic DIP 375mW
  (derate 7mW/°C above +70°C)
  Small Outline 375mW
  (derate 7mW/°C above +70°C)
Lead Temperature (soldering, 10 sec) ..... 300°C

SPECIFICATIONS

V_{CC} = 5V±5%; typicals at 25°C; $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS					
Digital Inputs					DI, EN, $\overline{EN}$, EN_1/EN_2, EN_3/EN_4
Voltage					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Input Current			±2	µA	
DRIVER OUTPUTS					
Differential Voltage			5	Volts	I_O = 0; unloaded
	2			Volts	R_L = 50 ohms (RS422)
	1.5	2	5	Volts	R_L = 27 ohms (RS485); *Fig. 1*
Change in Output Magnitude			0.2	Volts	for complementary output state
					R_L = 27 ohms or 50 ohms; *Fig. 1*
Common Mode Output Voltage		2.3	3	Volts	R_L = 27 ohms or 50 ohms; *Fig. 1*
Change in Common Mode Output Magnitude			0.2	Volts	for complementary output state
					R_L = 27 ohms or 50 ohms; *Fig. 1*
Driver Data Rate			5	Mbps	
Short–circuit Current					
V_{OH}			250	mA	–7V ≤V_O ≤ +12V
V_{OL}			250	mA	–7V ≤V_O ≤ +12V
High Impedance Output Current		±2	±200	µA	V_O = –7V to +12V
POWER REQUIREMENTS					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		100	200	µA	No load, output enabled
		100	200	µA	No load, output disabled
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
–C	0		+70	°C	
–E	–40		+85	°C	
Storage Temperature	–65		+150	°C	
Package					
–S	16–pin Plastic DIP				
–T	16–pin SOIC				

PINOUT — SP486



SP486 PINOUT

Pin 1 — DI_1 — Driver 1 Input — If Driver 1 output is enabled, logic 0 on DI_1 forces driver output DO_1A low and DO_1B high. A logic 1 on DI_1 with Driver 1 output enabled forces driver DO_1A high and DO_1B low.

Pin 2 — DO_1A — Driver 1 output A.

Pin 3 — DO_1B — Driver 1 output B.

Pin 4 — EN — Driver Output Enable. Please refer to SP486 *Truth Table (1).*

Pin 5 — DO2B — Driver 2 output B.

Pin 6 — DO_2A — Driver 2 output A.

Pin 7 — DI_2 — Driver 2 Input — If Driver 2 output is enabled, logic 0 on DI_2 forces driver output DO_2A low and DO_2B high. A logic 1 on DI_2 with Driver 2 output enabled forces driver DO_2A high and DO_2B low.

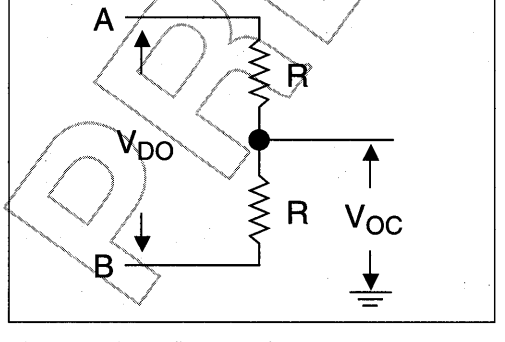


Figure 1. Driver DC Test Load

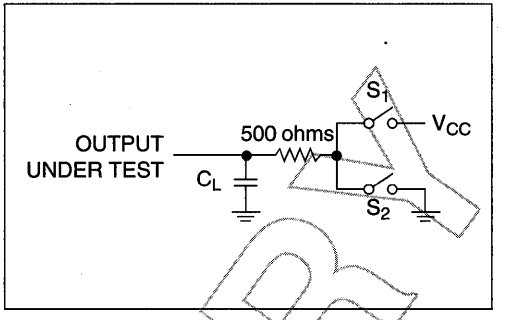


Figure 3. Driver Timing Test Load

Pin 8 — GND — DIgital Ground.

Pin 9 — DI_3 — Driver 3 Input — If Driver 3 output is enabled, logic 0 on DI_3 forces driver output DO_3A low and DO_3B high. A logic 1 on DI_3 with Driver 3 output enabled forces driver DO_3A high and DO_3B low.

Pin 10 — DO_3A — Driver 3 output A.

Pin 11 — DO_3B — Driver 3 output B.

Pin 12 — $\overline{EN}$ — Driver Output Disable. Please refer to SP486 *Truth Table (1).*

Pin 13 — DO_4B — Driver 4 output B.

Pin 14 — DO_4A — Driver 4 output A.

Pin 15 — DI_4 — Driver 4 Input — If Driver 4 output is enabled, logic 0 on DI_4 forces driver output DO_4A low and DO_4B high. A logic 1 on DI_4 with Driver 3 output enabled forces driver DO_4A high and DO_4B low.

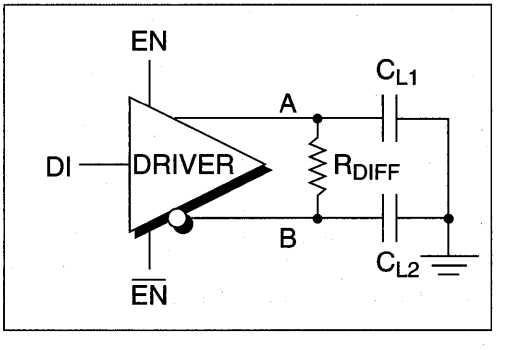
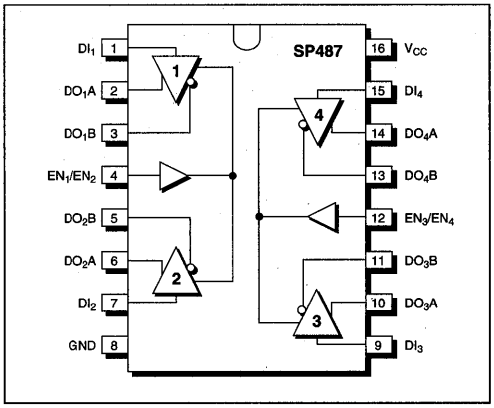


Figure 2. Driver Timing Test

PINOUT — SP487



Pin 16 — Supply Voltage V_{CC} — 4.75V ≤ V_{CC} ≤ 5.25V.

SP487 PINOUT

Pin 1 — DI_1 — Driver 1 Input — If Driver 1 output is enabled, logic 0 on DI_1 forces driver output DO_1A low and DO_1B high. A logic 1 on DI_1 with Driver 1 output enabled forces driver DO_1A high and DO_1B low.

Pin 2 — DO_1A — Driver 1 output A.

Pin 3 — DO_1B — Driver 1 output B.

Pin 4 — EN_1/EN_2 — Driver 1 and 2 Output Enable. Please refer to SP487 Truth Table (2).

Pin 5 — DO_2B — Driver 2 output B.

Pin 6 — DO_2A — Driver 2 output A.

Pin 7 — DI_2 — Driver 2 Input — If Driver 2 output is enabled, logic 0 on DI_2 forces driver output DO_2A low and DO_2B high. A logic 1 on DI_2 with Driver 2 output enabled forces driver DO_2A high and DO_2B low.

Pin 8 — GND — Digital Ground.

Pin 9 — DI_3 — Driver 3 Input — If Driver 3 output is enabled, logic 0 on DI_3 forces driver output DO_3A low and DO_3B high. A logic 1 on DI_3 with Driver 3 output enabled forces driver DO_3A high and DO_3B low.

Pin 10 — DO_3A — Driver 3 output A.

INPUT	ENABLES		OUTPUTS	
DI	EN	$\overline{EN}$	OUTA	OUTB
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Hi-Z	Hi-Z

Table 1. SP486 Truth Table

Pin 11 — DO_3B — Driver 3 output B.

Pin 12 — EN_3/EN_4 — Driver 3 and 4 Output Enable. Please refer to SP487 *Truth Table (2).*

Pin 13 — DO_4B — Driver 4 output B.

Pin 14 — DO_4A — Driver 4 output A.

Pin 15 — DI_4 — Driver 4 Input — If Driver 4 output is enabled, logic 0 on DI_4 forces driver output DO_4A low and DO_4B high. A logic 1 on DI_4 with Driver 3 output enabled forces driver DO_4A high and DO_4B low.

Pin 16 — Supply Voltage V_{CC} — 4.75V ≤ V_{CC} ≤ 5.25V.

FEATURES...

The **SP486** and **SP487** are low–power quad differential line drivers meeting RS485 and RS422 standards. The **SP486** features active high and active low common driver enable controls; the **SP487** provides independent, active high driver enable controls for each pair of drivers. The driver outputs are short–circuit limited to 200mA. Data rates up to 5Mbps are supported. Both are available in 16–pin plastic DIP and SOIC packages.

INPUT	ENABLES	OUTPUTS	
DI	EN1/EN2 or EN3/EN4	OUTA	OUTB
H	H	H	L
L	H	L	H
X	L	Hi-Z	Hi-Z

Table 2. SP487 Truth Table

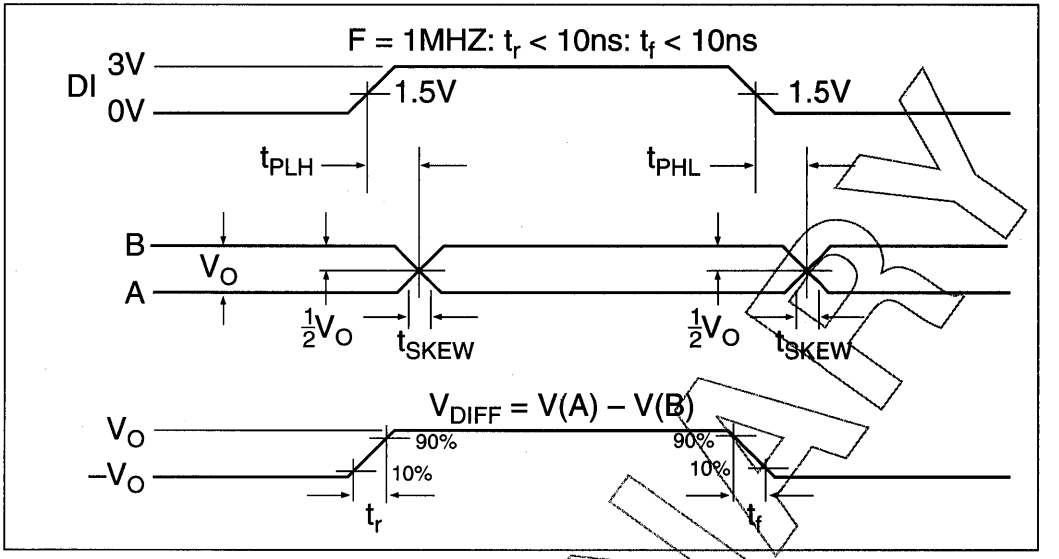


Figure 4. Driver Propagation Delays

AC PARAMETERS

V_{CC} = 5V±5%; typicals at 25°C; 0°C ≤ T_A ≤ +70°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PROPAGATION DELAY					
Driver Input to Output					R_{DIFF} = 54 ohms, C_{L1} = C_{L2} = 100pF; *Figure 2*
Low to High (t_{PLH})	20	40	60	ns	
High to Low (t_{PHL})	20	40	60	ns	
Driver Output to Output (t_{SKEW})		5	15	ns	
Driver Rise Time (t_R)					10% to 90%
SP486		20		ns	
SP487		20		ns	
Driver Fall Time (t_F)					90% to 10%
SP486		20		ns	
SP487		20		ns	
DRIVER ENABLE					
To Output High		35	70	ns	C_L = 100pF; *Figures 3 and 5* (S_2 closed)
To Output Low		44	75	ns	C_L = 100pF; *Figures 3 and 5* (S_1 closed)
DRIVER DISABLE					
From Output Low		55	92	ns	C_L = 15pF; *Figures 3 and 5* (S_1 closed)
From Output High		45	75	ns	C_L = 15pF; *Figures 3 and 5* (S_2 closed)

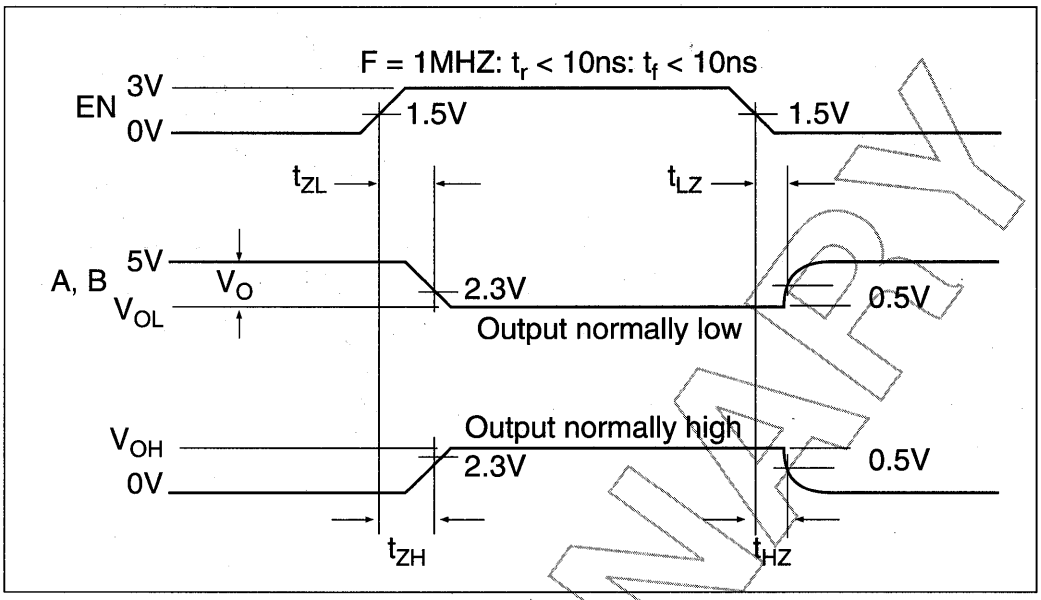


Figure 5. Driver Enable/Disable Timing

ORDERING INFORMATION

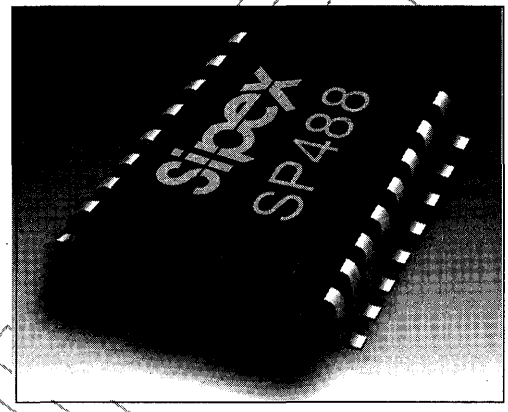
Quad RS485 Drivers:

Model	Enable/Disable	Temperature Range	Package
SP486CS	Common; active Low and Active High	0°C to +70°C	16–pin Plastic DIP
SP486CT	Common; active Low and Active High	0°C to +70°C	16–pin SOIC
SP486ES	Common; active Low and Active High	–40°C to +85°C	16–pin Plastic DIP
SP486ET	Common; active Low and Active High	–40°C to +85°C	16–pin SOIC
SP487CS	One per driver pair; active High	0°C to +70°C	16–pin Plastic DIP
SP487CT	One per driver pair; active High	0°C to +70°C	16–pin SOIC
SP487ES	One per driver pair; active High	–40°C to +85°C	16–pin Plastic DIP
SP487ET	One per driver pair; active High	–40°C to +85°C	16–pin SOIC

SP488 and SP489

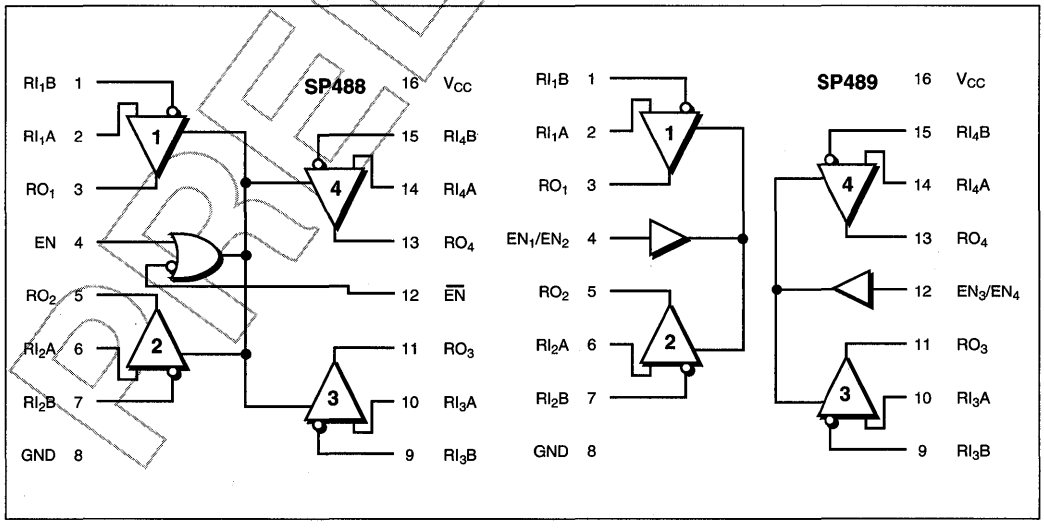
Quad RS485/422 Line Receivers

- RS485 or RS422 Applications
- Quad Differential Line Receivers
- Tri–state Output Control
- 120ns Typical Receiver Propagation Delays
- –7V to +12V Common Mode Input Range
- 1mA Supply Current
- Single +5V Supply Operation
- Pin Compatible with SN75173, SN75175, LTC488 and LTC489



DESCRIPTION...

The **SP488** and **SP489** are low–power quad differential line receivers meeting RS485 and RS422 standards. The **SP488** features a common receiver enable control; the **SP489** provides independent receiver enable controls for each pair of receivers. Both feature tri–state outputs and wide common–mode input range. The receivers have a fail–safe feature which forces a logic "1" output when receiver inputs are left floating. Both are available in 16–pin plastic DIP and SOIC packages.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +12V
Input Voltages
  Logic ..... –0.5V to (V_{CC} +0.5V)
  Receiver ..... ±14V
Receiver Output Voltage ..... –0.5V to (V_{CC} +0.5V)
Input Currents
  Logic ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Power Dissipation
  Plastic DIP 375mW
  (derate 7mW/°C above +70°C)
  Small Outline 375mW
  (derate 7mW/°C above +70°C)
Lead Temperature (soldering, 10 sec) ..... 300°C

SPECIFICATIONS

V_{CC} = 5V±5%; typicals at 25°C; $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS					
Digital Inputs					EN, $\overline{EN}$, EN_1/EN_2, EN_3/EN_4
Voltage					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Input Current			±2	µA	I_{IN1}
RECEIVER INPUTS					
Input Resistance	12			Kohm	$-7V \le V_{CM} \le 12V$
Differential Input Threshold	–0.2		±0.2	Volts	$-7V \le V_{CM} \le 12V$
Input Current (A, B)					V_{CC} = 0V or 5.25V; I_{IN2}
			+1.0	mA	V_{IN} = +12V
			–0.8	mA	V_{IN} = –7V
Receiver Data Rate			5	Mbps	
RECEIVER OUTPUTS					
Output Voltage					
V_{OH}	3.5			V	I_O = –4mA; V_{ID} = +0.2V
V_{OL}			0.4	V	I_O = +4mA; V_{ID} = –0.2V
High Impedance Output Current			±1	µA	V_{CC} = maximum; $0.4V \le V_O \le 2.4V$
POWER REQUIREMENTS					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		1		mA	No load
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
–C	0		+70	°C	
–E	–40		+85	°C	
Storage Temperature	–65		+150	°C	
Package					
–_S	16–pin Plastic DIP				
–_T	16–pin SOIC				

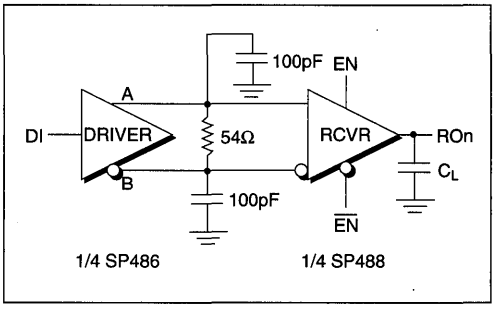


Figure 1. Timing Test Circuit

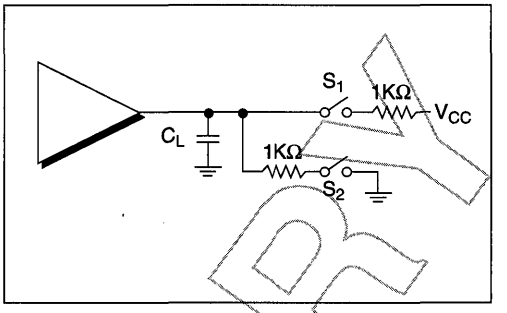


Figure 2. Enable/Disable Timing Test Circuit

SP488 PINOUT

Pin 1 — RI_1B — Receiver 1 input B.

Pin 2 — RI_1A _ Receiver 1 input A.

Pin 3 — RO_1 — Receiver 1 Output — If Receiver 1 output is enabled, if $RI_1A > RI_1B$ by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if $RI_1A < RI_1B$ by 200mV, Receiver 1 output is low.

Pin 4 — EN — Receiver Output Enable. Please refer to SP488 *Truth Table (1).*

Pin 5 — RO_2 — Receiver 2 Output — If Receiver 2 output is enabled, if $RI_2A > RI_2B$ by 200mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if $RI_2A < RI_2B$ by 200mV, Receiver 2 output is low.

Pin 6 — RI_2A — Receiver 2 input A.

Pin 7 — RI_2B — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

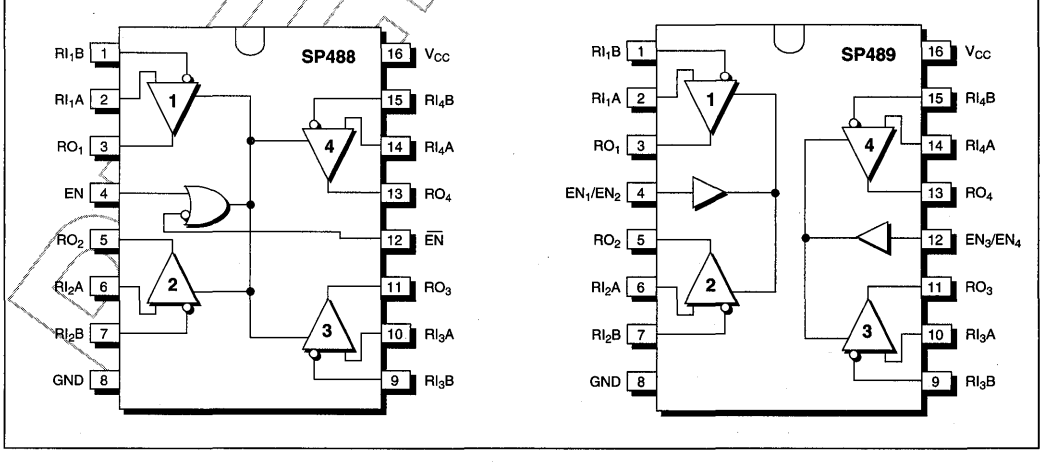
Pin 9 — RI_3B — Receiver 3 input B.

Pin 10 — RI_3A — Receiver 3 input A.

Pin 11 — RO_3 — Receiver 3 Output — If Receiver 3 output is enabled, if $RI_3A > RI_3B$ by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if $RI_3A < RI_3B$ by 200mV, Receiver 3 output is low.

Pin 12 — $\overline{EN}$ — Receiver Output Enable. Please refer to SP488 Truth Table (1).

PINOUT



Pin 13 — RO_4 — Receiver 4 Output — If Receiver 4 output is enabled, if $RI_4A > RI_4B$ by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if $RI_4A < RI_4B$ by 200mV, Receiver 4 output is low.

Pin 14 — RI_4A — Receiver 4 input A.

Pin 15 — RI_4B — Receiver 4 input B.

Pin 16 — Supply Voltage V_{CC} — 4.75V V_{CC} 5.25V.

SP489 PINOUT

Pin 1 — RI_1B — Receiver 1 input B.

Pin 2 — RI_1A — Receiver 1 input A.

Pin 3 — RO_1 — Receiver 1 Output — If Receiver 1 output is enabled, if $RI_{1A} > RI_1B$ by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if $RI_1A < RI_1B$ by 200mV, Receiver 1 output is low.

Pin 4 — EN1/EN2 — Receiver 1 and 2 Output Enable. Please refer to SP489 *Truth Table (2)*.

Pin 5 — RO_2 — Receiver 2 Output — If Receiver 2 output is enabled, if $RI_2A > RI_2B$ by 200mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if $RI_2A < RI_2B$ by 200mV, Receiver 2 output is low.

Pin 6 — RI_2A — Receiver 2 input A.

Pin 7 — RI_2B — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

DIFFERENTIAL	ENABLES		OUTPUT
A – B	EN	$\overline{EN}$	RO
V_{ID} 0.2V	H	X	H
	X	L	H
–0.2V < V_{ID} < +0.2V	H	X	?
	X	L	?
V_{ID} 0.2V	H	X	L
	X	L	L
X	L	H	Hi–Z

Table 1. SP488 Truth Table

Pin 9 — RI_3B — Receiver 3 input B.

Pin 10 — RI_3A — Receiver 3 input A.

Pin 11 — RO_3 — Receiver 3 Output — If Receiver 3 output is enabled, if $RI_3A > RI_3B$ by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if $RI_3A < RI_3B$ by 200mV, Receiver 3 output is low.

Pin 12 — EN3/EN4 — Receiver 3 and 4 Output Enable. Please refer to SP489 Truth Table (2).

Pin 13 — RO_4 — Receiver 4 Output — If Receiver 4 output is enabled, if $RI_4A > RI_4B$ by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if $RI_4A < RI_4B$ by 200mV, Receiver 4 output is low.

Pin 14 — RI_4A — Receiver 4 input A.

Pin 15 — RI_4B — Receiver 4 input B.

Pin 16 — Supply Voltage V_{CC} — 4.75V V_{CC} 5.25V.

FEATURES...

The **SP488** and **SP489** are low–power quad differential line receivers meeting RS485 and RS422 standards. The **SP488** features active high and active low common receiver enable controls; the SP489 provides independent, active high receiver enable controls for each pair of receivers. Both feature tri–state outputs and a –7V to +12V common–mode input range permitting a ±7V ground difference between devices on the communications bus. The **SP488/489** are equiped with a fail–safe feature which forces a logic high at the receiver output when the input is left floating. Data rates up to 5Mbps are supported. Both are available in 16–pin plastic DIP and SOIC packages.

DIFFERENTIAL	ENABLES	OUTPUT
A – B	EN_1/EN_2 or EN_3/EN_4	RO
V_{ID} 0.2V	H	H
–0.2V < V_{ID} < +0.2V	H	?
V_{ID} 0.2V	H	L
X	L	Hi–Z

Table 2. SP489 Truth Table

AC PARAMETERS

V_{CC} = 5V±5%; typicals at 25°C; 0°C ≤ T_A ≤ +70°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PROPAGATION DELAY					
Receiver Input to Output					C_L = 15pF; *Figure 1, 3*
Low to High (tPLH)		120		ns	
High to Low (tPH_L)		120		ns	
Differential Receiver Skew (t_{SKD})		13		ns	
Receiver Rise Time (t_R)					10% to 90%
SP488		20		ns	
SP489		20		ns	
Receiver Fall Time (tF)					90% to 10%
SP488		20		ns	
SP489		20		ns	
RECEIVER ENABLE					
To Output High		20		ns	C_L = 15pF; *Figures 2 and 4* (S2 closed)
To Output Low		20		ns	CL = 15pF; *Figures 2 and 4* (S1 closed)
RECEIVER DISABLE					
From Output Low		20		ns	CL = 15pF; *Figures 2 and 4* (S1 closed)
From Output High		20		ns	CL = 15pF; *Figures 2 and 4* (S2 closed)

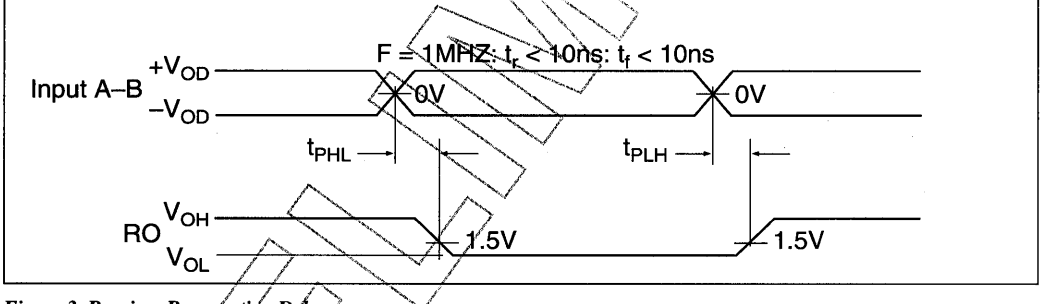


Figure 3. Receiver Propagation Delays

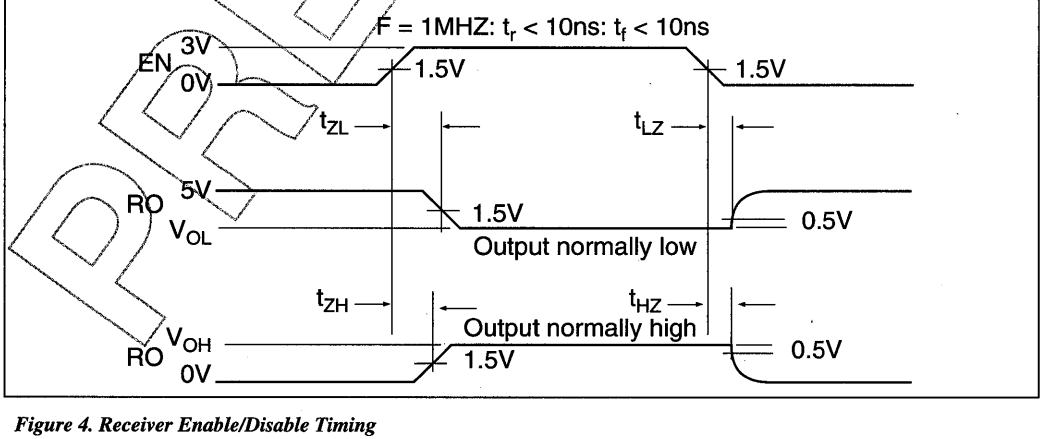


Figure 4. Receiver Enable/Disable Timing

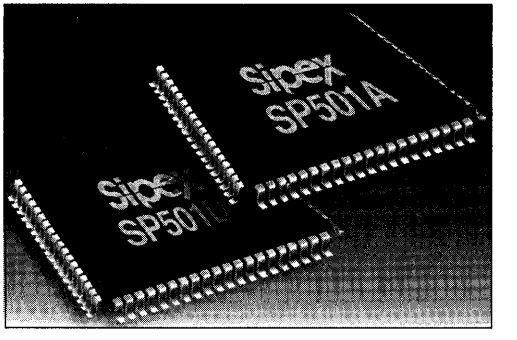
ORDERING INFORMATION

Quad RS485 Receivers:

Model	Enable/Disable	Temperature Range	Package
SP488CS	Common; active Low and Active High	0°C to +70°C	16–pin Plastic DIP
SP488CT	Common; active Low and Active High	0°C to +70°C	16–pin SOIC
SP488ES	Common; active Low and Active High	–40°C to +85°C	16–pin Plastic DIP
SP488ET	Common; active Low and Active High	–40°C to +85°C	16–pin SOIC
SP489CS	One per driver pair; active High	0°C to +70°C	16–pin Plastic DIP
SP489CT	One per driver pair; active High	0°C to +70°C	16–pin SOIC
SP489ES	One per driver pair; active High	–40°C to +85°C	16–pin Plastic DIP
SP489ET	One per driver pair; active High	–40°C to +85°C	16–pin SOIC

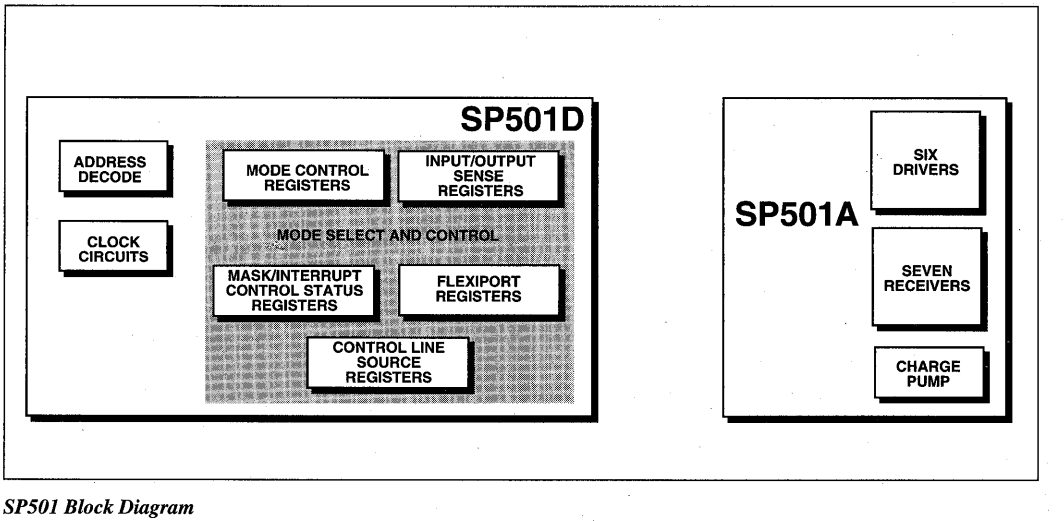
flexiPORT™ Multi–Mode Serial Transceiver

- Supports Industry Standard Software–Selectable Protocols:
  - RS232 (V.28)
  - RS422A (V.11, X.27)
  - RS423A (V.10, X.26)
  - RS449
  - RS485
  - V.35
  - MIL-STD-188C
  - MIL-STD-188-114A, Unbalanced
  - MIL-STD-188-114A, Balanced, Type II
  - EIA-562
  - EIA-530
- Six Outputs/Seven Inputs Provide Complete Communication Interface



DESCRIPTION...

The **SP501** provides programmable support for a variety of serial digital interface standards in two, 80–pin QFP packages. It features a host of operating modes including local and remote loopback modes, supports DTE and DCE transmit clock, multi–drop operation, maskable interrupt control line and status change detection. A **Sipex**–patented charge pump (5,306,954) internal to the **SP501** allows for +5V–only operation. The **SP501** can be used as a stand–alone multi–protocol interface, or with the **METACOMP** flexiPORT™ cabling system, which allows software determination of the protocol required for the equipment to which it is connected.



SP501 Block Diagram

ABSOLUTE MAXIMUM RATINGS

V_{CC} 6.5V
Receiver Inputs ..... ±25V
TTL Inputs ..... V_{CC} +0.3V; -0.3V

SPECIFICATIONS

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS/OUTPUTS					
DCD, RxC, RI, RxD, DSR, CTS, TxC, INT					
V_{OL}		0.4		Volts	I_{OUT} = 3.2mA
V_{OH}		3.5		Volts	I_{OUT} = -1.00mA
D_7 - D_0					
V_{OL}		0.4		Volts	I_{OUT} = 6.0mA
V_{OH}		3.5		Volts	I_{OUT} = -4.00mA
I_{OZ}		10.0		µA	V_{IH} or V_{IL}
I_L		1.0		µA	V_{CC} or GND
DRIVER OUTPUTS					
RS-485					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output(s)					
High Level Output			+6.0	Volts	
Low Level Output			-6.0	Volts	
Differential Output	±1.5		±5.0	Volts	R_L = 54Ω, C_L = 50pF
Open Circuit Voltage, V_O			±6.0	Volts	
Output Current	28			mA	R_L = 54Ω
Short Circuit Current			±250	mA	Terminated in -7V to +12V
Transition Time			120	ns	Rise/Fall time; 10–90%
Transmission Rate			2.5	Mbps	
V.35					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output(s)					
Differential Output		2.0		Volts	R_L = 100Ω; Note 4
Transition Time			40	ns	Rise/Fall time; 10–90%
Transmission Rate			2.5	Mbps	
MIL-STD-188C					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output(s)					
High Level Output	+5.0		+7.0	Volts	R_L = 6kΩ, V_{IN} = 0.8V
Low Level Output	-7.0		-5.0	Volts	R_L = 6kΩ, V_{IN} = 2.0V
Short Circuit Current			±250	mA	
Output Impedance			100	Ω	I_{OUT} ≥ 10mA
Transition Time			0.75	µs	Rise/Fall time; 10–90%
Transmission Rate			200	kbps	

SPECIFICATIONS (continued)

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS					
RS-422					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output(s)					
Differential Output	±2.0		±5.0	Volts	R_L = 100Ω, ≥ 50% V_O
Open Circuit Voltage,V_O			±6.0	Volts	
Balance			±0.4	Volts	V_T - V_T
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	
Transition Time			60	ns	Rise/Fall time; 10–90%
Transmission Rate			2.5	Mbps	
RS-423					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output(s)					
High Level Output	+3.6		+9.0	Volts	R_L = 450Ω (3 drivers)
Low Level Output	-9.0		-3.6	Volts	R_L = 450Ω (3 drivers)
Open Circuit Voltage,V_O	±4.0		±9.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	
Transition Time			40	ns	Rise/fall time, 10—90%
Transmission Rate			100	kbps	
RS-232E					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output(s)					
High Level Output	+5.0		+15.0	Volts	R_L = 3kΩ, V_{IN} = 0.8V
Low Level Output	-15.0		-5.0	Volts	R_L = 3kΩ, V_{IN} = 2.0V
Open Circuit Voltage,V_O	-15.0		+15.0	Volts	
Short Circuit Current			±100	mA	
Power Off Impedance	300			Ω	V_{CC} = 0V; V_O = ±2V
Slew Rate			30	V/µs	R_L = 3kΩ, C_L = 15pF
Transition Time			2	µs	Rise/Fall time; 10–90%
Transmission Rate			120	kbps	
EIA-562					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output(s)					
High Level Output	+3.7		+13.2	Volts	Stnd unit load*, V_{IN} = 0.8V
Low Level Output	-13.2		-3.7	Volts	Stnd unit load*, V_{IN} = 2.0V
Open Circuit Voltage,V_O	-13.2		+13.2	Volts	
Short Circuit Current			±60	mA	
Power Off Impedance	300			Ω	V_{CC} = 0V; V_O = ±2V
Slew Rate	4.0		30	V/µs	
Transition Time	0.22		3.1	µs	From -3.3V to +3.3V; stnd unit load
Transmission Rate			64.0	kbps	

*Standard unit loads: R_L = 3kΩ, C_L = 2,500 pF; 0 to 20kbps; R_L = 3kΩ, C_L = 1,000 pF; > 20kbps

SPECIFICATIONS (continued)

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
RS-485					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	(a) - (b)
Low Threshold	-7.0		-0.2	Volts	(a) - (b)
Common Mode Range	-7.0		+12.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			0.2	Volts	Note 3
Input Impedance	1			Unit load	Refer to graph
V.35					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	(a) - (b)
Low Threshold	-7.0		-0.2	Volts	(a) - (b)
Common Mode Range	-7.0		+12.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			0.2	Volts	Note 3
Input Impedance	1			Unit load	Note 4
MIL-STD-188C					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Input Current			+0.1	mA	At minimum 6kΩ input resistance
Low Input Current			-0.1	mA	At minimum 6kΩ input resistance
Input Impedance	6			kΩ	
RS-422					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+6.0	Volts	(a) - (b)
Low Threshold	-6.0		-0.2	Volts	(a) - (b)
Common Mode Range	-7.0		+7.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			kΩ	
RS-423					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+6.0	Volts	(a) - (b)
Low Threshold	-6.0		-0.2	Volts	(a) - (b)
Common Mode Range	-7.0		+7.0	Volts	
High Input Current					Refer to graph

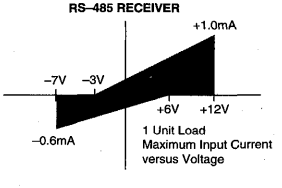
SPECIFICATIONS (continued)

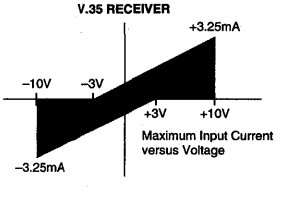
(Typical @ 25°C and nominal supply voltages unless otherwise noted)

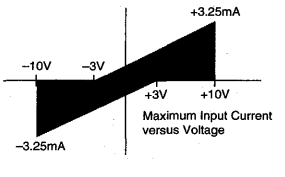
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
RS-423					
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			kΩ	
RS-232E					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+3.0		+15.0	Volts	
Low Threshold	-15.0		-3.0	Volts	
Receiver Open Circuit Bias	0		+2.0	Volts	
Input Impedance	3		7	kΩ	
EIA-562					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+3.0		+15.0	Volts	
Low Threshold	-15.0		-3.0	Volts	
Input Impedance	3		7	kΩ	Over -15V to +15V range
POWER REQUIREMENTS					
V_{CC}	4.5	5.0	5.5	Volts	
I_{CC}			30	mA	No load; all driver and TTL outputs
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		70	°C	Commercial
	-40		+85	°C	Industrial
Storage Temperature	-65		+150	°C	
Package					
SP501A and SP501D		80-pin QFP			

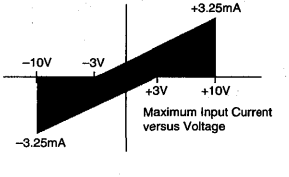
Notes:

1. Both V_{DD} and V_{SS} are generated internally by the on-chip charge pump and are not controlled by the user.
2. V_{SS} will be programmed to -5.0V in the RS423 mode, and -10.0V in all other operating modes.
3. Over -7.0V to +12.0V common mode range
4. The termination network shown in the *Typical Operating Circuit* must be implemented when the **SP501** is to be used with V.35. With the termination network in place, V_{OL} and V_{OH} levels will be 0.55V ±20% with a 100Ω load.

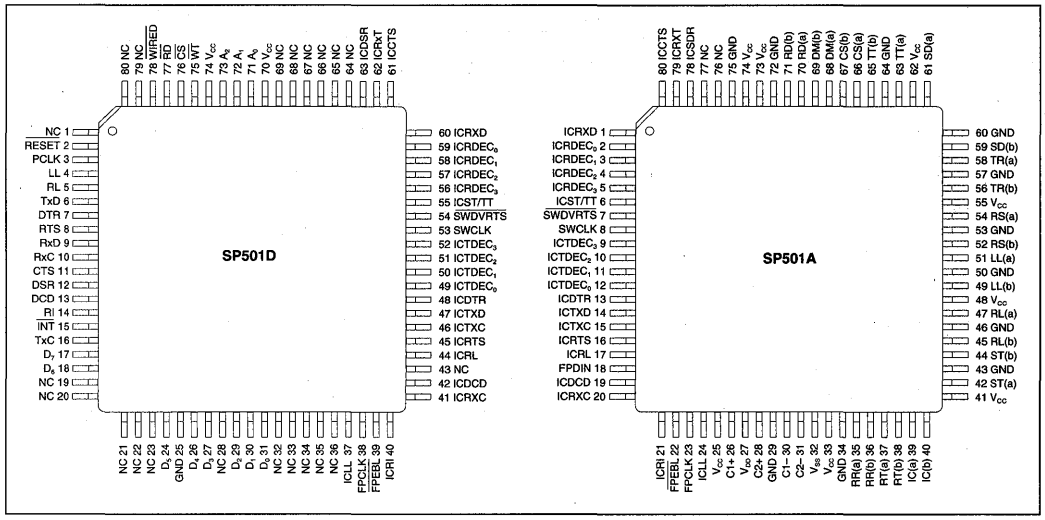








PIN ASSIGNMENTS



PIN DESCRIPTIONS

Please refer to other sections of this data sheet and to the separate **SP501** Technical Reference document to see how each of the paired signals described below are interconnected for each protocol. Only pins connected to external signals are described. Pins that provide interconnections between the **SP501A** and **SP501D** are not described, but should be connected per the *Typical Operating Circuit* diagram.

CLOCK AND DATA GROUP

TxD (Pin 6, SP501D) — TTL Input — Transmit Data; source for SD(a) and SD(b) outputs.

SD(a) (Pin 61, SP501A) — Analog Out — Send Data; inverted; sourced from TxD.

SD(b) (Pin 59, SP501A) — Analog Out — Send Data; non-inverted; sourced from TxD.

TxC (Pin 16, SP501D) — TTL — Transmit Clock; bi-directional; sourced to or from TT(a) and TT(b), bi-directional, or ST(a) and ST(b) [outputs only].

TT(a) (Pin 63, SP501A) — Analog In or Out — Terminal Timing, inverted; sourced to or from TxC output or input, respectively.

TT(b) (Pin 65, SP501A) — Analog In or Out — Terminal Timing, non-inverted; sourced to or from TxC output or input, respectively.

ST(a)/FPCLK (Pin 42, SP501A) — Analog Out — Send Timing, inverted; sourced from TxC; FPCLK Output supplies flexiPORT™ output configuration signal.

ST(b)/FPDIN (Pin 44, SP501A) — Analog In or Out — Send Timing Output, non-inverted; sourced from TxC; FPDIN inputs data from flexiPORT™ adapter.

RxD (Pin 9, SP501D) — TTL Output — Receive Data; sourced from RD(a) and RD(b) inputs.

RD(a) (Pin 70, SP501A) — Analog In — Receive Data, inverted; source for RxD.

RD(b) (Pin 71, SP501A) — Analog In — Receive Data, non-inverted; source for RxD.

RxC (Pin 10, SP501D) — TTL Output — Receive Clock; sourced from RT(a) and RT(b) inputs.

RT(a) (Pin 37, SP501A) — Analog In — Receive

Timing, inverted; source for RxC.

RT(b) (Pin 38, SP501A) — Analog In — Receive Timing, non-inverted; source for RxC.

CONTROL LINE GROUP

RS, TR, RL, LL(a) and (b) are sourced from a TTL input pin or an internal register.

RTS (Pin 8, SP501D) — TTL Input — Request To Send; source for RS(a) and RS(b) outputs.

RS(a) (Pin 54, SP501A) — Analog Out — Request to Send, inverted; sourced from RTS.

RS(b) (Pin 52, SP501A) — Analog Out — Request to Send, non-inverted; sourced from RTS.

DTR (Pin 7, SP501D) — TTL Input — Data Terminal Ready; source for TR(a) and TR(b) outputs.

TR(a) (Pin 58, SP501A) — Analog Out — Terminal Ready, inverted; sourced from DTR.

TR(b) (Pin 56, SP501A) — Analog Out — Terminal Ready, non-inverted; sourced from DTR.

RL (Pin 5, SP501D) — TTL Input — Remote Loop-back; source for RL(a) and RL(b) outputs.

RL(a) (Pin 47, SP501A) — Analog Out — Remote Loopback, inverted; sourced from RL.

RL(b) (Pin 45, SP501A) — Analog Out — Remote Loopback, non-inverted; sourced from RL.

LL (Pin 4, SP501D) — TTL Input — Local Loopback; source for LL(a) and LL(b) outputs.

LL(a) (Pin 51, SP501A) — Analog Out — Local Loopback, inverted; sourced from LL.

LL(b) (Pin 49, SP501A) — Analog Out — Local Loop–back, non-inverted; sourced from LL.

CTS (Pin 11, SP501D) — TTL Output — Clear To Send; sourced from CS(a) and CS(b) inputs.

CS(a) (Pin 66, SP501A) — Analog In — Clear to Send, inverted; source for CTS.

CS(b) (Pin 67, SP501A) — Analog In — Clear to Send, non-inverted; source for CTS.

DSR (Pin 12, SP501D) — TTL Output — Data Set Ready; sourced from DM(a), DM(b) inputs.

DM(a) (Pin 68, SP501A) — Analog In — Data Mode, inverted; source for DSR.

DM(b) (Pin 69, SP501A) — Analog In — Data Mode, non-inverted; source for DSR.

DCD (Pin 13, SP501D) — TTL Output — Data Carrier Detect; sourced from RR(a) and RR(b) inputs.

RR(a) (Pin 35, SP501A) — Analog In — Receiver Ready, inverted; source for DCD.

RR(b) (Pin 36, SP501A) — Analog In — Receiver Ready, non-inverted; source for DCD.

RI (Pin 14, SP501D) — TTL Output — Ring In; sourced from IC(a) and IC(b) inputs.

IC(a) (Pin 39, SP501A) — Analog In — Incoming Call, inverted; source for RI.

IC(b) (Pin 40, SP501A) — Analog In — Incoming Call, non-inverted; source for RI.

MICROCESSOR INTERFACE

D_7-D_0 (Pins 17, 18, 24, 26, 27, 29, 30, 31; SP501D) — TTL — Data lines for RD/WT registers; Bi-directional.

A_0-A_3 (Pins 71, 72, 73, 74; SP501D) — TTL Input — Address lines for RD/WT registers.

$\overline{RD}$ (Pin 77, SP501D) — TTL Input — Read strobe, low true, with CS, reads data from registers.

$\overline{WT}$ (Pin 75, SP501D) — TTL Input — Write strobe, low true, with CS, writes data to registers.

$\overline{CS}$ (Pin 76, SP501D) — TTL Input — Chip Select enables registers for RD or WT operation. Low true.

$\overline{RESET}$ (Pin 2, SP501D) — TTL Input — Resets **SP501** to known configuration, with all outputs disabled and resets control line status change inter-

rupt. Low true.

$\overline{\text{INT}}$ (Pin 15, SP501D) — TTL Output — Interrupt request indicating control line status change. Low true.

PCLK (Pin 3, SP501D) — TTL Input — 1 MHz to 5 MHz clock input to drive internal logic.

$\overline{\text{WIRED}}$ (Pin 78, SP501D) — TTL Input — Selects internal registers or external control of Line Driver and Receiver operating modes.

POWER SUPPLIES

V_{CC} (Pin 70, SP501D; Pins 25, 33, 41, 48, 55, 62, 73, 74, SP501A) — + 5V — Operating voltage for all modes; all V_{CC} pins can be tied together on pc board; V_{CC} must be bypassed with a 22µF capacitor to ground.

DIGITAL GROUND (Pin 25, SP501D; Pins 29, 34, 43, 46, 53, 57, 60, 64, 72, 75, SP501A) — Voltage common for all circuitry.

V_{DD} (Pin 27, SP501A) — +10V Charge Storage Capacitor — External charge storage capacitor to V_{CC}. DO NOT APPLY VOLTAGE TO THIS PIN.

V_{SS} (Pin 32, SP501A) — –10V Charge Storage Capacitor — External charge storage capacitor to ground. DO NOT APPLY VOLTAGE TO THIS PIN.

C_1^+ and C_1^- (Pins 26 and 30, SP501A) — Pins for floating capacitor for charge pump power supplies. Capacitor values of 22µF will provide proper operation.

C_2^+ and C_2^- (Pins 28 and 31, SP501A) — Pins for floating capacitor for charge pump power supplies. Capacitor values of 22µF will provide proper operation.

FEATURES...

The **SP501** is a highly integrated monolithic line transceiver and controller that provides programmable support for a variety of serial digital interface standards. The **SP501** can be integrated into systems as a stand-alone multi-protocol[1] interface, or can be used with the **METACOMP** flexiPORT™† cable system as a complete multi-protocol interface system. When used with the **METACOMP** flexi-Port™ cabling system, the **SP501** can determine the type of interface to which it is connected, and can be programmatically configured to transmit and receive in the appropriate protocol. The ability to both support multiple interface protocols and to determine the protocol required by the equipment that is connected to it, eliminates the manual setting of jumpers and switches, and the potential damage that results from errors in improperly configuring the communications port. Because the **SP501** integrates all the necessary circuitry to support multiple protocols, with no external jumpers or switches, all of the protocols can often be implemented in less space than a single RS232 interface.

Each of the line driver elements can output signals which conform with three different electrical voltage level specifications: RS-232, RS-422/RS-485, and RS-423. Using these three modes, the **SP501** supports each of the protocols listed in the Features list on the first page of this data sheet, as well as others which are equivalent. Different standards require various combinations of these outputs. For example, V.35 requires V.11 voltages on the transmit and receive clock and data lines, but all control lines are RS-232. Similarly, the RS-449 specification requires RS-422 voltages on clock and data, and most control lines, but RL and LL control lines are RS-423. The EIA-530 specification has the same RS-422 and RS-423 signal requirements as RS-449, but uses a DB-25 connector instead of the DB-37 required by RS-449. Thus selecting RS-449 protocol means selecting certain drivers as RS-422 outputs and others as RS-423. Programming the **SP501** to one of the interface standards (i.e. EIA 562, RS449, etc) will automatically select the correct underlying standards as required for each pin.

The protocol and operating mode programming of the **SP501** is done via a set of internal registers. The registers are equipped with data readback to allow the user to query the **SP501** and determine the current operating mode. Operating modes include normal communications using the selected protocol, local and remote loopback for local- or remote-initiated diagnostics and flexiPORT™ cable/connector interrogation. Additional features include the generation of an interrupt on mask–programmable status line state changes, selectable internal or external control of line drivers/receivers, and selectable inversion of the sense

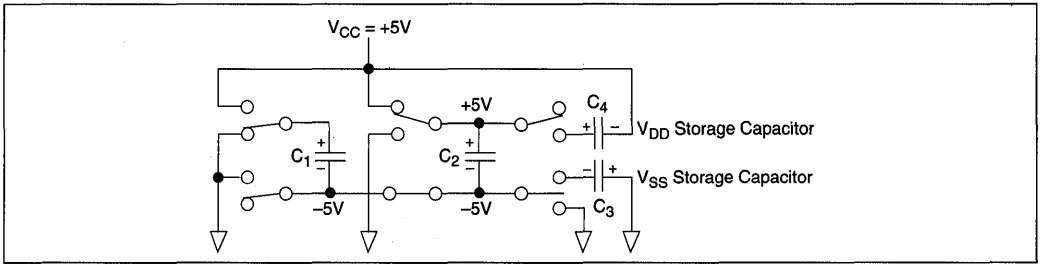


Figure 1. Charge Pump — Phase 1

of any individual output or input signal. The **SP501** also contains circuitry to detect unused or floating inputs as false.

The **SP501** is implemented as a two–chip, custom ASIC, incorporating mixed analog and digital processes. The two–chip set incorporates **SIPEX** line driver and receiver technology and **METACOMP** flexiPORT™ technology. The **SP501** provides a complete, totally integrated multi-protocol interface solution. The **SP501** is packaged in two 80-pin QFP packages. It requires a single +5V power supply; all internal positive and negative operating voltages are generated by a proprietary† internal charge pump circuit. Units are available for operation over the commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. Please consult the factory for product screened to MIL-STD-883C.

** flexiPORT™ is a proprietary, patent-pending technology of **METACOMP Inc.**, 10989 Via Frontera, San Diego, CA 92127. The **SP501** is a joint development effort between **METACOMP** and **SIPEX CORPORATION**. For the flexiPORT™ circuitry to determine the interface protocol, the remote equipment must be interconnected to the host serial port supported by the **SP501** with a flexiPORT™ "smart" adapter. The term flexiPort is a trademark of **METACOMP, Inc.**

† Patented (5,306,954)

‡ Strictly speaking, level 1 standards are not "protocols"; correctly used, the term refers to open systems interconnect (OSI) level 2 and higher standards. However, it has become common practice within the industry to apply the term "protocol" within the context of discussions regarding level 1 standards. When used in this data sheet, the terms "protocol" or "industry standard interface" are used interchangeably and should be taken to mean the OSI level 1, physical level, interface standards (e.g. EIA–530, V.35, etc.).

CHARGE–PUMP

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. *Figure 3a* shows the waveform found on the positive side of capcitor C_2, and *Figure 3b* shows the negative side of capcitor C_2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –10V to

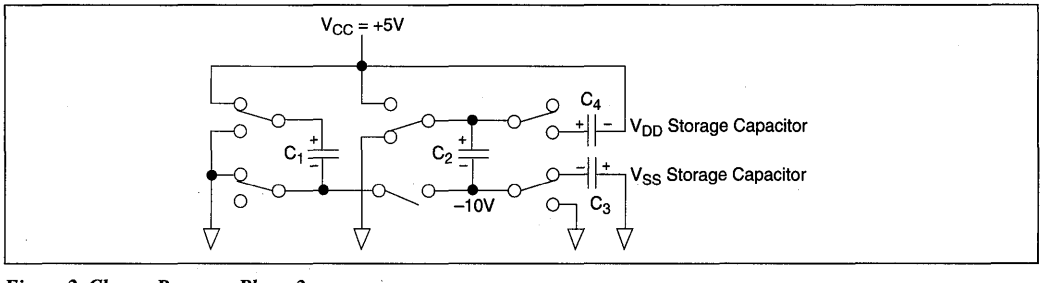


Figure 2. Charge Pump — Phase 2

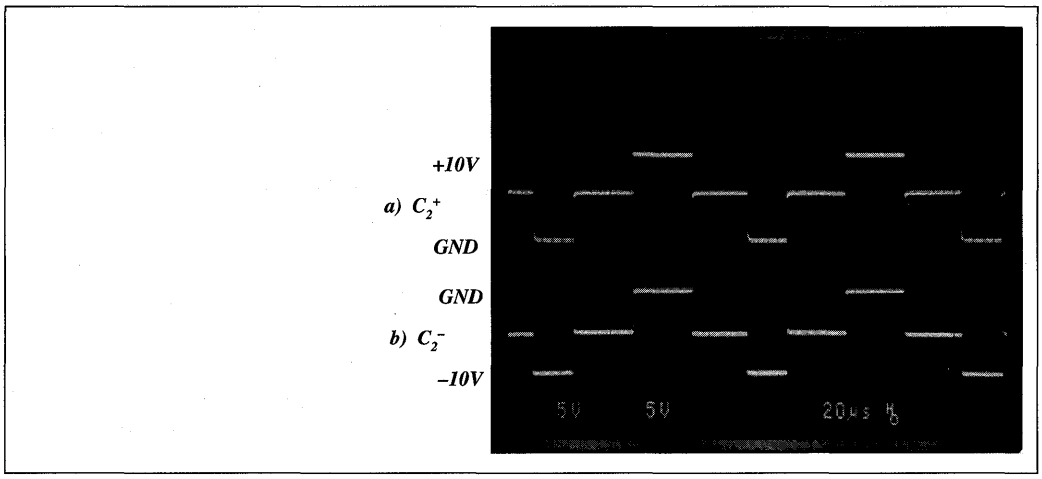


Figure 3. Charge Pump Waveforms

C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated 10V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC} in a no–load condition, V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 22µF with a 16V breakdown voltage rating. Two external Schottky diodes are required for high rate of rise power supplies, as shown in the Typical Operating Circuit elsewhere in this data sheet.

USING THE SP501... PROGRAMMING

Programming of the **SP501** is done via a group of 8-bit read/write registers, which allow for data readback and verification of current register status. The various control registers are addressed as shown in *Table 1, SP501 Register Address Map.*

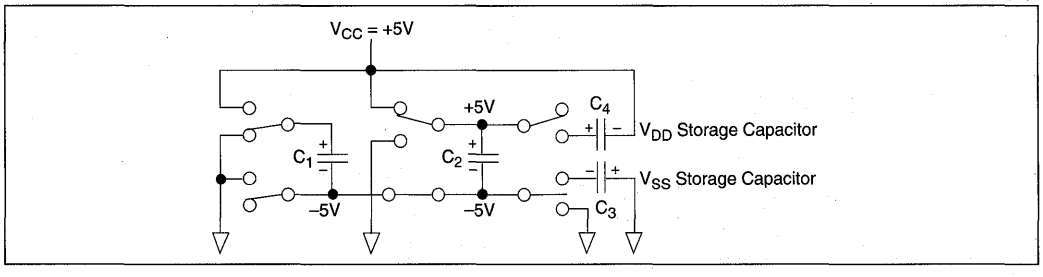


Figure 4. Charge Pump — Phase 3

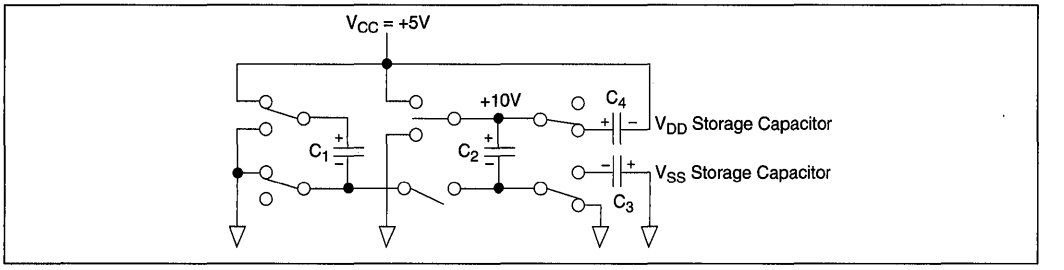


Figure 5. Charge Pump — Phase 4

Output Mode Register (R_0)

The **Output Mode Register** (R_0) is used to select the protocol to be used on all transmitted data as shown in *Table 2, Output Mode Register.* With this register addressed, data is written into the register to set the drivers to the selected protocol.

D_7 of the **Output Mode Register** selects CONTINUOUS or MULTIDROP mode within the selected protocol. If CONTINUOUS is set (D_7=1), the output drivers are always enabled. If MULTIDROP is set (D_7=0), the output drivers are enabled or tri-stated under the control of the DTR TTL input control line. The source of the DTR control line is determined by the Control Line Configuration Register (R_5), and is either the TTL input pin DTR, or Register 6. General output enable is controlled by the Interface Configuration Register (R_2).

The current state of the **Output Mode Register** can be read back at any time by the microprocessor. Bits D_6 - D_4 will be read back as undefined (as either 1's or 0's), and bits D_7 and D_3 - D_0 will reflect the current programmed state. It is important that *when the operating mode is changed, or the outputs are enabled (via R_2), the start of data transmission* ***must be delayed by one second to allow the internal charge pump to stabilize so***

REGISTER ADDRESS MAP		
ADDRESS	MODE	REGISTER
0	RD/WT	Register 0 - Output Mode Register
1	RD/WT	Input Mode Register
2	RD/WT	Configuration Register
3	RD	Receive Control Line Status Register
4	RD	Status Change Interrupt Cause Register
4	WT	Reset Interrupt Cause Register - Set Interrupt Mask
5	RD/WT	Control Line Configuration Register
6	RD/WT	DTR Control Register
7	RD/WT	RTS Control Register
8	RD/WT	RL Control Register
9	RD/WT	LL Control Register
A	WT	flexiPort Control Register
A	RD	flexiPort Status Register
B	—	Not Used
C	RD	flexiPort Data Register
D	RD/WT	Output Sense Register
E	RD/WT	Input Sense Register
F	—	Not Used

Table 1. SP501 Register Address Map

R_0 — OUTPUT MODE REGISTER (RD/WT)			
D_7	D_6 D_5 D_4	D_3 — D_0	PROTOCOL
If =0, Multi–drop	N/A	0000	All outpus tri–stated
If = 1, Continuous			
		0001	MIL–STD–118C
		0010	RS–232
		0011	EIA–562
		0100	RS–422
		0101	RS–485
		0110	MIL–STD–188–114A (Balanced)
		0111	Not Used
		1000	RS–423
		1001	MIL–STD–188–114A (Unbalanced)
		1010	Not Used
		1011	Not Used
		1100	RS–449
		1101	EIA–530
		1110	V.35
		1111	Not Used

Table 2. R_0 Output Mode Register

that the full output voltage is available. Following a reset, all output drivers remain disabled until after R_0 has been programmed.

Input Mode Register (R_1)

The **Input Mode Register** (R_1) is used to select the protocol to be used on all received data as shown in *Table 3, Input Mode Register*. With this register addressed, 4-bit data is written into the register to set the receivers to the appropriate single-ended or differential configuration and threshold levels required by the selected protocol. In a manner similar to the **Output Mode Register**, the **SP501** takes care of programming the data, clock and control lines to the levels necessary for proper operation as the selected protocol interface.

Line receivers have three different configurations. Configuration 0 is suitable for receiving RS-232 signals. It is single-ended, with a comparator threshold between 1.0Vand 1.5V, so that a floating input signal always registers as false. Configuration 1 receivers are differential inputs, with a sufficent sensitivity, and narrow enough hysteresis window to detect V.35 signals. These also provide detection of floating signals as false. Configuration 2 is single-ended, with a comparator threshold near 0V for detecting lower-level incoming signals such as RS-423. Configuration 2 inputs are also biased so that they detect floating inputs as false. Like the **Output Mode Register** (R_0), RS-449, EIA 530 and V.35 modes indicate certain arrangements of line receivers set to configuration 0, 1, or 2.

Some users of RS-423 will use Configuration 2 referenced to local signal common.Others will choose to use the Configuration 1 differential input receivers and connect the (b) input lead to signal common at the driving point. This is done by programming the drivers to RS-423, and the receivers to RS-422.

The **Input Mode Register** may be read back at any time to determine it's current state. Bits D_7 - D_4 are undefined, and bits D_3 - D_0 will reflect the current programmed states.

Interface Configuration Register (R_2)

The **Interface Configuration Register** (R_2) is a register that enables the driver outputs, and controls the normal, local and remote loop–back modes, and the direction and interconnection of the TxC, TT(a), TT(b), ST(a) and ST(b) pins. Please refer to the separate **SP501** Technical Reference document for a diagram of the actual

R_1 — INPUT MODE REGISTER (RD/WT)		
D_7 D_6 D_5 D_4	D_3 — D_0	PROTOCOL
N/A	0000	Disables receivers; all receiver outputs are undefined
	0001	MIL–STD–118C
	0010	RS–232
	0011	EIA–562
	0100	RS–422
	0101	RS–485
	0110	MIL–STD–188–114A (Balanced)
	0111	Not Used
	1000	RS–423
	1001	MIL–STD–188–114A (Unbalanced)
	1010	Not Used
	1011	Not Used
	1100	RS–449
	1101	EIA–530
	1110	V.35
	1111	Not Used

Table 3. R_1 Input Mode Register

configuration of these pins for the various operating modes that affect them.

Both D_0 and D_1 control the loopback mode of the **SP501**. When set to 0, the NORMAL mode is selected; signals flow from the TTL pins to or from the Analog pins. When D_0 is programmed with a 1, LOCAL LOOPBACK mode is selected. The signals to be transmitted are fed back internally to the receiver side of the **SP501**, and the input pins normally connected to the receivers are disabled. The output signals continue to be transmitted in order to allow them to be observed with an oscilloscope for test purposes.

If D_1 is programmed with a 1, REMOTE LOOPBACK mode is selected. The signals received from the remote end of the link are fed back to the line driver side of the **SP501**, enabling diagnostics to be run from the far end of the link. The incoming signals can still be received locally. If both local and remote loopback are selected at the same time, both sides would be independently looped back.

If D_2 is programmed to 0, TxC is sourced from the TT(a) and TT(b) pins. If programmed to a 1, TxC is the source for the TT(a) and TT(b) pins or ST(a) and ST(b) pins, as controlled by Register A, bit D_0.

A reset clears all bits of R_2 and disables all outputs (D_3=0). Enabling the flexiPORT™ circuitry will also disable the driver outputs by resetting bit D_3; after flexiPORT™ operations are complete, R_2 must be written again to enable the driver outputs by setting D_3 =1. When either the Local or Remote Loopback mode is selected, TxD is connected to RxD, TxC is connected to RxC, RTS is connected to CTS, DTR is connected to DSR, LL is connected with RI and RL is connected to DCD.

Receive Control Line Status Register (R_3) [Read Only]

The **Receive Control Line Register** (R_3) (see *Table 5*) is a register that reads the current status of the incoming control lines. These control lines are also available on output pins for use by external circuitry. Reading a 1 in bits D_3–D_0 indicates a FALSE condition of the control line; a 0 indicates a TRUE condition.

Status Change Interrupt Cause and Reset Register (R_4) [Read Only]

The **SP501** has a Latched Status Holding Register and

R_2 - INTERFACE CONFIGURATION REGISTER [RD/WT]			
D_3	D_2**	D_1	D_0
0=Outputs Off	0=TxC In	0=Normal mode	0 = Normal mode
1=Outputs On	1=TxC Out	1=Remote Loopback	1 = Local Loopback
** with respect to the **SP501**; with D_2=0, TxC is an input to the **SP501**; with D_2=1, TxC is output from the **SP501**, coming from TT(a) and TT(b) or ST(a) and ST(b), depending on the configuration chosen.			

Table 4. R_2 Interface Configuration Register

circuitry to continuously compare the latched status with the current control line status. Should one or more of the control lines change state, it will, if it is so enabled by the Interrupt Mask Register, generate an interrupt to the host microprocessor.

The **Status Change Interrupt Cause and Reset Register** ($\mathbf{R_{4a}}$) (see *Table 6)* is a register that contains the present state of the RI, DCD, DSR and CTS control lines in bits D_7 -D_4 respectively, which are the same as R_3. Bits D_3 - D_0 contain bits set to 1 for each of these control lines that have changed state since their status was last latched into the Latched Status Holding Register due to a prior read operation to $\mathbf{R_{4a}}$. Whenever any bit in this register is set, the interrupt output line is asserted. Once a bit is set, it remains set until the $\mathbf{R_{4a}}$ register status is read, so that an interrupt is generated even if the control line returns to it's original status. Each bit is set independently so that all status line changes are stored. Reading a 1 in bits D_7–D_4, the present state status, indicates the applicable control line has changed state since the last read; a 0 means the control line has not changed state.

Interrupt Mask Register (R_{4b}) [WT]

When R_4 is written it enables each control line whose corresponding bit is set to 1 to generate an interrupt under the conditions described above.

Interrupts will only be generated in response to changes in the status of lines which have a 1 stored in their bit position, thus control line interrupts can be selectively enabled. The current control line status is stored into the Latched Status Holding Register whenever the interrupt is reset as a result of reading register $\mathbf{R_{4a}}$; thus the next interrupt will be generated by a control line change from the state at the time the **Interrupt Cause and Reset Register** was last read.

Control Line Source Register (R_5) [RD/WT]

The **Control Line Source Register** ($\mathbf{R_5}$) (see *Table 8*) is a register that independently determines the line driver source for each of the DTR, RTS, RL and LL control lines. Each can be selected to be received from either an internal register ($\mathbf{R_6}$ through $\mathbf{R_9}$, repectively) or the TTL level input pin from external circuitry.

Writing a 0 to D_0 programs the input source of the DTR Line Driver to be the DTR TTL input (pin 7, **SP501D**). Writing a 1 to D_0 programs the DTR Line Driver source to be $\mathbf{R_6}$, the **DTR Control Register**.

Writing a 0 to D_1 programs the input source of the RTS Line Driver to be the RTS TTL input (pin 8, **SP501D**). Writing a 1 to D_1 programs the RTS Line Driver source to be $\mathbf{R_7}$, the **RTS Control Register**.

Writing a 0 to D_2 programs the input source of the RL Line Driver to be the RL TTL input (pin 5, **SP501D**). Writing a 1 to D_2 programs the RL

R_3 - RECEIVE CONTROL LINE STATUS REGISTER [Read Only]			
D_3	D_2	D_1	D_0
RI	DCD	DSR	CTS

Table 5. R_3 Receive Control Line Status Register

R_{4a} - STATUS CHANGE INTERRUPT CAUSE AND RESET REGISTER [Read Only]							
PRESENT STATE				INTERRUPT CAUSE			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RI	DCD	DSR	CTS	RI	DCD	DSR	CTS

Table 6. R_{4a} Status Change Interrupt Cause and Reset Register

R_{4b} - INTERRUPT MASK REGISTER [WT]							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	RI	DCD	DSR	CTS

Table 7. R_{4b} Interrupt Mask Register

Line Driver source to be **R_8**, the **RL Control Register**.

Writing a 0 to D_3 programs the input source of the LL Line Driver to be the LL TTL input (pin 4, **SP501D**). Writing a 1 to D_3 programs the LL Line Driver source to be **R_9**, the **LL Control Register**.

DTR Control Register (R_6) [RD/WT]

When the DTR source is programmed as internal by **R_5**, writing a 0 to **R_6** outputs a DTR False, and writing a 1 outputs a DTR True, as reflected on the TR(a) and TR(b) pins. When **R_5** is programmed as EXTERNAL, this register has no effect.

This register may be read back at any time to determine it's current state. D_0 will reflect the current programmed state of the DTR control register.

RTS Control Register (R_7) [RD/WT]

When the RTS source is programmed as internal by **R_5**, writing a 0 to **R_7** outputs a RTS False, and writing a 1 outputs a RTS True as reflected on the RS(a) and RS(b) pins. When **R_5** is programmed as EXTERNAL, this register has no effect.

This register may be read back at any time to determine it's current state. D_0 will reflect the current programmed state of the RTS control register.

RL Control Register (R_8) [RD/WT]

When the RL source is programmed as internal by **R_5**, writing a 0 to **R_8** outputs a RL False, and writing a 1 outputs a RL True as reflected on the RL(a) and RL(b) pins. When **R_5** is programmed as EXTERNAL, this register has no effect.

This register may be read back at any time to determine it's current state. D_0 will reflect the current programmed state of the RL control register.

LL Control Register (R_9) [RD/WT]

When the LL source is programmed as internal by **R_5**, writing a 0 to **R_9** outputs a LL False, and writing a 1 outputs a LL True as reflected on the LL(a) and LL(b) pins. When **R_5** is programmed as EXTERNAL, this register has no effect.

This register may be read back at any time to determine it's current state. D_0 will reflect the current programmed state of the LL control register.

flexiPORT™ Control Register (R_A) [WT only]

flexiPORT™ is a **METACOMP** proprietary, patent-pending technique for determining the interface type of an attached interface adapter. Programming D_3 to a 1 enables the flexiPORT™ circuitry; a 0 disables it. Enabling the

R_5 - CONTROL LINE SOURCE REGISTER [RD/WT]			
D_3	D_2	D_1	D_0
LL	RL	RTS	DTR
	0 = EXTERNAL	1 = INTERNAL	

Table 8. R_5 Control Line Source Register

CONTROL REGISTERS [RD/WT]								
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R_6- DTR	N/A	N/A	N/A	N/A	N/A	N/A	N/A	DTR
R_7- RTS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	RTS
R_8- RL	N/A	N/A	N/A	N/A	N/A	N/A	N/A	RL
R_9- LL	N/A	N/A	N/A	N/A	N/A	N/A	N/A	LL

Table 9. R_{6-9} DTR, RTS, RL and LL Control Registers

flexiPORT™ circuitry clears the **Interface Configuration Register** ($\mathbf{R_2}$), bit D_3, which disables all line drivers except FPCLK. After flexiPORT™ operations are completed, the desired line driver and receiver types must be programmed and enabled by writing to $\mathbf{R_0}$, $\mathbf{R_1}$ and then $\mathbf{R_2}$. It is important to note that for normal operations, D_3 *must* be set to 0. For a complete description of how the flexiPORT™ control registers and associated circuitry function, please refer to the separate **SP501** Technical Reference document.

The **flexiPORT™ Control Register** D_0 is used to control TxC pin usage. If $D_0 = 0$, its reset state, pins TT(a) and TT(b) are used for TxC out or in, depending on the state of $\mathbf{R_2}$—D_2, which controls the direction of TxC. With D_0 of the **flexiPORT™ Control Register** ($\mathbf{R_A}$) set to 0, pins ST(a)/FPCLK and ST(b)/FPDIN are used for flexiPORT™ operations. If D_0 = 1, pins ST(a) and ST(b) are sourced from the TxC input. This permits easily conforming to standard RS-232 or EIA-530 pinouts for users not using flexiPORT™ adapters.

flexiPORT™ Status Register (R_A) [RD only]

Register $\mathbf{R_A}$ can be read at any time to determine the status of the flexiPORT™ operations (see *Table 11*). For a complete description of how the flexiPORT™ control registers and associated circuitry function, please refer to the separate **SP501** Technical Reference document.

flexiPORT™ Data Register (R_C) [RD only]

For a complete description of how the flexiPORT™ control registers and associated circuitry function, please refer to the separate **SP501** Technical Reference document.

Output Sense Register (R_D) [RD/WT]

Register $\mathbf{R_D}$ is used to change the sense of any output driver. This register is cleared by a RESET. Writing a 1 to any bit position reverses the output polarity of that signal. This and the following register are used mainly to conform to MIL-STD 188C, which has certain signals inverted in polarity from the RS-232 standards. This register may be read back at any time to determine it's current state. Bits D_7 and D_6 will be read back as undefined, and bits D_5 through D_0 will reflect the current programmed states.

Input Sense Register (R_E) [RD/WT]

Register $\mathbf{R_E}$ is used to change the sense of any input receiver. This register is cleared by a RESET. Writing a 1 to any bit position reverses the input polarity of that signal. This register may be read back at any time to determine it's current state. Bits D_7 and D_6 will be read back as undefined, and bits D_5 through D_0 will reflect the current programmed states.

R_A — FLEXIPORT™ CONTROL REGISTER [WT only]							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	flexiPort	Vcc	CLOCK	CLOCK
				ENABLE	OUT	OUT	PIN

Table 10. R_A flexi-Port™ Control Register

R_A — FLEXIPORT™ STATUS REGISTER [RD only]							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RDY	N/A	N/A	N/A	flexiPort	Vcc	CLOCK	CLOCK
				ENABLE	OUT	OUT	PIN

Table 11. R_A flexiPORT™ Status Register

R_C — FLEXIPORT™ DATA REGISTER [RD only]							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
8-BIT FLEXIPORT DATA							

Table 12. R_C flexiPORT™ Data Register

R_D — OUTPUT SENSE REGISTER [RD/WT]							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	TxC	TxD	LL	RL	RTS	DTR

Table 13. R_D Output Sense Register

R_E — INPUT SENSE REGISTER [RD/WT]							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	RxC	RxD	RI	DCD	DSR	CTS

Table 14. R_E Input Sense Register

RESET

The RESET control line clears all registers to the following state:

- Register R_0, D_7, $D_3 - D_0 = 0$
- Register R_1, $D_3 - D_0 = 0$
- Register R_2, $D_3 — D_0 = 0$
- Register R_3, $D_3 — D_0$ = Present Status
- Register R_{4a}, $D_7 — D_4$ = Present Status
  $D_3 — D_0 = 0$
- Register R_{4b}, $D_3 — D_0 = 0$
- Register R_5, $D_3 — D_0 = 0$
- Register R_6, $D_0 = 0$
- Register R_7, $D_0 = 0$
- Register R_8, $D_0 = 0$
- Register R_9, $D_0 = 0$
- Register R_A, $D_3 — D_0 = 0$

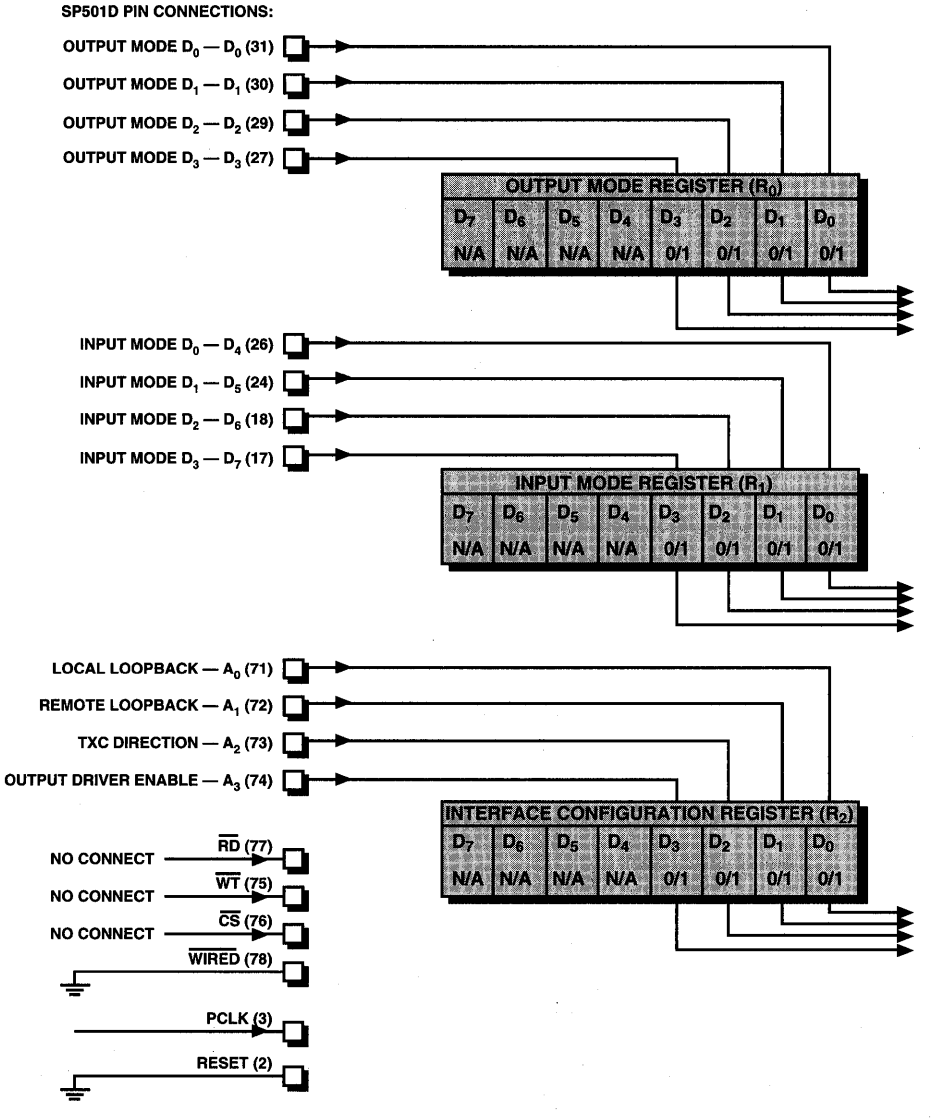
- Register R_C, $D_7 — D_0 = 0$
- Register R_D, $D_5 - D_0 = 0$
- Register R_E, $D_5 - D_0 = 0$

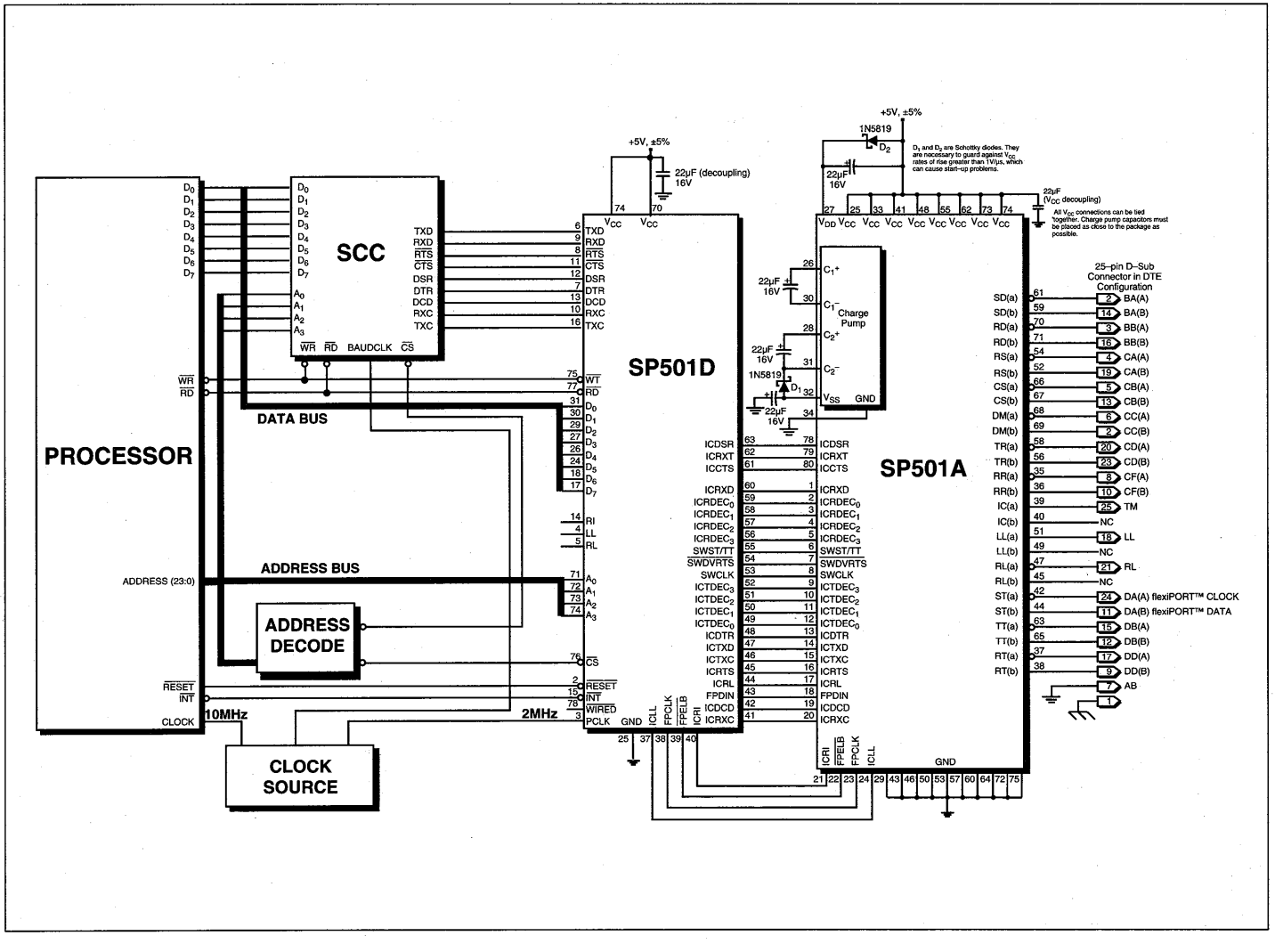
HARD-WIRED OPERATING MODE

In those applications not controlled by a microprocessor, the **SP501** has an operating mode whereby all controls can be provided via jumpers tied to logic "1" or "0". With pin 78 (**SP501D**) ($\overline{\text{WIRED}}$) tied low, the entire control register interface is replaced with direct access to the Line Driver and Receiver mode control bits. When controlled in this manner, each pin provides the functions as described below.

Input pins D_3-D_0 (27, 29–31; **SP501D**) supply the Output Driver control bits normally provided by the Output Mode Register (R_0) D_3-D_0. Input pins D_7-D_4 (17, 18, 24 and 26; **SP501D**) supply the Input Receiver control bits normally provided by the Input Register (R_1), D_3-D_0. The address bus inputs A_0-A_3 (pins 71–75, **SP501D**) provide the Interface Configuration Register (R_2) lines. A_0 (pin 71, **SP501D**) provides the LOCAL LOOPBACK function normally provided by R_2, D_0. A_1(pin 72, **SP501D**) provides the REMOTE LOOPBACK function normally provided by R_2, D_1. A_2 (pin 73, **SP501D**) provides the TxC clock direction function normally provided by R_2, D_2. The output driver tri-state function normally provided by R_2, D_3 is provided by A_3 (pin 74, **SP501D**).

HARD–WIRED CONTROL





OPERATING MODE BLOCK DIAGRAMS

The following pages describe the individual driver and receiver configurations for each operating mode of the **SP501**. User–specific programming, such as TxC direction or DTR signal source, are not shown specifically, but are indicated by control register bit and corresponding controlled switch positions.

The operating protocols that share comon configurations are grouped together. There are four groups of protocols:

Group 1 — RS232/RS423/EIA562/MIL–188C/MIL–114AUB
Group 2 — RS449/EIA530
Group 3 — RS422/RS485/MIL–114A–B–2
Group 4 — V.35

Separate drawings are shown for the CLOCK AND DATA LINES and the CONTROL LINES for each Group. In addition to the protocol groupings, the local and remote loopback operating modes are shown, as is the flexi–Port™ operating mode.

REGISTER OR SIGNAL:

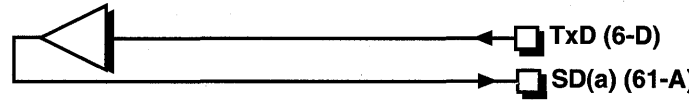
**Signal (Pin - A=SP501A
D=SP501D)**

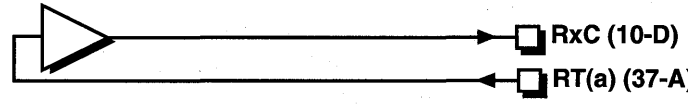
OUTPUT MODE REGISTER (R_0)

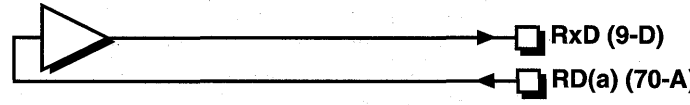
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	N/A	N/A	N/A	X	X	X	X

INPUT MODE REGISTER (R_1)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	X	X	X	X







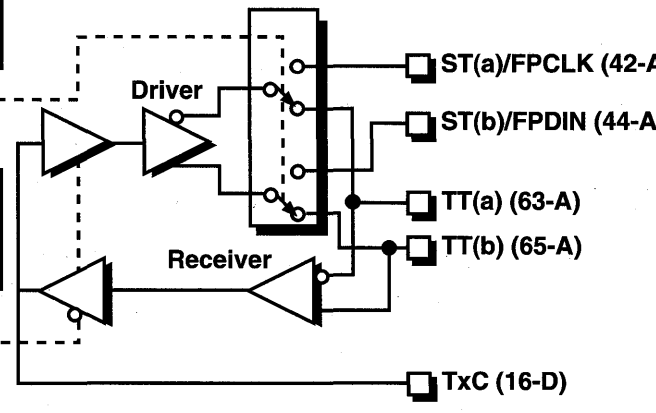
flexiPort CONTROL REGISTER (R_A)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				

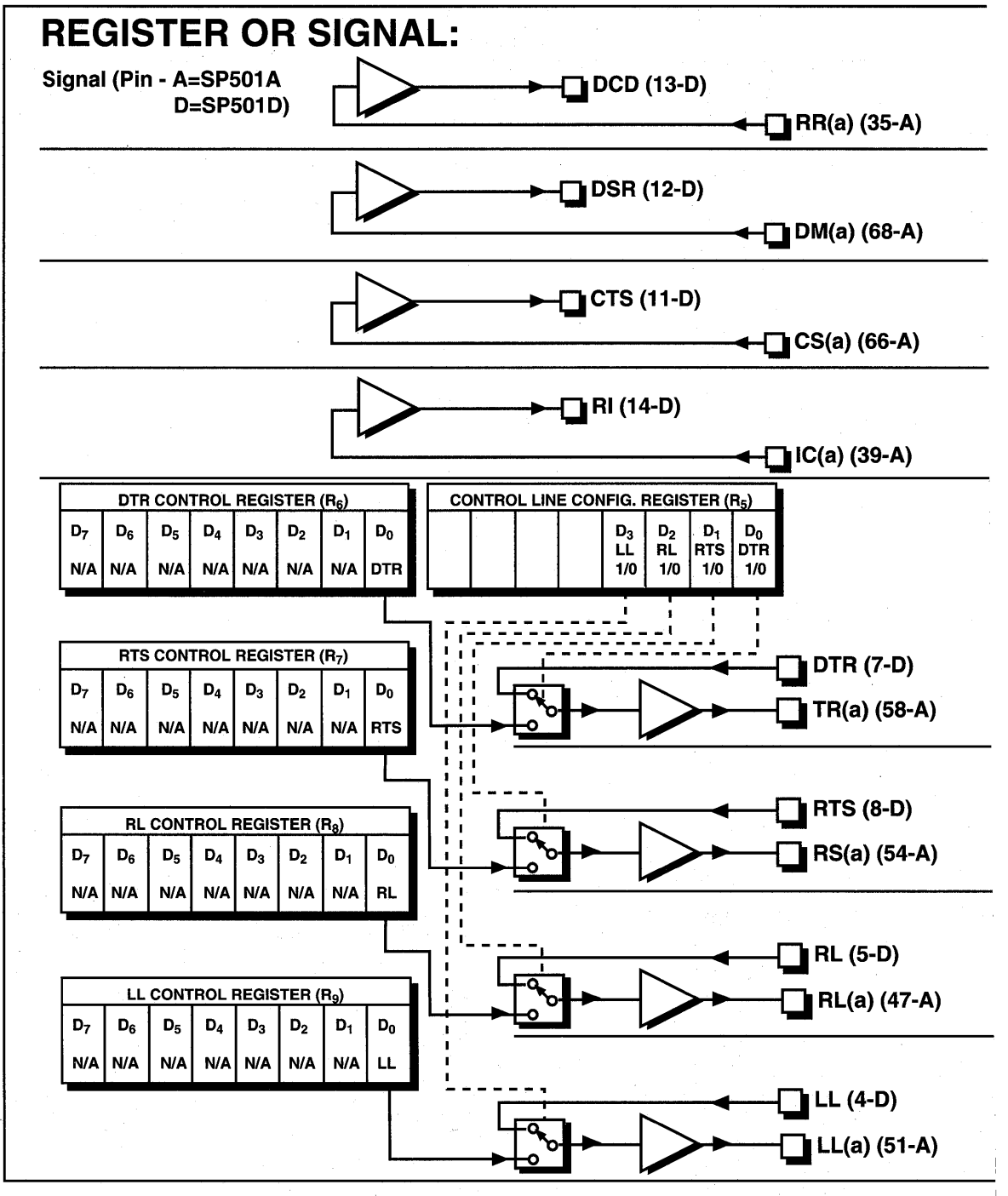
0 = TT
1 = ST

INTERFACE CONFIGURATION REGISTER (R_2)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				



PROTOCOL:				
RS-232E (V.28)	RS-423	EIA-562	MIL-188C	MIL-114AUB
82 1XXX 0010	88 1XXX 1000	83 1XXX 0010	81 1XXX 0001	89 1XXX 1001
02 XXXX 0010	08 XXXX 1000	03 XXXX 0010	01 XXXX 0001	09 XXXX 1001
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423


REGISTER OR SIGNAL:
Signal (Pin - A=SP501A
D=SP501D)
DCD (13-D)
RR(a) (35-A)
DSR (12-D)
DM(a) (68-A)
CTS (11-D)
CS(a) (66-A)
RI (14-D)
IC(a) (39-A)
DTR CONTROL REGISTER (R6)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 DTR
CONTROL LINE CONFIG. REGISTER (R5)
D3 LL 1/0
D2 RL 1/0
D1 RTS 1/0
D0 DTR 1/0
RTS CONTROL REGISTER (R7)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 RTS
DTR (7-D)
TR(a) (58-A)
RL CONTROL REGISTER (R8)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 RL
RTS (8-D)
RS(a) (54-A)
LL CONTROL REGISTER (R9)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 LL
RL (5-D)
RL(a) (47-A)
LL (4-D)
LL(a) (51-A)

PROTOCOL:				
RS-232E (V.28)	RS-423	EIA-562	MIL-188C	MIL-114AUB
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423
RS-232	RS-423	RS-232	RS-232	RS-423

REGISTER OR SIGNAL:

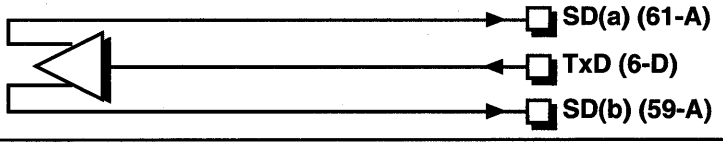
Signal (Pin - A=SP501A
D=SP501D)

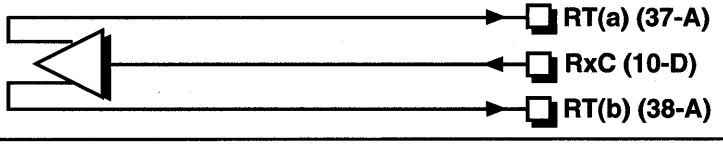
OUTPUT MODE REGISTER (R_0)

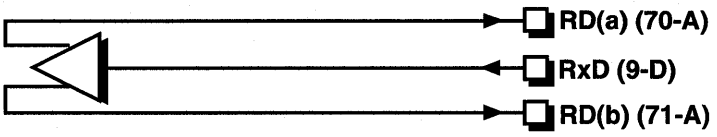
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	N/A	N/A	N/A	X	X	X	X

INPUT MODE REGISTER (R_1)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	X	X	X	X







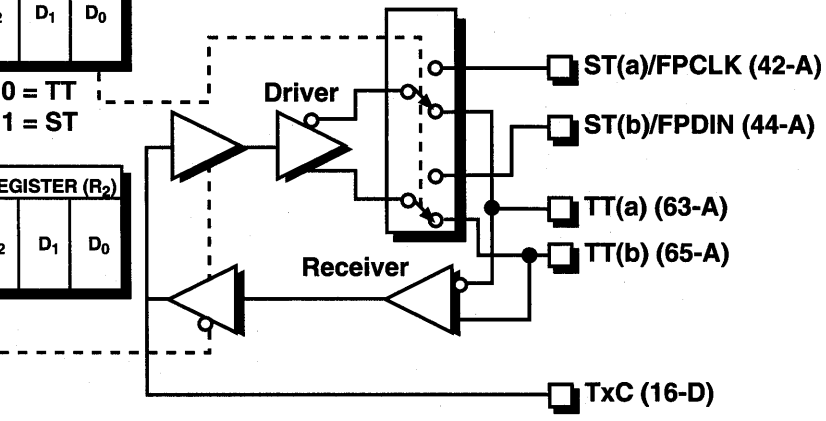
flexiPort CONTROL REGISTER (R_A)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				

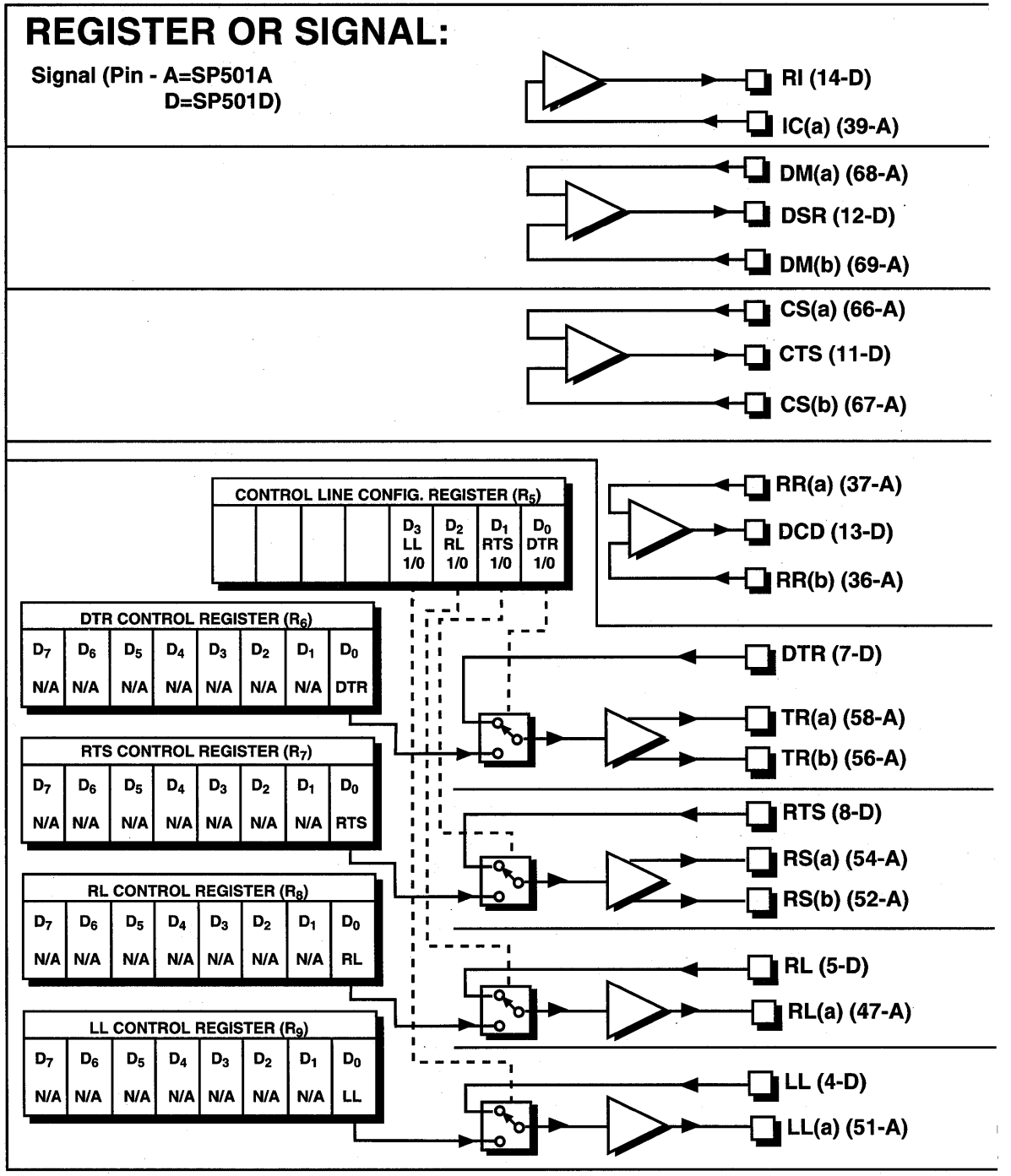
0 = TT
1 = ST

INTERFACE CONFIGURATION REGISTER (R_2)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				



PROTOCOL:	
RS-449	EIA-530
8C 1XXX 1100	8D 1XXX 1101
0C XXXX 1100	0D XXXX 1101
RS-422	RS-422
RS-422	RS-422
RS-422	RS-422
RS-422	RS-422


REGISTER OR SIGNAL:
Signal (Pin - A=SP501A
D=SP501D)
RI (14-D)
IC(a) (39-A)
DM(a) (68-A)
DSR (12-D)
DM(b) (69-A)
CS(a) (66-A)
CTS (11-D)
CS(b) (67-A)
CONTROL LINE CONFIG. REGISTER (R5)
D3 LL 1/0
D2 RL 1/0
D1 RTS 1/0
D0 DTR 1/0
RR(a) (37-A)
DCD (13-D)
RR(b) (36-A)
DTR CONTROL REGISTER (R6)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 DTR
DTR (7-D)
TR(a) (58-A)
TR(b) (56-A)
RTS CONTROL REGISTER (R7)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 RTS
RTS (8-D)
RS(a) (54-A)
RS(b) (52-A)
RL CONTROL REGISTER (R8)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 RL
RL (5-D)
RL(a) (47-A)
LL CONTROL REGISTER (R9)
D7 N/A
D6 N/A
D5 N/A
D4 N/A
D3 N/A
D2 N/A
D1 N/A
D0 LL
LL (4-D)
LL(a) (51-A)

PROTOCOL:	
RS-449	EIA-530
RS-423	RS-423
RS-422	RS-422
RS-422	RS-422
RS-422	RS-422
RS-422	RS-422
RS-422	RS-422
RS-423	RS-423
RS-423	RS-423

REGISTER OR SIGNAL:

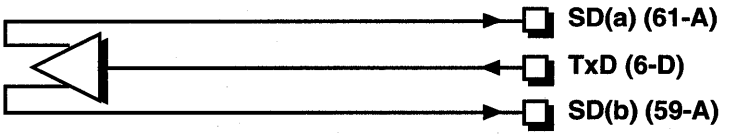
Signal (Pin - A=SP501A
D=SP501D)

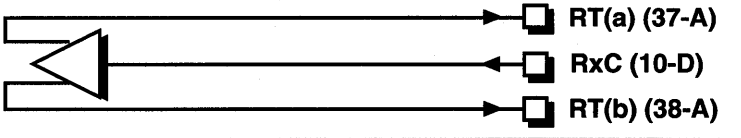
OUTPUT MODE REGISTER (R_0)

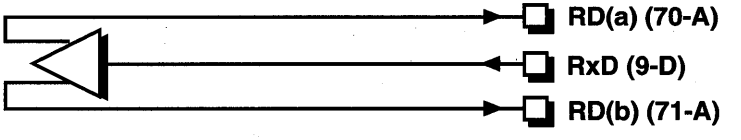
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	N/A	N/A	N/A	X	X	X	X

INPUT MODE REGISTER (R_1)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	X	X	X	X







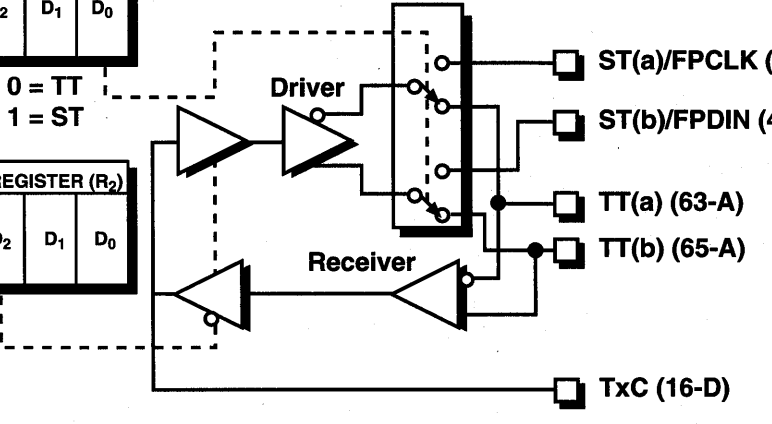
flexiPort CONTROL REGISTER (R_A)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				

0 = TT
1 = ST

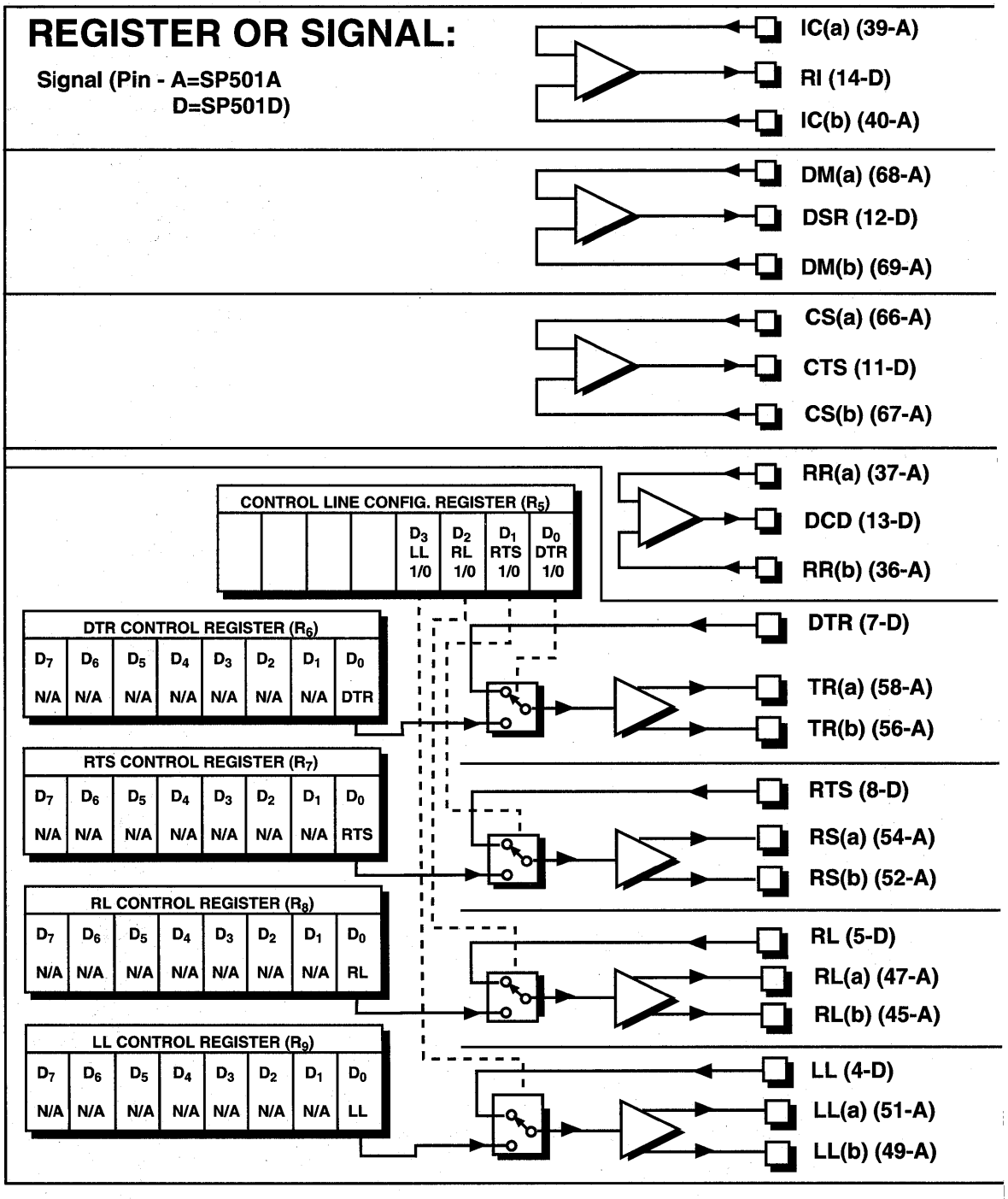
INTERFACE CONFIGURATION REGISTER (R_2)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				



PROTOCOL:		
RS-422 (V.11, V.27)	RS-485	MIL-114A-B-2
84 1XXX 0100	85** 1XXX 0101	86 1XXX 0110
04 XXXX 0100	05 XXXX 0101	06 XXXX 0110
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422 **RS-485 protocol often operates in a multi-drop mode; in this case R_0 would be 05, not 85	RS-422 TT(a) (76)/ST(a) (55) only

CONTROL LINE CONFIGURATION — GROUP 3
RS–422, RS–485 AND MIL–STD–188–114A BALANCED PROTOCOLS



PROTOCOL:		
RS-422 (V.11, V.27)	RS-485	MIL-114A-B-2
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422
RS-422	RS-422	RS-422

REGISTER OR SIGNAL:

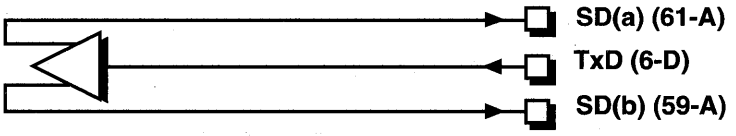
Signal (Pin - A=SP501A
D=SP501D)

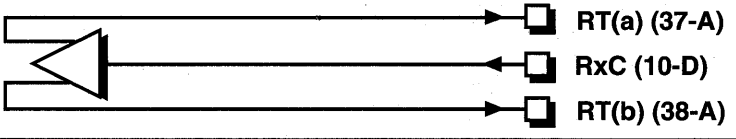
OUTPUT MODE REGISTER (R_0)

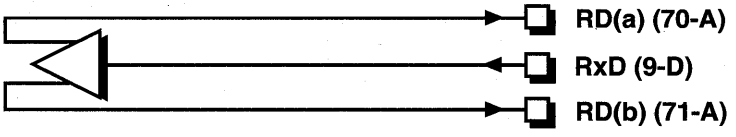
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	N/A	N/A	N/A	X	X	X	X

INPUT MODE REGISTER (R_1)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	X	X	X	X







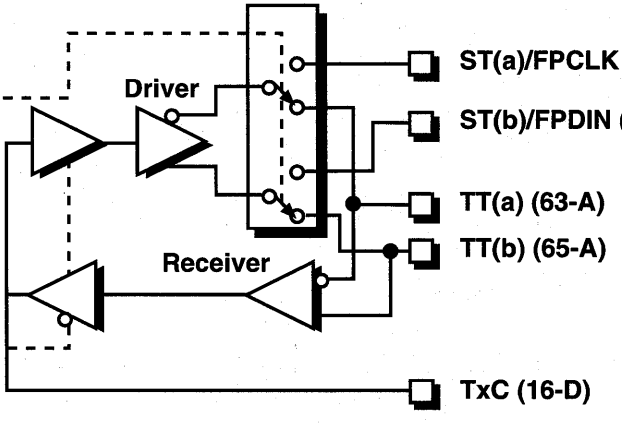
flexiPort CONTROL REGISTER (R_A)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				

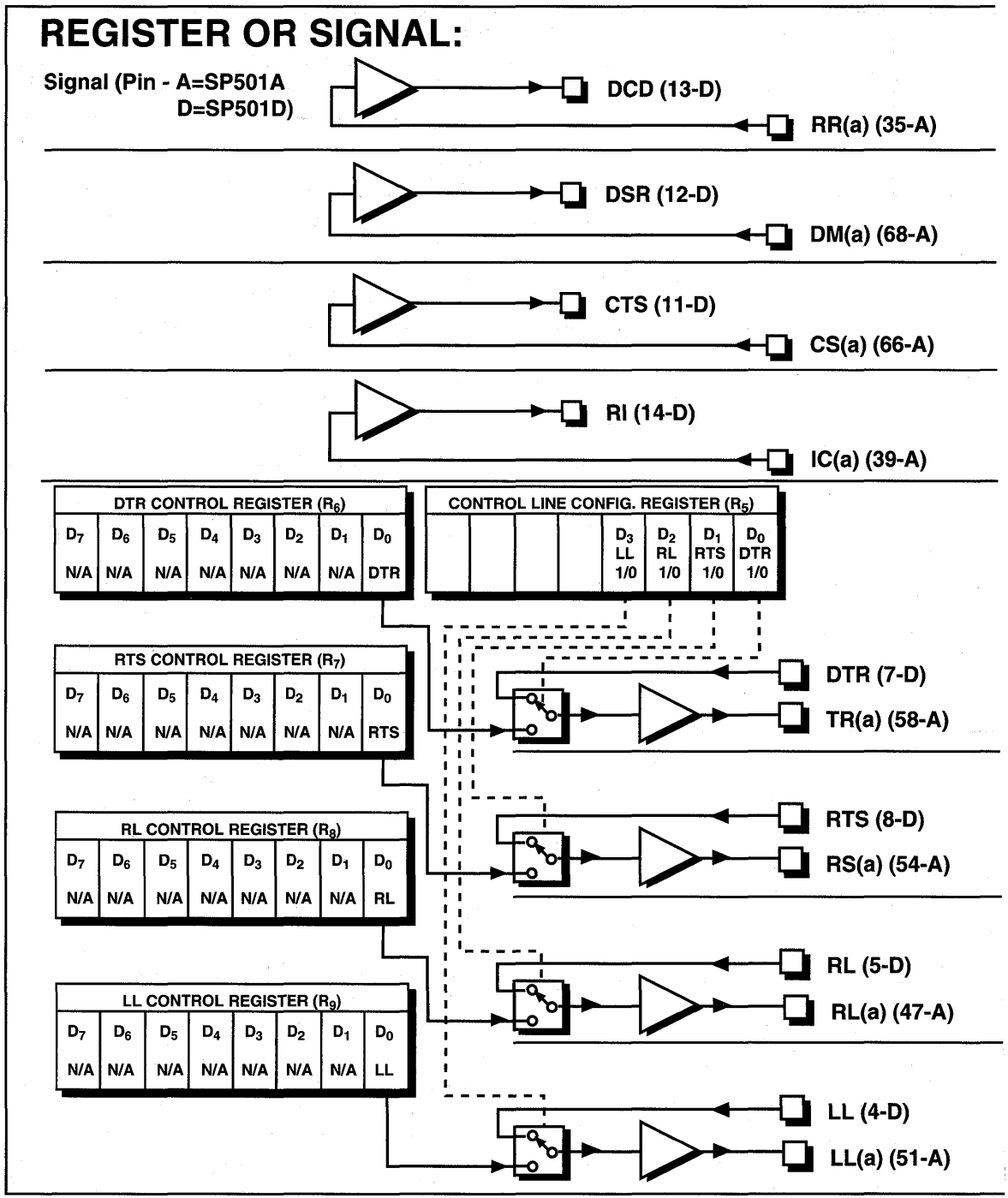
0 = TT
1 = ST

INTERFACE CONFIGURATION REGISTER (R_2)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A				



PROTOCOL:
V.35
8E 1XXX 1110
0E XXXX 1110
RS–422 (or V.35 with external attenuator)
RS–422 (or V.35 with external attenuator)
RS–422 (or V.35 with external attenuator)
RS–422 (or V.35 with external attenuator)


REGISTER OR SIGNAL:
Signal (Pin - A=SP501A
D=SP501D)
DCD (13-D)
RR(a) (35-A)
DSR (12-D)
DM(a) (68-A)
CTS (11-D)
CS(a) (66-A)
RI (14-D)
IC(a) (39-A)
DTR CONTROL REGISTER (R6)
D7 D6 D5 D4 D3 D2 D1 D0
N/A N/A N/A N/A N/A N/A N/A DTR
CONTROL LINE CONFIG. REGISTER (R5)
D3 LL 1/0
D2 RL 1/0
D1 RTS 1/0
D0 DTR 1/0
RTS CONTROL REGISTER (R7)
D7 D6 D5 D4 D3 D2 D1 D0
N/A N/A N/A N/A N/A N/A N/A RTS
DTR (7-D)
TR(a) (58-A)
RL CONTROL REGISTER (R8)
D7 D6 D5 D4 D3 D2 D1 D0
N/A N/A N/A N/A N/A N/A N/A RL
RTS (8-D)
RS(a) (54-A)
LL CONTROL REGISTER (R9)
D7 D6 D5 D4 D3 D2 D1 D0
N/A N/A N/A N/A N/A N/A N/A LL
RL (5-D)
RL(a) (47-A)
LL (4-D)
LL(a) (51-A)

	PROTOCOL:
	V.35
	RS–232
	RS–232
	RS–232
	RS–232
	RS–232
	RS–232
	RS–232
	RS–232

LOCAL LOOPBACK MODE

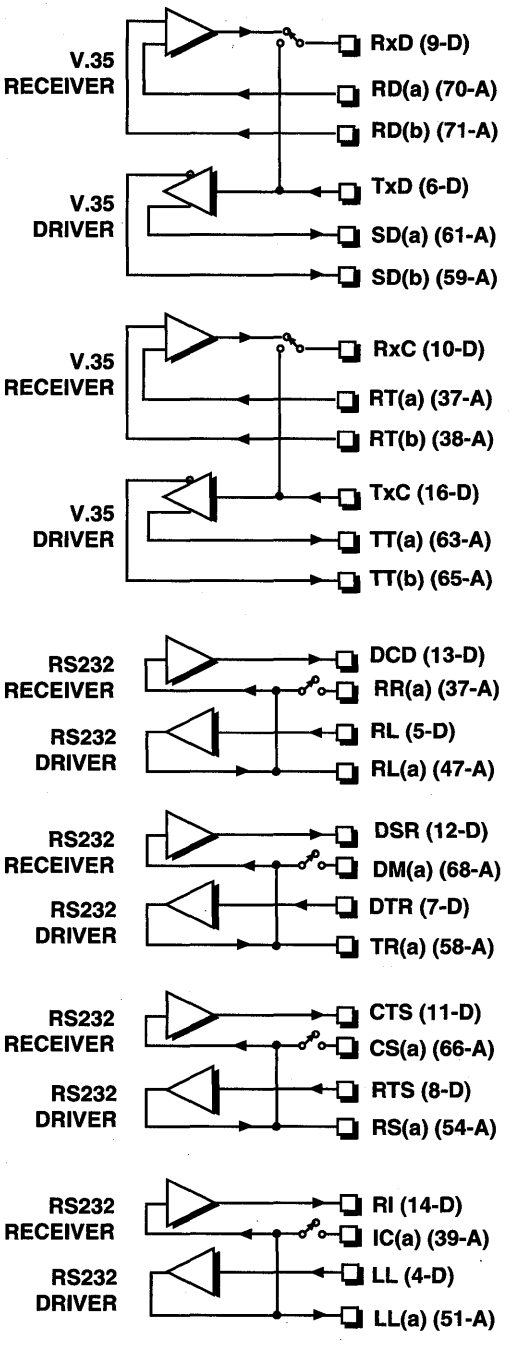
(V.35 PROTOCOL SHOWN)

Signal (Pin - A=SP501A D=SP501D)

OUTPUT MODE REGISTER (R_0)							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	N/A	N/A	N/A	1	1	1	0

INPUT MODE REGISTER (R_1)							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	1	1	1	0

INTERFACE CONFIGURATION REGISTER (R_2)							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	1	0	0	1



REMOTE LOOPBACK MODE

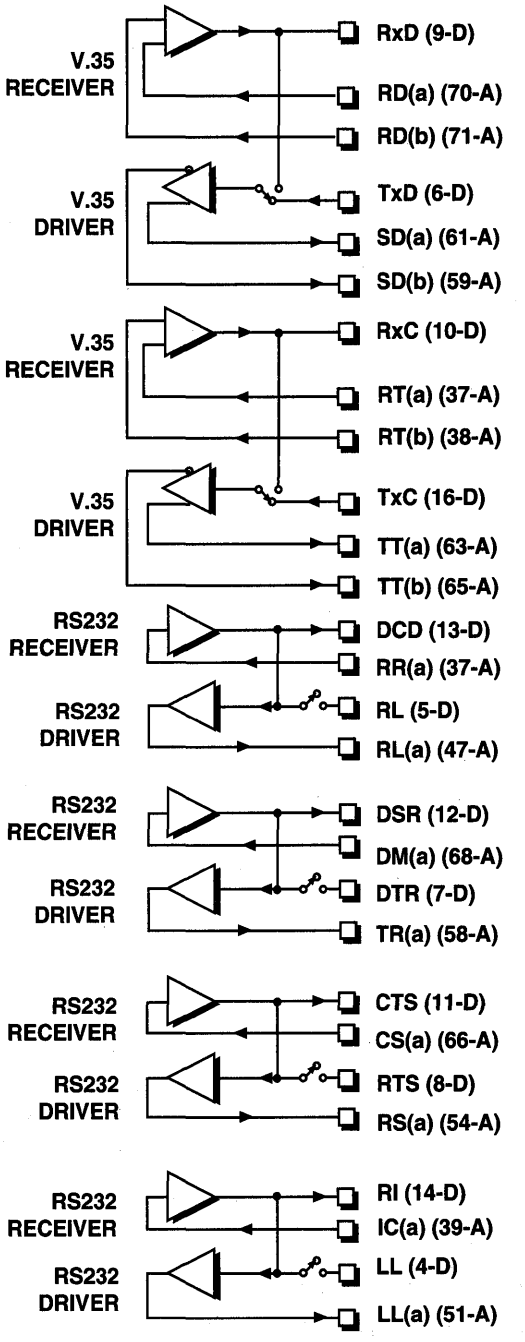
(V.35 PROTOCOL SHOWN)

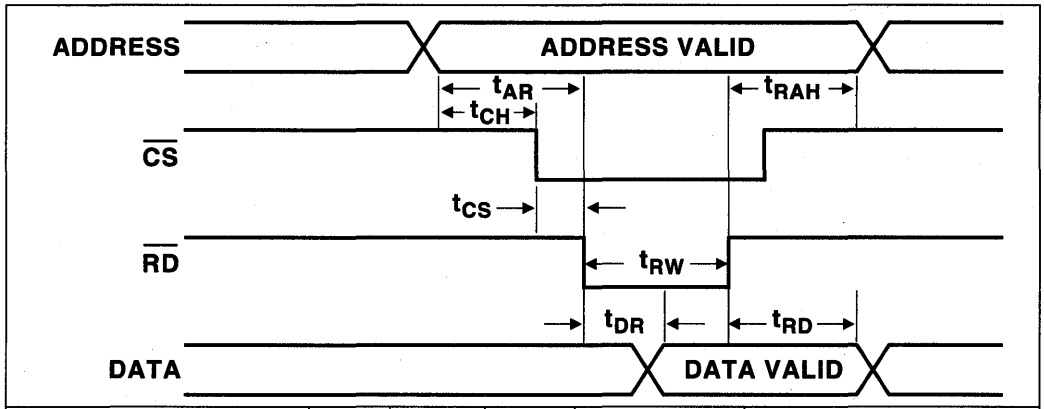
Signal (Pin - A=SP501A
D=SP501D)

OUTPUT MODE REGISTER (R_0)							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	N/A	N/A	N/A	1	1	1	0

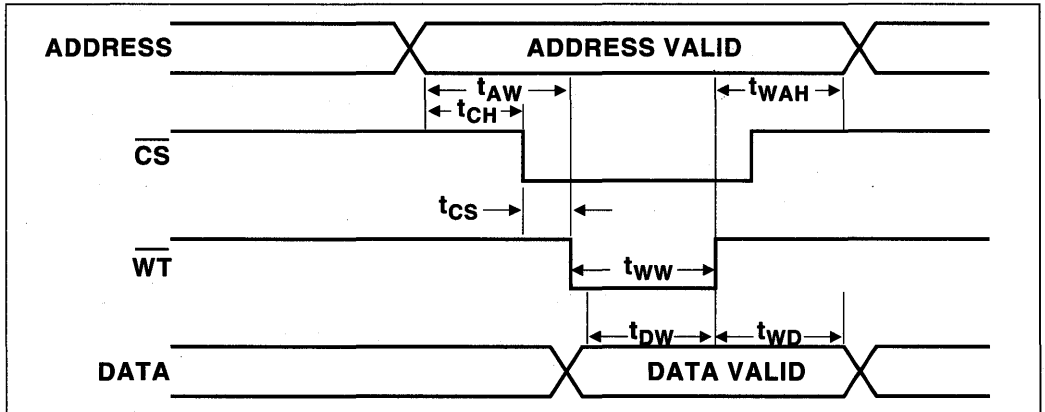
INPUT MODE REGISTER (R_1)							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	1	1	1	0

INTERFACE CONFIGURATION REGISTER (R_2)							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
N/A	N/A	N/A	N/A	1	0	1	0





	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ TIMNG					
Address Valid to CS Low		50		ns	t_{CH}
CS Low to RD Low Setup	0			ns	t_{CS}
Address Valid to RD Low		50		ns	t_{AR}
Data Valid after RD		300		ns	t_{DR}
RD Low Pulse Width		200		ns	t_{RW}
Data Hold after RD		50		ns	t_{RD}
Address Hold after RD		50		ns	t_{RAH}



	MIN.	TYP.	MAX.	UNITS	CONDITIONS
WRITE TIMNG					
Address Valid to CS Low		50		ns	t_{CH}
CS Low to WT Low Setup	0			ns	t_{CS}
Address Valid to WT Low		50		ns	t_{AW}
Data Setup before WT		225		ns	t_{DW}
WT Low Pulse Width		200		ns	t_{WW}
Data Hold after WT		100		ns	t_{WD}
Address Hold after WT		50		ns	t_{WAH}

ORDERING INFORMATION

flexiPORT™ Multi–Mode SerialTransceiver

Model	Temperature Range	Package
SP501ACF	0°C to +70°C	80–pin QFP
SP501DCF	0°C to +70°C	80–pin QFP

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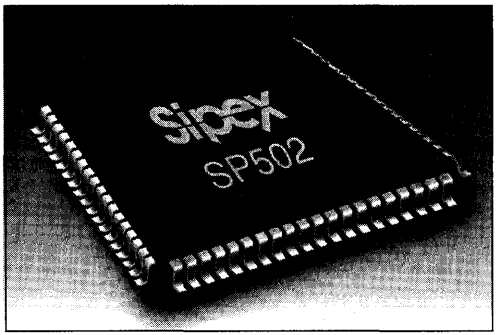
SP502

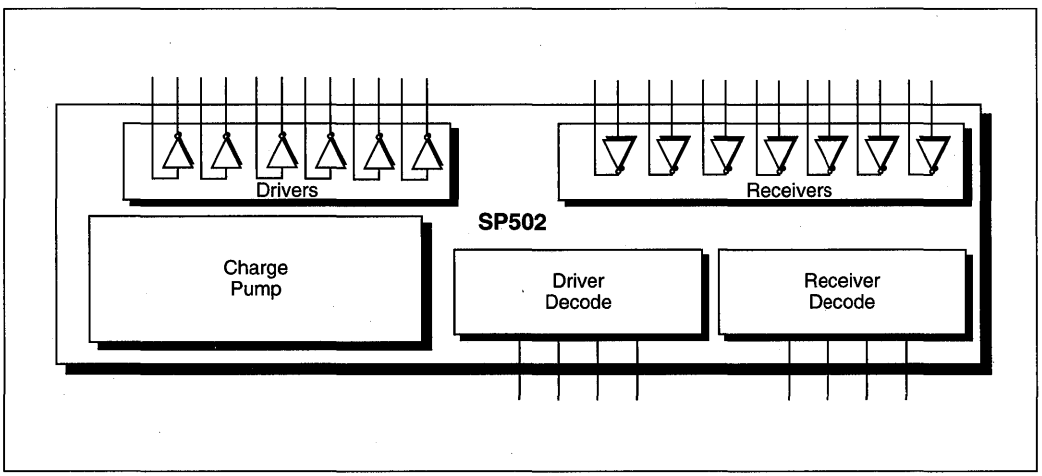
Multi–Mode Serial Transceiver

- Single–Chip Serial Transceiver Supports Industry–Standard
- Software–Selectable Protocols:
  - — RS232 (V.28)
  - — RS422A (V.11, X.27)
  - — RS449
  - — RS485
  - — V.35
  - — EIA–530
- Programmable Selection of Interface
- +5V–Only Operation
- Six (6) Drivers and Seven (7) Receivers
- Surface Mount Packaging



DESCRIPTION...

The **SP502** is a highly integrated serial transceiver that allows software control of its interface modes. It offers hardware interface modes for RS232 (V.28), RS422A (V.11), RS449, RS485, V.35, and EIA530. The **SP502** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.



SPECIFICATIONS

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= 3.2mA
V_{OH}			3.5	Volts	I_{OUT}= 1.0mA
RS485 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}			2.0	Volts	
Outputs					
High Level Output			+6.0	Volts	
Low level Output			–0.3	Volts	
Differential Output	±1.5		±5.0	Volts	R_L=54Ω, C_L=50pF
Open Circuit Voltage			±6.0	Volts	
Output Current	28			mA	R_L=54Ω
Short Circuit Current			±250	mA	Terminated in –7V to +12V
Transition Time			120	nS	Rise/fall time, 10%–90%
Transmission Rate			5	Mbps	
RS485 RECEIVER					
TTL Output Levels					
VOL	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12	Volts	(a)-(b)
Low Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			0.2	Volts	Over –7V to +12V common mode range
Receiver Open Circuit Bias					
Input Impedance			1	Unit load	Refer to graph
V.35 DRIVER					
TTL Input Levels					
VIL	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±0.44		±0.66	Volts	With termination network; R_L=100Ω
Output Impedance	50		150	Ω	with termination network
Transition Time			40	nS	
Transmission Rate			5	Mbps	
V.35 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	(a)-(b)
Low Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
Receiver Sensitivity			0.2	Volts	Over –7V to +12V common mode range
Input Impedance	50		150	Ω	with termination network

SPECIFICATIONS (continued)

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

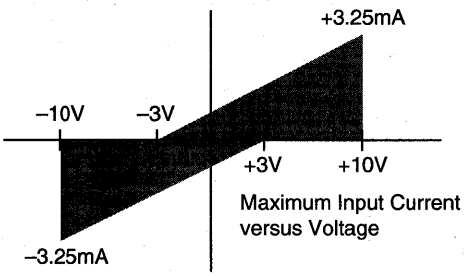
PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RS422 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±2.0		±5.0	Volts	R_L=100Ω
Open Circuit Voltage,VO			±6.0	Volts	
Balance			±0.4	Volts	$\|V_T\| - \|\overline{V_T}\|$
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	
Transition Time			60	ns	Rise/fall time, 10%-90%
Transmission Rate			5	Mbps	
RS422 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+6.0	Volts	(a)-(b)
Low Threshold	–6.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+7.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			KΩ	
RS232 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
High Level Output	+5.0		+15	Volts	RL=3KΩ, VIN=0.8V
Low Level Output	–15.0		–5	Volts	RL=3KΩ, VIN=2.0V
Open Circuit Voltage	–15		+15	Volts	
Short Circuit Current			±100	mA	
Power Off Impedance	300			Ω	
Slew Rate			30	V/µs	RL=3KΩ, CL=15pF
Transition Time			2	µs	
Transmission Rate			120	Kbps	
RS232 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold		1.7	2.4	Volts	
Low Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias	0		+2.0	Volts	
Input Impedance	3	5	7	KΩ	
RS423 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output					
High Level Output	+3.6		+6.0	Volts	RL=450Ω
Low Level Output	–6.0		–3.6	Volts	RL=450Ω

SPECIFICATIONS (continued)

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

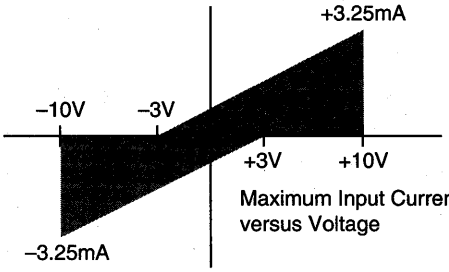
PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RS423 DRIVER					
Open Circuit Voltage	±4.0		±9.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	
Transition Time			40	ns	Rise/fall time, 10-90%
Transmission Rate			120	Kbps	
RS423 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	
Low Threshold	–6.0		–0.2	Volts	
Common Mode Range	–7.0		+12.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			KΩ	
POWER REQUIREMENTS					
V_{CC}	4.75		5.25	Volts	
I_{CC}		20	30	mA	V_{CC}= 5V; no interface selected
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	–65		+150	°C	
Package		80–pin QFP			

RS422 RECEIVER



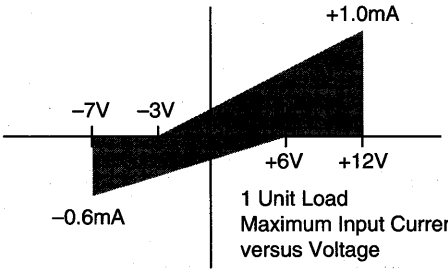
Maximum Input Current versus Voltage

RS423 RECEIVER



Maximum Input Current versus Voltage

RS485 RECEIVER



1 Unit Load
Maximum Input Current versus Voltage

AC CHARACTERISTICS

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SINGLE-ENDED MODE					
RS232					
Driver Propagation Delay					Input = 0.8V to 2.0V; 60kHz
t_{PHL}		1.7		µs	Unloaded
t_{PLH}		1.1		µs	Unloaded
t_{PHL}		2.1		µs	Loaded with 3KΩ and 2,500pF
t_{PLH}		1.7		µs	Loaded with 3KΩ and 2,500pF
Receiver Propagation Delay					Input = 0V to 5.0V; 60kHz; note 1
t_{PHL}		69		ns	
t_{PLH}		60		ns	
RS423					
Driver Propagation Delay					Input = 0.8V to 2.0V; 60kHz
t_{PHL}		2.0		µs	Loaded with 450Ω
t_{PLH}		1.3		µs	Loaded with 450Ω
Receiver Propagation Delay					Input = –0.2V to 2.0V; 60kHz; note 2
t_{PHL}		625		ns	
t_{PLH}		88.0		ns	
DIFFERENTIAL MODE					
RS485					
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz; note 3
t_{PHL}		76.0		ns	Loaded with 54Ω
t_{PLH}		62.0		ns	Loaded with 54Ω
Receiver Propagation Delay					Input = A to GND; B=–200mV to +200mV; 100kHz, note 4
t_{PHL}		150		ns	
t_{PLH}		213		ns	
RS422					
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz; note 3
t_{PHL}		78		ns	Loaded with 100Ω
t_{PLH}		65		ns	Loaded with 100Ω
Receiver Propagation Delay					Input = A to GND; B=–200mV to +200mV; 100kHz, note 4
t_{PHL}		149		ns	
t_{PLH}		213		ns	V.35
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz; note 3
t_{PHL}		79		ns	R = 100Ω with termination network
t_{PLH}		65		ns	R = 100Ω with termination network
Receiver Propagation Delay					Input = A to GND; B=–200mV to +200mV; 100kHz, note 4
t_{PHL}		246		ns	
t_{PLH}		143		ns	

AC CHARACTERISTICS (continued)

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DELAY TIME FROM ENABLE MODE TO TRI–STATE MODE					
RS232 (SINGLE–ENDED MODE)					
t_{PZL}; Enable to Output low		186.8		ns	3KΩ pull–up to output
t_{PZH}; Enable to Output high		127.0		ns	3KΩ pull–down to output
t_{PLZ}; Disable from Output low		264.0		ns	5V to input
t_{PHZ}; Disable from Output high		392.5		ns	GND to input
RS422 (DIFFERENTIAL MODE)					
t_{PZL}; Enable to Output low		94.2		ns	3KΩ pull–up to output
t_{PZH}; Enable to Output high		101.0		ns	3KΩ pull–down to output
t_{PLZ}; Disable from Output low		124.5		ns	5V to input
t_{PHZ}; Disable from Output high		135.5		ns	GND to input

Notes:
1. Measured from 2.5V of R_{IN} to 2.5V of R_{OUT}.
2. Measured from one–half of R_{IN} to 2.5V of R_{OUT}.
3. Measured from 1.5V of T_{IN} to one–half of T_{OUT}.
4. Measured from 2.5V of R_O to 0V of A and B.

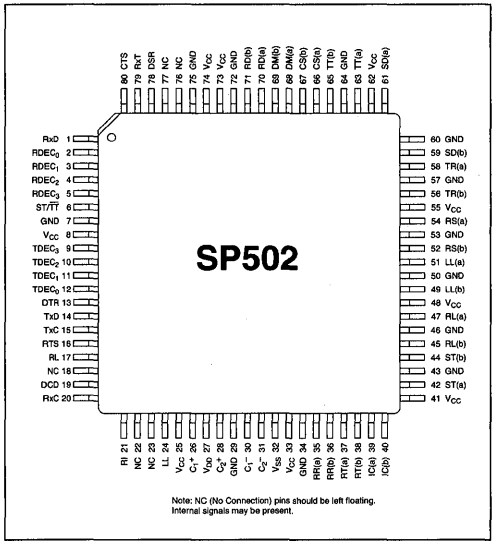
POWER MATRIX

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

Mode	Open Input	Input to 5V	Input to GND	AC Signal to Input	5V to Input with Load	GND to Input with Load	AC Signal with Load	Conditions
V.35 1110	20.71 mA	21.5mA	20.74mA	28.32mA	58.19mA	55.64mA	73.08mA	With external driver output termination network; input =0.8V to 2V, 60KHz; Load =3KΩ, 2500pF for RS232; load =100Ω for V.35
RS232 0010	22.53mA	22.41 mA	23.15mA	31.54mA	43.74mA	40.96mA	62.47mA	Input = 0.8V to 2V, 60KHz; Load = 3KΩ, 2500pF
RS422 0100	17.93mA	17.83mA	14.13mA	32.92mA	143.47mA	140.65mA	146.55mA	Input =0.8V to 2V, 2.5MHz; Load = 100Ω
RS485 0101	17.82mA	17.74mA	14.07mA	32.85mA	182.93mA	180.71 mA	183.65mA	Input = 0.8V to 2V, 2.5MHz; Load = 54Ω
RS449 1100	19.93mA	19.87mA	17.84mA	23.57mA	134.90mA	131.35mA	131.94mA	Input = 0.8V to 2V, 60KHz; Load = 450Ω for RS423; Load =100Ω for RS422
EIA530 1101	19.85mA	19.83mA	17.82mA.	23.54mA	134.90mA	131.25mA	131.78mA	Input = 0.8V to 2V, 60KHz; Load = 450Ω for RS423; Load =100Ω for RS422

*All Driver Input Common V_{CC}=5V

PINOUT...



PIN ASSIGNMENT...

CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; common TTL input for both ST and TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from TxC.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from TxC.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog In or Out — Terminal Timing, inverted; sourced to TxC or RxT.

Pin 65 — TT(b) — Analog In or Out — Terminal Timing, non–inverted; sourced to TxC or RxT.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a)— Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b)— Incoming Call; analog input,non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.
Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — RDEC0 – RDEC3 — Receiver decode register; configures receiver modes; TTL inputs.
Pin 6 — ST/$\overline{TT}$ — Enables ST or TT drivers; TTL input.
Pins 12–9 — TDEC0 – TDEC3 — Transmitter decode register; configures transmitter modes; TTL inputs.

POWER SUPPLIES

Pins 8, 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.
Pins 7, 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.
Pin 27 — VDD +10V Charge Pump Capacitor — Connects from VDD to VCC. Suggested capacitor size is 22µF, 16V.
Pin 32 — VSS –10V Charge Pump Capacitor — Connects from ground to VSS. Suggested capacitor size is 22µF, 16V.
Pins 26 and 30 — C1+ and $C1^-$ — Charge Pump Capacitor — Connects from C1+ to $C1^-$. Suggested capacitor size is 22µF, 16V.
Pins 28 and 31 — C2+ and $C2^-$ — Charge Pump Capacitor — Connects from C2+ to $C2^-$. Suggested capacitor size is 22µF, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

FEATURES...

The **SP502** is a highly integrated serial transceiver that allows software control of its interface modes. The **SP502** offers hardware interface modes for RS232 (V.28), RS422A (V.11), RS449, RS485, V.35, and EIA530. The interface mode selection is done via an 8–bit switch; four (4) bits control the drivers and four (4) bits control the receivers. The **SP502** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.

The **SP502** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The **SP502** has five (5) independent drivers and six (6) independent receivers and one half–duplex transceiver channel, which allows a maximum of six (6) drivers and seven (7) receivers. The driver and receiver configuration for the **SP502** is ideal for DTE applications. The **SP502** is made up of four separate circuit blocks — the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in detail below.

THEORY OF OPERATION

Charge–Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. *Figure 3a* shows the waveform found on the positive side of capacitor C_2, and *Figure 3b* shows the negative side of capacitor C_2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— VSS charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— VSS transfer — Phase two of the clock connects the negative terminal of C_2 to the VSS storage capacitorand the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capaci-

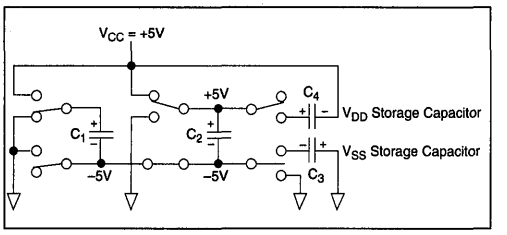


Figure 1. Charge Pump Phase 1.

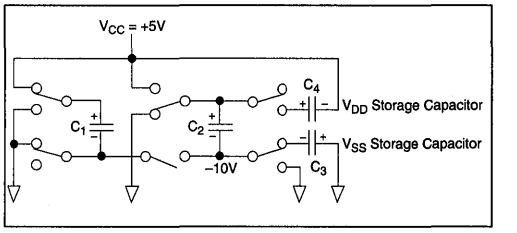


Figure 2. Charge Pump Phase 2.

tor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated 10V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V^- are separately generated from V_{CC} in a no–load condition, V+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V+ will show a decrease in the magnitude of V^- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15KHz. The external capacitors must be 22µF with a 16V breakdown rating. Two external Schottky diodes connected as in *Figure 6* are required for high rate of rise power supplies.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V^- pins. The value of the external supply voltages must be no greater than ±10V. The current drain for the ±10V supplies is used for RS232, and RS423 drivers. For the RS232 driver the current requirement will be 3.5mA per driver, and for the RS423 driver the worst case current drain will be 11mA per driver. It is critical that

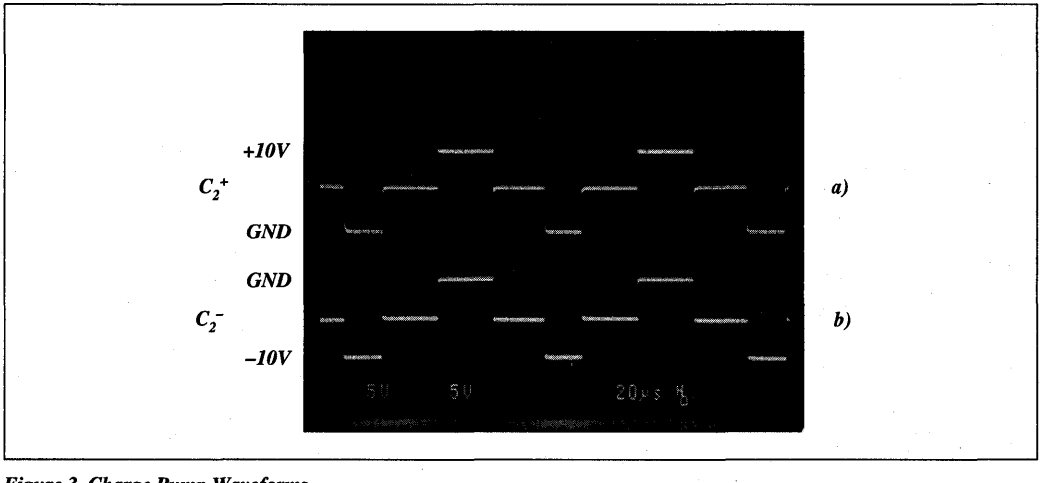


Figure 3. Charge Pump Waveforms

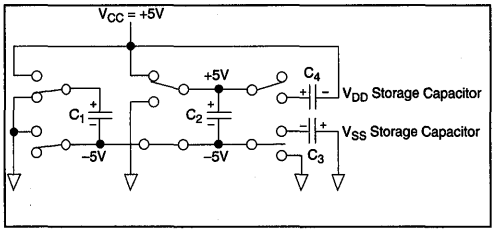


Figure 4. Charge Pump Phase 3.

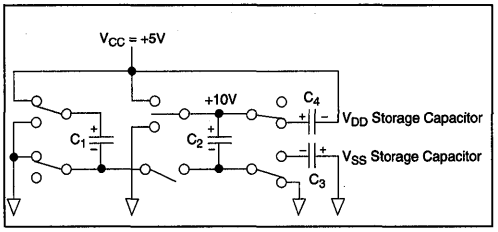


Figure 5. Charge Pump Phase 4.

the external power supplies provide a power supply sequence of :+l0V, then +5V, followed by –l0V.

Drivers

The **SP502** has six (6) drivers which can be programmed in six different modes of operation. One of the drivers for the **SP502** is internally connected to an internal receiver input to make up a half-duplex configuration. As shown in the Mode Diagrams the driver input of the half-duplex channel is shared with an adjacent driver such that when one is active the other is disabled.

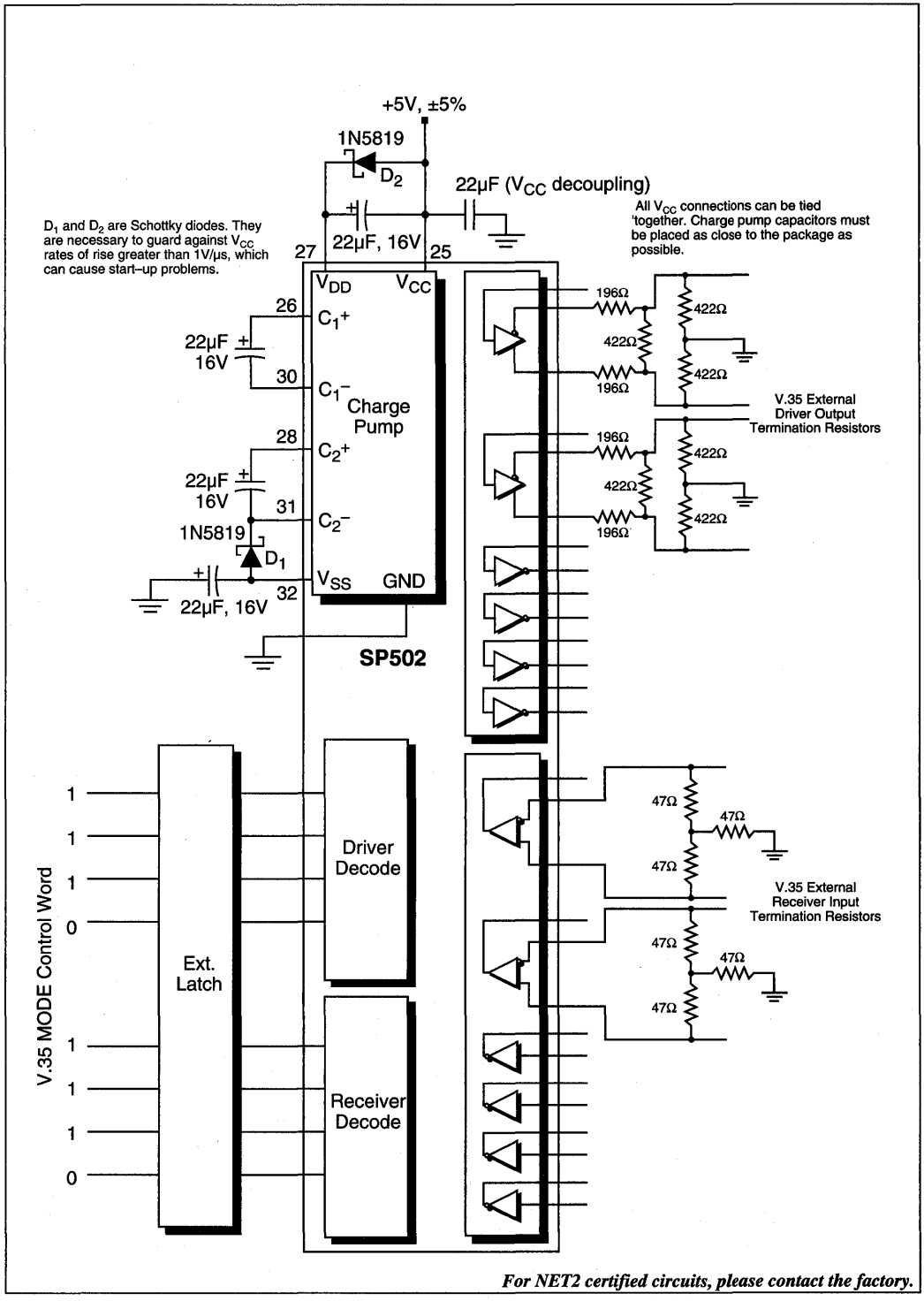
Control for the mode selection is done via a four–bit control word. The **SP502** does not have a latch; the control word must be externally latched either high or low to write the appropriate code into the **SP502**. The drivers are pre-arranged such that for each mode of operation the relative position and functionality of the drivers are set up to accomodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. *Table 1* shows a summary of the electrical characteristics of the drivers in the different interface modes. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull–up resistors to +5V or pull–down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value resistor less than 100KΩ will suffice.

There are three basic types of driver circuits — RS232, RS423, and RS485. The RS232 drivers output a minimum of ±5V level single–ended signals (with 3KΩ and 2500pF loading), and

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530
$TDEC_3$–$TDEC_0$	0000	0010	1110	0100	0101	1100	1101
SD(a)	tri–state	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
SD(b)	tri–state	tri–state	V.35+	RS422+	RS485+	RS422+	RS422+
TR(a)	tri–state	RS232	RS232	RS422–	RS485–	RS422–	RS422–
TR(b)	tri–state	tri–state	tri–state	RS422+	RS485+	RS422+	RS422+
RS(a)	tri–state	RS232	RS232	RS422–	RS485–	RS422–	RS422–
RS(b)	tri–state	tri–state	tri–state	RS422+	RS485+	RS422+	RS422+
RL(a)	tri–state	RS232	RS232	RS422–	RS485–	RS423	RS423
RL(b)	tri–state	tri–state	tri–state	RS422+	RS485+	tri–state	tri–state
LL(a)	tri–state	RS232	RS232	RS422–	RS485–	RS423	RS423
LL(b)	tri–state	tri–state	tri–state	RS422+	RS485+	tri–state	tri–state
ST(a)*	tri–state	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
ST(b)*	tri–state	tri–state	V.35+	RS422+	RS485+	RS422+	RS422+
TT(a)*	tri–state	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
TT(b)*	tri–state	15KΩ to GND	V.35+	RS422+	RS485+	RS422+	RS422+

*The ST and TT driver outputs cannot be enabled simultaneously.

Table 1. SP502 Drivers



For NET2 certified circuits, please contact the factory.

Figure 6. Typical Operating Circuit

can operate up to 120Kbps. The RS232 drivers are used in RS232 mode for all signals, and also in V.35 mode where they are used as the control line signals.

The RS423 drivers output a minimum of ±3.6V level single–ended signals (with 450Ω loading) and can operate up to 120Kbps. Open circuit V_{OL} and V_{OH} measurements may exceed the ±6V limitation of RS423. The RS423 drivers are used in RS449 and EIA530 modes as RL and LL outputs.

The third type of driver supports RS485, which is a differential signal that can maintain ±1.5V differential output levels with a worst case load of 54Ω. The signal levels and drive capability of the RS485 drivers allow them to also support RS422 requirements of ±2V differential output levels with 100Ω loads. The RS422 drivers are used in RS449 and EIA530 modes as clock, data and some control line signals.

The RS485–type drivers are also used in the V.35 mode. V.35 levels require ±0.55V signals with a load of 100Ω. In order to meet the voltage requirements of V.35, external series resistors with source impedance termination resistors must be implemented to voltage divide the driver outputs from 0 to +5V to 0 to +0.55V. *Figure 6* shows the values of the resistor network and how to connect them. The termination network also achieves the 50Ω to 150Ω source impedance for V.35. For applications that require V.11 signals for clock and data instead of V.35 levels, omit the external termination networks. All of the differntial drivers, RS485, RS422, and V.35 can operate up to 5Mbps.

Receivers

The **SP502** is equipped with seven (7) receivers which can be programmed in six (6) different modes of operation. One of the seven (7) receivers (RxT) is part of a half–duplex channel, which means its inputs are shared with a driver output, as shown in the Mode Diagrams. The RxT receiver has its inputs internally connected to the TT(a) and TT(b) pins. The select pin labeled ST/$\overline{TT}$ enables either the TT–driver or the ST–driver, but it does not disable the receiver. The RxT receiver is always connected to the TT(a) and TT(b) pins. Any signal that is received or transmitted on TT(a) and TT(b) will trigger a TTL–output at the RxT pin.

Control for the mode selection is done via a 4–bit control word that is independant from the driver control word. The coding for the drivers and receivers is identical. Therefore, if the modes for the drivers and receivers are supposed to be identical in the application, the control lines can be tied together.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed,

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530
$RDEC_3$–$RDEC_0$	0000	0010	1110	0100	0101	1100	1101
RD(a)	Undefined	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
RD(b)	Undefined	15KΩ to GND	V.35+	RS422+	RS485+	RS422+	RS422+
RT(a)	Undefined	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
RT(b)	Undefined	15KΩ to GND	V.35+	RS422+	RS485+	RS422+	RS422+
CS(a)	Undefined	RS232	RS232	RS422–	RS485–	RS422–	RS422–
CS(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	RS422+	RS422+
DM(a)	Undefined	RS232	RS232	RS422–	RS485–	RS422–	RS422–
DM(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	RS422+	RS422+
RR(a)	Undefined	RS232	RS232	RS422–	RS485–	RS422–	RS422–
RR(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	RS422+	RS422+
IC(a)	Undefined	RS232	RS232	RS422–	RS485–	RS423	RS423
IC(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	15KΩ to GND	15KΩ to GND
TT(a)*	Undefined	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
TT(b)*	Undefined	15KΩ to GND	V.35+	RS422+	RS485+	RS422+	RS422+

*TT(a) and TT(b) can be programmed as driver outputs or receiver inputs.

Table 2. SP502 Receivers

the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows a summary of the electrical characteristics of the receivers in the different interface modes. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver output, a pull–up resistor of 100KΩ to +5V should be connected to the inverting input for a logic low, or the non–inverting input for a logic high. For single-ended receivers, a pull–down resistor to ground of 5KΩ is internally connected, which will ensure a logic high output.

There are three basic types of receivers — RS232, RS423, and RS485. The RS232 receiver is a single–ended input with a threshold of 0.8V to 2.4V. The RS232 receiver has an operating voltage range of ±15V and can receive signals up to 120Kbps. RS232 receivers are used in RS232 mode for all signal types, and in V.35 mode for control line signals.

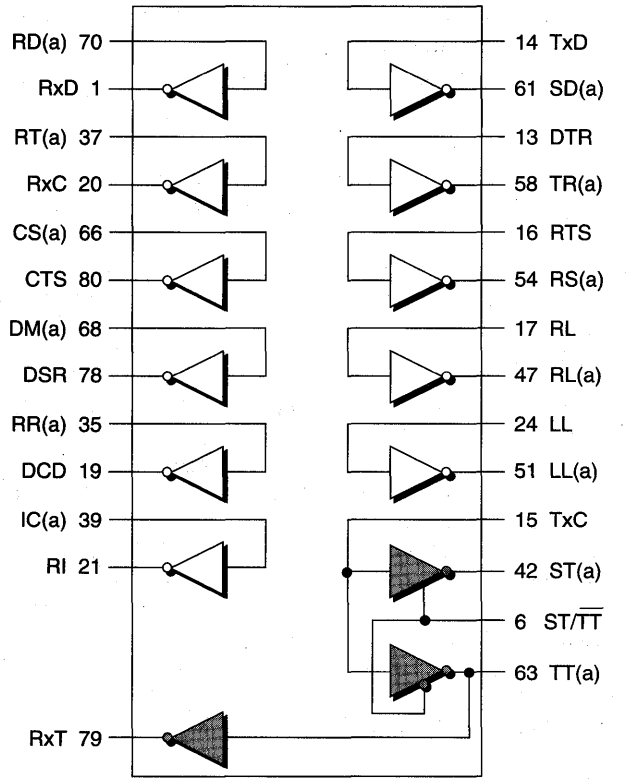
The RS423 receivers are also single–ended but have an input threshold as low as ±200mV. The input imedance is guaranteed to be greater than 4KΩ, with an operating voltage range of ±7V. The RS423 receivers can operate up to 120Kbps. RS423 receivers are used for the IC signal in RS449 and EIA530 modes, as shown in *Table 2*.

The third type of receiver supports RS485, which is a differential interface mode. The RS485 receiver has an input impedance of 15KΩ and a differential threshold of ±200mV. Since the characteristics of an RS422 receiver are actually subsets of RS485, the receivers for RS422 requirements are identical to the RS485 receivers. RS422 receivers are used in RS449 and EIA530 for receiving clcok, data, and some control line signals. The RS485 receivers are also used for the V.35 mode. In order to meet the V.35 input impedance of 100Ω, the external termination network of *Figure 6* must be applied. The threshold of the V.35 receiver is ±200mV. The V.35 receivers can operate up to 5Mbps. All of the differential receivers can receive data up to 5Mbps.

Decoder

The **SP502** has the ability to change the interface mode of the drivers or receivers via an 8–bit switch. The decoder for the drivers and receivers is not latched; it is merely a combinational logic switch. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP502**. Undefined codes may represent other interface modes not specified or random outputs, (consult the factory for more information). The drivers are controlled with the data bits labeled $TDEC_3$–$TDEC_0$. The drivers can be put into tri-state mode by writing 0000 to the driver decode switch. The receivers are controlled with data bits $RDEC_3$–$RDEC_0$; the code 0000 written to the receivers will place the outputs in an undetermined state. The receivers do not have tri-state capability, the outputs will either be high or low depending upon the state of the receiver input.

MODE: RS232							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	0	1	0	0	0	1	0



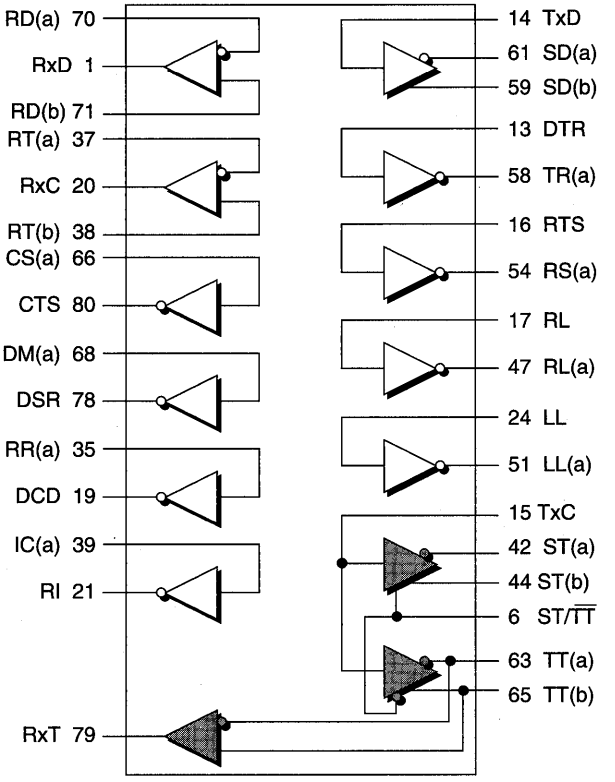
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 7. Mode Diagram — RS232

MODE: V.35							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	0	1	1	1	0



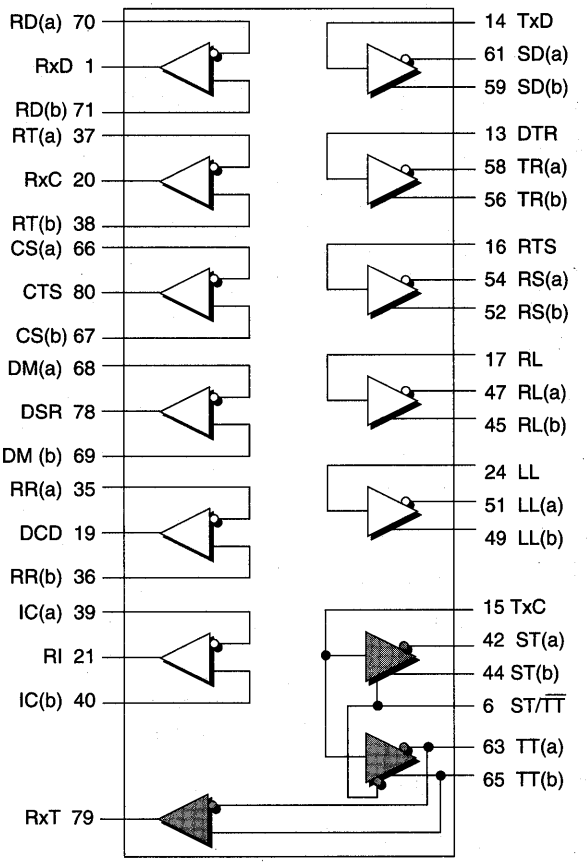
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 8. Mode Diagram — V.35

MODE: RS422							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	0	0	1	0	0



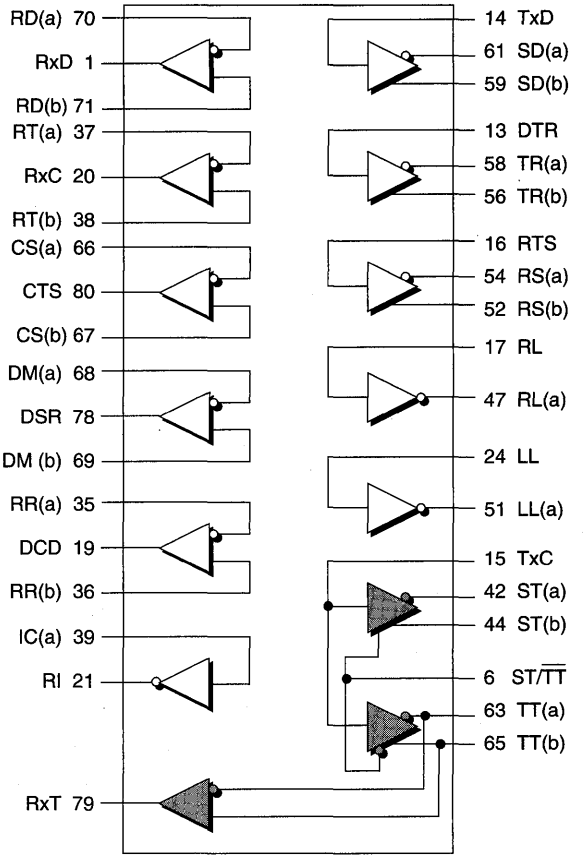
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 9. Mode Diagram — RS422

MODE: RS449							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	0	1	1	0	0



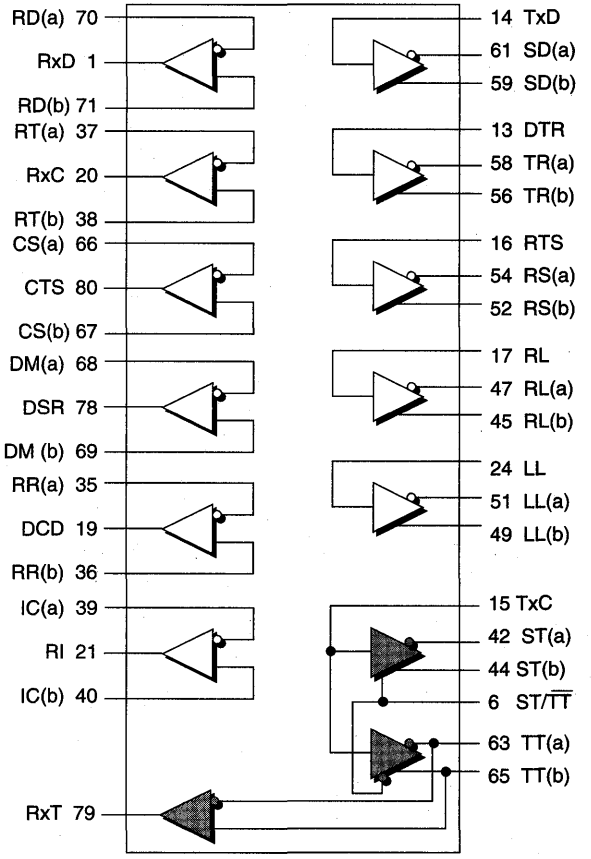
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 10. Mode Diagram — RS449

MODE: RS485							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	1	0	1	0	1



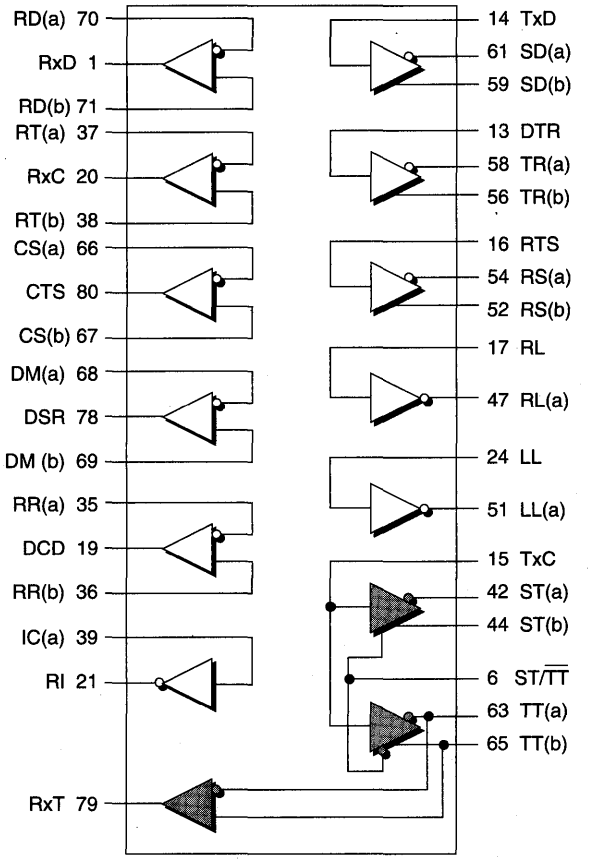
$ST/\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 11. Mode Diagram — RS485

MODE: EIA 530							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	1	1	1	0	1



ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 12. Mode Diagarm — EIA530

APPLICATION EXAMPLE

The example application that follows is a fully configured serial I/O channel in a DTE configuration. The example is comprised of the following functional elements:

- Processor
- SCC
- **SP502**
- Mode Select Register (R0[WR])
- RL & LL Control Bit Register (R1[WR])
- RI Status Bit Register (R1[RD])
- Address Decode Logic
- Baud Rate Clock Source
- I/O Connector Interface

Each of the elements of the application example are described below. Please refer to *Figure13*.

Processor

The example schematic shows a generic 8–bit processor connected to a generic SCC. The processor is also connected to three registers. The registers are described in further detail below.

Address Decode Logic

The address decode logic is connected to the Processor control and address busses and provides the logic necessary to decode the I/O read and write operations for the SCC, Mode Select Register, RL and LL Control Bit Register and the RI Status Bit Register.

SCC

The SCC provides the I/O functions for a single serial channel. The SCC is connected to the Processor I/O bus and is programmed by the user software. The SCC's TTL-level serial I/O pins are connected to the corresponding TTL–level serial I/O pins on the **SP502**.

SP502

The **SP502** provides buffering and translation from TTL levels to the selected physical level interface standard, such as RS-232, V.35, etc. The physical level interface pins are connected to a standard 25 pin D-sub miniature connector wired in a DTE configuration with the pin assignments corresponding to the EIA–530 specification. This choice was purely arbitrary. However, it provides all the necessary signals to support standards other than EIA–530, such as V.35, RS–232, RS–449, etc. with an appropriate cable adapter.

The **SP502** driver and receiver modes are independently configured by programming the **SP502**'s RDEC and TDEC input pins. In the example, the pins are driven by the Mode Select Register with a programmed value stored by the user's software.

Since the **SP502** is shown in a DTE configuration, the example assumes that any synchronous interface clocking will be provided by the attached DCE device. Consequently, the ST/TT pin is tied to +5V, thus causing the **SP502** to receive the transmit clock on the TT(a) and TT(b) input pins and output the transmit clock to the SCC on the RxT output pin. The receive clock is input to the **SP502** on the RT(a) and RT(b) pins and output to the SCC on the RxC pin.

Mode Select Register

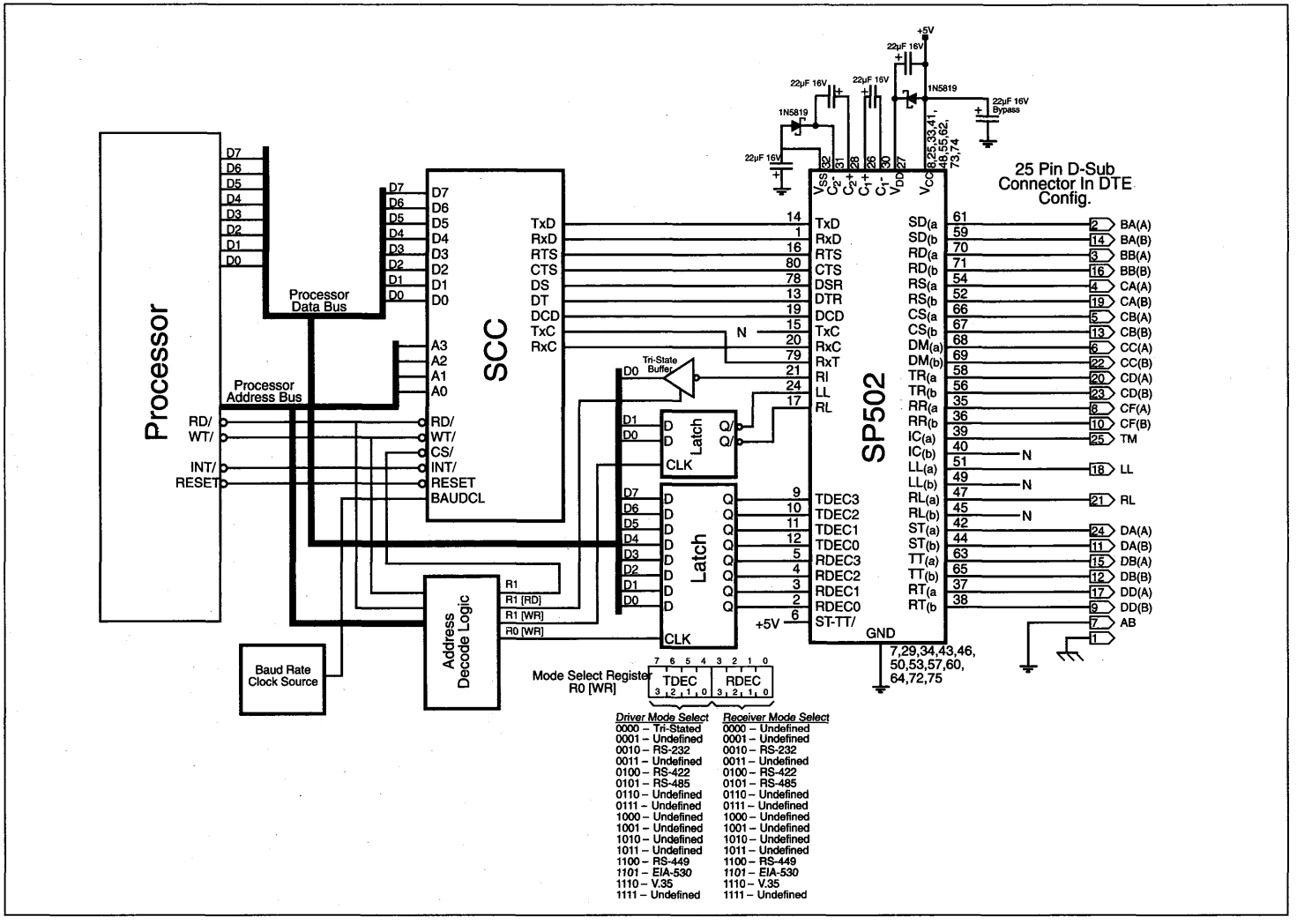
The mode select register is an 8–bit latch attached to the Processor data bus. The Processor, under user–software control, can program the Mode Select Register with the appropriate values to select the **SP502**'s driver and receiver modes.

The table shown on the schematic below the register lists the values for programming the register to drive the RDEC and TDEC pins on the **SP502** for the desired physical level interface. The receivers and drivers can be programmed independently, but in this example the Mode Select Register must be programmed with both the RDEC and TDEC values at the same time. This is because the RDEC and TDEC pins are driven from the same 8–bit latch.

Note that selecting modes for TDEC that are shown in the table as undefined will result in the drivers operating in an undefined mode and should not be used. Likewise, selecting modes for RDEC that are shown in the table as undefined will result in indeterminate logic levels present on the TTL outputs of the **SP502**. Undefined RDEC or TDEC values should never be programmed.

Several other approaches for driving the RDEC and TDEC signals are possible. One approach would use two independent 4–bit latches, one each to drive the RDEC and TDEC pins as separate groups. Another approach would use one 4–bit latch,

Figure 13. DTE Serial Communications Channel



each output of the latch would drive a corresponding pair of RDEC/TDEC signals. For instance, $RDEC_0$ and $TDEC_0$ could be tied together and be driven by the low order bit of the 4–bit latch.

RL & LL Control Bit Registers

A 2–bit latch is used to allow the Processor to program the states of the RL and LL interface signals. This latch is necessary since most SCCs do not support RL and LL control signals.

RI Status Bit Register

A 1–bit read register is implemented using a tri–state buffer. This will allow the Processor to read the state of the RI (Ring Indicator) interface signal. This is necessary since most SCCs do not support the RI interface signal.

The example interface shows the **SP502A**'s IC(a) input tied to the EIA530 signal TM (Test Mode). EIA530 does not specify an RI signal. If EIA530 operation is required, the RI Status Bit Register could be used to monitor the condition of the TM signal or it could be ignored. For other interface standards, the connector pin 25 on the schematic could be tied to the RI signal through a cable adapter arrangement. For instance, if RS232 operation is used, pin 25 of the connector could be tied to pin 22 of the RS232 adapter (circuit CE) and the RI Status Bit Register then used to monitor the RS232 signal for ring indicator.

Baud Rate Clock Source

Most SCCs require an external clock source for operation in asynchronous and self-clocking applications.

I/O Connector Interface

The I/O connector is wired to the **SP502A** such that the interface represents a DTE device. As shown, the connector is wired in an EIA–530 configuration with EIA530 signal mnemonics. A 25–pin connector wired to the EIA–530 specification provides pins for all interface signals supported by the **SP502**. If the **SP502** is programmed for other physical interfaces, such as V.35, then an adapter cable will provide the necessary conversion from the EIA530 pin–outs to those required by the V.35 standard together with its ISO 2593 connector.

Notes Regarding V.35 Operation

The user will have to provide additional resistor networks if correct V.35 signal levels and termination impedances are required. This is necessary because the **SP502** does not provide V.35 signal terminations when programmed for V.35 operation. Two approaches are possible. First, if the **SP502** is permanently programmed to operate as V.35 only, with no other interface standard required, then the appropriate resistors can be mounted on the PCB near the **SP502**. Second, if the **SP502** will be programmed for a variety of standards, then a better approach might be to provide the resistors as part of the cable adapter assembly used to convert from the standard EIA530 connector pin–outs shown in the example to the V.35/ ISO–2593 connector and pin–outs.

SP502/SP503 EVALUATION BOARD

The **SP502/SP503 Evaluation Board** (EB) Is designed to offer as much flexibility to the user as possible. Each board comes equipped with an 80–pin QFP Zero– Insertion socket to allow for testing of multiple devices. The control lines and inputs and outputs of the device can be controlled either manually or via a data bus under software control. There is a 50–pin connector to allow for easy connection to an existing system via a ribbon cable. There are also open areas on the PC board to add additional circuitry to support application–specific requirements.

Manual Control

The SP502/SP503EB will support both the **SP502** or **SP503** multi–mode serial transceivers. When used for the **SP502,** disregard all notation on the board that is in [brackets] . The **SP502** has a half–duplex connection between the RxT receiver and the TT driver. Due to this internal connection, the RxT receiver inputs can be accessed via the TT(a) and TT(b) pins. If the user needs separate receiver input test pins, jumpers JP1 and JP2 can be inserted to allow for separate receiver inputs located at SCT(a) and SCT(b). The corresponding TTL output for this receiver is labeled as SCT. This test point is tied to pin 79 of the **SP502** or **SP503**. Pin 7 of the evaluation board is connected to the DIP switch, and is labeled as (SCTEN). When used with the **SP502**, this pin should be switched to a low state. When the evaluation board is used with the **SP503**, pin 7 is a tri–state control pin for the SCT receiver.

The transceiver I/O lines are brought out to test pins arranged in the same configuration as shown elsewhere in this data sheet. A top layer silk–screen shows the drivers and receivers to allow direct correlation to the data sheet. The transmitter and receiver decode bits are tied together and are brought out to a DIP switch for manual control of both the driver and receiver interface modes. Since the coding for the drivers and receivers is identical, the bits have been tied together. The DIP switch has 7 positions, four of which are reserved for the TDEC/RDEC control and the other three are used as tri–state control pins. The labels that are in [brackets] apply only to the **SP503**, If a logic one is asserted the corresponding red LED will be lit; If a zero is asserted the corresponding red LED will not be lit.

Software Control

A 50–pin connector brings all the analog and digital I/O lines, V_{CC}, and GND to the edge of the card. This can be wired to the user's existing design via a ribbon cable, The pinout for the connector is described in the following section. When the evaluation board is operated under software control, the DIP switch should be set up so that all bits are low (all LEDs off). This will tie pulldown resistors from the inputs to ground and let the external system control the state of the control inputs.

Power and Ground Requirements

The evaluation board layout has been optimized for performance by using basic analog circuit techniques, The four charge–pump capacitors must be 22µF (16V) and be placed as close to the unit as possible; tantalum capacitors are suggested. The decoupling capacitor must be a minimum of 1µF; depending upon the operating environment, 10µF should be enough for worst case situations. The ground plane for the part must be solid, extending completely under the package, The power supplies for the device should be as accurate as possible; for rated performance ±5% is necessary. The power supply current will vary depending upon the selected mode, the amount of loading and the data rate. As a maximum, the user should reserve 200mA for I_{CC}. The worst–case operating mode is RS485 under full load of six (6) drivers supplying 1.6V to 54Ω loads. The power and ground inputs can be supplied through either the banana jacks on the evaluation board (Red = V_{CC} = +5V±5%; Black = GND) or through the connector.

For reference, the 80–pin QFP Socket is a TESCO part number FPQ–80–65–09A. The 50–pin connector is an AMP part number 749075–5.

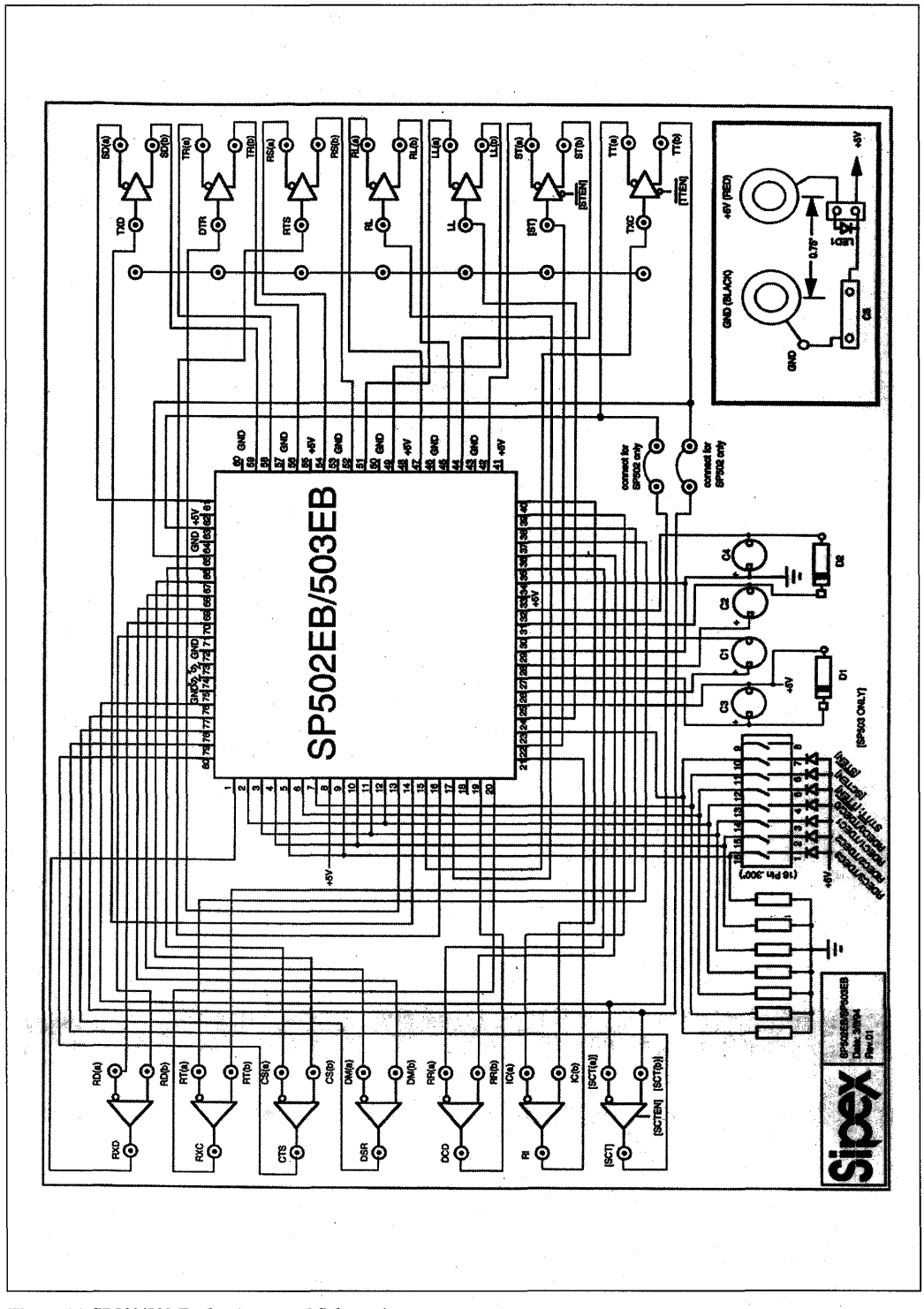


Figure 16. SP502/503 Evaluation Board Schematic

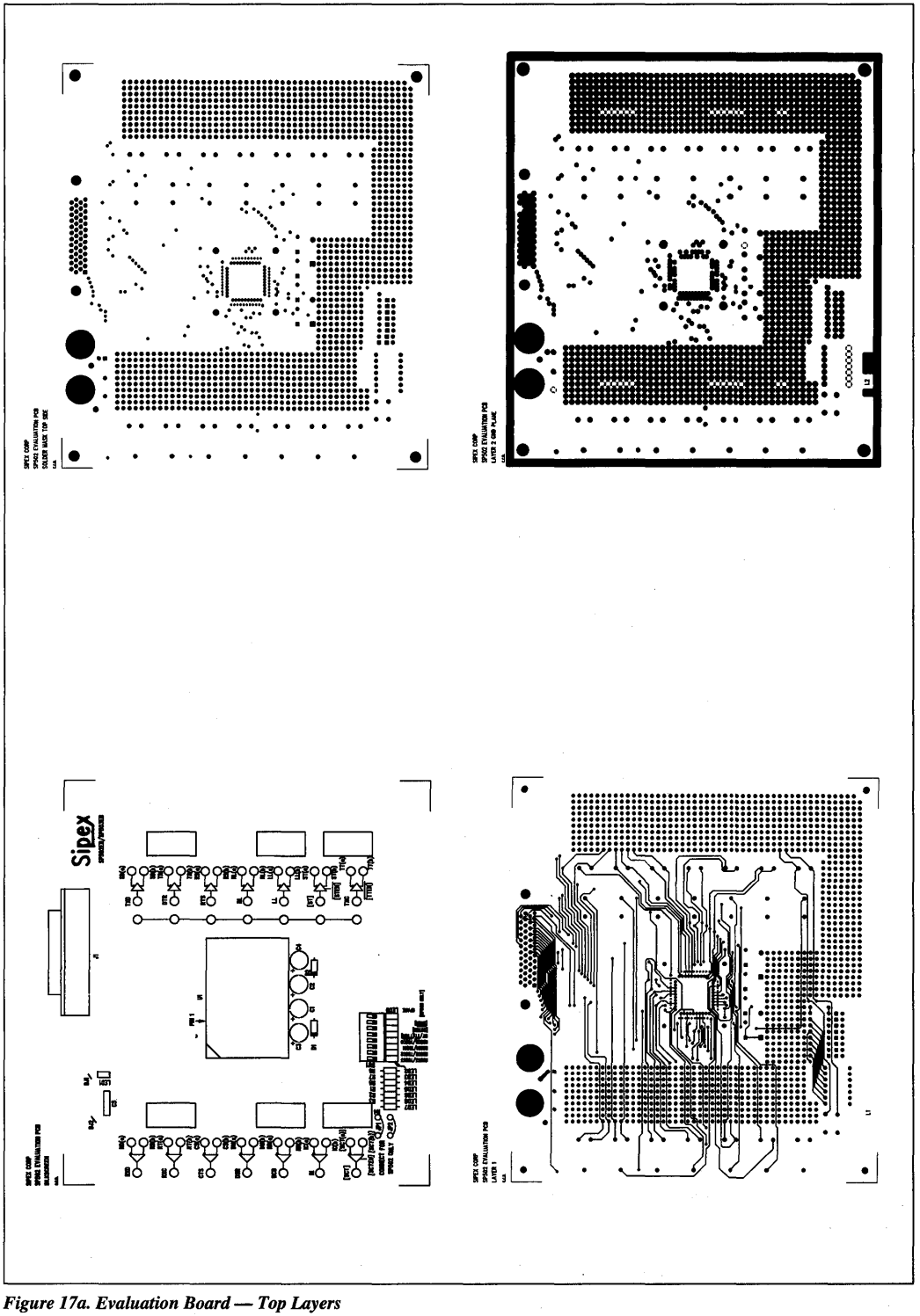
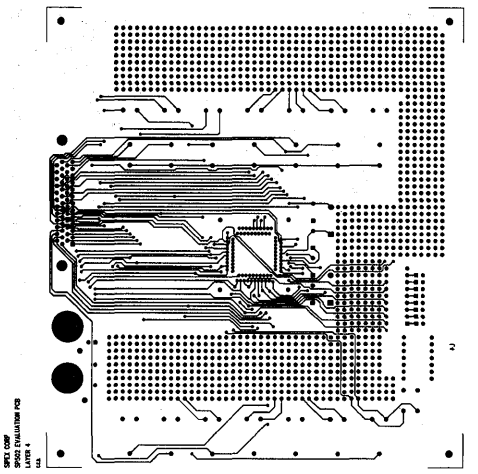
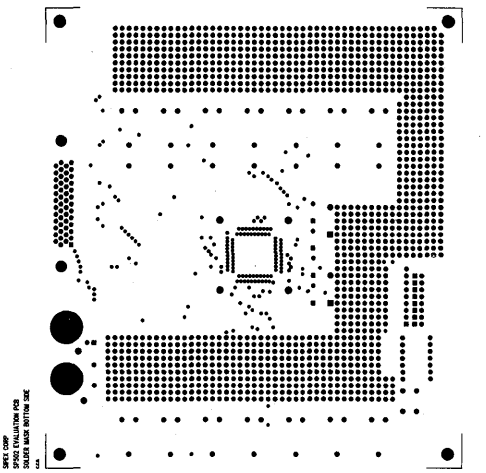


Figure 17a. Evaluation Board — Top Layers





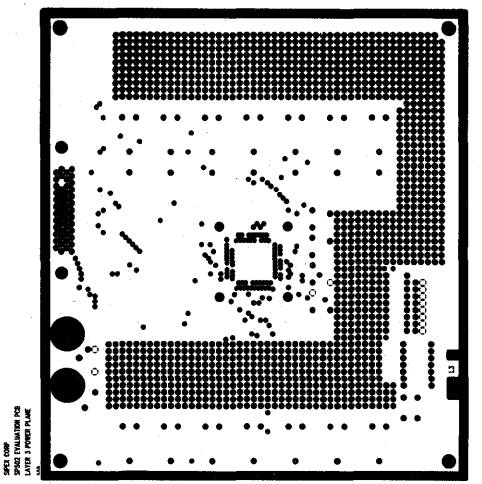


Figure 17b. Evaluation Board — Bottom Layers

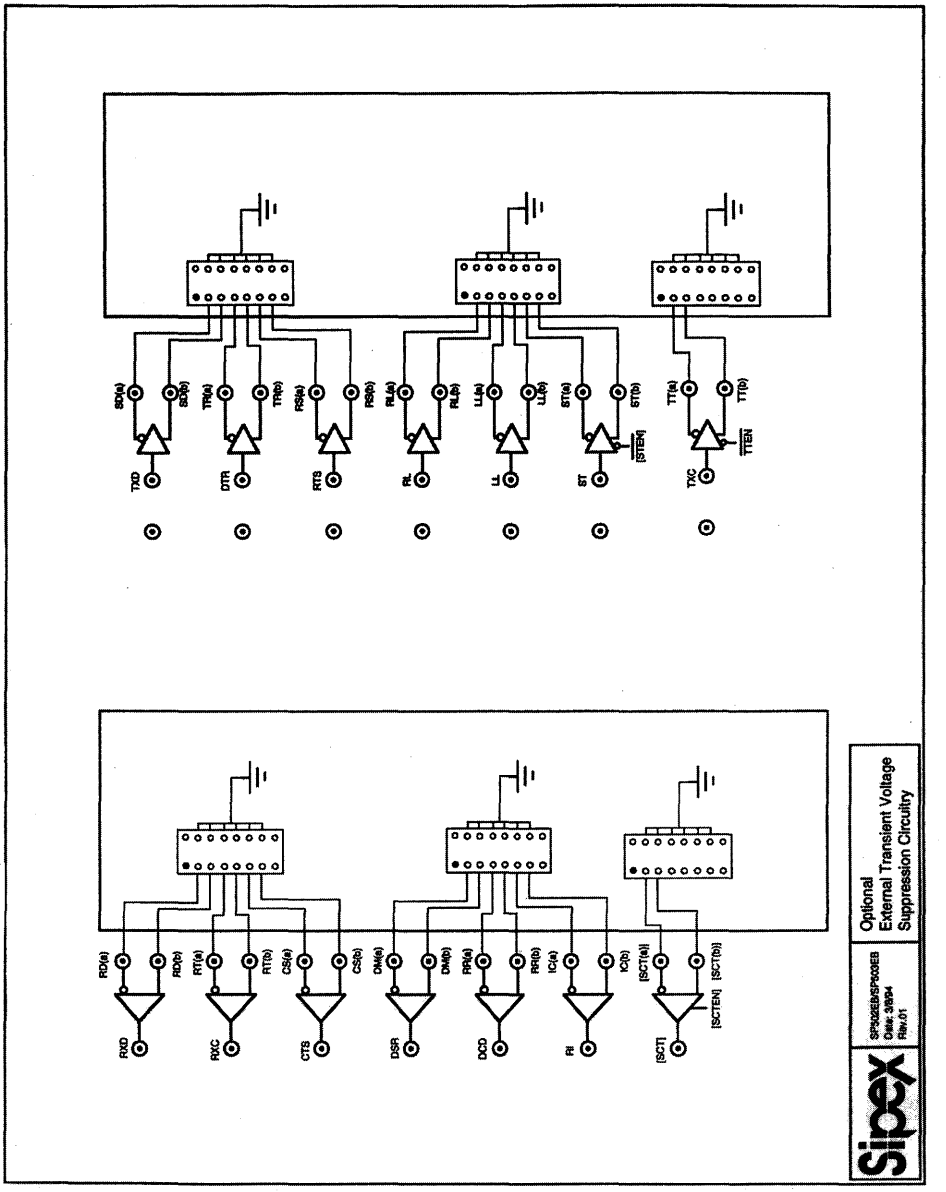
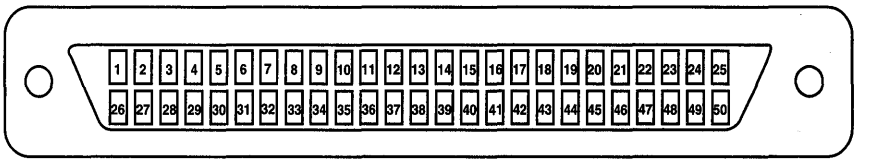
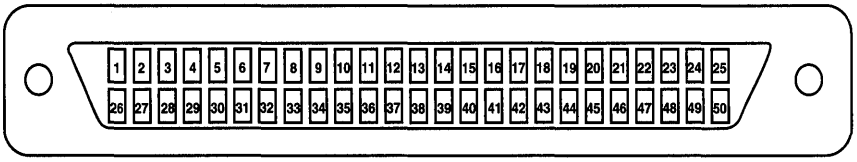


Figure 18. External Transient Suppressors



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
01	TxD (pin 14) –TTL Input – Transmit data; source for SD(a) and SD(b) outputs.
02	DTR (pin 13) – TTL Input – Data terminal ready: source for TR(a) and TR(b) outputs.
03	ST/$\overline{TT}$ (pin 6) –TTL Input – ST/$\overline{TT}$ select pin; enables ST drivers and disables TT drivers when high. Disables ST drivers and enables TT drivers when low.
04	$TDEC_3$/$RDEC_3$ (pin 5) – TTL Input – Transmitter/Receiver decode register.
05	$TDEC_2$/$RDEC_2$ (pin 4) – TTL Input – Transmitter/Receiver decode register.
06	$TDEC_1$/$RDEC_1$ (pin 3) – TTL Input – Transmitter/Receiver decode register.
07	$TDEC_0$/$RDEC_0$ (pin 2) – TTL Input – Transmitter/Receiver decode register.
08	RxD (pin 1) – TTL Output – Receive data; sourced from RD(a) and RD)b) inputs.
09	CTS (pin 80) – TTL Output – Clear to send; sourced from CS(a) and CS(b) inputs.
10	RxT (pin 79) – TTL Output – RxT; sourced from TT(a), TT(b) inputs.
11	DSR (pin 78) – TTL Output – Data set ready; sourced from DM(a) and DM(b) inputs.
12	RD(b) (pin 71) – Analog In – Receive data, non–inverted; source for RxD.
13	RD(a) (pin 70) – Analog In – Receive data, inverted: source for RxD.
14	DM(b) (pin 69) – Analog In – Data mode, non–inverted; source for DSR.
15	DM(a) (pin 68) – Analog In – Data mode, inverted; source for DSR.
16	CS(b) (pin 67) – Analog In – Clear to send; non–inverted; source for CTS.
17	CS(a) (pin 66) – Analog In – Clear to send, inverted; source for CTS.
18	TT(b) (pin 65) – Analog In or Out – Terminal timing, non–inverted: sourced to RxT or from TxC input.
19	TT(a) (pin 63) – Analog In or Out – Terminal timing; inverted: sourced to RxT or from TxC input.
20	TR(a) (pin 58) – Analog Out – Terminal ready, inverted; sourced from DTR.
21	TR(b) (pin 56) – Analog Out – Terminal ready; non–inverted; sourced from DTR.
22	SD(a) (pin 61) – Analog Out – Send data, inverted; sourced from TxD.
23	SD(b) (pin 59) – Analog Out – Send data; non–inverted; sourced from TxD.
24	RS(a) (pin 54) – Analog Out – Ready to send; inverted; sourced from RTS.
25	RS(b) (pin 52) – Analog Out – Ready to send, non–inverted; sourced from RTS.



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
26	ST (pin 22) – TTL Input – Send Timing; source for ST(a) and ST(b) outputs. SP503 only.
27	[$\overline{\text{STEN}}$] (pin 23) – TTL Input — Driver enable control pin; active low; SP503 only.
28	[SCT(a)] (pin 76) – Analog Input – Inverting; input for SCT receiver; SP503 only.
29	[SCT(b)] (pin 77) – Analog Input – Non–inverting; input for SCT receiver. SP503 only.
30	V_{CC} — +5V for all circuitry.
31	GND — signal and power ground.
32	LL(a) (pin 51) – Analog Out – Local loopback, inverted; sourced from LL.
33	LL(b) (pin 49) – Analog Out – Local loopback, non–inverted sourced from LL.
34	RL(a) (pin 47) – Analog Out – Remote loopback; inverted; sourced from RL.
35	RL(b) (pin 45) – Analog Out – Remote loopback; non–inverted; sourced from RL.
36	ST(b) (pin 44) – Analog Out – Send timing, non–inverted; sourced from TxC.
37	ST(a) (pin 42) – Analog Output –Send timing, inverted; sourced from TxC.
38	IC(b) (pin 40) – Analog In – Incoming call; non–inverted; source for RI.
39	IC(a) (pin 39) – Analog In – Incoming call; inverted; source for RI.
40	RT(b) (pin 38) – Analog In – Receive timing, non–inverted; source for RxC.
41	RT(a) (pin 37) – Analog In – Receive timing; inverted; source from RxC.
42	RR(b) (pin 36) – Analog In – Receiver ready; non–inverted; source for DCD.
43	RR(a) (pin 35) – Analog In – Receiver ready; inverted; source for DCD.
44	LL (pin 24) – TTL Input – Local loopback; source for LL(a) and LL(b) outputs.
45	RI (pin 21) – Output – Ring indicator; sourced from IC(a) and IC(b) inputs.
46	RxC (pin 20) – TTL Output – Receive clock; sourced from RT(a) and RT(b) inputs.
47	DCD (pin 19) – TTL Output – Data carrier detect; sourced from RR(a) and RR(b) inputs.
48	RL (pin 17) – Analog Out – Remote loopback; source for RL(a) and RL(b) outputs.
49	RTS (pin 16) – TTL Input – Ready to send; source for RS(a) and RS(b) outputs.
50	TxC (pin 15) – TTL Input – Transmit clock; common TTL input for both ST and TT driver outputs.

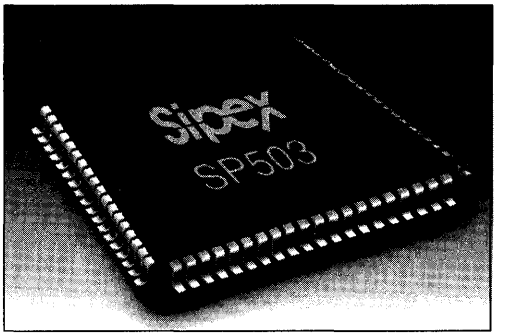
ORDERING INFORMATION

Model	Temperature Range	Package Types
SP502CF	0°C to +70°C	80–pin QFP

SP503

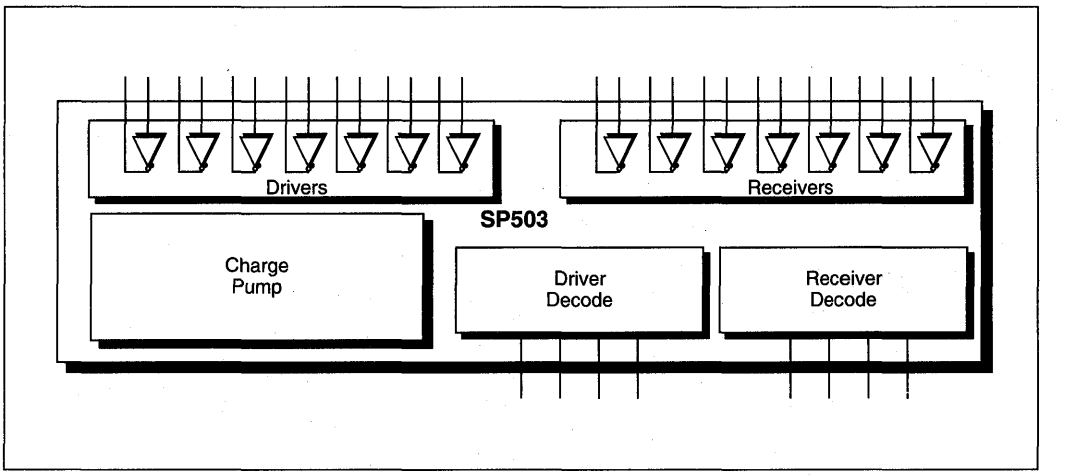
Multi–Mode Serial Transceiver

- Single-Chip Serial Transceiver Supports Industry-Standard
- Software-Selectable Protocols:
  - — RS232 (V.28)
  - — RS422A (V.11, X.27)
  - — RS449
  - — RS485
  - — V.35
  - — EIA-530
- Programmable Selection of Interface
- +5V-Only Operation
- Seven (7) Drivers and Seven (7) Receivers
- Surface Mount Packaging



DESCRIPTION...

The **SP503** is a highly integrated serial transceiver that allows software control of its interface modes. It offers hardware interface modes for RS232 (V.28), RS422A (V.11), RS449, RS485, V.35, and EIA530. The **SP503** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.



SPECIFICATIONS

Typical at 25°C and nominal supply voltages unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= 3.2mA
V_{OH}			3.5	Volts	I_{OUT}= 1.0mA
RS485 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}			2.0	Volts	
Outputs					
High Level Output			+6.0	Volts	
Low level Output			–0.3	Volts	
Differential Output	±1.5		±5.0	Volts	R_L=54Ω, C_L=50pF
Open Circuit Voltage			±6.0	Volts	
Output Current	28			mA	R_L=54Ω
Short Circuit Current			±250	mA	Terminated in –7V to +12V
Transition Time			120	nS	Rise/fall time, 10%–90%
Transmission Rate			5	Mbps	
RS485 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12	Volts	(a)-(b)
Low Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			0.2	Volts	Over –7V to +12V common mode range
Receiver Open Circuit Bias					
Input Impedance			1	Unit load	Refer to graph
V.35 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±0.44		±0.66	Volts	With termination network; R_L=100Ω
Output Impedance	50		150	Ω	with termination network
Transition Time			40	nS	
Transmission Rate			5	Mbps	
V.35 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	(a)-(b)
Low Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
Receiver Sensitivity			0.2	Volts	Over –7V to +12V common mode range
Input Impedance	50		150	Ω	With termination network

SPECIFICATIONS (Continued)

Typical at 25°C and nominal supply voltages unless otherwise noted.

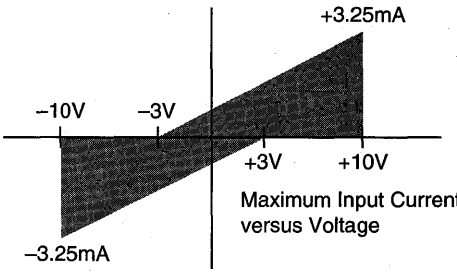
	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS422 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±2.0		±5.0	Volts	R_L=100Ω
Open Circuit Voltage,V_O			±6.0	Volts	
Balance			±0.4	Volts	$\|V_T\| - \overline{\|V_T\|}$
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	
Transition Time			60	ns	Rise/fall time, 10%-90%
Transmission Rate			5	Mbps	
RS422 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+6.0	Volts	(a)-(b)
Low Threshold	–6.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+7.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			KΩ	
RS232 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
High Level Output	+5.0		+15	Volts	R_L=3KΩ, V_{IN}=0.8V
Low Level Output	–15.0		–5	Volts	R_L=3KΩ, V_{IN}=2.0V
Open Circuit Voltage	–15		+15	Volts	
Short Circuit Current			±100	mA	
Power Off Impedance	300			Ω	
Slew Rate			30	V/µs	R_L=3KΩ, C_L=15pF
Transition Time			2	µs	
Transmission Rate			120	Kbps	
RS232 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold		1.7	2.4	Volts	
Low Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias	0		+2.0	Volts	
Input Impedance	3	5	7	KΩ	
RS423 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output					
High Level Output	+3.6		+6.0	Volts	R_L=450Ω
Low Level Output	–6.0		–3.6	Volts	R_L=450Ω
Open Circuit Voltage	±4.0		±9.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	

SPECIFICATIONS (Continued)

Typical at 25°C and nominal supply voltages unless otherwise noted.

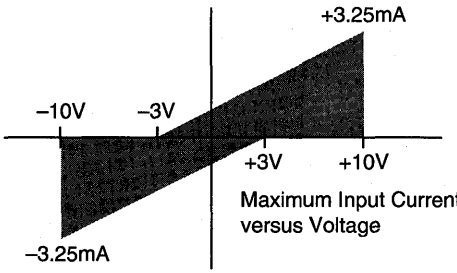
	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS423 DRIVER					
Transition Time			40	ns	Rise/fall time, 10-90%
Transmission Rate			120	Kbps	
RS423 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
High Threshold	+0.2		+12.0	Volts	
Low Threshold	–6.0		–0.2	Volts	
Common Mode Range	–7.0		+12.0	Volts	
High Input Current					Refer to graph
Low Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			KΩ	
POWER REQUIREMENTS					
V_{CC}	4.75		5.25	Volts	
I_{CC}		20	30	mA	V_{CC}=5V; no interface selected
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	–65		+150	°C	
Package		80–pin QFP			

RS422 RECEIVER



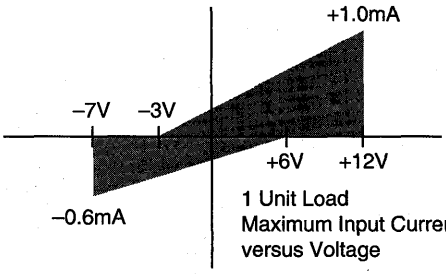
Maximum Input Current versus Voltage

RS423 RECEIVER



Maximum Input Current versus Voltage

RS485 RECEIVER



1 Unit Load
Maximum Input Current versus Voltage

AC CHARACTERISTICS

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SINGLE-ENDED MODE					
RS232					
Driver Propagation Delay					Input = 0.8V to 2.0V; 60kHz
t_{PHL}		1.7		µs	Unloaded
t_{PLH}		1.1		µs	Unloaded
t_{PHL}		2.1		µs	Loaded with 3KΩ and 2,500pF
t_{PLH}		1.7		µs	Loaded with 3KΩ and 2,500pF
Receiver Propagation Delay					Input = 0V to 5.0V; 60kHz; note 1
t_{PHL}		69		ns	
t_{PLH}		60		ns	
RS423					
Driver Propagation Delay					Input = 0.8V to 2.0V; 60kHz
t_{PHL}		2.0		µs	Loaded with 450Ω
t_{PLH}		1.3		µs	Loaded with 450Ω
Receiver Propagation Delay					Input = –0.2V to 2.0V; 60kHz; note 2
t_{PHL}		625		ns	
t_{PLH}		88.0		ns	
DIFFERENTIAL MODE					
RS485					
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz; note 3
t_{PHL}		76		ns	Loaded with 54Ω
t_{PLH}		62		ns	Loaded with 54Ω
Receiver Propagation Delay					Input = A to GND; B=–200mV to +200mV; 100kHz, note 4
t_{PHL}		149		ns	
t_{PLH}		213		ns	
RS422					
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz; note 3
t_{PHL}		78		ns	Loaded with 100Ω
t_{PLH}		65		ns	Loaded with 100Ω
Receiver Propagation Delay					Input = A to GND; B=–200mV to +200mV; 100kHz, note 4
t_{PHL}		149		ns	
t_{PLH}		213		ns	V.35
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz; note 3
t_{PHL}		79		ns	R = 100Ω with termination network
t_{PLH}		65		ns	R = 100Ω with termination network
Receiver Propagation Delay					Input = A to GND; B=–200mV to +200mV; 100kHz, note 4
t_{PHL}		246		ns	
t_{PLH}		143		ns	

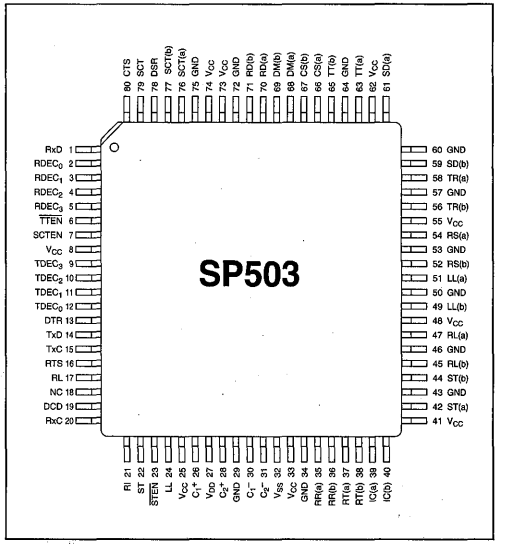
AC CHARACTERISTICS (continued)

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DELAY TIME FROM ENABLE MODE TO TRI–STATE MODE					
RS232 (SINGLE–ENDED MODE)					
t_{PZL}; Enable to Output low		186.8		ns	3KΩ pull–up to output
t_{PZH}; Enable to Output high		127.0		ns	3KΩ pull–down to output
t_{PLZ}; Disable from Output low		264.0		ns	5V to input
t_{PHZ}; Disable from Output high		392.5		ns	GND to input
RS422 (DIFFERENTIAL MODE)					
t_{PZL}; Enable to Output low		94.2		ns	3KΩ pull–up to output
t_{PZH}; Enable to Output high		101.0		ns	3KΩ pull–down to output
t_{PLZ}; Disable from Output low		124.5		ns	5V to input
t_{PHZ}; Disable from Output high		135.5		ns	GND to input

Notes:
1. Measured from 2.5V of R_{IN} to 2.5V of R_{OUT}.
2. Measured from one–half of R_{IN} to 2.5V of R_{OUT}.
3. Measured from 1.5V of T_{IN} to one–half of T_{OUT}.
4. Measured from 2.5V of R_O to 0V of A and B.

PINOUT...



PIN ASSIGNMENTS...
CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non–inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit: analog input, non–inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a)— Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b)— Incoming Call; analog input,non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — $RDEC_0$ – $RDEC_3$ — Receiver decode register; configures receiver modes; TTL inputs.

Pin 6 — $\overline{TTEN}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pins 12–9 — $TDEC_0$ – $TDEC_3$ — Transmitter decode register; configures transmitter modes; TTL inputs.

Pin 23 — $\overline{STEN}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 8, 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capaci-

tor size is 22µF, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22µF, 16V.

Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^-. Suggested capacitor size is 22µF, 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^-. Suggested capacitor size is 22µF, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

FEATURES...

The **SP503** is a highly integrated serial transceiver that allows software control of its interface modes. The **SP503** offers hardware interface modes for RS232 (V.28), RS422A (V.11), RS449, RS485, V.35, and EIA530. The interface mode selection is done via an 8–bit switch; four (4) bits control the drivers and four (4) bits control the receivers. The **SP503** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.

The **SP503** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The SP503 has seven (7) independent drivers and seven (7) independent receivers. The seventh driver of the SP503 allows the it to support applications which require two separate clock outputs making it ideal for DCE applications.

THEORY OF OPERATION

The **SP503** is made up of four separate circuit blocks — the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in more detail below.

Charge–Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. Figure la shows the waveform found on the positive side of capcitor C2, and figure lb shows the negative side of capcitor C2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is l0V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated l0V across C_2 to C_4, the V_{DD} storage capacitor. Again,

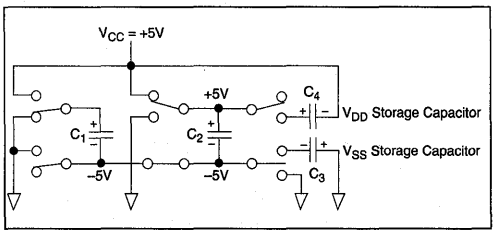


Figure 1. Charge Pump Phase 1.

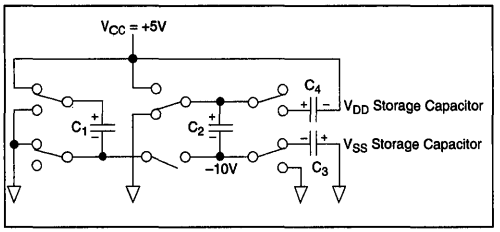


Figure 2. Charge Pump Phase 2.

simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V^- are separately generated from V_{CC} in a no–load condition, V+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V+ will show a decrease in the magnitude of V^- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 22µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V^- pins. The value of the external supply voltages must be no greater than ±10V. The current drain for the ±10V supplies is used for RS232, and RS423 drivers. For the RS232 driver the current requirement will be 3.5mA per driver, and for the RS423 driver the worst case current drain will be 11mA per driver. It is critical that the external power supplies provide a power supply sequence of :+10V, then +5V, followed by –10V.

Drivers

The **SP503** has seven (7) independant drivers, two of which have separate active–low tri–state controls. If a half-duplex channel is required, this can be achieved with external connections.

Control for the mode selection is done via a four–bit control word. The **SP503** does not have a latch; the control word must be externally latched either high or low to write the appropriate code into the **SP503**. The drivers are prearranged such that for each mode of operation the relative position and functionality of the drivers are set up to accomodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. T*able 1* shows a summary of the electrical characteristics of the drivers in the different interface modes. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull–up resistors to +5V or pull–down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value

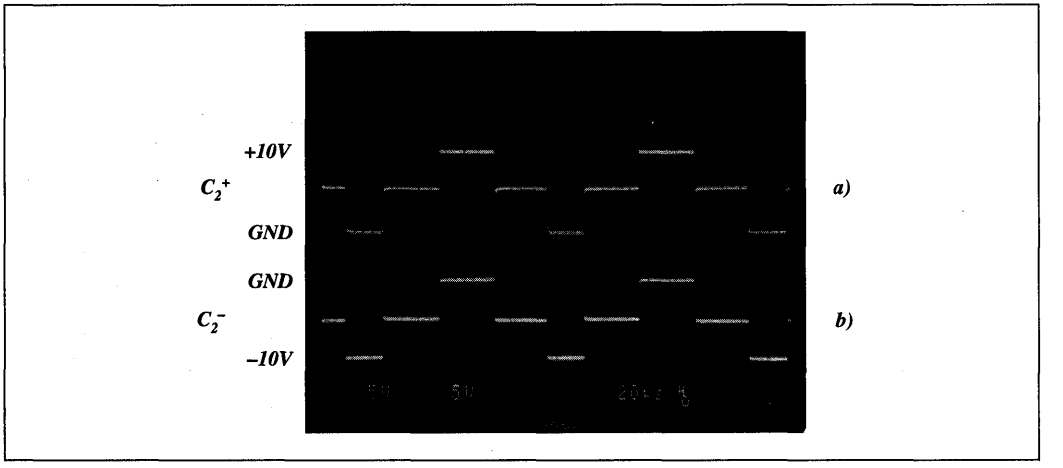


Figure 3. Charge Pump Waveforms

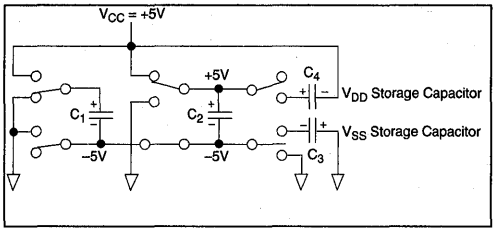


Figure 4. Charge Pump Phase 3.

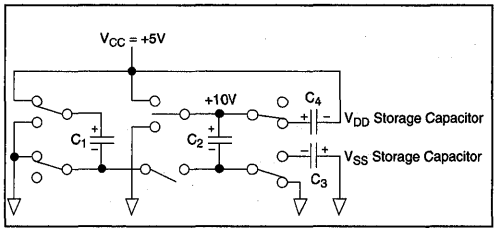


Figure 5. Charge Pump Phase 4.

resistor less than 100KΩ will suffice.

There are three basic types of driver circuits — RS232, RS423, and RS485. The RS232 drivers output a minimum of ±5V level single–ended signals (with 3KΩ and 2500pF loading), and can operate up to 120Kbps. The RS232 drivers are used in RS232 mode for all signals, and also in V.35 mode where they are used as the control line signals.

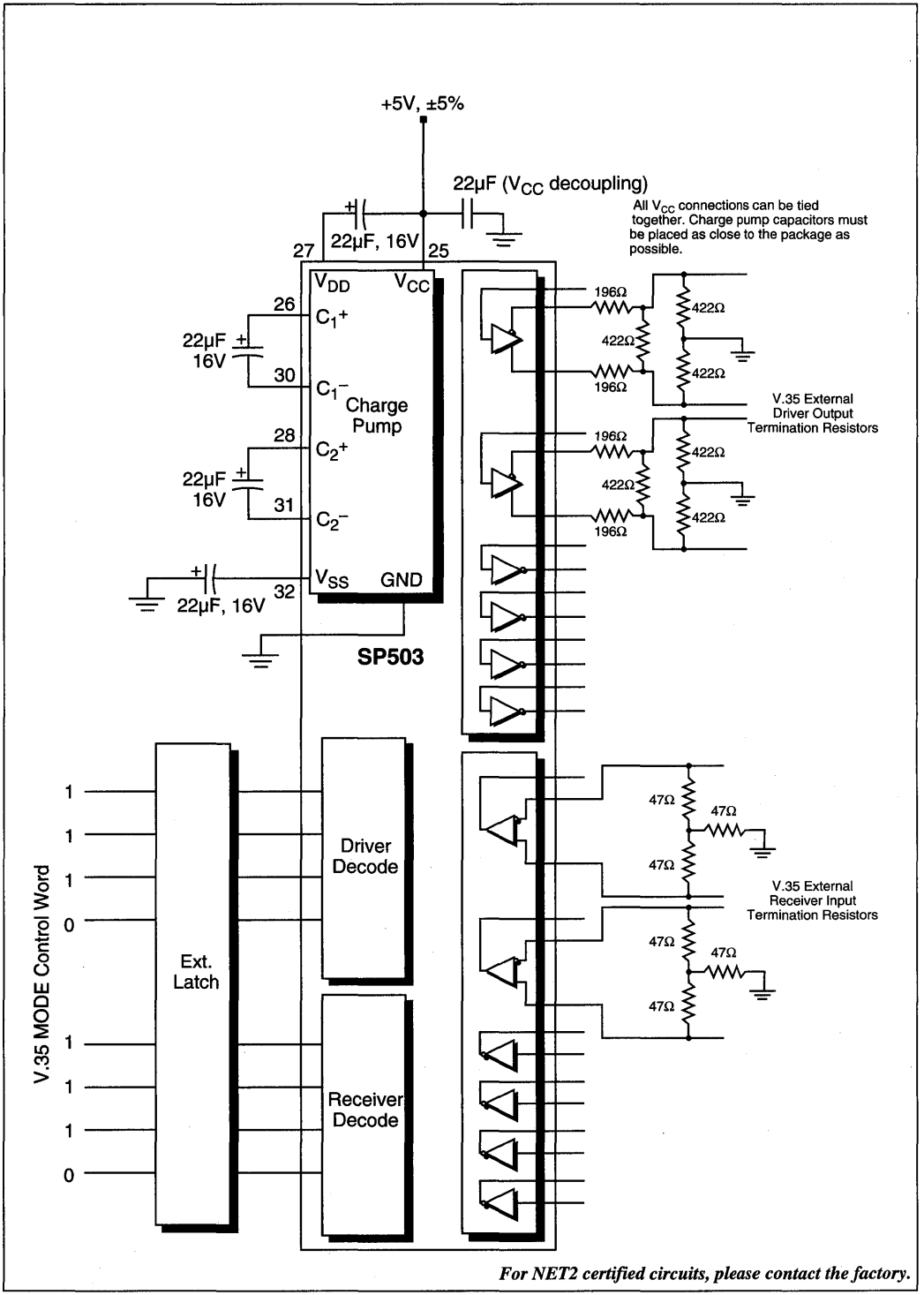
The RS423 drivers output a minimum of ±3.6V level single–ended signals (with 450Ω loading) and can operate up to 120Kbps. Open circuit V_{OL} and V_{OH} measurements may exceed the ±6V limitation of RS423. The RS423 drivers are used in RS449 and EAI530 modes as RL and LL outputs.

The third type of driver supports RS485, which is a differential signal that can maintain ±1.5V differential output levels with a worst case load of 54Ω. The signal levels and drive capability of the RS485 drivers allow the drivers to also support RS422 requirements of ±2V differential output levels with 100Ω loads. The RS422 drivers are used in RS449 and EIA530 modes as clock, data and some control line signals.

The RS485–type drivers are also used in the V.35 mode. V.35 levels require ±0.55V signals with a load of 100Ω. In order to meet the voltage requirements of V.35, external series resistors with source impedance termination resistors must be implemented to voltage divide the driver outputs from 0 to +5V to 0 to +0.55V. *Figure 6* shows the values of the resistor network and how to connect them. The termination network also achieves the 50Ω to 150Ω source impedance for V.35. For applications that require V.11 signals for clock and data instead of V.35 levels, omit the external termination networks. All of the differntial drivers, RS485, RS422,

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530
$TDEC_3$–$TDEC_0$	0000	0010	1110	0100	0101	1100	1101
SD(a)	tri–state	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
SD(b)	tri–state	tri–state	V.35+	RS422+	RS485+	RS422+	RS422+
TR(a)	tri–state	RS232	RS232	RS422–	RS485–	RS422–	RS422–
TR(b)	tri–state	tri–state	tri–state	RS422+	RS485+	RS422+	RS422+
RS(a)	tri–state	RS232	RS232	RS422–	RS485–	RS422–	RS422–
RS(b)	tri–state	tri–state	tri–state	RS422+	RS485+	RS422+	RS422+
RL(a)	tri–state	RS232	RS232	RS422–	RS485–	RS423	RS423
RL(b)	tri–state	tri–state	tri–state	RS422+	RS485+	tri–state	tri–state
LL(a)	tri–state	RS232	RS232	RS422–	RS485–	RS423	RS423
LL(b)	tri–state	tri–state	tri–state	RS422+	RS485+	tri–state	tri–state
ST(a)	tri–state	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
ST(b)	tri–state	tri–state	V.35+	RS422+	RS485+	RS422+	RS422+
TT(a)	tri–state	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
TT(b)	tri–state	tri–state	V.35+	RS422+	RS485+	RS422+	RS422+

Table 1. SP503 Drivers



For NET2 certified circuits, please contact the factory.

Figure 6. Typical Operating Circuit

and V.35 can operate up to 5Mbps.

Receivers

The **SP503** has seven (7) independant receivers which can be programmed for six (6) different interface modes. One of the seven (7) receivers (SCT) has an active–high enable control, as shown in the Mode Diagrams.

Control for the mode selection is done via a 4–bit control word that is independant from the driver control word. The coding for the drivers and receivers is identical. Therefore, if the modes for the drivers and receivers are supposed to be identical in the application, the control lines can be tied together.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows a summary of the electrical characteristics of the receivers in the different interface modes. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver output, a pull–up resistor of 100KΩ to +5V should be connected to the inverting input for a logic low, or the non–inverting input for a logic high. For single-ended receivers, a pull–down resistor to ground of 5KΩ is internally connected, which will ensure a logic high output.

There are three basic types of receivers — RS232, RS423, and RS485. The RS232 receiver is a single–ended input with a threshold of 0.8V to 2.4V. The RS232 receiver has an operating voltage range of ±15V and can receive signals up to 120Kbps. RS232 receivers are used in RS232 mode for all signal types, and in V.35 mode for control line signals.

The RS423 receivers are also single–ended but have an input threshold as low as ±200mV. The input impedance is guaranteed to be greater than 4KΩ, with an operating voltage range of ±7V. The RS423 receivers can operate up to 120Kbps. RS423 receivers are used for the IC signal in RS449 and EIA530 modes, as shown in *Table 2*.

The third type of receiver supports RS485, which is a differential interface mode. The RS485 receiver has an input impedance of 15KΩ and a differential threshold of ±200mV. Since the characteristics of an RS422 receiver are actually subsets of RS485, the receivers for RS422 requirements are identical to the RS485 receivers. RS422 receivers are used in RS449 and EIA530 for receiving clcok, data, and some control line signals. The RS485 receivers are also used for the V.35 mode. V.35 levels require the ±0.55V signals with a load of 100Ω. In order to meet the V.35 input impedance of 100Ω, the external termination network of *Figure 6* must be applied. The threshold of the V.35 receiver is

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530
$RDEC_3$–$RDEC_0$	0000	0010	1110	0100	0101	1100	1101
RD(a)	Undefined	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
RD(b)	Undefined	15KΩ to GND	V.35+	RS422+	RS485+	RS422+	RS422+
RT(a)	Undefined	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
RT(b)	Undefined	15KΩ to GND	V.35+	RS422+	RS485+	RS422+	RS422+
CS(a)	Undefined	RS232	RS232	RS422–	RS485–	RS422–	RS422–
CS(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	RS422+	RS422+
DM(a)	Undefined	RS232	RS232	RS422–	RS485–	RS422–	RS422–
DM(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	RS422+	RS422+
RR(a)	Undefined	RS232	RS232	RS422–	RS485–	RS422–	RS422–
RR(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	RS422+	RS422+
IC(a)	Undefined	RS232	RS232	RS422–	RS485–	RS423	RS423
IC(b)	Undefined	15KΩ to GND	15KΩ to GND	RS422+	RS485+	15KΩ to GND	15KΩ to GND
SCT(a)	Undefined	RS232	V.35–	RS422–	RS485–	RS422–	RS422–
SCT(b)	Undefined	15KΩ to GND	V.35+	RS422+	RS485+	RS422+	RS422+

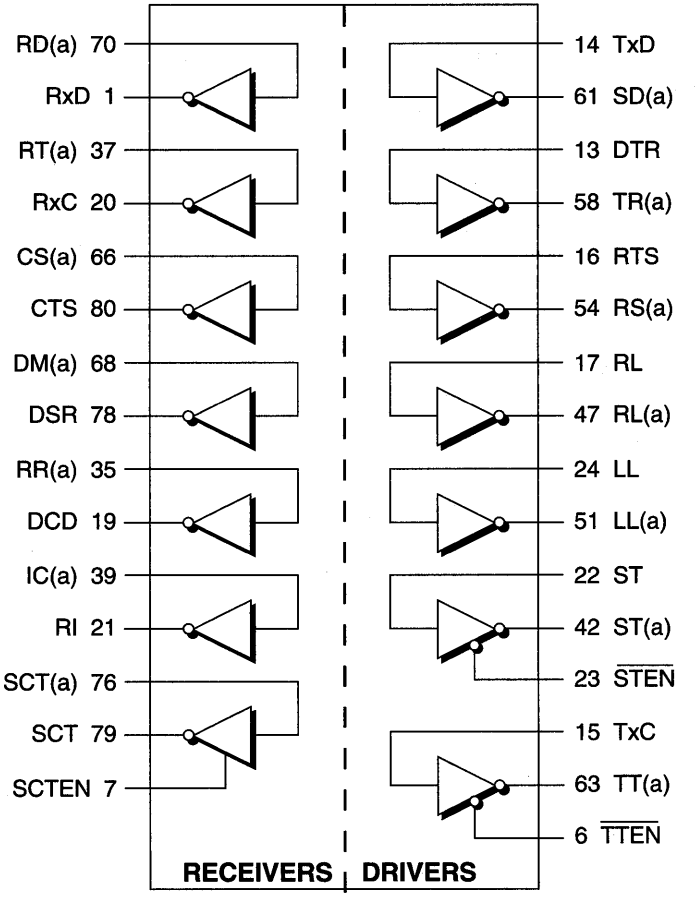
Table 2. SP503 Receivers

±200mV. The V.35 receivers can operate up to 5Mbps. All of the differential receivers can receive data up to 5Mbps.

Decoder

The **SP503** has the ability to change the interface mode of the drivers or receivers via an 8–bit switch. The decoder for the drivers and receivers is not latched; it is merely a combinational logic switch. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP503**. Undefined codes may represent other interface modes not specified or random outputs, (consult the factory for more information). The drivers are controlled with the data bits labeled $TDEC_3$–$TDEC_0$. The drivers can be put into tri-state mode by writing 0000 to the driver decode switch. The receivers are controlled with data bits $RDEC_3$–$RDEC_0$; the code 0000 written to the receivers will place the outputs in an undetermined state. All receivers, with the exception of SCT, do not have tri-state capability; the outputs will either be high or low depending upon the state of the receiver input.

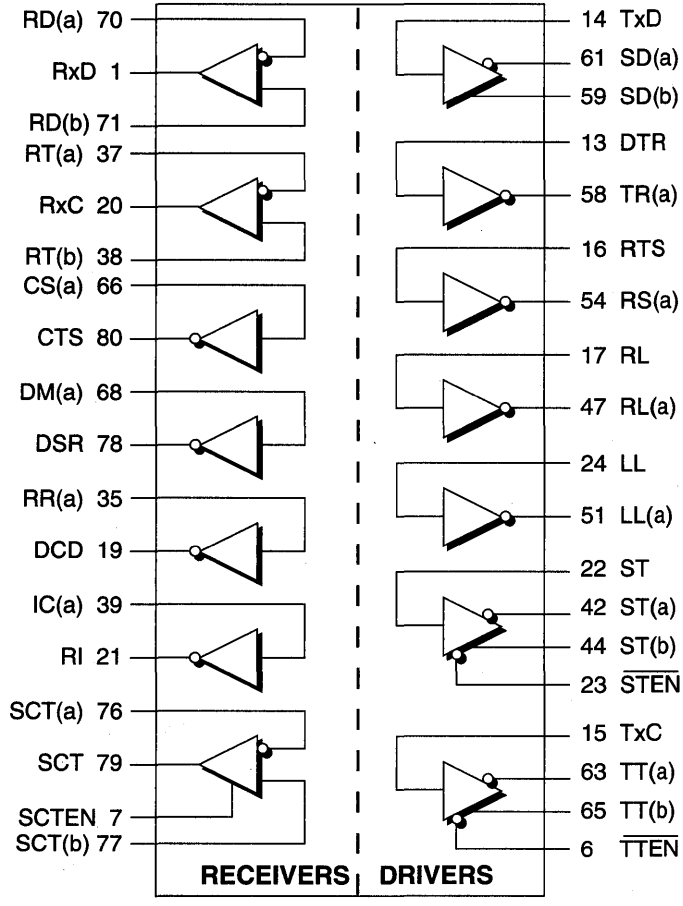
MODE: RS232							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	0	1	0	0	0	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 7. Mode Diagram — RS232

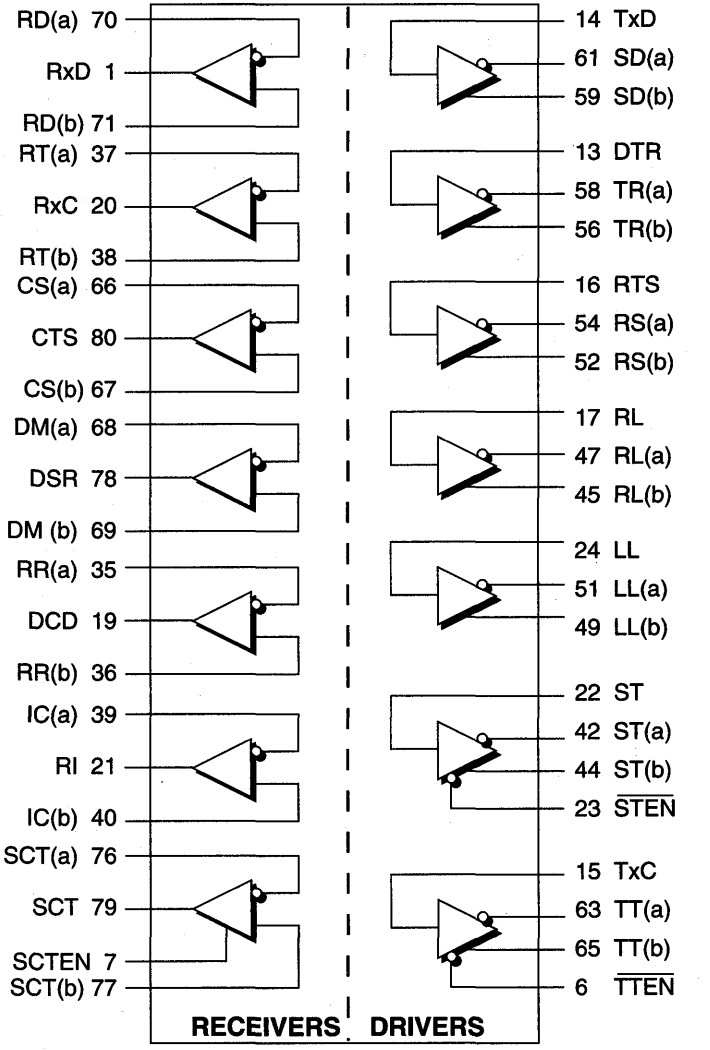
MODE: V.35							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	0	1	1	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 8. Mode Diagram — V.35

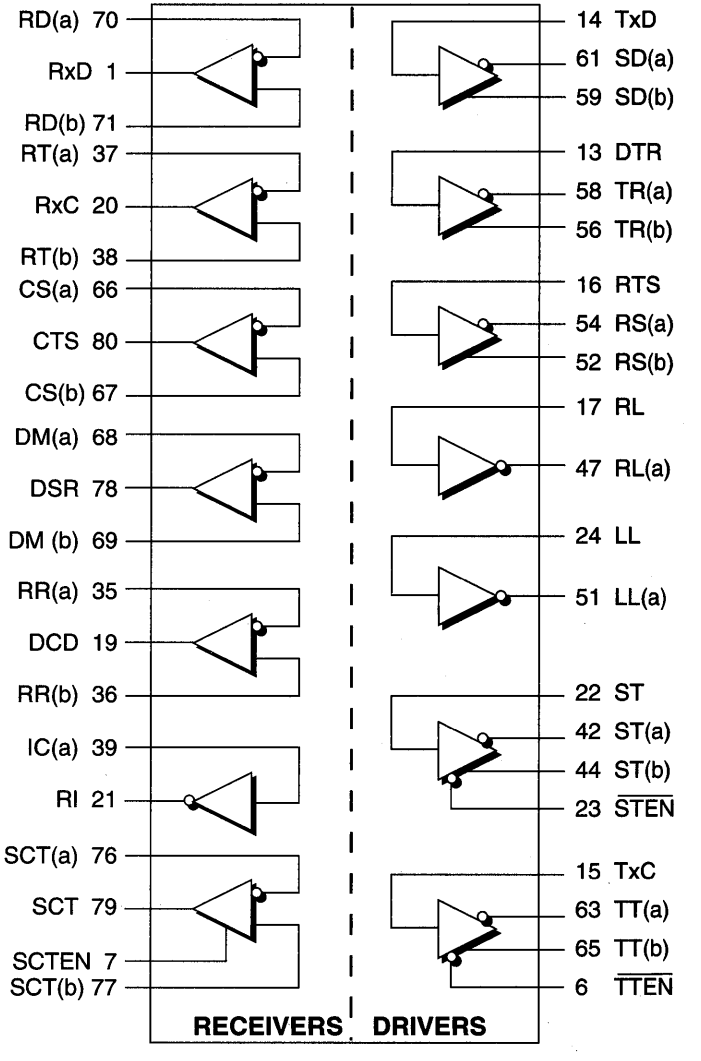
MODE: RS422							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	0	0	1	0	0



STEN	ST	TTEN	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 9. Mode Diagram — RS422

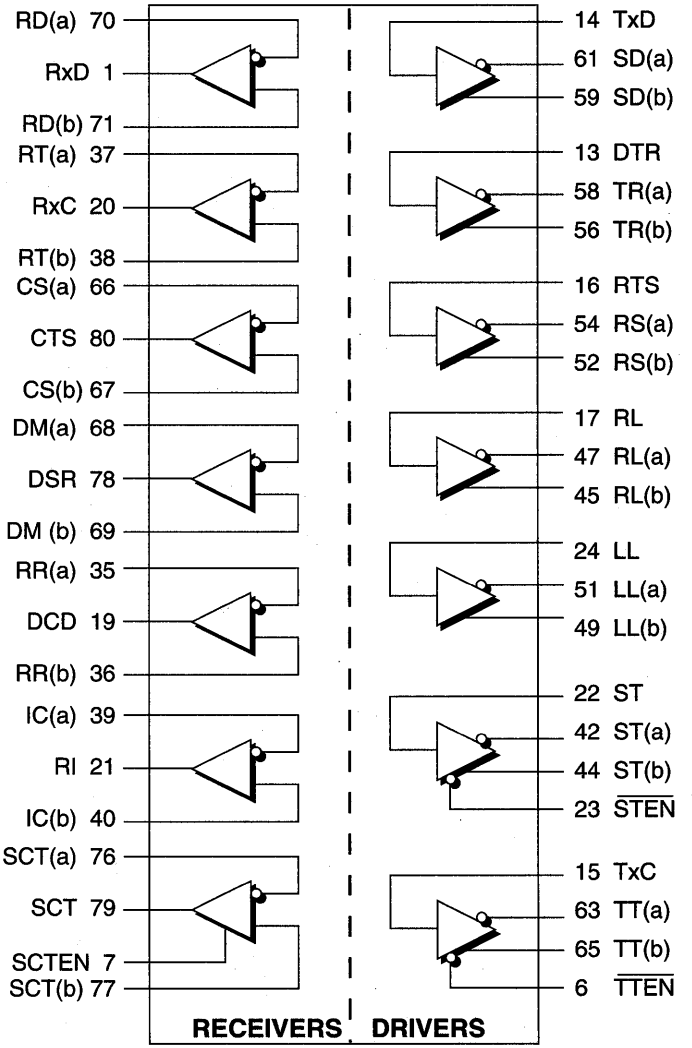
MODE: RS449							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	0	1	1	0	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 10. Mode Diagram — RS449

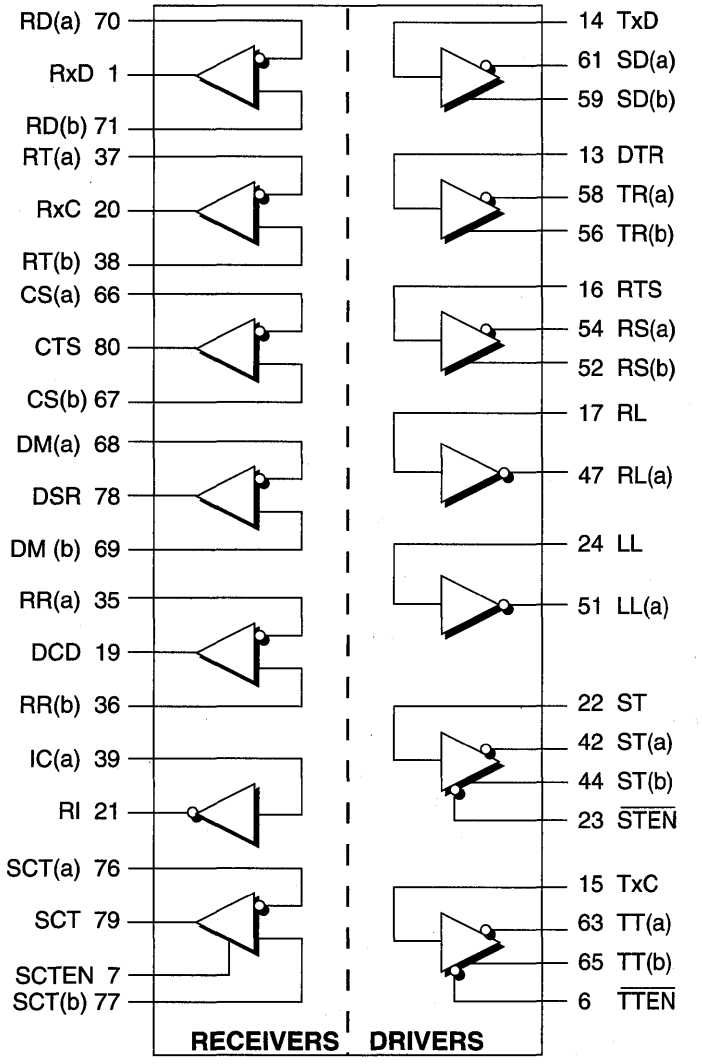
MODE: RS485							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	1	0	1	0	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 11. Mode Diagram — RS485

MODE: EIA 530							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	1	1	1	0	1



STEN	ST	TTEN	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 12. Mode Diagarm — EIA530

SP502/SP503 EVALUATION BOARD

The **SP502/SP503 Evaluation Board** (EB) Is designed to offer as much flexibility to the user as possible. Each board comes equipped with an 80-pin QFP Zero- Insertion socket to allow for testing of multiple devices. The control lines and Inputs and outputs of the device can be controlled either manually or via a data bus under software control. There is a 50-pin connector to allow for easy connection to an existing system via a ribbon cable. There are also open areas on the PC board to add additional clrcuitry to support application-specific requirements.

Manual Control

The SP502/SP503EB will support both the **SP502** or **SP503** multi-mode serial transceivers. When used for the **SP502,** disregard all notation on the board that Is In (brackets) . The **SP502** has a half-duplex connection between the RxT receiver and the TT driver. Due to this internal connection, the RxT receiver inputs can be accessed via the TT(a) and TT(b) pins. If the user needs separate receiver input test pins, jumpers JP1 and JP2 can be inserted to allow for separate receiver inputs located at SCT(a) and SCT(b). The corresponding TTL output for this receiver Is labeled as SCT. This test point Is tied to pin 79 of the **SP502** or **SP503**. Pin 7 of the evaluation board is connected to the DIP switch, and is labeled as (SCTEN). When used with the **SP502**, this pin should be switched to a low state. When the evaluation board is used with the **SP503**, pin 7 Is a tri-state control pin for the SCT receiver.

The transceiver I/O lines are brought out to test pins arranged in the same configuration as shown elsewhere in this data sheet. A top layer silk-screen shows the drivers and receivers to allow direct correlation to the data sheet. The transmitter and receiver decode bits are tied together and are brought out to a DIP switch for manual control of both the driver and receiver interface modes. Since the coding for the drivers and receivers is identical, the bits have been tied together. The DIP switch has 7 positions, four of which are reserved for the TDEC/RDEC control and the other three are used as tri-state control pins. The labels that are in [brackets] apply only to the **SP503**, If a logic one Is asserted the corresponding red LED will be lit; If a zero is asserted the corresponding red LED will not be lit.

Software Control

A 50-pin connector brings all the analog and digital I/O lines, V_{CC}, and GND to the edge of the card. This can be wired to the user's existing design via a ribbon cable, The pinout for the connector is described in the following section. When the evaluation board is operated under software control, the DIP switch should be set up so that all bits are low (all LEDs off). This will tie 20KΩ pulldown resistors from the inputs to ground and let the external system control the state of the control inputs.

Power and Ground Requirements

The evaluation board layout has been optimized for performance by using basic analog circuit techniques, The four charge-pump capacitors must be 22µF (16V) and be placed as close to the unit as possible; tantalum capacitors are suggested. The decoupling capacitor must be a minimum of 1µF; depending upon the operating environment, 10µF should be enough for worst case situations. The ground plane for the part must be solid, extending completely under the package, The power supplies for the device should be as accurate as possible; for rated performance ±5% is necessary. The power supply current will vary depending upon the selected mode, the amount of loading and the data rate. As a maximum, the user should reserve 200mA for I_{CC}. The worst-case operating mode is RS485 under full load of six (6) drivers supplying 1.6V to 54Ω loads. The power and ground inputs can be supplied through either the banana jacks on the evaluation board (Red = V_{CC} = +5V±5%; Black = GND) or through the connector.

For reference, the 80-pin QFP Socket is a TESCO part number FPQ-80-65-09A. The 50-pin connector is an AMP part number 749075-5.

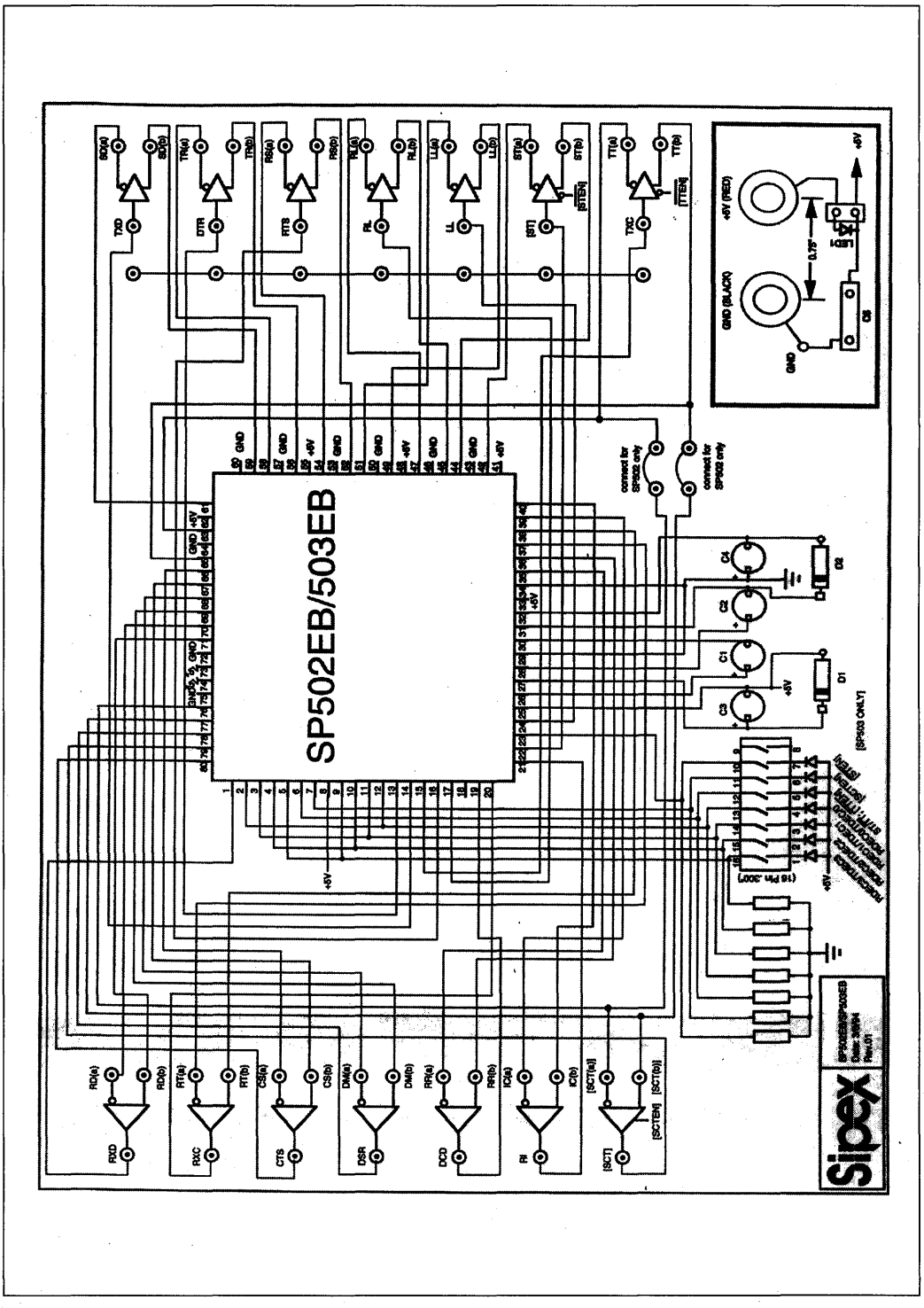


Figure 13. SP502/503 Evaluation Board Schematic

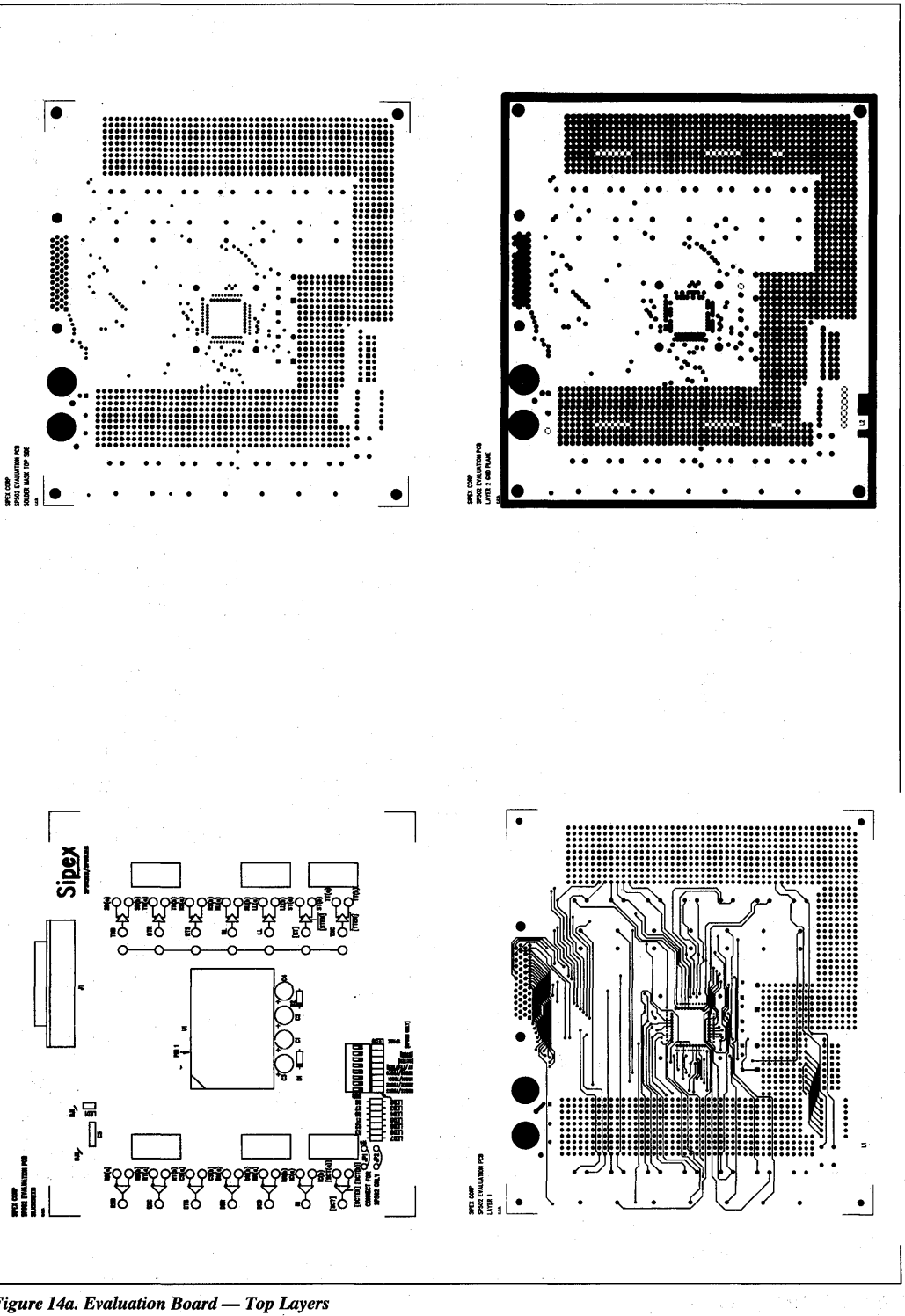


Figure 14a. Evaluation Board — Top Layers

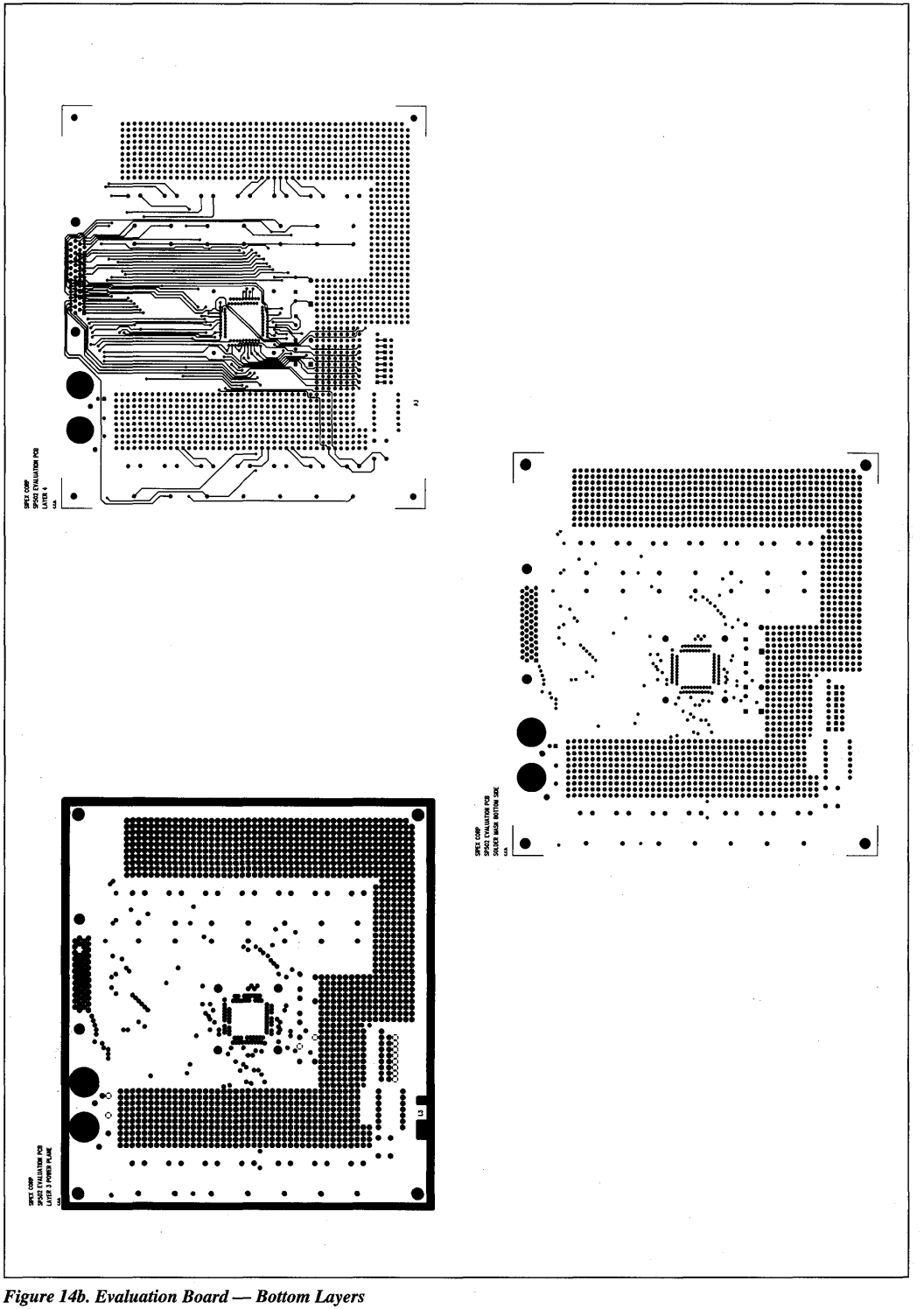


Figure 14b. Evaluation Board — Bottom Layers

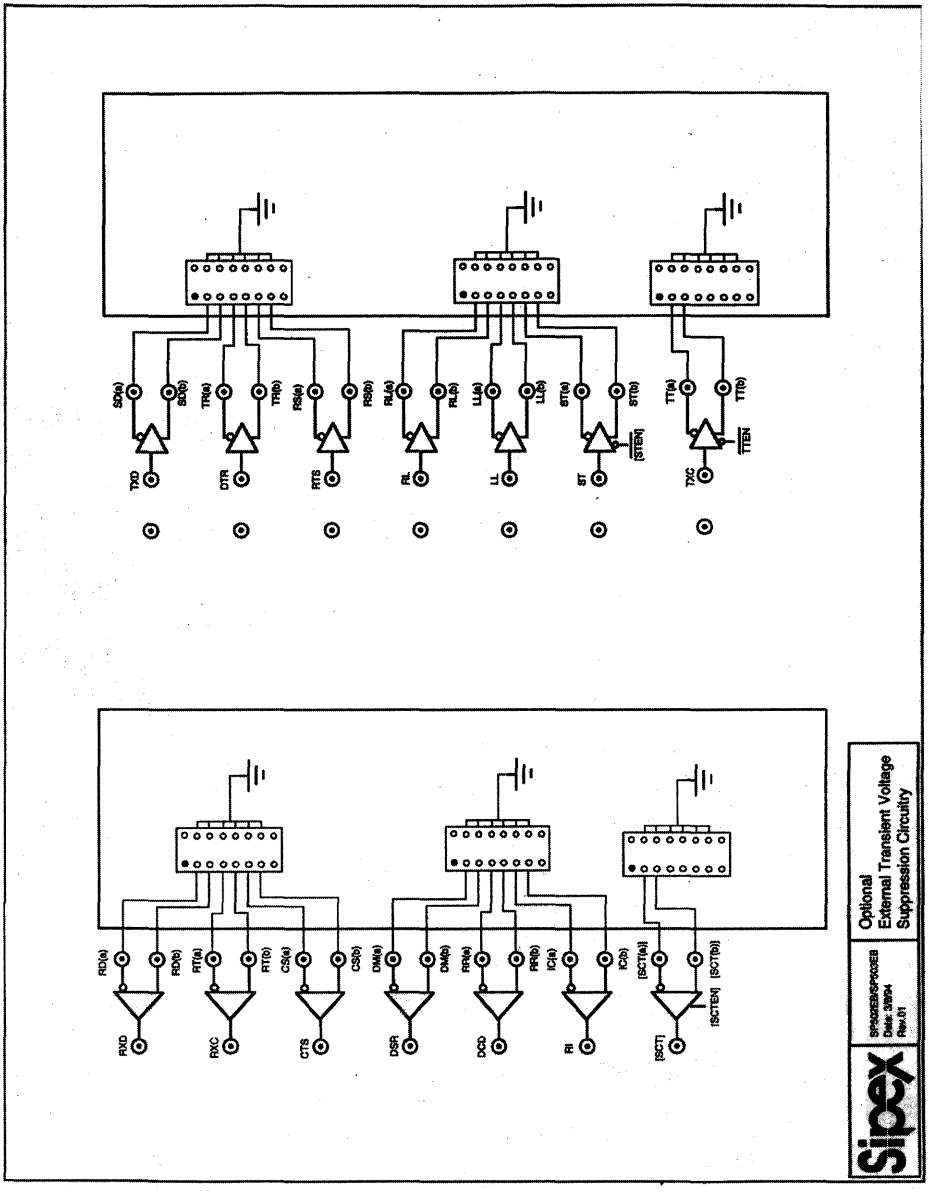
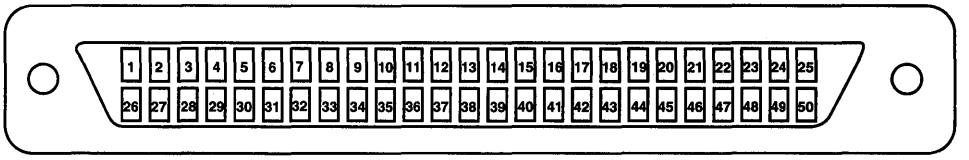
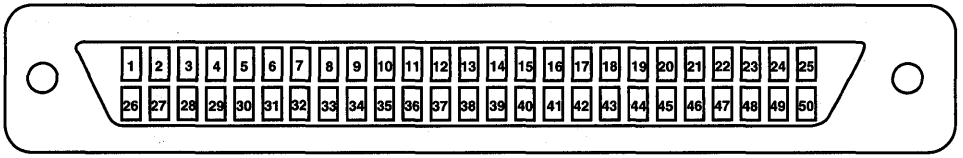


Figure 15. External Transient Suppressors



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
01	TxD (pin 14) –TTL Input – Transmit data; source for SD(a) and SD(b) outputs.
02	DTR (pin 13) – TTL Input – Data terminal ready: source for TR(a) and TR(b) outputs.
03	ST/$\overline{TT}$ (pin 6) –TTL Input – ST/$\overline{TT}$ select pin; enables ST drivers and disables TT drivers when high. Disables ST drivers and enables TT drivers when low.
04	DEC_3/$RDEC_3$ (pin 5) – TTL Input – Transmitter/Receiver decode register.
05	$TDEC_2$/$RDEC_2$ (pin 4) – TTL Input – Transmitter/Receiver decode register.
06	$TDEC_1$/$RDEC_1$ (pin 3) – TTL Input – Transmitter/Receiver decode register.
07	$TDEC_0$/$RDEC_0$ (pin 2) – TTL Input – Transmitter/Receiver decode register.
08	RxD (pin 1) – TTL Output – Receive data; sourced from RD(a) and RD)b) inputs.
09	CTS (pin 80) – TTL Output – Clear to send; sourced from CS(a) and CS(b) inputs.
10	RxT (pin 79) – TTL Output – RxT; sourced from TT(a), TT(b) inputs.
11	DSR (pin 78) – TTL Output – Data set ready; sourced from DM(a) and DM(b) inputs.
12	RD(b) (pin 71) – Analog In – Receive data, non–inverted; source for RxD.
13	RD(a) (pin 70) – Analog In – Receive data, inverted: source for RxD.
14	DM(b) (pin 69) – Analog In – Data mode, non–inverted; source for DSR.
15	DM(a) (pin 68) – Analog In – Data mode, inverted; source for DSR.
16	CS(b) (pin 67) – Analog In – Clear to send; non–inverted; source for CTS.
17	CS(a) (pin 66) – Analog In – Clear to send, inverted; source for CTS.
18	TT(b) (pin 65) – Analog In or Out – Terminal timing, non–inverted: sourced to RxT or from TxC input.
19	TT(a) (pin 63) – Analog In or Out – Terminal timing; inverted: sourced to RxT or from TxC input.
20	TR(a) (pin 58) – Analog Out – Terminal ready, inverted; sourced from DTR.
21	TR(b) (pin 56) – Analog Out – Terminal ready; non–inverted; sourced from DTR.
22	SD(a) (pin 61) – Analog Out – Send data, inverted; sourced from TxD.
23	SD(b) (pin 59) – Analog Out – Send data; non–inverted; sourced from TxD.
24	RS(a) (pin 54) – Analog Out – Ready to send; inverted; sourced from RTS.
25	RS(b) (pin 52) – Analog Out – Ready to send, non–inverted; sourced from RTS.



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
26	ST (pin 22) – TTL Input – Send Timing; source for ST(a) and ST(b) outputs. SP503 only.
27	$\overline{\text{STEN}}$ (pin 23) – TTL Input — Driver enable control pin; active low. SP503 only,
28	SCT(a) (pin 76) – Analog Input – Inverting; input for SCT receiver; SP503 only.
29	SCT(b) (pin 77) – Analog Input – Non–inverting; input for SCT receiver. SP503 only.
30	V_{CC} — +5V for all circuitry.
31	GND — signal and power ground.
32	LL(a) (pin 51) – Analog Out – Local loopback, inverted; sourced from LL.
33	LL(b) (pin 49) – Analog Out – Local loopback, non–inverted sourced from LL.
34	RL(a) (pin 47) – Analog Out – Remote loopback; inverted; sourced from RL.
35	RL(b) (pin 45) – Analog Out – Remote loopback; non–inverted; sourced from RL.
36	ST(b) (pin 44) – Analog Out – Send timing, non–inverted; sourced from TxC.
37	ST(a) (pin 42) – Analog Output –Send timing, inverted; sourced from TxC.
38	IC(b) (pin 40) – Analog In – Incoming call; non–inverted; source for RI.
39	IC(a) (pin 39) – Analog In – Incoming call; inverted; source for RI.
40	RT(b) (pin 38) – Analog In – Receive timing, non–inverted; source for RxC.
41	RT(a) (pin 37) – Analog In – Receive timing; inverted; source from RxC.
42	RR(b) (pin 36) – Analog In – Receiver ready; non–inverted; source for DCD.
43	RR(a) (pin 35) – Analog In – Receiver ready; inverted; source for DCD.
44	LL (pin 24) – TTL Input – Local loopback; source for LL(a) and LL(b) outputs.
45	RI (pin 21) – Output – Ring indicator; sourced from IC(a) and IC(b) inputs.
46	RxC (pin 20) – TTL Output – Receive clock; sourced from RT(a) and RT(b) inputs.
47	DCD (pin 19) – TTL Output – Data carrier detect; sourced from RR(a) and RR(b) inputs.
48	RL (pin 17) – Analog Out – Remote loopback; source for RL(a) and RL(b) outputs.
49	RTS (pin 16) – TTL Input – Ready to send; source for RS(a) and RS(b) outputs.
50	TxC (pin 15) – TTL Input – Transmit clock; common TTL input for both ST and TT driver outputs.

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP503CF	0°C to +70°C	80–pin QFP

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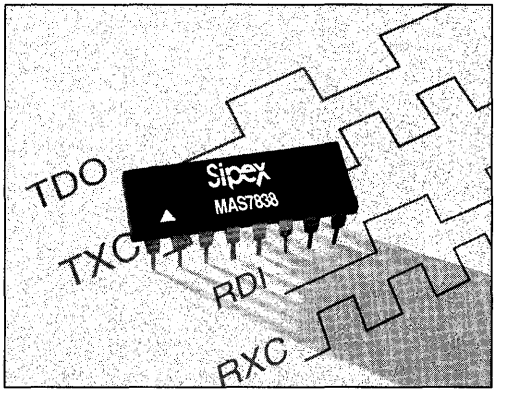
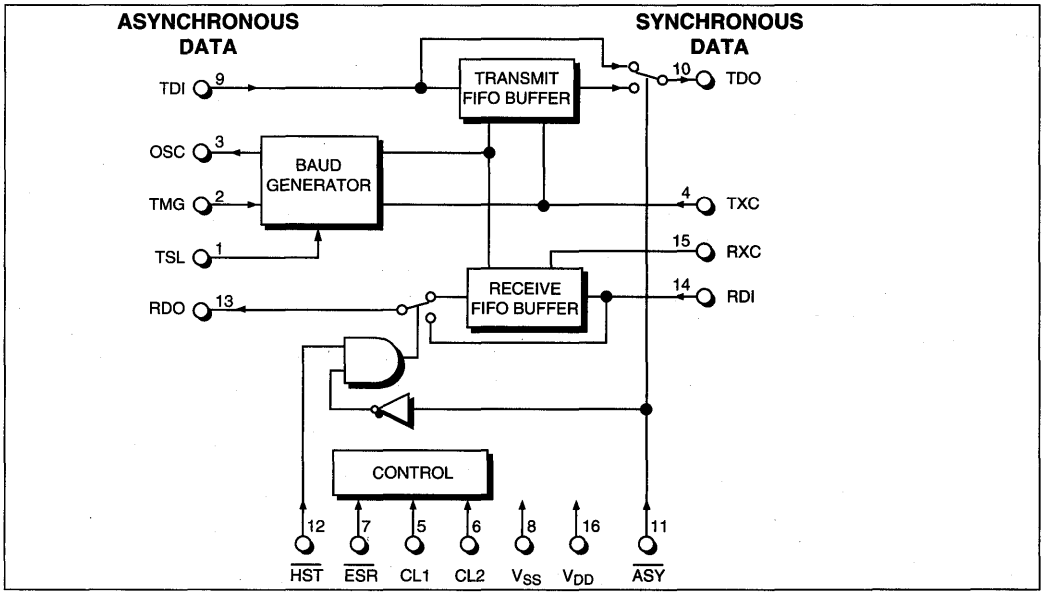
CMOS Asynchronous to Synchronous Converter

- Interfaces an asynchronous channel to a synchronous channel
- Implements CCITT recommendation V.22
- 64 kbit/s transmission rate
- 25mW typical power dissipation
- Single +5V supply



DESCRIPTION...

The **MAS7838** implements a duplex synchronous to asynchronous converter in a single IC. It converts asynchronous start/stop characters to synchronous character format. The receiver channel converts incoming synchronous data to asynchronous start/stop character format with start/stop bit insertion. Both conversions conform to CCITT V.22 recommendations. The **MAS7838** operates at any frequency to its rated maximum.



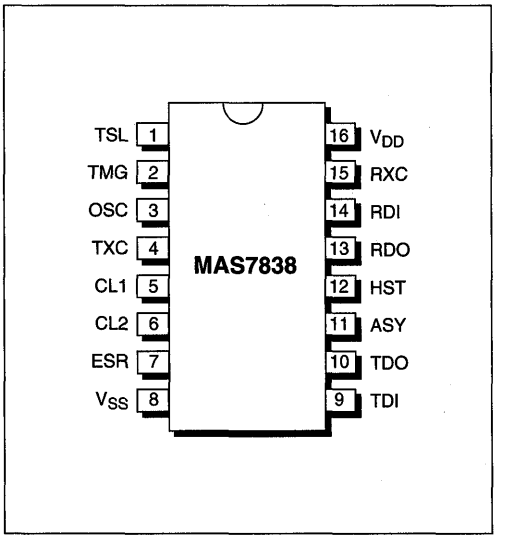
CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

V_{DD} = +5V, V_{SS}=0V; 0°C to +70°C

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DATA OUTPUT					
Output Voltage					
V_{OL}			0.4	Volts	I_{OL}= 0.6mA
V_{OH}	4.6			Volts	I_{OM}= 0.4mA
DATA INPUT					
Input Voltage					
V_{IL}	–0.5		1.1	Volts	
V_{IH}	3.5		5	Volts	
Leakage Current		–100		pA	I_L
Capacitance		5		pF	CI
Pull–Up Resistor		350		kohms	$R_{pull-up}$; V_{IN}=0.4V
		850		kohms	$R_{pull-up}$; V_{IN}=2.5V
LOGIC TRANSITION					
Low–to–High		20		ns	t_R; C_L=10pF
High–to–Low		20		ns	t_F; C_L=10pF
POWER REQUIREMENTS					
Supply Voltage	4.5	+5	5.5	Volts	V_{DD}
Supply Current		4	6	mA	I_{DD}
Power Dissipation		20	30	mW	
ENVIRONMENTAL AND MECHANICAL					
Temperature Range					
Operating	0		+70	°C	
Storage	–25		+85	°C	
Package	16–pin Plastic DIP				

PINOUT...



PIN DESCRIPTION...

Pin 1 — TSL — Timing Select — Selects between internally or externally generated timing signals to be used for internal asynchronous timing reference. A logic '0" selects sampling timing from Pin 2. A logic "1" inserts a divider between the signal on Pin 2 and the timing reference circuit. This divider automatically divides the signal on Pin 2 by 256...8,192, depending on the frequency of the signal present on Pin 2. The divider frequency is selected such that the internal timing reference is always 16x the asynchronous transmit clock bit rate.

Pin 2 — TMG — Timing Input — Squarewave timing signal input; If TSL=0, this signal must be 16x the synchronous transmit clock bit rate. IF TSL=1, this signal can be 256...8,192 times the synchronous transmit clock bit rate, with a maximum frequency of 10MHz.

Pin 3 — OSC — Oscillator Input — Output from crystal oscillator. If one is used, it is connected between pins 2 and 3. The crystal frequency is selected to be 16x the synchronous data bit rate. If the crystal frequency is less than 5MHz, 22pF capacitors to ground must be connected between pin 2 and ground, and pin 3 and ground. (See *Figure 1*)

Pin 4 — TXC — Synchronous Transmit Timing — Squarewave timing signal input for synchronous transmit timing. The transmitted data output, TDO, is synchronized to the rising edge of TXC. The duty cycle of TXC must be 50%±5%.

Pins 5 and 6 — CL1/CL2 — Character Length — The total character length including one start bit , one stop bit, and possible parity bit, is selected by logic levels on CL1 and CL2 per *Table 1*.

Pin 7 — $\overline{\text{ESR}}$ — Extended Signalling Rate — The tolerance of the synchronous bit rate can be extended. With pin 7 at a logic "1", TXC can vary from –2.5% to +1.0%. With pin 7 at a logic "0", TXC can vary from –2.5% to +2.3%.

Pin 8 — V_{SS} — Ground

Pin 9 — TDI — Transmitted Data Input — Input data to be transmitted is applied to this pin. A logic "0" is a space, start or break signal; a logic "1" is a mark or stop bit.

Pin 10 — TDO — Transmitted Data Output — The output data is synchronized to the leading edge of the synchronous timing signal TXC (pin 4). A logic "0" is a space; a logic "1" is a mark.

Pin 11 — $\overline{\text{ASY}}$ — Asynchronous Mode — A logic "0" selects the asynchronous transmission mode; a logic "1" selects the synchronous transmission mode. In the synchronous transmission mode, the converter is totally bypassed in both directions, such that TDI = TDO and RDI = RDO.

CHARACTER LENGTH TRUTH TABLE

CL2	CL1	Character Length
0	1	8 bits
0	0	9 bits
1	1	10 bits
1	0	11 bits

Table 1. Character Length Truth Table

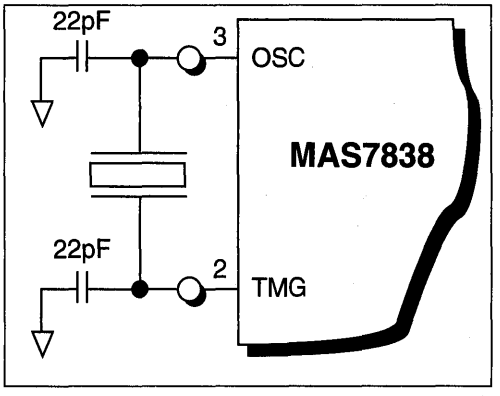


Figure 1. Crystal Oscillator Circuit Diagram

Pin 12 — $\overline{\text{HST}}$ — Higher Speed Signalling Timing — Selects between normal (CCITT V.22 or Bell 212) synchronous–to–asynchronous conversion, and an overspeed asynchronous mode. TXC and RXC must be 1-2% higher than the normal bit rate to allow some overspeed in the asynchronous data. On the receiver side, the RX buffer is deleted, and the synchronous data RDI is connected directly to the asynchronous output RDO. A logic "0" selects the higher speed synchronous timing mode; a logic "1" selects normal conversion.

Pin 13 — RDO — Received Data Output — RDO is the received data converted back to asynchronous mode. Logic "0" is a space, start or break signal; logic "1" is a mark or stop bit.

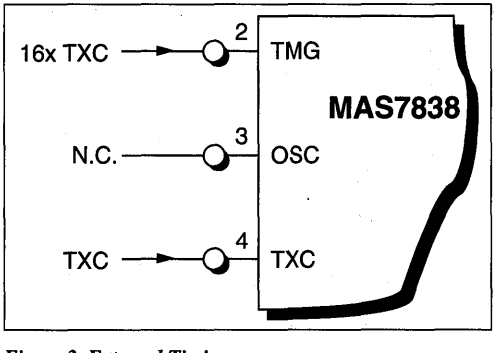


Figure 2. External Timing

Pin 14 — RDI — Received Data Input — The received data must be synchronized to the received timing RXC from the synchronous channel, pin 15. A logic "0" is a space; a logic "1" is a mark.

Pin 15 — RXC — Received Timing — Received squarewave timing from the synchronous channel. The received data RDI must be synchronized to the rising edge of RXC. (See Figure 7).

Pin 16 — V_{DD} — +5V±0.5V

FEATURES...

The **MAS7838** is a single chip implementation of a duplex synchronous to asynchronous converter. It converts asynchronous start/stop characters to synchronous character format, with stop bit deletion when required by CCITT V.22. The receiver channel converts the incoming synchronous data to asynchronous start/stop character format with stop bit insertion when required by CCITT V.22. The **MAS7838** implements the data modes for the synchronous interface as specified in V.22, chapter 1.2. Operating frequency can be configured at any speed up to a 64 kbit/s device maximum. The **MAS7838** is supplied in a 16-pin plastic DIP. It is specified over the 0°C to +70°C commercial operating temperature range.

USING THE MAS7838...

Timing Selection

The **MAS7838** requires proper synchronous clock signals to function correctly. These signals may be generated by either a crystal oscillator connected to pins 2 and 3, or, if the proper signals are available in the system, can be supplied from an external source. In either case, clock signals must have a 50%±5% duty cycle. The clock signal, TXC, is used by the **MAS7838** for 1) shifting data out from the transmit buffer to the transmitted data output (TDO), 2) shifting data into the receive buffer from the received data input (RDI), and 3) detection of the bit rate in order to adjust the internal baud rate generator (with TSL=1 only; see below).

To use a crystal oscillator connected to pins 2 and 3, TSL (pin 1) should be at a logic "0". Select the crystal frequency to be 16x the required synchronous data bit rate (TXC) so that the asynchronous data stream can be sampled at the proper speed. As shown in *Figure 1*, if the crystal frequency is less than 5MHz, 22pF capacitors should be tied between pin 2 and ground, and pin 3 and ground.

To use a synchronous clock signal generated externally, TSL (pin 1) should be at a logic "1". The squarewave input to the TMG/Timing Input (pin 2) must be at any frequency between 256x and 8,192x the required synchronous data bit rate (TXC). With TLS=1, the clock signal is passed through an internal divider that automatically determines the input frequency and programs itself to generate the appropriate internal clock signal. The squarewave input to the TMG/Timing Input can be at any frequency up to a 10MHz maximum.

Asynchronous–to–Synchronous Conversion

The asynchronous start/stop character is read in to the transmit buffer through the transmitted data input (TDI). When the character is available, the databits are transmitted as TDO with the synchronous timing signal TXC. The bit rate of TDI must be the same as the TDO bit rate, within the tolerance set by the state of $\overline{ESR}$ ($\overline{ESR}$=1, –2.5% to +1.0%; $\overline{ESR}$=0, –2.5% to +2.3%, extended). If TDI is slower than TDO, the transmitter adds extra stop bits to the synchronous data stream. An overspeed condition causes one stop bit in every eighth character maximum in the synchronous output data (TDO). When the extended data rate is used ($\overline{ESR}$=0) every fourth stop bit may be deleted.

Break signals are detected when at least M bits of start polarity are received, where M is the character length as programmed by CL1/CL2 (pins 5 and 6). When the break is detected, the **MAS7838** sends 2M+3 bits of start polarity to TDO. If the break signal is longer than 2M+3 bits, then all bits are transferred to TDO. After a break signal, at least 2M bits of stop polarity must be transmitted before sending additional data.

Synchronous–to–Asynchronous Conversion

The synchronous data received by the received data input (RDI) is buffered to recognize the start and stop bits. If a missing stop bit is detected, it is added to the RDO, and the stop bits are shortened

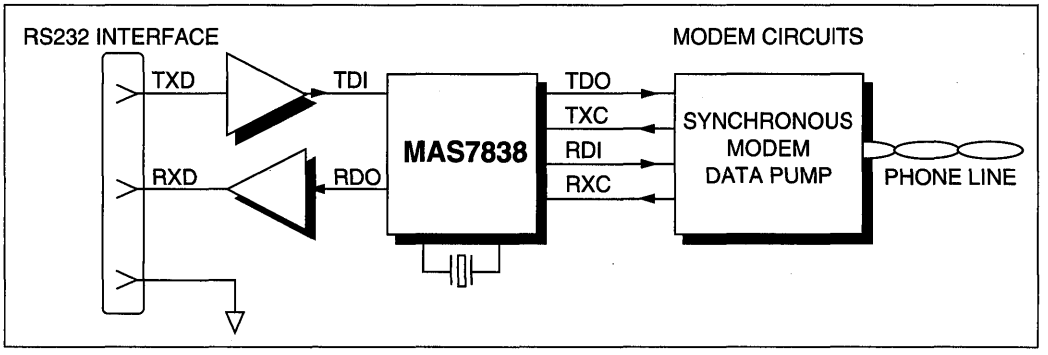


Figure 3. Synchronous Modem to Asynchronous Interface

12.5% if $\overline{ESR}$=1, or 25% if $\overline{ESR}$=0 during each character. When the receiver receives at least 2M+3 bits of start polarity, no stops bits are added to RDO. This enables the break signal to go through the buffer unchanged.

Higher–Speed Conversion Mode

If the overspeed asynchronous timing mode is used ($\overline{HST}$=0), the synchronous timing signal frequencies TXC and RXC are increased by 1-2%. In this case, there is no need to delete any stop bits in the transmitter buffer and break signals go through the buffer unchanged. On the receiver side, the synchronous data RDI is transferred directly to the asynchronous output RDO with RXC.

Typical Applications

The **MAS7838** is intended for applications where an asynchronous and synchronous data source must be connected together. A typical example is that of a data modem where the terminal interface of the modem is asynchronous, but the modem datapump operates synchronously. *Figure 3* depicts the typical interconnection for such an application. In other typical applications, a USART is used as a data source. This configuration is depicted in *Figure 4*. A third application for the **MAS7838** is that of a data multiplexer/demultiplexer. By using the **MAS7838** to convert the asynchronous data to synchronous, a synchronous multiplexer can be used, greatly reducing the required sampling rate to only one sample per databit. (See *Figure 5*.)

A final application example for a simple synchronous–to–asynchronous converter is shown in *Figure 6*. The **MAS7838** selects the conversion speed to that of that of the synchronized data clock and performs the conversion. The **SIPEX SP208** provides the RS232 drivers and receivers for interfacing with the data bus. A generic 78L05 whose input is connected to the

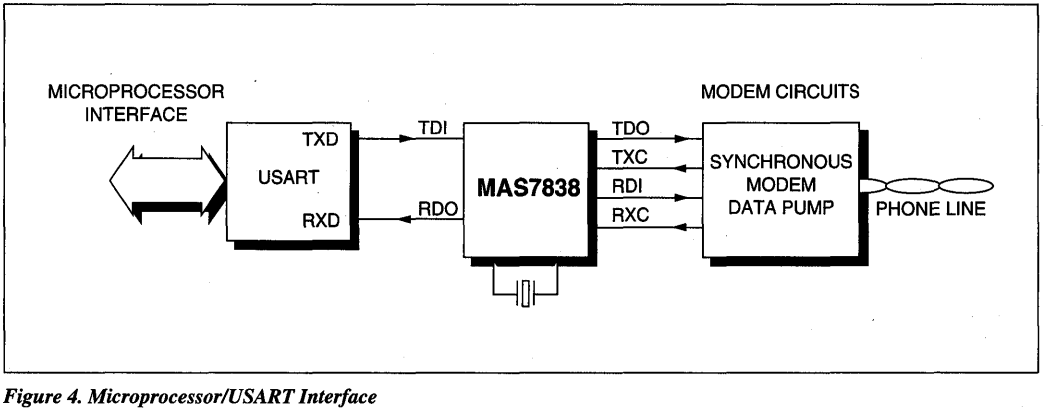


Figure 4. Microprocessor/USART Interface

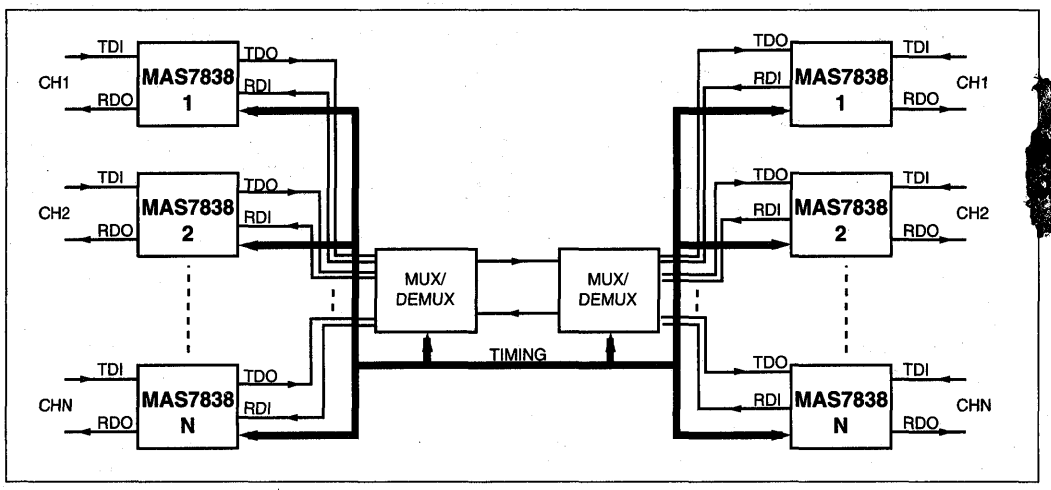


Figure 5. Data Multiplexer/Demultiplexer

+12V on pin 9 of the DB25 connector provides the +5V power supply required by both the **MAS7838** and the **SP208**. A crystal frequency of 4.91MHz converts to 19.2Kb/s or a sub–multiple of the synchronous data rate (9.6Kbps, 4.8Kbps, 2.4Kbps, etc.). Two 1N4001 diodes protect the external RTS control circuitry if the RTS is enabled by S1. When JP1 is removed, the converter is transparent in the synchronous mode, and no conversion will take place. In the configuration shown, the data word is strapped for 10 bits.

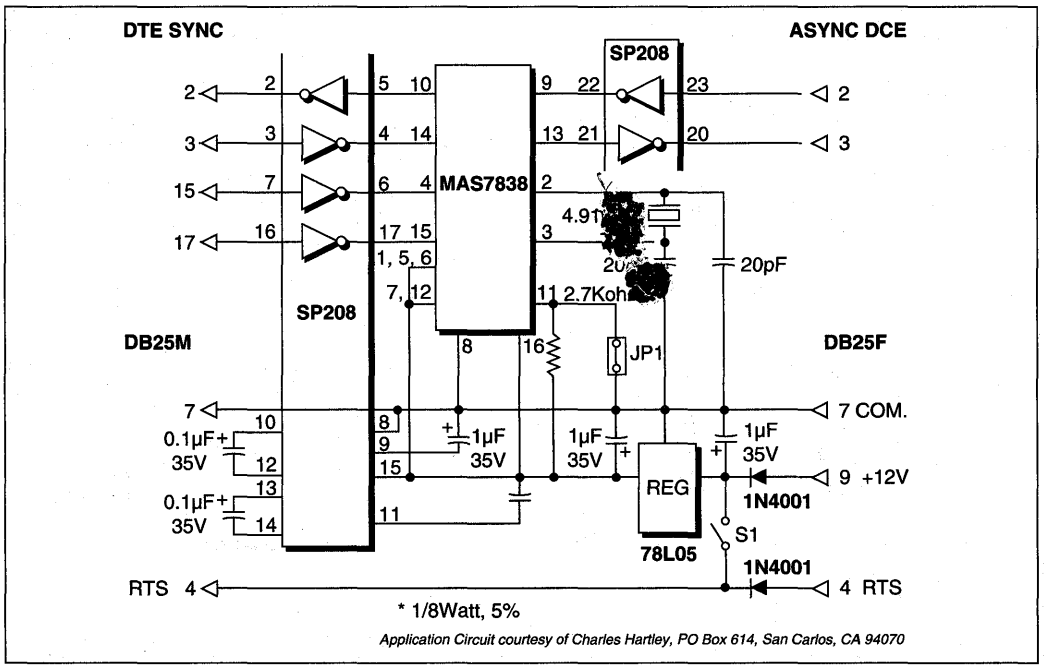


Figure 6. RS232 Sync–to–Async Converter

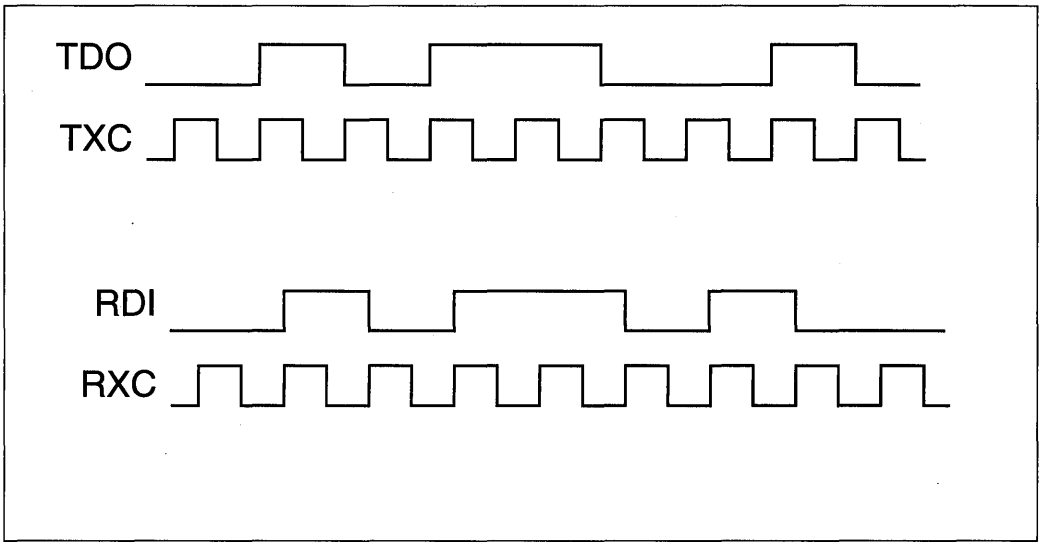


Figure 7. Transmit and Receive Timing

ORDERING INFORMATION

CMOS Synchronous to Asynchronous Converter

Model	Package
MAS7838CN	16–pin Plastic DIP

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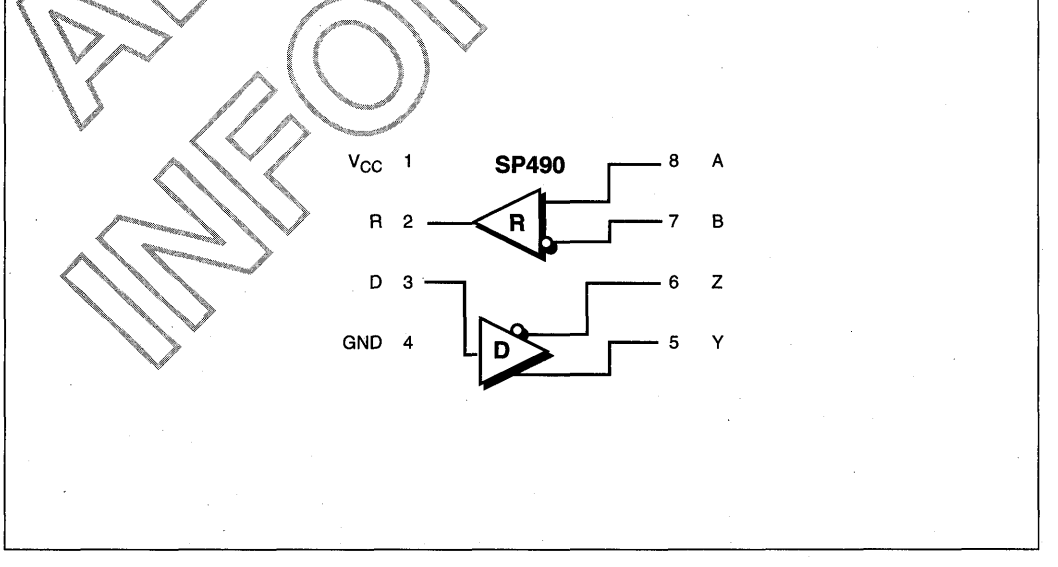
RS485 Line Driver/Receiver Pair

- RS485 and RS422
- +5V Only Power Supply Required
- Low Power — I_{CC} = 300µA Typical
- –7V to +12V Common Mode Range
- 70mV Typical Input Hysteresis
- Short–Circuit Protected
- Pin Compatible with LTC490 and SN75179

DESCRIPTION...

The **SP490 is a** low–power differential line driver/receiver meeting RS485 and RS422 standards up to 5Mbps. The **SP490 features** ±200mV input sensitivity, a wide common mode range and input hysteresis. The **SP490** is available in 8–pin plastic DIP and SOIC packages, for operation over the commercial and industrial temperature ranges.



SPECIFICATIONS

V_{CC} = 5V±5%; typicals at 25°C; 0°C ≤ T_A ≤ +70°C unless otherwise noted.

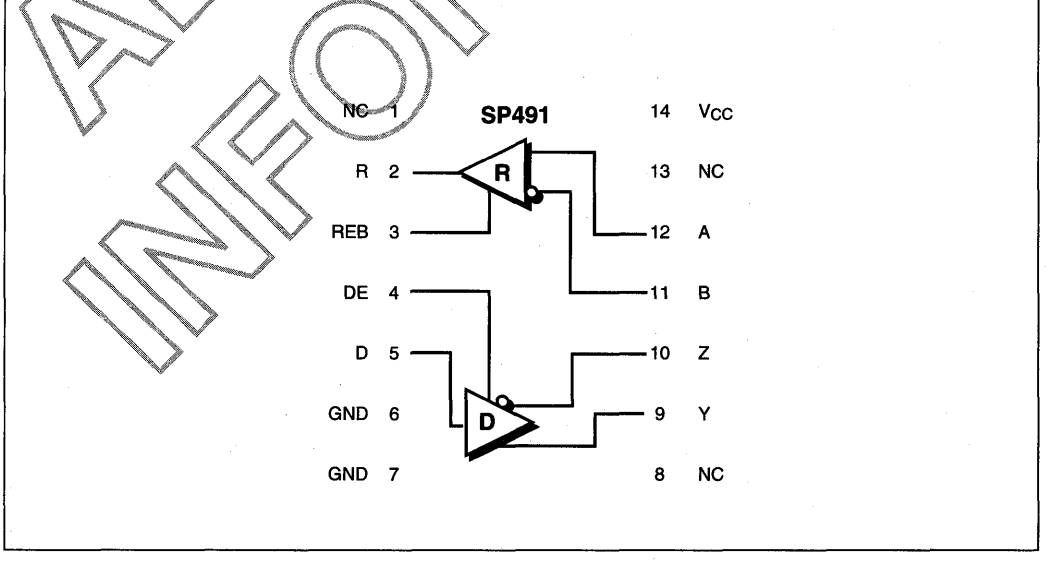
PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DRIVER					
Input Voltage					
V_{IL}			0.8	Volts	D
V_{IH}	2.0			Volts	
Input Current			±2	µA	
Output					
Differential Voltage			5	Volts	I_O = 0; unloaded
	2			Volts	R_L = 50 ohms (RS422)
	1.5	2	5	Volts	R_L = 27 ohms (RS485)
Change in Output Magnitude			0.2	Volts	for complementary output state
					R_L = 27 ohms or 50 ohms
Common Mode Output Voltage		2.3	3	Volts	R_L = 27 ohms or 50 ohms
Change in Common Mode Output Magnitude			0.2	Volts	for complementary output state
					RL = 27 ohms or 50 ohms
Short–circuit Current					
VOH			250	mA	–7V ≤VO ≤ +12V
VOL			250	mA	–7V ≤VO ≤ +12V
RECEIVER					
Diff. Input Threshold Voltage	–0.2		±0.2	Volts	–7V ≤V_{CM} ≤ +12V
Input Current			+1.0	mA	V_{CC} = 0V or 5.25V; V_{IN} = +12V
			–0.8	mA	V_{CC} = 0V or 5.25V; V_{IN} = _7V
Input Hysteresis		70		mV	V_{CM} = 0V
Input Resistance	12			KΩ	–7V ≤V_{CM} ≤ +12V
Output Voltage					
V_{OH}	3.5			Volts	I_O = –4mA; V_{ID} = +0.2V
V_{OL}			0.4	Volts	I_O = +4mA; V_{ID} = –0.2V
POWER REQUIREMENTS					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		300	500	µA	No load, D = GND or V_{CC}
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
–C	0		+70	°C	
–E	–40		+85	°C	
Storage Temperature	–65		+150	°C	
Package					
_S	8–pin Plastic DIP				
_T	8–pin SOIC				

RS485 Driver/Receiver Pair

- RS485 and RS422
- +5V Only Power Supply Required
- Low Power — I_{CC} = 300µA Typical
- Glitch–Free Power Up/Down
- –7V to +12V Common Mode Range
- 70mV Typical Input Hysteresis
- Short–Circuit Protected
- Pin Compatible with LTC491 and SN75180

DESCRIPTION...

The **SP491** is a low–power differential line driver/receiver meeting RS485 and RS422 standards up to 5Mbps. The **SP491 features** ±200mV input sensitivity, a wide common mode range and input hysteresis. The **SP491** features tri–state control of both the driver and receiver. The **SP491** is available in a 14–pin plastic DIP and SOIC packages for operation over the commerical and industrial temperature ranges.



SPECIFICATIONS

V_{CC} = 5V±5%; typicals at 25°C; 0°C ≤ T_A ≤ +70°C unless otherwise noted.

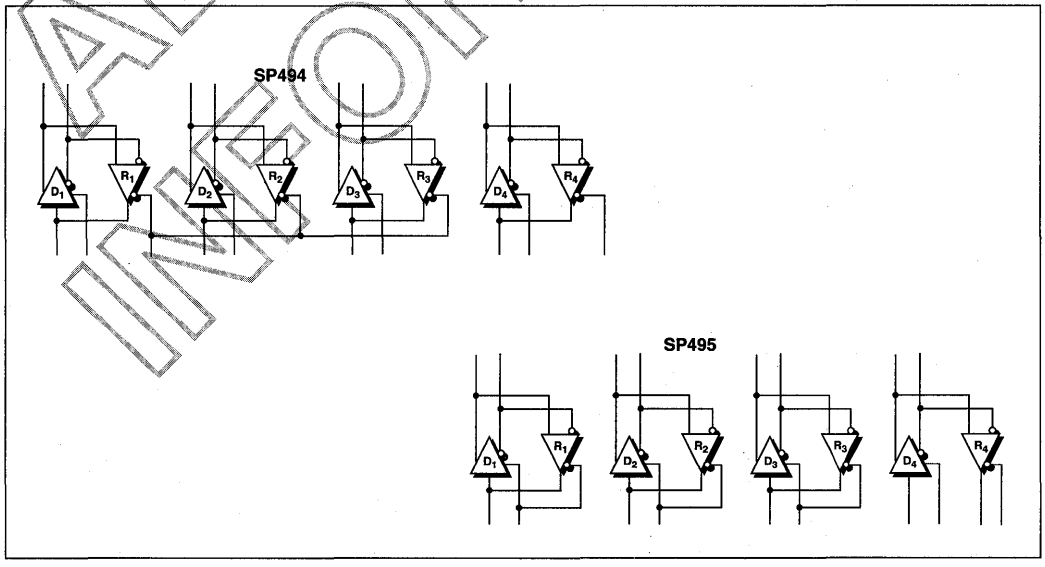
PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DRIVER					
Input Voltage					D
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Input Current			±2	µA	
Driver Output					
Differential Voltage			5	Volts	I_O = 0; unloaded
	2			Volts	R_L = 50 ohms (RS422)
	1.5	2	5	Volts	R_L = 27 ohms (RS485)
Change in Output Magnitude			0.2	Volts	for complementary output state
					R_L = 27 ohms or 50 ohms
Common Mode Output Voltage		2.3	3	Volts	R_L = 27 ohms or 50 ohms
Change in Common Mode			0.2	Volts	for complementary output state
Output Magnitude					R_L = 27 ohms or 50 ohms
Short–circuit Current					
V_{OH}			250	mA	–7V ≤ V_O ≤ +12V
V_{OL}			250	mA	–7V ≤ V_O ≤ +12V
High Impedance Output Current		±2	±200	µA	V_O = –7V to +12V
RECEIVER					
Diff. Input Threshold Voltage	–0.2		+0.2	Volts	–7V ≤ V_{CM} ≤ +12V
Input Current			+1.0	mA	V_{CC} = 0V or 5.25V; V_{IN} = +12V
			–0.8	mA	V_{CC} = 0V or 5.25V; V_{IN} = –7V
Input Hysteresis		70		mV	V_{CM} = 0V
Input Resistance	12			KΩ	–7V ≤ V_{CM} ≤ +12V
Output Voltage					
V_{OH}	3.5			Volts	I_O = –4mA; V_{ID} = +0.2V
V_{OL}			0.4	Volts	I_O = +4mA; V_{ID} = –0.2V
High Impedance Output Current			±1	µA	V_{CC} = 5.25v; 0.4V ≤ V_O ≤ 2.4V
POWER REQUIREMENTS					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		300	500	µA	No load, D = GND or V_{CC}
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
_C	0		+70	°C	
_E	–40		+85	°C	
Storage Temperature	–65		+150	°C	
Package					
_S	14–pin Plastic DIP				
_T	14–pin SOIC				

Quad Differential RS485/RS422 Transceivers

- RS485 and RS422
- +5V Only Power Supply Required
- Receiver Fail–Safe Mode
- Glitch–Free Power Up/Down
- Pin Compatible with DS36950/ DS36954

DESCRIPTION...

The **SP494/495** is a quad differential line driver/receiver meeting both RS485 and RS422 specifications. The **SP494/495** features three separate half–duplex transceivers for data bus connections, and a fourth transceiver, with individual driver/receiver enables. The **SP495** has a common enable line for three of the transceivers. The **SP494** and **SP495** are available in a 20–pin plastic LCC package for operation over the commerical and industrial temperature ranges.



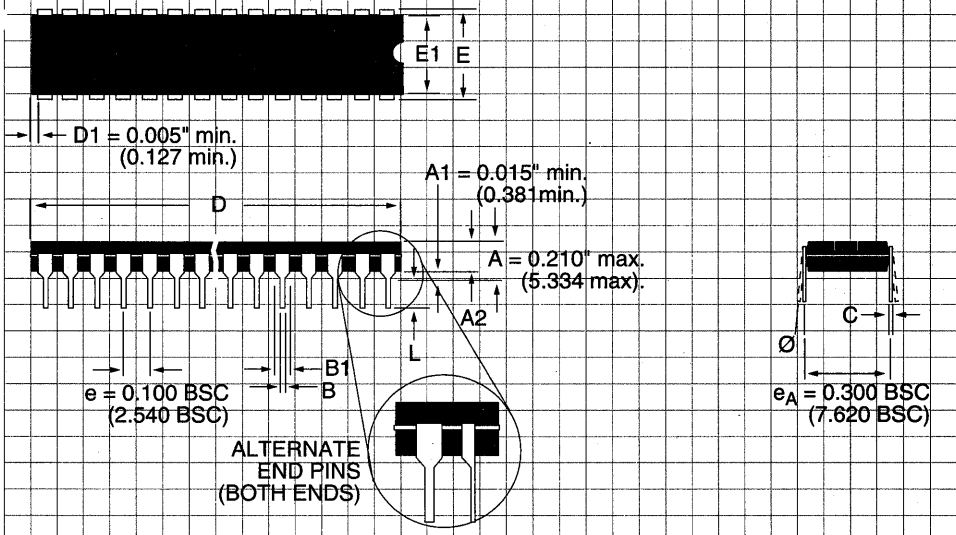
SPECIFICATIONS

V_{CC} = 5V±5%; typicals at 25°C; 0°C ≤ T_A ≤ +70°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DRIVERS					
Input Voltage					DR, DE
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Input Current					
I_{IL}			20	µA	V_{IN} = 2.4V
I_{IH}			–20	µA	V_{IN} = 0.4V
Input Clamp Voltage			–1.5	Volts	I = –18mA
Output Diff. Voltage	1.5	1.9		Volts	I_L = 60mA, V_{CM} = 0V; full load
	2.0	3.5		Volts	R_L = 100 ohms (RS422); termination load
	1.5	3.2		Volts	R_L = 54 ohms (RS485); termination load
Change in Output Magnitude			0.2	Volts	for complementary output state R_L = 27 ohms or 50 ohms
Common Mode Output Voltage		2.3	3	Volts	R_L = 54 ohms (RS485)
Change in Common Mode Output Magnitude			0.2	Volts	for complementary output state RL = 54 ohms or 100 ohms
Output Voltage					
V_{OH}	2.7	3.2		Volts	I_{OH} = –55mA
V_{OL}		1.4	1.7	Volts	I_{OH} = 55mA
Short Circuit Output Current		–130	–250	mA	V_O = –7V (RS485)
		–90	–150	mA	V_O = 0V (RS422)
		130	250	mA	V_O = +12V (RS485)
RECEIVER					
Diff. Input Threshold Voltage					RS422/485
V_{TH}		0.03	0.2	Volts	$V_O = V_{OH}$; I_O = –0.4mA
V_{TL}	–0.2	0.03		Volts	$V_O = V_{OL}$; I_O = 0.4mA
Input Hysteresis		60		mV	V_{CM} = 0V
Output Voltage					
V_{OH}	2.4	3.0		Volts	I_{OH} = –4mA; V_{ID} = +0.2V
V_{OL}		0.35	0.5	Volts	I_{OL} = +4mA; V_{ID} = –0.2V
High Impedance Output Current			20	µA	0.4V ≤ V_O ≤ 2.4V
Short–Circuit Output Current	–15	–30	–75	mA	V_O = 0V
POWER REQUIREMENTS					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		75	90	mA	No load, outpus enabled
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
–C	0		+70	°C	
–E	–40		+85	°C	
Storage Temperature	–65		+150	°C	
Package	20–pin Plastic LCC				

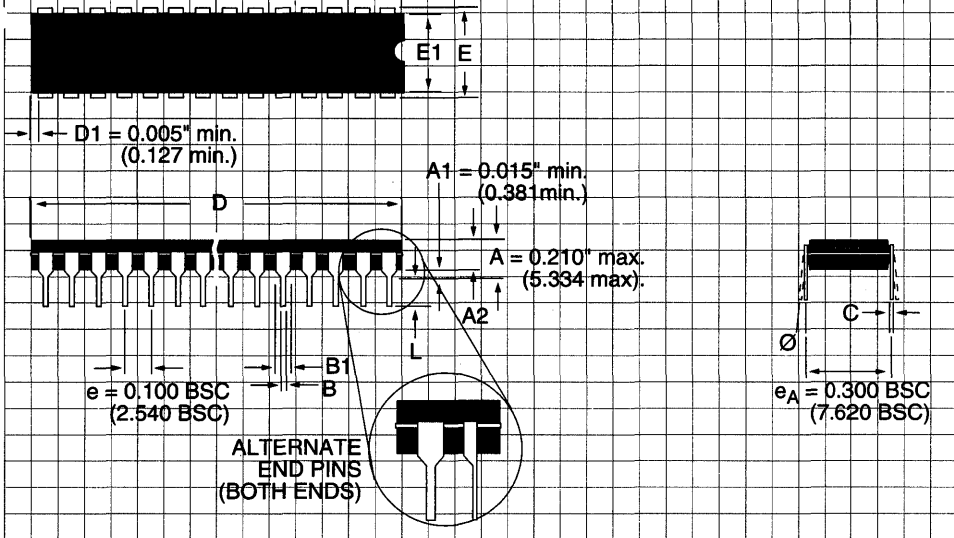
PACKAGE DRAWINGS

PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



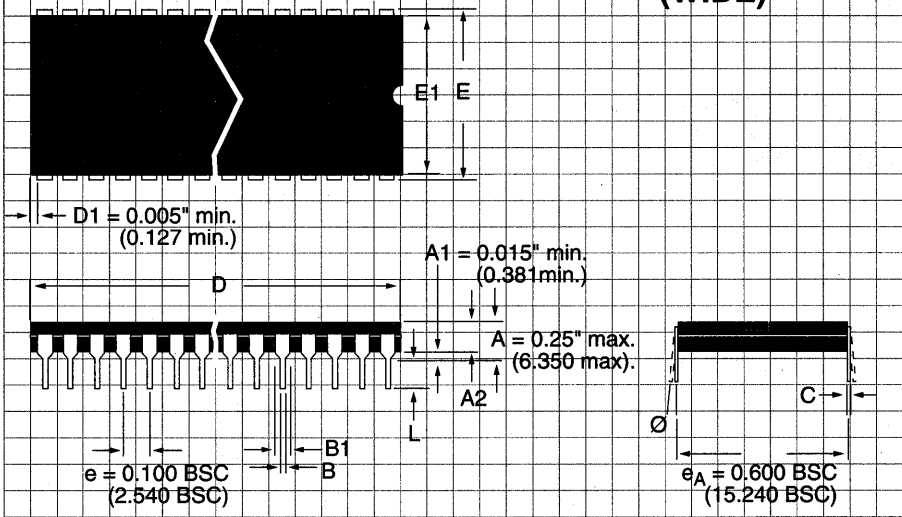
DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



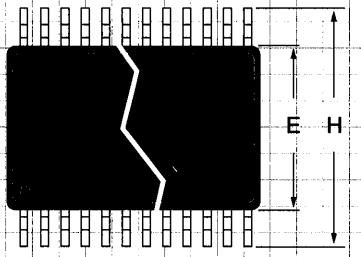
DIMENSIONS (Inches) Minimum/Maximum (mm)	24-PIN	28-PIN				
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)				
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)				
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)				
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)				
D	1.230/1.280 (31.24/32.51)	1.385/1.405 (35.179/35.687)				
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)				
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)				
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)				
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)				

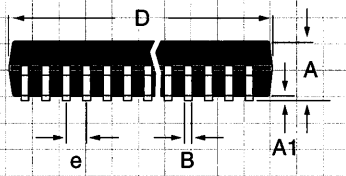
PACKAGE: PLASTIC DUAL–IN–LINE (WIDE)

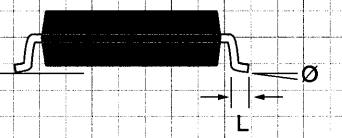


DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN	40–PIN	48–PIN		
A2	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)		
B	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559)	0.014/0.022 (0.366/0.559)		
B1	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)		
C	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)		
D	1.150/1.290 (29.21/32.76)	1.380/1.565 (35.05/39.75)	1.980/2.095 (50.29/53.21)	2.385/2.480 (60.57/62.99)		
E	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)		
E1	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)		
L	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)		
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)		

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)

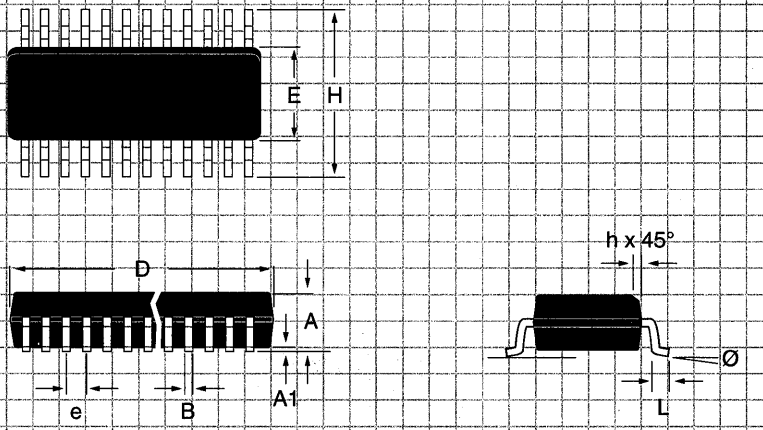






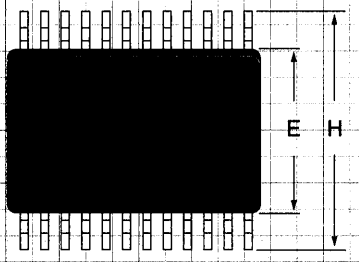
DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN				
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)				
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)				
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)				
D	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)				
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)				
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)				
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)				
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)				
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)				

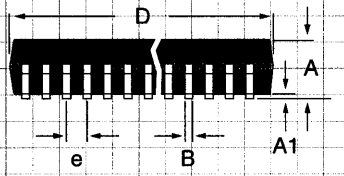
PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)

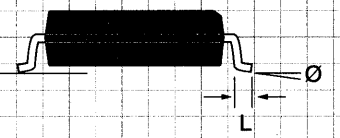


DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN			
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)			
A1	0.004/0.010 (0.102/0.249	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)			
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)			
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)			
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)			
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)			
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)			
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)			
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)			
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)			

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)

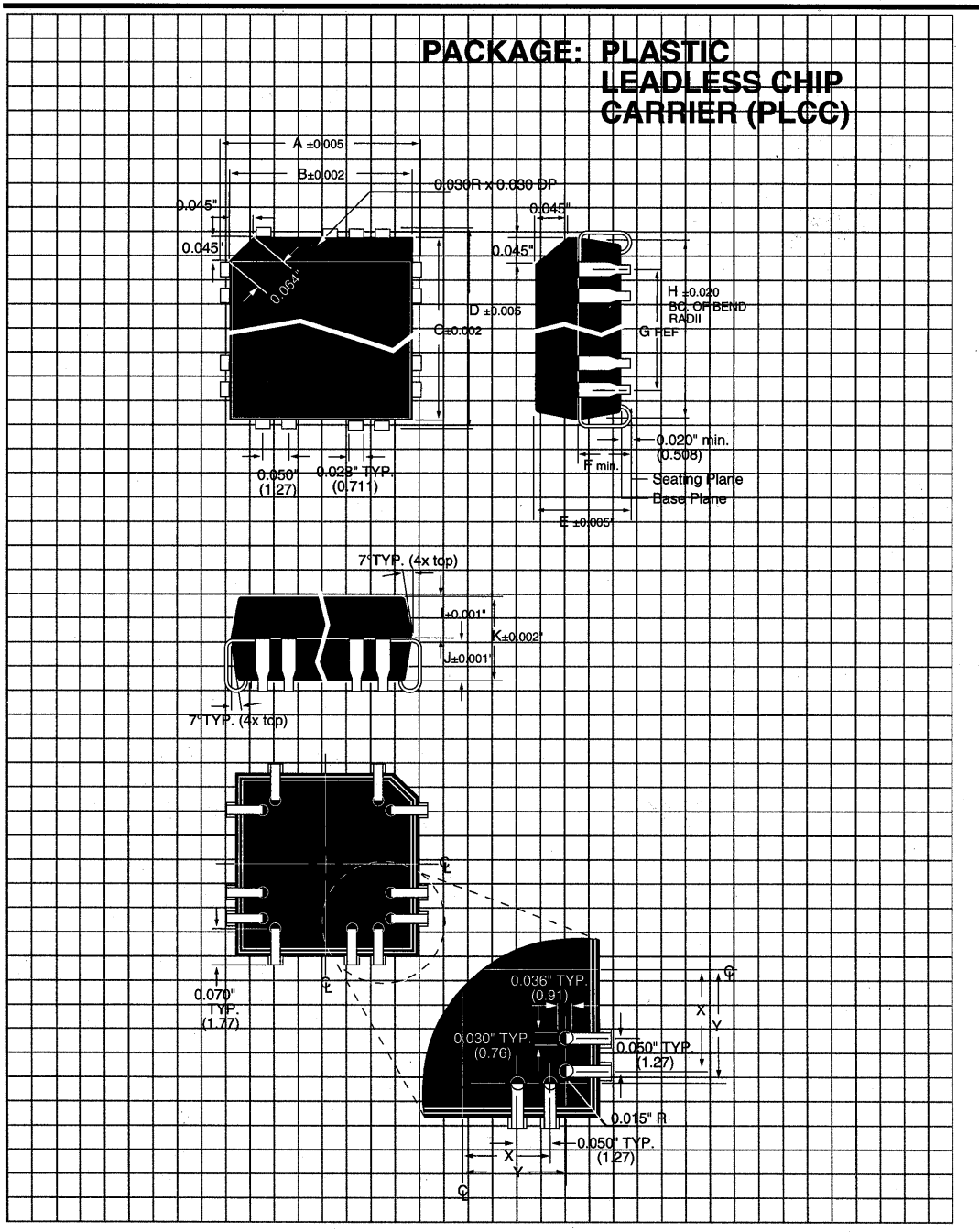






DIMENSIONS (Inches) Minimum/Maximum (mm)	14–PIN	16–PIN	18–PIN	20–PIN	24–PIN	28–PIN
A	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.348/0.363 (8.83/9.22)	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)	0.496/0.512 (12.60/13.00)	0.599/0.614 (15.20/15.59)	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC))	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

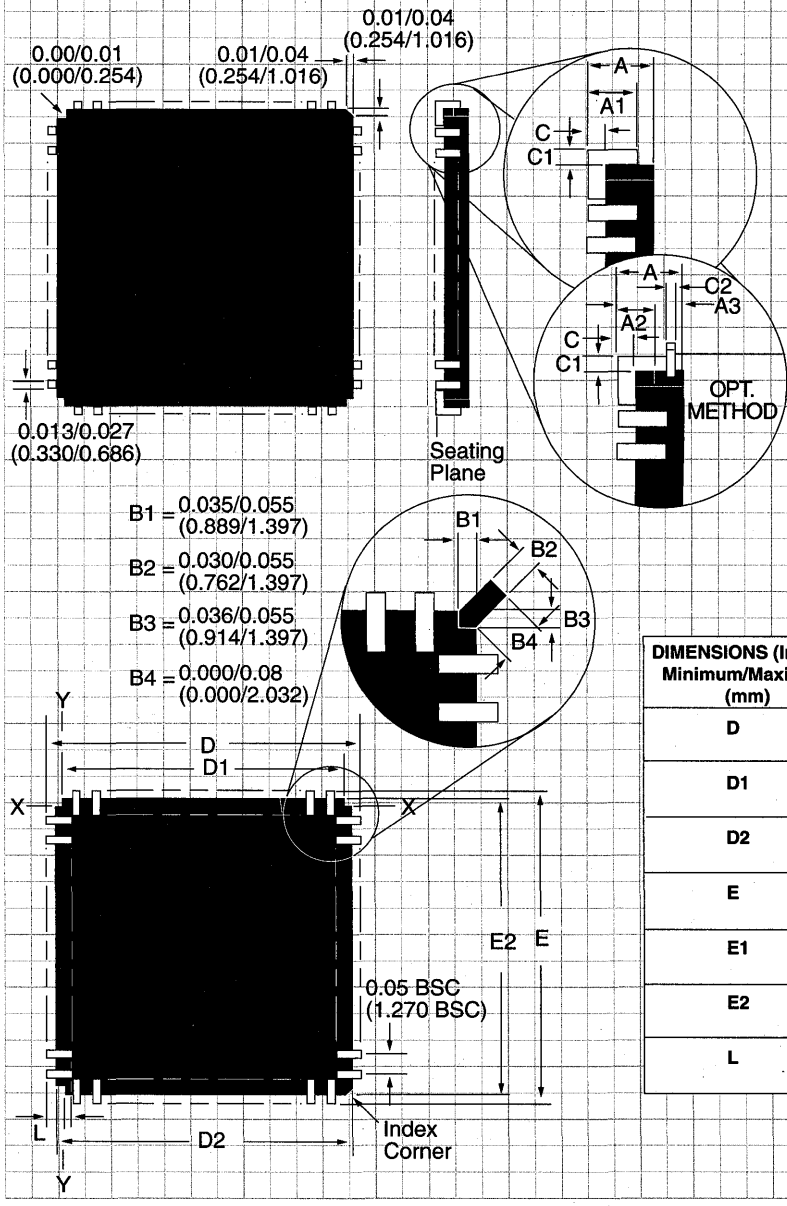
PACKAGE: PLASTIC LEADLESS CHIP CARRIER (PLCC)



PACKAGE: PLASTIC LEADLESS CHIP CARRIER (PLCC)

DIMENSIONS (Inches) Minimum/Maximum (mm)	20–PIN	28–PIN	44–PIN	68–PIN	84–PIN
A	0.385/0.395 (9.77/10.03)	0.485/0.495 (12.31/12.57)	0.685/0.695 (17.39/17.65)	0.985/0.995 (25.02/25.27)	1.185/1.195 (30.09/30.35)
B	0.350/0.355 (8.89/9.017)	0.452/0.456 (11.48/11.58)	0.652/0.656 (16.56/16.61)	0.952/0.956 (24.18/24.28)	1.152/1.156 (29.26/29.36)
C	0.350/0.355 (8.89/9.017)	0.452/0.456 (11.48/11.58	0.652/0.656 (16.56/16.61	0.952/0.956 (24.18/24.28)	1.152/1.156 (29.26/29.36)
D	0.385/0.395 (9.77/10.03)	0.485/0.495 (12.31/12.57)	0.685/0.695 (17.39/17.65	0.985/0.995 (25.02/25.27))	1.185/1.195 (30.09/30.35)
E	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)	0.170/0.180 (4.32/4.57)
F	0.098/– (2.48/–)	0.098/– (2.48/–)	0.098/– (2.48/–)	0.098/– (2.48/–)	0.098/– (2.48/–)
G	0.200 REF (5.08 REF)	0.300 REF (7.62 REF)	0.500 REF (12.7 REF)	0.800 REF (20.32 REF)	1.000 REF (25.44 REF)
H	0.290/0.330 (7.36/8.38)	0.390/0.430 (9.906/10.922)	0.590/0.630 (14.98/16.00)	0.890/0.930 (22.60/23.62)	1.090/1.130 (27.69/28.70)
I	0.065/0.070 (1.65/1.77)	0.070/0.072 (1.77/1.83	0.070/0.072 (1.77/1.83	0.070/0.072 (1.77/1.83)	0.070/0.072 (1.77/1.83
J	0.08/– (2.03/–)	0.070/0.072 (1.77/1.82)	0.070/0.072 (1.77/1.82)	0.070/0.072 (1.77/1.83)	0.070/0.072 (1.77/1.82)
K	0.145/0.156 (3.68/3.96)	0.148/0.152 (3.75/3.86)	0.148/0.152 (3.75/3.86)	0.148/0.152 (3.75/3.86)	0.148/0.152 (3.75/3.86)
X	0.100 REF (2.54 REF)	0.150 REF (3.810 REF)	0.250 REF (6.35 REF)	0.400 REF (10.16 REF)	0.500 REF (12.7 REF)
Y	0.140/0.147 (3.50/3.733)	0.180 REF (4.572 REF)	0.280 REF (7.11 REF)	0.430 REF (10.92 REF)	0.530 REF (13.46 REF)

PACKAGE: PLASTIC LEADLESS CHIP CARRIER 52-PIN



A = 0.155/0.175 (3.937/4.445)

A1 = 0.090/0.130 (2.286/3.302)

A2 = 0.060/0.080 (1.524/2.032)

A3 = 0.090/0.110 (2.286/2.794)

C = 0.030/0.045 (0.762/1.143)

C1 = 0.010/0.030 (0.254/0.762)

C2 = 0.000/0.020 (0.000/0.508)

B1 = 0.035/0.055 (0.889/1.397)

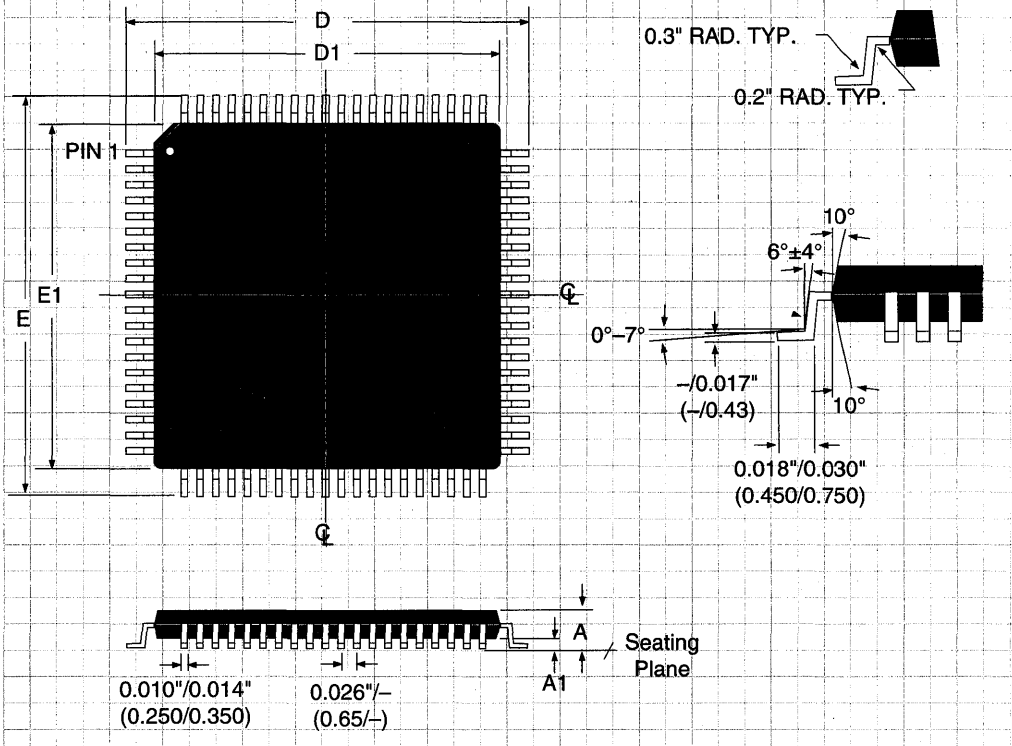
B2 = 0.030/0.055 (0.762/1.397)

B3 = 0.036/0.055 (0.914/1.397)

B4 = 0.000/0.08 (0.000/2.032)

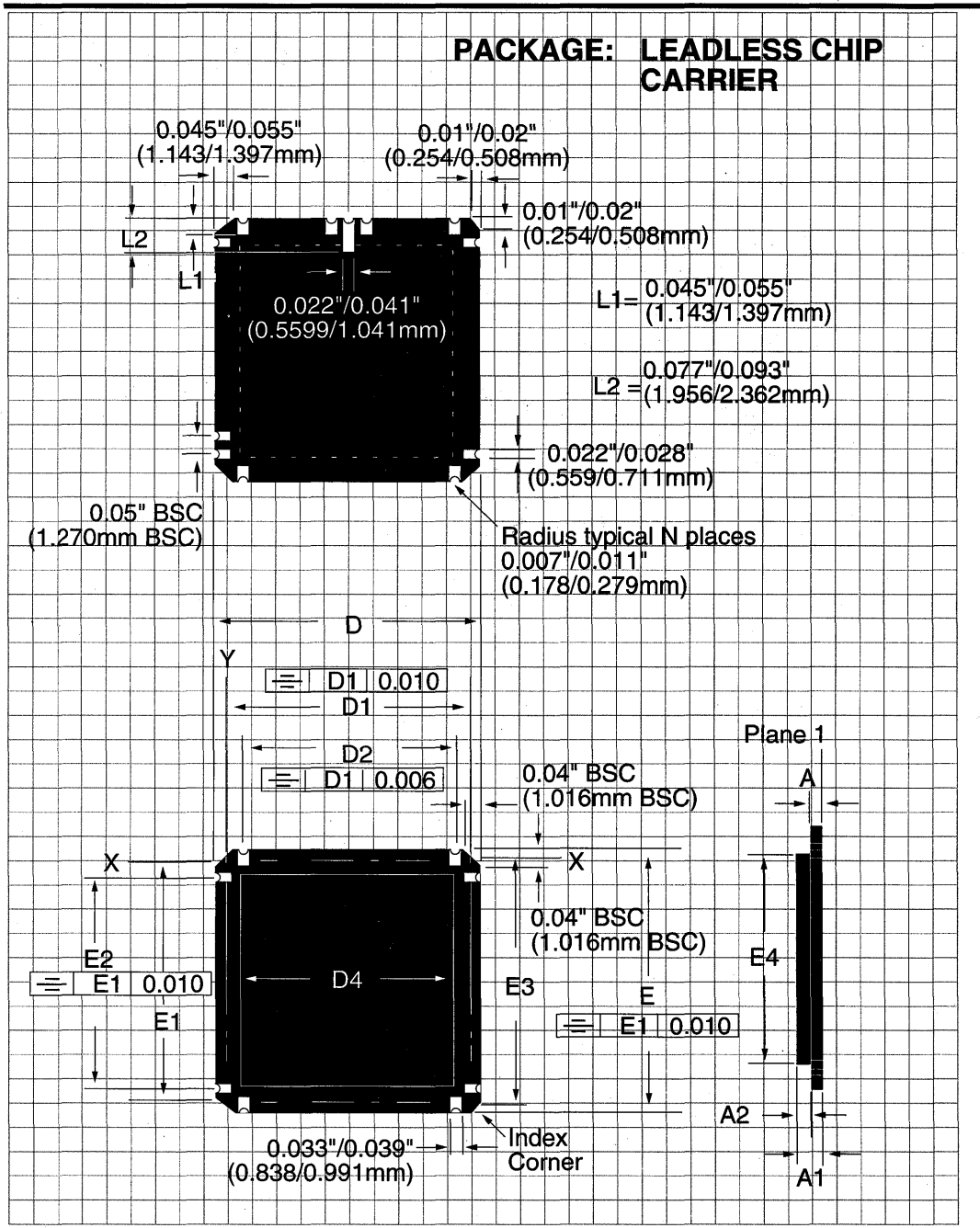
DIMENSIONS (Inches) Minimum/Maximum (mm)	52–PIN
D	0.0770/0.810 (19.558/20.574)
D1	0.645/0.655 (16.383/16.637)
D2	0.740/0.780 (18.796/19.812)
E	0.0770/0.810 (19.558/20.574))
E1	0.645/0.655 (16.383/16.637)
E2	0.740/0.780 (18.796/19.812)
L	0.045/0.060 (1.143/1.524)

PACKAGE: QUAD FLATPACK 80–PIN



DIMENSIONS (Inches) Minimum/Maximum (mm)	80–PIN
A	–/0.096 (–/2.450)
A1	–/0.010 (–/0.250)
D	0.620/0.640 (15.750/16.250)
D1	0.547/0.555 (13.900/14.100)
E	0.620/0.640 (15.750/16.250)
E1	0.547/0.555 (13.900/14.100)

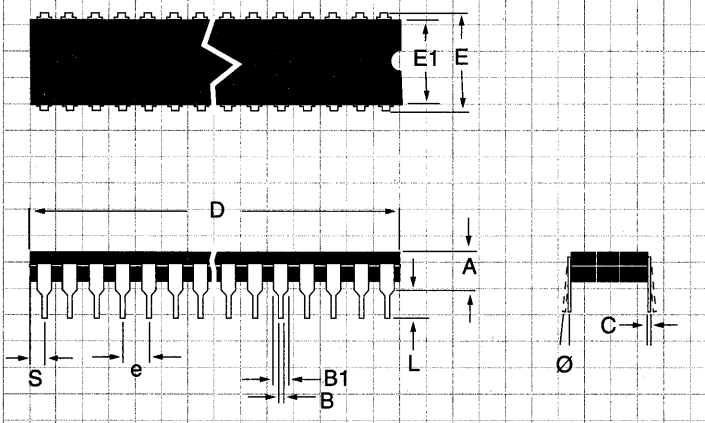
PACKAGE: LEADLESS CHIP CARRIER



PACKAGE: LEADLESS CHIP CARRIER

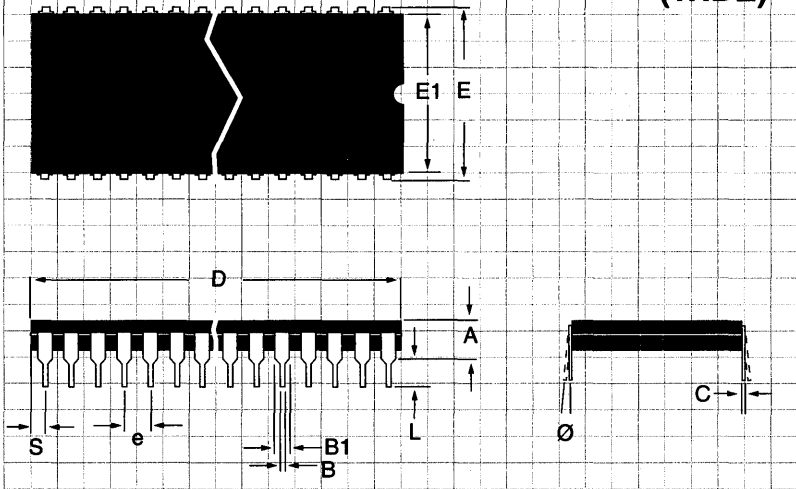
DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN	44–PIN		
A	0.017/0.088 (0.432/2.235)	0.037/0.088 (0.940/2.235)		
A1	0.064/0.100 (1.626/2.540)	0.069/0.120 (1.753/3.048)		
A2	0.007/0.075 (0.178/1.905)	0.007/0.080 (0.178/2.032)		
D	0.442/0.458 (11.227/11.633)	0.640/0.660 (16.256/16.764)		
D1	0.404/0.415 (10.262/10.541)	0.600/0.620 (15.240/15.748)		
D2	0.300/– (7.620/–)	0.500/– (12.700/–)		
D3	0.420 REF (10.668 REF)	0.620 REF (15.748 REF)		
D4	0.406/0.458 (10.312/11.633)	0.495/0.560 (12.573/14.224)		
E	0.442/0.458 (11.227/11.633)	0.640/0.660 (16.256/16.764)		
E1	0.404/0.415 (10.262/10.541)	0.600/0.62 (15.240/15.748)		
E2	0.300/– (7.620/–)	0.500/– (12.700/–)		
E3	0.42 REF (10.668 REF)	0.62 REF (15.748 REF)		
E4	0.406/0.458 (10.312/11.633)	0.495/0.560 (12.573/14.224)		

PACKAGE: CERAMIC DUAL–IN–LINE (NARROW)



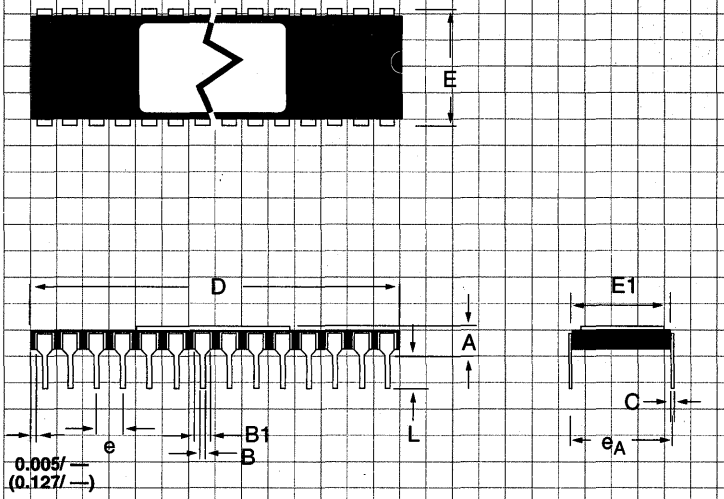
DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16 –PIN	18–PIN	20–PIN
A	0.105/0.175 (2.667/4.445)	0.105/0.175 (2.667/4.445)	0.105/0.175 (2.667/4.445)	0.105/0.175 (2.667/4.445)	–/0.200 (–/5.08)
B	0.015/0.021 (0.381/0.533)	0.015/0.021 (0.381/0.533)	0.015/0.021 (0.381/0.533)	0.015/0.021 (0.381/0.533)	0.014/0.023 (0.36/0.58)
B1	0.038/0.060 (0.965/1.524)	0.038/0.060 (0.965/1.524)	0.038/0.060 (0.965/1.524)	0.038/0.060 (0.965/1.524)	0.038/0.065 (0.97/1.65)
C	0.008/0.012 (0.203/0.305)	0.008/0.012 (0.203/0.305)	0.008/0.012 (0.203/0.305)	0.008/0.012 (0.203/0.305)	0.008/0.015 (0.20/0.38)
D	0.380/0.550 (9.652/13.970)	0.690/0.770 (17.526/19.558)	0.770/0.830 (19.558/21.082)	0.880/0.930 (22.352/23.622)	—/1.060 (—/26.92)
E	0.290/0.325 (7.366/8.255)	0.290/0.325 (7.366/8.255)	0.290/0.325 (7.366/8.255)	0.290/0.325 (7.366/8.255)	0.220/0.310 (5.59/7.87)
E1	0.280/0.310 (7.112/7.874)	0.280/0.310 (7.112/7.874)	0.280/0.310 (7.112/7.874)	0.280/0.310 (7.112/7.874)	0.290/0.320 (7.37/8.13)
e	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)
L	0.125/0.175 (3.175/4.445)	0.125/0.175 (3.175/4.445)	0.125/0.175 (3.175/4.445)	0.125/0.175 (3.175/4.445)	0.125/0.200 (3.18/5.08)
S	0.030/0.120 (0.762/3.048)	0.030/0.095 (0.762/2.413)	0.020/0.065 (0.508/1.651)	0.030/0.065 (0.762/1.651)	–/0.080 (–/2.03)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: CERAMIC DUAL–IN–LINE (WIDE)



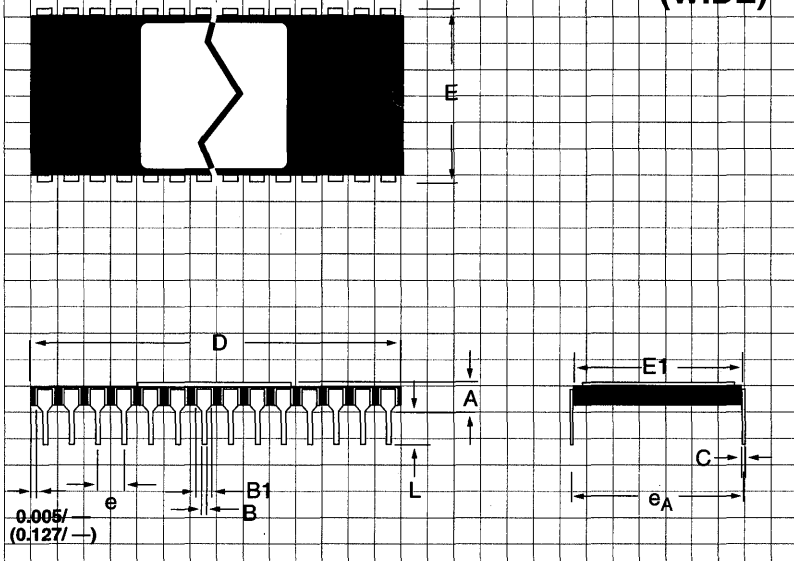
DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN	40–PIN	44–PIN	
A	0.085/0.190 (2.159/4.826)	0.085/0.190 (2.159/4.826)	0.085/0.190 (2.159/4.826)	0.085/0.190 (2.159/4.826)	
B	0.015/0.023 (0.381/0.584)	0.015/0.023 (0.381/0.584)	0.015/0.023 (0.381/0.584)	0.015/0.023 (0.381/0.584))	
B1	0.038/0.060 (0.965/1.524)	0.038/0.060 (0.965/1.524)	0.038/0.060 (0.965/1.524)	0.038/0.060 (0.965/1.524)	
C	0.008/0.012 (0.203/0.305)	0.008/0.012 (0.203/0.305)	0.008/0.012 (0.203/0.305)	0.008/0.012 (0.203/0.305)	
D	1.180/1.220 (29.972/30.988)	1.380/1.430 (35.052/36.322)	1.980/2.030 (50.29/51.56)	2.180/2.230 (55.37/56.64)	
E	0.575/0.610 (14.605/15.494)	0.595/0.625 (15.113/15.875)	0.595/0.625 (15.113/15.875)	0.595/0.625 (15.113/15.875)	
E1	0.575/0.610 (14.605/15.494)	0.575/0.610 (14.605/15.494)	0.575/0.610 (14.605/15.494)	0.575/0.610 (14.605/15.494)	
e	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	
L	0.125/0.175 (3.175/4.445)	0.125/0.175 (3.175/4.445)	0.125/0.175 (3.175/4.445)	0.125/0.175 (3.175/4.445)	
S	0.030/0.065 (0.762/1.652)	0.030/0.065 (0.762/1.652)	0.030/0.065 (0.762/1.652)	0.030/0.065 (0.762/1.652)	
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	

PACKAGE: SIDE-BRAZED DUAL-IN-LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN	18-PIN	20-PIN	22-PIN	24-PIN	28-PIN
A	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)
B	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)
B1	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)
C	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)
D	0.780/0.820 (19.81/20.82)	0.880/0.920 (22.35/23.36)	0.980/1.020 (24.89/25.09)	1.080/1.120 (27.43/28.44)	1.180/1.220 (29.97/30.98)	1.380/1.420 (35.05/36.06)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255))	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255))	0.300/0.325 (7.620/8.255)
E1	0.280/0.310 (7.112/7.874)	0.280/0.310 (7.112/7.874)	0.280/0.310 (7.112/7.874)	0.280/0.310 (7.112/7.874))	0.280/0.310 (7.112/7.874)	0.280/0.310 (7.112/7.874)
e	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)
e_A	0.300 BSC (7.620 BSC)	0.300 BSC (7.620 BSC)	0.300 BSC (7.620 BSC)	0.300 BSC (7.620 BSC)	0.300 BSC (7.620 BSC)	0.300 BSC (7.620 BSC)
L	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)

PACKAGE: SIDE–BRAZED DUAL–IN–LINE (WIDE)



DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN	32–PIN	40–PIN
A	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)	0.085/0.200 (2.159/5.080)
B	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)	0.015/0.022 (0.381/0.559)
B1	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)	0.045/0.065 (1.143/1.651)
C	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)	0.009/0.015 (0.229/0.381)
D	1.180/1.220 (29.97/30.98)	1.380/1.420 (35.05/36.06)	1.580/1.620 (40.13/41.14)	1.980/2.020 (50.29/51.30)
E	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)
E1	0.580/0.610 (14.732/15.494)	0.580/0.610 (14.732/15.494)	0.580/0.610 (14.732/15.494)	0.580/0.610 (14.732/15.494)
e	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)	0.100 BSC (2.540 BSC)
e_A	0.600 BSC (15.240 BSC)	0.600 BSC (15.240 BSC)	0.600 BSC (15.240 BSC)	0.600 BSC (15.240 BSC)
L	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)	0.125/0.200 (3.175/5.080)

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