

## Over Sampling Digital Filter LSI

**Description**

CXD1144BP is a over sampling digital filter LSI developed for CD player and digital PB system.

**Features**

- Filtering with quadrupled/octupled over sampling.
- Filter characteristics  
Ripple : within  $\pm 0.00001\text{dB}$   
Attenuation : under  $-120\text{dB}$
- Deemphasis function (when quadrupled)

**Application**

- Compact disc player, Digital amplifier.

**Structure**

CMOS - IC

**Function**

- Built-in filters for 2 channels.
- Filtering with quadrupled/octupled over sampling.  
3 stage FIR filters interconnected in cascade (293rd).
- Filter characteristics  
Ripple : within  $\pm 0.00001\text{dB}$  (0 to 20kHz)  
Attenuation : under  $-120\text{dB}$  (24.1k to 150kHz)
- Serial I/O data  
Format : 2's complement MSB first (serial)  
Word length : 16/18bit
- Soft-muting function
- Deemphasis function (when quadrupled)

**Absolute Maximum Ratings (Ta = 25°C)**

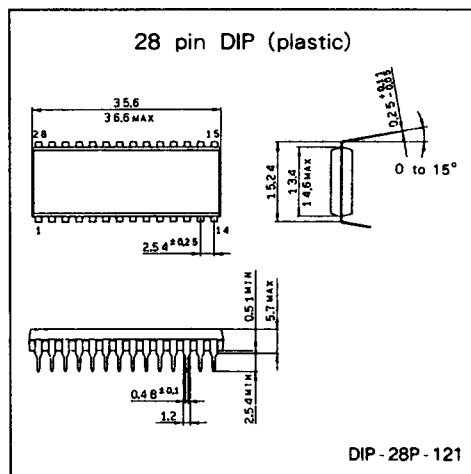
• Supply voltage	V <sub>DD</sub>	- 0.5 to + 6.5	V
• Input voltage	V <sub>I</sub>	- 0.5 to V <sub>DD</sub> + 0.5	V
• Storage temperature	T <sub>stg</sub>	- 55 to + 150	°C
• Allowable power dissipation	P <sub>D</sub>	500	mW (Ta = 60°C)

**Recommended Operating Conditions**

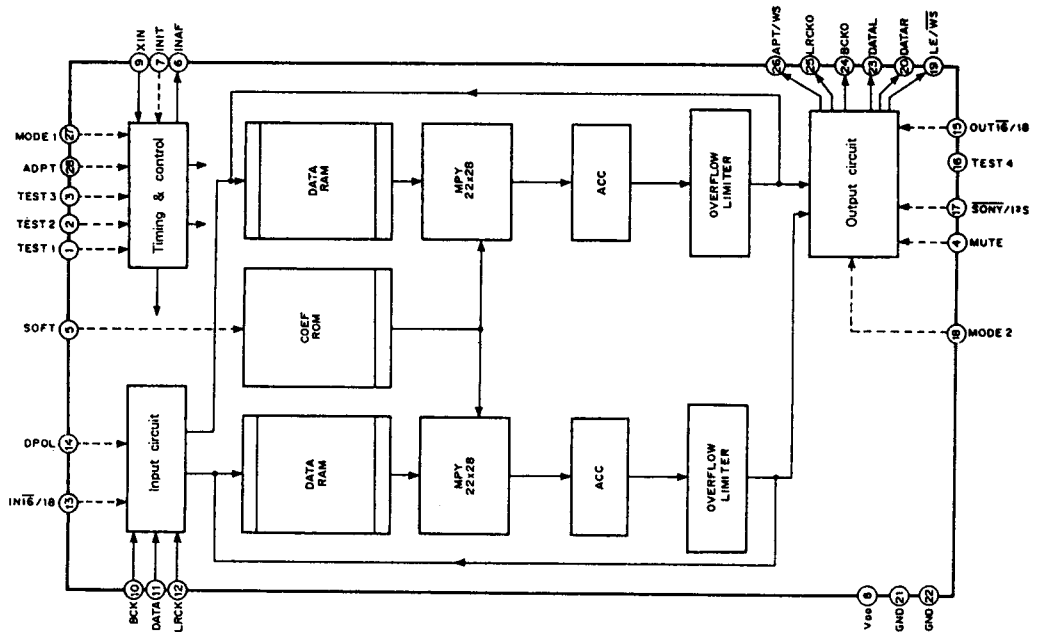
• Supply voltage	V <sub>DD</sub>	4.75 to 5.25	V
• Operating temperature	T <sub>opr</sub>	- 10 to 60	°C
• OSC frequency	f <sub>x</sub>	12.0 to 18.5	MHz

**Package Outline**

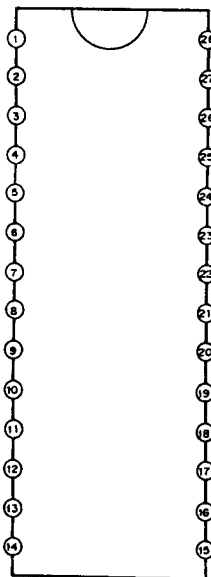
Unit : mm



Block Diagram



Pin Configuration (Top View)



## Pin Description

No.	Symbol	I/O	Description
1	TEST1	I	Test pin ; fixed at "L" level in usual operation.
2	TEST2	I	Test pin ; fixed at "L" level in usual operation.
3	TEST3	I	Test pin ; fixed at "L" level in usual operation.
4	MUTE	I	Nullifies output to "0" value ; valid at "H".
5	SOFT	I	ON/OFF for soft muting ; muting at "H".
6	INAF	O	Outputs "H" when input/output synchronization is off.
7	INIT	I	Resynchronization at rising edge of signal.
8	V <sub>DD</sub>	—	+ Power supply (+ 5V).
9	XIN	I	Master CLK input (f = 384 fs).
10	BCK	I	BCK input.
11	DATA	I	Serial data input (complement of 2).
12	LRCK	I	LRCK input.
13	IN16/18	I	Specification of input data word length ; "H" ; 18 bits, "L" ; 16 bits.
14	DPOL	I	Inverts the polarity of input data.
15	OUT16/18	I	Specification of output data word length, "H" : 18 bits, "L" ; 16 bits.
16	TEST4	I	Test pin ; fixed at "H" level in usual operation.
17	SONY/I <sup>2</sup> S	I	Specification of output format ; "H" : I <sup>2</sup> S, "L" : SONY.
18	MODE2	I	Specification of ADPT ; "H" : 8Fs, "L" : EMP. *
19	LE/WS	O	LE output (in SONY mode) /WS output (in I <sup>2</sup> S mode).
20	DATAR	O	RCH serial data output (complement of 2)
21	GND	—	
22	GND	—	
23	DATAL	O	LCH serial data output (complement of 2)
24	BCKO	O	BCK output
25	LRCKO	O	LRCK output
26	APT/WS	O	APT output (in SONY mode) /WS output (in I <sup>2</sup> S mode).
27	MODE1	I	Specification of ADPT ; "H" : 8Fs, "L" : EMP. *
28	ADPT	I	ON/OFF for ADPT ; ON at "H".

\* Note) MODE1 and MODE2 should have the same polarity.

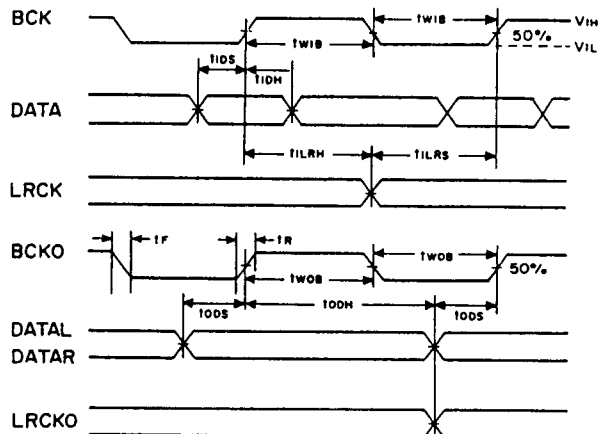
## Electrical Characteristics

## DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V <sub>IH</sub>		0.76V <sub>DD</sub>			V
"L" input voltage	V <sub>IL</sub>				0.24V <sub>DD</sub>	V
Input leak voltage	I <sub>LI</sub>				± 5	μ A
"H" output voltage	V <sub>OH</sub>	I <sub>o</sub> = - 2mA (BCK)	V <sub>DD</sub> - 0.5			V
		I <sub>o</sub> = - 1mA (Others)	V <sub>DD</sub> - 0.5			V
"L" output voltage	V <sub>OL</sub>	I <sub>o</sub> = 2mA (BCK)			0.4	V
		I <sub>o</sub> = 1mA (Others)			0.4	V

AC characteristics

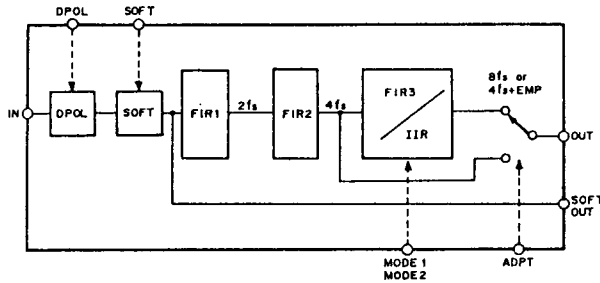
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
OSC frequency	$f_x$		12.0	16.9	18.5	MHz
Input BCK frequency	$f_{bck}$				2.31	MHz
Input BCK pulse width	$t_{wIB}$	DUTY : $50 \pm 10\%$	100			ns
Input data set up time	$t_{iDS}$		20			ns
Input data hold time	$t_{iDH}$		20			ns
Input LRCK set up time	$t_{iLRS}$		50			ns
Input LRCK hold time	$t_{iLRH}$		50			ns
Output BCK pulse width	$t_{wOB}$	$f_x = 16.9\text{MHz}$ SONY output mode	40			ns
Output data set up time	$t_{oDS}$	8Fs, BCK24 CL = 25pF BCKOCL = 50pF	25			ns
Output data hold time	$t_{oDH}$		25			ns
Output BCK pulse width	$t_{wOB}$	$f_x = 16.9\text{MHz}$ I <sup>2</sup> S output mode	60			ns
Output data set up time	$t_{oDS}$	8Fs, CL = 25pF BCKOCL = 50pF	35			ns
Output data hold time	$t_{oDH}$		35			ns
Output BCK pulse width	$t_{wOB}$	$f_x = 18.5\text{MHz}$ SONY output mode	40			ns
Output data set up time	$t_{oDS}$	8Fs, BCK24 CL = 25pF BCKOCL = 50pF	20			ns
Output data hold time	$t_{oDH}$		20			ns
Output BCK pulse width	$t_{wOB}$	$f_x = 18.5\text{MHz}$ I <sup>2</sup> S output mode	60			ns
Output data set up time	$t_{oDS}$	8Fs, CL = 25pF BCKOCL = 50pF	32			ns
Output data hold time	$t_{oDH}$		32			ns
Output signal rise/fall time	$t_R, t_F$	CL = 25pF BCKOCL = 50pF			30	ns



**Function**

**1. Conceptual block diagram**

A conceptual block diagram of this LSI is shown in the following figure :



SOFT OUT (1fs) is output from DATA R only in 1<sup>st</sup> 4fs mode.

**2. Selection of over-sampling mode**

The following three modes are selectable via ADPT, MODE1 and MODE2 pins :

- 4fs mode
- 4fs + emphasis mode
- 8fs mode.

ADPT	MODE1 MODE2	"H"	"L"
	"H"		8fs
"L"		4fs	4fs

The time constant for emphasis takes values of  $\tau 1 = 50 \mu s$  and  $\tau 2 = 15 \mu s$  at  $f_s = 44.1 \text{ kHz}$ .

**3. Soft muting**

This function smoothly conducts muting and releases muting of data by turning ON/OFF the SOFT pin. ON/OFF switchover is not applicable within 30 ms.

**4. Input/output synchronization circuit**

**1) Principle**

In the synchronizing circuit, a window for 10 clocks of the internal system clock ( $XIN/2$ ) is provided to monitor as to whether or not the rising edge of LRCK ( $f$ ) to be entered is within this window. When LRCK  $f$  is outside the window upon turning on power, the synchronizing circuit causes the internal processing to discontinue at timing of the window center, and causes it to start upon appearance of the next LRCK  $f$ . This action ensures synchronization between an external system and this LSI.

## 2) Resynchronization by INIT.

Even when the LRCK  $f$  is outside the window, synchronization may be off due to the mixture of external noise if the LRCK  $f$  is located near an end of the window. To avoid this, it is necessary to apply resynchronization without fall after turning on power. Resynchronizing action is done at timing of rising of INIT and initializes the synchronizing circuit to locate the LRCK  $f$  at the window center. When synchronization is off, INAF output becomes on "H" level.

## 5. Muting

Muting is applied to data entered into the LSI when :

INIT : "L" and "0" data are entered.

Output data become "0" data when :

INIT : "L" or MUTE : "H".

## 6. Data polarity

The DPOL pin permits switchover between invert and non-invert of output data.

DPOL : "L" ... non-invert

DPOL : "H" ... invert.

## 7. Latch timing of input/output signals

1) Inputs INT $\bar{6}$ /18, DPOL, SOFT, MUTE, OUT $\bar{6}$ /18, SONY/I $\bar{S}$ , ADPT, MODE1 and MODE2 :

These input signals are latched by an internal clock corresponding to LRCK.

2) Outputs LRCK0, BCK0, DATAL, DATAR, APT/WS and LE/WS :

These output signals are latched by an internal clock corresponding to BCK0.

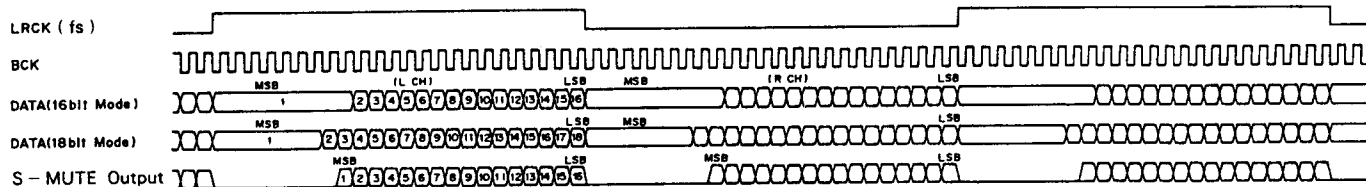
## 8. Selection of output format

An output format for this LSI is selected as shown in the following table :

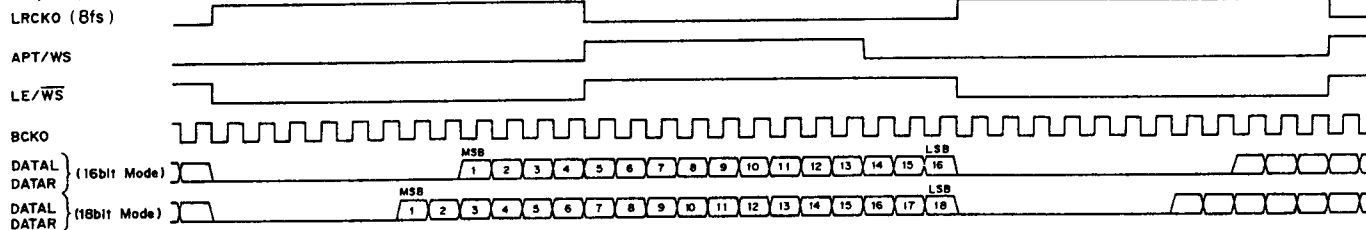
	4fs			8fs		
	SONY mode, 16-bit output	SONY mode, 18-bit output	I $\bar{S}$ mode	SONY mode, 16-bit output	SONY mode, 18-bit output	I $\bar{S}$ mode
< Control pin >						
ADPT	ON/OFF	←	←	ON	←	←
MODE1	4fs	←	←	8fs	←	←
MODE2	4fs + EMP	←	←	8fs	←	←
SONY/I $\bar{S}$	SONY	←	I $\bar{S}$	SONY	←	I $\bar{S}$
OUT $\bar{6}$ /18	16	18	Invalid	16	18	Invalid
< Output pin >						
LRCK0	4LRCK	←	←	8LRCK	←	4LRCK
BCK0	24	24	16	24	24	16
DATAL/DATA	DATAL	←	MIX DATA	DATAL	←	Composite DATA
DATAR/S-MUTE	DATAR	←	S-MUTE	DATAR	←	Composite DATA
APT/WS	APT	←	WS	APT	←	WS
LE/WS	LE	←	WS	LE	←	WS

# I/O Timing Chart

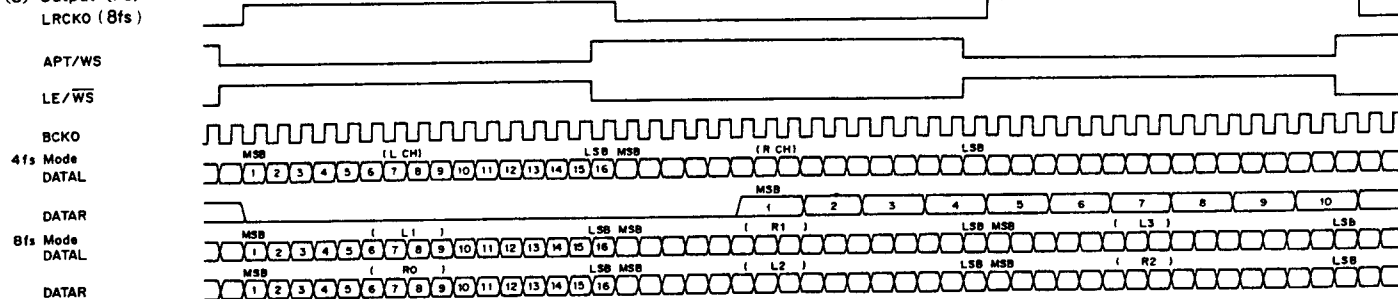
## (1) Input



## (2) Output (SONY)



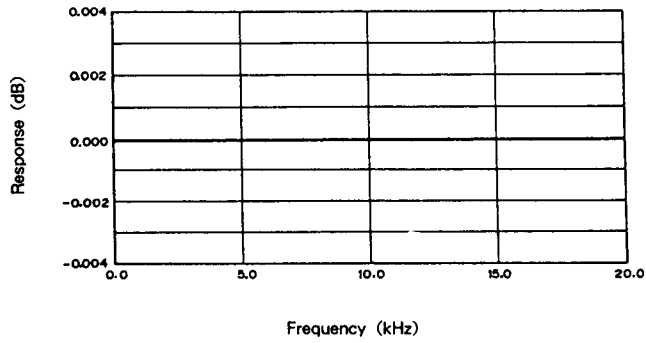
## (3) Output (PS)



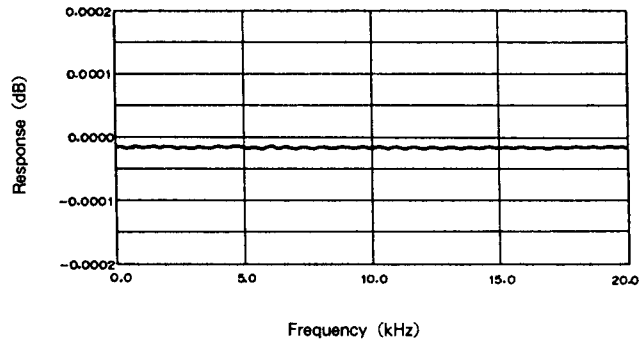
**Filter Characteristics**

1) 4fs Mode (ADPT = L, MODE1 = MODE2 = H)

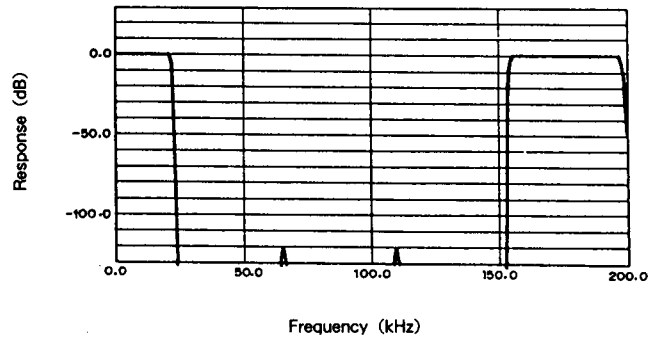
**Frequency characteristics**



**Ripple characteristics**



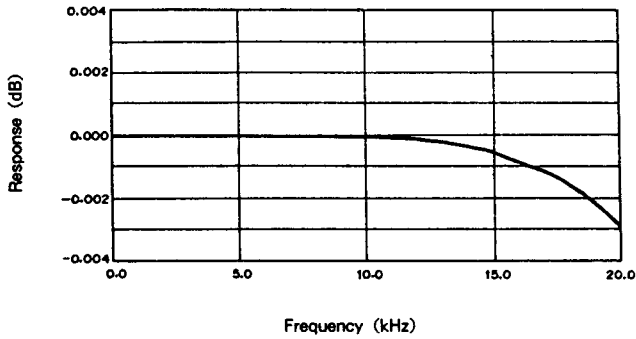
**Attenuation characteristics**



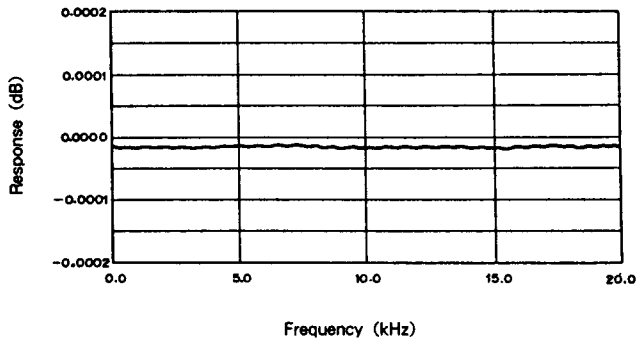


2) 8fs Mode (ADPT = MODE1 = MODE2 = H)

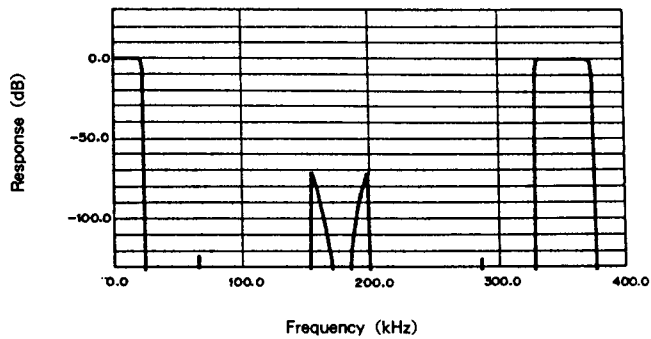
**Frequency characteristics**



**Ripple characteristics**



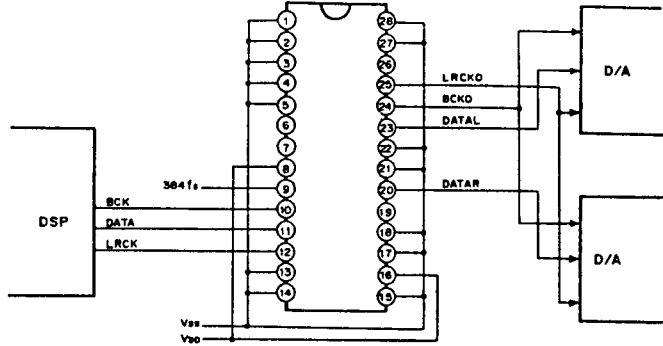
**Attenuation characteristics**



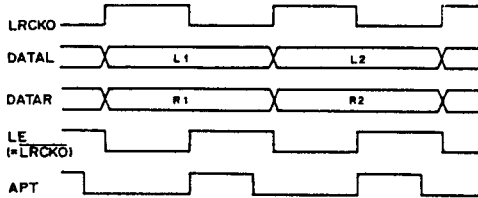
Application Circuit

1) 4fs

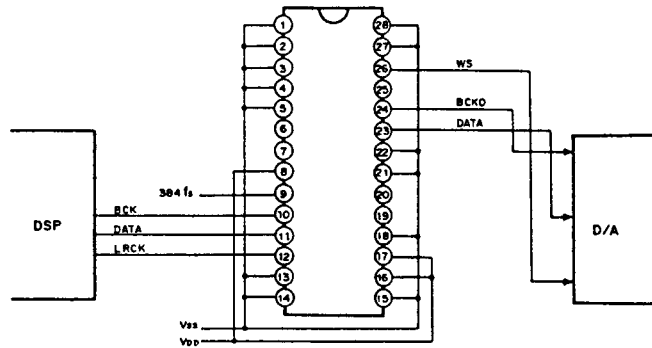
SONY Mode



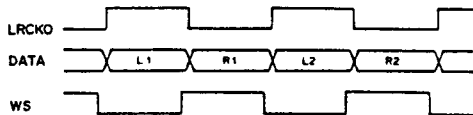
(Top View)  
CXD1144BP



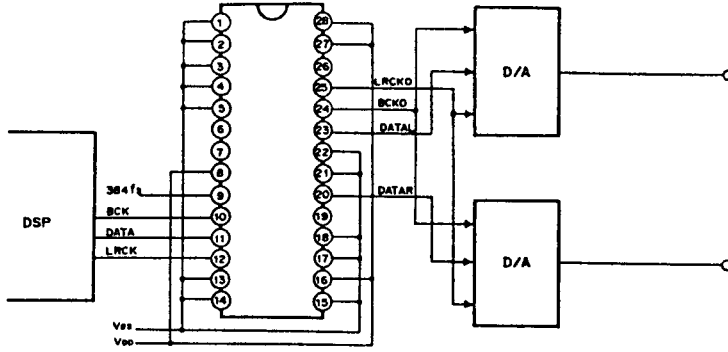
I<sup>2</sup>S Mode



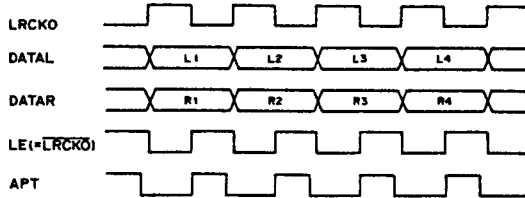
(Top View)  
CXD1144BP



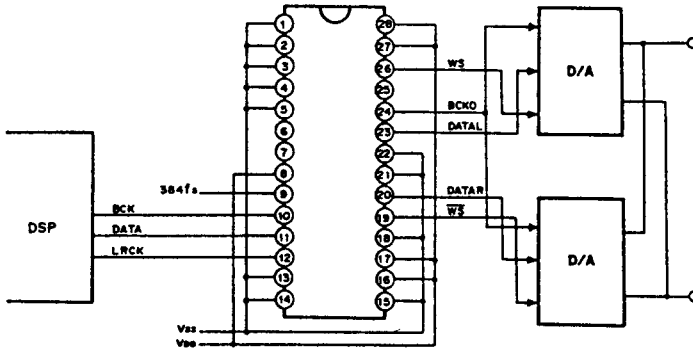
2) 8fs  
SONY Mode



(Top View)  
CXD1144BP



I<sup>2</sup>S Mode



(Top View)  
CXD1144BP

