MEMORY
DATA BOOK

THOMSON
COMPONENTS
MOSTEK

MEMORY

THOMSON
MOSTEK
1987

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CHAPTER 1 - STATIC RAMs

ZEROPOWER™ AND TIMEKEEPER™ RAMs

Description	Part number	Organization	Access Time	I_{CC}	I_{SB}	Page
TIMEKEEPER SRAM	MK48T02-12	2K x 8	120 ns	80 mA	3 mA	1-5
	MK48T02-15	2K x 8	150 ns	80 mA	3 mA	
	MK48T02-20	2K x 8	200 ns	80 mA	3 mA	
	MK48T02-25	2K x 8	250 ns	80 mA	3 mA	
TIMEKEEPER SRAM	MK48T12-12	2K x 8	120 ns	80 mA	3 mA	1-5
V_{CC}=±10%	MK48T12-15	2K x 8	150 ns	80 mA	3 mA	
	MK48T12-20	2K x 8	200 ns	80 mA	3 mA	
	MK48T12-25	2K x 8	250 ns	80 mA	3 mA	
ZEROPOWER SRAM	MK48Z02-15	2K x 8	150 ns	80 mA	1 mA	1-23
	MK48Z02-20	2K x 8	200 ns	80 mA	1 mA	
	MK48Z02-25	2K x 8	250 ns	80 mA	1 mA	
ZEROPOWER SRAM	MK48Z12-12	2K x 8	120 ns	80 mA	1 mA	1-23
V_{CC}=±10%	MK48Z12-15	2K x 8	150 ns	80 mA	1 mA	
	MK48Z12-20	2K x 8	200 ns	80 mA	1 mA	
	MK48Z12-25	2K x 8	250 ns	80 mA	1 mA	
ZEROPOWER SRAM	MK48Z08-15	8K x 8	150 ns	80 mA	1 mA	1-35
	MK48Z08-20	8K x 8	200 ns	80 mA	1 mA	
	MK48Z08-25	8K x 8	250 ns	80 mA	1 mA	
ZEROPOWER SRAM	MK48Z18-15	8K x 8	150 ns	80 mA	1 mA	1-35
V_{CC}=±10%	MK48Z18-20	8K x 8	200 ns	80 mA	1 mA	
	MK48Z18-25	8K x 8	250 ns	80 mA	1 mA	
ZEROPOWER SRAM	MK48Z09-15	8K x 8	150 ns	80 mA	1 mA	1-35
WITH POWER FAIL	MK48Z09-20	8K x 8	200 ns	80 mA	1 mA	
INTERRUPT OUTPUT	MK48Z09-25	8K x 8	250 ns	80 mA	1 mA	
ZEROPOWER SRAM	MK48Z19-15	8K x 8	150 ns	80 mA	1 mA	1-35
WITH POWER FAIL	MK48Z19-20	8K x 8	200 ns	80 mA	1 mA	
INTERRUPT OUTPUT	MK48Z19-25	8K x 8	250 ns	80 mA	1 mA	
V_{CC}=±10%						

BATTERY BACK-UP RAMs

Description	Part number	Organization	Access Time	I_{CC}	I_{BAT}	Page
BATTERY BACK-UP SRAM	MK48C02-15	2K x 8	150 ns	80 mA	50 μA	1-49
	MK48C02-20	2K x 8	200 ns	80 mA	50 μA	
	MK48C02-25	2K x 8	250 ns	80 mA	50 μA	
	MK48C02L-15	2K x 8	150 ns	80 mA	1 μA	
	MK48C02L-20	2K x 8	200 ns	80 mA	1 μA	
	MK48C02L-25	2K x 8	250 ns	80 mA	1 μA	

BiPORT™ DEVICES

Description	Part number	Organization	Access Time	Cycle	I_{CC}	Page
BiPORT FIFO	MK4501-65	512 x 9	65 ns	80 ns	80 mA	1-57
	MK4501-80	512 x 9	80 ns	100 ns	80 mA	
	MK4501-10	512 x 9	100 ns	120 ns	80 mA	
	MK4501-12	512 x 9	120 ns	140 ns	80 mA	
	MK4501-15	512 x 9	150 ns	175 ns	80 mA	
	MK4501-20	512 x 9	200 ns	235 ns	80 mA	
	MK4503-50	2048 x 9	50 ns	65 ns	120 mA	1-71
	MK4503-65	2048 x 9	65 ns	80 ns	120 mA	
	MK4503-80	2048 x 9	80 ns	100 ns	120 mA	
	MK4503-10	2048 x 9	100 ns	120 ns	120 mA	
	MK4503-12	2048 x 9	120 ns	140 ns	120 mA	
	MK4503-15	2048 x 9	150 ns	175 ns	120 mA	
	MK4503-20	2048 x 9	200 ns	235 ns	120 mA	
VERY HIGH SPEED CLOCKED FIFO	MK4505M-25	1024 x 5	15 ns	25 ns	100 mA	1-87
	MK4505M-33	1024 x 5	20 ns	33 ns	100 mA	
	MK4505M-50	1024 x 5	25 ns	50 ns	100 mA	
VERY HIGH SPEED CLOCKED FIFO (3 state outputs)	MK4505S-25	1024 x 5	15 ns	25 ns	100 mA	1-87
	MK4505S-33	1024 x 5	20 ns	33 ns	100 mA	
	MK4505S-50	1024 x 5	25 ns	50 ns	100 mA	
BiPORT RAM	MK4511-12	512 x 9	120 ns	150 ns	50 mA	1-105
	MK4511-15	512 x 9	150 ns	190 ns	50 mA	
	MK4511-20	512 x 9	200 ns	250 ns	50 mA	

STATIC RAMs

Description	Part number	Organization	Access Time	I_{CC}	I_{SB}	Page
FAST SRAM	MK4801A-55	1K x 8	55 ns	110 mA	—	1-117
	MK4801A-70	1K x 8	70 ns	110 mA	—	
	MK4801A-90	1K x 8	90 ns	110 mA	—	
	MK4801A-1	1K x 8	120 ns	110 mA	—	1-123
	MK4801A-2	1K x 8	150 ns	110 mA	—	
	MK4801A-3	1K x 8	200 ns	110 mA	—	
	MK4801A-4	1K x 8	250 ns	110 mA	—	
	ET2147H-1	4K x 1	35 ns	180 mA	30 mA	1-129
	ET2147H-2	4K x 1	45 ns	180 mA	30 mA	
	ET2147H-3	4K x 1	55 ns	180 mA	30 mA	
	ET2147H-4	4K x 1	55 ns	125 mA	20 mA	

VERY FAST CMOS STATIC RAM

Description	Part number	Organization	Access Time	I_{CC}	I_{SB}	Page
FAST $\overline{CS}$ ACCESS	MK41H66-20	16K x 1	20 ns	120 mA	—	1-135
	MK41H66-25	16K x 1	25 ns	120 mA	—	
	MK41H66-35	16K x 1	35 ns	120 mA	—	
	MK41L66-25	16K x 1	25 ns	60 mA	—	1-149
	MK41L66-35	16K x 1	35 ns	60 mA	—	
	MK41L66-45	16K x 1	45 ns	60 mA	—	
	MK41H69-20	4K x 4	20 ns	120 mA	—	1-163
	MK41H69-25	4K x 4	25 ns	120 mA	—	
	MK41H69-35	4K x 4	35 ns	120 mA	—	
	MK41L69-25	4K x 4	25 ns	60 mA	—	1-177
	MK41L69-35	4K x 4	35 ns	60 mA	—	
	MK41L69-45	4K x 4	45 ns	60 mA	—	
$\overline{CE}$ POWER-DOWN	MK41H67-20	16K x 1	20 ns	120 mA	50 µA	1-135
	MK41H67-25	16K x 1	25 ns	120 mA	50 µA	
	MK41H67-35	16K x 1	35 ns	120 mA	50 µA	
	MK41L67-25	16K x 1	25 ns	60 mA	50 µA	1-149
	MK41L67-35	16K x 1	35 ns	60 mA	50 µA	
	MK41L67-45	16K x 1	45 ns	60 mA	50 µA	
	MK41H68-20	4K x 4	20 ns	120 mA	50 µA	1-163
	MK41H68-25	4K x 4	25 ns	120 mA	50 µA	
	MK41H68-35	4K x 4	35 ns	120 mA	50 µA	
	MK41L68-25	4K x 4	25 ns	60 mA	50 µA	1-177
	MK41L68-35	4K x 4	35 ns	60 mA	50 µA	
	MK41L68-45	4K x 4	45 ns	60 mA	50 µA	
	MK41H87-25	64K x 1	25 ns	60 mA	50 µA	1-219
	MK41H87-35	64K x 1	35 ns	60 mA	50 µA	
	MK41H87-45	64K x 1	45 ns	60 mA	50 µA	
$\overline{CE}$/$\overline{OE}$	MK41H78-20	4K x 4	20 ns	120 mA	50 µA	1-191
	MK41H78-25	4K x 4	25 ns	120 mA	50 µA	
	MK41H78-35	4K x 4	35 ns	120 mA	50 µA	
	MK41L78-25	4K x 4	25 ns	60 mA	50 µA	1-205
	MK41L78-35	4K x 4	35 ns	60 mA	50 µA	
	MK41L78-45	4K x 4	45 ns	60 mA	50 µA	
$\overline{CE}$/$\overline{OE}$/$\overline{CLR}$	MK41H79-20	4K x 4	20 ns	120 mA	—	1-191
	MK41H79-25	4K x 4	25 ns	120 mA	—	
	MK41H79-35	4K x 4	35 ns	120 mA	—	
	MK41L79-25	4K x 4	25 ns	60 mA	—	1-205
	MK41L79-35	4K x 4	35 ns	60 mA	—	
	MK41L79-45	4K x 4	45 ns	60 mA	—	
CACHE MEMORY COMPARATOR TAGRAM™	MK41H80-20	4K x 4	20 ns	120 mA	—	1-229
	MK41H80-25	4K x 4	25 ns	120 mA	—	
	MK41H80-35	4K x 4	35 ns	120 mA	—	

MK48T02/12/03/13(B)-12/15/20/25

2K · 8 ZEROPOWER /TIMEKEEPER RAM

MEMORY COMPONENTS

FEATURES

- ☐ Integrated Ultra Low Power SRAM, Real Time Clock, Crystal, Power-fail Control Circuit and Battery
- ☐ BYTEWIDE™ RAM-like Clock Access
- ☐ BCD Coded Year, Month, Day, Date, Hours, Minutes and Seconds
- ☐ Software Controlled Clock Calibration for High Accuracy Applications
- ☐ Predicted Worst Case Battery Storage Life of 11 years @ 70°C
- ☐ Pin and Function Compatible with JEDEC Standard 2K x 8 SRAMs (MK48T02/12)
- ☐ Pin and functionally compatible with JEDEC Standard 2K × 8 EEPROM (MK48T03/13)
- ☐ Automatic Power-fail Chip Deselect/Write Protection
- ☐ Two Power-fail Deselect Trip Points Available
  MK48T02/03: 4.75 V ≥ V_{PFD} ≥ 4.50 V
  MK48T12/13: 4.50 V ≥ V_{PFD} ≥ 4.20 V

Part Number	Access Time	R/W Cycle Time
MK48TXX-12	120 ns	120 ns
MK48TXX-15	150 ns	150 ns
MK48TXX-20	200 ns	200 ns
MK48TXX-25	250 ns	250 ns

TRUTH TABLE (MK48T02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
<V_{CC} (Max) >V_{CC} (Min)	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
<V_{PFD} (Min) >V_{SO}	X	X	X	Power-Fail Deselect	High-Z
≤V_{SO}	X	X	X	Battery Back-up	High-Z

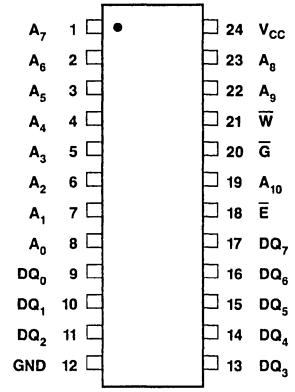


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{10}	Address Input	V_{CC}	+5 Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0 - DQ_7 Data In/Data Out			

TRUTH TABLE (MK48T03/13)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
<V_{CC} (Max) >V_{CC} (Min)	V_{IH} V_{IL} V_{IL} V_{IL}	X V_{IH} V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
<V_{PFD} (Min) >V_{SO}	X	X	X	Power-Fail Deselect	High-Z
≤V_{SO}	X	X	X	Battery Back-up	High-Z

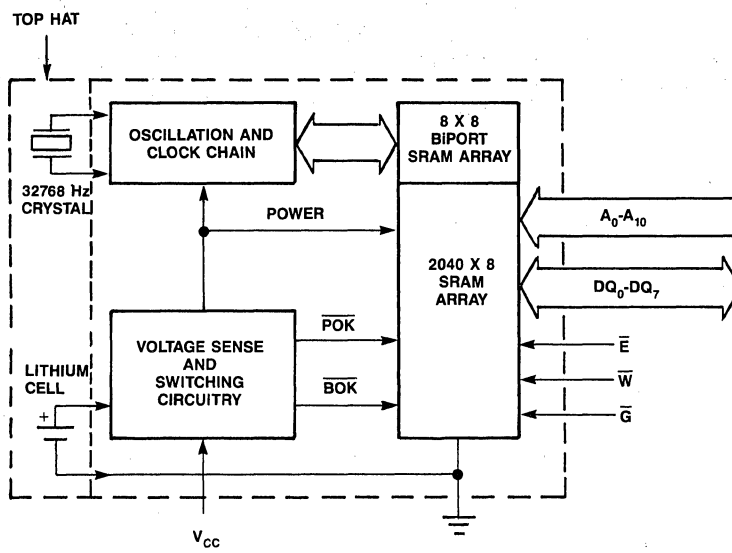


Figure 2. Block Diagram

DESCRIPTION

The MK48T02/12/03/13 combines a 2K x 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery, all in a single plastic DIP package. The MK48T02/12/03/13 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM, such as the 6116 or 5517. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the Clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 Hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a Control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T02/12/03/13 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T02/12/03/13 also has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

OPERATION

READ MODE

The MK48T02/12/03/13 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access (changing Addresses without removing Chip Enable) to any of the 2048 address locations in the static storage array. Valid data will be available at the Data I/O pins within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied.

If $\overline{E}$ or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{CEA}) or at Output Enable Access Time (t_{OEA}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until t_{AA}. If the Address inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold Time (t_{OH}) but will go indeterminant until the next t_{AA}.

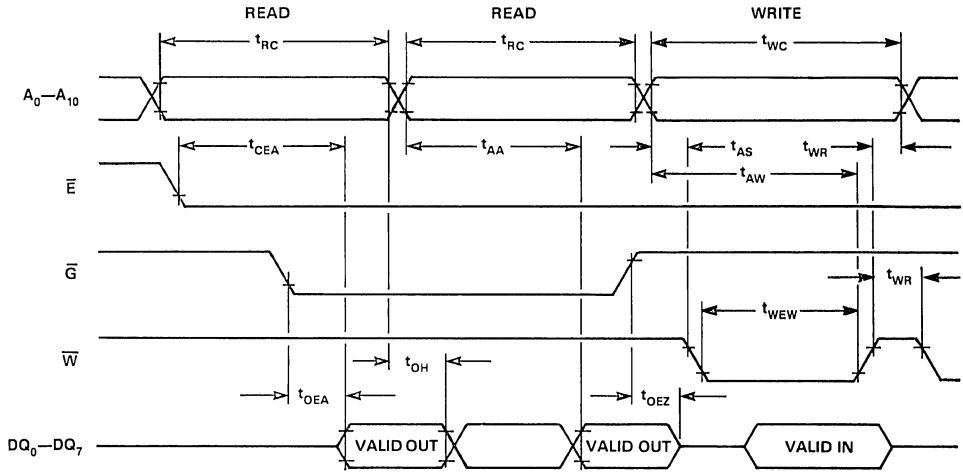


Figure 3. Read-Read-Write Timing

AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48TXX-12		MK48TXX-15		MK48TXX-20		MK48TXX-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

NOTE

1. Measured using the Output Load Diagram shown in Figure 13.

WRITE MODE

The MK48T02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The MK48T03/13 requires $\overline{G}$ to be held high in addition to $\overline{W}$ and $\overline{E}$ being held low. The start of a Write is referenced to the latter occurring falling edge of either W or $\overline{E}$, or the rising edge of $\overline{G}$ (MK48T03/13). A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$, or the falling edge of $\overline{G}$ (MK48T03/13). The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high, or $\overline{G}$ must return low (MK48T03/13) for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. The MK48T03/13 allow a user to easily overcome this problem by holding $\overline{G}$ low with the power-on reset signal. MK48T02/12 users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48T02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

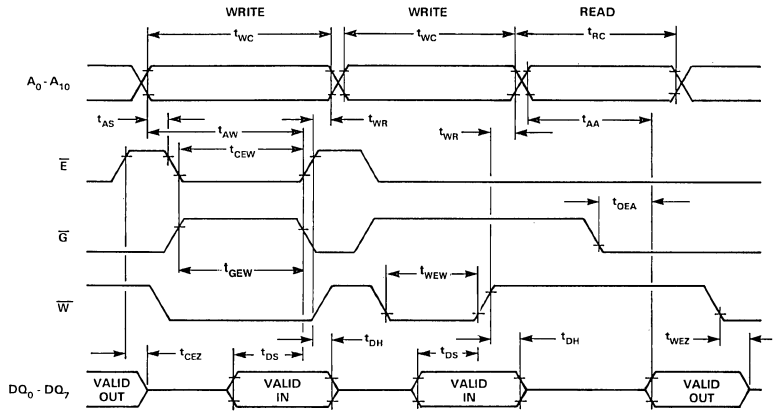


Figure 4. Write-Write-Read Timing

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48TXX-12		MK48TXX-15		MK48TXX-20		MK48TXX-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		150		200		250		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	
t_{GEW}	$\overline{G}$ to End of Write	75		90		120		160		ns	1

NOTE:
1. Applies to MK48T03/13 only

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be Halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting the Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values the actual TIMEKEEPER counters and allows normal operation to resume. The KS bit, FT bit and the bits marked with zeroes in Figure 5 must be written with zeroes to allow normal TIMEKEEPER and RAM operation.

ADDRESS	DATA								FUNCTION	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
7FF	—	—	—	—	—	—	—	—	YEAR	00-99
7FE	0	0	0	—	—	—	—	—	MONTH	01-12
7FD	0	0	—	—	—	—	—	—	DATE	01-31
7FC	0	FT	0	0	0	—	—	—	DAY	01-07
7FB	KS	0	—	—	—	—	—	—	HOUR	00-23
7FA	0	—	—	—	—	—	—	—	MINUTES	00-59
7F9	ST	—	—	—	—	—	—	—	SECONDS	00-59
7F8	W	R	S	—	—	—	—	—	CONTROL	

KEY: ST = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT S = SIGN BIT KS = KICK START

Figure 5. The MK48T02/12/03/13 Register Map

Calibrating the Clock

The MK48T02/12/03/13 is driven by a quartz crystal controlled oscillator with a nominal frequency of 32768 Hz.The crystal is mounted in the tophat along with the battery. A typical MK48T02/12/03/13 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed ± 35 ppm (Parts Per Million) oscillator frequency error at 25°C, which comes to about ±1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T02/12/03/13 design, however, employs periodic counter correction. The calibration circuit adds or subtracts count from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control register. Adding count speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. The byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 128 oscillator cycles, that is one tick of the divide by 256 stage. If a binary 1 is loaded into the register, only the first two minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

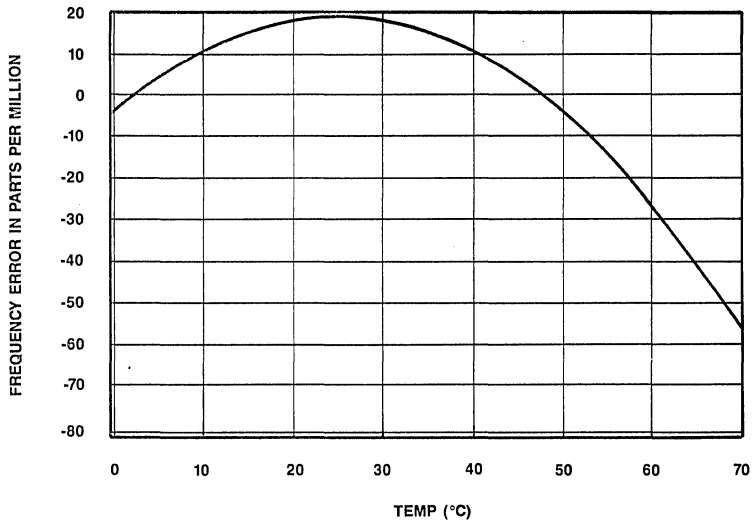


Figure 6. The MK48T02/12/03/13 Oscillator Frequency vs. Temperature

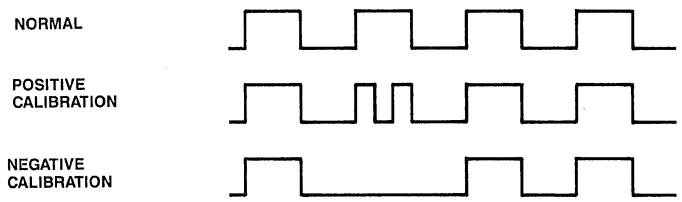


Figure 7. Adjusting the Divide by 256 Pulse Train

Therefore, each calibration step has the effect of adding or subtracting 256 oscillator cycles for every 125,829,120 (32768 x 60 x 64) actual oscillator cycles, that is 2.034 ppm of adjustment per calibration step; giving the user a ± 63.07 ppm calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 5.35 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T02/12/03/13 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ_0) of the Seconds register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.00512 Hz would indicate a +10 ppm (1−(512/512.00512)) oscillator frequency error, requiring a −5 (000101_2) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must be stable at Address 7F9 when reading the 512 Hz on DQ_0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds register is monitored by holding the MK48T02/12/03/13 in an extended read of the Second register, without having the Read bit set. The FT bit MUST be reset to a "0" for normal clock operations to resume.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB of the Seconds register. Setting it to a "1" stops the oscillator. In order to make the oscillator as stingy with current as possible, the oscillator is designed to require an extra "kick" to begin oscillation again. The extra kick is provided by the Kick Start (KS) bit, the MSB of the Hours register. To start the oscillator, implement the following procedure.

1. Set the Write Bit to "1".
2. Reset the Stop Bit to "0".
3. Set the Kick Start Bit to "1".
4. Reset the Write Bit to "0".
5. Wait 2 seconds.
6. Set the Write Bit to "1".
7. Reset the Kick Start Bit to "0".
8. Set the Correct time and date.
9. Reset the Write Bit to "0".

Note: Leaving the KS bit set will cause the Clock to draw excessive current and will shorten battery life.

DATA RETENTION MODE

With V_{CC} applied, the MK48T02/12/03/13 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48T02/03 has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48T12/13 has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48T02/12/03/13 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 8 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high or $\overline{G}$ low (MK48T03/13) as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

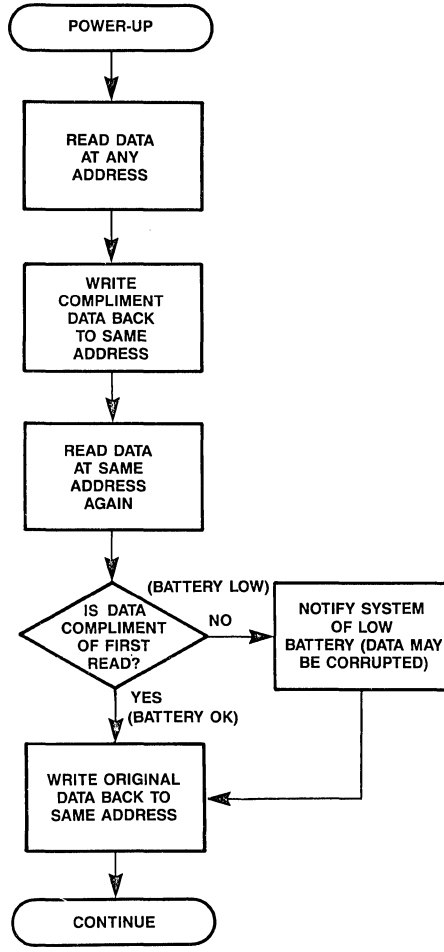


Figure 8. Checking the $\overline{BOK}$ Flag Status

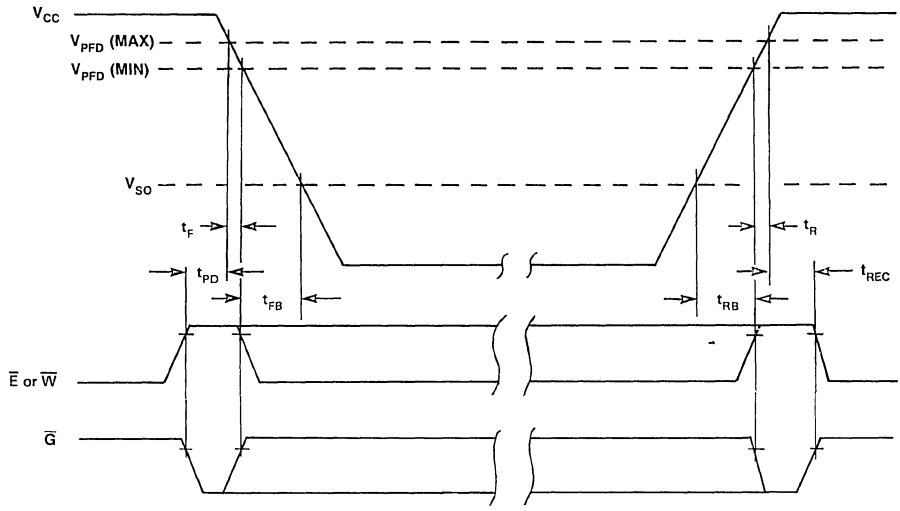


Figure 9. Power-Down/Power-Up Timing

DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48T02/03)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48T12/13)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} or $\overline{G}$ at V_{IL} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		μs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		μs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		μs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		μs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} or $\overline{G}$ at V_{IL} after Power Up	2		ms	

NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 μs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 μs may cause corruption of RAM data or stop the clock.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data or stop the clock.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T02/12/03/13 is expected to ultimately come to an end for one of two reasons; either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T02/12/03/13 are so low, they can be neglected in practical Storage Life calculations. Therefore, application of V_{CC} or turning off the oscillator can extend the effective Back-up System life.

Predicting Storage Life

Figure 10 illustrates how temperature affects Storage Life of the MK48T02/12/03/13 battery. As long as V_{CC} is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T02/12/03/13.

Storage Life predictions presented in Figure 10 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by Thomson - Mostek. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of Thomson - Mostek's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

> A Special Note: The summary presented in Figure 10 represents a conservative analysis of the data presently available. While Thomson - Mostek is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 10. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 10 indicates that a particular MK48T02/12/03/13 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48T02/12/03/13 is marked with a four digit manufacturing date code in the form YYWW (Example: 8625 = 1986, week 25).

Calculating Predicted Storage Life of the Battery

As Figure 10 indicates, the predicted Storage Life of the battery in the MK48T02/12/03/13 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 10. If the MK48T02/12/03/13 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = \frac{1}{[(TA_1/TT)/SL_1]+[(TA_2/TT)/SL_2]+\ldots+[(TA_n/TT)/SL_n]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

SL_1, SL_2, SL_n = Predicted Storage Life at Temp 1, Temp 2, etc. (See Figure 10).

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T02/12/03/13 is exposed to temperatures of 30°C (86°F) or less for 4672 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

Reading predicted $t_{1\%}$ values from Figure 10; SL_1 = 456 yrs., SL_2 = 175 yrs., SL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 =3650 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Storage Life} \geq \frac{1}{[(4672/8760)/456]+[(3650/8760)/175]+[(438/8760)/11.4]}$$

$\geq$ 126 yrs.

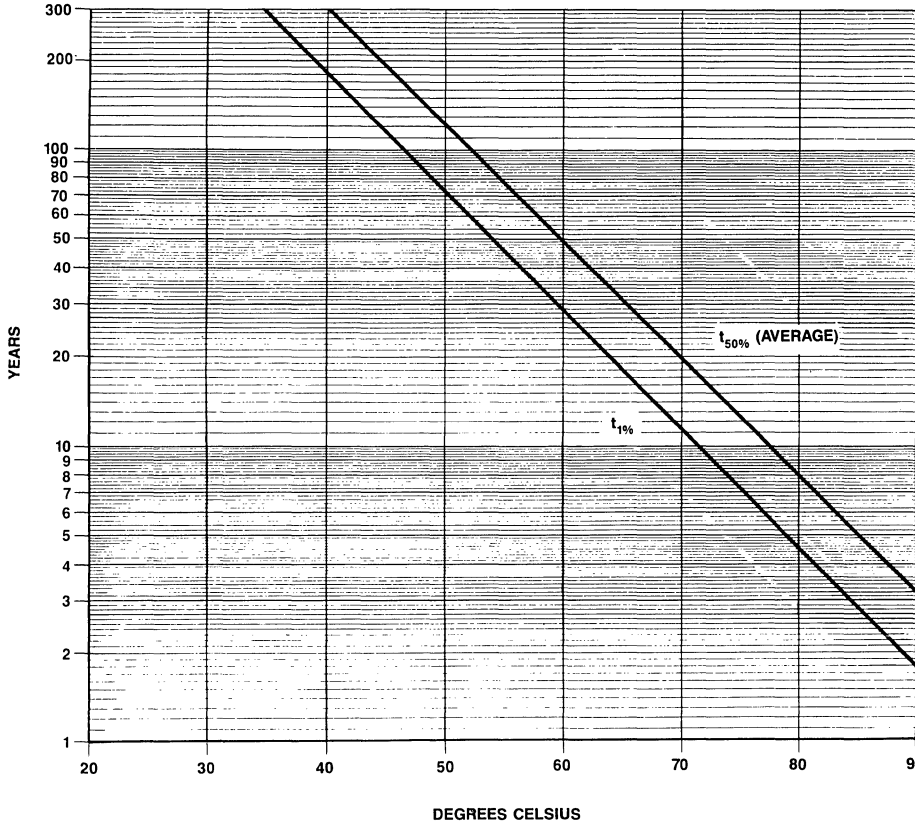


Figure 10. MK48T02/12/03/13 Predicted Battery Storage Life vs. Temperature

Predicting Capacity Consumption Life

The MK48T02/12/03/13 internal cell has a minimum rated capacity of 35 mAh. The device places a nominal combined RAM and TIMEKEEPER load of 1.2 μA on a typical internal 37 mAh lithium battery when the clock is running and the device is in Battery Back-up mode. At that rate, the MK48T02/12/03/13 will consume the cell's capacity in 29,166 hours, or about 3.3 years. But, as Figure 11 shows, Capacity Consumption can be spread over a much longer period of time.

Naturally, Back-up current varies with temperature. As Figure 12 indicates, the rate of Current Consumption by the MK48T02/12/03/13 with the clock running in Battery Back-up mode is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate consumption rates in a given design. As long as ambient temperature is held reasonably constant, expected Capacity Consumption life can be estimated by reading 0% V_{CC} Duty Cycle Capacity Consumption life directly from Figure 12, and dividing by the expected V_{CC} Duty Cycle (i.e. at 25°C with a 66% Duty Cycle, Capacity Consumption Life = 3.3/(1-.66) = 9.5 years).

If the MK48T02/12/03/13 spends an appreciable amount of time at a variety of temperatures, the same equation provided in the previous Storage Life section should be used to estimate Capacity Consumption life.

Example Consumption Life Calculation

Taking the same cash register/terminal used earlier, let's assume that the high and low temperature periods are the non-operating, Battery Back-up mode periods, and that the register is turned on 10 hours a day seven days per week. The two points of interest on the curves in Figure 12 will be the 25°C and the 70°C points.

Reading Capacity Life values from Figure 12; CL_1 = 3.3 yrs., CL_2 = 3.55 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 438 hrs./yr.

$$\text{Capacity Life} \geq \frac{1}{[(4672/8760)/3.3]+[(438/8760)/3.55]}$$

$$\geq 5.69 \text{ yrs.}$$

Estimating Back-up System Life

The procedure for estimating Back-up System Life is simple. Pick the lower of the two numbers. In the case calculated in the examples, that would be 5.69 years.

The fact is, since either mechanism, Storage Life or Capacity Consumption, can end the system's life, the end is marked by whichever occurs first.

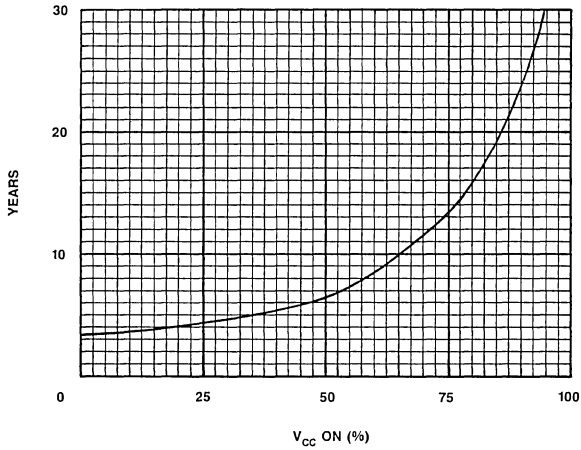


Figure 11. Typical Capacity Consumption Life at 25°C vs. V_{CC} Duty Cycle

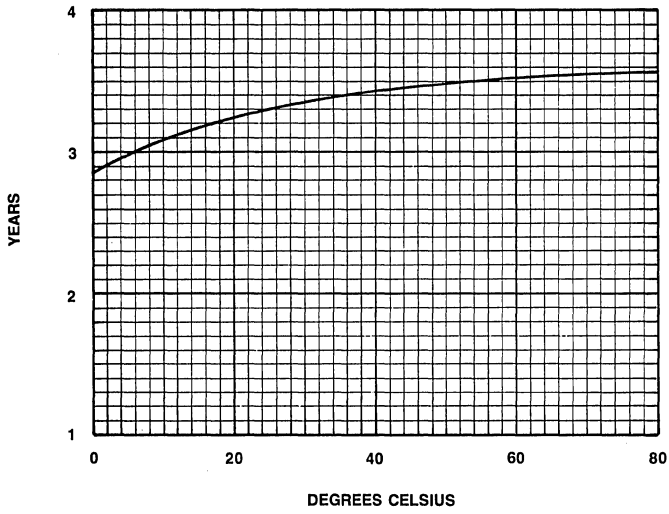


Figure 12. Current Consumption Life Over Temperature with 0% V_{CC} Duty Cycle

APPLICATION NOTE:

BINARY TO BCD, AND BCD TO BINARY CONVERSION

The MK48T02/12/03/13 presents and accepts TIMEKEEPER data in BCD format. Conversion to or from other formats can be executed in a single line of code, as the following example BASIC program demonstrates.

```
10 REM  BINARY TO BCD
20 DEF  FNA (X)=INT (X/10)*16+X-INT (X/10)*10
30 REM  BCD TO BINARY
40 DEF  FNB (X)=INT (X/16)*10+(XAND15)
```

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND ..... −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) ..... 0°C to +70°C
Ambient Storage (V_{CC} Off, Oscillator Off) Temperature ..... −20°C to +70°C
Total Device Power Dissipation ..... 1 Watt
Output Current Per Pin ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48T02/03)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48T12/13)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$ = V_{IH})		5	mA	4
I_{CC3}	CMOS Standby Current ($\overline{E}$ = V_{CC} −0.2 V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	5
I_{OL}	Output Leakage Current	−5	+5	μA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	6,7

NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with Control Bits set as follows: R = 1; W, ST, KS, FT = 0.
5. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
6. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{V\Delta}$ with ΔV = 3 volts and power supply at 5.0 V.
7. Measured with outputs deselected.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V

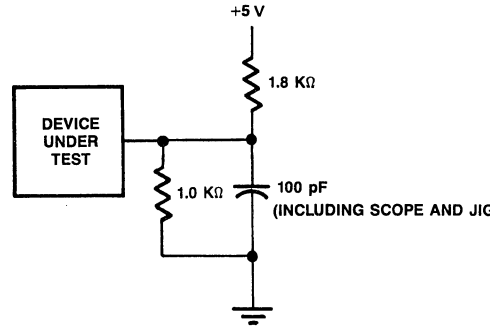
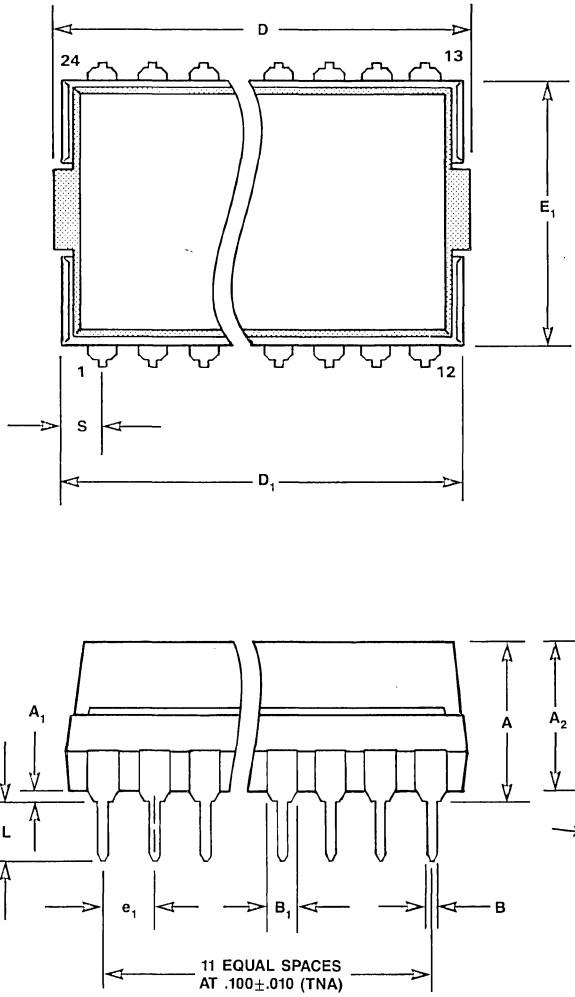


Figure 13. Equivalent Output Load Diagram

PACKAGE DESCRIPTION
B Package
24 Pin



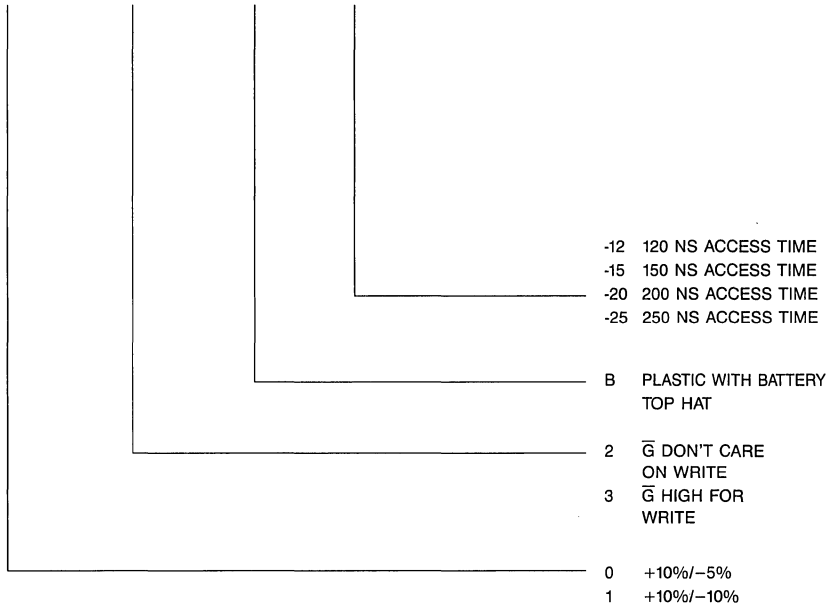
	DIM.	INCHES MIN	INCHES MAX	NOTES
BATTERY ONLY	D	—	1.295	
	Z	.550	.570	
	A	.320	.380	
	A_2	.300	.360	
	E_1	.530	.550	
	B	.015	.021	4
	B_1	.045	.070	
	C	.008	.014	4
24 PIN PLASTIC D.I.L. ONLY	D_1	—	1.270	1
	E	.530	.640	
	e_A	.600	.700	3
	e_1	.090	.110	
	L	.120	.150	
	A_1	.015	.030	2
	S	.060	.090	

NOTES:

1. Overall length includes .010 in. flash on either end of the package.
2. Package standoff to be measured per JEDEC requirements.
3. Measured from centerline to centerline at lead tips.
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

ORDERING INFORMATION

MK48T	X	X	B	-XX
DEVICE FAMILY	V_{CC} RANGE	$\overline{G}$ FUNCTION	PACKAGE	SPEED



MK48Z02/03/12/13(B)-12/15/20/25

2K x 8 ZEROPOWER® RAM

MEMORY COMPONENTS

FEATURES

- ☐ Predicted worst case battery life of 11 years @ 70°C
- ☐ Data retention in the absence of power
- ☐ Data security provided by automatic write protection during power failure
- ☐ Pin and functional compatibility with 2K × 8 Byte Wide Static RAMs (MK48Z02/12)
- ☐ Pin and function compatible with 2K × 8 EEPROMs (MK48Z03/13)
- ☐ +5 Volt only Read/Write
- ☐ Conventional SRAM write cycles
- ☐ Full CMOS-440 mW active; 5.5 mW standby
- ☐ 24-Pin Dual in Line package, JEDEC pinouts
- ☐ Read-cycle time equals write-cycle time
- ☐ Low-Battery Warning
- ☐ Two power-fail deselect trip points available
  MK48Z02/03 $4.75V \geq V_{PFD} \geq 4.50V$
  MK48Z12/13 $4.50V \geq V_{PFD} \geq 4.20V$

Part Number	Access Time	R/W Cycle Time
MK48ZXX-12	120 ns	120 ns
MK48ZXX-15	150 ns	150 ns
MK48ZXX-20	200 ns	200 ns
MK48ZXX-25	250 ns	250 ns

TRUTH TABLE (MK48Z02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$<V_{CC}$ (Max) $>V_{CC}$ (Min)	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$<V_{PFD}$ (Min) $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

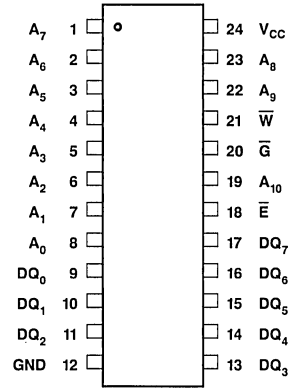


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7 Data In/Data Out			

TRUTH TABLE (MK48Z03/13)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$<V_{CC}$ (Max) $>V_{CC}$ (Min)	V_{IH} V_{IL} V_{IL} V_{IL} V_{IL}	X V_{IH} V_{IL} V_{IH} V_{IL}	X V_{IL} V_{IH} V_{IH} V_{IL}	Deselect Write Read Read Read	High-Z D_{IN} D_{OUT} High-Z High-Z
$<V_{PFD}$ (Min) $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

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DESCRIPTION

The MK48Z02/03/12/13 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02/03/12/13 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

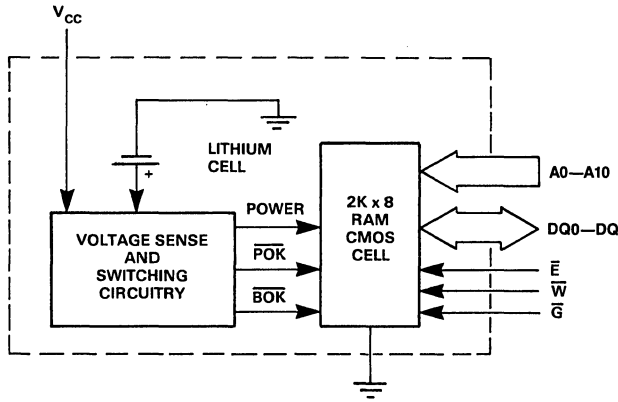


Figure 2. Block Diagram

OPERATION

Read Mode

The MK48Z02/03/12/13 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

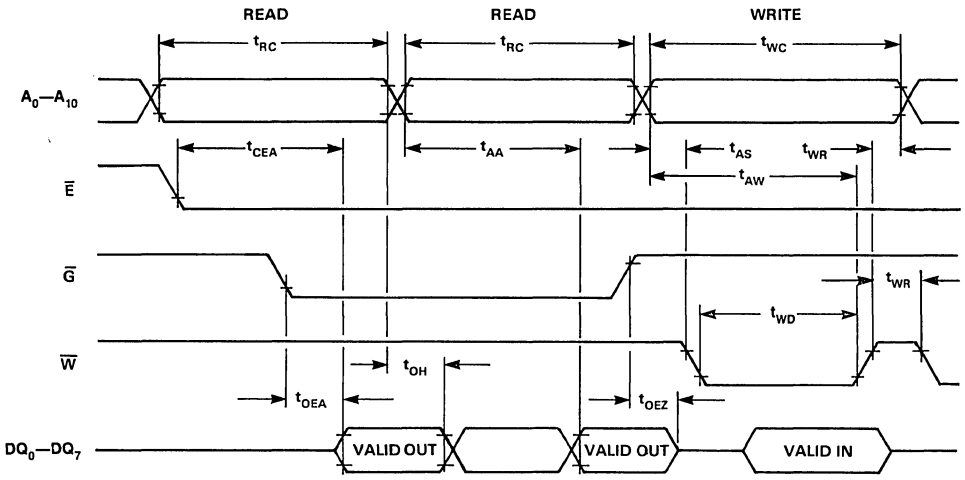


Figure 3. Read-Read-Write Timing

AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48ZXX-12		MK48ZXX-15		MK48ZXX-20		MK48ZXX-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

NOTE

1. Measured using the Output Load Diagram shown in Figure 8.

WRITE MODE

The MK48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The MK48Z03/13 requires $\overline{G}$ to be held high in addition to $\overline{W}$ and $\overline{E}$ being held low. The start of a Write is referenced to the latter occurring falling edge of either W or $\overline{E}$, or the rising edge of $\overline{G}$ (MK48Z03/13). A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$, or the falling edge of $\overline{G}$ (MK48Z03/13). The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high, or $\overline{G}$ must return low (MK48Z03/13) for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. The MK48Z03/13 allow a user to easily overcome this problem by holding $\overline{G}$ low with the power-on reset signal. MK48Z02/12 users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

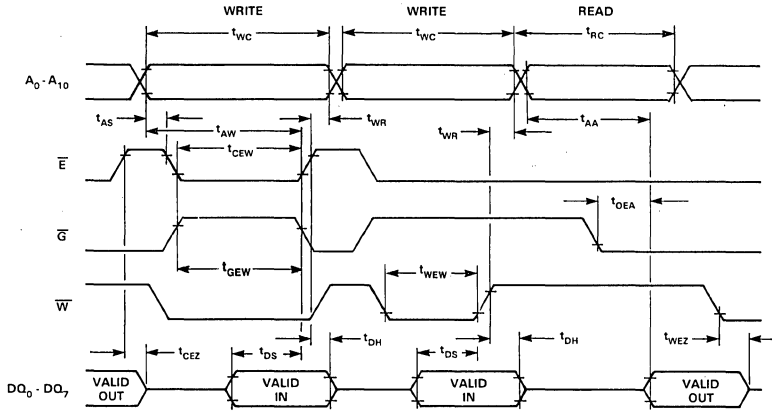


Figure 4. Write-Write-Read Timing

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48ZXX-12		MK48ZXX-15		MK48ZXX-20		MK48ZXX-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		150		200		250		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	
t_{GEW}	$\overline{G}$ to End of Write	75		90		120		160		ns	1

NOTE:
1. Applies to MK48Z03/13 only

DATA RETENTION MODE

With V_{CC} applied, the MK48Z02/12/03/13 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48Z02/03 has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48Z12/13 has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48Z02/12/03/13 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high or $\overline{G}$ low (MK48Z03/13) as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

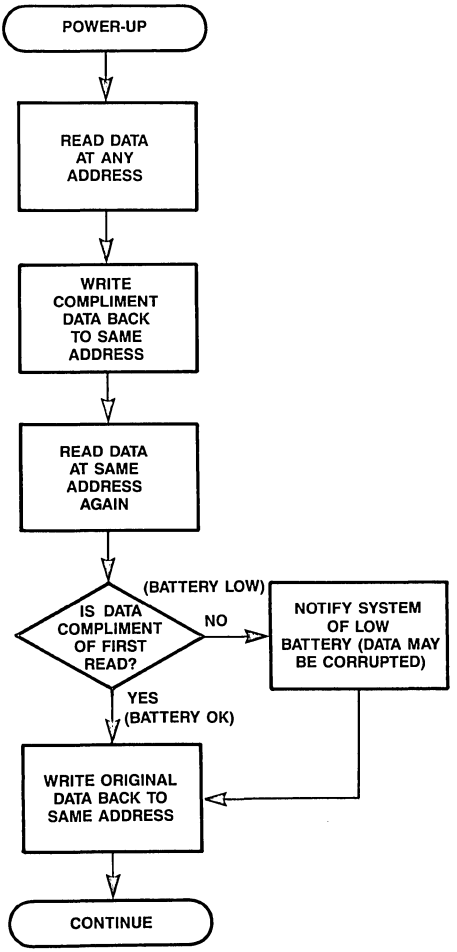


Figure 5. Checking the $\overline{BOK}$ Flag Status

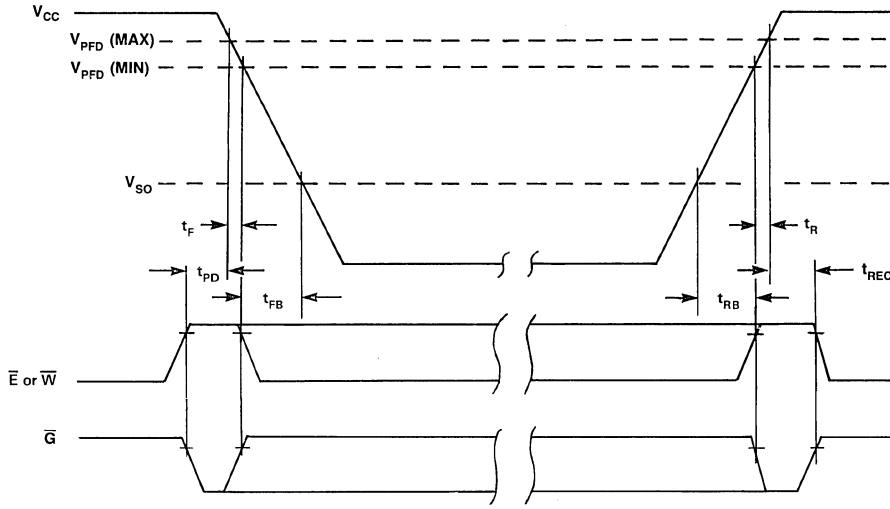


Figure 6. Power-Down/Power-Up Timing

DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48Z02/03)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z12/13)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} or $\overline{G}$ at V_{IL} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		μs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		μs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		μs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		μs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} or $\overline{G}$ at V_{IL} after Power Up	2		ms	

NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 μs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 μs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MK48Z02/03/12/13 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z02/03/12/13 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by Thomson - Mostek. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of Thomson - Mostek's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While Thomson - Mostek is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z02/03/12/13 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 12 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z02/03/12/13 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 7 indicates, the predicted life of the battery in the MK48Z02/03/12/13 is a function of temperature. The back-up current required by the memory matrix in the MK48Z02/03/12/13 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MK48Z02/03/12/13 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

$$TT = \text{Total Time} = TA_1 + TA_2 + \ldots + TA_n$$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z02/03/12/13 is exposed to temperatures of 30°C (86°F) or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 5256 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

Reading predicted typical life values from Figure 7; BL_1 = 456 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 =5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/456]+[(5256/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 116.5 \text{ yrs.}$$

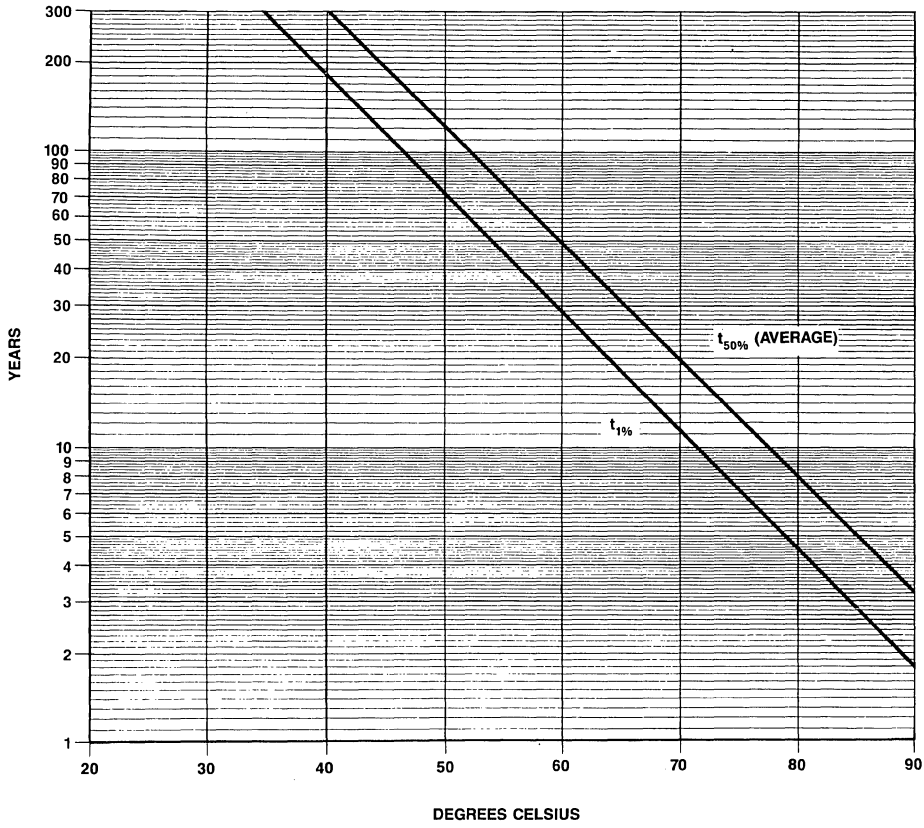


Figure 7. MK48Z02/03/12/13 Predicted Battery Storage Life vs Temperature

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND ..... −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) ..... 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature ..... −40°C to +85°C
Total Device Power Dissipation ..... 1 Watt
Output Current Per Pin ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z02/03)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48Z12/13)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le +70°C$) (V_{CC} (max) $\ge V_{CC} \ge V_{CC}$ (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \ge V_{CC} - 0.2$ V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	4
I_{OL}	Output Leakage Current	−5	+5	μA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,5

NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $GND \le V_I \le V_{CC}$ and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} (MK48Z02/03)	4.75 V to 5.5 V
V_{CC} (MK48Z12/13)	4.5 V to 5.5 V

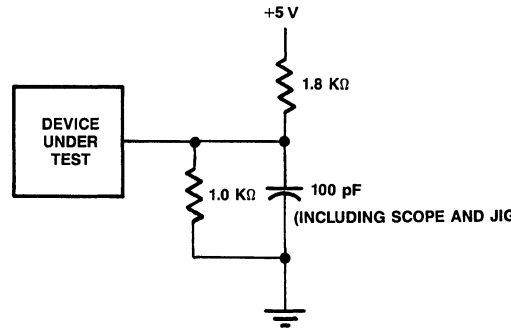


Figure 8. Output Load Diagram

ORDERING INFORMATION

MK48Z	X	X	B	-XX
DEVICE FAMILY	V_{CC} RANGE	$\overline{G}$ FUNCTION	PACKAGE	SPEED

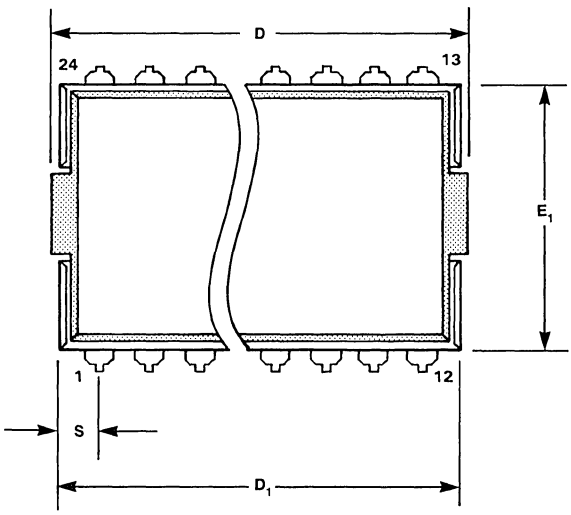
-12 120 NS ACCESS TIME
-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

B PLASTIC WITH BATTERY TOP HAT

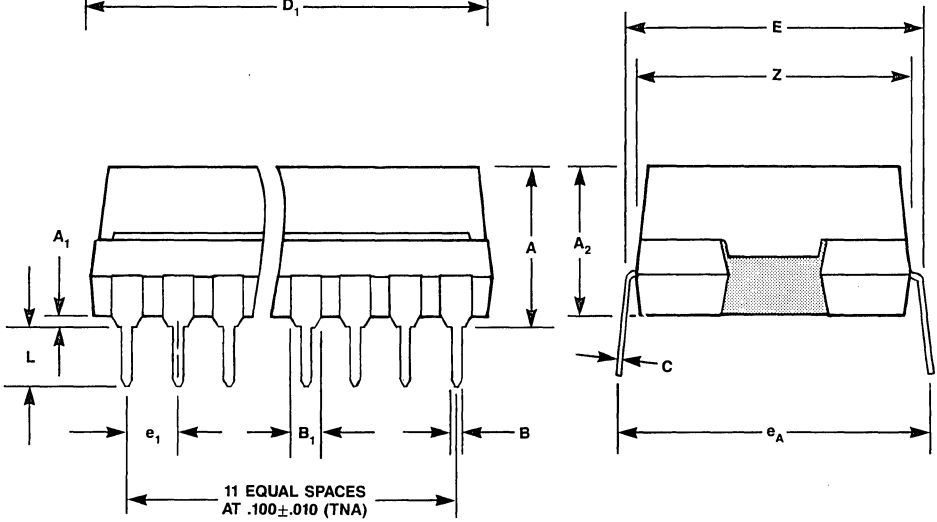
2 $\overline{G}$ DON'T CARE ON WRITE
3 $\overline{G}$ HIGH FOR WRITE

0 +10%/–5%
1 +10%/–10%

PACKAGE DESCRIPTION
B Package
24 Pin



	DIM.	INCHES MIN	INCHES MAX	NOTES
BATTERY ONLY	D	—	1.295	
	Z	.550	.570	
	A	.320	.380	
	A_2	.300	.360	
	E_1	.530	.550	
	B	.015	.021	4
	B_1	.045	.070	
	C	.008	.014	4
24 PIN PLASTIC D.I.P. ONLY	D_1	—	1.270	1
	E	.530	.640	
	e_A	.600	.700	3
	e_1	.090	.110	
	L	.120	.150	
	A_1	.015	.030	2
	S	.060	.090	



NOTES:

1. Overall length includes .010 in. flash on either end of the package.
2. Package standoff to be measured per JEDEC requirements.
3. Measured from centerline to centerline at lead tips.
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

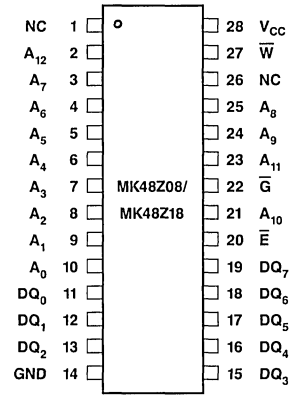
MK48Z08/18/09/19(B)-15/20/25

8K × 8 ZEROPOWER® RAM

FEATURES

- ☐ Predicted Worst Case Battery Life of 11 years @ 70°C
- ☐ Data retention in the absence of power
- ☐ Power Fail Interrupt Output (MK48Z09/19)
- ☐ Extra data security provided by early write protection during power failure (MK48Z08/09)
- ☐ Direct replacement for volatile 8K x 8 Byte Wide Static RAM
- ☐ +5 Volt only Read/Write
- ☐ Unlimited write cycles
- ☐ 28-Pin Dual In Line package, JEDEC pinout
- ☐ Read-cycle time equals write-cycle time
- ☐ Low-Battery Warning
- ☐ Two power-fail deselect trip points available
  MK48Z08/09: $4.75V \geq V_{PFD} \geq 4.50V$
  MK48Z18/19: $4.50V \geq V_{PFD} \geq 4.20V$

Part Number	Access Time	R/W Cycle Time
MK48Z08B-25	250 ns	250 ns
MK48Z08B-20	200 ns	200 ns
MK48Z08B-15	150 ns	150 ns
MK48Z18B-25	250 ns	250 ns
MK48Z18B-20	200 ns	200 ns
MK48Z18B-15	150 ns	150 ns
MK48Z09B-25	250 ns	250 ns
MK48Z09B-20	200 ns	200 ns
MK48Z09B-15	150 ns	150 ns
MK48Z19B-25	250 ns	250 ns
MK48Z19B-20	200 ns	200 ns
MK48Z19B-15	150 ns	150 ns



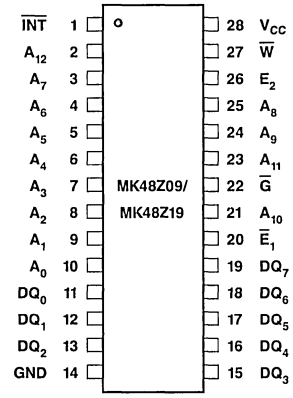


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{12}	Address Inputs	V_{CC} System Power (+5 V)
$\overline{E_1}$, E_2	Chip Enable	$\overline{W}$ Write Enable
GND	Ground	$\overline{G}$ Output Enable
DQ_0 - DQ_7	Data In/Data Out	$\overline{INT}$ Power Fail Interrupt Output

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DESCRIPTION

The MK48Z08/MK48Z18/MK48Z09/MK48Z19 is a 65,536-bit, Non-Volatile Static RAM, organized 8K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 8K x 8 static RAM, directly conforming to the popular Byte Wide 28-pin DIP package (JEDEC). MK48Z08/18/09/19 also matches the pinning of 2764 EPROM and 8K x 8 EEPROMs. Like other static RAM, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

TRUTH TABLE MK48Z08/18

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
$<V_{CC}$ (max)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
$>V_{CC}$ (min)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
$<V_{PFD}$ (min) $>V_{SO}$	X	X	X	Deselect	High Z	CMOS Standby
$\leq V_{SO}$	X	X	X	Deselect	High Z	Battery Back-up Mode

TRUTH TABLE MK48Z09/19

V_{CC}	$\overline{E_1}$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
$<V_{CC}$ (max)	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	D_{IN}	Active
$>V_{CC}$ (min)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
$<V_{PFD}$ (min) $>V_{SO}$	X	X	X	X	Deselect	High Z	CMOS Standby
$\leq V_{SO}$	X	X	X	X	Deselect	High Z	Battery Back-up Mode

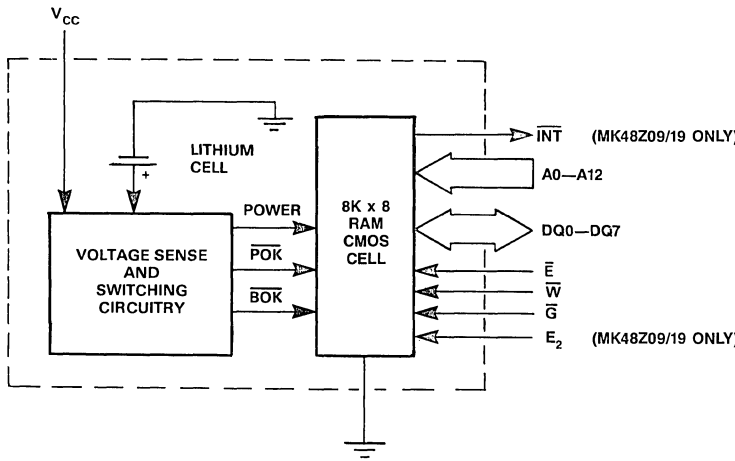


Figure 2. Block Diagram

OPERATION

Read Mode

The MK48Z08/18/09/19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E_1}$ (Chip Enable) is low, and E_2 is high (MK48Z09/19), providing a ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs (A_n) defines which one of 8,192 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the Chip Enable and $\overline{G}$ access times are satisfied. If Chip Enable or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{OEA} or t_{CEA1} or t_{CEA2}), rather than the address. The state of the eight Data I/O signals is controlled by the Chip Enable and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

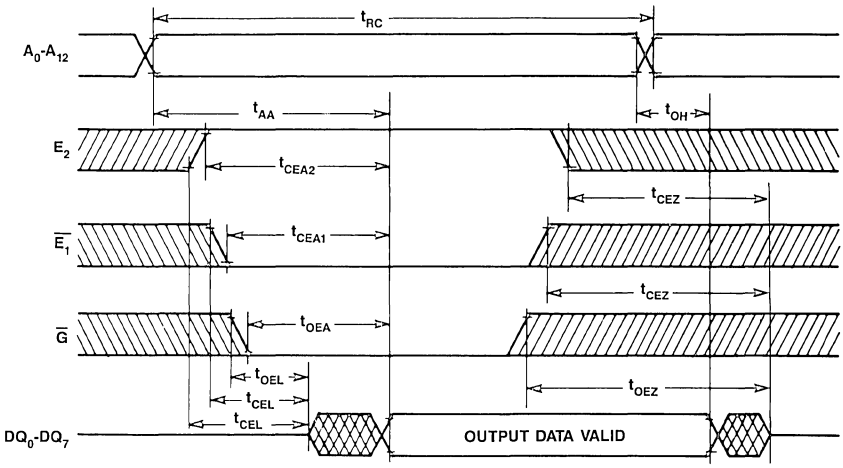


Figure 3. Read Cycle

READ CYCLE
AC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ +70°C) (V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max))

		MK48ZXX-15		MK48ZXX-20		MK48ZXX-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150	—	200	—	250	—	ns	
t_{AA}	Address Access Time	—	150	—	200	—	250	ns	
t_{CEA1}	$\overline{E_1}$ Access Time	—	150	—	200	—	250	ns	
t_{CEA2}	E_2 Access Time	—	150	—	200	—	250	ns	
t_{OEA}	Output Enable to Output in Valid	—	75	—	100	—	125	ns	
t_{CEL}	Chip Enable ($\overline{E_1}$, E_2) to Output In Low-Z	10	—	10	—	15	—	ns	
t_{OEL}	Output Enable to Output Low-Z	5	—	5	—	10	—	ns	
t_{CEZ}	Chip Enable ($\overline{E_1}$, E_2) Output In High-Z	—	75	—	100	—	125	ns	
t_{OEZ}	Output Enable to Output High-Z	—	60	—	80	—	100	ns	
t_{OH}	Output Data Hold Time	20	—	20	—	25	—	ns	

Write Mode

The MK48Z08/18/09/19 is in the Write Mode whenever the $\overline{W}$ and $\overline{E_1}$ are low and E_2 (MK48Z09/19) is high. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E_1}$, or the rising edge of E_2 (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E_1}$ or the falling edge of E_2 (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E_1}$ or $\overline{W}$ must return high or E_2 (MK48Z09/19) must return low for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid t_{DS} prior to the end of write and must remain valid for t_{DH} afterward.

Because $\overline{G}$ is a Don't Care in Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

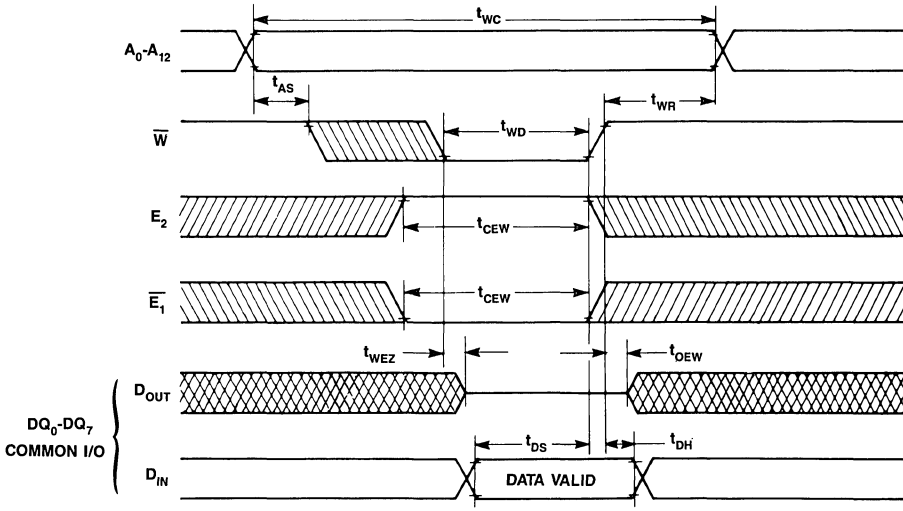


Figure 4. Write Cycle 1 ($\overline{W}$ Controlled Write)

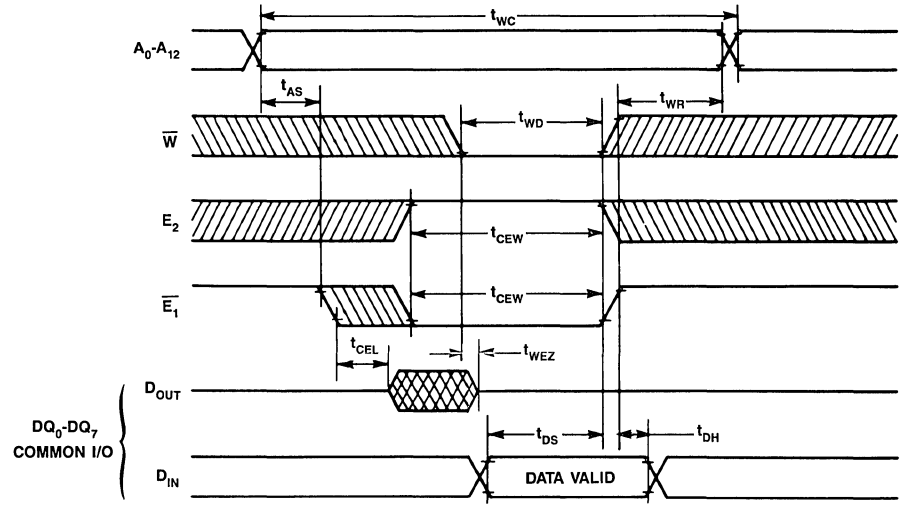


Figure 5. Write Cycle 2 ($\overline{E_1}$ Controlled Write)

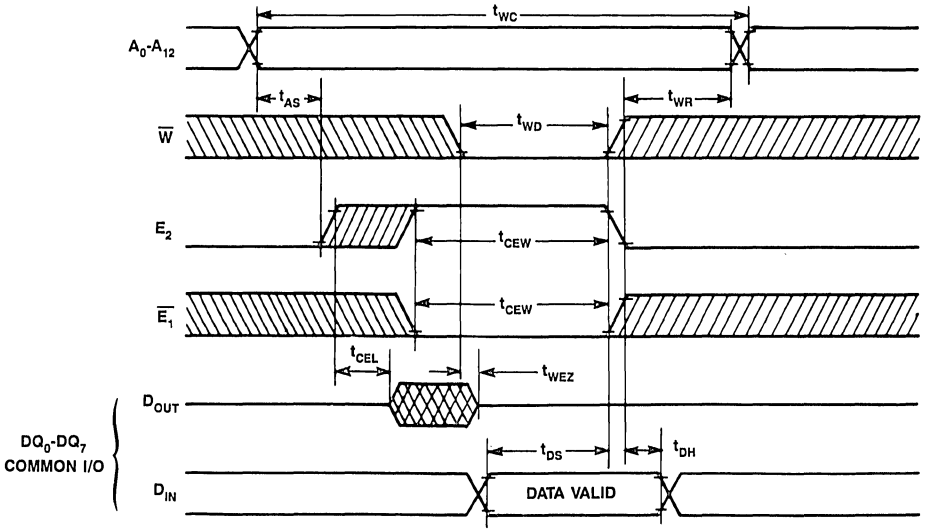


Figure 6. Write Cycle 3 (E_2 Controlled Write)

WRITE CYCLE
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$) (V_{CC} (min) $\leq V_{CC} \leq V_{CC}$ (max))

		MK48ZXX-15		MK48ZXX-20		MK48ZXX-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	150	—	200	—	250	—	ns	
t_{WD}	Write Pulse Width	100	—	150	—	200	—	ns	
t_{CEW}	Chip Selection to End of Write	130	—	180	—	230	—	ns	
t_{AS}	Address Set up Time	0	—	0	—	0	—	ns	
t_{WR}	Write Recovery Time	10	—	10	—	10	—	ns	
t_{WEZ}	$\overline{W}$ to Output High-Z	—	75	—	100	—	125	ns	
t_{DS}	Data Setup Time	70	—	80	—	90	—	ns	
t_{DH}	Data Hold Time	5	—	5	—	5	—	ns	

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		μs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		μs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		μs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		μs	
t_{REC}	$\overline{E_1}$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power-Up	100		μs	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	μs	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		100	μs	4
t_{FB}	V_{PFD} (Min) to V_{SO}	10		μs	

DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)

($0°C \leq T_A \leq +70°C$)

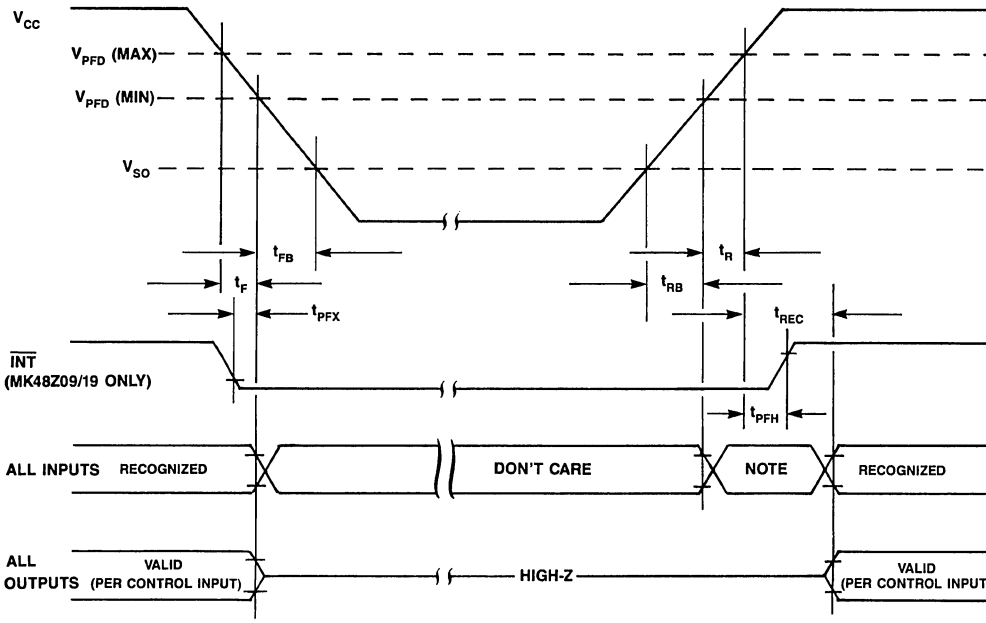
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48Z08/09)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z18/19)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 40 μs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 μs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.
4. INT may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

CAUTION

Negative Undershoots Below −0.3 volts are not allowed on any pin while in Battery Back-up mode.



NOTE:
Inputs may or may not be recognized at this time.
Caution should be taken to keep $\overline{E_1}$ or $\overline{W}$ in the high state or E_2 low as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Figure 7. Power Down/Power-Up Timing

Power Fail and Data Retention

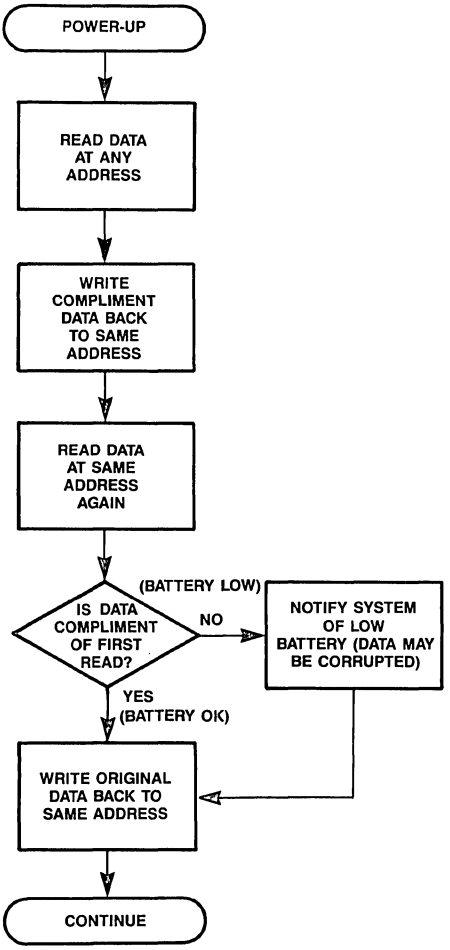
With V_{CC} applied, the MK48Z08/18/09/19 operates as a static RAM. The Power-Fail Detect Circuit of the MK48Z08/18/09/19 constantly monitors V_{CC}. Because the reference voltage applied to the detector/comparator is stabilized over temperature, the Power-Fail Detect trip point remains within the V_{PFD} min/max window under all rated conditions. Once deselection has occurred, all inputs and outputs are "Don't Cares" and may have anywhere from −0.3 to V_{CC} +0.3 volts applied to them with absolutely no effect upon the RAM.

As V_{CC} falls below approximately V_{SO} volts, the power switching circuit connects the lithium battery to supply power to the RAM.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above approximately V_{SO} volts. As V_{CC} rises from V_{PFD} (min) to V_{PFD} (max), the battery voltage is checked. If the voltage is too low, an Internal Battery Not OK ($\overline{BOK}$) flag will be set.

Normal RAM operation can resume t_{REC} after V_{CC} reaches V_{PFD} (max). Caution should be taken to keep $\overline{E_1}$, or $\overline{W}$ in the high state or E_2 low as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins.

The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 8 illustrates how a $\overline{BOK}$ check routine could be structured. Note: $\overline{E_1}$ on the MK48Z09/19 and $\overline{E}$ on the MK48Z08/18 need not be active to clear the $\overline{BOK}$ Flag. Care should be taken not to inadvertantly clear the $\overline{BOK}$ Flag.



NOTE:
Users not concerned about data retention beyond battery end of life, need not to check $\overline{BOK}$ status, however, make sure to use a dummy write cycle on power-up when not checking $\overline{BOK}$ to avoid losing first write cycle.

Figure 8. Checking the $\overline{BOK}$ Flag Status

DATA RETENTION TIME

About Figure 9

Figure 9 illustrates how expected MK48Z08/18/09/19 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z08/18/09/19 spends in battery back-up mode.

Battery life predictions presented in Figure 9 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by Thomson - Mostek. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of Thomson - Mostek's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 9 represents a conservative analysis of the data presently available. While Thomson - Mostek is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 9. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 9 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 22 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 22 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z08/18/09/19 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 9 indicates, the predicted life of the battery in the MK48Z08/18/09/19 is a function of temperature. The back-up current required by the memory matrix in the MK48Z08/18/09/19 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 9. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

$$TT = \text{Total Time} = TA_1 + TA_2 + \ldots + TA_n$$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 9).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z08/18/09/19 is exposed to temperatures of 30°C (86°F) or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 5256 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

Reading predicted t1% life values from Figure 9; BL_1 = 456 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 =5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/456]+[(5256/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 116.5 \text{ yrs.}$$

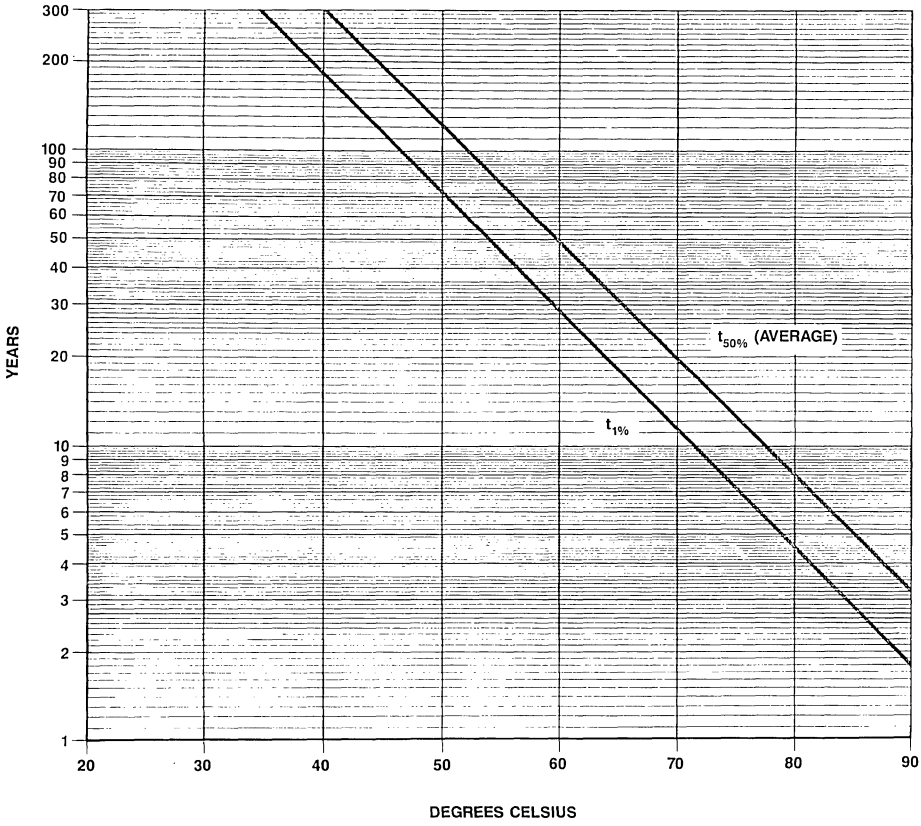


Figure 9. MK48Z08/18/09/19 Predicted Battery Life vs Temperature

ABSOLUTE MAXIMUM RATINGS*

Total Power Dissipation ..... 1.0 watt
Output Current Per Pin ..... 10 mA
Voltage On Any Pin Relative To GND ..... −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) ..... 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature ..... −40°C to +85°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z08/09)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48Z18/19)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E_1}$ = V_{IH} or E_2 = V_{IL})		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E_1}$ ≥ V_{CC} −0.2 V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	4
I_{LO}	Output Leakage Current	−5	+5	μA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	CONDITIONS	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

NOTES
1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} MK48Z08/09	4.75 V to 5.5 V
V_{CC} MK48Z18/19	4.5 V to 5.5 V

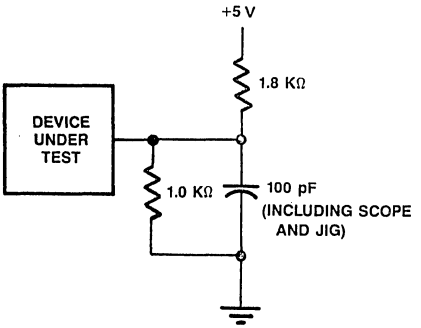


Figure 10. Output Load Diagram

ORDERING INFORMATION

MK48Z	X	X	B	-XX
DEVICE FAMILY	V_{CC} RANGE	SPECIAL FUNCTIONS	PACKAGE	SPEED

-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

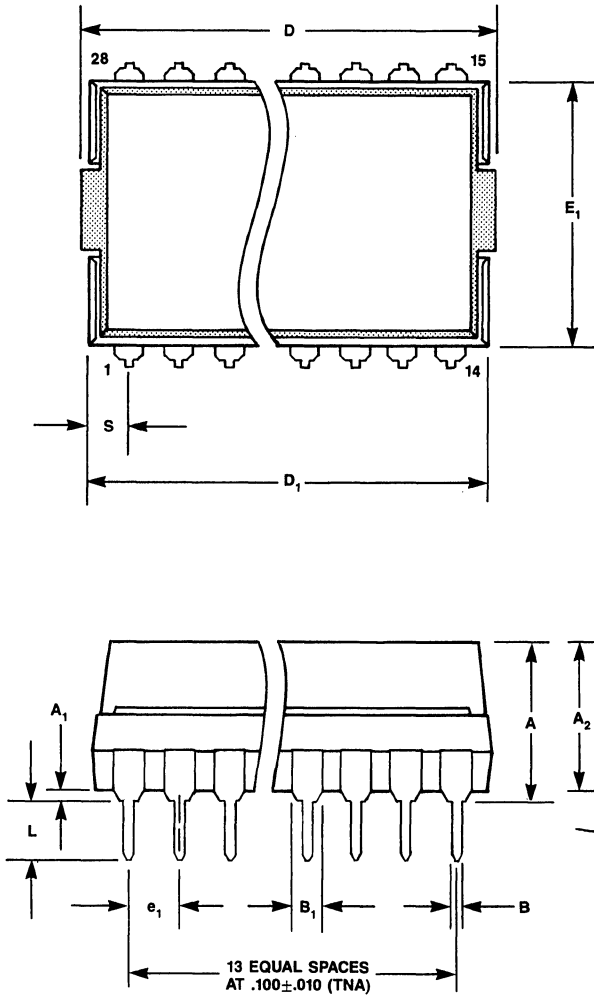
B PLASTIC WITH BATTERY TOP HAT

8 SINGLE CHIP SELECT
9 TWO CHIP SELECTS AND INTERRUPT OUT

0 V_{CC} = +10%/−5%
1 V_{CC} = +10%/−10%

PACKAGE DESCRIPTION
B Package
28 Pin

	DIM.	INCHES MIN	INCHES MAX	NOTES
BATTERY ONLY	D	—	1.495	
	Z	.550	.570	
28 PIN PLASTIC D.I.P. ONLY	A	.320	.380	
	A_2	.300	.360	
	E_1	.530	.550	
	B	.015	.021	4
	B_1	.045	.070	
	C	.008	.014	4
	D_1	—	1.470	1
	E	.530	.640	
	e_A	.600	.700	3
	e_1	.090	.110	
	L	.120	.150	
	A_1	.015	.030	2
	S	.060	.090	



NOTES:
1. Overall length includes .010 in. flash on either end of the package.
2. Package sstandoff to be measured per JEDEC requirements.
3. Measured from centerline to centerline at lead tips.
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

MK48C02 • MK48C02L(N) 15/20/25

2K x 8 BATTERY BACK-UP RAM

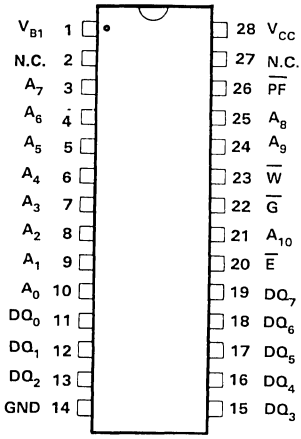
FEATURES

- Ideal Non-Volatile RAM with a single external Lithium Cell
- Data security provided by automatic write protection during power failure
- No battery drain during normal operating conditions
- Ultra low battery drain during battery back-up
- Data retention down to 1.8 V
- Low battery warning
- Power fail detect signal available for memory expansion
- Fully static Chip Enable and Output Enable facilitate bus control
- High performance

Part No.	Access Time	R/W Cycle Time
MK48C02-15 MK48C02L-15	150 ns	150 ns
MK48C02-20 MK48C02L-20	200 ns	200 ns
MK48C02-25	250 ns	250 ns

PIN CONNECTIONS

Figure 1

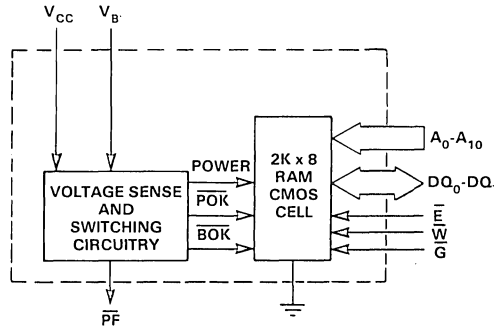


PIN NAMES

A_0 - A_{10} = Address Inputs	E = Chip Enable
DQ_0 - DQ_7 = Data In/Data Out	W = Write Enable
GND = Ground	G = Output Enable
V_{CC} = Power (+5 V) VB = Battery Inputs	PF = Power Fail Detect Output

BLOCK DIAGRAM

Figure 2



TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
≤5.5 volts	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
≥4.75 volts	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
<4.5 volts	X	X	X	Write Protect	High Z	CMOS Standby

DESCRIPTION

The MK48C02/MK48C02L is a CMOS RAM with integral power fail support circuitry for battery backup applications. The fully static RAM uses a HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V_{CC} transients. Battery voltage is checked on each power-up with the status communicated via the V_{LB} pin. A precision voltage detector, nominally set at 4.60 volts, write-protects the RAM to prevent inadvertent loss of data when V_{CC} is out of tolerance. In this way, all input and output pins (including $\overline{E}$ and $\overline{W}$) become "don't care". The device permits full functional ability of the RAM for V_{CC} above 4.75 volts, provides write protection for V_{CC} less than 4.50 volts, and maintains data in the absence of V_{CC} with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5 na) because all power-consuming circuitry is turned off. The low battery drain allows the use of a long life Lithium primary cell.

OPERATION

Read Mode

The MK48C02/MK48C02L is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) define which one of 2048 bytes of data is to be accessed.

Valid data will be available to the eight Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Write Mode

The MK48C02/MK48C02L is in the Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are in the low state. The latter occurring falling edge of either $\overline{W}$ or $\overline{E}$ will determine the start of the Write Cycle. Therefore, t_{AS}, t_{WD}, and t_{CEW} are referenced to this latter occurring edge of $\overline{E}$ or $\overline{W}$. The Write Cycle is terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$. The addresses must be held valid throughout the cycle. $\overline{W}$ must return to the high state for a minimum of t_{WR} prior to the initiation of another cycle. If the output bus has been enabled ($\overline{E}$ and $\overline{G}$ low), then $\overline{W}$ will disable the outputs in t_{WEZ} from its falling edge; however care must be taken to avoid a potential bus contention. Data-In must be valid t_{DS} prior to the rising edge of $\overline{E}$ or $\overline{W}$ and must remain valid for t_{DH} after the rising edge of $\overline{E}$ or $\overline{W}$.

Data Retention Mode

In the normal mode of operation, the MK48C02/MK48C02L operates as a static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically write-protect itself in the V_{CC} range between 4.75 and 4.50 volts as long as the slew rate (t_f) specification is satisfied. The open collector output, $\overline{PF}$, will go low when the RAM is write-protected. By holding $\overline{E}$ or $\overline{W}$ above V_{IH} for a minimum of t_{PD} before power-down, incomplete write cycles to the RAM will be avoided. Once V_{CC} falls below 4.50 volts, all inputs to the RAM become "don't care" and may be as high as 5.50 volts.

As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the external energy source to supply power to the RAM. In the Data Retention mode, the current drain on the energy source will be less than I_{BAT} max.

This redundant battery scheme has been provided to enhance data retention reliability. If only one battery is used, VB_1 and VB_2 should be connected together.

When V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the external energy source. As V_{CC} rises from a 4.50 to 4.75 volts, the external energy source is checked. If the voltage is below V_{LB}, a BOK (Battery OK) flag will be set. Normal RAM operation can resume t_{REC} after V_{CC} exceeds 4.75 volts. Whenever V_{CC} is between 4.50 and 4.75 volts, $\overline{E}$ or $\overline{W}$ must be in the high state to prevent inadvertant write cycles. The BOK flag can be checked on the first write cycle after a power-up. This write cycle will not be executed if either battery is below V_{LB}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.3 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.5 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,6
V_B	Battery Voltage	1.8	3.5	V	1,7
V_{LB}	Low Battery Warning (I_{LOAD} = 10μA)	1.8	2.4	V	1
ΔV_B	Battery Switch Differential Voltage		0.7	V	

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts + 10% - 5%)

SYM	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current			80	mA	5
I_{CC2}	TTL Standby Current ($\overline{E}$ = V_{IH})			3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ - 0.2 V)			1	mA	
I_{IL}	Input Leakage Current (Any Input)		-1	+1	μA	2
I_{OL}	Output Leakage Current		-5	+5	μA	2
V_{OH}	Output Logic "1" Voltage (I_{OUT} = -1.0 mA)		2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)			0.4	V	
V_{PFL}	$\overline{PF}$ Logic "0" Voltage I_{OUT} = 50 μA			0.4	V	
I_{BAT}	Battery Back-Up Current V_B = 3.5 V, V_{CC} = 0 V	MK48C02L		1	μA	
		MK48C02		50	μA	
I_{CHG}	Battery Charging Current V_B = 1.8 V, V_{CC} = 5.5 V		-5	+5	na	

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 V + 10% – 5%)

SYM	PARAMETER	MK48C02-15 MK48C02L-15		MK48C02-20 MK48C02L-20		MK48C02-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	3
t_{CEA}	Chip Enable Access Time		150		200		250	ns	3
t_{CEZ}	Chip Enable Data Off Time		35		40		50	ns	
t_{OEA}	Output Enable Access Time		70		80		90	ns	3
t_{OEZ}	Output Enable Data Off Time		35		40		50	ns	
t_{OH}	Output Hold from Address Change	15		15		15		ns	
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{WD}	Write Pulse Width	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{WEZ}	Write Enable Data Off Time		50		60		80	ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

CAPACITANCE

(T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	8
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,9

NOTES:

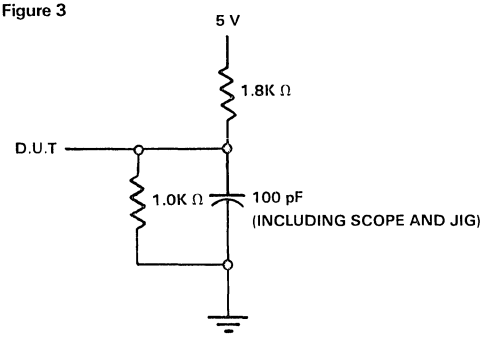
1. All voltages referenced to GND.
2. Measured with GND $\leq V_I \leq V_{CC}$ and outputs deselected.
3. Measured with load as shown in Figure 3.
4. Output buffer is deselected.
5. I_{CC1} measured with outputs open.
6. Negative spikes of –1.0 volts allowed for up to 10 ns once per cycle.
7. Battery voltages below V_B min may allow loss of data.
8. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$, with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels:	0.8 V or 2.2 V

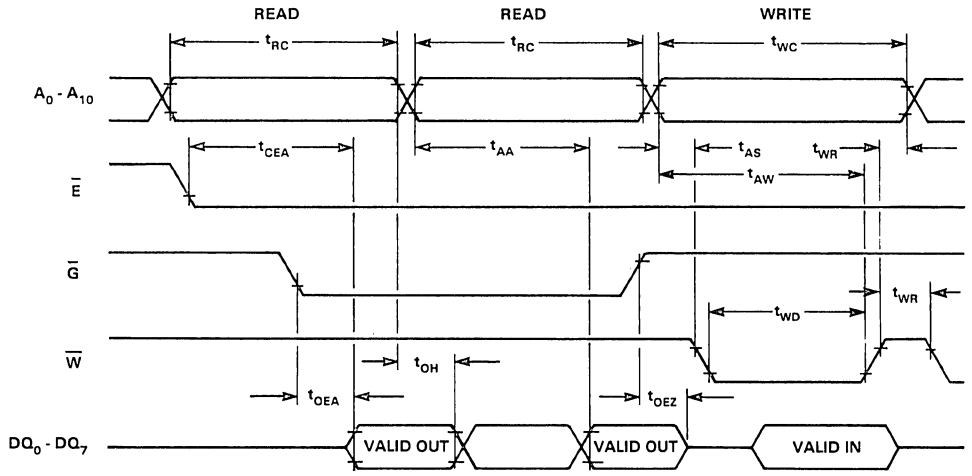
OUTPUT LOAD DIAGRAM

Figure 3



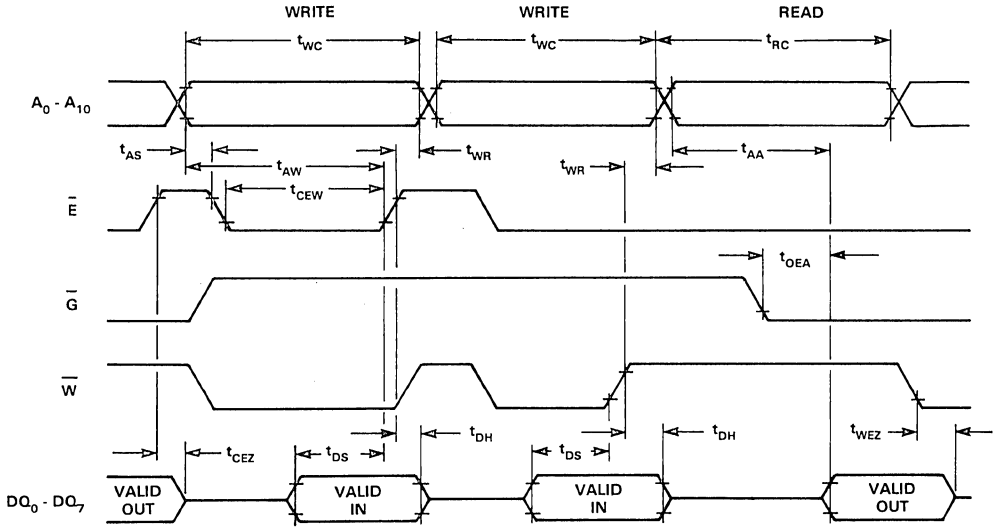
TIMING DIAGRAM

Figure 4



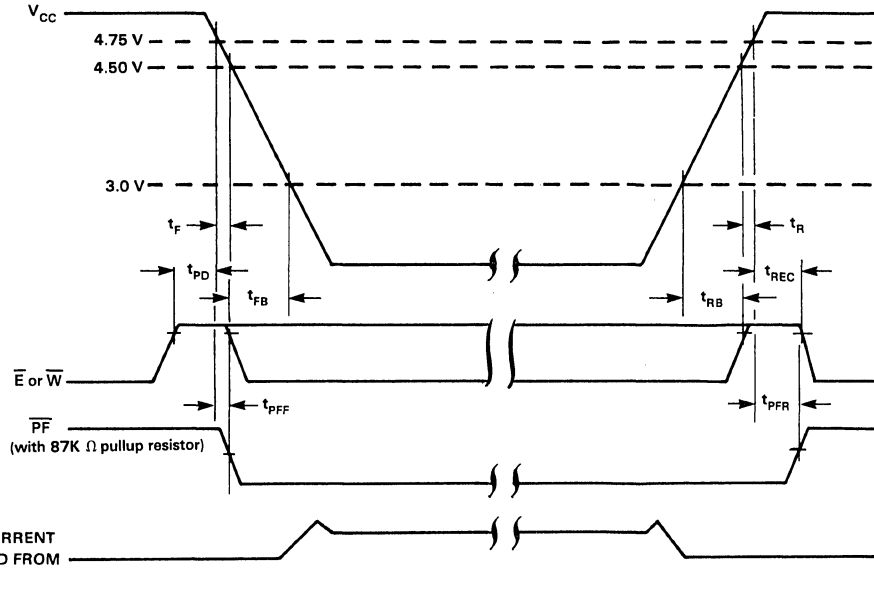
TIMING DIAGRAM

Figure 5



POWER-DOWN, POWER-UP CONDITIONS

Figure 6



POWER-DOWN/POWER-UP TIMING

(0°C ≤ T_A ≤ +70°C)

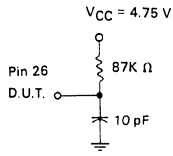
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		μS	
t_F	V_{CC} slew from 4.75 V to 4.50 V ($\overline{E}$ or $\overline{W}$ at V_{IH})	300		μS	
t_{FB}	V_{CC} slew from 4.50 to 3.0 V	10		μS	
t_{RB}	V_{CC} slew from 3.0 V to 4.50 V	1		μS	
t_R	V_{CC} slew from 4.50 to 4.75 V ($\overline{E}$ or $\overline{W}$ at V_{IH})	0		μS	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	
t_{PFF}	$\overline{PF}$ at logic '0' (V_{CC} ≤ 4.50 V)		0	ns	1,2
t_{PFR}	$\overline{PF}$ at logic '1' (V_{CC} ≥ 4.75 V)		2	ms	2

NOTES:

1. $\overline{PF}$ starts to go low when V_{CC} < 4.75 V. It is guaranteed to be at a logic '0' when V_{CC} ≤ 4.50 V.

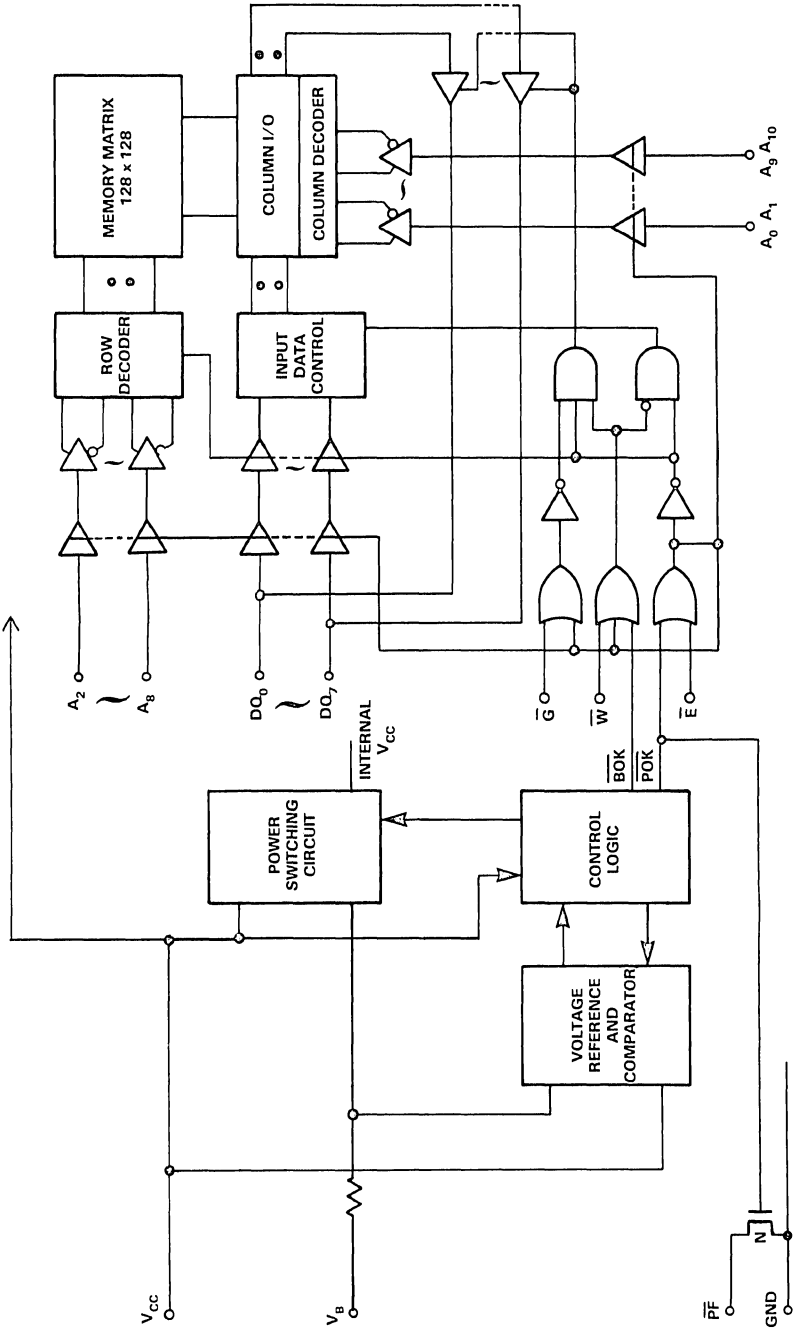
WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

2. Measured with load



2K x 8 BATTERY BACK-UP RAM FUNCTIONAL DIAGRAM

Figure 7



ORDERING INFORMATION

PART NO.	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK48C02N-15	150 ns	Plastic	0° to 70°C
MK48C02LN-15	150 ns	Plastic	0° to 70°C
MK48C02N-20	200 ns	Plastic	0° to 70°C
MK48C02LN-20	200 ns	Plastic	0° to 70°C
MK48C02N-25	250 ns	Plastic	0° to 70°C

MK4501(N)-65*/80/10/12/15/20

512 x 9 CMOS BiPORT FIFO

MEMORY COMPONENTS

FEATURES

- ☐ First-In, First-Out Memory Based Architecture
- ☐ Flexible 512 x 9 organization
- ☐ Low Power HCMOS technology
- ☐ Asynchronous and simultaneous read/write
- ☐ Bidirectional applications
- ☐ Fully expandable by word width or depth
- ☐ Empty and full warning flags
- ☐ Retransmit capability
- ☐ High performance

Part No.	Access Time	R/W Cycle Time
MK4501-65	65 ns	80 ns
MK4501-80	80 ns	100 ns
MK4501-10	100 ns	120 ns
MK4501-12	120 ns	140 ns
MK4501-15	150 ns	175 ns
MK4501-20	200 ns	235 ns

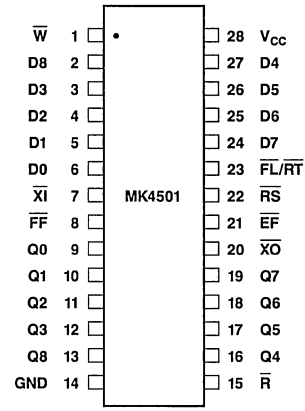


Figure 1. Pin Connections

PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion In
$\overline{R}$	= Read	$\overline{XO}$	= Expansion Out
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL}/\overline{RT}$	= First Load/ Retransmit	$\overline{EF}$	= Empty Flag
		V_{CC}	= 5 Volts
D	= Data In	GND	= Ground
Q	= Data Out		

DESCRIPTION

The MK4501 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

BiPORT is a trademark of Mostek Corporation.
* The MK4501N-65 specifications are preliminary.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4501 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the MK4501 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4501 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4501 allows connecting the read, write, data in, and data out lines of the MK4501s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins as appropriate (see the Expansion Timing section for a more complete discussion).

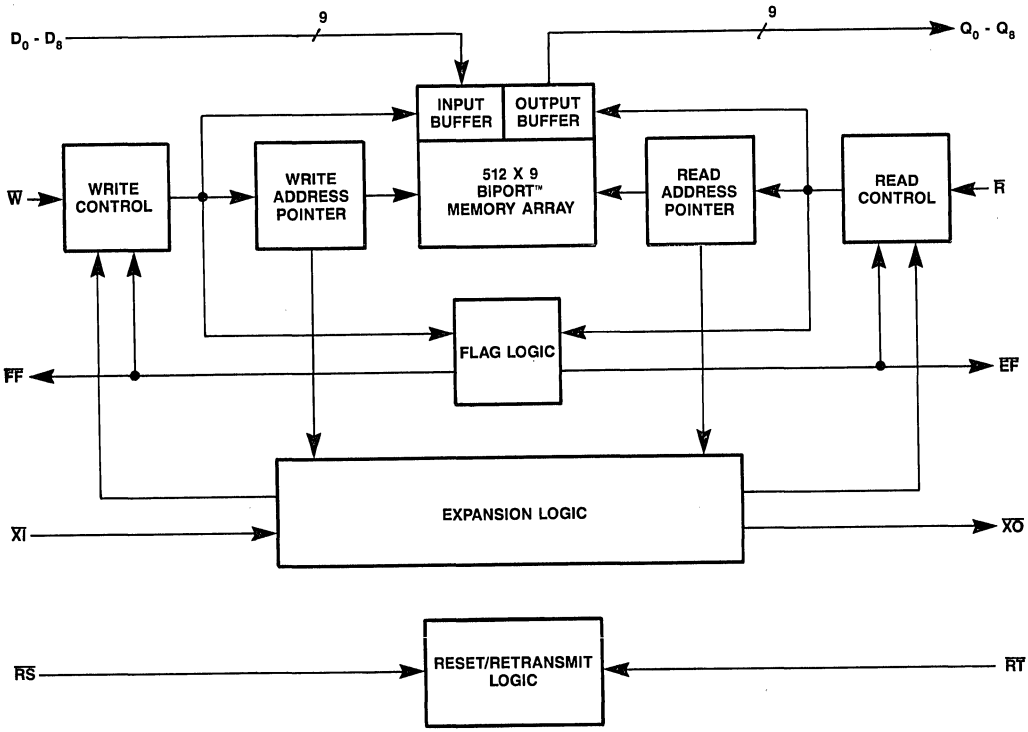


Figure 2. MK4501 Block Diagram

WRITE MODE

The MK4501 initiates a Write Cycle (see Figure 3) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4501 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

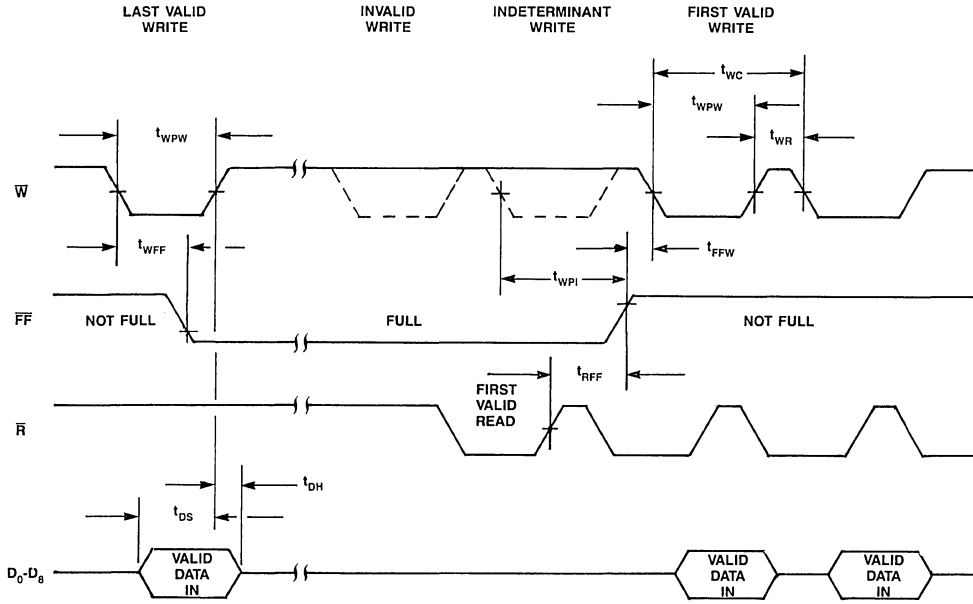


Figure 3. Write and Full Flag Timing

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	4501-65		4501-80		4501-10		4501-12		4501-15		4501-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	20		25		35		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		75		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		75		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant		35		35		35		35		35		35	ns	2

READ MODE

The MK4501 initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4501 provides a fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

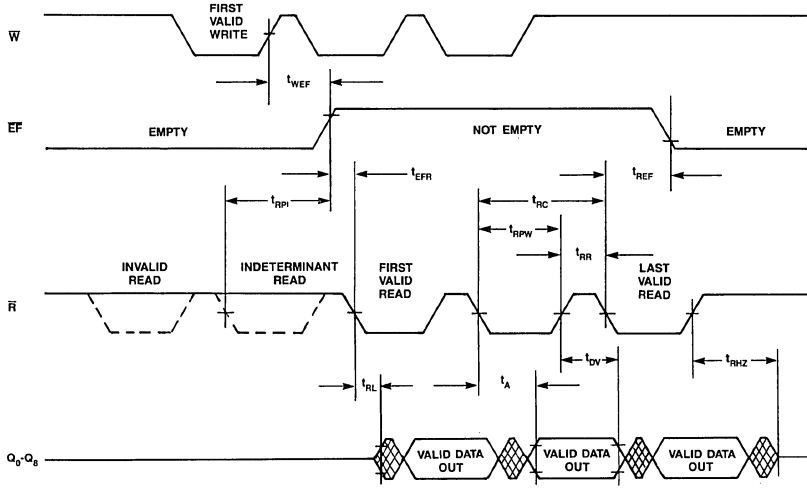


Figure 4. Read and Empty Flag Timing

AC ELECTRICAL CHARACTERISTICS

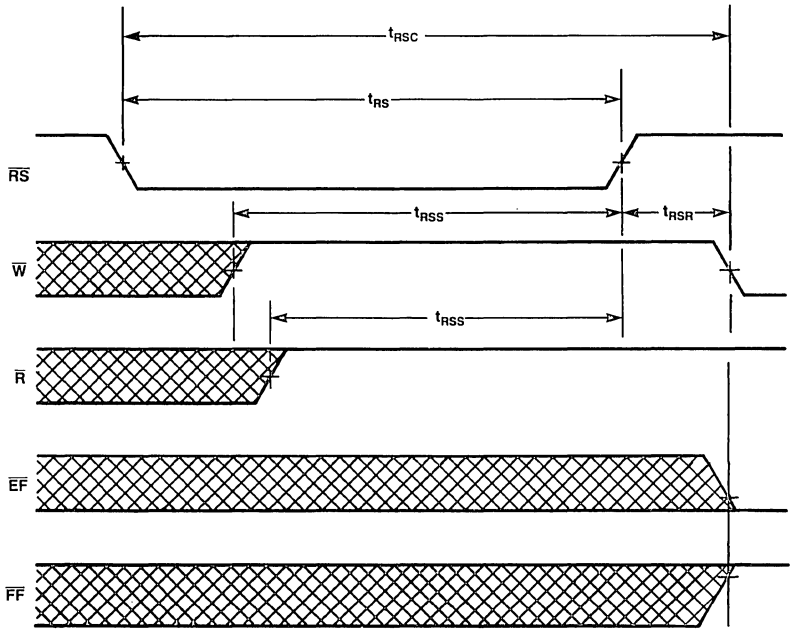
($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	20		20		20		20		25		25		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

RESET

The MK4501 is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.



NOTE
$\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Figure 5. Reset

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

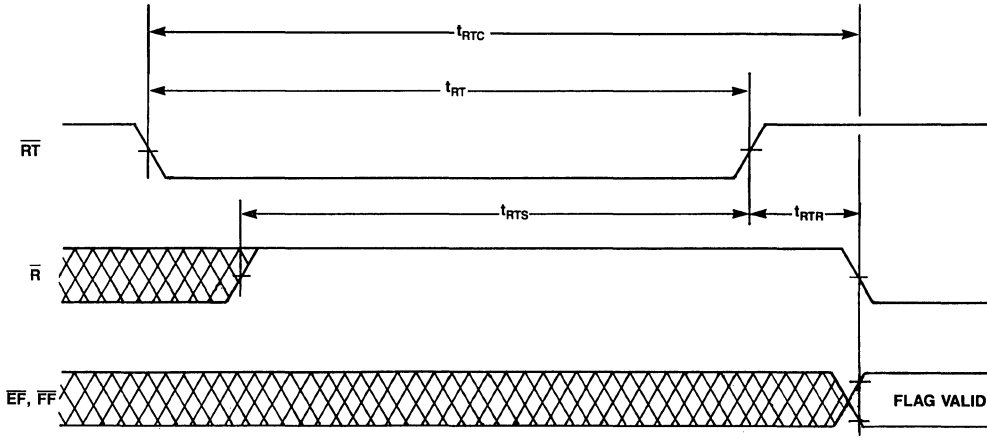
		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	45		60		80		100		130		180		ns	

RETRANSMIT

The MK4501 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 6).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 512 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.



NOTE
$\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Setup Time	45		60		80		100		130		180		ns	

SINGLE DEVICE CONFIGURATION

A single MK4501 may be used when application requirements are for 512 words or less. The MK4501 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK4501s. Any word width can be attained by adding additional MK4501s.

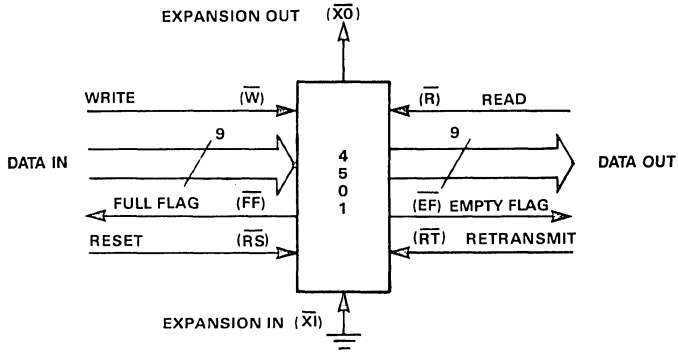
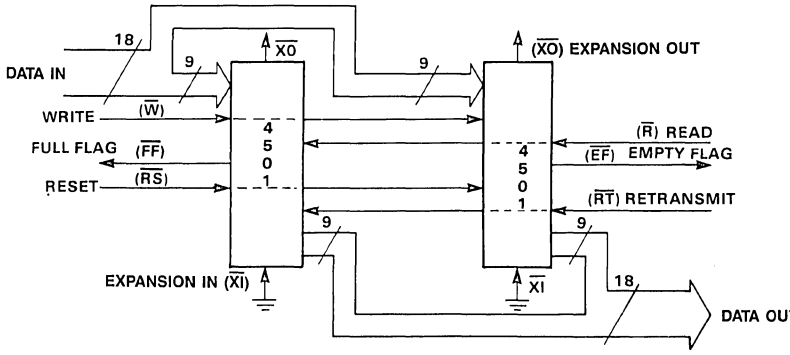


Figure 7. A Single 512 x 9 FIFO Configuration



NOTE
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

Figure 8. A 512 x 18 FIFO Configuration (Width Expansion)

DEPTH EXPANSION (DAISY CHAIN)

The MK4501 can easily be adapted to applications when the requirements are for greater than 512 words. Figure 9 demonstrates Depth Expansion using three MK4501s. Any depth can be attained by adding additional MK4501s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4501 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.

2. All other devices must have $\overline{FL}$ in the high state.

3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.

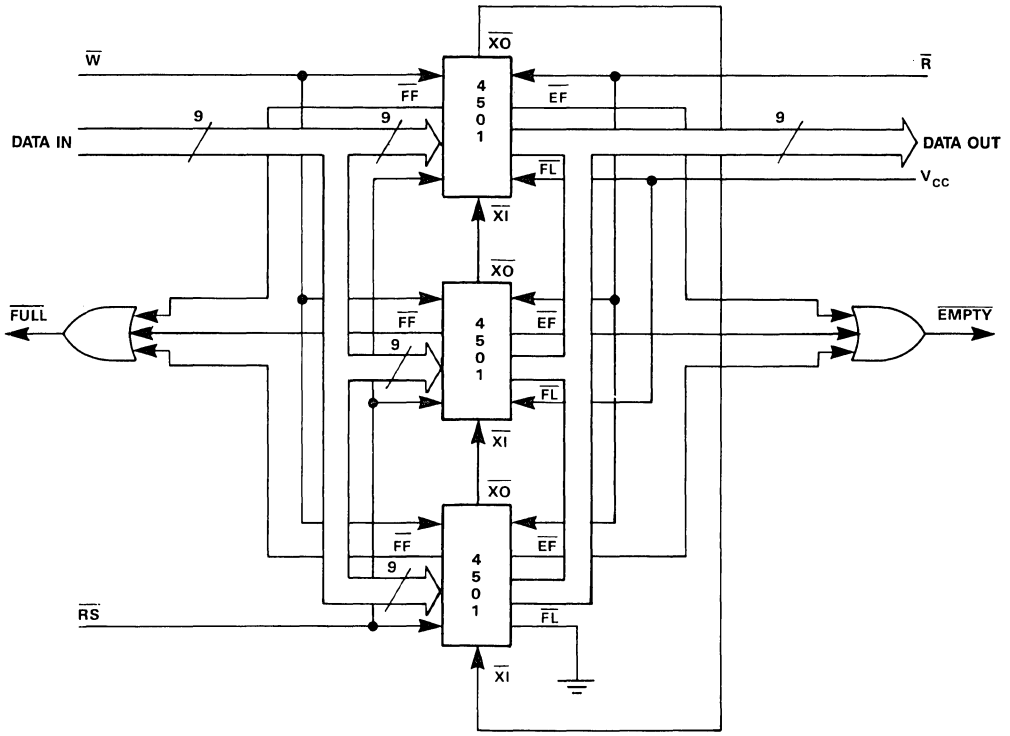


Figure 9. A 1536 x 9 FIFO Configuration (Depth Expansion)

EXPANSION TIMING

Figures 10 and 11 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

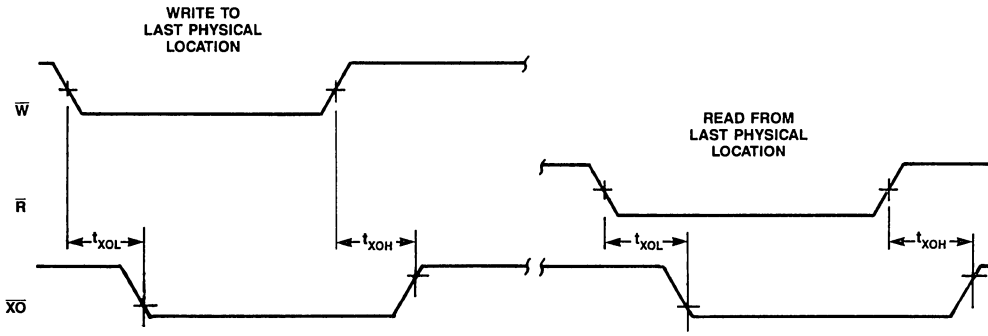


Figure 10. Expansion Out Timing

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4501 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4501 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

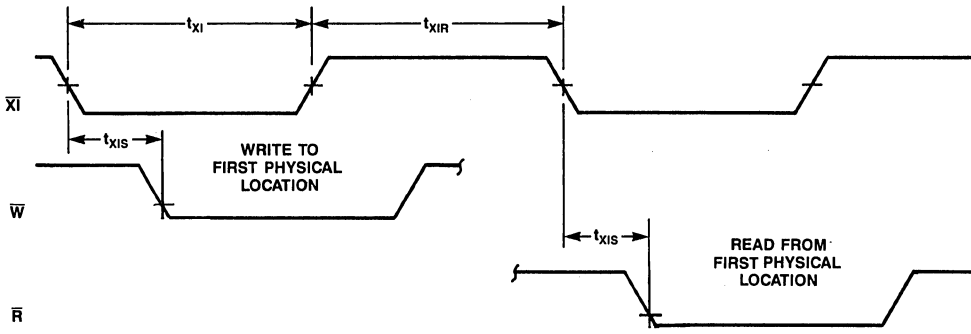


Figure 11. Expansion In Timing

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

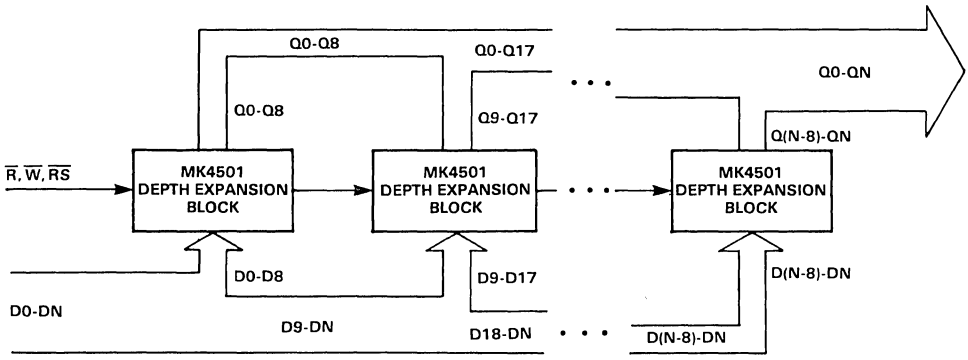
		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XI}	Expansion In Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	25		30		45		50		60		85		ns	

COMPOUND EXPANSION

The two expansion techiques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 12).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4501s, as shown in Figure 13. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.



NOTES
1. For depth expansion block see DEPTH EXPANSION Section and Figure 9.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

Figure 12. Compound FIFO Expansion

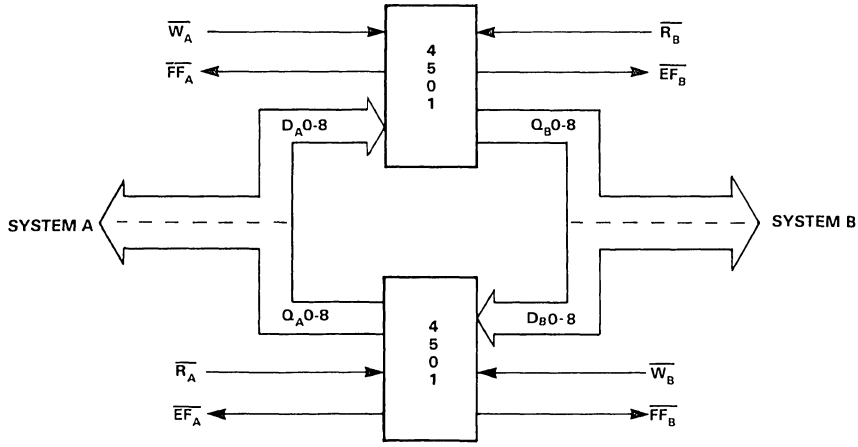


Figure 13. Bidirectional FIFO Application

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND . . . . . -0.5 V to + 7.0 V
Operating Temperature T_A (Ambient) . . . . . 0°C to + 70°C
Storage Temperature . . . . . -55°C to + 125°C
Total Device Power Dissipation . . . . . 1 Watt
Output Current per Pin . . . . . 20 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.0		V_{CC} + 1	V	3
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS

(0°C≤T_A≤+70°C) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current (Any Input)	-1	1	μA	5
I_{OL}	Output Leakage Current	-10	10	μA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	7
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})		8	mA	7
I_{CC3}	Power Down Current (All Inputs ≥ V_{CC} -0.2 V)		500	μA	7

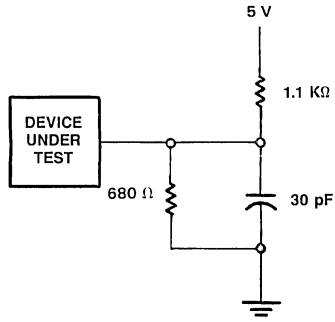
AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on Input Pins		7 pF	
C_Q	Capacitance on Output Pins		12 pF	8

NOTES

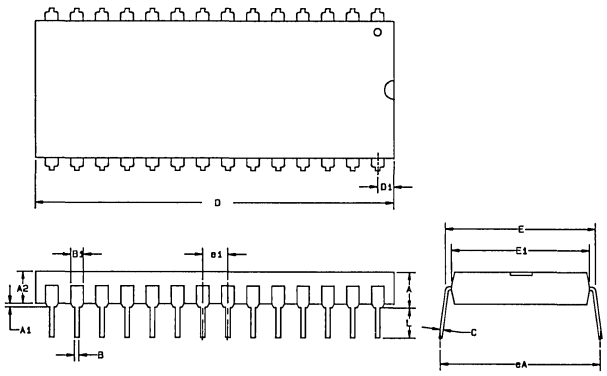
1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to ground.
4. −1.5 volt undershoots are allowed for 10 ns once per cycle.
5. Measured with $0.4 \le V_{IN} \le V_{CC}$.
6. $\overline{R} \ge V_{IH}$, $0.4 \ge V_{OUT} \le V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.



AC TEST CONDITIONS:

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Level	0.8 V and 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10%

Figure 14. Output Load



DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.140	.160	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.440	1.470	1
D1	.065	.085	
E	.600	.625	
E1	.530	.560	
e1	.090	.110	
eA	.600	.700	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

Figure 15. MK4501 Plastic (N type) Dual-In-Line, 28 pins

ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK4501N-65	65 ns	80 ns	12.5 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-80	80 ns	100 ns	10.0 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-10	100 ns	120 ns	8.3 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-12	120 ns	140 ns	7.1 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-15	150 ns	175 ns	5.7 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-20	200 ns	235 ns	4.2 MHz	28 Pin Plastic DIP	0° to 70°C

MK4503(N/K)-50/65/80/10/12/15/20

2048 x 9 CMOS BiPORT™ FIFO

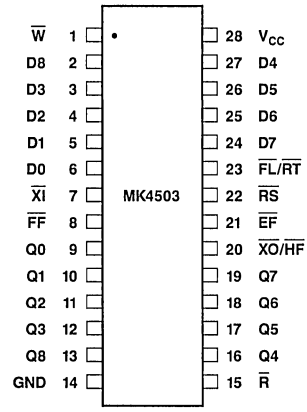
PRELIMINARY

MEMORY COMPONENTS

FEATURES

- ☐ First-In, First-Out Memory Based Architecture
- ☐ Flexible 2048 x 9 organization
- ☐ Low Power HCMOS technology
- ☐ Asynchronous and simultaneous read/write
- ☐ Bidirectional applications
- ☐ Fully expandable by word width and depth
- ☐ Empty and full warning flags
- ☐ Retransmit capability
- ☐ High performance
- ☐ Half full flag in single device mode

Part No.	Access Time	R/W Cycle Time
MK4503-50	50 ns	65 ns
MK4503-65	65 ns	80 ns
MK4503-80	80 ns	100 ns
MK4503-10	100 ns	120 ns
MK4503-12	120 ns	140 ns
MK4503-15	150 ns	175 ns
MK4503-20	200 ns	235 ns



28 Pin Plastic DIP

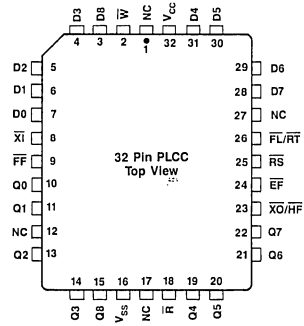


Figure 1. Pin Connections

DESCRIPTION

The MK4503 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, half full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4503 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The

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PIN NAMES

W̄	= Write	X̄I	= Expansion In
R̄	= Read	XO/HF	= Expansion Out Half Full Flag
RS̄	= Reset	F̄F	= Full Flag
FL/RT	= First Load/ Retransmit	EF	= Empty Flag
D	= Data In	VCC	= 5 Volts
Q	= Data Out	GND	= Ground
		NC	= No Connection

full, half full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4503 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the MK4503 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Twin internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

The address pointers automatically loop back to address zero after reaching address 2047. The empty/half full and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4503 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4503 allows connecting the read, write, data in, and data out lines of the MK4503s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

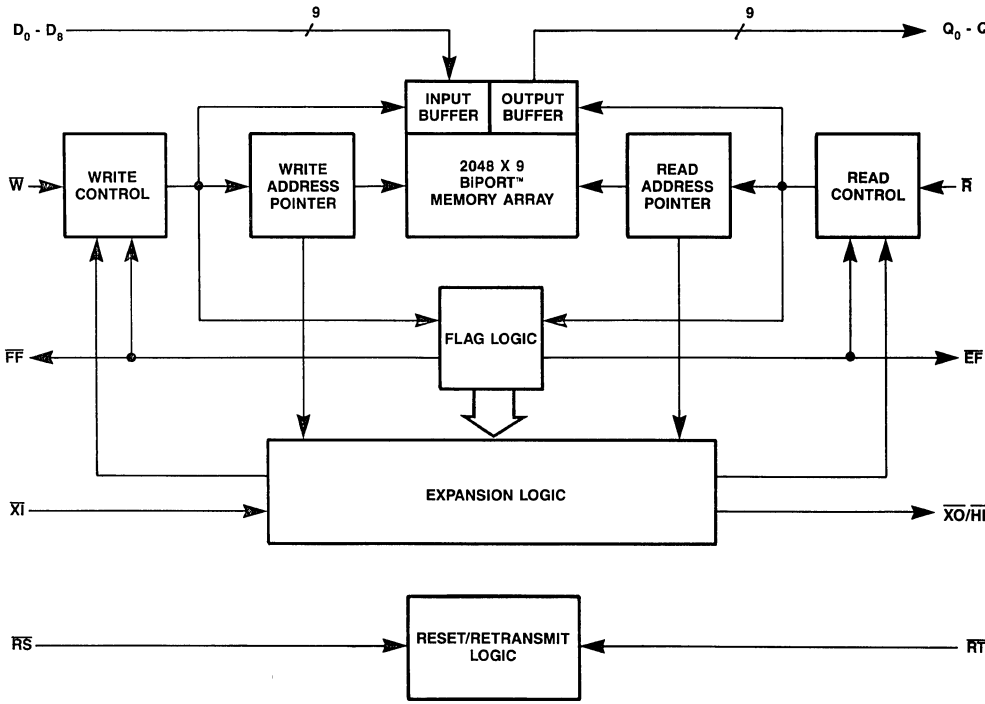


Figure 2. MK4503 Block Diagram

WRITE MODE

The MK4503 initiates a Write Cycle (see Figure 3) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4503 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

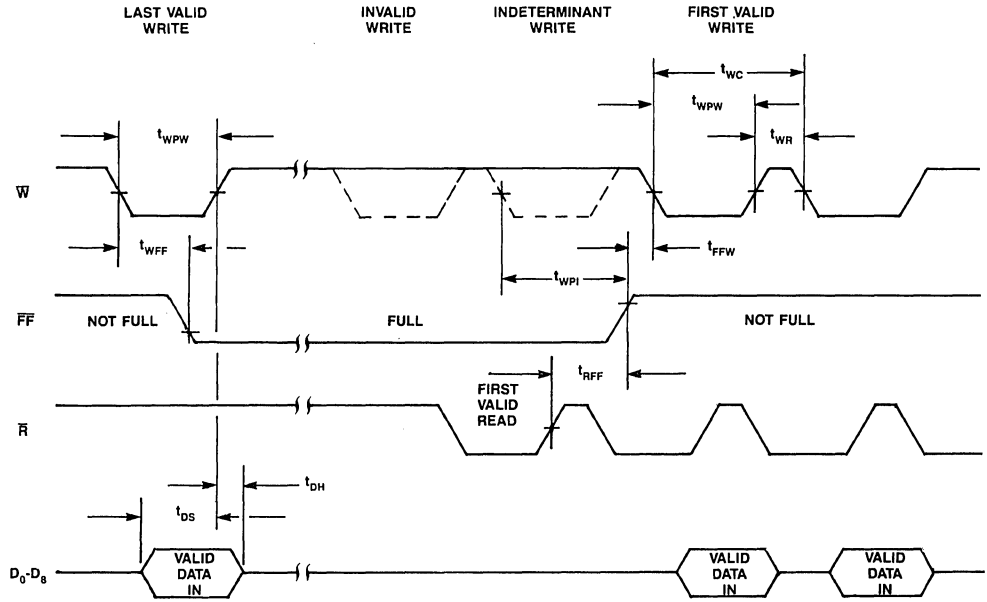


Figure 3. Write and Full Flag Timing

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	65		80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	50		65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	30		30		40		40		40		50		65		ns	
t_{DH}	Data Hold Time	5		10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		45		60		70		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10			10		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		45		60		70		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant	35			35		35		35		35		35		35	ns	2

READ MODE

The MK4503 initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4503 provides a fast access to data from 9 of 18432 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	65		80		100		120		140		175		235		ns	
t_A	Access Time		50		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		45		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		45		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35		35	ns	2

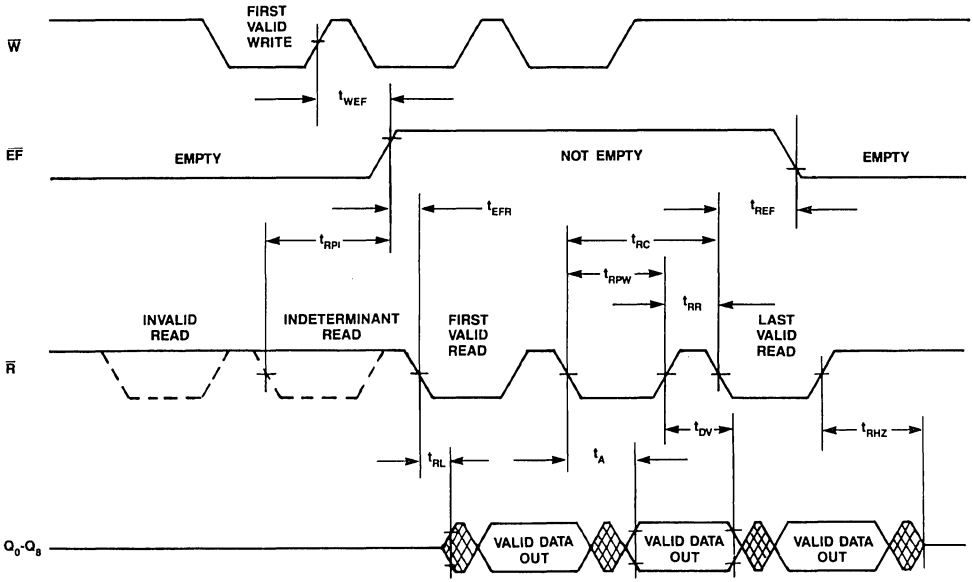
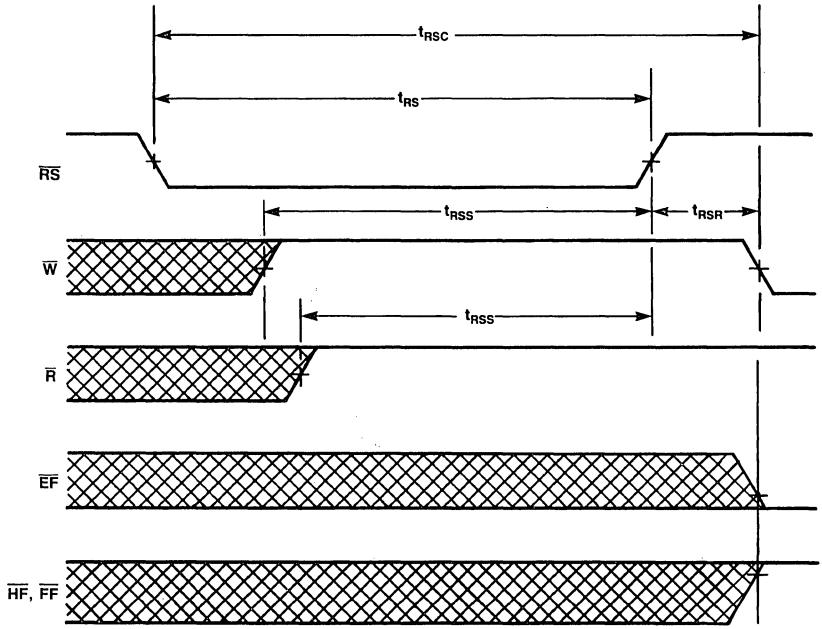


Figure 4. Read and Empty Flag Timing

RESET

The MK4503 is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.



NOTE
$\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Figure 5. Reset

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

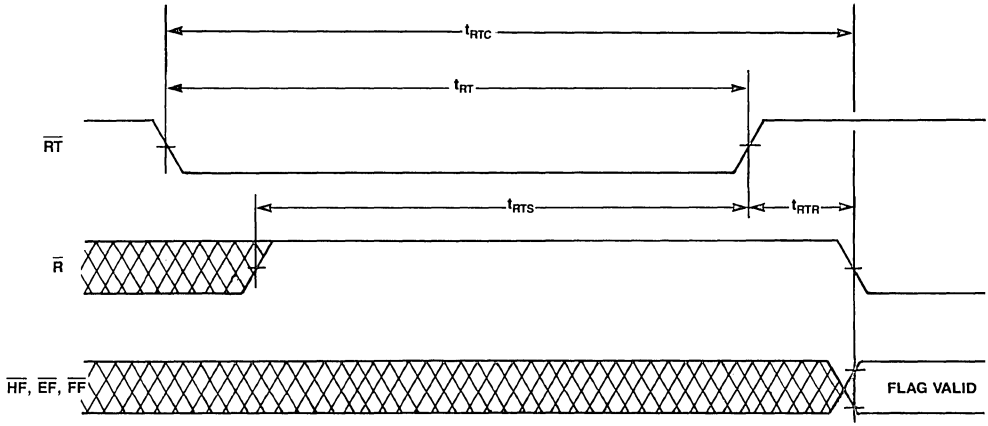
		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RSC}	Reset Cycle Time	65		80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	30		45		60		80		100		130		180		ns	

RETRANSMIT

The MK4503 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 6).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.



NOTE
$\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RTC}	Retransmit Cycle Time	65		80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Setup Time	30		45		60		80		100		130		180		ns	

SINGLE DEVICE CONFIGURATION

A single MK4503 may be used when application requirements are for 2048 words or less. The MK4503 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK4503s. Any word width can be attained by adding additional MK4503s. The half full flag ($\overline{HF}$) operates the same as in the single device configuration.

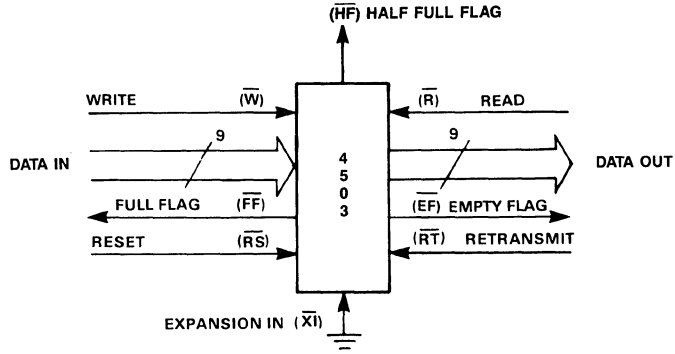
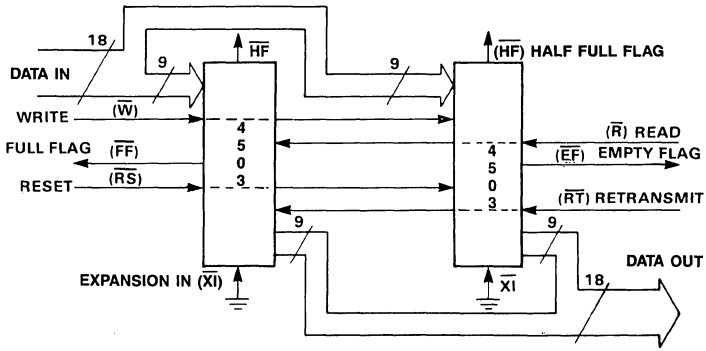


Figure 7. A Single 2048 x 9 FIFO Configuration



NOTE
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

Figure 8. A 2048 x 18 FIFO Configuration (Width Expansion)

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation. See Figure 9.

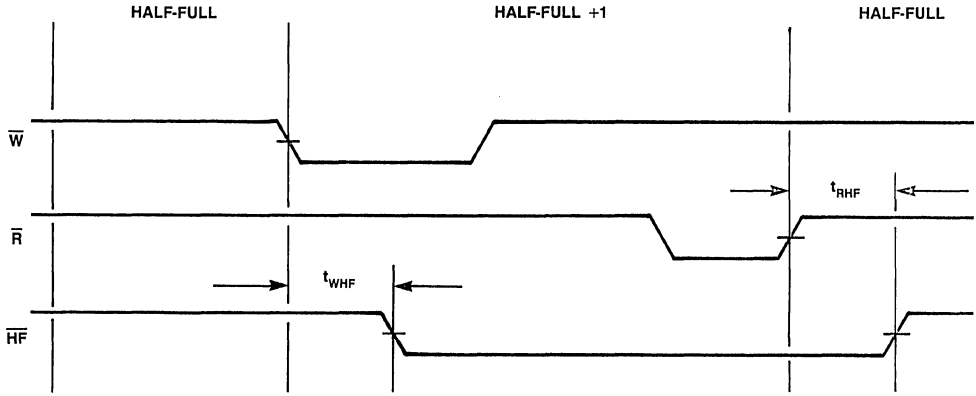


Figure 9. Half Full Flag Timing

AC ELECTRICAL CHARACTERISTICS ·

(0°C≤T_A≤+70°C) (V_{CC} = +5 Volts ±10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WHF}	Write Low to Half Full Flag Low		65		80		100		120		140		175		235	ns	
t_{RHF}	Read High to Half Full Flag High		65		80		100		120		140		175		235	ns	

DEPTH EXPANSION (DAISY CHAIN)

The MK4503 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 10 demonstrates Depth Expansion using three MK4503s. Any depth can be attained by adding additional MK4503s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4503 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In (XI) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

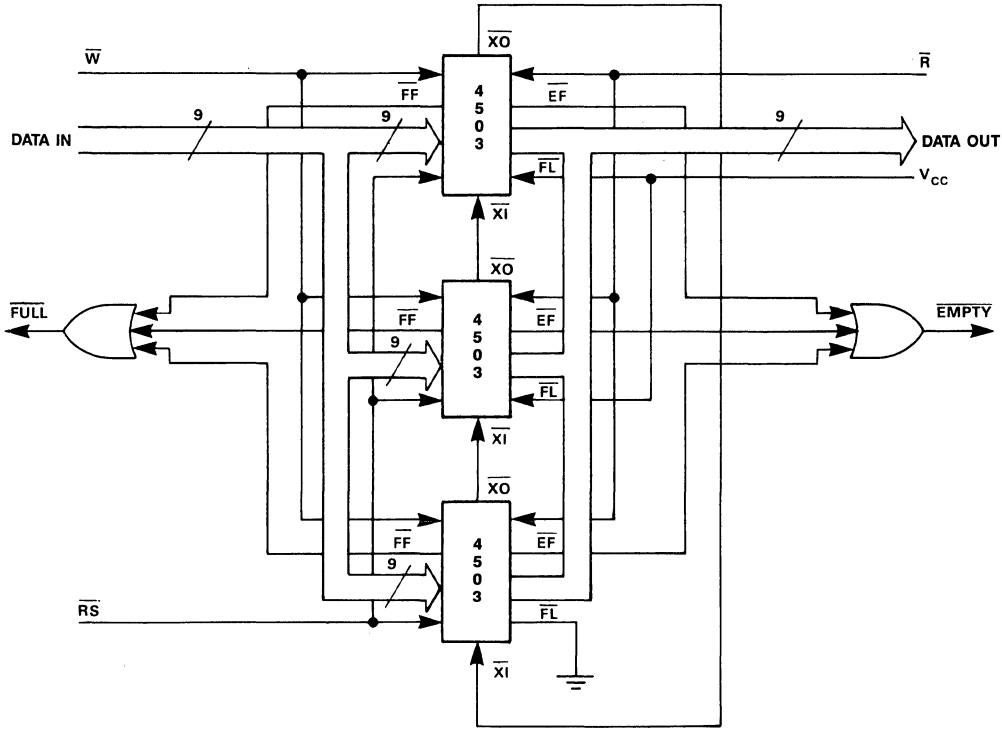


Figure 10. A 6K x 9 FIFO Configuration (Depth Expansion)

EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

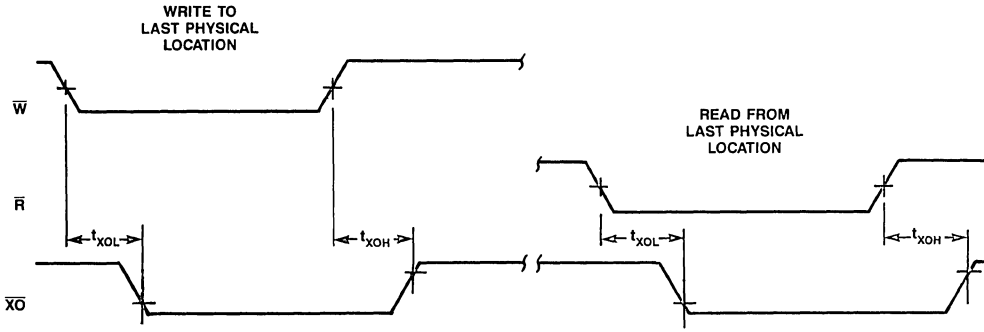


Figure 11. Expansion Out Timing

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XOL}	Expansion Out Low		40		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		45		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4503 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4503 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

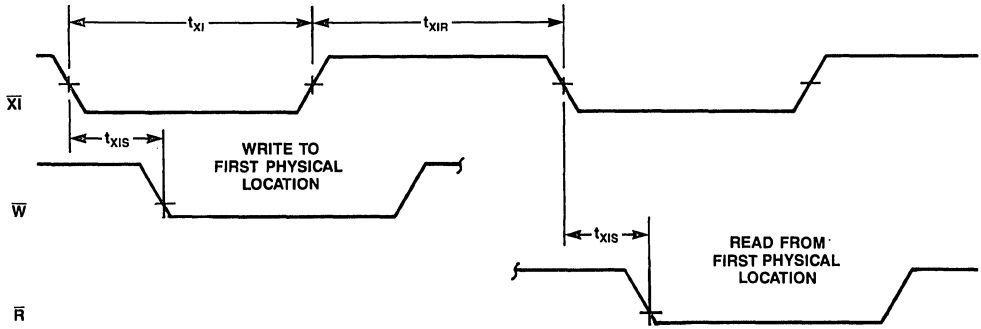


Figure 12. Expansion In Timing

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

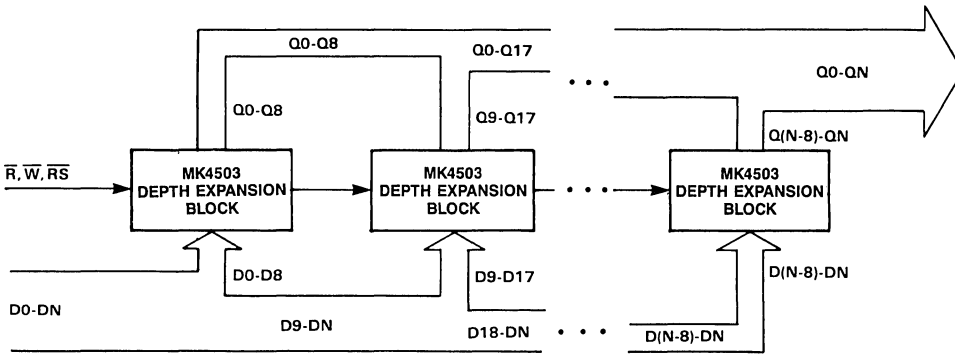
		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XI}	Expansion In Pulse Width	45		60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	20		25		30		45		50		60		85		ns	

COMPOUND EXPANSION

The two expansion techiques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 13).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4501s, as shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.



NOTES
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

Figure 13. Compound FIFO Expansion

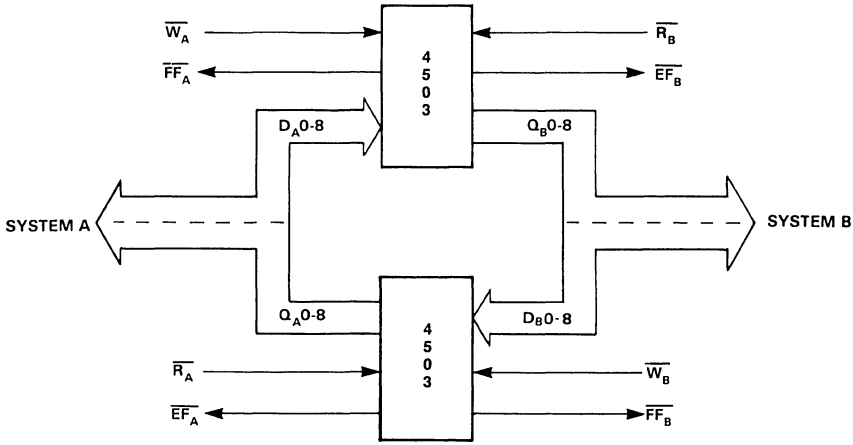


Figure 14. Bidirectional FIFO Application

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND . . . . . -0.5 V to + 7.0 V
Operating Temperature T_A (Ambient) . . . . . 0°C to + 70°C
Storage Temperature . . . . . -55°C to + 125°C
Total Device Power Dissipation . . . . . 1 Watt
Output Current per Pin . . . . . 20 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.2		V_{CC} + .3	V	3, 9
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	3, 4, 9

DC ELECTRICAL CHARACTERISTICS

(0°C≤T_A≤+70°C) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current (Any Input)	-1	1	μA	5
I_{OL}	Output Leakage Current	-10	10	μA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	7
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})		12	mA	7
I_{CC3}	Power Down Current (All Inputs ≥ V_{CC} -0.2 V)		4	mA	7

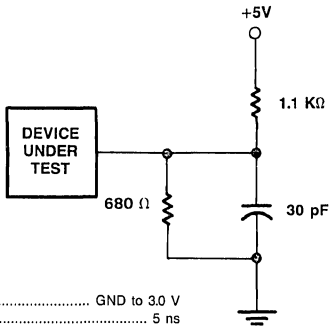
AC ELECTRICAL CHARACTERISTICS

(0°C≤T_A≤±70°C) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on Input Pins		7 pF	
C_O	Capacitance on Output Pins		12 pF	8

NOTES

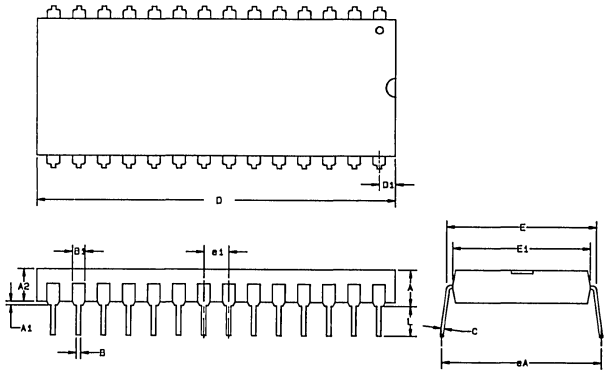
1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to ground.
4. −1.5 volt undershoots are allowed for 10 ns once per cycle.
5. Measured with 0.0≤V_{IN}≤V_{CC}.
6. $\overline{R}$≥V_{IH}, 0.0≤V_{OUT}≤V_{CC}.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. Input levels tested at 500 ns cycle time.



AC TEST CONDITIONS:

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Level	0.8 V and 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10%

Figure 15. Output Load

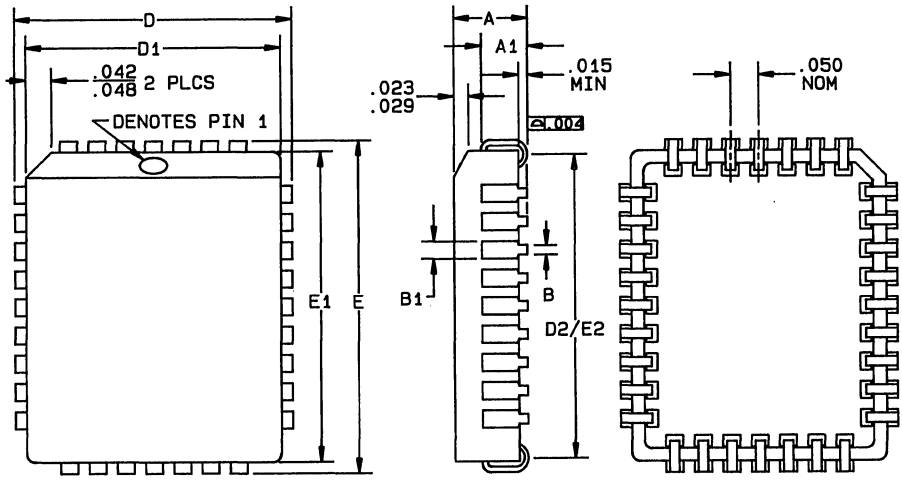


DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.140	.160	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.440	1.470	1
D1	.065	.085	
E	.600	.625	
E1	.530	.560	
e1	.090	.110	
eA	.600	.700	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

Figure 16. MK4503 Plastic (N type) Dual-In-Line, 28 pins



DIM	INCHES	
	MIN	MAX
A	.120	.140
A1	.078	.095
B	.013	.021
B1	.026	.032
D	.485	.495
D1	.447	.453
D2	.390	.430
E	.585	.595
E1	.547	.553
E2	.490	.530

Figure 17. MK4503 Plastic Leaded Chip Carrier, 32 Pin (K Type)

MK4505M/4505S(N,K)-25,33,50

VERY HIGH SPEED CMOS CLOCKED FIFO

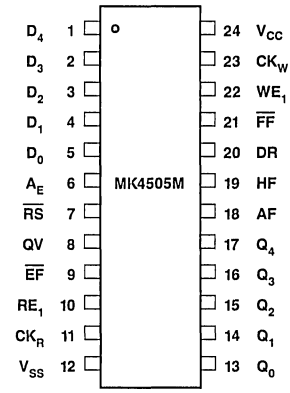
PRELIMINARY — MEMORY COMPONENTS

FEATURES

- ☐ 1024 x 5 Organization
- ☐ Very high performance

Part No.	Cycle Time	Cycle Frequency	Access Time
4505-25	25 ns	40 MHz	15 ns
4505-33	33 ns	30 MHz	20 ns
4505-50	50 ns	20 MHz	25 ns

- ☐ Rising edge triggered clock inputs
- ☐ Supports free-running 40% to 60% Duty Cycle Clock Inputs
- ☐ Separate Read and Write Enable Inputs
- ☐ Fully asynchronous and simultaneous Read/Write operation
- ☐ Cascadable to any depth with no additional logic
- ☐ Width Expandable to more than 40 bits with no additional logic
- ☐ Half Full Status Flag
- ☐ Full and Empty Flags, Almost Full, Almost Empty, Input Ready, Output Valid Status Flags (4505M)
- ☐ TTL and CMOS Compatible
- ☐ 3 State Outputs



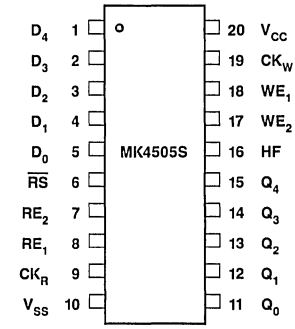


Figure 1. Pin Configuration, 300 mil DIP

PIN NAMES

D_0 - D_4	- Data Input
Q_0 - Q_4	- Data Output
CK_W, CK_R	- Write and Read Clock
WE_1	- Write Enable Input 1
RE_1	- Read Enable Input 1
$\overline{RS}$	- Reset (Active Low)
HF	- Half Full Flag
V_{CC}, GND	- +5 Volt, Ground

(4505M Only)

$\overline{FF}$, $\overline{EF}$	- Full and Empty Flag (Active Low)
AF, AE	- Almost Full, Almost Empty Flag
DR, QV	- Input Ready, Output Valid

(4505S Only)

WE_2	- Write Enable Input 2
RE_2	- Read Enable Input 2 (3 State Control)

DESCRIPTION

The MK4505 is a Very High Speed 1K x 5 Clocked FIFO memory. It achieves its high performance through the use of a pipelined architecture, a 1.2μ full CMOS, single poly, double level metal process, and a memory array constructed using Thomson-Mostek's 8 transistor BiPORT™ memory cell.

The device is designed for use in applications where data is moving through a system on a square wave clock; applications such as digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, Radar return sampling or data tracing.

The device is available in two versions; a Master, the MK4505M, and a Slave, the MK4505S. The Master provides all of the control signals necessary for reliable, full speed, fully asynchronous width expansion and/or depth expansion. The Master also provides a full compliment of status flags, including Output Valid, Empty, Almost Empty, Half Full, Almost Full, Full, and Input Ready. The Master cannot be written while Full or read while Empty. The Slave, in contrast, can be forced to write and/or read continuously regardless of device status; a feature useful in triggered data acquisitions, or for retransmit (repeat reading) applications.

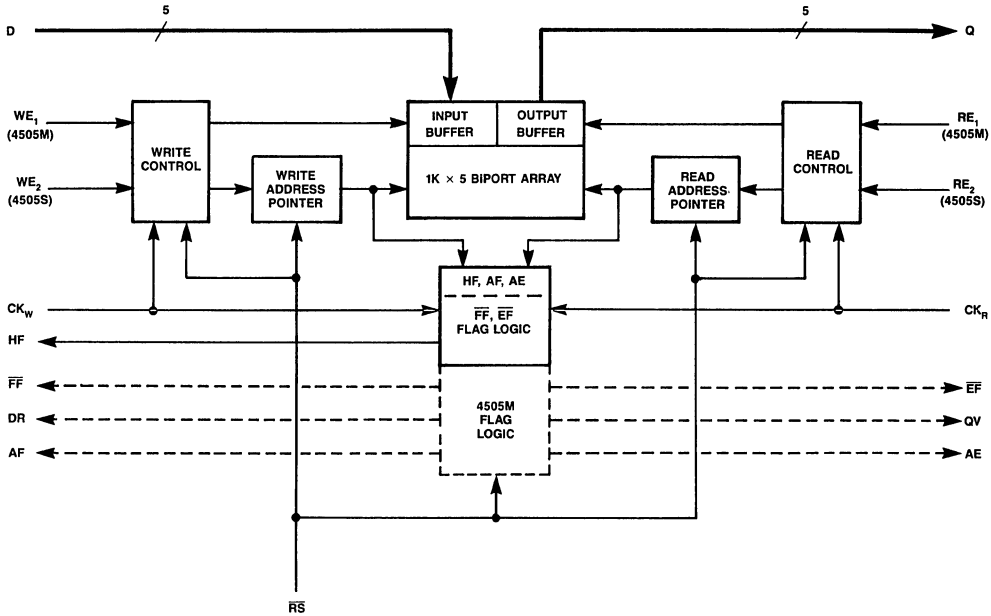


Figure 2. Block Diagram MK4505M/4505S

4505M WRITE TRUTH TABLE

CK_W	PRESENT STATE				NEXT OPERATION	NEXT STATE		
	$\overline{RS}$	WE_1	$\overline{FF}$	DR		$\overline{FF}$	DR	D
X	0	X	X	X	Reset	1	1	Don't Care
↑	1	0	1	1	No-Op	1	1	Don't Care
↑	1	X	0	0	No-Op	?	?	Don't Care
↑	1	1	1	1	Write	?	?	Data In

4505M READ TRUTH TABLE

CK_R	PRESENT STATE				NEXT OPERATION	NEXT STATE		
	$\overline{RS}$	RE_1	$\overline{EF}$	QV		$\overline{EF}$	QV	Q
X	0	X	X	X	Reset	0	0	High Z
↑	1	X	0	X	No-Op	?	0	High Z
↑	1	0	1	0	Hold	?	1	Previous Q
↑	1	1	1	X	Read	?	1	Data Out

4505S WRITE TRUTH TABLE

CK_W	PRESENT STATE			NEXT OPERATION	NEXT STATE
	$\overline{RS}$	WE_1	WE_2		D
X	0	X	X	Reset	Don't Care
↑	1	0	X	No-Op	Don't Care
↑	1	X	0	No-Op	Don't Care
↑	1	1	1	Write	Data In

4505S READ TRUTH TABLE

CK_R	PRESENT STATE			NEXT OPERATION	NEXT STATE
	$\overline{RS}$	RE_1	RE_2		Q
X	0	X	X	Reset	High Z
↑	1	X	0	No-Op	High Z
↑	1	0	1	Hold	Previous Data Out
↑	1	1	1	Read	Data Out

X = Don't care

? = The next state will be active but the logic level is unknown.

WRITE OPERATIONS

The device will perform a Write on the next rising edge of the Write Clock (CK_W) whenever (see figure 3):

- (4505S) WE_1 and WE_2 are high at the rising edge of the clock.
- (4505M) WE_1 and $\overline{FF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Full Flag ($\overline{FF}$) on the rising edge of CK_W, the appearance of an active Full Flag at valid flag access time, t_A, assures the user that the next rising edge of the clock will be ignored.

READ AND HOLD OPERATIONS

The device will perform a Read on the next rising edge of the Read Clock (CK_R) whenever (see figure 4):

- (4505S) RE_1 and RE_2 are high at the rising edge of the clock.
- (4505M) RE_1 and $\overline{EF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Empty Flag ($\overline{EF}$) on the rising edge of CK_R, the appearance of an active Empty Flag at valid flag access time, t_A, assures the user that the next rising edge of the clock will be ignored.

The device will perform a Hold Cycle (hold over previous data) if RE_1 is low at the rising edge of the clock (CK_R). If $\overline{EF}$ (4505M) or RE_2 (4505S) is low at the rising edge of the clock, then the outputs will go to High-Z.

RESET

$\overline{RS}$ is an asynchronous master reset input. A Reset is required after power-up, before first write. Reset commences on the falling edge of $\overline{RS}$ irrespective of the state of any other input or output. While deactivating Write and/or Read Enable inputs is not required for performance of a Reset, failure to do so requires the user's observance of Reset Set Up Time (t_{RSS}) to assure First Write (and/or First Read of a stand alone 4505S) will occur at the first rising edge of the clock after $\overline{RS}$ is taken high (Figure 6).

After Reset, if no valid Read operations have been performed since Reset, the "previous data" that will be output when executing the first Hold cycle will be all zeroes (see Figure 7.)

AC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70 C, V_{CC} = 5.0 ± 10%)

SYM	PARAMETER	4505-25		4505-33		4505-50		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{CK}	Clock Cycle Time	25		33		50		ns	1
t_{CKH}	Clock High Time	10		13		20		ns	1
t_{CKL}	Clock Low Time	10		13		20		ns	1
t_S	Set Up Time	10		13		16		ns	1
t_H	Hold Time	0		0		0		ns	
t_A	Output Access Time		15		20		25	ns	1,2
t_{OH}	Output Hold Time	5		5		5		ns	1,2
t_{QZ}	Clock to Outputs High-Z		15		20		25	ns	1,3
t_{QL}	Clock to Outputs Low-Z	5		5		5		ns	1,3
t_{RSS}	Reset Set Up Time	12		16		25		ns	1,4
t_{RS}	Reset Pulse Width	25		33		50		ns	
t_{FRL}	First Read Latency	50		66		100		ns	1,5
t_{FFL}	First Flag Cycle Latency	25		33		50		ns	1,6
t_{FT}	Fall-Through Delay	•71		94		135		ns	

NOTES

1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/40pf Output Load (Figure 12A).
3. Measured w/5pf Output Load (Figure 12B).
4. Need not be met unless device is Read and/or Write Enabled.
5. Minimum first Write to first Read delay required to assure valid first Read.
6. Minimum first Write to first Read Clock delay required to assure clearing the Empty Flag.

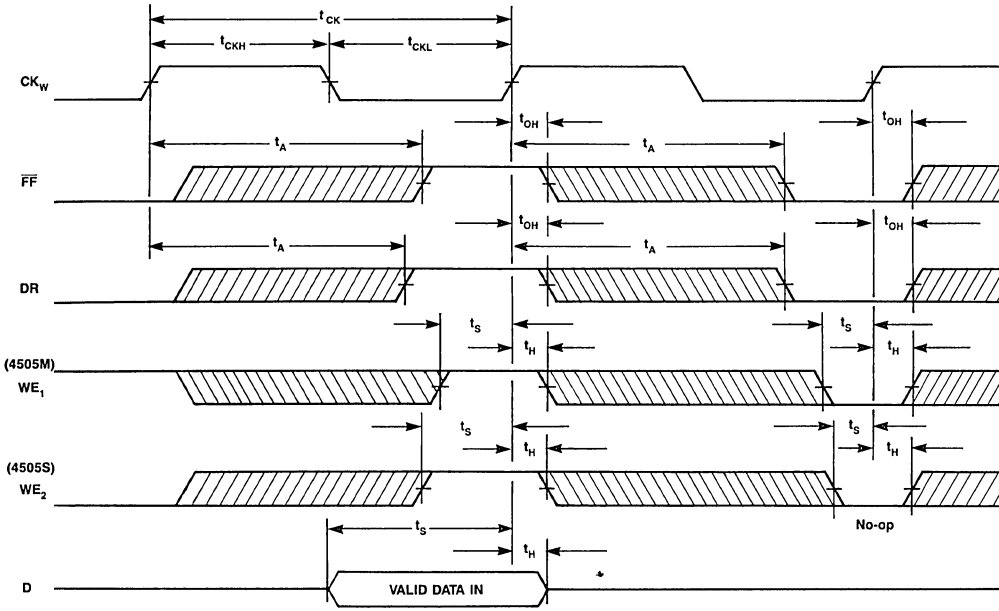


Figure 3. Write Cycle Timing

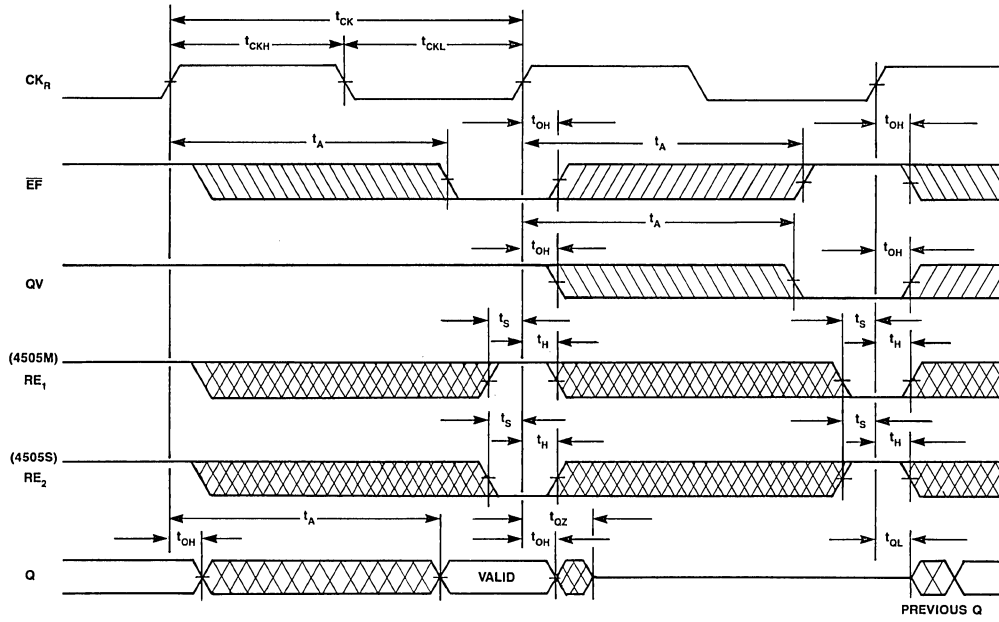


Figure 4. Read Cycle Timing

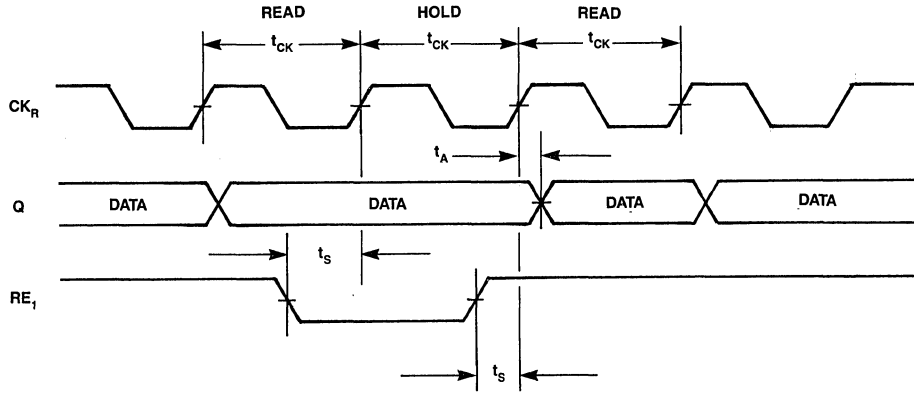
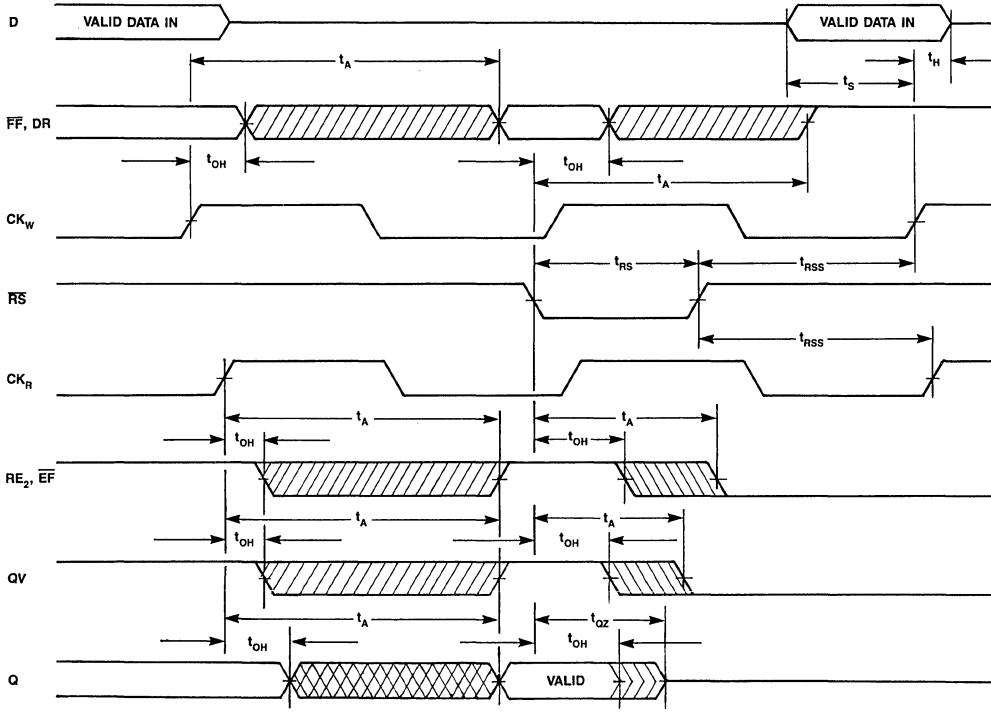


Figure 5. Hold Cycle Timing



NOTE: t_{RSS} NEED NOT BE MET UNLESS DEVICE IS READ AND/OR WRITE ENABLED

Figure 6. Reset Cycle Timing (4505M/S)

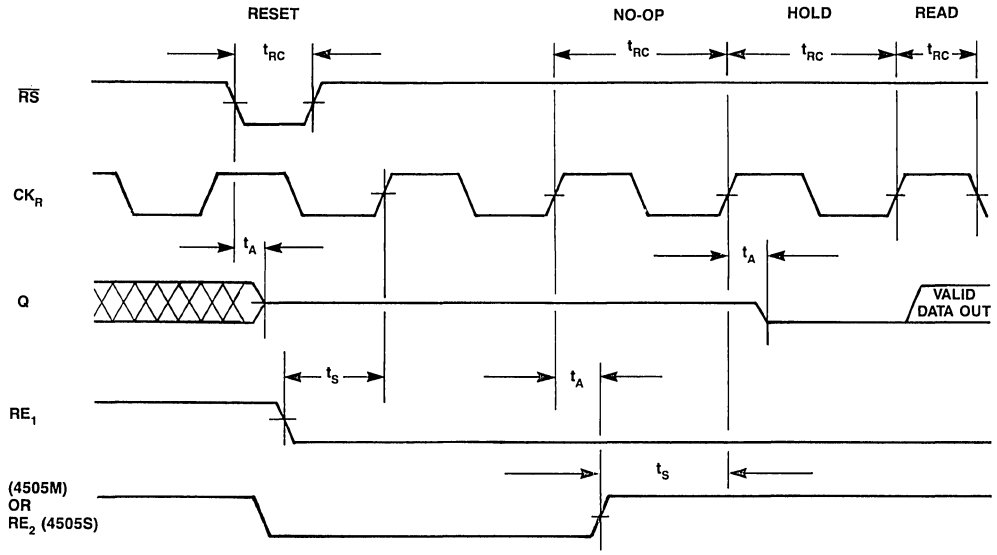


Figure 7. First Hold After Reset

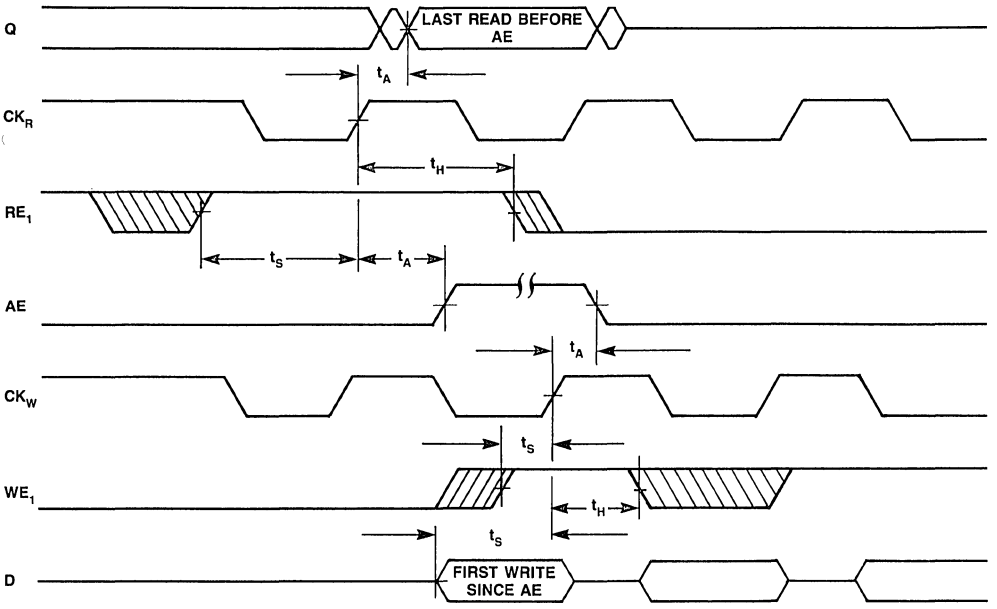


Figure 8. Almost Empty Flag Timing (4505M)

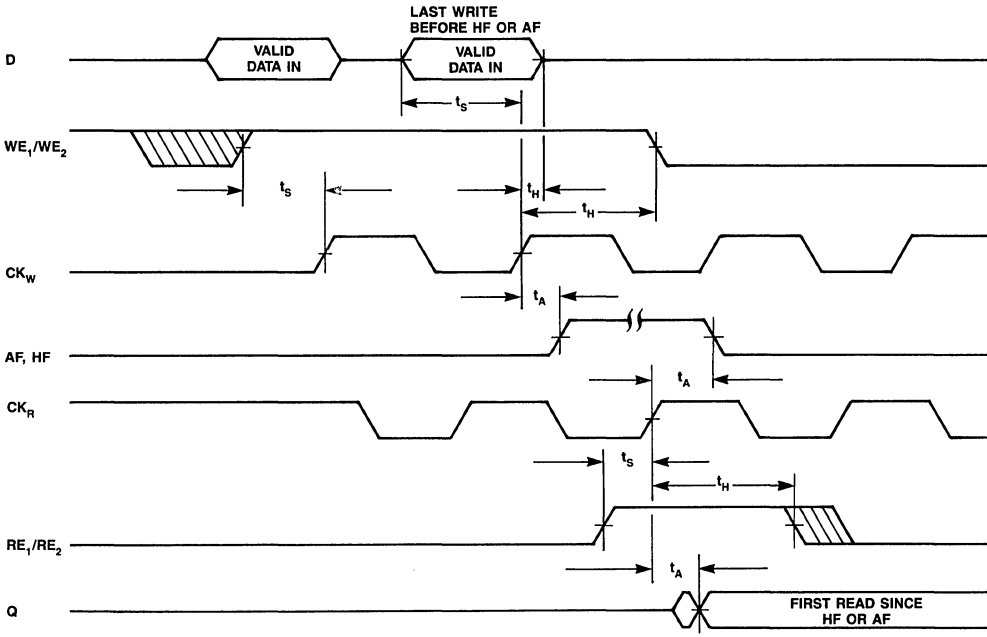


Figure 9. Almost Full, Half Full Flag Timing (4505M/S)

Flag Interpretation Key

FLAG	CURRENT STATE	VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
		MIN	MAX	MIN	MAX
AE	1	1016	1024	0	8
	0	0	1015	9	1024
HF	1	0	512	512	1024
	0	513	1024	0	511
AF	1	0	8	1016	1024
	0	9	1024	0	1015

NOTE
The table describes the number of valid cycles that can be performed, including the next rising edge of the clock.

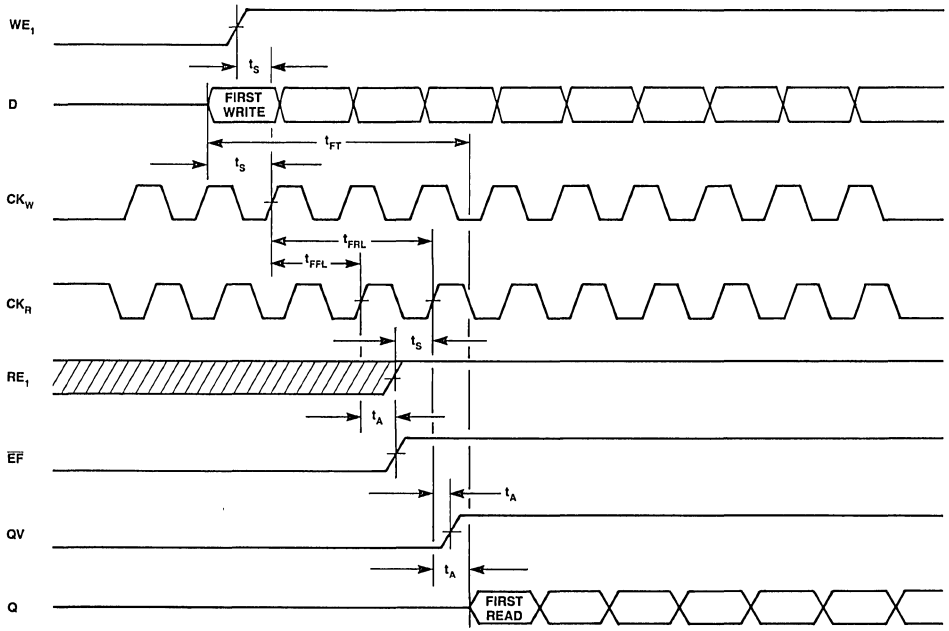


Figure 10. Simultaneous Write/Read Timing (4505M)

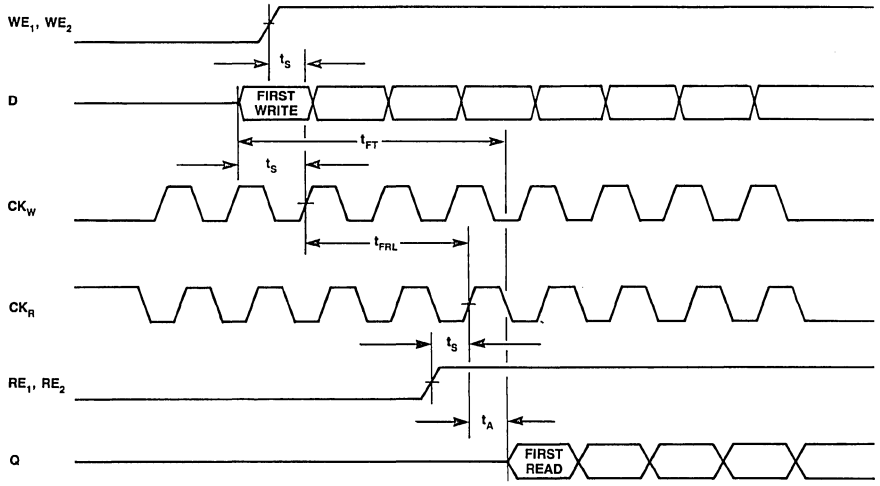


Figure 11. Simultaneous Write/Read Timing (4505S)

WIDTH AND DEPTH EXPANSION

A single Master (MK4505M) is required for each 1k of depth configured. The number of Slaves that can be driven by a single Master is limited only by the effects of adding extra load capacitance (Write and Read Enable Input Capacitance) onto the Input Ready (DR), Output Valid (QV), Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) outputs. However, even 40 bits of width (8 devices) results in only 40pf of loading, which corresponds to the amount of load called out in the AC Test Conditions. Additional loading will slow the flags down, but as long as Enable Set Up time (t_S) is met, slowing the flags has no negative consequences.

WIDTH AND DEPTH EXPANSION EXAMPLES

The width and depth expansion interface timing diagrams (Figures 13 and 14) are in reference to the width and depth expansion schematic in Figure 12 (For simplicity all clocks have the same frequency and transistion rate). Example 1 - First Write Since Empty - Reading the timing diagram from the top left to bottom right, one can determine that Figure 13 illustrates the effects of the first WRITE/READ cycles from an EMPTY array of FIFOs. Both of the $\overline{EF}$ pins are initially low ($\overline{EF_X}$, EF and RE_2). As data is written into Bank A, the expansion clock reads data from Bank A and writes it to Bank B, the interface $\overline{EF}$ ($\overline{EF}$ and RE_2) and the external $\overline{EF}$ ($\overline{EF_X}$) go inactive (logic 1) while data is shifted through the FIFO array from Bank A through Bank B to the external output (Q_X). The $\overline{EF}$ logic goes valid (logic 0) once data is shifted out of its respective bank.

Example 2 - First Read Since Full - Reading the timing diagram from the bottom left to top right, one can determine that Figure 14 illustrates the effects of the first READs from a FULL array of FIFOs. As data is read out of the system (Q_X), it allows Bank B to receive data shifted from Bank A. As Bank B shifts data out via Q_X, allowing Bank A to shift data into Bank B, both banks will show an invalid $\overline{FF}$ status (logic 1) on the internal $\overline{FF}$ ($\overline{FF}$ and WE_2) as well as the external $\overline{FF}$ ($\overline{FF_X}$). When Bank A is no longer considered FULL, Data In from the system (D_X) is now written into Bank A and shifted to Bank B until the FIFO array is again completely Full.

APPLICATION

The MK4505 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK4505 can also interface to 5 volt CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK4505, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each FIFO. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

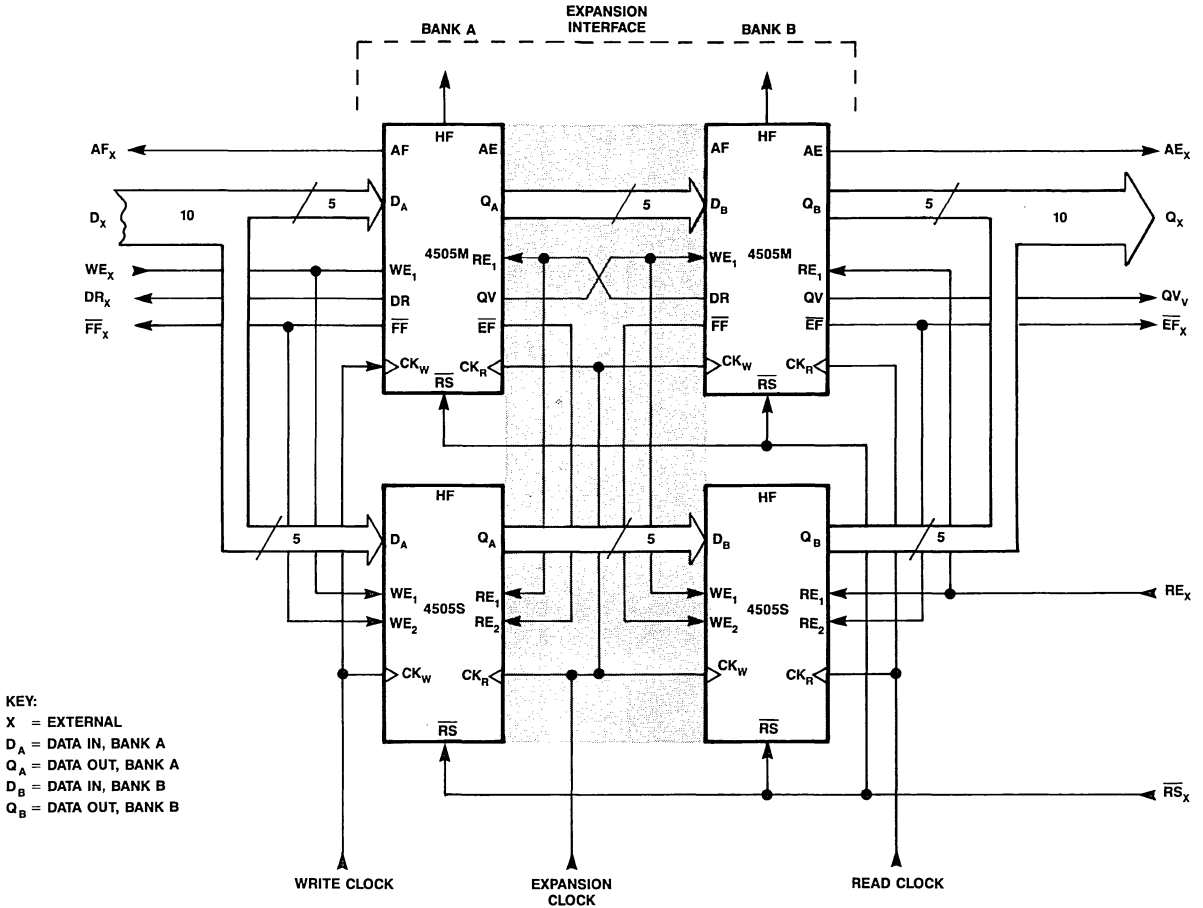
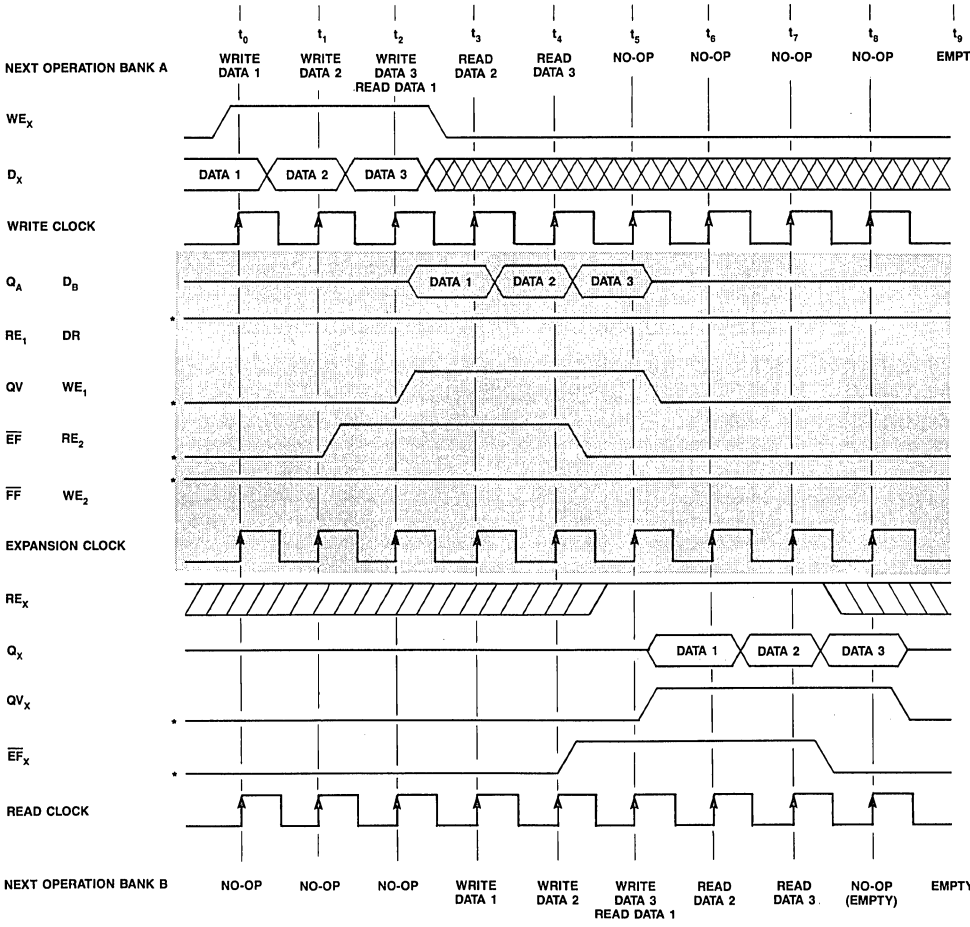
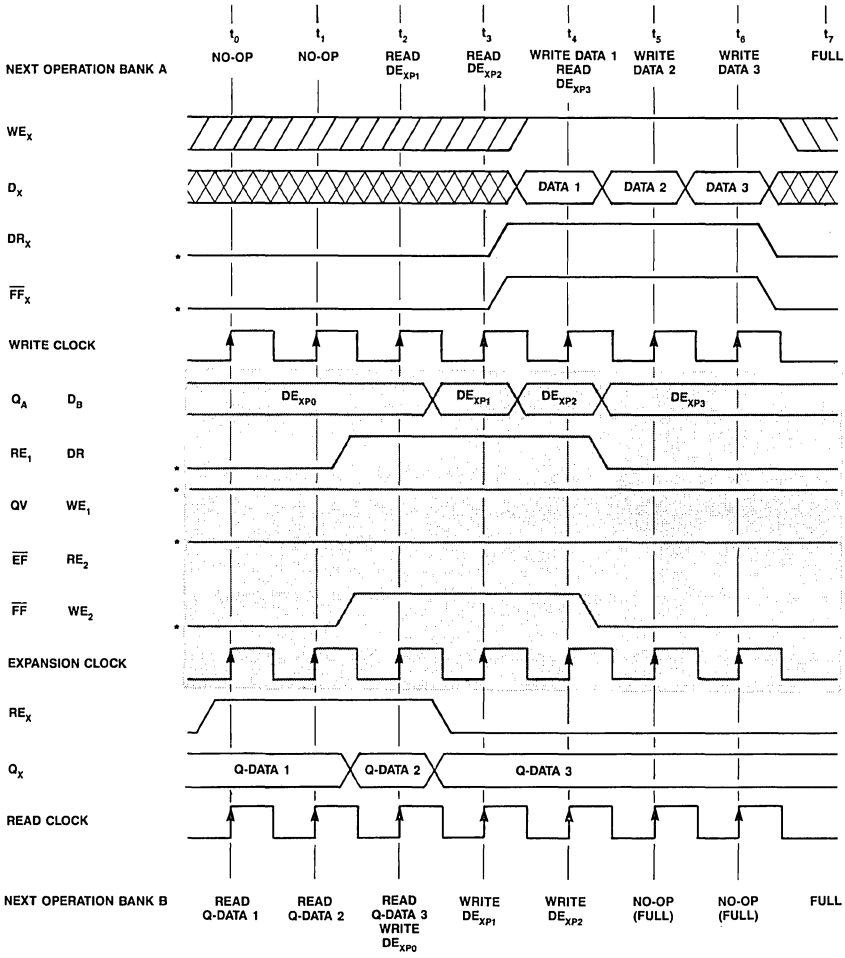


Figure 12. MK4505M/S 2k × 10 Width and Depth Expansion Schematic



* NOTE: EXAMPLE BEGINS WITH BOTH BANKS EMPTY, AS STATUS FLAGS INDICATE

Figure 13. Example 1 - Width and Depth Expansion Interface Timing



* NOTE: EXAMPLE BEGINS WITH BOTH BANKS FULL, AS INDICATED BY STATUS FLAGS

Figure 14. Example 2 - Width and Depth Expansion Interface Timing

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND ..... −1.5V to +7.0V
Ambient Operating Temperature (T_A) ..... 0 to +70 C
Ambient Storage Temperature (Plastic) ..... −55 to +125 C
Total Device Power Dissipation ..... 1 Watt
RMS Output Current per Pin 25mA

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		V_{CC}+1.0	V	1
V_{IL}	Logic 0 Input	−1.0		0.8	V	1,2

NOTES
1. All voltages referenced to GND.
2. V_{IL} may undershoot to −2.0V for 200ns or less once per cycle.

DC ELECTRICAL CHARACTERISTICS

,($0°C \leq T_A \leq 70°C$), V_{CC} = 5.0 ± 10%)

SYM	PARAMETER	LIMITS		UNITS	NOTE
		MIN	MAX		
I_{CC}	Average Power Supply Current		100	mA	1
I_{IL}	Input Leakage Current	−1	+1	μA	2
I_{OL}	Output Leakage Current	−10	+10	μA	3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = −4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4

NOTES
1. Measured with both ports operating at t_{CK} Min, outputs open. V_{CC} max.
2. Measured with V_{IN} = 0.4V to V_{CC}.
3. Measured at Q_0 - Q_4.
   Measured after clocking with RE_2 = 0 (4505S).
   Measured with QV = 0 (4505M).
4. All voltages referenced to GND.

CAPACITANCE

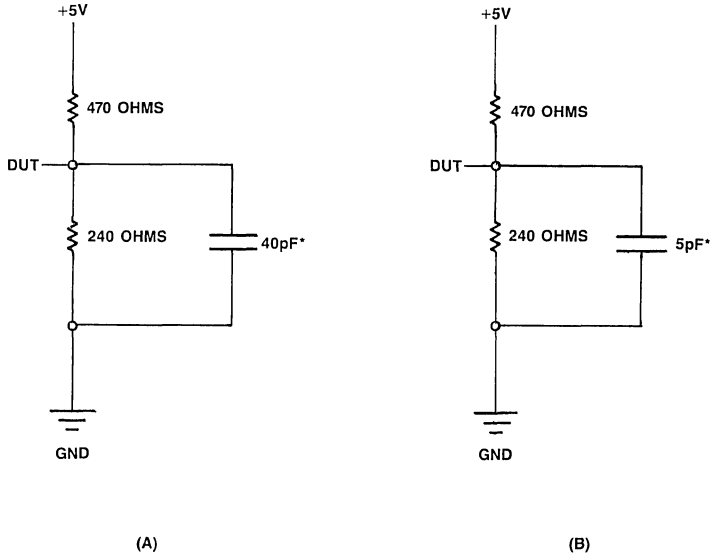
(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	LIMITS		UNITS	NOTE
		TYP	MAX		
C_I	Input Capacitance	4	5	pf	1
CO_1	Output Capacitance	8	10	pf	1,2
CO_2	Output Capacitance	12	15	pf	1,3

NOTES
1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data and flag outputs except $\overline{EF}$ and $\overline{FF}$.
3. Measured at $\overline{EF}$ and $\overline{FF}$.

AC TEST CONDITIONS

Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0 to 70 C
V_{CC}	5.0 Volts ± 10%

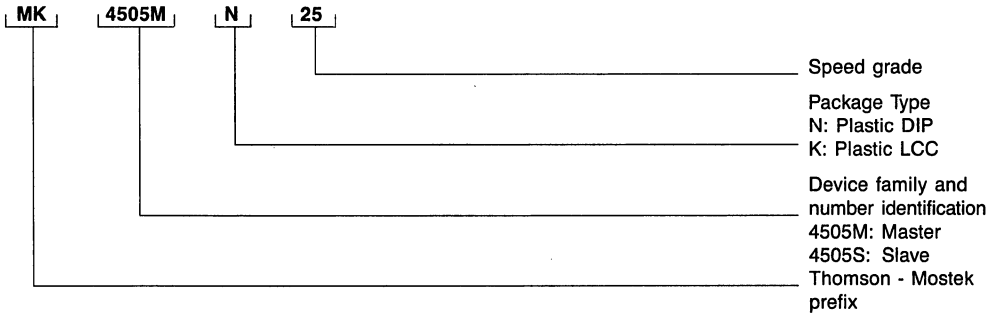


* INCLUDES SCOPE AND TEST JIG.

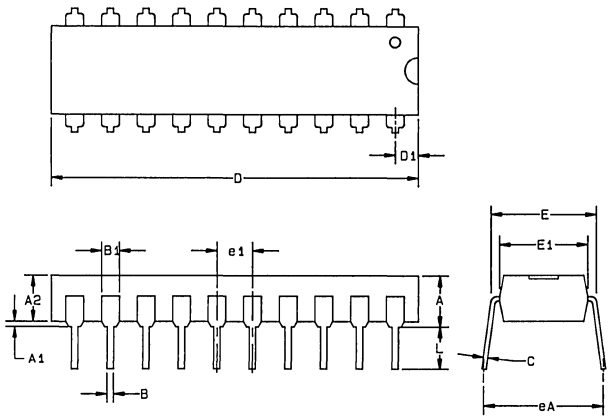
Figure 15. Equivalent Output Load Circuit

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE
MK4505M(N)-25	15ns	24 pin Plastic DIP	0°C to 70°C
MK4505M(N)-33	20ns	24 pin Plastic DIP	0°C to 70°C
MK4505M(N)-50	25ns	24 pin Plastic DIP	0°C to 70°C
MK4505S(N)-25	15ns	20 pin Plastic DIP	0°C to 70°C
MK4505S(N)-33	20ns	20 pin Plastic DIP	0°C to 70°C
MK4505S(N)-50	25ns	20 pin Plastic DIP	0°C to 70°C
MK4505M(K)-25	15ns	32 pin Plastic LCC	0°C to 70°C
MK4505M(K)-33	20ns	32 pin Plastic LCC	0°C to 70°C
MK4505M(K)-50	25ns	32 pin Plastic LCC	0°C to 70°C
MK4505S(K)-25	15ns	32 pin Plastic LCC	0°C to 70°C
MK4505S(K)-33	20ns	32 pin Plastic LCC	0°C to 70°C
MK4505S(K)-50	25ns	32 pin Plastic LCC	0°C to 70°C



20 PIN "N" PACKAGE
PLASTIC DIP (MK4505S)

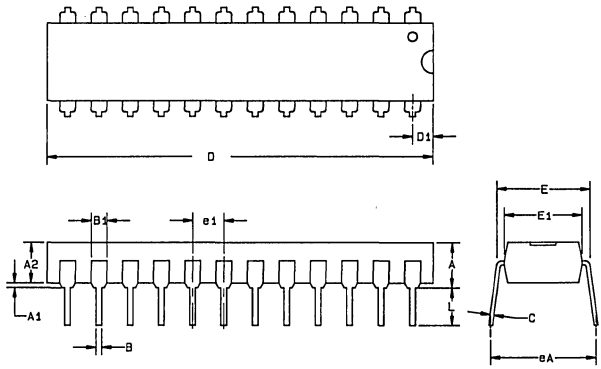


DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

24 PIN "N" PACKAGE
PLASTIC DIP (4505M)



DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.220	1.250	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

MK4511(N)-12/15/20

512 x 9 CMOS BiPORT™ RAM

MEMORY COMPONENTS

FEATURES

- ☐ Single Chip Bi-directional Message Passing
- ☐ Software Controlled Interrupt Outputs
- ☐ Addressable Status/Control Flags
- ☐ Identical Ports, 3-wire Controlled I/O

PIN NAMES

AD - Address/Data I/O	$\overline{INT}$ - Interrupt Output
$\overline{CE}$ - Chip Enable	GND - Ground
$\overline{OE}$ - Output Enable	V_{CC} - +5 Volts
$\overline{WE}$ - Write Enable	

Part Number	Access Time	Cycle Time	Cycle Rate
MK4511-12	120 ns	150 ns	6.67 MHz
MK4511-15	150 ns	190 ns	5.26 MHz
MK4511-20	200 ns	250 ns	4.00 MHz

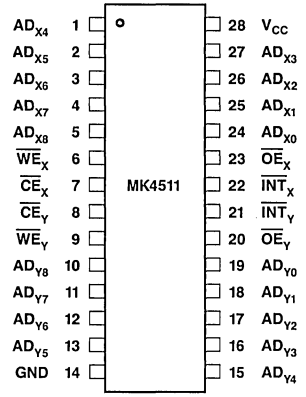


Figure 1. Pin Connections

DESCRIPTION

The MK4511 dual port RAM contains a single 512 x 9 CMOS memory matrix that can be accessed simultaneously from both of the input/output ports. Dual port operation is achieved through the use of a memory array composed of BiPORT memory cells. Each memory cell is accessible from both ports at all times.

Pin count is kept low through the use of address/data multiplexing. This technique is being used on advanced microprocessors and other devices to keep pin counts and package sizes down.

The MK4511 incorporates all functions required for dual port operations, including software controlled interrupt outputs. Use of the interrupt outputs is optional, allowing both polled and interrupt controlled applications.

SINGLE PORT OPERATIONS

The MK4511 may be viewed from either port as an ordinary three wire controlled 512 x 9 static RAM. Timing of read and write operations is altogether conventional; the presence of the other port is effectively transparent to the accessing processor. Therefore, all timing parameters are specified without references that differentiate between the ports.

READ MODE

The MK4511 is in Read Mode whenever Chip Enable ($\overline{CE}$) is low and Write Enable ($\overline{WE}$) is high. A stable address must be placed onto the AD lines t_{AS} prior to Chip Enable becoming active. The address must be held valid for t_{AH} following the falling edge of $\overline{CE}$.

In Read Mode the bi-directional AD lines are driven alternately by the user and the MK4511. Bus contention will occur if the user's address driver remains active too long. An Output Enable input ($\overline{OE}$) is provided, offering an improved ability to avoid bus contention. The $\overline{OE}$ control keeps the AD lines in a high impedance state while held high and for t_{OEL} after it goes low. Output data will be valid at the latter of t_{OEA} or t_{CEA}. A Chip Enable recovery time (t_{CER}) must be observed between assertions of $\overline{CE}$.

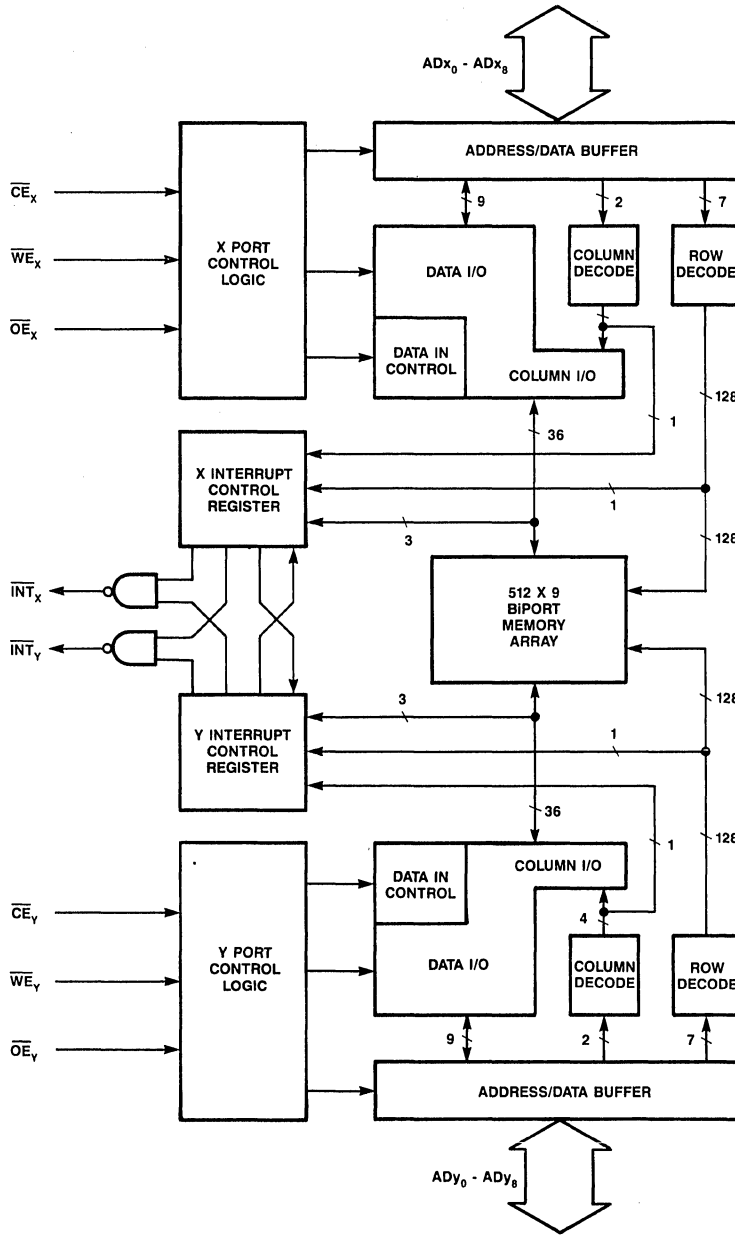


Figure 2. MK4511 Block Diagram

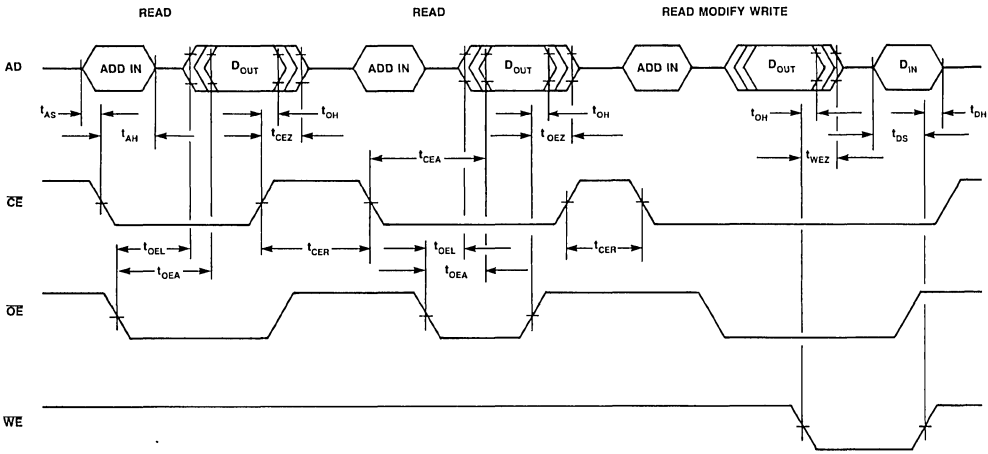


Figure 3. Read-Read-Read Modify Write

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK4511-12		MK4511-15		MK4511-20			
SYM	PARAMETERS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150		190		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AH}	Address Hold Time	20		25		35		ns	
t_{CEA}	Chip Enable Access Time		120		150		200	ns	1
t_{OEL}	Output Enable to Lo-Z	15		15		15		ns	
t_{OEA}	Output Enable Access Time		55		70		90	ns	1
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable Hi to Hi-Z		90		110		150	ns	
t_{OEZ}	Output Enable Hi to Hi-Z		40		50		65	ns	
t_{WEZ}	Write Enable Lo to Hi-Z		40		50		65	ns	
t_{CER}	Chip Enable Recovery Time	30		40		50		ns	

WRITE MODE

The MK4511 is in Write Mode whenever Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) are active low. As in Read Mode, the falling edge of $\overline{CE}$ latches the addresses present at the AD lines. The same addresses set-up and hold times apply. Input to the AD pins must then change from the address to input data. Input data present on the AD lines must be stable for t_{DS} prior to the end of write and must remain valid for t_{DH} afterward. A write cycle may be ended by the rising edge of $\overline{WE}$ or $\overline{CE}$. Chip Enable recovery time must also be observed in write mode.

Even if $\overline{WE}$ becomes active prior to $\overline{CE}$ becoming active, $\overline{CE}$ falling actually begins the cycle, latching the address present on the AD lines. Such cycles must reference t_{WEW}, t_{DS} and t_{DH} to the rising and falling edges of $\overline{CE}$ and $\overline{WE}$.

Read-Modify-Write cycles are possible if the outputs are enabled and the assertion of $\overline{WE}$ is delayed through t_{CEA}. The write cycle will begin when $\overline{WE}$ goes low. $\overline{WE}$ going low or $\overline{OE}$ going high will return the output drivers to high-Z within t_{WEZ} or t_{OEZ} respectively. The address latched when $\overline{CE}$ went low is still the valid address as the write cycle proceeds. The cycle is ended by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

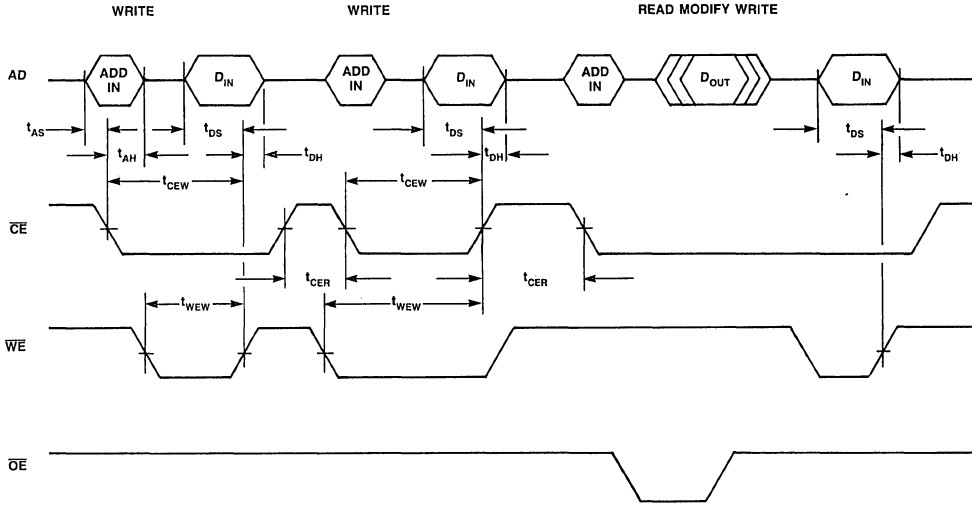


Figure 4. Write-Write-Read Modify Write

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK4511-12		MK4511-15		MK4511-20			
SYM	PARAMETERS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	150		190		250		ns	
t_{CEW}	Chip Enable to End of Write	120		150		200		ns	
t_{WEW}	Write Enable to End of Write	80		105		130		ns	
t_{DS}	Data Setup Time	40		55		65		ns	
t_{DH}	Data Hold Time	10		10		10		ns	

DUAL PORT OPERATIONS

INTERRUPT CONTROL

Although the Interrupt Control Registers for each port are accessed in parallel with RAM locations 000_H and $1FF_H$, they do not reside within the RAM array. They do not derive their control inputs from the RAM cells' status. In fact, changing the RAM location's contents via an opposite port will not affect a Interrupt Control Register at all. Therefore, for example, Port Y writing to address 000_H cannot affect the status of the Port X Interrupt Register.

The lower three bits of each byte written to the top and bottom addresses are the ones routed simultaneously to the Interrupt Control Registers. The Interrupt Control Registers consists of three flip-flops per port that serve as the Interrupt Request/Cancel flag (REQ/$\overline{CAN}$), Interrupt Output Enable/Disable flag (ENA/$\overline{DIS}$) and Interrupt Acknowledge/Ready flag (ACK/$\overline{RDY}$). As Figure 5 shows, the logic attached to the Interrupt Control Registers interprets interrupt status and drives the Interrupt Outputs.

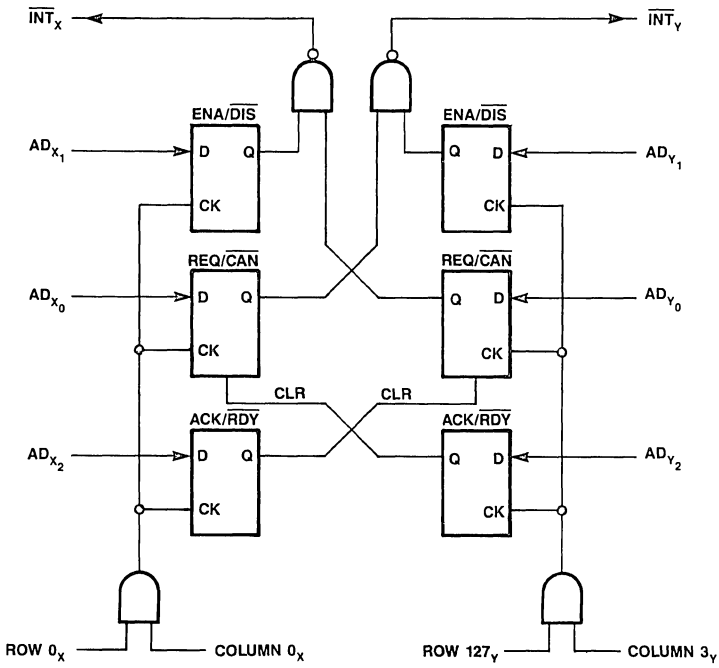


Figure 5. MK4511 Interrupt Control Registers and Interrupt Logic

INTERRUPT BYTE STRUCTURE

Because only the lower 3 bits of each interrupt byte are used to control the interrupt logic, the six MSBs written to the RAM have no affect on the state of the interrupt outputs, and may be used for any other purpose. The functions of the three control bits are:

Interrupt Output Enable/Disable
ENA/$\overline{DIS}_X$ (AD_{X1}) and ENA/$\overline{DIS}_Y$ (AD_{Y1})

Each port can disable its own interrupt outputs by writing a 0 ($XXXXXXXO_X$) into its ENA/$\overline{DIS}$ bit. If disabled, the interrupt pin will remain high regardless of interrupt requests from the other port. If an interrupt is requested of a disabled port, and an enabling 1 is later written into ENA/$\overline{DIS}$ of the disabled port, the interrupt output will go low t_{WIL} following the rising edge of the enabling write. Disabling a port with an active interrupt output pin will result in the output going high t_{WIH} after the end of the disabling write.

Interrupt Request/Cancel REQ/$\overline{CAN}_X$ (AD_{X0}) and REQ/$\overline{CAN}_Y$ (AD_{Y0})

Assuming that the Enable and Ready flags are set, writing a 1 into a REQ/$\overline{CAN}$ bit drives an enabled interrupt output pin on the opposite port low. The interrupt line will be driven low t_{WIL} following the end of the write that places a 1 in the REQ/$\overline{CAN}$ bit. For example, when $XXXXXXX1_2$ is written into location 000_H setting REQ/$\overline{CAN}_X$, $\overline{INT}_Y$ will go active low within t_{WIL}. Writing a 0 into the REQ/$\overline{CAN}$ bit cancels the interrupt request, returning the $\overline{INT}$ output to a high state t_{WIH} after the end of write.

Interrupt Acknowledge/Ready ACK/$\overline{RDY}_X$ (AD_{X2}) and ACK/$\overline{RDY}_Y$ (AD_{Y2})

Once an interrupt has been received at a port, the interrupt can be turned off by writing a 1 ($XXXXXX1XX_2$) into the ACK/$\overline{RDY}$ bit of the receiving port. Writing an acknowledge will cause the interrupt output to go high t_{WIH} after the end of the write. The interrupt request flag cannot be set while the acknowledge flag is active. An acknowledge must always be followed with a ready (writing a 0 over the 1) before requests from the other port can be recognized. Interrupt requests can be recognized t_{RRR} after a ready.

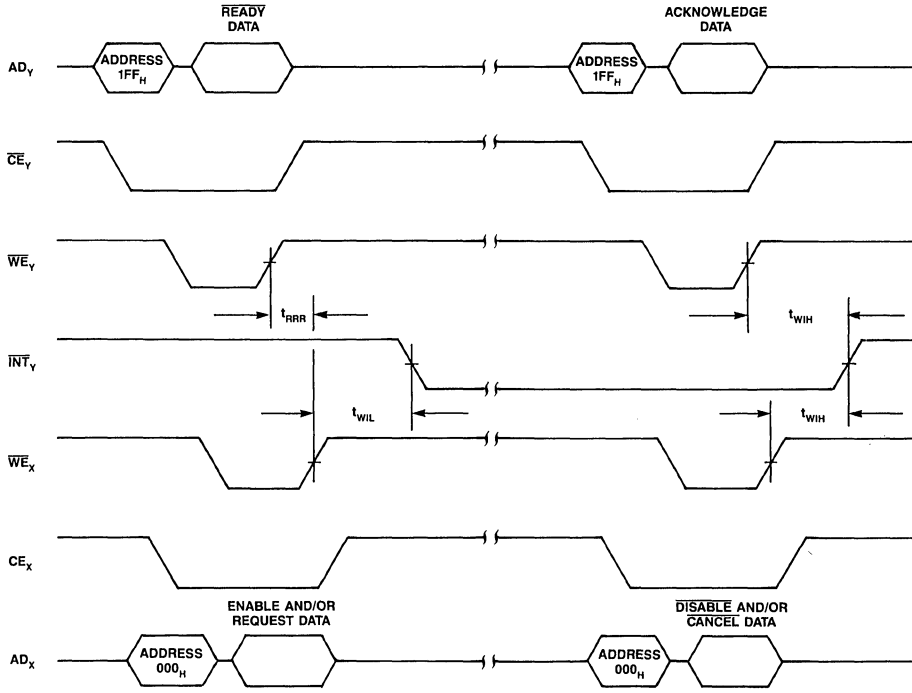


Figure 6. Interrupt Request Timing

INTERRUPT OUTPUT TIMING AC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12 MIN	MK4511-12 MAX	MK4511-15 MIN	MK4511-15 MAX	MK4511-20 MIN	MK4511-20 MAX	UNITS	NOTES
t_{WIL}	End of Write to $\overline{INT}$ Low		50		60		85	ns	
t_{WIH}	End of Write to $\overline{INT}$ High		50		60		85	ns	
t_{RRR}	Ready to Request Recognized		10		10		15	ns	

IMPLEMENTATION

Use of the interrupt feature is completely optional, allowing simple implementation of either interrupt driven or polled inter-processor communications applications. Either port can read or write any of the 512 bytes without restriction. Users who choose not to utilize the interrupt feature should leave the interrupt pins unconnected.

Any inter-processor communications application will doubtless employ some type of semaphore scheme. The use of the REQ/$\overline{\text{CAN}}$, ENA/$\overline{\text{DIS}}$ and ACK/$\overline{\text{RDY}}$ bits allow for each port to follow the exact status of the other port. The following example covers the case of port X interrupting port Y but applies equally well for port Y interrupting port X.

An Example Approach to Inter-processor Communications Using Pre-Allocated Memory Blocks and Interrupts

Pre-define six memory blocks of 85 bytes each (for a total of 510 bytes). Assign some number of blocks (probably three) to the X port and the balance to the Y port. Each port will write only to its assigned memory blocks, preventing port X and port Y attempting to load their messages into the same area.

Write the message to be passed into the Port X message area. When finished, read ACK/$\overline{\text{RDY}}_X$. If ready, request an interrupt on port Y by writing a 1 into REQ/$\overline{\text{CAN}}_X$. Indicate which message block(s) contain valid message data, using the upper six bits of the interrupt register byte.

Now, acknowledge the interrupt to Port Y by writing a 1 to the acknowledge flag on Port Y. Begin reading the message via Port Y. The acknowledge should not be removed until after the message has been read. When it has been, set the ACK/$\overline{\text{RDY}}_Y$ flag to ready.

Check to see that the message was received. Monitor ACK/$\overline{\text{RDY}}_Y$ via Port X. Changes to the message block should not be made by Port X until ACK/$\overline{\text{RDY}}_Y$ is zero, indicating Port Y has finished reading its message.

COLLISION

The central objective of the MK4511 design effort was to produce a component that makes implementation of asynchronous, random access dual port memory applications, that can assure data integrity, as simple and inexpensive to design and implement as possible.

Data integrity can be called into question if port to port collision occurs. A collision is defined as both ports attempting to write at the same address or one port reading and one writing at the same address at the same time.

While a collision is generally considered undesirable, the conditions that can lead to ill-defined results are definable and manageable. In the case of a write/write collision, the data stored at the address in question may or may not have any similarity to either write attempted or the previously resident data if the delay between the ends of the writes (t_{WWL})is not long enough. On the other hand, write/read collisions do not affect the integrity of data storage, but do have an impact on the validity of output data at definable points in time (t_{ODI} and t_{ODV}). Figures 7 and 8 describe these conditions.

All of the parameters indicated reference the validity of the entire byte of data. Individual bits of a byte change state at slightly different rates. Though this is a subtle distinction, it is nonetheless important, particularly in the case of monitoring ACK/$\overline{RDY}$. Be aware that a read may catch the ready bit at a valid zero before the rest of the byte has finished transition. Nevertheless, because there is no reason for the ready bit to go low, other than that the opposite port is writing a zero into it, catching it low is a reliable indication that the other port is ready. This is all to say that single significant bit flag write/read operations can proceed reliably under collision conditions where byte wide operations cannot.

Simultaneous reads at the same address will always produce valid data and are therefore not considered a collision in this context.

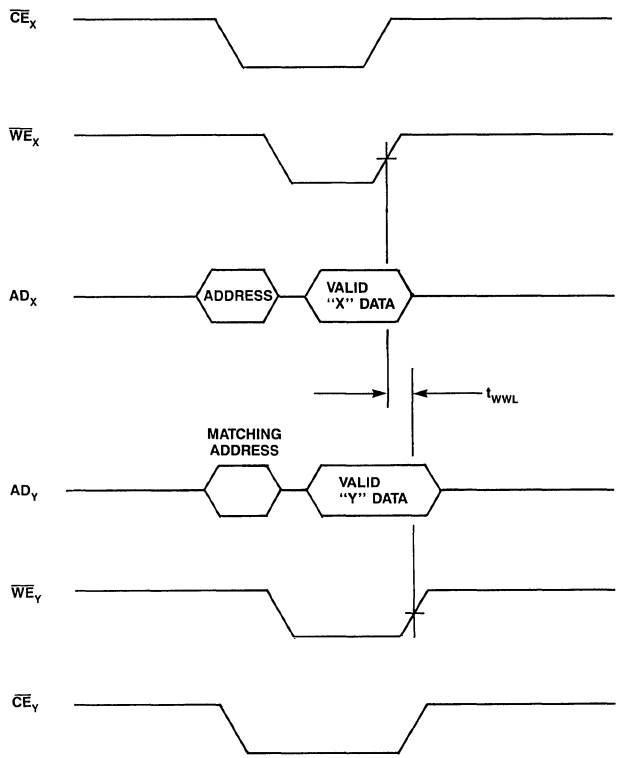


Figure 7. Minimum Write To Write Latency For Valid Data Storage

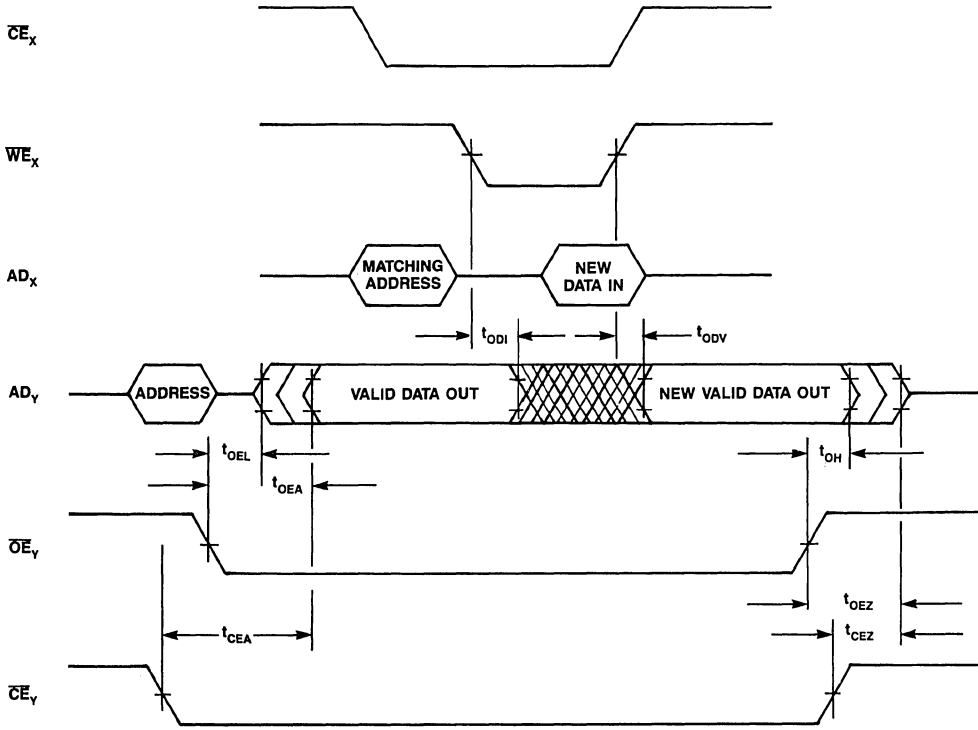


Figure 8. Simultaneous Read Write Timing

COLLISION TIMING
AC ELECTRICAL CHARACTERISTICS

(0°C≤T_A≤70°C) (V_{CC} = 5.0 V ± 10 percent)

		MK4511-12		MK4511-15		MK4511-20			
SYM	PARAMETERS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{ODI}	Output Data Indeterminant	10		10		10		ns	
t_{ODV}	Output Data Valid		90		115		150	ns	
t_{WWL}	Write to Write Latency	80		105		130		ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −0.3 V to +7.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature ..... −55°C to +125°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 20 mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} + 0.3	V	2,3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	2,3

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current per Port		25	mA	4
I_{CC2}	TTL Standby Current per Port		2.5	mA	5
I_{CC3}	CMOS Standby Current per Port		1	mA	6
I_{IL}	Input Leakage Current	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−5	+5	μA	7
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −1 mA)	2.4		V	2
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 2.1 mA)		0.4	V	2

CAPACITANCE

(T_A = 25°C; f = 1.0 MHz)

SYM	PARAMETERS	TYP	UNITS	NOTES
C_I	Capacitance on any Input Pin	4	pF	8
C_O	Capacitance on any Output Pin	10	pF	8,9

NOTES
1. Measured with load shown in Figure 9.
2. All voltages referenced to GND.
3. No more than one negative undershoot or positive overshoot of 1.5 V with a maximum pulse width of 10 ns is allowed once per cycle.
4. Output buffer is deselected, both ports are active.
5. All inputs = V_{IH}.
6. All inputs ≥ V_{CC} − 0.2V
7. Measured with $GND \leq V_I \leq V_{CC}$ and outputs deselected.
8. Effective capacitance is calculated as follows: $C = \frac{\Delta Q}{\Delta V}$ ΔV = 3 V
9. Output buffer is deselected.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Levels	0.8 V and 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

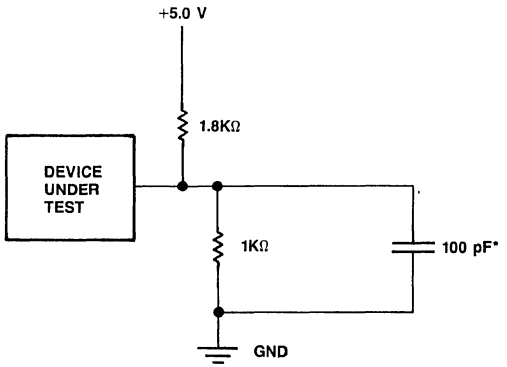


Figure 9. Equivalent Output Load Circuit

ORDERING INFORMATION

Part Number	Access Time	Package Type	Temperature Range
MK4511N-12	120 ns	28 pin Plastic DIP	0°C to 70°C
MK4511N-15	150 ns	28 pin Plastic DIP	0°C to 70°C
MK4511N-20	200 ns	28 pin Plastic DIP	0°C to 70°C

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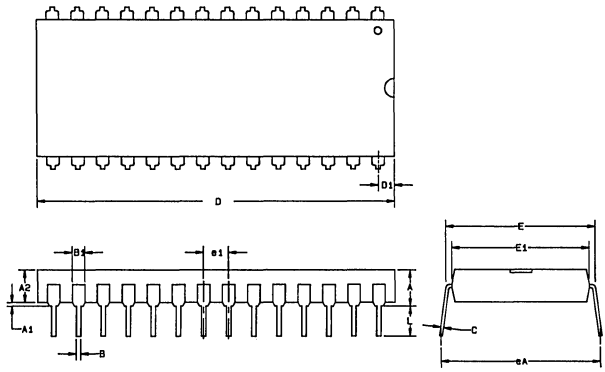
28 PIN
"N"Package



DIM	INCHES		NOTES
	MIN	MAX	
A	-	.210	2
A1	.015	-	2
A2	.140	.160	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.440	1.470	1
D1	.065	.085	
E	.600	.625	
E1	.530	.560	
e1	.090	.110	
eA	.600	.700	
L	.120	-	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

THOMSON COMPONENTS
MOSTEK

MK4801A(N,P)-55/70/90

1K x 8 BIT STATIC RAM

MEMORY COMPONENTS

FEATURES

- Static operation
- Organization: 1K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- 24/28 pin ROM/PROM compatible pin configuration
- High performance
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control

Part No.	Access Time	R/W Cycle Time
MK4801A-55	55 nsec	55/65 nsec
MK4801A-70	70 nsec	70/80 nsec
MK4801A-90	90 nsec	90/100 nsec

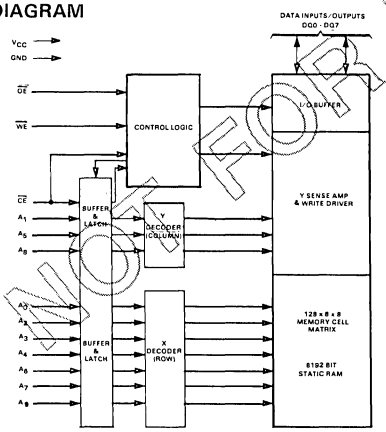
DESCRIPTION

The MK4801A uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

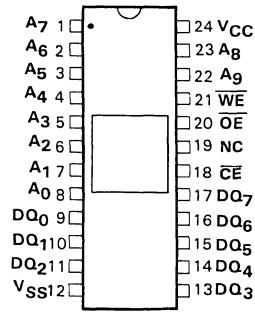
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5V to + 7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[7]

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-2.0		.8	V	1,9

DC ELECTRICAL CHARACTERISTICS[1,7]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 V ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		60	125	mA	8
I_{IL}	Input Leakage Current (Any Input)	-10		10	μA	2
I_{OL}	Output Leakage Current	-10		10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = 1 mA	2.4			V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA			0.4	V	

CAPACITANCE[1,7]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 V ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	All pins (except D/Q)	4 pF	6 pF	
$C_{D/Q}$	D/Q pins	10 pF	12 pF	6

AC ELECTRICAL CHARACTERISTICS [3,4]

($0°C \leq T_A \leq 70°$) (V_{CC} = 5.0 V ± 5%)

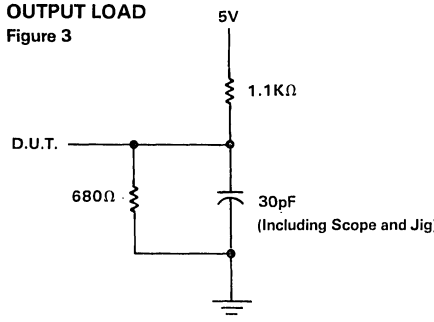
SYM	PARAMETER	MK4801A-55		MK4801A-70		MK4801A-90		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	55		70		90		ns	
t_{AA}	Address Access Time		55		70		90	ns	5
t_{CEA}	Chip Enable Access Time		25		35		45	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	15	5	20	5	30	ns	
t_{OEA}	Output Enable Access Time		25		35		45	ns	5
t_{OEZ}	Output Enable Data Off Time	5	15	5	20	5	30	ns	
t_{AZ}	Address Data Off Time	10		10		10		ns	
t_{WC}	Write Cycle Time	65		80		100		ns	
t_{AS}	Address Setup Time	0		0		0		ns	see text
t_{AH}	Address Hold Time	15		20		30		ns	see text
t_{DSW}	Data To Write Setup Time	5		5		5		ns	
t_{DHW}	Data From Write Hold Time	10		10		10		ns	
t_{WD}	Write Pulse Duration	25		30		40		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	10	5	15	5	25	ns	
t_{WPL}	Write Pulse Lead Time	40		50		60		ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. Measured with $.4 \leq V_I \leq 5.0$ V, outputs deselected and V_{CC} = 5 V.
3. AC measurements assume Transition Time = 5 ns, levels V_{SS} to 3.0 V.
4. Input and output timing reference levels are at 1.5 V.
5. Measured with a load as shown in Figure 3.
6. Output buffer is deselected.
7. A minimum of 2 ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
8. I_{CC} measured with outputs open.
9. Negative undershoots to a minimum of –1.5 V are allowed with a maximum of 50 ns pulse width.

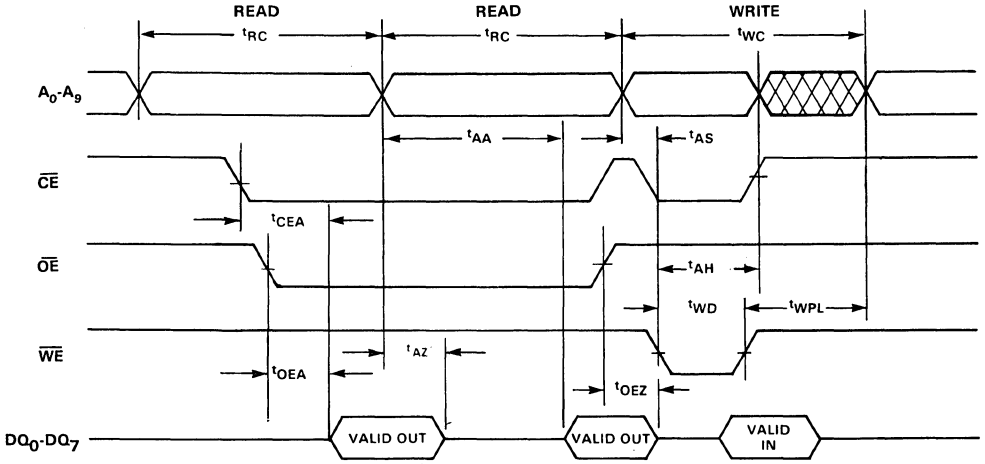
OUTPUT LOAD

Figure 3



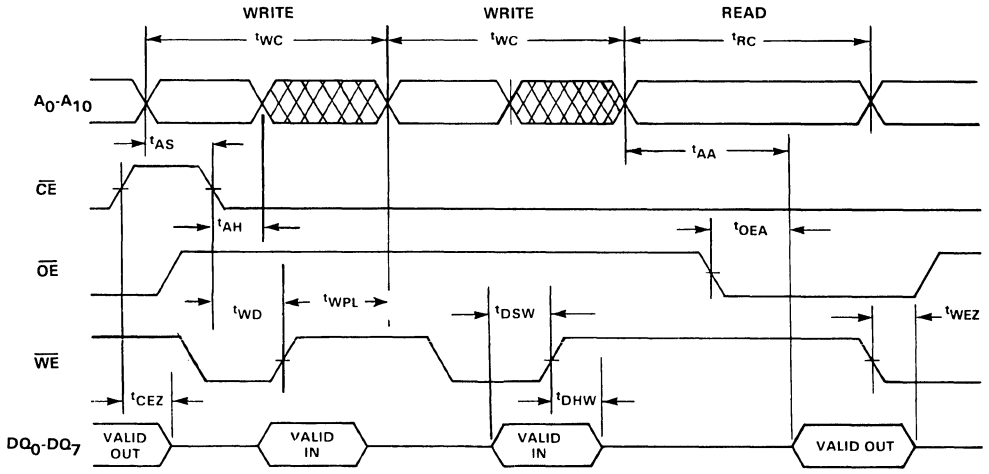
TIMING DIAGRAM

Figure 4



TIMING DIAGRAM

Figure 5



The MK4801A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

OPERATION

Read Mode

The MK4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

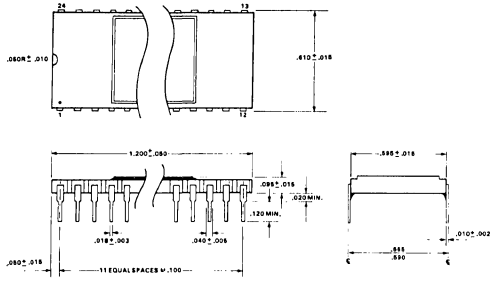
The MK4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

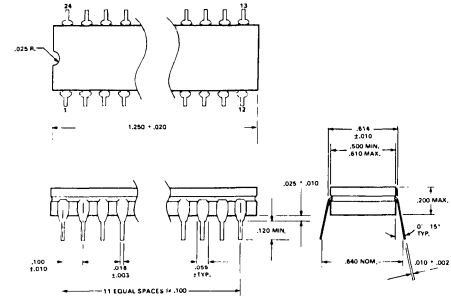
NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

PACKAGE DESCRIPTION
Ceramic Dual-In-Line (P)
24 Pin
Figure 6



PACKAGE DESCRIPTION
Cerdip (J)
24 Pin
Figure 7



MK4801A(N,P)-1/2/3/4

1K x 8 BIT STATIC RAM

MEMORY COMPONENTS

FEATURES

- Static operation
- Organization: 1K x 8 bit RAM JEDEC pinout
- High performance
- Pin compatible with Mostek's BYTEWYDE™ memory family
- 24/28 pin ROM/PROM compatible pin configuration
- CE and OE functions facilitate bus control
- MKB version screened to MIL-STD-883

Part No.	R/W Access Time	R/W Cycle Time
MK4801A-1	120 nsec	120 nsec
MK4801A-2	150 nsec	150 nsec
MK4801A-3	200 nsec	200 nsec
MK4801A-4	250 nsec	250 nsec

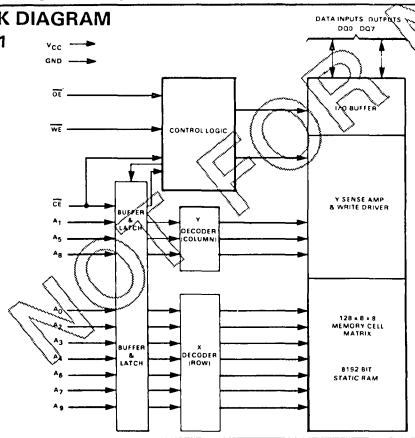
DESCRIPTION

The MK4801A uses Mostek's advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's microprocessor applications.

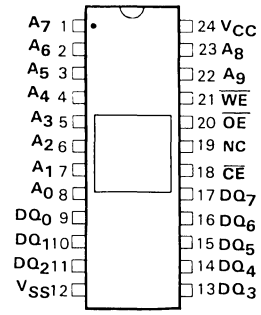
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

CE	OE	WE	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	WE	Write Enable
CE	Chip Enable	OE	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[7]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1, 9

DC ELECTRICAL CHARACTERISTICS[1,7]

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 V ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		50	80	mA	8
I_{IL}	Input Leakage Current (Any Input)	-10		10	μA	2
I_{OL}	Output Leakage Current	-10		10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = 1 mA	2.4			V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA			0.4	V	

CAPACITANCE[1,7]

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 V ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	All pins (except D/Q)	4 pF	6 pF	
$C_{D/Q}$	D/Q pins	10 pF	12 pF	6

AC ELECTRICAL CHARACTERISTICS [3,4]

(0°C ≤ T_A ≤ 70°) (V_{CC} = 5.0 V ± 5%)

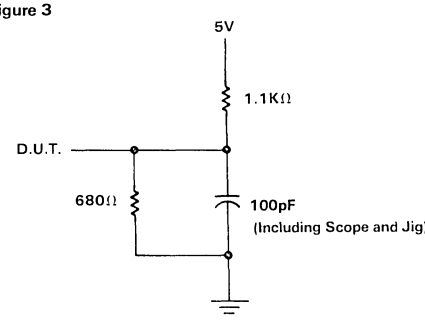
		-1		-2		-3		-4			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	5
t_{CEA}	Chip Enable Access Time		60		75		100		125	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{OEA}	Output Enable Access Time		60		75		100		125	ns	5
t_{OEZ}	Output Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{AZ}	Address Data Off Time	10		10		10		10		ns	
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	see text
t_{AH}	Address Hold Time	40		50		65		80		ns	see text
t_{DSW}	Data To Write Setup Time	10		10		15		20		ns	
t_{DHW}	Data From Write Hold Time	10		10		10		10		ns	
t_{WD}	Write Pulse Duration	45		50		60		70		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{WPL}	Write Pulse Lead Time	75		90		130		170		ns	

NOTES:

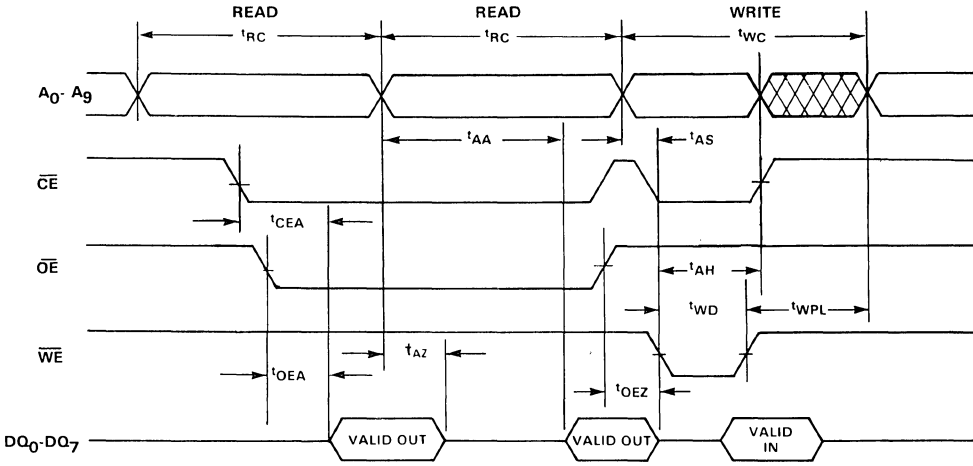
1. All voltages referenced to V_{SS}
2. Measured with .4 ≤ V_I ≤ 5.0 V, outputs deselected and V_{CC} = 5 V
3. AC measurements assume Transition Time = 5 ns, levels V_{SS} to 3.0 V
4. Input and output timing reference levels are at 1.5 V
5. Measured with a load as shown in Figure 3.
6. Output buffer is deselected.
7. A minimum of 2ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
8. I_{CC} measured with outputs open.
9. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

OUTPUT LOAD

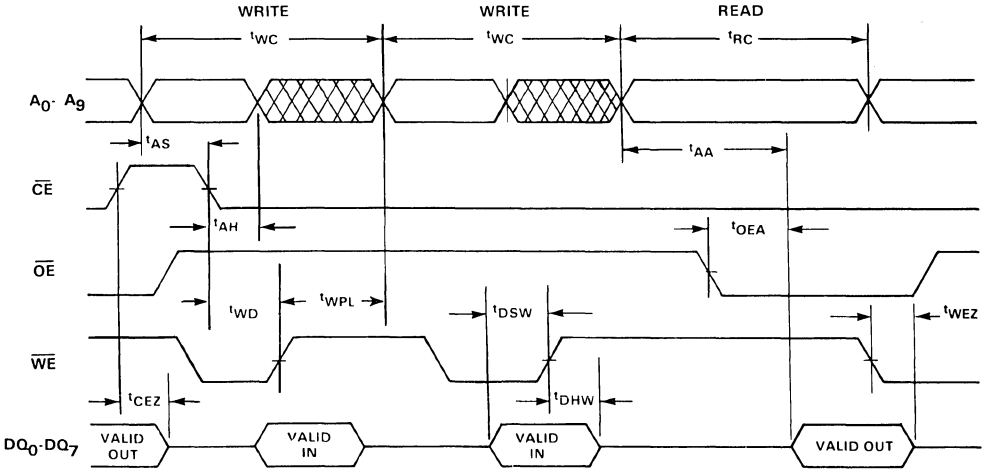
Figure 3



TIMING DIAGRAM
Figure 4



TIMING DIAGRAM
Figure 5



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The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs. Mostek also offers a higher performance version of the MK4801A designated the MK4801A.

OPERATION

Read Mode

The MK4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

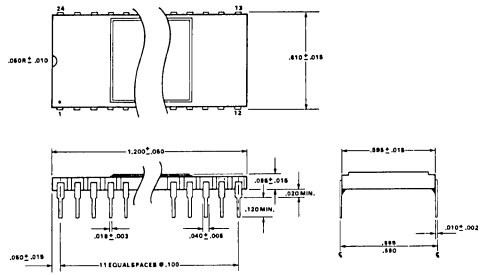
The MK4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

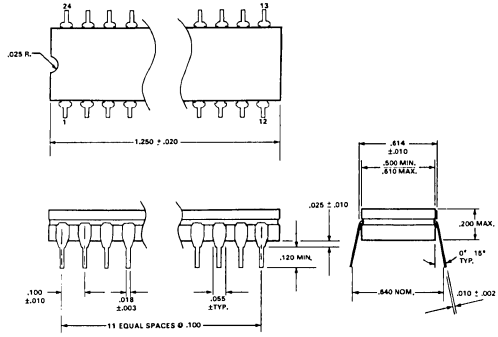
NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

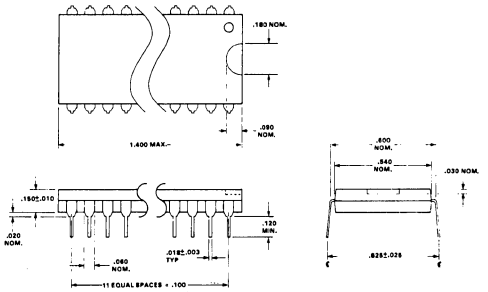
PACKAGE DESCRIPTION
Ceramic Dual-In-Line (P)
24 Pin
Figure 6



PACKAGE DESCRIPTION
CERDIP (J)
24 Pin
Figure 7



Plastic Dual-In-Line (N)
24 Pin
Figure 8



NOTE. Overall length includes .008 flash on either end of package

THOMSON COMPONENTS
MOSTEK

ET2147H • ETL2147H(N,J)-35/45/55

4096 x 1 STATIC RAM

MEMORY COMPONENTS

The ET2147H is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology X-MOS. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out non destructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high.

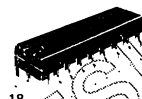
The output is held in a high impedance state during write to simplify common I/O applications.

- All inputs and outputs directly TTL compatible
- Static operation - no clocks or refreshing required
- Automatic power down
- High speed - down to 35 ns access time
- Three-state output for bus interface
- Separate Data In and Data Out pins
- Single + 5V supply
- Standard 18-pin dual-in-line package

Max Access/Current	ET2147H-1	ET2147H-2	ET2147H-3	ETL2147H-3
Access (TAVQV—ns)	35	45	55	55
Active Current (ICC—mA)	180	180	180	125
Standby Current (ISB—mA)	30	30	30	20

NMOS

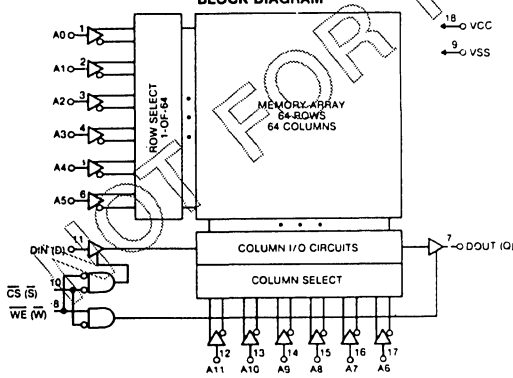
4096 X 1
STATIC RAMs



N SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE
J SUFFIX
CERDIP PACKAGE

BLOCK DIAGRAM*

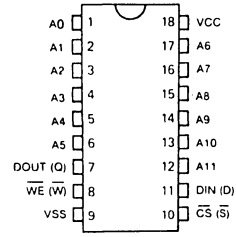


TRUTH TABLE*

CS (S)	WE (W)	DIN (D)	DOUT (Q)	Mode	Power
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

* The symbols in parentheses are proposed industry standard

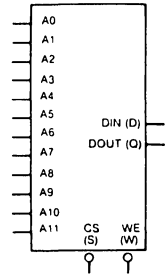
PIN ASSIGNMENT



PIN NAMES*

A0–A11	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
DIN (D)	Data In
DOUT (Q)	Data Out
VCC	Power (5V)
VSS	Ground

LOGIC SYMBOL*



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to VSS	– 3.5V to + 7V
Storage Temperature Range	–65°C to + 150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	– 65°C to + 135°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions	MIN	MAX	UNITS
Supply Voltage (VCC)	4.5	5.5	V
Ambient Temperature (TA)	0	+ 70	°C

DC ELECTRICAL CHARACTERISTICS TA = 0°C to + 70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	ETL 2147H-3		ET2147H -1, -2, -3		Units
			Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max	–	10	–	10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max	–	50	–	50	μA
VIL	Input Low Voltage		– 3.0	0.8	– 3.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA	–	0.4	–	0.4	V
VOH	Output High Voltage	IOH = – 4.0 mA	2.4		2.4	–	V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open	–	125	–	180	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH	–	20	–	30	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min	–	30	–	40	mA

CAPACITANCE TA = 25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V	–	5	pF
COUT	Output Capacitance	VOUT = 0V	–	6	pF

Note 1 : The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute

Note 2 : These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper orientation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3 : This parameter is guaranteed by periodic testing.

AC TEST CONDITIONS

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Level (H-1)	1.5V
Output Timing Reference Levels (H.2, H.3, H.3L)	0.8V and 2.0V
Output Load (See Fig. 1)	

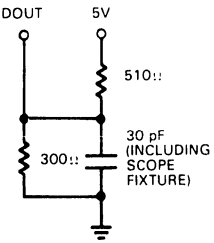


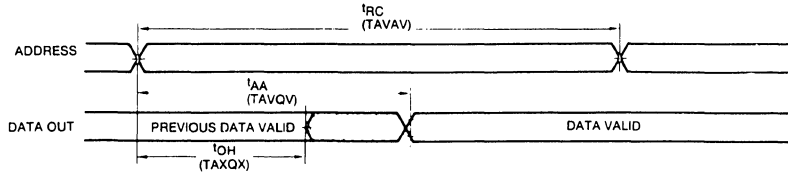
Fig. 1 – Ouptut Load

READ CYCLE AC ELECTRICAL CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10% (Note 1)

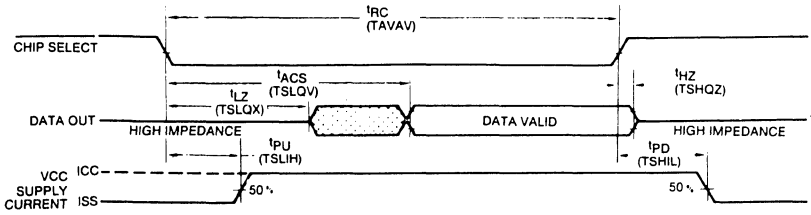
Symbol		Parameter	ET2147H -1		ET2147H -2		ET2147H-3 ETL2147H-3		Unit
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	35	–	45	–	55	–	ns
t_{AA}	TAVQV	Address Access Time	–	35	–	45	–	55	ns
t_{ACS}	TSLQV	Chip Select Access Time (Note 4)	–	35	–	45	–	55	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	5	–	5	–	10	–	ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	30	0	30	0	30	ns
t_{OH}	TAXQX	Output Hold from Address Change	5	–	5	–	5	–	ns
t_{PU}	TSLIH	Chip Select to Power-Up	0	–	0	–	0	–	ns
t_{PD}	TSHIL	Chip Deselect to Power-Down	–	20	–	20	–	20	ns

READ CYCLE WAVEFORMS*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



Note 4 : Address must be valid coincident with or prior to the chip select transition from high to low.

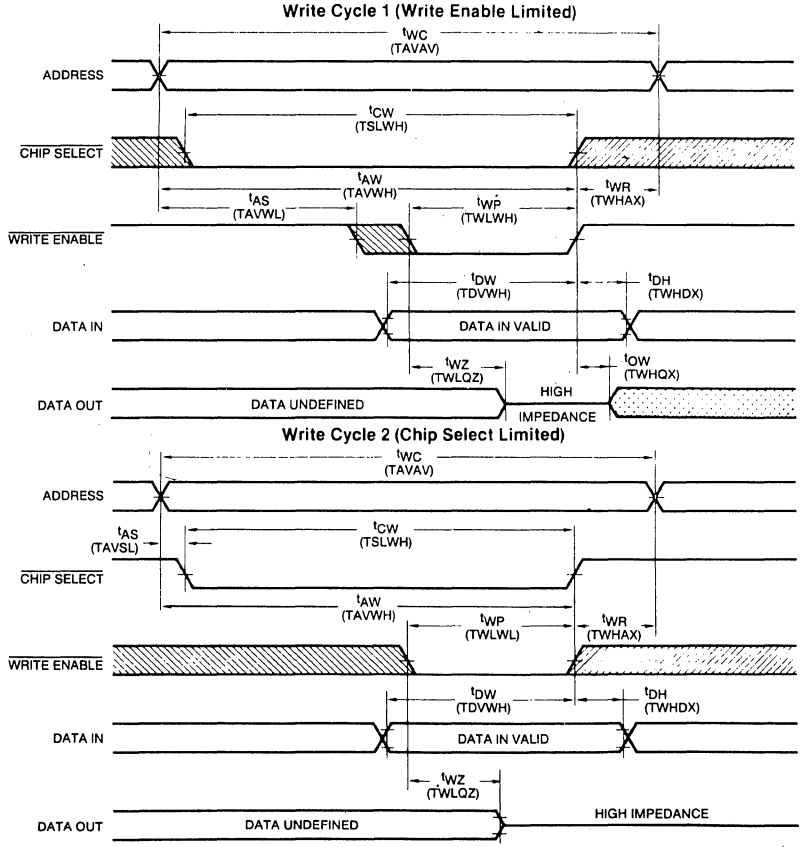
Note 5 : Measured ± 50 mV from steady state voltage. This parameter is sampled and not 100 % tested.

*The symbols in parentheses are proposed industry standard.

WRITE CYCLE AC ELECTRICAL CHARACTERISTICS TA = 0°C to + 70°C, VCC = 5V ± 10% (Note 1)

Symbol		Parameter	ET2147H -1		ET2147H -2		ET2147H-3 ETL2147H-3		Unit
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	35	–	45	–	55	–	ns
t_{CW}	TSLWH	Chip Select to End of Write	35	–	45	–	45	–	ns
t_{AW}	TAVWH	Address Valid to End of Write	35	–	45	–	45	–	ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0	–	0	–	0	–	ns
t_{WP}	TWLWH	Write Pulse Width	20	–	25	–	25	–	ns
t_{WR}	TWHAX	Write Recovery Time	0	–	0	–	10	–	ns
t_{DW}	TDVWH	Data Set-Up Time	20	–	25	–	25	–	ns
t_{DH}	TWHDX	Data Hold Time	10	–	10	–	10	–	ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	20	0	25	0	25	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 5)	0	–	0	–	0	–	ns

WRITE CYCLE WAVEFORMS* (Note 6)

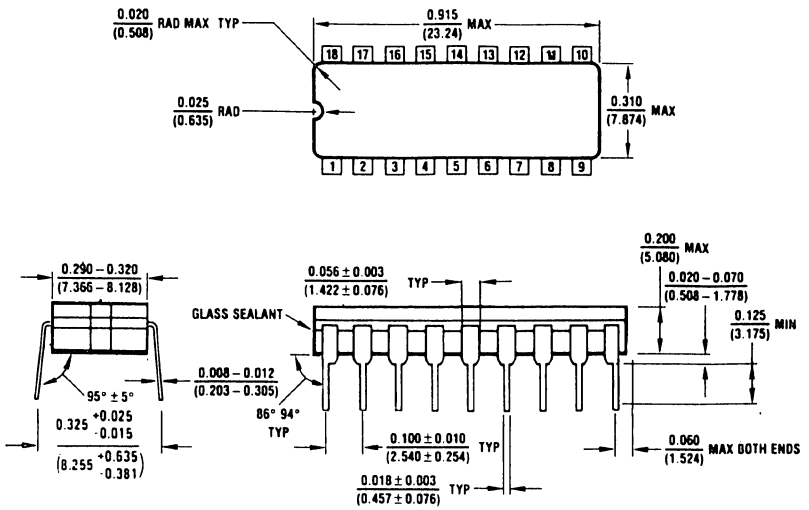


Note 6 : The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

* The symbols in parentheses are proposed industry standard.

PHYSICAL DIMENSIONS

inches (millimeters)



Ceramic Dual-In-Line-Package (J)
Order Number ET2147HJ -1, -2, -3
ETL2147HJ-3
ET Package Number J18A

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

MK41H66/MK41H67(N,P)-20/25/35

16K × 1 CMOS STATIC RAM

MEMORY COMPONENTS

FEATURES

- ☐ 20, 25, and 35 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 20-pin, 300 mil Plastic and Ceramic DIP
- ☐ All input and output pins TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 μA CMOS Standby Current (MK41H67)
- ☐ High speed chip select (MK41H66)
- ☐ JEDEC standard pinout

MK41H66 TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Q	Power
H	X	Deselect	High Z	Active
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

X = Don't Care

MK41H67 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	Mode	Q	Power
H	X	Deselect	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

DESCRIPTION

The MK41H66 and MK41H67 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single +5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H67 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

The MK41H66 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

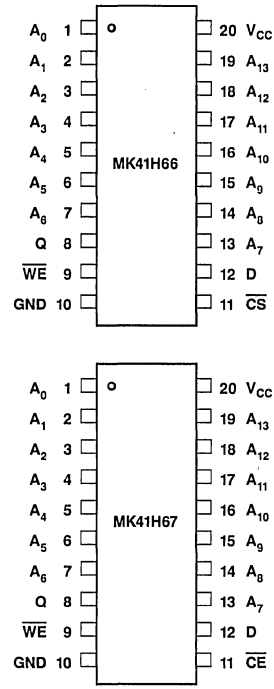


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{13} - Address	$\overline{WE}$ - Write Enable
$\overline{CE}$ - Chip Enable (MK41H67)	GND - Ground
$\overline{CS}$ - Chip Select (MK41H66)	V_{CC} - + 5 volts
	D - Data In
	Q - Data Out

OPERATIONS

READ MODE

The MK41H66/7 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}/\overline{CS}$ (Chip Enable/Select) is low, providing a ripple-through access to any one of 16,384 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}/\overline{CS}$ access time is satisfied. If $\overline{CE}/\overline{CS}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the Data Output pin is controlled by the $\overline{CE}/\overline{CS}$, and $\overline{WE}$ control signals. The Q may be in an indeterminate state at t_{CL}, but the Q will always have valid data at t_{AA}.

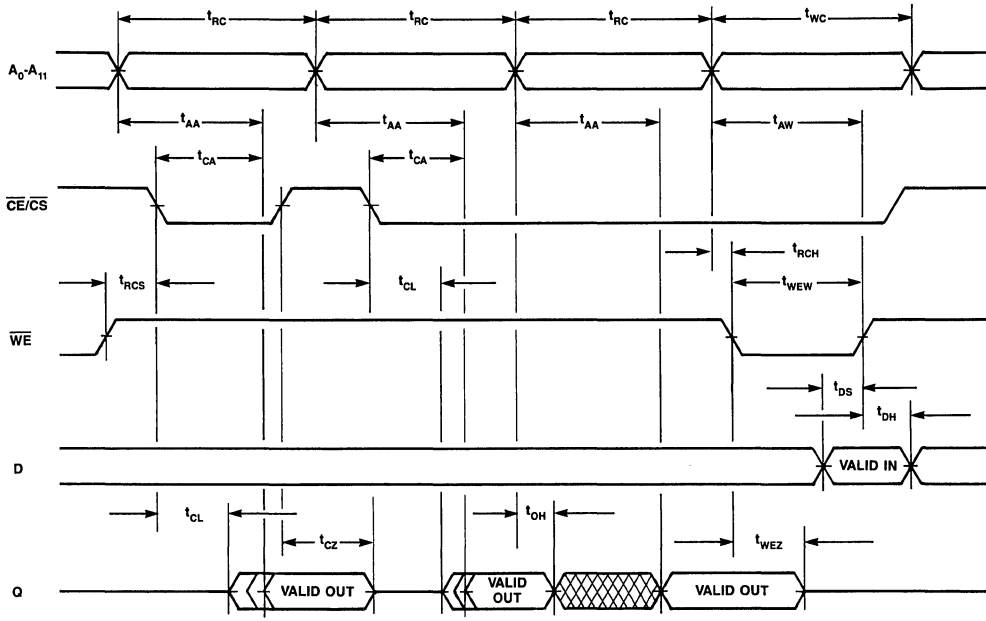


Figure 2. Read-Read-Read-Write Timing

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H6X-20		MK41H6X-25		MK41H6X-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CL}	Chip Enable to Low-Z (MK41H67)	5		5		5		ns	2
t_{CL}	Chip Select to Low-Z (MK41H66)	3		3		3		ns	2
t_{CA}	Chip Enable Access Time (MK41H67)		20		25		35	ns	1
t_{CA}	Chip Select Access Time (MK41H66)		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41H67)		8		10		13	ns	2
t_{CZ}	Chip Select to High-Z (MK41H66)		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H66/7 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}/\overline{CS}$ inputs are in the low state. $\overline{CE}/\overline{CS}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}/\overline{CS}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}/\overline{CS}$, or $\overline{WE}$.

If the output is enabled ($\overline{CE}/\overline{CS}$ is low), then $\overline{WE}$ will return the output to high impedance within t_{WEZ} of its falling edge. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}/\overline{CS}$ or $\overline{WE}$.

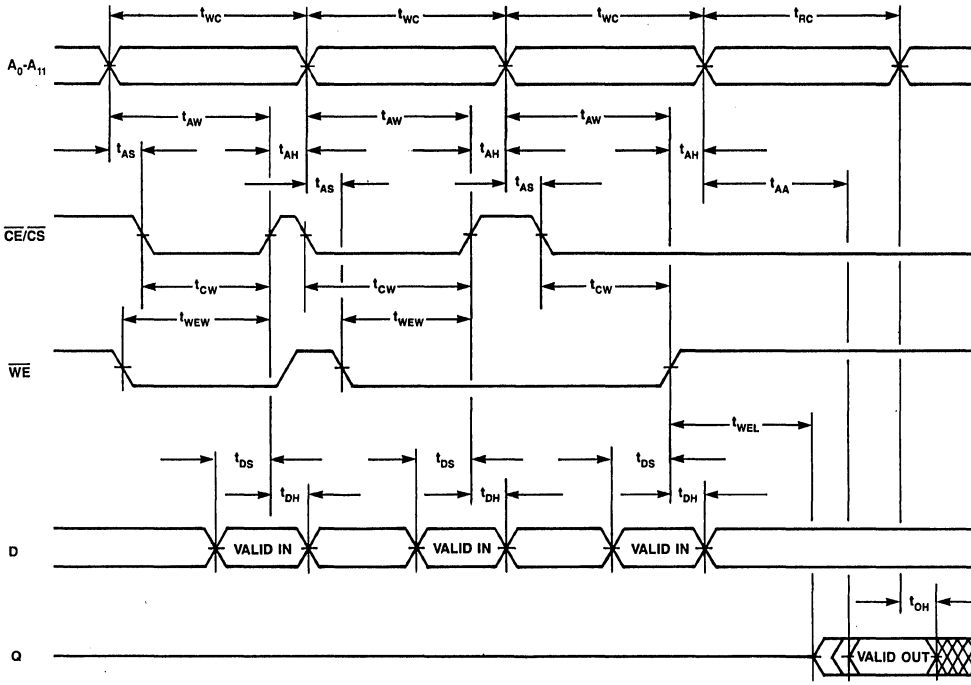


Figure 3. Write-Write-Write-Read Timing

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H6X-20		MK41H6X-25		MK41H6X-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	10		12		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

LOW V_{CC} DATA RETENTION TIMING (MK41H67)

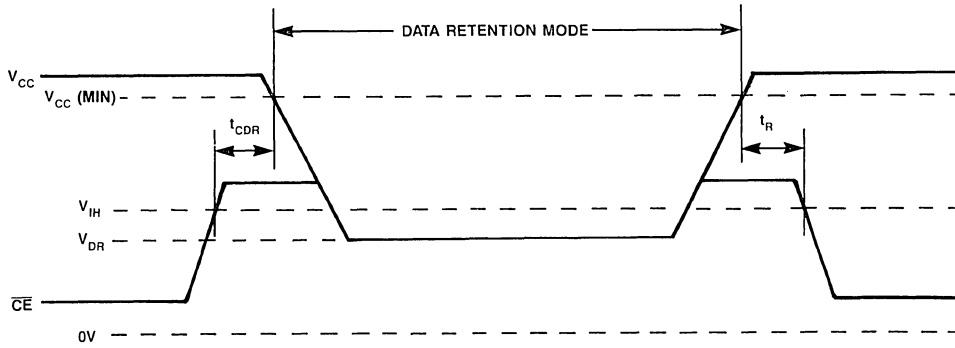


Figure 4. Data Retention Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41H67 Only)

The MK41H67 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

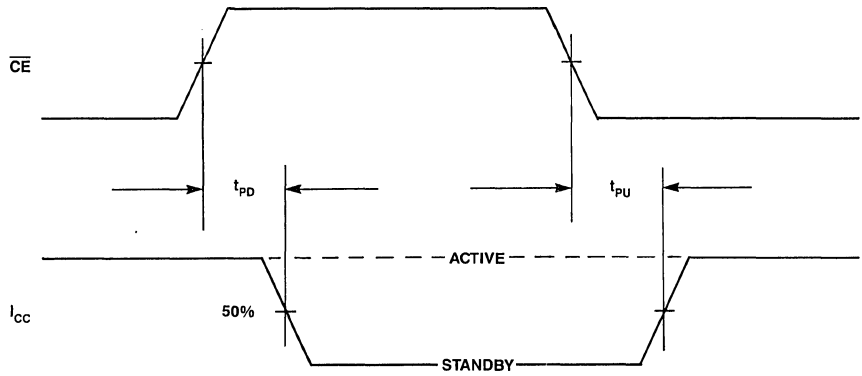


Figure 5. Standby Mode Timing

STANDBY MODE
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

		MK41H67-20		MK41H67-25		MK41H67-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H66/7 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H66/7 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H66/7, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−1.0		0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	5
I_{CC2}	TTL Standby Current (MK41H67 only)		10	mA	6
I_{CC3}	CMOS Standby Current (MK41H67 only)		50	µA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	µA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	µA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

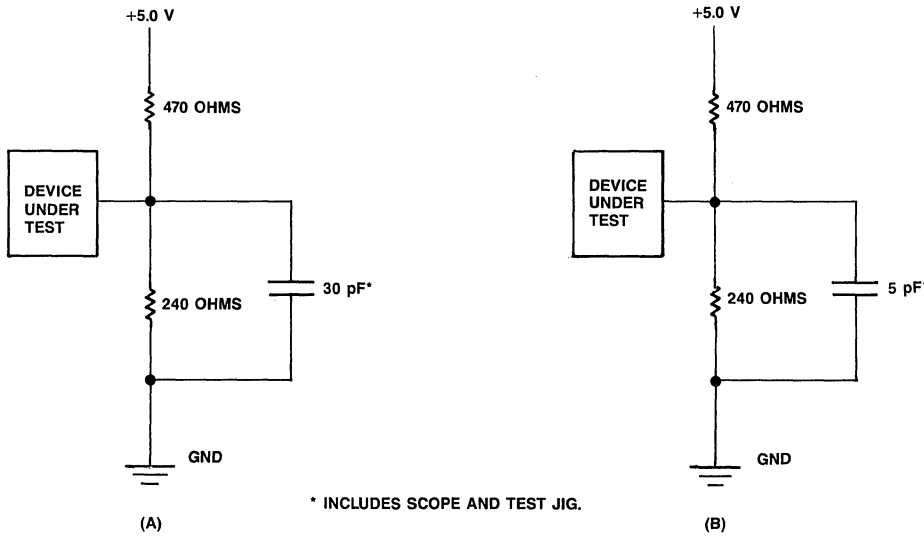
SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on Q pin	8	10	pF	6,10

NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
6. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
7. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V
   GND + 0.3 V ≥ A_0-A_{13} ≥ V_{IL} (min) or V_{IH} (max) ≥ A_0-A_{13} ≥ V_{CC} −0.3 V.
   All Other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}$/$\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

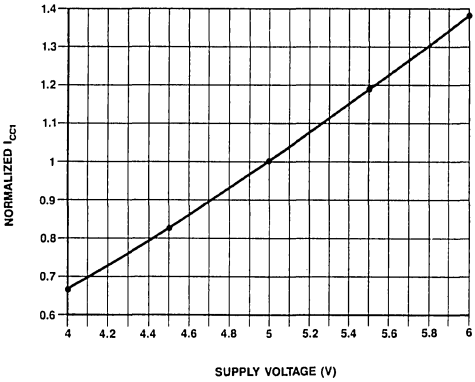


* INCLUDES SCOPE AND TEST JIG.

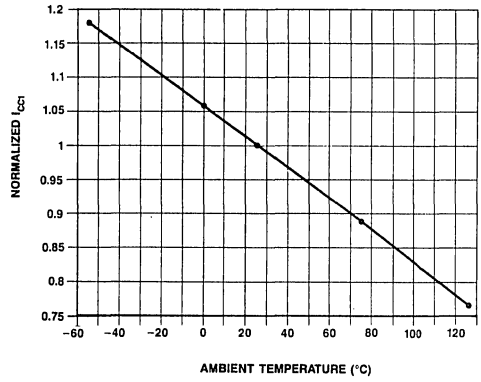
Figure 6. Output Load Circuits

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

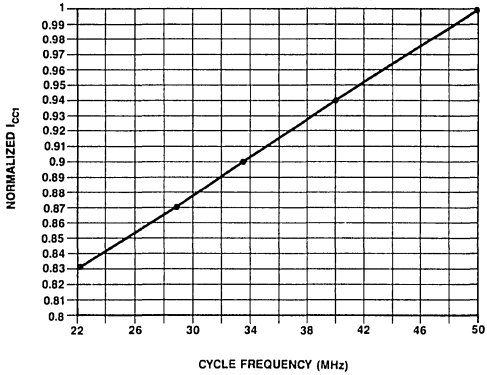
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE T_A=0°C



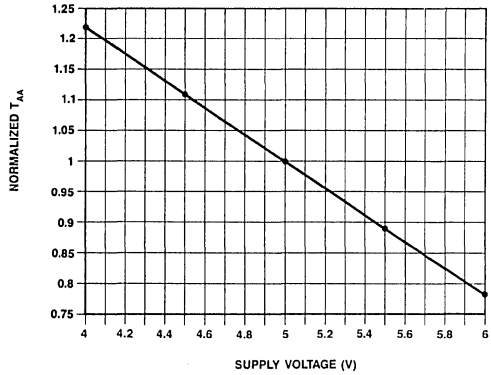
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



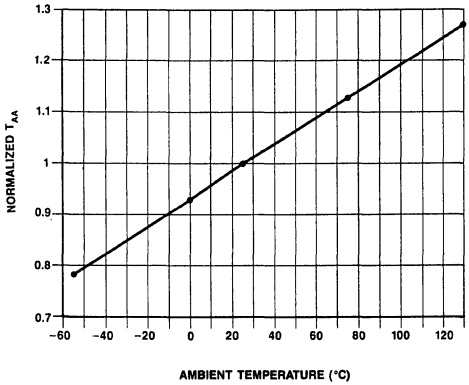
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC}=5.0V T_A=25°C



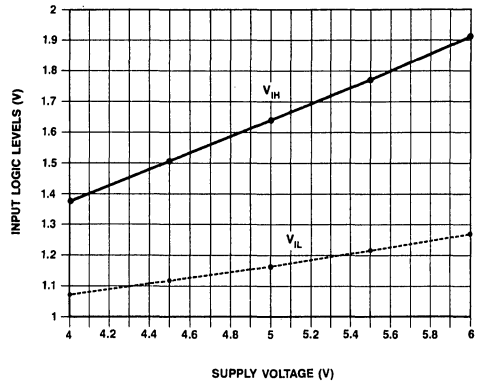
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A=25°C



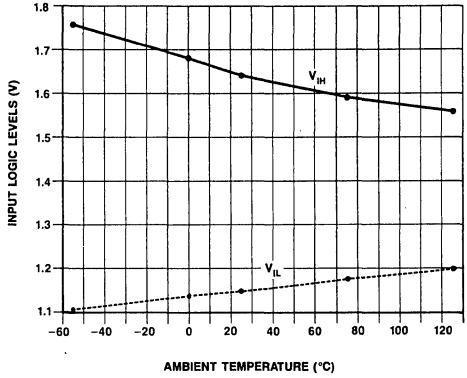
NORMALIZED CHIP ENABLE ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



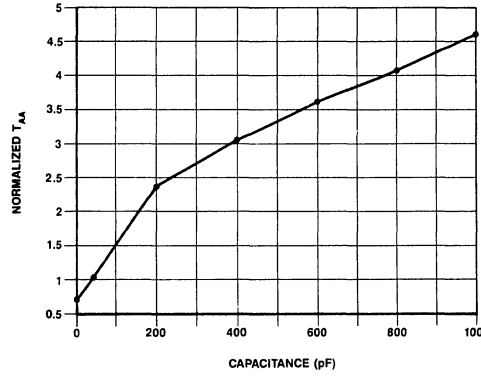
LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A=25°C



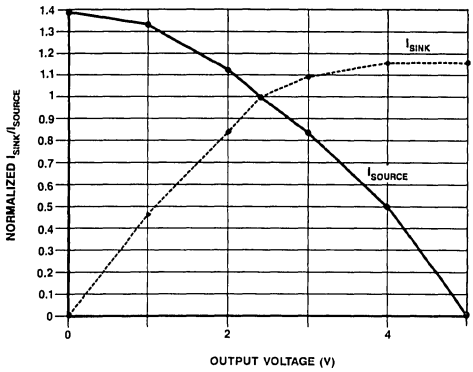
LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



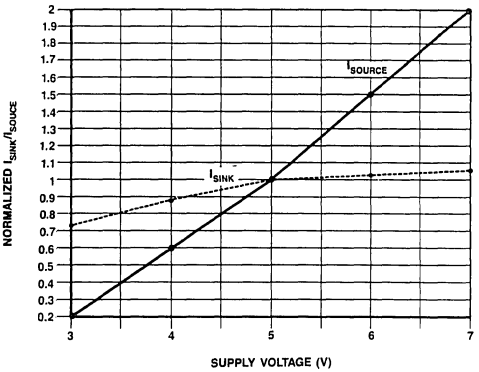
NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC}=5.0 V T_A=25°C



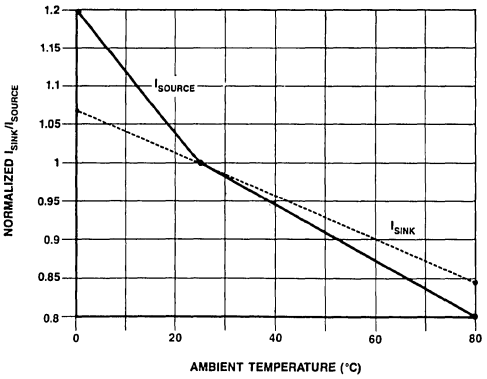
NORMALIZED SOURCE AND SINK CURRENTS VS. OUTPUT VOLTAGE VOLTAGE V_{CC}=5.0V T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS. SUPPLY VOLTAGE T_A=25°C

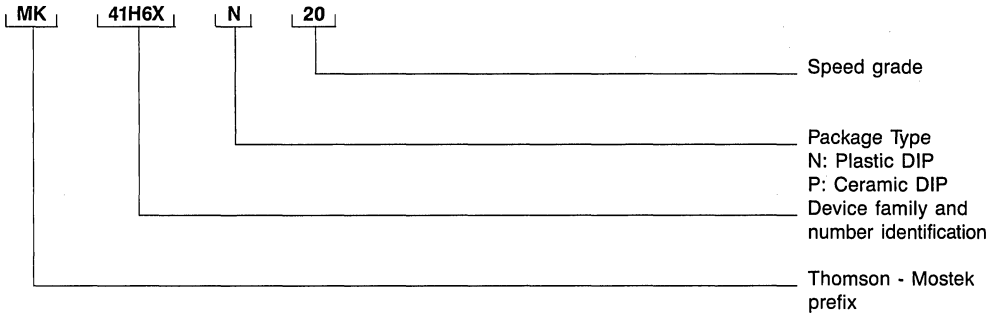


NORMALIZED SOURCE AND SINK CURRENTS VS. AMBIENT TEMPERATURE V_{CC}=5.0V

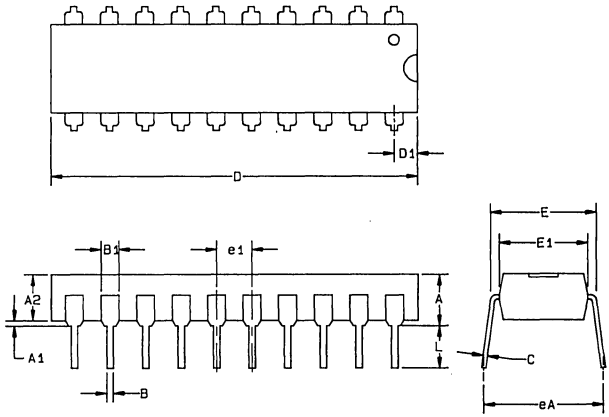


ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H67N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H67N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H67N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H66N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H66N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H66N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H67P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H67P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H67P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H66P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H66P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H66P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C



20 PIN "N" PACKAGE
PLASTIC DIP

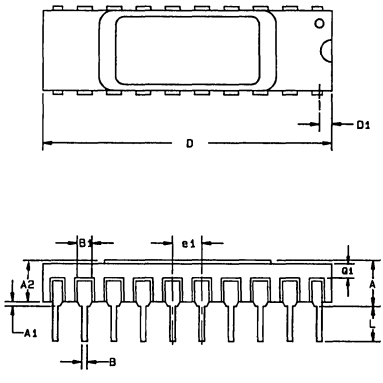


DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

20 PIN "P" PACKAGE
SIDE BRAZED CERAMIC DIP



DIM	INCHES		NOTES
	MIN	MAX	
A	–	.175	1
A1	.020	–	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	.965	.995	
D1	.025	.055	
E	.295	.325	
E1	.280	.310	
e1	.090	.110	
eA	.290	.365	
L	.120	–	
Q1	.005	–	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

MK41L66/MK41L67(N,P)-25/35/45

16K x 1 CMOS STATIC RAM

PRELIMINARY

MEMORY COMPONENTS

FEATURES

- ☐ JEDEC LVTTL standard +3.3 volt operation
- ☐ 25, 35 and 45 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 20-pin, 300 mil Plastic and Ceramic DIP
- ☐ All input and output pins TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 μA CMOS Standby Current (MK41L67)
- ☐ High speed chip select (MK41L66)
- ☐ JEDEC standard pinout

MK41L66 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	Mode	Q	Power
H	X	Deselect	High Z	Active
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

MK41L67 TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Q	Power
H	X	Deselect	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

X = Don't Care

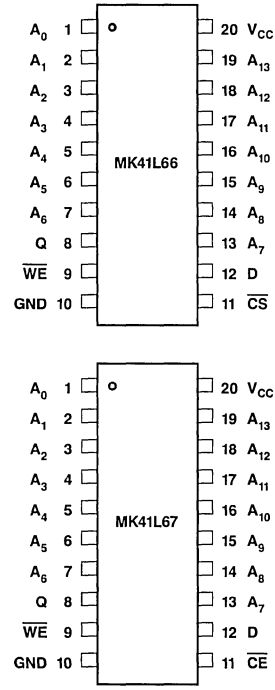


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{13} - Address	$\overline{WE}$ - Write Enable
$\overline{CE}$ - Chip Enable (MK41L67)	GND - Ground
$\overline{CS}$ - Chip Select (MK41L66)	V_{CC} - + 3.3 volts
	D - Data In
	Q - Data Out

DESCRIPTION

The MK41L66 and MK41L67, together with their by 4 counterparts, the MK41L68 and MK41L69, are the first devices on the market that meet or exceed the JEDEC standard for LVTTL VLSI digital circuits. The LVTTL standard provides for compatability between +5.0 ±0.5 volt TTL devices and +3.3 ±0.3 volt LVTTL devices within the same system. Adoption of a lower power supply voltage standard allows dimensional scaling of silicon die to continue, which in turn allows density and performance increases to continue. Scaling down the supply voltage provides a number of other potential benefits including reduced EMI, RFI, power consumption and increased reliability.

The MK41L66 and MK41L67 feature fully static operation requiring no external clocks or timing strobes, and

equal address access and cycle times.The MK41L67 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

The MK41L66 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

OPERATIONS

READ MODE

The MK41L66/7 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}/\overline{CS}$ (Chip Enable/Select) is low, providing a ripple-through access to any one of 16,384 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}/\overline{CS}$ access time is satisfied. If $\overline{CE}/\overline{CS}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the Data Output pin is controlled by the $\overline{CE}/\overline{CS}$, and $\overline{WE}$ control signals. The Q may be in an indeterminate state at t_{CL}, but the Q will always have valid data at t_{AA}.

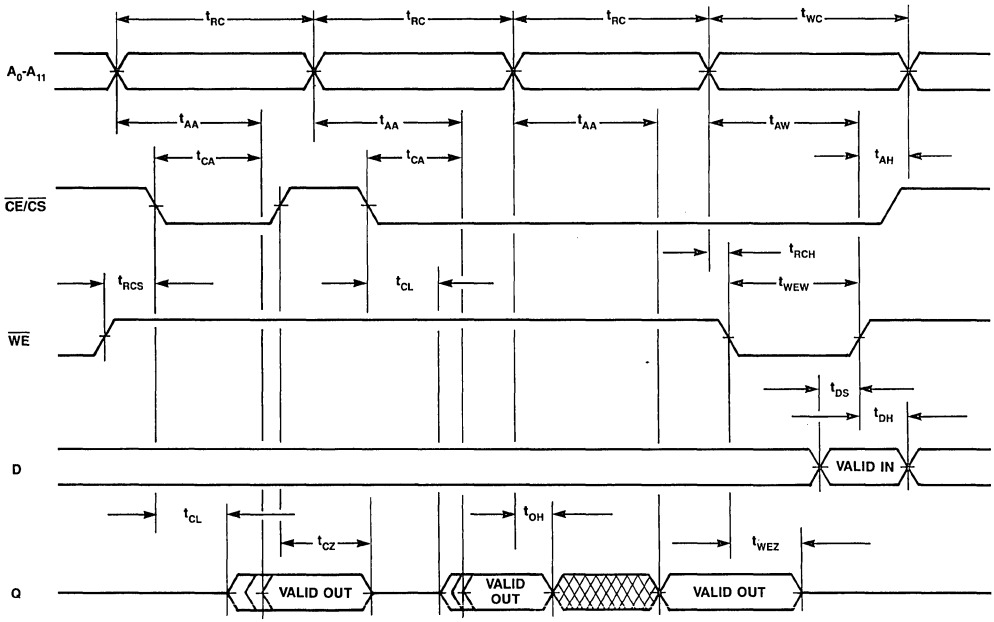


Figure 2. Read-Read-Read-Write Timing

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 3.3 V ± 0.3 V)

		MK41L6X-25		MK41L6X-35		MK41L6X-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	25		35		45		ns	
t_{AA}	Address Access Time		25		35		45	ns	1
t_{CL}	Chip Enable to Low-Z (MK41L67)	7		7		7		ns	2
t_{CL}	Chip Select to Low-Z (MK41L66)	5		5		5		ns	2
t_{CA}	Chip Enable Access Time (MK41L67)		25		35		45	ns	1
t_{CA}	Chip Select Access Time (MK41L66)		12		15		17	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41L67)		10		13		17	ns	2
t_{CZ}	Chip Select to High-Z (MK41L66)		8		10		12	ns	2
t_{WEZ}	Write Enable to High-Z		10		13		17	ns	2
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

WRITE MODE

The MK41L66/7 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}/\overline{CS}$ inputs are in the low state. $\overline{CE}/\overline{CS}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}/\overline{CS}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}/\overline{CS}$, or $\overline{WE}$.

If the output is enabled ($\overline{CE}/\overline{CS}$ is low), then $\overline{WE}$ will return the output to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}/\overline{CS}$ or $\overline{WE}$.

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C≤T_A≤70°C) (V_{CC} = 3.3 V ± 0.3 V)

		MK41L6X-25		MK41L6X-35		MK41L6X-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	25		35		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	20		30		40		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	22		32		40		ns	
t_{WEW}	Write Enable to End of Write	20		30		40		ns	
t_{DS}	Data Setup Time	14		15		18		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

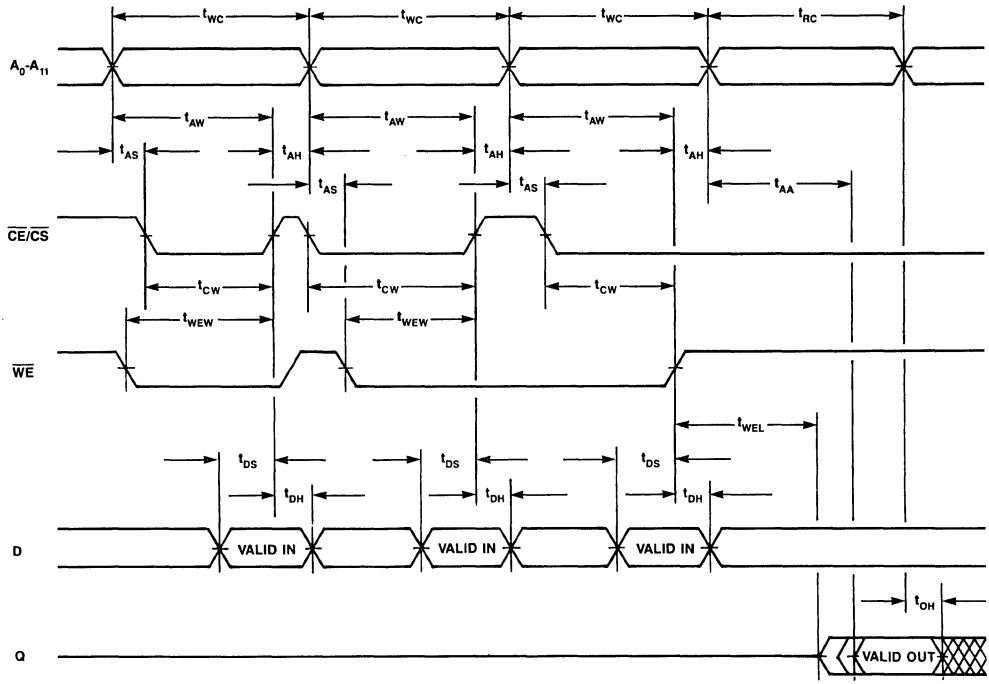


Figure 3. Write-Write-Write-Read Timing

LOW V_{CC} DATA RETENTION TIMING (MK41L67)

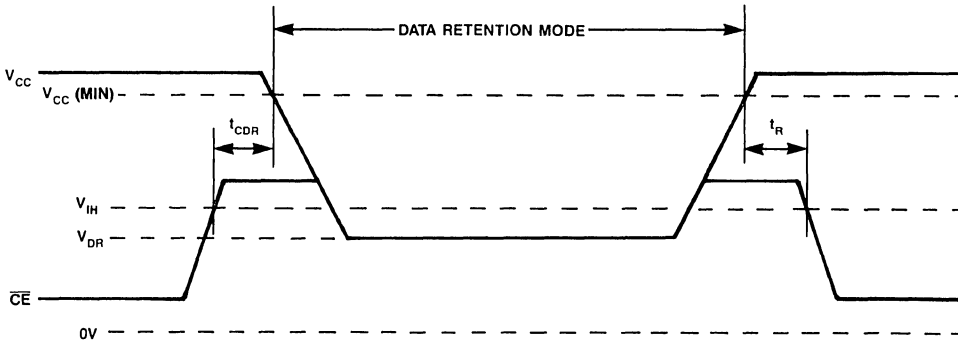


Figure 4. Data Retention Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41L67 Only)

The MK41L67 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

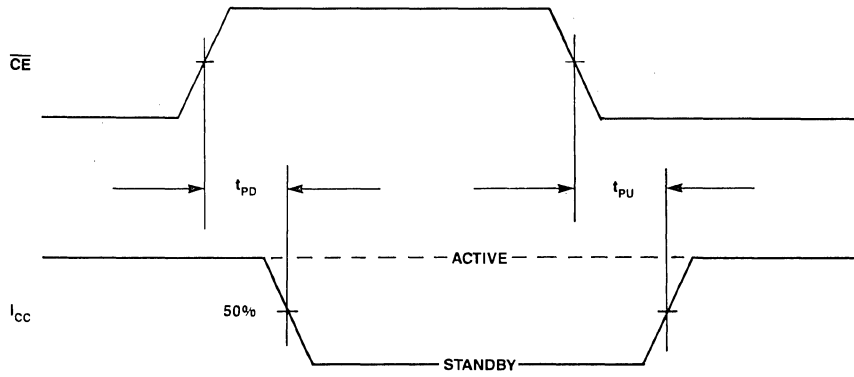


Figure 5. Standby Mode Timing

STANDBY MODE
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 3.3 V ± 0.3 V)

		MK41L67-25		MK41L67-35		MK41L67-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		25		35		45	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41L66/7 operates from a 3.3 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly 5 volt TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41L66/7 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41L66/7, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +6.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.0		V_{CC}+1.2	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−1.0		0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		60	mA	5
I_{CC2}	TTL Standby Current (MK41L67 only)		8	mA	6
I_{CC3}	CMOS Standby Current (MK41L67 only)		50	µA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	µA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	µA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −1 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +4 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

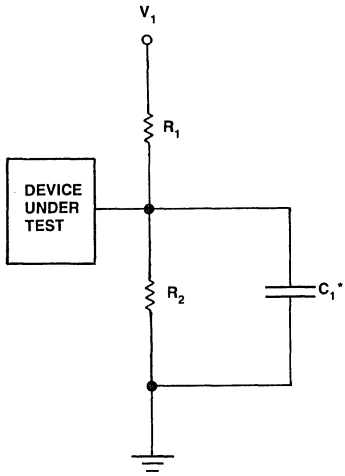
SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on Q pin	8	10	pF	6,10

NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. t cycle = min. duty cycle 100%.
6. $\overline{CE} = V_{IH}$, All Other Inputs = Don't Care.
7. V_{CC} (max) $\geq \overline{CE} \geq V_{CC}$ − 0.3 V
   GND + 0.3 V $\geq A_0$-$A_{13} \geq V_{IL}$ (min) or V_{IH} (max) $\geq A_0$-$A_{13} \geq V_{CC}$ −0.3 V.
   All Other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that $0 V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
9. Output leakage current specifications are valid for all V_{OUT} such that $0 V < V_{OUT} < V_{CC}$, $\overline{CE/CS} = V_{IH}$ and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	3.3 V ± 0.3 V



LOAD CIRCUIT VALUES

V_1	5.0 V	3.3 V
R_1	1000Ω	660Ω
R_2	670Ω	1016Ω
C_1	30 pF	30 pF

* INCLUDES SCOPE AND TEST JIG

EQUIVALENT TO:

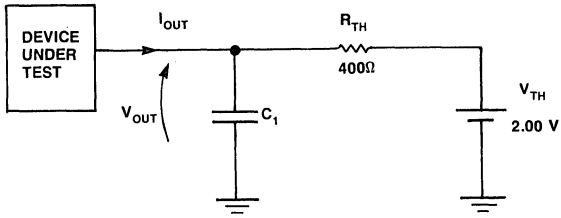
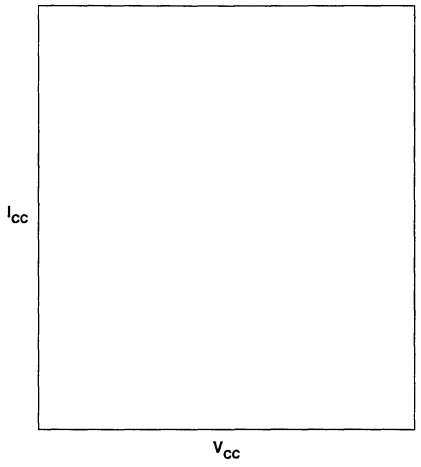
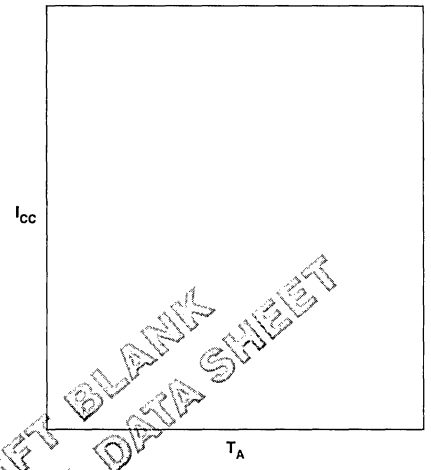


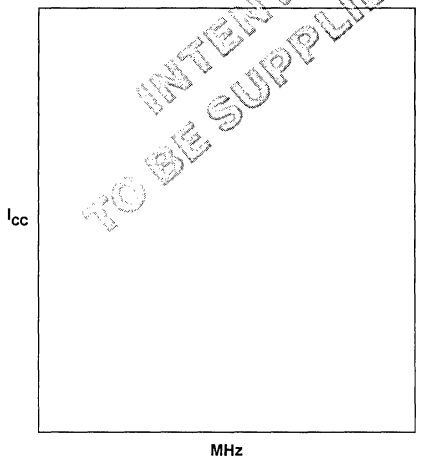
Figure 6. Output Load Circuits



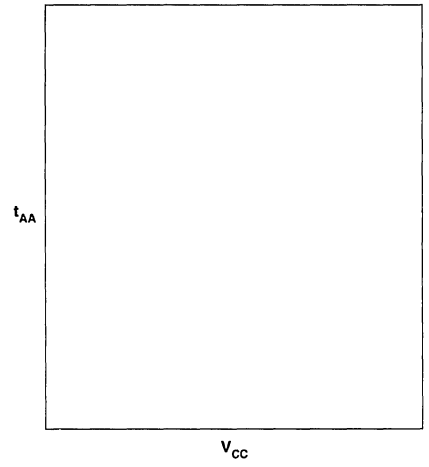
Normalized Supply Current vs. Supply Voltage



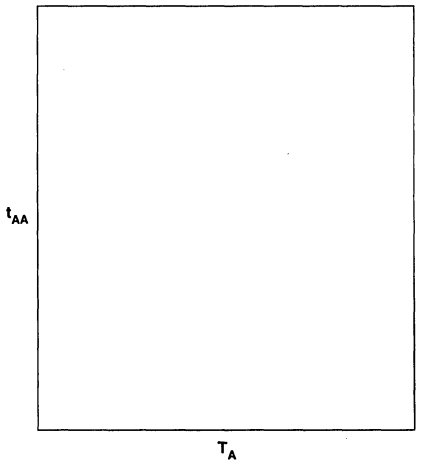
Normalized Supply Current vs. Ambient Temperature



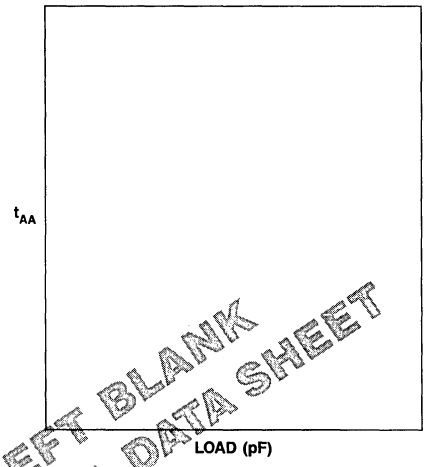
Normalized Supply Current vs. Cycle Time



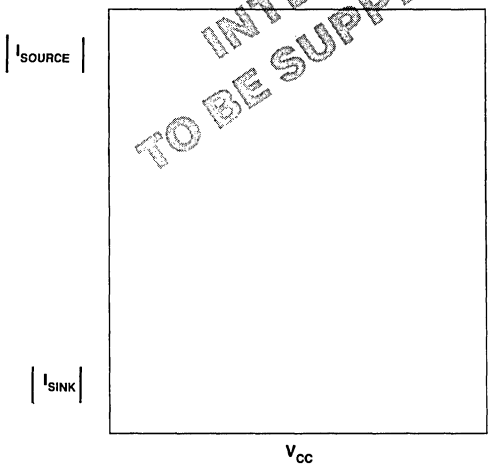
Normalized Address Access Time vs. Supply Voltage



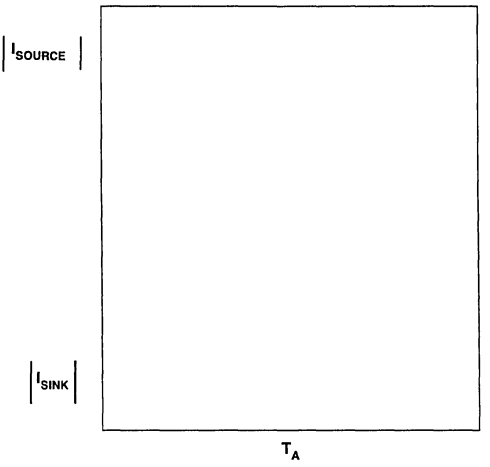
Normalized Address Access Time vs. Ambient Temperature



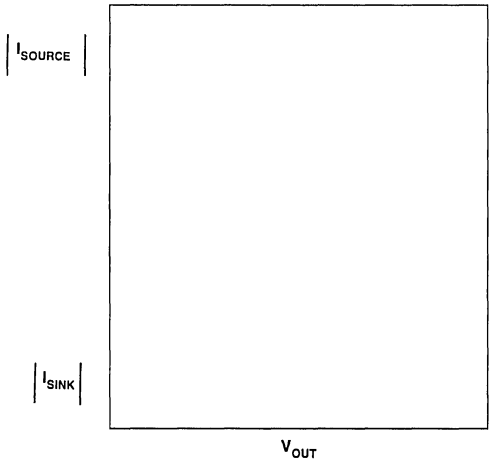
Normalized Address Access Time vs. Output Loading



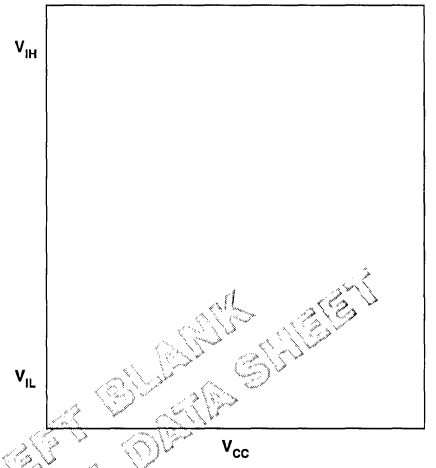
Normalized Output Source and Sink Currents vs. Supply Voltage



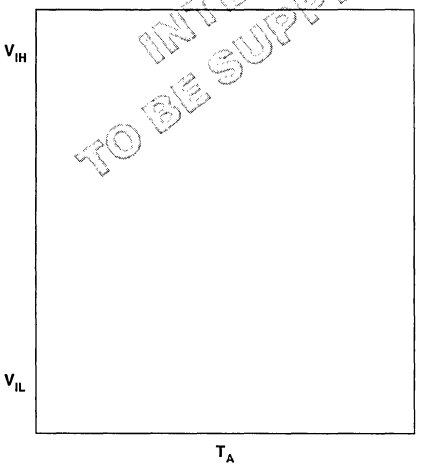
Normalized Output Source and Sink Currents vs. Ambient Temperature



Normalized Output Source and Sink Currents vs. Output Voltage



Logic Thresholds vs. Supply Voltage

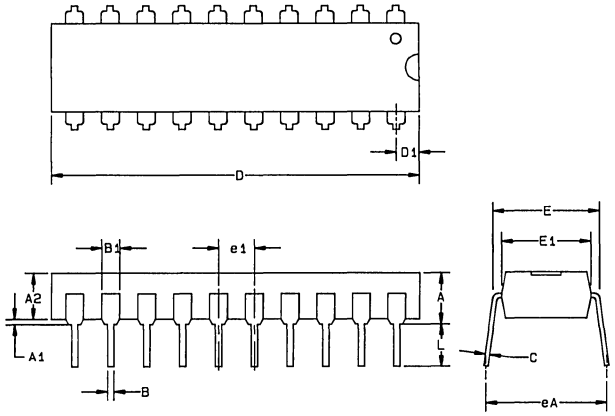


Logic Thresholds vs. Ambient Temperature

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41L66N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41L66N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41L66N-45	45 ns	20 pin Plastic DIP	0°C to 70°C
MK41L67N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41L67N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41L67N-45	45 ns	20 pin Plastic DIP	0°C to 70°C
MK41L66P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L66P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L66P-45	45 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L67P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L67P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L67P-45	45 ns	20 pin Ceramic DIP	0°C to 70°C

20 PIN "N" PACKAGE
PLASTIC DIP

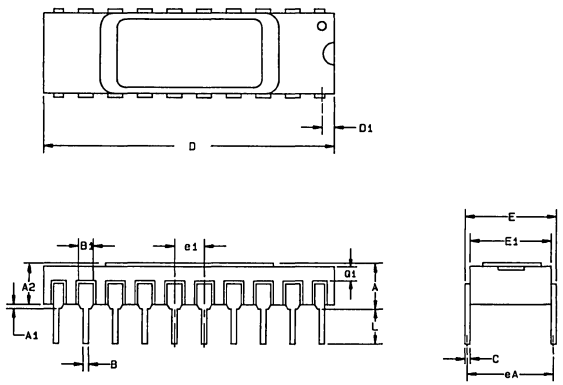


DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

20 PIN "P" PACKAGE
SIDE BRAZED CERAMIC DIP



DIM	INCHES		NOTES
	MIN	MAX	
A	–	.175	1
A1	.020	–	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	.965	.995	
D1	.025	.055	
E	.295	.325	
E1	.280	.310	
e1	.090	.110	
eA	.290	.365	
L	.120	–	
Q1	.005	–	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

MK41H68/MK41H69(N,P)-20/25/35

4K × 4 CMOS STATIC RAM

MEMORY COMPONENTS

FEATURES

- ☐ 20, 25, and 35 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 20-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 μA CMOS Standby Current (MK41H68)
- ☐ TTL Standby Current unaffected by address activity (MK41H68)
- ☐ High speed chip select (MK41H69)
- ☐ JEDEC standard pinout

MK41H68 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

MK41H69 TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Active
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

X = Don't Care

DESCRIPTION

The MK41H68 and MK41H69 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single +5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H68 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full V_{CC} voltage.

The MK41H69 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

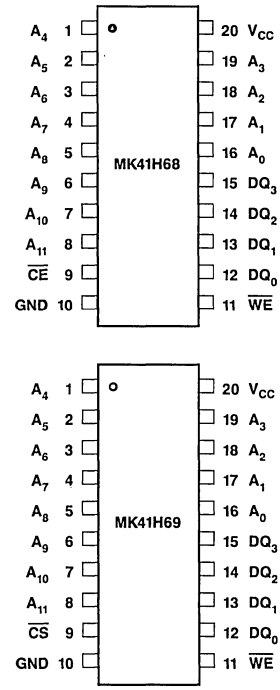


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{11} - Address	$\overline{WE}$ - Write Enable
DQ_0 - DQ_3 - Data I/O	GND - Ground
$\overline{CE}$ - Chip Enable (MK41H68)	V_{CC} - + 5 volts
$\overline{CS}$ - Chip Select (MK41H69)	

OPERATIONS

READ MODE

The MK41H68/9 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}/\overline{CS}$ (Chip Enable/Select) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}/\overline{CS}$ access time is satisfied. If $\overline{CE}/\overline{CS}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}/\overline{CS}$, and $\overline{WE}$ control signals. The data lines may be in an indeterminate state at t_{CL}, but the data lines will always have valid data at t_{AA}.

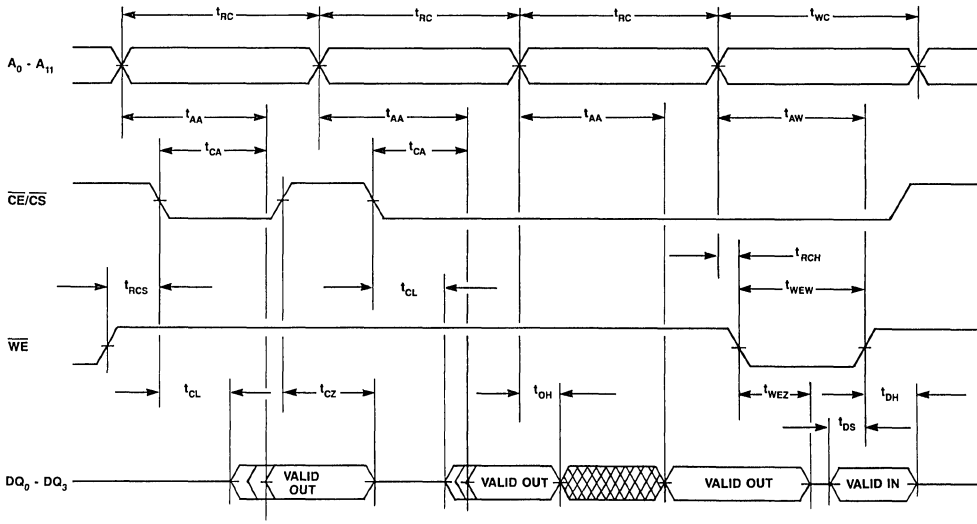


Figure 2. Read-Read-Read-Write Timing

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H6X-20		MK41H6X-25		MK41H6X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CL}	Chip Enable to Low-Z (MK41H68)	7		7		7		ns	2
t_{CL}	Chip Select to Low-Z (MK41H69)	5		5		5		ns	2
t_{CA}	Chip Enable Access Time (MK41H68)		20		25		35	ns	1
t_{CA}	Chip Select Access Time (MK41H69)		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41H68)		8		10		13	ns	2
t_{CZ}	Chip Select to High-Z (MK41H69)		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H68/9 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}/\overline{CS}$ inputs are in the low state. $\overline{CE}/\overline{CS}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}/\overline{CS}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}/\overline{CS}$, or $\overline{WE}$.

If the output is enabled ($\overline{CE}/\overline{CS}$ is low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}/\overline{CS}$ or $\overline{WE}$.

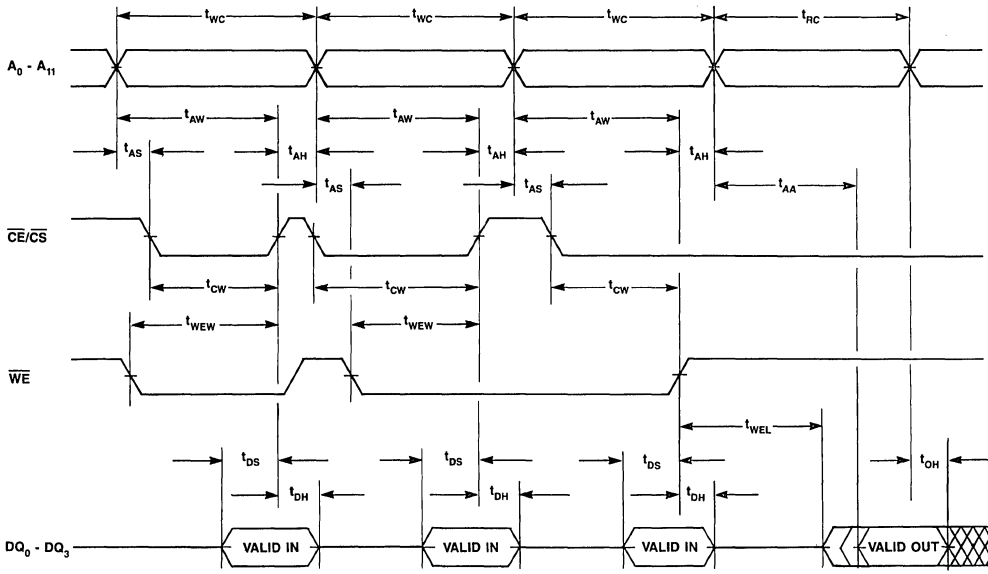


Figure 3. Write-Write-Write-Read Timing

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H6X-20		MK41H6X-25		MK41H6X-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

LOW V_{CC} DATA RETENTION TIMING (MK41H68)

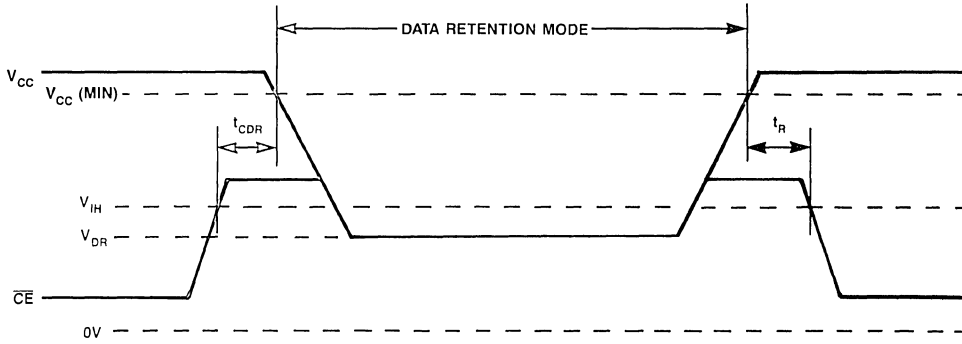


Figure 4. Data Retention Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	µA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41H68 Only)

The MK41H68 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

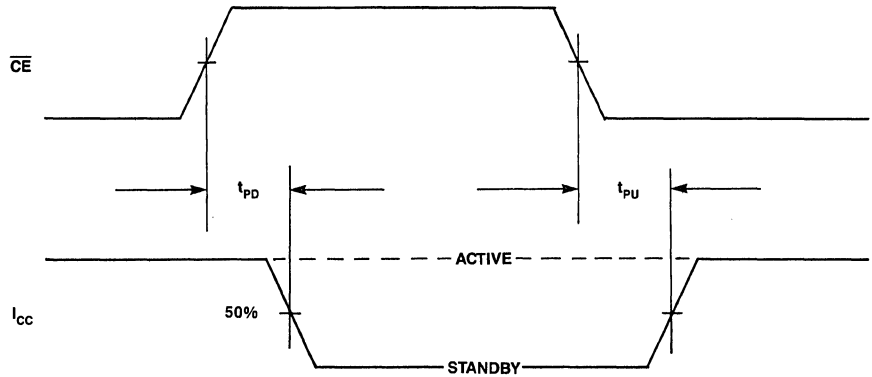


Figure 5. Standby Mode Timing

STANDBY MODE
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H68-20		MK41H68-25		MK41H68-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H68/9 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H68/9 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H68/9, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−1.0		0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	5
I_{CC2}	TTL Standby Current (MK41H68 only)		8	mA	6
I_{CC3}	CMOS Standby Current (MK41H68 only)		50	μA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on DQ pins	8	10	pF	6,10

NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
6. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
7. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V, All Other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that $0 V < V_{IN} < V_{CC}$. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that $0 V < V_{OUT} < V_{CC}$, $\overline{CE}/\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

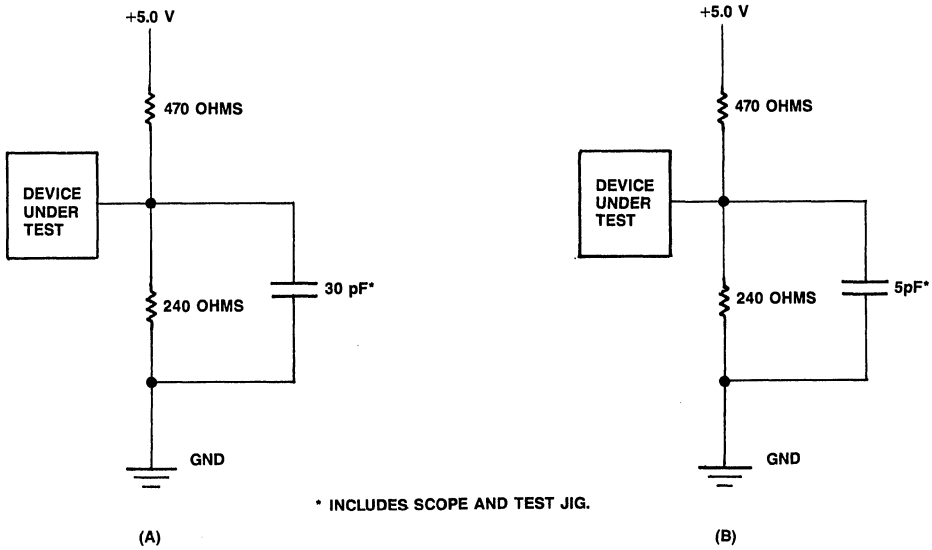
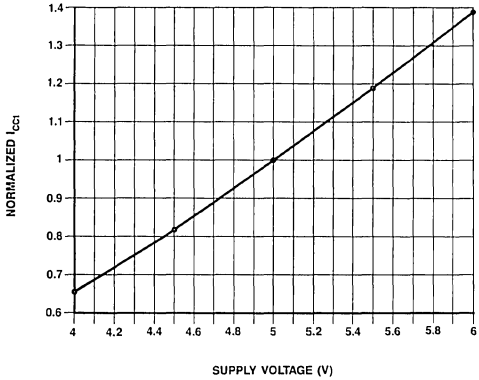


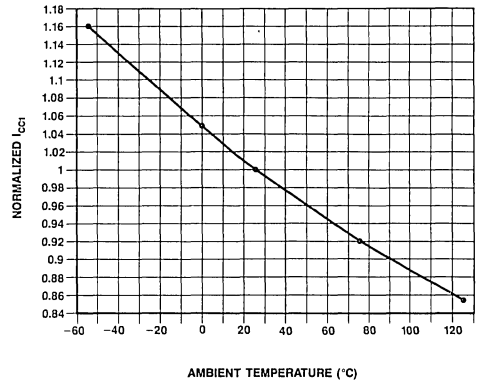
Figure 6. Output Load Circuits

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

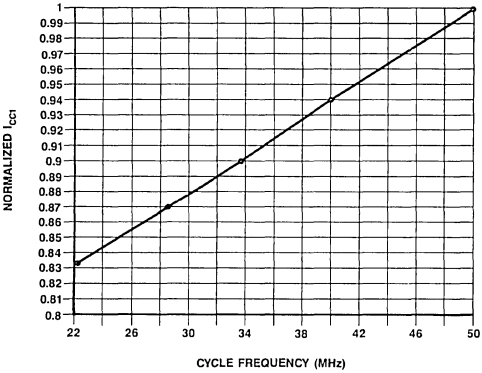
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE T_A=0°C



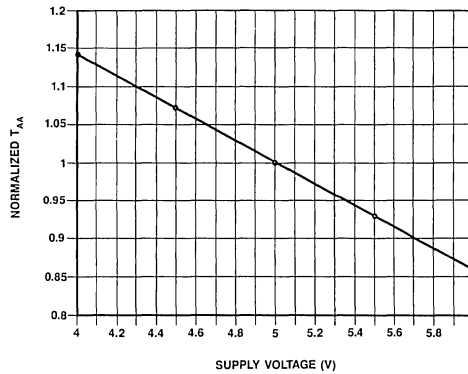
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



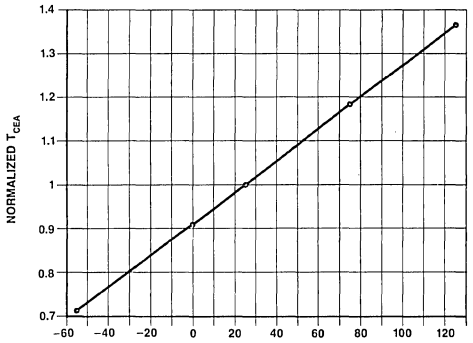
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC}=5.0V T_A=25°C



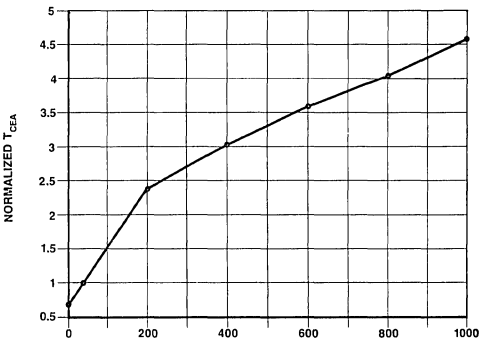
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A=25°C



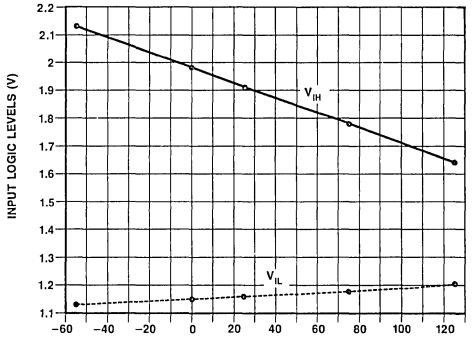
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



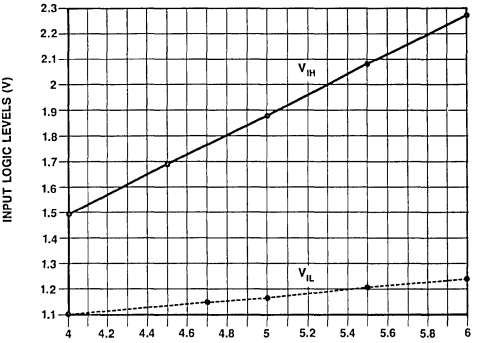
NORMALIZED ACCESS TIME VS.
OUTPUT LOADING V_{CC}=5.0V T_A=25°C



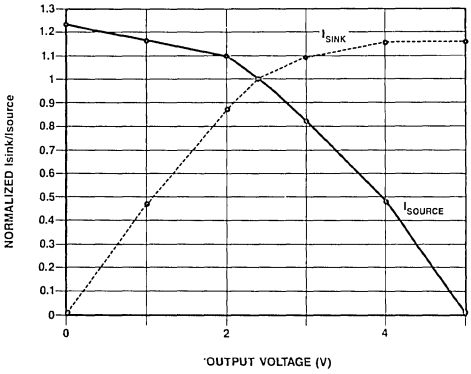
LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



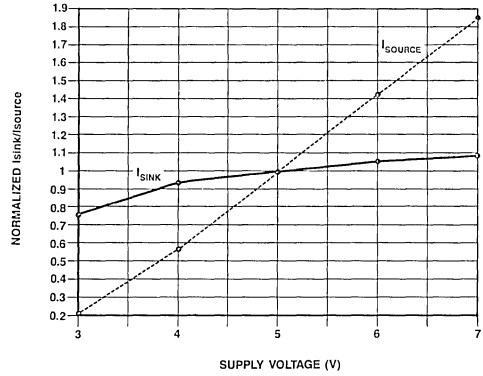
LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A=25°C



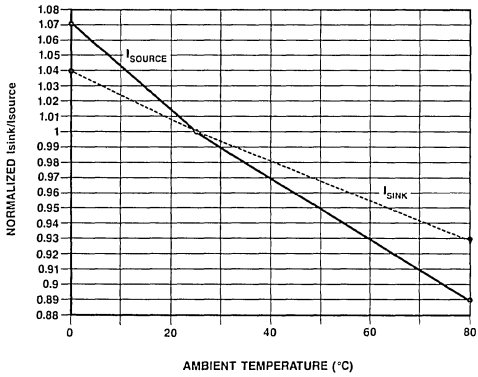
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC}=5.0V T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A=25°C

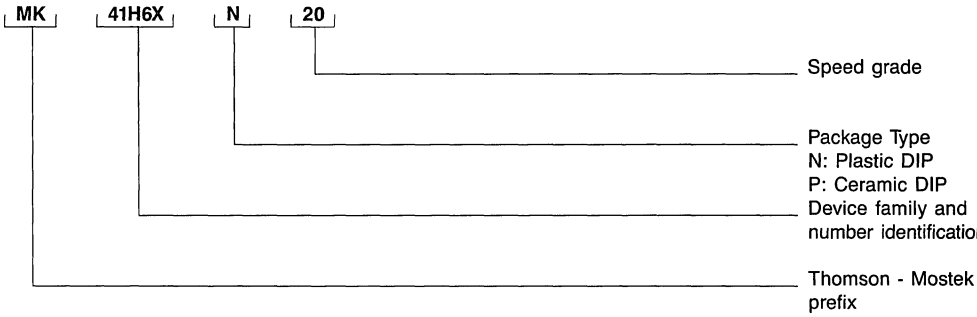


NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC}=5.0V

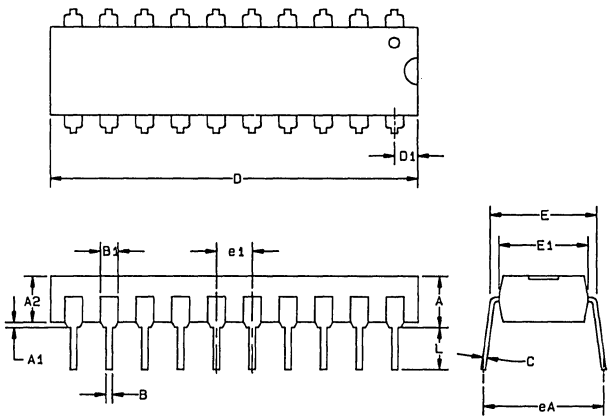


ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H68N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H68N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H68N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H69N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H69N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H69N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H68P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H68P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H68P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H69P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H69P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H69P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C



20 PIN "N" PACKAGE
PLASTIC DIP

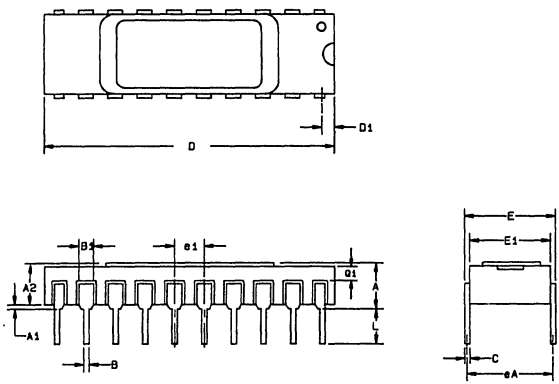


DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

20 PIN "P" PACKAGE
SIDE BRAZED CERAMIC DIP



DIM	INCHES		NOTES
	MIN	MAX	
A	–	.175	1
A1	.020	–	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	.965	.995	
D1	.025	.055	
E	.295	.325	
E1	.280	.310	
e1	.090	.110	
eA	.290	.365	
L	.120	–	
Q1	.005	–	

NOTES

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MK41L68/MK41L69(N,P)-25/35/45

4K x 4 CMOS STATIC RAM

PRELIMINARY

MEMORY COMPONENTS

FEATURES

- ☐ JEDEC LVTTL Standard +3.3 volt operation
- ☐ 25, 35 and 45 ns Address Access Time
- ☐ Automatic Power-up Clear
- ☐ Equal access and cycle times
- ☐ 20-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 μA CMOS Standby Current (MK41L68)
- ☐ TTL Standby unaffected by address activity (MK41L68)
- ☐ High speed chip select (MK41L69)
- ☐ JEDEC standard pinout

MK41L68 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

MK41L69 TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Active
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

X = Don't Care

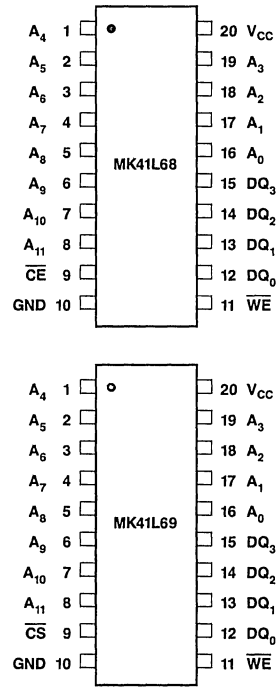


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{11} - Address	$\overline{WE}$ - Write Enable
DQ_0 - DQ_3 - Data I/O	GND - Ground
$\overline{CE}$ - Chip Enable (MK41L68)	V_{CC} - + 3.3 volts
$\overline{CS}$ - Chip Select (MK41L69)	

DESCRIPTION

The Mostek MK41L68 and MK41L69, together with their 22 pin derivatives, the MK41L78 and MK41L79, are the first devices on the market that meet or exceed the JEDEC Standard for LVTTL VLSI digital circuits. The LVTTL standard provides for compatability between +5.0 ± 0.5 volt TTL devices and +3.3 ± 0.3 volt LVTTL devices within the same system. Adoption of a lower power supply voltage standard allows dimensional scaling of silicon die to continue, which in turn allows density and performance increases to continue. Scaling

down the supply voltage provides a number of other potential benefits including reduced EMI, RFI, power comsumption and increased reliability.

The MK41L68 and MK41L69 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The MK41L68 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full V_{CC} voltage. The MK41L69 Chip Select pin provides a high speed chip select access, allowing fast read cycles to be achieved despite decoder delays.

OPERATIONS

READ MODE

The MK41L68/9 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and CE/CS (Chip Enable/Select) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}/\overline{CS}$ access time is satisfied. If $\overline{CE}/\overline{CS}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}/\overline{CS}$ and $\overline{WE}$ control signals. The data lines may be in an indeterminate state at t_{CL}, but the data lines will always have valid data at t_{AA}.

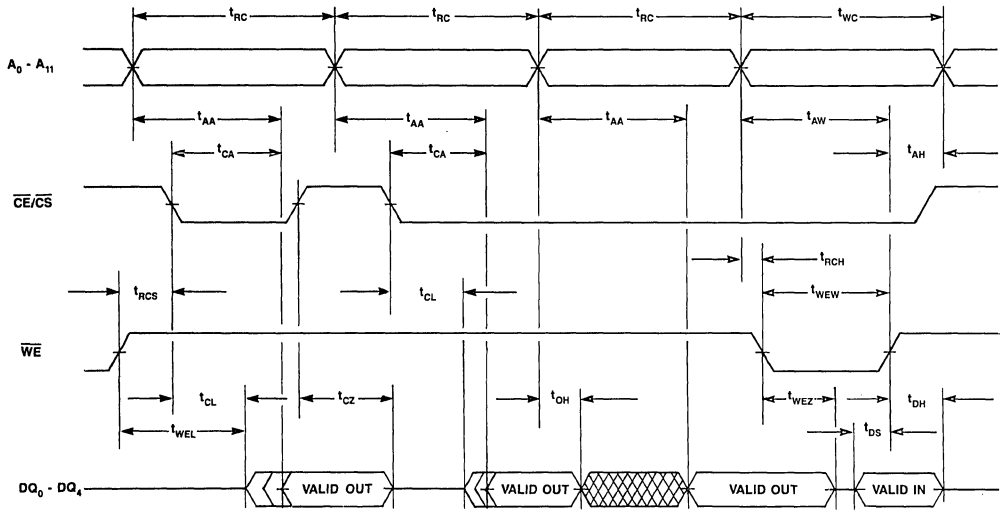


Figure 2. Read-Read-Read-Write Timing

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 3.3 ± 0.3 V)

		MK41L6X-25		MK41L6X-35		MK41L6X-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	25		35		45		ns	
t_{AA}	Address Access Time		25		35		45	ns	1
t_{CL}	Chip Enable to Low-Z (MK41L68)	7		7		7		ns	2
t_{CL}	Chip Select to Low-Z (MK41L69)	5		5		5		ns	2
t_{CA}	Chip Enable Access Time (MK41L68)		25		35		45	ns	1
t_{CA}	Chip Select Access Time (MK41L69)		12		15		18	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41L68)		10		13		17	ns	2
t_{CZ}	Chip Select to High-Z (MK41L69)		8		10		12	ns	2
t_{WEZ}	Write Enable to High-Z		10		13		17	ns	2
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

WRITE MODE

The MK41L68/9 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}/\overline{CS}$ inputs are in the low state. $\overline{CE}/\overline{CS}$, or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}/\overline{CS}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}/\overline{CS}$, or $\overline{WE}$. The write cycle is terminated by the earlier rising edge of CE/CS, or $\overline{WE}$.

If the output is enabled ($\overline{CE}/\overline{CS}$ is low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}/\overline{CS}$ or $\overline{WE}$.

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C≤T_A≤70°C) (V_{CC} = 3.3 ± 0.3 V)

		MK41L6X-25		MK41L6X-35		MK41L6X-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	25		35		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write	20		30		40		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	22		32		40		ns	
t_{WEW}	Write Enable to End of Write	20		30		40		ns	
t_{DS}	Data Setup Time	14		15		18		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

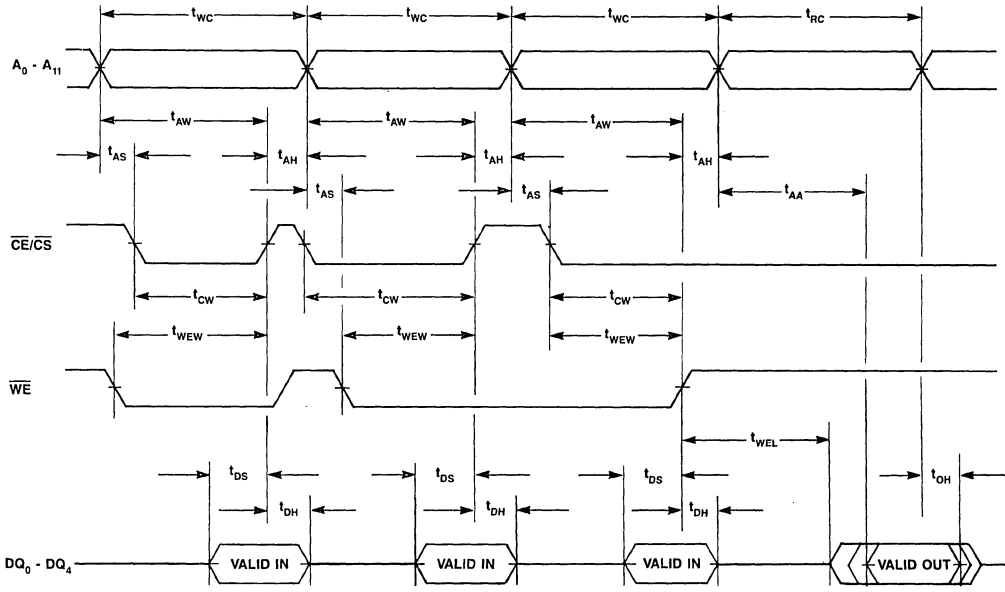


Figure 3. Write-Write-Write-Read Timing

LOW V_{CC} DATA RETENTION TIMING (MK41L68)

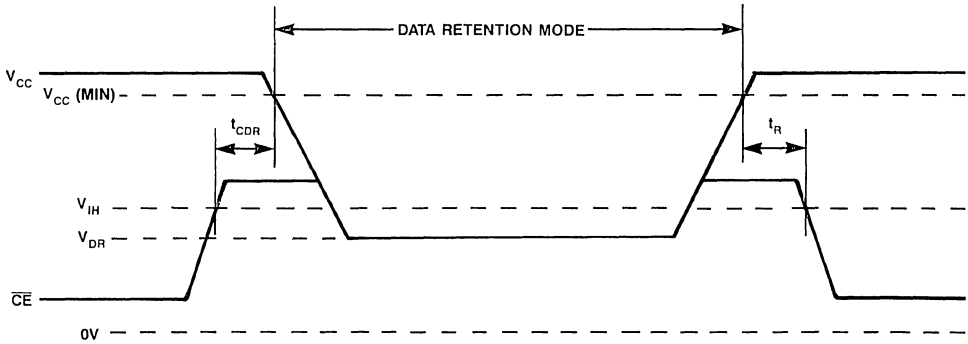


Figure 4. Data Retention Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41L68 Only)

The MK41L68 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

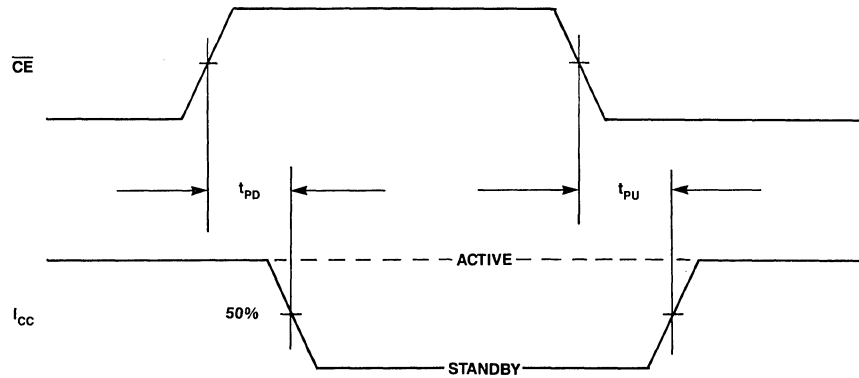


Figure 5. Standby Mode Timing

STANDBY MODE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 3.3 ± 0.3 V)

		MK41L68-25		MK41L68-35		MK41L68-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		25		35		45	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41L68/9 operates from a 3.3 volt supply. It is compatible with all standard TTL families. The device should share a solid ground plane with any other devices interfaced with it, particularly 5 volt TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK41L68/69 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41L68/9, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +6.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.0		V_{CC}+1.2	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−1.0		0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 3.3 ± 0.3 V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		60	mA	5
I_{CC2}	TTL Standby Current (MK41L68 only)		8	mA	6
I_{CC3}	CMOS Standby Current (MK41L68 only)		50	μA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −1 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +4 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

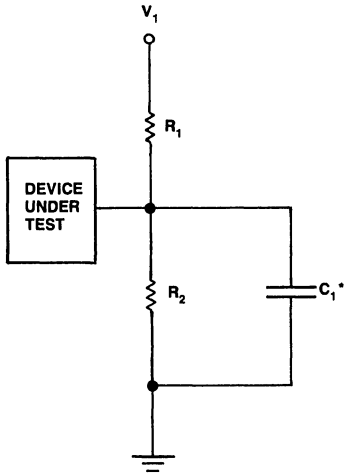
SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on DQ pins	8	10	pF	6,10

NOTES

1. Measured with load shown in Figure 6.
2. Measured with load shown in Figure 6, C_1 = 5 pF.
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t cycle = min. duty cycle 100%.
6. CE = V_{IH}, all other inputs = Don't Care.
7. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V. All other inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}$/$\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	3.3 ± 0.3 V



LOAD CIRCUIT VALUES

V_1	5.0 V	3.3 V
R_1	1000Ω	660Ω
R_2	670Ω	1016Ω
C_1	30 pF	30pF

* INCLUDES SCOPE AND TEST JIG

EQUIVALENT TO:

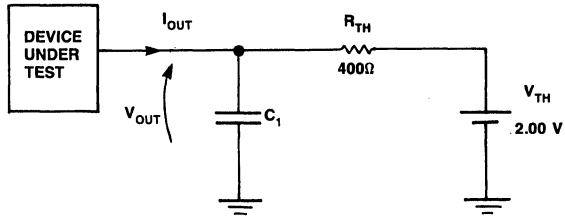
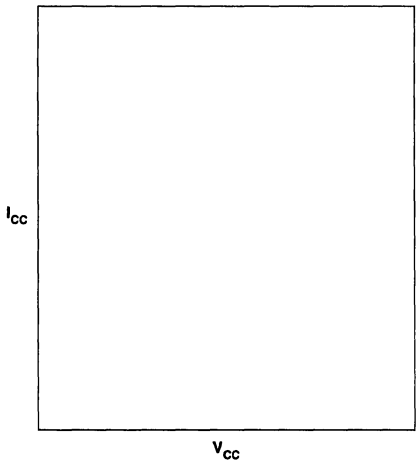
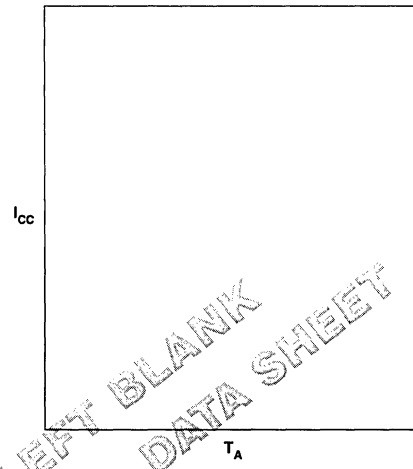


Figure 6. Output Load Circuits

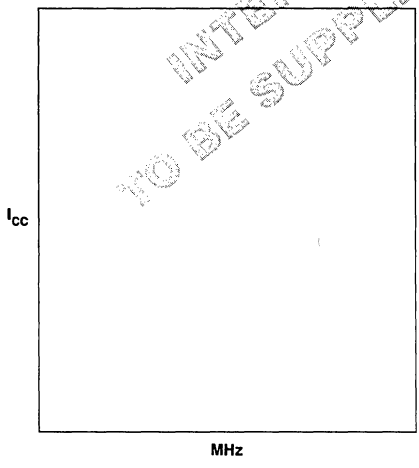
NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS



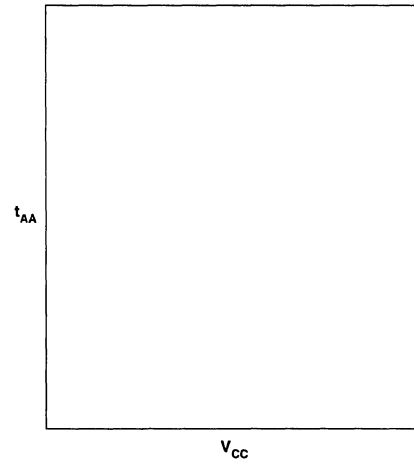
Normalized Supply Current vs. Supply Voltage



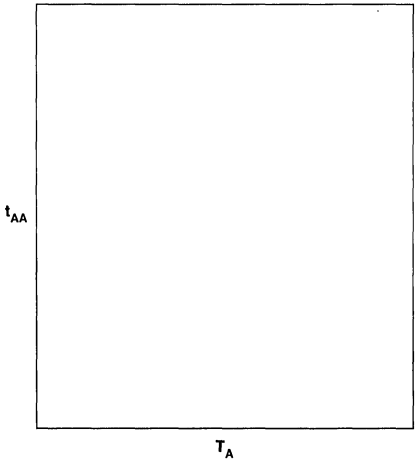
Normalized Supply Current vs. Ambient Temperature



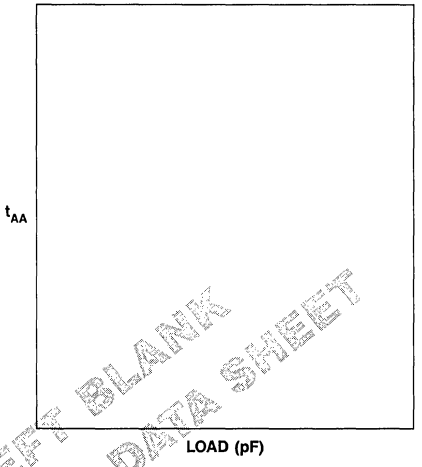
Normalized Supply Current vs. Cycle Time



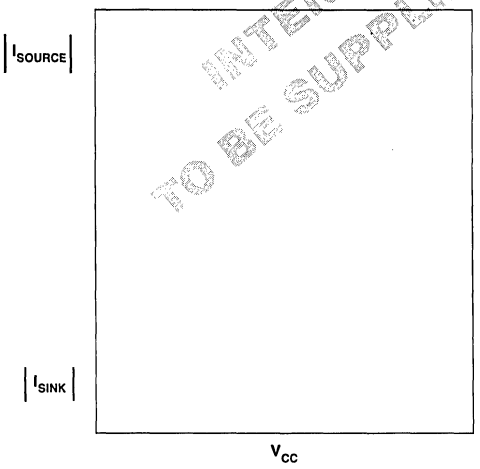
Normalized Address Access Time vs. Supply Voltage



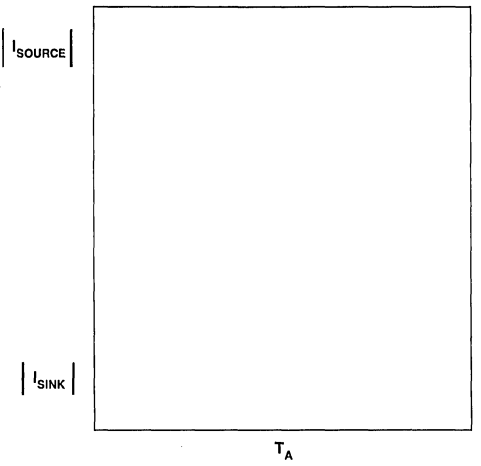
Normalized Address Access Time vs. Ambient Temperature



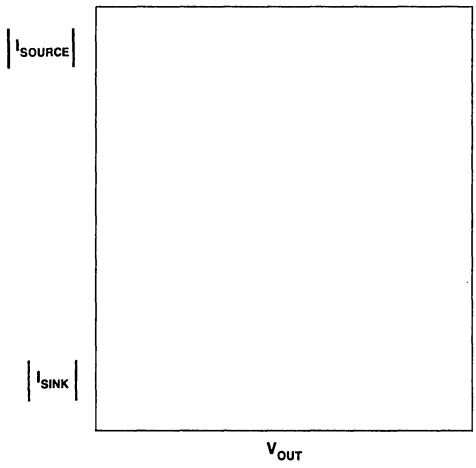
Normalized Address Access Time vs. Output Loading



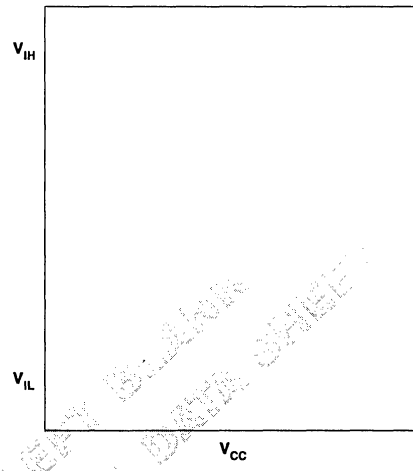
Normalized Output Source and Sink Currents vs. Supply Voltage



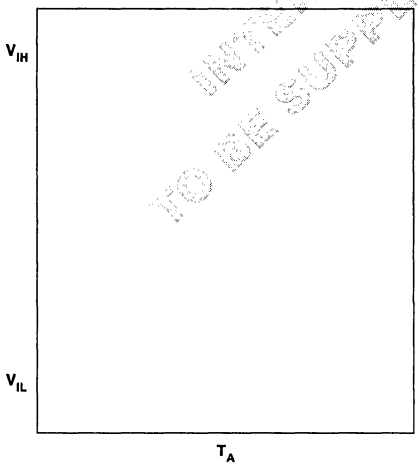
Normalized Output Source and Sink Currents vs. Ambient Temperature



Normalized Output Source and Sink Currents vs. Output Voltage



Logic Thresholds vs. Supply Voltage

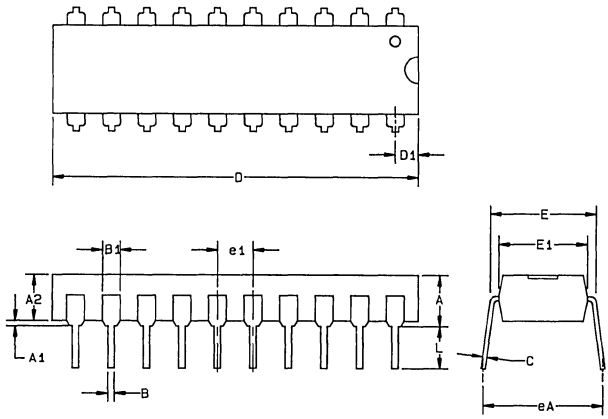


Logic Thresholds vs. Ambient Temperature

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41L68N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41L68N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41L68N-45	45 ns	20 pin Plastic DIP	0°C to 70°C
MK41L69N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41L69N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41L69N-45	45 ns	20 pin Plastic DIP	0°C to 70°C
MK41L68P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L68P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L68P-45	45 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L69P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L69P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41L69P-45	45 ns	20 pin Ceramic DIP	0°C to 70°C

20 PIN "N" PACKAGE
PLASTIC DIP



DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
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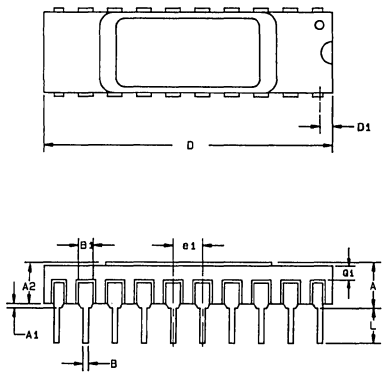
20 PIN "P" PACKAGE
SIDE BRAZED CERAMIC DIP



DIM	INCHES		NOTES
	MIN	MAX	
A	–	.175	1
A1	.020	–	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	.965	.995	
D1	.025	.055	
E	.295	.325	
E1	.280	.310	
e1	.090	.110	
eA	.290	.365	
L	.120	–	
Q1	.005	–	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

MK41H78/79(N,P)-20/25/35

4K × 4 CMOS STATIC RAM

FEATURES

- ☐ 20, 25, and 35 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 22-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 μA CMOS Standby Current
- ☐ TTL Standby Current unaffected by address activity
- ☐ Separate Output Enable control
- ☐ Flash Clear Function (MK41H79)

TRUTH TABLE

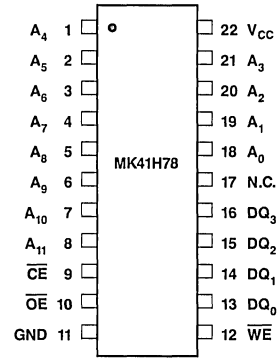
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	*$\overline{CLR}$	Mode	DQ	Power
H	X	X	X	Deselect	High Z	Standby
L	X	L	H	Write	D_{IN}	Active
L	L	H	H	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active
L	X	L	L	Flash Clear	High Z	Active
L	L	H	L	Flash Clear	Low Z	Active
L	H	H	L	Flash Clear	High Z	Active

* - Applies to MK41L79 only. X = Don't Care

DESCRIPTION

The MK41H78/79 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. It requires a single +5V ± 10 percent power supply and is fully TTL compatible.

The device has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full V_{CC} voltage. An Output Enable ($\overline{OE}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus.



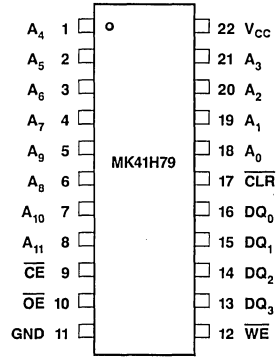


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{11} - Address	$\overline{OE}$ - Output Enable
DQ_0 - DQ_3 - Data I/O	$\overline{WE}$ - Write Enable
N.C. - No Connect	GND - Ground
$\overline{CE}$ - Chip Enable	V_{CC} - + 5 volts

Flash Clear operation is provided on the MK41H79 via the $\overline{CLR}$ pin, and $\overline{CE}$ active (low). A low applied to the $\overline{CLR}$ pin clears all RAM bits to zero, making it especially useful for high speed cache and buffer storage applications.

OPERATIONS

READ MODE

The MK41H78/79 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ control signals. The data lines may be in an indeterminate state at t_{CEL} and t_{OEL}, but the data lines will always have valid data at t_{AA}.

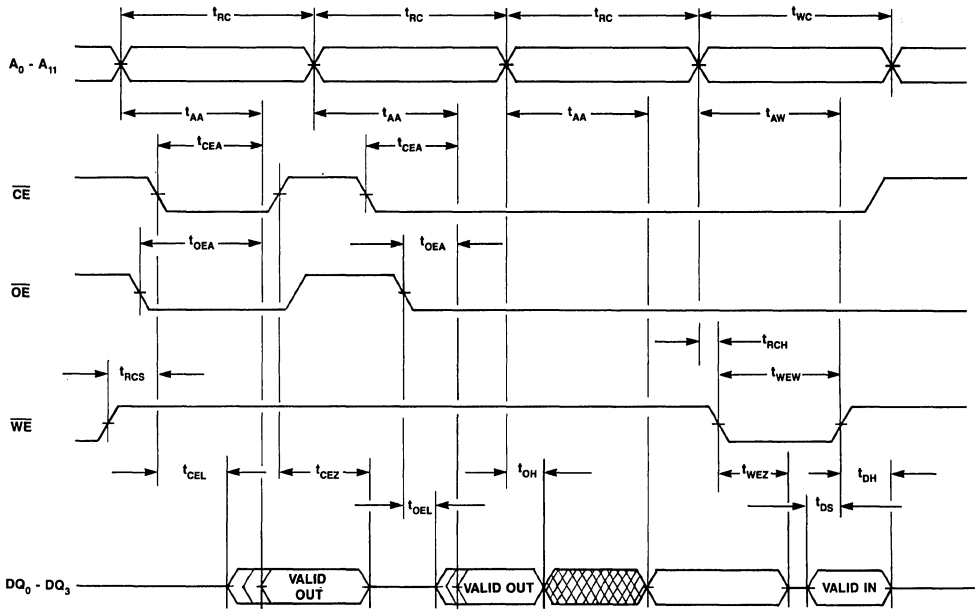


Figure 2. Read-Read-Read-Write Timing

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

		MK41H7X-20		MK41H7X-25		MK41H7X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CEL}	Chip Enable to Low-Z	7		7		7		ns	2
t_{CEA}	Chip Enable Access Time		20		25		35	ns	1
t_{OEL}	Output Enable to Low-Z	2		2		2		ns	2
t_{OEA}	Output Enable Access Time		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable to High-Z		8		10		13	ns	2
t_{OEZ}	Output Enable to High-Z		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H78/79 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}$ inputs are in the low state. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$. Therefore, t_{AS} is referenced to the latter occurring edge of CE or WE. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

If the output is enabled ($\overline{CE}$ and $\overline{OE}$ low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}$ or $\overline{WE}$.

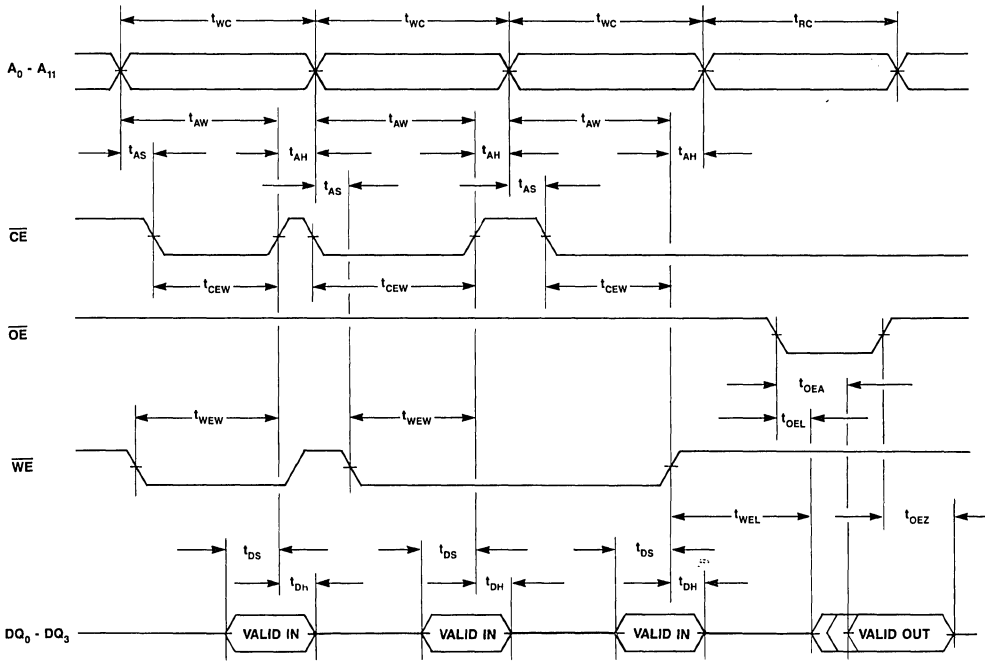


Figure 3. Write-Write-Write-Read Timing

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H7X-20		MK41H7X-25		MK41H7X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

LOW V_{CC} DATA RETENTION TIMING (MK41H78)

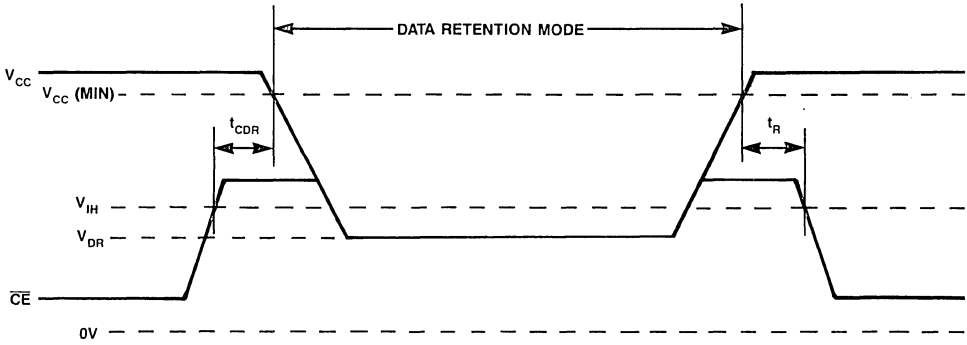


Figure 4. Data Retention Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

CLEAR CYCLE TIMING (MK41H79)
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

		MK41H79-20		MK41H79-25		MK41H79-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{FCC}	Flash Clear Cycle Time	40		50		70		ns	
t_{CEC}	Chip Enable Low to End of Clear	40		50		70		ns	
t_{CLP}	Flash Clear Low to End of Clear	38		48		68		ns	
t_{CX}	Clear to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear to Inputs Recognized	0		0		0		ns	
t_{CWX}	Clear to Write Enable Don't Care	0		0		0		ns	
t_{OHC}	Valid Data Out Hold from Clear	5		5		5		ns	1

FLASH CLEAR (MK41H79 Only)

A Flash Clear cycle sets all 16,384 bits in the RAM to logic zero. A Clear begins at the concurrence of a low on Chip Enable ($\overline{CE}$) and Flash Clear ($\overline{CLR}$). A Clear may be ended by a high on either $\overline{CE}$ or $\overline{CLR}$. A low on CLR has no effect if the device is disabled (CE high). A Clear may be executed within either a Read or a Write cycle. Figure 5 illustrates a Clear within a Read cycle. Clears within Write cycles are constrained only in that Write timing parameters must be observed as soon as the Flash Clear pin returns high.

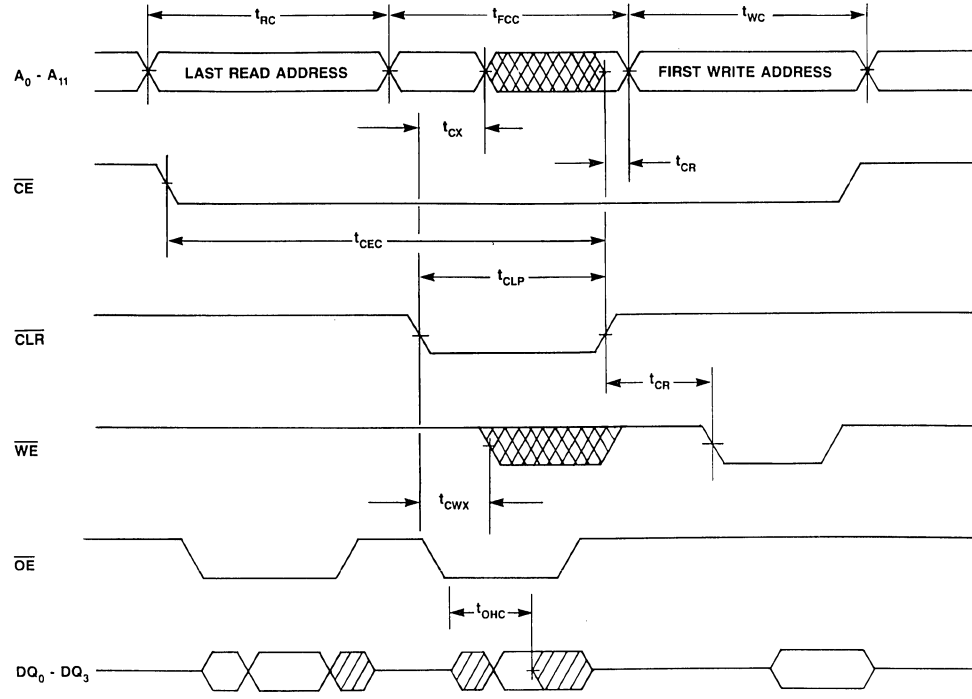


Figure 5. Last Read-Flash Clear-First Write

STANDBY MODE

The MK41H78/79 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

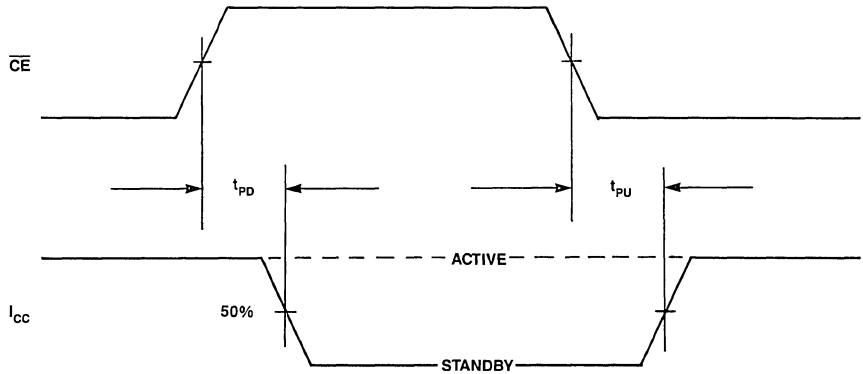


Figure 6. Standby Mode

STANDBY MODE

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

		MK41H7X-20		MK41H7X-25		MK41H7X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H78/79 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H78/79 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H78/79, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−1.0		0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	5
I_{CC2}	TTL Standby Current (MK41H78)		10	mA	6
I_{CC2}	TTL Standby Current (MK41H79)		16	mA	6
I_{CC3}	CMOS Standby Current (MK41H78)		50	μA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on DQ pins	8	10	pF	10

NOTES

1. Measured with load shown in Figure 7(A).
2. Measured with load shown in Figure 7(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{RC} = t_{RC} (min) is used.
6. $\overline{CE}$ = V_{IH}, all other inputs = Don't Care.
7. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V, all other inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that $0 V < V_{IN} < V_{CC}$. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that $0 V < V_{OUT} < V_{CC}$, $\overline{CE}$ = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

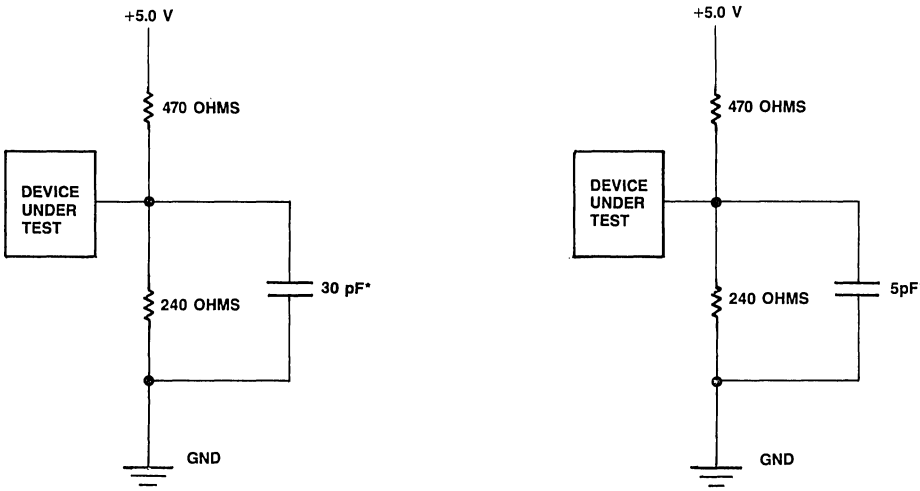
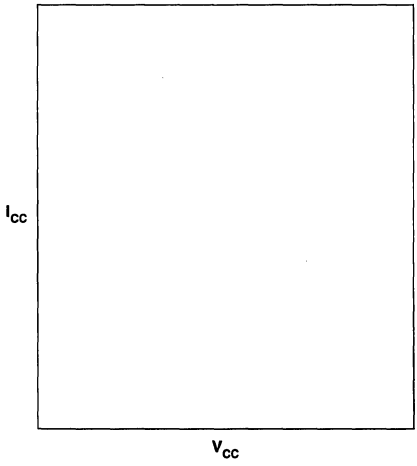
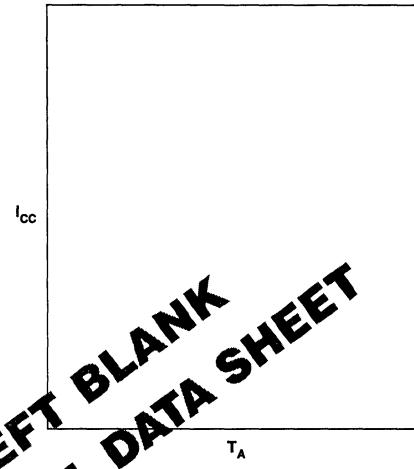


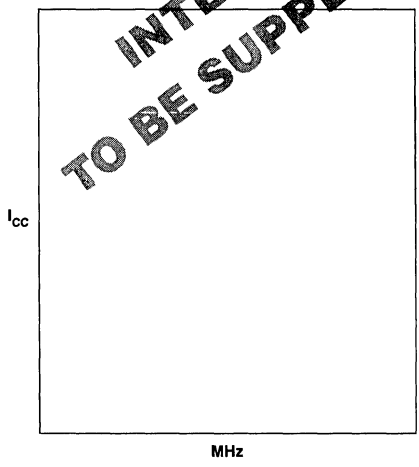
Figure 7. Output Load Circuits



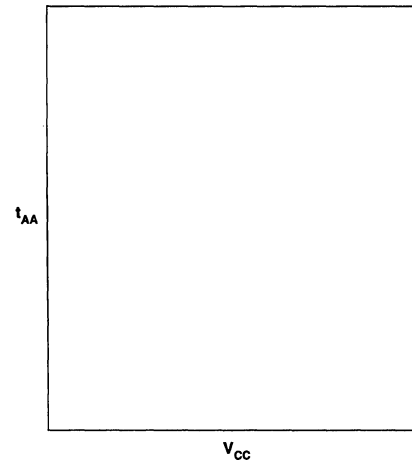
Normalized Supply Current vs. Supply Voltage



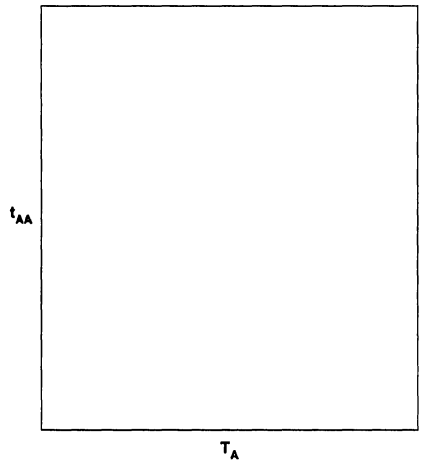
Normalized Supply Current vs. Ambient Temperature



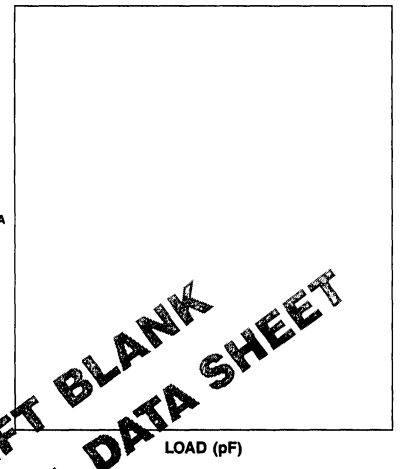
Normalized Supply Current vs. Cycle Time



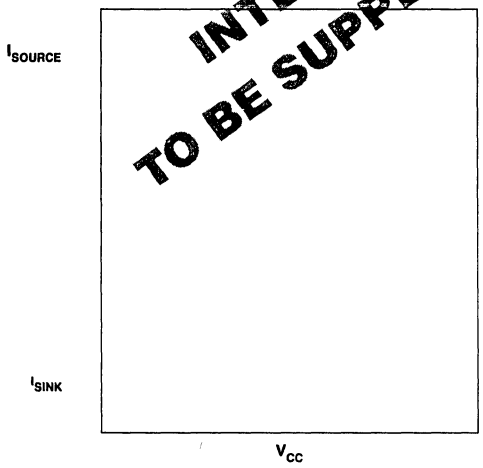
Normalized Address Access Time vs. Supply Voltage



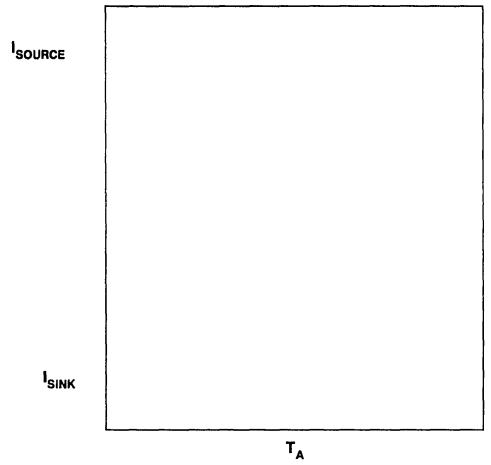
Normalized Address Access Time vs. Ambient Temperature



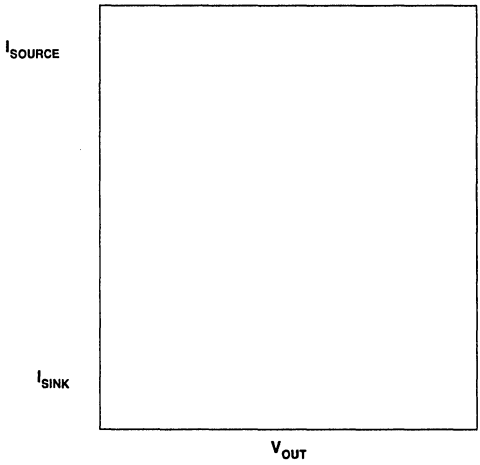
Normalized Address Access Time vs. Output Loading



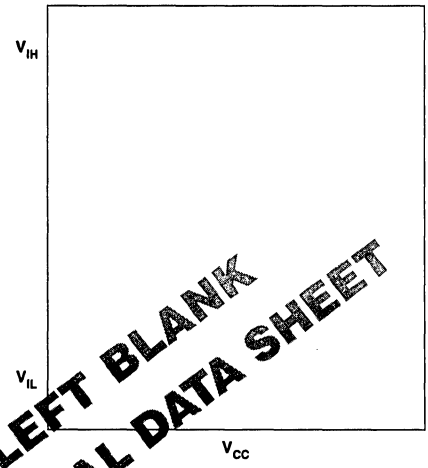
Normalized Output Source and Sink Currents vs. Supply Voltage



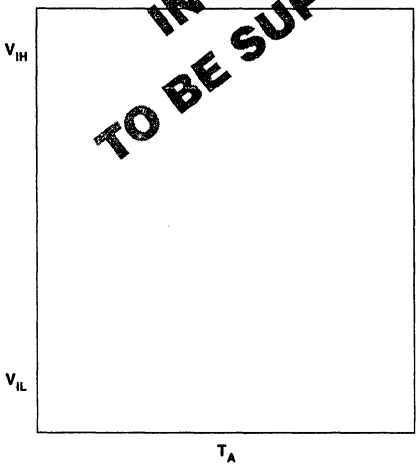
Normalized Output Source and Sink Currents vs. Ambient Temperature



Normalized Output Source and Sink Currents vs. Output Voltage

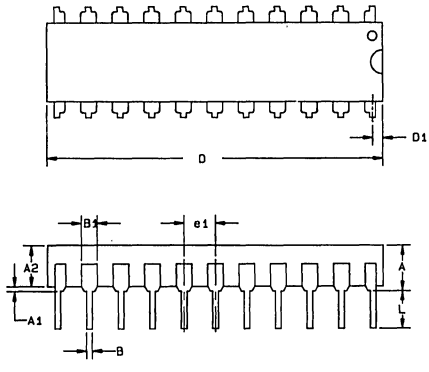


Logic Thresholds vs. Supply Voltage



Logic Thresholds vs. Ambient Temperature

22 PIN "N" PACKAGE
PLASTIC DIP

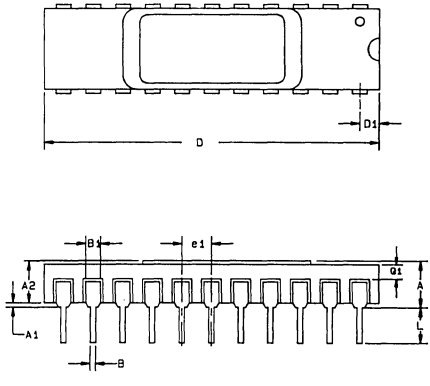


DIM	INCHES		NOTES
	MIN	MAX	
A	-	.210	2
A1	.015	-	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.010	.025	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	-	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

22 PIN "P" PACKAGE
SIDE BRAZED CERAMIC DIP



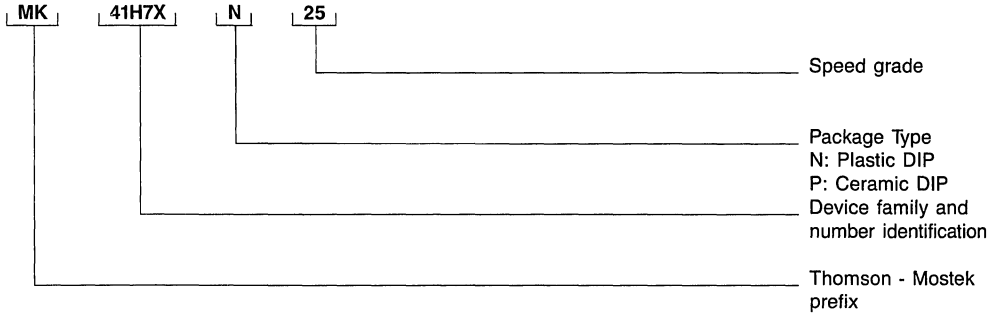
DIM	INCHES		NOTES
	MIN	MAX	
A	-	.175	1
A1	.020	-	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	1.085	1.115	
D1	.035	.065	
E	.295	.325	
E1	.280	.310	
e1	.090	.110	
eA	.290	.365	
L	.120	-	
Q1	.005	-	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H78N-20	20 ns	22 pin Plastic DIP	0°C to 70°C
MK41H78N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H78N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H78P-20	20 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H78P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H78P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H79N-20	20 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79P-20	20 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H79P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H79P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C



MK41L78/MK41L79(N,P)-25/35/45

4K x 4 CMOS STATIC RAM

PRELIMINARY

MEMORY COMPONENTS

FEATURES

- ☐ JEDEC LVTTL standard +3.3 volt operation
- ☐ 25, 35 and 45 nsec Address Access Time
- ☐ Equal access and cycle times
- ☐ 22-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ 50μA CMOS standby current
- ☐ TTL standby current unaffected by address activity
- ☐ Separate Output Enable control
- ☐ Flash Clear function (MK41L79)

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	*$\overline{CLR}$	Mode	DQ	Power
H	X	X	X	Deselect	High Z	Standby
L	X	L	H	Write	D_{IN}	Active
L	L	H	H	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active
L	X	L	L	Flash Clear	High Z	Active
L	L	H	L	Flash Clear	Low Z	Active
L	H	H	L	Flash Clear	High Z	Active

* - Applies to MK41L79 only. X = Don't Care

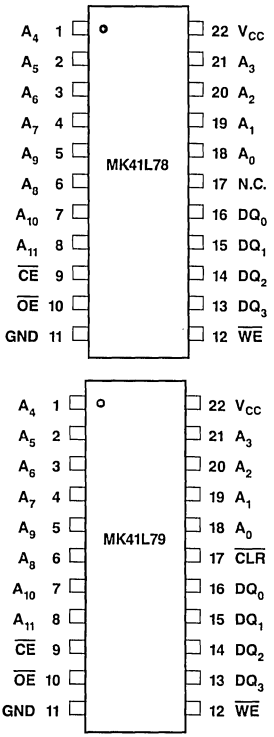


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{11} - Address	$\overline{OE}$ - Output Enable
DQ_0 - DQ_3 - Data I/O	$\overline{WE}$ - Write Enable
N.C. - No Connect (MK41L78)	GND - Ground
$\overline{CLR}$ - Flash Clear (MK41L79)	V_{CC} - +3.3 volts
$\overline{CE}$ - Chip Enable	

DESCRIPTION

The Mostek MK41L78 and MK41L79, together with their 20 pin derivatives, the MK41L68 and MK41L69, are the first devices on the market that meet or exceed the JEDEC Standard for LVTTL VLSI digital circuits. The LVTTL standard provides for compatibility between +5.0 ± 0.5 volt TTL devices and +3.3 ± 0.3 volt LVTTL devices within the same system. Adoption of a lower power supply voltage standard allows dimensional scaling of silicon die to continue, which in turn allows density and performance increases to continue. Scaling down the supply voltage provides a number of other potential benefits including reduced EMI, RFI, power consumption and increased reliability.

The MK41L78 and MK41L79 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The devices have a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full V_{CC} voltage. An output enable ($\overline{OE}$) pin provides a high speed three state control, allowing fast read/write cycles to be achieved with the common-I/O data bus.

Flash Clear operation is provided on the MK41L79 via the $\overline{CLR}$ pin, and $\overline{CE}$ active (low). A low applied to the $\overline{CLR}$ pin clears all RAM bits to zero, making it especially useful for high speed cache and buffer storage applications.

OPERATIONS

READ MODE

The MK41L78/9 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ control signals. The data lines may be in an indeterminate state at t_{CEL} and t_{OEL}, but the data lines will always have valid data at t_{AA}.

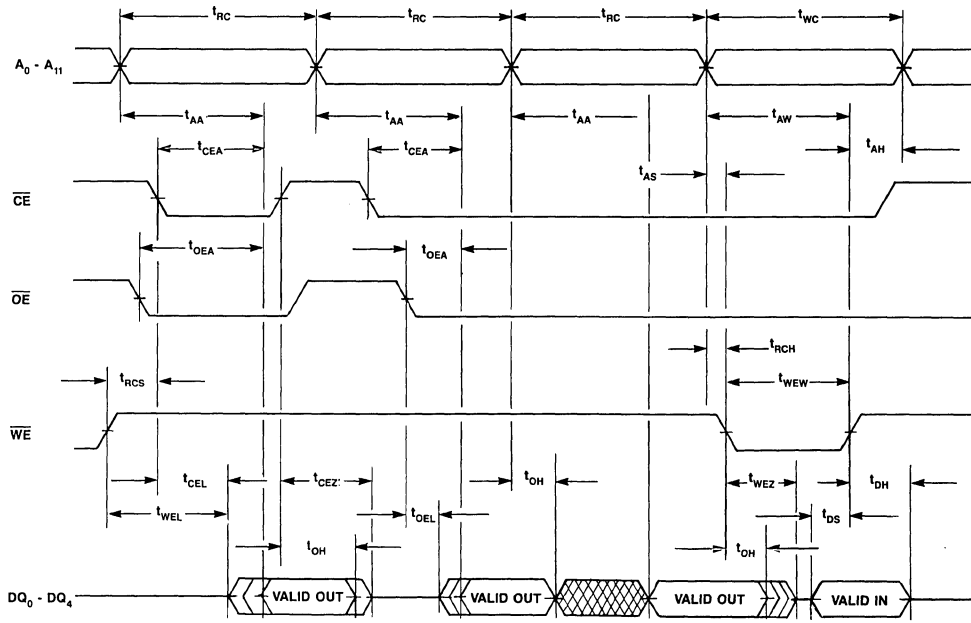


Figure 2. Read-Read-Read-Write Timing

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 3.3 ± 0.3 Volts)

		MK41L7X-25		MK41L7X-35		MK41L7X-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	25		35		45		ns	
t_{AA}	Address Access Time		25		35		45	ns	1
t_{CEL}	Chip Enable to Low-Z	7		7		7		ns	2
t_{CEA}	Chip Enable Access Time		25		35		45	ns	1
t_{OEL}	Output Enable to Low-Z	3		3		3		ns	2
t_{OEA}	Output Enable Access Time		12		15		18	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable to High-Z		10		13		15	ns	2
t_{OEZ}	Output Enable to High-Z		8		10		12	ns	2
t_{WEZ}	Write Enable to High-Z		10		13		15	ns	2
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

WRITE MODE

The MK41L78/9 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}$ inputs are in the low state. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

If the output is enabled ($\overline{CE}$ and $\overline{OE}$ low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}$ or $\overline{WE}$.

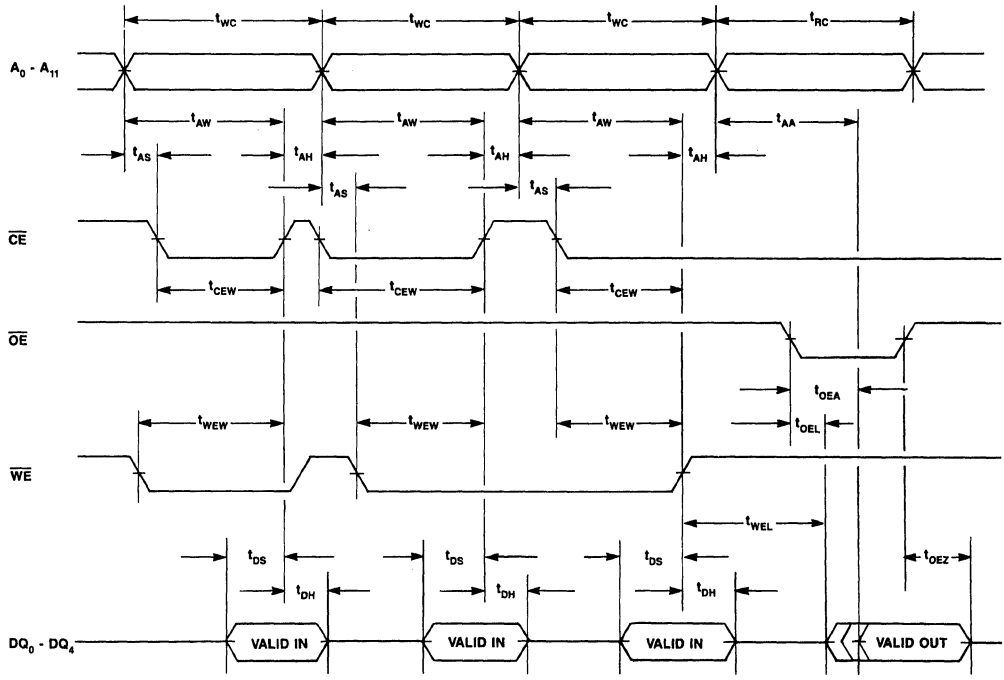


Figure 3. Write-Write-Write-Read Timing

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 3.3 ± 0.3 Volts)

SYM	PARAMETER	MK41L7X-25		MK41L7X-35		MK41L7X-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	25		35		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write	20		30		40		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	22		32		40		ns	
t_{WEW}	Write Enable to End of Write	20		30		40		ns	
t_{DS}	Data Setup Time	14		15		18		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

LOW V_{CC} DATA RETENTION TIMING (MK41L78)

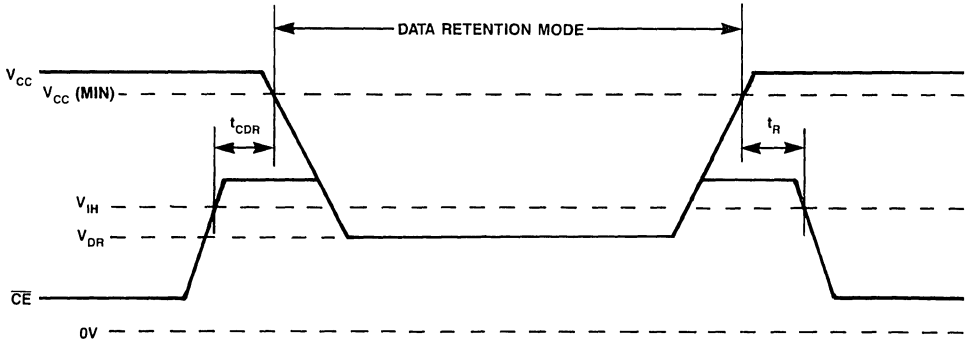


Figure 4. Data Retention Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

CLEAR CYCLE TIMING (MK41L79)
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 3.3 ± 0.3 Volts)

SYM	PARAMETER	MK41L79-25		MK41L79-35		MK41L79-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{FCC}	Flash Clear Cycle Time	50		70		90		ns	
t_{CEC}	Chip Enable Low to End of Clear	50		70		90		ns	
t_{CLP}	Flash Clear ($\overline{CLR}$) Pulse Width	45		65		85		ns	
t_{CX}	Clear to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear to Inputs Recognized	0		0		0		ns	
t_{CWX}	Clear to Write Enable Don't Care	0		0		0		ns	
t_{OHC}	Valid Data Out Hold from Clear	5		5		5		ns	1

FLASH CLEAR (MK41L79 Only)

A Flash Clear cycle sets all 16,384 bits in the RAM to logic zero. A Clear begins at the concurrence of a low on Chip Enable ($\overline{CE}$) and Flash Clear ($\overline{CLR}$). A Clear may be ended by a high on either $\overline{CE}$ or $\overline{CLR}$. A low on CLR has no effect if the device is disabled (CE high). A Clear may be executed within either a Read or a Write cycle. Figure 5 illustrates a Clear within a Read cycle. Clears within Write cycles are constrained only in that Write timing parameters must be observed as soon as the Flash Clear pin returns high.

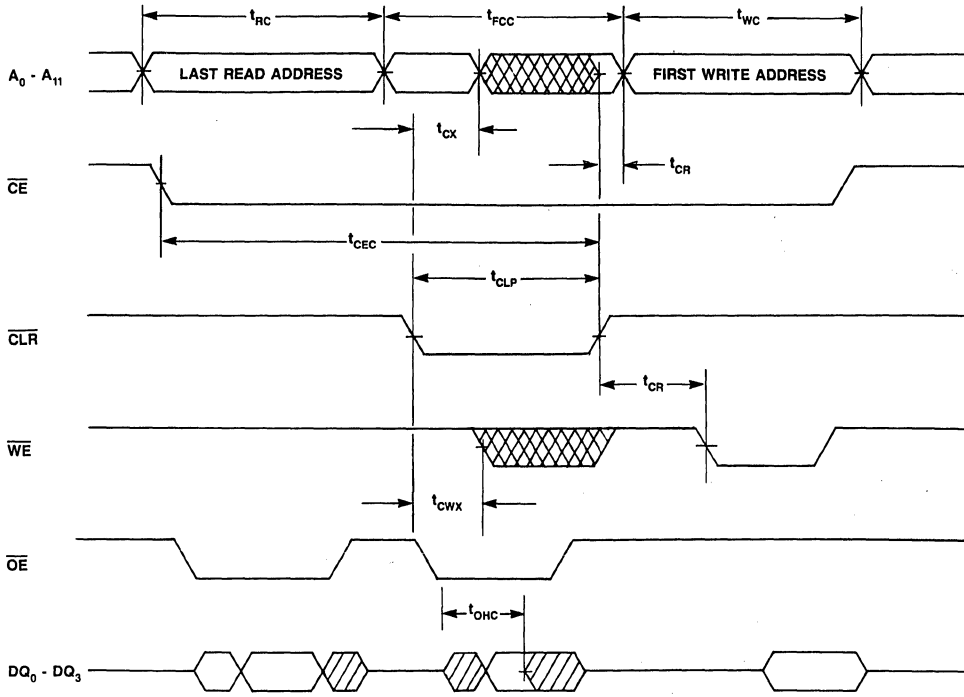


Figure 5. Last Read-Flash Clear-First Write

STANDBY MODE

The MK41L78/9 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

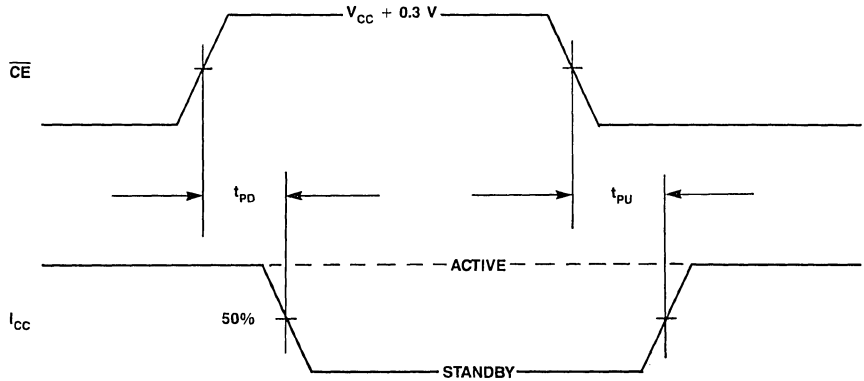


Figure 6. Standby Mode

STANDBY MODE CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 3.3 ± 0.3 volts)

		MK41L7X-25		MK41L7X-35		MK41L7X-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		25		35		45	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41L78/9 operates from a 3.3 volt supply. It is compatible with all 5 volt TTL families, such as ALS, F, and LS, on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly 5 volt TTL devices. Even though the Absolute Maximum Ratings allow the device to be accidentally installed in a 5 volt socket, care should be taken in normal applications to avoid driving inputs past the V_{IH} (max) specifications. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41L78/9, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM, especially in applications utilizing Flash Clear. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +6.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.0		V_{CC}+1.2	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−1.0		0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 3.3 ± 0.3 Volts)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		60	mA	5
I_{CC2}	TTL Standby Current (MK41L78)		8	mA	6
I_{CC2}	TTL Standby Current (MK41L79)		14	mA	6
I_{CC3}	CMOS Standby Current (MK41L78)		50	μA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −1 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +4 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

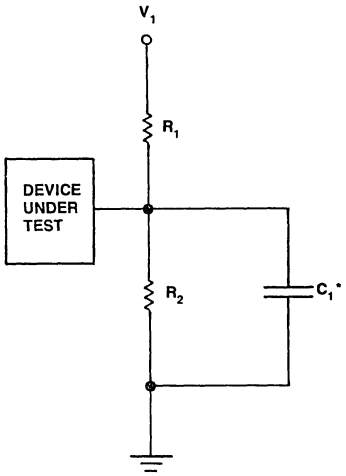
SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on DQ pins	8	10	pF	6,10

NOTES

1. Measured with load shown in Figure 7(A).
2. Measured with load shown in Figure 7(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t cycle = min. duty cycle 100%.
6. CE = V_{IH}.
7. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V, all other inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, CE- = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	3.3 ± 0.3 V



LOAD CIRCUIT VALUES

V_1	5.0 V	3.3 V
R_1	1000Ω	660Ω
R_2	670Ω	1016Ω
C_1	30 pF	30 pF

* INCLUDES SCOPE AND TEST JIG

EQUIVALENT TO:

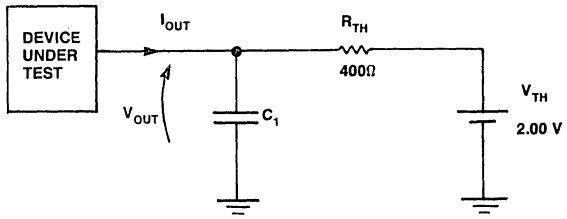
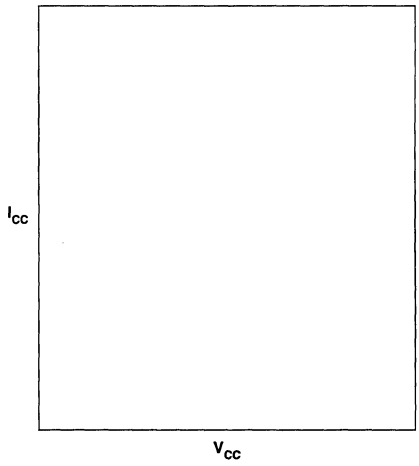
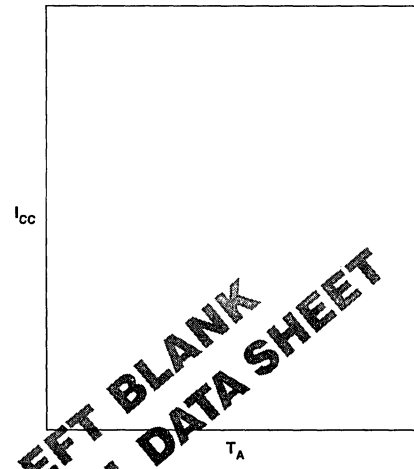


Figure 7. Output Load Circuits

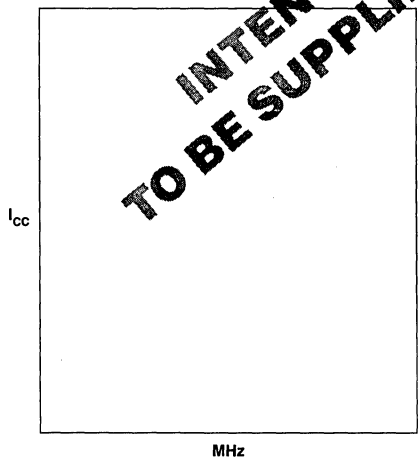
NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS



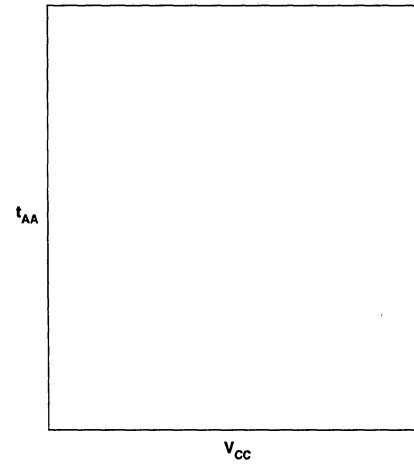
Normalized Supply Current vs. Supply Voltage



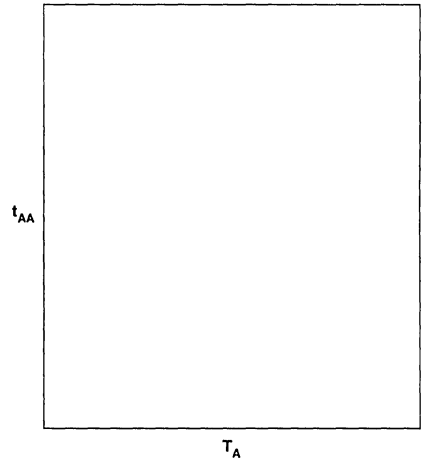
Normalized Supply Current vs. Ambient Temperature



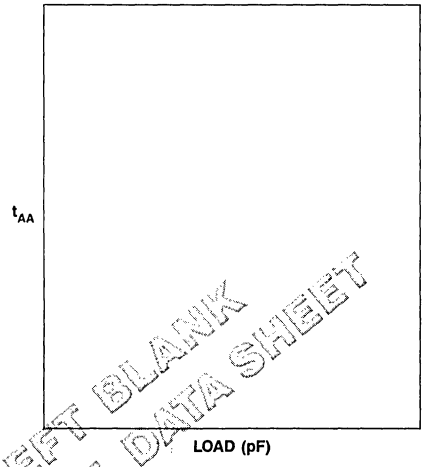
Normalized Supply Current vs. Cycle Time



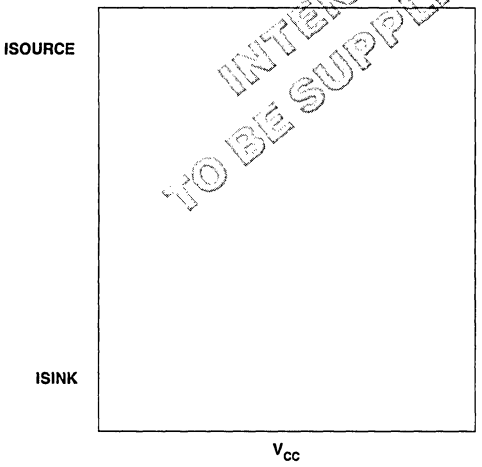
Normalized Address Access Time vs. Supply Voltage



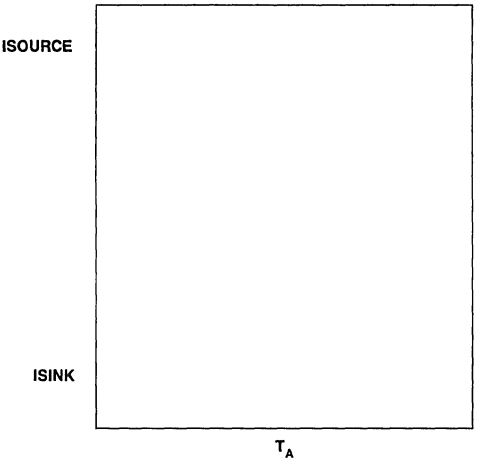
Normalized Address Access Time vs. Ambient Temperature



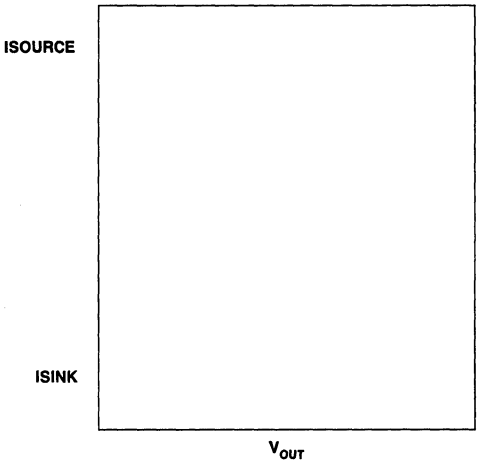
Normalized Address Access Time vs. Output Loading



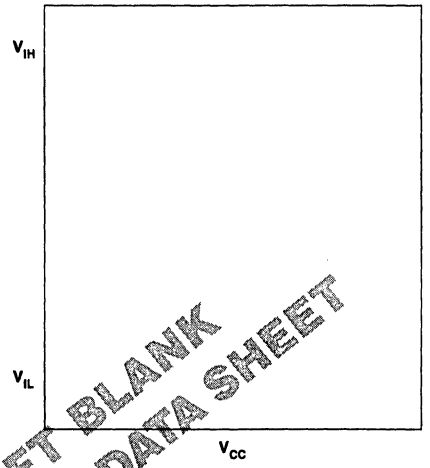
Normalized Output Source and Sink Currents vs. Supply Voltage



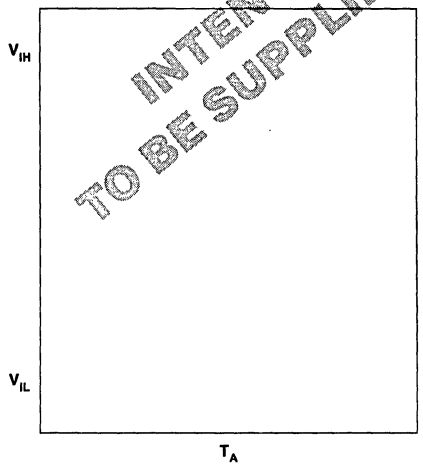
Normalized Output Source and Sink Currents vs. Ambient Temperature



Normalized Output Source and Sink Currents vs. Output Voltage

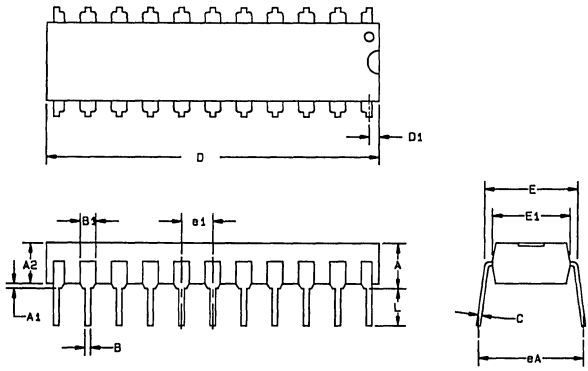


Logic Thresholds vs. Supply Voltage



Logic Thresholds vs. Ambient Temperature

22 PIN "N" PACKAGE
PLASTIC DIP

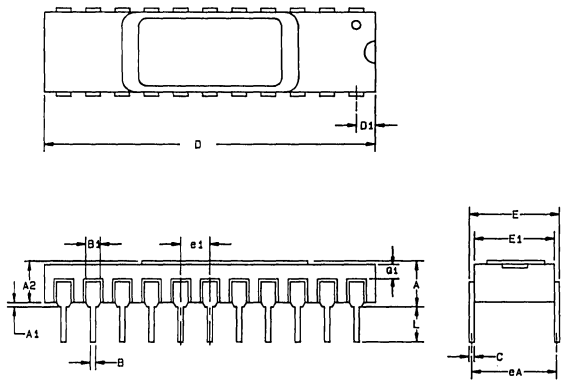


DIM	INCHES		NOTES
	MIN	MAX	
A	-	.210	2
A1	.015	-	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.010	.025	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	-	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

22 pin "P" PACKAGE
SIDE BRAZED CERAMIC DIP



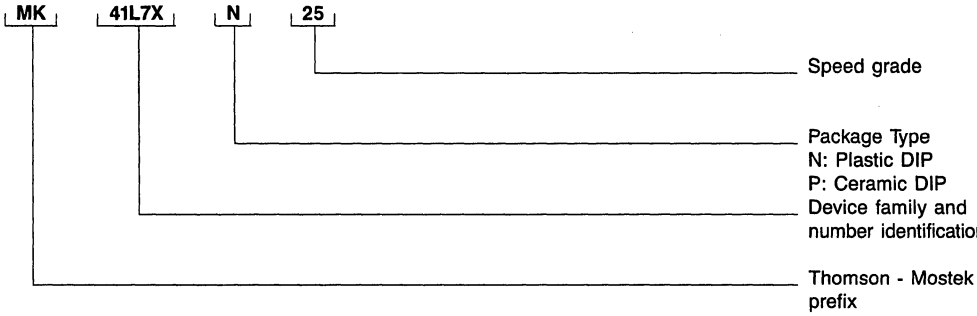
DIM	INCHES		NOTES
	MIN	MAX	
A	-	.175	1
A1	.020	-	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	1.085	1.115	
D1	.035	.065	
E	.295	.325	
E1	.280	.310	
e1	.090	.110	
eA	.290	.365	
L	.120	-	
Q1	.005	-	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41L78N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41L78N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41L78N-45	45 ns	22 pin Plastic DIP	0°C to 70°C
MK41L79N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41L79N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41L79N-45	45 ns	22 pin Plastic DIP	0°C to 70°C
MK41L78P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41L78P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C
MK41L78P-45	45 ns	22 pin Ceramic DIP	0°C to 70°C
MK41L79P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41L79P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C
MK41L79P-45	45 ns	22 pin Ceramic DIP	0°C to 70°C



MK41H87(N,P)-25/35/45

64K × 1 CMOS STATIC RAM

PRELIMINARY

MEMORY COMPONENTS

FEATURES

- ☐ 25, 35, and 45 ns Address Access Time
- ☐ Equal access and cycle times
- ☐ 22-pin, 300 mil Plastic and Ceramic DIP
- ☐ All inputs and outputs TTL compatible, low capacitance, and protected against static discharge
- ☐ 50 μA CMOS Standby Current
- ☐ Battery Backup Operation
- ☐ JEDEC standard pinout

MK41H87 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	Mode	Q	Power
H	X	Deselect	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

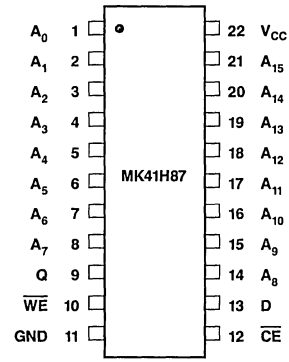


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{15} - Address	V_{CC} - + 5 volts
$\overline{CE}$ - Chip Enable	D - Data In
$\overline{WE}$ - Write Enable	Q - Data Out
GND - Ground	

DESCRIPTION

The MK41H87 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The MK41H87 requires only a single +5V ± 10 percent power supply, and it is fully TTL compatible.

The MK41H87 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

OPERATIONS

READ MODE

The MK41H87 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from one of 65,536 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ access time is satisfied. If $\overline{CE}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the Data Output pin is controlled by the CE and $\overline{WE}$ control signals. The Q may be in an indeterminate state at t_{CL}, but the Q will always have valid data at t_{AA}.

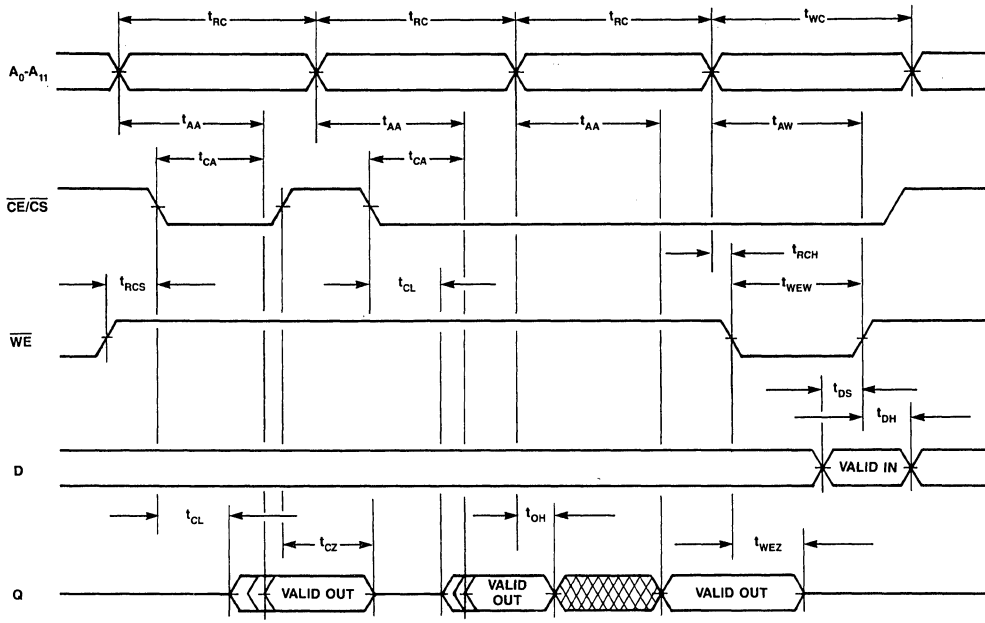


Figure 2. Read-Read-Read-Write Timing

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H87-25		MK41H87-35		MK41H87-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	25		35		45		ns	
t_{AA}	Address Access Time		25		35		45	ns	1
t_{CL}	Chip Enable to Low-Z	5		5		5		ns	2
t_{CA}	Chip Enable Access Time		25		35		45	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z		10		12		15	ns	2
t_{WEZ}	Write Enable to High-Z		10		12		15	ns	2

WRITE MODE

The MK41H87 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}$ inputs are in the low state. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. If the output is enabled ($\overline{CE}$ is low), then $\overline{WE}$ will return the output to high impedance within t_{WEZ} of its falling edge. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}$ or $\overline{WE}$.

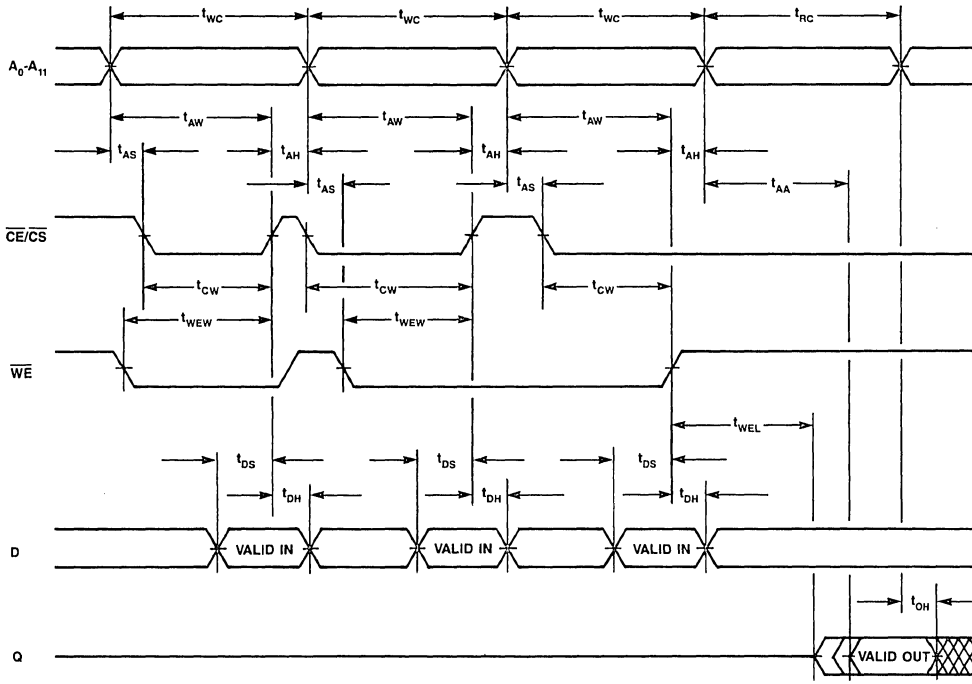


Figure 3. Write-Write-Write-Read Timing

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H8X-25		MK41H8X-35		MK41H8X-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	25		35		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	20		30		40		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable to End of Write	20		30		40		ns	
t_{WEW}	Write Enable to End of Write	20		25		30		ns	
t_{DS}	Data Setup Time	20		25		35		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

LOW V_{CC} DATA RETENTION TIMING

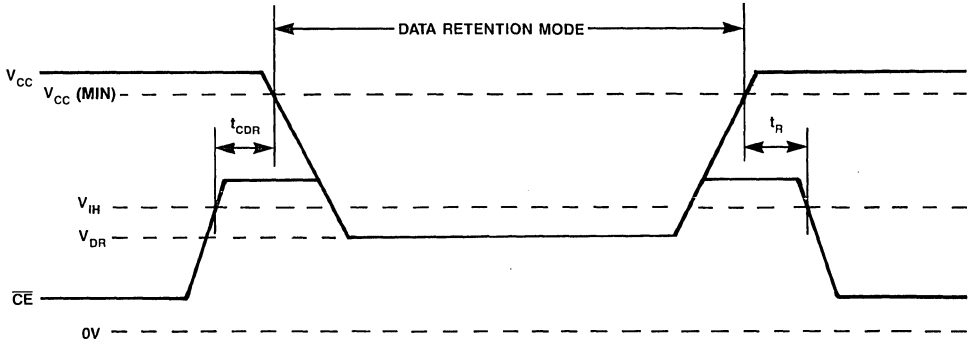


Figure 4. Data Retention Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41H87)

The MK41H87 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

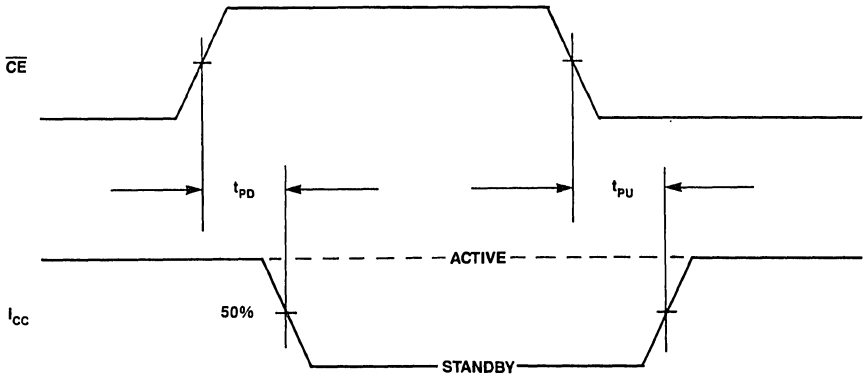


Figure 5. Standby Mode Timing

STANDBY MODE
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H87-25		MK41H87-35		MK41H87-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{PD}	Chip Enable High to Power Down		25		35		45	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H87 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H87 can also interface to 5 volt CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK41H87, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Ambient Storage Temperature (Plastic) ..... −55°C to +125°C
Ambient Storage Temperature (Ceramic) ..... −65°C to +150°C
Total Device Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−1.0		0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		60	mA	5
I_{CC2}	TTL Standby Current		4	mA	6
I_{CC3}	CMOS Standby Current		50	μA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on DQ pins	8	10	pF	6,10

NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
6. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
7. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V
   GND + 0.3 V ≥ A_0-A_{15} ≥ V_{IL} (min) or V_{IH} (max) ≥ A_0-A_{15} ≥ V_{CC} −0.3 V.
   All Other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}$/$\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

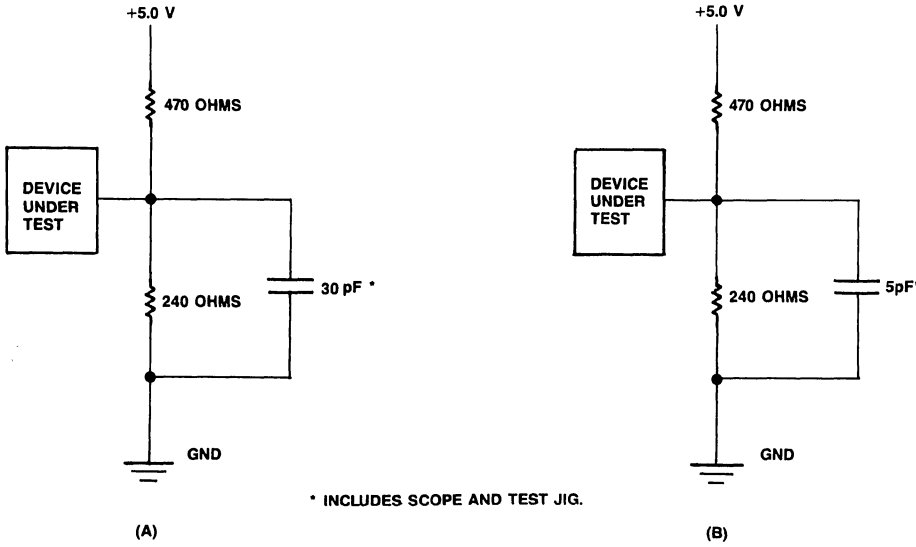
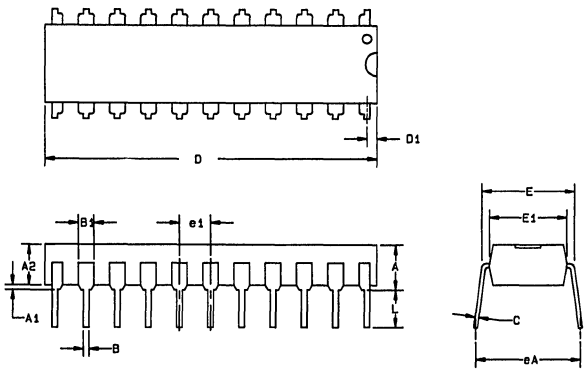


Figure 6. Output Load Circuits

22 PIN "N" PACKAGE
PLASTIC DIP

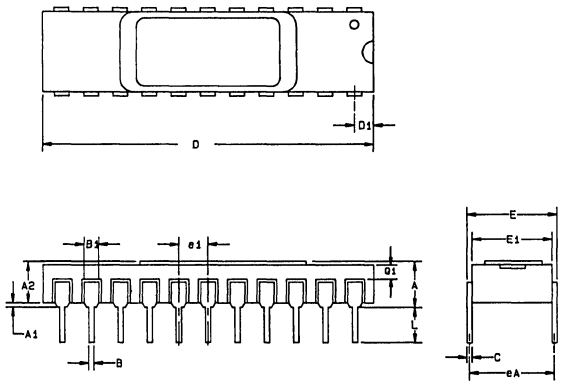


DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.020	1.050	1
D1	.010	.025	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

22 PIN "P" PACKAGE
SIDE BRAZED CERAMIC DIP



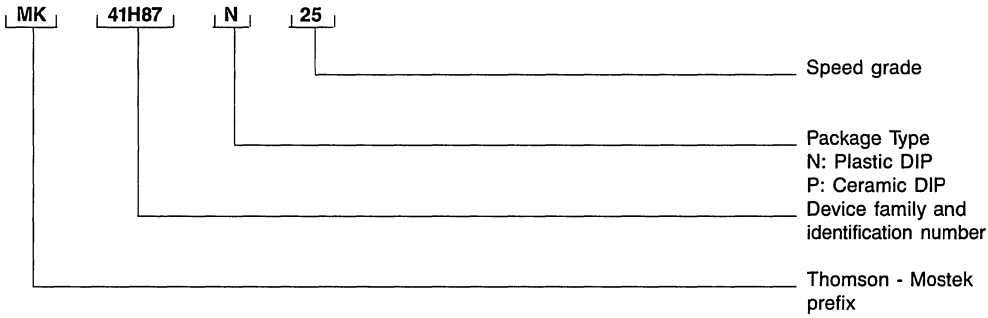
DIM	INCHES		NOTES
	MIN	MAX	
A	–	.175	1
A1	.020	–	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	1.085	1.115	
D1	.035	.065	
E	.295	.325	
E1	.280	.310	
e1	.090	.110	
eA	.290	.365	
L	.120	–	
Q1	.005	–	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H87N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H87N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H87N-45	45 ns	22 pin Plastic DIP	0°C to 70°C
MK41H87P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H87P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H87P-45	45 ns	22 pin Ceramic DIP	0°C to 70°C



MK41H80(N/P)-20/25/35

4K × 4 CMOS TAGRAM™

FEATURES

- ☐ 4K × 4 SRAM with onboard 4 bit Comparator
- ☐ 20, 25, and 35ns Address to Compare Access Time
- ☐ 12, 15, and 20 ns Tag Data to Compare Access Time
- ☐ Equal Access, Read and Write Cycle Times
- ☐ Flash Clear Function
- ☐ 22-pin, 300 mil Plastic and Ceramic Dip
- ☐ All Inputs and Outputs are TTL compatible, low capacitance, and protected against static discharge
- ☐ Word Width Expandable

TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	MODE
H	H	H	Valid	Compare Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Flash Clear Cycle

X = Don't Care

DESCRIPTION

The MK41H80 is a member of Mostek's 4K × 4 CMOS Static RAM family featuring fully static operation requiring no external clocks or timing strobes. Cycle Time and Compare Access Time are equal. The MK41H80 is powered by a single +5V ±10% power supply and the inputs and outputs are fully TTL compatible.

The MK41H80 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high match on the MATCH pin or an active low miss on the MATCH pin. The MATCH pins of several MK41H80's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

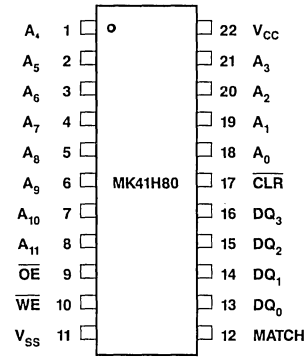


Figure 1. Pin Connections

PIN NAMES

A_0 - A_{11}	- Address Inputs
DQ_0 - DQ_3	- Data Input/Output
MATCH	- Comparator Output
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
$\overline{CLR}$	- Flash Clear
V_{CC}	- Power (+5V)
V_{SS}	- Ground

Tag data can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0-DQ_3).

Flash Clear operation is provided on the MK41H80 via the ($\overline{CLR}$) pin. A low applied to the $\overline{CLR}$ pin clears all RAM bits to a logic zero.

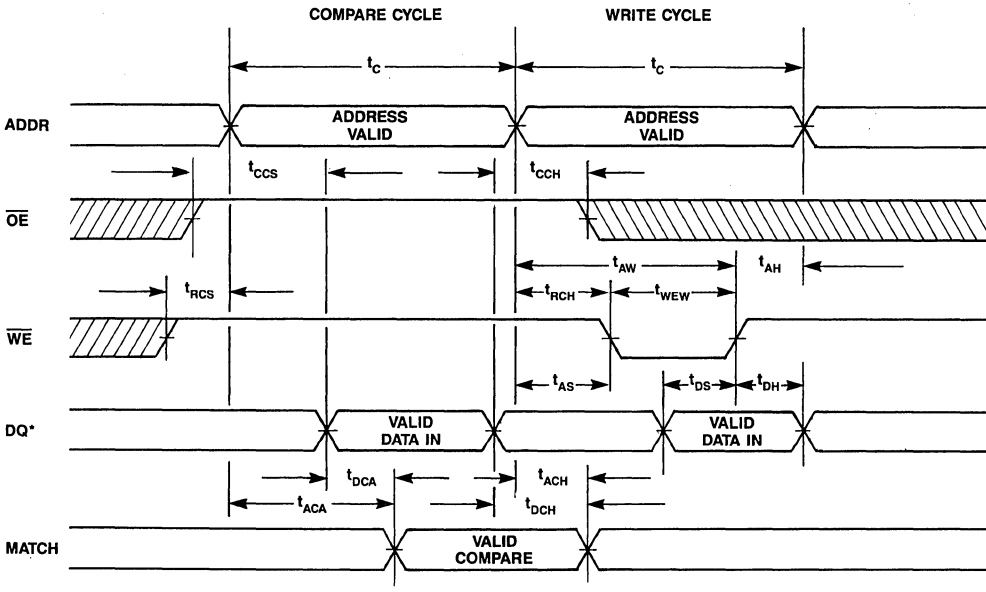


Figure 2. Compare and Write Cycle

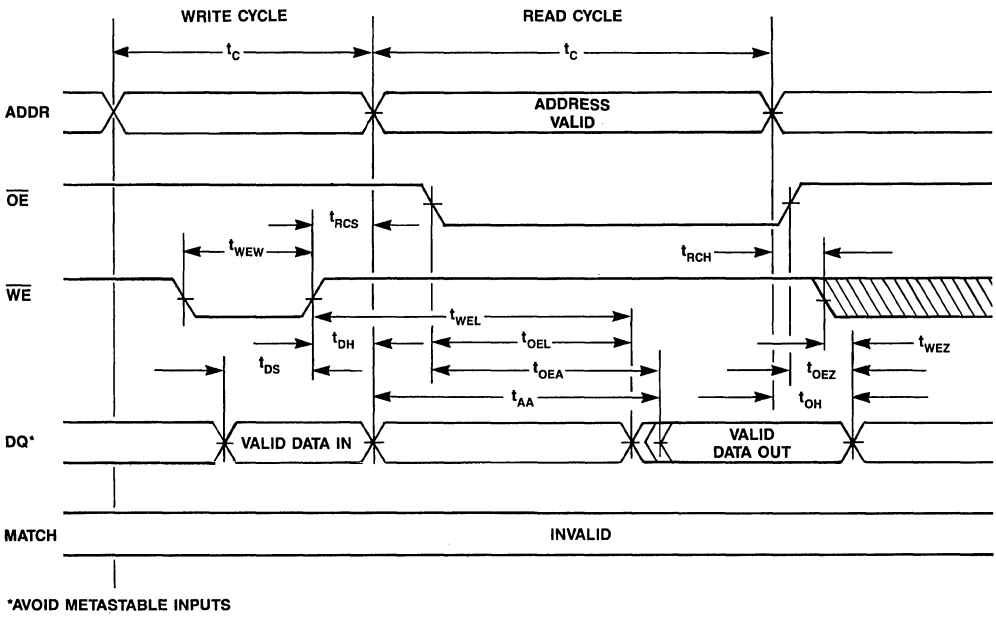


Figure 3. Write and Read Cycle

COMPARE, WRITE AND READ TIMING

The MK41H80 employs three signals for device control. The Write Enable ($\overline{WE}$) pin enables a Write Cycle if low and either a Compare Cycle or a Read Cycle when high. The $\overline{OE}$ pin enables a Read Cycle if low or a Compare Cycle if high. The $\overline{CLR}$ pin enables a Flash Clear Cycle when brought low.

The MK41H80 begins a Compare Cycle with the application of a valid address (see Figure 2). A valid MATCH is enabled when $\overline{OE}$ and $\overline{WE}$ go high in conjunction with their respective Set Up and Hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In. MATCH will then go invalid t_{ACH} after the address changes.

The MK41H80 starts a Write Cycle with stable addresses (see Figure 2). $\overline{OE}$ may be in either logic state. $\overline{WE}$ may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be held valid t_{DS} before and t_{DH} after $\overline{WE}$ goes high. MATCH will be invalid during this cycle.

The MK41H80 begins a Read Cycle with stable addresses and $\overline{WE}$ high (see Figure 3). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of $\overline{OE}$. DQ outputs become invalid t_{OH} after the address becomes invalid or t_{OEZ} after $\overline{OE}$ is brought high. Ripple through data access may be accomplished by holding $\overline{OE}$ active low while strobing addresses A_0-A_{11}, and holding $\overline{CLR}$ and $\overline{WE}$ high. The MATCH output will be invalid during the Read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

		-20		-25		-35			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_C	Cycle Time	20		25		35		ns	
t_{CCS}	Compare Command Set Up Time	7		8		10		ns	
t_{CCH}	Compare Command Hold Time	0		0		0		ns	
t_{RCS}	Read Command ($\overline{WE}$) Set Up Time	0		0		0		ns	
t_{RCH}	Read Command ($\overline{WE}$) Hold Time	0		0		0		ns	
t_{AS}	Address Set-up Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write Command ($\overline{WE}$)	16		20		30		ns	
t_{AH}	Address Hold Time after End of Write	0		0		0		ns	
t_{WEW}	Write Command ($\overline{WE}$) to End of Write	16		20		30		ns	
t_{DS}	Data Set Up Time	12		13		14		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{DCA}	Data Compare Access Time		12		15		20	ns	4
t_{ACA}	Address Compare Access Time		20		25		35	ns	4
t_{ACH}	Address Compare Hold Time	5		5		5		ns	4
t_{DCH}	Data Compare Hold Time	3		3		3		ns	4
t_{OEA}	Output Enable ($\overline{OE}$) Access Time		10		12		15	ns	4
t_{OH}	Valid Data Out ($\overline{DQ}$) Hold Time	5		5		5		ns	4
t_{AA}	Address Access Time		20		25		35	ns	4
t_{OEZ}	Output Enable ($\overline{OE}$) to High-Z		7		8		10	ns	5
t_{OEL}	Output Enable ($\overline{OE}$) to Low-Z	2		2		2		ns	5
t_{WEZ}	Write Enable ($\overline{WE}$) to High-Z		8		10		13	ns	5
t_{WEL}	Write Enable ($\overline{WE}$) to Low-Z	5		5		5		ns	5

APPLICATION

The MK41H80 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK41H80 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Because high frequency current transients will be associated with the operation of the MK41H80, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance.

The MK41H80 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents MATCH. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input data generating a miss. Since the comparator circuitry is always enabled, metastable data input levels can result in excessive MATCH output activity. Therefore, the use of data bus pull-up or pull-down resistors is recommended.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

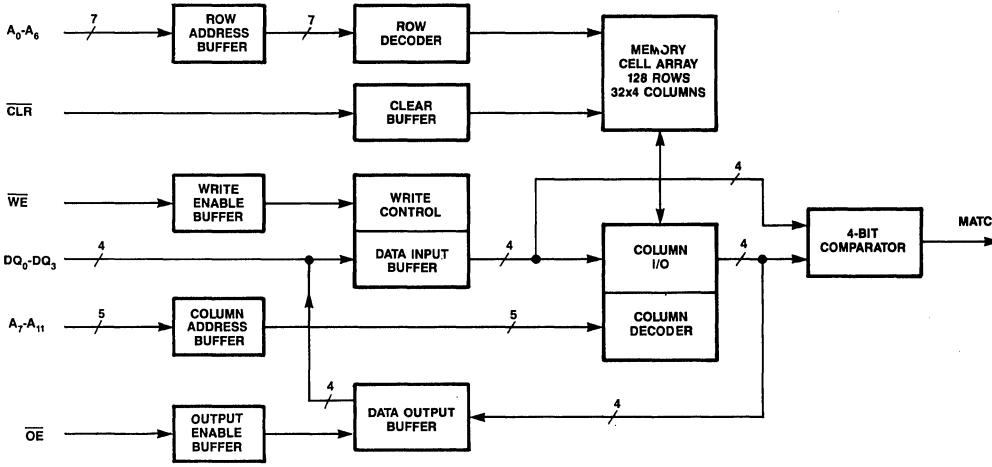


Figure 4. Block Diagram

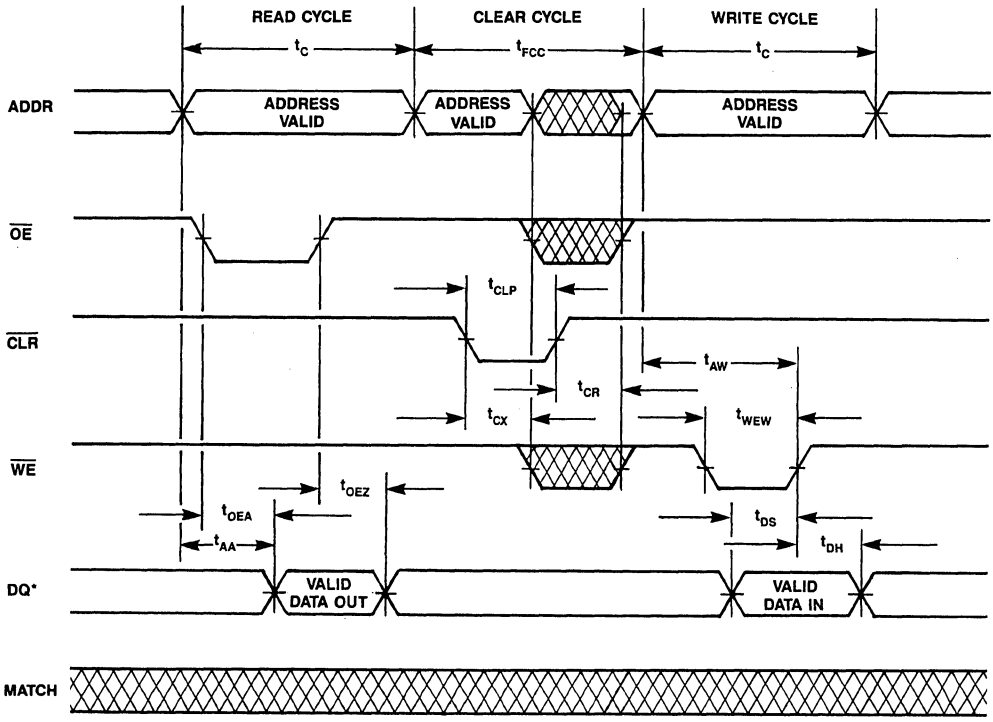
FLASH CLEAR CYCLE

A Flash Clear Cycle begins as $\overline{CLR}$ is brought low (see Figure 5). A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control Inputs will not be recognized from t_{CX} after $\overline{CLR}$ falls to t_{CR} after $\overline{CLR}$ is brought high. $\overline{OE}$ and $\overline{WE}$ are Don't Cares and DQ is High-Z. MATCH will be invalid while $\overline{CLR}$ is low.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

		-20		-25		-35			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{FCC}	Flash Clear Cycle Time	40		50		70		ns	
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear ($\overline{CLR}$) to Inputs Recognized	0		0		0		ns	
t_{CLP}	Flash Clear ($\overline{CLR}$) Pulse Width	36		44		60		ns	



*AVOID METASTABLE INPUTS

Figure 5. Read-Flash Clear-Write Cycle

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... −1.0V to +7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... −65°C to +150°C
Storage Temperature (Plastic) ..... −55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current per Pin ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (Referenced to V_{SS})	4.5	5.0	5.5	V	
V_{SS}	Ground	0.0	0.0	0.0	V	
V_{IH}	Input High (Logic 1) voltage, All Inputs (Referenced to V_{SS})	2.2		$V_{CC}+1$	V	
V_{IL}	Input Low (Logic 0) voltage, All Inputs (Referenced to V_{SS})	−1.0		0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Operating Current - Average Power Supply Operating Current		120	mA	2
I_{IL}	Input Leakage Current, Any input	−1	1	µA	6
I_{OL}	Output Leakage Current	−10	10	µA	7
V_{OH}	Output High (Logic 1) voltage Referenced to V_{SS}; I_{OH} = −4mA	2.4		V	
V_{OL}	Output Low (Logic 0) voltage Referenced to V_{SS}; I_{OL} = +8mA		0.4	V	

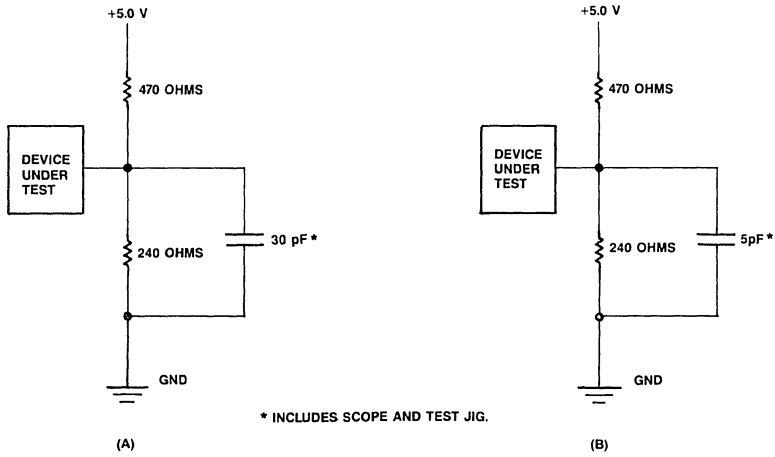
AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on any Input Pin	4	5	pF	3
C_2	Capacitance on any Output Pin	8	10	pF	3

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

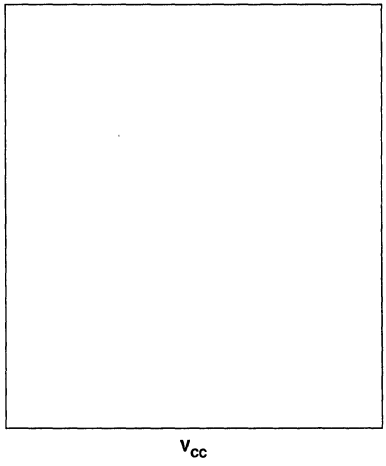


NOTES

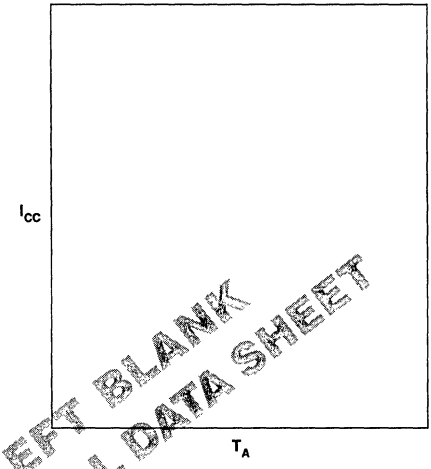
1. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
2. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. t cycle = min duty cycle 100%.
3. Capacitances are sampled and not 100% tested.
4. Measured with load shown in Figure 6(A).
5. Measured with load shown in Figure 6(B).
6. Input leakage current specifications are valid for all V_{IN} such that $0V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
7. Output leakage current specifications are valid for all DQs such that $0V < V_{OUT} < V_{CC}$. With exception to MATCH which is always enabled.

Figure 6. Output Load Circuits

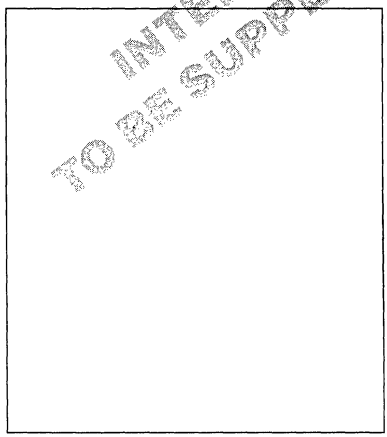
NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS



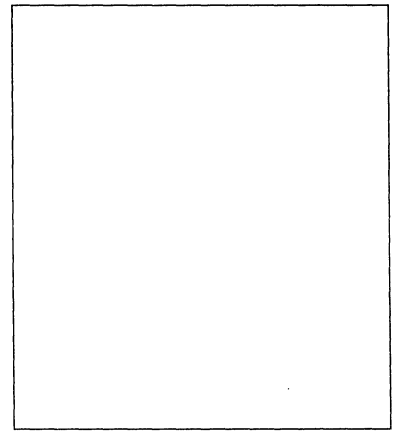
Normalized Supply Current vs. Supply Voltage



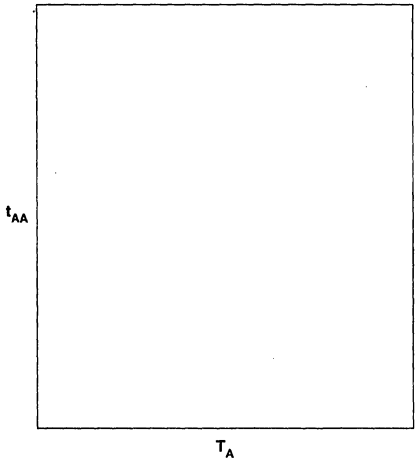
Normalized Supply Current vs. Ambient Temperature



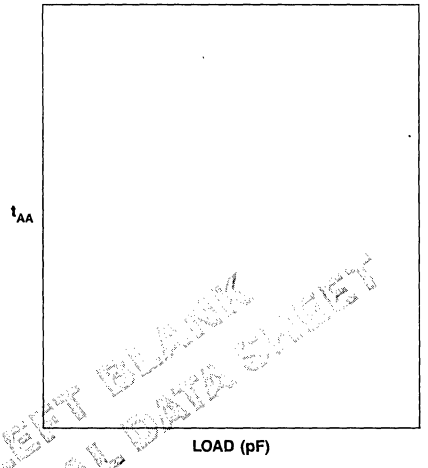
Normalized Supply Current vs. Cycle Time



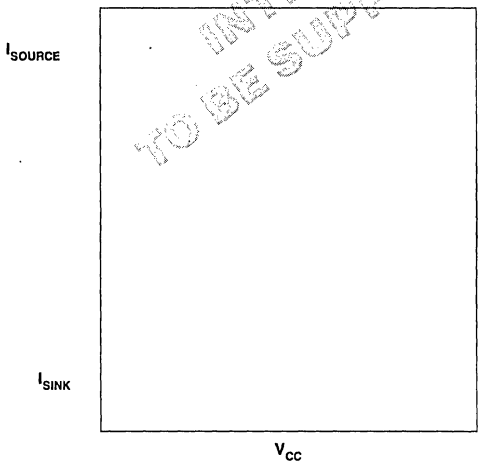
Normalized Access Time vs. Supply Voltage



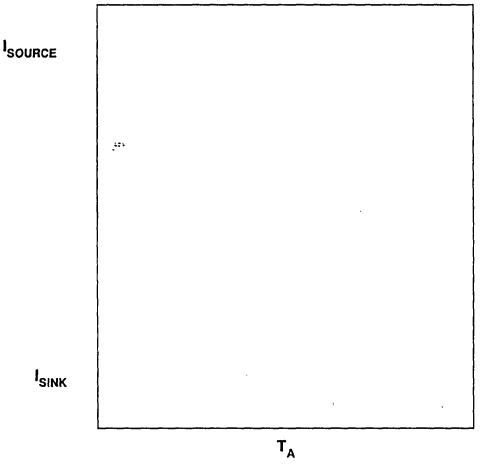
Normalized Access Time vs. Ambient Temperature



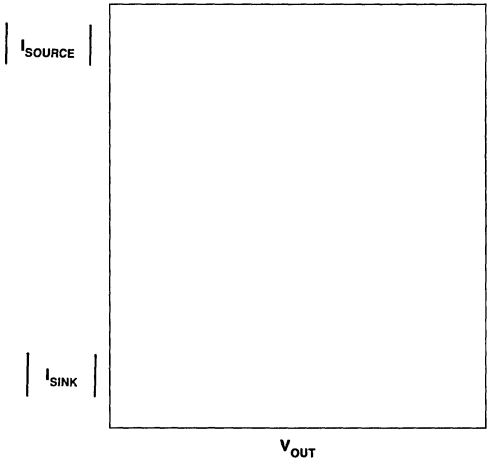
Normalized Access Time vs. Output Loading



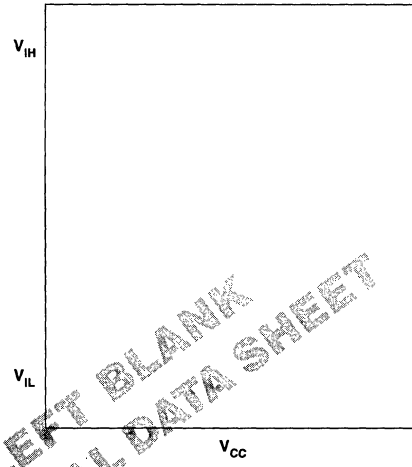
Normalized Output Source and Sink Currents vs. Supply Voltage



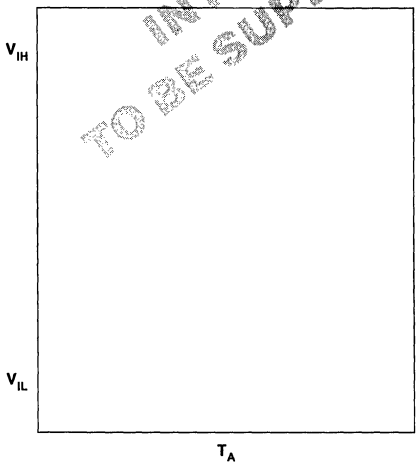
Normalized Output Source and Sink Currents vs. Ambient Temperature



Normalized Output Source and Sink Currents vs. Output Voltage

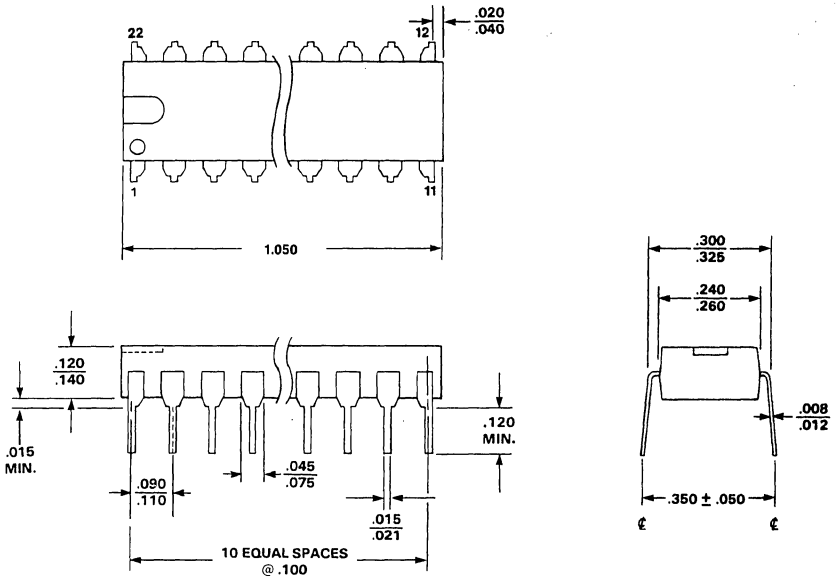


Logic Thresholds vs. Supply Voltage



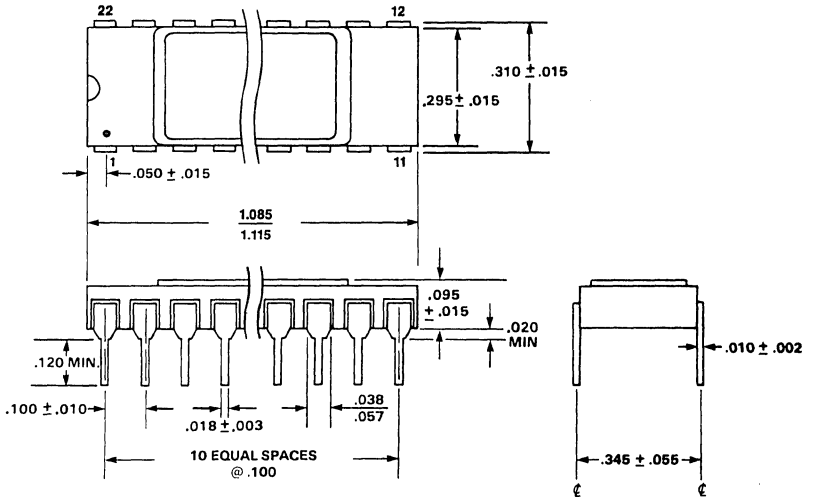
Logic Thresholds vs. Ambient Temperature

22 PIN "N" PACKAGE
PLASTIC DIP



NOTE: Overall length includes .010 flash on either end of package

22 PIN "P" PACKAGE
SIDE BRAZED CERAMIC DIP



ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H80N-20	20 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80P-20	20 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H80P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H80P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C

CHAPTER 2 - PROGRAMMABLE ROMs

NMOS EPROMs

Description	Part number	Organization	Access Time	Consumption	Page
UV ERASABLE PROM	ET2716	2K x 8	450 ns	500/125 mW	2-5
	ET2716-1	2K x 8	350 ns	500/125 mW	

CMOS EPROMs

Description	Part number	Organization	Access Time	Consumption	Page
UV ERASABLE PROM	ETC2716-5	2K x 8	550 ns	25/0.5 mW	2-11
	ETC2716	2K x 8	450 ns	25/0.5 mW	
	ETC2716-1	2K x 8	350 ns	25/0.5 mW	
	ETC2732-55	4K x 8	550 ns	25/0.5 mW	2-17
	ETC2732-45	4K x 8	450 ns	25/0.5 mW	
	ETC2732-35	4K x 8	350 ns	25/0.5 mW	
	TS27C64-30	8K x 8	300 ns	150/2.5 mW	2-25
	TS27C64-25	8K x 8	250 ns	150/2.5 mW	
	TS27C64-20	8K x 8	200 ns	150/2.5 mW	
	TS27C64-15	8K x 8	150 ns	150/2.5 mW	
	TS27C256-30	32K x 8	300 ns	200/2.5 mW	2-33
	TS27C256-25	32K x 8	250 ns	200/2.5 mW	
	TS27C256-20	32K x 8	200 ns	200/2.5 mW	
	TS27C256-15	32K x 8	150 ns	200/2.5 mW	
	TS27C1024	64K x 16	150 ns	250/5 mW	2-41
	TS27C1001	128K x 8	150 ns	250/5 mW	2-43

CMOS EEPROMs

Description	Part number	Organization	Access Time	Page
ELECTRICALLY ERASABLE PROM	TS59C11	64K x 16 or 128K x 8	—	2-45
	TS93C46	64K x 16 or 128K x 8	—	2-47
	TS28C16A	2K x 8	150 ns	2-49
	TS28C17A	2K x 8	150 ns	2-51
	TS28C64	8K x 8	150 ns	2-53

OTP ROMs

Description	Part number	Organization	Access Time	Consumption	Page
ONE TIME PROGRAMMABLE ROM	TS27C64P-20	8K x 8	200 ns	150/2.5 mW	2-55
	TS27C64P-25	8K x 8	250 ns	150/2.5 mW	
	TS27C64P-30	8K x 8	300 ns	150/2.5 mW	
	TS27C64P-35	8K x 8	350 ns	150/2.5 mW	
	TS27C256P-20	32K x 8	200 ns	200/2.5 mW	2-63
	TS27C256P-25	32K x 8	250 ns	200/2.5 mW	
	TS27C256P-30	32K x 8	300 ns	200/2.5 mW	
	TS27C256P-35	32K x 8	350 ns	200/2.5 mW	

THOMSON COMPONENTS
MOSTEK

ET2716(Q) • ET2716(Q)-1

16,384-BIT (2048 x 8) UV ERASABLE PROM

MEMORY COMPONENTS

The ET2716 is a high speed16K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

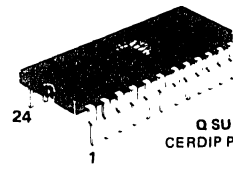
The ET2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology X-MOS.

- 2048 × 8 organization
- 525 mW max active power, 132 mW max standby power
- Low power during programming
- Access time ET2716-1, 350ns ; ET2716, 450ns
- Single 5V power supply
- Static-no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- Three-state output with OR-tie capability

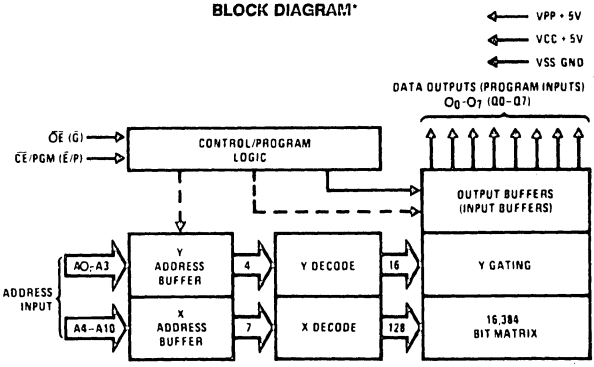
NMOS

16,384-BIT
(2048 x 8)
UV ERASABLE PROM

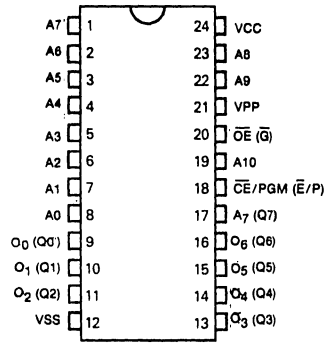


Q SUFFIX
CERDIP PACKAGE

BLOCK DIAGRAM*



PIN ASSIGNMENT



Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	OUTPUTS 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

*Symbols in parentheses are proposed JEDEC standard.

PIN NAMES*

A0–A10	Address Inputs
O0–O7 (Q0–Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature Under Bias	− 10° C to 80° C	All Input or Output Voltages with Respect to VSS (except VPP)	6V to − 0.3V
Storage Temperature	− 65° C to + 125° C	Power Dissipation	1.5 W
VPP Supply Voltage with Respect to VSS	26.5V to − 0.3V	Lead Temperature (Soldering, 10 seconds)	300° C

READ OPERATION (Note 2)

DC OPERATING CHARACTERISTICS (Note 3)

T_A = 0° C to + 70° C, VCC = 5V ± 5 % for ET2716, VCC = 5V ± 10 % for ET2716-1
VPP = VCC (Note 4), VSS = 0V, (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILI	Input Current	VIN = 5.25V or VIN = VIL	−	−	10	µA
ILO	Output Leakage Current	VOUT = 5.25V, $\overline{CE}$/PGM = 5V	−	−	10	µA
IPP1	VPP Supply Current	VPP = 5.25 V	−	−	5	mA
ICC1	VCC Supply Current (Standby)	$\overline{CE}$/PGM = VIH, $\overline{OE}$ = VIL	−	10	25	mA
ICC2	VCC Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	−	57	100	mA
VIL	Input Low Voltage		-0.1	−	0.8	V
VIH	Input High Voltage		2.0	−	V_{CC} +1	V
VOH	Output High Voltage	IOH = -400 µA	2.4	−	−	V
VOL	Output Low Voltage	IOL = 2.1 mA	−	−	0.45	V

AC CHARACTERISTICS

T_A = 0° C to +70° C, VCC = 5V ±5% for ET2716, VCC = 5V ±10% for ET2716-1
VPP = VCC (Note 4), VSS = 0V, (Unless otherwise specified)

SYMBOL		PARAMETER	CONDITIONS	ET2716-1		ET2716		UNITS
STANDARD	JEDEC			MIN	MAX	MIN	MAX	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	−	350	−	450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL	−	350	−	450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL	−	120	−	120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0	−	0	−	ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	0	100	ns

CAPACITANCE (Note 5)

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

AC Test Conditions

Output Load : 1 TTL gate and CL = 100 pF
Input Rise and Fall Times 20 ns
Input pulse levels : 0.45V to 2.4V
Timing measurement reference level = Inputs and outputs 0.8V and 2V

Note 1 : "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2 : VCC must be applied at the same time or before VPP and removed after or at the same time as VPP

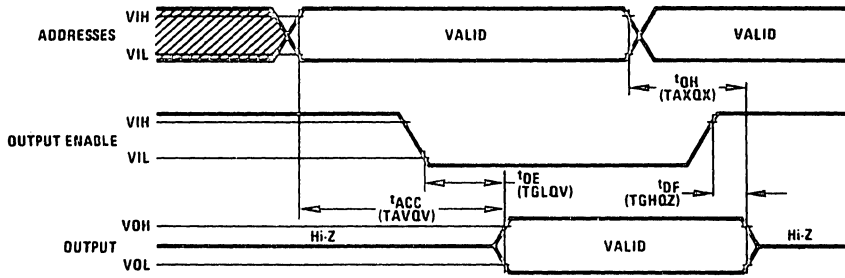
Note 3 : Typical conditions are for operation at : T_A = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V

Note 4 : VPP may be connected to VCC except during program.

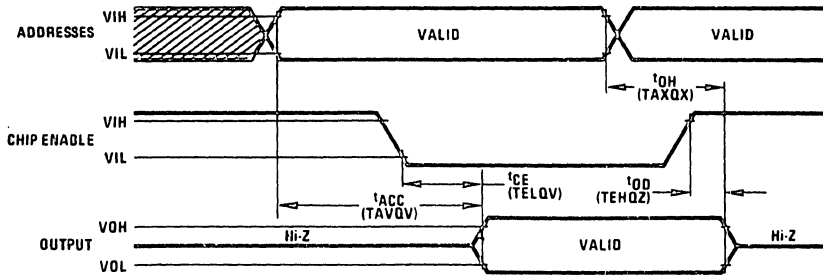
Note 5 : Capacitance is guaranteed by periodic testing. T_A = 25° C, f = 1 MHz.

SWITCHING TIME WAVEFORMS*

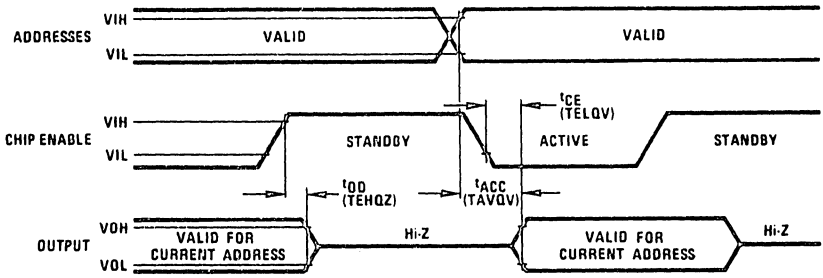
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



* Symbols in parentheses are proposed JEDEC standard.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (Notes 1 and 2)
(T_A = 25°C ± 5°C) (VCC = 5V ± 5 %, VPP = 25V ± 1V)

SYMBOL	PARAMETER	MIN	MAX	UNITS
ILI	Input Leakage Current (Note 3)	–	10	μA
VIL	Input Low Level	−0.1	0.8	V
VIH	Input High Level	2.0	VCC + 1	V
ICC	VCC Power Supply Current	–	100	mA
IPP1	VPP Supply Current (Note 4)	–	5	mA
IPP2	VPP Supply Current During Programming Pulse (Note 5)	–	30	mA

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes 1, 2, and 6)
(T_A = 25°C ± 5°C) (VCC = 5V ± 5 %, VPP = 25V ± 1V)

SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS
STANDARD	JEDEC					
t_{AS}	TAVPH	Address Setup Time	2	–	–	μs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2	–	–	μs
t_{DS}	TDVPH	Data Setup Time	2	–	–	μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2	–	–	μs
t_{DH}	TPLDX	Data Hold Time	2	–	–	μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0	–	100	ns
t_{CE}	TGLQV	Chip Enable to Output Delay (Note 4)	–	–	120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5	–	–	ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5	–	–	ns

Note 1 : VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.
Note 2 : Care must be taken to prevent overshoot of the VPP supply when switching to + 25V
Note 3 : $0.45V \leqslant VIN < 5.25V$
Note 4 : $\overline{CE}$/PGM = VIL, VPP = VCC
Note 5 : VPP = 26 V
Note 6 : Transition times $\leqslant$ 20 ns unless otherwise noted

Program Mode

The ET2716 is programmed by introducing "0" s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels including the program pulse on chip enable are TTL compatible. The programming sequence is :

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIL = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) must not be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. ET2716's may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the ET2716 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with VPP = 25V (or 5V) in either case. VPP must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

Program Inhibit Mode

The program inhibit mode allows programming several ET2716's simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the ET2716 may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

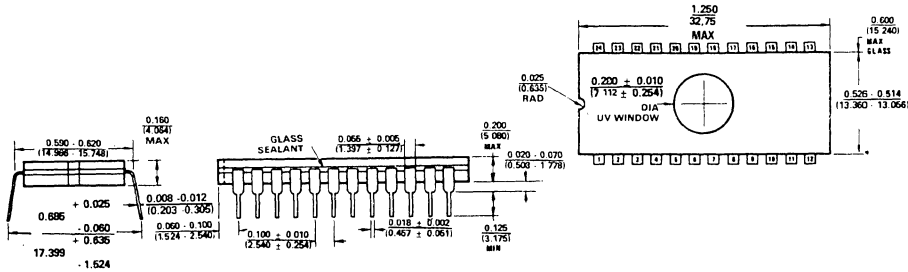
ERASING

The ET2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the ET2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm² power rating is used. The ET2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PHYSICAL DIMENSIONS inches (millimeters)

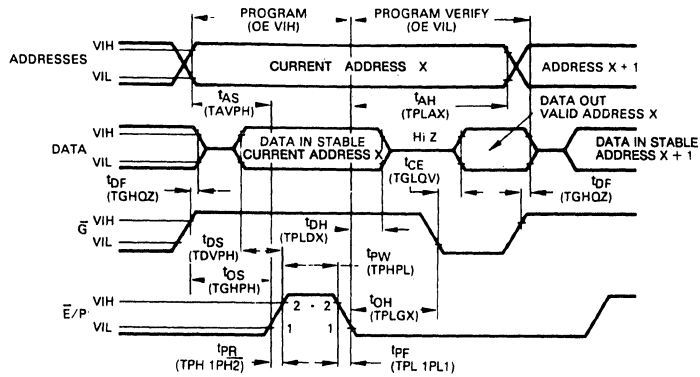


UV window Cavity Dual-In-Line Package (JQ)
Order Number ET2716Q (-, 1)
Package Number J24 CQ

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

TIMING DIAGRAM *

Program Mode



DEVICE OPERATION

The ET2716 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The ET 2716 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PCM = VIL and that addresses A0—A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The ET 2716 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more ET2716's for memory expansion.

Standby Mode (Power Down)

The ET2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25 % (132 mW max) of the normal operating power. VCC and VPP must be maintened at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The ET 2716 is shipped from THOMSON SEMICONDUCTEURS completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

TABLE I. OPERATING MODES (VCC = VPP = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	VPP 21	OUTPUTS Q 9–11, 13–17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

* Symbols in parentheses are proposed JEDEC standard

ETC2716(Q) • ETC2716(Q)-1/5

16,384-BIT (2048 x 8) CMOS UV ERASABLE PROM

The ETC 2716 is a high speed16K UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around pattern experimentation and low power consumption are important requirements.

The ETC 2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

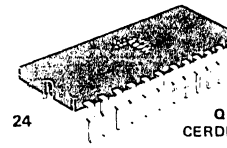
This EPROM is fabricated with the reliable, high volume, time proven, P2CMOS silicon gate technology.

- CMOS power consumption
- Performance compatible to market standard 8-bit CMOS Microp
- 2048 x 8 organization
- Pin compatible to 2716
- Access time down to 350 ns
- Single 5V power supply
- Static - no clocks required
- TTL compatible I/Os during both read and program modes
- Three-state output with OR-tie capability
- Oper. temp.: 0°C,+ 70°C ; –25°C,+ 70°C (E suffix) ; –40°C,+ 85°C (V suffix)

Parameter/Part Number	ETC 2716-1	ETC 2716	ETC 2716-5
Access Time (ns)	350	450	550
Active Current (mA a 1 MHz)	5	5	5
Standby Current (mA)	0.1	0.1	0.1

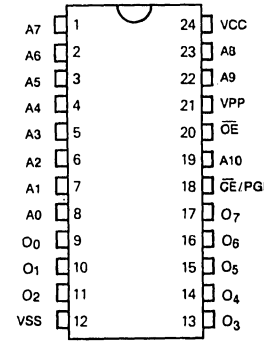
CMOS

16,384-BIT
(2048 x 8)
UV ERASABLE PROM

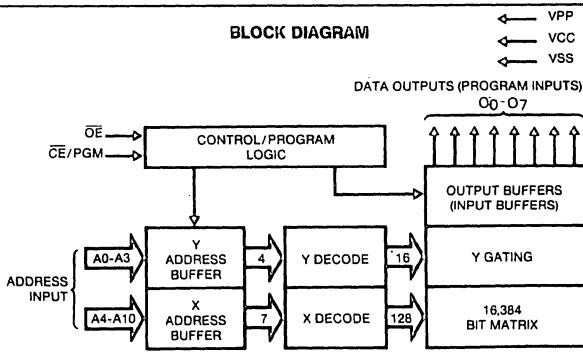


Q SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT



BLOCK DIAGRAM



Pin Connection During Read or Program

Mode	Pin Name/Number				
	CE/PGM 18	OE 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

PIN NAMES

A0-A10	Address Inputs
O_0-O_7	Data Outputs
CE/PGM	Chip Enable/Program
OE	Output Enable
VPP	Read 5V, Program 25V
VCC	5V
VSS	Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature Under Bias	−10°C to + 80°C
Storage Temperature	−65°C to +125°C
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V
Input Voltages with Respect to VSS except VPP (Note 5)	6V to −0.3V
Output Voltages with Respect to VSS	VCC + 0.3V to VSS − 0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION (Note 2)

DC OPERATING CHARACTERISTICS

TA = 0°C to +70°C, VCC = 5V ± 5%, VPP = VCC (Note 3), VSS = 0V,(Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
ILI	Input Current	VIN = VCC or GND	–	–	10	μA
ILO	Output Leakage Current	VOUT = 5.25V, $\overline{CE}$/PGM = VIH	–	–	10	μA
VIL	Input Low Voltage		−0.1	–	0.8	V
VIH	Input High Voltage	(Note 5)	2.0	–	VCC + 1	V
VOL1	Output Low Voltage	IOL = 2.1 mA	–	–	0.45	V
VOH1	Output High Voltage	IOH = −400 μA	2.4	–	–	V
VOL2	Output Low Voltage	IOL = 0 μA	–	–	0.1	V
VOH2	Output High Voltage	IOH = 0 μA	VCC − 0.1	–	–	V
IPP1	VPP Supply Current	VPP = 5.25V	–	–	10	μA
ICC1	VCC Supply Current Active (TTL Levels)	$\overline{CE}$/PGM, $\overline{OE}$ = VIL Addresses = VIH or VIL Frequency 1 MHz, I/O = 0 mA	–	2	10	mA
ICC2	VCC Supply Current Active (CMOS Levels)	$\overline{CE}$/PGM, $\overline{OE}$ = VIL (Note 5) Addresses = GND or VCC Frequency 1 MHz, I/O = 0 mA	–	1	5	mA
ICCSB1	VCC Supply Current Standby	$\overline{CE}$/PGM = VIH	–	0,1	1	mA
ICCSB2	VCC Supply Current Standby	$\overline{CE}$/PGM = VCC	–	0,01	0,1	mA

CAPACITANCE (Note 4) TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

AC TEST CONDITIONS

Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and CL = 100 PF
Input and Output Timing Reference Levels	0.8V, 2V

Note 1 : "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2 : Typical conditions are for operation at : TA = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V.

Note 3 : VPP may be connected to VCC except during program.

Note 4 : Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.

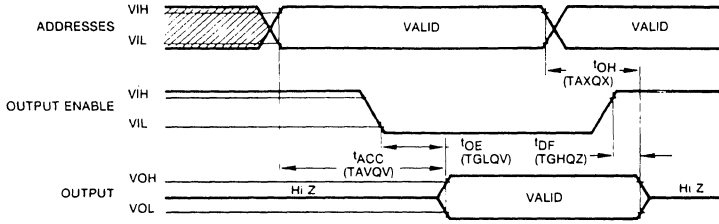
Note 5 : The inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3V.

AC CHARACTERISTICS TA = 0°C to + 70°C, VCC = 5V ± 5%, VPP = VCC, VSS = 0V, (Unless otherwise specified)

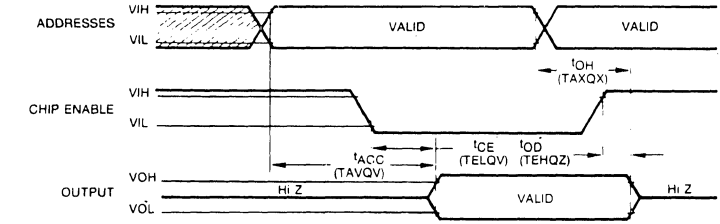
Symbol		Paramoter	Conditions	ETC2716-1		ETC 2716		ETC 2716-5		UNIT
Alternate	Standard			Min	Max	Min	Max	Min	Max	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	–	350	–	450	–	550	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL	–	350	–	450	–	550	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL	–	120	–	120	–	120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0	–	0	–	0	–	ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	0	100	0	100	ns

SWITCHING TIME WAVEFORMS

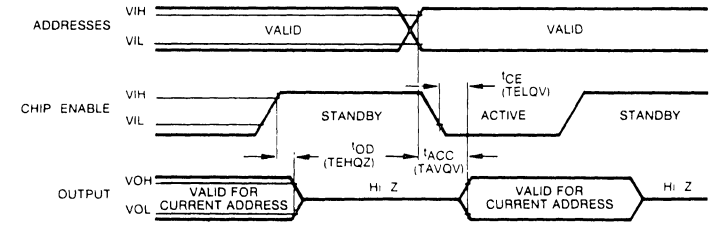
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power-Down Mode ($\overline{OE}$ = VIL)



PROGRAM OPERATION

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (Notes 1 and 2)
(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

Symbol	Parameter	Min	Typ	Max	Units
ILI	Input Leakage Current (Note 3)	–	–	10	μA
VIL	Input Low Level	– 0.1	–	0.8	V
VIH	Input High Level (Note 7)	2.2	–	VCC + 1	V
ICC	VCC Power Supply Current	–	–	10	mA
IPP1	VPP Supply Current (Note 4)	–	–	10	μA
IPP2	VPP Supply Current During Programming Pulse (Note 5)	–	–	30	mA

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes 1, 2, and 6)
(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ±1V)

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	2	–	–	μs
t_{OS}	$\overline{OE}$ Set-up Time	2	–	–	μs
t_{DS}	Data Set-up Time	2	–	–	μs
t_{AH}	Address Hold Time	2	–	–	μs
t_{OH}	$\overline{OE}$ Hold Time	2	–	–	μs
t_{DH}	Data Hold Time	2	–	–	μs
t_{DF}	Output Disable to Output Three state Delay (Note 4)	0	–	100	ns
t_{OE}	Output Enable to Output Delay (Note 4)	–	–	120	ns
t_{PW}	Program Pulse Width	45	50	55	ms
t_{PR}	Program Pulse Rise Time	5	–	–	ns
t_{PF}	Program Pulse Fall Time	5	–	–	ns
t_{VS}	VPP Set-Up Time	2	–	–	μs
t_{VH}	VPP Hold Time	2	–	–	μs

Note 1 : VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2 : Care must be taken to prevent overshoot of the VPP supply when switching to + 26 V max

Note 3 : $0\ V \leqslant VIN \leqslant 5.25V$

Note 4 : $\overline{CE}/PGM$ = VIL, VPP = VCC

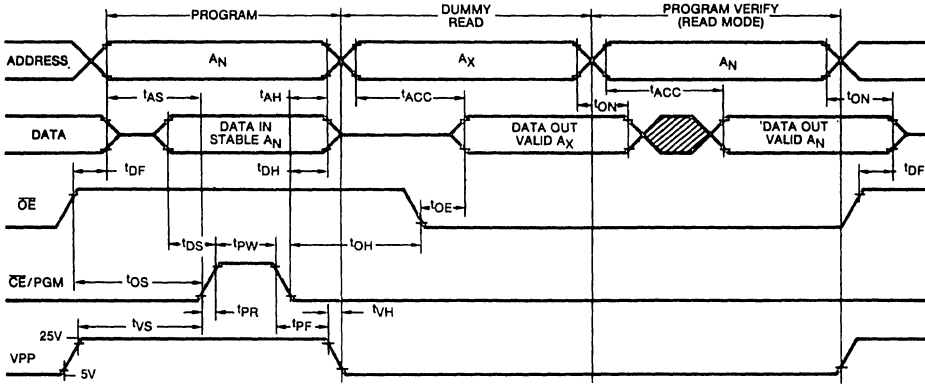
Note 5 : VPP = 26 V

Note 6 : Transition times $\leqslant$ 20 ns unless otherwise noted..

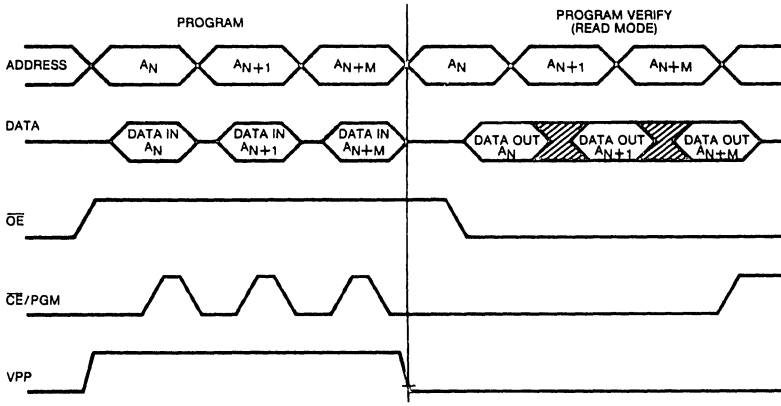
Note 7 : The inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3V to VSS — 0.3V.

PROGRAM TIMING DIAGRAMS

Single Address Programming Followed by a Verify Mode



Multiple Address Programming Followed by a Verify Mode*



* All timings are the same as the single address programming mode. A dummy read is required only if the last programmed byte is the first byte to be verified.

FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The ETC 2716 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The ETC 2716 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

TABLE I. OPERATING MODES (VCC = 5V)

Mode	Pin Name/Number		
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	Outputs 9-11, 13-17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

Deselect Mode

The ETC 2716 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more ETC 2716 for memory expansion.

Standby Mode (Power Down)

The ETC 2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 0.4% of the normal operating power. VCC must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The ETC 2716 is shipped from THOMSON SEMICONDUCTEURS completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

FUNCTIONAL DESCRIPTION (Continued)

TABLE II. PROGRAMMING MODES (VCC = 5V)

Mode	Pin Name/Number			
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	VPP 21	Outputs Q 9-11, 13-17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

Program Mode

The ETC 2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIL = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. ETC 2716 may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the ETC 2716 is verified in the program verify mode which has VPP at VCC (see Table II). **After programming an address, that same address cannot be immediately verified without an address change (dummy read).**

Program Inhibit Mode

The program inhibit mode allows programming several ETC 2716 simultaneously with different data for each one by controlling which ones receive the program pulse.

All similar inputs of the ETC 2716 may be paralleled.

Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

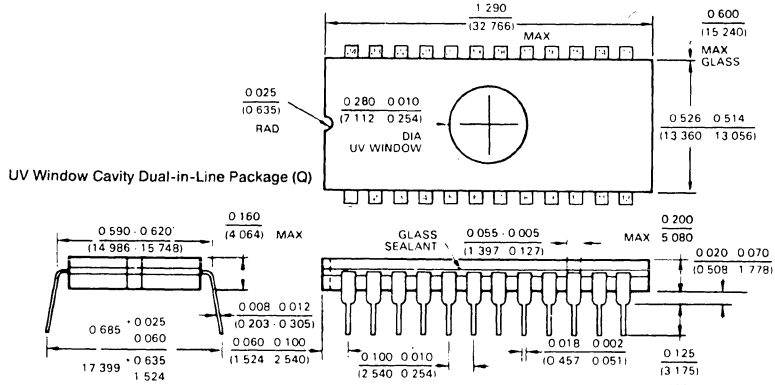
ERASING

The ETC 2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the ETC 2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm^2 power rating is used. The ETC 2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PHYSICAL DIMENSIONS inches (millimeters)



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON COMPONENTS
MOSTEK

ETC2732(Q)-35/45/55

32,768-BIT (4096 x 8) CMOS UV ERASABLE PROM

MEMORY COMPONENTS

The ETC 2732 is a high speed 32K UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

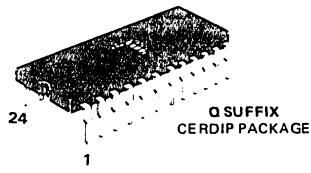
The ETC 2732 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure. This EPROM is fabricated with the reliable, high volume, time proven, P^2 CMOS silicon gate technology.

- CMOS power consumption : 26.25 mW max active power, 0.53 mW max standby power
- 4096 × 8 organization
- Pin compatible to ET 2716, ETC 2716, ET 2732, ET 2764
- Access time down to 350 ns
- Single 5V power supply
- Static - no clocks required
- TTL compatible I/Os during both read and program modes
- Three-state output with OR-tie capability
- Oper. temp. : 0°C, + 70°C ; −20°C, + 70°C (D suffix) ; −25°C, + 70°C (E suffix) ; −40°C, + 85°C (V suffix).

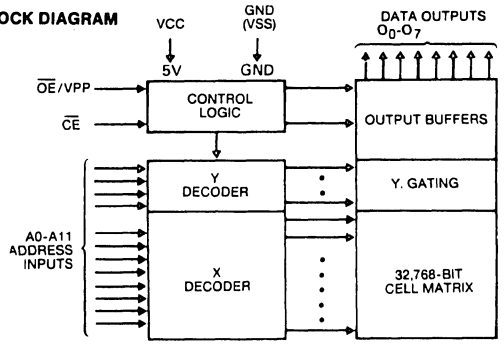
Parameter/Part Number	ETC2732Q-35	ETC2732Q-45	ETC2732Q-55
Access Time (ns)	350	450	500
Active Current (mA at 1 MHz)	5	5	5
Standby Current (mA)	0.1	0.1	0.1

CMOS

(4096 x 8)
32,768 - BIT
UV ERASABLE PROM

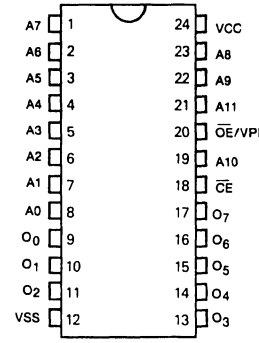


BLOCK DIAGRAM



Mode	Pin Name/Number CE 18	OE/VPP 20	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5V	DOUT
Standby	VIH	Don't Care	5V	Hi-Z
Program	VIL	25V	5V	DIN
Program Verify	VIL	VIL	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

PIN ASSIGNMENT



PIN NAMES

A0-A11	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Read RV, Program 25V
V_{CC}	5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature Under Bias	−10°C to + 80°C	Output Voltages with Respect to VSS	VCC + 0.3V to VSS −0.3V
Storage Temperature	−65°C to +125°C	Power Dissipation	1.0W
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V	Lead Temperature (Soldering, 10 seconds)	300°C
Input Voltages with Respect to VSS except VPP (Note 5)	6V to −0.3V		

READ OPERATION (Note 2)

DC OPERATING CHARACTERISTICS TA = 0°C to + 70°C, VCC = 5V ± 5 %, VSS = 0V, (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
ILI	Input Current	VIN=VCC or GND	–	–	10	μA
ILO	Output Leakage Current	VOUT=VCC or VSS, $\overline{CE}$ = VIH	–	–	10	μA
VIL	Input Low Voltage		−0.1	–	0.8	V
VIH	Input High Voltage	(Note 4)	2.0	–	VCC+1	V
VOL1	Output Low Voltage	IOL=2.1 mA	–	–	0.45	V
VOH1	Output High Voltage	IOH = −400μA	2.4	–	–	V
VOL2	Output Low Voltage	IOL = 0μA	–	–	0.1	V
VOH2	Output High Voltage	IOH = 0μA	VCC−0.1	–	–	V
ICC1	VCC Supply Current Active (TTL Levels)	$\overline{CE}$ = $\overline{OE}$ = VIL Inputs = VIH or VIL Frequency 1 MHz, I/O = 0 mA	–	2	10	mA
ICC2	VCC Supply Current Active (CMOS Levels)	$\overline{CE}$ = $\overline{OE}$ = VIL (Note 4) Inputs=GND or VCC Frequency 1 MHz, I/O = 0 mA	–	1	5	mA
ICCSB1	VCC Supply Current Standby	$\overline{CE}$ = VIH	–	0.1	1	mA
ICCSB2	VCC Supply Current Standby	$\overline{CE}$ = VCC	–	0.01	0.1	mA

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 5 %, VSS = 0V, (Unless otherwise specified)

Symbol	Parameter	Conditions	ETC2732Q-35		ETC2732Q-45		ETC2732Q-55		UNIT
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$/PGM=$\overline{OE}$=VIL	–	350	–	450	–	550	ns
t_{CE}	CE to Output Delay	$\overline{OE}$ = VIL	–	350	–	450	–	550	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL	–	150	–	150	–	150	ns
t_{DF}	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL (Note 5)	0	130	0	130	0	130	ns
t_{OH}	Address to Output Hold	$\overline{CE}$/PGM=$\overline{OE}$=VIL	0	–	0	–	0	–	ns

CAPACITANCE (Note 3) (T_A = +25°C, f = 1 MHz)

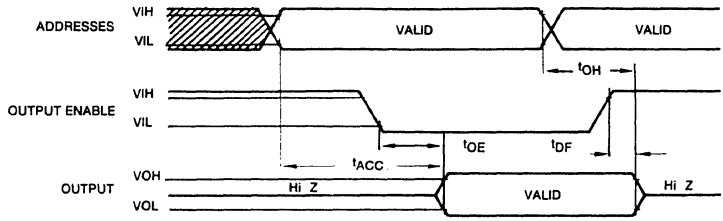
Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	V_{IN} = 0V	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	—	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC TEST CONDITIONS

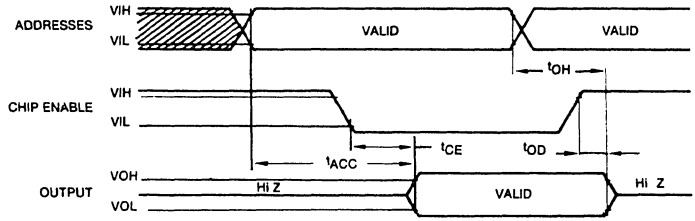
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	< 20 ns
Output Load	1 TTL Gate and CL=100 PF
Input and Output Timing Reference Levels:	0.8V and 2V

SWITCHING TIME WAVEFORMS

Read Cycle ($\overline{CE}$ = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Note 1 : "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2 : Typical conditions are for operation at : TA = 25°C, VCC = 5V, VPP = VCC, and VSS=0V.

Note 3 : Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.

Note 4 : The inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC +0.3V.

Note 5 : The t_{DF} compare level is determined as follows :
High to Hi-Z, the measured V_{OH1} (DC) — 0.10V
Low to Hi-Z, the measured V_{OL1} (DC) + 0.10V

DC PROGRAMMING CHARACTERISTICS (Notes 1 and 2)
TA = +25°C ± 5°C, VCC = 5V ± 5 %, VPP = 25V ± 1V) (Unless otherwise specified)

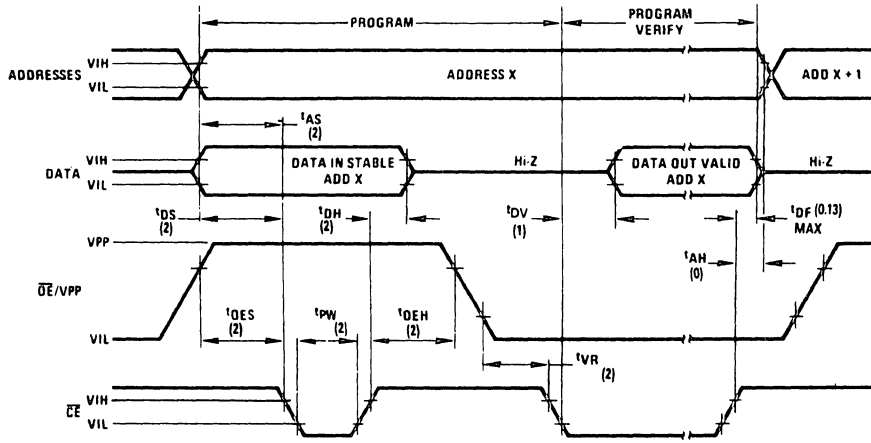
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All inputs)	$V_{IN} = V_{CC}$ or GND	–	–	10	µA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA	–	–	0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ µA	2.4	–	–	V
I_{CC}	V_{CC} Supply Current		–	2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1	–	0.8	V
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)		2.0	–	$V_{CC}+1$	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$	–	–	30	mA

AC PROGRAMMING CHARACTERISTICS (TA = +25°C ± 5°C, VCC = 5V ± 5 %, VPP 25V ± 1V)

Symbol	Parameter	Conditions	Min	Typ	Max	
t_{AS}	Address Set-Up Time		2	–	–	µs
t_{OES}	$\overline{OE}$ Set-Up Time		2	–	–	µs
t_{DS}	Data Set-Up Time		2	–	–	µs
t_{AH}	Address Hold Time		0	–	–	µs
t_{OEH}	$\overline{OE}$ Hold Time		2	–	–	µs
t_{DH}	Data Hold Time		2	–	–	µs
t_{DF}	Chip Enable to Output Float Delay		0	–	130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$;$\overline{OE} = V_{IL}$	–	–	1	µs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50	–	–	ns
t_{VR}	V_{PP} Recovery Time		2	–	–	µs

PROGRAMMING WAVEFORMS

Note : All times shown in parentheses are minimum and in μs unless otherwise specified.
The input timing reference is 0.8V for a V_{IL} and 2V for a V_{IH}.



AC TEST CONDITIONS

V_{CC}	5V ± 5 %
V_{PP}	25V ± 1V
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level Inputs , Outputs	0.8V and 2V

Note 1 : Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The ETC 2732 must not be inserted into or removed from a board with Vpp at 25 ± 1V to prevent damage to the device.

Note 2 : The maximum allowable voltage which may be applied to the Vpp pin during programming is 26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across Vpp,Vcc to GND to suppress spurious voltage transients which may damage the device.

FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The five modes of operation of the ETC 2732 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

Read Mode

The ETC 2732 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The ETC 2732 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53mW. The ETC 2732 is placed in the standby mode, by applying a TTL high signal to the $\overline{CE}$ input when in standby mode the outputs are in a high impedance state, independant of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMS are usually used in larger memory arrays, we have provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for.

a)the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION : Exceeding 26.5V on pin 20 (V_{PP}) will damage the ETC 2732.

Initially, and after each erasure, all bits of the ETC 2732 are in the "1" state. Data is introduced by selectively programming "Os" into the desired bit locations. Although only "Os" will be programmed, both "1s" and "Os" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The ETC 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1 µF capacitor be placed across $\overline{OE}/V_{PP}$, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time-either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms.
The ETC 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple ETC 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled ETC 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled.

Program Inhibit

Programming multiple ETC 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel ETC 2732s may be common. A TTL level program pulse applied to an ETC 2732s $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25 V will program that ETC 2732. A high level $\overline{CE}$ input inhibits the other ETC 2732s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

TABLE I. MODE SELECTION

Mode / Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20	V_{CC} (24)	Outputs (9-11, 13-17)
Read.	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Program	V_{IL}	V_{PP}	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	5	Hi-Z

ERASURE CHARACTERISTICS

The erasure characteristics of the ETC 2732 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 Å – 4000 Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical ETC 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the ETC 2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the ETC 2732 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

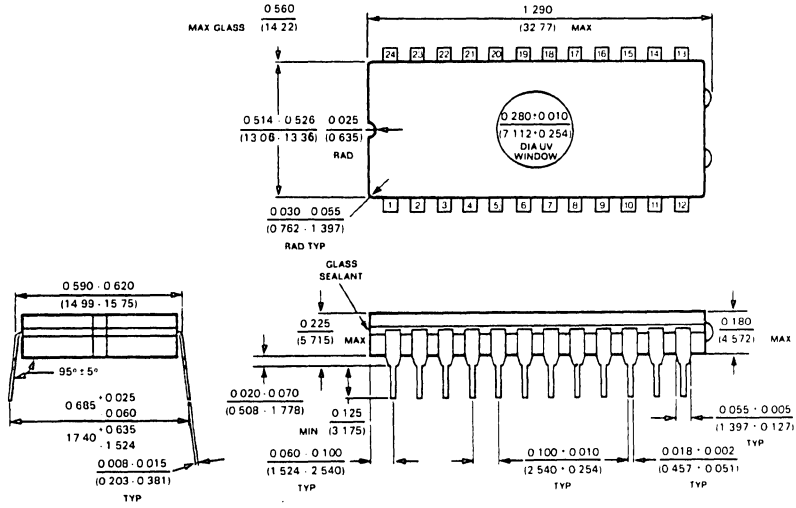
The recommended erasure procedure for the ETC 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm² power rating. The ETC 2732 should be place within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer — the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

PHYSICAL DIMENSIONS inches (millimeters)



UV Window Cavity Dual-In-Line Package (Q)

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

The TS27C64 is a high speed 64K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

The TS27C64 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

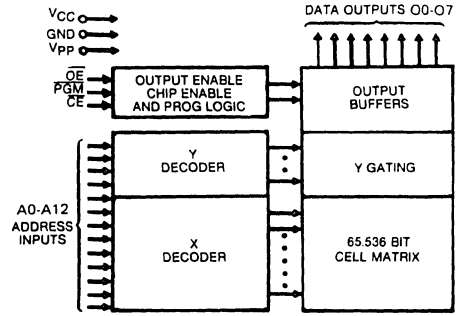
- Fast Access time – 150ns, 200ns, 250ns, 300ns
- Compatible to high speed microprocessors zero wait state
- 28-pin JEDEC approved pin-out
- Low power consumption : active 20 mA (max.)
  standby 1 mA (max.)
- Programming voltage : 12.5 V
- High speed programming (< 1 minute)
- Electronic signature
- Also proposed in plastic packages (OTP)

TABLE 1 : ORDERING INFORMATION

PART NUMBER	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}
TS27C64-15	150	150	75	5V ± 10 %
TS27C64-20	200	200	80	5V ± 10 %
TS27C64-25	250	250	100	5V ± 10 %
TS27C64-30	300	300	120	5V ± 10 %

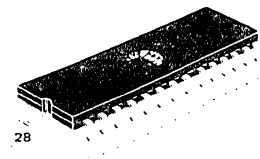
Operating temperature range
0°C to + 70°C (CQ suffix), – 40°C to + 85°C (VQ suffix)
– 55°C to + 125°C (MQ suffix) TS27C64-25MQ TS27C64-30MQ

BLOCK DIAGRAM



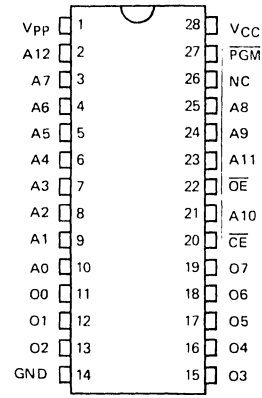
CMOS

65,536-BIT
(8192 x 8)
UV ERASABLE PROM



Q SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0-O7	Outputs
$\overline{PGM}$	Program
NC	Non Connected

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Operating temperature range TS27C64Q TS27C64VQ TS27C64MQ	T_{amb}	T_L to T_H 0 to + 70 − 40 to + 85 −55 to + 125	°C
Storage temperature range	T_{stg}	−65 to + 125	°C
Supply voltage	V_{PP}*	−0.6 to + 14	V
Input voltage A9 Except V_{PP}, A9	V_{in}*	−0.6 to + 13.5 −0.6 to + 6.25	V
Max power dissipation	P_D	1.5	W
Lead temperature (Soldering : 10 seconds)		+ 300	°C

* With respect to V_{SS}

Note 1 : "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.

READ OPERATION (Note 2)

DC CHARACTERISTICS

$T_{amb} = T_L$ to T_H, $V_{CC} = 5\ V \pm 10\ \%$, $V_{SS} = 0\ V$ (Unless otherwise specified)

Characteristic	Symbol	Min	Typ (Note 2)	Max	Unit
Input load current (V_{in}= V_{CC} or GND)	I_{LI}	–	–	10	μA
Ouput leakage current (V_{out}= V_{CC} or V_{SS}, $\overline{CE}$ = V_{IH})	I_{LO}	–	–	10	μA
V_{PP} read voltage	V_{PP}	V_{CC} −0.7	–	V_{CC}	V
Input low voltage	V_{IL}	−0.1	–	0.8	V
Input high voltage (Note 2)	V_{IH}	2.0	–	V_{CC}+ 1	V
Output low voltage I_{OL} = 2.1 mA I_{OL} = 0 μA	V_{OL}	 – –	 – –	 0.45 0.1	V
Output high voltage I_{OH} = −400 μA I_{OH} = 0 μA	V_{OH}	 2.4 V_{CC} − 0.1	 – –	 – –	V
V_{CC} supply active current (TTL levels) $\overline{CE}$ = $\overline{OE}$ = V_{IL}, Inputs = V_{IH} or V_{IL}, f = 5 MHz, I/O = 0 mA	I_{CC2}	–	10	30	mA
V_{CC} supply standby current $\overline{CE}$ = V_{IH} $\overline{CE}$ = V_{CC}	 I_{CCSB1} I_{CCSB2}	 – –	 0.5 10	 1 100	 mA μA
V_{PP} read current (V_{PP} = V_{CC} = 5.5 V)	I_{PP1}	–	–	100	μA

AC CHARACTERISTICS (Notes 3, 4, 5)

$T_{amb} = T_L$ to T_H

Characteristic	Symbol	Min	Maximum values				Unit
			TS27C64 -15	TS27C64 -20	TS27C64 -25	TS27C64 -30	
Address to output delay ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{ACC}	–	150	200	250	300	ns
CE to output delay ($\overline{OE}$ = V_{IL})	t_{CE}	–	150	200	250	300	ns
Output enable to output delay ($\overline{CE}$ = V_{IL})	t_{OE}	–	75	80	100	120	ns
Output enable high to output float ($\overline{CE}$ = V_{IL})	t_{DF} (Note 4)	0	50	50	60	105	ns
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{OH}	0	–	–	–	–	ns

CAPACITANCE (Note 5)
T_{amb} = + 25° C, f = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{in} = 0V)	C_{in}	–	4	6	pF
Output capacitance (V_{out} = 0 V)	C_{out}	–	8	12	pF

Note 2 : Typical conditions are for operation at : T_{amb} = + 25°C, V_{CC} = 5 V, V_{PP} = V_{CC}, and V_{SS} = 0 V

Note 3 : V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}
V_{PP} may be connected to V_{CC} except during program.

Note 4 : The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured V_{OH}(DC) – 0.1V
Low to THREE-STATE the measured V_{OL}(DC) + 0.1V.

Note 5: Capacitance is guaranteed by periodic testing. T_{amb} = + 25° C, f = 1 MHz

AC TEST CONDITIONS (Figure 1,2)

Output Load	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs , Outputs	0.8V and 2V

FIGURE 1 – OUTPUT LOAD CIRCUIT

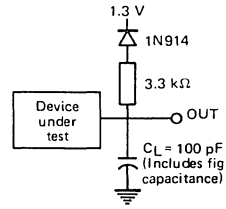
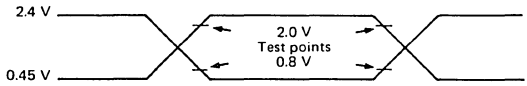
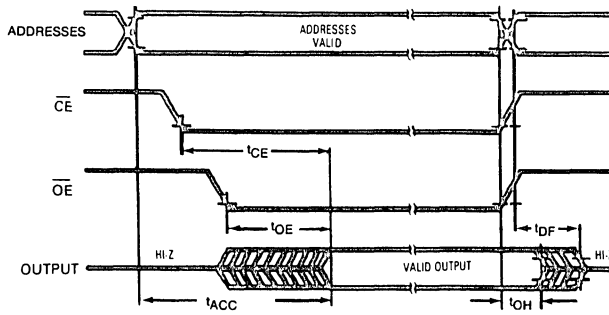


FIGURE 2 – AC TESTING INPUT/OUTPUT WAVEFORM



AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8V for a logic "0".

AC WAVEFORMS (READ MODE)



DC PROGRAMMING CHARACTERISTICS

$T_{amb} = 25 \pm 5°C$, $V_{CC} = 6.0\ V \pm 0.25\ V$, $V_{PP} = 12.5\ V \pm 0.3\ V$ (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Input current (all inputs - $V_I = V_{IL}$ or V_{IH})	I_I	–	–	10	μA
Input low level (all inputs)	V_{IL}	-0.1	–	0.8	V
Input high level	V_{IH}	2.0	–	$V_{CC}+1$	V
Output low voltage during verify ($I_{OL} = 2.1$ mA)	V_{OL}	–	–	0.45	V
Output high voltage during verify ($I_{OH} = -400\ \mu A$)	V_{OH}	2.4	–	–	V
V_{CC} supply current (Program & Verify)	I_{CC3}	–	–	30	mA
V_{PP} supply current (Program - $\overline{CE} = V_{IL} = \overline{PGM}$)	I_{PP2}	–	–	30	mA

AC PROGRAMMING CHARACTERISTICS

$T_{amb} = 25 \pm 5°C$, $V_{CC} = 6.0\ V \pm 0.25\ V$, $V_{PP} = 12.5\ V \pm 0.3\ V$ (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Address set-up time	t_{AS}	2	–	–	μs
$\overline{OE}$ set-up time	t_{OES}	2	–	–	μs
Data set-up time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
Output enable to output float delay	t_{DF}	0	–	130	ns
V_{PP} set-up time	t_{VPS}	2	–	–	μs
V_{CC} set-up time	t_{VCS}	2	–	–	μs
$\overline{PGM}$ initial program pulse width	t_{PW}	0.95	1.0	1.05	ms
$\overline{PGM}$ overprogram pulse width (Note 2)	t_{OPW}	2.85	–	78.75	ms
$\overline{CE}$ set-up time	t_{CES}	2	–	–	μs
Data valid from $\overline{OE}$	t_{OE}	–	–	150	ns

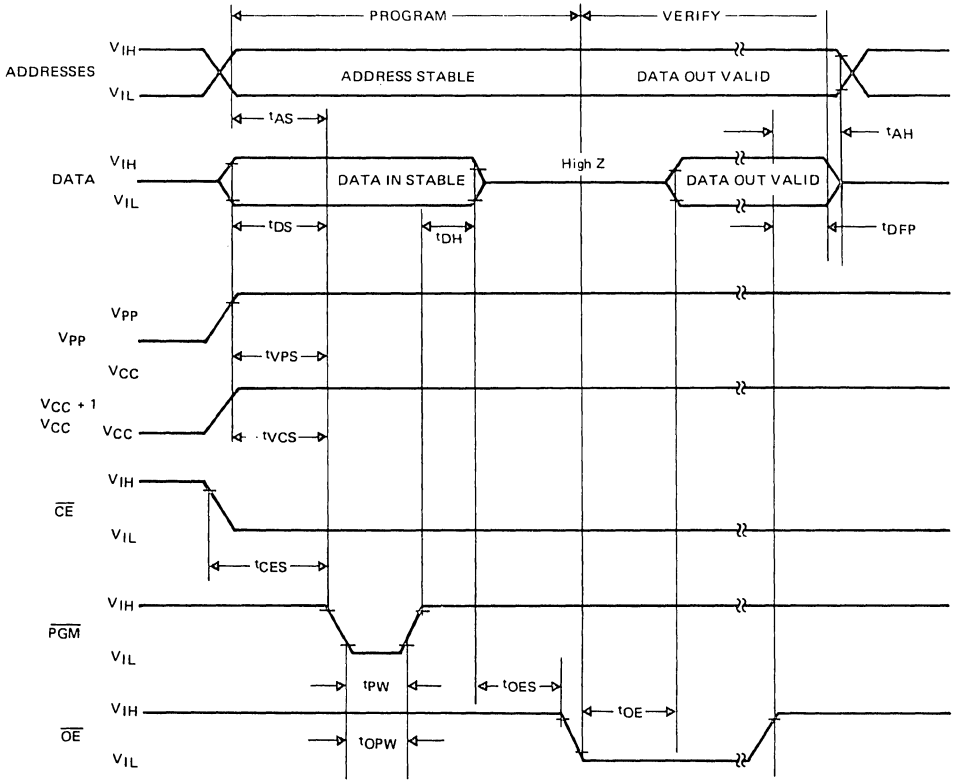
AC TEST CONDITIONS

Input rise and fall times (10% to 90%)	20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Ouptut timing reference level	0.8V and 2.0V

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 2 : t_{OPW} is defined in flow chart.

HIGH SPEED PROGRAMMING WAVE FORMS



1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the TS27C64, a 0.1 µF capacitor is required across Vpp and ground to suppress spurious voltage transients which can damage the device.

TABLE 2. MODE SELECTION

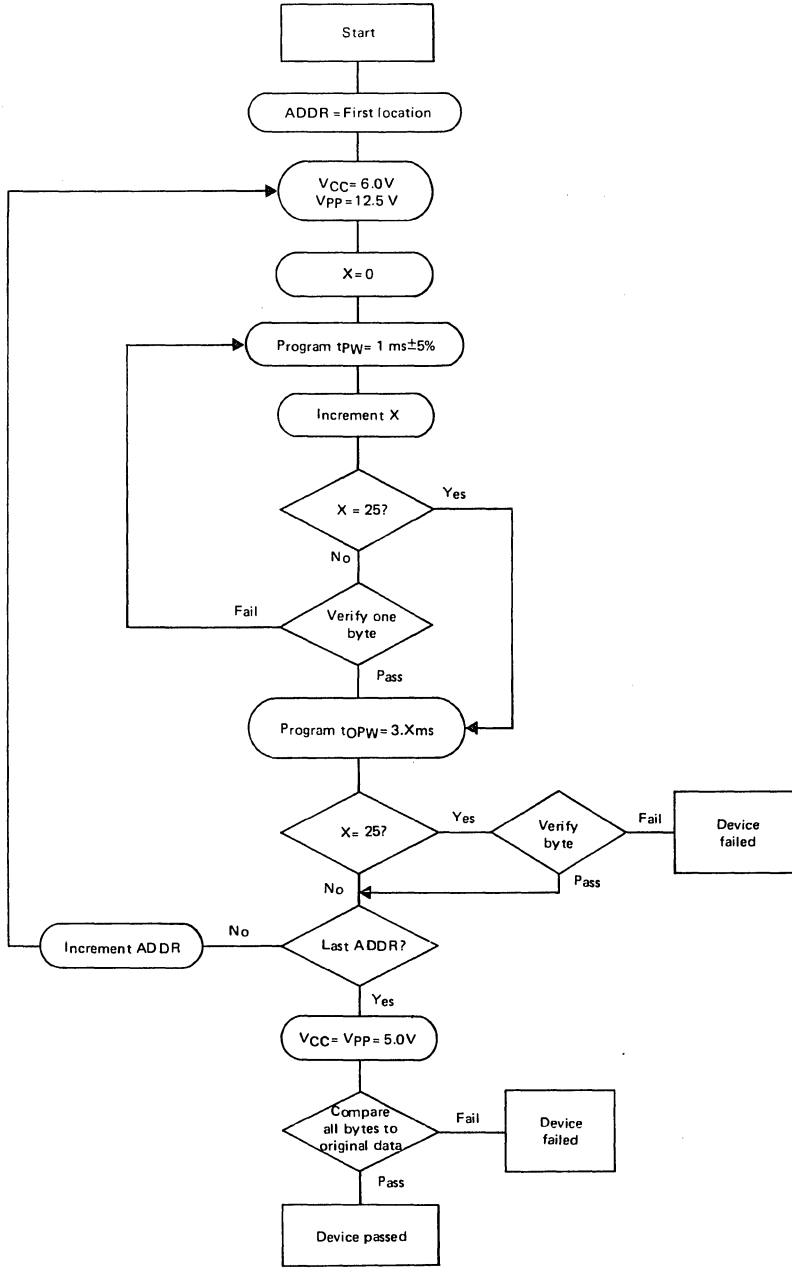
Modes \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs (11-13 15-19)
Read	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	Hi-Z
High speed programming	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	Hi-Z
Electronic signature (Note 3)	V_{IL}	V_{IL}	V_H Note 2	V_{IH}	V_{CC}	V_{CC}	CODE

NOTES : 1 - X can be either V_{IL} or V_{IH}

2 - V_H = 12.0 V ±0.5 V

3 - All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 98) to V_{IH} (type code: 08).

HIGH SPEED PROGRAMMING FLOW CHART



FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The seven modes of operation of the TS27C64 are listed in Table 2. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp.

Read Mode

The TS27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-$t_{\overline{OE}}$.

Standby Mode

The TS27C64 has a standby mode which reduces the maximum power dissipation to 5.5 mW. The TS27C64 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accommodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming modes

CAUTION : Exceeding 14V on pin 1(Vpp) will damage the TS27C64.

Initially, and after each erasure, all bits of the TS27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C64 is in the programming mode when the Vpp input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. It is required that a 0.1 μF capacitor be placed across Vpp, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled TS27C64s.

- **High speed programming**

  The high speed programming algorithm described in the flow chart page 6 rapidly programs TS27C64 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 1 minute.

- **Program inhibit**

  Programming of multiple TS27C64s in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64s may be common. A TTL low-level pulse applied to a TS27C64 $\overline{CE}$ and $\overline{PGM}$ inputs with Vpp at 12.5 V will program that TS27C64.

- **Program verify**

  A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and Vpp at 12.5 V.

- **Electronic signature mode**

  Electronic signature mode allows the reading out of a binary code that will identify the EPROM manufacturer and type.
  This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64.
  To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 (pin 24) of the TS27C64. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

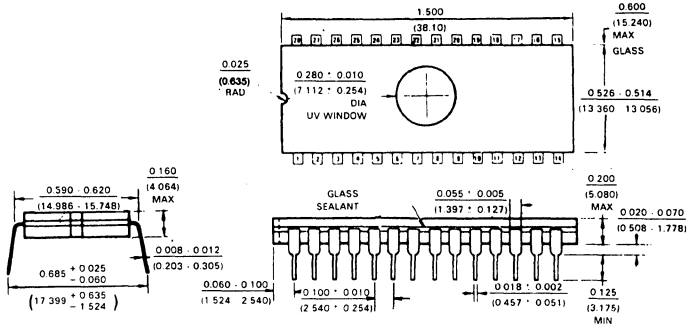
ERASING

The TS27C64 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the TS27C64 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm² power rating is used. The TS27C64 to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PHYSICAL DIMENSIONS inches (millimeters)



THOMSON COMPONENTS
MOSTEK

TS27C256(Q)-15/20/25/30

262,144-BIT (32,768 x 8) CMOS UV ERASABLE PROM

MEMORY COMPONENTS

ADVANCE INFORMATION

The TS27C256 is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.
The TS27C256 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

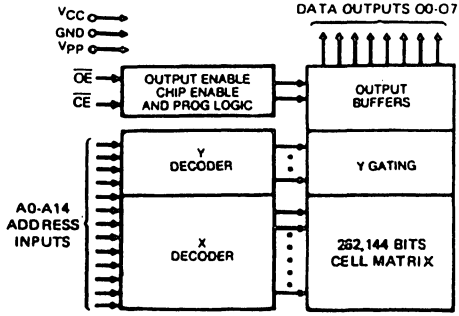
- Fast access time – 150 ns, 200 ns, 250 ns, 300 ns
- Compatible to high speed microprocessors zero wait state
- 28-pin JEDEC approved pin-out
- Low power consumption : active 40 mA (max.)
  standby 1 mA (max.)
- Programming voltage : 12.5 V
- High speed programming
- Electronic signature.
- Will be proposed in plastic packages (OTP)

TABLE 1 – ORDERING INFORMATION

PART NUMBER	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}*
TS27C256-15	150	150	75	5V ± 10 %
TS27C256-20	200	200	75	5V ± 10 %
TS27C256-25	250	250	100	5V ± 10 %
TS27C256-30	300	300	120	5V ± 10 %

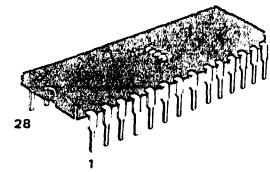
Operating temperature range
0°C to + 70°C (CQ suffix), –40°C to + 85°C (VQ suffix)

BLOCK DIAGRAM



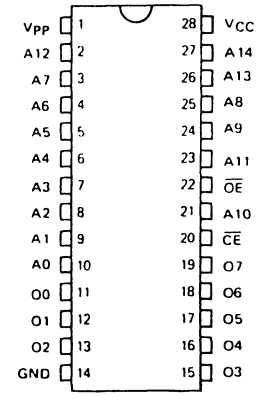
CMOS

262,144 BIT
(32,768 x 8)
UV ERASABLE PROM



Q SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT



PIN NAMES

A0-A14	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0-O7	Outputs

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Operating temperature range TS27C256CQ TS27C256VQ	T_{amb}	T_L to T_H −10 to + 80 −40 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 125	°C
Supply voltage	V_{PP}*	−0.6 to + 14	V
Input voltage A9 Except V_{PP}, A9	V_{in}*	−0.6 to + 13.5 −0.6 to + 6.25	V
Max power dissipation	P_D	1.5	W
Lead temperature (Soldering : 10 seconds)		+ 300	°C

* With respect to V_{SS}

Note 1 : "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.

READ OPERATION (Note 2)

DC CHARACTERISTICS

$T_{amb} = T_L$ to T_H, $V_{CC} = 5\ V \pm 10\ \%$, $V_{SS} = 0\ V$ (Unless otherwise specified)

Characteristic	Symbol	Min	Typ (Note 2)	Max	Unit
Input load current (V_{in}= V_{CC} or GND)	I_{LI}	–	–	10	μA
Ouput leakage current (V_{out}= V_{CC} or V_{SS}, CE = V_{IH})	I_{LO}	–	–	10	μA
V_{PP} read voltage	V_{PP}	V_{CC} −0.7	–	V_{CC}	V
Input low voltage	V_{IL}	−0.1	–	0.8	V
Input high voltage (Note 2)	V_{IH}	2.0	–	V_{CC} + 1	V
Output low voltage I_{OL} = 2.1 mA I_{OL} = 0 μA	V_{OL}	 – –	 – –	 0.45 0.1	V
Output high voltage I_{OH} = −400 μA I_{OH} = 0 μA	V_{OH}	 2.4 V_{CC} − 0.1	 – –	 – –	V
V_{CC} supply active current (TTL levels) $\overline{CE} = \overline{OE} = V_{IL}$, Inputs = V_{IH} or V_{IL}, f = 5 MHz, I/O = 0 mA	I_{CC2}	–	10	40	mA
V_{CC} supply standby current $\overline{CE} = V_{IH}$, $\overline{OE}$ = Inputs = V_{IH} or V_{IL} $\overline{CE} = V_{CC}$ − 0.1 V, $\overline{OE}$ = Inputs = V_{CC} − 0.1 V or V_{SS} + 0.1 V	 I_{CCSB1} I_{CCSB2}	 – –	 0.5 1	 1 10	 mA μA
V_{PP} read current (V_{PP} = V_{CC} = 5.25 V)	I_{PP1}	–	–	10	μA

AC CHARACTERISTICS (Notes 3, 4, 5)

$T_{amb} = T_L$ to T_H

Characteristic	Symbol	Min	Maximum values				Unit
			TS27C256 -15	TS27C256 -20	TS27C256 -25	TS27C256 -30	
Address to output delay ($\overline{CE} = \overline{OE} = V_{IL}$)	t_{ACC}	–	150	200	250	300	ns
CE to output delay ($\overline{OE} = V_{IL}$)	t_{CE}	–	150	200	250	300	ns
Output enable to output delay ($\overline{CE} = V_{IL}$)	t_{OE}	–	75	75	100	120	ns
Output enable high to output float ($\overline{CE} = V_{IL}$)	t_{DF} (Note 4)	0	50	55	60	75	ns
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first ($\overline{CE} = \overline{OE} = V_{IL}$)	t_{OH}	0	–	–	–	–	ns

CAPACITANCE (Note 5)
T_{amb} = + 25° C, f = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{in} = 0V)	C_{in}	–	4	6	pF
Output capacitance (V_{out} = 0 V)	C_{out}	–	8	12	pF

Note 2 : Typical conditions are for operation at : T_{amb} = + 25°C, V_{CC} = 5 V, V_{PP} = V_{CC}, and V_{SS} = 0 V

Note 3 : V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}
V_{PP} may be connected to V_{CC} except during program.

Note 4 : The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured V_{OH}(DC) – 0.1V
Low to THREE-STATE the measured V_{OL}(DC) + 0.1V.

Note 5 : Capacitance is guaranteed by periodic testing. T_{amb} = + 25°C, f = 1 MHz.

AC TEST CONDITIONS (Figure 1,2)

Output Load	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs , Outputs	0.8V and 2V

FIGURE 1 – OUTPUT LOAD CIRCUIT

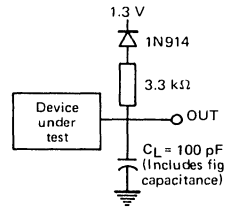
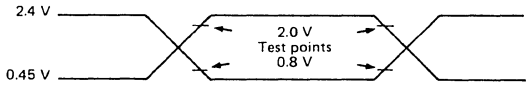
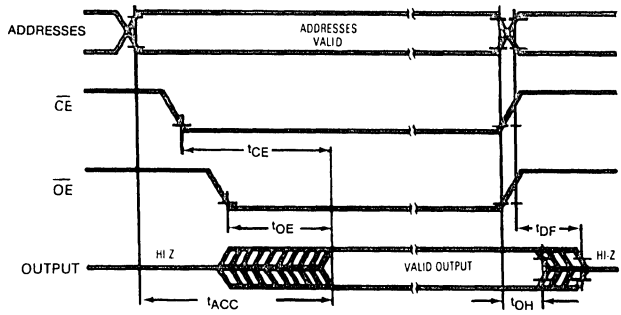


FIGURE 2 – AC TESTING INPUT/OUTPUT WAVEFORM



AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8V for a logic "0".

AC WAVEFORMS (READ MODE)



DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Input current (all inputs - $V_I = V_{IL}$ or V_{IH})	I_I	–	–	10	μA
Input low level (all inputs)	V_{IL}	-0.1	–	0.8	V
Input high level	V_{IH}	2.0	–	V_{CC} + 1	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.45	V
Output high voltage during verify (I_{OH} = -400 μA)	V_{OH}	2.4	–	–	V
V_{CC} supply current (Program & Verify)	I_{CC3}	–	–	40	mA
V_{PP} supply current (Program - $\overline{CE} = V_{IL}$)	I_{PP2}	–	–	30	mA

AC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Address set-up time	t_{AS}	2	–	–	μs
$\overline{OE}$ set-up time	t_{OES}	2	–	–	μs
Data set-up time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
Output enable to output float delay	t_{DF}	0	–	130	ns
V_{PP} set-up time	t_{VPS}	2	–	–	μs
V_{CC} set-up time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial program pulse width	t_{PW}	0.95	1.0	1.05	ms
$\overline{CE}$ overprogram pulse width (Note 2)	t_{OPW}	2.85	–	78.75	ms
Data valid from $\overline{OE}$	t_{OE}	–	–	150	ns

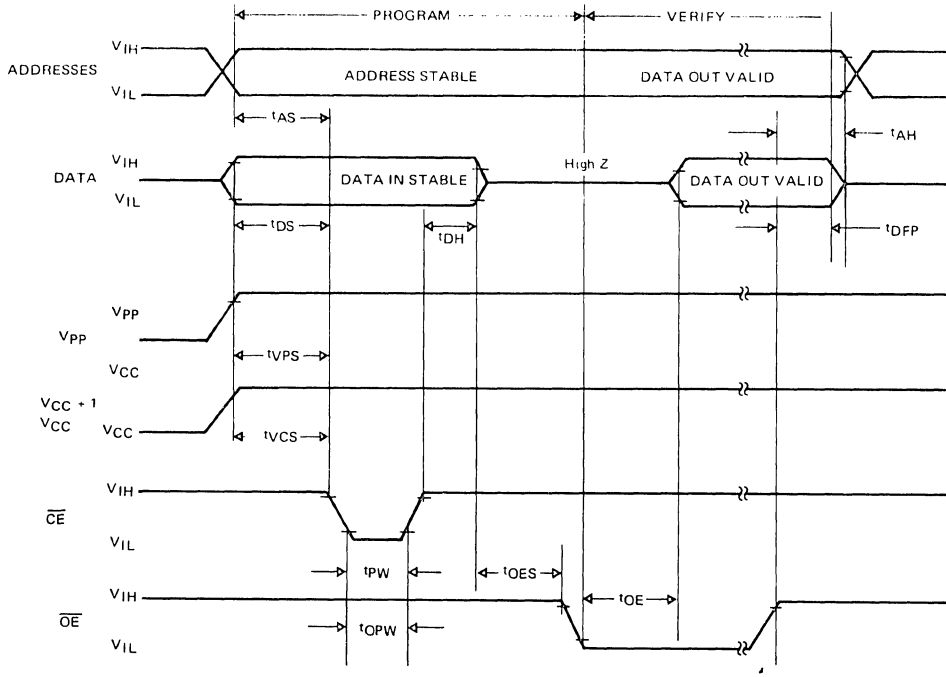
AC TEST CONDITIONS

Input rise and fall times (10% to 90%)	20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Ouptut timing reference level	0.8V and 2.0V

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 2 : t_{OPW} is defined in flow chart.

HIGH SPEED PROGRAMMING WAVE FORMS



1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the TS27C256, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

TABLE 2. MODE SELECTION

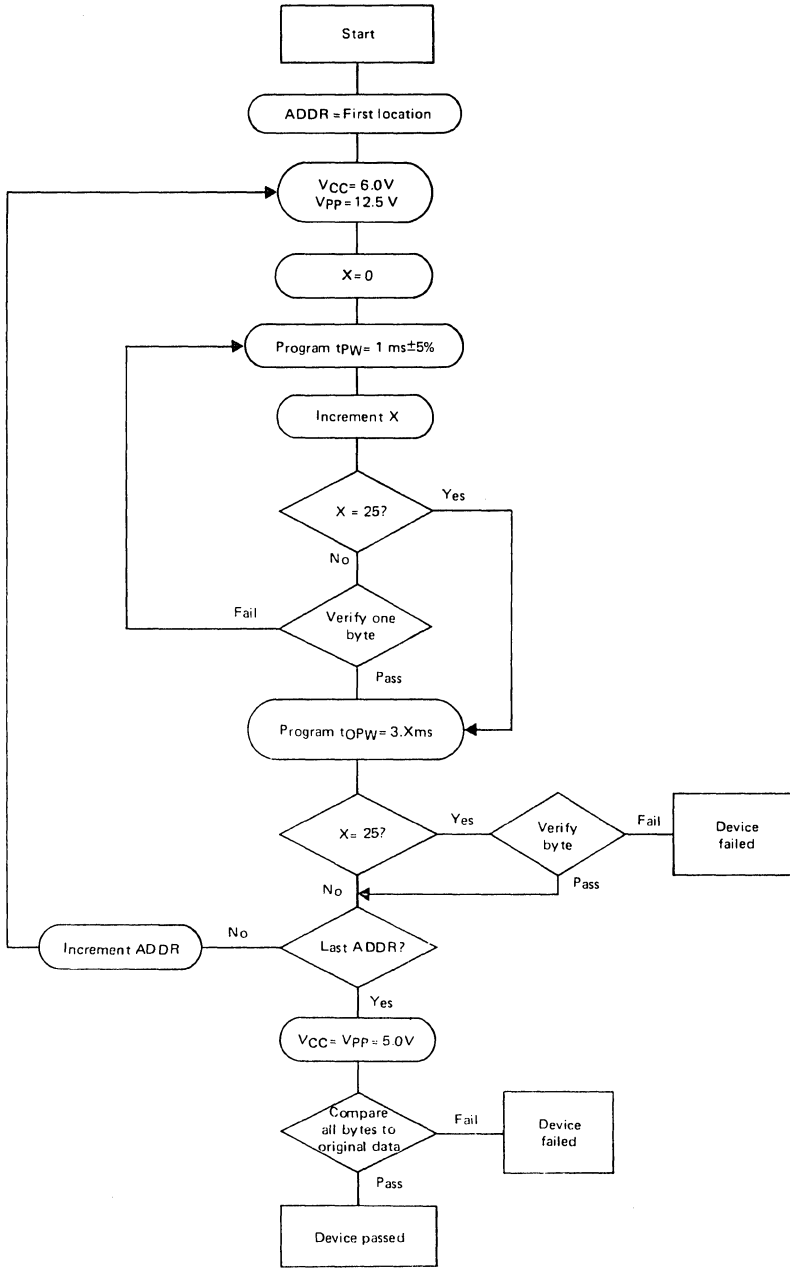
Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
High speed programming	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	Hi-Z
Electronic signature (Note 3)	V_{IL}	V_{IL}	V_H Note 2	V_{CC}	V_{CC}	CODE

NOTES : 1 - X can be either V_{IL} or V_{IH}

2 - V_H = 12.0 V ±0.5 V

3 - All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 9B) to V_{IH} (type code: 04)

HIGH SPEED PROGRAMMING FLOW CHART



DEVICE OPERATION

The seven modes of operation of the TS27C256 are listed in Table 2. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

Read Mode

The TS27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-$t_{\overline{OE}}$.

Standby Mode

The TS27C256 has a standby mode which reduces the maximum power dissipation to 5.25 mW. The TS27C256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accommodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming modes

CAUTION : Exceeding 14V on pin 1(V_{PP}) will damage the TS27C256.

Initialy, and after each erasure, all bits of the TS27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C256 is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ is at TTL low. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled TS27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled TS27C256s.

- **High speed programming**

  The high speed programming algorithm described in the flow chart page 3 rapidly programs TS27C256 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 5 minutes.

- **Program inhibit**

  Programming of multiple TS27C256s in parallel with different data is also easily accomplised by using the program inhibit mode. A high level on $\overline{CE}$ input inhibits the other TS27C256s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C256s may be common. A TTL low level pulse applied to a TS27C256 CE input with V_{PP} at 12.5 V will program that TS27C256.

- **Program verify**

  A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5 V.

- **Electronic signature mode**

  Electronic signature mode allows the reading out of a binary code that will identify the EPROMs manufacturer and type.
  This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C256. To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 (pin 24) of the TS27C256. Two bytes may then be sequenced from the device outputs by toggling address line A0 (Pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

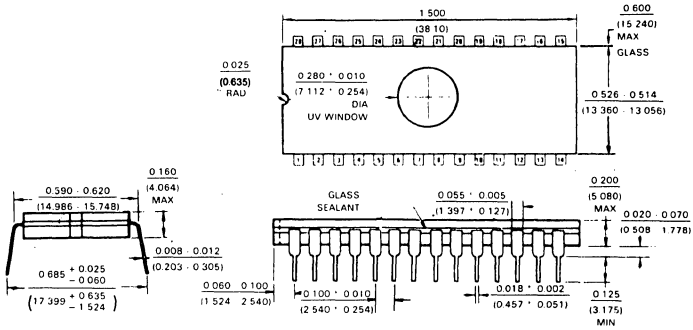
ERASING

The TS27C256 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the TS27C256 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm² power rating is used. The TS27C256 to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PHYSICAL DIMENSIONS inches (millimeters)



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

TS27C1001(Q)-12/15/20/25

131,072 x 8 BIT CMOS UV OR ONE TIME EPROM

PRODUCT PREVIEW

CMOS
131,072 x 8 BITS

UV OR ONE TIME
EPROM

The TS27C1001 is a high speed 1 Mbit UV erasable and electrically reprogrammable EPROM ideally suited for 8 bits microprocessors systems requiring large programs.

— 8 bits outputs:
  - CERDIP 32 pins package with window also proposed in plastic package (one time programmable),
  - 32 pins DIL (600 MILS).

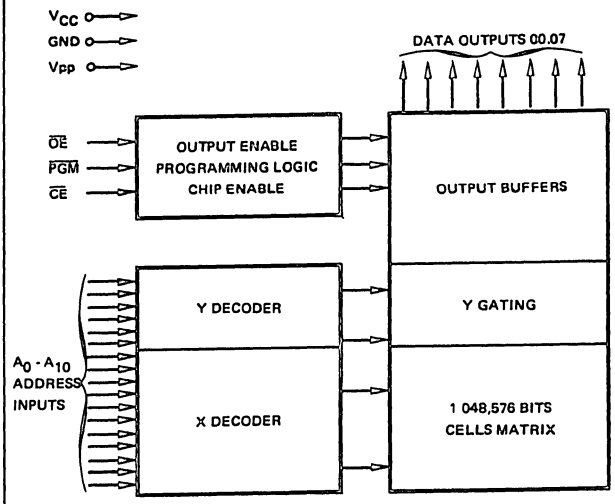
— Fast access time 150 ns.
Low power "CMOS" consumption 50 mA (max.).

— Programming voltage 12.5 V.
Electronic signature for automated programming.
Programming times in the 30 seconds range.

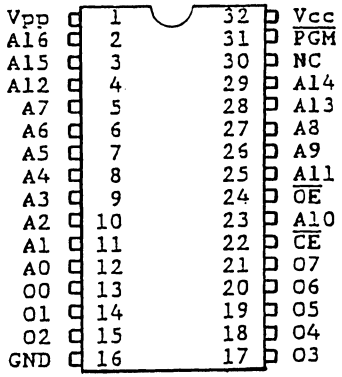
— Easy to implement on all existing 8 bits systems to expand the software or on new sophisticated. Large and very fast systems. Upgrade capability up to 8 Mbits.

Q (CERDIP WITH WINDOW)

BLOCK DIAGRAM



PIN ASSIGNMENT



ORDERING INFORMATION

Part number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}
TS27C1001 - 12	120	120	65	5 V ± 10%
TS27C1001 - 15	150	150	75	5 V ± 10%
TS27C1001 - 20	200	200	75	5 V ± 10%
TS27C1001 - 25	250	250	100	5 V ± 10%

Operating Temperature Range

0°C to + 70°C (C suffix) — 40°C to + 85°C (V suffix)

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

TS27C1024(Q)-12/15/20/25

65.536 x 16 BIT CMOS UV OR ONE TIME EPROM

MEMORY COMPONENTS

PRODUCT PREVIEW

The TS27C1024 is a high speed 1 Mbit UV erasable and electrically reprogrammable EPROM ideally suited for 16 bits or 32 bits microprocessors systems.

— 16 bits outputs:
- CERDIP 40 pins package with window also proposed in plastic package (one time programmable),
- 40 pins DIL (600 MILS),
- 44 pins plastic leaded chip carrier.

— Fast access time 150 ns.
Low power "CMOS" consumption 50 mA (max.).

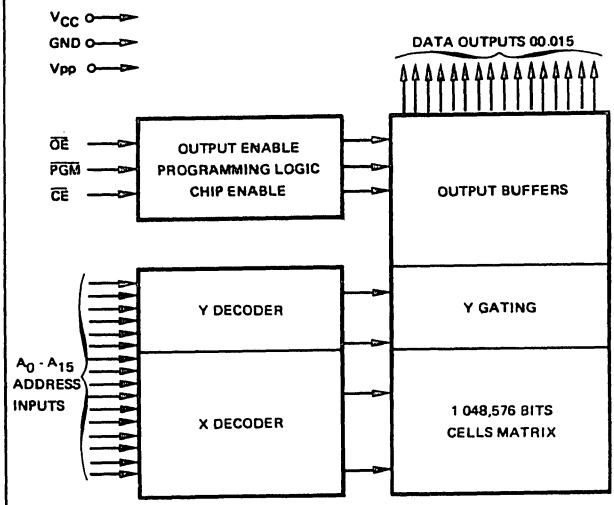
— Programming voltage 12.5 V.
Electronic signature for automated programming.
Programming times in the 30 seconds range.

— Easy layout of the components on printed circuit upgrade capability up to 4 Mbits.

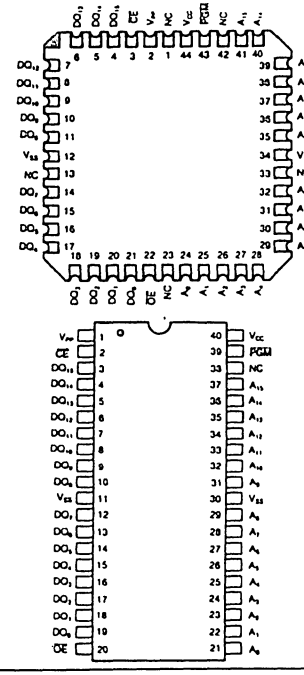
CMOS
65,536 x 16 BITS
UV OR ONE TIME EPROM

Q (CERDIP WITH WINDOW)

BLOCK DIAGRAM



PIN ASSIGNMENT



ORDERING INFORMATION

Part number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}
TS27C1024 - 12	120	120	65	5 V ± 10%
TS27C1024 - 15	150	150	75	5 V ± 10%
TS27C1024 - 20	200	200	75	5 V ± 10%
TS27C1024 - 25	250	250	100	5 V ± 10%

Operating Temperature Range

0°C to + 70°C (C suffix) — 40°C to + 85°C (V suffix)

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

PRODUCT PREVIEW

Main features:

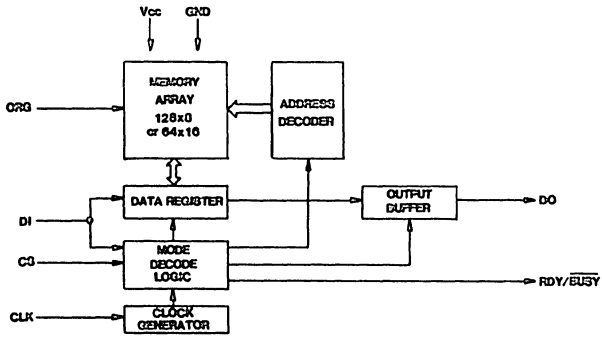
Highly reliable CMOS floating gate technology.
Single 5-volt supply.
Eight pin package.
64 x 16 or 128 x 8 user selectable serial memory.
Compatible with General Instrument GI 5911.
Self timed programming cycle.
Word and chip erasable.
Operating Range 0°C to 70°C.
10,000 erase/write cycles.
Ten year data retention.
Power-on data protection.

1K BIT SERIAL EEPROM

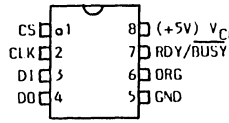
P SUFFIX
PLASTIC PACKAGE

CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Input
ORG	Organization Input
R/$\overline{B}$	Ready/Busy Output
V_{CC}	+ 5 V Power Supply
GND	Ground

TS93C46(P,C)

1K BIT CMOS SERIAL EEPROM

MEMORY COMPONENTS

PRODUCT PREVIEW

Main features:

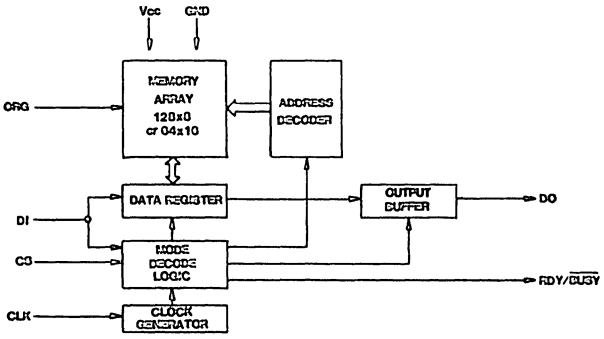
Highly reliable CMOS floating gate technology.
Single 5-volt supply.
Eight pin package.
64 x 16 or 128 x 8 user selectable serial memory.
Compatible with National Semiconducteurs NMC 9346.
Self timed programming cycle.
Word and chip erasable.
Operating Range 0°C to 70°C.
10,000 erase/write cycles.
Ten year data retention.
Power-on data protection.

1K BIT SERIAL EEPROM

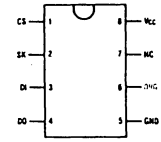
P SUFFIX
PLASTIC PACKAGE

CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

CS	:	Chip Select
SK	:	Clock Input
DI	:	Serial Data Input
DO	:	Serial Data Output
ORG	:	Organization Input
V_{CC}	:	+ 5 V Power Supply
GND	:	Ground
NC	:	No Connect

PRODUCT PREVIEW

DESCRIPTION

The TS28C16A is a fast, low power, 5 V only CMOS EEPROM requiring a simple interface for in-system programming.

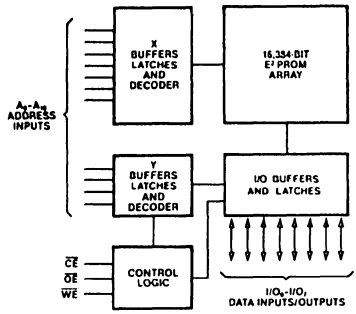
On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time.

The TS28C16A is fabricated in reliable floating gate CMOS technology. It is designed for up to 10,000 write cycles and 10 years data retention.

Main features:

- Very fast access time 150 ns maximum.
- Low CMOS power:
  - active : 25 mA maximum,
  - standby : 100 μA maximum.
- 5 V only operation.
- Simple write operation:
  - on-chip address and data latches,
  - self-timed write cycle with auto-erase,
  - power up/down write protection.
- Fast write cycle time 5 ms max. byte write.
- Reliable floating-gate CMOS technology.
- Operating Range: 0°C to 70°C.

BLOCK DIAGRAM



CMOS
16,384-BIT (2K x 8)
ELECTRICALLY
ERASABLE PROM

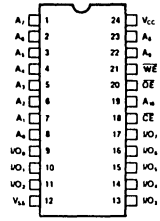
P SUFFIX
PLASTIC PACKAGE

CERAMIC PACKAGE

PIN NAMES

A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground

PIN ASSIGNMENT



PRODUCT PREVIEW

DESCRIPTION

The TS28C17A is a fast, low power, 5 V only CMOS EEPROM requiring a simple interface for in-system programming.

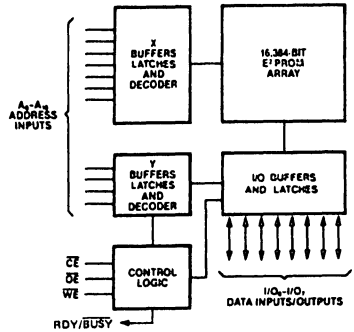
On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Ready/$\overline{Busy}$ output indicates status of chip to the microprocessor. Data polling is provided to allow the user to minimize write cycle time.

The TS28C17A is fabricated in reliable floating gate CMOS technology. It is designed for up to 10,000 write cycles and 10 years data retention.

Main features:

- Very fast access time 150 ns maximum.
- Low CMOS power:
  - active : 25 mA maximum,
  - standby : 100 μA maximum.
- 5 V only operation.
- Simple write operation:
  - on-chip address and data latches,
  - self-timed write cycle with auto-erase,
  - power up/down write protection.
- Ready/$\overline{Busy}$ open drain status output.
- Fast write cycle time 5 ms max. byte write.
- Reliable floating-gate CMOS technology.
- Operating Range: 0°C to 70°C.

BLOCK DIAGRAM



CMOS
16,384-BIT (2K x 8)
ELECTRICALLY
ERASABLE PROM

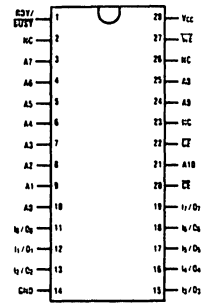
P SUFFIX
PLASTIC PACKAGE

CERAMIC PACKAGE

PIN NAMES

A_0 - A_{10}	Addresses
I/O_0 - I/O_9	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BUSY}$	Device Ready/Busy
NC	No Connect

PIN ASSIGNMENT



PRODUCT PREVIEW

DESCRIPTION

The TS28C64 is a fast, low power, 5 V only CMOS EEPROM requiring a simple interface for in-system programming.

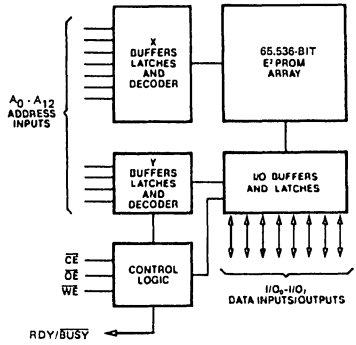
On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Ready/Busy output indicates status of chip to the microprocessor. Data polling is provided to allow the user to minimize write cycle time.

The TS28C64 is fabricated in reliable floating gate CMOS technology. It is designed for up to 10,000 write cycles and 10 years data retention.

Main features:

- Very fast access time 150 ns maximum.
- Low CMOS power:
  - active : 25 mA maximum,
  - standby : 100 μA maximum.
- 5 V only operation.
- Simple write operation:
  - on-chip address and data latches,
  - self-timed write cycle with auto-erase,
  - power up/down write protection.
- Ready/Busy open drain status output.
- Fast write cycle time 5 ms max. byte write.
- Reliable floating-gate CMOS technology.
- Operating Range: 0°C to 70°C.

BLOCK DIAGRAM



CMOS
65,536-BIT (8K x 8)
ELECTRICALLY
ERASABLE PROM

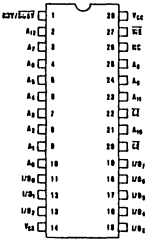
P SUFFIX
PLASTIC PACKAGE

CERAMIC PACKAGE

PIN NAMES

A_0 - A_{12}	Addresses
I/O_0 - I/O_9	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BUSY}$	Device Ready/Busy
NC	No Connect

PIN ASSIGNMENT



TS27C64P-15/20/25/30

65.536-BIT (8192 x 8) CMOS ONE TIME PROGRAMMABLE-ROM

ADVANCE INFORMATION

The TS27C64P is a high speed 64K bits one time electrically programmable ROM ideally suited for applications where fast turn-around is an important requirement.

The TS27C64P is packaged in a 28-pin dual-in-line plastic package and therefore can not be re-written. Programming is performed according to standard THOMSON SEMICONDUCTEURS 64K EPROM procedure.

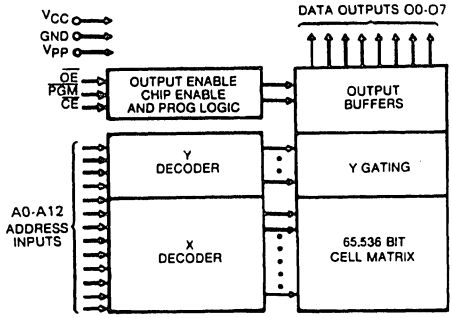
- Compatible to standard TS27C64 (electrical parameters)
- Programming voltage 12.5 V
- High speed programming
- 28-pin JEDEC approved pin-out
- Ideal for automatic insertion
- Also proposed in PLCC (32 pins JEDEC standard)

TABLE 1: ORDERING INFORMATION

PART NUMBER	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}
TS27C64P-15	150	150	75	5V ± 10%
TS27C64P-20	200	200	80	5V ± 10%
TS27C64P-25	250	250	100	5V ± 10%
TS27C64P-30	300	300	120	5V ± 10%

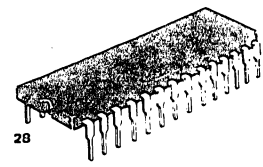
Operating temperature range
0°C to+ 70°C (CP suffix), – 40°C to+ 85°C (VP suffix)
– 40°C to 105°C (TP suffix)

BLOCK DIAGRAM



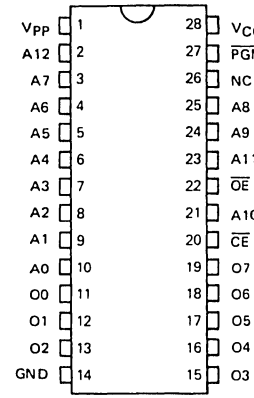
CMOS

65.536-BIT
(8192 x 8)
ONE TIME PROGRAMMABLE-ROM



P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0-O7	Outputs
$\overline{PGM}$	Program
NC	Non Connected

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Operating temperature range TS27C64CP TS27C64VP TS27C64TP	T_{amb}	T_L to T_H 0 to+ 70 − 40 to+ 85 − 40 to+ 105	°C
Storage temperature range	T_{stg}	−65 to + 125	°C
Supply voltage	V_{PP}*	−0.6 to + 14	V
Input voltage A9 Except V_{PP}, A9	V_{in}*	−0.6 to + 13.5 −0.6 to + 6.25	V
Max power dissipation	P_D	1.5	W
Lead temperature (Soldering : 10 seconds)		+ 300	°C

* With respect to V_{SS}

Note 1 : "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.

READ OPERATION (Note 2)

DC CHARACTERISTICS

$T_{amb} = T_L$ to T_H, $V_{CC} = 5$ V ± 10 %, $V_{SS} = 0$ V (Unless otherwise specified)

Characteristic	Symbol	Min	Typ (Note 2)	Max	Unit
Input load current (V_{in}= V_{CC} or GND)	I_{LI}	–	–	10	µA
Ouput leakage current (V_{out}= V_{CC} or V_{SS}, $\overline{CE}$ = V_{IH})	I_{LO}	–	–	10	µA
V_{PP} read voltage	V_{PP}	V_{CC} −0.7	–	V_{CC}	V
Input low voltage	V_{IL}	−0.1	–	0.8	V
Input high voltage (Note 2)	V_{IH}	2.0	–	V_{CC}+ 1	V
Output low voltage I_{OL} = 2.1 mA I_{OL} = 0 µA	V_{OL}	 – –	 – –	 0.45 0.1	V
Output high voltage I_{OH} = −400 µA I_{OH} = 0 µA	V_{OH}	 2.4 V_{CC} − 0.1	 – –	 – –	V
V_{CC} supply active current (TTL levels) $\overline{CE}$ = $\overline{OE}$ = V_{IL}, Inputs= V_{IH} or V_{IL}, f= 5 MHz, I/O= 0 mA	I_{CC2}	–	10	30	mA
V_{CC} supply standby current $\overline{CE}$ = V_{IH} $\overline{CE}$ = V_{CC}	 I_{CCSB1} I_{CCSB2}	 – –	 0.5 10	 1 100	 mA µA
V_{PP} read current (V_{PP}= V_{CC}= 5.5 V)	I_{PP1}	–	–	100	µA

AC CHARACTERISTICS (Notes 3, 4, 5)

$T_{amb} = T_L$ to T_H

Characteristic	Symbol	Min	Maximum values				Unit
			TS27C64 -15	TS27C64 -20	TS27C64 -25	TS27C64 -30	
Address to output delay ($\overline{CE}$= $\overline{OE}$= V_{IL})	t_{ACC}	–	150	200	250	300	ns
CE to output delay ($\overline{OE}$= V_{IL})	t_{CE}	–	150	200	250	300	ns
Output enable to output delay ($\overline{CE}$= V_{IL})	t_{OE}	–	75	80	100	120	ns
Output enable high to output float ($\overline{CE}$= V_{IL})	t_{DF} (Note 4)	0	50	50	60	105	ns
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first ($\overline{CE}$= $\overline{OE}$= V_{IL})	t_{OH}	0	–	–	–	–	ns

CAPACITANCE (Note 5)
T_{amb} = + 25° C, f = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{in} = 0V)	C_{in}	–	4	6	pF
Output capacitance (V_{out} = 0 V)	C_{out}	–	8	12	pF

Note 2 : Typical conditions are for operation at : T_{amb} = + 25°C, V_{CC} = 5 V, V_{PP} = V_{CC}, and V_{SS} = 0 V

Note 3 : V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}
V_{PP} may be connected to V_{CC} except during program.

Note 4 : The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured V_{OH}(DC) – 0.1V
Low to THREE-STATE the measured V_{OL}(DC) + 0.1V.

Note 5: Capacitance is guaranteed by periodic testing. T_{amb} = + 25° C, f = 1 MHz

AC TEST CONDITIONS (Figure 1,2)

Output Load	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs , Outputs	0.8V and 2V

FIGURE 1 – OUTPUT LOAD CIRCUIT

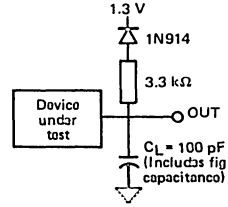
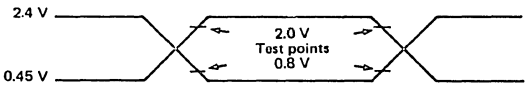
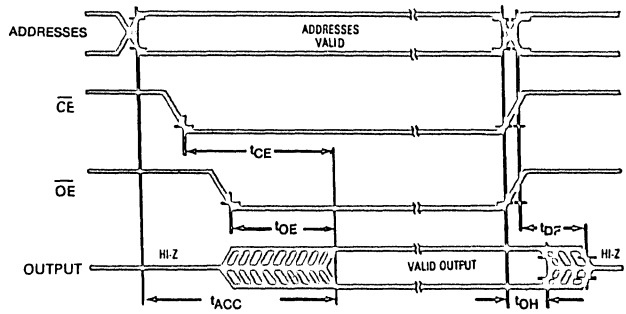


FIGURE 2 – AC TESTING INPUT/OUTPUT WAVEFORM



AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8V for a logic "0".

AC WAVEFORMS (READ MODE)



DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Input current (all inputs - $V_I = V_{IL}$ or V_{IH})	I_I	–	–	10	μA
Input low level (all inputs)	V_{IL}	-0.1	–	0.8	V
Input high level	V_{IH}	2.0	–	V_{CC} + 1	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.45	V
Output high voltage during verify (I_{OH} = -400 μA)	V_{OH}	2.4	–	–	V
V_{CC} supply current (Program & Verify)	I_{CC3}	–	–	30	mA
V_{PP} supply current (Program - $\overline{CE} = V_{IL} = \overline{PGM}$)	I_{PP2}	–	–	30	mA

AC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Address set-up time	t_{AS}	2	–	–	μs
$\overline{OE}$ set-up time	t_{OES}	2	–	–	μs
Data set-up time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
Output enable to output float delay	t_{DF}	0	–	130	ns
V_{PP} set-up time	t_{VPS}	2	–	–	μs
V_{CC} set-up time	t_{VCS}	2	–	–	μs
$\overline{PGM}$ initial program pulse width	t_{PW}	0.95	1.0	1.05	ms
$\overline{PGM}$ overprogram pulse width (Note 2)	t_{OPW}	2.85	–	78.75	ms
$\overline{CE}$ set-up time	t_{CES}	2	–	–	μs
Data valid from $\overline{OE}$	t_{OE}	–	–	150	ns

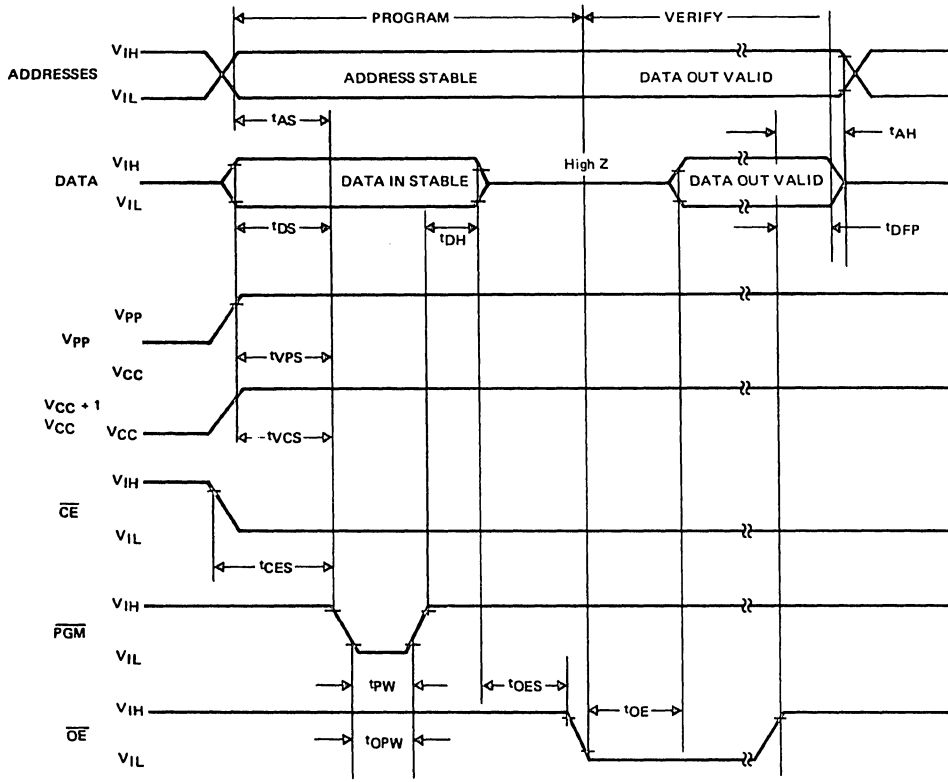
AC TEST CONDITIONS

Input rise and fall times (10% to 90%)	20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Ouptut timing reference level	0.8V and 2.0V

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 2 : t_{OPW} is defined in flow chart.

HIGH SPEED PROGRAMMING WAVE FORMS



1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the TS27C64, a 0.1 µF capacitor is required across Vpp and ground to suppress spurious voltage transients which can damage the device.

TABLE 2. MODE SELECTION

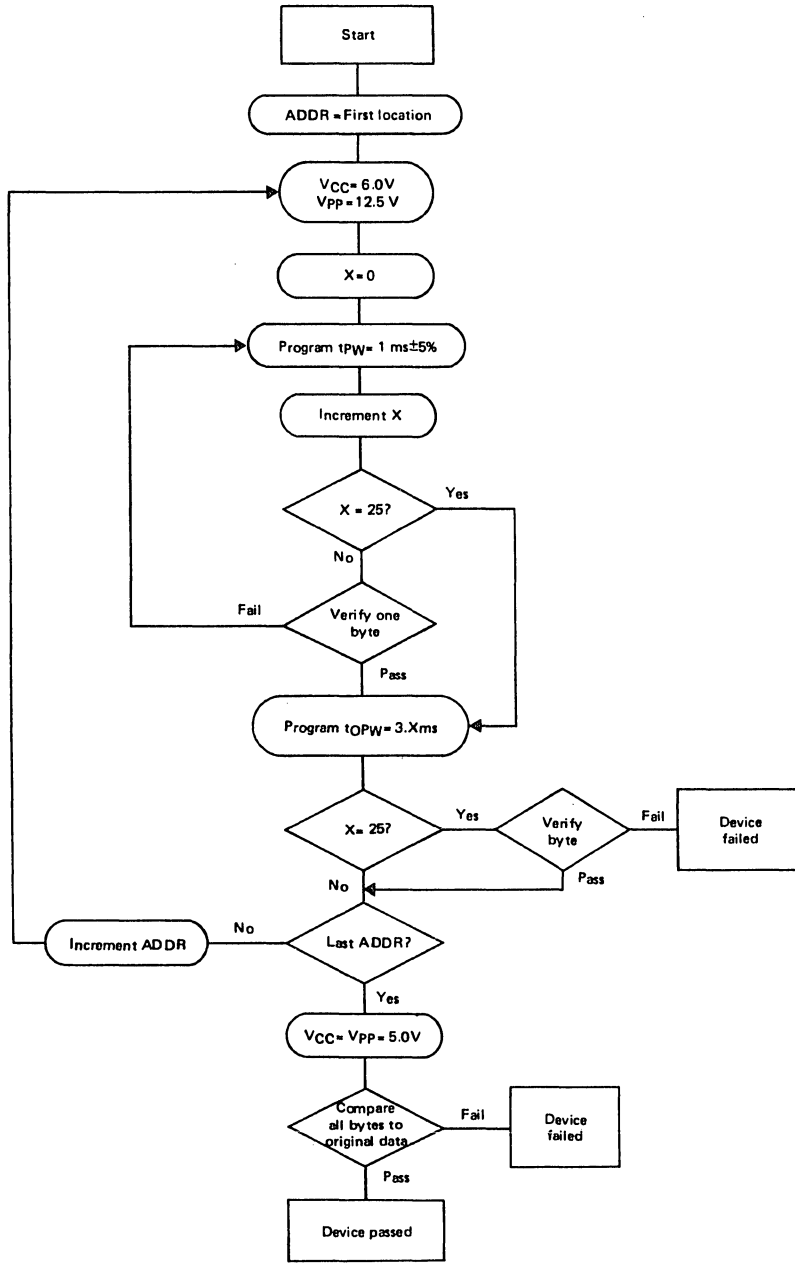
Pins / Modo	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	Vpp (1)	Vcc (20)	Outputs (11-13 15-19)
Read	V_{IL}	V_{IL}	X	V_{IH}	Vcc	Vcc	DOUT
Output disable	V_{IL}	V_{IH}	X	V_{IH}	Vcc	Vcc	Hi-Z
Standby	V_{IH}	X	X	X	Vcc	Vcc	Hi-Z
High speed programming	V_{IL}	V_{IH}	X	V_{IL}	VPP	Vcc	DIN
Program Verify	V_{IL}	V_{IL}	X	V_{IH}	VPP	Vcc	DOUT
Program Inhibit	V_{IH}	X	X	X	VPP	Vcc	Hi-Z
Electronic signature (Note 3)	V_{IL}	V_{IL}	V_H Note 2	V_{IH}	Vcc	Vcc	CODE

NOTES : 1 - X can be either V_{IL} or V_{IH}

2 - V_H = 12.0 V ±0.5 V

3 - All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 9B) to V_{IH} (type code: 08).

HIGH SPEED PROGRAMMING FLOW CHART



FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The seven modes of operation of the TS27C64 are listed in Table 2. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp.

Read Mode

The TS27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-$t_{\overline{OE}}$.

Standby Mode

The TS27C64 has a standby mode which reduces the maximum power dissipation to 5.5 mW. The TS27C64 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accommodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming modes

CAUTION : Exceeding 14V on pin 1(Vpp) will damage the TS27C64.

Initially, and after each erasure, all bits of the TS27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C64 is in the programming mode when the Vpp input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. It is required that a 0.1 μF capacitor be placed across Vpp, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled TS27C64s.

- **High speed programming**

  The high speed programming algorithm described in the flow chart page 6 rapidly programs TS27C64 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 1 minute.

- **Program inhibit**

  Programming of multiple TS27C64s in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64s may be common. A TTL low-level pulse applied to a TS27C64 $\overline{CE}$ and $\overline{PGM}$ inputs with Vpp at 12.5 V will program that TS27C64.

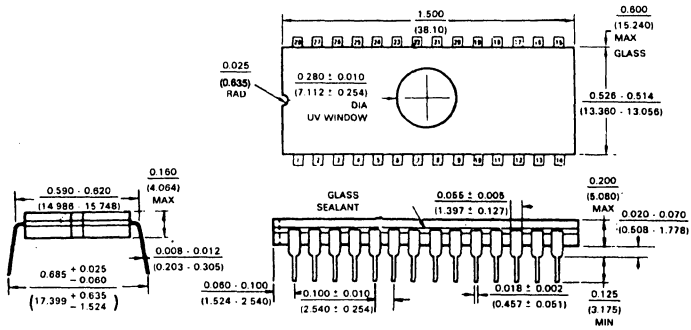
- **Program verify**

  A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and Vpp at 12.5 V.

- **Electronic signature mode**

  Electronic signature mode allows the reading out of a binary code that will identify the EPROM manufacturer and type.
  This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64.
  To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 (pin 24) of the TS27C64. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

PHYSICAL DIMENSIONS inches (millimeters)



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON COMPONENTS
MOSTEK

TS27C256P-20/25/30/35

262,144-BIT (32,768 x 8) CMOS ONE TIME PROGRAMMABLE ROM

MEMORY COMPONENTS

ADVANCE INFORMATION

The TS27C256P is a high speed 256K bits one time electrically pogram-mable ROM ideally suited for applications where fast turn-around is an important requirement.

The TS27C256P is packaged in a 28-pin dual-in-line plastic package and therefore can not be re-written. Programming is performed according to standard THOMSON SEMICONDUCTEURS 256K EPROM procedure.

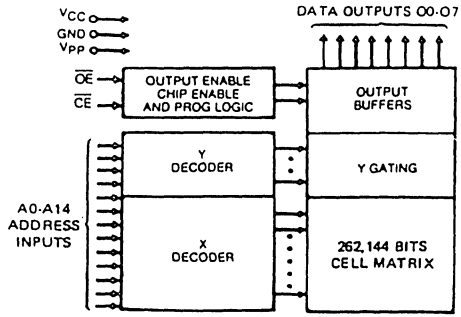
- Compatible to standard TS27C256 (electrical parameters)
- Programming voltage 12.5 V
- High speed programming
- 28-pin JEDEC approved pin-out
- Ideal for automatic insertion
- Also proposed in PLCC (32 pins JEDEC standard)

TABLE 1 – ORDERING INFORMATION

PART NUMBER	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}*
TS27C256-20	200	200	75	5V ± 10 %
TS27C256-25	250	250	100	5V ± 10 %
TS27C256-30	300	300	120	5V ± 10 %
TS27C256-35	350	350	120	5V ± 10 %

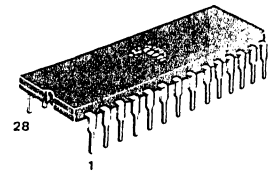
Operating temperature range
0°C to + 70°C (CP suffix), – 40°C to + 85°C (VP suffix)
– 40°C to 105°C (TP suffix)

BLOCK DIAGRAM



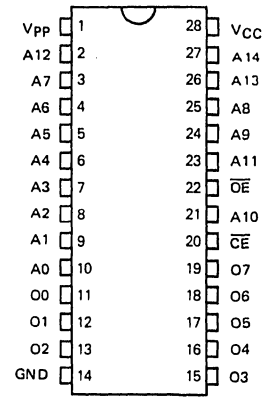
CMOS

262,144 BIT
(32,768 x 8)
ONE TIME PROGRAMMABLE-ROM



P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0-O7	Outputs

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Operating temperature range TS27C256 CP TS27C256 VP TS27C256 TP	T_{amb}	T_L to T_H 0 to+ 70 −40 to + 85 − 40 to+ 105	°C
Storage temperature range	T_{stg}	−65 to + 125	°C
Supply voltage	V_{PP}*	−0.6 to + 14	V
Input voltage A9 Except V_{PP}, A9	V_{in}*	−0.6 to + 13.5 −0.6 to + 6.25	V
Max power dissipation	P_D	1.5	W
Lead temperature (Soldering : 10 seconds)		+ 300	°C

* With respect to V_{SS}

Note 1 : "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.

READ OPERATION (Note 2)

DC CHARACTERISTICS

$T_{amb} = T_L$ to T_H, $V_{CC} = 5$ V ± 10 %, $V_{SS} = 0$ V (Unless otherwise specified)

Characteristic	Symbol	Min	Typ (Note 2)	Max	Unit
Input load current (V_{in}= V_{CC} or GND)	I_{LI}	–	–	10	µA
Ouput leakage current (V_{out}= V_{CC} or V_{SS}, $\overline{CE}$ = V_{IH})	I_{LO}	–	–	10	µA
V_{PP} read voltage	V_{PP}	V_{CC} −0.7	–	V_{CC}	V
Input low voltage	V_{IL}	−0.1	–	0.8	V
Input high voltage (Note 2)	V_{IH}	2.0	–	V_{CC}+ 1	V
Output low voltage I_{OL}= 2.1 mA I_{OL}= 0 µA	V_{OL}	 –	 –	 0.45	V
		–	–	0.1	
Output high voltage I_{OH}= −400 µA I_{OH}= 0 µA	V_{OH}	 2.4	 –	 –	V
		V_{CC} − 0.1	–	–	
V_{CC} supply active current (TTL levels) $\overline{CE}$ = $\overline{OE}$ = V_{IL}, Inputs= V_{IH} or V_{IL}, f= 5 MHz, I/O= 0 mA	I_{CC2}	–	10	40	mA
V_{CC} supply standby current $\overline{CE}$ = V_{IH}, $\overline{OE}$ = Inputs = V_{IH} or V_{IL} $\overline{CE}$ = V_{CC} − 0.1V, $\overline{OE}$ = Inputs = V_{CC} − 0.1V or V_{SS} + 0.1V	 I_{CCSB1} I_{CCSB2}	 – –	 0.5 1	 1 10	 mA µA
V_{PP} read current (V_{PP}= V_{CC}= 5.25 V)	I_{PP1}	–	–	10	µA

AC CHARACTERISTICS (Notes 3, 4, 5)

$T_{amb} = T_L$ to T_H

Characteristic	Symbol	Min	Maximum values				Unit
			TS27C256 -15	TS27C256 -20	TS27C256 -25	TS27C256 -30	
Address to output delay ($\overline{CE}$= $\overline{OE}$= V_{IL})	t_{ACC}	–	150	200	250	300	ns
CE to output delay ($\overline{OE}$= V_{IL})	t_{CE}	–	150	200	250	300	ns
Output enable to output delay ($\overline{CE}$= V_{IL})	t_{OE}	–	75	75	100	120	ns
Output enable high to output float ($\overline{CE}$= V_{IL})	t_{DF} (Note 4)	0	50	55	60	75	ns
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first ($\overline{CE}$= $\overline{OE}$= V_{IL})	t_{OH}	0	–	–	–	–	ns

CAPACITANCE (Note 5)
T_{amb} = + 25° C, f = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{in} = 0V)	C_{in}	–	4	6	pF
Output capacitance (V_{out} = 0 V)	C_{out}	–	8	12	pF

Note 2 : Typical conditions are for operation at : T_{amb} = + 25°C, V_{CC} = 5 V, V_{PP} = V_{CC}, and V_{SS} = 0 V

Note 3 : V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}
V_{PP} may be connected to V_{CC} except during program.

Note 4 : The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured V_{OH}(DC) – 0.1V
Low to THREE-STATE the measured V_{OL}(DC) + 0.1V.

Note 5 : Capacitance is guaranteed by periodic testing. T_{amb} = + 25° C, f = 1 MHz.

AC TEST CONDITIONS (Figure 1,2)

Output Load	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs , Outputs	0.8V and 2V

FIGURE 1 – OUTPUT LOAD CIRCUIT

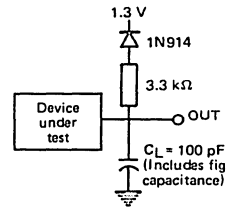
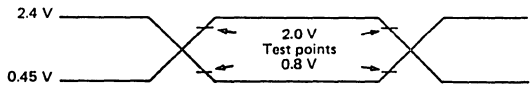
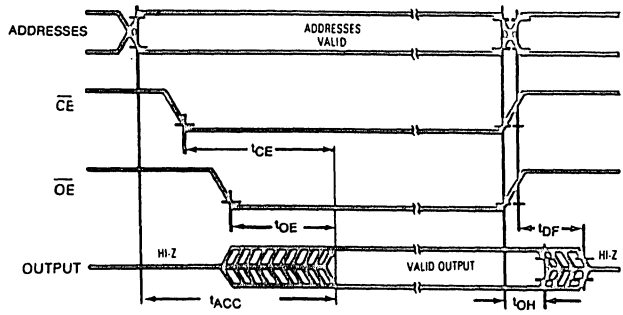


FIGURE 2 – AC TESTING INPUT/OUTPUT WAVEFORM



AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8V for a logic "0".

AC WAVEFORMS (READ MODE)



HIGH SPEED PROGRAMMING CHARACTERISTICS

DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Input current (all inputs - $V_I = V_{IL}$ or V_{IH})	I_I	–	–	10	μA
Input low level (all inputs)	V_{IL}	-0.1	–	0.8	V
Input high level	V_{IH}	2.0	–	V_{CC} + 1	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.45	V
Output high voltage during verify (I_{OH} = -400 μA)	V_{OH}	2.4	–	–	V
V_{CC} supply current (Program & Verify)	I_{CC3}	–	–	40	mA
Vpp supply current (Program - $\overline{CE} = V_{IL}$)	I_{PP2}	–	–	30	mA

AC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Address set-up time	t_{AS}	2	–	–	μs
$\overline{OE}$ set-up time	t_{OES}	2	–	–	μs
Data set-up time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
Output enable to output float delay	t_{DF}	0	–	130	ns
Vpp set-up time	t_{VPS}	2	–	–	μs
V_{CC} set-up time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial program pulse width	t_{PW}	0.95	1.0	1.05	ms
$\overline{CE}$ overprogram pulse width (Note 2)	t_{OPW}	2.85	–	78.75	ms
Data valid from $\overline{OE}$	t_{OE}	–	–	150	ns

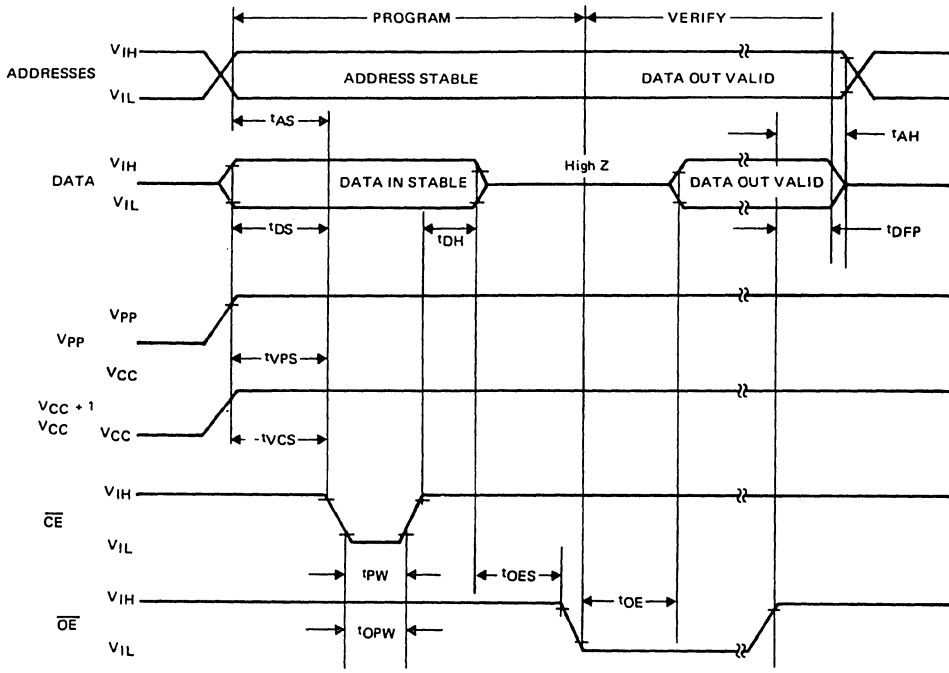
AC TEST CONDITIONS

Input rise and fall times (10% to 90%)	20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Ouptut timing reference level	0.8V and 2.0V

Note 1 : V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after V_{PP}.

Note 2 : t_{OPW} is defined in flow chart.

HIGH SPEED PROGRAMMING WAVE FORMS



1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the TS27C256, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

TABLE 2. MODE SELECTION

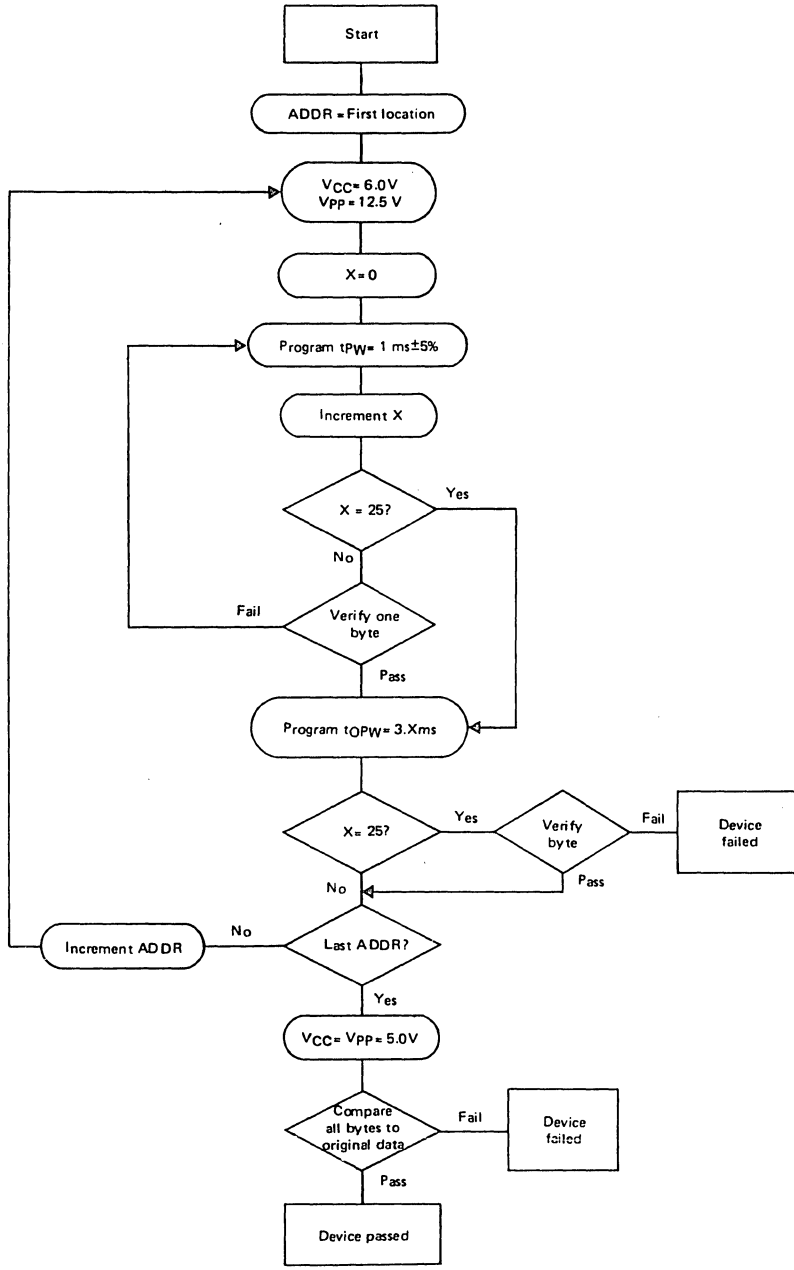
Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
High speed programming	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	Hi-Z
Electronic signature (Note 3)	V_{IL}	V_{IL}	V_H Note 2	V_{CC}	V_{CC}	CODE

NOTES : 1 - X can be either V_{IL} or V_{IH}

2 - V_H = 12.0 V ± 0.5 V

3 - All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 98) to V_{IH} (type code: 04)

HIGH SPEED PROGRAMMING FLOW CHART



FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The seven modes of operation of the TS27C256 are listed in Table 2. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

Read Mode

The TS27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-$t_{\overline{OE}}$.

Standby Mode

The TS27C256 has a standby mode which reduces the maximum power dissipation to 5.25 mW. The TS27C256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accommodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming modes

CAUTION : Exceeding 14V on pin 1(V_{PP}) will damage the TS27C256.

Initialy, and after each erasure, all bits of the TS27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C256 is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ is at TTL low. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled TS27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled TS27C256s.

- **High speed programming**

  The high speed programming algorithm described in the flow chart page 3 rapidly programs TS27C256 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 5 minutes.

- **Program inhibit**

  Programming of multiple TS27C256s in parallel with different data is also easily accomplised by using the program inhibit mode. A high level on $\overline{CE}$ input inhibits the other TS27C256s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C256s may be common. A TTL low level pulse applied to a TS27C256 CE input with V_{PP} at 12.5 V will program that TS27C256.

- **Program verify**

  A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5 V.

- **Electronic signature mode**

  Electronic signature mode allows the reading out of a binary code that will identify the EPROMs manufacturer and type.
  This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C256. To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 (pin 24) of the TS27C256. Two bytes may then be sequenced from the device outputs by toggling address line A0 (Pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

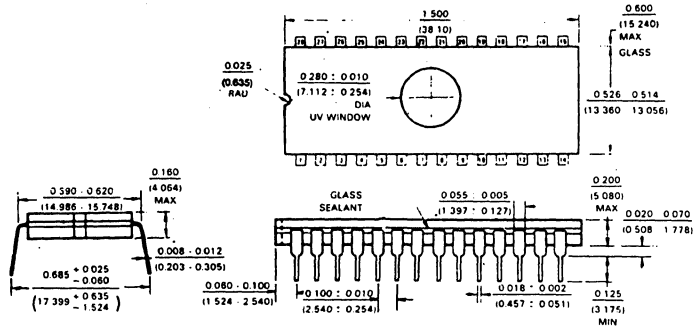
ERASING

The TS27C256 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the TS27C256 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm² power rating is used. The TS27C256 to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PHYSICAL DIMENSIONS inches (millimeters)



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

CHAPTER 3 - BIPOLAR PROMs

FAST PROM

Description	Part number	Organization	Access Time	Output	Page
8K FAST PROM	TS71180A	1K x 8	45 ns	Open collector	3-5
	TS71180B	1K x 8	35 ns	Open collector	
	TS71180C	1K x 8	25 ns	Open collector	
	TS71181A	1K x 8	45 ns	3-state	
	TS71181B	1K x 8	35 ns	3-state	
	TS71181C	1K x 8	25 ns	3-state	
	TS71280A	1K x 8	45 ns	Open collector	
	TS71280B	1K x 8	35 ns	Open collector	
	TS71280C	1K x 8	25 ns	Open collector	
	TS71281A	1K x 8	45 ns	3-state	
	TS71281B	1K x 8	35 ns	3-state	
	TS71281C	1K x 8	25 ns	3-state	
16K FAST PROM	TS71190	2K x 8	80 ns	Open collector	3-11
	TS71190A	2K x 8	60 ns	Open collector	
	TS71190B	2K x 8	45 ns	Open collector	
	TS71190C	2K x 8	35 ns	Open collector	
	TS71191	2K x 8	80 ns	3-state	
	TS71191A	2K x 8	60 ns	3-state	
	TS71191B	2K x 8	45 ns	3-state	
	TS71191C	2K x 8	35 ns	3-state	
	TS71290C	2K x 8	35 ns	Open collector	
	TS71291C	2K x 8	35 ns	3-state	
32K FAST PROM	TS71321B	4K x 8	55 ns	3-state	3-17
	TS71321C	4K x 8	45 ns	3-state	
64K FAST PROM	TS71640	8K x 8	55 ns	Open collector	3-23
	TS71641	8K x 8	55 ns	3-state	

THOMSON COMPONENTS MOSTEK

TS71180 • TS71181 • TS71280 • TS71281(P,C,J)-C/B/A

8192-BIT (1024 x 8) FAST PROM

MEMORY COMPONENTS

PRODUCT PREVIEW

The TS71180, 71181, 71280, 71281 are programmable read-only memories (PROM) organized in 1024 words by 8-bit configuration and are field programmable. They are shipped in an unprogrammed form and have "0" in all locations.

These PROM's are available with open collector (TS71180/71280) or three state outputs (TS71181/71281).

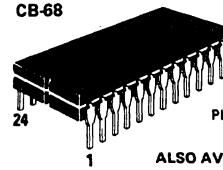
- Fast access times :
  Address access time : 25 ns max (TS71180C-71181C-71280C-71281C)
  35 ns max (TS71180B-71181B-71280B-71281B)
  45 ns max (TS71180A-71181A-71280A-71281A)
- Low voltage programming
- Highly reliable fuses Ti/W for ultra-fast programming
- Low power Schottky technology (oxide isolation process)
- TTL compatible
- Industry standard pin configuration.

APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

8 K FAST PROMs

CASES

CB-68



TS71180
TS71181

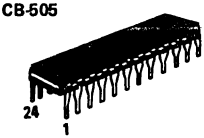
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

C SUFFIX
CERAMIC PACKAGE

CB-505



TS71280
TS71281

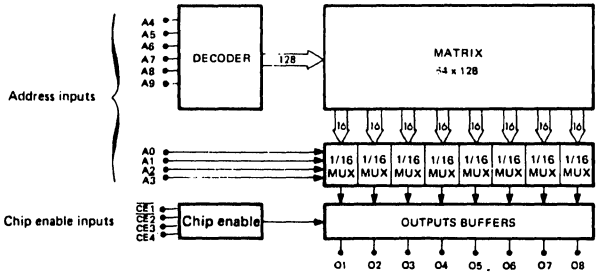
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

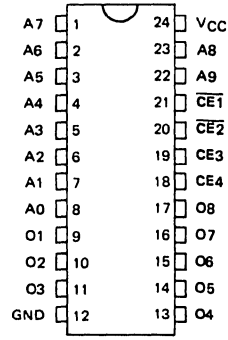
J SUFFIX
CERDIP PACKAGE

C SUFFIX
CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	7 ± 5 %	7 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (V_{CC} = V_{CC} max, V_O = 0) (Note 1)	I_{SC}	- 20	–	- 70	- 15	–	- 85	mA
Low level output voltage (V_{CC} = V_{CC} min, I_{OL} = 16 mA, V_I = V_{IH} or V_{IL})	V_{OL}	–	–	0.45	–	–	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	–	175	–	–	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, CE2 = CE3 = 0.4 V)								
V_O = 5.5 V 71180/71280	I_{OFF}	–	–	+ 40	–	–	+ 60	µA
V_O = 5.5 V 71181/71281	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V 71181/71281	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

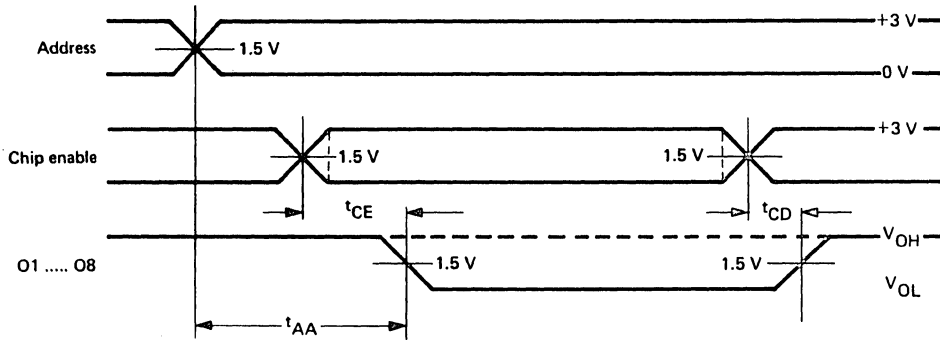
Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

Note 2 : These parameters are not 100 % tested, but are periodically sampled.

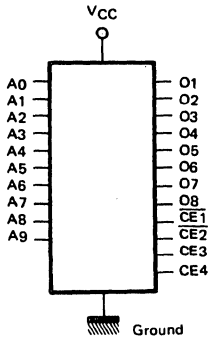
SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

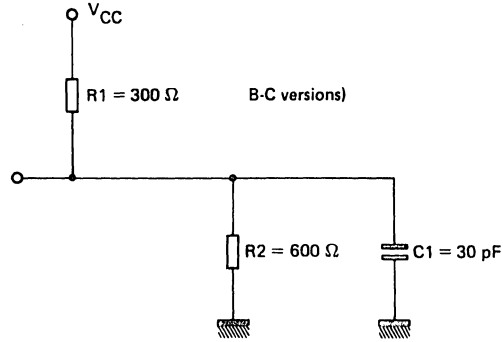
Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Address access time (A0-A9) → (O1....O8)	t_{AA}							ns
TS71180A, TS71181A, TS71280A, TS71281A		–	–	45	–	–	70	
TS71180B, TS71181B, TS71280B, TS71281B		–	–	35	–	–	50	
TS71180C, TS71181C, TS71280C, TS71281C		–	–	25	–	–	30	
Chip enable access time ($\overline{CE1}$, $\overline{CE2}$, CE3, CE4) → (O1....O8)	t_{CE}							ns
TS71180A, TS71181A, TS71280A, TS71281A		–	–	30	–	–	40	
TS71180B, TS71181B, TS71280B, TS71281B		–	–	25	–	–	30	
TS71180C, TS71181C, TS71280C, TS71281C		–	–	20	–	–	25	
Chip disable time ($\overline{CE1}$, $\overline{CE2}$, CE3, CE4) → (O1....O8)	t_{CD}							ns
TS71180A, TS71181A, TS71280A, TS71281A		–	–	30	–	–	40	
TS71180B, TS71181B, TS71280B, TS71281B		–	–	25	–	–	30	
TS71180C, TS71181C, TS71280C, TS71281C		–	–	20	–	–	25	

READING SEQUENCE



DYNAMIC TEST



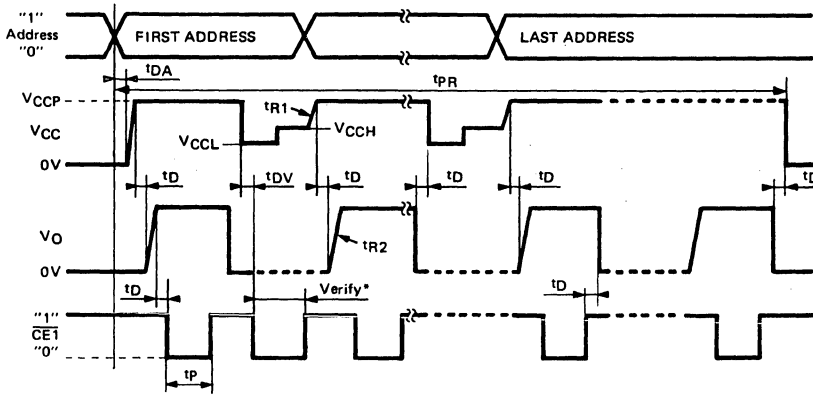


PROGRAMMING CHARACTERISTICS

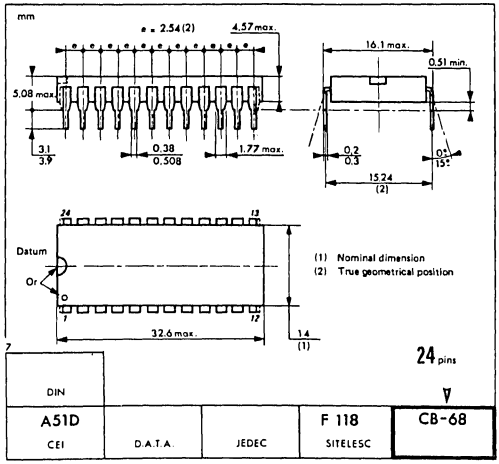
Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} programming pulse	V_{CCP}	12.5	–	13	V
V_{CC} during verify	V_{CCL} V_{CCH}	4.5 –	– –	– 5.5	V V
Programming supply current (V_{CCP} = 12.75 ± 0.25 V)	I_{CCP}	–	420	550	mA
Input voltage	V_{IL} V_{IH}	0 2.4	– –	0.5 5.5	V V
Output programming voltage	V_O	11.5	12	12.5	V
Output programming current (V_O = 12 ± 0.5)	I_O	–	1.5	–	mA
V_{CC} pulse rise time	t_{R1}	5	–	10	µs
Output pulse rise time	t_{R2}	10	–	20	µs
$\overline{CE1}$ programming pulse width	t_P	40	50	60	µs
Address set-up time / V_{CCP}	t_{DA}	100	–	–	ns
Pulse sequence delay	t_D	10	–	–	µs
Delay time before verify	t_{DV}	3	–	–	µs
Programming time (V_{CC} = V_{CCP})	t_{PR}	–	–	10	s
Allowed fusing attempts		–	–	1	

1. Select the address to be programmed. Apply $\overline{CE1}$ = H ; CE2 = H ; CE3 = H.
2. After a delay $t_{DA} \geq 100$ ns, raise V_{CC} to V_{CCP} = 12.75 V ± 0.25 V.
3. After a delay $t_D \geq 10$ µs, apply V_O = 12 ± 0.5 V to the output to be programmed. Program one output at the time. Other outputs are open.
4. After a delay $t_D \geq 10$ µs, apply a logic low level to the $\overline{CE1}$ input. This level will be held during t_P = 50 ± 10 µs.
5. After a delay $t_D \geq 10$ µs, remove output voltage V_O from the output to be programmed.
6. After a delay $t_D \geq 10$ µs, lower the voltage V_{CCP} to V_{CC} = 5 ± 0.5 V.
7. After a delay $t_{DV} \geq 3$ µs, apply a logic low level to the $\overline{CE1}$ input and verify that the programmed output remains in the high state for V_{CCH} = 5.5 V and V_{CCL} = 4.5 V (*). Then, apply a logic high level to the $\overline{CE1}$ chip select input.
8. Repeat steps 1 through 7 to program other locations of the PROM.

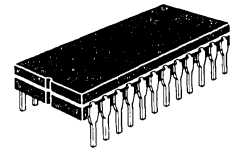
TYPICAL PROGRAMMING SEQUENCE



* Programming verification at both max and min V_{CC} is optional (V_{CCH}, V_{CCL}).



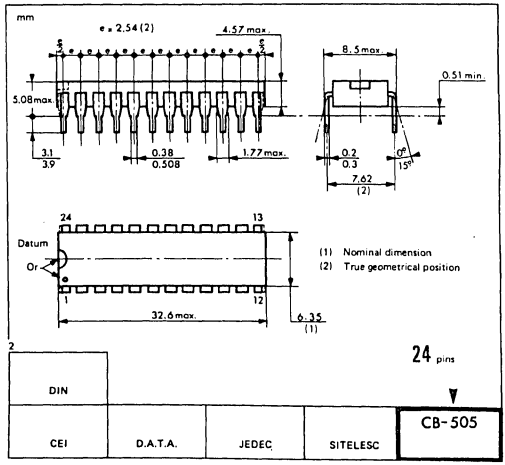
CB-68



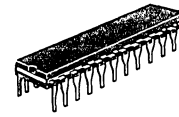
TS71180
TS71181

C SUFFIX
CERAMIC PACKAGE

ALSO AVAILABLE
J SUFFIX
CERDIP PACKAGE



CB-505



TS71280
TS71281

C SUFFIX
CERAMIC PACKAGE

ALSO AVAILABLE

J SUFFIX	**P SUFFIX**
CERDIP PACKAGE	PLASTIC PACKAGE

ORDERING INFORMATION

TS71181C | C | P | -D

- TS71181C: Part number
- C: Oper. temp.
- P: Package
- -D: Screening class

The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER		OPER. TEMP.		PACKAGE				SCREENING CLASS			
		C	M	P	J	C	E	Std	-D	G/B	B/B
45 ns	TS71180A, TS71181A	●		●	●			●	●		
	TS71280A, TS71281A	●		●	●			●	●		
35 ns	TS71180B, TS71181B	●		●	●			●	●		
	TS71280B, TS71281B,	●		●	●			●	●		
25 ns	TS71180C, TS71181C	●		●	●			●	●		
	TS71280C, TS71281C	●		●	●			●	●		

Examples : TS71181CP, TS71181CP-D, TS71181CJ, TS71181CJ-D

Oper. temp. : C : 0°C to +70°C, **M :** −55°C to +125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic DIL, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **-D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.

TS71190 • TS71191 • TS71290 • TS71291(P,C,J,E)-C/B/A

16.384-BIT (2048 x 8) FAST PROM

MEMORY COMPONENTS

ADVANCE INFORMATION

The TS71190, 71191, 71290, 71291 are programmable read-only memories (PROM) organized in a 2048 words by 8-bit configuration and are field programmable. They are shipped in an unprogrammed form and have "0" in all locations.
These PROM's are available with open collector (TS71190/71290) or three state outputs (TS71191/71291).

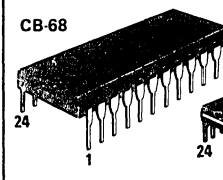
- Fast access times :
  Address access time : 80 ns max. (TS71190, TS71191)
  60 ns max. (TS71190A, TS71191A)
  45 ns max. (TS7190B, TS71191B)
  35 ns max. (TS71190C, TS71191C)
  (TS71290C, TS71291C)
- Temperature compensating circuits to achieve a wide range of operation
- Low voltage programming
- Highly reliable fuses Ti/W for ultra-fast programming
- Low power Schottky technology
- TTL compatible
- Industry standard pin configuration.

APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

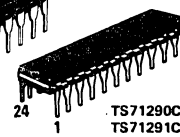
16 K FAST PROMs

CASES

CB-68



CB 505



TS71290C
TS71291C

P SUFFIX
PLASTIC PACKAGE

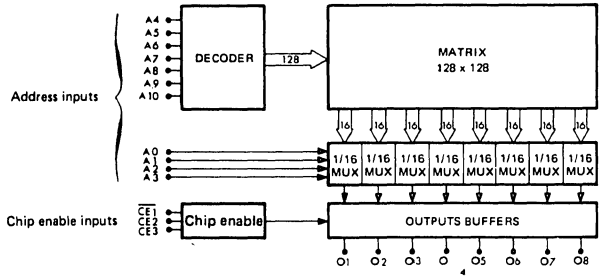
ALSO AVAILABLE
C SUFFIX CERAMIC PACKAGE
J SUFFIX CERDIP PACKAGE

CB-707

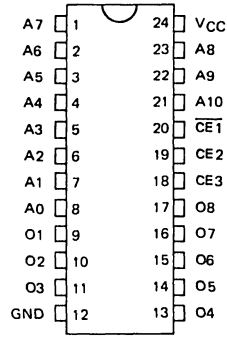
TS71191A,B

E SUFFIX
TRICECOP (LCC)
CHIP CARRIER PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



A0 to A10 : Address inputs
$\overline{CE1}$, CE2, CE3 : Chip enable inputs
V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	7 ± 5 %	7 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (Note 1)	I_{SC}							
V_{CC} = V_{CC} max, V_O = 0 71191,A,B,C		- 20	–	- 70	- 15	–	- 85	mA
71291								
Low level output voltage (V_{CC} = V_{CC} min, V_I = V_{IH} or V_{IL})	V_{OL}							
I_{OL} = 9.6 mA 71190,A		–	0.35	0.45	–	0.35	0.5	V
I_{OL} = 16 mA 71190B,C / 71191B,C / 71290C / 71291C		–	0.35	0.45	–	0.35	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	135	175	–	135	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, $CE2$ = $CE3$ = 0.4 V)								
V_O = 5.5 V 71190,A,B,C/71290C	I_{OFF}	–	–	+ 40	–	–	+ 60	µA
V_O = 5.5 V 71191,A,B,C/71291C	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V 71191,A,B,C/71291C	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

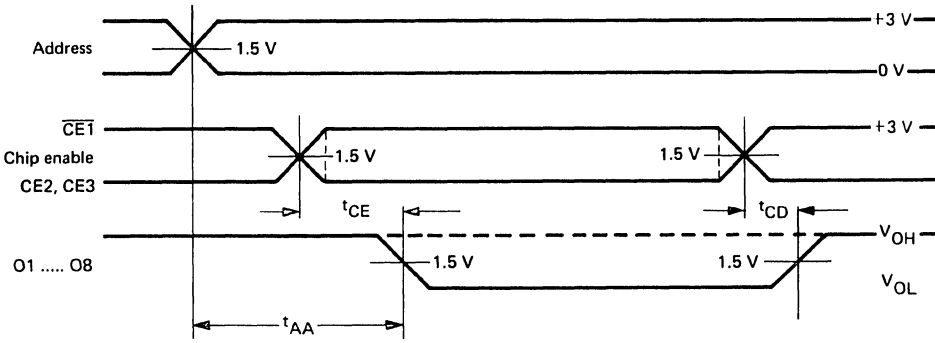
Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

Note 2 : These parameters are not 100 % tested, but are periodically sampled.

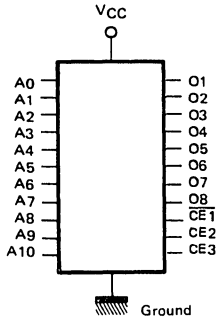
SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

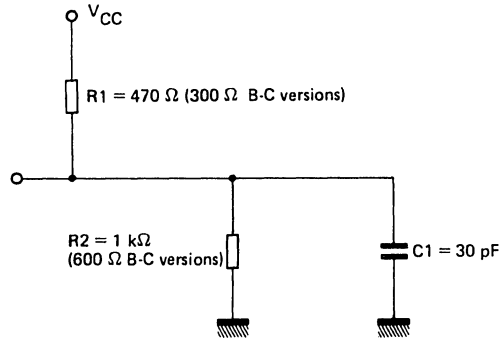
Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Address access time (A0 - A10) ⟶ (O1 ..... O8)	t_{AA}							ns
TS71190 - TS71191		–	40	80	–	50	100	
TS71190A - TS71191A		–	40	60	–	50	80	
TS71190B, TS71191B		–	–	45	–	–	65	
TS71190C, TS71191C TS71290C, TS71291C		–	–	35	–	–	55	
Chip enable access time ($\overline{CE1}$, CE2, CE3) ⟶ (O1 ..... O8)	t_{CE}							ns
TS71190,A/TS71191,A		–	20	35	–	20	45	
TS71190B, TS71191B		–	–	30	–	–	35	
TS71190C, TS71191C TS71290C, TS71291C		–	–	25	–	–	30	
Chip disable time ($\overline{CE1}$, CE2, CE3) ⟶ (O1 ..... O8)	t_{CD}							ns
TS71190,A/TS71191,A		–	20	35	–	20	45	
TS71190B, TS71191B		–	–	30	–	–	35	
TS71190C, TS71191C TS71290C, TS71291C		–	–	25	–	–	30	

READING SEQUENCE



DYNAMIC TEST



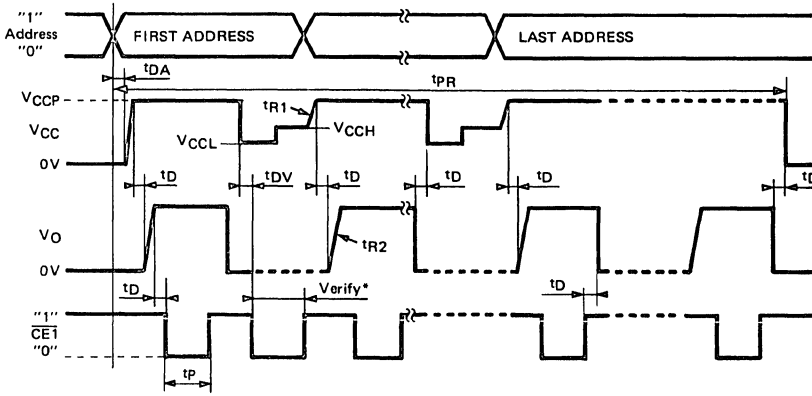


PROGRAMMING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} programming pulse	V_{CCP}	12.5	–	13	V
V_{CC} during verify	V_{CCL} V_{CCH}	4.5 –	– –	– 5.5	V V
Programming supply current (V_{CCP} = 12.75 ± 0.25 V)	I_{CCP}	–	420	550	mA
Input voltage	V_{IL} V_{IH}	0 2.4	– –	0.5 5.5	V V
Output programming voltage	V_O	11.5	12	12.5	V
Output programming current (V_O = 12 ± 0.5)	I_O	–	1.5	–	mA
V_{CC} pulse rise time	t_{R1}	5	–	10	μs
Output pulse rise time	t_{R2}	10	–	20	μs
$\overline{CE_1}$ programming pulse width	t_P	40	50	60	μs
Address set-up time / V_{CCP}	t_{DA}	100	–	–	ns
Pulse sequence delay	t_D	10	–	–	μs
Delay time before verify	t_{DV}	3	–	–	μs
Programming time (V_{CC} = V_{CCP})	t_{PR}	–	–	10	s
Allowed fusing attempts		–	–	1	

1. Select the address to be programmed. Apply $\overline{CE1}$ = H ; CE2 = H ; CE3 = H.
2. After a delay $t_{DA} \geqslant 100$ ns, raise V_{CC} to V_{CCP} = 12.75 V ± 0.25 V.
3. After a delay $t_D \geqslant 10$ μs, apply V_O = 12 ± 0.5 V to the output to be programmed. Program one output at the time. Other outputs are open.
4. After a delay $t_D \geqslant 10$ μs, apply a logic low level to the $\overline{CE1}$ input. This level will be held during t_P = 50 ± 10 μs.
5. After a delay $t_D \geqslant 10$ μs, remove output voltage V_O from the output to be programmed.
6. After a delay $t_D \geqslant 10$ μs, lower the voltage V_{CCP} to V_{CC} = 5 ± 0.5 V.
7. After a delay $t_{DV} \geqslant 3$ μs, apply a logic low level to the $\overline{CE1}$ input and verify that the programmed output remains in the high state for V_{CCH} = 5.5 V and V_{CCL} = 4.5 V (*). Then, apply a logic high level to the $\overline{CE1}$ chip select input.
8. Repeat steps 1 through 7 to program other locations of the PROM.

TYPICAL PROGRAMMING SEQUENCE



* Programming verification at both max and min V_{CC} is optional (V_{CCH}, V_{CCL}).

ORDERING INFORMATION

TS71191 | M | J | B/B

Part number — Screening class
Oper. temp. — Package

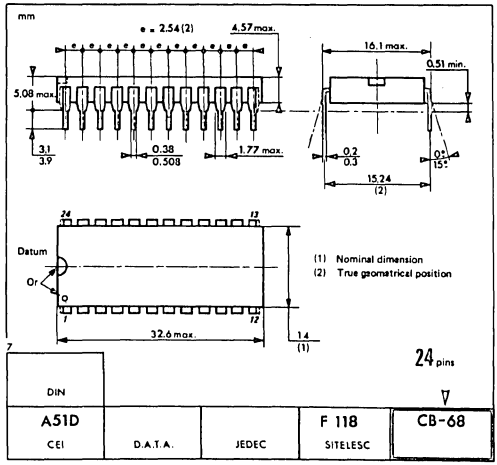
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER		OPER. TEMP.		PACKAGE				SCREENING CLASS			
		C	M	P	J	C	E	Std	–D	G/B	B/B
60 ns	TS71190	O		O	O			O	O		
	TS71191	O		O	O			O	O		
			O		O			O		O	
			O			O	O	O		O	O
	TS71190A	O		O	O			O	O		
	TS71191A	O		O	O			O	O		
			O		O			O		O	
			O			O	O	O		O	O
45 ns	TS71190B	O		O	O			O	O		
	TS71191B	O		O	O			O	O		
			O		O			O		O	
			O			O	O	O		O	O
35 ns	TS71190C	O		O	O			O	O		
	TS71191C	O		O	O			O	O		
			O		O			O		O	
			O			O	O	O		O	O
	TS71290C	O		O	O			O	O		
	TS71291C	O		O	O			O	O		
			O		O			O		O	
			O			O		O		O	O

Examples : TS71190CP, TS71190CP-D, TS71190CJ, TS71190CJ-D

Oper. temp. : **C** : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

PHYSICAL DIMENSIONS



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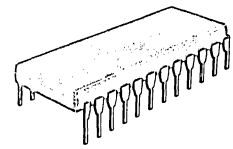


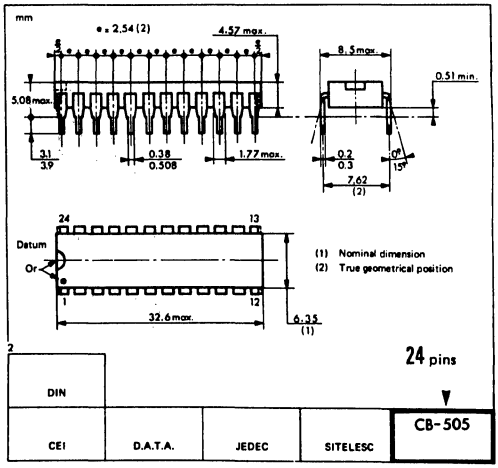
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

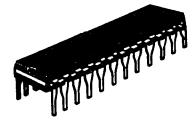
C SUFFIX
CERAMIC PACKAGE

J SUFFIX
CERDIP PACKAGE

PHYSICAL DIMENSIONS



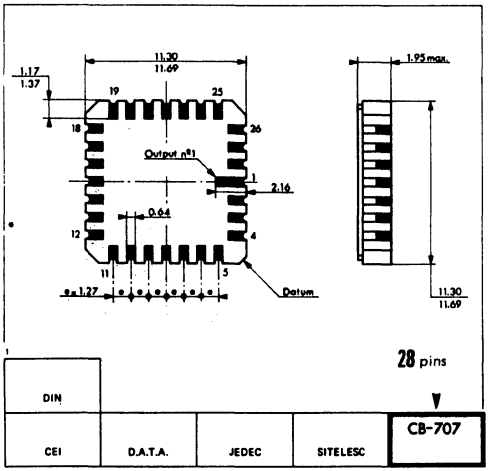
CB 505



TS71290C
TS71291C

P SUFFIX
PLASTIC PACKAGE

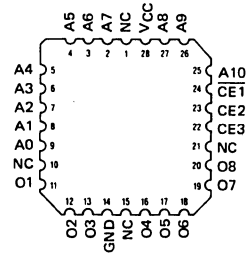
ALSO AVAILABLE
C SUFFIX CERAMIC PACKAGE
J SUFFIX CERDIP PACKAGE



CB-707

TS71190A,B
TS71191A,B

E SUFFIX
TRICECOP (LCC)
CHIP CARRIER PACKAGE



These specifications are subject to change without notice
Please inquire with our sales offices about the availability of the different packages

TS71321(P,C,J)-C/B

32,768-BIT (4096 x 8) FAST PROM

MEMORY COMPONENTS

PRODUCT PREVIEW

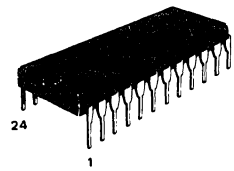
The TS71321 is programmable read-only memory (PROM) organized in a 4096 words by 8-bit configuration and is field programmable. It is shipped in an unprogrammed form and has "0" in all allocations. This PROM's is available with three state outputs (TS71321).

- Fast access times :
  Address access time : 45 ns max TS71321C
  55 ns max TS71321B
- Low voltage programming
- Highly reliable fuses Ti/W for ultra-fast programming
- Low power Schottky technology (oxide isolation process)
- TTL compatible
- Industry standard pin configuration.

APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

32 K FAST PROMs

CASE CB-68

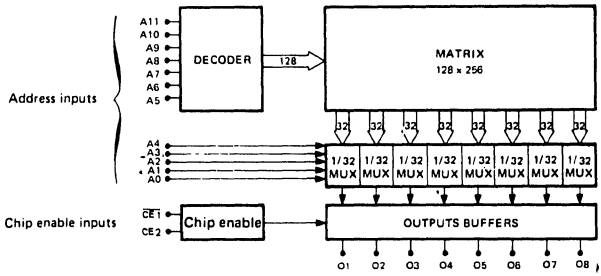


P SUFFIX
PLASTIC PACKAGE

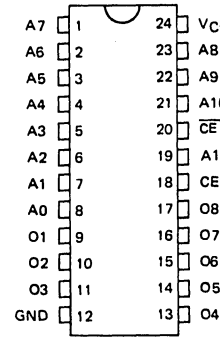
ALSO AVAILABLE

J SUFFIX	C SUFFIX
CERDIP PACKAGE	CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	7 ± 5 %	7 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (V_{CC} = V_{CC} max, V_O = 0) (Note 1)	I_{SC}	- 20	–	- 70	- 15	–	- 85	mA
Low level output voltage (V_{CC} = V_{CC} min, I_{OL} = 16 mA, V_I = V_{IH} or V_{IL})	V_{OL}	–	–	0.45	–	–	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	–	175	–	–	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, CE2 = CE3 = 0.4 V)								
V_O = 5.5 V	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

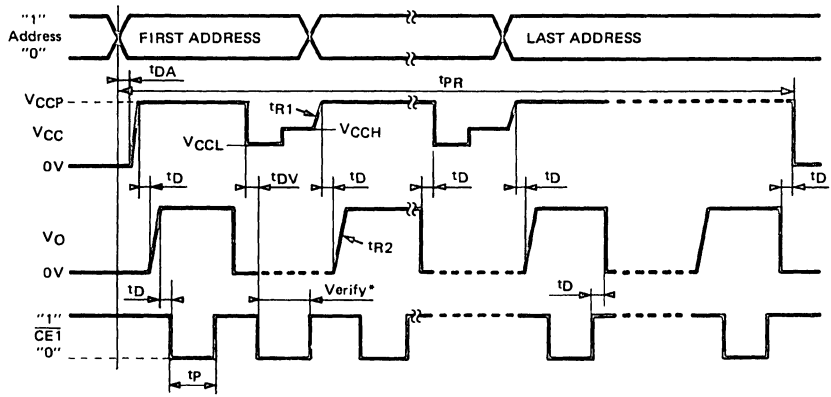
Note 2 : These parameters are not 100 % tested, but are periodically sampled.

PROGRAMMING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} programming pulse	V_{CCP}	12.5	–	13	V
V_{CC} during verify	V_{CCL} V_{CCH}	4.5 –	– –	– 5.5	V V
Programming supply current (V_{CCP} = 12.75 ± 0.25 V)	I_{CCP}	–	420	550	mA
Input voltage	V_{IL} V_{IH}	0 2.4	– –	0.5 5.5	V V
Output programming voltage	V_O	11.5	12	12.5	V
Output programming current (V_O = 12 ± 0.5)	I_O	–	1.5	–	mA
V_{CC} pulse rise time	t_{R1}	5	–	10	µs
Output pulse rise time	t_{R2}	10	–	20	µs
$\overline{CE_1}$ programming pulse width	t_P	40	50	60	µs
Address set-up time / V_{CCP}	t_{DA}	100	–	–	ns
Pulse sequence delay	t_D	10	–	–	µs
Delay time before verify	t_{DV}	3	–	–	µs
Programming time (V_{CC} = V_{CCP})	t_{PR}	–	–	10	s
Allowed fusing attempts		–	–	1	

1. Select the address to be programmed. Apply $\overline{CE1}$ = H ; CE2 = H ; CE3 = H.
2. After a delay $t_{DA} \geqslant 100$ ns, raise V_{CC} to V_{CCP} = 12.75 V ± 0.25 V.
3. After a delay $t_D \geqslant 10$ µs, apply V_O = 12 ± 0.5 V to the output to be programmed. Program one output at the time. Other outputs are open.
4. After a delay $t_D \geqslant 10$ µs, apply a logic low level to the $\overline{CE1}$ input. This level will be held during t_P = 50 ± 10 µs.
5. After a delay $t_D \geqslant 10$ µs, remove output voltage V_O from the output to be programmed.
6. After a delay $t_D \geqslant 10$ µs, lower the voltage V_{CCP} to V_{CC} = 5 ± 0.5 V.
7. After a delay $t_{DV} \geqslant 3$ µs, apply a logic low level to the $\overline{CE1}$ input and verify that the programmed output remains in the high state for V_{CCH} = 5.5 V and V_{CCL} = 4.5 V (*). Then, apply a logic high level to the $\overline{CE1}$ chip select input.
8. Repeat steps 1 through 7 to program other locations of the PROM.

TYPICAL PROGRAMMING SEQUENCE

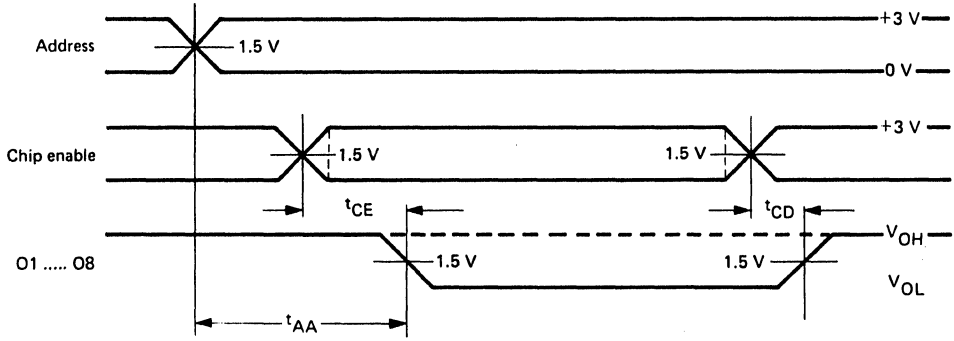


* Programming verification at both max and min V_{CC} is optional (V_{CCH}, V_{CCL}).

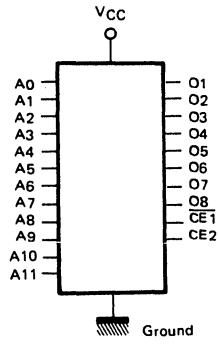
SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

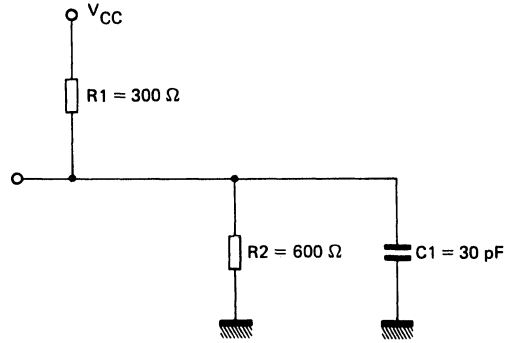
Characteristic		Symbol	C suffix			M suffix			Unit
			Min	Typ	Max	Min	Typ	Max	
Address access time	(A0-A11) → (O1....O8)	t_{AA}							ns
TS71321B			–	–	55	–	–	65	
TS71321C			–	–	45	–	–	60	
Chip enable access time	($\overline{CE1}$, CE2) → (O1....O8)	t_{CE}							ns
TS71321B			–	–	35	–	–	40	
TS71321C			–	–	20	–	–	30	
Chip disable time	(CE1, CE2) → (O1....O8)	t_{CD}							ns
TS71321B			–	–	35	–	–	40	
TS71321C			–	–	20	–	–	30	

READING SEQUENCE

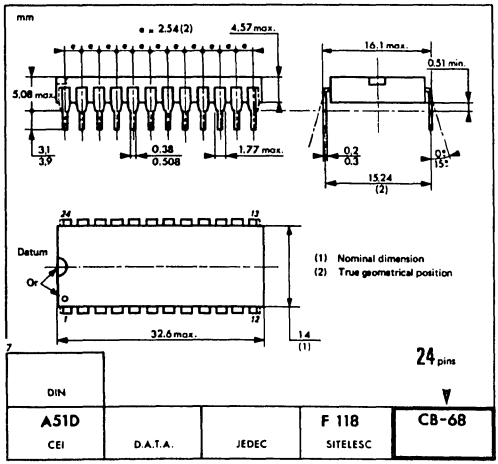


DYNAMIC TEST





PHYSICAL DIMENSIONS



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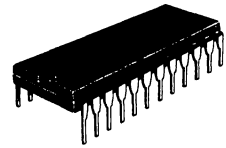
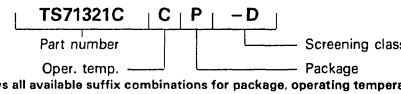


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	**C SUFFIX**
CERDIP PACKAGE	CERAMIC PACKAGE

ORDERING INFORMATION



The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS71321C 45 ns	●		●	●			●	●		
TS71321B 55 ns	●		●	●			●	●		

Examples : TS71321CP, TS71321CP-D, TS71321CJ, TS71321CJ-D

Oper. temp. : C : 0°C to + 70°C, **M :** –55°C to +125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic DIL, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **–D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.

THOMSON COMPONENTS
MOSTEK

TS71640 • TS71641(C)

64.536-BIT (8192 x 8) FAST PROM

MEMORY COMPONENTS

PRODUCT PREVIEW

The TS71640, 71641 are programmable read-only memories (PROM) organized in a 8192 words by 8-bit configuration and are field programmable. They are shipped in an unprogrammed form and have "0" in all allocations. These PROM's are available with open collector (TS71640) or three state outputs (TS71641).

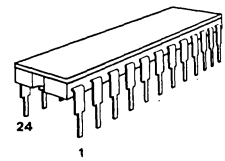
- Fast access times :
  Address access time : 55 ns max.
  Enable access time : 30 ns max.

- Highly reliable shorting junction concept
- Low power Schottky technology (oxide isolation process)
- TTL compatible
- Industry standard pin configuration.

APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

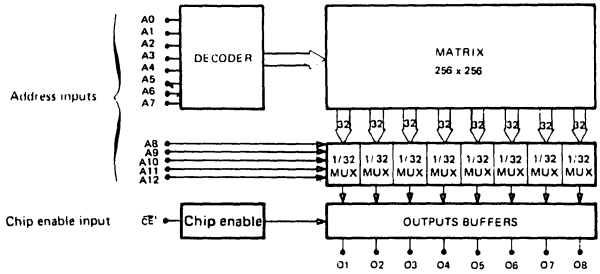
64 K FAST PROMs

CASE CB-68

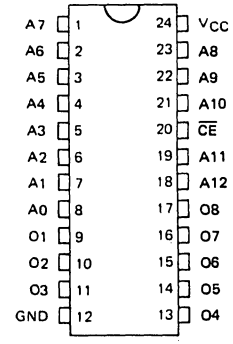


C SUFFIX
CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	7 ± 5 %	7 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (V_{CC} = V_{CC} max, V_O = 0) (Note 1)	I_{SC}	- 20	–	- 70	- 15	–	- 85	mA
Low level output voltage (V_{CC} = V_{CC} min, I_{OL} = 16 mA, V_I = V_{IH} or V_{IL})	V_{OL}	–	–	0.45	–	–	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	–	175	–	–	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, CE_2 = CE_3 = 0.4 V)								
V_O = 5.5 V 71640	I_{OFF}	–	–	+ 40	–	–	+ 60	µA
V_O = 5.5 V 71641	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V 71641	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

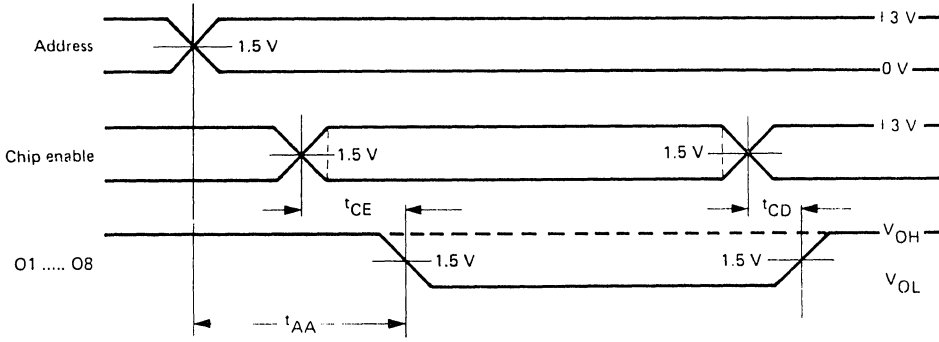
Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

Note 2 : These parameters are not 100 % tested, but are periodically sampled.

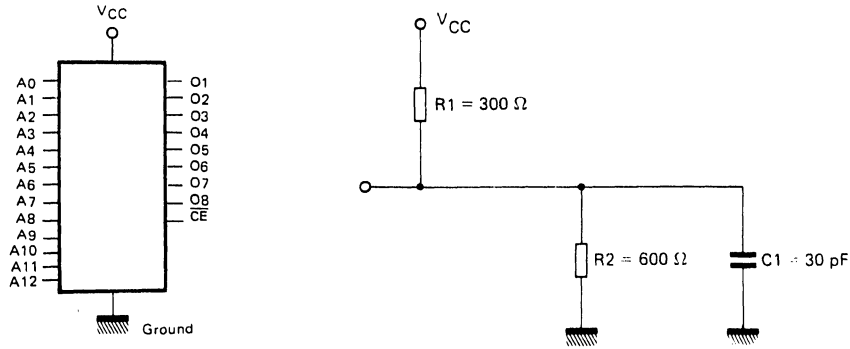
SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

Characteristic		Symbol	C suffix			M suffix			Unit
			Min	Typ	Max	Min	Typ	Max	
Address access time	(A0 - A12) ⟶ (O1 ..... O8)	t_{AA}	–	–	55	–	–	65	ns
Chip enable access time	($\overline{CE}$) ⟶ (O1 ..... O8)	t_{CE}	–	–	30	–	–	35	ns
Chip disable time	($\overline{CE}$) ⟶ (O1 ..... O8)	t_{CD}	–	–	30	–	–	35	ns

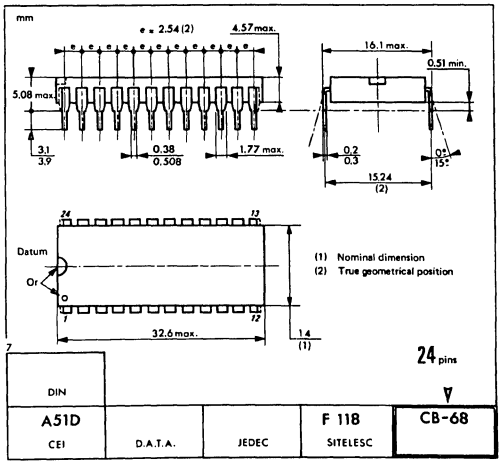
READING SEQUENCE



DYNAMIC TEST



PHYSICAL DIMENSIONS



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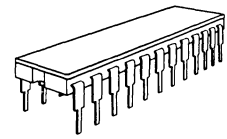

C SUFFIX
CERAMIC PACKAGE

ORDERING INFORMATION

TS71640 | **P** | **–D**

- TS71640: Part number
- P: Oper. temp. / Package
- –D: Screening class

The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS71640	●		●	●			●	●		
TS71641	●		●	●			●	●		

Examples : TS71640CP, TS71640CP-D, TS71640CJ, TS71640CJ-D

Oper. temp. : C : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : P : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : Std (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

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