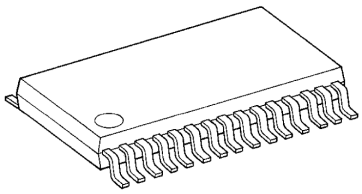
TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

TA8552AFN

PLL Data Synchronizer For DAT Streamer

The TA8552AFN is PLL data synchronizer for digital audio tape (DAT) strteamer, digital data storage (DDS).



SSOP30-P-300-0.65

Weight: 0.17g (typ.)

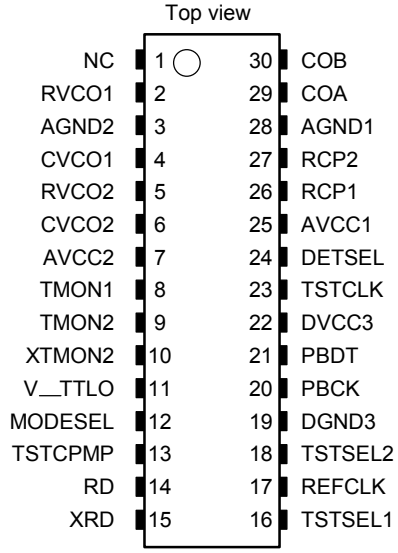
Features

- The TA8552AFN incorporates edge detector, data synchronizer, and latch for data separator.
  Also the TA8552AFN is available to correspond to ×1, ×2 and ×3 of data transfer rates by adjusting external devices.
- The data synchronizer is avalable to correspond to ±7% variation of data transfer rate.
- By employing full differential signal processing in PLL loop, the TA8552AFN eliminates the influence of external noise.
  Fast & stable locking is realized by switching between the frequency detective mode and the phase detective mode.
- Operating power supply voltage range: 4.5V to 5.5V
- Small package; SSOP30−P−300−0.65

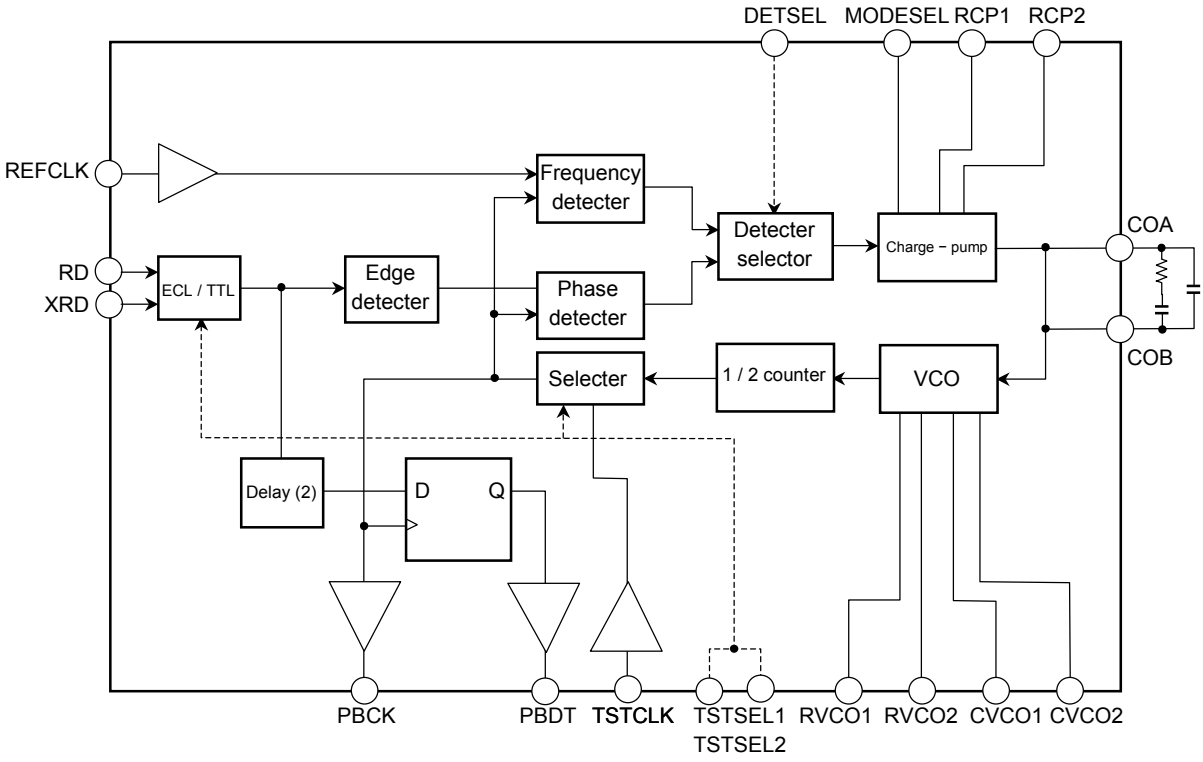
Handle with care to prevent devices from deterioration by static electricity.

Pin Connectoion

Top view



Block Diagram



Pin Function

Pin No.	Pin Name	Function	In / Out
1	NC	NC terminal. (open at normal use)	—
2	RVCO1	VCO adjusting terminal. Connect an external resistor (R_{VCO1}) between V_{CC}.	—
3	AGND2	Analog ground for VCO.	—
4	CVCO1	VCO adjusting terminal. Connect a capacitor (C_{VCO}) between this pin and pin6.	—
5	RVCO2	VCO adjusting terminal. Connect an external resistor (R_{VCO2}) between V_{CC}.	—
6	CVCO2	VCO adjusting terminal. Connect a capacitor (C_{VCO}) between this pin and pin4.	—
7	AVCC2	Analog power supply voltage for VCO.	—
8	TMON1	NC terminal (open at normal use)	—
9	TMON2	NC terminal (open at normal use)	—
10	XTMON2	NC terminal (open at normal use)	—
11	V_TTLO	Input terminal for TTL voh (high voltage level of pin20, and pin21 output) limitting.	—
12	MODESEL	Input terminal for switching the normal mode and the serching mode. (H: Normal mode, L: Serching mode)	TTL−in
13	TSTCPMP	NC terminal. (open at normal use.)	—
14	RD	Input terminal of data (normal phase)	ECL−in or TTL−in
15	XRD	Input terminal of data (reverse phase). (this terminal is active when TSTSEL1 = L and TSTSEL2 = H. Otherelse, short with V_{CC}.)	(ECL−in)
16	TSTSEL1	Input terminal for test mode selecting. (refer the chapter of "test mode")	—
17	REFCLK	Reference clock input of frequency synchronizer.	TTL−in
18	TSTSEL2	Input terminal for test mode selecting. (refer the chapter of "test mode")	—
19	DGND3	Digital ground for TTL output.	—
20	PBCK	Output terminal of data latch clock.	TTL−out
21	PBDT	Output terminal of data latch.	TTL−out
22	DVCC3	Digital power supply voltage for TTL output.	—
23	TSTCLK	Input terminal of ×1 / 2 vco test clock. (short with V_{CC} at mormal use.)	—
24	DETSEL	Input terminal for switching the frequency detective mode and the phase detective mode. (L : The frequency detective mode H : The phase detective mode.)	TTL−in
25	AVCC1	Analog power supply voltage.	—

Pin No.	Pin Name	Function	In / Out
26	RCP1	Adjusting terminal of charge pump at normal mode. Connect an external resistor (R_{cp1}) between GND.	—
27	RCP2	Adjusting terminal of charge pump at normal mode. Connect an external resistor (R_{cp2}) between GND.	—
28	AGND1	Analog ground	—
29	COA	Connecting terminal of loop filter. Connect an external loop filter between this pin and 30pin.	—
30	COB	Connecting terminal of loop filter. Connect an external loop filter between this pin and 29pin.	—

Absolute Maximum Rating (Ta = 27°C)

Parameter	Symbol	Rating	Unit
Supply voltage	AVCC	7	V
Input voltage	V_{IN}	−0.3~V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3~V_{CC}+0.3	V
Storage temperature	T_{stg}	−55~150	°C

Recommended Operating Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	AVCC	—	4.5	5	5.5	V
Operation temperature	T_{opr}	—	−5	—	75	°C

Power Supply (unless otherwise specifide, Ta = 27°C, V_{CC} = 5.0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	IPLCC	TSTSEL1 = H, TSTSEL2 = L DETSEL = L, MODSEL = H			65	mA

Electrical Characteristic (unless otherwise specified, Ta = 27°C, V_{CC} = 5.0V)

Parameter	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH}	—	TTL input pins	2.0	—	—	V
Low level input voltage (1)	V_{IL}	—	TTL input pins	—	—	0.4	V
High level input current (1)	I_{IH}	—	TTL input pins	—	—	20	μA
Low level input current (1)	I_{IL}	—	TTL input pins	—	—	−360	μA
High level input voltage (2)	VIHE	—	ECL input pins	V_{CC} −1.0	—	—	V
Low level input voltage (2)	VILE	—	ECL input pins	—	—	V_{CC} −1.5	V
High level input current (2)	IIHE	—	ECL input pins	—	—	2.0	mA
Low level input current (2)	IILE	—	ECL input pins	—	—	1.6	mA
High level output voltage (1)	V_{OH}	—	TTL output pins I_{OH} = 400μA	VTTLO −0.2		VTTLO +0.2	V
Low level output voltage (1)	V_{OL}	—	TTL output pins I_{OL} = 4mA	—	—	1.0	V
Output rise time (1)	TOR	—	TTL output pins 1.5V to 3.5V C_L≤30pF *1	—	—	5	ns
Output fall time (1)	TOF	—	TTL output pins 3.5V to 1.5V C_L≤30pF *1	—	—	5	ns
Input voltage range to VTTLO terminal	VTTLO	—		2.7	—	3.3	V

*1; Design guaranteed value.

Charge Pump (unless otherwise specified, Ta = 27°C, V_{CC} = 5.0V)

Parameter	Symbol	Test Circuit	Condition	Min.	Typ.	Max.	Unit
Range of output current setting	I_{CP}	—	At normal mode *1	30	—	—	μA
		—	At serching mode *2	—	—	800	
Accuracy of output current setting	I_{acu}	—	At normal mode	−6	—	+6	%
		—	At serching mode	−8	—	+8	
Leak current	I_{reak}		Between COA pin and COB pin, at high impedance	−3.5		+3.5	μA

*1; Output current is set by an external resistor (R_{cp1}), as following;
$2 \times 1.3 / R_{cp1}$ = (output current at normal mode).

*2; Output current is set by external resisters (R_{cp1}, R_{cp2}), as following;
$2 \times 1.3 / R_{cp1} + 8 \times 1.3 / R_{cp2}$ = (output current at search mode).

(Note) The above values are all at open loop.

VCO (unless otherwise specified, Ta = 27°C, V_{CC} = 5.0V)

Parameter	Symbol	Test Circuit	Condition	Min.	Typ.	Max.	Unit
Input voltage of VCO (V (COB −COA))	V_{VCO}	—	R_{VCO1} = 3.75 kΩ R_{VCO2} = 1.21 kΩ C_{VCO} = 39pF *1 f_{VCO} = 28.224MHz	0.25		0.45	V
Upper limitation of VCO frequency	f_{max}	—	R_{VCO1} = 3.75 kΩ R_{VCO2} = 1.21 kΩ C_{VCO} = 39pF *1 V (COB −COA) = 0.6V	29.5			MHz
Lower limitation of VCO frequency	f_{min}	—	R_{VCO1} = 3.75 kΩ R_{VCO2} = 1.21 kΩ C_{VCO} = 39pF *1 V (COB −COA) = −0.6V			23.5	MHz
Control gain (F / V)	G_{VCO}	—	R_{VCO1} = 3.75 kΩ R_{VCO2} = 1.21 kΩ C_{VCO} = 39pF *1 Voltage (COB −COA) Excursion 0.3V to −0.3V	6		7.7	MHz / V
VCO jitter	t_{jit}	—	PBCK pin at ×3 transfer rate *2		300		ps

*1; C_{VCO} inclides the package capacitance.

*2; Design guaranteed value.

(Note) The above values are all at open loop, measured at the PBCK pin

Closed Loop (unless otherwise specified, Ta = 27°C, V_{CC} = 5.0V)

Parameter	Symbol	Test Circuit	Condition	Min.	Typ.	Max.	Unit
VCO jitter in closed loop	t_{jit2N}	—	In search mode lock to REFCLK			0.5	ns
VCO jitter in closed loop	t_{jit2S}	—	In normal mode lock to RD			0.4	ns

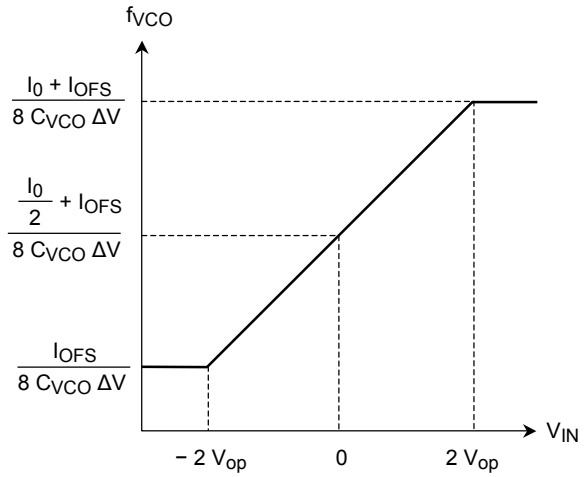
Values of external parts are (R_{VCO1} = 3.75 kΩ, R_{VCO2} = 1.21 kΩ, C_{VCO} = 39pF (including storage capacitor), R_{CP1} = 8.25k, R_{CP2} = 30.1k).

Character Of VCO

The connection of input voltage and output frequency of VCO (measured at PBCK after the 1 / 2 frequency counter) is written as following;

$$f_{vco} = \begin{cases} \frac{1}{8 \cdot C_{vco} \cdot \Delta V} \cdot (I_O + I_{ofs}) & (V_{in} > 2V_{op}) \\ \frac{1}{8 \cdot C_{vco} \cdot \Delta V} \left(\frac{I_O}{4V_{op}} \cdot Vin + \frac{I_O}{2} + I_{ofs} \right) & (2V_{op} > V_{in} > -2V_{op}) \\ \frac{1}{8 \cdot C_{vco} \cdot \Delta V} \cdot I_{ofs} & (V_{in} < -2V_{op}) \end{cases}$$

Where; C_{vco} is an external capacitor between 4pin and 6pin, $\Delta V = 0.35V$, $V_{op} = 0.275V$, V_{in} is the input voltage of VCO (differential), $I_O = 3 \times 1.3 / R_{vco1}$, and $I_{ofs} = 2 \times 1.3 / R_{vco2}$.



So, the gain of VCO is defined as following (at PBCK);

$$\frac{1}{8 \cdot C_{vco} \cdot \Delta V} \cdot \frac{I_O}{4V_{op}}$$

And, upper limitation f upper, and lower limitation of VCO frequency f lower is defined as follows;

$f_{upper} = (I_O + I_{ofs}) / 8C_{vco}\,\Delta V$

$f_{lower} = I_{ofs} / 8C_{vco}\,\Delta V$

I 0 can be determined by selecting R_{vco1}, and I ofs can by R_{vco2}. So, you can independently determine the gain of VCO, upper limitation and lower limitation of VCO frequency by selecting C_{vco}, R_{vco1}, and R_{vco2}.

【Example】When, C_{vco} = 22.1pF, R_{vco1} = 2.6kΩ, R_{vco2} = 2.6 kΩ,

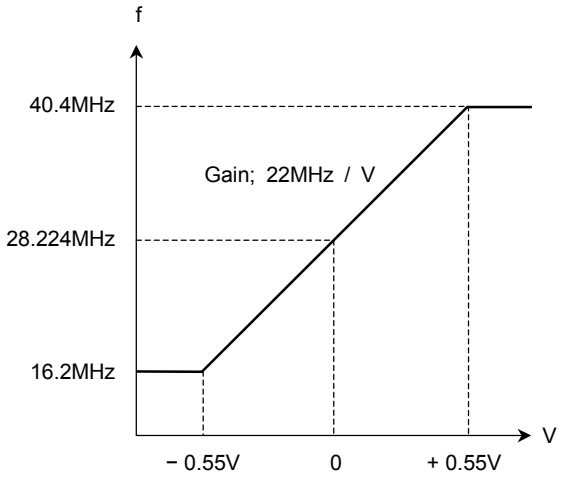
Gain of VCO ; $\dfrac{1.3 / (2.6\times10^{3})\times3}{8\times22.1\times10^{-12}\times0.35\times4\times0.275}$ = 22MHz / V

Upper limitation

of VCO frequency ; $\dfrac{1.3 / (2.6\times10^{3})\times3+1.3 / (2.6\times10^{3})\times2}{8\times22.1\times10^{-12}\times0.35}$ = 40.4MHz

Lower limitation

of VCO frequency ; $\dfrac{1.3 / (2.6\times10^{3})\times2}{8\times22.1\times10^{-12}\times0.35}$ = 16.2MHz



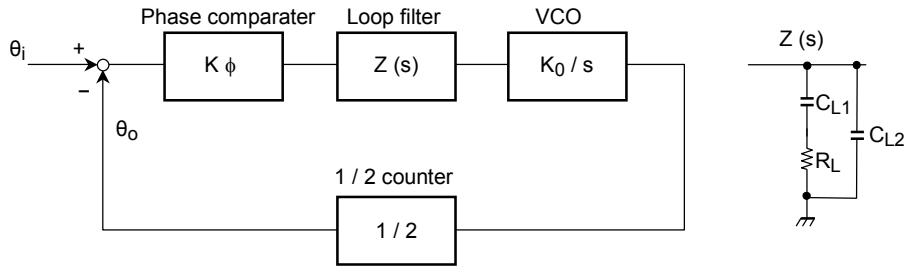
Function Description:

The angular frequency (ω_n) and dumping facter (ζ) are adjusted by external devices.
The setting procedure is shown as following.

The setting conditions to lock PLL inside a constant time;

- Data transfer rate: 28.224Mbps (f_M = 28.244MHz)
- The capturing signal of PLL: The rectangle wave of 14.112MHz (data pattern is 101010...),
  The term of this data is continuous 180 bits.
- The capturing time of PLL: $1 / (14.114\times10^{6}) \times 180 = 12.75\times10^{-6}$s
  $12.75\times10^{-6}\times0.9 = 11.5\mu$s (this 0.9 is a factor of margin.)

【The transfer function of PLL】



The transfer function (F (S)), the angular frequency (ω_n), and the dumping facter (ζ) of the above composition are defined as following (However C_{L2} is ignored as $C_{L2} \ll C_{L1}$):

$$\omega_n = \left(\frac{K}{C_{L1}}\right)^{1/2}$$

$$\zeta = \frac{R_L C_{L1} \omega_n}{2}$$

【Calculation of ζ】
The dumping factor (ζ) is set to 0.7 as the most stable response characteristic. Besides ω_n t is assumed to set as 6.

【Calculation of ω_n】

The capturing time of PLL is expected as above 11.5μs. Therefore (ω_n) is determinated as the following:

$\omega_n = 6 / (11.5\times10^{-6}) = 552$krad / s

【Calculation of K_0 (VCO control gain)】

K_0 is determined as the following;

$K_0 = 40$MHz / V = 251.3Mrad / V

【Calculation of $K\phi$ (phase detector gain)】

$K\phi$ is estimated as the following (the current of charge pump is set as ±50μA.)

$$K\phi = \frac{1}{2} \cdot \frac{1}{2\pi} \times 50\times10^{-6} = 3.98\times10^{-6}(\text{A / rad})$$

The current of charge pump (Ichp) is set by an external resister (R_{cp1}), connected with R_{cp1} (26pin). When "H"level voltage inputs to MODESEL (12pin), Ichp is set as the following:

$I_{chp} = 2\times1.3 / R_{CP1} \rightarrow R_{CP1} = 2\times1.3 / I_{chp} = 2\times1.3 / 50\times10^{-6} = 52\times10^{3}\Omega$

Therefore, when R_{CP1} is 52kΩ, I_{chp} is set as ±50μA

【Calculation of external devices of loop–filter】

$$C_{L1} = \frac{K\phi\times K_0}{2\omega_n} = \frac{3.98\times10^{-6}\times251.3\times10^{6}}{2\times(522\times10^{3})^2} = 1800\times10^{-6}\text{F}$$

$$R_L = \frac{2\zeta}{C_{L1}\omega_n} = \frac{2\times0.7}{1800\times10^{-12}\times522\times10^{3}} = 1.5\times10^{3}\Omega$$

$C_{L2} = C_{L1} / 10 = 180$pF

Modesel Switching Function

The TA8552AFN has a function to correspond with the high–speed serching mode of DAT streamer. In the searching mode, the data transfer rate will shift with small percentage error. The TA8552AFN is available to solve this problem by extending the lock–in–range ($\Delta\omega_L$). In the serching mode the current of charge pump will be increased to raise the phase detecter gain, then the lock–in–range ($\Delta\omega_L$) will extend.
This function is selected by modesel (12pin).
(H: Normal mode / L: Searching mode)

【Calculation of the charge pump's current in the searching mode】

The charge pump's current in the searching mode is estimated as the following (the shift rateX of data, transfer is assumed as X = 7% in this example);

$$I_{chp} = \frac{f_M \times X \times 2\pi}{R \times K_0} \times 8\pi = \frac{28.224 \times 10^6 \times 0.07 \times 2 \times 3.14}{1.5 \times 10^3 \times 251.3 \times 10^6} \times 8 \times 3.14 = 830 \times 10^{-6} (A)$$

When "L" level voltage inputs to modesel (12pin), the charge pump's current (Ichp) increases. In the normal mode, the charge pump's current (I_{cp1}) is set by an external resister (R_{cp1}). And in the searching mode, another current (I_{cp2}), is set by an external resisiter (R_{cp2}), adds to Icp1.
This (R_{cp2}) is the resister to be connected with RCP2 (27pin)
The additional current (I_{cp2}) is determined by the following:

$$I_{cp2} = 8 \times 1.3 / R_{cp2}$$

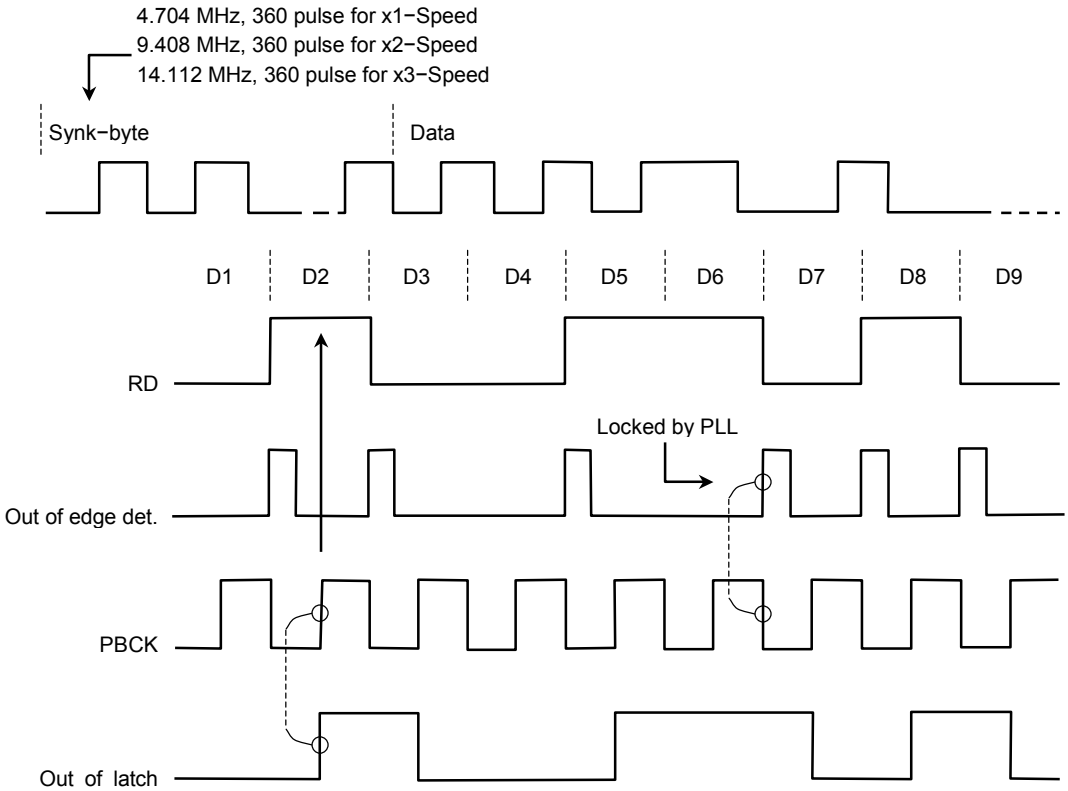
Therefore, R_{cp2} is estimated as the following:

$$R_{cp2} = \frac{8 \times 1.3}{830 \times 10^{-6} - 50 \times 10^{-6}} = 13.3 \times 10^3 \Omega$$

Modesel function is summarized by the followings

Mode	Normal Mode	High–speed Searghing Mode
Modesel (12pin)	H	L
Charge pump current Ichp	I_{cp1}	$I_{cp1}+I_{cp2}$
Setting definition	$2 \times 1.3 / R_{cp1}$	$2 \times 1.3 / R_{cp1} + 8 \times 1.3 / R_{cp2}$

Timing Chart Of Latch



(Note) Test Monitor Output Terminal

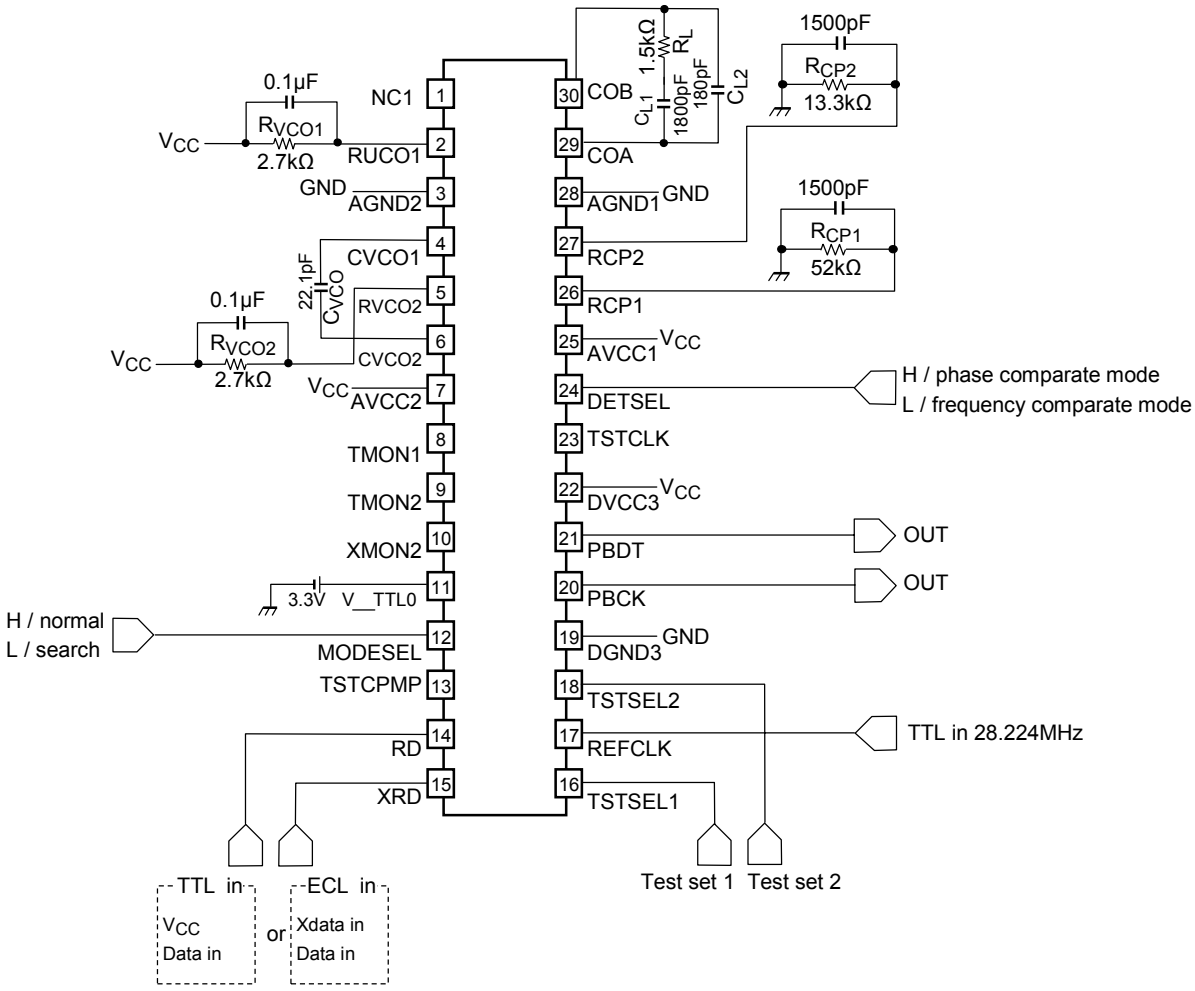
Tstsel		Datainput	Function
1	2		
L	L	TTL input from 14pin (RD)	—
H	L	TTL input from 14pin (RD)	PBCK (20pin) & PBDT (21pin) becomes disable
L	H	ECL input from 14pin (RD) and 15pin (XRD)	—
H	H	TTL input from 14pin (RD)	The internal PLL becomes disable, and the external clock from tstclk (23pin) becomes enable as input data signal.

(Note) ● We commend the use of this IC under the comdition of ECL input from 14pin (RD) and 15pin (XRD) when (TSTSEL1, TSTSEL2) = (L, H)

● It is possible of the use of TTL input from 14pin (RD) when (TSTSEL1, TSTSEL2) = (L, L)

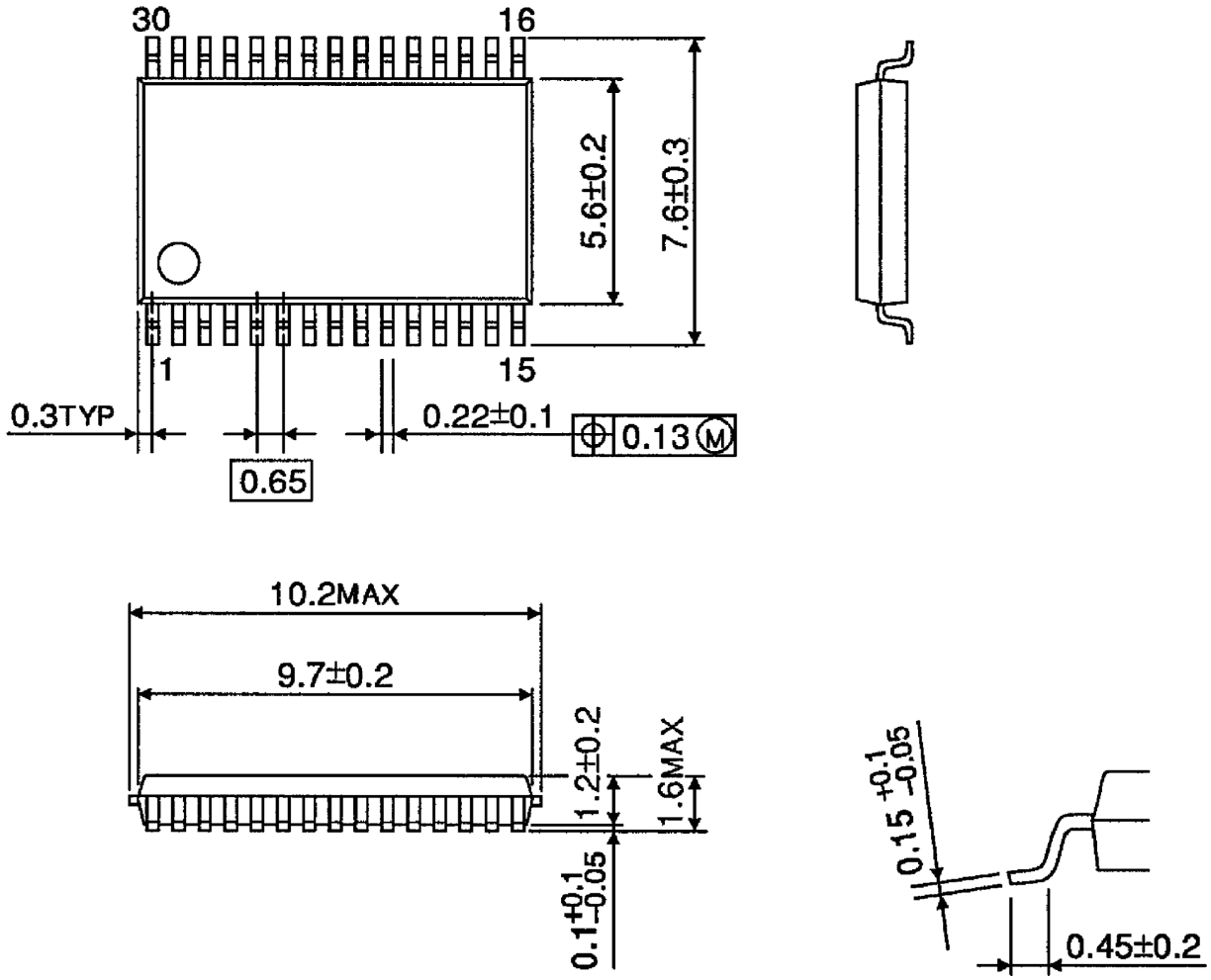
Application Diagram

When the data transfer rate is 28.224Mbps, the application diagram is shown below.



Package Dimensions

SSOP30-P-300-0.65 Unit : mm



Weight: 0.17g (typ.)

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