TC8565P/F

(Floppy Disk Controller)

1 INTRODUCTION

TC8565P/F is a single chip LSI for Floppy Disk Controller. This LSI has circuits and control functions for interfacing a processor to floppy disk drives. This LSI has a capability of executing 15 different commands. Each of these commands require multiple 8-bit bytes to accomplish the operation which the processor wishes the FDC to perform.

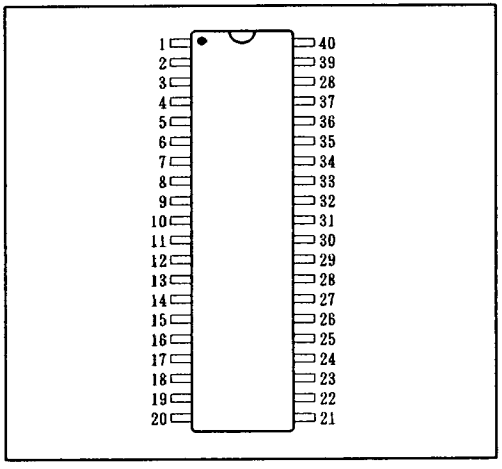
2 FEATURES

- o Si-Gate CMOS Single Chip LSI
- o Single +5V Power Supply
- o Low Power Consumption (Max.10mA at 8MHz 5V)
- o 40 pin Plastic DIP ,44 pin Plastic mini FP
- o Compatible with 8080 System Data & Control Buses
- o Single-phase Clock 8MHz (for Standard Floppy Disk)
  4MHz (for Mini Floppy Disk)
- o FM,MFM Recording Formats (Specified by Command)
- o Multi-sector Data Transfer
- o Multi-track Data Transfer
- o Up to Four Floppy Disk Drives
- o Parallel Seek Operation Up to Four Floppy Disk Drives
- o Programmable Step Rate Time
- o Write Pre-compensation Control Signal Outputs
- o Compatible with IBM Diskette 1
  (one-side 128,256,512 byte/sector)
- o Compatible with IBM Diskette 2
  (one-side 256 byte/sector)
- o Programmable Data Record Lengths
  (128,256,512,1024,2048,4096 and 8192 byte/sector)
- o Capability of Read/Write to the Middle of the Sector When the Record Length is Programmed to 128 Bytes
- o Including CRC Check Function ($X^{16}+X^{12}+X^{5}+1$)
- o Programmable Head Load Time and Head Unload Time
- o Data Scanning Function (Detection of Equal,High or Low)
- o DMA/Non-DMA (Interrupt) Data Transfer

3 PIN DESCRIPTION

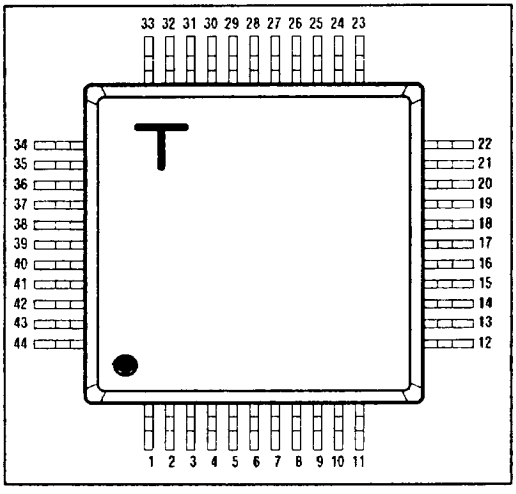
3.1 PIN CONFIGURATION

TC8565P



PIN NO.	IO	NAME	PIN NO.	IO	NAME
1	I	RST	21	I	WCK
2	I	-RD	22	I	DW
3	I	-WR	23	I	RDT
4	I	-CS	24	O	SYNC
5	I	RS	25	O	WE
6	IO	D0	26	O	MFM
7	IO	D1	27	O	HS
8	IO	D2	28	O	DS1
9	IO	D3	29	O	DS0
10	IO	D4	30	O	WDT
11	IO	D5	31	O	PS1
12	IO	D6	32	O	PS0
13	IO	D7	33	I	FLT/TKO
14	O	DRQ	34	I	WP/2S
15	I	-DAC	35	I	RDY
16	I	TC	36	O	HL
17	I	IDX	37	O	FR/STP
18	O	INT	38	O	LC/DR
19	I	CLK	39	O	-RW/SK
20	G	VSS	40	V	VDD

TC8565F



PIN NO.	IO	NAME	PIN NO.	IO	NAME
1		NC	23		NC
2	O	MFM	24	IO	D0
3	O	HS	25	IO	D1
4	O	DS1	26	IO	D2
5	O	DS0	27	IO	D3
6	O	WDT	28	IO	D4
7	O	PS1	29	IO	D5
8	O	PS0	30	IO	D6
9	I	FLT/TKO	31	IO	D7
10	I	WP/2S	32	O	DRQ
11	I	RDY	33	I	-DAC
12		NC	34	I	TC
13	O	HL	35	I	IDX
14	O	FR/STP	36	O	INT
15	O	LC/DR	37	I	CLK
16	O	-RW/SK	38	G	(VSS)
17	V	(VDD)	39	V	(VDD)
18	I	RST	40	I	WCK
19	I	-RD	41	I	DW
20	I	-WR	42	I	RDT
21	I	-CS	43	O	SYNC
22	I	RS	44	O	WE

3.2 Description of Pin Function

o RST [Reset] Input
"High level" on this pin makes the FDC idle state, and makes outputs on the FDD side except [WDT], [PS0] and [PS1] to "Low level".

o -RD [Read] Input
Control signal to transfer data from the FDC to the Data-Bus.

o -WR [Write] Input
Control signal to transfer data from the Data-Bus to the FDC.

o -CS [Chip Select] Input
"Low level" on this pin selects the FDC, and allows [-RD] and [-WR] to be effective.

o RS [Register Select] Input
"High level" on this pin selects Data Register. "Low level" selects Status Register.

o D0-7 [Data Bus] Input/Output
Bidirection 8-bit Data Bus.

o DRQ [DMA Request] Output
Request signal for DMA transfer. This pin requires to connect pulled up resistance.

o -DAC [DMA Acknowledge] Input
When data are transferred in DMA mode, "Low active" DMA acknowledge signal from DMA controller is applied.

o TC [Terminal Count] Input
"High active" signal is applied to indicate the termination of the data transfer.

o IDX [Index] Input
"High active" Index signal from FDD is applied to indicate the beginning of a disk track.

o INT [Interrupt] Output
"High active" interrupt request signal.

o CLK [Clock] Input
FDC's system clock input.
8MHz for Standard Floppy(data transfer rate is 500kbps)
4MHz for Mini Floppy (data transfer rate is 250kbps)

o WCK [Write Clock] Input
Clock signal to write data. Clock is necessary for all read/write operations. The rising edge of WCK must match with that of CLK.

Standard Floppy	MFM mode	1MHz
	FM mode	500KHz
Mini Floppy	MFM mode	500KHz
	FM mode	250KHz

o DW [Data Window] Input
Data Window signal is for separating the read data into "data bits" and "clock bits". This signal is usually generated by a PLL circuit.

o RDT [Read Data] Input
This signal indicates read data from a FDD. This signal contains clock bits and data bits.

o SYNC [VFO Sync] Output
This signal indicates to the PLL that data are read out.

o WE [Write Enable] Output
This signal indicates the write timing of the write data.

o MFM [MFM data] Output
"High level" of this pin indicates MFM mode, "Low level" FM mode.

o HS [Head Select] Output
"Low level" of this pin indicates Head 0, and "High level" Head 1.

o DS1,DS0 [Drive Select 1,0] Output
DS1 and DS0 are multiplexed drive select signal. FDC selects one of four connected disk drives.

o WDT [Write Data] Output
This signal is for FDD's Write Data including clock bits and data bits.

o PS1,0 [Preshift] Output
These signal indicate the write precompensation information to the FDD in MFM mode.

PS0	PS1	MEANING
Low	Low	Normal
Low	High	Late
High	Low	Early

o FLT/TK0 [Fault/Track 0] Input
Sense input. In read/write mode, sensing the FDD fault condition. In Seek mode, sensing the Track 0 condition.

o WP/2S [Write Protect/Two Side] Input
Sense input. In read/write mode, sensing the FDD Write Protect status. In Seek mode, sensing the Two Side condition.

o RDY [Ready] Input
This pin senses the FDD ready status signal.

o HL [Head Load] Output
This is the control signal of the Head Load of the FDD.

o FR/STP [Fault Reset/Step] Output
This signal resets fault status in the FDD in read/write mode. Provides the step pulses to move head to the another cylinder in Seek mode.

o LC/DR [Low Current/Direction] Output
In the read/write mode, this signal indicates that read/write head is inner the forty-third track. In Seek mode, shows direction that the head will step.

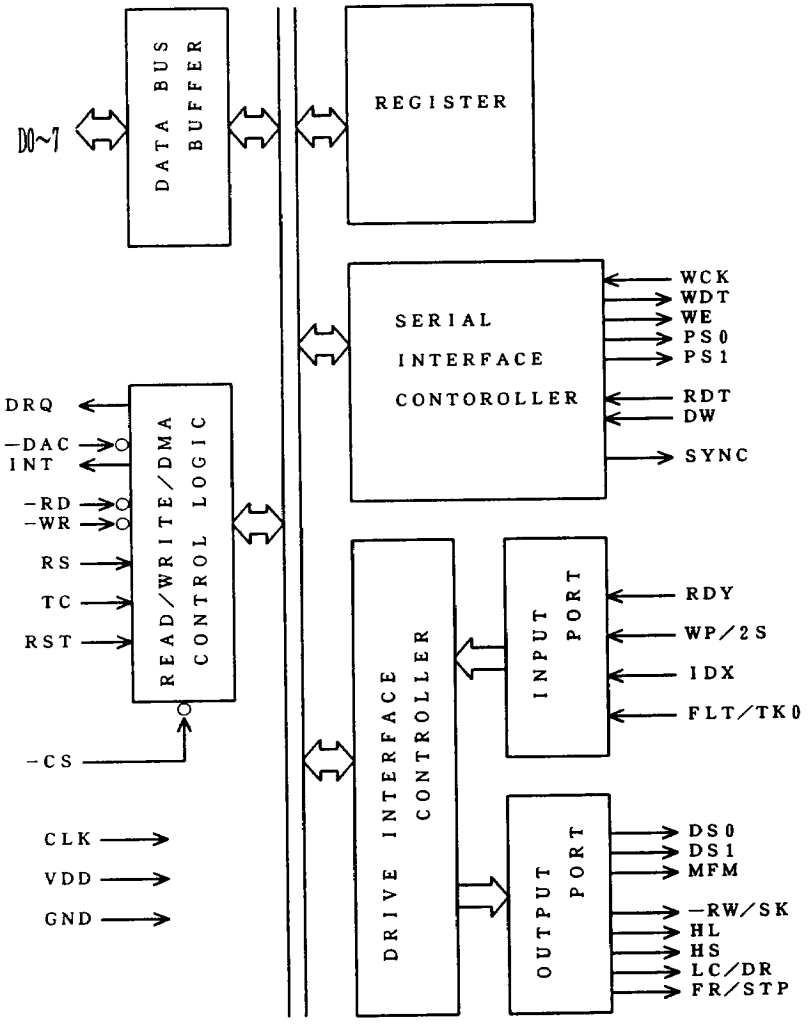
o -RW/SK [Read:Write/Seek] Output
"Low" shows that read/write mode is selected, and "High" shows that Seek mode is selected.

o VDD [DC Power]
Power supply terminal.

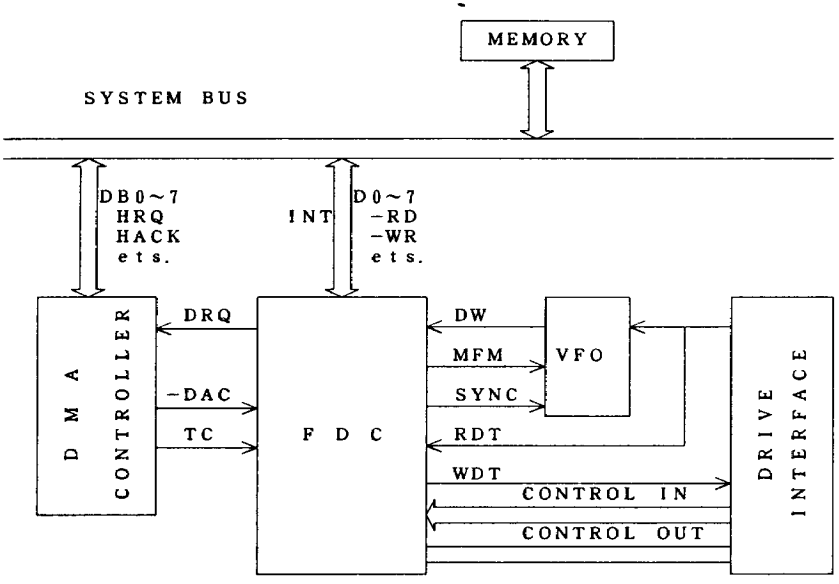
o VSS [Ground]
LSI's ground terminal.

4 FDC APPLICATION SYSTEM

4.1 TC8565P/F BLOCK DIAGRAM



4.2 SYSTEM CONFIGURATION



4.3 OPERATION SUMMARY

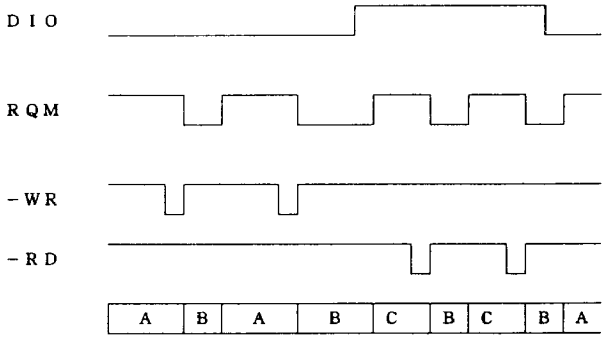
4.3.1 FDC's REGISTER and CPU INTERFACE

FDC has two 8-bit registers accessible by the main system processor. One is a Main Status Register, and the other is a Data Register. The Main Status Register indicates the status information of the FDC and is always accessible. The Data Register is used for data transfer between the FDC and the main processor. Command bytes are written into the Data Register in order to program the FDC, and also Status bytes are read out of the Data Register in order to obtain the result after execution of the commands. Main Status Register may be read and is used to facilitate the data transfer between the processor and the FDC. The relationship between Main Status Register and [-RD],[-WR] and [RS] signals is shown below.

[-CS]	[RS]	[-RD]	[-WR]	FUNCTION
H	X	X	X	Non Select
L	L	L	L	Illegal
L	L	L	H	Read Main Status Register
L	L	H	L	Illegal
L	H	L	H	Illegal
L	H	L	H	Read from Data Register
L	H	H	L	Write into Data Register

Each bit in the Main Status Register are defined as TABLE 1.
The RQM and DIO bits in the Main Status Register indicate whether Data Register is ready or not and in which direction data will be transferred on Data Bus.

FIG.1 Main Status Register Timing



A: (DIO="Low" and RQM="High") The processor may write the data in Data Register.
B: (RQM="Low") Data Register is not ready.
C: (DIO="High" and RQM="High") In data register, data byte which will be read out by processor is already prepared.

TABLE 1 Main Status Register

BIT	SYMBOL	NAME	MEANING
D7	RQM	REQUEST for MASTER	Indicates that Data Register is ready to send the data to or to receive the data from the processor.
D6	DIO	DATA INPUT/ OUTPUT	Indicates the direction of data transfer between Data Register and the processor. When DIO is a "High", transfer is from Data Register to the processor. When DIO is a "Low", transfer from the processor to Data Register.
D5	NDM	Non-DMA mode	Indicates that the FDC is Non-DMA mode. It is set only during Execution-Phase in Non-DMA mode.
D4	CB	FDC BUSY	Indicates that FDC is in Execution-Phase of a read/write command , in Command-Phase, or in Result-Phase .
D3	D3B	FDD 3 BUSY	FDD number 3 is in the Seek mode.
D2	D2B	FDD 2 BUSY	FDD number 2 is in the Seek mode.
D1	D1B	FDD 1 BUsy	FDD number 1 is in the Seek mode.
D0	D0B	FDD 0 BUSY	FDD number 0 is in the Seek mode.

FDC supports fifteen different commands. Each of commands is initiated by a multi-byte transfer from the processor, and the result after executing of the command is a multi-byte transfer to the processor. Because the multi-byte information is interchanged between the FDC and the Processor, it is regarded that each command consists of following three phases.

Commands-Phase : The FDC receives the necessary information to perform a particular operation from the processor.
Execution-Phase : The FDC performs the specified operation .
Result-Phase : After the operation Result Status information or other information is sent to the processor.

In the Command-Phase or the Result-Phase, the processor must read out the Main Status Register before each byte of information is written into or read out from the Data Register.

When each byte of the command and the parameter is written into the FDC, bit D7 and D6 in the Main Status Register must be in high level and low level ,respectively.

Because most of the Commands need multiple bytes, the Main Status Register must be read out before each byte is transferred to the FDC. In the Result-phase, the bit D7 and D6 in Main Status Register must be both in high levels before each byte is read out from the Data Register.

The reading out of the Main Status Register before each byte transfer to the FDC is necessary only in the Command-Phase and the Result-Phase,

but it is not always necessary in the Execution-Phase.

When the FDC is in Non-DMA mode, the receipt of each data byte (if the FDD is now reading out data from the FDD) is indicated by the Interrupt signal on the eighteenth pin.

The generation of the Read signal ([-RD]=0) will not only output the data on the data bus but also reset the INT signal. If the processor can not deal with interrupts fast enough (within 13us for MFM mode.), then it examines the Main Status Register, and then bit 7 (RQM) functions just like the Interrupt signal. Similarly in the Write command, Write signal resets the Interrupt signal.

If the FDC is in the DMA mode, then the Interrupt signal is not generated during the Execution-Phase. When the each data byte is available, the FDC generates DRQ(DMA request) signal. Then the DMA controller generates both DMA Acknowledge signal and Read signal ([-DAC]=0 and [-RD]=0).

In a Read command, when the DMA acknowledge signal becomes low level, the FDC automatically resets the DRQ. In a Write command, [-WR] is substituted for [-RD]. If the Execution-Phase is terminated (Terminal Count has been inputted), the Interrupt request is generated. This means the beginning of the Result-Phase. When the first data byte is read during the Result-Phase, Interrupt signal is automatically reset. During the Result-Phase, all data bytes shown in the COMMAND TABLE must be read.

For example, the READ DATA COMMAND has seven data bytes in the Result-Phase. All seven data bytes must be read out in order to complete the READ DATA COMMAND. This FDC will not accept the next command until all these seven data bytes are read out. In the same way, all the data bytes of the other commands must be read out during the Result-Phase. The FDC has five Status Registers. The Main Status Register mentioned above can always be read out by the processor. The Other four Result Status Register (ST0,ST1,ST2,ST3) is available only in the Result-Phase, and read out only after the termination of the command .

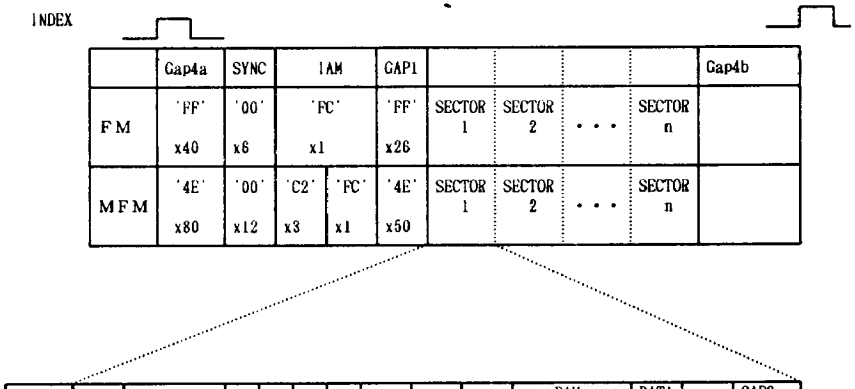
The specified command determines how many the Result Status Registers will be read. The COMMAND TABLE shows the data bytes that are sent to the FDC in the Command-Phase and read out from the FDC in the Result-Phase. That is, the command code must be sent first, and the other bytes must be sent in order. So the Command-Phase and the Result-Phase can not be shorten. When the last data byte in the Command-Phase is sent to the FDC, the Execution-Phase automatically starts. Similarly, when the last byte in the Result-Phase is read out, the command is automatically terminated, and then the FDC is ready for a new command.

4.3.2 Polling Feature of the FDC

After the SPECIFY COMMAND has been sent to the FDC, the drive select signals , the DS1 and DS0 , are automatically in the polling mode. Between the commands (and between the step pulses in the Seek mode), the FDC checks the four FDDs looking for a change of the ready signals from drive units.

If the Ready signal is changed, then the FDC generates the Interrupt signal. After the processor has issued the SENSE INTERRUPT STATUS COMMAND, the Result Status Register 0 (ST0) is read out, and the Not Ready bit (NR) in ST0 shows the present status. Because of the polling of Ready signal between the Commands, the processor can notice which drives are on line or which drives are off line.

4.3.3 Track Format (IBM Format)



	Gap4a	SYNC	IAM	GAP1					Gap4b
FM	'FF' x40	'00' x6	'FC' x1	'FF' x26	SECTOR 1	SECTOR 2	• • •	SECTOR n	
MFM	'4E' x80	'00' x12	'C2' x3	'FC' x1	'4E' x50	SECTOR 1	SECTOR 2	• • •	SECTOR n	

	SYNC	IDAM	C	H	R	N	CRC	Gap2	SYNC	DAM (DDAM)	DATA *1	CRC	GAP3 *1
FM	'00' X6	'FE' x1	x1	x1	x1	x1	x2	'FF' x21	'00' x6	'FB' ('F8') x1			
MFM	'00' x12	'A1' x3	'FE' x1	x1	x1	x1	x1	x2	'4E' x22	'00' x12	'A1' x3	'FB' ('F8') x1			

(*1) Programmable

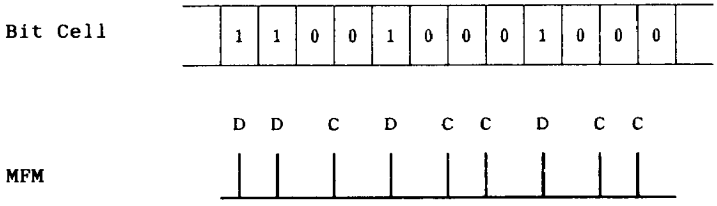
Missing Clocks in Address Marks

AM	FM		MFM	
	Data	Clock	Data	Clock
IAM	FC	D7	C2	14
IDAM	FE	C7	A1	0A
DAM	FB	C7	A1	0A
DDAM	F8	C7	A1	0A

4.3.4 MFM rules

The data bit is written where the each bit will correspond to the center of the bit sell with "1". The clock bit is written at the head of the bit cell with "0" whose previous bit cell has "0".

FIG.2 MFM Rules



D : Data Bit
C : Clock Bit

5 COMMAND

5.1 COMMAND TABLE

(x:Don't care)

READ DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		MT	MFM	SK	0	0	1	1	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
C	W	R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
		ST0								
		ST1								
		ST2								
R	R	C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

WRITE DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		MT	MFM	0	0	0	1	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
C	W	R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
		ST0								
		ST1								
		ST2								
R	R	C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

WRITE DELETED DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	0	0	1	0	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

READ DELETED DATA COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	SK	0	1	1	0	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

READ DIAGNOSTIC COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		0	MFM	0	0	0	0	1	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
C	W	R								* of command
		N								* execution
		EOT								
		GPL								
		DTL								
E										Data transfer
		ST0								
		ST1								
		ST2								
R	R	C								* ID information
		H								* of end sector
		R								* of command
		N								* execution

READ ID COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	MFM	0	0	1	0	1	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
E										Data transfer
		ST0								
		ST1								
		ST2								
R	R	C								* The first correct
		H								* ID information
		R								* read out during
		N								* Execution-Phase

FORMAT COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	MFM	0	0	1	1	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		N								
		SC								
		GPL								
		D								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* No meaning in
		H								* this case
		R								*
		N								*

SCAN EQUAL COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	MT	MFM	SK	1	0	0	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
		R								* of command
		N								* execution
		EOT								
		GPL								
		STP								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* ID information
		H								* of last compared
		R								* sector
		N								*

SCAN LOW or EQUAL COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		MT	MFM	SK	1	1	0	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
C	W	R								* of command
		N								* execution
		EOT								
		GPL								
		STP								
E										Data transfer
		ST0								
		ST1								
		ST2								
R	R	C								* ID information
		H								* of last
		R								* compared sector
		N								*

SCAN HIGH or EQUAL COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		MT	MFM	SK	1	1	1	0	1	Command code
		x	x	x	x	x	HS	DS1	DS0	
		C								* ID information of
		H								* starting sector
C	W	R								* of command
		N								* execution
		EOT								
		GPL								
		STP								
E										Data transfer
		ST0								
		ST1								
		ST2								
R	R	C								* ID information
		H								* of last
		R								* compared sector
		N								*

SEEK COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		0	0	0	0	1	1	1	1	Command code
C	W	x	x	x	x	x	x	DS1	DS0	
		NCN								
E										Seek

RECALIBRATE COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	0	1	1	1	Command code
		x	x	x	x	x	x	DS1	DS0	
E										Recalibrate

SENSE INTERRUPT STATUS COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	1	0	0	0	Command code
R	R	STO								
		PCN								

SPECIFY COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		0	0	0	0	0	0	1	1	Command code
C	W	SRT				HUT				
		HLT							ND	

SENSE DEVICE STATUS COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	0	0	0	0	0	1	0	0	Command code
		x	x	x	x	x	HS	DS1	DS0	
R	R	ST3								

INVALID COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
C	W	Invalid codes								
R	R	ST0								ST0=80H

TABLE 2 Symbols in the COMMAND TABLE

SYMBOL	NAME	DESCRIPTION
C	Cylinder Number	Indicates the cylinder number.
D	Data	Indicates the data pattern which is going to be written into data field.
D7-D0	Data Bus	8 bit data bus , D7 is MSB and D0 is LSB.
DS1,0	Drive Select	Indicates the drive number(0,1,2,3).
DTL	DATA Length	IF N=00, indicates the data length per sector which is going to be processed.
EOT	End of Track	Indicates the last Sector of a cylinder.
GPL	Gap Length	Indicates the length of Gap 3 (see 4-3-3 Track Format).
H	Head Address	Indicates the logical head address.
HS	Head Select	Indicates the physical head address.
HLT	Head Load Time	Indicates the head load time of FDD defined by Specify Command.
HUT	Head Unload Time	Indicates the head unload time after a read or write operation has completed which is defined by Specify Command .
MFM	MFM mode	If "Low" , FM mode is selected. If "High", MFM mode is selected.
MT	Multi Track	If "High" , multi track operation is to be performed.
N	Number	N is the code which indicates the number of data bytes written in a sector.
NCN	New Cylinder Number	Indicates the new cylinder number to be reached as a result of the seek operation.
ND	Non-DMA	Indicates the Non-DMA mode. Defined by the Specify Command.
PCN	Present Cylinder Number	Indicates the cylinder number when the Sense Interrupt Status Command has completed.
R	Record	Indicates the sector number.
R/W	Read/ Write	Indicates whether Read or Write.
SC	Sector	Indicates the number of sector per cylinder.
SK	Skip	Indicates the skip of the sector which has DDAM or DAM.
SRT	Step Rate Time	Indicates the step rate of FDD which is defined by Specify Command.

SYMBOL	NAME	DESCRIPTION
STP	Step	During the Scan operation , if STP is "1", then data in contiguous sector is compared byte by byte with data sent from the processor ,and if STP is "2" ,then alternate sectors are read and compared.

5.2 Command Description

During the Command-Phase, the CPU must examine the Main Status Register before the writing of the each data byte into the Data Register. The DIO and RQM in the Main Status Register must be in a low level and a high level , respectively , before each byte is written into the FDC.

5.2.1 READ DATA COMMAND

The FDC needs nine data bytes in order to execute the READ DATA COMMAND. After the READ DATA COMMAND has been issued, the FDC loads the head (if it is in unload state), and waits the specified head load time . After the head load time has passed, the FDC begins to search ID Address Marks and read ID fields. If ID information stored in the ID Register agrees with ID information in ID field read from the diskette, then the FDC outputs data from the data field byte-by-byte to the main system via the data bus.

After the read operation of the current sector has been completed, the Sector Number (R) is incremented by one , the FDC reads the data from the next sector , and outputs the data on the data bus.

This continuous read function is called a "Multi-Sector Read Operation". The READ DATA COMMAND may be terminated by receiving a Terminal Count (TC) signal. If the FDC receives a TC signal, the FDC stops outputting data to processor, but continues to read data from the current sector, and checks the CRC(Cyclic Redundancy Code) bytes, and then terminates the READ DATA COMMAND at the end of the sector.

The amount of data which can be handled with a single command to the FDC depends on MT(Multi-Track), MFM(MFM/FM), and N(Number of bytes/sector). The Transfer Capacity is shown in TABLE 3 below.

TABLE 3 Transfer Capacity

MT	MFM	N	Maximum Transfer Capacity		Final Sector
			Bytes/Sector	Number of Sector	
0	0	00	128	26	SIDE 0 SECTOR 26 or
	1	01	256		SIDE 1 SECTOR 26
1	0	00	128	52	SIDE 1 SECTOR 26
	1	01	256		
0	0	01	256	16	SIDE 0 SECTOR 15 or
	1	02	512		SIDE 1 SECTOR 15
1	0	01	256	30	SIDE 0 SECTOR 15
	1	02	512		
1	0	02	512	8	SIDE 0 SECTOR 8 or
	1	03	1024		SIDE 1 SECTOR 8
1	0	02	512	16	SIDE 1 SECTOR 8
	1	03	1024		

This FDC can read out the data from both sides of the diskette by the Multi-Track function. Data transfer will be performed from the Sector 1 of Side 0 to the last Sector of Side 1 for a particular cylinder at a time. But this function is effective to only one cylinder of the diskette.

After the reading out of the last sector, the FDC must receive the Terminal Count. If the FDC does not receive the Terminal Count signal, then the FDC sets the EN(end of cylinder) flag of ST1 to a high level and terminates the READ DATA COMMAND (bits 7 and 6 of ST0 is also set to a low level and a high level respectively : abnormal termination).

When N=0, DTL defines the data length which the FDC must treat as a sector. IF DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the data bus, but the FDC reads the whole sector internally, and then checks CRC bytes. When N≠0 DTL has no meaning.

When the READ DATA COMMAND has been completed , the head is not unloaded until the Head Unload Time(specified in the Specify Command) has passed. When the processor issues the next command (a read/write command) before head is unloaded, the head load time of the command is saved.

If the FDC can not find out the right sector until the FDC detects the Index Hole twice, and the FDC sets the ND(No Data) flag in ST1 to a high level, and the READ DATA COMMAND will be abnormal terminated (bit 7 and bit 6 in ST0 set to a low level and a high level respectively).

After the reading of the ID field and the data field of the each sector, the FDC checks the CRC bytes. If a read error (incorrect CRC bytes in the ID field) is detected, the FDC sets the DE(Data Error) flag of ST1 to a high level, and if data error in the data field is detected , the DD(Data Error in Data Field) flag in ST2 is set to a high level, and then the READ DATA COMMAND is abnormal terminated.

IF the FDC read a Deleted Data Address Mark in the diskette, and SK bit (D5 bit in the Command code)is not set, then the FDC sets CM (Control Mark) flag to a high level after reading out all the data in the sector, and terminates the READ DATA COMMAND. When SK=1, the FDC skips the Sector that has DDAM, and reads out the next sector.

During the data transfer between the FDC and the processor, the FDC must receive the service from the processor within 25us in FM mode, and 13 us in MFM mode. If the FDC does not receive this service, the FDC sets OR (Over Run) flag to a high level, and terminates the READ DATA COMMAND (abnormal termination).

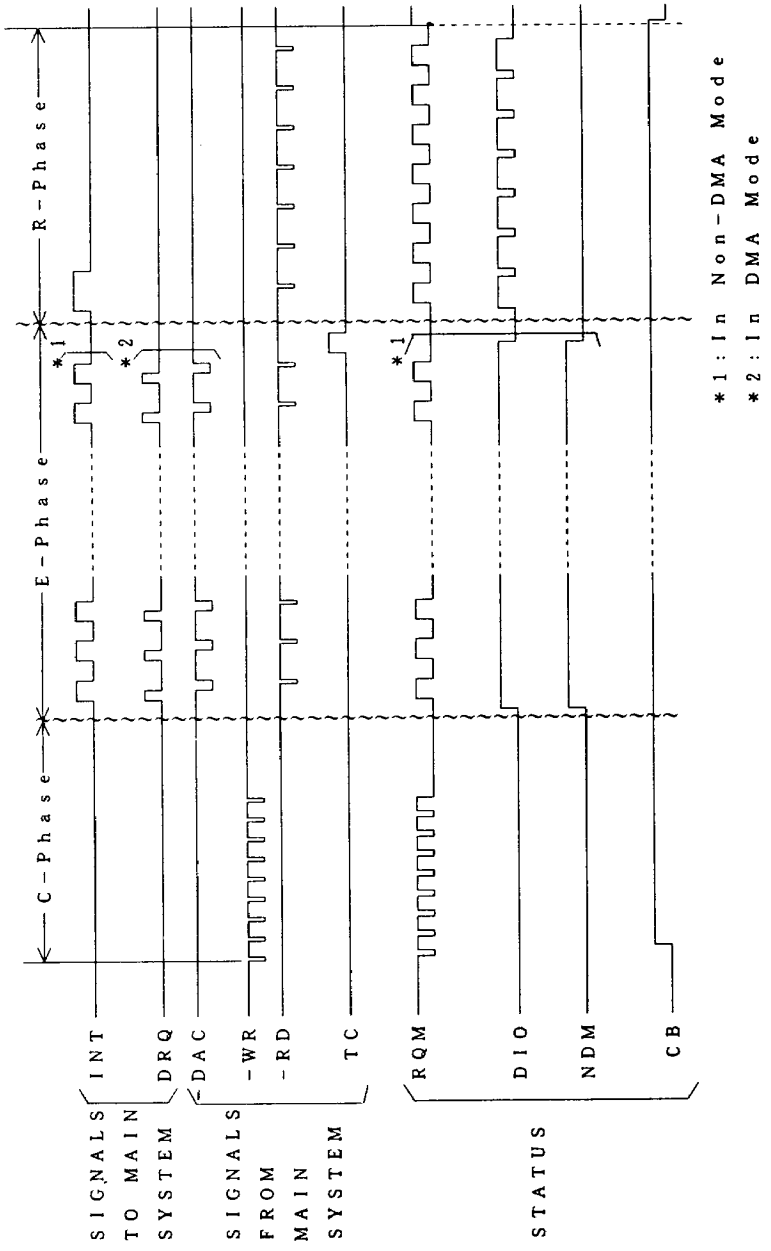
If a read (or write) operation is terminated by inputting the Terminal Count signal, the information of Result-Phase is defined by MT bit and EOT byte. TABLE 4 shows the value for C,H,R and N when the command is normally terminated.

TABLE 4 ID Information at Normal Termination

MT	EOT	Final Transferred Sector	ID Information in Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C+1	NC	R=01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C+1	NC	R=01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R=01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R+1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C+1	LSB	R=01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes: NC(No Change): The same value as the one at the beginning of command execution.
LSB(Least Significant Bit): The least significant bit of H is complemented.

FIG.3 Operation Timings of The READ DATA COMMAND



5.2.2 WRITE DATA COMMAND

The FDC needs nine data bytes in order to execute the WRITE DATA COMMAND. If the WRITE DATA COMMAND has been issued, the FDC loads the head (if the head is in the unload state). After the specified head load waiting time(defined in the SPECIFY COMMAND) has passed, the FDC begins to read the ID field. If the sector number stored in ID Register (IDR) matched with the sector number read from the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs to the FDD.

After the writing the data into the current sector, the FDC increments the sector number stored in R by one, and then the FDC writes the next data field. The FDC continues this Multi-Sector write operation until the Terminal Count signal is issued. Even if the FDC has received the Terminal Count signal, the FDC continues writing for the sector, and the data field will be completed. If the FDC receives the Terminal Count signal while the FDC is writing data in data field, then the remained data field will be filled with 00.

The FDC reads out the each sector of ID field, and checks the CRC bytes. If the FDC finds out the Read Error in ID field (incorrect CRC bytes), the FDC sets DE (Data Error) of ST1 to a high level, and terminates the WRITE DATA COMMAND(Abnormal termination).

The rules of the WRITE COMMANDs are much similar to the rules of the READ DATA COMMAND. The following items are same ; see the previous section (5.2.1).

Transfer Capacity
EN flag
Head unload time
ID information at the normal termination
Meaning of DTL when N=0 and when N≠ 0

During the execution of the WRITE DATA COMMAND, the data transfer between the processor and the FDC must be performed within 31us in FM mode, and 15us in MFM mode. If it is not performed, the FDC sets OR flag of ST1 to a high level, and terminates the command (Abnormal Termination).

5.2.3 WRITE DELETED DATA COMMAND

This command is the same command as the WRITE DATA COMMAND except that the FDC writes the DDAM (Deleted Data Address Mark) at the beginning of the Data Field instead of the normal DAM (Data Address Mark).

5.2.4 READ DELETED DATA COMMAND

This command is the same as the READ DATA COMMAND except that the FDC reads the sectors with DDAM instead of those with DAM at the beginning of a Data Field. If the FDC detects DAM and SK=0 ,then the FDC will read the whole sector and set CM flag in ST2 to a high level and terminate the command (Normal Termination). If the FDC finds out DAM and SK=1 then the FDC will skip the sector with DAM and read the next sector.

5.2.5 READ DIAGNOSTIC COMMAND

This command is the same as the READ DATA COMMAND except that the FDC reads all the data continuously from each sector of a track. Just after the FDC receives the Index signal, the FDC begins to read out all the data field on the track as a continuous block. Even if the FDC finds out the CRC error in ID or data field, the FDC continues to read data from the track. The FDC compares the ID information read out from each sector with the value stored in IDR, and if there is no comparison, the FDC sets ND flag to a high level. This command has neither the Multi-Track function nor the skip function.

This command will be terminated when EOT number of sectors have been read out. When ID Address Mark on the diskette is not found out until the FDC finds out the Index Hall twice, MA (Missing Address Mark) in ST1 is set to a high level, and the command is terminated(Abnormal Termination).

5.2.6 READ ID COMMAND

This command is used to inform the processor of the current head point. The FDC stores the first ID information to be read out. If the right ID Address Mark is not found on the diskette until the FDC finds out the Index Hall twice, the FDC sets MA flag in ST1 to a high level, and if there is no ID field without CRC error, ND flag in ST1 is set to a high level, and the command is terminated(Abnormal Termination).

5.2.7 FORMAT COMMAND

The Format Command allows an entire track to be formatted. After the Index Hall is detected, the FDC writes data on the Diskette. Gaps, Address Marks, ID fields and Data fields in IBM System34 (double density) or IBM System3740 (single density) Format are recorded. The particular format is controlled by the values programmed in N,SC,GPL and D during the Command-Phase. The data byte stored in D is written into the data field. The data bytes of ID field in each sector is provided by the processor. That is, the FDC requests four data bytes per sector for C, H, R and N. This function allows the diskette to be formatted with nonsequential sector numbers.

After the each sector is formatted, the processor must send the new values of C,H,R and N to the FDC for the next sector on the track. After a sector is formatted, the contents of the R-register is incremented by one. Thus, when the R register is read out during the Result-Phase, it contains a value of R+1. This incrementing and formatting continues for the track until the FDC detects the Index Hall for the second time. When the FDC finds the Index Hall twice, the command is terminated.

When the FDC received the Fault signal from the FDD at the end of the write operation, the FDC sets the EC flag in ST0 to a high level, and sets bit 7 and bit 6 in ST0 to a low level and a high level respectively, and terminates the command. If the Ready signal changes to a low level at the beginning of the command execution, then the command is terminated.

TABLE 5 shows the relationship of N, SC and GPL for various Sector sizes.

TABLE 5 Relationship of Sector Sizes

FORMAT	SECTOR SIZE byte/sector	N (16)	SC (16)	GPL (16)	REMARKS
FM mode	128	00	1A	1B	IBM Diskette 1
	256	01	0F	2A	IBM Diskette 2
	512	02	08	3A	
	1024	03	04	-	
	2048	04	02	-	
	4096	05	01	-	
MFM mode	256	01	1A	36	IBM Diskette 2D
	512	02	0F	54	
	1024	03	08	74	IBM Diskette 2D
	2048	04	04	-	
	4096	05	02	-	
	8192	06	01	-	

5.2.8 SCAN COMMAND

The SCAN COMMANDs allow the data read from the diskette to be compared with the data sent from the Main System (the processor in Non-DMA mode, and the DMA controller in DAM mode). The FDC compares the data byte-by-byte, and searches the sector which meets the condition(equal, low or equal, high or equal).

After a entire sector is compared ,if the condition is not met, the sector number is incremented (R+STP>R), and the scan operation is continued. The scan operation is continued until the following conditions occur ;

- o The conditions for scan are met (equal,high or equal,low or equal).
- o The last sector on the track (EOT) is reached.
- o The Terminal Count signal is received.

If the scan equal condition are met, the FDC sets SH(Scan Hit) flag in ST2 to a high level, and then the SCAN COMMAND is terminated(Normal termination). If the condition for scan is not met between the starting sector (specified by R) and the last sector (EOT) on the same cylinder, the FDC sets the SN (Scan Not Satisfied) flag in ST2 to a high level, and then terminates the command. If the FDC receives the Terminal Count from the processor or the DMA controller during the scan operation, the FDC completes the comparison of the data byte in process, and then terminates the command. TABLE 6 shows the status of bit SN and SH under the scan conditions.

TABLE 6 Scan Status Codes

COMMAND	ST2		COMMENTS
	SN	SH	
SCAN EQUAL	0	1	DISK = MAIN
	1	0	DISK ≠ MAIN
SCAN LOW or EQUAL	0	1	DISK = MAIN
	0	0	DISK < MAIN
	1	0	DISK > MAIN
SCAN HIGH or EQUAL	0	1	DISK = MAIN
	0	0	DISK > MAIN
	1	0	DISK < MAIN

If the FDC finds out the DDAM on the sector and SK=0, then the FDC regards the sector as the last sector on the cylinder, and sets the CM flag in ST2 to a high level, and terminates the command (Normal Termination). If SK=1, the FDC skips the sector with DDAM, and reads out the next sector. Then the FDC sets CM flag in ST2 to a high level in order to show that the DDAM is found out. When either STP or MT is programmed, the FDC must read out the last sector on the track. For example, if STP=02, MT=0 and the sectors are numbered in sequence 1 to 26, and SCAN COMMAND is started from the 21 Sector, then the FDC reads out the sector 21,23,25 and skips the next sector 26 , and finds out the Index Hall before reading the EOT value of 26. This result causes the abnormal termination of the command. If EOT is set at 25 or the scanning is started at the sector 20, then the command will be normal termination.

During the SCAN COMMAND, it is necessary to transfer the data which will be compared with the data read out from the diskette to the FDC by whether the processor or the DMA controller. If the data are not transferred within 27us in FM mode and 13us in MFM mode, the FDC sets the OR (Over Run) flag in ST1, and terminates the command (Abnormal Termination).

5.2.9 SEEK COMMAND

This command is used to move the Read/Write Head from cylinder to cylinder. The FDC compares the PCN which is current head position with the NCN. If there is a difference, the FDC performs the following operation.

PCN < NCN : Direction signal to the FDD is set to a high level,and the Step Pulses are issued (Step In).
PCN > NCN: Direction signal to the FDD is set to a low level,and the Step Pulses are issued (Step Out).

The rate of outputting the step pulses is controlled by the SRT (Step Rate Pulse) in the SPECIFY COMMAND. The FDC compares NCN with PCN at outputting the step pulses, and if NCN=PCN, then SE (Seek End) flag in ST0 is set to a low level, and the command is terminated. The FDC is in FDC Busy state during the Command-Phase of this command, but the FDC is in Non-Busy state during the Execution-Phase of this command. If the FDC

is in Non-Busy state, the FDC accepts another SEEK COMMAND. This function allows the FDC to do the parallel seek operation for up to 4 FDDs at a time.

If the FDD is in the Not Ready state at the beginning of the Execution-Phase of this command or during the seek operation, the NR (Not Ready) flag in ST0 is set to a high level and the command is terminated.

5.2.10 RECALIBRATE COMMAND

The Read/Write Head within the FDD is moved to the Track 0 position under control of the RECALIBRATE COMMAND. The FDC clears the contents of PCN register, and checks the Track 0 signal. If the Track 0 signal is in a low level, the FDC sets the Direction signal to a low level, and issues the Step Pulses.

When the Track 0 signal changes to a high level, the FDC sets SE (Seek End) flag to a high level, and terminates the command. If the Track 0 signal is still low after the FDC has issued the 77 Step Pulses, SE flag and EC flag in ST0 are set to both high levels, and the command is terminated. The RECALIBRATE COMMAND is the same as the SEEK COMMAND about the function to overlap the operation to multiple FDDs and about the loss of the Ready signal.

5.2.11 SENSE INTERRUPT STATUS COMMAND

The FDC generates the Interrupt signal by the following reasons.

1 The beginning of Result-Phase in the Following commands:
   - a READ DATA COMMAND
   - b READ DIAGNOSTIC COMMAND
   - c READ ID COMMAND
   - d READ DELETED DATA COMMAND
   - e WRITE DATA COMMAND
   - f FORMAT COMMAND
   - g WRITE DELETED DATA COMMAND
   - h SCAN COMMANDS

2 The change of Ready line of FDD.
3 At the end of the SEEK or RECALIBRATE COMMAND.
4 During the Execution-Phase in the Non-DMA mode.

Interrupts caused by reason 1 and 4 occur during the normal command operation, and the processor can notice the interrupts easily. But the interrupts caused by the reason 2 and 3 may be identified with the request of issuing the SENSE INTERRUPT STATUS COMMAND. When this command is issued, Interrupt signal is reset, and bit 5, bit 6 and bit 7 in ST0 indicate the reason of the interrupt.

Neither the SEEK nor the RECALIBRATE COMMAND has a Result-Phase. Therefore, it is necessary to use the SENSE INTERRUPT COMMAND after these commands in order to terminate them effectively and confirm the head position (PCN).

TABLE 7 SEEK , INTERRUPT CODES

INTERRUPT CODE BIT 7	INTERRUPT CODE BIT 6	SEEK END BIT 5	MEANING
1	1	0	Changing of the state of the READY LINE
0	0	1	Normal Termination of the SEEK and RECALIBRATE COMMAND
0	1	1	Abnormal Termination of the SEEK and RECALIBRATE COMMAND

5.2.12 SPECIFY COMMAND

This SPECIFY COMMAND initializes the values of three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution-Phase of the read/write commands to the unloading of the head. This timer is programmable from 16 to 240 ms at intervals of 16 ms (01=16ms, 02=32ms,...,0F=240ms).

The SRT defines the time interval between step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F=1ms,E=2ms ,...,0=16ms). The HLT defines the time from the rising of the Head Load signal to the starting of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2ms (01=2ms, 02=4ms, 03=6ms,...,7F=254ms).

The interval times mentioned above are a direct function of the clock. The times indicated above are for a 8MHz clock. If the clock frequency is 4MHz (mini floppy), all the times are twice as long as the times indicated above.

The ND bit is a flag to select the DMA operation or Non-DMA operation. If ND is in a high level then Non-DMA mode is selected, and if ND is in a low level then DMA mode is selected.

5.2.13 SENSE DEVICE STATUS COMMAND

The processor may use this command whenever it wishes to know the status of the FDDs. The drive status information is contained in ST3.

5.2.14 INVALID COMMAND

If an invalid command (a command not defined above) is send to the FDC, the FDC terminates the command. The FDC does not generate the Interrupt signal during the Result-Phase. Bit 6 and bit 7 in the Main Status Register set to both high levels indicates to the processor that the FDC is in the Result-Phase and that the contents of ST0 must be read out. ST0 is set to a 80H showing that an invalid command was received.

The SENSE INTERRUPT STATUS COMMAND must be sent after an interrupt of the SEEK COMMAND or RECALIBRATE COMMAND has occurred, otherwise the FDC

regards this command as invalid. The users may use this command as a Non-Op command to place the FDC in a stand-by or non-operation state.

5.3 RESULT STATUS REGISTER

5.3.1 RESULT STATUS REGISTER 0 (ST0)

BIT	SYMBOL	NAME	DESCRIPTION
D7 D6	IC	Interrupt Code	D7=0 and D6=0 Normal Termination of Command (NT), Command was completed and properly executed.
			D7=0 and D6=1 Abnormal Termination of Command(AT). Command execution was started, but was not successfully completed.
			D7=1 and D6=0 Command was Invalid Command(IC). The command which has been issued was not started.
			D7=1 and D6=1 Abnormal Termination because of the changing of the Ready Line from the FDD during the execution of command.
D5	SE	Seek End	This flag is set to a "1",when the SEEK COMMAND was completed.
D4	EC	Equipment Check	When the FDC received the Fault signal from the FDD, or when the Track 0 signal was not set to a "1" after 77 step pulses during the RECALIBRATE COMMAND, this flag is set to a "1".
D3	NR	Not Ready	When the FDD is in the Not-Ready state and a read/write command is issued, this flag is set. For example, when a read/write command is issued for Side 1 of a single sided drive, this flag is set.
D2	HD	Head Address	This flag indicates the state of the head at interrupt.
D1 D0	DS1 DS0	Drive Select 0,1	These flags indicate the drive number at interrupt.

5.3.2 RESULT STATUS REGISTER 1 (ST1)

BIT	SYMBOL	NAME	DESCRIPTION
D7	EN	End of Cylinder	This flag is set when the FDC tries to access a sector beyond the last sector of a cylinder.
D6	-		
D5	DE	Data Error	This flag is set when the FDC finds the CRC Error either in the ID field or the data field.
D4	OR	Over Run	This flag is set when the FDC does not receive the service from the main system during data transfers within a certain time interval.
D3	-		
D2	ND	No Data	o This flag is set when the FDC can not find out the sector specified in the IDR during the execution of following commands: READ DATA READ DELETED DATA WRITE DATA WRITE DELETED DATA SCAN o This flag is set when the FDC can not find the ID field without the CRC error during the execution of the READ ID COMMAND. o This flag is set when the starting sector cannot be found during the executing the READ DIAGNOSTIC COMMAND.
D1	NW	Not Writable	This flag is set if the FDC detects the write protect signal from the FDD during the executing following commands: WRITE DATA WRITE DELETED DATA FORMAT
D0	MA	Missing Address Mark	o This flag is set if IDAM cannot be found out until the FDC finds the Index Hall twice. o This flag is set if the FDC can not find the DAM or DDAM. The MD flag of ST2 is also set in this case.

5.3.3 RESULT STATUS REGISTER 2 (ST2)

BIT	SYMBOL	NAME	DESCRIPTION
D7	-		
D6	CM	Control Mark	While executing the READ DATA or the SCAN COMMAND, this flag is set when the FDC finds out the sector with the DDAM. During executing the READ DELETED DATA COMMAND, this flag is set when the FDC finds out the Sector with the DAM.
D5	DD	Data Error in Data Field	This flag is set when the FDC detects a CRC Error in data field.
D4	NC	No Cylinder	This flag is set when the contents of C on the medium is different from that stored in the IDR. This flag is related with the ND flag.
D3	SH	Scan Equal Satisfied	This flag is set if the condition of "equal" is satisfied during the execution of the SCAN COMMAND.
D2	SN	Scan Not Satisfied	This flag is set if the FDC cannot find out the sector which satisfies the condition during the execution of the SCAN COMMAND.
D1	BC	Bad Cylinder	This flag is set if the content of C on the medium is FF and differs from that stored in IDR. This bit is related with the ND bit.
D0	MD	Missing Address Mark in Data Field	This flag is set if the FDC cannot find out the DAM or DDAM while the data are read from the medium.

5.3.4 RESULT STATUS REGISTER 3 (ST3)

BIT	SYMBOL	NAME	DESCRIPTION
D7	FLT	Fault	This bit indicates the state of the Fault signal from the FDD.
D6	WP	Write Protect	This bit indicates the state of the the Write Protect signal from the FDD.
D5	RDY	Ready	This bit indicates the state of the Ready signal from the FDD.
D4	TK0	Track 0	This bit indicates the state of the Track 0 signal from the FDD.
D3	2S	Two Side	This bit indicates the state of the Two Side signal from the FDD.
D2	HD	Head Address	This bit indicates the state of the Head Select signal to the FDD.
D1	DS1	Drive Select 1	This bit indicates the state of the Drive Select 1 signal to the FDD.
D0	DS0	Drive Select 0	This bit indicates the state of the Drive Select 0 signal to the FDD.

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT
Power Supply	VDD	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to +7.0	V
Operating Temperature	Topr	-10 to + 70	°C
Storage Temperature	Tstg	-40 to +125	°C

6.2 DC CHARACTERISTICS

Ta = -10°C to +70°C VDD = 5V ± 5%

PARAMETER	SYMBOL	MAX	MIN	UNIT	CONDITION
Input Low Voltage	VIL	0	0.8	V	
Input High Voltage	VIH	2.2	VDD	V	
Output Low Current	IOL	2.0	-	mA	VOL=0.4V
Output High Current	IOH	-2.0	-	mA	VOH=4.6V
Input Low Leak Current	IIL	-10	+10	uA	Vin=0V
Input High Leak Current	IIH	-10	+10	uA	Vin=Vdd
Supply Current	IDD	-	10	mA	

6.3 AC CHARACTERISTICS

6.3.1 AC CHARACTERISTICS

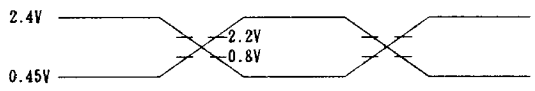
Ta = -10°C to +70°C VDD = 5V ± 5%

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Cycle Time	tCY	120			ns	
Clock "High" Period	tCH	40			ns	
-RS,-CS,-DAC Setup Time to -RD↓	tSR	0			ns	
-RS,-CS,-DAC Hold Time from -RD↑	tRS	0			ns	
-RD Pulse Width	tRR	250			ns	
Data Delay Time from -RD↓	tDR			200	ns	
Data Float Delay Time from -RD↑	tRD	20		100	ns	
-RS,-CS,-DAC Setup Time to -WR↑	tSW	0			ns	
-RS,-CS,-DAC Hold Time from -WR↑	tWS	0			ns	
-WR Pulse Width	tWW	250			ns	
Data Setup Time to -WR↑	tDW	30			ns	*3
Data Hold Time from -WR↑	tWD	30			ns	*3
INT Delay Time from -RD↑	tRI			500	ns	*1
INT Delay Time from -WR↑	tWI			500	ns	*1
DMA Cycle Time	tDRQCY	13			us	*1
-DAC↓ to DQR↓	tACDRQ			200	ns	
DRQ↑ to -RD↓	tDRQR	800			ns	*1
DRQ↑ to -WR↓	tDRQW	250			ns	*1
DRQ↑ to -RD↑/WR↑	tDRQRW			12	us	*1

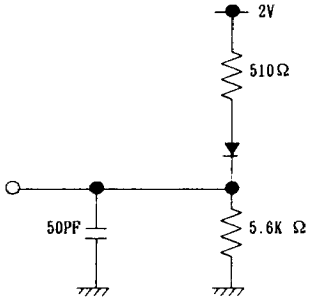
PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
TC Pulse Width		tTC	1			tCY	
RST Pulse Width		tRST	14			tCY	
WCK Cycle Time	FM mode	tWCY		2 or 4		us	*2
	MFM mode	tWCY		1 or 2		us	*2
WCK "High" Period		tWCH	100	250	350	ns	
PS0,PS1 Delay Time from WCK↑		tCP			100	ns	
WDT Delay Time from WCK↑		tCD			100	ns	
WE Delay Time from WCK↑		tCWE			100	ns	
WDT "High" Pulse Width		tWDD	tWCH-50			ns	
RDT "High" Pulse Width		tRDD	40			ns	
DW Cycle Time	FM mode	tWWCY		2 or 4		us	*2
	MFM mode	tWWCY		1 or 2		us	*2
DW Setup Time to RDT↑		tWRD	15			ns	
DW Hold Time from RDT↓		tRDW	15			ns	
DS0,DS1 Setup Time to -RW/SK↑		tDSS	12			us	*1
-RW/SK Hold Time from LC/DR		tSD	7			us	*1
LC/DR Setup Time to FR/STP↑		tDST	1			us	*1
DS0,DS1 Hold Time from FR/STP↓		tSTDS	5			us	*1
STP "High" Pulse Width		tSTP		7		us	*1
FR "High" Pulse Width		tFR	8		10	us	*1
-RW/SK Hold Time from LC/DR		tDS	30			us	*1
LC/DR Hold Time from FR/STP↓		tSTD	24			us	*1
STP Cycle Time		tSC	33			us	*1
IDX "High" Pulse Width		tIDX		625		us	*1

NOTE: *1 8MHz Clock
*2 The former is for standard floppy
The latter is for mini floppy
*3 PRELIMINARY

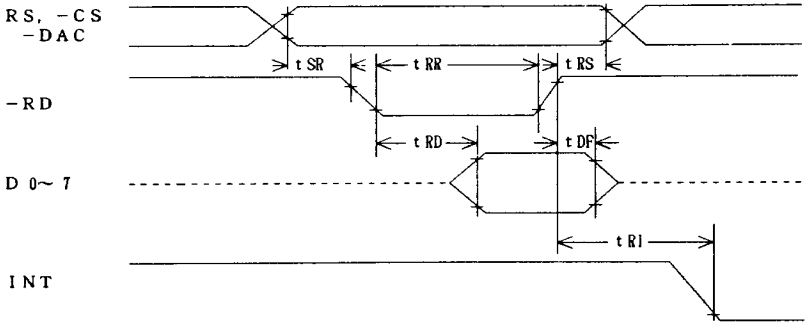
6.3.2 AC Test Waveform



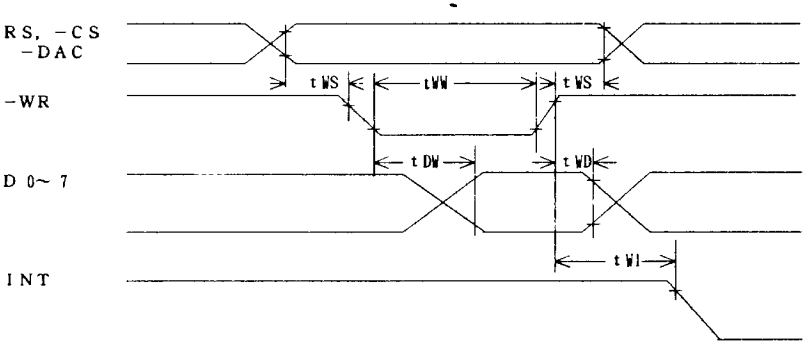
6.3.3 External Loading Condition for Terminal



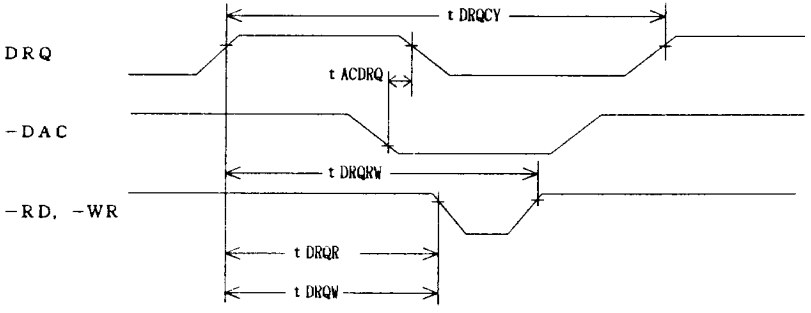
6.3.4 Read Operation



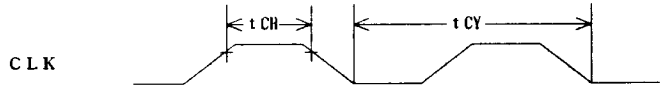
6.3.5 Write Operation



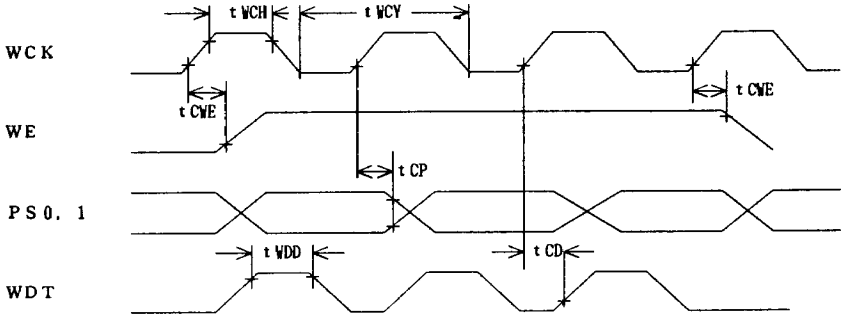
6.3.6 DMA Operation



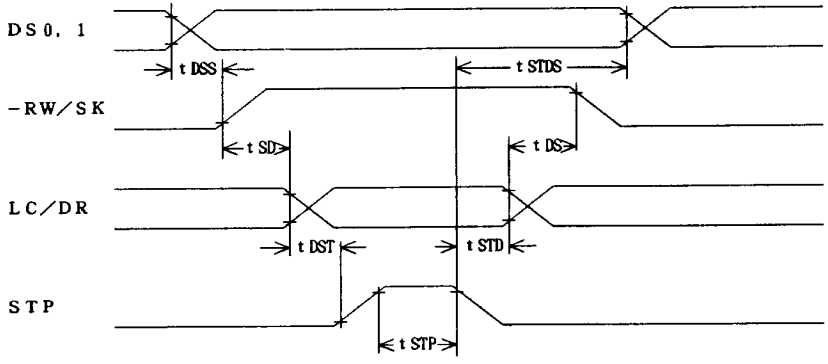
6.3.7 Clock Waveform



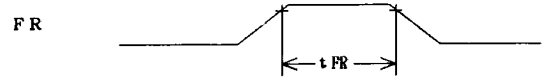
6.3.8 FDD Write Operation



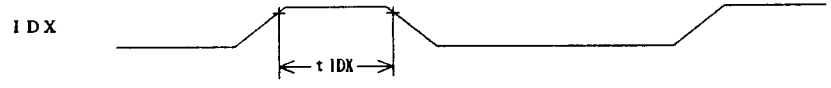
6.3.9 Seek Operation



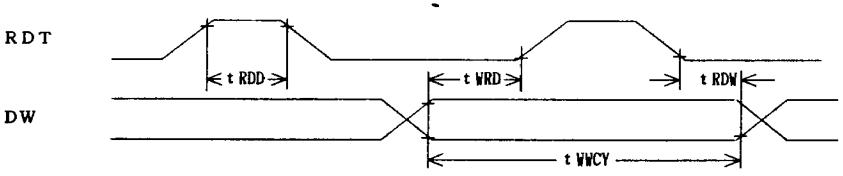
6.3.10 Fault Reset



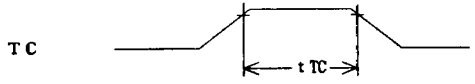
6.3.11 Index



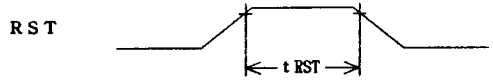
6.3.12 FDD Read Operation



6.3.13 Terminal Count

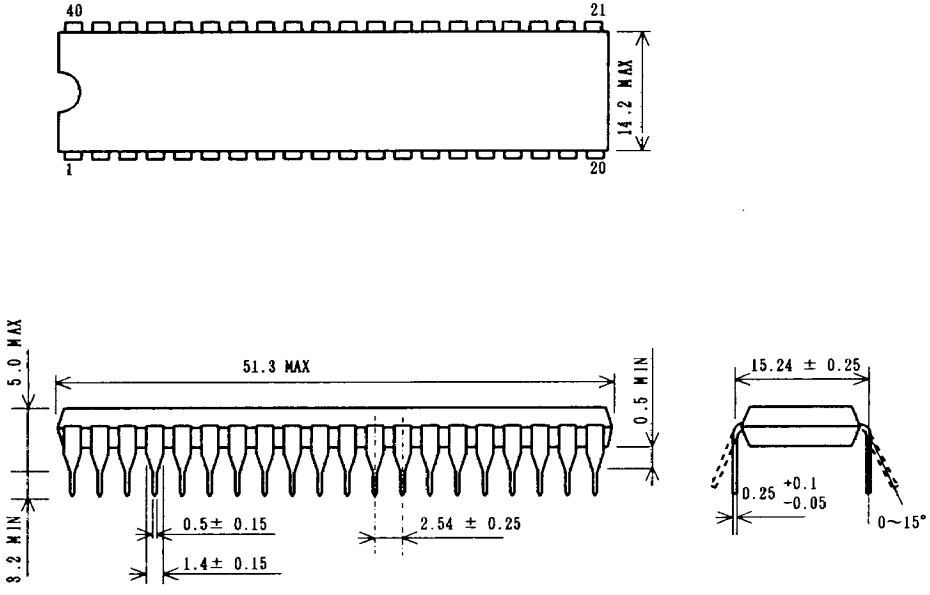


6.3.14 Reset



7 PACKAGE OUTLINE

DIP 40 PIN (PLASTIC PACKAGE) Unit: mm



mini FP 44 PIN (PLASTIC PACKAGE)

Unit : mm