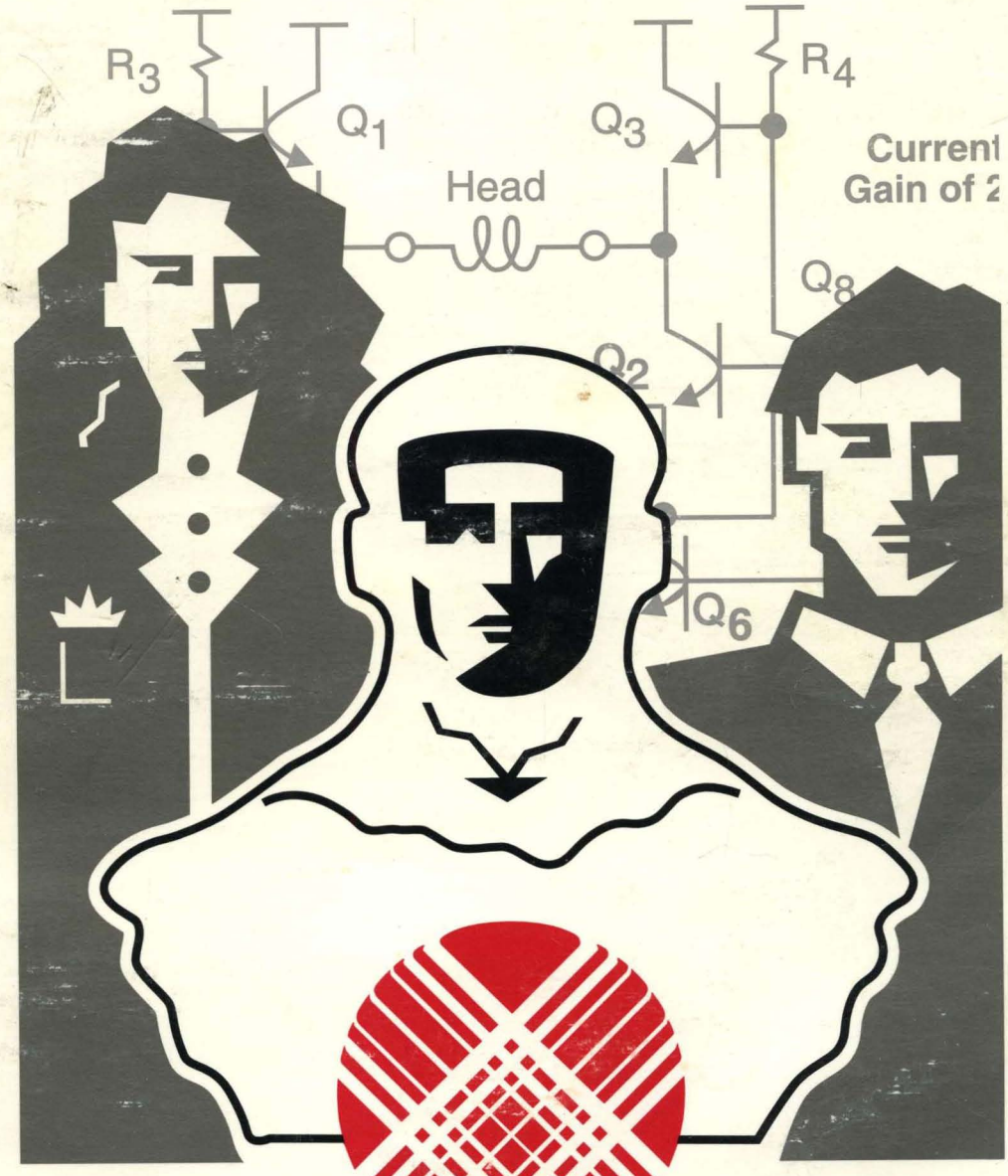
DATA STORAGE INTEGRATED CIRCUITS



VTC Inc.

Value The Customer

DATA STORAGE
INTEGRATED CIRCUITS

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VTC Inc.
Value the Customer™

The leader in quality, high-performance integrated circuits and customer service for the mass storage industry.

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DATA SHEET AND PRODUCT DEFINITIONS

Advance Information: This data sheet contains the design specifications for products in development. Specifications may change in any manner without notice. Typically this indicates first silicon has been evaluated, but not completely verified.

Preliminary: This data sheet contains preliminary data. Supplementary data will be published at a later date. VTC reserves the right to make changes at any time without notice in order to improve design or enhance the product. Preliminary indicates the product is in the first production stage.

No Identification: This data sheet contains final specifications as confirmed through design, verification and device characterization. This device is in final production.

ATTENTION
JEDEC-14/Symbol

Although all VTC products have input and output circuits that protect against damage due to high static voltage or electrostatic fields, VTC still recommends following normal ESD precautions for handling semiconductor devices.

VTC Incorporated reserves the right to make changes to its products without notice in order to improve design, performance, function or reliability. VTC assumes no responsibility for use of any circuits described or represented other than the circuitry embodied in its products.

DB007-6—Printed 994

QUALITY AND RELIABILITY ASSURANCE

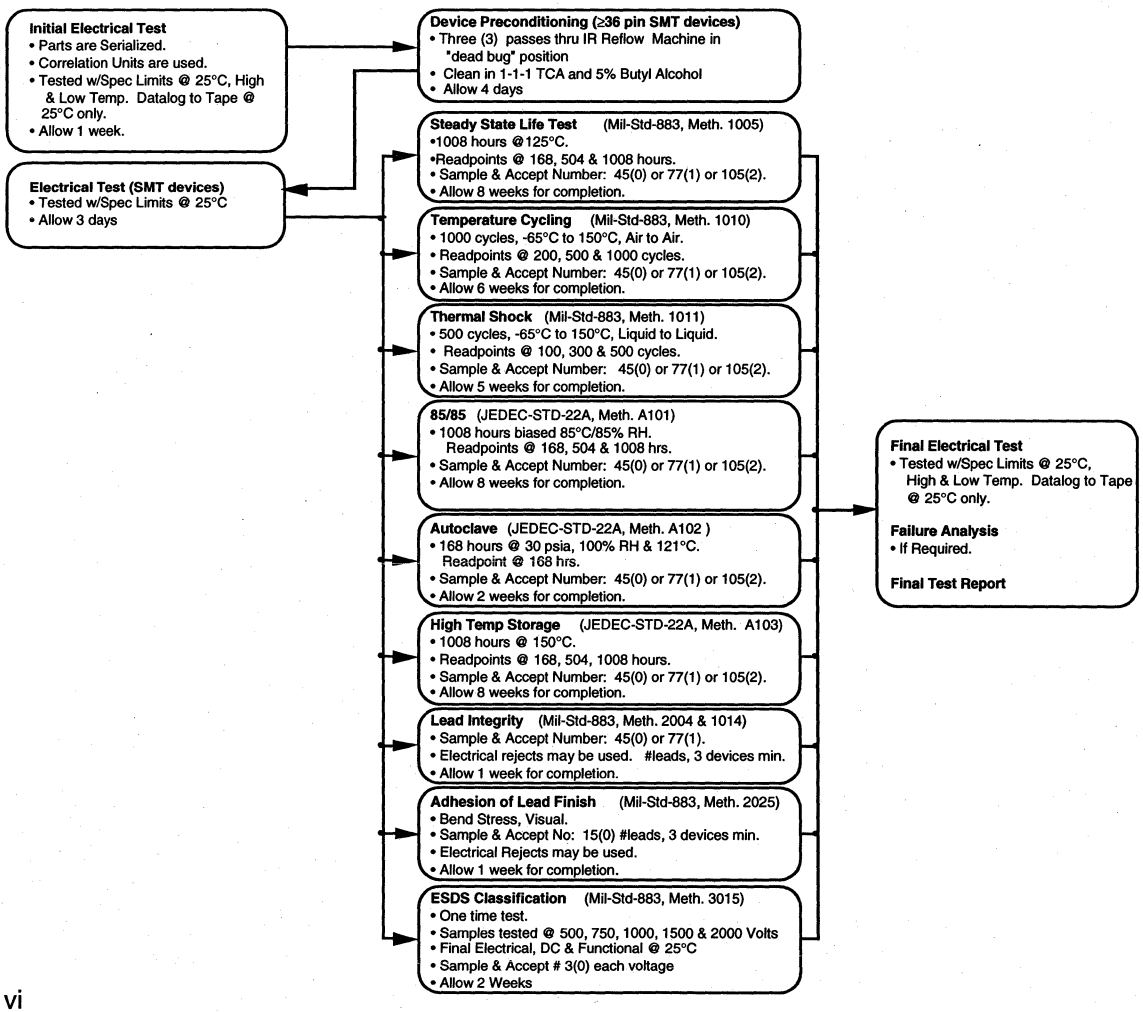
VTC's quality journey encompasses every facet of its business from marketing to manufacturing.

VTC's objective is to establish industry standards for quality and reliability and to be recognized by its customers as a company dedicated to providing exceptional service with honesty and integrity.

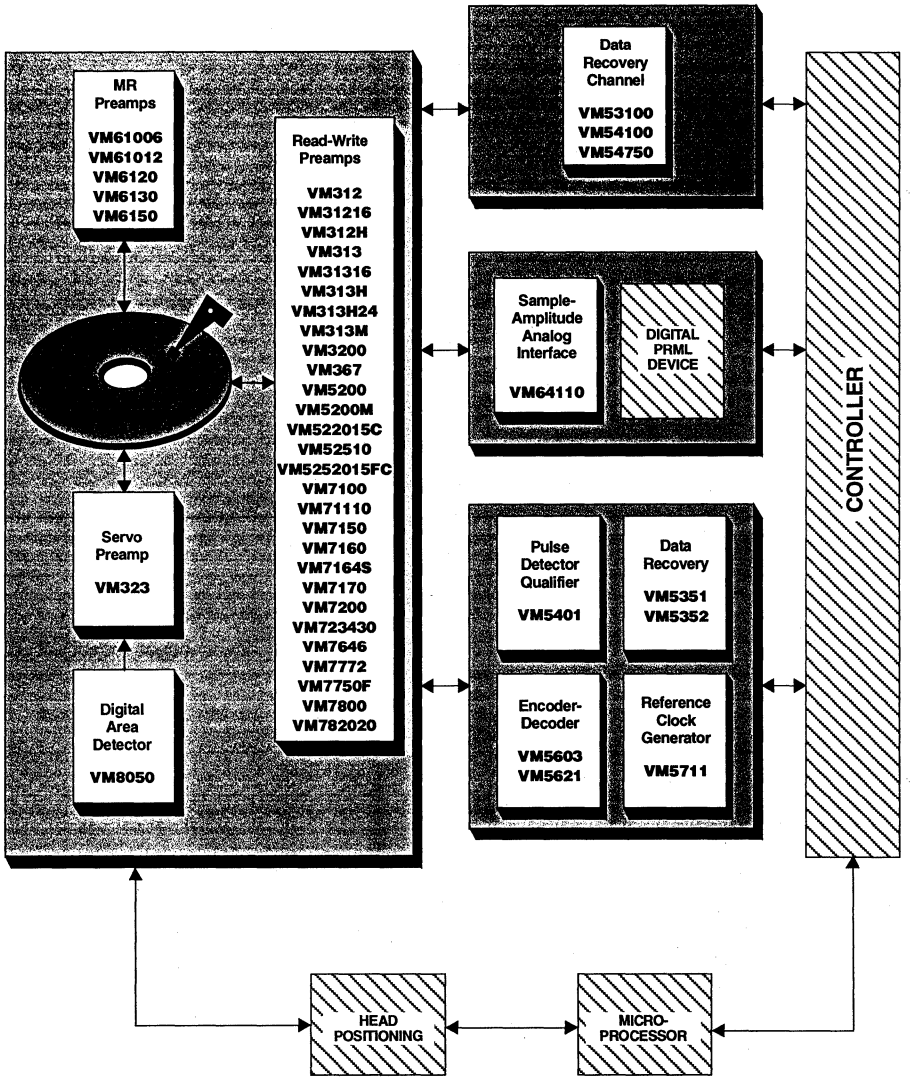
VTC understands that success depends on the high **quality** of products, on the excellence of **service** provided to customers, and on the low **cost** of producing products. To meet the goals of quality, service and cost, VTC involves all its employees in a program of **continuous improvement** in the following ways:

- Employees are trained in the use of on-line and off-line statistical process control tools, which enables them to understand and reduce variability in manufacturing processes with 6σ as a goal.
- Quality is designed into products and processes, thus eliminating dependence on quality inspections.
- Highly focused project teams use time-proven problem analysis and solution tools.
- PPM and qualification/ORT programs are used to monitor progress.

Commercial Qualification Process



THE VTC CHANNEL



READ/WRITE PREAMPLFIERS SELECTOR GUIDE

Product	Current Revision	Pins	Package Type	Channels	WDI	Read Gain (V/V) Typ.	Input Noise (nV/√Hz) Max.	Input Cap. (pF) Max.	Current Gain (mA/mA)
MR HEAD									
VM61006FTQJ	Aug-94	64	TQFP	6	PECL	350	0.55	10	20
VM61006TQJ	Aug-94	64	TQFP	6	PECL	350	0.55	10	20
VM61012XA	Aug-94		DIE	12	PECL	500	0.55	10	20
VM61210FTQJ	Aug-94	64	TQFP	10	PECL	150	0.65	18	20
VM61210FTQK	Aug-94	64	TQFP	10	PECL	150	0.65	18	20
VM61210TQJ	Aug-94	64	TQFP	10	PECL	150	0.65	18	20
VM61210TQK	Aug-94	64	TQFP	10	PECL	150	0.65	18	20
VM61312FXC	Aug-94		DIE	12	PECL	350	0.55	10	20
VM61312SXC	Aug-94		DIE	12	PECL	350	0.95	10	20
VM61312XC	Aug-94		DIE	12	PECL	350	0.55	10	20
THREE-TERMINAL									
VM367N425POK	Aug-94	24	SOIC	4	TTL	250	0.95	22	20
VM367N225PO20L	Aug-94	24	SOIC	2	TTL	250	0.95	22	20
VM7002NOL	Aug-94	16	SOIC	2	TTL	200	0.85	22	20
VM7002POL	Aug-94	16	SOIC	2	TTL	200	0.85	22	20
VM7004POL	Aug-94	20	SOIC	4	TTL	200	0.85	22	20
VM7004SSL	Aug-94	20	SSOP	4	TTL	200	0.85	22	20
VM7004VSL	Aug-94	20	VSOP	4	TTL	200	0.85	22	20
TWO-TERMINAL									
VM31210PO36L	Aug-94	52	PQFP	16	TTL	150	0.8	25	1
VM31216QFL	Aug-94	52	PQFP	16	TTL	150	0.8	25	1
VM3126SSL	Aug-94	28	SSOP	6	TTL	150	0.8	25	1
VM3128PML	Aug-94	34	SOIC-Mirror	8	TTL	150	0.8	25	1
VM3128PO34L	Aug-94	34	SOIC	8	TTL	150	0.8	25	1
VM3129POL	Aug-94	34	SOIC	9	TTL	150	0.8	25	1
VM312H14PLL	Aug-94	44	PLCC	14	TTL	250	0.8	25	1
VM312H14POL	Aug-94	44	SOIC	14	TTL	250	0.8	25	1
VM312H14QFL	Aug-94	44	PQFP	14	TTL	250	0.8	25	1
VM31316QFJ	Aug-94	52	PQFP	16	PECL	150	0.8	25	1
VM3139PO36L	Aug-94	36	SOIC	9	PECL	150	0.8	25	1
VM3139PO36M	Aug-94	36	SOIC	9	PECL	150	0.8	25	1
VM3139POL	Aug-94	34	SOIC	9	PECL	150	0.8	25	1
VM313H13POL	Aug-94	44	SOIC	13	PECL	250	0.8	25	1
VM313H14POL	Aug-94	44	SOIC	14	PECL	250	0.8	25	1
VM3204POK	Aug-94	20	SOIC	4	TTL	150,200,300	0.7	20/12	22
VM3204SSK	Aug-94	20	SSOP	4	TTL	150,200,300	0.7	20/12	22
VM521015FPO36L	Aug-94	36	SOIC	10	PECL	150	0.75	18	20
VM521015FTQL	Aug-94	48	TQFP	10	PECL	150	0.75	18	20
VM521015PO36L	Aug-94	36	SOIC	10	PECL	150	0.75	18	20
VM521015XC	Aug-94		DIE	10	PECL	150	0.75	18	20
VM521420TQ64L	Aug-94	64	TQFP	14	PECL	200	0.75	18	20
VM521420XC	Aug-94		DIE	14	PECL	200	0.75	18	20
VM522015CTQL	Aug-94	64	TQFP	20	PECL	150	0.8	13	20
VM522015FTQL	Aug-94	64	TQFP	20	PECL	150	0.75	18	20
VM522015FTXC	Aug-94		DIE	20	PECL	150	0.75	18	20
VM522015TQL	Aug-94	64	TQFP	20	PECL	150	0.75	18	20
VM522015TXC	Aug-94		DIE	20	PECL	150	0.75	18	20

*Based on typical head load.

Write Current Range (mA)	Write Voltage (Vp-p) Min.	Damping Resistor	Rise/Fall Time L=0, R=0 (ns) Max.	Multiple Servo Write	Head Induct. Range (μH)	Power Supply	Recommend New Design?
10 - 30	4.5	YES	6*	NO	0.1 - 2	+5V; -4.5V	YES
10 - 30	4.5	YES	6*	NO	0.1 - 2	+5V; -4.5V	YES
10 - 30	4.5	YES	6*	NO	0.1 - 2	+5V; -4.5V	YES
20 - 40	4.5	YES	4*	YES	0.4 - 1	+5V; -3V	YES
20 - 40	4.5	YES	4*	YES	0.4 - 1	+5V; -3V	YES
20 - 40	4.5	YES	4*	YES	0.4 - 1	+5V; -3V	YES
20 - 40	4.5	YES	4*	YES	0.4 - 1	+5V; -3V	YES
20 - 40	4.5	YES	4*	NO	0.15 - 0.4	+5V; -4.5V	YES
20 - 40	4.5	YES	4*	NO	0.15 - 0.4	+5V; -4.5V	YES
20 - 40	4.5	YES	4*	NO	0.15 - 0.4	+5V; -4.5V	YES
4 - 40	10	NO	TBD	YES	1 - 10	+5V	YES
4 - 40	10	NO	TBD	YES	1 - 10	+5V	YES
15 - 50	4.8	YES	10	NO	1 - 5	+5V	YES
15 - 50	4.8	YES	10	NO	1 - 5	+5V	YES
15 - 50	4.8	YES	10	NO	1 - 5	+5V	YES
15 - 50	4.8	YES	10	NO	1 - 5	+5V	YES
15 - 50	4.8	YES	10	NO	1 - 5	+5V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
5 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
10 - 40	7	YES	5	NO	0.2 - 3	+5V, +12V	YES
2 - 25	4.5	YES	6	NO	0.2 - 5	3V - 5V	YES
2 - 25	4.5	YES	6	NO	0.2 - 5	3V - 5V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES
5 - 35	9	OPTIONAL	2	NO	0.2 -1.5	+5V, +12V	YES

READ/WRITE PREAMPLFIERS SELECTOR GUIDE (continued)

Product	Current Revision	Pins	Package Type	Channels	WDI	Read Gain (V/V) Typ.	Input Noise (nV/√Hz) Max.	Input Cap. (pF) Max.	Current Gain (mA/mA)
VM710430POL	Aug-94	16	SOIC	4	TTL	300	0.75	23	20
VM710430SSL	Aug-94	20	SSOP	2	TTL	300	0.75	23	20
VM710430VSL	Aug-94	20	VSOP	4	TTL	300	0.75	23	20
VM7104POL	Aug-94	20	SOIC	4	TTL	150 - 300	0.75	23	20
VM7104SSL	Aug-94	20	SSOP	4	TTL	150 - 300	0.75	23	20
VM710630SSJ	Aug-94	24	SSOP	6	TTL	300	0.75	23	20
VM7108POL	Aug-94	36	SOIC	4	TTL	150 - 300	0.75	23	20
VM711420POJ	Aug-94	20	SOIC	20	TTL	200	0.6	15	20
VM711420SSJ	Aug-94	20	SSOP	20	TTL	200	0.6	15	20
VM711420VSJ	Aug-94	20	VSOP	20	TTL	200	0.6	15	20
VM711620SSJ	Aug-94	24	SSOP	6	TTL	200	0.5	15	20
VM711630SSJ	Aug-94	24	SSOP	6	TTL	300	0.5	15	20
VM7124VSL	Aug-94	20	VSOP	4	TTL	300	0.75	23	1
VM7128POL	Aug-94	36	SOIC	8	TTL	300	0.75	23	1
VM7142POL	Aug-94	16	SOIC	2	PECL	300	0.75	33	20
VM7158POJ	Aug-94	36	SOIC	8	PECL	200 - 300	0.65	18	20
VM715N2POL	Aug-94	16	SOIC	2	PECL	200 - 300	0.65	18	20
VM715N4POK	Aug-94	20	SOIC	4	PECL	200 - 300	0.65	18	20
VM716430SPOK	Aug-94	20	SOIC	4	TTL	300	0.65	18	20
VM716430SSSK	Aug-94	20	SSOP	4	TTL	300	0.65	18	20
VM716430SVSK	Aug-94	20	VSOP	4	TTL	300	0.65	18	20
VM7164SSJ	Aug-94	20	SSOP	4	TTL	200 - 300	0.65	23	20
VM716N8POK	Aug-94	36	SOIC	8	TTL	200 - 300	0.65	23	20
VM7204POJ	Aug-94	20	SOIC	4	TTL	200	0.75	23	20
VM7204SSJ	Aug-94	20	SSOP	4	TTL	200	0.75	23	20
VM7204VSJ	Aug-94	20	VSOP	4	TTL	200	0.75	23	20
VM7206SSJ	Aug-94	28	SSOP	6	TTL	200	0.75	23	20
VM7208POJ	Aug-94	36	SOIC	8	TTL	200	0.75	23	20
VM720H4POL	Aug-94	20	SOIC	4	TTL	275	0.75	23	20
VM720H8POJ	Aug-94	16	SOIC	8	TTL	275	0.75	23	20
VM723430POP	Aug-94	20	SOIC	4	TTL	300	0.75	23	1
VM723430SSP	Aug-94	20	SSOP	4	TTL	300	0.75	23	1
VM7238POJ	Aug-94	36	SOIC	8	TTL	250	0.75	23	1
VM775430FPOJ	Aug-94	20	SOIC	4	PECL	300	0.65	11	20
VM775430FSSJ	Aug-94	20	SSOP	4	PECL	300	0.65	11	20
VM775630FSSJ	Aug-94	24	SSOP	6	PECL	300	0.65	13	20
VM780420POJ	Aug-94	20	SOIC	4	PECL	200	0.65	15	20
VM780620SSJ	Aug-94	24	SSOP	6	PECL	200	0.65	15	20
VM781020XB	Aug-94		DIE	10	PECL	200	0.65	15	20
VM782020TQJ	Aug-94	64	TQFP	20	PECL	200	0.65	15	20
VM782020XA	Aug-94	64	DIE	20	PECL	200	0.65	15	20
VM7851015XB	Aug-94		DIE	10	PECL	150	0.65	15	20
VM7851020POK	Aug-94	36	SOIC	10	PECL	200	0.65	15	20
VM7851020XB	Aug-94		DIE	10	PECL	200	0.65	15	20
VM785420POJ	Aug-94	20	SOIC	4	PECL	200	0.65	15	20
VM785437FPOJ	Aug-94	20	SOIC	4	PECL	270	0.65	15	20
VM785620SSJ	Aug-94	24	SSOP	6	PECL	200	0.65	15	20
VM785620XA	Aug-94		DIE	6	PECL	200	0.65	15	20
VM785820POK	Aug-94	36	SOIC	8	PECL	200	0.65	15	20

Write Current Range (mA)	Write Voltage (Vp-p) Min.	Damping Resistor	Rise/Fall Time L=0, R=0 (ns) Max.	Multiple Servo Write	Head Induct. Range (µH)	Power Supply	Recommend New Design?
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	NO
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	NO
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	NO
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	NO
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	NO
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	NO
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.7 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.7 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.7 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.7 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.7 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	YES
1 - 40	4.5	OPTIONAL	6	NO	0.2 - 5	+5V	YES
5 - 35	4	OPTIONAL	6	YES	0.2 - 5	+5V	YES
5 - 35	4	OPTIONAL	6	YES	0.2 - 5	+5V	YES
5 - 35	4	OPTIONAL	6	YES	0.2 - 5	+5V	YES
5 - 35	4	YES	6	YES	0.7 - 5	+5V	YES
5 - 35	4	YES	6	YES	0.2 - 5	+5V	YES
5 - 35	4	YES	6	YES	0.2 - 5	+5V	YES
5 - 35	4	OPTIONAL	6	YES	0.2 - 5	+5V	YES
5 - 35	4	OPTIONAL	6	YES	0.2 - 5	+5V	YES
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
10 - 40	4	YES	8	NO	0.2 - 10	+5V	NO
5 - 20	5.7	OPTIONAL	4	YES	0.2 - 10	+5V	YES
5 - 20	5.7	OPTIONAL	4	YES	0.2 - 10	+5V	YES
5 - 20	5.7	OPTIONAL	4	YES	0.2 - 10	+5V	YES
5 - 35	7.8	YES	4	NO	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	NO	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	NO	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	NO	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	NO	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	YES	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	NO	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	YES	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	YES	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	YES	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	YES	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	YES	0.2 - 5	+5V	YES
5 - 35	7.8	YES	4	YES	0.2 - 5	+5V	YES

CHANNEL CIRCUITS SELECTOR GUIDE

Product	Current Revision	Pins	Package Type	Functional Description	Power Supply	Maximum Transfer Rate
VM53100QFL	Aug-94	64	PQFP	Data Separator Channel	±5V	105 Mbits/sec
VM5351PLL	Aug-94	44	PLCC	Data Separator	±5V	64 Mbits/sec
VM5352PLK	Aug-94	44	PLCC	Data Separator	±5V	64 Mbits/sec
VM5401PLL	Aug-94	44	PLCC	Pulse Detector/Qualifier	±5V or +5V, +12V	64 Mbits/sec
VM54100QFJ	Aug-94	44	PQFP	Peak Detection Read Channel	+5V	105 Mbits/sec
VM54750QFJ	Aug-94	52	PQFP	Pulse Detector/Servo Peak Detect	+5V	75 Mbits/sec
VM5603PLK	Aug-94	28	PLCC	(1,7) Encoder-Decoder	+5V	64 Mbits/sec
VM5621PLL	Aug-94	28	PLCC	(2,7) Encoder-Decoder	+5V	48 Mbits/sec
VM5622PLJ	Aug-94	28	PLCC	(2,7) Encoder-Decoder	±5V	48 Mbits/sec
VM5711POL	Aug-94	36	SOIC	Frequency Synthesizer	+5V	64 Mbits/sec
VM64110QHL	Aug-94	64	PQFP	Analog PRML Front End	+5V	110 Mbits/sec
VM8050PLL	Aug-94	28	PLCC	Digital Area Detector	+5V	N/A

TAPE DRIVE CIRCUITS SELECTOR GUIDE

Product	Current Revision	Pins	Package Type	Functional Description	Power Supply	Maximum Transfer Rate
VM5353PLL	Aug-94	44	PLCC	Data Separator	+5V, +12V	64 Mbits/sec
VM5353QFL	Aug-94	44	PQFP	Data Separator	+5V, +12V	64 Mbits/sec
VT520424FPOJ	Aug-94	20	SOIC	Inductively Coupled, Read/Write Preamplifier	+5V, +12V	N/A
VT520424POJ	Aug-94	20	SOIC	Inductively Coupled, Read/Write Preamplifier	+5V, +12V	N/A
VT520437POJ	Aug-94	20	SOIC	Inductively Coupled, Read/Write Preamplifier	+5V, +12V	N/A

Product Features
33 to 105 Mbits/sec Transfer Rate, (1,7) and (2,7) RLL Codes, ZDR Compatible, Marginalization
30 to 64 Mbits/sec Transfer Rate, (1,7) and (2,7) RLL Codes, ZDR Compatible, Marginalization
30 to 64 Mbits/sec Transfer Rate, (1,7) and (2,7) RLL Codes, ZDR Compatible, Marginalization
24 to 64 Mbits/sec Transfer Rate, Erase Feature, Qualifies based on Zero Crossing, Amplitude, Slope and Polarity
33 to 105 Mbits/sec Transfer Rate, Serial Interface for Programmability, Dual AGC, Dual Filter for Data and Servo Patterns
24 to 75 Mbits/sec Transfer Rate, Dual AGC Mode, Dual Filter for Data and Servo Patterns
10 to 64 Mbits/sec Transfer Rate, (1,7) Encoder-Decoder, ZDR Compatible, Write Precompensation
10 to 48 Mbits/sec Transfer Rate, (2,7) Encoder-Decoder, ZDR Compatible, Write Precompensation
10 to 48 Mbits/sec Transfer Rate, (2,7) Encoder-Decoder, ZDR Compatible, Write Precompensation
64 Mbits/sec Transfer Rate, VCO Frequency Range 40 to 200 MHz, ZDR Compatible
16 to 110 Mbits/sec Transfer Rate, (1,7) RLL, 120 M-Sample/sec Flash ADC, Write Precompensation, Quadrature Servo, Active Filter, ZDR
Analog to Digital Conversion of Servo Data for Digital Servo Applications

Product Features
30 to 64 Mbits/sec Transfer Rate, (1,7), (2,7) and (0,3) RLL Codes, ZDR Compatible, Marginalization
30 to 64 Mbits/sec Transfer Rate, (1,7), (2,7) and (0,3) RLL Codes, ZDR Compatible, Marginalization
High-Performance, Read/Write Preamplifier Designed for a Helical-Scan Head, Gain = 240, Without Flip-Flop
High-Performance, Read/Write Preamplifier Designed for a Helical-Scan Head, Gain = 240, With Flip-Flop
High-Performance, Read/Write Preamplifier Designed for a Helical-Scan Head, Gain = 375, With Flip-Flop

Sections

1 MR Preamplifiers

VTC Inc.
Value the Customer™

VM61006

6-CHANNEL, HIGH-PERFORMANCE, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

PRELIMINARY

August, 1994

FEATURES

- Read Gain = 350 V/V
- MR Bias Current Range = 8 - 20 mA
- Low Input Noise = 0.55 nV/√Hz Maximum
- Write Current Range = 10 - 30 mA
- Head Inductance Range = 100 - 700 nH
- Low Idle Power = 116 mW Maximum
- Rise Time = 5 ns Typical
- Power Supply Fault Protection
- +5V, -4.5V Power Supplies
- Write Unsafe Detection
- Head-to-Disk Contact Monitor
- Mask-Selectable Write Damping Resistor
- Reduced Mode and Head Selection Delays in FAST Mode
- Disk Voltage Monitor
- Differential PECL Write Data Inputs
- Current Sense Configuration

FUNCTIONAL DESCRIPTION

The VM61006 is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM6100 contains a thin-film head writer, an MR reader and associated fault circuitry to address up to six heads. It also provides bias current and control loops for setting the DC voltages on the MR element.

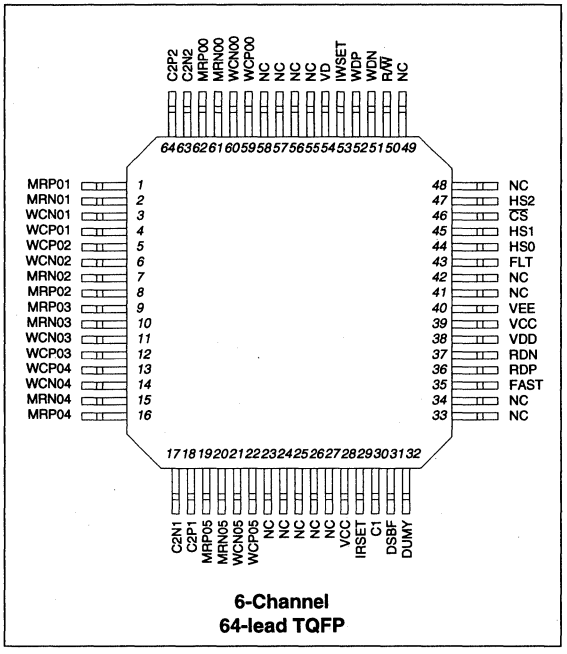
The VM61006 has two modes of operation. In read mode, the device operates as a low-noise differential preamplifier which senses resistance changes in the MR element that correspond to flux changes on the disk. The amplitude of the sense current is set either by an external resistor or by a current source and has a current gain of 20 mA/mA. In write mode, the circuit operates as a thin-film head write current switch, driving the thin-film write element of the MR head. The write current is externally programmed either by a resistor or an external current source and has a current gain of 20 mA/mA.

Fault protection is provided so during power sequencing, voltage faults or an invalid head select, the write current generator is disabled protecting the disk from potential transients. For added data protection, internal pull-up resistors are connected to the mode select lines, $\overline{CS}$ and R/$\overline{W}$, to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition.

The VM61006 operates from a +5V, -4.5V power supply. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters a sleep mode which reduces the power dissipation to only 116mW.

The VM61006 is available in a variety of package options, as well as die. Please consult VTC for details.

CONNECTION DIAGRAM



6-Channel
64-lead TQFP

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
- V_{DD} ..... -0.3V to + 7V
- V_{EE} ..... -7V to +0.3V

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{DD}+ 0.3V)

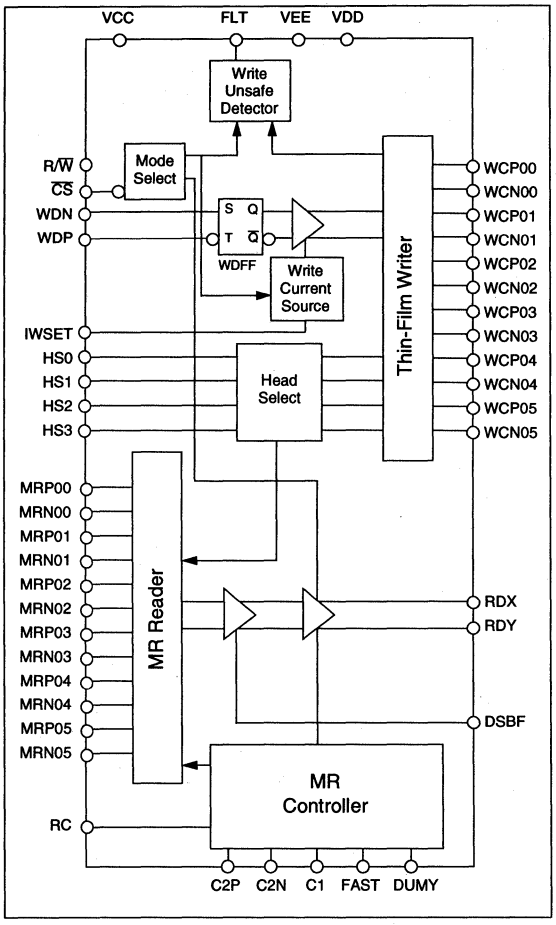
Storage Temperature T_{stg} .....-65° to 150°C
Junction Temperature T_J ..... 150°C
Thermal Impedance, Θ_{JA}: ..... 70°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{DD} .....+5V ± 10%
- V_{CC} ..... -4.5V ± 10%

Junction Temperature T_J ..... 0°C to 125°C

BLOCK DIAGRAM



CIRCUIT OPERATION

In all modes of operation, the VM61006 controls the common mode potential of all MR elements. This is necessary because the MR element cannot be insulated, so that a small voltage differential will cause arcing to the disk and damage the heads. Head voltages are held within ±250mV of the voltage on the VD pin, which monitors the disk potential of the drive. Thus, the disk may be grounded, as is done in disk drives having conventional thin film or ferrite recording heads, or isolated as the application may require.

In read mode, the VM61006 activates the MR bias current source, which then drives the selected MR element. The read bias current magnitude is determined by an external resistor connected between the IRSET pin and VCC. An internally-generated 2.5 volt reference is present at the IRSET pin. The magnitude of the MR bias current is:

$$I_{MR} = 50/R_{RSET} \qquad \textit{(eq. 1)}$$

where R_{RSET} is the resistor connected at IRSET.

The fault output pin, FLT, is high to indicate a non-fault condition. If the voltage drops below a certain threshold on either supply, FLT will be pulled low to indicate a fault. Also, if a head-to-disk contact occurs, the thermal asperity in the MR element will result in an abnormally high readback signal, which is monitored by detection circuitry and will be also flagged by a low FLT output.

The read preamplifier is activated and connected to the selected head. The write current source and write unsafe detection circuitry is deactivated. RDP and RDN outputs are emitter follower and are in phase with the MRP and MRN head ports. These outputs should be AC-coupled to the load. The output common mode voltage is maintained in the write mode, thereby substantially reducing the write-to-read recovery delay in the subsequent pulse detection circuitry.

In write mode, the preamplifier is shut off and the VM6100 is converted to a current switch. However, MR bias current is maintained in order to minimize the write-to-read delay. The write current source is activated and drives the thin film element of the selected head. The polarity of the current is initially into the WCN port following a read-to-write transition. Write current polarity is reversed on low-to-high transitions of the write data input (WDP low-to-high). Circuitry is activated to detect various fault conditions. If any of the faults occur, they will be flagged as a high voltage output on the FLT pin. In addition, if a VDD fault occurs, the write current source is deactivated in order to protect recorded data.

The write current magnitude is determined by an external resistor connected between the IWSET pin and VCC. An internally-generated 2.5 volt reference is present at the IWSET pin. The magnitude of the write current (0-peak) is:

$$I_W = 50/\left[R_W \times \left(1 + \frac{R_H}{R_D}\right)\right] \qquad \textit{(eq. 2)}$$

where R_W is the resistor connected at IWSET, R_H is the series resistance of the head, and R_D is an internal damping resistor of 360Ω.

Power supply fault protection provides data security by disabling the write current generator during a VDD fault or power-up/down. The writer is independent of VEE, so VEE faults do not affect it. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin FLT. Two positive transitions of write data may be required to clear the fault after the safe condition is restored.

- No write current
- Open write head
- Write Data frequency too low
- Device in read or idle mode
- Head shorted to ground

Fast mode is utilized during head-to-head and idle-to-read transitions. When the FAST mode pin is high, the unity-gain frequency of the offset control loop is increased such that it is inside the passband of the reader, allowing the delay to be reduced to less than 5µs. This pin must be brought low before read data is valid.

A DUMY mode pin allows the selection of a dummy head in read or write mode. MR bias current is routed to an internal resistor, and the write current source is deactivated. This mode

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is optionally used during power-up/down and following head-to-disk contacts. When the DUMY pin is high, the write current source is disabled to protect recorded data. An internal pull-up resistor is provided in event of an accidental open. If this pin is not used it should be grounded for normal operation.

In idle mode, the MR bias and write current sources are deactivated, and the device enters a low-power mode in which power dissipation is less than 116mW. Write and read fault detection circuitry is disabled. MR common mode and offset control loops still receive power in order to reduce idle-to-read mode recovery.

Mode control and head selection are accomplished via $\overline{CS}$, R/$\overline{W}$, and HS0-2 pins. Internal pull-up resistors are provided on $\overline{CS}$ and R/$\overline{W}$ pins to force the device into a non-writing condition if either control line is opened accidentally. In addition, invalid head select codes disable the writer and select head MR00. Truth tables for mode and head selection are shown in Table 1 and Table 2, respectively.

Table 1: Mode Select Logic

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select Logic

HS2	*HS1*	*HS0*	*DUMY*	*HEAD*
X	X	X	1	DUMY
0	0	0	0	00
0	0	1	0	01
0	1	0	0	02
0	1	1	0	03
1	0	0	0	04
1	0	1	0	05
1	1	X	0	DUMY

PIN_FUNCTION LIST AND DESCRIPTION

1)	$\overline{CS}$	(I)	Chip select: a low level enables the device.
2)	R/$\overline{W}$	(I*)	Read/Write: a high level enables read mode.
3)	HS0-HS2	(I*)	Head Select: selects one of the twelve heads.
4)	DUMY	(I*)	A high level enables the dumy mode.
5)	FAST	(I*)	A high level enables fast settling of the reader.
6)	FLT	(O*)	Write/Read Fault: A high level indicates a fault in write mode. A low level indicates a fault in read mode.
7)	WDP, WDN	(I*)	Differential Pseudo-ECL write data in: a positive edge on WDP toggles the direction of the head current.
8)	MRP00-MRP05	(I)	MR head connections, positive end.
9)	MRN00-MRN05	(I)	MR head connections, negative end.
10)	WCP00-WCP05	(O)	Write head connections, positive end.
11)	WCN00-WCN05	(O)	Write head connections, negative end.
12)	RDP, RDN	(O*)	Read Data: Differential read signal outputs.
13)	IWSET	(*)	Write current pin: used to set the magnitude of write current.
14)	IRSET	(*)	MR bias reference pin: used to set the magnitude of MR bias current.
15)	C2P,C2N	(*)	Compensation capacitor pins for the MR head current loop.
16)	C1	(*)	Noise bypass for the MR bias current generator. The other end of cap connected to VEE.
17)	VD	(I*)	Analog reference for the disk bias.
18)	DSBF	(*)	Disables disk contact detector if tied to VCC. To enable, leave open.
19)	VEE	-	-4.5V supply
20)	VDD	-	+5V supply
21)	VCC	-	Ground

* When more than one device is used, these signals can be wire OR'ed together

I = Input pin

O = Output pin

STATIC (DC) CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, 0°C < T_A < 80°C, 4.5V < V_{DD} < 5.5V, -5.0V < V_{EE} < -4.0V.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{DD} Power Supply Current	I_{DD}	Read Mode, I_{MR} = 16mA			95	mA
		Write Mode, I_W = 20mA, I_{MR} = 16mA			140	mA
		Idle Mode			12	mA
V_{EE} Power Supply Current	I_{EE}	Read Mode, I_{MR} = 16mA			70	mA
		Write Mode, I_W = 20mA, I_{MR} = 16mA			65	mA
		Idle Mode			10	mA
Power Supply Dissipation	P_d	Read Mode, I_{MR} = 16mA			873	mW
		Write Mode, I_W = 20mA, I_{MR} = 16mA			1095	mW
		Idle Mode			116	mW
Input High Voltage	V_{IH}	PECL	V_{DD} - 1.0		V_{DD} - 0.7	V
		CMOS	3.5			V
Input Low Voltage	V_{IL}	PECL	V_{DD} - 1.9		V_{DD} - 1.6	V
		CMOS			1.65	V
Disk Reference Voltage Range	V_D		-250		250	mV
Input High Current	I_{IH}	PECL			120	µA
		CMOS	-160		160	µA
Input Low Current	I_{IL}	PECL			120	µA
		CMOS	-160		160	µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{DD} Fault Threshold	V_{DTH}		3.75		4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.75		-3.25	V

DYNAMIC (AC) CHARACTERISTICS

READ MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0V < V_{EE} < -4.0$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		8		20	mA
MR Head Current Tolerance	I_{MR}	$8 < I_{MR} < 18$ mA	-5		+5	%
MR Bias Reference Voltage	V_{RSET}	$2775 < R_{RSET} < 6250\ \Omega$		2.5		V
IRSET to MR Bias Current Gain	A_{IMR}	$2775 < R_{RSET} < 6250\ \Omega$		20		mA/mA
Differential Voltage Gain	A_V	$V_{IN} = 1mV_{pp}$ @10MHz, R_L (RDP, RDN) = 1kΩ, I_{MR} = 16mA, $R_{MR} = 12\Omega$	300	350	400	V/V
Passband Upper Frequency Limit	f_{HR}	$R_{MR} = 13\Omega$; L_{MR} = 20nH; -1dB		40		MHz
		-3dB	60			
Passband Lower -3dB Frequency Limit	f_{LR}	$R_{MR} = 12\Omega$; L_{MR} = 20nH	0.1		0.5	MHz
Equivalent Input Noise	e_n	$R_{MR} = 13\Omega$; I_{MR} = 16mA; 1 < f < 20 MHz			0.55	nV/√Hz
Differential Input Capacitance	C_{IN}	$R_{MR} = 12\Omega$; I_{MR} = 16mA			10	pF
Differential Input Resistance	R_{IN}	I_{MR} = 16mA			4	Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at $V_{IN} = 1mV_{pp}$ @ f = 10 MHz	4			mV_{pp}
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, I_{MR} = 16mA, $R_{MR} = 12\Omega$, 1 < f < 50 MHz	30			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz, on V_{DD} or V_{EE}, I_{MR} = 16mA, $R_{MR} = 12\Omega$, 1 < f < 50 MHz	30			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mVp-p @ 5MHz, 1 < f < 50 MHz	30			dB
Output Offset Voltage	V_{OS}	I_{MR} = 16mA, $R_{MR} = 12\Omega$			100	mV
Common Mode Output Voltage	V_{OCM}		V_{DD} - 2.8	V_{DD} -2.5	V_{DD}-2.2	V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			250	mV
Single-Ended Output Resistance	R_{SEO}				35	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	±1.5			mA
Total Harmonic Distortion	THD	$V_{in} = 4mV_{pp}$; ten harmonics			0.5	%
MR Head-to-Disk Contact Current	I_{DISK}	Extended contact, R_{DISK} = 10MΩ			100	µA
		Maximum peak discharge, C_{DISK} = 300pF, R_{DISK} = 10MΩ			20	mA
MR Head Potential	V_{MR}	I_{MR} = 16mA, $R_{MR} = 12\Omega$	-300		300	mV

WRITE MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.
$0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0 < V_{EE} < -4.0$, $I_W = 20mA$, $L_H = 500nH$, $R_H = 30\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
I_{WSET} Pin Voltage	V_{WSET}			2.5		V
I_{WSET} to Write Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = V_{WSET} * A_I$	46	50	54	V
Write Current Range	I_W		10		30	mA
Write Current Tolerance	ΔI_W	$6 < I_W < 30$ mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open head	4.5	6.5		V_{pp}
Unselected Head Transition Current	I_{UH}	$I_W = 30mA$			50	μA_{pk}
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	Internal damping resistance	290	360	430	Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT = Low	1.0			MHz

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0 < V_{EE} < -4.0$, $I_W = 20mA$, $L_H = 500nH$, $R_H = 30\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			0.5	µs
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope			0.5	µs
$\overline{CS}$ to Read Mode	t_{CS}	To 90% of envelope; FAST = low			50	µs
		† Fast = high for 3.5µs			5	µs
$\overline{CS}$ to Write Mode	t_{CS}	To 90% of write current			0.5	µs
HS0 - HS3 to Any Head	t_{HS}	To 90% of envelope; FAST = low			50	µs
		† FAST = high for 3.5µs			5	µs
DUMY Mode to Any Head	t_{DH}	To 90% of envelope; FAST = low			50	µs
		† FAST = high for 3.5µs			5	µs
$\overline{CS}$ to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe*	t_{D1}	50% WDP to 50% FLT	0.6		3.6	µs
Unsafe to Safe*	t_{D2}	50% WDP to 50% FLT			1	µs
Head Current Propagation Delay*	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, $L_H = 0$, $R_H = 0$			0.2	ns
Rise/Fall Time	t_r / t_f	20-80%; $I_W = 20mA$; $L_H = 550nH$, $R_H = 40\Omega$			6	ns
		$L_H = 0$, $R_H = 0$; $I_W = 20mA$			3	ns
Settling Time	T_{WSET}	$I_{WC} = 20mA$, $L_H = 550nH$, $R_H = 40\Omega$; to ±10%			15	ns
Overshoot	W_{COV}	$I_{WC} = 20mA$; $L_H = 550nH$, $R_H = 40\Omega$		25		%

*See Figure 1 for write mode timing diagram.
† See Figure 2 for read mode timing diagram.

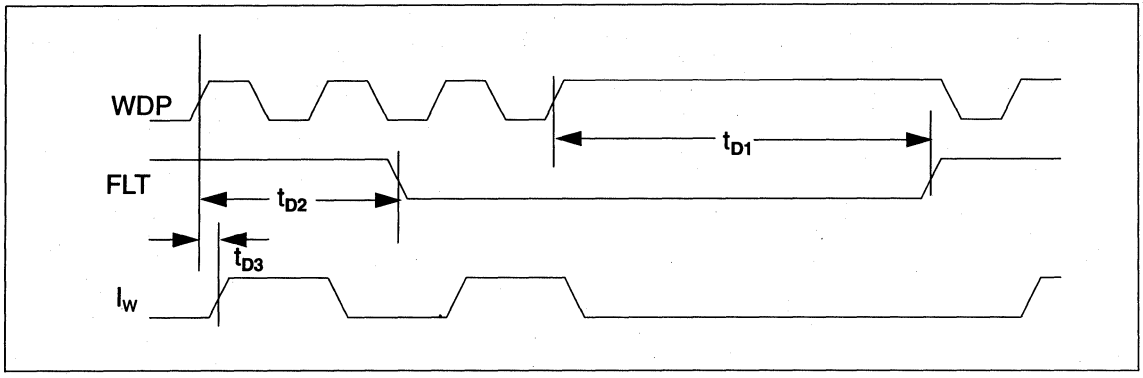


Figure 1: Write Mode Timing Diagram

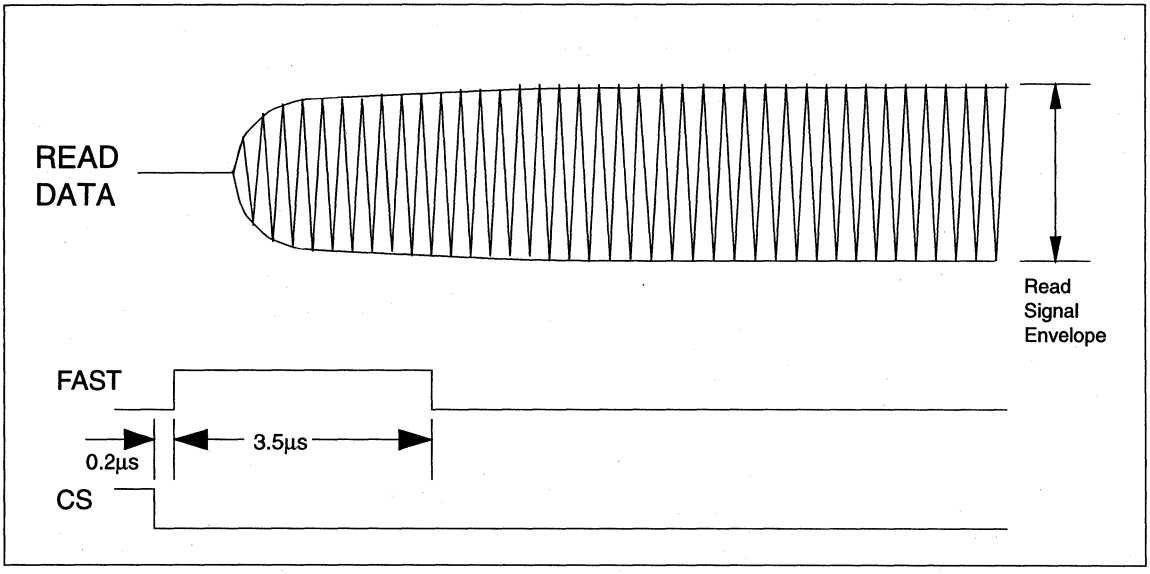
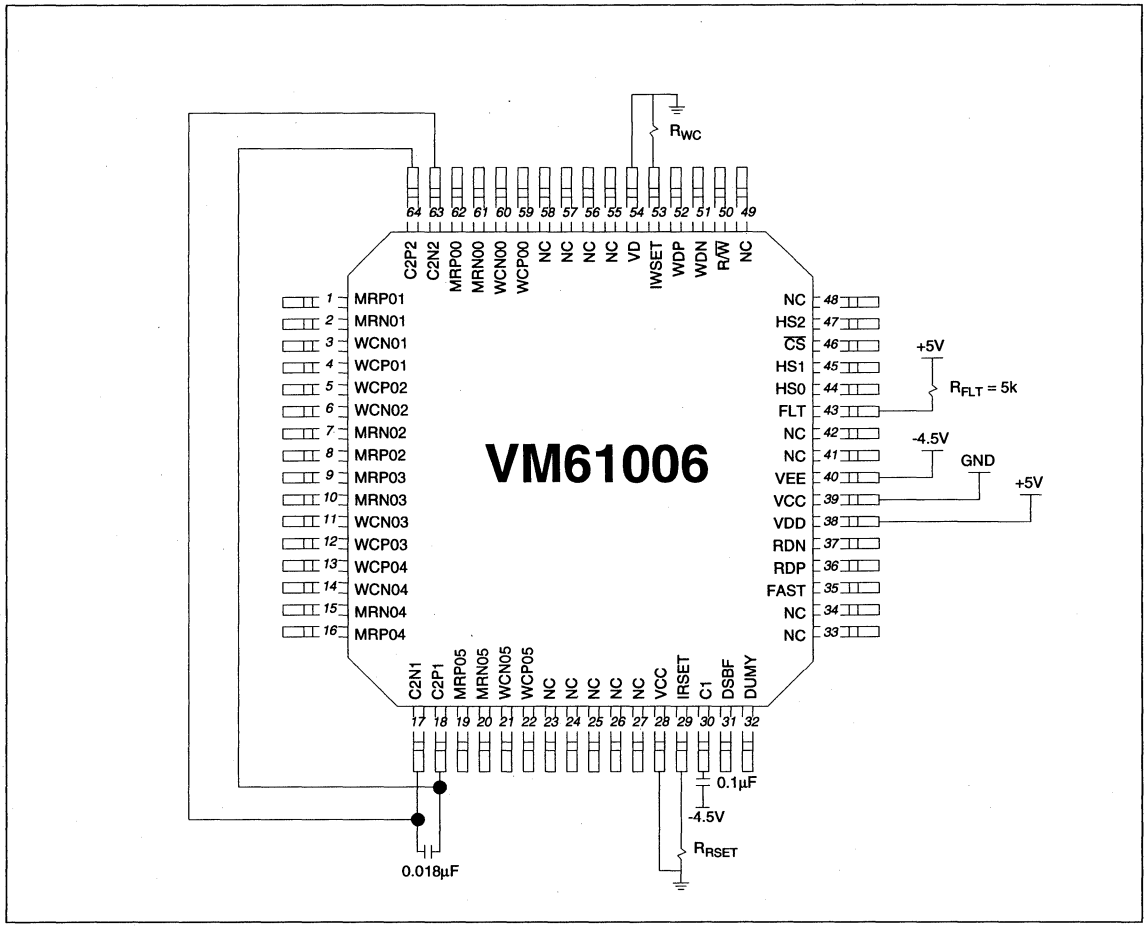


Figure 2: Read Mode Timing Diagram. Also applies to DUMY and HS0 - HS3.

TYPICAL CONNECTION DIAGRAM



Note 1: IRSET = MR Bias Current = $50/R_{RSET}$
Note 2: I_{WSET} = Write Current = $50/R_{WC}(1+R_H/360)$, R_H = Head Series Resistance
Note 3: V_{DD} = +5V, V_{CC} = GND, V_{EE} = -4.5V

VTC Inc.
Value the Customer™

VM61012

12-CHANNEL, HIGH-PERFORMANCE, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

PRELIMINARY

August,1994

FEATURES

- Read Gain = 500 V/V
- MR Bias Current Range = 8 - 18 mA
- Low Input Noise = 0.55 nV/$\sqrt{Hz}$ Maximum
- Write Current Range = 10 - 30 mA
- Head Inductance Range = 100 - 700 nH
- Low Idle Power = 116 mW Maximum
- Rise Time = 5 ns Typical
- Power Supply Fault Protection
- +5V, -4.5V Power Supplies
- Write Unsafe Detection
- Head-to-Disk Contact Monitor
- Mask-Selectable Write Damping Resistor
- Reduced Mode and Head Selection Delays in FAST Mode
- Disk Voltage Monitor
- Differential PECL Write Data Inputs
- Current Sense Configuration

FUNCTIONAL DESCRIPTION

The VM61012 is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM61012 contains a thin-film head writer, an MR reader and associated fault circuitry to address up to 12 heads. It also provides bias current and control loops for setting the DC voltages on the MR element.

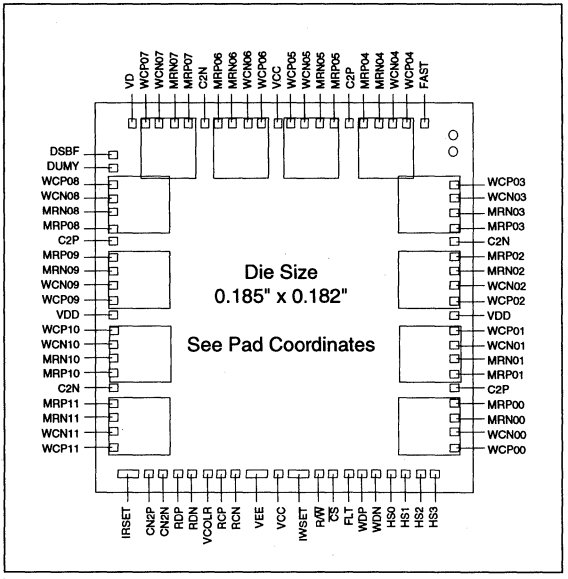
The VM61012 has two modes of operation. In read mode, the device operates as a low-noise differential preamplifier which senses resistance changes in the MR element that correspond to flux changes on the disk. The amplitude of the sense current is set either by an external resistor or by a current source and has a current gain of 20 mA/mA. In write mode, the circuit operates as a thin-film head write current switch, driving the thin-film write element of the MR head. The write current is externally programmed either by a resistor or an external current source and has a current gain of 20 mA/mA.

Fault protection is provided so during power sequencing, voltage faults or an invalid head select, the write current generator is disabled protecting the disk from potential transients. For added data protection, internal pull-up resistors are connected to the mode select lines, $\overline{CS}$ and R/$\overline{W}$, to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition.

The VM61012 operates from a +5V, -4.5V power supply. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters a sleep mode which reduces the power dissipation to only 116mW.

The VM61012 is available in die form for chip-on-flex applications or in several package configurations. Please consult VTC for details.

DIE PAD DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
- V_{DD} ..... -0.3V to + 7V
- V_{EE} ..... -7V to +0.3V

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{DD} + 0.3V)

Storage Temperature T_{stg} .....-65° to 150°C

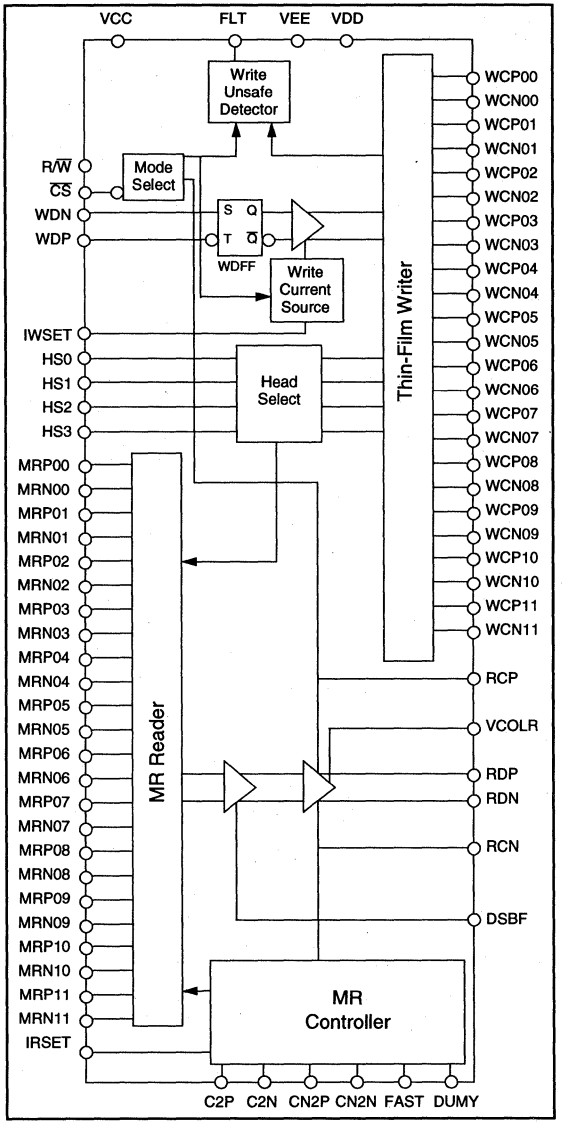
Junction Temperature T_J ..... 150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{DD} .....+5V ± 10%
- V_{EE} ..... -4.5V ± 10%

Junction Temperature T_J ..... 0°C to 125°C

BLOCK DIAGRAM



CIRCUIT OPERATION

In all modes of operation, the VM61012 controls the common mode potential of all MR elements. This is necessary because the MR element cannot be insulated, so that a small voltage differential will cause arcing to the disk and damage the heads. Head voltages are held within ±250mV of the voltage on the VD pin, which monitors the disk potential of the drive. Thus, the disk may be grounded, as is done in disk drives having conventional thin film or ferrite recording heads, or isolated as the application may require.

In read mode, the VM61012 activates the MR bias current source, which then drives the selected MR element. The read bias current magnitude is determined by an external resistor connected between the IRSET pin and VCC. An internally-generated 2.5 volt reference is present at the IRSET pin. The magnitude of the MR bias current is:

$$I_{MR} = 50/R_{RSET} \qquad \textit{(eq. 1)}$$

where R_{RSET} is the resistor connected at IRSET.

The fault output pin, FLT, is high to indicate a non-fault condition. If the voltage drops below a certain threshold on either supply, FLT will be pulled low to indicate a fault. Also, if a head-to-disk contact occurs, the thermal asperity in the MR element will result in an abnormally high readback signal, which is monitored by detection circuitry and will be also flagged by a low FLT output.

The read preamplifier is activated and connected to the selected head. The write current source and write unsafe detection circuitry is deactivated. RDP and RDN outputs are emitter follower and are in phase with the MRP and MRN head ports. These outputs should be AC-coupled to the load. The output common mode voltage is maintained in the write mode, thereby substantially reducing the write-to-read recovery delay in the subsequent pulse detection circuitry.

Internal second stage resistors may be optionally removed at wafer test, allowing external resistors to be used in the application. The internal resistors are removed by blowing a pair of fuse links, and the discrete resistors are then connected from open collector output RCP to VCOLR, and from RCN to VCOLR. This provision allows tighter tolerance of read gain because of better tolerances available on discrete resistors. It also allows the user to choose the gain required for the application. The output can be taken at the emitter follower pair RDP-RDN, or at the open collector pair RCP-RCN if preferred.

In write mode, the preamplifier is shut off and the VM61012 is converted to a current switch. However, MR bias current is maintained in order to minimize the write-to-read delay. The write current source is activated and drives the thin film element of the selected head. The polarity of the current is initially into the WCN port following a read-to-write transition. Write current polarity is reversed on low-to-high transitions of the write data input (WDP low-to-high). Circuitry is activated to detect various fault conditions. If any of the faults occur, they will be flagged as a high voltage output on the FLT pin. In addition, if a VDD fault occurs, the write current source is deactivated in order to protect recorded data.

The write current magnitude is determined by an external resistor connected between the IWSET pin and VCC. An internally-generated 2.5 volt reference is present at the IWSET pin. The magnitude of the write current (0-peak) is:

$$I_W = 50/\left[R_W \times \left(1 + \frac{R_H}{R_D}\right)\right] \qquad \textit{(eq. 2)}$$

where R_W is the resistor connected at IWSET, R_H is the series resistance of the head, and R_D is an internal damping resistor of 360Ω.

Power supply fault protection provides data security by disabling the write current generator during a VDD fault or power-up/down. The writer is independent of VEE, so VEE faults do not affect it. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin

FLT. Two positive transitions of write data may be required to clear the fault after the safe condition is restored.

- No write current
- Open write head
- Write Data frequency too low
- Device in read or idle mode
- Head shorted to ground

Fast mode is utilized during head-to-head and idle-to-read transitions. When the FAST mode pin is high, the unity-gain frequency of the offset control loop is increased such that it is inside the passband of the reader, allowing the delay to be reduced to less than 5µs. This pin must be brought low before read data is valid.

A DUMY mode pin allows the selection of a dummy head in read or write mode. MR bias current is routed to an internal resistor, and the write current source is deactivated. This mode is optionally used during power-up/down and following head-to-disk contacts. When the DUMY pin is high, the write current source is disabled to protect recorded data. An internal pull-up resistor is provided in event of an accidental open. If this pin is not used it should be grounded for normal operation.

In idle mode, the MR bias and write current sources are deactivated, and the device enters a low-power mode in which power dissipation is less than 116mW. Write and read fault detection circuitry is disabled. MR common mode and offset control loops still receive power in order to reduce idle-to-read mode recovery.

Mode control and head selection are accomplished via $\overline{CS}$, R/$\overline{W}$, and HS0-3 pins. Internal pull-up resistors are provided on $\overline{CS}$ and R/$\overline{W}$ pins to force the device into a non-writing condition if either control line is opened accidentally. In addition, invalid head select codes disable the writer and select head MR00. Truth tables for mode and head selection are shown in Table 1 and Table 2, respectively.

Table 1: Mode Select Logic

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select Logic

HS3	*HS2*	*HS1*	*HS0*	*DUMY*	*HEAD*
X	X	X	X	1	DUMY
0	0	0	0	0	00
0	0	0	1	0	01
0	0	1	0	0	02
0	0	1	1	0	03
0	1	0	0	0	04
0	1	0	1	0	05
0	1	1	0	0	06
0	1	1	1	0	07
1	0	0	0	0	08
1	0	0	1	0	09
1	0	1	0	0	10
1	0	1	1	0	11
1	1	X	X	0	00

PIN_FUNCTION LIST AND DESCRIPTION

1)	$\overline{CS}$	(I)	Chip select: a low level enables the device.
2)	R/$\overline{W}$	(I*)	Read/Write: a high level enables read mode.
3)	HS0-HS3	(I*)	Head Select: selects one of the twelve heads.
4)	DUMY	(I*)	A high level enables the dumy mode.
5)	FAST	(I*)	A high level enables fast settling of the reader.
6)	FLT	(O*)	Write/Read Fault: A high level indicates a fault in write mode. A low level indicates a fault in read mode.
7)	WDP, WDN	(I*)	Differential Pseudo-ECL write data in: a positive edge on WDP toggles the direction of the head current.
8)	MRP00-MRP11	(I)	MR head connections, positive end.
9)	MRN00-MRN11	(I)	MR head connections, negative end.
10)	WCP00-WCP11	(O)	Write head connections, positive end.
11)	WCN00-WCN11	(O)	Write head connections, negative end.
12)	RDP, RDN	(O*)	Read Data: Differential read signal outputs.
13)	IWSET	(*)	Write current pin: used to set the magnitude of write current.
14)	IRSET	(*)	MR bias reference pin: used to set the magnitude of MR bias current.
15)	C2P,C2N	(*)	Compensation capacitor for the MR head current loop.
16)	CN2P, CN2N	(*)	Noise bypass for the MR bias current generator.
17)	VD	(I*)	Analog reference for the disk bias.
18)	DSBF	(*)	Disables disk contact detector if tied to VCC.
19)	RCP, RCN	(*)	Differential output for connection of external gain-setting resistors.
20)	VCOLR	(*)	Common mode output for connection of external resistors RCP, RCN.
21)	VEE	-	-4.5V supply
22)	VDD	-	+5V supply
23)	VCC	-	Ground

* When more than one device is used, these signals can be wire OR'ed together

I = Input pin

O = Output pin

STATIC (DC) CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, 0°C < T_A < 80°C, 4.5V < V_{DD} < 5.5V, -5.0V < V_{EE} < -4.0V.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{DD} Power Supply Current	I_{DD}	Read Mode, I_{MR} = 16mA			95	mA
		Write Mode, I_W = 20mA, I_{MR} = 16mA			140	mA
		Idle Mode			12	mA
V_{EE} Power Supply Current	I_{EE}	Read Mode, I_{MR} = 16mA			70	mA
		Write Mode, I_W = 20mA, I_{MR} = 16mA			65	mA
		Idle Mode			10	mA
Power Supply Dissipation	P_d	Read Mode, I_{MR} = 16mA			873	mW
		Write Mode, I_W = 20mA, I_{MR} = 16mA			1095	mW
		Idle Mode			116	mW
Input High Voltage	V_{IH}	PECL	V_{DD} - 1.0		V_{DD} - 0.7	V
		CMOS	3.5			V
Input Low Voltage	V_{IL}	PECL	V_{DD} - 1.9		V_{DD} - 1.6	V
		CMOS			1.65	V
Disk Reference Voltage Range	V_D		-250		250	mV
Input High Current	I_{IH}	PECL			120	µA
		CMOS	-160		160	µA
Input Low Current	I_{IL}	PECL			120	µA
		CMOS	-160		160	µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{DD} Fault Threshold	V_{DTH}		3.75		4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.75		-3.25	V

DYNAMIC (AC) CHARACTERISTICS

READ MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0V < V_{EE} < -4.0$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		8		18	mA
MR Head Current Tolerance	I_{MR}	$8 < I_{MR} < 18$ mA	-5		+5	%
MR Bias Reference Voltage	V_{RSET}	$2775 < R_{RSET} < 6250\Omega$		2.5		V
IRSET to MR Bias Current Gain	A_{IMR}	$2775 < R_{RSET} < 6250\Omega$		20		mA/mA
Differential Voltage Gain	A_V	$V_{IN} = 1mV_{pp}$ @10MHz, R_L (RDP, RDN) = 1kW, $I_{MR} = 16mA$, $R_{MR} = 12\Omega$	400	500	600	V/V
Passband Upper Frequency Limit	f_{HR}	-1dB: $R_{MR} = 13\Omega$; $L_{MR} = 20nH$		40		MHz
		-3dB	60			
Passband Lower -3dB Frequency Limit	f_{LR}	$R_{MR} = 12\Omega$; $L_{MR} = 20nH$	0.1		0.5	MHz
Equivalent Input Noise	e_n	$R_{MR} = 13\Omega$; $I_{MR} = 16mA$; $1 < f < 20$ MHz			0.55	nV/√Hz
Differential Input Capacitance	C_{IN}	$R_{MR} = 12\Omega$; $I_{MR} = 16mA$			10	pF
Differential Input Resistance	R_{IN}	$I_{MR} = 16mA$			4	Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at $V_{IN} = 1mV_{pp}$ @ f = 10 MHz	4			mV_{pp}
Common Mode Rejection Ratio	CMRR	$V_{CM} = 100mVpp$, $I_{MR} = 16mA$, $R_{MR} = 12\Omega$, $1 < f < 50$ MHz	30			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz, on V_{DD} or V_{EE}, $I_{MR} = 16mA$, $R_{MR} = 12\Omega$, $1 < f < 50$ MHz	30			dB
Channel Separation	CS	Unselected Channels: $V_{IN} = 100mVp-p$ @ 5MHz, $1 < f < 50$ MHz	30			dB
Output Offset Voltage	V_{OS}	$I_{MR} = 16mA$, $R_{MR} = 12\Omega$			100	mV
Common Mode Output Voltage	V_{OCM}		V_{DD} - 2.8	V_{DD} -2.5	V_{DD}-2.2	V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			250	mV
Single-Ended Output Resistance	R_{SEO}				35	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	±1.5			mA
Total Harmonic Distortion	THD	$V_{in} = 4mV_{pp}$; ten harmonics			0.5	%
MR Head-to-Disk Contact Current	I_{DISK}	Extended contact, $R_{DISK} = 10M\Omega$			100	µA
		Maximum peak discharge, $C_{DISK} = 300pF$, $R_{DISK} = 10M\Omega$			20	mA
MR Head Potential	V_{MR}	$I_{MR} = 16mA$, $R_{MR} = 12\Omega$	-300		300	mV

WRITE MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.
$0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0 < V_{EE} < -4.0$, $I_W = 20mA$, $L_H = 500nH$, $R_H = 30\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
I_{WSET} Pin Voltage	V_{WSET}			2.5		V
I_{WSET} to Write Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = V_{WSET} * A_I$	46	50	54	V
Write Current Range	I_W		10		30	mA
Write Current Tolerance	ΔI_W	$6 < I_W < 30$ mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open head	4.5	6.5		V_{pp}
Unselected Head Transition Current	I_{UH}	$I_W = 30mA$			50	μA_{pk}
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	Internal damping resistance	290	360	430	Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT = Low	1.0			MHz

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0 < V_{EE} < -4.0$, $I_W = 20mA$, $L_H = 500nH$, $R_H = 30\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			0.5	µs
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope			0.5	µs
CS to Read Mode	t_{CS}	To 90% of envelope; FAST = low			50	µs
		† Fast = high for 3.5µs			5	µs
$\overline{CS}$ to Write Mode	t_{cs}	To 90% of write current			0.5	µs
HS0 - HS3 to Any Head	t_{HS}	To 90% of envelope; FAST = low			50	µs
		† FAST = high for 3.5µs			5	µs
DUMY Mode to Any Head	t_{DH}	To 90% of envelope; FAST = low			50	µs
		† FAST = high for 3.5µs			5	µs
$\overline{CS}$ to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe*	t_{D1}	50% WDP to 50% FLT	0.6		3.6	µs
Unsafe to Safe*	t_{D2}	50% WDP to 50% FLT			1	µs
Head Current Propagation Delay*	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, $L_H = 0$, $R_H = 0$			1.0	ns
Rise/Fall Time	t_r / t_f	20-80%; $I_W = 20mA$; $L_H = 550nH$, $R_H = 40\Omega$			6	ns
		$L_H = 0$, $R_H = 0$; $I_W = 20mA$			3	ns
Settling Time	T_{WSET}	$I_{WC} = 20mA$, $L_H = 550nH$, $R_H = 40\Omega$; to ±10%			15	ns
Overshoot	W_{COV}	$I_{WC} = 20mA$; $L_H = 550nH$, $R_H = 40\Omega$		25		%

*See Figure 1 for write mode timing diagram.
† See Figure 2 for read mode timing diagram.

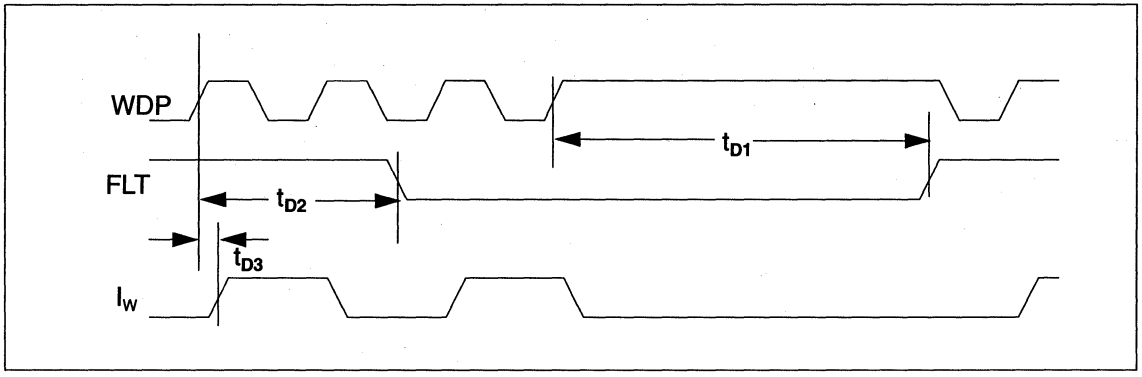


Figure 1: Write Mode Timing Diagram

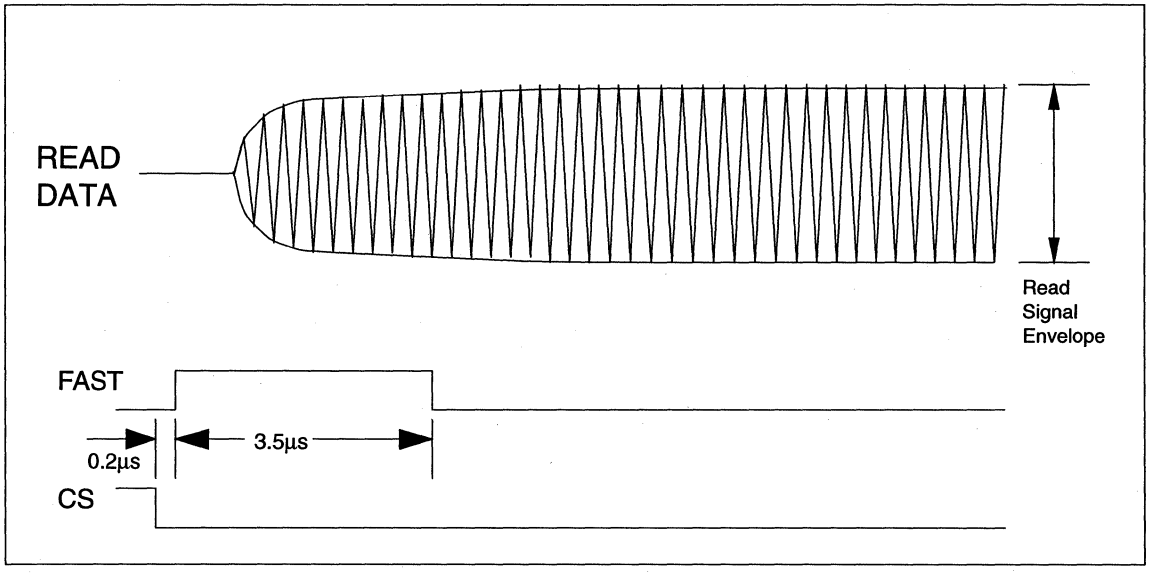
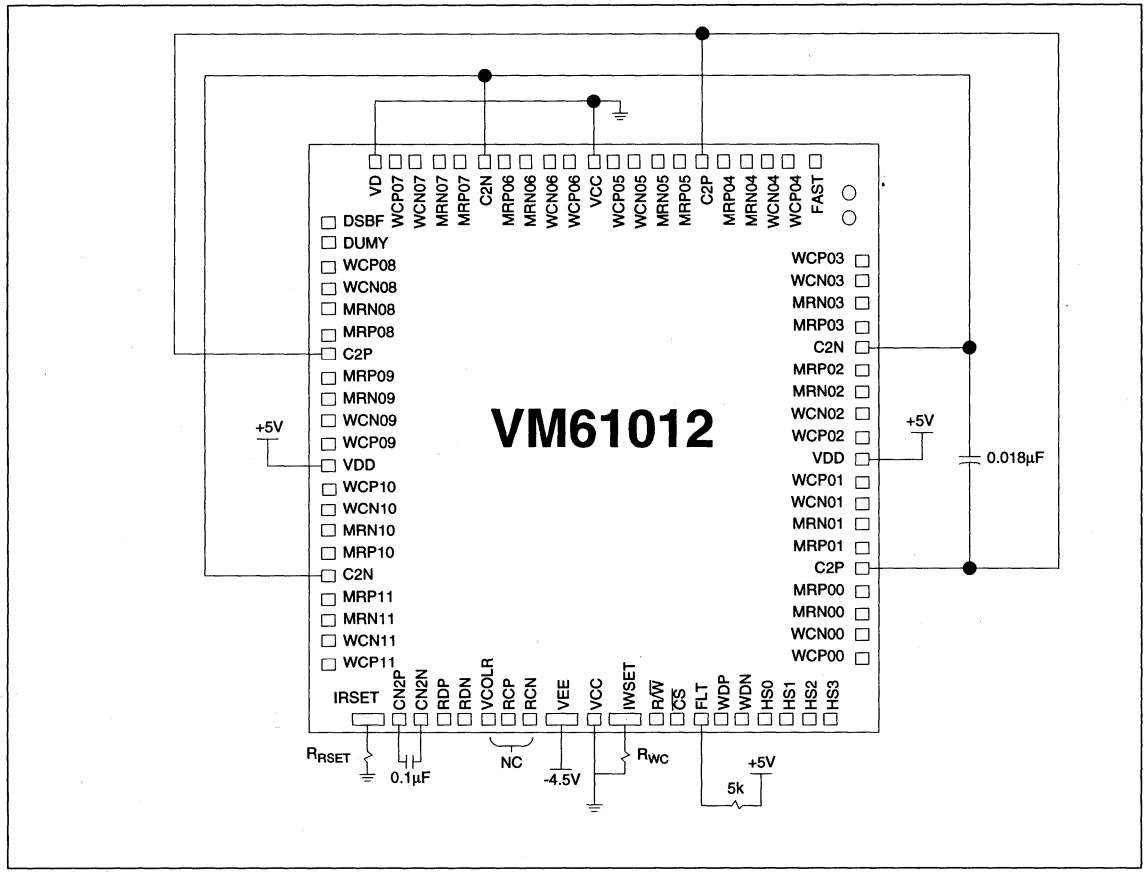


Figure 2: Read Mode Timing Diagram. Also applies to DUMY and HS0 - HS3.

TYPICAL CONNECTION DIAGRAM



Note 1: IRSET = MR Bias Current = $50/R_{RSET}$

Note 2: I_{WSET} = Write Current = $50/R_{WC}(1+R_H/360)$, R_H = Head Series Resistance

Note 3: V_{DD} = +5V, V_{CC} = GND, V_{EE} = -4.5V

VM61012 PAD COORDINATES

PIN NAME	X AXIS	Y AXIS
WCP11	-2063.25	-1809.00
WCN11	-2063.25	-1629.00
MRN11	-2063.25	-1449.00
MRP11	-2063.25	-1269.00
C2N	-2063.25	-1089.00
MRP10	-2063.25	-909.00
MRN10	-2063.25	-729.00
WCN10	-2063.25	-549.00
WCP10	-2063.25	-369.00
VDD:P	-2063.25	-189.00
WCP09	-2063.25	-9.00
WCN09	-2063.25	171.00
MRN09	-2063.25	351.00
MRP09	-2063.25	531.00
C2P	-2063.25	711.00
MRP08	-2063.25	891.00
MRN08	-2063.25	1071.00
WCN08	-2063.25	1251.00
WCP08	-2063.25	1431.00
DUMMY	-2063.25	1618.00
DSBF	-2063.25	1814.75
VD	-1820.00	2172.00
WCP07	-1620.00	2172.00
WCN07	-1440.00	2172.00
MRN07	-1260.00	2172.00
MRP07	-1080.00	2172.00
C2N	-900.00	2172.00
MRP06	-720.00	2172.00
MRN06	-540.00	2172.00
WCN06	-360.00	2172.00
WCP06	-180.00	2172.00
VDD	0.00	2172.00
WCP05	180.00	2172.00
WCN05	360.00	2172.00
MRN05	540.00	2172.00
MRP05	720.00	2172.00
C2P	900.00	2172.00
MRP04	1080.00	2172.00
MRN04	1260.00	2172.00
WCN04	1440.00	2172.00
WCP04	1620.00	2172.00
FAST	1860.00	2172.00
WCP03	2063.25	1431.00
WCN03	2063.25	1251.00
MRN03	2063.25	1071.00
MRP03	2063.25	891.00
C2N	2063.25	711.00
MRP02	2063.25	531.00
MRN02	2063.25	351.00
WCN02	2063.25	171.00
WCP02	2063.25	-9.00
VDD	2063.25	-189.00
WCP01	2063.25	-369.00
WCN01	2063.25	-549.00
MRN01	2063.25	-729.00
MRP01	2063.25	-909.00
C2P	2063.25	-1089.00
MRP00	2063.25	-1269.00
MRN00	2063.25	-1449.00
WCN00	2063.25	-1629.00
WCP00	2063.25	-1809.00
HS3	1896.50	-2171.75
HS2	1716.50	-2171.75
HS1	1536.50	-2171.75
HS0	1356.50	-2171.75
WDN	1176.50	-2171.75
WDP	996.50	-2171.75
FLT	816.50	-2171.75
CSN	636.50	-2171.75
RNW	456.50	-2171.75
IWSET	206.50	-2171.75
VCC	-53.50	-2171.75
VEE	-308.50	-2171.75
RCN	-563.50	-2171.75
RCP	-743.50	-2171.75
VCOLR	-923.50	-2171.75
RDN	-1103.50	-2171.75
RDP	-1283.50	-2171.75
CN2N	-1463.50	-2171.75
CN2P	-1643.50	-2171.75
IRSET	-1897.50	-2171.75

1. Octagonal pins are for factory use only.

2. The die was designed so only one C2N pad needs to be bonded out. This is currently being verified.

3. The die was designed so only one C2P pad needs to be bonded out. This is currently being verified.

4. The capacitor connected to CN2N must also be connected to VEE.

VTC Inc.
Value the Customer™

VM61210

10-CHANNEL, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER WITH SERVO WRITE

PRELIMINARY

August, 1994

FEATURES

- High Performance
  - Read Voltage Gain = 150 V/V Typical
  - Input Noise = 0.65 nV/√Hz Typical
  - Head Inductance Range = 100 nH to 500 nH
  - Write Current Range = 20 - 40 mA
  - Input Capacitance = 18 pF Typical
  - Rise Time = 4 ns Maximum (L_H = 200 nH, I_W = 30 mA)
- Operates from +5 and -3 Volt Power Supplies
- Up to 10-Channels Available
- Multi-Channel Servo Write
- Fault Detect Capability
- Designed for Use With Four-Terminal MR Heads
- MR BIAS Current Range 6 - 16 mA
- Optional WDFF
- Voltage Sense Configuration

DESCRIPTION

The VM61210 is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM61210 contains a thin-film head writer, an MR reader and associated fault circuitry to address up to 10 heads. It also provides bias current and control loops for setting the DC voltages on the MR element. The VM61210 also provides a 5-channel servo write feature, enabling the user to write servo information directly through the preamplifier.

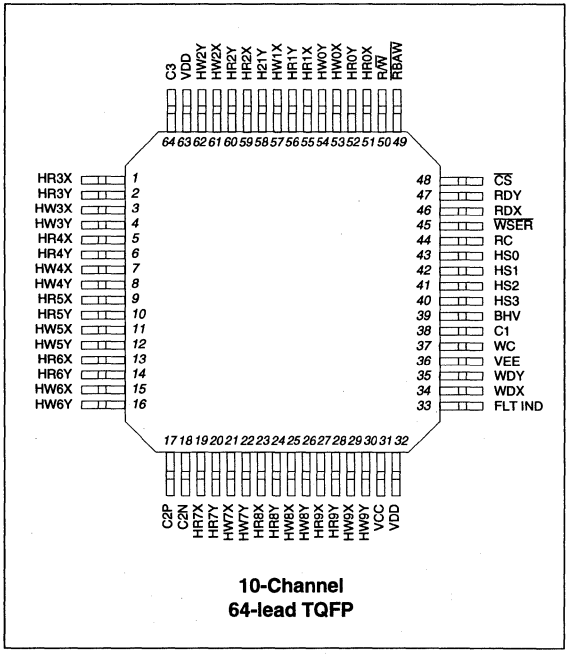
The VM61210 has two modes of operation. In read mode, the device operates as a low-noise differential preamplifier which senses resistance changes in the MR element that correspond to flux changes on the disk. The amplitude of the sense current is set either by an external resistor or by a current source and has a current gain of 20 mA/mA. In write mode, the circuit operates as a thin-film head write current switch, driving the thin-film write element of the MR head. The write current is externally programmed either by a resistor or an external current source and has a current gain of 20 mA/mA.

Fault protection is provided so during power sequencing, voltage faults or an invalid head select, the write current generator is disabled protecting the disk from potential transients. For added data protection, internal pull-up resistors are connected to the mode select lines, $\overline{CS}$ and R/$\overline{W}$, to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition.

The VM61210 operates from +5V, -3V power supplies. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters a sleep mode which reduces the power dissipation to only 116mW.

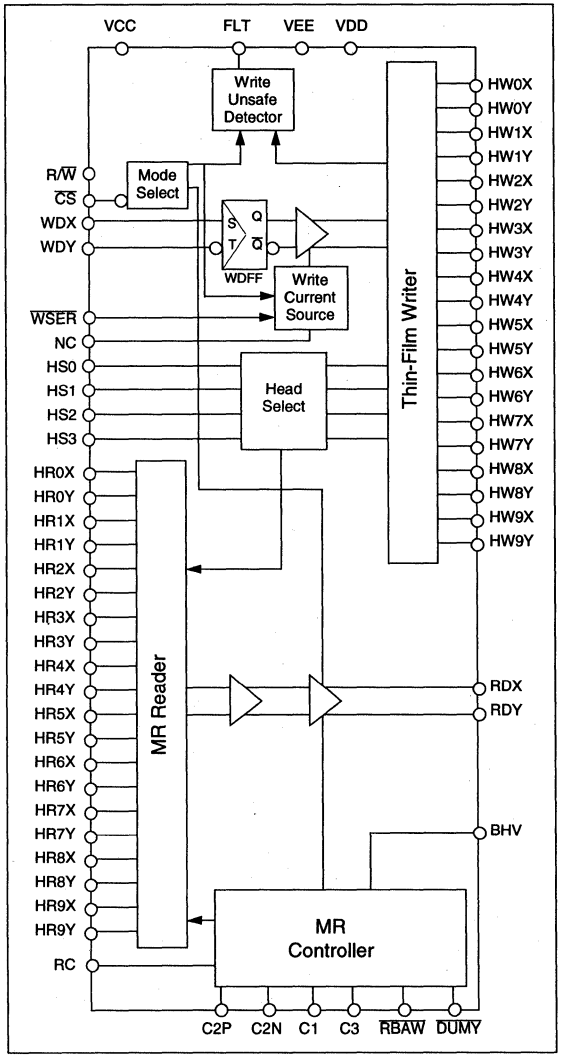
The VM61210 is available in die form for chip-on-flex applications or in several package configurations. Please consult VTC for details.

CONNECTION DIAGRAM



10-Channel
64-lead TQFP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{EE} ..... +0.3V to -7V
- V_{DD} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... V_{EE} -0.3V to (V_{DD} + 0.3)V
- Head Port Voltage V_H ..... V_{EE} -0.3V to (V_{DD} + 0.3)V

Output Current:
- RDX, RDY: I_O .....-10mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 64-lead TQFP ..... 70°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{EE} ..... -3V ± 10%
- V_{DD} .....+5V ± 10%

Junction Temperature (T_J) ..... 0°C to 125°C

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head. The magnitude of the write current is externally programmed either by a resistor or a current source. The writer has a current gain of 20 mA/mA. The appropriate TTL level on $\overline{CS}$, R/$\overline{W}$ and $\overline{WSER}$ lines puts the preamp in the write mode and activates the write unsafe detect circuitry. In the write mode, the write data (PECL) signals on the WDX and WDY lines drive the internal flip-flop which drives the current switch to the thin film writer.The write data flip-flop internal to the chip is an option. The value of the write current is set by an external resistor connected between WC and ground.

Read Mode

In the read mode, the circuit operates as a low noise differential amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk. In this mode, the bias generator, the input multiplexer, the read preamp and the read fault detection circuitry is turned on. The VM61210 uses the current bias, voltage sensing, MR design. Due to the use of a negative supply, the MR head center voltage is at ground potential minimizing current spikes during disk contact.

Servo Write

In servo write mode, five channels of the VM61210 are active at the same time. Pin $\overline{WSER}$ controls the servo mode and HS0 controls which five heads are simultaneously written. When $\overline{WSER}$, $\overline{CS}$ and R/$\overline{W}$ are low, the chip is in servo write mode: five channels are written at the same time dependent on the state of HS0. When HS0 = 0, heads 0, 1, 2, 3 and 4 are written and when HS0 = 5V, heads 5, 6, 7, 8 and 9 are written (see Table 2). When $\overline{WSER}$ is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select lines.

Fault Detect

The VM61210 is equipped with fault detect circuitry for both the read and write mode. In the write and servo mode, a TTL high on the FLT IND line indicates a fault condition. In the read mode, a TTL low on the FLT line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- WDI frequency too low
- Device in read or idle mode
- Open head
- Head short to ground
- No write current
- MR bias current too high

The following conditions will result in the shutdown of the write current source internal to the chip:

- Low power supply voltage
- Head short to ground
- Invalid head select code
- Non write mode

MR Bias Active During Write($\overline{RBAW}$)

Applying a TTL low level on $\overline{RBAW}$ during write mode turns on the MR bias prior to entering read mode to speed up the write to read transition time (see Table 3).

Table 1: Mode Select

MODE	*$\overline{CS}$*	*R/$\overline{W}$*	*$\overline{WSER}$*	*DESCRIPTION*
Read	0	1	1	Preamp in read mode
Write	0	0	1	Preamp in write mode
Servo	0	0	0	Preamp in servo bank mode
Idle	1	X	X	Preamp in idle mode

Table 2: Servo Mode Head Select

HS0	*$\overline{CS}$*	*R/$\overline{W}$*	*$\overline{WSER}$*	*DESCRIPTION*
0	0	0	0	Head 0, 1, 2, 3, and 4 are on for servo write
1	0	0	0	Head 5, 6, 7, 8, and 9 are on for servo write

Table 3: Read Bias Active During Write Mode

MODE	*R/$\overline{W}$*	*$\overline{RBAW}$*	*MR BIAS CURRENT*
Read	1	X	On
Write	0	0	On
Write	0	1 or open	Off

Table 4: Head Select

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

PIN_FUNCTION LIST AND DESCRIPTION

1)	$\overline{CS}$	(I)	Chip select: a TTL low level enables the device.
2)	R/$\overline{W}$	(I*)	Read/Write: a TTL high level enables read mode.
3)	HS0-HS3	(I*)	Head Select: selects one of the ten heads.
4)	$\overline{RBAW}$	(I*)	A low level enables the Read Bias Active in Write mode.
5)	$\overline{WSER}$	(I*)	A low level enables servo mode.
6)	FLT	(O*)	Write/Read Fault: A high level indicates a fault n write mode. A low level indicates a fault in read mode.
7)	WDX, WDY	(I*)	Differential Pseudo-ECL write data in: a positive edge on WDX toggles the direction of the head current.
8)	HR0X-HR9X	(I)	MR head connections, positive end.
9)	HR0Y-HR9Y	(I)	MR head connections, negative end.
10)	HW0X-HW9X	(O)	Thin-Film write head connections, positive end.
11)	HW0Y-HW9Y	(O)	Thin-Film write head connections, negative end
12)	RDX, RDY	(O*)	Read Data: Differential read signal outputs.
13)	WC	(*)	Write current pin: used to set the magnitude of write current.
14)	RC	(*)	MR bias reference pin: used to set the magnitude of MR bias current.
15)	C1		Noise bypass capacitor input for the MR bias current source.
16)	C2P, C2N		Reader AC coupling capacitor.
17)	C3		Compensation capacitor for the MR head current loop.
18)	BHV	(O)	Buffered MR Head Voltage output.
19)	VEE	-	-3.0V supply
20)	VDD	-	+5.0V supply
21)	VCC	-	Ground

* When more than one device is used, these signals can be wire OR'ed together

I = Input pin

O = Output pin

STATIC (DC) CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-3.3V < V_{EE} < -2.7V$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{DD} Power Supply Current	I_{DD}	Read Mode, I_{MR} = 11mA		65	90	mA
		Write Mode, I_w = 30mA, I_{MR} = 11mA		105	140	
		Idle Mode		4	5	
		Read Bias Active in Write Mode, I_W = 30mA, I_{MR} = 11mA		130	175	
		Servo Mode, I_W = 30mA		200	265	
V_{EE} Power Supply Current	I_{EE}	Read Mode, I_{MR} = 11mA		45	60	mA
		Write Mode, I_w = 30mA, I_{MR} = 11mA		75	105	
		Idle Mode		2.5	3.5	
		Read Bias Active in Write Mode, I_W = 30mA, I_{MR} = 11mA		95	125	
		Servo Mode, I_W = 30mA		180	240	
Power Supply Dissipation	P_d	Read Mode, I_{MR} = 11mA		460	630	mW
		Write Mode, I_w = 30mA, I_{MR} = 11mA		750	995	
		Idle Mode		28	35	
		Read Bias Active in Write Mode, I_W = 30mA, I_{MR} = 11mA		935	1250	
		Servo Mode, I_W = 30mA		1540	2040	
Input High Voltage	V_{IH}	PECL	V_{DD} - 1.0		V_{DD} - 0.7	V
		TTL	2.0		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{DD} - 1.9		V_{DD} - 1.6	V
		TTL	-0.3		0.8	V
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-160			µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{DD} Fault Threshold	V_{DTH}		3.5		4.2	V
V_{EE} Fault Threshold	V_{ETH}		-2.5		-2.1	V

READER CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-3.3V < V_{EE} < -2.7V$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		6		16	mA
MR Head Current Tolerance	I_{MR}	$6 < I_{MR} < 16$ mA	-5		+5	%
Unselected MR Head Current					10	µA
MR Bias Reference Voltage	V_{RC}	$2500 < R_{RC} < 6667\ \Omega$		2.0		V
IRC to MR Bias Current Gain	A_{IMR}	$2500 < R_{RC} < 6667\ \Omega$		20		mA/mA
Differential Voltage Gain	A_V	$V_{IN} = 1mV_{pp}$ @10MHz, R_L(RDP, RDN) = 1kΩ, I_{MR} = 11mA, $R_{MR} = 22\Omega$	125	150	175	V/V
Passband Upper Frequency Limit	f_{HR}	$R_{MR} = 22\Omega$; L_{MR} = 80nH; -1dB	70	100		MHz
		-3dB	90	120		
Passband Lower -3dB Frequency Limit	f_{LR}	$R_{MR} = 22\Omega$; L_{MR} = 80nH	0.1		0.8	MHz
Equivalent Input Noise	e_n	$R_{MR} = 22\Omega$; I_{MR} = 11mA; 1 < f < 20 MHz		0.65	0.80	nV/√Hz
Differential Input Capacitance	C_{IN}	$R_{MR} = 22\Omega$; I_{MR} = 11mA		18	30	pF
Differential Input Resistance	R_{IN}	I_{MR} = 11mA	600	1400		W
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at $V_{IN} = 1mV_{pp}$ @ f = 5 MHz	8			mV_{pp}
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, I_{MR} = 11mA, $R_{MR} = 22\Omega$, 1 < f < 60 MHz	45			dB
Power Supply Rejection Ratio	PSRR	$100mV_{pp}$ on V_{DD} or V_{EE}, I_{MR} = 11mA, $R_{MR} = 22\Omega$, 1 < f < 60 MHz	45			dB
Channel Separation	CS	Unselected Channels: $V_{IN} = 100mV_{pp}$, 1 < f < 60 MHz	45			dB
Output Offset Voltage	V_{OS}	I_{MR} = 11mA, $R_{MR} = 22\Omega$	-100		100	mV
Common Mode Output Voltage	V_{OCM}	Read Mode		V_{DD} -2.8		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode			50	W
Output Current	I_O	AC Coupled Load, RDX to RDY	1.5			mA
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK} = 10MΩ			100	µA
		Maximum Peak Discharge, C_{DISK} = 300pF, R_{DISK} = 10MΩ			1	mA
MR Head Potential, Selected Head	V_{MR}	I_{MR} = 11mA, R_{MR} = 22Ω	-100		600	mV
Buffered Head Voltage	BHV		$I_{MR}*R_{MR}$ - 10		$I_{MR}*R_{MR}$ + 10	mV

WRITER CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-3.3 < V_{EE} < -2.7$ $I_W = 30mA$, $L_H = 220nH$, $R_H = 25\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}			2.0		V
I_{WC} to Write Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = V_{WC} * A_I$	36	40	44	V
Write Current Range	I_W		20		40	mA
Write Current Tolerance	ΔI_W	$20 < I_W < 40$ mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open Head		7.8		V_{pp}
Unselected Head Transition Current	I_{UH}	$I_W = 30mA$			50	μA_{pk}
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	Internal Damping Resistance	555	695	835	Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1.0			MHz

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-3.3 < V_{EE} < -2.7$, $I_W = 30mA$, $L_H = 220nH$, $R_H = 25\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			0.1	µs
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope; $\overline{RBAW}$ low for 10µs			2.0	µs
$\overline{CS}$ to Read Mode	t_{CS}	To 90% of envelope			60	µs
HS0 - HS3 to Any Head	t_{HS}	To 90% of envelope			30	µs
$\overline{CS}$ to Unselect	t_{RI}	To 10% of read envelope or write current			0.5	µs
Safe to Unsafe*	t_{D1}	50% WDP to 50% FLT		0.7	1.5	µs
Unsafe to Safe*	t_{D2}	50% WDP to 50% FLT		0.1	0.3	µs
Head Current Propagation Delay*	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, $L_H = 0$, $R_H = 0$			0.5	ns
Rise/Fall Time	t_r / t_f	20-80%; $I_W = 30mA$; $L_H = 220nH$, $R_H = 25\Omega$			4	ns

*See Figure 1 for write mode timing diagram.

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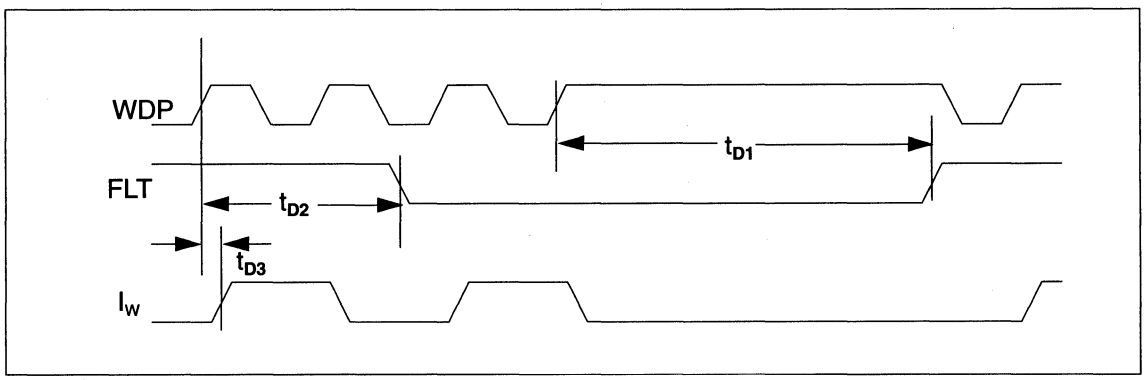
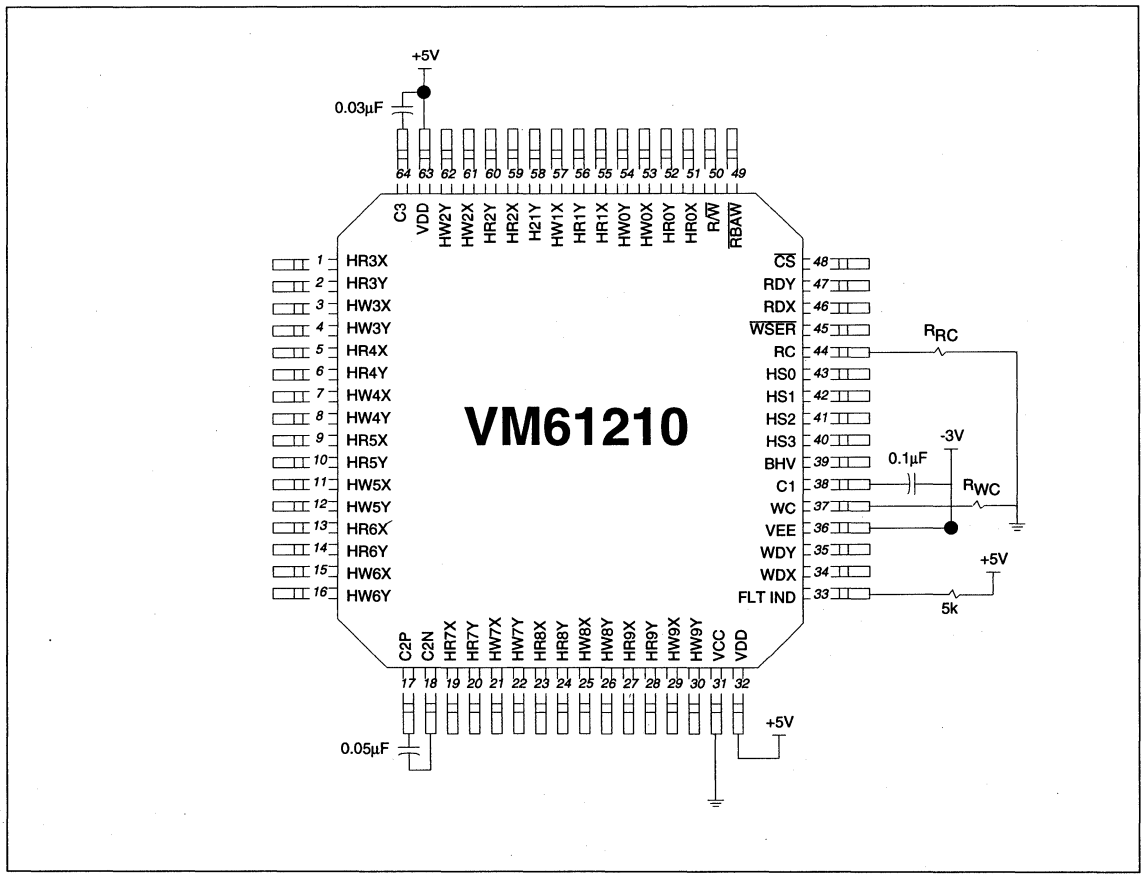


Figure 1: Write Mode Timing Diagram

TYPICAL CONNECTION DIAGRAM



Note 1: IRC = MR Bias Current = $40/R_{RSET}$
Note 2: I_{WC} = Write Current = $40/R_{WC}(1+R_H/700)$, R_H = Head Series Resistance
Note 3: V_{DD} = +5V, V_{CC} = GND, V_{EE} = -3V
Note 4: Pins C3 is connected to pin 32 internally, but external connection is preferred for noise immunity.

VTC Inc.
Value the Customer™

VM61312

12-CHANNEL, HIGH-PERFORMANCE, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

PRELIMINARY

August,1994

FEATURES

- Read Gain = 350 V/V
- MR Bias Current Range = 8 - 20 mA
- Low Input Noise = 0.55 nV/√Hz Maximum
- Write Current Range = 20 - 40 mA
- Head Inductance Range = 0.15 - 0.4 µH
- Low Idle Power = 116 mW Maximum
- Rise Time = 4 ns Maximum, Typical Load
- Power Supply Fault Protection
- +5V, -4.5V Power Supplies
- Write Unsafe Detection
- Head-to-Disk Contact Monitor
- Mask-Selectable Write Damping Resistor
- Reduced Mode and Head Selection Delays in FAST Mode
- Disk Voltage Monitor
- Differential PECL Write Data Inputs
- Current Sense Configuration

FUNCTIONAL DESCRIPTION

The VM61312 is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM61312 contains a thin-film head writer, an MR reader and associated fault circuitry to address up to 12 heads. It also provides bias current and control loops for setting the DC voltages on the MR element.

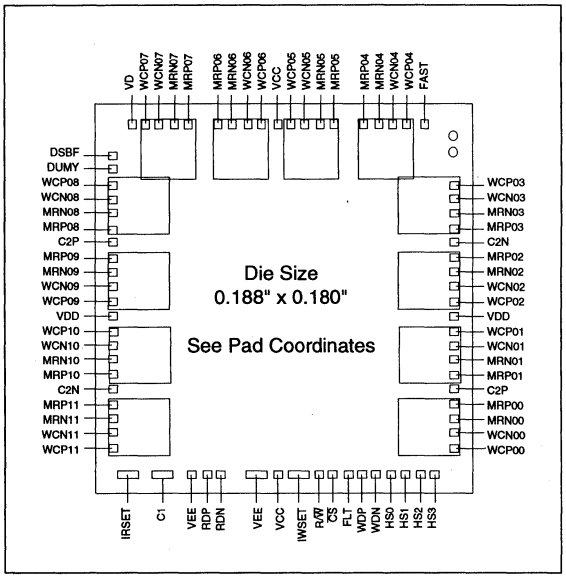
The VM61312 has two modes of operation. In read mode, the device operates as a low-noise differential preamplifier which senses resistance changes in the MR element that correspond to flux changes on the disk. The amplitude of the sense current is set either by an external resistor or by a current source and has a current gain of 20 mA/mA. In write mode, the circuit operates as a thin-film head write current switch, driving the thin-film write element of the MR head. The write current is externally programmed either by a resistor or an external current source and has a current gain of 20 mA/mA.

Fault protection is provided so during power sequencing, voltage faults or an invalid head select, the write current generator is disabled protecting the disk from potential transients. For added data protection, internal pull-up resistors are connected to the mode select lines, $\overline{CS}$ and R/$\overline{W}$, to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition.

The VM61312 operates from a +5V, -4.5V power supply. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters a sleep mode which reduces the power dissipation to only 116mW.

The VM61312 is available in die form for chip-on-flex applications or in several package configurations. Please consult VTC for details.

DIE PAD DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
- V_{DD} ..... -0.3V to + 7V
- V_{EE} ..... -7V to +0.3V

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{DD}+ 0.3V)

Storage Temperature T_{stg} .....-65˚ to 150˚C

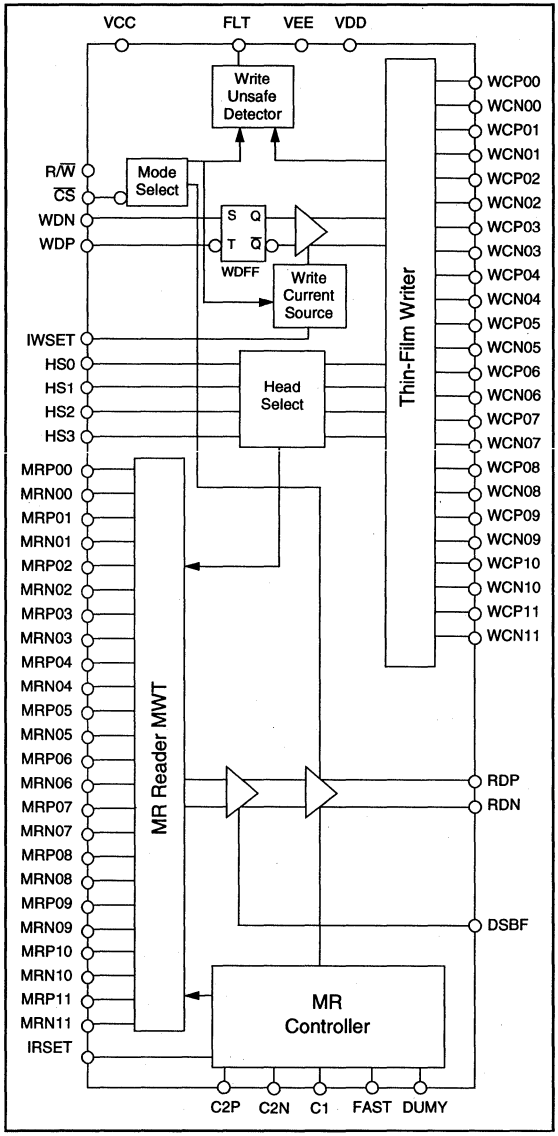
Junction Temperature T_J ..... 150˚C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{DD} .....+5V ± 10%
- V_{EE} ..... -4.5V ± 10%

Junction Temperature T_J ..... 0˚C to 125˚C

BLOCK DIAGRAM



CIRCUIT OPERATION

In all modes of operation, the VM61312 controls the common mode potential of all MR elements. This is necessary because the MR element cannot be insulated, so that a small voltage differential will cause arcing to the disk and damage the heads. Head voltages are held within ±250mV of the voltage on the VD pin, which monitors the disk potential of the drive. Thus, the disk may be grounded, as is done in disk drives having conventional thin film or ferrite recording heads, or isolated as the application may require.

In read mode, the VM61312 activates the MR bias current source, which then drives the selected MR element. The read bias current magnitude is determined by an external resistor connected between the IRSET pin and VCC. An internally-generated 2.5 volt reference is present at the IRSET pin. The magnitude of the MR bias current is:

$$I_{MR} = 50/R_{RSET} \qquad \textit{(eq. 1)}$$

where R_{RSET} is the resistor connected at IRSET.

The fault output pin, FLT, is high to indicate a non-fault condition. If the voltage drops below a certain threshold on either supply, FLT will be pulled low to indicate a fault. Also, if a head-to-disk contact occurs, the thermal asperity in the MR element will result in an abnormally high readback signal, which is monitored by detection circuitry and will be also flagged by a low FLT output.

The read preamplifier is activated and connected to the selected head. The write current source and write unsafe detection circuitry is deactivated. RDP and RDN outputs are emitter follower and are in phase with the MRP and MRN head ports. These outputs should be AC-coupled to the load. The output common mode voltage is maintained in the write mode, thereby substantially reducing the write-to-read recovery delay in the subsequent pulse detection circuitry.

In write mode, the preamplifier is shut off and the VM61312 is converted to a current switch. However, MR bias current is maintained in order to minimize the write-to-read delay. The write current source is activated and drives the thin film element of the selected head. The polarity of the current is initially into the WCN port following a read-to-write transition. Write current polarity is reversed on low-to-high transitions of the write data input (WDP low-to-high). Circuitry is activated to detect various fault conditions. If any of the faults occur, they will be flagged as a high voltage output on the FLT pin. In addition, if a VDD fault occurs, the write current source is deactivated in order to protect recorded data.

The write current magnitude is determined by an external resistor connected between the IWSET pin and VCC. An internally-generated 2.5 volt reference is present at the IWSET pin. The magnitude of the write current (0-peak) is:

$$I_W = 50/\left[R_W \times \left(1 + \frac{R_H}{R_D}\right)\right] \qquad \textit{(eq. 2)}$$

where R_W is the resistor connected at IWSET, R_H is the series resistance of the head, and R_D is an internal damping resistor of 360Ω.

Power supply fault protection provides data security by disabling the write current generator during a VDD fault or power-up/down. The writer is independent of VEE, so VEE faults do not affect it. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin FLT. Two positive transitions of write data may be required to clear the fault after the safe condition is restored.

- No write current
- Open write head
- Write Data frequency too low
- Device in read or idle mode
- Head shorted to ground

Fast mode is utilized during head-to-head and idle-to-read transitions. When the FAST mode pin is high, the unity-gain fre-

quency of the offset control loop is increased such that it is inside the passband of the reader, allowing the delay to be reduced to less than 5µs. This pin must be brought low before read data is valid.

A DUMY mode pin allows the selection of a dummy head in read or write mode. MR bias current is routed to an internal resistor, and the write current source is deactivated. This mode is optionally used during power-up/down and following head-to-disk contacts. When the DUMY pin is high, the write current source is disabled to protect recorded data. An internal pull-up resistor is provided in event of an accidental open. If this pin is not used it should be grounded for normal operation.

In idle mode, the MR bias and write current sources are deactivated, and the device enters a low-power mode in which power dissipation is less than 116mW. Write and read fault detection circuitry is disabled. MR common mode and offset control loops still receive power in order to reduce idle-to-read mode recovery.

Mode control and head selection are accomplished via $\overline{CS}$, R/$\overline{W}$, and HS0-HS3 pins. Internal pull-up resistors are provided on $\overline{CS}$ and R/$\overline{W}$ pins to force the device into a non-writing condition if either control line is opened accidentally. In addition, invalid head select codes disable the writer and select head MR00. Truth tables for mode and head selection are shown in Table 1 and Table 2, respectively.

Table 1: Mode Select Logic

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select Logic

HS3	*HS2*	*HS1*	*HS0*	*DUMY*	*HEAD*
X	X	X	X	1	DUMY
0	0	0	0	0	00
0	0	0	1	0	01
0	0	1	0	0	02
0	0	1	1	0	03
0	1	0	0	0	04
0	1	0	1	0	05
0	1	1	0	0	06
0	1	1	1	0	07
1	0	0	0	0	08
1	0	0	1	0	09
1	0	1	0	0	10
1	0	1	1	0	11
1	1	X	X	0	00

PIN_FUNCTION LIST AND DESCRIPTION

1)	$\overline{CS}$	(I)	Chip select: a low level enables the device.
2)	R/$\overline{W}$	(I*)	Read/Write: a high level enables read mode.
3)	HS0-HS3	(I*)	Head Select: selects one of the twelve heads.
4)	DUMY	(I*)	A high level enables the dumy mode.
5)	FAST	(I*)	A high level enables fast settling of the reader.
6)	FLT	(O*)	Write/Read Fault: A high level indicates a fault in write mode. A low level indicates a fault in read mode.
7)	WDP, WDN	(I*)	Differential Pseudo-ECL write data in: a positive edge on WDP toggles the direction of the head current.
8)	MRP00-MRP11	(I)	MR head connections, positive end.
9)	MRN00-MRN11	(I)	MR head connections, negative end.
10)	WCP00-WCP11	(O)	Write head connections, positive end.
11)	WCN00-WCN11	(O)	Write head connections, negative end.
12)	RDP, RDN	(O*)	Read Data: Differential read signal outputs.
13)	IWSET	(*)	Write current pin: used to set the magnitude of write current.
14)	IRSET	(*)	MR bias reference pin: used to set the magnitude of MR bias current.
15)	C2P,C2N	(*)	Compensation capacitor for the MR head current loop.
16)	C1	(*)	Noise bypass for the MR bias current generator.
17)	VD	(I*)	Analog reference for the disk bias.
18)	DSBF	(*)	Disables disk contact detector if tied to VCC.
19)	VEE	-	-4.5V supply
20)	VDD	-	+5V supply
21)	VCC	-	Ground

* When more than one device is used, these signals can be wire OR'ed together
I = Input pin
O = Output pin

STATIC (DC) CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, 0°C < T_A < 80°C, 4.5V < V_{DD} < 5.5V, -5.0V < V_{EE} < -4.0V.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{DD} Power Supply Current	I_{DD}	Read Mode, I_{MR} = 16mA			95	mA
		Write Mode, I_W = 20mA, I_{MR} = 16mA			140	mA
		Idle Mode			12	mA
V_{EE} Power Supply Current	I_{EE}	Read Mode, I_{MR} = 16mA			70	mA
		Write Mode, I_W = 20mA, I_{MR} = 16mA			65	mA
		Idle Mode			10	mA
Power Supply Dissipation	P_d	Read Mode, I_{MR} = 16mA			873	mW
		Write Mode, I_W = 20mA, I_{MR} = 16mA			1095	mW
		Idle Mode			116	mW
Input High Voltage	V_{IH}	PECL	V_{DD} - 1.0		V_{DD} - 0.7	V
		CMOS	3.5			V
Input Low Voltage	V_{IL}	PECL	V_{DD} - 1.9		V_{DD} - 1.6	V
		CMOS			1.65	V
Disk Reference Voltage Range	V_D		-250		250	mV
Input High Current	I_{IH}	PECL			120	µA
		CMOS	-160		160	µA
Input Low Current	I_{IL}	PECL			120	µA
		CMOS	-160		160	µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{DD} Fault Threshold	V_{DTH}		3.75		4.25	V
V_{EE} Fault Threshold	V_{ETH}		-3.75		-3.25	V

DYNAMIC (AC) CHARACTERISTICS

READ MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0V < V_{EE} < -4.0$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		8		20	mA
MR Head Current Tolerance	I_{MR}	$8 < I_{MR} < 18$ mA	-5		+5	%
MR Bias Reference Voltage	V_{RSET}	$2775 < R_{RSET} < 6250\Omega$		2.5		V
IRSET to MR Bias Current Gain	A_{IMR}	$2775 < R_{RSET} < 6250\Omega$		20		mA/mA
Differential Voltage Gain	A_V	$V_{IN} = 1mV_{pp}$ @10MHz, R_L (RDP, RDN) = 1kΩ, I_{MR} = 16mA, $R_{MR} = 12\Omega$		350		V/V
Passband Upper Frequency Limit	f_{HR}	-1dB: $R_{MR} = 13\Omega$; L_{MR} = 20nH		40		MHz
		-3dB	60			
Passband Lower -3dB Frequency Limit	f_{LR}	$R_{MR} = 12\Omega$; L_{MR} = 20nH	0.1		0.5	MHz
Equivalent Input Noise	e_n	$R_{MR} = 13\Omega$; I_{MR} = 16mA; 1 < f < 20 MHz			0.55	nV/√Hz
Differential Input Capacitance	C_{IN}	$R_{MR} = 12\Omega$; I_{MR} = 16mA			10	pF
Differential Input Resistance	R_{IN}	I_{MR} = 16mA			4	Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at $V_{IN} = 1mV_{pp}$ @ f = 10 MHz	4			mV_{pp}
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVpp, I_{MR} = 16mA, $R_{MR} = 12\Omega$, 1 < f < 50 MHz	30			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz, on V_{DD} or V_{EE}, I_{MR} = 16mA, $R_{MR} = 12\Omega$, 1 < f < 50 MHz	30			dB
Channel Separation	CS	Unselected Channels: V_{IN} = 100mVp-p @ 5MHz, 1 < f < 50 MHz	30			dB
Output Offset Voltage	V_{OS}	I_{MR} = 16mA, $R_{MR} = 12\Omega$			100	mV
Common Mode Output Voltage	V_{OCM}		V_{DD} - 2.8	V_{DD} -2.5	V_{DD}-2.2	V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			250	mV
Single-Ended Output Resistance	R_{SEO}				35	Ω
Output Current	I_O	AC Coupled Load, RDP to RDN	±1.5			mA
Total Harmonic Distortion	THD	$V_{in} = 4mV_{pp}$; ten harmonics			0.5	%
MR Head-to-Disk Contact Current	I_{DISK}	Extended contact, $R_{DISK} = 10M\Omega$			100	µA
		Maximum peak discharge, C_{DISK} = 300pF, $R_{DISK} = 10M\Omega$			20	mA
MR Head Potential	V_{MR}	I_{MR} = 16mA, $R_{MR} = 12\Omega$	-300		300	mV

WRITE MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.
$0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0 < V_{EE} < -4.0$, $I_W = 30mA$, $L_H = 220nH$, $R_H = 30\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
I_{WSET} Pin Voltage	V_{WSET}			2.5		V
I_{WSET} to Write Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = V_{WSET} \cdot A_I$	46	50	54	V
Write Current Range	I_W		20		40	mA
Write Current Tolerance	ΔI_W	$6 < I_W < 30$ mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open head	9	10		V_{pp}
Unselected Head Transition Current	I_{UH}	$I_W = 30mA$			50	μA_{pk}
Differential Output Capacitance	C_O				6	pF
Differential Output Resistance	R_O	Internal damping resistance	290	360	430	Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT = Low	1			MHz

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{DD} < 5.5V$, $-5.0 < V_{EE} < -4.0$, $I_W = 30mA$, $L_H = 220nH$, $R_H = 30\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current			0.5	µs
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope			0.5	µs
$\overline{CS}$ to Read Mode	t_{CS}	To 90% of envelope; FAST = low			50	µs
		† FAST = high for 3.5µs			5	µs
$\overline{CS}$ to Write Mode	t_{CS}	To 90% of write current			0.5	µs
HS0 - HS3 to Any Head	t_{HS}	To 90% of envelope; FAST = low			50	µs
		† FAST = high for 3.5µs			5	µs
DUMY Mode to Any Head	t_{DH}	To 90% of envelope; FAST = low			50	µs
		† FAST = high for 3.5µs			5	µs
$\overline{CS}$ to Unselect	t_{RI}	To 10% of read envelope or write current			0.6	µs
Safe to Unsafe*	t_{D1}	50% WDP to 50% FLT	0.6		3.6	µs
Unsafe to Safe*	t_{D2}	50% WDP to 50% FLT			1	µs
Head Current Propagation Delay*	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, $L_H = 0$, $R_H = 0$			0.2	ns
Rise/Fall Time	t_r / t_f	20-80%; $I_W = 20mA$; $L_H = 220nH$, $R_H = 40\Omega$		3	4	ns
		$L_H = 0$, $R_H = 0$; $I_W = 30mA$			TBD	ns
Settling Time	T_{WSET}	$I_{WC} = 30mA$, $L_H = 220nH$, $R_H = 40\Omega$; to ±10%			TBD	ns
Overshoot	W_{COV}	$I_{WC} = 30mA$; $L_H = 220nH$, $R_H = 40\Omega$		10		%

*See Figure 1 for write mode timing diagram.
† See Figure 2 for read mode timing diagram.

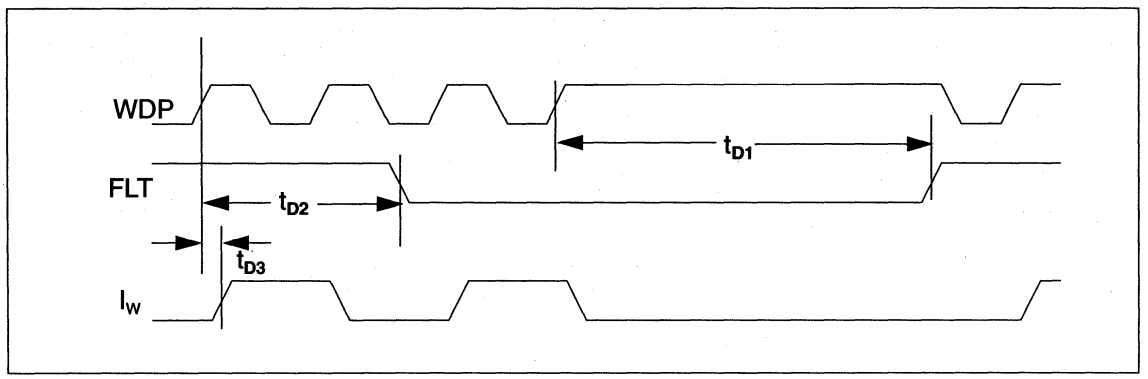


Figure 1: Write Mode Timing Diagram

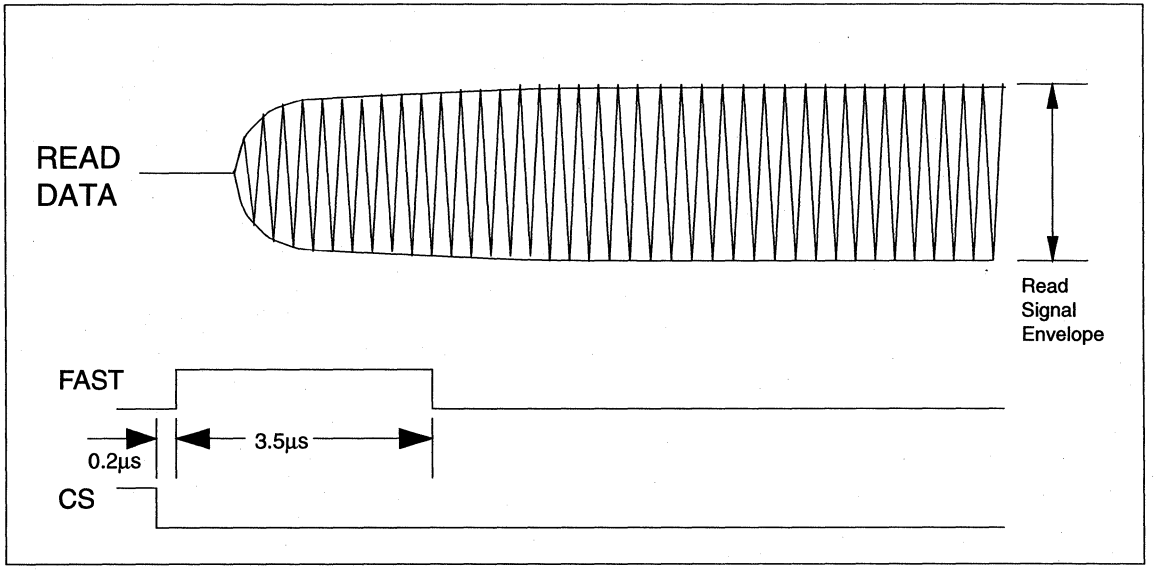
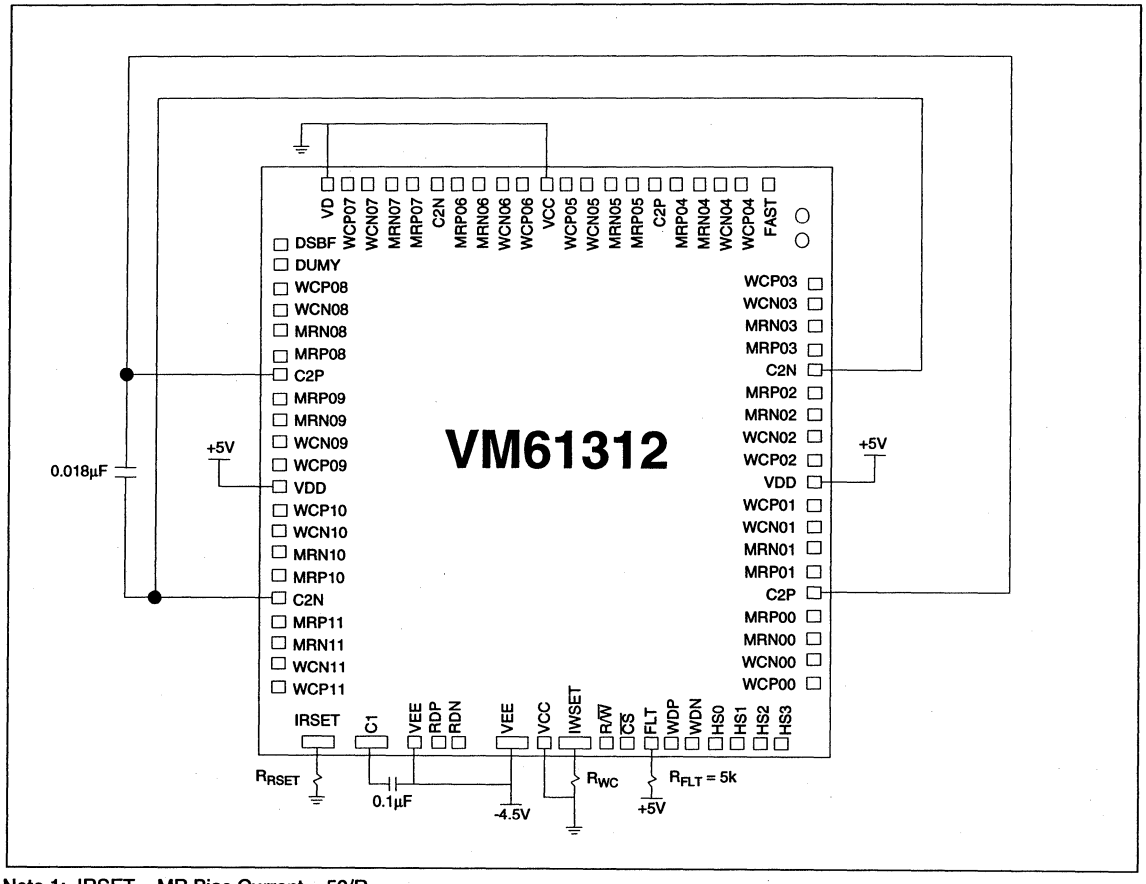


Figure 2: Read Mode Timing Diagram. Also applies to DUMY and HS0 - HS3.

TYPICAL CONNECTION DIAGRAM



Note 1: IRSET = MR Bias Current = $50/R_{RSET}$
Note 2: I_{WSET} = Write Current = $50/R_{WC}(1+R_H/360)$, R_H = Head Series Resistance
Note 3: V_{DD} = +5V, V_{CC} = GND, V_{EE} = -4.5V

VM61312 PAD COORDINATES

PIN NAME	X AXIS	Y AXIS
WCP11	-2063.25	-1809.00
WCN11	-2063.25	-1629.00
MRN11	-2063.25	-1449.00
MRP11	-2063.25	-1269.00
C2N	-2063.25	-1089.00
MRP10	-2063.25	-909.00
MRN10	-2063.25	-729.00
WCN10	-2063.25	-549.00
WCP10	-2063.25	-369.00
VDD	-2063.25	-189.00
WCP09	-2063.25	-9.00
WCN09	-2063.25	171.00
MRN09	-2063.25	351.00
MRP09	-2063.25	531.00
C2P	-2063.25	711.00
MRP08	-2063.25	891.00
MRN08	-2063.25	1071.00
WCN08	-2063.25	1251.00
WCP08	-2063.25	1431.00
DUMY	-2063.25	1618.00
DSBF	-2063.25	1814.75
VD	-1820.00	2172.00
WCP07	-1620.00	2172.00
WCN07	-1440.00	2172.00
MRN07	-1260.00	2172.00
MRP07	-1080.00	2172.00
MRP06	-720.00	2172.00
MRN06	-540.00	2172.00
WCN06	-360.00	2172.00
WCP06	-180.00	2172.00
VCC	0	2172.00
WCP05	180.00	2172.00
WCN05	360.00	2172.00
MRN05	540.00	2172.00
MRP05	720.00	2172.00
MRP04	1080.00	2172.00
MRN04	1260.00	2172.00
WCN04	1440.00	2172.00
WCP04	1620.00	2172.00
FAST	1860.00	2172.00
WCP03	2063.25	1431.00
WCN03	2063.25	1251.00
MRN03	2063.25	1071.00
MRP03	2063.25	891.00
C2N	2063.25	711.00
MRP02	2063.25	531.00
MRN02	2063.25	351.00
WCN02	2063.25	171.00
WCP02	2063.25	-9.00
VDD	2063.25	-189.00
WCP01	2063.25	-369.00
WCN01	2063.25	-549.00
MRN01	2063.25	-729.00
MRP01	2063.25	-909.00
C2P	2063.25	-1089.00
MRP00	2063.25	-1269.00
MRN00	2063.25	-1449.00
WCN00	2063.25	-1629.00
WCP00	2063.25	-1809.00
HS3	1896.50	-2171.75
HS2	1716.50	-2171.75
HS1	1536.50	-2171.75
HS0	1356.50	-2171.75
WDN	1176.50	-2171.75
WDP	996.50	-2171.75
FLT	816.50	-2171.75
CSN	636.50	-2171.75
RWN	456.50	-2171.75
IWSET	201.50	-2171.75
VCC	-53.50	-2171.75
VEE	-308.50	-2171.75
RDN	-563.50	-2171.75
RDP	-743.50	-2171.75
VEE	-1103.50	-2171.75
C1	-1358.50	-2171.75
IRSET	-1898.50	-2171.75

1. Octagonal pins are for factory use only.

2. The die was designed so only one C2N pad needs to be bonded out. This is currently being verified.

3. The die was designed so only one C2P pad needs to be bonded out. This is currently being verified.

4. The capacitor connected to CN2N must also be connected to VEE.

VTC Inc.
Value the Customer™

VM6150

4 OR 8-CHANNEL, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER WITH SERVO WRITE

ADVANCE INFORMATION

September,1994

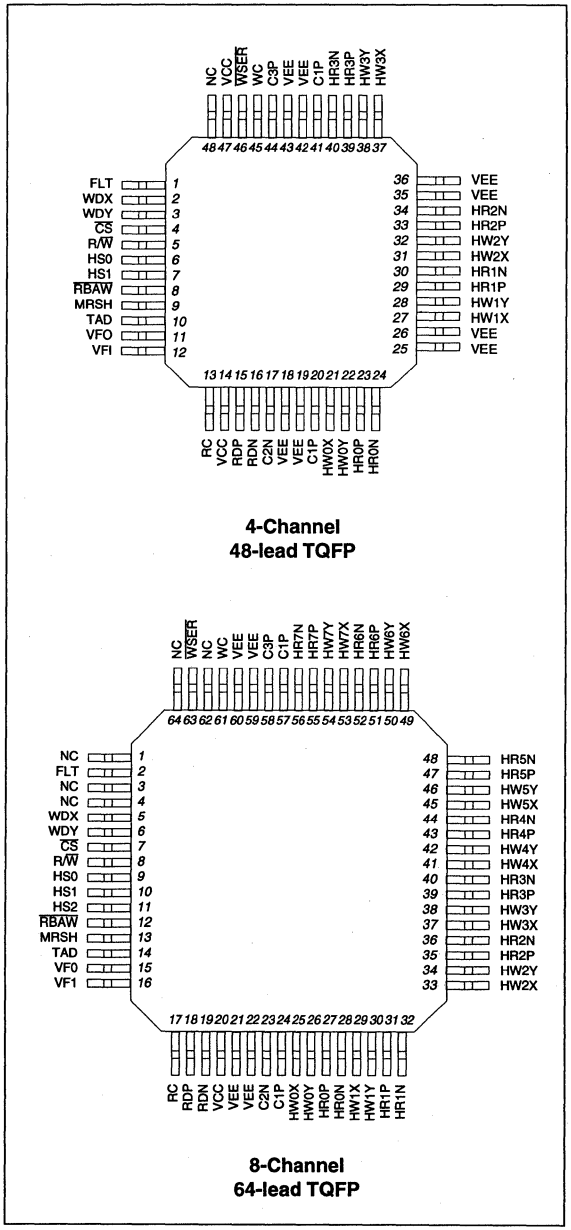
FEATURES

- High Performance
  - Bandwidth = 50 MHz Nominal
  - Input Noise = 0.65 nV/√Hz Nominal
  - Rise Time = 5.5 ns
- Single 5V Power Supply
- Current Bias/Current Sense Architecture
- Adjustable Bias Current
- Adjustable Write Current
- WUS Disable
- Dual Reader Input with One Side Grounded Internally
- Multichannel Servo Write
- Read, Write Fault Detection
- Thermal Asperity Detect
- Available in a Plastic TQFP Package

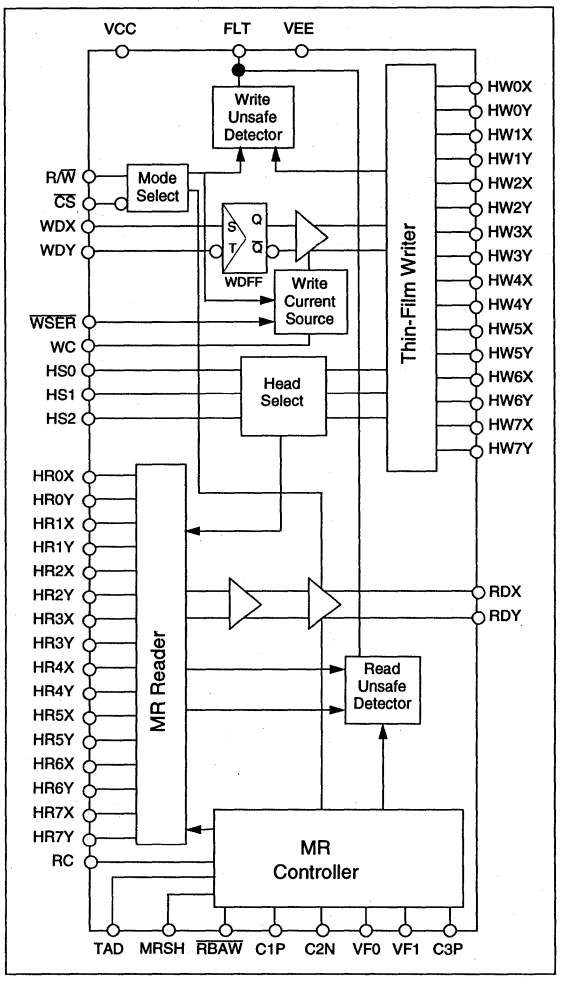
DESCRIPTION

The VM6150 is a high-performance read/write preamp designed for use with 4-terminal magneto-resistive recording heads. The VM6150 operates from +5V power supply. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detect, and multi-channel servo write. This device also provides low voltage power supply detection, power saving idle mode, and an optional write data flip-flop for NRZ and NRZI data.

CONNECTION DIAGRAMS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Write Current I_W 60mA
Input Voltages:
Digital Input Voltage V_{IN} ..... V_{EE} -0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H ..... V_{EE} -0.3V to (V_{CC} + 0.3)V
Output Current:
RDX, RDY: I_O .....-10mA
Junction Temperature ..... 150°C
Storage Temperature T_{stg} ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
48-lead TQFP ..... 80°C/W
64-lead TQFP ..... 70°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Junction Temperature (T_J) ..... 0°C to 125°C

Write Mode

In the write mode, the circuit operates as a thin film head write current switch, driving the thin film write element of the MR head. The magnitude of the write current is externally programmed either by a resistor or a current source. The writer has a current gain of 20 mA/mA. The appropriate TTL level on $\overline{CS}$, R/$\overline{W}$ and $\overline{WSER}$ lines puts the preamp in the write mode and activates the write unsafe detect circuitry. In the write mode, the write data (PECL) signals on the WDX and WDY lines drive the internal flip-flop which drives the current switch to the thin film writer. The write data flip-flop internal to the chip is an option.

Read Mode

In the read mode, the circuit operates as a low noise, single ended amplifier which senses resistance changes in the MR element which correspond to flux changes on the disk. The appropriate TTL level on $\overline{CS}$, R/$\overline{W}$ and $\overline{WSER}$ lines puts the preamp in the read mode and activates the read unsafe detect circuitry. The VM6150 uses a current bias, current sense architecture. The output of the read preamp is differential.

Servo Write

The VM6150 contains multi-channel servo write. The appropriate TTL levels applied to $\overline{WSER}$ and HS0 applies write current to 4 of the 8-channels for servo write applications.

Fault Detect

The VM6150 is equipped with fault detect circuitry for both the read and write mode. In the write and servo mode, a TTL high on the FLT IND line indicates a fault condition. In the read mode, a TTL low on the FLT IND line indicates a fault condition. The fault condition can be triggered by any of the following conditions:

- MR head shorted to ground (Reader)
- MR head thermal asperity (Reader)
- Open write head
- Low write current
- Low write data frequency
- Device in read or idle

The following conditions will result in the shutdown of the write current source internal to the chip:

- Low supply voltage

Table 1: Mode Select

MODE	*$\overline{CS}$*	*R/$\overline{W}$*	*$\overline{WSER}$*	*DESCRIPTION*
Read	0	1	1	Preamp in read mode
Write	0	0	1	Preamp in write mode
Servo	0	0	0	Preamp in servo bank mode
Idle	1	X	X	Preamp in idle mode

Table 2: Servo Mode Head Select

HS0	*$\overline{CS}$*	*R/$\overline{W}$*	*$\overline{WSER}$*	*DESCRIPTION*
0	0	0	0	Head 0, 2, 4 and 6 are on for servo write
1	0	0	0	Head 1, 3, 5, and 7 are on for servo write

Table 3: Frequency Compensation Table

VF1	*VF0*	*FUNCTION*
0	0	No compensation selected
0	1	Highest compensation frequency
1	0	Nominal compensation
1	1	Lowest compensation frequency

Table 4: Head Select

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

PIN_FUNCTION LIST AND DESCRIPTION

1)	$\overline{CS}$	(I)	Chip select: a TTL low level enables the device.
2)	R/$\overline{W}$	(I*)	Read/Write: a TTL high level enables read mode.
3)	HS0-HS2	(I*)	Head Select: selects one of the four or eight heads.
4)	$\overline{RBAW}$	(I*)	A low level enables the Read Bias Active in Write mode.
5)	$\overline{WSER}$	(I*)	A low level enables servo mode.
6)	FLT	(O*)	Write/Read Fault: A high level indicates a fault in write mode. A low level indicates a fault in read mode.
7)	WDX, WDY	(I*)	Differential Pseudo-ECL write data in: a negative edge on WDX toggles the direction of the head current.
8)	HR0P-HR7P	(I)	MR head connections, positive end.
9)	HR0N-HR7N	(I)	MR head connections, negative end.
10)	HW0X-HW7X	(O)	Thin-Film write head connections, positive end.
11)	HW0Y-HW7Y	(O)	Thin-Film write head connections, negative end
12)	RDP, RDN	(O*)	Read Data: Differential read signal outputs.
13)	WC	(*)	Write current reference pin: used to set the magnitude of write current.
14)	RC	(*)	MR bias reference pin: used to set the magnitude of MR bias current.
15)	C2N, C3P	-	Noise bypass capacitors.
16)	C1P	-	Compensation capacitor for the MR head current loop.
17)	VEE	-	Ground
18)	VCC	-	+5.0V supply
19)	VF0, VF1	-	Frequency compensation select bits.
20)	MRSH	-	MR Head Short Detect. A low level disables this function.
21)	TAD	-	Thermal Asperity Detect. A low level disables this function.

* When more than one device is used, these signals can be wire OR'ed together
I = Input pin
O = Output pin

STATIC (DC) CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{CC} < 5.5V$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
V_{CC} Power Supply Current	I_{CC}	Read Mode, I_{MR} = 20mA		70		mA
		Write Mode, I_w = 40mA		80		
		Idle Mode		10		
		Read Bias Active in Write Mode, I_W = 40mA, I_{MR} = 13mA		120		
		Servo Mode, I_W = 40mA		250		
Power Dissipation	P_d	Read Mode, I_{MR} = 11mA		350		mW
		Write Mode, I_w = 40mA		400		
		Idle Mode		50		
		Read Bias Active in Write Mode, I_W = 40mA, I_{MR} = 13mA		600		
		Servo Mode, I_W = 40mA		1250		
Input High Voltage	V_{IH}	PECL	V_{CC} - 1.0		V_{CC} - 0.7	V
		TTL	2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	PECL	V_{CC} - 1.9		V_{CC} - 1.6	V
		TTL	-0.3		0.8	V
Input High Current	I_{IH}	PECL			120	µA
		TTL, V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	PECL			100	µA
		TTL, V_{IL} = 0.4V	-160			µA
Output High Current	I_{OH}	FLT: V_{OH} = 5.0V			50	µA
Output Low Voltage	V_{OL}	FLT: I_{OL} = 4mA			0.5	V
V_{CC} Fault Threshold	V_{DTH}		3.5		4.2	V

READER CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{CC} < 5.5V$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		10	15	20	mA
MR Head Current Tolerance	I_{MR}	$10 < I_{MR} < 20$	-5		+5	%
Unselected MR Head Current					10	µA
MR Bias Reference Voltage	V_{RC}	$2k < R_{RC} < 4k\Omega$		2.0		V
IRC to MR Bias Current Gain	A_{IMR}	$2k < R_{RC} < 4k\Omega$		20		mA/mA
Differential Voltage Gain	A_V	$V_{IN} = 1mV_{pp}$ @10MHz, R_L(RDP, RDN) = 1kΩ, I_{MR} = 13mA, $R_{MR} = 25\Omega$		250		V/V
Passband Upper Frequency Limit	f_{HR}	$R_{MR} = 25\Omega$; L_{MR} = 100nH; -3dB		50		MHz
Passband Lower -3dB Frequency Limit	f_{LR}	$R_{MR} = 25\Omega$; L_{MR} = 100nH	0.1		0.3	MHz
Equivalent Input Noise	e_n	$R_{MR} = 25\Omega$; I_{MR} = 13mA; 1 < f < 20 MHz		0.7	0.9	$nV/\sqrt{Hz}$
Input Resistance	R_{IN}	I_{MR} = 13mA		2.5		Ω
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at $V_{IN} = 1mV_{pp}$ @ f = 5 MHz	TBD	8		mV_{pp}
Power Supply Rejection Ratio	PSRR	$100mV_{pp}$ on V_{CC} or V_{EE}, I_{MR} = 13mA, $R_{MR} = 25\Omega$, 1 < f < 30 MHz	TBD	30		dB
Channel Separation	CS	Unselected Channels: $V_{IN} = 100mV_{pp}$, 1 < f < 40 MHz	40			dB
Output Offset Voltage	V_{OS}	I_{MR} = 13mA, $R_{MR} = 25\Omega$	-150		150	mV
Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} -2.6		V
Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE)			250	mV
Single-Ended Output Resistance	R_{SEO}	Read Mode			50	Ω
Output Current	I_O	AC Coupled Load, RDX to RDY	1.5			mA
MR Head-to-Disk Contact Current	I_{DISK}	Extended Contact, R_{DISK} = 10MΩ			TBD	µA
		Maximum Peak Discharge, C_{DISK} = 300pF, R_{DISK} = 10MΩ			TBD	mA
MR Head Potential, Selected Head	V_{MR}	I_{MR} = 13mA, $R_{MR} = 25\Omega$		325	500	mV

WRITER CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{CC} < 5.5V$, $I_W = 40mA$, $L_H = 200nH$, $R_H = 15\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.0		V
I_{WC} to Write Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = V_{WC} \cdot A_I$	36	40	44	V
Write Current Range	I_W		10		40	mA
Write Current Tolerance	ΔI_W	$10 < I_W < 40$ mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open Head		TBD		V_{pp}
Unselected Head Transition Current	I_{UH}	$I_W = 40mA$			50	μA_{pk}
Differential Output Resistance	R_O	Internal Damping Resistance	200	250	300	Ω
Write Data Frequency for Safe Condition	f_{DATA}	FLT low	1.0			MHz

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0°C < T_A < 80°C$, $4.5V < V_{CC} < 5.5V$, $I_W = 40mA$, $L_H = 200nH$, $R_H = 15\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	To 90% of write current		0.5		µs
R/$\overline{W}$ to Read Mode	t_{WR}	To 90% of envelope; $\overline{RBAW}$ inactive		2		µs
$\overline{CS}$ to Read Mode	t_{CS}	To 90% of envelope		10		µs
HS0 - HS3 to Any Head	t_{HS}	To 90% of envelope; read mode		2		µs
$\overline{CS}$ to Unselect	t_{RI}	To 10% of read envelope or write current			0.5	µs
Safe to Unsafe*	t_{D1}	50% WDP to 50% FLT		0.7	1.5	µs
Unsafe to Safe*	t_{D2}	50% WDP to 50% FLT		0.1	0.3	µs
Head Current Propagation Delay*	t_{D3}	From 50% points			30	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time, $L_H = 0$, $R_H = 0$			0.5	ns
Rise/Fall Time	t_r / t_f	10-90%; $I_W = 40mA$; $L_H = 200nH$, $R_H = 15\Omega$			5.5	ns

*See Figure 1 for write mode timing diagram.

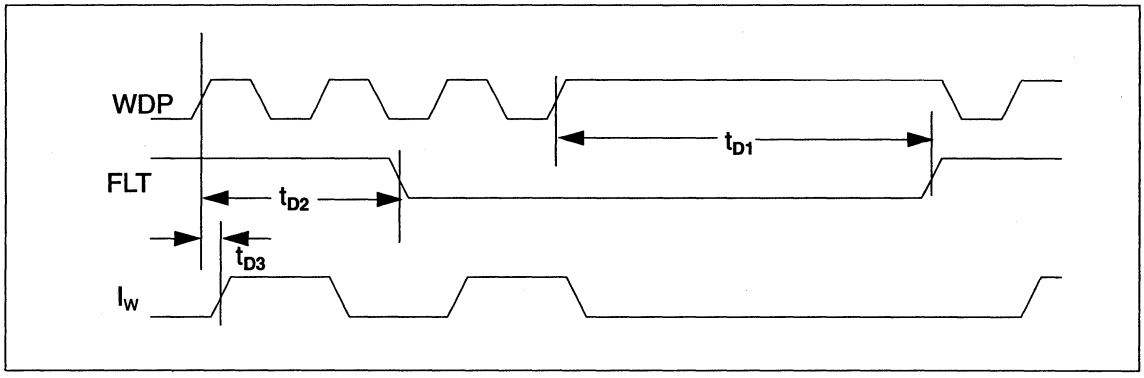
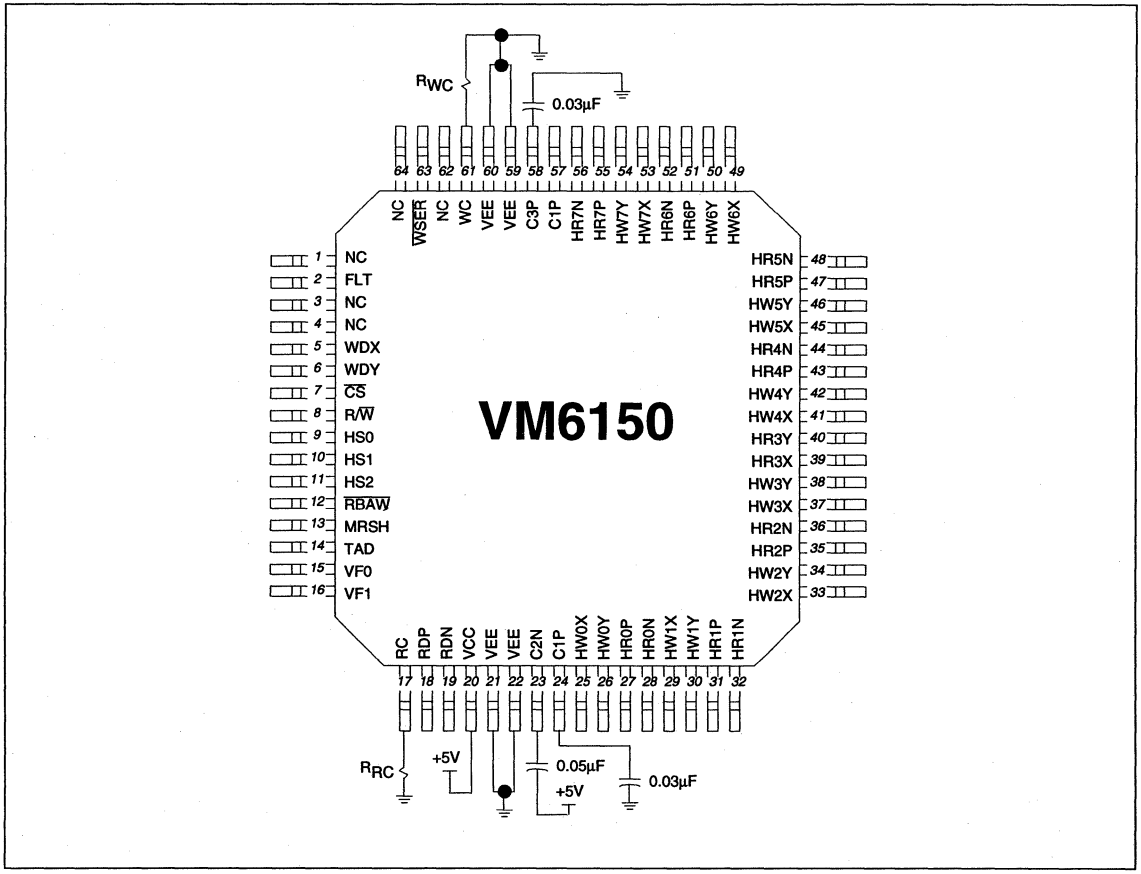


Figure 1: Write Mode Timing Diagram

TYPICAL CONNECTION DIAGRAM



Note 1: I_{RC} = MR Bias Current = $40/R_{RC}$
Note 2: I_{WC} = Write Current = $40/R_{WC}(1+R_H/251)$, R_H = Head Series Resistance
Note 3: V_{CC} = +5V, V_{EE} = GND
Note 4: Pin 57 is connected to pin 24 internally, but external connection is preferred for noise immunity.

2 Two-Terminal Preamplifiers

Two-Terminal High-Performance +5/+12V Read/Write Preamplifiers

VTC Inc.
Value the Customer™

VM312

10-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 150 V/V
  - Low Input Noise = 0.8nV/$\sqrt{Hz}$ Maximum
  - Input Capacitance = 25 pF Maximum
  - Write Current Range = 10 mA to 40 mA
  - Head Inductance Range = 200 nH to 3 µH
  - Head Voltage Swing = 7 Vp-p Minimum
  - Write Current Rise Time = 5 ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Mirror Image Pinout Options Available
- Available in 6, 8, 9 or 10-Channel Options
- Pin-compatible with SSI 32R512

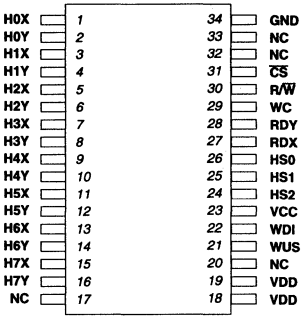
DESCRIPTION

The VM312 is a high-performance, low-power, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for ten channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode.

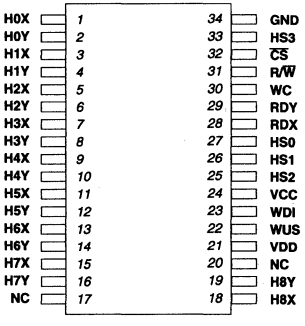
Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400-ohm damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM312 is available in several different packages. Please consult VTC for package availability.

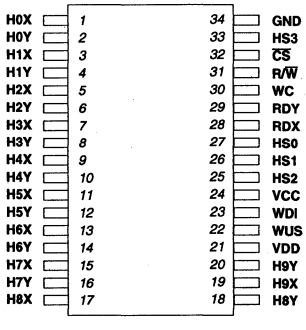
CONNECTION DIAGRAMS



8-Channel
34-lead SOIC



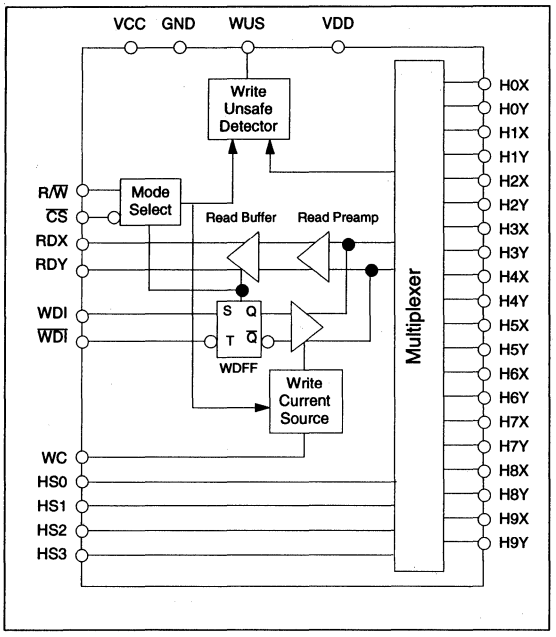
9-Channel
34-lead SOIC



10-Channel
34-lead SOIC

For additional connection diagrams see the last page of this data sheet.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 28-lead SSOP ..... 100°C/W
- 34-lead SOIC ..... 60°C/W
- 36-lead SOIC ..... 80°C/W
- 44-lead PLCC ..... 10°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM312 addresses up to 24 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Table 1. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM312 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the Write Data Flip-Flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The part is also available without the write data flip-flop. In this option the write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM312 because the internal 380Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VM312 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. There is also a mask option to make RDX and RDY open collector outputs. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19
0	0	1	0	1	20
1	0	1	0	1	21
0	1	1	0	1	22
1	1	1	0	1	23

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		47	50	mA
		Write Mode		30	32	
		Idle Mode		1.3	1.5	
VDD Supply Current	I_{DD}	Read Mode		0.8	1.2	mA
		Write Mode		$20 + I_W$	$22 + I_W$	
		Idle Mode		0.83	1	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		270	291	mW
		Write Mode: I_W = 20mA		660	730	
		Idle Mode		18	22	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{\text{WDI}}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{\text{WDI}}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{\text{WDI}}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{\text{WDI}}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VCC Fault Voltage	V_{DDF}		9.5	10	10.5	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} 3.8V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	40	50**		MHz
		-3dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	50	75**		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.52	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz	12	15	18	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	260	550		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	50	60		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	45	50		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45	50		dB
Output Offset Voltage	| V_{OS} |	V_{IN} = 0 on selected head , A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		17	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

** The bandwidth is head dependent due to the capacitive cancellation circuitry. When the preamplifier is used with a head the bandwidth is dominated by the inductance of the head and the input capacitance of the preamplifier even if the LC pole is beyond the amplifier bandwidth as given above.

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0μH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 35mA	9	9.5	10	Vp-p
Unselected Head Current	I_{UH}			0.3	1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			18	22	pF
Differential Output Resistance	R_{OUT}	Without damping resistor	3.2			kΩ
		With damping resistor		400		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.0			MHz
Write Current Range	I_W	1430Ω< R_{WC} < 5kΩ	10		35	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 35mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time	t_r/t_f	(L_H = 1µH)		6.5	9	ns
Rise/Fall Time	t_r/t_f	(L_H = 0µH)		2	5	ns

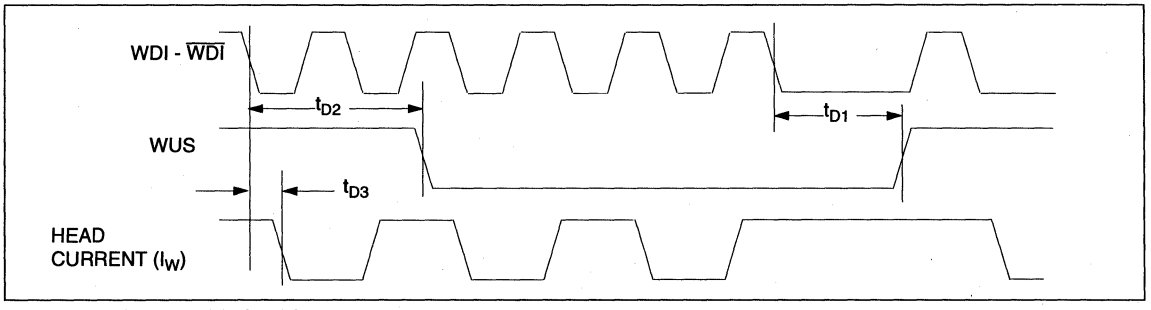
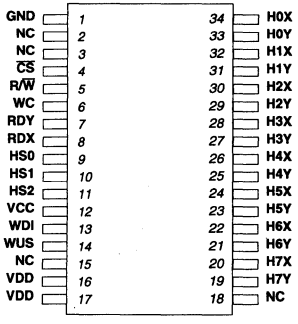
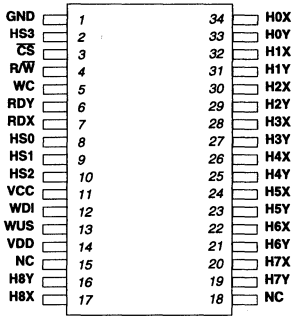


Figure 1: Write Mode Timing Diagram

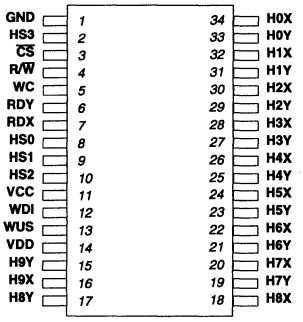
ADDITIONAL CONNECTION DIAGRAMS



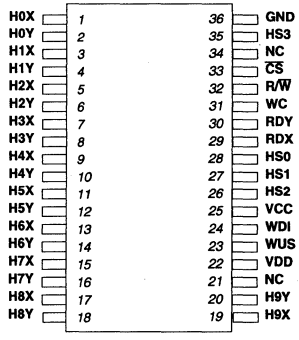
8-Channel
34-lead SOIC
(Mirror Version)



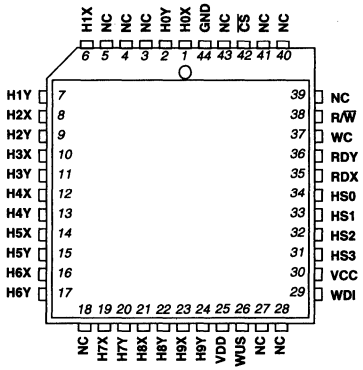
9-Channel
34-lead SOIC
(Mirror Version)



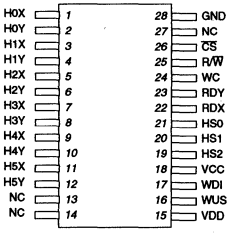
10-Channel
34-lead SOIC
(Mirror Version)



10-Channel
36-lead SOIC



10-Channel
44-lead PLCC



6-Channel
28-lead SSOP

VTC Inc.
Value the Customer™

VM31216

16-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 150 V/V
  - Low Input Noise = 0.85nV/√Hz Maximum
  - Input Capacitance = 25 pF Maximum
  - Write Current Range = 10 mA to 40 mA
  - Head Inductance Range = 200 nH to 3 µH
  - Head Voltage Swing = 7 Vp-p Minimum
  - Write Current Rise Time = 5 ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- TTL Compatible Write Data Input
- Pin-compatible with SSI 32R2015

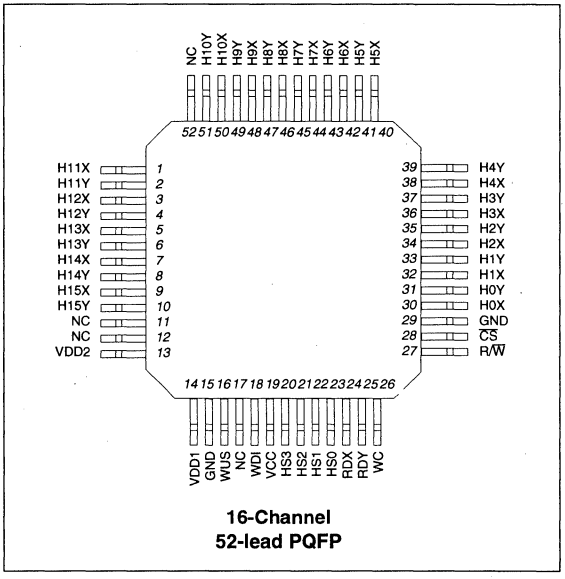
DESCRIPTION

The VM31216 is a high-performance, low-power, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for ten channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode.

Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM31216 is available in a 52-Lead PQFP. Please consult VTC for package availability.

CONNECTION DIAGRAM



16-Channel
52-lead PQFP

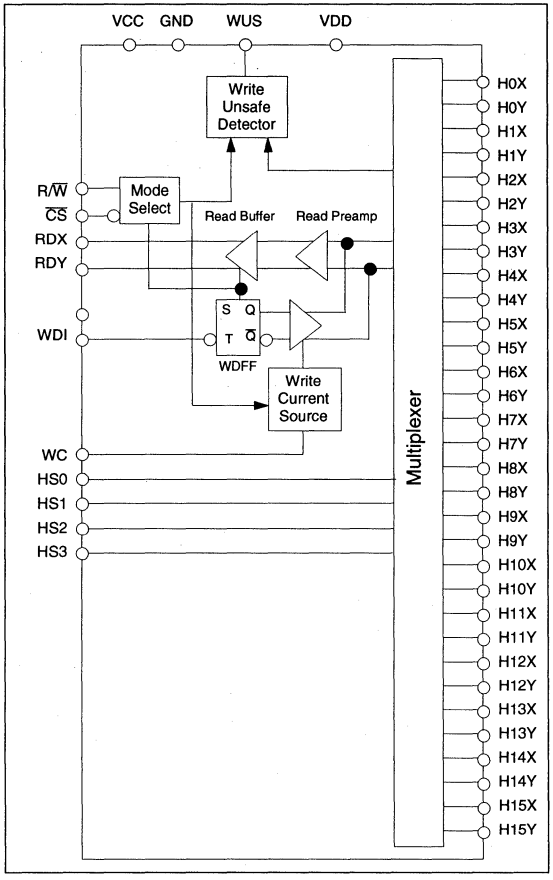
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:	
V_{DD}	-0.3V to +14V
V_{CC}	-0.3V to +7V
Write Current (I_W)	100mA
Input Voltages:	
Digital Input Voltage V_{IN}	-0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H	-0.3V to (V_{DD} + 0.3)V
WUS Pin Voltage Range V_{WUS}	-0.3V to +14V
Output Current:	
RDX, RDY: I_O	-10mA
WUS: I_{WUS}	+12mA
Junction Temperature,	150°C
Storage Temperature Range	-65° to 150°C
Thermal Characteristics, Θ_{JA}:	
52-lead PQFP	70°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:	
V_{DD}	12V ± 10%
V_{CC}	5V ± 10%
Junction Temperature	0°C to 125°C

BLOCK DIAGRAM



CIRCUIT OPERATION

The VM31216 addresses 16 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM31216 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V / R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM31216 because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Read Mode

Read mode configures the VM31216 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry. Multiple devices may have there read outputs wire OR'ed together.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180 mW for a ***sleep mode***.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select

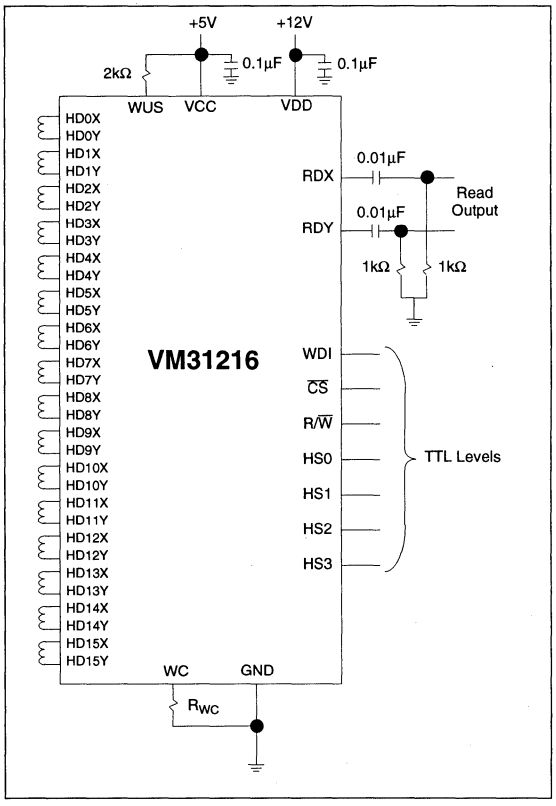
HS0	*HS1*	*HS2*	*HS3*	*HEAD*
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	15

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to 16 heads
H0X - H15X H0Y - H15Y	I/O	X, Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current.
$\overline{CS}$	I	Chip select: low level enables the device
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION



DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4	
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			$30 + I_W$	
		Idle Mode			12	
Power Dissipation ($T_J = 125°C$)	P_D	Read Mode		500	670	mW
		Write Mode: $I_W = 20mA$		625	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	$V_{IL} = 0.8V$	-0.4			mA
Input High Current	I_{IH}	$V_{IH} = 2.0V$			100	µA
WUS Output Low Voltage	V_{OL}	$I_{OL} = 8mA$			0.5	V
VCC Fault Voltage	V_{DDF}		9		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, $0 < V_{CC} \leq 3.5V$, $0 < V_{DD} < 9V$	-200		+200	µA
		Write Mode, $0 < V_{CC} < 5.5V$, $0 < V_{DD} < 13.2V$	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	125		175	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	25			MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.65		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω< R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 600nH, R_H = 20Ω			9	ns

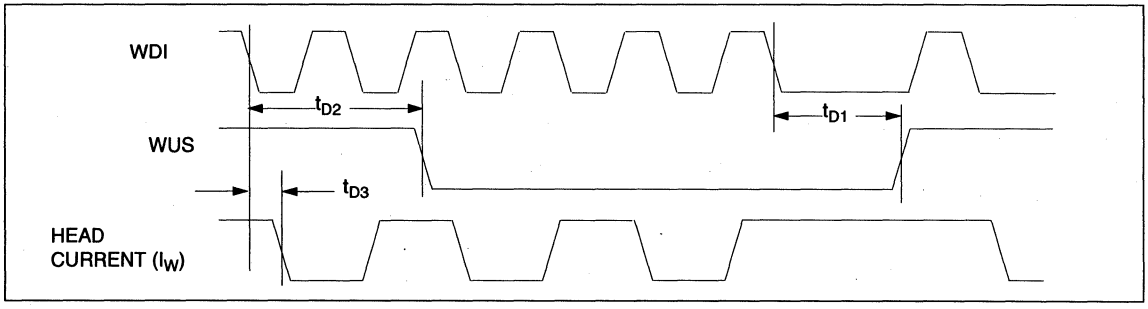


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM312H

14-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 250 V/V
  - Low Input Noise = 0.8nV/√Hz Maximum
  - Input Capacitance = 25 pF Maximum
  - Write Current Range = 10 mA to 40 mA
  - Head Inductance Range = 200 nH to 5 µH
  - Head Voltage Swing = 7 Vp-p Minimum
  - Write Current Rise Time = 5 ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Mirror Image Pinout Options Available
- Pin-compatible with SSI 32R5121

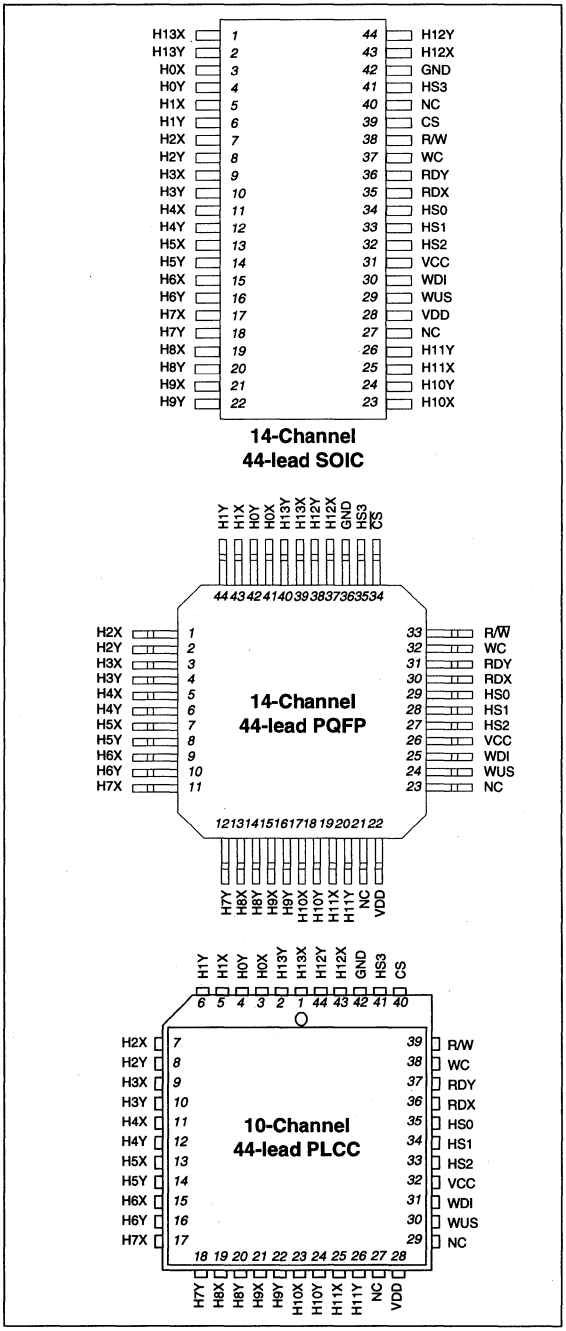
DESCRIPTION

The VM312H is a high-performance, low-power, high-gain, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for fourteen channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode.

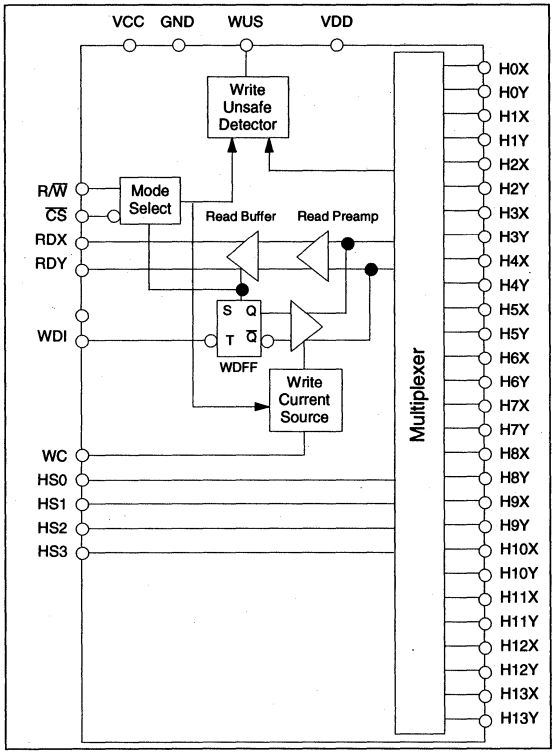
Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode and a suitable damping resistance in the write mode.

The VM312H is available in a variety of package configurations including a mirror-image pinout to facilitate multiple device applications. Channel count options are also available. Please consult VTC for package availability.

CONNECTION DIAGRAMS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{DD} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 44-lead PLCC ..... 10°C/W
- 44-lead PQFP ..... 90°C/W
- 44-lead SOIC ..... 70°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM312H addresses fourteen two-terminal thin-film recording heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM312H as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V / R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM312H because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Read Mode

Read mode configures the VM312H as a low-noise high gain differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180 mW for a ***sleep mode***.

Table 1: Mode Select

R/$\overline{W}$	$\overline{CS}$	MODE
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select

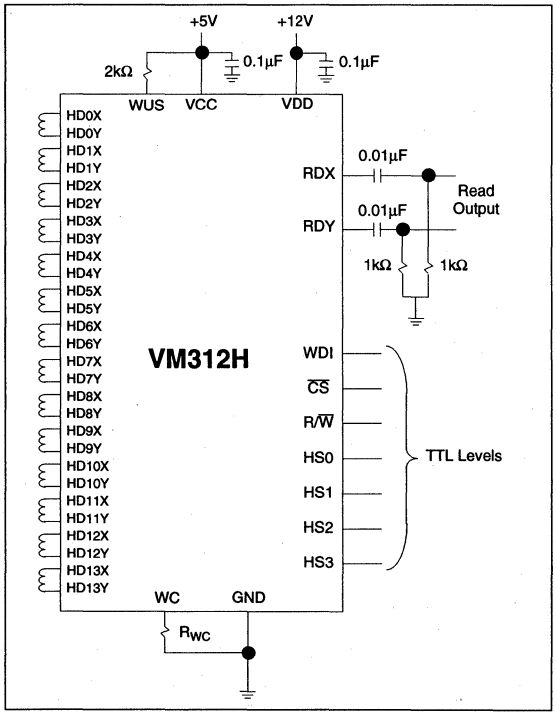
HS0	HS1	HS2	HS3	HEAD
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0 - HS3	I*	Head Select: selects one of up to 14 heads
H0X - H13X H0Y - H13Y	I/O	X, Y Head Terminals
WDI	I*	Write Data Input: a negative transition toggles direction of head current.
$\overline{CS}$	I	Chip select: low level enables the device
R/$\overline{W}$	I*	Read/Write select: high level selects read mode
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION



DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		33	47	mA
		Write Mode		21	27	
		Idle Mode		1.5	4	
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			$30 + I_W$	
		Idle Mode		8	12	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		440	670	mW
		Write Mode: I_W = 20mA		620	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	V_{IL} = 0.8V	-0.4			mA
Input High Current	I_{IH}	V_{IH} = 2.0V			100	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
VCC Fault Voltage	V_{DDF}		9	9.9	10.5	V
VCC Fault Voltage	V_{CCF}		3.5	4.1	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, $0 < V_{CC} \leq 3.5V$, $0 < V_{DD} < 9V$	-200		+200	µA
		Write Mode, $0 < V_{CC} < 5.5V$, $0 < V_{DD} < 13.2V$	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	210	250	290	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	14	40		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	27	55		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	54			dB
Output Offset Voltage	V_{OS}		-400	25	400	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		12	30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.71		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7	7.8		Vp-p
Unselected Head Current	I_{UH}			0.3	1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω < R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8	±1	+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 600nH, R_H = 20Ω			9	ns

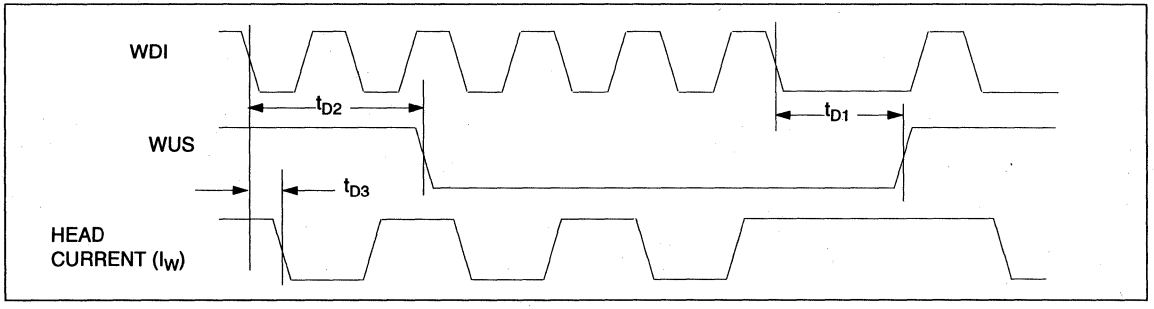


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM313

10-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 150 V/V
  - Low Input Noise = 0.8nV/√Hz Maximum
  - Input Capacitance = 25 pF Maximum
  - Write Current Range = 10 mA to 40 mA
  - Head Inductance Range = 200 nH to 3 µH
  - Head Voltage Swing = 7 Vp-p Minimum
  - Write Current Rise Time = 5 ns
- Differential Pseudo ECL Write Data Input
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Mirror Image Pinout Option Available
- Pin-Compatible with SSI 32R528
- Available in 8, 9 or 10-Channel Options

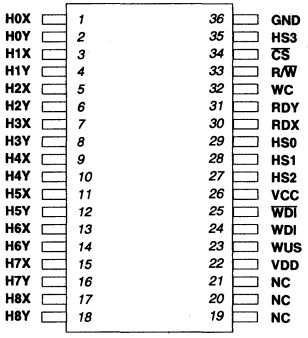
DESCRIPTION

The VM313 is a high-performance, low-power, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for ten channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode.

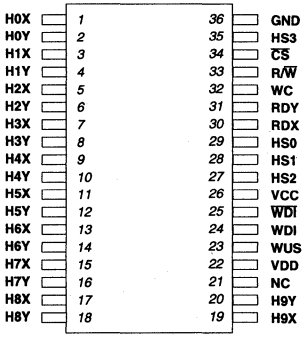
Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM313 is available in a variety of package configurations. Please consult VTC for package availability.

CONNECTION DIAGRAMS

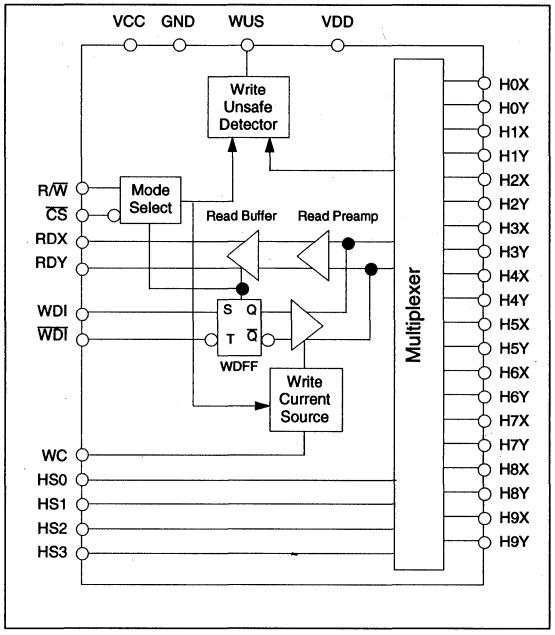


9-Channel
36-lead SOIC



10-Channel
36-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM313 addresses ten two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM313 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM313 because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VM313 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180mW for a ***sleep mode***. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select

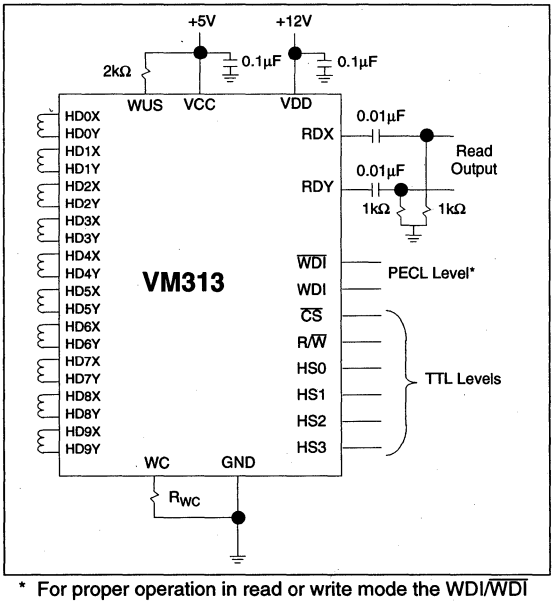
HS0	*HS1*	*HS2*	*HS3*	*HEAD*
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to ten heads
H0X - H9X H0Y - H9Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Input: A negative transition (WDI - $\overline{WDI}$) toggles direction of head current.
$\overline{CS}$	I	Chip select: low level enables the device
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC	*	Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION



* For proper operation in read or write mode the WDI/$\overline{WDI}$ inputs must be correctly biased to their respective PECL levels. They cannot float of both be tied high or low.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4	
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			30 + I_W	
		Idle Mode			12	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		500	670	mW
		Write Mode: I_W = 20mA		625	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-0.4			mA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
VCC Fault Voltage	V_{DDF}		9.0		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} ≤ 3.5V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} < 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	125		175	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	25			MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.65		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω < R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 600nH, R_H = 20Ω			9	ns

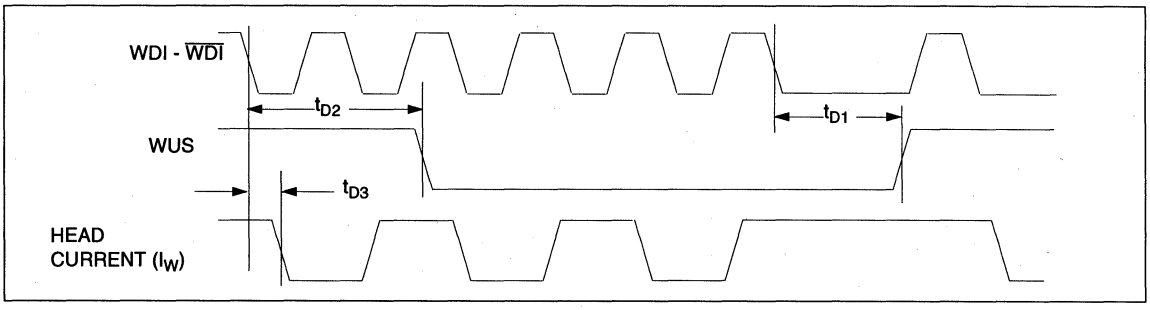


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM31316

16-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 150 V/V
  - Low Input Noise = 0.8nV/√Hz Maximum
  - Input Capacitance = 25 pF Maximum
  - Write Current Range = 10 mA to 40 mA
  - Head Inductance Range = 200 nH to 3 µH
  - Head Voltage Swing = 7 Vp-p Minimum
  - Write Current Rise Time = 5 ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Differential PECL Write Data Inputs
- Pin-compatible with SSI 32R2010

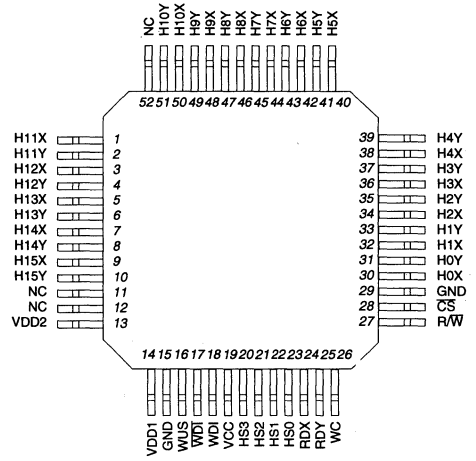
DESCRIPTION

The VM31316 is a high-performance, low-power, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for ten channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode.

Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM31316 is available in a 52-Lead PQFP. Please consult VTC for package availability.

CONNECTION DIAGRAM



16-Channel
52-lead PQFP

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

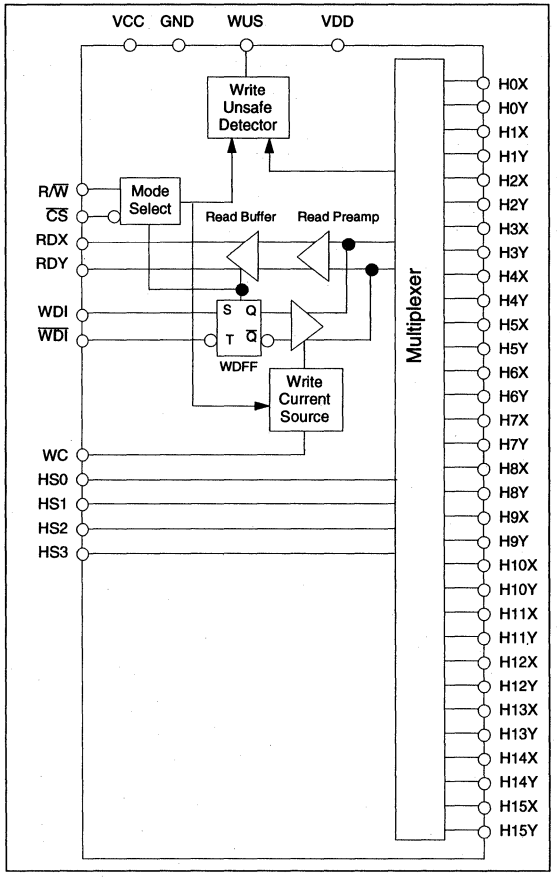
Thermal Characteristics, Θ_{JA}:
- 52-lead PQFP ..... 70°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature .....0°C to 125°C

BLOCK DIAGRAM



CIRCUIT OPERATION

The VM31316 addresses 16 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM31316 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential PECL write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V / R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM31316 because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Read Mode

Read mode configures the VM31316 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry. Multiple devices may have there read outputs wire OR'ed together.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180 mW for a ***sleep mode***..

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select

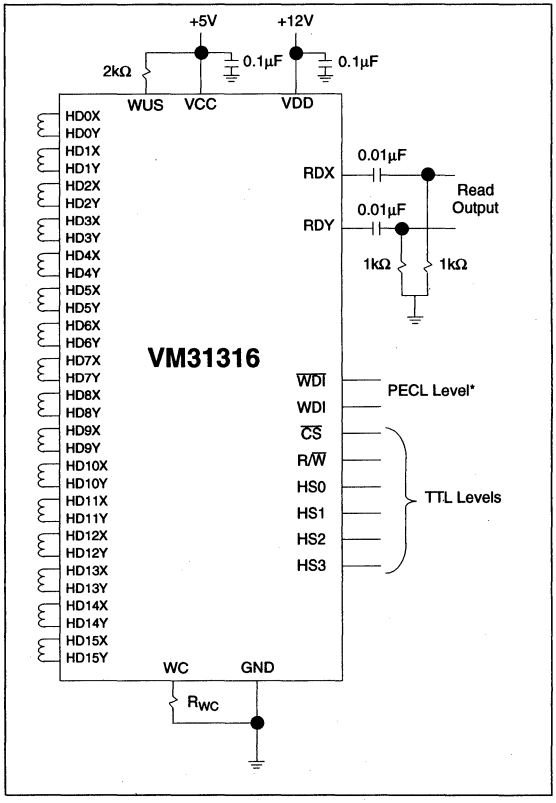
HS0	*HS1*	*HS2*	*HS3*	*HEAD*
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	15

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to 16 heads
H0X - H15X H0Y - H15Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Input: A negative transition (WDI - $\overline{WDI}$) toggles direction of head current.
$\overline{CS}$	I	Chip select: low level enables the device
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION



* For proper operation in read or write mode the WDI/$\overline{WDI}$ inputs must be correctly biased to their respective PECL levels. They cannot float of both be tied high or low.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4	
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			30 + I_W	
		Idle Mode			15	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		500	670	mW
		Write Mode: I_W = 20mA		625	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-0.4			mA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
VCC Fault Voltage	V_{DDF}		9.0		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} ≤ 3.5V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} < 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	125		175	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	25			MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.65		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω< R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 600nH, R_H = 20Ω			9	ns

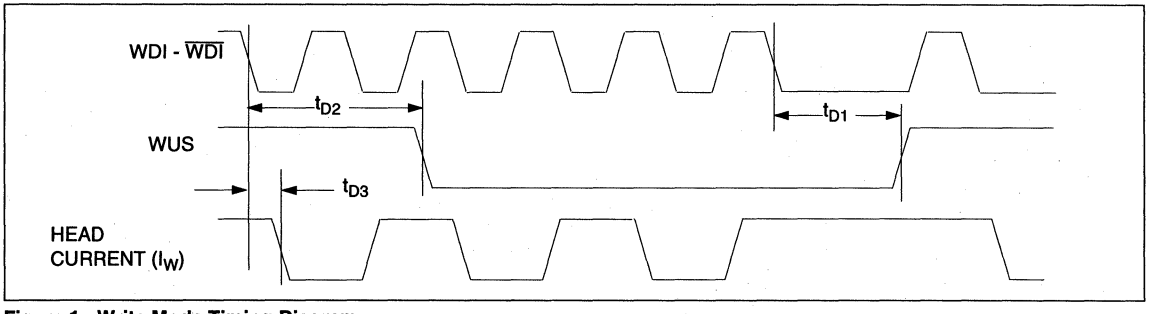


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM313H

14-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 250V/V
  - Low Input Noise = 0.8nV/$\sqrt{Hz}$ Maximum
  - Input Capacitance = 25pF Maximum
  - Write Current Range = 10mA to 40mA
  - Head Inductance Range = 200nH to 3µH
  - Head Voltage Swing = 7Vp-p Minimum
  - Write Current Rise Time = 5ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Differential Pseudo ECL Write Data Input

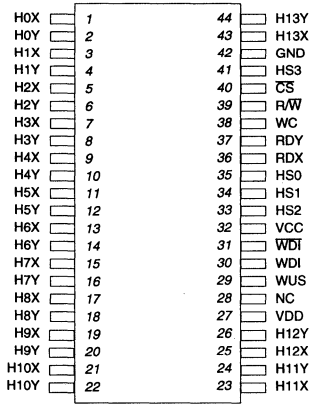
DESCRIPTION

The VM313H is a high-performance, low-power, high gain, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for fourteen channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode. The VM313H features a read mode voltage gain of 250V/V.

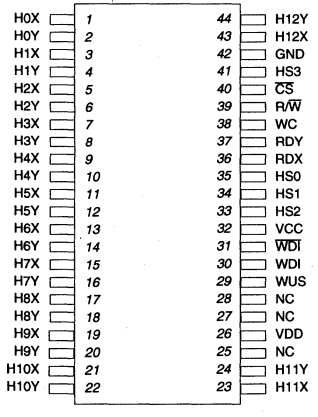
Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM313H is available in a variety of package configurations. Please consult VTC for package availability.

CONNECTION DIAGRAMS

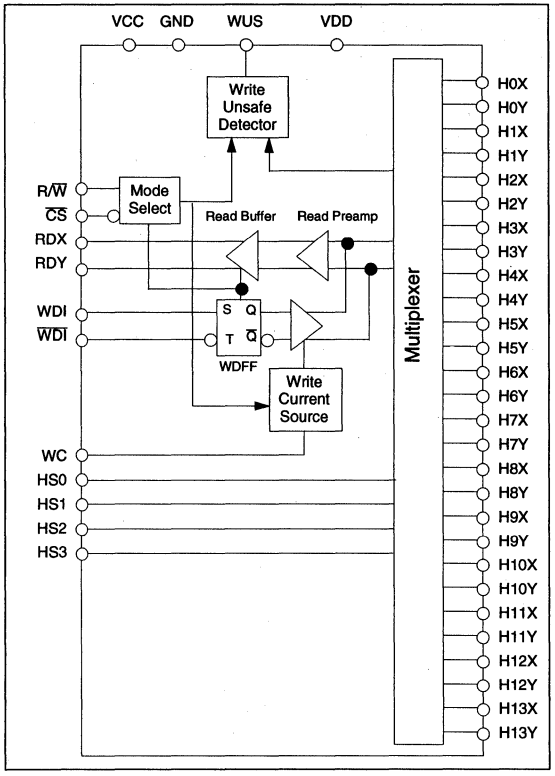


14-Channel
44-lead SOIC



13-Channel
44-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 44-lead SOIC ..... 70°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature .....0°C to 125°C

CIRCUIT OPERATION

The VM313H addresses fourteen two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM313H as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM313H because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Read Mode

Read mode configures the VM313H as a low-noise high gain differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180 mW for a ***sleep mode***.

Table 1: Mode Select

R/$\overline{W}$	$\overline{CS}$	MODE
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select

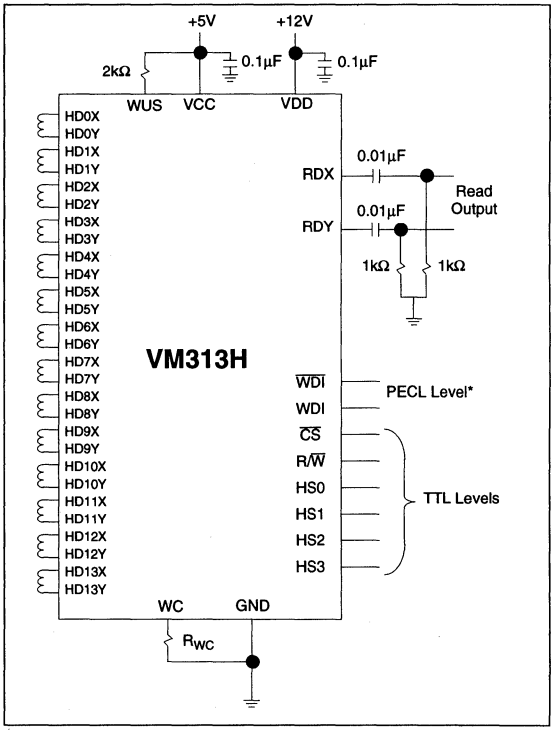
HS0	HS1	HS2	HS3	HEAD
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0 - HS3	I*	Head Select: selects one of up to 14 heads
H0X - H13X H0Y - H13Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Input: A negative transition (WDI - $\overline{WDI}$) toggles direction of head current.
$\overline{CS}$	I	Chip select: low level enables the device
R/$\overline{W}$	I*	Read/Write select: high level selects read moden
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION



* For proper operation in read or write mode the WDI/$\overline{WDI}$ inputs must be correctly biased to their respective PECL levels. They cannot float of both be tied high or low.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4	
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			30 + I_W	
		Idle Mode			12	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		500	670	mW
		Write Mode: I_W = 20mA		625	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-0.4			mA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
VCC Fault Voltage	V_{DDF}		9.0		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} ≤ 3.5V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} < 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	210	250	290	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	25			MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.65		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω < R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 600nH, R_H = 20Ω			9	ns

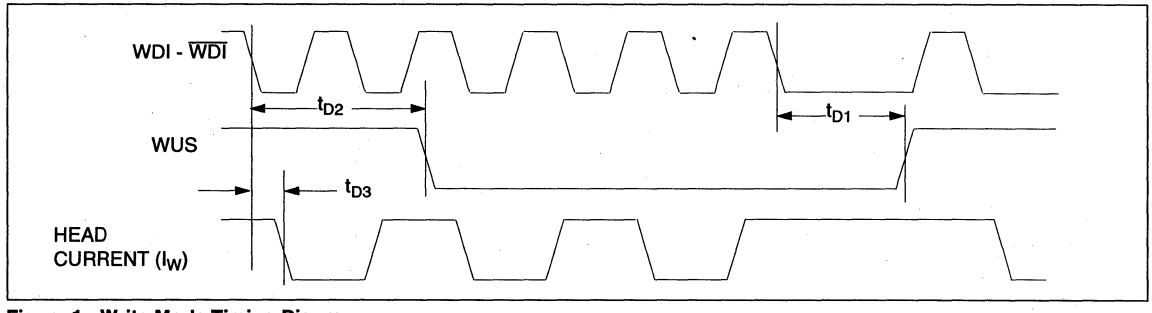


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM313H24

24-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 250V/V
  - Low Input Noise = 0.8nV/$\sqrt{Hz}$ Maximum
  - Input Capacitance = 25pF Maximum
  - Write Current Range = 10mA to 40mA
  - Head inductance Range = 200nH to 3µH
  - Head Voltage Swing = 7Vp-p Minimum
  - Write Current Rise Time = 5ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Differential Pseudo ECL Write Data Input

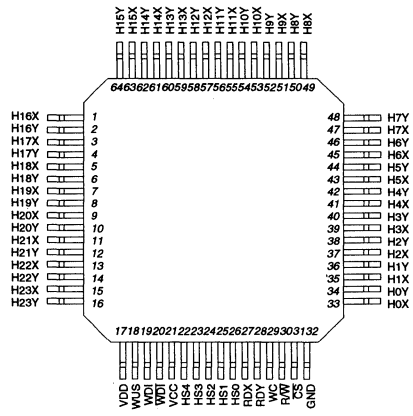
DESCRIPTION

The VM313H24 is a high-performance, low-power, high gain, bipolar monolithic read/write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for 16 to 24 channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode. The VM313H24 features a read mode voltage gain of 250V/V.

Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM313H24 is available in a variety of package configurations. Please consult VTC for package availability.

CONNECTION DIAGRAM



24-Channel
64-lead TQFP

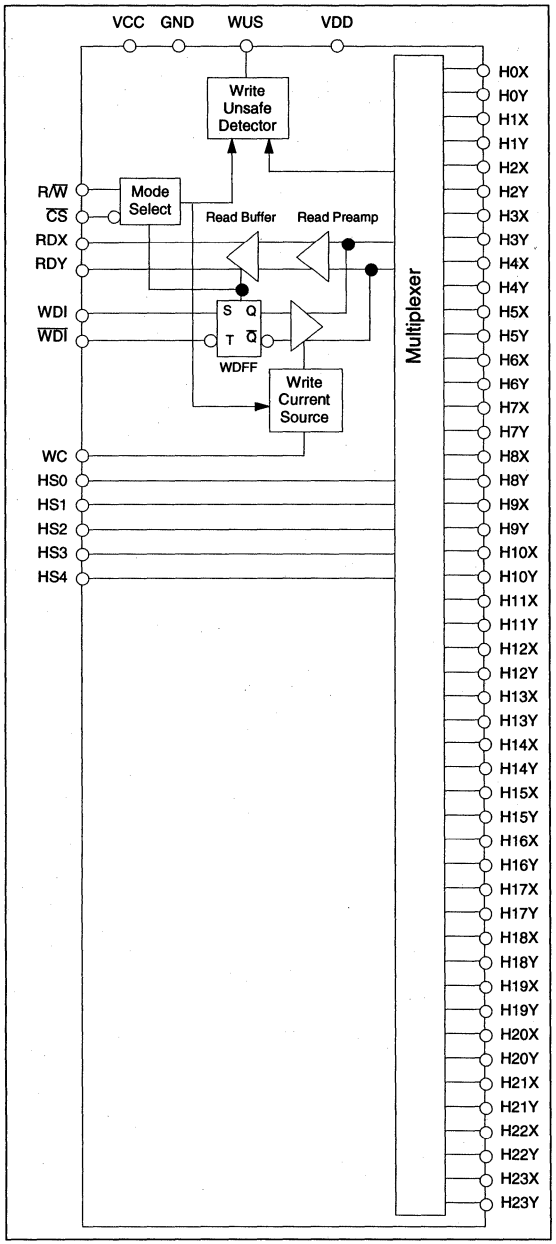
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:	
V_{DD}	-0.3V to +14V
V_{CC}	-0.3V to +7V
Write Current (I_W)	100mA
Input Voltages:	
Digital Input Voltage V_{IN}	-0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H	-0.3V to (V_{DD} + 0.3)V
WUS Pin Voltage Range V_{WUS}	-0.3V to +14V
Output Current:	
RDX, RDY: I_O	-10mA
WUS: I_{WUS}	+12mA
Junction Temperature,	150°C
Storage Temperature Range	-65° to 150°C
Thermal Characteristics, Θ_{JA}:	
64-lead TQFP	60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:	
V_{DD}	12V ± 10%
V_{CC}	5V ± 10%
Junction Temperature	0°C to 125°C

BLOCK DIAGRAM



CIRCUIT OPERATION

The VM313H24 addresses from 16 to 24 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM313H24 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM313H24 because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Read Mode

Read mode configures the VM313H24 as a low-noise high gain differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180 mW for a ***sleep mode***.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select

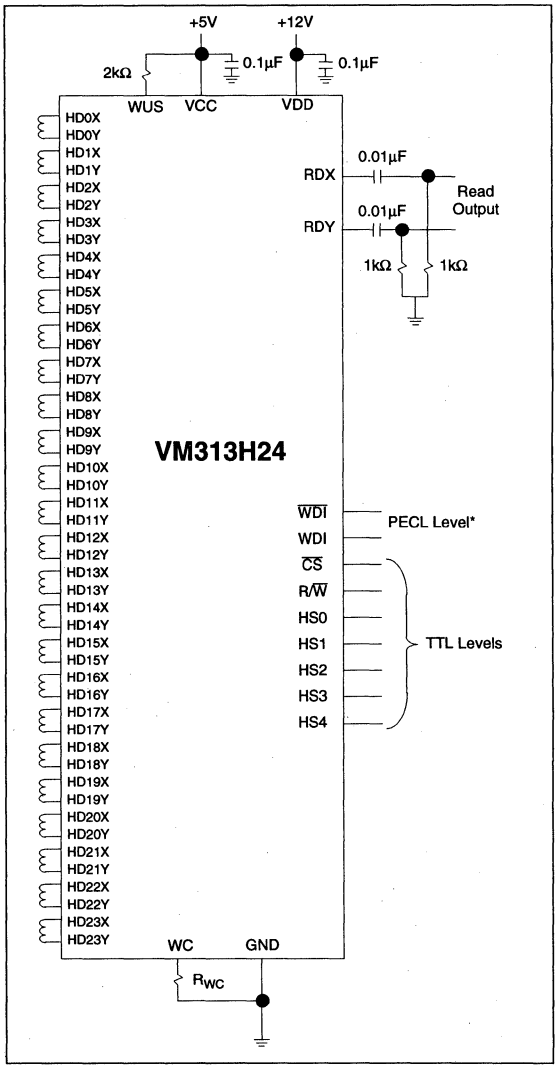
HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19
0	0	1	0	1	20
1	0	1	0	1	21
0	1	1	0	1	22
1	1	1	0	1	23

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS4	I*	Head Select: selects one of up to 24 heads
H0X - H23X H0Y - H23Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Input: A negative transition (WDI - $\overline{WDI}$) toggles direction of head current.
$\overline{CS}$	I	Chip select: low level enables the device
R/$\overline{W}$	I*	Read/Write select: high level selects read moden
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION



* For proper operation in read or write mode the WDI/$\overline{WDI}$ inputs must be correctly biased to their respective PECL levels. They cannot float of both be tied high or low.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4	
VDD Supply Current	I_{DD}	Read Mode			40	mA
		Write Mode			40 + I_W	
		Idle Mode			22	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		500	787	mW
		Write Mode: I_W = 20mA		625	941	
		Idle Mode		105	312	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-0.4			mA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
VCC Fault Voltage	V_{DDF}		9.0		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} ≤ 3.5V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} < 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	210	250	290	V/V
Bandwidth	BW	-1dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	25			MHz
		-3dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.64	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	25	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-400		+400	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.71		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω < R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 600nH, R_H = 20Ω			9	ns

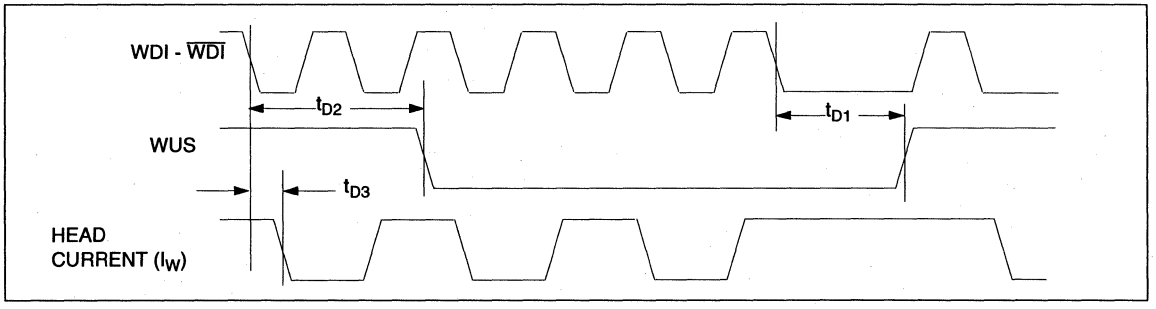


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM313M

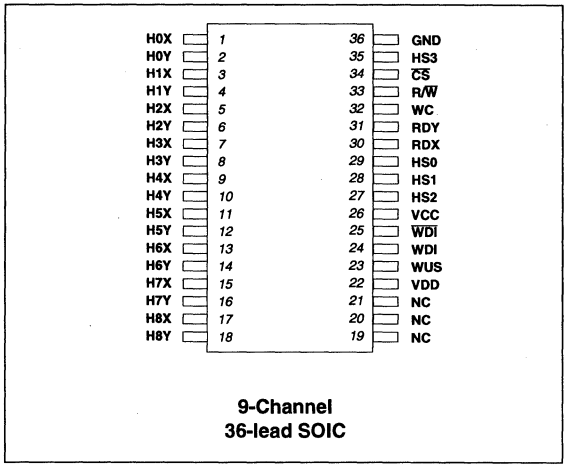
10-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance:
  - Read Mode Gain = 150 V/V
  - Low Input Noise = 0.8nV/$\sqrt{Hz}$ Maximum
  - Input Capacitance = 25 pF Maximum
  - Write Current Range = 5 mA to 40 mA
  - Head Inductance Range = 200 nH to 3 µH
  - Head Voltage Swing = 7 Vp-p Minimum
  - Write Current Rise Time = 5 ns
- Differential Pseudo ECL Write Data Input
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Mirror Image Pinout Option Available
- Pin-Compatible with SSI 32R528
- Available in 8, 9 or 10-Channel Options

CONNECTION DIAGRAM



9-Channel
36-lead SOIC

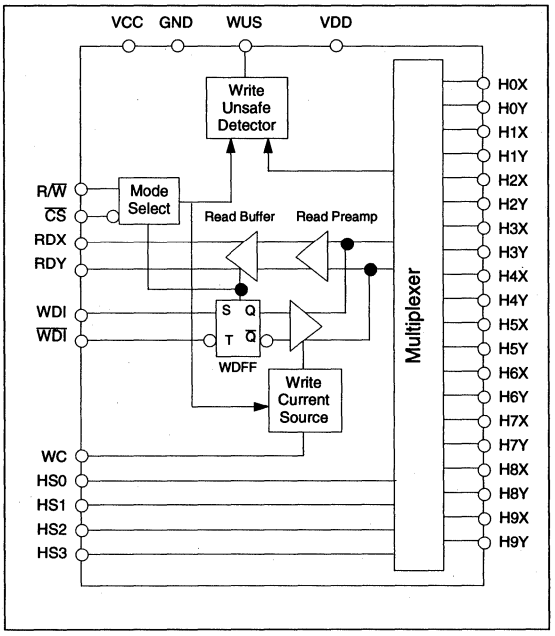
DESCRIPTION

The VM313M is a high-performance, low-power, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for ten channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode.

Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM313M is available in a variety of package configurations. Please consult VTC for package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 32-lead SOIC ..... 55°C/W
- 34-lead SOIC ..... 60°C/W
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM313M addresses ten two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM313M as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM313M because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VM313M as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180mW for a ***sleep mode***. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
X	1	Idle

Table 2: Head Select

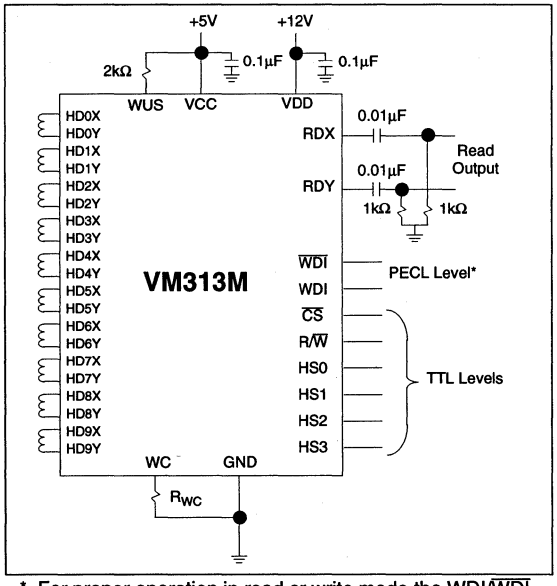
HS0	*HS1*	*HS2*	*HS3*	*HEAD*
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to ten heads
H0X - H9X H0Y - H9Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Input: A negative transition (WDI - $\overline{WDI}$) toggles direction of head current.
$\overline{CS}$	I	Chip select: low level enables the device
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC	*	Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION



* For proper operation in read or write mode the WDI/$\overline{WDI}$ inputs must be correctly biased to their respective PECL levels. They cannot float of both be tied high or low.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4	
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			30 + I_W	
		Idle Mode			12	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		500	670	mW
		Write Mode: I_W = 20mA		625	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-0.4			mA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
VCC Fault Voltage	V_{DDF}		9.0		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} ≤ 3.5V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} < 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	125		175	V/V
Bandwidth	BW	-1dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	25			MHz
		-3dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}			1.65		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω < R_{WC} < 330Ω	5		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, I_W = 20mA, L_H = 600nH, R_H = 20Ω			9	ns

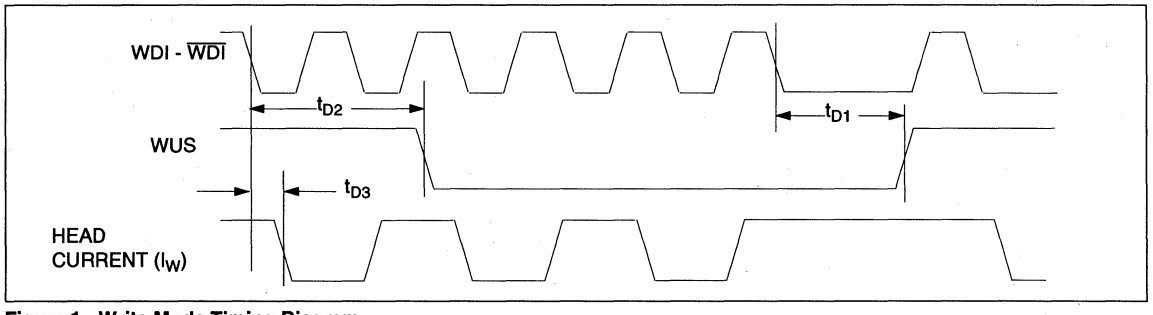


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM5200

10, 14 OR 20-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

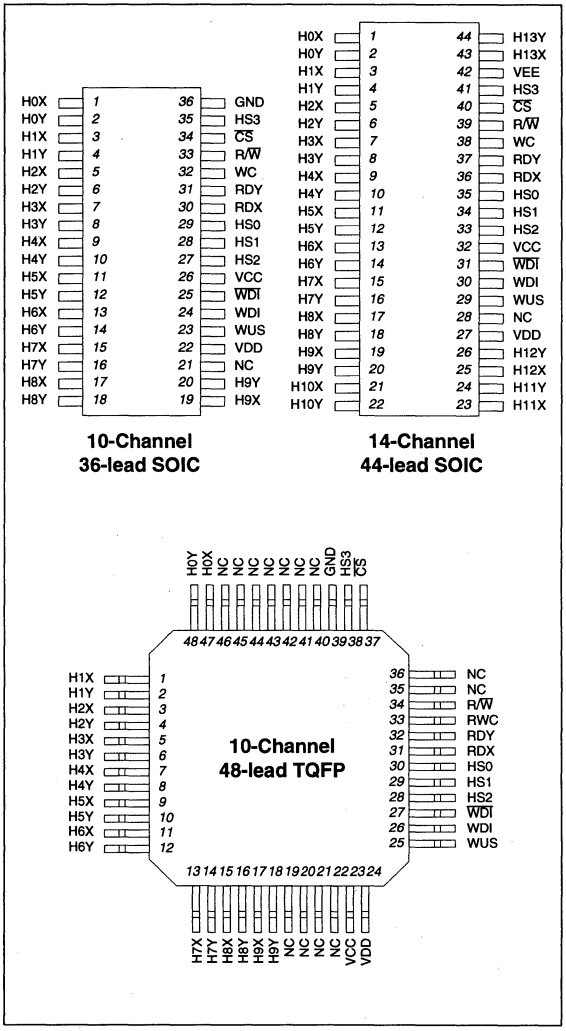
- High Performance
  - Rise/Fall Times = 6.5 ns Typical into 1 μH Head
  - Input Capacitance = 15 pF Typical
  - Input Noise = 0.52 nV/√Hz Typical
  - Head Inductance Range = 0.2 – 1.5 μH
  - Voltage Gain = 150 V/V - Other Options Available
- PECL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V
- Power Supply Fault Protection
- Options Available
  - WDFF on the Write Data Inputs Connected or Disconnected
- Available With up to 20-Channels, Consult VTC for Other Options

DESCRIPTION

The VM5200 is a high-performance, integrated read/write preamplifier designed for use with two-terminal, thin-film recording heads. The circuit contains read amplifiers and write drivers to address up to 20-channels. Internal damping resistors provide different values of damping resistance between the read mode and write modes. When deselected, the circuit enters a low-power sleep mode. Current gain in the write mode is 20 and it is DAC or resistor-controllable. The power supply fault detect circuit shuts off write current in the event the power supply level drops below a unsafe threshold, thus protecting the data on the disk from any potential transients. If a line should open up, the mode select lines ($\overline{CS}$ and R/$\overline{W}$) have internal pullup resistors to ensure the select lines will be forced into a high state to prevent the device from affecting data on the disk.

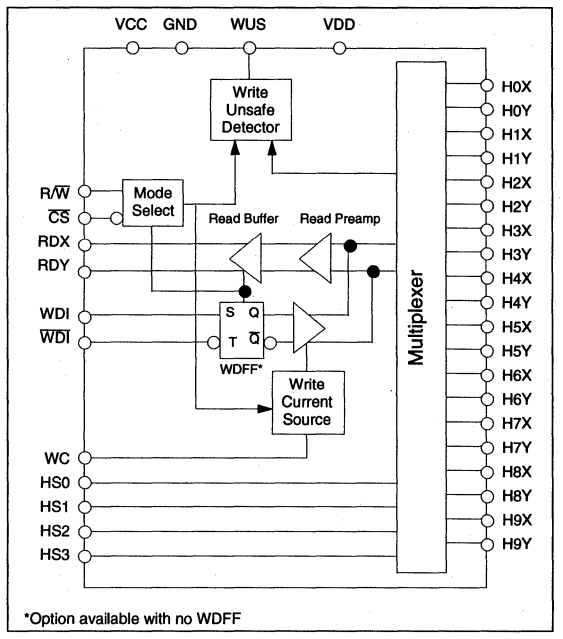
The VM5200 is available in a variety package options. Please consult VTC for package availability.

CONNECTION DIAGRAMS



For additional connection diagrams see the last page of this data sheet.

BLOCK DIAGRAM



*Option available with no WDFF

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ...150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 36-lead SOIC ..... 80°C/W
- 44-lead SOIC ..... 70°C/W
- 48-lead TQFP ..... 80°C/W
- 64-lead TQFP ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM5200 addresses up to 20 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Table 1. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM5200 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the Write Data Flip-Flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The part is also available without the write data flip-flop. In this option the write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM5200 because the internal 380Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VM5200 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load.

There is also a mask option to make RDX and RDY open collector outputs. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		47	52	mA
		Write Mode		26	32	
		Idle Mode		1.1	1.5	
VDD Supply Current	I_{DD}	Read Mode		0.6	1.6	mA
		Write Mode		$18 + I_W$	$24 + I_W$	
		Idle Mode		0.6	1.5	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		242	307	mW
		Write Mode: I_W = 20mA		586	757	
		Idle Mode		12.7	28	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{\text{WDI}}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{\text{WDI}}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{\text{WDI}}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{\text{WDI}}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VDD Fault Voltage	V_{DDF}		9.5	10	10.5	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, $0 < V_{CC} < 3.8V$, $0 < V_{DD} < 9V$	-200		+200	µA
		Read/Idle Mode, $0 < V_{CC} < 5.5V$, $0 < V_{DD} < 13.2V$	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	40	50**		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	50	75**		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.52	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz	12	15	18	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	380	650		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	8		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	50	60		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	45	80		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45	55		dB
Output Offset Voltage	| V_{OS} |	V_{IN} = 0 on selected head, A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		17	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

** The bandwidth is head dependent due to the capacitive cancellation circuitry. When the preamplifier is used with a head the bandwidth is dominated by the inductance of the head and the input capacitance of the preamplifier even if the LC pole is beyond the amplifier bandwidth as given above.

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0μH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 35mA	9	9.5	10	Vp-p
Unselected Head Current	I_{UH}			0.3	1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			18	22	pF
Differential Output Resistance	R_{OUT}	Without damping resistor	3.2			kΩ
		With damping resistor		400		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.0			MHz
Write Current Range	I_W	1430Ω< R_{WC} < 5kΩ	10		35	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 35mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time	t_r/t_f	(L_H = 1µH)		7	9	ns
Rise/Fall Time	t_r/t_f	(L_H = 0µH)		2	5	ns

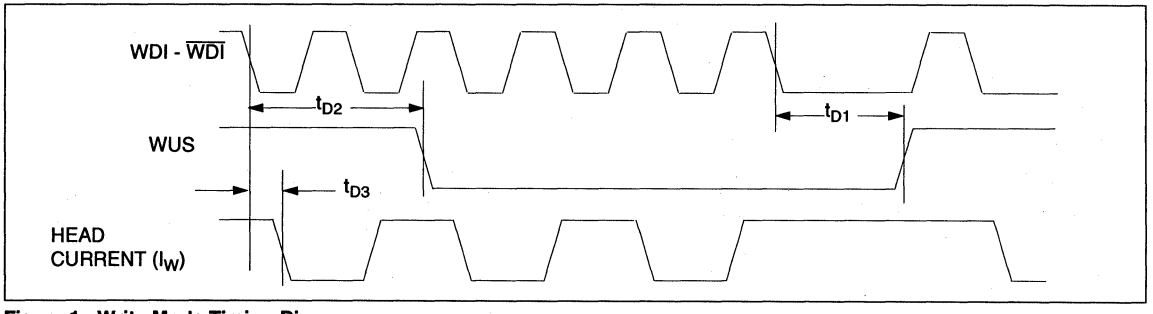
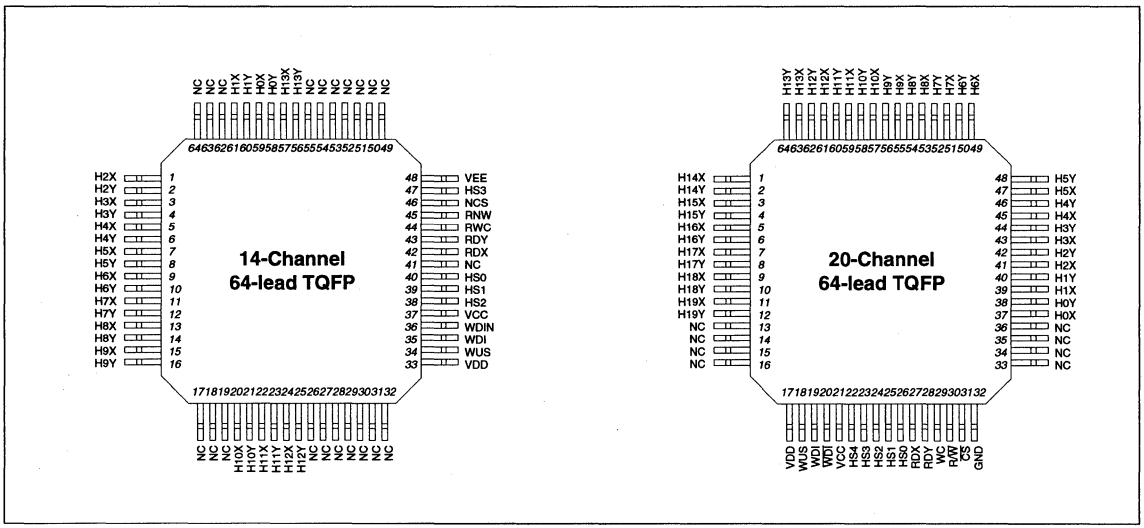


Figure 1: Write Mode Timing Diagram

ADDITIONAL CONNECTION DIAGRAMS



VTC Inc.
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VM5200M

10 OR 20-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

PRELIMINARY

August, 1994

FEATURES

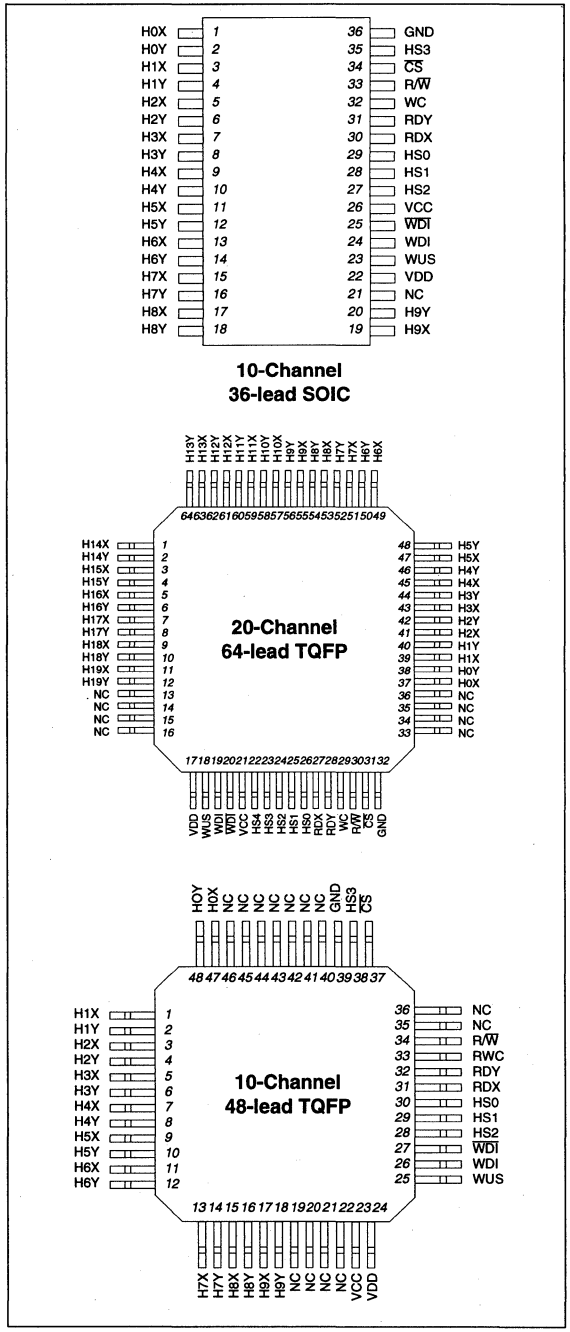
- High Performance
  - Rise/Fall Times = 6.5 ns Typical into 1 µH Head
  - Input Capacitance = 10 pF Typical
  - Input Noise = 0.52 nV/√Hz Typical
  - Head Inductance Range = 0.2 – 1.5 µH
  - Voltage Gain = 150 V/V - Other Options Available
- PECL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V
- Power Supply Fault Protection
- Options Available
  - WDFF on the Write Data Inputs Connected or Disconnected

DESCRIPTION

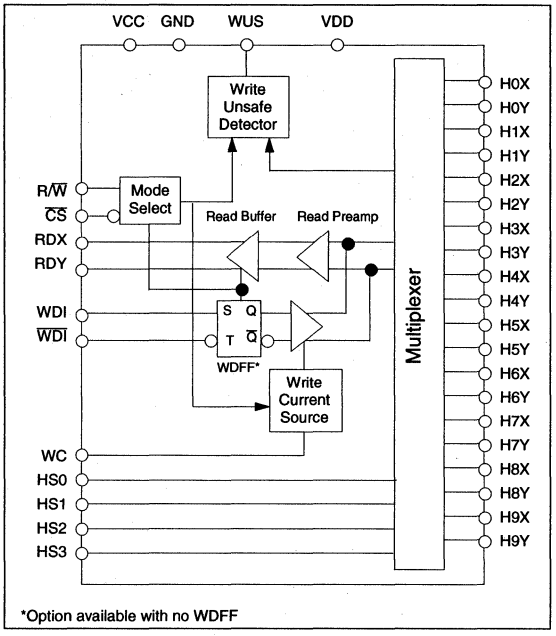
The VM5200M is a high-performance, integrated read/write preamplifier designed for use with two-terminal, thin-film recording heads. The circuit contains read amplifiers and write drivers to address up to 20-channels. Internal damping resistors provide different values of damping resistance between the read mode and write modes. When deselected, the circuit enters a low-power sleep mode. Current gain in the write mode is 20 and it is DAC or resistor-controllable. The power supply fault detect circuit shuts off write current in the event the power supply level drops below a unsafe threshold, thus protecting the data on the disk from any potential transients. If a line should open up, the mode select lines ($\overline{CS}$ and R/$\overline{W}$) have internal pullup resistors to ensure the select lines will be forced into a high state to prevent the device from affecting data on the disk.

The VM5200M is available in a variety package options. Please consult VTC for package availability.

CONNECTION DIAGRAMS



BLOCK DIAGRAM



*Option available with no WDFF

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 36-lead SOIC ..... 80°C/W
- 48-lead TQFP ..... 80°C/W
- 64-lead TQFP ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM5200M addresses up to 20 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Table 1. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM5200M as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the Write Data Flip-Flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The part is also available without the write data flip-flop. In this option the write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM5200M because the internal 380Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VM5200M as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load.

There is also a mask option to make RDX and RDY open collector outputs. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		47	50	mA
		Write Mode		30	32	
		Idle Mode		1.3	1.5	
VDD Supply Current	I_{DD}	Read Mode		0.8	1.2	mA
		Write Mode		20 + I_W	22 + I_W	
		Idle Mode		0.83	1	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		270	291	mW
		Write Mode: I_W = 20mA		660	730	
		Idle Mode		18	22	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	V_{IL} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VCC Fault Voltage	V_{DDF}		9.5	10	10.5	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} 3.8V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	40	50**		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	50	75**		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.52	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		10	14	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	260	550		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	50	60		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	45	50		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45	50		dB
Output Offset Voltage	$\|V_{OS}\|$	V_{IN} = 0 on selected head, A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		17	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

** The bandwidth is head dependent due to the capacitive cancellation circuitry. When the preamplifier is used with a head the bandwidth is dominated by the inductance of the head and the input capacitance of the preamplifier even if the LC pole is beyond the amplifier bandwidth as given above.

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 35mA	9	9.5	10	Vp-p
Unselected Head Current	I_{UH}			0.3	1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			18	22	pF
Differential Output Resistance	R_{OUT}	Without damping resistor	3.2			kΩ
		With damping resistor		400		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.0			MHz
Write Current Range	I_W	1430Ω< R_{WC} < 5kΩ	10		35	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 35mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time	t_r/t_f	(L_H = 1µH)		6.5	9	ns
Rise/Fall Time	t_r/t_f	(L_H = 0µH)		2	5	ns

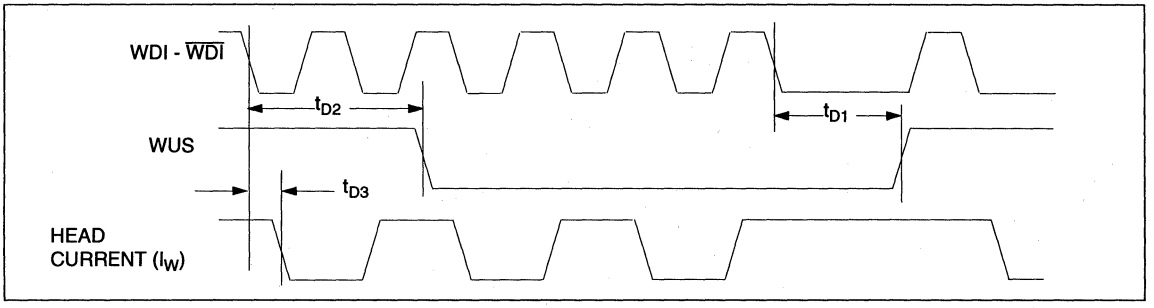


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM522015C

20-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August,1994

FEATURES

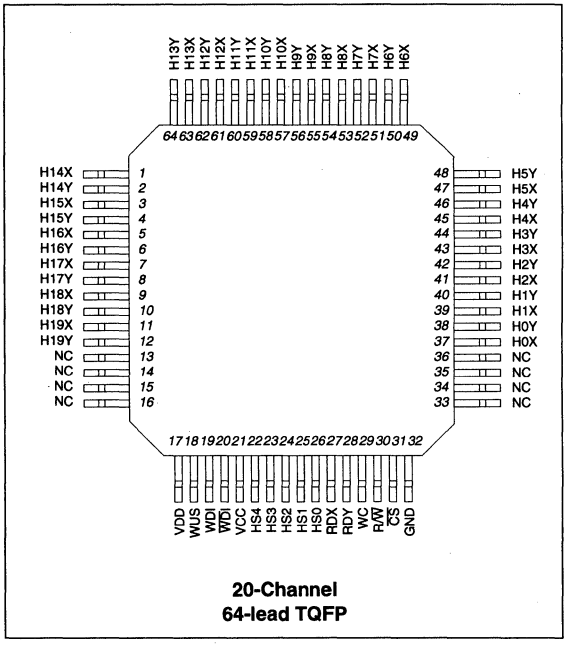
- High Performance
  - Rise/Fall Times = 4 ns Typical into 600 nH Head
  - Input Capacitance = 10 pF Typical
  - Input Noise = 0.65 nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 400 - 800 nH
  - Voltage Gain = 150 V/V
- PECL Write Data Lines
- Write Current Range 5 – 25 mA
- Operates From +5V/+12V
- Power Supply Fault Protection
- 400Ω Schottky Damping Resistor

DESCRIPTION

The VM522015C is a high-performance, integrated read/write preamplifier designed for use with two-terminal, thin-film recording heads. The circuit contains read amplifiers and write drivers to address 20-channels. Internal damping resistors provide different values of damping resistance between the read mode and write modes. When deselected, the circuit enters a low-power sleep mode. Current gain in the write mode is 20 and it is DAC or resistor-controllable. The power supply fault detect circuit shuts off write current in the event the power supply level drops below a unsafe threshold, thus protecting the data on the disk from any potential transients. If a line should open up, the mode select lines ($\overline{CS}$ and R/$\overline{W}$) have internal pullup resistors to ensure the select lines will be forced into a high state to prevent the device from affecting data on the disk.

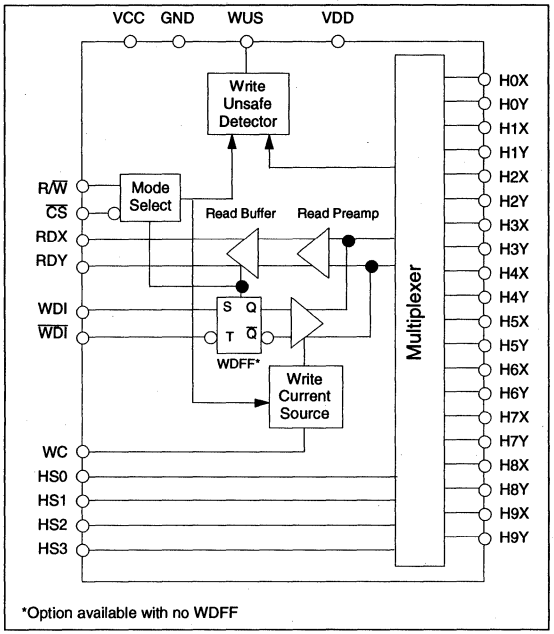
The VM522015C is available in a variety package options. Please consult VTC for package availability.

CONNECTION DIAGRAM



20-Channel
64-lead TQFP

BLOCK DIAGRAM



*Option available with no WDFF

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65°C to 150°C

Thermal Characteristics, Θ_{JA}:
- 64-lead TQFP ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} ..... 12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM522015C addresses 20 two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM522015C as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The part is also available without the write data flip-flop. In this option the write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM522015C because the internal 380Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VM522015C as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load.

There is also a mask option to make RDX and RDY open collector outputs. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		47	60	mA
		Write Mode		30	35	
		Idle Mode		1.3	2.6	
VDD Supply Current	I_{DD}	Read Mode		0.8	1.5	mA
		Write Mode		20 + I_W	29 + I_W	
		Idle Mode		0.83	1.4	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		270	370	mW
		Write Mode: I_W = 20mA		660	750	
		Idle Mode		18	33	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	V_{IL} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VCC Fault Voltage	V_{DDF}		9.5	10	10.5	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} 3.8V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	40	50**		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz	65	75**		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.80	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		10	13	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	260	550		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	60			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	55	65		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	45	50		dB
Output Offset Voltage	| V_{OS} |	V_{IN} = 0 on selected head, A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		17	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

** The bandwidth is head dependent due to the capacitive cancellation circuitry. When the preamplifier is used with a head the bandwidth is dominated by the inductance of the head and the input capacitance of the preamplifier even if the LC pole is beyond the amplifier bandwidth as given above.

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 600nH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 25mA	9	9.5	10	Vp-p
Unselected Head Current	I_{UH}			0.3	1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			15	18	pF
Differential Output Resistance	R_{OUT}			400		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.0			MHz
Write Current Range	I_W	10kΩ > R_{WC} > 2kΩ	5		25	mA
Write Current Tolerance	ΔI_W	I_W range 5mA to 25mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 600nH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time	t_r/t_f	L_H = 600nH		4	5.5	ns
Rise/Fall Time	t_r/t_f	L_H = 0µH		2	5	ns

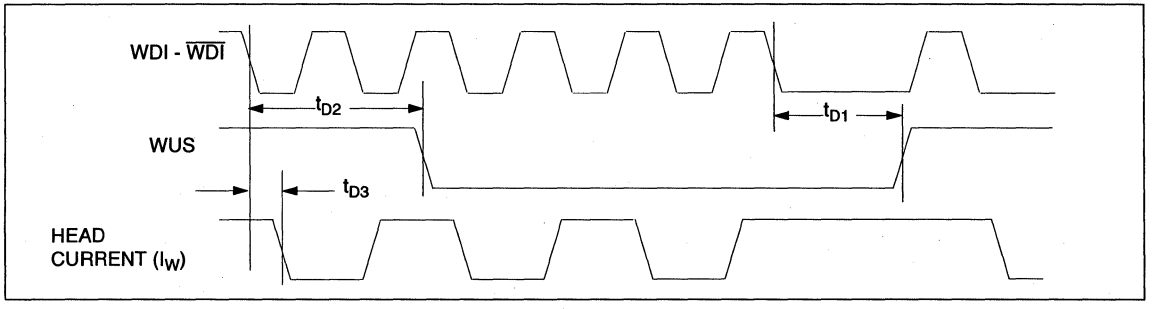


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM52510

10-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH SERVO WRITE

ADVANCE INFORMATION August, 1994

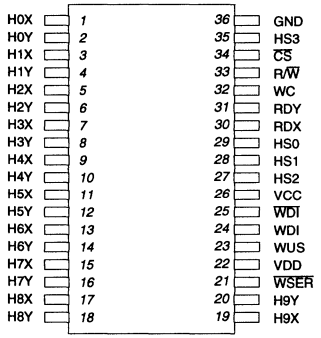
FEATURES

- High Performance
  - Rise/Fall Times = 4.0 ns Typical into 0.5 µH
  - Input Capacitance = 13 pF Typical
  - Input Noise = 0.52 nV/√Hz Typical
  - Head Inductance Range = 0.2 – 1.5 µH Optimized for 0.5µH
  - Voltage Gain = 150 V/V
- PECL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V and +5V/+7V in Servo Mode
- Power Supply Fault Protection
- Servo Write All 10-Channels or Banks of Five Option

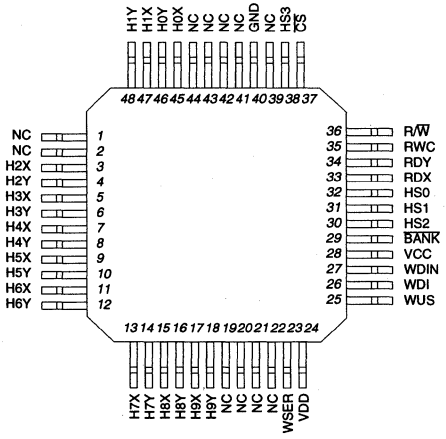
DESCRIPTION

The VM52510 is a high-performance, integrated read/write preamplifier designed for use with two-terminal, thin-film recording heads. The circuit contains read amplifiers and write drivers to address ten channels. Internal damping resistors provide different values of damping resistance between the read mode and write modes. When deselected, the circuit enters a low-power sleep mode. Current gain in the write mode is 20 and it is DAC or resistor-controllable. The power supply fault detect circuit shuts off write current in the event the power supply level drops below a unsafe threshold, thus protecting the data on the disk from any potential transients. If a line should open up, the mode select lines ($\overline{CS}$ and R/$\overline{W}$) have internal pullup resistors to ensure the select lines will be forced into a high state to prevent the device from affecting data on the disk.

CONNECTION DIAGRAMS

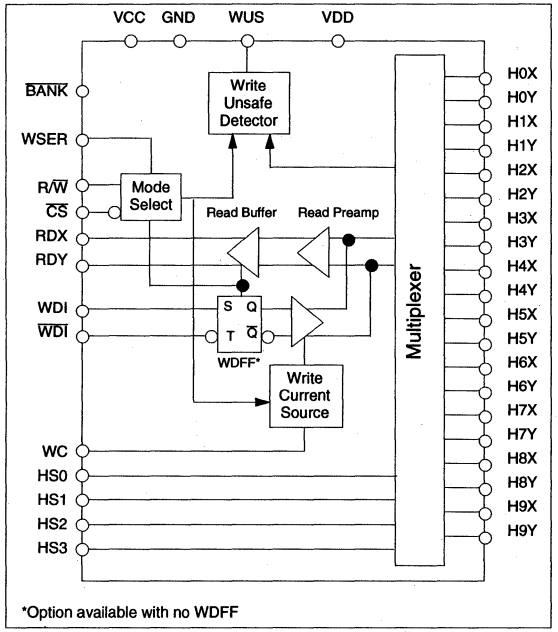


10-Channel
36-lead SOIC



10-Channel
48-lead TQFP

BLOCK DIAGRAM



*Option available with no WDFF

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ...150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 36-lead SOIC ..... 80°C/W
- 48-lead TQFP ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM52510 addresses up to ten two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM52510 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The part is also available without the write data flip-flop. In this option the write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM52510 because the internal 350Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device in servo mode (applicable when WUS is not used for servo selection)
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Write Servo Mode

In this mode, the operation is the same as described above except that ten channels are written at the same time. Two options are available for servo mode control. The first is to use pin WSER to control when the device is in servo mode. The second option is to use the WUS external resistor to control servo mode. In either case servo mode must be preceded by lowering VDD to 7V ±10%. To select servo using the WUS resistor the following procedure is used:

1. Lower VDD to 7V ±10%
2. Enter read mode via R/$\overline{W}$ high
3. WUS pull-up resistor should be tied at least 1.3V above VCC.

The device is now in servo mode will all ten heads writing at the same time. To return to normal operations the following sequence is used:

1. Enter read mode
2. Return WUS resistor to VCC
3. Raise VDD supply back to 12V ±10%
4. Drop the R/$\overline{W}$ line low

For bank servo select of five channels at a time. A bond option exists for pin $\overline{BANK}$ which can be used to select servo head 0 - 4 and heads 5 - 9. $\overline{BANK}$ low puts the VM52510 into bank select mode and HS0 is used to select which bank (0 - 4) or (5 - 9) is active. This mode of selection is applicable to either servo selection scheme (using WUS resistor or WSER pin). Pin WSER goes low to enable the servo write feature.

Upon entering write servo mode the VDD fault level will be lowered to a 5.8V threshold.

Read Mode

Read mode configures the VM5210 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		TBD	TBD	mA
		Write Mode		TBD	TBD	
		Idle Mode		TBD	TBD	
VDD Supply Current	I_{DD}	Read Mode		TBD	TBD	mA
		Write Mode		TBD	TBD	
		Idle Mode		TBD	TBD	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		TBD	TBD	mW
		Write Mode: I_W = 20mA		TBD	TBD	
		Idle Mode		TBD	TBD	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VCC Fault Voltage	V_{DDF}		9.5	10	10.5	V
VDD Servo Mode Fault	V_{DDFS}		5.5	5.8	6.1	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} 3.8V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} 5.5V, 0< V_{DD} < 13.2V	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz		50		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz		75		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.52	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		13	18	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	380	750		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	50	60		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	45	50		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz , Selected Channels V_{IN} = 0mVp-p	45	50		dB
Output Offset Voltage	| V_{OS} |	V_{IN} = 0 on selected head , A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 0.5µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 35mA	9	9.5	10	Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			18	22	pF
Differential Output Resistance	R_{OUT}	Without damping resistor	3.2			kΩ
		With damping resistor		350		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.0			MHz
Write Current Range	I_W	1430Ω < R_{WC} < 5kΩ	10		35	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 35mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 0.5µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.3	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.5	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time*	t_r/t_f	L_H = 0.5µH, I_W = 20mA		4		ns
Rise/Fall Time	t_r/t_f	(L_H = 0µH)		TBD		ns

*Rise/Fall time might vary according to customer rise fall/settle time trade off. Rise/Fall time and settle time will be selected for maximum bit cell.

WRITE SERVO CHARACTERISTICS

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Current	I_{CC}	Servo Mode		TBD		mA
VDD Supply Current	I_{DD}	Servo Mode, V_{DD} = 7V ±10%		TBD		mA
Power Dissipation	P_D	Servo Mode @ I_W = 15mA		TBD		W
Servo Write Current Tolerance			-10		+10	%
Servo Write Current Range			5		15	mA
Rise/Fall Time		L_H = 0.5µH, I_W = 15mA		7		ns
Asymmetry		L_H = 0, R_H = 0			0.5	ns
WDI Input			1		15	MHz

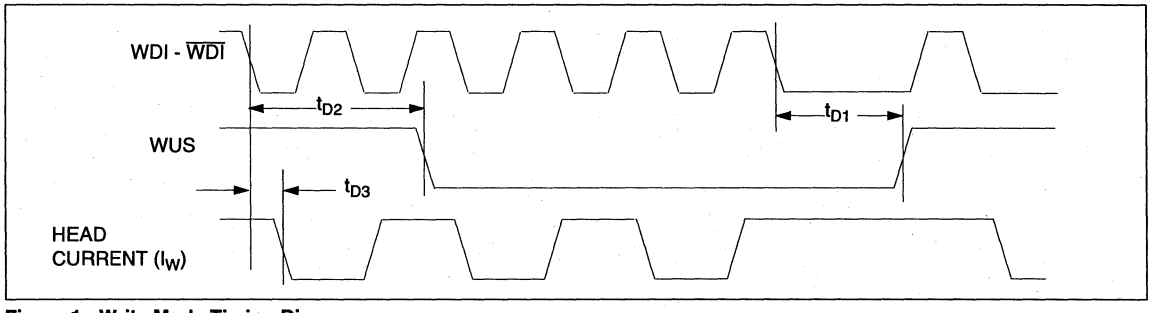


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM5252015FC

20-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH SERVO WRITE

ADVANCE INFORMATION August,1994

FEATURES

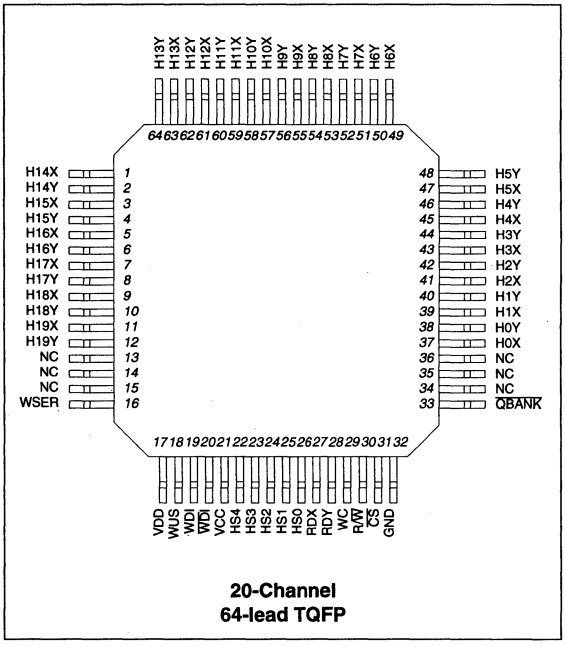
- High Performance
  - Rise/Fall Times = 4.0 ns Typical into 0.5 µH
  - Input Capacitance = 9 pF Typical
  - Input Noise = 0.6 nV/√Hz Typical
  - Head Inductance Range = 0.2 – 1.5 µH Optimized for 0.5µH
  - Voltage Gain = 150 V/V
- PECL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V and +5V/+7V in Servo Mode
- Power Supply Fault Protection
- Servo Write Two Banks of Ten Channels or Four Banks of Five Channels
- No Write Data Flip-Flop

DESCRIPTION

The VM5252015FC is a high-performance, integrated read/write preamplifier designed for use with two-terminal, thin-film recording heads. The circuit contains read amplifiers and write drivers to address twenty channels. Internal damping resistors provide different values of damping resistance between the read mode and write modes. When deselected, the circuit enters a low-power sleep mode. Current gain in the write mode is 20 and it is DAC or resistor-controllable. The power supply fault detect circuit shuts off write current in the event the power supply level drops below a unsafe threshold, thus protecting the data on the disk from any potential transients. If a line should open up, the mode select lines ($\overline{CS}$ and R/$\overline{W}$) have internal pullup resistors to ensure the select lines will be forced into a high state to prevent the device from affecting data on the disk.

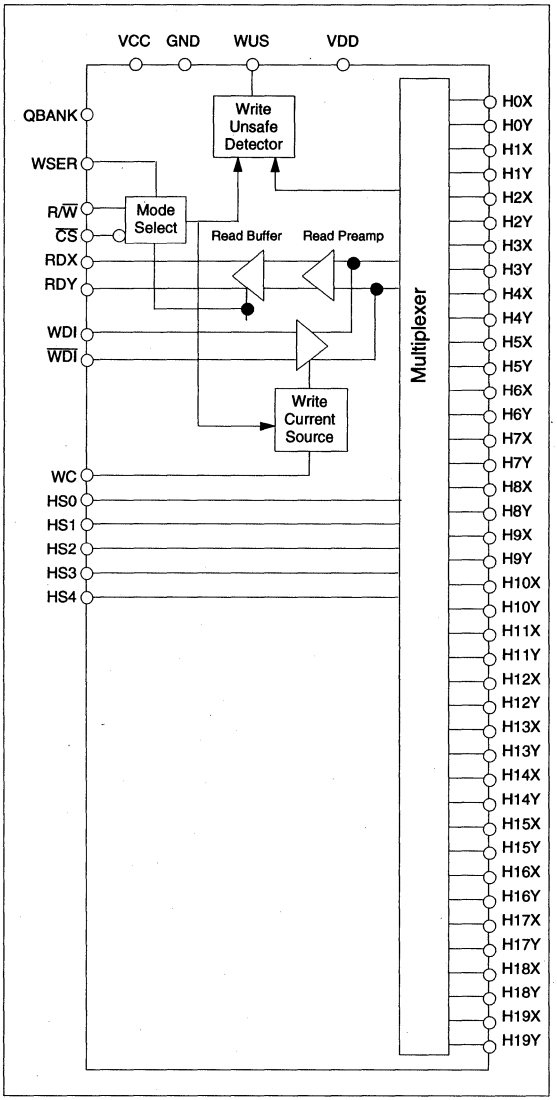
The part has a servo write mode for writing five or ten channels at a time.

CONNECTION DIAGRAM



20-Channel
64-lead TQFP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 64-lead TQFP ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature .....0°C to 125°C

CIRCUIT OPERATION

The VM5252015FC addresses up to ten two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM5252015FC as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

The write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM5252015FC because the internal 300Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device in servo mode (applicable when WUS is not used for servo selection)
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Write Servo Mode

In this mode, the operation is the same as described above except that five or ten channels are written at the same time. Two options are available for servo mode control. The first is to use pin WSER to control when the device is in servo mode (pull WSER low to enable the servo write feature). The second option is to use the WUS external resistor to control servo mode. In either case servo mode must be preceded by lowering VDD to 7V ±10%. To select servo using the WUS resistor the following procedure is used:

1. Lower VDD to 7V ±10%
2. Enter read mode via R/$\overline{W}$ high
3. WUS pull-up resistor should be tied at least 1.3V above VCC through a 1k resistor.

The device is now in servo mode with either five or ten heads writing at the same time. Upon entering write servo mode the VDD fault level will be lowered to a 5.8V threshold. To return to normal operations the following sequence is used:

1. Enter read mode
2. Return WUS resistor to VCC.
3. Raise VDD supply back to 12V ±10%
4. Drop the R/$\overline{W}$ line low

The $\overline{QBANK}$ pin is used to permit servo writing in four banks of five heads each. When $\overline{QBANK}$ is pulled low, the VM5252015FC enters quad bank select mode and HS0 and HS1 are used to select the active banks (heads 0 - 4 for HS0 = low and HS1 = low, heads 5 - 9 for HS0 = high and HS1 = low, heads 10 - 14 for HS0 = low and HS1 = high, and heads 15 - 19 for HS0 and HS1 = high). When $\overline{QBANK}$ is pulled high, the VM5252015FC enters dual bank select mode and HS0 is used to select the active banks (heads 0 - 9 for HS0 = low and heads 10 - 19 for HS0 = high). The bank selection scheme applies to either of the two servo selection methods (using WUS resistor or the WSER pin). The $\overline{QBANK}$ pin is available on all package types.

Read Mode

Read mode configures the VM5252015FC as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS4	I*	Head Select: selects one of up to 19 heads. HS0 and HS1 also select which bank of heads is written to during servo write when $\overline{\text{QBANK}}$ is pulled low (heads 0 - 4 for HS0 and HS1 = low, heads 5 - 9 for HS0 = high and HS1 = low, heads 10 - 14 for HS0 = low and HS1 = high, and heads 15 - 19 for HS0 and HS1 = high). HS0 also selects which bank of heads is written to during servo write when $\overline{\text{QBANK}}$ is pulled high (heads 0 - 9 for HS0 = low and heads 10 - 19 for HS0 = high)
H0X - H19X H0Y - H19Y	I/O	X,Y Head Terminals
WDI, $\overline{\text{WDI}}$	I*	Write Data Input: Differential PECL input signal, negative transition toggles direction of head current
$\overline{\text{CS}}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{\text{W}}$	I*	Read/Write Select: high level selects read mode, low level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply
GND		Ground
$\overline{\text{QBANK}}$		Quad Bank Select: low level selects four banks of heads for servo write (0 - 4, 5 - 9, 10 -1 4 and 15 - 19); high level selects two banks of heads for servo write (0 - 9 and 10 - 19)
WSER		Servo Write: when pulled low, servo write feature is enabled on selected heads

* May be wire-ORed for multi-chip usage.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		TBD	TBD	mA
		Write Mode		TBD	TBD	
		Idle Mode		TBD	TBD	
VDD Supply Current	I_{DD}	Read Mode		TBD	TBD	mA
		Write Mode		TBD	TBD	
		Idle Mode		TBD	TBD	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		250	TBD	mW
		Write Mode: I_W = 20mA		650	TBD	
		Idle Mode		25	TBD	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VDD Fault Voltage	V_{DDF}		9.5	10	10.5	V
VDD Servo Mode Fault	V_{DDFS}		5.5	5.8	6.1	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} 3.8V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} 5.5V, 0< V_{DD} < 13.2V	-200		+200	

WRITE SERVO CHARACTERISTICS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Servo Mode		TBD		mA
VDD Supply Current	I_{DD}	Servo Mode, V_{DD} = 7V ±10%		TBD		mA
Power Dissipation	P_D	Servo Mode @ I_W = 15mA		TBD		W
Servo Write Current Tolerance			-10		+10	%
Servo Write Current Range			5		15	mA
Rise/Fall Time		L_H = 0.5µH, I_W = 15mA, @ V_{DD} = 7V		7		ns
Asymmetry		L_H = 0, R_H = 0			0.5	ns
WDI Input			1		15	MHz

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz		50		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz		75		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.60	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		9	14	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	380	750		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	50	60		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	45	50		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	45	50		dB
Output Offset Voltage	$\|V_{OS}\|$	V_{IN} = 0 on selected head, A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 0.5µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 35mA	10	11	12	Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			18	22	pF
Differential Output Resistance	R_{OUT}	Without damping resistor	3.2			kΩ
		With damping resistor		300		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.0			MHz
Write Current Range	I_W	1430Ω, < R_{WC} < 5kΩ	5		35	mA
Write Current Tolerance	ΔI_W	I_W range 5mA to 35mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 0.5µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.2	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.5	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time*	t_r/t_f	L_H = 0.5µH, I_W = 20mA		4		ns
Rise/Fall Time	t_r/t_f	(L_H = 0µH)		TBD		ns

*Rise/Fall time might vary according to customer rise fall/settle time trade off. Rise/Fall time and settle time will be selected for maximum bit cell.

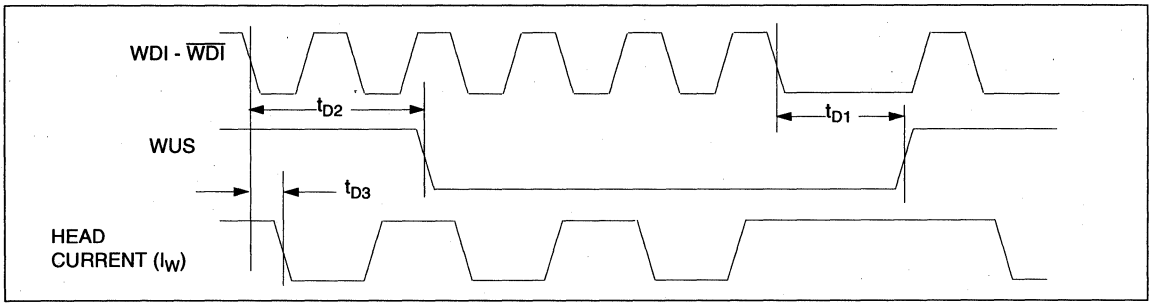


Figure 1: Write Mode Timing Diagram

Two-Terminal High-Performance +5V Preamplifiers

VTC Inc.
Value the Customer™

VM3200

2 OR 4-CHANNEL, 3.3 TO 5-VOLT, TWO-TERMINAL, THIN-FILM/MIG HEAD, READ/WRITE PREAMPLIFIER

August,1994

FEATURES

- High Performance
  - Read Gain = 300, 200 or 150 V/V
  - Input Noise = 0.48nV/√Hz Typical
  - Head Inductance Range = 0.2 – 5 µH
  - Write Current Range 2 - 25 mA
  - Input Capacitance: Standard = 20 pF
    Low = 12 pF
- Improved Write Voltage = 5 Vp-p Diff. Typical (3V supply)
- Very Low Power Dissipation = 0.3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Single Power Supply = 3.3V to 5V ±10%
- Fault Detect Capability
- Designed for Two-Terminal, Thin-Film or MIG Heads
- Standard Schottky - Isolated 400 W Damping Resistor (patent pending)
- Available in 2 or 4 Channels

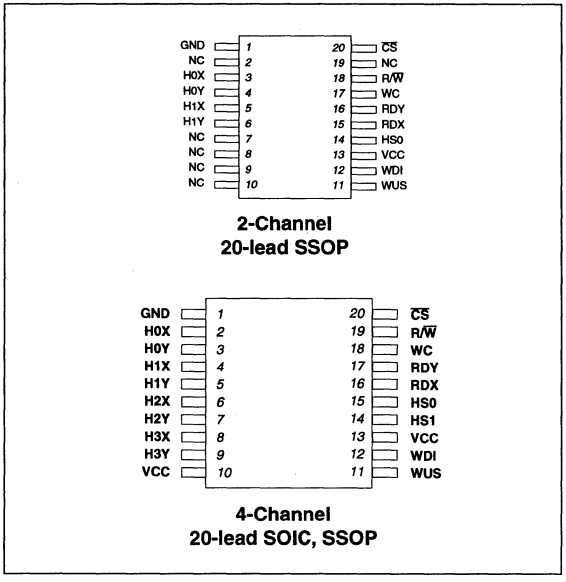
DESCRIPTION

The VM3200 is a high-performance, very low-power read/write preamplifier designed for use with two-terminal, thin-film or MIG recording heads. This device will operate on a single power supply from 3-volts to 5-volts. This makes the VM3200 ideally suited for both battery-powered and 5-volt disk drive applications.

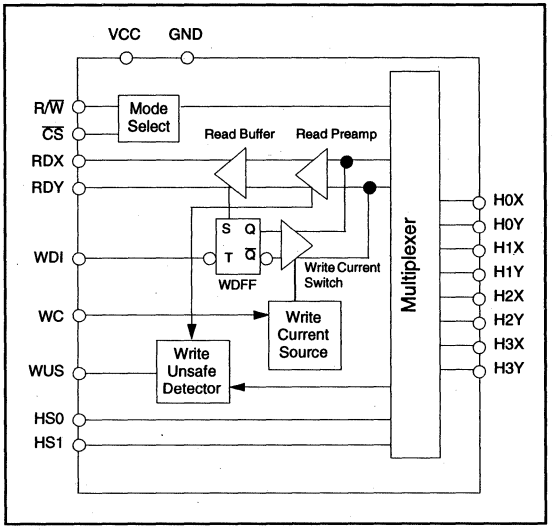
The VM3200 provides write current switching in the write mode and a low noise data path in the read mode for up to four read/write heads. When deactivated, the device enters a sleep mode that reduces power dissipation to 0.7 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power up/down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes. Write mode performance is improved by providing 5-volt with 3.3-volt supply differential peak-to-peak head voltage allowing the write current to swing faster.

The VM3200 is available in a variety of package options. Please consult VTC for package availability.

CONNECTION DIAGRAMS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to 5.5V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+3.3V to +5V ± 10%

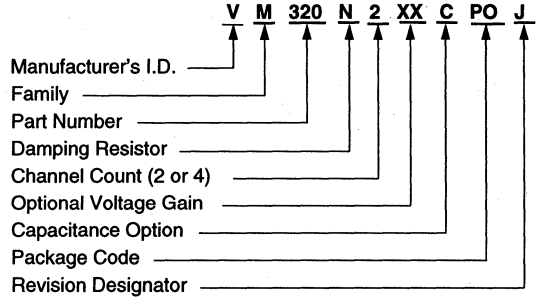
Write Current (I_W) ..... 2 to 25mA

Head Inductance (L_H) ..... 0.2 to 5µH

Junction Temperature (T_J) ..... 25°C to 125°C

ORDERING INFORMATION

The VM3200 part type is available with a wide variety of possible options that allow the device to closely fit different applications. In order to simplify the task of defining the various possible options, ordering information is included here. Please note, not all possible combinations of options may actually have been built. Please consult the factory with any questions.



DAMPING RESISTOR
- Blank = Schottky Diode Connected Damping Resistor
- N = No Internal Damping Resistor

VOLTAGE GAIN
- 10 = 100 Voltage Gain
- 15 = 150 Voltage Gain
- 20 = 200 Voltage Gain
- 25 = 250 Voltage Gain
- 30 = 300 Voltage Gain

CAPACITANCE OPTION
- C = Low Capacitance
- Blank = Low Noise

PACKAGE CODES
- PO = Small Outline Integrated Circuit (SOIC)
- SS = Shrink Small Outline Package (SSOP)

CIRCUIT OPERATION

The VM3200 addresses up to four 2-terminal, thin-film or MIG recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control are determined by the head select lines, HS1, HS2 and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups, provided on the $\overline{CS}$ and R/$\overline{W}$ lines, will force the device into a non-write condition if either control line opens up. The part's operation over a wide range of inductive loads makes it suitable for two-terminal MIG heads also.

Write Mode

In write mode, the VM3200 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. When switching from read-to-write mode, write current flows into the "X" head port. Write current is toggled between the X and Y sides of the selected head in each high to low transition on the write data flip-flop (WDFF).

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and ground. An internally generated reference voltage is present at the WC pin. The magnitude of the write current is:

$$I_W = K_W/R_{WC} = 25/R_{WC}$$

where,

I_W = Write Current
K_W = Write Current Constant
R_{WC} = Write Current Set Resistor

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, may be required to clear the WUS line. Write unsafe detect conditions:

- No write current
- WDI frequency too low
- Read or sleep mode

In write mode, the VM3200 provides 5 Vp-p differential head voltage swing with 3.3-volt supply that allows the write current to swing faster. This results in faster rise/fall times and improved writer performance.

Read Mode

In read mode, the VM3200 acts as a low-noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the pulse detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 0.7 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low "wakes up" the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Table 1: Head Select

HS1	*HS0*	*HEAD*
0	0	0
0	1	1
1	0	2
1	1	3

Table 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	*MODE*
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS1	I*	Head Select: selects one of up to four heads
H0X - H3X H0Y - H3Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O	Read Data Output: differential output data
VCC		+3.3V Supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode		33	47	mA
		Write Mode		$30 + 1.375I_W$	$35 + 1.375I_W$	
		Idle Mode		0.3	TBD	
Power Dissipation	PD	Read Mode		120	170	mW
		Write Mode, I_W = 15mA		165	200	
		Idle Mode		0.7	1.3	
Input High Voltage	V_{IH}		2		5.5	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V	-400		+1	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-1		+20	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA			0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 3.3V			100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA		2.5		V

Note 1: Typical values are given at T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	260	300	340	V/V
			170	200	330	
			120	150	180	
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	25	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	35	60		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.48	TBD	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz, standard		20	TBD	pF
		V_{IN} = 1mVp-p, f = 5MHz, low		12	TBD	
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	1000		pF
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	4		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	73		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	70		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	60		dB
Output Offset Voltage	V_{OS}		-300	25	+300	mV
Single-Ended Output Resistance	R_{SEO}				50	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1µH, R_H = 30Ω, I_W = 15mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.114		V
I_{WC} to Head Current Gain	A_I	V_{CC} = 3V		22		mA/mA
		V_{CC} = 5V		24.7		
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$, V_{CC} = 3V	23	25	27	V
		$K_W = (V_{WC})(A_I)$, V_{CC} = 5V		27.5	28	
Write Current Range	I_W	$1 < R_{WC} < 12.5k\Omega$	2		25	mA
Write Current Tolerance	ΔI_W	I_W = 2 - 25mA	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open head, V_{CC} = 3V		5		Vp-p
		Open head, V_{CC} = 5V		9		
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				20	pF
Differential Output Resistance	R_{OUT}		3200			Ω
Unselected Head Current	I_{UH}	I_W = 15mA		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			1.6		V

Note 1: Typical values are given at T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 15mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W			1.0	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope			1.0	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0, HS1 any Head Delay	t_{HS}	HS0, HS1 to 90% of 100mV, 10MHz read signal envelope			0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		1.3		5.6	µs
WUS Unsafe to Safe Delay	t_{D2}				1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, I_W = 15mA, L_H = 0, R_H = 0		3	6	ns
		10% to 90% points, I_W = 15mA, L_H = 1µH, R_H = 30Ω		10	14	

Note 1: Typical values are given at T_A = 25°C.

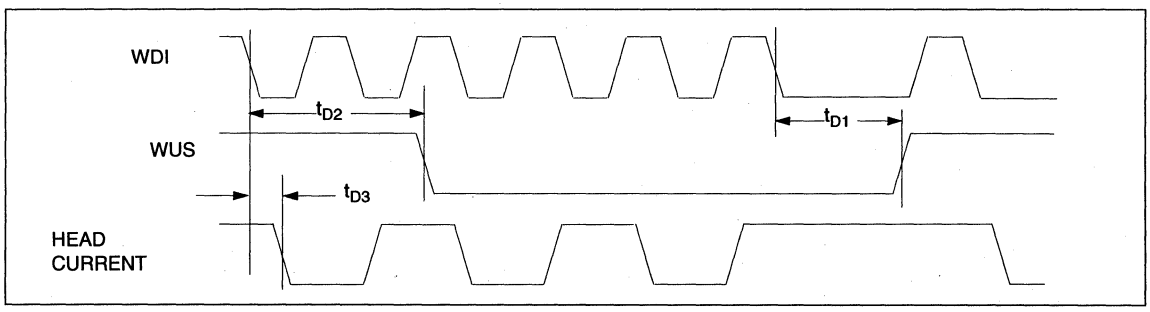


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7100

2, 4, 6 OR 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance
  - Read Gain Options Available (refer to Table 4)
  - Input Noise (refer to Table 3)
  - Head Inductance Range = 0.2 – 5 µH
  - Write Current Range 1 - 40 mA
  - Input Capacitance (refer to Table 3)
- Low Input Capacitance Option Available, C_{IN} = 16 pF max
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Designed for 2-Terminal Thin-Film or MIG Heads
- Optional Schottky Diode - Isolated 400Ω Damping Resistor Available (patent pending)
- Available in 2, 4, 6 or 8-Channels

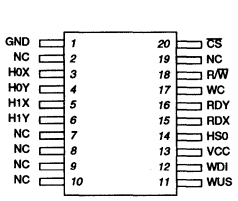
DESCRIPTION

The VM7100 is a high-performance, very low-power read/write preamplifier designed for use with external 2-terminal, thin-film or MIG recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives.

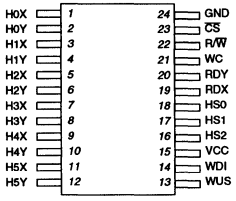
The VM7100 provides write current switching in the write mode and provides a low noise data path in the read mode for up to eight read/write recording heads. When deactivated, the device enters a ***sleep mode*** which reduces power dissipation to 3 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

The VM7100 is available in several different packages. Please consult VTC for package availability, additional read mode voltage gains and input capacitance/noise options.

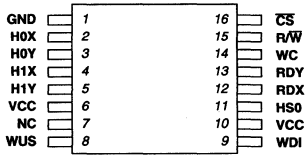
CONNECTION DIAGRAMS



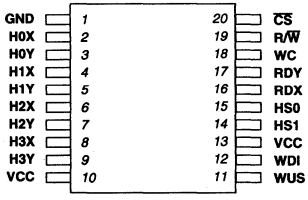
2-Channel
20-lead SSOP



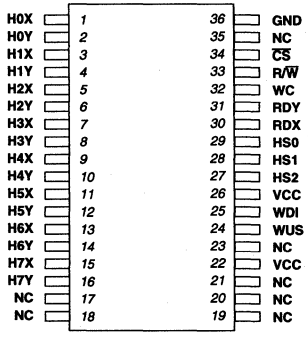
6-Channel
24-lead SSOP



2-Channel
16-lead SOIC

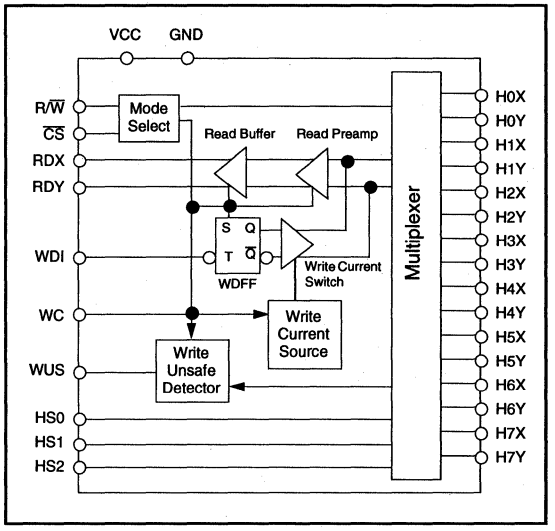


4-Channel
20-lead SOIC, SSOP, VSOP



8-Channel
36-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 16-lead SOIC ..... 100°C/W
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 20-lead VSOP ..... 120°C/W
- 24-lead SSOP ..... 100°C/W
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

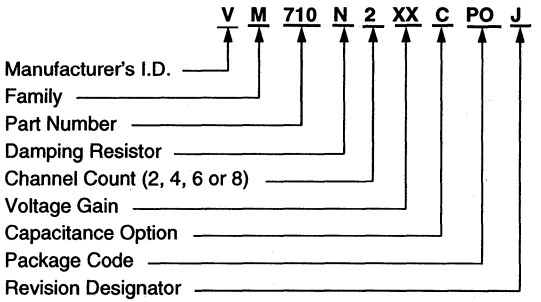
Write Current (I_W) ..... 1 to 40mA

Head Inductance (L_H) ..... 0.2 to 10µH

Junction Temperature (T_J) ..... 25°C to 125°C

ORDERING INFORMATION

The VM7100 part type is available with a wide variety of possible options that allow the device to closely fit different applications. In order to simplify the task of defining the various possible options, ordering information is included here. Please note, not all possible combinations of options may actually have been built. Please consult the factory with any questions.



DAMPING RESISTOR
- Blank = Schottky Diode Connected Damping Resistor
- N = No Internal Damping Resistor

VOLTAGE GAIN
- 10 = 100 Voltage Gain
- 15 = 150 Voltage Gain
- 20 = 200 Voltage Gain
- 25 = 250 Voltage Gain
- 30 = 300 Voltage Gain

CAPACITANCE OPTION (refer to Table 3)
- C = Low Capacitance
- I = Intermediate Capacitance/Noise
- Blank = Low Noise

PACKAGE CODES
- PO = Small Outline Integrated Circuit (SOIC)
- SS = Shrink Small Outline Package (SSOP)
- VS = Very Small Outline Package (VSOP)

CIRCUIT OPERATION

The VM7100 addresses up to eight 2-terminal, thin-film recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control is determined by the head select lines (HS2 - HS0) and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pull-ups provided on the $\overline{CS}$ and R/$\overline{W}$ lines will force the device into a non-write condition if either control line opens up. The part's operation over a wide range of inductive loads makes it suitable for 2-terminal MIG heads.

Write Mode

In write mode, the VM7100 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the write data flip-flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and ground. An

internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} + 0.2mA$$
$$= 50/R_{WC} + 0.2mA$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- No write current
- WDI frequency too low
- Read or sleep mode

Read Mode

In read mode, the VM7100 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the pulse detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 3 mW in the ***sleep mode.*** Switching the $\overline{CS}$ line low wakes up the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Diode Connected Damping Resistor (patent pending)

The VM7100 has damping resistors isolated by Schottky diodes as an option. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform.

Input Structure:

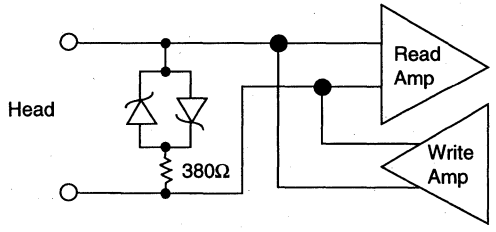


Table 1: Head Select

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	*MODE*
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I*	Head Select: selects one of up to eight heads
H0X - H7X H0Y - H7Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode		$40 + 0.05I_W$	$51 + 0.05I_W$	mA
		Write Mode		$44 + 1.05I_W$	$52 + 1.05I_W$	
		Idle Mode		0.6	3	
Power Dissipation	PD	Read Mode, $I_W = 20mA$		205	286	mW
		Write Mode, $I_W = 20mA$		320	402	
		Idle Mode		3	17	
Input High Voltage	V_{IH}		2		$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	$V_{IH} = 2.7V$			80	µA
Input Low Current	I_{IL}	$V_{IL} = 0.4V$	-160		-0.6	µA
WUS Output Low Voltage	V_{OL}	$I_{OL} = 4.0mA$		0.35	0.5	V
WUS Output High Current	I_{OH}	$V_{OH} = 5.0V$		13	100	µA
VCC Value for Write Current Turn Off		$I_H < 0.2mA$	3.7	4.0	4.3	V

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

Table 3: Input Noise and Differential Input Capacitance Options Available

Input Noise			*Input Capacitance*			*Option Designator*
TYP	*MAX*	*UNIT*	*TYP*	*MAX*	*UNIT*	
0.50	0.70	nV/√Hz	32	45	pF	None/Standard
0.60	0.75		16	32		I
0.70	0.85		9	16		C

Table 4: Differential Read Voltage Gain

MIN	*TYP*	*MAX*	*UNIT*	*Gain Option Designator*
84	100	116	V/V	10
125	150	175		15
167	200	233		20
210	250	290		25
250	300	350		30

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz, see Table 4				V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p, gain = 150	40	55		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p, gain = 150	65	85		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0, see Table 3		0.5	0.7	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz, see Table 3		33	45	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, see Table 3		9	16	pF
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	70		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	66		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	55		dB
Output Offset Voltage	V_{OS}		-300	2	+300	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		VDC
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	-45	350	mV
Single-Ended Output Resistance	R_{SEO}			22	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, $L_H = 1\mu H$, $R_H = 30\Omega$, $I_W = 20mA$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$	46	50	54	V
Write Current Range	I_W	$12.56 < R_{WC} < 62.5k\Omega$	1		40	mA
Write Current Tolerance	ΔI_W	$I_W = 10 - 40mA$	-8	-1	+8	%
Differential Head Voltage Swing	V_{DH}		4.5	5.4		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3200			Ω
Unselected Head Current	I_{UH}			0.15	1	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			$V_{CC} - 2.7$		V

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.06	1.0	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.15	1.0	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.23	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.02	0.6	µs
HS0 - HS2 any Head Delay	t_{HS}	HS0 - HS2 to 90% of 100mV, 10MHz read signal envelope		0.23	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	2.1	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}				1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points		12	30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.04	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		2	5	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		12	16	

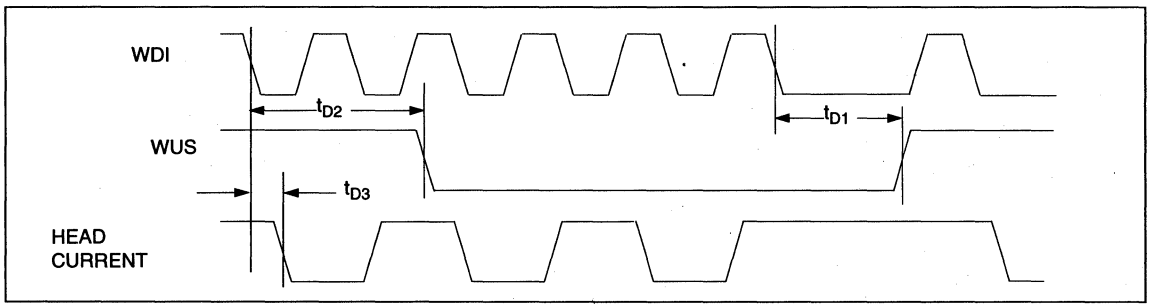


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM71110

4, 6, 8 OR 10-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

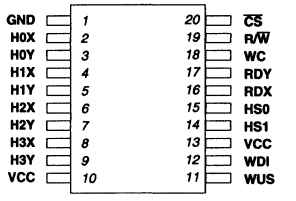
- High Performance
  - Read Gain = 200 300 V/V
  - Input Noise = 0.5nV/√Hz Typical
  - Head Inductance Range = 0.4 – 5 µH
  - Write Current Range 1 - 40 mA
  - Input Capacitance = 13 pF Typical
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Designed for 2-Terminal Thin-Film or MIG Heads

DESCRIPTION

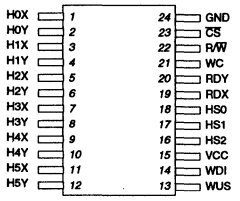
The VM71110 is a high-performance, very low-power read/write preamplifier designed for use with external 2-terminal, thin-film or MIG recording heads. This circuit operates on a single 5-volt power supply.

The VM71110 provides write current switching in the write mode and provides a low noise data path in the read mode for up to ten read/write recording heads. When deactivated, the device enters a ***sleep mode*** which reduces power dissipation to 3 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

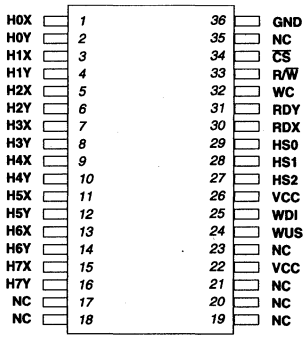
CONNECTION DIAGRAM



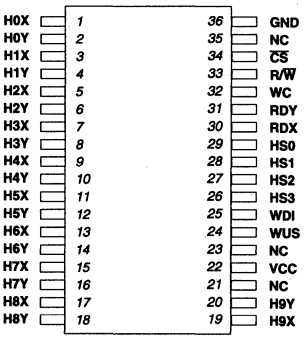
VM7114
4-Channel
20-lead SOIC, SSOP, VSOP



VM7116
6-Channel
24-lead SSOP

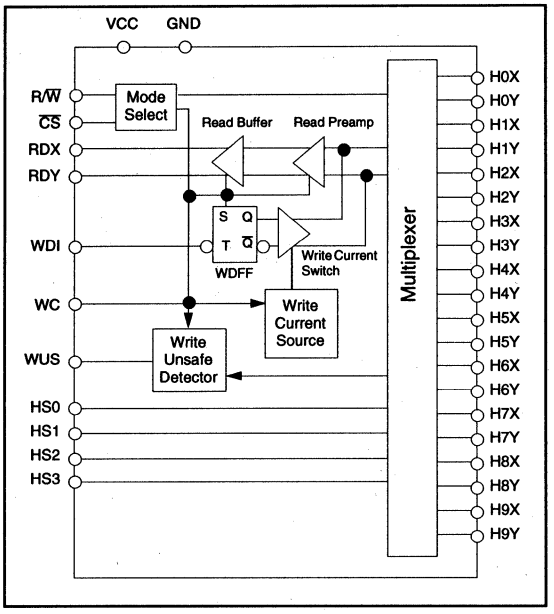


VM7118
8-Channel
36-lead SOIC



VM71110
10-Channel
36-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 20-lead VSOP ..... 120°C/W
- 24-lead SSOP ..... 100°C/W
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

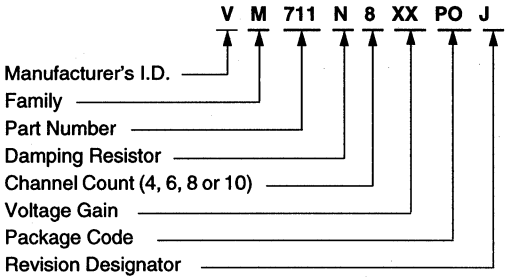
Write Current (I_W) ..... 1 to 40mA

Head Inductance (L_H) ..... 0.4 to 10µH

Junction Temperature (T_J) ..... 25°C to 125°C

ORDERING INFORMATION

The VM71110 is available with a wide variety of possible options that allow the device to closely fit different applications. In order to simplify the task of defining the various possible options, ordering information is included here. Please note, not all possible combinations of options may actually have been built. Please consult the factory with any questions.



DAMPING RESISTOR
- Blank = Schottky Diode Connected Damping Resistor
- N = No Internal Damping Resistor

VOLTAGE GAIN
- 20 = 200 Voltage Gain

PACKAGE CODES
- PO = Small Outline Integrated Circuit (SOIC)
- SS = Shrink Small Outline Package (SSOP)
- VS = Very Small Outline Package (VSOP)

CIRCUIT OPERATION

The VM71110 addresses up to ten 2-terminal, thin-film recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control is determined by the head select line, HS1 and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups, provided on the $\overline{CS}$ and R/$\overline{W}$ lines, will force the device into a non-write condition if either control line opens up. The part's operation over a wide range of inductive loads makes it suitable for 2-terminal MIG heads.

Write Mode

In write mode, the VM71110 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the write data flip-flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and ground. An internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} + 0.2mA$$
$$= 50/R_{WC} + 0.2mA$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally,

the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- No write current
- WDI frequency too low
- Read or sleep mode

Read Mode

In read mode, the VM71110 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the pulse detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, all circuitry is shut down so that power dissipation is reduced to 3 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low *wakes up* the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Input Structure:

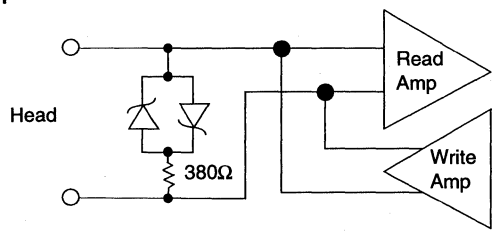


Table 1: Head Select

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
0	0	0	0	8
0	0	0	1	9

Table 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	*MODE*
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to ten heads
H0X - H9X H0Y - H9Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode		$40 + 0.05I_W$	$51 + 0.05I_W$	mA
		Write Mode		$31 + 1.05I_W$	$45 + 1.05I_W$	
		Idle Mode		0.6	3	
Power Dissipation	PD	Read Mode, $I_W = 20mA$		205	286	mW
		Write Mode, $I_W = 20mA$		320	402	
		Idle Mode		3	5.5	
Input High Voltage	V_{IH}		2		$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	$V_{IH} = 2.7V$			80	µA
Input Low Current	I_{IL}	$V_{IL} = 0.4V$	-160		-0.6	µA
WUS Output Low Voltage	V_{OL}	$I_{OL} = 4.0mA$		0.35	0.5	V
WUS Output High Current	I_{OH}	$V_{OH} = 5.0V$		13	100	µA
VCC Value for Write Current Turn Off		$I_H < 0.2mA$	3.7	4.0	4.3	V

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	167	200	233	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p, gain = 150	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p, gain = 150	65	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.7	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		13	16	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	280	1000		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	9		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	63		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	66		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	60		dB
Output Offset Voltage	V_{OS}		-300	50	+300	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		VDC
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	-60	350	mV
Single-Ended Output Resistance	R_{SEO}			16	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$	46	50	54	V
Write Current Range	I_W	$12.56 < R_{WC} < 62.5k\Omega$	5		40	mA
Write Current Tolerance	ΔI_W	I_W = 10 - 40mA	-8	-1	+8	%
Differential Head Voltage Swing	V_{DH}		4.5	5.4		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		2200			Ω
Unselected Head Current	I_{UH}			0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.06	0.3	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.55	1	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.30	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.05	0.6	µs
HS0 - HS3 any Head Delay	t_{HS}	HS0 - HS3 to 90% of 100mV, 10MHz read signal envelope		0.03	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	2.3	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}			0.4	1	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points		12	30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.03	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.9	5	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		12	16	

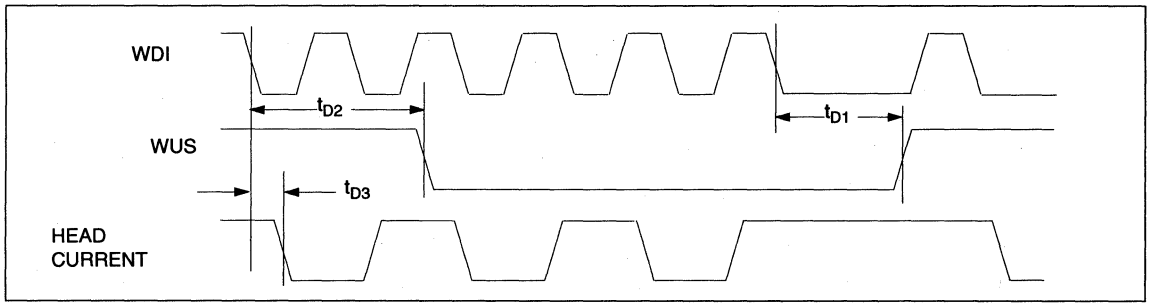


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7150

2, 4 OR 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH MULTIPLE SERVO WRITE CAPABILITY

August, 1994

FEATURES

- High Performance
  - Read Gain = 200 - 300 V/V Typical
  - Input Noise 0.75 nV/$\sqrt{Hz}$ Maximum
  - Head Inductance Range = 0.4 – 5 µH (0.5 µH Typical)
  - Write Current Range 5 - 35 mA
  - Input Capacitance = 18pF Maximum (14 pF Typical)
- Pseudo ECL Write Data Inputs
- Servo Write Two or Four Channels at the Same Time
  - VM7152 Two-Channel Servo Write
  - VM7154 Four-Channel Servo Write
  - VM7158 Two Banks of Four-Channel Servo Write
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Fast Write-to-Read and Read-to-Write Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Designed for 2-Terminal Thin-Film or MIG Heads
- Other Read Gain Options Available
- Available in 2, 4 or 8-Channels

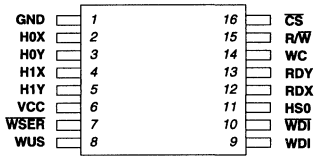
DESCRIPTION

The VM7150 is a high-performance, very low-power read/write preamplifier designed for use with external 2-terminal, thin-film or MIG recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives. The VM7150 provides a two or four channel servo write feature, enabling the user to write servo information directly through the preamp.

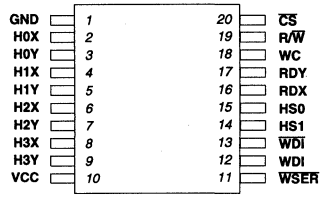
The VM7150 provides write current switching in the write mode and a low noise data path in the read mode for up to eight read/write recording heads. When deactivated, the device enters a ***sleep mode*** that reduces power dissipation to 4.5 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

The VM7150 is available in several different packages. Please consult VTC for package availability and additional read mode voltage gains.

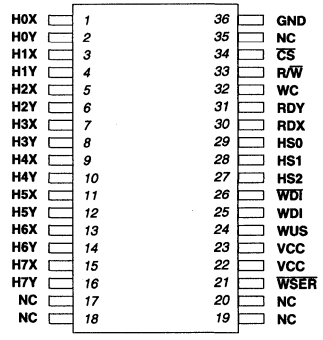
CONNECTION DIAGRAMS



2-Channel
16-lead SOIC
(narrow .150" wide body)

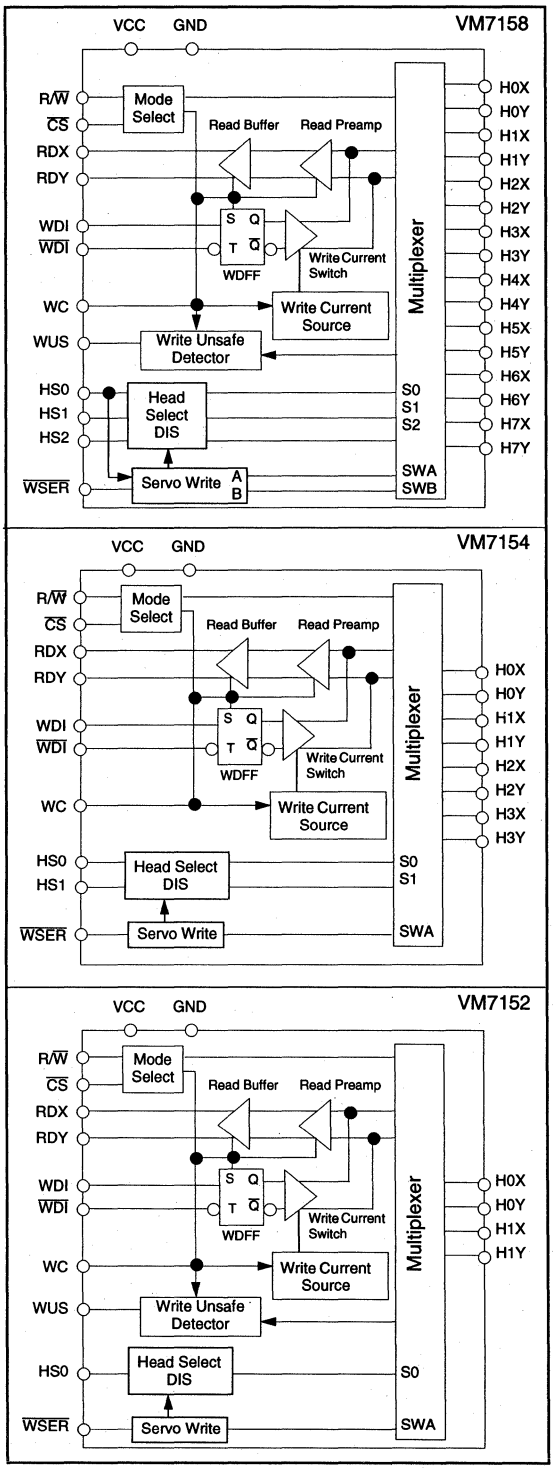


4-Channel
20-lead SOIC



8-Channel
36-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 16-lead Narrow SOIC ..... 100°C/W
- 20-lead SOIC ..... 90°C/W
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write Current (I_W) ..... 1 to 40mA

Head Inductance (L_H) ..... 0.4 to 10µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7152 addresses two two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins $\overline{WSER}$, HS0, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1a and 2a.

The VM7154 addresses four two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins $\overline{WSER}$, HS0, HS1, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1b and 2b.

The VM7158 addresses eight two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HS0, HS1, HS2, $\overline{WSER}$, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1c and 2c.

On all versions, internal pull-up resistors on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

In write mode, the VM7150 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the Write Data Flip-Flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and Ground. An internally generated reference voltage is present at the WC pin.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} + 0.2mA$$
$$= 50/R_{WC} + 0.2mA$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- Multiple servo write
- No write current
- WDI frequency too low
- Read or sleep mode

The WUS function is not operational and, therefore, not pinned out on the VM7154.

Servo Write Mode

In servo write mode, two channels of the VM7152 are active at the same time. Pin $\overline{WSER}$ controls the servo mode. When $\overline{WSER}$ and R/$\overline{W}$ are low, the chip is in servo write mode, where both heads are written independent of the head select line (see table 1a). When $\overline{WSER}$ is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select line.

In servo write mode, four channels of the VM7154 are active at the same time. Pin $\overline{WSER}$ controls the servo mode. When $\overline{WSER}$ and R/$\overline{W}$ are low, the chip is in servo write mode: four channels are written at the same time, independent of the head select lines (see table 1b). When $\overline{WSER}$ is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select lines.

In servo write mode, four channels of the VM7158 are active at the same time. Pin $\overline{WSER}$ controls the servo mode and HS0 controls which four heads are simultaneously written. When $\overline{WSER}$ and R/$\overline{W}$ are low, the chip is in servo write mode: four channels are written at the same time dependent on the state of HS0. When HS0 = 0, heads 0, 2, 4 and 6 are written and when HS0 = 5V, heads 1, 3, 5 and 7 are written (see Table 1c). When $\overline{WSER}$ is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select lines.

On all versions, an internal pull-up resistor on pin $\overline{WSER}$ will force the device into single head write mode if the control line is accidentally opened.

Read Mode

In read mode, the VM7150 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the Pulse Detector circuit connected to these outputs.

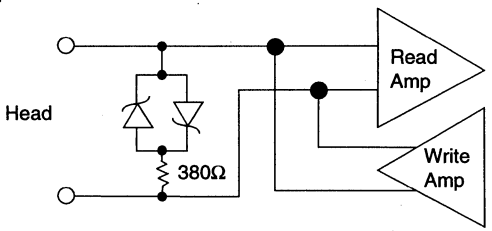
Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 4.5 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low wakes up the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Diode Connected Damping Resistor (patent pending)

The VM7158 has damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform.

Input Structure:



Please consult factory for damping resistor options on other devices.

Table 1a: Mode Selection for VM715N2

R/$\overline{W}$	$\overline{CS}$	$\overline{WSER}$	MODE
0	0	1	Write Single
1	0	X	Read
X	1	X	Idle
0	0	0	Write Servo (head 0, 1)

Table 1b: Mode Selection for VM715N4

R/$\overline{W}$	$\overline{CS}$	$\overline{WSER}$	MODE
0	0	1	Write Single
1	0	X	Read
X	1	X	Idle
0	0	0	Write Servo (head 0,1,2,3)

Table 1c: Mode Selection for VM7158

R/$\overline{W}$	$\overline{CS}$	$\overline{WSER}$	HS0	MODE
0	0	1	X	Write Single
1	0	X	X	Read
X	1	X	X	Idle
0	0	0	0	Write Servo (head 0,2,4,6)
0	0	0	1	Write Servo (head 1,3,5,7)

Table 2a: Head Selection in Single Write Mode ($\overline{WSER}$ = HIGH) for VM715N2

HS0	*HEAD*
0	0
1	1

Table 2b: Head Selection in Single Write Mode ($\overline{WSER}$ = HIGH) for VM715N4

HS1	*HS0*	*HEAD*
0	0	0
0	1	1
1	0	2
1	1	3

Table 2c: Head Selection in Single Write Mode ($\overline{WSER}$ = HIGH) for VM7158

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 3: Differential Read Voltage Gain

MIN	*TYP*	*MAX*	*UNIT*	*Gain Option Designator*
84	100	116	V/V	10
125	150	175		15
167	200	233		20
208	250	292		25
250	300	350		30

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I*	Head Select: selects one of up to eight heads
H0X - H7X H0Y - H7Y	I/O	X,Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Input: PECL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground
$\overline{WSER}$	I*	Servo Write: a low level enables servo mode.

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode, I_W = 20mA		39 + 0.25I_W	49 + 0.25I_W	mA
		Write Mode, I_W = 35mA Normal, VM7152		44 + I_W	52 + I_W	
		Normal, VM7154 & VM7158		54 + I_W	64 + I_W	
		Servo, VM7152		44 + 2I_W	56 + 2I_W	
		Servo, VM7154 & VM7158		70 + 4I_W	82 + 4I_W	
		Sleep Mode		0.6	3	
Power Dissipation VM7152	PD	Read Mode, I_W = 20mA		220	297	mW
		Write Mode, I_W = 35mA Normal		395	479	
		Servo		570	693	
		Sleep Mode		3	17	
Power Dissipation VM7154 & VM7158	PD	Read Mode, I_W = 20mA		220	297	mW
		Write Mode, I_W = 35mA Normal		445	545	
		Servo		1050	1221	
		Sleep Mode		3	17	
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	Pseudo ECL			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	Pseudo ECL			80	µA
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160		-0.6	µA
WUS Ouput Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA, VM7152	3.7	4.0	4.3	V
		I_H < 0.2mA, VM7154 & VM7158	3.5	3.8	4.2	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz, see Table 3	250	300	350	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	55	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		14	18	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	350	800		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	70		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	63		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	55		dB
Output Offset Voltage	V_{OS}		-250	±10	250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		V
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	50	350	mV
Single-Ended Output Resistance	R_{SEO}			16	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$, 10 - 30mA	46	50	54	V
		$K_W = (V_{WC})(A_I)$, 5 - 35mA	45	50	55	
Write Current Range	I_W	1.258K < R_{WC} < 60Ω	5		35	mA
Write Current Tolerance	ΔI_W	I_W = 10 - 30mA	-8		+8	%
		I_W = 5 - 35mA	-10		+10	
Differential Head Voltage Swing	V_{DH}		4.5	5.2		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3200			Ω
Unselected Head Current	I_{UH}			0.15	1	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

VM7152 (Two Channels), VM7154 and VM7158 (Four Channels) Write

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 35mA			10	%
Duty Cycle (25mA/head)					20	%

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.04	0.3	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.4	1	µs
$\overline{WSER}$ to Read Delay	tSR	R/W to 90% of 100mV, 10MHz read signal envelope		0.4	1	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.15	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.05	0.6	µs
HS0 - HS2 any Head Delay	t_{HS}	HS0 - HS2 to 90% of 100mV, 10MHz read signal envelope		0.03	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	2.1	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}				1.0	µs
Head Current Propagation Delay	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.04	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.9	5	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		12	16	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

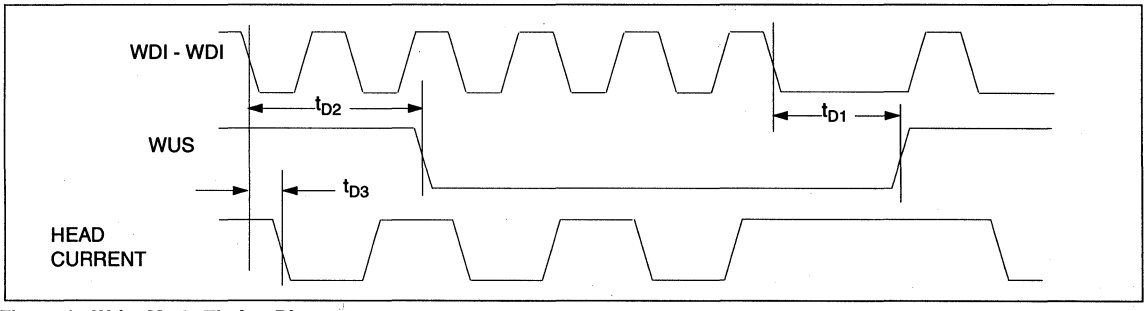


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7160

2, 4 OR 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH MULTIPLE SERVO WRITE CAPABILITY

August, 1994

FEATURES

- High Performance
  - Read Gain = 200 - 300 V/V Typical
  - Input Noise 0.75 nV/√Hz Maximum
  - Head Inductance Range = 0.2 – 5 µH (0.5 µH Typical)
  - Write Current Range 5 - 35 mA
  - Input Capacitance = 18pF Typical
- TLL Write Data Inputs
- Servo Write Two or Four Channels at the Same Time
  - VM7162 Two-Channel Servo Write
  - VM7164 Four-Channel Servo Write
  - VM7168 Two Banks of Four-Channel Servo Write
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Fast Write-to-Read and Read-to-Write Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Designed for 2-Terminal Thin-Film or MIG Heads
- Other Read Gain Options Available
- Available in 2, 4 or 8-Channels

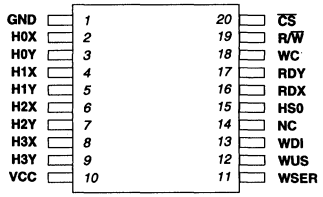
DESCRIPTION

The VM7160 is a high-performance, very low-power read/write preamplifier designed for use with external 2-terminal, thin-film or MIG recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives. The VM7160 provides a two or four channel servo write feature, enabling the user to write servo information directly through the preamp.

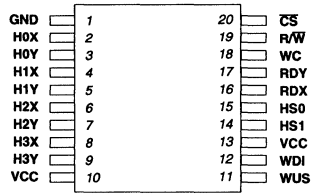
The VM7160 provides write current switching in the write mode and a low noise data path in the read mode for up to eight read/write recording heads. When deactivated, the device enters a ***sleep mode*** that reduces power dissipation to 4.5 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

The VM7160 is available in several different packages. Please consult VTC for package availability and additional read mode voltage gains.

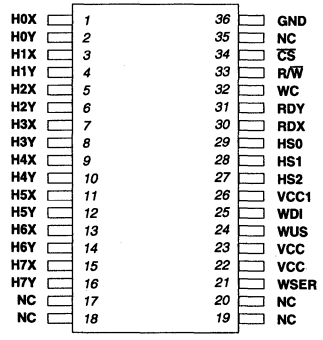
CONNECTION DIAGRAMS



2-Channel
16-lead SSOP

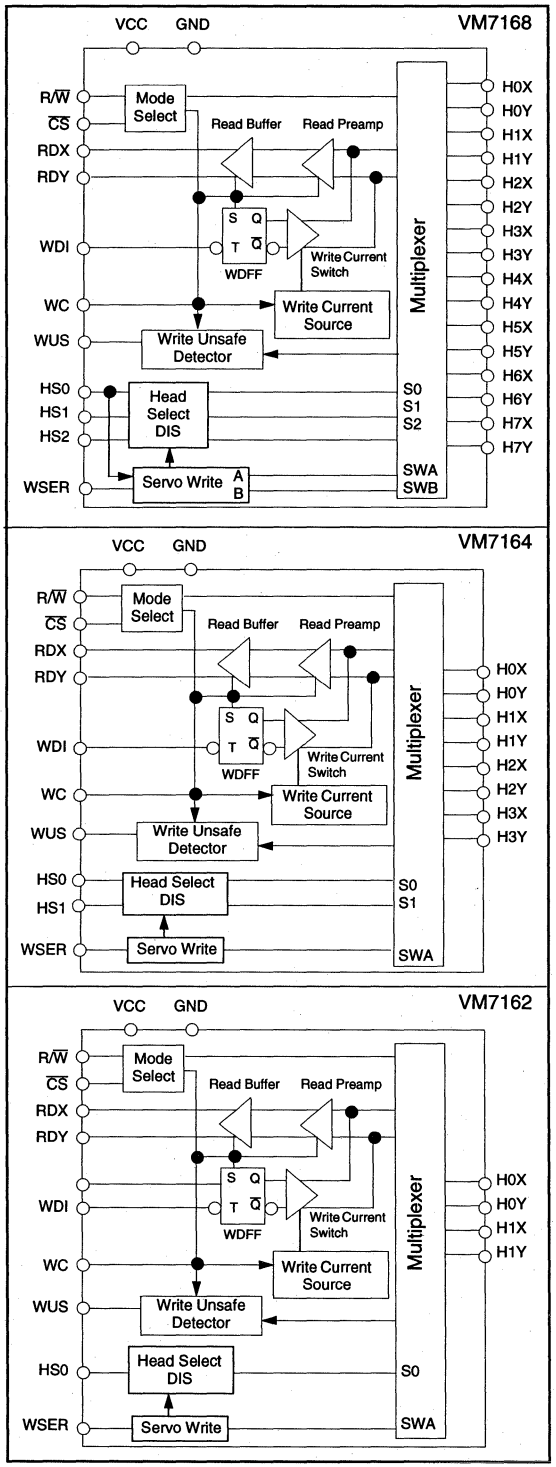


4-Channel
20-lead SOIC



8-Channel
36-lead SOIC

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write Current (I_W) ..... 1 to 40mA

Head Inductance (L_H) ..... 0.2 to 5µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7162 addresses two two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins WSER, HS0, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1a and 2a.

The VM7164 addresses four two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins WSER, HS0, HS1, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1b and 2b.

The VM7168 addresses eight two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HS0, HS1, HS2, WSER, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1c and 2c.

On all versions, internal pull-up resistors on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

In write mode, the VM7160 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the Write Data Flip-Flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and Ground. An internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} + 0.2mA$$
$$= 50/R_{WC} + 0.2mA$$

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- No write current
- WDI frequency too low
- Read or sleep mode

Servo Write Mode

In servo write mode, two channels of the VM7162 are active at the same time. Pin WSER controls the servo mode. When WSER and R/$\overline{W}$ are low, the chip is in servo write mode, where both heads are written independent of the head select line (see table 1a). When WSER is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select line.

In servo write mode, four channels of the VM7164 are active at the same time. Pin WSER controls the servo mode. When WSER and R/$\overline{W}$ are low, the chip is in servo write mode: four channels are written at the same time, independent of the head select lines (see table 1b). When WSER is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select lines.

In servo write mode, four channels of the VM7168 are active at the same time. Pin WSER controls the servo mode and HS0 controls which four heads are simultaneously written. When WSER and R/$\overline{W}$ are low, the chip is in servo write mode: four channels are written at the same time dependent on the state of HS0. When HS0 = 0, heads 0, 2, 4 and 6 are written and when HS0 = 5V, heads 1, 3, 5 and 7 are written (see Table 1c). When WSER is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select lines.

On all versions, an internal pull-up resistor on pin WSER will force the device into single head write mode if the control line is accidentally opened.

Read Mode

In read mode, the VM7160 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the Pulse Detector circuit connected to these outputs.

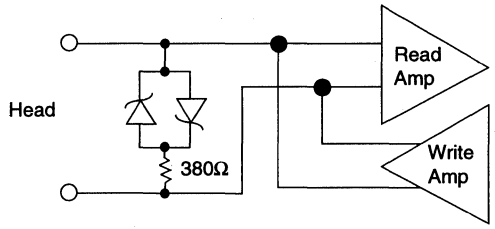
Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 4.5 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low wakes up the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Diode Connected Damping Resistor (patent pending)

The VM7162 has damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform.

Input Structure:



Please consult factory for damping resistor options on other devices.

Table 1a: Mode Selection for VM716N2

R/$\overline{W}$	$\overline{CS}$	WSER	MODE
0	0	0	Write Single
1	0	X	Read
X	1	X	Idle
0	0	1	Write Servo (head 0, 1)

Table 1b: Mode Selection for VM716N4

R/$\overline{W}$	$\overline{CS}$	WSER	MODE
0	0	0	Write Single
1	0	X	Read
X	1	X	Idle
0	0	1	Write Servo (head 0,1,2,3)

Table 1c: Mode Selection for VM7158

R/$\overline{W}$	$\overline{CS}$	WSER	HS0	MODE
0	0	1	X	Write Single
1	0	X	X	Read
X	1	X	X	Idle
0	0	1	0	Write Servo (head 0,2,4,6)
0	0	1	1	Write Servo (head 1,3,5,7)

Table 2a: Head Selection in Single Write Mode (WSER = HIGH) for VM716N2

HS0	*HEAD*
0	0
1	1

Table 2b: Head Selection in Single Write Mode (WSER = HIGH) for VM716N4

HS1	*HS0*	*HEAD*
0	0	0
0	1	1
1	0	2
1	1	3

Table 2c: Head Selection in Single Write Mode (WSER = HIGH) for VM7168

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I*	Head Select: selects one of up to eight heads
H0X - H7X H0Y - H7Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground
WSER	I*	Servo Write: a high level enables servo mode.

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operatong conditions apply, unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode, I_W = 20mA		$39 + 0.25I_W$	$49 + 0.25I_W$	mA
		Write Mode, I_W = 35mA Normal, VM7162		$44 + I_W$	$52 + I_W$	
		Normal, VM7164 & VM7168		$54 + I_W$	$64 + I_W$	
		Servo, VM7162		$44 + 2I_W$	$56 + 2I_W$	
		Servo, VM7164 & VM7168		$70 + 4I_W$	$82 + 4I_W$	
Power Dissipation VM7162	PD	Read Mode		220	297	mW
		Write Mode, I_W = 35mA Normal		395	479	
		Servo		570	693	
		Sleep Mode		0.6	3	
Power Dissipation VM7164 & VM7168	PD	Read Mode		220	297	mW
		Write Mode, I_W = 35mA Normal		445	545	
		Servo		1050	1221	
		Sleep Mode		3	17	
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WUS Ouput Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.7	4.0	4.3	V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz, VM7162	250	300	350	V/V
		V_{IN} = 1mVrms, 1MHz, VM7164	250	300	350	
		V_{IN} = 1mVrms, 1MHz, VM7168	210	250	290	
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	55	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.53	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		18	22	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	1000		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	70		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	63		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	55		dB
Output Offset Voltage	V_{OS}		-250		250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		V
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	50	350	mV
Single-Ended Output Resistance	R_{SEO}			16	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, $L_H = 1\mu H$, $R_H = 30\Omega$, $I_W = 20mA$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$, 10 - 30mA	46	50	54	V
Write Current Range	I_W	$1.44K < R_{WC} < 10.4K$	5		35	mA
Write Current Tolerance	ΔI_W	$I_W = 5 - 35mA$	-8		8	%
Differential Head Voltage Swing	V_{DH}		4.5	5.2		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3200			Ω
Unselected Head Transient Current	I_{UH}			0.15	1	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			$V_{CC} - 2.7$		V

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

VM7162 (Two Channels), VM7164 and VM7168 (Four Channels) Write

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Matching Between Channels	ΔI_W	$5mA < I_W < 35mA$			10	%
Duty Cycle (25mA/head)					20	%

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* (Note 1)	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.04	0.3	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.4	1	µs
$\overline{WSER}$ to Read Delay	tSR	R/W to 90% of 100mV, 10MHz read signal envelope		0.4	1	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.15	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.05	0.6	µs
HS0 - HS2 any Head Delay	t_{HS}	HS0 - HS2 to 90% of 100mV, 10MHz read signal envelope		0.03	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	2.1	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}				1.0	µs
Head Current Propagation Delay	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.04	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.9	5	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		12	16	

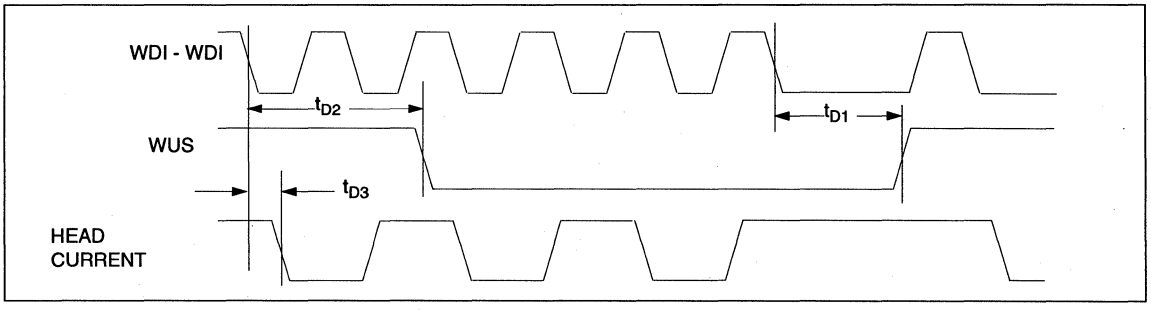


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7164S

4-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH MULTIPLE SERVO WRITE CAPABILITY

August,1994

FEATURES

- High Performance
  - Read Gain = 300 V/V Typical
  - Input Noise 0.75 nV/√Hz Maximum
  - Head Inductance Range = 0.4 – 5 µH (1 µH typical)
  - Write Current Range 5 - 35 mA
  - Input Capacitance = 18pF Maximum (14 pF typical)
- TLL Write Data Input
- Servo Write Four Channels at the Same Time
- Very Low Power Dissipation = 4.5 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Fast Write-to-Read and Read-to-Write Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Designed for 2-Terminal Thin-Film or MIG Heads
- Other Read Gain Options Available
- Available in 4-Channel

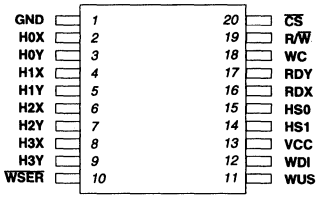
DESCRIPTION

The VM7164S is a high-performance, very low-power read/write preamplifier designed for use with external 2-terminal, thin-film or MIG recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives. The VM7164S provides a four channel servo write feature, enabling the user to write servo information directly through the preamp.

The VM7164S provides write current switching in the write mode and a low noise data path in the read mode for up to four read/write recording heads. When deactivated, the device enters a ***sleep mode*** that reduces power dissipation to 4.5 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

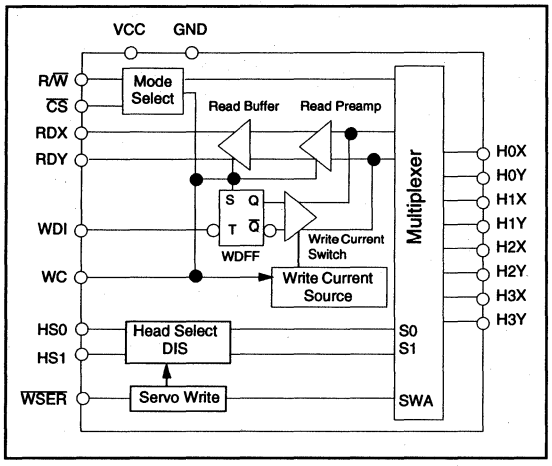
The VM7164S is available in several different packages. Please consult VTC for package availability and additional read mode voltage gains.

CONNECTION DIAGRAM



4-Channel
20-lead SOIC, SSOP. VSOP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 20-lead VSOP ..... 120°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write Current (I_W) ..... 5 to 35mA

Head Inductance (L_H) ..... 0.4 to 5µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7164S addresses four two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins $\overline{WSER}$, HS0, HS1, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2.

Internal pull-up resistors on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

In write mode, the VM7164S acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the Write Data Flip-Flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and Ground. An internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} + 0.2mA$$
$$= 50/R_{WC} + 0.2mA$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- Multiple servo write
- No write current
- WDI frequency too low
- Read or sleep mode

The WUS function is not operational and, therefore, not pinned out on the VM7164S

Servo Write Mode

In servo write mode, four channels of the VM7164S are active at the same time. Pin $\overline{WSER}$ controls the servo mode. When $\overline{WSER}$ and R/$\overline{W}$ are low, the chip is in servo write mode: four channels are written at the same time, independent of the head select lines (see table 1). When $\overline{WSER}$ is high and R/$\overline{W}$ is low, the chip is in normal write mode: one head is written at a time based on the state of the head select lines.

Internal pull-up resistor on pin $\overline{WSER}$ will force the device into single head write mode if the control line is accidentally opened.

Read Mode

In read mode, the VM7164S acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the Pulse Detector circuit connected to these outputs.

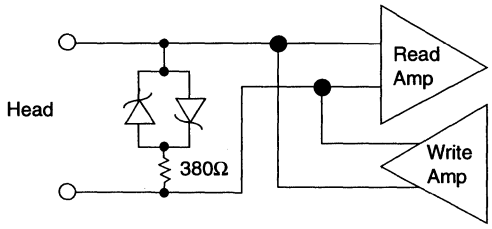
Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 4.5 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low wakes up the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Diode Connected Damping Resistor (patent pending)

The VM7164S has damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform.

Input Structure:



Please consult factory for damping resistor options on other devices.

Table 1: Mode Selection for VM7164S

R/$\overline{W}$	$\overline{CS}$	$\overline{WSER}$	MODE
0	0	1	Write Single
1	0	X	Read
X	1	X	Idle
0	0	0	Write Servo (head 0,1,2,3)

Table 2: Head Selection in Single Write Mode ($\overline{WSER}$ = HIGH) for VM7164S

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0 - HS1	I*	Head Select: selects one of up to four heads
H0X - H3X H0Y - H3Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground
$\overline{WSER}$	I*	Servo Write: a low level enables servo mode.

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operatong conditions apply, unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode, I_W = 20mA		39 + 0.25I_W	49 + 0.25I_W	mA
		Write Mode, I_W = 35mA Normal		54 + I_W	64 + I_W	
		Servo		70 + 4I_W	82 + 4I_W	
		Sleep Mode		0.6	3	
Power Dissipation	PD	Read Mode, I_W = 20mA		220	297	mW
		Write Mode, I_W = 35mA Normal		445	545	
		Servo		1050	11221	
		Sleep Mode		3	17	
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WUS Ouput Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.5	3.8	4.2	V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	250	300	350	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	55	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		14	16	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	350	800		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	70		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	63		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	60		dB
Output Offset Voltage	V_{OS}		-250	±10	250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		V
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	50	350	mV
Single-Ended Output Resistance	R_{SEO}			16	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$, 10 - 30mA	46	50	54	V
		$K_W = (V_{WC})(A_I)$, 5 - 35mA	45	50	55	
Write Current Range	I_W	1.44K < R_{WC} < 10.4K	5		35	mA
Write Current Tolerance	ΔI_W	I_W = 10 - 30mA	-8		+8	%
		I_W = 5 - 35mA	-10		+10	
Differential Head Voltage Swing	V_{DH}		4.5	5.2		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3200			Ω
Unselected Head Transient Current	I_{UH}			0.15	1	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

VM7164S (Four Channels) Write

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 35mA			10	%
Duty Cycle (25mA/head)					20	%

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.04	0.3	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.4	1	µs
$\overline{WSER}$ to Read Delay	tSR	R/W to 90% of 100mV, 10MHz read signal envelope		0.4	1	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.15	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.05	0.6	µs
HS0, HS1 any Head Delay	t_{HS}	HS0, HS1 to 90% of 100mV, 10MHz read signal envelope		0.03	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	2.1	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}				1.0	µs
Head Current Propagation Delay	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.04	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.9	5	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		12	16	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

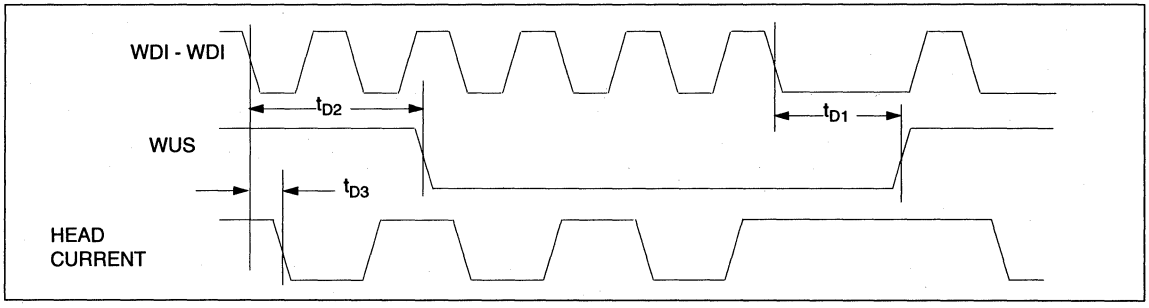


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7170

2 OR 4-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

ADVANCE INFORMATION

August, 1994

FEATURES

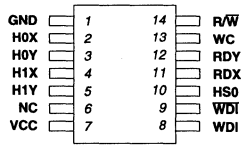
- High Performance
  - Read Gain = 300 V/V
  - Input Noise = 0.5nV/√Hz Typical
  - Head Inductance Range = 0.4 – 5 µH
  - Write Current Range 1 - 30 mA
  - Input Capacitance = 13 pF Typical
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Single Power Supply = 5 V ± 10%
- Designed for 2-Terminal Thin-Film or MIG Heads
- Optional Schottky Diode - Isolated 300 Ω Damping Resistor Available (patent pending)
- Available in 2 or 4-Channels

DESCRIPTION

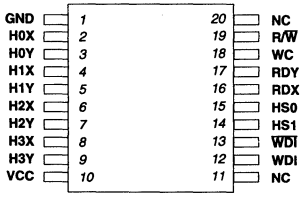
The VM7170 is a high-performance, very low-power read/write preamplifier designed for use with external 2-terminal, thin-film or MIG recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives.

The VM7170 provides write current switching in the write mode and provides a low noise data path in the read mode for up to eight read/write recording heads. When deactivated, the device enters a ***sleep mode*** which reduces power dissipation to 3 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

CONNECTION DIAGRAMS

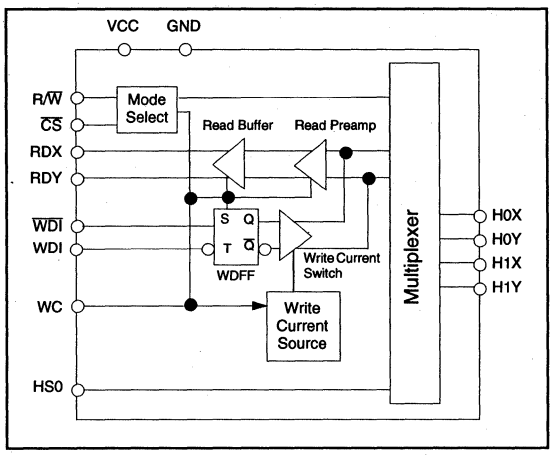


2-Channel
14-lead Narrow SOIC
VM717230NOJ



4-Channel
20-lead SOIC
VM717430POJ

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Write Current I_W 40mA
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
Output Current:
RDX, RDY: I_O .....-10mA
Junction Temperature ..... 150°C
Storage Temperature T_{stg} ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
14-lead Narrow SOIC .....TBD
20-lead SOIC..... 90°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Write Current (I_W) ..... 1 to 30mA
Head Inductance (L_H) ..... 0.4 to 10µH
Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7170 2-channel device addresses two 2-terminal, thin-film recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control is determined by the head select lines, HS0 and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups, provided on the $\overline{CS}$ and R/$\overline{W}$ lines, will force the device into a non-write condition if either control line opens up. The part's operation, over a wide range of inductive loads, makes it suitable for 2-terminal MIG heads. The VM7170 is also available as a 4-channel device.

Write Mode

In write mode, the VM7170 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the write data flip-flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and ground. An internally generated reference voltage is present at the WC pin.

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions.

Read Mode

In read mode, the VM7170 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the pulse detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, all circuitry is shut down so that power dissipation is reduced to 3 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low *wakes up* the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Input Structure:

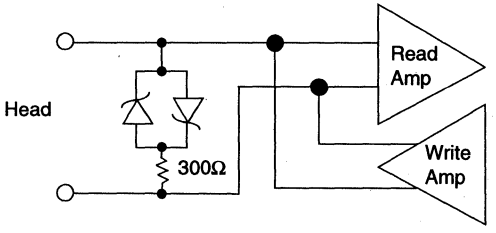


Table 1: Head Select

HS1	*HS0*	*HEAD*
0	0	0
0	1	1
1	0	2
1	1	3

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Table 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0 - HS1	I*	Head Select: selects one of four heads
H0X - H3X H0Y - H3Y	I/O	X,Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Input: PECL input signals, negative transition on WDI toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Unless otherwise specified, V_{CC} = 5V ±10%, T_A = 25°C

PARAMETER	SYM	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Power Supply Current	I_{CC}	Read Mode		40 + 0.05I_W	51 + 0.05I_W	mA
		Write Mode		31 + 1.05I_W	45 + 1.05I_W	
		Idle Mode		0.6	3	
Power Dissipation	PD	Read Mode, I_W = 20mA		205	286	mW
		Write Mode, I_W = 20mA		320	402	
		Idle Mode		3	5.5	
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160		-0.6	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.7	4.0	4.3	V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
WC Pin Voltage	V_{WC}			TBD		V
I_{WC} to Head Current Gain	A_I			10		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$	46	50	54	V
Write Current Range	I_W	TBD	5		30	mA
Write Current Tolerance	ΔI_W	I_W = 5 - 30mA			TBD	%
Differential Head Voltage Swing	V_{DH}		4.5	5.4		Vp-p
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3200			Ω
Unselected Head Current	I_{UH}			0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	250	300	350	V/V
Bandwidth	BW	-1dB |Zsl < 5Ω, V_{IN} = 1mVp-p, gain = 150	30	40		MHz
		-3dB |Zsl < 5Ω, V_{IN} = 1mVp-p, gain = 150	65	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.7	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		13	16	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	280	1000		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	9		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	63		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	66		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	60		dB
Output Offset Voltage	V_{OS}		-300	50	+300	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		VDC
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	-60	350	mV
Single-Ended Output Resistance	R_{SEO}			16	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.06	1	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.55	1	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.30	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.05	0.6	µs
HS0, HS1 any Head Delay	t_{HS}	HS0, HS1 to 90% of 100mV, 10MHz read signal envelope		0.03	0.6	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points		12	30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.03	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.9	5	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		12	16	

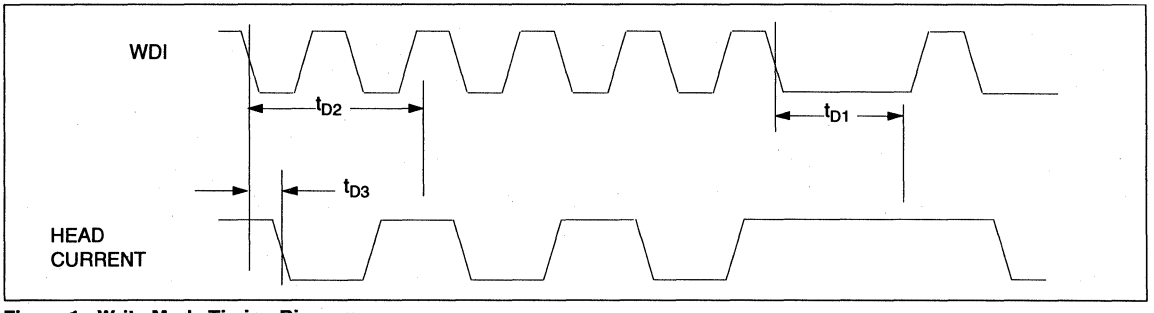


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7200

2, 4, 6 OR 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August,1994

FEATURES

- High Performance
  - Read Gain = 200 V/V Typical
  - Input Noise = 0.75nV/√Hz Maximum
  - Head Inductance Range = 0.2 – 10 µH
  - Write Current Range 10 - 40 mA
  - Input Capacitance = 23 pF Maximum
- Very Low Power Dissipation = 7.5 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Designed for Thin-Film Heads
- Write Unsafe Detection
- Optional Schottky Diode - Isolated 400Ω Damping Resistor Available (patent pending)
- Available in 2, 4, 6 or 8-Channels

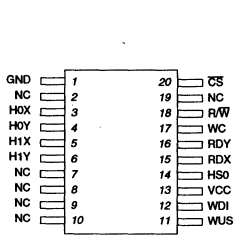
DESCRIPTION

The VM7200 is a high-performance, very low-power read/write preamplifier designed for use with external thin-film or MIG recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives.

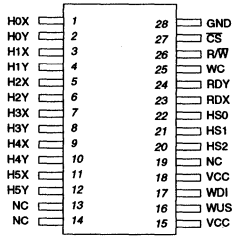
The VM7200 provides write current and data protection circuitry, and low noise read functions for up to eight read/write heads. When deactivated, the device enters a ***sleep mode*** which reduces power dissipation to 7.5 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

The VM7200 is available in several different packages. Please consult VTC for package availability.

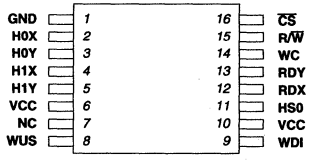
CONNECTION DIAGRAMS



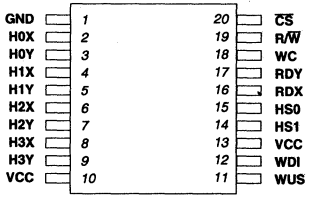
2-Channel
20-lead SSOP



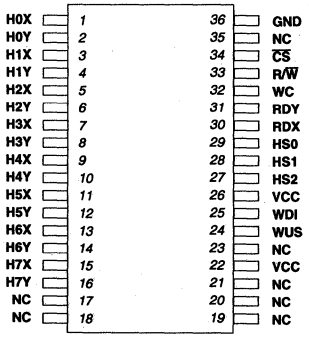
6-Channel
28-lead SSOP



2-Channel
16-lead SOIC

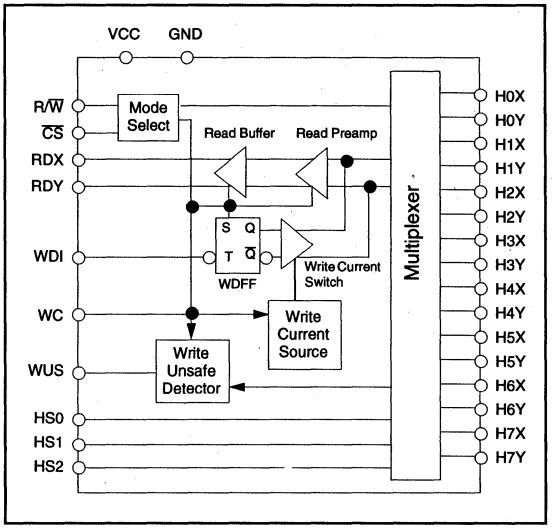


4-Channel
20-lead SOIC, SSOP, VSOP



8-Channel
36-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 16-lead SOIC ..... 100°C/W
- 20-lead SOIC ..... 60°C/W
- 20-lead SSOP ..... 110°C/W
- 20-lead VSOP ..... 120°C/W
- 28-lead SSOP ..... 100°C/W
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write Current (I_W) ..... 10 to 40mA

Head Inductance (L_H) ..... 0.2 to 10µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7200 addresses up to eight 2-terminal, thin-film recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control is determined by the head select lines, HS0, HS1, HS2 and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups, provided on the $\overline{CS}$ and R/$\overline{W}$ lines, will force the device into a non-write condition if either control line opens up. The part's operation over a wide range of inductive loads makes it suitable for non-thin-film two-terminal heads also.

Write Mode

In write mode, the VM7200 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the Write Data Flip-Flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and Ground. An internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} = 50/R_{WC}$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- No write current
- WDI frequency too low
- Read or sleep mode

Read Mode

In read mode, the VM7200 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the Pulse Detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 7.5 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low "wakes up" the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Diode Connected Damping Resistor (patent pending)

The VM7200 has damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform.

Input Structure:

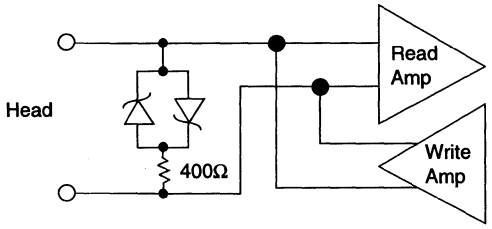


Table 1: Head Select

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 2: Mode Select

$\overline{CS}$	$R/\overline{W}$	*MODE*
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I*	Head Select: selects one of up to eight heads
H0X - H7X H0Y - H7Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
$R/\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.

** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode		33	45	mA
		Write Mode		42 + I_W	50 + I_W	
		Idle Mode		1.5	3	
Power Dissipation	PD	Read Mode		165	230	mW
		Write Mode, I_W = 20mA		310	385	
		Idle Mode		7.5	17	
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.7	4.0	4.3	V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz, Note 2	167	195	233	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	25	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	35	60		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.56	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		19	23	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain at 0.2mVrms input, f = 5MHz	4	10		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	73		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	70		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz. Selected channels V_{IN} = 0mVp-p	45	60		dB
Output Offset Voltage	V_{OS}		-300	25	+300	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.3		VDC
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	120	350	mV
Single-Ended Output Resistance	R_{SEO}			36	50	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.
Note 2: A_V is mask programmable for the VM7200L of 15 V/V.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.55		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$	46	51.5	54	V
Write Current Range	I_W	12.5K < R_{WC} < 5kΩ	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10 - 40mA	-8	+3	+8	%
Differential Head Voltage Swing	V_{DH}	Open head	4	5.2		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}	Small signal conditions			25	pF
Differential Output Resistance	R_{OUT}	Small signal conditions	3200			Ω
Unselected Head Current	I_{UH}	I_W = 20mA		0.15	1	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.3		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.1	1.0	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.6	1.0	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.27	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.08	0.6	µs
HS0 - HS2 any Head Delay	t_{HS}	HS0 - HS2 to 90% of 100mV, 10MHz read signal envelope		0.19	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	3.1	4.5	µs
WUS Unsafe to Safe Delay	t_{D2}			0.1	1	µs
Head Current Propagation Delay	t_{D3}	L_H = 0, R_H = 0, from 50% points		19	30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.2	1.0	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		5	8	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		16	24	

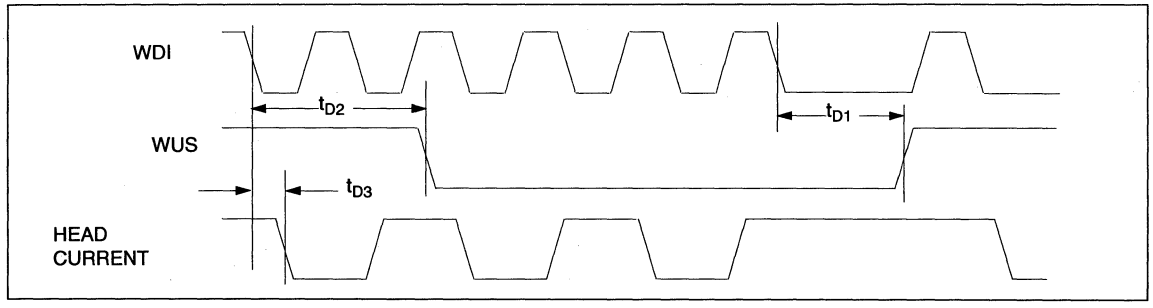


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM723430

4-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

- High Performance
  - Read Gain = 300 V/V Typical
  - Input Noise = 0.75nV/√Hz Maximum
  - Head Inductance Range = 0.2 - 10 µH
  - Write Current Range 10 - 40 mA
  - Input Capacitance = 23 pF Maximum
- Very Low Power Dissipation = 7.5 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Write Unsafe Detection
- VM723430 - Schottky Isolated 400Ω Damping Resistor
- Socket Compatible with 2020 Preamp

DESCRIPTION

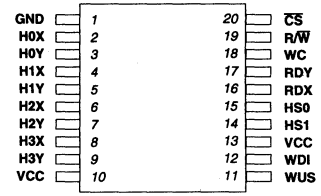
The VM723430 is a high-performance, very low-power read/write preamplifier designed for use with external thin-film recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives.

The VM723430 is plug compatible with parts using a 1:1 write current gain, while at the same time preserving the head voltage swing/switching speed advantage of VTC's VM7200.

The VM723430 provides write current and data protection circuitry, and low noise read functions for up to eight read/write heads. When deactivated, the device enters a sleep mode which reduces power dissipation to 7.5 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

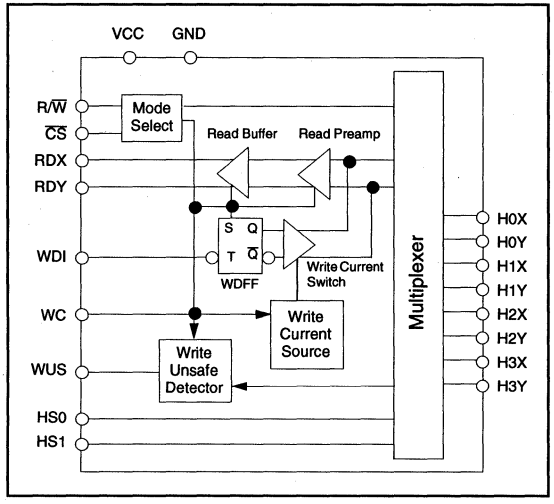
The VM723430 is available in several different packages. Please consult VTC for package availability.

CONNECTION DIAGRAM



4-Channel
20-lead SOIC, SSOP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write Current (I_W) ..... 10 to 40mA

Head Inductance (L_H) ..... 0.2 to 10µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM723430 addresses up to four 2-terminal, thin-film recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control is determined by the head select lines, HS1, HS2 and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups, provided on the $\overline{CS}$ and R/$\overline{W}$ lines, will force the device into a non-write condition if either control line opens up. The part's operation over a wide range of inductive loads makes it also suitable for non-thin-film two-terminal heads.

Write Mode

In write mode, the VM723430 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the Write Data Flip-Flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (R_{WC}) connected between the WC pin and Ground. An internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} = 1.25/R_{WC}$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- No write current
- WDI frequency too low
- Read or sleep mode
- Open head detect

Read Mode

In read mode, the VM723430 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the Pulse Detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 7.5 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low "wakes up" the chip and the device will enter the read or write mode, depending on the status of the R/W line.

Diode Connected Damping Resistor (patent pending)

The VM723430 has damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform. The VM723430 version has the damping network removed.

Input Structure:

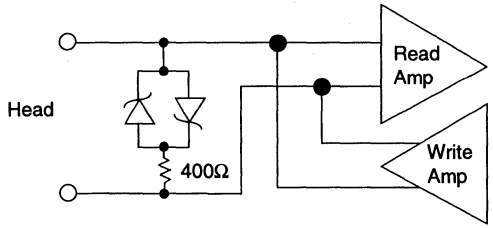


Table 1: Head Select

HS1	*HS0*	*HEAD*
0	0	0
0	1	1
1	0	2
1	1	3

Table 2: Mode Select

$\overline{CS}$	$R/\overline{W}$	*MODE*
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS1	I*	Head Select: selects one of up to four heads
H0X - H3X H0Y - H3Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
$R/\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode		$33 + I_W/4$	$42 + I_W/4$	mA
		Write Mode		$42 + 1.25I_W$	$50 + 1.25I_W$	
		Idle Mode		1.5	3	
Power Dissipation	PD	Read Mode		210	255	mW
		Write Mode, $I_W = 20mA$		370	415	
		Idle Mode		7.5	17	
Input High Voltage	V_{IH}		2		$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	$V_{IH} = 2.7V$			80	µA
Input Low Current	I_{IL}	$V_{IL} = 0.4V$	-160			µA
WUS Output Low Voltage	V_{OL}	$I_{OL} = 4.0mA$		0.35	0.5	V
WUS Output High Current	I_{OH}	$V_{OH} = 5.0V$		13	100	µA
VCC Value for Write Current Turn Off		$I_H < 0.2mA$	3.7	4.0	4.3	V

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	250	300	350	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	25	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	35	60		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.56	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		19	23	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain at 0.2mVrms input, f = 5MHz	3	6		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	73		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	70		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz. Selected channels V_{IN} = 0mVp-p	45	60		dB
Output Offset Voltage	V_{OS}		-300	25	+300	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.3		VDC
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-250	120	250	mV
Single-Ended Output Resistance	R_{SEO}			36	50	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1μH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Write Current Constant	K_W		1.15	1.25	1.35	V
Write Current Range	I_W	31.2 < R_{WC} < 125Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10 - 40mA	-8	0.5	+8	%
Differential Head Voltage Swing	V_{DH}	Open head	4	5.2		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3200			Ω
Unselected Head Current	I_{UH}	I_W = 20mA		0.15	1	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.3		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.1	1.0	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.6	1.0	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.27	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.08	0.6	µs
HS0, HS1 any Head Delay	t_{HS}	HS0, HS1 to 90% of 100mV, 10MHz read signal envelope		0.19	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	2.2	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}			0.1	1	µs
Head Current Propagation Delay	t_{D3}	L_H = 0, R_H = 0, from 50% points		19	30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time: L_H = 0, R_H = 0		0.2	1.0	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		5	8	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		16	24	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

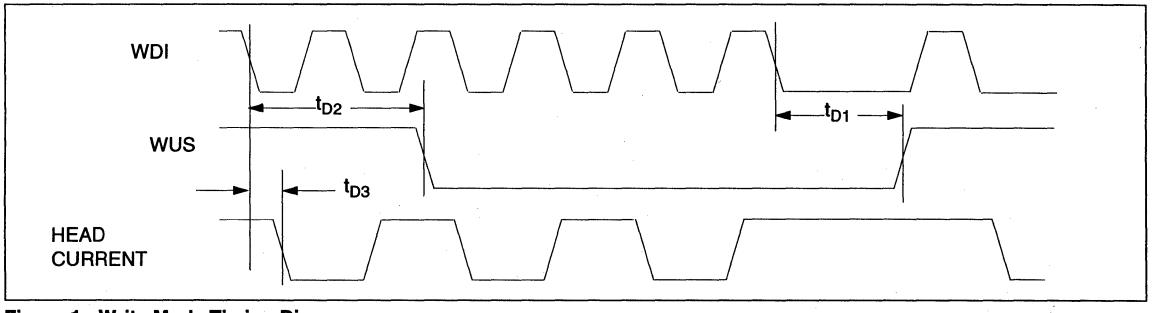


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7646

6-CHANNEL, 5-VOLT, PROGRAMMABLE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

PRELIMINARY 8/25/94

FEATURES

- Supports Recording Rates From 24 to 75 MBits/sec With No Component Changes
- Differential Write Data Input
- Programmable Write Current
- Low-Power (standby) Mode
- Mask-Programmable Write Mode Damping Resistances
- 10 MBits/sec Serial Interface for Programmability
- Programmable Disable of Write Unsafe Detector
- Supports up to Six Channels
- Supports Toggle and Non-Toggle Write Data Interface
- Available in 24 and 28-Lead SSOP

DESCRIPTION

The VM7646 is a programmable Thin-Film Read/Write preamplifier designed for use in high-performance disk drives.

A serial interface is incorporated to enable a common hardware interface for any number of heads, and to accommodate selection of heads and adjustment of write current by the microprocessor.

CIRCUIT OPERATION

The VM7646programmable preamp incorporates a serial interface to enable configuration of gain and write current as well as head selection by the microprocessor. The low-power (standby mode) is activated by the $\overline{CS}$ pin.

Both the read data output drivers and write data input receivers are differential (Pseudo ECL) for superior timing accuracy and noise immunity. An on board 4-bit DAC is used for write current control. A write unsafe detector monitors the write current amplitude and frequency and asserts a signal of programmable polarity (WUSF) when the write current is outside of the specified limits.

Serial Interface

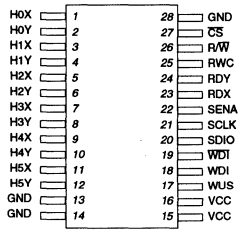
The serial interface is always available for communication between the microprocessor and the read/write device during all modes of operation. However, the serial interface pins must be kept inactive during read and write operations, to avoid any potential noise coupling.

Serial interface operations begin by sending seven bits of address and a command bit to the read write device using the SENA, SDIO and SCLK pins. The command bit indicates wether the following operation is to be a register read (cmd = 1) or register write operation (cmd = 0).

For write operations all sixteen bits (seven address, one command and eight data bits) can bit transferred continuously using the SENA, SDIO and SCLK pins.

Read operations are composed of first a transfer of seven address bits and command bit. The processor must then wait a specified amount of time (Ttrn) before clocking out the eight bits of data to be read.

CONNECTION DIAGRAM



6-Channel
28-lead SSOP

Operational Modes

The serial interface is always available for data transfer and mode control. In addition to the serial interface. The input pins $\overline{CS}$ and R/$\overline{W}$ are also available for mode control. The R/$\overline{W}$ pin selects the read or write operational modes, and the $\overline{CS}$ pin is used to select power conservation modes. Refer to Table 1.

Power down mode can only be invoked over the serial interface. (See bit 7 of config. reg. 0 in table 3). This state takes precedence over any of the other states (read, write or standby).

Special Test Modes

To enhance testing at the assembly level the $\overline{CS}$, R/$\overline{W}$, WDIX and WDIY pin states can be observed (read) using the serial interface via test register 4.

Also to enhance testing at the assembly level, a mode is available to loop the write data input pins (WDIX, WDIY) back to the read data output pins (RDX, RDY) via the LPBCK bit in test register 4.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*STBY REG. BIT*	*PDN REG. BIT*	*MODE*
0	0	0	0	Read
0	0	0	0	Write
X	0	1	0	Standby
X	1	x	0	Standby
X	X	X	1	Power Down

Table 2: Address Map Definition

A6	A5	A4	A3	A2	A1	A0	REGISTER
1	1	1	0	0	X	X	Test Reg. 0(read only)
1	1	1	0	1	X	X	Configuration Reg. 1
1	1	1	1	0	X	X	Test Reg. 2(read only)
1	1	1	1	1	X	X	Configuration Reg. 3

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
H0X - H5X H0Y - H5Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I	Differential Read Data Input
$\overline{CS}$	I	Chip Select: a programmable level activates standby mode
R/$\overline{W}$	I	Read/Write: a low-level selects write mode
WUS	O	Write Unsafe: a programmable level indicates write unsafe
SENA	I	Serial Interface Enable (high true)
SCLK	I	Serial Interface Strobe (data captured on the rising edge)
SDIO	I/O	Serial Data Bi-directional
WC	A	Connection to external resistor for current reference
RDX-RDY	O	Differential Read Data Output
VCC	P	+5 volt supply for analog, digital, driver circuits
GND	P	Ground voltage supply for analog, digital, driver circuits

I = Input, O = Output, I/O = Bidirectional, A = Analog Component Pin, P = Power Line.

Table 3: Configuration Register 3

DATA BIT	DEFINTION	FUNCTION
D0	TFD	Toggle F/F disable. (zero means toggle enabled)
D1	TMD	Activate test mode. Must be zero for normal use.
D2	WUSD	Disable the write unsafe output. (zero means enable)
D[4:3]	GSEL[1:0]	Gain select (00 = 150V/V, 01 = 200V/V, 10 = 300V/V, 11 = 400V/V)
D5	LPBCK	When true, $\overline{WDI}$, WDI pins looped back to RDX, RDY
D6	STBY	Standby mode. One means standby
D7	PDN	Power Down mode. One means power down

Table 4: Head Select Register 1

DATA BIT	DEFINTION	FUNCTION
D[0:2]	HS[0:3]	Head Select
D[4:7]	WC[0:3]	Write Current Select

Table 5: Test Register 2

DATA BIT	DEFINTION	FUNCTION
D0	WFPS	Write Fault; power supply outside of specifications flag
D1	WFIW	Write Fault: write current outside of specifications flag
D2	WFWF	Write Fault: write data input frequency is out of spec flag
D3	$\overline{CS}$	State of the $\overline{CS}$ input pin
D4	R$\overline{W}$	State of the R$\overline{W}$ input pin
D[5:6]	WDI,$\overline{WDI}$	State of the WDI and $\overline{WDI}$ input pins
D7	UNUSED	Unused (always a one)

Table 6: Test Register 0

DATA BIT	DEFINTION	FUNCTION
D[0:3]	VC[0:3]	Four bit vendor code = 001
D[4:7]	PC[0:3]	Four bit product code

DC CHARACTERISTICS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read mode, data rate = 25 - 75MB/sec		48	TBD	mA
		Write mode, data rate = 25 - 75MB/sec		50 + I_W	TBD	
		Standby mode		12	TBD	
		Power down mode'		3	TBD	
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IH} = 2.0V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.8V	-160			µA
Output High Voltage	V_{OH}	I_{OH} = 400µA	2.7			V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.5	V
Output High Current	I_{OH}	$V_{OH} = V_{CC}$		13	100	µA
PECL INPUTS						
Input High Voltage	V_{IHpe}		2			V
Input Low Voltage	V_{ILpe}				0.8	V
Input High Level Mismatch	V_{IHMpe}				100	mV
Single Ended Input Swing	V_{Spe}		300			mV
Output Low Voltage	V_{IHpe}	$V_{ILpe} = V_{CC}$ - 1.6V			80	µA
Output High Current	I_{ILpe}	$V_{IHpe} = V_{CC}$ - 0.7V			100	µA

WRITE CHARACTERISTICS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Head Voltage Swing	V_{DH}	I_W = 18.5mA,open head	TBD	6		Vp-p
Differential Output Capacitance	C_{OUT}			8	12	pF
Differential Output Resistance (note 1)	R_{OUT}	Mask programmable damping resistance	100		350	Ω
Unselected Head Current	I_{UH}	Under all conditions		20	±200	µApk
Differential Output Resistance Accuracy					20	%
Write Safe WDI Frequency Range		Over all current settings, not WUS detect	1			MHz
Write Unsafe Power Supply Limit		Hysteresis for write current turn on	3.6		4.0	V
Write Current Control Pin Voltage		1kΩ ≤ R_{WC}		2.5		V
RDX - RDY Common Mode Output				V_{CC} - 2.7		V

Note 1: six mask programmable optinos available (from 100Ω to 350Ω in 50Ω steps).

WRITE CURRENT CONTROL DAC

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range (minimum)		R_{WC} = 2.5kΩ, DAC setting = 0000	3.15	3.5	3.85	mA(pk)
Write Current Range (maximum)		R_{WC} = 2.5kΩ, DAC setting = 1111	16.5	18.5	20.5	mA(pk)
Write Current Resolution		R_{WC} = 2.5kΩ	0.9	1	1.1	mA
Write Current Gain Accuracy (note 1)		Variation of slope for least square fit line			±10	%
Write Current Offset Accuracy (note 1)		Variation of offset should track gain			±10	%
Write Current DNL (note 1)		Worst case distance from least sq. fit line			±0.25	LSB
Write Current Matching		Worst case mismatch channel to channel			±5	%

Note 1: for DAC setting, required write current is I_W = (Zero Setting Current ±10%) + [(DAC Setting)(1mA ± 10%)].

READ CHARACTERISTICS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVpp, 15MHz, read gain bits = 00	135	150	175	V/V
		V_{IN} = 1mVpp, 15MHz, read gain bits = 01	167	200	233	
		V_{IN} = 1mVpp, 15MHz, read gain bits = 10	250	300	350	
		V_{IN} = 1mVpp, 15MHz, read gain bits = 11	333	400	467	
Bandwidth (high gain mode)	BW	-1dB, V_{IN} = 1mVpp, 15MHz, read gain bits = 00	60			MHz
		-3dB, V_{IN} = 1mVpp, 15MHz, read gain bits = 00	120	160		
Bandwidth (low gain mode)	BW	-3dB, V_{IN} = 1mVpp, 15MHz, read gain bits = 11	50			MHz
		-3dB, V_{IN} = 1mVpp, 15MHz, read gain bits = 11	100	140		
Input Noise Voltage	e_{in}	L_H = 0, R_H = 0		0.5	0.6	$nV/\sqrt{Hz}$
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f =30MHz		11	TBD	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 30MHz	300	800		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input, f = 30MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	RDX = RDY = 100mVp-p f = 2 - 30MHz	45	80		dB
Power Supply Rejection Ratio	PSRR	100mVp-p, f = 2 - 30MHz on all V_{CC} lines	40	85		dB
Total Harmonic Distortion	THD	V_{IN} = 1.8mVpp, f = 2 - 30MHz			1	%
Channel Separation	CS	Unselected channels driven with V_{IN} = 0VDC + 100mVpp, f = 2 - 30MHz	45			dB
Output Offset Voltage	V_{OS}	RDX vs. RDY	-200		+200	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read mode or write mode	V_{CC} - 3.05	V_{CC} - 2.70	V_{CC} - 2.45	V
		Loopback mode	V_{CC} - 2.60	V_{CC} - 1.85	V_{CC} - 1.60	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			35	Ω
Output Current Magnitude	$\|I_O\|$	AC coupled to load , RDX and RDY	1.5			mA
Single-Ended Capacitive Load	C_L	RDY and RDX			20	pF

SWITCHING CHARACTERISTICS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read to Write	t_{RW}	RW trailing edge to 90% read amplitude		40	200	ns
Read to Standby		CS trailing edge to standby level ICC			10	µs
Read to Power Down	t_{WR}	PDN control bit to power down level ICC			10	µs
Write to Read		RW trailing edge to 90% read amplitude*		250	330	ns
Standby to Read		CS trailing edge to 90% read amplitude*			600	ns
Power Down to Read		PDN control bit to 90% read amplitude			5	ms
WUS Detect (case of loss of WDI)		Loss of WDI to WUS rising edge			1.5	µs
WUS Minimum High Pulse Width		Overall temperature and supply voltages	100			ns
Head Select	t_{HS}	Register update (note 1) to 90% of 100mV, 10NHz, read signal envelope			600	ns
Gain Charge		Register update (note 1) to 90% of 100mV, 10NHz, read signal envelope			5	µs
WDI Pulse Width		Measured at 50% points	4			µs
Write CurrentPropagation Delay		$L_H = 0$, $R_H = 0$, delay from 50% points		18	30	ns
Write Current Asymmetry	A_{SYM}	WDI has 50% duty cycle & 500ps rise/fall times, $L_H = 0$, $R_H = 0$		200	500	ps
Write Current Rise/Fall Time	t_r, t_f	$L_H = 1\mu H$, $R_H = 30\Omega$, $I_W = 10mA$b-p		5.5	8	ns
		$L_H = 0\mu H$, $R_H = 0\Omega$, $I_W = 10mA$b-p		2	4	

SERIAL INTERFACE TIMING REQUIREMENTS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
$\overline{CS}$ & R/$\overline{W}$ to SENA Rising Edge Setup Time	T_{CS}		50			ns
$\overline{CS}$ & R/$\overline{W}$ to SENA Falling Edge Hold Time	T_{CH}		50			ns
SENA to SCLK Setup Time	T_{LCS}		35			ns
SENA to SCLK to Hold Time	T_{LCH}		20			ns
SENA to First SCLK Falling Edge	T_{PDD}		200			ns
SDIO to SCLK Setup Time	T_{DCX}		15			ns
SDIO from SCLK Hold Time	T_{DCH}		10			ns
SENA to SDIO Tristate Delay	T_{ZCD}				50	ns
Ninth Low Period of SCLK	T_{TSON}	Read operation	65			
SCLK Cycle Time	T_{SCYC}		100			ns
SCLK Low Pulse Width	T_{SCHW}	Write to serial port	35			ns
	T_{SCHR}	Read from serial port	50			
SCLK High Pulse Width	T_{SCLW}	Write to serial port	35			ns
	T_{SCLR}	Read from serial port	50			

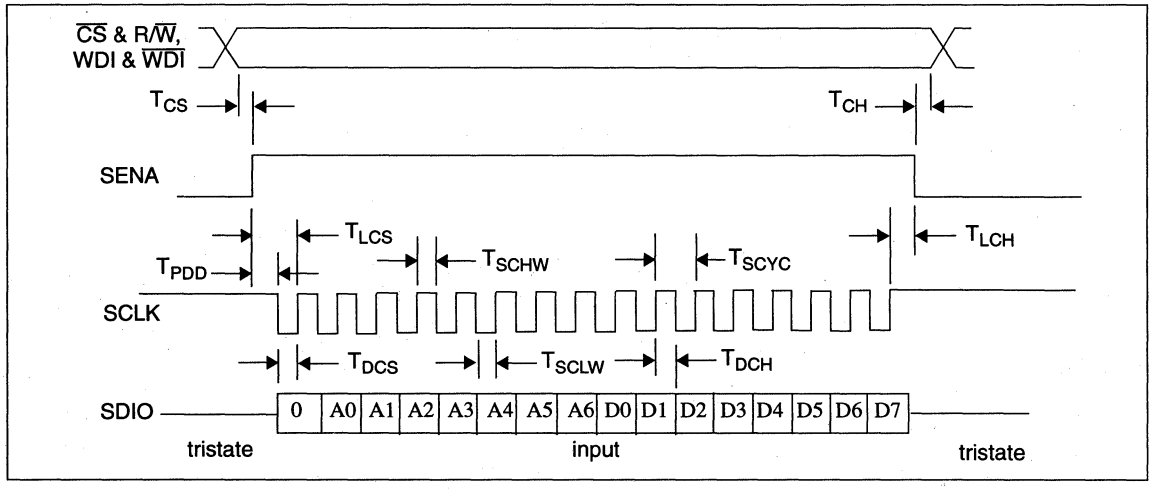


Figure 1: Serial Interface Write Timing Diagram

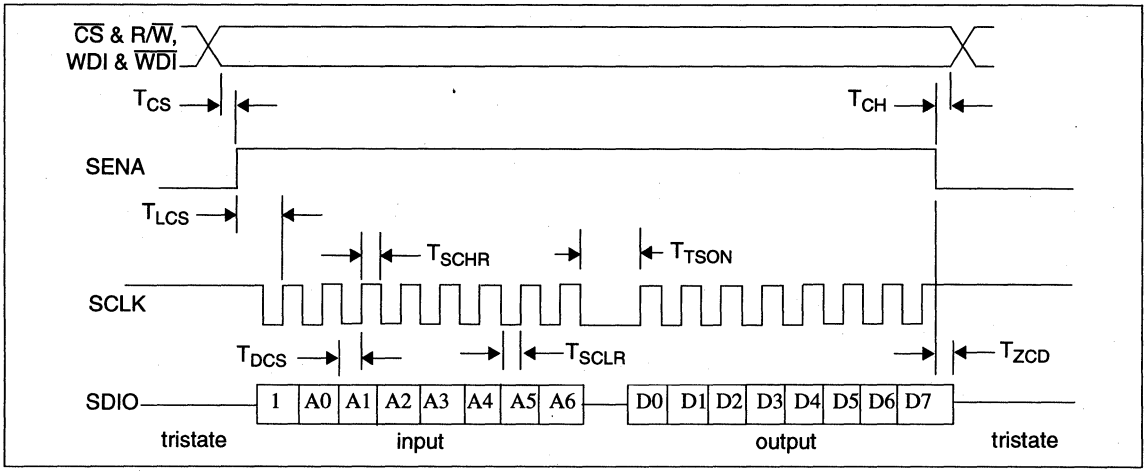


Figure 2: Serial Interface Read Timing Diagram

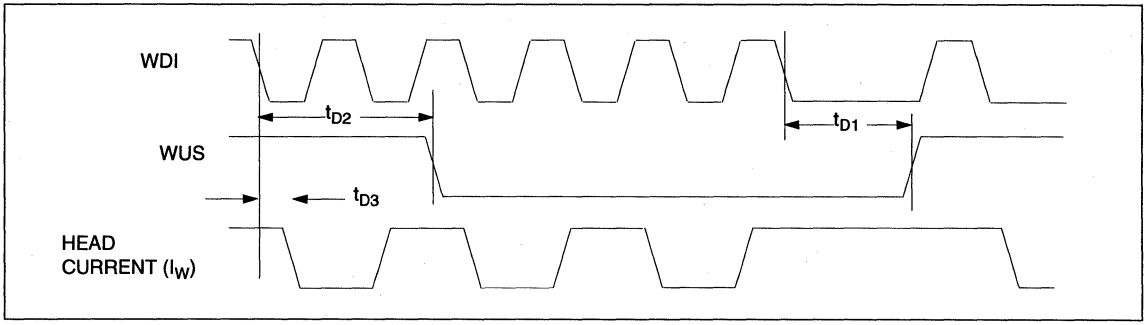


Figure 3: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7750F

4 OR 6-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH MULTIPLE SERVO WRITE CAPABILITY

PRELIMINARY

August, 1994

FEATURES

- High Performance
  - Read Gain = 300 V/V Typical
  - Input Noise = 0.49nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 0.2 – 1 µH (0.65 µH Typical)
  - IW Rise/Fall Times = 3.5 ns (L_H = 0.54 µH, I_W = 10 mA b-p)
  - Write Current Range 5 - 20 mA
  - Low Input Capacitance = 11 pF Typical
- PECL Write Data Inputs
- Multi-Channel Servo Write
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Single Power Supply = 5 V ± 10%
- Write Unsafe Detection
- Reduced Write-to-Read Recovery Time
- No Write Data Flip-Flop on Chip
- Available in 4 or 6-Channels

DESCRIPTION

The VM7750F is a high-performance read/write preamplifier designed for use in high-end disk drives. It provides write current control, data protection circuitry, and a low-noise read preamplifier for six channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 3mW.

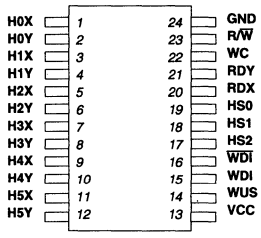
Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

Very low-power dissipation from the +5V supply is achieved through use of high-speed bipolar processing and innovative circuit design techniques.

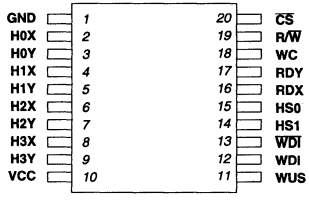
In multi-channel servo write mode, multiple heads can be written simultaneously. The VM7750F servo mode is activated via the WUS line and, when active, write all heads simultaneously.

The VM7750F is available in several different packages. Please contact VTC for package availability.

CONNECTION DIAGRAMS

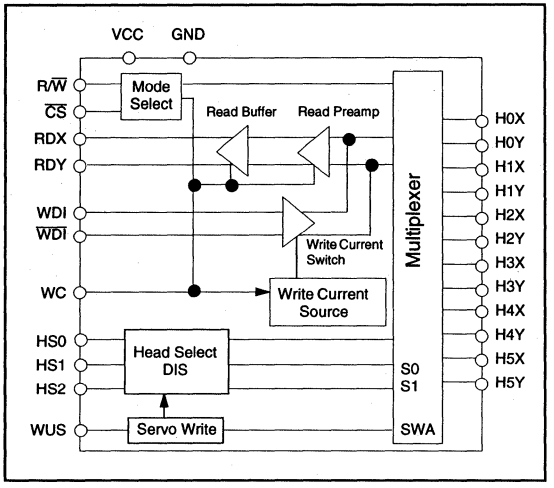


6-Channel
24-lead SSOP



4-Channel
20-lead SOIC, SSOP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 30mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature Tstg ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 24-lead SSOP ..... 100°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write current (I_W) ..... 5 to 20mA

Head Inductance (L_H) ..... 0.2 to 1µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7750F addresses up to six two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HS0, $\overline{CS}$ and R/$\overline{W}$, as shown in Table 1. Table 2 shows the head select during normal (single head) write mode. Internal resistor pull-high provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM7750F as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of a selected head on each transition on pins WDI (write data inputs). On the high-to-low transition of WDI current goes into H0Y. On the high-to-low transition of $\overline{WDI}$ current goes into H0X

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally-generated 2.5 V reference voltage is present at the WC pin. The magnitude of the write current (0-pk ±10%) is:

$$I_W = K_W/R_{WC} + 0.3mA = (50/R_{WC}) + 0.3mA \quad \textit{(eq. 1)}$$

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS. Two transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- No write current
- WDI frequency too low
- Device in read or sleep mode

Multi-Channel Servo Write Mode

In this mode, the operation is the same as described above except that multiple channels are written at the same time (see tables 1 - 3). Servo mode is controlled using the WUS pin. To initiate servo mode the following procedure is used:

1. Enter read mode via R/$\overline{W}$ high
2. Select Head 1
3. Pull WUS pin to VCC + 1.9V
4. Drop the R/$\overline{W}$ line to low

The device is now in servo mode with all six heads writing at the same time. If any other head is selected during servo the part will only write selected head. (i.e. part will fall out of servo.) To return to normal operations the following sequence is used:

1. Enter read mode
2. Drop the WUS pin (the device is in normal read mode)
3. Will also occur if any head except head 1 is selected, but will return to servo mode if HDI is reselected

Read Mode

The read mode configures the VM7750F as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to 3mW typical for sleep mode, In sleep mode, the reader outputs are high impedance. This allows multiple chip connection by simply wiring the reader outputs together.

Table 1: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
0	0	Servo
1	0	Read
X	1	Idle

Table 2: Head Selection

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I*	Head Select: selects one of up to six heads
H0X - H5X H0Y - H5Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Inputs: PECL input signal, negative transition toggles direction of head current. (every transition on "F" option)
$\overline{CS}$	I	Chip select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write unsafe: open collector output, high level indicates writes unsafe condition/also used during servo
WC		Write Current Adjust: a resistor adjusts level of write current
RDX-RDY	O*	Read Data Output: differential output data
VCC		+5 volt supply
GND		Ground

* May be wire-OR'ed for multi-chip usage.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Voltage	V_{CC}	Servo Mode	4.5	5.0	5.5	mA
VCC Supply Current	I_{CC}	Read Mode	TBD	28 + 0.05I_W	TBD	mA
		Write Mode, I_W = 10mA, Normal	TBD	26 + 1.05I_W	TBD	
		Write Mode, Servo	TBD	26 + 6.05I_W	TBD	
		Sleep Mode		0.5	TBD	
Power Supply Power Dissipation	PD	Read Mode		155	210	mW
		Write Mode, I_W = 10mA, Normal		200	240	
		Write Mode, Servo		475	TBD	
		Sleep Mode		3	TBD	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.5		V_{CC} - 0.5	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{IH} - 1.5		V_{IH} - 0.5	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	V_{IH} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.3	3.6	4.0	V
WUS Servo Enable				V_{CC} +1.9		

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; L_H = 0.650µH, R_H = 35Ω, I_W = 120mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}		2.2	2.5	2.9	V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	V_{CC} = 5V ±10%	46	50	54	V
Write Current Range	I_W	9.95K > R_{WC} > 1.42Ω	5		20	mA
Write Current Tolerance	ΔI_W	V_{CC} ±10%	-8		+8	%
Differential Head Voltage Swing	V_{DH}	Open head	5.7	6.4		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
Unselected Head Current	I_{UH}	I_W = 20mA		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	275	300	325	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	35			MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	65			
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.49	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		11	15	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	700		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}	Steady state read	-250		250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
RDX, RDY Common Mode Output Voltage Difference Between Modes	ΔV_{OCM}	100mVp-p @ 5MHz on V_{CC}	-350		+350	mV
Single-Ended Output Resistance	R_{SEO}	f = MHz			35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

Servo Five Channels Write

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 35mA			10	%
Duty Cycle (25mA/head)					20	%

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 10mA, f_{DATA} = 5MHz, L_H = 0.650µH, R_H = 35Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* (Note 1)	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.1	0.3	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.3	0.6	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0 - HS3 any Head Delay	t_{HS}	HS0 - HS3 to 90% of 100mV, 10MHz read signal envelope			0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6		3.6	µs
WUS Unsafe to Safe Delay	t_{D2}	I_W = 10mA			1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.5	4	ns
		10% to 90% points, L_H = 540nH, I_W = 10mA, R_H = 20Ω		3.5	6	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

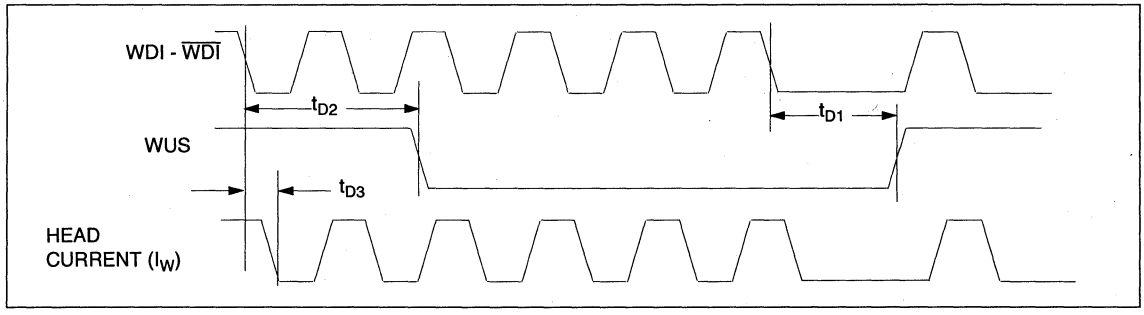


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM7800

4, 6, OR 10-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH MULTIPLE SERVO WRITE CAPABILITY

August, 1994

FEATURES

- High Performance
  - Read Gain Options = 150 - 300 V/V Typical
  - Input Noise = 0.55nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 0.2 – 5 µH (0.5 µH typical)
  - IW Rise/Fall Times = 9 ns (L_H = 1 µH, I_W = 20 mA b-p)
  - Write Current Range 5 - 35 mA
  - Low Input Capacitance = 14 pF Typical
  - Head Voltage Swing = 8.8 Vpp Typical
- PECL Write Data Inputs
- Multi-Channel Servo Write Available
- Very Low Power Dissipation = 1 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Single Power Supply = 5 V ± 10%
- Write Unsafe Detection
- Fast Write-to-Read Recovery Time
- Available in 4, 6, or 10-Channels

DESCRIPTION

The VM7800 is a high-performance read/write preamplifier designed for use in high-end disk drives. It provides write current control, data protection circuitry, and a low-noise read preamplifier for ten channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 1mW.

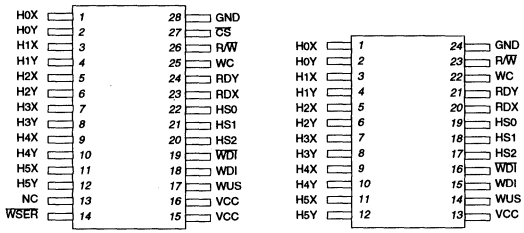
Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

Very low-power dissipation from the +5V supply is achieved through use of high-speed bipolar processing and innovative circuit design techniques.

In multi-channel servo write mode, multiple heads can be written simultaneously. The 4- and 6-channel VM7800 devices have an active low servo-write enable ($\overline{WSER}$) and, when active, write all heads simultaneously. The 10-channel VM7800 device has an active high servo-write enable (WSER) and, when active, writes all even or odd heads simultaneously depending on the state of the head select zero pin (HS0). An internal resistor pulls up or down pin $\overline{WSER}$/WSER so that when it is left open, the chip will be in normal single head write mode.

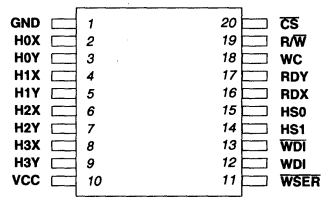
The VM7800 is available in several different packages. Not all of the VM7800 features are available in every package style. Please contact VTC for package availability.

CONNECTION DIAGRAMS

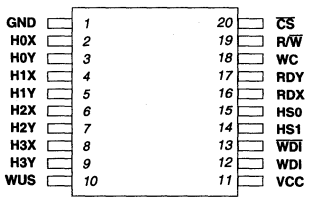


VM7856
6-Channel
28-lead SSOP

VM7806
6-Channel
24-lead SSOP



VM7854
4-Channel
20-lead SOIC



VM7804
4-Channel
20-lead SOIC

For additional connection diagrams see the last page of this datasheet.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Write Current I_W 60mA
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V
Output Current:
RDX, RDY: I_O .....-10mA
WUS: I_{WUS} ..... +12mA
Junction Temperature ..... 150°C
Storage Temperature Tstg ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
20-lead SOIC ..... 90°C/W
24-lead SSOP ..... 100°C/W
28-lead SSOP ..... 100°C/W
36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Write current (I_W) ..... 5 to 35mA
Head Inductance (L_H) ..... 0.2 to 5µH
Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7800 addresses up to ten two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins WSER/$\overline{\text{WSER}}$, HS0, $\overline{\text{CS}}$ and R/$\overline{\text{W}}$, as shown in Tables 1 and 4. Tables 2 and 3 shows the head select during servo write mode. Internal resistor pull-high provided on pins $\overline{\text{CS}}$ and R/$\overline{\text{W}}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM7800 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of a selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally-generated 2.5 V reference voltage is present at the WC pin. The magnitude of the write current (0-pk ±10%) is:

$$I_W = K_W/R_{WC} + 0.2mA = 50/R_{WC} + 0.2mA \qquad \textit{(eq. 1)}$$

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Multi-write mode
- No write current
- WDI frequency too low
- Device in read or sleep mode

Multi-Channel Servo Write Mode

In this mode, the operation is the same as described above except that multiple channels are written at the same time (see tables 1 - 3). Pin WSER/$\overline{\text{WSER}}$ would be high/low to enable the multi-write feature. Pin HS0 is used on the 10-channel VM7800 to select which bank of five heads are written simultaneously.

Read Mode

The read mode configures the VM7800 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Idle Mode

When $\overline{\text{CS}}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to 1mW typical for sleep mode, In sleep mode, the reader outputs are high impedance. This allows multiple chip connection by simply wiring the reader outputs together.

Table 1: Mode Select

R/$\overline{\text{W}}$	*$\overline{\text{CS}}$*	*WSER*	*$\overline{\text{WSER}}$*	*MODE*
0	0	0	1	Write Single
0	0	1	0	Write Servo
1	0	X	X	Read
X	1	X	X	Idle

Table 2: Head Selection in Servo Write Mode (WSER = high) 10-Channel

HS0	*WSER*	*HEAD*
0	1	0, 2, 4, 6, 8
1	1	1, 3, 5, 7, 9

Table 3: Head Selection in Servo Write Mode ($\overline{\text{WSER}}$ = low) 4 and 6-Channel

CHANNELS	*$\overline{\text{WSER}}$*	*HEAD*
4	0	0, 1, 2, 3
6	0	0, 1, 2, 3, 4, 5

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Table 4: Head Selection

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to ten heads
H0X - H9X H0Y - H9Y	I/O	X, Y Head Terminals
WDI, $\overline{\text{WDI}}$	I*	Write Data Inputs: PECL input signal, negative transition toggles direction of head current.
$\overline{\text{CS}}$	I	Chip select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{\text{W}}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX-RDY	O*	Read Data Output: differential output data
VCC		+5 volt supply**
GND		Ground
WSER	I*	Servo Write: a high level enables servo mode for 10-channel VM7800
$\overline{\text{WSER}}$	I*	Servo Write: a low level enables servo mode for 4 and 6-channel VM7800

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	mA
VCC Supply Current	I_{CC}	Read Mode		58	70	mA
		Write Mode, Normal	44 + I_W	57 + I_W	70 + I_W	
		Write Mode, Servo	65 +5*I_W	100 +5*I_W	120 +5*I_W	
		Sleep Mode		9.5	12	
Power Supply Power Dissipation	PD	Read Mode		320	385	mW
		Write Mode, I_W = 20mA, Normal		421	495	
		Write Mode, Servo		1100	1210	
		Sleep Mode		52	66	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	V_{IH} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.3	3.6	3.9	V

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* (Note 1)	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	V_{CC} = 5V, I_W = 5 - 30mA	41	50	59	V
Write Current Range	I_W	9.95K > R_{WC} > 1.42Ω	5		35	mA
Write Current Tolerance	ΔI_{WI}	V_{CC} = 5V, 5 < I_W < 30mA	-18		+18	%
		V_{CC} = 5V, 30mA < I_W < 35mA	-20	-8	+5	%
Write Current Supply Sensitivity	$\Delta I_W/V$	V_{CC} = 5V ±10%	-6	3	+6	%
Differential Head Voltage Swing	V_{DH}	Open head	7	8.8		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
Unselected Head Current	I_{UH}	I_W = 20mA		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* (Note 1)	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	168	200	232	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	55	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		14	16	pF
Differential INput Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	800		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}		-200		+200	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
RDX, RDY Common Mode Output Voltage Difference	ΔV_{OCM}	100mVp-p @ 5MHz on V_{CC}	-350		+350	mV
Single-Ended Output Resistance	R_{SEO}	f = MHz		15	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

Servo Five Channels Write

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 35mA			22	%
Duty Cycle (25mA/head)					20	%
Write Current Tolerance		5mA < I_W < 35mA, V_{CC} = 5V	-24		+24	%

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* (Note 1)	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.04	0.2	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.3	0.5	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0 - HS3 any Head Delay	t_{HS}	HS0 - HS3 to 90% of 100mV, 10MHz read signal envelope			0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6		3.6	µs
WUS Unsafe to Safe Delay	t_{D2}	I_W = 35mA			1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			1.0	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.5	4	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		9	12	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

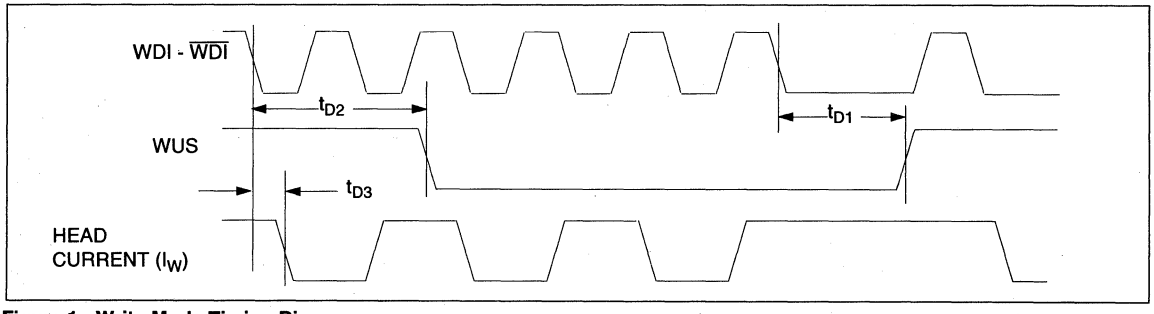
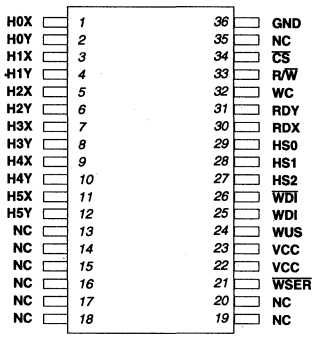
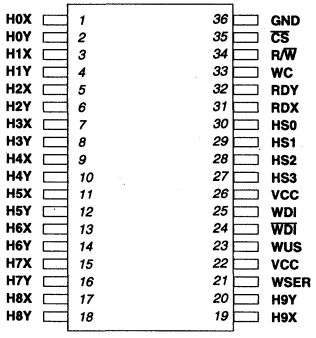


Figure 1: Write Mode Timing Diagram

ADDITIONAL CONNECTION DIAGRAMS



VM7856
6-Channel
36-lead SOIC



VM78510
10-Channel
36-lead SOIC

VTC Inc.
Value the Customer™

VM782020

20-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August,1994

FEATURES

- High Performance
  - Read Gain = 200 V/V Typical
  - Input Noise = 0.55nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 0.2 – 5 µH (0.5 µH Typical)
  - IW Rise/Fall Times = 9 ns (L_H = 1 µH, I_W = 20 mA b-p)
  - Write Current Range 5 - 35 mA
  - Low Input Capacitance = 14 pF Typical
  - Head Voltage Swing = 8.8 Vpp Typical
- PECL Write Data Inputs
- Very Low Power Dissipation = 1 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Single Power Supply = 5 V ± 10%
- Write Unsafe Detection
- Fast Write-to-Read Recovery Time

DESCRIPTION

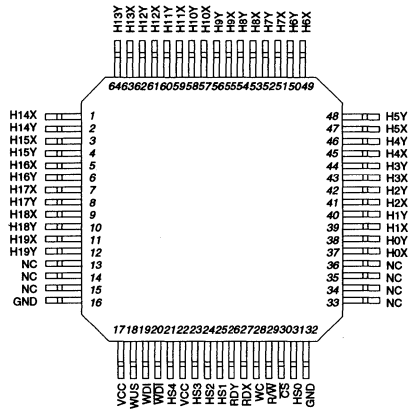
The VM782020 is a high-performance read/write preamplifier designed for use in high-end disk drives. It provides write current control, data protection circuitry, and a low-noise read preamplifier for 20-channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 1mW.

Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

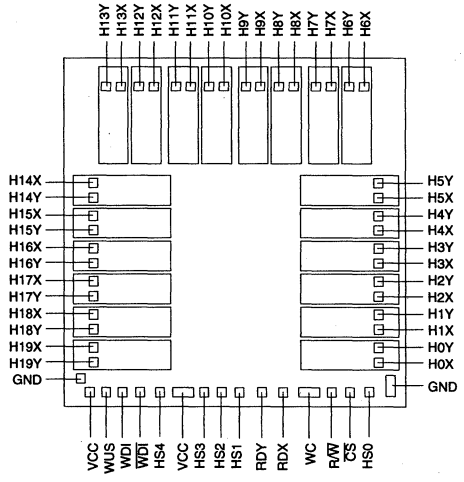
Very low-power dissipation from the +5V supply is achieved through use of high-speed bipolar processing and innovative circuit design techniques.

The VM782020 is available in a 64-lead TQFP and in die form. Please contact VTC for package availability.

CONNECTION DIAGRAMS



VM782020
20-Channel
64-lead TQFP



VM782020
Die Size = .160" x .164"

ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Write Current I_W 60mA
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V
Output Current:
RDX, RDY: I_O .....-10mA
WUS: I_{WUS} ..... +12mA
Junction Temperature ..... 150°C
Storage Temperature Tstg ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
64-lead PQFP ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Write current (I_W) ..... 5 to 35mA
Head Inductance (L_H) ..... 0.2 to 5µH
Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM782020 addresses up to 20 two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HS0, $\overline{CS}$ and R/$\overline{W}$, as shown in Table 1. Table 2 shows the head select during servo write mode. Internal resistor pull-high provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM782020 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of a selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally-generated 2.5 V reference voltage is present at the WC pin. The magnitude of the write current (0-pk ±10%) is:

$$I_W = K_W/R_{WC} + 0.2mA = 50/R_{WC} + 0.2mA \qquad (eq.\ 1)$$

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Multi-write mode
- No write current
- WDI frequency too low
- Device in read or sleep mode

Read Mode

The read mode configures the VM782020 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to 1mW typical for sleep mode, In sleep mode, the reader outputs are high impedance. This allows multiple chip connection by simply wiring the reader outputs together.

Table 1: Mode Select

R/$\overline{W}$	$\overline{CS}$	MODE
0	0	Write Single
1	0	Read
X	1	Idle

Table 2: Head Selection

HS4	HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS4	I*	Head Select: selects one of up to 20 heads
H0X - H19X H0Y - H19Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Inputs: PECL input signal, negative transition toggles direction of head current.
$\overline{CS}$	I	Chip select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX-RDY	O*	Read Data Output: differential output data
VCC		+5 volt supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	mA
VCC Supply Current	I_{CC}	Read Mode, I_W = 20mA		48	60	mA
		Write Mode, Normal, I_W = 20mA		48 + I_W	60 + I_W	
		Sleep Mode		0.5	6	
Power Supply Power Dissipation	PD	Read Mode		240	330	mW
		Write Mode, I_W = 20mA, Normal		340	440	
		Sleep Mode		2.5	33	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	V_{IH} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.3	3.6	3.9	V

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	V_{CC} = 5V, I_W = 5 - 30mA	41	50	59	V
Write Current Range	I_W	9.95K > R_{WC} > 1.42Ω	5		35	mA
Write Current Tolerance	ΔI_{WI}	V_{CC} = 5V, 5 < I_W < 30mA	-18		+18	%
		V_{CC} = 5V, 30mA < I_W < 35mA	-20	-8	+5	%
Write Current Supply Sensitivity	$\Delta I_W/V$	V_{CC} = 5V ±10%	-6	±3	+6	%
Differential Head Voltage Swing	V_{DH}	Open head	7	8.8		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		1.6			kΩ
Unselected Head Current	I_{UH}	I_W = 20mA		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	168	200	232	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	55	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		14	16	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	800		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}		-200		+200	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
RDX, RDY Common Mode Output Voltage Difference	ΔV_{OCM}	100mVp-p @ 5MHz on V_{CC}	-350		+350	mV
Single-Ended Output Resistance	R_{SEO}	f = 5MHz		15	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.04	0.2	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.3	0.5	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0 - HS4 any Head Delay	t_{HS}	HS0 - HS4 to 90% of 100mV, 10MHz read signal envelope			0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6		3.6	µs
WUS Unsafe to Safe Delay	t_{D2}				1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			1.0	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.5	4	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		9	12	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

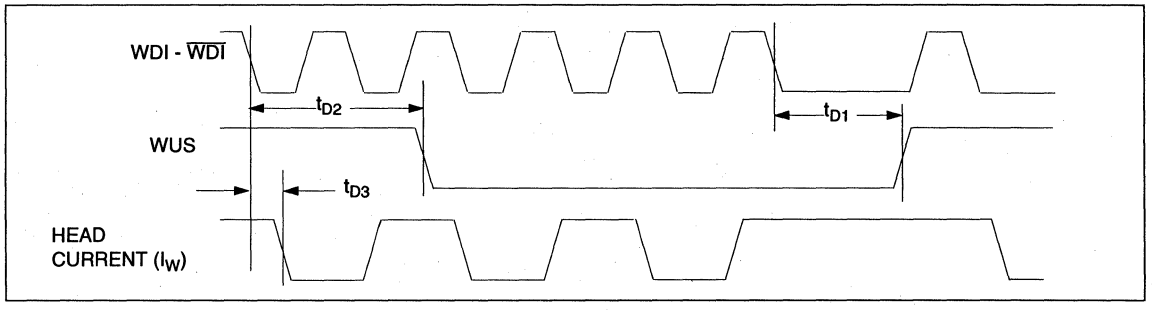


Figure 1: Write Mode Timing Diagram

3 Three-Terminal Preamplifiers

Three-Terminal High-Performance Center-Tapped Read/Write Preamplifiers

VTC Inc.
Value the Customer™

VM367

4-CHANNEL, CENTER-TAPPED FERRITE, THIN-FILM AND MIG HEAD, READ/WRITE PREAMPLIFIER

August,1994

FEATURES

- High Performance
  - Read Gain = 250 V/V Typical
  - Input Noise = 0.72nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 1 – 10 µH
  - I_W Current Range 8 - 40 mA
  - Input Capacitance = 18 pF Typical
- Very Low Power Dissipation = 10 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Power Supply V_{CC} = 5 V ± 10%
- TTL Write Data Input

DESCRIPTION

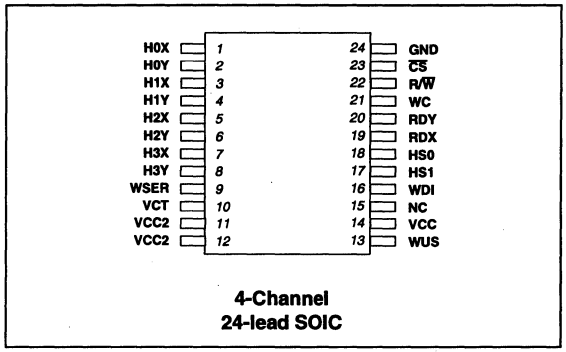
The VM367 is a four-channel low-power, bipolar monolithic servo read/write preamplifier designed for use with three-terminal center-tapped ferrite or MIG recording heads.

It has a TTL inputs for the write data. It provides write current control, data protection circuitry, and a low-noise read preamplifier for four channels. When unselected, the device enters a sleep mode, with power dissipation reduced to 10mW.

Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

In servo write mode, four channels are active at the same time. Pin $\overline{WSER}$ controls the servo mode. When it is low, the chip is in servo write mode: four channels are written at the same time. When it is high, the chip is in normal write mode: one head is written at one time. An internal resistor pulls up pin $\overline{WSER}$ so that when it is left open, the chip will be in normal single head write mode.

CONNECTION DIAGRAM



4-Channel
24-lead SOIC

THREE-TERMINAL PREAMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7VDC

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} .....-0.3V to (V_{CC} + 0.3)VDC
- Head Port Voltage V_H .....-0.3V to (V_{CC} + 0.3)VDC

Write Unsafe (WUS) ..... -0.3V to 10VDC

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Storage Temperature Range ..... -65° to 150°C

Lead Temperature (soldering 60 sec) ..... 300°C

Thermal Characteristics, Θ_{JA}:
- 24-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%
- V_{CC2} .....+5V ± 10%

Write Current (I_W) ..... 8 to 40mA

Head Inductance (L_H) ..... 1 to 5µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM367 addresses four three-terminal heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins $\overline{WSER}$, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pulled-up provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM367 as a current switch. Write current is toggled between the X and Y direction of a selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally-generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk ±12%) is:

$$I_W = K_W/R_{WC} = 50/R_{WC} + 0.2mA$$

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag. It is an optional mask for this feature if TTL write data input is used.

The fault detections are:

- Servo write mode
- No write current
- WDI frequency too low
- Device in read or sleep mode
- Open and short head
- Open and short center-tap voltage pin
- Power supply

Write Servo Mode

In this mode, the operation is the same as described above except that four channels are written at the same time. Pin $\overline{WSER}$ would be low to enable the servo write feature.

Read Mode

The read mode configures the VM367 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to 10mW typical for sleep mode. In sleep mode, the reader outputs are high impedance. This allows multiple chip connection by simply wiring the reader outputs together.

Table 1: Mode Selection Active Low $\overline{WSER}$

R/$\overline{W}$	*$\overline{CS}$*	*$\overline{WSER}$*	*MODE*
0	0	1	Write Single
1	0	X	Read
X	1	X	Idle
0	0	0	Write Servo (heads (0,1,2,3)

Table 2: Head Selection

HS1	*HS0*	*HEAD*
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS1	I*	Head Select: selects one of four heads
H0X - H3X H0Y - H3Y	I/O	X, Y Head Terminals
WDI	I*	Write Data Input: negative transition (WDI) toggles direction of head current.
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX-RDY	O*	Read Data Output: differential output data
VCT		Voltage Center Tap: voltage bias for head center tap
VCC		+5 volt supply**
VCC2		+5 volt supply
GND		Ground
$\overline{WSER}$	I*	Servo Write: a low level enables servo mode

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
POWER SUPPLY						
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
	V_{CC2}	Servo Mode	4.5		8.5	
		Normal Mode	4.5		13.2	
VCC Supply Current	I_{CC}	Read Mode		48	55	mA
		Write Mode, Normal		30	55	
		Write Mode, Servo		35	58	
		Idle Mode		1	4	
VCC2 Supply Current	I_{CC2}	Read Mode		1.4	5	mA
		Write Mode, Normal		$7 + I_W$	$20 + I_W$	
		Write Mode, Servo		$15 + 4I_W$	$27 + 4I_W$	
		Idle Mode		0.14	0.2	
Power Supply Power Dissipation	PD	Read Mode		276	300	mW
		Write Mode, I_W = 20mA		320	410	
		Idle Mode		10	15	
DIGITAL TTL INPUTS: $\overline{CS}$, R/$\overline{W}$, HS, WDI						
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.5V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.5V	-160			µA
WUS OUTPUT						
Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
POWER SUPPLY FAULT VOLTAGE						
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.5	4.0	4.3	V

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WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; L_H = 150nH, R_H = 20Ω, I_W = 40mA, single-ended, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
NORMAL SINGLE CHANNEL						
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W		44	50	56	V
Write Current Range	I_W	12.5kΩ > R_{WC} > 1.66kV	8		40	mA
Write Current Tolerance	ΔI_W	8mA < I_W < 35mA	-12		12	%
Write Current Pin Voltage	V_{CM}			2.5		V
Differential Head Voltage Swing	V_{DH}	L_H = 10µH, R_H = 0Ω	V_{CC}	2(V_{CC} - 2.5)		Vb-p
WDI Transition Frequency	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
Unselected Head Current	I_{UH}	I_W = 15mA		±0.2	1	mA(pk)
Center-Tap Voltage	V_{CT}			V_{DD} - 0.2		
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V
SERVO FOUR CHANNELS						
Write Current Matching Between Channels	D_{IW}				15	%

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, @1MHz	208	250	291	V/V
Bandwidth (-3 dB)	BW	-1dB |Zsl < 5V, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zsl < 5V, V_{IN} = 1mVp-p	55	75		
Dynamic Range	DR	AC Input Voltage Where A_V Gain Falls 90% @ V_{IN} = 0.2Vrms, 5MHz	2			mVrms
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.72	0.95	nV/$\sqrt{Hz}$
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		18	22	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	400	1000	1800	Ω
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}			±250		mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
Read to Write Common Mode Output Voltage	ΔV_{OCM}	100mVp-p @ 5MHz on V_{CC}	-350		+350	mV
Single-Ended Output Resistance	R_{SEO}				35	V
Output Load Current	I_{OUT}	AC coupled load, RDX to RDY	±1.5			mA
Center-Tapped Voltage in Read				V_{CC} - 2.4V		

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SWITCHING CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read-to-Write Switching	t_{RW}	50% of R/$\overline{W}$ to 90% of Write Output Envelope		50	300	ns
Write-to-Read Switching Delay	t_{WR}	50% of R/$\overline{W}$ to 90% of 100mVp-p RDX, RDY Envelope		0.3	0.6	µs
Idle-to-Read Switching	t_{IR}	50% of $\overline{CS}$ to 90% of 100mVp-p RDX, RDY Envelope			0.6	µs
Read-to-Idle Switching Delay	t_{RI}	50% of $\overline{CS}$ to 10% of RDX, RDY Envelope			0.6	µs
Head Select Switching Delay	t_{HS}	50% of HS Transition to 90% of 100mVp-p RDX, RDY Envelope from Selected Head			0.6	µs
Write Unsafe Delay Safe-to Unsafe	t_{D1}	I_W = 35mA	0.6		3.6	µs
Write Unsafe Delay Unsafe-to-Safe	t_{D2}	I_W = 35mA			1.0	µs
Head Current Propagation Delay	t_{D3}	L_H = 0			30	ns
Head Current Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time; L_H = 0			1.0	ns
Head Current Rise/Fall Time	t_r/t_f	L_H = 1µH, R_H = 30Ω, I_W = 15µAb-p		7	TBD	ns

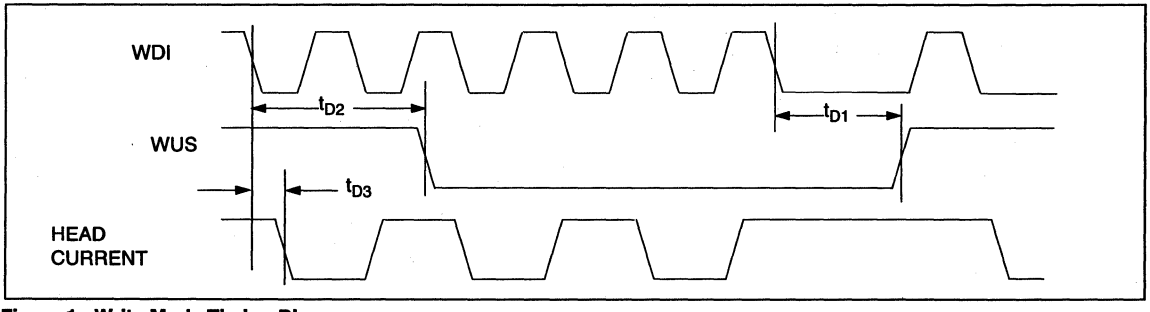


Figure 1: Write Mode Timing Diagram

VTC Inc.
Value the Customer™

VM367N225

2-CHANNEL, CENTER-TAPPED FERRITE, THIN-FILM AND MIG HEAD, READ/WRITE PREAMPLIFIER

August,1994

FEATURES

- High Performance
  - Read Gain = 250 V/V Typical
  - Input Noise = 0.72nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 1 – 10 µH
  - I_W Current Range 4 - 40 mA
  - Input Capacitance = 18 pF Typical
- Very Low Power Dissipation = 10 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Power Supply V_{CC} = 5 V ± 10%
- TTL Write Data Input

DESCRIPTION

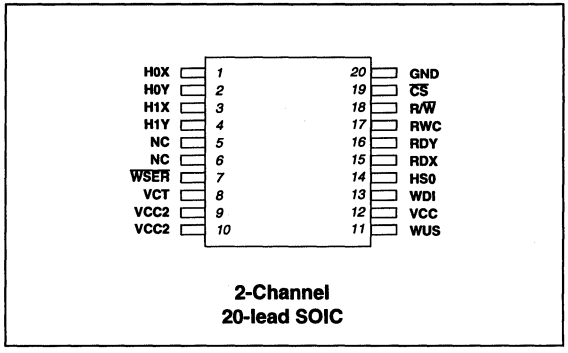
The VM367N225 is a two-channel low-power, bipolar monolithic servo read/write preamplifier designed for use with three-terminal center-tapped ferrite or MIG recording heads.

It has a TTL inputs for the write data. It provides write current control, data protection circuitry, and a low-noise read preamplifier for two channels. When unselected, the device enters a sleep mode, with power dissipation reduced to 10mW.

Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

In servo write mode, two channels are active at the same time. Pin $\overline{WSER}$ controls the servo mode. When it is low, the chip is in servo write mode: two channels are written at the same time. When it is high, the chip is in normal write mode: one head is written at one time. An internal resistor pulls up pin $\overline{WSER}$ so that when it is left open, the chip will be in normal single head write mode.

CONNECTION DIAGRAM



2-Channel
20-lead SOIC

ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7VDC
Write Current I_W 60mA
Input Voltages:
Digital Input Voltage V_{IN} .....-0.3V to (V_{CC} + 0.3)VDC
Head Port Voltage V_H .....-0.3V to (V_{CC} + 0.3)VDC
Write Unsafe (WUS) ..... -0.3V to 10VDC
Output Current:
RDX, RDY: I_O .....-10mA
WUS: I_{WUS} ..... +12mA
Storage Temperature Range ..... -65° to 150°C
Lead Temperature (soldering 60 sec) ..... 300°C
Thermal Characteristics, Θ_{JA}:
20-lead SOIC ..... 90°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
V_{CC2} .....+5V ± 10%
Write Current (I_W) ..... 4 to 40mA
Head Inductance (L_H) ..... 1 to 5µH
Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM367N225 addresses up to two three-terminal heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins $\overline{WSER}$, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pulled-up provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM367N225 as a current switch. Write current is toggled between the X and Y direction of a selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally-generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk ±12%) is:

$$I_W = K_W/R_{WC} = 50/R_{WC} + 0.2mA$$

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag. It is an optional mask for this feature if TTL write data input is used.

The fault detections are:

- Servo write mode
- No write current
- WDI frequency too low
- Device in read or sleep mode
- Open and short head
- Open and short center-tap voltage pin
- Power supply

Write Servo Mode

In this mode, the operation is the same as described above except that four channels are written at the same time. Pin $\overline{WSER}$ would be low to enable the servo write feature.

Read Mode

The read mode configures the VM367N225 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to 10mW typical for sleep mode. In sleep mode, the reader outputs are high impedance. This allows multiple chip connection by simply wiring the reader outputs together.

Table 1: Mode Selection Active Low $\overline{WSER}$

R/$\overline{W}$	*$\overline{CS}$*	*$\overline{WSER}$*	*MODE*
0	0	1	Write Single
1	0	X	Read
X	1	X	Idle
0	0	0	Write Servo (heads (0,1)

Table 2: Head Selection

HS0	*HEAD*
0	0
1	1

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0	I*	Head Select: selects one of up to two heads
H0X - H1X H0Y - H1Y	I/O	X, Y Head Terminals
WDI	I*	Write Data Input: negative transition (WDI) toggles direction of head current.
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX-RDY	O*	Read Data Output: differential output data
VCT		Voltage Center Tap: voltage bias for head center tap
VCC		+5 volt supply**
VCC2		+5 volt supply
GND		Ground
$\overline{WSER}$	I*	Servo Write: a low level enables servo mode

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
POWER SUPPLY						
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
	V_{CC2}	Servo Mode	4.5		8.5	
		Normal Mode	4.5		13.2	
VCC Supply Current	I_{CC}	Read Mode		48	55	mA
		Write Mode, Normal		30	55	
		Write Mode, Servo		35	58	
		Idle Mode		1	4	
VCC2 Supply Current	I_{CC2}	Read Mode		1.4	5	mA
		Write Mode, Normal		$7 + I_W$	$20 + I_W$	
		Write Mode, Servo		$15 + 4I_W$	$27 + 4I_W$	
		Idle Mode		0.14	0.2	
Power Supply Power Dissipation	PD	Read Mode		276	300	mW
		Write Mode, I_W = 20mA		320	410	
		Idle Mode		10	15	
DIGITAL TTL INPUTS: $\overline{CS}$, R/$\overline{W}$, HS, WDI						
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.5V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.5V	-160			µA
WUS OUTPUT						
Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
POWER SUPPLY FAULT VOLTAGE						
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.5	4.0	4.3	V

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WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; L_H = 150nH, R_H = 20Ω, I_W = 40mA, single-ended, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
NORMAL SINGLE CHANNEL						
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W		44	50	56	V
Write Current Range	I_W	12.5kΩ > R_{WC} > 1.66kV	4		40	mA
Write Current Tolerance	ΔI_W	5mA < I_W < 35mA	-12		12	%
Write Current Pin Voltage	V_{CM}			2.5		V
Differential Head Voltage Swing	V_{DH}	L_H = 10µH, R_H = 0Ω	V_{CC}	2(V_{CC} - 2.5)		Vb-p
WDI Transition Frequency	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
Unselected Head Current	I_{UH}	I_W = 15mA		±0.2	1	mA(pk)
Center-Tap Voltage	V_{CT}			V_{DD} - 0.2		
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V
SERVO FOUR CHANNELS						
Write Current Matching Between Channels	D_{IW}				15	%

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, @1MHz	208	250	292	V/V
Bandwidth (-3 dB)	BW	-1dB |Zsl < 5V, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zsl < 5V, V_{IN} = 1mVp-p	55	75		
Dynamic Range	DR	AC Input Voltage Where A_V Gain Falls 90% @ V_{IN} = 0.2Vrms, 5MHz	2			mVrms
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.72	0.95	nV/$\sqrt{Hz}$
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		18	22	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	400	1000	1800	Ω
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}			±250		mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
Read to Write Common Mode Output Voltage	ΔV_{OCM}	100mVp-p @ 5MHz on V_{CC}	-350		+350	mV
Single-Ended Output Resistance	R_{SEO}				35	V
Output Load Current	I_{OUT}	AC coupled load, RDX to RDY	±1.5			mA
Center-Tapped Voltage in Read				V_{CC} - 2.4V		

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SWITCHING CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read-to-Write Switching	t_{RW}	50% of R/$\overline{W}$ to 90% of Write Output Envelope		50	300	ns
Write-to-Read Switching Delay	t_{WR}	50% of R/$\overline{W}$ to 90% of 100mVp-p RDX, RDY Envelope		0.3	0.6	µs
Idle-to-Read Switching	t_{IR}	50% of $\overline{CS}$ to 90% of 100mVp-p RDX, RDY Envelope			0.6	µs
Read-to-Idle Switching Delay	t_{RI}	50% of $\overline{CS}$ to 10% of RDX, RDY Envelope			0.6	µs
Head Select Switching Delay	t_{HS}	50% of HS Transition to 90% of 100mVp-p RDX, RDY Envelope from Selected Head			0.6	µs
Write Unsafe Delay Safe-to Unsafe	t_{D1}	I_W = 35mA	0.6		3.6	µs
Write Unsafe Delay Unsafe-to-Safe	t_{D2}	I_W = 35mA			1.0	µs
Head Current Propagation Delay	t_{D3}	L_H = 0			30	ns
Head Current Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time; L_H = 0			1.0	ns
Head Current Rise/Fall Time	t_r/t_f	L_H = 1µH, R_H = 30Ω, I_W = 15µAb-p		7	TBD	ns

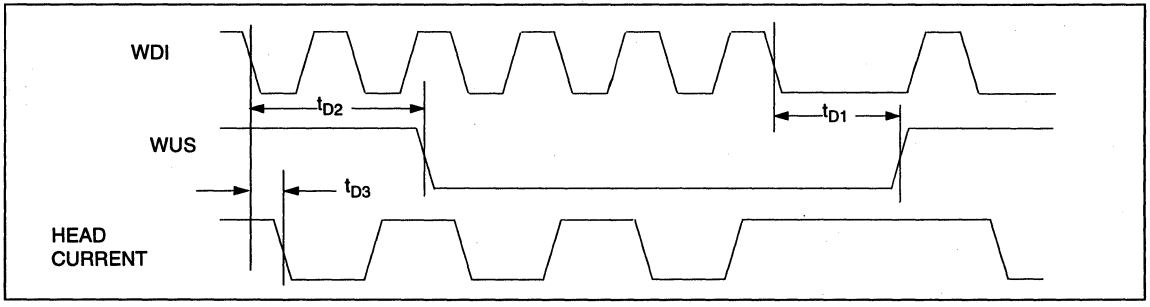


Figure 1: Write Mode Timing Diagram

4 Servo Preamplifiers

Servo Read/Write Preamplifier

VTC Inc.
Value the Customer™

VM323

SINGLE CHANNEL, THIN-FILM HEAD, READ/WRITE, SERVO PREAMPLIFIER

August,1994

FEATURES

- Read Mode Gain = 250 V/V
- Input Noise = 0.85nV/√Hz Maximum
- Input Capacitance = 20 pF Maximum
- Write Current Range = 10 - 40 mA
- Data Protection
- Unsafe Detection
- 5-Volt-Only Operation
- TTL or ECL Inputs
- Pin Compatible with the SSI523, but Does Not Require +12V
- Schottky Isolated Damping Resistor Standard

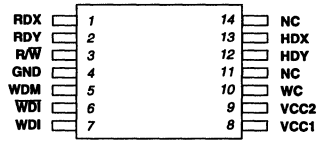
DESCRIPTION

The VM323 single-channel servo read/write preamplifier is a bipolar integrated circuit designed for use with a two terminal thin-film recording head used in disk drive servo systems. This circuit includes a low-noise read preamp for reading servo position signals off the disk and write current control for write servo patterns on to the disk.

In the servo application, the circuit is used once in the write mode and then permanently switched to the read mode. A 650Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain hig- input resistance in the read mode and suitable damping resistance in the write mode. Data protection is provided in both the read and write modes to ensure servo data integrity. Power supply fault detect circuitry protects data from write splash by turning off the write current source in the event of sudden power down. Shorted head-to-ground detect capability also protects data in the write mode.

The VM323 operates on a 5-volt-only power supply. Please consult VTC for package availability.

CONNECTION DIAGRAM



Single-Channel
14-lead SOIC

ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{DD1} ..... -0.3V to 14V
- V_{DD2} ..... -0.3V to 14V
- V_{CC} ..... -0.3V to 6V

Input Voltages:
- Head Select (HS) ..... -0.3V to V_{CC} + 0.3V
- Write Unsafe (WUS) ..... -0.3V to 10V
- Write Data Input (WDI) ..... -0.3V to V_{CC} + 0.3V
- Chip Select ..... -0.3V to V_{CC} + 0.3V
- Read/Write Select (R/W) ..... -0.3V to V_{CC} + 0.3V

Output Current:
- Write Current (I_W) 60mA
- Read Data (RDX, RDY) 10mA
- Center Tap Current (I_{CT}) 60mA
- Write Unsafe (WUS) 12mA

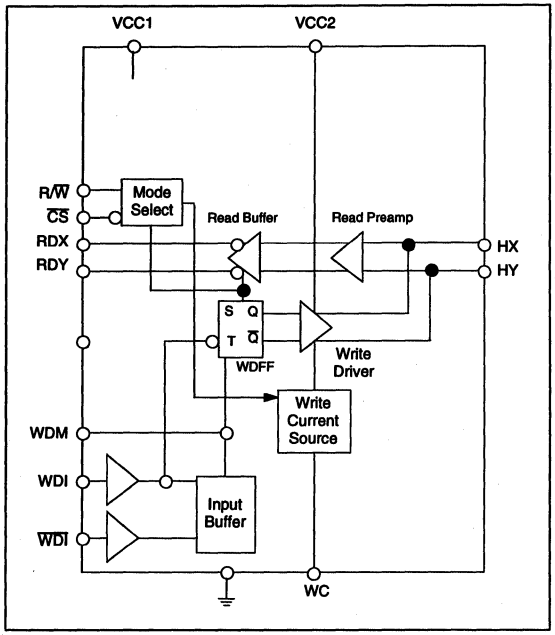
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to 150°C
Lead Temperature (Soldering 60 Seconds) ..... 300°C
Thermal Characteristics, Θ_{JA}:
- Junction Temperature ..... 150°C
- 14-lead SOIC ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{CC1} ..... 5V ± 10%
- V_{CC2} ..... 5V ± 10%

Head Inductance (L_H) ..... 0.15 to 5μH
Damping Resistance (R_D) ..... 650Ω ± 20%
RCT Resistor at I_W = 40mA 120Ω
RDX, RDY Output Current (Read Mode) ..... 0 to 0.5mA
Write Current Range ..... 10 to 40mA
Operating Junction Temperature ..... 25° to +70°C

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The VM323 provides write current control and read amplification. Mode control is accomplished with the Write Data Mode (WDM) and Read/Write select (R/W) pins as shown in table A. An internal pullup resistor on the R/W line will force the device into a non-write condition in the event of an open line.

Write Mode

In write mode, the VM323 is a differential current switch. The level on the WDM pin allows the option of using TTL or Psuedo-ECL levels on the write data (WDI/WDI) pins. With WDM open, the WDI pin is used with TTL level data and the write current toggles between the x and y direction at the head on each high to lo transition. A preceding read operation initializes the Write Data flip flop to pass current in the x direction. With WDM grounded, both the WDI/WDI pins are used with Psuedo-ECL data levels to control the write current direction. In the write mode, the read amp is powered down to reduce power dissipation.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.65V reference voltage is present at the WC pin. The magnitude of the write current (0-pk) is:

$$I_W = V_{WC}/R_{WC} = 1.65V/R_{WC}$$

Read Mode

In read mode, the VM323 is a low noise differential amplifier and the write current source is powered down to ensure data integrity and reduce power dissipation. The RDX,RDY lines are open collector outputs.

Data Protection

Power supply fault detection/protection improves data security by turning off the write current generator during a sudden power up/down condition. The shorted head to ground detect will also turn off the write current generator.

PIN DESCRIPTIONS

R/W: high level selects read mode

WDI, WDI: toggles direction of the write current

HDX,HDY: current in the X direction flows into the X pin

RDX,RDY: differential read data output

WC: used to set write current

WDM: grounded, use WDI/WDI with direct differential data inputs. open, use WDI with TTL data input.

VCC1: +5 Volt supply

VCC2: +5 Volt supply

GND: ground

Table 1: Mode Selection

R/W	*WDM*	*MODE*
0	GND	PECL Write Diff. Input (WDI, $\overline{WDI}$)
0	Open (high)	TTL Write Input (WDI)
1	X	Read

Table 2: External Resistor vs. Write Current

External resistor vs. DC write current I_W into the selected head terminal X or Y with V_{CT} shorted only to the respected X or Y terminal	
External Resistor R_{WC} (Ω)	Write Current I_W (mA)
165	10
82.5	20
55	30
41.25	40

Note: Effective current I_{FLUX} generated in the magnetic head is related to I_W by the expression:

$$I_{FLUX} = I_W\left(\frac{R_D}{R_H + R_D}\right) \qquad \textit{(eq. 1)}$$

Where R_H equals the full coil resistance of a center-tapped ferrite head and R_D is the damping resistor connected internally or externally between the X and Y terminals. Nominal internal resistance on VM323 is 650Ω.

PREAMPLIFIERS

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

DC CHARACTERISTICS $V_{CC1} = V_{CC2} = 5V \pm 10\%$, $T_A = 25°C$, unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
POWER SUPPLY						
VCC1 Supply Current		Read Mode			35	mA
		Write Mode			30	
VCC2 Supply Current		Read Mode			7	mA
		Write Mode			19 + I_W	
Power Dissipation		Read Mode			500	mW
		Write Mode, I_{WC} = 40mA			500	
DIGITAL INPUTS						
Input High Voltage	V_{IH}				0.8	V
Input Low Voltage	V_{IL}		2.0			V
Input High Current	I_{IH}	V_{IH} = 2.0V			100	µA
Input Low Current	I_{IL}	V_{IL} = 0.8V	-0.4			mA
Input Voltage (WDI, $\overline{WDI}$)		WDM = GND	3		VCC1	V
Differential Input Voltqge (WDI, $\overline{WDI}$)		WDM = GND	200			mV
VCC1 Fault Voltage			3.5		4.1	V
Head Current HDX, HDY		Write Mode	-200		+200	µA
		Read Mode	-200		+200	

WRITE CHARACTERISTICS Unless otherwise specified; $L_H = 1.5\mu H$, $R_L = 30\Omega$, $I_W = 15mA$, $f_{DATA} = 5MHz$, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W	(See table 2)	10		40	mA
WC Pin Voltage	V_{WC}			1.65 ±5%		V
Differential Head Voltage Swing	V_{DH}		4			Vpp

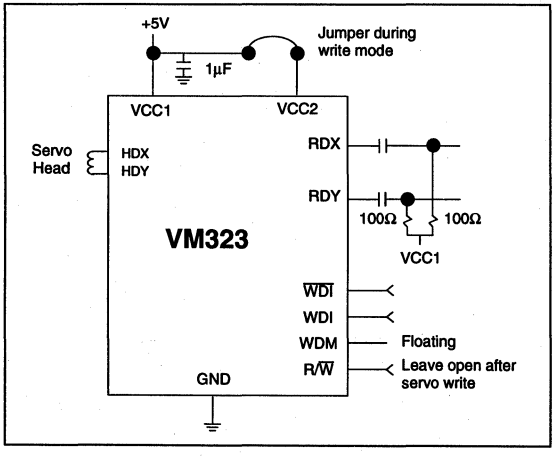
READ CHARACTERISTICS $V_{CC1} = V_{CC2} = 5V \pm 10\%$, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, @ 1MHz	200	250	300	V/V
Bandwidth	BW	V_{IN} = 1mVrms, @ 300kHz, -1dB	10	20		MHz
		V_{IN} = 1mVrms, @ 300kHz, -1dB	20	45		
Dynamic Range	DR		-2		2	mV
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.85	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVpp, f = 5MHz		16	20	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVpp, f = 5MHz	460	750	1400	Ω
Common Mode Rejection Ratio	CMRR	V_{IN} = 0VDC + 100mVp-p @ 5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz, on V_{CC}	54			dB
Output Offset Voltage	V_{OS}	V_{IN} = 0	-300		+300	mV
Gain Sensitivity		15°C < T_A < 55°C		-16		%/°C

SWITCHING CHARACTERISTICS $V_{CC1} = V_{CC2} = 5V \pm 10\%$, $T_A = 25°C$, $I_W = 15mA$, $L_H = 1.5\mu H$, $f_{DATA} = 5MHz$, unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read-to-Write Switching	t_{RW}	R/$\overline{W}$ to 90% of I_W			0.6	ns
Write-to-Read Switching Delay	t_{WR}	R/$\overline{W}$ to 90% of Read Envelope			0.6	ns
Head Current Propagation Delay	t_{D3}	50% of WDI to I_{HX}, I_{HY}		20		ns
Asymmetry	A_S				1	ns
Rise/Fall Time	t_r/t_f	10 - 90% points, L_H = 0, R_H = 0		5	7	ns

TYPICAL APPLICATION



5 Data Recovery Circuits

VTC Inc.
Value the Customer™

VM53100
DATA SEPARATOR CHANNEL CHIP

August,1994

FEATURES
- (1,7) RLL Code
- Data Rates From 33 to 100 Mbits/sec
- Compatible with Zoned-Density Recording
- Data Separator has Zero-Phase Restart & Marginalization
- Programmable Write Precompensation
- Designed to Operate with the VM54100
- Erase False Peak Feature
- Single Supply 5-Volt Operation
- Differential ECL Type Encoded Write Data Output
- Available in a 64-Lead PQFP Package

DESCRIPTION
The VM53100 is an integrated circuit designed to be used for data storage/recovery in high performance disk drive systems. The chip includes a frequency synthesizer, write precompensation, read data separator, (1,7) encoder/decoder, serial interface shift register, biasing circuitry that includes sleep and nap mode functions, and test multiplexers for I/O test capability. The circuit has a two bit parallel interface to the drive controller, is designed to operate at data rates from 33 to 100 MBits/sec, is zone density compatible and comes in a 64-lead PQFP package. Refer to the VM53100 block diagram.

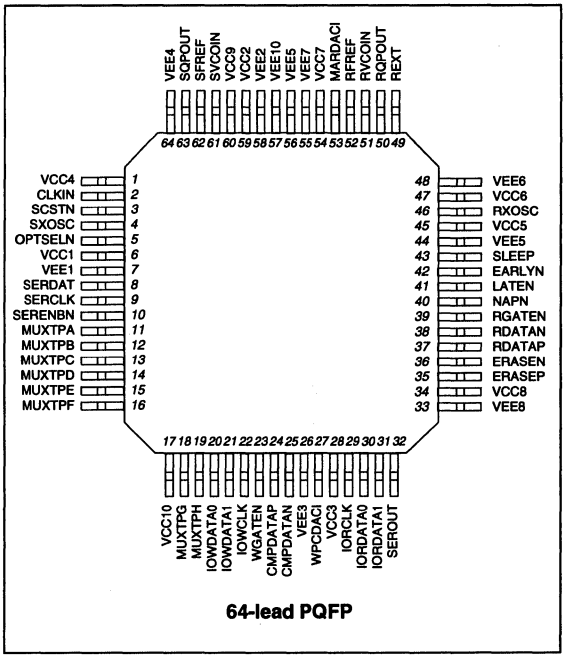
ABSOLUTE MAXIMUM RATINGS

Supply Voltage:
V_{CC} (V_{EE} = 0) ..... -0.5V to 6.5V
Junction Operating Temperature ..... 0° to +150°C
Voltage Applied to TTL Inputs (V_{EE} = 0V) -0.5V to V_{CC} +0.5V
Voltage Applied to PECL Inputs (V_{EE} = 0V) ..... 0V to VCC
PECL Output Current - Continuous 25mA
PECL Output Current - Surge 50mA
Storage Temperature ..... -65° to 150°C
Maximum Power Dissipation 700mW
Lead Temperature (soldering 60 seconds) ..... 300°C

RECOMENDED OPERATING CONDITIONS

Supply Voltage:
V_{CC} (V_{EE} = 0) ..... +4.5V to 5.5V
Junction Temperature ..... 0° to 100°C
Data Rate Frequency ..... 33 to 100Mbits/sec
Ambient Operating Temperature, T_A ..... 0 to 70°C

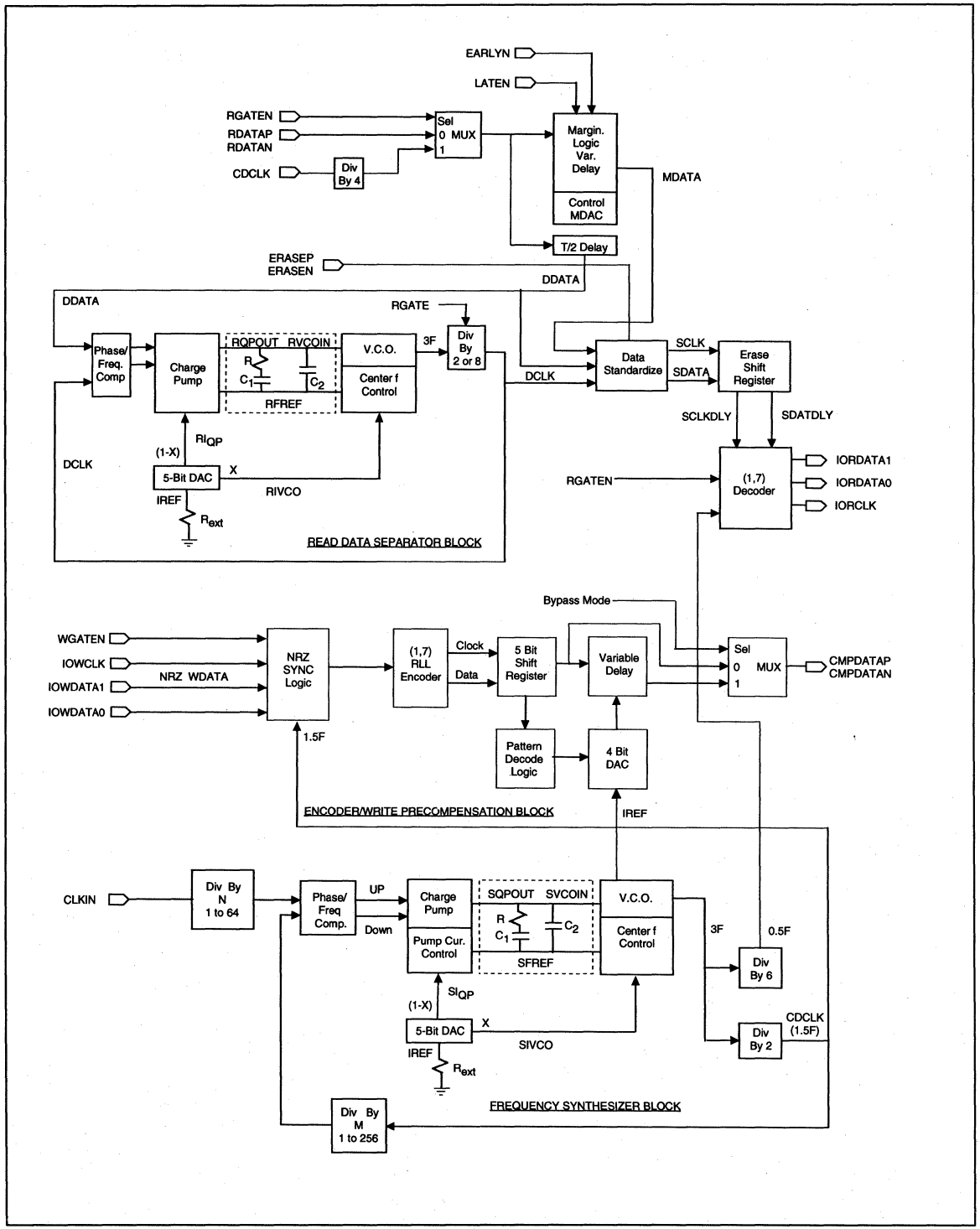
CONNECTION DIAGRAM



64-lead PQFP

DATA RECOVERY CIRCUITS

BLOCK DIAGRAM



DATA RECOVERY CIRCUITS

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FREQUENCY SYNTHESIZER

The frequency synthesizer is implemented using a charge pump type phase-locked loop (PLL). The PLL consists of a phase/frequency detector, charge pump, VCO and two programmable frequency dividers.

The synthesizer reference clock signal that is used to drive the divide-by-N block comes into the chip through the CLKIN input pin. The divide-by-N counter divides the incoming reference clock by a programmable integer value from 1 to 64. The output of the divide-by-N becomes the reference clock for the synthesizer PLL. The divide-by-M counter divides the CDCLK output by a programmable integer value from 1 to 256. The output of the Divide-by-M becomes the variable input to the synthesizer PLL. Both counters are programmed from the serial registers.

The phase/frequency detector block is a true frequency discriminating comparator with 2π radians per cycle usable for phase/frequency correction. An input pulse at the reference input initiates a pump-up signal to the Charge Pump and an input pulse at the variable input initiates a pump-down signal. When both pump-up and pump-down are true the circuit is reset. The minimum pump-up and pump-down pulse widths are determined by internal propagation delays and are about 3 ns. In the locked condition, the pump-up and the pump-down signals are true for a short and equal period and are coincident in time.

The charge pump sources and sinks correction current at the SQPOUT pin when the pump-up and pump-down signals are true, respectively. An external RC network, connected between pins SQPOUT, SVCOIN and SFREF, is used to set the PLL dynamic characteristics. The SFREF pin is a low impedance voltage source used as a loop filter reference node to minimize noise coupling into the VCO input. The voltage at this pin is about 2.3 V. The charge pump current driven into the loop filter generates a differential voltage at pin SVCOIN with respect to pin SFREF. This voltage drives the VCO block inputs. The charge pump gain (the output current magnitude divided by 2π) is set by the current output from the internal 5-bit DAC.

The VCO block converts the differential voltage between pins SVCOIN and SFREF into a frequency. This frequency is fed back to the Phase/Frequency Comparator through the divide-by-M counter. Center frequency occurs when the voltage between SVCOIN and SFREF is zero. The VCO center frequency is trimmed to ±10% at wafer test. Center frequency is set by the REXT resistor and the internal synthesizer DAC. Adjusting the VCO center frequency with the DAC "X" output current changes the VCO gain constant in a proportional manner. A second current, the DAC "1-X" current, is used to offset this change by adjusting the Charge Pump gain proportional to "1-X", thus maintaining a reasonably constant loop gain.

Table 1: Output Clock Frequencies (where m is the VCO divisor and n is the CLKIN divisor)

CLKIN	*VCOCLK*	*IORCLK*	*CDCLK*
f_i	$f_o = 2f_i$ (m/n)	$f_o/6$	$f_o/2$

SYNTHESIZER DAC

The Synthesizer DAC is a five-bit, current output, digital to analog converter. It is used internally to set the VCO center frequency and the Charge Pump gain as described in the section above. The VCO center frequency, f_c and the Charge Pump current (the "1-X" current), I_{QP} are given by the expressions below.

R_{REXT} is the resistance value in Ohms from the REXT pin to VEE, X is the decimal equivalent of the DAC input bits and K_{VCO} (MHZ/V) is the VCO gain.

$$I_{QP} = \left(\frac{0.01875}{R_{REXT}}\right) \times (63 - X) \qquad \textit{(eq. 1)}$$

$$f_c = \left(\frac{7.875 \times 10^9}{R_{REXT}}\right) \times (33 + X) \qquad \textit{(eq. 2)}$$

$$K_{VCO} = 0.44 \times f_c \text{MHz} \qquad \textit{(eq. 3)}$$

WRITE DATA ENCODER

The write data encode function includes the NRZSYNC, ENCODER STATE MACHINE, and ENCODER SHIFT REGISTER blocks.

The NRZSYNC block receives TTL NRZ, 2 bit parallel write data (IOWDATA0 and IOWDATA1) and the TTL write clock (IOWCLK) from the drive controller. The drive controller uses the 0.5f clock output from the frequency synthesizer (IORCLK) as a data rate reference clock to clock out NRZ write data. This 0.5f clock is returned as IOWCLK by the controller. However, this clock must also pass through an arbitrary cable delay before it is returned. This creates an unknown phase relationship between IOWCLK and the 1.5f clock from the synthesizer, its source. The purpose of the NRZSYNC block is to automatically choose the appropriate internal IOWCLK phase to reliably clock in IOWDATA0/IOWDATA1. This edge selection occurs upon each assertion of WGATEN.

The ENCODER block takes each pair of IOWDATA bits and encodes them into three encoded bits according to the following code tables.

DATA	*CODE*
11	101
10	100
01	001
00	010

In instances where the last table produces code sequences which violate the (1,7) run length constraint, the following violation code table is invoked (the MSB {left-most bit} is written/read first):

DATA	*CODE*
11 11	101 000
11 10	100 000
01 11	001 000
01 10	010 000

WRITE PRECOMPENSATION

The write precompensation circuitry consists of a 5-bit shift register, pattern decode logic and a DAC controlled delay cell. It is able to precompensate two different data patterns as shown

in the Precompensation Rules Table. The amount of compensation for each pattern is individually controlled by a 4-bit word programmed via the serial interface. The third case is 'all others' pattern that requires no precompensation. These patterns default to nominal precompensation and the variable delay DAC input is hard-wired to 1000.

The encoded (1,7) write data is clocked through a 5-bit shift register. As the data is shifted through, decode logic is able to recognize the two different predetermined data patterns as shown in the Precompensation Rules Table - the center bit always being a '1' for precompensation. When a pattern is found, the appropriate address in the serial register is read and inputted to the 4 bit DAC. The DAC then adjusts the programming current for the variable delay block which shifts the proper bit early or late. The delay tracks with zone frequency and is therefore always a percentage of the 1.5f write clock period. The maximum precompensation is -24/+21 % T with resolution of 3.0% T, T being the period of the 1.5f write clock. Refer to WPC Shift Magnitude Table

Precompensation Rules Table

PATTERN #	*NAME*	*BIT SEQUENCE*				
		N-2	N-1	N	N+1	N+2
1	2T:>2T	1	0	1	0	1
2	>2T:2T	0	0	1	0	0

WPC Shift Magnitude Table

DAC Bits	% Time Shift	DAC Bits	% Time Shift
0000	-24.0	1000	0.0 (NOM)
0001	-21.0	1001	3.0
0010	-18.0	1010	6.0
0011	-15.0	1011	9.0
0100	-12.0	1100	12.0
0101	-9.0	1101	15.0
0110	-6.0	1110	18.0
0111	-3.0	1111	21.0

READ DATA SEPARATOR (RDS)

The circuit is composed of the following functional blocks: a high precision phase-frequency detector, a differential charge pump, a differential input VCO, an external filter, a zero-phase VCO restart, a divider, a data standardizer, a synchronization control block, window marginalization, a delay control loop, and a post PLL erase shift register.

Read Operation

There are two stages in the read PLL locking sequence

1) lock to the reference oscillator
2) locking to data.

Initially, the data separator locks to the CDCLK/4 input. This is a standby state which the data separator is in when not reading data. The VCO locks to the CDCLK frequency which is very close to the frequency of the input data stream RDATAP/N. This minimizes the frequency step when the PLL input is switched to RDATA. When the VCO is locked to CDCLK, the phase detector is in the phase/freq mode and guarantees non-harmonic lock up.

The assertion of RGATEN initiates a read operation. Internally, the part switches the input to the PLL from CDCLK to RDATA. At this time, the VCO is momentarily stopped and restarted in phase with the third data bit in the preamble. This allows very fast and repeatable lockup to the preamble field. The phase detector switches into the phase mode which allows the PLL to lock to harmonics. This also allows great flexibility in the preamble pattern. The user could actually lock up in the middle of a data field if so desired.

Sync Control

The synchronization control block controls the input multiplexer, the phase/frequency detector, the zero phase restart block, and the enable for the data standardizer. It guarantees that the phase locked loop switches smoothly from one mode to another.

The control pin setting and corresponding modes are summarized in the table below.

RGATEN	MUX SEL	DIVIDER	PHASE/FREQ DET
0	RDATA	div-by-2	phase mode
1	CDCLK/4	div-by-8	phase/freq mode

Data MUX

In idle mode, the PLL locks to the CDCLK/4 coming from the synthesizer VCO. In the read mode, the PLL locks to the RDATA input. The DATA MUX multiplexer selects which input (CDCLK/4 or RDATA) the PLL will lock to.

Delay Line/One-Shot

The RDS uses an internal one-shot circuit to delay the data coming into the phase detector. The one-shot is activated on the rising/leading edge of the incoming pulses from the Data MUX. The width of the output pulse is nominally set to one half of the 1.5F clock period. The leading edge (negative going) of the one-shot output enables the phase detector and allows it to anticipate incoming data bits. The trailing edge (positive going) occurs 0.5T later carrying the timing information of the RDATA Pulse stream and initiates the up pulse of the PFD. The output pulse width is controlled by the synthesizer VCO loop and is insensitive to external components, supply voltage, temperature, and IC processing.

Phase/Frequency Detector (PFD)

The phase/frequency detector has two modes of operation, the phase/frequency mode used during the Idle/Write mode and phase mode used when reading data. Each mode is described below.

In the phase/frequency mode both phase and frequency differences of the two incoming signals are detected. In this mode the PLL cannot lock to harmonics of the reference input. The rising edge of the reference input (DDATA) to the PFD initiates an UP signal to the charge pump, and a rising edge of the VCO feedback input (DCLK) initiates a DOWN signal to the charge pump. When both UP and DOWN are HI, the internal flip-flops are reset and the signals return LO again. The minimum pulse width of the UP and DOWN signals is determined by internal propagation

delays and is approximately 4 ns. In a locked state, the rising and falling edges of the UP and DOWN signals are coincident and there is no net effect on the PLL phase and frequency.

When in the phase mode, the PFD detects only the phase of the two inputs. The phase mode is used whenever RGATEN gate is asserted. The anticipator delay is 0.5T and is used to condition the phase detector for a phase comparison. The operation of the phase detector is the same as in the phase/frequency mode except that a phase comparison cannot be initiated until a data pulse is input to the phase detector. This allows the PLL to lock to harmonics of the VCO frequency.

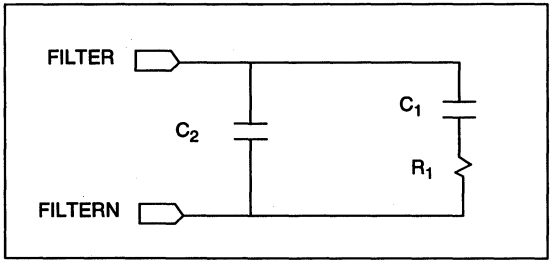
Charge Pump

The charge pumps use high speed NPN and PNP switches to feed current in and out of the RQPOUT pin. The UP and DOWN signals from the phase detector feed into the charge pump and cause it to pump current in or out of the differential lead-lag filter. The high speed current switches in the charge pump sink or source current at the RQPOUT pin, as determined by the UP and DOWN inputs from the PFD. The RVCOIN side of the filter acts as a voltage source. The charge pump current for the VCO is set by the external resistor connected to the REXT pin and the VCO DAC. The current can be varied from 200 to 700 µA by adjusting the REXT resistor.

Filter

The filter resides external to the chip, allowing the system designer to control the loop dynamics. It is composed of two capacitors and a resistor.

RDS Loop Filter



VCO

The VCO is a multivibrator type oscillator which has good linearity over its frequency range. The differential voltage between the RVCOIN and RFREF pins controls the VCO frequency. The RVCOIN pin is typically connected to the RQPOUT pin but can be externally disconnected for testing purposes. The VCO is at its center frequency when the differential voltage between RVCOIN/RQPOUT and RFREF is zero. The external resistor tied from the REXT pin to VEE and the VCO DAC inputs set the VCO center frequency and gain. The VCO gain is proportional to the VCO center frequency.

The VCO center frequency is trimmed to within 10% at wafer level to compensate for on-chip capacitor variations.

Divider

The divider block divides down the VCO frequency. The divided VCO signal (DCLK) is routed to the data standardizer and also to the phase-frequency detector to complete the loop. This division is switchable from a divide-by-two to a divide-by-eight. The VCO divided-by-two is used in the Read mode when the phase-frequency detector is in the phase (harmonic) mode. The VCO divided-by-eight is used when the phase-frequency detector is in the phase-frequency mode and the PLL is locking to the synthesizer clock (CDCLK/4).

Data Standardizer and Erase Shift Register

The divided VCO clock and the data input to the PLL contain the data and clock information needed but are not synchronized to one another. For this reason, they are fed to a data standardizer which takes out any bit shift in the data and puts the bit in a decode window. The data standardizer uses the falling edge of the divided VCO clock to generate the decode window. If an ERASE pulse occurs, it is synchronized to the data and the clock. The synchronized data and clock then feed into an eight bit shift register along with a possible erase signal originating in the PDQ in the VM54100. When an ERASE condition is detected, the most recent "one" bit in the register is removed. The SCLKDLY and SDATDLY lines to the decoder are produced by this block.

Zero-Phase Restart

A zero-phase restart of the VCO is performed whenever the input to the PLL is switched from the reference to data. The zero-phase restart block interfaces to several other blocks on the chip and guarantees a smooth transition when switching. The time that the VCO is stopped is a function of the preamble data pattern. The lower the preamble frequency, the longer the VCO may wait for a preamble bit to restart itself. No spurious data and clock signals will occur when RGATEN is switched.

Window Marginalization

The RDS contains circuitry which can be used to artificially shift a data bit in the clock window. This function can be used either for system calibration or for re-reading blocks of data with altered phase during a read re-try. When EARLYN or LATEN is asserted, the marginalization block is activated and the data standardizer accepts data from the MDELAY outputs rather than the DELAY cell. The DELAY and MDELAY cells are identically matched cells controlled by the synthesizer multiplier so that their nominal delays are equal. The PLL will continue to lock to data from the DELAY cell, however, the delay of the MDELAY cell can be independently varied about its nominal value via the MDAC cell. Hence the phase between the clock and data can be externally controlled. The magnitude of the phase shift is controlled by a 4 bit DAC which is programmed via the serial interface. These four bits must be programmed to the correct magnitude before asserting EARLYN and LATEN. The user can see how much the bit is being shifted by looking at the phasing of DCLK and MDATA. When the bit is exactly centered, the rising edge of MDATA should fall exactly in the center of the falling edges of DCLK. The EARLYN and LATEN pins are control signals for the marginalization block. When data is to arrive before the clock, the EARLYN signal is asserted. When data is to arrive after the clock, the LATEN signal is asserted. Under normal operation (when marginalization is not being used), both EARLYN and LATEN float HI, the marginalization circuitry is powered down, MDATA floats to an intermediate PECL level, and the marginalization block plays no role in the data synchronization. Marginalization DAC settings are shown in the Marginalization DAL Setting Table and in the timing diagrams.

Marginalization DAC Setting Table

B_3	B_2	B_1	B_0	Window Shift (% of 1.5f clock period)
0	0	0	0	0.0
0	0	0	1	2.0
0	0	1	0	4.0
0	0	1	1	6.0
0	1	0	0	8.0
0	1	0	1	10.0
0	1	1	0	12.0
0	1	1	1	14.0
1	0	0	0	16.0
1	0	0	1	18.0
1	0	1	0	20.0
1	0	1	1	22.0
1	1	0	0	24.0
1	1	0	1	26.0
1	1	1	0	28.0
1	1	1	1	30.0

RDS Loop Constraints

When changing frequency zones on the disk, it is desirable to modify the PLL response to maximize performance. This could include changing the loop bandwidth (filter components) and loop gain. Unfortunately, switching filter components to change the bandwidth is not easily done and requires additional external components. For that reason, only one set of filter components is used. The loop gain and response are kept nearly constant over all zones. This gives predictable loop behavior in both inner and outer zones on the disk.

An important characteristic of the VCO is that the gain (radians/volt) is proportional to the center frequency. This means that the loop gain also varies with center frequency. One way to offset the loop gain variation caused by the VCO is to change the charge pump gain equally but in the opposite direction. This keeps the overall gain product of the loop nearly constant and gives a consistent PLL response at all data rates.

Control of the VCO center frequency and charge pump currents is accomplished via the VCO/QPUMP DAC. The DAC has X and (1-X) outputs, with X being proportional to the DAC input code. The X output supplies the VCO bias current and the (1-X) output supplies the charge pump bias current. As the VCO center frequency increases for the outer zones on the disk, the charge pump current decreases. As the VCO center frequency decreases at inner zones on the disk, the charge pump current is increased.

This method of controlling the PLL gain works well but is not perfect. The product of X and (1-X) is a maximum when X=0.5. Thus the product of the charge pump gain and VCO gain is a maximum at the center zone on the disk. Toward the inner or outer zones on the disk, the loop gain begins to go down.

Expressions for the maximum transfer rate (TRmax)(2* IORCLK) and Iqpump vs Rext is as follows:

$$R_{EXT} = \frac{168}{TR_{max}} \qquad \textit{(eq. 4)}$$

where TRmax is in MHz and Rext is in KΩ, and the VCO DAC code is set to 11111. The transfer rate as a function of DAC code is:

$$TR = \left(\frac{TR_{max}}{64}\right) \times (33 + DACcode) \qquad \textit{(eq. 5)}$$

The VCO DAC code varies from 0 to 31. The 1.5F SCLK output is equal to 1.5*TR (MHz) and the internal VCO clock runs at 3*TR (MHz). The Iqpump current expression and VCO center frequency expressions are:

$$I_{QP} = \left(\frac{0.01875}{R_{REXT}}\right) \times (63 - X) \qquad \textit{(eq. 6)}$$

$$f_c = \left(\frac{7.875 \times 10^9}{R_{REXT}}\right) \times (33 + X) \qquad \textit{(eq. 7)}$$

$$K_{VCO} = 0.44 \times f_c MHz \qquad \textit{(eq. 8)}$$

The 5-bit VCO QPUMP DAC gives 2.1% step resolution in VCO center frequency and charge pump current from the center zone on the disk i.e. DAC setting = 10000. The DAC allows a maximum outer to inner zone frequency ratio of 2:1.

When changing zones, the controller should reprogram the synthesizer dividers and VCO DAC first. This is because the PLLs take longer to settle after reprogramming. The write precomp bits and marginalization bits can be reprogrammed last since these blocks recover very quickly after the serial enable is brought HI.

DECODER

The decoder block decodes the 2/3 rate (1,7) Run Length Limited (RLL) modulation code used by the disk drive recording channel. In READ mode, the (1,7) encoded read data and a code rate clock are received from the RDS and NRZ read data and read clock are output to the drive controller.

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DECODE TABLE

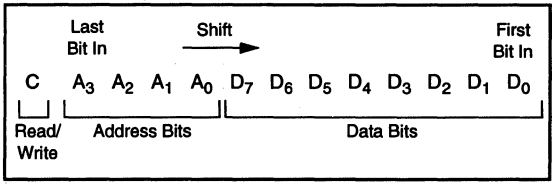
READ ENCODED DATA			NRZ DATA D1 D0
LAST BIT OF PREVIOUS CODE WORD	PRESENT CODE WORD t→	NEXT CODE WORD	
X	101	XXX	11
X	100	not 000	10
X	100	000	11
X	001	XXX	01
X	010	not 000	00
X	010	000	01
0	000	XXX	10
1	000	XXX	11

The Decoder block receives encoded read data and a code rate clock from the erase shift register on the RDS. The Decoder begins searching for a 10X10X10X1 pattern. Since the Decoder shift register suppresses the bit following a 1 to a 0, these bits are don't cares in the sync pattern. When the pattern is detected, the Decoder is framed to the proper incoming read code phase, and 3-5 code clock cycles later, begins putting out decoded read data at IORDATA. This output is held LO up to this time. The decode algorithm is specified in the coding table. Single-bit error propagation is 5-bits maximum. The IORCLK output must be continuous when switching between READ and idle/write modes with no more than two missing periods and no short duration glitches occurring at an interval less than one half a data rate period. When RGATEN goes inactive, the IORDATA0/ IORDATA1 output is immediately pulled LO to eliminate the possibility of extraneous data being sent back to the controller at the end of a read.

SERIAL INTERFACE

The disk drive controller programs the chip via a serial interface. The interface consists of four TTL-level signals for input data, output data, clock, and enable. Upon asserting SERENBN, the serial port is enabled and ready for input on SERDAT and SERCLK. The SERDAT line provides the data, address and read/write control information. During a write cycle the serial control stream is shifted into the input register on the rising edge of the SERCLK starting with the LSB (bit 0) of the data byte, after the MSB (bit 7) of the data has been inputted, the four (4) address bits are clocked in starting with the LSB. After all 12 bits have been clocked into the shift register, a "0" must be placed on the SERDAT input (but NOT clocked in by SERCLK) to indicate data is being written to the chip. The data is then latched into the proper register when SERENBN is de-asserted. The process must be performed six times to load all six register banks. Refer to the Serial Interface Load Timing Diagram.

The serial interface also has the capability of reading the programmed data back out of the internal registers on the SEROUT (tri-stated serial output) pin. After asserting SERENBN, a 4-bit address must be clocked into the shift register. A "1" must be placed on the SERDAT input (but NOT clocked in by SERCLK) to indicate data is being read from the chip. When the SERENBN line is de-asserted the SEROUT pin is taken out of tri-state mode and put ino the active mode. After a short delay the output will settle to the state of bit 0 from the selected register. To complete the read operation the SERENBN line must be re-asserted and the SERCLK must be strobed to transfer successive bits to the output line. After the SERCLK line is strobed seven times the MSB of the data will be present on the output line. To read the address word, the SERCLK must be strobed four additional times, at which time the MSB of the address will reside on the output line. To complete the read cyle, the SERDAT line must be put into the "0" state and then the SERENBN can be de-asserted for the second time. After the SERENBN is de-asserted the second time the output buffer is placed into a high impedance tri-state mode. Refer to the Serial Interface Read Timing Diagram.



SLEEP MODE

The VM53100 has a sleep mode that can be used when the circuit is not used for an extended period of time. Much of the chip is powered down to reduce power dissipation. The chip becomes non-functional in this mode. The chip must be completely reprogrammed when the chip 'wakes up'. Output signal, CMPDATA is undefined for 18 IORCLK cycles following removal of the SLEEP command. The drive design should ensure that these signals are ignored during this time.

NAP MODES

The VM53100 has a nap mode that can be used to reduce the power dissipation in the read, write, and idle modes. If NAPN is HI, then no power reduction is initiated. If NAPN is LO, and WGATEN is HI, then the encoder and WPC circuits are powered down. If NAPN is LO, and RGATEN is HI, then the decoder is powered down. If NAPN is LO, and both WGATEN and RGATEN are HI, then the encoder/decoder and WPC circuits are all powered down.

SERIAL INTERFACE REGISTER TYPICAL SETTING TABLE

REGISTER ADDRESS	DATA BIT							
	7	6	5	4	3	2	1	0
0000	1	1	1	1	0	0	0	0
0001	0	1	1	1	1	1	1	1
0010	1	0	1	1	1	1	1	1
0011	1	0	0	0	1	0	0	0
0100	1	1	1	1	1	0	0	0
0101	0	0	0	0	Unused			

0 = VCO/QPUMP DAC is set to its center zone, 10000; TPFD, BPDIV and DVRST are all disabled

1 = The divide-by-m counter set to divide-by-128, 01111111

2 = ROSEL is diabled; Divide-by-n counter set to divide-by-32, 011111; SOSEL is disabled

3 = All write precomp patterns are set for nominal compensation, 1000

4 = The marginalization DAC is set to 50% marginalization, 1000; DISERS, TDEC, BPWPC, BPENC are all disabled

Serial Register Table

REGISTER ADDRESS	DATA BIT							
	7	6	5	4	3	2	1	0
0000	DVRST*	BPDIV*	TPFD*	VCO/QPUMP 5-BIT DAC				
0001	DIVIDE-BY-M COUNTER							
0010	SOSEL*	DIVIDE-BY-N COUNTER						ROSEL*
0011	WPC PATTERN 2				WPC PATTERN 1			
0100	BPENC*	BPWPC*	TDEC*	DISERS	RDS MARGIN DAC			
0101	DISA-D	DISE-H	TS1	TS0	UNUSED			

* The DVRST,M BPDIV, TPFD, SOSEL, ROSEL, BPENC, BPWPC and TDEC signals must be accompanied by a ground connection to the OPTSELN input pin order to become active

Serial Interface Register Allocation

REG ADDR	Function and Explanation
0000	Synthesizer and RDS VCO/QPUMP 5 bit DAC (bits D0 through D4) Active HI data bits are programmed according to the formulas in the synthesizer DAC and VCO DAC TPFD - Test Mode Phase/Frequency Detector (bit D5) When programmed LO, and the OPTSELN is LO, then the phase frequency detector in the RDS is in the phase/frequency mode and can be used to force up/down conditions in the PFD. BPDIV - Divider Bypass Mode (Bit 6) When programmed LO, and OPTSELN is LO, the SXOSC is brought in after the divide by 2 in the Synth. (immediately before the div-by-M), ALSO the RXOSC, for the RDS, is brought directly into the Data Standardizer in place of DCLK, thereby bypassing the DIVVCO block. The DIVVCO block however still feeds the RPFD. DVRST Divider Reset (bit D7) When programmed LO, and OPTSELN is LO, then the M & N dividers in the Synthesizer are reset to zero. Also, the DIVVCO and DIV4 blocks in the data separator, and the Decoder DIV3 and CLKMUX blocks are reset to zero.
0001	Divide-By- M counter (bits D0 through D7) The serial interface bits should be programmed to one less than the desired divider value. For example, to divide by 32 in the M counter, the serial interface should be programmed to 31.
0010	ROSEL - RDS Oscillator Select (bit D0) When programmed LO, and OPTSELN is LO, then a TTL signal applied to RXOSC input pin replaces the on chip RDS VCO. Divide-By-N counter (bits D1 through D6) Program to one less than the desired divide-by number. SOSEL - Synthesizer Oscillator Select (bit D7) When programmed LO, and OPTSELN is LO, then a TTL signal applied to SXOSC input pin replaces the on chip Synthesizer VCO.
0011	WPC Pattern 1 & 2

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Serial Interface Register Allocation

REG ADDR	Function and Explanation
0100	RDS Margin DAC (bits D0 through D3) The percent that the marginalization is set to the margin DAC is used in conjunction with the EARLYN and LATEN pins. DISERS - (bit D4) When programmed LO, the erase signal to the RDS shift erase register is disabled. TDEC - Test Decoder (bit D5) When programmed LO, and OPTSELN is LO then data may be directly inputted to the decoder at the full data rate. The data needs to inputted via the RDATAP/N input pins and the clock inputted through the ERASEP/N pins. BPWPC - Bypass Write Precomp (bit D6) When programmed LO, and OPTSELN is LO, the write precomp circuitry is powered down and the uncompensated encoded data comes out on the CMPDATA outputs. BPENC - Bypass Encoder (bit D7) When programmed LO, and OPTSELN is LO, the encoder is powered down and the IOWDATA1 and IOWCLK bypass the encoder and go directly into the WPC circuit. Compensated data comes out on the CMPDATA outputs.
0101	TS0 (bit D4) The TS0 bit is used in conjunction with the TS1 register bit for selection of the TPMUX outputs given in the Multiplexed Internal Test Points Table. TS1 (bit D5) The TS1 bit is used in conjunction with the TS0 register bit for selection of the TPMUX outputs given in the Multiplexed Internal Test Points Table. DISE-H - Disable TPMUX's E-H (bit D6) When Programmed LO, output buffers TPMUXE-H are powered down. DISA-D - Disable TPMUX's A-D (bit D7) When Programmed LO, output buffers TPMUXA-D are powered down.

Multiplexed Internal Test Points

Inputs		Single-Ended Outputs				Differential Outputs			
TS1	TS0	MUXTPA	MUXTPB	MUXTPC	MUXTPD	MUXTPE	MUXTPF	MUXTPG	MUXTPH
0	0	MDIV	NDIV	SUP	SDOWN	CDCLKP	CDCLKN	IOCLKP	IOCLKN
0	1		DDATA	RUP	RDOWN	DCLKP	DCLKN	MDATAP	MDATAN
1	0	EWCLK	EWDATA	UNCMP		SDATAP	SDATAN	DDATAP	DDATAN
1	1	ERASE	SDATA	RDOWN	RUP	SCLKP	SCLKN	SDATDLYP	SDATDLYN

Descriptions of Single Ended Test Point Outputs

NAME	*DESCRIPTION*
MDIV	Output of the CDCLK clock frequency divided by M. M is the divide-by setting for the 8 bit feedback counter.
NDIV	Output of the CLKIN input clock frequency divided by N. N is the divide-by setting for the 6 bit input counter.
SUP	Pump up signal from the phase-frequency detector in the frequency synthesizer.
SDOWN	Pump down signal from the phase-frequency detector in the frequency synthesizer.
DDATA	Delayed data which has been phase aligned with DCLK before entering the Data Standardizer.
RUP	Pump up signal from the phase-frequency detector in the Read Data Separator.
RDOWN	Pump down signal from the phase-frequency detector in the Read Data Separator.
EWCLK	1.5F clock synchronized to EWDATA.
EWDATA	(1,7) encoded write data before being compensated.
UNCMP	Uncompensated (1,7) encoded write data, after the 5 bit shift register, before being precompensated.
ERASE	Syncronized ERASE signal from the Data Standardizer before entering the Erase Shift registers
SDATA	Synchronized data from the Data Standardizer before entering the erase shift register.

Description of Differential Test Point Outputs

NAME	*DESCRIPTION*
CDCLKP	Differential PECL output of 1.5f clock derived from frequency synthesizer VCO.
CDCLKN	
IOCLKP	Differential PECL output of 0.5f interface clock derived from frequency synthesizer VCO.
IOCLKN	
DCLKP	Clock which has been phase aligned with DDATA. This signal will be the RDS VCO/8 when in idle/write mode and RDS VCO/2 when in read mode.
DCLKN	
DDATAP	Delayed data which has been phase aligned with DCLK before entering the Data Standardizer.
DDATAN	
MDATAP	Data signal that has been phase shifted with respect to DCLK for marginalization. (This is the output of the marginalization delay before entering the Data Standardizer)
MDATAN	
SDATAP	Synchronized data from the Data Standardizer before entering the Erase Shift Register.
SDATAN	
SCLKP	Clock which SDATADLYP/N is syncronized to. This is the same signal as DDCLK except skewed by several gate delays.
SCLKN	
SDATADLYP	Corrected synchronized data from the Erase Shift Register before entering the Decoder.
SDATADLYN	

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Pin Function List and Description for the 64-Lead PQFP Package

PIN NAME	*PIN #*	*DESCRIPTION*
Digital Inputs		
SLEEP	43	TTL input which powers down most of the chip when at a logic "1". This pin must **NOT** be allowed to float, tie to VEE5 (pin 44) if not used.
NAPN	40	TTL control input which when LO manages the chip power dissipation. When NAPN = LO and WGATEN = HI, then the Encoder and the WPC circuits are powered down. When NAPN = LO and RGATEN = HI, the decoder is powered down. When NAPN is HI these circuits remain powered up.
RGATEN	39	TTL control input which when LO initiates lock up to data. When HI, the RDS VCO is in idle mode and locks to the Synthesizer 1.5F clock signal.
WGATEN	23	TTL control input which when LO initiates a write operation.
EARLYN	42	TTL inputs which enable the marginalization circuitry and force the data to arrive early or late in the bit window. Both pins are active LO. EARLYN LATEN MODE 0 0 Shift data early 0 1 Shift data early 1 0 Shift data late 1 1 Marg. Disabled
LATEN	41	
SCSTN	3	TTL input which when LO disables the frequency synthesizer phase detector/charge pump.
CLKIN	2	TTL input reference clock for the frequency synthesizer.
IOWDATA0	20	TTL input of unencoded NRZ write data (Bit 0) sent from the controller.
IOWDATA1	21	TTL input of unencoded NRZ write data (Bit 1) sent from the controller.
IOWCLK	22	TTL input of 0.5f write clock from the controller synchronized with IOWDATA0/1.
SERDAT	8	TTL level data input to the shift register. High true data is clocked in using SERCLK.
SERENBN	10	TTL level shift enable and latch input. When low, it enables SERDAT to be clocked into the serial register using SERCLK. When high, the SERDAT and SERCLK inputs are ignored and the data existing in the serial register passes through a parallel set of transparent latches.
SERCLK	9	TTL level clock input to the shift register. The rising edge is used to clock in SERDAT.
SXOSC	4	TTL test input pin for the Synthesizer VCO. This input replaces the on chip VCO when the SOSEL input in the serial register is programmed LO and OPTSELN is LO.
RXOSC	46	TTL test input pin for the RDS VCO. This input replaces the on chip VCO when the ROSEL input in the serial register is programmed LO and OPTSELN is LO.
OPTSELN	5	TTL input when LO allows specified optional functions to be set up via the serial interface.
ERASEP	35	Differential PECL input of erase signal from the VM54100 pulse detector. An erase pulse indicates a false RDATA pulse has previously occured and should be erased before decoding.
ERASEN	36	
RDATAP	37	Differential PECL input of unsynchonized detected data pulse coming from the VM54100 Pulse detector.
RDATAN	38	
Digital Outputs		
CMPDATAP	24	Differential PECL output of compensated (1,7) encoded write data from the write precompensation block.
CMPDATAN	25	
IORDATA0	30	TTL output NRZ read data output to the drive controller clocked out on the negative edge of IORCLK. When RGATEN is high, this output is held low.
IORDATA1	31	

PIN NAME	PIN #	DESCRIPTION
IORCLK	29	TTL output 0.5f clock synchronized to IORDATA. This output provides the reference clock back to the controller. In read mode, this clock is derived from the RDS. In write and idle mode, this clock is derived from the frequency synthesizer. This output clock runs continuously with no more than 2 missing clock pulses and no short duration glitches associated with mode changes.
SEROUT	32	TTL serial output to read out data stored in the serial interface.
MUXTPA	11	Single-ended PECL outputs of multiplexed internal test points.
MUXTPB	12	
MUXTPC	13	
MUXTPD	14	
MUXTPE	15	Differential PECL outputs of multiplexed internal test points.
MUXTPF	16	
MUXTPG	18	
MUXTPH	19	
Analog Pins		
SVCOIN	61	Voltage control input to the Synthesizer VCO. The dynamic range on pin SVCOIN relative to pin SFREF is ±0.55 volts. The VCO center frequency occurs when the voltage between SVCOIN and SFREF is zero. The filter RC network is connected between SVCOIN and SFREF.
SFREF	62	DC reference voltage of 2.3v for the synthesizer loop filter.
SQPOUT	63	The Synthesizer charge pump output that sources and sinks current to the loop filter. The current is controlled by REXT and the DAC setting. Under normal operation, SQPOUT is shorted to SVCOIN.
RVCOIN	51	Voltage control input to the RDS VCO.The dynamic range on pin RVCOIN relative to pin RFREF is ±0.55 volts. The VCO center frequency occurs when the voltage between RVCOIN and RFREF is zero. The filter RC network is connected between RVCOIN and RFREF.
RFREF	52	DC reference voltage of 2.3v for the RDS loop filter.
RQPOUT	50	The RDS charge pump output that sources/sinks current to the loop filter. The current is controlled by REXT and the DAC setting. Under normal operation, RQPOUT is shorted to RVCOIN.
MARDACI	53	Analog current output of the Marginalization DAC. This pin **must** be externally connected to VCC7 (Pin 54) for normal operation.
WPCDACI	27	Analog current output of the WPC DAC. This pin **must** be externally connected to VCC3 (Pin 28) for normal operation.
REXT	49	Sets the reference current for the VCO/QPUMP 5 bit DAC. The external resistor is tied to VEE. The voltage at pin REXT is approximately 1.18v.
VEE1	7	Write Digital ground
VEE2	58	Analog ground
VEE3	26	WPC Analog ground
VEE4	64	SVCO Analog ground
VEE5	44,56	Read Digital ground (Both pins are internally connected)
VEE6	48	RVCO Analog ground
VEE7	55	Delay Analog ground
VEE8	33	TTL ground
VEE10	57	Chip Substrate ground
VCC1	6	Write Digital +5v
VCC2	59	Analog +5V

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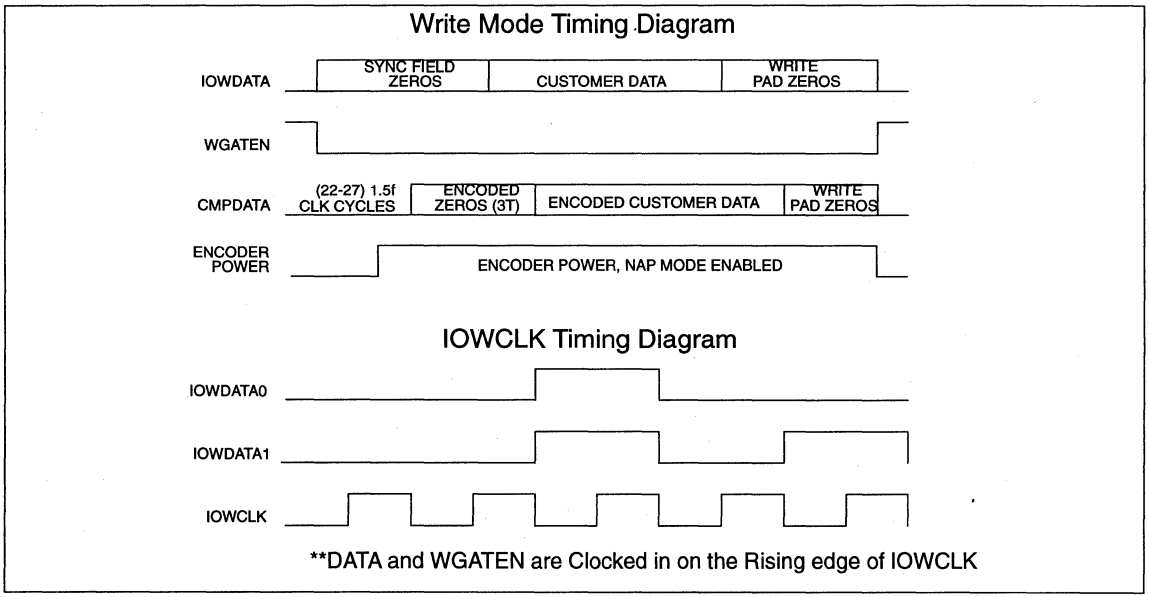
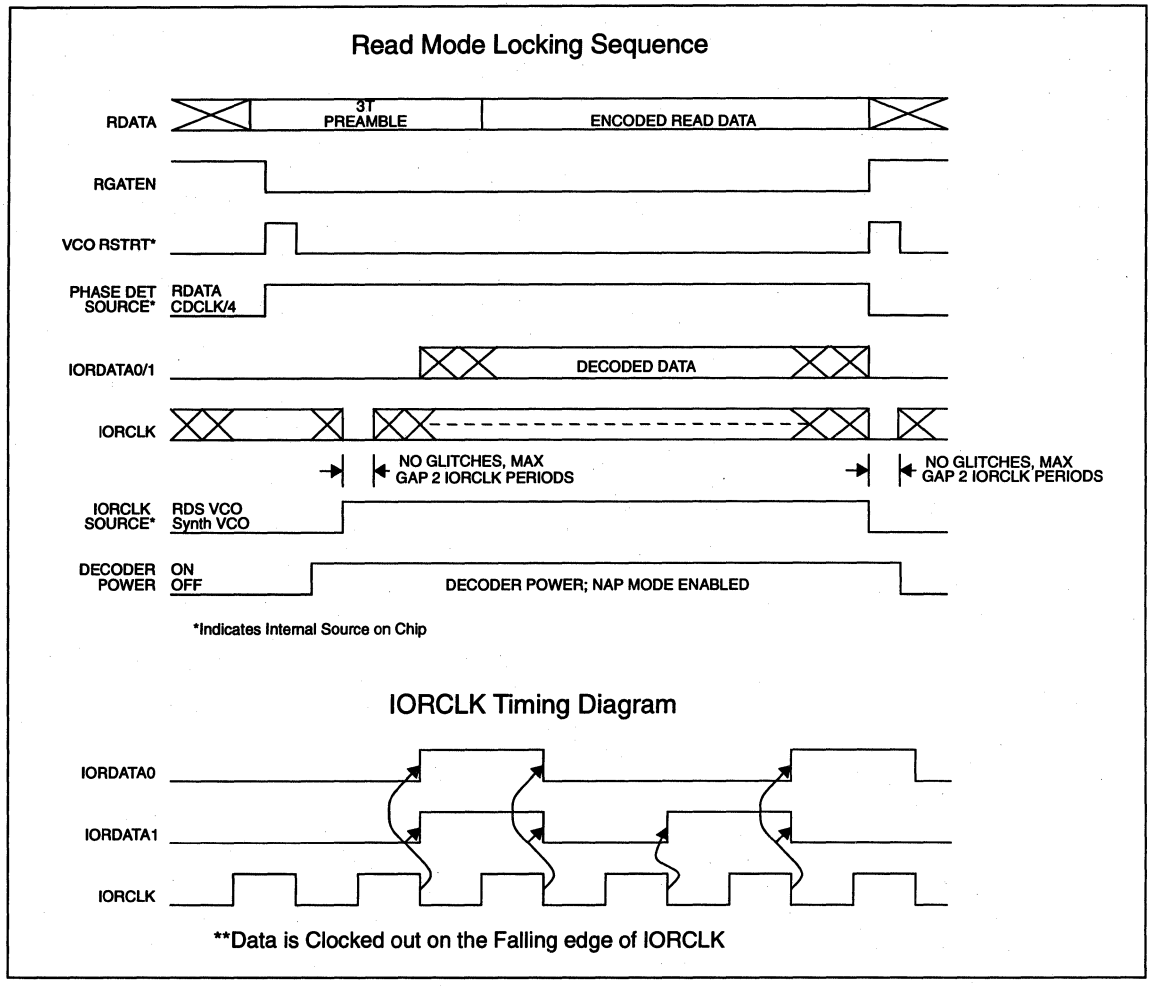
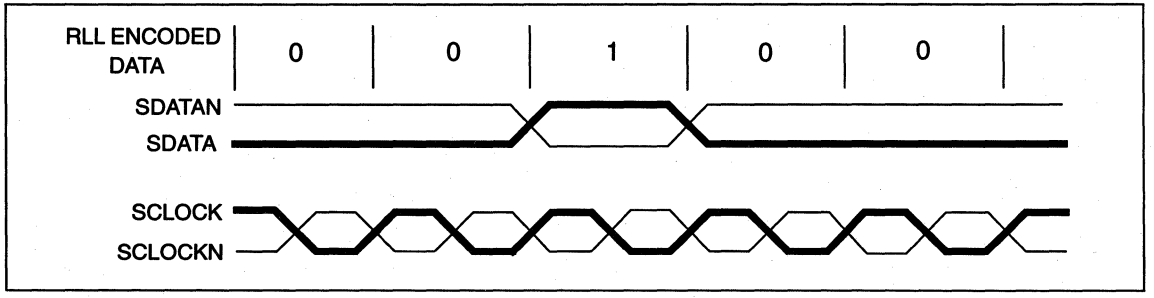
PIN NAME	PIN #	DESCRIPTION
VCC3	28	WPC Analog +5v
VCC4	1	SVCO Analog +5v
VCC5	45	Read Digital +5v
VCC6	47	RVCO Analog +5v
VCC7	54	Delay Analog +5v
VCC8	34	TTL +5V
VCC9	60	Synthesizer Analog +5v
VCC10	17	ECL +5v



WRITE DATA TIMING DIAGRAM



READ MODE LOCKING SEQUENCE



SYNCHRONIZED DATA AND CLOCK TIMING DIAGRAM

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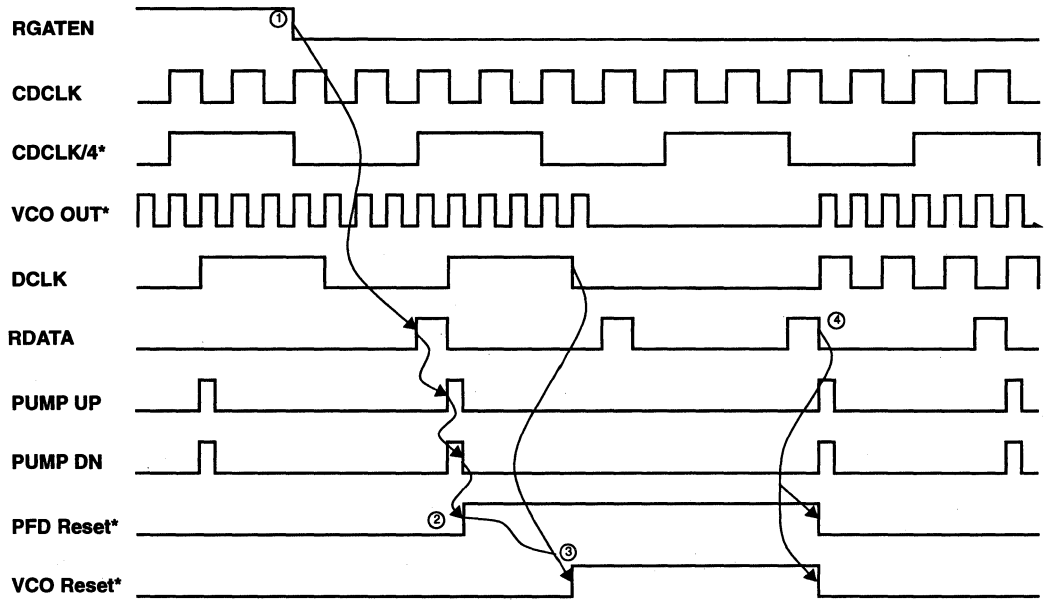


*Internal Signal

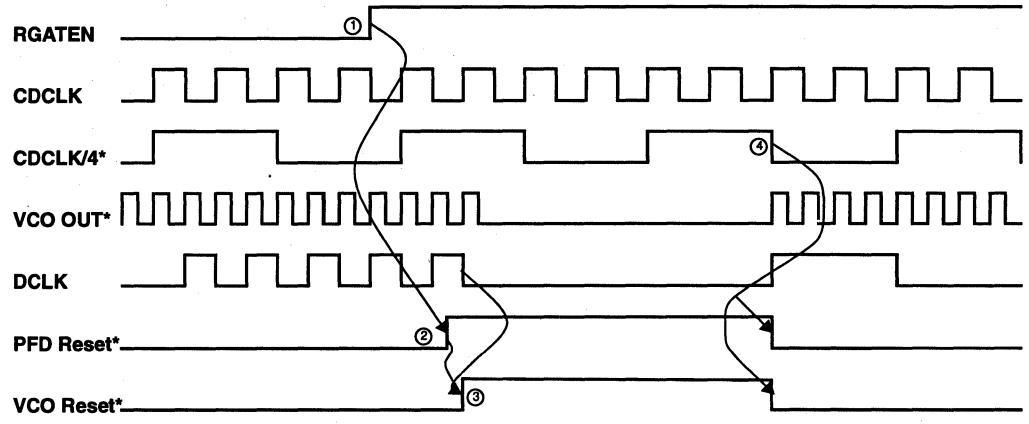
① Zero Phase Restart sequence begins with the RGATEN signal going low (Signaling an Idle to Read transistion)

② The RPFD is disabled following the next rising edge of RDATA, rising edge of pump up and falling edge of pump down from the RPFD, in respective order.

③ The VCO is stopped following the QPUMP being disabled and the next DCLK falling edge (thereby not causing any glitches)

④ After the falling edge of the third RDATA bit is sensed, the VCO and PFD are restarted, with the VCO in phase with the incoming data. The DCLK is now the VCO divided by two, Read Mode.

VCO ZERO-PHASE RESTART TIMING DIAGRAM, IDLE-TO-READ



*Internal Signal

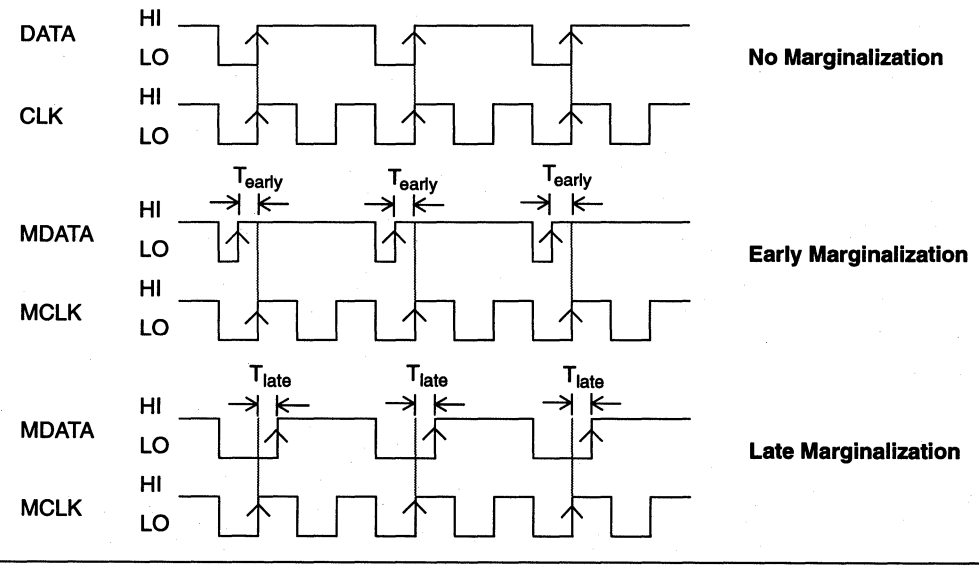
① Zero Phase Restart sequence begins with the RGATEN signal going high (Signaling a Read to Idle transistion)

② The PFD is disabled once the Decoder has completed switching the IORCLK signal from the RDS VCO to the Synth. VCO.

③ The VCO is stopped following the QPUMP being disabled and the next DCLK falling edge (thereby not causing any glitches)

④ After the falling edge of the second CDCLK/4 is sensed after the VCO has been stopped, the VCO and PFD are restarted, with the VCO in phase with the incoming data. The DCLK is now the VCO divided by eight, Idle Mode.

VCO ZERO-PHASE RESTART TIMING DIAGRAM, READ-TO-IDLE



MARGINALIZATION TIMING DIAGRAM

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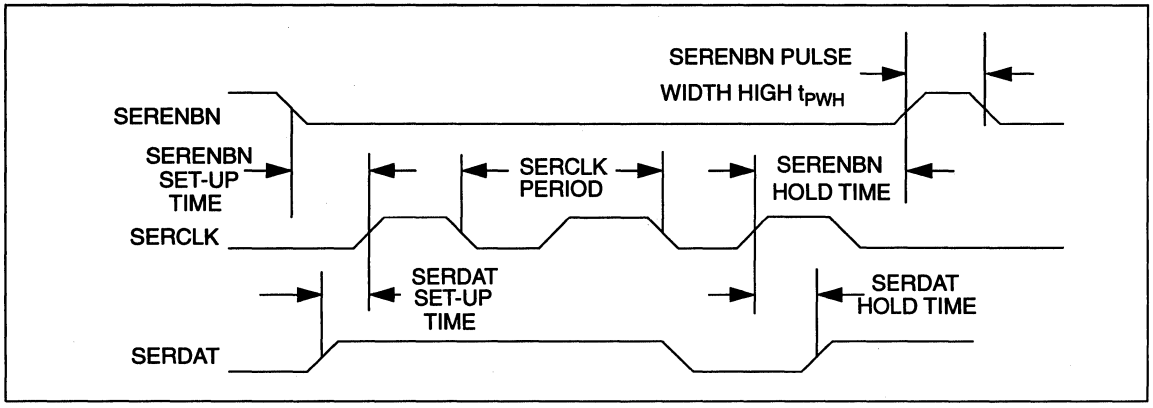
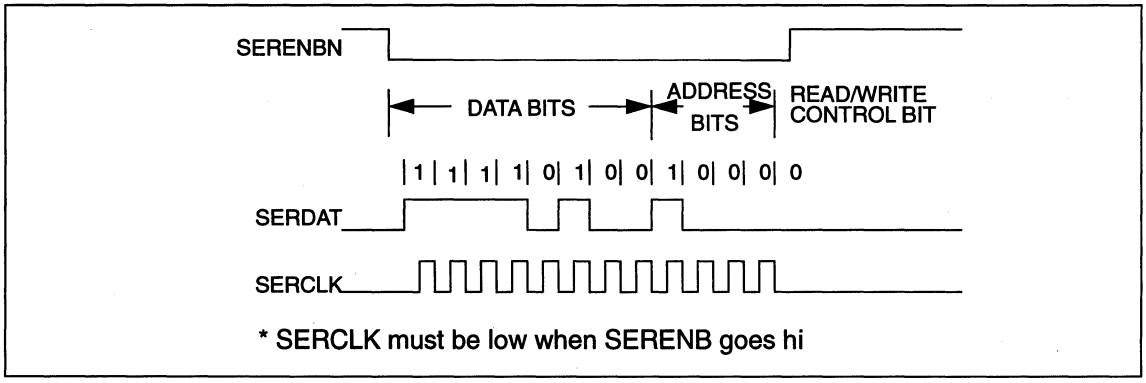
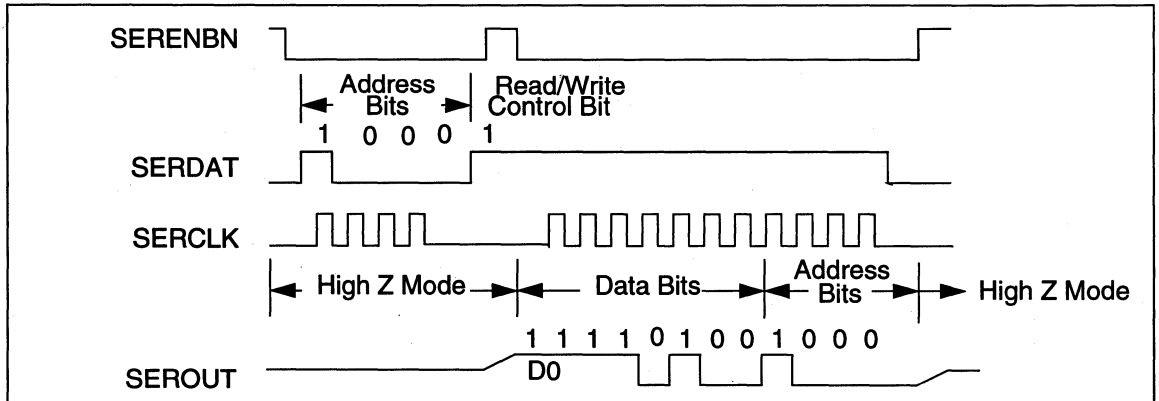


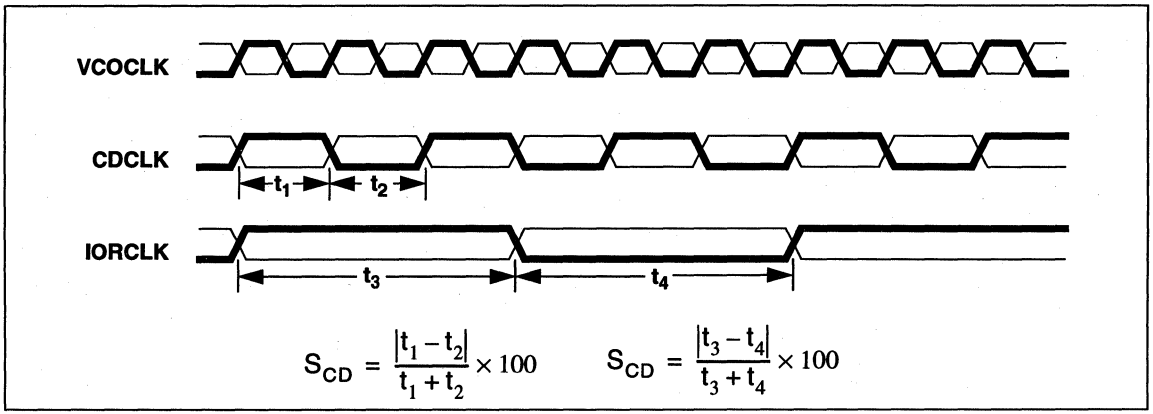
SERIAL INTERFACE TIMING DIAGRAM



LOADING INTERNAL REGISTERS WITH SERIAL INTERFACE TIMING DIAGRAM



READING INTERNAL REGISTERS WITH SERIAL INTERFACE TIMING DIAGRAM



Clock Symmetry Calculations

External Component Selection

COMPONENT	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R_{REXT}			1.68		6.0	kΩ
This resistor defines the range for the charge pump currents and vco center frequency.						

Encoder and Write Precompensation

PARAMETER	*SYM*	*CONDITONS*	*MIN*	*TYP*	*MAX*	*UNITS*
IOWDATA set-up time	$t_{sIOW-DATA}$		<5			ns
IOWDATA in hold time	$t_{hIOW-DATA}$		<2			ns
CMPDATA data phase noise	t_{jCD}			<50		ps

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DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, 0°C<TA<70°C, 4.5V<VCC<5.5V

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
TTL Inputs						
Input High Current	I_{IH}	VCC=5.5V; VIN=2.7V			20	µA
		VCC=5.5V; VIN=6.0V			100	µA
Input Low Current	I_{IL}	VCC=5.5V; VIN=0.5V			-0.6	µA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Clamp Volts	V_{IK}	I_{IN} = -18mA; VCC = 4.5V			-1.5	V
Differential PECL Input/Output Characteristics						
Common mode input voltage	V_{CIM}		Vcc-2.3		Vcc-0.3	V
Differential input voltage	V_{INDIF}		200		1220	mV
Input Current High	I_{IH}	VCC=5.5V; VIN = 4.6V			25	µA
Input Current Low	I_{IL}	VCC=5.5V; VIN = 3.6V			25	µA
Output High Voltage	V_{OH}	100Ω to VCC -2V	VCC-1.02		VCC-0.66	V
Output Low Voltage	V_{OL}	100Ω to VCC -2V	VCC-1.95		VCC-1.63	V
Single-Ended PECL (Notes 2 and 3)						
Input High Current	I_{IH}	VCC=5.0V			250	µA
Input Low Current	I_{IL}	VCC=5.0V			250	µA
Input High Voltage	V_{IH}		VCC-1.13		VCC-0.73	V
Input Low Voltage	V_{IL}		VCC-1.95		VCC-1.45	V
Output High Voltage	V_{OH}	100Ω to VCC -2V	VCC-1.02		VCC-0.66	V
Output Low Voltage	V_{OL}	100Ω to VCC -2V	VCC-1.95		VCC-1.63	V
Charge Pump Current: (R/SQPOUT Pins)			200		700	µA
Power Supply Current	I_{CC}	T=25°C, SLEEP=LO		130	235	mA
Power Supply Current	I_{CC}	T=25°C, SLEEP=HI			10	mA

Note 1: TTL inputs will float to a logic one if unconnected.
Note 2: ALL PECL inputs and outputs track with the VCC voltage supply.
Note 3: The differential outputs are open-emitter differential outputs requiring an external 511 ohm pull down resistor to VEE when in active use. The outputs should be allowed to float when not needed. A differential PECL receiver should be used to receive the signal. Single-ended PECL inputs float to a logic LO when left unconnected.

Dynamic (AC) Electrical Specifications
DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified $0°C<T_A<70°C$, $4.5V<V_{CC}<5.5V$
Frequency Synthesizer

COMPONENT	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCO phase noise (Note 3)	f_{VCO}			<50		ps
VCO center frequency variation	f_C		-10		+10	%
VCO maximum center frequency R_{REXT}=2kΩ, DAC setting=11111	f_{CMAX}			252		MHz
Maximum CLKIN (reference) frequency	f_{IN}				50	MHz
VCO dynamic range from f_c (Note 1)	f_{VCODR}		$\pm 0.20 f_c$		$\pm 0.35 f_c$	MHz
VCO gain (Note 2)	K_O			$0.44 f_c$		MHz/v
Charge pump output linearity (Note 2)	f_{LIN}		-10		+10	%
CDCLK Symmetry (See Diagram 8)	S_{CD}				±3	%
IORCLK Symmetry (See Diagram 8)	S_{IO}				±2	%
VCO output phase noise (Note 4)	σ_{vcoph}				45	psec rms
Rise time of any ECL output (20% to 80%, term = 50Ω to +3v)	t_r		0.7	1.0	3.8	ns
Fall time of any ECL output (20% to 80%, term = 50Ω to +3v)	t_f		0.7	1.0	4.4	ns
1σ phase jitter vs V_{CC} power supply ripple Lock range (center frequency = f_c)	$1\sigma_{fclr}$		$-0.1 f_c$		100 $+0.1 f_c$	ps MHz
SLEEP power up, time required before programming of the chip may begin SLEEP power down, time required for chip to reach specified sleep I_{CC} current					10 10	µs µs
Note 1: Conditions: f_c=223MHz, R_{REXT}=TBD, DAC Setting=10000 Note 2: Range is 0 to 2Π Note 3: M/N=TBD/TBD. Phase noise is measured with an HP5370B or equivalent counter, set for 10000 sample, and 1 sigma limit. Note 4: VCOIN=F_{REF}, DAC=10000, R_{REXT}=4000, f_c=96MHz nominal						

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Value the Customer™

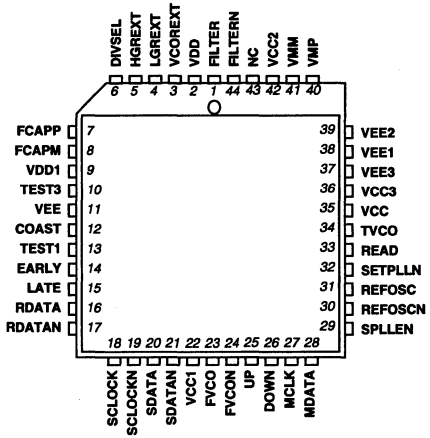
VM5351/VM5352
DATA SEPARATOR

August,1994

FEATURES

- Operates at Data Rates from 10 to 48 Mbits/sec (2,7) Code
- Operates at Data Rates from 10 to 64 Mbits/sec (1,7) Code
- Static Window Error Less Than 500 pS
- Zero Phase VCO Restart for Rapid Data Lockup
- Internal Silicon Delay Line
- Compatible with Zoned Density Recording Applications
- Contains Internal Window Marginalization Circuitry
- User Determined PLL Loop Filter Network
- Dual Gain PLL With External Control of PLL Loop Bandwidth
- PLL Free Run (Coast) Control
- Power Dissipation less than 1W
- VM5351 has Power Supplies of +5V and +12V
- VM5352 has Power Supplies of –5V and +5V

CONNECTION DIAGRAM

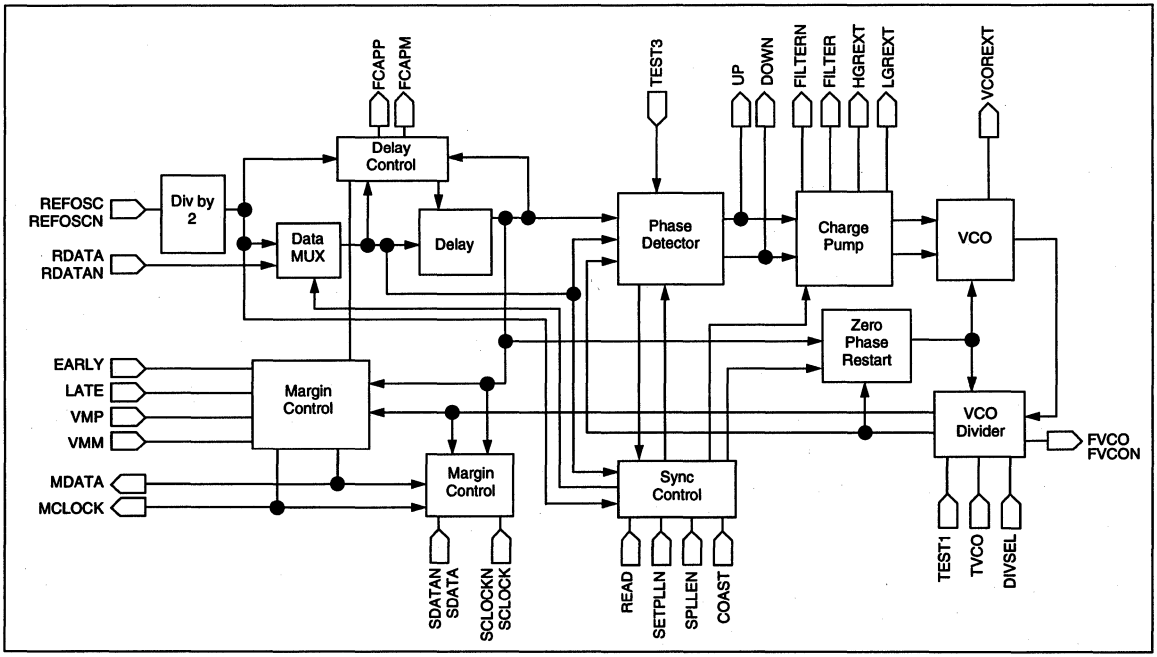


44-lead PLCC

DESCRIPTION

The VM5351/VM5352 is an integrated circuit designed to be used in high-performance data recovery systems. The data separator is a phase locked loop which provides a stable read clock of up to 96 MHz for system timing during the disk readback operation. It tracks the slow variations in the data frequency while eliminating noise and peak shifting in the data. The circuit will operate with either the (2,7) or (1,7) RLL codes. The VM5351/VM5352 uses the high-speed CBP (Complementary Bipolar Process).

BLOCK DIAGRAM



DATA RECOVERY CIRCUITS

ABSOLUTE MAXIMUM RATINGS

VM5351

Storage Temperature ..... -65° to +150°C
Ambient Operating Temperature ..... 0° to +70°C
Junction Operating Temperature ..... 0° to +125°C
Supply Voltage,
V_{CC} (V_{EE} = 0V, V_{DD} = 12V) ..... -0.5V to +6.5V
Voltage Applied to
TTL Inputs (V_{EE} = 0V) ..... -0.5V to V_{CC} +0.5V
ECL Inputs (V_{EE} = 0V) ..... 0 to V_{CC}
ECL Output Current - Continuous 25mA
- Surge 50mA
Maximum Power Dissipation 1300mW
Thermal Impedance, 44-lead PLCC
Junction-to-Case, Θ_{JC} ..... 10°C/W
Junction-to-Ambient, Θ_{JA} ..... 53°C/W

VM5352

Storage Temperature ..... -65° to +150°C
Ambient Operating Temperature ..... 0° to +70°C
Junction Operating Temperature ..... 0° to +125°C
Supply Voltage,
V_{DD} (V_{EE} = -5V, V_{CC} = 0V) ..... -0.5V to +6.5V
V_{EE} (V_{CC} = 0V, V_{DD} = 5V) ..... -6.5V to +0.5V
Voltage Applied to
TTL Inputs (V_{EE} = 0V) ..... -0.5V to V_{DD} +0.5V
ECL Inputs (V_{EE} = 0V) ..... 0 to V_{EE}
ECL Output Current - Continuous 25mA
- Surge 50mA
Maximum Power Dissipation 1200mW
Thermal Impedance, 44-lead PLCC
Junction-to-Case, Θ_{JC} ..... 10°C/W
Junction-to-Ambient, Θ_{JA} ..... 53°C/W

READ OPERATION

There are three states in the read PLL locking sequence:

1. Lock to the reference oscillator
2. Lock to the preamble data in high gain
3. Lock to data in low gain.

Initially, the data separator locks to the REFOSC input. This is a standby state which the data separator is in when not reading data. The VCO runs at a frequency which is very close to that required when locking to the data stream. This minimizes the frequency step when the PLL input is switched to data. In this state of operation, the phase detector is in the phase/frequency mode which guarantees non-harmonic lock up. The charge pump is sourcing high-gain currents. The higher loop gain ensures rapid lock of the PLL.

The assertion of the READ gate initiates the read operation. Internally, the part waits for the first data bit and then switches the input to the PLL from REFOSC to RDATA. At this time, the VCO is momentarily stopped and restarted in phase with the first data bit in the preamble. This allows very fast and repeatable lockup to the preamble field. The loop is still in a high gain mode so any remaining phase error is due to the zero phase restart is quickly tracked out. The phase detector is in a phase mode which allows the PLL to lock to harmonics. This also allows great flexibility in the preamble pattern. The user could actually lock up in the middle of a data field if so desired. The length of the preamble lock can be controlled in two ways. It may be controlled externally by the SETPLLN input or automatically limited to 32 REFOSC clock cycles. The SPLLEN pin selects which method of control is used.

After the preamble lockup is over, the PLL switches to the lock-to-data mode and the data is read. In this mode, the charge pump is sourcing low-gain currents. This forms a low-gain loop which is desirable for reading data. The loop becomes less responsive to bit shift in the data stream.

When the read operation is complete, READ gate is brought high, a zero phase restart of the VCO is performed and the PLL locks to the reference oscillator once again. Refer to Figure 1 for Read Timing Diagrams.

CIRCUIT BLOCK DESCRIPTION

The circuit is composed of the following functional blocks: high-precision phase-frequency detector, differential charge pump, differential input VCO, filter, zero phase VCO restart, divider, data standardizer and synchronization control block. Refer to the block diagram.

SYNC Control

The sync control block controls the input multiplexer, the phase/frequency detector, the charge pump gain and the divider setting. It guarantees that the phase locked loop switches smoothly from one mode to another. The control pin setting and corresponding modes are summarized in the table below.

READ	*SETPLLN*	*GAIN*	*MUXSEL*	*DIVIDER*	*PHASE/FREQ DET*
1	X	High	REFOSC	div by 4	Phase/Freq. Mode
0	X	Low	DATA	div by 2	Phase Mode
1	X	High	REFOSC	div by 4	Phase/Freq. Mode
0	1	High	DATA	div by 2	Phas Mode
0	0	Low	DATA	div by 2	Phase Mode

1 = Logic HI, 0 = Logic LO, X = Don't Care

This table shows that when SPLLEN is HI, the high-to-low gain switch is controlled externally by the SETPLLN pin. If the SPLLEN pin is LO, the loop automatically switches from high-to-low gain 32 REFOSC clock cycles after READ gate is asserted. The above table assumes that DIVSEL is LO, meaning that the extra divide-by-two is not in the VCO feedback path.

Delay Line

The VM5351/VM5352 uses an internal delay line to delay the data coming into the phase detector. The delay allows the phase detector to anticipate incoming data and enable a phase comparison to occur. The delay is nominally one half of the REFOSC period. A separate control loop regulates the propagation delay through the delay line by comparing it to the REFOSC frequency. This delay line configuration relies only on the REFOSC frequency and is insensitive to external components, supply voltage, temperature and IC processing. It requires that the reference oscillator frequency be present at all times and that there be no extended gaps in the data when READ gate is active.

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Data Mux and Phase/Frequency Detector

The two highest frequency inputs to the data separator are the REFOSC and the RDATA pins. The REFOSC pin is tied to an external reference oscillator or servo reference. The PLL locks to the REFOSC input when no data is being read from the disk. The REFOSC signal must be present at all times because it is used in the anticipator delay circuitry. The RDATA pin is the input for the raw data and is tied to the output of the pulse detector circuit in the disk drive. Because these two signals are the highest frequencies coming onto the chip, they are differential ECL inputs. This helps reduce unwanted coupling of these signals into the PLL. A multiplexer DATA MUX is used to select which input (REFOSC or RDATA) the PLL will lock to.

The output of the anticipator delay goes to the PLL input of the phase/frequency detector (PFD) block. The phase/ frequency detector has two modes of operation, the phase/frequency mode and phase mode. Each mode is described below.

The phase/frequency mode allows the phase detector to detect both phase and frequency of the two incoming signals. This mode does not allow the PLL to lock to harmonics of the reference input. The phase/frequency mode is used along with the charge pump high gain mode and the filter high bandwidth mode to form a high gain-high bandwidth loop for fast lock up times. This mode is used when locking to the reference oscillator and the preamble. The reference input to the PFD initiates an UP signal to the charge pump, and the VCO feedback input initiates a DOWN signal to the charge pump. When both UP and DOWN are high, the internal flip-flops are reset and the signals return low again. The minimum pulse width of the UP and DOWN signals is determined by internal propagation delays and is approximately 5 ns. In a locked state, the rising and falling edges of the UP and DOWN signals are coincident and there is no net effect on the PLL phase and frequency.

When in the phase mode, the PFD detects only the phase of the two inputs. The phase mode is used whenever READ gate is asserted. The anticipator delay value is one half a REFOSC period window and is used to condition the phase detector for a phase comparison. The operation of the phase detector is the same as in the phase/frequency mode except that a phase comparison cannot be initiated until a data pulse is input to the phase detector. This allows to the PLL to lock to harmonics of the VCO frequency.

Charge Pump

The charge pump uses high speed NPN and PNP switches to source current in and out of the FILTER pin. The UP and DOWN signals from the phase detector feed into the charge pump and cause it to pump current in or out of the differential lead-lag filter. The high speed current switches in the charge pump sink or source current out of the FILTER pin, as determined by the UP and DOWN inputs. The FILTERN side of the filter acts as a voltage source. The high and low gain current are set by external resistors connected to the HGREXT and LGREXT pins. The high gain current can be varied from 0.5 to 2.0 mA by adjusting the HGREXT resistor. The low gain current can be varied from 100 to 400 μA by adjusting the LGREXT resistor. This allows the user to vary the high gain/low gain current ratio from 20:1 to 5:4.

Filter

The filter resides external to the chip, allowing the system designer to control the loop dynamics. It is composed of two capacitors and one resistor. Refer to the VM5351/VM5352/ VM5353 Application Note.

VCO

The VCO is a multi-vibrator type oscillator which has good linearity over its frequency range. The differential voltage between the FILTER and FILTERN pins controls the VCO frequency. The VCO center frequency occurs when the differential voltage across FILTER and FILTERN is zero. An external resistor tied from the VCOREXT pin to VEE sets the VCO center frequency and gain.

Divider

The divider block divides down the VCO frequency. It is composed of several divide-by-two sub blocks which can be switched in and out. The VCO frequency is split into to separate signals which are divided down individually. One of the divided VCO signals is routed to the data standardizer and margin control blocks. This is a straight divide-by-two at all times. The other divided VCO signal wraps around back into the phase-frequency detector to complete the loop. This division is switchable from a divide-by-two to a divide-by-four. The VCO divided-by-two is used when the phase-frequency detector is in the phase (harmonic) mode. The VCO divided-by-four is used when the phase-frequency detector is in the phase-frequency mode and the PLL is locking to REFOSC. This matches the REFOSC divided-by-two frequency. Refer to the block diagram.

The DIVSEL pin can be used to insert an extra divide-by-two into the front end of the divider block to extend the lower end of VCO range without changing the VCOREXT resistor. This is used when operating at lower data rates ($f \leq 15$MBS).

The divider block can be put into a test mode by forcing the TEST1 pin to a logic low. This switches an internal mux that allows an external frequency to be injected into the divider through the TVCO input pin.

Data Standardizer

The divided VCO clock and data input to the PLL contain clock and data information needed but are not synchronized to one another. For this reason, they are put through a data standardizer which takes out any bit shift in the data and puts the bit in a decode window. The data standardizer uses the falling edge of the divided VCO clock to generate the decode window. The rising edge of the clock output SCLOCK is centered in the middle of the synchronized data output SDATA. The rising edge of the SCLOCK indicates the data is valid and clocks the data bit into the decoder circuitry of a decoder IC. The SCLOCK and SDATA outputs are differential ECL signals. A Synchronized Data and Clock Timing Diagram is shown in Figure 3.

Zero Phase Restart

A zero phase restart of the VCO is performed both when switching from the reference oscillator to data and vice versa. The loop is in a high gain mode whenever a zero phase restart occurs. This allows fast lockup to the preamble field and when going back to the idle state. The zero phase restart block interfaces to several other blocks on the chip and guarantees a

sequence of events when the switch happens. No spurious data or clock signals will occur when READ gate is switched. Timing diagrams for the VCO Zero-Phase Restart are shown in Figure 4.

Window Marginalization

The VM5351/VM5352 contains circuitry which can be used to artificially shift the data bit in the clock window. This function can be used either for system calibration or for rereading blocks of data with altered phase during a READ retry. The marginalization block takes the data and clock from the PLL and allows the user to vary the phase of the two signals before they enter the data standardizer. The magnitude of the phase shift is controlled by the differential voltage between two analog input pins, VMP and VMM. An external resistor divider can be tied to VMP and VMM to set the phase shift. The MCLK and MDATA outputs are the phase shifted clock and data signals. The user can see how much the bit is being shifted by looking at the phasing of MCLK and MDATA. When the bit is exactly centered, the rising edge of MDATA should fall exactly in the center of the falling edges of MCLK. The EARLY and LATE pins are control signals for the marginalization block. When data is to arrive before the clock, the EARLY signal is asserted. When data is to arrive after the clock, the LATE signal is asserted. Under normal operation (when marginalization is not being used), both EARLY and LATE pins float HI, the marginalization circuitry is powered down, MCLK and MDATA float to an intermediate ECL level, and the marginalization block plays no role in the data synchronization. Marginalization Timing Diagrams are shown in Figure 2.

Zoned Density Recording

The VM5351/VM5352 can be used with zoned density recording. The synthesized frequency is brought into the REFOSC input. Different values for the VCOREXT resistor must be switched in and out using an external analog switch when changing the VCO center frequency. A zero temperature coefficient current DAC will not work well to set up the VCO center frequency. This is because the VCO requires a negative temperature coefficient current to give a constant VCO frequency over temperature.

PIN DESCRIPTIONS

DIGITAL INPUTS:

REFOSC, REFOSCN: Reference oscillator which the PLL locks to when in the idle state. A differential ECL input. REFOSC frequencies for the different data rates and codes are:

DATA RATE - f	*1/2 (2,7) - 2f*	*2/3 (1,7) - 1.5f*
64 Mbits/sec	—	96 MHz
48 Mbits/sec	96 MHz	72 MHz
30 Mbits/sec	60 MHz	45 MHz
25 Mbits/sec	50 MHz	37.5 MHz
20 Mbits/sec	40 MHz	30 MHz
15 Mbits/sec	30 MHz	22.5 MHz
10 Mbits/sec	20 MHz	15 MHz

REFOSC minimum pulse width high and low: 4ns. The duty cycle of REFOSC is not critical.

RDATA, RDATAN: Encoded read data from the disk drive read channel, active high. RDATA minimum pulse width: 4ns. A differential ECL input.

READ: A TTL control input which when low initiates lock up to data. When high, the PLL is in an idle state and locks to the REFOSC signal.

SETPLLN: A TTL input which when activated in conjunction with READ gate determines the bandwidth mode of the PLL. The SPLLEN pin must be floating high to enable the SETPLLN input.

SPLLEN: An input which selects the procedure for switching the PLL to the low gain mode. It allows an automatic switch to low gain or a manual switch to low gain using the SETPLLN pin.

SPLLEN	MODE
Tied to V_{EE}	The loop automatically goes to low gain 32 REFOSC clock cycles after READ gate is asserted. The SETPLLN pin is disabled.
Floating	SETPLLN input is enabled and controls when the loop is in high and low gain.

EARLY, LATE: TTL inputs which enable the marginalization circuitry and force the data to arrive early or late in the bit window. Both pins are active low.

EARLY	LATE	MODE
0	0	Shift data early in the bit window
0	1	Shift data early in the bit window
1	0	Shift data late in the bit window
1	1	Normal operation, marginalization disabled

COAST: A TTL input which controls the coast function on the data separator. When the coast input is a logic low, the phase detector is cleared and held in a reset state, allowing the VCO to coast regardless of the incoming data. This happens synchronously within the circuit. When a logical high, the phase detector operates normally.

COAST	MODE
Tied to V_{EE} (VM5351)	VCO coast
Tied to V_{CC} (VM5352)	
Floating	Normal operation

DIVSEL: An input used to switch in and out an extra divide-by-two in the VCO divider block. The extra divide by two can be used to extend the low end frequency range of the VCO.

DIVSEL	MODE
Tied to V_{EE}	Extra divide by two switched out. (f_o above 60MHz)
Floating	Extra divide by two switched in. (f_o below 60MHz)

TEST1: An input used to enable a test feature on the data separator. When enabled, it allows an external VCO frequency signal to be injected into the divider block through the TVCO pin. For test purposes only.

TEST1	MODE
Tied to V_{EE}	External VCO frequency injected into divider block.
Floating	Normal operation

TEST3: An input used to enable a test feature on the data separator. When enabled, it forces the phase detector into a phase-frequency detector at all times. For test purposes only.

TEST3	MODE
Tied to V_{EE}	Phase detector in phase frequency mode at all times.
Floating	Normal operation

TVCO: The test VCO input pin. This input is enabled by the TEST1 control pin. This is a TTL input.

DIGITAL OUTPUTS:

SDATA, SDATAN: Encoded data read from the disk which is synchronous with the falling edge of the Data Clock. SDATA is active high. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. A differential ECL receiver should be used to receive the signal.

SCLOCK, SCLOCKN: Data clock output referenced to the VCO which is synchronous with the Synchronized Data. The rising edge of SCLOCK indicates the presence of valid data on SDATA. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. A differential ECL receiver should be used to receive the signal.

FVCO, FVCON: Output frequency of the VCO available for data decoding. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. The outputs should be allowed to float when not needed. A differential ECL receiver should be used to receive the signal.

Nominal FVCO output frequencies for the specified data rates and coding schemes are given below.

DATA RATE - f	*DIVSEL*	*1/2 (2,7) - 4f*	*2/3 (1,7) - 3f*
64 Mbits/sec	V_{EE}	———	192 MHz
48 Mbits/sec	V_{EE}	192 MHz	144 MHz
30 Mbits/sec	V_{EE}	120 MHz	90 MHz
25 Mbits/sec	V_{EE}	100 MHz	75 MHz
20 Mbits/sec	V_{EE}	80 MHz	60 MHz
15 Mbits/sec	Float	60 MHz	45 MHz
10 Mbits/sec	Float	40 MHz	30 MHz

When DIVSEL is low, the FVCO pin outputs the actual frequency of the internal VCO frequency divided by two.

UP: Active high whenever the phase detector issues a pump up to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed.

DOWN: Active high whenever the phase detector issues a pump down to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed.

MCLK: Clock signal that has been phase shifted for marginalization. This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed. MCLOCK is active on the rising edge.

MDATA: This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed. MDATA is active high.

ANALOG PINS:

VCOREXT: Used to bias up the current source that sets the VCO center frequency f_o. An external resistor is tied from this pin to the most negative supply voltage (V_{EE}). The voltage on the VCOREXT pin is typically V_{EE} + 2.8 volts with an ambient temperature of 25°C. The VCOREXT resistor is R6 in the typical connection diagram in Figures 5 and 6. The VCOREXT resistor value vs. VCO center frequency can be calculated from the following equation:

$$R_{VCOREXT}(k\Omega) = 0.268 + \frac{223.2}{f_o} + \frac{7632}{f_o^2}(k\Omega) \qquad \textit{(eq. 1)}$$

where f_o is in MHz. For an example of f_o = 70MHz;

$$R_{VCOREXT}(k\Omega) = 0.268 + \frac{223.2}{70} + \frac{7632}{4900} = 5.01k\Omega \qquad \textit{(eq. 2)}$$

The VCO is at its center frequency when there is zero differential voltage across the FILTER and FILTERN pins. The FILTER and FILTERN pins may be shorted together to measure the center frequency. Note that the frequency observed at FVCO, FVCON is either the VCO frequency or VCO frequency divided by two, depending on the DIVSEL pin setting.

HGREXT: Used to set the magnitude of the high gain current for the charge pump. Normally a resistor will be tied from this pin to the most negative supply of the IC. The voltage on the HGREXT pin is typically V_{EE} +1.18 volts. The user may vary the high gain charge pump current from 0.5mA to 2.0mA. The HGREXT resistor can be calculated from the following equation:

$$HGREXT(\Omega) = \frac{1.18\,(V)}{(\text{High gain charge pump current})} \qquad \textit{(eq. 3)}$$

Refer to Figures 5 and 6, R_2 is typical HGREXT register.

LGREXT: Used to set the magnitude of the low gain current for the charge pump. Normally a resistor will be tied from this pin to the most negative supply of the IC. The voltage on the LGREXT pin is typically V_{EE} +1.18 volts. The user may vary the low gain charge pump current from 100µA to 400µA. The LGREXT resistor can be calculated from the following equation:

$$\text{HLGREXT}(\Omega) = \frac{1.18\,(\text{V})}{(\text{Low gain charge pump current})} \quad \textit{(eq. 4)}$$

Refer to Figures 5 and 6, R_4 is typical HGREXT resistor.

FCAPP, FCAPM: Differential loop filter pins for the delay control feedback loop. A large capacitor is placed across these pins, typically 0.5µF.

FILTER, FILTERN: Differential loop filter pins for the main phase locked loop. These outputs are referenced to VDD and will therefore track with VDD. The FILTER pin is the high impedance side of filter. The FILTERN pin is always a low impedance voltage source which is inversely proportional to the voltage on the FILTER pin.

$$\Delta V_{FILTER} = (-1) \bullet \Delta V_{FILTERN} \quad \textit{(eq. 5)}$$

The DC voltage crossover point for FILTER and FILTERN is approximately (VDD – 4.75V). The differential range is ± 3V. The VCO center frequency f_o is defined as the VCO frequency when the VCO control voltage is at the middle of its range. This occurs when there is zero differential voltage across FILTER and FILTERN. The VCO frequency can be controlled directly by forcing the voltage on the FILTER pin. VCO gain can then be measured by plotting the differential voltage across FILTER and FILTERN vs. FVCO frequency and calculating the slope of the line.

VMP, VMM: Analog pins which control the magnitude of the phase shift introduced by the marginalization circuitry. VMP acts as a voltage source of approximately (V_{EE} + 3.2V) and can source up to 2.0mA. VMM is a high impedance analog input. When VMP and VMM are shorted together, the data and clock (MCLK and MDATA) are in phase. As the voltage on VMM decreases (the differential voltage between VMP and VMM increases), the phase shift between MDATA and MCLK increases. The shift can be related to the differential voltage and REFOSC period by the following expression:

$$t_{SHIFT} = 0.286(T_{REFOSC})(V_{VMP} - V_{VMM}) \quad \textit{(eq. 6)}$$

t_{SHIFT} and T_{REFOSC} are in units of ns, and (V_{VMP} - V_{VMM}) in units of volts. Typically a variable resistor (R11 in the Typical Connection Diagram, Figures 5 and 6) is put across VMP and VMM and a 3.0kΩ resistor (R10 in the typical connection diagram, Figures 5 and 6) between VMM and V_{EE}. The variable resistor can be used to control the phase shift of MDATA and MCLK. The bottom resistor could be replaced by a current output DAC but the phasing accuracy from part to part may suffer slightly, particularly when marginalizing more than 5% of the decode window. If marginalization is not being used, VMM should be tied to VMP and not to external components.

SUPPLY PINS:

VEE: Most negative digital supply.

VEE1: Most negative analog supply.

VEE2: Most negative VCO supply.

VEE3: Most negative supply for delay.

VCC: Digital middle supply 5 volts greater than VEE.

VCC1: ECL supply 5 volts greater than VEE.

VCC2: VCO supply 5 volts greater than VEE2.

VCC3: Delay control supply 5 volts greater than VEE3.

VDD: Most positive digital supply.

VDD1: Most positive analog supply.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

The data separator is inherently a sensitive circuit, and thus circuit performance can be degraded significantly without careful attention to board layout. The following guidelines should be followed:

1. V_{EE}, V_{CC} and V_{DD} supply bypass filtering should be liberal and as close to the supply pins as possible. Ideally, a bypass capacitor should be soldered directly to each supply pin. The electrical lead length of the bypass capacitors between the supply and ground pins should be minimized to reduce lead inductance. Only high-quality capacitors should be used.
2. Use the main digital ground plane for all grounding associated with the device.
3. Locate all passive components associated with the chip as close to their respective device pins as possible. It is extremely critical that the PLL filters be very tightly spaced. In addition the $R_{VCOREXT}$ resistor should be tightly spaced or located closely to the VCOREXT pin. Chip capacitors and resistors work very well for these filters.
4. For best performance, the chip pins should be soldered directly to the printed circuit board. If a socket must be used, a low-profile, low-resistance, forced-insertion type socket is recommended.
5. Allow any unused digital outputs to float, unconnected to any other traces.
6. Very fast ECL edge rates should be avoided. Rise/Fall times for the differential ECL signals (REFOSC AND RDATA) should not exceed 2.5ns. If 10KH drivers are used, a 100Ω series resistor works well to reduce the edge speeds

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DC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	I_{CC}			129.3	170	mA
	I_{DD}			22.3	40	mA
Power Dissipation	P_D	$V_{DD} = 13.2V$, $V_{CC} = 5.5V$		1.02	1.3	W
Charge Pump		High gain	0.5		2	mA
		Low gain	0.1		0.4	mA
TTL Inputs (Note 1)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current High	I_{IH}	$V_{IH} = 2.7V$, $V_{CC} = 5.5V$			20	µA
		$V_{IH} = 6V$, $V_{CC} = 5.5V$			100	
Input Current Low	I_{IL}	$V_{IN} = 0.5V$, $V_{CC} = 5.5V$			-0.6	mA
Differential ECL Inputs (Note 2)						
			V_{CC} - 2.3			V
			200			mV
Input High Current	I_{IH}	$V_{CC} = 5.5V$			25	µA
Input Low Current	I_{IL}	$V_{CC} = 5.5V$			25	µA
Voltage Output High	V_{OH}		V_{CC} - 1.02		V_{CC} - 0.66	V
Voltage Output Low	V_{OL}		V_{CC} - 1.95		V_{CC} - 1.63	V

Note 1: TTL inputs will float to a logic HI if left unconnected.
Note 2: All inputs and outputs denoted as ECL track with the V_{CC} supply voltage.

EXTERNAL COMPONENT SELECTION

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
RHGREXT			590		2400	Ω
RLGREXT			2.95		12	kΩ
RVCOREXT			1.6		6	kΩ
VMP Series Resistor to Ground			2		5	kΩ
FCAPP, FCAPM Capacitor				0.5		µF

AC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
REFOSC, REFOSCN Period	T_{REFOSC}		10			ns
REFOSC, REFOSCN Pulse Width	$t_{pwREFOSC}$		4			ns
RDATA, RDATAN Pulse Width	$t_{pwRDATA}$		4			ns
Window Center Offset	t_{WINDOW}			<300		ps
Delay Line Propagation Delay	t_{pDL}			Note 1		ns
VCO Phase Noise	ϕ_{VCO}	Locked to preamble, 1σ (note 2)		<50		ps
VCO Center Frequency Variation	Δf_o	@ f_o = 70MHz	-10		+10	%
VCO Zero Phase Restart Error	t_{ZPR}			<1		ns
VCO Maximum Center Frequency	f_{cMAX}			192		MHz
VCO Dynamic Range from f_o	f_{VCODR}	f_o = 70MHz, $R_{VCOREXT}$ = 4.9kΩ	$0.7f_o$		$1.3f_o$	MHz
VCO Gain	K_O	f_o = 70MHz, $R_{VCOREXT}$ = 4.9kΩ	$0.9f_o$	$0.105f_o$	$0.13f_o$	MHz/V
Charge Pump Output Linearity	f_{LIN}	Range is 0 to 2π	-10		+10	%
SCLOCK Duty Clock	t_{dcSCLK}			50		%
Propagation Delay from SCLOCK Negative Edge to SDATA Rising Edge	t_{pdSD}	C_{load} = 20pF		$-1.5 < t_{pdSD} < 1.5$		ns
Propagation Delay from FVCO Rising Edge to SCLOCK Rising Edge	t_{pdSCLK}	C_{load} = 20pF		$-2 < t_{pdSCLK} < 4$		ns
Marginalization Maximum Shift	$t_{MAXMARG}$			0.25 (T_{REFOSC})		ns
Marginalization Variation from Nominal	t_{MARG}	$V_{VMP} - V_{VMM}$ = 100mV		±0.02 (T_{REFOSC})		ns

Note 1: Nominal value for t_{pDL} is: $[0.5(T_{REFOSC}) - 1] < t_{pDL} < [0.5(T_{REFOSC}) + 1]$.
Note 2: VCOCLK output 1σ point measured over 10,000 samples on an HP5370B time interval counter. $\sigma_{fcl} = \sqrt{\sigma_a^2 - \sigma_b^2}$, where σ_a = rms jitter measurement and σ_b = self jitter of HP5370B (see HP app. note 191-4).

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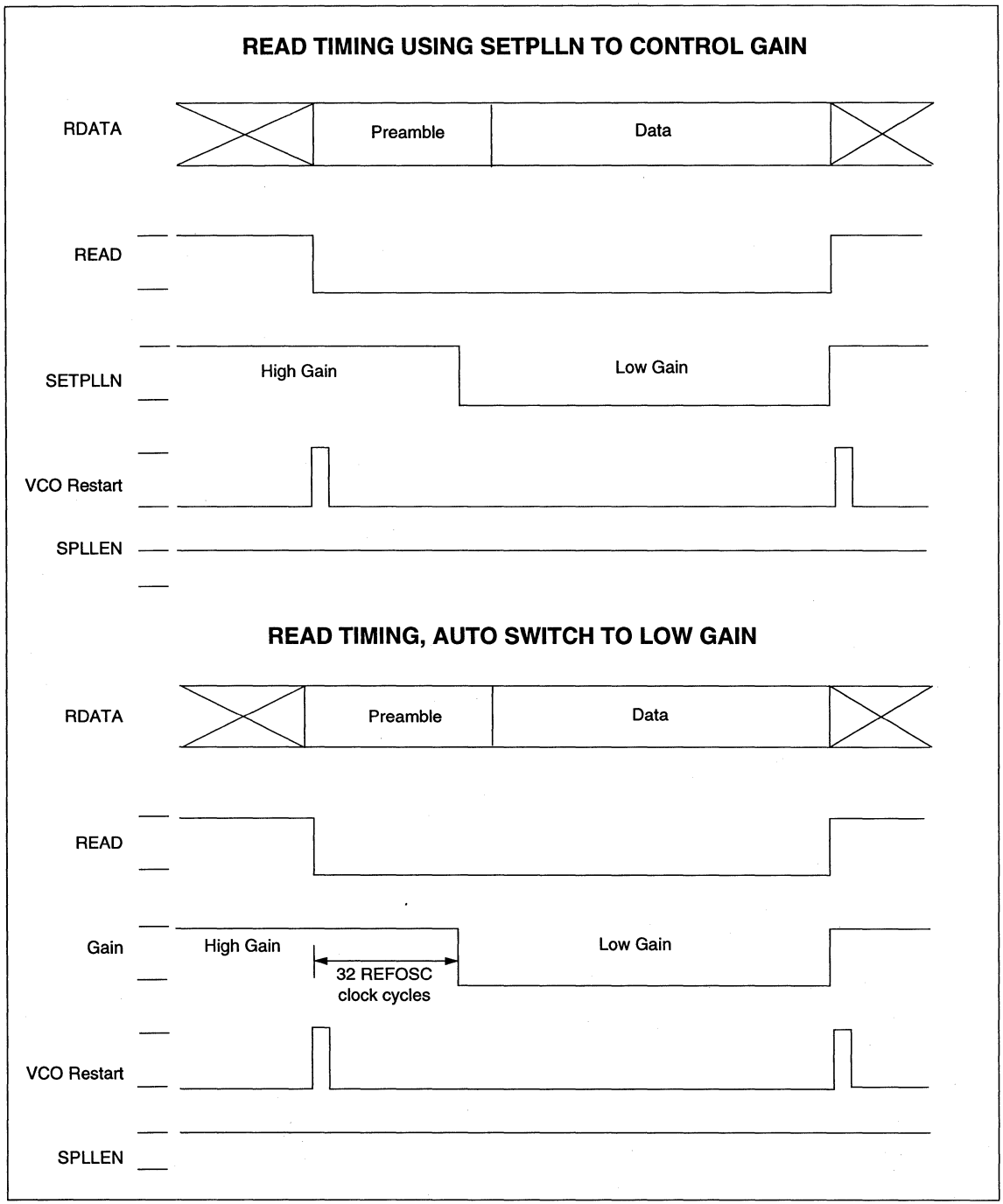

Figure 1: Read Timing Diagrams

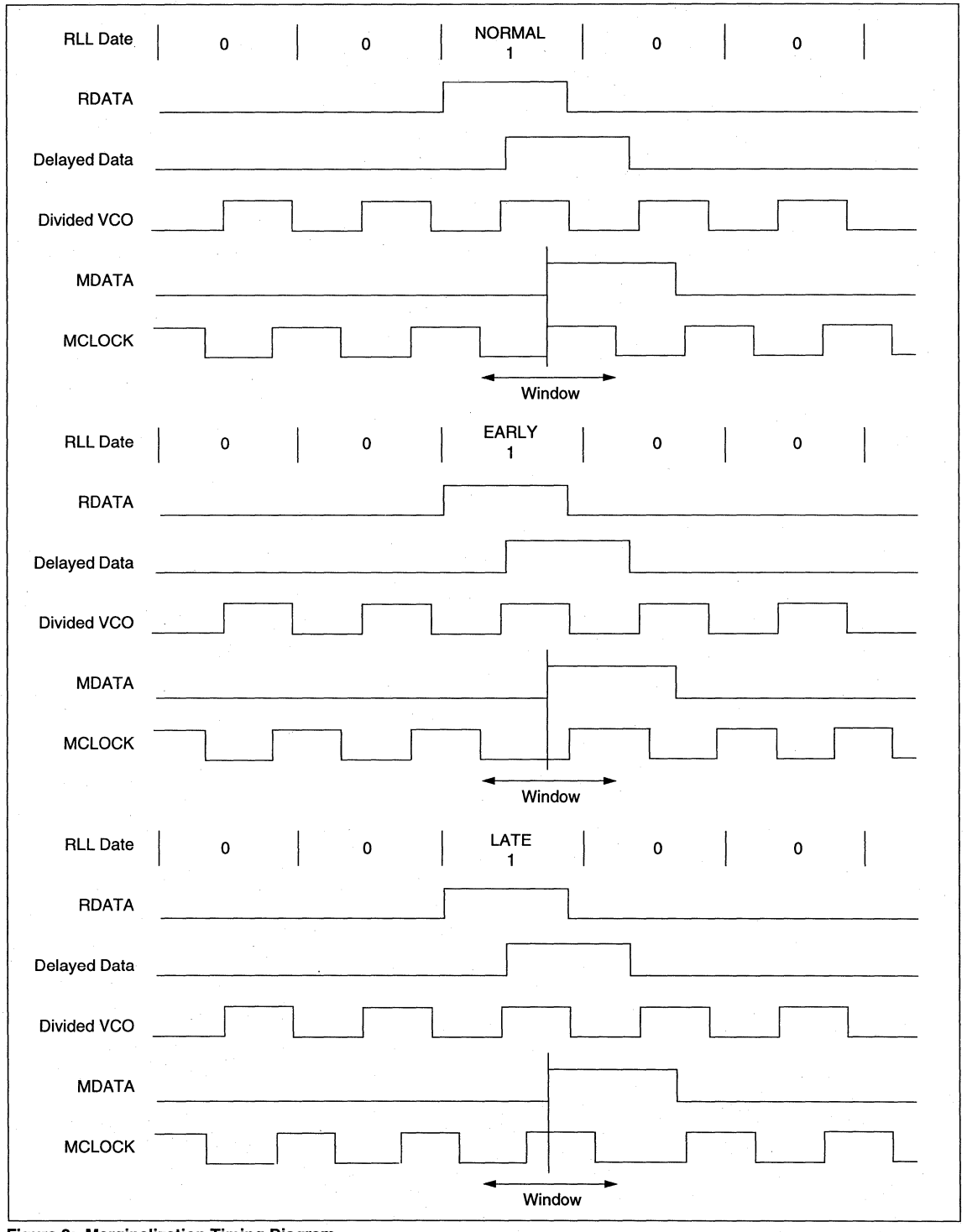

Figure 2: Marginalization Timing Diagram

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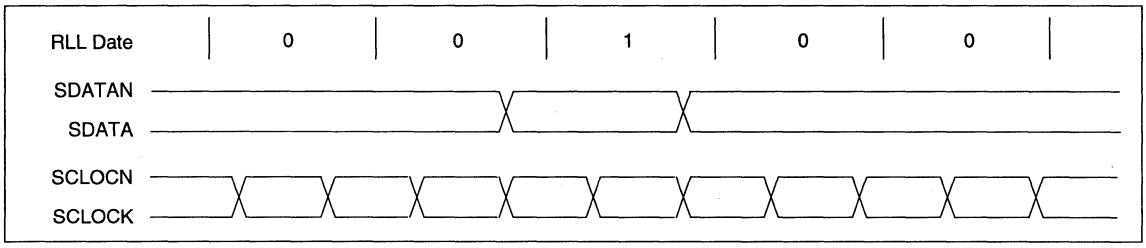


Figure 3: Synchronized Data and Clock Timing

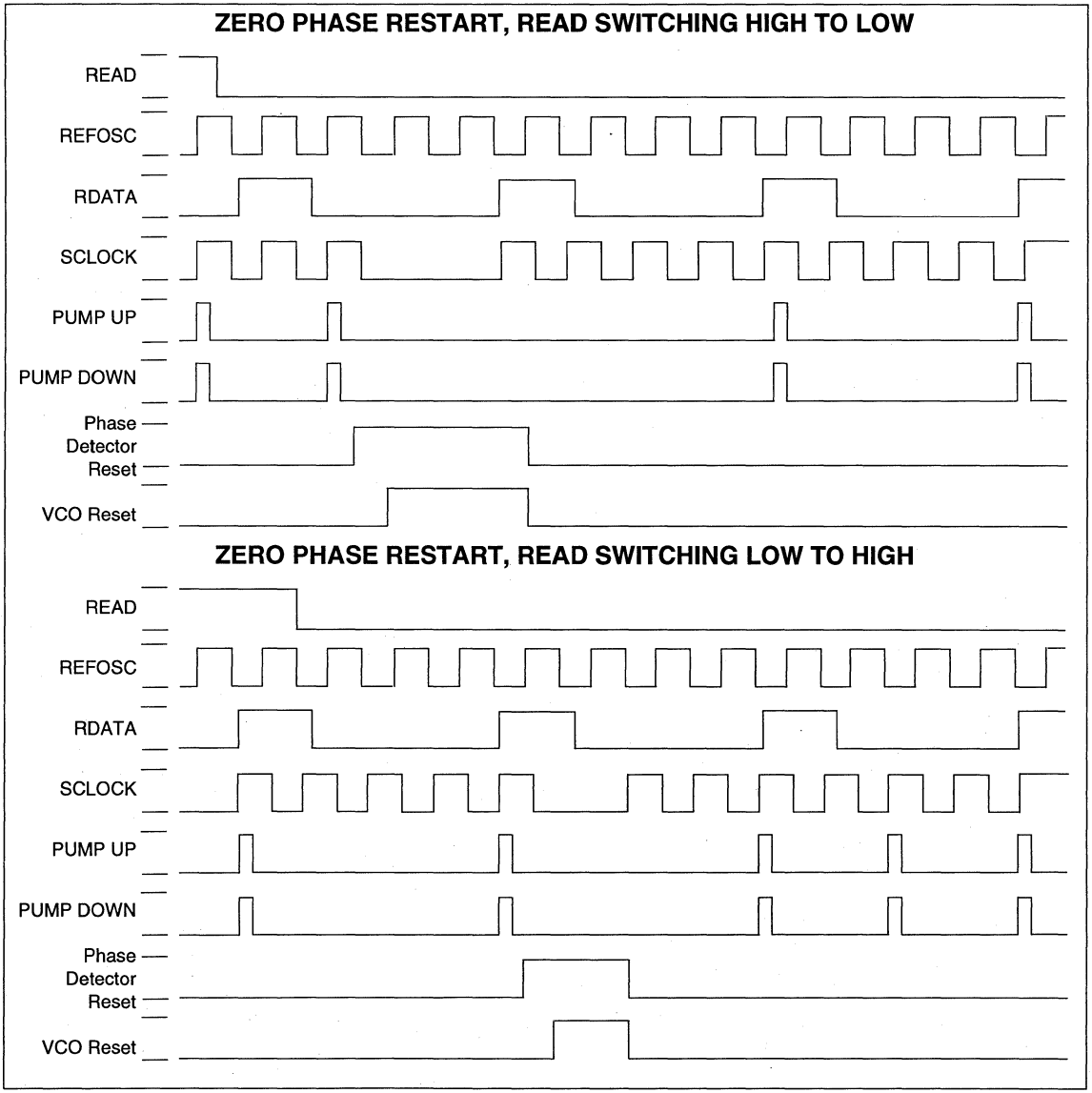
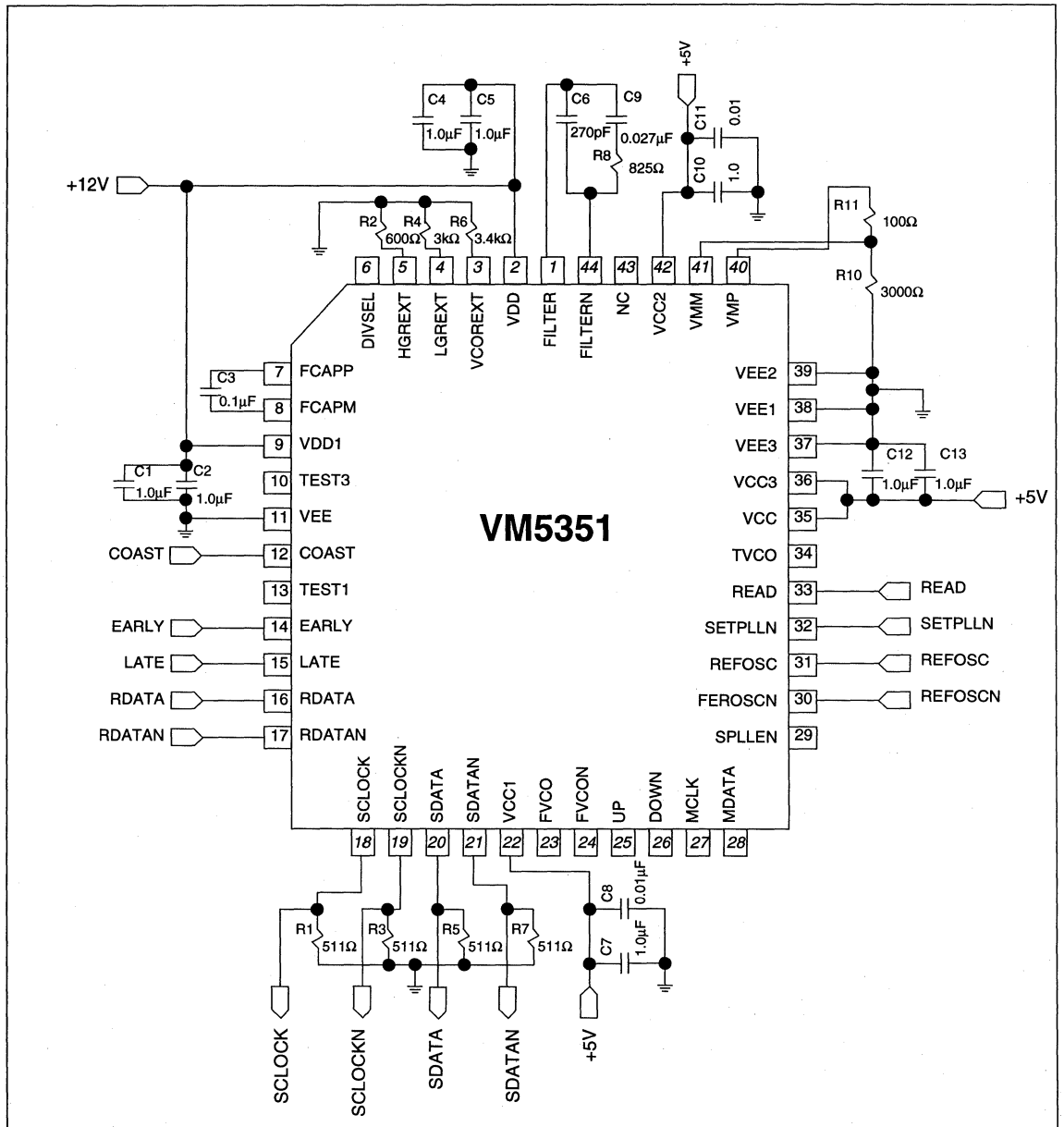
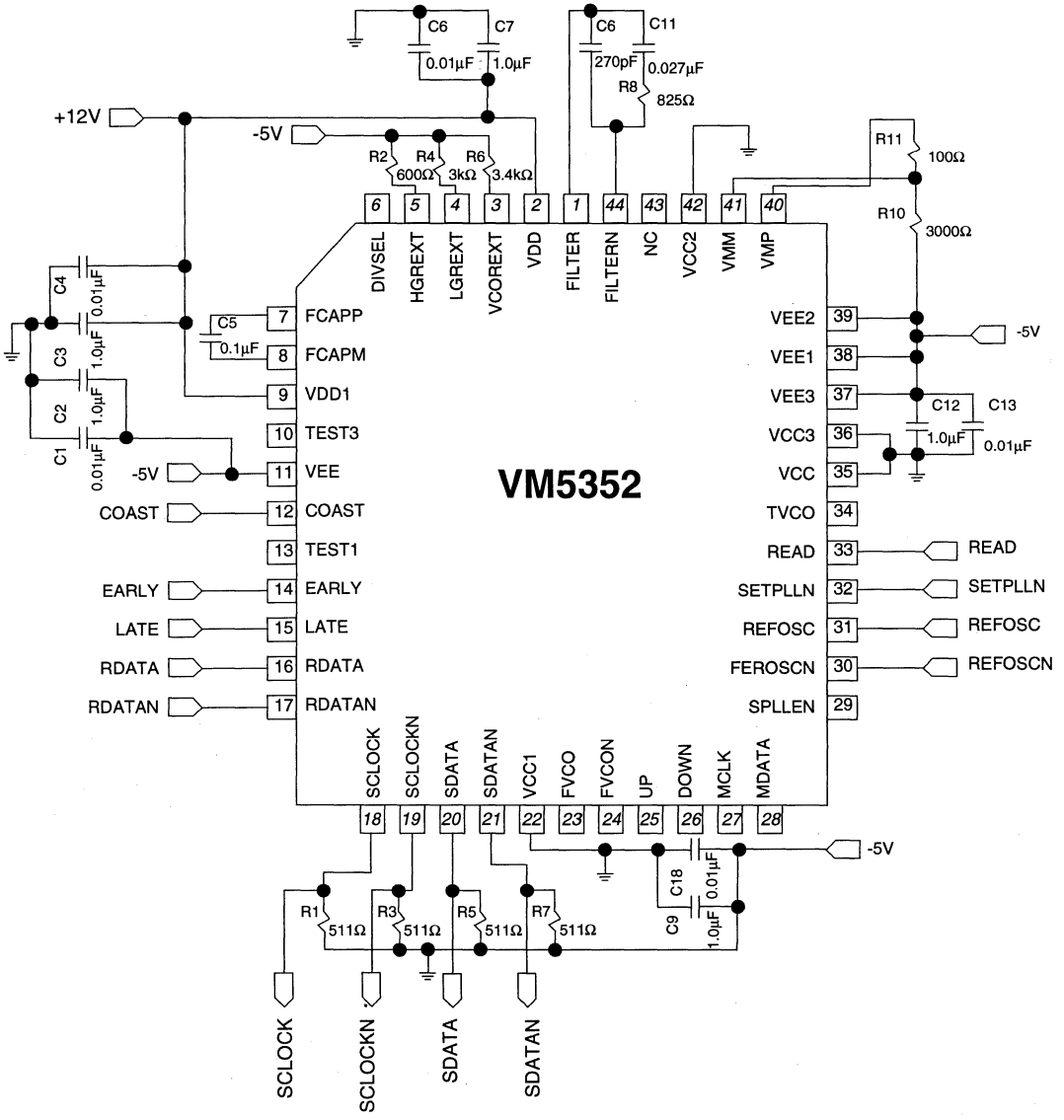


Figure 4: VCO Zero Phase Restart Timing



NOTE: This circuit is set up for 25Mbits/sec using (2,7) code. The REFOSC input frequency is a 50MHz differential ECL signal. The high and low gain charge pump currents are set to 2.0mA and 400µA, respectively. The VCO center frequency is set to 100MHz, giving a VCO gain of 10.5MHz/V.

Figure 5: VM5351 Typical Connection Diagram



NOTE: This circuit is set up for 25Mbits/sec using (2,7) code. The REFOSC input frequency is a 50MHz differential ECL signal. The high and low gian charge pump currents are set to 2.0mA and 400µA, respectively. The VCO center frequency is set to 100MHz, giving a VCO gain of 10.5MHz/V.

Figure 6: VM5352 Typical Connection Diagram

VTC Inc.
Value the Customer™

VM5401
PULSE DETECTOR/QUALIFIER

August,1994

FEATURES
- Qualifies Pulses Based on Zero-Crossing, Amplitude, Slope and Polarity.
- Erases Bad Pulses when Successive Same-Polarity Peaks Occur
- 64 Mbits/sec Transfer Rate
- 23.5 dB Input Dynamic Range (no closed loop AGC needed)
- ±5V or +5V / +12V Operation
- 750mW Typical Power Dissipation (400 mW in sleep mode)
- Externally Adjustable Amplitude Threshold Tracks Envelope of Read Signal
- On-Chip Bandgap Reference Biases External Filter/ Equalizer
- Pulse-Pairing Less Than 3% of Coded Clock Period (<333 ps @ 64 Mbits/sec)
- Designed for Use With VM5351 Data Separator
- Available in a 44-lead PLCC

DESCRIPTION
The VM5401 is fabricated on VTC's high-performance complementary bipolar process. The device is designed to operate in ±5V or +5/+12V systems. The VM5401 receives filtered analog readback signals from the read/write preamp and delivers qualified logic pulses to the read data separator. Errors due to false peaks are detected and erased after the data separator output (by the VM5401) prior to interpretation by the encoder/ decoder.

ABSOLUTE MAXIMUM RATINGS

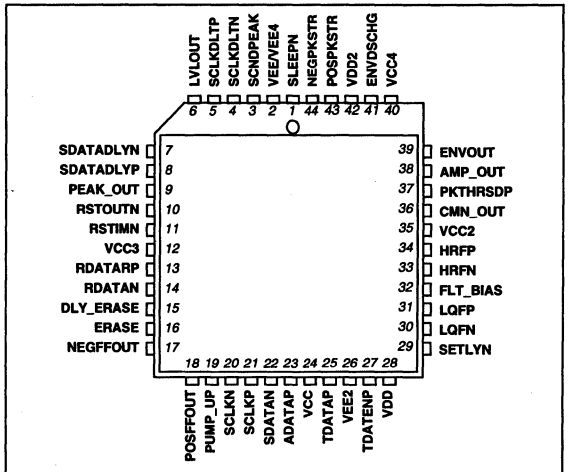
±5 Volt Supplies

V_{DD} ..... -0.5V to +7V
V_{CC} 0V
V_{EE} ..... -7V to +0.5V
Analog Input Voltage, V_{IN} ..... V_{EE}-0.5V to +0.5V
ECL Input Voltage, V_{IN} ..... V_{EE} to 0V
ECL Output Current,
I_{OUT} (cont) 25mA
I_{OUT} (surge) 50mA
Junction Temperature, T_J ..... 0°C to +150°C
Storage Temperature, T_{stg} ..... -65°C to +150°C

+5 Volt, +12 Volt Supplies

V_{DD} .....-0.5V to +13.5V
V_{CC} ..... -0.5V to +7V
V_{EE} 0V
Analog Input Voltage, V_{IN} ..... -0.5V to V_{CC} +0.5V
ECL Input Voltage, V_{IN} ..... 0V to V_{CC}
ECL Output Current,
I_{OUT} (cont) 25mA
I_{OUT} (surge) 50mA
Junction Temperature, T_J ..... 0°C to +150°C
Storage Temperature, T_{stg} ..... -65°C to +150°C

CONNECTION DIAGRAM



44-lead PLCC

RECOMMENDED OPERATING CONDITIONS

±5 Volt Supplies

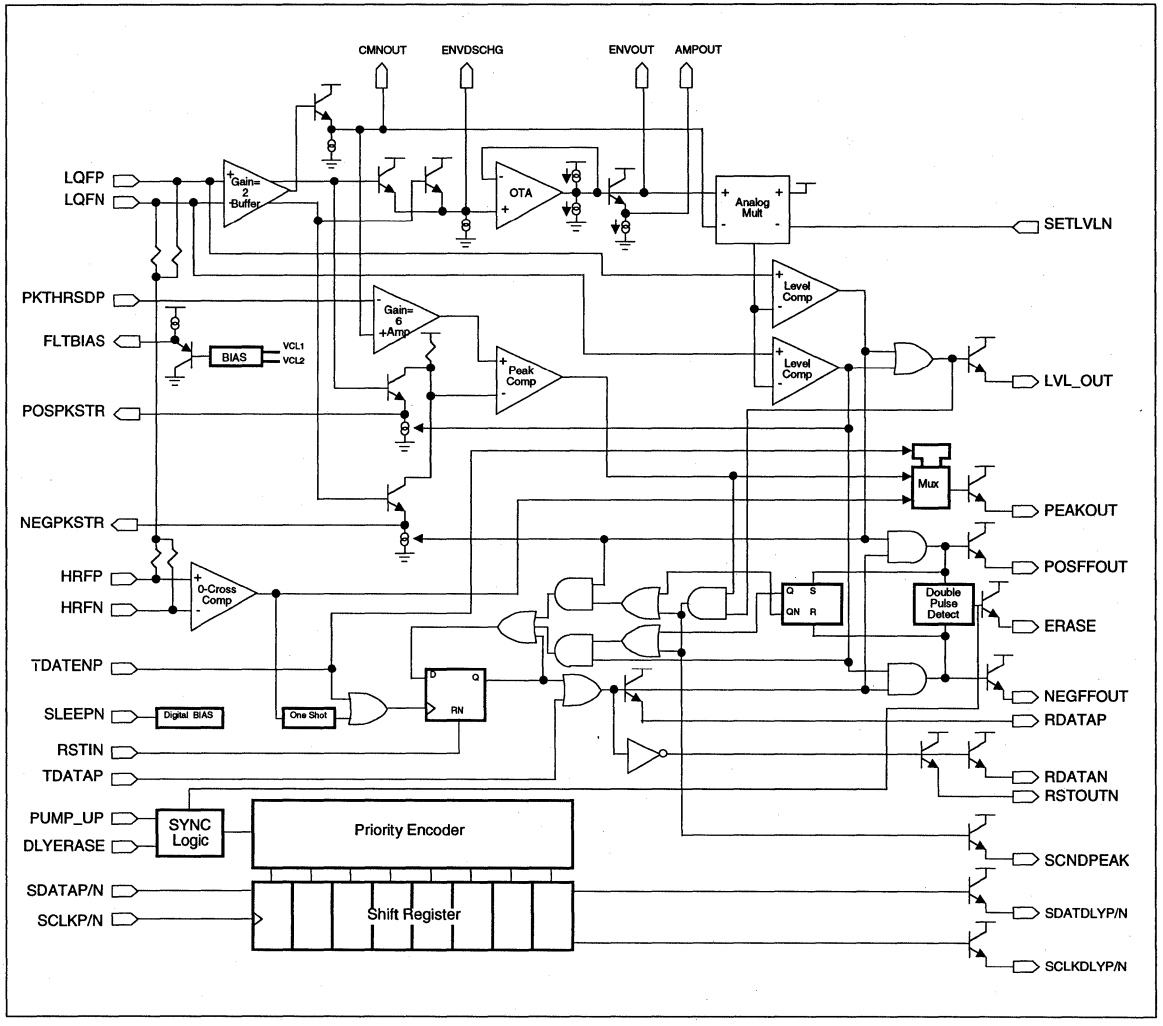
V_{DD} ..... +4.5V to +5.5V
V_{CC} 0V
V_{EE} ..... -5.5V to -4.5V
Ambient Temperature, T_A .....0°C to +70°C
Junction Temperature, T_J ..... 0°C to +100°C

+5 Volt, +12 Volt Supplies

VDD .....+10.8V to +13.2V
VCC .....+4.5V to +5.5V
VEE ..... 0°C to +100°C

DATA RECOVERY CIRCUITS

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL BLOCK DESCRIPTION

Two analog input channels are processed by the VM5401. The timing channel receives input from the high resolution (HR) channel filter, which represents a differentiated version of the readback signal. The level qualification (LQ) channel is a result of low pass filtering of the readback signal.

The high resolution signal is converted to digital pulses using a zero-crossing comparator and self-resetting pulse former logic. Thus, a pulse is produced at each zero-crossing on the HR channel. The HR pulses are qualified by signals which are derived from the LQ channel. Two comparators indicate when the positive and negative extents of the LQ signal exceed a certain percentage of the average peak amplitude of the LQ signal. In addition, two peak detectors respond to positive and negative slopes on the LQ signal and ignore subsequent lower amplitude peaks of the same polarity.

The average peak amplitude of the LQ signal is determined by an envelope follower circuit. The product of the envelope follower output and an external DC control voltage is generated by an analog multiplier circuit. Hence, a threshold is produced which is proportional to the average peak amplitude of the LQ signal.

In addition to the HR pulse former, digital logic stores the polarity of the LQ signal and qualifies consecutive peaks of the same polarity with the peak detector signals. A qualified RDATA pulse is then produced with provisions for external control of the RDATA pulse width via an RC network or delay line. Error conditions result in an ERASE pulse, which is synchronized to the SDATA pulse from the Read Data Separator (RDS), and post RDS logic erases the erroneous SDATA pulse.

The block diagram of the circuit is shown above. The following is a brief description of each cell contained in the block diagram.

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BIAS

Two bandgap reference circuits generate a 0 T.C. current, VCC1, and a 0 T.C. voltage, VCC2. VCL1 is used for envelope peak detection, where external capacitors must be charged and discharged at a rate that is relatively independent of supply voltage and temperature. VCL2, is used where precise voltage drops are required, including FLTBIAS, a voltage reference at 2V below VCC2 with source/sink capability of ±1mA. FLTBIAS is used to bias the HR and LQ filters, as well as provide the maximum end of the voltage control range of SETLVLN to establish the LQ comparator thresholds.

0-Cross COMP

This is the HR comparator. It is designed for short propagation delay, high gain, and low input offset voltage. The overall gain of this comparator is about 10,000V/V. Prop delay is about 3ns. Offset is typically 0.8mV. Internal resistors bias the comparator inputs to the FLTBIAS voltage.

Gain = 2 Buffer

This is a differential amplifier and level shifter circuit. Differential outputs and a common mode output are generated. The gain is nominally two and the bandwidth is about 60MHz. Internal resistors bias the amplifier inputs to the FLTBIAS voltage.

Envelope Follower

The differential and common mode outputs of the BUFFER are inputs to the envelope follower circuit (top center of block diagram). In the first stage a precision rectifier circuit combines the differential signals such that the most positive extent of the two signals is buffered and stored on an external capacitor on the ENVDSCHG pin. An emitter follower drives this capacitor in the positive-going direction and a 200µA current source provides a slow voltage decay. The second stage forms a unity gain feedback OTA with ±200µA output drive to the ENVOUT pin. The output of the OTA and the common mode output from the BUFFER cell are buffered by emitter followers. Short circuit protection is provided for the emitter follower on the ENVDSCHG pin.

Analog MULT

This is a four-quadrant Gilbert multiplier cell with emitter degeneration. Only two quadrants are actually used due to the single-ended threshold control pin, SETLVLN. The other input to the multiplier comes from the envelope follower. The overall gain of the multiplier is about 0.25. The output controls the qualification thresholds.

Level COMP

The LQ comparators are triggered when the LQ channel signal exceeds the threshold percentage, as set by the envelope follower and the voltage on SETLVLN. These comparators are similar to the 0-Cross COMP. The propagation delay and gain are comparable to the 0-Cross COMP.

Peak Detectors

Two identical peak detector circuits are used in the VM5401. One receives the positive output from the BUFFER, and the other receives the negative output. At the core of each peak detector is an emitter follower that drives an external capacitor. A resistor in the collector circuit produces a voltage drop that is proportional to the charging current in the capacitor. When the input signal falls, the base-emitter junction of the emitter follower transistor tends to cut off, leaving a charge on the capacitor that represents a peak in the signal. The voltage on the capacitor remains essentially constant until either the capacitor is discharged or the signal exceeds this peak value. Discharge of the capacitor is controlled by the level comparator. The discharge current is nominally 6mA.

Gain = 6 AMP

This cell sets the threshold for peak detection. The voltage gain of the circuit is approximately six, and is linear from a differential voltage of 0 volts to about 1.5 volts. To generate a peak threshold that is proportional to input amplitude, PKTHRSDP should be connected to a resistor divider driven by AMPOUT and CMNOUT (see typical application).

Peak COMP

This is the peak detector comparator/level shifter. It triggers when the peak detector output drops below the threshold.

LOGIC

The heart of the VM5401 logic is the D-flip flop that is clocked by a one shot driven by the HR zero-cross comparator. the output of this flip flop is the Read Data (RDATA) pulse that goes to the Read Data Separator. The D-input is qualified by the level qual signals and the last polarity information.

To produce an RDATA pulse, one of the following two conditions must occur.

1. A zero-crossing on the HR input and an LQ input that exceeds the level threshold and the previous RDATA was derived from the opposite LQ polarity.
2. A zero-crossing on the HR input and an LQ input that exceeds the level threshold and a second peak on the LQ input of the same polarity but with greater amplitude.

POSFFOUT and NEGFFOUT are formed by gating RDATA with the LQ channel polarity. Then two POSFFOUTs or NEGFFOUTs in a row occur the DOUBLE PULSE DETECT block generates an ERASE pulse. This pulse is used to delete a synchronized data pulse from the erase shift register.

The width of the RDATA pulse is controlled by the delay from RSTOUTN to RSTIN. This delay can be implemented using an RC network as shown in the typical application schematic. PEAKOUT, LVL_OUT and SCNDPEAK are test signals.

PEAKOUT reflects the signal out of either the HR comparator or the peak detector comparator, depending on the state of TDATENP.

TDATENP	*PEAKOUT*
0	Peak Detector
1	HR Comparator

The two LQ comparator outputs are OR'ed to produce LVLOUT. SCNDPEAK comes from the qualified peak detect signal and will pulse to a logic "1" only when two peaks of the same polarity occur.

PIN DESCRIPTIONS

LQFP, LQFN: Differential input signal from the level qualification filter.

HRFP, HRFN: Differential input signal from the high resolution filter.

POSPKSTR: Analog pin for storing the positive peak value from the peak detector. Capacitor, C_{EXT}, should be connected to this pin.

$$C_{EXT} \approx 600pF - \left(\frac{18pF}{MHz}\right)f, \qquad \textit{(eq. 1)}$$

f = LQF_{MAX} frequency (MHz)

NEGPKSTR: Analog pin for storing the positive peak value from the peak detector. A capacitor, with the same value as C_{EXT}, should be connected to this pin.

PKTHRSDP: Analog input pin for setting peak detector comparator threshold.

$$\%THRESHOLD = \frac{3}{5\pi fC} \bullet k \quad (0 < k < 1) \qquad \textit{(eq. 2)}$$

F = LQF_{MAX} frequency (MHz)
C = C_{EXT} (Farads)
k = the fraction of (AMPOUT - CMNOUT) fed into pkTHRSDP

ENVOUT: Analog output pin from the envelope follower. A capacitor on this pin controls the charge rate.

$$C_{EFC} = \frac{200\mu A}{dv/dt} \qquad \textit{(eq. 3)}$$

ENVDSCHG: Analog output pin from the envelope follower. A capacitor on this pin controls the discharge rate.

$$C_{EFD} = \frac{200\mu A}{dv/dt} \qquad \textit{(eq. 4)}$$

FLT_BIAS: Analog output pin which supplies VCC-2V level to bias external filters.

CMN_OUT: Analog output pin for use as common mode reference with AMP_OUT to set the PKTHRSDP level.

SETLVLN: Analog input pin used to set % of threshold for level qualification comparators.

0% level @ V_{CC}
32% level @ V_{CC} - 1V
64% level @ V_{CC} - 2V
} % thr = (VCC - SETLVLN) * 32

AMP_OUT: Analog output pin (buffered version of ENVOUT) for use with CMN_OUT to set PKTHRSDP level.

SDATAP, SDATAN: Differential ECL input pins with synchronized serial data from Read Data Separator.

SCLKP, SCLKN: Differential ECL input pins with serial data clock from Read Data Separator.

DLYERASE: Single-ended ECL input which is connected to ERASE through a delay line.

RSTINN: Single-ended ECL input used to control the RDATA pulse width. Should be delayed from RSTOUTN.

$$\text{RDATA Pulse Width} \cong \frac{\tau}{3} + 5ns \qquad \textit{(eq. 5)}$$

where $\tau = R_L \bullet C_R$

TDATAP: Single-ended ECL input used only in system test to supply pulses to the Read Data Separator.

TDATENP: Single-ended ECL input which disables HR comparator during system test. A logic "1" disables. Also selects HR comparator or peak detect output to PEAK_OUT.

PUMP_UP: Single-ended ECL input from the read data separator used to synchronize ERASE logic. When used, ERASE and DLYERASE are left open.

SLEEPN: Single-ended TTL input which powers down the digital logic when at a logic "0". Floats high.

RDATAP, RDATAN: Differential ECL output of detected data pulse to Read Data Separator.

SDATDLYP, SDATDLYN: Differential ECL output of corrected serial data for Endec.

SCLKDLYP, SCLKDLYN: Differential ECL output derived from SCLK. Synchronous with SDATDLY.

RSTOUTN: Single-ended ECL output used to control the RDATA pulse width. Should be delayed to RSTINN.

$$\text{RDATA Pulse Width} \cong \frac{\tau}{3} + 5ns \qquad \textit{(eq. 6)}$$

where $\tau = R_L \bullet C_R$

ERASE: Single-ended ECL output which drives a delay line to DLYERASE. Matches RDS delay. When used, PUMP_UP is left open.

LVL_OUT: Single-ended ECL output which represents to logical OR of the two LQ comparators.

PEAK_OUT: Single-ended ECL output which represents the peak detector output or HR comparator, depending on TDATENP.

POSFFOUT: Single-ended ECL output from the positive level flip flop.

NEGFFOUT: Single-ended ECL output from the negative level flip flop.

SCNDPEAK: Single-ended ECL output which is the clock input to the second peak flip flop.

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POWER PINS

PIN NAME	*±5V*	*+5V/+12V*
VCC	Digital 0V	Digital +5V
VCC2	Analog 0V	Analog +5V
VCC3	ECL Output 0V	PECL Output +5V
VCC4	Noisy Analog 0V	Noisy Analog +5V
VEE	Digital -5V	Digital 0V
VEE2	Analog -5V	Analog 0V
VDD	Analog +5V	Analog +12V
VDD2	Noisy Analog +5V	Noisy Analog +12V

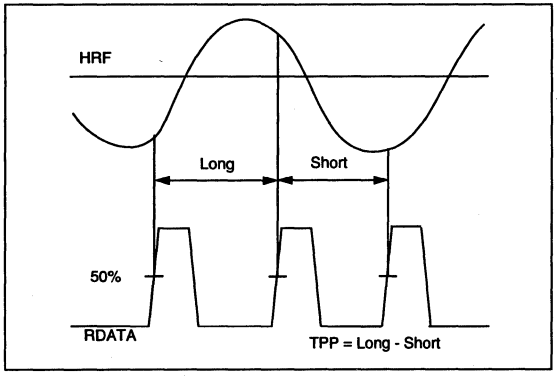

Figure 1: Pulse Pairing

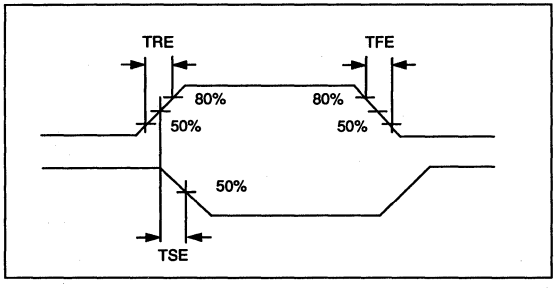

Figure 2: Output Rise/Fall Time and Differential Skew

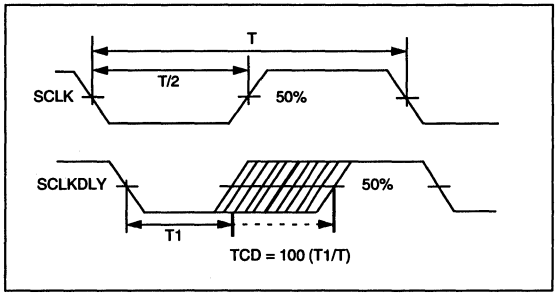

Figure 3: Clock Output Duty Cycle

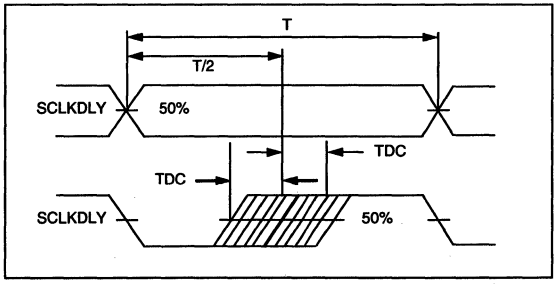

Figure 4: SDATDLY to SCLKDLY Skew

DC CHARACTERISTICS Unless otherwise specified, ±5V recommended operating conditions apply.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current	I_{DD}	See default test schematic	10	20	30	mA
Negative Supply Current	I_{EE}	See default test schematic	60	110	320	mA
Input High Current	I_{IH}	ECL			250	µA
Input Low Current	I_{IL}	ECL	0.5		250	µA
Input High Current	I_{TH}	TTL			80	µA
Input Low Current	I_{TL}	TTL			1.6	mA
Output High Voltage	V_{OH}	ECL, 100Ω to -2V	-1.02		-0.66	V
Output Low Voltage	V_{OL}	ECL, 100Ω to -2V	-1.95		-1.63	V
Input High Voltage	V_{IH}	Single-ended ECL inputs	-1.13		-0.73	V
Input Low Voltage	V_{IL}	Single-ended ECL inputs	-1.95		-1.45	V
Input High Voltage	V_{TH}	TTL, relative to VEE	2			V
Input Low Voltage	V_{TL}	TTL, relative to VEE			0.8	V
Common Mode Input Voltage	V_{CM}	ECL, Differential ECL inputs	-2.50		-0.30	V
Differential Input Voltage	V_{DI}	ECL, Differential ECL inputs	200		1220	mV
FLT_BIAS Output Voltage	V_{FB}	±1mA output current	-2.15	-2	-1.85	V
CMN_OUT Output Voltage	V_{CN}	±0.3mA output current	-2.75	-2.55	-2.3	V
AMP_OUT Output Voltage	V_{AM}	±0.3mA output current	ENVOUT -1.25		ENVOUT -0.75	V
LQFP,N Input Resistance	R_{LQ}	Single-ended to FLT_BIAS	3	6	9	kΩ
HRFP,N Input Resistance	R_{HR}	Single-ended to FLT_BIAS	3	6	9	kΩ
Envelope Follower Offset	T_{EO}	LQFP-VFB bs LQFN - VFB @ 0.75V		3		%
ENVOUT Source Current	I_{EH}	ENVOUT at -2.2V	150	200	250	µA
ENVOUT Sink Current	I_{EL}	ENVOUT = 0V	150	200	250	µA
ENVDSCHG Source Current	I_{DH}	LQFP, N = VFB; -2< ENVDSCHG < 1.7V	1.6			mA
ENVDSCHG Sink Current	I_{DL}	ENVDSCHG = 0V	150	200	250	µA
Envelope Follower Current Ratio Tracking	T_{EI}	IDL, IEH, IDL (all three) IEH IEL IEL	0.65	1	1.35	mA
HR Comparator DC Gain	A_{HR}		2000	4000		V/V
LQ Comparator DC Gain	A_{LQ}		2000	4000		V/V
POSPKSTR to CMN_OUT Amplitude Tracking	T_{PC}	1.5mA from POSPKSTR to VEE; 50mV < LQFP - VFB < 750mV			10	%
NEGPKSTR to CMN_OUT Amplitude Tracking	T_{NC}	1.5mA from POSPKSTR to VEE; 50mV < LQFN - VFB < 750mV			10	%
TPC to TNC Tracking	T_{PN}	2 • (TPC - TNC) / (TPC + TNC)			5	%
POSPKSTR Leakage Current	I_{PL}	ENVOUT = CMN_OUT + 1.25V; SETLVLN = VFB; POSPKSTR = 1.5V	-1		1	µA
NEGPKSTR Leakage Current	I_{NL}	ENVOUT = CMN_OUT + 1.25V; SETLVLN = VFB; NEGPKSTR = 1.5V	-1		1	µA
POSPKSTR Discharge Current	I_{PD}	POSPKSTR = -1.0V; SETLVLH = 0V; LQFN - VFB = 0.75V; ENVOUT = -1.5V	4		12	mA

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DC CHARACTERISTICS (Continued) Unless otherwise specified, ±5V recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Envelope Follower Current Ratio Tracking	T_{EI}	$\frac{IDL}{IEH}, \frac{IEH}{IEL}, \frac{IDL}{IEL}$ (all three)	0.65	1	1.35	mA
HR Comparator DC Gain	A_{HR}		2000	4000		V/V
LQ Comparator DC Gain	A_{LQ}		2000	4000		V/V
POSPKSTR to CMN_OUT Amplitude Tracking	T_{PC}	1.5mA from POSPKSTR to VEE; 50mV < LQFP - VFB < 750mV			10	%
NEGPKSTR to CMN_OUT Amplitude Tracking	T_{NC}	1.5mA from POSPKSTR to VEE; 50mV < LQFN - VFB < 750mV			10	%
TPC to TNC Tracking	T_{PN}	2 • (TPC - TNC) / (TPC + TNC)			5	%
POSPKSTR Leakage Current	I_{PL}	ENVOUT = CMN_OUT + 1.25V; SETLVLN = VFB; POSPKSTR = 1.5V	-1		1	µA
NEGPKSTR Leakage Current	I_{NL}	ENVOUT = CMN_OUT + 1.25V; SETLVLN = VFB; NEGPKSTR = 1.5V	-1		1	µA
POSPKSTR Discharge Current	I_{PD}	POSPKSTR = -1.0V; SETLVLH = 0V; LQFN - VFB = 0.75V; ENVOUT = -1.5V	4		12	mA
NEGPKSTR Discharge Current	I_{ND}	NEGPKSTR = -1.0V; SETLVLH = 0V; LQFN - VFB = 0.75V; ENVOUT = -1.5V	4		12	mA

AC CHARACTERISTICS Unless otherwise specified, ±5V recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
HRFP,N Dynamic Range	V_{HD}	Differential peak-to-peak	0.2	1	3	V
LQFP,N Dynamic Range	V_{LD}	Differential peak-to-peak	0.2	1	3	V
HRFP,N Frequency Range	F_{HR}		1.4		22.5	MHz
LQFP,N Frequency Range	F_{LQ}		1.4		22.5	MHz
HRFP,N Common Mode Range	V_{HC}		-2.3	-2	-1.75	V
LQFP,N Common Mode Range	V_{LC}		-2.3	-2	-1.75	V
HR Comparator Input Offset Voltage	V_{HO}	300Ω from HRFP,N to FLT_BIAS			0.8	mV
LQ Comparator Input Offset Voltage	V_{LO}	300Ω from LQFP,N to FLT_BIAS			2	mV
HR Comparator Input Offset Voltage Drift	V_{HT}	300Ω from HRFP,N to FLT_BIAS			10	µV/C
LQ Comparator Input Offset Voltage Drift	V_{LT}	300Ω from LQFP,N to FLT_BIAS			10	µV/C
HRFP,N Input Capacitance	C_{HR}	F_{HR} = 5MHz		8	12	pF
LQFP,N Input Capacitance	C_{LQ}	F_{LQ} = 5MHz		8	12	pF
AMP_OUT-CMN_OUT Linearity	T_{AC}	Over F_{LQ} and V_{LD} range			5	%
HR Pulse Pairing Error	T_{PP}	See Figure1; FHR from 1.5 to 5MHz; VHD = 200mV sine wave			0.03/16 FHR	s
SETLVLN Adjust Accuracy	T_{SA}	% Threshold = SETLVLN/3	-15		15	%
SETLVLN Adjust Range	T_{SR}	SETLVLN from 0V to -2.2V	0		110	%
Peak Detect Threshold Adjust Accuracy	T_{PT}	I_{IN}/V_{IN} = 0.012; where I_{IN} is from POSPKSTR (NEGPKSTR) to V_{EE}, and V_{IN} is PKTHRSDP-CMN_OUT, with LQFP (LQFN) = -1.5V and LQFN (LQFP) = -2V			40	%
Peak Detect Sensitivity	V_{PS}	LQFP,N at FLQmax	200			mV
ECL Output Rise Time	T_{RE}	20 to 80%; R_L = 100Ω, C_L < 10pF; see Figure 2	0		2	ns
ECL Output Fall Time	T_{FE}	20 to 80%; R_L = 100Ω, C_L < 10pF; see Figure 2	0		2	ns
Skew on Differential ECL Outputs	T_{SE}	See Figure 2			0.3	ns
SCLKDLY Output Duty Cycle	T_{CD}	See Figure 3	47	50	53	%
SDATDLY to SCLKDLY Skew	T_{DC}	See Figure 4			1	ns
SCLK Frequency	F_{SC}				90	MHz

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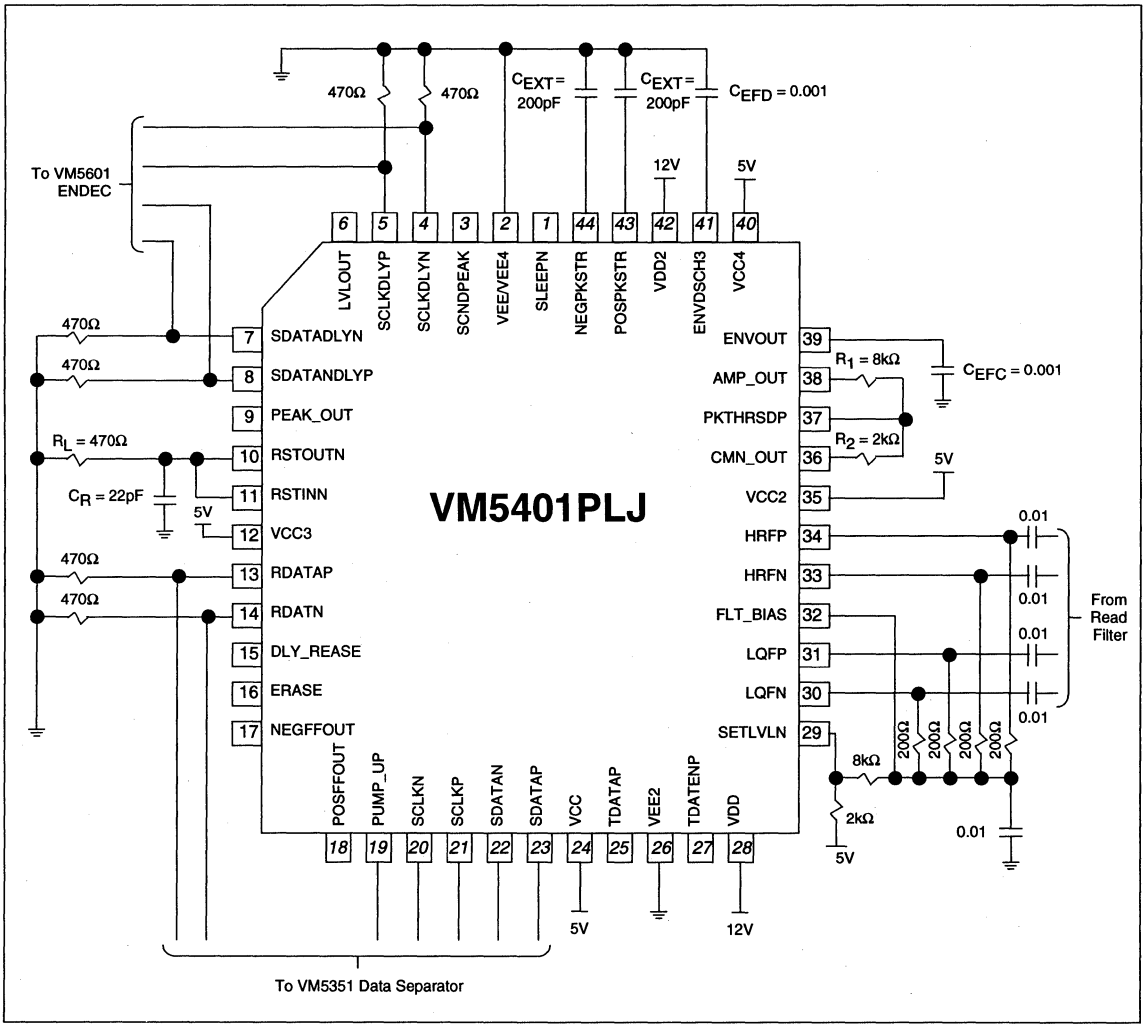


Figure 5: VM5401 Typical Connection Diagram

VTC Inc.
Value the Customer™

VM54100

COMPLETE 100 MBITS/SEC PEAK-DETECTION READ CHANNEL

ADVANCE INFORMATION August,1994

FEATURES

- Compatible with 100 MBits/sec NRZ Data Rate Operation
- Dual Mode VGA Supports AGC and PGC Modes
- Low Z and Fast AGC Modes for Quick Write Recovery
- Programmable Filter with Pulse Slimming
- Multiplexed Filter Tuning Supports Servo and Data Fields
- Demodulation of Servo Bursts
- Low Power (Standby) Mode Along with a Very Low Power (Sleep) Mode

DESCRIPTION

The VM54100 is a PolarMOS2 integrated circuit that provides all of the data processing for detection and qualification of read signals from a head preamplifier. This device can handle NRZ data rates of 100Mbits/sec. This device along with its companion chip, the VM53100 comprises a complete 100Mbits/sec read channel.

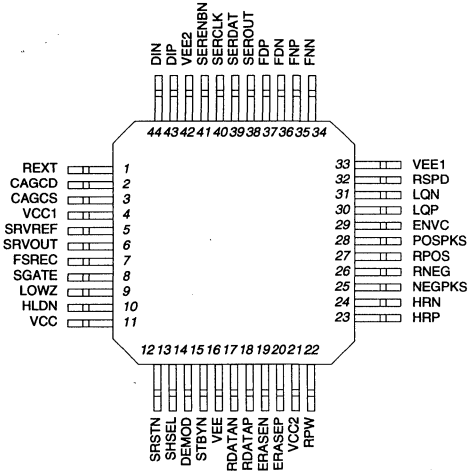
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
V_{CC} ..... -0.3V to 7.0V
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to V_{CC} +0.3V
Analog Input Voltage V_{IN} ..... -0.3V to V_{CC} +0.3V
Junction Temperature T_J ..... 150°C
Storage Temperature T_{stg} ..... -65° to 150°C
Thermal Impedance Θ_{JA};
44-lead PQFP ..... 60°C/W

RECOMENDED OPERATING CONDITIONS

Supply Voltage:
V_{CC} .....+5V ±10%
Junction Temperature ..... 0° to 125°C

CONNECTION DIAGRAM



44-lead PQFP

DATA RECOVERY CIRCUITS

Functional Description

The VM54100 consists of a variable gain amplifier (VGA) with an automatic gain control circuit. The automatic gain control (AGC) circuit can be disabled, which allows the VGA to be operated in programmable gain control (PGC) mode.

A seven pole linear phase 0.05 degree equiripple low pass filter (LPF) with pulse slimming is included in the VM54100. Normal and differentiated outputs from the filter are provided with matched delays.

The filter provides for programmable unboosted cutoff frequencies from 4.68MHz to 37.5MHz. Likewise, the pulse slimming is programmable from 0dB to 13dB.

A pulse detector and qualifier is provided which includes an envelope detector, adjustable dV/dt sensitivity, programmable threshold and independent qualification of negative and positive threshold to suppress error propagation.

A peak detecting servo demodulator with an array of sample and hold amplifiers provides for the demodulation of up to four servo fields.

A low power mode is available through the use of the STBYN pin. In standby mode (STBYN = 0) the VGA, sections of the filter, the PDQ, and the demodulator sections are powered down.

The majority of the chip functionality is controlled via a serial digital interface

Gain Control (GC)

The Gain Control section of the VM54100 consists of a wide band variable gain amplifier (VGA) with a charge pump, amplitude detector, and exponentiator. The Gain Control has two modes: Automatic (AGC), and Programmable (PGC) gain control. The mode of the Gain Control is controlled by the PGC control bit (Addr = 1001,bit = 7).

The read back signal is externally AC coupled into the VGA amplifier on the DIP/DIN pins (see Diagram 1). The signal is amplified by the VGA and equalized by the 0.05° equiripple low pass filter. The normal output of the filter, FNP/FNN, is externally AC coupled back into the LQP/LQN inputs where it is amplitude detected by the AGC loop and locked to $1.0V_{ppd}$. With a nominal filter gain of 1 volts/volt, the VGA provides a $1.0V_{ppd}$ signal to the filter for inputs ranging from 24 to 320 mV_{ppd} on the DIP/DIN pins. A test mode is provided (test mode 5) in which the filter is completely bypassed, and the VGA outputs DOP/DON and filter inputs FIP/FIN are multiplexed to the FNP/FNN and FDP/FDN chip outputs respectively.

When in the AGC mode PGC bit is "0", the gain of the VGA is controlled by an amplitude detector, charge pump, exponentiator, and CAGCx capacitor, either CAGCD or CAGCS. The amplitude detector determines if the signal level (V_{LQ}) at the LQP/LQN inputs is above or below the target amplitude of $1.0V_{ppd}$. If the amplitude is below $1.0V_{ppd}$, the normal charging current (I_{QCN}) charges the CAGCx capacitor to increase the gain of the VGA. If the amplitude is greater than $1.0V_{ppd}$ but below $1.25V_{ppd}$, the normal discharging current (I_{QDN}) discharges the CAGCx capacitor to reduce the gain of the VGA. And if the amplitude exceeds $1.25V_{ppd}$, a fast discharging current (I_{QDF}) that is 7X the normal discharging current, quickly discharges the CAGCx capacitor until the signal level is back below $1.25V_{ppd}$. The magnitude of the normal discharging current (I_{QDN}) is set by an external resistor connected between the REXT pin and ground and is given by the following equation

$$I_{QDN} = \frac{1.2V}{REXT} \qquad \textit{(eq. 1)}$$

where REXT should set to 4.8kΩ. **This value should not be altered to adjust the loop response** because this current is also used as a reference to the DAC's. Adjust the loop responses by altering the AGC caps discussed below. The normal discharging current is 40X the normal charging current, resulting in an asymmetrical loop response.

A fast recovery from small input signals is provided with a '0'-to-'1' transition on the FSREC input. A fast charging current (I_{QCF}) that is 7X the normal discharging current quickly charges the CAGCx capacitor until the $1.0V_{ppd}$ signal level is reached, after which the loop resumes normal operation.

There are two AGC capacitors, the CAGCD pin capacitor which is used for the data field when SGATE = 0, and the CAGCS pin capacitor which is used for the servo field when SGATE = 1. This allows the data and servo fields to have independent discharging and charging rates. It also avoids reacquisition of gain at the beginning of the servo and data fields. When HLDN = 0 the discharging and charging currents are disabled, and the AGC action is halted to allow for servo burst measurement.

In the AGC mode, the VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. Equation (2) expresses the VGA normal mode gain (A_V), in volts/volts, as an exponential function of the control voltage on the selected CAGCx pin.

$$A_V = A_{V(max)} \bullet e^{-\left(\frac{2.8V - V_{CAGCX}}{0.53V}\right)} \qquad \textit{(eq. 2)}$$

where $A_{V(max)}$ is 56 volts/volt and V_{CAGCx} nominally ranges from1.4V to 2.8V.

When in the PGC mode (Addr = 1001, bit7 = "1"), the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by the "VGA Gain" DAC. The control word for the DAC is read from the Data VGA Gain register (Addr = 1011, bits[4:0]) when SGATE = 0 otherwise its read for Servo VGA GAIN register (Addr = 1100, bits[4:0]). In PGC mode, the VGA has a linear gain versus binary control word characteristic to insure predictable controlled input response. Equation (3) expresses the VGA gain as a linear function of the control word.

$$A_V = 4 + \frac{46}{31} \times N \qquad \textit{(eq. 3)}$$

where N ranges between 0 and 31decimal or 00000 to 11111 binary (bit 4 is the MSB).

For fast write to read recovery a low input impedance mode is provided. When LOWZ = 1, the gain of the VGA goes to zero, the input impedance is reduced to $1/60^{th}$ of its normal value, and the charge pump currents are disabled to retain the gain values set by the CAGCx capacitors. Also, a low impedance is initiated for the on-chip AC coupling capacitors between the VGA output and the filter input. Upon releasing the LOWZ mode, the on-chip

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coupling capacitors are held in the low impedance mode for an extra 200ns while the VGA restores its gain. This eliminates any transient offset effects that may occur while the loop is locking.

While the VM54100 is idle (STBYN = 0) or in SLEEP mode (Addr = 1000, bit7 = "0"), the VGA amplifier is powered down.

Programmable Low Pass Filter (LPF) / Equalizer

The filter is implemented as a 7-pole 0.05 degree linear phase equiripple low pass filter with matched normal and differential outputs. The cutoff frequency and boost equalization are programmable.

The basic building block for the filter is the integrator (g_m-C) stage which consists of a transconductance amplifier driving on-chip capacitors. Figure 2 shows how g_m-C stages are connected to form a bi-quad, which realizes a second-order transfer function. The equation below is the expression for the transfer function of such a bi-quad. In Diagram 3, three of these bi-quads and a single g_m-C stage are cascaded to form a seven-pole low pass filter. In parallel with the final g_m-C stage is a nearly identical single g_m-C stage configured as a high-pass, or differentiator section. The various sections supply normal or differentiated low-pass outputs with matched group delays. The normal output goes to the AGC and servo sections. The differentiated output, along with the normal output, is used by the PDQ block to provide data and servo peak position information. Because the high-pass differentiator stage tracks the other g_m-C stages, the relative gain AO_D of the differentiated output to the normal output is nearly constant (at two-thirds the unboosted cutoff frequency) over the range of the cutoff frequency and boost level of the filter, as depicted in Graph 1.

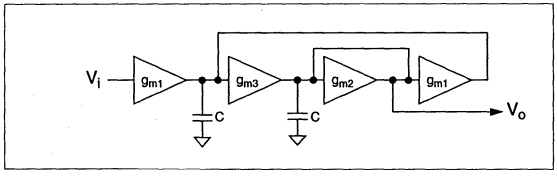


Figure 2: State-Variable Biquad

$$\frac{V_o}{V_i} = \frac{\omega_o^2}{s^2 + s(\omega_o/Q_o) + \omega_o^2} \qquad \textit{(eq. 4)}$$

where $\omega_o = \frac{\sqrt{g_{m1} \cdot g_{m2}}}{C}$ and $Q_o = \frac{\sqrt{g_{m1} \cdot g_{m3}}}{g_{m2}}$

The filter utilizes transconductor-capacitor (g_m-C) techniques to provide a cutoff frequency (f_C) that is directly proportional to g_m/C. An accurate g_m is derived from the Frequency Cutoff (Fc) DAC input current and an on-chip bandgap voltage using a feedback circuit. The parts are trimmed during wafer probe to compensate for on-chip capacitance variations.

Cutoff frequency is controlled by the "Frequency Cutoff" DAC. The control word for the DAC is read from the Data Frequency Cutoff register (Addr = 1000, bits[6:0]) when SGATE=0 otherwise its read from the Servo Frequency Cutoff register (Addr = 1001, bits[6:0]). Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation

$$f_c = (0.256 \times N) + 4.68 \qquad \textit{(eq. 5)}$$

where N ranges between 0 and 127decimal or 0000000 to 1111111 binary (bit 6 is the MSB).

The gain (g_m) of each g_m-C stage is established using MOSFET input devices. These devices are operated in the triode region, resulting in a transconductance of:

$$g_m \approx \mu \bullet C_{ox} \bullet \frac{W}{L} \bullet V_{ds} \qquad \textit{(eq. 6)}$$

where μ is the MOSFET channel mobility, C_{ox} is the MOSFET gate oxide capacitance per unit area, W and L are the MOSFET channel width and length respectively, and V_{ds} is the MOSFET drain-to-source voltage. The magnitude of the g_m of each stage is set to the desired cutoff frequency by adjusting V_{ds}. Stage-to-stage g_m ratios determine the shape of the filter transfer function and are achieved by rationing the MOSFET widths (W).

The filter gm reference is generated using an external resistor on the REXT pin and on-chip bandgap references.

The amount of boost equalization depends on the output of the BOOST DAC. Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function. Graph 1 shows normalized filter response curves with maximum boost for both the normal and differentiated outputs. Graph 2 shows the nominal relationship between the BOOST control word and the resulting boost level. Notice the absence of boost when BOOST is below 4. In this region the bandwidth is being pushed out but the gain doesn't peak above the DC level.

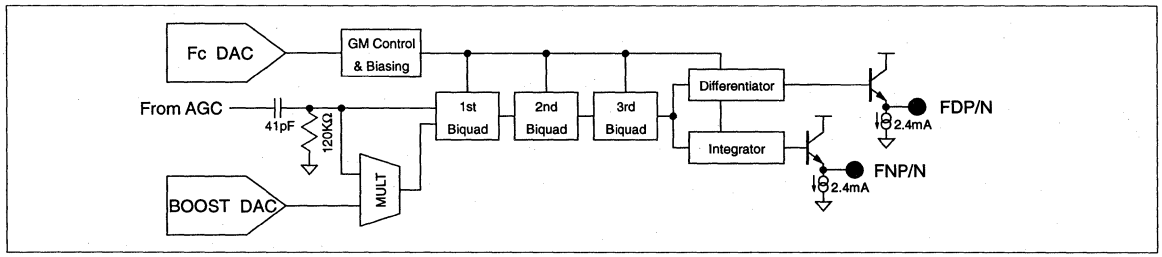
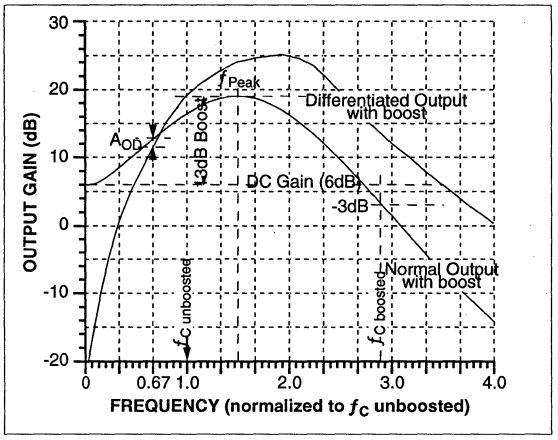
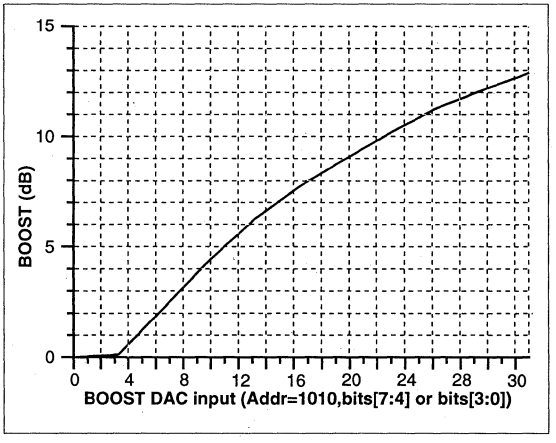


Figure 1: Filter Block Diagram



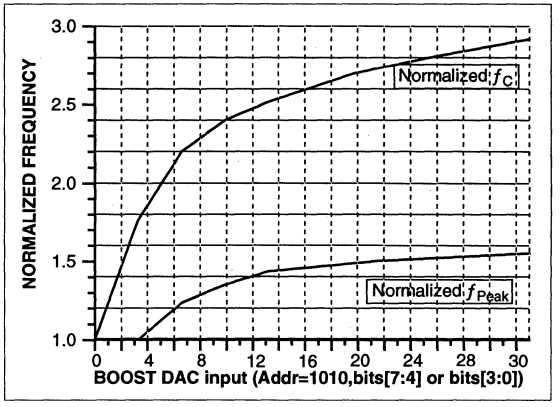
Graph 1: Normal and Differentiated Output Gains

Graph 3 shows the effect of boost on the cutoff frequency. With maximum boost the cutoff frequency is nearly triple the unboosted value. Also shown is gain peak frequency, which for maximum boost achieves a value of over 1.5. Thus, as an example, if the unboosted cutoff frequency is programmed to 30MHz, with maximum boost the peak gain of 13dB will occur at approximately 46MHz, and the net cutoff frequency will be 88MHz.



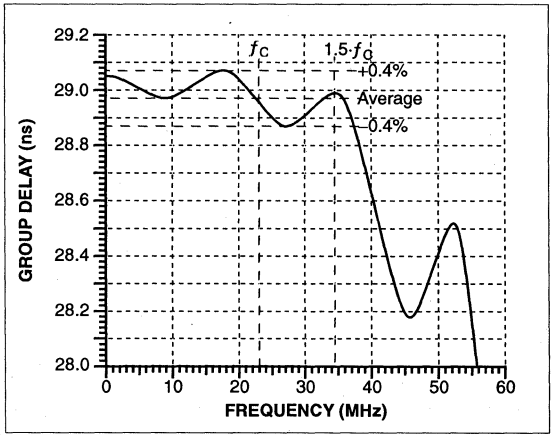
Graph 2: Ideal Boost (in dB) versus BOOST DAC input

Boost, or pulse slimming, is implemented by feeding the filter input through a variable gain stage to the normally grounded terminals of the capacitors in the first bi-quad. This yields a pair of programmable symmetric zeros on the real axis. Because the resulting transfer function has an added $K \cdot s^2$ in the numerator, the group delay is unaffected by the amount of boost.



Graph 3: Normalized f_C and f_{Peak} versus BOOST DAC input

Group delay for an ideal 0.05 degree equiripple filter is flat within 1% out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a "real" filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM54100 group delay flatness is specified to be less then ±2% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 24ns at a cutoff of 30MHz. Thus at this cutoff frequency, the group delay varies by less than±0.5ns out to 45MHz. A typical group delay is shown in Graph 4 with measurements displayed.



Graph 4: Typical Group Delay of AGC and Filter (with f_C = 23MHz)

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The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay (T_{GD}), in nanoseconds, is expressed below as a function of the cutoff frequency.

$$T_{GD} = 6ns + \frac{0.53}{f_C} \qquad \textit{(eq. 7)}$$

where f_C is the unboosted cutoff frequency in Hz.

Because the filter is AC-coupled from the Gain Control output, a zero occurs at DC and a pole occurs at about 60KHz. This pole-zero pair distorts the frequency response of the filter below frequencies of about 1.3MHz. Test Mode 0 bypasses the Gain Control circuit and AC-coupling network, which allows direct filter measurements from the DIP/DIN pins.

Pulse Detector and Qualifier (PDQ)

The PDQ receives filtered analog readback signals from the Read/Write Preamp and delivers qualified logic pulses to the Read Data Separator. Errors due to false peaks are detected in the PDQ and erased in the Data Separator prior to decoding of the data. A block diagram of the PDQ section is shown in Diagram 4 below.

Two analog input channels are processed by the PDQ. The timing channel inputs HRP/HRN (HR) are AC coupled from the differentiated output of the filter FDP/FDN. The level qualification channel inputs LQP/LQN (LQ) are AC coupled from the normal outputs of the filter FNP/FNN.

The high resolution signal is converted to digital pulses using a zero-crossing comparator and self-resetting one-shot circuit having a nominal pulse width of 3.5ns. The timing channel clocks a D-type Flip-Flop on either positive or negative transitions of the HR input. Visibility into the timing channel signals HRCOMP and HRCLK are provided in test mode (see Test Mode description).

The HR pulses are qualified by signals which are derived from the LQ channel. Two comparators indicate when the positive (LP) and negative (LN) extents of the LQ signal exceed a certain percentage of the average peak amplitude of the LQ signal. In addition, two peak detectors qualify consecutive same polarity peaks, if the subsequent peaks are of higher amplitude and have sufficient slope. All subsequent lower amplitude peaks are ignored. The first opposite polarity peak following a valid RDATA pulse is not slope qualified. The digital logic stores the polarity of the peak and qualifies consecutive peaks based on the sensitivity level threshold V_{TH}(detect) set by the PEAK Threshold DAC. If a second peak is qualified, an RDATA pulse is generated with a coincident Erase pulse. Two comparators indicate when the positive (POSPK) and negative (NEGPK) slope detectors exceed the sensitivity level threshold.

The average peak amplitude of the LQ signal is determined by an envelope follower circuit consisting of an input buffer ($A_V = 2$), a rectifier/peak detector, and a unity gain transconductance amplifier (g_m). The buffer stage drives a precision rectifier circuit combining the differential outputs such that the most positive extent of the signal is stored (peak detected) on an internal capacitor (10pF). The storage capacitor charges quickly from its common mode value ($V_{LQ} = 0$) to approximately $V_{LQ}/2$. It's rate of discharge is set by the current I_D, related to the charge pump normal discharging current (I_{QDN}) by the expression

$$I_D = \frac{I_{QDN}}{20} \qquad \textit{(eq. 8)}$$

The envelope follower output voltage (V_{ENVC}) on the ENVC pin 'follows' the peak detector voltage at a rate fixed by the transconductors output currents and the external capacitor ENVC. The transconductors charge and discharge currents, I_{EC} and I_{ED}, are also related to the charge pump normal discharging current (I_{QDN}) by the expressions

$$I_{EC} = 3.32 \cdot I_{QDN} \quad \text{and} \quad I_{ED} = \frac{I_{QND}}{8} \qquad \textit{(eq. 9)}$$

The charge current is 26.6X the discharge current resulting in an asymmetric response.

The product of the envelope follower is the output (V_{ENVC}), which is equal to one-half the average peak amplitude of the LQ signal. The envelope follower output voltage is combined with the dc control voltage, provided by the LVLQ DAC, to create the threshold for "level" qualification ($V_{TH(LQ)}$). The control word for the DAC is read from the LVLQ THRESHOLD register (Addr = 1101, bits[4:0]). The threshold voltage is set proportional to the average peak amplitude of the LQ signal (V_{LQ}) as specified by the DAC input according to following relationship:

$$V_{TH\,(LQ)}(qual) = V_{LQ} \times \left(\frac{1.1}{31}\right) \times N \qquad \textit{(eq. 10)}$$

where N ranges between 0 and 31decimal or 00000 to 11111 binary (bit 4 is the MSB).

In addition, the envelope follower output voltage is combined with the dc control voltage, provided by the PEAK DAC, to create the threshold for "peak" detection ($V_{TH(PD)}$). The control word for the DAC is read from the PEAK THRESHOLD register (Addr = 1110, bits[4:0]). The threshold voltage is set proportional to the average peak amplitude of the LQ signal (V_{LQ}) as specified by the DAC input according to following relationship:

$$V_{TH\,(PD)}(detect) = V_{LQ} \times \left(\frac{1.1}{31}\right) \times N \qquad \textit{(eq. 11)}$$

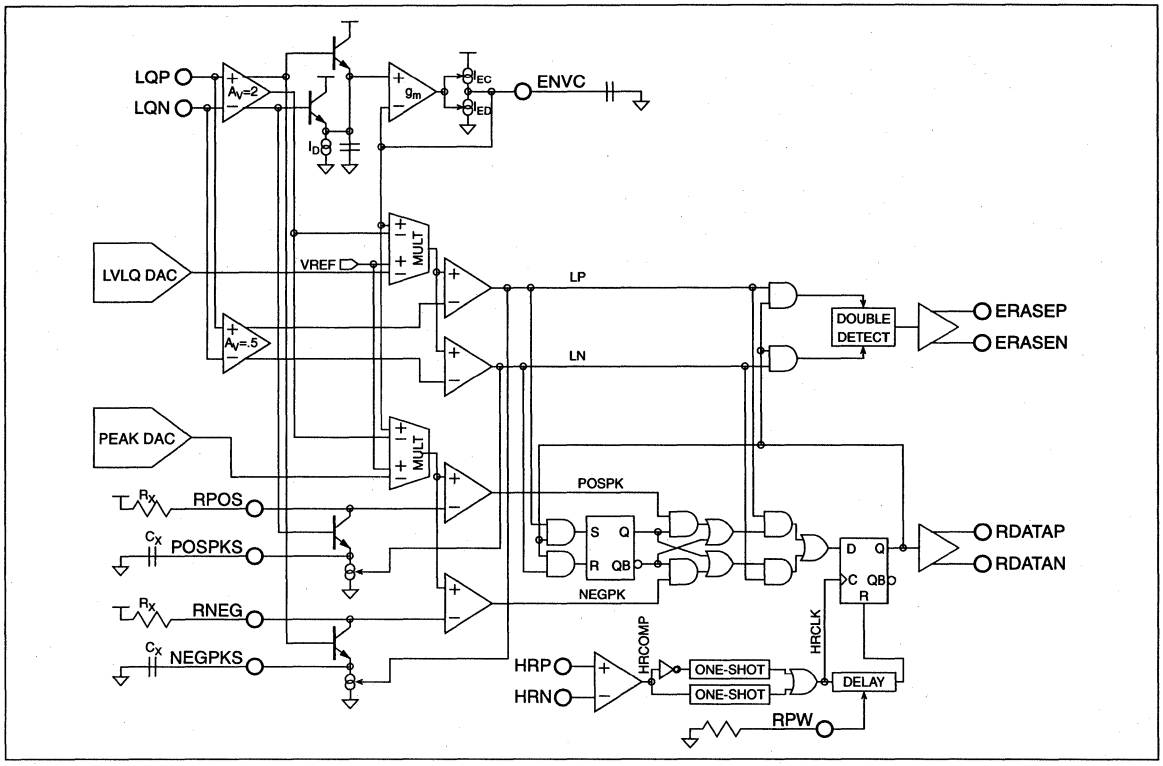
where N ranges between 0 and 31 decimal or 00000 to 11111 binary (bit 4 is the MSB). The slope detector threshold voltage is referenced to V_{CC} and is compared against the pin voltages of RPOS and RNEG, also referenced to V_{CC}. If the most negative extent of either V_{RPOS} or V_{RNEG} exceeds the sensitivity level threshold, comparator outputs POSPK or NEGPK produce a logical '1'. Qualified consecutive same polarity higher amplitude peaks produce both ERASE and RDATA pulses.

The signal voltages on the RPOS and RNEG pins depend on the external components selected. The RC time constant (Rx • Cx) and the LQ signal frequency (f_{LQ}) are both proportional to the magnitude of the voltage (V_{Rx}) across the Rx resistors. The expression for V_{Rx} can be written as

$$\begin{aligned} V_{Rx} &= Rx \cdot Cx \cdot \frac{dV_{LQ}}{dt} \\ &= Rx \cdot Cx \cdot 1.0V \cdot \pi \cdot f_{LQ} \cdot \sin(2 \cdot \pi \cdot f_{LQ} \cdot t) \end{aligned} \qquad \textit{(eq. 12)}$$

where $V_{LQ} = 0.5V \cdot \sin(2 \cdot \pi \cdot f_{LQ} \cdot t)$. And thus the maximum peak voltage across RPOS and RNEG is

PULSE DETECTOR AND QUALIFEIER (PDQ) BLOCK



$$V_{Rx}(max) = Rx \cdot Cx \cdot 1.0V \cdot \pi \cdot f_{LQ} \qquad (eq.\ 13)$$

V_{Rx}(max) is frequency dependent, and hence Rx, Cx, and the slope detector sensitivity level (V_{TH}) must be chosen carefully over the frequency range of interest. For normal operation, $V_{Rx}(max) \geq\geq V_{TH}$ at the minimum signal frequency. The recommended resistance value ranges from 50Ω to 500Ω for Rx, and the capacitance value ranges from 20pF to 200pF for Cx. VTC also recommends using a low threshold of 5% to 30% (high sensitivity). The values chosen should be optimized for system requirements.

The qualified RDATA pulses have provision for external control of the pulse width via an external resistor connected to the RPW pin. The pulse width (PW_{RDATA}) ranges from 3ns to 18ns and is expressed as a function of RPW by the following

$$PW_{RDATA} = 0.5ns/K\Omega \cdot RPW + 1.8ns \qquad (eq.\ 14)$$

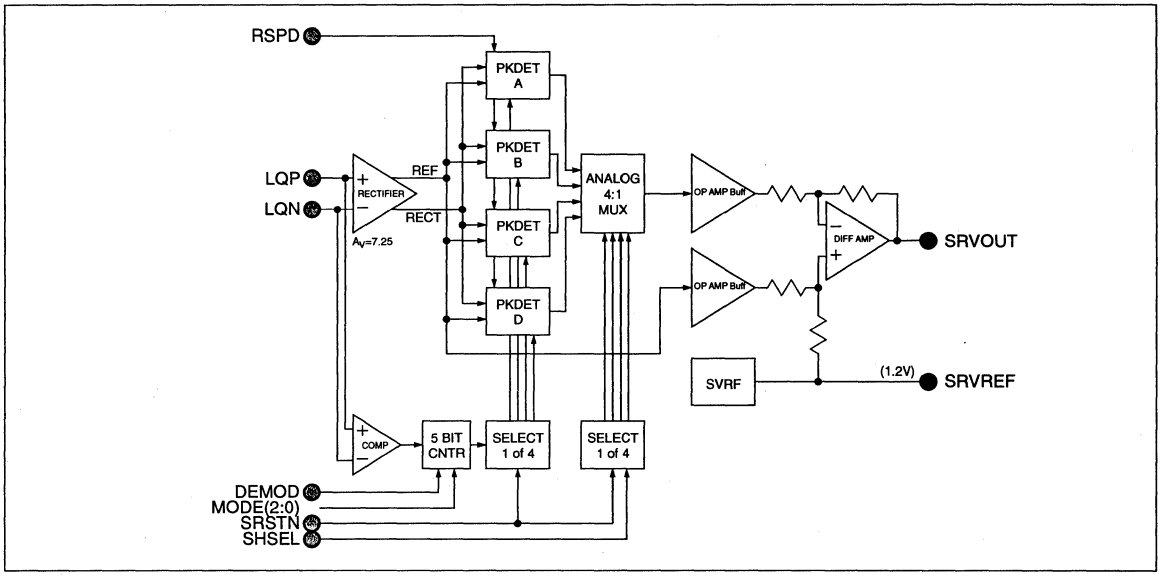
where RPW is given in KΩ and ranges from 4KΩ to 32KΩ.

Servo Demodulator

The servo demodulator supports full quadrature demodulation through the use of an array of four peak detector channels. A block diagram for the servo demodulator is shown above. The filtered servo bursts are AC coupled into the chip through the LQP and LQN inputs. The signal is amplified immediately to maximize the signal amplitude and reduce mismatch effects introduced by subsequent blocks. The amplified signal is full wave rectified and input to an array of four peak detectors. The peak detector consists of an emitter follower and on-chip hold capacitor. Each peak detector is selectively enabled and detects the peak voltage amplitude of the servo burst. After the peak has been detected, the peak detector is disabled and 'holds' the peak voltage for subsequent processing. A 4:1 analog switch allows each peak detector output to be multiplexed to the servo output. The multiplexed peak detector output and its corresponding reference are buffered before feeding into a difference amplifier. The difference amplifier output is the SRVOUT output pin and is referenced to the SRVREF pin (typically 1.2V).

The peak detectors capture the servo burst information under the control of the DEMOD input signal. Both synchronous and asynchronous modes of operation are supported. In asynchronous mode (MODE = 000_b), on the leading (rising) edge of the DEMOD input pin, the peak detectors are enabled and begin tracking the servo signal asynchronously. Likewise, on the falling edge, the peak detectors are disabled and asynchronously stop tracking the servo signal. In synchronous mode (MODE ≠ 000_b), the leading (rising) edge of the DEMOD input pin is synchronized to an internal clock. The clock is generated by a comparator that detects the high to low zero crossings of the input waveform to the peak detector. The comparator has 60mV of input hysteresis which removes low amplitude noise and yields cleaner clock transitions. The synchronized DEMOD signal causes the peak detectors to sample the input waveform synchronously with the incoming waveform to reduce any charge injection nonlinearity. The MODE[2:0] word (Addr = 1011,bits[7:5]) selects the number of cycles counted by a 5-bit

SERVO DEMODULATOR BLOCK DIAGRAM



counter. Note that the full wave rectifier causes both halves of a cycle to be peak detected. The definition of the decoding of the MODE[2:0] word is shown in the normal mode register decode table.

MODE[2:0] word			*MODE*	*NORMAL DEFINITION*
2	*1*	*0*		
0	0	0	0	async mode
0	0	1	1	4 cycles
0	1	0	2	8 cycles
0	1	1	3	12 cycles
1	0	0	4	16 cycles
1	0	1	5	20 cycles
1	1	0	6	24 cycles
1	1	1	7	28 cycles

If the proper number of cycles have not arrived when the trailing edge of the DEMOD input pin occurs, then the peak detectors asynchronously progresses to a Hold mode as a fail safe feature.

Consecutive cycles of the DEMOD pin cause the A, B, C, and D peak detectors to sample the input waveform. The SHSEL input pin is provided to select the various peak detector outputs. The rising edge of SHSEL causes the selection to change to the A peak detector, the second pulse selects B, etc. The servo demodulator control logic and all peak detectors are reset by a low level on the SRSTN input pin. Upon the low level of SRSTN, the SRVOUT pin is reset to the SRVREF voltage. The servo blocks may also be reset automatically by an internal one-shot. The one-shot initiates a reset pulse of ~500ns when SGATE = 1 and STBYN = 0. This automatic reset feature is useful when going back and forth between servo tracking and standby mode.

The RSPD pin gives the user some control of the peak detector bandwidth. A resistor is placed between the RSPD pin and the VCC1 supply. This resistor ties to the collector of each emitter follower in the peak detector. This is shown in Diagram 6.

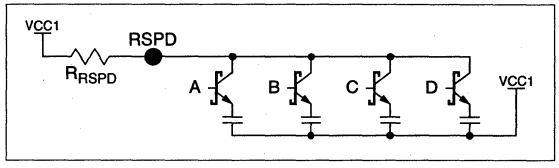


Figure 3: Peak Detector Bandwidth Control Circuitry

When a rising edge comes into the peak detector, the emitter follower charges the capacitor. The charging current flows through the collector and a voltage drop is seen across R_{RSPD}. If $Ic \cdot R_{RSPD}$ becomes large enough, the emitter follower will saturate thus limiting further charging of the capacitor. As R_{RSPD} is increased, the effective bandwidth of the peak detector is reduced and lessens the sensitivity to incoming noise spikes in the servo waveform.

$$\text{BandWidth} \propto \frac{1}{RSPD} \qquad \textit{(eq. 15)}$$

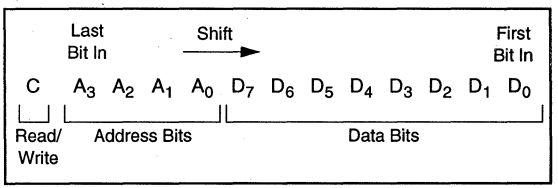
The RSPD Resistor Selection Table gives some typical values for RSPD as a function of servo frequency and the number of cycles used for demodulation. These RSPD values are the maximum resistance that may be used and still guarantee that the demodulated signal will reach 99.75% of the final value, given that servo frequency and number of demodulation cycles.

RSPD Resistor Selection Table

		# OF DEMOD CYCLES	
		4	28
SERVO INPUT FREQUENCY (MHz)	4	4KΩ	300KΩ
	10	1.5KΩ	20KΩ

Digital Control

Control of the chip is performed through a serial digital interface, a 7 byte register file and 5 digital to analog converters. Control information is stored in the register file and used directly as digital control lines or sent to one of the DACs to create analog control signals. The interface consists of four TTL-level signals for input data, output data, clock, and enable. Upon asserting SERENBN, the serial port is enabled and ready for input on SERDAT and SERCLK. The SERDAT line provides the data, address and read/Write control information. During a write cycle the serial control stream is shifted into the input register on the rising edge of the SERCLK starting with the LSB (bit0) of the data byte, after the MSB (bit 7) of the data has been read the four (4) address bits are clocked in starting with the LSB. After all 12 bits have been clocked into the shift register, a "0" must be placed on the SERDAT input (but NOT clocked in by SERCLK) to indicate data is being written to the chip. The data is then latched into the proper register when SERENBN is de-asserted. This process must be performed seven times to load all seven register banks. Refer to the Timing Diagram for Loading Internal Registers with the Serial Interface. The serial interface also has the capability of reading the programmed data back out of the internal registers on the SEROUT(tri-stated serial output) pin. After asserting SERENBN, a 4 bit address must be clocked into the shift register. A "1" must be placed on the SERDAT input (but NOT clocked in by SERCLK) to indicate data is being read from the chip. When the SERENBN line is de-asserted the SEROUT pin is taken out of tri-state mode and put into the active mode. After a short delay the output will settle to the state of bit0 from the selected register. To complete the read operation the SERENBN line must be reasserted and the SERCLK must be strobed to transfer successive bits to the output line. After the SERCLK line is strobed seven times the MSB of the data will be present on the output line. To read the address word the SERCLK must be strobed four additional times, at which time the MSB of the address will reside on the output line. To complete the read cycle the SERDAT line must be put into the "0" state and then the SERENBN can be de-asserted for the second time. After the SERENBN is de-asserted the second time the output buffer is placed into a high impedance tri-state mode. The Refer to the serial interface read timing diagram.



There are 8 control words used to drive the 5 control DACs. There are two control words one for SERVO mode and one for DATA mode for each of the three DACs FREQUENCY CUT-OFF, BOOST and VGA GAIN. The words are selected by the condition of the SGATE pin. The control range and resolution is given in the table below.

DAC Control Range and Resolution Table

DAC	RANGE		RESOLUTION STEP SIZE	UNITS
	MIN (000...)	MAX (111...)		
Frequency Control	3.75	30	0.207	MHz
Boost	0(0)	4.467(13)	0.298	V/V (dB)
VGA Gain	4	50	1.48	V/V
LVLQ Threshold	0	110	3.55	%
Peak Threshold	0	110	3.55	%

COMPONENT PINS

There are a number of different input and output buffers used on this chip. There are CMOS TTL inputs, Bipolar ECL-like differential outputs, Analog differential inputs, and several analog reference input and output pins. Because of pin limitations some pins serve double duty. A table showing the various pin types is provided below.

POWER SUPPLY PINS:

PIN NAME	PIN NO.	DESCRIPTION
VCC	10	Digital CMOS Power
VCC1	3	Analog Power
VCC2	20	Digital Bipolar Power

GROUND SUPPLIES PINS:

PIN NAME	PIN NO.	DESCRIPTION
VEE	15	Digital Ground
VEE1	32	Analog Ground
VEE2	43	Substrate Ground

CMOS TTL INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
FSREC (active High)	6	Fast Recovery mode control
SGATE	7	Servo mode control (active High)
LOWZ (active High)	8	Low Impedance mode control
HLDN Low)	9	AGC Hold mode control (active
SRSTN	11	Servo Reset (active Low)

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SHSEL 12 Servo Peak Detector select

DEMOD 13 Demodulation Clock

STBYN 14 Standby mode control (active Low)

SERENBN 40 Serial I/O enable (active low)

SERCLK 39 Serial clock (latch on positive edge)

SERDAT 38 Serial input data

TTL OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
SEROUT	35	Serial output data (alias stp)

EXTERNAL PINS:

PIN NAME	PIN NO.	DESCRIPTION
RPW	21	RDATA Pulse Width control, Resistor (4KΩ to 32KΩ) to Ground [see equation (14)]
RNEG	25	Negative Slope Detector Gain control, Resistor (50Ω to 500Ω) to VCC [see equation (13)]
RPOS	26	Positive Slope Detector Gain control, Resistor (50Ω to 500Ω) to VCC [see equation (13)]
RSPD	31	Servo Peak Detector Charge limit, Resistor (0 to 5KΩ) to VCC [see equation (15)]
REXT	44	Reference current for the control DACs Resistor (4.8K) to Ground [see equation (1)]
CAGCD	1	AGC Data Field Gain storage, Capacitor (390pF) to Ground
CAGCS	2	AGC Servo Field Gain storage, Capacitor (390pF) to Ground
NEGPKS	24	Negative Peak Voltage Level storage, Capacitor (20pF to 200pF) to Ground [see equation (13)]
POSPKS	27	Positive Peak Voltage Level storage, Capacitor (20pF to 200pF) to Ground [see equation (13)]
ENVC	28	Envelope Tracking Rate control, Capacitor (1200pF) to Ground

ANALOG DIFFERENTIAL INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
HRP	22-23	High Resolution Comparator
HRN		
LQP	29-30	Level Qualifier
LQN		
DIP	41-42	Read Data Input
DIN		

BIPOLAR ECL-LIKE DIFFERENTIAL OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
RDATAN	16-17	Pulse Detector Data Output
RDATAP		
ERASEN	18-19	Pulse Detector Erase Flag
ERASEP		
FDN	36-37	Filter Differentiated Output
FDP		
FNN	33-34	Filter Normal Output
FNP		

ANALOG OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
SRVREF	4	Servo Reference Voltage
SRVOUT	5	Selected Sample & Hold Amplifier Output

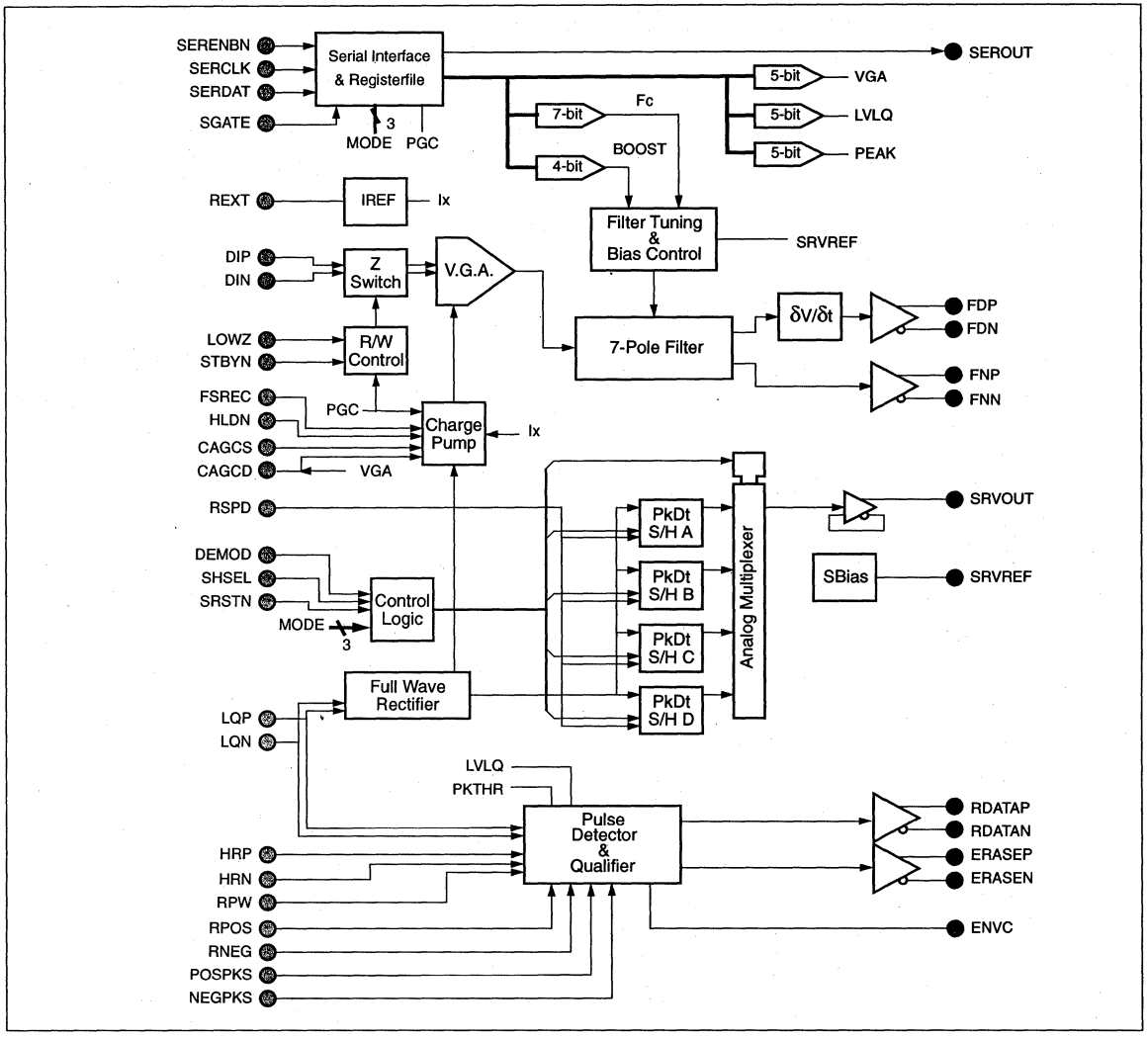
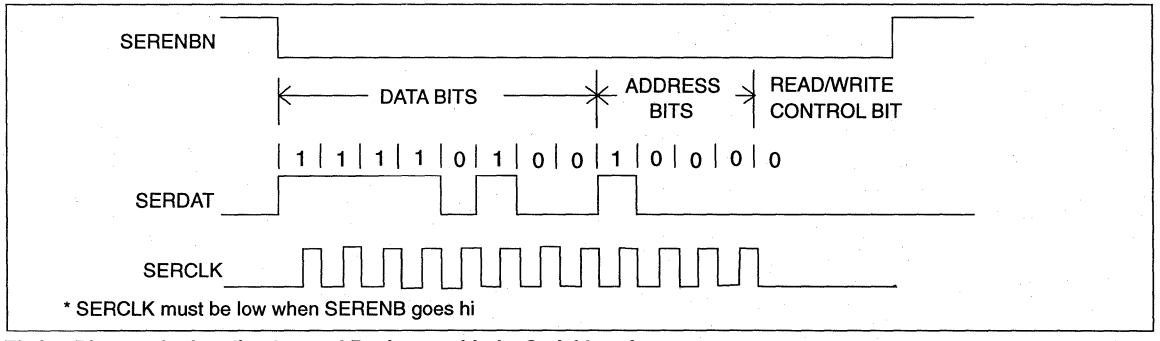
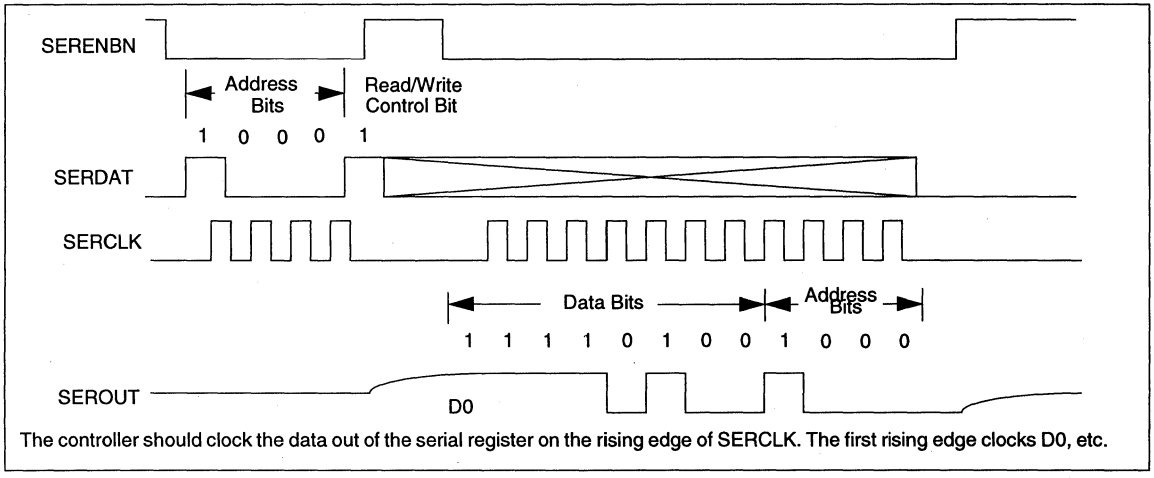


Figure 4: VM54100 Block Diagram



Timing Diagram for Loading Internal Registers with the Serial Interface



The controller should clock the data out of the serial register on the rising edge of SERCLK. The first rising edge clocks D0, etc.

Timing Diagram for Reading Internal Registers with the Serial Interface

Serial Register Table

Register Address	*DATA BIT*							
	7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
1000	SLEEP	DATA "FREQUENCY CUTOFF" DAC						
1001	PGC	SERVO "FREQUENCY CUTOFF" DAC						
1010	DATA "BOOST" DAC				SERVO "BOOST" DAC			
1011	TM2	TM1	TM0	DATA "VGA GAIN" DAC				
1100	TBD	TBD	IQTF	SERVO "VGA GAIN" DAC				
1101	TBD	TBD	TBD	"LVLQ THRESHOLD" DAC				
1110	TBD	TBD	TBD	"PEAK THRESHOLD" DAC				

SLEEP - (Addr1000, bit7). When LO, the chip goes into a sleep mode. The list of powered down blocks includes all those controlled by STBYN, the reference generators and OUTTTLZ

DATA FREQ CUTOFF DAC - (Addr1000, bits[6:0]). Sets the filter cutoff when SGATE is LO.

PGC - (Addr 1001, bit 7). When LO, it disables the AGC loop and enables the VGA gain DAC.

SERVO FREQ CUTOFF DAC - (Addr 1001, bits[6:0]). Sets the filter cutoff when SGATE is HI.

DATA BOOST DAC - (Addr 1010, bits[7:4]). Sets the filter boost when SGATE is LO.

SERVO BOOST DAC - (Addr 1010, bits[3:0]). Sets the filter boost when SGATE is HI.

TM2,TM1,TM0 (Addr 1011, bits[7:5]). Select bits for the test mode options.

DATA VGA GAIN DAC (Addr 1011, bits[4:0]). Set the VGA gain when the PGC bit is LO and SGATE is LO.

SERVO VGA GAIN DAC (Addr1100, bits[4:0]). Sets the VGA gain when hte PGC bit is LO and SGATE is HI.

IQTF - (Addr 1100, bit[5]) set charage pump current to track filter cutoff frequency.

LVLQ THRESHOLD (Addr 1101, bits[4:0]) set the relative threshold for for Pulse data qualification

PEAK THRESHOLD (Addr 1110, bits[4:0]) sets the peak qualification threshold

AC AND DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified $0°C < T_A < 70°C$, $4.5V < V_{CC} < 5.5V$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode, Data Rate = 24Mbps			<TBD>	mA
		Read Mode, Data Rate = 1Gbps		<TBD>	<TBD>	mA
		Standby Mode			<TBD>	mA
Recovery time Standby to fully functional	T_{REC}	AGC within 10% final value, Pulse Detector w/o pulse pairing, Filter cutoff within 10% final value			10	µs

LOGICAL SIGNALS: ALL DIGITAL PINS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input High Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input Leakage Current	I_{IL}	$V_{IL} = 0.8V$			±10	µA
	I_{IH}	$V_{IH} = 2.0V$			±10	µA
Control Signal rise and fall times	T_{CS}				100	ns
Input Capacitance	C_{IN}				10	pF

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GAIN CONTROL

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Common for both AGC and PGC modes						
Input dynamic range	V_{DI}	$V_{DI} = (V_{DIP} - V_{DIN})$ [THD_S applies for 250 to 320mV_{ppd}]	24		320	mV_{ppd}
Input common mode voltage	V_{CMDI}	$V_{CMDI} = (V_{DIP} + V_{DIN})/2$	V_{CC}–3.1	Vcc-2.7	V_{CC}–2.3	V
Differential input resistance	$R_{in(DA)}$	LOWZ = Low	3.0	6.0	9.0	KΩ
		LOWZ = High	50	100	150	Ω
Single ended input impedance	$R_{in(SA)}$	LOWZ = Low	1.5	3.0	4.5	KΩ
		LOWZ = High	25	50	75	Ω
Output common mode voltage	V_{CMFN}	$V_{CMFN} = (V_{FNP} + V_{FNN})/2$ Test Mode 5	V_{CC}–3.4	Vcc-3.0	V_{CC}–2.6	V
Output common mode voltage	V_{CMFD}	$V_{CMFD} = (V_{FDP} + V_{FDN})/2$ Test Mode 5	Vcc-3.0	Vcc-2.6	Vcc-2.2	V
Output offset voltage	V_{OS}	for V_{FN}, over entire gain range, Test Mode 5	–200		200	mV
Output distortion of V_{FN}	THD	V_{DI} = 250mV_{ppd}, $V_{FN} \leq 1.1V_{ppd}$, Test Mode 5, 1st, 2nd, and 3rd harmonics only			1.0	%
RX pin voltage	V_{RX}	R_{ext} = 6KΩ<TBD>	1.05	1.2	1.35	V
Only for AGC mode (PGC=Low)						
Output dynamic range	V_{FN}	$V_{FN} = (V_{FNP} - V_{FNN})$ 24$mV_{ppd} \leq V_{DI} \leq$ 250mV_{ppd} 4MHz < f_{in} < 36MHz	0.9		1.1	V_{ppd}
AGC minimum Gain	AV_{min}	$AV=V_{FN}/V_{DI}$ V_{CAGCD}=0.8v, Test Mode 5, [0]			4.0	V/V
AGC maximum Gain	AV_{max}	$AV=V_{FN}/V_{DI}$ V_{CAGCD}=3.2v, Test Mode 5, [0]	38	50		V/V
Gain settle from –30% V_{DI} step	T_{GD}	$V_{FN} \geq 0.9 \cdot$(final value)		31	TBD	µs
Gain settle from +30% V_{DI} step	T_{GA}	$V_{FN} \leq 1.1 \cdot$(final value)			2.0	µs
Charge Pump Normal Discharging current	I_{QDN}	0.55v ≤ V_{LQ} ≤ 0.56v (static), R_{ext} = 4.8KΩ	210	250	280	µA
Charge Pump Fast Discharging current	I_{QDF}	$V_{LQ} \geq$ 0.70v (static)	$6.8 \cdot I_{QDN}$		$7.5 \cdot I_{QDN}$	µA
Charge Pump Normal Charging current	I_{QCN}	$V_{LQ} \leq$ 0.40v (static)	I_{QDN}+44		I_{QDN}+36	µA
Charge Pump Fast Charging current	I_{QCF}	$V_{LQ} \leq$ 0.40v (static), FSREC Low to High edge triggered	$6.8 \cdot I_{QDN}$		$7.5 \cdot I_{QDN}$	µA
Charge Pump Leakage current	I_{LK}	HLDN = Low	–10		10	nA
Only for PGC mode (PGC=High)						
PGC minimum Gain	AV_{min}	$AV=V_{FN}/V_{DI}$ VGA_{DAC}=0h, Test Mode 5,			4.0	V/V
PGC maximum Gain	AV_{max}	$AV=V_{FN}/V_{DI}$ VGA_{DAC}=1Fh, Test Mode 5,	38	50	56	V/V

[0] Linearity of 0.5% from 1/8 to 7/8 of 550 mV_{ppd} required.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Common for both AGC and PGC modes						
Special Distortion	THD_S	250 mV ≤ V_{DI} ≤ 320 mV, V_{FN} ≤ 1.1V_{ppd} , Test Mode 5			4	%
Differential input capacitance	$C_{in(DA)}$				10	pF
Input referred noise voltage	V_{IRN}	gain =AV_{max}, BW = 15MHz V_{DIP} = V_{DIN}			10	nV/√Hz
Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common mode rejection ratio	$CMRR_G$	gain = AV_{max}, f_{in} = 5MHz, V_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_G$	gain = AV_{max}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB
Only for AGC mode (PGC=Low)						
AGC Gain Sensitivity to CAGCx voltage	AV_{PV}	(Typical range is 1.4v to 2.8v)		17.5		dB/V
Only for PGC mode (PGC=High)						
Settling time to step change in VGA_{DAC}	T_{PGS}	zero to full scale after completion of the write cycle (SERENBN ↑)			300	ns

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Normal output noise voltage	V_{NN}	BW = 100MHz, f_C = 37.5MHz [1] V_{DIP} = V_{DIN} , Test Mode 4			TBD	mV_{rms}
Differentiated output noise voltage	V_{ND}	BW = 100MHz, f_C = 37.5MHz [1] V_{DIP} = V_{DIN} , Test Mode 4			9.0	mV_{rms}
Common mode rejection ratio	$CMRR_F$	f_{in} = 5MHz, Fc_{DAC}=7Fh , REXT=4.8KΩV_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp}	40			dB
Filter settle from step in Fc and BOOST	T_{FS}	Fc_{DAC} or $BOOST_{DAC}$ step to V_{FN} settle			300	ns
Group delay variation (normal or differential)	T_{GD3}	2.3MHz ≤ f_{in} ≤ 1.5f_C, 6MHz ≤ f_C ≤ 37.5MHz, V_{DI} = 250mV_{ppd} , $BOOST_{DAC}$=Fh ,	–3.6		3.6	ns
	T_{GD4}	1.3MHz ≤ f_{in} ≤ 1.5f_C, 6MHz ≤ f_C ≤ 37.5MHz, V_{DI} = 250mV_{ppd} , $BOOST_{DAC}$=Fh,	–5.25		5.25	ns
[1] Fc_{DAC}=7Fh, $BOOST_{DAC}$=Fh (boost level is 8.6dB).						
For Reference Sources and Gain Control Inputs						

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LOW PASS FILTER (7-POLE, 0.05°, EQUIRIPPLE PHASE)

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Filter cutoff frequency (low end)	f_{Cmin}	Fc_{DAC}=00h , REXT=4.8KΩ	3.18	4.68	5.38	MHz
Filter cutoff frequency (middle)	f_{Cmid}	Fc_{DAC}=40h , REXT=4.8KΩ	19	21.12	23.2	MHz
Filter cutoff frequency (high end)	f_{Cmax}	Fc_{DAC}=7Fh , REXT=4.8KΩ	33.75	37.5	41.25	MHz
Normal lowpass gain (V_{FN} vs. V_{DI})	AO_N	no boost, Fc_{DAC}=00h , REXT=4.8KΩ, f_{in} = 4MHz, Test Mode 4	-1.0	0	1.0	dB
Differentiated lowpass gain (V_{FD} vs. V_{FN}))	AO_D	no boost, $f_{in} = 0.67f_C$, Test Mode 4	AO_N–5.0	AO_N–3.5	AO_N-2.3	dB
Filter Boost (low end)	AB_{min}	$BOOST_{DAC}$=0h , REXT=4.8KΩ		0	0.5	dB
Filter Boost (high end)	AB_{max}	$BOOST_{DAC}$=Fh , REXT=4.8KΩ	11.5	13.0	16.0	dB
Normal filter output offset	V_{OSFN}	V_{DI} = 0.0v, Test Mode 4	–200		200	mV
Differentiated filter output offset	V_{OSFD}	V_{DI} = 0.0v, Test Mode 4	–200		200	mV
Total harmonic distortion (V_{FN} or V_{FD} vs. V_{DI})	THD_F	$f_{in} = 0.67f_C$,Fc_{DAC}=7Fh , REXT = 4.8KΩ, $V_{DI} \le 1.0V_{ppd}$, Test Mode 4, 1st, 2nd, and 3rd harmonics only			1.5	%
Filter Input common mode level (V_{DI})	F_{ICM}	Test Mode 4	Vcc-3.1	Vcc-2.7	Vcc-2.3	V
Phase shift from FNP-N to FDP-N (upper)	PS_{FU}	$f_{in} = 0.67f_C$, $f_C \ge$ 20MHz	85	90	95	degree
Phase shift from FNP-N to FDP-N (lower)	PS_{FL}	$f_{in} = 0.67f_C$, $f_C <$ 20MHz	87	90	93	degree
Normal/Diff common mode voltage	V_{CMFx}	Normal Output Differential Output	V_{CC} – 2.6 V_{CC} – 3.0	V_{CC}–2.2 V_{CC} –2.6	V_{CC} – 1.8 V_{CC} – 2.2	V
Normal/Diff output resistance	R_{OFx}				60	Ω
Normal/Diff output current	I_{OFx}		–1.0		1.0	mA
Group Delay	T_{GD}	Fc_{DAC}=7Fh , REXT=4.8KΩ	15	20	25	ns
Group delay variation (normal or differential)	T_{GD1}	$0.1f_C \le f_{in} \le 1.5f_C$, 10MHz ≤ f_C ≤ 38MHz, $V_{DI} = 1.0V_{ppd}$, $BOOST_{DAC}$=0h , REXT=4.8KΩ, Test Mode 4	–4		+4	%
	T_{GD2}	$0.1f_C \le f_{in} \le 1.5f_C$, 10MHz ≤ f_C ≤ 38MHz, $V_{DI} = 1.0V_{ppd}$, $BOOST_{DAC}$=Fh , REXT=4.8KΩ, Test Mode 4	–5		+5	%

PULSE QUALIFIER (PDQ)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input dynamic range	V_{LQ}	$V_{LQ} = (V_{LQP} - V_{LQN})$	0.5		1.5	V_{ppd}
Input common mode voltage	V_{CMLQ}	$V_{CMLQ} = (V_{LQP} + V_{LQN})/2$	V_{CC}–2.6	V_{CC}–2.2	V_{CC}–1.8	V
LQP/N differential input resistance	R_{LQ}		3.0		9.0	KΩ
HRP/N differential input resistance	R_{HR}		3.0		9.0	KΩ
ENVC Common Mode Voltage	V_{ENV0}	V_{LQ} = 0.0v	V_{CC} – 2.5	V_{CC}–2.1	V_{CC} – 1.7	V
Envelope follower offset [2]	N_{EO}	V_{ENVP} for V_{LQ}=+0.25v and V_{ENVN} for V_{LQ}=–0.25v	–3.0		3.0	%
Envelope follower gain	A_{ENV}	$\Delta N_{EO} / \Delta V_{LQ}$, where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
Envelope follower charging current	I_{EC}	$V_{ENV} = V_{ENV0} - 0.5v$, V_{LQ} = 0.0v, R_{EXT}=4.8KΩ	700	875	1050	µA
Envelope follower discharging current	I_{ED}	$V_{ENV} = V_{ENV0} + 0.5v$, V_{LQ} = 0.0v, R_{EXT}=4.8KΩ	30	37.5	45	µA
Envelope follower current tracking	N_{EI}	Variation of I_{EH} to I_{EL} ratio, $[(I_{EC}/I_{ED})(25/660)-1]\cdot 100$	–15		15	%
POSPKS detector gain	A_{PDP}	$\Delta V_{POSPKS} / \Delta V_{LQ}$, where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
NEGPKS detector gain	A_{PDN}	$\Delta V_{NEGPKS} / \Delta V_{LQ}$, where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
xPKS Common Mode Voltage	V_{CMxPKS}	V_{LQ} = 0v	V_{CC} –4.0	V_{CC}–3.5	V_{CC} – 3.0	V
POSPKS leakage current	I_{PL}	$LVLQ_{DAC}$=09h(32%), V_{LQ} = 0.0v, $V_{POSPKS} = V_{CMPPKS} + 0.5v$	–1		1	µA
NEGPKS leakage current	I_{NL}	$LVLQ_{DAC}$=09h(32%), V_{LQ} = 0.0v, $V_{NEGPKS} = V_{CMNPKS} + 0.5v$	–1		1	µA
POSPKS discharge current	I_{PD}	$LVLQ_{DAC}$=09h(32%), V_{LQ} = -0.5v, $V_{POSPKS} = V_{CMPPKS} + 0.5v$	12.5	15	17.5	mA
NEGPKS discharge current	I_{ND}	$V_{SETLV} = V_{REF} - 0.3v$, V_{LQ} = +0.5v, $V_{NEGPKS} = V_{CMNPKS} + 0.5v$	12.5	15	17.5	mA
Input dynamic range	V_{HR}	$V_{HR} = (V_{HRP} - V_{HRN})$	0.2		1.5	V_{ppd}
Input common mode voltage	V_{CMHR}	$V_{CMHR} = (V_{HRP} + V_{HRN})/2$	V_{CC}–3.0	V_{CC}–2.6	V_{CC}–2.2	V
HRP,N input frequency range	$f\Delta_{HR}$		2.3		38	MHz
Level Qual Threshold	TH_{LVLQ}	0.5v ≤ V_{LQ} ≤ 1.5v,(32%) $LVLQ_{DAC}$=09h	22		42	%
		0.5v ≤ V_{LQ} ≤ 1.5v,(81.6%) $LVLQ_{DAC}$=17h	70		95	%
Peak Detect Threshold	TH_{PD}	0.5v ≤ V_{LQ} ≤ 1.5v, (32%) $PEAK_{DAC}$=09h	22		42	%
		0.5v ≤ V_{LQ} ≤ 1.5v,(81.6%) $PEAK_{DAC}$=17h	70		95	%
Pulse pairing, $T_{PP} = 0.03/(16\cdot f_{in})$ $\phi_{HR}=\phi_{LQ} - 90^{\circ}$ [HR leads LQ in phase]	T_{PP}	$V_{LQ} = V_{HR}$ = 500mV_{ppd}, f_{in} = 4 MHz			468	ps
		$V_{LQ} = V_{HR}$ = 500mV_{ppd}, f_{in} = 38 MHz			67	ps

[2] where $N_{EO} = (V_{ENVP}-V_{ENVN}) / (V_{ENVP}+V_{ENVN})$

DATA RECOVERY CIRCUITS

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PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
For both RDATAP/N and ERASEP/N outputs						
Single ended output high level	V_{OHpe}	I_{OHpe} = 4.0mA	V_{CC} – 1.0		V_{CC} – 0.6	V
Single ended output low level	V_{OLpe}	I_{OLpe} = –4.0mA	V_{CC} – 1.9		V_{CC} – .975	V
Single ended output swing	V_{Spe}		375	500	1000	mV
Pulse width	T_{PW1}	Max. pulse width, RPW=24KΩ [3]	11		17	ns
	T_{PW2}	Min. pulse width, RPW=8KΩ [3]	4		8	ns
Idle	T_{PW3}	Relaxation time trailing to leading edge [3]	3		8	ns
[3] Measured from differential cross over points.						

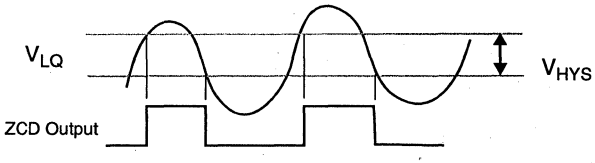
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Pseudo ECL rise and fall times	T_{RF}	±375mV of Zero cross, C_L=15pF, 220Ω across output			2.0	ns
delay from leading edge RDATA to leading edge ERASE	T_{EF}	[3]			±3.0	ns
peak detect sensitivity (of successive peaks)	Vps	TBD	200			mV
[3] Measured from differential cross over points.						

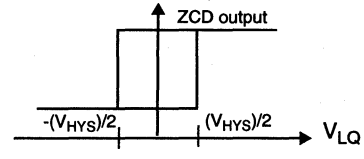
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
LQ comparator DC gain	A_{LQ}			700		V/V
HR comparator DC gain	A_{HR}			1600		V/V
Internal envelope detector discharge current	I_{ID}	R_{EXT}=4.8KΩ		12.5		µA
Internal envelope detector capacitance	C_{ID}		9		11	pF
LQ comparator input offset	V_{LO}				2	mV
LQ comparator input offset drift	V_{LT}				10	µV/°C
HR comparator input offset	V_{HO}				0.8	mV
Data detection F/F setup time	T_{DS}				1	ns

SERVO PEAK DETECTING DEMODULATOR

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Servo Input frequency	f_{INS}		4		13.5	MHz
Gain $[(V_{SVO}-V_{SVR})/V_{LQ}]$	AV_S	measured over 1/4 to 3/4 of scale [4]	1.60	1.725	1.85	V/V
Input dynamic range [low end]	V_{DIL}	$V_{DIL}=(V_{DIP}-V_{DIN})$ 1/8 of 24mVppd min [5]			3	mV_{ppd}
Input dynamic range [high end]	V_{DIH}	$V_{DIH}=(V_{DIP}-V_{DIN})$ 7/8 of 250mVppd max [5]	218			mV_{ppd}
Linearity of V_{FN} vs. V_{DI}	V_{FL}	measured over 1/8 to 7/8 of scale [6]	–0.5		0.5	%
Linearity of $V_{SVO}-V_{SVR}$ vs. V_{DI}	V_{DL1}	measured over 1/8 to 3/4 of scale [6]	–1.4		1.4	%
	V_{DL2}	measured over 3/4 to 7/8 of scale [6]	–4.5		4.5	%
Output offset (not referred to input)	V_{SO}	intercept of regressed line [6]	–40		40	mV
Output for zero input	V_{ZI}	[6]	0	60	80	mV
Mismatch of sample & holds	V_{MM}	Variation for a common input % of full scale			±1.0	%
SRVREF voltage	V_{SR}		1.14	1.20	1.26	V
Sample and Hold voltage decay rate	V_{DR}	0.1% of full scale droop in 50µs			40	V/sec
ZX comparator differential hysteresis	V_{HYS}	4% to 8% of full scale at LQ pins [7]	40		80	mV_{ppd}

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[5] V_{DIL} and V_{DIH} specify the input range over which all other specifications must be met.
[6] In addition to the linearity and offset specifications, the output must also be guaranteed monotonic.
[7] Refer to waveshapes below for this specification.





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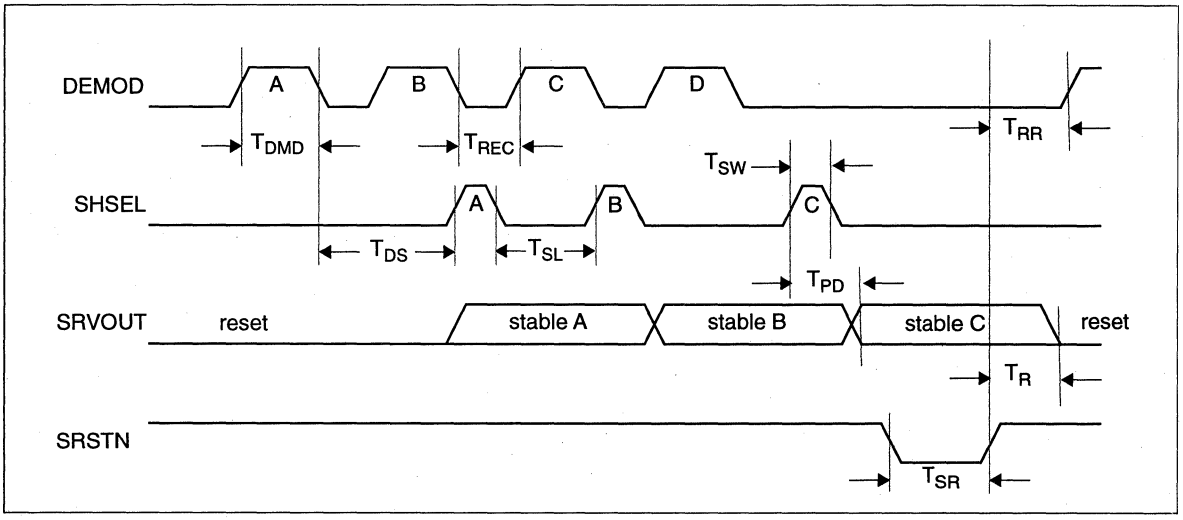
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Channel to channel cross talk	V_{CT}	Effect of A on B etc. % of full scale			±0.5	%
Output impedance	R_{SO}	SRVREF and SRVOUT pins			50	Ω
Demodulator repeatability (52dB)	N_{DR}	Repeatability without external noise			±5.0	mV
Power supply rejection ratio	$PSRR_S$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp} [8]	25			dB
Common mode rejection ratio	$CMRR_S$	0MHz ≤ f_{in} ≤ 1MHz V_{LQP} = V_{LQN} = 100mV_{pp} [8]	25			dB
Total System Gain Variation $[(V_{SVO}-V_{SVR})/V_{DI}]$	AV_A	over all V_{DI}, 1/4 to 3/4 of scale [4]	1.54	1.725	1.92	V/V

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[8] The required demodulator output Signal-to-Noise Ratio (SNR) due to external noise is 49dB.

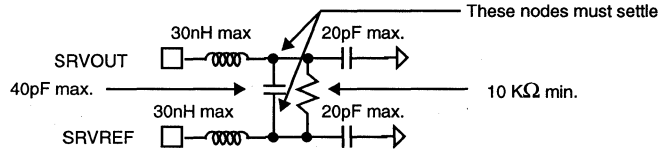
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Peak Detector Bandwidth	f_{PD}	-3dB roll down of rectifier	68			MHz

DEMODULATOR TIMING (Pins: DEMOD, SHSEL, SRVOUT, SGATE, SRSTN)



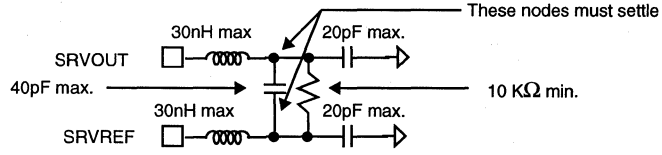
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Select clock pulse width	T_{SW}		50			ns
Select clock (SHSEL) to stable SRVOUT delay	T_{PD}	0.25% of final value [9]			150	ns
SRSTN pulse width	T_{SR}		600			ns

[9] Load condition for SRVOUT and SRVREF given below.

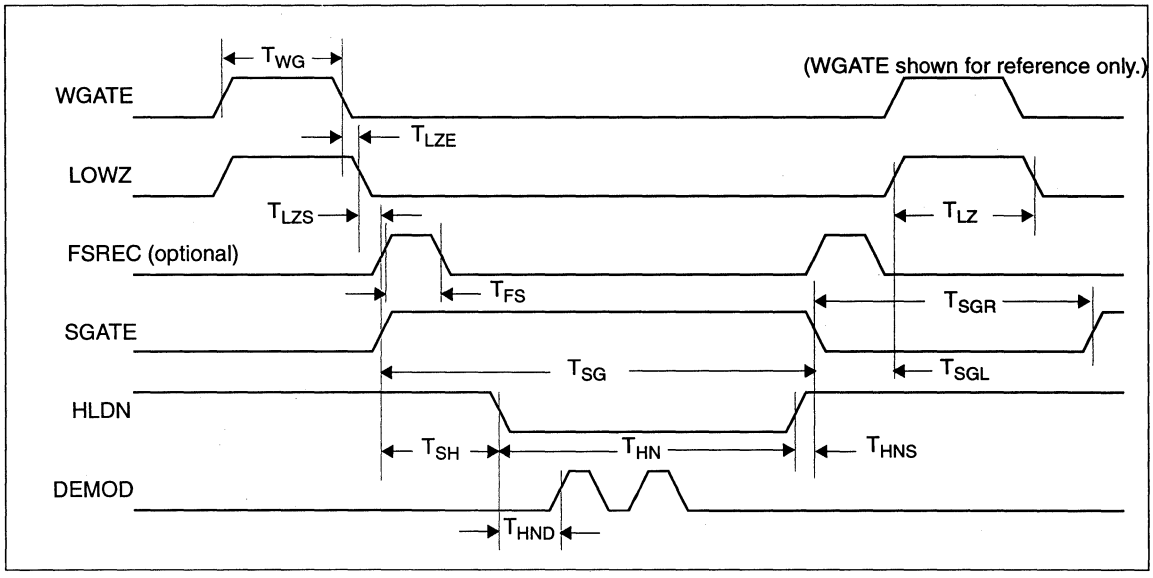


PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
DEMOD pulse width	T_{DMD}		150			ns
DEMOD recovery time	T_{REC}		150			ns
Select clock (SHSEL) inactive time	T_{SL}		50			ns
DEMOD to corresponding select clock delay	T_{DS}		0			ns
Sample and Hold step response	T_{SH}	0.25% of final value [9]			150	ns
Trailing edge SRSTN to SRVOUT reset delay	T_R	0.25% of final value [9]	150			ns
Trailing edge SRSTN to DEMOD recovery	T_{RR}		100			ns

[9] Load condition for SRVOUT and SRVREF given below.



SYSTEM TIMING DIAGRAM (NORMAL MODE) (Pins: LOWZ, FSREC, SGATE, HLDN, DEMOD)

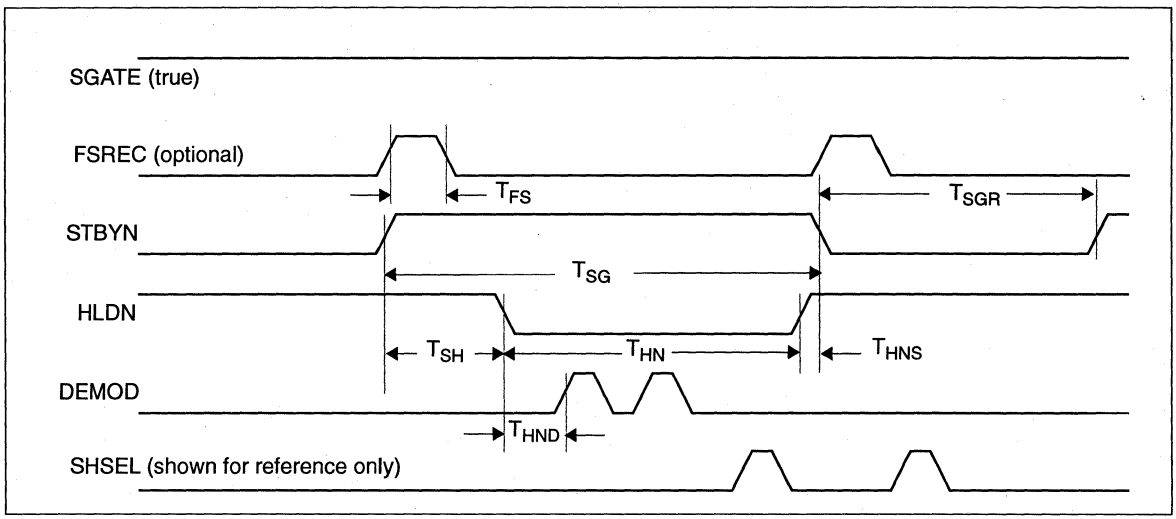


PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
FSREC leading edge to V_{FN} stable	T_{FD}	V_{FN} stable within 10%			2.3	µs
Trailing edge of LOWZ to V_{FN} stable to 10%	T_{WR}	CAGCD value correct			500	ns
Lead, trailing edge SGATE to V_{FN} stable 10%	T_{GS}	CAGCS or D value correct			500	ns

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
LOWZ pulse width	T_{LZ}		1.6			µs
LOWZ to SGATE delay	T_{LZS}		–500			ns
SGATE (or STBYN) pulse width	T_{SG}		5			µs
SGATE (or STBYN) inactive width	T_{SGR}		100			µs
SGATE to LOWZ delay	T_{SGL}		0			ns
HLDN pulse width	T_{HN}		500			ns
HLDN to DEMOD delay	T_{HND}		25			ns
trailing edge of HLDN to SGATE delay	T_{HNS}		0			ns
FSREC pulse width	T_{FSW}		80		250	ns

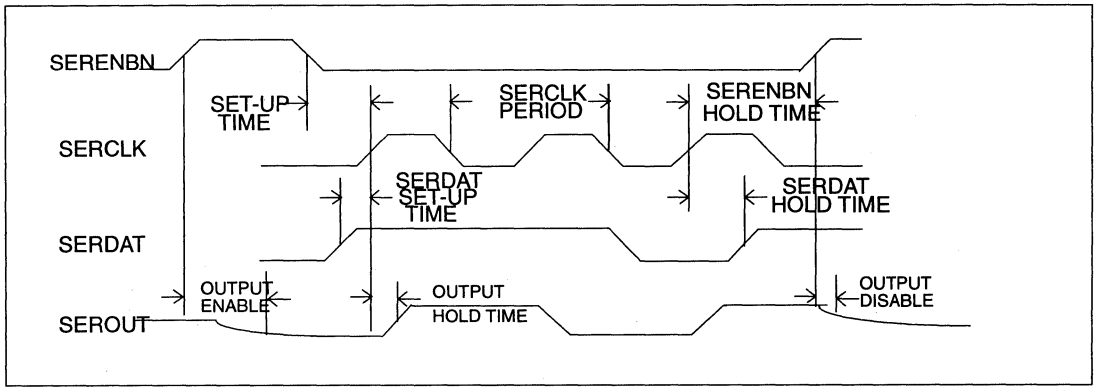
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WGATE pulse width (given for reference only)	T_{WG}		1.6			µs
LOWZ extension time	T_{LZE}				500	ns

SYSTEM TIMING DIAGRAM (STANDBY MODE) (Pins: FSREC, SGATE, STBYN, HLDN, DEMOD)



PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
SGATE (or STBYN) pulse width	T_{SG}		5			µs
SGATE (or STBYN) inactive width	T_{SGR}		100			µs
HLDN pulse width	T_{HN}		500			ns
HLDN to DEMOD delay	T_{HND}		25			ns
Trailing edge of HLDN to SGATE delay	T_{HNS}		0			ns
FSREC pulse width	T_{FSW}		100		250	ns
FSREC leading edge to V_{FN} stable	T_{FDT}	V_{FN} stable within 10%			3.8	µs
Lead, trailing edge STBYN to V_{FN} stable 10%	T_{GST}	CAGCS or CAGCD value correct			2	µs

SERIAL INTERFACE DIAGRAM



PARAMETER	*SYM*	*MIN*	*TYP*	*MAX*	*UNITS*
SERENBN pulse width	t_{pwSRE}	200			ns
SERDAT set-up time	t_{sSERD}	20			ns
SERDAT hold time	t_{hSERD}	5			ns
SERENBN set-up time	t_{sSRE}	40			ns
SERENBN hold time	t_{hSRE}	40			ns
SERCLK period	t	50			ns
SERENBN hi to low	t	50			ns
SEROUT enable	t_{OEN}			20	ns
SEROUT disable	t_{ODIS}			30	ns
SEROUT hold time	t_{OUTHLD}	8			ns

VTC Inc.
Value the Customer™

VM54750

PULSE DETECTOR WITH FILTER AND SERVO PEAK DETECT

August,1994

FEATURES

- Compatible with 75 MBits/sec NRZ Data Rate Operation
- Dual Mode VGA Supports AGC and PGC Modes
- Low Z and Fast AGC Modes for Quick Write Recovery
- Programmable Filter with Pulse Slimming
- Multiplexed Filter Tuning Supports Servo and Data Fields
- Demodulation of Servo Bursts
- Low Power (Standby) Mode

DESCRIPTION

The VM54750 consists of a variable gain amplifier (VGA) with an automatic gain control circuit. The automatic gain control (AGC) circuit can be disabled, which allows the VGA to be operated in programmable gain control (PGC) mode.

A seven pole linear phase 0.05 degree equiripple low pass filter (LPF) with pulse slimming is included in the VM54750. Normal and differentiated outputs from the filter are provided with matched delays.

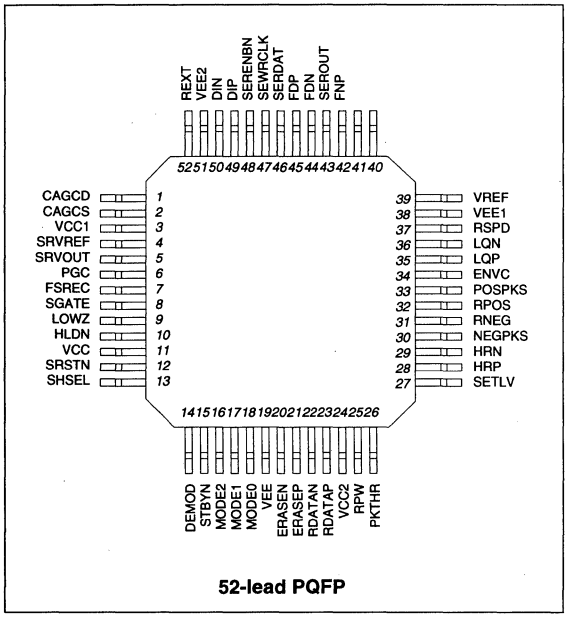
The filter provides for programmable unboosted cutoff frequencies from 3.75MHz to 30MHz. Likewise, the pulse slimming is programmable from 0dB to 13dB.

A pulse detector and qualifier is provided which includes an envelope detector, adjustable dV/dt sensitivity, programmable threshold and independent qualification of negative and positive threshold to suppress error propagation.

A peak detecting servo demodulator with an array of sample and hold amplifiers provides for the demodulation of up to four servo fields.

A low power mode is available through the use of the STBYN pin. In standby mode (STBYN) the VGA, sections of the filter, the PDQ, and the demodulator sections are powered down when STBYN = 0

CONNECTION DIAGRAM



52-lead PQFP

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
- V_{CC} ..... -0.3V to 7.0V

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to V_{CC} +0.3V
- Analog Input Voltage V_{IN} ..... -0.3V to V_{CC} +0.3V

Junction Temperature T_J ..... 150°C
Storage Temperature T_{stg} ..... -65° to 150°C
Thermal Impedance Θ_{JA}:
- 52-lead PQFP ..... 70°C/W

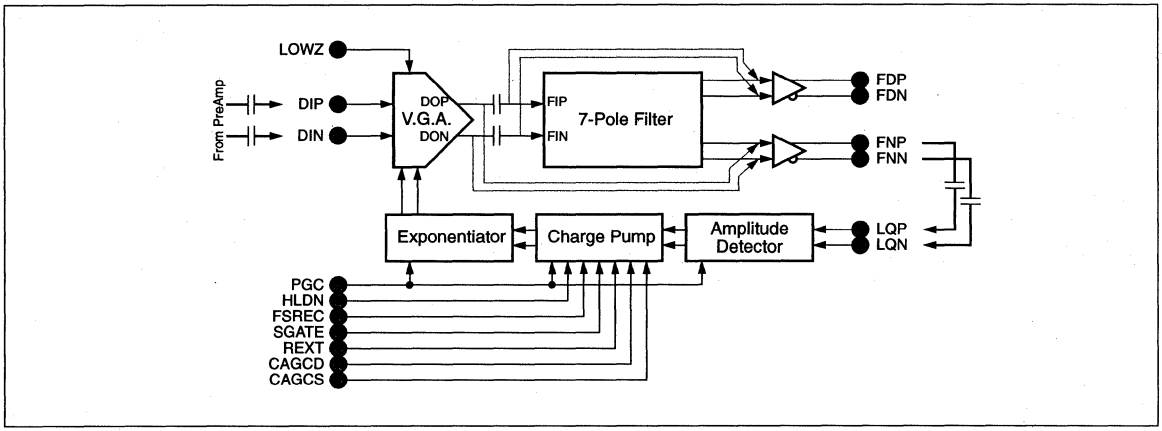
RECOMENDED OPERATING CONDITIONS

Supply Voltage:
- V_{CC} .....+5V ±10%

Junction Temperature ..... 0° to 125°C

DATA RECOVERY CIRCUITS

BLOCK DIAGRAM



Gain Control (GC)

The Gain Control section of the VM54750 consists of a wide band variable gain amplifier (VGA) with a charge pump, amplitude detector, and exponentiator. The Gain Control has two modes: Automatic (AGC), and Programmable (PGC) gain control. The mode of the Gain Control is controlled by the PGC digital input.

The read back signal is externally AC coupled into the VGA amplifier on the DIP/DIN pins (see the Block Diagram). The signal is amplified by the VGA and equalized by the 0.05° equiripple low pass filter. The normal output of the filter, FNP/FNN, is externally AC coupled back into the LQP/LQN inputs where it is amplitude detected by the AGC loop and locked to $1.0V_{ppd}$. With a nominal filter gain of 1.0 volts/volt, the VGA provides a $1.0V_{ppd}$ signal to the filter for inputs ranging from 24 to 320 mV_{ppd} on the DIP/DIN pins. A test mode is provided (test mode 5) in which the filter is completely bypassed, and the VGA outputs DOP/DON and filter inputs FIP/FIN are multiplexed to the FNP/FNN and FDP/FDN chip outputs respectively.When in the AGC mode (PGC = 0), the gain of the VGA is controlled by an amplitude detector, charge pump, exponentiator, and CAGCx capacitor, either CAGCD or CAGCS. The amplitude detector determines if the signal level (V_{LQ}) at the LQP/LQN inputs is above or below the target amplitude of $1.0V_{ppd}$. If the amplitude is below $1.0V_{ppd}$, the normal charging current (I_{QCN}) charges the CAGCx capacitor to increase the gain of the VGA. If the amplitude is greater than $1.0V_{ppd}$ but below $1.25V_{ppd}$, the normal discharging current (I_{QDN}) discharges the CAGCx capacitor to reduce the gain of the VGA. And if the amplitude exceeds $1.25V_{ppd}$, a fast discharging current (I_{QDF}) that is 7X the normal discharging current, quickly discharges the CAGCx capacitor until the signal level is back below $1.25V_{ppd}$. The magnitude of the normal discharging current (I_{QDN}) is set by an external resistor connected between the REXT pin and ground and is given by the following equation:

$$I_{QDN} = \frac{1.2V}{REXT} \qquad \textit{(eq. 1)}$$

where REXT ranges from 4KΩ to 12KΩ. The normal discharging current is 40X the normal charging current, resulting in an asymmetrical loop response.

A fast recovery from small input signals is provided with a '0'-to-'1' transition on the FSREC input. A fast charging current (I_{QCF}) that is 7X the normal discharging current quickly charges the CAGCx capacitor until the $1.0V_{ppd}$ signal level is reached, after which the loop resumes normal operation.

There are two AGC capacitors, the CAGCD pin capacitor which is used for the data field when SGATE = 0, and the CAGCS pin capacitor which is used for the servo field when SGATE = 1. This allows the data and servo fields to have independent discharging and charging rates. It also avoids reacquisition of gain at the beginning of the servo and data fields. When HLDN = 0 the discharging and charging currents are disabled, and the AGC action is halted to allow for servo burst measurement.

In the AGC mode, the VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. Equation (2) expresses the VGA normal mode gain (A_V), in volts/volts, as an exponential function of the control voltage on the selected CAGCx pin.

$$A_V = A_{V(max)} \bullet e^{-\left(\frac{2.8V - V_{CAGCX}}{0.53V}\right)} \qquad \textit{(eq. 2)}$$

where $A_{V(max)}$ is 56 volts/volt and V_{CAGCx} nominally ranges from1.4V to 2.8V.

When in the PGC mode (PGC = 1), the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by a voltage (V_{GC}) forced externally on the CAGCD pin. Gain control remains on the CAGCD pin independent of the state of SGATE. In PGC mode, the VGA has a linear gain versus control voltage characteristic to insure predictable control input response. Equation (3) expresses the VGA gain as a linear function of the control voltage (V_{GC}) on the CAGCD pin.

$$4A_V = 48\left[1 - \left(\frac{V_{REF} - V_{GC}}{1v}\right)\right] \qquad \textit{(eq. 3)}$$

where V_{REF} is nominally 2.4v and V_{GC} ranges from (V_{REF} – 1.0V) to V_{REF} .

For fast write to read recovery a low input impedance mode is provided. When LOWZ = 1, the gain of the VGA goes to zero, the input impedance is reduced to $1/60^{th}$ of its normal value, and

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the charge pump currents are disabled to retain the gain values set by the CAGCx capacitors. Also, a low impedance is initiated for the on-chip AC coupling capacitors between the VGA output and the filter input. Upon releasing the LOWZ mode, the on-chip coupling capacitors are held in the low impedence mode for an extra 200ns while the VGA restores its gain. This eliminates any transient offset effects that may occur while the loop is locking.

While the VM54750 is idle (STBYN =0), the VGA amplifier is powered down, and the V_{GC} input (CAGCD pin) should be held at the VREF voltage by the user.

Programmable Low Pass Filter (LPF) / Equalizer

The filter is implemented as a 7-pole 0.05 degree linear phase equiripple low pass filter with matched normal and differential outputs. The cutoff frequency and boost equalization are programmable.

The basic building block for the filter is the integrator (g_m-C) stage which consists of a transconductance amplifier driving on-chip capacitors. Figure 2 shows how g_m-C stages are connected to form a bi-quad, which realizes a second-order transfer function. The equation below is the expression for the transfer function of such a bi-quad. In Diagram 3, three of these bi-quads and a single g_m-C stage are cascaded to form a seven-pole low pass filter. In parallel with the final g_m-C stage is a nearly identical single g_m-C stage configured as a high-pass, or differentiator section. The various sections supply normal or differentiated low-pass outputs with matched group delays. The normal output goes to the AGC and servo sections. The differentiated output, along with the normal output, is used by the PDQ block to provide data and servo peak position information. Because the high-pass differentiator stage tracks the other g_m-C stages, the relative gain AO_D of the differentiated output to the normal output is nearly constant (at two-thirds the unboosted cutoff frequency) over the range of the cutoff frequency and boost level of the filter, as depicted in Graph 1.

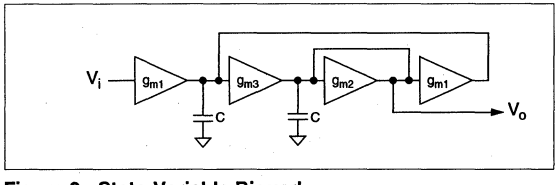


Figure 2: State-Variable Biquad

$$\frac{V_o}{V_i} = \frac{\omega_o^2}{s^2 + s(\omega_o/Q_o) + \omega_o^2} \qquad \textit{(eq. 4)}$$

where $\omega_o = \frac{\sqrt{g_{m1} \cdot g_{m2}}}{C}$ and $Q_o = \frac{\sqrt{g_{m1} \cdot g_{m3}}}{g_{m2}}$

The filter utilizes transconductor-capacitor (g_m-C) techniques to provide a cutoff frequency (f_C) that is directly proportional to g_m/C. An accurate g_m is derived from the Frequency Cutoff (Fc) DAC input current and an on-chip bandgap voltage using a feedback circuit. The parts are trimmed during wafer probe to compensate for on-chip capacitance variations.

Probe pads F1, F2, and F3 have fusible links that are used for cutoff frequency trimming during wafer test. These pads are not accessible after the part is packaged. The fusible links are between the pads and VEE1 and can be blown open by grounding the appropriate pad and pulsing a current into VEE1.

Fusible Link Truth Table

TDN15	*TUP10*	*TUP5*	$\Delta\Delta f_C$
intact	open	open	+16.0%
intact	open	intact	+10.0%
intact	intact	open	+ 5.0%
intact	intact	intact	0.0%
open	open	open	- 1.0%
open	open	intact	-5.0%
open	intact	open	-10.0%
open	intact	intact	-15.0%

Cutoff frequency is programmed by sourcing a DC current to the IFC pin in the range of 100 to 800 microamperes. Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation

$$f_c = 3.75 \bullet IFC \qquad \textit{(eq. 5)}$$

where IFC is in milliamperes.

The gain (g_m) of each g_m-C stage is established using MOSFET input devices. These devices are operated in the triode region, resulting in a transconductance of:

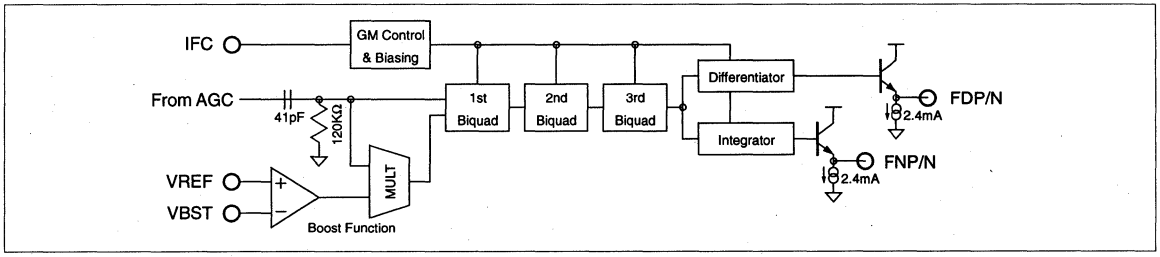


Figure 1: Filter Block Diagram

$$g_m \approx \mu \bullet C_{ox} \bullet \frac{W}{L} \bullet V_{ds} \qquad \textit{(eq. 6)}$$

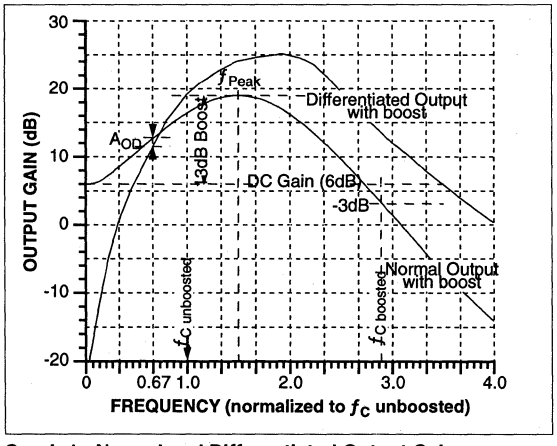
where μ is the MOSFET channel mobility, C_{ox} is the MOSFET gate oxide capacitance per unit area, W and L are the MOSFET channel width and length respectively, and V_{ds} is the MOSFET drain-to-source voltage. The magnitude of the g_m of each stage is set to the desired cutoff frequency by adjusting V_{ds}. Stage-to-stage g_m ratios determine the shape of the filter transfer function and are achieved by ratioing the MOSFET widths (W).

A filter reference current is generated using external resistors on the RXD and RXS pins and on-chip bandgap references. The current sourced by IFR depends on the state of SGATE as follows:

$$IFR = \frac{1.28V}{RXD} \quad (SGATE = 0) \qquad \textit{(eq. 7)}$$

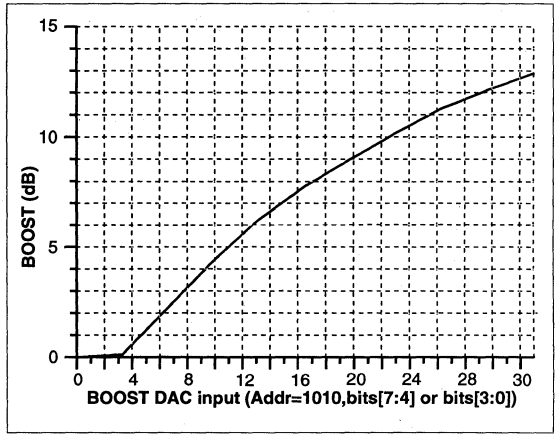
$$IFR = \frac{1.28V}{RXS} \quad (SGATE=1) \qquad \textit{(eq. 8)}$$

The amount of boost equalization depends on the output of the BOOST DAC. Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function. Graph 1 shows normalized filter response curves with maximum boost for both the normal and differentiated outputs. Graph 2 shows the nominal relationship between the BOOST control word and the resulting boost level. Notice the absence of boost when BOOST is below 4. In this region the bandwidth is being pushed out but the gain doesn't peak above the DC level.



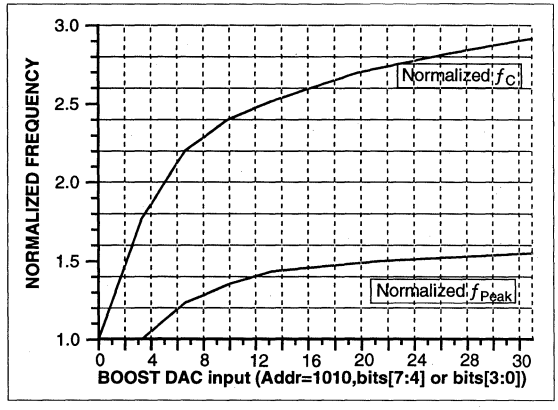
Graph 1: Normal and Differentiated Output Gains

Graph 3 shows the effect of boost on the cutoff frequency. With maximum boost the cutoff frequency is nearly triple the unboosted value. Also shown is gain peak frequency, which for maximum boost achieves a value of over 1.5. Thus, as an example, if the unboosted cutoff frequency is programmed to 30MHz, with maximum boost the peak gain of 13dB will occur at approximately 46MHz, and the net cutoff frequency will be 88MHz.



Graph 2: Ideal Boost (in dB) versus BOOST DAC input

Boost, or pulse slimming, is implemented by feeding the filter input through a variable gain stage to the normally grounded terminals of the capacitors in the first bi-quad. This yields a pair of programmable symmetric zeros on the real axis. Because the resulting transfer function has an added $K \cdot s^2$ in the numerator, the group delay is unaffected by the amount of boost.



Graph 3: Normalized f_C and f_{Peak} versus VBST

Group delay for an ideal 0.05 degree equiripple filter is flat within one percent out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a "real" filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM54750 group delay flatness is specified to be less then ±2% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 24ns at a cutoff of 30MHz. Thus at this cutoff frequency, the group delay varies by less than ±0.5ns out to 45MHz. A typical group delay is shown in Graph 4 with measurements displayed.

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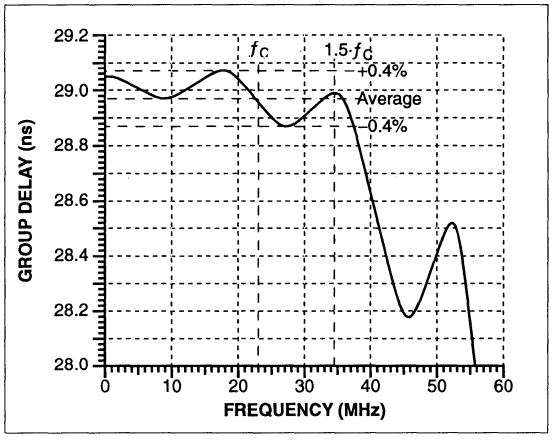


Graph 4: Typical Group Delay of AGC and Filter (with f_C = 23MHz)

The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay (T_{GD}), in nanoseconds, is expressed below as a function of the cutoff frequency

$$T_{GD} = 6ns + \frac{0.53}{f_C} \qquad (eq.\ 9)$$

where f_C is the unboosted cutoff frequency in Hz.

Because the filter is AC-coupled from the Gain Control output, a zero occurs at DC and a pole occurs at about 60KHz. This pole-zero pair distorts the frequency response of the filter below frequencies of about 1.3MHz. Test Mode 0 bypasses the Gain Control circuit and AC-coupling network, which allows direct filter measurements from the DIP/DIN pins.

The filter block also generates VREF which serves as a reference voltage for the following analog input control pins: VBST, SETLV, PKTHR, and CAGCD (if PGC asserted). This output is nominally at 2.4 volts with 2mA of source/sink drive capability. A Brokaw bandgap circuit establishes a temperature-compensated voltage which is buffered by an opamp circuit in a voltage-follower configuration. For stable operation this output should not drive more than 100pF of stray capacitance. This output is typically used as an external DAC reference voltage.

Pulse Detector and Qualifier (PDQ)

The PDQ receives filtered analog readback signals from the Read/Write Preamp and delivers qualified logic pulses to the Read Data Separator. Errors due to false peaks are detected in the PDQ and erased in the Data Separator prior to decoding of the data.

Two analog input channels are processed by the PDQ. The timing channel inputs HRP/HRN (HR) are AC coupled from the differentiated output of the filter FDP/FDN. The level qualification channel inputs LQP/LQN (LQ) are AC coupled from the normal outputs of the filter FNP/FNN.

The high resolution signal is converted to digital pulses using a zero-crossing comparator and self-resetting one-shot circuit having a nominal pulse width of 3.5ns. The timing channel clocks a D-type Flip-Flop on either positive or negative transitions of the HR input. Visibility into the timing channel signals HRCOMP and HRCLK are provided in test mode (see Test Mode description).

The HR pulses are qualified by signals which are derived from the LQ channel. Two comparators indicate when the positive (LP) and negative (LN) extents of the LQ signal exceed a certain percentage of the average peak amplitude of the LQ signal. In addition, two peak detectors qualify consecutive same polarity peaks, if the subsequent peaks are of higher amplitude and have sufficient slope. All subsequent lower amplitude peaks are ignored. The first opposite polarity peak following a valid RDATA pulse is not slope qualified. The digital logic stores the polarity of the peak and qualifies consecutive peaks based on the sensitivity level threshold V_{TH}(detect) set by the PEAK Threshold DAC. If a second peak is qualified, an RDATA pulse is generated with a coincident Erase pulse. Two comparators indicate when the positive (POSPK) and negative (NEGPK) slope detectors exceed the sensitivity level threshold.

The average peak amplitude of the LQ signal is determined by an envelope follower circuit consisting of an input buffer ($A_V = 2$), a rectifier/peak detector, and a unity gain transconductance amplifier (g_m). The buffer stage drives a precision rectifier circuit combining the differential outputs such that the most positive extent of the signal is stored (peak detected) on an internal capacitor (10pF). The storage capacitor charges quickly from its common mode value ($V_{LQ} = 0$) to approximately $V_{LQ}/2$. It's rate of discharge is set by the current I_D, related to the charge pump normal discharging current (I_{QDN}) by the expression

$$I_D = \frac{I_{QDN}}{20} \qquad (eq.\ 10)$$

The envelope follower output voltage (V_{ENVC}) on the ENVC pin 'follows' the peak detector voltage at a rate fixed by the transconductors output currents and the external capacitor ENVC. The transconductors charge and discharge currents, I_{EC} and I_{ED}, are also related to the charge pump normal discharging current (I_{QDN}) by the expressions

$$I_{EC} = 3.32 \cdot I_{QDN} \quad \text{and} \quad I_{ED} = \frac{I_{QND}}{8} \qquad (eq.\ 11)$$

The charge current is 26.6X the discharge current resulting in an asymmetric response.

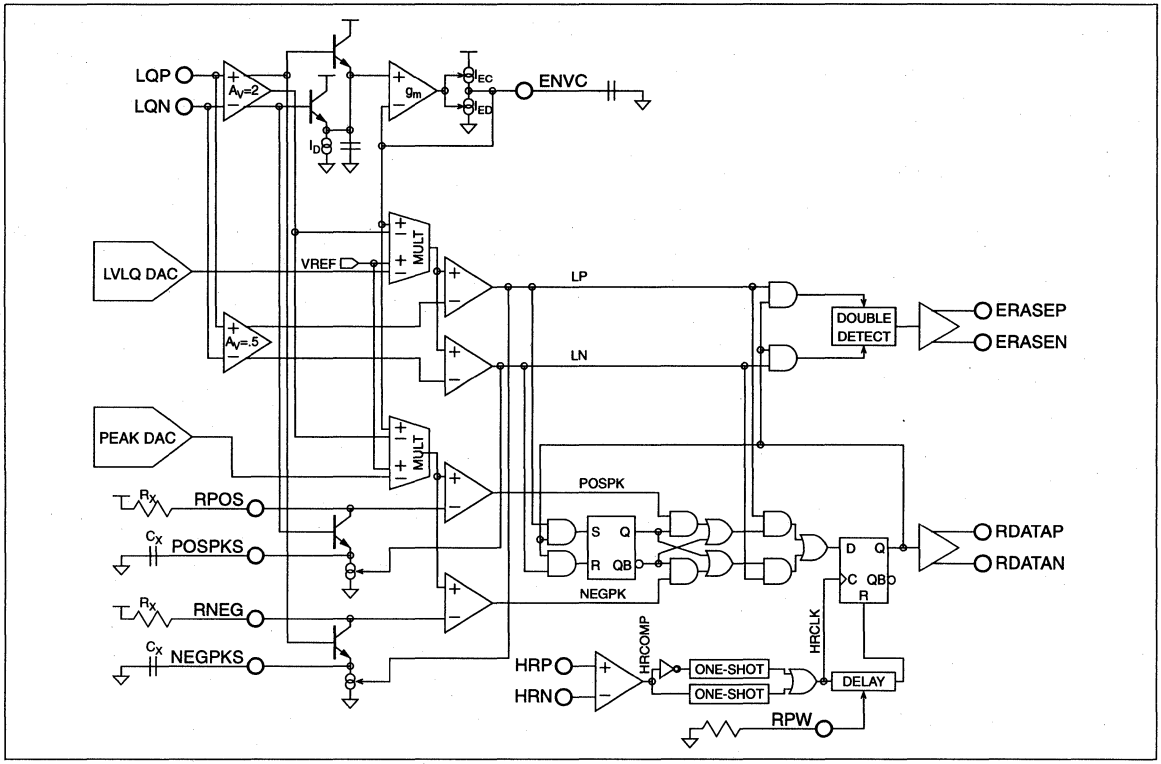
The product of the envelope follower output (V_{ENVC}), which is equal to one-half the average peak amplitude of the LQ signal, and the external DC control voltage at the SETLV pin (V_{SETLV}), generated by the analog multiplier circuit, produces a qualification level threshold (V_{TH}) that is proportional to the average peak amplitude of the LQ signal (V_{LQ}) and is given by the following equation:

$$V_{TH(LQ)}(qual) = V_{LQ} \cdot \left(\frac{V_{REF} - V_{SETLV}}{1V} \right) \qquad (eq.\ 12)$$

where V_{REF} is nominally 2.4V, and V_{SETLV} ranges from (V_{REF} – 1.1V) to V_{REF}.

In addition, the product of the envelope follower output and the external DC control voltage at the PKTHR pin (V_{PKTHR}), gener-

PULSE DETECTOR AND QUALIFEIER (PDQ) BLOCK DIAGRAM



ated by the analog multiplier circuit, produces a detection level threshold for the two peak/slope detectors that is proportional to the average peak amplitude of the LQ signal, and is given by the following equation:

$$V_{TH(PD)}(\text{detect}) = V_{LQ} \cdot \left(\frac{1V + V_{PKTHR} - V_{REF}}{1V} \right) \qquad \textit{(eq. 13)}$$

where V_{REF} is nominally 2.4V, and V_{PKTHR} ranges from (V_{REF} - 1.1V) to V_{REF}. The slope detector threshold voltage is referenced to V_{CC} and is compared against the pin voltages of RPOS and RNEG, also referenced to V_{CC}. If the most negative extent of either V_{RPOS} or V_{RNEG} exceeds the sensitivity level threshold, comparator outputs POSPK or NEGPK produce a logical '1'. Qualified consecutive same polarity higher amplitude peaks produce both ERASE and RDATA pulses.

The signal voltages on the RPOS and RNEG pins depend on the external components selected. The RC time constant (Rx·Cx) and the LQ signal frequency (f_{LQ}) are both proportional to the magnitude of the voltage (V_{Rx}) across the Rx resistors. The expression for V_{Rx} can be written as

$$V_{Rx} = Rx \cdot Cx \cdot \frac{dV_{LQ}}{dt} \qquad \textit{(eq. 14)}$$
$$= Rx \cdot Cx \cdot 1.0V \cdot \pi \cdot f_{LQ} \cdot \sin(2 \cdot \pi \cdot f_{LQ} \cdot t)$$

where $V_{LQ} = 0.5V \cdot \sin(2 \cdot \pi \cdot f_{LQ} \cdot t)$. And thus the maximum peak voltage across RPOS and RNEG is

$$V_{Rx}(\max) = Rx \cdot Cx \cdot 1.0V \cdot \pi \cdot f_{LQ} \qquad \textit{(eq. 15)}$$

V_{Rx}(max) is frequency dependent, and hence Rx, Cx, and the slope detector sensitivity level (V_{TH}) must be chosen carefully over the frequency range of interest. For normal operation, $V_{Rx}(\max) \geq V_{TH}$ at the minimum signal frequency. The recommended resistance value ranges from 50Ω to 500Ω for Rx, and the capacitance value ranges from 20pF to 200pF for Cx. VTC also recommends using a low threshold of 5% to 30% (high sensitivity). The values chosen should be optimized for system requirements.

The qualified RDATA pulses have provision for external control of the pulse width via an external resistor connected to the RPW pin. The pulse width (PW_{RDATA}) ranges from 3ns to 18ns and is expressed as a function of RPW by the following

$$PW_{RDATA} = 0.5ns/K\Omega \cdot RPW + 1.8ns \qquad \textit{(eq. 16)}$$

where RPW is given in KΩ and ranges from 4KΩ to 32KΩ.

Servo Demodulator

The servo demodulator supports full quadrature demodulation through the use of an array of four peak detector channels. A block diagram for the servo demodulator is shown on the following page. The filtered servo bursts are AC coupled into the chip

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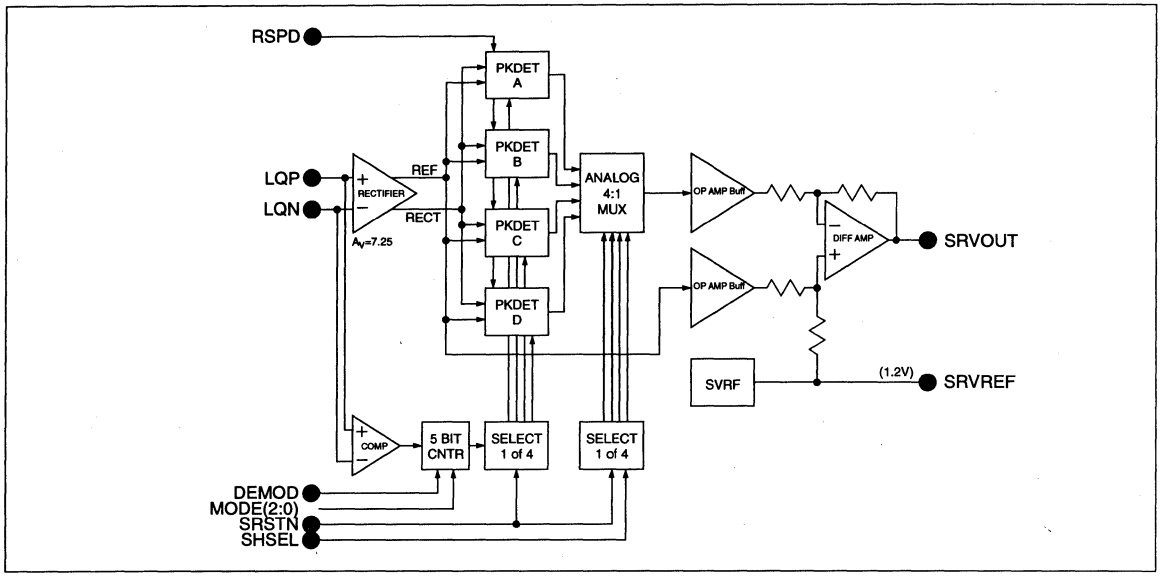
SERVO DEMODULATOR BLOCK DIAGRAM



through the LQP and LQN inputs. The signal is amplified immediately to maximize the signal amplitude and reduce mismatch effects introduced by subsequent blocks. The amplified signal is full wave rectified and input to an array of four peak detectors. The peak detector consists of an emitter follower and on-chip hold capacitor. Each peak detector is selectively enabled and detects the peak voltage amplitude of the servo burst. After the peak has been detected, the peak detector is disabled and 'holds' the peak voltage for subsequent processing. A 4:1 analog switch allows each peak detector output to be multiplexed to the servo output. The multiplexed peak detector output and its corresponding reference are buffered before feeding into a difference amplifier. The difference amplifier output is the SRVOUT output pin and is referenced to the SRVREF pin (typically 1.2V).

The peak detectors capture the servo burst information under the control of the DEMOD input signal. Both synchronous and asynchronous modes of operation are supported. In asynchronous mode (MODE = 000_b), on the leading (rising) edge of the DEMOD input pin, the peak detectors are enabled and begin tracking the servo signal asynchronously. Likewise, on the falling edge, the peak detectors are disabled and asynchronously stop tracking the servo signal. In synchronous mode (MODE $\neq 000_b$), the leading (rising) edge of the DEMOD input pin is synchronized to an internal clock. The clock is generated by a comparator that detects the high to low zero crossings of the input waveform to the peak detector. The comparator has 60mV of input hysteresis which removes low amplitude noise and yields cleaner clock transitions. The synchronized DEMOD signal causes the peak detectors to sample the input waveform synchronously with the incoming waveform to reduce any charge injection nonlinearity. The MODE[2:0] word (Addr = 1011, bits[7:5]) selects the number of cycles counted by a 5-bit counter. Note that the full wave rectifier causes both halves of a cycle to be peak detected. The definition of the decoding of the MODE[2:0] word is shown in the normal mode register decode table.

Normal Mode Pin Decode and RSPD Resistor Selection

MODE[2:0] word			*MODE*	*NORMAL DEFINITION*	*SERVO INPUT FREQUENCY*	
2	*1*	*0*			*4MHz*	*10MHz*
0	0	0	0	async mode		
0	0	1	1	4 cycles	4kΩ	1.5kΩ
0	1	0	2	8 cycles		
0	1	1	3	12 cycles		
1	0	0	4	16 cycles		
1	0	1	5	20 cycles		
1	1	0	6	24 cycles		
1	1	1	7	28 cycles	300kΩ	20kΩ

If the proper number of cycles have not arrived when the trailing edge of the DEMOD input pin occurs, then the peak detectors asynchronously progresses to a hold mode as a fail safe feature.

Consecutive cycles of the DEMOD pin cause the A, B, C, and D peak detectors to sample the input waveform. The SHSEL input pin is provided to select the various peak detector outputs. The rising edge of SHSEL causes the selection to change to the A peak detector, the second pulse selects B, etc. The servo demodulator control logic and all peak detectors are reset by a low level on the SRSTN input pin. Upon the low level of SRSTN, the SRVOUT pin is reset to the SRVREF voltage. The servo blocks may also be reset automatically by an internal one-shot. The one-shot initiates a reset pulse of ~500ns when SGATE = 1 and STBYN = 0. This automatic reset feature is useful when going back and forth between servo tracking and standby mode.

The RSPD pin gives the user some control of the peak detector bandwidth. A resistor is placed between the RSPD pin and the VCC1 supply. This resistor ties to the collector of each emitter follower in the peak detector. This is shown in Figure 3.

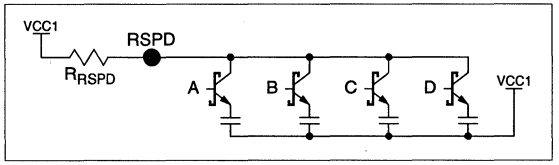


Figure 3: Peak Detector Bandwidth Control Circuitry

When a rising edge comes into the peak detector, the emitter follower charges the capacitor. The charging current flows through the collector and a voltage drop is seen across R_{RSPD}. If $Ic \cdot R_{RSPD}$ becomes large enough, the emitter follower will saturate thus limiting further charging of the capacitor. As R_{RSPD} is increased, the effective bandwidth of the peak detector is reduced and lessens the sensitivity to incoming noise spikes in the servo waveform.

$$\text{BandWidth} \propto \frac{1}{\text{RSPD}} \qquad \textit{(eq. 17)}$$

The RSPD Resistor Selection Table gives some typical values for RSPD as a function of servo frequency and the number of cycles used for demodulation. These RSPD values are the maximum resistance that may be used and still guarantee that the demodulated signal will reach 99.75% of the final value, given that servo frequency and number of demodulation cycles.

TEST MODES

There are eight test modes that are used in the VM54750 and they are defined in the following paragraphs.

Test Mode Summary:

All test modes are activated by a low level on the HLDN pin, and a high level on the PGC and SRSTN pins. Once this state has been detected, the value on the MODE(2:0) pins will be captured and decoded. Then the corresponding test mode will be activated. The test mode will continue to be active until the SRSTN pin has been detected at a low level. For the most part, test modes act upon the output of the RDATAP/N and ERASEP/N digital output driver pins with the exception on test modes 4 and 5. The test mode which is activated will be selected by the MODE(2:0) pins, as shown in the Test Mode Register Decode Table.

Test Mode Register Decode Table

MODE BITS			*MODE*	*OUTPUT PINS*			
2	*1*	*0*		*RDATAP*	*RDATAN*	*ERASEP*	*ERASEN*
0	0	0	0	LP	LN	POSEN	HRCLK
0	0	1	1	POSPK	NEGPK	SCNDPK	HRCOMP
0	1	0	2	SHSEL	DEMOD	LOWZ	FSREC
0	1	1	3	ZCCLK	DEMODOUT	RST	SRV1S
1	X	X	X	tristate	tristate	tristate	tristate

Test Mode 0 [MODE = 000_b]:

The goal of this test mode is to provide observability of internal signals of the PDQ section. In this test mode the following features are enabled:

- The positive level comparator (*LP*) is connected to the RDATAP pin
- The negative level comparator (*LN*) is connected to the RDATAN pin
- The pulse polarity indicator (*POSEN*) is connected to the ERASEP pin
- The high resolution dual one-shot (*HRCLK*) is connected to the ERASEN pin

Test Mode 1 [MODE = 001_b]:

The goal of this test mode is to provide observability of internal signals of the PDQ section. In this test mode the following features are enabled:

- The positive peak comparator (*POSPK*) is connected to the RDATAP pin
- The negative peak comparator (*NEGPK*) is connected to the RDATAN pin
- The second peak indicator (*SCNDPK*) is connected to the ERASEP pin
- The high resolution comparator (*HRCOMP*) is connected to the ERASEN pin

Test Mode 2 [MODE = 010_b]:

The goal of this test mode is to allow as many digital pin connections as possible to verify in a bed of nails environment. (This technique is referred to as "IO Mapping".) In this test mode the following features are enabled:

- The SHSEL input pin is connected to the RDATAP pin
- The DEMOD input pin is connected to the RDATAN pin
- The LOWZ input pin is connected to the ERASEP pin
- The FSREC input pin is connected to the ERASEN pin

Test Mode 3 [MODE = 011_b]:

The goal of this test mode is to provide observability of internal signals of the demodulator section. In this test mode the following features are enabled:

- The internal signal *ZCCLK* is connected to the RDATAP pin. The *ZCCLK* signal is the output of the servo zero cross comparator and drives the internal synchronous counter. By forcing the LQP/N inputs and observing the *ZCCLK* output signal, the hysteresis of the comparator can be measured.

- The internal signal *DEMODOUT* is connected to the RDATAN pin. The *DEMODOUT* signal is an internal synchronized version of the DEMOD input. When DEMOD goes HI, the *DEMODOUT* signal goes HI two LQP/N cycles later and remains HI for the appropriate number of cycles as programmed by the MODE word. The *DEMODOUT* signal allows testing of the SRVSYNC 5 bit counter.
- The internal signal *RST* is connected to the ERASEP pin. This is an internal reset for the SRVSYNC 5 bit counter and simply an inverted version of *DEMODOUT*.
- The internal signal *SRV1S* is connected to the ERASEN pin. The *SRV1S* is a one-shot reset pulse for the servo peak detectors. The one-shot pulse width is determined by an on-chip RC time constant. This pulse is generated when the VM54840 is in servo mode and then comes out of standby mode, i.e. SGATE is HI and STBYN going from LOW to HI. This condition can occur when the drive is in an idle mode. The chip is basically asleep but periodically wakes up to demodulate the servo information and make sure the head is on the center of the track.

Test Mode 4 [MODE = 100_b]:
The goal of this test mode is to isolate the filter block. The DIP/DIN inputs are multiplexed directly into the filter. The AGC output has no effect on the filter in this mode. This allows the filter block to be tested individually. The internal filter tuning voltage is also multiplexed out on the VREF pin. The RDATAP/N and ERASEP/N outputs are tristated for the purposes of a bed of nails PCB testing.

Test Mode 5 [MODE = 101_b]:
The goal of this test mode is to provide observability for the internal nodes of the VGA. The VGA outputs (*DOP* and *DON*) are connected to the FNP/N pins. The filter inputs (*FIP* and *FIN* which are after the AC coupling capacitors) are connected to the FDP/N pins. The RDATAP/N and ERASEP/N outputs are tristated for the purposes of a bed of nails PCB testing.

Test Mode 6 [MODE = 110_b]:
The goal of this test mode is to provide a variable current to the charge pump output. The charge pump discharging current (I_{QDN}) in this mode is equal to $0.25 \cdot Fc_{DAC}$. The RDATAP/N and ERASEP/N outputs are tristated for the purposes of a bed of nails PCB testing.

Test Mode 7 [MODE = 111_b]:
The RDATAP/N and ERASEP/N outputs are tristated for the purposes of a bed of nails PCB testing.

COMPONENT PINS

There are a number of different input and output buffers used on this chip. There are CMOS TTL inputs, Bipolar ECL-like differential outputs, Analog differential inputs, and several analog reference input and output pins. Because of pin limitations some pins serve double duty.

POWER SUPPLY PINS:

PIN NAME	PIN NO.	DESCRIPTION
VCC	11	Digital CMOS Power
VCC1	3	Analog Power
VCC2	24	Digital Bipolar Power

GROUND SUPPLIES PINS:

PIN NAME	PIN NO.	DESCRIPTION
VEE	19	Digital Ground
VEE1	38	Analog Ground
VEE2	51	Substrate Ground

CMOS TTL INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
PGC	6	PGC mode control (active high)
FSREC (active High)	7	Fast Recovery mode control
SGATE	8	Servo mode control (active High)
LOWZ (active High)	9	Low Impedance mode control
HLDN Low)	10	AGC Hold mode control (active
SRSTN	12	Servo Reset (active Low)
SHSEL	13	Servo Peak Detector select
DEMOD	14	Demodulation Clock
STBYN Low)	15	Standby mode control (active
MODE (2:0)	16-18	Mode control bits (3)

EXTERNAL PINS:

PIN NAME	PIN NO.	DESCRIPTION
RPW	25	RDATA Pulse Width control, Resistor (4KΩ to 32KΩ) to Ground [see equation (14)]
RNEG	31	Negative Slope Detector Gain control, Resistor (50Ω to 500Ω) to VCC [see equation (13)]
RPOS	32	Positive Slope Detector Gain control, Resistor (50Ω to 500Ω) to VCC [see equation (13)]
RSPD	37	Servo Peak Detector Charge limit, Resistor (0 to 5KΩ) to VCC [see equation (15)]
RXS	45	Servo Frequency Range Control, Resistor (3.8kΩ to 14.1kΩ) to Ground [see equation (8)]

RXD 46 Data Frequency Range Control, Resistor (3.8kΩ to 14.1kΩ) to Ground [see equation (7)]

REXT 52 Reference current for the control DACs Resistor (6K) to Ground [see equation (1)]

CAGCD 1 AGC Data Field Gain storage, Capacitor (390pF) to Ground

CAGCS 2 AGC Servo Field Gain storage, Capacitor (390pF) to Ground

NEGPKS 30 Negative Peak Voltage Level storage, Capacitor (20pF to 200pF) to Ground [see equation (13)]

POSPKS 33 Positive Peak Voltage Level storage, Capacitor (20pF to 200pF) to Ground [see equation (13)]

ENVC 34 Envelope Tracking Rate control, Capacitor (1200pF) to Ground

ANALOG DIFFERENTIAL INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
HRP ***HRN***	28-29	High Resolution Comparator
LQP ***LQN***	35-36	Level Qualifier
DIP ***DIN***	49-50	Read Data Input

BIPOLAR ECL-LIKE DIFFERENTIAL OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
RDATAN ***RDATAP***	22-23	Pulse Detector Data Output
ERASEN ***ERASEP***	20-21	Pulse Detector Erase Flag
FDN ***FDP***	42-43	Filter Differentiated Output
FNN ***FNP***	40-41	Filter Normal Output

ANALOG OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
SRVREF	4	Servo Reference Voltage.
SRVOUT output	5	Selected sample & hold amplifier
VREF	39	Control Referenece Voltage
IFR	44	Filter Tuning Reference Current

CONTROL VOLTAGE OR CURRENT INPUTS PINS:

PIN NAME	PIN NO.	DESCRIPTION
PKTHR voltage	26	Peak threshold sensitivty control
SETLV voltage	27	Detection threshold control
IFC current	47	Filter controlfrequency control
VBST	48	Filter boost control voltage

CIRCUITS

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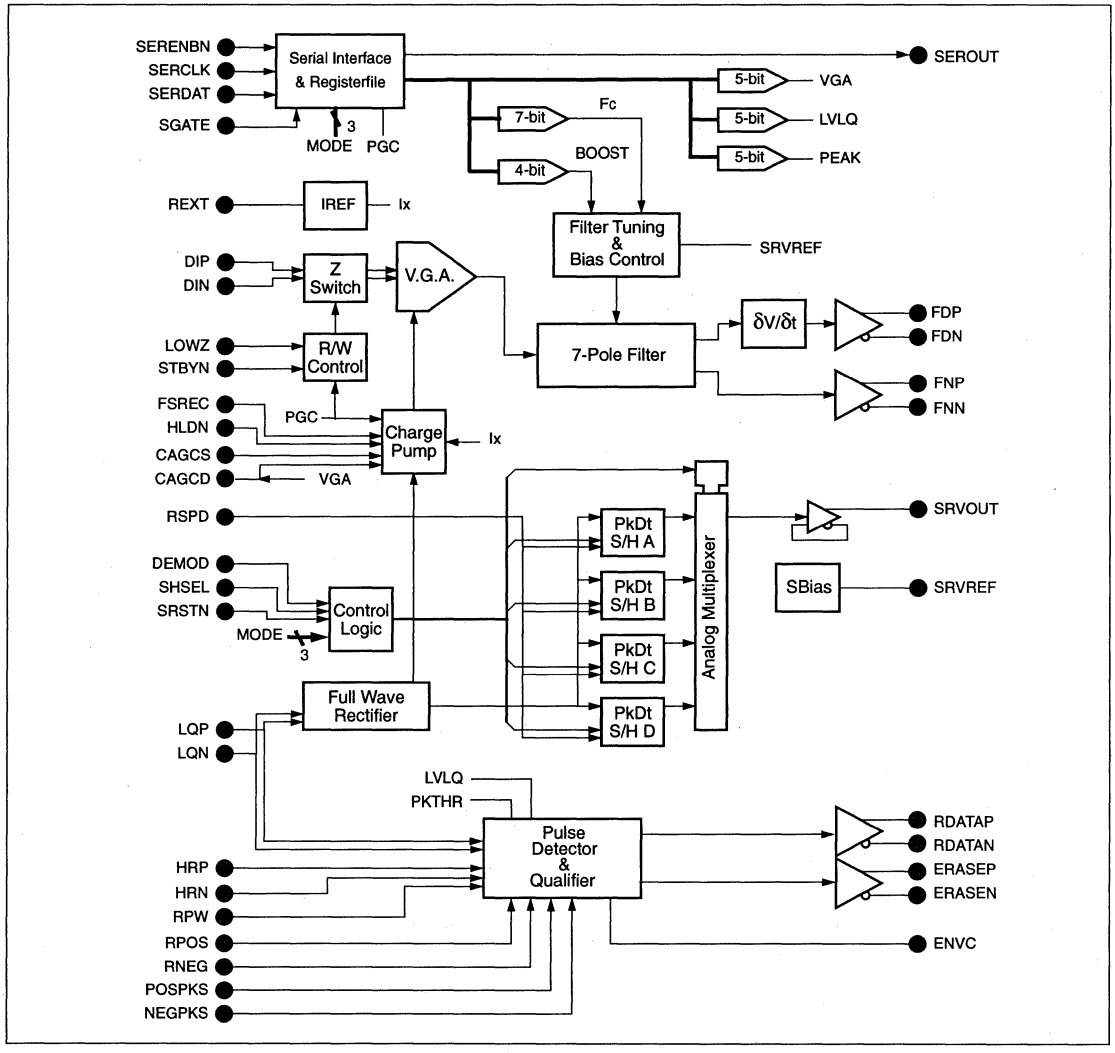

Figure 4: VM54750 Top-Level Schematic / Logic Blocks

AC AND DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified $0°C < T_A < 70°C$, $4.5V < V_{CC} < 5.5V$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode, Data Rate = 24Mbps			<TBD>	mA
		Read Mode, Data Rate = 75 Mbps		150	200	mA
		Standby Mode			<TBD>	mA
Recovery time Standby to fully functional	T_{REC}	AGC within 10% final value, Pulse Detector w/o pulse pairing, Filter cutoff within 10% final value			10	µs

LOGICAL SIGNALS: ALL DIGITAL PINS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input High Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input Leakage Current	I_{IL}	$V_{IL} = 0.8V$			±10	µA
	I_{IH}	$V_{IH} = 2.0V$			±10	µA
Control Signal rise and fall times	T_{CS}				100	ns
Input Capacitance	C_{IN}				10	pF

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GAIN CONTROL

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Common for both AGC and PGC modes						
Input dynamic range	V_{DI}	$V_{DI} = (V_{DIP} - V_{DIN})$ [THD_S applies for 250 to 320mV_{ppd}]	24		320	mV_{ppd}
Input common mode voltage	V_{CMDI}	$V_{CMDI} = (V_{DIP} + V_{DIN})/2$	V_{CC}–3.1	Vcc-2.7	V_{CC}–2.3	V
Differential input resistance	$R_{in(DA)}$	LOWZ = Low	3.0	6.0	9.0	KΩ
		LOWZ = High	50	100	150	Ω
Single ended input impedance	$R_{in(SA)}$	LOWZ = Low	1.5	3.0	4.5	KΩ
		LOWZ = High	25	50	75	Ω
Output common mode voltage	V_{CMFN}	$V_{CMFN} = (V_{FNP} + V_{FNN})/2$ Test Mode 5	V_{CC}–3.4	Vcc-3.0	V_{CC}–2.6	V
Output common mode voltage	V_{CMFD}	$V_{CMFD} = (V_{FDP} + V_{FDN})/2$ Test Mode 5	Vcc-3.0	Vcc-2.6	Vcc-2.2	V
Output offset voltage	V_{OS}	for V_{FN}, over entire gain range, Test Mode 5	–200		200	mV
Output distortion of V_{FN}	THD	$V_{DI} = 250mV_{ppd}$, $V_{FN} \leq 1.1V_{ppd}$, Test Mode 5, 1st, 2nd, and 3rd harmonics only			1.0	%
RX pin voltage	V_{RX}	R_{ext} = 6KΩ<TBD>	1.05	1.2	1.35	V
Only for AGC mode (PGC=Low)						
Output dynamic range	V_{FN}	$V_{FN} = (V_{FNP}-V_{FNN})$ $24mV_{ppd} \leq V_{DI} \leq 250mV_{ppd}$ $4MHz < f_{in} < 30MHz$	0.9		1.1	V_{ppd}
AGC minimum Gain	AV_{min}	$AV=V_{FN}/V_{DI}$ V_{CAGCD}=0.8v, Test Mode 5, [0]			4.0	V/V
AGC maximum Gain	AV_{max}	$AV=V_{FN}/V_{DI}$ V_{CAGCD}=3.2v, Test Mode 5, [0]	38	50		V/V
Gain settle from –30% V_{DI} step	T_{GD}	$V_{FN} \geq 0.9 \cdot$(final value)		31	TBD	µs
Gain settle from +30% V_{DI} step	T_{GA}	$V_{FN} \leq 1.1 \cdot$(final value)			2.0	µs
Charge Pump Normal Discharging current	I_{QDN}	$0.55v \leq V_{LQ} \leq 0.56v$ (static), R_{ext} = 6KΩ	170	200	230	µA
Charge Pump Fast Discharging current	I_{QDF}	$V_{LQ} \geq 0.70v$ (static)	$6.8 \cdot I_{QDN}$		$7.5 \cdot I_{QDN}$	µA
Charge Pump Normal Charging current	I_{QCN}	$V_{LQ} \leq 0.40v$ (static)	$I_{QDN} \div 44$		$I_{QDN} \div 36$	µA
Charge Pump Fast Charging current	I_{QCF}	$V_{LQ} \leq 0.40v$ (static), FSREC Low to High edge triggered	$6.8 \cdot I_{QDN}$		$7.5 \cdot I_{QDN}$	µA
Charge Pump Leakage current	I_{LK}	HLDN = Low	–10		10	nA
Only for PGC mode (PGC=High)						
PGC minimum Gain	AV_{min}	$AV=V_{FN}/V_{DI}$ VGA_{DAC}=0h, Test Mode 5,			4.0	V/V

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
PGC maximum Gain	AV_{max}	$AV=V_{FN}/V_{DI}$ VGA_{DAC}=1Fh, Test Mode 5,	38	50	56	V/V
Gain Control Input Current (CAGCD Input)	I_{GC}	V_{CAGCD} = VREF			±10	µA
[0] Linearity of 0.5% from 1/8 to 7/8 of 550 mV_{ppd} required.						

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Common for both AGC and PGC modes						
Special Distortion	THD_S	250 mV ≤ V_{DI} ≤ 320 mV, V_{FN} ≤ 1.1V_{ppd} , Test Mode 5			4	%
Differential input capacitance	$C_{in(DA)}$				10	pF
Input referred noise voltage	V_{IRN}	gain =AV_{max}, BW = 15MHz V_{DIP} = V_{DIN}			10	nV/√Hz
Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common mode rejection ratio	$CMRR_G$	gain = AV_{max}, f_{in} = 5MHz, V_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_G$	gain = AV_{max}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB
Only for AGC mode (PGC=Low)						
AGC Gain Sensitivity to CAGCx voltage	AV_{PV}	(Typical range is 1.4v to 2.8v)		17.5		dB/V
Only for PGC mode (PGC=High)						
Settling time to step change in VGA_{DAC}	T_{PGS}	zero to full scale after completion of the write cycle (SERENBN ↑)			300	ns

LOW PASS FILTER (7-POLE, 0.05°, EQUIRIPPLE PHASE)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Filter cutoff frequency (low end)	f_{Cmin}	Fc_{DAC}=00h , REXT=6KΩ	2.50	3.75	4.50	MHz
Filter cutoff frequency (middle)	f_{Cmid}	Fc_{DAC}=40h , REXT=6KΩ	15.9	16.9	17.8	MHz
Filter cutoff frequency (high end)	f_{Cmax}	Fc_{DAC}=7Fh , REXT=6KΩ	28.5	30	31.5	MHz
Normal lowpass gain (V_{FN} vs. V_{DI})	AO_N	no boost, Fc_{DAC}=00h , REXT=6KΩ, f_{in} = 4MHz, Test Mode 4	-1.0	0	1.0	dB
Differentiated lowpass gain (V_{FD} vs. V_{FN}))	AO_D	no boost, f_{in} = 0.67f_C, Test Mode 4	AO_N–5.0	AO_N–3.5	AO_N-2.3	dB
Filter Boost (low end)	AB_{min}	$BOOST_{DAC}$=0h , REXT=6KΩ		0	0.5	dB
Filter Boost (high end)	AB_{max}	$BOOST_{DAC}$=Fh , REXT=6KΩ	11.5	13.0	16.0	dB
Normal filter output offset	V_{OSFN}	V_{DI} = 0.0v, Test Mode 4	–200		200	mV
Differentiated filter output offset	V_{OSFD}	V_{DI} = 0.0v, Test Mode 4	–200		200	mV

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PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Total harmonic distortion (V_{FN} or V_{FD} vs. V_{DI})	THD_F	$f_{in} = 0.67f_C$, Fc_{DAC}=7Fh , REXT = 6KΩ, $V_{DI} \leq 1.5V_{ppd}$, Test Mode 4, 1st, 2nd, and 3rd harmonics only			1.5	%
Filter Input common mode level (V_{DI})	F_{ICM}	Test Mode 4	Vcc-3.1	Vcc-2.7	Vcc-2.3	V
Phase shift from FNP-N to FDP-N (upper)	PS_{FU}	$f_{in} = 0.67f_C$, $f_C \geq$ 20MHz	85	90	95	degree
Phase shift from FNP-N to FDP-N (lower)	PS_{FL}	$f_{in} = 0.67f_C$ $f_C <$ 20MHz	87	90	93	degree
IFC Pin Compliance Voltage Range	V_{FC}	100µA ≤ IFC < 800µA	0.7		2.3	V
Normal Lowpass Gain (V_{FN} vs. V_{FN})	AO_n	No boost, IFC = 800µA, f_C = 4MHz, test mode 4	-1.0		1.0	δβ
Differentiated lowpass gain (V_{FD} vs. V_{FN}))	AO_D	no boost, $f_{in} = 0.67f_C$, Test Mode 4	AO_N–5.0	AO_N–3.5	AO_N-2.3	dB
VBST pin input current limit	I_{BST}	$V_{BST} = V_{REF}$			±10	µA
Filter Boost (low end)	AB_{min}	$V_{BST} = V_{REF}$		0	0.5	dB
Filter Boost (high end)	AB_{max}	$V_{BST} = V_{REF} - 1.0V$	11.5	13.0	16.0	dB
Normal filter output offset	V_{OSFN}	V_{DI} = 0.0V or Open, Test Mode 4	–200		200	mV
Differentiated filter output offset	V_{OSFD}	V_{DI} = 0.0V or Open, Test Mode 4	–200		200	mV
Total harmonic distortion (V_{FN} or V_{FD} vs. V_{DI})	THD_F	$f_{in} = 0.67f_C$, IFC=800µA $V_{DI} \leq 1.5V_{ppd}$, Test Mode 4, 1st, 2nd, and 3rd harmonics only			1.5	%
Filter Input common mode level (V_{DI})	F_{ICM}	Test Mode 4	Vcc-3.1	Vcc-2.7	Vcc-2.3	V
Phase shift from FNP-N to FDP-N (upper)	PS_{FU}	$f_{in} = 0.67f_C$, $f_C \geq$ 20MHz	85	90	95	degree
Phase shift from FNP-N to FDP-N (lower)	PS_{FL}	$f_{in} = 0.67f_C$ $f_C <$ 20MHz	87	90	93	degree
Normal/Diff common mode voltage	V_{CMFx}	Normal Output Differential Output	$V_{CC} - 2.6$ $V_{CC} - 3.0$	V_{CC}–2.2 V_{CC}–2.6	$V_{CC} - 1.8$ $V_{CC} - 2.2$	V
Normal/Diff output resistance	R_{OFx}	ΔV/ΔI = +/-1mA			60	Ω
Normal/Diff output sink current	I_{SFx}	V_{CMFX} + 1V	1.75			mA
Group Delay	T_{GD}	IFC = 800µA	17	24	31	ns
Group delay variation (normal or differential)	T_{GD1}	$0.1f_C \leq f_{in} \leq 1.5f_C$, 10MHz ≤ f_C ≤ 28MHz, $V_{DI} = 1.0V_{ppd}$, V_{BST}=V_{REF}, Test Mode 4	–2.0		2.0	%
	T_{GD2}	$0.1f_C \leq f_{in} \leq 1.5f_C$, 10MHz ≤ f_C ≤ 28MHz, $V_{DI} = 1.0V_{ppd}$, V_{BST}=V_{REF}–1v, Test Mode 4	–2.5		2.5	%

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
For Reference Sources and Gain Control Inputs						
Reference Voltage at RXD & RXS	V_{RXx}	3.8 KΩ ≤ RXD or RXS ≤ 14.1 KΩ	1.216	1.28	1.344	V
Bias Current Output on IFR pin	I_{FR}	RXD (or RXS) = 3.8KΩ	303	337	371	µA
		RXD (or RXS) = 14.1KΩ	80	89	98	µA
Bias Current Leakage on IFR pin	I_{lk}	RXD =3.8KΩ, RXS=, SGATE=5V	-10		10	µA
		RXS =3.8KΩ, RXD=, SGATE=0V	-10		10	µA
IFR pin output compliance	V_{IFR}		0.7		1.6	V
Bias Voltage Output of VREF pin	V_{REF}	$-2mA \leq I_{REF} \leq 2mA$, $C_L \leq 100pF$	2.28	2.40	2.52	V

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Normal output noise voltage	V_{NN}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			TBD	mV_{rms}
Differentiated output noise voltage	V_{ND}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			9.0	mV_{rms}
Common mode rejection ratio	$CMRR_F$	f_{in} = 5MHz, IFC=800µA $V_{DIP} = V_{DIN} = 100mV_{pp}$	40			dB
Power supply rejection ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or $\Delta V_{EE} = 100mV_{pp}$	40			dB
Filter settle from step in I_{FC} and V_{BST}	T_{FS}	I_{FC} or V_{BST} step to V_{FN} settle			300	ns
Group delay variation (normal or differential)	T_{GD3}	$2.3MHz \leq f_{in} \leq 1.5f_C$, $6MHz \leq f_C \leq 28MHz$, $V_{DI} = 250mV_{ppd}$, $V_{BST}=V_{REF}-1v$,	–3.6		3.6	ns
	T_{GD4}	$1.3MHz \leq f_{in} \leq 1.5f_C$, $6MHz \leq f_C \leq 28MHz$, $V_{DI} = 250mV_{ppd}$, $V_{BST}=V_{REF}-1v$,	–5.25		5.25	ns
[1] RXx = 8KΩ, boost level is 8.8dB.						
For Reference Sources and Gain Control Inputs						
SGATE to IFR stable delay	T_{FR}	SGATE to IFR settled (10%) RXD =2KΩ, RXS =6KΩ, RIFR =3KΩ to GND.			200	ns

PULSE QUALIFIER (PDQ)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input dynamic range	V_{LQ}	$V_{LQ} = (V_{LQP} - V_{LQN})$	0.5		1.5	V_{ppd}
Input common mode voltage	V_{CMLQ}	$V_{CMLQ} = (V_{LQP} + V_{LQN})/2$	V_{CC}–2.6	V_{CC}–2.2	V_{CC}–1.8	V
LQP/N differential input resistance	R_{LQ}		3.0		9.0	KΩ
HRP/N differential input resistance	R_{HR}		6.0		12.0	KΩ

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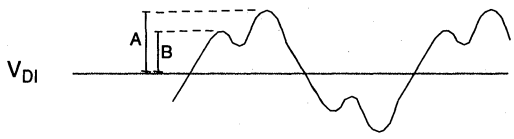
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
ENVC Common Mode Voltage	V_{ENV0}	V_{LQ} = 0.0v or Open	V_{CC} – 2.5	V_{CC}–2.1	V_{CC} – 1.7	V
Envelope follower offset [2]	N_{EO}	V_{ENVP} for V_{LQ}=+0.25v and V_{ENVN} for V_{LQ}=–0.25v	–3.0		3.0	%
Envelope follower gain	A_{ENV}	$\Delta N_{EO} / \Delta V_{LQ}$, where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
Envelope follower charging current	I_{EC}	$V_{ENV} = V_{ENV0} - 0.5v$ V_{LQ} = 0.0v, R_{EXT}=6KΩ	560	700	840	µA
Envelope follower discharging current	I_{ED}	$V_{ENV} = V_{ENV0} + 0.5v$ V_{LQ} = 0.0v, R_{EXT}=6KΩ	24	30	36	µA
Envelope follower current tracking	N_{EI}	Variation of I_{EH} to I_{EL} ratio, $[(I_{EC}/I_{ED})(25/660)–1]\cdot100$	–15		15	%
POSPKS detector gain	A_{PDP}	$\Delta V_{POSPKS} / \Delta V_{LQ}$, @ 4 and 28MHz where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
NEGPKS detector gain	A_{PDN}	$\Delta V_{NEGPKS} / \Delta V_{LQ}$, @ 4 and 28MHz where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
xPKS Common Mode Voltage	V_{CMxPKS}	V_{LQ} = 0v	V_{CC} –4.0	V_{CC}–3.5	V_{CC} – 3.0	V
POSPKS leakage current	I_{PL}	$V_{SETLV} = V_{REF} - 0.3v$, V_{LQ} = 0.0v, $V_{POSPKS} = V_{CMPPKS} + 0.5v$	–1		1	µA
NEGPKS leakage current	I_{NL}	$V_{SETLV} = V_{REF} - 0.3v$, V_{LQ} = 0.0v, $V_{NEGPKS} = V_{CMNPKS} + 0.5v$	–1		1	µA
POSPKS discharge current	I_{PD}	$V_{SETLV} = V_{REF} - 0.3v$, V_{LQ} = -0.5v, $V_{POSPKS} = V_{CMPPKS} + 0.5v$	10		14	mA
NEGPKS discharge current	I_{ND}	$V_{SETLV} = V_{REF} - 0.3v$, V_{LQ} = +0.5v, $V_{NEGPKS} = V_{CMNPKS} + 0.5v$	10		14	mA
Input dynamic range	V_{HR}	$V_{HR} = (V_{HRP} - V_{HRN})$	0.2		1.5	V_{ppd}
Input common mode voltage	V_{CMHR}	$V_{CMHR} = (V_{HRP} + V_{HRN})/2$	V_{CC}–3.0	V_{CC}–2.6	V_{CC}–2.2	V
LQP,N/HRP,N input frequency range	$f\Delta_{HR}$ $f\Delta_{LQ}$		2.3		30	MHz
LQP,N/HRP,N input Capacitance	$f\Delta_{HR}$ $f\Delta_{LQ}$				10	pf
Level Qual Threshold F_{LQ}= 4 and 28MHz	TH_{LQ}	0.5v ≤ V_{LQ} ≤ 1.5v, (30%) $V_{SETLV} = V_{REF} - 0.3v$	20		40	%
		0.5v ≤ V_{LQ} ≤ 1.5v, (50%) $V_{SETLV} = V_{REF} - 0.5v$	40		60	%
		0.5v ≤ V_{LQ} ≤ 1.5v, (80%) $V_{SETLV} = V_{REF} - 0.8v$	65		95	%
Peak Detect Threshold F_{DI}=2.5Mhz with 5th harmonic as shown below. Amplitude ratio B/A of 50% and 80%	TH_{PD}	V_{DI} =250mvppd, (10%) $V_{PKTHR} = V_{REF} - 0.7v$	20		40	%
		0.5v ≤ V_{LQ} ≤ 1.5v, (100%) $V_{PKTHR} = V_{REF}$	90		110	%
SETLV input current	I_{LSL}	$V_{SETLV} = V_{REF}$			±10	µA

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
PKTHR input current	I_{PKTHR}	$V_{PKTHR} = V_{REF}$			±10	µA
RPDW pin Voltage	V_{RPDW}	3.8 KΩ ≤ RPDW≤ 24 KΩ	1.05	1.2	1.35	V
Pulse pairing $T_{PP} = 0.03/(16 \cdot f_{in})$ $\phi_{HR}=\phi_{LQ} - 90°$ [HR leads LQ in phase]	T_{PP}	$V_{LQ} = V_{HR} = 500mV_{ppd}$, f_{in} = 4 MHz			468	ps

[2] where $N_{EO} = (V_{ENVP}-V_{ENVN}) / (V_{ENVP}+V_{ENVN})$



For both RDATAP/N and ERASEP/N outputs

Single ended output high level	V_{OHpe}	I_{OHpe} = 4.0mA	V_{CC} – 1.0		V_{CC} – 0.6	V
Single ended output low level	V_{OLpe}	I_{OLpe} = –4.0mA	V_{CC} – 1.9		V_{CC} – .975	V
Single ended output swing	V_{Spe}		375	500	1000	mV
Pulse width	T_{PW1}	Max. pulse width, RPW=24KΩ [3]	11		17	ns
	T_{PW2}	Min. pulse width, RPW=8KΩ [3]	4		8	ns
Idle	T_{PW3}	Relaxation time trailing to leading edge [3]	3		8	ns

[3] Measured from differential cross over points.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Pseudo ECL rise and fall times	T_{RF}	±375mV of Zero cross, C_L=15pF, 220Ω across output			2.0	ns
delay from leading edge RDATA to leading edge ERASE	T_{EF}	[3]			±3.0	ns
peak detect sensitivity (of successive peaks)	Vps	TBD	200			mV
Pulse pairing $T_{PP} = 0.03/(16 \cdot f_{in})$ $\phi_{HR}=\phi_{LQ} - 90°$ [HR leads LQ in phase]	T_{PP}					
		$V_{LQ} = V_{HR} = 500mV_{ppd}$, f_{in} = 28 MHz,			67	ps

[3] Measured from differential cross over points.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
LQ comparator DC gain	A_{LQ}			700		V/V
HR comparator DC gain	A_{HR}			1600		V/V

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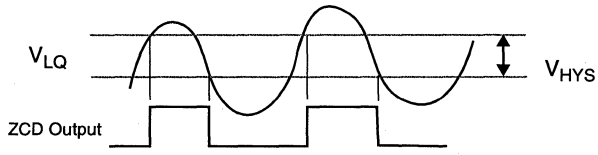
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Internal envelope detector discharge current	I_{ID}	R_{EXT}=6KΩ		10		µA
Internal envelope detector capacitance	C_{ID}		9		11	pF
LQ comparator input offset	V_{LO}				2	mV
LQ comparator input offset drift	V_{LT}				10	µV/°C
HR comparator input offset	V_{HO}				0.8	mV
Data detection F/F setup time	T_{DS}				1	ns
SETLV input voltage	V_{IN}		V_{REF}–1.33		V_{REF}	V
PKTHR input voltage	V_{IN}		V_{REF}–1.33		V_{REF}	V

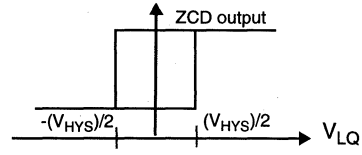
SERVO PEAK DETECTING DEMODULATOR

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Servo Input frequency	f_{INS}		4		13.5	MHz
Gain [(V_{SVO}–V_{SVR})/V_{LQ}]	AV_S	measured over 1/4 to 3/4 of scale [4]	1.60	1.725	1.85	V/V
Input dynamic range [low end]	V_{DIL}	V_{DIL}=(V_{DIP}-V_{DIN}) 1/8 of 24mVppd min. [5]			3	mV_{ppd}
Input dynamic range [high end]	V_{DIH}	V_{DIH}=(V_{DIP}-V_{DIN}) 7/8 of 250mVppd max. [5]	218			mV_{ppd}
Linearity of V_{FN} vs. V_{DI}	V_{FL}	measured over 1/8 to 7/8 of scale [6]	–0.5		0.5	%
Linearity of V_{SVO}–V_{SVR} vs. V_{DI}	V_{DL1}	measured over 1/8 to 3/4 of scale [6]	–1.4		1.4	%
	V_{DL2}	measured over 3/4 to 7/8 of scale [6]	–4.5		4.5	%
Output offset (not referred to input)	V_{SO}	intercept of regressed line [6]	–40		40	mV
Output for zero input	V_{ZI}	[6]	0	60	80	mV
Mismatch of sample & holds	V_{MM}	Variation for a common input % of full scale			±1.0	%
SRVREF voltage	V_{SR}		1.14	1.20	1.26	V
Sample and Hold voltage decay rate	V_{DR}	0.1% of full scale droop in 50µs			40	V/sec
ZX comparator differential hysteresis	V_{HYS}	4% to 8% of full scale at LQ pins [7]	40		80	mV_{ppd}

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[5] V_{DIL} and V_{DIH} specify the input range over which all other specifications must be met.
[6] In addition to the linearity and offset specifications, the output must also be guaranteed monotonic.
[7] Refer to waveshapes below for this specification.





PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Channel to channel cross talk	V_{CT}	Effect of A on B etc. % of full scale			±0.5	%
Output impedance	R_{SO}	SRVREF and SRVOUT pins			50	Ω
Demodulator repeatability (52dB)	N_{DR}	Repeatability without external noise			±5.0	mV
Power supply rejection ratio	$PSRR_S$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp} [8]	25			dB
Common mode rejection ratio	$CMRR_S$	0MHz ≤ f_{in} ≤ 1MHz $V_{LQP} = V_{LQN}$ = 100mV_{pp} [8]	25			dB
Total System Gain Variation $[(V_{SVO}-V_{SVR})/V_{DI}]$	AV_A	over all V_{DI} , 1/4 to 3/4 of scale [4]	1.54	1.725	1.92	V/V

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[8] The required demodulator output Signal-to-Noise Ratio (SNR) due to external noise is 49dB.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Peak Detector Bandwidth	f_{PD}	-3dB roll down of rectifier	68			MHz

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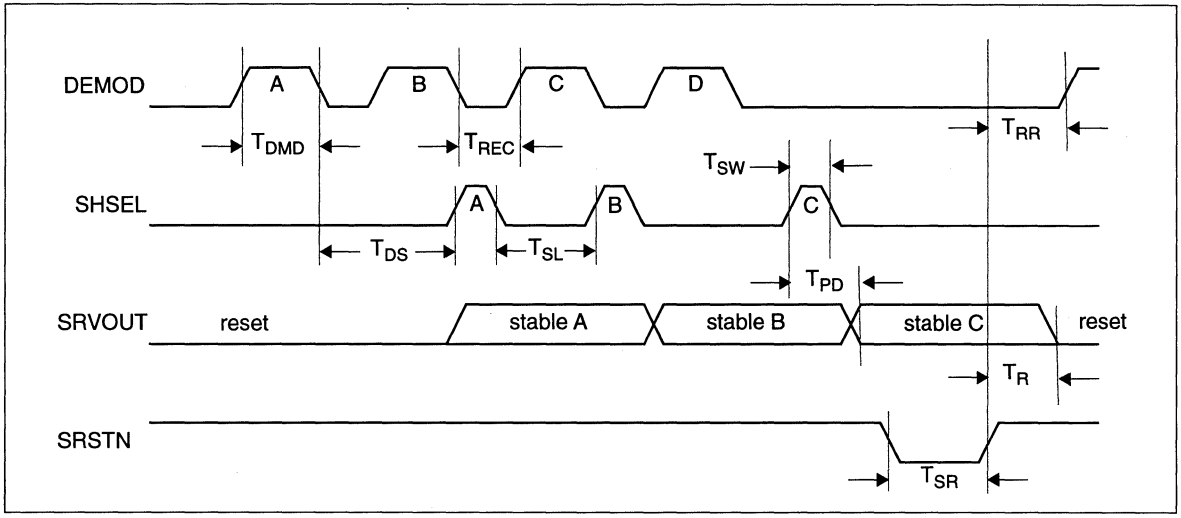
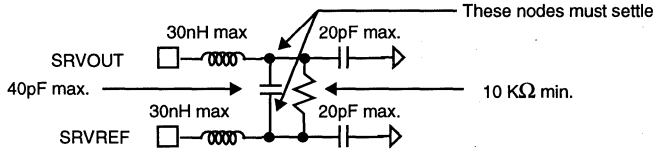
DEMODULATOR TIMING (Pins: DEMOD, SHSEL, SRVOUT, SGATE, SRSTN)



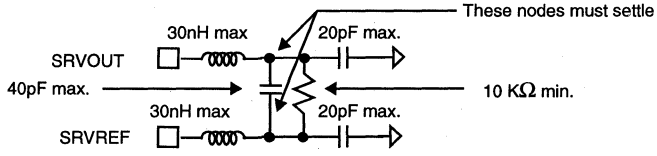
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Select clock pulse width	T_{SW}		50			ns
Select clock (SHSEL) to stable SRVOUT delay	T_{PD}	0.25% of final value [9]			150	ns
SRSTN pulse width	T_{SR}		600			ns

[9] Load condition for SRVOUT and SRVREF given below.

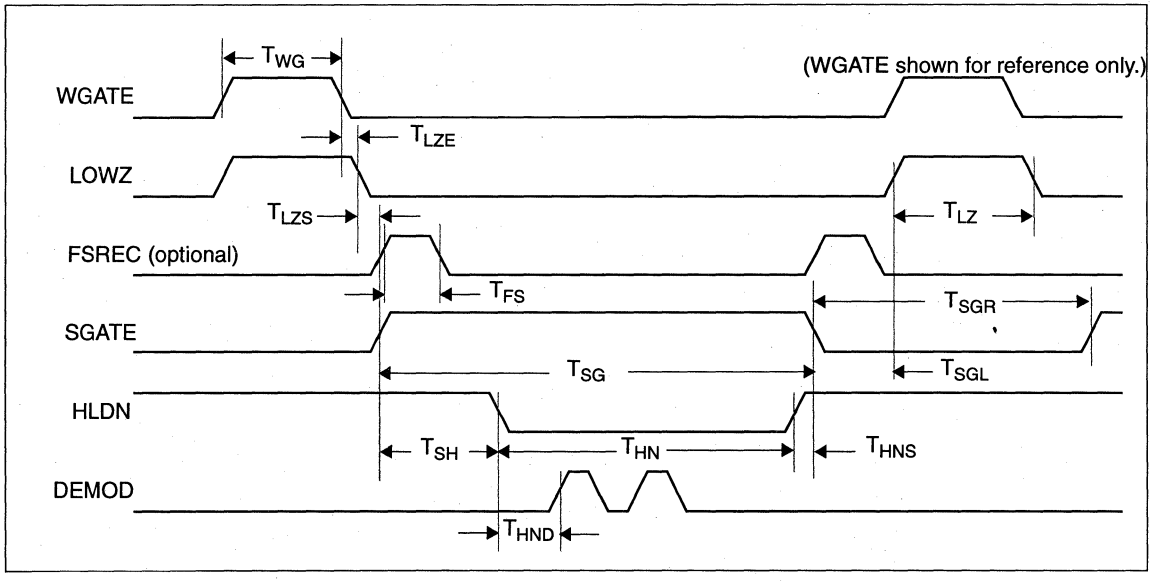


PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
DEMOD pulse width	T_{DMD}		150			ns
DEMOD recovery time	T_{REC}		150			ns
Select clock (SHSEL) inactive time	T_{SL}		50			ns
DEMOD to corresponding select clock delay	T_{DS}		0			ns
Sample and Hold step response	T_{SH}	0.25% of final value [9]			150	ns
Trailing edge SRSTN to SRVOUT reset delay	T_R	0.25% of final value [9]	150			ns
Trailing edge SRSTN to DEMOD recovery	T_{RR}		100			ns

[9] Load condition for SRVOUT and SRVREF given below.



SYSTEM TIMING DIAGRAM (NORMAL MODE) (Pins: LOWZ, FSREC, SGATE, HLDN, DEMOD)



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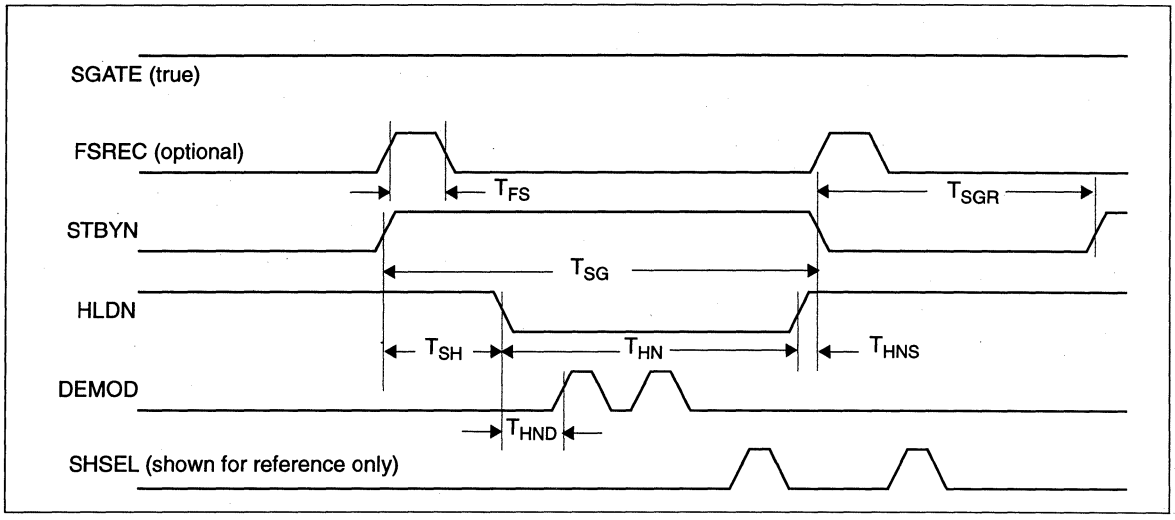
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
FSREC leading edge to V_{FN} stable	T_{FD}	V_{FN} stable within 10%			2.3	µs
Trailing edge of LOWZ to V_{FN} stable to 10%	T_{WR}	CAGCD value correct			500	ns
Lead, trailing edge SGATE to V_{FN} stable 10%	T_{GS}	CAGCS or D value correct			500	ns

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
LOWZ pulse width	T_{LZ}		1.6			µs
LOWZ to SGATE delay	T_{LZS}		–500			ns
SGATE (or STBYN) pulse width	T_{SG}		5			µs
SGATE (or STBYN) inactive width	T_{SGR}		100			µs
SGATE to LOWZ delay	T_{SGL}		0			ns
HLDN pulse width	T_{HN}		500			ns
HLDN to DEMOD delay	T_{HND}		25			ns
trailing edge of HLDN to SGATE delay	T_{HNS}		0			ns
FSREC pulse width	T_{FSW}		80		250	ns

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WGATE pulse width (given for reference only)	T_{WG}		1.6			µs
LOWZ extension time	T_{LZE}				500	ns

SYSTEM TIMING DIAGRAM (STANDBY MODE) (Pins: FSREC, SGATE, STBYN, HLDN, DEMOD)



PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
SGATE (or STBYN) pulse width	T_{SG}		5			µs
SGATE (or STBYN) inactive width	T_{SGR}		100			µs
HLDN pulse width	T_{HN}		500			ns
HLDN to DEMOD delay	T_{HND}		25			ns
Trailing edge of HLDN to SGATE delay	T_{HNS}		0			ns
FSREC pulse width	T_{FSW}		100		250	ns
FSREC leading edge to V_{FN} stable	T_{FDT}	V_{FN} stable within 10%			3.8	µs
Lead, trailing edge STBYN to V_{FN} stable 10%	T_{GST}	CAGCS or CAGCD value correct			2	µs

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VTC Inc.
Value the Customer™

VM5603

(1,7) ENCODER-DECODER WITH WRITE PRECOMPENSATION

August,1994

FEATURES

- (1,7) RLL Code
- Data Rates From 10 to 64 Mbits/sec
- Differential ECL Encoded Data and Clock
- Compatible with Zoned-Density Recording
- Programmable Write Precompensation
- Programmable Preamble Length Counted Before Decoder Enabled
- Designed to Operate with VM5351 Data Separator and VM5711 Reference Clock Generator
- Compatible with the AM95C95 Disk Data Controller
- Single Supply 5-Volt Operation
- Differential ECL Type Encoded Write Data Output
- Available in a 28-Lead PLCC Package

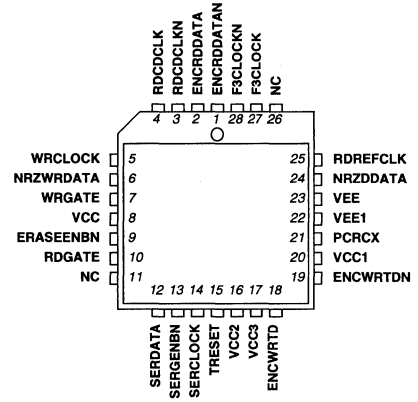
DESCRIPTION

The primary function of the VM5603 (1,7) ENDEC circuit is to encode and decode the 2/3 rate (1,7) Run Length Limited (RLL) modulation code used by the disk drive recording channel. In WRITE mode, the device receives NRZ write data and a write clock from the drive controller and outputs (1,7) encoded data to be recorded on the disk media. In READ mode, the device receives (1,7) encoded read data and a code rate clock from the drive read channel and outputs NRZ read data and a read clock to the drive controller.

The device also provides programmable write precompensation (WPC). This adjusts the encoded write data bit-to-bit timing to help compensate for fixed head/media induced read time errors (bit shift). An erase function is provided to enable DC erasure during drive testing and formatting.

The device is designed to be compatible with the AM95C95 Disk Data Controller IC in SCSI drive interface applications. It is also designed to be ESDI compatible. It is intended to support hard sector formats only.

CONNECTION DIAGRAM



28-lead PLCC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:	
V_{CC} (V_{EE} = 0)	0V to 7.0V
Ambient Operating Temperature	0° to +70°C
Junction Operating Temperature	0° to +130°C
Voltage Applied to TTL Inputs	-0.5V to V_{CC} +0.5V
Voltage Applied to ECL Inputs	0V to VCC
Storage Temperature	-55° to 150°C
Maximum Power Dissipation	650mW
Thermal Impedance Θ_{JA};	
28-lead PLCC	53°C/W

RECOMENDED OPERATING CONDITIONS

Supply Voltage:	
V_{CC} (V_{EE} = 0)	+4.5V to 5.5V
Junction Temperature	25° to 125°C
Data Rate Frequency (RD REF CLK)	10 to 64Mbits/sec
Write Precomp Full Scale Time Shift	3.5 to 14ns

DATA RECOVERY CIRCUITS

WRITE DATA ENCODE

The Write Data Encode function includes the Write Clock Resync, Encoder, Write Precompensation and Write Data Driver blocks (Shift Register block described separately).

The Write Clock Resync block receives TTL-level NRZ write data (NRZWRDATA) and the write clock (WRCLOCK) from the drive controller. The drive controller uses the read reference clock (RDREFCLK) from the VM5603 as a data rate reference to clock out NRZ write data. The RDREFCLK signal is returned as WRCLOCK by the drive controller. However, in an ESDI application, RDREFCLK must also pass through an arbitrary cable delay before it is returned as WRCLOCK. This creates an unknown phase relationship between WRCLOCK, and RDREFCLK, its source. The purpose of the Write Clock Resync block is to automatically choose the appropriate internal WRCLOCK phase to reliably clock in NRZWRDATA. This edge selection occurs upon each assertion of WRGATE.

The Encoder block takes each pair of NRZWRDATA bits (as WRDATA) and encodes them into three write data bits (ENCDATA) according to the following code tables.

DATA	*CODE*
11	110
10	100
01	001
00	000

In instances where the above table produces code sequences which violate the (1,7) run length constraint, the following violation code table is invoked (the MSB {left-most bit} is written/read first):

DATA	*CODE*
11 11	101 000
11 10	100 000
01 11	001 000
01 10	010 000

The NRZWRDATA input must be held low for three WRCLOCK periods after the assertion of WRGATE to allow internal clock edge selection (described above) and initialization of the encoder to a 3T code sequence (all zeros data). WRGATE must not be terminated prior to the completion of a write sequence. The Write Precompensation (WPC) block receives encoded write data (ENCDATA) and outputs precompensated data (ENCWRTD/ENCWRTDN) according to the following bit sequence algorithm:

BIT SEQUENCE					*COMPENSATION*
N-2	N-1	N	N+1	N+2	(at time N)
1	0	1	0	1	none
0	0	1	0	0	none
1	0	1	0	0	early
0	0	1	0	1	late

The magnitude of the WPC time shift is controlled by the Shift Register block output bits: B_0, B_1, B_2. With all bits low, no precompensation is employed. Seven timing values (binary sequence) can be programmed into the Shift Register block, with all bits high yielding the maximum or full scale time shift. The maximum shift is used when writing at lower data rates (inner zones on the disk). The minimum shift is used when writing at higher data rates (outer zones on the disk). The full scale time shift magnitude is set by an external capacitor and resistor tied from the PCRCX pin respectively to VCC and ground. This RC network sets up a time constant whose slope determines the amount of WPC shift. The full scale time shift is adjusted externally by the capacitor, C_{EXT}, tied from the PCRCX pin to VCC. The capacitor value is related to the full scale time shift by the following expression:

$$C_{EXT} = (5.86)(t_{WPC})$$

C_{EXT} is in pF and t_{WPC} is the full scale time shift in ns. The capacitor C_{EXT} is relatively small, so, parasitic capacitances associated with the PCRCX pin should be minimized. An external resistor R_{EXT} is tied from the PCRCX pin to ground and set to 2kΩ for **all applications**. This resistor is necessary to balance the internal circuitry and for the WPC time constant. It must be used even if the WPC function is not. To turn off the WPC function and minimize any time shift due to parasitic capacitance, it is recommended to set all of the WPC bits (B0 - B2) low and remove the capacitor from the PCRCX pin.

The ERASEENBN input, when held low, forces the ENCWRTD output low (and ENCWRTDN high) regardless of the other device inputs. The input will float high if left unconnected. The ENCWRTD output is also held high (and ENCWRTDN low) when WRGATE is inactive.

READ DATA DECODE

The Read Data Decode function includes the Decoder, Data Clock Generator/Read Initialize, Read Data/Ref Clock Generator and Shift Register blocks (Shift Register block described separately).

The Decoder block receives differential encoded read data (ENCRDATA/ENCRDATAN) and a differential code rate clock (RDCDCLK/RDCDCLKN) from the drive read channel. On the assertion of read gate (RDGATE), the Data Clock Generator/Read Initialize block counts a programmed number of data clock periods to give the drive read channel PLL/Data Synchronizer time to lock to the read data. The number of data clock periods is set by bits B3 through B7 of the Shift Register block, which loads a programmable counter. The least significant bit, B3, counts four periods. The five bit binary counter provides a programmable count from 4 to 124 in steps of four. All zeros loaded into the register puts the device in a special test mode such that the first clock edge of RDREFCLK gives VFOLKN assertion.

When the programmed count is reached, the Decoder begins receiving read data, looking for the first 010 010 code sequence which is the preamble PLL lock field pattern (all zeros NRZ data). When the pattern is detected, the Decoder is framed to the proper incoming read code phase, and seven code clock cycles later, begins outputting decoded read data at NRZRDDATA, which has been held low up to this time. The decode algorithm is the inverse of the coding algorithm specified in the coding table. Single-bit error propagation is five bits maximum.

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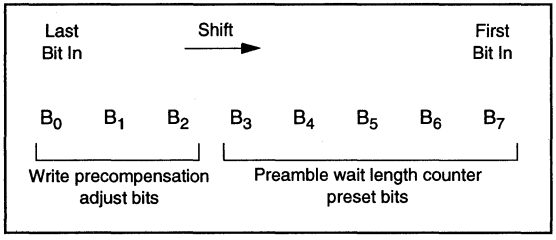
The Data Clock Generator/Read Initialize block also receives the differential 3F Clock (F3CLOCK/F3CLOCKN) from the drive read channel PLL/Data Synchronizer. The 3F clock must have a 50% duty cycle. The rising edge of the 3F clock must be synchronous with read code clock (1.5F, RDCDCLK) and meet the timing constraints outlined in the AC characteristics section. The 3F clock is divided by three, then outputted as RDREFCLK.

The Read Data/Ref Clock Driver block generates NRZRDDATA and RDREFCLK. It includes logic to hold the NRZRDDATA output low when RDGATE is inactive (low). The RDREFCLK output must be continuous when switching between operating modes with no more than two missing periods and no short duration glitches occurring at an interval less than one half a data rate period.

SHIFT REGISTER

The Shift Register block is an eight bit DFF-type serial storage register. Data is shifted into the register via the SERDATA and SERCLOCK pins when the SERGENBN pin is low. When the SERGENBN pin is high, the SERDATA and SERCLOCK inputs are ignored. The serial register stores bits B_0 through B_7, (B_7 is the most significant bit and is shifted into the serial register first). The definition for bits B0 - B7 is shown below.



Shift register code for programmable preamble length counter. Count = the number of data clock (RDREFCLK) periods from RGATE assertion, until the Decoder is enabled to read the preamble (VFOLKN signal goes low).

LSB				*MSB*	
B3	***B4***	***B5***	***B6***	***B7***	***COUNT***
1	1	1	1	1	4
0	1	1	1	1	8
1	0	1	1	1	12
0	0	1	1	1	16
1	1	0	1	1	20
0	1	0	1	1	24
1	0	0	1	1	28
0	0	0	1	1	32
1	1	1	0	1	36
0	1	1	0	1	40
1	0	1	0	1	44
0	0	1	0	1	48
1	1	0	0	1	52
0	1	0	0	1	56
1	0	0	0	1	60
0	0	0	0	1	64
1	1	1	1	0	68
0	1	1	1	0	72
1	0	1	1	0	76
0	0	1	1	0	80
1	1	0	1	0	84
0	1	0	1	0	88
1	0	0	1	0	92
0	0	0	1	0	96
1	1	1	0	0	100
0	1	1	0	0	104
1	0	1	0	0	108
0	0	1	0	0	112
1	1	0	0	0	116
0	1	0	0	0	120
1	0	0	0	0	124
0	0	0	0	0	*

* First rising edge of RDREFCLK gives VFOLKN high to low.

Shift register code for WPC magnitude (FS = full scale).

LSB		*MSB*	***Write Precompensation Magnitude***
B0	***B1***	***B2***	
0	0	0	NONE
1	0	0	(1/7)FS
0	1	0	(2/7)FS
1	1	0	(3/7)FS
0	0	1	(4/7)FS
1	0	1	(5/7)FS
0	1	1	(6/7)FS
1	1	1	FS

PIN DESCRIPTIONS

INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
ENCRDDATAN, ENCRDDATA	1, 2	Differential, ECL level encoded read data from the drive read channel PLL/Data Synchronizer.

RDCDCLKN, RDCDCLK 3, 4 Differential, ECL level, code rate clock from the drive read channel PLL/Data Synchronizer. Used to clock in ENCRDDATA in read mode and used as a code rate reference clock in write mode.

WRCLOCK 5 TTL level clock at the system data rate used to clock in NRZWRDATA, active on rising edge.

NRZWRDATA 6 TTL level (active high) NRZ write data from the drive controller.

WRGATE 7 TTL Level (active high) input from the drive controller used to put the device in write (encode) mode.

ERASEENBN 9 TTL level input which, when low, holds the ENCWRTD output low and ENCWRTDN high regardless of the other device inputs. The pin has an internal resistor pull-up.

RDGATE 10 TTL level (active high) input from the drive controller used to put the device in read (decode) mode.

SERDATA 12 TTL level data (active high) input to the shift register. Data is clocked in using SERCLOCK. The MSB of the register word (B7) is clocked in first.

SERGENBN 13 TTL level shift enable and latch input. When low, it enables SERDATA to be clocked into the serial register using SERCLOCK. When high, the SERDATA and SERCLOCK inputs are ignored and the data existing in the serial register passes through a parallel set of transparent latches.

SERCLOCK 14 TTL level clock input to the shift register. The rising edge is used to clock in SERDATA.

TRESET 15 TTL level (active low) pin used to reset the device for testing at VTC. Normally left open in application.

F3CLOCK, F3CLOCKN 27, 28 A differential ECL level clock at three times the system data rate, active on the rising edge. This clock comes from the drive read channel PLL/Data Synchronizer. It is used to generate the RDREFCLK output.

OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
ENCWRTD	18	This pin is one side of a differential ECL output, with ENCWRTDN being its complement. The rising edges are (1,7) encoded write data transitions to be recorded on the drive media. When WRGATE is low, this output is held low.
ENCWRTDN	19	Complement of ENCWRTD.
NRZRDDATA	24	TTL level (active high) NRZ read data output to the drive controller. When RDGATE is low, this output is held low. The output is also held low after the assertion of RDGATE for the duration of the internal programmable counter time.
RDREFCLK	25	TTL level clock output. In read mode, it is used to clock NRZRDDATA into the drive controller. In write mode, the controller uses it as a data rate reference clock to clock out NRZWRDATA. The output runs continuously with no more than two missing clock pulses and no short duration glitches associated with mode changes.

ANALOG PINS:

PIN NAME	PIN NO.	DESCRIPTION
PCRCX	21	Used to set the WPC full scale time shift value with an external resistor to ground and external capacitor to VCC.

Note: C_{EXT} can range between 0pF and 100pF. Care should be taken when choosing C_{EXT} at higher data rates such that the full scale time shift does not extend the window size. For example, at 64Mbits/sec NRZ data rate, the RDCDCLK is 96MHz. This equates to a window size of 10.4ns. If a 100pF capacitor is used for C_{EXT}, then the full scale WPC shift would be 17.1ns and the shifted pulse would be lost.

POWER PINS:

PIN NAME	PIN NO.	DESCRIPTION
VCC	8	+5V supply for internal logic.
VCC1	20	+5V supply for TTL output buffers.
VCC2	16	+5V supply for analog functions.
VCC3	17	+5V supply for ECL output buffers.
VEE1	22	Ground for TTL output circuits.
VEE	23	Ground for internal logic and analog.

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DC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	ICC		50		120	mA
TTL Inputs (Note 1)						
Voltage In High	V_{IH}		2.0			V
Voltage In Low	V_{IL}				0.8	V
Input Current High	I_{IH}	$V_{IN} = 2.7V$, $V_{CC} = 5.5V$			20	µA
Input Current High	I_{IH}	$V_{IN} = 6V$, $V_{CC} = 5.5V$			100	µA
Input Current Low	I_{IL}	$V_{IN} = 0.5V$, $V_{CC} = 5.5V$			-0.6	mA
Clamp Voltage	V_{IK}	Input Current = -18mA, $V_{CC} = 4.5V$			-1.2	V
TTL Outputs						
Voltage Output High	V_{OH}	$I_{OH} = -400µA$, $V_{CC} = 4.5V$	2.5			V
Voltage Output Low	V_{OL}	$I_{OL} = 4mA$, $V_{CC} = 4.5V$			0.4	V
Output Short circuit Current	I_{OS}	$V_{CC} = 5.5V$, (Note 3)	-20		-130	mA
ECL Input (Differential)(Notes 2 & 4)						
Voltage In	V_{IN}		V_{CC} - 2.3		V_{CC} - 0.3	V
Differential Input Voltage	V_{DIFF}		200			mV
Input Current	I_{IN}	$V_{CC} = 5.5V$, $V_{IN} = 3.2V$ to 5.2V			25	µA
ECL Outputs (Differential)(Note 2)						
Voltage Output High	V_{OH}	$T_A = 0°C$	V_{CC}-1.02		V_{CC} - 0.78	V
Voltage Output High	V_{OH}	$T_A = 25°C$	V_{CC}-0.98		V_{CC} - 0.75	V
Voltage Output High	V_{OH}	$T_A = 70°C$	V_{CC}-0.93		V_{CC} - 0.67	V
Voltage Output Low	V_{OL}	$0°C \le T_A < 70°C$	V_{CC} - 1.95		V_{CC} - 1.60	V

Note 1: TTL inputs will float to a logic one if unconnected.
Note 2: All inputs and outputs denoted as ECL track with the V_{CC} supply voltage.
Note 3: Not more than one output shorted at one time. Duration of test not to exceed one second.
Note 4: DC test limits are specified after thermal equilibrium has been established. All ECL outputs are loaded with 50Ω to V_{CC} - 2.0V.

CONTROL FUNCTION DELAYS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
SERDATA Setup Time	t_{sSERD}		40			ns
SERDATA Hold Time	t_{hSERD}		0			ns
SERGENBN Setup Time	t_{sSERE}		40			ns
SERGENBN Hold Time	t_{hSERE}		40			ns
SERCLOCK Period	t_{SERC}		100			ns

AC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$, $R_{EXT} = 2k\Omega$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
NRZWRDATA Setup Time	t_{sWNRZ}		3			ns
NRZWRDATA Hold Time	t_{hWNRZ}		1			ns
WRCLOCK Duty Cycle	t_{dcWCLK}		35	50	65	%
ENCWRTDN Output Propagation Delay from WRCLOCK Positive Edge	t_{pdWDO}	t_{RCC} is cycle time of RDCDCLK	(13 * t_{RCC} + 5)		(14 * t_{RCC} + 25)	ns
ENCWRTD/N Fall Time	t_{fWDO}	C_{load} = 15pF		3.25		ns
ENCWRTD/N Rise Time	t_{rWDO}	C_{load} = 15pF		2.75		ns
ENCWRTD/N Pulse Width	t_{pwWDO}	Precompensation off: no C_{EXT}, f_{RCC} is cycle time of RDRDCLK		t_{RCC}		ns
Full Scale WPC Time Shift	t_{WPC}		-15%	C_{EXT}/5.86	+15%	ns
WPC Time Shift Linearity	LIN (WPC)		-0.4		0.4	LSB
t_{WPC} Symmetry $\lvert t_{WPC}$ (early)$\rvert$ - $\lvert t_{WPC}$ (late)$\rvert$	SYM (WPC)		(-0.5 * C_{EXT}/5.86)	0	(-0.5 * C_{EXT}/5.86)	ns

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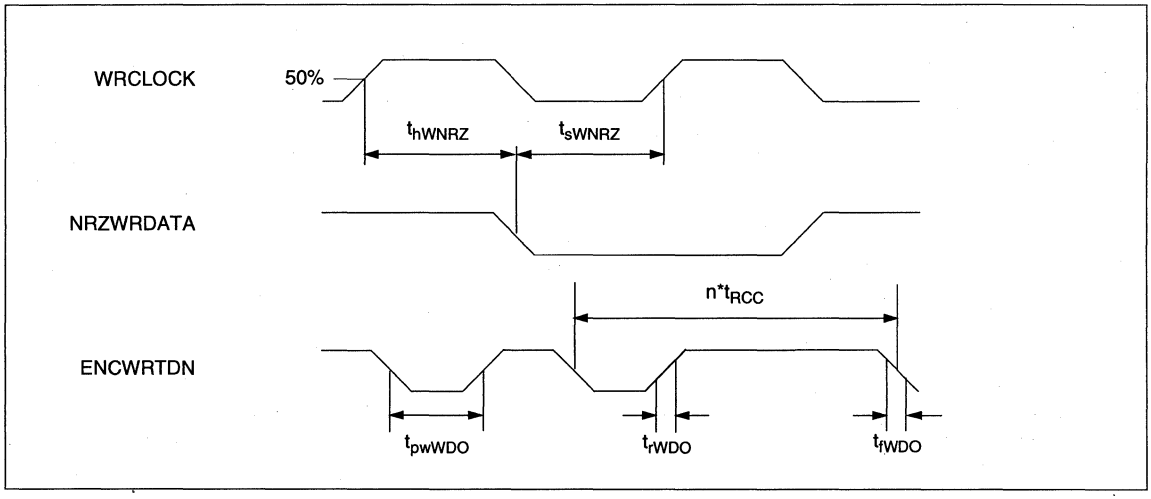
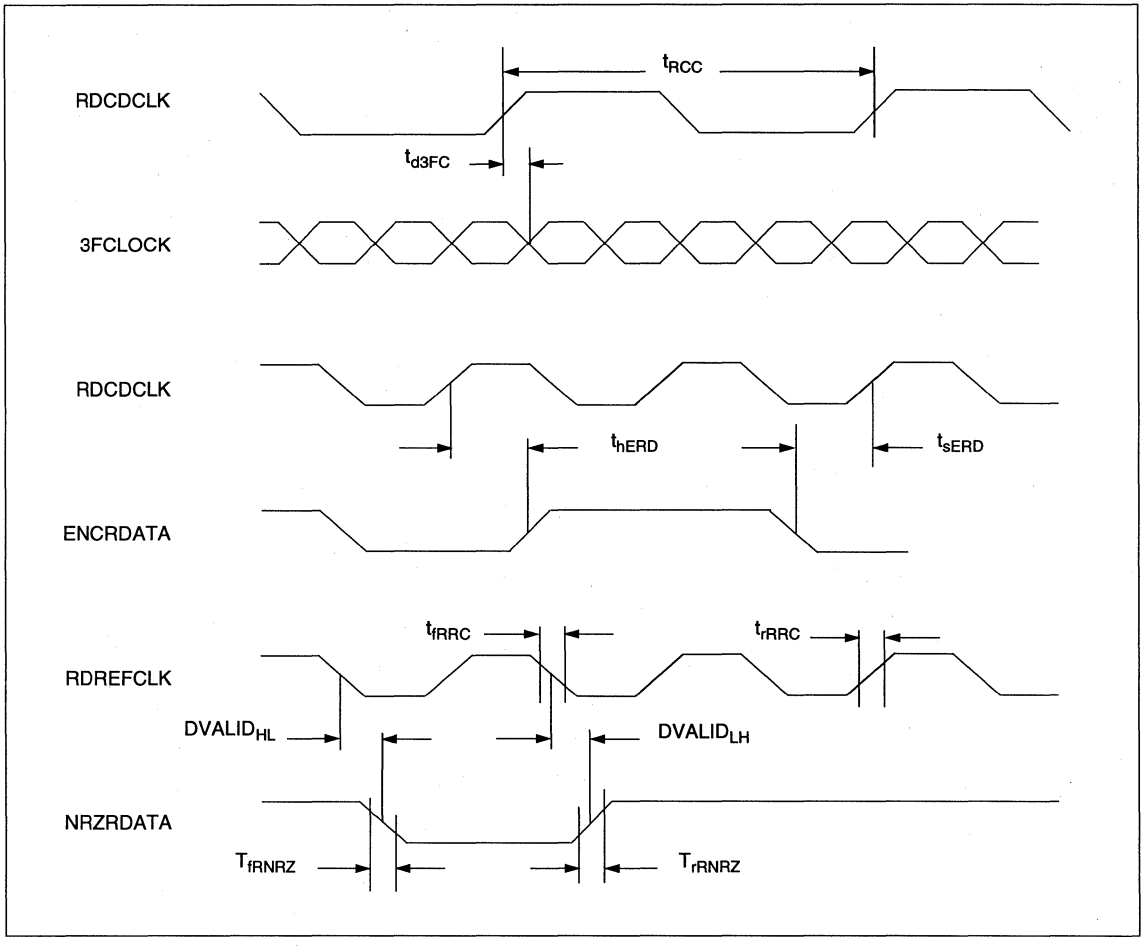
READ CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
ENCRDDATA/N Setup Time	t_{sERD}		3			ns
ENCRDDATA/N Hold Time	t_{hERD}		1			ns
RDCDCLK Duty Cycle	t_{dcRCC}		45		55	%
NRZRDDATA Propagation Delay from RDCDCLK Positive Edge	t_{pdRNRZ}	t_{RCC} is cycle time of RDCDCLK	(7 *t_{RCC} +5)		(8 *t_{RCC} +25)	ns
RDREFCLK Fall Time	t_{fRRC}	C_{load} = 15pF		3.25		ns
RDREFCLK Rise Time	t_{rRRC}	C_{load} = 15pF		2.75		ns
NRZRDDATA Fall Time	t_{fRNRZ}	C_{load} = 15pF		3.25		ns
NRZRDDATA Rise Time	t_{rRNRZ}	C_{load} = 15pF		2.75		ns
NRZRDDATA High Data Valid	$DVALID_{LH}$	Measured from RDREFCLK falling edge 1.5V threshold		2.25	4.3	ns
NRZRDDATA Low Data Valid	$DVALID_{HL}$	Measured from RDREFCLK falling edge 1.5V threshold		2.0	3.4	ns
RDREFCLK Duty Cycle	t_{dcRRC}		40		60	%
F3CLOCK Delay Time	t_{d3FC}		3			ns
F3CLOCK Duty Cycle	t_{dc3FC}		40		60	%

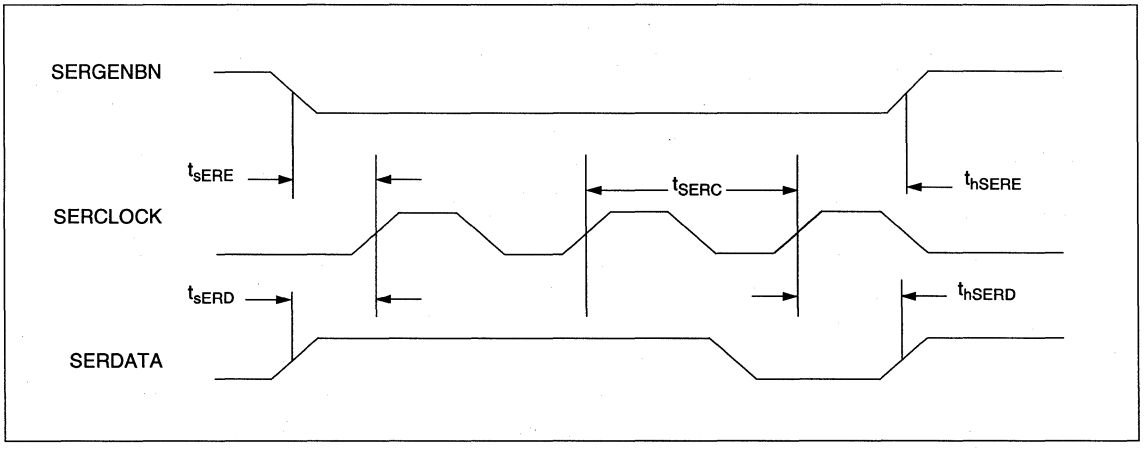
WRITE TIMING DIAGRAMS



READ TIMING DIAGRAMS



CONTROL FUNCTION TIMING DIAGRAMS



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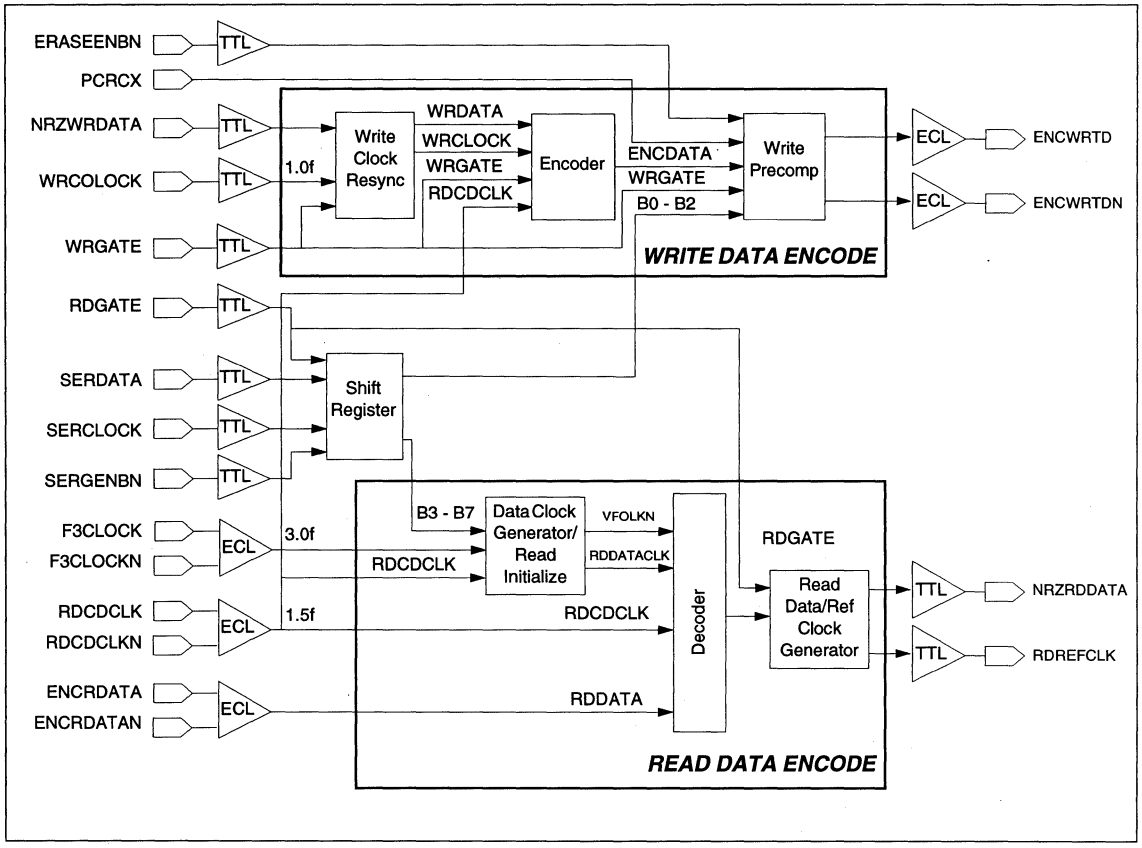
VM5603 BLOCK DIAGRAM



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VM5621/VM5622

(2,7) ENCODER-DECODER

August,1994

FEATURES

- Encodes and Decodes IBM (2,7) Code
- 48 Mbits/sec Maximum Code Rate
- Soft-Sector 2T Frequency Address Mark Generation
- Preamble Lock Time = 64 • T (T = one period of 2F clock)
- 4T (1000...) Preamble Frequency Detection
- Two Supply Options:
  VM5622: ±5V Supplies, TTL Above Ground and Differential ECL Below Ground
  VM5621: +5V Supply Only, TTL and ECL Run Above Ground
- VM5621 is Compatible With the VM5351/VM5352
- The VM5621 has a Power Dissipation of 405mW Typca
- The VM5622 has a Power Dissipation of 505mW Typical
- Differential ECL Drivers and Receivers for Clock and Data Interface Lines
- Available in a 28-lead PLCC Package

DESCRIPTION

The (2,7) Encoder/Decoder (ENDEC) performs the encoding and decoding necessary to use the (2,7,1,2,4) Run-Length Limited (RLL) code for disk drive memory systems.

The ENDEC also performs many other functions such as writing of an address mark for soft sectored disk formats, and the reading of a preamble pattern (PLL sync field) that is compatible with the (2,7) RLL code. The ENDEC is fabricated using a high-speed ECL 2.5 bipolar process.

ABSOLUTE MAXIMUM RATINGS

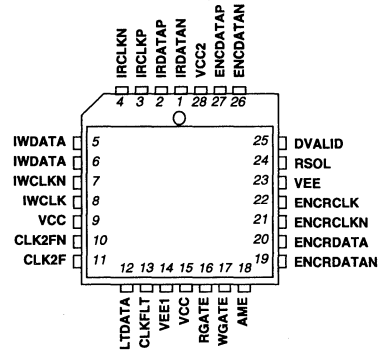
VM5621

Power Supply Voltages
(V_{EE} = 0V) ..... 0V to 7V
Storage Temperature Range ..... -55° to +150°C
Ambient Temperature Range ..... 0° to +70°C
Voltage Applied to TTL Inputs (V_{EE} = 0V) ..... V_{CC} + 0.5V
Voltage Applied to ECL Inputs (V_{EE} = 0V) ..... 0V to V_{CC}
Maximum Power Dissipation 515mW
Junction Temperature ..... 150°C
Thermal Impedance, Θ_{JA}
28-lead PLCC ..... 53°C/W

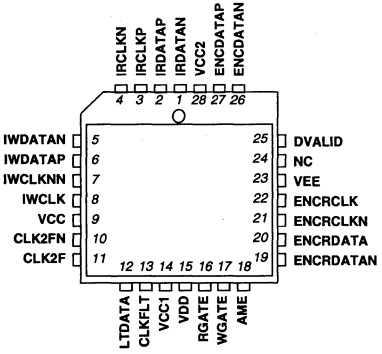
VM5622

Power Supply Voltages
V_{DD} (V_{CC} = 0V) ..... 0V to 7V
V_{EE} (V_{CC} = 0V) ..... 0V to -5.72V
Storage Temperature Range ..... -55° to +150°C
Ambient Temperature Range ..... 0° to +70°C
Voltage Applied to TTL Inputs (V_{CC} = 0V) -0.5V to V_{DD} +0.5V
Voltage Applied to ECL Inputs (V_{CC} = 0V) ..... 0V to V_{EE}
Maximum Power Dissipation 630mW
Junction Temperature ..... 150°C
Thermal Impedance, Θ_{JA}
28-lead PLCC ..... 53°C/W

CONNECTION DIAGRAMS



28-lead PLCC (1 supply)



28-lead PLCC (2 supply)

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
V_{EE} ..... -4.5V to -5.72V
V_{CC}, V_{DD} ..... 4.5V to 5.5V
Ambient Operating Temperature ..... 0° to 70°C
Operating Junction Temperature ..... 0° to 130°C
Data Rate ..... 10 to 48Mbits/sec

DATA RECOVERY CIRCUITS

PIN DESCRIPTIONS

INPUT SIGNALS:

ENCODED READ DATA (ENCRDATA) (differential ECL): This is the encoded data output of the data separator circuit. It is synchronized with the ENCODED READ CLOCK. The positive edge of the ENCODED READ CLOCK signal is used to strobe the ENCODED READ DATA into the (2,7) ENDEC.

ENCODED READ CLOCK (ENCRCLK) (differential ECL): This is the clock synchronized to the ENCODED READ DATA and is generated by the data separator.

READ GATE (RGATE) (TTL): This is a control signal which initiates a read operation when asserted. The input is active low.

INTERFACE WRITE DATA (IWDATA) (differential ECL): This is the unencoded NRZ write data from the disk controller. The INTERFACE WRITE CLOCK strobes the INTERFACE WRITE DATA into the VM5621/VM5622.

INTERFACE WRITE CLOCK (IWCLK) (differential ECL): This clock strobes the INTERFACE WRITE DATA into the encoder and is generated by the controller.

WRITE GATE (WGATE) (TTL): This is a control signal which initiates a write operation when asserted. The input is active low.

ADDRESS MARK ENABLE (AME) (TTL): This is a control signal which works in conjunction with the WRITE GATE input. Assertion of ADDRESS MARK ENABLE (low) concurrently with WRITE GATE asserted (low) causes writing of a 2T frequency address mark.

2F CLOCK (CLK2F) (differential ECL): This signal originates on the drive and is used to clock the encoder and lock to data timer blocks. The frequency of the 2F clock is two times the data bit rate.

RSOL (TTL): Used by an intelligent interface controller to correct a detected frame error (caused by a system noise) active on falling edge.

OUTPUT SIGNALS:

INTERFACE READ DATA (IRDATA) (differential ECL): This is the decoded read data from the disk. A high level represents a one of decoded data. It is strobed into the disk controller by the positive edge of the INTERFACE READ CLOCK.

INTERFACE READ CLOCK (IRCLK) (differential ECL): This is the clock synchronized to the INTERFACE READ DATA and drives the READ CLOCK input of the disk controller. The positive edge of the REFERENCE CLOCK should be used by the disk controller to strobe the READ DATA bit when in the read mode.

LOCK TO DATA (LTDATA) (TTL): This is a control output which signifies that a minimum length of a preamble pattern has been read. This output may be used to switch the Data Separator circuit from a high to a low tracking rate mode. The output is active low.

ENCODED WRITE DATA (ENCDATA) (differential ECL): This is the encoded (2,7) write data in RZ format. It drives the Read/Write amplifier circuit. A high level pulse returning to zero is output for each 'one' that is to be written on the disk's media.

DVALID (ECL): An active high signal in sync with valid encoded data (ENCDATAP, ENCDATAN).

CLKFLT (TTL): An active low signal which detects an 8 or greater gap in the interface write clock.

CIRCUIT CHARACTERISTICS

2T ADDRESS MARK: This address mark actually violates the (2,7) RLL constraints. Instead of detecting a gap, the VM5621/VM5622 will write a 2T frequency address mark but is not capable of detecting the address mark. An external circuit is required for 2T address mark detection.

Decoding Sequence of Events

A read operation is initiated by asserting READ-GATE (low) with AME high. At this time, the LTDATA timer circuit begins to count 2f clock pulses and the data separator IC begins locking to the preamble sync field. LTDATA remains false for 64 2f clock cycles after READ GATE is asserted. After the timer has completed its count, LTDATA is asserted and the LTDATA output goes low, the decoder synchronizes itself to the preamble sync field (4T pattern), and the read data is decoded. Refer to the control timing diagrams.

DATA/ (2,7) CODE MAPPING

NRZ DATA ←		*CODE* ←	
MSB	*LSB*	*MSB*	*LSB*
00		1000	
01		0100	
100		001000	
101		100100	
111		000100	
1100		00001000	
1101		00100100	

Most significant bit (MSB) is read/written first.

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DC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
TTL Inputs (Note 1)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.5V, note 4			20	µA
		V_{IH} = 6V, V_{CC} = 5.5V, note 4			100	
Input Low Current	I_{IL}	V_{IN} = 0.5V, V_{CC} = 5.5V, note 4			-0.6	mA
Output High Voltage	V_{OH}	V_{CC} = 4.5V; I_{OH} = -400µA, note 4	2.5			V
Output Low Voltage	V_{OL}	V_{CC} = 4.5V; I_{OL} = 4mA, note 4			0.4	V
Input Clamp Voltage	V_{IK}	V_{CC} = 4.5V; V_{IN} = -18mA, note 4			-1.2	V
Output Short Circuit Current	I_{OS}	V_{CC} = 5.5V; V_{IN} = 0V, notes 3 & 4	-20		-130	mA
Differential ECL Inputs (Notes 2 & 4)						
Common Mode Input Voltage	V_{CIM}		V_{CC} - 2.3		V_{CC} - 0.3	V
Differential Input Voltage	V_{INDIF}		200			mV
Input High Current	I_{IH}	V_{IH} = maximum			25	µA
Input Low Current	I_{IL}	V_{IL} = maximum			25	µA
Voltage Output High	V_{OH}	0°C	V_{CC} - 1.02		V_{CC} - 0.78	V
		25°C	V_{CC} - 0.98		V_{CC} - 0.75	
		70°C	V_{CC} - 0.92		V_{CC} - 0.66	
Voltage Output Low	V_{OL}	0°C	V_{CC} - 1.95		V_{CC} - 1.63	V
		25°C	V_{CC} - 1.95		V_{CC} - 1.63	
		70°C	V_{CC} - 1.95		V_{CC} - 1.63	
MECL 10KH Compatible (Notes 2 & 4)						
Voltage Output High	V_{OH}	0°C	V_{CC} - 1.00		V_{CC} - 0.84	V
		25°C	V_{CC} - 0.96		V_{CC} - 0.81	
		70°C	V_{CC} - 0.90		V_{CC} - 0.74	
Voltage Output Low	V_{OL}	0°C	V_{CC} - 1.95		V_{CC} - 1.63	V
		25°C	V_{CC} - 1.95		V_{CC} - 1.63	
		70°C	V_{CC} - 1.95		V_{CC} - 1.63	

Note 1: TTL inputs will float to a logic HI if left unconnected.

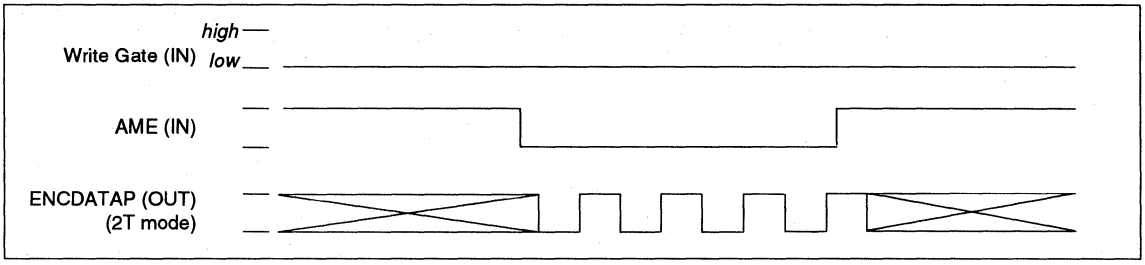
Note 2: All inputs and outputs denoted as ECL track with the V_{CC} supply voltage.

Note 3: Not more than one output shorted at one time duration of test not to exceed one second

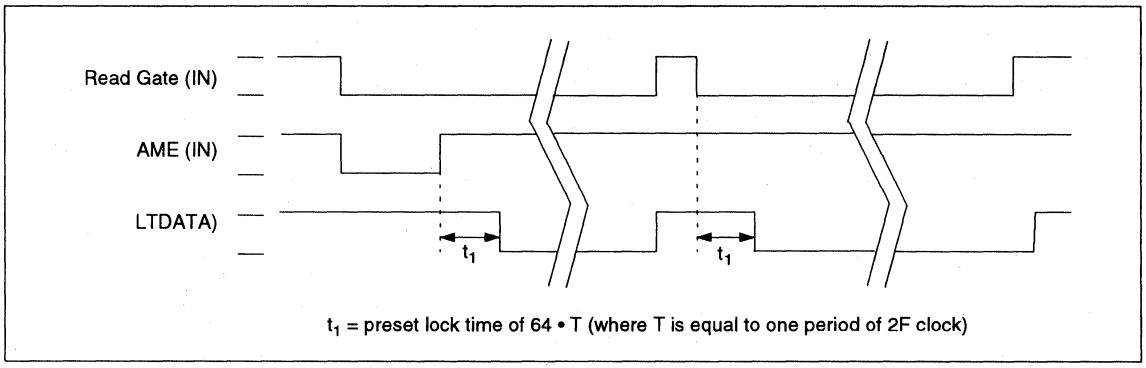
Note 4: DC test limits are specified after thermal equilbrium has been established with the device having a controlled transverse air flow of 750lfpm. VM5621, V_{CC} = 5.0V, V_{EE} = 0, V_{DD} N/A. VM5622, V_{CC} = 0, V_{DD} = 5.0V, V_{EE} = -5.2V. All ECL outputs are loaded with 50Ω to V_{CC} - 2.0V, except DVALID which is loaded with 100Ω to V_{CC} - 2.0V.

CONTROL SIGNAL TIMING

A: Address Mark Write



B: Read Timing (Compatible with SMD Standards)



t_1 = preset lock time of 64 • T (where T is equal to one period of 2F clock)

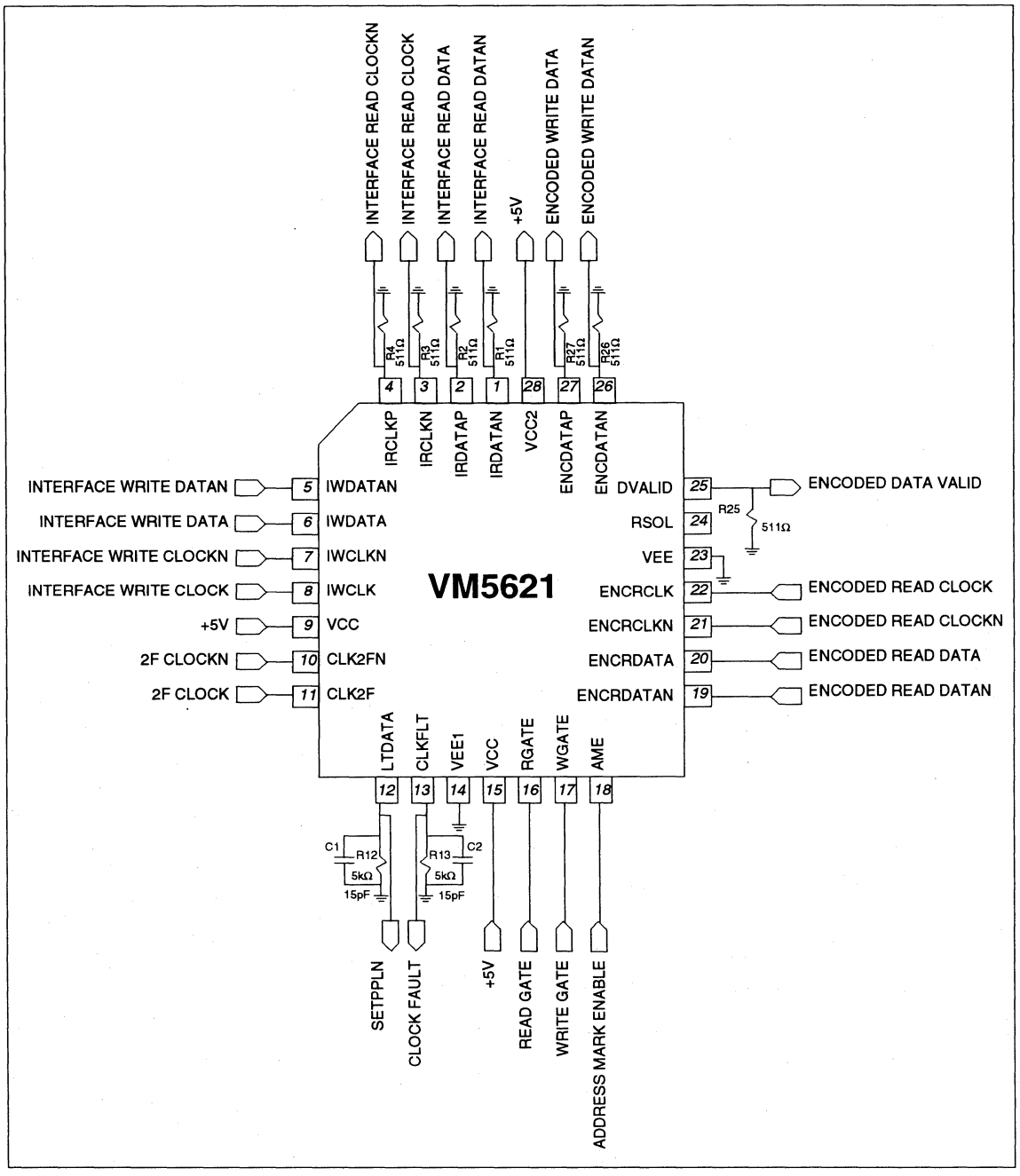


Figure 1: VM5621 Typical Connection Diagram

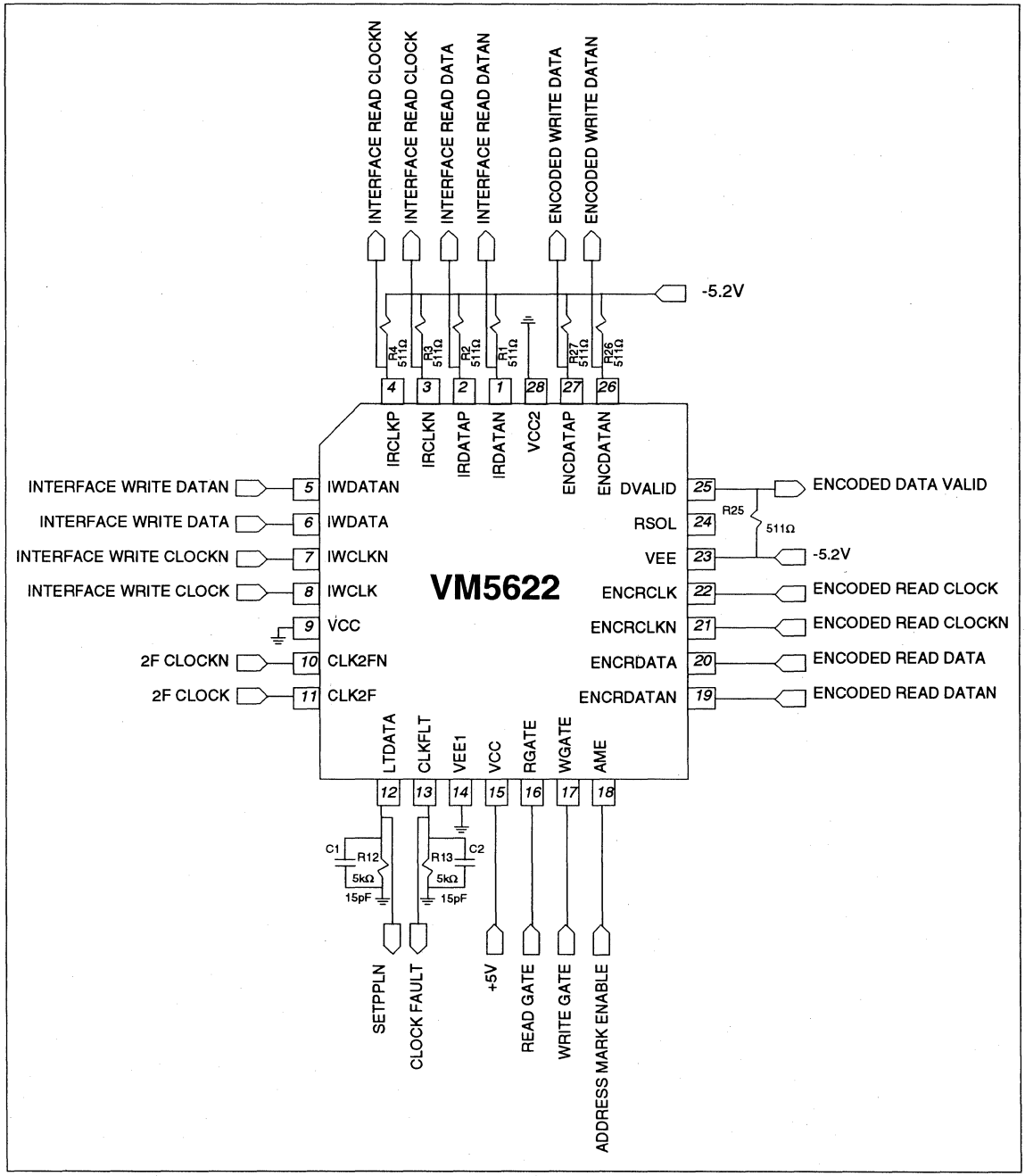


Figure 2: VM5622 Typical Connection Diagram

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VTC Inc.
Value the Customer™

VM5711

FREQUENCY SYNTHESIZER/PHASE LOCKED LOOP

August,1994

FEATURES

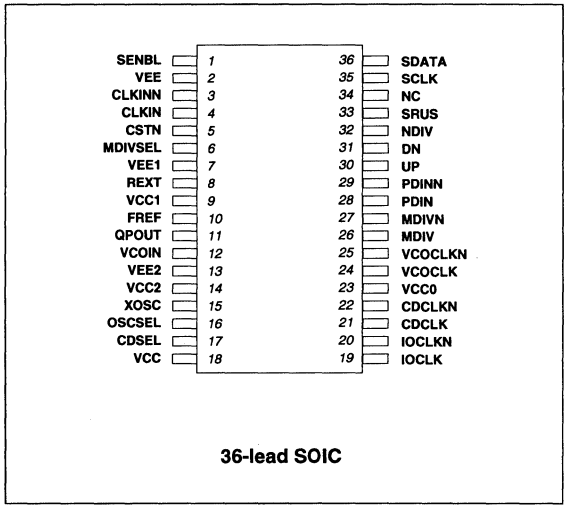
- Compatible with Zoned-Density Recording Applications
- Suitable for Many Applications in Data Communications, Graphics, etc.
- Differential ECL Output Frequency from 40 to 200 MHz
- Supports (1,7) Channel Data Rates up to 64 Mbits/sec
- Compatible with VTC's VM5603, VM5355, and VM5351/VM5352
- User Determined PLL Loop Filter Network
- Low Power Mode
- Power Dissipation less than 500 mW typical
- Power Supplies: +5 V Only

DESCRIPTION

The VM5711 is an integrated circuit designed to be used in high-performance zoned-density recording schemes. Its primary circuit function is to generate a variable frequency reference clock which is used as the fundamental system clock by the data recording channel. A serial microprocessor interface provides convenient access to internal registers which control the internal dividers and DAC. It can be used in zoned density schemes with recording frequency ratios of up to 1:2.5.

Please consult VTC for package availability.

CONNECTION DIAGRAM



36-lead SOIC

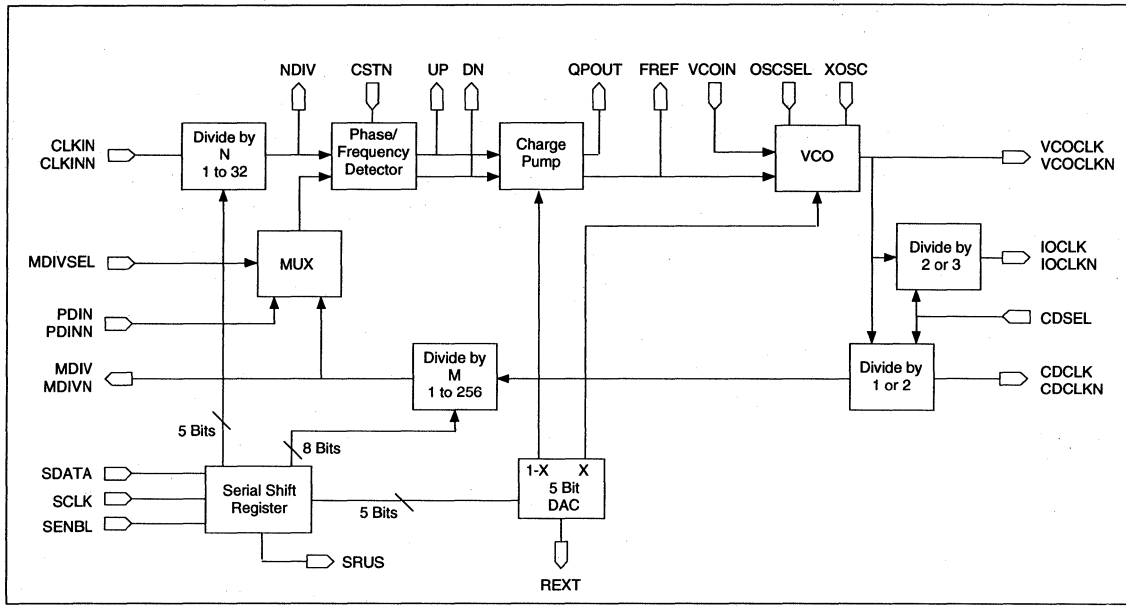
ABSOLUTE MAXIMUM RATINGS

Supply Voltage:
V_{CC} (V_{EE} = 0) ..... -0.5V to 7.0V
Voltage Applied to TTL Inputs
V_{EE} = 0V ..... -0.5V to VCC +0.5V
ECL Output Current - Continuous 25mA
- Surge 50mA
Ambient Operating Temperature ..... 0° to +70°C
Junction Temperature ..... 0° to +150°C
Storage Temperature ..... -65° to 150°C
Maximum Power Dissipation 650mW
Thermal Impedance Θ_{JA};
36-lead SOIC ..... 50°C

RECOMENDED OPERATING CONDITIONS

Supply Voltage:
V_{CC}, V_{CC0}, V_{CC1}, V_{CC2} ..... +4.5V to 5.5V
Junction Operating Temperature ..... 0° to 130°C
Operating Temperature ..... 0° to +70°C
ECL Reference Input Frequency
CLKIN, CLKINN ..... 4 to 50MHz
Synthesizer Output Frequency ..... 40 to 200MHz
R_{EXT} Resistance (DAC current set) ..... 1.25 to 5kΩ

BLOCK DIAGRAM



FREQUENCY SYNTHESIZER

The frequency synthesizer is implemented using a charge pump type Phase-Lock Loop (PLL) with programmable reference clock and VCO feedback frequency dividers. The frequency synthesizer consists of a VCO, charge pump, phase/frequency detector, and two programmable frequency dividers. Refer to the block diagram.

The synthesizer reference clock signal that is used to drive the block comes into the chip through the CLKIN, CLKINN input pins. The Divide-by-N counter divides the incoming reference clock by a programmable integer value from 1 to 32. The output of the Divide-by-N becomes the reference clock for the synthesizer PLL. The Divide-by-M counter divides the CDCLK output by a programmable integer value from 1 to 256. The output of the Divide-by-M becomes the variable input to the synthesizer PLL. Both counters are programmed from the serial registers.

The phase/frequency detector block is a true frequency discriminating comparator with 2π radians per cycle usable for phase/frequency correction. An input pulse at the reference input initiates a pump-up signal to the Charge Pump and an input pulse at the variable input initiates a pump-down signal. When both pump-up and pump-down are true the circuit is reset. The minimum pump-up and pump-down pulse widths are determined by internal propagation delays and are about 5ns. In the locked condition, the pump-up and the pump-down signals are true for a short and equal period and are coincident in time. The pump-up and pump-down signals may be observed at the UP and DN test pins.

The charge pump sources and sinks correction current at the QPOUT pin when the pump-up and pump-down signals are true, respectively. An external RC network, connected between pin VCOIN and pin FREF, is used to set the PLL dynamic characteristics. The FREF pin connects to a low impedance loop filter reference node to minimize noise coupling into the VCO input. The voltage at this pin is about 2.5V. The charge pump current driven into the loop filter generates a differential voltage at pin VCOIN with respect to pin FREF. This voltage drives the VCO block inputs. The charge pump gain (the output current magnitude divided by 2π) is set by the current output from the internal DAC determined by R_{EXT} and the DAC setting.

The VCO block converts the differential voltage between pins VCOIN and FREF into a frequency. This frequency is output at the two differential (uncompensated) ECL pins VCOCLK and VCOCLKN and is also fed back to the Phase/Frequency Comparator through the Divide-by-M counter. Center frequency occurs when the voltage between the filter pins is zero. Center frequency is set by the R_{EXT} and the DAC setting. Adjusting the VCO center frequency with the DAC "X" output current changes the VCO gain constant in a proportional manner. A second current, the DAC "1-X" current, IQP is used to offset this change by adjusting the Charge Pump gain proportional to "1-X", thus maintaining a reasonably constant loop gain.

Table 1: Output Clock Frequencies (where m is the VCO divisor and n is the CLKIN divisor)

CLKIN	*CDSEL*	*VCOCLK*	*IOCLK*	*CDCLK*
f_i	0 (2,7)	$f_o = f_i$ (m/n)	$f_o/2$	f_o
f_i	1 (1,7)	$f_o = 2f_i$ (m/n)	$f_o/3$	$f_o/2$

REFERENCE DAC

The reference DAC is a five-bit, current output digital to analog converter. The DAC are driven in parallel from Parallel Register A.

The I_{REXT} reference current is used internally to set the VCO center frequency and the Charge Pump gain as described in the section above. The VCO center frequency f_o (the DAC's "X" out-

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put current), and the charge pump gain current (the "1-X" current, I_{QP}), are given by the expressions below. R_{EXT} is the resistance value in ohms from the R_{EXT} pin to VEE and X is the decimal equivalent of the DAC input bits A_5 through A_9, with A_9 being the most significant bit, f_o (MHz) is the VCO center frequency and K_{VCO} (MHz/V) is the VCO gain.

$$I_{QP}\ (\mu A) = 0.878 \bullet 10^6 \bullet (5/3 - X/32) / (R_{EXT}\ [ohms])$$

$$f_o\ (MHz) = 0.23 \bullet 10^6 \bullet (2/3 + X/32) / (R_{EXT}\ [ohms])$$

$$K_{VCO}\ (MHz/V) = 0.38 \bullet f_o\ (MHz)$$

SERIAL REGISTERS

Data to program the DAC and programmable counters of the Frequency Synthesizer are loaded into the circuit through an 11-bit serial input register which consists of 11 D-type flip-flops. Data at the SDATA input is loaded into the serial register on the rising edge of the serial clock at pin SCLK when the serial register enable pin SENBL is LO. Data bit S_{10} is the most significant bit and is shifted in first. When pin SENBL is HI, inputs at pin SDATA and pin SCLK are ignored. All three serial interface signals, SDATA, SCLK, and SENBL, are TTL level signals.

Parallel Register A and Parallel Register B are 10-bit and 8-bit transparent latch type registers, respectively. Data is transferred from the Serial Register to one of the Parallel Registers on the rising edge of the serial enable signal at pin SENBL. Parallel Register A is loaded if bit S_{10} is LO and Parallel Register B is loaded if S_{10} is HI. The data in the unselected parallel register is unchanged by the load operation. Parallel Register B bits B_{00} through B_{07} are used to program the Divide-by-M. Parallel Register A bits A_{00} through A_{04} program the Divide-by-N counter and bits A_{05} through A_{09} program the 5-bit DAC. Data is transferred from the Serial Register, through the Parallel Registers, to the Divide-by or DAC circuits according to the Bit Assignment Table below.

Table 2: Register Bit Assignment

INPUT ORDER	*SERIAL BIT*	*S_{10} = LO PARALLEL A BIT*	*S_{10} = HI PARALLEL B BIT*
1	S_{12}	A_{12} --> Fault 1	
2	S_{11}	A_{11} --> Fault 0	
3	S_{10}	S_{10} = LO	S_{10} = HI
4	S_{09}	A_{09} --> DAC_4	x
5	S_{08}	A_{08} --> DAC_3	x
6	S_{07}	A_{07} --> DAC_2	B_{07} --> M_7
7	S_{06}	A_{06} --> DAC_1	B_{06} --> M_6
8	S_{05}	A_{05} --> DAC_0	B_{05} --> M_5
9	S_{04}	A_{04} --> N4	B_{04} --> M_4
10	S_{03}	A_{03} --> N3	B_{03} --> M_3
11	S_{02}	A_{02} --> N2	B_{02} --> M_2
12	S_{01}	A_{01} --> N1	B_{01} --> M_2
13	S_{00}	A_{00} --> N0	B_{00} --> M_0

The value of the DAC bits, (DAC_4 - DAC_0), are the same as register bits A_{09} - A_{05}. So, if a DAC value of sixteen is desired (A_{09} - A_{05}) = 10000. The N and M values are different, however. Since divide-by-zero is not possible, the divide-by-N or M is the decimal value of register bits (A_{04} - A_{00}) or (B_{07} - B_{00}) plus 1. For example, if N = 4 and M = 6 are the desired divide values, then (A_{04} - A_{00}) = 00011 and (B_{07} - B_{00}) = 00000101. This gives N = 3 + 1 = 4 and M = 5 + 1 = 6.

PIN DESCRIPTIONS

DIGITAL INPUT PINS:

SCLK: Serial register clock input, data is loaded from pin SDATA on each rising edge of SCLK while SENBL is LO, standard TTL levels.

SDATA: Serial register data input, data on this pin is loaded into the serial register on each rising edge of SCLK while SENBL is LO, standard TTL levels.

SENBL: Serial register enable, standard TTL levels. A LO input enables the loading of the serial register using pins SCLK and SDATA. Data is transferred from the serial register to one of the parallel register on the rising edge of SENBL. Inputs at SCLK and SDATA are ignored while SENBL is HI.

CLKIN, CLKINN: Reference frequency input. The differential ECL clock at these pins will be the reference frequency of the frequency synthesizer.

PDIN, PDINN: Phase/Frequency detector input. These differential ECL inputs will normally originate from the MDIV, MDIVN outputs. PDIN, PDINN inputs are selected when MDIVSEL is LO. If unused tie to MDIV/MDIVN or bias HI/LO within VIN range (VCC - 2.3V) to avoid oscillation.

MDIVSEL: A TTL input used to select the feedback input to the phase/frequency detector. MDIVSEL LO selects PDIN, PDINN inputs, allowing external or additional divide-by-M-counters to be added externally. MDIVSEL HI selects the divide-by-M counter output internally.

CDSEL: A TTL input used to select the code option. CDSEL LO = (2,7) code: HI = (1,7) code (code formats for disk drive data channels).

OSCSEL: A TTL input used to enable a VCO test feature. A LO level allows an external VCO frequency to be input into the divider blocks through the XOSC pin. A HI level allows normal operation.

XOSC: A TTL test VCO input pin. This input replaces the on chip VCO when the OSCSEL input is LO.

CSTN: A TTL input used to enable/disable the phase/frequency detector. A HI level enables the phase/frequency detector. A LO level shuts off the phase frequency detector and allows the VCO to coast.

DIGITAL OUTPUT PINS:

VCOCLK, VCOCLKN: Frequency synthesizer VCO output pins, used as the 3f clock for 1,7 code or 2f clock for 2,7 code by the disk drive read/write channel. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. The output levels are uncompensated ECL and should be used with a differential ECL receiver.

IOCLK, IOCLKN: VCO frequency divided output pins, used as the 1f reference clock by the disk drive read/write channel. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. The output levels are uncompensated ECL and should be used with a differential ECL receiver.

CDCLK, CDCLKN: VCO frequency divided output pins, used as the code rate (1.5f for 1,7 code or 2f for 2,7 code) reference clock by the disk drive read/write channel. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. The output levels are uncompensated ECL and should be used with a differential ECL receiver.

MDIV, MDIVM: CDCLK frequency divided by M. These pins are open emitter differential outputs, each requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not in use.

NDIV: Input frequency (CLKIN, CLKINN) divided by M. This pin is an open emitter ECL output, requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not is use.

UP: Active HI whenever the phase/frequency detector issues a pump-up to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not in use.

DN: Active HI whenever the phase/frequency detector issues a pump-down to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull-down resistor to VEE. This test output should be unconnected when not in use.

SRUS: The shift register unsafe fault pin, TTL levels. This pin will go low if a fault in the programmable M and N counter latches occurs due to an inadvertent static discharge to the drive. This pin normally sits high.

ANALOG PINS:

FREF, VCOIN: Differential loop filter pins for the frequency synthesizer's phase locked loop. The filter RC network is connected between these pins as shown in the Typical Connection Diagram. Pin FREF is a low impedance reference node with a voltage of 2.5 volts at nominal supply voltage. The VCO center frequency occurs when the voltage between pin FREF and VCOIN is zero. The dynamic range on pin VCOIN relative to pin FREF is ±0.75 volts. The VCO frequency can be controlled directly by forcing the voltage on VCOIN.

QPOUT: Charge pump output pin, outputs current into the loop filter. The current is controlled by REXT and the DAC setting. Under normal operation, QPOUT is shorted to VCOIN.

REXT: I_{REXT} reference current, the resistor R_{EXT} connected between pin REXT and VEE1 sets the current reference for the internal DAC that drives the frequency synthesizer's VCO and Charge Pump circuits. The voltage at pin REXT is approximately 1.17V.

SUPPLY PINS:

VCC: Digital power, +5.0 volts

VCC0: ECL emitter follower collector power, +5.0 volts

VCC1: Analog power, +5.0 volts

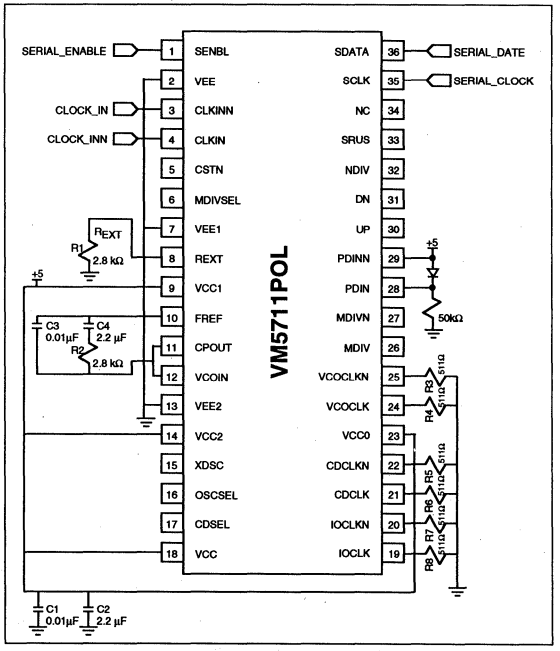
VCC2: VCO power, +5.0 volts

VEE: Digital ground

VEE1: Analog ground

VEE2: VCO ground

TYPICAL CONNECTION DIAGRAM



Resistor R_{EXT} is a ±1% absolute tolerance in value.

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DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ, $V_{CC} = V_{CC0} = V_{CC1} = V_{CC2}$. Refer to the typical connection diagram.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Currents						
Total Current		All ECL outputs open			130	mA
Digital Supply	I_{CC}	All ECL outputs open		77		mA
Analog Supplies	I_{CC1},I_{CC2}			15		mA
TTL Inputs (Note 2)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current High	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.5V			20	µA
		V_{IH} = 7V, V_{CC} = 5.5V (note 1)			100	µA
Input Current Low	I_{IL}	V_{IN} = 0.4V, V_{CC} = 5.5V			-0.6	mA
Clamp Voltage	V_{IK}	I_{IN} = -18mA, V_{CC} = 4.5V			-1.5	V
Differential ECL Inputs						
Common Mode Input Voltage	V_{CIM}		V_{CC} - 2.3		V_{CC} - 0.3	V
Differential Input Voltage	V_{INDIF}		200			mV
Input High Current	I_{NH}	V_{IH} maximum			25	µA
Input Low Current	I_{NL}	V_{IL} minimum			25	µA
Differential ECL Outputs (note 3)						
Voltage Output High	V_{OH}	T_{amb} = 0°C MECL 10KH Compatible	V_{CC} - 1.02 V_{CC} - 1.00		V_{CC} - 0.78 V_{CC} - 0.84	V
		T_{amb} = 25°C MECL 10KH Compatible	V_{CC} - 0.98 V_{CC} - 0.96		V_{CC} - 0.75 V_{CC} - 0.81	
		T_{amb} = 70°C MECL 10KH Compatible	V_{CC} - 0.92 V_{CC} - 0.90		V_{CC} - 0.66 V_{CC} - 0.74	
Voltage Output Low	V_{OL}	T_{amb} = 0°C MECL 10KH Compatible	V_{CC} - 1.95 V_{CC} - 1.95		V_{CC} - 1.63 V_{CC} - 1.65	V
		T_{amb} = 25°C MECL 10KH Compatible	V_{CC} - 1.95 V_{CC} - 1.95		V_{CC} - 1.63 V_{CC} - 1.65	
		T_{amb} = 70°C MECL 10KH Compatible	V_{CC} - 1.95 V_{CC} - 1.95		V_{CC} - 1.60 V_{CC} - 1.65	
Analog Pins						
DAC Bias	V_{REXT}	R_{EXT} = 2.8kΩ		1.17		V
Filter Bias	V_{FREF}	V_{CC} = 4.5V		2.45		V
		V_{CC} = 5.0V		2.50		
		V_{CC} = 5.5V		2.55		
VCO Input Range	V_{VCOIN}		1.75		3.25	V
Charge Pump Output Range	V_{QPOUT}		1.75		3.25	V
Charge Pump Current	I_{QP}	R_{EXT} = 2.8kΩ, DAC Setting = 10000	328	365	402	µA

Note 1: All TTL inputs except PWRDN pin. PWRDN pin has ESD protection diodes to both rails where as standard TTL inputs have protection to V_{EE} rail only.
Note 2: TTL inputs will float to a logic HI if left unconnected.
Note 3: All outputs denoted as ECL are +5V referenced track with the V_{CC} supply voltage. The following DC specifications assume VCC is +5V. Limits are specified after thermal equilibrium has been established.

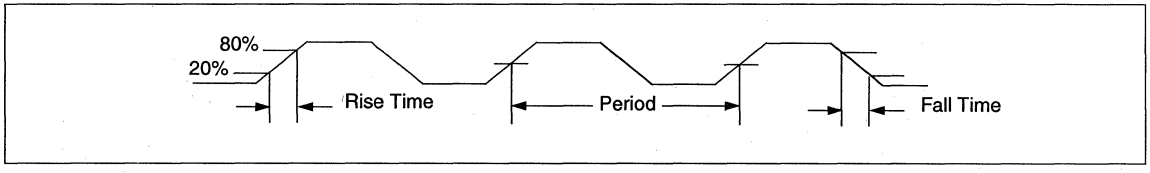
AC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, $C_3 = 0.01\mu F$, $C_4 = 2.2\mu F$, $R_1 = 2.8k\Omega$, $R_2 = 2.8k\Omega$, $V_{CC} = V_{CC0} = V_{CC1} = V_{CC2} = 5V \pm 10\%$, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCO Center Frequency	t_o	$R_{EXT} = 2.8k\Omega$, VCOIN and FREF pins connected together, DAC setting = 10000	86.4	96	105.6	MHz
VCO Dynamic Tuning Range			±28			%
VCO Gain	K_{VCO}	$R_{EXT} = 2.8k\Omega$, DAC setting = 10000, note 4	34.2	38	41.8	MHz/V
Output Rise Time	t_r	$f_o = 100MHz$	0.7		3.8	ns
Output Fall Time	t_f	$f_o = 100MHz$	0.7		4.4	ns
VCO Frequency Jitter	σ_{fVCO}	$f_o = 100MHz$, note 4 & 5		75		ps rms
Serial Registers						
SCLK Clock Rate					10	MHz
SDATA Setup Time			40			ns
SDATA Hold Time			5			ns
SENBL Setup Time			40			ns
SENBL Hold Time			40			ns
SENBL Pulse Time			200			ns

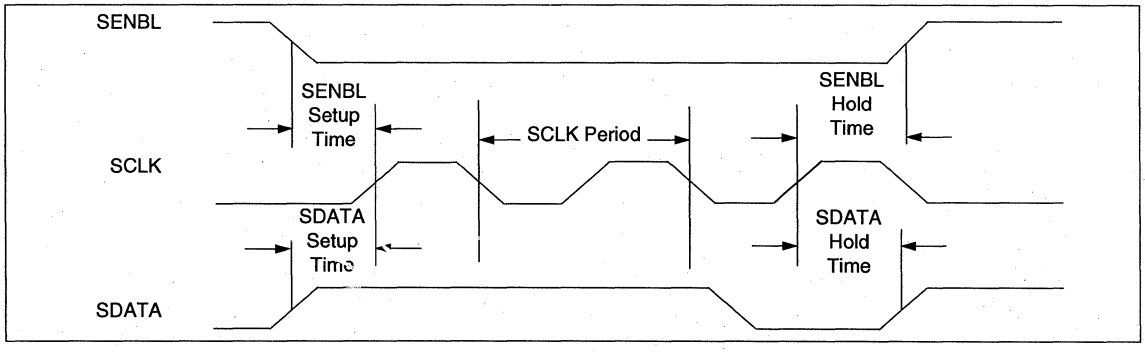
Note 1: Force VCOIN and measure frequency differentially between pins VCOCLK and VCOCLKN with the DAC register = 10,000. Calculate gain using KVCO = $(f_1 - f_0)$ / [VCOIN (f_1) - VCOIN (f_0)].

Note 2: VCOCLK output 1σ point measured over 10,000 samples on an HP5370B time interval counter. $\sigma_{fcl} = \sqrt{\sigma_a^2 - \sigma_b^2}$, where σ_a = rms jitter measurement and σ_b = self jitter of HP5370B (see HP app. note 191-4)

PHASE LOCK LOOP TIMING DIAGRAM



SERIAL REGISTER TIMING DIAGRAM



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Value the Customer™

VM64110
DIGITAL READ/WRITE CHANNEL

August, 1994

FEATURES

- Channel Rate Operation From 30 to 120 MHz
- Compatible With Any d = 0 RLL Code
- Full Support for Zone Density Recording
- Digitally Controlled VGA for Data and Servo Gain Control
- Digitally Controlled VFO with Zero-Phase-Restart for Clock Recovery
- Programmable Active Filter with Variable Cutoff and Boost
- 6-Bit 120 MSamples/s Flash ADC
- Optional Envelope Follower Servo Demodulation Mode
- Write Precompensation for Three, 3-bit Patterns
- Frequency Synthesizer with 8-Bit Divider Resolution
- Serial-Interfaced Control Registers with Readback Capability
- Power Management Features
- TTL Compatible Control I/O
- Differential ECL-Like Datapath I/O With Programmable Load
- Minimum Number of Off-Chip Discrete Components (5)
- Operation From a Single 5V Supply

DESCRIPTION

The VM64110 is the analog half of a digital read/write channel chip set for hard disk drive applications and can be used with any compatibly designed digital chip. The chip provides for a high degree of user programmability allowing the customization of the chip to suit any specific application.

The VM64110 is fabricated in VTC's PolarMOS process which offers high-performance bipolar and MOS devices for precision analog circuitry, and low-power CMOS technology for digital control functions. The VM64110 operates off a single 5-Volt supply and dissipates between 0.6W and 1.5W depending upon operating conditions. In the sleep mode the power dissipation is reduced to 2.5mW. The VM64110 is available in a 64-pin Plastic Quad Flatpack.

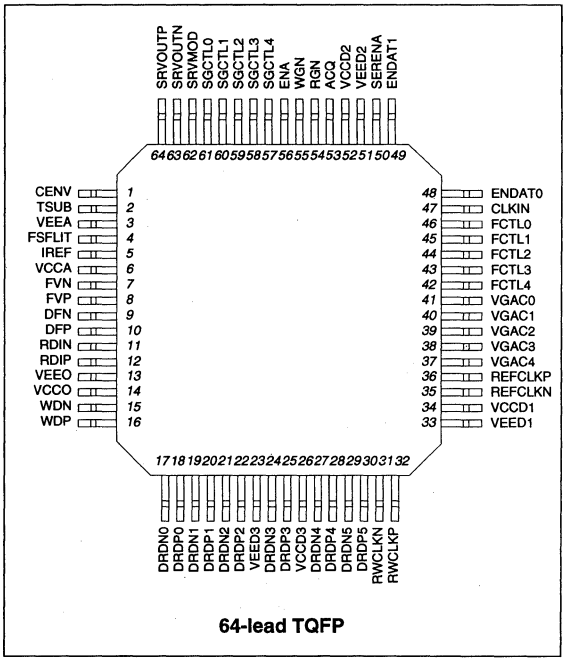
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
V_{CC} ..... -0.3V to +7V
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to +7V
Storage Temperature T_{stg} ..... -65° to 150°C
Junction Temperature T_J ..... 150°C
Thermal Impedance, Θ_{JA}
64-Lead PQFP ..... 40°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
Junction Temperature T_J ..... 0°C to 125°C

CONNECTION DIAGRAM



64-lead TQFP

FUNTIONAL DESCRIPTION

The chip receives differential analog read data input from a read/write preamp on pins RDIP and RDIN, and amplifies it with a digitally controlled variable gain amplifier (VGA). The five VGAC pins, along with five control register bits, control the gain of the VGA. The VGA output is equalized and filtered in a programmable active filter. The user specifies cutoff frequency and boost via the control register. The filter output is sampled by a 6-bit analog-to-digital converter (ADC). The sampling clock is generated by a digitally controlled variable-frequency oscillator (VFO) operating at the channel rate frequency. The 5-bit FCTL bus modulates the frequency of the VFO digitally. The ADC is output on the differential ECL DRD pins while the sampling clock is output on the read/write reference clock RWCLK, also differential ECL compatible. Signal swing on these pins is reduced to 0.5V from the standard 0.9V to reduce power dissipation. Offset through the datapath is minimized by the use of AC coupling capacitors on the filter output and an offset control word in the ADC.

A frequency synthesizer, composed of a charge-pump-based phase-locked loop, provides a reference for the VFO and generates the write reference clock output on RWCLK during write and idle mode. The center frequency for the voltage controlled oscillator (VCO) of the synthesizer is programmed by a digital-to-analog converter (DAC) which scales an external current provided by a resistor connected from V_{CC} to the IREF pin. Two

DATA RECOVERY CIRCUITS

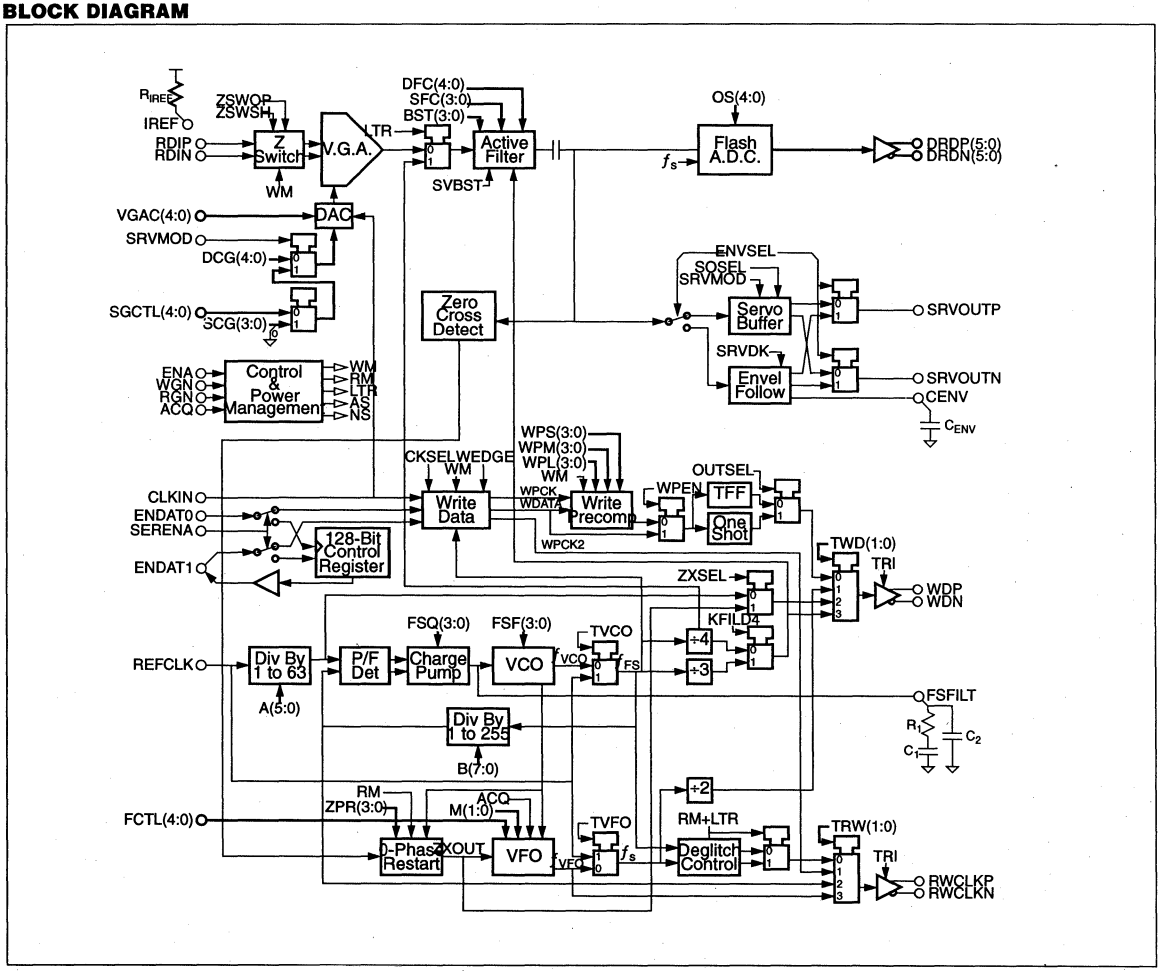
programmable dividers, A and B, allow the input frequency on the REFCLK pin to be multiplied up to the desired frequency with 8-bit resolution. The A and B dividers, the frequency DAC, and a DAC for the charge pump, are all programmed via the control register.

Write Precompensation for non-linear bit shift is provided for the 2-bit parallel write data inputs ENDAT1 and ENDAT0 and output on pins WDP and WDN. A parallel-to-serial conversion is made and a 3-bit pattern is detected. Three different user-programmable 4-bit DAC's control the shift for three unique patterns '010', '110', and '111'. The middle '1' is shifted late by an amount set by the corresponding DAC in the serial control register. A '011' pattern is uncompensated. Serial, precompensated write data is output on WD. A T-flip-flop may be optionally inserted into the output datapath.

Pin SRVMOD places the part in servo mode. A five-bit parallel interface on pins SGCTL(4:0) allows for direct control of the VGA DAC, overriding the serial coarse gain bits and disabling the VGAC fine gain inputs. Separate control bits for filter cutoff and boost are enabled. Pins SRVOUTP,N output the servo filter signal for off-chip demodulation. An optional envelope follower mode is enabled through the ENVSEL bit in the serial control register where the demodulated servo signal is output on the SRVOUTP pin along with appropriate reference voltages on the SRVOUTN pin. A zero-cross detector provides an edge for zero-phase restart corresponding to the positive zero-crossing of the filtered output.

The ENA pin provides for a Sleep mode, or an optional Nap mode, so that the chip can be put into a low power mode (<2.5mW). A Reset mode allows the chip to be reinitialized. A number of control register bits can disable the various blocks of the chip both independently and as a function of mode. The read gate and write gate pins, RGN and WGN, control the mode of the chip (Read, Write, or Idle). An acquisition pin ACQ specifies acquisition or tracking when in read mode and defines a lock-to-reference mode (LTR) when in idle. The serial enable pin (SERENA), along with the serial clock (SERCLK) and serial data pin (SERDAT), controls the loading and readback of the control register via the serial interface. Due to pin limitations, SERCLK and SERDAT are multiplexed with ENDAT0 and ENDAT1 respectively.

BLOCK DIAGRAM



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VTC Inc.
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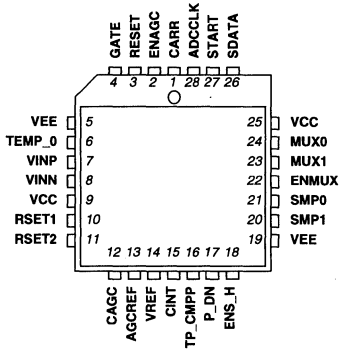
VM8050
DIGITAL AREA DETECTOR

ADVANCE INFORMATION August,1994

FEATURES
- 9-Bit DAC
- Track and Hold Circuitry
- Zero-Cross Detector
- Full-Wave Rectifier
- Low-Power Mode
- Typical Power Dissipation = 250 mW
- Adjustable AGC Reference
- Serial Digital Data Output
- 2.5V Reference for System Use
- Only Three External Components Needed for Operation

DESCRIPTION
The VM8050 Digital Area Detector (DAD) circuit takes a derived embedded servo burst signal, reads the area of the full-wave rectified version of the signal, and then does a 9-bit analog-to-digital conversion of that result. Since four servo bursts occur in quick succession, track and hold circuitry is used so that one servo burst can be processed simultaneously while tracking and holding the other three. The DAD chip is fabricated using VTC's high-performance Bipolar process and is supplied in a 28-lead PLCC package. Please contact VTC for other packaging options.

CONNECTION DIAGRAM



28-Lead PLCC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:
- V_{CC} ..... -0.5V to 7.0V
- V_{EE} 0V

Junction Temperature T_J ..... 0° to +150°C
Storage Temperature T_{stg} ..... -65° to 150°C
Thermal Impedance Θ_{JA}:
- 28-lead PLCC ..... 53°C/W

RECOMENDED OPERATING CONDITIONS

- V_{CC} ..... 4.65V to 5.35V
- V_{EE} 0V

Junction Temperature T_J ..... 0° to +100°C

DATA RECOVERY CIRCUITS

FUNCTIONAL DESCRIPTION

The VM8050 is made-up of two distinct sections - the area detector and the analog-to-digital converter (see block diagram). The purpose of the area detector is to integrate a servo burst for a fixed number of cycles and generate a proportional voltage on the capacitor connected to the CINT pin. The CINT value is stored in track and hold circuitry and digitized using a sucessive approximation analog-to-digital converter (ADC). This digitized value is then sent off-chip via the SDATA pin to external servo control logic. This procedure is repeated four times, once for each servo burst. Area detection and digitizing can be done simultaneously to increase the thru-put.

The area detector consists of the VGA transconductance stage (VGA_GM) and a charge pump/reset (CPRST) circuit. The carrier comparator, AGC_GM, and 2x-OPAMP (OP-2X) circuits also play important parts in the area detection operation. The ADC circuitry consists of track and hold (T/H) circuits, a multiplexer, decoding logic, and an ADC made up of an SAR, a 9-bit DAC, and a comparator. In addition to the above circuitry, general bias currents are provided by the BIAS cell and general voltages are supplies by a VREF cell. The VREF pin provides 2.5V externally for continuous system use. Finally, a majority of the circuits are powered-down via the P_DN pin. This feature can be used between servo sectors to reduce power consumption to a minimum.

The servo burst comes into the chip as a differential voltage on pins VINP and VINP, which come directly from the preamp outputs. The comparator cell, which is a high speed, high gain amplifier, receives this input signal and generates a digital representation with edges at the zero crossings of the input. The output of this block goes to the VGA_GM stage and comes out on the CARR pin. The CARR signal makes a level transition at every zero-crossing of an incoming servo burst signal and can be used externally to count the number of servo transitions.

The VGA_GM cell is a differential voltage to differential current amplifier with variable gain and full-wave rectification capabilities. The differential input voltage from the comparator cell is converted to differential current. The gain of the voltage to current amplifier is controlled by an external resistor (RSET) installed across pins RSET1 and RSET2 and the voltage on the CAGC capacitor. The gain is inversely proportional to RSET, which ranges from 1K to 5K ohms, and is proportional to the voltage on CAGC pin, which has a range of 1.3V to 2.3V. The voltage on the CAGC pin modifies the differential voltage to differential current gain such that the gain when VCAGC = 2.3V is typically five times the gain when VCAGC = 1.3V. The assertion of the ENAGC pin causes the voltage on CAGC to be increased or decreased depending on the AGCREF and CINT voltages. The voltage at AGCREF is doubled by the OP-2X block and compared to CINT. If CINT is smaller, CAGC will be pumped up and if CINT is larger, CAGC will be pumped down. The ENAGC pin when disabled (low), will cause the CAGC pin to become high impedance. The comparison and charge pumping of CAGC is done by the AGC_GM cell.

The OP-2X cell is a voltage amplifier with a fixed gain of two. The AGC_GM cell is a differential voltage to single-ended current (charge pump) amplifier with a nominal gain (gm) of 0.02 mhos (Siemens). The input voltage to the AGC_GM block is the difference between the output of the OP-2X (2X) and the voltage on CINT. Thus, the current delivered to pin CAGC equals 0.02x (VCINT - 2X), where a positive current is into CAGC.

Full-wave rectification is accomplished in the VGA_GM block by driving a Gilbert cell multiplier with the digital carrier generated by the comparator cell.

The charge pump/reset block (CPRST) takes the full-wave rectified differential current from the VGA_GM cell and converts it into a single-ended current source that pumps up the integrating capacitor CINT. The voltage on CINT equals the integral of the single-ended current, (i.e. $VCINT = C_{CINT}\int idt$). The GATE pin, which is an active high input, is used to enable or disable the current source. The charge pumping occurs when GATE is asserted. The GATE is internally synchronized to the zero crossings of VINP/VINN by a signal from the comparator block.This ensures that the charge pumping occurs only for an equal integral number of cycles every time a servo burst is measured.

The CPRST cell also performs a reset function. When RESET is brought high, the voltage on CINT is forced to an initial voltage of 0.8V by an amplifier with 7 mA (typical) of available current. This is the only use for RESET on this chip.

The voltage on the CINT pin, which runs between 0.8V to 2.8V, is tracked by one of the four track and hold (T/H) circuits as selected by the SMP1, SMP0, and ENS_H pins. There are four T/H cells corresponding to CINT values for each servo burst. They are unity gain buffers with an internal hold capacitor at their outputs. When ENS_H is high, the selected T/H circuit is in tracking mode and the output of the T/H cell tracks the input. The remaining three T/H circuits are in hold mode regardless of the state of ENS_H. When ENS_H is deselected, the CINT value is stored on an internal capacitor as VHOLD.

ADC operation begins by selecting one of the VHOLD values using the MUX0, MUX1, and ENMUX pins, and then pulsing the START line during the falling edge of ADCCLK. Capturing the START pulse constitutes the beginning of the conversion process. The ADC in the VM8050 is a successive approximation type using a 9-bit DAC, a comparator, and a SAR register. The selected VHOLD voltage and the DAC voltage are compared internally to gauge weather the respective SDATA bit should be set or reset. This continues for nine cycles, one for each DAC bit.

The total analog-to-digital conversion will take 10 ADCCLK cycles to complete plus one more for reset. The eleventh clock resets the SDATA line, otherwise it stays at what state B0 is in until the start of the next conversion. SDATA (serial data) is clocked out of the chip after the falling edge of the second ADCCLK cycle, and will be valid at the next rising edge of the ADCCLK. The servo system must store each SDATA bit as they occur since they may change at each successive ADCCLK. From there, the system has to convert the externally stored 9-bit SDATA code word into a voltage relative value using the fact that CINT ranges from .8V (SDATA = 000000000) to 2.8V (SDATA = 111111111), with a mid-range value of 1.8V. The accuracy of the SAR ADC is 4mV/bit. The relationship between VCINT and SDATA is shown below (see figure 3):

$$VCINT = .004(SDATA_{10}) + 0.8V$$

Figure 4 shows a typical conversion using a VCINT value of 2.2V which should correspond to a SDATA value of 350.

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PIN DESCRIPTIONS

PIN NAME	*PIN #*	*TYPE*	*I/O*	*DESCRIPTION*
CARR	1	TTL	Output (O.C.)	CARR is the output of the comparator. CARR makes a level transition at every zero-crossing of an incoming servo burst signal. Note that CARR will be indeterminate when the servo burst amplitude is low.
ENAGC	2	TTL	Input	When high, ENAGC enables the AGC loop transconductance amplifier. ENAGC should be asserted subsequent to integration of the AGC portion of the servo burst.
RESET	3	TTL	Input	A logic high, on RESET enables the area detector reset transconductance amplifier and asynchronously clears the GATE re-synchronizing flip-flop. The area detector must be reset prior to a servo burst integration operation.
GATE	4	TTL	Input	Asserting this pin enables the area detector to measure the area of the servo burst signal delivered by the VGA_GM block. Note that GATE is re-synchronized to the rising edge of the area detector carrier (CARR) by an on-chip flip-flop prior to application of the gate to the area detector. For proper operation, GATE must be asserted by external logic for a constant number of cycles of the input servo burst signal. See Figure 2.
VEE	5, 19	Ground	—	This pin has no potential
TEMP_D	6	Temperature Diode String	—	This pin is the anode of the first of four series-connected diodes (referenced to ground) that are meant for use for thermal analysis. It should remain open during normal operation.
VINP, VINN	7, 8	Differential Analog	Input	Differential input signals to the VGA. They must be capacitively coupled to the read channel analog output.
VCC	9, 25	—	Power	+5V
RSET1, RSET2	10, 11	—	—	Pins for external Gain-Setting Resistor (RSET). This resistor adjusts the range of allowable input voltages by changing the gain of the AGC center point.
CAGC	12	Analog	—	The AGC loop compensating capacitor is connected between this pin and ground. The voltage across this capacitor controls the VGA gain directly.
AGCREF	13	Analog	Input	The set point of the on-chip area-regulating loop is established by the voltage applied to the AGCREF pin. The voltage applied to this pin is multiplied by two, then applied as a set point to the AGC loop.
VREF	14	Analog	Output	VREF delivers the buffered output of a 2.5v bandgap reference and is available for use elsewhere in the servo system.
CINT	15	Analog	—	The area detector integrating capacitor is connected between this pin and ground. The voltage across the CINT capacitor at the end of a burst integration measures the area of that burst.
TP_CMPP	16	CML	Output	Test Pin - B-Level CML Output of the ADC Comparator. This pin shows the status of the ADC at each conversion point and should be pulled down with a 3k resistor. In normal operation, this pin should remain unconnected.
P_DN	17	TTL	Input	Asserting P_DN (power down) causes the VM8050 to enter a low power mode. In this mode, all circuits, except the bandgap reference, are biased down. The VREF voltage is delivered at its normal level during both the normal and low power modes. Other chip output signals will become indeterminate during low power mode. To conserve system power, P_DN may be asserted between servo sectors. Note VINP/N float high during power down mode.

PIN DESCRIPTIONS

PIN NAME	*PIN #*	*TYPE*	*I/O*	*DESCRIPTION*
ENS_H	18	TTL	Input	Asserting ENS_H establishes track mode in the track & hold channel selected by the SMP0 and SMP1 pins. Tracking is maintained as long as ENS_H remains asserted.
SMP1, SMP0	20, 21	TTL	Inputs	The code applied to these pins determines which track & hold channel is set to the track when ENS_H is asserted. All other track & hold channels remain in the hold mode, irrespective of the state of ENS_H. The channel selected versus SMP1 and SMP0 settings are shown below: ***SMP1*** ***SMP0*** ***SELECTED BURST*** 0 0 A 0 1 B 1 1 C 1 0 D
ENMUX	22	TTL	Input	The analog multiplexer is enabled by asserting ENMUX. The multiplexer must be enabled prior to an ADC operation and must remain enabled until the ADC operation is complete. To minimize bias current induced droop on the track & hold capacitors, a given multiplexer channel should be enabled only for the course of the ADC operation on that channel.
MUX1, MUX0	23, 24	TTL	Input	The code applied to these pins determines which track & hold channel output is connected to the ADC when ENMUX is asserted. The channel selected versus MUX1 and MUX0 settings are shown below: ***MUX1*** ***MUX0*** ***SELECTED BURST*** 0 0 A 0 1 B 1 1 C 1 0 D
SDATA	26	TTL	Output (O.C.)	This serial data pin delivers the result of the ADC operation in bit-serial form, MSb first. SDATA changes state on the falling edge of ADCCLK.
START	27	TTL	Input	When START is pulsed during a falling edge of the ADCCLK, the ADC operation sequence is initiated. The start pulse should be only 1 ADCCLK period long.
ADCCLK	28	TTL	Input	The ADCCLK pin must be pulsed ten times for each ADC operation. The falling edge of the first pulse, issued when START is a logic high, initiates the ADC operation. The falling edge of each of the subsequent nine pulses causes conversion of a single bit of the digital code representing the analog voltage applied to the input of the ADC (via the mux). Note that the input of the ADC must be held constant throughout the ADC operation.

DC CHARACTERISTICS Unless otherwise specified, V_{CC} = 5V ±10% and T_A = 0° to 70°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
TTL INPUT/OUTPUT BUFFERS						
Input Voltage Low	V_{IL}				0.8	V
Input Voltage High	V_{IH}		2.0			V
Output Voltage Low	V_{OL}	O.C. - 2k to VCC load			0.4	V
Output Voltage High	V_{OH}	O.C. - 2k pullup to VCC	V_{CC} - 0.2			V
CARRIER COMPARATOR						
Gain		With respect to VINN/VINP	55			dB
Offset					3.0	mV
POWER DOWN						
Startup Time		P_DN false to chip ready			5.0	µs
Supply Current		Normal mode			TBD	mA
Supply Current		Power down mode			TBD	mA

DC CHARACTERISTICS Unless otherwise specified, V_{CC} = 5V ±10% and T_A = 0° to 70°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VGA AND AGC AMPLIFIER						
VINP/VINN Differential Input Voltage Range	V_{VIN}		0.30		3	Vp-p
Input Resistance	R_{IN}		10			kΩ
Input Capacitance	C_{IN}			10		pF
Noise		Bandwidth 20MHz			20	nV/√Hz
Bandwidth		-3dB, with VINP/VINN capactively coupled to the source	20			MHz
AGC Gain Range		Higher voltages on CAGC pin result in higher gain	1:4	1:5	1:6	
CAGC Leakage Current		With 2x op amp gated off			500	nA
AGC Gm Amplifier Transconductance				0.019		Siemens
AGC Gm Amplifier Output Current			500			µA
AGC Gm Amplifier Turn Off Time					50	ns
AGCREF Pin Bias Current				1		µA
Ratio at AGC Equilibrium		Between CINT output voltage and AGCREF input voltage		2		V/V
AGCREF Pin Voltage In			0.4		1.4	V

DC CHARACTERISTICS Unless otherwise specified, V_{CC} = 5V ±10% and T_A = 0° to 70°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
AREA DETECTOR						
Output Voltage			0.8		2.8	V
Signal Current Into CINT With GATE Enabled			600			µA
Unbalance Current					10	µA
CINT Leakage Current From Integrator		RESET off, GATE off			100	nA
CINT Reset Current			TBD			mA
CINT Reset Potential			TBD	0.8	TBD	V
CINT Reset Time to 1/2 LSB		CINT capacitor = 200pF, initial voltage = full-scale saturated			200	ns
Reset		Gm amplifier turn-off time			50	ns
GATE Setup Time Relative to CARR Rising Time			10			ns
GATE Hold Time Relative to CARR Rising Edge			0			ns
SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER						
Resolution			9			Bits
Differential Linearity		No missing codes	-1		+1	LSB
Zero Code Voltage		Output code hex 0		0.8		V
Full Scale Code Voltage		Output code = hex 1FF		2.8		V
START Setup Time		Relative to ADCCLK falling edge	10			ns
START Hold Time		Relative to ADCCLK falling edge	0			ns
ADCCLK Low Pulse Width			60			ns
ADCCLK High Pulse Width			60			ns
ADCCLK Period			200			ns
Clock Cycles per Conversion				10		
Time From Falling Edge of ADCCLK to SDATA Valid					30	ns
LSB Quantum				3.91		mV
BANDGAP REFERENCE						
VREF Voltage			TBD	2.5	TBD	V
VREF Sink Current			1			mA
VREF Source Current					-3	mA
VREF Output Resistance					10	Ω
TRACK AND HOLD AND ANALOG MULTIPLEXOR						

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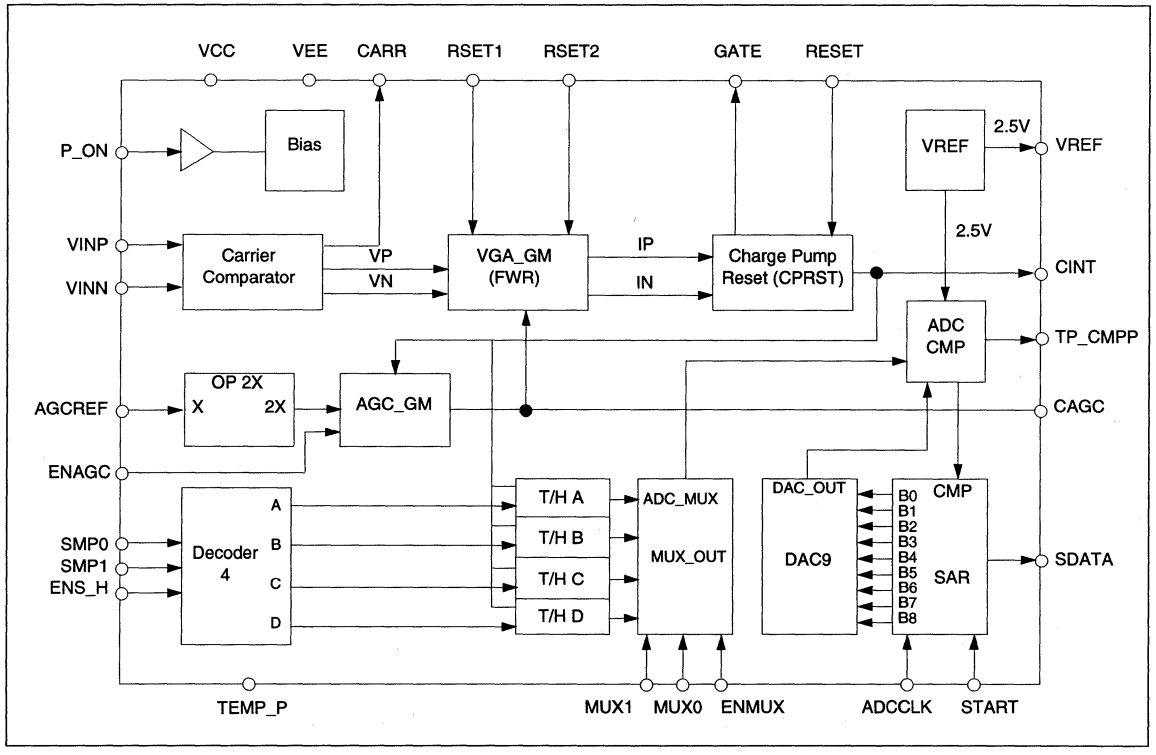
DC CHARACTERISTICS Unless otherwise specified, V_{CC} = 5V ±10% and T_A = 0° to 70°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Acquisition Time		Full scale step input to ±12 LSB			400	ns
Droop Rate		Hold mode with multiplexor not selected			(1.8)/2	LSB/µs
		Hold mode with multiplexor selected			(1/2)/2	
Track and Hold Input Bias Current in Track Mode					500	nA
Track and Hold Input Bias Current in Hold Mode					100	mA
Track-to-Hold Transition Time					20	ns
Gain				1		V/V
Channel Offset Mismatch					TBD	mV

BLOCK DIAGRAM



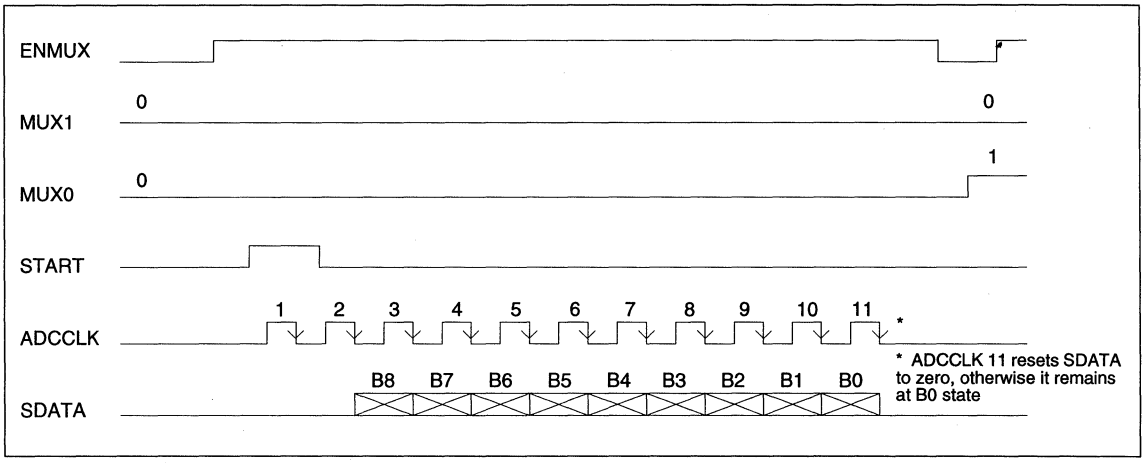


Figure 1: General ADC Conversion Operation

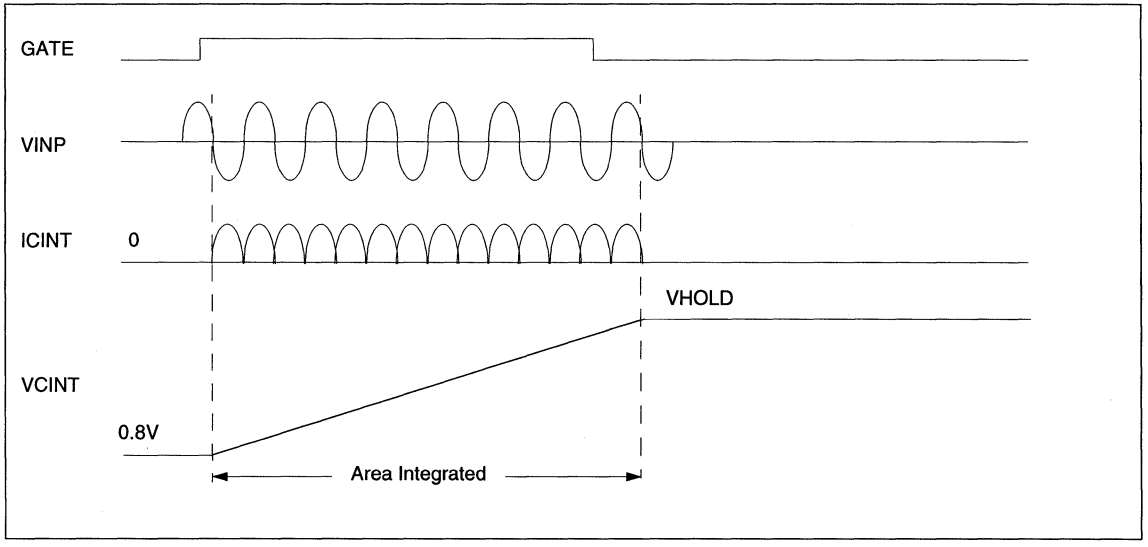


Figure 2: Intergration Operation

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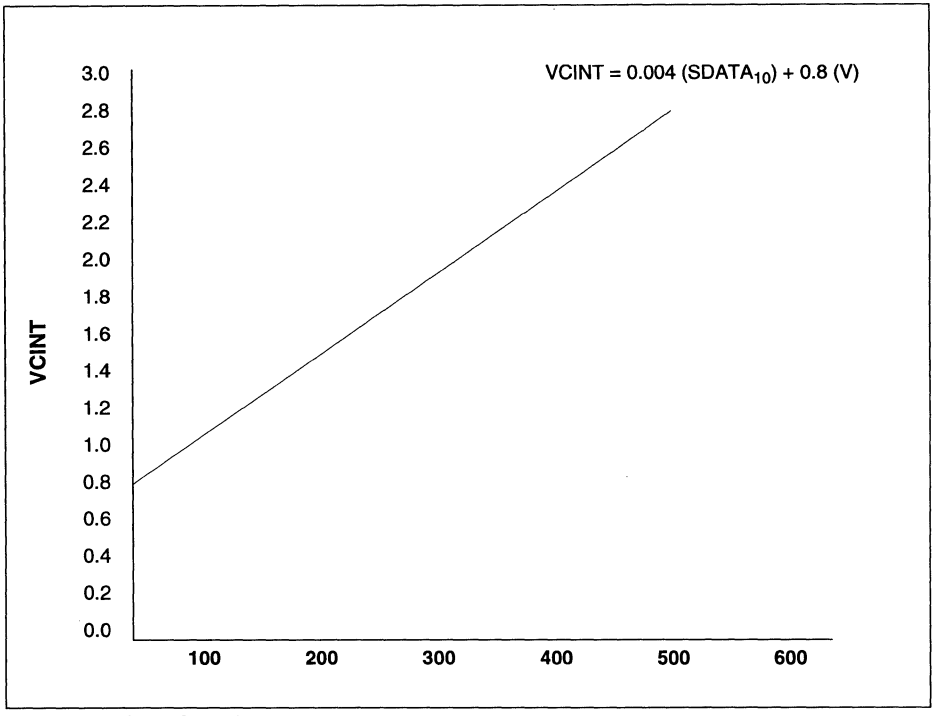


Figure 3: CINT vs SDATA

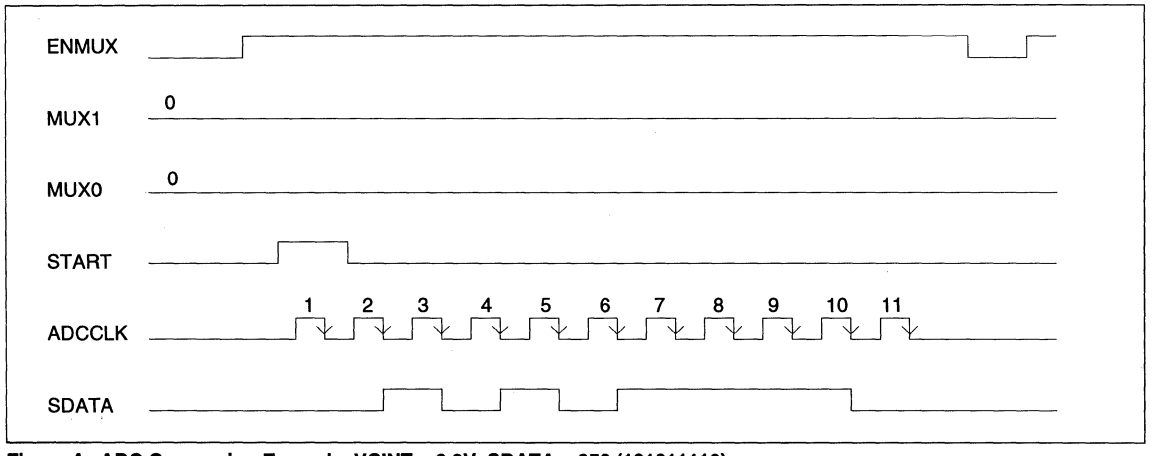


Figure 4: ADC Conversion Example, VCINT = 2.2V, SDATA = 350 (101011110)

6 Tape Drive Circuits

VTC Inc.
Value the Customer™

VM5353
DATA SEPARATOR

August,1994

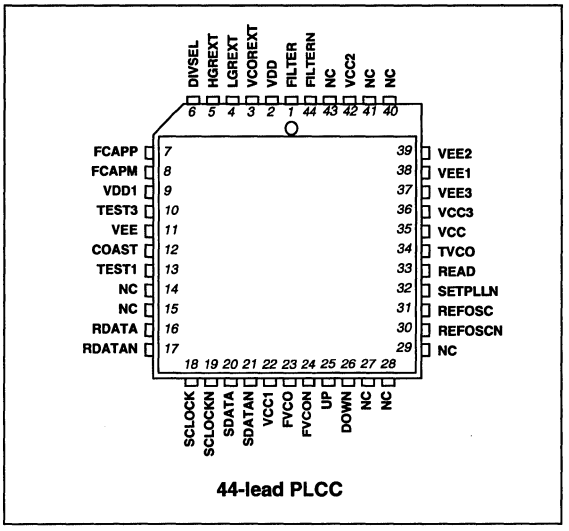
FEATURES

- Operates at Data Rates from 10 to 48 Mbits/sec (2,7) Code
- Operates at Data Rates from 10 to 64 Mbits/sec (1,7) Code and (0,3) Codes
- Static Window Error Less Than 500 pS
- Zero Phase VCO Restart for Rapid Data Lockup
- Internal Silicon Delay Line
- Compatible with Zoned Density Recording Applications
- Contains Internal Window Marginalization Circuitry
- User Determined PLL Loop Filter Network
- Dual Gain PLL With External Control of PLL Loop Bandwidth
- PLL Free Run (Coast) Control
- Power Dissipation Less Than 1W
- VM5353 has Power Supplies of +5V and +12V

DESCRIPTION

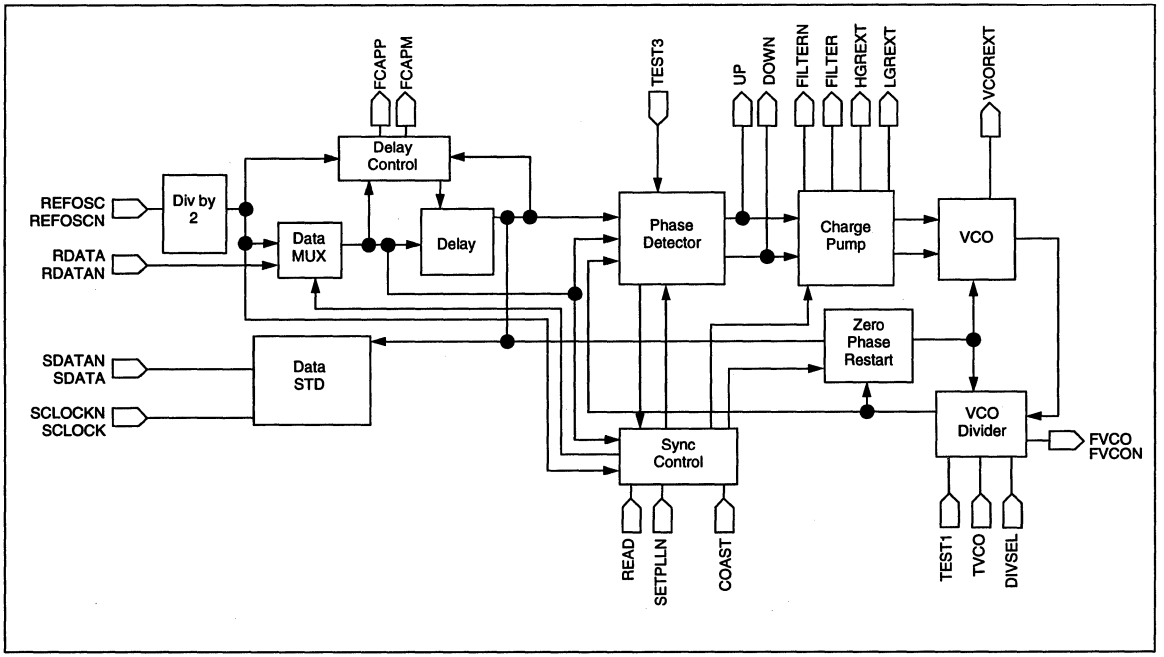
The VM5353 is an integrated circuit designed to be used in high-performance data recovery systems. The data separator is a phase locked loop which provides a stable read clock of up to 96 MHz for system timing during the disk readback operation. It tracks the slow variations in the data frequency while eliminating noise and peak shifting in the data. The circuit will operate with either the (2,7), (1,7) or (0,3) RLL codes. The VM5353 uses the high-speed CBP (Complementary Bipolar Process).

CONNECTION DIAGRAM



44-lead PLCC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

VM5353

Storage Temperature ..... -65° to +150°C
Ambient Operating Temperature ..... 0° to +70°C
Junction Operating Temperature ..... 0° to +125°C
Supply Voltage,
V_{CC} (V_{EE} = 0V, V_{DD} = 12V) ..... -0.5V to +6.5V
Voltage Applied to
TTL Inputs (V_{EE} = 0V) ..... -0.5V to V_{CC} +0.5V
ECL Inputs (V_{EE} = 0V) ..... 0 to V_{CC}
ECL Output Current - Continuous 25mA
- Surge 50mA
Maximum Power Dissipation 1300mW
Thermal Impedance, 44-lead PLCC
Junction-to-Case, Θ_{JC} ..... 10°C/W
Junction-to-Ambient, Θ_{JA} ..... 53°C/W

READ OPERATION

There are three states in the read PLL locking sequence:

1. Lock to the reference oscillator
2. Lock to the preamble data in high gain
3. Lock to data in low gain.

Initially, the data separator locks to the REFOSC input. This is a standby state which the data separator is in when not reading data. The VCO runs at a frequency which is very close to that required when locking to the data stream. This minimizes the frequency step when the PLL input is switched to data. In this state of operation, the phase detector is in the phase/frequency mode which guarantees non-harmonic lock up. The charge pump is sourcing high-gain currents. The higher loop gain ensures rapid lock of the PLL.

The assertion of the READ gate initiates the read operation. Internally, the part waits for the first data bit and then switches the input to the PLL from REFOSC to RDATA. At this time, the VCO is momentarily stopped and restarted in phase with the first data bit in the preamble. This allows very fast and repeatable lockup to the preamble field. The loop is still in a high gain mode so any remaining phase error is due to the zero phase restart is quickly tracked out. The phase detector is in a phase mode which allows the PLL to lock to harmonics. This also allows great flexibility in the preamble pattern. The user could actually lock up in the middle of a data field if so desired. The length of the preamble lock is controlled externally by the SETPLLN input.

After the preamble lock-up is over, the PLL switches to the lock-to-data mode and the data is read. In this mode, the charge pump is sourcing low-gain currents. This forms a low-gain loop which is desirable for reading data. The loop becomes less responsive to bit shift in the data stream.

When the read operation is complete, READ gate is brought high, a zero phase restart of the VCO is performed and the PLL locks to the reference oscillator once again. Refer to Figure 1 for Read Timing Diagrams.

CIRCUIT BLOCK DESCRIPTION

The circuit is composed of the following functional blocks: high-precision phase-frequency detector, differential charge pump, differential input VCO, filter, zero phase VCO restart, divider, data standardizer and synchronization control block. Refer to the block diagram.

SYNC Control

The sync control block controls the input multiplexer, the phase/frequency detector, the charge pump gain and the divider setting. It guarantees that the phase locked loop switches smoothly from one mode to another. The control pin setting and corresponding modes are summarized in the table below.

READ	*SETPLLN*	*GAIN*	*MUXSEL*	*DIVIDER*	*PHASE/FREQ DET*
1	X	High	REFOSC	div by 4	Phase/Freq. Mode
0	X	Low	DATA	div by 2	Phase Mode
1	X	High	REFOSC	div by 4	Phase/Freq. Mode
0	1	High	DATA	div by 2	Phas Mode
0	0	Low	DATA	div by 2	Phase Mode

1 = Logic HI, 0 = Logic LO, X = Don't Care

This table shows that the high-to-low gain switch is controlled externally by the SETPLLN pin. The above table assumes that DIVSEL is LO, meaning that the extra divide-by-two is not in the VCO feedback path.

Delay Line

The VM5353 uses an internal delay line to delay the data coming into the phase detector. The delay allows the phase detector to anticipate incoming data and enable a phase comparison to occur. The delay is nominally one half of the REFOSC period. A separate control loop regulates the propagation delay through the delay line by comparing it to the REFOSC frequency. This delay line configuration relies only on the REFOSC frequency and is insensitive to external components, supply voltage, temperature and IC processing. It requires that the reference oscillator frequency be present at all times and that there be no extended gaps in the data when READ gate is active.

Data Mux and Phase/Frequency Detector

The two highest frequency inputs to the data separator are the REFOSC and the RDATA pins. The REFOSC pin is tied to an external reference oscillator or servo reference. The PLL locks to the REFOSC input when no data is being read from the disk. The REFOSC signal must be present all times because it is used in the anticipator delay circuitry. The RDATA pin is the input for the raw data and is tied to the output of the pulse detector circuit in the disk drive. Because these two signals are the highest frequencies coming onto the chip, they are differential ECL inputs. This helps reduce unwanted coupling of these signals into the PLL. A multiplexer DATA MUX is used to select which input (REFOSC or RDATA) the PLL will lock to.

The output of the anticipator delay goes to the PLL input of the phase/frequency detector (PFD) block. The phase/ frequency detector has two modes of operation, the phase/frequency mode and phase mode. Each mode is described below.

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The phase/frequency mode allows the phase detector to detect both phase and frequency of the two incoming signals. This mode does not allow the PLL to lock to harmonics of the reference input. The phase/frequency mode is used along with the charge pump high gain mode and the filter high bandwidth mode to form a high gain-high bandwidth loop for fast lock up times. This mode is used when locking to the reference oscillator and the preamble. The reference input to the PFD initiates an UP signal to the charge pump, and the VCO feedback input initiates a DOWN signal to the charge pump. When both UP and DOWN are high, the internal flip-flops are reset and the signals return low again. The minimum pulse width of the UP and DOWN signals is determined by internal propagation delays and is approximately 5 ns. In a locked state, the rising and falling edges of the UP and DOWN signals are coincident and there is no net effect on the PLL phase and frequency.

When in the phase mode, the PFD detects only the phase of the two inputs. The phase mode is used whenever READ gate is asserted. The anticipator delay value is one half a REFOSC period window and is used to condition the phase detector for a phase comparison. The operation of the phase detector is the same as in the phase/frequency mode except that a phase comparison cannot be initiated until a data pulse is input to the phase detector. This allows to the PLL to lock to harmonics of the VCO frequency.

Charge Pump

The charge pump uses high speed NPN and PNP switches to source current in and out of the FILTER pin. The UP and DOWN signals from the phase detector feed into the charge pump and cause it to pump current in or out of the differential lead-lag filter. The high speed current switches in the charge pump sink or source current out of the FILTER pin, as determined by the UP and DOWN inputs. The FILTERN side of the filter acts as a voltage source. The high and low gain current are set by external resistors connected to the HGREXT and LGREXT pins. The high gain current can be varied from 0.5 to 2.0 mA by adjusting the HGREXT resistor. The low gain current can be varied from 100 to 400 µA by adjusting the LGREXT resistor. This allows the user to vary the high gain/low gain current ratio from 20:1 to 5:4.

Filter

The filter resides external to the chip, allowing the system designer to control the loop dynamics. It is composed of two capacitors and one resistor. Refer to the VM5351/VM5352/VM5353 Application Note.

VCO

The VCO is a multivibrator type oscillator which has good linearity over its frequency range. The differential voltage between the FILTER and FILTERN pins controls the VCO frequency. The VCO center frequency occurs when the differential voltage across FILTER and FILTERN is zero. An external resistor tied from the VCOREXT pin to VEE sets the VCO center frequency and gain.

Divider

The divider block divides down the VCO frequency. It is composed of several divide-by-two sub blocks which can be switched in and out. The VCO frequency is split into to separate signals which are divided down individually. One of the divided VCO signals is routed to the data standardizer. This is a straight divide-by-two at all times. The other divided VCO signal wraps around back into the phase-frequency detector to complete the loop. This division is switchable from a divide-by-two to a divide-by-four. The VCO divided-by-two is used when the phase-frequency detector is in the phase (harmonic) mode. The VCO divided-by-four is used when the phase-frequency detector is in the phase-frequency mode and the PLL is locking to REFOSC. This matches the REFOSC divided-by-two frequency. Refer to the block diagram.

The DIVSEL pin can be used to insert an extra divide-by-two into the front end of the divider block to extend the lower end of VCO range without changing the VCOREXT resistor. This is used when operating at lower data rates ($f \leq 15$MBS).

The divider block can be put into a test mode by forcing the TEST1 pin to a logic low. This switches an internal mux that allows an external frequency to be injected into the divider through the TVCO input pin.

Data Standardizer

The divided VCO clock and data input to the PLL contain clock and data information needed but are not synchronized to one another. For this reason, they are put through a data standardizer which takes out any bit shift in the data and puts the bit in a decode window. The data standardizer uses the falling edge of the divided VCO clock to generate the decode window. The rising edge of the clock output SCLOCK is centered in the middle of the synchronized data output SDATA. The rising edge of the SCLOCK indicates the data is valid and clocks the data bit into the decoder circuitry of a decoder IC. The SCLOCK and SDATA outputs are differential ECL signals. A Synchronized Data and Clock Timing Diagram is shown in Figure 2.

Zero Phase Restart

A zero phase restart of the VCO is performed both when switching from the reference oscillator to data and vice versa. The loop is in a high gain mode whenever a zero phase restart occurs. This allows fast lockup to the preamble field and when going back to the idle state. The zero phase restart block interfaces to several other blocks on the chip and guarantees a sequence of events when the switch happens. No spurious data or clock signals will occur when READ gate is switched. Timing diagrams for the VCO Zero-Phase Restart are shown in Figure 3.

Zoned Density Recording

The VM5353 can be used with zoned density recording. The synthesized frequency is brought into the REFOSC input. Different values for the VCOREXT resistor must be switched in and out using an external analog switch when changing the VCO center frequency. A zero temperature coefficient current DAC will not work well to set up the VCO center frequency. This is because the VCO requires a negative temperature coeficient current to give a constant VCO frequency over temperature.

PIN DESCRIPTIONS

DIGITAL INPUTS:

REFOSC, REFOSCN: Reference oscillator which the PLL locks to when in the idle state. A differential ECL input. REFOSC frequencies for the different data rates and codes are:

DATA RATE - f	*1/2 (2,7) - 2f*	*2/3 (1,7) - 1.5f*
64 Mbits/sec	—	96 MHz
48 Mbits/sec	96 MHz	72 MHz
30 Mbits/sec	60 MHz	45 MHz
25 Mbits/sec	50 MHz	37.5 MHz
20 Mbits/sec	40 MHz	30 MHz
15 Mbits/sec	30 MHz	22.5 MHz
10 Mbits/sec	20 MHz	15 MHz

REFOSC minimum pulse width high and low: 4ns. The duty cycle of REFOSC is not critical.

RDATA, RDATAN: Encoded read data from the disk drive read channel, active high. RDATA minimum pulse width: 4ns. A differential ECL input.

READ: A TTL control input which when low initiates lock up to data. When high, the PLL is in an idle state and locks to the REFOSC signal.

SETPLLN: A TTL input which when activated in conjunction with READ gate determines the bandwidth mode of the PLL.

COAST: A TTL input which controls the coast function on the data separator. When the coast input is a logic low, the phase detector is cleared and held in a reset state, allowing the VCO to coast regardless of the incoming data. This happens synchronously within the circuit. When a logical high, the phase detector operates normally.

COAST	MODE
Tied to V_{EE}	VCO coast
Floating	Normal operation

DIVSEL: An input used to switch in and out an extra divide-by-two in the VCO divider block. The extra divide by two can be used to extend the low end frequency range of the VCO.

DIVSEL	MODE
Tied to V_{EE}	Extra divide by two switched out. (f_o above 60MHz)
Floating	Extra divide by two switched in. (f_o below 60MHz)

TEST1: An input used to enable a test feature on the data separator. When enabled, it allows an external VCO frequency signal to be injected into the divider block through the TVCO pin. For test purposes only.

TEST1	MODE
Tied to V_{EE}	External VCO frequency injected into divider block.
Floating	Normal operation

TEST3: An input used to enable a test feature on the data separator. When enabled, it forces the phase detector into a phase-frequency detector at all times. For test purposes only.

TEST3	MODE
Tied to V_{EE}	Phase detector in phase frequency mode at all times.
Floating	Normal operation

TVCO: The test VCO input pin. This input is enabled by the TEST1 control pin. This is a TTL input.

DIGITAL OUTPUTS:

SDATA, SDATAN: Encoded data read from the disk which is synchronous with the falling edge of the Data Clock. SDATA is active high. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. A differential ECL receiver should be used to receive the signal.

SCLOCK, SCLOCKN: Data clock output referenced to the VCO which is synchronous with the Synchronized Data. The rising edge of SCLOCK indicates the presence of valid data on SDATA. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. A differential ECL receiver should be used to receive the signal.

FVCO, FVCON: Output frequency of the VCO available for data decoding. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. The outputs should be allowed to float when not needed. A differential ECL receiver should be used to receive the signal.

Nominal FVCO output frequencies for the specified data rates and coding schemes are given below.

DATA RATE - f	*DIVSEL*	*1/2 (2,7) - 4f*	*2/3 (1,7) - 3f*
64 Mbits/sec	V_{EE}	———	192 MHz
48 Mbits/sec	V_{EE}	192 MHz	144 MHz
30 Mbits/sec	V_{EE}	120 MHz	90 MHz
25 Mbits/sec	V_{EE}	100 MHz	75 MHz
20 Mbits/sec	V_{EE}	80 MHz	60 MHz
15 Mbits/sec	Float	60 MHz	45 MHz
10 Mbits/sec	Float	40 MHz	30 MHz

When DIVSEL is low, the FVCO pin outputs the actual frequency of the internal VCO frequency divided by two.

UP: Active high whenever the phase detector issues a pump up to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed.

DOWN: Active high whenever the phase detector issues a pump down to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed.

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ANALOG PINS:

VCOREXT: Used to bias up the current source that sets the VCO center frequency f_o. An external resistor is tied from this pin to the most negative supply voltage (V_{EE}). The voltage on the VCOREXT pin is typically V_{EE} + 2.8 volts with an ambient temperature of 25°C. The VCOREXT resistor is R6 in the typical connection diagram in Figure 4. The VCOREXT resistor value vs. VCO center frequency can be calculated from the following equation:

$$R_{VCOREXT}(k\Omega) = 0.268 + \frac{223.2}{f_o} + \frac{7632}{f_o^2}(k\Omega) \quad \textit{(eq. 1)}$$

where f_o is in MHz. For an example of f_o = 70MHz;

$$R_{VCOREXT}(k\Omega) = 0.268 + \frac{223.2}{70} + \frac{7632}{4900} = 5.01k\Omega \quad \textit{(eq. 2)}$$

The VCO is at its center frequency when there is zero differential voltage across the FILTER and FILTERN pins. The FILTER and FILTERN pins may be shorted together to measure the center frequency. Note that the frequency observed at FVCO, FVCON is either the VCO frequency or VCO frequency divided by two, depending on the DIVSEL pin setting.

HGREXT: Used to set the magnitude of the high gain current for the charge pump. Normally a resistor will be tied from this pin to the most negative supply of the IC. The voltage on the HGREXT pin is typically V_{EE} +1.18 volts. The user may vary the high gain charge pump current from 0.5mA to 2.0mA. The HGREXT resistor can be calculated from the following equation:

$$HGREXT(\Omega) = \frac{1.18(V)}{(\text{High gain charge pump current})} \quad \textit{(eq. 3)}$$

Refer to Figure 4, R_2 is typical HGREXT register.

LGREXT: Used to set the magnitude of the low gain current for the charge pump. Normally a resistor will be tied from this pin to the most negative supply of the IC. The voltage on the LGREXT pin is typically V_{EE} +1.18 volts. The user may vary the low gain charge pump current from 100µA to 400µA. The LGREXT resistor can be calculated from the following equation:

$$HLGREXT(\Omega) = \frac{1.18(V)}{(\text{Low gain charge pump current})} \quad \textit{(eq. 4)}$$

Refer to Figure 4, R_4 is typical HGREXT resistor.

FCAPP, FCAPM: Differential loop filter pins for the delay control feedback loop. A large capacitor is placed across these pins, typically 0.5µF.

FILTER, FILTERN: Differential loop filter pins for the main phase locked loop. These outputs are referenced to VDD and will therefore track with VDD. The FILTER pin is the high impedance side of filter. The FILTERN pin is always a low impedance voltage source which is inversely proportional to the voltage on the FILTER pin.

$$\Delta V_{FILTER} = (-1) \bullet \Delta V_{FILTERN} \quad \textit{(eq. 5)}$$

The DC voltage crossover point for FILTER and FILTERN is approximately (VDD – 4.75V). The differential range is ± 3V.

The VCO center frequency f_o is defined as the VCO frequency when the VCO control voltage is at the middle of its range. This occurs when there is zero differential voltage across FILTER and FILTERN. The VCO frequency can be controlled directly by forcing the voltage on the FILTER pin. VCO gain can then be measured by plotting the differential voltage across FILTER and FILTERN vs. FVCO frequency and calculating the slope of the line.

SUPPLY PINS:

VEE:	Most negative digital supply.
VEE1:	Most negative analog supply.
VEE2:	Most negative VCO supply.
VEE3:	Most negative supply for delay.
VCC:	Digital middle supply 5 volts greater than VEE.
VCC1:	ECL supply 5 volts greater than VEE.
VCC2:	VCO supply 5 volts greater than VEE2.
VCC3:	Delay control supply 5 volts greater than VEE3.
VDD:	Most positive digital supply.
VDD1:	Most positive analog supply.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

The data separator is inherently a sensitive circuit, and thus circuit performance can be degraded significantly without careful attention to board layout. The following guidelines should be followed:

1. V_{EE}, V_{CC} and V_{DD} supply bypass filtering should be liberal and as close to the supply pins as possible. Ideally, a bypass capacitor should be soldered directly to each supply pin. The electrical lead length of the bypass capacitors between the supply and ground pins should be minimized to reduce lead inductance. Only high-quality capacitors should be used.
2. Use the main digital ground plane for all grounding associated with the device.
3. Locate all passive components associated with the chip as close to their respective device pins as possible. It is extremely critical that the PLL filters be very tightly spaced. In addition the $R_{VCOREXT}$ resistor should be tightly spaced or located closely to the VCOREXT pin. Chip capacitors and resistors work very well for these filters.
4. For best performance, the chip pins should be soldered directly to the printed circuit board. If a socket must be used, a low-profile, low-resistance, forced-insertion type socket is recommended.
5. Allow any unused digital outputs to float, unconnected to any other traces.
6. Very fast ECL edge rates should be avoided. Rise/Fall times for the differential ECL signals (REFOSC AND RDATA) should not exceed 2.5ns. If 10KH drivers are used, a 100Ω series resistor works well to reduce the edge speeds

DC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	I_{CC}			129.3	170	mA
	I_{DD}			22.3	40	mA
Power Dissipation	P_D	$V_{DD} = 13.2V$, $V_{CC} = 5.5V$		1.02	1.3	W
Charge Pump		High gain	0.5		2	mA
		Low gain	0.1		0.4	mA
TTL Inputs (Note 1)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current High	I_{IH}	$V_{IH} = 2.7V$, $V_{CC} = 5.5V$			20	µA
		$V_{IH} = 6V$, $V_{CC} = 5.5V$			100	
Input Current Low	I_{IL}	$V_{IN} = 0.5V$, $V_{CC} = 5.5V$			-0.6	mA
Differential ECL Inputs (Note 2)						
			V_{CC} - 2.3			V
			200			mV
Input High Current	I_{IH}	$V_{CC} = 5.5V$			25	µA
Input Low Current	I_{IL}	$V_{CC} = 5.5V$			25	µA
Voltage Output High	V_{OH}		V_{CC} - 1.02		V_{CC} - 0.66	V
Voltage Output Low	V_{OL}		V_{CC} - 1.95		V_{CC} - 1.63	V

Note 1: TTL inputs will float to a logic HI if left unconnected.
Note 2: All inputs and outputs denoted as ECL track with the V_{CC} supply voltage.

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EXTERNAL COMPONENT SELECTION

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
RHGREXT			590		2400	Ω
RLGREXT			2.95		12	kΩ
RVCOREXT			1.6		6	kΩ
VMP Series Resistor to Ground			2		5	kΩ
FCAPP, FCAPM Capacitor				0.5		µF

AC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
REFOSC, REFOSCN Period	T_{REFOSC}		10			ns
REFOSC, REFOSCN Pulse Width	$t_{pwREFOSC}$		4			ns
RDATA, RDATAN Pulse Width	$t_{pwRDATA}$		4			ns
Window Center Offset	t_{WINDOW}			<300		ps
Delay Line Propagation Delay	t_{pDL}			Note 1		ns
VCO Phase Noise	ϕ_{VCO}	Locked to preamble, 1σ (note 2)		<50		ps
VCO Center Frequency Variation	Δf_o	@ f_o = 70MHz	-10		+10	%
VCO Zero Phase Restart Error	t_{ZPR}			<1		ns
VCO Maximum Center Frequency	f_{cMAX}			192		MHz
VCO Dynamic Range from f_o	f_{VCODR}	f_o = 70MHz, $R_{VCOREXT}$ = 4.9kΩ	$0.7f_o$		$1.3f_o$	MHz
VCO Gain	K_O	f_o = 70MHz, $R_{VCOREXT}$ = 4.9kΩ	$0.9f_o$	$0.105f_o$	$0.13f_o$	MHz/V
Charge Pump Output Linearity	f_{LIN}	Range is 0 to 2π	-10		+10	%
SCLOCK Duty Clock	t_{dcSCLK}			50		%
Propagation Delay from SCLOCK Negative Edge to SDATA Rising Edge	t_{pdSD}	C_{load} = 20pF		$-1.5 < t_{pdSD} < 1.5$		ns
Propagation Delay from FVCO Rising Edge to SCLOCK Rising Edge	t_{pdSCLK}	C_{load} = 20pF		$-2 < t_{pdSCLK} < 4$		ns
Marginalization Maximum Shift	$t_{MAXMARG}$			0.25 (T_{REFOSC})		ns
Marginalization Variation from Nominal	t_{MARG}	$V_{VMP} - V_{VMM}$ = 100mV		±0.02 (T_{REFOSC})		ns

Note 1: Nominal value for t_{pDL} is: $[0.5(T_{REFOSC}) - 1] < t_{pDL} < [0.5(T_{REFOSC}) + 1]$.
Note 2: VCOCLK output 1σ point measured over 10,000 samples on an HP5370B time interval counter. $\sigma_{fcl} = \sqrt{\sigma_a^2 - \sigma_b^2}$, where σ_a = rms jitter measurement and σ_b = self jitter of HP5370B (see HP app. note 191-4).

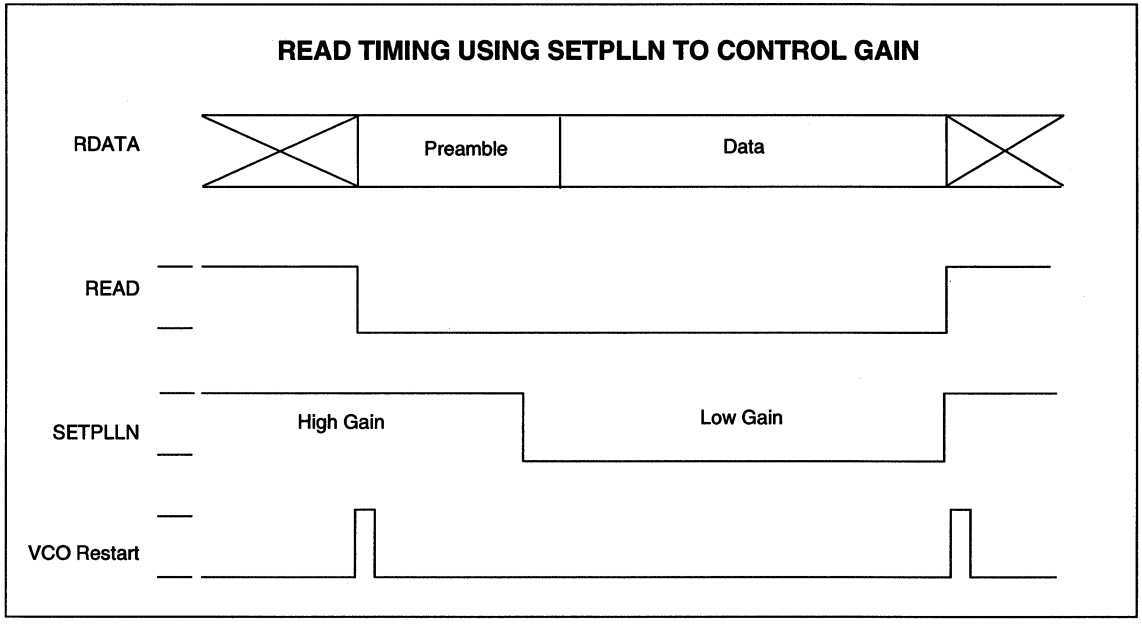

Figure 1: Read Timing Diagrams

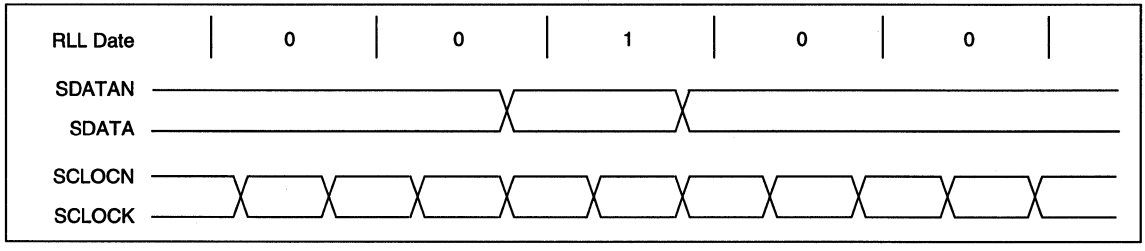

Figure 2: Synchronized Data and Clock Timing

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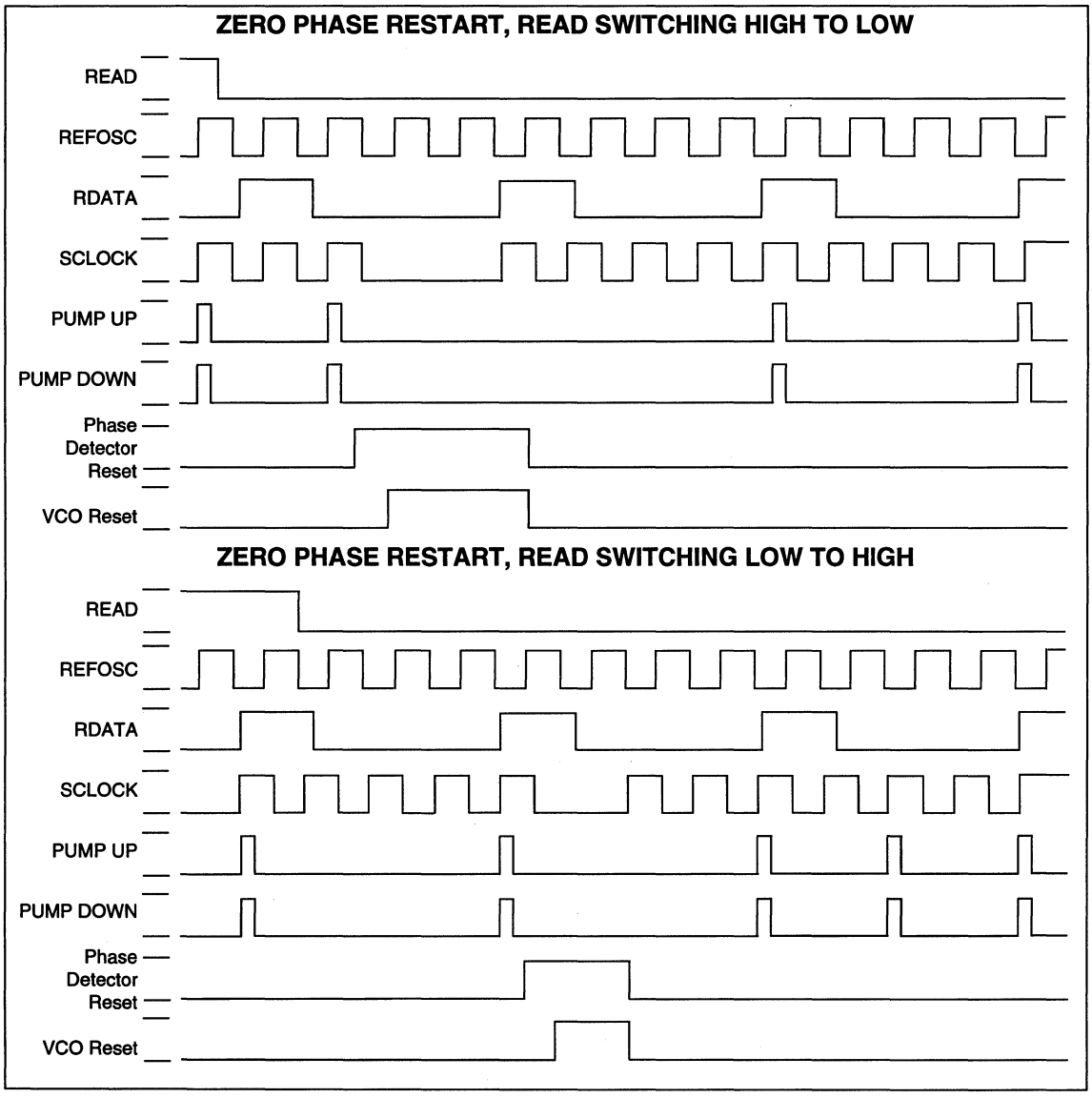
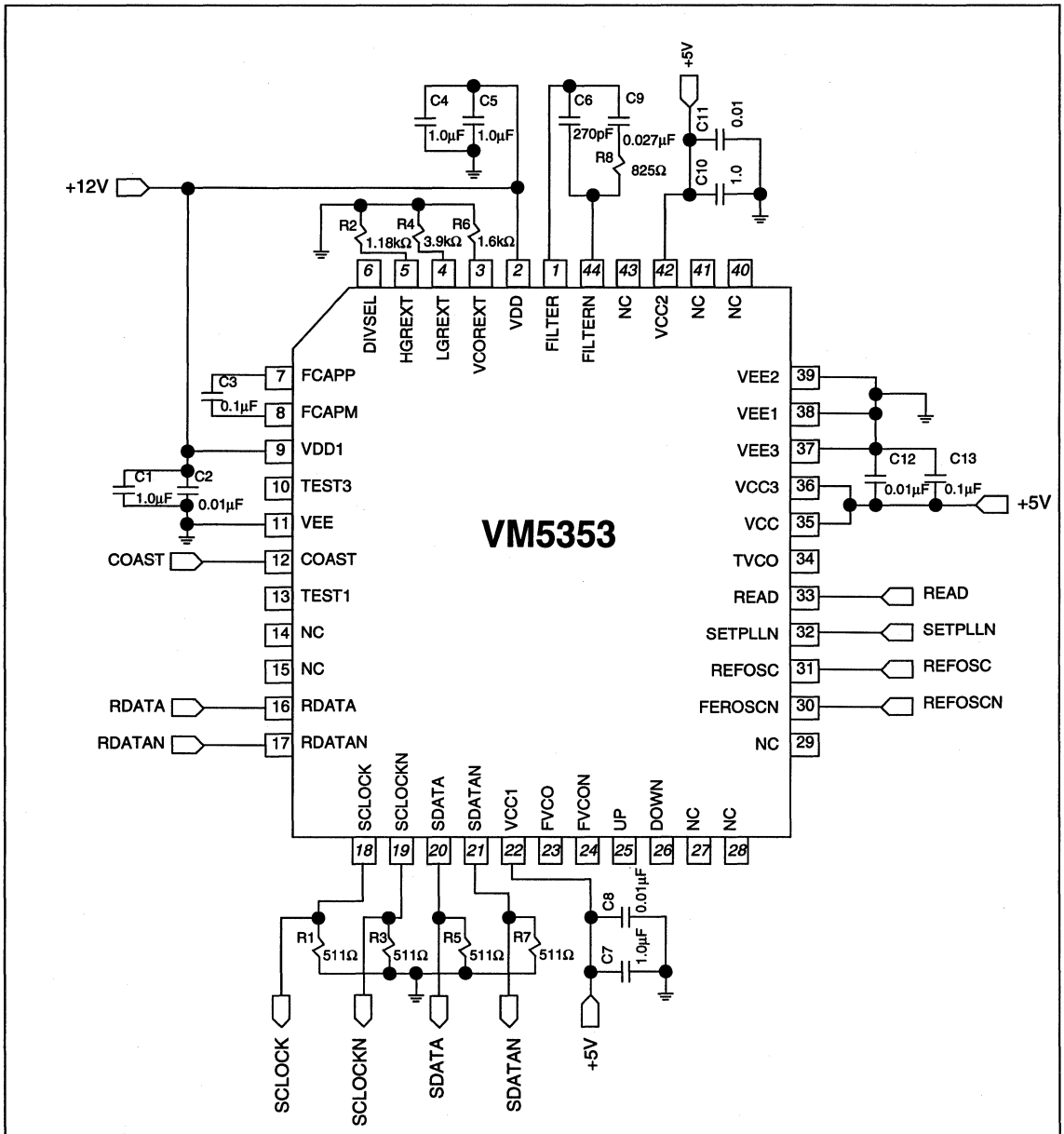


Figure 3: VCO Zero Phase Restart Timing



NOTE: This circuit is set up for 64Mbits/sec using (1,7) code. The REFOSC input frequency is a 96MHz differential ECL signal. The high and low gain charge pump currents are set to 1.0mA and 0.3mA, respectively. The VCO center frequency is set to 192MHz, giving a VCO gain of 20.2MHz/V. This is a general setup and not intended to be optimized for 4Mbits/sec.

Figure 4: VM5353 Typical Connection Diagram

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VTC Inc.
Value the Customer™

VT5204

2-CHANNEL, HIGH-PERFORMANCE, INDUCTIVELY COUPLED FERRITE HEAD, READ/WRITE PREAMPLIFIER

PRELIMINARY August,1994

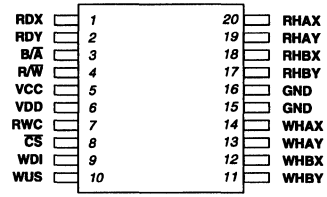
FEATURES

- High Performance
  - Rise/Fall Times = 8.3 ns Typical into 2.3 µH Head
  - Input Capacitance = 8 pF Typical
  - Input Noise = 0.72 nV/√Hz Typical
  - Head Inductance Range = 1 – 7 µH
  - Voltage Gain = 240 or 375 V/V
- TTL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V
- Power Supply Fault Protection
- Options Available
  - WDFF on the Write Data Inputs Connected or Disconnected
  - Open Collector or Emitter Follower Output in Read Mode
  - With or Without Switchable Damping Resistor

DESCRIPTION

The VT5204 is a high-performance, integrated read/write preamplifier designed for a helical-scan head which is coupled to the circuit by an inductive transformer. The VT5204 has eight head pins which connect to two read heads and two write heads. The circuit has one input which allows analog control of the write current for the selected write head and two digital inputs which allow selection of write/read mode and A/B channel. The VT5204 circuit is powered by a +12/+5VDC supplies. The circuit is designed to have a power supply fault detect circuit which shuts off write current in the event the power supply level drops below a unsafe threshold. This protect the data on the media from potential transients. If a line should open up, the mode select lines will be forced into a high state to prevent the device from affecting data recorded on the media.

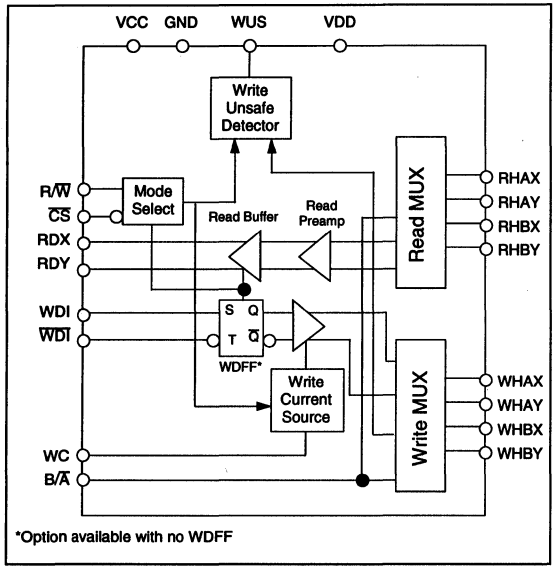
CONNECTION DIAGRAM



2-Channel
20-lead SOIC

TAPE DRIVE CIRCUITS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 35mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Read Head Port Voltage V_{RH} ..... -0.3V to (V_{CC} + 0.3)V
- Write Head Port Voltage V_{WH} ..... -0.3V to (V_{CC} + TBD)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} .....12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature .....0°C to 125°C

CIRCUIT OPERATION

The VT5204 addresses the head selected by the digital inputs providing write drive or read amplification. Head selection and mode control are accomplished with pins B/$\overline{A}$, R/$\overline{W}$, and $\overline{CS}$. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VT5204 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current flows into the "X" head port when WDI is a logical "1" and flows into the "Y" head port when WDI is a logical "0".

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (± 8%) is:

$$I_W = 50/R_{WC}$$
(mA, 0-pk, R_{WC} in kΩ)

In programmable write current applications, the proper write current level can be selected by using a current DAC or by selecting different resistor values using analog switches or MOS gates. The magnitude of the write current can also be calculated as:

$$I_W = 20 * I_{WC}$$
(mA, 0-pk, I_{WC} is programmed value in mA)

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Read Mode

Read mode configures the VT5204 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay when switching between write mode and read mode.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 20mW for a sleep mode.

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Table 1: Mode Select

R/$\overline{W}$	$\overline{CS}$	MODE
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 2: Head Select

B/$\overline{A}$	HEAD
0	A
1	B

PIN DESCRIPTIONS

NAME	#	DESCRIPTION
RDX	1	Read amplifier multiplexed differential output (X)
RDY	2	Read amplifier multiplexed differential output (Y)
B/$\overline{A}$	3	TTL Digital Control: switches between A and B channels
R/$\overline{W}$	4	TTL Digital Control: switches between write and read modes
VCC	5	+5V DC power supply input
VDD	6	+12V DC power supply input
WC	7	Output write current control reference (I_{WC} = 20 * I_{WC})
$\overline{CS}$	8	Chip Select: $\overline{CS}$ = '0' for normal operation; $\overline{CS}$ = '1', enables low power mode
WDI	9	TTL Digital Write Data: WDI = '1' I_W into WHX pin
WUS	10	Write unsafe flags improper write conditions
WHBY	11	Write head channel B, Y output
WHBX	12	Write head channel B, X output
WHAY	13	Write head channel A, Y output
WHAX	14	Write head channel A, X output
GND	15	Ground
GND	16	Ground
RHBY	17	Read head channel B, Y input
RHBX	18	Read head channel B, X input
RHAY	19	Read head channel A, Y input
RHAX	20	Read head channel A, X input

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		32	TBD	mA
		Write Mode		23.5	TBD	
		Idle Mode		0.6	TBD	
VDD Supply Current	I_{DD}	Read Mode		0.6	TBD	mA
		Write Mode		8 + I_W	TBD	
		Idle Mode		0.6	TBD	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		167	TBD	mW
		Write Mode: I_W = 20mA		454	TBD	
		Idle Mode		22	TBD	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-0.6			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VDD Fault Voltage	V_{DDF}		9.5	10	10.5	V
VCC Fault Voltage	V_{CCF}		3.5	4.0	4.5	V
Write Head Current	I_H	Write protect mode, power supply fault or non-selected head	-200		+200	µA

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ. Input source (head), impedance is L_H (typical) = 5µH, L_H (minimum) = 1µH, R_H < 1Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	200	240	280	V/V
			300	375	450	
Bandwidth	BW	-1dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	25	40		MHz
		-3dB, |Zsl < 5Ω, V_{IN} = 1mVp-p @300kHz	40	65		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.72	TBD	nV/√Hz
Input Noise Current	I_{IN}			1.8		pA/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		8	10	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	TBD	3000	TBD	Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90%, A_V @ V_{IN} = 0.2mVrms, f = 5MHz	2	4		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = V_{CC} + 100mVp-p @ f = 5MHz	50	60		dB
Power Supply Rejection Ratio	PSRR	100mVp-p, f = 5MHz on V_{DD} or V_{CC}	45	50		dB
Channel Separation	CS	Unselected channel V_{IN} = 100mVp-p, f = 5MHz, V_{IN} = 0mVp-p selected	45	50		dB
Output Offset Voltage	V_{OS}			±300		mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.7	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.7	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			35	Ω
Output Current	I_O	AC coupled load	±1.5			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 2.3µH, R_H = 1Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}			2.5		VDC
Write Current Voltage	V_{DH}	I_{WC} = 35mA		19		V
Unselected Head Write Current	I_{UH}				0.2	mA (pk)
Differential Output Capacitance	C_{OUT}			5		pF
Differential Output Resistance	R_{OUT}	Internal damping resistance @ 2.5kΩ		1.5		kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	350			kHz
Write Current Range	I_W	1430Ω< R_{WC} < 10kΩ	5		35	mA
Write Current ERR	I_{ERR}	I_W range 1mA to 35mAo-p	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 2.3µH, R_H = 1Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	Delay to 90% I_W		50	300	ns
Write to Read Mode	t_{WR}	Delay to 90% I_W or to 90% of 100mVp-p output @ 10MHz			600	ns
$\overline{CS}$ to Select	t_{IR}	Delay to 10% I_W			600	ns
$\overline{CS}$ to Unselect	t_{IW}	Delay to 90%, 100mVp-p output @ 10MHz		300	600	ns
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	Duty cycle 50% WDI, 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	L_H = 2.3µH, R_H = 1Ω, internal damping resistance 2.5kΩ		8.3	9.5	ns
Output Current Rise/Fall Time	t_r/t_f	L_H = 0µH, R_H = Ω		2	5	ns

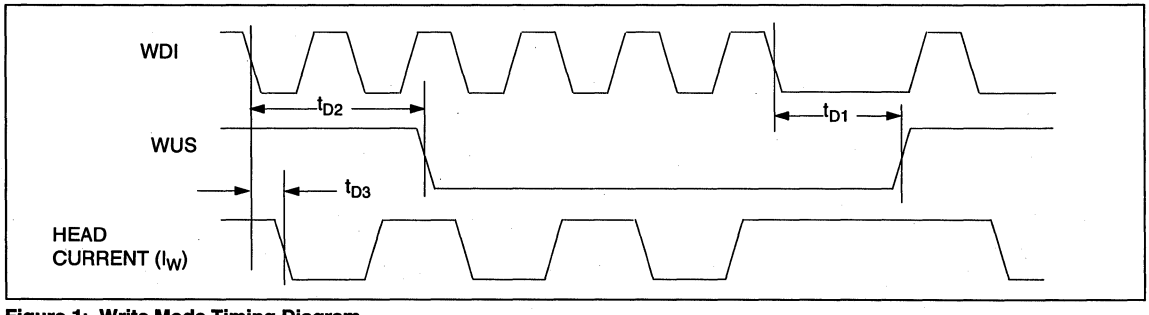

Figure 1: Write Mode Timing Diagram

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7 Application Notes

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LOOP FILTER DESIGN FOR THE VM5351/VM5352 AND VM5353

August, 1994

PLL LOOP FILTER DESIGN

In order to maintain design flexibility for the customer, all PLL filter components and charge pump gain settings reside external to the chip. All PLL dynamics are under the control of the system designer. The following is a brief analysis of the PLL loop filter design. For a detailed deviation of the equations used here see the Phase-Lock Loop Application Fundamentals for Disk Drives Application Note APN-6. Refer to the VM5351/VM5352 and VM5353 PLL block diagram in Figure 1.

The impedance of the loop filter can be written as follows:

$$Z(s) = \frac{R\left(s + \frac{1}{RC_1}\right)}{sC_2R\left(s + \frac{1}{RC_1} + \frac{2}{RC_2}\right)} \qquad \textit{(eq. 1)}$$

The open loop gain for Figure 1 is:

$$G(s) = \frac{K_{VCO}K_{CP}K_{div}R\left(s + \frac{1}{RC_1}\right)}{s^2C_2R\left[s + \frac{1}{RC_1}\left(\frac{C_1 + C_2}{C_2}\right)\right]} \qquad \textit{(eq. 2)}$$

where, $K_{CP} = K_d = 1.18/R_L$,
$K_{VCO} = K_O = 0.105f_o$,
$K_{div} = 1/AB = 1/ANT_R = 1/A2T_R$

B is defined as NT_R. N is the hard-wired divide ratio and equals 2. T_R is the relative encoded data pattern length. For example, a 4T preamble field would correspond to T_R equals 4. When locked to the reference, T_R is equal to 2. The divide-by-A block is defined as:

A = 1 if the DIVSEL pin is LO
A = 2 if the DIVSEL pin is HI

The VCO center frequency is f_o. R_L is the HGREXT or LGREXT external resistor, depending on whether the PLL is high-gain or low-gain mode.

Substituting these values into G(s) and using the second order approximation where $C_2 << C_1$, G(s) becomes:

$$G(s) = \frac{K(s + \omega_1)}{s^2}, \quad \text{where } \omega_1 = \frac{1}{RC_1}$$
$$\text{and } K = K_{CP}K_{VCO}K_{div}R = \frac{0.062f_cR}{AT_RR_L} \qquad \textit{(eq. 3)}$$

Looking at G(s), there are two poles at s = 0 and one zero at $s = -\omega_1$. The closed loop gain H(s) is defined as:

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{K(s + \omega_1)}{s^2 + Ks + K\omega_1} \qquad \textit{(eq. 4)}$$

The denominator of H(s) is called characteristic equation. It can be compared to the standard form for second degree characteristic equation as follows:

$$s^2 + Ks + K\omega_1 = s^2 + 2\zeta\omega_n + \omega_n^2 \qquad \textit{(eq. 5)}$$

Equating the component values gives:

$$K = 2\zeta\omega_n \text{ and } K\omega_1 = \omega_n^2 \qquad \textit{(eq. 6)}$$

where ω_n is the natural frequency of the loop and ζ is the damping factor.

Now, substituting for K and ω_1, the values for R and C can be obtained.

$$R = \frac{\zeta\omega_nAT_RR_L}{0.031f_o}$$
$$C_1 = \frac{0.062f_o}{\omega_n^2AT_RR_L} \qquad \textit{(eq. 7)}$$
$$C_2 \text{ is chosen such that } \frac{C_1}{1000} \le C_2 \le \frac{C_1}{10}$$

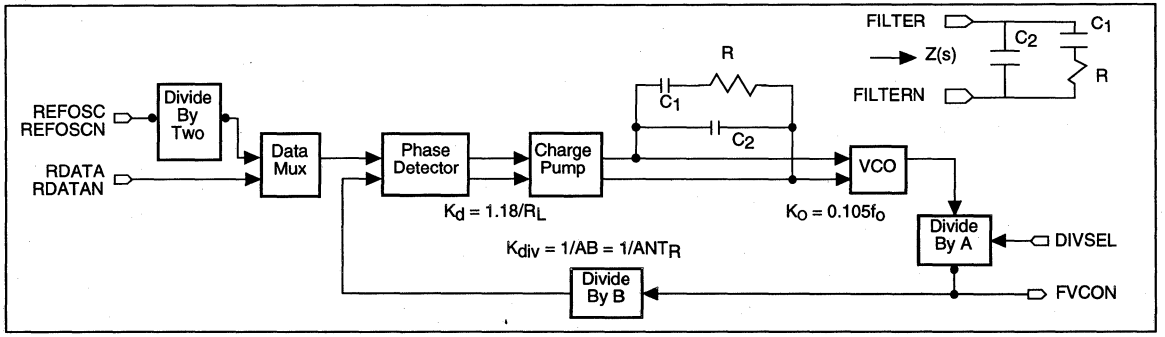

Figure 1: Basic VM5351/VM5352 and VM5353 PLL Block Diagram

APPLICATION NOTES

Component values can now be selected in accordance with specific system requirements. The following system parameters must be specified: f_o, R_L, N , ω_n and ζ in order to choose values for R, C_1 and C_2.

LOOP FILTER DESIGN USING (2,7) RLL CODE
System Requirements:

NRZ Data Rate = 24Mbits/sec (= f)
VCO Center Frequency = f_o = 96MHz (= 4f)
REFOSC Frequency = 48MHz (= 2f)
ω_n = 139K rad/s
ζ = 1.55

Preamble length = 11 NRZ bytes (EDSI min.) = 3.67µs
(44 recorded pulses)

The VM5351/VM5352 and VM5353 has a zero-phase restart function which minimizes the initial phase step encountered when switching the input of the PLL. However, the PLL may encounter a step in frequency that can be as large as ±1%. Given the PLL must only correct for the frequency step, the user needs to consider the following loop requirements when determining the loop filter values:

1. Residual phase error at the end of the preamble.
2. The lock-in range required for the frequency step encountered.
3. The minimum 3dB bandwidth in the data field must be greater than the maximum mechanical vibrations (typically 10KHz).
4. The natural frequency ω_n and damping ratio ζ must be optimized to achieve maximum jitter rejection in the data field. The minimum damping ratio ζ for adequate stability is 0.5.
5. Re-lock to the reference clock must be minimized.

Since the VCO center frequency is greater than 60MHz, the DIVSEL pin should be tied low, which implies that A = 1 for the divide-by-A block.

The first step is too choose the three external resistors HGREXT, LGREXT and VCOREXT as follows:

$$\text{HGREXT} = \frac{1.18\text{V}}{\text{HG Charge Pump Current}} = \frac{1.18\text{V}}{1.0\text{mA}} = 1.18\text{k}\Omega$$

$$\text{LGREXT} = \frac{1.18\text{V}}{\text{LG Charge Pump Current}} = \frac{1.18\text{V}}{400\mu\text{A}} = 2.95\text{k}\Omega$$

$$\text{VCOREXT} = 0.268 + \frac{223.2}{96} + \frac{7632}{96^2} = 3.4\text{k}\Omega$$

The low gain mode is used when locking to data and the high gain mode is used when locking to the reference oscillator or preamble. The component values can be chosen for either the high or low gain mode, but since lock-to-data is more critical, LGREXT will be used for R_L. Also, an average data pattern of 4T is assumed.

The values for R, C_1 and C_2 are calculated as follows:

$$R = \frac{(1.55)\left(139\times10^3\right)(1)\,(4)\,(2950)}{0.031\left(96\times10^6\right)} = 854\Omega \approx 866\Omega$$

$$C_1 = \frac{0.062\left(96\times10^6\right)}{\left(139\times10^3\right)^2(1)\,(4)\,(2950)} = 0.026\mu\text{F} \approx 0.22\mu\text{F}$$

$$C_2 = 0.01C_1 = 220\text{pF}$$

Now using the standard values, ω_n and ζ should be recalculated to insure accuracy along with the phase margin ϕ_R.

$$\omega_n = \sqrt{\frac{K}{RC_1}} = \sqrt{\frac{0.062\left(96\times10^6\right)(850)}{4\,(2950)\,(66)\left(0.22\times10^{-6}\right)}} = 151\text{Krad/s}$$

$$\zeta = \frac{\omega_n RC_1}{2} = \frac{124,000\,(66)\left(0.22\times10^{-6}\right)}{2} = 1.44$$

$$\phi_R \cong \tan{-1}\left(4\zeta^2\right) = \tan{-1}\left(4\,(1.44)^2\right) = 83.1°$$

The values for ω_n and ζ changed slightly here, but depending on what standard component values are used, they could change substantially. The phase margin should be greater than 45° for stability. In this case there is plenty of margin since ϕ_R = 83°.

The above values are not optimized for systems using this data rate, code and preamble. The derivations are only shown as an example.

APPLICATION NOTES

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VTC Inc.
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CURRENT GAIN OF 20 vs. CURRENT GAIN OF 1 FOR 5-VOLT READ/WRITE PREAMPLIFIERS

August, 1994

INTRODUCTION

Improved read/write preamplifiers with a current gain of 20 are becoming available as replacements for the gain-of-1 chips, with the benefits of higher write voltage, lower ringing and overshoot, insensitivity to flex layout, and flexible control of the write current.

DESCRIPTION

In a hard disk drive, digital data is written into the magnetic medium by changing the magnetic field at the pole tips of a tiny horseshoe magnet (the read/write head) suspended on air bearings above the surface of the rapidly rotating magnetic medium. The write circuitry that drives the switching current through the inductive head is a key system element and should be chosen with care for the drive.

A variety of read/write preamps are available for disk drives today and it is easier to understand the choices and tradeoffs involved if the basic circuitry is understood. This Application Note has been written to provide better insight into the features of write electronics.

Switching an inductor (the read/write head is best represented as an inductor with substantial series resistance) at high frequencies is a technological challenge. The head is an energy-storage element and the parasitic capacitance of the preamp and the head-preamp interconnections is another energy-storage element, so that with inadequate care in design it is easy to produce a system which is unstable and bursts into spurious self-sustained oscillations. Parasitic elements in the flex circuit can also contribute to oscillation problems. No preamp is totally foolproof in this regard. Under sufficiently extreme application conditions spurious oscillations can always occur. However, preamps may differ markedly in the margin against oscillation.

Inherent stability against self-sustained oscillations for a wide range of head inductance and Q is an explicit design goal for VTC preamps. VTC products consistently achieve superior stability margins on the flex.

The write circuit is designed to produce current pulses of magnitude $\pm I_w$, i.e. it switches the write current between values $+I_w$ and $-I_w$ upon command of the digital write data (WD) signal. When the write current switches, it produces a flux reversal in the magnetization of the medium, which is read back as digital data during the read process. The magnitude of the write current must be carefully controlled at a value that is best for the particular heads (medium, flying height etc.) to be used.

The dynamics of head current switching is governed by the basic inductor equation $V = L(dI/dt)$. Written in another way, this implies $(dI/dt) = V/L$; in other words the rise and fall times of the head current (and hence the head field which is writing the medium) are inversely proportional to the voltage put out by the write circuitry and directly proportional to the head inductance.

BASIC WRITE CIRCUITRY

There are two basic types of write circuit, shown in simplified form in Figure 1. The open circles indicate off-chip connections. Both types handle head current switching through an ***H-switch***, made up of transistors Q_1-Q_4 with the read/write head connected as shown. The H-switch has two states, one with Q_1, Q_2 ON and Q_3, Q_4 OFF, and the other with the reverse of this. In the first state current flows through Q_1, then left-to-right through the head, and down through Q_2 while Q_3 and Q_4 are OFF. In the other state the current will flow right-to-left through the head. The two types of write circuit differ in how the write current magnitude is controlled.

In both types of writer the elements Q_6, Q_7, Q_8, R_2, R_3, R_4 provide logical inversion and level shifting of the write data signals WD and $\overline{WD}$ needed to force the Q_1, Q_2-ON Q_3, Q_4-OFF condition.

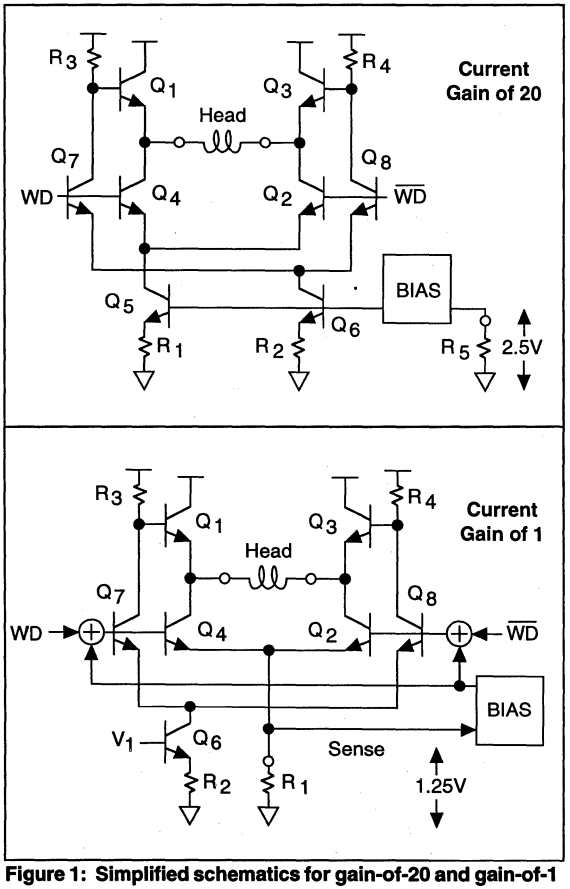

Figure 1: Simplified schematics for gain-of-20 and gain-of-1 write circuitry in a read/write preamp.

APPLICATION NOTES

The gain-of-1 and gain-of-20 write circuits[1] differ primarily in how the write current Iw is controlled. In the gain-of-20 circuit, transistors Q_2, Q_4 of the H-switch are connected as a differential pair biased with the current source R_1, Q_5, and the write current is controlled by adjusting the DC voltage supplied to the base of Q_5. In the gain-of-20 case, resistor R_1 is on-chip (an important point which we will return to) and the needed base bias of Q_5 is set by a bias network that applies an internally generated temperature-compensated 2.5 V to the reference resistor R_5, and compares the resulting current to 1/20 of the write current (using precision current-ratio techniques, which make use of the excellent matching of on-chip components) in a feedback loop. Thus the gain-of-20 circuit uses indirect control of the write current.

In the gain-of-1 case transistors Q_2,Q_4 of the H-switch are connected to an ***off-chip*** resistor R_1 rather than a current source. While this is conceptually simpler (fewer elements), it introduces a number of complications that can result in more elements in the full schematic. In the gain-of-20 case the write current is set by a simple DC bias voltage. In the gain-of-1 case the needed DC bias voltage must be added to the (digital) write data signals WD and WD (shown by the sum symbols in the schematic). The write current is set by comparing the voltage on the sense line to a fixed bias voltage (usually 1.25 V in existing chips) and a feedback control loop[2].

A COMPARISON OF GAIN-OF-20 AND GAIN-OF-1

This application note will consider the pros and cons of these two circuits in terms of the 5-Volt preamps that are commonly used today.

In the gain-of-20 circuit the write current is controlled by entirely separate DC circuitry which has no other function than to regulate I_w. In the gain-of-1 case the voltage on the sense line comes from a point in the circuit with large amounts of switching noise[3] and the bias circuitry must distinguish its DC component. Likewise, the output of the bias loop is a DC voltage which must be added to the AC write data signal. Thus the current-control feedback loop is substantially more complicated in the gain-of-1 case despite the simpler circuitry for the H-switch itself. One consequence of this is that it is often harder to achieve good stability of the write current with gain-of-1. An example of this can be seen in Figure 2, which compares the write current waveforms for the VM7200 (gain-of-20) and a competing alternate-source gain-of-1 part with a 4.4 µH head. The gain-of-1 chip has a 160 ns risetime, while the gain-of-20 part has 125 nsec risetime. This 37% improvement in the write risetime is due largely to the higher write voltage inherent in the gain-of-20 design.

Figure 3 shows the write current waveforms with a 940 nH head. Here the transient behavior is dominated more by the relatively high coil resistance and less by the inductance, and risetimes are about equal between the two devices. The response time of the head circuit is much shorter here, and the inherent stability of the design shows up more clearly. Due to the inherent advantages of the gain-of-20 design and the simpler feedback loop used to control the write current the overshoot is substantially less for the gain-of-20 design, showing its inherently better stability.

Current-setting accuracy is strongly influenced by the load impedance at the emitters of the current-sink transistors Q_2 and Q_4. In the gain-of-1 circuit this is just the resistance of R_1, which may be as low as 25 Ω (at 50 mA). In the gain-of-20 circuit it is the output impedance of an active current source made up of Q_5

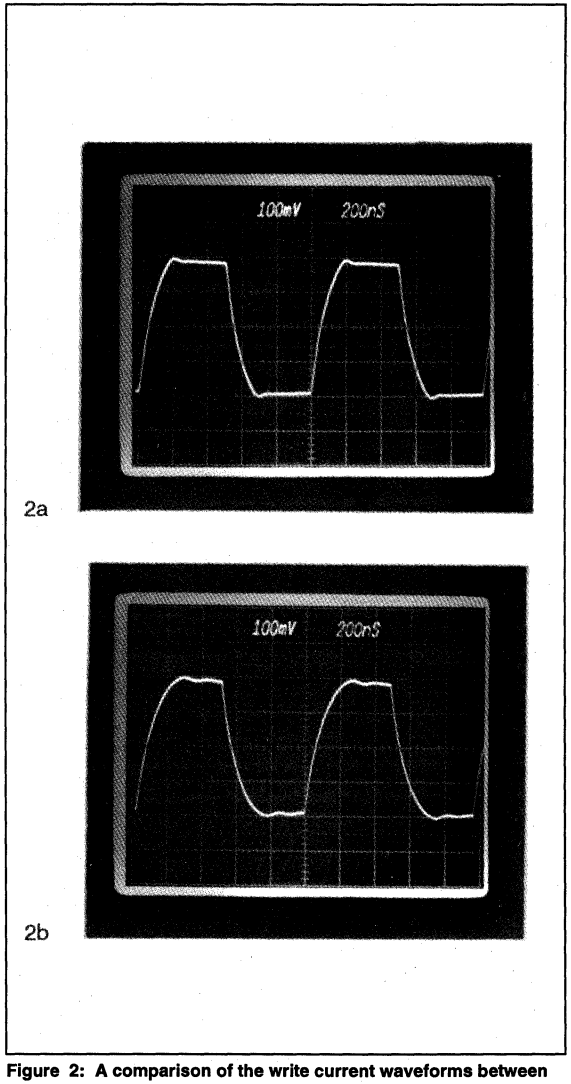

Figure 2: A comparison of the write current waveforms between the VM7200 gain-of-20 preamp (a) and a competing gain-of-1 chip (b). Both chips were operated with VCC = 4.5 V, a head inductance of 4.4 µH (30Ω series resistance), a nominal write current of 40 mA, and a 2 MHz square wave at the write input. Note the substantially (37%) shorter risetime for the gain-of-20 chip, which is inherent in the circuit design.

[1] These circuits are called gain-of-1 and gain-of-20 because the current passing through the current-setting resistor is 1x or (1/20)x the actual write current in the two cases. By gain we mean current gain

[2] This circuit is commonly used in 5V gain-of-1 preamps. Some 12V gain-of-1 preamps, such as VTC's VM312, VM313, and VM326, use a different technique that does not have the same performance drawbacks

[3] To complicate things, this switching noise is not at a single frequency, but is pattern-dependent and contains all the Fourier components of the data.

and R_1, and at 50 mA the impedance will be VA/I = 1000 Ω[4]. This helps greatly to maintain tight control of the write current.

An important difference is the on-chip versus off-chip position of the current-setting resistor. In the gain-of-20 case, the bias network and R_1 have the same on-chip ground, and ground drops pickup of extraneous signals, etc. can be closely controlled by chip layout. In the gain-of-1 case, R_1 and the bias network have different grounds, with all the hazards of crosstalk to other signals on the flex or DC ground differences. Because of the common ground, the higher sense voltage, and lower sensitivity to parasitic resistances (on the flex, etc.) the gain-of-20 circuit inherently sets the write current more accurately and repeatably.

Another significant aspect of the off-chip location of the current-setting resistor in the gain-of-1 preamp is the parasitic inductance and capacitance of the resistor and its traces on the flex. The capacitance can be up to 6-8 pF and the inductance may be 10 nH, while an on-chip current-setting resistor will have parasitics at least ten times less. Moreover, these parasitics vary with the flex layout and positioning within the drive, while for the gain-of-20 design they are repeatable and well-controlled properties of the chip itself. These large off-chip parasitic elements can significantly affect the overall stability (suppression of spurious oscillations). In the gain-of-20 case there is no AC signal in the current-setting resistor, and parasitic inductance and capacitance have little effect on circuit behavior. Thus the gain-of-20 chip has an ease-of-design advantage. It is less sensitive to details of the flex layout, component positioning, crosstalk to other signals on the flex, etc.

WRITE VOLTAGE

As noted earlier, the available write voltage sets a limit on the rise and fall times of the write current, which can be a serious limitation on bit density. This is especially important for 5-Volt preamps, which have inherently limited write voltage capability.

In the gain-of-1 case, it is necessary to drop a substantial voltage across R_1 so the errors due to ground differences, switching noise, etc. are small; 1.25 V is a typical nominal value. Because of the common on-chip ground and the indirect control scheme the voltage drop across R_1 can be much smaller in the gain-of-20 case, typically 0.3 V for VTC designs. In the gain-of-20 scheme the collector-emitter voltage drop on the current source transistor Q_5 can be as low as 0.3 V, so that only about 0.6 V of head room is wasted for current control, versus the 1.25 V used for the gain-of-1 scheme. This results in substantially more write voltage with gain-of-20. The difference is illustrated in Figure 4, which shows a direct comparison of the write voltage waveforms of the VM7200 with a 4.4 µH head and a competing gain-of-1 part operated at the worst-case[5] low supply voltage of 4.5 V. The VM7200 shows nominally 16% higher write voltage, which under these conditions translates to 37% shorter write current rise and fall times (see Figure 2).

[4] V_A is the Early voltage of the transistor, with 50V typical of integrated NPNs.

[5] Almost all VTC's customers insist on ±10% power supply tolerance, usually mandated by the OEMs they sell to, and VTC datasheets reflect this. Some preamp data sheets from other suppliers are specified with ±5% power supply tolerances, which makes their stated write voltage look artificially better.

The write voltage waveform consists of a jump where the write data input switches, a decaying peak as the write driver applies a large voltage which begins to reverse the head current via the relation dI/dt = V/L, and a plateau where the write current is constant and the voltage is just the resistive drop in the head. The excess of the peak voltage above the plateau represents the useful voltage which is effective in reversing the head current. The gain-of-20 chip not only shows a higher peak, but it is sustained longer, both of which contribute to the superior risetime.

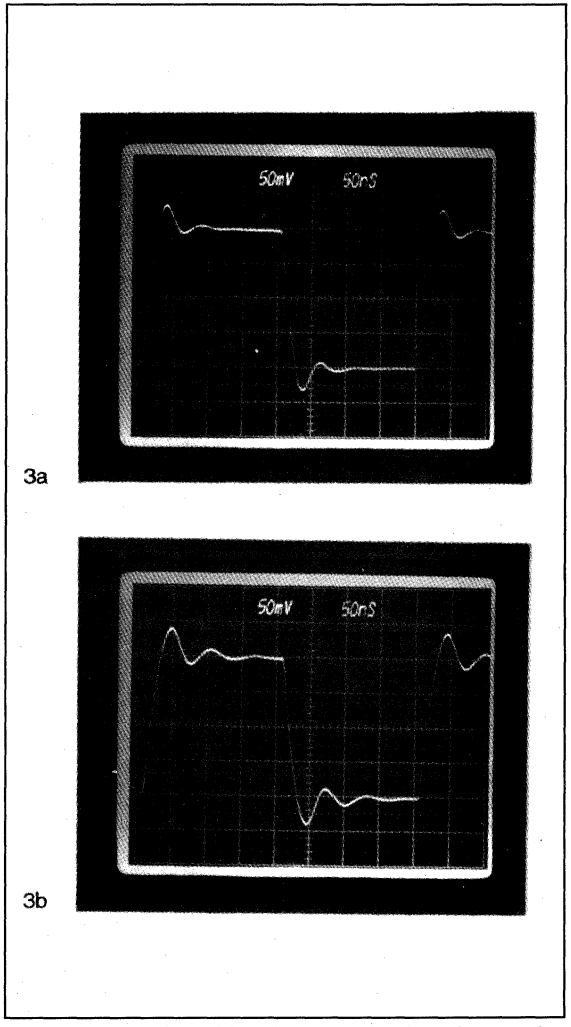

Figure 3: A comparison of the write current waveforms between the VM7200 gain-of-20 preamp (a) and a competing gain-of-1 chip (b). Both chips were operated with VCC = 4.5 V, a head inductance of 940 nH (30 Ω series resistance), a nominal write current of 40 mA, and a 5 MHz square wave at the write input. Note the lower overshoot for the gain-of-20 design.

VARYING THE WRITE CURRENT IN ZONE DENSITY RECORDING

The use of different recording frequencies in different zones of the disk to increase the amount of data stored on a surface has become widespread today. The drive control circuitry sets up different read and write frequencies and several other parameters individually for each zone by setting the inputs of several DACs. Because of the differences in such parameters as flying height between the inner and outer radius of the disk, the optimum write current may also vary.

In a gain-of-1 preamp it is possible in principle to replace R_1 by a current-output DAC and thus control the write current -- but such a DAC would need to sink up to 50 mA while the output does not rise more than 1.25V above ground. It is not known if there are any off-the-shelf DACs that can do this. An additional complication with the gain-of-1 chip is the fact that the DAC's output capacitance would occur at a point in the circuit with a substantial AC signal, which could negatively impact ringing and overshoot. With the indirect control used in a gain-of-20 preamp the DAC would need to put out only 2.5 mA and the output could operate up to 2.5 V above ground, greatly easing the electrical requirements. The parasitic capacitance of the DAC output is of no importance in the gain-of-20 case since there is no AC signal at that point.

In fact the gain-of-20 chip allows the write current to be controlled by simply using several current-setting resistors in parallel and switching them in and out using FET analog switches since the resistor values are much higher than typical FET ON resistances. The use of this FET switching technique is feasible with a gain-of-1 preamp, but requires a quite large FET. With gain-of-20 the FET can easily be an open-drain NMOS output device readily available on CMOS gate arrays and cell-library chips without requiring an unrealistically low ON resistance or drawing so much current through the MOSFET that reliability is compromised.

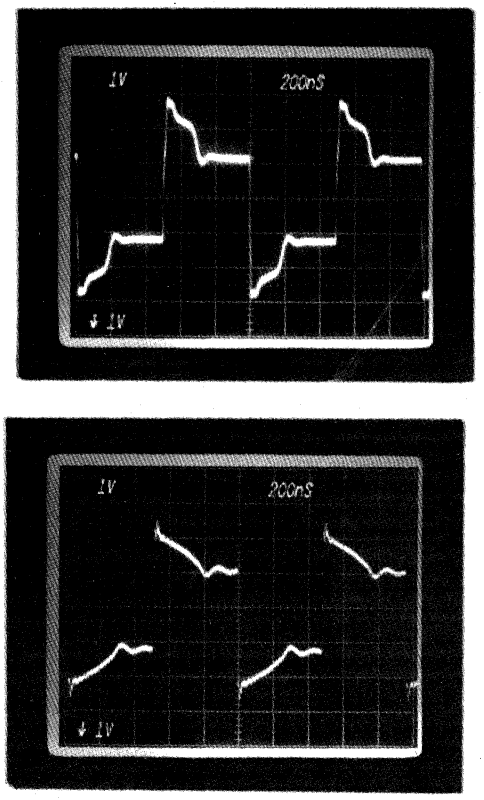

Figure 4: A comparison of the write voltage waveforms between the VM7200 gain-of-20 preamp and a competing gain-of-1 chip. Both chips were operated with VCC = 4.5 V, a head inductance of 4.4 μH (30 Ω series resistance), a nominal write current of 40 mA, and a 2 MHz square wave at the write input. The gain-of-20 preamp puts out about 16% higher write voltage due to fundamental design differences, which results in 37% shorter risetimes (see Figure 2)

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PULSE PAIRING IN READ CHANNELS

August, 1994

In a typical READ channel the input signal is differentiated to produce a signal which has zero crossings at the locations of the peaks (flux reversals). The output of the differentiator is then fed to a differential comparator which has zero crossings (output transitions) where the peaks occurred in the READ signal. A simplified block diagram for a typical system is shown in Figure 1. Offsets in the comparator and differentiator can cause an effect called ***pulse pairing error***. The pulse pairing effect is created when the comparator outputs do not cross zero exactly for zero input, but at some nominal offset voltage from the input crossing point. This offset creates a skew of opposite sign for alternating zero crossing[1] in the output data stream. This error directly detracts from system timing margins by consuming a portion of the bit cell window.

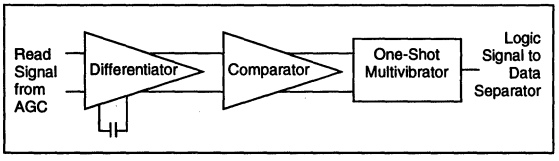

Figure 1: Differentiator, comparator, and pulse output circuits for a typical READ channel

The primary source of pulse pairing error is offsets in the comparator and the differentiator. These can be lumped together as an equivalent input offset for an ideal comparator. For a sinusoidal input this offset causes a non-symmetric output as shown in Figure 2. This asymmetry produces a shift between pulses from positive and negative peaks in the sine wave at the pulse output.

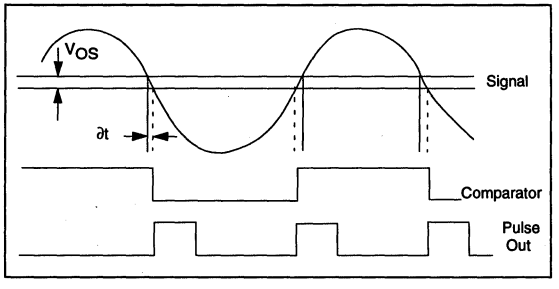

Figure 2: Read channel waveforms for a sine wave in the presence of circuit offsets. a) comparator input; b) comparator output; c) pulse output (input to data separator).

[1] The zero crossings corresponding to positive peaks in the READ data will be shifted one way, while those for negative peaks will shift in the opposite direction. Thus a perfectly spaced sequence of positive and negative peaks in the input waveform will appear to be pulled closer together in pairs in the output pulses.

The pulse pairing error can be observed by feeding a balanced fixed-frequency signal into the differentiator inputs and viewing the digital pulse output on an oscilloscope. The oscilloscope is triggered on successive leading edges. The second pulse after the trigger point will show two traces spaced at twice the pulse pairing error since each pulse is shifted by the same amount in opposite directions. An example of such a measurement is shown in Figure 3.

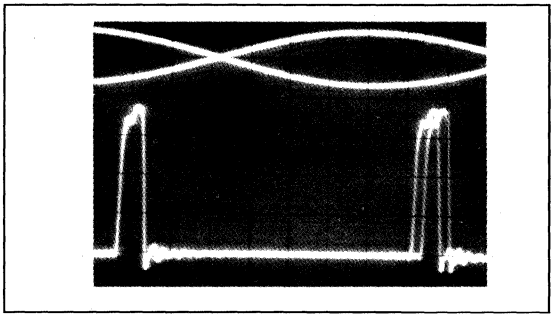

Figure 3: Oscilloscope traces showing the input signal (top) and the pulse output signal with pulse pairing. The shift in the second pulse is twice the pulse pairing error dt because it shows two pulses shifted in opposite directions.

The contribution to pulse pairing error from comparator offset for a sinusoidal input of form $V(t) = Vpeak \sin(\omega t)$ can be determined analytically as shown in Figure 2. The slope of the sinusoid at the zero crossing is $[dV/dt]0 = \omega\, Vpeak = (2\pi f)\, Vpeak$. Thus a voltage shift of V_{OS} due to an offset translates to a time shift (assuming that the shift is a small part of the signal period) of:

$$\Delta t = V_{OS}/[dV/dt]0 = (1/2\pi f)\,(V_{OS}/V_{peak}) = (T/2\pi)\,(V_{OS}/V_{peak}) \quad \textit{(eq. 1)}$$

where T is the period of the sinusoid.

The time shift dt is called the ***pulse pairing shift***, or more commonly just the ***pulse pairing***. It is the shift of an individual peak due to the offsets in the circuitry.

For a sinusoidal signal a more exact analysis gives

$$\Delta t = (1/2\pi f)\,\arcsin(V_{OS}/V_{peak}) = (T/2\pi)\,\arcsin(V_{OS}/V_{peak}) \quad \textit{(eq. 2)}$$

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This result is important in that sinusoidal signals are often used for test purposes, and this formula allows one to relate the observed pulse pairing error for a sine wave to the offset. A sine wave is, of course, somewhat unrealistic.

A more realistic case is shown in Figure 4, for a READ signal given by:

$$VR(t) = (5/6)\,V0\,[\sin(\omega t) - (1/5)\sin(3\omega t)] \quad \textit{(eq. 3)}$$

so that the differentiator waveform $V_D(t)$ takes the form

$$V_D(t) = (5/8)\,V_{peak}\,[\cos(\omega t) - (3/5)\cos(3\omega t)] \quad \textit{(eq. 4)}$$

$$dV_D/dt = (5/8)\,\omega V_{peak}\,[-\sin(\omega t) + (9/5)\cos(3\omega t)] \quad \textit{(eq. 5)}$$

The derivative waveform has its zero crossings when $\omega t = \pi/2$, thus:

$$[dV/dt]\,0 = (5/8)\,\omega V_{peak}\,[-\sin(\pi/2) + (9/5)\sin(3\pi/2)]$$
$$= (5/8)\,\omega V_{peak}\,[-1-(9/5)] = -(7/4)\,\omega V_{peak} \quad \textit{(eq. 6)}$$

from which we find a pulse pairing shift (magnitude)

$$t = V_{OS}/[dV/dt]\,0 = (4/7)\,(1/2\pi f)\,(V_{OS}/V_{peak})$$
$$= (0.57T/2\pi)\,(V_{OS}/V_{peak}) \quad \textit{(eq. 7)}$$

which is substantially less than for the sine wave case. This difference arises from the fact that in a real READ waveform the differentiated signal ***flattens out*** between pulses, so that zero crossings are steeper and an offset has a relatively smaller effect. Real READ waveforms probably fall somewhere in between equations (1) and (7). The magnitude of this effect will vary from inner tracks (where the pulses are crowded) to outer tracks.

Stated in another way, we have shown that the effect of higher odd harmonics in the READ signal is to decrease the pulse pairing error, so that equation (1) can be viewed as a worst case.

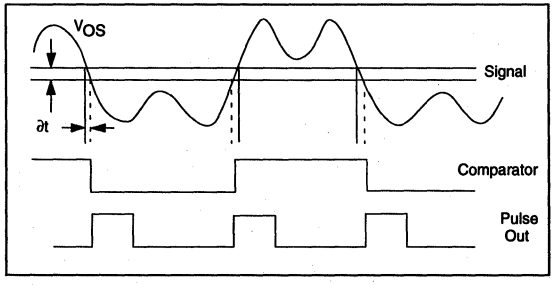

Figure 4: READ channel waveforms for an input signal (defined by equation 3) with substantial harmonic content as occurs in real READ data signals[2].

[2] If the input signal corresponds to an evenly spaced sequence of flux reversals, the READ signal will contain the fundamental frequency and as many odd-order harmonics as the amplifier bandwidth permits. The third harmonic can be expected to be dominant.

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VTC Inc.
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PHASE-LOCKED LOOP APPLICATION FUNDAMENTALS FOR DISK DRIVES

August, 1994

SUMMARY

Phase-locked loops (PLLs) are widely used in disk drives to recover the READ clock and to generate the WRITE clock at a variety of frequencies as needed for zoned-density recording. Such PLLs have off-chip components such as capacitors and resistors as well as on-chip registers (for division ratios, DAC inputs, etc.), which allow performance to be tailored to a given set of requirements. This application note describes typical PLLs in hard disk drives, how to select external components and internal register values, and the trade-offs and optimizations that a user will need to understand when designing with PLLs.

INTRODUCTION

The reading of data from a disk drive is an asynchronous operation. The rotation of the disk is not synchronized with the system clock and the pulse peaks representing flux reversals can have any phase with respect to the system clock. It is necessary to extract a read clock from the data itself. The read clock establishes the timing of proper bit-cell boundaries, and is used to determine the bit value (0 or 1) within each read-data window. Read clock extraction is done using a phase-locked loop which employs negative feedback to force a voltage-controlled oscillator (VCO) to be in synchronism with the read signal.

Most disk drives use zoned-density recording (ZDR) today. The disk rotation rate is fixed, but a higher data frequency is used near the outer diameter (OD) than at the inner diameter (ID) such that the physical width of a bit cell is kept approximately the same over the whole disk area. A zone is defined between two radii r_1 and r_2, and a typical drive will have from four to twenty zones in all. The write frequency is constant within a given zone. This requires different write frequencies be generated in each zone. For this purpose a type of phase-locked loop called a frequency synthesizer is used to derive multiple output frequencies from a single input frequency.

This report describes phase-locked loops in the form commonly used in disk drives, and includes a systematic mathematical analysis of PLL loop dynamics in both the time and frequency domain. Then two types of applications are described, data separators and frequency synthesizers, and the selection of the user-specified parameters (capacitors, resistors, divider ratios, etc.) are discussed in terms of the performance objectives for each device.

The scope of this application note is limited to the common concerns of disk drive designers. Phase-locked loops are a large subject and several excellent texts exist which cover further details beyond the scope of this report. References can be found at the end of this report.

PLL Basics: Time Domain

Figure 1 shows a generic phase-locked loop with a lead/lag loop filter (R, C_1, C_2). The input frequency is f_i and the output frequency is f_o. f_o is locked to have some exact ratio to f_i. The input may be a crystal-controlled reference frequency, a reference clock from the servo PLL, or it may be digital data from which a clock is to be extracted.

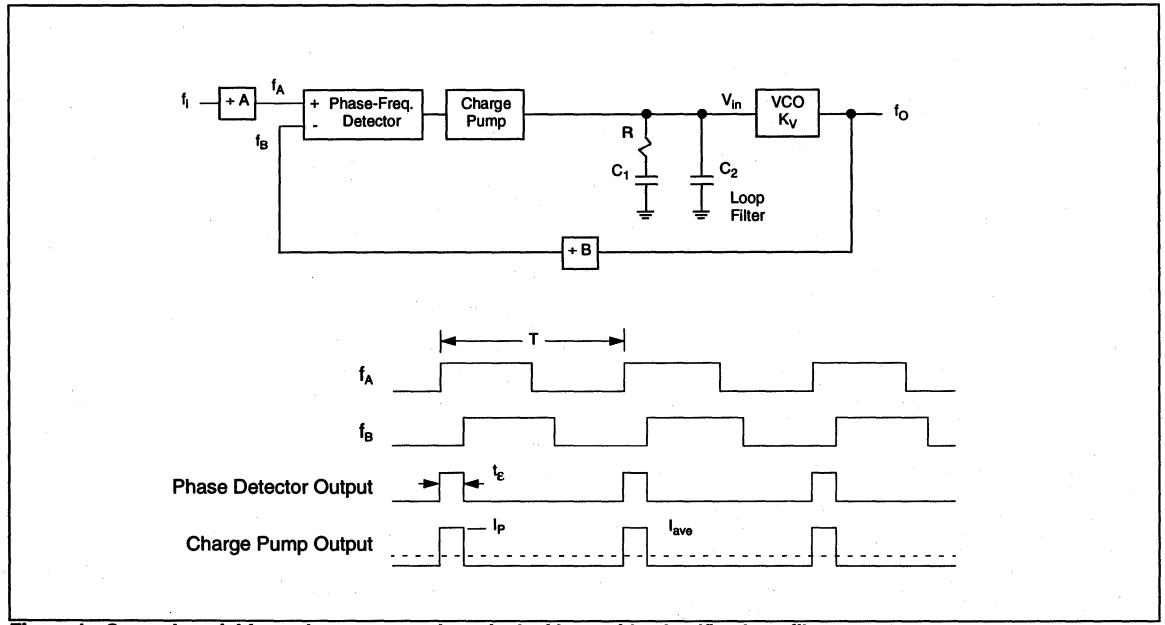

Figure 1: General model for a charge-pump phase-locked loop with a lead/lag loop filter.

APPLICATION NOTES

The input frequency is divided by A, which is an integer, using a digital frequency divider. This produces a frequency f_A at the positive input to the phase-frequency detector.

$$f_A = \frac{f_i}{A} \qquad \textit{(eq. 1)}$$

The VCO output frequency is similarly divided by an integer B, producing a frequency f_B, which is fed into the negative input of the phase-frequency detector.

$$f_B = \frac{f_o}{B} \qquad \textit{(eq. 2)}$$

The phase-frequency detector puts out a string of pulses with a width t_ε, equal to the time difference between the rising edges of f_A and f_B, which is fed into the charge pump. The charge pump puts out a similar string of current pulses of width t_ε and amplitude I_p which are fed into the loop filter. The current pulses can be positive or negative depending on the phase relation between f_A and f_B. This current is averaged over many cycles by the loop filter capacitors. Thus, in the steady state (or locked) condition where time periods are long compared to $T = 1/f_A = 1/f_B$, we can represent the current by its average value,

$$I_{ave} = I_p\left(\frac{\tau_\varepsilon}{T}\right) \qquad \textit{(eq. 3)}$$

The value of I_p is user-controlled in most cases. The loop filter stores the charge pumped by the charge pump on capacitors C_1 and C_2 (ordinarily $C_1 >> C_2$) and in the steady state, produces a voltage V_{in} given approximately by

$$V_{in} = \left(\frac{1}{C_1}\right)\int I_{ave}dt \qquad \textit{(eq. 4)}$$

Note, that in this simplified discussion we treat the filter as a capacitor (neglect R and C_2). In a real PLL, the resistor R is used to put a zero into the transfer characteristics which improves stability. If the loop had only R and C_1 the stability would be OK, but the pump current would produce a very large instantaneous voltage drop across R putting a voltage spike into the VCO and causing problems. Capacitor C_2 is added to reduce these voltage spikes. Also, we assume the value of R is low compared to the impedance of C_1 at all frequencies of interest.

Thus, the VCO converts its input voltage V_{in}, to an output frequency f_o with a transfer gain of K_V given by,

$$f_o = K_V V_{in} \qquad \textit{(eq. 5)}$$

The output frequency f_o is divided by B to complete the loop. This arrangement can be thought of as a negative feedback scheme. The phase-frequency detector produces an error signal proportional to the phase difference between f_A and f_B. The loop filter and VCO are connected so as to force f_A and f_B to be in phase. With ideal components, the phase difference is forced to exactly zero.

To get a better understanding of the situation consider the case where f_A and f_B are out of phase, with f_A leading f_B, as shown in the timing diagram of Figure 1. The phase-frequency detector output turns on the charge pump for a time t_ε pumping a charge Q_ϕ into the loop filter with a value of,

$$Q_\phi = I_p t_\varepsilon \qquad \textit{(eq. 6)}$$

This charge increases the voltage at V_{in} by

$$\Delta V = \frac{Q_\phi}{C_1} \quad (C_1 >> C_2) \qquad \textit{(eq. 7)}$$

and f_o will increase by

$$\Delta f = K_V \Delta V_{in} \qquad \textit{(eq. 8)}$$

With the frequency increasing, the rising edges of f_B will now occur earlier in time. This causes the next t_ε pulse to be shorter and the process continues until $t_\varepsilon = 0$ (at which point f_A and f_B are in phase), $I_{ave} = 0$, and V_{in} is constant in time. A similar argument can be made if f_A lags f_B. Since f_A and f_B are equal in phase and frequency then,

$$f_o = \left(\frac{B}{A}\right) f_i \qquad \textit{(eq. 9)}$$

This is the basic frequency synthesizer equation. A very large number of output frequencies can be produced by simply changing the frequency division ratios A and B.

The model presented above can be used for a data separator (data synchronizer) PLL, if we set A = 1 and let B represent the number of cycles between nearest 1 bits. While the input to the frequency synthesizer is a simple square wave, a data separator will have many different data periods occurring in random order as dictated by the particular data stream of interest. For (1,7) code, 1 bits are always isolated; there may be from one to seven 0 bits between 1 bits. In other words, when we are locking to a real data stream there are many frequencies in the input. We must consider all values of B compatible with the code used in the given application.

One final note, it should be obvious from the PLL description given that if a long string of 0 bits appear in the data there will be no transitions (edges) and the PLL will lose track of the phase value. The PLL views such a data sequence as DC and reacts by pushing the PLL frequency toward zero. This is the reason for run-length limited (RLL) codes because they impose limitations on the lengths of runs of same-type symbol.

PLL Blocks

It is desirable that the user of PLLs have an idea of how the main circuit blocks work at the transistor level. In this section we give typical simplified schematics of phase detectors, charge pumps, and voltage-controlled oscillators (VCOs).

(a) Phase detectors. Phase detection is generally done using logic circuits. Such digital circuits handle phase as an analog quantity by using pulse width as an analog variable. The most commonly used phase detector is shown in Figure 2a and is a phase-frequency detector (see [3] on page 26).

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Figure 2a

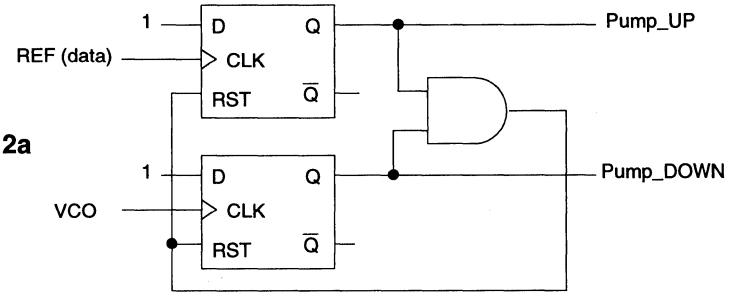

Figure 2b

Figure 2c

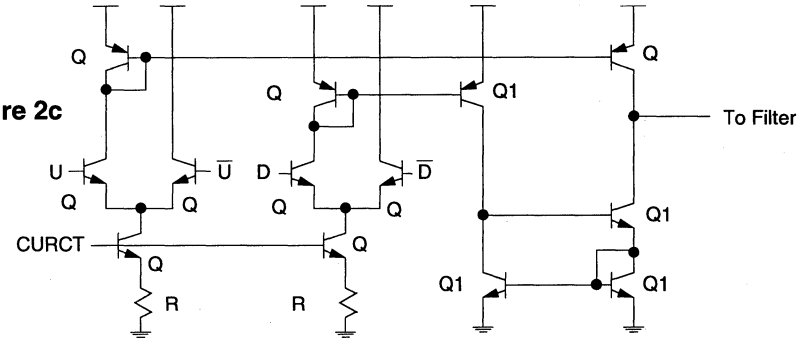

Figure 2d

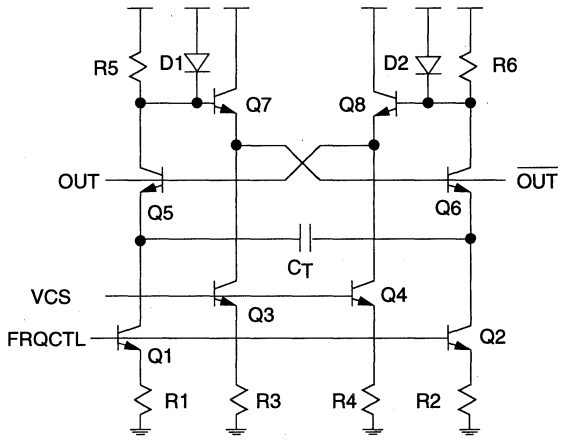

Figure 2: Typical circuitry in PLL blocks. (a) Phase-frequency detector. (b) Phase detector. (c) Charge pump. (d) Voltage-controlled oscillator.

The reference frequency (data)[1] is fed into the clock input of one edge-triggered D flipflop and the VCO output is fed into the other. The true outputs are ANDed together and fed back to asynchronous reset inputs for both flipflops. To understand the circuit operation, first consider the situation where the rising edges of the VCO pulses arrive later than those of the reference frequency. This means that the VCO phase is lagging, and we need to increase its frequency to catch-up. Assume an initial state where both flipflops have Q = 0 (the usual case). The reference rising edge arrives first and causes the Q output of the upper flipflop to go to a 1. This signal is called PUMP_UP and is used to turn on a current source which feeds current into the filter. The rising edge of the VCO output arrives later and causes the lower flipflop to be set to Q = 1. This causes a 1 to appear at the output of the AND gate, which feeds back to return both flipflops to the initial Q = 0 state and turns off the PUMP_UP current source. The cycle then repeats.

It is obvious from this description that the positions of waveform edges are the only thing that counts here, and that the phase error is in-effect sampled once per edge.

This type of phase-frequency detector has a practical problem when the phase error is very small. In real flipflops the Q output will not get fully flipped before the reset action comes around. This is described as a dead band which happens with nearly zero phase error and can cause erratic operation. One solution to this problem is to insert extra gate delays after the AND gate so, that in the locked condition, both pump-up and pump-down pulses are of finite, but equal width. With the averaging effect of the filter, the pulses will cancel each other out.

Figure 2b shows an alternative type of detector called a phase or phase-only detector (see [3] on page 26). It is simply an exclusive-OR gate. Here the single output is used to cause a pump-up condition when 1 or a pump-down condition when 0. A little thought shows that the steady-state condition of the circuit occurs when the pump-up and pump-down pulses occur with equal duty cycle and this can only occur when the two inputs (VCO and REF) are 90° out of phase (i.e., shifted by T/4, where T = 360°).

The phase-frequency detector has the desirable property that it shows little tendency to lock on harmonics (see [3] on page 26)

(b) Charge pumps. A typical charge pump circuit is shown in Figure 2c. The U and D inputs and their complements are the PUMP_UP and PUMP_DOWN outputs of Figure 2a, suitably level shifted. The pump current is generated by the current sources Q1, Q2, R1, R2 and is controlled by the CURCTL analog input which allows the value of the pump current to be changed (DAC-controlled, for example). In the normal condition (U = D = 0), the pump current is steered to VCC through Q4 and Q6, but when either U or D is high it is fed to one of the current mirrors (Q7, Q8 and Q9, Q10). The PUMP_DOWN current is again mirrored by Q11-Q13 so that it turns on a current sink. The up and down pulses are then combined at the collectors of Q11 and Q8 and this net current is fed to the filter.

This circuit has a number of nonidealities. The collector currents of Q8 and Q11 must match exactly for ideal operation. If they do not, a steady-state phase error will occur. But in reality component mismatches of this sort cause only small deviations from this condition. The pump-down current must pass through the extra mirror Q11-Q13 and this has a small effect on current matching and current switching dynamics. The collector currents of Q8 and Q11 are not completely independent of the DC voltage at the filter (the Early effect) and this is an additional source of error. Practical charge pumps often contain additional circuitry to cancel or correct these errors. In general, charge pumps work much better if fast PNP transistors are available in the process.

(c) VCOs. The circuit of Figure 2d is often called an emitter-coupled multivibrator and is very widely used for VCOs (see [6] on page 26). The current sources Q1, Q2, R1, R2 set up two equal currents IO, with the value of the current controlled by the voltage FRQCTL which comes from the filter output[2]. In the two half-cycles of circuit operation there is current through R5 and not through R6 or vice versa . Let us begin by assuming a state where there is current in R5, and none in R6. R5 has a relatively high value, so some of the collector current of Q5 flows through D1, which effectively clamps the voltage at the base of Q7 at VCC - V_{be}. Thus the base of Q5 will have a potential about V_{be} higher than Q6. Both currents IO pass through the emitter of Q5, one directly and the other through timing capacitor C_T. As current passes through C_T, it is gradually discharged and the potential at the emitter of Q6 ramps down, eventually becoming low enough that Q6 can turn on. When this point is reached, there is a very rapid regenerative (positive feedback) switching event which flips the circuit to the other half-cycle. A half-cycle requires that a current IO change the voltage across C_T by $2V_{be}$, so that period $T = 1/f \approx 4V_{be}CT/IO$. Note that the frequency is proportional to the current IO (and also FRQCTL) — important for a linear PLL. The inherent 50% duty cycle of the complementary outputs from this circuit is a desirable feature.

The circuit as shown has a few problems. For one thing the frequency is temperature-dependent through $V_{be}(T)$. There are also tolerance questions since the VCO center frequency must be controlled to fairly close limits. Practical VCOs of this class incorporate additional circuitry for wide-range temperature-independent operation. There is often extra circuitry which can freeze the VCO in one half-cycle, so that it can then be started in synchronism with a detected read-data edge thus shortening the lock-on transient (this feature is called zero-phase restart). Another important feature is input clamping. The circuitry must be designed in such a way that the frequency can vary only between two values f_1 and f_2. If the frequencies are too low(e.g., too-low FRQCTL values) the oscillator may simply stop oscillating, and there may be no recovery from this extreme nonlinear condition. If the allowed range is too broad, there is a potential for locking on harmonics with equally disastrous results.

Early data separators had capacitor C_T off-chip so that it was user-selected. Today most integrated PLLs have C_T on-chip so that a much lower C_T value can be used and power saved. With fast-switching transistors on-chip VCOs usable to beyond 300 MHz have been built.

When very low phase jitter is desired (as in a frequency synthesizer) great care must be taken to prevent crosstalk (e.g.,

[1] This input is the reference frequency for a synthesizer or the data for a data separator.

[2] Often a unity-gain buffer is placed between filter and VCO, designed in such a way as to drain minimal current form the filter capacitors during a hold condition. Otherwise the filter would have to supply base current for Q1 and Q2.

from clocks, switchmode power supplies, etc.) from the VCO to extraneous signals. This requires good chip design, careful board layout, and bypassing by the user.

Frequency-Domain Description of a PLL; Overshoot and Stability

In our simple time-domain analysis of the PLL in Figure 1 we neglected the effects of C_2 and R as nonessential to a basic qualitative explanation. In reality, all three filter elements are necessary for satisfactory operation. A full analysis of the charge pump PLL including a description of the action of the lead-lag filter requires a more rigorous treatment of the PLL and that is provided here.

In the simple picture treated earlier (neglecting R and C_2) we saw that if f_A leads f_B the negative feedback action will steadily increase the VCO frequency until the phase difference is zero. Actually, when the phase difference has reached zero, the VCO frequency will be substantially higher than its steady-state center frequency, f_o. Thus, the phase will continue to decrease and pass through the zero-phase point, becoming negative, and a new correction cycle will begin. If the loop filter is only a capacitor, the PLL exhibits substantial overshoot in its phase dynamics. The additional filter elements R and C_2 allow the user to control this overshoot and optimize the phase dynamics[3].

We will assume that the loop is running near its center frequency, f_o. We also assume that any changes in the input phase difference or the VCO frequency occur slowly enough that f_B and f_A differ by only a small amount, but can have any phase relationship. Phase can be thought of as the relative position of the rising edge of one signal as compared to a second signal, divided by the period T ($T \approx 1/f_A \approx 1/f_B$).

In reality, a PLL of this kind is a sampled-data system. The phase is only defined at the edges of the f_A and f_B signals (see [1] on page 26) In our analysis we are in effect making a continuous approximation, i.e., that the highest frequencies in the behavior of the loop dynamics are much less than the center frequency, or equivalently, that the bandwidth of the loop filter is much less than the center frequency. In Nyquist terms, we are assuming that there are many samples per period for the shortest period in the loop response. Most practical PLLs operate in this regime. At the same time we are in effect considering only the linear behavior of the system so that the ordinary ideas of linear system theory apply. With large phase and frequency deviations the system will show nonlinear behavior, and in fact the initial capture transient is always nonlinear (see,, and). A rigorous sampled-data treatment has been given by Gardner (see [1] on page 26)

Mathematically, the phase $\Theta(t)$ (units radians) is the time integral of the angular frequency ω

$$\Theta(t) = \int \omega dt \quad \text{where } \omega = 2\pi f \qquad \textit{(eq. 10)}$$

The f_A and f_B signals can be described by their phases $\Theta_A(t)$ and $\Theta_B(t)$. The phase-frequency detector thus puts out an error phase $\Theta_\varepsilon(t)$ equal to the phase difference of $\Theta_A(t)$ and $\Theta_B(t)$ (this is the analog equivalent of the time error t_ε in the PLL Basics section).

$$\Theta_\varepsilon(t) = \Theta_A(t) - \Theta_B(t)$$
$$t_\varepsilon = \left(\frac{\Theta_\varepsilon(t)}{2\pi}\right)T \qquad \textit{(eq. 11)}$$

The average charge pump current will be

$$I_{ave} = I_p\left(\frac{t_\varepsilon}{T}\right) = \left(\frac{I_p}{2\pi}\right)(\Theta_\varepsilon(t) \equiv K_{cp}\Theta_\varepsilon(t)) \qquad \textit{(eq. 12)}$$

The loop filter impedance is Z_F, so

$$V_{in} = I_{ave}Z_F \qquad \textit{(eq. 13)}$$

The VCO converts its input voltage V_{in} to an output frequency f_o

$$f_o = K_V V_{in} \quad \text{or} \quad \omega_o = K_{vco}V_{in} \qquad \textit{(eq. 14)}$$

where $K_{VCO} = 2pK_V$. Thus, the VCO output phase is

$$\Theta_o(t) = \int \omega_o dt \qquad \textit{(eq. 15)}$$

The frequency dividers scale the phase as well as the frequency, so

$$\Theta_B(t) = \frac{\Theta_o(t)}{B}, \qquad \Theta_A(t) = \frac{\Theta_i(t)}{A} \qquad \textit{(eq. 16)}$$

Combining the equations, we find that

$$\Theta_B(t) = \left(\frac{K_{VCO}}{B}\right)\left(\frac{I_p}{2\pi}\right)\int\{Z_F[\Theta_A(t) - \Theta_B(t)]\}dt \qquad \textit{(eq. 17)}$$

Taking the Laplace transform of this equation (which puts things in terms of the complex frequency variable s), we find

$$\Theta_B(s) = \left(\frac{1}{s}\right)\left(\frac{K_{VCO}}{B}\right)\left(\frac{I_p}{2\pi}\right)Z_F(s)(\Theta_A(s) - \Theta_B(s)) \qquad \textit{(eq. 18)}$$

where,

$$Z_F(s) = \frac{\left(R + \frac{1}{sC_1}\right)\left(\frac{1}{sC_1}\right)}{R + \frac{1}{sC_1} + \frac{1}{sC_2}}$$

$$= \frac{R\left(s + \frac{1}{RC_1}\right)}{sC_2R\left[s + \frac{1}{RC_1}\left(\frac{C_1 + C_2}{C_2}\right)\right]} \qquad \textit{(eq. 19)}$$

[3] The frequency and phase in a PLL behave like the displacement and momentum of a simple mechanical oscillator and many analogies can be drawn. In most practical cases the behavior is oscillatory. When the phase error is at a maximum the frequency error will be zero and conversely during a system transient.

APPLICATION NOTES

In what follows we will use the phases as independent variables in describing the loop dynamics, as shown in the signal-flow diagram of Figure 3.

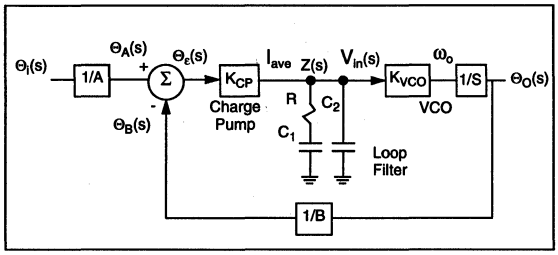

Figure 3: Signal flow diagram for a phase-locked loop with a lead-lag loop filter.

Putting in the explicit form of $Z_F(s)$ we can now write $\Theta_B(s)$ as

$$\Theta_B(s) = \frac{K_{VCO}K_{CP}R\left(s+\frac{1}{RC_1}\right)}{Bs^2C_2R\left[s+\frac{1}{RC_1}\left(\frac{C_1+C_2}{C_2}\right)\right]}(\Theta_A(s)-\Theta_B(s)) \qquad \textit{(eq. 20)}$$

This is the transfer function for $\Theta_B(s)$ in the complex frequency domain. Both the numerator and denominator are polynomials in s. Thus, $\Theta_B(s)$ can be described by an amplitude and phase response, a Bode plot, etc., like any other dynamical variable. We can also consider the amplitude response of the phase and the phase response of the phase, just as for an amplifier.

A word of caution. Unlike a feedback amplifier where the transfer function of interest is voltage gain, a phase-locked loop deals with phase gain. The transfer function has real and imaginary components which can be described in terms of a magnitude and angle (or argument). For a feedback amplifier the angle is actually the phase of the signal. It is rather easy to comprehend the gain and phase of an amplifier and consequently the angle of the complex transfer function is routinely referred to as phase. In the case of a PLL, however, the magnitude of the transfer function is the phase gain while the angle represents a time delay of the phase gain. It is tempting to refer to the angle as the phase and retain terms like phase margin that most users are already familiar with from amplifier analysis. Thus, we have the phase of the phase which can be rather confusing. The solution to this quandary is to treat the frequency domain phase variable as just a gain variable with real and imaginary parts, which have mathematical and graphical stability properties that are true regardless of the particular PLL application. When insight and intuition are needed the reader can return to the time domain, at least mentally, and not worry about the true meaning of phase. Here the magnitude of the transfer function will be referred to as phase gain while the angle will simply be called the angle. The term phase margin will still be used to refer to the angle of the transfer function in relation to 180°.

The closed-loop gain of the system is denoted by H(s), and is the gain from input $\Theta_A(s)$ to output $\Theta_B(s)$,

$$H(s) = \frac{\Theta_B(S)}{\Theta_A(s)} \qquad \textit{(eq. 21)}$$

The significance of this is that if the input phase is phase modulated at some frequency **S** with a phase deviation **X**, then the output will be similarly phase modulated with a phase deviation H(s)x (the amplitude response in this case). There will also be a phase difference between these input and output phase deviations, i.e., they are not simultaneous in time, and this is the phase response of the PLL phase error.

The open-loop gain of the system is denoted G(s) and is the phase gain from input to output if the feedback loop is broken. This is equivalent to the gain from $\Theta_\varepsilon(s)$ to $\Theta_B(s)$, or

$$G(s) = \frac{\Theta_B(S)}{\Theta_\varepsilon(s)} = \frac{\Theta_B(s)}{(\Theta_A(s)-\Theta_B(s))} \qquad \textit{(eq. 22)}$$

Thus G(s) = H(s)/(1 - H(s)) and H(s) = G(s)/(1 + G(s)). From the relations above

$$G(s) = \frac{K_{VCO}K_{CP}R\left(s+\frac{1}{RC_1}\right)}{Bs^2C_2R\left[s+\left(\frac{1}{RC_1}\right)\left(\frac{C_1+C_2}{C_2}\right)\right]} \qquad \textit{(eq. 23)}$$

Let, $\tau = RC_1$

$\omega_1 = 1/t = 1/RC_1$

$K = (K_{VCO}\,K_{CP}\,R)/B = K_V\ I_p\ R/B$

$b = 1 + (C_1/C_2) = (C_1 + C_2)/C_2$

$\omega_2 = b\omega_1 = [(C_1 + C_2)/C_2]/RC_1$

then,

$$G(s) = \frac{K(\omega_2-\omega_1)(s+\omega_1)}{s^2(s+\omega_2)} \qquad \textit{(eq. 24)}$$

The open-loop response of the system is third-order, type II (see and). There are two poles at s = 0, a third pole at s = $-\omega_2$, and a zero at s = $-\omega_1$. Insight into the loop behavior can be gained by drawing a Bode plot of G(jω) as shown in Figure 4

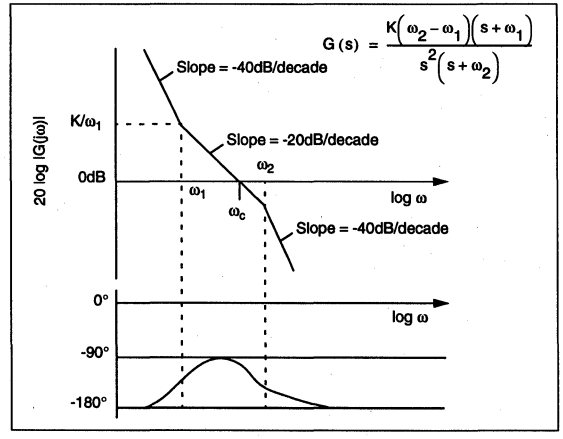

Figure 4: Bode plot of the open-loop response G(jω) for a charge-pump PLL.

The open-loop response is infinite when $\omega = 0$ and rolls off at -40 dB/decade due to the two poles at the origin until $\omega = \omega_1$. This zero cancels one of the poles causing the response to roll off at -20dB/decade until $\omega = \omega_2$. At this point it rolls off again at -40dB/decade due to the pole at $-\omega_2$. The angle of $G(j\omega)$ starts at -180° and rises to -90° at some point above $\omega = \omega_1$, and then returns to -180° beyond $\omega = \omega_2$.

We recall from linear system theory that for a system to be stable, the angle of the transfer function at the frequency where $|G(j\omega)| = 1$ should be more than 45° from -180° (in a feedback amplifier system this is referred to as phase margin)[4]. From the Bode diagram, we see that this can only happen if $|G(j\omega)|$ crosses the unity-gain axis at a point where the slope of $|G(j\omega)|$ is -20dB/decade.

The frequency at which $|G(j\omega)| = 1$ is called the crossover frequency ω_c. As seen from the Bode diagram:

$$|G(j\omega)| = 1 \quad @ \quad \omega = \omega_c \qquad \textit{(eq. 25)}$$

A necessary condition for stability is

$$\omega_1 < \omega_c < \omega_2 \qquad \textit{(eq. 26)}$$

We also see that if ω_1 and ω_2 are too close to one another $\angle G(j\omega)$ will never rise much above -180°. According to Gardner [1], $\omega_2 > 9\,\omega_1$ for most practical cases. This fact can be used to simplify G(s). For $\omega << \omega_1$, $s + \omega_2 \approx \omega_2$ and $\omega_2 - \omega_1 \approx \omega_2$, so that

$$G(s) \approx \frac{K(s+\omega_1)}{s^2} \qquad \textit{(eq. 27)}$$

Using the assymtptotic approximation characteristics of the Bode Diagram:

$$|G(\omega_1)| = \frac{K}{\omega_1} \qquad \text{for} \omega_1 << \omega_c << \omega_c \qquad \textit{(eq. 28)}$$

If $\omega_c << \omega_2$, and $\omega_c >> \omega_1$, then:

$$|G(\omega_c)| = 1 = \frac{K}{\omega_c} \Rightarrow \omega_c = K \qquad \textit{(eq. 29)}$$

The unity gain or crossover frequency for the loop is equal to K, which is known as the loop gain. ω_c is often referred to as the loop bandwidth since it represents the frequency above which frequency variations are filtered out of the loop. The loop is said to track any change in input frequency below ω_c. In a data synchronizer application the loop bandwidth should be set high enough so that bit shifts due to mechanical inaccuracies in the drive will be tracked by the loop. In a frequency synthesizer, however, loop bandwidth is generally set low so that any jitter in the input frequency (from a switching power supply for example) will be filtered out.

Thus we see that loop gain and the loop bandwidth are actually the same thing. This seems somewhat puzzling intuitively, but if the third-order loop equation is inspected we see that K must have units of frequency. Remember too that the VCO in effect integrates frequency into phase, yielding the additional 1/s term which must be accounted for in the units for K, so that G(s) is unitless.

We now consider the closed-loop response H(s)

$$\frac{\Theta_B(S)}{\Theta_A(S)} = H(s) = \frac{G(s)}{1+G(s)}$$

$$= \frac{K(\omega_2-\omega_1)(s+\omega_1)}{s^3 + \omega_2 s^2 + K(\omega_2-\omega_1)s + K(\omega_2-\omega_1)\omega_1} \qquad \textit{(eq. 30)}$$

In general this is a third-order polynomial and there are no simple formulas for the roots (zeroes). A number of inexpensive programs are available which can find the roots of any reasonable polynomial.

If $\omega_2 >> \omega_1$, which we know must be true from the open-loop stability analysis, then we can approximate the loop as second order by letting ω_2 approach infinity giving,

The denominator is a quadratic second order which can be rewritten as

$$H(s) = \frac{K(s+\omega_1)}{s^2 + Ks + K\omega_1} \qquad \textit{(eq. 31)}$$

where $\omega_n = [K\omega_1]1/2$ and $\zeta = (1/2)[K/\omega_1]^{1/2}$. ω_n is called the natural frequency of the loop and ζ is known as the damping factor. The poles of H(s) are found by solving the equation

$$s^2 + s\zeta\omega_n s + \omega_n^2 \qquad \textit{(eq. 32)}$$

When this is done we find the poles P_1 and P_2 are:

$$P_1, P_2 = -\omega_n\left[\zeta \pm \left(\zeta^2 - 1\right)^{1/2}\right] \qquad \textit{(eq. 33)}$$

Different values of ζ lead to the following three cases:

1. If $\zeta > 1$, then P_1 and P_2 are real and the ioop is unconditionally stable and is said to be overdamped.
2. If $\zeta = 1$, then $P_1 = P_2 = \omega_n$ and the loop is unconditionally stable and is said to be critically damped.
3. If $\zeta < 1$, then P_1 and P_2 form a pair of complex conjugate poles and the loop becomes less stable as ζ approaches 0 and is said to be underdamped.

The damping concept should be familiar from other disciplines (such as mechanics). Often the loop is specified to have a desired damping factor ζ and loop bandwidth ω_c. Damping is of practical importance in disk drive design because we require that the phase errors[5] of the recovered read clock be settled to some specified degree before we regard the recovered data as valid. It is the damping which determines how long it takes the phase error to settle to zero.

[4] The condition is often stated in the form that oscillation will occur if the phase response is 360°. In our case a feedback transfer function phase response of 180° will lead to oscillation because the inherent negative feedback (inversion) in the phase detector is equivalent to a 180° phase shift.

[5] That is to say, the pahse difference between the VCO output and the peaks in an ideal read signal.

APPLICATION NOTES

There are a number of useful identities for the second-order loop:

$$\omega_n = (K\omega_1)^{1/2} = \left(\frac{K}{\tau}\right)^{1/2}$$

$$= \left(\frac{\omega_c}{\tau}\right) = (\omega_c\omega_1)^{1/2}$$

$$\zeta = \left(\frac{1}{2}\right)\left(\frac{K}{\omega_1}\right)^{1/2} = \left(\frac{1}{2}\right)(K\tau)^{1/2}$$

$$= \left(\frac{1}{2}\right)(\omega_c\tau)^{1/2} = \left(\frac{1}{2}\right)\left(\frac{K\omega_c}{\omega_1}\right)^{1/2} \quad \textit{(eq. 34)}$$

thus,

$$\omega_c = K = 2\zeta\omega_n,\ K\tau = \frac{\omega_c}{\omega_1} = 4\zeta^2,$$

$$\frac{K}{\tau} = \omega_c\omega_1 = \omega_n^2,\ \omega_n\tau = \frac{\omega_n}{\omega_1} = 2\zeta \quad \textit{(eq. 35)}$$

The loop is completely specified with either pair of variables K and τ or ω_n and ζ, and one set can be calculated from the other.

The loop transient response is of interest. An underdamped system is fairly responsive but tends to overshoot and ring. An overdamped system has no overshoot but is rather slow in reaching its final steady-state value when responding to a transient input. It can be shown (see and) that a damping factor of $\zeta = 0.707 = 1/\sqrt{2}$ will yield an optimal transient response to a frequency ramp input. Here the phase of the output will reach its final steady state output in 3.4 $\omega_n t$ with 5% overshoot. Generally most data synchronizers have ζ between 0.5 and 0.8 so that they can acquire lock quickly at the beginning of a read cycle . The noise bandwidth B_L of a second-order PLL is given by.

$$B_L = \left(\frac{\omega_n}{2}\right)\left[\zeta + \frac{1}{4\zeta}\right] = \frac{1}{4}(\omega_c + \omega_1) \quad \textit{(eq. 36)}$$

An input noise signal at frequencies above B_L will be filtered out of the loop. B_L is at a minimum of $0.5\omega_n$ for $\zeta = 0.5$, but is still only 0.53 at $\zeta = 0.707$. In a frequency synthesizer noise filtering is important and consequently it has a damping factor range of about 0.5 to 1.0 as well.

Component Selection for the Second-Order Loop

Choosing the resistor and two capacitors in the lead/lag filter is one of the main problems facing the disk drive designer. Before proceeding the following parameters must be specified:

Charge pump gain:	$K_{cp} = I_p/2\pi$
VCO gain:	$K_{VCO} = 2\pi K_V$
Feedback divider ratio:	B
Loop bandwidth:	$f_c = \omega_c/2\pi = K/2\pi$
Damping factor:	ζ

The first three may be fixed by the monolithic design of the phase-locked loop, but for chips supporting zone-density recording they usually can be controlled by the user over some restricted range. The last two are always user-definable for devices with off-chip loop filter components.

In the second-order approximation, the capacitor C_2 should be chosen such that $C_2 \leq C_1/10$. This follows from the stability criteria, and is also required for the second-order approximation to be valid. We will not deal further in this section with the choice of C_2 as it is usually non-critical. The bigger C_2 is, however, the more the charge pump ripple is filtered, yielding steadier VCO input voltage.

The charge pump gain is usually specified as a current I_p. The VCO gain is usually given as K_V in MHz/V. Often the VCO gain scales with frequency and may be specified as a fixed fraction of the center frequency,

$$K_V = \alpha f_o \quad \textit{(eq. 37)}$$

where α generally ranges from 0.1 to 0.5. Note that α has units of 1/V. The feedback divider is simply an integer. Zone-programmable frequency synthesizers allow B to be changed, typically through a serial register interface. Data synchronizers sometimes allow the feedback divider to be programmed, but B as defined here also incorporates the effect of the data pattern. Thus, the effective B value will change as the data pattern varies from 01010 to 01000000010 (the extreme limits for (1,7) code). To ease confusion, B can be rewritten as the product of the internal hard-wired (or firmwired) divider ratio and the data pattern length. Let T_R be the relative data pattern length such that T_R = 2 for a 2T[6] pattern, 3 for a 3T pattern, etc., and let N be the hardware division ratio. Then

$$B = NT_R \quad \textit{(eq. 38)}$$

From the equations derived earlier

$$f_c = \frac{\omega_c}{2\pi} = \frac{K}{2\pi} = \frac{K_{VCO}K_{CP}R}{2\pi B}$$

$$= \frac{K_V I_p R}{2\pi B} = \frac{\alpha f_o I_p R}{2\pi N T_R}$$

$$\zeta = \left(\frac{1}{2}\right)\left(\frac{\omega_c}{\omega_1}\right)^{1/2} = \left(\frac{1}{2}\right)(2\pi f_c R C_1)^{1/2} \quad \textit{(eq. 39)}$$

Solving for R and C_1 we find

$$R = \frac{2\pi f_c B}{K_V I_p} = \frac{2\pi f_c N T}{\alpha f_o I_p}$$

$$C_1 = \frac{2\zeta^2}{\pi f_c R} = \left(\frac{\zeta}{\pi f}\right)^2 \frac{K_V I_p}{B} = \left(\frac{\zeta}{\pi f_c}\right)\frac{\alpha f_o I_p}{N T_R} \quad \textit{(eq. 40)}$$

[6] In disk drives a 2T pattern is a repeating 10, a 3T pattern is a repeating 100, 4T = 1000, etc.

The phase margin ϕ_R for the loop can be calculated by determining the angle of the open loop transfer function G(s) @ $\omega = \omega_c$ and subtracting -180°7. Using the second-order loop approximation

$$G(s) \approx \frac{K(s+\omega_1)}{s^2}$$

$$\angle G(j\omega_c) = \frac{\angle K(j\omega_c+\omega_1)}{(j\omega_c)}$$

$$= \tan^{-1}\frac{\omega_c}{\omega_1} - \pi$$

$$= \tan^{-1}\left(4\zeta^2\right) - \pi$$

$$\phi_R = \left[\tan^{-1}\left(4\zeta^2\right) - \pi\right] - (-\pi)$$

$$= \tan^{-1}\left(4\zeta^2\right) \qquad \textit{(eq. 41)}$$

From the results given in [4] this can be approximated as

$$\phi_R \approx 100\zeta \quad (\text{for}\phi_R \text{ in degrees}) \qquad \textit{(eq. 42)}$$

For a data synchronizer the phase margin and hence the damping factor, should be calculated for each data pattern to ensure stability of the loop. Generally phase margin should exceed 45°, which implies $\zeta > 0.5$. As an example,

$$\text{for}\zeta = 1/(\sqrt{2}) = 0.707, \quad \phi = 63.4° \qquad \textit{(eq. 43)}$$

Second Order Example Using the VM5351 Data Separator.

How do we best set up the variable loop parameters such as the filter components for (1,7) code using the second order approximation?

The phase-frequency detector is only active when there is an edge in the data input. In real data the edges are spaced far apart and this has the same effect on the loop as changing the feedback divider B. For (1,7) code the highest-frequency data pattern is a repeating 0101 pattern. This is called a 2T pattern because it has a period of 2T, where T is the period of the 1.5f code clock. Because it is necessary to generate both a 1f and a 1.5f clock from the data synchronizer loop, the VCO is often run at 3f so a divide-by-2 circuit can be used for the 1.5 f clock and a divide-by-3 circuit for the 1f clock. The frequency at f_B must be 1.5f so that a divide-by-2 circuit is needed in the feedback path. The 2T pattern acts like another divide-by-2, so

$$B = NT_R = 2 \bullet 2 = 4 \text{ for a 2T pattern}$$

The lowest-frequency pattern in (1,7) code is 01000000010 which has an 8T period. This is effectively a division ratio of 16, so

$$B = 2 \bullet 8 = 16 \text{ for an 8T pattern}$$

The filter components should be chosen to get satisfactory response under these extreme conditions, as well as, all pattern in between.

Code (1,7) or 2/3 RLL
NRZ Data Rate = 64Mbits/sec (= f)
VCO Center Frequency = f_o = 192MHz (= 3f)
REFOSC Frequency = 96MHz (= 1.5f)
Crossover frequency, ω_c = 1000K rad/s
$\zeta = 0.7$
Preamble length = 11 NRZ bytes (EDSI min.)
= 3.67µs (44 recorded pulses)

Refer to Figure 7. The impedance of the loop filter can be written as follows:

$$Z(s) = \frac{R\left(s+\frac{1}{RC_1}\right)}{sC_2R\left(s+\frac{1}{RC_1}+\frac{1}{RC_2}\right)} \qquad \textit{(eq. 44)}$$

The open loop gain is:

$$G(s) = \frac{K_{VCO}K_{CP}K_{div}R\left(s+\frac{1}{RC_1}\right)}{s^2C_2R\left[s+\frac{1}{RC_1}\left(\frac{C_1+C_2}{C_2}\right)\right]} \qquad \textit{(eq. 45)}$$

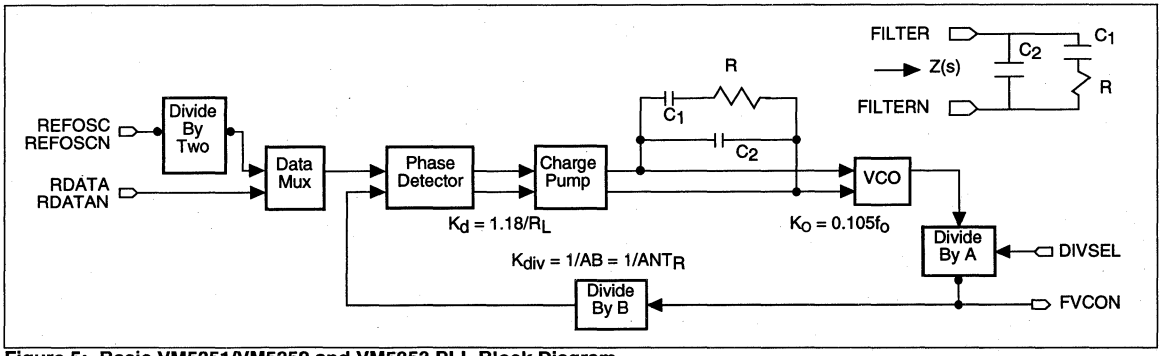

Figure 5: Basic VM5351/VM5352 and VM5353 PLL Block Diagram

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where, $K_{CP} = K_d = 1.18/R_L$,
$K_{VCO} = K_O = 0.105f_o$,
$K_{div} = 1/AB = 1/ANT_R = 1/A2T_R$

B is defined as NT_R. N = 2 and T_R is the relative encoded data pattern length. For example, a 4T preamble field would correspond to T_R equals 4. When locked to the reference, T_R is equal to 2. The divide-by-A block is defined as:

A = 1 if the DIVSEL pin is LO
A = 2 if the DIVSEL pin is HI

The VCO center frequency is f_o. R_L is the HGREXT or LGREXT external resistor, depending on whether the PLL is high-gain or low-gain mode.

Substituting these values into G(s) and using the second order approximation where $C_2 << C_1$, G(s) becomes:

$$G(s) = \frac{K(s+\omega_1)}{s^2}, \quad \text{where } \omega_1 = \frac{1}{RC_1}$$

$$\text{and } K = K_{CP}K_{VCO}K_{div}R = \frac{0.124f_oR}{A2T_RR_L} \qquad \textit{(eq. 46)}$$

Looking at G(s), there are two poles at s = 0 and one zero at s = -ω1. The closed loop gain H(s) is defined as:

$$H(s) = \frac{G(s)}{1+G(s)} = \frac{K(s+\omega_1)}{s^2+Ks+K\omega_1} \qquad \textit{(eq. 47)}$$

The denominator of H(s) is called the characteristic equation. It can be compared to the standard form for second degree characteristic equation as follows:

$$s^2+Ks+K\omega_1 = s^2+2\zeta\omega_n+\omega_n^2 \qquad \textit{(eq. 48)}$$

Equating the component values gives:

$$K = 2\zeta\omega_n \text{ and } K\omega_1 = \omega_n^2 \qquad \textit{(eq. 49)}$$

where ω_n is the natural frequency of the loop and ζ is the damping factor.

Now, substituting for K and ω_1, the values for R, C_1, and C_2 can be obtained.

$$R = \frac{(2\zeta\omega_n)(A2T_RR_L)}{0.124f_o} = \frac{\omega_c(A2T_R)R_L}{0.124f_o}$$

$$C_1 = \frac{0.124f_o}{\omega_n^2A2T_RR_L} = \left[\frac{2\zeta}{\omega_c}\right]^2\frac{0.124f_{oo}}{(A2T_R)R_L}$$

$$C_2 \text{ is choosen to be between: } \frac{C_1}{10} \text{ to } \frac{C_1}{1000} \qquad \textit{(eq. 50)}$$

Component values can now be selected in accordance with specific system requirements. The following system parameters must be specified: f_o (VCO center frequency), R_L (in high or low gain mode), T_R, ω_n or ω_c and ζ in order to choose values for R, C_1 and C_2.

Since the VCO center frequency is greater than 60MHz, the DIVSEL pin should be tied low, which implies that A = 1 for the divide-by-A block.

The first step is too choose the three external resistors. They are the HGREXT and LGREXT resistors that setup the change pump current gain, and VCOREXT which sets the VCO center Frequency. They are determined as follows:

$$HGREXT = \frac{1.18V}{\text{HG Charge Pump Current}}$$

$$= \frac{1.18V}{1.0mA} = 1.18k\Omega$$

$$LGREXT = \frac{1.18V}{\text{LG Charge Pump Current}}$$

$$= \frac{1.18V}{0.3mA} = 3.9k\Omega$$

$$VCOREXT = 0.268 + \frac{223.2}{192} + \frac{7632}{192^2} = 1.6k\Omega \qquad \textit{(eq. 51)}$$

The low gain mode is used when locking to data and the high gain mode is used when locking to the reference oscillator or preamble. The component values can be chosen for either the high or low gain mode. Assume lock-to-data so, LGREXT will be used for R_L. Also, an average data pattern of 4T is assumed.

The values for R, C_1 and C_2 are calculated as follows:

$$R = \frac{\left(1000\times10^3\right)(1)(2)(4)(3900)}{0.124\left(192\times10^6\right)} = 1310\Omega$$

$$C_1 = \left(\frac{2(0.7)}{1000\times10^3}\right)^2\left(\frac{0.124\left(192\times10^6\right)}{(1)(2)(4)(3900\exists)}\right) = 1.5nF$$

$$C_2 = 0.01C_1 = 15pF \qquad \textit{(eq. 52)}$$

Now, ω_c and ζ should be recalculated to insure accuracy along with the phase margin ϕ_R.

$$\omega_c = K = \frac{0.124f_oR}{A2T_RR_L} = 999Krad/s$$

$$\zeta = \frac{1}{2} = \sqrt{RC_1\omega_c} \qquad \textit{(eq. 53)}$$

$$= \frac{1}{2}\sqrt{(1310)\left[1.5\times10^{-9}\left(999\times10^3\right)\right]} = 0.7$$

$$\phi_R \cong \tan{-1}\left(4\zeta^2\right) = \tan{-1}\left[4(0.7)^2\right] = 62.96°$$

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The values for ω_n and ζ did not change much here, but depending on what standard component values are used, they could change substantially. The phase margin should be greater than 45° for stability. In this case there is plenty of margin since $\phi_R = 63°$.

The above values are most likely not optimized for all systems using this data rate, code and preamble. The derivations are only shown as an example.

Component Selection for the Third-Order Loop

The second-order loop approximation results in loop filter component value calculations which are algebraically quite simple. This gives the user a quick way to get the loop running about where it should be. Often the second-order loop approximation works fine, particularly if $C_2 << C_1$. However, the purpose of C_2 is to filter the ripple on R and C_1 inherent to charge pump design so it is desirable to make C_2 as large as possible. The loop will then also roll off more quickly with frequency (i.e., higher Q) which may be desirable. The user who needs every ounce of performance from the PLL should really treat the loop as a true third-order loop. Unfortunately, the results are not as simple algebraically and numerical methods are often needed. Some useful approximations can still be made, however.

Note that the third-order loop requires one more parameter to be specified. That parameter is b, and is defined as, $b = 1 + (C_1/C_2)$. Standard values for capacitors are usually 1 decade apart, so b is often chosen to be 11.

From inspection of the open loop Bode diagram (Figure 4) shown earlier it can be seen that for small ω_2 values which approach w1 it is hard to achieve a good phase margin for the system. Phase margin is optimal when the crossover frequency ω_c occurs at the point where $\angle G(\omega)$ peaks. Graphically we expect this to happen when ω_c is half-way between ω_1 and ω_2. Because of the logarithmic scale used in Bode diagrams, this half-way point is the geometric mean of ω_1 and ω_2 which is,

$$\omega_c = (\omega_1\omega_2)^{1/2} \quad \text{for optimal phase margin} \qquad \textit{(eq. 54)}$$

We recall that,

$$G(s) = \frac{K\omega_1(b-1)(s+\omega_1)}{s^2(s+b\omega_1)}$$

$$\omega_2 = b\omega_1 \qquad \textit{(eq. 55)}$$

so,

$$\omega_c = \sqrt{b\omega_1^2} = \omega_1\sqrt{b} \qquad \textit{(eq. 56)}$$

In the asymptotic approximation for $\omega_1 < \omega_c < \omega_2$,

$$G(s)\frac{K\omega_1(b-1)s}{s^2 b\omega_1} = \frac{k}{s}\left(\frac{b-1}{b}\right) \qquad \textit{(eq. 57)}$$

By definition,

$$|G(j\omega_c)| = 1 = \left(\frac{k}{\omega_c}\right)\frac{b-1}{b} \Rightarrow \omega_c = \frac{K(b-1))}{b} \qquad \textit{(eq. 58)}$$

Substituting for ω_1 and K, C_1 can be found as follows,

$$\omega_1\sqrt{b} = \frac{K(b-1)}{b} \Rightarrow \omega_1 = \frac{K(b-1)}{b\sqrt{b}}$$

$$\frac{1}{RC_1} = \frac{K_V I_P R(b-1)}{Bb\sqrt{b}} \qquad \textit{(eq. 59)}$$

or,

$$C_1 = \frac{Bb\sqrt{b}}{K_V I_P R^2(b-1)} \qquad \textit{(eq. 60)}$$

Now R can be found as follows,

$$\omega_c = \frac{K(b-1)}{b} = \left[\frac{K_V I_P R}{B}\right]\left(\frac{b-1}{b}\right) \qquad \textit{(eq. 61)}$$

or,

$$R = \left[\frac{\omega_c B}{K_V I_P}\right]\frac{b}{b-1} \qquad \textit{(eq. 62)}$$

Collecting all of these results together, the filter component values C_1, C_2, and R for the optimized third-order loop can be calculated from the expressions:

$$C_1 = \left[\frac{K_V I_P}{(2\pi f_c)^2 B}\right]\frac{b-1}{\sqrt{b}} = \left[\frac{\kappa f_o I_P}{(2\pi f_c)^2 N T_R}\right]\frac{b-1}{\sqrt{b}}$$

$$C_2 = \frac{C_1}{b-1}$$

$$R = \left[\frac{2\pi f_c B}{K_V I_P}\right]\frac{b}{b-1} = \left[\frac{2\pi f_c N T_R}{\kappa f_o I_P}\right]\frac{b}{b-1} \qquad \textit{(eq. 63)}$$

This analysis only applies to a PLL with optimal phase margin. As T_R, and hence B vary, the phase margin will vary. One can optimize the phase margin for a typical data pattern, such as 3T (001) and then calculate the phase margins for other data patterns. Phase margin is defined as,

$$\begin{aligned}\phi_R &= \angle G(j\omega_c) - (-\pi)\\ G(j\omega_c) &= \frac{K\omega_1(b-1)(j\omega_c+\omega_1)}{(j\omega_c)^2(j\omega_c+b\omega_1)}\\ \angle G(j\omega_c) &= \angle(j\omega_c+\omega_1) - \angle(j\omega_c+b\omega_1) - \pi\\ \phi_R &= \tan{-1}\left(\frac{\omega_c}{\omega_1}\right) - \tan{-1}\left(\frac{\omega_c}{b\omega_1}\right)\end{aligned} \qquad \textit{(eq. 64)}$$

The crossover frequency ω_c can be found as follows:

$$|G(j\omega_c)| = 1 = \frac{K\omega_1(b-1)\left(j\omega_c^2+\omega_1^2\right)^{1/2}}{\omega_c^2\left(\omega_c^2+b^2\omega_1^2\right)^{1/2}} \qquad \textit{(eq. 65)}$$

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The equation above (eq. 65) can be transformed to:

$$\omega_c^6 + b^2\omega_1^2\omega_c^4 - K^2\omega_1^2(b-1)^2\omega_c^2 - K^2\omega_1^2(b-1)^2\omega_1^2 = 0 \qquad \textit{(eq. 66)}$$

This is a cubic polynomial in ω_c^2 which can be solved numerically given K, ω_1, and b which are all functions of K_V, I_p, B, R, C_1, and b. ω_c can then be used to calculate ϕ_R exactly. Alternatively we can use the asymptotic approximation for ω_c derived earlier

$$\omega_c \approx K\left(\frac{b-1}{b}\right) \qquad \textit{(eq. 67)}$$

$$\text{then, } \phi_R \approx \tan{-1}\left[\frac{K(b-1)}{\omega_1 b}\right] - \tan{-1}\left[\frac{K(b-1)}{\omega_1 b^2}\right] \qquad \textit{(eq. 68)}$$

For the loop with optimized phase margin we have

$$\frac{K}{\omega_1} = \frac{b\sqrt{b}}{b-1} \Rightarrow \frac{K(b-1)}{\omega_1 b} = \sqrt{b} \qquad \textit{(eq. 69)}$$

$$\text{or, } \phi_R \approx \tan{-1}(\sqrt{b}) - \tan{-1}\left(\frac{1}{\sqrt{b}}\right) \qquad \textit{(eq. 70)}$$

As an example, if b = 11, then $\phi_R = 56.4°$. This is lower than that calculated from the second-order approximation but still a reasonable value.

The damping factor ζ is no longer applicable to the third-order loop, so besides ω_c and b we need a third parameter to completely specify the loop. We could choose ϕ_R but then the values for K and ω_1 and hence R and C_1 would be embedded inside a transcendental equation. The recommended design procedure is to roughly calculate R and C_1 using the second-order approximation on an average data pattern and then calculate phase margins for all data patterns. Should any one of them drop below 45°, tweak the R and C values, recalculate ϕ_R, and iterate until adequate phase margin is achieved. An example of this procedure for the VM5711 Frequency Synthesizer used in a zone-density application is given below in the frequency synthesis section.

Third Order Example Using the VM5711 Frequency Synthesizer

We will treat the VM5711 Frequency Synthesizer with the following set of assumed specifications:

- (1,7) RLL code
- Three zones with NRZ data rates of 27 Mbits/sec, 38 Mbits/sec, and 50 Mbits/sec
- f_c = 20 kHz
- Input clock fi = 16 MHz

The VM5711 parameters can be varied by setting a DAC input by means of a serial register to a value which we will call X ($1 \le X \le 32$). According to the data sheet, we have:

I_p (μA) = 0.878 x 10^6 (5/3 - X/32) / R_{ext} (R_{ext} in Ω)

f_o (MHz) = 0.23 x 10^6 (2/3 + X/32) / R_{ext}

K_V (MHz/V) = 0.38 f_o (f_o in MHz)

Here R_{ext} is the value of an external user-selected resistor which sets the center frequency of the VCO.

Choose R_{ext}

R_{ext} must be chosen to keep the VCO centered in its range for all three zones for values of X between 1 and 32. In the VM5711 the VCO runs at three times the NRZ clock frequency, and for (1,7) code we must have:

f_o = 81 MHz (zone 1)
f_o = 114 MHz (zone 2)
f_o = 150 MHz (zone 3)

The largest available frequency ratio for the DAC is (5/3 - 0)/(5/3 - 31/32) = 2.39, while the largest frequency ratio required for the zones is 150/81 = 1.85. If the DAC is centered over the VCO range, then

$$0.2310^6(2/3 + 16/32)/R_{ext} = (105 + 81)/2 \qquad \textit{(eq. 71)}$$

from which it follows that R_{ext} = 2.32 kΩ.

Determine the DAC setting X for each zone

$$X = 32\left\{\left[\frac{f_o R_{EXT}}{0.23 \times 10^6}\right] - \left(\frac{2}{3}\right)\right\} \qquad \textit{(eq. 72)}$$

thus, X = 5 (zone 1)
X = 15 (zone 2)
X = 27 (zone 3)

Determine divider settings M and N for each zone.[7]

M and N must be chosen for each zone such that $f_o = (2M/N)fi$. The factor 2 is needed because (1,7) code is being used. The CDSEL input the VM5710 must be set HIGH, So:

81 = (2M1/N1)(16 MHz)
114 = (2M2/N2)(16 MHz)
150 = (2M3/N3)(16 MHz)

There are a variety of solutions which will work, but because the VM5711 has a charge pump current which scales inversely with X and a VCO gain which scales linearly with X, the result is a loop gain which scales with M since,

$$K = \frac{K_V I_P R}{B} = \frac{K_V I_P R}{2M} \qquad \textit{(eq. 73)}$$

Thus, we will want to fix B (M) for all zones. (Not all synthesizers have a charge pump current which scales with zone, so keeping M fixed with zone is not valid in general). Simplifying the equations, we have,

M1 = (81/32) N1 = 2.53 N1
M2 = (114/32) N2 = 3.56 N2
M3 = (150/32) N3 = 4.69 N3

[7] Here we use M and N in place of the A and B of the earlier text to conform to the VM5711 data sheet.

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For the VM5711, M can range from 1 to 256 while N goes from 1 to 32. The following M and N values will work to synthesize exactly the data rates specified:

M1 = 81; N1 = 32
M2 = 57; N2 = 16
M3 = 75; N3 = 16

M is not fixed as desired. This will cause a shift in ω_c, which will probably not be a big problem. The alternative is to tweak the data rates to something which will allow a fixed M. In general the user will have to make these tradeoffs. A perfect solution may not always be possible for every design.

Calculate R, C_1, and C_2.

These values are the same for all zones, so some compromises may have to be made. Using the second-order approximation,

$$R = \frac{2\pi f_c B}{K_V I_P} = \frac{4\pi f_c M}{K_V I_P} \qquad C_1 = \frac{2\zeta^2}{\pi f_c R} \qquad \textit{(eq. 74)}$$

Substituting for K_V, I_p, B, and R_{ext} we find

$$R = \frac{[2\pi (2320) f_c 2M]}{\left[(0.38)\left(0.878 \times 10^6\right)(5/3) - (x/32) f_o\right]} = \left[\frac{2.79}{(53.3 - X)}\right]\left(\frac{Mf_c}{f_o}\right) \qquad \textit{(eq. 75)}$$

Putting in the zone-dependent values X, M, and f_o we find

R = 2.79 (81) f_c / (53.3 - 5) (81) = 0.058 f_c (zone 1)
R = 2.79 (57) f_c / (53.3 - 15) (114) = 0.036 f_c (zone 2)
R = 2.79 (75) f_c / (53.3 - 27) (150) = 0.053 f_c (zone 3)

Zone 2 will have the highest f_c for the same R. Usually the specified bandwidth f_c is the highest bandwidth desired, so if zone 2 is used to calculate R we have,

$$R = 0.036\ (20\ kHz) = 720\Omega \qquad \textit{(eq. 76)}$$

Rounding to the closest standard value we get **R = 750Ω.** Recalling the open-loop Bode plot, w1 is fixed by R and C_1 and hence the zone with the lowest f_c will have the lowest ζ and hence the smallest ϕ_R. So zone 1 is used to calculate C_1.

$$C_1 = \frac{2\zeta^2}{\pi f_c R}, \quad \text{where} \quad f_c = \frac{R}{0.058} \qquad \textit{(eq. 77)}$$

If we let $\zeta = 0.7$ then,

$$C_1 = \frac{2\,(0.7)^2\,(0.058)}{750^2\pi} = 0.032\mu F \qquad \textit{(eq. 78)}$$

Again picking a standard value we find $C_1 = 0.033\ \mu F$. C_2 is found assuming b = 11 and is $C_2 = 0.0033\ \mu F$. We now calculate the phase margin ϕ_R and bandwidth f_c for each zone using,

$$f_c = \left(\frac{K}{2\pi}\right)\left(\frac{b-1}{b}\right)$$

$$\phi_R = \tan^{-1}\left[\frac{K(b-1)}{\omega_1 b}\right] - \tan^{-1}\left[\frac{K(b-1)}{\omega_1 b^2}\right] \qquad \textit{(eq. 79)}$$

which were derived using the third-order asymptotic model. For convenience all pertinent equations are shown below along with a tabulation of loop parameters for each zone:

$K = K_V I_p R/B$ $\quad B = 2M$ $\quad K_V = 0.38\ f_o$
$\omega_1 = 1/RC_1$ $\quad b = 1 + (C_1/C_2)$ $\quad \zeta = (1/2)[K/\omega_1]^{1/2}$
$R = 750\Omega$ $\quad C_1 = 0.033\mu F$ $\quad C_2 = 0.0033\mu F$
$R_{ext} = 2.32k\Omega$ $\quad I_p = 0.878 \times 10^6\ (5/3 - X/32) / R_{ext}\ (\mu A)$

Parameter	*Zone 1*	*Zone 2*	*Zone 3*
NRZ Data Rate (Mb/s)	27	38	50
f_o (MHz)	81	114	150
X (DAC setting)	5	15	27
N	32	16	16
M	81	57	75
K_V (MHz/V)	30.8	3.3	57
I_p (μA)	562	453	311
f_c (kHz)	11.8	18.7	12.8
ζ	0.71	0.89	0.74
DVPO (mV)	0.83	0.82	0.47
ϕ_R	51.9°	56.2°	53.1°

A chart like this can be generated for any zone-density drive design. It may be convenient to use a spread sheet program. We can see from the results above that the loop has adequate phase margin and a loop bandwidth within specifications for each zone.

Application Considerations for Clock Recovery (Data Separation)

(a) The Use of Codes. As noted above, the coding scheme for data written on a disk must ensure that there is at least some minimum number of transitions (flux reversals) per unit time. Without readout peaks the data separator soon loses track of the correct phase of the read clock and will give erroneous results when it hits data again.

The most common code in use today is the (1,7) code. There are several versions, all of which obey the rules given below:

- Two input (NRZ) bits are encoded as 3 output bits.
- Each 1 bit is isolated (cannot be followed by a 1)
- The strings of 0 bits between 1 bits can be 1 to 7 bits long.

Such codes are often referred to as RLL (Run-Length Limited) codes since the no-more-than-7-zeroes constraint imposes a limit on the length of runs of same-type symbols.

From the viewpoint of PLL operation, the data in an RLL input stream differs fundamentally from the square-wave input of a frequency synthesizer. The positions of 1 and 0 symbols are random and the data contains many different frequencies. So, steps must be taken in design to insure that phase comparisons are made only where a transition (edge) occurs in the data.

(b) Data Separator Block Diagram. Data separator PLLs take the general form described above, but have some additional features. Figure 5 shows a generic data separator PLL. The basic PLL is at the upper right. The RD_GATE signal is used to control switches S1 and S2. During write operations the read PLL is on standby and gets its input from the reference clock (S1 in lower position and S2 in the upper position). This keeps the PLL locked at about the right frequency so that it can rapidly switch to reading upon command (i.e., without a long settling transient). In read mode, the data flipflop gets its data from the undelayed read signal and its clock from the delayed[8] read signal, which has the effect of suppressing phase comparisons when there is no edge. This corresponds to S1 in the upper position and S2 in the lower position.

During seeks, etc. there are times when the data separator PLL is idle but one would like to keep the same frequency so as to be able to lock again rapidly. This is done using the coast mode or hold mode controlled by switch S5. In the down position shown the PLL operates normally. In the up position (the coast mode) the loop filter capacitors are isolated and hold the VCO frequency as a stored charge. There is a certain slow bleed-off of charge due to base currents and low-level leakages which leads to droop in the frequency and limits the length of time over which the VCO remembers its frequency.

(c) Lock Acquisition; Preambles; Zero-Phase Restart. The data separator reacquires the read clock at the beginning of each sector. The sector header information contains a region of constant-frequency data (such as repeating 100 symbols) during which the PLL acquires the clock. This is called the preamble. Often the charge pump current I_p is temporarily increased during the preamble to promote faster lock (wider loop bandwidth).

Because the data separator PLL has been locked to the reference clock when idle it is at about the right frequency when it hits the preamble. However, it may begin the lockup transient with a substantial phase error. In order to promote rapid clock acquisition, a zero-phase restart signal is generated within the chip. When RD_GATE is asserted the restart control logic looks for edges in the preamble data. It then issues a zero-phase restart command to the VCO which momentarily freezes it in a 1 or 0 state and then releases it with a definite phase (usually nominally zero) simultaneously with a data edge. This greatly aids in fast clock acquisition.

(d) The Read Window; Window Margin; Marginalization. The data separator PLL is set up so as to align the rising edges of the recovered read clock with the rising edges of the data coming

[8] The data is delayed by T/3 relative to the NRZ period or T/2 relative to the coded data period for optimal window centereing of the PLL

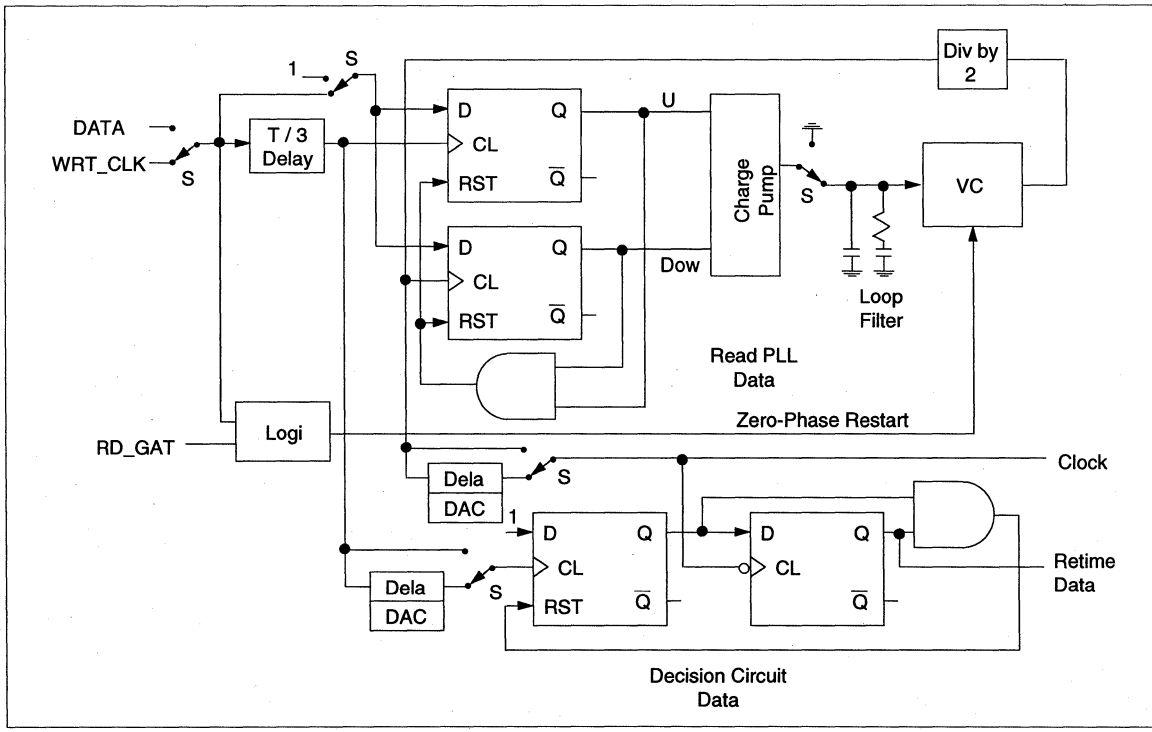


Figure 6: A typical clock recovery PLL (data separator or read PLL

from the pulse detector. Ideally, the decision circuit at the bottom of Figure 5 will work correctly if the data edge is anywhere within the read window shown in Figure 6a (the ideal case). It is possible to get a noncentered window as shown in Figure 6b in the pulse detector circuitry for a number of reasons — finite propagation delay in the decision circuit logic, imbalance in internal signal lines, offsets and other problems (e.g. pulse pairing, mismatch of the UP and DN currents in the charge pump). The amount of early or late mistiming of the data edges which can be tolerated without an error is referred to as the window margin.

Another important problem is jitter, as shown in Figure 6c. This picture is what would be seen if one looked at the data separator output while triggering on the recovered clock. This jitter arises from a number of causes, noise in the read signal, noise in the VCO and loop filter, etc. If there is too much jitter for an acceptable BER (Bit Error Rate), changes may need to be made in bits/inch or preamp and head components.

The window centering error shown in Figure 6b can be compensated for by what is called marginalization. In normal PLL operation, switches S3 and S4 are in the up position, so that the decision circuit operates directly on the clock and data. When the marginalization is turned on two DAC-controlled delays are inserted before the decision circuit, with the DAC values being set by on-chip serial register bits. This allows the user to skew the timing deliberately either way. As a diagnostic tool, this allows the drive designer to determine the earliest and latest edges which lead to a given error rate, thus allowing window centering to be determined. The marginalization feature can also be used in an adaptive scheme in which a calibration procedure is done for each head. In this way, the optimum marginalization delay can be individually set for each head.

Application Considerations for Frequency Synthesis

In this section we will describe some important aspects of frequency synthesizer operation and give a complete detailed example of a multi-zone setup for the VM5711.

(a) Frequency Divider Ratios. Typically a frequency synthesizer operates continuously, but during a seek operation between zones it must settle to a new frequency. The settling time should be kept less than a typical minimum seek time, often a few msec. This might seem like plenty of time, but in reality there are a couple of factors which slow things down. In the first place, drive designers may wish to have fine frequency resolution. This calls for large divider ratios, and with large divider ratios waveform edges only occur infrequently at the phase detector. Phase comparison only occurs at edges, so in effect the sampling rate becomes quite low. This leads in turn to low ω_n, and slow response (which calls for a large C_1).

Consider a case where we are synthesizing an output frequency of 21.37 MHz (T = 46.8 nsec), with the B divider (Figure 1) set at 211. Then we only sample the phase every 46.8 x 211 = 9875 nsec. If it requires 50 sampling periods to achieve adequate settling then the transient conditions will last for 50 x 9875 = 0.49 msec. Smaller divider ratios will reduce this transient recovery time.

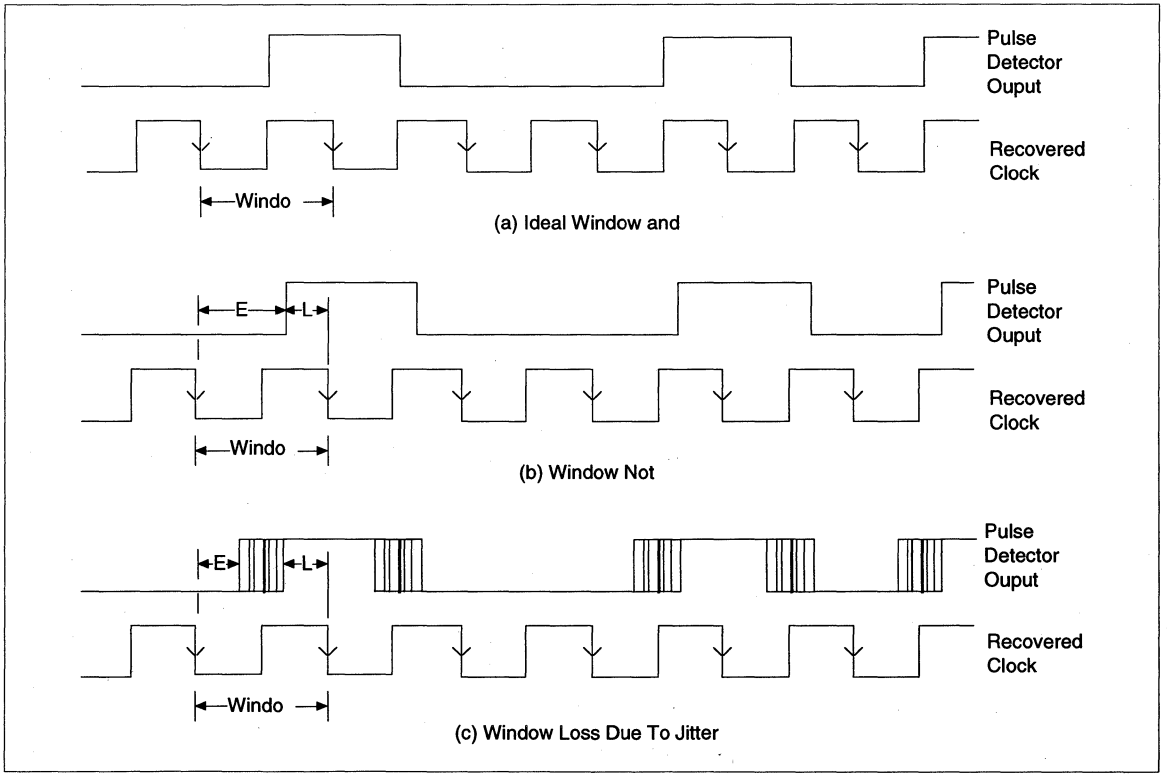


Figure 7: A typical clock recovery PLL (data separator or read PLL

(b) Phase Jitter, Pull-Out Problems; Cycle Slips. For frequency synthesizers a very low RMS jitter is usually called for. The overall read/write error budget is better if the write jitter can be made negligible. The noise bandwidth BL scales as wn. Minimum in-band noise and, thus, minimum phase jitter is achieved by making wn as small as possible. There would seem to be no real limit to this, leading one to the idea of 20 μF filter capacitors, etc. Bigger is always better. But is it?

In fact, if too-large filter capacitors are used ***even a rather small disturbance can lead to loss of lock and a cycle slip.*** This basically relates to the nonlinear behavior of the circuit and cannot be treated exactly. Best [3] gives us the following equation:

$$\Delta\omega_{PO} = 1.8\omega_n(\zeta + 1) = \frac{1.8\omega_c(\zeta + 1)}{2\zeta} \qquad \textit{(eq. 80)}$$

Here $\Delta\omega_{PO}$ is the largest frequency step which can be tolerated by the PLL without loss of lock (the so-called pull-out condition). How could such a frequency step arise? Suppose that some electrical event causes the VCO input voltage to change. Since large filter capacitors are needed for frequency synthesizers they are invariably off-chip, and nearby clocks, logic signals, switching power supply glitches etc. can be picked up by the filter components. ***A voltage step at the VCO input is a frequency step to the PLL***, and it will go into a transient condition when one occurs. Suppose that:

ω_n = 5.103 rad/sec (about 1 kHz)
ζ = .7 (near-optimum)
K_{VCO} = 15.106 rad/V-sec (1 V shifts f_o by 2.4 MHz)

Then $\Delta\omega_{PO}$ = 15,300 rad/sec. The VCO input voltage shift $\Delta\varsigma PO$ corresponding to this is:

$$\Delta\omega_{PO} = \frac{\Delta\omega_{PO}}{K_{VCO}} = \frac{1.8\omega_n(\zeta + 1)}{K_{VCO}}$$
$$= 1.8\omega_c\left(\frac{\zeta + 1}{2\zeta}\right)\left(\frac{1}{K_{VCO}}\right) = 1.02 \times 10^{-3}\text{V} \qquad \textit{(eq. 81)}$$

In other words, ***a 1 mV disturbance on the filter capacitors will cause loss of lock under these conditions!*** It is probably not practical to design a board which keeps pickup pulses below 1 mV, and thus the pull-out condition imposes a practical upper limit on the sizes of filter capacitors.

This pull-out instability (loss of lock) and the resulting cycle slips show up in drives as an intermittent failure of the write clock and appears to be problem both in theory and in practice.

We also note that there is a certain irreducible jitter (phase noise) in the VCO itself, and the use of very narrow loop bandwidths does not defeat this. The currents and voltages within the VCO are subject to thermal and shot noise, and this in effect makes small random changes in the switching thresholds for regeneration from cycle to cycle. This phenomenon has been described in a closely related type of oscillator in [7].

REFERENCES

[1] Floyd M. Gardner, Charge-Pump Phase-Locked Loops, IEEE Transactions on Communications, COM-28, No. 11, pp. 1849-1858, November (1980). A detailed analysis of the type of PLL commonly used in disk drives.

[2] Floyd M. Gardner, Phaselock Techniques, 2nd Ed., Wiley, NY (1979). A standard reference in the field.

[3] Roland E. Best, Phase-Locked Loops. Theory, Design, and Applications, McGraw-Hill, NY (1984). Probably the best general reference for the newcomer.

[4] Heinrich Meyr and Gerd Ascheid, Synchronization in Digital Communications, Vol. 1, Wiley, NY (1990). An excellent recent book; more theoretical than the others.

[5] Phase-Locked Loops, ed. by William Lindsey and Chak Chie, IEEE Press (1986). A collection of technical article reprints, including [1].

[6] Analysis and Design of Analog Integrated Circuits, P. R. Gray and R. G. Meyer, Wiley (1977). A widely-used text on analog IC design; Ch. 10 deals with phase-locked loops. More hardware detail than other books.

[7] A. A. Abidi and R. G. Meyer, Noise in Relaxation Oscillators, IEEE J. Solid-State Circuits, SC-18, 794-802, December (1983).

VTC Inc.
Value the Customer™

AUTOMATIC GAIN CONTROL TECHNIQUE FOR HARD DISK DRIVES

August, 1994

INTRODUCTION

Several VTC ICs provide automatic gain control for the READ signal from a rigid disk drive. The method used has a number of features that optimize it for this application. The system has two thresholds for the signal amplitude, V+ and V-. When the output voltage V_S of the AGC amplifier satisfies $V_S > V+$ the gain is steadily reduced until $V_S = V+$ at which point the gain stabilizes (this is called a release transient). When V_S satisfies $V_S < V+$ and $V_S > V-$ the gain is steadily increased until $V_S = V+$ at which point the gain stabilizes (this is called an attack transient). When V_S satisfies $V_S < V-$ the gain is in a "hold" mode and changes only very slowly (due to device leakage currents). The latter feature is useful during periods of low or noisy signal when the gain would otherwise be driven to its maximum value resulting in a long recovery time when a normal signal level is restored.

AGC OUTPUT SAMPLING CIRCUIT

An AGC loop must sample the output and generate a suitable amplitude-control voltage which is fed back to the variable gain stage(s). The arrangement for sampling the AGC output amplitude is shown schematically in Figure 1. The signals V_S+ and V_S- (shown as solid and dashed lines) are the complementary outputs of the AGC amplifier. They are fed to four emitter followers, two of which have their emitters tied together to form a full-wave rectifier. Offset resistors R_L and R_H create two level-shifted replicas of the rectified signal. A set of comparators (1-4) generates level crossings which are then ORed in pairs and fed to an ***edge-triggered*** RS flipflop. The flip-flop outputs are then used to control two switchable nominally equal-valued current sources (CSUP and CSDN) which are connected to a capacitor C in a charge-pump arrangement. The capacitor voltage is then fed back (through a suitable buffer) to the amplitude control input of the AGC stage(s).

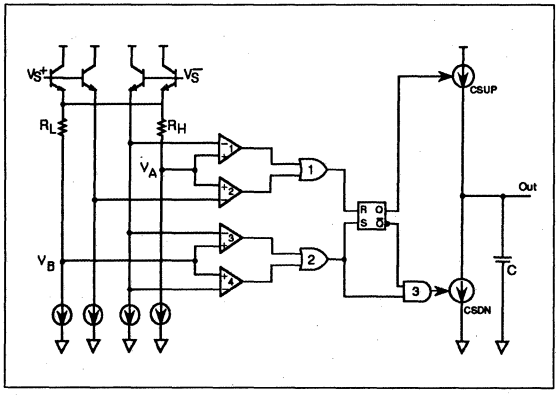


Figure 1: Output sampling and charge pump scheme for the AGC loop.

The charge pump provides loop filtering for the AGC loop, and the value of C governs the response time of the AGC loop.

Figure 2 shows ideal circuit waveforms when the output amplitude is too high. Note that the duty cycle for the PUMP UP and PUMP DOWN waveforms is such that the PUMP DOWN current source is on for a much longer time than the PUMP UP source, so that the output amplitude will steadily ramp down under these conditions. Figure 3 shows the waveforms when the output amplitude is very close to the intended value. Now the PUMP UP and PUMP DOWN duty cycles are nearly identical and the output amplitude will stabilize. Note that when the data pattern contains a missing pulse both current sources are off, so that the AGC feedback is unaffected, i.e., the amplitude detection scheme senses only peaks (it "coasts" over missing pulses). The waveforms when V_S lies between V- and V+ are shown in Figure 4. Here the outputs of comparators C1 and C2 are

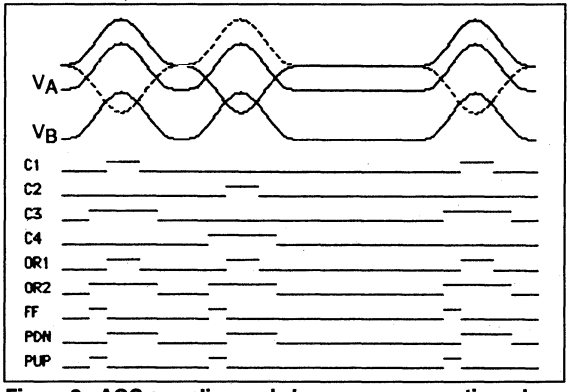


Figure 2: AGC sampling and charge pump operation when V_S substantially exceeds V+.

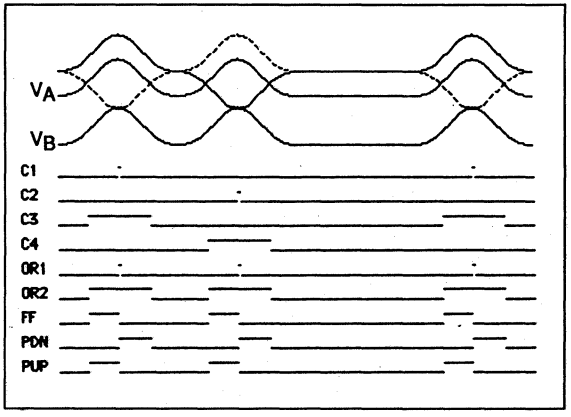


Figure 3: AGC sampling and charge pump operation when V_S exceeds V+ by only a small amount.

APPLICATION NOTES

always LOW, and the first rising edge on the C3 or C4 output will set the RS flipflop into a state where the PUMP UP current is on at all times, leading to a steady increase in the voltage gain and output amplitude until C1 and C2 begin to change state.

Figure 5 shows the waveforms when V_S is less than V-. Here none of the comparator outputs ever goes high, and both current sources remain off. This puts the AGC loop into a "hold" condition, similar to that which occurs during a missing pulse. The behavior of the gain under these conditions depends on the leakage currents present in the chip and on the board, and the resulting behavior is usually a slow rise in the AGC gain (i.e., leakage sources predominate over leakage sinks).

THE IMPEDANCE SWITCH

The READ signal normally comes into the pulse detector chip as a capacitively-coupled differential signal. While this is convenient for avoiding offsets, etc., the relatively high impedance presented at the AGC amplifier input means that when there is a sudden change of input amplitude or waveform the recovery will be slow and the AG loop will take a long time to stabilize unless special measures are taken. In many of its AGC amplifiers VTC provides a ***fast acquisition*** mode to facilitate rapid stabilization of the AGC loop. It is controlled by an external logic signal (normally labeled FAQ) which, when asserted causes the input impedance to be lower by several-fold than its normal value.

A fast acquisition operation begins with a high-to-low transition of FAQ, which lowers the input impedance and reduces the output signal to zero. The output signal will remain at zero as long as FAQ is held low. Upon a low-to-high transition of FAQ the input impedance is rapidly restored to its normal value and a PUMP UP current source with a magnitude many times larger than the normal ***slow-tracking*** value switches on and rapidly brings the output amplitude within the control range. When the output amplitude reaches its nominal value the large PUMP UP current source is automatically turned off by circuits within the chip.

ADJUSTING THE AGC PARAMETERS

Most of the AGC parameters, such as minimum and maximum gain, attack and release time, AGC loop response time constant, etc. can be adjusted by suitable choice of off-chip discrete resistors and capacitors. The details differ for various chips, and are covered in the corresponding data sheets.

The convention for the control action is when a logical high is generated the current is ON and with a logical low it is OFF.

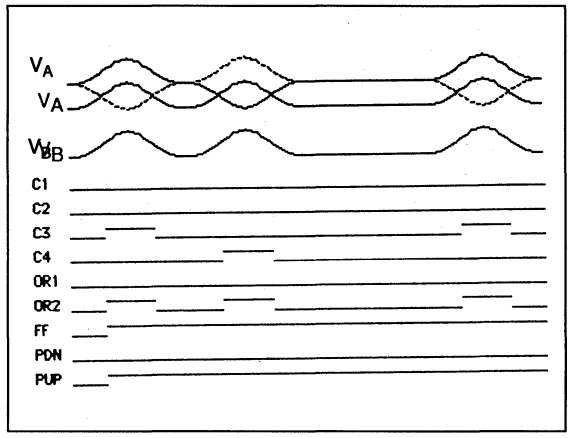


Figure 4: AGC sampling and charge pump operation when V_S lies between V- and V+.

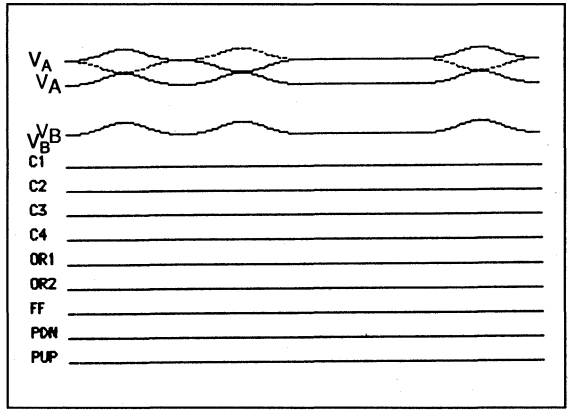
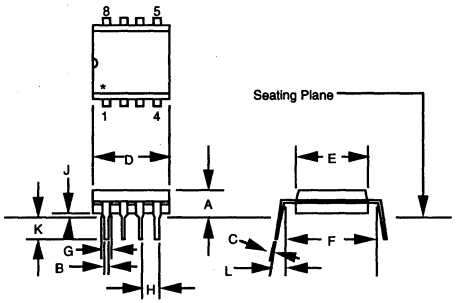


Figure 5: AGC sampling and charge pump operation when V_S is less than V-.

8 Packaging and Ordering

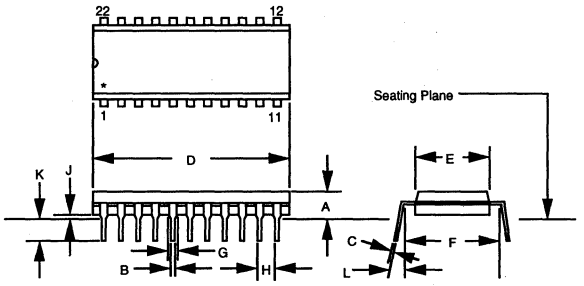
Plastic DIP (PDIP)

8-Lead PDIP (300 mil)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.170	—	4.32
B	0.016	0.020	0.41	0.51
C	0.008	0.012	0.20	0.30
D	0.360	0.370	9.14	9.40
E	0.240	0.260	6.10	6.60
F	0.300	0.325	7.62	8.26
G	0.055	0.065	1.40	1.65
H	0.100	BSC	2.54	BSC
J	0.015	—	0.38	—
K	0.125	0.135	3.18	3.43
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.
Note: Measurement "A" is to the pin standoffs.

22-Lead PDIP (300 mil)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	—	0.170	—	3.30
B	0.016	0.020	0.41	0.51
C	0.008	0.012	0.20	0.30
D	1.025	1.035	26.04	26.29
E	0.240	0.260	6.10	6.60
F	0.300	0.325	7.62	8.26
G	0.055	0.065	1.40	1.65
H	0.100	BSC	2.54	BSC
J	0.015	—	0.38	—
K	0.125	0.135	3.18	3.43
L	0°	15°	0°	15°

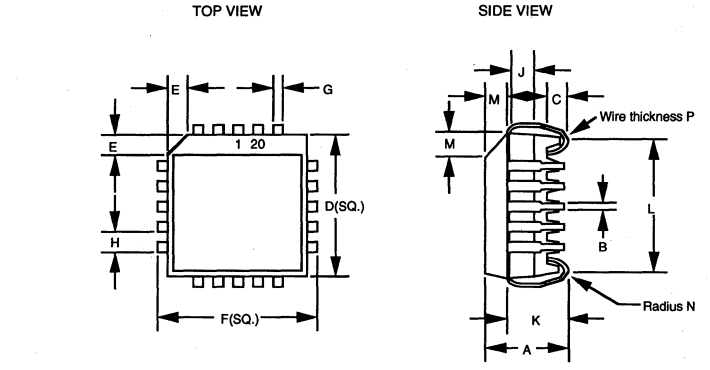


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.
Note: Measurement "A" is to the pin standoffs.

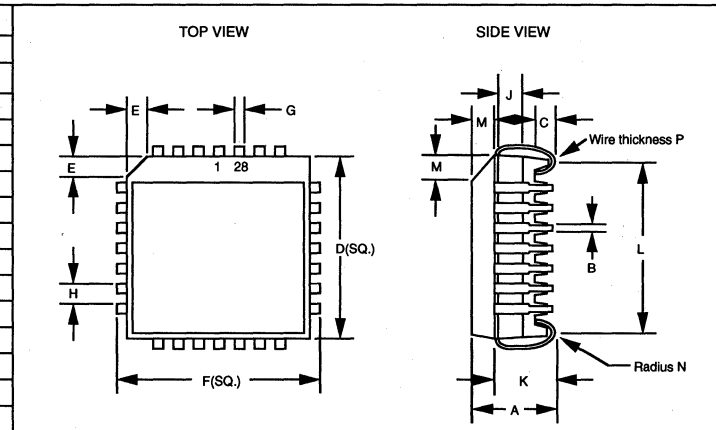
PACKAGING AND ORDERING

Plastic Leaded Chip Carrier (PLCC)

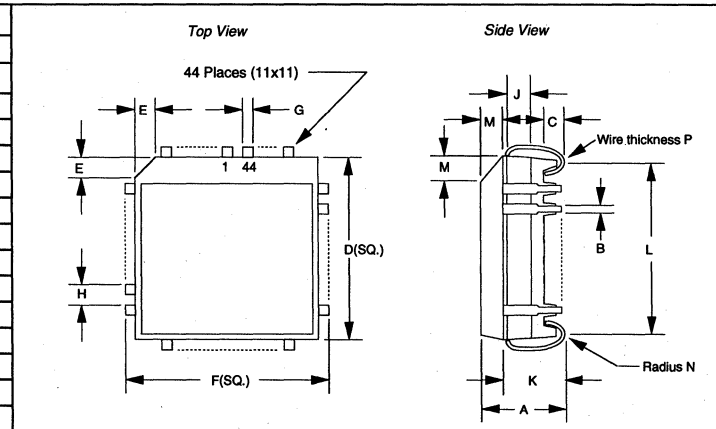
20-Lead Plastic Leaded Chip Carrier (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.165	0.180	4.20	4.57
B	0.013	0.021	0.33	0.53
C	0.025	——	0.63	——
D	0.350	0.354	8.89	8.99
E	0.042	0.048	1.07	1.22
F	0.385	0.395	9.78	10.03
G	0.026	0.032	0.66	0.81
H	0.050	BSC	1.27	BSC
J	0.060	0.070	1.52	1.78
K	0.100	0.110	2.54	2.79
L	0.290	0.330	7.37	8.38
M	0.042	0.056	1.07	1.42
N	0.025	0.045	0.64	1.14
P	0.004	0.012	0.10	0.30



28-Lead Plastic Leaded Chip Carrier (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
B	0.013	0.021	0.33	0.53
C	0.025	——	0.63	——
D	0.450	0.454	11.43	11.53
E	0.042	0.048	1.066	1.22
F	0.485	0.495	12.32	12.57
G	0.026	0.032	0.66	0.81
H	0.050	BSC	1.27	BSC
J	0.060	0.070	1.52	1.78
K	0.100	0.110	2.54	2.79
L	0.390	0.430	9.91	10.93
M	0.042	0.056	1.07	1.42
N	0.025	0.045	0.64	1.14
P	0.004	0.012	0.10	0.30

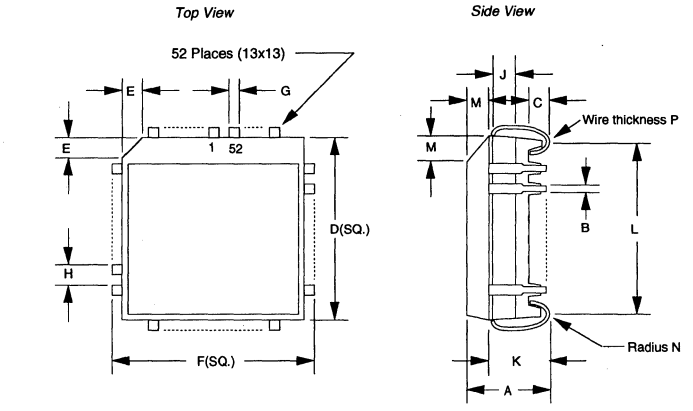


44-Lead Plastic Leaded Chip Carrier (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.191	4.572
B	0.013	0.021	0.330	0.533
C	0.025	——	0.635	——
D	0.650	0.654	16.51	16.61
E	0.042	0.048	1.06	1.22
F	0.685	0.695	17.40	17.65
G	0.026	0.032	0.660	0.813
H	0.050	BSC	1.27	BSC
J	0.060	——	1.52	——
K	0.100	0.110	2.54	2.79
L	0.590	0.630	14.98	16.00
M	0.042	0.056	1.066	1.42
N	0.020	0.040	0.508	1.015
P	0.004	0.012	0.102	0.304



PACKAGING AND ORDERING

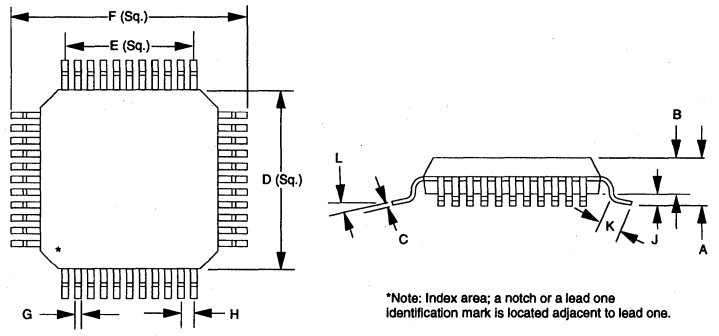
52-Lead Plastic Leaded Chip Carrier (PLCC)				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.191	4.572
B	0.013	0.021	0.330	0.533
C	0.025	—	0.635	—
D	0.750	0.754	19.05	19.15
E	0.042	0.048	1.07	1.22
F	0.785	0.795	19.93	20.20
G	0.026	0.032	0.660	0.813
H	0.050	BSC	1.27	BSC
J	0.060	—	1.52	—
K	0.100	0.110	2.54	2.79
L	0.690	0.730	17.52	18.54
M	0.042	0.056	1.07	1.42
N	0.020	0.040	0.508	1.01
P	0.004	0.012	0.101	0.304



Plastic Quad Flatpack (PQFP)

44-Lead PQFP (2.0mm thick body, 1.60mm leadform)

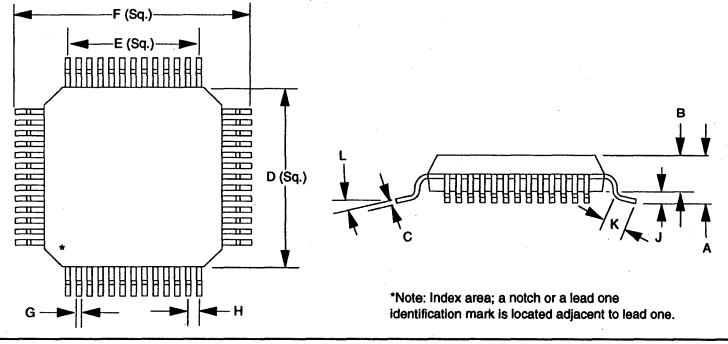
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.084 nom	0.096	2.13 nom	2.45
B	0.077	0.083	1.95	2.10
C	0.0051	0.008	0.13	0.203
D	0.390	0.398	9.90	10.10
E	0.315	REF	8.00	REF
F	0.510	0.530	12.95	13.45
G	0.012	0.018	0.30	0.45
H	0.0315	BSC	0.80	BSC
J	0.000	0.005 nom	0.00	0.13 nom
K	0.024	0.037	0.60	0.95
L	0°	7°	0°	7°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

52-Lead PQFP (10.0 x 10.0 x 2.0mm, 1.60mm leadform)

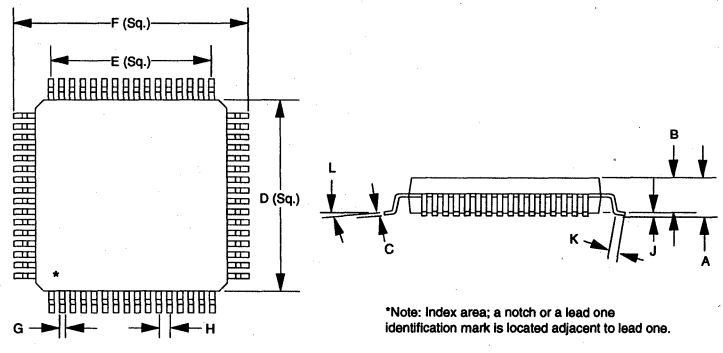
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.085 nom	0.093	2.15 nom	2.35
B	0.077	0.083	1.95	2.10
C	0.005	0.009	0.13	0.23
D	0.390	0.398	9.90	10.10
E	0.307	REF	7.80	REF
F	0.510	0.530	12.95	13.45
G	0.009	0.015	0.22	0.38
H	0.0256	BSC	0.65	BSC
J	0.004	0.010	0.10	0.25
K	0.026	0.037	0.65	0.95
L	0°	7°	0°	7°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

64-LEAD PQ14 (14.0 x 14.0 x 2.67mm, 1.60mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.111 nom	.118	2.82 nom	3.00
B	.100	.108	2.55	2.75
C	.005	.009	0.13	0.23
D	.549	.553	13.95	14.05
E	.472	REF	12.00	REF
F	.667	.687	16.95	17.45
G	.012	.018	0.30	0.45
H	.0315	BSC	0.80	BSC
J	.004	.010	0.10	0.25
K	.026	.037	0.65	0.95
L	0°	7°	0°	7°



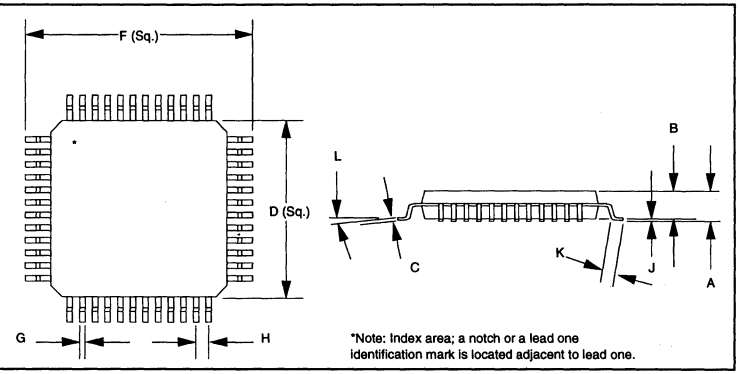
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

PACKAGING AND ORDERING

Thin Quad Flatpack (TQFP)

48-Lead TQFP (7.0 x 7.0 x 1.0mm, 1.00mm leadform)

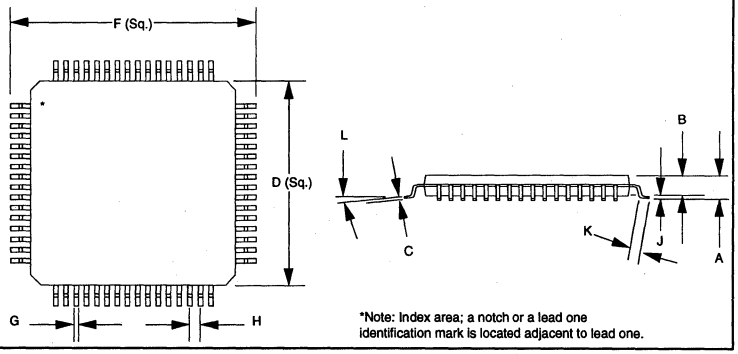
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	.050	–	1.27
B	.037	.044	0.95	1.12
C	.004	.007	0.09	0.18
D	.275	BSC	7.00	BSC
F	.354	BSC	9.00	BSC
G	.005	.012	0.14	0.30
H	.0197	BSC	0.50	BSC
J	.002	.006	0.05	0.15
K	.018	.030	0.45	0.75
L	0°	7°	0°	7°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

64-Lead TQFP (10.0 x 10.0 x 1.0mm, 1.00mm leadform)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	.050	–	1.27
B	.037	.044	0.95	1.12
C	.004	.007	0.09	0.18
D	.394	BSC	10.00	BSC
F	.472	BSC	12.00	BSC
G	.005	.012	0.14	0.30
H	.0197	BSC	0.50	BSC
J	.002	.006	0.05	0.15
K	.018	.030	0.45	0.75
L	0°	7°	0°	7°

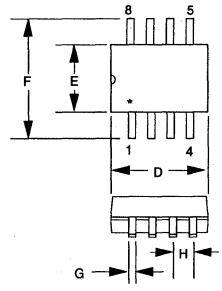


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

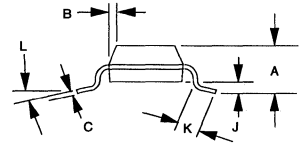
Small Outline Integrated Circuit (SOIC)

8-Lead SOIC (150 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
B	0.010	0.016	0.25	0.41
C	0.008	0.010	0.19	0.25
D	0.189	0.196	4.80	4.98
E	0.150	0.157	3.81	3.99
F	0.230	0.244	5.84	6.20
G	0.014	0.020	0.35	0.49
H	0.050	BSC	1.27	BSC
J	0.004	0.010	0.10	0.25
K	0.016	0.035	0.41	0.89
L	0°	8°	0°	8°

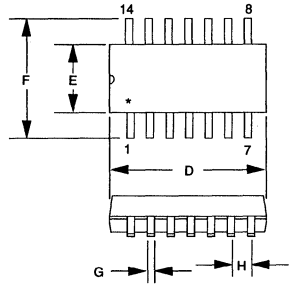


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

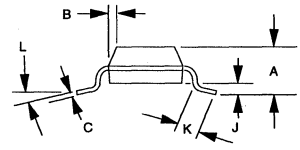


14-Lead Narrow SOIC (150 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
B	0.010	0.016	0.25	0.41
C	0.008	0.010	0.19	0.25
D	0.337	0.344	8.58	8.74
E	0.150	0.157	3.81	3.99
F	0.230	0.244	5.84	6.20
G	0.014	0.020	0.35	0.49
H	0.050	BSC	1.27	BSC
J	0.004	0.010	0.10	0.25
K	0.016	0.035	0.41	0.89
L	0°	8°	0°	8°

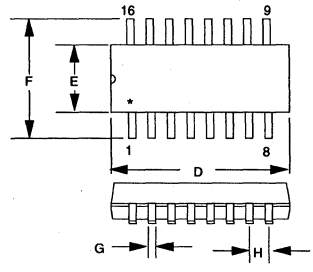


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

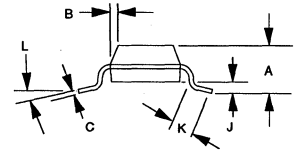


16-Lead SOIC NARROW (150 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
B	0.010	0.016	0.25	0.41
C	0.008	0.010	0.19	0.25
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
F	0.230	0.244	5.84	6.20
G	0.014	0.020	0.35	0.49
H	0.050	BSC	1.27	BSC
J	0.004	0.010	0.10	0.25
K	0.016	0.035	0.41	0.89
L	0°	8°	0°	8°



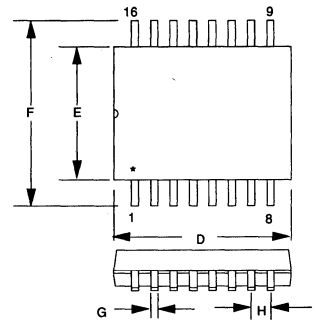
*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



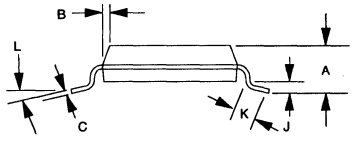
PACKAGING AND ORDERING

16-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.402	0.412	10.21	10.46
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050	BSC	1.27	BSC
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0°	8°	0°	8°

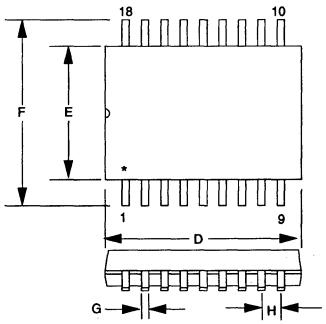


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

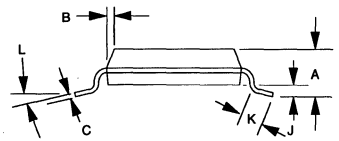


18-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.451	0.461	11.46	11.71
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050	(BSC)	1.27	(BSC)
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0°	8°	0°	8°

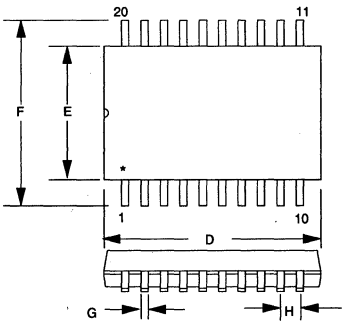


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

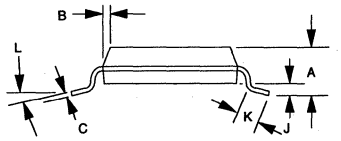


20-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050	BSC	1.27	BSC
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0°	8°	0°	8°

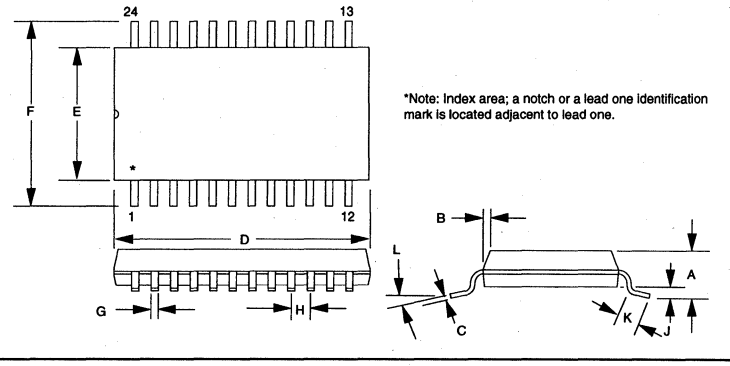


*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



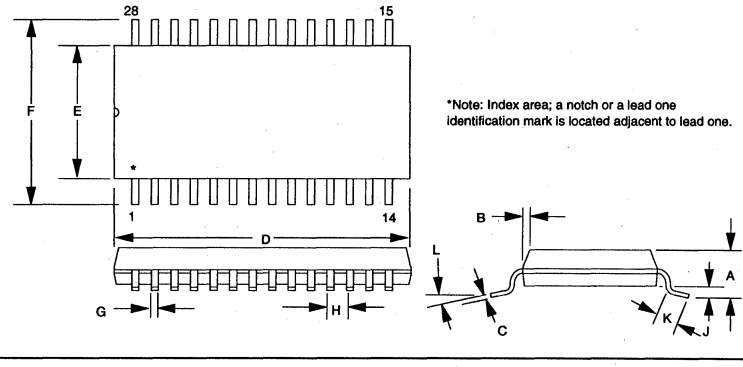
24-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050	BSC	1.27	BSC
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0 °	8 °	0 °	8 °



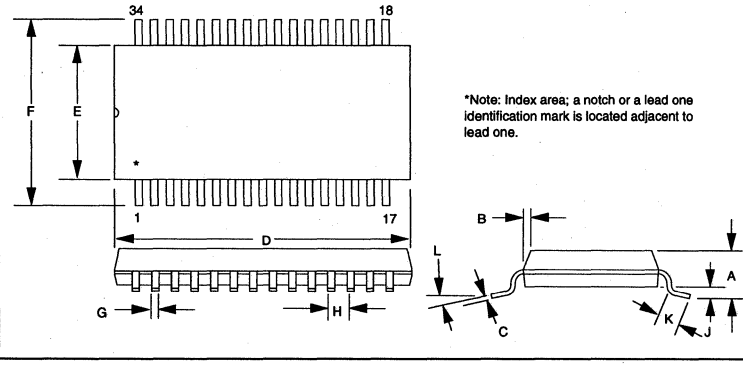
28-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.32
D	0.701	0.711	17.81	18.06
E	0.291	0.300	7.40	7.60
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.050	BSC	1.27	BSC
J	0.005	0.012	0.13	0.29
K	0.024	0.040	0.61	1.02
L	0 °	8 °	0 °	8 °



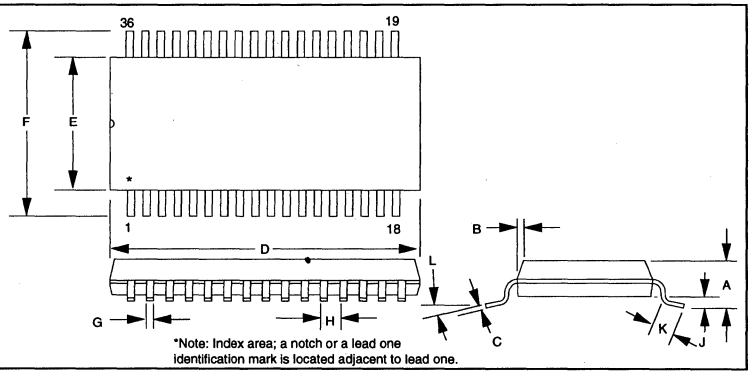
34-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.097	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.0091	0.0125	0.23	0.32
D	0.701	0.711	17.81	18.06
E	0.292	0.299	7.42	7.59
F	0.400	0.410	10.16	10.41
G	0.014	0.019	0.35	0.48
H	0.040	BSC	1.016	BSC
J	0.005	0.0115	0.127	0.29
K	0.024	0.040	0.61	1.02
L	0°	8°	0°	8°



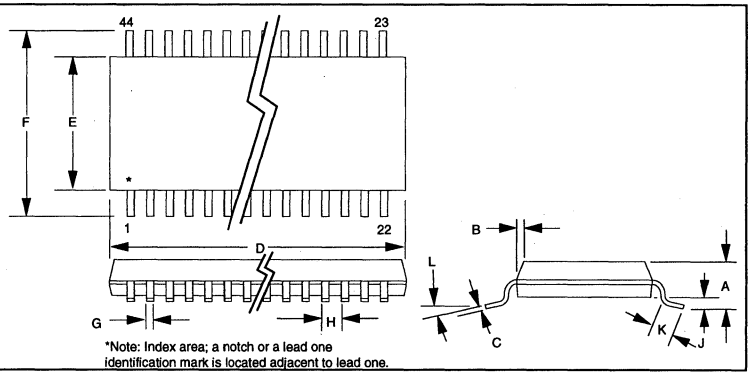
36-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.094	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.33
D	0.602	0.612	15.29	15.54
E	0.293	0.300	7.39	7.62
F	0.398	0.416	10.11	10.57
G	0.012	0.018	0.30	0.46
H	0.0315	BSC	0.80	BSC
J	0.004	0.012	0.10	0.30
K	0.016	0.035	0.41	0.89
L	0°	8°	0°	8°



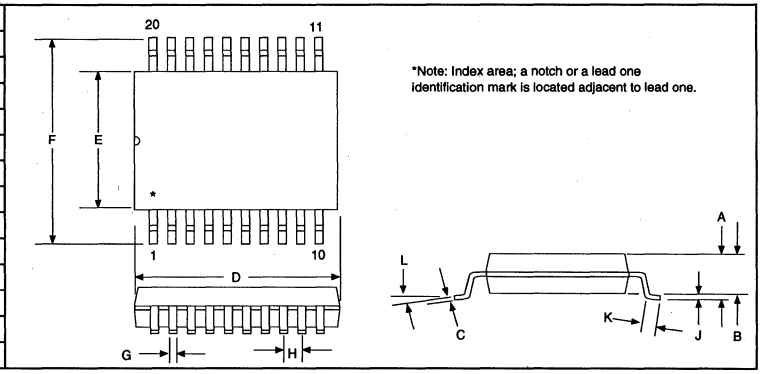
44-Lead SOIC (300 mil)

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.094	0.104	2.46	2.64
B	0.010	0.016	0.25	0.41
C	0.009	0.013	0.23	0.33
D	0.701	0.711	17.81	18.06
E	0.291	0.300	7.39	7.62
F	0.398	0.416	10.11	10.57
G	0.012	0.018	0.30	0.46
H	0.0315	BSC	0.80	BSC
J	0.004	0.012	0.10	0.30
K	0.016	0.035	0.41	0.89
L	0°	8°	0°	8°

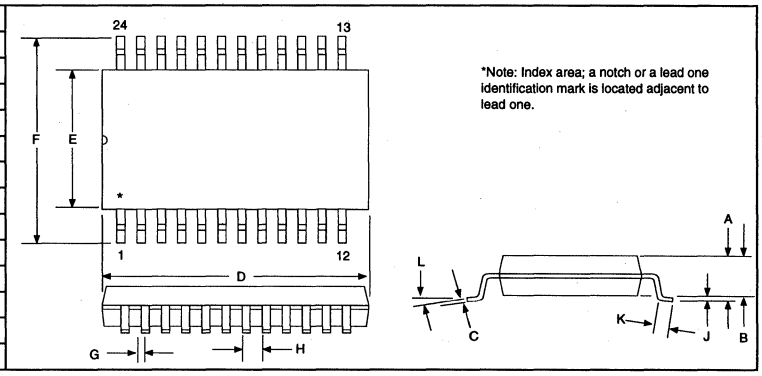


Shrink Small Outline Package (SSOP)

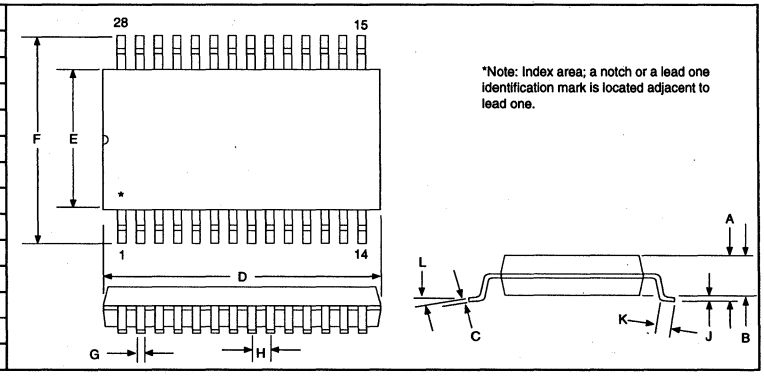
20-LEAD SSOP (5.3mm BODY, 0.65mm LEAD PITCH)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.068	.078	1.73	1.99
B	.066	.070	1.68	1.78
C	.005	.009	0.13	0.22
D	.278	.289	7.07	7.33
E	.205	.212	5.20	5.38
F	.301	.311	7.65	7.90
G	.010	.015	0.25	0.38
H	.0256	BSC	0.65	BSC
J	.002	.008	0.05	0.21
K	.022	.037	0.55	0.95
L	0°	8°	0°	8°



24-LEAD SSOP (.209" BODY, 0.65mm LEAD PITCH)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.068	.078	1.73	1.99
B	.066	.070	1.68	1.78
C	.005	.009	0.13	0.22
D	.318	.328	8.07	8.33
E	.205	.212	5.20	5.38
F	.301	.311	7.65	7.90
G	.010	.015	0.25	0.38
H	.0256	BSC	0.65	BSC
J	.002	.008	0.05	0.21
K	.022	.037	0.55	0.95
L	0°	8°	0°	8°



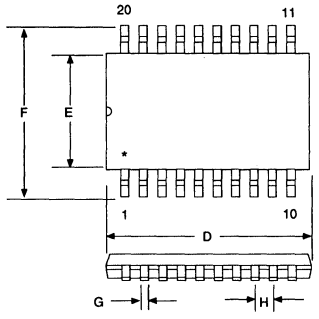
28-LEAD SSOP (5.3mm BODY, 0.65mm LEAD PITCH)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.068	.078	1.73	1.99
B	.066	.070	1.68	1.78
C	.005	.009	0.13	0.22
D	.397	.407	10.07	10.33
E	.205	.212	5.20	5.38
F	.301	.311	7.65	7.90
G	.010	.015	0.25	0.38
H	.0256	BSC	0.65	BSC
J	.002	.008	0.05	0.21
K	.022	.037	0.55	0.95
L	0°	8°	0°	8°



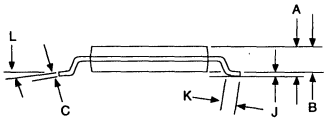
PACKAGING AND ORDERING

Very Small Outline Package (VSOP)

20-Lead VSOP (4.40mm BODY, 0.65mm LEAD PITCH)				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	–	.0394	–	1.00
B	.0325	nom	0.825	nom
C	.004	.0078	0.107	0.197
D	.252	.260	6.40	6.60
E	.169	.176	4.30	4.48
F	.246	.256	6.25	6.50
G	.004	.012	0.10	0.30
H	.0256	BSC	0.65	BSC
J	.002	.006	0.05	0.15
K	.016	.024	0.40	0.60
L	0°	8°	0°	8°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.



PACKAGING AND ORDERING

Ordering Information

Fax or Mail Orders to: VTC Inc.
Attn: Customer Service

Mailing Address: 2800 East Old Shakopee Road
Bloomington, MN 55425-1350

Fax: (612) 853-3355

Telephone: (612) 853-5100

Toll Free: (800) VTC-DISC

ORDERING GUIDE FOR MASS STORAGE PRODUCTS

V M 715 N XX 4 PO *

Manufacturer's ID

Family
M = Mass Storage (Disk Drive Circuits)

Part Number

Damping Resistor Designator on Preamps
R = Indicates Damping Resistor
N = No Damping Resistor on VM312, VM100, VM7200 Families*
No Designator = Indicates no damping resistor or indicates a Schottky Isolated Resistor on the VM312, VM313, VM326, VM7000, VM7100 or VM7200 Families*

Revision Designator Supplied by Factory

Package Code
F = Flatpack
NO = Narrow SOIC
P = Plastic DIP (PDIP)
PL = Plastic Leaded Chip Carrier (PLCC)
PM = Mirrored Pinout (SOIC)
PO = Plastic Small Outline Integrated Circuit (SOIC)
QF = Plastic Quad Flatpack (PQFP)
SS = Shrink Small Outline Package (SSOP)
TQ = Thin Quad Flatpack (TQFP)
VS = Very Small Outline Package (VSOP)
CP = Plastic Sampling Package (CAVPAK)

Two Most Significant Digits of Read Voltage Gain

Channel Count on Preamps

*See the VM7100 datasheet for specific ordering information for the VM7100 device.

VTC Inc.
2800 East Old Shakopee Road
Bloomington, MN 55425-1350
Tel: (612) 853-5100
Fax: (612) 853-3355

Toll Free: 800 VTC-DISC

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