WD61C23A

High Performance

Hard Disk Controller

WESTERN DIGITAL

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1.0 DESCRIPTION

The WD61C23A is a high integration, high performance, low cost controller for hard disk drives. This device contains XT and AT interfaces, buffer manager, and disk data formatter. The disk data formatter only controls the formatting and serialization of the disk drive data. Head positioning, head selection, etc. are expected to be supported by other devices. This device, together with the WD61C12 servo/spindle controller and the WD10C27 ENDEC/Data Synchronizer/Frequency Synthesizer device, forms a high performance, high integration chip set for embedded drives.

1.1 FEATURES

1.1.1 Host Interface

- Compatible with PC/AT and PC/XT interfaces
- Supports PC/AT I/O speeds up to 16 MHz
- Internal 24 mA drivers and Schmitt-trigger receivers for direct connection to the PC/XT or PC/AT system bus
- Host transfer rates up to 5 Mwords/sec (10 Mbyte/sec)
- Master/slave mode allows two AT drives on one connector. Hardware ignores host commands when drive is not selected.
- DMA and PIO data transfers. Supports EISA-type B DMA (4 Mbytes/sec).
- Automatic DRQ assertion in AT mode for Write, Write Buffer, Write Long, and Format commands
- Automated Task File update in AT mode for Read, Write, Read Multiple, and Write Multiple commands allows multiple sectors to be transferred without microcontroller intervention. Programmable delay from end of transfer to next HIRQ pulse
- Directly support AT IDE, two-chip select interface or standard AT, one-chip select, four address interface
- PCMCIA interface support ($\overline{\text{HIRQ}}$ and HRST polarity control
- Supports non-AT compatible DRQ enable bit in Fixed Disk Register
- Guaranteed wide index status to AT host
- High current I/O ports to handle $\overline{\text{PDIAG}}$ and $\overline{\text{DASP}}$ controls in AT mode
- Reset control logic combines hard and soft resets from host and generates either system reset, microcontroller interrupt, or both

1.1.2 Buffer Manager

- Direct interface for up to 256 Kbytes of static RAM
- Up to 13.5 Mbyte/sec RAM bandwidth (27 MHz crystal)
- Supports scatter-gather and segmented caching
- Multisector arming of buffers reduces firmware overhead requirements
- Supports Write Caching (allows control of auto-DRQ buffer address)
- Automatic segment wrap control for segment sizes from 4 Kbytes to 256 Kbytes
- 24 byte host FIFO and 12 byte disk FIFO

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1.1.3 SERDES

- Data rate of 27 Mbps NRZ
- Supports embedded servo
- Proprietary data field segmentation allows for optimal selection of servo sample frequency, ZBR support, and defect management. Up to four segments per data field.
- Multiple defect management schemes supported: byte level push-down, sector level push-down, and sector relocation.
- Software selectable 56-bit ECC, 32-bit ECC, or 16-bit CRC for data fields
- Degree 6, 3-way interleaved Reed Solomon ECC with inlaid 32-bit CRC. Can correct single bursts up to 17-bits on-the-fly without microcontroller intervention. Can correct up to nine random bytes using software correction.
- Data Byte Sync redundancy
- ID redundancy
- Software selectable 32-bit ECC or 16-bit CRC for ID fields
- Supports both CHS (cylinder, head, sector) and LBA (logical block address) ID formats. Autoincrement of three byte LBA for multisector commands.
- Supports sector size up to 4096 bytes (743 with Reed-Solomon ECC)
- Supports 5-bit head number field and 12-bit cylinder number field in CHS mode
- Dual-port register file allows full time access to the SERDES state
- Fast abort of SERDES execution
- WF/WUS filter and asynchronous WF/WUS latching
- Automatic power-down of SERDES when idle

1.1.4 Miscellaneous

- Supports Intel-type and Motorola-type microcontrollers. Muxed address/data bus.
- Compatible with the newer high performance microcontrollers such as the Siemens 80C166 and the NEC 78K6 series.
- Programmable $\overline{\text{MCINT}}$ polarity
- All interrupt sources are individually maskable
- $\overline{\text{MCS}}$ pin can be tied to the same source as the WD61C12 and WD10C27 for simpler interfacing to microcontrollers
- Version number of part posted in disk data formatter register after reset
- Internal crystal oscillator
- Low power sleep modes: maximum 50 mW Idle1, 25 mW Idle2, 2.5 µW Standby power
- Direct control of external FET to power drive circuits
- Low power 1.25 micron CMOS design
- Available in 100-pin MQFP and SQFP packages

2.0 SIGNAL DESCRIPTION

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
3	100	BA15	O	**Buffer Address 15** Buffer address when connected to 64K x 4, 128K x 8, or 256K x 4 SRAM devices.
		$\overline{\text{BCS0}}$	O	**$\overline{\text{Buffer Chip Sel 0}}$** Buffer RAM chip select when connected to two 32K x 8 SRAM devices.
4	1	BA16	O	**Buffer Address 16** Buffer address when connected to 128K to 256K bytes of SRAM.
		$\overline{\text{BCS1}}$	O	**$\overline{\text{Buffer Chip Sel 1}}$** Buffer RAM chip select when connected to two 32K x 8 SRAM devices.
5	2	BA17	O	**Buffer Address 17** Buffer address when connected to 256 Kbytes of SRAM.
6	3	HCIO2	I/O	**High Current I/O 2** This is a 24 mA open drain output which can be used for the DRIVE ACTIVE/SLAVE PRESENT ($\overline{\text{DASP}}$) signal on the AT IDE cable. HCIO2 can also be used as an open drain general purpose I/O.
7	4	$\overline{\text{CS0}}$/HA9	I	**$\overline{\text{Chip Select 0}}$** This signal is decoded from the AT/XT bus and is used to qualify $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ when accessing the Control Block Registers.
8	5	$\overline{\text{CS1}}$/$\overline{\text{HCS}}$	I	**$\overline{\text{Chip Select 1}}$** This signal is decoded from the AT address bus and is used to qualify $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ when accessing the Control Block Registers. $\overline{\text{CS1}}$ is ignored in XT mode.
9	6	HCIO1	I/O	**High Current I/O 1** This is a 24 mA open drain output which can be used for the Passed Diagnostic ($\overline{\text{PDIAG}}$) signal on the AT IDE cable. HCIO1 can also be used as an open drain general purpose I/O.

TABLE 2-1. SIGNAL DESCRIPTION

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NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
10	7	$\overline{\text{IOCS16}}$	O	**$\overline{\text{I/O Chip Select 16}}$** This output is used to indicate fast 16-bit data transfers in AT mode. It is asserted for all PIO Data Port transfers except for ECC byte transfers. It can optionally be used in DMA mode to suppress wait states during DMA cycles.
11	8	HIRQ/$\overline{\text{HIRQ}}$	O	**Interrupt Request /$\overline{\text{Interrupt Request}}$** HIRQ indicates to the PC/AT or PC/XT that a data block transfer is requested or a command has been completed. $\overline{\text{HIRQ}}$ is the active low version of this function, if HPOL = 1
12	9	DREQ	O	**DMA Request** This signal is used in DMA mode to control data transfers. This output is tristated at power-up.
13	10	$\overline{\text{DACK}}$	I	**$\overline{\text{DMA Acknowledge}}$** DACK is asserted by the Host in response to the DREQ signal assertion in order to complete the DMA handshake. It qualifies IOR and IOW during DMA Data Port transfers.
14	11	NC	NA	**No Connect** No Connection.
15	12	VSS	NA	**Ground** Ground
16	13	VDD	NA	**+5V** + 5V
17	14	$\overline{\text{IOR}}$	I	**$\overline{\text{IOR Read}}$** IOR is asserted by the PC/AT or PC/XT host together with CS0, CS1, or DACK to read an internal register or the FIFO.
18	15	$\overline{\text{IOW}}$	I	**$\overline{\text{I/O Write}}$** IOW is asserted by the PC/AT or PC/XT host together with CS0, CS1, or DACK to write an internal register or the FIFO.
19-26	16-23	HD15 THRU HD8	I/O	**Host Data 15 thru Host Data 8** These eight pins are used for the upper byte of 16-bit host data transfers. When in 8-bit mode these pins are optionally terminated to Vcc interally.
27	24	VSS	NA	**Ground** Ground.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
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PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
28	25	HRST/	I	**Host Reset** This input, when asserted will reset the WD61C23A and cause a reset interrupt to the microcontroller. Assertion of this input will cause RESET to be asserted when the DRO control bit is 0.
		HRST		**Host Reset** HRST is the active high version of this function, if HPOL = 1.
29 30 31	26 27 28	HA1 HA0 HA2	I I I	**Host Address 1, Host Address 0, Host Address 2** These three inputs are used to select which internal host register is selected. The register set is a function of the AT/XT mode select bit. HA2 is not used in XT mode.
32	29	VSS	NA	**Ground** Ground.
33-40	30-37	HD7 THRU HD0	O	**Host Data 7 thru Host Data 0** These eight pins are used to transfer 8-bit data as well as to access the host registers.
41	38	VDD	NA	**+ 5V** + 5V
42	39	VSS	NA	**Ground** Ground.
43	40	SCT	I	**Sector** In hard sector mode SCT is used to indicate the start of a sector. It also indicates the position of embedded servo burst when data field segmentation is used.
44	41	IDX	I	**Index** Index input is used to define the beginning of a track.
45	42	SGATE	I	**Servo Gate** SGATE is an input from the servo control which is asserted over the servo fields. It is used to disable the AME/AMD handshake as well as to inhibit RWB over the servo fields.
46	43	WF/WUS	I	**Write Fault/Write Unsafe** Schmitt-triggered Write Fault/Write Unsafe input.
47	44	RWB	O	**Read/Write** RWB is an open drain output used to control the pulse detector and head preamp.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
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PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
48	45	ALE	I	**Address Latch Enable** ALE is used to latch the lower eight address bits from the multiplexed address/data lines (AD7-AD0).
49	46	$\overline{MRE}$	I	**$\overline{Microcontroller\ Read\ Enable}$** MRE is asserted by the local microcontroller to read an internal register or the buffer.
		DS	I	**Data Strobe** DS is used by Motorola-type microcontrollers to enable the data transfer.
50-57	47-54	AD0 THRU AD7	I/O	**Address/Data 0 thru Address/Data 7** The multiplexed address/data lines are used to load the register address on the falling edge of ALE, and are used for data transfers to/from the local microcontroller.
58	55	$\overline{MCS}$	I	**$\overline{Microcontroller\ Chip\ Select}$** This signal is decoded from the upper microcontroller address and is used internally to qualify MRE and MWE when accessing registers or the buffer.
59	56	$\overline{PWR}$	NA	**$\overline{Power}$** Power is used to drive an external FET to control power down for the rest of the drive circuits.
60	57	$\overline{MWE}$ MRWB	I	**Microcontroller Write Enable,** **Microcontroller Read/$\overline{Write}$** MWE is asserted by the local microcontroller to write an internal register or the buffer. MR/$\overline{W}$ is used by Motorola-type microcontrollers to control the direction of data transfers.
61	58	$\overline{MCINT}$	O	**$\overline{Microcontroller\ Interrupt}$** This output is used as an interrupt signal in order to alert the local microcontroller it is necessary to check command parameters or status. For the XT mode, MCINT is asserted when the controller is selected.
62	59	RBIAS	NA	**Bias Resistor** This pin is connected to a 1 Kohm 1% resistor to control the output driver transition speed to minimize switching noise.
63	60	XIN	I	**Crystal Input** Crystal oscillator input. The crystal frequency is twice the buffer data rate.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
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PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
64	61	XOUT	O	**Crystal Out** Crystal oscillator output.
65	62	VSS	NA	**Ground** Ground.
66	63	$\overline{\text{RESET}}$	I/O	**$\overline{\text{Reset}}$** Open-drain output, can be wire-ORed with an external reset. The WD61C23A will reset all logic when this input is asserted. When the host issues a soft reset or asserts the HRST pin, then this output will be asserted as long as the DRO control bit is 0.
67	64	WCKO	O	**Write Clock Output** WCKO is an output generated from RRCK and is used to clock WDATA into the external ENDEC.
68	65	WDATA	O	**Write Data** WDATA is the NRZ data written to the disk or external ENDEC.
69	66	RRCK	I	**Read/Reference Clock** RRCK is used to shift in the RDATA during reads and to shift out the WDATA during writes. RRCK is also used to control the internal sequencer.
70	67	RDATA	I	**Read Data** RDATA is NRZ read data from the disk or external ENDEC.
71	68	RGATE	O	**Read Gate** RGATE is asserted to initiate a search for an address mark. It remains asserted until the end of the ID or data field.
72	69	ENCEN	O	**Encode Enable** ENCEN is asserted when valid data is to be written to the disk/ENDEC. It enables the encoding function and is negated on Write Fault (WF/WUS) or if the Abort port is written.
73	70	AME	O	**Address Mark Enable** The Address Mark Enable signal is used to control the writing of and searching for Address Marks when connected to an ESDI disk drive or external ENDEC.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
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PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
74	71	$\overline{\text{AMDETECT}}$	I	**$\overline{\text{AM Detect}}$** In soft sector mode, AMD asserted low indicates that the external ESDI drive or ENDEC has detected an Address Mark.
		$\overline{\text{SYNDET}}$	I	**$\overline{\text{Sync Detect}}$** $\overline{\text{SYNDET}}$ is asserted by an ENDEC device when it has detected a byte sync character, if sync detection is done in the ENDEC.
75	72	$\overline{\text{BWE}}$	O	**$\overline{\text{Buffer Write Enable}}$** BWE is asserted by the chip to write data into the external SRAM buffer.
76	73	$\overline{\text{BOE}}$	O	**$\overline{\text{Buffer Output Enable}}$** BOE is asserted by the chip to read data from the external SRAM buffer.
77-84	74-81	BD0 THRU BD7	I/O	**Buffer Data 0 thru Buffer Data 7** Buffer data bus, which connects directly to a static RAM. Also used to read up to eight configuration pullup resistors.
1,2 85-90, 92-94, 97-100	98,99 82-87, 89-91, 94-97	BA0 THRU BA14	O	**Buffer Address 0 thru Buffer Address 14** Buffer address bus, for direct connection up to 256 Kbytes of SRAM.
91	82	VDD	NA	**+ 5V** + 5V
95	92	VSS	NA	**Ground** Ground.
96	95	VSS	NA	**Ground** Ground.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

3.0 ARCHITECTURE

The WD61C23A is a high performance, high integration, low cost hard disk controller designed for PC/At and PC/XT applications. It is a 100-pin CMOS VLSI device which contains a disk formatter and serializer (SERDES), buffer manager, and host interface logic. The WD61C23A will support 1:1 interleave and disk data rates up to 27 Mbits/sec NRZ and 8- or 16-bit host data transfers up to 10 Mbytes/sec (5 Mwords/sec).

The WD61C23A includes four major blocks. The host interface connects directly to a PC/AT or PC/XT-type bus. The WD61C23A has 24 mA high current drivers and Schmitt trigger inputs on the host port which allow it to be connected directly to the PC/AT or PC/XT bus. The host interface includes advanced DMA logic that supports high speed burst transfers such as EISA-type B DMA. The device contains features designed to reduce the amount of real-time interaction needed by the microcontroller to manage the host protocol. The device pinout has been optimized for XT and AT IDE applications.

The local microcontroller interface is used to interface to a microcontroller such as the 8051, 80C196 (16 MHz), 68HC11, Siemens 80C166 (40 MHz), NEC K6 (40 MHz), etc. It has an 8-bit muxed address/data bus. It has a chip select input allowing it to be accessed anywhere in the microcontroller's address space. Internal logic decodes this 8-bit address and only allows access in a limited range of the 256 location register space. This allows the WD61C23A to use the same chip select as the WD61C12 servo/spindle chip and the WD10C27 ENDEC/data synchronizer/frequency synthesis chip.

The buffer manager can control multiple sector buffers up to 256 Kbytes using static RAM and allows simultaneous access from both the host and the disk. The pipelined architecture allows sophisticated scatter-gather and segmented buffer management as well as simple ring buffering. Multisector arming and automatic pointer segment wrap control ease the microcontroller overhead.

The SERDES contains a formatter which can support advanced defect management schemes, zone bit recording, hard or soft sectoring, and programmable format. The SERDES supports multitrack commands automatically. An NRZ interface is used to connect to an external ENDEC. Data integrity is insured through 16-bit CRC, 32-bit ECC, or 56-bit polynomials, and degree 6, three-way interleaved Reed-Solomon ECC. Additional options support Data Byte Sync redundancy and ID field redundancy.

3.1 HOST INTERFACE ORGANIZATION

The WD61C23A host interface is designed to connect to the IBM PC/XT or IBM PC/AT system bus as well as the system bus of any PC/XT or PC/AT clone. The WD61C23A has high current drivers and Schmitt receivers which allow for direct connection to the system bus. The host interface is inactive at power-up. The host interface is controlled by the AT/XT control bit in General Control Register 2 which is written by the local microcontroller.

3.1.2 XT Host Interface

When the AT/$\overline{XT}$ control bit is written to 0, then the WD61C23A is in PC/$\overline{XT}$-compatible interface mode. In this mode the $\overline{CS0}$ chip select should be active when I/O ports 320 hex through 323 hex are addressed for the primary controller in the XT system and for I/O ports 324 through 327 for the secondary controller. HA0 and HA1 select which register is being accessed. HA2 and $\overline{CS1}$ are not used in this mode and are optionally terminated to V_{DD} through internal registers.

Data transfers in this mode may be either PIO or DMA and can be either 8- or 16-bits wide. When 8-bit data transfer mode is selected, then the upper eight host data inputs may be optionally terminated to V_{DD} through internal registers.

3.1.2 AT Host Interface

When the AT/$\overline{XT}$ control bit is written to 1, then the WD61C23A is in PC/AT-compatible interface mode. $\overline{CS0}$ should be active when I/O ports 1F0 hex through 1F7 hex are addressed for the primary controller in the AT system. $\overline{CS1}$ should be active when 3F6 hex and 3F7 hex are addressed. Addresses 170 through 177 hex ($\overline{CS0}$) and 376, 377 hex ($\overline{CS1}$) are used for the secondary controller.

Buffer data transfers can be either PIO or DMA and can be either 8 or 16 bits. The ECC byte transfers

in a long mode read or write commands are always 8 bits. All other register transfers are 8 bits. When 16-bit PIO data transfers occur for port 0 then the IOCS16 output will be asserted. There is an option to allow the IOCS16 to be asserted during PIO transfers on DMA commands. There is also an option to allow IOCS16 to be asserted during DMA transfers, allowing an interarchitecture high speed DMA transfer mode. There is also an option to allow nonstandard host register bits to control the DMA interface.

There are additional features to alleviate the microcontroller from some of the real-time requirements of the AT host interface. First, there is a mode to automatically arm the first buffer transfer for Write, Write Long, Write Buffer, and Format commands. This buffer may be selected to be either buffer 0 of the buffer pointed to by the Host Buffer Pointer Pipeline registers. This feature allows write operations to be cached. When this mode is used, care should be taken to ensure that the buffer selection (both ADQBC bit and pipeline registers) are only modified when ABSY=1 in the Drive Status registers.

Secondly, the WD61C23A can be programmed to automatically sequence the AT task file during multisector Read, Write, Read Multiple, and Write Multiple data transfers. When this option is used, the microcontroller need only maintain the host buffer manager and the WD61C23A will automatically update the task file before releasing each sector or group of sectors to the host.

The microcontroller sets up the logical sectors per track and heads per cylinder parameters and the internal state machine will automatically handle logical track boundaries. Hardware in the part will automatically reset the Auto Task-File Update bit (ATU) upon receipt of a new command to prevent an unwanted task file increment at the start of any of the auto-DRQ commands mentioned above.

It is therefore important that the microcontroller pulse the RHBM bit in the Buffer Command Register at the start of any new command.

The AT task file is implemented as a dual port RAM allowing full time access by the microcontroller. This is true even when the internal state machine updates the task file and is independent of the state of the ABSY status bit.

There are features in the part to handle the IDE dual drive interface. First, there is internal hardware to allow only the selected drive to assert the bus interface signals. Secondly, the WD61C23A will only go busy on commands when it is the selected drive. The exception to this is on the Controller Diagnostic command. For this command the WD61C23A will go busy regardless of which drive is currently selected. Also on the Controller Diagnostic command, hardware in the WD61C23A will force the drive selection bit in the host Drive/Head Register to select drive 0.

The WD61C23A has two features that allow the part to be easily interfaced to the PCMCIA interface. First, the polarities of the HIRQ/HIRQ and HRST/HRST pins are programmable. Secondly, the part supports a single chip select, four address host decode option in addition to the traditional IDE two-chip select, three address interface.

The part also includes high current outputs and Schmitt receivers to handle the DASP and PDIAG IDE signals. This helps to eliminate external glue logic needed to implement an IDE drive. HCIO1 (PDIAG) will be set and HCIO2 (DASP) will be cleared upon any reset. In addition, HCIO1 (PDIAG) will be set upon receipt of a Controller Diagnostic command in AT mode.

3.2 MICROCONTROLLER INTERFACE

The microcontroller controls the Host Interface mode (PCAT or PCXT) and controls the buffer manager and the SERDES. The microcontroller is told to perform any required tasks by the assertion of the $\overline{\text{MCINT}}$ output. There are a number of sources for this $\overline{\text{MCINT}}$ and they are individually maskable. The polarity of the $\overline{\text{MCINT}}$ output is programmable.

In PCXT mode, $\overline{\text{MCINT}}$ is asserted when the controller is selected. In PCAT mode $\overline{\text{MCINT}}$ will be asserted when the Host writes to the command register. $\overline{\text{MCINT}}$ will be asserted whenever a buffer address is transferred from a pipeline register to the appropriate pointer.

$\overline{\text{MCINT}}$ is also asserted by the detection of a host soft or hard reset, FIFO error, or by the SERDES.

The microcontroller can have either the Intel-type (8051 or 80C196) or the Motorola-type (68HC11) interface. The WD61C23A has the built-in logic to sense the processor interface type and can therefore be directly interfaced to either type processor. Data and address are transferred via an 8-bit multiplexed bus. The WD61C23A has been designed to share a common chip select with the WD61C12 servo/spindle controller and the WD10C27 ENDEC/data synchronizer/frequency synthesizer.

3.3 BUFFER MANAGER DESCRIPTION

The buffer manager can control multiple sector buffers totalling up to 256 Kbytes using static RAM. The sector buffers can be any size up to 4095 bytes, excluding ECC, and can be located on any byte boundary. The buffer manager has two address counters, one for the host interface and one for the disk data buffer. Both counters can access the SRAM concurrently. The buffer manager handles the arbitration between the host interface and the disk formatter. Both address counters have a pipeline register that can be loaded with a new buffer address while a transfer is in progress. This allows discontiguous buffer locations to be linked without the loss of RAM bandwidth between blocks. The transfer length on the host side is controlled by a 12-bit transfer count register. The disk transfer length is controlled by the disk formatter.

The buffer manager has two pipelined block counters allowing up to 256 blocks (sectors) to be armed at one time. This eliminates the sector-by sector buffer interrupt handling required by earlier controllers. Secondly, a segment wrap control feature allows the buffer memory to be broken into several smaller buffer segments with automatic wrap from the end of each segment back to the start. The segment sizes are programmable from 4 Kbytes to 256 Kbytes.

Both ports have FIFOs allowing sustained host bandwidth of 5 Mwords/sec for 16-bit wide transfers and 10 Mbytes/sec for 8-bit wide transfers. The buffer manager can sustain a RAM bandwidth of 12.5 Mbytes/sec when using a 25 MHz crystal.

The local microcontroller accesses the buffer RAM by using the Disk Buffer Manager logic. It first loads the desired starting address into the Disk Buffer Pointer. The proper buffer manager control bits are then set to enable the local microcontroller access to the buffer. When the local microcontroller accesses the special RAM access port (Register 3E) the data will be read/written through the disk formatter's FIFO port to the buffer. The RAM can only be accessed sequentially from the starting address and only in one direction at a time as set by the DRWB control bit. When the microcontroller is accessing the buffer, the disk formatter must be idle.

There is a special mode in the buffer manager that allows the microcontroller to sense the presence of external pullups on the BD bus. These pullups can be used to reconfigure the firmware. To use this feature, the microcontroller writes the RDCF bit to 1 and then after 5 µsec reads the configuration port. If a pullup is present on a BD line then the appropriate bit in the configuration register will be read as a 1. If there is no external pullup then the bit will be read as a 0.

3.4 DISK FORMATTER DESCRIPTION

The WD61C23A has a high speed disk formatter which can handle the requirements of high performance embedded drives. The WD61C23A has an NRZ interface which allows it to be connected to an external ENDEC.

The formatter supports data rates up to 27 Mbit/sec. Software selectable 16-bit CRC, 32-bit ECC, and 56-bit ECC polynomials ensure data reliability.

The WD61C23A qualifies NRZ disk data using the Sector (SCT) and Address Mark Detect (AMD) signals, and controls the Read Gate and Write Gate timing.

The disk data formats are software programmable. The WD61C23A supports both soft and hard sectoring. The gaps and PLO fields are programmable. The ID is programmable in size from 4 to 12 bytes. The extra bytes can be used for flag information for defect management, or for size information for segmenting data fields around defects or around servo bursts. With this feature, zone bit recording with embedded servo positioning is possible with minimal processor overhead.

The disk formatter has internal control logic to automatically support zone bit recording and defect management without microcontroller intervention. Logic in the disk formatter will interpret the ID information pertaining to segmentation and automatically step around servo fields and defects. In addition, the disk formatter will interpret special flag information in the ID for detecting the last sector on a track to support sector push down defect management and multitrack commands. Finally, the disk formatter will interpret another ID flag bit to detect that a sector has been relocated to a spare area on the drive. In this case the disk formatter can be configured to automatically read out a pointer to the spare sector used to replace the defective sector.