Please use this Xicor Data Book Supplement in conjunction with the Xicor 1988 Data Book, Stock No. 100-080, which contains additional product line information, product reliability reports and application notes.

NEW 1990 Xicor Data Book Reservations:
In order to reserve a copy of the new 1990 Xicor Data Book, please complete a Business Reply Card as provided at the back of this Supplement, and mail it to:

Xicor, Inc.
851 Buckeye Court
M/S 301
Milpitas, CA 95035
Precautions for the Handling of MOS Devices

Xicor products are designed with effective input protection to prevent damage to the devices under most conditions. However, any MOS circuit can be catastrophically damaged by excessive electrostatic discharge or transient voltages. The following procedures are recommended to avoid accidental circuit damage.

I. Testing MOS Circuits:
   1. All units should be handled directly from the conductive or antistatic plastic tube in which they were shipped if possible. This action minimizes touching of individual leads.
   2. If units are to be tested without using the tube carrier, the following precautions should be taken:
      a. Table surfaces which potentially will come in contact with the devices either directly or indirectly (such as through shipping tubes) must be metal or of another conductive material and should be electrically connected to the test equipment and to the test operator (a grounding bracelet is recommended).
      b. The units should be transported in bundled antistatic tubes or metal trays, both of which will assume a common potential when placed on a conductive table top.
      c. Do not band tubes together with adhesive tape or rubber bands without first wrapping them in a conductive layer.

II. Test Equipment (Including Environmental Equipment):
   1. All equipment must be properly returned to the same reference potential (ground) as the devices, the operator, and the container for the devices.
   2. Devices to be tested should be protected from high voltage surges developed by:
      a. Turning electrical equipment on or off.
      b. Relay switching.
      c. Transients from voltage sources (AC line or power supplies).

III. Assembling MOS Devices Onto PC Boards:
   1. The MOS circuits should be mounted on the PC board last.
   2. Similar precautions should be taken as in Item I above, at the assembly work station.
   3. Soldering irons or solder baths should be at the same reference (ground) potential as the devices.
   4. Plastic materials which are not antistatic treated should be kept away from devices as they develop and maintain high levels of static charge.

IV. Device Handling:
   1. Handling of devices should be kept to a minimum. If handling is required, avoid touching the leads directly.

V. General:
   1. The handler should take every precaution that the device will see the same reference potential when moved.
   2. Anyone handling individual devices should develop a habit of first touching the container in which the units are stored before touching the units.
   3. Before placing the units into a PC board, the handler should touch the PC board first.
   4. Personnel should not wear clothing which will build up static charge. They should wear smocks and clothing made of 100% cotton rather than wool or synthetic fibers.
   5. Be careful of electrostatic build up through the movement of air over plastic material. This is especially true of acid sinks.
   6. Personnel or operators should always wear grounded wrist straps when working with MOS devices.
   7. A 1 meg ohm resistance ground strap is recommended and will protect people up to 5,000 volts AC RMS or DC by limiting current to 5 milliamperes.
   8. Antistatic ionized air equipment is very effective and useful in preventing electrostatic damage.
   9. Low humidity maximizes potential static problems. Maintaining humidity levels above 45% is one of the most effective ways to guard against static handling problems.
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NOVRAM is Xicor's nonvolatile static RAM device.
Please use this Xicor Data Book Supplement in conjunction with the Xicor 1988 Data Book, Stock No. 100-080, which contains additional product line information, product reliability reports and application notes.
TYPICAL FEATURES

• Low Power CMOS
  —2 mA Active Current Typical
  —60 µA Standby Current Typical
• Internally Organized 128 x 8
• 2 Wire Serial Interface
  —Provides Bidirectional Data Transfer Protocol
• Four Byte Page Write Mode
• Self Timed Write Cycle
  —Typical Write Cycle Time of 5 ms
• Inherent 100+ Years Data Retention
• 8-Pin Mini-DIP Package
• 8-Pin SOIC Package

DESCRIPTION

The X24C01 is a CMOS 1024 bit serial E²PROM, internally organized as 128 x 8. The X24C01 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance.
ABSOLUTE MAXIMUM RATINGS*  

Temperature Under Bias  
X24C01 ........................................... -10°C to + 85°C  
X24C011 .......................................... -65°C to + 135°C  
Storage Temperature ..................... -65°C to + 150°C  
Voltage on any Pin with Respect to VSS .................. -1.0V to + 7V  
D.C. Output Current .......................... ≤ 5 mA  
Lead Temperature (Soldering, 10 Seconds) ............... ≤ 300°C  

D.C. OPERATING CHARACTERISTICS  

X24C01  
TA = 0°C to + 70°C, VCC = +5V ± 10%, unless otherwise specified.  
X24C011  
TA = -40°C to +85°C, VCC = +5V ± 10%, unless otherwise specified.  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(1)</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Power Supply Current</td>
<td>2.0</td>
<td>3.0</td>
<td>mA</td>
<td>fSCL = 100 KHz</td>
<td></td>
</tr>
<tr>
<td>ISB(2)</td>
<td>Standby Current</td>
<td>60</td>
<td>100</td>
<td>µA</td>
<td>VIN = GND or VCC</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage Current</td>
<td>0.1</td>
<td>10</td>
<td>µA</td>
<td>VIN = GND to VCC</td>
<td></td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td>0.1</td>
<td>10</td>
<td>µA</td>
<td>VOUT = GND to VCC</td>
<td></td>
</tr>
<tr>
<td>VIL(3)</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td></td>
<td>V</td>
<td>VCC × 0.3</td>
<td></td>
</tr>
<tr>
<td>VIH(3)</td>
<td>Input High Voltage</td>
<td>VCC × 0.7</td>
<td></td>
<td>V</td>
<td>VCC + 0.5</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td>IOL = 2.1 mA</td>
<td></td>
</tr>
</tbody>
</table>

CAPACITANCE  
T_A = 25°C, f = 1.0 MHz, V_CC = 5V  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIO(4)</td>
<td>Input/Output Capacitance (SDA)</td>
<td>8</td>
<td>pF</td>
<td>VIN/O = 0V</td>
</tr>
<tr>
<td>CIN(4)</td>
<td>Input Capacitance (SCL)</td>
<td>6</td>
<td>pF</td>
<td>VIN = 0V</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST  

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>VCC × 0.1 to VCC × 0.9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>VCC × 0.5</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and CL = 100 pF</td>
</tr>
</tbody>
</table>

Notes:  
(1) Typical values are for T_A = 25°C and nominal supply voltage.  
(2) SDA and SCL require pull-up resistor.  
(3) VIL min. and VIH max. are for reference only and are not tested.  
(4) This parameter is periodically sampled and not 100% tested.  

SYMBOL TABLE  

WAVEFORM  
<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td>Don't Care: Changes</td>
<td>State Not Allowed</td>
</tr>
<tr>
<td>N/A</td>
<td>Center Line is High Impedance</td>
</tr>
</tbody>
</table>
A.C. CHARACTERISTICS LIMITS

X24C01 $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.
X24C01I $T_A = -40^\circ C$ to $+85^\circ C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

### Read & Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SCL}$</td>
<td>SCL Clock Frequency</td>
<td>0</td>
<td>100</td>
<td>KHz</td>
</tr>
<tr>
<td>$T_1$</td>
<td>Noise Suppression Time Constant at SCL, SDA Inputs</td>
<td></td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AA}$</td>
<td>SCL Low to SDA Data Out Valid</td>
<td>0.3</td>
<td>3.5</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{BUF}$</td>
<td>Time the Bus Must Be Free Before a New Transmission Can Start</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{HD:STA}$</td>
<td>Start Condition Hold Time</td>
<td>4.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{LOW}$</td>
<td>Clock Low Period</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{HIGH}$</td>
<td>Clock High Period</td>
<td>4.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{SU:STA}$</td>
<td>Start Condition Setup Time</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{HD:DAT}$</td>
<td>Data In Hold Time</td>
<td>0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{SU:DAT}$</td>
<td>Data In Setup Time</td>
<td>250</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_R$</td>
<td>SDA and SCL Rise Time</td>
<td></td>
<td>1</td>
<td>µs</td>
</tr>
<tr>
<td>$t_F$</td>
<td>SDA and SCL Fall Time</td>
<td></td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SU:STO}$</td>
<td>Stop Condition Setup Time</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>Data Out Hold Time</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### Typical Power-Up Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PUR}^{(5)}$</td>
<td>Power-Up to Read Operation</td>
<td>1</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{PUW}^{(5)}$</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

### Bus Timing

Note: (5) This parameter is periodically sampled and not 100% tested.
Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ. (6)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{WR} ) (7)</td>
<td>Write Cycle Time</td>
<td></td>
<td>5</td>
<td>10</td>
<td>ms</td>
</tr>
</tbody>
</table>

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

Write Cycle Timing

PIN DESCRIPTIONS

Serial Clock (SCL)
The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)
SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

DEVICE OPERATION

The X24C01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. A controller initiates data transfers, and provides the clock for both transmit and receive operations.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C01 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. This is true only if the previous sequence was correctly terminated with a stop condition.

Notes:

(6) Typical values are for \( T_A = 25^\circ \text{C} \) and nominal supply voltage (5V).

(7) \( t_{WR} \) is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
Stop Condition
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Acknowledge
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C01 will always respond with an acknowledge after recognition of a start condition, a seven bit word address and a R/W bit. If a write operation has been selected, the X24C01 will respond with an acknowledge after each byte of data is received.

In the read mode the X24C01 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the controller, the X24C01 will continue to transmit data. If an acknowledge is not detected, the X24C01 will terminate further data transmissions and await the stop condition to return to the standby power mode.
WRITE OPERATIONS

Byte Write

To initiate a write operation, the controller sends a start condition followed by a seven bit word address and a write bit. The X24C01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The controller then terminates the transfer by generating a stop condition, at which time the X24C01 begins the internal write cycle to the non-volatile memory. While the internal write cycle is in progress, the X24C01 inputs are disabled, and the device will not respond to any requests from the controller. Refer to Figure 4 for the address, acknowledge and data transfer sequence.
Page Write
The most significant five bits of the word address define the page address. The X24C01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the controller can transmit up to three more bytes. After the receipt of each data byte, the X24C01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the controller should transmit more than four data bytes prior to generating the stop condition, the address counter will “roll over” and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Acknowledge Polling
The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host’s write operation the X24C01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a read or write operation. If the X24C01 is still busy with the write operation no ACK will be returned. If the X24C01 has completed the write operation an ACK will be returned and the controller can then proceed with the next read or write operation.

READ OPERATIONS
To terminate a read operation, the controller must either issue a stop condition during the ninth cycle or hold SDA high during the ninth clock cycle (i.e. not issue an acknowledge) and then issue a stop condition later.

Byte Read
To initiate a read operation, the controller sends a start condition followed by a seven bit word address and a read bit. The X24C01 responds with an acknowledge and then transmits the eight bits of data. If the controller does not acknowledge the transfer and generates a stop condition, the X24C01 will discontinue transmission. Refer to Figure 6 for the start, word address, read bit, acknowledge and data transfer sequence.

Figure 5: Page Write
**X24C01, X24C01I**

**Figure 6: Byte Read**

Sequential Read
Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the controller now responds with an acknowledge, indicating it requires additional data. The X24C01 continues to output data for each acknowledge received. The read operation is terminated by the controller not responding with an acknowledge and generating a stop condition.

**Figure 7: Sequential Read**

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. When the highest address is reached, the counter “rolls over” to address 0 and the X24C01 continues to output data for each acknowledge received. Refer to Figure 7 for the address, acknowledge and data transfer sequence.
FUNCTIONAL DIAGRAM

(8) Vcc --
(4) Vss --
(5) SDA --
(6) SCL --

START CYCLE

H.V. GENERATION TIMING & CONTROL

E2PROM 32 x 32

XDEC 32

YDEC 8

DATA REGISTER

DOUT

ACK

LOAD

INC

R/W

PIN

CK
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

\[ R_{\text{MIN}} = \frac{V_{\text{CC MAX}}}{I_{\text{OL MIN}}} = 2.6 \, \text{k}\Omega \]

\[ R_{\text{MAX}} = \frac{t_{\text{RISE}}}{C_{\text{BUS}}} \]

Resistors

BUS CAPACITANCE (pF)
## ORDERING INFORMATION
### SERIAL E²PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X24C01S</td>
<td>128 x 8</td>
<td>•</td>
<td>†</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24C01SI</td>
<td>128 x 8</td>
<td>•</td>
<td>I</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24C01P</td>
<td>128 x 8</td>
<td>•</td>
<td>†</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24C01PI</td>
<td>128 x 8</td>
<td>•</td>
<td>I</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

**Key:**
- † = Blank = Commercial = 0°C to +70°C
- I = Industrial = −40°C to +85°C
- M = Military = −55°C to +125°C

- S = 8-Lead Plastic Small Outline Gull Wing
- P = 8-Lead Plastic DIP
- D = Cerdip
- C = Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
- F2 = Ceramic Flat Pack for X28C256 and X28C256B
- K = Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

---

### LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

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**U.S. PATENTS**

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,481; 4,553,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482. Foreign patents and additional patents pending.

**LIFE RELATED POLICY**

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor’s products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
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TYPICAL FEATURES
• 3V–6V \( V_{CC} \) Operation
• Low Power CMOS
  —2 mA Active Current Typical
  —60 \( \mu \)A Standby Current Typical
• Internally Organized 128 x 8
• 2 Wire Serial Interface
  —Provides Bidirectional Data Transfer Protocol
• Four Byte Page Write Mode
• Self Timed Write Cycle
  —Typical Write Cycle Time of 5 ms
• Inherent 100 + Years Data Retention
• 8-Pin Mini-DIP Package
• 8-Pin SOIC Package

DESCRIPTION
The X24LC01 is a CMOS 1024 bit serial E²PROM, internally organized as 128 x 8. The X24LC01 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance.

PIN NAMES
1 to 3 No Connect
4 \( V_{SS} \)
5 SDA Serial Data
6 SCL Serial Clock
7 No Connect
8 \( V_{CC} +3V \) to +6V

Characteristics subject to change without notice
X24LC01, X24LC011

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
- X24LC01 .............................. -10°C to +85°C
- X24LC011 ............................ -65°C to +135°C

Storage Temperature .............. -65°C to +150°C
Voltage on any Pin with Respect to V88 .................. -1.0V to +7V
D.C. Output Current ....................... 5 mA
D.C. Lead Temperature (Soldering, 10 Seconds) .......... 300°C

*COMMENT
Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

- X24LC01 TA = 0°C to +70°C, VCC = +3V to +6V, unless otherwise specified.
- X24LC011 TA = -40°C to +85°C, VCC = +3V to +6V, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td>Power Supply Current</td>
<td>Min.</td>
<td>Typ.(1)</td>
<td>Max.</td>
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<tr>
<td></td>
<td></td>
<td>2.0</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td>Isb(2)</td>
<td>Standby Current VCC = 6V</td>
<td></td>
<td></td>
<td>150</td>
</tr>
<tr>
<td>Isb(2)</td>
<td>Standby Current VCC = 3V</td>
<td></td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>Il</td>
<td>Input Leakage Current</td>
<td></td>
<td>0.1</td>
<td>10</td>
</tr>
<tr>
<td>Ilo</td>
<td>Output Leakage Current</td>
<td></td>
<td>0.1</td>
<td>10</td>
</tr>
<tr>
<td>VIL(3)</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td></td>
<td>VCC x 0.3</td>
</tr>
<tr>
<td>Vih(3)</td>
<td>Input High Voltage</td>
<td>VCC x 0.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vol</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td></td>
<td>VOUT = GND to VCC</td>
</tr>
</tbody>
</table>

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = 5V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cioc(4)</td>
<td>Input/Output Capacitance (SDA)</td>
<td></td>
<td>8</td>
<td>pF</td>
<td>VIN = 0V</td>
</tr>
<tr>
<td>Cio(4)</td>
<td>Input Capacitance (SCL)</td>
<td></td>
<td>6</td>
<td>pF</td>
<td>VOUT = GND to VCC</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST

| Input Pulse Levels | VCC x 0.1 to VCC x 0.9 |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Levels | VCC x 0.5 |
| Output Load | 1 TTL Gate and Cl = 100 pF |

Notes: (1) Typical values are for TA = 25°C and nominal supply voltage (5V).
(2) SDA and SCL require pull-up resistor.
(3) VIL min. and VIH max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

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<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
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<tbody>
<tr>
<td>Must be steady</td>
<td>Will be steady</td>
<td></td>
</tr>
<tr>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
<td></td>
</tr>
<tr>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
<td></td>
</tr>
<tr>
<td>Don't Care:</td>
<td>Changing:</td>
<td></td>
</tr>
<tr>
<td>Changes State Not Allowed</td>
<td>Known</td>
<td></td>
</tr>
<tr>
<td>Center Line is High Impedance</td>
<td></td>
<td></td>
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1-18
X24LC01, X24LC01I

A.C. CHARACTERISTICS LIMITS
X24LC01 $T_A = 0°C$ to $+70°C$, $V_{CC} = +3V$ to $+6V$, unless otherwise specified.
X24LC01I $T_A = -40°C$ to $+85°C$, $V_{CC} = +3V$ to $+6V$, unless otherwise specified.

Read & Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SCL}$</td>
<td>SCL Clock Frequency</td>
<td>0</td>
<td>100</td>
<td>KHz</td>
</tr>
<tr>
<td>$T_I$</td>
<td>Noise Suppression Time</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{AA}$</td>
<td>SCL Low to SDA Data Out Valid</td>
<td>0.3</td>
<td>3.5</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{BUF}$</td>
<td>Time the Bus Must Be Free Before a New Transmission Can Start</td>
<td>4.7</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{HD:STA}$</td>
<td>Start Condition Hold Time</td>
<td>4.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{LOW}$</td>
<td>Clock Low Period</td>
<td>4.7</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{HIGH}$</td>
<td>Clock High Period</td>
<td>4.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{SU:STA}$</td>
<td>Start Condition Setup Time</td>
<td>4.7</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{HD:DAT}$</td>
<td>Data In Hold Time</td>
<td>0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{SU:DAT}$</td>
<td>Data In Setup Time</td>
<td>250</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_R$</td>
<td>SDA and SCL Rise Time</td>
<td>1</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_F$</td>
<td>SDA and SCL Fall Time</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{SU:STO}$</td>
<td>Stop Condition Setup Time</td>
<td>4.7</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>Data Out Hold Time</td>
<td>300</td>
<td>ns</td>
<td></td>
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</table>

Typical Power-Up Timing

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.(5)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PUR}(6)$</td>
<td>Power-Up to Read Operation</td>
<td>2.0</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{PUW}(6)$</td>
<td>Power-Up to Write Operation</td>
<td>2.0</td>
<td>ms</td>
</tr>
</tbody>
</table>

Bus Timing

Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).
(6) This parameter is periodically sampled and not 100% tested.
Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ. (7)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>twWR (8)</td>
<td>Write Cycle Time</td>
<td></td>
<td>5</td>
<td>10</td>
<td>ms</td>
</tr>
</tbody>
</table>

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

Write Cycle Timing

PIN DESCRIPTIONS

Serial Clock (SCL)
The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)
SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

DEVICE OPERATION

The X24LC01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. A controller initiates data transfers, and provides the clock for both transmit and receive operations.

Clock and Data Conventions
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition
All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC01 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. This is true only if the previous sequence was correctly terminated with a stop condition.

Notes: (7) Typical values are for TA = 25°C and nominal supply voltage (5V).
(8) twWR is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
**Stop Condition**
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

**Acknowledge**
Acknowledgment is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC01 will always respond with an acknowledge after recognition of a start condition, a seven bit word address and a R/W bit. If a write operation has been selected, the X24LC01 will respond with an acknowledge after each byte of data is received.

In the read mode the X24LC01 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the controller, the X24LC01 will continue to transmit data. If an acknowledge is not detected, the X24LC01 will terminate further data transmissions and await the stop condition to return to the standby power mode.
WRITE OPERATIONS

Byte Write
To initiate a write operation, the controller sends a start condition followed by a seven bit word address and a write bit. The X24LC01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The controller then terminates the transfer by generating a stop condition, at which time the X24LC01 begins the internal write cycle to the non-volatile memory. While the internal write cycle is in progress, the X24LC01 inputs are disabled, and the device will not respond to any requests from the controller. Refer to Figure 4 for the address, acknowledge and data transfer sequence.
Page Write
The most significant five bits of the word address define the page address. The X24LC01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the controller can transmit up to three more bytes. After the receipt of each data byte, the X24LC01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the controller should transmit more than four data bytes prior to generating the stop condition, the address counter will "roll over" and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Acknowledge Polling
The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a read or write operation. If the X24LC01 is still busy with the write operation no ACK will be returned. If the X24LC01 has completed the write operation an ACK will be returned and the controller can then proceed with the next read or write operation.

READ OPERATIONS
To terminate a read operation, the controller must either issue a stop condition during the ninth cycle or hold SDA high during the ninth clock cycle (i.e. not issue an acknowledge) and then issue a stop condition later.

Byte Read
To initiate a read operation, the controller sends a start condition followed by a seven bit word address and a read bit. The X24LC01 responds with an acknowledge and then transmits the eight bits of data. If the controller does not acknowledge the transfer and generates a stop condition, the X24LC01 will discontinue transmission. Refer to Figure 6 for the start, word address, read bit, acknowledge and data transfer sequence.

Figure 5: Page Write
Sequential Read
Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the controller now responds with an acknowledge, indicating it requires additional data. The X24LC01 continues to output data for each acknowledge received. The read operation is terminated by the controller not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address \( n \) followed by the data from \( n+1 \). The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. When the highest address is reached, the counter "rolls over" to address 0 and the X24LC01 continues to output data for each acknowledge received. Refer to Figure 7 for the address, acknowledge and data transfer sequence.
Functional Diagram
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

\[
R_{\text{MIN}} = \frac{V_{\text{CC MAX}}}{I_{\text{OL MIN}}} = 2.85 \text{ K}\Omega
\]

\[
R_{\text{MAX}} = \frac{t_{\text{RISE}}}{C_{\text{BUS}}}
\]

![Graph showing resistance vs. bus capacitance]
# X24LC01, X24LC01I

## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Process Technology</th>
<th>Processing Level</th>
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</thead>
<tbody>
<tr>
<td>X24LC01S</td>
<td>128 x 8</td>
<td>•</td>
<td>†</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC01SI</td>
<td>128 x 8</td>
<td>•</td>
<td>I</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC01P</td>
<td>128 x 8</td>
<td>•</td>
<td>†</td>
<td>CMOS</td>
<td>Standard</td>
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<tr>
<td>X24LC01PI</td>
<td>128 x 8</td>
<td>•</td>
<td>I</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

**Key:**
- † = Blank = Commercial = 0°C to + 70°C
- I = Industrial = - 40°C to + 85°C
- M = Military = - 55°C to + 125°C
- S = 8-Lead Plastic Small Outline Gull Wing
- P = 8-Lead Plastic DIP
- D = Cerdip
- C = Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
- F2 = Ceramic Flat Pack for X28C256 and X28C256B
- K = Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

## LIMITED WARRANTY

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### U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482. Foreign patents and additional patents pending.

### LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor’s products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPES

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
### Sales Offices

#### U.S. Sales Offices

<table>
<thead>
<tr>
<th>Area</th>
<th>Company</th>
<th>Address</th>
<th>Phone</th>
<th>Telex</th>
<th>Fax</th>
</tr>
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<tbody>
<tr>
<td><strong>Northeast Area</strong></td>
<td>Xicor, Inc.</td>
<td>83 Cambridge Street, Unit 1D, Burlington, MA 01803</td>
<td>617/273-2110</td>
<td>230322889</td>
<td>617/273-3116</td>
</tr>
<tr>
<td><strong>Southeast Area</strong></td>
<td>Xicor, Inc.</td>
<td>201 Park Place, Suite 203, Altamonte Springs, FL 32701</td>
<td>407/767-8010</td>
<td>510-100-7141</td>
<td>407/767-8912</td>
</tr>
<tr>
<td><strong>Mid-Atlantic Area</strong></td>
<td>Xicor, Inc.</td>
<td>50 North Street, Danbury, CT 06810</td>
<td>203/743-1701</td>
<td>230853137</td>
<td>203/794-9501</td>
</tr>
<tr>
<td><strong>North Central Area</strong></td>
<td>Xicor, Inc.</td>
<td>953 North Plum Grove Road, Suite D, Schaumburg, IL 60173</td>
<td>312/605-1310</td>
<td>910-997-3663</td>
<td>312/605-1316</td>
</tr>
<tr>
<td><strong>South Central Area</strong></td>
<td>Xicor, Inc.</td>
<td>9330 Amberton Parkway, Suite 137, Dallas, TX 75243</td>
<td>214/669-2022</td>
<td>62027057</td>
<td>214/644-5835</td>
</tr>
<tr>
<td><strong>Southwest Area</strong></td>
<td>Xicor, Inc.</td>
<td>4141 MacArthur Boulevard, Suite 205, Newport Beach, CA 92660</td>
<td>714/752-8700</td>
<td>510-101-0110</td>
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<td>408/292-2011</td>
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#### International Sales Offices

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<tr>
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<th>Address</th>
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<tr>
<td><strong>Northern Europe Area</strong></td>
<td>Xicor Ltd.</td>
<td>Hawkins House, Carterton, Oxford OX8 3QA, United Kingdom</td>
<td>44.993.844.435</td>
<td>851838029</td>
<td>44.993.841.029</td>
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<tr>
<td><strong>Southern Europe Area</strong></td>
<td>Xicor GmbH</td>
<td>Technopark Neukeferloh, D-8011 Grasbrunn bei Muenchen, West Germany</td>
<td>(49) 89/ 463089</td>
<td>5213883</td>
<td>(49) 89/4605472</td>
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<tr>
<td><strong>Japan Area</strong></td>
<td>Xicor Japan K.K.</td>
<td>Suzuki Building, 4th Floor, 1-6-8 Shinjuku, Shinjuku-ku, Tokyo 160, Japan</td>
<td>(03) 225-2004</td>
<td>225-2319</td>
<td></td>
</tr>
<tr>
<td><strong>Far East Area</strong></td>
<td>Xicor, Inc.</td>
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<td>408/432-8888</td>
<td>910-379-0033</td>
<td>408/432-0640</td>
</tr>
</tbody>
</table>
TYPICAL FEATURES

- 3V–6V VCC Operation
- Low Power CMOS
  - 2 mA Active Current Typical
  - 60 μA Standby Current Typical
- Internally Organized as Two Pages
  - Each 256 x 8
- 2 Wire Serial Interface
- Provides Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- Inherent 100+ Years Data Retention
- 8-Pin Mini-DIP Package
- 14-Pin SOIC Package

DESCRIPTION

The X24LC04 is a CMOS 4096 bit serial E²PROM, internally organized as two 256 x 8 pages. The X24LC04 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance.
ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias
X24LC04 ........................................... -10°C to + 85°C
X24LC041 ............................................. -65°C to +135°C

Storage Temperature .................... - 65°C to + 150°C

Voltage on any Pin with
Respect to Vss ........................... -1.0V to + 7V
D.C. Output Current ..................... 5 mA

Lead Temperature
(Soldering, 10 Seconds) .................. 300°C

*COMMENT
Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS
X24LC04 TA = 0°C to + 70°C, VCC = + 3V to + 6V, unless otherwise specified.
X24LC041 TA = -40°C to + 85°C, VCC = + 3V to + 6V, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICc</td>
<td>Power Supply Current</td>
<td>Min.</td>
<td>Typ. (1)</td>
<td>Max.</td>
</tr>
<tr>
<td>ISB(2)</td>
<td>Standby Current VCC = 6V</td>
<td>2.0</td>
<td>3.0</td>
<td>150</td>
</tr>
<tr>
<td>ISB(2)</td>
<td>Standby Current VCC = 3V</td>
<td>0.1</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>IU</td>
<td>Input Leakage Current</td>
<td>0.1</td>
<td>10</td>
<td>150</td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td>0.4</td>
<td>10</td>
<td>150</td>
</tr>
<tr>
<td>VIL(3)</td>
<td>Input Low Voltage</td>
<td>- 1.0</td>
<td>VCC × 0.3</td>
<td>V</td>
</tr>
<tr>
<td>VIH(3)</td>
<td>Input High Voltage</td>
<td>VCC × 0.7</td>
<td>VCC + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>V</td>
<td>IOL = 3 mA</td>
</tr>
</tbody>
</table>

CAPACITANCE  T_A = 25°C, f = 1.0 MHz, VCC = 5V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ci/O(4)</td>
<td>Input/Output Capacitance (SDA)</td>
<td>8</td>
<td>pF</td>
<td>VIN = 0V</td>
</tr>
<tr>
<td>CIN(4)</td>
<td>Input Capacitance (A0, A1, A2, SCL)</td>
<td>6</td>
<td>pF</td>
<td>VIN = 0V</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>VCC × 0.1 to VCC × 0.9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>VCC × 0.5</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and CL = 100 pF</td>
</tr>
</tbody>
</table>

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) SDA and SCL require pull-up resistor.
(3) VIL min. and VIH max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM
| INPUTS | OUTPUTS |
|--------|---------|--------|
| | Must be steady | Will change steady |
| | May change from Low to High | Will change from Low to High |
| | May change from High to Low | Will change from High to Low |
| | Don't Care: Changes | State Not Allowed |
| | N/A | Center Line is High Impedance |
X24LC04, X24LC04I

A.C. CHARACTERISTICS LIMITS
X24LC04 TA = 0°C to +70°C, VCC = +3V to +6V, unless otherwise specified.
X24LC04I TA = −40°C to +85°C, VCC = +3V to +6V, unless otherwise specified.

Read & Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>fSCL</td>
<td>SCL Clock Frequency</td>
<td>0</td>
<td>100</td>
<td>KHz</td>
</tr>
<tr>
<td>T1</td>
<td>Noise Suppression Time</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tAA</td>
<td>SCL Low to SDA Data Out Valid</td>
<td>0.3</td>
<td>3.5</td>
<td>µs</td>
</tr>
<tr>
<td>tBUF</td>
<td>Time the Bus Must Be Free Before a New Transmission Can Start</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tHD:STA</td>
<td>Start Condition Hold Time</td>
<td>4.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tLOW</td>
<td>Clock Low Period</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tHIGH</td>
<td>Clock High Period</td>
<td>4.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tSU:STA</td>
<td>Start Condition Setup Time (for a Repeated Start Condition)</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tHD:DAT</td>
<td>Data In Hold Time</td>
<td>0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tSU:DAT</td>
<td>Data In Setup Time</td>
<td>250</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tR</td>
<td>SDA and SCL Rise Time</td>
<td>1</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tF</td>
<td>SDA and SCL Fall Time</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSU:STO</td>
<td>Stop Condition Setup Time</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tDH</td>
<td>Data Out Hold Time</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Typical Power-Up Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.(6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPUR(6)</td>
<td>Power-Up to Read Operation</td>
<td>2.0</td>
<td>µs</td>
</tr>
<tr>
<td>tPUW(6)</td>
<td>Power-Up to Write Operation</td>
<td>2.0</td>
<td>µs</td>
</tr>
</tbody>
</table>

Bus Timing

Notes: (5) Typical values are for TA = 25°C and nominal supply voltage.
(6) This parameter is periodically sampled and not 100% tested.
X24LC04, X24LC04I

Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(7)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tWR(8)</td>
<td>Write Cycle Time</td>
<td>10</td>
<td>5</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC04 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing

<table>
<thead>
<tr>
<th>SCL</th>
<th>-----</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDA</td>
<td>----</td>
</tr>
</tbody>
</table>

PIN DESCRIPTIONS

Serial Clock (SCL)
The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)
SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output implies the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

Address (A0)
A0 is unused by the X24LC04, however, it must be tied to VSS to insure proper device operation.

Address (A1, A2)
The Address inputs are used to set the least significant two bits of the six bit slave address. These inputs can be used static or driven. If used statically they must be tied to VSS or VCC as appropriate. If driven they must be driven by open collector outputs with resistor pull-ups to VCC.

DEVICE OPERATION

The X24LC04 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24LC04 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC04 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (7) Typical values are for TA = 25°C and nominal supply voltage (5V).
(8) tWR is the minimum cycle time from the system perspective; it is the maximum time the device requires to perform the internal write operation.
**X24LC04, X24LC04I**

**Figure 1: Data Validity**

```
SDA
SCL
DATA STABLE
DATA CHANGE
```

**Figure 2: Definition of Start and Stop**

```
SDA
SCL
START BIT
STOP BIT
```

**Stop Condition**

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC04 to place the device in the standby power mode.

**Acknowledge**

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC04 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24LC04 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24LC04 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24LC04 will continue to transmit data. If an acknowledge is not detected, the X24LC04 will terminate further data transmissions and await the stop condition to return to the standby power mode.
DEVICE ADDRESSING
Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24LC04 this is fixed as 1010[B].

Figure 4: Slave Address

The next two significant bits address a particular device. A system could have up to four X24LC04 devices on the bus (see Figure 10). The four addresses are defined by the state of the A1 and A2 inputs.

The next bit of the slave address field (bit 1) is the page select bit. It is used by the host to toggle between the two 256 word pages of memory. This is, in effect the most significant bit for the word address.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Following the start condition, the X24LC04 monitors the SDA bus comparing the slave address being transmitted with its address (device type and state of A1 and A2 inputs). Upon a compare the X24LC04 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24LC04 will execute a read or write operation.

WRITE OPERATIONS

Byte Write
For a write operation, the X24LC04 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24LC04 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24LC04 begins the internal write cycle to the non-volatile memory. While the internal write cycle is in progress the X24LC04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.
Page Write

The X24LC04 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24LC04 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC04 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24LC04 is still busy with the write operation no ACK will be returned. If the X24LC04 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Note: For each read operation, SDA must be brought back to a high level prior to the stop bit.

Current Address Read

Internally the X24LC04 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/W set to one, the X24LC04 issues an acknowledge and transmits the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X24LC04 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.
Random Read
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24LC04 and then by the eight bit word. The master does not acknowledge the transfer but does generate the stop condition and the X24LC04 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read
Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24LC04 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. If more than 512 words are read, the counter “rolls over” and the X24LC04 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.
Figure 9: Sequential Read

BUS ACTIVITY: MASTER
SDA LINE
BUS ACTIVITY: SLAVE ADDRESS

Figure 10: Typical System Configuration

FUNCTIONAL DIAGRAM

(8) VCC
(4) VSS
(5) SDA
(6) SCL
(3) A7
(2) A6
(1) A5
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

\[ R_{\text{MIN}} = \frac{V_{CC \text{ MAX}}}{I_{DL \text{ MIN}}} = 1.8 \, \text{K}\Omega \]

\[ R_{\text{MAX}} = \frac{t_{\text{RISE}}}{C_{\text{BUS}}} \]

MIN. RESISTANCE

MAX. RESISTANCE

BUS CAPACITANCE (pF)
# ORDERING INFORMATION

## SERIAL E2PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X24LC04S</td>
<td>512 x 8</td>
<td>•</td>
<td>†</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC04SI</td>
<td>512 x 8</td>
<td>•</td>
<td>I</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC04P</td>
<td>512 x 8</td>
<td>•</td>
<td>†</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC04PI</td>
<td>512 x 8</td>
<td>•</td>
<td>I</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC04D</td>
<td>512 x 8</td>
<td>•</td>
<td>†</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC04DI</td>
<td>512 x 8</td>
<td>•</td>
<td>I</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

Key:
- † = Blank = Commercial = 0°C to + 70°C
- I = Industrial = −40°C to + 85°C
- M = Military = −55°C to + 125°C

- S = 14-Lead Plastic Small Outline Gull Wing
- P = 8-Lead Plastic DIP
- D = 8-Lead Ceramic DIP
- C = Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
- F2 = Ceramic Flat Pack for X28C256 and X28C256B
- K = Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

## LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

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## U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,688,932; 4,752,912. Foreign patents and additional patents pending.

## LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
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TWX: 910-379-0033
Fax: 408/432-0640
PRELIMINARY INFORMATION

16K Commercial X24LC16
Industrial X24LC16I
2048 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES
• 3V–6V VCC Operation
• Low Power CMOS
  —2 mA Active Current Typical
  —60 µA Standby Current Typical
• Internally Organized as Eight Pages
  —Each 256 x 8
• 2 Wire Serial Interface
• Provides Bidirectional Data Transfer Protocol
• Sixteen Byte Page Write Mode
  —Minimizes Total Write Time Per Byte
• Self Timed Write Cycle
  —Typical Write Cycle Time of 5 ms
• Inherent 100+ Years Data Retention
• 8-Pin Mini-DIP Package
• 14-Pin SOIC Package

DESCRIPTION
The X24LC16 is a CMOS 16,384 bit serial E2PROM, internally organized as eight 256 x 8 pages. The X24LC16 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E2PROMs are designed and tested for applications requiring extended endurance.

PIN CONFIGURATIONS

PLASTIC CERDIP

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>YSS</th>
<th>VSS</th>
<th>NC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>8</td>
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</table>

CERDIP

<table>
<thead>
<tr>
<th>VCC</th>
<th>TEST</th>
<th>SCL</th>
<th>SDA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
<td>6</td>
<td>5</td>
</tr>
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</table>

X24LC16

SOIC

<table>
<thead>
<tr>
<th>NC</th>
<th>1</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>A1</td>
<td>A2</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>5</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>X24LC16</th>
<th>4</th>
<th>11</th>
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<tbody>
<tr>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VSS</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td>8</td>
</tr>
</tbody>
</table>

PIN NAMES

<table>
<thead>
<tr>
<th>A0–A2</th>
<th>Address Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDA</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SCL</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>TEST</td>
<td>Hold at VSS</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>VCC</td>
<td>+3V to +6V</td>
</tr>
<tr>
<td>NC</td>
<td>No Connect</td>
</tr>
</tbody>
</table>

Characteristics subject to change without notice
X24LC16, X24LC161

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias
- X24LC16: -10°C to +85°C
- X24LC161: -65°C to +135°C

Storage Temperature
- X24LC16: -65°C to +150°C
- X24LC161: -65°C to +150°C

Voltage on any Pin with Respect to VSS
- X24LC16: -1.0V to +7V
- X24LC161: -1.0V to +7V

D.C. Output Current
- X24LC16: 5 mA
- X24LC161: 5 mA

Lead Temperature (Soldering, 10 Seconds)
- X24LC16: 300°C
- X24LC161: 300°C

**D.C. OPERATING CHARACTERISTICS**

X24LC16 TA = 0°C to +70°C, VCC = +3V to +6V, unless otherwise specified.
X24LC161 TA = -40°C to +85°C, VCC = +3V to +6V, unless otherwise specified.

### Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(1)</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td>Power Supply Current</td>
<td>2.0</td>
<td>3.0</td>
<td>mA</td>
<td>ISCL = 100 KHz</td>
<td></td>
</tr>
<tr>
<td>ISB(2)</td>
<td>Standby Current VCC = 6V</td>
<td>150</td>
<td>µA</td>
<td>VIN = GND or VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISB(2)</td>
<td>Standby Current VCC = 3V</td>
<td>50</td>
<td>µA</td>
<td>VIN = GND or VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Input Leakage Current</td>
<td>0.1</td>
<td>10</td>
<td>µA</td>
<td>VIN = GND to VCC</td>
<td></td>
</tr>
<tr>
<td>LO</td>
<td>Output Leakage Current</td>
<td>0.1</td>
<td>10</td>
<td>µA</td>
<td>VOUT = GND to VCC</td>
<td></td>
</tr>
<tr>
<td>VL(3)</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td>VCC × 0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VH(3)</td>
<td>Input High Voltage</td>
<td>VCC × 0.7</td>
<td>VCC + 0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>V</td>
<td>IOL = 3 mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Capacitance

TA = 25°C, f = 1.0 MHz, VCC = 5V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIO(4)</td>
<td>Input/Output Capacitance (SDA)</td>
<td>8</td>
<td>pF</td>
<td>VIO = 0V</td>
</tr>
<tr>
<td>CIN(4)</td>
<td>Input Capacitance (A0, A1, A2, SCL)</td>
<td>6</td>
<td>pF</td>
<td>VIN = 0V</td>
</tr>
</tbody>
</table>

### A.C. CONDITIONS OF TEST

| Input Pulse Levels | VCC × 0.1 to VCC × 0.9 |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Levels | VCC × 0.5 |
| Output Load | 1 TTL Gate and CL = 100 pF |

**Notes:**

1. Typical values are for TA = 25°C and nominal supply voltage.
2. SDA and SCL require pull-up resistor.
3. \( V_{IL} \) min. and \( V_{IH} \) max. are for reference only and are not tested.
4. This parameter is periodically sampled and not 100% tested.

**COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
X24LC16, X24LC16I

A.C. CHARACTERISTICS LIMITS
X24LC16 T\textsubscript{A} = 0°C to +70°C, \( V_{CC} = +3V \) to +6V, unless otherwise specified.
X24LC16I T\textsubscript{A} = -40°C to +85°C, \( V_{CC} = +3V \) to +6V, unless otherwise specified.

Read & Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>f\textsubscript{SCL}</td>
<td>SCL Clock Frequency</td>
<td>0</td>
<td>100</td>
<td>KHz</td>
</tr>
<tr>
<td>T\textsubscript{I}</td>
<td>Noise Suppression Time</td>
<td></td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{AA}</td>
<td>SCL Low to SDA Data Out Valid</td>
<td>0.3</td>
<td>3.5</td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{BUF}</td>
<td>Time the Bus Must Be Free Before a New Transmission Can Start</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{HD:STA}</td>
<td>Start Condition Hold Time</td>
<td>4.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{LOW}</td>
<td>Clock Low Period</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{HIGH}</td>
<td>Clock High Period</td>
<td>4.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{SU:STA}</td>
<td>Start Condition Setup Time (for a Repeated Start Condition)</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{HD:DAT}</td>
<td>Data In Hold Time</td>
<td>0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{SU:DAT}</td>
<td>Data In Setup Time</td>
<td>250</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{R}</td>
<td>SDA and SCL Rise Time</td>
<td>1</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{F}</td>
<td>SDA and SCL Fall Time</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{SU:STO}</td>
<td>Stop Condition Setup Time</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{DH}</td>
<td>Data Out Hold Time</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Typical Power-Up Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.(5)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsubscript{PUR}(6)</td>
<td>Power-Up to Read Operation</td>
<td>2.0</td>
<td>µs</td>
</tr>
<tr>
<td>t\textsubscript{PUW}(6)</td>
<td>Power-Up to Write Operation</td>
<td>2.0</td>
<td>µs</td>
</tr>
</tbody>
</table>

Bus Timing

Notes: (5) Typical values are for T\textsubscript{A} = 25°C and nominal supply voltage.
(6) This parameter is periodically sampled and not 100% tested.
X24LC16, X24LC16I

Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ. (7)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tWR(8)</td>
<td>Write Cycle Time</td>
<td>10</td>
<td>5</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC16 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing

PIN DESCRIPTIONS

Serial Clock (SCL)
The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)
SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output implies the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

Address (A0, A1, A2)
The A0, A1 and A2 inputs are unused by the X24LC16, however, they must be tied to VSS to insure proper device operation.

DEVICE OPERATION

The X24LC16 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24LC16 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC16 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes:
(7) Typical values are for TA = 25°C and nominal supply voltage (5V).
(8) tWR is the minimum cycle time from the system perspective; it is the maximum time the device requires to perform the internal write operation.
Stop Condition
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC16 to place the device in the standby power mode.

Acknowledge
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC16 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24LC16 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24LC16 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24LC16 will continue to transmit data. If an acknowledge is not detected, the X24LC16 will terminate further data transmissions and await the stop condition to return to the standby power mode.
DEVICE ADDRESSING
Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24LC16 this is fixed as 1010[B].

Figure 4: Slave Address

The next three bits of the slave address field are the page select bits. They are used by the master device to select which of the eight 256 word pages of memory are to be accessed. These bits are, in effect, the three most significant bits of the word address. It should be noted, the protocol limits the size of memory to eight pages of 256 words; therefore, the protocol can support only one X24LC16 per system.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Following the start condition, the X24LC16 monitors the SDA bus comparing the slave address being transmitted with its slave address. Upon a compare the X24LC16 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24LC16 will execute a read or write operation.

WRITE OPERATIONS
Byte Write
For a write operation, the X24LC16 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the X24LC16 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24LC16 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24LC16 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.
Page Write

The X24LC16 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24LC16 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order seven bits of the word address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC16 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24LC16 is still busy with the write operation no ACK will be returned. If the X24LC16 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Note: For each read operation, SDA must be brought back to a high level prior to the stop bit.

Current Address Read

Internally the X24LC16 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/W set to one, the X24LC16 issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition and the X24LC16 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.
Random Read
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24LC16 and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition and the X24LC16 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read
Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24LC16 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. If more than 2048 words are read, the counter "rolls over" and the X24LC16 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.
Figure 9: Sequential Read

**BUS ACTIVITY:**
- **MASTER**
  - **SLAVE ADDRESS:**
  - **SDA LINE:**
    - A
    - C
    - K
    - DATA n
    - DATA n + 1
    - DATA n + 2
    - DATA n + x

**BUS ACTIVITY:**
- **X24LC16**
  - **SDA LINE:**
    - K
    - ~K
    - P

Figure 10: Typical System Configuration

**FUNCTIONAL DIAGRAM**

- **(8) Vcc**
- **(4) Vss**
- **(5) SDA**
  - **START STOP LOGIC**
  - **SLAVE ADDRESS REGISTER + COMPARATOR**
  - **CONTROL LOGIC**
    - **WORD ADDRESS COUNTER**
      - **LOAD**
      - **INC**
    - **START CYCLE**
  - **H.V. GENERATION TIMING & CONTROL**
  - **E'PROM 256 x 64**
  - **YDEC**
    - **3**
    - **64**
  - **DATA REGISTER**
    - **8**
    - **DOUT**
    - **ACK**
    - **PIN**
    - **CK**
    - **R/W**
    - **5**
    - **3**
  - **MASTER TRANSMITTER/ RECEIVER**
  - **SLAVE TRANSMITTER/ RECEIVER**
  - **SLAVE RECEIVER**
  - **START CYCLE**
  - **MASTER TRANSMITTER/ RECEIVER**
    - **LOAD**
    - **INC**
  - **H.V. GENERATION TIMING & CONTROL**

0105-13
0105-14
0105-15
Guidelines for Calculating Typical Values of
Bus Pull-Up Resistors

\[
R_{\text{MIN}} = \frac{V_{\text{CC MAX}}}{I_{OL \text{ MIN}}} = 1.8 \text{ k}\Omega
\]

\[
R_{\text{MAX}} = \frac{t_{\text{RISE}}}{C_{\text{BUS}}}
\]

MIN.
RResistance

BUS CAPACITANCE (pF)

RESISTANCE (k\Omega)

0 20 40 60 80 100 120

Vee MAX

RMIN = IOL MIN

0105-16
## ORDERING INFORMATION

### SERIAL E²PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X24LC16S</td>
<td>2048 x 8</td>
<td>•</td>
<td></td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC16SI</td>
<td>2048 x 8</td>
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<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC16P</td>
<td>2048 x 8</td>
<td>•</td>
<td></td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC16PI</td>
<td>2048 x 8</td>
<td>•</td>
<td></td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC16D</td>
<td>2048 x 8</td>
<td>•</td>
<td></td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X24LC16DI</td>
<td>2048 x 8</td>
<td>•</td>
<td></td>
<td>CMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

**Key:**
- † = Blank = Commercial = 0°C to + 70°C
- I = Industrial = -40°C to + 85°C
- M = Military = -55°C to +125°C

- S = 14-Lead Plastic Small Outline Gull Wing
- P = 8-Lead Plastic DIP
- D = 8-Lead Cerdip
- C = Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
- F2 = Ceramic Flat Pack for X28C256 and X28C256B
- K = Ceramic Pin Grid Array
- J = J-Hook Plastic Lead Chip Carrier
- E = Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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### LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
# Sales Offices

## U.S. Sales Offices

### Northeast Area
Xicor, Inc.  
83 Cambridge Street  
Unit 1D  
Burlington, Massachusetts 01803  
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### Southeast Area
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### Mid-Atlantic Area
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### North Central Area
Xicor, Inc.  
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Fax: 312/605-1316

### South Central Area
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Fax: 214/644-5835

### Southwest Area
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TWX: 510-101-0110  
Fax: 714/752-8634

### Northwest Area
Xicor, Inc.  
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Milpitas, California 95035  
Phone: 408/292-2011  
TWX: 910-379-0033  
Fax: 408/432-0640

## International Sales Offices

### Northern Europe Area
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### Japan Area
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Xicor, Inc.  
851 Buckeye Court  
Milpitas, California 95035  
USA  
Phone: 408/432-8888  
TWX: 910-379-0033  
Fax: 408/432-0640
Please use this Xicor Data Book Supplement in conjunction with the Xicor 1988 Data Book, Stock No. 100-080, which contains additional product line information, product reliability reports and application notes.
FEATURES

• 200 ns Access Time
• High Performance Advanced NMOS Technology
• Fast Write Cycle Times
  —16-Byte Page Write Operation
  —Byte or Page Write Cycle: 5 ms Typical
  —Complete Memory Rewrite: 640 ms Typical
• Effective Byte Write Cycle Time of 300 µs Typical
• DATA Polling
  —Allows User to Minimize Write Cycle Time
• Simple Byte and Page Write
  —Single TTL Level WE Signal
  —Internally Latched Address and Data
  —Automatic Write Timing
• JEDEC Approved Byte-Wide Pinout
• Inherent 100+ Years Data Retention

DESCRIPTION

The Xicor X2816C is a 2K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2816C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2816C supports a 16-byte page write operation, typically providing a 300 µs/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816C also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance.
**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias
- **X2816C**: -10°C to +85°C
- **X2816CI**: 65°C to +135°C

Storage Temperature: -65°C to +150°C

D.C. Output Current: ≤ 5 mA

Lead Temperature (Soldering, 10 Seconds): 300°C

D.C. OPERATING CHARACTERISTICS

**X2816C**
- $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V ± 10%$, unless otherwise specified.

**X2816CI**
- $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V ± 10%$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CC}$</td>
<td>$V_{CC}$ Current (Active)</td>
<td>Min. 80 Typ. 120 Max. mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SB}$</td>
<td>$V_{CC}$ Current (Standby)</td>
<td>Min. 45 Typ. 60 Max. mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Current</td>
<td>Min. 10 Typ. 10 Max. µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LO}$</td>
<td>Output Leakage Current</td>
<td>Min. 10 Typ. 10 Max. µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>Min. -1.0 Typ. 0.8 Max. V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>Min. 2.0 Typ. $V_{CC} + 1.0$ Max. V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>Min. 0.4 Typ. Max. V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>Min. 2.4 Typ. Max. V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TYPICAL POWER-UP TIMING**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ. (1)</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{puR}$</td>
<td>Power-Up to Read Operation</td>
<td>1 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{puW}$</td>
<td>Power-Up to Write Operation</td>
<td>5 ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CAPACITANCE**  
$T_A = 25°C$, $f = 1.0$ MHz, $V_{CC} = 5V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{i/o}$</td>
<td>Input/Output Capacitance</td>
<td>10 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{in}$</td>
<td>Input Capacitance</td>
<td>6 pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**A.C. CONDITIONS OF TEST**

<table>
<thead>
<tr>
<th>Mode Selection</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>$CE$</td>
<td>$OE$</td>
<td>$WE$</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
</tr>
</tbody>
</table>

**Notes:**
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.
3. This parameter is periodically sampled and not 100% tested.
### A.C. Characteristics

$X2816C$ $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V ± 10\%$, unless otherwise specified.

$X2816CI$ $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V ± 10\%$, unless otherwise specified.

#### Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{RC}$</td>
<td>Read Cycle Time</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CE}$</td>
<td>Chip Enable Access Time</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AA}$</td>
<td>Address Access Time</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OE}$</td>
<td>Output Enable Access Time</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{LZ}^{(4)}$</td>
<td>Chip Enable to Output in Low Z</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HZ}^{(5)}$</td>
<td>Chip Disable to Output in High Z</td>
<td>10</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OLZ}^{(4)}$</td>
<td>Output Enable to Output in Low Z</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OHZ}^{(6)}$</td>
<td>Output Disable to Output in High Z</td>
<td>10</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OH}$</td>
<td>Output Hold from Address Change</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

#### Read Cycle

![Read Cycle Diagram](image)

**Notes:**

1. $t_{LZ}$ min. and $t_{OLZ}$ min. are periodically sampled and not 100% tested.
2. $t_{HZ}$ max. and $t_{OHZ}$ max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. $t_{HZ}$ min. and $t_{OHZ}$ min. are periodically sampled and not 100% tested.
### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(6)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{WC}(^7)$</td>
<td>Write Cycle Time</td>
<td>5</td>
<td>10</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{AS}$</td>
<td>Address Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AH}$</td>
<td>Address Hold Time</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CS}$</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CH}$</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CW}$</td>
<td>OE Pulse Width</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OES}$</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OEH}$</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WP}$</td>
<td>WE Pulse Width</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WP}$</td>
<td>WE High Recovery</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DV}$</td>
<td>Data Valid</td>
<td>300</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DS}$</td>
<td>Data Setup</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>Data Hold</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DW}$</td>
<td>Delay to Next Write</td>
<td>500</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{BLC}$</td>
<td>Byte Load Cycle</td>
<td>3</td>
<td>20</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

### WE Controlled Write Cycle

![WE Controlled Write Cycle Diagram]

**Notes:**

(6) Typical values are for $T_A = 25°C$ and nominal supply voltage.

(7) $t_{WC}$ is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.


**CE Controlled Write Cycle**

![Diagram of CE Controlled Write Cycle]

**Page Mode Write Cycle**

![Diagram of Page Mode Write Cycle]

---

**Notes:**

(8) Between successive byte writes within a page write operation, OE can be strobed LOW; e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram

Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

SYMBOL TABLE

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td></td>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td></td>
<td>N/A</td>
<td>Center Line is High Impedance</td>
</tr>
</tbody>
</table>
PIN DESCRIPTIONS

Addresses (A0–A10)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O0–I/O7)
Data is written to or read from the X2816C through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X2816C.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X2816C supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X2816C allows the entire memory to be typically written in 640 ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816C prior to the commencement of the internal programming cycle. Although the host system may read data from any location in the system to transfer to the X2816C, the destination page address of the X2816C should be the same on each subsequent strobe of the WE and CE inputs. That is, A4 through A10 must be the same for each transfer of data to the X2816C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 20 µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 20 µs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20 µs.

DATA Polling
The X2816C features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X2816C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O7 will reflect true data.

WRITE PROTECTION
There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A WE pulse which is typically less than 20 ns will not initiate a write cycle.
- VCC Sense—All functions are inhibited when VCC is ≤3V, typically.
- Write Inhibit—Holding either OE LOW, WE HIGH or CE HIGH during power-on and power-off, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

ENDURANCE
Xicor E2PROMs are designed and tested for applications requiring extended endurance.
SYSTEM CONSIDERATIONS

Because the X2816C is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that OE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2816C has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM
X2816C, X2816CI

Normalized Active Supply Current vs. Ambient Temperature

![Normalized Active Supply Current Graph](image)

Normalized Standby Supply Current vs. Ambient Temperature

![Normalized Standby Supply Current Graph](image)

Normalized Access Time vs. Ambient Temperature

![Normalized Access Time Graph](image)
X2816C, X2816CI

ORDERING INFORMATION
16K E2PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X2816CP-20</td>
<td>2048 x 8</td>
<td>P</td>
<td>†</td>
<td>200 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2816CPl-20</td>
<td>2048 x 8</td>
<td>P</td>
<td>†</td>
<td>200 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2816CJ-20</td>
<td>2048 x 8</td>
<td>P</td>
<td>†</td>
<td>200 ns</td>
<td>NMOS</td>
<td>Standard</td>
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<tr>
<td>X2816CJI-20</td>
<td>2048 x 8</td>
<td>P</td>
<td>†</td>
<td>200 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

Key:
† = Blank = Commercial = 0°C to + 70°C
I = Industrial = -40°C to +85°C
M = Military = -55°C to +125°C
S = Plastic Small Outline Gull Wing
P = 24-Lead Plastic DIP
D = Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor’s products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY
### U.S. Sales Offices

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64K Commercial
Industrial
X2864B
X2864BI
8192 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

• 120 ns Access Time
• High Performance Scaled NMOS Technology
• Fast Write Cycle Times
  —32-Byte Page Write Operation
  —Byte or Page Write Cycle: 3 ms Typical
  —Complete Memory Rewrite: 750 ms Typical
  —Effective Byte Write Cycle Time of 95 μs Typical
• DATA Polling
  —Allows User to Minimize Write Cycle Time
• Simple Byte and Page Write
  —Single TTL Level WE Signal
  —Internally Latched Address and Data
  —Automatic Write Timing
• JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X2864B is a 8K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864B supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

PIN CONFIGURATIONS

<table>
<thead>
<tr>
<th>PLASTIC</th>
<th>CERDIP</th>
<th>FLAT PACK</th>
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<tbody>
<tr>
<td>NC</td>
<td>1</td>
<td>29</td>
</tr>
<tr>
<td>A2</td>
<td>2</td>
<td>27</td>
</tr>
<tr>
<td>A7</td>
<td>3</td>
<td>26</td>
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<tr>
<td>A6</td>
<td>4</td>
<td>25</td>
</tr>
<tr>
<td>A5</td>
<td>5</td>
<td>24</td>
</tr>
<tr>
<td>A4</td>
<td>6</td>
<td>23</td>
</tr>
<tr>
<td>A3</td>
<td>7</td>
<td>22</td>
</tr>
<tr>
<td>A2</td>
<td>8</td>
<td>21</td>
</tr>
<tr>
<td>A1</td>
<td>9</td>
<td>20</td>
</tr>
<tr>
<td>A0</td>
<td>10</td>
<td>19</td>
</tr>
<tr>
<td>I/O3</td>
<td>11</td>
<td>18</td>
</tr>
<tr>
<td>I/O1</td>
<td>12</td>
<td>17</td>
</tr>
<tr>
<td>I/O2</td>
<td>13</td>
<td>16</td>
</tr>
<tr>
<td>VSS</td>
<td>14</td>
<td>15</td>
</tr>
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<table>
<thead>
<tr>
<th>PLCC</th>
<th>LCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>VCC</td>
<td>VCC</td>
</tr>
<tr>
<td>WE</td>
<td>NC</td>
</tr>
<tr>
<td>A0</td>
<td>A0</td>
</tr>
<tr>
<td>A1</td>
<td>A1</td>
</tr>
<tr>
<td>A2</td>
<td>A2</td>
</tr>
<tr>
<td>A3</td>
<td>A3</td>
</tr>
<tr>
<td>A4</td>
<td>A4</td>
</tr>
<tr>
<td>A5</td>
<td>A5</td>
</tr>
<tr>
<td>A6</td>
<td>A6</td>
</tr>
<tr>
<td>A7</td>
<td>A7</td>
</tr>
<tr>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>WE</td>
<td>WE</td>
</tr>
<tr>
<td>VCC</td>
<td>VCC</td>
</tr>
<tr>
<td>VSS</td>
<td>VSS</td>
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<table>
<thead>
<tr>
<th>X2864B (TOP VIEW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
</tr>
<tr>
<td>VCC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN NAMES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0–A12</td>
</tr>
<tr>
<td>I/O0–I/O7</td>
</tr>
<tr>
<td>WE</td>
</tr>
<tr>
<td>CE</td>
</tr>
<tr>
<td>OE</td>
</tr>
<tr>
<td>VCC</td>
</tr>
<tr>
<td>VSS</td>
</tr>
<tr>
<td>NC</td>
</tr>
</tbody>
</table>

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Characteristics subject to change without notice
X2864B, X2864BI

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Temperature Under Bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>X2864B</td>
</tr>
<tr>
<td>X2864BI</td>
</tr>
<tr>
<td>Storage Temperature</td>
</tr>
</tbody>
</table>

Voltage on any Pin with Respect to Ground: -1.0V to +7V

D.C. Output Current: 5 mA

Lead Temperature (Soldering, 10 Seconds): 300°C

**COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. OPERATING CHARACTERISTICS**

X2864B $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified.

X2864BI $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

**Symbol** | **Parameter** | **Limits** | **Units** | **Test Conditions**
--- | --- | --- | --- | ---

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(1)</th>
<th>Max.</th>
<th>CE = OE = $V_{IL}$</th>
<th>( CE = V_{IH}, OE = V_{IL} )</th>
<th>All I/O's = Open</th>
<th>Other Inputs = $V_{CC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CC}$</td>
<td>$V_{CC}$ Current (Active)</td>
<td>80</td>
<td>150</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SB}$</td>
<td>$V_{CC}$ Current (Standby)</td>
<td>50</td>
<td>80</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Current</td>
<td>10</td>
<td></td>
<td>μA</td>
<td>$V_{IN} = GND$ to $V_{CC}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LO}$</td>
<td>Output Leakage Current</td>
<td>10</td>
<td></td>
<td>μA</td>
<td>$V_{OUT} = GND$ to $V_{CC}, CE = V_{IH}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td></td>
<td>-1.0</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td></td>
<td>2.0</td>
<td>$V_{CC} + 1.0$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td>$I_{OL} = 2.1 \text{ mA}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td></td>
<td>2.4</td>
<td>V</td>
<td>$I_{OH} = -400 \mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TYPICAL POWER-UP TIMING**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.(3)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PUR}$</td>
<td>Power-Up to Read Operation</td>
<td>1</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{PULW}$</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

**CAPACITANCE** $T_A = 25°C$, $f = 1.0$ MHz, $V_{CC} = 5V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{I/O}$</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td>pF</td>
<td>$V_{I/O} = 0V$</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>6</td>
<td>pF</td>
<td>$V_{IN} = 0V$</td>
</tr>
</tbody>
</table>

**A.C. CONDITIONS OF TEST**

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>0.4V to 2.4V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>0.8V and 2.0V</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and $C_L = 100 \text{ pF}$</td>
</tr>
</tbody>
</table>

**MODE SELECTION**

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>$D_{OUT}$</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>$D_{IN}$</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Notes:**

1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.
3. This parameter is periodically sampled and not 100% tested.
X2864B, X2864BI

A.C. CHARACTERISTICS
X2864B $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified.
X2864BI $T_A = -40^\circ C$ to $+85^\circ C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X2864B-12</th>
<th>X2864BI-12</th>
<th>X2864B-15</th>
<th>X2864BI-15</th>
<th>X2864B-18</th>
<th>X2864BI-18</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RC}$</td>
<td>Read Cycle Time</td>
<td>120</td>
<td>150</td>
<td>180</td>
<td>180</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{CE}$</td>
<td>Chip Enable Access Time</td>
<td>120</td>
<td>150</td>
<td>180</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AA}$</td>
<td>Address Access Time</td>
<td>120</td>
<td>150</td>
<td>180</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OE}$</td>
<td>Output Enable Access Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>70</td>
</tr>
<tr>
<td>$t_{LZ}(4)$</td>
<td>$OE$ Low to Active Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OLZ}(4)$</td>
<td>$OE$ Low to Active Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HZ}(5)$</td>
<td>$CE$ High to High Z Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OHZ}(5)$</td>
<td>$OE$ High to High Z Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OH}$</td>
<td>Output Hold from Address Change</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Read Cycle

Notes:
(4) $t_{LZ}$ min. and $t_{OLZ}$ min. are shown for reference only, they are periodically characterized and are not tested.
(5) $t_{HZ}$ max. and $t_{OHZ}$ max. are measured from the point when $CE$ or $OE$ return high (whichever occurs first) to the time when the outputs are no longer driven. $t_{HZ}$ min. and $t_{OHZ}$ min. are shown for reference only, they are periodically characterized and are not tested.
## Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.,(6)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{WC}</td>
<td>Write Cycle Time</td>
<td>3</td>
<td>5</td>
<td>5</td>
<td>ms</td>
</tr>
<tr>
<td>t_{AS}</td>
<td>Address Setup Time</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{AH}</td>
<td>Address Hold Time</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CS}</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CH}</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CW}</td>
<td>OE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{OES}</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{OEH}</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{WP}</td>
<td>WE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{WPH}</td>
<td>WE High Recovery</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{DV}</td>
<td>Data Valid</td>
<td></td>
<td>100</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>t_{DS}</td>
<td>Data Setup</td>
<td>50</td>
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<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{DH}</td>
<td>Data Hold</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{DW}</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>t_{BLC}</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td>100</td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

### WE Controlled Write Cycle

![Diagram of WE Controlled Write Cycle](image)

**Note:** (6) Typical values are for \( T_A = 25^\circ C \) and nominal supply voltage.
**CE Controlled Write Cycle**

![Diagram of CE Controlled Write Cycle]

**Page Mode Write Cycle**

![Diagram of Page Mode Write Cycle]

Notes:

1. Between successive byte writes within a page write operation, CE can be strobed LOW; e.g., this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

2. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram(9)

**Symbol Table**

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td></td>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Center Line is High Impedance</td>
</tr>
<tr>
<td></td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS

Addresses (A₀–A₁₂)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O₀–I/O₇)
Data is written to or read from the X2864B through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X2864B.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X2864B supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation
The page write feature of the X2864B allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864B prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A₅ through A₁₂ must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 µs the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide so long as the host continues to access the device within the byte load cycle time of 100 µs.

DATA Polling
The X2864B features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X2864B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₇ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O₇ will reflect true data.

WRITE PROTECTION
There are two features that protect the nonvolatile data from inadvertent writes.

• VCC Sense—All functions are inhibited when VCC is ≤3.5V.

• Write Inhibit—Holding either OE LOW, WE HIGH or CE HIGH during power-on and power-off, will inhibit inadvertent writes.
SYSTEM CONSIDERATIONS
Because the X2864B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 \mu F high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 \mu F electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.
# Ordering Information

## 64K EPROMs

<table>
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<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
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**Key:**

† = Blank = Commercial = 0°C to +70°C  
I = Industrial = -40°C to +85°C  
M = Military = -55°C to +125°C  
T = Ultra High Temp. = 0°C to +150°C  
S = Plastic Small Outline Gull Wing  
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E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)  
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
### ORDERING INFORMATION

#### 64K E2PROMs (Continued)

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**LIMITED WARRANTY**

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

**U.S. PATENTS**

Xicor products are covered by one or more of the following U.S. Patents: 4,283,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,466,769; 4,468,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932. Foreign patents and additional patents pending.

**LIFE RELATED POLICY**

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F1

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NL ± 0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

CGG032
Sales Offices

U.S. Sales Offices

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Fax: 312/490-0637

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Telex: 62027057
Fax: 214/644-5835

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TWX: 510-101-0110
Fax: 714/752-8634

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Milpitas, California 95035
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TWX: 910-379-0033
Fax: 408/432-0640

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Carterton
Oxford 0X8 3QA
United Kingdom
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Telex: 851838029
Fax: 44.993.841.029

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Xicor, GmbH
Forstausstrasse 1
D8013 Haar bei Muenchen
West Germany
Phone: 49.8946.3089
Telex: 8415213883
Fax: 49.89.460.5472

Far East Area
Xicor, Inc.
851 Buckeye Court
Milpitas, California 95035
USA
Phone: 408/432-8888
TWX: 910-379-0033
Fax: 408/432-0640
TYPICAL FEATURES
• 120 ns Access Time
• High Performance Scaled NMOS Technology
• Fast Write Cycle Times
  —32-Byte Page Write Operation
  —Byte or Page Write Cycle: 3 ms Typical
  —Complete Memory Rewrite: 750 ms Typical
  —Effective Byte Write Cycle Time of 95 µs Typical
• DATA Polling
  — Allows User to Minimize Write Cycle Time
• Simple Byte and Page Write
  — Single TTL Level WE Signal
  — Internally Latched Address and Data
• Automatic Write Timing
• JEDEC Approved Byte-Wide Pinout

DESCRIPTION
The Xicor X2864B is an 8K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864B supports a 32-byte page write operation, effectively providing a 95 µs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.
ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .................................. -65°C to +135°C
Storage Temperature .................................. -65°C to +150°C
Voltage on any Pin with Respect to Ground .......... -1.0V to +7V
D.C. Output Current .................................. 5 mA
Lead Temperature (Soldering, 10 Seconds) .......... 300°C

D.C. OPERATING CHARACTERISTICS

T_A = -55°C to +125°C, V_CC = +5V ±10%, unless otherwise specified.

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<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
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<td>Typical</td>
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<td></td>
</tr>
<tr>
<td>I_O</td>
<td>Output Leakage Current</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>V_L</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td></td>
<td>0.8</td>
</tr>
<tr>
<td>V_H</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>V_CC + 1.0</td>
<td></td>
</tr>
<tr>
<td>V_O</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_OH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td></td>
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TYPICAL POWER-UP TIMING

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.(1)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_puR</td>
<td>Power-Up to Read Operation</td>
<td>1</td>
<td>ms</td>
</tr>
<tr>
<td>t_puw</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

CAPACITANCE

TA = 25°C, f = 1.0 MHz, V_CC = 5V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/I/O</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td>pF</td>
<td>V_I/O = 0V</td>
</tr>
<tr>
<td>C/IN</td>
<td>Input Capacitance</td>
<td>6</td>
<td>pF</td>
<td>V_IN = 0V</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>0.4V to 2.4V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>0.8V and 2.0V</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and C_L = 100 pF</td>
</tr>
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MODE SELECTION

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>D_OUT</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>D_IN</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. V_IL min. and V_IH max. are for reference only and are not tested.
3. This parameter is periodically sampled and not 100% tested.
A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

### Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X2864BM-12</th>
<th>X2864BM-15</th>
<th>X2864BM-18</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
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<tr>
<td>$t_{RC}$</td>
<td>Read Cycle Time</td>
<td>120</td>
<td>150</td>
<td>180</td>
<td>ns</td>
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<tr>
<td>$t_{CE}$</td>
<td>Chip Enable Access Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$t_{AA}$</td>
<td>Address Access Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{OE}$</td>
<td>Output Enable Access Time</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{LZ}^{(4)}$</td>
<td>$\overline{CE}$ Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OLZ}^{(4)}$</td>
<td>$\overline{OE}$ Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HZ}^{(5)}$</td>
<td>$\overline{CE}$ High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
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<tr>
<td>$t_{OHZ}^{(5)}$</td>
<td>$\overline{OE}$ High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
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<tr>
<td>$t_{OH}$</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Read Cycle**

**Notes:**

(4) $t_{LZ}$ min. and $t_{OLZ}$ min. are shown for reference only, they are periodically characterized and are not tested.

(5) $t_{HZ}$ max. and $t_{OHZ}$ max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. $t_{HZ}$ min. and $t_{OHZ}$ min. are shown for reference only, they are periodically characterized and are not tested.
X2864BM

Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
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<th>Typ.(6)</th>
<th>Max.</th>
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<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>3</td>
<td>5</td>
<td></td>
<td>ms</td>
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<tr>
<td>tAS</td>
<td>Address Setup Time</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCS</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCH</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCW</td>
<td>OE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOES</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOEH</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWP</td>
<td>WE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWPH</td>
<td>WE High Recovery</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tdV</td>
<td>Data Valid</td>
<td>100</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>tdS</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tdH</td>
<td>Data Hold</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tdW</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>tBLC</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td>100</td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

WE Controlled Write Cycle

Note: (6) Typical values are for $T_A = 25°C$ and nominal supply voltage.
**CE Controlled Write Cycle**

![CE Controlled Write Cycle Diagram]

**Page Mode Write Cycle**

![Page Mode Write Cycle Diagram]

Notes:

1. Between successive byte writes within a page write operation, \( \overline{OE} \) can be strobed LOW; e.g., this can be done with \( \overline{CE} \) and \( \overline{WE} \) HIGH to fetch data from another memory device within the system for the next write; or with \( \overline{WE} \) HIGH and \( \overline{CE} \) LOW effectively performing a polling operation.

2. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the \( \overline{CE} \) or \( \overline{WE} \) controlled write cycle timing.

*For each successive write within the page write operation, \( A_5-A_{12} \) should be the same or writes to an unknown address could occur.*
DATA Polling Timing Diagram

**ADDRESS**

**OE**

**WE**

**OE**

**I/O**

**SYMBOL TABLE**

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Must be steady</td>
<td>Will be steady</td>
<td></td>
</tr>
<tr>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
<td></td>
</tr>
<tr>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
<td></td>
</tr>
<tr>
<td>Don't Care:</td>
<td>Changing:</td>
<td></td>
</tr>
<tr>
<td>Changes:</td>
<td>State Not Known</td>
<td></td>
</tr>
<tr>
<td>Allowed</td>
<td>Center Line is High</td>
<td></td>
</tr>
<tr>
<td>N/A</td>
<td>Impedance</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
X2864BM

PIN DESCRIPTIONS

Addresses (A0–A12)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O0–I/O7)
Data is written to or read from the X2864B through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X2864B.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X2864B supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation
The page write feature of the X2864B allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864B prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A5 through A12 must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

DATA Polling
The X2864B features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X2864B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O7 will reflect true data.

WRITE PROTECTION
There are two features that protect the nonvolatile data from inadvertent writes.

- VCC Sense—All functions are inhibited when VCC is ≤3.5V.
- Write Inhibit—Holding either OE LOW, WE HIGH or CE HIGH during power-on and power-off, will inhibit inadvertent writes.
SYSTEM CONSIDERATIONS
Because the X2864B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that \( \overline{CE} \) be decoded from the address bus and be used as the primary device selection input. Both \( \overline{OE} \) and \( WE \) would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling \( CE \) will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 \( \mu F \) high frequency ceramic capacitor be used between \( V_{CC} \) and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 \( \mu F \) electrolytic bulk capacitor be placed between \( V_{CC} \) and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM

![Diagram](image-url)
# X2864BM

## ORDERING INFORMATION

### 64K E²PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X2864BDM-12</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>120 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864BDM-15</td>
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<td>•</td>
<td>M</td>
<td>150 ns</td>
<td>NMOS</td>
<td>Standard</td>
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<td>•</td>
<td>M</td>
<td>180 ns</td>
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<td>Standard</td>
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<tr>
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<td>•</td>
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<td>120 ns</td>
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<td>•</td>
<td>M</td>
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<td>NMOS</td>
<td>Standard</td>
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<tr>
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<td>•</td>
<td>M</td>
<td>180 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

### Key:
- † = Blank = Commercial = 0°C to +70°C
- ‡ = Industrial = -40°C to +85°C
- § = Military = -55°C to +125°C
- ‡‡ = Ultra High Temp. = 0°C to +150°C

- S = Plastic Small Outline Gull Wing
- P = Plastic DIP
- D = 28-Lead Cerdip
- C = Side Braze
- F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
- F2 = Ceramic Flat Pack for X28256 and X28C256
- K = 28-Pin Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
- G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
## ORDERING INFORMATION

### 64K E²PROMs (Continued)

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
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<td>150 ns</td>
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<td>•</td>
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<td>•</td>
<td>M</td>
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<td>NMOS</td>
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<tr>
<td>X2864BGMB-18</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>180 ns</td>
<td>NMOS</td>
<td>883 Rev. C, Class B</td>
</tr>
</tbody>
</table>

**Key:**
- † = Blank = Commercial = 0°C to + 70°C
- I = Industrial = -40°C to + 85°C
- M = Military = -55°C to +125°C
- T = Ultra High Temp. = 0°C to +150°C
- S = Plastic Small Outline Gull Wing
- P = Plastic DIP
- D = 28-Lead Cerdip
- C = Side Braze
- F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
- F2 = Ceramic Flat Pack for X28256 and X28C256
- K = 28-Pin Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
- G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

### LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

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### U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,488,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932. Foreign patents and additional patents pending.

### LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

2-48
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS
<table>
<thead>
<tr>
<th>Sales Offices</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>U.S. Sales Offices</strong></td>
</tr>
<tr>
<td><strong>Northeast Area</strong></td>
</tr>
<tr>
<td>Xicor, Inc.</td>
</tr>
<tr>
<td>Montvale Executive Park</td>
</tr>
<tr>
<td>91 Montvale Avenue</td>
</tr>
<tr>
<td>Stoneham, Massachusetts 02180</td>
</tr>
<tr>
<td>Phone: 617/279-0220</td>
</tr>
<tr>
<td>Telex: 230322889</td>
</tr>
<tr>
<td>Fax: 617/279-1132</td>
</tr>
<tr>
<td><strong>Southeast Area</strong></td>
</tr>
<tr>
<td>Xicor, Inc.</td>
</tr>
<tr>
<td>201 Park Place</td>
</tr>
<tr>
<td>Suite 203</td>
</tr>
<tr>
<td>Altamonte Springs</td>
</tr>
<tr>
<td>Florida 32701</td>
</tr>
<tr>
<td>Phone: 305/767-8010</td>
</tr>
<tr>
<td>TWX: 510-100-7141</td>
</tr>
<tr>
<td>Fax: 305/767-8912</td>
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<tr>
<td><strong>Mid-Atlantic Area</strong></td>
</tr>
<tr>
<td>Xicor, Inc.</td>
</tr>
<tr>
<td>Patriot Square</td>
</tr>
<tr>
<td>39 Mill Plain Road</td>
</tr>
<tr>
<td>Danbury, Connecticut 06810</td>
</tr>
<tr>
<td>Phone: 203/743-1701</td>
</tr>
<tr>
<td>Telex: 230853137</td>
</tr>
<tr>
<td>Fax: 203/794-9501</td>
</tr>
<tr>
<td><strong>North Central Area</strong></td>
</tr>
<tr>
<td>Xicor, Inc.</td>
</tr>
<tr>
<td>953 North Plum Grove Road</td>
</tr>
<tr>
<td>Suite D</td>
</tr>
<tr>
<td>Schaumburg, Illinois 60173</td>
</tr>
<tr>
<td>Phone: 312/490-1310</td>
</tr>
<tr>
<td>TWX: 910-997-3663</td>
</tr>
<tr>
<td>Fax: 312/490-0637</td>
</tr>
<tr>
<td><strong>South Central Area</strong></td>
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<tr>
<td>Xicor, Inc.</td>
</tr>
<tr>
<td>9330 Amberton Parkway</td>
</tr>
<tr>
<td>Suite 137</td>
</tr>
<tr>
<td>Dallas, Texas 75243</td>
</tr>
<tr>
<td>Phone: 214/669-2022</td>
</tr>
<tr>
<td>Telex: 62027057</td>
</tr>
<tr>
<td>Fax: 214/644-5835</td>
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<tr>
<td><strong>Southwest Area</strong></td>
</tr>
<tr>
<td>Xicor, Inc.</td>
</tr>
<tr>
<td>4141 MacArthur Boulevard</td>
</tr>
<tr>
<td>Suite 205</td>
</tr>
<tr>
<td>Newport Beach, California 92660</td>
</tr>
<tr>
<td>Phone: 714/752-8700</td>
</tr>
<tr>
<td>TWX: 510-101-0110</td>
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<tr>
<td>Fax: 714/752-8634</td>
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<tr>
<td><strong>Northwest Area</strong></td>
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<tr>
<td>Xicor, Inc.</td>
</tr>
<tr>
<td>851 Buckeye Court</td>
</tr>
<tr>
<td>Milpitas, California 95035</td>
</tr>
<tr>
<td>Phone: 408/292-2011</td>
</tr>
<tr>
<td>TWX: 910-379-0033</td>
</tr>
<tr>
<td>Fax: 408/432-0640</td>
</tr>
</tbody>
</table>

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| **Northern Europe Area** |
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| Hawkins House |
| 14 Black Bourton Road |
| Carterton |
| Oxford OX8 3QA |
| United Kingdom |
| Phone: 44.993.844.435 |
| Telex: 851838029 |
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| **Southern Europe Area** |
| Xicor, GmbH |
| Forsthausstrasse 1 |
| D8013 Haar bei Muenchen |
| West Germany |
| Phone: 49.8946.3089 |
| Telex: 8415213883 |
| Fax: 49.89.460.5472 |
| **Far East Area** |
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| Milpitas, California 95035 |
| USA |
| Phone: 408/432-8888 |
| TWX: 910-379-0033 |
| Fax: 408/432-0640 |
TYPICAL FEATURES

- 70 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - 32-Byte Page Write Operation
  - Byte or Page Write Cycle: 3 ms Typical
  - Complete Memory Rewrite: 750 ms Typical
- Effective Byte Write Cycle Time of 95 μs Typical
- DATA Polling
  - Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - Single TTL Level WE Signal
  - Internally Latched Address and Data
  - Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X2864H is a high speed 8K x 8 E2PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864H features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, and EPROMs.

The X2864H supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864H also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

PIN CONFIGURATIONS

X2864H

<table>
<thead>
<tr>
<th>PIN NAMES</th>
<th>X2864H (TOP VIEW)</th>
<th>PGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0~A12</td>
<td>Address Inputs</td>
<td></td>
</tr>
<tr>
<td>I/O0~I/O7</td>
<td>Data Input/Output</td>
<td></td>
</tr>
<tr>
<td>WE</td>
<td>Write Enable</td>
<td></td>
</tr>
<tr>
<td>CE</td>
<td>Chip Enable</td>
<td></td>
</tr>
<tr>
<td>OE</td>
<td>Output Enable</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>+5V</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>No Connect</td>
<td></td>
</tr>
</tbody>
</table>

Characteristics subject to change without notice
**ABSOLUTE MAXIMUM RATINGS**

*Temperature Under Bias*
- X2864H: -10°C to +85°C
- X2864HI: -85°C to +135°C

*Storage Temperature*
- -65°C to +150°C

*Voltage on any Pin with Respect to Ground*
- -1.0V to +7V

*D.C. Output Current* (Soldering, 10 Seconds)
- 5 mA

*X2864H* TA = 0°C to +70°C, Vcc = +5V ±5%, unless otherwise specified.
*X2864HI* TA = -40°C to +85°C, Vcc = +5V ±10%, unless otherwise specified.

**D.C. OPERATING CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
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<tbody>
<tr>
<td>ICC</td>
<td>Vcc Current (Active)</td>
<td>Min.</td>
<td>Typ.(1)</td>
</tr>
<tr>
<td></td>
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<tr>
<td></td>
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<tr>
<td>ISB</td>
<td>Vcc Current (Standby)</td>
<td>Min.</td>
<td>Typ.(1)</td>
</tr>
<tr>
<td></td>
<td></td>
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<tr>
<td></td>
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<tr>
<td>ILI</td>
<td>Input Leakage Current</td>
<td>Min.</td>
<td>Typ.(1)</td>
</tr>
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<td></td>
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<td>ILO</td>
<td>Output Leakage Current</td>
<td>Min.</td>
<td>Typ.(1)</td>
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<tr>
<td>VIL(2)</td>
<td>Input Low Voltage</td>
<td>Min.</td>
<td>Typ.(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<tr>
<td>VIL(2)</td>
<td>Input High Voltage</td>
<td>Min.</td>
<td>Typ.(1)</td>
</tr>
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<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>Min.</td>
<td>Typ.(1)</td>
</tr>
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<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>Min.</td>
<td>Typ.(1)</td>
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**TYPICAL POWER-UP TIMING**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.(1)</th>
<th>Units</th>
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<tbody>
<tr>
<td>tpuR(3)</td>
<td>Power-Up to Read Operation</td>
<td>1</td>
<td>ms</td>
</tr>
<tr>
<td>tpuw(3)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
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</table>

**CAPACITANCE**

TA = 25°C, f = 1.0 MHz, VCC = 5V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>pF</th>
</tr>
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<tbody>
<tr>
<td>C1/O(3)</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>C1N(3)</td>
<td>Input Capacitance</td>
<td>6</td>
<td>VIO = 0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VIN = 0V</td>
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**A.C. CONDITIONS OF TEST**

<table>
<thead>
<tr>
<th>Input Levels</th>
<th>0.4V to 2.4V</th>
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<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
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<tr>
<td>Input and Output Timing Levels</td>
<td>0.8V and 2.0V</td>
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<tr>
<td>Output Load</td>
<td>1 TTL Gate and CL = 30 pF</td>
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**MODE SELECTION**

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<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>DOUT</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>DIN</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Typical values are for TA = 25°C and nominal supply voltage.
2. VIL min. and VIH max. are for reference only and are not tested.
3. This parameter is periodically sampled and not 100% tested.
A.C. CHARACTERISTICS

X2864H $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified.

X2864HI $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X2864H-70</th>
<th>X2864HI-70</th>
<th>X2864H-90</th>
<th>X2864HI-90</th>
<th>Units</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
<td>ns</td>
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<tr>
<td>$t_{RC}$</td>
<td>Read Cycle Time</td>
<td>70</td>
<td>90</td>
<td>70</td>
<td>90</td>
<td>ns</td>
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<tr>
<td>$t_{CE}$</td>
<td>Chip Enable Access Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$t_{AA}$</td>
<td>Address Access Time</td>
<td>70</td>
<td>90</td>
<td>70</td>
<td>90</td>
<td>ns</td>
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<tr>
<td>$t_{OE}$</td>
<td>Output Enable Access Time</td>
<td>35</td>
<td>45</td>
<td>35</td>
<td>45</td>
<td>ns</td>
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<tr>
<td>$t_{LZ}^{(4)}$</td>
<td>CE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
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<tr>
<td>$t_{OLZ}^{(4)}$</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
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<tr>
<td>$t_{HZ}^{(5)}$</td>
<td>CE High to High Z Output</td>
<td>0</td>
<td>40</td>
<td>0</td>
<td>40</td>
<td>ns</td>
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<tr>
<td>$t_{OHZ}^{(5)}$</td>
<td>OE High to High Z Output</td>
<td>0</td>
<td>40</td>
<td>0</td>
<td>40</td>
<td>ns</td>
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<tr>
<td>$t_{OH}$</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

Read Cycle

Notes:

(4) $t_{LZ}$ min. and $t_{OLZ}$ min. are shown for reference only, they are periodically characterized and are not tested.

(5) $t_{HZ}$ max. and $t_{OHZ}$ max. are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven. $t_{HZ}$ min. and $t_{OHZ}$ min. are shown for reference only, they are periodically characterized and are not tested.
## Write Cycle Limits

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<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X2864H-70</th>
<th>X2864H-90</th>
<th>Units</th>
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<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
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<td>t(_{WC})</td>
<td>Write Cycle Time</td>
<td>5</td>
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<td>5</td>
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<tr>
<td>t(_{AS})</td>
<td>Address Setup Time</td>
<td>5</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>t(_{AH})</td>
<td>Address Hold Time</td>
<td>50</td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>t(_{CS})</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>t(_{CH})</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>t(_{CW})</td>
<td>CE Pulse Width</td>
<td>60</td>
<td></td>
<td>80</td>
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<tr>
<td>t(_{OES})</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>t(_{OEH})</td>
<td>OE High Hold Time</td>
<td>5</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>t(_{WP})</td>
<td>WE Pulse Width</td>
<td>60</td>
<td></td>
<td>80</td>
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<tr>
<td>t(_{WPH})</td>
<td>WE High Recovery</td>
<td>50</td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>t(_{DV})</td>
<td>Data Valid</td>
<td>100</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>t(_{DS})</td>
<td>Data Setup</td>
<td>35</td>
<td></td>
<td>35</td>
</tr>
<tr>
<td>t(_{DH})</td>
<td>Data Hold</td>
<td>5</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>t(_{DW})</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td>10</td>
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<tr>
<td>t(_{BLC})</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td></td>
<td>100</td>
</tr>
</tbody>
</table>

### WE Controlled Write Cycle

![Diagram of WE Controlled Write Cycle](image)
CE Controlled Write Cycle

Page Mode Write Cycle

Notes: (6) Between successive byte writes within a page write operation, OE can be strobed LOW; e.g., this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram

SYMBOL TABLE

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td></td>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td></td>
<td>N/A</td>
<td>Center Line Is High Impedance</td>
</tr>
</tbody>
</table>

Note: (b) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS
Addresses (A<sub>0</sub>-A<sub>12</sub>)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O<sub>0</sub>-I/O<sub>7</sub>)
Data is written to or read from the X2864H through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X2864H.

DEVICE OPERATION
Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X2864H supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation
The page write feature of the X2864H allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864H prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A<sub>5</sub> through A<sub>12</sub> must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the 100 µs byte load cycle time.

DATA Polling
The X2864H features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X2864H, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data.

WRITE PROTECTION
There are two features that protect the nonvolatile data from inadvertent writes.

• V<sub>CC</sub> Sense—All functions are inhibited when V<sub>CC</sub> is ≤4.0V.
• Write Inhibit—Holding OE LOW, WE HIGH or CE HIGH during power-on and power-off, will inhibit inadvertent writes.
SYSTEM CONSIDERATIONS
Because the X2864H is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864H has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between \( V_{CC} \) and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between \( V_{CC} \) and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM
**X2864H, X2864HI**

ORDERING INFORMATION

64K E²PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>S</td>
<td>P</td>
<td>D</td>
<td>C</td>
<td>F1</td>
</tr>
<tr>
<td>X2864HP-70</td>
<td>8192 x 8</td>
<td><img src="image1.png" alt="Image" /></td>
<td>†</td>
<td>70 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HP-90</td>
<td>8192 x 8</td>
<td><img src="image2.png" alt="Image" /></td>
<td>†</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HPI-90</td>
<td>8192 x 8</td>
<td><img src="image3.png" alt="Image" /></td>
<td>I</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HD-70</td>
<td>8192 x 8</td>
<td><img src="image4.png" alt="Image" /></td>
<td>†</td>
<td>70 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HD-90</td>
<td>8192 x 8</td>
<td><img src="image5.png" alt="Image" /></td>
<td>†</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
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<td>X2864HDI-90</td>
<td>8192 x 8</td>
<td><img src="image6.png" alt="Image" /></td>
<td>I</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HF-70</td>
<td>8192 x 8</td>
<td><img src="image7.png" alt="Image" /></td>
<td>†</td>
<td>70 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HF-90</td>
<td>8192 x 8</td>
<td><img src="image8.png" alt="Image" /></td>
<td>†</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HFI-90</td>
<td>8192 x 8</td>
<td><img src="image9.png" alt="Image" /></td>
<td>I</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HK-70</td>
<td>8192 x 8</td>
<td><img src="image10.png" alt="Image" /></td>
<td>†</td>
<td>70 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HK-90</td>
<td>8192 x 8</td>
<td><img src="image11.png" alt="Image" /></td>
<td>†</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HKI-90</td>
<td>8192 x 8</td>
<td><img src="image12.png" alt="Image" /></td>
<td>I</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HJ-70</td>
<td>8192 x 8</td>
<td><img src="image13.png" alt="Image" /></td>
<td>†</td>
<td>70 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HJ-90</td>
<td>8192 x 8</td>
<td><img src="image14.png" alt="Image" /></td>
<td>†</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HJI-90</td>
<td>8192 x 8</td>
<td><img src="image15.png" alt="Image" /></td>
<td>I</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)
## ORDERING INFORMATION

### 64K E²PROMs (Continued)

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<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X2864HE-70</td>
<td>8192 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>†</td>
<td>70 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HE-90</td>
<td>8192 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>†</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HEI-90</td>
<td>8192 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>I</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HG-70</td>
<td>8192 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>†</td>
<td>70 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HG-90</td>
<td>8192 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>†</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HGI-90</td>
<td>8192 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>I</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

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- G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

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In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS
## Sales Offices

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TWX: 910-379-0033  
Fax: 408/432-0640
**Electrically Erasable PROM**

**TYPICAL FEATURES**
- **90 ns Access Time**
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - 32-Byte Page Write Operation
  - Byte or Page Write Cycle: 3 ms Typical
  - Complete Memory Rewrite: 750 ms Typical
  - Effective Byte Write Cycle Time of 95 µs Typical
- **DATA Polling**
  - Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - Single TTL Level WE Signal
  - Internally Latched Address and Data
  - Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

**DESCRIPTION**
The Xicor X2864H is a high speed 8K x 8 E²PROM, fabricated with Xicor's propriety, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864H features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864H supports a 32-byte page write operation, effectively providing a 95 µs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864H also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

**PIN CONFIGURATIONS**

- **CERDIP FLAT PACK**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
</tr>
<tr>
<td>2</td>
<td>A1</td>
</tr>
<tr>
<td>3</td>
<td>A2</td>
</tr>
<tr>
<td>4</td>
<td>A3</td>
</tr>
<tr>
<td>5</td>
<td>A4</td>
</tr>
<tr>
<td>6</td>
<td>A5</td>
</tr>
<tr>
<td>7</td>
<td>A6</td>
</tr>
<tr>
<td>8</td>
<td>X2864H</td>
</tr>
<tr>
<td>9</td>
<td>A7</td>
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<tr>
<td>10</td>
<td>A8</td>
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<td>11</td>
<td>A9</td>
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<td>A10</td>
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<tr>
<td>27</td>
<td>NC</td>
</tr>
<tr>
<td>28</td>
<td>VCC</td>
</tr>
</tbody>
</table>

- **LCC**

- **PGA**

**PIN NAMES**

- A₀–A₁₂: Address Inputs
- I/O₀–I/O₇: Data Input/Output
- WE: Write Enable
- CE: Chip Enable
- OE: Output Enable
- VCC: +5V
- VSS: Ground
- NC: No Connect

Characteristics subject to change without notice
### ABSOLUTE MAXIMUM RATINGS*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Under Bias</td>
<td>-65°C to +135°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage on Any Pin with</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Respect to Ground</td>
<td>-1.0V to +7V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D.C. Output Current</td>
<td>.5 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 Seconds)</td>
<td>300°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D.C. OPERATING CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA = -55°C to +125°C, VCC = +5V ±10%, unless otherwise specified.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
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### D.C. OPERATING CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VCC Current (Active)</td>
<td>Min.</td>
<td>Typ. (1)</td>
</tr>
<tr>
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<td></td>
<td>80</td>
<td>150</td>
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<td></td>
<td>VCC Current (Standby)</td>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td>Input Leakage Current</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Output Leakage Current</td>
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<td>µA</td>
</tr>
<tr>
<td></td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>VCC +1.0</td>
</tr>
<tr>
<td></td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>V</td>
</tr>
</tbody>
</table>

### TYPICAL POWER-UP TIMING

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ. (1)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>tPUR(3)</td>
<td>Power-Up to Read Operation</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>tPUW(3)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
</tr>
</tbody>
</table>

### CAPACITANCE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C110(3)</td>
<td>10</td>
<td>pF</td>
<td>V1/O = 0V</td>
</tr>
<tr>
<td></td>
<td>C1N(3)</td>
<td>6</td>
<td>pF</td>
<td>V1N = 0V</td>
</tr>
</tbody>
</table>

### A.C. CONDITIONS OF TEST

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pulse Levels</td>
<td>0.4V to 2.4V</td>
</tr>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>0.8V and 2.0V</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and CL = 30 pF</td>
</tr>
</tbody>
</table>

### MODE SELECTION

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>DOUT</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>D_IN</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Notes:**

1. Typical values are for $T_A = 25^\circ C$ and nominal supply voltage.
2. $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.
3. This parameter is periodically sampled and not 100% tested.
A.C. CHARACTERISTICS

$T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

### Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{RC}$</td>
<td>Read Cycle Time</td>
<td>90</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CE}$</td>
<td>Chip Enable Access Time</td>
<td></td>
<td>90</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AA}$</td>
<td>Address Access Time</td>
<td></td>
<td>90</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OE}$</td>
<td>Output Enable Access Time</td>
<td></td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{LZ(4)}$</td>
<td>$\overline{CE}$ Low to Active Output</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OLZ(4)}$</td>
<td>$\overline{OE}$ Low to Active Output</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HZ(5)}$</td>
<td>$\overline{CE}$ High to High Z Output</td>
<td>0</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OHZ(5)}$</td>
<td>$\overline{OE}$ High to High Z Output</td>
<td>0</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OH}$</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:

(4) $t_{LZ}$ min. and $t_{OLZ}$ min. are shown for reference only, they are periodically characterized and are not tested.

(5) $t_{HZ}$ max. and $t_{OHZ}$ max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. $t_{HZ}$ min. and $t_{OHZ}$ min. are shown for reference only, they are periodically characterized and are not tested.
### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{WC} )</td>
<td>Write Cycle Time</td>
<td>5</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_{AS} )</td>
<td>Address Setup Time</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AH} )</td>
<td>Address Hold Time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CS} )</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CH} )</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OW} )</td>
<td>OE Pulse Width</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OES} )</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OEH} )</td>
<td>OE High Hold Time</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WP} )</td>
<td>WE Pulse Width</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WPH} )</td>
<td>WE High Recovery</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DV} )</td>
<td>Data Valid</td>
<td></td>
<td>100</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{DS} )</td>
<td>Data Setup</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DH} )</td>
<td>Data Hold</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DW} )</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{BLC} )</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td>100</td>
<td>( \mu \text{s} )</td>
</tr>
</tbody>
</table>

### WE Controlled Write Cycle

![Diagram of WE Controlled Write Cycle](image)
**CE Controlled Write Cycle**

![Diagram of CE Controlled Write Cycle](image)

**Page Mode Write Cycle**

![Diagram of Page Mode Write Cycle](image)

---

Notes:

(6) Between successive byte writes within a page write operation, OE can be strobed LOW; e.g., this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram

**Symbol Table**

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td></td>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Note:** (8) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS

Addresses (A₀-A₁₂)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O₀-I/O₇)
Data is written to or read from the X2864H through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X2864H.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X2864H supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation
The page write feature of the X2864H allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864H prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A₅ through A₁₂ must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the 100 μs byte load cycle time.

DATA Polling
The X2864H features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X2864H, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₇ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O₇ will reflect true data.

WRITE PROTECTION
There are two features that protect the nonvolatile data from inadvertent writes.

- VCC Sense—All functions are inhibited when VCC is ≤4.0V.
- Write Inhibit—Holding OE LOW, WE HIGH or CE HIGH during power-on and power-off, will inhibit inadvertent writes.
SYSTEM CONSIDERATIONS
Because the X2864H is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both CE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864H has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a $0.1 \mu F$ high frequency ceramic capacitor be used between $V_{CC}$ and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a $4.7 \mu F$ electrolytic bulk capacitor be placed between $V_{CC}$ and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM
### ORDERING INFORMATION

**64K E²PROMs**

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X2864HDM-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HDMB-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>883 Rev. C, Class B</td>
</tr>
<tr>
<td>X2864HFM-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HFMB-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>883 Rev. C, Class B</td>
</tr>
<tr>
<td>X2864HKM-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HKMB-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>883 Rev. C, Class B</td>
</tr>
<tr>
<td>X2864HEM-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HEMB-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>883 Rev. C, Class B</td>
</tr>
<tr>
<td>X2864HGM-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X2864HGMB-90</td>
<td>8192 x 8</td>
<td>•</td>
<td>M</td>
<td>90 ns</td>
<td>NMOS</td>
<td>883 Rev. C, Class B</td>
</tr>
</tbody>
</table>

**Key:**
- ✧ = Blank = Commercial = 0°C to + 70°C
- ✤ = Industrial = -40°C to + 85°C
- ✦ = Military = -55°C to +125°C
- ✧ = Ultra High Temp. = -5°C to +150°C
- S = Plastic Small Outline Gull Wing
- P = Plastic DIP
- D = 28-Lead Cerdip
- C = Side Braze
- F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
- F2 = Ceramic Flat Pack for X28256 and X28C256
- K = 28-Pin Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
- G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

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**LIFE RELATED POLICY**

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F1

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: LEADS 4, 12, 18 & 26

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS
# Sales Offices

## U.S. Sales Offices

### Northeast Area
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Fax: 305/767-8912

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Telex: 230853137  
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Telex: 62027057  
Fax: 214/644-5835

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TWX: 510-101-0110  
Fax: 714/752-8634

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TWX: 910-379-0033  
Fax: 408/432-0640

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United Kingdom  
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Telex: 851838029  
Fax: 44.993.841.029

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D8013 Haar bei Muenchen  
West Germany  
Phone: 49.8946.3089  
Telex: 8415213883  
Fax: 49.89.460.5472

### Far East Area
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851 Buckeye Court  
Milpitas, California 95035  
USA  
Phone: 408/432-8888  
TWX: 910-379-0033  
Fax: 408/432-0640
**FEATURES**

- **LOW Power CMOS**
  - -60 mA Active Current Max.
  - -200 µA Standby Current Max.

- **Fast Write Cycle Times**
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 0.625 Sec. Typical
  - Effective Byte Write Cycle Time: 78 µs Typical

- **Software Data Protection**
- **End of Write Detection**
  - DATA Polling
  - Toggle Bit

- **Simple Byte and Page Write**
  - Single TTL Compatible WE Signal
  - Internally Latched Address and Data
  - Automatic Write Timing

- **JEDEC Approved Byte-Wide Pinout**

**DESCRIPTION**

The Xicor X28C64 is a 8K x 8 E²PROM, fabricated with Xicor’s proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C64 supports a 64-byte page write operation, effectively providing a 78 µs/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor’s hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

**PIN CONFIGURATIONS**

**PLASTIC CERDIP FLAT PACK**

| NC | 1 | 28 | VCC |
| NC | 2 | 27 | WE |
| A0 | 3 | 26 | NC |
| A1 | 4 | 25 | A2 |
| A2 | 5 | 24 | A3 |
| A3 | 6 | 23 | A4 |
| A4 | 7 | 22 | OE |
| A5 | 8 | 21 | A6 |
| A6 | 9 | 20 | CE |
| A7 | 10 | 19 | I/O7 |
| VCC | 11 | 18 | I/O6 |
| VDD | 12 | 17 | I/O5 |
| VDD | 13 | 16 | I/O4 |
| VDD | 14 | 15 | I/O3 |

**X28C64 (TOP VIEW)**

**PLCC LCC**

**PGA**

- VO1, VO2, VO3, VO4, VO5, VO6, VO7
- AO, AO, AO, AO, AO, AO, AO
- CE, CE
- OE, OE
- VCC, +5V
- VSS, Ground
- NC, No Connect

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Characteristics subject to change without notice
ABSOLUTE MAXIMUM RATINGS*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ. (1)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Under Bias</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X28C64</td>
<td></td>
<td></td>
<td>-10°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+ 85°C</td>
<td></td>
</tr>
<tr>
<td>X28C641</td>
<td></td>
<td></td>
<td>-65°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+ 135°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td></td>
<td></td>
<td>-65°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+ 150°C</td>
<td></td>
</tr>
<tr>
<td>Voltage on any Pin with</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Respect to Ground</td>
<td></td>
<td></td>
<td>-1.0V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+ 7V</td>
<td></td>
</tr>
<tr>
<td>D.C. Output Current</td>
<td></td>
<td></td>
<td>5 mA</td>
<td></td>
</tr>
<tr>
<td>(Soldering, 10 Seconds)</td>
<td></td>
<td></td>
<td></td>
<td>300°C</td>
</tr>
</tbody>
</table>

D.C. OPERATING CHARACTERISTICS

X28C64 $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.
X28C641 $T_A = -40^\circ C$ to $+85^\circ C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
<td>Typ. (1)</td>
<td>Max.</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>$V_{CC}$ Current (Active) (TTL Inputs)</td>
<td>60 mA</td>
<td></td>
</tr>
<tr>
<td>$I_{SB1}$</td>
<td>$V_{CC}$ Current (Standby) (TTL Inputs)</td>
<td>2 mA</td>
<td></td>
</tr>
<tr>
<td>$I_{SB2}$</td>
<td>$V_{CC}$ Current (Standby) (CMOS Inputs)</td>
<td>100 µA</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Current</td>
<td>10 µA</td>
<td></td>
</tr>
<tr>
<td>$I_{IO}$</td>
<td>Output Leakage Current</td>
<td>10 µA</td>
<td></td>
</tr>
<tr>
<td>$V_{IL(2)}$</td>
<td>Input Low Voltage</td>
<td>-1.0 V</td>
<td></td>
</tr>
<tr>
<td>$V_{IH(2)}$</td>
<td>Input High Voltage</td>
<td>2.0 V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>0.4 V</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>2.4 V</td>
<td></td>
</tr>
</tbody>
</table>

TYPICAL POWER-UP TIMING

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ. (1)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PUR(3)}$</td>
<td>Power-Up to Read Operation</td>
<td>100 µs</td>
<td></td>
</tr>
<tr>
<td>$t_{PUPW(3)}$</td>
<td>Power-Up to Write Operation</td>
<td>5 ms</td>
<td></td>
</tr>
</tbody>
</table>

CAPACITANCE $T_A = 25^\circ C$, $f = 1.0$ MHz, $V_{CC} = 5V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{I/O(3)}$</td>
<td>Input/Output Capacitance</td>
<td>10 pF</td>
<td></td>
<td>$V_{I/O} = 0V$</td>
</tr>
<tr>
<td>$C_{IN(3)}$</td>
<td>Input Capacitance</td>
<td>6 pF</td>
<td></td>
<td>$V_{IN} = 0V$</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST

| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | 1 TTL Gate and $C_L = 100$ pF |

MODE SELECTION

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>$D_{OUT}$</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>$D_{IN}$</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes: (1) Typical values are for $T_A = 25^\circ C$ and nominal supply voltage.
(2) $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.
A.C. CHARACTERISTICS

X28C64 $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

X28C641 $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X28C64-20</th>
<th>X28C64-25</th>
<th>X28C64</th>
<th>X28C64I</th>
<th>X28C64I-35</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>$t_{RC}$</td>
<td>Read Cycle Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>$t_{CE}$</td>
<td>Chip Enable Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>$t_{AA}$</td>
<td>Address Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>$t_{OE}$</td>
<td>Output Enable Access Time</td>
<td>80</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>$t_{LZ}$(4)</td>
<td>CE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>$t_{OLZ}$(4)</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>$t_{HZ}$(5)</td>
<td>CE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>$t_{OHZ}$(5)</td>
<td>OE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>$t_{OH}$</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Notes:

(4) $t_{LZ}$ min. and $t_{OLZ}$ min. are shown for reference only, they are periodically characterized and are not tested.

(5) $t_{HZ}$ max. and $t_{OHZ}$ max. are measured from the point when $CE$ or $OE$ return high (whichever occurs first) to the time when the outputs are no longer driven. $t_{HZ}$ min. and $t_{OHZ}$ min. are shown for reference only, they are periodically characterized and are not tested.
### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(6)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{WC}$</td>
<td>Write Cycle Time</td>
<td></td>
<td>5</td>
<td>10</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{AS}$</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AH}$</td>
<td>Address Hold Time</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CS}$</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CH}$</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CW}$</td>
<td>CE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OES}$</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OEH}$</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WP}$</td>
<td>WE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WPH}$</td>
<td>WE High Recovery</td>
<td>200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OV}$</td>
<td>Data Valid</td>
<td>1</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{DS}$</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>Data Hold</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DW}$</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{BLC}$</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td></td>
<td>100</td>
<td>µs</td>
</tr>
</tbody>
</table>

#### WE Controlled Write Cycle

![Diagram of WE Controlled Write Cycle](image)

**Note:** (6) Typical values are for $T_A = 25°C$ and nominal supply voltage.
**CE Controlled Write Cycle**

For each successive write within the page write operation, A\textsubscript{6}-A\textsubscript{12} should be the same or writes to an unknown address could occur.

Notes:

1. Between successive byte writes within a page write operation, OE can be strobed LOW: e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

2. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram (9)

ADDRESS

\[ \text{An} \]

\[ \text{An} \]

\[ \text{An} \]

\[ \text{OE} \]

\[ \text{OE} \]

\[ \text{WE} \]

\[ \text{WE} \]

\[ \text{I/O} \]

\[ \text{I/O} \]

\[ D_{\text{IN}} = X \]

\[ D_{\text{OUT}} = X \]

\[ t_{\text{WC}} \]

\[ t_{\text{DEH}} \]

\[ t_{\text{DES}} \]

\[ t_{\text{DW}} \]

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

Toggle Bit Timing Diagram (9)

\[ \text{OE} \]

\[ \text{WE} \]

\[ \text{OE} \]

\[ \text{I/O} \]

\[ \text{I/O} \]

\[ \text{I/O} \]

\[ \text{I/O} \]

\[ t_{\text{WC}} \]

\[ t_{\text{DEH}} \]

\[ t_{\text{DES}} \]

\[ t_{\text{DW}} \]

\[ *I/O\text{O}_6\text{ beginning and ending state will vary, depending upon actual }t_{\text{WC}}.* \]

SYMBOL TABLE

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td></td>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td></td>
<td>xxxx</td>
<td>Center Line Is High Impedance</td>
</tr>
<tr>
<td></td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS
Addresses (A0–A12)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O0–I/O7)
Data is written to or read from the X28C64 through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X28C64.

DEVICE OPERATION
Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X28C64 supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C64 allows the entire memory to be written in 0.625 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C64 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A5 through A12) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The X28C64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment

DATA Polling (I/O7)
The X28C64 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O7 will reflect true data. Note: If the X28C64 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

Toggle Bit (I/O6)
The X28C64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA POLLING I/O7
Figure 2a: DATA Polling Bus Sequence

DATA Polling can effectively halve the time for writing to the X28C64. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.
THE TOGGLE BIT I/Os
Figure 3a: Toggle Bit Bus Sequence

*Beginning and ending state of I/O6 will vary.

Figure 3b: Toggle Bit Software Flow

The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C64 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION
The X28C64 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A WE pulse less than 20 ns will not initiate a write cycle.
- Default V\textsubscript{CC} Sense—All write functions are inhibited when V\textsubscript{CC} is \( \leq 3\) V.
- Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION
The X28C64 offers a software controlled data protection feature. The X28C64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V\textsubscript{CC} was stable.

The X28C64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM
Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.\(^{(10)}\) Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: \(^{(10)}\) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.
SOFTWARE DATA PROTECTION
Figure 4a: Timing Sequence—Byte or Page Write

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C64 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.
In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After \( t_{WC} \), the X28C64 will be in standard operating mode.

**Note:** Once initiated, the sequence of write operations should not be interrupted.
SYSTEM CONSIDERATIONS

Because the X28C64 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM
### ORDERING INFORMATION
#### 64K E²PROMs

<table>
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<tr>
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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor’s products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

PIN 1 INDEX

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

TYP. 0.010 (0.25)

0°
15°
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F1

1.000 ± 0.010

PIN 1 INDEX

0.740 (18.80) MAX.

0.019 (0.48) 0.015 (0.38)

0.050 (1.27) BSC

0.045 (1.14) MAX.

0.400 (10.16) MAX.

0.006 (0.15) 0.003 (0.08)

0.370 (9.40) 0.250 (6.35)

TYP. 0.300 2 PLCS.

0.180 (4.57) MIN.

0.040 (1.02) 0.026 (0.66)

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B, X2864H AND X28C64

CAF028
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

NOTE: LEADS 4, 12, 18 & 26
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
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2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS
# Sales Offices

## U.S. Sales Offices

### Northeast Area
Xicor, Inc.
Montvale Executive Park
91 Montvale Avenue
Stoneham, Massachusetts 02180
Phone: 617/279-0220
Telex: 230322889
Fax: 617/279-1132

### Southeast Area
Xicor, Inc.
201 Park Place
Suite 203
Altamonte Springs
Florida 32701
Phone: 305/767-8010
TWX: 510-100-7141
Fax: 305/767-8912

### Mid-Atlantic Area
Xicor, Inc.
Patriot Square
39 Mill Plain Road
Danbury, Connecticut 06810
Phone: 203/743-1701
Telex: 230853137
Fax: 203/794-9501

### North Central Area
Xicor, Inc.
953 North Plum Grove Road
Suite D
Schaumburg, Illinois 60173
Phone: 312/490-1310
TWX: 910-997-3663
Fax: 312/490-0637

### South Central Area
Xicor, Inc.
9330 Amberton Parkway
Suite 137
Dallas, Texas 75243
Phone: 214/669-2022
Telex: 62027057
Fax: 214/644-5835

### Southwest Area
Xicor, Inc.
4141 MacArthur Boulevard
Suite 205
Newport Beach, California 92660
Phone: 714/752-8700
TWX: 510-101-0110
Fax: 714/752-8634

### Northwest Area
Xicor, Inc.
851 Buckeye Court
Milpitas, California 95035
Phone: 408/292-2011
TWX: 910-379-0033
Fax: 408/432-0640

## International Sales Offices

### Northern Europe Area
Xicor Ltd.
Hawkins House
14 Black Bourton Road
Carterton
Oxford OX8 3QA
United Kingdom
Phone: 44.993.844.435
Telex: 851838029
Fax: 44.993.841.029

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ADVANCED INFORMATION

64K Military X28C64M 8K x 8 Bit

Electrically Erasable PROM

FEATURES
- LOW Power CMOS
  - 60 mA Active Current Max.
  - 200 μA Standby Current Max.
- Fast Write Cycle Times
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 0.625 Sec. Typical
- Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - DATA Polling
  - Toggle Bit
- Simple Byte and Page Write
  - Single TTL Compatible WE Signal
  - Internally Latched Address and Data
  - Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION
The Xicor X28C64 is a 8K x 8 E2PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C64 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

PIN CONFIGURATIONS

PIN NAMES
- A0–A12 Address Inputs
- I/O0–I/O7 Data Input/Output
- WE Write Enable
- CE Chip Enable
- OE Output Enable
- VCC +5V
- VSS Ground
- NC No Connect

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Characteristics subject to change without notice
**ABSOLUTE MAXIMUM RATINGS**

- Temperature Under Bias: -65°C to +135°C
- Storage Temperature: -65°C to +150°C
- Voltage on any Pin with Respect to Ground: -1.0V to +7V
- D.C. Output Current: 5 mA
- Lead Temperature (Soldering, 10 Seconds): 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. OPERATING CHARACTERISTICS**

TA = -55°C to +125°C, VCC = +5V ± 10%, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min.</td>
<td>Typ. (1)</td>
<td>Max.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Icc</td>
<td>VCC Current (Active) (TTL Inputs)</td>
<td>60 mA</td>
<td>CE = OE = VIL, WE = VIH</td>
<td>All I/O's = Open</td>
</tr>
<tr>
<td>Isb1</td>
<td>VCC Current (Standby) (TTL Inputs)</td>
<td>2 mA</td>
<td>CE = VIH, OE = VIL</td>
<td>All I/O's = Open</td>
</tr>
<tr>
<td>Isb2</td>
<td>VCC Current (Standby) (CMOS Inputs)</td>
<td>200 µA</td>
<td>CE = WE = VCC - 0.3V</td>
<td>All I/O's = Open</td>
</tr>
<tr>
<td>Ils</td>
<td>Input Leakage Current</td>
<td>10 µA</td>
<td>VIN = GND to VCC</td>
<td></td>
</tr>
<tr>
<td>IlO</td>
<td>Output Leakage Current</td>
<td>10 µA</td>
<td>VOUT = GND to VCC, CE = VIH</td>
<td></td>
</tr>
<tr>
<td>VIL (2)</td>
<td>Input Low Voltage</td>
<td>-1.0 V</td>
<td>0.8 V</td>
<td></td>
</tr>
<tr>
<td>VIH (2)</td>
<td>Input High Voltage</td>
<td>2.0 V</td>
<td>VCC + 1.0 V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4 V</td>
<td>1OL = 2.1 mA</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4 V</td>
<td>1OH = -400 µA</td>
<td></td>
</tr>
</tbody>
</table>

**TYPICAL POWER-UP TIMING**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ. (1)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tpUR(3)</td>
<td>Power-Up to Read Operation</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>tpUW(3)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

**CAPACITANCE**

TA = 25°C, f = 1.0 MHz, VCC = 5V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1/O(3)</td>
<td>Input/Output Capacitance</td>
<td>10 pF</td>
<td>V1/O = 0V</td>
<td></td>
</tr>
<tr>
<td>C1/N(3)</td>
<td>Input Capacitance</td>
<td>6 pF</td>
<td>VIN = 0V</td>
<td></td>
</tr>
</tbody>
</table>

**A.C. CONDITIONS OF TEST**

| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | 1 TTL Gate and CL = 100 pF |

**MODE SELECTION**

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>DOUT</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>DIN</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Notes:**

1. Typical values are for TA = 25°C and nominal supply voltage.
2. VIL min. and VIH max. are for reference only and are not tested.
3. This parameter is periodically sampled and not 100% tested.

2-120
A.C. CHARACTERISTICS

\( T_A = -55^\circ C \) to \( +125^\circ C \), \( V_{CC} = +5V \pm 10\% \), unless otherwise specified.

### Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>( X28C64M-20 )</th>
<th>( X28C64M-25 )</th>
<th>( X28C64M )</th>
<th>( X28C64M-35 )</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{RC} )</td>
<td>Read Cycle Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CE} )</td>
<td>Chip Enable Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AA} )</td>
<td>Address Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OE} )</td>
<td>Output Enable Access Time</td>
<td>80</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{LZ(4)} )</td>
<td>CE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OLZ(4)} )</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{HZ(5)} )</td>
<td>CE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
<td>0 50</td>
</tr>
<tr>
<td>( t_{OHZ(5)} )</td>
<td>OE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
<td>0 50</td>
</tr>
<tr>
<td>( t_{OH} )</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Read Cycle

```
ADDRESS

\( t_{RC} \)

\( t_{CE} \)

\( t_{OE} \)

\( t_{LZ} \)

\( t_{OLZ} \)

\( t_{HZ} \)

\( t_{OHZ} \)

\( t_{OH} \)

\( t_{AA} \)

DATA I/O

HIGH Z

DATA VALID

DATA VALID
```

**Notes:**

(4) \( t_{LZ} \) min. and \( t_{OLZ} \) min. are shown for reference only, they are periodically characterized and are not tested.

(5) \( t_{HZ} \) max. and \( t_{OHZ} \) max. are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven. \( t_{HZ} \) min. and \( t_{OHZ} \) min. are shown for reference only, they are periodically characterized and are not tested.
## X28C64M

### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(6)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\text{wc}</td>
<td>Write Cycle Time</td>
<td>5</td>
<td></td>
<td>10</td>
<td>ms</td>
</tr>
<tr>
<td>t\text{AS}</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{AH}</td>
<td>Address Hold Time</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{CS}</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{CH}</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{CW}</td>
<td>\text{CE} Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{OES}</td>
<td>\text{OE} High Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{OEH}</td>
<td>\text{OE} High Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{WP}</td>
<td>\text{WE} Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{WPH}</td>
<td>\text{WE} High Recovery</td>
<td>200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{DV}</td>
<td>Data Valid</td>
<td>1</td>
<td></td>
<td></td>
<td>\mu s</td>
</tr>
<tr>
<td>t\text{DS}</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{DH}</td>
<td>Data Hold</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\text{DW}</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td></td>
<td>\mu s</td>
</tr>
<tr>
<td>t\text{BLC}</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td></td>
<td>100</td>
<td>\mu s</td>
</tr>
</tbody>
</table>

### WE Controlled Write Cycle

![Diagram of WE Controlled Write Cycle]

**Note:** (6) Typical values are for \( T_A = 25^\circ \text{C} \) and nominal supply voltage.
CE Controlled Write Cycle

For each successive write within the page write operation, A6–A12 should be the same or writes to an unknown address could occur.

Notes:
(7) Between successive byte writes within a page write operation, OE can be strobed LOW: e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.
(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram(9)

**ADDRESS**

```
| An | An | An |
```

**CE**

```
\[ t_{OEH} \]
```

**WE**

```
\[ t_{OES} \]
```

**OE**

```
\[ t_{DW} \]
```

**I/O\_7**

```
\[ t_{WC} \]
```

Toggle Bit Timing Diagram(9)

**CE**

```
\[ t_{OEH} \]
```

**WE**

```
\[ t_{OES} \]
```

**OE**

```
\[ t_{DW} \]
```

**I/O\_8**

```
\[ t_{WC} \]
```

* I/O\_8 beginning and ending state will vary, depending upon actual t\_WC.

**SYMBOL TABLE**

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
<td>Center Line is High Impedance</td>
</tr>
</tbody>
</table>

**Note:** (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
**PIN DESCRIPTIONS**

**Addresses (A₀–A₁₂)**
The Address inputs select an 8-bit memory location during a read or write operation.

**Chip Enable (CE)**
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

**Output Enable (OE)**
The Output Enable input controls the data output buffers and is used to initiate read operations.

**Data In/Data Out (I/O₀–I/O₇)**
Data is written to or read from the X28C64 through the I/O pins.

**Write Enable (WE)**
The Write Enable input controls the writing of data to the X28C64.

**DEVICE OPERATION**

**Read**
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

**Write**
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X28C64 supports both CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

**Page Write Operation**
The page write feature of the X28C64 allows the entire memory to be written in 0.625 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C64 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A₆ through A₁₂) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

**Write Operation Status Bits**
The X28C64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

**Figure 1: Status Bit Assignment**

The X28C64 provides DATA Polling as a method to indicate to the host system that the byte or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₀ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O₀ will reflect true data. Note: If the X28C64 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

**Toggle Bit (I/O₁₀)**
The X28C64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O₁₀ will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA Polling can effectively halve the time for writing to the X28C64. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.
THE TOGGLE BIT I/Os

Figure 3a: Toggle Bit Bus Sequence

Figure 3b: Toggle Bit Software Flow

*Beginning and ending state of I/O will vary.

The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C64 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION
The X28C64 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A WE pulse less than 20 ns will not initiate a write cycle.
- Default VCC Sense—All write functions are inhibited when VCC is ≤3V.
- Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION
The X28C64 offers a software controlled data protection feature. The X28C64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once VCC was stable.

The X28C64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM
Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: Once the three byte sequence is issued it must be followed by a valid byte or page write operation.
SOFTWARE DATA PROTECTION
Figure 4a: Timing Sequence—Byte or Page Write

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C64 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.
In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After \( t_{WC} \), the X28C64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.
SYSTEM CONSIDERATIONS
Because the X28C64 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM
### Ordering Information

**64K E²PROMs**

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X28C64DM-20</td>
<td>8192 x 8</td>
<td>S</td>
<td>M</td>
<td>200 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C64DM-25</td>
<td>8192 x 8</td>
<td>S</td>
<td>M</td>
<td>250 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C64DM</td>
<td>8192 x 8</td>
<td>S</td>
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**Key:**
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- **D** = 28-Lead Cerdip
- **C** = Side Braze
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---

2-132
### Ordering Information

64K E²PROMs (Continued)

<table>
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<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
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<td>•</td>
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<td>M</td>
<td>350 ns</td>
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LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

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Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,461; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F1

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B, X2864H AND X28C64
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS
## Sales Offices

### U.S. Sales Offices

#### Northeast Area
Xicor, Inc.
Montvale Executive Park
91 Montvale Avenue
Stoneham, Massachusetts 02180
Phone: 617/279-0220
Telex: 23032889
Fax: 617/279-1132

#### Southeast Area
Xicor, Inc.
201 Park Place
Suite 203
Altamonte Springs
Florida 32701
Phone: 305/767-8010
TWX: 510-100-7141
Fax: 305/767-8912

#### Mid-Atlantic Area
Xicor, Inc.
Patriot Square
39 Mill Plain Road
Danbury, Connecticut 06810
Phone: 203/743-1701
Telex: 230853137
Fax: 203/794-9501

#### North Central Area
Xicor, Inc.
953 North Plum Grove Road
Suite D
Schaumburg, Illinois 60173
Phone: 312/490-1310
TWX: 910-997-3663
Fax: 312/490-0637

#### South Central Area
Xicor, Inc.
9330 Amberton Parkway
Suite 137
Dallas, Texas 75243
Phone: 214/669-2022
Telex: 62027057
Fax: 214/644-5835

#### Southwest Area
Xicor, Inc.
4141 MacArthur Boulevard
Suite 205
Newport Beach, California 92660
Phone: 714/752-8700
TWX: 510-101-0110
Fax: 714/752-8634

#### Northwest Area
Xicor, Inc.
851 Buckeye Court
Milpitas, California 95035
Phone: 408/292-2022
TWX: 910-379-0033
Fax: 408/432-0640

### International Sales Offices

#### Northern Europe Area
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14 Black Bourton Road
Carterton
Oxford OX8 3QA
United Kingdom
Phone: 44.993.844.435
Telex: 851838029
Fax: 44.993.841.029

#### Southern Europe Area
Xicor GmbH
Forsthausstrasse 1
D-8013 Haar bei Muenchen
West Germany
Phone: (49) 89/463089
Telex: 5213883
Fax: (49) 89/4605472

#### Far East Area
Xicor, Inc.
851 Buckeye Court
Milpitas, California 95035
USA
Phone: 408/432-8888
TWX: 910-379-0033
Fax: 408/432-0640
FEATURES

• LOW Power CMOS
  — 60 mA Active Current Max.
  — 200 µA Standby Current Max.
• Fast Write Cycle Times
  — 64-Byte Page Write Operation
  — Byte or Page Write Cycle: 5 ms Typical
  — Complete Memory Rewrite: 2.5 Sec. Typical
  — Effective Byte Write Cycle Time: 78 µs Typical
• Software Data Protection
• End of Write Detection
  — DATA Polling
  — Toggle Bit
• Simple Byte and Page Write
  — Single TTL Compatible WE Signal
  — Internally Latched Address and Data
  — Automatic Write Timing
• Upward Compatible with X2864A
• JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X28C256 is a 32K x 8 EPROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78 µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor EPROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.
X28C256, X28C256I

**ABSOLUTE MAXIMUM RATINGS**

<table>
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<tr>
<th>Parameter</th>
<th>Limit</th>
<th>Units</th>
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</thead>
<tbody>
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<td>Temperature Under Bias</td>
<td>-10°C to +85°C</td>
<td>X28C256</td>
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<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Voltage on any Pin with Respect to Ground</td>
<td>-1.0V to +7V</td>
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<tr>
<td>D.C. Output Current</td>
<td>5 mA</td>
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<tr>
<td>Lead Temperature (Soldering, 10 Seconds)</td>
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**D.C. OPERATING CHARACTERISTICS**

X28C256 TA = 0°C to +70°C, VCC = +5V ± 10%, unless otherwise specified.
X28C256I TA = -40°C to +85°C, VEE = +5V ± 10%, unless otherwise specified.

**POWER-UP TIMING**

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<th>Parameter</th>
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<td>tpuR(3)</td>
<td>Power-Up to Read Operation</td>
<td>100</td>
<td>μs</td>
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<td>tpuwC(3)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
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</table>

**CAPACITANCE**

TA = 25°C, f = 1.0 MHz, VCC = 5V

<table>
<thead>
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<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
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</thead>
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<td>Input/Output Capacitance</td>
<td>10</td>
<td>pF</td>
<td>V1/O = 0V</td>
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<td>C1IN(3)</td>
<td>Input Capacitance</td>
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<td>pF</td>
<td>V1N = 0V</td>
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**A.C. CONDITIONS OF TEST**

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<th>Parameter</th>
<th>Value</th>
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<td>Input Rise and Fall Times</td>
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<td>Input and Output Timing Levels</td>
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<td>Output Load</td>
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**MODE SELECTION**

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<th>CE</th>
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<td>H</td>
<td>Read</td>
<td>DOUT</td>
<td>Active</td>
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<td>H</td>
<td>X</td>
<td>X</td>
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<td>High Z</td>
<td>Standby</td>
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<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
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<td>—</td>
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<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
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</tbody>
</table>

**Notes:**
(1) Typical values are for TA = 25°C and nominal supply voltage.
(2) VI,L min. and VI,H max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.
**A.C. CHARACTERISTICS**

X28C256 \( T_A = 0^\circ C \) to +70\(^\circ C\), \( V_{CC} = +5V \pm 10\% \), unless otherwise specified.

X28C256I \( T_A = -40^\circ C \) to +85\(^\circ C\), \( V_{CC} = +5V \pm 10\% \), unless otherwise specified.

### Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X28C256-20</th>
<th>X28C256-25</th>
<th>X28C256</th>
<th>X28C256-35</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{RC} )</td>
<td>Read Cycle Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>100</td>
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<tr>
<td>( t_{CE} )</td>
<td>Chip Enable Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>100</td>
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<tr>
<td>( t_{AA} )</td>
<td>Address Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>100</td>
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<tr>
<td>( t_{OE} )</td>
<td>Output Enable Access Time</td>
<td>80</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>80</td>
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<tr>
<td>( t_{LZ}^{(4)} )</td>
<td>CE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( t_{OLZ}^{(4)} )</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( t_{HZ}^{(5)} )</td>
<td>CE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>( t_{OHZ}^{(5)} )</td>
<td>OE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>0</td>
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<tr>
<td>( t_{OH} )</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</table>

**Notes:**
- (4) \( t_{LZ} \) min. and \( t_{OLZ} \) min. are shown for reference only, they are periodically characterized and are not tested.
- (5) \( t_{HZ} \) max. and \( t_{OHZ} \) max. are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven. \( t_{HZ} \) min. and \( t_{OHZ} \) min. are shown for reference only, they are periodically characterized and are not tested.
**Write Cycle Limits**

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Typ.(6)</th>
<th>Max.</th>
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<td>Write Cycle Time</td>
<td></td>
<td>5</td>
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<td>ms</td>
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<td>tAS</td>
<td>Address Setup Time</td>
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<td>tAH</td>
<td>Address Hold Time</td>
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<td>ns</td>
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<td>tCH</td>
<td>Write Hold Time</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCW</td>
<td>CE Pulse Width</td>
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<td>100</td>
<td></td>
<td>ns</td>
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<tr>
<td>tOES</td>
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<td>10</td>
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<tr>
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<td>OE High Hold Time</td>
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<td>ns</td>
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<tr>
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<td>WE Pulse Width</td>
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<td>ns</td>
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<td>tWPH</td>
<td>WE High Recovery</td>
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<td>tDV</td>
<td>Data Valid</td>
<td></td>
<td>1</td>
<td></td>
<td>µs</td>
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<td>Data Hold</td>
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<tr>
<td>tDW</td>
<td>Delay to Next Write</td>
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<td>tBLC</td>
<td>Byte Load Cycle</td>
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<td>100</td>
<td>µs</td>
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</table>

**WE Controlled Write Cycle**

Note: (6) Typical values are for T_A = 25°C and nominal supply voltage.
**CE Controlled Write Cycle**

*For each successive write within the page write operation, A0–A14 should be the same or writes to an unknown address could occur.*

**Page Write Cycle**

*For each successive write within the page write operation, CE can be strobed LOW: e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.*

**Notes:**

1. Between successive byte writes within a page write operation, CE can be strobed LOW: e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

2. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram

ADDRESS

OE

WE

OE

I/O7

DIN = X  DOUT = X

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

Toggle Bit Timing Diagram

OE

WE

OE

I/O6

HIGH Z

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

SYMBOL TABLE

WAVEFORM  INPUTS  OUTPUTS

Must be steady  Will be steady

May change from Low to High  Will change from Low to High

May change from High to Low  Will change from High to Low

Don't Care: Changes State Not Known

Changes Allowed Center Line is High Impedance

N/A

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS

Addresses (A₀–A₁₄)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O₀–I/O₇)
Data is written to or read from the X28C256 through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X28C256.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X28C256 supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A₆ through A₁₄) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment

DATA Polling (I/O₇)
The X28C256 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₇ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O₇ will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

Toggle Bit (I/O₆)
The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O₆ will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA POLLING I/O
Figure 2a: DATA Polling Bus Sequence

Figure 2b: DATA Polling Software Flow

DATA Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.
THE TOGGLE BIT I/O

Figure 3a: Toggle Bit Bus Sequence

The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION
The X28C256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.
• Noise Protection—A WE pulse less than 20 ns will not initiate a write cycle.
• Default VCC Sense—All write functions are inhibited when VCC is ≤3V.
• Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION
The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/power-down operations through the use of external circuits. The host would then have open read and write access of the device once VCC was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM
Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: Once the three byte sequence is issued it must be followed by a valid byte or page write operation.
SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.
RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

Figure 5b: Software Sequence to Deactivate
Software Data Protection

WRITE DATA AA TO ADDRESS 5555
WRITE DATA 55 TO ADDRESS 2AAA
WRITE DATA 80 TO ADDRESS 5555
WRITE DATA AA TO ADDRESS 5555
WRITE DATA 55 TO ADDRESS 2AAA
WRITE DATA 20 TO ADDRESS 5555

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E2PROM programmer, the following six step algorithm will reset the internal protection circuit. After $t_{WC}$, the X28C256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.
SYSTEM CONSIDERATIONS
Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM
Normalized Active Supply Current vs. Ambient Temperature

Normalized Standby Supply Current vs. Ambient Temperature

V_{CC} = 5.0V
### ORDERING INFORMATION

#### 256K $E^2$PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
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</thead>
<tbody>
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**Key:**

† = Blank = Commercial = 0°C to +70°C  
I = Industrial = −40°C to +85°C  
M = Military = −55°C to +125°C  
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing  
P = 28-Lead Plastic DIP  
D = 28-Lead Cerdip  
C = Side Braze  
F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H  
F2 = 28-Lead Ceramic Flat Pack for X28256 and X28C256  
K = 28-Pin Ceramic Pin Grid Array  
J = 32-Lead J-Hook Plastic Leaded Chip Carrier  
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)  
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)
### ORDERING INFORMATION

256K E²PROMs (Continued)

<table>
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<td>X28C256J-20</td>
<td>32768 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>†</td>
<td>200 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C256J-25</td>
<td>32768 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>†</td>
<td>250 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C256J</td>
<td>32768 x 8</td>
<td>S P D C F1 F2 K J E G</td>
<td>†</td>
<td>300 ns</td>
<td>CMOS</td>
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<td>I</td>
<td>350 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

**Key:**
- † = Blank = Commercial = 0°C to +70°C
- I = Industrial = −40°C to +85°C
- M = Military = −55°C to +125°C
- T = Ultra High Temp. = 0°C to +150°C
- S = Plastic Small Outline Gull Wing
- P = 28-Lead Plastic DIP
- D = 28-Lead Cerdip
- C = Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
- F2 = 28-Lead Ceramic Flat Pack for X28256 and X28C256
- K = 28-Pin Ceramic Pin Grid Array
- J = 32-Lead J-Hook Plastic Leaded Chip Carrier
- E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)
ORDERING INFORMATION

256K E²PROMs (Continued)

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
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<tr>
<td>X28C256E-20</td>
<td>32768 x 8</td>
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<td>†</td>
<td>200 ns</td>
<td>CMOS</td>
<td>Standard</td>
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<tr>
<td>X28C256E-25</td>
<td>32768 x 8</td>
<td></td>
<td>†</td>
<td>250 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C256E</td>
<td>32768 x 8</td>
<td></td>
<td>†</td>
<td>300 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C256E-35</td>
<td>32768 x 8</td>
<td></td>
<td>†</td>
<td>350 ns</td>
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<td>Standard</td>
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<td>X28C256EI-20</td>
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<td></td>
<td>I</td>
<td>200 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C256EI-25</td>
<td>32768 x 8</td>
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<td>I</td>
<td>250 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C256EI</td>
<td>32768 x 8</td>
<td></td>
<td>I</td>
<td>300 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C256EI-35</td>
<td>32768 x 8</td>
<td></td>
<td>I</td>
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LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

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U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labelling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X28256 AND X28C256
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: LEADS 4, 12, 18 & 26

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
# Sales Offices

## U.S. Sales Offices

### Northeast Area
Xicor, Inc.
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91 Montvale Avenue
Stoneham, Massachusetts 02180
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Fax: 617/279-1132

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Fax: 305/767-8912

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Telex: 230853137
Fax: 203/794-9501

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Schaumburg, Illinois 60173
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TWX: 910-997-3663
Fax: 312/490-0637

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Dallas, Texas 75243
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Telex: 62027057
Fax: 214/644-5835

### Southwest Area
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4141 MacArthur Boulevard
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Newport Beach, California 92660
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TWX: 510-101-0110
Fax: 714/752-8634

### Northwest Area
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851 Buckeye Court
Milpitas, California 95035
Phone: 408/292-2011
TWX: 910-379-0033
Fax: 408/432-0640

## International Sales Offices

### Northern Europe Area
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Carterton
Oxford OX8 3QA
United Kingdom
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Telex: 851838029
Fax: 44.993.841.029

### Southern Europe Area
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Forsthausstrasse 1
D8013 Haar bei Muenchen
West Germany
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Telex: 8415213883
Fax: 49.89.460.5472

### Far East Area
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851 Buckeye Court
Milpitas, California 95035
USA
Phone: 408/432-8888
TWX: 910-379-0033
Fax: 408/432-0640
FEATURES

- **LOW Power CMOS**
  - 60 mA Active Current Max.
  - 200 µA Standby Current Max.
- **Fast Write Cycle Times**
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 2.5 Sec. Typical
- **Software Data Protection**
- **End of Write Detection**
  - DATA Polling
  - Toggle Bit
- **Simple Byte and Page Write**
  - Single TTL Compatible WE Signal
  - Internally Latched Address and Data
  - Automatic Write Timing
- **Upward Compatible with X2864A**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

The Xicor X28C256 is a 32K x 8 E2PROM, fabricated with Xicor’s proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78 µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor’s hardware write protect capability.

Xicor E2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.
### Absolute Maximum Ratings*

- Temperature Under Bias: -65°C to +135°C
- Storage Temperature: -65°C to +150°C
- Voltage on any Pin with Respect to Ground: -1.0V to +7V
- D.C. Output Current (Soldering, 10 Seconds): 0.5 mA
- Lead Temperature: -1.0V to +7V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D.C. Operating Characteristics

**TA = -55°C to +125°C, VCC = +5V ±10%, unless otherwise specified.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
</table>
| Icc    | VCC Current (Active) (TTL Inputs) | Min. Typ. Max. | mA | \( \overline{CE} = \overline{OE} = V_{IL}, WE = V_{IH} \)  
All I/O’s = Open  
Address Inputs = TTL Levels @ f = 5 MHz |
| Isb1   | VCC Current (Standby) (TTL Inputs) | 2 | mA | \( \overline{CE} = V_{IH}, \overline{OE} = V_{IL} \)  
All I/O’s = Open  
Other Inputs = VIH |
| Isb2   | VCC Current (Standby) (CMOS Inputs) | 100 | 200 | \( \mu A \) | \( \overline{CE} = V_{CC} - 0.3V, \overline{OE} = V_{IL} \)  
All I/O’s = Open  
Other Inputs = VCC |
| Ii1    | Input Leakage Current | 10 | µA | \( V_{IN} \) = GND to VCC |
| Ii0    | Output Leakage Current | 10 | µA | \( V_{OUT} \) = GND to VCC, \( CE = V_{IH} \) |
| Vih(2) | Input High Voltage | -1.0 | 2.0 | V |
| Vll(2) | Input Low Voltage | 0.8 | V |
| Vol    | Output Low Voltage | 2.4 | V | \( I_{OL} \) = 2.1 mA |
| Voh    | Output High Voltage | 0.4 | V | \( I_{OH} \) = -400 µA |

### Power-Up Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TpuR(3)</td>
<td>Power-Up to Read Operation</td>
<td>100</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>TpuW(3)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

### Capacitance

**TA = 25°C, f = 1.0 MHz, VCC = 5V**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1/C(3)</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td>pF</td>
<td>( V_{I/O} = 0V )</td>
</tr>
<tr>
<td>C1/N(3)</td>
<td>Input Capacitance</td>
<td>6</td>
<td>pF</td>
<td>( V_{IN} = 0V )</td>
</tr>
</tbody>
</table>

### A.C. Conditions of Test

- Input Pulse Levels: 0V to 3.0V
- Input Rise and Fall Times: 10 ns
- Input and Output Timing Levels: 1.5V
- Output Load: 1 TTL Gate and \( C_L = 100 \) pF

### Mode Selection

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>DOUT</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>DIN</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Notes:**

1. Typical values are for \( T_A = 25°C \) and nominal supply voltage.
2. \( V_{IL} \) min. and \( V_{IH} \) max. are for reference only and are not tested.
3. This parameter is periodically sampled and not 100% tested.
A.C. CHARACTERISTICS

\[ T_A = -55^\circ C \text{ to } +125^\circ C, \quad V_{CC} = +5V \pm 10\%, \text{ unless otherwise specified.} \]

**Read Cycle Limits**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X28C256M-20</th>
<th>X28C256M-25</th>
<th>X28C256M</th>
<th>X28C256M-35</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{RC})</td>
<td>Read Cycle Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>(t_{CE})</td>
<td>Chip Enable Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>(t_{AA})</td>
<td>Address Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>(t_{OE})</td>
<td>Output Enable Access Time</td>
<td>80</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>(t_{LZ}^{(4)})</td>
<td>CE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>(t_{OLZ}^{(4)})</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>(t_{HZ}^{(5)})</td>
<td>CE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>(t_{OHZ}^{(5)})</td>
<td>OE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>(t_{OH})</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Read Cycle**

**Notes:**

(4) \(t_{LZ}\) min. and \(t_{OLZ}\) min. are shown for reference only, they are periodically characterized and are not tested.

(5) \(t_{HZ}\) max. and \(t_{OHZ}\) max. are measured from the point when \(CE\) or \(OE\) return high (whichever occurs first) to the time when the outputs are no longer driven. \(t_{HZ}\) min. and \(t_{OHZ}\) min. are shown for reference only, they are periodically characterized and are not tested.
Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(6)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td></td>
<td>5</td>
<td>10</td>
<td>ms</td>
</tr>
<tr>
<td>tAS</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCS</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCH</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCW</td>
<td>OE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOES</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tOEH</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWP</td>
<td>WE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tWPH</td>
<td>WE High Recovery</td>
<td>200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDV</td>
<td>Data Valid</td>
<td>1</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDW</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tBLC</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td></td>
<td>100</td>
<td>µs</td>
</tr>
</tbody>
</table>

Note: (6) Typical values are for TA = 25°C and nominal supply voltage.
**CE Controlled Write Cycle**

![Diagram of CE Controlled Write Cycle]

**Page Write Cycle**

![Diagram of Page Write Cycle]

*Notes:*

(7) Between successive byte writes within a page write operation, OE can be strobed LOW: e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram

ADDRESS

I/O

- Must be steady
- May change from Low to High
- May change from High to Low
- Don't Care: Changes Allowed
- N/A

WAVEFORM

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>steady</td>
<td>Will be steady</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Will change from Low to High</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Will change from High to Low</td>
<td></td>
</tr>
<tr>
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<tr>
<td></td>
<td>Center Line is High Impedance</td>
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Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS

Addresses (A0–A14)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O0–I/O7)
Data is written to or read from the X28C256 through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X28C256.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X28C256 supports both CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A6 through A14) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

Write Operation Status Bits
The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment

DATA Polling (I/O7)
The X28C256 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O7 will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

Toggle Bit (I/O6)
The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.
The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION
The X28C256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

• Noise Protection—A WE pulse less than 20 ns will not initiate a write cycle.
• Default VCC Sense—All write functions are inhibited when VCC is ≤ 3V.
• Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION
The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once VCC was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM
Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: Once the three byte sequence is issued it must be followed by a valid byte or page write operation.
SOFTWARE DATA PROTECTION

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.
RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

Figure 5b: Software Sequence to Deactivate Software Data Protection

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After $t_{WC}$, the X28C256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.
SYSTEM CONSIDERATIONS

Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM
Normalized Active Supply Current
vs. Ambient Temperature

![Normalized Active Supply Current vs. Ambient Temperature Graph]

Normalized Standby Supply Current
vs. Ambient Temperature

![Normalized Standby Supply Current vs. Ambient Temperature Graph]
**X28C256M**

**ORDERING INFORMATION**

256K E²PROMs

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Key:
- † = Blank = Commercial = 0°C to +70°C
- I = Industrial = -40°C to +85°C
- M = Military = -55°C to +125°C
- T = Ultra High Temp. = 0°C to +150°C
- S = Plastic Small Outline Gull Wing
- P = Plastic DIP
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- C = Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
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Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor's products are not authorized for use as critical components in life support devices or systems. In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F2

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X28256 AND X28C256
PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

NOTE: LEADS 4, 12, 18 & 26

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

**NOTES:**

1. **Dimensions:** All dimensions are in inches (in parentheses, in millimeters).
2. **Tolerance:** ±1% with a minimum limit of ±0.005 (0.127)

---

**Dimensions:**

- **Dimensional Tolerances:** ±0.005 (0.127)
- **Material Thickness:** 0.040 (1.02) x 45° Referenced
- **BSC (Before Soldering Curtain):** 0.050 (1.27) ft
- **Package Outline:** 0.028 (0.71)
- **Number of Pins:** 32

---

**Pin 1 Index Corner:**

- **Offset:** 0.458 (11.63) ft
- **Dimensional Tolerances:** ±0.005 (0.127)

---

**Material Thickness:**

- **Material Thickness:** 0.040 (1.02) x 45° Referenced
- **BSC (Before Soldering Curtain):** 0.050 (1.27)
- **Package Outline:** 0.028 (0.71)
- **Number of Pins:** 32

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**Pin 1 Index Corner:**

- **Offset:** 0.458 (11.63) ft
- **Dimensional Tolerances:** ±0.005 (0.127)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS
Sales Offices

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Requirements for Chip Erase

Chip erase functionality will be guaranteed via C-Spec only. Add C6767 to Xicor part number when ordering.

Description

The X28C256MB may be erased (all bits cleared to logic "1") by two different methods. Both erasure methods clear the device within 10 ms. Because both methods employ Fowler-Nordheim Tunneling vs. Avalanche Programming, previously written data is not recoverable; thus, providing a method for maintaining security of proprietary information.

The first method is similar to that employed on earlier generations of E²PROMs requiring the application of V_{OE} to the OE pin. Although a high voltage is applied to the pin, it is not coupled internally into the device. The voltage is sensed as being greater than V_{IH} and in conjunction with CE and WE LOW initiates an internal erase cycle. The voltages required to perform the actual erase operation are developed and controlled internally.

The second method of erasure is an extension of the Software Data Protection command sequence. It is a 5V only operation; thereby, eliminating the need for dual voltages within a system. Once the command sequence is issued by the host, the X28C256MB will automatically complete the erasure of the device within 10 ms.
### A.C. CHIP ERASE CHARACTERISTICS

$T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = +5V \pm 10\%$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OE}$</td>
<td>Output Enable Voltage</td>
<td>+14</td>
<td>+16</td>
</tr>
<tr>
<td>$t_{CS}$</td>
<td>CE to WE Setup Time</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$t_{DS}$</td>
<td>Data to WE Setup Time</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>Data Hold after WE High</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$t_{WP}$</td>
<td>Write Enable Pulse Width</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>$t_{CH}$</td>
<td>WE High to CE Hold Time</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$t_{OES(1)}$</td>
<td>$V_{OE}$ to WE Setup Time</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$t_{OEH(1)}$</td>
<td>$V_{OE}$ Hold Time</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$t_{WC}$</td>
<td>Erase Cycle Time</td>
<td></td>
<td>10</td>
</tr>
</tbody>
</table>

#### Chip Erase Cycle

![Chip Erase Cycle Diagram](image)

**Note:** (1) $t_{OES}$ and $t_{OEH}$ guaranteed by design, not 100% tested.
Note: 5V only erase function timings are referenced to the WE or CE inputs, whichever is last to go LOW, and the WE or CE inputs, whichever is first to go HIGH.

The command sequence must conform to the page write timing.

Refer to the X28C256M data sheet for write timing parameters.

Write protection is set after 5V Only Chip Erase.
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DESCRIPTION

The Xicor X28C256B is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C256B is a 5V only device. The X28C256B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256B supports a 64-byte page write operation, effectively providing a 78 µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256B also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256B includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.
X28C256B, X28C256BI

**ABSOLUTE MAXIMUM RATINGS**

*Temperature Under Bias*
- X28C256B: -10°C to +85°C
- X28C256BI: -65°C to +135°C

*Storage Temperature*
- -65°C to +150°C

*Voltage on any Pin with Respect to Ground*
- X28C256B: -1.0V to +7V
- X28C256BI: -1.0V to +7V

*D.C. Output Current (Soldering, 10 Seconds)*
- 5 mA

*COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. OPERATING CHARACTERISTICS**

X28C256B: TA = 0°C to +70°C, VCC = +5V ±10%, unless otherwise specified.
X28C256BI: TA = -40°C to +85°C, VCC = +5V ±10%, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>VCC Current (Active)</td>
<td>60 mA</td>
<td></td>
<td>CE = OE = VIH, WE = VIH</td>
</tr>
<tr>
<td></td>
<td>(TTL Inputs)</td>
<td></td>
<td></td>
<td>All I/O’s = Open</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Address Inputs = TTL Levels @ f = 5 MHz</td>
</tr>
<tr>
<td>ISB1</td>
<td>VCC Current (Standby)</td>
<td>2 μA</td>
<td></td>
<td>CE = VIH, OE = VIH</td>
</tr>
<tr>
<td></td>
<td>(TTL Inputs)</td>
<td></td>
<td></td>
<td>All I/O’s = Open, Other Inputs = VIH</td>
</tr>
<tr>
<td>ISB2</td>
<td>VCC Current (Standby)</td>
<td>100 200 μA</td>
<td></td>
<td>CE = VCC - 0.3V, OE = VIH</td>
</tr>
<tr>
<td></td>
<td>(CMOS Inputs)</td>
<td></td>
<td></td>
<td>All I/O’s = Open, Other Inputs = VCC</td>
</tr>
<tr>
<td>ILI</td>
<td>Input Leakage Current</td>
<td>10 μA</td>
<td></td>
<td>VIN = GND to VCC</td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td>10 μA</td>
<td></td>
<td>VOUT = GND to VCC, CE = VIH</td>
</tr>
<tr>
<td>VIL(2)</td>
<td>Input Low Voltage</td>
<td>-1.0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH(2)</td>
<td>Input High Voltage</td>
<td>2.0 V</td>
<td></td>
<td>VCC + 1.0 V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4 V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**POWER-UP TIMING**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPU(3)</td>
<td>Power-Up to Read Operation</td>
<td>100 μs</td>
<td></td>
</tr>
<tr>
<td>tPW(3)</td>
<td>Power-Up to Write Operation</td>
<td>5 ms</td>
<td></td>
</tr>
</tbody>
</table>

**CAPACITANCE**

TA = 25°C, f = 1.0 MHz, VCC = 5V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1/O(3)</td>
<td>Input/Output Capacitance</td>
<td>10 pF</td>
<td></td>
<td>V1/O = 0V</td>
</tr>
<tr>
<td>C1IN(3)</td>
<td>Input Capacitance</td>
<td>6 pF</td>
<td></td>
<td>V1N = 0V</td>
</tr>
</tbody>
</table>

**A.C. CONDITIONS OF TEST**

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>0V to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and CL = 100 pF</td>
</tr>
</tbody>
</table>

**MODE SELECTION**

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>DOUT</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>DIN</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes: (1) Typical values are for TA = 25°C and nominal supply voltage.
(2) VIL min. and VIH max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.
X28C256B, X28C256BI

A.C. CHARACTERISTICS
X28C256B T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C256BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
<td></td>
</tr>
<tr>
<td>t_{RC}</td>
<td>Read Cycle Time</td>
<td>150</td>
<td>180</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CE}</td>
<td>Chip Enable Access Time</td>
<td>150</td>
<td>180</td>
<td>150</td>
<td>180</td>
<td>ns</td>
</tr>
<tr>
<td>t_{AA}</td>
<td>Address Access Time</td>
<td>150</td>
<td>180</td>
<td>150</td>
<td>180</td>
<td>ns</td>
</tr>
<tr>
<td>t_{OE}</td>
<td>Output Enable Access Time</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>t_{LZ}(4)</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{OLZ}(4)</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{HZ}(5)</td>
<td>OE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>t_{OHZ}(5)</td>
<td>OE High to High Z Output</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>t_{OH}</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
(4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.
(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.
### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.(^{(6)})</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_{WC})</td>
<td>Write Cycle Time</td>
<td>5</td>
<td>10</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>t(_{AS})</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{AH})</td>
<td>Address Hold Time</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{CS})</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{CH})</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{CW})</td>
<td>CE Pulse Width</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{OES})</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{OEH})</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{WP})</td>
<td>WE Pulse Width</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{WPH})</td>
<td>WE High Recovery</td>
<td>200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{DV})</td>
<td>Data Valid</td>
<td>1</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>t(_{DS})</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{DH})</td>
<td>Data Hold</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(_{DW})</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>t(_{BLC})</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td>100</td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

### WE Controlled Write Cycle

![Diagram of WE Controlled Write Cycle]

**Note:** \(^{(6)}\) Typical values are for \(T_A = 25°C\) and nominal supply voltage.
**CE Controlled Write Cycle**

- **ADDRESS**
  - $t_{AS}$
  - $t_{AH}$
  - $t_{CW}$
  - $t_{WP}$
  - $t_{DS}$
  - $t_{DH}$

- **CE**
  - $t_{DE}$
  - $t_{DEH}$

- **OE**
  - $t_{DES}$

- **WE**
  - $t_{CS}$
  - $t_{CH}$

- **DATA IN**
  - **DATA VALID**

- **DATA OUT**
  - HIGH Z

---

**Page Write Cycle**

- (7) **OE**
  - $t_{WP}$
  - $t_{BLC}$

- **CE**
  - $t_{WP}$
  - $t_{BLC}$

- **WE**
  - $t_{WP}$

- (8) **ADDRESS**
  - **LAST BYTE**

- **I/O**
  - BYTE 0
  - BYTE 1
  - BYTE 2
  - BYTE $n$
  - BYTE $n+1$
  - BYTE $n+2$

---

**Notes:**

(7) Between successive byte writes within a page write operation, OE can be strobed LOW; e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
**DATA Polling Timing Diagram**

ADDRESS: An

**Toggle Bit Timing Diagram**

*I/O6 beginning and ending state will vary, depending upon actual tWC.

**SYMBOL TABLE**

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td></td>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td></td>
<td>N/A</td>
<td>Center Line is High Impedance</td>
</tr>
</tbody>
</table>

**Note:** (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS

Addresses (A₀–A₁₄)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O₀–I/O₇)
Data is written to or read from the X28C256B through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X28C256B.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X28C256B supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C256B allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256B prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A₀ through A₁₄) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The X28C256B provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment

DATA Polling (I/O₇)
The X28C256B features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C256B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₇ (i.e., write data = 0xx xxxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O₇ will reflect true data. Note: If the X28C256B is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

Toggle Bit (I/O₆)
The X28C256B also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O₆ will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA POLLING I/O
Figure 2a: DATA Polling Bus Sequence

DATA Polling can effectively halve the time for writing to the X28C2568. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.
THE TOGGLE BIT I/Os

*Beginning and ending state of I/Os will vary.

The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C256B memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION

The X28C256B provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- **Noise Protection**—A WE pulse less than 20 ns will not initiate a write cycle.
- **Default VCC Sense**—All write functions are inhibited when VCC is ≤3V.
- **Write Inhibit**—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C2568 offers a software controlled data protection feature. The X28C256B is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/power-down operations through the use of external circuits. The host would then have open read and write access of the device once VCC was stable.

The X28C256B can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256B is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

**Note**: Once the three byte sequence is issued it must be followed by a valid byte or page write operation.
SOFTWARE DATA PROTECTION

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C256B will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256B will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.
In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After tWC, the X28C256B will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.
SYSTEM CONSIDERATIONS
Because the X28C256B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C256B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM

![Functional Diagram](image-url)
Normalized Active Supply Current vs. Ambient Temperature

Normalized Standby Supply Current vs. Ambient Temperature

\[ V_{CC} = 5.0V \]
X28C256B, X28C256BI

ORDERING INFORMATION

256K E²PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
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</thead>
<tbody>
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<td>Standard</td>
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<td>Standard</td>
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<td>I</td>
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<tr>
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<td>I</td>
<td>180 ns</td>
<td>CMOS</td>
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</table>

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C
S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)
ORDERING INFORMATION
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<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
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LIFE RELATED POLICY
In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.
1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
### Sales Offices

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Milpitas, California 95035  
USA  
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TWX: 910-379-0033  
Fax: 408/432-0640
**FEATURES**

- Low Power CMOS
  - 50 mA Active Current Max.
  - 500 μA Standby Current Max.
- High Speed Page Write Operation
- Fast Write Cycle Times
  - 256-Byte Page Size
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 2.5 Sec.
  - Effective Byte Write Cycle Time: 19 μs
- End of Write Detection
  - DATA Polling
  - Toggle Bit Testing
- Accommodates Multiprocessor Applications
- Software Data Protection
- JEDEC Approved Byte-Wide Pinout for DIPs

**DESCRIPTION**

The Xicor X28C010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19 μs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C010 also features DATA Polling and Toggle Bit test, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports the Software Data Protection option.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

**PIN CONFIGURATIONS**

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<thead>
<tr>
<th>SIDE BRAZE</th>
<th>LCC</th>
<th>PIN NAMES</th>
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<td>A15</td>
<td>A0–A16</td>
</tr>
<tr>
<td>A16 2</td>
<td>A14</td>
<td>/I/O7</td>
</tr>
<tr>
<td>A15 3</td>
<td>A13</td>
<td>/I/O6</td>
</tr>
<tr>
<td>A14 4</td>
<td>A12</td>
<td>/I/O5</td>
</tr>
<tr>
<td>/I/O4 5</td>
<td>A11</td>
<td>/I/O4</td>
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<td>/I/O3 6</td>
<td>A10</td>
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**ABSOLUTE MAXIMUM RATINGS**

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<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
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<tbody>
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<td>+85°C</td>
<td>°C</td>
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</tr>
<tr>
<td>X28C0101</td>
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<td>+135°C</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
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<td>+150°C</td>
<td>°C</td>
<td></td>
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<tr>
<td>Voltage on any Pin with</td>
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<td>+7V</td>
<td>V</td>
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<tr>
<td>D.C. Output Current</td>
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<td>mA</td>
<td></td>
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<tr>
<td>Lead Temperature (Soldering, 10 seconds)</td>
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<td>300°C</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

*COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. OPERATING CHARACTERISTICS**

X28C010 \( T_A = 0^\circ \text{C} \) to +70°C, \( V_{CC} = +5V \pm 10\% \), unless otherwise specified.
X28C0101 \( T_A = -40^\circ \text{C} \) to +85°C, \( V_{CC} = +5V \pm 10\% \), unless otherwise specified.

**Symbol**  
**Parameter**  
**Limits**  
**Units**  
**Test Conditions**  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>CE = OE = V_{IL}, WE = V_{IH}</th>
<th>All I/O’s = Open</th>
<th>Address Inputs = TTL Levels @ f = 5 MHz</th>
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<td>I_{SB1}</td>
<td>V_{CC} Current (Standby) (TTL Inputs)</td>
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<td>mA</td>
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<td>All I/O’s = Open</td>
<td>Other Inputs = V_{IH}</td>
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</tr>
<tr>
<td>I_{SB2}</td>
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<td>( \mu A )</td>
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<td>Other Inputs = V_{CC}</td>
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<td>( \mu A )</td>
<td>V_{OUT} = GND to V_{CC}, OE = V_{IH}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IL}(1)</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IH}(1)</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>V_{CC} + 1.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>V</td>
<td>I_{OL} = 2.1 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>V</td>
<td>I_{OH} = -400 ( \mu A )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**POWER-UP TIMING**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{PU}(2)</td>
<td>Power-Up to Read Operation</td>
<td>100</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>t_{PW}(2)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

**CAPACITANCE**  
\( T_A = 25^\circ \text{C}, f = 1.0 \text{ MHz}, V_{CC} = 5V \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{I/O}(2)</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td>pF</td>
<td>V_{I/O} = 0V</td>
</tr>
<tr>
<td>C_{IN}(2)</td>
<td>Input Capacitance</td>
<td>10</td>
<td>pF</td>
<td>V_{IN} = 0V</td>
</tr>
</tbody>
</table>

**A.C. CONDITIONS OF TEST**

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>0V to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and ( C_L = 100 \text{ pF} )</td>
</tr>
</tbody>
</table>

**MODE SELECTION**

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>D_{OUT}</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>D_{IN}</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. \( V_{IL} \) min. and \( V_{IH} \) max. are for reference only and are not tested.
2. This parameter is periodically sampled and not 100% tested.
A.C. CHARACTERISTICS

X28C010 TA = 0°C to +70°C, VCC = +5V ± 10%, unless otherwise specified.
X28C010I TA = -40°C to +85°C, VCC = +5V ± 10%, unless otherwise specified.

Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X28C010-20</th>
<th>X28C010-25</th>
<th>X28C010</th>
<th>X28C010-35</th>
<th>X28C010I-20</th>
<th>X28C010I-25</th>
<th>X28C010I</th>
<th>X28C010I-35</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>tCE</td>
<td>Chip Enable Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>tAA</td>
<td>Address Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>tOE</td>
<td>Output Enable Access Time</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>100</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>tLZ(3)</td>
<td>CE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tOLZ(3)</td>
<td>OE Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tHZ(4)</td>
<td>CE High to High Z Output</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>tOHZ(4)</td>
<td>OE High to High Z Output</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>tOH</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

Read Cycle

Notes:

(3) tLZ min. and tOLZ min. are shown for reference only, they are periodically characterized and are not tested.
(4) tHZ max. and tOHZ max. are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven.
### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>twc</td>
<td>Write Cycle Time</td>
<td>10</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>tas</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tah</td>
<td>Address Hold Time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tcs</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tch</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tcw</td>
<td>CE Pulse Width</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>toes</td>
<td>OE High Setup Time</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>toeh</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>twp</td>
<td>WE Pulse Width</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>twph</td>
<td>WE High Recovery</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tdv</td>
<td>Data Valid</td>
<td>1</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tds</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tdh</td>
<td>Data Hold</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tdw</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>tblc</td>
<td>Byte Load Cycle</td>
<td>0.20</td>
<td>200</td>
<td>µs</td>
</tr>
</tbody>
</table>

**WE Controlled Write Cycle**

[Diagram showing the timing relationships between ADDRESS, CE, OE, WE, DATA IN, and DATA OUT.]
CE Controlled Write Cycle

Page Write Cycle

Notes:
(5) Between successive byte writes within a page write operation, OE can be strobed LOW; e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram

 SYMBOL TABLE

WAVEFORM | INPUTS                        | OUTPUTS                      |
----------|------------------------------|------------------------------|
            | Must be steady               | Will be steady               |
            | May change from Low to High  | Will change from Low to High |
            | May change from High to Low  | Will change from High to Low |
            | Don't Care: Changes Allowed  | Changing: State Not Known    |
            |                             | N/A Center Line is High Impedance |

*I/O<sub>8</sub> beginning and ending state will vary.

Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS

Addresses (A0–A16)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O0–I/O7)
Data is written to or read from the X28C010 through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X28C010.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X28C010 supports both CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C010 allows the entire memory to be written in 2.5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A8 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-five bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 200 μs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 200 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 200 μs.

Write Operation Status Bits
The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment

DATA Polling (I/O7)
The X28C010 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O7 (i.e., write data = 0xxxx xxxx, read data = 1xxxx xxxx). Once the programming cycle is complete, I/O7 will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

Toggle Bit (I/O6)
The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O6 will alternate between one and zero on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA Polling I/O

Figure 2a: DATA Polling Bus Sequence

DATA Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.
THE TOGGLE BIT I/Os

Figure 3a: Toggle Bit Bus Sequence

The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION
The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A WE pulse less than 10 ns will not initiate a write cycle.
- Default VCC Sense—All write functions are inhibited when VCC is ≤3.8V.
- Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION
The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/power-down operations through the use of external circuits. The host would then have open read and write access of the device once VCC was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM
Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.
Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.
RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

![Diagram](image)

Figure 5b: Software Sequence to Deactivate Software Data Protection

- WRITE DATA AA TO ADDRESS 5555
- WRITE DATA 55 TO ADDRESS 2AAA
- WRITE DATA 80 TO ADDRESS 5555
- WRITE DATA AA TO ADDRESS 5555
- WRITE DATA 55 TO ADDRESS 2AAA
- WRITE DATA 20 TO ADDRESS 5555

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After \( t_{WC} \), the X28C010 will be in standard operating mode.

**Note:** Once initiated, the sequence of write operations should not be interrupted.
SYSTEM CONSIDERATIONS

Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that \( \overline{CE} \) be decoded from the address bus and be used as the primary device selection input. Both \( \overline{OE} \) and \( WE \) would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling \( \overline{CE} \) will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 \( \mu \text{F} \) high frequency ceramic capacitor be used between \( V_{CC} \) and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 \( \mu \text{F} \) electrolytic bulk capacitor be placed between \( V_{CC} \) and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.
## ORDERING INFORMATION

### 1M E²PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X28C010C-20</td>
<td>131072 x 8</td>
<td>•</td>
<td>†</td>
<td>200 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010C-25</td>
<td>131072 x 8</td>
<td>•</td>
<td>†</td>
<td>250 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010C</td>
<td>131072 x 8</td>
<td>•</td>
<td>†</td>
<td>300 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010C-35</td>
<td>131072 x 8</td>
<td>•</td>
<td>†</td>
<td>350 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010CI-20</td>
<td>131072 x 8</td>
<td>•</td>
<td>I</td>
<td>200 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010CI-25</td>
<td>131072 x 8</td>
<td>•</td>
<td>I</td>
<td>250 ns</td>
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<td>Standard</td>
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<tr>
<td>X28C010CI</td>
<td>131072 x 8</td>
<td>•</td>
<td>I</td>
<td>300 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010CI-35</td>
<td>131072 x 8</td>
<td>•</td>
<td>I</td>
<td>350 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

**Key:**
- † = Blank = Commercial = 0°C to +70°C
- I = Industrial = -40°C to +85°C
- M = Military = -55°C to +125°C
- S = Plastic Small Outline Gull Wing
- P = Plastic DIP
- D = Cerdip
- C = 32-Lead Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
- F2 = Ceramic Flat Pack for X28256 and X28C256B
- K = Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = 44-Pad Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

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In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

32-LEAD SIDE BRAZE PACKAGE TYPE C

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
### Sales Offices

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**FEATURES**

- **Low Power CMOS**
  - 50 mA Active Current Max.
  - 500 µA Standby Current Max.
- **High Speed Page Write Operation**
- **Fast Write Cycle Times**
  - 256-Byte Page Size
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 2.5 Sec.
  - Effective Byte Write Cycle Time: 19 µs
- **End of Write Detection**
  - DATA Polling
  - Toggle Bit Testing
  - Accommodates Multiprocessor Applications
- **Software Data Protection**
- **JEDEC Approved Byte-Wide Pinout for DIPs**

**DESCRIPTION**

The Xicor X28C010 is a 128K x 8 E2PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19 µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C010 also features DATA Polling and Toggle Bit test, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports the Software Data Protection option.

Xicor E2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.
X28C010M

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ........................................... -65°C to +135°C
Storage Temperature .............................................. -65°C to +150°C
Voltage on any Pin with Respect to Ground ..................... -1.0V to +7V
D.C. Output Current .............................................. 5 mA
Lead Temperature (Soldering, 10 Seconds) ......................... 300°C

D.C. OPERATING CHARACTERISTICS

\[ T_A = -55°C \text{ to } +125°C, \ V_{CC} = +5V \pm 10\%, \text{ unless otherwise specified.} \]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min.</td>
<td>Max.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{CC}</td>
<td>( V_{CC} \text{ Current (Active)} ) (TTL Inputs)</td>
<td>50 mA</td>
<td></td>
</tr>
<tr>
<td>I_{SB1}</td>
<td>( V_{CC} \text{ Current (Standby)} ) (TTL Inputs)</td>
<td>3 mA</td>
<td></td>
</tr>
<tr>
<td>I_{SB2}</td>
<td>( V_{CC} \text{ Current (Standby)} ) (CMOS Inputs)</td>
<td>500 µA</td>
<td></td>
</tr>
<tr>
<td>I_{LI}</td>
<td>Input Leakage Current</td>
<td>10 µA</td>
<td></td>
</tr>
<tr>
<td>I_{LO}</td>
<td>Output Leakage Current</td>
<td>10 µA</td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Input Low Voltage</td>
<td>-1.0 V to +0.8 V</td>
<td></td>
</tr>
<tr>
<td>V_{IH}</td>
<td>Input High Voltage</td>
<td>+2.0 V to +1.0 V</td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Output Low Voltage</td>
<td>2.4 V</td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>Output High Voltage</td>
<td>0.4 V</td>
<td></td>
</tr>
</tbody>
</table>

Test Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( CE = \overline{OE} = V_{IL}, \ \overline{WE} = V_{IH} )</td>
<td>All I/O's = Open \nAddress Inputs = TTL Levels ( @ f = 5 \text{ MHz} )</td>
</tr>
</tbody>
</table>
| \( CE = V_{IH}, \ \overline{OE} = V_{IL} \) | All I/O's = Open, Other Inputs = \( V_{IH} \)
| \( CE = V_{CC} - 0.3V, \ OE = V_{IL} \) | All I/O's = Open, Other Inputs = \( V_{CC} \)
| \( V_{IN} = \text{GND to } V_{CC} \) | \( V_{OUT} \) = \( V_{CC} \), \( CE = V_{IH} \)

POWER-UP TIMING

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{PUR}(2)</td>
<td>Power-Up to Read Operation</td>
<td>100</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>t_{PLWU}(2)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

CAPACITANCE \( T_A = 25°C, f = 1.0 \text{ MHz}, V_{CC} = 5V \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{V/O}(2) )</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>( C_{IN}(2) )</td>
<td>Input Capacitance</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST

| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | \( 1 \text{ TTL Gate and } C_L = 100 \text{ pF} \) |

MODE SELECTION

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>D_{OUT}</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>D_{IN}</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes: (1) \( V_{IL} \) min. and \( V_{IH} \) max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
A.C. CHARACTERISTICS

\[ T_A = -55^\circ C \text{ to } +125^\circ C, \ V_{CC} = +5V \pm 10\%, \text{ unless otherwise specified.} \]

Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X28C010M-20</th>
<th>X28C010M-25</th>
<th>X28C010M</th>
<th>X28C010M-35</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{RC} )</td>
<td>Read Cycle Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CE} )</td>
<td>Chip Enable Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AA} )</td>
<td>Address Access Time</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OE} )</td>
<td>Output Enable Access Time</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{LZ}^{(3)} )</td>
<td>( \overline{CE} ) Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OLZ}^{(3)} )</td>
<td>( \overline{OE} ) Low to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{HZ}^{(4)} )</td>
<td>( \overline{CE} ) High to High Z Output</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OHZ}^{(4)} )</td>
<td>( \overline{OE} ) High to High Z Output</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OH} )</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes: (3) \( t_{LZ} \) min. and \( t_{OLZ} \) min. are shown for reference only, they are periodically characterized and are not tested.

(4) \( t_{HZ} \) max. and \( t_{OHZ} \) max. are measured from the point when \( \overline{CE} \) or \( \overline{OE} \) return high (whichever occurs first) to the time when the outputs are no longer driven.
## Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{WC} )</td>
<td>Write Cycle Time</td>
<td>10</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_{AS} )</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{AH} )</td>
<td>Address Hold Time</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CS} )</td>
<td>Write Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CH} )</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CW} )</td>
<td>( CE ) Pulse Width</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OES} )</td>
<td>( OE ) High Setup Time</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{OEH} )</td>
<td>( OE ) High Hold Time</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WP} )</td>
<td>( WE ) Pulse Width</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WPH} )</td>
<td>( WE ) High Recovery</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DV} )</td>
<td>Data Valid</td>
<td>1</td>
<td></td>
<td>( \mu )S</td>
</tr>
<tr>
<td>( t_{DS} )</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DH} )</td>
<td>Data Hold</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DW} )</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td>( \mu )S</td>
</tr>
<tr>
<td>( t_{BLC} )</td>
<td>Byte Load Cycle</td>
<td>0.20</td>
<td>200</td>
<td>( \mu )S</td>
</tr>
</tbody>
</table>

---

## WE Controlled Write Cycle

The diagram illustrates the timing sequence for a WE-controlled write cycle, showing the interplay of address, control signals (\( CE \), \( OE \), \( WE \)), and data signals (\( DATA \) in, \( DATA \) out). Key points include
- \( t_{AS} \): Address Setup Time
- \( t_{AH} \): Address Hold Time
- \( t_{CS} \): Write Setup Time
- \( t_{CH} \): Write Hold Time
- \( t_{CW} \): \( CE \) Pulse Width
- \( t_{OES} \): \( OE \) High Setup Time
- \( t_{OEH} \): \( OE \) High Hold Time
- \( t_{WP} \): \( WE \) Pulse Width
- \( t_{WPH} \): \( WE \) High Recovery
- \( t_{DV} \): Data Valid
- \( t_{DS} \): Data Setup
- \( t_{DH} \): Data Hold
- \( t_{DW} \): Delay to Next Write
- \( t_{BLC} \): Byte Load Cycle

---

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CE Controlled Write Cycle

**ADDRESS**

**CE**

**OE**

**WE**

**DATA IN**

**DATA OUT**

HIGH Z

Page Write Cycle

(5) OE

(6) ADDRESS

I/O

BYTE 0  BYTE 1  BYTE 2  BYTE n  BYTE n+1  LAST BYTE

BYTE n+2

*For each successive write within the page write operation, A_9-A_{16} should be the same or writes to an unknown address could occur.*

**Notes:**

(5) Between successive byte writes within a page write operation, OE can be strobed LOW; e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
DATA Polling Timing Diagram

I/O 7

Toggle Bit Timing Diagram

*I/O 6 beginning and ending state will vary.

SYMBOL TABLE

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td>-</td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td>-</td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td>-</td>
<td>Don't Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td>-</td>
<td>Changes Allowed</td>
<td>Center Line is High Impedance</td>
</tr>
</tbody>
</table>

Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.
PIN DESCRIPTIONS

Addresses (A₀–A₁₆)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O₀–I/O₇)
Data is written to or read from the X28C010 through the I/O pins.

Write Enable (WE)
The Write Enable input controls the writing of data to the X28C010.

DEVICE OPERATION

Read
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X28C010 supports both CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C010 allows the entire memory to be written in 2.5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A₀ through A₁₆) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-five bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 200 μs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 200 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 200 μs.

Write Operation Status Bits
The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment

DATA Polling (I/O₇)
The X28C010 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₇ (i.e., write data = 0xxxx xxxx, read data = 1xxxx xxxx). Once the programming cycle is complete, I/O₇ will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

Toggle Bit (I/O₀)
The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O₀ will alternate between one and zero on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA POLLING I/O

Figure 2a: DATA Polling Bus Sequence

- DATA Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

Figure 2b: DATA Polling Software Flow
The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION
The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A WE pulse less than 10 ns will not initiate a write cycle.
- Default V CC Sense—All write functions are inhibited when V CC is ≤3.8V.
- Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION
The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once V CC was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM
Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.
Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.
In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E2PROM programmer, the following six step algorithm will reset the internal protection circuit. After $t_{WC}$, the X28C010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.
SYSTEM CONSIDERATIONS
Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between VCC and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.
## ORDERING INFORMATION

1M E²PROMs

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Package</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>X28C010CM-20</td>
<td>131072 x 8</td>
<td>⋄</td>
<td>M</td>
<td>200 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010CM-25</td>
<td>131072 x 8</td>
<td>⋄</td>
<td>M</td>
<td>250 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010CM</td>
<td>131072 x 8</td>
<td>⋄</td>
<td>M</td>
<td>300 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>X28C010CM-35</td>
<td>131072 x 8</td>
<td>⋄</td>
<td>M</td>
<td>350 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
</tbody>
</table>

**Key:**

- † = Blank
- Commercial = 0°C to + 70°C
- Industrial = −40°C to + 85°C
- Military = −55°C to + 125°C
- S = Plastic Small Outline Gull Wing
- P = Plastic DIP
- D = Cerdip
- C = 32-Lead Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
- F2 = Ceramic Flat Pack for X28C256 and X28C256B
- K = Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = 44-Pad Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

---

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

32-LEAD SIDE BRAZE PACKAGE TYPE C

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
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FEATURES

• High Density 1Megabit (128K x 8) E²PROM Module
• Access Time of 250 ns at -55°C to +125°C
• Base Memory Component: Xicor CMOS X28C256
• JEDEC Standard 32-Pin 600 Mil Wide Ceramic Side Braze Package
• Pin Compatible with the X28C010 1Megabit Monolithic CMOS E²PROM
• Fast Write Cycle Times Supported by:
  — Internal Program Cycle 10 ms Max.
  — 64-Byte Page
  — DATA Polling
  — Toggle Status Bit
• High Rel Module Available with:
  — 100% MIL-STD-883 Compliant Components
  — 100% Screening and MIL-STD-883 Processing of Modules
• Software Data Protection

DESCRIPTION

The XM28C010 is a high density 1Megabit E²PROM comprised of four X28C256 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28C010 is configured 128K x 8 bit and features the JEDEC approved pinout for byte-wide memories, compatible with the monolithic X28C010.

The XM28C010 is available in commercial, industrial and military temperature ranges. The military temperature range module is built with MIL-STD-883 Class B microcircuit components. In addition, after being assembled all High Rel modules undergo 100% screening.

The XM28C010 supports a 64-byte page write operation, this, combined with DATA Polling or Toggle Bit testing, effectively provides a 78 µs/byte write cycle, enabling the module memory array to be rewritten in 10 seconds.

The XM28C010 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28C010 provides the same high endurance and data retention as the base memory components.

FUNCTIONAL DIAGRAM
XM28C010

ABSOLUTE MAXIMUM RATINGS*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Under Bias</td>
<td>-65°C</td>
<td>135°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C</td>
<td>150°C</td>
</tr>
<tr>
<td>Voltage on any Pin with Respect to Ground</td>
<td>-1.0V</td>
<td>7V</td>
</tr>
<tr>
<td>D.C. Output Current</td>
<td>5 mA</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 Seconds)</td>
<td>300°C</td>
<td></td>
</tr>
</tbody>
</table>

D.C. OPERATING CHARACTERISTICS

XM28C010 \( T_A = 0°C \) to \( +75°C \), \( V_{CC} = +5V \) ± 10%, unless otherwise specified.

XM28C010I \( T_A = -40°C \) to \( +85°C \), \( V_{CC} = +5V \) ± 10%, unless otherwise specified.

XM28C010M \( T_A = -55°C \) to \( +125°C \), \( V_{CC} = +5V \) ± 10%, unless otherwise specified.

D.C. OPERATING CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{CC}</td>
<td>( V_{CC} ) Current (Active)</td>
<td>70 mA</td>
<td></td>
</tr>
<tr>
<td>I_{SB1}</td>
<td>( V_{CC} ) Current (Standby)</td>
<td>15 mA</td>
<td></td>
</tr>
<tr>
<td>I_{SB2}</td>
<td>( V_{CC} ) Current (Standby)</td>
<td>800 µA</td>
<td></td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Input Leakage Current</td>
<td>10 µA</td>
<td></td>
</tr>
<tr>
<td>I_{OL}</td>
<td>Output Leakage Current</td>
<td>10 µA</td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td>0.8</td>
</tr>
<tr>
<td>V_{IH}</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>( V_{CC} + 1.0 )</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>V_{OH}</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>V</td>
</tr>
</tbody>
</table>

TYPICAL POWER-UP TIMING

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{PUP}(2)</td>
<td>Power-Up to Read Operation</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>t_{PUP}(2)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

CAPACITANCE \( T_A = 25°C, f = 1.0 \) MHz, \( V_{CC} = 5V \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{I/O}(2)</td>
<td>Input/Output Capacitance</td>
<td>40</td>
<td>pF</td>
<td>( V_{I/O} = 0V )</td>
</tr>
<tr>
<td>C_{IN}(2)</td>
<td>Input Capacitance</td>
<td>24</td>
<td>pF</td>
<td>( V_{IN} = 0V )</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>0V to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>1 TTL Gate and ( C_L = 100 ) pF</td>
</tr>
</tbody>
</table>

MODE SELECTION

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>D_{OUT}</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>D_{IN}</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes: (1) Typical values are for \( T_A = 25°C \) and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
XM28C010

A.C. CHARACTERISTICS
XM28C010 TA = 0°C to +75°C, VCC = +5V ± 10%, unless otherwise specified.
XM28C010I TA = -40°C to +85°C, VCC = +5V ± 10%, unless otherwise specified.
XM28C010M TA = -55°C to +125°C, VCC = +5V ± 10%, unless otherwise specified.

Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>XM28C010-25</th>
<th>XM28C010</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>Min. 250</td>
<td>Max. 300</td>
<td>ns</td>
</tr>
<tr>
<td>tCE</td>
<td>Chip Enable Access Time</td>
<td>Min. 250</td>
<td>Max. 300</td>
<td>ns</td>
</tr>
<tr>
<td>tAA</td>
<td>Address Access Time</td>
<td>Min. 250</td>
<td>Max. 300</td>
<td>ns</td>
</tr>
<tr>
<td>tOE</td>
<td>Output Enable Access Time</td>
<td>Min. 100</td>
<td>Max. 100</td>
<td>ns</td>
</tr>
<tr>
<td>tLZ</td>
<td>CE Low to Active Output</td>
<td>Min. 0</td>
<td>Max. 0</td>
<td>ns</td>
</tr>
<tr>
<td>tOLZ</td>
<td>OE Low to Active Output</td>
<td>Min. 0</td>
<td>Max. 0</td>
<td>ns</td>
</tr>
<tr>
<td>tHZ(3)</td>
<td>CE High to High Z Output</td>
<td>Min. 0</td>
<td>Max. 100</td>
<td>ns</td>
</tr>
<tr>
<td>tOHZ(3)</td>
<td>OE High to High Z Output</td>
<td>Min. 0</td>
<td>Max. 100</td>
<td>ns</td>
</tr>
<tr>
<td>tOH</td>
<td>Output Hold from Address Change</td>
<td>Min. 0</td>
<td>Max. 0</td>
<td>ns</td>
</tr>
</tbody>
</table>

Read Cycle

Note: (3) tHZ and tOHZ are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven.
### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>WE Controlled Write</th>
<th>CE Controlled Write(^{(4)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{WC})</td>
<td>Write Cycle Time</td>
<td>10</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>(t_{AS})</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>(t_{AH})</td>
<td>Address Hold Time</td>
<td>150</td>
<td></td>
<td>175</td>
</tr>
<tr>
<td>(t_{CS})</td>
<td>Write Setup Time</td>
<td>25</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>(t_{CH})</td>
<td>Write Hold Time</td>
<td>0</td>
<td></td>
<td>25</td>
</tr>
<tr>
<td>(t_{CW})</td>
<td>CE Pulse Width</td>
<td>125</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>(t_{OES})</td>
<td>OE High Setup Time</td>
<td>1</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>(t_{OEH})</td>
<td>OE High Hold Time</td>
<td>10</td>
<td></td>
<td>35</td>
</tr>
<tr>
<td>(t_{WP})</td>
<td>WE Pulse Width</td>
<td>100</td>
<td></td>
<td>125</td>
</tr>
<tr>
<td>(t_{WPH})</td>
<td>WE High Recovery</td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>(t_{DV})</td>
<td>Data Valid</td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>(t_{DS})</td>
<td>Data Setup</td>
<td>50</td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>(t_{DH})</td>
<td>Data Hold</td>
<td>10</td>
<td></td>
<td>35</td>
</tr>
<tr>
<td>(t_{CW})</td>
<td>Delay to Next Write</td>
<td>10</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>(t_{BLC})</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td>100</td>
<td>1</td>
</tr>
</tbody>
</table>

### WE Controlled Write Cycle

![Diagram of WE Controlled Write Cycle](image)

**Note:** (4) Due to the inclusion of the decoder IC on board the module, the WE and CE write controlled timings will vary. When utilizing the CE controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a WE controlled write operation, CE must be a minimum of 125 ns to accommodate the additional setup time required.
**CE Controlled Write Cycle**

For each successive write within the page write operation, $A_0$-$A_{16}$ should be the same or writes to an unknown address could occur.

---

**Page Write Cycle**

*For each successive write within the page write operation, $A_0$-$A_{16}$ should be the same or writes to an unknown address could occur.*
DATA Polling Timing Diagram

Toggle Bit Timing Diagram

*Starting and ending state of $I/O_6$ will vary, depending upon actual $t_{WC}$. 
**PIN DESCRIPTIONS**

**Addresses (A₀–A₁₅)**
The Address inputs select an 8-bit memory location during a read or write operation.

**Chip Enable (CE)**
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced (see Note 4).

**Output Enable (OE)**
The Output Enable input controls the data output buffers and is used to initiate read operations.

**Data In/Data Out (I/O₀–I/O₇)**
Data is written to or read from the XM28C010 through the I/O pins.

**Write Enable (WE)**
The Write Enable input controls the writing of data to the XM28C010.

**DEVICE OPERATION**

**Read**
Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

**Write**
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The XM28C010 supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms (see Note 4).

**Page Write Operation**
The page write feature of the XM28C010 allows the entire memory to be written in 10 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the XM28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A₀ through A₁₅) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

**Write Operation Status Bits**
The XM28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

![Figure 1: Status Bit Assignment](image)

**DATA Polling (I/O₇)**
The XM28C010 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the XM28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₇ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O₇ will reflect true data. Note: If the XM28C010 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

**Toggle Bit (I/O₆)**
The XM28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O₆ will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.
DATA Polling can effectively halve the time for writing to the XM28C010. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.
The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple XM28C010 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.
HARDWARE DATA PROTECTION
The XM28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A WE pulse less than 20 ns will not initiate a write cycle.
- Default VCC Sense—All functions are inhibited when VCC is ≤3V.
- Write Inhibit—Holding OE LOW will prevent an inadvertent write cycle during power-on and power-off.

SOFTWARE DATA PROTECTION
The XM28C010 does provide the Software Data Protection (SOP) feature. Because the module is comprised of four discrete X28C256 LCCs, the algorithm will differ from the algorithm employed for the monolithic 1 Megabit X28C010.

The module is shipped from Xicor with the Software Data Protect NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once VCC is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described below.

SOFTWARE COMMAND SEQUENCE
A15 and A16 are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 4a and 4b. Because this involves writing to a nonvolatile bit the device will become protected after tWC has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 5a and 5b. This is a nonvolatile operation, and the host will have to wait a minimum of tWC before attempting to write new data.
SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.
RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

* A₁₅ & A₁₆ select one of four devices on the module.

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After \( t_{WC} \), the device will be in standard operating mode.
SYSTEM CONSIDERATIONS

Because the XM28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between VCC and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between VCC and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

SYMBOL TABLE

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td></td>
<td>May change from Low to High</td>
<td>Will change from Low to High</td>
</tr>
<tr>
<td></td>
<td>May change from High to Low</td>
<td>Will change from High to Low</td>
</tr>
<tr>
<td></td>
<td>Don’t Care: Changes Allowed</td>
<td>Changing: State Not Known</td>
</tr>
<tr>
<td></td>
<td>N/A</td>
<td>Center Line is High Impedance</td>
</tr>
</tbody>
</table>
XM28C010

Ordering Information

1 MEGABIT E² MODULES

<table>
<thead>
<tr>
<th>Device Order Number</th>
<th>Organization</th>
<th>Temp. Range</th>
<th>Access Time</th>
<th>Process Technology</th>
<th>Processing Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>XM28C010-25</td>
<td>131072 x 8</td>
<td>†</td>
<td>250 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>XM28C010I-25</td>
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<td>I</td>
<td>250 ns</td>
<td>CMOS</td>
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<tr>
<td>XM28C010M-25</td>
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<td>250 ns</td>
<td>CMOS</td>
<td>High Rel</td>
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<td>XM28C010</td>
<td>131072 x 8</td>
<td>†</td>
<td>300 ns</td>
<td>CMOS</td>
<td>Standard</td>
</tr>
<tr>
<td>XM28C010I</td>
<td>131072 x 8</td>
<td>I</td>
<td>300 ns</td>
<td>CMOS</td>
<td>Standard</td>
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<tr>
<td>XM28C010M</td>
<td>131072 x 8</td>
<td>M</td>
<td>300 ns</td>
<td>CMOS</td>
<td>High Rel</td>
</tr>
</tbody>
</table>

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

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In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
XM28C010

Packaging Information

32-PIN DUAL-IN-LINE PACKAGE
CERAMIC LEADLESS CHIP CARRIERS
ON SIDE BRAZED CERAMIC SUBSTRATE

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
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Please use this Xicor Data Book Supplement in conjunction with the Xicor 1988 Data Book, Stock No. 100-080, which contains additional product line information, product reliability reports and application notes.
**E²POT™ Digitally Controlled Potentiometer**

**FEATURES**
- Solid State Reliability
- Single Chip MOS Implementation
- Three Wire TTL Control
- Operates From Standard 5V Supply
- 99 Resistive Elements
  - Temperature Compensated
  - ±20% End to End Resistance Range
- 100 Wiper Tap Points
  - Wiper Position Digitally Controlled
  - Wiper Position Stored in Nonvolatile Memory Then Automatically Recalled on Power-Up
- 100 Year Wiper Position Retention
- 8 Pin Mini-DIP Package
- 14 Pin SOIC Package

**DESCRIPTION**

The Xicor X9MME is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

The X9MME is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element on the array is controlled by the CS, U/D, and INC inputs. The position of the wiper can be stored in nonvolatile memory and is recalled upon a subsequent power-up.

The resolution of the X9MME is equal to the maximum resistance value divided by 99. As an example; for the X9503 (50 kΩ) each tap point represents 505Ω.

Xicor E² products are designed and tested for applications requiring extended endurance. Refer to Xicor reliability reports for further endurance information.

**PIN NAMES**

- \( V_H \) - High Terminal of Pot
- \( V_W \) - Wiper Terminal of Pot
- \( V_L \) - Low Terminal of Pot
- \( V_{SS} \) - Ground
- \( V_{CC} \) - System Power
- U/D - Up/Down Control
- INC - Wiper Movement Control
- CS - Chip Select for Wiper Movement/Storage
- NC - No Connect

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Characteristics subject to change without notice
**X9MME, X9MMEI**

**ANALOG CHARACTERISTICS**

**Electrical Characteristics**

- **End to End Resistance Tolerance**: ± 20%
- **Power Rating at 25°C**
  - X9102, X9103, X9503 and X9104: 10 mW
  - X9102: 16 mW
- **Wiper Current**: ± 1 mA Max.
- **Typical Wiper Resistance**: 40 Ω at 1 mA
- **Typical Noise**
  - X9102: < -120 dB/Hz Ref: 1V
  - X9103, X9503 and X9104: < -95 dB/Hz Ref: 1V
- **Resolution**
  - Resistance: 1/0%
- **Linearity**
  - Absolute Linearity: ± 1.0 Ml(2)
  - Relative Linearity: ± 0.2 Ml(2)
- **Temperature Coefficient**
  - -40°C to + 85°C
    - X9102: ± 600 ppm/°C Typical
    - X9103, X9503 and X9104: ± 300 ppm/°C Typical
- **Wiper Adjustability**
  - Unlimited Wiper Adjustment (Volatile Mode While Chip is Selected)
  - Nonvolatile Storage of Wiper Position: 10,000 Cycles Typical

**Environmental Characteristics**

- **Temperature Range**
  - Operating X9MME: 0°C to + 70°C
  - X9MMEI: -40°C to + 85°C
  - Storage: -65°C to + 150°C

**D.C. OPERATING CHARACTERISTICS**

X9MME TA = 0°C to + 70°C, VCC = + 5V ± 10%, unless otherwise specified.
X9MMEI TA = -40°C to + 85°C, VCC = + 5V ± 10%, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td>Supply Current</td>
<td>Min.</td>
<td>Typ.(4)</td>
<td>Max.</td>
</tr>
<tr>
<td>Il</td>
<td>Input Leakage Current</td>
<td>-</td>
<td>±10</td>
<td>µA</td>
</tr>
<tr>
<td>Vih</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vil</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>Rw</td>
<td>Wiper Resistance</td>
<td>40</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Vvh(5)</td>
<td>Vh Voltage</td>
<td>-5.0</td>
<td>+5.0</td>
<td></td>
</tr>
<tr>
<td>Vvl(5)</td>
<td>Vl Voltage</td>
<td>-5.0</td>
<td>+5.0</td>
<td></td>
</tr>
<tr>
<td>Cin(6)</td>
<td>CS, INC, U/D, Input Capacitance</td>
<td>-</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**Notes:**
(1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

\[
\text{Absolute Linearity} = \left( V_{W(n)}(\text{actual}) - V_{W(n)}(\text{expected}) \right) \leq 1 \text{ Ml Max.}
\]

(2) 1 Ml = \( R_{TOT} / 99 \) or \( V_{H} - V_{L} / 99 \) = Minimum Increment.

(3) Relative Linearity is utilized to determine the actual change in voltage between successive tap position when used as a potentiometer. It is a measure of the error in step size.

\[
\text{Relative Linearity} = \left| V_{W(n+1)} - [V_{W(n)} + \text{Ml}] \right| \leq 0.2 \text{ Ml Max.}
\]

Typical values of Linearity are shown in Figures 3, 6, 9 and 12.

(4) Typical values are for TA = 25°C and nominal supply voltage.

(5) \( \Delta V \) for X9102: \( |V_{H} - V_{L}| \leq 4V. \Delta V \) for X9103, X9503 and X9104: \( |V_{H} - V_{L}| \leq 10V. \)

(6) This parameter is periodically sampled and not 100% tested.
A.C. CONDITIONS OF TEST

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>0V to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>10 ns</td>
</tr>
<tr>
<td>Input</td>
<td>1.5V</td>
</tr>
</tbody>
</table>

A.C. CHARACTERISTICS

X9MME $T_A = 0^\circ$C to $+70^\circ$C, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

X9MMEI $T_A = -40^\circ$C to $+85^\circ$C, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>$t_{CI}$</td>
<td>CS to INC Setup</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ID}$</td>
<td>INC High to U/D Change</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DI}$</td>
<td>U/D to INC Setup</td>
<td>2.9</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{IL}$</td>
<td>INC Low Period</td>
<td>1</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{IH}$</td>
<td>INC High Period</td>
<td>3</td>
<td>$\mu$s</td>
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<tr>
<td>$t_{IC}$</td>
<td>INC Inactive to CS Inactive</td>
<td>1</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{CPH}$</td>
<td>CS Deselect Time</td>
<td>20</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{IW}$</td>
<td>INC to $V_W$ Change</td>
<td>100 to 500</td>
<td>$\mu$s</td>
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</table>

A.C. Timing

**Note:** (7) Typical values are for $T_A = 25^\circ$C and nominal supply voltage.
PIN DESCRIPTIONS

**V<sub>H</sub>**
The high terminal of the X9MME is capable of handling an input voltage from -5V to +5V.

**V<sub>L</sub>**
The low terminal input is limited from -5V to +5V.

**V<sub>W</sub>**
The wiper terminal series resistance is typically less than 40Ω. The value of the wiper is controlled by the use of U/D and INC.

**Up/Down (U/D)**
The U/D input controls the direction of the wiper movement and the value of the nonvolatile counter.

**Increment (INC)**
The INC input is negative-edge triggered. Toggling INC will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/D input.

**Chip Select (CS)**
The device is selected when the CS input is LOW. The current counter value is stored in nonvolatile memory when CS is returned HIGH with INC HIGH.

DEVICE OPERATION
The INC, U/D and CS inputs control the movement of the wiper along the resistor array. HIGH to LOW transitions on INC, with CS LOW, increment (U/D = HIGH) or decrement (U/D = LOW) an internal counter. The output of the counter is decoded to position the wiper. When CS is brought HIGH the counter value is automatically stored in the nonvolatile memory. Upon power-up the nonvolatile memory contents are restored to the counter.

With the wiper at position 99, additional increments (U/D = HIGH) will not move the wiper. With the wiper at position 0, additional decrements (U/D = LOW) will not move the wiper.

The state of U/D may be changed while CS remains LOW, allowing a gross then fine adjustment during system calibration.

If V<sub>CC</sub> is removed while CS is LOW the contents of the nonvolatile memory may be lost.

The end to end resistance of the array will fluctuate once V<sub>CC</sub> is removed.

APPLICATIONS
The combination of a digital interface and nonvolatile memory in a silicon based trimmer pot provides many application opportunities that could not be addressed by either mechanical potentiometers or digital to analog circuits. The X9MME addresses and solves many issues that are of concern to designers of a wide range of equipment.

Consider the possibilities:

Automated assembly line calibration versus mechanical tweaking of potentiometers.

Protection against drift due to vibration or contamination.

Eliminate precise alignment of PWB mounted potentiometers with case access holes.

Eliminate unsightly access holes on otherwise aesthetically pleasing enclosures.

Product enhancements such as keyboard adjustment of volume or brightness control.

Front panel microprocessor controlled calibration of test instruments.

Remote location calibration via radio, modem or LAN link.

Calibration of hard to reach instruments in aircraft or other confined spaces.

APPLICATION CIRCUITS

**Application Circuit #1**

![Diagram 1](0039-4)

Approximating audio trim with external resistor.

**Application Circuit #2**

![Diagram 2](0039-5)

Utilizing the X9MME as a variable resistor.

**Note:** Maximum Wiper Current = 1 mA.
Figure 1: Typical Frequency Response for X9102

TEST CONDITIONS

- $V_{CC} = 5.0V$
- Temp. = Room
- Wiper @ Tap 50
- $V_H = 0.5V$ RMS
- Normalized (0 dB @ 1 KHz)
- Test Circuit #1

Figure 2: Typical Total Harmonic Distortion for X9102

TEST CONDITIONS

- $V_{CC} = 5.0V$
- Temp. = Room
- Wiper @ Tap 50
- $V_H = 2V$ RMS
- Test Circuit #1
Figure 3: Typical Linearity for X9102

TEST CONDITIONS
VCC = 5.0V
Temp. = Room
Test Circuit #2

KEY:
--- = ABSOLUTE
----- = RELATIVE

Figure 4: Typical Frequency Response for X9103

TEST CONDITIONS
VCC = 5.0V
Temp. = Room
Wiper @ Tap 50
VH = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1
Figure 5: Typical Total Harmonic Distortion for X9103

**TEST CONDITIONS**
- $V_{CC} = 5.0V$
- Temp. = Room
- Wiper @ Tap 50
- $V_H = 2V$ RMS
- Test Circuit #1

Figure 6: Typical Linearity for X9103

**TEST CONDITIONS**
- $V_{CC} = 5.0V$
- Temp. = Room
- Test Circuit #2

**KEY:**
- = ABSOLUTE
- = RELATIVE
**X9MME, X9MMEI**

**Figure 7: Typical Frequency Response for X9503**

![Graph showing typical frequency response for X9503](image)

**TEST CONDITIONS**
- $V_{CC} = 5.0V$
- Temp. = Room
- Wiper @ Tap 50
- $V_H = 0.5V$ RMS
- Normalized (0 dB @ 1 KHz)
- Test Circuit #1

**Figure 8: Typical Total Harmonic Distortion for X9503**

![Graph showing typical total harmonic distortion for X9503](image)

**TEST CONDITIONS**
- $V_{CC} = 5.0V$
- Temp. = Room
- Wiper @ Tap 50
- $V_H = 2V$ RMS
- Test Circuit #1
**X9MME, X9MMEI**

**Figure 9: Typical Linearity for X9503**

![Graph showing typical linearity for X9503](image)

**TEST CONDITIONS**
- $V_{CC} = 5.0V$
- Temp. = Room
- Test Circuit #2

**KEY:**
- \(\text{---} = \text{ABSOLUTE}\)
- \(\text{-----} = \text{RELATIVE}\)

**Figure 10: Typical Frequency Response for X9104**

![Graph showing typical frequency response for X9104](image)

**TEST CONDITIONS**
- $V_{CC} = 5.0V$
- Temp. = Room
- Wiper @ Tap 50
- $V_H = 0.5V$ RMS
- Normalized (0 dB @ 1 KHz)
- Test Circuit #1
Figure 11: Typical Total Harmonic Distortion for X9104

**TEST CONDITIONS**

- $V_{CC} = 5.0V$
- Temp. = Room
- Wiper @ Tap 50
- $V_H = 2V$ RMS
- Test Circuit #1

Figure 12: Typical Linearity for X9104

**TEST CONDITIONS**

- $V_{CC} = 5.0V$
- Temp. = Room
- Test Circuit #2

**KEY:**

- Dashed line = ABSOLUTE
- Solid line = RELATIVE
X9MME, X9MME1

Test Circuit #1

Test Circuit #2

Standard Parts

<table>
<thead>
<tr>
<th>Minimum Resistance</th>
<th>Wiper Increments</th>
<th>Maximum Resistance</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>40Ω</td>
<td>10.1Ω</td>
<td>1 KΩ</td>
<td>X9102</td>
</tr>
<tr>
<td>40Ω</td>
<td>101Ω</td>
<td>10 KΩ</td>
<td>X9103</td>
</tr>
<tr>
<td>40Ω</td>
<td>505Ω</td>
<td>50 KΩ</td>
<td>X9503</td>
</tr>
<tr>
<td>40Ω</td>
<td>1010Ω</td>
<td>100 KΩ</td>
<td>X9104</td>
</tr>
</tbody>
</table>

FUNCTIONAL DIAGRAM

- 7 BIT COUNTER
- NONVOLATILE MEMORY
- PROGRAMMING CONTROL AND POWER-ON DETECT
- WIPER POSITION DECODE
- TRANSFER LOGIC
- ARRAY
## ORDERING INFORMATION

**E²POTENTIOMETERS**

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<th>Device Order Number</th>
<th>Maximum Resistance</th>
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<th>P</th>
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<th>C</th>
<th>F1</th>
<th>F2</th>
<th>K</th>
<th>J</th>
<th>E</th>
<th>G</th>
<th>Temp. Range</th>
<th>Processing Level</th>
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</table>

**Key:**
- † = Blank = Commercial = 0°C to +70°C
- I = Industrial = -40°C to +85°C
- M = Military = -55°C to +125°C
- S = 14-Lead Plastic Small Outline Gull Wing
- P = 8-Lead Plastic DIP
- D = 8-Lead Cerdip
- C = Side Braze
- F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
- F2 = Ceramic Flat Pack for X28C256 and X28C256B
- K = Ceramic Pin Grid Array
- J = J-Hook Plastic Leaded Chip Carrier
- E = Ceramic Leadless Chip Carrier (Solder Seal)
- G = Ceramic Leadless Chip Carrier (Glass Frit Seal)
**ORDERING INFORMATION**

**E2POTENTIOMETERS (Continued)**

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<th>Device Order Number</th>
<th>Maximum Resistance</th>
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**LIFE RELATED POLICY**

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPES

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
PACKAGING INFORMATION

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
Sales Offices

U.S. Sales Offices

Northeast Area
Xicor, Inc.
Montvale Executive Park
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Fax: 617/279-1132

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Altamonte Springs
Florida 32701
Phone: 407/767-8010
TWX: 510-100-7141
Fax: 407/767-8912

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Xicor, Inc.
50 North Street
Danbury, Connecticut 06810
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Telex: 230853137
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Fax: 312/605-1316

South Central Area
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9330 Amberton Parkway
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Dallas, Texas 75243
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Telex: 62027057
Fax: 214/644-5835

Southwest Area
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4141 MacArthur Boulevard
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Newport Beach, California 92660
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Fax: 714/752-8634

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851 Buckeye Court
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Fax: 44.993.841.029

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Fax: (49) 89/4605472

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Fax: (03) 225-2319

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851 Buckeye Court
Milpitas, California 95035
USA
Phone: 408/432-8888
TWX: 910-379-0033
Fax: 408/432-0640
1990 Data Book Reservation Form

1. Is the information you received adequate?
   - Yes
   - No

2. What additional information do you need?

3. Have you been contacted by a Xicor sales representative?
   - Yes
   - No

4. If not, would you like a Xicor sales representative to call you?
   - Yes
   - No
   Phone No: ( ) Ext.

5. What distributor do you buy from?

6. What is your time requirement?
   - Immediate
   - 3-6 months
   - 1-3 months
   - 6-12 months

7. Please select the description below that best matches your interest and circle one number under each category.

   **A. My Job Function is:**
   1. Corporate Management
   2. Operations Management
   3. Engineering Management
   4. Components Engineer
   5. Design Engineer
   6. Purchasing
   7. Marketing
   8. Consultant
   9. Library
   10. Other

   **B. My Product Application is:**
   1. Industrial Control
   2. Commercial
   3. Military
   4. Computer
   5. Instrumentation
   6. Telecommunications
   7. Consumer
   8. Automotive
   9. Medical
   10. Other

   **C. My Primary Product Interest is:**
   1. Byte-Wide NOVRAMs
   2. Nibble-Wide NOVRAMs
   3. Serial NOVRAMs
   4. 4K, 16K, 64K PROMs
   5. 256K PROMs
   6. 1M PROMs
   7. Serial PROMs
   10. Other

   **D. My Primary Technology Interest is:**
   1. NMOS
   2. CMOS

Name _________________________ Title _________________________
Company ____________________________________________
Address ____________________________________________
City _____________________________ State ______ Zip __________
Country ____________________________ Country Code ____________

Thank You