XCELL

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THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS

XILINX®

The Programmable Logic Company℠

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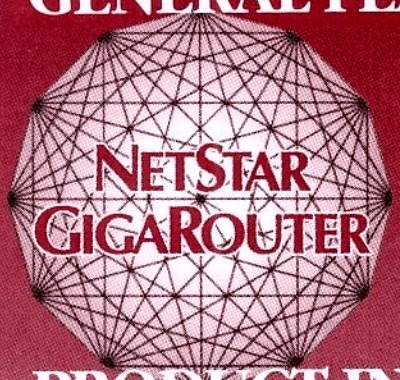

Customer Success Story:

NetStar

NetStar's GigaRouter™ an excellent example of a product which benefits from Xilinx FPGAs...

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PRODUCT INFORMATION

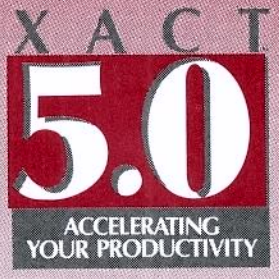
New Product:

BGA Packaging

The new Ball Grid Array will become the package of choice for applications requiring more than 200 pins..

See Page 10

DEVELOPMENT SYSTEMS



XACT 5.0

The exciting new release of the powerful XACT Development System is discussed in depth...

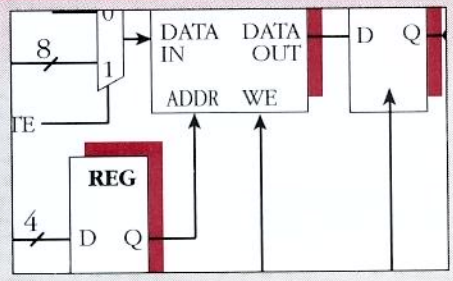
See Pages 17-23

DESIGN TIPS & HINTS

High-Speed RAM in XC4000

Implementing high-speed RAM in the XC4000 FPGA explained..

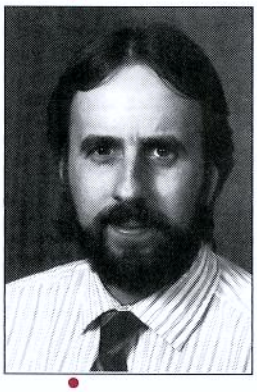
See Page 26



Keep Those Cards Coming

By BRADLY FAWCETT ◆ Editor

The next major release of the Xilinx design software, XACT® 5.0, will start shipping early in 1994, reflecting our continuing commitment to provide the most-advanced software tools for FPGA design.



As described elsewhere in this issue, XACT 5.0 adds many features to the Xilinx tool set, including improved place-and-route algorithms, Windows compatibility, incremental design tools for the XC4000 family, and X-BLOX support for the XC3000A family, to name but a few. However, the only Xilinx customers who will automatically receive this update have:

1) purchased their development system within the past year *and* sent in their software registration card, or
2) maintained their software support through the purchase of a software maintenance contract.

Thus, it is extremely important that you mail in the software registration card every time you receive a new software product from Xilinx. Registering each software purchase results in several benefits to you. First and foremost, it provides us with the name and address of the person who should receive future software updates. Since almost all of our development system products are sold through distributors, the software registration card often is the only easy way for us to identify the user who needs to receive the updates. Furthermore, your software registration provides you with access to technical support facilities such as the telephone "hotline" and Xilinx bulletin board (and helps us to serve you better when you do call for assistance). Registering your software also automatically adds your name to the mailing list for this newsletter. (I realize that I may be "preaching to the choir" here; if you are receiving this newsletter, chances are that it's because you sent in your software registration card.)

Occasionally, registration cards also are included in software updates. This helps us verify that the update was delivered and the registration information is current. So please be diligent about mailing those back to us, also.

We ship a major update to the core implementation tools (APR and PPR) at least once every 18 months. Other updates — support for new FPGA products and speed grades, improved netlist interfaces and the occasional "bug fix" — are distributed much more frequently. Most are shipped to the affected customers, while others are placed on the bulletin board. The first year of updates is included in the purchase price of the original software license; again, send in your registration cards so we know where to ship the updates! After the first year, you can ensure the continual flow of new updates by purchasing software maintenance contracts.

> *"It is extremely important that you mail in the software registration card every time you receive a new software product from Xilinx."*

About 60 days before your yearly software maintenance contract expires, the

Continued on page 4

XCELL

Please direct all inquiries, comments and submissions to:

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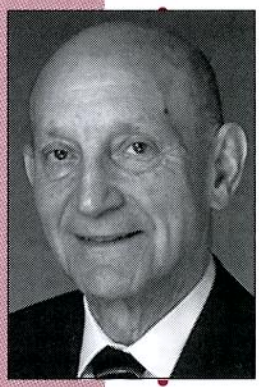
GUEST EDITORIAL

Making Fabless Strategies Work

By BERNIE VONDERSCHMITT ◆ President, Xilinx Inc.

Xilinx is just one of more than 100 semiconductor companies that do not own their own wafer fabrication facility, and use independent silicon "foundries" for fabrication services. "Fabless" companies are not a fad; their streamlined structure fits today's tumultuous, fast-moving marketplace. Being fabless allows Xilinx to concentrate on what we do best — the design and marketing of programmable logic devices.



Hewlett-Packard's announcement that it is quitting the foundry business and the recent troubles of a few fabless companies have led some industry pundits to once again question the viability of fabless semiconductor suppliers. (Hewlett-Packard Co. is *not* one of Xilinx's wafer sources.) We strongly believe that the oracles predicting the demise of the fabless semiconductor vendor are wrong. While ours is not the best business model for everyone, Xilinx and many other fabless companies will continue to succeed by establishing a win-win business relationship with our foundry partners.

The first key to a successful fabless strategy is to employ standard fabrication processes that are compatible with a variety of foundries. Xilinx FPGAs and EPLDs are based on "plain-vanilla" SRAM and EPROM technologies. This allows us to benefit automatically from the industry's latest process improvements and to establish multiple foundry sources for our products.

Multiple foundry sources ensure adequate and continuous product availability in case of disasters. Competition between foundries, as well as ongoing process and product improvements, ensure that price projections are met. In contrast, fabless companies with specialized processes have fewer potential suppliers and less leverage in the "foundry market." If a foundry agrees to a specialized process, prices inevitably will be higher due to the special attention needed to get and keep that process under control.

"The relationship between a fabless semiconductor company and its foundries must be long term, based on mutual trust, and of benefit to both parties."

The relationship between a fabless semiconductor company and its foundries must be long term, based on mutual trust, and of benefit to both parties. Xilinx benefits financially by gaining access to advanced fabrication processes without huge capital investments. We can focus on innovation, providing value through the development of better products.

Our foundry partners benefit by diversifying their manufacturing capacity over different equipment markets; through Xilinx, they have gained access to a significant new market segment without incurring the expense of product and market development. Foundries minimize demand volatility through this market diversification. Assuming a long-term relationship, the foundry can improve its competitiveness compared to other manufacturers.

Continued on page 4

XILINX®

THE FAWCETT

Continued from page 2

Xilinx Customer Service group will automatically send you a new maintenance contract (again, assuming that the information on your registration is current). Then you need to have your purchasing department send a copy of the contract back to us with a purchase order or check within 30 days to ensure uninterrupted support. No additional paperwork is required, and you will have the peace-of-mind of knowing that you'll always be up-to-date with the latest software.

Yes, software maintenance contracts do cost money. This revenue helps us to offset the cost of maintaining the registration list and the direct costs of the updates themselves (diskettes, tapes, documents, handling, shipping, etc.). No, software maintenance contracts are not a source of profit to Xilinx. In fact, our finance and accounting folks estimate that our direct costs for software updates are about twice as much as our revenue from maintenance contracts. We feel that the update service is well worth the cost to you and the cost to us.

A big update is about to occur. If you're not sure if we have all the correct information about the status of your system (development systems get transferred between departments, addresses change, engineers sometimes move from project to project and from company to company), you will want to change or verify your registration information or maintenance status by simply faxing or telephoning our Customer Service group. The FAX number is 408-559-0115. Customer Service personnel are assigned to particular geographic areas, and the telephone numbers are as follows:

- **United States and Canada:**
  - Southwest U.S. 408-879-4917
  - Northwest U.S. & British Columbia 408-879-5150
  - Northeast U.S., Mid-Atlantic U.S., & Canada (except B.C.) 408-879-4939
  - Central U.S. 408-879-5321
  - Southeast U.S. 408-879-5383
- **Europe** 408-879-5383
- **Japan** 408-879-5321
- **Southeast Asia & Rest of World** 408-879-4917

If you have PC-based software, it will help us if you have the serial number from your software protection key available when you call.

If you have let your software maintenance agreement lapse, and are interested in reinstating your support and getting the latest updates, special pricing is available. Just contact your local Xilinx sales representative or distributor.

Good luck with your designs, and have a wonderful holiday season! ♦

GUEST EDITORIAL

Continued from page 3

Xilinx's foundries have gained a significant additional benefit — the ability to use FPGAs as "process drivers" — the technology used to drive and verify process advancements. The regularity and 100% testability of our FPGAs facilitates defect analysis and fault testing.

Our foundries have learned that by applying 10% to 20% of their capacity to FPGAs, they gain excellent rewards from process control diagnostics. The resulting improvements to their processes can be applied to their other CMOS product lines. (It should also be noted that Xilinx employs its own process experts, who work closely with our foundry partners in the development and implementation of process technology improvements.)

Thus, Xilinx can effectively drive process improvements through our working relationships with our foundry partners. But these relationships must be based on mutual benefits. In the future, as in the past, this will be a necessary ingredient for success. ♦

NetStar's High Performance Networking System Benefits From Xilinx FPGAs

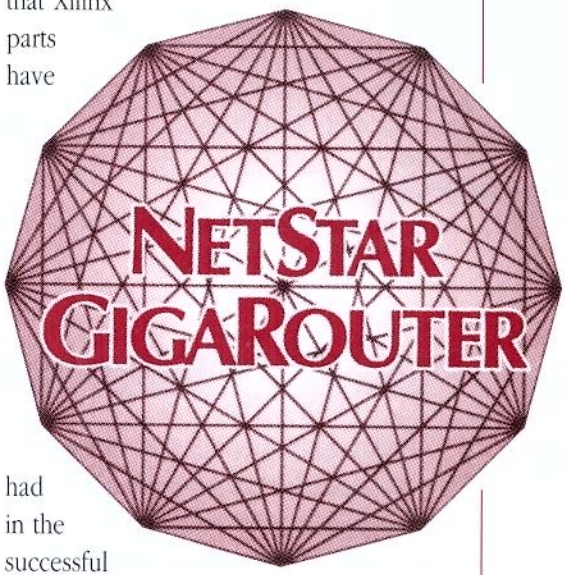
The use of programmable logic in systems design transcends most product and market boundaries. Xilinx FPGAs and EPLDs can be found in many of today's most innovative products, covering a broad range of market segments. Consider the GigaRouter™, a switched routing network system made by NetStar of Minneapolis, Minnesota.

NetStar developed the GigaRouter in response to market demands for a networking system that combines high performance with media flexibility. Xilinx FPGAs are used to implement a variety of functions, including data bus multiplexing and control, DMA and DRAM control, and switch core interfacing. Each network board uses 18 Xilinx devices ranging from the high-speed XC3100 family to the feature-rich XC4000 family. Also, NetStar uses Xilinx's latest TQFP packaging.

According to John Mullaney, NetStar's director of engineering, "Xilinx FPGAs were the only high-density programmable logic solultion which provided the high speed we required. In addition, we needed high I/O counts and lots of logic for pipelining. Design iterations on a high-density device make reprogrammability a necessity. Furthermore, the ability to migrate to HardWire™ gate arrays leaves open the possibility for future high-volume cost reduction."

"Design iterations on a high-density device make reprogrammability a necessity."

The GigaRouter allows networks to keep pace with the tremendous amount of computing power available today. NetStar's users benefit from more effective use of their computer resources and their own user's time. "With the integral role that Xilinx parts have had in the successful development of the GigaRouter, we have every reason to use Xilinx in future products," said Mullaney. ◆



Programmable Logic in the GigaRouter:

Xilinx part	Qty	Usage
XC3142-5	8	Data bus MUX
"	1	Switch core interface
XC3164-5	2	Shared memory and hardware control
XC3190-5	1	HIPPI destination chip
"	1	Communications bus control
XC3195-3	1	HIPPI source chip
XC3195-5	2	DMA and DRAM controller
XC4005A-5	2	Serialization/de-serialization control

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order please contact your local Xilinx sales representative. ♦

TITLE	DESCRIPTION	PART NUMBER
FPGAs		
ZERO+ Family Overview	Features/benefits	#0010179-01
ZERO+ Family Data Sheet	Technical data	#0010165-02
EPLDs		
PAL Conversion Guide & Datasheets	Technical data	#0401149-01
Logic Professor Demo Diskette	PC-based tutorial on replacing PALs with Xilinx EPLDs	#0010181-01
EPLD Mixed Volt Applications Note	Technical data	#0010180-01
Packaging		
Ball Grid Array Overview	Features/benefits	#0010184-01
Ball Grid Array White Paper	Technical Data	#0010186-01
Corporate		
Product Description & Selection Guide	Overview of entire Xilinx product line and services	#0010130-03

For a complete list, please contact your sales representative or see XCELL Issue #10.

Mark Your Calendars

COMING EVENTS

Xilinx applications engineers, consultants and customers will present educational papers at several upcoming industry conferences. These sessions provide an excellent opportunity to learn from those who have put Xilinx products to work in a variety of leading-edge applications.

ACM International Workshop on FPGAs

February 13-15

University of California, Berkeley

This workshop will examine several aspects of designing with FPGAs: CAD for FPGAs, fast-prototyping, applications, new architectures and field-programmable interconnect chips and analog arrays.

For specific information on Xilinx sessions, contact Jan Houts at (408) 879-5164.

European Design and Test Conference

February 28 - March 3

Paris, France

A joint promotion of EDAC, ETC and EuroASIC, this event will provide those involved in system or ASIC design with the latest information on state-of-the-art technologies and techniques.

PLD Conference

April 11-13

San Jose, California

The fourth annual PLD Design Conference and Exhibit promotes the practical use of all types of programmable logic devices. Paper session topics include design trends, advanced design techniques, applications, in-circuit reprogrammability, rapid prototyping and emulation and benchmarking. ♦

Advanced Training Opportunities Available For Current Xilinx Users

Since you receive *XCELL*, you are probably already using the Xilinx Development System, so you may be interested in some of the following advanced training opportunities:

Advanced Training

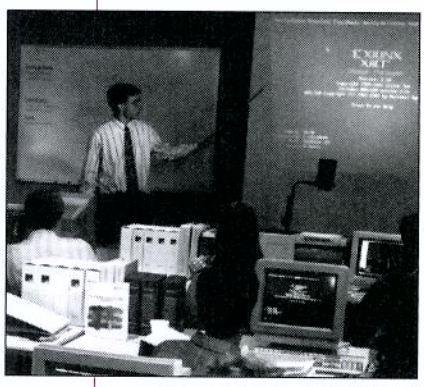
Free Advanced Training sessions are held regularly at Xilinx's San Jose facility. They can also be brought into your facility by your local Field Applications Engineer and even customized to cover the specific topics of interest to those in attendance. Popular topics include:

- Logic design for FPGA architectures
- Optimizing for speed or density
- Techniques to complete difficult designs
- Advanced capabilities of the development system

Advanced Training can last up to a full day, depending on your needs. The only prerequisite is that you should be familiar with the Xilinx software, and it is preferable that you have already started at least one design. If you don't have that familiarity, attend one of our standard training classes held regularly throughout the world.

On-Site Classes

Did you know that Xilinx can bring its training classes directly to your facility? At an on-site class, you have more control over the duration and content of the class. Most of these classes have a mixture of those just getting started with Xilinx and those who have used the products extensively. We arrange the class so that the new users are brought up to speed during the the first segment, while the experienced users join the class later -- a proven method to spread Xilinx knowledge around your company without your having to invest a great deal of time. If you don't have an appropriate classroom facility, Xilinx can arrange for one close by.



For the Latest Information

Xilinx's course offerings will change significantly with the XACT 5.0 software update. To find out the latest information on classes, call Candace Blackwell, the Xilinx Training Registrar, at (408) 879-5090, or call your local Xilinx sales representative. ◆

FINANCIAL REPORT

Record Second Quarter Revenues for Xilinx

Xilinx Inc. reported record revenues for the second fiscal quarter of 1994 (ending Oct. 2, 1993). Sales revenue for the quarter rose to $60.1 million, up 41% from the same quarter in fiscal 1993, and up 10.4% from the immediately preceding quarter. For the first six months of the 1994 fiscal year (April 1 - Oct. 2, 1993) revenues totaled $114.5 million, an increase of 40% from the comparable period in fiscal 1993. (Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX.)

Continued demand for programmable devices with higher speed and capacity is fueling this growth. Sales of the XC4000 family FPGAs increased by 22% and sales of the XC3100 family grew 68% over the previous quarter. The mask-programmed HardWire product also showed a strong sequential increase, growing 31% from last quarter; these customized products provide a low cost migration path for high volume applications. ◆

COMPONENT AVAILABILITY CHART - OCTOBER 1993

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3120	XC3130	XC3142	XC3164	XC3190	XC3195	XC4003	XC4005	XC4006	XC4008	XC4010	XC4013	XC4002A	XC4003A	XC4004A	XC4005A	XC4003H	XC4005H	XC7236	XC7272	XC7236A	XC7272A	XC7354	XC7372	XC73108
44	PLASTIC PLCC	PC44	◆	◆			◆				◆											◆												◆					◆		◆				
	CERAMIC CLCC	WC44																																					◆		◆		◆				
48	PLASTIC DIP	PD48	◆																																												
64	PLASTIC VQFP	VQ64		◆	◆	◆					◆					◆	◆																															
68	PLASTIC PLCC	PC68	◆	◆	◆		◆	◆			◆	◆										◆	◆																		◆		◆	◆	◆			
	CERAMIC CLCC	WC68																																					◆		◆	◆	◆			
	CERAMIC PGA	PG68	◆																																												
84	PLASTIC PLCC	PC84		◆		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆						◆	◆	◆	◆			◆		◆		◆	◆		
	CERAMIC CLCC	WC84																																					◆		◆		◆	◆		
	CERAMIC PGA	PG84		◆			◆	◆	◆		◆	◆	◆									◆	◆	◆				◆												◆		◆		◆			
100	PLASTIC PQFP	PQ100					◆	◆	◆			◆	◆	◆								◆	◆	◆				◆						◆	◆											
	PLASTIC TQFP	TQ100		◆				◆	◆														◆	◆																							
	PLASTIC VQFP	VQ100				◆						◆	◆				◆	◆																	◆	◆											
	TOP BRZ. CQFP	CB100					◆		◆																										◆											
120	CERAMIC PGA	PG120																										◆						◆	◆	◆										
132	PLASTIC PGA	PP132						◆	◆				◆	◆									◆	◆																							
	CERAMIC PGA	PG132						◆	◆				◆	◆									◆	◆																							
144	PLASTIC TQFP	TQ144											◆	◆				◆	◆				◆															◆	◆							
	CERAMIC PGA	PG144																																												◆	
156	CERAMIC PGA	PG156																											◆	◆							◆									
160	PLASTIC PQFP	PQ160								◆	◆				◆	◆									◆	◆	◆		◆	◆							◆	◆							◆
164	TOP BRZ. CQFP	CB164									◆																		◆																
175	PLASTIC PGA	PP175									◆					◆										◆	◆																			
	CERAMIC PGA	PG175									◆					◆										◆	◆																			
176	PLASTIC TQFP	TQ176														◆					◆																										
191	CERAMIC PGA	PG191																													◆	◆						◆								
196	TOP BRZ. CQFP	CB196																														◆														
208	PLASTIC PQFP	PQ208									◆					◆										◆	◆		◆	◆							◆	◆								
	METAL MQFP	MQ208																													◆	◆	◆												
223	CERAMIC PGA	PG223																									◆					◆							◆							
225	PLASTIC BGA	PB225																																												N
	CERAMIC BGA	WB225																																												N
240	PLASTIC PQFP	PQ240																																												
	METAL MQFP	MQ240																																◆						◆						

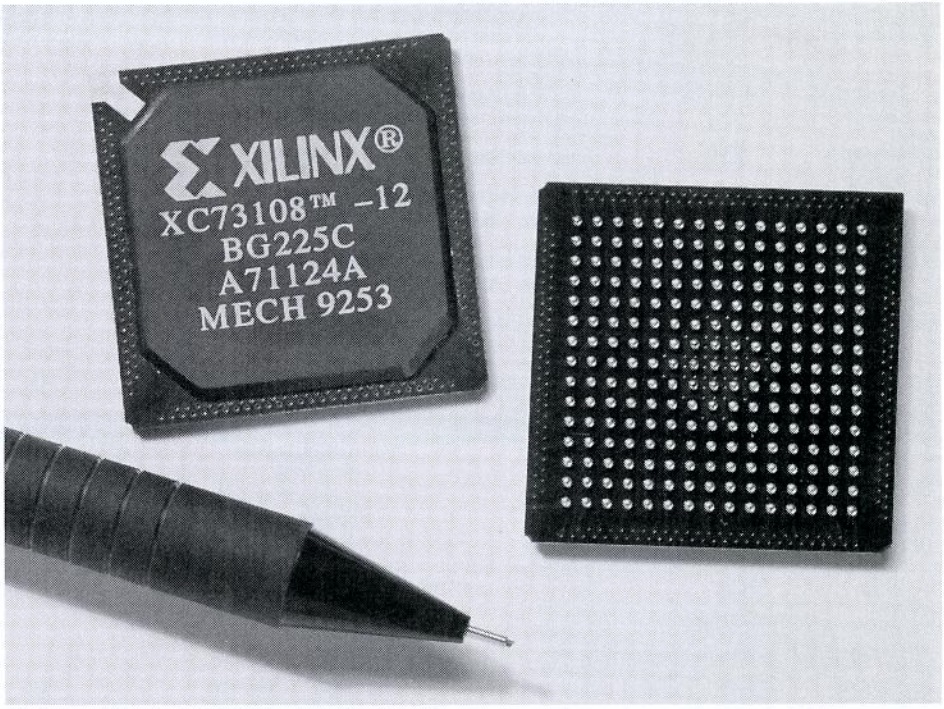
◆ = Product currently shipping or planned N = New since last XCELL

XILINX RELEASED SOFTWARE STATUS - NOVEMBER 1993

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform					Last Update
					PC1 *5.0*	NC2 *3.30*	SN2 *4.1.x*	AP1 *10.4*	HP7 *9.01*	
XILINX INDIVIDUAL PRODUCTS										
CORE FPGA	XC2,3,4K Support	Core Implementation	DS-502-xxx	1.41	1.42	1.42	1.42	1.42	1.42	07/93
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	4.00	4.10		4.10			08/93
Mentor[1]	V7.00	I/F and Libraries	DS-343-xxx	4.00				4.10		02/93
Mentor[1]	V8.20	I/F and Libraries	DS-344-xxx	1.00			1.10	1.10	1.10	07/93
OrCad[2]		I/F and Libraries	DS-35-xxx	4.22A	4.23	4.20				06/93
Synopsys[1]		I/F and Libraries	DS-401-xxx	2.00			3.01	3.01	3.01	09/93
Viewlogic[2]	ViewDraw	I/F and Libraries	DS-390-xxx	4.14	4.15					06/93
Viewlogic[2]	ViewSim	I/F and Libraries	DS-290-xxx	4.14	4.15					06/93
Viewlogic[2]		I/F and Libraries	DS-391-xxx	4.14	4.15		5.01			06/93
XABEL[2]		Entry, Sim, Lib, Opt.	DS-371-xxx	1.03	4.30		4.30			10/93
X-BLOX[1]		Architectural Synthesis	DS-380-xxx	1.03	1.04	1.04	1.04	1.04	1.04	10/92
XILINX PACKAGES										
Mentor 8	Standard		DS-MN8-STD-xxx	1.00			1.10	1.10	1.10	07/93
Mentor 8	Extended		DS-MN8-EXT-xxx	1.00			1.10	1.10	1.10	07/93
Mentor 7	Standard		DS-MN7-STD-xxx	1.00				1.10		07/93
Mentor 7	Extended		DS-MN7-EXT-xxx	1.00				1.10		07/93
OrCad	Base		DS-OR-BAS-xxx	1.10	1.20					07/93
OrCad	Standard		DS-OR-STD-xxx	1.10	1.20					07/93
Synopsys	Standard		DS-SY-STD-xxx	1.01			1.10	1.10	1.10	09/93
Viewlogic	Base		DS-VL-BAS-xxx	1.10	1.20		1.20			07/93
Viewlogic	Standard		DS-VL-STD-xxx	1.10	1.20		1.20			07/93
Viewlogic	Extended		DS-VL-EXT-xxx	1.10	1.20		1.20			07/93
Viewlogic/S	Base		DS-VLS-BAS-xxx	1.10	1.20					08/93
Viewlogic/S	Standard		DS-VLS-STD-xxx	1.10	1.20					08/93
Viewlogic/S	Extended		DS-VLS-EXT-xxx	1.10	1.20					08/93
XILINX HARDWARE										
Prom Pgmr.	Conf. Prom. Pgmr.	Software	HW-112	3.30	3.31					04/93
Programmer	Conf. Pgmr.		HW-120		3.14					
THIRD PARTY PRODUCTION SOFTWARE VERSIONS										
Cadence	Composer	Schematic Entry	N/A				4.2.2		4.2.2	N/A
Cadence	Verilog	Simulation	N/A				1.6.c.5		1.6.c.5	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A				1.3-P3		1.3-P3	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A				2.0-P11		2.0-P11	N/A
Mentor	NETED	Schematic Entry	N/A					7.XX		N/A
Mentor	QuickSim II	Simulation	N/A					7.XX		N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2			8.2-5	8.2-5	8.2-5	N/A
Mentor	QuickSim	Simulation	N/A	8.1			8.20	8.20	8.20	N/A
OrCad	SDT	Schematic Entry	N/A			4.00				N/A
OrCad	VST	Simulation	N/A			4.00				N/A
OrCad	SDT 386+	Schematic Entry	N/A		1.10					N/A
OrCad	VST 386+	Simulation	N/A		1.10					N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.0A			3.0b	3.0b	3.0b	N/A
Viewlogic	ViewDraw	Schematic Entry	N/A		4.1.3A		5.1			N/A
Viewlogic	ViewSim	Simulation	N/A		4.1.3A		5.1			N/A
XABEL	ABEL Compiler	Entry and Simulation	N/A		4.3		4.3			N/A

NOTE: [1]FPGA Only [2]FPGA and EPLD

Xilinx Offers PLDs in New Ball G



Ball Grid Array Package pictured with the tip of a pencil to demonstrate its size.

As the newest alternative for high-density surface-mount packaging, the ball grid array (BGA) offers higher density than the plastic quad flat package (PQFP). The BGA also eliminates handling and assembly issues commonly associated with PQFPs. The BGA will rapidly become the preferred package for applications that require more than 200 pins in a surface-mount configuration.

> *"As PLDs grow in functionality and complexity, packaging technology must adapt to meet both the high-pin-count requirements and surface mount assembly capabilities."*

The BGA uses solder balls on the underside of a small substrate instead of leads to connect to a PC board. The inherent mechanical ruggedness of the balls along with a wide pin-to-pin pitch of 1.5 mm results in improved manufacturing yields. PC board space is reduced and electrical and thermal performance is improved compared with the PQFP.

As PLDs grow in functionality and complexity, packaging technology must adapt to meet both the high-pin-count requirements and surface-mount assembly capabilities. The BGA accommodates both these needs nicely and, as a result, Xilinx will support this new technology by offering its industry-leading EPLDs and FPGAs in the BGA package.

EPLD Program Advantages in BGA

EPLDs are often used in applications requiring very fast pin-to-pin timing and predictable performance. Typically they

Array Package

"The BGA provides the best solution for high-pin-count programming by completely eliminating the problems associated with the handling and programming of PQFPs."

are programmed in a device programmer, and then inserted into the PC board for prototyping or production. Because each individual device requires handling prior to insertion, there is a risk of lead damage with fine-pitch packaging (QFPs). The BGA provides the best solution for high-pin-count programming by completely eliminating the problems associated with the handling and programming of PQFPs.

BGA Prototyping and Manufacturing

Because of its advantages when used with complex PLDs, the BGA will rapidly be accepted as a package technology. The BGA has been proposed for JEDEC registration. Supporting test hardware is available.

A BGA socket adapter for the standard Xilinx EPLD Programmer will be available Q4'93, while third-party programming support will follow in early 1994. BGA test socket availability continues to increase, with 3M/Textool offering a 225-pin socket (part # 2-0225-08172-000-019-002). Emulation Technology also offers both ZIF and production BGA socket support.

Xilinx EPLD/FPGA BGA Availability

The Xilinx XC73108™ is the first EPLD to be offered in the 225-pin BGA. Initial samples are available now. Production is planned for 1Q94. Xilinx will also offer its industry-leading FPGAs in BGAs. Both the XC4010 and XC4013 FPGAs are scheduled for sampling in 1Q94. ♦

BGA Package Advantages

The BGA package offers a host of advantages when compared to PQFPs.

Smaller Package Size	BGA	PQFP
Area	729 mm² (225 BGA)	952 mm² (208 PQFP)
Height	1.9 mm	3.7 mm
Improved Performance	**169 BGA**	**160 PQFP**
Lead Inductance	5.4 nH	10 nH
Capacitance	1.1 pF	1.6 pF
Theta J/A	23°C/W	35°C/W
Improved Manufacturing	**BGA**	**PQFP**
Lead pitch	1.5 mm	0.5 mm (208 PQFP)
Programmer Insertion	easy	potential lead damage
Lead coplanarity	no issue	difficult to maintain
Pick and Place	Trays or Tape & Reel	Trays only
Placement tolerance	0.3 mm	0.075 mm
Solder defects	<20 ppm	>500 ppm

EPLDs Offer 100% Populated Interconne

EPLDs (also called Complex PLDs) are typically multiple PAL® blocks whose inputs and outputs may be programmed to connect through an interconnect matrix. It is easy to assume that all EPLDs provide the same degree of routability, capability, and ease-of-use. However, that is not the case.

The structure of the interconnect matrix determines the extent to which routability is dependent on the specifics of the user application. For example, many EPLD architectures specify constraints on the user application, such as limiting the percent utilization of macrocells, in order to ensure a reasonable probability of successful routing. For designs that try to use all the available macrocell and pin resources, this often leads to frustration and unexpected results.

"By allowing logic capability in the interconnect matrix, more logic may be performed within a single PAL block."

Many common EPLDs have an interconnect matrix that is sparsely populated. In order to route a particular design, the architecture relies on the ability to swap all resources (including macrocells, input pads, and output pads) as needed in order to fit the sparse matrix pattern. Design iterations may lead to unexpected pinout changes or failure to route.

UIM: 100% Populated Matrix

The Xilinx XC7000 EPLD family offers a unique, patented Universal Interconnect Matrix (UIM™) that provides 100%

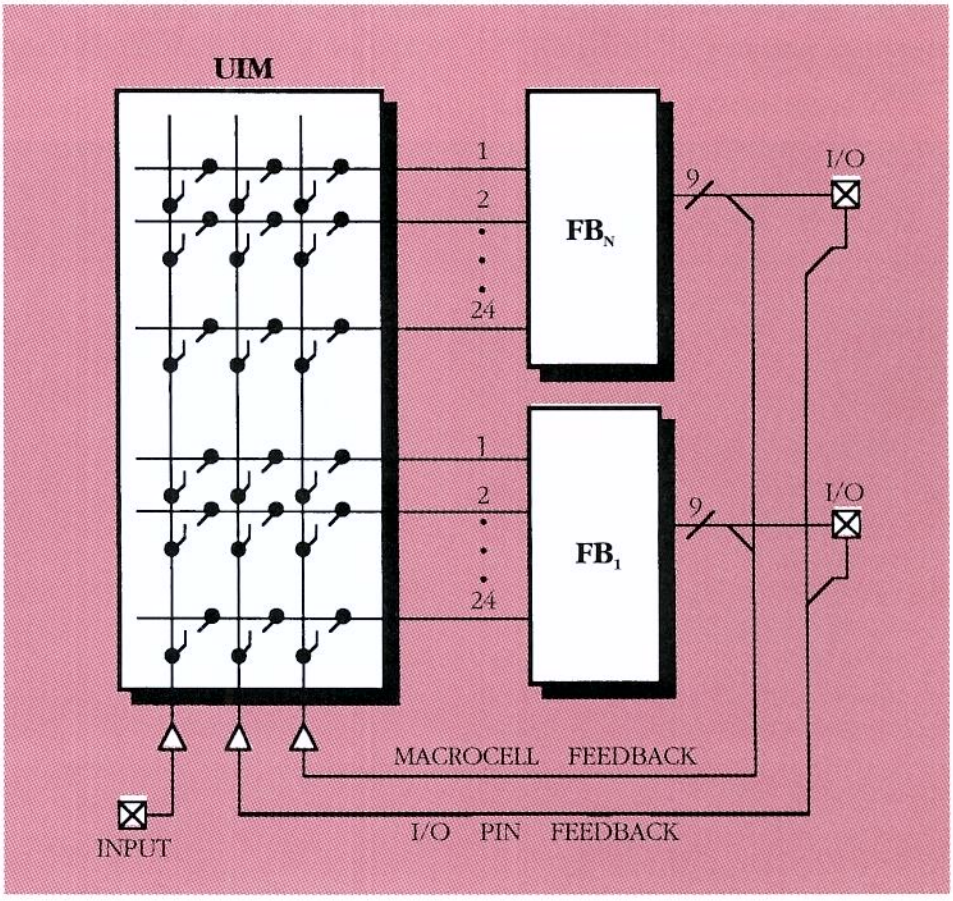


Figure1: Fully populated UIM with 100% routability

Matrix with Logic Capability

routability in a fully-populated interconnect matrix. In the UIM, every macrocell output and every input pad is represented as a vertical line, every block input is represented by a horizontal line and every intersection of these lines is a possible connection. In this way, any key signal may be fed to any block, without affecting the routability of any other signal. With the UIM, 100% routability is guaranteed!

UIM Has Logic Capability

Physically, the UIM is an array of programmable EPROM switches much like the AND Array used for product term logic. In particular, the UIM can perform *wide AND functions* in the same way the AND Array does, hence offering an additional level of logic. In other words, the interconnect matrix that links all the PAL blocks on the device can also act as an AND plane, all without any speed penalty! This capability is unique among all EPLDs currently on the market today.

By allowing logic capability in the interconnect matrix, more logic may be performed within a single PAL block. In applications such as binary counters that stretch across multiple blocks, the UIM can be used effectively to perform the carry function across block boundaries with no speed penalty. Applications such as complex-state machines can use the UIM as a partial condition decode as well. In many cases, this capability provides higher performance than competing products for applications that may otherwise require multiple passes through the device.

The UIM offers a fully populated interconnect matrix *and* logic capability. This feature can only be found on Xilinx EPLDs! ♦

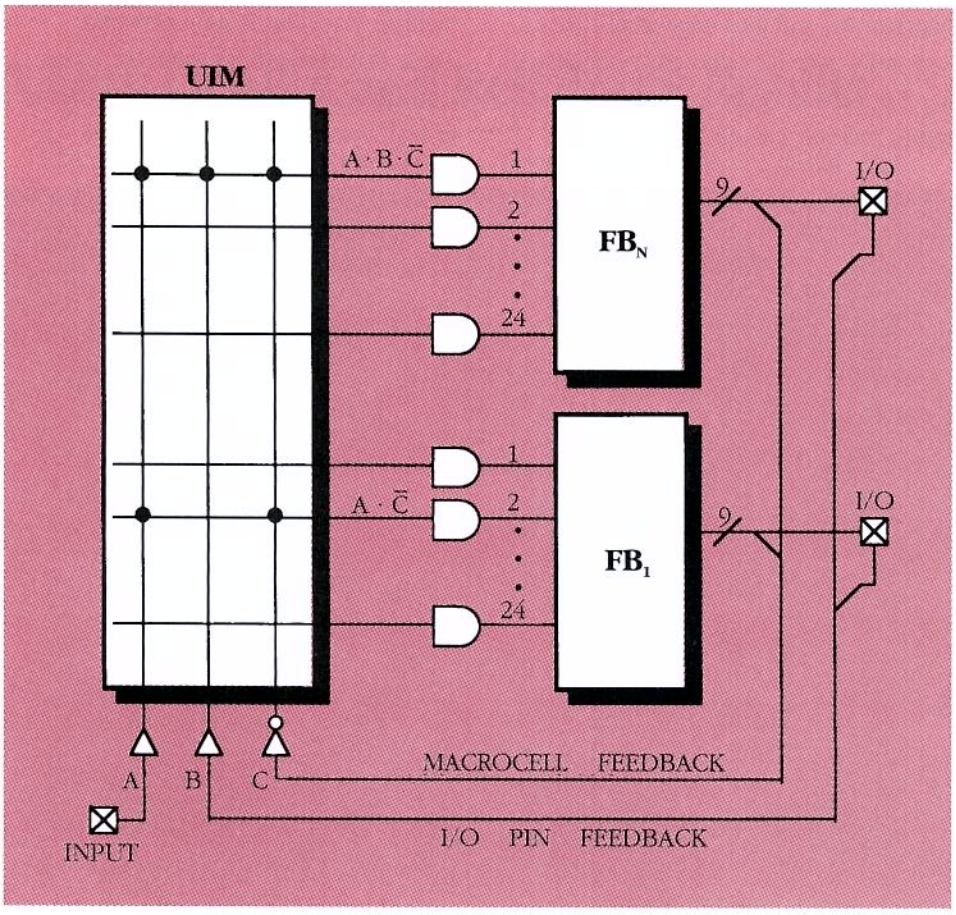


Figure 2: UIM has logic capability

PREP Results

Benchmarks Confirm XC4013 as Highest-Density FPGA

Complete PREP™ benchmark results for the XC4013 FPGA were submitted to the PREP committee for verification in October. The submitted results are shown in the accompanying table. These benchmark results firmly establish the XC4013 as the highest-density FPGA available today.

For some benchmarks, both "automatic" and "manual" results are shown. In most cases, the "manual intervention" that produced the "manual results" only involved floor planning of the basic layout.

Benchmarks one and nine were implemented both with and without logic synthesis. The synthesis results were generated by entering the benchmark circuits using the VHDL language and compiling them with the Synopsys FPGA-Compiler. The synthesis tools recognize that some logic is common to each instance of these benchmarks, and thus implements that logic only once (as opposed to implementing it in each instance). The synthesized results indicate a much higher capacity level than the non-synthesized results. Both are shown in the table.

We believe that removing logic from each instance in this manner exploits the artificial nature of "step-and-repeat" benchmarks, violating the spirit of the PREP benchmark specifications. However, one of our competitors did so in the March, 1993, PREP results in order to "prove" that they had the largest device. We have included both synthesized and non-synthesized results for these benchmarks so that more equitable comparisons to other devices can be made.

It should be noted that the logic content and "step-and-repeat" methodology of the PREP benchmarks precludes the use of some significant features of the XC4000 architecture, such as on-chip memory capability, edge decoders, internal three-state buffers, boundary scan support and multiple clock distribution networks. These features further extend the actual capacity and efficiency of XC4000 devices in real, system-level applications. ◆

PRELIMINARY, UNCERTIFIED. XC4013 data is not certified by PREP, but is derived according to PREP PLD Benchmark Suite #1, Version 1.2, dated 3/28/93.

		Instances	% Use	Speed (MHz) Best	Average	Worst	External
#1 - Data Path	Auto (Syn)	70	100	106	87	54	27
	Man (Syn)	70	100	112	109	84	21
#2 - Timer/Counter	Auto	46	100	35	28	23	26
	Man	48	100	40	39	38	32
#3 - Small State Machine	Auto	52	99	46	37	29	26
#4 - Large State Machine	Auto	22	99	29	24	21	21
#5 - 4-Bit Multiplier/Accumulator	Auto	27	99	20	18	16	14
	Man	36	100	19	19	19	16
#6 - 16-Bit Accumulator	Auto	72	100	31	30	23	18
	Man	60	94	39	39	32	26
	Man	72	100	31	31	28	23
#7 - 16-Bit Counter	Auto	72	100	40	40	36	23
	Man	60	94	43	42	40	41
	Man	72	100	40	40	40	40
#8 - Pre-Scaled 16-Bit Counter	Auto	72	100	40	40	36	23
	Man	60	94	62	54	49	41
#9 - Memory Mapper	Auto (Syn)	92	99	37	31	20	14
Average	Man (Syn)	59	--	47	44	37	26
	Auto (Syn)	58	--	43	37	29	21

New Speed Grade for the XC2000 Family

The XC2000 FPGA family is being extended with the addition of a -130 speed grade. The part is significantly faster than the -100 speed grade; combinatorial delays are 31% faster and clock to output is 21% faster.

The new speed grade is available for the following device-packages:

- XC2018-PC68
- XC2018-PC84
- XC2018-VQ64
- XC2018-TQ100
- XC2018-PG84

For the XC2064, the new speed grade will be available in 1Q94.

Along with providing a high speed migration path within the XC2000 family, the new speed grade enhances and further develops the cost-effective XC2000 product line.

Please contact your local Xilinx sales representative for samples and datasheets. ◆

Timing Parameter	Symbol	XC2000-100	XC2000-130
Combinatorial Delay	T_{ilo}	8	5.5 ns
Setup time	T_{ICK}	6	2.5 ns
Clock to pad	T_{OPS}	7	5.5 ns
Pad to input	T_{PID}	4	3.5 ns
Max toggle rate	F_{CLK}	100	130 MHz

Xilinx Quality and Reliability Results

Because Xilinx FPGAs are built using a standard, highly-reliable CMOS SRAM process, Xilinx has outstanding quality results. The following data is from the Xilinx internal reliability monitor. A FIT is a Failure In Time measured as failures that occur in one billion (10^9) hours of operation. If you are more familiar with Mean Time to Failure (MTTF) as a measure of reliability, then just take the inverse of the FIT measurement:

MTTF = 1/FIT = 10^9 hours/failures

For example, equipment that contains 1000 devices, each with a 4 FITs reliability level, has a 50% probability of having one device failure in $10^9/(4 \times 1000)$ = 250,000 hours (about 30 years) of uninterrupted operation (24 hours/day).

As is clear from the chart, the XC3000 family reliability reflects a mature, high-volume product. Both the XC3000 and XC4000 family have significantly better reliability than many other forms of logic.

The Xilinx quality and reliability guide, available from your local sales representative, is updated on a quarterly basis. ◆

Static and Dynamic High Temperature Operating Life (HTOL) Test FIT Rate at 70°C

Quarter	XC3000 Static	XC3000 Dynamic	XC4000 Static	XC4000 Dynamic
Mar. 1992	20 FIT	9 FIT	45 FIT	N/A
June 1992	20 FIT	9 FIT	45 FIT	N/A
Sept. 1992	16 FIT	4 FIT	43 FIT	0 FIT
Dec. 1992	15 FIT	2 FIT	32 FIT	5 FIT
Mar. 1993	13 FIT	2 FIT	30 FIT	5 FIT
June 1993	13 FIT	1 FIT	35 FIT	2 FIT

HardWire™ Gate Arrays:
A Mask-Programmed Migration Path

Xilinx FPGAs offer you the speed and flexibility necessary to get your products to market quickly. The Xilinx HardWire Gate Array combines these features with an easy, transparent migration path to a lower-cost, mask-programmed device, providing a low-cost, no-risk solution for high-volume production applications.

HardWire Gate Arrays are mask-programmed versions of Xilinx FPGAs. In high-volume applications where the design is stable, the programmable devices used for development and initial production can be replaced by their HardWire equivalents. The HardWire family offers a significant cost reduction from the programmable device with virtually no risk or engineering resources required.

The HardWire family addresses the three primary issues the designer must resolve when making any change to the design: (1) functional compatibility, (2) timing compatibility, and (3) testability. First, unlike ordinary, general-purpose gate arrays, the HardWire gate array is architecturally identical to its FPGA counterpart. No logic is changed or lost and functional compatibility is guaranteed. Second, timing compatibility is exhaustively verified by Xilinx without the requirement of customer-supplied simulation vectors. Third, patented built-in test logic, along with Xilinx's Automatic Test Generation (ATG) software, provide 100% fault coverage with no need for customer supplied test vectors. Migration is simple, so you spend less time on rework and more time on new projects.

HardWire gate arrays offer pin-compatible replacements for Xilinx FPGAs, and, since they match FPGAs architecturally and support FPGA configuration, they can be used in conjunction with FPGAs, giving you the benefits of both cost reduction and in-system reprogrammability. The combination of Xilinx FPGAs and HardWire gate arrays provide the total solution for the complete life cycle of your product.

Xilinx offers HardWire gate arrays as migration paths for all Xilinx FPGA families, providing 50% to 85% cost reductions from the equivalent FPGAs. Minimum quantitiies and a small NRE are required. Contact your Xilinx sales representative for more information. ♦

"The HardWire family offers a significant cost reduction from the programmable device with virtually no risk or engineering resources required."

XACT 5.0:
Accelerating Your Productivity

The newest version of the XACT Development System, XACT 5.0, will begin shipping in the first quarter of 1994. Registered Xilinx development system owners with active software maintenance agreements will automatically receive this update.

XACT 5.0 contains several enhancements and features designed to increase the productivity of Xilinx users. (Several of these are expanded upon in subsequent articles in this issue.) New features include the following:

Enhancements Common to All Devices

- **Windows Compatibility**
  For PC users, XACT 5.0 will offer compatiblity with Windows v3.1. A new DOS extender allows designers to run the Xilinx XACT software without exiting Windows. This enables PPR/APR to be run in the background/multitasking mode while the computer is used for other applications.
- **Common Flows for All Xilinx Architectures**
  XACT 5.0 takes a major leap towards the standardization of the Xilinx design environment. Both schematic and behavioral entry is available for both FPGAs and EPLDs, along with support of all Xilinx families from popular third-party tools (including schematic editors, logic compilers, fitters, and simulators). FPGA and EPLD development uses the same basic design flow, with XNF interfaces, utilities such as XNFMerge, XMAKE, and XSimMake, and support for the Unified Library.
- **Unified Libraries**
  The Xilinx libraries have been re-engineered to allow easy migration between Xilinx programmable logic families. With the exception of a few architecture-dependent symbols, designs using the Unified Library can easily be retargeted to any Xilinx FPGA or EPLD device. (See related article on page 21.)
- **CD ROM Software Distribution and Programmable Key**
  For the first time, Xilinx will offer most software on CD-ROM media. CD-ROM distribution of software, combined with a programmable key (for PCs only), offers the following exciting capabilities:

Continued on next page

XACT 5.0 contains several enhancements designed to increase user productivity.

XILINX®

XACT 5.0 PREVIEW (Continued)

- The Programmable Key will allow multiple executions of any Xilinx program, allowing you to "test drive" the software before you decide to buy it.
- Significantly easier installation. All software is on a single CD-ROM instead of multiple floppy disks.
- Easier to archive software
- No issues with version incompatibility

(See related article on page 20.)

- **Design Rule Checker**
  XACT 5.0 contains a new design rule checker to help pinpoint problem areas before the design gets to the place and route phase. The output of the design rule checker contains detailed descriptions of problems, including specific signal and symbol names.
- **Xilinx-ABEL improvements**
  Xilinx-ABEL 5.0 includes several enhancements that make it easier to design sections of an FPGA or EPLD, or to design an entire EPLD. (See related article on page 24).
- **Simulation "Make" Command**
  Just as XMAKE automatically performs all the steps necessary to implement a design, a new utility called XSimMake will automatically perform all the steps needed to prepare a completed LCA or EPLD design for full timing simulation, including the back-annotation of signal names.

XC4000 Software Enhancements

- **Incremental Design**
  The XACT 5.0 release will add incremental design capability for XC4000 series designs. The incremental design methodology uses a previous design as a "guide" for the new design. For small changes, incremental design can significantly shorten the overall design cycle. *(See related article on page 22.)*
- **PPR Improvements**
  XACT 5.0 will continue to improve PPR routability and resulting device performance. The improvements to the "place and route" algorithms will be particularly noticeable in the implementation of highly-structured designs.
- **Enhanced XACT-Performance Control**
  This release will continue to build on the features of XACT-Performance™ including management of clock skew, support of the RPM library elements, RAM support, and improved carry-logic support.
- **Improved Back-Annotation for Functional and Timing Simulation**
  Users who have experienced difficulty in simulating XC4000 designs will find the XACT 5.0 release significantly easier. *(See related article on page 22.)*

XC3000 Software Enhancements

- **PPR for the XC3000A**
  Design implementation of XC3000A family FPGAs is now supported by the same PPR (Partition, Place, and Route) program used for the XC4000 family. This will bring the features of PPR, including XACT-Performance and X-BLOX support, to the XC3000A architecture. (The XC3000 and XC3100 family will continue to be supported by the APR implementation program.)
- **XACT-Performance for XC3000A**
  XACT-Performance allows designers to enter their exact performance requirements, up-front, at the schematic level. Previously available for the XC4000 family, XACT 5.0 will extend this capability to the XC3000A family. *(See related article on page 21.)*
- **X-BLOX for XC3000A**
  X-BLOX will support the XC3000A family in the XACT 5.0 release. *(See related article on page 23.)* ◆

XACT 5.0
ACCELERATING YOUR PRODUCTIVITY

XEPLD 5.0 Release Offers Significant Enhancements

The upcoming release of XEPLD 5.0, the portion of the XACT Development System supporting EPLD design, has many new features that significantly enhance the user's capability to create high-performance, high-density designs:

Increased Support for Conventional ASIC Design Approaches

With XEPLD 5.0, a user does not require in-depth knowledge of the EPLD architecture to implement efficient EPLD designs easily. Designs are created using schematic entry with the Unified Library's macros and primitives, and/or using behavioral entry, as with Xilinx-ABEL. Pin and resource assignments can be entered as parameters on the schematic. Functional and timing simulation are fully supported.

Ease of PAL Conversion

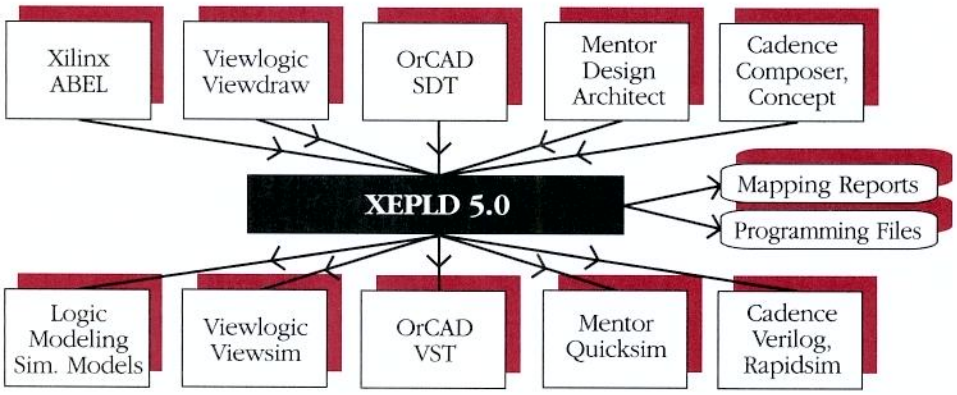
Existing PAL designs can be converted to the Xilinx EPLD architecture automatically, allowing users to replace multiple PAL devices with a single EPLD easily. Any changes to the integrated design can be implemented using familiar PAL development tools or PLUSASM, the Xilinx native EPLD development language.

Full Support of X-ABEL Compiler

The Xilinx-ABEL compiler is fully supported. Users can create complete designs with behavioral entry, or include Xilinx-ABEL files as submodules within a schematic. Major enhancements in the compiler itself have improved resource utilization.

Logic Resource Assignment

Enhancements have been made to PLUSASM that enable users to place logic into specific device resources. For example, the user can control the mapping of logic into specific function blocks or macrocells. Similarly, device pins, global clocks, and global three-state output controls can be automatically assigned by the software or manually assigned by the user.



Extensive Third-Party CAE Support

XEPLD 5.0 supports Viewlogic, OrCAD, and Xilinx-ABEL on PC and Sun workstation platforms. Mentor Graphics tools are supported on both Sun and HP7000 series platforms. Cadence Design Systems tools are supported on the Sun workstation. Board-level device simulation models are available from Logic Modeling Corp. for many simulators and platforms (See related article on page 25). ♦

XACT 5.0 ACCELERATING YOUR PRODUCTIVITY

The Xilinx Programmable Key for PC Users: *Questions & Answers*

Q: What is the Programmable Key?

A: The programmable key is a protection lock that attaches to the parallel port of a PC, just like the current Xilinx keys do. It will be required to run the XACT 5.0 PC versions of APR, XDE, PPR, X-BLOX and Xilinx-ABEL.

Q: How do I get this new key?

A: You will receive keys as part of the XACT 5.0 update for PC products. Base Packages will not require a key. Keys will be included with FPGA Core Implementation and Standard and Extended System packages.

Q: Does the new key look different from the old one?

A: Yes. The old keys are black and have a serial number beginning with 'A'. The new keys will be beige, have a Xilinx logo embedded in the plastic, and have serial numbers beginning with 'C'.

Q: Do I still need the old key(s) I currently have?

A: Yes. Keep these keys to be able to run pre-XACT 5.0 software. Also, Viewlogic's DOS versions of Viewdraw-LCA (DS-390-PC1) and Viewsim-LCA (DS-290-PC1) will still use the old key. These customers will chain both the old and new keys on the parallel port. Users of the DS-VLS-BAS-PC1, which includes Viewdraw-LCA and Viewsim-LCA, will use just the old key.

Q: So what are the basic steps I take to use the XACT 5.0 release with the new key?

A: It depends on the products you own:

Case 1: If you use a Base Package (DS-OR-BAS-STD-PC1 or DS-VL-BAS-PC1), you do not need a key at all with XACT 5.0 and may remove your old black key from your parallel port.

Case 2: If you have a DS-290-PC1 (Viewsim-LCA), DS-390-PC1 (Viewdraw-LCA), DS-VLS-STD-PC1 (Viewlogic Stand-alone Standard System), or DS-VLS-EXT-PC1 (Viewlogic Stand-alone Extended System with ViewSynthesis), add the new key onto the back of your current Xilinx key so that both keys are attached.

Case 3: If you have the DS-VLS-BAS-PC1, continue to use just the old key.

Case 4: If you own products other than those listed above, remove the old Xilinx key from your parallel port and attach the new one instead.

Q: Why aren't the Viewlogic DS-290-PC1 and DS-390-PC1 products using the new key?

A: Viewlogic does not plan to modify their existing DOS product. However, the new Viewlogic PRO Series Windows products will use the new key.

Q: What benefits does the new key offer over the old one?

A: The new key offers two new features. The first is the ability to evaluate any Xilinx software product you wish. With XACT 5.0, all of our PC software will be available on one CD-ROM disk. If you opt for CD-ROM, you will be able to install any product and execute it a limited number of times. A utility called XKEY will allow you to observe your key's remaining number of evaluation runs. The second benefit of the new key allows you to instantly authorize new products. Xilinx customer service can give you a password that, when supplied to the XKEY utility, will reprogram your key to be authorized for additional software products. ♦

XACT 5.0
ACCELERATING YOUR PRODUCTIVITY

Unified Libraries and RPMs

Have you ever wanted to move a design from an XC4000 to an XC3000 device? Have you ever wondered if a design is better suited for an EPLD or an FPGA? With XACT 5.0, Xilinx is making it easier to migrate designs between device families. XACT 5.0 includes the Unified Library, a totally revamped set of library elements for schematic entry that provides for design migration and reuse of proven designs in new applications.

Consistency and uniformity are the key attributes of the Unified Library. All primitives and macros common to two or more Xilinx device families are consistent in name and appearance. For example, the symbol for a 2-input AND has the same label, size, and pin locations whether you target the XC2000, XC3000 or XC4000 FPGA family or the XC7000 EPLD family. Thus, migration of a design from one family to another requires only a change in the compilation target and, if needed, the editing of any family-specific symbols used in the design.

As your own libraries grow, the Unified Library makes it simple to insert portions of proven designs into new designs. Again, consistent symbology makes your design easy to move and reuse, regardless of the target device. The libraries for future Xilinx architectures will use the Unified Library conventions, ensuring easy design migration and reuse for future product generations.

Relationally Placed Macros

Concurrent with the release of the Unified Library is support for Relationally Placed Macros (RPMs). Relationally Placed Macros are schematic-based macros with relative location constraints to guide the placement of the logic within an FPGA. RPMs replace hard macros, providing several key advantages. Because RPMs are designed on the schematic level, they are fully supported by both functional and timing simulation. Unlike hard macros, which are treated as a "black box" by the partition, place and route tool (PPR), RPMs allow PPR to utilize unused logic within the "boundary" of the RPM on the device, as well as apply XACT-Performance constraints to the logic within the RPM. Providing PPR with relative rather than fixed placement information means that routing resources can be used more intelligently, resulting in higher speed and more complete utilization. In short, RPMs offer all the advantages of Hard Macros, while also providing full simulation support and better performance.

The Unified Libraries also include 1200 pages of new, comprehensive documentation on all symbols — including detailed functional descriptions, symbol references, truth tables and schematic diagrams. ♦

XACT 5.0 ACCELERATING YOUR PRODUCTIVITY

XACT-Performance™ Provides Help for XC3000A Designs

A key feature of XACT 5.0 is XACT-Performance for the XC3000A family. As in the XC4000, XACT-Performance allows designers to enter their exact performance requirements, up-front, at the schematic level using the TimeSpec symbol and TS Flags.

After accepting this information, XACT 5.0 partitions, places and routes the design to achieve the specified performance goals. XACT-Performance makes FPGA designs much more predictable by allowing the software to focus on the overall problem of achieving the required performance for the entire design.

If a timing requirement is unachievable, the XACT software will alert the user early in the design process. XACT-Performance has been a very effective tool for designers using the XC4000 FPGAs, and should yield similar performance and ease-of-use advantages for XC3000A designs. ♦

Improved Back-Annotation Supports XC4000 Simulation

Three areas in previous releases of the XACT software caused signal back-annotation problems when simulating XC4000 designs:

- Usage of Hard Macros,
- Usage of X-BLOX symbols, and
- Correlation between original signal names and back-annotated signal names.

All areas have been addressed in the XACT 5.0 release.

The Hard Macro library has been converted to a new Relationally Placed Macro library (RPM library) in which partitioning and relative placement are controlled from the schematic level. This includes usage of schematic based carry-logic. Since the RPM library contains schematics for each library element, back-annotation to the schematic is no longer an issue. Designers can even drop down into RPM symbols and view the current state of the logic within the macro itself.

X-BLOX fully supports back-annotation, including back-annotation to X-BLOX buses. This capability exists for both functional and timing simulation.

XACT 5.0 also includes a new back-annotation program that provides virtually 100% signal matching between the designers original netlist and the back-annotated netlist. ◆

XACT 5.0 Features Incremental Design Support for the XC4000

The XACT 5.0 release will add incremental design capability for XC4000 series designs. This powerful feature (already available for the XC3000, XC3000A and XC3100 families) allows a previous design iteration to be used as a "guide" for a new pass on the same design.

Where the two designs match, the exact placement and routing is preserved, thereby preserving timing characteristics as well. Since only logic new to the design is subjected to the place and route algorithms, large designs that initially required a few hours to implement can be modified in only a few minutes.

The implementation and timing characterisitics of the unchanged portions of the design are preserved, easing the timing analysis and debugging process.

One note of caution: Existing LCA files do not include enough information to serve as a guide file for XC4000 designs. To take advantage of incremental design in PPR, users will have to reprocess their designs with PPR v5.0. ◆

This powerful feature allows a previous design iteration to be used as a "guide."

XACT 5.0 ACCELERATING YOUR PRODUCTIVITY

X-BLOX™ Adds XC3000A/L Family Support

The power of X-BLOX module generators is now available to users of the XC3000A and XC3000L device families. X-BLOX makes your designs smaller and faster by automatically using the special architectural features of Xilinx FPGAs. For example, X-BLOX will automatically use I/O block flip-flops, Global Clock Buffers, and Global Reset lines to yield a faster and more area-efficient design.

To use X-BLOX, use the X-BLOX schematic capture library of symbols along with your usual Xilinx primitives and macros. These symbols consist of generic modules customized to a particular width and style by hooking up specific pins and optionally adding attributes *(see Figure 1)*. XMAKE will automatically run the X-BLOX program to synthesize and optimize your design.

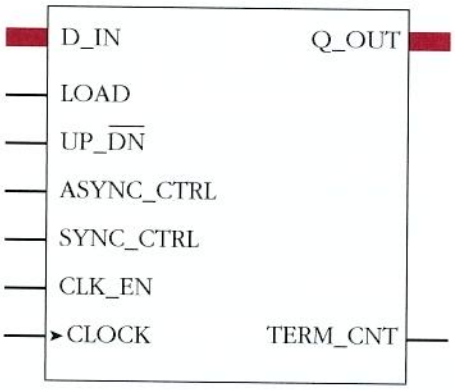


Figure 1: An X-BLOX Counter symbol, one of over 30 parameterized X-BLOX symbols.

Special features were added to X-BLOX to support the XC3000A/L families:

- Up until now, custom logic was required to implement asynchronously-loaded, non-zero values for accumulators, shifters, counters, registers and clock dividers. X-BLOX will automatically do this by using resettable flip-flops with inverters to implement asynchronous sets.
- Unlike the XC4000 architecture, the XC3000A/L does not have dedicated fast-carry logic. X-BLOX accumulators, adders, counters, and comparators are implemented with a limited look-ahead carry method.
- Adders and accumulators offer a STYLE option that provides a speed/area tradeoff control. For example, when implementing an 8-bit counter, the "slow style" mode generates one CLB per bit with a delay of 8 * T_{ILO}. Alternatively, if the default "fast style" is selected, carry-look-ahead logic is implemented, resulting in 1.5 CLBs per bit and a delay of 5 * T_{ILO}.
- X-BLOX PROM modules are synthesized into CLB lookup tables, resulting in a fast, small implementation.
- X-BLOX SRAM modules are synthesized into the edge-triggered flip-flops of the XC3000A/L families..

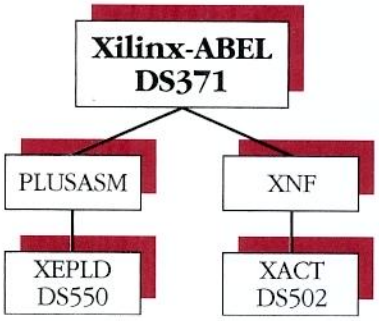
The XACT 5.0 release supports both unit-delay and full-timing simulation of X-BLOX modules in OrCAD, Viewlogic, or Mentor designs, complete with schematic back-annotation of simulation values for Mentor and Viewlogic. X-BLOX will automatically generate gate-level models to permit unit-delay simulation. Just as XMAKE generates LCA and BIT files, a new utility, XSimMake (fncsim8 and timsim8 for Mentor users) will automatically generate the necessary files for simulation. ♦

XACT 5.0
ACCELERATING YOUR PRODUCTIVITY

Xilinx-ABEL Provides Technology-Independent Design Environment

Xilinx-ABEL now supports both Xilinx EPLD and FPGA devices. Xilinx users can design with ABEL-HDL, an industry-standard design language, and implement the designs in either a Xilinx FPGA or EPLD device.

Xilinx-ABEL provides all the standard features of Data I/O's ABEL, including a friendly user-interface, comprehensive state machine, Boolean, and truth-table design language capabilities, extensive PAL device support and accurate functional simulation. Xilinx-ABEL can be used as a stand-alone design compiler to generate complete EPLD design files. It can also be used to create modules within a hierarchical EPLD or FPGA design. In other words, Xilinx-ABEL can be used along with schematic capture systems for mixed-mode design entry.



Xilinx-ABEL and EPLD Design

Xilinx-ABEL allows the user to develop an EPLD design in a technology-independent manner through its high-level Hardware Design Language. Users can pass device-specific control parameters to the EPLD fitter through "property" statements. The current version (V4.3) fully supports the Xilinx XC7000 EPLD family on the PC platform.

Xilinx-ABEL supports a large and comprehensive set of simple PAL devices. Existing ABEL or JEDEC files for these PALs can be directly compiled and used to create Xilinx EPLD design files. Stand-alone equation files can also be created for use as PLUSASM "Include" files.

New Features in Xilinx-ABEL with XACT 5.0

With the release of XACT 5.0, Xilinx-ABEL will be enhanced with more features, making it even easier to design sections of an FPGA or to design an entire EPLD:

- **ABEL 5 Support**
  ABEL 5 support comes with XACT 5.0. Users of Xilinx-ABEL will be on par with those using the version of ABEL offered by Data I/O.
- **Area - Speed Optimizations**
  Users can specify speed requirements with greater precision, setting them closer to actual specifications. Xilinx-ABEL will include a LEVEL optimizer with a 'timespec'-like syntax. Users can constrain timing for types of paths (e.g., pad-to-pad) using the Xilinx PROPERTY statement. Xilinx-ABEL then optimizes these paths to meet the specified timing constraints. The rest of the design is optimized for area.
- **New Options for Symbolic State Machine Compilation**
  Users can specify whether they want one-hot, binary, or clustered (combination of one-hot and binary) encoding for their symbolic state machines, allowing them to pinpoint the implementation and use of area required.
- **Optimization Enhancements**
  As always, improvements are constantly being made in optimization routines. Users will notice faster compilations and improved use of resources.
- **Sun Workstation Support**
  Xilinx-ABEL 5.0 will be available on both the PC and Sun platforms as part number DS371. Of course, current in-warranty customers will be sent an update. ◆

EDA Vendors Show Support for Xilinx at Alliance and Syndicate Meetings

Xilinx has two major programs to encourage and assist third-party EDA vendors in tailoring their products to support the design of Xilinx FPGAs and EPLDs. The **Alliance Program**, founded in 1990, concentrates on third-party design entry and verification tools such as schematic editors, timing analyzers, and simulators. The recently-established **Syndicate Program** is focused on logic synthesis tools.

Xilinx held a very successful inaugural Syndicate Program Seminar in September, with every major synthesis vendor learning how to get better speed and utilization out of Xilinx devices. The attendees included all the top names of the EDA industry. In two days of seminars and meetings, vendors learned how to:

- Take advantage of X-BLOX architectural optimization,
- Implement memory and combinatorial logic, and
- Use system features such as carry logic, RAM, and global buffers.

Extensive use of X-BLOX was encouraged so as to free synthesis tools from many implementation details.

The Syndicate Program provides ongoing support for synthesis vendors targeting Xilinx devices. Besides an annual seminar, Xilinx technical personnel meet individually with all the vendors throughout the year to discuss particular issues. The success of the seminar in attracting representatives from throughout the industry will mean that users can look forward to better and better synthesis with Xilinx devices.

The Fourth Annual Alliance Seminar preceeded the Syndicate Seminar. The Alliance Program members were updated on enhancements in Xilinx's upcoming software release, XACT 5.0, giving them time to modify their design kits before XACT 5.0 begins shipping.

Companies that participated in the Alliance and Syndicate meetings:

Aptix
AT&T/Bell Labs
Cadence
Chronology
Compass
Data I/O
Exemplar Logic
GenRad
IBM-EDA
IKOS Systems
Intergraph
ISDATA
Logical Devices
Logic Modeling
Mentor Graphics
MINC
NeoCAD
OrCAD
Racal-Redac
Sophia Systems
Synopsys
Tokyo Electron
Topdown Design Solutions
Viewlogic ◆

SmartModel® Support for Latest EPLDs

Logic Modeling Corporation has added the new Xilinx XC7236/A, XC7272/A, XC7336, XC7354, XC7372, and XC73108 EPLDs to its SmartModel library of behavioral models. These models allow users to easily and accurately incorporate the Xilinx EPLDs into their board and system designs. In addition to the standard SmartModel features, these models include Logic Modeling's SmartModels Windows™ feature, allowing designers to look "inside" the EPLD device and change register values during simulation.

Xilinx and Logic Modeling worked closely together to ensure the accuracy and performance of the models. These new models, like all models in the SmartModel Library, have been validated for use in most commercial simulation environments.

First shipments are scheduled for the fourth quarter of 1993. For more information, contact your local Logic Modeling Corp. sales representative, or call Logic Modeling at 800-344-0004. ◆

High-Speed RAM Design

High-speed RAM can be implemented in the XC4000 FPGA by using a "read-modify-write" strategy to control memory contents.

The timing requirements of the XC4000 RAM primitive dictate that the address must be set up before the start of the Write Enable pulse (WE), and held for a short time after its end; data must be set up before the end of WE, and held until its end. While such requirements are not unusual, they are not always easily met in an LCA device.

Conventionally, the presence or absence of WE determines whether a RAM cycle is a read or a write. In larger RAMs, WE must also be gated to individual banks according to the address. A clock rate twice the RAM-cycle rate is usually required to control the timing skew created in the generation and distribution of the WE signal.

With read-modify-write operation, the RAM is read and written during every cycle. In write cycles, the data written into the RAM is new; in read cycles, the data read from the RAM is rewritten, leaving the contents of the RAM unchanged. The unconditional write permits the clock-High time to be used directly as WE. The guaranteed low skew of the dedicated clock distribution nets simplifies the design, and increases its performance.

"The address hold time will be satisfied by the output delay of the address register, provided that both the address register and WE are driven directly from the same global clock net."

A 16-word RAM is shown in Figure 1. The clock signal is used as the active-High WE, and no WE gating is provided. During the clock-Low period the address sets up on the RAM. Data is read and registered on the rising edge of the clock.

The flip-flops used for this register are available in every RAM-configured CLB and cannot be used for any other purpose, since the DIN and H1 inputs are used in the RAM operation.

The Write signal determines whether old or new data is written during the clock-High period. The selected data must be set up an appropriate time before the

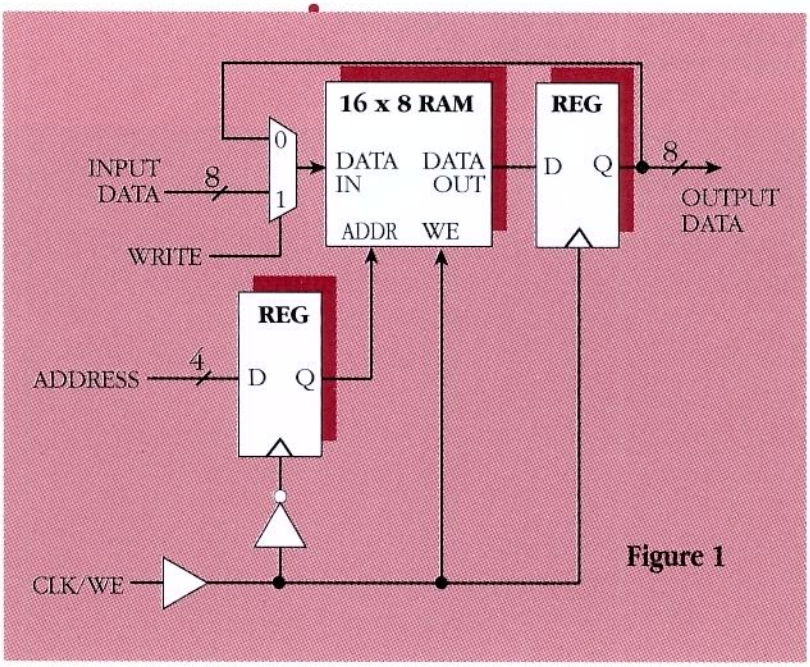


Figure 1

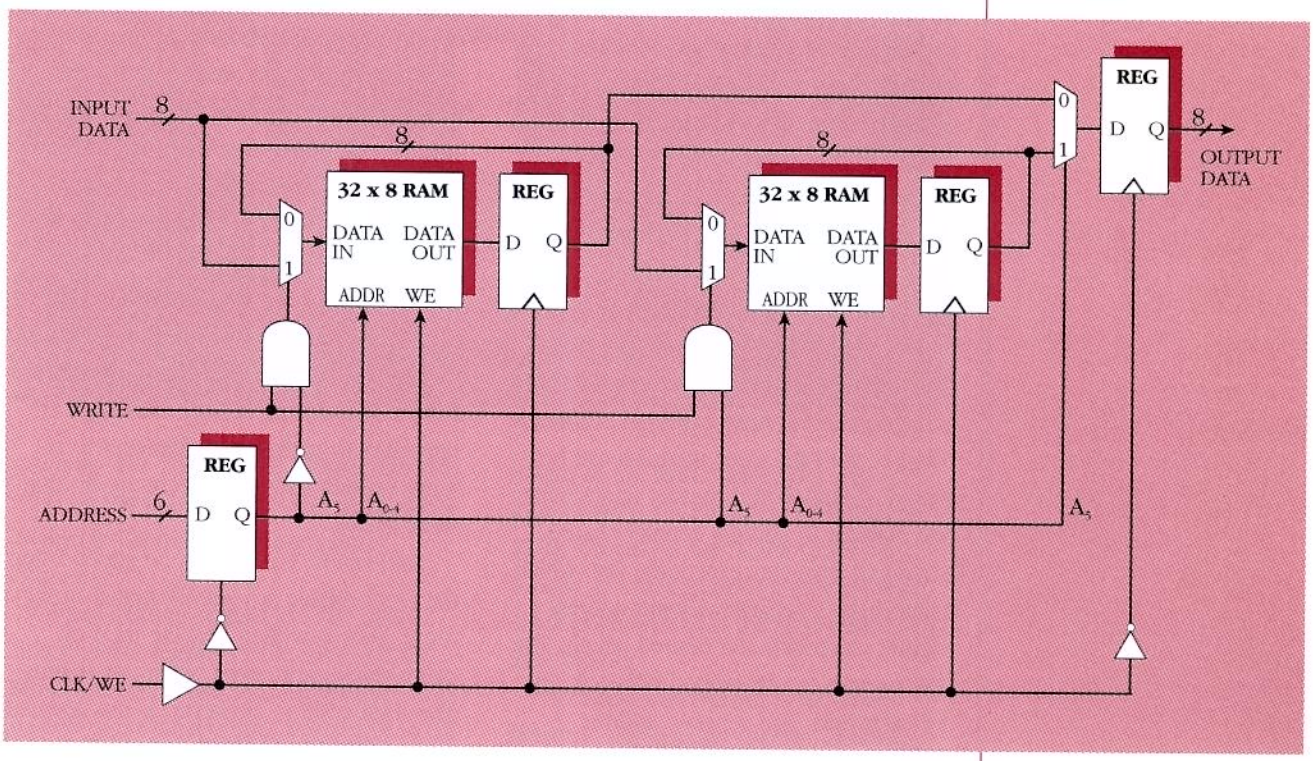


Figure 2

end of WE and held until the end of WE. This condition is easily satisfied if changes in the Input-Data and Write signals are triggered by the falling edge of Clock/WE.

The address hold time will be satisfied by the output delay of the address register, provided that **both** the address register and WE **are driven directly from the same global clock net**. This can only be achieved by using a BUFGS as the clock driver. The clock inverter for the address register is absorbed into the CLB to select the active clock edge, and does not create any skew.

Several factors control the achievable performance. The minimum required clock-Low time is determined by the clock-to-set-up time from the address register to the RAM-output register; the minimum clock-High time is determined by the clock-to-set-up time from the RAM-output register to the trailing edge of WE in the RAM. The total cycle time must permit both the Input Data and the Write signal to set up to the trailing edge of WE.

Figure 2 shows a 64-word RAM. Two banks of 32 words are used and both banks are written unconditionally. Write selection between the two banks is achieved using separate input data multiplexers. The Write control is ANDed with bank-select controls decoded from the address. Thus, data is only written to the appropriate bank. The output data from the appropriate bank is selected in a multiplexer to provide the read data output.

The pipeline stage at the multiplexer output is optional. If it is required to access the write data as it is being written, an additional connection may be made directly to the RAM outputs. The new data should be captured on the falling edge of the clock. ♦

Implementing Shift Registers in On-Chip RAM

Large shift registers can be implemented using the XC4000's on-chip RAM capability as shown in Figure 1. In this design, shift-register segments of 16-words or less are concatenated to any required length. Sixteen is chosen to minimize the RAM cycle time, and eliminate the need for bank switching or multiplexing.

For clarity, Figure 1 shows each segment having its own address counter. This is unnecessary in most cases since address counters with the same modulus can be shared. A typical shift register might have one modulo-16 address counter shared among all segments except the last, which would have a separate, shorter address counter to provide the desired length. The shift register can be tapped between any two segments, and separate address counters can provide arbitrary taps.

The address counters need not be conventional binary counters. Provided an appropriate-length address sequence is used repeatedly, the order is irrelevant. A 4-bit counter with any desired sequence can never require more than two CLBs; all four flip-flops are fed back to the four function generators, which determine the next state of their respective flip-flops. Counters based on linear feedback shift registers may use fewer function generators.

The shift register in Figure 1 does not have a shift-enable control, making it unnecessary to include a multiplexer to rewrite existing data since there are no non-write cycles.

Shift-enable control can be added using the clock-enable scheme illustrated in Figure 2. Data is written into the RAM on every clock cycle, even when not shifting. The RAM address, however, is not updated while shifting is disabled; instead, the address is held constant while the corresponding RAM location is overwritten re-

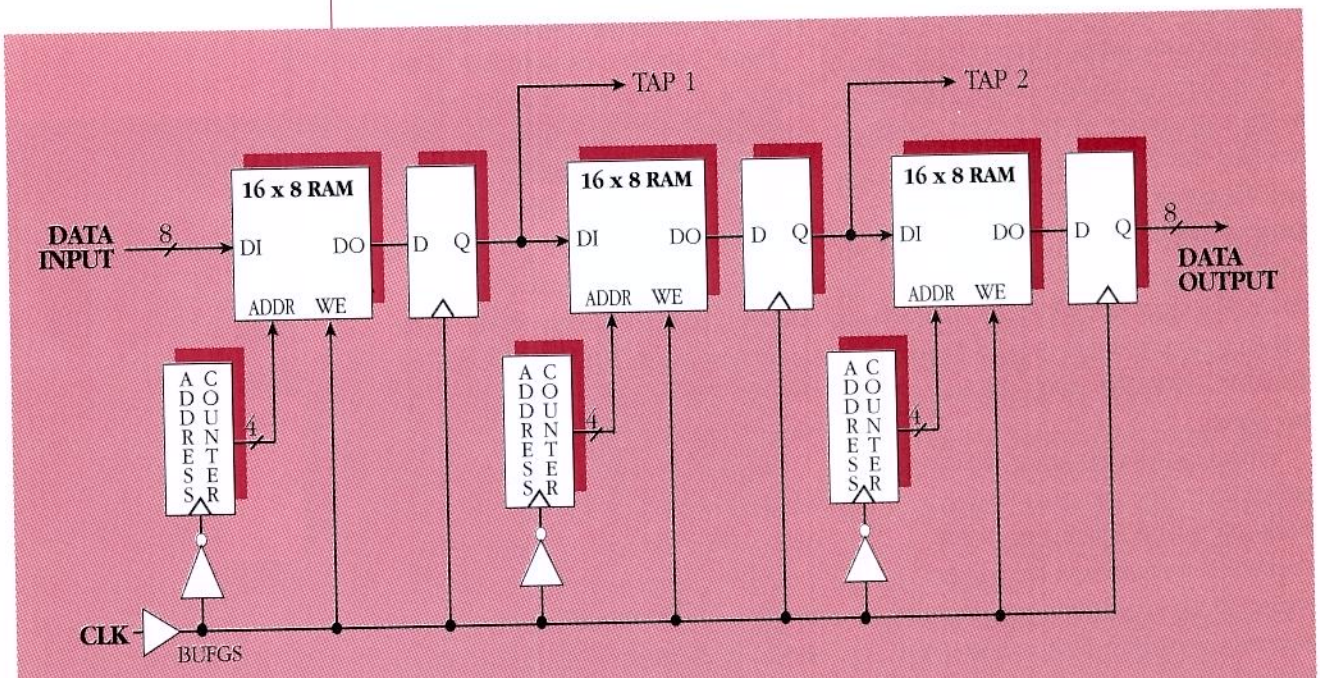


Figure 1: Byte-wide RAM-based shift register.

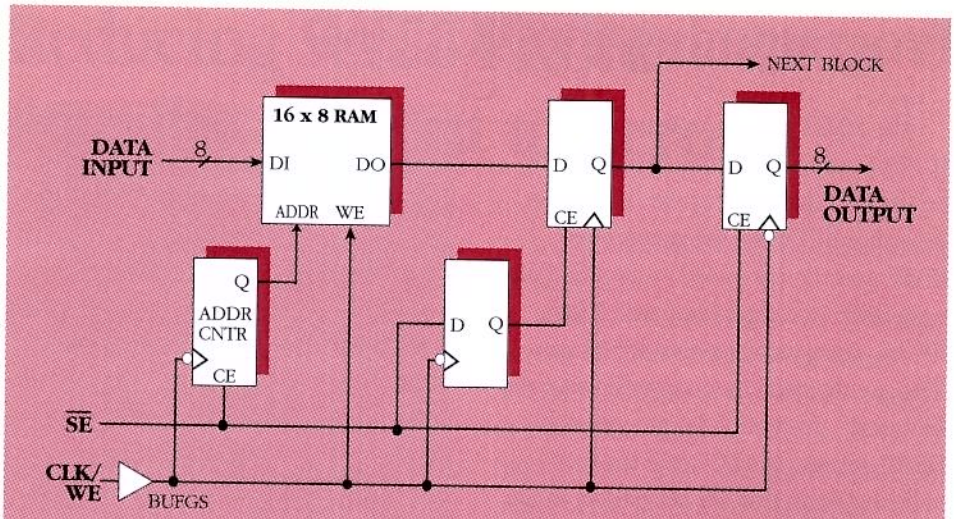


Figure 2: RAM-based shift register with shift enable.

peatedly. The shift-enable control must be valid on the falling clock edge to properly enable or disable the registers and counters.

When shifting is disabled, the data stored in the register at the RAM output remains there. When shifting resumes, it is passed to the final output register or to the next sequential RAM location. The final output register prevents the output of the shift register from changing when shifting is first disabled. This does not alter the length of the shift register (for example, in a 16-word shift register, data appears at the output on the falling clock edge exactly 16 clock periods after the falling clock edge on which the data entered the shift register).

No additional register is required between shift-register blocks. However, if there is a shift-register tap between blocks, the tap must be provided with an output register. ◆

Use Correct Lead-Pitch Dimensions

The standards for PLCC, CQFP and PGA packages were set by an American institution, JEDEC, which led to their dimensions being defined in inches, with lead pitches of 50 or 100 mils (i.e., 0.050" or 0.100").

The Japanese established the standard for PQFP, MQFP, TQFP and VQFP packages, and so used metric units. Those devices have a lead pitch of 0.5 mm, except for the 100 and 160 PQFP, which have a lead pitch of 0.65 mm.

By definintion, the lead pitch has no **accumulating** tolerance or error. However, that assumes that the values are described in their original measuring system. The **derived** valued of 25.6 mil (for 0.65 mm) and 20 or 19.7 mil (for 0.5 mm) are not exact, leading to unacceptable errors when concatenated.

For example, for the PQFP package, 0.20" is an approximation only, so always use the 0.5 mm value for laying out your PC board.

The Xilinx 1993 Data Book gives all dimensions in inches only, except for the VQ64, TQ100, VQ100 and TQ144, where dimensions are given in millimeters as well. Because of the potential for measurement discrepencies, the 1994 Data Book will provide measurements only in the controlling standard, either inches or millimeters. ◆

Programming the XC1736D

The RESET polarity of the new XC1736D serial PROM can be selected by the user, a capability that did not exist in the earlier XC1736A. Programmable RESET polarity was added to the XC1736D to enhance its compatibility with Xilinx FPGAs; using an active-Low RESET can eliminate the need for an extra inverter on the board. To control the programmable RESET polarity, the XC1736D has four additional bytes that are not present in the XC1736A. These locations do not contain user data, but control the function of the RESET pin. In a blank (unprogrammed) device, these locations are all set to the value '1', and the device operates with an active HIGH Reset. To select an active-Low RESET, these locations must all be programmed to contain '0's.

The PROM files for the XC1736A and XC1736D will be the same. The PROM file (the output from the MAKEPROM utility) does NOT contain any information regarding the RESET polarity (MAKEPROM doesn't know anything about it). The actual definition of the RESET polarity bits is done at the time of programming, and is NOT part of the bitstream. Therefore, the PROM file is the same whether or not the target device has programmable RESET polarity.

On the Data I/O programmers (and some other manufacturer's programmers, as well), the checksum for an XC1736D is different than that for an XC1736A programmed with the same code. This is due to the addition of the programmable RESET polarity and the implementation of the standard programming algorithm on the DATA I/O programmers. The checksum calculation made by the Data I/O programmer includes all bits in the device. When the XC1736D is set to active-High RESET Polarity (compatible with the XC1736A) the 32 additional RESET Polarity bits are all unprogrammed and are read as '1's. This is added to the checksum, so it is different from the checksum of the XC1736A. If converting from the XC1736A to the XC1736D in a production design, we strongly recommend that production documentation be updated to reflect this new checksum.

"Programmable RESET polarity was added to the XC1736D to enhance its compatibility with Xilinx FPGAs..."

For the Xilinx XC1736D, the internal device address for the RESET polarity bits is address 2000H - 2003H. (This *physical* address is identical on the XC1718D, XC1736D and XC1765D, and simplifies the design and programming of the device.) In the Data I/O implementation, the *logical* address on the Data I/O programmer, where the user enters the desired value, follows immediately after the end of the user-data space (locations 11B8-11BB for the XC1736D). The data I/O programmer translates this logical address to the correct physical address.

The same checksum compatibility problem does not exist when replacing the XC1765 with the XC1765D. The original XC1765 has programmable RESET polarity. Since the extra 32 bits were there all along, the original checksum takes them into account. Therefore, the checksum will be the same when programming the XC1765D with the same code. ♦

Reducing Serial PROM Standby Current to Zero

Xilinx serial PROMs have a fairly high standby (quiescent) current (close to 1 mA), which is not acceptable for battery-operated equipment. Future redesigns of these devices will power-down their internal read amplifiers and thus achieve much lower standby current.

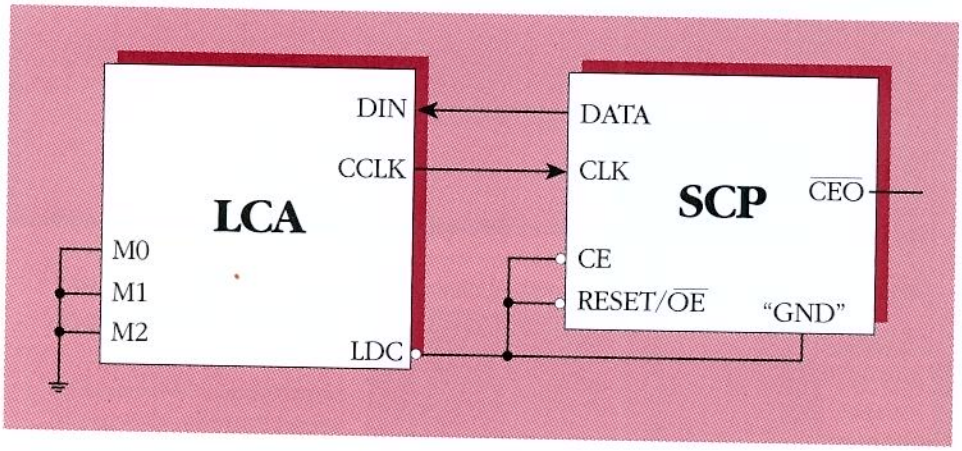
In the meantime, it is possible to achieve zero standby current by disconnecting the PROM ground lead from the system ground and connecting it to the $\overline{\text{LDC}}$ pin of the LCA. As a result, the PROM powers up together with the LCA ($\overline{\text{LDC}}$ goes Low immediately after power-up) and the PROM stays powered-up until start-up. When the user outputs go active, $\overline{\text{LDC}}$ goes 3-state and thus cuts off the PROM supply current. $\overline{\text{LDC}}$ must be configured as an input with pull-up resistor, not an active High output.

The PROM operating current (typically <5 mA) causes a voltage drop of typically 100 mV on the $\overline{\text{LDC}}$ output, reducing the PROM supply voltage by that amount. This violates the specification, but is guaranteed to work, since all PROMs are factory-tested at 4.5 V Vcc.

Multiple PROMs increase the $\overline{\text{LDC}}$ sink current by only 0.5 mA per additional PROM. $\overline{\text{LDC}}$ must never be active High, because there might be a few more CCLK pulses which would pull the PROM's CLK input below the level of the PROM "ground" pin. Therefore, in user mode, avoid driving the PROM with any active levels. That means that the $\overline{\text{LDC}}$ and DIN pins cannot be used in user mode; they should both be configured as inputs with a pull-up resistor.

The $\overline{\text{CE}}$ input must be tied to the SCP ground pin, i.e. to LDC. If RESET is active High, it must be tied to LDC, the same as CE. If RESET is active Low, it must be tied to Vcc.

This assumes a simple design with one configuration stored in one or multiple PROMs. It is inherently impossible to use this design when multiple bitstreams are stored in one PROM or one daisy chain of PROMs. ♦



Routing Tough Designs With PPR

You can instruct PPR to work very hard to optimize the performance of a design by setting the right PPR options. This will result in some or all of the following benefits:

- A design may route in a smaller device.
- A design may route to performance using a slower speed grade.
- A design may route to performance automatically, saving you the need to floorplan.

For extremely tough designs, create a file name "xactinit.dat" in your local directory which contains the following lines (leading "#" indicates a comment):

```
#ensure that xact-performance is enabled
/ppr/path_timing = true
/ppr/timing = forced_on

#the router effort is maximized without regard to runtime
/ppr/improve_routing = true
/ppr/mxmazer/ripup_allowance = -1

#activate (by removing the leading "#" character) in
#order to give PPR more freedom to optimize register
#transfer paths. You should only activate if the paths
#are non-critical to your design.
#Note: the lines with "##" below should not be edited
#(they are actual comments).

##do not transfer c2s requirements to p2s/c2p
#/ppr/extend_c2s = false
##ignore combinational paths (pin-to-pin)
#/ppr/dp2p = ignore
##ignore clock to pad (off chip)
#/ppr/dc2p = ignore
##ignore pad to setup (on chip)
#/ppr/dp2s = ignore
##do not optimize paths between flip-flops controlled by
different specs
#pa_control_other_c2s = false
#the placement effort maximized without regard to runtime
/ppr/mincut_tries = 10
/ppr/mincut_passes = 20
/ppr/seeds_to_try = 10
/ppr/improvecount = 20
```

With these options, you should expect runtimes to increase markedly, but in many cases this will enable PPR to find a solution automatically that meets your performance requirements. ◆

Additional Routing Resources in the XC3000A Deliver Higher Density and Better Performance

The XC3000A family provides additional routing resources in its architecture. The benefits are twofold: **improved performance and higher density**. For bus-oriented and TBUF-intensive designs, the XC3000A offers a noticeable improvement in routability over the original XC3000 architecture. Local interconnect resources in the XC3000A can increase by as much as 40% for bus-oriented designs.

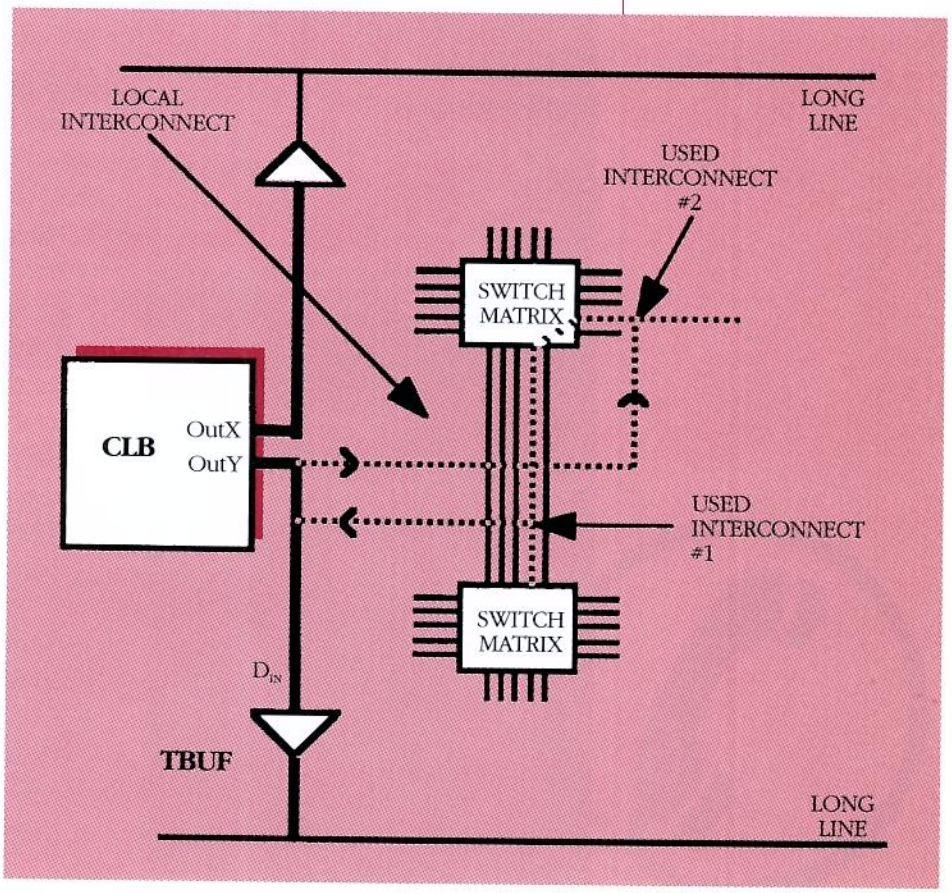
The two important routing enhancements in the XC3000A architecture are:

- A direct connection between the output of a CLB to the D_{IN} of a TBUF *(see diagram)*
- Extra routing resources between the clock-enable of a CLB and a vertical Longline.

The direct connection between the output of a CLB to the D_{IN} of a TBUF frees up two general interconnect lines. More routing resources are now available for other logic. The delays are shorter than with the previous path that used up to two interconnects.

In XC3000 devices, the clock-enable (CE) to a CLB and the three-state-enable to the TBUF share the same vertical Longline. Either the CE or the three-state-enable can access the Longline, but not both. The XC3000A allows the CE pin of the CLB to connect to another Longline. This allows both the CE and the three-state-enable to use separate vertical Longlines. Not only does this free up routing resources that were used by one of the enables, but it decreases the delay of the CE or three-state enable path. This leads to improved performance for parallel enabled applications such as counters and multiplexers.

The XC3000A is a drop-in replacement for the XC3000. However, bitstreams generated from XC3000A designs should not be loaded into an XC3000 device. *(More information on bitstream compatibility can be found in issue 10 of XCELL, page 24).* ◆



Improvements to Xilinx's XC3000A include direct connection between configurable logic blocks (CLBs) and three-state buffers (TBUFs) as shown with heavy lines. The dotted line shows the routing structure of the original XC3000 family. The change increased availability of local interconnect resources by up to 40 percent.

Using The Xilinx Technic

Wonder which options in APR or PPR will give you the fastest routing time?

Having trouble getting the DONE pin to go High after configuration?

Need some clarification regarding a section of the documentation?

Want to know how to calculate the performance of a design in the Dual-Block EPLD architecture?

If you answered "yes" to any of these questions, or similar questions of your own, then you need to know about the Xilinx Technical Support Hotline. Xilinx offers a toll free number for users to consult with a highly trained Customer Support Engineer (CSE). In addition to the hotline, users have other convenient means for obtaining help, including fax, bulletin board, and e-mail services. A summary of these services appears in the table on page 35.

Hotline Structure

Your call is initially answered by our Customer Response Center (CRC). The CRC will ask a few basic questions to ensure that you are transferred to the appropriate Customer Support Engineer. Each CSE is an expert for a particular third-party interface. Presently, our expertise includes Viewlogic, OrCAD, Mentor Graphics, Synopsys, Xilinx-ABEL, and Cadence tools. In addition, CSEs are extremely knowledgeable about Xilinx's "core products" (i.e. place and route tools, configuration, component specifications, X-BLOX, etc.).

"Xilinx offers a toll free number for users to consult with a highly trained Customer Support Engineer (CSE)."

The average call duration is 20 minutes. Because we are often quite busy, your call might have to be placed in a call-back queue. The next available CSE with the appropriate product expertise will call you back as soon as possible. As of this writing, approximately 65% of all calls are placed in a queue, and the average call back time is 30 minutes. We are working to improve on this record, and have enacted a program of additional hiring and additional training.

Getting the Best Service

You can help us to help you. When calling, faxing or e-mailing, please be prepared with the following information:

- **Name & Company** — We'll locate or enter you in the call tracking database, so no calls get lost.
- **Telephone Number** — Please provide the number where you can be reached for the next 30 minutes to an hour.
- **Software or Hardware?** — Please indicate if your inquiry concerns a software or IC product.
  If Software, then please provide:
  - **Software Product Name** — Please provide the CRC with the name of the product that is the subject of your call (such as Viewlogic's Viewdraw, Mentor Graphic's Quicksim, PPR, XACT-Performance, X-BLOX with OrCAD, etc.)

Support Hotline

- **Version Numbers** — Please provide the version number of the software product. Version numbers can be easily determined using the "utilities/version" command within XDM, or by typing the program executable at the command line without any arguments.

- **Error Messages** — If you are calling concerning an error message, please be prepared to repeat the message exactly as it appeared.

- **Platform** — Please indicate the type of platform you are using, i.e. PC, Sun, Hewlett-Packard, etc.

If IC component, then:

- **Product Name** — Please indicate the product name, i.e. XC3020, XC4010, XC73108, XC1736D, etc.

Please be patient with our questions. Since the luxury of being able to "see" the problem doesn't exist over telephone lines, precise communication is necessary, and we want to fully understand your query.

Finally, when should you call? Typically, the busiest periods are 8 a.m. to noon and 1-3 p.m. Pacific Time. Therefore, you may wish to call after 3 p.m. or during lunch. Monday and Friday are the slowest days, while Wednesday is the busiest. ♦

Summary of Technical Support services:

Customer Support Hotline:	**800-255-7778**	*Hrs: 8 a.m. - 5 p.m. Pacific time*
Customer Support Fax Number:	**408-879-4442**	*Avail: 24 hrs/day-7 days/week*
Electronic Technical Bulletin Board:	**408-559-9327**	*Avail: 24 hrs/day-7 days/week*
Internet E-mail Address:	**hotline@xilinx.com**	
Customer Service*:	**408-559-7778**	*Ask for customer service*

** Call for software updates, authorization codes, documentation updates, etc.*

"When should you call? Typically, the busiest periods are 8 a.m. to noon and 1-3 p.m. Pacific Time. Therefore, you may wish to call after 3 p.m. or during lunch. Monday and Friday are the slowest days, while Wednesday is the busiest."

General - FPGA

Q: When invoking MakeBits within XDE v4.30 or v4.31 on the PC, my mouse stops working. Why?

A: Typically, this problem occurs with Logitech mice and 2-button Microsoft mice. This problem is a known bug and will be fixed for the next release. What happens? When MakeBits is invoked for the first time after starting XDE or when the MakeBits or DebugLoad command is invoked for the first time from the Probe menu in EditLCA, XDE scans the serial ports to detect for the presence of an XChecker cable. If found, the program then knows to use the cable for all download operations.

Unfortunately, XDE sometimes mistakes the mouse for the XChecker cable, therefore causing the mouse to stop working. Below are some possible workarounds:

- If you have two serial ports and an XChecker cable, connect the XChecker cable to COM1 and the mouse to COM2. Make certain that the cable is connected and powered by the board when XDE is invoked. XDE will then find the XChecker cable before it has the opportunity to find the mouse. This will only work if the XChecker is used; other download cables will not be detected. If the mouse does not immdediately work, type "mouse com2" to reset the mouse port
- Unplug the mouse before entering MakeBits, or using the equivalent Probe commands, for the first time only. Obviously, the mouse will not be detected by XDE when the scan is done. The mouse may then be plugged in again once inside MakeBits (or once the Probe command is complete).
- Use MakeBits from the XDM menu rather than from within XDE. This problem does not occur with this MakeBits version.

Q: How do I create a bitstream for a daisy chain of LCAs?

A: In order to download daisy chained devices, you must create a single programming bitstream for all of the devices in the daisy chain. The only way to do this is to use MakePROM. MakePROM will concatenate the bitstreams of all the devices together and then calculate the total length count.

Use the LOAD command in MakePROM to load each of the bit files in the order in which they are to be connected, starting with the first device in the daisy chain. Then save. DO NOT load a bit file, save it, load a bit file, save it, etc. as this will not provide a single preamble nor a single total length count. By default, MakePROM will create a single file called <filename>.MCS. This .MCS file can then be downloaded either to the target design with XChecker or to a PROM programmer.

Q: I have several hard macros in my design. Can PPR use the unused portions of the CLBs that are in these hard macros?

A: No. Hard macro logic is impermeable. Neither the user nor PPR can access the unused portions of the CLBs that are associated with the hard macro.

"Q: How do I create a bitstream for a daisy chain of LCAs?"

General - EPLD

Q: How do I drive a product term control signal to a global net?

A: Currently, this can only be implemented using schematic entry. Treat the product term control signal as a normal macrocell output, but connect the output to the appropriate signal:

- *For clocks:* PLFCLKIO
- *For output enables (OE):* PLFOEIO
- *For clock enables (CE):* PLFCEIO

The compiler then knows to drive the respective global nets internally. The associated external pin can no longer be used, since the control signal also will drive the designated pin.

Q: What do I do with unused pins on a symbol on my schematic?

A: In order to take advantage of the automatic "logic munching" (that is, the deletion of unused logic), unused control inputs should be tied to their inactive level, unused outputs should be tied High or Low, and unused data inputs can be left unconnected. For example, to use an 8-bit counter symbol to create a 6-bit counter, tie the two highest-order counter outputs High or Low, and the logic needed to implement the upper two bits of the 8-bit counter is automatically deleted. (The connecting of unused outputs to High or Low will not be necessary starting with XACT 5.0.)

Q: When I simulate, why do I get "?" on certain nodes, but get the expected output on nets driven by those nodes?

A: These nodes are probably the output of ANDs implemented within the Universal Interconnect Matrix (UIM). You will always see a "?" on a node in the UIM. If you really need to verify the signals at these nodes, use the "OPT=NO" attribute on the instance and recompile. This will prevent optimization of the design. Be sure to go back and recompile after removing the "OPT=NO" attribute, to increase device utilization.

Q: When I try to simulate, why do I get "X" on every output?

A: The PRLD signal must be toggled from High to Low to get valid output from a simulation.

Mentor Graphics

Q: I am trying to simulate my FPGA design using Quicksim. Why do none of the flip-flops seem to be functioning correctly?

A: Typically, this results when the global reset has not been forced to its inactive state during simulation. You must de-assert the global reset with a command similar to the one shown below. Note that the global reset is active Low for the XC2000 and XC3000 families, and active High for the XC4000 family. For XC2000 and XC3000 designs, the following will de-assert the active low reset at <time>:

force //globalresetb 1 <time>

For XC4000 designs, the following will de-assert the active High reset at <time>:

force //globalsetreset 0 <time>

Continued on the next page

"A: The only way to do this is to use MakePROM."

Viewlogic

Q: I am running WIR2XNF v4.14. Ocassionally, an error message similar to the following is encountered:

Abnormal program termination: Page fault
CS:EIP = 000c:00001D4B

A: Normally, this message means that the program has run out of RAM memory. One possible solution is to use the -x option with WIR2XNF. Note, however, WIR2XNF will not automatically translate the entire heirarchy when the -x switch is used. Therefore, you must be sure to run WIR2XNF on all user created symbols that contain schematics, in addition to the top level of the design. The -x switch does not use as much RAM memory since it only flattens Xilinx created macros. The -x switch is the default used when processed within XMAKE. If the problem persists beyond this, please contact the Technical Support Hotline.

Q: How can I confiure my system so that I may use my Logitech mouse driver in the same mode for both XDM/XACT and Viewlogic?

A: For this to be accomplished, the mouse driver must be v6.02 or later. Setup the environment as follows:

1. Configure the mouse driver as required by Workview:
   mouse pc /<port#>
   example: mouse pc /2
2. Add the following line to your AUTOEXEC.BAT file:
   SET VLPCM=1
3. Verify that the XDM, XDE, and XDELAY profiles specify the correct mouse port. These files should contain lines similar to the one shown below:
   mouse com<port#>

For users of the Logitech Trackman C9 who are experiencing trouble using your mouse with XDM v2.60, we recommend the following:

1. At the command line, type: mouse init /1200
2. Remove the "set vlpcm=1" line from the AUTOEXEC.BAT and reboot.

Synopsys

Q: I am using the Synopsys FPGA Compiler. How can I optimize my results for area?

A: The current version of the FPGA Compiler, 3.0b-12654, does not map logic from different levels of hierarchy into the same CLB. You may improve your area utilization by using the following compile methodology:

1. compile (using whatever options you prefer)
2. ungroup -all -flatten
3. compile

This methodology will allow the FPGA Compiler to combine logic that may not have been in the same CLB. What is happening in step 2? The ungroup command removes all hierarchy from the design. The ungroup command also ungroups any modules that were inferred from the DW01 DesignWare library. The macros in the DW01 DesignWare library contain hierarchy; the ungroup command removes that heirarchy.

If you wish only to compile once to save time, you may use the following command to obtain similar (although not optimum) results:

compile -ungroup -all ♦

1993 Xilinx Data Book Errata

This is a list of known errors in the 1993 Xilinx Data Book. These errors will be fixed in the 1994 Data Book, expected in the first quarter of 1994.

- Page 1-6: Chart on bottom half of the page does not list 144TQ package.
- Page 2-34: In the figure, Dout goes to Din (**not CCLK**) of "optional daisy-chained LCA devices ..."
- Page 2-40: During READ STATUS, the Do...D6 data lines **go active Low**.

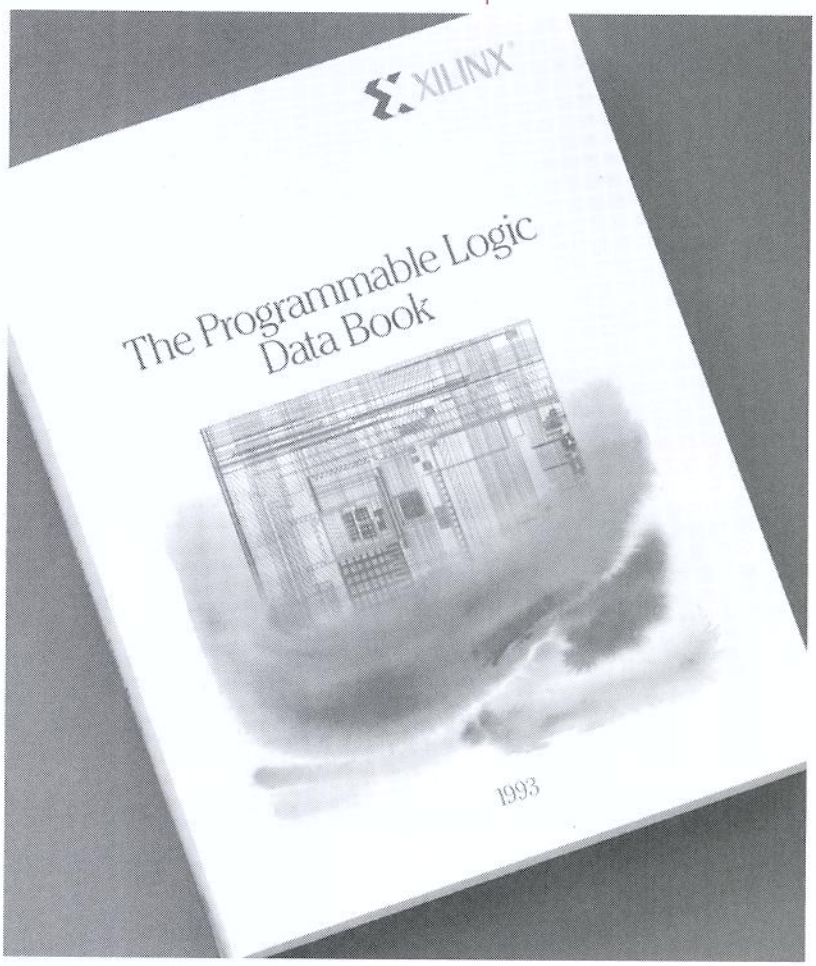
  (Affects pages 2-40, 41, and 45.)
- Page 2-41: Read Status timing diagram (top right): 'Ready' and 'Busy' labels belong **inside** the wave shape.
- Page 2-42: Program latencies are ten times longer than stated -- a minimum of **30** and maximum of **200 µs per CLB column**
- Page 2-43: The rightmost "SYN. PERIPH" heading should be "**ASYN PERIPH**"
- Page 2-50: "**T** going **toto** LL...." should read "**I** going **to**..." like page 2-68 and 2-88.

  Split-LL delay = LL delay in device with half the # of CLB columns.
- Page 2-95: For PG223 package, D5 (I/O) is bonded on pin U12, not unbonded.
- Page 2-147: I_{cco} for TTL levels is **10 mA**, not 10 µA
- Page 2-148: All numbers are wrong (they refer to XC3100). The correct values are on page 2-42 of the 1992 Data Book.
- Page 2-169: Features:

  ...**Max** powerdown and quiescent current is **5 mA**, not 0.5 mA.
- Page 2-206: "Pin 20 on 44 pin PLCC is LDC.
- Page 2-225/226: Missing capacity information for serial PROMS :

  XC1718D: 18,144 bits XC1736D: 36,288 bits

  XC1765D: 65,536 bits XC17128: 131,072 bits
- Page 3-47: end of 3rd paragraph -- "unused **Function Blocks** are automatically..."
- Page 3-48: The lower block in figure 8 should be a **Fast Function Block**.
- Page 5-1: Bulletin phone number is (408) 559-**9327** (not: 9372!)
- Page 8-15: Figure 9 has wrong caption; it should be "**Battery Back-up**". ♦



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