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Digital Design

Industry Spotlight: CAD/CAM

STD Bus Designers Guide

UPS • Video Display • Programmable Controllers

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 6/83

VOL. 13
NO. 6

"Racal-Vadic's Invisible Modem Gives Grid's Ultra-Portable Computer Access to a Whole World of Data!"

Dave Hanna — V.P. Marketing and Sales, Grid Systems, Inc., Palo Alto, California

One of the hottest personal computers on the market is the new Grid Compass. It weighs about 10 pounds and takes up less than half of a standard briefcase.

Business Week calls Compass "a Porsche for top executives."

A custom Racal-Vadic modem is behind the smashing success of Compass. This VS212A/103 modem — complete with auto dial and auto answer — is built on a 6″ by 6″ PC board. "Without this built-in modem we couldn't have made the product," says Glenn Edens, V.P. of Development for Grid Systems, Inc., Palo Alto, California.

Racal-Vadic's incredibly small modem is vital because it gives Compass a unique communication capability, setting it apart from other portable computers. For example, Compass can "talk" to another Compass... or to Compass Central, a user-owned, 240 Mbyte desk-top computer, which is designed to support a number of Compass computers in the field. It can also access Grid Central, a Grid-owned mainframe which distributes new software and provides data storage for its users. And there's more! The ultra-portable Compass can access corporate mainframes and public data bases.

Imagine... a Fortune 500 executive in a hotel room with the whole wide world of data at his or her fingertips — using the dial-up telephone.

Why Racal-Vadic? Because we invented 1200 bps full-duplex technology. Because we ship more modems than anyone. Because we utilize the most advanced automated production equipment and superb quality control. And because our custom modem department is dedicated to creating integral modems for OEMs.

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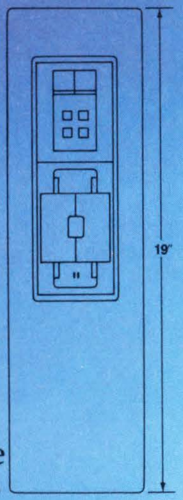

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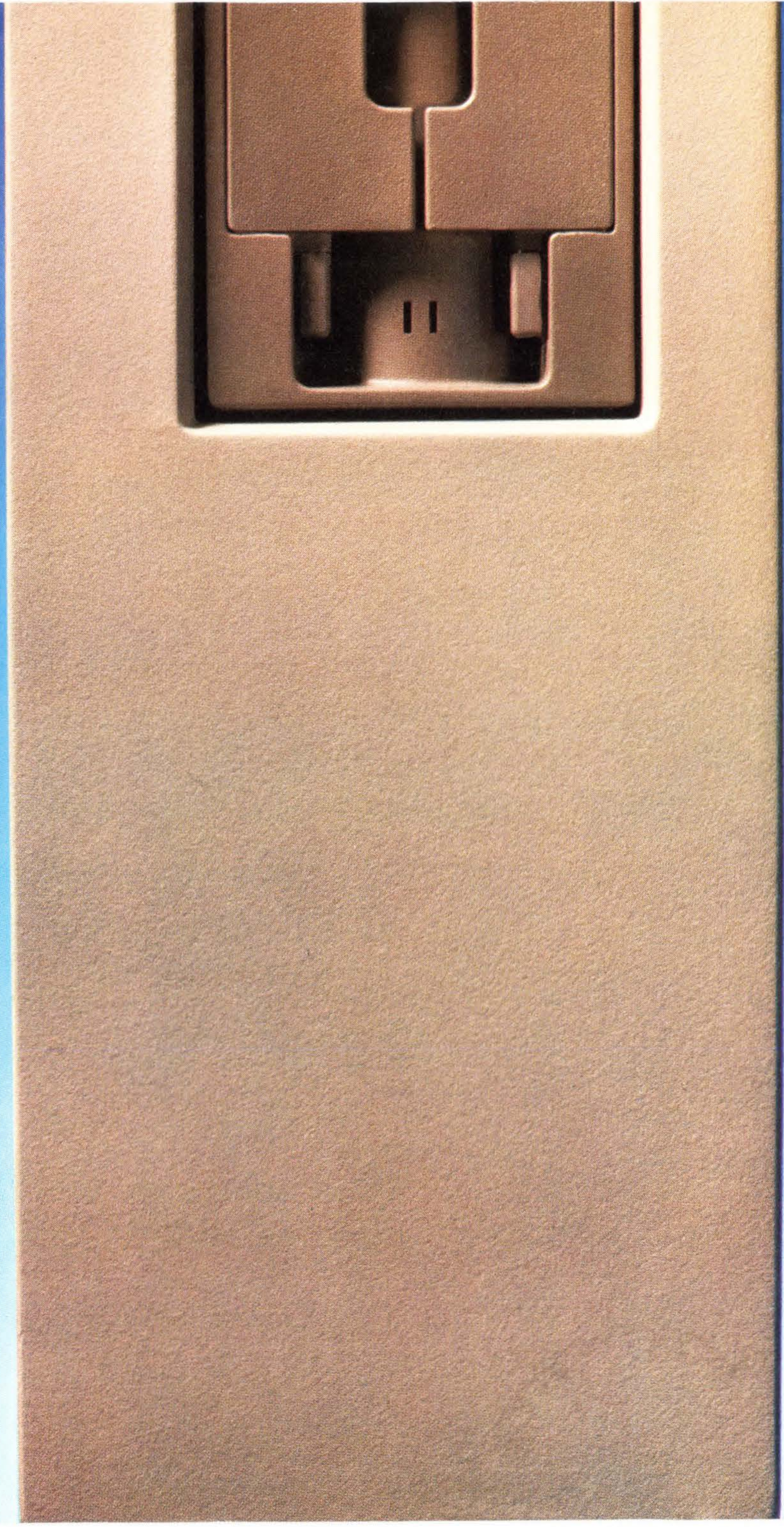

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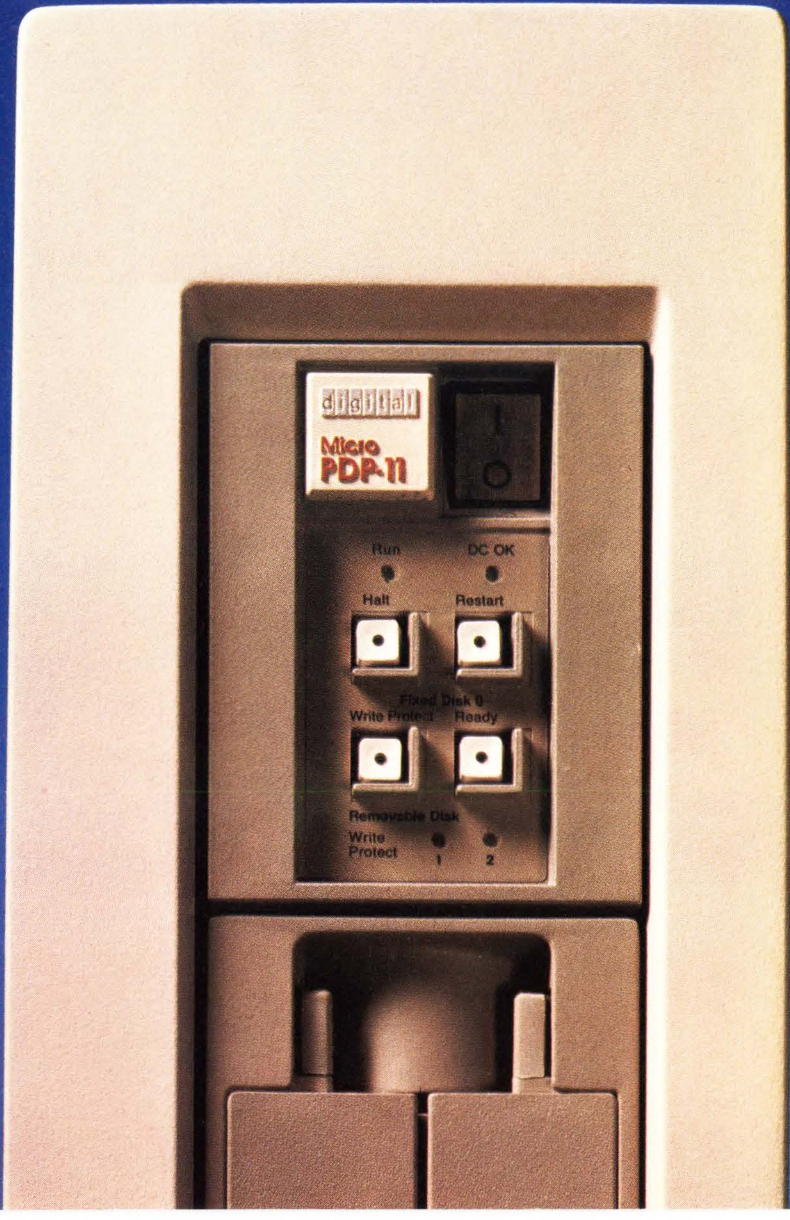

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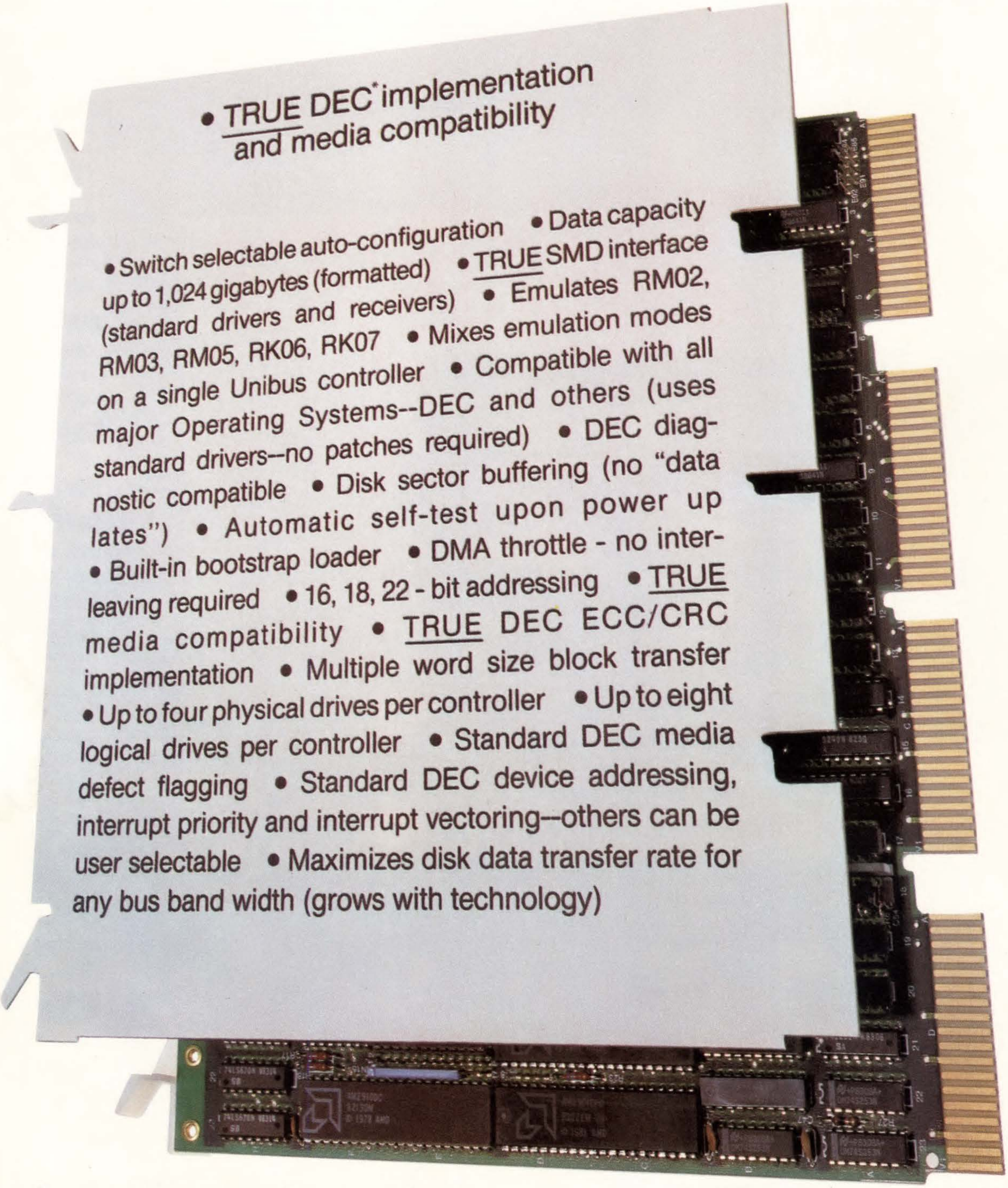

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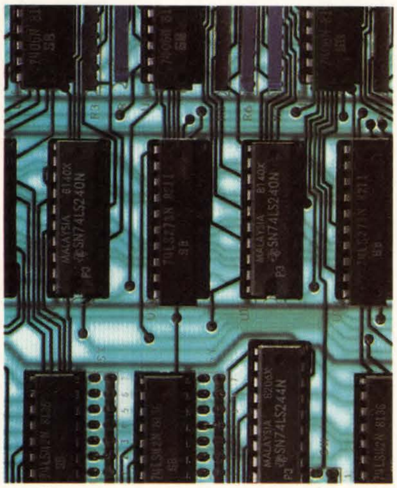
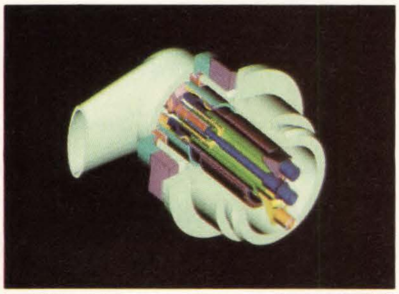
p. 22 *(photo courtesy CGX)*



p. 55 *(photo courtesy Pro-Log)*



p. 27 *(photo courtesy Aydin Controls)*

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Smart Graphics™ GX-100

The Modgraph **GX-100** is the first low cost graphics terminal to offer multi-page high resolution graphics and alphanumerics. Designed to be compatible with Plot-10® (4010/4014) and DEC's VT-100 and VT-52. We call it **Smart Graphics™** and with good reason — powerful graphics, multi-page alphanumerics and more.

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NEWS UPDATE

Emulex To Supply UK OEM

Emulex Corp. has reached agreement with Systime Computers Ltd. to supply them selected Emulex products; Systime is one of Britain's largest computer manufacturers. Systime will use Emulex's disk and disk/tape controllers and Emulex's communications controllers and multiplexers for its PDP–11 and VAX–11 systems. The products involved are Emulex's SC21, SC71, SC750, and V–Master/780 disk controllers, TC11 tape controllers, and CS11 communications multiplexers.

Priam Signs $6M Contract

Priam Corp. signed a two-year $6.0 million contract with Philips Data Systems of West Germany to supply an undisclosed number of its high performance 8″ Winchester disk drives, the 3450 (35 MB), and 7050 (70 MB). These drives employ fully servoed linear voice-coil positioners for fast data access and fit into the same space required for an 8″ floppy disk drive. Philips will use these drives mainly in the storage subsystems within their P4000 line of business computers.

Lundy, ISS, Development Agreement

Lundy Electronics & Systems, Inc. (AMEX–LDY), has entered into a joint agreement with Intelligent Software Systems (ISS) to develop a DataViews device driver for Lundy's color raster graphics products. The driver is scheduled for release in March 1983. ISS' DataViews graphics software system, allows users to compose screens of animated displays to simultaneously track hundreds of variables.

VLSI Network Solutions

Sytek, Intel, and General Instrument are working to define VLSI controllers that will improve cost-effective inter-vendor compatibility for broadband CSMA/CD networks. The Intel 82586 CSMA/CD controller is the first component that Sytek and GI are designing into broadband equipment. To promote inter-vendor compatibility, the three companies are presenting an approach to the IEEE 802 local network standards committee covering the optimal use of CSMA/CD in broadband systems. The proposed approach is based on the IEEE 802 baseband CSMA/CD specification, with the physical layer sections incorporating broadband-specific material, drawing from the current 802 token-bus broadband specification whenever possible.

Charles River Sells Line

Charles River Data Systems has sold its line of DEC-compatible peripherals and systems to Dataram Corp. of Cranbury, NJ. Products covered by the agreement include the MF211 and FD311 disk sub-systems and the RLX line of LSI–11 based microsystems.

IBM To Buy Cipher Drive

IBM, Boca Raton, FL has signed an agreement with Cipher Data Products to purchase Cipher's 1600/3200 BPI Microstreamer II ½″ streaming tape drives for the IBM Series/I computer systems. The multiyear contract is expected to exceed $10M in revenues for Cipher.

National Cuts Prices

National Semiconductor has reduced prices on all 1 MHz versions of its popular CMOS NSC800 μP family of CPUs and peripherals up to 50%, making the NSC800–1 (1 MHz NSC800) available for under $5 each in high-volume quantities. This price reduction applies to all 1MHz devices in plastic dual-inline packages and commercial and industrial temperature ranges.

Speech IC Demos

To demonstrate its new line of Real Voice speech synthesis ICs, Oki Semiconductor, Inc. has established a toll-free telephone number which gives voice messages and music and allows callers to record and play back their own messages.

Callers in the US (except California) can participate by calling 800-453-4300; in California, dial 800-858-9313.

Philips Completes Micom Purchase

Philips Information Systems has exercised its option to purchase the remaining 20% of Micom Co. The cash value of the transaction was not disclosed. Products formerly marketed in the US and Canada under the Micom label will now be sold and supported by Phillips Information Systems. These include the Philips 1000, 2000, and 3000 series of standalone and small cluster word processing systems, and the Information Management Facility (IMF) for office mail.

New Generation of Modems

Rockwell Int. Corp. has invested $10 million in developing a new generation of nine integral modem products based on VLSI technology that will be available this fall.

Because of the importance of the Japanese facsimile market, Rockwell targeted its design efforts to produce a high-speed modem for facsimile transmission of data. The R96F has on-board features such as T-30 protocol (the CCITT standard procedures and signaling scheme for facsimile transmission), and three-level equalization — adaptive, link amplitude and delay and cable.

Rockwell also plans to offer three other high speed modems: the R96MP, R96DP and R48DP, will be plug compatible and operate over dedicated unconditioned lines or the general switched telephone network with appropriate terminations. All three will allow transfer of data either serially over a CCITT V.24 interface or in parallel over a μP bus.

Two new medium-speed modem subsystems, the R1212 and R2424, were specifically designed for inclusion in personal computers, peripherals, and box modems. Both will be produced on plug compatible Eurocard-size modules.

WASHINGTON REPORT

by Anne Armstrong

Washington is a strange blend of power and inefficiency. Ideas can drift around the corridors for months, suddenly take life and become a regulation or a law almost overnight. This column is designed to track the progress of goings on in Washington, to help alert executives, planners, and implementers to what's likely and what's ahead, as well as what just happened.

The primary focus will be on executive branch decisions which affect the computer industry, on proposed legislation and its prospects, on court decisions, and occasionally on the efforts of trade associations to influence events in the city.

If everything has a season, this is the money season in Washington. The administration has sent its proposed budget to the Hill and the discussions, or haggling, if you will, have begun. For the first quarter of the year, Congress has really been tied up with funding, and there has not been any new and significant legislation.

An early skirmish in the budget war has been over the administration's attempt to eliminate most of the National Bureau of Standards' data processing standards activity. In keeping with its overall philosophy, the administration would like standards to be set by the marketplace and so the 1984 budget proposed only $3 million for the NBS Institute for Computer Sciences and Technology. Its current budget is $10 million.

After vigorous opposition from members of the DP community, academics and industry executives, the administration announced that it was reconsidering its budget request. In the meantime, however, the Senate adopted the recommendation of its Commerce, Science and Transportation Committee and restored the institute funds to current levels.

The Internal Revenue Service has spurred major computer manufacturers and software producers into action by announcing a proposed regulation to eliminate tax credits for the research and development costs of software. The Computer and Business Equipment Manufacturers Association (CBEMA) and the Association of Data Processing Service Organizations (ADAPSO) are leading the fight to defeat the proposed change. Joining the battle in late April were 37 congressmen who wrote a letter to Treasury Secretary Donald T. Regan asserting that denial of tax credits would be "contrary to the intent of Congress" when it passed the 1981 Economic Recovery Act. Hearings have been scheduled, and lobbying efforts will be intense. This is one the industry does not want to lose.

On the brighter side, the Defense Department has decided to ask Congress for $50 million to fund research and development of a new generation of supercomputers. The Defense Advanced Research Projects Agency (DARPA) plans to put the money into research at universities and corporations during fiscal 1984 as part of a project called "Strategic Computing and Survivability," but dubbed "Supercomputers" inside the Pentagon.

Although the project states its purpose is to maintain U.S. supremacy in computer technology, DARPA officials acknowledge that it is specifically designed to counter Japanese efforts to build a Fifth Generation computer. The Japanese Ministry of International Trade and Industry (MITI) is a government funded agency which works with Japanese companies and funds research and development efforts. MITI is reported to have $500 million earmarked over the next 10 years for research designed to replace dominance in large computers.

Anne Armstrong is editor of the Bulletin of the American Society for Information Science *and acts as a consultant on information technology.*

CCIA Requires Strong Separate Subsidiary Regulation

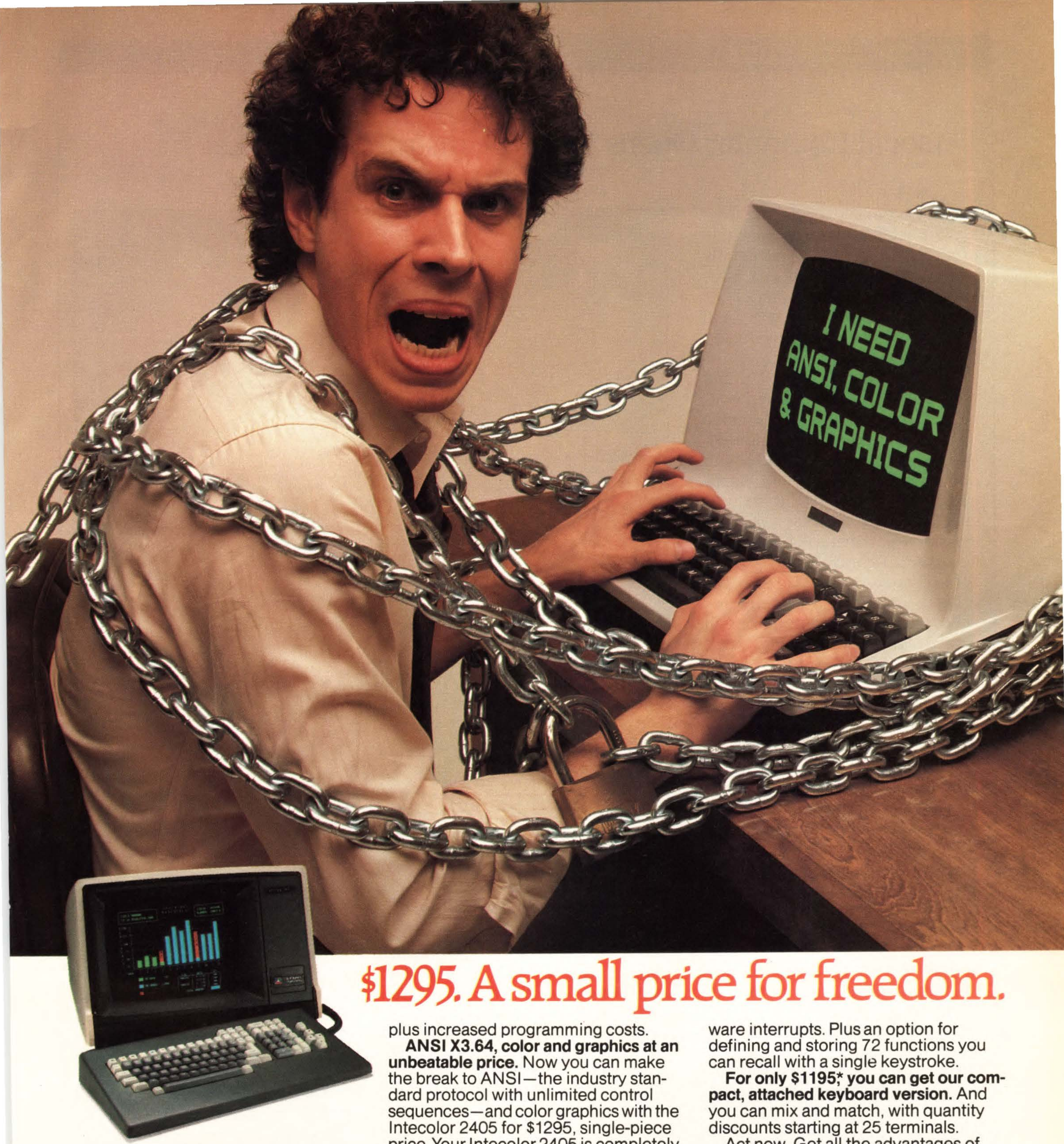
The Computer & Communications Industry Association (CCIA) filed comments on April 25, asking the Federal Communications Commission to continue to require that Bell Operating Companies (BOCs) form separate subsidiaries for the provision of their unregulated offerings after divestiture.

CCIA stated that any significant reduction of the Commission's current separate subsidiary requirements regarding the BOCs would serve to undermine the entire regulatory scheme as envisioned in Computer II to enhance competition.

The CCIA argued that there has been no show of changed circumstances sufficient to warrant the elimination of the separate subsidiary requirement for the BOCs' unregulated offerings in the post-divestiture stage. After divestiture the BOCs' incentives and opportunities for cross-subsidization of their competitive activities will continue to exist in the absence of strong separate subsidiary requirements.

The CCIA found that full separation through subsidiaries is the best means of discouraging the misuse of the divested BOCs dominant position in the marketplace. Without separation, CCIA cautioned the Commission, the BOCs' offerings of regulated services and non-regulated products will be inextricably intertwined. CCIA noted that the costs of providing unregulated products would likely become an issue in the BOCs' rate tariffs filed with the states, threatening the Commission's entire deregulatory scheme. Failure to require separation will likely result in no uniformity in the structural restrictions placed on BOCs.

For more information contact: *Computer & Communications Industry Association, 1500 Wilson Blvd., Suite 512, Arlington, VA 22209. (703) 524-1360.*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Personal Computer Opens Up New Instrument Market

By the end of the 1970s, the market for intelligent, programmable products began to expand rapidly as most traditional test and measurement companies, such as Hewlett-Packard, Tektronix and Philips, introduced μP-based instruments.

The demand for sophisticated test and measurement devices remained concurrent with the move to incorporate μP technology. Simple measurements made with one or two probes, and hand-guided through a circuit to provide a visual display of raw measured parameters, became inadequate. Relatively large numbers of nodes now needed to be probed; many test occurrences needed to be acquired; and often data needed to be accumulated, sorted, calculated or otherwise interpreted prior to presentation to the user. In addition, testing time became important as a result of the large and complex nature of the task.

In order to meet these needs, general purpose computer controllers were added to stand-alone instruments through instrument interface buses (e.g. GPIB). Using this approach, a group of instruments designed primarily for stand-alone operation are made to operate as a system. As a result of this bottom-up approach, the solution is not generally optimized for minimal cost of the computer and instrument functions or for maximum efficiency of interactive system level operation. The expense of purchasing the system components, and the time involved in programming system functions according to pre-defined formats, has restricted the application of these bus-based instrument systems.

By designing general purpose instrumentation products closely coupled to the personal computer, Northwest Instrument Systems (Beaverton, OR) has avoided duplication of the processor, memory, display and human interface found in traditional instrument systems (**Figure 1**). The new architecture provides the user with direct access to a general purpose computer, allowing the user to perform extensive analysis, customization of displays, and peripheral control at a systems cost which the company claims is 3–10 times less than conventional instrument approaches.

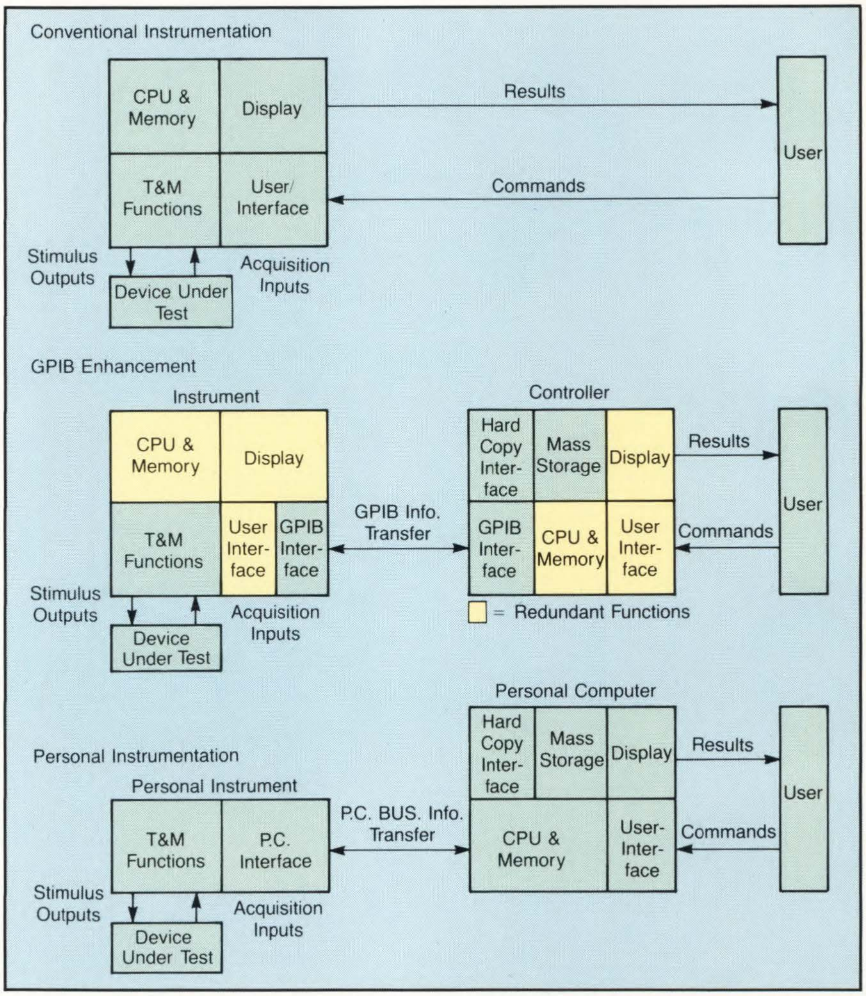


Figure 1: The personal instrumentation approach removes duplication of function.

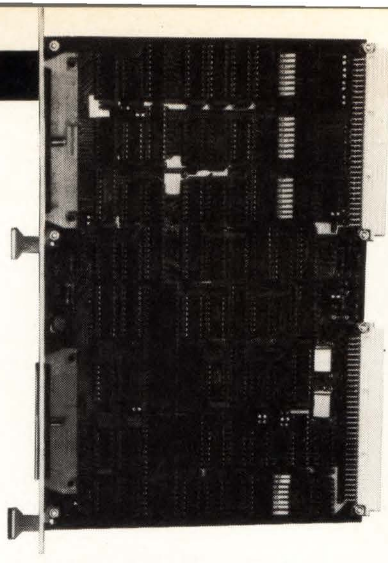
Northwest introduced Model 85 aScope, the first instrument based on the personal instrument approach in February, 1982. The Model 85 aScope is a Digital Memory Oscilloscope which operates as a peripheral to the Apple II personal computer family.

On March 31, 1983, NWIS added three new members to its personal instrument family: The μAnalyst 2000 Mainframe and the Model 2100 Interactive State Analyzer; the Model 65 aGen Programmable Function Generator, and the Model 75 aSource Arbitrary Waveform Generator.

The primary market focus of NWIS is technical applications, especially engineering design and manufacturing test. Other key market segments include medical, physical science, education and depot service applications. All NWIS products will provide "hooks" such as user programmability, user application libraries, and modular design, for volume-end users and OEMs to drive products into vertical markets.

Write 231

VME Bus Market Growth Imminent



Elite Corp.'s VMEbus Card.

The acceptance of any bus-specific designs in the marketplace is related to a number of critical factors that influence manufacturers, or prospective manufacturers of products for that bus. Major competitive advantages of the VME bus that may appeal to manufacturers over other bus architectures include its 32-bit data bus, DIN connectors and Eurocard compatibility.

For many, it appears that the bus looks like the successor to the Multibus, although with the imminent introduction of Multibus 2 many are taking a "wait and see" attitude. The VME bus is, at present, in the "chicken or the egg" stage of development.

When an OEM commits to a bus, he must be certain that a wide range of products are available: CPUs, memories, I/O cards, etc. to support his design. Although the spec may look impressive, if no product exists he must change his product plans. A manufacturer will not commit to a bus unless a specific market does already, or is certain to, exist. Historically, the market push for a specific bus has come from the company that spec'd the bus initially. Intel's Multibus and Pro-Log's/Mostek's STD bus are prime examples of companies that introduced a wide variety of products to capture market interest early. The proliferation of third party interest that followed owed a lot to the product and marketing skills of the bus inventors.

In a recent questionnaire prepared by Fred Mazanec at the Ironoak Co., (La Jolla, CA) a major manufacturer's product offering was cited as one of the reasons fundamental to a third party vendor's decision to manufacture VME-based products. At present Mazanec has identified 29 manufacturers who currently manufacture VME buses, 35 who definitely plan to manufacture, and 50 who are taking a "wait and see" posture.

Finally, a single source for multi-processor, designed for OEMs and systems integrators. Now that's intelligent.

Intelligent Systems introduces the Datavue multi-processor, multi-user computer system.

The Datavue system offers OEMs and system integrators a powerful solution for multi-user, multi-tasking, terminal-based environments—and all the advantages of single-sourcing.

With Datavue you configure just the right amount of computer power for current needs and deliver to your customers a simple, economical growth path from one to eight users.

Advanced systems architecture delivers stand-alone performance. For advanced applications—decision support systems, office automation, management productivity, and even process control—Datavue provides a simple computing environment with a dedicated computer for each user (or control application).

Up to eight computer cards can be inserted in the Datavue system which resource shares mass storage and common I/O. Each user gets a full microcomputer with a Z80A, 64Kb RAM, and CP/M* 2.2. As a result, all users get stand-alone performance with the economies of a multi-user shared resource system.

Add intelligent terminals to meet your customers' needs. Since 1973, Intelligent Systems has been a world leader in designing and manufacturing color graphics terminals. Now, you can profit from our expertise with: The Intecolor 2405, the indus-

One-on-One Architecture For IBM CAD/CAM Network

CGX Corp. has introduced the Graphics Display System 2001, an IBM-compatible network of interactive workstations designed to perform mainframe-based computer-aided design and manufacturing (CAD/CAM) tasks.

The display system lets users mix independent color raster and monochrome vector terminals on a single cable network due to CGX's multiprocessor-based "One-on-One Architecture" which incorporates a dedicated graphics processor in each workstation.

The mainframe-based CGX 2010 Channel Unit can run any combination of up to 16 color and monochrome CAD/CAM workstations, on a single coaxial cable stretching up to two miles. The CGX 2020 Vector Display Station and the CGX 2030 Color-Raster Display Station emulate the IBM 3250 Graphics Display terminal, and are each designed to provide the interactive response speeds required by CADAM, CADAM PRANCE, NCAD, CATIA, CAEDS, and other IBM-compatible CAD/CAM graphics software.

Running from IBM series 360/370, 30XX and 43XX family, or IBM plug-compatible host mainframe computers, the basic system includes: the CGX 2010 Channel Unit; the CGX 2020 Vector Display Station; and the CGX 2030 Color-Raster Display Station.

The Channel Unit connects directly to any block multiplexer or selector input/output (I/O) channel of the host mainframe. It controls the interface between the graphics application software program and the Display Stations, passing host-supplied data and control information to each workstation along the coaxial cable. CGX will also offer other network communications options, including 56 Kbyte Bell Digital Data Service, Bell T-1, microwave, and fiber optics system links.

Each CGX Channel Unit contains separate processor and channel interface boards. The processor board dedicates each of three μPs to specific tasks. An Intel 8088 command processor supervises internal timing, data trans-

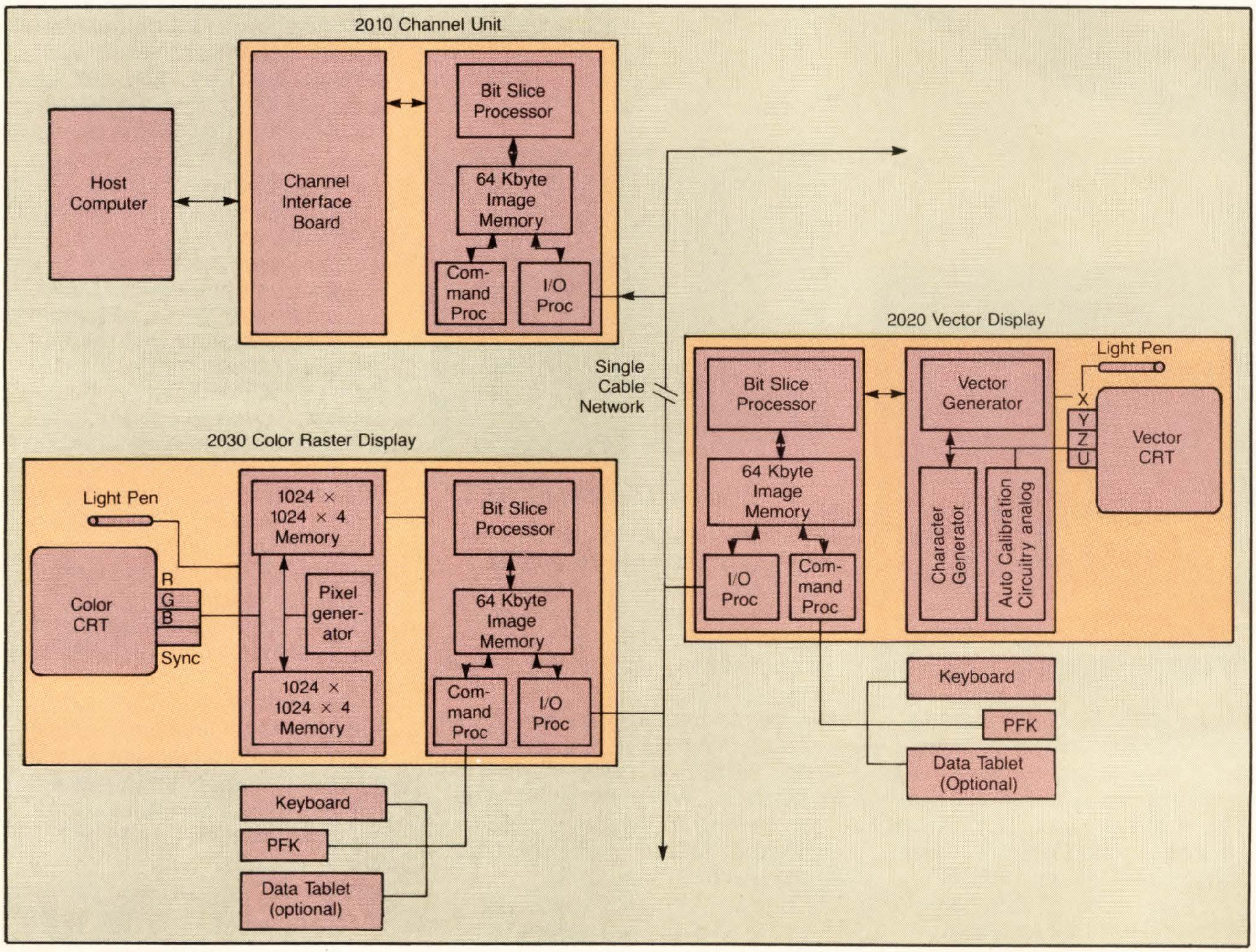


Figure 1: Graphics display system 2001.

fers, interrupts and control-panel communications. An AMD 2901 bit-slice processor connects to the channel interface board, depositing data, status, graphic commands, image programs, and address information from the host into the Channel Unit's 64 Kbyte data buffer. The Intel 8089 I/O processor transfers that information to the selected Display Station, where the workstation's local graphics processor converts it into image information. The CGX-developed Graphics Microcode Operating System (GMOS) stored in the Channel Unit and each Display Station governs these data transfer processes.

The Channel Unit enables network data transfers to and from the host computer at speeds up to 1 Mbyte/sec, twice the data-transfer speed of the IBM 3250 system. This frees the host for other tasks by minimizing I/O channel loads. The Display Stations can be connected anywhere along a two mile long cable, and have direct access to the cable network and the host-based Channel Unit for faster response times. The Channel Unit transfers information to and from the Display Stations at rates up to 1.67 Mbits/sec.

The two dedicated graphics-processor boards in each display also use Intel 8088 command, Intel 8089 I/O, and AMD 2910 bit slice processors, and feature 64 Kbytes of buffer memory storage for graphics image data. This same multiprocessor-based design, combined with the fast pixel-writing speed and screen refresh rates of the Color Raster and Vector Display Stations, provides flicker-free images and response times under 0.4 sec to an operator's light pen inputs.

Both color and monochrome workstations have as standard a light pen, an adjustable 32-key programmable function keyboard, and an alphanumeric keyboard. CGX also supplies an optional data tablet and stylus for light pen emulation and digitizing.

The Vector Display Stations have a black/white 21″ diagonal CRT screen with 4K × 4K addressable-point resolution, while Color-Raster Display Stations feature a color 19″ diagonal screen with 1024 × 1024 pixel resolution. The display has eight user-selectable beam intensities for highlighting vectors. The vector unit refreshes stored images in the buffer memory at 60 cycles/sec, and redraws screen line images at 500,000 ins/sec, practically eliminating CRT flicker.

The Color-Raster terminal uses dual memory buffers to rapidly update and refresh pixel images within the 0.4 sec response time desired by users of CADAM-compatible software. The color workstations also draw polygon fills, display 16 colors from a 4096-color palette, and feature a hardware graphics cursor.

Both vector and color raster displays can draw solid, dotted, dashed, and dot-dashed lines. Each station contains a 96-character EBCDIC set with nine special engineering symbols, emulating IBM 3250 small, medium, basic, and large character sizes.

The Vector Display Station also incorporates CGX's Auto Calibrate feature, which self-calibrates, automatically adjusts, and locks in the screen image without manual or mechanical adjustments.

A typical CGX Graphics Display System 2001 configuration, consisting of four CGX Model 2020 Vector Display Stations; four CGX Model 2030 Color-Raster Display Stations; and a CGX Model 2010 Channel Unit, is priced at $299,000. Individual component prices are: $23,000 for the Channel Units; $27,000 for the Vector Displays; and $42,000 for the Color-Raster Displays.

CGX Corp., 42 Nagog Park, Acton, MA 01720

Write 233

Figure 2: The 2030 raster display.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- Individual windows can emulate different system protocols.

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- Graphos supports a host and most input/output devices. . . truly device independent.

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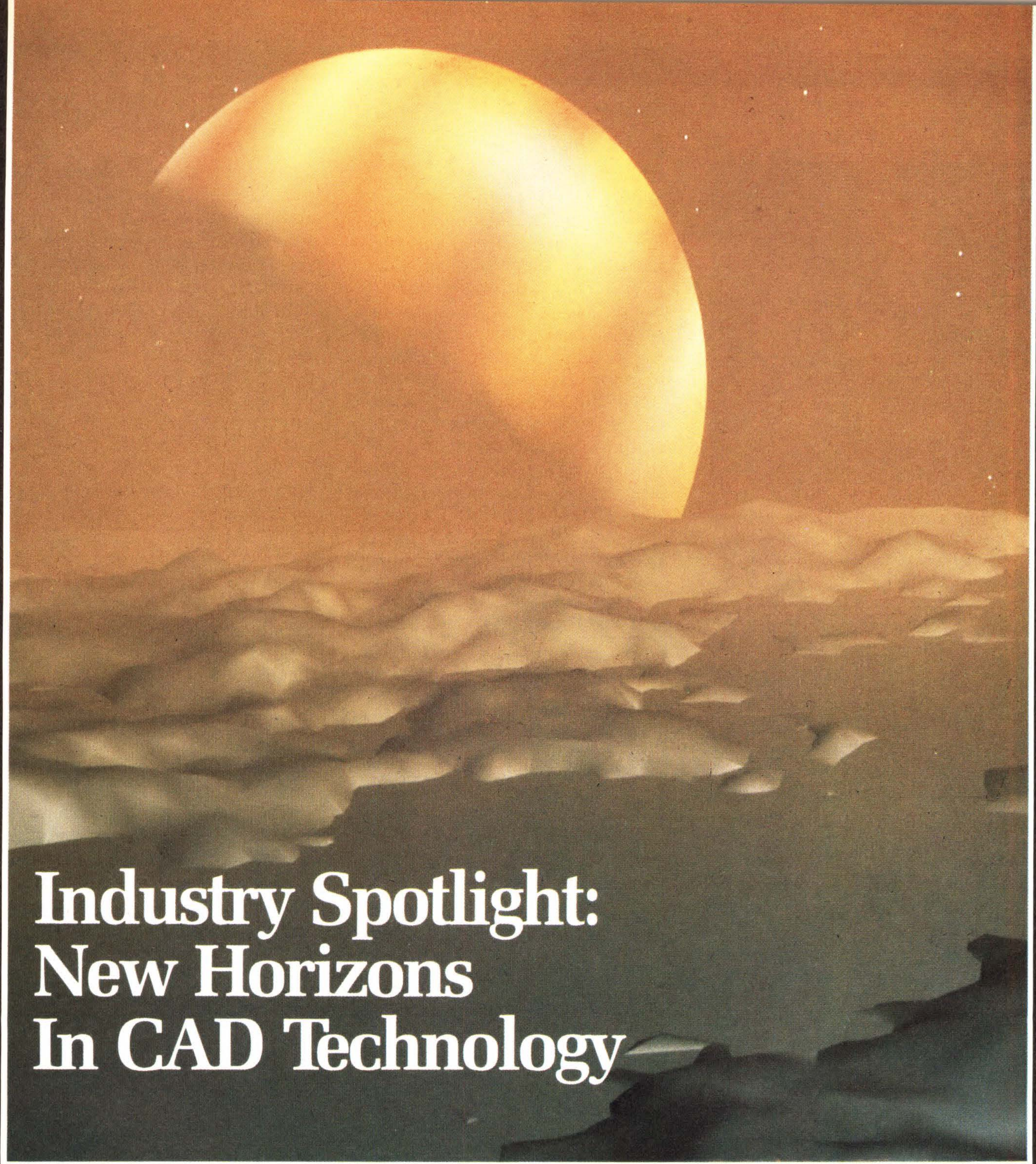

Industry Spotlight: New Horizons In CAD Technology

Digital Scene Simulation, photo courtesy Digital Productions, Los Angeles, CA.

Decreased system costs and increased capabilities are bringing CAD/CAM into new environments and applications.

by Jerry Borrell, Editor-In-Chief

Computer-aided design (CAD) in industry has become so widespread that it is difficult for designers to be familiar with all of its related developments. The three primary applications of computer graphics to industry are: CAD, which may mean computer-aided design or computer-aided drafting; CAM, computer-aided manufacture; and CAE or computer assisted engineering.

Each name implies a different focus. CAD as drafting means that the computer is used to provide the designer or draftsman with graphic tools that automate drawing, storing and manipulating designs. CAD as design provides the draftsman with integrated capabilities such as analysis and aesthetic evaluation. CAM most often describes the application of CAD tools to the processes of manufacturing. Typically, output

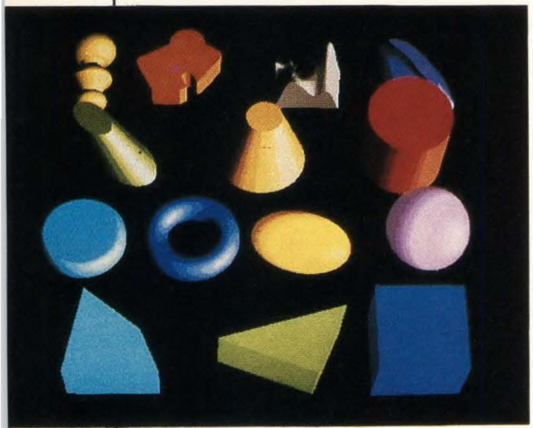

Figure 1: Geometric primitives may be combined or modified to create objects used by designers as tools of software interaction. Photo courtesy MAGI Synthavision.

from a CAD system provides input for devices performing numerical control of milling or other manufacturing devices. CAE primarily describes the application of computers to analysis and testing of engineering concepts.

All of these areas overlap to form more comprehensive groupings of technology. These groupings are known collectively as computer integrated manufacturing or process technology. Three factors are acting to combine disparate elements from these areas.

- The graphics display's growth as a medium of visual communication.
- Software systems that are developed with subroutines from design, analysis, and manufacturing.
- Increasingly intelligent computing devices that can perform functions in all three of the areas mentioned.

With industry making a transition in design, analysis, and engineering, the application of these new technologies is more complicated, and system builders and suppliers will likely be faced with these problems for the next several years. Hardware and software trends are probably the best indicators of what the problems are and how manufacturers of graphics systems are addressing them. The marketplace provides indicators of likely solutions in terms of users' demands and developing markets resulting from converging technologies.

Hardware Trends

CAD systems developers have traditionally been at the forefront of graphics systems design. Some of the changes being introduced into systems design are a result of European ergonomic standards: CRT adjustment, work surfaces and detached keyboards. Other machine-related design changes include resolution, color, and increased intelligence.

Screen display resolution of 1024^2 appears to be a near de facto standard for CAD applications. There are two notable caveats to be added here. First, some systems providers, such as Raster Technologies, achieve displays of extremely high quality by use of anti-aliasing and color—Raster's 512^2 system can, for example, use up to 22 bit planes of color memory. Other firms, such as Lundy, offer up to 1500 × 1200 pixels of display, but allow a much smaller portion of the screen to be viewed at one time through maneuverable windows. Displays from Lexidata, Genisco, and others are actually displayable and viewable at 1024^2 (Genisco terminals have a bit map display of 4096^2).

One problem is that few display monitors with very high pixel resolution are currently available. Japanese manufacturers dominate the field (Ikegami, Mitsubishi, Sony, & Hitachi), but even they are unable to produce large quantities of 1024^2 CRTs in the near term.

The increasing use of raster display tubes is exemplified by their use by such long standing firms as Adage and Lundy, whose primary markets are in vector refresh tubes. The demand for high qual-

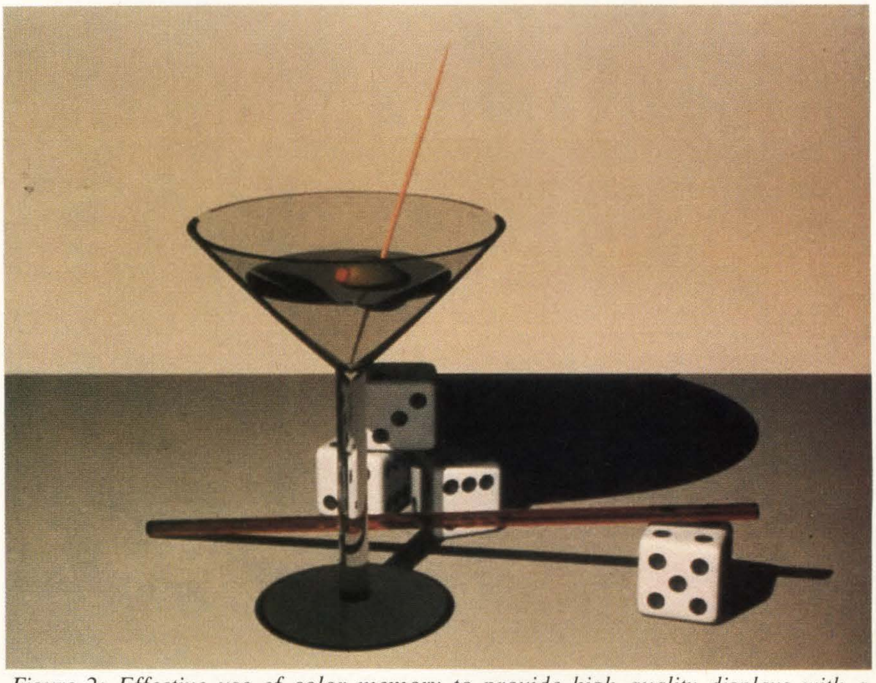

Figure 2: Effective use of color memory to provide high quality displays with a screen resolution of 512 × 512. Photo courtesy Raster Technologies.

Jerry Borrell is the Editor-in-Chief of **Digital Design,** *and has been active in the computer graphics field since authoring a key report, "Computer Graphics Technology And Applications" for the U.S. Congress. He is presently the Director of Information Resources International, a Washington, DC consulting firm, and North American Editor of* **Electronics Publishing Review.**

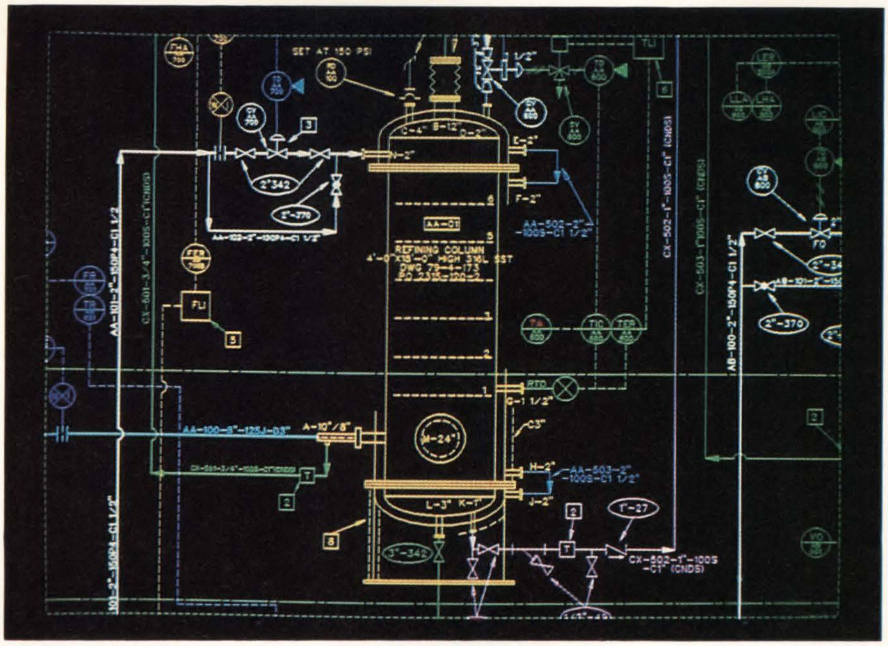

Figure 3: Wire frame drawing of a pressure vessel represents automated drafting applications of CAD. Photo courtesy Calma.

ity displays has pushed a move towards non-interlaced (60Hz) tubes for even better display quality through decrease in flicker (the distortion that occurs when alternating fields of the display are redrawn in interlaced tubes).

Color has become popular not merely because it is available, but because engineers and designers use it to increase effective communication. Color may be associated with data from analysis in engineering or with discrete parts in the makeup of design such as integrated circuit layers or mechanical assemblies. Light, shading and dimensions also improve communications.

Both color and resolution are enhanced through increased functionality of logic in systems. These technical changes have three origins: the availability of μPs with larger address spaces (i.e. 32-bit processors); the use of logic devices such as bit slice processors; and the implementation of graphics display functions as firmware or hardware.

The most common approach to 32-bit addressing is the use of Motorola's 68000 family of devices; implementors include Adage, Florida Computer Graphics, Lexidata, Applicon, Raster Technologies, Calma, and Apollo. One criticism of the 68000 is its 16-bit I/O data channel, a limitation Apollo addresses through use of the 68010, which has a page fault capability that allows it to accept 32-bit blocks of data. Other companies use the AMD 2900 series of 4-bit μPs incrementally to form processors of 4, 8, 12, or 16 bit data channels. Superset uses 12 2901s in its FORTRAN engine to allow a 48-bit word length. The 2901 arithmetic logic unit is combined with a program sequence controller and additional chips as needed. Their primary advantage is in high speed program execution for drawing graphics displays. Computervision and Hewlett-Packard have developed their own 32-bit processors—an effort that few companies can support.

Control Data offers users of its ICEM CAD package 64-bit word length on its Cyber supercomputers, but this is clearly beyond the scope of most CAD systems. The HP approach appears to offer the most flexibility, and the HP-9000 in a 9030 configuration of three CPUs is expected by many to become a benchmark for small systems. The 9030 will support a UNIX operating system and has a whetstone rating of 0.8 to 2.3 MIPS. In this power range, both Apollo and HP claim to be the top competitors for the VAX 730/750 based systems.

The second of the approaches to increasing intelligence, adding capability for graphics functions, is best represented by firms such as Evans & Sutherland, Megatek, Calcomp, Lexidata, and Genisco, who have implemented software routines for graphics operations. Most often called "display lists," functions stored in PROM accumulate actions such as vector definitions, primitives and attributes as directly-accessible commands which allow the fast processing of capabilities for variable zoom, clipping and transformations. Another technique for increasing graphics capability is the use of dedicated graphics chips such as the NEC 7220. Genisco has combined the 2901 and 2 NEC chips for extremely fast processing.

Many firms such as Apollo still use one central CPU for all arithmetic functions—both graphics and non-graphics—and the larger address space and speed of 32-bit processors makes the implementation effective. However, most firms show a trend toward dedicated processing. Lexidata's latest product, Imageview, combines hardware, software, and firmware functions for graphics, indicating that developers of graphics chips or custom products have a great deal more development to do to remain current with graphics software.

These advances provide system designers with many options for implementing graphics: board-based products, rack-mountable systems as standalone or host supported systems, and standalone work stations incorporating display, keyboard and I/O as configurable elements. Jupiter Systems indicates a trend towards increased power in standalones: an additional processor in its keyboard effectively offloads the central CPU for graphics processes.

Hard Copy

Ironically, hardcopy output has become one of the greatest strengths and weaknesses of the CAD field. Mechanical and electrostatic hardcopy systems can output drawings on different media (paper, mylar and film) at high speeds and with great accuracy. The increasing use of raster devices, however, introduces difficulties, because unlike vector systems, raster devices have no output devices of plotter quality at acceptable cost. Color camera and ink jet systems are now best for color output, and electrostatic is best for monochrome. However there is no device for color analogous to the Tektronix silver paper production system with its low cost, fast production, and high resolution.

Few users can now use photographs or ink jet drawings for working copies of CAD output. Calma will be providing its users with an option for the new Versatec color electrostatic printer, but the cost (about $100,000) is high and the application (PC/IC layout) is particularly suitable for the format. Ink jet and thermal color devices are continually improving, but problems remain. The RGB output from display devices to hardcopy systems, for example, has several difficulties: impedance, resolution shift (from display to output system), daisy-chained hardware, and the interface to camera systems. DAC circuits in hardcopy devices introduce further inaccuracy. Genisco and Tektronix address the latter problem by using their IEEE 488 interface for the digital transmission of signal to hardcopy. Solid modeling systems exacerbate this shortage, and there is no best solution in sight.

Custom Processors

Many manufacturers indicate that over the next two years they will attempt to implement graphics generators in hardware. Gate array technology offers the most promising avenue for custom work, but this is only beginning to be practical for companies with the low production volume of most graphics manufacturers. Others point out that discrete logic will be as effective in the near term for graphics processing and that the primary advantage in using gate arrays is reducing space rather than increasing capability.

Software Trends

Software development is the key to improvements in the design process and continued growth of sales for manufacturers; as a medium of machine/designer interface, CAD software determines the efficiency of the entire system.

Traditionally there have been three types of interaction: command, prompt and menu based software. Within menus the use of applications symbols and command libraries has proliferated for both screen and tablet overlays; Calma, Applicon, Calcomp, Intergraph and others offer several

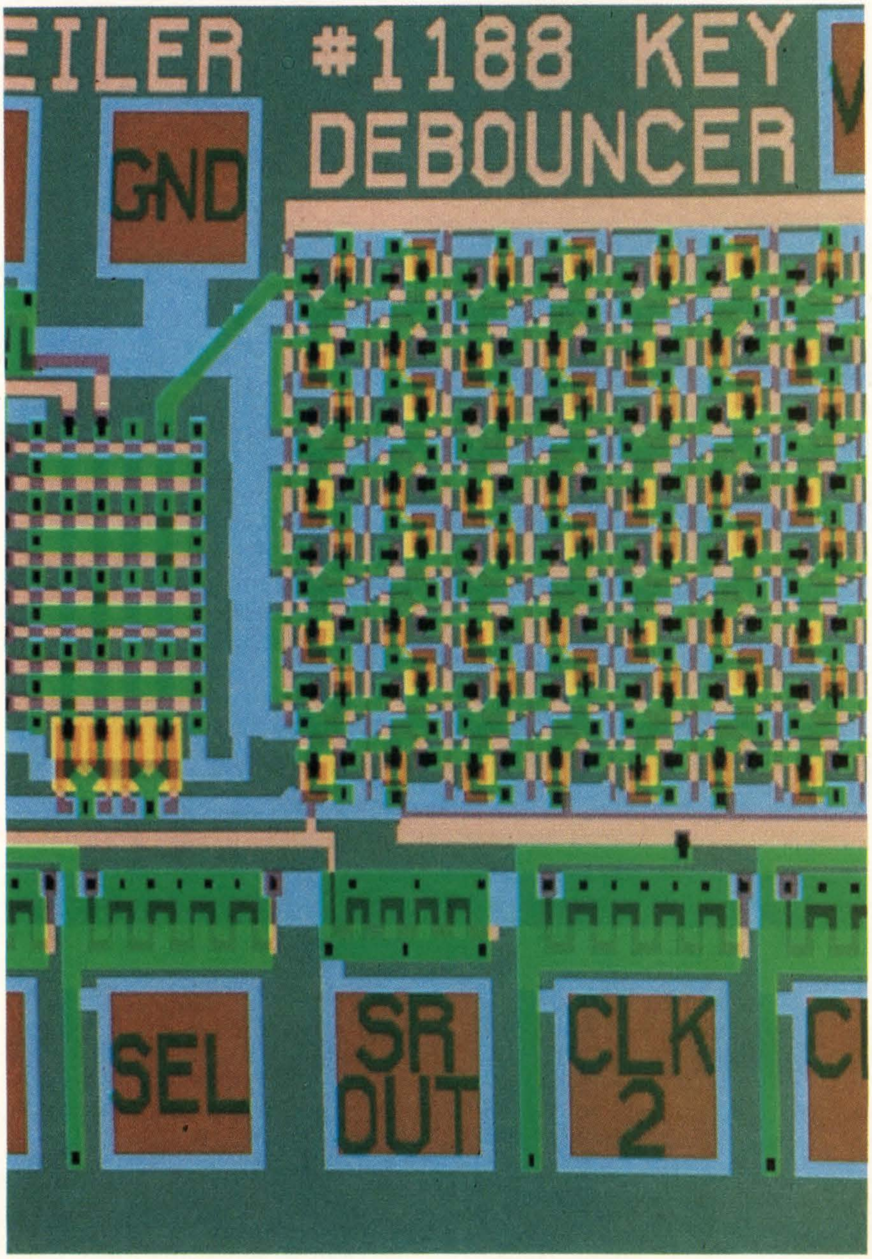

Figure 4: Printed circuit/integrated circuit design is becoming one of the most competitive markets for CAD. Photo courtesy Jupiter Systems, by Alan Paeth.

PrintaColor's new TC1040 is the perfect printer for your color graphics system. Hardcopy can be generated by virtually any computer or color display terminal—faster and easier than ever.

Color fast and picture perfect
The TC1040 was designed with full image-seeking and bidirectional capabilities that allow it to produce an 8½" × 11" image in one and a half minutes.

With resolution of up to 120 dots per inch, your images are printed crisply and clearly every time on a variety of media from 8½" to 14 7/8" wide.

4,913 choices of color
TC1040 ink-jet technology produces sharp text and precise graphics in just about any color you can imagine via PrintaColor's versatile method of ordered dithering.

Quiet and simple
Non-impact, whisper-quiet operation makes the TC1040 ideal in any office setting. Snap-in, disposable cartridges contain specially formulated inks that dry instantly on plain paper.

Built for long life
The TC1040 has a performance rating of over 3,900 hours MTBF. The drop-on-demand printhead has a proven reliability of more than 10 billion operations. Modular design simplifies routine maintenance checks and minor adjustments.

And the TC1040 has all applicable regulatory agency approvals.

The Logical Choice
For greater speed, more colors and higher quality resolution in a color printer, look to PrintaColor's TC1040—the new color hardcopy solution—for text, image and graphics.

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types and levels of this interaction. Gerber's prompt support demonstrates the improved use of this technique, in which an LED display queries the user (at selectable levels of system competency) about subsequent actions.

Software is also vital as the medium for program development. Raster Technologies, for example, does not sell applications packages. Instead it has written strong software development tools for programmers including "macro programming" functions and software debuggers.

Most suppliers are striving to provide basic packages for mechanical, electronic, AEC and other applications. This requires vendors to retain application engineers in each area of specialization. The difficulty for manufacturers is in recognizing what level of tools they should provide to users: they cannot, after all, afford to know more than the user and still remain cost effective.

Software Standards

One of the most contentious issues in graphics during the past five years has been the development of standards to lessen device interface problems and increase the usefulness of software libraries. The focus has been on US technical groups' development of the SIGGRAPH CORE standard and the European developed (and US modified) GKS standard. Before the development of either of these standards there were several de facto standards such as Tektronix Plot 10 Software, the ability to emulate the widely used series of Tektronix storage tubes, and the use of Calcomp-developed output device interface software.

As the number of graphics systems producers and applications have increased, the demand for more comprehensive standards has also grown. The National Bureau of Standards, ANSI and SIGGRAPH have all promoted discussion and development of such standards and promulgated the CORE standard for several years in hopes of giving users more flexibility and enhanced capabilities. The GKS standard, however, has become more widely respected and most vendors now indicate that they will support GKS in their next announcements. Many of these same vendors are, however, quick to note that GKS is only a partial solution, with shortcomings in resolution and 3D display. Genisco and Spectragraphics have developed packages with GKS routines that also allow for high resolution color and 3D displays. The key appears to be in using GKS as a redefinable kernel of functions.

The most important software standard for CAD/CAM vendors is the IGES, promoted and developed primarily by the National Bureau of Standards. In CAD, the transferability of files between work stations and between locations is of great importance because of the complexity of many designs and because of the distributed nature of the manufacturing process. Government and military play an important role as well, requiring contractors to make files available between designers and approval agencies.

Another growing trend is vendors' acceptance and encouragement of third party developed software. The software needed to exploit new applications requires more resources for development than many manufacturers can afford. One solution is to target specific areas for development. In Architectural, Engineering, and Construction (AEC), for instance, Intergraph, Calcomp, McAuto and Auto-Trol have developed specialized expertise.

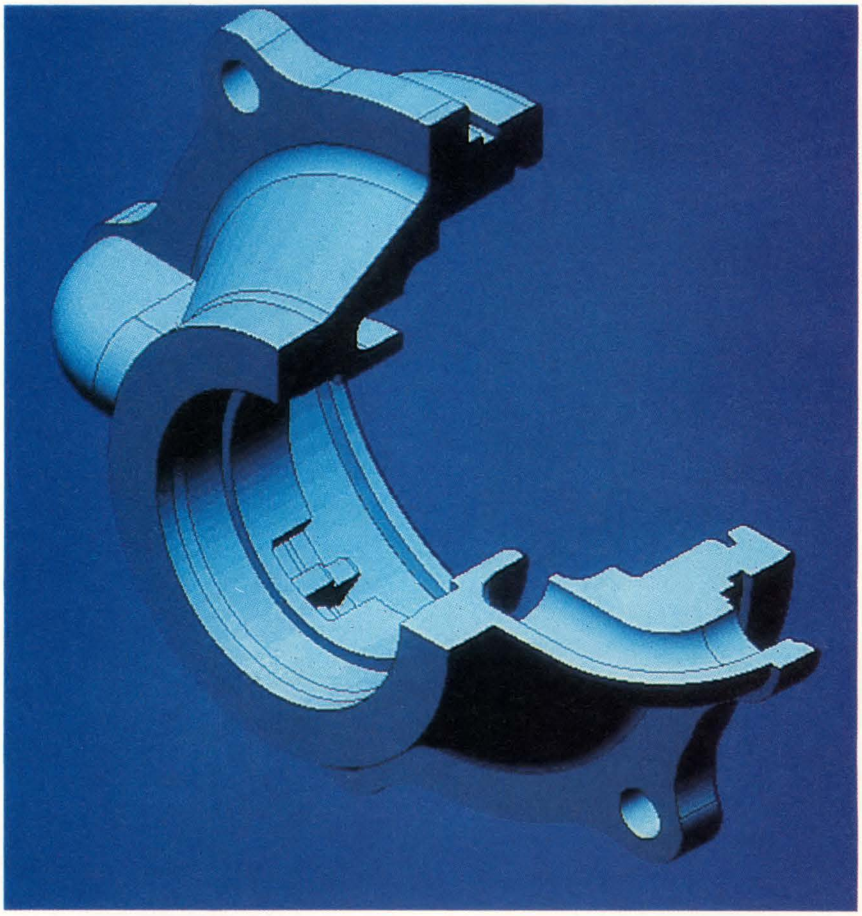


Figure 5: A mechanical part created on Applicon's solid modeling system has been sectioned to provide the designer with an interior view of the object.

Figure 6: Gerber Systems Technology's PC board design.

As software development costs are increasing, hardware costs are on the decline. To justify continuing high profit margins, vendors must increase the value they add through software. One area of software development not often discussed is the use of data base management systems. Several announcements at this summer's trade shows focus on DBMS packages. Calma is annoucing its DMCS to allow multiple access to design models, and Gerber's Shared Resources Manager will offer shared access to files, tapes, plotters, and NC tape devices.

Solid Modeling

Almost without exception, the vendors of CAD/CAM are working to develop solid modeling (SM) systems or software. Potential purchasers are using the presence or absence of SM packages as an indicator of the future growth of a manufacturer. There remain several problems with both approaches to SM software, *boundary representation* and *constructive solid geometry* (CSG): lack of direct application to drafting functions, lack of non-keyboard interaction, the need for 32-bit based systems, the need to retrain designers, difficulties in the generation of irregular surfaces, and problems in exchanging file data from CSG to boundary files. On the positive side, solids are valuable in the near term for design concept communication. In addition, SM packages are at the heart of integration for CAD/CAM/ and CAE. The resulting complexity of implementation ensures that their successful use for turnkey graphics will be slow in coming.

The support of SM displays requires the accumulation of data that enables the display to store and manipulate a data base that is a geometrically accurate representation of a solid object; ideally one is able to distinguish a point adjacent to, within, or external to a plane. SM packages also ideally contain information about the moments of inertia, density, and other physical characteristics of an object in driving manufacturing devices for CAM.

One comment from industry is that SM will become more practical when software programmers learn to make packages available for users' formats (mechanical or architectural) rather than expecting users to adapt the packages. Hewlett-Packard's 32-bit desktop minicomputer holds promise for SM by making these available to single users. As an intermediate step, Calcomp and Intergraph have introduced packages that provide capabilities similar to SM, including surface shading and physical data such as volumetric information.

It remains to be seen whether SM will allow the integration of 2D, 3D and CAE applications. While SM is a powerful software enhancement, it lacks the direct interaction with finite element modeling (such as Patran), Finite Element Analysis (Ansys or Patran) and numeric control software (APT for multiaxis milling and Compact II for lathe milling). At present, several systems will support operations of individual packages like these, but interoperability from a single program requires more development. SM must also adopt many of the efficiencies of 2D packages such as multiple windowing, multiple menu overlay, and dimensioning.

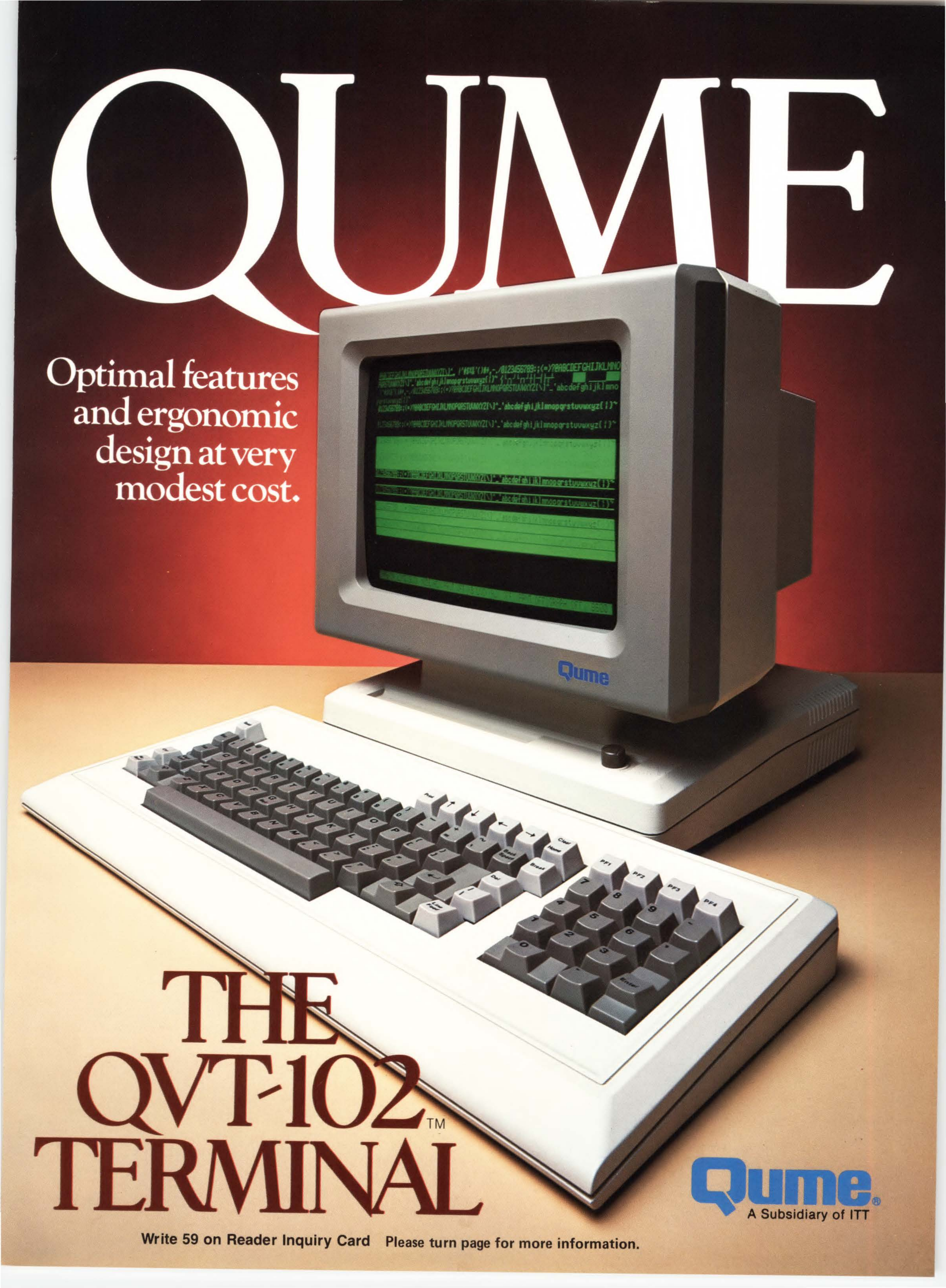
System Design

Price Performance And Specialized Niches. One of the most evident factors shaping the design of systems is the decreasing cost of hardware. Lower costs for specialized chip memory and display tubes causes the system integrator to target audiences where it will be best received. Another trend is for manufacturers to increase capability (such as the processing time required for rendering or manipulating displays) while lowering price. The best recent example is the Advanced Electronic Design (AED) "512" product which was lowered in price from $17K to $7K. Cost/performance competition is also reflected by major integrators using the hardware of smaller firms: McAuto/Megatek, Autotrol/Apollo, Data General/Raster Technologies.

Purchasers no longer consider merely price tags in acquisitions, but the ability to enhance the system over time. This could be either hardware improvements or the ability of the system to become an integral part of an existing computer environment such as IBM or DEC. Spectragraphics, the first of the manufacturers to specifically target the color terminal market for IBM (and recently DEC) provides a more cost effective entry to design than IBM itself. The Spectragraphics terminal draws the display a tenth of a second faster than IBM's own terminal. This can be important in evaluating long term effectiveness, because in the CADAM software package there is a feature that allows the number of user interactions with a system to be tallied. Slow update and redraw becomes immediately evident, considering a range of interaction rates is 12 to 60 per minute.

Another type of flexibility is advocated in the provision of system interfaces for peripheral devices that allow users to acquire new processors or peripherals without replacing an entire system. CalComp favors a standard interface such as the Multibus, providing the user with a variety of disk storage devices that can be attached.

Networking And Communications. All of the CAD system providers are of the need for communications between workstations or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QVT-102
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Qume's new QVT 102™ CRT terminal has all the features of the Hazeltine 1500, Lear Siegler ADM 3A/5, and Televideo 910, and emulates any of these terminals by simple menu selection. Features found in higher-priced terminals are standard, including block and conversational modes, local editing, 25th status line, menu set-up mode, and screen content printing.

The QVT 102 takes up minimal workspace and is designed to please the operator. Its non-glare green or amber screen minimizes eye strain with a big 9 x 12 character cell. The screen tilts and swivels for perfect viewing, and the low-profile keyboard is detached to allow placement for ideal reach and hand-rest position.

Sophistication. Comfort. And affordable price. Qume's Model 102 terminal is easily the smartest choice in its class. Features include:
• Line block, Page block, and Unprotected block transfer modes • Four separate function keys (twelve functions) • Line drawing graphics characters • Tilt/swivel, non-glare, green screen (amber optional) • 9 x 12 character cell resolution, 7 x 9 character size • Detachable, low-profile typewriter style keyboard with numeric pad • 24 lines x 80 characters with a 25th status/menu set-up line • Screen-saver time out (an inactive terminal shuts off its screen after fifteen minutes with no screen data loss) • 5 video attributes: blink, blank, reverse video, underline, and half-intensity • 3 emulations: Hazeltine 1500, Lear Siegler ADM 3A/5, and Televideo 910 • Self test • Switching power supply (efficient operation and low power consumption)

Display Format
24 lines x 80 Characters
25th status/set-up line (defeatable)

Character Formation
7 x 9 matrix in a 9 x 12 cell

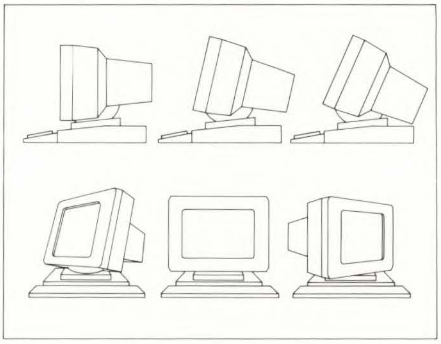
Displayed Character Set
96 ASCII characters, 15 line-drawing symbols, and 32 control character symbols

Editing
Cursor: up, down, left, right, and home. Character/line insert and delete, erase to end of line/field/page, tab, back tab, field tab, field back tab

Communications Interface
EIA RS232-C, 20 mA current loop

Communication Protocols
DRT and/or X-ON/X-OFF

Communication Modes
Full or half duplex, block/line, block/page; 7 or 8 data bits



Baud Rates
15 selections from 50 to 19.2k

Auxiliary Port
Unidirectional EIA RS232-C, partial/full screen copy, transparent

Screen
Tilt/swivel 12-inch diagonal standard non-glare green (optional non-glare amber)

Character Attributes
Blink, blank, underline, reverse video, half intensity

Keyboard
Detachable, low-profile (home row 30mm from work surface), alphanumeric keys, 14-key numeric pad, 4 function keys (12 functions), defeatable auto-repeat and key click. Print, setup, and no scroll keys.

Fields
Protected and Unprotected fields

Parity
Odd, even, mark, space

Screen-saver
Screen shut off after 15 minutes of inactivity with no data loss (defeatable)

Emulations
Hazeltine 1500, Lear Siegler ADM-3A/5, Televideo 910

Set-Up Mode
Menu style, preserved in non-volatile memory

Power Requirements
95-125 VAC
200-264 VAC
50/60 Hz, 30W

Dimensions
Keyboard 1.5″(H) X 18″(W) X 8″(D)
Display 14″(H) X 13″(W) X 12″(D)

Weight
Display 19 lbs. 2 oz., Keyboard 3 lbs.

Options
Amber phosphor screen
14-inch screen
Foreign character sets
20 mA current loop (passive and active)

Command Codes

Cursor home	Ctrl/ ^
Cursor right	Ctrl/L
Cursor left	Ctrl/H
Cursor up	Ctrl/K
Cursor down	Ctrl/J
Clear screen	Ctrl/Z
Clear from cursor to end of line	Esc T
Clear from cursor to end of screen (background)	Esc ,
Clear all foreground	Esc ;
Line insert	Esc E
Line delete	Esc R
Keyboard lock	Esc #
Keyboard unlock	Esc "
Bell ring	Ctrl/G
Tab	Ctrl/I
Address cursor (row/column)	Esc=(nn)
Read cursor (row/column)	Esc?(nn)
25th line display	Esc }
25th line suppress	Esc {
Monitor mode on	Esc U
Monitor mode off	Esc X or Esc u
Print transparent on	Ctrl/R
Print transparent off	Ctrl/T
Write protect on (half intensity)	Esc)
Write protect off (full intensity)	Esc (
Graphic mode on	Esc $
Graphic mode off	Esc %
Auxiliary port off	Esc @
Auxiliary port on	Esc A
New line	Ctrl/_
Back tab	Esc I
Clear screen to nulls	Esc *
Display control character equivalent	Esc F n
Load cursor line	Esc [n
Load cursor column	Esc] n
Print entire screen	Esc P
Print from top to cursor	Esc N
Print from cursor to end	Esc O
Tab set	Esc 1
Tab clear	Esc 2
Tab all clear	Esc 3
Autoscroll on/off	Esc H
Self test	Esc V
Protect mode on	Esc &
Protect mode off	Esc '
Send line unprotected only	Esc 4
Send page unprotected only	Esc 5
Send line all	Esc 6
Send page all	Esc 7
Clear unprotected to nulls	Esc :
Block/page on	Esc B
Conversational mode on	Esc C
Block/line on	Esc D
Character insert	Esc Q
Character delete	Esc W
Termination character select	Esc x N

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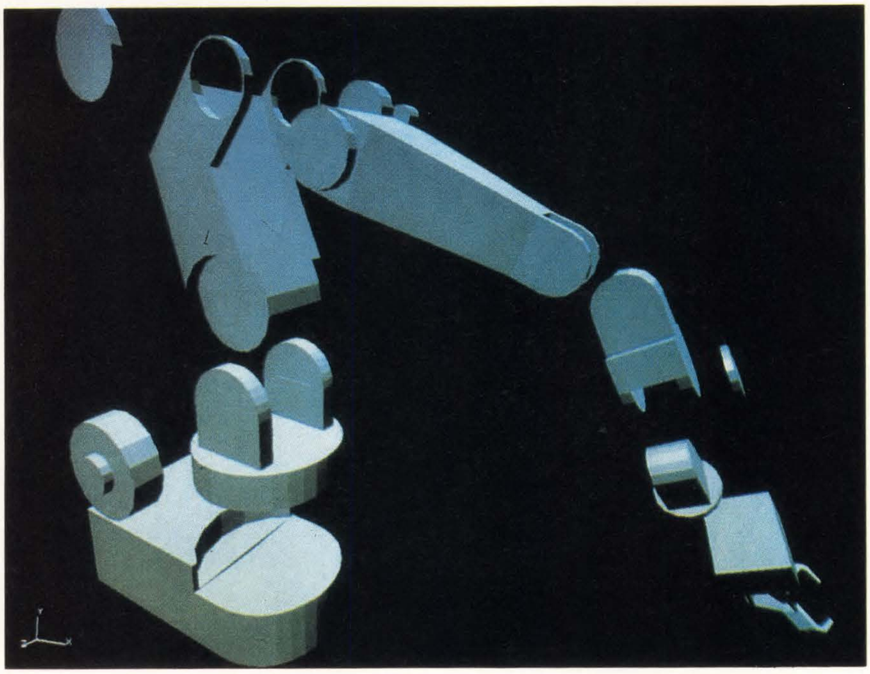

Figure 7: A robot device is assembled using geometric primitives.

Figure 8: In a combination of design and engineering processes, color is applied to a model to provide the designer with information about stress. Photos courtesy GE/CAE International.

between terminals. The Ethernet (modified by the IEEE as its 608 proposal) and Ungermann-Bass are the most frequently mentioned configurations; others include proprietary networks (Domain, Calmanet and DECNET). Because the IBM communication market for graphics is not well developed by secondary suppliers, there is only an indication that SDLC or Bisynchronous environments will be important. Some vendors think this is potentially the largest market.

Terminals Versus Standalone Workstations. Increasing intelligence has blurred the definition of terminal and workstation, but the key concept remains that systems must not be merely programmable for graphics, but capable of supporting software for CAD/CAM/CAE applications. Even when this becomes practical, however, data intensive applications will require much offline storage.

There is a market for both terminal and workstation systems, but μP and memory advances are improving the amount of direct interaction between the designer and the system. Users maintain that, at present, standalone systems cannot offer the doublepoint precision needed in mechanical design (with the exception of systems such as Apollo for which terminal cost can be high). The key lies in the amount of power required for tasks assigned to the designer, who values the ability to operate a system in an autonomous fashion. Terminal systems offer advantages where input of graphical information is relatively simple and not tied to intensive interactive processing demands in which multiple users can cause device response to degrade noticeably.

Other considerations for workstation design include display, I/O and physical size. Dual monitor systems with concurrent display of software functions and design work (in some cases multiple views of the design) have become very popular. Increasing intelligence, on the other hand, allows the physical size to decrease so that the design station may actually become a desktop device. Similarly, color is made more practical by advances in color look up tables, lowered costs of semiconductor memory for color planes, and software techniques such as dithering to simulate a broader range of display capability.

The Marketplace

All of the efforts in system design are influenced in part by the demand from the marketplace, although many consider CAD to be driven by technology and not demand. Whatever the impetus, there are several trends in the sale of systems.

Pricing. Until recently the competitive price was approximately $120K per terminal; prices for newer standalone and terminal systems is moving towards the $60K area. However we are still in the arena of $100K systems and this figure remains important for two reasons. First, this approximates the amount of capital spent for laboratory devices of an engineer and may make system acquisition more acceptable. Secondly, $100K if amortized over five years is about what would be paid for a technician or starting engineer. The most important price barrier, however, for many manufacturers is $35K to $40K because it is at that level that a mass terminal market is practical.

Shifts In Marketing. CAD was well known for almost two decades as the proving ground of mechanical design in aerospace and

automotive engineering. In the 1970s, a strong demand for electronic design supported the growth of several of today's larger firms, including Computervision, Applicon, Calma. At present many of the long-standing firms are re-emphasizing their markets. Applicon, for example, is making an effort in mechanical design to match increasing sales there. Calma, whose primary market is PC/IC, is now attempting to exploit AEC markets.

Several manufacturers consider the AEC market the fastest growing segment of CAD, although not the largest in terms of sales. AEC designs, however, are distinct from other areas: they are very dense (graphics, text, dimensions, and multiple layers); they address a very broad range of applications (space visualizations, thermal efficiency, life cycle, aesthetics, and use projections); and users are not as acquainted with computers as their counterparts in mechanical or electronic design. The latter expresses itself as less concern with the power of the CPU and more with ease of use. The marketplace is also segmented differently. Of over 22,000 architectural firms, only 150 have over 500 employees, but over 15,000 have less than 10. The market is also more volatile than others; implementation by several important firms such as Fluor or Bechtel could cause industrywide demand.

While the growing demand for SM packages is due to increased use of mechanical design, there is a commensurate increase in growth for electronic design. Several new firms have targeted electronics, Avera, Daisy, Metheus, Valid and VIA among them. These smaller firms are bringing heightened competition to marketplace niches. VIA is the epitome because it is offering not only PC/IC layout artwork, but logic simulation and interface to NC programs (the latter for production of photomasks). A firm as large as Calma may be unable to move as quickly to develop new software packages; in large companies, policy may inhibit marketing. Several of the larger firms point out that it is easier to develop graphics for PC/IC design because the displays represent relatively insignificant computational tasks. Start-up firms' venture capital support may require marketing within a time period insufficient to develop an original mechanical package. There are also several electronics packages in the public domain available for modification by entrepreneurs.

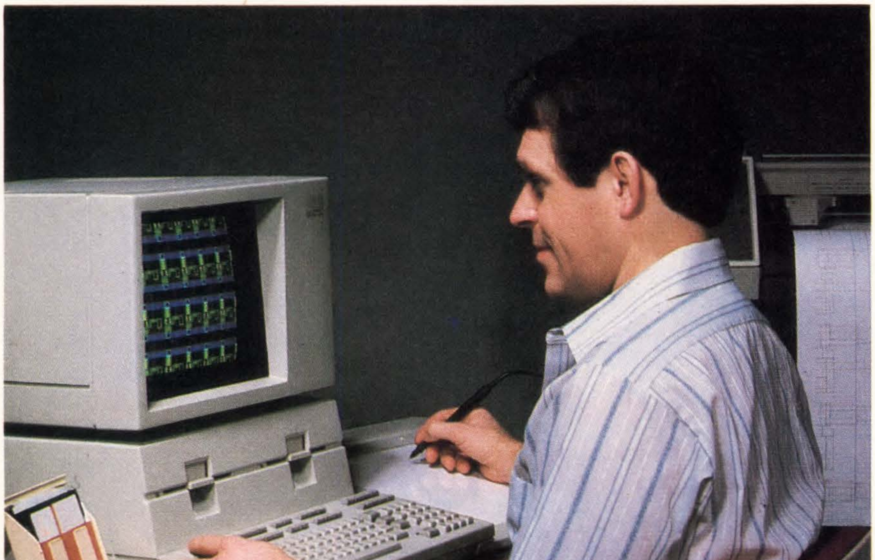
Figure 9: The HP-9000, a 32-bit engineering workstation, signifies a trend in personal desktop engineering workstations. Photo courtesy Hewlett-Packard.

A more subtle shift in the marketplace for CAD systems is due to the increasing use of microelectronics in mechanical subsystems. This shift may disguise new areas of growth for CAD, such as the design of digital to analog converters on gate arrays or the next generation of standard cell designs. At some point the markets begin to overlap.

OEM Integrators Versus Unique System Manufacturers. One of the most spectacular areas of growth for graphics systems in CAD has been among the developers of discrete components for graphics systems such as Lexidata, Raster Technologies, Genisco, Spectragraphics, Superset, and Apollo. Their systems have become key components in the products of others. Several of these vendors have experienced the problems of one producer becoming an important segment of their market. Nevertheless, the trend is away from the Computervision and CalComp approach of developing all of the needed technology. The pace of change in graphics is so fast that no manufacturer can hope to be all things to all markets—integrator, manufacturer, software developer, and service organization.

IBM's recent success in the personal computer market should indicate that there is to be another influence on the graphics market for CAD in the near future. Spectragraphics, Adage, and CGX all have developed products in anticipation of the IBM announcement for color—despite the lack of specifications for the 3250 line of products. DEC-compatible products may likewise be expected to have an effect, if smaller, upon the market.

Shifts In Ownership. Larger manufacturing concerns have recently paid significant interest to graphics system producers, partly to improve business efficiency

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If you have been waiting to view your solid models, your waiting days (or even minutes) are over. Now there's SOLIDVIEW.™ A revolutionary, new display technology for viewing solid models that significantly increases system speed. And significantly decreases host overhead, software development time, and total system cost.

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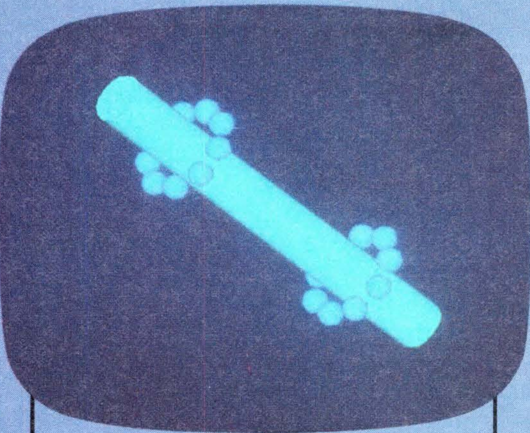

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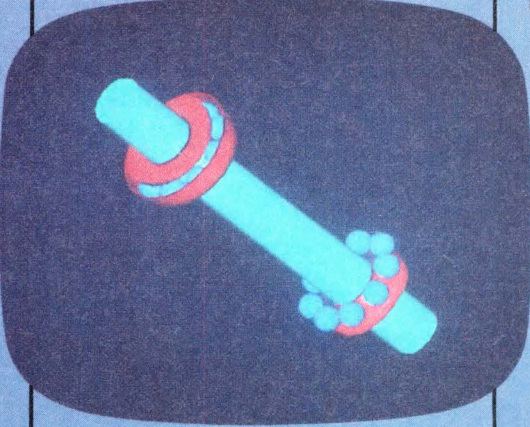

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through vertical integration. The General Electric acquisition of Calma, CAE, and SDRC; Sanders' acquisition of CalComp, & Talos by CalComp; Schlumberger's purchase of Applicon and MDSI, Evans and Sutherland's acquisition of Shape Data Ltd.—there are examples on all levels within different types of industry. Some manufacturers seek advanced technology to benefit other operating divisions from graphics vendors seeking to enhance their market position. It is not clear, however, that the acquisition of high technology firms will foster the continued growth of the acquired firms.

One of the most successful partnerships, likely to become more active in the near future, is that of Gerber and Hewlett-Packard. The H-P developed 9000 workstation has the potential to dramatically affect the market for, and development of, graphics workstations.

Other Factors. Though military and aerospace markets were early forces shaping the development of graphics systems, they seem less important today (although they play a disproportionate role in terms of dollar sales). The commercial demands for mechanical, electronics and AEC uses, or in graphics applications at large, such as animation or simulation, are proving to be much more demanding of high resolution, color, interactivity, and displays. CAD itself is one of the proving grounds for system integrators seeking to combine software capabilities of design and analysis into comprehensive packages.

Japanese systems developers are beginning to compete for American markets, but as in computing in general, they lack marketing or software to compete effectively on all fronts. Japanese manufacturers do, however, have the potential to affect commodities markets within graphics: digitizers, CRTs, plotters, and other areas where a low entry price buys a part of the market share allows them to compete effectively and eventually to raise prices. The Japanese contribution would appear to be the best in the area of thermal, ink jet, and electrostatic hardcopy systems.

CAD's Future

Not only is the technology of CAD changing, but so too is the customer base. Hardware advances are being pushed by display processing, software and OEM integrators. Techniques such as gate array for custom graphics products may shape systems, but probably not for the next two years. The advances incipient in software are indicated by efforts such as Applicon's to integrate surface modeling, finite element modeling and analysis and solid modeling under its

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GRAFEM and IFAD products. CAD system developers are also moving to incorporate the color capabilities of image processing with the interactivity of graphics.

On the market side, there is the potential in the near future to develop a new market entirely by lowering the cost of systems and making productivity even more attractive through CAD use. Hewlett-Packard points out that the key is engineering a workstation dedicated to the single engineer or designer. Another factor is the growing sophistication in users' appreciation for what a CAD system should be able to do. Where shading, sectioning, and hidden line removal were primary issues several years ago, purchasers are now able to address questions such as the ability to examine mass properties. There is increasing competition across all markets. Vendors are still subject to tremendous pressure from their purchasers—pressures that push announcements before they might otherwise be made or before products are fully evaluated. The continued strength of the dollar abroad has caused sales internationally to decline, but it may also prevent internal foreign competition. It would appear that the critical price range of $40K may be practical within the next two to three years, which will bring about another cycle of renewed interest in CAD, and much wider application. □

Producers Of CAD Systems

To obtain more information on the following CAD system companies, write in the appropriate Write Number on the *Digital Design* reader inquiry card.

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Advanced Color Technology
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AED Inc.
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Apollo Computer Inc.
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Applicon
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Write 304

Arrigoni Computer Graphics Inc.
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Write 305

Autotrol Technology Corp.
Denver, CO
Write 306

Avera Corp.
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Write 307

Aydin Controls
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Write 308

CADAM
Burbank, CA
Write 309

Cadlinc
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Cadmatics
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Write 311

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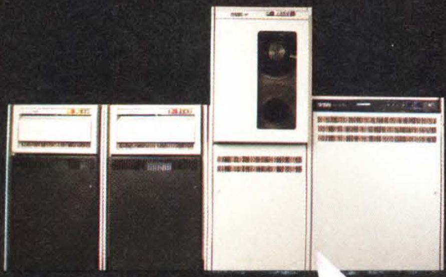
2D/3D INTERACTIVE COLOR TERMINAL

MATROX GXT-1000



THE NEW MATROX GXT-1000 color graphics terminal delivers true 2D/3D interactive performance. It's fast. It's intelligent. It's high resolution. And it costs less than $10,000 in OEM quantities. Complete.

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- up to 1280 x 1024
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- interlaced or non-interlaced

HIGH SPEED
- 80286 graphics engine
- 6 pipelined slave processors
- up to 20,000 short vectors/sec
- up to 5000 filled rectangles/sec

HIGH PERFORMANCE
- 64K x 64K x 64K virtual addressing
- local picture storage up to 22 Mbytes on disk
- local segment storage up to 1 Mbyte (2000 segments) in RAM
- full 2D transformations standard
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- real time pan in 64K x 64K virtual space

LOCAL I/O SUPPORT
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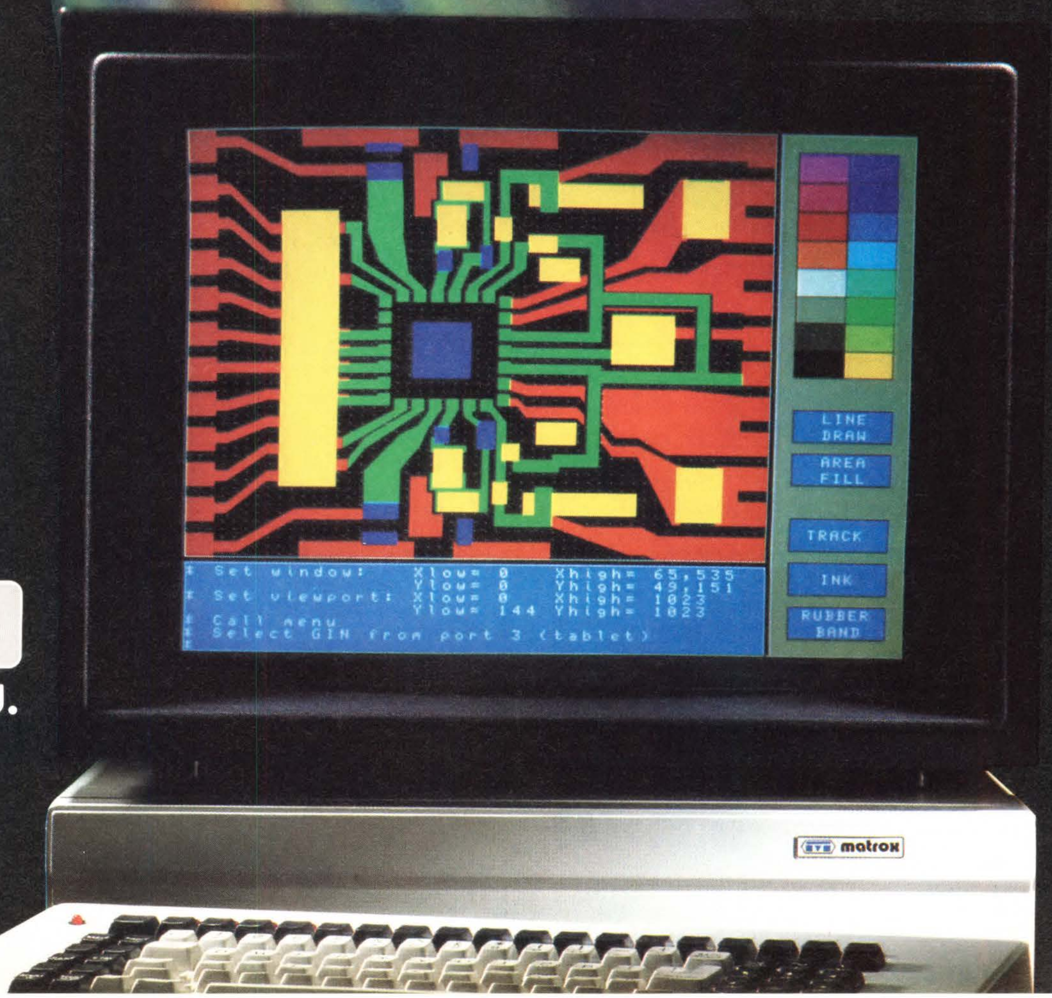
- add-on Winchester/floppy disks

OEM OPTIONS
- desktop or rackmount electronics
- available unbundled as Multibus board set
- VAX host software package

Multibus, 80286 - TM INTEL VAX - TM DEC



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electronic systems ltd.

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Calma
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Computervision
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Write 317

Control Data Corp.
Minneapolis, MN
Write 318

Data General
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Design Aids
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Digital Equipment Corp.
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Evans and Sutherland
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Florida Computer Graphics
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Futurenet
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Genisco Computer Corp.
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Gerber Systems Technology Inc.
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Houston Instrument
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Information Display Terminals
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Intelligent Systems Corp.
Norcross, GA
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Intergraph Corp.
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Lexidata Corp.
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Lundy Electronics and Systems
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MAGI
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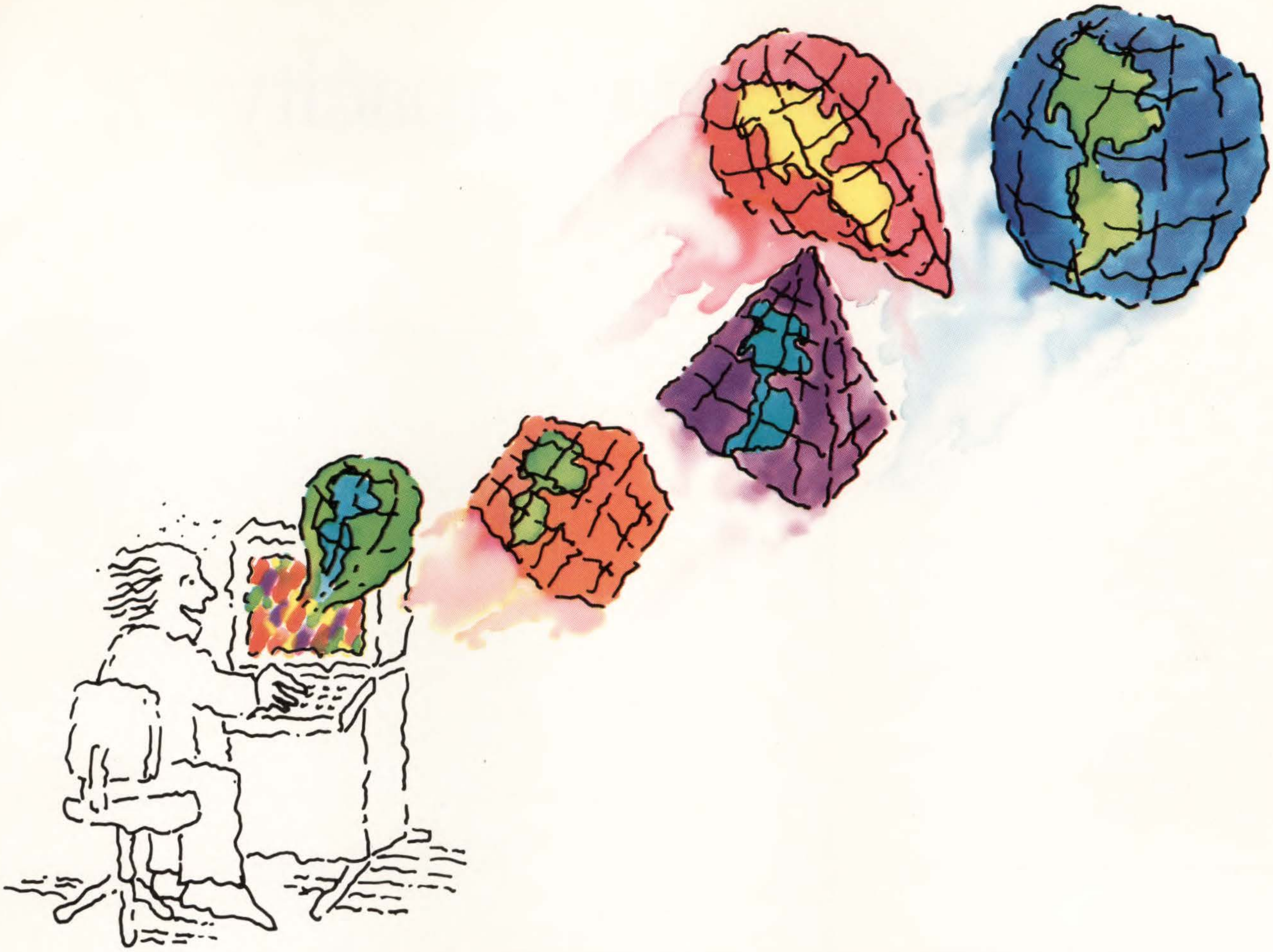

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D-SCAN
Seiko Instruments U.S.A., Inc.

ESDI Boosts Drive Capacity

by Doug Eidsmore
West Coast Technical Editor

A newly proposed 5¼″ Winchester interface standard could allow manufacturers to take full advantage of state of the art recording technologies. Present 5¼″ Winchesters are designed to meet the current ST506/412 interface standard. The new Enhanced Small Disk Interface (ESDI) doubles the transfer rate of the ST506/412 and allows 10 Mbits/sec to be sent between the disk and controller. Getting data on and off faster will allow more data to be stored on a disk. Higher recording densities and advanced coding schemes that increase overall capacities can be implemented.

5¼″ Winchesters could soon talk to controllers at 10 Mbits/sec, but some manufacturers feel standardization is premature.

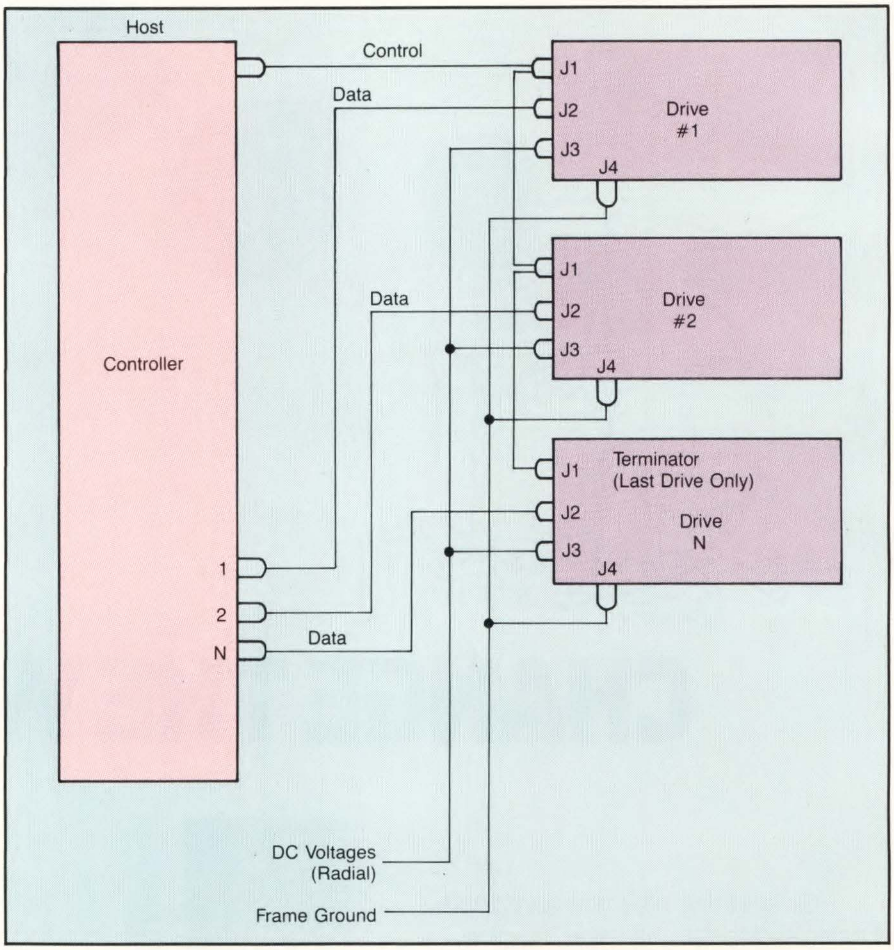

Figure 1: Typical multiple drive ESDI connection. In STEP mode the maximum number of drives is 3 and in SERIAL mode the maximum is 7.

In the long run, raising the transfer rate may prove to be the least costly way of increasing capacity. The interface is currently supported by 15 disk drive and 11 controller manufacturers (**Table 1**). The degree to which they support the standard varies. Some are planning to build drives and controllers to the ESDI specification; others feel the specification is a step in the right direction but are waiting for it to evolve further. For example, there is talk of placing the entire controller on the drive in the not too distant future.

ESDI's transfer rate will allow memory to keep up with high performance μP bus rates. For example, in local area networks, users will have a stronger illusion of drawing from private memory. Also, microcomputers in UNIX environments can be less I/O constricted. In a CAD system the higher performance means data can be pulled off a disk drive rather than from inordinately large RAM. The higher transfer rate is not the only salient feature of ESDI.

The interface specifies non return to zero (NRZ) data transfer between the drive and the controller. The data separator is on the drive instead of on the controller as in ST506/412 compatible drives. This gives OEMs the freedom to choose data encoding schemes such as run-length-limited (RLLC) encoding to increase total storage capacity over the now widely used MFM encoding scheme. Maxtor (Santa Clara, CA) announced a drive designed to the ESDI specifications at NCC. The high ESDI transfer rate allows recording den-

Our 8″ Slimline disk drives are the smallest and our 5¼″ half heights are rolling out by the truck load.

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You say you need drives that are half the height but all-the-way reliable? From a source that's equally reliable? And you want a choice of configurations too?

Our response is a line of 5¼″ Slimline™ drives built with three different bezels and door styles, your choice of direct or belt drive motors, and either of two densities, 48 TPI or 96 TPI. But only one quality standard: the highest.

They come single or double-sided, with capacities from 250 Kbytes to 1 Mbyte. And for those who can do with a little less speed MPI responds with a consumer model at a lower price tag.

And when you wanted smaller, compact 8″ drives, we replied with the smallest ones there are. Our 8″ Slimline™ series. Only 2″ thick and 11.5″ deep. The selection doesn't end there. You can also get a 4.6″ bezel as well as a half size version at 2.3″.

To the cry for ever-smaller disks, MPI answered with the smallest disk drive ever. A 3″ micro floppy that interfaces with 5¼″ systems, handles 500 Kbytes of data and uses media protected by a hard shell so you can carry it in your shirt pocket safely.

That's how MPI operates. By responding with what you need. Then delivering. By the truck load from the West Coast. By the ship load from Singapore. Our own second source in the Orient that duplicates the precision production of our California plant. What's more, we are manufacturing our own heads.

That all adds up to MPI's kind of R & D. Response and Delivery. And that makes us the company to bank on.

MICRO PERIPHERALS, INC.

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Micro Peripherals, Inc., 9754 Deering Ave., Chatsworth, CA 91311. Phone (213) 709-4202. TWX (910) 494-1213.
MPI, Inc. Europe, 11A Reading Rd., Pangbourne, Berkshire, RG8 7LR England. Phone 7357-4711. Telex 848-135-MPI EURG.

sities to be increased to 14,873 flux changes per inch. By using a 2,7 RLLC encoding scheme, the Maxtor drives achieve an effective bit density of 22,310 bits per inch. Although track density stayed 980 tracks per inch, the new EXT4000 disk drives will have a storage capacity of 25.52 Mbytes/disk surface. Four models will be offered, with the 380 Mbyte (unformatted) EXT-4380 the top of the line.

Maxtor announced their ESDI compatible drive at NCC. Prototypes will be available late '83 and production should follow shortly thereafter. But they are a step away from producing it. Why? Because the high density drive electronics are not ready. High capacity drives will benefit most from ESDI, but such multiple-disk, high-end drives have the least space in which to implement such electronics as the data separator, read/write clock and address mark generation and detection. Available space may be less than 4 in^2. All this presents controller manufacturers a golden opportunity. Western Digital (Irvine, CA) and Adaptec (Milpitas, CA) should soon have data separator chips, as should the semiconductor houses. Real estate is so precious that the circuitry will probably end up in LSI custom, surface mounted devices, hybrids or maybe all three. This is not an insurmountable problem. Evotek already has an integral data separator on their drives.

Interface Features

ESDI was written with a number of optional features. The optional serial command and response capability allows absolute cylinder addressing, which reduces command transfer time. In addition, the response capability makes it possible for controllers to dynamically determine the configuration of the attached drives. Other optional serial commands enhance error recovery and diagnostics through such functions as track and data strobe offsets.

Operating systems and drivers can be designed that are generic to storage devices. The systems integrator can ask the drive about the number of cylinders, track capacity and bytes/sector, for example. Additionally, ESDI will allow multiple drive systems to do overlapped seeks, thus enhancing system-wide performance. A new head select line allows access to 16 surfaces or, in removable drives, can be used to signal the controller that a new cartridge was inserted. Address marks are not fixed.

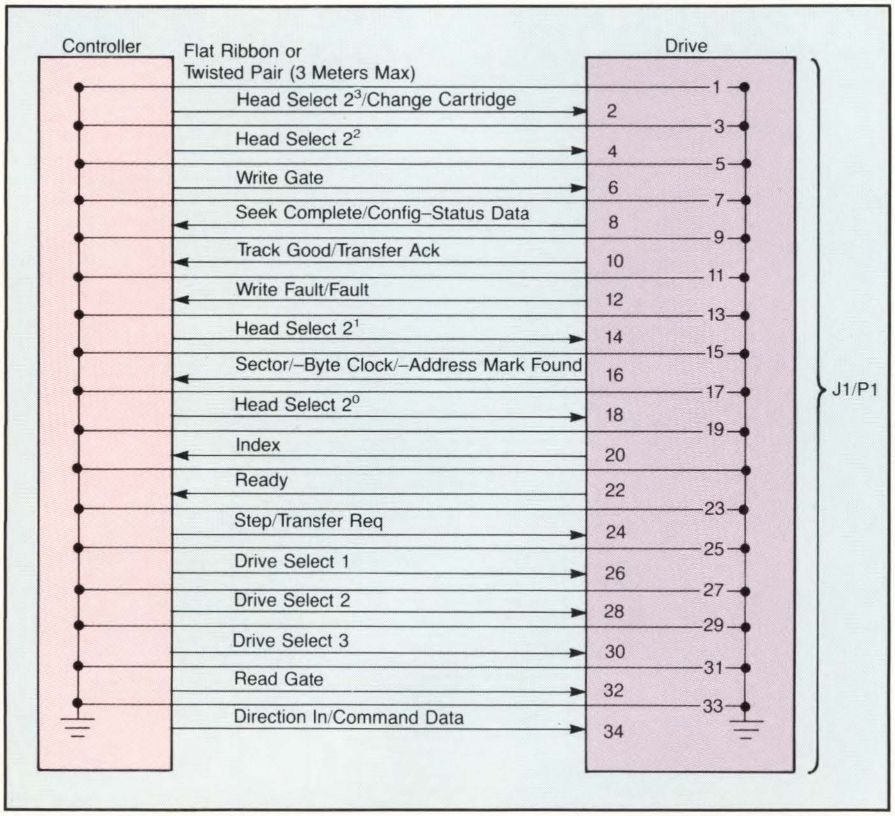

Figure 2: ESDI control signals. Provision is made for selecting up to 16 heads, cartridge changes on removable drives and flexible address marking.

ESDI Details

Two modes of operation may be used, STEP and SERIAL. ESDI does not require that both of these modes be available on any drive; it is up to the disk drive manufacturer which mode to implement. Both modes may be implemented and a selection method established if the manufacturer so desires.

The interface consists of a control cable and a data cable; both are limited in length to 3 meters. The control cable allows for daisy chaining up to three drives in STEP mode and seven drives in SERIAL mode with the last drive being terminated (**Figure 1**). The data cable must be attached radially. The ESDI can be divided into three separate categories: control signals, data signals, and DC power. All control lines are digital (open collector TTL) and either provide signals to the drive (input) or signals to the host (output). The data transfer signals provide data either to or from the drive.

There are two types of control input signals: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals (**Figure 2**) to be multiplexed are READ GATE, WRITE GATE, HEAD SELECT 2^0, HEADSELECT 2^1, HEADSELECT 2^2, HEADSELECT 2^3, STEP/TRANSFER REQ and DIRECTION IN/COMMAND DATA. The signal to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, and DRIVE SELECT 3.

DRIVE SELECT, when low, connects the drive interface to the control lines. Addressing is made by providing a connection between two appropriate points on the drive

Disk Drive and Controller Manufacturers Who Have Endorsed ESDI

For more information about disk drive and controller manufacturers, write in the appropriate Write Number on the *Digital Design* Reader Inquiry Card.

ATASI Corp.	
San Jose, CA	Write 375
Cynthia Peripheral Corp.	
Palo Alto, CA	Write 376
Disctron Inc.	
Milpitas, CA	Write 377
DMA Systems	
Goleta, CA	Write 378
Evotek	
Fremont, CA	Write 379
International Memories Inc.	
Cupertino, CA	Write 380
Iomega Corp.	
Ogden, UT	Write 381
Magnetic Peripherals Inc. (A Control Data Subsidiary)	
Oklahoma City, OK	Write 382
Maxtor	
Santa Clara, CA	Write 383
Memorex Corp.	
Santa Clara, CA	Write 384
Micropolis Corp.	
Chatsworth, CA	Write 385
MiniScribe Corp.	
Longmont, CO	Write 386
NEC Information Systems, Inc.,	
Lexington, MA	Write 387
Priam	
San Jose, CA	Write 388
Vertex Peripherals	
San Jose, CA	Write 389

CONTROLLER MANUFACTURERS

Adaptec, Inc.	
Milpitas, CA	Write 390
Advanced Micro Devices	
Sunnyvale, CA	Write 391
Data Systems Design	
San Jose, CA	Write 392
Data Technology Corp.	
Santa Clara, CA	Write 393
Emulex Corp.	
Costa Mesa, CA	Write 394
Interphase Corp.	
Dallas, TX	Write 395
National Semiconductor	
Santa Clara, CA	Write 396
OMTI	
Campbell, CA	Write 397
Scientific Micro Systems, Inc.	
Mt. View, CA	Write 398
Sysgen, Inc.	
Santa Clara, CA	Write 399
Western Digital Corp.	
Irvine, CA	Write 400

PCB (jumper, switch, etc.). This connection determines the address to which the drive will respond. In the STEP mode one drive may be selected for each DRIVE SELECT line. In the SERIAL Mode, the three lines are to be decoded for drive select. Decode 000 shall be a no select. A matrix is used to select drives 1 through 7. Decode 111 selects drive 7.

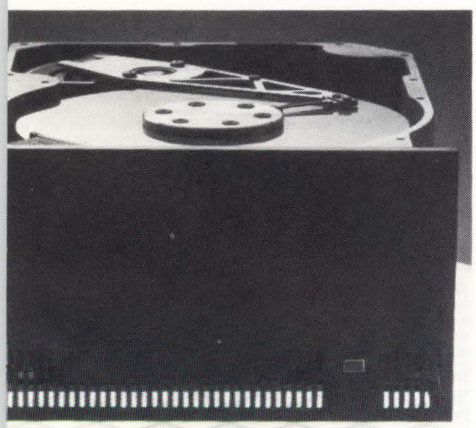

Figure 3: The EXT–4000 line of $5^1/_4$" disk drives from Maxtor stores up to 380 Mbytes and is ESDI-compatible. Prototypes should be available later this year.

The four head select lines allow selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Heads are numbered 0 through 15. When all HEAD SELECT lines are high (inactive), head 0 will be selected. Addressing more heads than contained in the drive will result in a write fault when attempting to perform a write operation. Head Select 2^3 has an alternate function for removable cartridge drives. The CHANGE CARTRIDGE line causes the cartridge to spin down to allow removal. A 220/330 Ω resistor pack allows for line termination.

The Direction In/Command Data signal has two selectable functions. In the STEP mode, the DIRECTION IN signal defines the direction of motion of the R/W heads when the STEP line is pulsed. An open circuit or high level defines the direction as "out" and if a pulse is applied to the STEP line, the R/W heads will move away from the center of the disk. If this line is a low level, the direction of motion is defined as "in" and the R/W heads will move toward the center of the disk.

ESDI is not a radical standard. In terms of complexity and intelligence it could be positioned midway between ST506/412 and SASI. It provides controller and disk manufacturers a specification from which they design and gives systems designers the freedom to use advanced recording technologies.□

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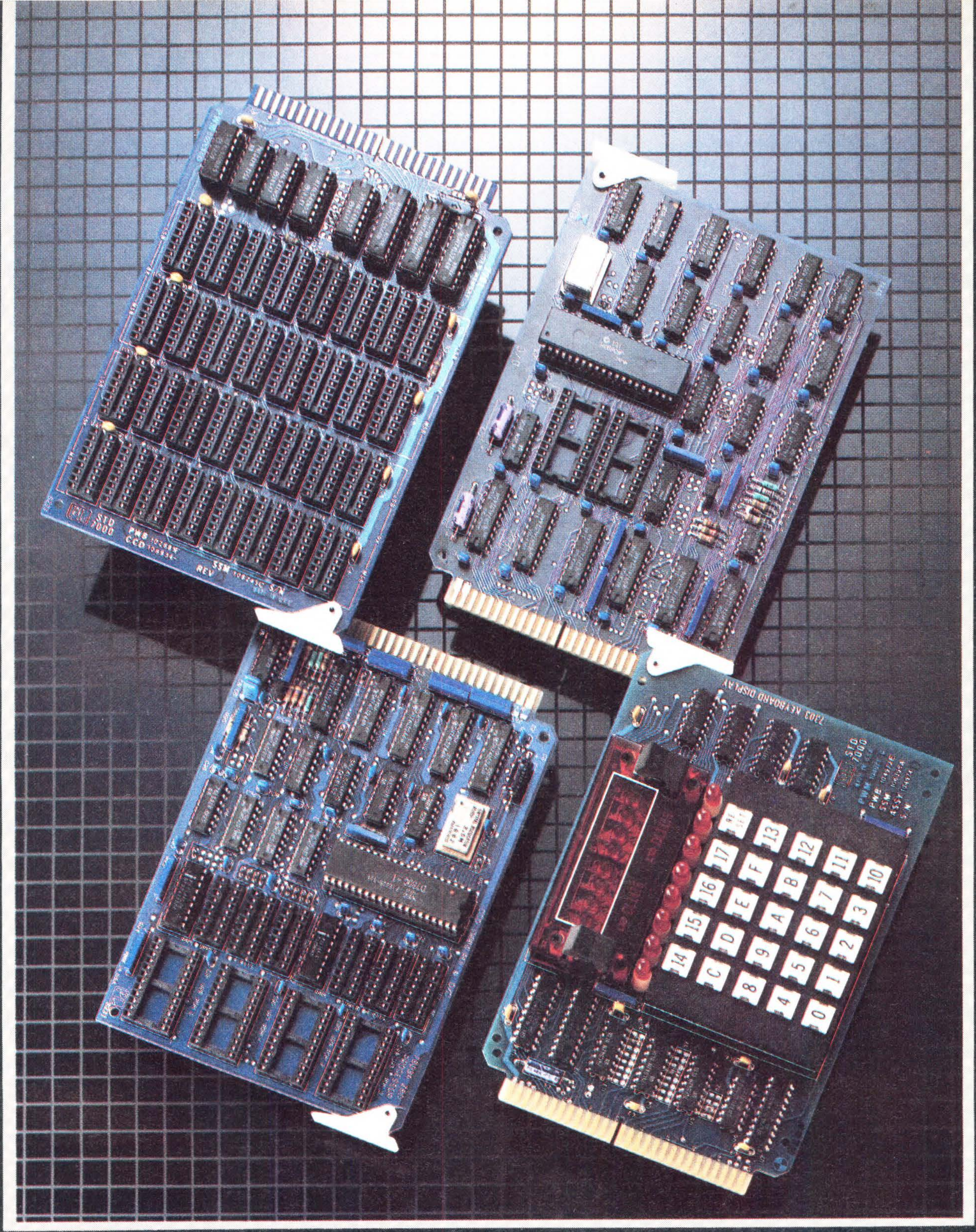

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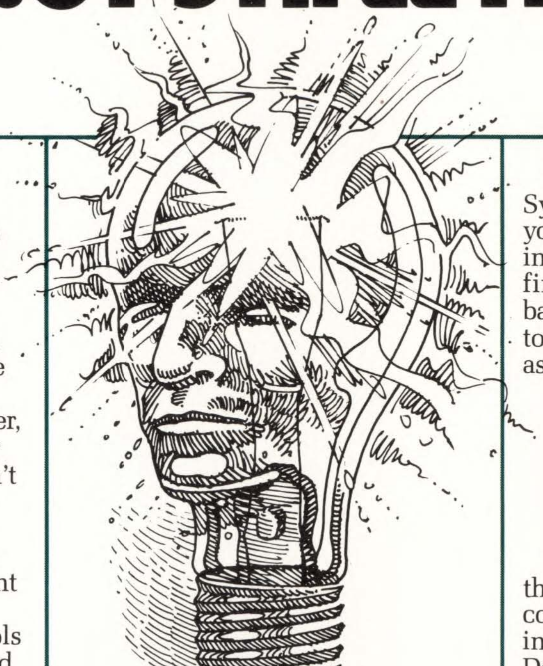

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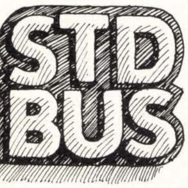

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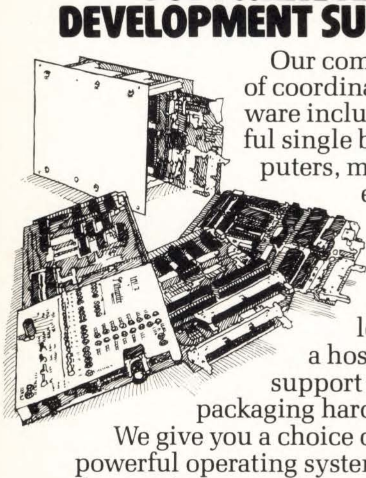

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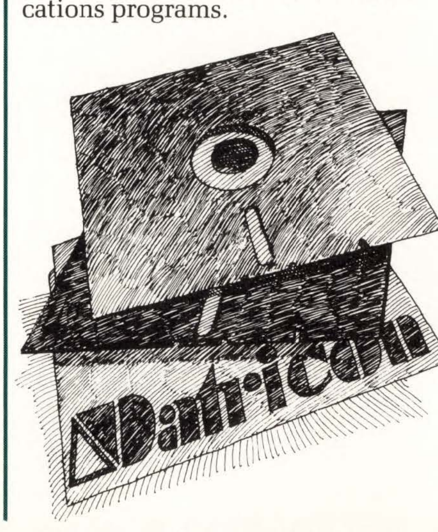

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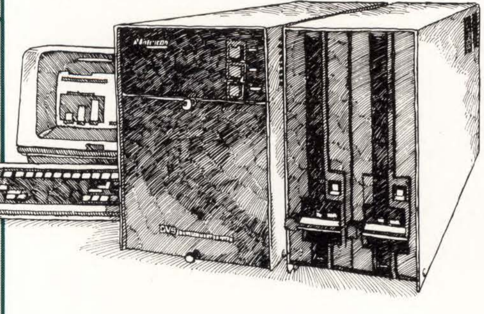

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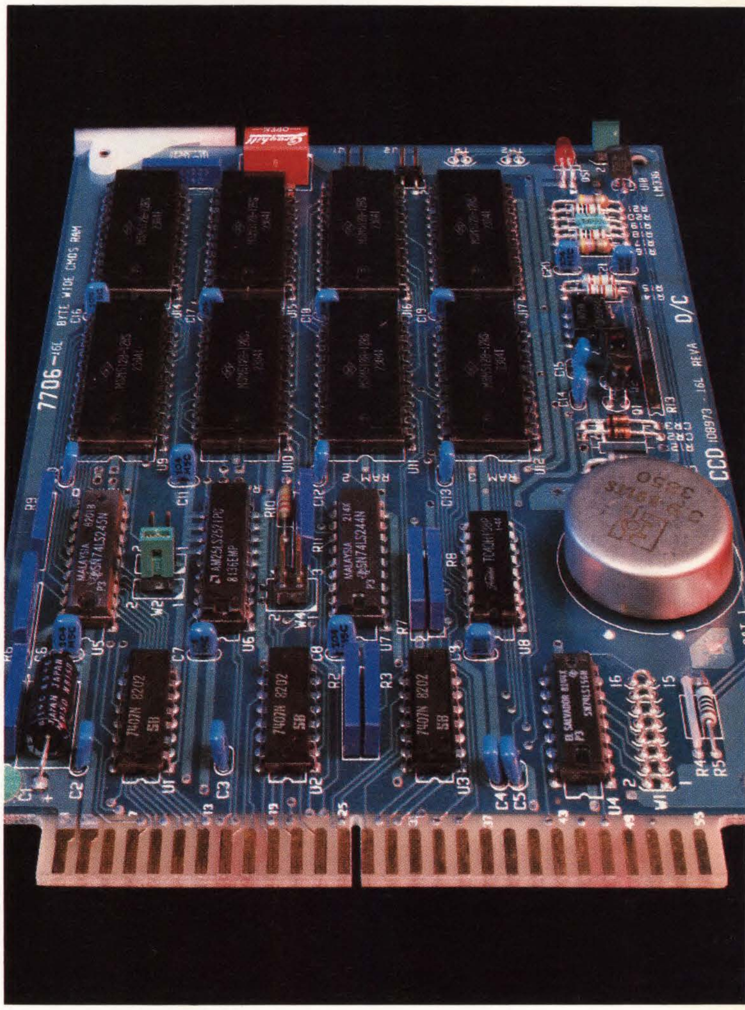
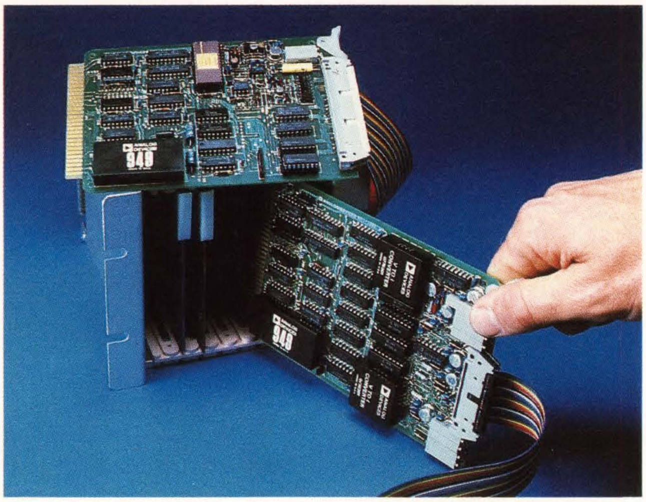
STD Bus: Meeting The Need For Distributed And Centralized Systems

Cover photo courtesy Pro-Log
Below left: Photo courtesy Analog Devices
Below: Photo courtesy Pro-Log





The STD bus has evolved from its initial support of 8-bit μPs, such as the Z80, to meet today's demand for more processing capability.

by Dave Wilson, Sr. Technical Editor

Since its introduction in 1978, over 90 manufacturers have introduced products based on the STD bus, providing the systems integrator with a wide choice of cards with which to configure his product. Pro-Log and Mostek developed the STD bus as a planned standard without the restrictions of patents, copyrights or trademarks.

Part of the success of the bus can be attributed to the fact that it was not patented, but the primary reason for its success is the modular board concept that allows users to select and pay for only needed features.

Initial board designs tended to be singular in function, partly due to board size and component density constraints. Early on, the bus catered to the price sensitive low end of the market. But with recent technological advances in μPs, RAMs, PALs, and gate arrays, more functions can be added on the same size board. William C. Cummings of Mostek feels that the trend is toward supplying the needs of the more sophisticated upper end of the market segment presently supported by the Multibus. Steve Gold at Micro Link has also recognized this dramatic shift of emphasis relative to the STD bus.

"The STD bus is no longer restricted to one function per card," he says. It is now possible, within the small card size, to produce multi-function cards at the same price as the older single-function cards. For example, serial or parallel I/O or a serial port and timers can be combined with a CPU. Many vendors have done this, including Micro-Link. With multi-function boards, the STD bus can be used in a wider variety of markets, including full-blown microcomputers. With the tre-

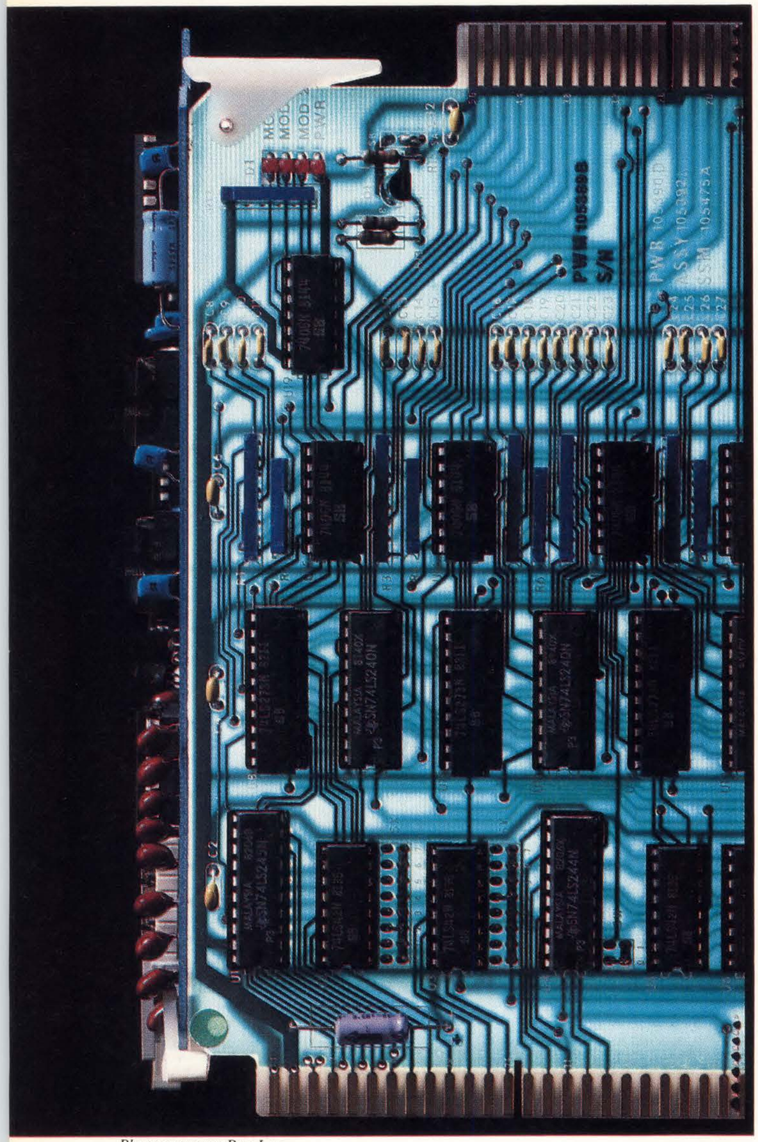


Photo courtesy Pro-Log

mendous range of industrial input/output functions available, a new breed of computer has emerged with data processing and control capabilities in the same box and now even on one small board.

Spenser Silverstein of Ironics found that "it is better to put more functions on a single card, rather than to try to distribute complex functions over many cards plugged into the bus." To this end, he sees more use of multilayer cards, small 'S0' surface mount packages such as those supplied by Signetics and the use of gate arrays to increase function, protect proprietary designs and reduce costs.

Since modularity was key to the success of the STD bus, it may seem strange that manufacturers would try to break away from it. Some larger cards have suffered in the market from packing too many functions onto the board that are not required by the designer, leading to wasted board area and components, and augmenting the troubleshooting headache. Increasing functionality onboard is related to OEM application and price reduction pressures.

The STD concept of "modular by function", has moved to "functionally modular." The difference is subtle but very important. Since more functions are being integrated on a single chip, the 4½″ × 6½″ board size is no longer a constraint to multiple functions on an STD board.

The major benefits to multiple functions on a board are space savings and potential cost savings. An example of this is Pro-Log's new 7806, a Z80 CPU card with four 28-pin JEDEC-compatible memory sockets, a dual UART and four channels of CTC on a single board. This card costs 27.5% less than the comparable functions on two boards.

Savings should be evaluated against the potential problems of integrating multiple functions on a single board. Pro-Log's product repair experience indicates the vast majority of field failure problems are associated with I/O. Separating the I/O board from the remainder of the system provides a measure of security by buffering the I/O, via the bus interface, from the processor and memory. This approach also reduces the cost of stocking spare boards, since I/O boards are usually less expensive than multifunction cards. If the STD bus application is neither space nor cost sensitive, as in a one-of-a-kind test system, it may make more sense to separate the I/O function and prevent potential problems.

In response to demand for more processing power, the STD bus will evolve to be a distributed system in which remote systems are served by a centrally located multiple processor system, as shown in **Figure 1**. In this configuration, the STD bus converts from an execution bus to a data transfer bus. Program execution is the responsibility of the processor on the individual cards in the system. Thus, system operating speed does not depend on the speed of the central or master processor. Data being transferred between processors can be handled in a high speed DMA mode, further enhancing system speed. Processing power and memory are distributed, accomplishing multi-tasks through multi-processing, which seems an obvious role of cheap processors and memory.

The shortage of processing power and memory space becomes a problem in the design of centralized systems, hence the integration of greater functionality on-board (**Table 1**). In contrast to high-performance bus systems, the STD bus has focused on the integration of specialized I/O control functions with μP technology through a modular bussing scheme.

The bus interface connector as shown in **Figure 2** is dedicated to μP control of the card functions. Peripheral and I/O device connections are made at the edge of the card defined as the user interface, for an orderly signal flow across the card from the bus interface to the user interface. Peripheral and I/O devices can be connected to the system using their unique connector and cabling requirements and complete functions can be modularly added to the system. The system designer

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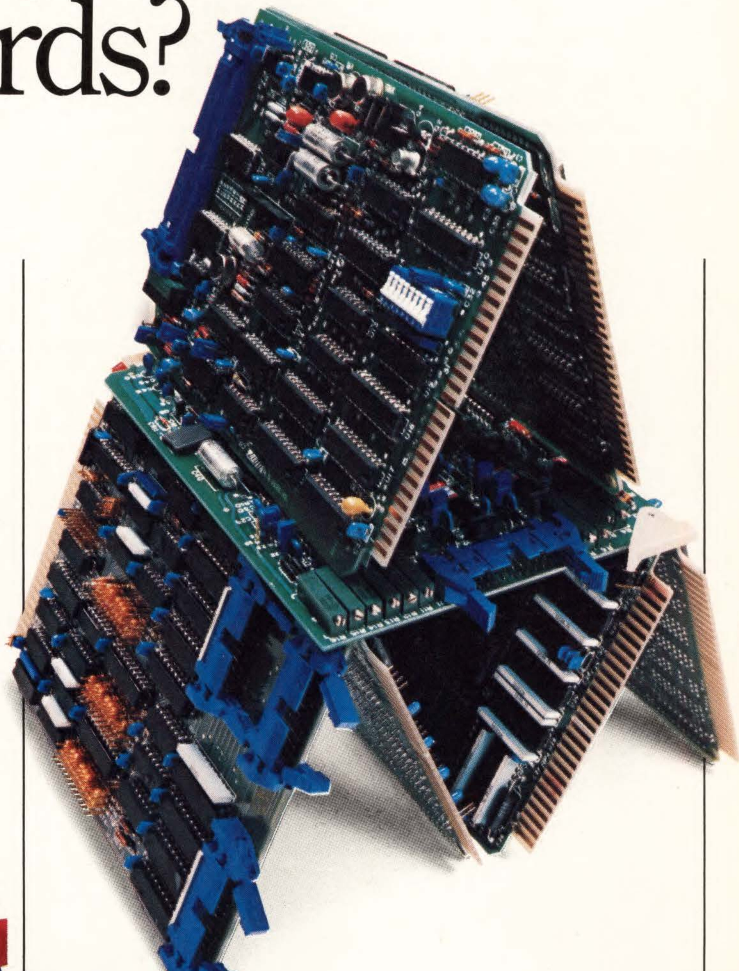

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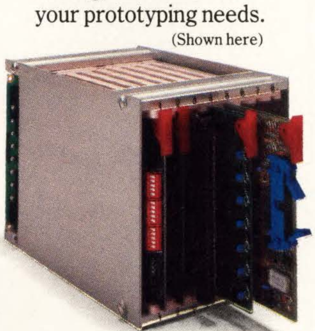

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has only to select a function and connect a cable to an often familiar interface.

STD Basics

As it exists today, the STD bus pinout consists of five functional groups: the logic power bus, the data bus, the address bus, the control bus, and the auxiliary power bus. (**Figure 3**). The data bus is 8-bit bidirectional and the address bus is 16 bits wide. The dual power busses accommodate both logic and analog power distribution. As many as five separate power supplies can be used with two separate ground returns. Pin 5 provides for alternate use as a battery backup supply voltage and for disconnect capability on the card for conflict reasons. STD bus cards that use peripheral chips usually depend on specific timing signals from the processor. This dependency prevents peripheral cards from being used interchangeably with cards from other families. The STD practice for designating compatibility is to label cards that are processor-timing dependent with reference to the CPU device: STD-Z80, STD-8085 and STD-6800, etc.

Interrupt And Control Lines

Interrupt and control lines allow for the implementation of such bus control schemes as DMA, multi-processing, single-stepping, slow memory, power-fail restart and a variety of interrupt methods.

The bus acknowledge signal (BUSAK*) originates from the permanent master to indicate that the bus is available for use by a temporary master. This release of the bus and acknowledge signal on the BUSAK* line is a response to a BUSRQ* signal from a temporary master. BUSRQ* causes the permanent master to suspend operations on the bus by releasing all 3-state bus lines. BUSAK* should occur at the completion of the current machine cycle and be combined with a pri-

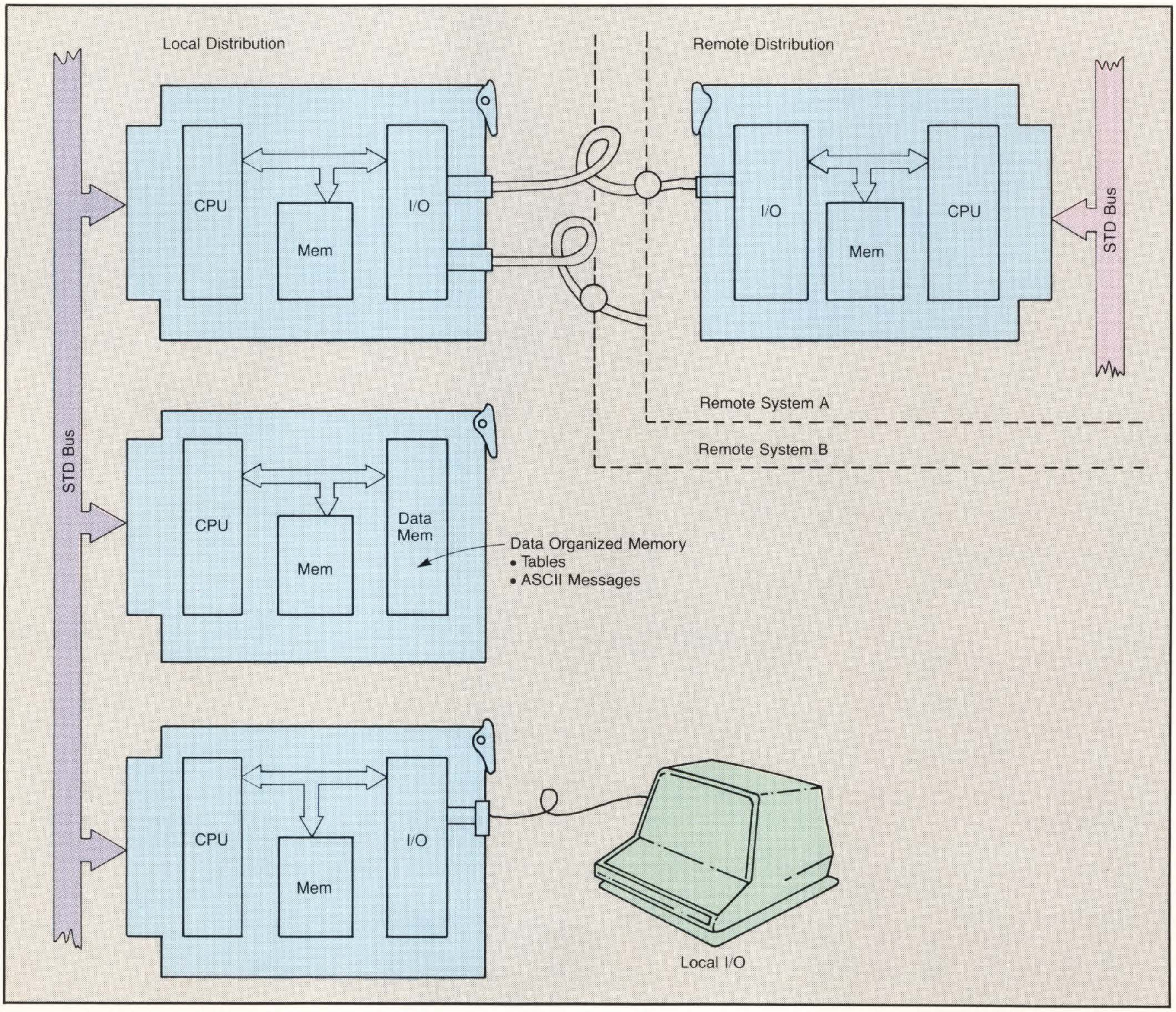

Figure 1: The STD bus as a distributed system.

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Interfacing to Motors

The STD-16 from Amtek (Seattle, WA) can be configured to provide STD-Bus computer interface for applications including virtually any type of servo motor or hydraulic primemover. Some examples of these applications are illustrated in **Figures 1, 2,** and **3.** The output control signal is an industry standard ±10VDC and can be matched to the vast majority of motor or valve servo amplifiers. The card has eight TTL inputs, two interrupt inputs, and eight TTL outputs. These are usually used for typical auxiliary controls, such as "home limit" switch and "stop" push button.

The input circuitry is arranged for quadrature incremental encoders, with full directional information detection. Power for the encoder can be routed through the card for easy connection. Acceleration and deceleration rates are controlled by the amplifier loop gain adjustments available on industry standard amplifiers.

In the application illustrated, the controlled axis shown is slaved to a pulse train that originates from a separate source. The source of these pulses can be another encoder, a clock card, an Amtek STD-25, or another Amtek STD-16. **Write 401**

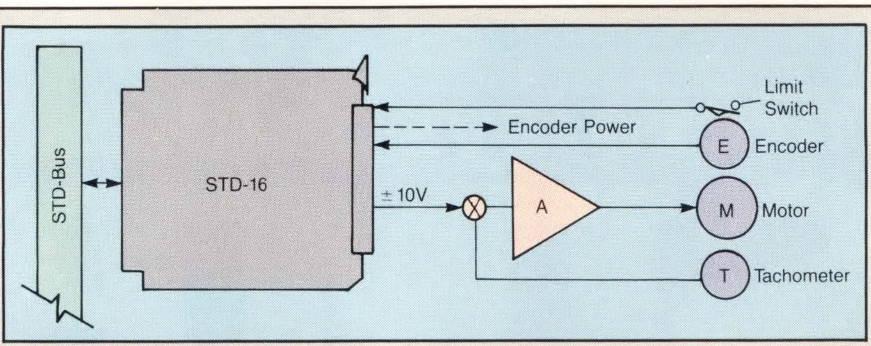


Figure 1: Motor-servo loop diagram.

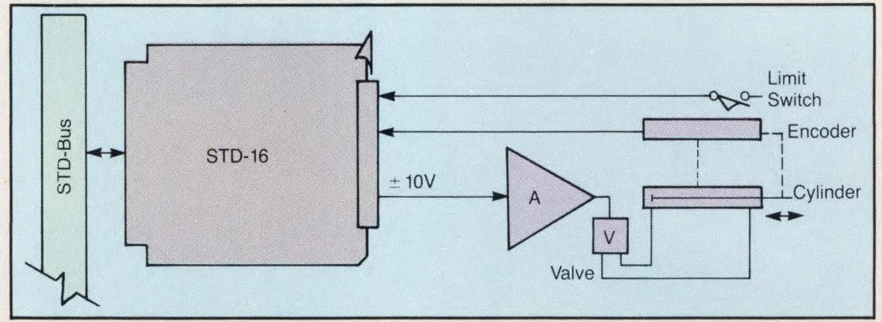


Figure 2: Hydraulic-servo loop diagram.

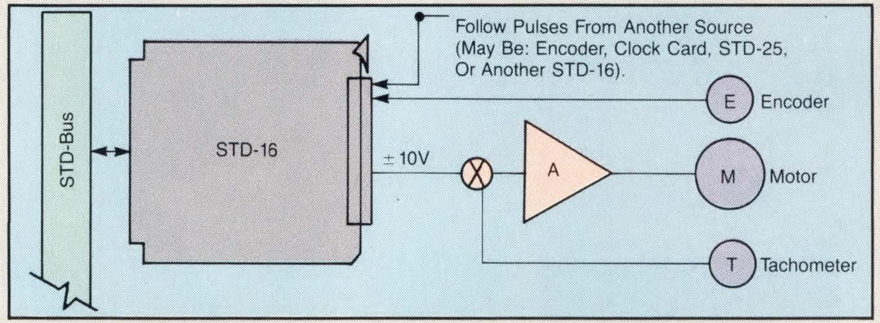


Figure 3: Slaved motor-servo loop diagram.

ority signal if multiple controllers need bus access.

BUSRQ* can be used in applications that require direct memory access (DMA). A DMA transfers data directly to and from memory without passing through a processor. Very high data rates are possible with this type of interface, but with complex hardware. DMA interfaces must include circuitry to share the bus with the processor, keep track of the current memory address being accessed, generate memory control signals, latch data being transferred and drive the data address and control lines. The requirements for the memory control signals are identical to those for the processor since memory does not know whether it is being accessed by the processor or by a DMA interface.

Interrupt Priority Practice

The STD bus provides signal lines for interrupt requests. In systems with only a single interrupting device, these lines are sufficient to allow direct implementation. In systems with multiple interrupting devices, a priority scheme is necessary. The STD bus includes a priority-chain bus signal for serial priority schemes. Serial priority, using PCI and PCO signals, requires that each peripheral needing priority must have logic on the card to service the request, as shown in **Figure 4.** This scheme is practical with peripheral devices designed to service a serial priority chain such as the Z80 family of devices.

A parallel priority scheme for interrupts can also be implemented on the STD bus, so that the priority logic resides on a separate card and not on each peripheral card. The parallel priority card has a modular function that can be tailored to individual processor requirements, allowing peripheral cards to be processor independent.

This scheme requires that the individual requests be made from the user edge of the card, as shown in **Figure 5.** The parallel priority encoder could be included on the processor card. Interrupts handled from the user edge of the card is a useful feature, because the processor can now go through the interrupt controller rather than using the daisy-chain method through the backplane.

As can be seen from **Figure 4**, there are three sig-

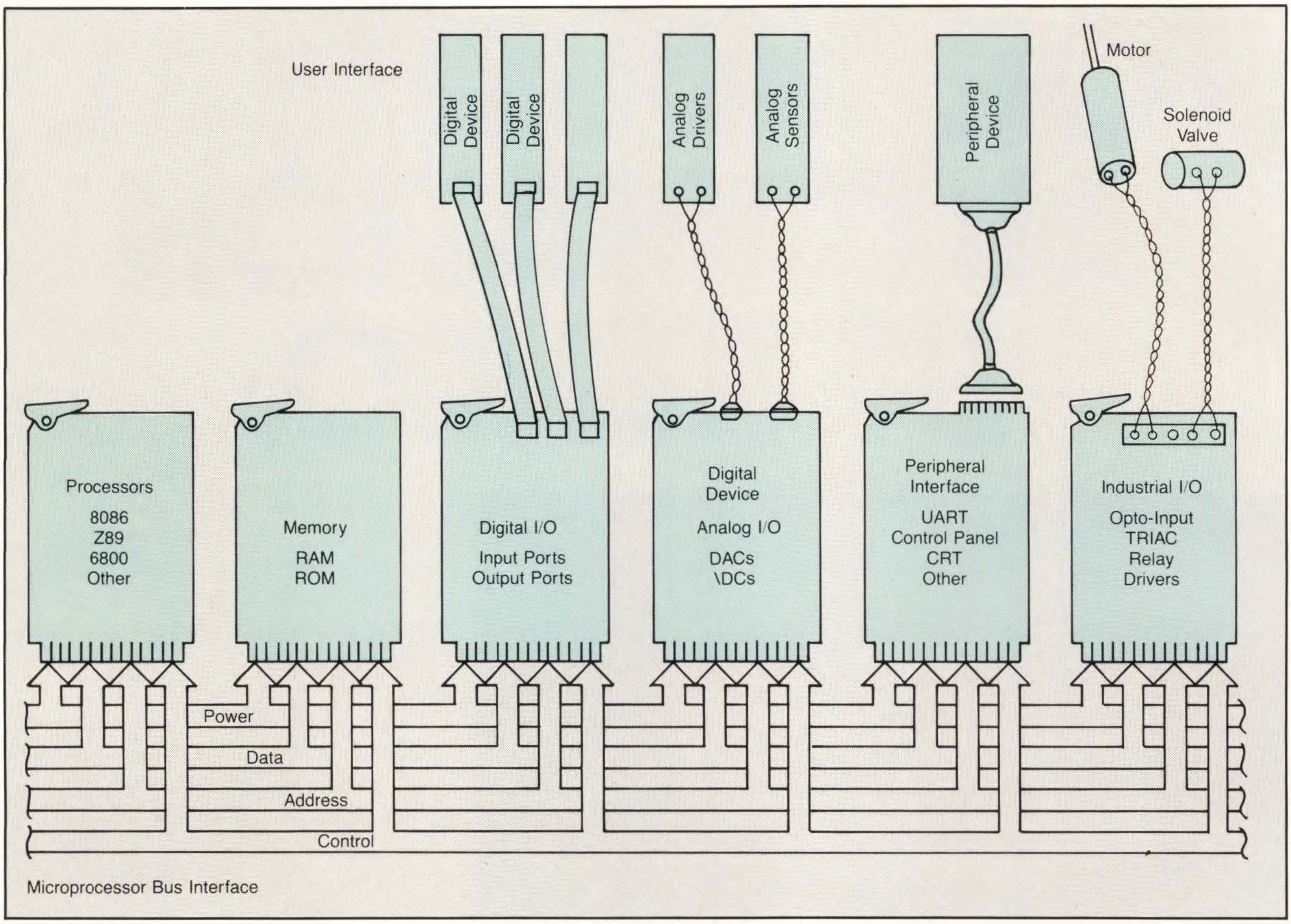


Figure 2: The STD bus interface connector.

nals that allow for the implementation of the serial priority scheme: the internal bus request (BRQ*), bus acknowledge in (BAI*) and bus acknowledge out (BAO*). The BRQ* signal indicates that the card is requesting bus control. BRQ* drives BUSRQ* on the bus. When BRQ* and BUSAK* are low and BAI* is high, bus control is given to this card. In serial priority, BAI* is high during a BUSAK* cycle if BRQ* is high. BAO* is connected to BAI* of the next lowest priority controller.

As can be seen from **Figure 5,** there are two signals that allow for the implementation of the parallel priority scheme, BRQ* and BAI*. BRQ* indicates that the card is requesting bus control and is passed separately by each controller card to a priority resolver card via the user interface. The priority resolver controls BUSRQ* and responds to BUSAK* on the STD bus. BAI* is passed separately from the priority resolver card to each controller card via the user interface. Bus control is given to the controller card that senses BAI* low.

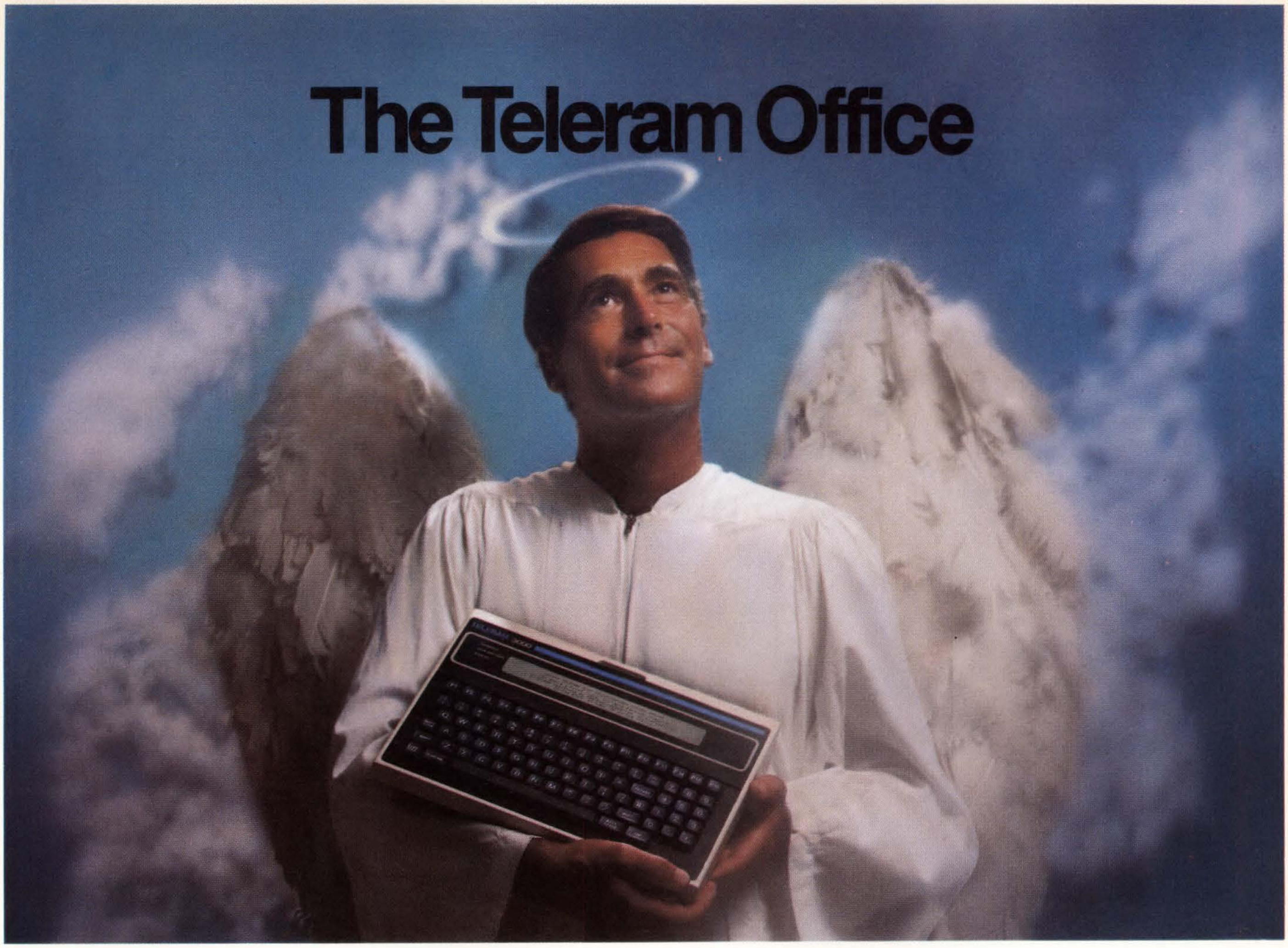
Interrupts

The STD bus supports two types of interrupts, maskable and nonmaskable. The nonmaskable interrupt (NMIRQ*) is a processor card interrupt of the highest priority and is usually used for critical processor signalling, such as power fail indications.

The interrupt acknowledge (INTAK*) is a signal that tells the interrupting device that the processor card is ready to respond to an interrupt. For vectored interrupts, the interrupting device places the vector address on the data bus during INTAK*. This signal can be combined with a priority signal if multiple control-

Distributed	Centralized
Hardware/Software Solution	Software Solution
Distributed Processing Power	Demands More Processing Power
Distributed Memory	Demands Larger Memory
Localized Modular Software	More Sophisticated Software (Multi-Tasking)
Modular	Integrated
Simple Conceptually	Complex Conceptually

Table 1: The differences between a distributed and centralized system.



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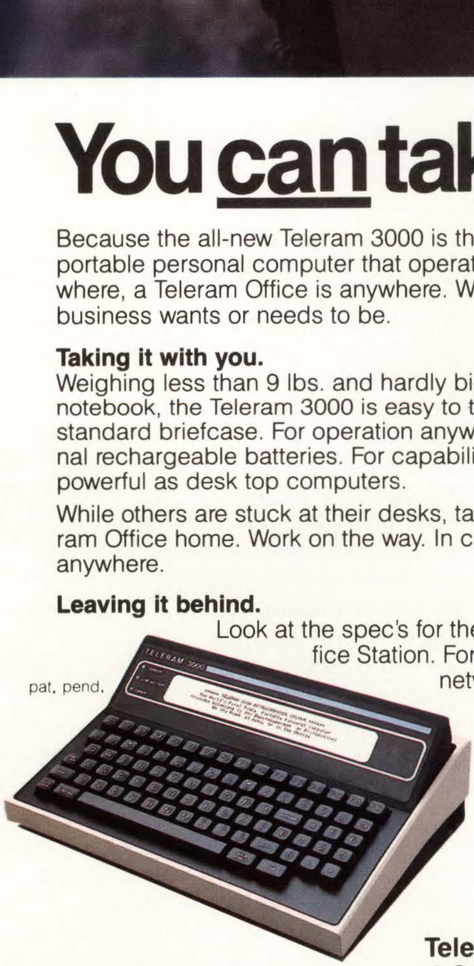
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RS232C Interface (communications or printing)
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Write 40 on Reader Inquiry Card

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5VDC	In	Logic Power (bussed)	2	+5VDC	In	Logic Power (bussed)
	3	GND	In	Logic Ground (bussed)	4	GND	In	Logic Ground (bussed)
	5	VBB#1/VBAT	In	Logic Bias #1/VBAT	6	VBB#2	In	Logic Bias #2 (−5V)
DATA BUS	7	D3/A19	In/Out	Low-Order Data Bus	8	D7/A23	In/Out	High-Order Data Bus
	9	D2/A18	In/Out	Low-Order Data Bus	10	D6/A22	In/Out	High-Order Data Bus
	11	D1/A17	In/Out	Low-Order Data Bus	12	D5/A21	In/Out	High-Order Data Bus
	13	D0/A16	In/Out	Low-Order Data Bus	14	D4/A20	In/Out	High-Order Data Bus
ADDRESS BUS	15	A7	Out	Low-Order Address Bus	16	A15	Out	High-Order Address Bus
	17	A6	Out	Low-Order Address Bus	18	A14	Out	High-Order Address Bus
	19	A5	Out	Low-Order Address Bus	20	A13	Out	High-Order Address Bus
	21	A4	Out	Low-Order Address Bus	22	A12	Out	High-Order Address Bus
	23	A3	Out	Low-Order Address Bus	24	A11	Out	High-Order Address Bus
	25	A2	Out	Low-Order Address Bus	26	A10	Out	High-Order Address Bus
	27	A1	Out	Low-Order Address Bus	28	A9	Out	High-Order Address Bus
	29	A0	Out	Low-Order Address Bus	30	A8	Out	High-Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Stataus	40	STATUS 0*	Out	CPU Status
	41	BVUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push-Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground (bussed)	54	AUXGND	In	AUX Ground (Bussed)
	55	AUX + V	In	AUX Positive (+12V DC)	56	AUX-V	In	AUX Negative (−12V DC)

*Low-level active indicator

Figure 3: Bus connector pin assignments.

lers need bus access. INTAK* is not used in non-vectored interrupt schemes.

The interrupt request (INTRQ*) is a processor-card input signal that conditionally interrupts the program. It is masked and deliberately ignored by the processor unless enabled by a program instruction. If the processor accepts the interrupt, it usually acknowledges by dropping INTAK* low.

More Memory

Memory handling techniques are currently being implemented to allow STD systems to be expanded beyond the 64K barrier to allow larger programs and more data to reside within main memory. Due to its 16-bit address bus, the STD bus supports a primary memory space of 64K. Expansion of memory to 128K is supported by the MEMEX line on the bus.

The MEMEX line is one of the signals for controlling fundamental memory operations, and MEMEX must be included in the memory selection decoders for the STD compatible memory cards. When MEMEX is low, the primary system memory is enabled. MEMEX may be used to enable an alternate 64K memory bank if the memory cards can be strapped for either high or low level enable by the MEMEX signal (**Figure 6**).

Additional memory is also made available to the CPU in banks. The CPU cannot address two separate banks without switching between the banks, and the technique is still limited to addressing 64K bytes at any one time. The memory banks are usually selected through an I/0 operation.

The on-board port scheme of memory expansion uses port address FF to decode and latch a strappable memory enable signal on each memory card. This scheme is represented in **Figure 7.** Port address FF is decoded to enable latching the card select from the data bus. The latch outputs are jumper selectable to allow bank assignment for individual cards. System reset forces selection of memory bank 1 for compatibility with existing software.

The off-board port scheme of memory expansion suggests using a standard output port and wiring to special memory cards via the user interface. The memory cards require a user interface connection into the memory selection decoder on the card, as shown in **Figure 8.**

According to Thomas Seim, President of Systek (Kennewick, WA), the first point for software with bank switched memory is that not all memory can be addressed at one time, so banks must be selected before being used. While this may seem obvious, it influences software organization.

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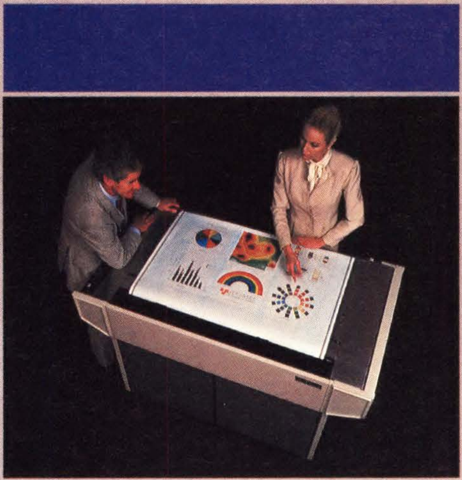

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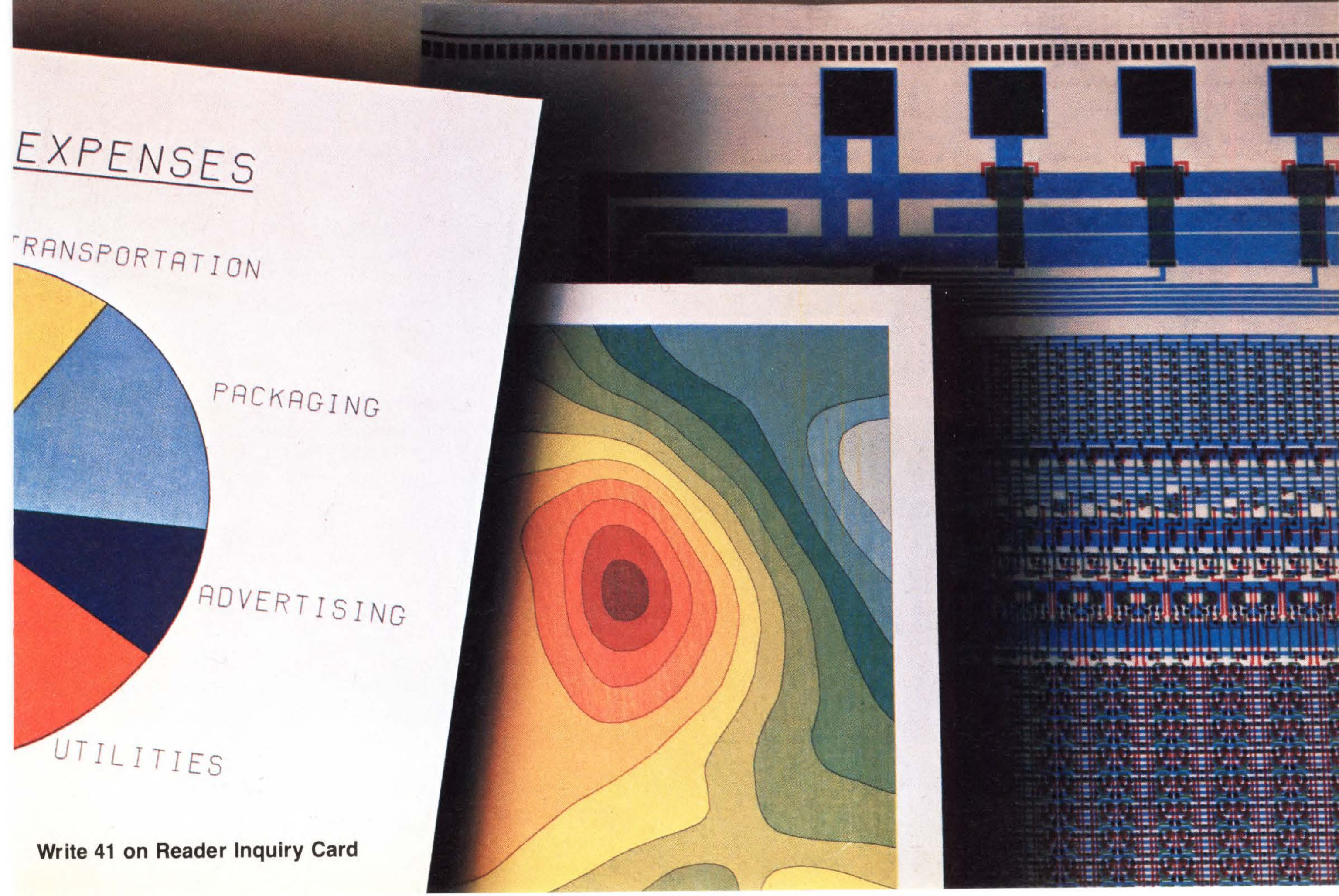
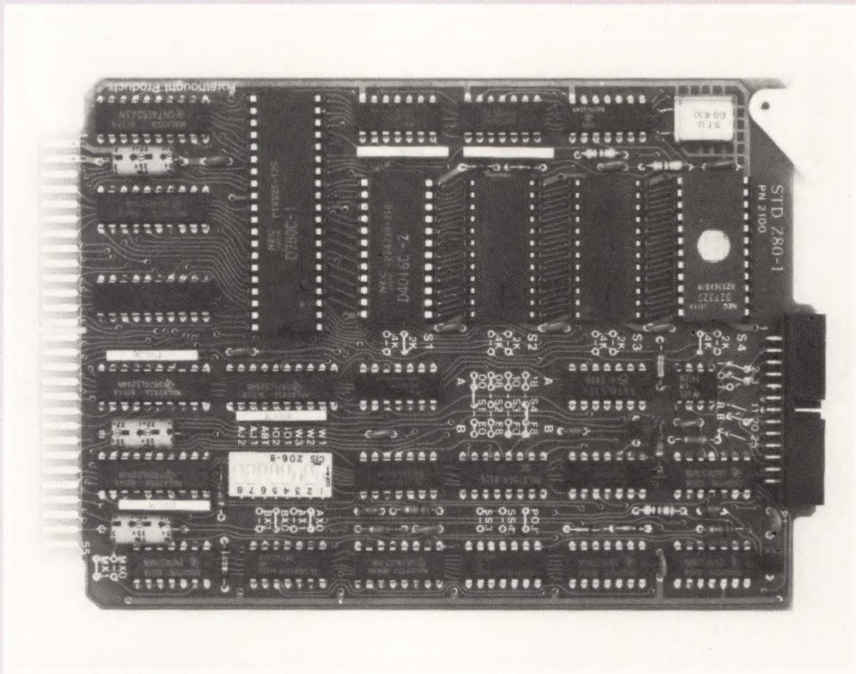
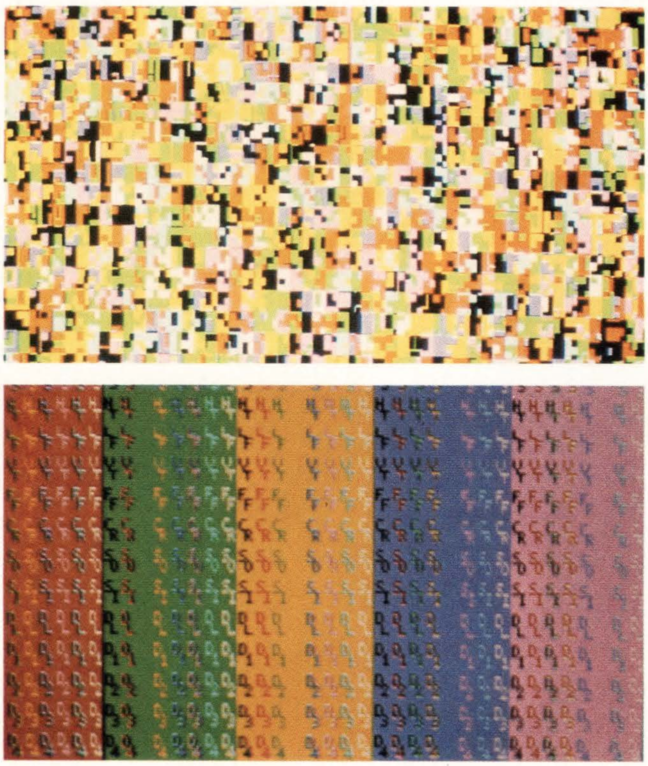


Write 41 on Reader Inquiry Card

STD Bus Processor Board Includes Diagnostic Functions

Forethought Products' (Eugene, OR) Z80 Smart Card combines a 4MHz Z80A μP with on-board serial port, RAM, and diagnostic firmware to become a combination processor/diagnostic unit for the STD bus. Connected to a standard RS-232 terminal, it can test any board (and even I/O devices) in the system with its built-in diagnostic functions. Additional commands, including Display/Alter memory and Read/Write to an I/O port, provide for system debugging. By setting an on-board switch the Smart Card functions as a normal Z80 processor card and does a power-on jump to user PROM. In the field, the system can be switched back to its diagnostic mode for system trouble-shooting, or maintenance. In addition, on-board hardware eliminates the need for additional RAM, ROM, or serial I/O boards in many applications. This simplifies system start-up and lowers system cost. **Write 402**





Color output from Ironics' CRT controller card. Top: full screen mode, bottom: character resolution within character block.

For example, it is inefficient to randomly access memory across bank boundaries as this requires the bank to be selected each time. As many operations as possible should be performed in one bank before switching to another. An example of this is a multi-user operating system that assigns each user one bank of memory. Banks are switched only as users are switched.

Because of the current trend in putting more powerful μPs such as Intel's 8088 onto the bus, it may be necessary to intermix both 16- and 20-bit memory boards in a system.

The Systek 1620 memory and I/O expansion controller for the STD bus permits the use of memory and memory-mapped I/O boards with 16-bit address decoding in systems with 20-bit memory addressing (Systek's model 8800 and Ziatech's model 8800 are both examples of CPU boards that generate a 20-bit address). Memory expansion is accomplished with the STD bus signal MEMEX. The 1620 decodes the most significant four address bits multiplexed over the data bus and asserts the MEMEX line when a jumper-selectable 64K byte block is addressed. MEMEX enables all 16-bit memory boards when asserted and disables them at all other times. This permits intermixing 16- and 20-bit memory boards (all 16-bit boards will map into the 64K byte segment set by the jumper matrix). Note that only those memory and memory-mapped boards that decode the MEMEX signal may

Core Memory For The STD Bus

8-bit STD bus products have found wide use in small industrial and process control systems. The modular organization of STD bus systems allows the designer to choose from many CPUs, memories, I/O and analog functions on the market today.

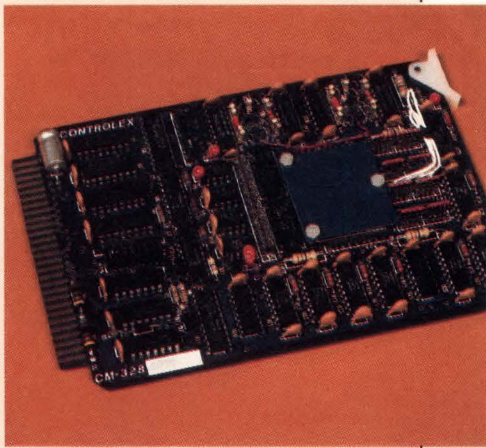


Figure 1: CM328, 256-byte core memory for STD bus.

An important requirement of real-time systems is the ability to store data and retain it through power shutdown, intentional or accidental. Such data may be safety limits, set points, machine or process states, real-time clock counts and tool positions. This class of data must be continuously updated during system operation, and at a rate such that devices such as EEPROMS, with their limited write endurance, are not usable. Another problem with NMOS devices is their relatively slow write speed, a clear disadvantage if updates are to be executed at full bus speed.

Controlex (Van Nuys, CA) chose core technology for the CM328 because it met all of the operational requirements for control systems: full bus speed, absolute nonvolatility without lifetime or fatigue, and cost competitiveness with alternate technologies.

The CM328, a 256 by 8 core memory system, is contained on a single STD bus format. In an effort to keep costs low, an industry standard 18 mil core was chosen that occupies less than one square inch of the board. Speed of the CM328 is sufficient to operate with a 2.5MHz CPU without wait states, and a faster version will be available for use with 4MHz CPUs.

The system is rated for operation from 0 to 70°C, and consumes an average power of 17W. Power is duty cycle dependent, with standby power of 9W. **Write 404**

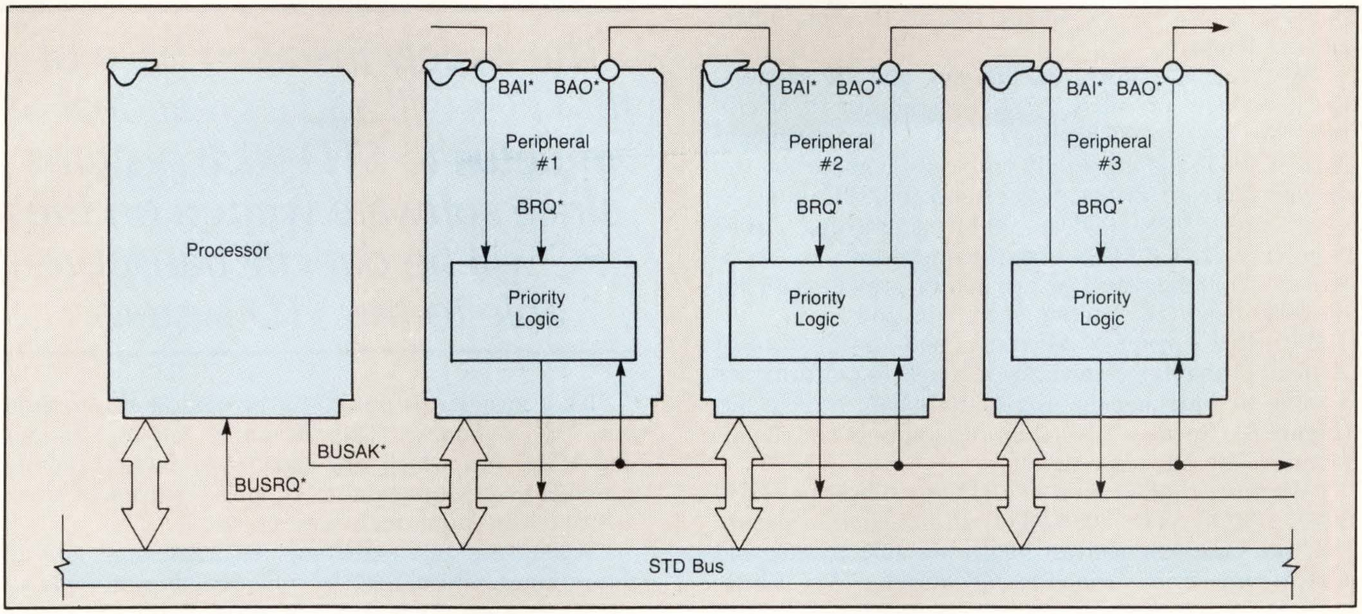


Figure 4: Serial scheme for bus priority.

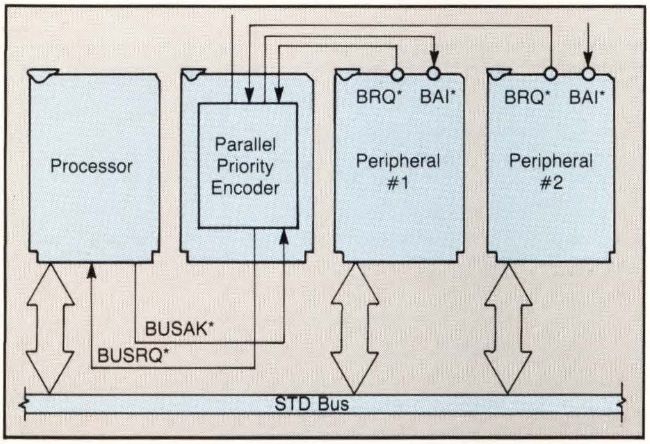


Figure 5: Parallel scheme for bus priority.

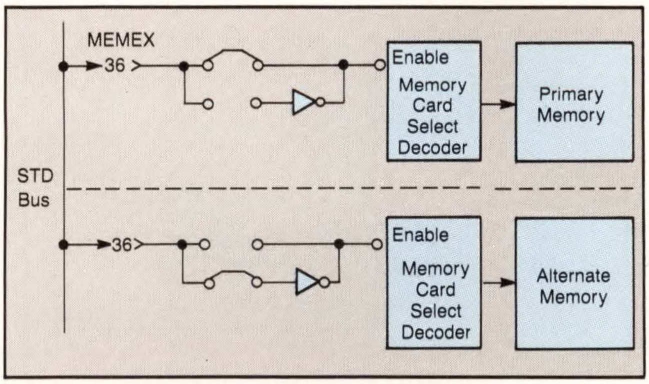


Figure 6: MEMEX memory bank selection.

be used in this manner.

The I/O expansion circuitry on the 1620 permits mixing I/O boards that decode only 8 bits with those that decode 16 bits through the use of the IOEXP signal. The IOEXP signal is asserted whenever an I/O address from 0 to 255 is generated (all upper eight address bits are zero). Only those I/O boards that decode IOEXP may be used with the 1620.

Moving Up To 16-Bits

The STD bus was designed around the requirements of an 8-bit μP. The limitations of an 8-bit data bus (one half what most 16-bit μPs need) and a 16-bit memory address bus (at least 4 bits short) presented a significant challenge to the STD system designer striving for an effective 16-bit design. In 1980, a committee headed by Bert Forbes at Ziatech was formed under the guidance of the STD Bus Manufacturers Association to develop a standard for the implementation of the 8088 processor. The 8088 was chosen because it has a byte-wide (8-bit) data bus that matched STD bus requirements. The real challenge was expanding the STD bus' memory addressing limits. The 8088 processor generates 20 address bits that represent the physical address in memory for a read or write cycle. The STD bus has only 16 dedicated address control lines, A0–A15, and 8088-based CPU cards must multiplex the higher order bits A16–A19 over the data bus lines at the beginning of each memory cycle. The memory board takes the 4 bits off the data bus, combines them with 16 bits from the address bus to achieve 1-Mbyte addressing.

As for the 8088 compatibility of existing STD I/O boards, several things should be taken into account. Speed is one important factor: some boards designed for old, slow CPUs require system wait states. If wait states must be forced by the CPU, the system is slowed up all the time. Therefore, an I/O board should originate wait states only when required. The I/O board interrupt modes must be compatible with the 8088 scheme. Z80 mode 1 and mode 2 interrupts are not supported by the 8088.

The widely installed base of IBM PCs will undoubtedly add a great deal of impetus to STD/8088 systems, since software written on the PC will be directly transportable to the STD system. While some express enthusiasm about the expanding role of the bus, others are less happy.

"We heartily endorse the scheme, and are supporting it on new products," says Ken Finster of Micro/Sys. "We have been shipping CP/M-86 since the beginning of 1983, and are wildly enthusiastic about the significant increase in the performance of STD bus systems with 8088 CPUs, 20-bit addressing, 8087 coprocessors, CP/M-86 and silicon-on-software techniques. This may well be the major growth path for the STD bus in the coming years," he adds.

Both Ken Finster of Micro/Sys and Jim Eckford of Ziatech probably perceive the increase in performance leading to widening the applications base for the bus (**Figure 9**). Spenser Silverstein of Ironics is one manufacturer who has some doubts.

"We see a proliferation of STD bus subspecies (Z80 STD, CMOS STD, 8088 STD) all designed to ensure that the customer will no longer be able to mix and match cards from various manufacturers." Mr. Silverstein feels that this will result in an S-100 like incompatibility problem where none existed before.

The widely installed base of IBM PCs will add a great deal of impetus to STD 8088 systems since software written on the PC will be directly transportable to the STD system.

"It's a mistake to put 16-bit processors on an 8-bit bus," he continues. "This should be left to Multibus and VME bus which are capable of handling more complex processors without kluging." Steven Connors at Data Translation feels the same way.

"When you start extending the addressing and all those things, you're making something very complicated out of something that was conceived as a simple thing for a customer to interface to," he says. "The

Development System For STD-Bus

Datricon Corp.'s (Lake Oswego, OR) software development system offers five high-level languages—PASCAL, COBOL, BASIC, C, and D-FORTH—as well as assembly language programming. This language library allows the engineer to choose the language that best matches the needs of both the particular application, and his own personal language preferences. The package includes two completely independent STD-Bus systems: a "development computer" (for generation and maintenance of application source code, and development of OS-9 based applications), and a "target" backplane (for configuration of actual application hardware and software).

All DV-9 development tools operate with or under Datricon's configuration of OS-9, a modular UNIX-like operating system which provides a multitasking, multi-user environment. The system is designed for generating ROM-resident application software based on either the OS-9 or D-FORTH high-level environment.

Write 403

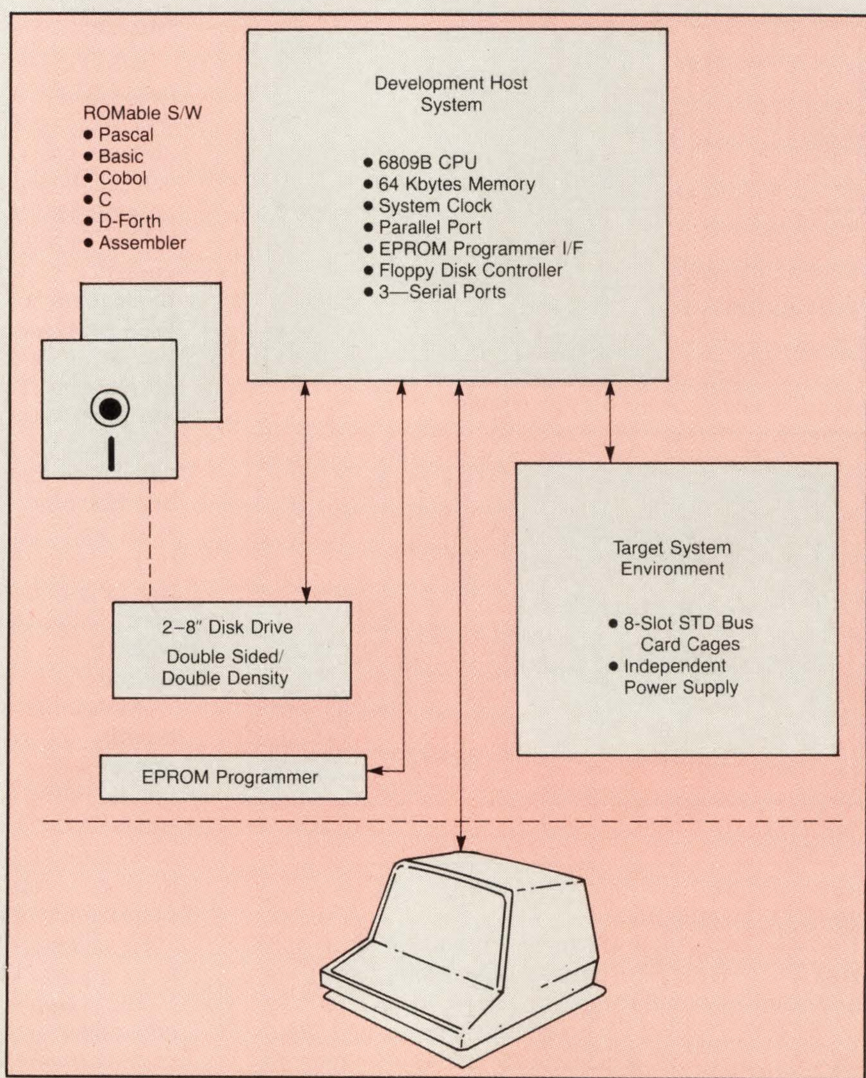


Figure 1: Datricon's DV-9 software engineering station.

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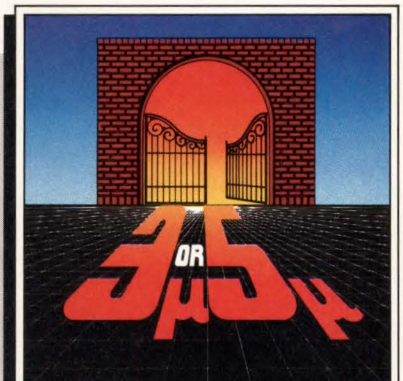

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1S03 or 5B	540	132 × 167	50 or 25 MHz	58
1S03 or 5C	720	159 × 167	50 or 25 MHz	64
1S03 or 5D	960	161 × 208	50 or 25 MHz	70
1S03 or 5E	1200	188 × 208	50 or 25 MHz	74
1S03 or 5F	1500	188 × 244	50 or 25 MHz	80
1S03 or 5G	1800	202 × 230	50 or 25 MHz	92
1S03 or 5H	2400	232 × 252	50 or 25 MHz	110

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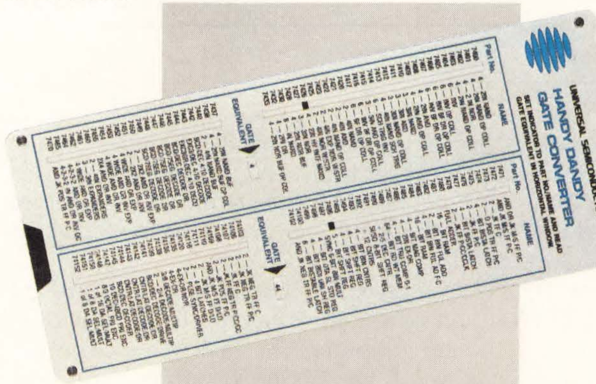

Write 43 on Reader Inquiry Card

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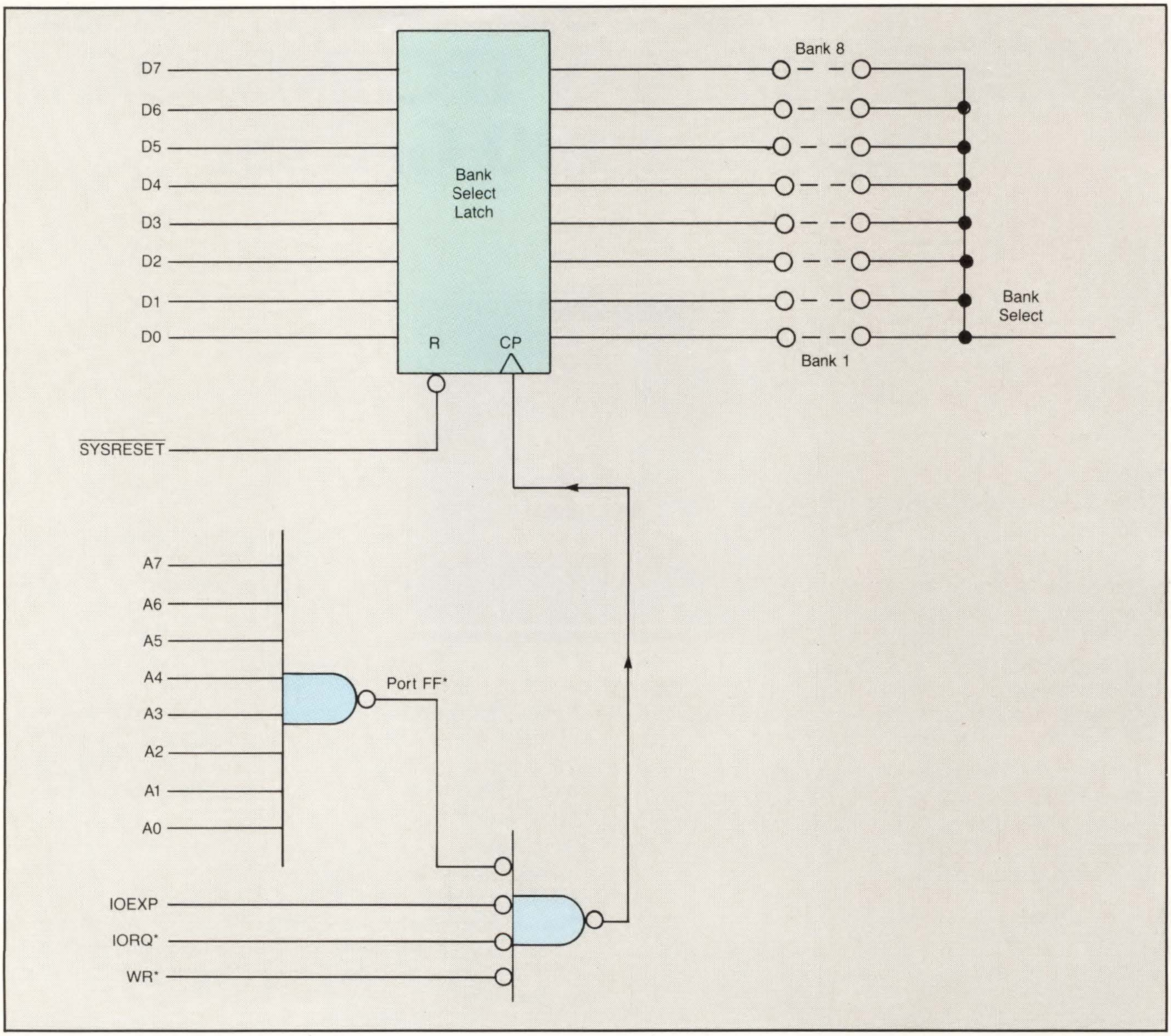


Figure 7: On board port memory selection.

STD bus is going into non-typical computer industries—if it gets more complicated, people will be isolated from the bus." Spenser Silverstein also perceives the vital need for simplicity, and feels that the STD bus will expand on the low end.

"The typical customer will be the one that missed the μP revolution and is now coming to grips with it via the kid's home computer," he says. This customer needs simplicity to sell him on the idea of using a computer—not confusion.

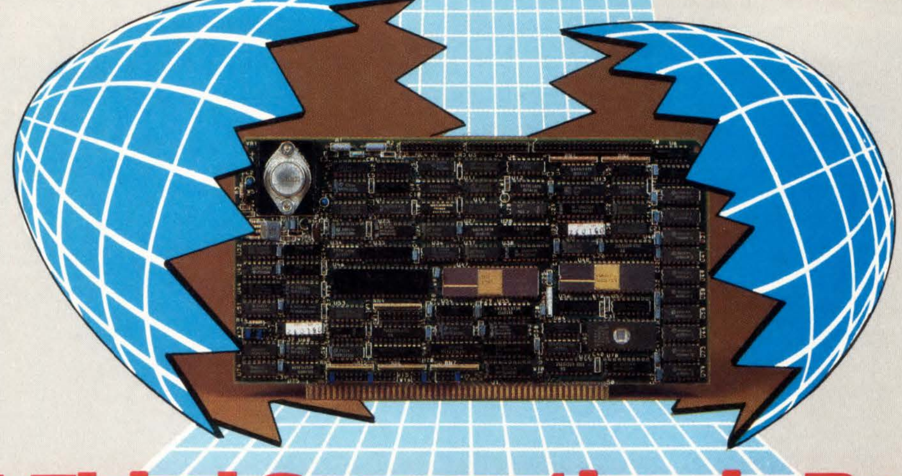
Multichannel I/O For The STD Bus

Many designers feel that the most attractive features of the STD bus are its simplicity, compactness and low power usage. Therefore, an I/O scheme that would require only one low power interface card and provide for the connection of many I/O devices would be ideal. One of the difficulties with establishing a standard of this type, as is currently the case with Intel's Multichannel design for the Multibus, is that it takes a year or so for I/O devices that contain compatible interface electronics to become available.

Fortunately, a type of Multichannel for the STD bus exists and currently interfaces to over 2000 instruments, peripherals, and computers. It is called the General Purpose Interface Bus (GPIB) and was adoped by the IEEE in 1978 as the IEEE-488 standard for programmable instrumentation interfacing.

Ziatech has adopted this multichannel scheme in 3 ways. The simplest way allows an STD bus to function as a talker/listener on a multichannel GPIB cable. As shown in **Figure 10,** an STD bus based transistor tester can be connected to the same cable along with up to 14 other devices. An extension of this capability allows

Incubation Complete



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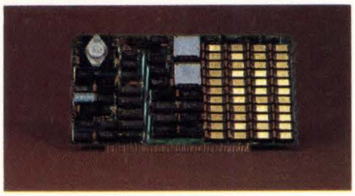

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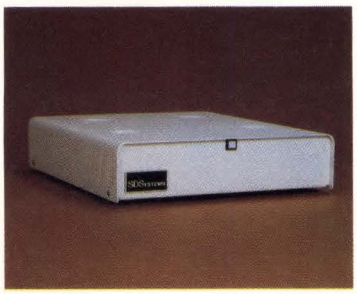

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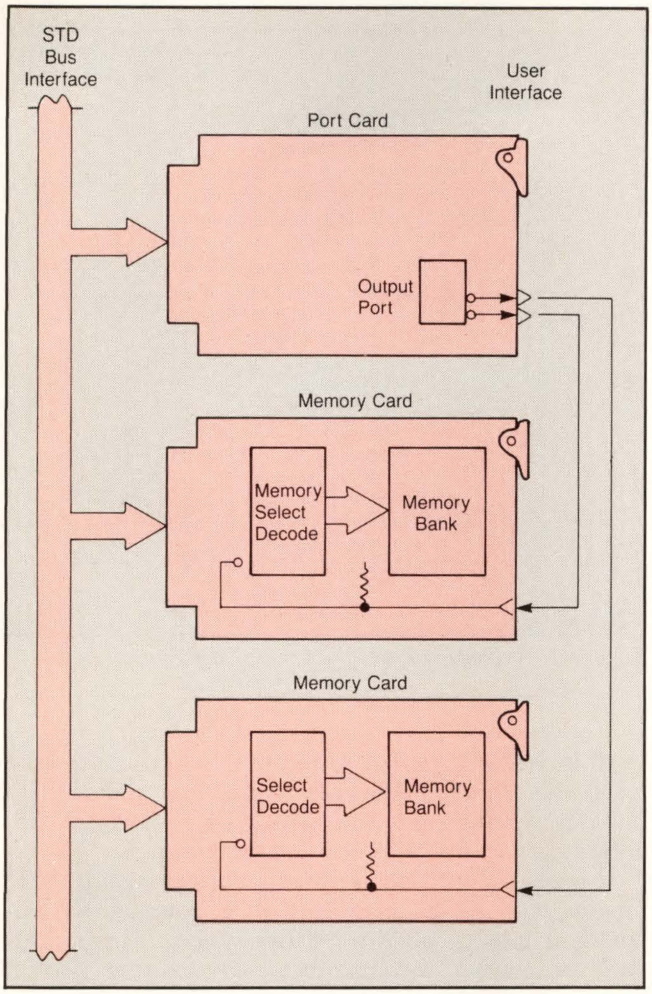

Figure 8: Off board port memory selection.

the STD bus system to function as a controller, so it can take charge of the bus and direct the activity of all the devices.

The most sophisticated system is a single STD bus board that contains GPIB controller capability as well as a general purpose 8085 processor, two channels of RS232 and RAM and ROM. This board, the ZT 7805, is a complete STD bus system with multichannel capability. For example, one OEM uses the 7805 in a blood analyzer to control the functions of the instrument as well as interface to an HP desktop computer through the GPIB (**Figure 11**).

Extending The STD Bus Off The Backplane

The STD bus backplane is sensitive to layout, length and loading and is subject to speed limitations. The bus is confined to the backplane so that its characteristics can be predicted and controlled. Because of the critical nature of the bus, extension of the bus off the backplane is not recommended.

The physical characteristics of the bus, with its ordered layout of parallel signal traces, causes the bus to act as a controlled transmission line. Transmission lines of this nature have the undesirable signal properties of crosstalk and line reflections. The ordered bus layout allows these properties to be predicted and controlled.

Crosstalk on a printed circuit bus backplane cannot be eliminated. However, some element of control is possible with proper layout considerations. Uniform track spacing and the use of ground planes or ground track shielding should be considered. A uniform distribution of signal track to ground capacitance will provide some rise time control that will reduce crosstalk.

Backplane Terminations

The reflection charcteristics of the bus signal lines can and should be controlled with proper termination. Ideally, each signal is terminated in its theoretical characteristic impedence. The backplane bus impedance is predictable; however, as cards are introduced into various slots along the bus, the impedance can only be estimated.

There are various methods of providing physical termination. An example using passive AC termination is shown in **Figure 12.** This circuit does not affect the DC drive and loading of the bus signal; however, high frequency ringing is effectively terminated to the characteristic impedance of the bus line.

Since loading changes with the number and location of cards on the bus, optional termination location is impossible. Considering first order effects, termination networks can be located either on the backplane motherboard or on a separate terminator card.

Bus driving devices for LSTTL do not pull the bus signals to the full 5V high level. Full 5V logic swings

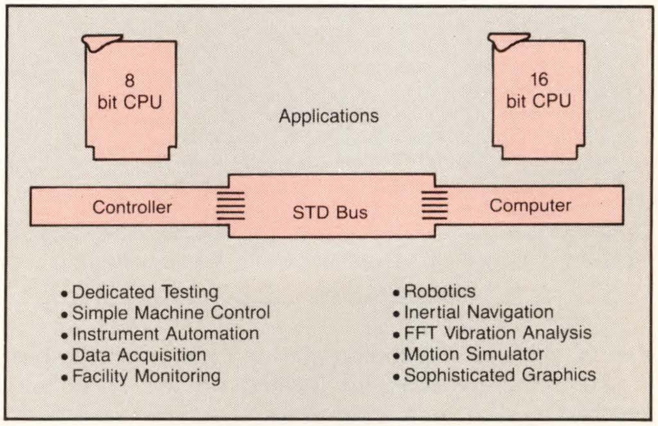

Figure 9: The widening applications base for the STD bus.

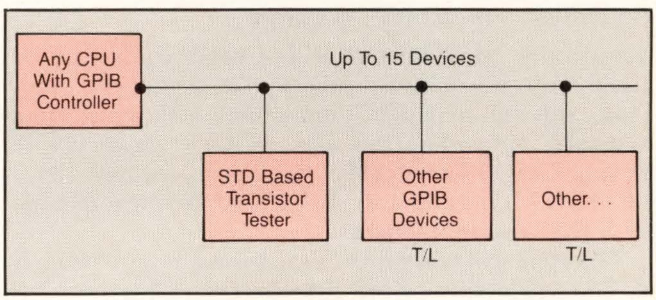

Figure 10: Talker/listener on a GPIB cable.

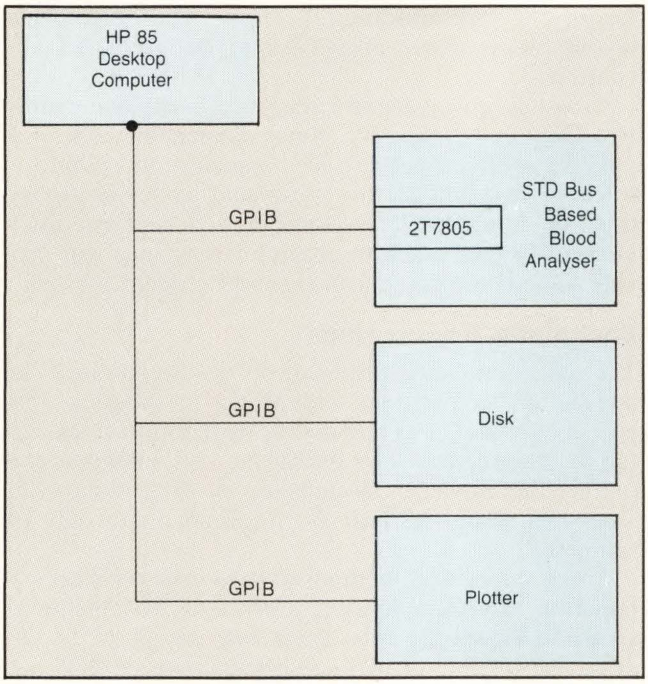

Figure 11: One OEM uses the Ziatech 7805 in a blood analyzer.

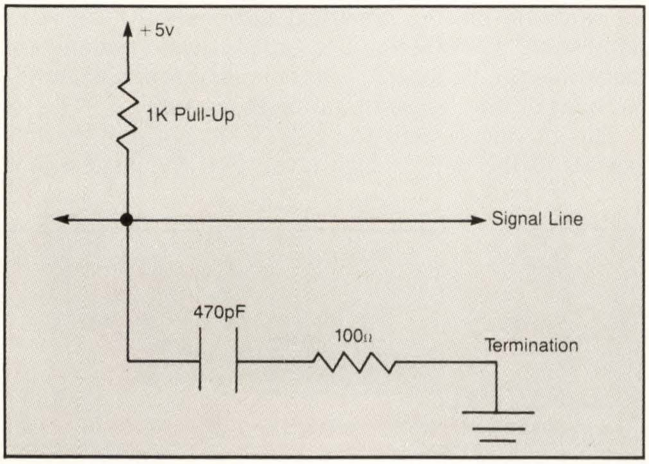

Figure 12: Passive AC termination and signal pull-ups.

can be achieved by adding pull-up resistors to the bus signals. Pull-ups may be located on the backplane motherboard or on a separate card. A 1KΩ resistor is recommended for the LSTTL bus (**Figure 12**).

STD Bus: The CMOS Version

Prospective purchasers of STD CMOS cards may be faced with two options in the future. Either the available cards will maintain compatibility with the existing standards, providing the user with the capability of mixing CMOS with NMOS products, or a new range of STD CMOS cards will appear that are incompatible with the existing standard.

The technical feasibility of the former approach rests on the availability of bus drivers (from Mitel, for example); this has been achieved by Baradine Products

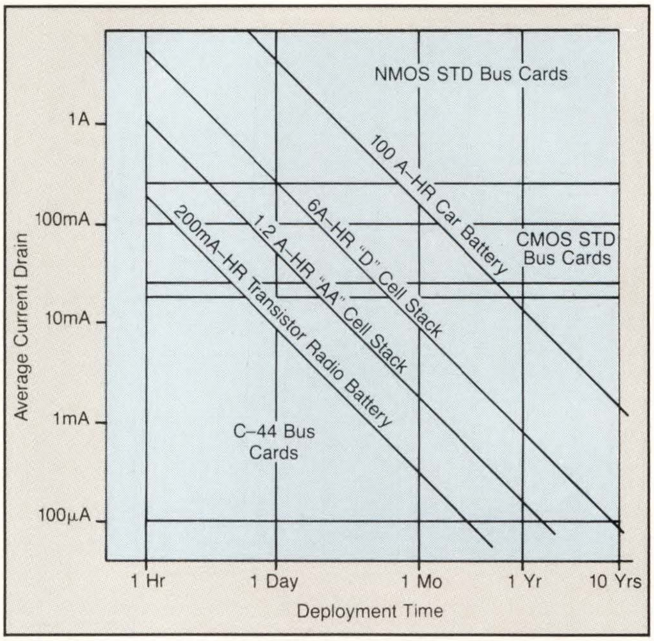

Figure 13: Average current drain versus deployment time.

with its NSC800 card reported in the April 1982 issue of *Digital Design*. However, a user may not wish to mix his existing cards with CMOS ones since CMOS' advantages lie in low power consumption.

Pro-Log's approach is to repopulate existing STD boards with pin-compatible CMOS components, enabling a user to build a CMOS system. These cards are, of course, incompatible with existing NMOS ones. The first three offerings from Pro-Log are the 80C85A-based card (the 78C05), a memory card (the 77C02) and a GPIB interface (the 75C05).

A more severe application limitation, according to Lon Hocker at Onset Computer (Falmouth, MA), is where battery power is the only power available. The deployment lifetime is determined by the average system current drain and the size of the battery pack (**Figure 13**), and can have a dramatic impact on the practicality of a design. For example, a data logger requiring a two-month deployment would take a motorcycle battery if the equipment drew 30mA average, a stack of D-cells at 3mA, and only a transistor radio battery if the current drain were 100 μA or less. Although the STD bus could be adapted for these low power applications, substantial modifications would be required.

Conclusion

The STD bus has a wide following in the industrial world, an area that has typically not employed a great deal of computer expertise. In addition to board level products, a wide variety of systems are available to help out with design tasks. Even Pro-Log recently entered the sytems business with their ABL-1, a system that can be used either as a development tool or as a target system. These design tools tend to be very easy to use, enabling design engineers to develop solutions to their companies' problems. □

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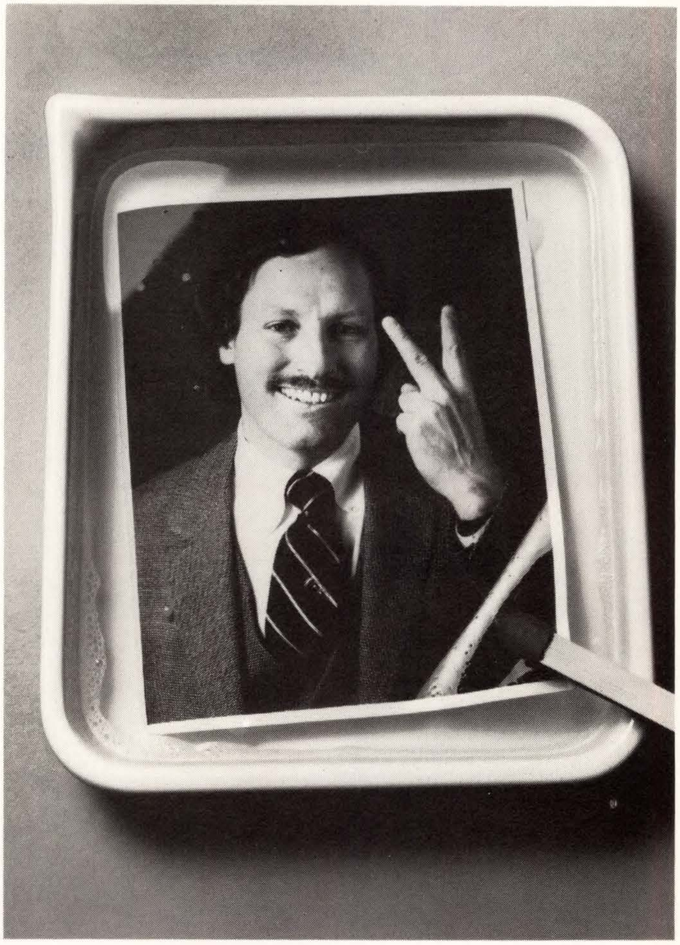

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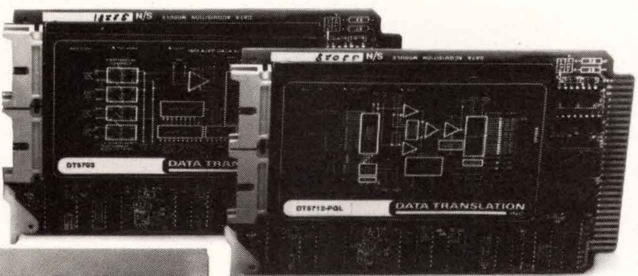

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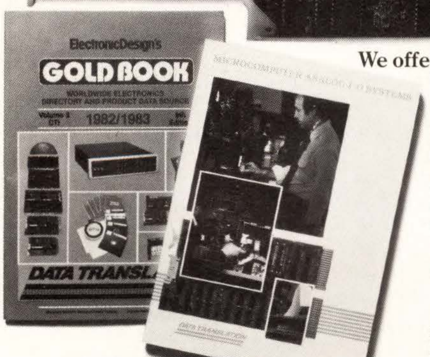

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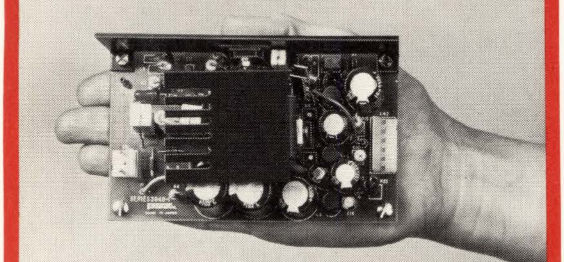

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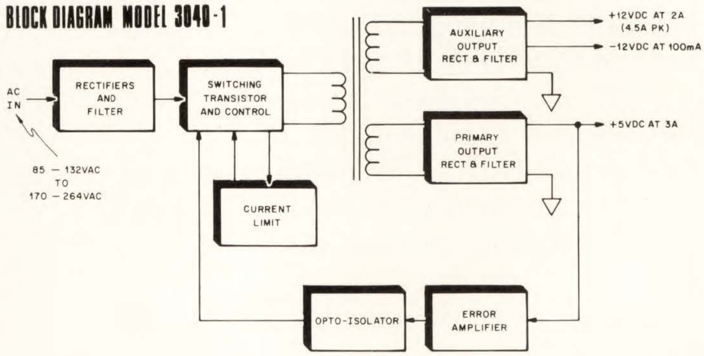

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3040-1	+ 5	0.45	3.0	± 2%	50	150	± 1%	± 0.4%	$79.00
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	− 12	0.00	0.1	± 10%	150	250	± 6%(1)	± 2%	
1035-1	+ 5	1	7	± 2%	100	100	± 2%	± 1%	$75.00
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1035-4	+ 24	0.3	1.5	± 2%	100	150	± 2%	± 1%	
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Diverse UPS Technologies Provide Design Alternatives

Recent advances in power systems technology are demanding an expansion of the definition of UPS.

by F. Kurt Shafer

"Power Failure" describes loss of power of any duration, from glitches of sub-μsec duration to blackouts lasting days. The task of isolating electronic systems from power failures has spawned a bewildering assortment of methods, systems and companies. Options range from isolation transformers that filter noise to engine generators capable of replacing utility power completely.

The primary goal of an Uninterruptible Power Supply (UPS) is to provide power to the load for enough time after utility power failure to allow for orderly system shutdown or transfer to an auxiliary power source for continued system operation. Traditionally, the term UPS describes an electronic system that takes utility AC power as its input, rectifies the AC to DC, stores energy in a battery bank, and converts the DC back to AC through a semiconductor inverter to drive a load. Recent advances in power systems technology demand an expansion of that definition. UPS is defined here to include DC backup, static inverters, and motor generator sets that use energy storage to provide uninterruptible power during a system's orderly shutdown or switch to alternate power.

F. Kurt Shafer is an engineer/technical writer residing in Manhattan Beach, CA.

Alternate Power Sources

Today there are several methods of providing auxiliary power. One possibility is to wire the facility with two independent utility power feeds from different power grids and different main generators. Then if one fails, the second is automatically switched over. Motor generator sets are often used to filter power in this case and provide "ride through" time during switch over from one utility to the other. Some users may even be able to contract with two independent utility power companies. This is an excellent solution, available to some users at little cost but to others only at substantial cost.

Another method is installing a backup engine generator (not to be confused with a motor generator). Diesel, gas and propane are the most popular types. NEMA standards require that engine generators be capable of starting and stabilizing under load in 10 secs. A minimum of 1 min. of backup time is recommended.

Finally, a battery energy storage system capable of providing power for extended periods of time can be installed. This is expensive, so it is done only when an engine generator backup is undesirable for some reason.

Orderly automatic system shutdown can take from seconds to minutes. Operators may request hours or days if they need to work through utility blackouts. The time necessary to provide uninterrupted power while an engine generator is starting or a system is being shut down is commonly called backup time. Using a 1 min. minimum backup time as the criterion for choosing a UPS system narrows the choices.

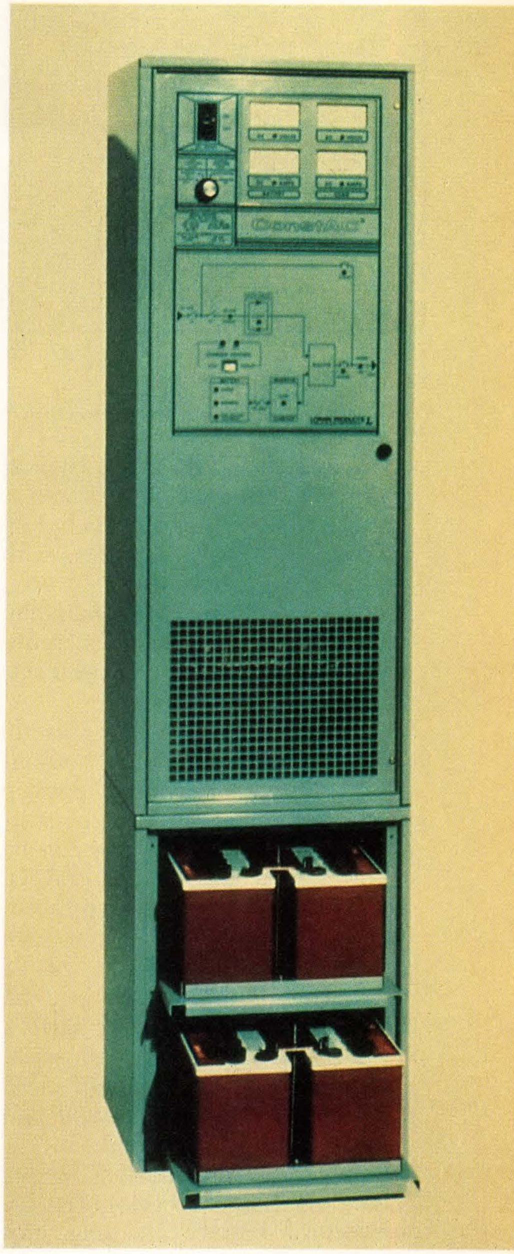


Figure 1: The 1 kVA Constac UPS from Lorain Products.

UPS Choices

At present, only two commonly available methods store enough energy for backup time over 1 min-

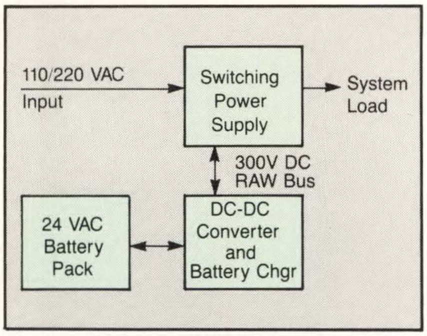


Figure 2: This "Hot-Standby" DUPS has a 5 min. backup time.

ute: batteries and flywheels (typical motor generator carryover time is 0.1 to 0.5 sec. if not augmented by a flywheel). Motor generators with flywheels capable of over 10 secs. have been built and are available, but are prone to mechanical problems. Therefore, battery-based systems are recommended.

Battery backup power is a useful tool in evaluating similar systems from different vendors. Backup power is a function of energy storage capacity and load, and can be expressed in kilowatt-hours (kWH), just as utility energy is expressed. For example, a 10 kW system with a maximum backup time of 15 mins. would have 10 kW × 0.25 hour or 2.5 kWH capacity. Such a system used on a 5 kW load would give backup time of 0.5 hour or 30 mins., ignoring the decreased efficiency with decreased load.

An important criterion in the choice of battery backup is the method of battery charging; this should be investigated carefully. The "recharge rate" determines the speed of recovery after battery discharge, and is usually expressed in hours or as a multiple of the backup time.

In addition to storing energy, most larger UPS systems isolate the load from utility power and provide clean, filtered power free of voltage transients, momentary interruptions, voltage dips and surges. It is important to note that every system requirement is different. Some loads only require isolation and filtering without energy storage. Others require backup times ranging from seconds to days or more.

Isolation and filtering can be obtained without the energy storage capability of a UPS system at substantially lower cost. Systems requiring hours or days of backup power might use an engine generator at a lower cost than battery banks. In that case, a 5 to 15 min. battery backup system would carry the load long enough to ensure stable engine generator output. Some systems may also benefit from power distribution centers which are available with or without filtering and isolation. System requirements must be defined prior to selecting the input power scheme.

An analysis of a typical load will serve to examine the ways to achieve battery backup. Nearly every electronic system takes high voltage Alternating Current provided by utility companies and converts it in two stages to low voltage Direct Current. An excellent example is the computer, since it can stand alone as a typical load, or it may be part of a larger system.

A simple computer could contain a CPU and a memory section requiring +5VDC to operate. It may also have a disk drive, needing +12VDC and a CRT display, requiring +24VDC. These voltages are produced by a "linear" or "switching" regulator power supply. The linear supply typically transforms the AC to low voltage "raw bus" DC (stage 1) and then regulates the raw bus through a linear regulator to a stable +5VDC (stage 2). The switching regulator supply typically multiplies the input AC to create a high voltage raw bus DC (stage 1). Then it uses high frequency pulse width modulation to regulate a +5VDC output (stage 2) (**Figure 3**).

The goal of an uninterruptible power supply is to prevent the system from losing power. The system, in this case, is the CPU and memory. Therefore, we have more than one place to store energy. In fact, the "bus filter capacitor" shown in both the linear and switching power supplies is commonly used by power supply designers to provide a small backup time known as *holdup time*. This holdup time is long compared to many AC power fluctuations. Most switching power supplies are designed for a minimum holdup time

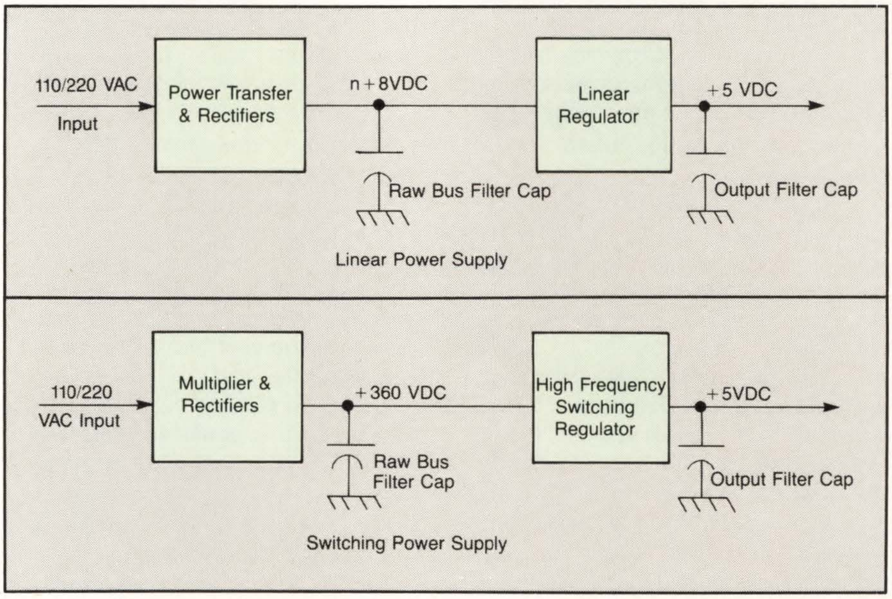
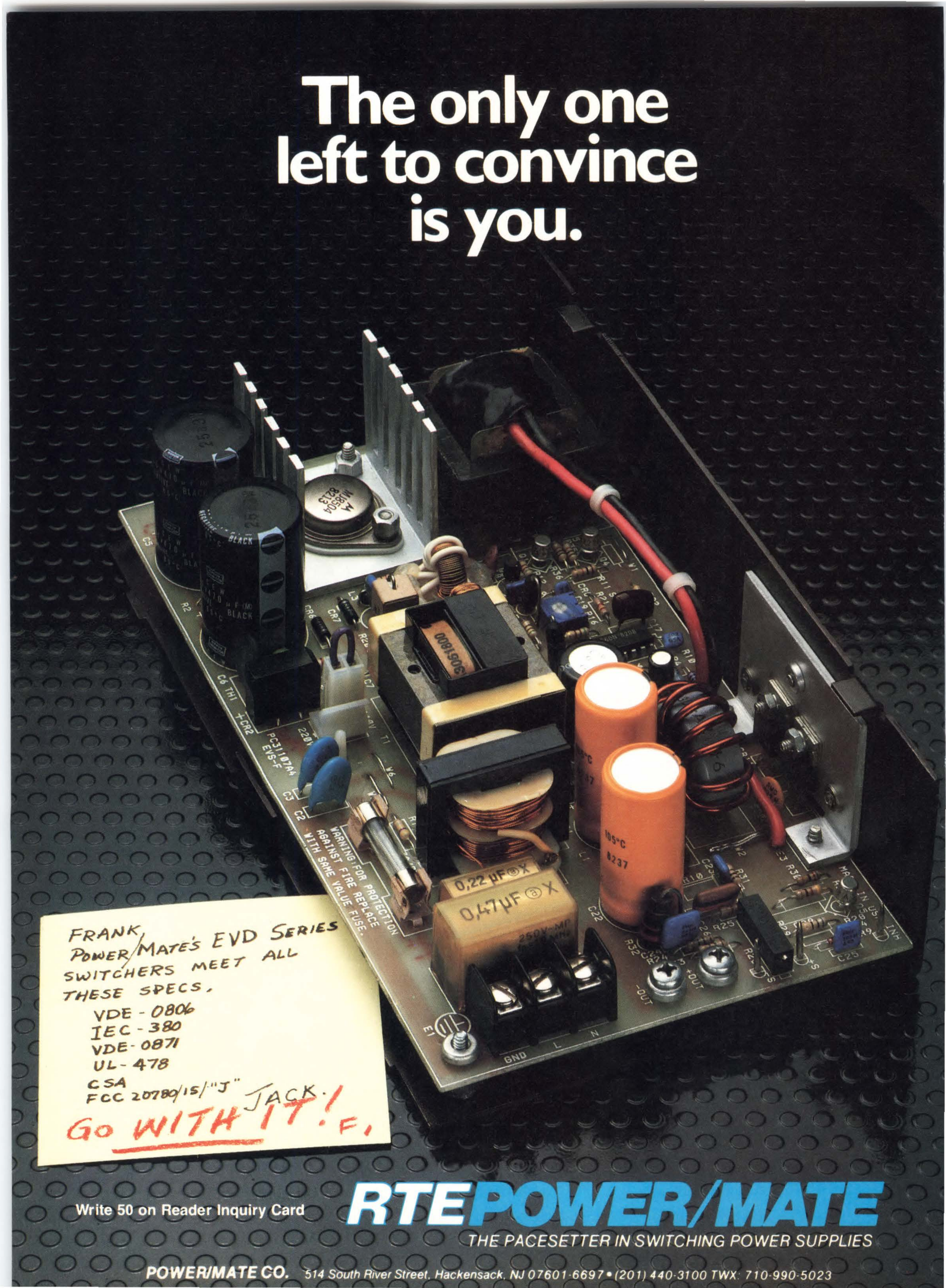


Figure 3: These typical power supply designs are suitable for systems up to about 15 kVA, single-phase.

of 16 msec. (1 cycle) under all conditions, with typical times of 32–48 msec. The time is determined by the storage capacity of the filter capacitor.

DUPS

The storage capacity of the filter capacitor together with a battery



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makes a Direct Current Uninterruptible Power Supply, or DUPS. The battery can connect to either the output (+5VDC) or to the raw bus. Digital Equipment Corporation's LSI-11 computer can accept a battery backup system made by Stevens-Arnold, (Boston, MA) that connects directly to the computer's +5VDC and +12VDC memory power bus to prevent memory loss during AC power failure. The UPS 2719 B has a backup time of 0.9 hour at full rated load (50 W DC output).

In systems using multiple output power supplies it is easiest to augment energy storage on the raw bus. This is especially convenient in a switching regulator design. A linear regulator may have a different raw bus voltage for each output, whereas a switcher has only one high voltage raw bus. Nearly all switchers utilize a 360VDC bus that can accept from 180 to 400VDC input in the case of AC failure. In fact, many switchers, like Todd Products' (Brentwood, NY) MOS series, will even accept DC input to their AC terminals, when wired for 220VAC input. The Todd units (in power outputs from 100 to 400W, 3 to 6 output voltages) are flexible enough to be powered by square wave output inverters with no degradation in operation.

Lorain Products' Business/Industrial Power Products Group (Lorain, OH) has a new line of 150W and 300W enclosed switching power supplies that are part of a "Companion" series (**Figure 6**). They have an optional 24VDC battery pack and a DC to DC converter which connects the switcher's 300V raw bus through a terminal strip. The converter module contains a battery charger. The batteries provide 5 min. of backup time under full output load and may be paralleled for more time. Recharge time is approximately 8 hours for one battery pack. This is a pure "hot standby" DUPS—the 300VDC bus is always connected to both the converter and to its own AC-DC rectifiers. Loss of AC power simply stops driving current through the power supply's input rectifiers and current is drawn from the DC-DC converter and battery. Charging is done off the 300VDC bus when it is up to voltage.

As these examples illustrate, it may be worthwhile for the system designer to plan ahead for battery backup at the DC level. Many small computer manufacturers have already done that, and some provide connectors for battery systems to be added by the user. This provides a simple, efficient method of providing backup time in the case of AC power failure.

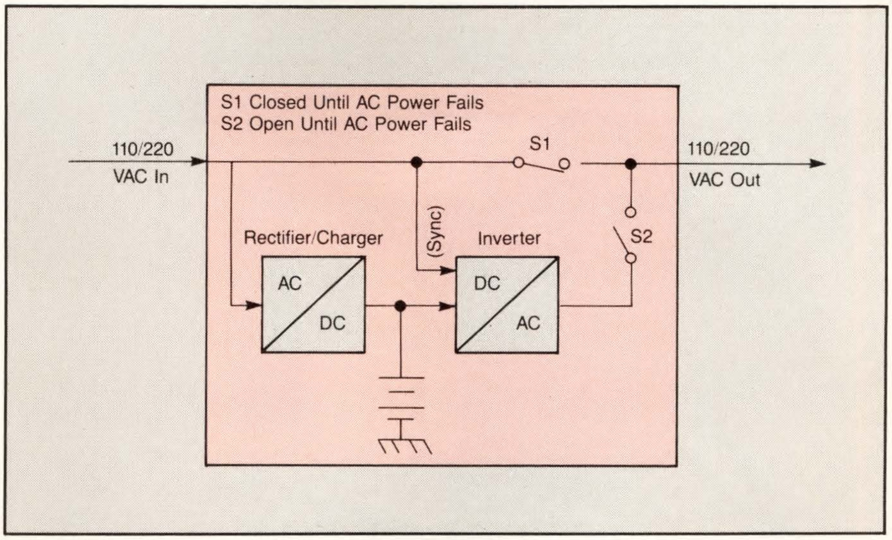

Figure 4: SUPS—Forward transfer is common in systems >1 kVA.

SUPS

For those cases where DUPS are not the answer due to frozen designs or multiple AC loads, a power system that generates AC becomes a necessity. Creating AC from DC is the task that has spawned the most methods, products, and companies. There are basically two accepted methods, *motor generators*, and *static inverters*. Generators are so obvious that they are often ignored. "Static" is used to describe any non-rotating method (non-dynamic).

Motor generators are firmly entrenched in certain industries, most notably those using very large 415 Hz loads such as IBM, Cray, and Amdahl computers. Energy storage in the past has been scarce (limited to flywheels) and the sytems were noisy, but they offer excellent isolation and filtering.

Static UPS systems (SUPS) were

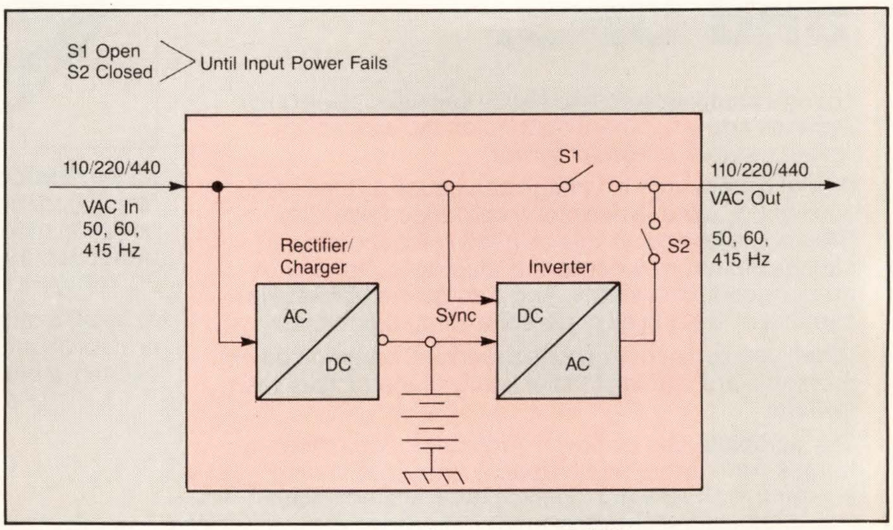

Figure 5: SUPS—Reverse transfer is used in systems <1 kVA.

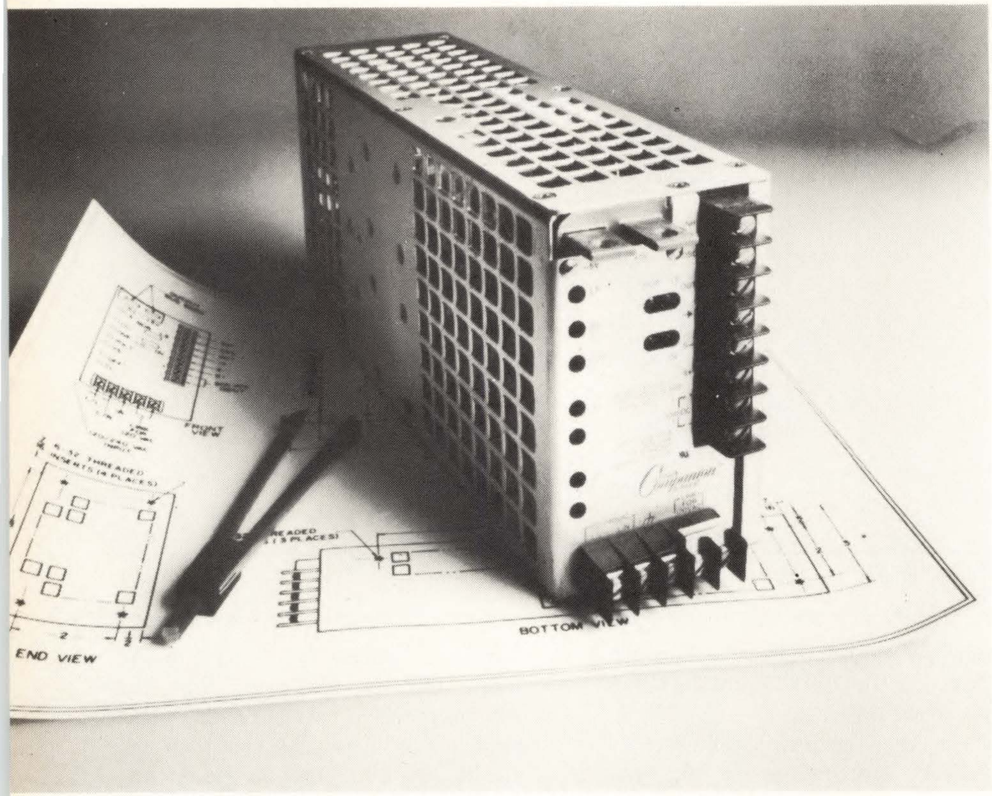

Figure 6: Lorain Products' Companion 150W power switcher.

developed to satisfy the need for battery energy storage, and offered isolation and filtering in the same unit. Recently, however, MG sets have started to challenge the SUPS for market acceptance due to developments in inverter technology, motor and generator technology and motor speed control technology. To understand why, a look at SUPS is helpful.

The SUPS basically converts input AC to DC and charges an energy storage battery or batteries, then converts the battery DC back to AC through an "inverter" when the utility AC power fails. There are many ways to build the DC to AC inverter and there are many ways to connect a SUPS between the AC line input and the system load (**Figures 3 and 4**).

Inverter design application notes are plentiful and available from nearly every SUPS manufacturer. Every manufacturer has a reason for their choice of designs, which they and their literature will explain in detail. In general, important considerations are:

Sine wave output vs. non-sine wave output. Most large (> 1 kVA) systems are sine wave output. Many small systems have pure square waves or modified square waves. Non-sine waves are less expensive to generate, but some loads are sensitive to the harmonic power content. Though most switching power supplies don't care, some linears with marginal input power transformers might overheat with non-sine wave input. Fan motors are relatively insensitive to all but pure square waves.

Frequency stability. Loads may or may not be sensitive to frequency stability. For example, switching power supplies typically don't care, but some CRT displays demand 60 Hz ±0.01%.

Efficiency. This is one of the most controversial factors, since efficiency is a major consideration in most larger systems. With smaller SUPS (< 1 kVA), it is usually unimportant, since the SUPS is used only when AC power fails. But in larger systems the SUPS is continuously running and supplying all AC power. At 200 kVA, for example, a 5% difference in *overall* efficiency can cost $10,000 a year (at 10¢/kWH).

Ability to handle overloads. Most SUPS can take 125% overloads for minutes, and 150% for seconds, but higher overloads require switching over to the unfiltered utility power until the overload surge subsides. Motor generators have much

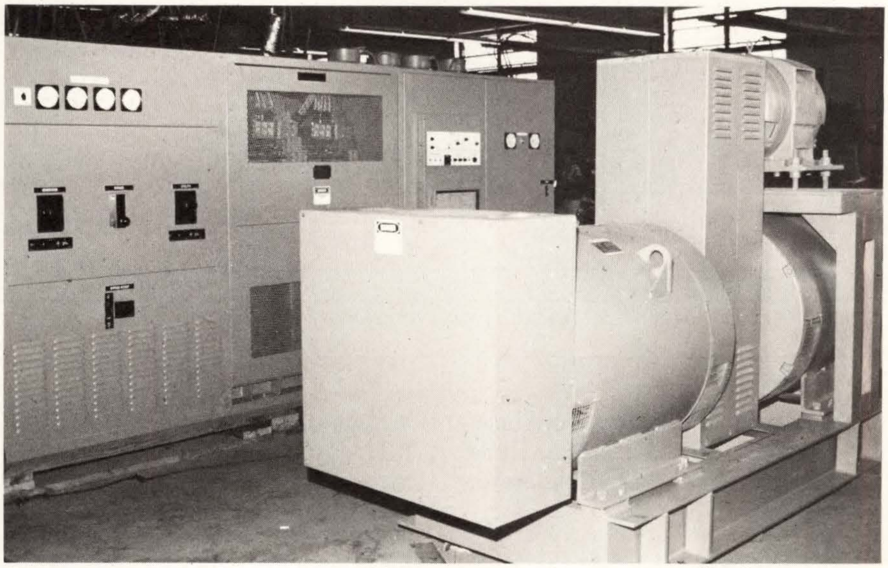

Figure 7: PSC's HUPS provides 400kW with motor bypass plus utility bypass.

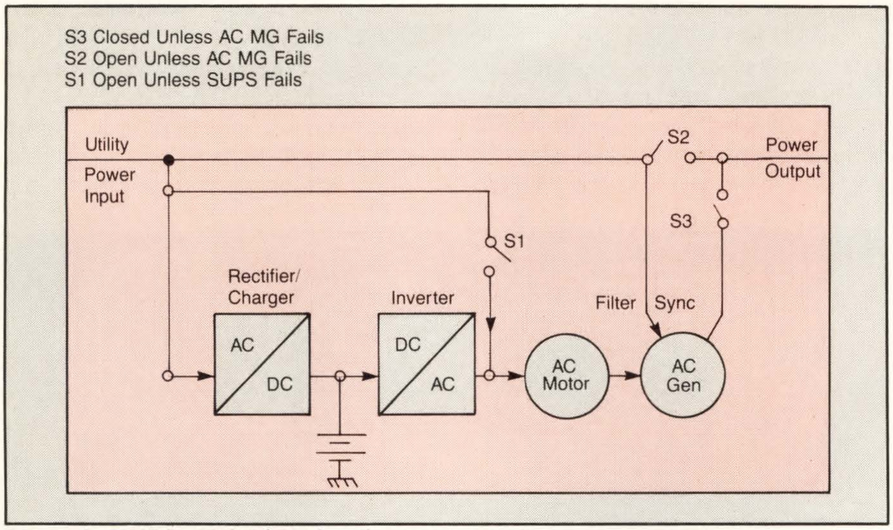

Figure 8: HUPS—Hybrid UPS with reverse transfer.

higher overload capacity. Conversely, most SUPS have faster load transient recovery times than motor generators.

SUPS vs. MG

SUPS have been providing the majority of uninterruptible power for years. With new technology, motor generators have been improved, however, and are no longer noisy or very hard to control. Motor generator (MG) sets have some significant operational differences from SUPS that make them a potential alternative to SUPS at power levels above 10 kVA. Some differences are obvious, others subtle.

- Motor technology has different MTBFs and MTTRs than semiconductor technology. MG MBTF is longer, but MTTR can be longer than some SUPS.
- The output impedence of a generator may be higher, which can result in larger voltage fluctuations in sytems with widely fluctuating current loads.
- MG load response time is slower than SUPS, and the designer must be sure either or both are compatible with the expected system operation.
- Most data shows that MG sets can operate more efficiently than SUPS at outputs of 70% or less of rated capacity. Efficiency of MG sets > 50 kVA is very nearly the same as SUPS above 70% of rated capacity.
- Regarding lightning protection, MG sets are more tolerant of super high voltage spikes on the input, and the isolation from motor to generator is 3–10 in. of air. In addition, most MG 3-phase systems can continue to operate after loss of one of the 3 phases.

The advantages of MG sets in certain applications have resulted in some new developments in Uninterruptible Power Systems. The combination of SUPS and MG sets into a "Hybrid UPS" (HUPS) and the use of a DC motor to create a "Rotary UPS" (RUPS) are notable examples.

HUPS

The HUPS (**Figure 7**) is described in detail in an application note by John Kammeter, VP of Engineering at Power Systems and Controls (PSC, Richmond, VA). It is, fundamentally, a SUPS with an MG set as its output filter, instead of the standard SUPS filter. The HUPS gives motor generator technology the benefit of battery energy storage for long backup time. In addition, the MG set continues to filter utility power in the event of failure of the SUPS section (**Figure 8**).

Teledyne Inet (Torrance, CA) is, like PSC, a manufacturer with experience in both SUPS and MG sets. "The emergence of user demand for HUPS has caused us to go to the drawing boards to develop our own system, scheduled to be introduced later this year," says Fred Tamjidi, Power Conditioning Product Manager for Computer Applications. Teledyne Inet builds SUPS from 75 to 500 kVA (single module) and MG sets from 25 to 375 kVA. These can be paralleled to achieve 3000 kVA only by the difficulty of getting transfer breakers above that power level.

RUPS

The RUPS (**Figure 9**) is a trademark name of Computer Power Products Division of Sweinhart Electric (CPP, Los Angeles, CA).

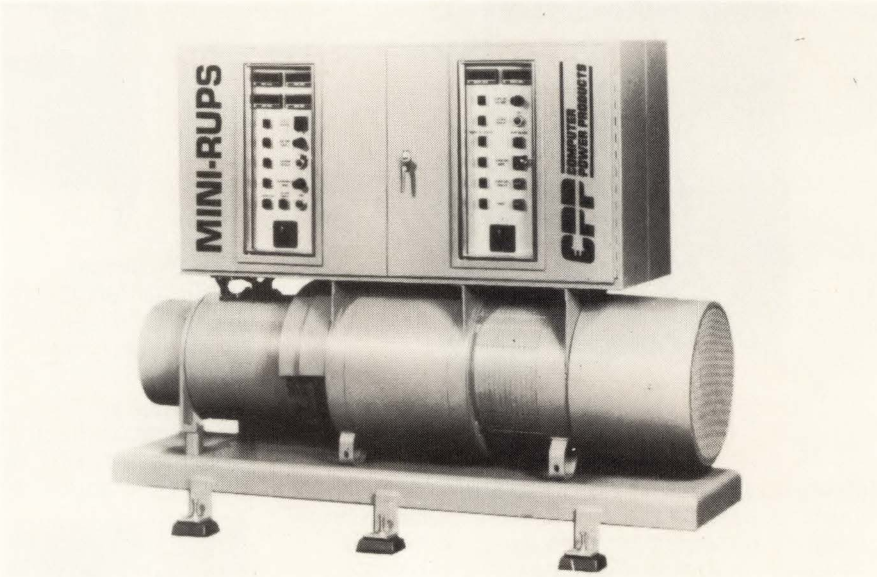

Figure 9: CPP's RUPS is suitable for minicomputers in the 12 kVA to 50 kVA range.

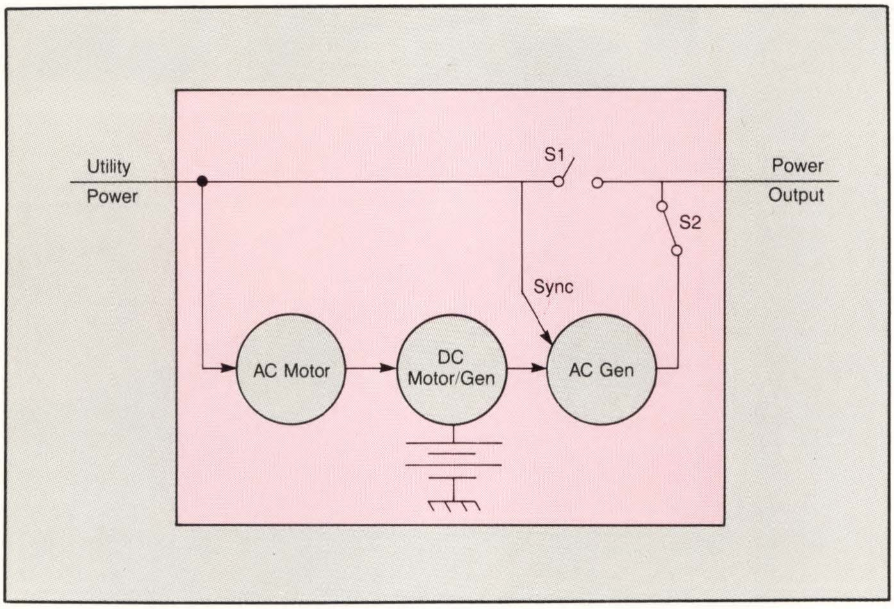

Figure 10: RUPS—Rotating UPS with reverse transfer.

After trying the HUPS approach in 1981, Richard Bowyer, VP of Marketing, revived an old idea using modern DC motor control technology to create a totally Rotating Uninterruptible Power Supply. CPP uses an AC motor to drive a shaft on which a DC motor generator and an AC generator are mounted. During normal utility power, the DC MG becomes a motor, continuing to drive the AC generator with no effect on the load (**Figure 10**). Regarding the reliability of this system, Mr. Bowyer says, "CPP has 40 years experience with rotating components used in this system, through our association with Robert Sweinhart. We are confident that we can meet or exceed the overall reliability of any other system on the market at a competitive price."

UPS Outlook

Providing uninterruptible power has many variables. The common thread is battery energy storage. DUPS should become more popular due to high efficiency and lower costs. HUPS and RUPS have potential, but the market is still clearly dominated by SUPS.

UPS Selection Guide

Key: **SUPS**—Static Uninterruptible Power Supply; **HUPS**—Hybrid UPS; **RUPS**—Rotating UPS; **DUPS**—Direct Current UPS; **MG Sets**—Motor Generator Sets

SUPS Company	Single-Phase Output Power Range (KVA)	Three Phase Output Power Range (KVA)
Abacus	1–10 50Hz 60Hz 400Hz	1.6–10 50Hz 60Hz 400Hz
Advance Conversion	.04–5 50/60	
ATR	.3–.7 110V, 60Hz	
Behlman	.1–5 50/60Hz	.3–15 50/60Hz
Clary	.75–10 50/60 Hz	.75–10 50/60Hz
CML Macarr	.1–.5 115V, 60Hz	
Compumart	.9–2.0 110V, 60Hz	
Computer Power, Inc.	.250–12.5 50/60Hz	.250–12.5 50/60Hz
Cuesta Systems	.09–.2 120/240, 50/60Hz	
Cyberex	2–100 50/60Hz	2–1500 50/60Hz
Elgar	.4–20 50/60Hz	5–45 50/60Hz
Emerson		20–3000 50/60Hz 60–750 415Hz
Exide		15-300 50/60Hz 80 415Hz
General Power Systems	.09–10 50/60Hz	15–35 60Hz only

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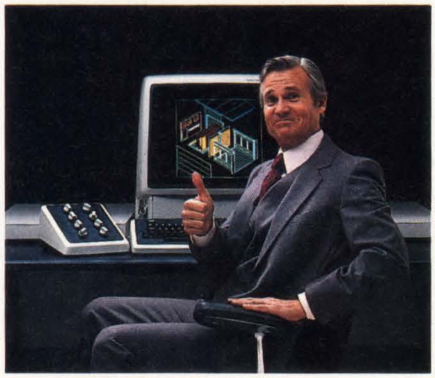

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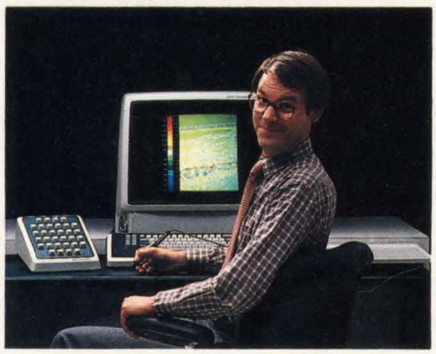

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Company	Single-Phase Output Power Range (KVA)	Three Phase Output Power Range (KVA)
Gould	.5–20 50/60Hz	15–45 50/60Hz
Hitran	1–15 50/60Hz	6–45 50/60Hz
HDR Power Instrumentation & Control Systems	1–60 50/60Hz .2–20 50/60Hz	15–100 50/60Hz
International Power Machine	20–400 50/60/415Hz	20–2000 50/60/415Hz
La Marche	.5–3 50/60Hz	2–5 50/60Hz
Liebert		50–1600 50/60Hz 75–150 415Hz
Lorain	1–10 50/60Hz	
Lortec	2–10 50/60Hz	2–156 50/60Hz
Nova	.2–3 120V 60Hz	
Power Mark	.1–.3 120V 60Hz	
Professional Systems Inc.		
Ratelco	1–15 50/60Hz	
RH Electronics	.150 115/220 50/60Hz	
RKS Industries	.2–.4	
Saft America	.2–.4 110/220 50/60Hz	
Sawyer Div. Ametek	.5–1 110V/60Hz	
Sola	.07–15 50/60Hz	1.5–15 50/60Hz
Solid State Controls	.5–20 50/60Hz	1–200 50/60Hz
Sun Research	.15–1 50/60Hz 120/240	
Tab	2–3 50/60Hz	
Teledyne Inet		75–3000 50/60/415Hz
Terado	.2–2 120V 60Hz	
TII	.2–.75 120V 60Hz	
Topaz	.5–15 50/60Hz	7.5–15 50/60Hz
UP Systems	2.5–10	15–50
Warren Communications	.5–10 50/60Hz	
Wilmore	.25–1 50/60Hz	

HUPS Company	Single-Phase Output Power Range (KVA)	Three Phase Output Power Range (KVA)
Emergency Power Engineering	5–50	5–225
Power Systems & Controls		30–313 @ 50, 60Hz 50–75 @ 415Hz
Teledyne Inet		100 @ 50, 60Hz (preliminary)

RUPS Company	Single-Phase Output Power Range (KVA)	Three Phase Output Power Range (KVA)
Computer Power Products	50Hz 12–50 60Hz 415Hz	50Hz 12–300 60Hz 415Hz

MGSets Company	Single Phase Output Power Range (KVA)	Three Phase Output Power Range (KVA)
American Electronics		5–200 @ 415Hz only
Atlas	50Hz 10–50 60Hz 415Hz	50Hz 10–750 60Hz 415Hz
Computer Power Products		10–40
Georater	.15–50, 60Hz .25–5.0 415Hz	.15–25 50/60Hz .5–25 415Hz
Horlick	3–50 50/60Hz	3–500 50/60Hz 3–300 415Hz
Power Systems & Controls		50–75 @ 415Hz 50–1000 @ 50,60Hz
Teledyne Inet		25–3000 50,60, 415Hz

DUPS Company	Single Phase (or DC for DUPS)	Three Phase Output Power Range (KVA)
Beaver Labs	.100	
Converter Concepts	.025–.075	
Lorain	.150–.300	
Semiconductor Circuits	.050–.150	
Stevens Arnold	.100	

UPS Manufacturers' Listing

To obtain more information on the following UPS manufacturers, write in the appropriate Write Number on the *Digital Design* reader inquiry card.

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Advance Conversion Devices Co.
Passaic, NJ
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American Electronics Inc.
Fullerton, CA
Write 407

Arnold Magnetics
Culver City, CA
Write 408

Atlas Energy Systems
S. El Monte, CA
Write 409

ATR Electronics
St. Paul, MN
Write 410

Avionic Instruments
Rahway, NJ
Write 411

Beaver Labs
Framingham, MA
Write 412

Behlman Engineering Corp.
Carpinteria, CA
Write 413

Bikor Corp.
Torrance, CA
Write 414

Clary Corp.
San Gabriel, CA
Write 415

CML Macarr
Brooklyn, NY
Write 416

Compumart Corp.
Memphis, TN
Write 417

Computer Power Inc.
High Bridge, NJ
Write 418

Computer Power Products
Gardena, CA
Write 419

Converter Concepts Inc.
Pardeeville, WI
Write 420

Cuesta Systems
San Luis Obispo, CA
Write 421

Cyberex, Inc.
Mentor, OH
Write 422

Elgar
San Diego, CA
Write 423

Emergency Power Engineering
Costa Mesa, CA
Write 424

Emerson Inc. Controls
Santa Ana, CA
Write 425

Exide Electronics
Philadelphia, PA
Write 426

General Power Systems
Anaheim, CA
Write 427

Gould, Inc.
San Diego, CA
Write 428

Georater Corp.
Manassas, VA
Write 429

Hitron
Flemington, NJ
Write 430

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Instrumentation & Control Systems
Addison, IL
Write 431

International Power Machines
Mesquite, TX
Write 432

La Marche Mfg. Co.
Des Plaines, IL
Write 433

Liebert Corp.
Sunnyvale, CA
Write 434

Lorain Products
Lorain, OH
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Nova Electric Mfg. Co.
Nutley, NJ
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PowerMark
San Diego, CA
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Power Systems & Controls
Richmond, VA
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Professional Systems, Inc.
Waukesha, WI
Write 439

Ratelco, Inc.
Seattle, WA
Write 440

RH Electronics, Inc.
Buellton, CA
Write 441

RKS Industries, Inc.
Scotts Valley, CA
Write 442

Saft America, Inc.
St. Paul, MN
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Sawyer Industries, Inc.
Arcadia, CA
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Semiconductor Circuits, Inc.
Windham, NH
Write 445

Sola Electric
Elk Grove Village, IL
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Solid State Controls, Inc.
Columbus, OH
Write 447

Stevens-Arnold
South Boston, MA
Write 448

Sun Research
New Durham, NH
Write 449

Tab Products Co.
Palo Alto, CA
Write 450

Technipower
Danbury, CT
Write 451

Teledyne Inet
Torrance, CA
Write 452

Terado Corp.
St. Paul, MN
Write 453

TII Industries, Inc.
Copiague, NY
Write 454

Topaz
Los Angeles, CA
Write 455

UPS Systems
Paramount, CA
Write 456

Warren Communications
Livingston, NJ
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Wilmore Electronics Co., Inc.
Hillsborough, NC
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FPU Provides Video Graphics Versatility

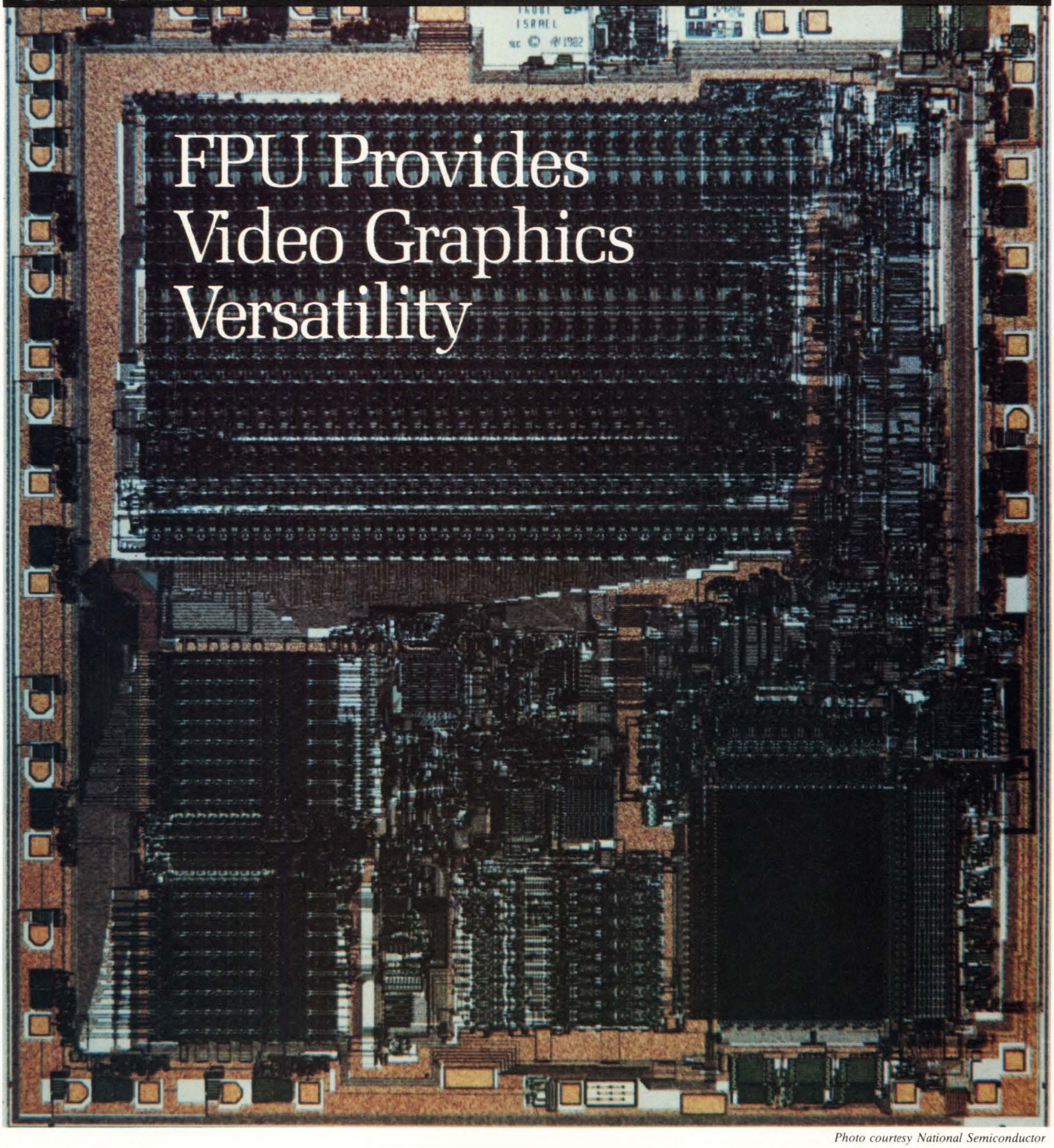

Photo courtesy National Semiconductor

by Subhash Ball

The 16081 may be used as either a support peripheral in a μP based system or a slave processor to ease the burden of both CPU and designer.

Today's video graphics systems need number-crunching powers that are often beyond the limits of the fixed-point processing capabilities of μPs.

To obtain the higher computation speeds necessary to increase product performance, designers and integrators of video graphics systems can switch from fixed-point computation to floating-point processing. By representing numbers as a mantissa and an exponent, a floating-point processing unit (FPU) can operate rapidly on both extremely

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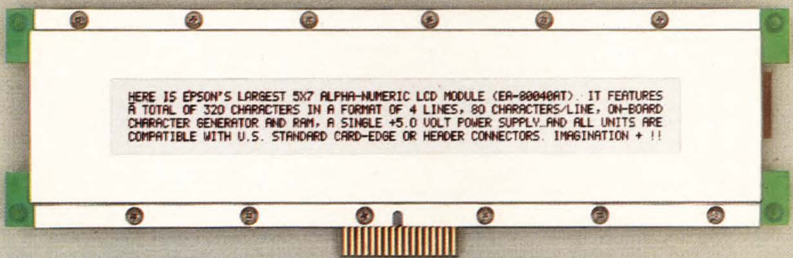
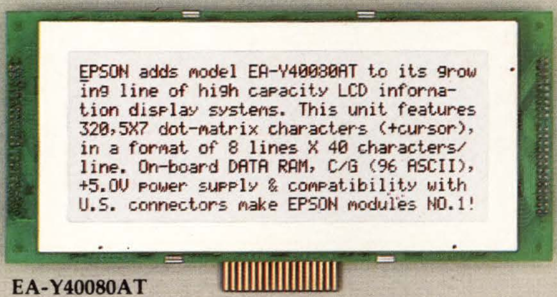


EA-Y80040AT



EA-Y40080AT

EA-Y40040AT

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- Backlighting possible with EL panel

Applications

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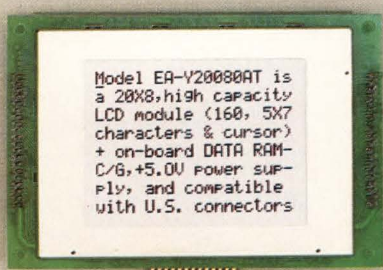
- Computer Terminals
- Word Processors/Typewriters
- POS Terminals
- Instrumentation
- Telecommunications
- Games/Toys

EG-Y84320AT



EA-Y20080AT

EA SERIES

Model Number	Character Format (characters × lines)	Character Size (with cursor)	Effective Viewing Area	Module Size (W × H × D)
EA-Y16015AZ	16 × 1	2.9 × 4.8 (6.2)	62 × 20	84 × 44 × 14.2
EA-Y16025AZ	16 × 2	2.9 × 4.1 (5.3)	62 × 20	84 × 44 × 14.2
EA-Y20015AZ	20 × 1	3.4 × 5.15 (6.65)	88.2 × 20	125 × 44 × 14.2
EA-Y20025AZ	20 × 2	3.4 × 5.15 (6.65)	88.2 × 20	125 × 44 × 14.2
EA-Y20080AT	20 × 8	3.0 × 4.8 (6.2)	84 × 64	140 × 95 × 19.2
EA-Y24015AZ	24 × 1	2.9 × 4.45 (5.75)	93 × 20	125 × 44 × 14.2
EA-Y40015AT	40 × 1	3.0 × 4.8 (6.2)	156 × 20	192 × 45 × 14.2
EA-Y40025AT	40 × 2	3.0 × 4.8 (6.2)	156 × 20	192 × 45 × 14.2
EA-Y40040AT	40 × 4	3.0 × 4.8 (6.2)	156 × 34	200 × 71 × 25.4
EA-Y40080AT	40 × 8	3.0 × 4.8 (6.2)	157 × 63	205 × 93 × 19.2
EA-Y80015AT	80 × 1	2.1 × 3.38 (4.32)	212 × 18	264 × 53 × 20.7
EA-Y80025AT	80 × 2	2.1 × 3.38 (4.32)	212 × 18	264 × 53 × 20.7
EA-Y80040AT	80 × 4	2.1 × 3.38 (4.32)	212 × 28	293 × 80 × 31.0

EG SERIES

Model Number	Dot Format (column × row)	Dot Size	Effective Viewing Area	Module Size (W × H × D)
EG-Y84320AT	84 × 32	0.75 × 0.75	76.3 × 33	132 × 60 × 15.7

Unit: mm

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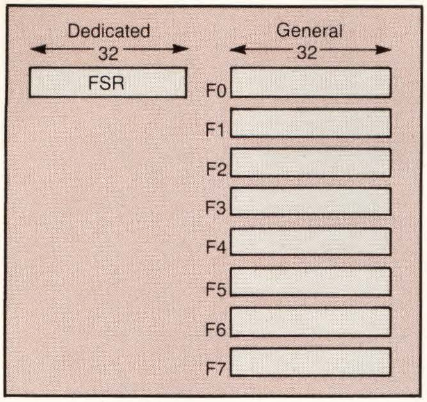


Figure 1: NS16081 register set layout.

large and extremely small numbers and yield well-behaved results. If designed properly, an FPU should be transparent to the user.

In graphics applications, common on-screen object manipulations can be annoyingly slow if done in fixed point. Each rotation, translation, or scaling requires a CPU to perform matrix transformations on hundreds of points, involving thousands of multiplication operations taking an average of 15 to 20 μsecs each. As an alternative, the National Semiconductor NS16081 FPU performs a 32-bit multiply in 4.8 μsecs.

A designer can add an FPU to a system that models and displays illuminated objects. Such a system must calculate the light intensity for each point on the surface of an object. If the object is modeled as a collection of small planar surfaces, the light intensity of each plane is found by performing a dot-product operation, which requires multiplying three numbers. Such an operation takes only 14.4 μsecs with the NS 16081 floating point unit, but could take between 40 and 45 μsecs with the fixed-point capabilities of a CPU alone. Considering that it takes many hundreds of these operations to formulate and display an illuminated object and that a user might also want to rotate or move this object on the screen, an FPU is an advantageous design addition.

Besides performing speedy arithmetic operations, an FPU is also capable of processing variables that have a wide dynamic range. Necessary in many graphics applications, a large dynamic range may not be accommodated in even 32-bit minicomputers. Workstations which simulate and display circuit designs, for example, must be able to process variables ranging from femtofarads capacitance to megohms resistance and physical dimensions ranging from microns to feet. Fixed point round-off errors are significant in such a system.

Floating-point processors can extend a computer's range of operands exponentially. In the case of the NS16081 FPU, close to 10^{800} different numbers can be manipulated, while a 32-bit computer is restricted to 10^{10} discrete numbers.

When performing rapid arithmetic operations on variables with a large dynamic range, a floating-point unit used in conjunction with a μP can enhance product performance in such applications as CAD integrated circuit layout, space flight simulation, and X-ray image enhancement.

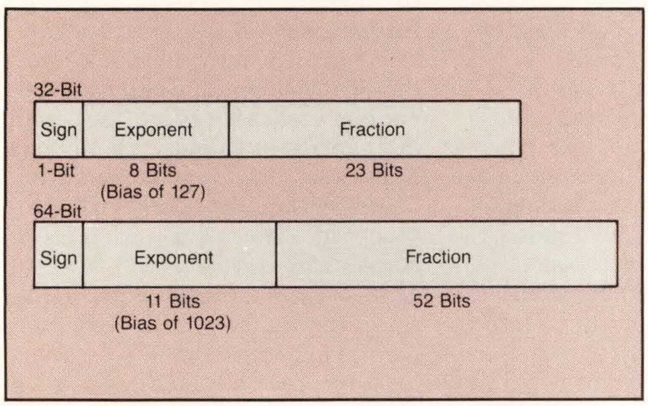
Choosing An FPU

When considering which floating point unit to buy, a video graphics system designer should be aware of the complex nature of the device. FPUs sometimes require even more gates (and therefore more chip space) than CPUs themselves. With today's technology, designing the FPU directly onto a CPU chip not only places a burden on the chip designer, but sometimes compromises circuit design, leading to inefficient data paths and slower processing speeds. And for the OEM who might not require an FPU capability, an FPU-integrated CPU design would be an unwarranted expense that would have to be passed on to the user.

Floating-Point Processing

Factors that must be considered when designing an FPU into a system include the handling of specific operations or instructions, the length of actual data (operands) permitted, the amount of support that the FPU subsystem can expect from the rest of the μP system, and the throughput schemes designed to enhance data communicated to and from the chip.

The NS16000 family has been designed to fully support 32-bit and 64-bit precision floating-point calculations (as well as 8-bit, 16-bit, and 32-bit fixed-point calculations) through its NS16081 FPU. The NS16081 itself contains 9 on-board, 32-bit registers (8 general purpose, 1 dedicated to FPU status), which may be used to provide either a single-precision (32 bit) or double-precision (64 bit) number (**Figure 1**). Double-precision operands imply both greater range (larger expo-



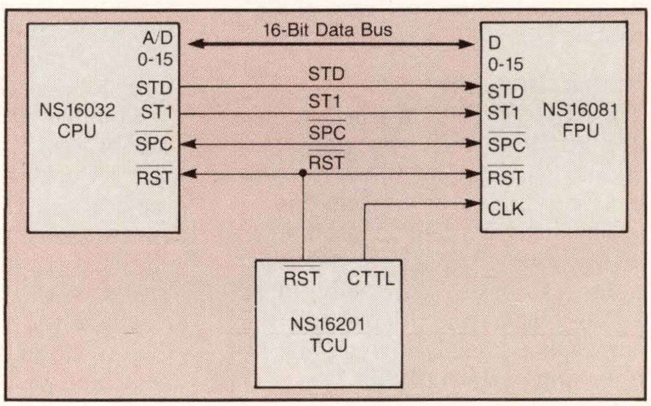


Figure 2: Floating point format and FPU system implementation.

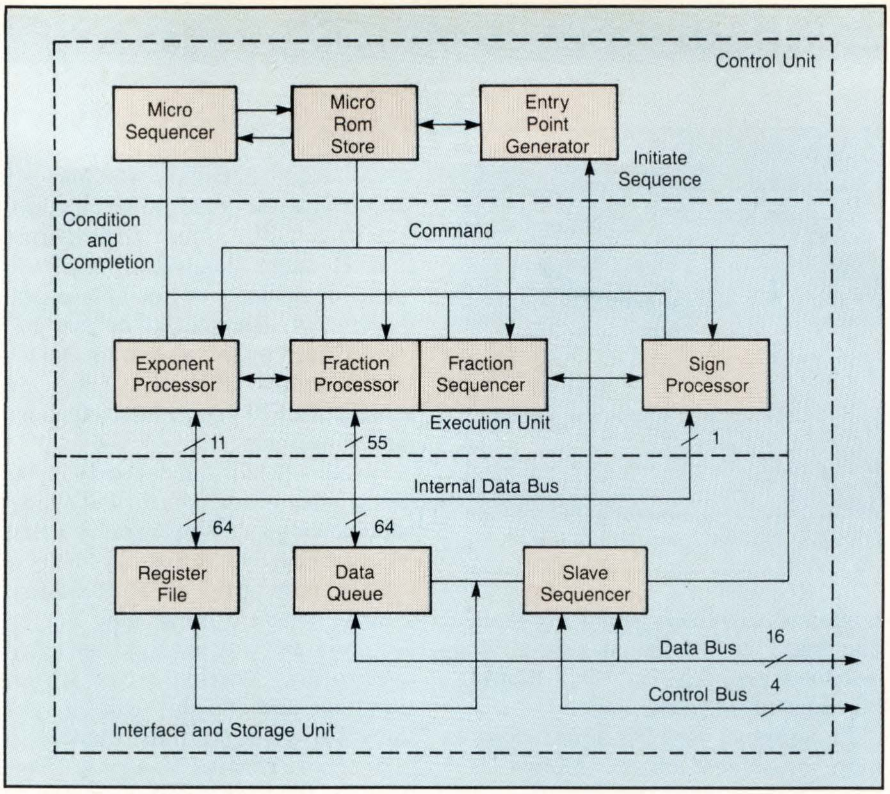


Figure 3: NS16081 FPU block diagram.

- **Add/Subtract/Multiply/Divide**—Hardware-programmed for two 32-bit or 64-bit operands.
- **Compare**—After comparing the magnitudes of two operands, the FPU posts the result in a CPU register.
- **Negate**—After complementing the sign of an FP source, the result is moved to a specified location.
- **Absolute**—Clears the sign of an FP source, then moves the result to a specified location.
- **Store/Load Status Register**—Transfers a double word between a specified location and the status register.
- **Floor/Trunc/Round**—These instructions allow floating-point-to-integer conversion; "floor" rounds toward minus infinity, "trunc" toward zero, and "round" to the nearest integer.
- **Move and Convert**—Integer-to-floating-point and floating-point-to-floating-point conversion.
- **Move**—This instruction transfers floating-point values without conversion.

Table 1: The FPU contains a total of 15 instructions.

nent) and higher precision (larger mantissa or fraction). This is accomplished by a joining (concatenation) of two 32-bit single-precision operands.

While the 8 general-purpose registers are reserved for actual data, the status register is used to hold both control and error information. *Control* options include enabling CPU traps and FPU errors, and setting the operand rounding mode, specified as: Round to nearest; Round towards zero; Round towards +infinity; Round towards −infinity.

Error conditions provided by the status register include traps for overflow, underflow, illegal division (divide by zero), illegal instruction and operation, inexact result, and reserved operand (all-zero or all-one exponent). All traps can be individually enabled or disabled by the programmer.

The NSC16000 architecture makes available to the FPU all system addressing modes, a feature essential for efficient data handling. For example, in a "scaled-index" mode, a large array of floating-point data elements may be addressed by its logical index rather than by its physical address. This not only facilitates finding the data (with the help of the CPU), but eliminates wasting time with unnecessary programming schemes.

Used in conjunction with the NS16082 MMU to simplify large-memory management and data retrieval, the full 16 Mbytes of virtual memory becomes available for data storage by each user, and all of the data-retrieval, dynamic-address, and memory-protection capability of the MMU becomes part of FPU routines.

Instruction Set

The NS16081 FPU instruction set is compatible with the proposed IEEE floating-point standard, without restricting user applications.

The FPU contains a total of 15 instructions that perform such functions as basic arithmetic operations, single- and double-precision conversions, and integer/floating-point conversions (**Table 1**).

Operations that a user may wish to incorporate in addition to the FPU may be added as software. This eliminates from firmware the costly and unnecessary IEEE functions that a user may not wish to carry out, but provides an easy way of supplementing the FPU to conform to a specific application.

To enhance FPU speeds, a separate processor (total of three) operates on each of the three principal segments of a number residing in either a 32-bit or 64-bit register—all under control of microcode. The first segment (containing 1 bit) is reserved for the sign, the second segment (8 or 11 bits) for the exponent, and the third segment (23 or 52 bits), the fraction or mantissa (**Figure 2**).

For quicker processing, all instructions can be made from register to register, register to memory, or memory to memory. This last feature—known as "two-address" capability—is only available with the NS16000 family. Because an operation can be carried out with both values in memory, eliminating transfer of one or both to an on-board register, processing may proceed with fewer steps, using fewer codes. This is particularly advantageous when dealing with HLL, since they almost exlusively perform memory-to-memory operations, rarely using on-chip registers. □

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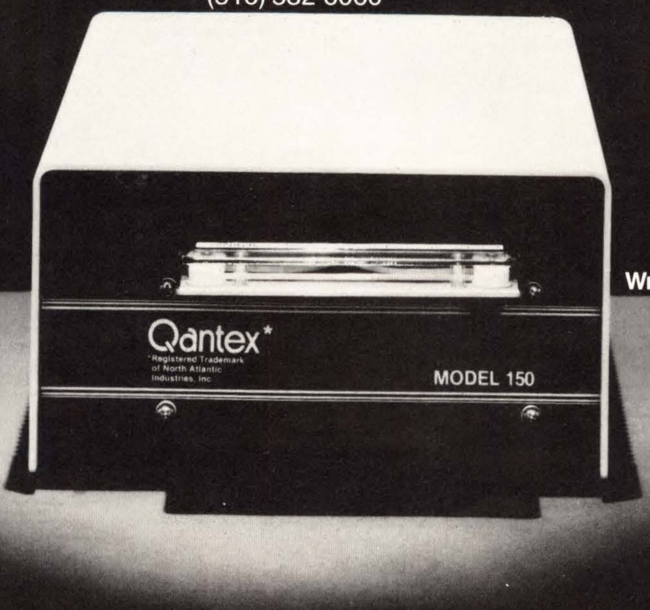


Write 62 on Reader Inquiry Card

Programmable Controllers Join Forces With Networks

By Dave Wilson

The programmable controller (PC) industry has grown at a phenomenal rate from its beginnings in 1970 to approximately $800 million worldwide today. According to William Schneider, VP Marketing and Strategy for ISSC (York, PA) this growth has caused the haphazard introduction of products with little relationship to or compatibility with one another.

Networks provide the solution to incompatibility between PCs, robotics controllers, and terminals.

One of the key reasons for the dramatic growth of the PC industry was its acceptance by non-computer personnel. The PC was the first computer packaged and programmed with the control engineer and maintenance man in mind—it was easy to understand, reliable and easy to repair.

As the industry grew, users requested additional functions and capabilities. The problem is that the industry lost touch with the people who must apply and maintain the products. Programming became more difficult, incompatibilities of software and hardware developed, and the products became so complex that identification and repair of PC problems became extremely difficult. These problems of incompatibility are now being addressed by the giant factory automation suppliers such as Westinghouse, and other smaller companies.

System Solutions

Although the larger companies are promoting total system solutions to the 'factory of the future' and can offer a wide range of products to meet the users' needs, they appear to have recognized that many manufacturing plants will avoid single sourcing capital equipment. Other plants may already have a good deal of capital investment tied up in existing equipment that must be 'integrated into' and not 'replaced by' a single company's grand plan.

Furthermore, in any industry, it is obvious that one supplier's products and services can never exactly meet the need for a specific application.

Networks

The solution to the incompatibility problem encountered between different PCs, robotics controllers, terminals, etc., has come in the form of networking systems. As Kevin Hughes of General Motors stated in the recent PC conference in Detroit, incompatibility results when a facility uses computers from different vendors. This situation demonstrates the need for establishing viable standards within manufacturing. Just as important, wide vendor support of such standards with cost-effective and compatible data communication products is required.

Plant managers need complete and timely information to make effective product decisions. This is only possible if PCs and other programmable devices are linked together in a system that can communicate with management information systems and decision support systems. In this way an operation can be monitored for maximum productivity.

Westnet

On March 8th, Westinghouse Electric introduced a new programmable controller data highway that integrates both industrial and process controls. The Westnet provides the user with the capability of interfacing Westinghouse programmable controllers and program loaders,

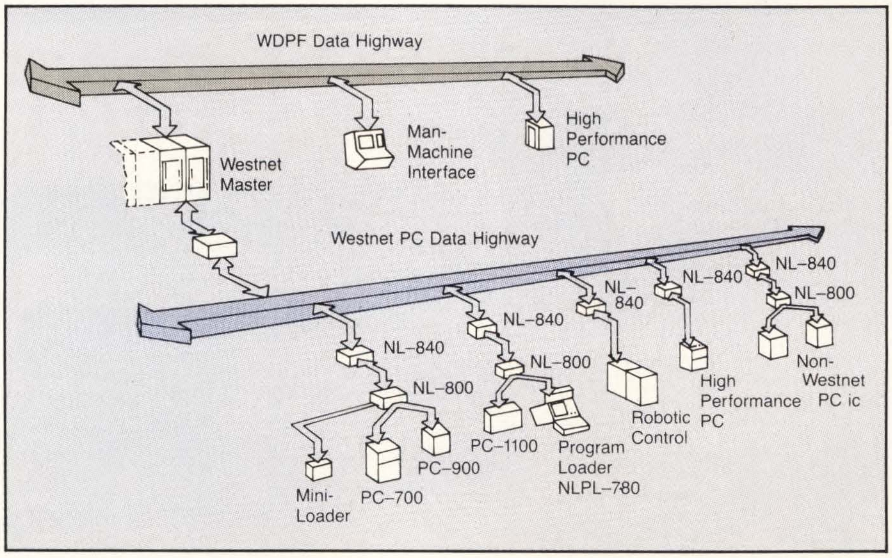


Figure 1: Westnet PC Local Area Network integrates both industrial and process controls.

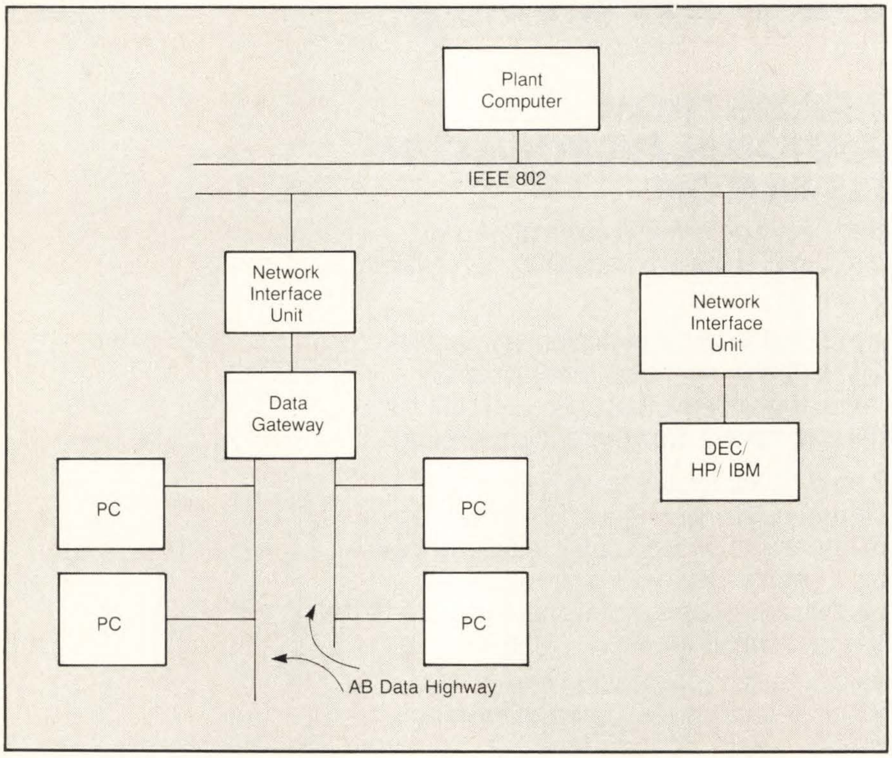


Figure 2: Allen Bradley's IEEE 802 network scheme links up to 64 stations together by cable up to 10,000 ft. long.

Westinghouse robotic controls, non-Westinghouse PCs, HP's 1000 series and Westinghouse WDPF distributed processing family 16-bit computers (**Figure 1**). The linking of the Westnet and WDPF systems integrates process control and PC highways. Previously, linking the two types of networks has resulted in costly software solutions that sacrificed data communication speed. Engineered on a multi-drop coaxial cable architecture, the Westnet PC data highway has a master/slave configuration. The maximum highway length is 1000 ft., yet the Westnet provides communications at a speed of 1 Mbaud.

Westinghouse offers two Westnet configurations in the factory automation network: the Westnet interfaces with a DEC PDP series computer or an HP 1000 as a master. Regardless of the configuration, however, Westnet offers complete PC control functions including programming and monitoring of PCs, uploading and downloading of PC programs, forcing PC contacts and coils, and changing PC register contents. These functions are available simultaneously from either the master drop or from any program loader connected to the highway.

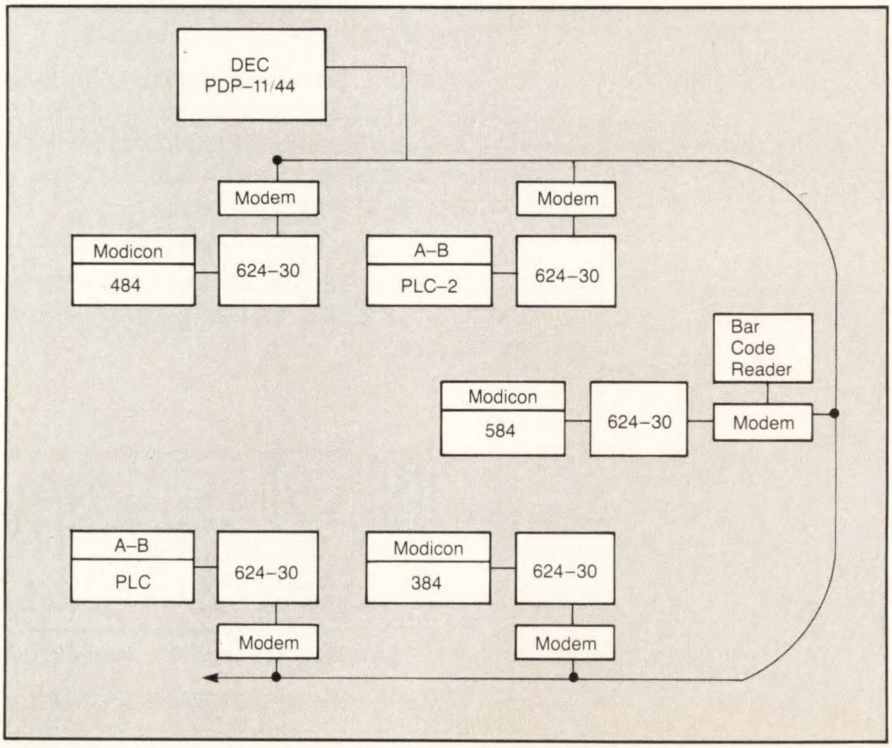
Data Highway

With the Allen Bradley Data Highway, users can set up a data communications network in which up to 64 stations are linked together by cable up to 10,000 ft. long (**Figure 2**). Individual stations on the Data Highway can include combination of Allen Bradley PCs and intelligent RS232C devices that can be located on a trunkline up to 100 ft. from the main cable. Multiple data highway clusters and individual programmable devices, computers and/or operator stations can be interconnected over a plant-wide broadband local area network. Data Gateways can be used to interconnect instrumentation systems' proprietary networks with the Allen Bradley Data Highway.

Standards

The establishment of standards is being strongly pursued by Westinghouse, Allen Bradley and other key names in the PC industry cooperating closely with the IEEE, ISO and NBS organizations. The emergence of networking standards will help to solve some of the systems integration problems of PCs and robotics controllers and produce simpler solutions to complex problems of the factory of the future. □

Figure 3: With COPNET, a DEC PDP-11/44 supervises data exchange for up to 254 devices.



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A System Architecture Approach to Microcomputer Benchmarking

by Rich Billig and Randy Cronk

Before undertaking an evaluation of various microcomputers, it is important to first establish relevant performance criteria. Engineers are constantly trying to select the best tool or component for a particular design. When that component is a microcomputer, it is necessary to determine which microcomputer runs the application the fastest, in the smallest package, for the least cost.

The only way to answer this question with complete certainty is to actually try out the application with each microcomputer under consideration. Because of time and cost, however, it is rarely possible to build a real-life application around several different microcomputers.

One reason is that real-life applications tend to involve special relationships between the microcomputer and particular hardware devices. These relationships are difficult to duplicate in a benchmark without going to all the trouble of actually building the special hardware environment to be used.

A second reason is that real-life applications are usually too large to program cost effectively only for the purpose of comparing microcomputers.

A common alternative to expensive real-life benchmarks is to run no benchmarks at all. Instead of benchmarks, the application engineer relies on product specifications, design descriptions and perhaps past experience to guide him in his microcomputer selection.

Rich Billig and Randy Cronk are with Digital Equipment Corporation, Hudson, MA 01749.

Benchmarking is defined as a measure of total system performance as opposed to simple hardware performance.

These indicators, however, do not go very far toward accurately predicting how a microcomputer will perform in a new and complex application.

A second alternative that is also used frequently is to run what might be called hardware benchmarks. These benchmarks are small segments of assembly code designed to test the pure execution time of the basic processor. The problem with hardware benchmarks is that they do not measure the performance of the microcomputer from the point of view of a high-level application. To increase programmer productivity, most applications are written in vendor-supplied high-level software, not assembly code.

A third way to benchmark is to run applications that consist of high-level code. These programs tend to draw upon all the resources of the microcomputer, not just the hardware. The challenge with this approach is to test total system performance without getting bogged down in special hardware or extensive programming.

Area	What Is It?	How To Measure It?
System Architecture (Instruction Set Processor)	The Original "Global Design" For A Computer	• Bit Efficiency • Orthogonality • Addressing Capability
Hardware Implementation	The Actual Realization Of The Design In Hardware	• Speed of Instruction Execution Per Unit Cost • Power • Physical Size
Software Implementation	The Actual Software Which Implements Applications on the Architecture	• Size and Speed of Runtime Executive • Size and Speed of Language Support Code • Size and Speed of Compiled Programs

Figure 1: Three major factors control microcomputer performance.

	Benchmarks					
	Integer Only			Floating Point		
	LIST	QUEENS	SALE97	SMALL1	MATRIX	WHET2
DEC FALCON SBC-11/21 with On-board Memory	23.6*	19.9	53.1*	58.2	61.8	72.3
DEC FALCON SBC-11/21 Q-Bus Memory	37.8	33.4	84.9	94.2	104.3	118.9
DEC LSI-11/2 With KEV11	31.0	31.0	34.1	43.5	34.7	22.4
DEC LSI-11/23 Without Floating Point Hardware	16.7	15.0	17.9	41.4	48.1	53.8
DEC LSI-11/23 With KEF11	16.7	15.0	17.9	9.0	19.5	14.8
DEC LSI-11/23 With FPF11	16.7	15.0	17.9	3.3	10.7	5.9
INTEL iSBC-86/12A w/o FP Hardware	37.0	14.5	302.0	510.0	1450.0	640.0
INTEL 86/330 w/ iSBC-337	43.0	15.0	304.0	3.9	19.5	8.6
MOTOROLA M68KMP4	23.0	18.8	31.0	33.0	40.0	34.0

* *Required more RAM than available on-board; benchmark is estimated from Q-bus memory time (1.6 to 1.7 times faster than on-board memory).*

Intel Pascal-86 V2.0 Motorola Pascal V2.0

Table 1: Pascal Benchmarks—speed of execution in seconds.

Total System Performance

Total microcomputer performance depends on performance in three areas: Instruction set and system architecture, hardware implementation of the architecture, and software implementation of the architecture (**Figure 1**). All computers implement a general scheme of organization, functions, and behavior known as an architecture. The architecture is the way the machine appears to the machine level programmer and can be characterized by the instruction set processor (ISP). A better architecture will make it possible to perform more functions with fewer instructions. Hence, although a processor may execute its instructions more slowly, it may execute an application faster because of a better architecture.

Several factors contribute to architectural performance. Three important factors are bit efficiency, orthogonality, and addressing capability. A bit efficient architecture allows the computer to execute an algorithm with fewer instruction bits. Bit efficiency is a function of the number of bits in the instruction word and the number of operations performed for each instruction. A computer with a large instruction word may be more bit efficient than a computer with a small instruction word if the computer can do an equal number of operations with far fewer instructions.

The benefits of bit efficiency are small program size and high execution speed. With fewer bits needed for operations, programs can be smaller. They are therefore more likely to fit into high speed onboard memory. Also fewer memory references are required to fetch program instructions.

Orthogonality measures the ability of a computer to address different data types the same way, independent of the data type it references. The problem that is likely to occur in a nonorthogonal architecture is that some data types will be harder for the computer to handle than others. Operations that use a more difficult data type will require more memory and execute more slowly.

The programmer's choice of data type should be a function of the application rather than the microcomputer. If an application calls for a problem data type, the programmer is faced with a hard choice. He can force the computer to work with the data type, inefficient though it may be. Or he can use a data type that matches the preferences of the computer at the expense of the applicaton. Neither choice is optimal.

An architecture with a good addressing capability will use the same instruction to address a processor register, main memory, or an I/O device. Moreover, no distinction is made between data and address locations anywhere within the system, including the processor registers.

This can be helpful when manipulating arrays, for example. In a system with dedicated data and address registers, an array subscript must often be created in data registers before it can be coded to address registers to access the operand. This transfer from data to address requires additional program code which can reduce system performance.

Hardware performance determines how fast the machine executes particular features of the architecture, such as a MOV instruction. This is a function of the basic technology, circuit layout, selection of components, ingenuity of design, and other factors. Good hardware design also reduces package size, cost, and electrical power requirements.

Software is the code executed by the hardware. It consists of compiled source code, the runtime executive, and high-level language support code. A high-level application typically consists of all three types of software.

The performance of an application depends to a great extent on the compiler which translates the source lines written by the programmer into executable machine object code. A better compiler produces fewer bytes of object code per line of source code. This implies that the hardware needs to execute fewer instructions per application so that applications execute faster from smaller memory.

A better compiler produces fewer bytes of object code per line of source code.

Sharing the target system's memory with the compiled source code are the microcomputer vendor's executive and language support services. The executive provides the routines needed to schedule and synchronize processes, drive external devices, and manage other software resources. The language support services are functions especially implemented for the high-level language. Some examples might be input/output data formating, special math functions, and dynamic allocation of storage space.

Runtime executive and language support software should occupy a minimum of computer memory. This allows more space for the compiled source code. Finally, faster executive and support software will allow faster and more reliable realtime applications.

Benchmark Methodology

The purpose of benchmarking is to measure performance in all areas that could affect the user's real-life application. Usually more than one benchmark program needs to be run in order to measure the various application components. It bears repeating, however, that *no* benchmark or set of benchmarks can take the place of the real-life application as a completely accurate test of how that application will run on a microcomputer.

The following would therefore be an appropriate list of microcomputer benchmarking guidelines:

- Benchmarks should represent a scaled-down version of the algorithms to be used in the actual applications.
- Benchmarks should be written in the high-level language intended for the application.
- Benchmarks should be compiled under the existing vendor-supplied compiler.
- Benchmarks should be run in the actual runtime environment to be used (i.e., with the vendor-supplied support software).
- Benchmarks should measure memory usage, in addition to

	Digital MicroPower/Pascal V1.06		Intel Pascal-86 V2.0		Motorola M68000 Pascal V2.0	
Benchmark	**Size**	**Ratio**	**Size**	**Ratio**	**Size**	**Ratio**
1	600	1.00	926	1.54	724	1.21
2	372	1.00	440	1.18	458	1.23
3	764	1.00	1048	1.37	980	1.28
4	148	1.00	271	1.83	238	1.61
5	338	1.00	571	1.69	560	1.66
6	1470	1.00	2048	1.39	1968	1.34
Average		**1.00**		**1.50**		**1.39**

Note: Sizes listed are in decimal bytes, and take into account all instructions generated, as well as any constant data (strings).

Table 2: Size of compiler generated programs.

execution speed.
- Benchmarks should always be measured, not estimated, in the intended execution configuration.

Such benchmarks, run on different microcomputer, would provide a reasonable basis to compare systems for high-level real-life applications.

	Digital MicroPower/Pascal		Intel Pascal-86 + iRMX/88		Motorola M68000 Pascal + MRS68K
Floating Point HW?	Yes	No	Yes	No	No
Initial ROM	64Kb	64Kb	64Kb	64Kb	64Kb
Minus Size Of Minimal OS Support	−5Kb	−5Kb	−21Kb	−21Kb	−17Kb
Net ROM After OS	59Kb	59Kb	43Kb	43Kb	47Kb
Minus Size Of Pascal Support Code	−2Kb	−3Kb	−9Kb	−27Kb	−5Kb
Net ROM for Pascal Prog.	57Kb	56Kb	34Kb	16Kb	42Kb
Divided by bytes/line Compiler Efficiency	/7.1	/7.1	/10.6	/10.6	/9.9
Estimated # of Source lines in 64Kb ROM	8.0K	7.9K	3.2K	1.5K	4.2K

[1]OS size includes nucleus and terminal handler plus I/O system. Sources: *Intel Systems Data Catalog*, #210299-001 (January, 1982); *M68000 Real-Time Multitasking Software User's Guide* #M68KRMS68K(D1) (December, 1980).

Table 3: Sample calculation of number of Pascal source lines that fit in 64kBytes ROM.

Microcomputer Benchmarks

When Digital recently ran microcomputer benchmarks against Motorola and Intel it selected Pascal as a high-level language. Pascal is one of three languages that are currently in wide-spread use in microcomputer applications. The others are PL/M and Fortran. Since PL/M is a vendor-specific language, it would be nearly impossible to benchmark as a standard across various manufacturers. Fortran, on the other hand, is implemented as a standard across different manufacturers. However, Pascal seems to be moving ahead of Fortran as the language of choice for microcomputer applications.

The subset of Pascal defined by Jensen and Wirth was selected because it is the Pascal standard most universally accepted.

Six benchmark programs were run. Each required compilation as well as various levels of system software support. Each program also was sufficiently complex to enjoy the advantages (or suffer the disadvantages) of each vendor's architecture. Of the six, three used integer-only computation and three used floating point computation. The goal in selecting the benchmarks was to find programs that demonstrated various aspects of performance in order to arrive at a general comparison of the total systems offered by the three vendors.

The six benchmarks were as follows:
- LIST — This function uses the "NEW()" function of Pascal to dynamically allocate 1000 records of the type that might be used by a compiler generating a symbol table. These records are then formed into link lists which are searched and manipulated. This program is specifically aimed at testing Pascal for system implementations.
- QUEENS — This classical Pascal benchmark calculates the number of possible ways to place eight queens on an 8×8 chessboard so that no queen is attacked by any other queen.
- SALE97 — This is a test of some of the more difficult to implement Pascal features such as set manipulation.
- SMALL1 — This program tests real number statement executions speed. The program calculates a short expression 30,000 times.
- MATRIX — This program tests operations on three 4×4 real number matrices. The main loop is repeated 1000 times.
- WHET2 — This is one of the Whetstone benchmarks translated from Fortran into Pascal. It performs a variety of complex floating point operations repeatedly.

Again, the first three benchmarks are integer-only while the second three are floating point.

As shown in **Table 1**, the Digital machines tested were a Falcon, LSI-11/2, and LSI-11/23. The Falcon was tested with the application running completely from on-board memory (its normal configuration as a single board computer) and also from a RAM card located on the Qbus. The LSI-11/2 was tested with the KEV11 hardware floating point option. The LSI-11/23 was tested without floating point hardware support and with both the KEF11 and FPF11 floating point hardware options. The Intel microcomputer tested was the iSBC-86/12A. It was tested both with and without the iSBC-337 hardware floating point option. The Motor-elscint

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Language & Machine	Compiled Size (Bytes)	Times Larger Than 11/23	Execute (Seconds)	Times Slower Than 11/23
NBS Pascal, PDP-11/70	333	2.49	2.6	0.60
MicroPower/Pascal, LSI-11/23	134	1.00	4.33	1.00
NBS Pascal, PDP-11/60	333	2.49	4.5	1.04
MicroPower/Pascal, LSI-11/2	134	1.00	8.83	2.04
MT Microsystems Pascal MT, 4MHz 68000	410	3.06	9.0	2.08
Intel PASCAL-86, System 86/330	267	1.99	7.9	1.82
RSI Pascal, 4 MHz 68000	318	2.37	10.2	2.36
Motorola M68000 Pascal, 8 MHz 68000	260	1.94	10.4	2.40
MT Microsystems Pascal MT+, Z80	308	2.30	19.0	4.39
Pascal, HP3000	—	—	20.0	4.62
UCSD Pascal, Pascal 100	298	2.22	54.0	12.5
UCSD Pascal, Pascal Microengine	298	2.22	63.0	14.5
Ithaca Intersystems Pascal/Z, Z80	761	5.68	109	25.2
Atari Pascal, Atari 800	—	—	190	43.9
UCSD Pascal, Z80	282	2.10	239	55.2
UCSD Pascal, TRS-80 Model II	282	2.10	274	63.2
UCSD Pascal, Terak LSI-11	282	2.10	317	73.2
Pascal/M, Z80	301	2.25	450	104
JRT Pascal, Z80	232	1.73	470	109
UCSD Pascal, Apple II (6502)	287	2.14	516	119

Table 4: Comparison of software products.

ola machine was the M68000-based M68KMPU.

It is interesting to note that the application run times show no relationship whatever to processor clock frequencies. **Table 2** shows the amount of object code generated by each of the three compilers involved.

Performance = Speed + Memory Efficiency

This data illustrates the importance of memory efficiency as a microcomputer performance parameter. Most benchmark data usually will not show the amount of memory required by the benchmark on various machines. This may be a serious oversight.

The software's ability to fit into a small area may determine whether or not a given application can even be run on a microcomputer in the first place. Another consideration is cost. At several hundred dollars per board, the cost of added memory modules can substantially impact the cost of an application. Physical size and weight are also factors. An extra memory card or two may severely restrict where an application can go.

Suppose, for example, that a particular application absolutely must fit into 64K bytes of ROM. The question then becomes: How many lines of high-level code can be executed from 64K bytes? The greater the number of lines, the more functions that can be put on a single board computer or single memory card. The question can be answered in two steps:

- Subtract from 64K bytes the amount of memory required for vendor-supplied system software. This yields the amount of memory available after loading the software required to handle system runtime requirements such as process scheduling and driving external devices.
- Divide into this available space the number of bytes typically generated for a line of Pascal by the vendor's Pascal compiler.

Data for both these steps is available from the benchmarks. To get data for step one, average the amount of runtime support required in each benchmark. To get data for step two, divide the number of Pascal lines into the number of bytes of instruction and constant data generated for each compiled program. Average this result across all the benchmarks. **Table 3** shows the results from doing these steps for the six benchmarks.

As **Table 3** shows, expertise in software can have a compounding effect on a high-level application. One vendor may leave more room for application machine code than another (after subtracting the space required for the operating system and system services). Often, too, it is the same vendor who is better at system design who is also better at compiler design. This means that usually the same vendor who leaves you more room to start with will also let you fill that room with more compiled source lines of application per byte of memory.

System efficiency is a function of architecture as well as system software. Even when an "optimum" operating system has been achieved, that system is still limited by the architecture. Instruction word size, orthogonality, and bit-efficiency ultimately determine the power of a byte of system-level code.

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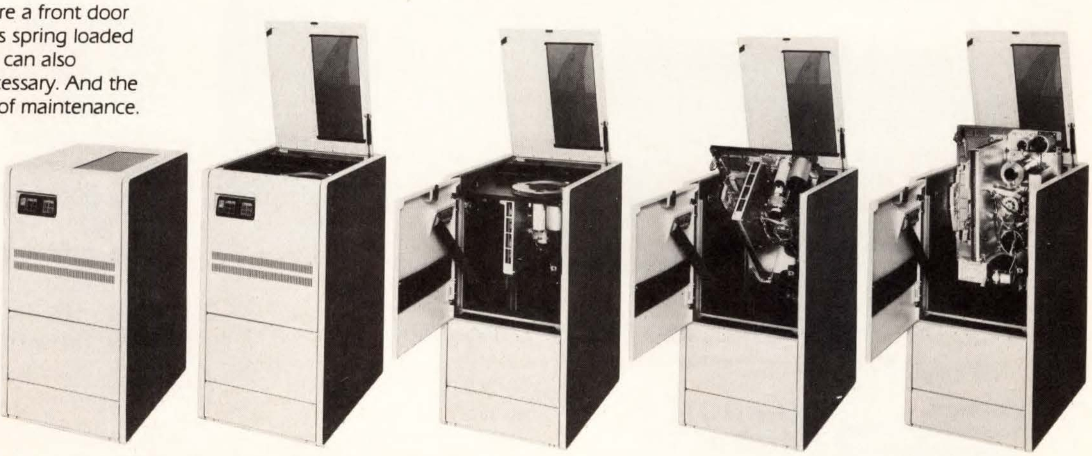

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Write 67 on Reader Inquiry Card

Third-Party Software For μPs

As 16-bit μP chips have become increasingly popular, a burgeoning "cottage" software industry has grown up around them. Certainly there are now more small companies offering μP software packages than there have been for minicomputers and mainframes. These companies have formed to fill a perceived market need for sophisticated software of different types (applications, communications, operating systems, language processors) which many of the semiconductor vendors were not initially offering.

Because of the wide variety of such offerings on the market today, this article cannot attempt to include sufficient benchmarks of these products to offer a representive spectrum. It is important, however, to review some general aspects of such third-party software packages.

The third-party software package for a microcomputer is often attractive to an engineer for one of several reasons. It may offer an application, operating system, or language which is not available directly from the microcomputer vendor, or it may be a more efficient implementation, or it may be less expensive to use (in initial purchase cost, or volume license fees). There are, however, negative aspects of purchasing third-party software which should be weighed against potential benefits. Two of the potential problem areas include quality/reliability/serviceability of the software, and maintaining support for new hardware/peripheral features.

Note that the January 1983 issue of *Byte* magazine offers additional data points on the Eratosthenes Sieves benchmark, showing the performance of some third-party packages on this single program. (Beware using a single program as a performance metric, however, as noted earlier in this article!) **Table 4** shows a comparison of some third party packages.

"Debugged Software" is (for the most useful programs) a contradiction in terms. The more useful the function of a software product, the greater its inherent complexity, and hence the number of potential decision paths through the software. In general, applications programs are less complex than operating system kernals, which are less complex than compilers for programming languages. Although current computer science advances are allowing small sections of operating system kernels to be "proven correct," such guarantees are not likely to be possible for complex functions such as compilers in the near future. When an engineer purchases software products as tools for an application, they are expected to perform according to their specifications. If, in the midst of the critical segment of applications development, a significant flaw is found in the software tools, development stops until the nature and impact of the error can be found.

When all components (hardware and software) come from the same supplier, the engineer can rightfully hold that supplier responsible for the quality of the tools. However, if the tools come from numerous sources, all of which disclaim total responsibility, the problem solution is almost always difficult.

The third-party software supplier stands at an additional disadvantage to the original microcomputer vendor. In introducing the new hardware capabilities, both in terms of CPU features and peripherals, the microcomputer vendor's software engineers have a head start on the third-party houses. The vendor's software people have earlier access to specifications, can effect changes in them to accommodate potential software problems, and can make use of the first hardware prototypes (and their design engineers) in debugging the software. The third-party vendor must make do with whatever is supplied to the average customers; it is only in cases where the vendor has little or no sophistication in software design and development that the third-party can compete. □

Product Index

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Local Area Networks: A Comparison Of Standard Bus Access Methods

by C. Kenneth Miller and Robert H. Douglas

The IEEE-802 Local Area Network Standards Committee recently completed a set of draft standards for Local Area Networks. IEEE 802.3 (Reference 1) is a standard for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) that is nearly identical to the Xerox Ethernet system (Reference 2). The second standard, IEEE 802.4 (Reference 3), describes a token passing access method, quite different in its characteristics from CSMA/CD.

Token Bus presents an alternative to CSMA/CD.

It is anticipated that these draft standards will be approved by the IEEE with possible minor revisions, forwarded to the American National Standards Institute (ANSI), sent to the International Standards Organization (ISO) and eventually become international standards. (Concurrent with the work of the IEEE in North America, the European Computer Manufacturer's Association (ECMA) has proposed nearly identical standards for LANs, lending further credibility to these two access methods.)

While CSMA/CD as used in Ethernet is widely known, token passing used on busses is relatively unknown. This article presents the significant differences between the access method described in the two draft standards.

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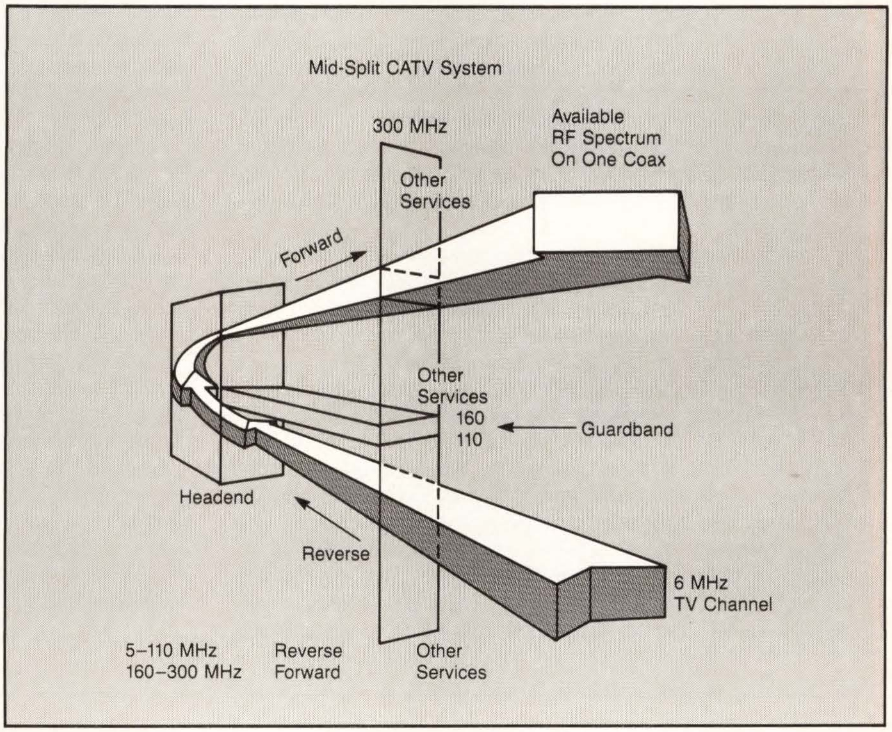

Figure 1: Every signal must be sent to the headend and back.

Access Methods

CSMA/CD uses the principle "listen before transmitting, listen while transmitting" to gain access to the network. All stations listen to the medium and defer transmitting if it is in use. If silence is heard, a station may jump in and immediately transmit. This is roughly analogous to the implicit rule we use in speaking within a group of people. When there is silence, anyone may speak; when someone is speaking, others wait until there is silence again. If multiple speakers attempt to talk simultaneously, they all detect the "collision" and stop talking.

One attribute of the CSMA/CD access method is apparent from comparing it to what happens in a busy, disorganized meeting. People try to talk at once, creating many interruptions. In a CSMA/CD LAN, high network loading may cause many collisions which restrict the total network throughput, and which even cause network throughput to decrease as the load increases (Reference 4).

Token Access

The other access method being standardized by the IEEE is poll-

Higher Level Services Are The Key To The LAN Environment

At the recent Communications Network 83 conference in New Orleans, Brian McGann discussed the Associated Computer Consultants Exchange System (ACCES).

ACCES products are not limited to specific local area network implementations. Hardware and software modules are strictly layered, allowing customers to build tailored networks from interchangeable building blocks. Software packages may be incorporated into operating environments from mainframes (running different operating systems), to microcomputer-based work stations, to intelligent peripheral interfaces. Whether a particular implementation be broadband or baseband, coax or fibre-optics, user application code and high level subsystem interfaces remain unchanged.

The first product, the IF-11/Ethernet was introduced a year ago, before the ACCES product line was officially established. The second product, the ACCES NS Protocol package was announced at the end of January 1983.

Two versions of the NS Package are offered. The first, NU-11/NS, is a host resident package which implements the NS Protocol Package through the Courier level (OSI model layer 6). All NS software modules reside in the host computer. One of these modules, the Network Interface Module, communicates with network hardware via the host's bus and appears in the system as an I/O driver. This model gives systems designers great flexibility in the selection of network hardware. By choosing an appropriate Network Interface Module, the ACCES NS Package may be configured to operate with hardware from a variety of vendors, including ACC.

The second version, the FE-11/NS, incorporates virtually the entire NS Protocol Package into ACC's programmable Ethernet Controller (IF-11/Ethernet). This version draws upon the benefits of a dedicated front-end processor to increase network performance and to significantly reduce the host's processing overhead. That is, all of the network services including remote procedure calls can be made at the I/O driver level, substantially minimizing impact to the host CPU.

McGann points out the need for the ACCES NS Protocol Package. "Standard Ethernet Controllers (3Com, Interlan) allow the user to connect the host to the Ethernet cable, but then what? The user is now in the analogous situation of having the phone company hook up a phone that has no handset, no dialing mechanism, and no phone book. You're connected, but it's only a technical fact, not a useful situation." He continues, "In our opinion, Ethernet as defined in the DIX (Digital, Intel, Xerox) Specification is logically little more than an intelligent RS232 cable. The user needs much more to get useful work done in an LAN environment. The higher level services are the key."

Beyond the ACCES NS Protocol Package and the programmable Ethernet controller, McGann expects to announce several more products this year, including an IBM Channel/Ethernet Interface, an X.25/Ethernet Bridge, an Intelligent VERSAbus Ethernet Front-end, and a Baseband/Broadband Converter. *—Wilson*

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ing, which in its distributed form is called token passing. A "token" designates the location of the poll in a distributed polling list. Possession of the token allows a station to transmit. When a station receives the token it may transmit. After sending any data, the station sends the token to the next station. In bus topologies, the token is passed around a logical ring. Using the token access protocol, accesses are ordered and occur only with possession of the token so that collisions do not occur during normal system operation.

Token access does not suffer from restricted throughput as loading increases, since it does not use collision detection as its access control method. As a result the capacity of a token access system is easily predictable, even under high loads. In applications where guaranteed rapid response time is important token access is more suitable than CSMA/CD.

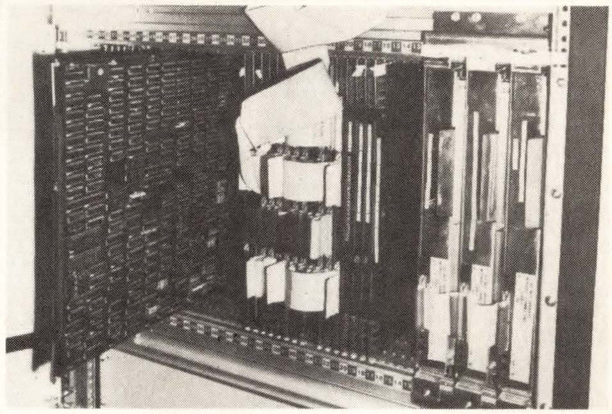
Network Size

As the length of a LAN increases, the maximum throughput of the network decreases. What may not be appreciated is that the rate of decrease depends on the access method.

To study the effect of increasing the length of a CSMA/CD network, imagine that our hypothetical meeting is taking place with the speakers miles apart. The time it takes for the speech to travel from one speaker to another becomes significant. A distant speaker will not be heard for a long time. During that time the other speaker still thinks there is silence and may attempt to talk. Since two speakers are talking at once, a collision has occurred and listeners located at different points may or may not hear both messages collision free.

CSMA/CD systems ensure that collisions can be detected by requiring messages to be greater than a minimum length. If two stations begin transmitting simultaneously, the messages must be long enough so that at least part of the messages will collide and the collisions will be heard while still transmitting, no matter how far apart the stations are. In Ethernet and in the proposed IEEE standard, messages must be at least 512 bits long. This minimum message length limits the maximum network size to 2500 me-

Interlan Puts Data General On Ethernet



Interlan has announced a controller board, the NI4010A, that converts Data General minicomputers, such as the Nova, and Eclipse, to the Ethernet LAN. A major OEM agreement for the Data General Ethernet controller and other Interlan controllers has been executed by Calma. The controllers will provide links between their Apollo based system CIRCUITS, major IC and mechanical CAD/CAM systems and Calma 170 office sized systems.

—*Wilson*

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ters of cable.

If CSMA/CD is used as the access method on broadband cable, the distance sensitivity is increased because the propagation path length may be doubled, since on broadband every signal must travel to the headend and back (**Figure 1**).

The token access method does not require the detection of collisions, nor does it mandate a minimum message length. While performance degrades as network length increases, due to the additional time to pass the token, the effect is much less than with CSMA/CD. Token access networks using high data rate with lengths of 10 to 20 miles are practical.

Cable Requirements

CSMA/CD places constraints on the physical medium to allow collision detection. What would happen to our "meeting" if each time one of the speakers started to talk he heard his echo? The speaker might interpret the echo as another speaker talking and so stop talking.

For CSMA/CD to work there cannot be a loud "echo" on the cable. Electrical echos are caused by reflections from impedance mismatches. Ethernet requires matched cable sections and special taps to prevent reflections. Additionally, the cable is carefully shielded to prevent external noise from being interpreted as a

Token/Net

Token/Net is Concord Data Systems' (Waltham, MA) turnkey, broadband CATV based local area network (LAN) designed to the IEEE-802 draft token bus standard. Network data rate is 5 Mbps in the initial product.

Token/Net is suited to general purpose applications and relatively large networks, made possible by the combination of token access and broadband media. Using the IEEE-802 priority feature it is feasible, for example, to have MIS/DP applications using the same network as factory automation, engineering, and office automation.

Extensive user services are provided in Token/Net. All common synchronous and asynchronous RS-232C/V.24 serial interfaces are provided at speeds from 75 to 19,200 bps. High speed serial ports (to 230.4 kbps) and IEEE-488 parallel ports are also available.

Ports may be connected as permanent or switched point-to-point, multipoint, or broadcast (multicast) connections. The switched connections may be established utilizing pathwords, i.e., "SEC" may be a generic name for a computer port for use by secretaries; users making a connection may use this mnemonic without having to remember numbers or addresses. Switched connections may have "rotaries," so that "SEC" may represent a set of ports, any free one of which may be automatically selected. Priority and queueing (camp-on) services are offered. Restricted service classes are available to restrict connection services between stations.

A privacy option solves the increasingly important problem of security, by allowing data to be encrypted using the DES standard.

Token/Net is software intensive and has a centralized network software reload unit. Network software upgrades and enhancements can be performed either by replacing a bubble memory carrier or by transmitting new software over the dial telephone network to the network reload unit without visiting the site. Unit and network diagnostics are provided, the latter including meaningful network statistics able to be generated by observing the characteristics of the token pass over time.

Since a broadcast protocol is used for simultaneously reloading stations on start-up, even networks with large numbers of stations can restart within seconds after a power failure.

The hardware for the network consists of Token/Net Interface Modules (TIMs). A TIM 200 provides either two RS-232C serial ports or one RS-232C and one high speed port (either RS-422/RS-449 serial or IEEE-488 parallel). A TIM 220 provides up to ten serial ports. A rack mount model can provide even more ports per station. A keypad dialer allows ports the features of switched connection services when the connected terminal is not suitable.

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collision.

Collisions are detected in the Ethernet system by adding a DC bias to the signal and having all transmitting stations and repeaters look for a DC level greater than that of a single transmitter. This technique may only be used on media that pass DC signals, making it applicable only to baseband systems.

CSMA/CD systems have been implemented on broadband media. In such systems, collision detection is usually implemented by the sender doing a bit by bit data comparison of what he transmits to what he receives (with some delay). If there are any mismatches, a collision is assumed. This method assumes that

Monitoring error rate and signal levels can often detect problems before they affect the user.

the colliding RF signals' levels are within a few dB of each other at each receiver so a collision causes an error. If the transmitted signals differ substantially in level, the stronger of the two signals may "capture" the receiver and no collision is detected. Although one message gets through, an unintended system characteristic manifests itself; transmitters with higher signal levels have a higher chance of gaining access to the medium than lower level transmitters, thus creating an unintended priority structure.

Some vendors have eliminated collision detection. CSMA without CD gets around the receiver capture difficulty, simplifies the medium interface, and eliminates the minimum message length requirement. Unfortunately, eliminating collision detection lowers maximum network throughput to about 18% (Reference 5). Thus a CSMA without CD network with a data rate of 10 Mbps has a limit of less than 2 Mbps of aggregate network traffic.

The presence of collisions as a consequence of normal system operation additionally has the potential to cause frequency "splatter" during collision time on broadband systems, inducing additional interference into other TV channels on the system.

Measuring Error Rates

In operating a large network, it is important to monitor network performance. If a cable is damaged or a repeater/amplifier begins to fail, the network often continues to function; however, error rates increase. Monitoring error rate and signal levels can often detect a problem before it affects the users.

Since collisions and the resultant garbled transmission occur normally on CSMA/CD networks, it is difficult to measure transmission error rates on an operating network. A token bus network sends data only when other stations are not transmitting so the number of garbled data messages is a good measure of the error rate. A high error rate is an indication of either an incipient failure in a station/repeater/amplifier or a defective cable.

Priority Levels

Some applications require that different priority levels of data may be sent over the same network. For example, terminals may be connected to a mainframe computer over the same network that is used to transfer data between computers. If more traffic is presented to the network than it can handle, it might be desired to defer transmitting the computer-to-computer traffic until network loading is reduced.

Since it is intended for operation at light loads, when response time is short, neither Ethernet nor the IEEE CSMA/CD standard provide for message priority.

The IEEE token bus standard provides four levels of priority. Transmissions of lower priority messages are deferred when the network is heavily loaded. Network loading is computed at each station by measuring the time between token passes. When the network is lightly loaded a station passes the token and receives it again in a short period of time. As loading increases the time for the token to return to a station increases. If the time exceeds a predetermined threshold value, low priority traffic is deferred until network load decreases. A separate threshold value exists for each of the three lower priority levels.

Summary

The presence of token bus products in the marketplace gives the user a real alternative. He can now obtain the features of token access in a product that conforms to a standard. Using a standard access protocol protects the customer from obsolescence and allows inter-operability of equipment from different manufacturers.

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4 E. Arthurs, B.W. Stuck, "Traffic Analysis Tools for Token Passing Media Access Methods for Local Area Networks," *Electro/82 Session Record,* May 1982.

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References 1 and 3 may be purchased from the IEEE Computer Society, 10622 Los Vaqueros, Los Alamitos, CA 90720. $30 for non-members.

Disk Controller Unburdens Real Time Applications

Computers are currently being used in real time applications more than ever. Equipment used in industrial automation, telecommunications and medicine relies on processors to provide intelligent control and data processing ability in real time situations.

Many applications require storage and retrieval of large amounts of data from one or more data bases. The processing overhead required to efficiently organize this data into files can be quite large. Because of the time constraints associated with real time applications, this function often cannot be performed by the same processor that performs real time control. File management software also requires significant amounts of memory space, further limiting the resources available to real time tasks. Because of the large amount of memory and processing resources used by file management systems, data storage and retrieval is often accomplished by downloading to an external computer or limited to simple direct sector data dumps onto disk storage devices.

A New Solution

Providing real time equipment with the file management power previously limited to much larger computing systems was the aim behind the PM-3001 disk controller. In addition to disk control circuitry, it contains 32 Kbits of cache RAM and PFMS, a ROM based file management system designed for maximum efficiency in real time applications. PFMS (which stands for Paged File Management System) is executed by a µP located on the PM-3001. PFMS performs all file manipulation by responding to simple high level commands issued by the host system.

Commands are issued to the PM-3001 by using host command blocks. A host command block is a buffer in the host computer's memory containing a one byte operation code followed by the parameters for that command.

To initiate action by the PM-3001, the following steps must be taken by the host processor. The host command block is assembled in the host memory. This may be done in real time by the host processor or may be loaded into the host memory along with the host program. The address of the first byte in the host command block is written into a register in the PM-3001 by the host processor. This initiates command execution by the PM-3001. The host processor may now spend its time servicing real time tasks. The PM-3001 reads the host command block using Direct Memory Access (DMA). All data transfers to or from disk are handled by the PM-3001 without any host processor intervention.

When command execution is completed, the PM-3001 transfers a result code to the specified location in host memory. A request for interrupt is then issued to the host processor by the PM-3001.

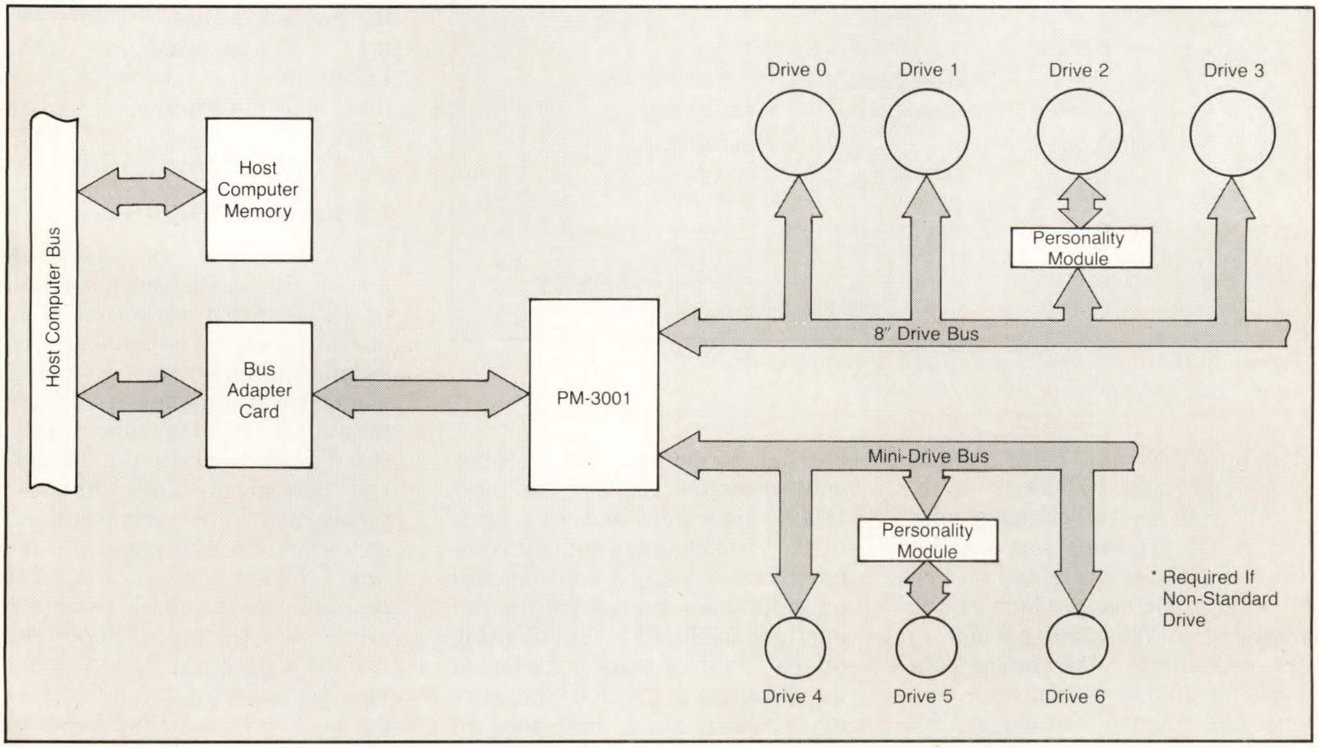

Figure 1: PM-3001 Floppy Disk Controller configuration: with an appropriate computer bus adapter card, it can control up to four 8" drives plus three mini-drives.

COMMAND	DESCRIPTION
READ SEGMENT	Transfers the specified number of bytes from a diskette file to the host computer memory.
WRITE SEGMENT	Transfers the specified number of bytes to a diskette file from the host computer memory.
CREATE FILE	Creates a PFMS file.
DELETE FILE	Deletes the specified file(s) from the diskette and frees the occupied disk space. Wild card file specifications are supported.
COPY FILE	Copies the specified source file(s) into the specified destination file(s). Wild card file specifications are supported.
VERIFY FILE	Compares the specified files and determines whether the data contained in the two files is identical.
RENAME FILE	Assigns a new name to an existing file. Wild card file specifications are supported.
COMMENT FILE	Allows the user to specify a 38-byte comment field to be displayed in the directory listing, for any PFMS file.
MAP FILE	Returns a formatted ASCII sector allocation map for the specified PFMS file.
FORMAT DISKETTE	Writes new track and sector boundries onto soft sectored floppy disk media.
SET VOLUME NUMBER	Allows the user to specify a 10-byte diskette volume number to be displayed in the directory listing, for any PFMS diskette.
COMMENT DISKETTE	Allows the user to specify an 80-byte directory comment field to be displayed in the directory listing, for any PFMS diskette.
COPY DISKETTE	Copies block for block the image of one diskette to another.
DIRECTORY	Returns the diskette directory in formatted ASCII or unformatted binary modes.
MAP DISK	Returns a formatted ASCII sector allocation map for the specified diskette.
READ SECTOR	Allows direct sector access of non-PFMS diskettes.
WRITE SECTOR	Allows direct sector access of non-PFMS diskettes.
DISKETTE TYPE	Returns the media format of the diskette in the specified drive.
SET SYSTEM DATE	Sets the PFMS system date.
VERSION	Returns the PM-3001 version number.
DIAGNOSTICS	Causes the PM-3001 to execute a self-test routine.
UNLOCK DRIVE	Sends an unlock signal to the specified drive.
CONTINUE	Instructs the PM-3001 to transmit another 80 character display line.
PROCEED/SKIP	Used in conjunction with any command which requires confirmation for an action to take place.
TERMINATE	Causes the command currently executing to abort.
RESET	Causes a PM-3001 system reset.

Figure 2: The Command List includes a complete set of file management functions, including wild card file specifications.

The host may now issue another command to the PM-3001.

All disk control circuitry, plus µP, ROM firmware and 32 Kbit cache RAM are contained on one 9″ × 11″ logic board which can be mounted in the same cabinet as the disk drives. This board connects via 40 pair ribbon cable to a host bus adapter card (**Figure 1**). The bus adapter card presents the proper pin-out configuration for interface to the host computer bus and generates signals for host DMA, interrupt, and I/O functions. Virtually any standard computer bus as well as non-standard or proprietary bus structures can interface to the PM-3001 by using off the shelf or custom designed bus adapters. Optional personality modules allow non-standard drives to be intermixed using one PM-3001. Step rates and head settle times are automatically varied to suit each drive's requirements.

File Management System

The PFMS file management system simplifies real time application programming by providing a unique file access method. Data is transferred to and from PFMS disk files much as data would be transferred between host memory and an external memory bank. Each file appears to the host computer as 2 Mbytes of virtual RAM. This means that any byte address from 0 to 2,097,151 may be accessed in a PFMS file regardless of the history of that file.

File space allocation and de-allocation is handled automatically by PFMS during and between disk accesses. When a disk file is created, only one disk sector is initially allocated to that file. All 2,097,151 bytes of the file will contain zeros. As data is written into the file by the host computer, sectors are allocated when necessary to hold non-zero data. Whenever a sector is found to contain all zero data, PFMS de-allocates that sector and places it back into the pool of available sectors so it may then be used in another PFMS file. This scheme increases disk space utilization and eliminates the need for fixed length record blocking by the host.

Unburdens Host Processor

One application for which off-loading file management functions to an intelligent peripheral is important would be an intelligent environmental control or energy management system. In such applications, processor time must be strictly allocated to the monitor and control of temperature set points and other environmental conditions. In addition to this real time function it is also frequently desirable to log these conditions for future reference. If floppy disk storage is used, the data files may then be easily archived or transported to other computer sites for analysis.

Conventional floppy disk controllers require that the system processor halt its real time tasks when data is to be logged so that file management code can be executed. If this code is not memory resident, additional time must be taken to "page in" file management code and to later page process control code back in. Disk writes may also take considerable time due to track seeks and rotational latency within the drive.

Access times for page-resident data for this disk controller, 8″ and 5¼″ floppy disk drives are shown in **Figure 3**. 256–byte sectors are assumed. Best and worst access times using the PM-3001 converge for data transfers greater than 4.5 Kbits. Note that in the same time it takes to transfer 2 Kbits on a 5¼″ drive or 4 Kbits on an 8″ drive, 24 Kbits can be transferred from the PM-3001 paging memory. On the average, 18 Kbits of page-resident data can be transferred before a single byte of disk data can be accessed.

The PM-3001 greatly simplifies the task of data logging since no file management code need be held in system memory or executed by the system processor. In addition, disk writes occur in much less time because of the cache memory on board.

In the case of disk write operations, the cache memory acts like a 32–Kbit write buffer. As data is transferred to the board it is partitioned into 256–byte segments and stored in cache. Although it may take up to one half second for some disk drives to seek the proper track and sector, the PM-3001 allows the host to resume execution of real time tasks as soon as all the data has been transferred into cache. This normally occurs within a few milliseconds.

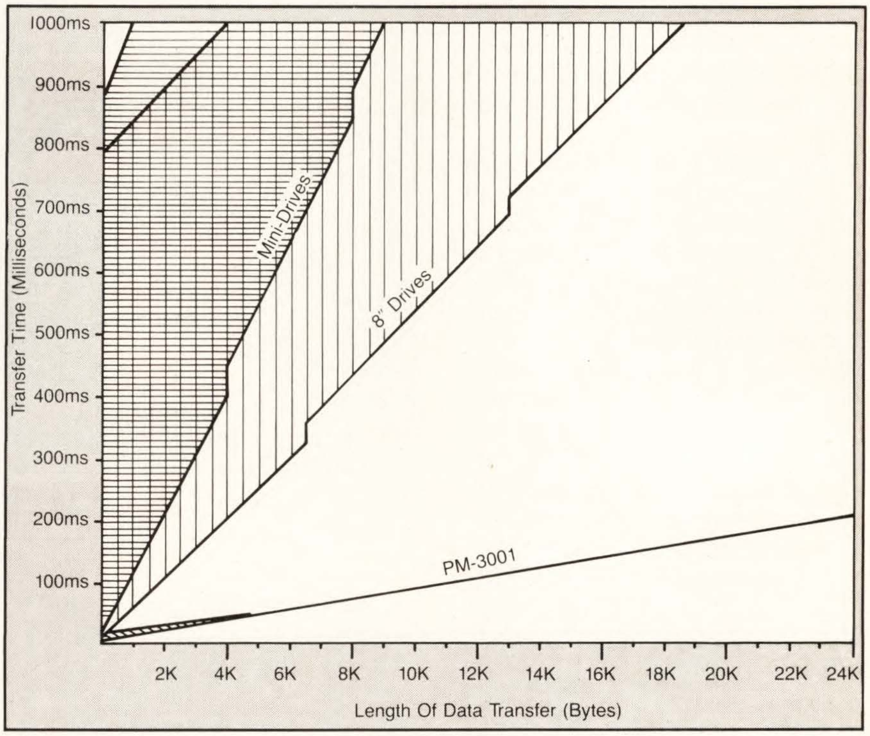

Figure 3: Comparison of best and worst case access plus transfer times for page-resident data using the PM-3001 versus sequentially stored data on 8″ and 5¼″ floppy disk drives.

Program Segmenting

Another common use of disk storage in real time systems is for program segmenting or paging. As an example, consider a computer controlled telephone system such as a PBX or "Private Branch Exchange." In such systems, a large control program is often broken up into smaller segments which are read into memory as needed from floppy disk storage. Program segments to control commonly used telephone functions may always be kept resident in system memory. Program segments that contain code for less frequently used functions might be kept on disk storage until needed. At that time the processor must temporarily suspend the execution of real time tasks in order to supervise the paging in of the desired program segment.

The PM-3001 cache memory greatly facilitates program segmenting not only because of its additional speed but because of its unique paging algorithm. The most frequently used disk data has the best chance of being found in cache. This means that commonly used program segments which are paged into cache most often will have the shortest access times. Program segments that are seldom accessed will more likely be moved out of cache by the PM-3001 to make room for other data.

The designer of telephone system software is not forced to guess which features will be used most often by telephone customers. The PM-3001 monitors disk data usage in real time and adjusts cache resident data for the quickest overall response times, increasing overall system throughput.

One Package

Since the PM-3001 incorporates disk control, file management and cache memory in one package, the design of real time systems is simplified and overall system throughout improved. Because the host processor need not execute file management code, it can handle more real time tasks with a subsequent increase in total system performance.

Stephen Goldman, President, Distributed Processing Technology, P.O. Box 1864, 132 Candace Drive, Maitland, FL 32751.

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CODEC/Filter Enhances System Flexibility

The new TP3051, TP3056 CODEC/filter family from National Semiconductor consists of the μ-255 law coder and decoder (TP3051) and the A-law coder and decoder (TP3056) monolithic pulse code modulation (PCM) devices. Key features of the family include a low operating power of 60mW (typical) and a power-down standby mode to 3mW (typical). Both devices contain internal precision voltage references and internal auto-zero circuitry on chip.

The TP3051 and TP3056 each comprise a complete CODEC and filtering system containing all necessary switched-capacitor filters to meet CCITT and D3/D4 specifications. The devices are pin-compatible parallel interface CODEC/filters for bus-oriented systems and are ideally-suited for use with the TP3100 family of digital line interface controllers (DLIC) designed to allow the user to develop more modular and cost-effective switching systems.

The benefits of a CODEC/filter with a parallel data bus, rather than the usual serial port, are illustrated in **Figure 1**. This shows a 16-channel line card in which the TP3051, TP3056 CODEC/filters share the data bus interface to a TP3110/TP3120 digital line interface controller. The DLIC can access up to 128 channels on the serial backplane, providing fully non-blocking time and space switching capability with optional redundancy. In conjunction with a local μP, typically from the INS8048 family, a standard HDLC control channel can be assigned, providing secure message capability between the line card and the system control processor. The local μP can also collect and process line status and signaling information, off-loading these tasks from the main processor. A prioritized vectored interrupt scheme is used for data transfers between the μP and DLIC.

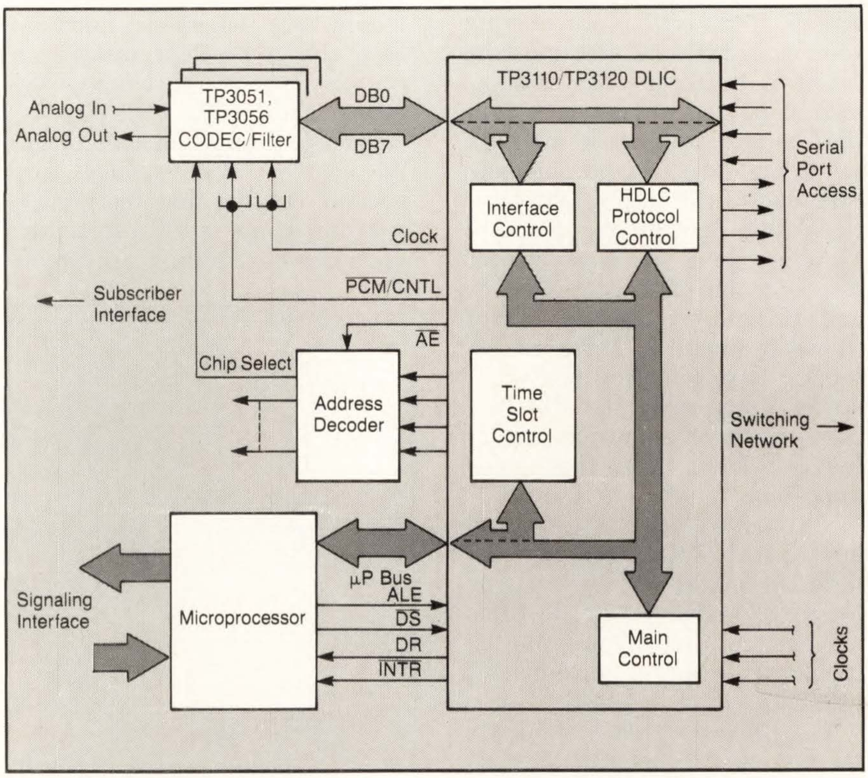


Figure 1: The benefits of a CODEC/Filter with a parallel data bus.

System flexibility can be further enhanced by adding 2 additional bits per frame to the PCM data, operating the DLIC with 80 Kb/sec channels rather than 64Kb/sec channels.

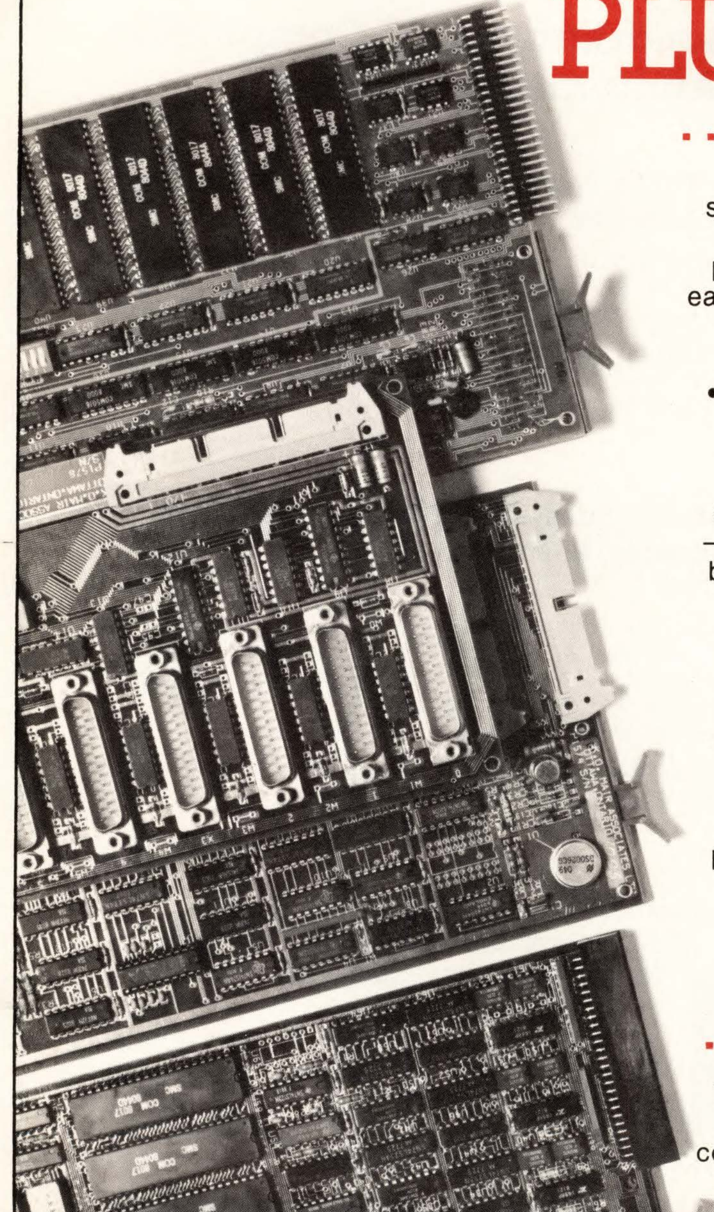
Another application of the T3051, TP3056 CODEC/filters is in the all-digital telephone. The analog and digital loopback test modes are particularly useful, enabling the switching system to verify the integrity of virtually the complete channel. The transmit op amp can be set for gains in excess of 20 dB, enabling a simple AC connection to an electret microphone (with integral FET buffer) to be made. A receive transducer with an impedance not less than 600Ω can be driven directly by the receive amplifier, with a resistive network providing gain adjustment and sidetone. Low impedance transducers require an audio matching transformer.

Both the TP3051 and TP3056 are housed in a 20-pin CERDIP package. These devices are available now in both sample and production quantities and are priced at $24.75 each in quantities of 100 and up. **Write 232**

Attention Data Communication Designers.
Free Samples . . .

National Semiconductor is offering a free sample of the CODEC to the first 500 designers who write in on their company letterhead. You must include a description of your application. Send your requests to:
Free Codec/Digital Design
National Semiconductor
2900 Semiconductor Drive
M/S 16250
Santa Clara, CA 95051

COMPATIBILITY PLUS...



. . . a DH11 for the LSI-11

The **DHK11** greatly enhances LSI-11/23 system performance by giving each terminal direct access to system memory. The processor need only service an interrupt for each block of data rather than each character transmitted. Some notable features of the DHK11 are:

• small size — single quad card or two dual cards • DH11 emmulation — supported by RSX11, RSTS and UNIX • Modular — 8 asynchronous ports per unit • 22 bit addressing for each of the 8 DMA channels — RS423 (RS232C) and RS422 interfacing on board • Software selectable line parameters and baud rates • Optional connector distribution panel • low cost per port comparible to a DLV11-J

The **DMK11** is a dual size board for LSI-11 systems. It provides full modem control for up to eight modems and is software compatible to Digital's DM11-BB modem controller. A distribution panel board is provided that combines the data signals for the DHK11 with the modem signals of the DMK11 into eight DP25P type modem connectors.

. . . a dual size DZV11 card

The **DZM11** is a four line serial asynchronous multiplexer for the LSI-11. It provides complete software compatibility with Digital's DZV11 plus:

• small size; one dual board half the size of the DZV11 • additional modem control; 7 signals per modem • split baud rates; independent receive and transmit baud rates can be configured • RS423 (RS232C) and RS422 capability • low power consumption.

For more information contact:

K.O. Mair Associated Limited,
145 Spruce Street, Ottawa, Ontario K1R 6P1
Telephone: (613) 238-7766 Telex: 053-4916

Digital is the registered trademark of Digital Equipment Corporation

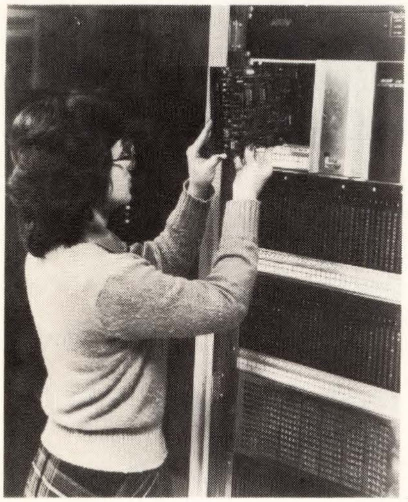
Write 70 on Reader Inquiry Card

Write 36 on Reader Inquiry Card

DATA PABX NETWORKING

With Interface Modules

The Micro600 Data PABX links local area networks together with a transparent "Interconnect Facility." The



networks span any distance and give users the ability to install local area networks at geographically dispersed locations or to fulfill the requirements of large single sites with thousands of terminals and computer ports. The Instatrunk480i T1 Local Multiplexor can provide up to 128 channels of a T1 communications link running at 1.544 Mbps. The Instamux470i, a plug-in version of the Instamux470 Local Multiplexor, can support up to eight asynchronous channels over the same two twisted-pairs conventionally used to support a single terminal. $600. **Micom Systems, Inc.,** 20151 Nordhoff St., Chatsworth, CA 91311.

Write 138

VIDEO SEQUENCE PROCESSOR

Digitally Records Images

The VSP is a computer system designed for the creation and processing of moving video sequences. It can digitally record up to eight minutes of moving image sequences on computer-accessible media in real-time; computer-process stored sequences or computer-generated image sequences frame-by-frame; and display these stored moving image sequences in real-time, slow motion, or still frame. The VSP records and plays back vid-

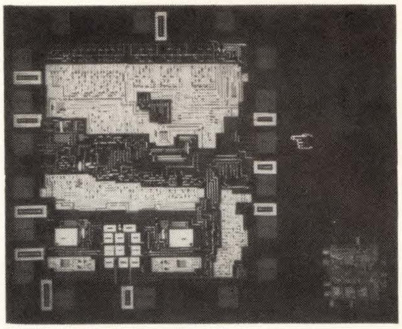
eo and graphic formats and has up to four workstations. Its applications include video animation, television post-production, video special effects, previewing film animation, and scientific modeling. $60,000. **PEL,** 635 Waverley St., Palo Alto, CA 94301

Write 135

GRAPHICS DISPLAY SYSTEM

Local Storage And Processing

The Model 8100/GS is a graphics subsystem with a locally executed software package called the LX/GP1 which enables local storage and processing of segmented display files. Its features include: *Segment/cell editing,* which allows the user to append or delete individual primitives within the cells; *Picking,* which refers to the ability to select a particular entity (segment, cell or primitive) for editing, inquiry or manipulation; and *Inquiry,* which allows the user to read back primitive and segment data for the purpose of keeping the host data base synchronized with the 8100/GS. The system utilizes a MC68000 μP and a Lexidata proprietary bipolar processor linked together by a DMA inter-



face. It is available in high resolution configurations and includes a 256-Kbyte RAM, four RS-232 serial ports and power-up diagnostics. \$15,950-\$21,850. **Lexidata,** 755 Middlesex Turnpike, Billerica, MA 01821.

Write 129

INTEGRATED WORK STATION

Emulates Popular CRTs

The video station features a 12″ etched green phosphor screen, 7 × 9 character display within a 9 × 12 ma-

trix, programmable screen attributes, 15 special graphics and 32 control character symbols, and a 93-key detached keyboard featuring 10 user defined function keys and 9 dedicated cursor control keys. Communication to the user-supplied boards is provided via an RS 232 or Current Loop interface. A 6-slot Multibus, or 14-slot STD-BUS card cage is standard and includes space for two 8″ storage devices. \$2375. **Psytek, Inc.,** 1900 Pickwick Ave., Glenview, IL 60025.

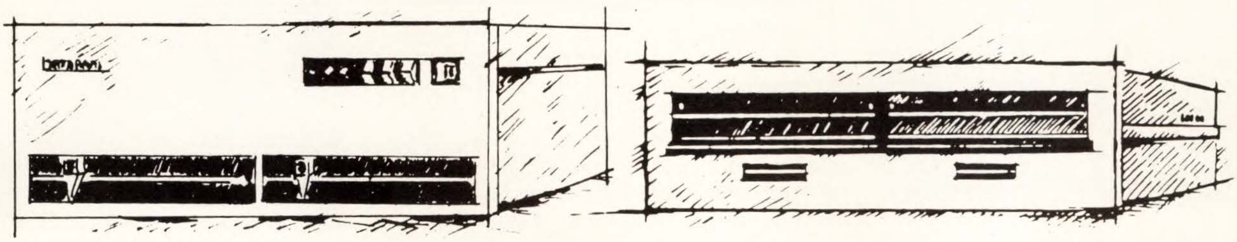
Write 136

MICROCOMPUTER SYSTEM

With Additional Storage Capacity

Three microcomputers, designated the 6221, 6231 and 6241, combine a 20.8-Mbyte Winchester disk drive with removable storage in one of three configurations: a one-Mbyte single floppy disk drive on the 6221,

DEC-COMPATIBLE DISKS FOR LESS



Dataram has acquired Charles River Data Systems' DEC-compatible product line. We will continue to offer their popular FD-311 dual floppy subsystems and have added an exciting new floppy-based system, Dataram's A21.

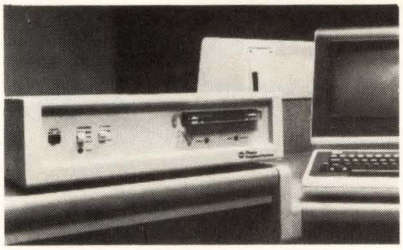
Q-bus and UNIBUS compatible versions of the FD-311 provide dual RX02-compatible 8″ floppy drives for $2,400. Our new 7″ high A21 combines dual RX02-compatible 8″ slimline floppies with an 8-quad slot Q-bus card cage for only $3,500. Both products are supported by the industry's widest range of LSI-11 compatible products. Call or write for details.

DATARAM

Dataram Corporation □ Princeton Road □ Cranbury, New Jersey 08512 □ Tel: 609-799-0071 □ TWX: 510-685-2542

Write 56 on Reader Inquiry Card

New Products



dual one-Mbyte floppy disk drives on the 6231 and a 20-Mbyte ¼" tape cartridge drive on the 6241. The standard microcomputer configuration includes: a multifunction module, 256 Kbytes of main memory, dual-wide 9-slot backplane, EIA cable and input and backup via single or dual floppy disk drives or a streaming tape cartridge. $10,255–$11,760. **Plessey Peripheral Systems,** 17466 Daimler Ave., Irvine, CA 92714. **Write 134**

PERSONAL CAD SYSTEM

With Automatic Photoplotting

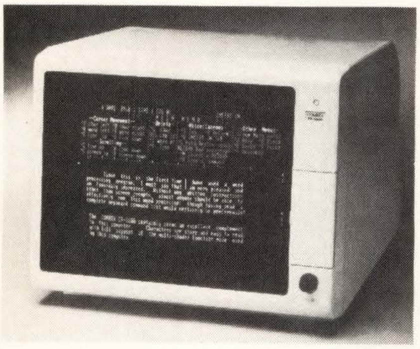
The Paragon 100 System is an interactive graphics system for printed circuit board design and manufacturing applications. It utilizes the 16-bit architecture of the LSI-11 minicomputer along with a proprietary graphics processor. The color monitor is a 14", 580 × 430, 7" color display and the system console is a 12" alphanumeric terminal with processors, memory,

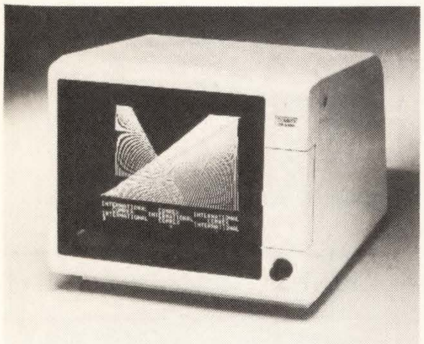
graphics, storage and interfaces. The user can design multilayer printed circuit boards of up to 14 layers and database modules are included for design rule checks (clearance, shorts, unconnects). The system has remote photoplotting and can be connected to additional peripherials such as pen plotter, papertape punch and printer. $39,950. **Paragon Technology Corp.** 421-5 N. Buchanan Circle, Pacheco, CA 94553. **Write 130**

DISPLAY MONITORS

For Personal Computers

The display monitors, Models CR-5400 and CR-5600 are the first offerings in a new line from Comrex. Model CR-5400 is a 9″ monitor with a





resolution of 800 lines/in and is designed for portable computer applications. Model CR-5600 is a 12″ monitor with a resolution of 1000 lines and is suited for desktop computer applications. Both monitors are offered with a choice of three image colors on an antiglare tube. CR-5400—$200. CR-5600—$230. **Comrex International, Inc.,** 3701 Skypark Dr., Torrance, CA 90505. **Write 166**

OEM PANEL PRINTER

Byte Serial Port

The 6620 μP-based printer features a Centronics byte serial port and a μP that can be factory-programmed for graphics capability or custom tailored for OEM applications. Its type is 5×7 dot matrix, 1, 7mm × 2, 4mm, and the user can select double high, double wide, and double high and wide fonts. A switch or control character provides provides first-line-up or first-line-down printing. Impact head prints 0.9 lines/sec. The 24-column printer is panel mounted and features a word-wrap switch which enables the user to eliminate split words or num-

bers on lines exceeding 24 characters. Type is left-justified and data continues on next line. Panel cutout is 4.50″×2.78″; depth is 9.00″. Adaptors fit the new 6620 to DIN 72×144 without modification. Standard power is 5V DC. **Digitec Corp.**, 918 Woodley Rd., PO Box 458, Dayton, OH 45401. **Write 176**

New Products • PERIPHERALS

DATA MODEM

With Auto Dialer

The PC212A is a Bell compatible 212A modem for use in the IBM Personal Computer. An auto dialer

stores up to 10 telephone numbers and the modem operates up to 300 bps asynchronously in the low speed mode or 1200 bps synchronously or character asynchronously in the high speed mode. Features include an EIA RS-232C asynchronous serial interface port and an internal μP which allows control, operation and optioning of the modem from the IBM PC keyboard. A user-friendly HELP list of commands is stored in the modem memory for instant screen display. The modem memory is battery protected. In the event of power failure or voluntary disconnection for relocation purposes, the numbers and options are protected. $495.00. **Rixon Inc.**, 2120 Industrial Pkwy., Silver Spring, MD 20901. **Write 173**

DIGITAL PROCESS RECORDER

30 Analog Channels

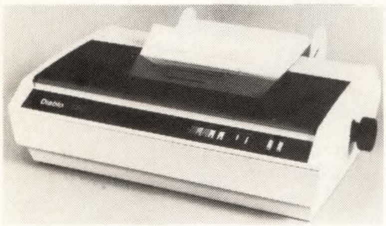
The DPR 1500 Digital Process Reporter is a high speed, multi-channel μP-based instrument for both manu-

facturing and laboratory testing applications. The recorder features 30 analog channels with built-in signal conditioning and digital displays that show channel number, process variable value and engineering units. The dot matrix print head has a speed of 170 characters/sec. Printing occurs in both directions of print head travel. The recorder can be configured for four ranges, extendable to a maximum of eight with a remote switching option. **Honeywell Inc.** M.S. MN/12-4118 (PCD-PA/62) Honeywell Plaza, Minneapolis, MN 55408. **Write 168**

INK JET PRINTER

For PC Applications

The four- and five-pass, 20 character/sec ink jet printer features switch-se-



lectable uni- and bidirectional printing capabilities and integrates both text and graphics on cut sheet or roll paper in seven colors. For graphic color applications, the printer places 120 dots/in, 1,024 by 1,024 dots/page in four minutes. It has a 16-nozzle head and can generate color backdrops, halftones, multiple color intensities, and complimentary imaging. $1,250. **Diablo Systems Inc.,** 2450 Industrial Blvd., Hayward, CA 94545. **Write 164**

OEM PRINTER

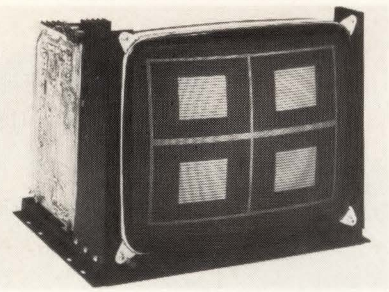
Prints 3 Lines/Sec

Model EX1601 is an OEM printer that can print at 3 lines/sec. It prints the full 96 character ASCII set on 8½" paper with an additional 128 symbols and foreign language characters. The printout is software selectable for an 80, 40 or 27 column wide format. A choice of standard parallel, RS232C and 20mA serial, or IEEE-488 interface is available. **Axiom Corp.,** 1014 Griswold Ave., San Fernando, CA 91340. **Write 165**

CRT MONITORS

For Graphics And Workstation

The CRT monitors are designed for the graphics, workstation, and composition systems of OEMs. They fea-

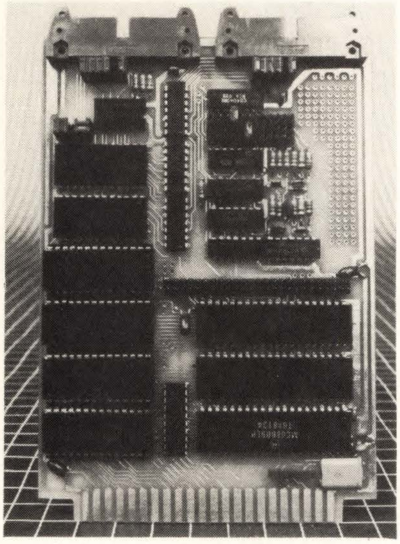


ture 15", 17", and 19" diagonal CRTs with 1100 visible lines at a 60Hz noninterlaced refresh rate and a choice of 70MHz or 120MHz video amplifiers. The 70MHz video amplifier accepts TTL, linear, or ECL levels while the 120MHz video amplifier interfaces to differential ECL. Vertical refresh rates of up to 90Hz, interlaced or noninterlaced are available. Horizontal rates from 30kHz to 65kHz may be ordered. Included on all monitors are a stator yoke, regulated high voltage, and dual axis dynamic focus to deliver minimum deflected spot growth and consistent resolution across the entire screen. Monitors may be ordered with any Jedec phosphor, contrast enhanced faceplates, and anti-reflection coatings. PX15 (15" CRT)—$685, PX17 (17" CRT)—$767, PX19 (19" CRT)—$799. **U.S. Pixel Corp.,** 125 Irving St., Framingham, MA 01701. **Write 160**

SINGLE-BOARD MICROCOMPUTER

For Instrumentation

This single-board computer based on the Motorola 6809 μP is designed to be used in applications such as dedi-



cated control, protocol conversion, instrumentation, communications, and robotics. Built on a 4.5″ by 6.5″ card, the board contains the 6809, watchdog timer, real-time clock, two RS-232 serial ports, four parallel ports plus handshaking, and accommodates up to 64K bytes of RAM and EPROM. The 6809 Control Module is compatible with all of the Wintek I/O modules, including Serial I/O, Parallel I/O, IEEE-488, Driver/Sensor, Floppy Disk Interface, Analog Interface, Parallel Breadboard, Console I/O, Cassette, and Counter/Timer Modules. Additional memory is available using a ROM Module or CMOS RAM Module. $245. **Wintek Corp.**, 1801 South St., Lafayette, IN 47904. **Write 157**

MICROCODE DEVELOPMENT STATION

With 3 Serial I/O Ports

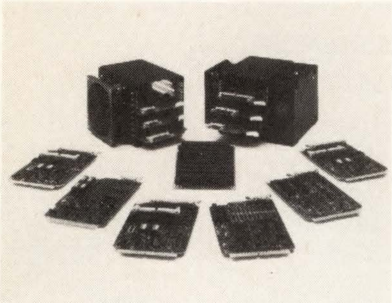
The STEP-7/FITS Firmware Integration and Test Station supports all microprogrammed designs, bit-slices, high speed controllers and digital signal processing circuits. High-performance μP designs get real-time support (to 36nsecs access times) from the memory and ROM emulation.

The station emulates high-speed memory, controls the target system clock and analyzes the logic state of the target. It is a single unit supported by a full sized CRT terminal and includes 6 slots (expandable to 10) for memory emulation and logic state analyzer boards. Two floppy disk drives and the CP/M operating system provide over 1.5 Mbytes of storage for code files, command files, machine state definitions and an on-line command summary. Three serial I/O ports are available to communicate with peripherals including a printer, a PROM programmer and a computer. $8,500–$60,000 depending on the amount of high speed RAM required. **Step Engineering**, 757 Pastoria, Sunnyvale, CA 94088. **Write 161**

STD BUS CONTROL CARDS

For Industrial Automation

The STD bus modular motion cards are designed to convert digital control data to analog drive signals; drive



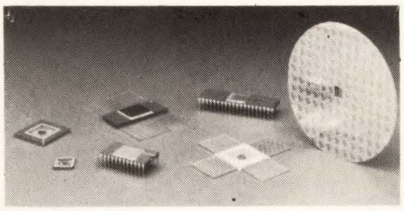
motor amplifiers; and position encoder and computer interface. They may be incorporated as subunits of existing equipment, or stand alone as self-contained systems. They are suited for industrial automation applications requiring digital data logging, machine monitoring, digital to analog servo control and other motion or process control applications. **Renco Corp.,** 26 Coromar Dr., Goleta, CA 93117.

Write 196

SCHOTTKY GATE ARRAYS

Bipolar Integrated

The Integrated Schottky Logic (ISL) configurable gate arrays consist of five array densities ranging from 836 gates with 48 I/O's to 2376 gates and 84 I/O's. They are designed with interdensity cell compatibility and topological uniformity permitting univer-



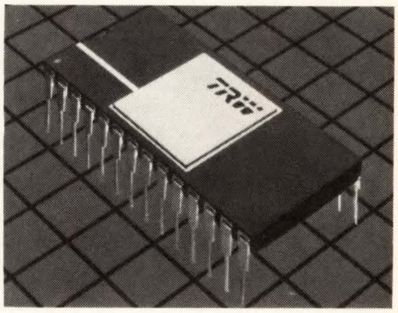
sal macrofunction and I/O designs. The typical gate propagation delay for all five arrays is 2.3nsec. A 1.8nsec enhanced version is available by selective hook-up of collector pull-up resistors that are available to each ISL gate. Power dissipation is 350 μW/gate, yielding a speed-power product of 0.8pJ. They are fully TTL compatible (8mA and 16mA drive current). The operating power supply requirements are V_{CC} = 5 and V_{BB} = 1.8. **Raytheon Semiconductor,** 350 Ellis St., Mountain View, CA 94040.

Write 206

FIFO MEMORY

TTL Compatible

This FIFO memory has a 15-MHz data rate and is useful in applications such as video time base corrections, A/D output buffers, input/output formatter for digital filters and FFT's, disk and tape certifications, voice syn-

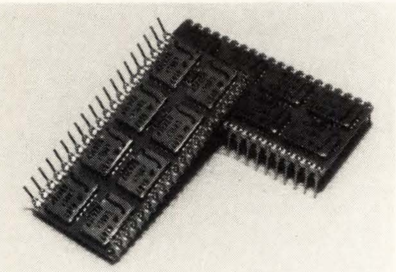


thesizers and medical ultrasound. The TDC1030J6 operates from a single 5V supply and has a fall-through time of 2 μsec. The 28-pin dual in-line package stores 64 words by 9 bits. Maximum power dissipation is 1.5 W. The FIFO is capable of expansion in both the word and bit dimension. \$38.00 in quantities of 250. **TRW LSI Products,** P.O. Box 2472, La Jolla, CA 92038. **Write 203**

CMOS MEMORY MODULE

For Aerospace Programs

The DP256KU is a 262,144 bit, high speed static CMOS RAM, which may be organized as 64K × 4, 32K × 8 or

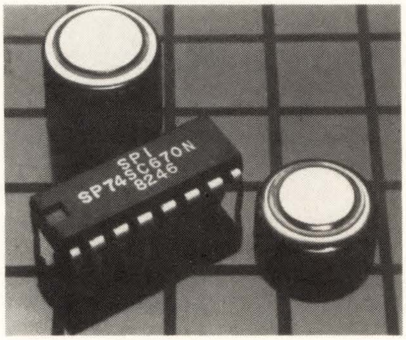


16K × 16. The module may be ordered in commercial, industrial or military grades with a -C, -I or -M suffix. -C and -I models use 100% screened components to the requirements of MIL-STD 883B Class C. -M units use components 100% processed in compliance with MIL-STD 883B, Method 5004 for highest reliability. Features include -M units that operate at -55°C to +125°C, the use of 16IDT 6167 16K × 1 CMOS RAMs and a high density 0.9 × 2.0″ 40-pin dual-in-line package. **Dense-Pac Development Ltd.,** 1588-A S. Anaheim Blvd., Anaheim, CA 92805. **Write 193**

REGISTER FILE

In High Speed CMOS

Designated the SP74SC670, the CMOS device is both speed and function compatible with its LSTTL ver-

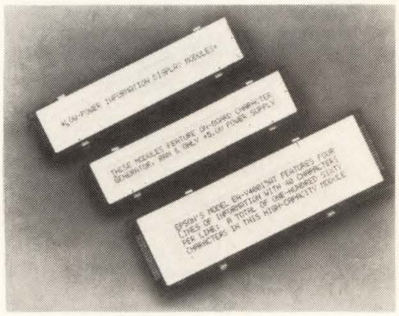


sion, and capable of interfacing directly with standard TTL logic levels. It requires 10 μW standby power (2μA at 5V). **Semi Processes, Inc.,** 1971 Capitol Ave., San Jose, CA 95132. **Write 194**

LCD MODULES

96 Character Display

Three modules feature 40, 80, and 160 characters in 5 × 7 dot matrix



formats which includes cursor. The modules, EA-Y40015AT (1 line × 40 characters/line), EA-Y400 25AT (2 lines × 40 characters/line), and EA-Y40040AT (4 lines × 40 characters/line) have character heights of 0.189″

and can display 96 ASCII characters. The modules feature row and column drivers and a Data RAM and Display Data controller. A +5.0V power supply is required and the units can be interfaced with μPs. **Epson America, Inc.,** 3415 Kashiwa St., Torrance, CA 90505. **Write 187**

BINARY COUNTER

Prescaler Function

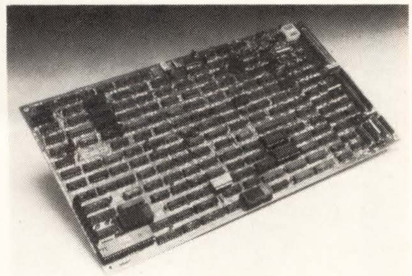
The MC10H016 is an ECL binary counter which is pin-compatible with

the Fairchild F10016. It has a counting frequency of 200 MHz and is processed on an oxide-isolated process called MOSAIC. The MC10H016 is compatible with the Motorola MECL III, Macrocell Arrays and MECL 10K series. Its applications include instrumentation and automatic test equipment and real-time purposes such as speed-to-time and time-to-distance conversions. The counter can also be used as a prescaler and as a control to keep track of the present state in small finite state machines. \$16.07–\$17.66. **Motorola,** P.O. Box 20912, Phoenix, AZ 85036. **Write 201**

SINGLE-BOARD CONTROLLER

With Data Separators

The C163 is a single-board intelligent controller that links the D160 24-track 160 Mbyte ½" streaming tape drive to a host processor and to two 8" or 14" SMD-compatible Winchester disk drives. It supports transfer rates up to 1.2 Mbytes/sec (8 MHz) across a SASI bus and off-line non-stop streaming file backup and restore at tape speeds of 90 ips (Model C163-90) or 130 ips (C163-130). The controller features two integral data separators for tape and disk, and on-board error-correction and control. The C163 supports direct file copy between disk drives, and automatic tape

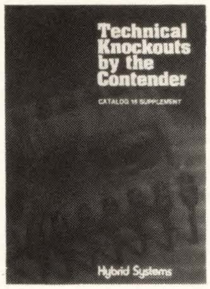


read/write error correction during backup. It handles disk formatting, head seeks, recalibration, local sector buffering and overlapped seeks. \$1295 in quantities of 500. **RossComp,** 16643 Valley View Ave., Cerritos, CA 90701. **Write 191**

Errata

The Portable Computer Buyers' Guide in our March issue contained two errors: Teleram's portable computer lists for \$2995 and not \$4995 as stated. Also, the Zorba computer from Telcon Industries now lists for \$2195, and not \$1595.

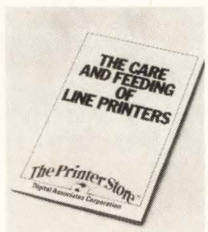
New Literature



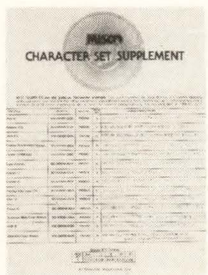
Components Catalog. The 40-page catalog supplement by Hybrid Systems describes in detail their line of monolithic, hybrid, and modular data converters. The product line includes A/D, D/A converters and programmable operational amplifiers. These devices are designed for measurement, control, and instrumentation applications. The devices are available in three temperature ranges: 0 to +70°C, −25°C to +85°C, and −55°C to +125°C.
Hybrid Systems **Write 264**

Data Acquisition Catalog. ADAC's catalog of A/D, D/A and digital data conversion LSI-11 bus interface products covers new products such as the BASYS integrated data aquisition and control system for inexperienced users. Also featured are the Model 3200 Falcon's Nest compact backplane, Series 1200, 2200 and 3200 full quad and half quad bus enclosures, Model 18MP RAM boards and RTD, load cell and strain gauge accessory panels.
Adac **Write 257**

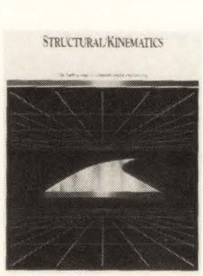
Electronics And Telecommunications Catalog. The catalog features 118 pages of tools and equipment for electronics, telecommunications, field service, and labs. Divided into 9 sections, it covers a line of wire-wrapping and testing tools, wire and cable, assembly products and aids, including N/C wire wrapping machines and support systems.
OK Industries **Write 258**



Line Printers Booklet. "The Care & Feeding of Line Printers" is a summary which covers thirteen aspects of line printer operation, and offers hints and facts about duty cycle, site environment, temperature, static, dust, power supply, ribbons, paper, printer service and maintenance, printer selection, and how to make a printer last longer.
The Printer Store **Write 254**

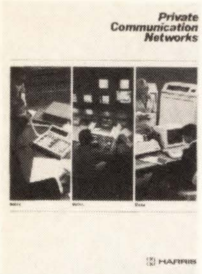


Daisywheel Brochure. This catalog lists character sets of 80 daisywheel and thimble print elements. MISCO offers printwheels from Qume and Diablo, thimbles from NEC plus compatible printwheels for Qume, Diablo and Xerox. The character sets are printed in actual size, showing sample letters and numerals plus symbol representation in the actual sequence they appear on the print element. They range from commonly used typefaces to foreign languages.
Misco **Write 255**

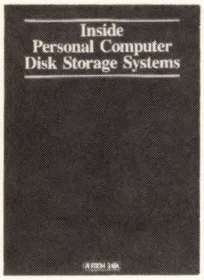


CAE Brochure. This brochure includes descriptions of the services and software products in the CAE field. It explains how computer-aided technology analyzes and improves a design before the user builds a prototype. At the prototype stage, computer-aided analysis and testing methods can be applied to design and manufacturing methods.
Structural Kinematics **Write 256**

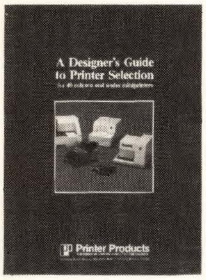
New Literature



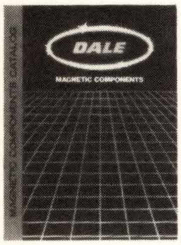
Communications Network Brochure. Focuses on the economics, technologies and available systems for private networks. Titled "Private Communications Networks," it covers the reduced costs and improved service benefits available to organizations with annual telecommunications expenses of $1 million or more, and gives examples of actual installations employing various communication technologies.
Harris Corp. **Write 262**



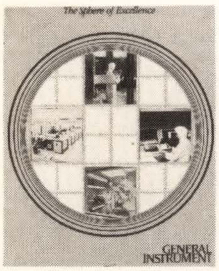
Disk Drive Booklet. "Inside Personal Computer Disk Storage Systems" is an overview of personal computer disk storage systems, both floppy and hard. The introductory manual covers disks, drives, controllers and operating systems.
Percom Data **Write 253**



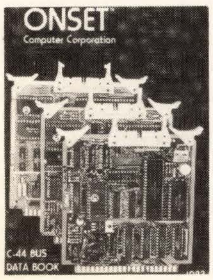
Printer Guide. The guide was written to help OEM and end user system designers to select appropriate alphanumeric dot matrix roll, slip/document, and label mini-printers. It describes six printer series with 27 and 40 column capacities. Products include roll printers for point-of-sale systems and data logging; slip/document printers for document validation and inventory control; and label printers for parts "kitting" and pharmaceutical applications.
Printer Products **Write 251**



Magnetic Components Catalog. Dale Electronics offers a 48-page book on magnetic components that includes both standard and special products, and has sections on switch mode magnetics and custom inductive products. The catalog covers axial lead and toroidal inductors as well as high current filter chokes. Specifications are provided.
Dale Electronics **Write 260**



Microelectronics Quality Brochure. This brochure by the Microelectronics Group of General Instrument Corp. describes the quality and reliability of their LSI microcircuits. The publication summarizes the various programs, especially the 12-point Quality Program and a 6-point Reliability Program employed by the company to test product quality.
General Instrument **Write 268**



C-44 Bus Data Book. The C-44 bus computer cards described in this booklet are designed to be used in systems where minimum power consumption is an important consideration. The 35 page book describes Onset Computers' single board computers and their features, which include two low power modes, 27C16 CMOS EPROMS, 6116 static RAMs, a fully buffered bus and current sense resistors.
Onset Computer Corp. **Write 250**

Calendar

July 4–5

Optical Imaging Systems Meeting. International Conference Center, Kobe, Japan. Contact: Dr. Ichiro Kitano, Nippon Sheet Glass Co. Ltd. 1. Kaido Shita Konoiki, Itami, Hyogo 664 Japan.

July 8

System Documentation Seminar. Seattle, WA. Contact: TCA, 1250 Oakmead Pkwy., #210, Los Angeles, CA (800) 792-0990.

July 9–12

NCC Board Conference. Las Vegas, NV. Contact: Ann-Marie Bartels, 1815 N. Lynn St., Arlington, VA 22209. (703) 558-3641.

July 11–13

Summer Computer Simulation Conference. Hyatt Regency, Vancouver, B.C., Canada. Contact: The Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. (714) 459-3888.

July 11–15

Digital Signal and Image Processing Course. Washington, DC. Contact: Integrated Computer Systems, 3304 Pico Blvd., Santa Monica, CA 90405. (213) 450-2060.

July 13–15

Computer Graphics. Los Angeles, CA. Contact: PR Dept., NIMR Seminars, PO Box 3727, Santa Monica, CA 90403. (213) 450-0500.

July 17–22

IEEE Power Engineering Society Summer Meeting. Los Angeles Hilton, Los Angeles, CA. Contact: Robert L. McMillen, Los Angeles Dept. of Water and Power, PO Box 111, 11 N. Hope St., Los Angeles, CA 90051.

July 17–20

IEEE Nuclear & Space Radiation Effects Conference. Sheraton Gatlinburg Hotel, Gatlinburg, TN. Contact: James Gover, Saudia National Laboratories, Div. 2155, Albuquerque, NM 87185.

July 24–26

Optical and Video Disk Systems. Monterey Bay, CA. Contact: Richard Murray, IGC, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

July 24–29

Siggraph '83. Detroit, MI. Contact: Siggraph '83 Conference Office, 111 E. Wacker Dr., Chicago, IL 60601. (312) 644-6610.

July 25–28

Softfair. Hyatt Regency, Crystal City, Arlington, VA. On Software Development: Tools, Techniques and Alternatives. Contact: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

August 7–9

Advances in Impactless Printing. Monterey Bay, CA. Contact: Richard Murray, IGC, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

August 7–11

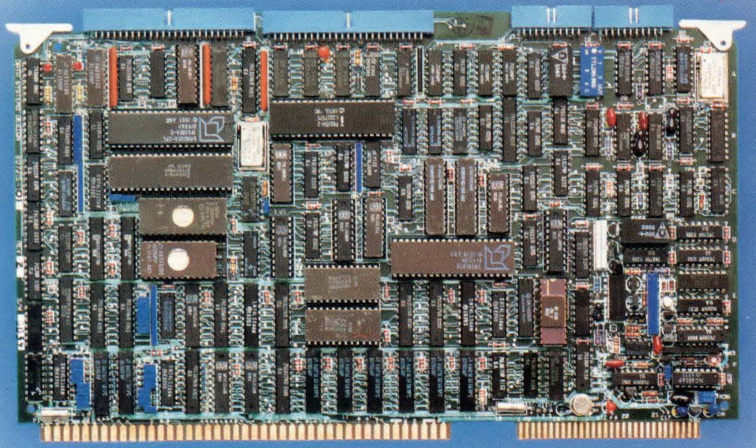
International Computers in Engineering Conference and Exhibit. Chicago, IL. Sponsored by the Computer Engineering Division of the American Society of Mechanical Engineers. Contact: Mary S.H. Benedict, ASME, 345 East 47th St., 13 M, New York, NY 10017. (212) 705-7100.

August 14–16

Multi-Media Teleconferencing. Andover, MA. Contact: Richard Murray, IGC, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

Advertiser Index

ONE SLOT SHOPPING.



INTRODUCING THE WINCHESTER/FLOPPY/TAPE THREE-IN-ONE MULTIBUS CONTROLLER.

Try this on for size.

DSD's new 7215 single-board Multibus® controller/interface handles two SA1000-type 40Mb Winchesters, a 1/4″ streamer, and two 8″ floppies.

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The 7215 and 5215 are the highest performance controllers on the market for 8″ and 5 1/4″ drives.

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And like all DSD products, our Multibus boards and systems are supported by our exclusive Rapid Module Exchange™ and regional service centers.

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Compare our incomparable Multibus boards and systems to anything else you like. To make it easy, just send your business card to DSD Corporate Headquarters, Marketing Communications Department, for a free copy of "The Multibus Buyers Guide."

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