

DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

JUNE 1985

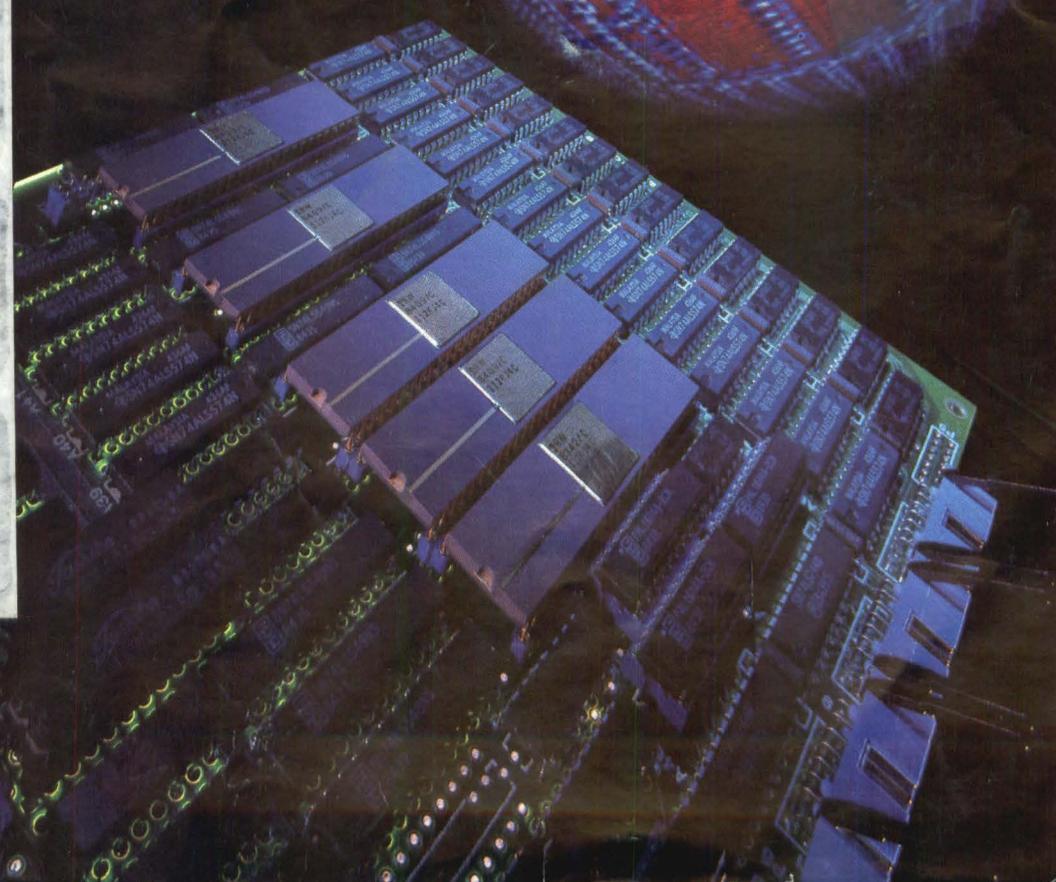
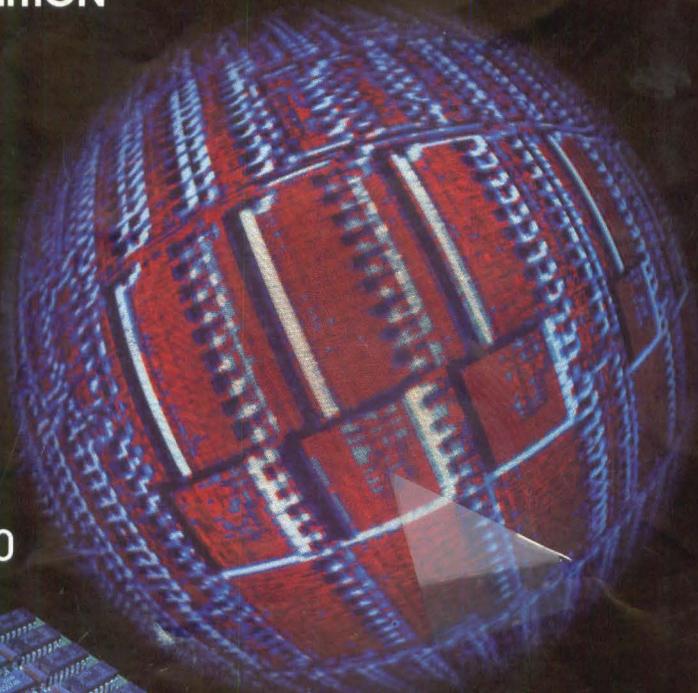
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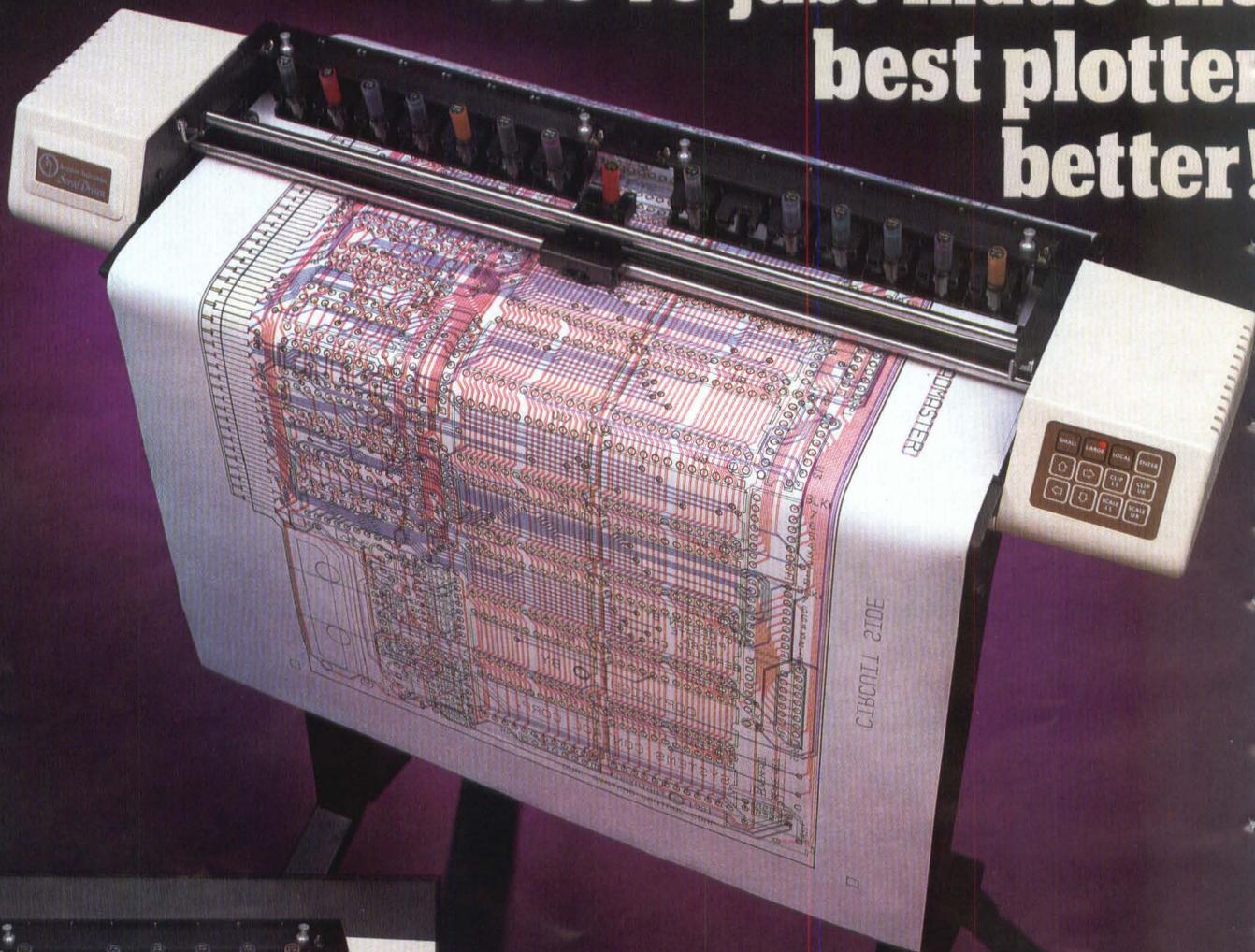
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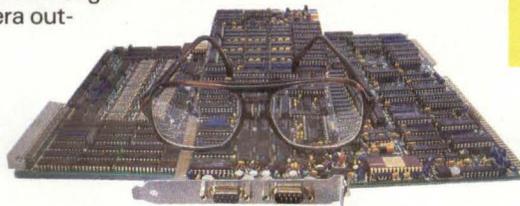
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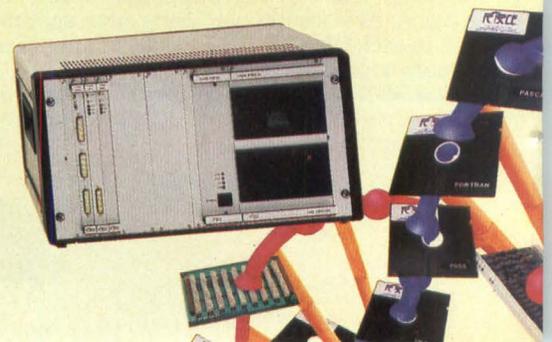
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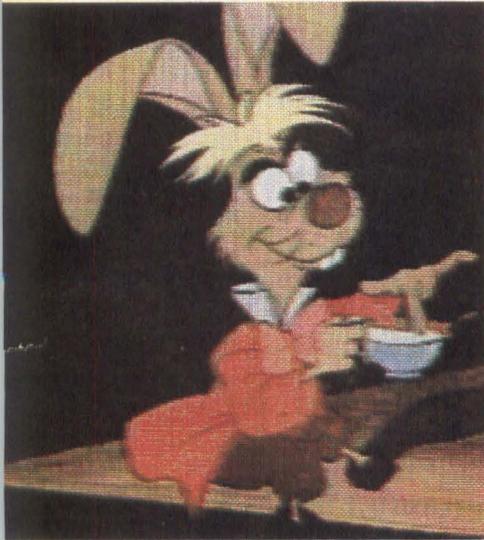
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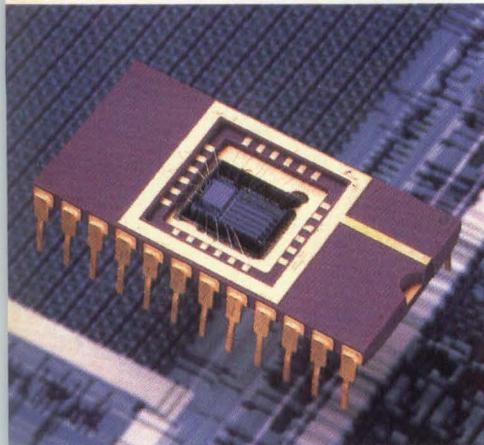
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Published monthly thirteen times a year with two issues in November. Subscription rates for non-qualified subscribers (US and Canada) — \$40/yr; foreign — surface mail — \$50/yr; airmail — \$85/yr. Single copies — \$4. Copyright 1985 by Morgan-Grampian Publishing Company, 1050 Commonwealth Ave., Boston, MA 02215. Second class postage paid at Boston, MA and at additional mailing offices. POSTMASTER: Send address changes to Morgan-Grampian Publishing Company, Berkshire Common, Pittsfield, MA 01201 ISSN 0147-9245.

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Machine vision is using faster architectures for color and gray scale processing.



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by Hugh Aldersey-Williams

The extended range of applications for machine vision systems is made possible by advances in the technology of the sensors and processing architectures used.

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by Brita Meng

Whether a speech recognition system is speaker-independent or speaker-dependent, isolated or continuous, the problem of recognition remains the same: how to develop a machine which emulates the way humans interpret speech.

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by Paul Brokaw

Of the various methods used for digital speech synthesis, pulse code modulation (PCM) is probably the most flexible.

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by Ronald Collett

While CMOS has made tremendous inroads in the past few years, TTL and ECL logic families are not likely to disappear.

72 **Effects Of Pipelining On Algorithms In The MC68020**

by David Olsen

In the past, the performance of an algorithm on a microprocessor was determined by how fast the processor ran and how many instructions the algorithm required. This has been changed by the advent of pipelining found in today's 32-bit microprocessors.

DESIGN TOOLS

75 **Advanced Microprocessors Demand High-Level Language Support**

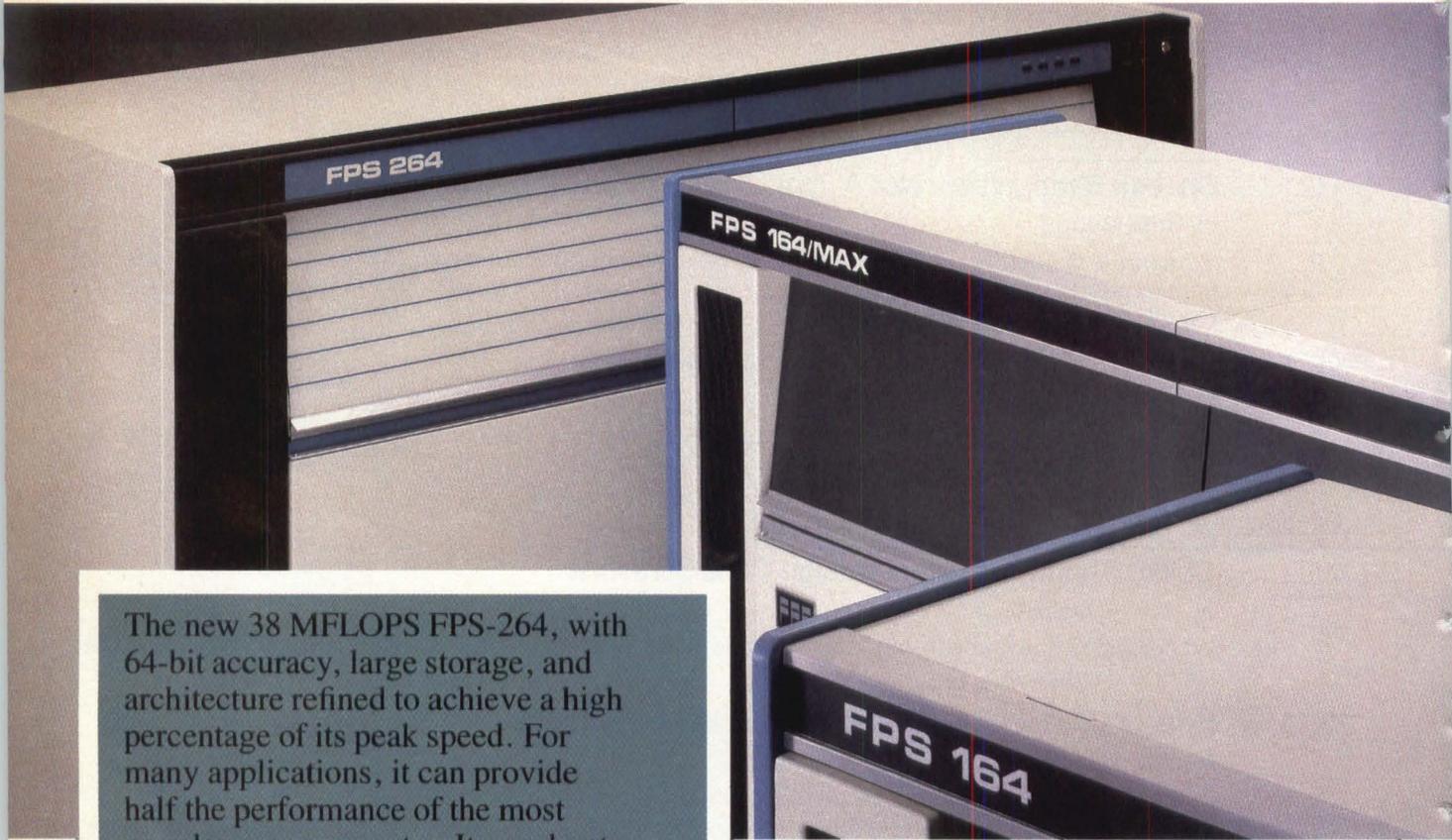
by Joe Aseo

Microprocessor software development has changed in character from individual programmers working on a monolithic piece of code to teams of programmers working on individual modules for later integration into a larger program.

ON THE COVER

A modular approach to machine vision hardware provides designers with increased system flexibility and expandability. Datacube's MaxVideo line of vision hardware modules includes VFIR, shown on the front cover, a real time 10-point image processor. Improved digital video interconnect design allows for operation in harsh environments. Gloria Simmons created the color enhanced VFIR image using a northwest directional filter. Photography by Steve Grohe.

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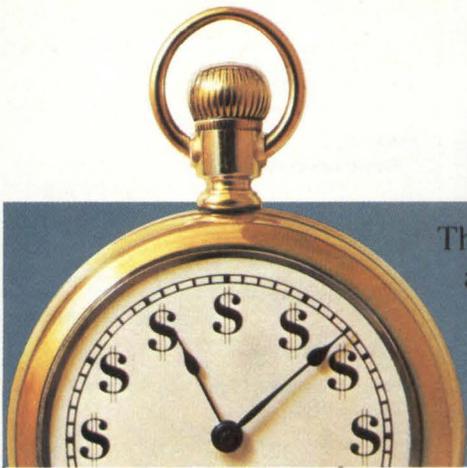
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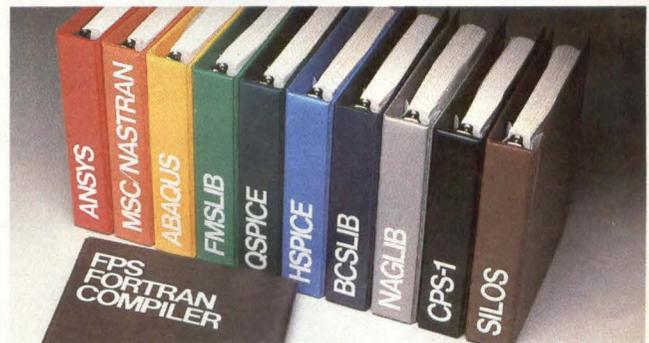


The FPS optimizing FORTRAN-77 Compiler lets you easily adapt code to FPS' pipelined architecture in a form that is nearly as efficient as hand-coded assembly language. With extensions for asynchronous I/O and for enhancing compatibility with other compilers, it is one of most comprehensive tools of its kind.

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Word size	64 bits	64 bits	64 bits
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Maximum disk storage capacity	16 Gbytes	3 Gbytes	3 Gbytes
Precision	15 decimal digits	15 decimal digits	15 decimal digits
Vector registers	4 x 2K	124 x 2K (max.)	4 x 2K
Scalar registers	64	184 (max.)	64
Host interfaces	IBM, DEC	IBM, DEC, Sperry, Apollo	
Program Development Software	FORTRAN Compiler, Overlay Linker, Assembler, Object Librarian, Interactive Debugger.		

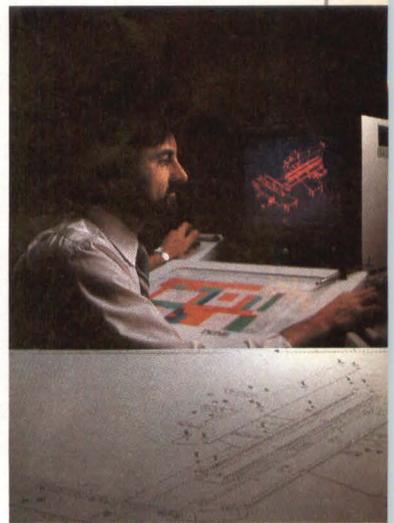
Family Performance Measures

	FPS-264	FPS-164/MAX	FPS-164	
Peak MFLOPS	38	15 accelerators 341	1 accelerator 33	11
Peak MOPS	190	1705	165	55
Peak MIPS (Instructions are multi-parcel)	19	5.5	5.5	5.5
Typical MFLOPS, LINPACK Benchmark	9.9	20.0	6.0	2.6
Whetstones, KWIPS (64-bit)	19,000	5440	5440	5440
1000x1000 matrix multiply, seconds	53	10	66	189
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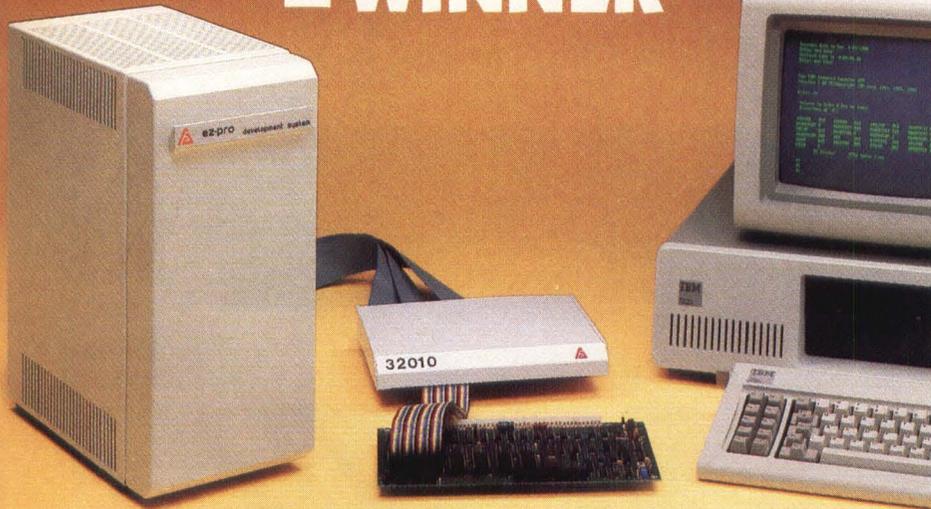
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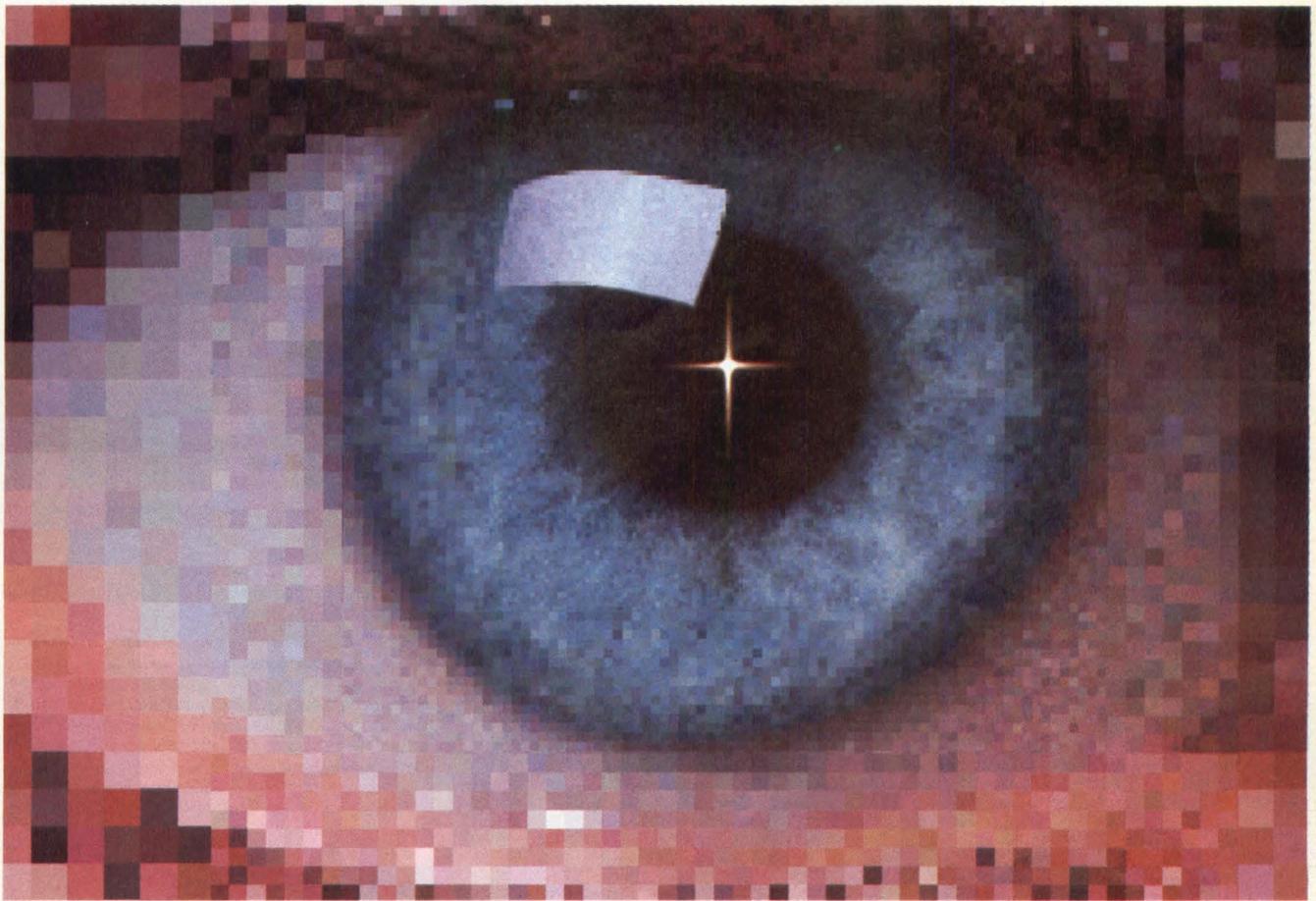
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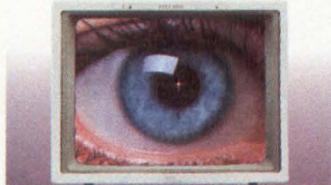
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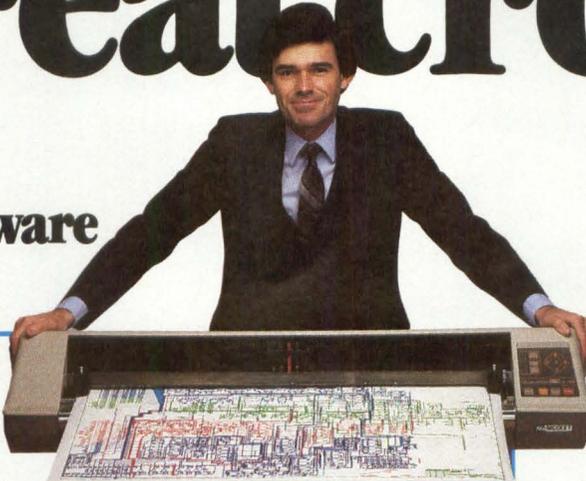
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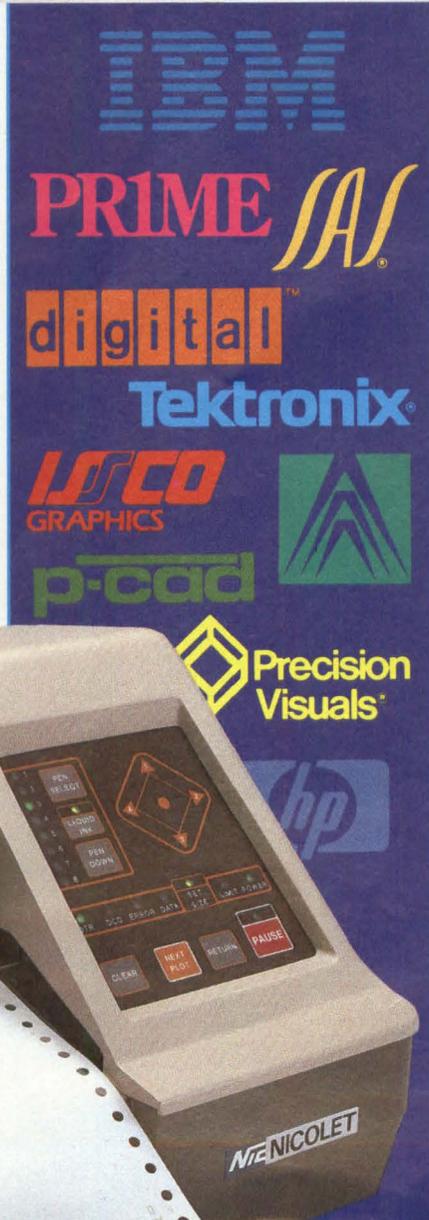
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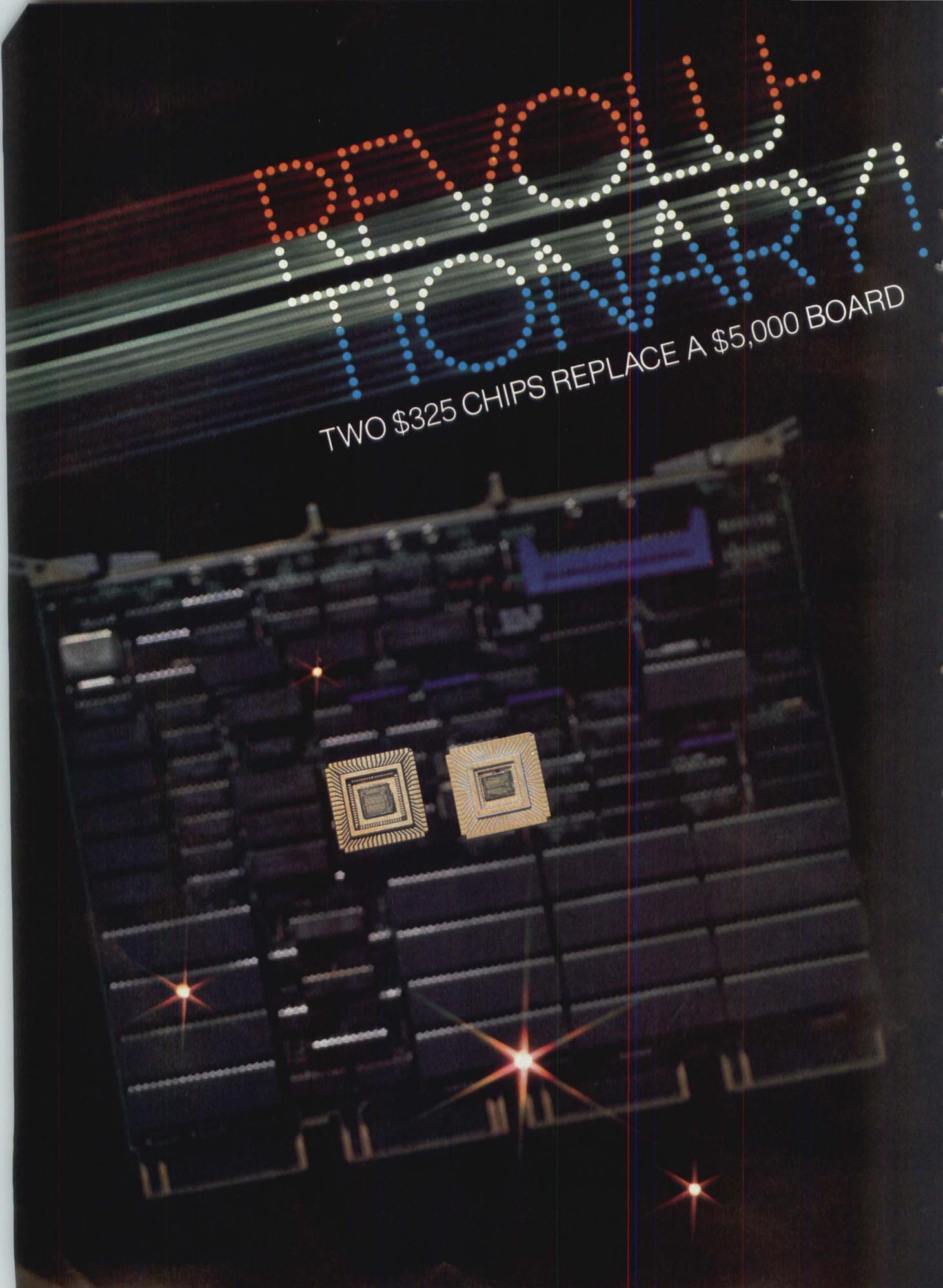


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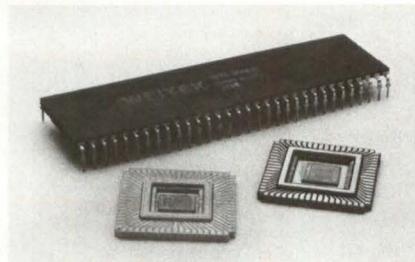
If your design specialty is instrumentation, graphics, telecommunications, CAD, CAE, aerospace or mini/micro applications, you'll want to use these powerful tools for faster, smaller designs while lowering your overall system costs.

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Available on leadless chip carriers and 64-pin DIPS for even lower power-consumption and broader interfacing alternatives, the new chips undergo an exhaustive proprietary burn-in process that assures reliable performance.

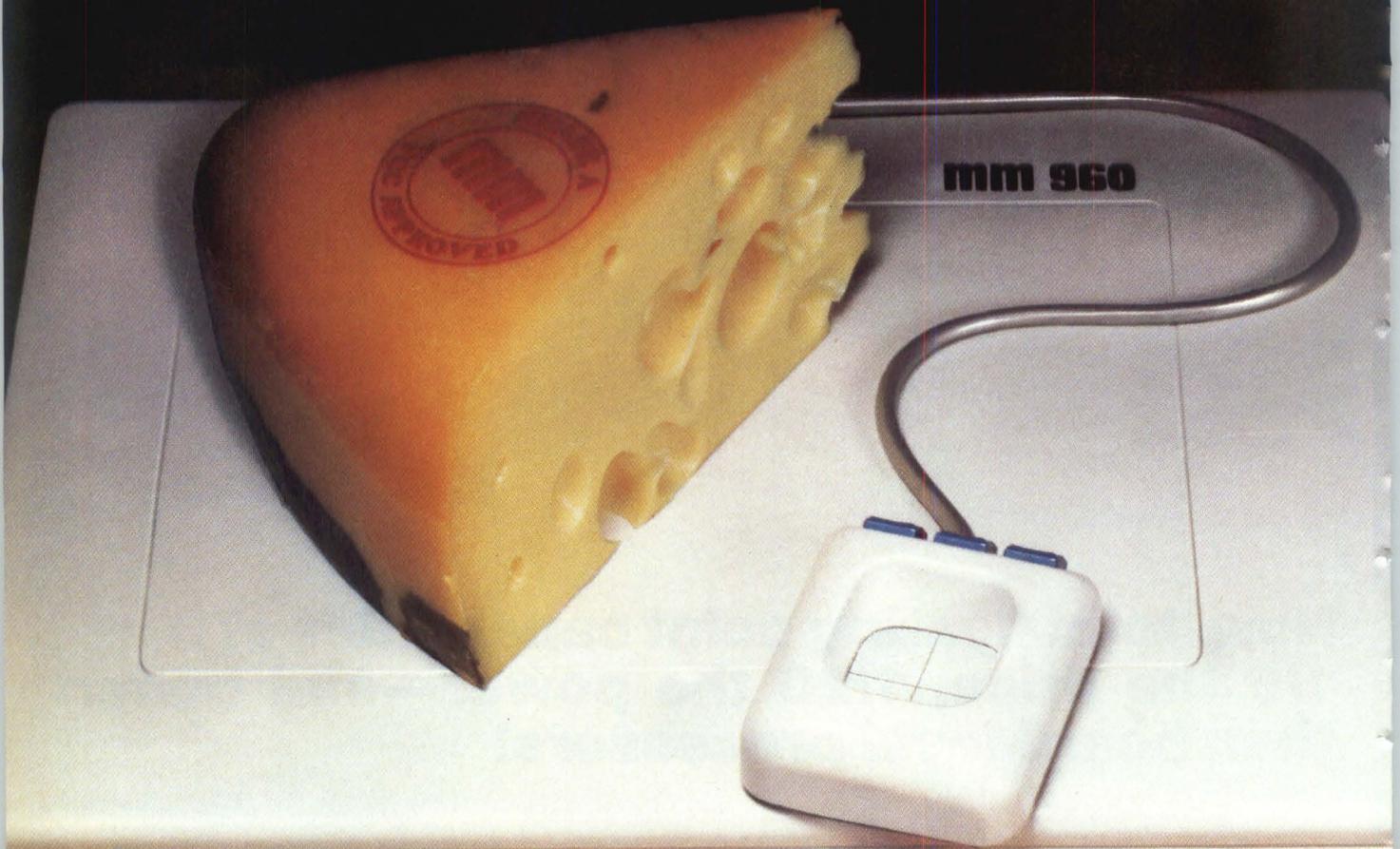
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EDITOR'S COMMENT

My Dog And AI

As the commercialization of artificial intelligence techniques takes hold, many in the field question whether AI can live up to its overblown promise. There is disagreement about what the term artificial intelligence means, although most researchers would include machines that merely appear to think. (The Turing Test?) Perhaps we should crawl before we run and try to model nonhuman intelligence first — my dog for instance. Although he's not very intellectual, he can accurately sort through thousands of smells, catch a ball in midair, and so on. He is also friendlier than most computers.

Obviously, this whole notion of intelligence remains slippery because it is based on subjective assessments. We don't really know what intelligence is or how to describe it to a computer so that it can be emulated. Instead we must be content to nibble away at the edges of the problem.

Human expertise, ironically, proves to be easiest to model. Common sense and tying shoelaces are harder to deal with. That's not surprising since expert behavior is most likely to be codified in formal rules, inferences, rules of thumb and common sense criteria that tell when to override the rules. Despite that, it's not easy to pull all this out of an expert so that an expert system can be programmed. Once built, however, such a system only represents artificial intelligence of a crude sort — more of an electronic idiot savant than human-like intelligence.

Designing real machine intelligence may take far longer for there are serious sensory input problems that must be dealt with. For example, global, pattern recognizing vision is an important input because so much of our information comes to us visually. But, visual pattern recognition is not necessarily intelligence (my dog does it quite well), although it's a necessary input. Perhaps even harder is natural language recognition with all its ambiguities. It's hard because we don't know how we do it. We can build systems that recognize a limited number of words or phrases from a limited number of speakers. In this technology my dog isn't much better than the more sophisticated systems on the market.

Such sensory input systems will have to be well developed before we can build artificial intelligence systems that exhibit that one universally agreed upon sign of intelligence — the ability to learn. We use our senses to acquire information and our intelligence to sift through, categorize and store it. A machine that only knows what we tell it can't really be classified as intelligent by human standards. It must be able to adapt to new situations and learn from mistakes, as even a dog can do.

AI techniques, as they presently exist, have the ability to solve problems that don't easily yield to conventional approaches. As we solve more difficult problems, we will undoubtedly learn more. So the correct approach may just be to solve increasingly intractable problems, inventing the necessary incremental techniques as we go along. This is the approach that the AI industry will almost certainly use. It should result in much more powerful hardware. According to Richard Morley and William Taylor of Gould Inc., today's supercomputers can process roughly about the same amount of information as a mosquito or bee. They need to be about 10,000 times more powerful to reach the chimpanzee level and perhaps a bit more for humans. Such computing power could be available by the year 2000, given the present rate of advance in silicon.

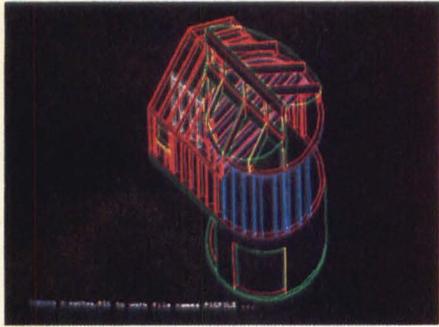
Availability of such massive computing power, however, will not guarantee the existence of human-like artificial intelligence. It will primarily be software that determines the rate of AI advancement. Conversely, AI software advances will cause hardware architectural changes that permit more efficient computing — as it already has in the case of LISP processors.

The main problem is not lack of hardware or software but lack of insight. AI companies will make improvements in hardware and software that will advance the state of the art. But a real understanding of intelligence must continue to come from the research community because there remain fundamental questions. We need to understand how we learn. We also must understand common sense — that ability to make decisions when rules and information are incomplete. For true intelligence we must also consider the nature of consciousness and self-awareness and find ways to copy such abstract concepts in our machines.

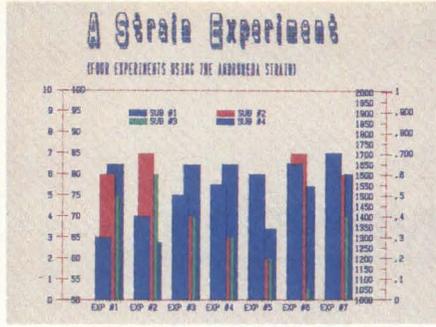
Meanwhile, I'll be happy if we can build some helpers that are just a bit more competent and reliable than my doctor, plumber or mechanic — and at least as user friendly as my dog.

— John Bond, Editor in Chief

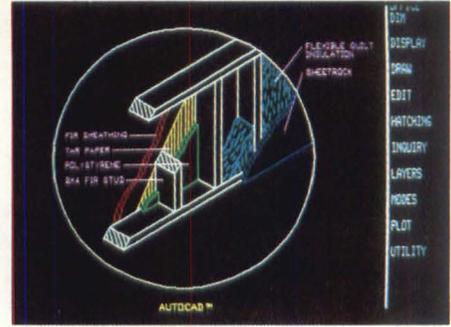




1. High Speed (MicroCAD Software)



2. Dual Display Modes (Energraphics Software)



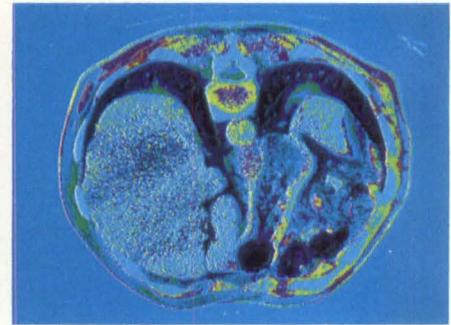
3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

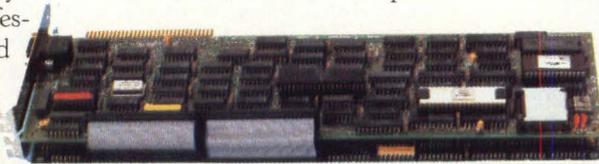
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HOTLINE

TOTAL SYSTEM SIMULATION AT 1 BILLION EVENTS/SEC The System Development Engine from Zycad, to be available early next year, will be able to simulate up to 1.5 million gates at 1 billion events/sec. Interfaced with VAX, IBM or Apollo computers, the engine will simulate a complete system, including software.

WE32100 32-BIT MICROPROCESSOR OFFERED COMMERCIALY AT&T has announced the seven-chip family of 32100 processor and six peripherals in 1.5 μ m CMOS.

1-MBIT CMOS EPROM TO BE IN PRODUCTION THIS SUMMER AMD has announced that quantities of its 1-Mbit CMOS EPROM will be available by the end of the summer. The Am27C1024, organized as 64K \times 16, contains a special user feature called two-word programming that allows the part to be programmed 32 bits at a time.

MULTIBUS 286 SBC TO COMPETE WITH INTEL In direct competition with the Intel line of single-board Multibus computers, Metacomp has announced the MPA-1000, a 286-based CPU board with up to 2 Mbytes of memory that supports the iLBX private memory interconnect.

FOUR CMOS VIDEO D/A CONVERTERS DEBUT Brooktree Corp. will announce a 50 MHz triple 8-bit D/A converter, a single 75 MHz 8-bit converter and a 75 MHz triple 4-bit D/A converter. Analogic has also announced a new device, the AH8308TC 8-bit video DAC.

HALF-MICRON CIRCUITS FABRICATED Scientists at IBM's Watson Research Center have fabricated the first circuits with half-micron line widths. An 8.5 square mm one-transistor memory cell has been fabricated on a memory array. A programmable logic array with 1700 transistors in a 0.1 mm silicon area is the densest logic circuit ever fabricated.

SMALL OPTICAL DISK R&D TO LEAD TO PRODUCT THIS YEAR A shared R&D agreement between Tallgrass Technologies, CPT Corp. and Information Storage Inc. is to produce small optical nonerasable disk drives by the end of the year.

VHSIC SIGNAL PROCESSING ICs ANNOUNCED Honeywell Data Conversion Product Center intends to market a set of VHSIC signal processing chips. The core of the chip set is the Electro-Optical Signal Processor (EOSP), a 3-chip set optimized for real-time image and video signal processing.

GRAPHICS BOARD FOR IBM PC WILL SPEED DISPLAY At next month's Siggraph show in San Francisco, Xtar will introduce an add-in graphics card for the PC. Intended for OEM applications, the Polygone board will feature a 100M pixel/sec polygon display speed.

PROBLEMS WITH VIDEO DACs?

Consider the Analogic Solution:

*Engineered Performance
+ Complete Family
= No Compromise*

Has your video display system design been compromised by inferior video DACs that fail to perform to your expectations? Have you had to add heat sinks or cooling fans to maintain acceptable operating temperatures? Have you been plagued by unacceptable video artifacts? Have you had to build in piggy-back boards to accommodate synchronization circuits that should have been in the DAC? Then check out the guaranteed performance features available off-the-shelf from Analogic's video DAC family.

Analogic engineered the AH8000 series of hybrid video DACs to offer a choice from many combinations of conversion rate, bit resolution, and logic compatibility. In addition, all members of the family meet such critical design criteria as low power dissipation, very low glitch

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The table below summarizes a few of the key parameters for some of our currently available units. Even if your requirements differ, give us a call! Using our proprietary chips and hybrid subassemblies, we have often configured custom DACs for our OEM customers—at surprisingly low cost.

We've helped many others solve their problems with video

DAC performance. We would like to help you. Call our Data Conversion Products Group and ask for the Video DAC Literature Pack at (617) 246-0300 X2291. Or write to: Analogic Corporation, Data Conversion Products Group, 360 Audubon Road, Wakefield, MA 01880.

Parameter / Feature	Analogic Model Number				
	Color (RGB)			Monochrome	
	AH8304TC	AH8304TM	AH8308TC	AH8308T	AH8308E
Resolution	3 x 4 bit	3 x 4 bit	3 x 8 bit	1 x 8 bit	1 x 8 bit
Logic Capability	TTL	TTL	TTL	TTL	ECL
Maximum Pixel Rate*	100 MHz	20 MHz	100 MHz	100 MHz	150 MHz
Look-Up Table Memory Size (Each Channel)	N/A	32 4-bit Words	N/A	N/A	N/A
Composite Blanking & Sync Controls	Yes	Yes	Yes	Yes	Yes
Blanking Control Timing	Synchronous	Synchronous	Synchronous	Asynchronous	Asynchronous
Power Dissipation	1.2W Typ. 1.7W Max.	1.5W Typ. 2.0W Max.	2.5W Typ. 3.0W Max.	0.9W Typ. 1.1W Max.	0.8W Typ. 1.0W Max.
Size (Inches)	1 x 1.3 x 0.3 24 Pin T-DIP	1 x 1.3 x 0.3 24 Pin T-DIP	2 x 1 x 0.3 40 Pin T-DIP	0.79 x 1 x 0.3 24 Pin D-DIP	0.79 x 1.3 x 0.3 24 Pin D-DIP

*Other Rates Available On Request

ANALOGIC ■

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TECHNOLOGY TRENDS

IMAGING

Image Processing With The IBM PC

Current estimates say that there are five million IBM PC or IBM PC-compatible computers in use in the US and that this figure is growing at the rate of two million per year. Because of this, a large number of vendors are putting the PC to work in applications ranging from business accounting to waveform analysis. In image processing, over 20 vendors are now supplying add-on boards and software to allow the PC to be used for in-

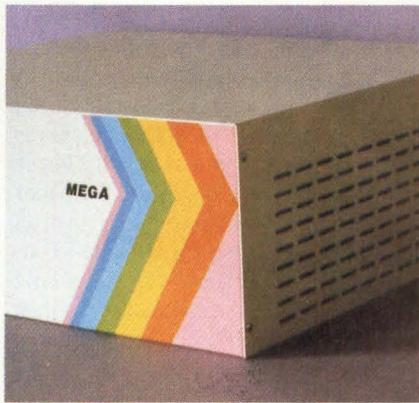


Figure 2: Laserus Productions' Megamachine is a multiprocessor system for the PC/XT/AT, capable of animating three-dimensional textured objects. A frame grabber will be available next quarter.

dustrial, medical and seismic applications (*Electronic Imaging*, March 1985, pp. 44-51).

This month, five more vendors entered the PC image processing field with a range of peripherals. At Biflyx (Irvine, CA), a full color frame grabber and software have been introduced which allow images to be captured in 1/60 of a second. Resolution of the captured image is 256 × 256 × 4 bits. Because the entire frame is bitmapped, users can combine com-

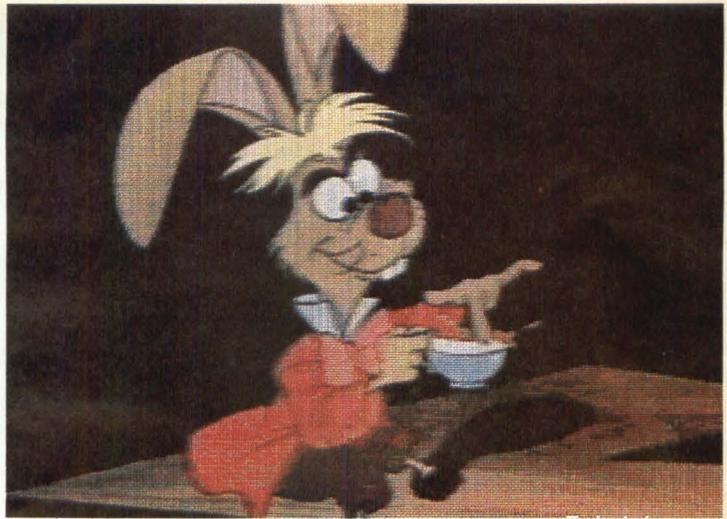


Figure 1: Video hardcopy image produced on the Biflyx videoprinter.

puter-generated graphics with the video image. Also, the company is offering its 1600 video printer which uses a thermal printing technique and color dye sheets to provide color hard copy with more than 4,000 hues (Figure 1).

US Video (Washington, DC) has also recognized the potential of PC imaging with the introduction of its RM-110, a PC add-on board that fits into the short slot of an IBM PC. The RM-110 superimposes computer images onto video and displays the output on a monitor. Input video can be any composite video or NTSC source while the computer-generated images can be generated from any PC-compatible graphics card.

Photographic communications is the primary market for the PC/Com system from Computer Systems (St. Clair Shores, MI). The system is a document-scanning and transmission system using PC/AT-compatible computers for image digitizing, processing and forwarding capabilities in information networks. Offering camera resolution of up to 400 dots per inch, the system can transmit documents to laser printers, color display terminal or IBM or DEC mainframes.

At Princeton Scientific Instruments (Kingston, NJ), a self-contained image data acquisition system has been intro-

duced for the XT or AT computers. The Model V CCD system uses a slow-scan CCD, interfaces for the XT or AT and associated software. The camera system provides optically isolated electrical outputs for the control of calibration lamp shutters that may be a part of the user's application. The CCD is in a cooled housing to reduce the CCD dark currents to levels compatible with long exposures. A list of the CCD types that can be used with the system is shown in Table 1. Software provided with the system is FORTH-based and allows CCD camera operation, data acquisition and reduction.

Following in the successful footsteps of Cubicomp's (Berkeley, CA) solid modeling system, the Modelmaker and Picturemaker which was first introduced two years ago, is Laserus Productions' (Berkeley, CA) Megamachine (Figure 2). It is a multiprocessor system for the PC/XT/AT, capable of animating three-dimensional textured objects. Megamachine system is capable of displaying 4096 colors from a palette of 16 million in 1024 × 768 × 8 or × 16 mode. Resolution is optionally expandable to 4096 × 4096. An optional digitizing frame buffer allows capture and manipulation of video images.

—A. Wilson

CCD	V × H Pixels	Pixel Size, Microns	Output Noise Electrons, RMS	Peak QE	Illuminated Surface
RCA SID-501	512 × 320	30 × 30	50	80	BACK
RCA SID-504	256 × 403	20 × 16	50	70	BACK
RCA SID-503	1024 × 640	15 × 15	50	80	BACK
GEC 8602	576 × 385	22 × 22	15	30	FRONT
RCA ICCD	256 × 403	39 × 31	50	20	S-20 PHOTOCATHODE
TEKTRONIX	512 × 512	27 × 27	~15	80	BACK
TEKTRONIX	2048 × 2048	27 × 27	~15	80	BACK
TI VPCCD	800 × 800	15 × 15	~25	50	FRONT

Table 1: A number of different CCDs can be used with the Model V data acquisition system from Princeton Scientific.

Automatic Digitizers Target Document Storage Applications

Automatic capture of engineering drawings to improve, among other things, design and drafting productivity, has long been a sought-after technology of companies with large engineering databases. Up until last year, there was no effective way to digitize large-format drawings or photographs into computer systems.

Realizing this, Eikonix (Bedford, MA) will enter the scanner market. The company's EZ Scan Model 44/34 is based on the 850 series 4096 × 1 CCD camera and is capable of digitizing drawings of up to 46" × 36" (Figure 1). This flatbed scanner can be interfaced to computer systems via the Multibus, Unibus, Q-Bus and later this year by any IEEE-488 interface. Priced at \$35,000, the scanner is capable

of digitizing documents to a resolution of 110 lines per inch. Eikonix sees applications of the scanner in architectural drawing, civil engineering and mapping applications.

Last year, Skantek Corp. (Warren, NJ) introduced an automatic digitizer, the SK-1010, capable of digitizing documents up to 40" wide by any length. The machine, which was introduced at the 1984 NCGA, uses a fixed-assembly scanning head consisting of two 40" long parallel lines of 10,000 fiber optic light pipes. One line conducts light from an incandescent source to the surface of the document to be digitized. The other picks up the reflected light and feeds it to a 2 cm square grid, consisting of 100 × 100 pixels. A CCD camera then scans the grid for the presence or absence of

reflected light. A 32-bit microcomputer then vectorizes and compresses the data, converting it to computer files which can be stored on magnetic tape in IGES, CADAM and other CAD/CAE system file formats.

Because of the relatively complex technology used in the scanner, the SK-1010 costs between \$125,000 and \$140,000 depending on the software options selected. Ronald Gerow, vice president of Industrial Vision Systems (Lowell, MA), sees this as one of the major setbacks to large scale use of the Skantek machine. The company's own scanner, the E/Scan, uses a less elegant but more manufacturable technique to digitize documents. In the design of the scanner, Industrial Vision employs four 2048 × 1 CCD cameras supported on an optical bench. These cameras face upwards toward the paper being scanned. The maximum eight pixel overlap is controlled by software to ensure correct digitization of the whole image. A single 8-bit A/D converter then digitizes the serial video stream into a logic board for image processing. Unlike the SK-1010, rasterized drawings are displayed not vectorized.

"CAD is a niche market at best," says Gerow of Industrial Vision. The firm has shipped 100 scanners to date, interfacing to either the Multibus, the IBM PC/XT or the Wang PC. The company is presently at work writing image processing algorithms to run on the ZIP-3216 from Mercury Computer Systems (Lowell, MA) which will be incorporated into the scanner. List price of the scanner is also lower than the Skantek 1010. At \$60,000, the scanner is able to digitize documents up to 36" wide by any length at 200 dots per inch. Figure 2 shows the type of image processing capable with the scanner.

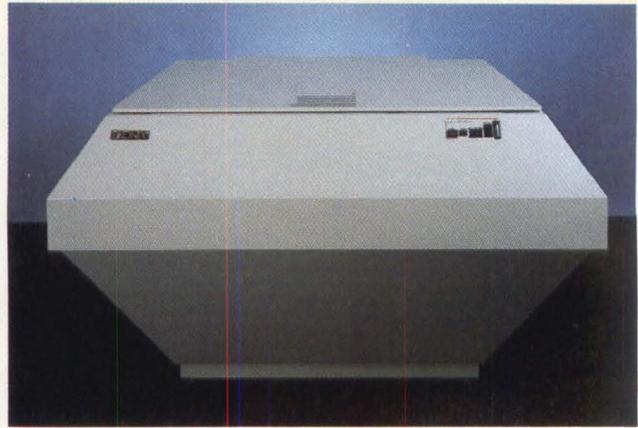


Figure 1: Eikonix EZ/Scan Model 44/34 scanner is capable of digitizing documents up to 46" × 36".

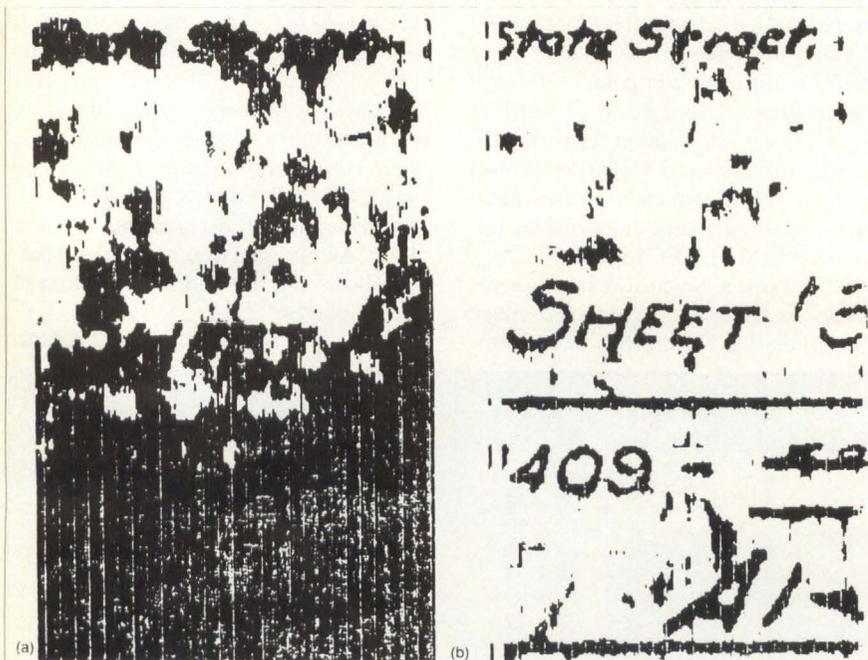
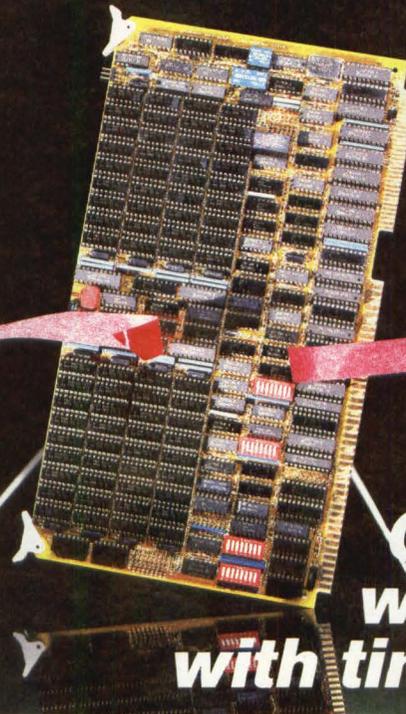


Figure 2: (a) Original image as scanned by the E/Scan from Industrial Vision Systems and (b) Image after pre-processing on the scanner.

—A. Wilson

In the Dual-Port Memory Dash...



**Central Data
wins again —
with time to spare.**

NEW—The Multibus* LBX 512K-2M Dual-Port Parity Checking Dynamic RAM Board

Here's the fastest dual-port memory available on the Multibus today, breaking the industry speed barrier with a *145ns typical LBX read data available time* on our super-fast version (195ns for our standard board). The super-fast board even runs zero-wait-states with an iSBC 286/10* CPU!

Both versions offer top system speed and performance for up to 2 megabytes (512K for super-fast version) of dual-ported RAM. The board can be strapped for either 64K or 256K RAMs to allow easy upgrading. Parity checking is standard, with both Multibus and LBX cycles optionally generating parity error interrupts. And quiet, reliable operation is assured by the board's six-layer construction.

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And more frontrunners in the Multibus memory field.

Central Data offers a complete line of Multibus memory boards to meet every system need. Call us for full details.

BOARDS	EDC	PARITY	DUAL PORT	TYPICAL ACCESS TIME (ns) ▲	AACK	BATTERY BACKUP	FORMER PART #	MEMORY SIZE (bytes)
CD21/2500	no	yes	yes	195	yes	yes	—	512K, 1M, 2M
CD21/2501	no	yes	yes	145	yes	yes	—	512K
CD21/2700	yes	no	no	180	no	no	B1027	128K-2M
CD21/2701	yes	no	no	140	no	no	B1027F	256K, 512K
CD21/2140	no	yes	no	170	yes	yes	B1040	128K-2M
CD21/2141	no	yes	no	135	yes	yes	B1040F	256K, 512K
CD21/2110	no	yes	no	295	yes	yes	97/0000C	1M, 2M, 4M
CD21/2100	no	yes	no	235	yes	yes	97/0000	128K-512K
CD21/2035	no	no	no	90+	yes	yes	B1035	*
CD21/5232	no	no	no	100+	no	—	96/5232	*
CD21/2014	no	no	no	100+	yes	no	B1014	8K-128K

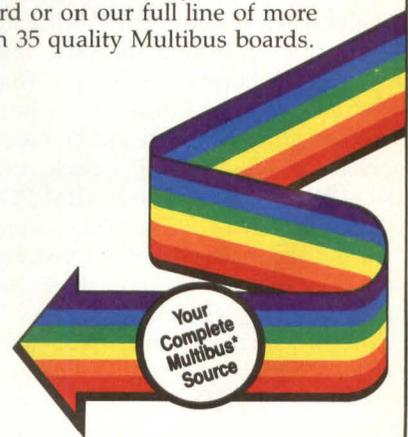
+ plus the access time of the device

* Addresses 8K-512K of EPROM, 8K-128K of RAM, or 8K-128K of EEPROM

• Addresses 8K-256K of EPROM, 8K-128K of RAM, or 8K-128K of EEPROM

▲ Typical data available access time

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SOFTWARE

Thermal Analysis Package Rapidly Assesses Heat Characteristics Of Designs

As circuits get both faster and denser, power dissipation problems mount. Analyzing the thermal properties of a printed circuit board is a tedious process; calculating the effects of fans, packaging and adjacent boards adds complexity to the problem. The EDA-2500 program from Telesis (Chelmsford, MA) analyzes heat characteristics of a PC board during design. Using a software package rather than an actual prototype, thermal properties can be predicted before a design is finished. The program's calculation speed allows various system designs to be explored for optimum thermal characteristics.

Component junction and case temperatures are predicted as well as overall board temperature profiles. Conduction, convection and radiation heat transfer are all considered in this analysis. The analyzer spots hot and cold regions of the board and summarizes results in a report or an isothermal plot. Various factors can be changed to explore design, packaging and cooling options. Telesis' IBM PC-based system or a DEC terminal is used for display and interaction. For speed, the calculations run on its 32-bit coprocessor or a VAX as a batch process.

The software consists of two programs, one for before component placement and another for after. For 'quick-check' pre-placement analysis, the designer inputs overall board size and total power dissipation, orientation, airflow, power dissipation of adjacent boards and board-to-board spacing. The preprocessing analysis shows whether natural convection will alleviate heat problems or whether fans will be needed. This prediction can actually drive board placement.

By changing parameters, a designer

can assess trade-offs of various configurations early in the design cycle. It will be clear not only which areas of the board will generate the most heat, but whether heat sinks could diffuse enough heat to eliminate the fan. The effect of changing board spacing or enclosure size can also be accurately predicted.

Post-placement analysis allows a more detailed look at thermal characteristics of a board. Once a design has been entered and placed at a Telesis workstation, the EDA-2500 automatically extracts placement information. The designer specifies only parameters not in the design database, like altitude, boundary conduction and local heat sinks. Up to 52 parameters can be adjusted to create various 'what if' scenarios.

An important feature for figuring actual performance that even prototypes cannot provide is worst case analysis. The EDA-2500 thermal analyzer can automatically increase power dissipation for all components and recompute the

temperature profile. This worst-case analysis could result in designs that fail less frequently once in production.

The trend toward smaller, denser systems will certainly not reverse. In higher performance systems, components are densely packed because going off-board to the backplane is unattractively slow. In addition, complex semicustom and standard ICs are often packaged with many pins on a small package, for very dense boards. This pin density as well as the high speed of current devices creates more potential heat problems.

Other PC board CAD vendors indicate that they are working on similar products. Thermal problems are mounting quickly and must be included in complete design cycle solutions. Early views of design trade-off options are increasingly important. Avoiding heat problems at the pre-layout stage may allow complex designs to become products within short market windows.

—Pingry

FAST RUN -- ENTER DESIRED INPUT AND THEN ENTER /Z(THERMAL)			
1	LENGTH OF PCB IN X-DIRECTION	30.0 (CM)	(1.0 - 100.)
2	LENGTH OF PCB IN Y-DIRECTION	40.0 (CM)	(1.0 - 100.)
3	SPACE BETWEEN BOARDS IN Z-DIR.	3.0 (CM)	(0.1 - 100.)
4	BOARD THICKNESS	0.3 (CM)	(0.01 - 1.)
5	EFF. BOARD THERMAL CONDUCTANCE	0.2 (W/CM-C)	(0. - 10.)
6	TOTAL BOARD POWER DISSIPATION	40.0 (W)	(0. - 1000.)
7	DIRECTION OF AIRFLOW	+X	(+X, +Y, -X, -Y)
8	DIRECTION OF GRAVITY	-X	(+X, +Y, -X, -Y)
9	INLET AMBIENT AIR TEMPERATURE	25.0 (C)	(0. - 100.)
10	AIR VELOCITY	0.5 (M/S)	(0. - 10.)

UP	DOWN	SELECT	DONE	RESTART	HELP	QUIT
SUMMARY	EDIT	CHANGE				
OF FILES	FILE	UNITS				
THERMAL	REPORT	FAST				
ANALYZER	WRITER	RUN				

A range of system parameters can be manipulated repeatedly in the EDA-2500 thermal analyzer from Telesis. What if scenarios can be created and rapidly processed before placement of components on a PC board.

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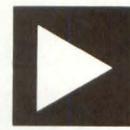
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TECHNOLOGY TRENDS

GRAPHICS

Custom Chips Provide Raster Operations

Raster operations are important in computer graphics for controlling repetitive graphics functions. Although these functions are typically implemented in software, there is a growing trend to use hardware for faster results and lower costs.

The raster operation (raster-op) called Bit-Blt is an example of a commonly used graphics primitive. Bit-Blt, or bit boundary block transfers, grew from the attempt to treat text and bitmap graphics similarly with Xerox's Smalltalk language. The function allows rapid transfer of hidden graphics or text characters onto a bitmapped screen.

Bit-Blt modifies a rectangular destination of a bitmap using data from an external source bitmap. The rectangular region is typically 16×16 pixels. The alternative is drawing the characters serially, which consumes more time.

Bit-Blt allows Boolean operations where characters can be copied to a destination in the frame buffer in a particular mode such as XOR. XORing characters or graphics allows the overlay of new data while retaining the graphics information underneath. After XORing once more, the original image is displayed intact. This capability is used extensively in nondestructive cursors and pop-up menus. The Bit-Blt function also facilitates rapid implementation of highlighting, scrolling screens, region filling and window manipulation.

Sun Microsystems (Mountain View, CA) was one of the first companies to use a custom chip for the Bit-Blt raster-op. A single chip replaced about 60 TTL chips. A bitmap of each character is stored in a separate memory location. The Bit-Blt chip swaps this memory onto the display bitmap. The Sun system allows one, two or three operands which are referred to as

destination, source and mask operand. Any one of the 256 possible combinations of Boolean functions can be selected.

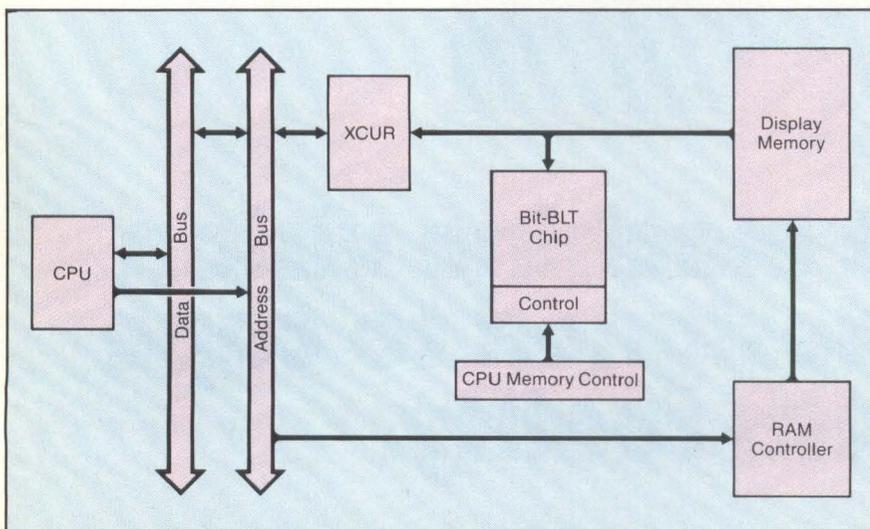
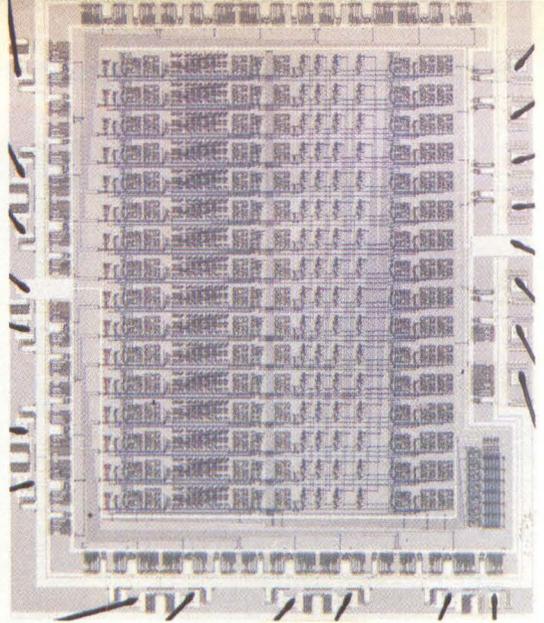
Two companies now offer the Bit-Blt raster-op on a chip. Sun Microsystems' chip was developed via silicon compilation at Silicon Compilers Inc. (Los Gatos, CA). It is now manufactured and sold through VLSI Technologies (San Jose, CA). A more recent Bit-Blt chip is the PMR 96016 from Pacific Mountain Research (Seattle, WA). This chip was also designed by means of silicon compilation at Seattle Silicon (Seattle, WA).

The RasterOp from VLSI is very similar to the Blt chip from Pacific Mountain Research. Both chips are available in 28-pin packages with similar pinouts. Operation is also similar. In a typical application, the Bit-Blt chip intercepts data from main memory on read cycles from the host and substitutes new data into the display buffer during write cycles. The host is only used as a source and destination address generator for the Bit-Blt chip.

The memory controller of the Bit-Blt chip causes write cycles from the host CPU to be converted into read-modify-write cycles. Data is first read from a destination such as a display bitmap to the Bit-Blt chip. New data from another location is then written to the display bitmap. The result is that a horizontal row of 16 pixels can be read from the display bitmap, combined logically with the new data and written back to the bitmap. This process takes approximately two bus cycles for 16 pixels using the PMR 96016. Implementation of the RasterOp on the Sun workstation results in $20 \mu\text{sec}$ for writing a 16×16 pixel character. At this rate, the whole screen can be filled with characters in 64 msec.

—MacNicol

PHOTO COURTESY PACIFIC MOUNTAIN RESEARCH



The Bit-Blt chip is positioned between the system CPU and the frame buffer. External bitmaps of 16×16 pixels can be modified and placed rapidly in the frame buffer's memory.

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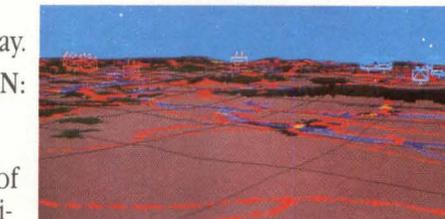
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TECHNOLOGY TRENDS

DESIGN TOOLS

Back Annotation Speeds Up Gate Array Design

For the first time, gate arrays can be designed from start to finish on an engineering workstation without the need for a large mainframe computer. Gould AMI (Santa Clara, CA) now provides back annotation capabilities for its CMOS gate array family to customers using the design tools on Mentor Graphics' (Beaverton, OR) workstations. As a result, both companies estimate that total design time can be reduced by two weeks or more.

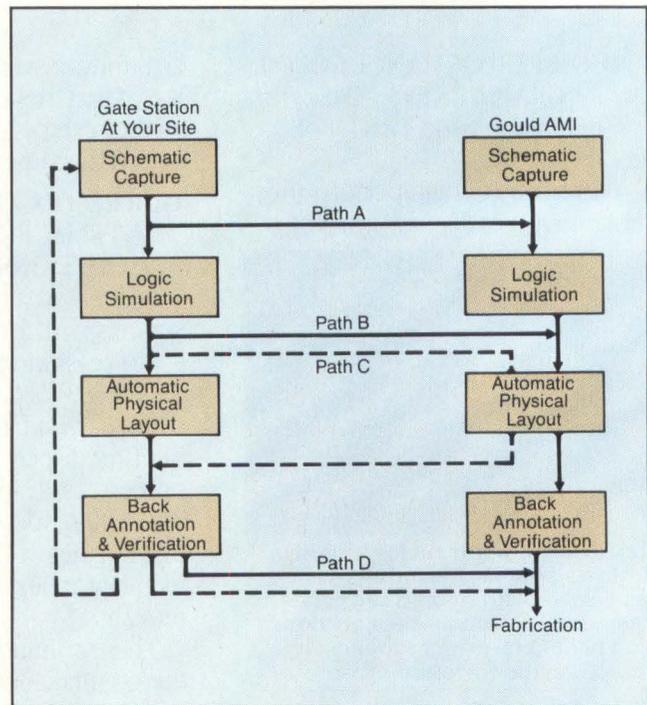
Back annotation provides the ability to download timing delay information garnered from the physical layout process back to the workstation (see *Digital Design*, February 1985, p. 66). Comprehensive timing analysis is crucial to the successful design of a CMOS gate array fully packed with logic elements since such factors as device propagation delay and wiring delays can impact performance at high operating speeds (above 20 MHz).

Gate array vendors typically provide timing analysis tools for use on workstations. These are used prior to actual routing with estimated values for wiring delays. A final timing analysis based on the actual values gathered from the routing process is also done to ensure that the chip will function properly. This is usually performed on the vendor's mainframe-based CAD/CAE system. Packages using such an approach include Design Verifier from LSI Logic (Milpitas, CA) and Easygate from International Microcircuits (Santa Clara, CA).

Should timing problems arise, the customer has two alternatives. One is to use the gate array vendor's CAD/CAE system to rectify the problem. However, the customer may not be familiar with the

With back annotation, a customer can transfer a gate array design

from a Mentor Graphics Gate Station to Gould AMI after simulation (C) for automatic placement and routing. The actual wire delays are downloaded to the workstation to be used for further design verification. As a result, the customer has the option of having the design completed after schematic capture (A), design simulation and verification (B) or automatic layout and resimulation (D).



CAD/CAE tools used on the vendor's system. The other option is to try to solve the problem working with the vendor's applications engineers over the telephone. Since the gate array vendor does not have an intimate knowledge of the circuit design, this can lengthen the design process by two weeks or more.

In contrast, Gould AMI allows post-layout timing analysis to be performed on the customer's workstation rather than just on the vendor's CAD/CAE system. The advantage to this approach is that the customer can alter the circuit when timing problems occur and recheck the timing on the workstation after rerouting.

Back annotation also proves useful when a customer seeks to optimize a gate array for either size or speed. Tom Vonderach of Gould AMI notes that wiring-delay estimates are often conservative to provide adequate margins over the intended speed and operating range of a gate array. These margins are needed because place-and-route software often

spreads logic for a particular function across the array to maximize the number of gates that can be automatically routed. However, significant propagation delays can occur as the array becomes more densely packed and fewer cell sites are available for routing. By using the actual wire-length delays rather than the estimated values, a customer can readily determine which paths need to be rerouted so that the overall performance of the circuit is enhanced.

By this fall, expect to see back annotation capabilities extended to gate arrays from other vendors. International Microcircuits is working on providing this capability on workstations from Mentor Graphics and Daisy Systems (San Jose, CA), and LSI Logic has announced similar plans for the Valid Logic (San Jose, CA) Scaldsystem. Mentor Graphics is also working with Mostek (Carrollton, TX) and Motorola Semiconductor (Austin, TX) for similar support.

—Aseo

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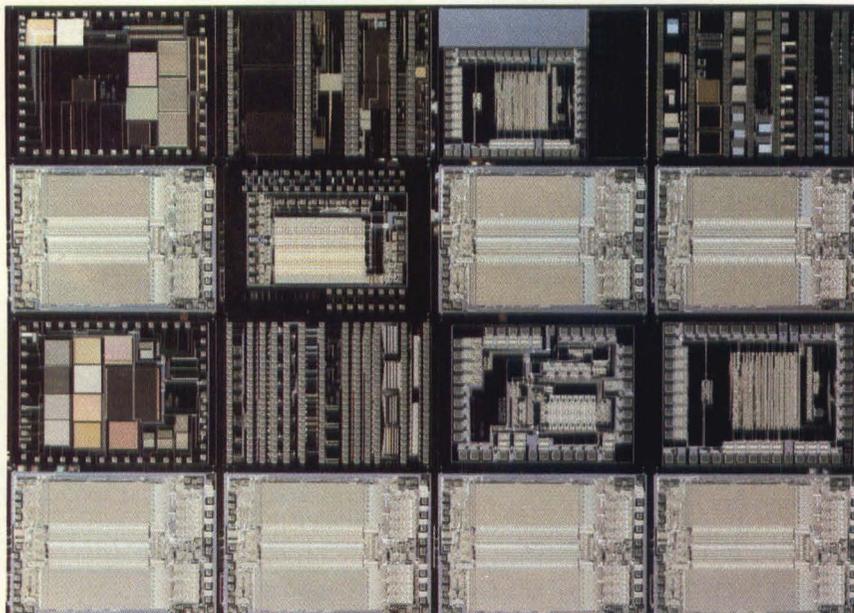
Circle 56 on Reader Inquiry Card

Cell Library Gains 32-Bit CMOS Bit-Slice Processor

Standard cell technology continues to move ahead rapidly. Most analysts agree that standard cells will become the preferred semicustom technology by the end of the decade. Compared to gate arrays, standard cells offer two primary advantages. First is the small die size, which approaches the area consumed by a comparable full-custom handcrafted chip. Many of today's off-the-shelf VLSI chips are designed using standard cells. Handcrafting of these devices is usually not cost-effective because laying out the large number of transistors is excessively time-consuming. The second advantage is that microprocessors and memory are available as macrocells in a cell library. Until

recently, most vendors' libraries contained an ALU and perhaps one core microprocessor, if any at all.

WaferScale Integration (Fremont, CA) recently announced the addition of a 32-bit CMOS bit-slice processor to its standard cell library. Designated the 59C032, the processor runs at 15 MHz, has a datapath delay time of 82 nsec and dissipates 300 mW of power. In addition, the 59C032 includes a scratch-pad 32-word \times 32-bit static RAM. The cell is fabricated in 2-micron CMOS, and its die size is 0.150 mils on a side. In comparison, when eight 4-bit bipolar 2901 processors from Advanced Micro Devices (Sunnyvale, CA) are linked together, the resulting 32-bit function has a datapath delay of 91 nsec and dissipates 12.1W.



A WaferScale Integration wafer showing one reticle field of 16 CMOS device sites. Ten different designs were produced concurrently on this wafer by stepping the 5 \times reticle across the wafer. Circuits illustrated are a high-speed CMOS EPROM, a high performance 4-bit bit-slice processor, a 2-micron standard cell evaluation chip, the same device shrunk using 1.5-micron design rules, process control monitor devices, device physics evaluation chips and an advanced experimental memory device.

Other cells in WSI's library include PLAs, CMOS EPROMs, CMOS static RAMs, ROMs, 4- and 16-bit bit-slice processors and over 100 SSI/MSI random logic devices. WSI supports engineering workstations from Daisy Systems, Mentor Graphics, DEC (VAX running Silvar Lisco's [Menlo Park, CA] CASS schematic capture program) and IBM (PC AT).

For designers not using a standard cell approach who need the high performance of the 59C032, WSI is introducing a packaged version of the processor. The chip will be available in the third quarter of this year. It will have a 0.200 mil per side die size and will be housed in a 100-pin pin grid array. Performance is expected to be around 15 MHz.

WSI will not remain alone in the bit-slice standard cell arena. Ricoh Co. (Santa Clara, CA) plans to include the 2901 in its library by the third quarter. Established manufacturers such as Zymos (Sunnyvale, CA) and NCR (Fort Collins, CO) presently offer core micros. Zymos provides the 80C49 processor and the ZycompII, a 4-bit microcontroller. NCR has its 65CX02, an extended version of the 6502 microprocessor.

Standard cell libraries that include core micros offer designers an excellent solution to protecting proprietary designs. Moreover, high density cells like ROM and RAM can be combined with core micros and glue logic on a single application-specific IC. This results in efficient silicon usage while optimizing performance.

Nonrecurring engineering (NRE) costs are usually higher for standard cell designs than for gate array designs. The bulk of the additional cost is due to tooling. Unlike a gate array, each standard cell design is fabricated using a unique set of masks. In a gate array, only the metalization masks are tailored for the particular design. However, as the use of standard cells becomes more widespread, NRE costs will likely decline.

— Collett

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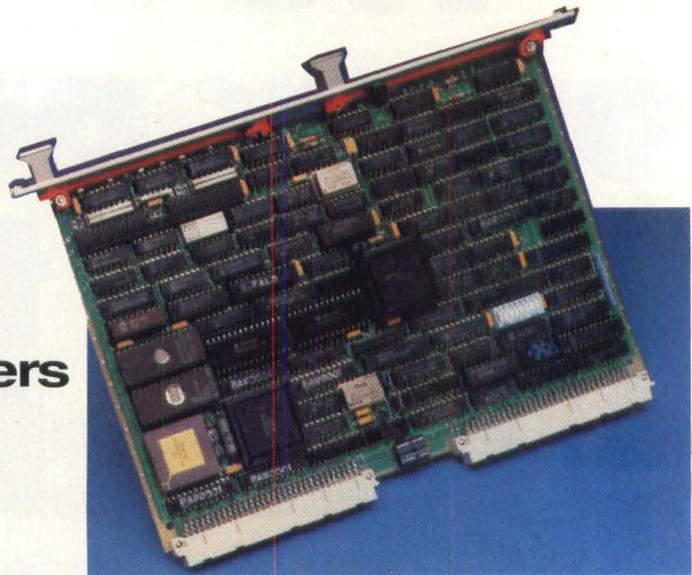
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Circle 32 on Reader Inquiry Card

BOARDS

Disk And Tape Controllers For 32-Bit Systems Emerge on VMEbus



The need for systems integrators to migrate to a 32-bit bus structure has resulted in success for the VMEbus. Although its closest contender, Multibus II, is vying for a piece of the same marketplace, the momentum behind the Intel bus structure has yet to emerge. In the high-performance disk and tape controller marketplace, major manufacturers are turning to the VMEbus. However, all these vendors have suggested they will provide Multibus II products when the market is large enough, even though the architecture is a radical departure from Multibus I.

The first evidence of VMEbus boards from traditional Multibus disk and tape controller makers is the Interphase (Dallas, TX) V/SMD 3200 SMD Winchester controller (Figure 1). Xylogics (Burlington, MA) and Ciprico (Plymouth, MN), two other high-performance Multibus controller manufacturers, have announced matched VMEbus SMD disk controllers and 1/2" tape controllers that will be in production by this fall.

The first VME product from Multibus manufacturer Minicomputer Technology (San Jose, CA) is a 1/4" tape controller, admittedly not particularly high performance. A matched ESDI disk controller and 1/2" tape controller board set on the VME should follow soon.

Since the main impetus to designing with a 32-bit bus is added speed, it is critical that disk-to-bus transfers are fast. Two bipolar state machines on the Interphase 3200 control data movement; one is used for transactions between the controller and the VMEbus, the other for those between the controller and one or

two SMD drives. Twelve Mbytes of on-board memory act as virtual buffers, available to either disk or VMEbus processes. Disk read operations begin at the first sector the head encounters, not necessarily the first sector requested; this ensures rapid disk-to-controller transfers. Data is transferred from controller buffers to main system memory when disk read begins, without waiting for the entire sector to be read.

Xylogics has addressed the disk-to-bus speed issue by using FIFOs. The advantage to using FIFOs rather than buffers is speed; emptying a buffer may use extra cycles. Interphase contends that its buffer-to-memory scheme provides performance similar to FIFOs without the data overruns and underruns inherent in FIFO-based systems. The Xylogics 751 and Interphase 3200 use custom silicon for DMA to improve speed. Ciprico, Xylogics and Interphase all find that microprocessor DMA is too slow.

A standard feature for fast system interaction with disk drives is cache. Interphase uses an extended read-ahead caching algorithm on the 3200 for raw speed between the disk and controller. Minicomputer Technology has a 32-Kbyte buffer in the initial specification for its ESDI controller. According to Minicomputer, some designs demand complex cache algorithms, but simpler, faster cache is best for many systems.

UNIX systems tend to fragment data on a disk, so caching physically contiguous sectors is not advantageous. Caching of logically contiguous blocks is relatively ineffective for multiuser and multi-

Figure 1: The Interphase V/SMD is the first high-performance SMD disk controller for full 32-bit VMEbus systems. Virtual buffering provides simultaneous disk and bus activity and high throughput rates. The 3200 is optimized for UNIX and its derivatives. A matching 1/2" GCR tape controller will be introduced in several months to ease software integration.

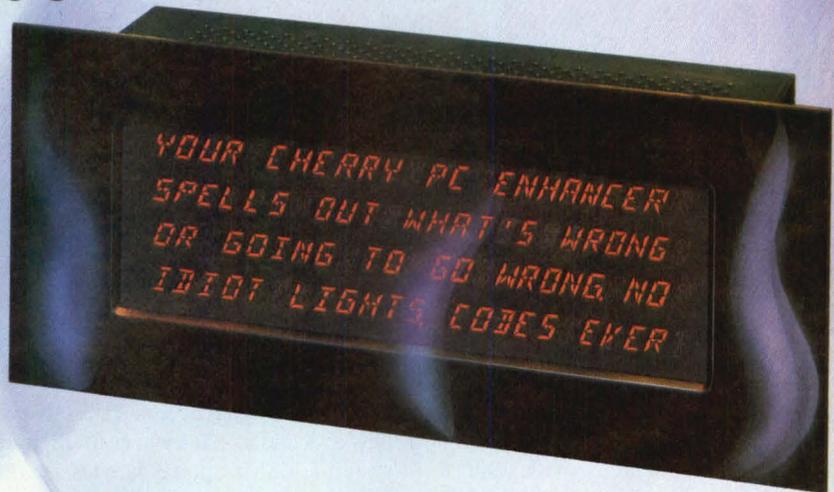
tasking systems because consecutive disk reads tend to be from different tasks. Ciprico intends to use a very large cache on its VME Rimfire 3200 and segment it to optimize for multiuser systems. A proprietary algorithm will determine which segment of cache to swap out.

Xylogics has chosen not to implement data cache, but uses "command caching." This command optimization algorithm makes no assumption of system data needs, but instead queues command requests to optimize disk accesses. This allows the controller to service system requests in rapid succession.

To optimize bus usage for multitasking, both Xylogics' 751 and Ciprico's 3200 will use throttles. Xylogics has used a software programmable throttle to determine how long the controller remains on the system bus in several products. Ciprico intends to provide both this time throttle and a byte throttle, selectable on system configuration.

Software interface and drivers are also critical to high-performance system design. Interphase, Xylogics and Minicomputer Technology are all planning to provide matched high-performance disk and tape controllers for 32-bit VME systems with a consistent interface. The

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TECHNOLOGY TRENDS/BOARDS

standard backup device for 32-bit systems is expected to be 1/2" tape. Either similar or identical 1/2" tape and disk controller interfaces for operating systems including UNIX are planned.

Now that there is a standard format for SMD bad block recording, the Xylogics controller will read defect information off the drives. The defect management system on the 751 controller will use sector slipping. This scheme provides spare sectors on the same track, so no head movement is required to skip from a bad sector to its substitute.

Interphase gives the user a choice of this spare sector per track or alternate track defect mapping. With large sectors, more disk space is taken by a sector-per-track scheme, but speed is greatly en-

hanced since no head seeking is needed. Spare tracks for defects may use disk space more efficiently, but may slow average access. Minicomputer Technology's ESDI controller will offer the track or sector choice and support loading a defect table from the disk into the controller.

There may also be a need to look into new disk and tape interfaces for high-end systems. ESMD, at a 3 Mbytes/sec data transfer rate, pushes the limits of drivers and receivers; currently, ECL parts are used. For faster data transfer, serial interfaces like SMD will need to be replaced by parallel schemes. The most likely candidate for replacing SMD is IPI. IPI provides byte-wide or even 16-bit transfers. IPI Level 2 is nearly defined and should

be implemented on products by next year. IPI Level 3 is an intelligent interface with half of the controller in the disk drive. Because of the close coordination needed between disk and controller manufacturers in intelligent interfaces, IPI Level 3 may take much longer to be defined.

In the meanwhile, SMD and 1/2" GCR tape controllers on VME boards will provide systems designers with options for full 32-bit performance. Those moving into higher performance from the Multibus I may be comfortable with the suppliers of disk and tape controllers supporting VME now. And in the near future, high-performance VMEbus, Multibus I and Multibus II products may all be available from these vendors.

—Pingry

ICs

Disk Controllers In The Chips

Chip sets to control rigid disks are moving from concept to full production. These highly integrated controllers will begin to appear on both disk drives and host CPUs. Traditional board-level disk controllers will also change as they assume the added responsibilities of floppy disk and tape drive control. As a consequence, system designers can tailor a controller to fit the application rather than be tied to an off-the-shelf solution.

Experience with disk controllers may be an initial advantage for vendors such as Adaptec (Milpitas, CA), Data Technology (Santa Clara, CA), OMTI (Mountain View, CA) and Western Digital (Irvine, CA). However, merchant semiconductor manufacturers are also entering the fray; Advanced Micro Devices (Sunnyvale, CA), Intel (Santa Clara, CA), National Semiconductor (Santa Clara, CA) and NEC Electronics

(Natick, MA) are all moving from sampling to mass production.

The key question for prospective users centers around the trade-off between functionality and flexibility. ICs from Advanced Micro Devices, Intel, NEC Electronics and Western Digital provide full functionality. They implement the data path (e.g., encoding/decoding, error correction, data separation) and the control electronics (e.g., handshaking signals) for a limited number of disk interfaces (e.g., ST-506, ESDI, SCSI). The disadvantage of this level of integration is reduced flexibility for handling variable record sizes, different data transfer rates or different encoding schemes.

This may prove less troublesome for the lower-performance ST-506 interface than either ESDI or SCSI. Disk drive and controller vendors have largely agreed to fixed parameters (e.g., 512-byte sectors) for ST-506 drives in both the 5 1/4" and

sub-4" arenas. There is less agreement among disk drive vendors for standard configurations for either ESDI or SCSI, so designers may want more flexibility to choose their own implementations.

In fact, chip implementations from Adaptec, Data Technology, National Semiconductor and OMTI allow users to select these parameters as well as the control signals and data path electronics for various device- and system-level interfaces. This imposes more responsibility on the system designer, who must determine which blend of parameters work best in the application, rather than accepting the limited options that the other chip sets provide.

Using these programmable chip sets, the designer must focus on three different aspects of the controller: the specific device-level interface, the core controller functions (serial/deserialization, formatting, data separation and error correction) and the interface to the host CPU itself. Most system designers can design the host interface, but may lack the expertise to properly fine-tune the remaining two functions.

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TECHNOLOGY TRENDS/ICs

As a result, the fixed-function chip sets that specify all functions will have a much larger clientele than chip sets offering full flexibility. One area where programmable chip sets are being used now is multi-function controllers that support rigid and floppy disk drives as well as tape backup. Floppy and rigid disk drive functions are so similar (the primary difference being the data transfer rate) that the same chip set could easily handle both types of drive. In contrast, a separate chip set may be needed to handle tape backup in a multifunction controller since tape drives are serial access rather than random access.

Fully-featured hard disk controller chips may move control functions from a standalone board to either the host CPU or the disk drive. Harry Laswell, peripheral product manager at Intel, notes that these chips should prove no more dif-

icult to integrate onto the host CPU than other microprocessor peripherals like DMA controllers.

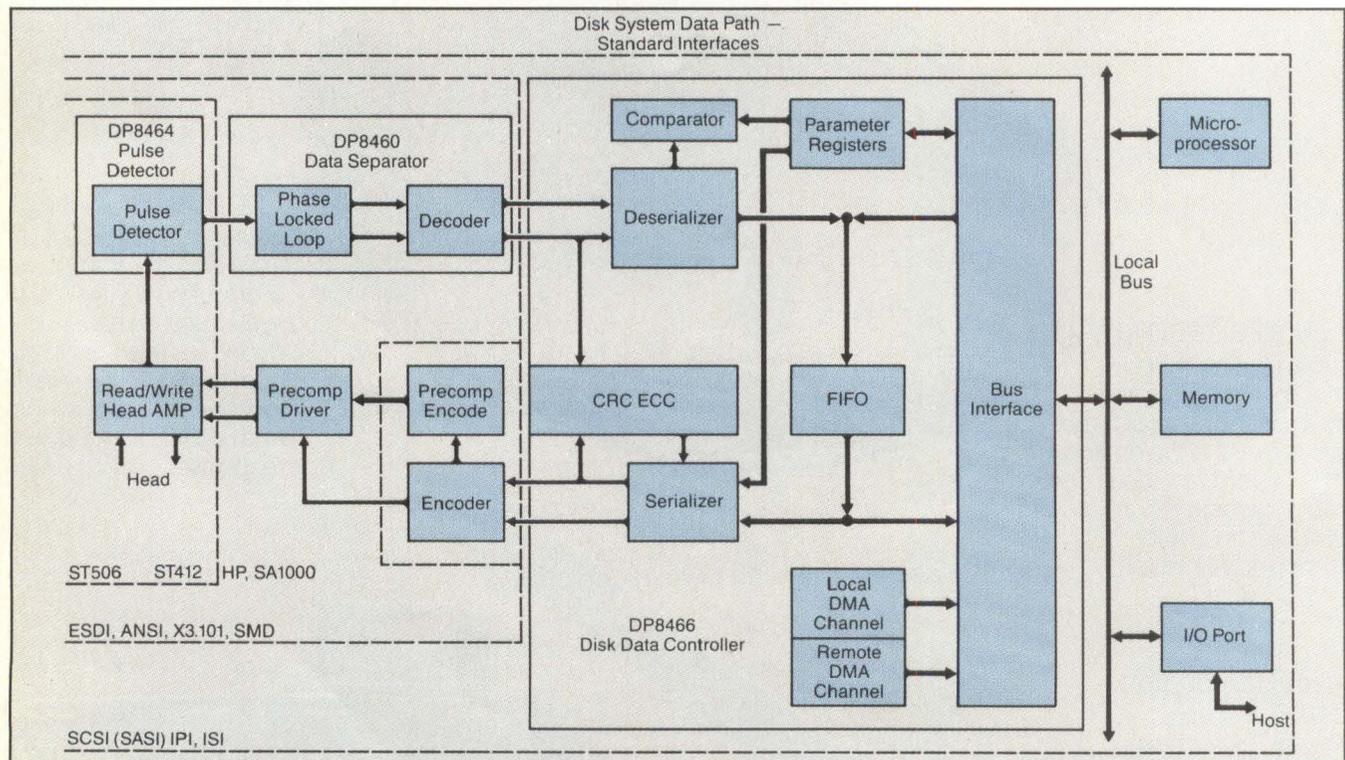
The effort required to move the controller onto the drive may be more difficult than integrating it with the CPU. Larry Boucher, president of Adaptec, notes that disk drive manufacturers may eventually gain the design expertise to include the control function with the read/write electronics. However, few of these vendors will invest in fabricating the controller chips. Instead, they will probably buy them from Adaptec, Western Digital and other vendors.

The benefits for a drive manufacturer bringing the controller on board include increased performance and reduced cost. Phil Devin of Xebec notes that the drives can be built with lower grade heads and media since error correction and data separation is controlled by the drive ven-

dor. By using a system-level interface like SCSI that requires block-oriented transfers, drives can operate without interleaving sectors for increased data transfer rates.

Which manufacturers prove to be more adept at building controller chips is still open for debate. Boucher notes that it remains to be seen whether the large semiconductor manufacturers like Advanced Micro Devices, Intel, National Semiconductor and NEC Electronics will devote the necessary personnel and capital resources to design the controller chips needed by both disk drive and board-level controller vendors. The only chip sets available in production quantities are from Adaptec and OMTI, whereas the others are still in the sampling stage. The wide availability of these chips will alter the face of the disk controller business.

—Aseo



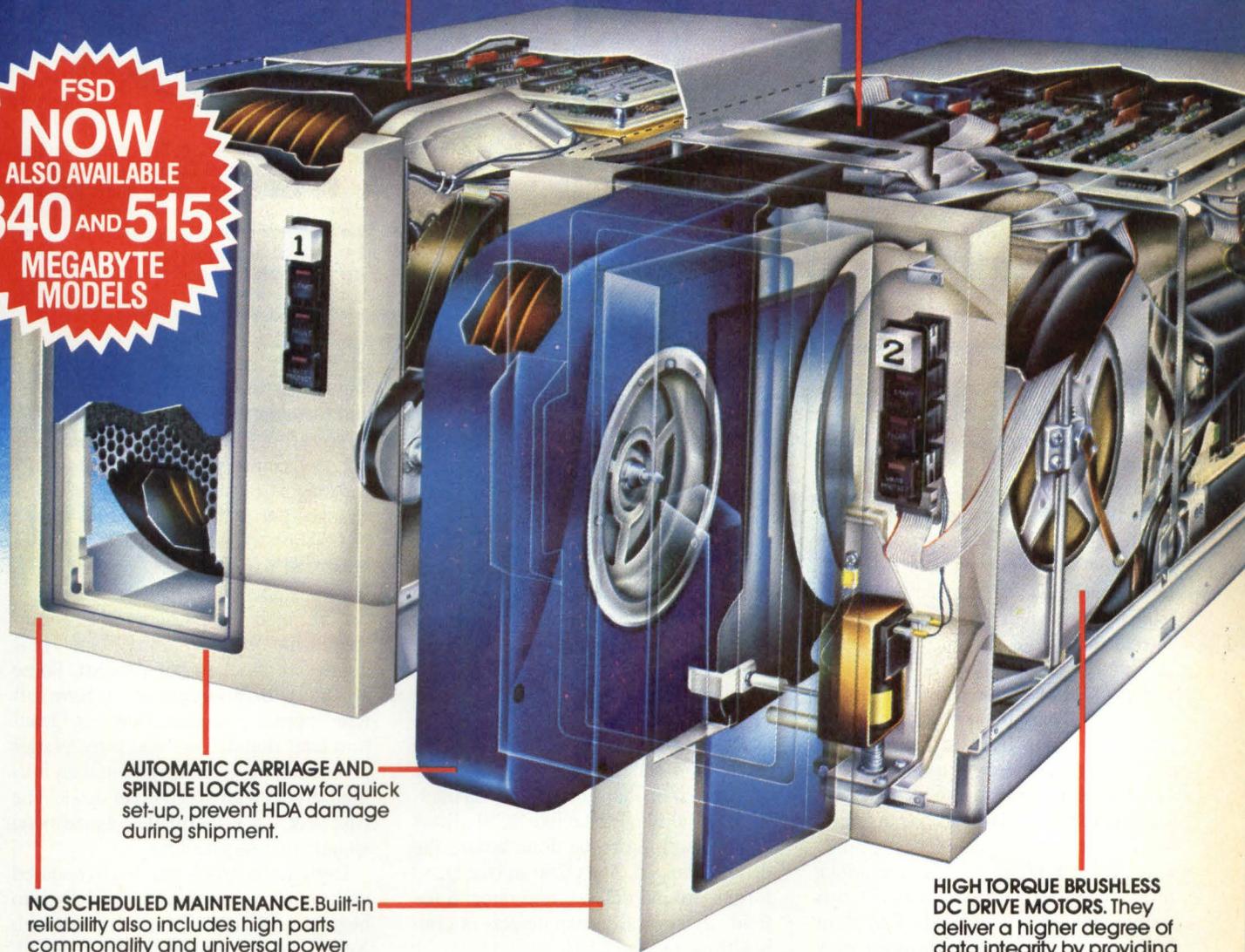
National Semiconductor's three-chip controller allows designers the flexibility to implement a wide variety of device- and system-level interfaces for rigid disk drives. The various interfaces are listed in the lower left-hand corner of the figure. Dotted lines show how much functionality each interface specification includes.

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TECHNOLOGY TRENDS

PERIPHERALS

5 1/4" Half-High Winchesters Rise To Meet High-Performance System Needs

Despite a push to small system enclosures such as the narrow desk-high and desk-deep tower, 8" and standard 5 1/4" Winchesters are used in most multiuser systems. Half-height 5 1/4" drives are attractive in size, but have not offered adequate capacity or performance for supermicros and superminis. However, by the end of the year, an intelligent 5 1/4" half-high drive will be available offering 53 or 80 Mbytes of formatted storage and sub-30 msec access times.

The Q250 and the Q280 intelligent half-high drives from Quantum (Milpitas, CA) with built-in system-level SCSI controllers could be a breakthrough for small high-performance systems. 5 1/4" intelligent SCSI drives have been available for some time from Xebec (Sunnyvale, CA), which plans to introduce models with 20 and 40 Mbytes this month. Tandon (Chatsworth, CA) plans the same type of product. However, only Quantum has announced plans to pack over 50 Mbytes in a half-high.

Unlike Xebec's intelligent SCSI drives for single-user systems, Quantum's products are designed for high-performance multiuser systems. The 53 Mbyte Q250 uses two platters; the 80 Mbyte Q280, three. Both use sputtered thin-film media and Whitney heads. An embedded servo system saves on both electronic and mechanical parts. Following the SCSI spec, a 1.25 Mbyte/sec speed can be sustained. To equalize between this speed and the sub-30 msec average disk access time, a 16-Kbyte FIFO acts as a buffer.

High-performance systems need low error rates as well as speed. The Q200 drives use a Reed-Solomon ECC with an

interleave of three. This provides one in 10^{14} unrecoverable sectors and one in 10^{21} miscorrected sectors.

One of the biggest challenges has been squeezing drive and control electronics into a single 5 1/4" form-factor board. Both the actuator and the motor speed are controlled by one microprocessor; Quantum has used two in other products. Only one off-the-shelf SCSI chip is used; gate arrays save space and optimize SCSI for Quantum's drive design. A 16 Kbyte buffer is included as well.

Advantages to a built-in controller begin with reliability. When the drive arrives to go into a system, there can be no doubt whether it will play properly with the controller. In addition, an intelligent system interface like SCSI allows defect mapping to be done before the drive is shipped. The Q250 and the Q280 format around defects, and once in the field, dynamically map defects in conjunction with the CPU.

System builders can integrate the drive without performing physical defect mapping or using special utilities. The goal is to ship drives to system builders' stock, without incoming test. Quantum quotes 25,000 hours MTBF.

SCSI not only permits system upgrades without new device-level interfaces for each peripheral type, it performs many I/O functions without host intervention. A copy command, for example, permits data backup with the CPU only issuing one command and the rest of the process occurring without host intervention or traffic on the bus. Quantum also implements the SCSI disconnect/arbitration/reconnect command, so peripherals can disconnect from the SCSI bus while



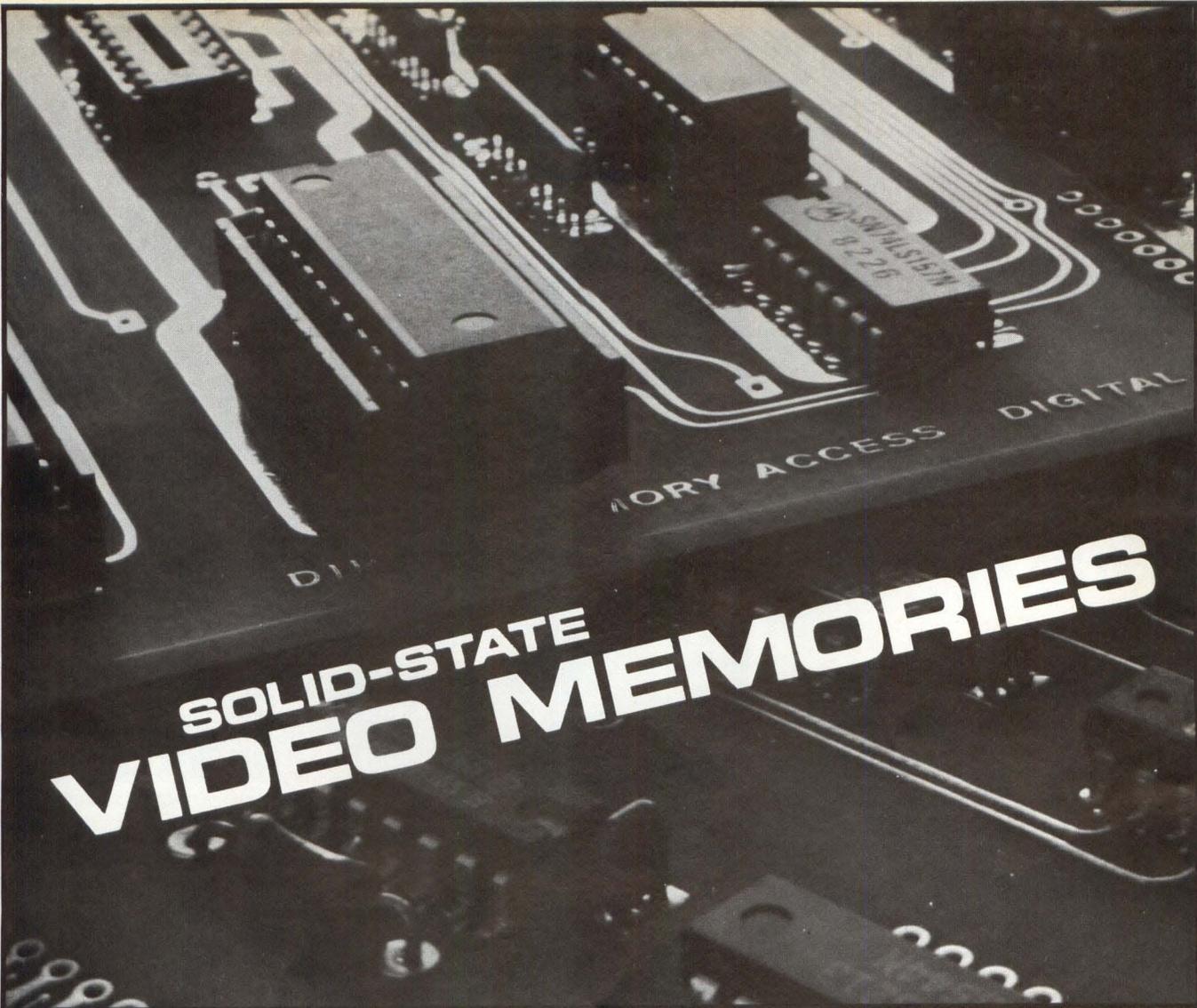
The Q280 Winchester disk drive from Quantum packs both 80 Mbytes of formatted capacity and a SCSI system-level controller into a half-high 5 1/4" package. A combination of sputtered thin-film media and Whitney heads helps storage density. The in-spindle motor permits three platters.

performing a time-consuming operation and, when finished, arbitrate for the bus and reconnect.

Thin-film media and small heads permit good density on the disk. By using 1,7 run length limited code, only 15,000 flux changes per inch are needed to record 20,000 bpi; with 876 tpi 13 1/3 Mbytes can be stored per disk surface. One servo burst is embedded for each of the thirty-two 512-byte sectors on a track. An in-spindle motor helps fit three platters plus controller into the 1.65" high box. Some systems with this motor design have suffered thermal problems. However, Quantum feels that its two- and three-platter drives will have less problem than full-high drives with six to eight disks. The base plate is also thermally coupled to the spindle to dissipate heat.

Evaluation drives are not scheduled until October, with volume production to begin near the end of the year. Although Xebec and Tandon are aiming to launch 5 1/4" drives with an integrated controller in the near future, probably neither company's product will top 40 Mbytes. And suppliers of higher-performance products, like Priam (San Jose, CA), have not yet announced comparable intelligent 5 1/4" drives. Makers of small multiuser systems, LAN file servers and graphics workstations will have more freedom with the combination of small size and high capacity. A tape backup or second disk drive can be used in a standard full-height 5 1/4" space. No slot is used for a controller. In addition, system builders or users will not need to match drive to controller or worry about defect mapping.

—Pingry

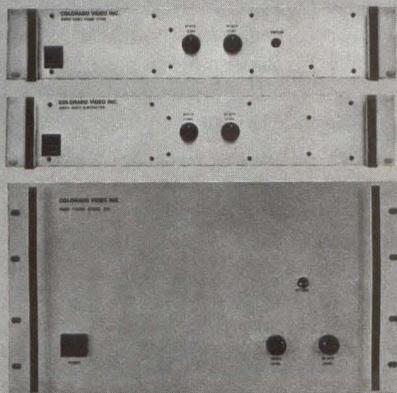


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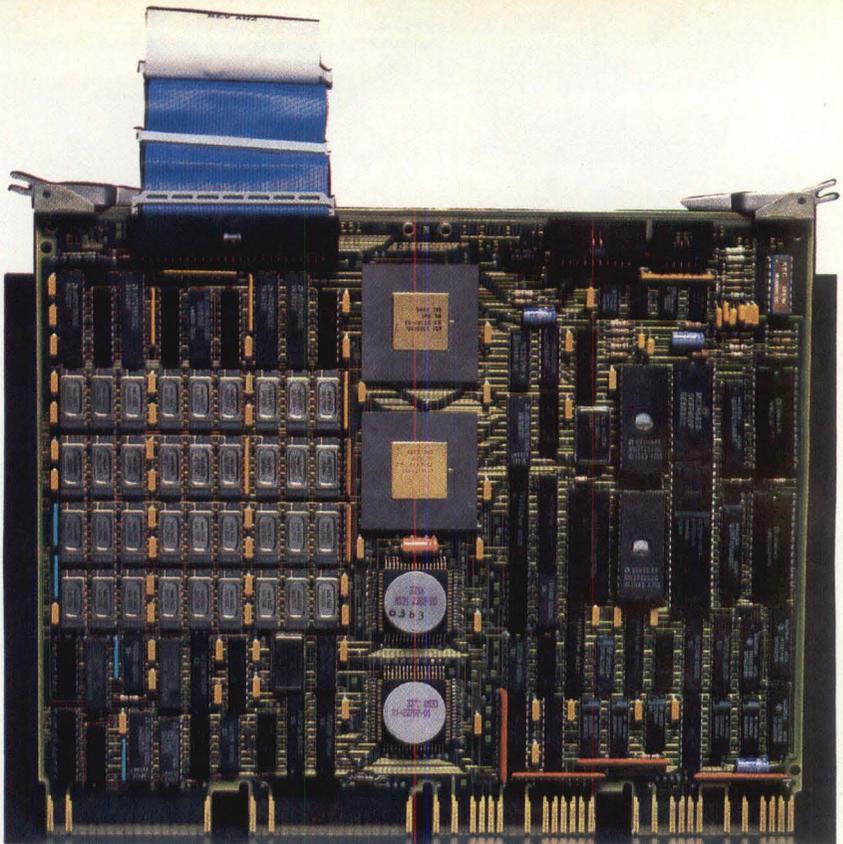
SYSTEMS

Digital Announces MicroVAX II

Two VLSI devices, a single chip processor with on-board memory management and a matching floating point device, form the heart of the latest MicroVAX product from Digital Equipment Corp. — MicroVAX II. Unlike its predecessor the MicroVAX I which implemented the CPU on two separate Q-Bus boards, the memory controller and the data path module, MicroVAX II takes advantage of VLSI devices to integrate the entire CPU on a single Q-Bus board. An over-the-top ribbon cable provides true 32-bit access to system memory; the Q-Bus is relegated to the task of I/O.

In terms of horsepower, existing customers of the MicroVAX II say that they are experiencing at least a two to one improvement over the MicroVAX I. Early benchmark tests run at Carnegie-Mellon University indicate that the machine runs at 75% the speed of the VAX 11/780 in a worst case scenario and normally at 80% to 90%. Some applications that were heavily register-oriented actually ran faster. The machine also seems to load down at the same level as the 11/780.

Although some initial concern was voiced about the limitations of the Q-Bus, it does not appear to be a performance-limiting factor for systems with a small number of users. Most customers are pleased at the range of drivers that DEC is providing, allowing them to configure the machine with a range of disk and tape drives. The only negative comments regarded the lack of color graphics in the workstation, a slack that will inevitably



The MicroVAX II CPU has been implemented on a single Q-Bus board. Included are the CPU and MMU and floating point unit.

be picked up by third party vendors.

The basic system configuration includes a MicroVAX II processor and floating point unit with 2 Mbytes of memory, RX50 dual 400-Kbyte 5 1/4" floppy drives and an internal 31-Mbyte Winchester disk. A second configuration has the same components as the basic configuration with the addition of two new DEC products, the RD53 71-Mbyte disk and a 95-Mbyte TK50 cartridge tape drive in lieu of the RX50 floppy drive and 31-Mbyte hard drive. Both of these configurations are packaged in the BA23 enclosure that DEC has previously used for the MicroVAX I and MicroPDP-11 line.

A third MicroVAX II system is intended for larger work groups and is packaged in a new BA123 enclosure. This system contains 3 Mbytes of main memory, an RD53 drive, an RX50 floppy and the TK50 streaming tape unit. In the same form factor, the fourth MicroVAX II configuration contains 5 Mbytes of main memory and three RD53 drives together with the TK50 tape drive. DEC will also provide a MicroVAX I to MicroVAX II upgrade kit.

Building on the MicroVAX II, DEC also introduced two VAXstation II workstations. They are both multiwindow, multiprocessing monochrome systems

that come with a 19" bit-mapped monitor, a keyboard and a three-button mouse. The screen provides a resolution of 864 × 1024, and both configurations are in the BA23 box. They include 2 Mbytes of main memory and Ethernet adapter, run Digital's MicroVMS operating system and workstation software and feature GKS graphics software as well as VT100 and Tektronix 4014 emulation. The basic VAXstation II includes the RD52 drive and the RX50 floppy. The enhanced version includes the RD53 drive and the TK50 streaming tape.

Expected early next year, MicroVAX III is expected to depart from the Q-Bus and use DEC's new BI bus structure. This may be of concern to some OEMs, since it may be impossible to upgrade MicroVAX I and II systems to MicroVAX III. However, DEC may cultivate third party vendors to provide a range of board-level products by the time of the announcement. Furthermore, the higher performance of the new bus will be worth the upgrade penalty. Over the next four to five years, DEC's PDP-11 architecture, limited by its addressing space, may be phased out as users demand the higher performance, lower cost VAX demand paged virtual memory machines.

—D. Wilson

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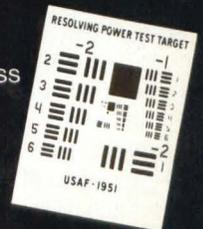
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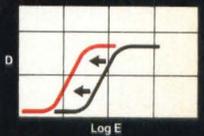
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Machine Vision Finds New Applications

by Hugh Aldersey-Williams, Contributing Editor

Machine vision has come a long way in the last year. This much was clear at the Society of Manufacturing Engineers' (SME) first Vision '85 show, held in Detroit at the end of March. Machine vision systems are beginning to make their mark in a range of industries. Certainly, heavy manufacturing will remain one area where much vision equipment is installed. Now, however, the technology has advanced to a point where it is applicable to packaging and to the manufacturing of consumer goods. Aside from manufacturing, it is being used in processed food production and in agriculture.

The extended range of applications for machine vision systems is made possible by advances in the technology of the sensors and processing architectures used. Faster processing in more highly parallel architectures allows images of higher resolution with gray scale or color information content to be analyzed at rates compatible with the rate of an industrial production line. Such added detail is vital to the inspection of nonstandard items (produce, for example) and items where a number or range of colors may occur. Food inspection needs this requirement with the additional demands placed by very high production throughput.

The addition of high resolution, gray scale and color detecting and processing capability is an indicator of one trend in the evolution of machine vision systems—toward a general-purpose multitask apparatus. On the other hand, more specialized systems are also being developed, tailored to specific applications.

Development Directions

The dichotomy between the two sorts of machine vision system—the general and the task-tailored—demands development along different technological lines. The most obvious trend is to devise a system that most closely imitates the operation of the human eye. This is the route being followed by those companies now introducing gray scale, high resolution, and color processing capabilities at high update rates.

Machine vision systems have developed to the point where some are capable of handling images of up to 1000×1000 picture elements. Up to 32 bits per pixel of gray scale (more than four billion shades) can be offered, though six or eight (64 or 256 shades) are more common. Update rates of images are typically 30 Hz. Some color perception and processing is being developed, and depth ranging to give three-dimensional vision is also on the way. However, these qualities are not all simultaneously available on any system.

The eye does combine these areas of functionality. It can process images at least the equivalent of $10,000 \times 10,000$ pixels



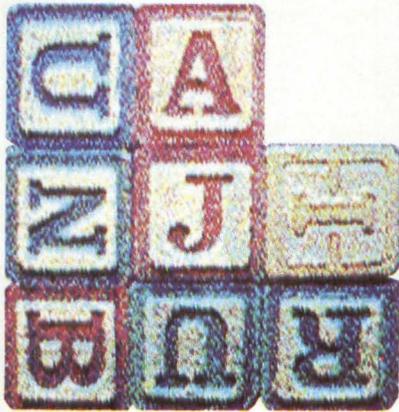
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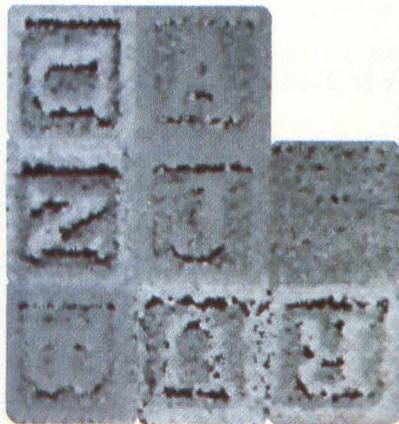
(b)

at over 30 frames per second. It has no trouble accepting three-dimensional data and simultaneously perceiving many levels of gray (generally put at something less than the 64 levels of 6-bit data) and millions of colors. Commercially available machine vision systems processing images at video rates are limited to scenes of up to about 80,000 (240×320 , for example) elements with a 6-bit gray scale. This means that the processing power behind the vision sensor must operate at $80,000 \times 6 \times 30$ operations per second or around 14 MOPS. This capacity must be built into the buses and A/D converters used in the vision system. The problem can be multiplied when the application demands that more than one camera send data to the central processor.

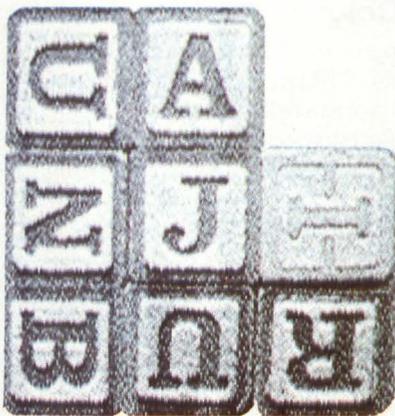
The new Vision Inspection Processor (VIP I) and the existing



(e)



(d)



(c)

Figure 1: True color processing is used by International Robomation/Intelligence. This sequence of images shows: (a) black-and-white video input, (b) color video input, (c) hue-encoded black-and-white output, (d) sampled black-and-white output, and (e) sampled encoded color output.

8000 from Itran (Manchester, NH) provide examples of systems with an option of high resolution. Up to 1024×1024 image resolution is available at a frame rate of 15 Hz. This makes possible inspection in more detail and of larger areas, says Itran's president, Stanley N. Lapidus. Up to 13 times the area coverage of other vision systems is also possible. VIP I can support up to eight cameras and is software-expandable. A second new product, the VIP II, does not accept the high resolution option. It has standard software and can support up to four cameras.

Because the higher resolution allows larger areas to be seen, it cuts the number of cameras needed in certain applications. Less space is needed for system installation; and easier maintenance, faster system programming and faster inspection speed result, claims Itran.

Machine vision systems are now doing more than checking car and electronic components, thanks to faster processing architectures.

Itran's 8000 was an early system which incorporated gray scale processing capability. The Pixie-5000 system from Applied Intelligent Systems (Ann Arbor, MI) is another design that offers both high resolution (1024×1024) and gray scale to eight bits deep. The system can also operate at 256×256 resolution with 32 bits per pixel and at various intermediate stages in resolution and gray scale capability.

The Pixie-5000 uses cellular automata technology whereby areas of the image are allocated to individual processors. Similar technology is used in equipment from two other Ann Arbor companies, Machine Vision International and Synthetic Vision Systems (*Electronic Imaging*, February 1985, p. 46). The cellular automata or Cytocomputer idea was developed locally at the Environmental Research Institute of Michigan (ERIM). The AIS design uses up to 1024 tightly coupled processors and static CMOS memory. The company claims this architecture gives a rate of up to 3.5 billion neighborhood operations per second. The bottleneck now, according to Stephen S. Wilson, vice president of research and development at AIS, becomes the camera throughput. He cites ceramic inspection as one area where very high resolution is needed to spot very fine faults.

True gray level vision capability has come about, according to Gary Rutledge of GMF Robotics (Troy, MI), as a result of available hardware which allows image data to be processed at video rates. GMF Robotics is making the move to incorporate vision in its robots with the announcement of three vision systems—GMF Arcweld, GMF V300 Grayscale Vision, and GMF V200 Grayscale Vision. "By 1990," says president Eric Mittelstadt, "if it doesn't have vision, you won't call it a robot."

According to Rutledge, many of the separate elements we see today will be integrated in a robot of the future, particularly vision that can cope with standard ambient lighting and contrast variation among its parts for inspection. The eventual aim is also to integrate two- and three-dimensional guidance.

Analysts estimate that only 10%-15% of the machine vision market will be for "robot eyes" in systems like the GMF V300, which allows for six degrees of freedom enabling the robot to perform an operation on a car body only loosely oriented on an

assembly line. Until now, it has been more cost-effective to locate parts to be inspected precisely. This type of system may be expensive to reprogram when there are changes in the model being assembled. Instead, it is now economical to build the flexibility into the inspection end of the set-up. Rather than locating the part being produced to within a fraction of a millimeter, it becomes practical for the vision-guided robot moving part to zero in accurately on the part for assembly.

Perceptron's (Farmington Hills, MI) MV-60 Visual Fixture system is an example. The system has been configured on a Detroit car production line to apply sealant to a body placed by the system to within 0.5 mm. Three stereo feature sensors and auxiliary floor lighting are used to give fixturing within five seconds.

The GMF V300 is intended for use in car windshield insertion, doors and hood placement within the automotive industry. The GMF V200 has only the one camera and therefore two-dimensional vision capability. Uses are limited to applications where identical parts are accurately positioned.

The gray scale ability of both GMF devices allows them to work by picking out edge detail even where the contrast is very low. Eight-bit gray scale is possible on the IVS-100 machine vision system from Analog Devices (Norwood, MA). The machine comprises an Intel 80286-based CPM, a frame grabber board for $512 \times 512 \times 8$ -bit images and an optional array processor on a 10 Mbyte/sec bus. In addition to the 256 gray levels there is a $512 \times 512 \times 1$ -bit memory for overlay to highlight features on an acquired image. Multiplexing allows the IVS-100 to process new images while slower robotic systems respond to commands as a result of previous image frames.

Datacube (Peabody, MA) is one of the companies supplying boards for machine vision applications. It has recently announced a range of boards on the VMEbus, the bus that currently looks most likely to achieve widespread acceptance in the machine vision field. Datacube's product, Maxvideo, provides for storage, display, signal processing and real-time image acquisition. The boards are comprised of Digimax, for A/D and D/A conversion; Framestore, a storage module with three $384 \times 512 \times 8$ -bit frame stores on a single VMEbus card using 256K DRAM technology; VFIR, for linear pixel processing; SNAP, a systolic neighborhood array processor operating on



Figure 3: The IVS-100 machine vision system from Analog Devices.

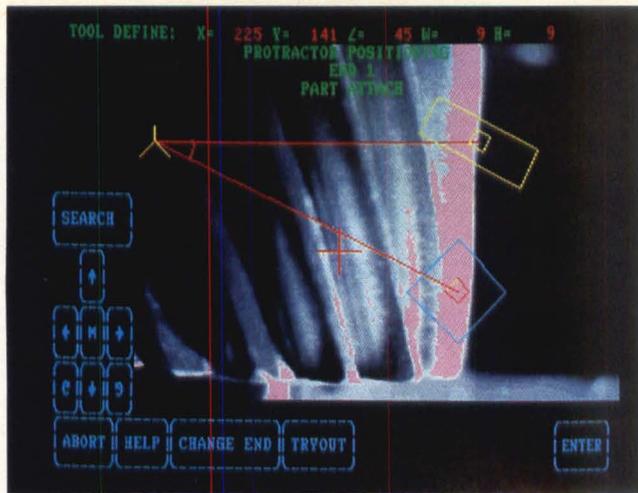


Figure 2: Itran's 8000 machine vision system image display with graphics overlay.

a 3×3 kernel; Featuremax, for real-time histogram and feature list extractions; and Max-SP, a general-purpose signal processor module.

A seventh board, Protomax, acts as a prototyping aid to allow the user to develop Maxvideo-compatible modules suited to a specific application. The boards communicate along a 10 MHz Maxbus. Datacube's aim in developing the Maxvideo architecture was to meet the machine vision industry's need for system configuration. Maxvideo is not a true general-purpose design, according to Datacube, but can be configured in a number of ways to meet a range of user needs. Another supplier of image processing boards, Imaging Technology (Woburn, MA) has agreed with Machine Vision International to sell \$2.4 million of its IP-512 modules for MVI's product range.

Dabbling With Color

Some machine vision systems are also able to detect color. AIS's Pixie-5000 has three parallel 7 MHz input channels optionally available to allow it to operate as a real-time full true color image processor. This is one of a few systems at present offering true color capability (not to be confused with the pseudocoloring sometimes used to highlight areas of interest in inspection tasks where there is human verification).

International Robotation/Intelligence (Carlsbad, CA) is another company looking at color vision. An easily overlooked problem in color vision processing, according to IRI's James C. Solinsky, is that the processing is multiplied not just three-fold (for red, green and blue channels) but nine-fold to allow for both individual channel processing and correlation. The advantage of color is that it rapidly provides accurate information. Color processing will allow machine vision to be applied in industries where it is currently useless in its limitation to monochrome image analysis. Food, agriculture and color printing will be among the areas to benefit.

Solinsky favors a two-channel system, capable of handling color and black-and-white scenes. This allows maximum flexibility of operation, with gray scale better at separating some colors, and encoding better for others. Eight-bit black-and-white output, for example, could be used either to give pseudocolor for a global view or contrast colors for local detail. Eight-bit RGB output gives true color reproduction.

The addition of more gray scale, color and higher resolution contributes to machine vision systems with greater similarity to the human eye. These general-purpose machine vision sys-

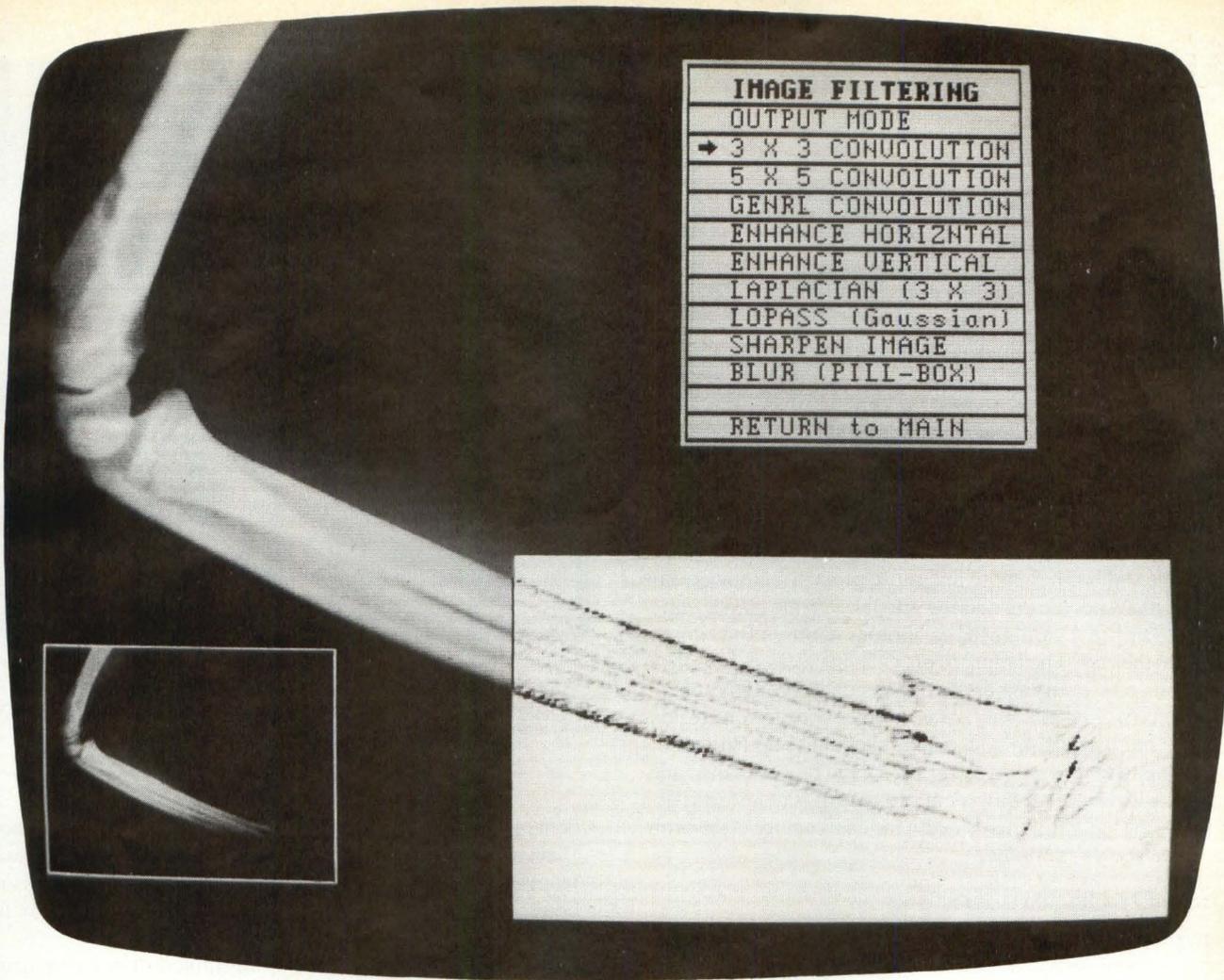


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	5 X 5 CONVOLUTION
	GENRL CONVOLUTION
	ENHANCE HORIZONTAL
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tems take a more global view of the environment within which they are expected to work. Such an approach is clearly valid when the task is one where the eye functions well. For example, a vision-guided vehicle would need to take such a view to interpret the variety of scenes that it will intercept and to negotiate its path through a range of surroundings.

The human eye, on the other hand, is notoriously bad at repetitive inspection tasks. According to research done at the University of Iowa, people asked to perform the visual sorting task of picking out a small minority of black ping-pong balls from a production line of white ones, reduced efficiency to only 85%. Even with several operators at the same line, no more than a 95% success rate was achieved.

It is not always appropriate, therefore, to follow the example of the eye and build in more and more processing power. The mistake many people are making is to fall into the classic entrepreneur's trap of regarding the technology as the end and not the means to the end. The failure to provide the necessary application focus was a rallying cry at the Vision '85 conference.

The increased availability of faster processing hardware does not demand that vision systems architects necessarily incorporate it into their designs. Many tasks can be performed adequately with simpler equipment. To incorporate more vision power is one answer; pinning down the exact nature of the problem to be solved is another.

Lack Of Understanding

High-powered processing may be overemphasized. There has been some concern that there is more technology now than is needed and a lack of understanding of manufacturers' real problems. Some experts don't believe the human model is a proper model for vision systems. Just as man never made an airplane that flapped its wings or a car with legs, so makers of machine vision equipment should stop looking to the human visual system for their inspiration. According to James West, vice presi-



Figure 5: Cyto IV three-dimensional image of a bin containing parts to be picked out by robot arm. Vertical relief was pseudocolored from processed data collected by laser range finding.

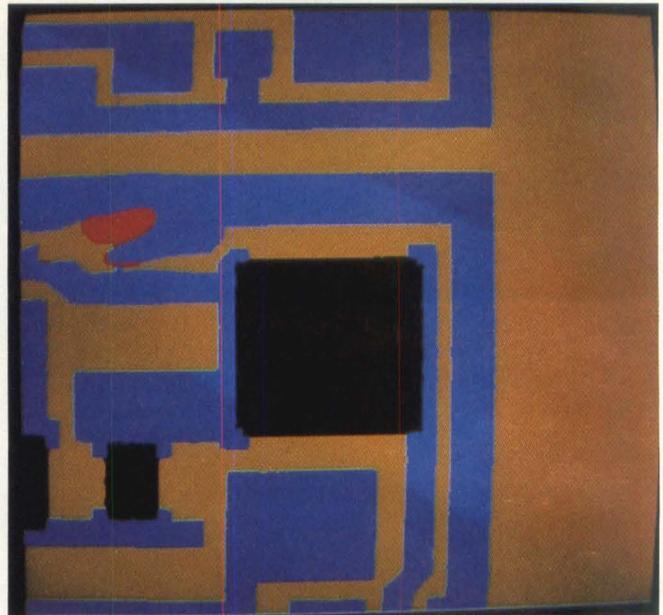


Figure 4: Pseudocolor is used on the Synthetic Vision Systems' Cyto IV pipelined cellular image processor to highlight defective areas (black) on a thick-film circuit. This facility aids operator interpretation; processing is executed with binary and gray scale powers only.

dent of Perceptron and chairman of the Vision '85 conference, "Successes of the last few years can be attributed to getting away from the human model." Nonetheless, this greater processing power is one factor opening up new fields of application for machine vision systems.

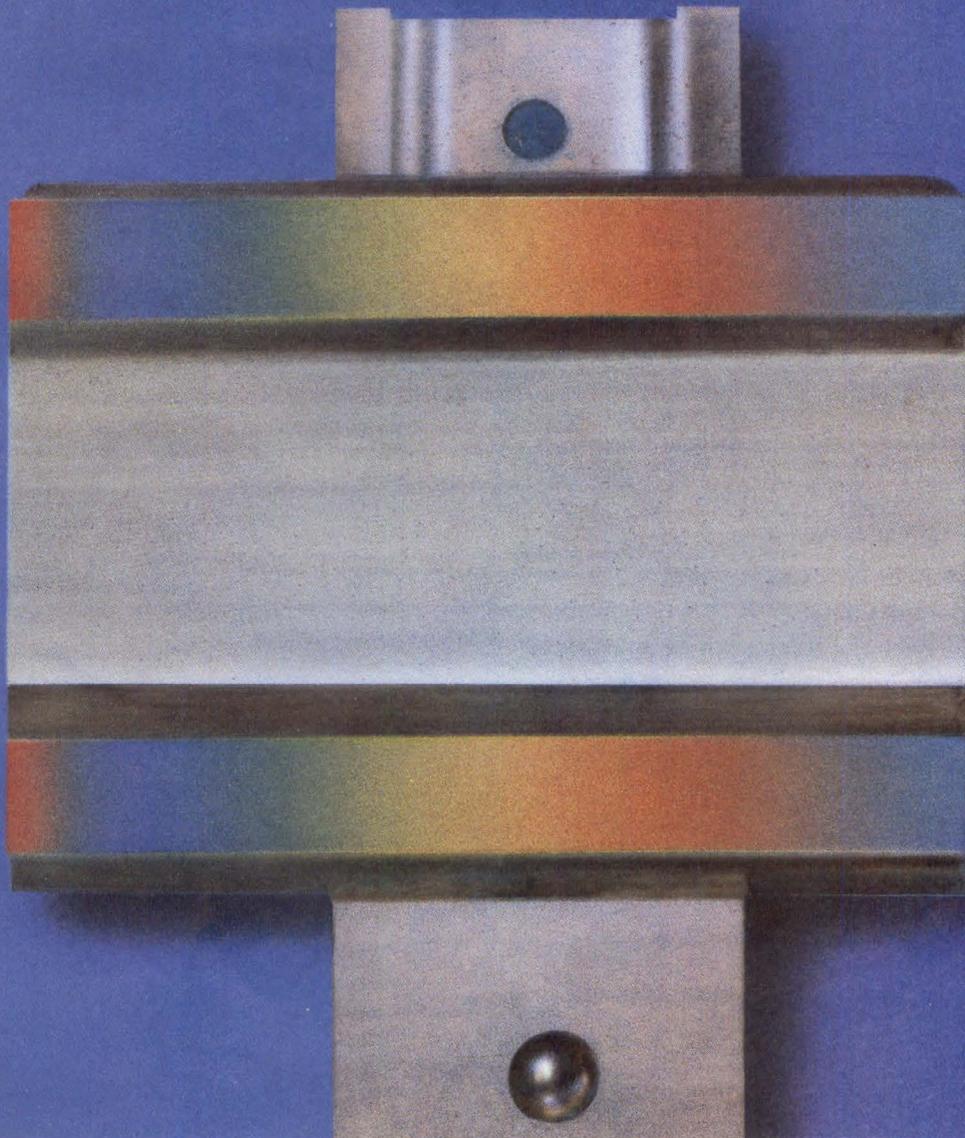
Whereas previous systems were limited to manufacturing applications, high-powered vision equipment is starting to move toward other applications. "Machine vision transcends manufacturing," says Nello Zuech, a consultant at Vision Systems International (Yardley, PA). He believes the Machine Vision Association should cut its ties with the Society of Manufacturing Engineers.

Zuech is looking ahead to new applications. "The impact of machine vision on services will be vast," he says. Systems will find uses in analytical laboratories for automatic sample preparation and in construction where vision-guided robots could perform tasks such as bricklaying. But agriculture and food production will be one of the largest and most immediate of the new markets. Machine vision here, says Zuech, could be applied right from crop planting and picking through process and quality control of the final form of the food product.

Processed food is already being inspected by computer. Octek (Burlington, MA) has a gray scale machine vision system which examines the color of pizza crusts to see if they are burnt. Key Technologies (Grosse Ile, MI) has a similar system for looking at french fries. In both cases, although it is the color of the product that is being examined, the camera is monochrome with an appropriate color filter and gray scale capability. The Key Technologies design makes do with a linear array, illustrating the comparative simplicity of a technique that can still be used to meet exacting inspection requirements.

Where gradations of one color are being examined, as in these applications, a filtered monochrome camera suffices. Where a number of known colors are expected, gray scale inspection can still be used, with suitable thresholding of the gray levels to separate the different colored parts in the image for analysis. Work at Arthur D. Little (Cambridge, MA) has con-

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centrated on gray scale techniques in the inspection of mixed vegetables and TV dinners by this method. The problem is more complex where a number of colors are expected, but it is not known exactly what colors may occur. Here, true full color processing, with its attendant greater demand on computer time, is the only answer.

Texture analysis is another technique which offers valuable analysis powers, but which has been too expensive in processing time in the past to incorporate into vision equipment. The surface texture is conveyed not in the pixel values only, but in the variations of gray level or intensity between the image pixels. Texture as perceived by a vision camera may vary greatly, depending on the prevailing lighting conditions and direction. Humans can easily understand such variations and still correctly inspect an object. For a computer, an averaging operation may be needed before further texture analysis to balance the lighting level across the object.

The degree of randomness of light reflected from a surface is what is being measured. However, it is very difficult for a computer vision system to distinguish between different types of randomness. We know what we mean when a surface is dimpled (a golf ball) or wrinkled (a walnut), but the problem is less trivial for the computer.

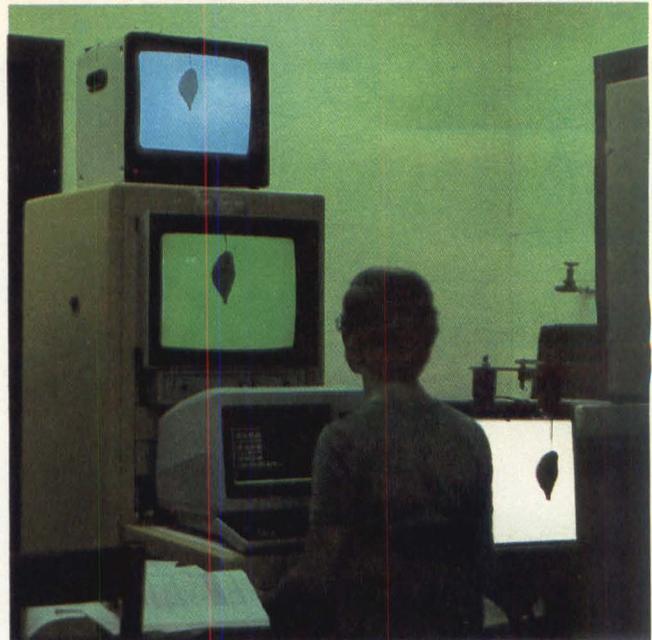
Agricultural Challenge

The convenient constraints of uniform size, color and orientation that may apply to man-made objects cannot be exploited in agriculture. For machine vision to make the transition from the factory, where environmental conditions and product uniformity are guaranteed within known tolerances, to the outside world, where conditions vary and where there is no standard product, is the result of image processing hardware advances.

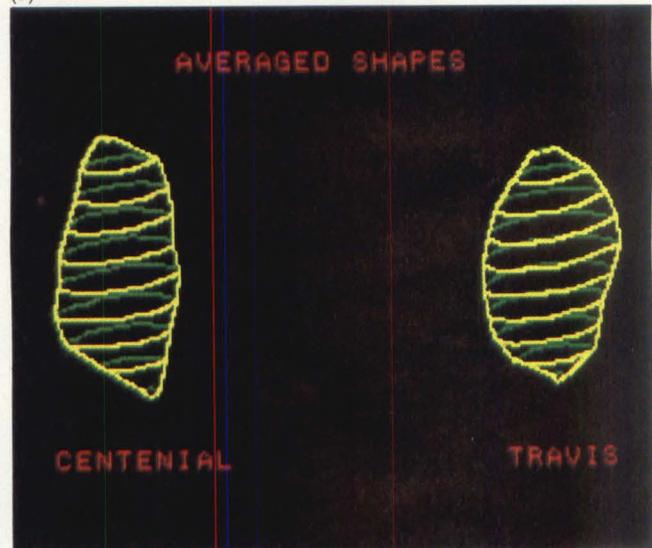
Machine vision must overcome the problem of texture and color analysis to gain a hold in the enormous food and agriculture industries where quality is largely judged by these criteria. Coupled with a robot arm, there is great applications potential for such equipment. In current machine harvesting, for example, harvesters pick all the crop in one pass. A more sophisticated harvester with a machine vision system aboard could select just the ripe items by their size and color. Unripe produce would remain on the plant for picking at a later date. According to Roger Brook, of the Agricultural Engineering Department at Michigan State University, a machine vision system could select between ripe and over-ripe red strawberries and unripe strawberries in both white and green stages of growth. At present, machine-picked strawberries are a mixture of this type and are only suitable for low-grade uses. Machine vision would allow the selection of the more valuable berries only.

Other agricultural machine vision applications are also the current subject of university research. At the University of Florida, researchers are looking at a system to pick citrus fruit. Citrus fruit are comparatively easy to detect using a filtered monochrome camera because they contrast well with the leaves of their plants and have a long time slot during which most of the fruit is ripe. The prototype system evaluates the centroid of the fruit at 1/15 second intervals as the robot arm swings in to pick it.

Today's machine vision systems are having a profound effect on not only heavy manufacturing industries but also consumer



(a)



(b)

Figure 6: (a) Apparatus at Louisiana State University for measurement of shape and volume of sweet potatoes. This work will form the basis of a sorting and grading system, and as a way of evaluating harvester effectiveness. (b) Average shapes of two sweet potato varieties.

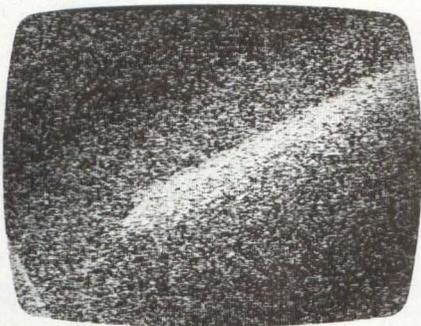
goods, processed food and agricultural industries. At present machine vision is generally a "black and white" technology; however, the industry will progress to using color for applications which will need color differentiation. Because of this, parallel processors and systolic architectures will lead the way to high-performance machines capable of emulating the human visual process. One final barrier, that of interpreting these images in a rapid and knowledgeable fashion, will be overcome by the use of artificial intelligence techniques, now in development.

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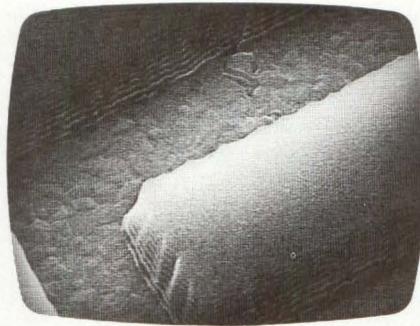
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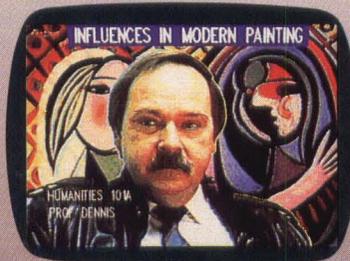
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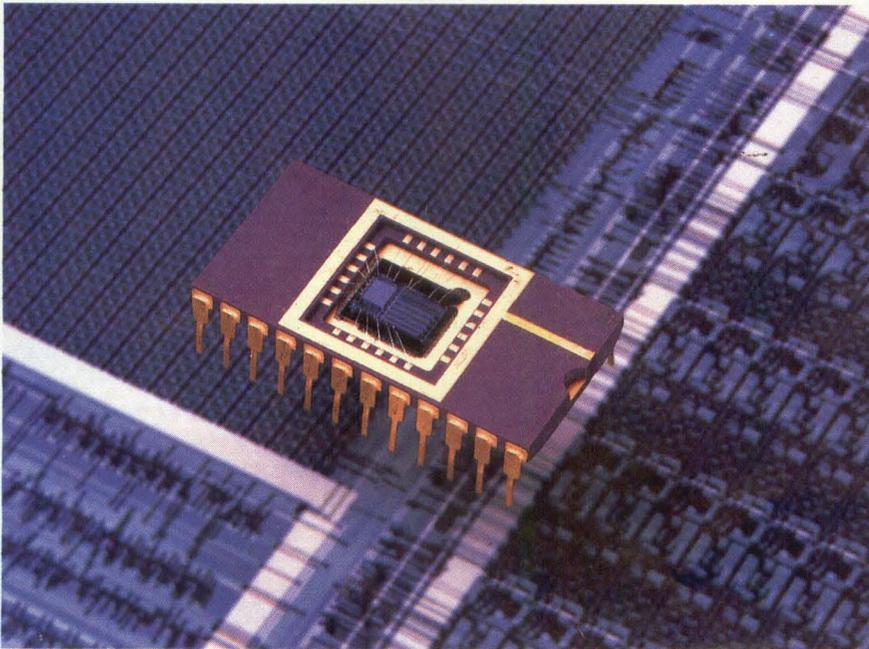
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Speech Recognition: Not A Typical Engineering Problem



The KSC 2408 Digital Filter chip from Kurzweil Applied Intelligence features 24 bits of data resolution. It is an example of custom-designed silicon chips recognition system designers are using to achieve high accuracy recognition.

Speech recognition systems designers have the task of making machines understand speech like humans, although the human process is not completely understood.

by Brita Meng, Technical Editor

Of the two speech technologies, recognition has always lagged behind synthesis. Indeed, progress in speech recognition appears disappointingly slow in comparison to the advances made in speech synthesis. Developments in synthesis have helped to drive those in recognition; however, automatic speech recognition is not a typical engineering problem. Areas of research such as physiology, phonetics, linguistics, statistics, chip design, signal processing, and probability theory all must be combined for a solution to the interdisciplinary problem of speech perception.

Although activity in speech recognition has increased somewhat in recent years, commercial machines have not as yet reached the point of understanding speaker-independent, continuous speech. The goal may become more realistic as hardware drops in price and as advances in algorithm and software occur. Nevertheless, whether the system is speaker-independent or speaker-dependent, isolated or continuous, the problem of recognition remains the same: how to develop a machine which emulates the way humans interpret speech.

Human Factors

Human perception of speech is a complicated procedure, involving both frequency and temporal analysis of information. When speech enters the outer ear, it does so as instantaneous pressure waves. These waves cause the tympanic membrane (eardrum) to vibrate; the resulting mechanical impulses are transduced to neural and electrical ones inside the cochlea, where small hair cells connect with the neurons that feed the central nervous system.

Because each neuron responds to a distinct frequency within the sound stream, a frequency analysis of the speech information occurs. This frequency mapping is maintained throughout the central nervous system. In addition to frequency, the auditory neurons code the pressure waveform into time domain electrical spikes for relay to the central nervous system. The discharge rate and the timing of the spikes aid in decoding the original waveform into perceptual information.

Whereas humans employ both temporal and frequency analysis to perceive speech, most speech recognition systems utilize only frequency domain analysis. It is much more difficult for

a machine to separate the various words and phonemes from each other within a constant stream of sound, as in continuous speech (Figure 1). Isolated or discrete speech, where words are separated by the speaker, sounds less natural to the human ear (Figure 2); however, it takes the job of finding beginning and end points of words away from the recognizer and puts the burden of clear boundaries on the speaker.

Strictly speaking, no available machine or system is capable of continuous speech recognition. Rather, those recognizers which do not fall into the isolated or discrete category are connected word recognizers. Dave Crabbs, senior engineer at Interstate Voice Products (Orange, CA) compares connected speech to the speaking style a person uses when dictating; the speech maintains a certain amount of distinct articulation. Continuous speech is the form of speech to which humans are most accustomed. Humans have no problem recognizing a phrase pronounced "Didja wanna go" as "Did you want to go."

Humans also have an innate capability, difficult to duplicate in a machine, to disregard factors affecting speech. Voice patterns vary from speaker to speaker depending upon sex, age, education and geographic origin; a syllable, word or other speech element may sound different because of loudness, speaker stress and pronunciation rates. Many recognition systems manufacturers have therefore concentrated on developing speaker-dependent recognizers which can be trained to specific users, rather than speaker-independent machines.

Speaker-independent speech recognition systems offer the advantage of unknown user access, even though their vocabularies are not as robust as those in speaker-dependent machines. The differences in vocabulary size between the two technologies have been somewhat overcome by using operational grammars for speaker-independent recognizers. Memory requirements, usually the main constraints on vocabularies for speaker-dependent systems, are not as stringent. In speaker-independent technology, the memory needed for one user is the same as that needed for 1,000 users. However, the biggest disadvantage today with a speaker-independent system is the fact that it can only use a fixed vocabulary. There is no way to retrain the system for new words.

Speaker-dependent technology has several advantages over speaker-independent technology. High performance is, relatively speaking, easier to achieve—even at vocabularies of over 40 words. The primary advantage of speaker-dependent systems is word flexibility. Changing vocabularies can be accomplished by merely retraining a system. Another important aspect of these machines is the ability to change speaker microphones by retraining. On the other hand, depending on the size of the vocabulary, training may be an exhaustive process, a disadvantage that results from the system's benefits.

More designers and users are becoming aware of system training, a necessity for all speaker-dependent recognition systems. In many ways, the quality of training for each user reflects upon the performance of the machine. Training a machine is not a complicated task: a speaker must create templates (digitized representations of vocal input), the parameters against which input speech is later compared for recognition, by speaking each vocabulary word into the machine for analysis and storage.

Depending on the number of words in the vocabulary and the number of times the system needs a word repeated in order to

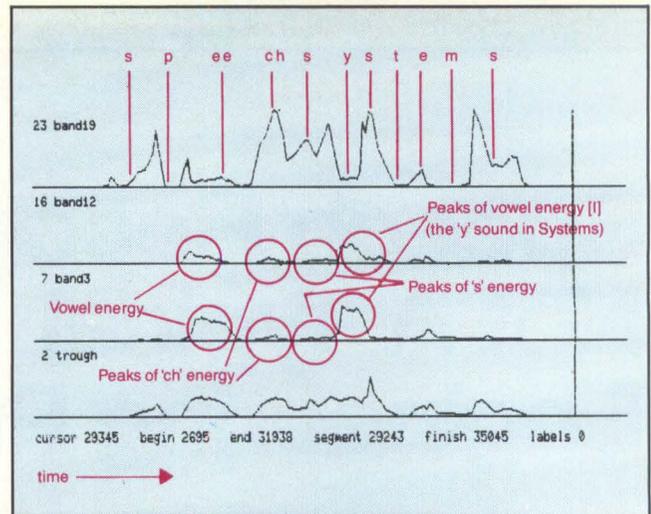


Figure 1: This is a sample of the phrase "speech systems" said in continuous speech. Detecting word boundaries is a primary problem in developing a continuous-speech recognition system. The masses of energy in the top parameter and the trough are noticeably joined at the "ch" and "s" between words. Although the two sounds seem at first glance to be indistinguishable, examining the energy components over different frequency ranges (the two middle bands in the figure) show that "ch" has more energy in lower frequencies than "s" does.

create an averaged template, this procedure for a speaker-dependent recognizer takes time and computer memory. According to Paul Mangione, director of marketing at Speech Systems Inc. (Tarzana, CA), a training period of more than 30 minutes may deter some users from employing the machine. For example, Interstate Voice Products, which makes several recognition products using template matching techniques, recommends that at least three passes during training be made for high accuracy recognition.

Speech Systems Inc., a company developing a speaker-dependent, connected speech-to-text dictation machine, is attempting to limit user enrollment time for its machine to less than 15 minutes by providing templates of various accents, dialects and sexes with the system. To train the machine, the user simply inputs selected words which determine speech patterns; the recognizer chooses the group of templates which most closely resemble the patterns of the user. Those templates are

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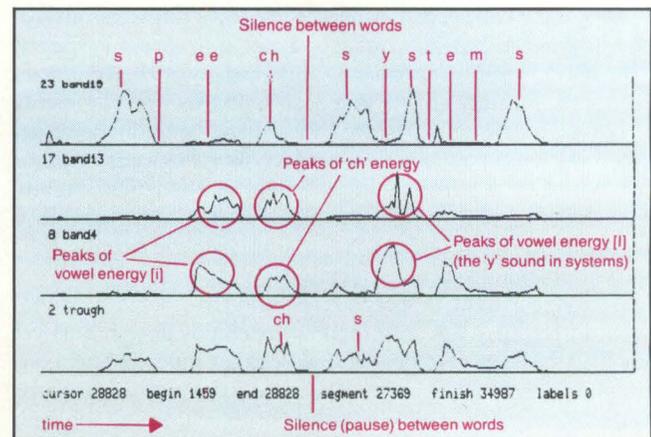


Figure 2: This is a sample of the phrase "speech systems" said in isolated or discrete speech. A gap separates the two words in all frequency bands and represents the silence between the "ch" sound in "speech" and the "s" sound in "system".

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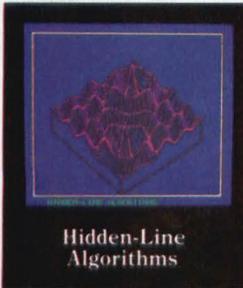
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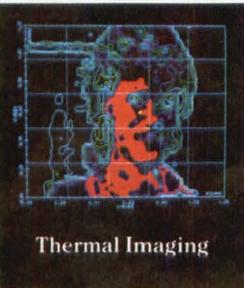
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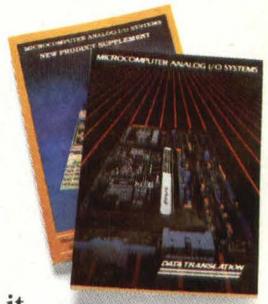
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then used whenever the user works with the machine. This training procedure is similar to the one used at IBM's Thomas J. Watson Research Center (Yorktown Heights, NY) for its experimental office dictation machine. A training document of 1500 words must be read in order for the machine, which has a statistical data base of 5000 words, to be able to recognize the speaker's voice.

System Factors

In speech recognition systems, the software models and algorithms, not necessarily the computer hardware, are the vital components. This is not to say, however, that hardware requirements are not important. A speech recognizer typically includes some form of analog-to-digital (A/D) converter; a processor, which supervises input signal analysis and pattern matching; and memory, which stores the reference patterns. With memory and converter prices rapidly dropping, the processor has become the primary hardware expense in building and developing a recognition system.

Several companies use off-the-shelf digital signal processing chips such as the Texas Instruments (Houston, TX) TMS-32010 in recognition systems. The chip was considered a breakthrough by many system designers because of its ability to address large instruction memories, a requirement imposed upon a system because of spectral analysis. Among the products using the chip are Votan's (Fremont, CA) VPC 2000, Texas Instruments' Speech Command and Verbex's (Bedford, MA) Model 4000.

With the availability of the TMS-32020, manufacturers may be able to shrink board and system sizes because of its increased

processing capability. One company currently evaluating the chip uses three 32010s in its recognizer; it may be able to replace those three digital signal processors with one TMS-32020.

The alternative to using such off-the-shelf processors is custom-designed filter and processing chips. According to Thomas Schalk of Voice Control Systems (Dallas, TX), such VLSI processors, which are optimized to run proprietary pattern matching algorithms, may be the best way to maintain high performance recognition as well as to develop relatively low-cost speech recognizers.

The KVW under development from Kurzweil Applied Intelligence (Waltham, MA) is a 10,000- to 15,000-word, isolated, speaker-dependent voice-activated typewriter. The primary element in the system is a customized VLSI filter circuit, the KSC 2408, which can sample at rates of 125 kHz with 24-bit data coefficients. Eight second-order filters can be programmed to create up to sixteenth-order filters. Bob Joseph, director of marketing at Kurzweil, claims each one of the filter circuits provides the equivalent of forty 68000 processors in speed to run the company's algorithm. The KVS-3000, a 1,000-word recognizer scheduled for production in the third quarter this year from Kurzweil, contains eight of the filter chips; the KVW contains twenty-five.

Several companies, including Kurzweil, either sell or plan to sell the filter and processing chips used in their recognizers separately from the systems. Interstate Voice Products produces the VCRI00-2A, a chip set included in its board-level product, the VRT300, which is aimed at the DEC VT100 terminal and compatibles. The chip set, as well as the board, has a vocabulary of 200 words and is a speaker-dependent, isolated-word system. NEC Electronics (Mountain View, CA) has produced a three-chip speech recognition set which allows a speaker-dependent, isolated-word system to be implemented with a

Performance Issues In Recognition

by Thomas B. Schalk and
Amy H. Snodgrass, Voice Control Systems

Commercially available speech recognizers exhibit a wide range of recognition performance. To assess performance, recognition accuracy of the system must be measured. In a crude sense, recognition accuracy refers to the percentage of time that the recognizer correctly classifies an input utterance. Recognition accuracy depends on a number of factors: whether the system is speaker-dependent or speaker-independent, whether the system is a discrete- or connected-word recognizer, the difficulty of the vocabulary, the cost of the system and the environment in which the system is used. If one had a recognizer that operated on continuous speech, did not require user training, operated on very large vocabularies and rarely made an error even in noisy environments, it would be a human. Technology cannot duplicate the capability of the human in speech recognition,

although this is the objective of many research activities in the technology.

There are three types of errors that a recognizer can make. One type, called a substitution error, is said to occur when an incorrect word is hypothesized for a valid input utterance. For example, if a "two" is hypothesized when a "nine" was actually spoken, then the recognizer is said to have made a substitution error. In general, substitution error rates must be less than 3% for user acceptance.

Another type of recognition error is a rejection error. A rejection is said to occur when a valid input utterance is not classified by the recognizer. When rejections occur, the user simply repeats the utterance until it is recognized. These errors are not as obnoxious as substitutions and should not occur more than 5% of the time. Substitution and rejection error rates tend to decrease as the user becomes

more accustomed to using the system.

A third type of recognition error is a spurious response error. A spurious error occurs when an invalid input sound, such as the sound caused by dropping the microphone or uttering a word not found in the vocabulary, is classified as a vocabulary word. It is not feasible to quantitatively measure the spurious response error rate for a given recognizer. To do so would involve collecting a database of all possible sounds that can occur. Nevertheless, if such a database did exist, spurious response error rates of 50% would not be surprising for a typical recognizer. Ideally, a recognizer should reject all spurious input, but today, no recognizer is immune to it. Spurious responses can be minimized by either using push-to-talk microphone arrangements or close-talk microphones or a combination of the two.

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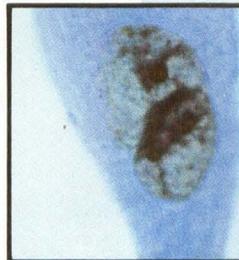
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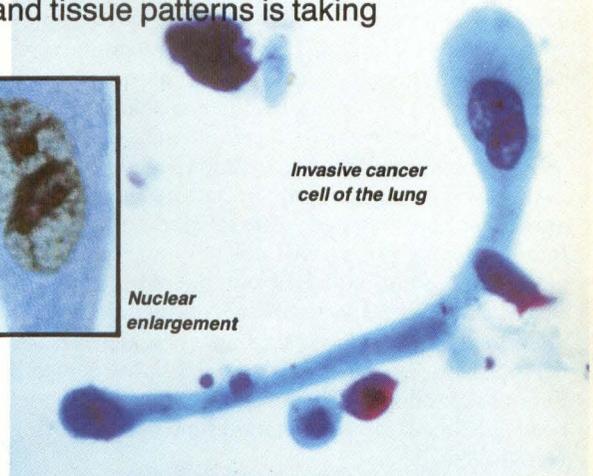
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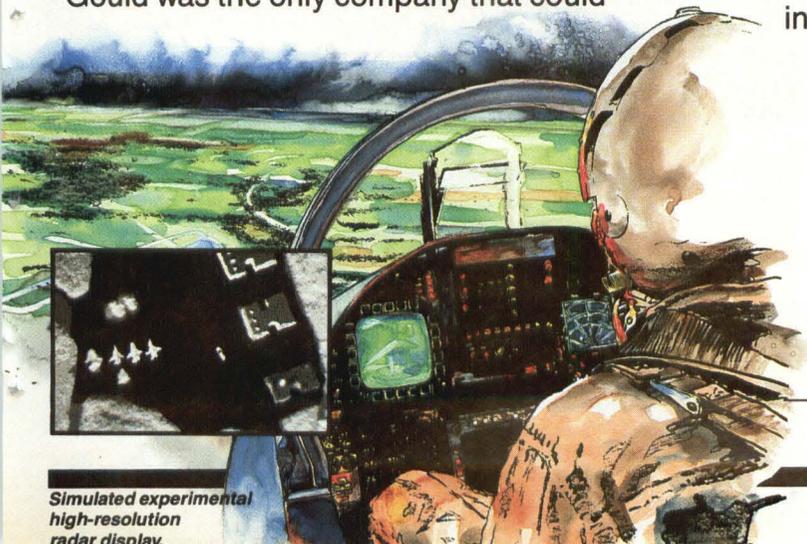
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minimum amount of hardware. The MC-4760 acts as the analog interface, the μ PD77661 as the analysis and matching processor and the μ PD7762 as the system control processor. Intel (Santa Clara, CA) and Dragon System Inc. (West Newton, MA) are examples of other companies offering chips or chip sets for recognition.

Some recognition methods require such massive amounts of computing power for real-time operation that array processors and mainframe computers are not fast enough. In such cases, some designers have resorted to parallel processing. Kurzweil uses its filter because it provides a degree of processor parallelism needed to achieve large vocabulary, real-time recognition. IBM's experimental speaker-independent, isolated-word dictation machine uses an IBM 4341 mainframe coupled with two array processors. Verbex (Bedford, MA) uses a bit-slice architecture to carry out signal processing and pattern matching for its speech systems. Until products which can process the tremendous amounts of information needed for speech recognition become readily available, various combinations of architectures and processors must be utilized.

Some manufacturers of recognition systems believe that adding hardware to or including specialized chips in a recognizer are neither feasible nor adequate solutions to the problem. Adding computing power will not help an inefficient speech algorithm become more efficient, but rather speed up its inefficiency. Many manufacturers are concentrating on developing algorithms which reduce the number of searches necessary for decision networks. Dragon Systems Inc. is one company which, through algorithmic improvements in stochastic modeling, has been able to cut the computation time needed during speech recognition.

Three basic approaches exist for speech recognition, each suited to particular combinations of speaker-dependent or speaker-independent and isolated or connected speech. Template matching, phonetic-based analysis and hidden Markov modeling all use some form of pattern matching between the spoken input data and information stored within the system. The differences between the three methods are mainly due to which features are extracted from the input and how the algorithms compare and match those identifying parameters contained in the digitized patterns or templates.

Template Recognizers

Figure 3 illustrates a typical template-based recognizer, the most prevalent type of speech recognizer. A template recognizer requires that whole words be stored separately on each template. The user sets the sensitivity for the recognizer to negate any problems resulting from variations in speaker loudness. The analog signal is digitized into a spectral representation. Parameters are taken from the digitized speech sample at designated intervals by operations such as filtering, Fourier transforms or linear predictive coding (LPC). An algorithm, usually proprietary, normalizes and compresses the extracted parameters for pattern matching by determining the beginning and the end of each isolated word.

Among the features that can be examined for pattern matching are the word's formants and fundamental frequencies. A matrix of features in numerical form results. This data is then compared with each of the templates stored within the recognizer. Word recognition results when an appropriate match is found

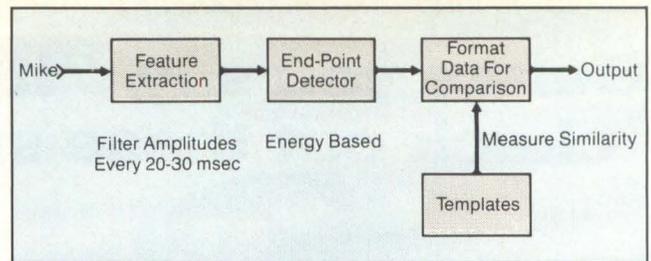


Figure 3: A block diagram from Voice Control Systems of a template-based speech recognizer. Most recognition systems use this technology.

between the input data and a template.

The matrix is the most elementary approach to classifying words or utterances; it is two-dimensional with time on one axis and frequency energy on the other. Computing the distance between corresponding matrix elements in unknown matrixes (the input speech) and the reference matrixes (the stored speech) for all elements determines a match.

Dynamic programming, an alternative to matrix comparison, is essentially an algorithm which chooses the minimum path between a series of points from among several potential paths. Using dynamic programming in a speech recognition system can increase computation burdens dramatically. However, the development of more efficient path searching algorithms have been able to reduce this load down to the scale of matrix comparison.

Certainly, the most obvious benefit from using dynamic programming techniques in speech recognizers is their ability to adjust to the variations inherent in speech. A speaker cannot reliably reproduce segment durations or pronounce all the syllables in words all of the time. As a result, the recognizer may be presented with a valid input which it cannot classify. Dynamic programming determines how to time-align the segments of the unknown speech with the reference speech.

Another normalization procedure is frequency-axis normalization. Whereas dynamic programming concentrates on the time-axis and therefore consonant matching, frequency normalization is more important for vowel recognition—a key concern of designers of speaker-independent recognizers.

Speaker-dependent systems generally store one template per desired word of vocabulary. As a result, response time is to some degree proportional to the number of templates which must be compared to the input data. The response rate is also dependent upon the computing power available to calculate the similarities between the input parameters and each of the templates.

Most of the speech recognizers available today are speaker-dependent, isolated-word template-based recognizers. Interstate Voice Products, which has probably sold more recognizers than any other vendor, recently announced the SRB board for the IBM PC, which is an isolated-word product handling up to 240 utterances. NEC manufactures a connected-word system, the DP-200, as well as some board-level recognizers which are isolated-word. Scott Instruments (Denton, TX) manufactures a connected-speech input terminal called the VET-232SD which provides the option of speaker-independence. Other companies with connected-word, speaker-dependent recognizers include Verbex, Votan and Texas Instruments.

In a speaker-independent system, template matching can be a very inefficient recognition method because such systems store up to 10 or 15 templates per word in the vocabulary. Therefore, if a speaker-independent recognizer had a 15 word vocabu-

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lary and 15 templates for each word, 225 comparisons would have to be made using a template-based algorithm for a recognition hypothesis. Some template matching, speaker-independent speech recognition systems do exist on the market today. Most are digit recognizers from such companies as Votan, NEC and Verbex and are, in general, relatively expensive.

Phonetic Recognizers

Phonetic-based recognition systems analyze the individual phonetic units of any utterance rather than the word as a whole. **Figure 4** is a block diagram of the speaker-independent phonetic recognition system developed by Voice Control Systems (Dallas, TX). A microphone transduces the speech input; it is then digitized by an A/D converter; and an analysis of background noise adjusts the input gain of the A/D converter. Every 10 msec, 20 time domain parameters are computed, some of which are then used for frequency domain analysis.

The triggering algorithm separates voiced sounds from unvoiced sounds to determine if a speech utterance exists. After capturing the utterance, the voicing boundaries of a word can be determined; other phonetic transitions are also determined. Once those boundaries and transitions are located, the individual phonetic elements are analyzed and identified. A recognition hypothesis occurs after this process.

For example, consider the word "listen." Four voicing boundaries exist in the word: at the beginning of the "l," at the end of the "i," at the beginning of the "e" and at the end of the "n." Two phonetic transitions would be located by the analyzer, between the "l" and the "i" and between the "e" and the "n."

The primary disadvantage of general phonetic-based recognition is that the segmentation problem has not been completely solved. This makes it difficult to create a fully adequate model for speech, and if a speaker does not pronounce a certain phoneme as it is stored, a match may not occur simply because the utterance does not fit into the developed model.

Unlike template-based speaker-independent systems, only one set of reference data is needed to characterize each phonetic unit. Another advantage of a phonetic-based system is that it is more similar to how a human recognizes speech—by phonetic sounds and not word by word. As a result, such a system may be more extenuous to a continuous speech system than a template-based recognizer. A finite number of phonemes exist in human speech, so in theory, every one of those phonemes can be programmed into a recognizer; the thought of trying to train a template-based recognition system for every word in the dictionary is ridiculous.

The company most associated with phonetic-based recognition is Voice Control Systems. The company has developed a customized 27-word, isolated, speaker-independent system for General Motors and plans to introduce a connected-speech, speaker-independent digit recognizer early next year. Kurzweil is the other company with definite plans to enter into the phonetic-based systems arena with an isolated 1,000-word speaker-dependent (or 101-word speaker-independent) system, the KVS-3000.

Hidden Markov Modeling

Hidden Markov modeling, a subset of more general stochastic modeling, is a statistic-based method of recognition. It represents the variations possible in sequences of words and sounds

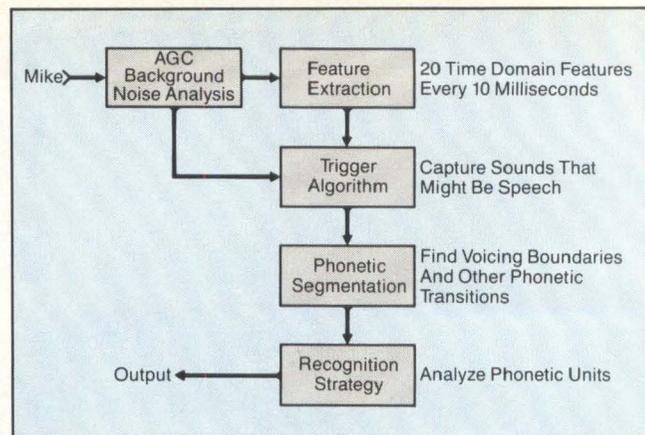


Figure 4: An illustration of a phonetic-based speech recognizer developed by Voice Control Systems.

and bases its decisions on the sound combinations. In some ways, Markov modeling resembles dynamic programming; it works with a state model for feature extraction. However, it differs from dynamic programming because it does not actively select the best path for assembling a word. Instead, it considers all paths and computes the probability of a match from all possible paths. Therefore, separate segments are not examined but rather the probabilities. The path with the highest probability is assumed to be the next element in the input speech.

Well-defined word combinations require less computation; however, more complex ones may necessitate up to 10 times the number of calculations—and at hidden levels transparent to the designer. IBM's experimental dictation machine is an example of a hidden Markov-based recognizer. Input utterances enter a VLSI signal processor performing vector quantizations which analyze the speech signal. This process segments the speech into pieces that are parameterized and quantized into a set of Markov codes. About 200 codes are used in the machine to reconstruct the word by probability.

Other companies currently investigating the possibilities of Markov modeling in speech recognizers are Dragon Systems and AT&T Bell Laboratories (Murray Hill, NJ). However, as yet, the recognition scheme generally is an experimental one. One reason for this may be that the matching algorithms required for Markov modeling are much more complex than those needed for either phonetic-based or template-matching recognizers. As a result, the hardware needed to implement those algorithms is more difficult to build. Only two products using statistical recognition techniques exist on the market; the Apricot Portable from Apricot Inc. (Fremont, CA) includes the recognition chip from Dragon Systems which is based on stochastic modeling. Verbex's algorithm for its 4000 system also utilizes hidden Markov technique.

Markov recognizers may also take a longer time to train because so many lexicons need be stored to define the general speech model. If a speaker does not fit the model, the system will certainly exhibit lower performance accuracies. Nevertheless, a Markov modeling recognition system is well-suited to large vocabularies. The statistical modeling may enable the system to distinguish between words that sound alike by considering their context.

The Natural Man-To-Machine Interface

Speaking commands to a computer is the ultimate in natural human-to-machine interface. As a result, users of speech

recognition systems place more stringent performance demands upon designers. Industry experts indicate that for complete user acceptance of a recognizer, the accuracy exhibited by the system must be approximately 99+ %.

Unfortunately, performance is a very difficult term to define. It is also difficult to determine. Some consider it to be the system throughput or the percentage of time a recognizer simply responds to speech input. These definitions do not take into consideration errors such as substitution, when the machine incorrectly classifies a valid utterance, or rejection, when the user is forced to repeat valid input. If the recognizer reacts with any word or reprompt, it is considered to have performed. Clearly, this definition is inaccurate and is unfair to present and potential users of speech recognition systems.

Performance accuracy depends upon many factors: vocabulary, speakers and environment. Standard vocabularies for evaluating performance, such as the TI vocabulary and the National Bureau of Standards vocabulary, have evolved to help rectify that problem. However, some systems are tested in environments which are not representative of the places many recognizers are installed. Designers of systems may find that the performance they get from a recognizer is higher than that achieved by inexperienced users, because the designers have become accustomed to the quirks in algorithms and adjust their vocal input accordingly.

In general, the market for the voice recognition industry is

developing more slowly than predicted from market surveys. Consumers may have become trapped in an unsatisfactory trade-off between high cost and high performance. The solution is the development of a low-cost, high-performance recognizer, and a trend towards such a system, driven by hardware and speech technology advances, exists. Many industry experts indicate that the general-purpose speech recognition system is no longer a viable product in such a potentially competitive field; approximately 25 companies are involved, to various extents, in speech recognition. Only application-specific products will be successful, even with dropping prices.

Humans receive a lifetime of training in grammar, logic and syntax—all of which provide vital contextual clues to understanding speech. A speech recognition system may only receive one hour of training before it is expected to comprehend spoken input. Continuous recognizers have the additional burden of needing to understand grammar, semantics and syntax. For these reasons, most recognition researchers believe that a continuous, large vocabulary, speaker-independent speech recognition system must rely heavily upon expert system and artificial intelligence technologies. And that, of course, is as human a computer can get. **DD**

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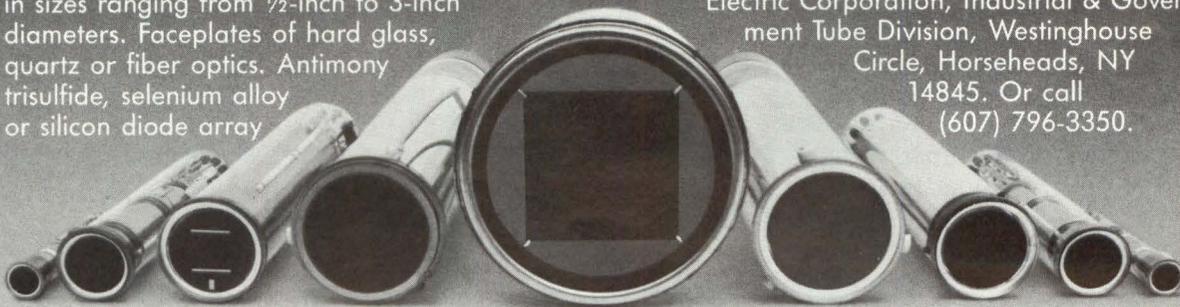
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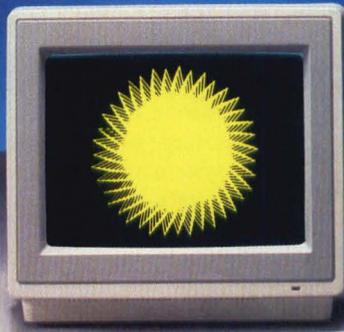
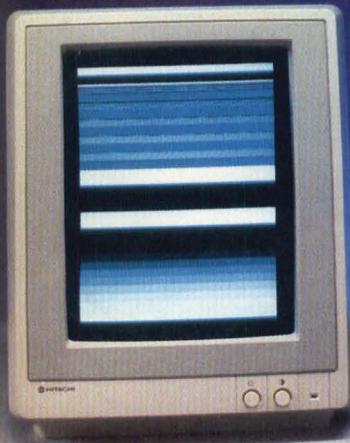


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Serial A/D Eases Speech Synthesis System Design

by Paul Brokaw, Analog Devices Inc.

Of the various methods used for digital speech synthesis, pulse code modulation (PCM) is probably the most flexible. Since it can reproduce essentially any waveform within a band-limited spectrum, PCM can synthesize not only speech, but also music, sound effects and any other signal. Adaptive Differential PCM (ADPCM) is a way of further encoding a sequence of PCM codes to reduce the total bit rate, the bandwidth requirements of a transmission channel and the necessary capacity of storage medium. The code, stored in either disk, read-only memory (ROM), random-access memory (RAM) or another type of memory can be used to reproduce speech, music and specific sounds on demand.

The Oki Semiconductor (Santa Clara, CA) MSM5218 combines analysis and synthesis modes on one chip. It can be used either to compress PCM code into ADPCM format for storage or to restore such code to linear PCM form. The chip includes a 10-bit D/A converter to reproduce the originally coded waveform and can be operated in both modes simultaneously as a demonstration and monitor of encoding quality.

In order to complete the analysis process, the MSM5218 requires the addition of a linear PCM encoder. The analyzer encodes a serial input data stream from an A/D converter; a sample and hold circuit and an antialiasing filter complete the linear encoder. The Analog Devices' (Wilmington, MA) 10-bit AD575 provides good speech quality with a data stream of the same resolution as the MSM5218 synthesizer D/A converter.

The serial output of the AD575 makes the device much simpler to interface than standard parallel output A/Ds, which require parallel to serial converters to provide the serial data stream used by the analyzer chip. Because of such special features as an internal clock, a continuous conversion mode and a short cycle and terminate (SCAT) line, the AD575, unlike most serial converters, needs only a quad gate and dual D-flop package to interface to the MSM5218. **Figure 1** shows all the circuitry required to analyze and to synthesize the speech waveform as well as a digital interface which can be used to control the encoded data.

The MSM5218 is powered from +5V and generates its own clock using a 384 kHz ceramic resonator. It can also be driven with an external clock if preferred. The analyzer calls for A/D conversions at an 8 kHz rate (as shown) with the $\overline{ST\ CONV}$ signal, which is the signal that sets the D-flop driving the CONV input to the AD575. The $\overline{ST\ CONV}$ signal initiates an A/D conversion by unblocking the data path from $\overline{D\ O}$ of the converter to DA IN of the analyzer. By remaining high, the signal puts the AD575 into continuous conversion mode. The data bits are clocked into the analyzer by the CO clock signal as the conversion progresses. When $\overline{E\ O\ C}$ goes low, signaling the end of the 10-bit conversion, a new conversion begins immediately after the last data bit is clocked into the analyzer.

Paul Brokaw is a division fellow at Analog Devices' Semiconductor Division in Wilmington, MA.

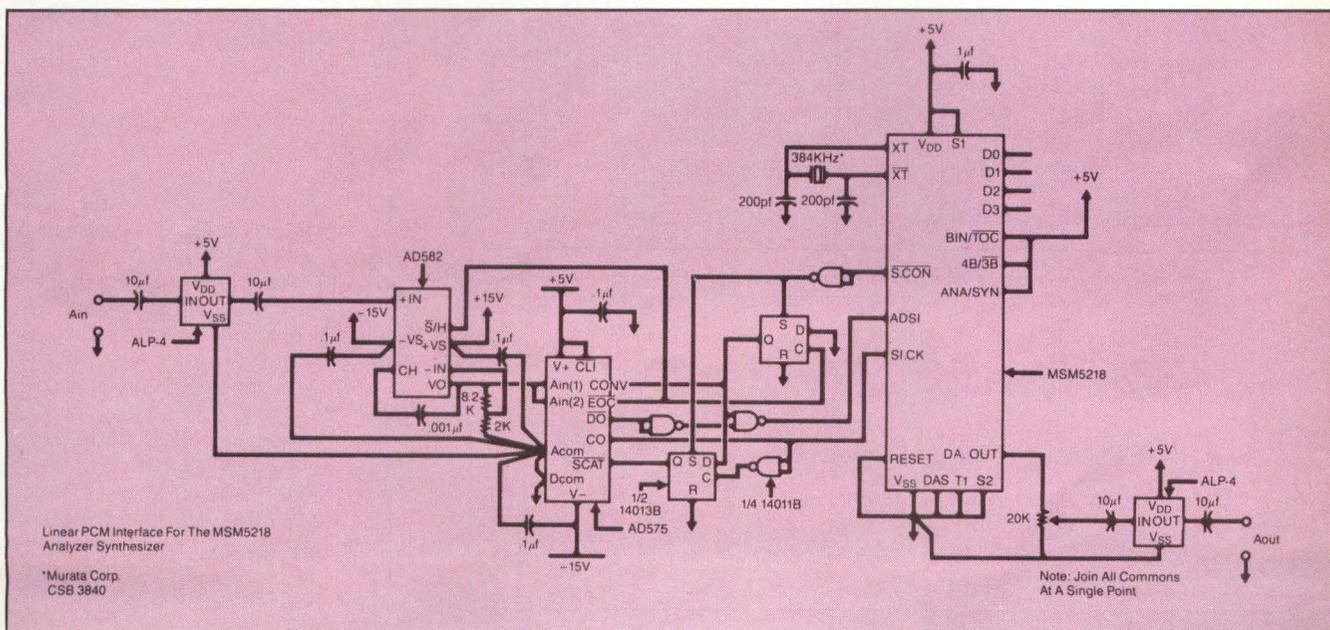


Figure 1: A Linear PCM interface for the MSM5218 analyzer/synthesizer using the AD575.

The start of this conversion resets the upper D-flop to block the data path so that a third conversion will not be initiated. After two more clock pulses have been generated, the lower D-flop drives the \overline{SCAT} line, terminating the conversion. The two extra clock pulses, which effect the second short conversion, shift the 10 valid data bits to the most significant slots of the analyzer's 12-bit input register. The last two bits of the register are filled with complemented zeros by the blocked data path.

This data is compressed and is available for storage at the microprocessor interface. Upon subsequent reconstruction, the data drives the synthesizer portion of the MSM5218. The internal 10-bit D/A converter reconstructs an audio output signal after the signal is smoothed by the ALP/4 active filter.

The audio input must be conditioned before it is encoded by the AD575. An ALP/4 low-pass filter is used as an antialiasing device to prevent high frequency signals from masquerading as extraneous low frequencies in the reconstructed signal. This effect is similar to what happens during optical sampling when a strobe light makes a rapidly spinning wheel appear to be spinning slowly. The filter accepts signals up to 1V peak-to-peak, filters them with a gain of two and drives the Analog Devices AD582 sample and hold. The sample and hold incorporates a gain of five to fill the 10V peak-to-peak bipolar range of the AD575. The EOC signal from the A/D converter controls the input of the sample and hold so that it tracks the input signal between conversions and holds a sample fixed during a conversion.

The MSM5218 can be used with PCM data up to 12 bits per word; however, in this configuration, the speech quality ob-

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tained with the 10-bit converter is practically indistinguishable from a similar arrangement with a 12-bit converter. Higher quality filters with improved frequency response and lower distortion improve performance. In addition, the MSM5218 can be operated in an expanded PCM mode which makes 12 bits available for an external serial input D/A converter. Other options include reduced sampling rates of 4 and 6 kHz and a data compression mode resulting in three rather than four data bits corresponding to each PCM input word. Each of these options reduces the amount of data which must be either stored or transmitted for a given speech utterance — the result may be intelligible speech, but of noticeably reduced quality.

This circuit, together with the options on the MSM5218, includes separable analysis and synthesis functions. It can be used to transmit compressed digital speech or to store the ADPCM code for later computer controlled synthesis. **DD**

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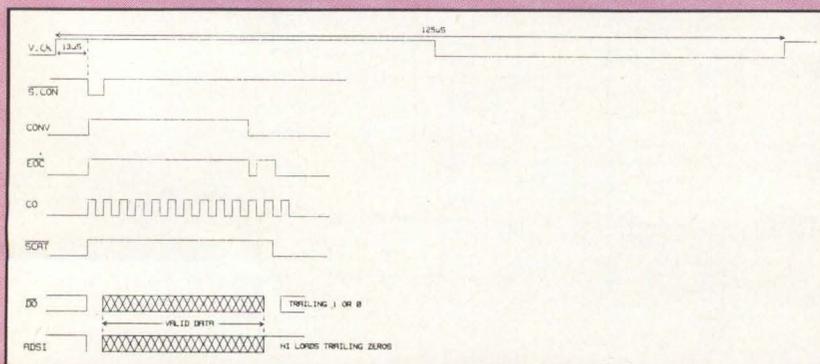
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Timing Interface For Synthesis

General timing diagrams are available for both the AD575 from Analog Devices and MSM5218 from Oki Semiconductor. This diagram illustrates important timing relationships between the circuits as well as signals generated by the two glue chips.

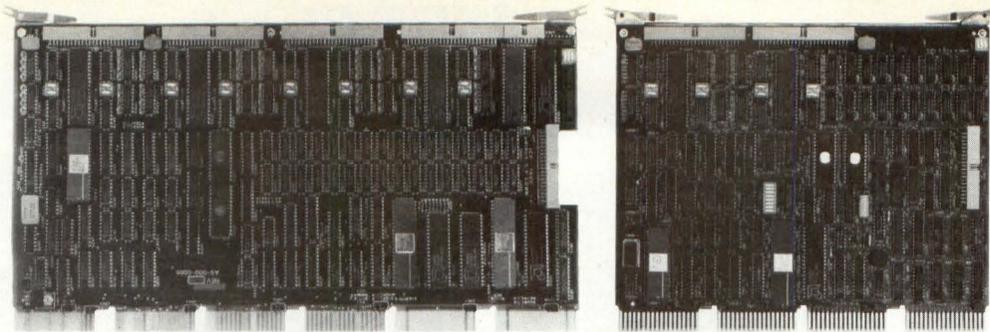
The Oki MSM5218 chip produces S.CON 13 μ s after V.CK to initiate conversion, which should finish during the positive half of the V.CK. A CONV signal, generated by one of the flip-flops in response to the inverted S.CON also sets the other flip-flop re-

storing \overline{SCAT} . The CONV into the AD575 clears \overline{EOC} and causes the \overline{DO} to output 10 complemented binary signal bits (MSB first) representing the analog signal. The signal will be stable during conversion, since \overline{EOC} high causes the Analog Devices AD582 SHA to go into the hold mode. An eleventh data bit during the first CO pulse is invalid, but this bit will be pushed through the MSM5218 input buffer and discarded. This function is performed by the two CO pulses following the 10-bit conversion.



At the end of the conversion, \overline{EOC} will go low; since CONV remains high, a second conversion will commence immediately and \overline{EOC} will be set by the falling edge of the eleventh CO pulse. This edge will clock the flip-flop clearing CONV, disabling the data path from \overline{DO} to ADSI, the serial input of the Oki Chip. The second conversion continues to produce additional clock pulses which shift the 10 data pulses to the MSB positions in the MSM5218 input register. The trailing edge of the first "extra" CO pulse (the twelfth) clocks the lower flip-flop switching the \overline{SCAT} line low, which causes the conversion to terminate after the next clock pulse, producing 13 total CO pulses.

The thirteen clock pulses shift the data consisting of a leading invalid bit, ten good data bits and two trailing zeros (signaled by a high level at ADSI) so that the valid MSB is in the MSB slot of the analyzer input register. At the end of the sequence the AD575 is ready for the next conversion, and \overline{EOC} is low so that the AD582 can acquire the signal. The data is processed by the MSM5218 during the remainder of V.CK; a new conversion starts with the next S.CON pulse.



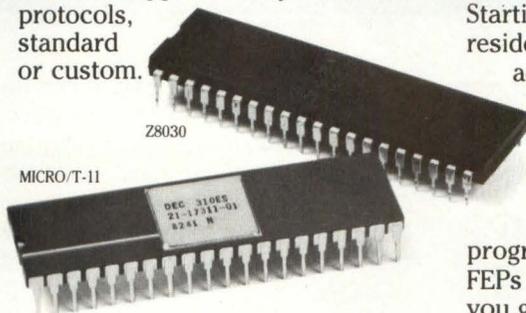
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CMOS Changes System Design Considerations

by Ronald Collett, Sr. Technical Editor

PHOTO DESIGNED AND PRODUCED BY GREGORY MACNICOL

CMOS will replace NMOS as the dominant technology used in system design. Incorporating one million components on an IC is within the range of many semiconductor manufacturers. This sophistication means that the number of NMOS transistors on a dense chip may exceed the packages' power dissipation capability. Thus, increasing VLSI chip density motivates IC makers to convert existing NMOS devices to CMOS. Moreover, CMOS devices with 1-micron geometries are approaching operating speeds on par with their TTL counterparts.

Aside from the advantage of decreased power consumption, CMOS offers excellent noise immunity, low input currents, wide operating supply voltage and operation over a broad temperature range. However, there are disadvantages including latch-up, numerous on-chip interconnections and lack of current drive capability.

Designers using a bipolar technology like TTL are accustomed to trading speed for power. In many instances, engineers prefer using TTL to CMOS when given the choice. Even when the design is to operate at low speeds, CMOS device failures caused by electrostatic discharge (ESD) have led designers to opt for low-speed bipolar logic. Until recently, CMOS com-

CMOS now offers low power without compromising performance.

ponents could withstand only a few hundred volts of ESD. This has been a particularly troublesome problem during the system manufacturing stage where the chips undergo continuous handling. Now, many manufacturers' devices are well above the accepted industry standard of 2000V.

Much research effort has been expended on improving the various problems with CMOS. Most major semiconductor manufacturers including Intel (Santa Clara, CA), Signetics (Sunnyvale, CA), Texas Instruments (Dallas, TX) and Advanced Micro Devices (Sunnyvale, CA) are banking on CMOS becoming the preferred technology. In hopes of capturing a share of the market, other smaller companies such as Zytex (Sunnyvale, CA) and Integrated Devices Technology (Sunnyvale, CA) recently introduced CMOS parts offering bipolar operating speeds and drive capability.

While CMOS has made tremendous inroads in the past few years, TTL and ECL logic families are not likely to disappear. Research effort is continuing in bipolar technology as well as CMOS. Since advances are being made in both, exceptionally high speed devices will remain bipolar. Most systems using CMOS are designed with a combination of CMOS and bipolar components. As a result, CMOS manufacturers are making

their chips TTL compatible. When interfacing the two types of components, design considerations include decreased noise immunity and increased power dissipation. Because the majority of applications do not require ECL-type speeds, engineers are currently making the transition from TTL to CMOS. At the same time, however, CMOS is not a panacea. High performance CMOS lends itself more readily to a particular class of designs.

CMOS, NMOS And TTL

When TTL and CMOS are compared, speed is the characteristic that receives the most attention. CMOS has traditionally been the slower of the two technologies, but new families of CMOS logic from Zytex and Integrated Devices Technology are changing this. Zytex claims its metal gate 54/74 AHCT logic offers the speed of TTL with the advantages of CMOS. The logic family has also been subjected to 1 MRad of total dose radiation, and tests reveal that it remains operational. **Figures 1 and 2** compare the Zytex offering with competing logic families.

Speed comparisons between the two technologies can often be deceiving. For example, Advanced Micro Devices' Am29C517 CMOS multiplier exhibits a clocked multiplication time of 65 nsec over the commercial temperature range; its bipolar equivalent, the Am29517A 16x16 multiplier, performs the same task in 38 nsec. From these two figures, it appears that the bipolar chip is 70% faster; however, the differences between the internal architectures of the two chips must be taken into consideration. The bipolar device does not rely on a recoding

algorithm and forms the product by summing 16 partial products. In contrast, the CMOS multiplier uses two-bit Booth recoding combined with fast adder techniques to improve speed. According to AMD, a bipolar device designed with two-bit Booth recoding and fast adders would be much faster than the 29517A.

CMOS performance improvements cannot be denied. But these improvements are leading to transmission line effects that are becoming increasingly noticeable in CMOS. Designers are encountering transmission line effects similar to those found in high-speed TTL-based systems. However, the problem is less severe with CMOS because of its increased voltage noise immunity. In addition, CMOS is sensitive to ESD and protection diodes are included that tend to clamp reflections to either rail.

Low power consumption has been the primary advantage of CMOS technology. The power a device consumes is divided into two terms: AC power and static power. CMOS devices consume static power in the quiescent state and AC power during the transition between logic levels. In general, today's IC packages are designed to dissipate about 1W. If a device exceeds this level, high temperatures causing leakage currents lead to circuit design problems. Moreover, increased temperatures reduce a system's mean time between failure (MTBF) value.

Static power (sometimes called standby power) of CMOS logic is usually negligible. By comparison, quiescent power dissipation in NMOS and bipolar devices contributes heavily to the chip's total power dissipation. For systems undergoing little switching, CMOS is the favored technology. Yet, in the rapidly growing field of digital signal processing (DSP), low static power is rarely a consideration. Chips in these systems

		TTL			ICEMOS		OTHER CMOS	
		74LS244	74ALS244A	74F244	74HCTLS244	74AHCT244	74HC244	74HCT244
Operating Voltage Range (Commercial)		4.75V to 5.25V	4.5V to 5.5V	4.75V to 5.25V	4.5V to 5.5V	4.5V to 5.5V	2V to 6V	4.5V to 5.5V
Operating Temperature Range (Commercial)		0°C to 70°C	0°C to 70°C	0°C to 70°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
Maximum Propagation Delay ($C_L = 50$ pF)		18 ns ($V_{CC} = 5V$, $T_A = 25^\circ C$)	10 ns (Over Operating Conditions)	8 ns (Over Operating Conditions)	18 ns ($V_{CC} = 5V$, $T_A = 25^\circ C$)	10 ns (Over Operating Conditions)	20 ns ($V_{CC} = 5V$, $T_A = 25^\circ C$)	18 ns ($V_{CC} = 5V$, $T_A = 25^\circ C$)
Maximum Quiescent Current		54 mA	27 mA	90 mA	0.08 mA	0.08 mA	0.08 mA	0.08 mA
Typical Power Dissipation	Static	120 mW	70 mW	260 mW	0.004 mW	0.004 mW	0.004 mW	0.004 mW
	At 100 kHz (All inputs toggling)	120 mW	70 mW	260 mW	0.6 mW	0.6 mW	1.0 mW	1.8 mW
Output Drive Currents	I_{OH}	-3 mA ($V_{OH} = 2.4V$) -15 mA ($V_{OH} = 2.0V$)	-3 mA ($V_{OH} = 2.4V$) -15 mA ($V_{OH} = 2.0V$)	-15 mA ($V_{OH} = 2.0V$)	-12 mA ($V_{OH} = 3.84V$)	-12 mA ($V_{OH} = 3.84V$)	-6 mA ($V_{OH} = 3.84V$)	-6 mA ($V_{OH} = 3.84V$)
	I_{OL}	12 mA ($V_{OL} = 0.4V$) 24 mA ($V_{OL} = 0.5V$)	12 mA ($V_{OL} = 0.4V$) 24 mA ($V_{OL} = 0.5V$)	64 mA ($V_{OL} = 0.55V$)	12 mA ($V_{OL} = 0.4V$) 24 mA ($V_{OL} = 0.5V$)	12 mA ($V_{OL} = 0.4V$) 24 mA ($V_{OL} = 0.5V$)	6 mA ($V_{OL} = 0.33V$)	6 mA ($V_{OL} = 0.33V$)
Input Threshold Voltages	V_{IL}	0.8V	0.8V	0.8V	0.8V	0.8V	0.9V ($V_{CC} = 4.5V$)	0.8V
	V_{IH}	2.0V	2.0V	2.0V	2.0V	2.0V	3.15V ($V_{CC} = 4.5V$)	2.0V
Input Currents	I_{IL}	-0.2 mA ($V_I = 0.4V$)	-0.1 mA ($V_I = 0.4V$)	-1.6 mA ($V_I = 0.5V$)	-1.0 μA	-1.0 μA	-1.0 μA	-1.0 μA
	I_{IH}	20 μA ($V_I = 2.7V$)	20 μA ($V_I = 2.7V$)	20 μA ($V_I = 2.7V$)	1.0 μA	1.0 μA	1.0 μA	1.0 μA

Figure 1: Zytex's recently announced CMOS families (HCTL and AHCT) are capable of bipolar speeds with power dissipation found in typical CMOS devices. Shown are the key performance characteristics for the 74XXX244 octal buffer.

are usually clocked at the highest rate possible. As a result, AC power dissipation determines the heat dissipated by the unit. Charging and discharging of capacitors within a CMOS device is the primary source of power dissipation. At a certain frequency, known as the crossover point, CMOS will dissipate more power than bipolar. Until recently, the crossover frequency of low power Schottky and high speed CMOS was around 10 MHz. Zytex claims that its CMOS has a crossover frequency of 50 MHz.

Estimating the AC power of a system can often prove to be difficult. The power is dependent on the number of nodes toggling within each clock cycle, and this varies among systems. In most situations, taking a direct power measurement is the only practical method to determine power consumption. Bipolar logic typically consumes up to 10 times the power of CMOS; the ratio depends on the operating frequency and the particular type of bipolar device.

In terms of die size, CMOS and bipolar gates offer comparable functional density. NMOS logic has a density advantage over both bipolar and CMOS logic. Nonetheless, the functional capability per 1W package of a bipolar or NMOS chip is lower than a CMOS IC because more CMOS gates can be put inside a 1W package. Enhanced photo lithography used in IC fabrication is resulting in NMOS transistor densities exceeding packaging capabilities. This problem has become apparent in 32-bit NMOS microprocessors and dense NMOS static RAMs. A comparison of the CMOS die sizes from various manufacturers is shown in **Figure 3**.

As far as speed is concerned, 25 nsec to 35 nsec access times represent present state-of-the-art technology in 64K CMOS static RAMs. ECL 4K static RAMs offer 10 nsec to 15 nsec access times, which is the highest performance currently available.

CMOS is a highly load dependent technology. As fan-out grows, signal rise and fall times become significantly slower

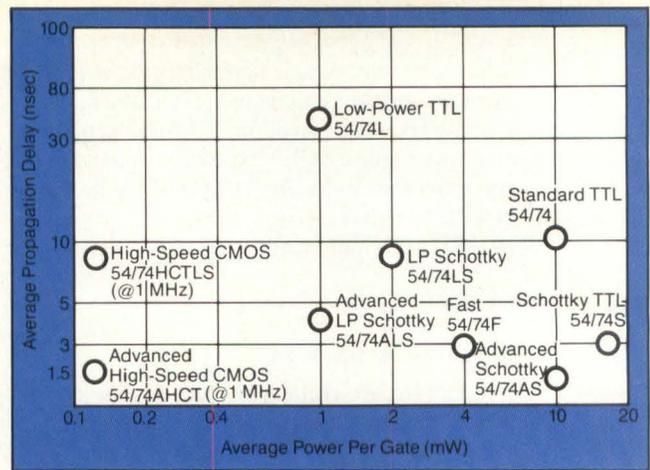
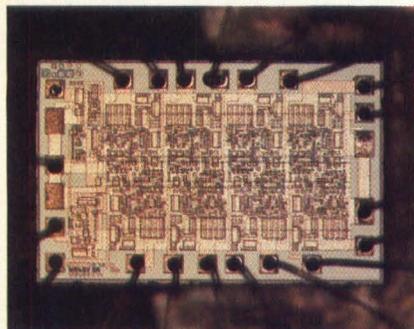


Figure 2: The graph illustrates the power dissipation vs. gate delay characteristics for a two-input NAND gate implemented in various bipolar technologies and Zytex's high speed CMOS.

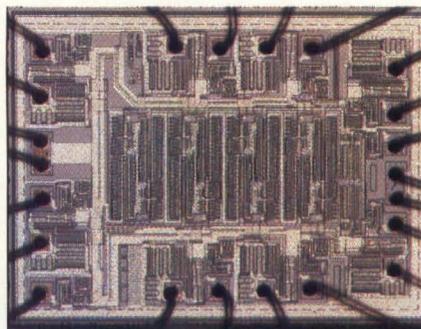
because the gate's output capacitive loading is increased. As the capacitance grows, the RC constant becomes longer. An equivalent effect takes place with interconnections between chips since lengthy signal paths are accompanied by increased resistance and capacitance.

Because CMOS is more sensitive to loading than bipolar devices, architectural and logic design concessions are often necessary to improve speed. An example of this is gate width. CMOS gates become slower as more inputs are added. To alleviate the problem, several two-input gates could replace a single multiple-input gate. Although performance improves, gate count rises — a problem in IC design, where gate count and die size are critical parameters.

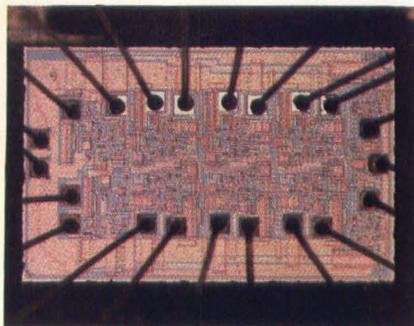
CMOS gates are sized according to their drive needs. Increasing transistor size at the output of a CMOS device is necessary for driving TTL and overcoming long interconnect paths. To raise the output current of buffers in CMOS gate arrays, several buffers are often connected in parallel. This is usually the



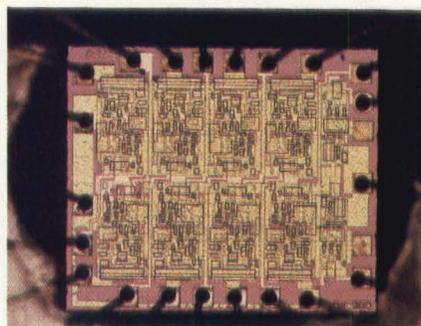
Fairchild 74F240



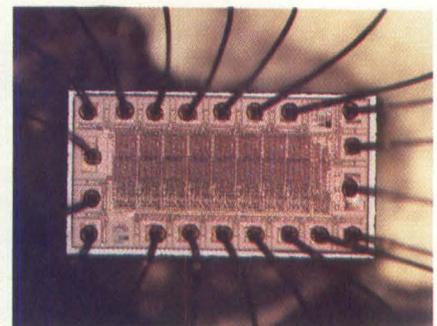
National Semiconductor 74HC240



Texas Instruments 74LS240



Texas Instruments 74ALS240



Zytex 74AHCT240

Figure 3: A comparison of die size of a 74XXX244 among various semiconductor manufacturers demonstrates the scaling achievements made in CMOS. The minimum possible feature size, as dictated by solid state physics, is 0.25 microns.



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solution used to accommodate large fan-outs. CMOS manufacturers stress that, like bipolar logic, many decoupling capacitors should be used to maintain system supply current.

Drive capability of most bipolar devices exceeds that of CMOS, permitting designers to be less concerned with lengthy signal paths having large capacitances. Bipolar drive advantages are apparent at both the chip and the board levels.

In comparing the noise immunity of bipolar and CMOS there are two schools of thought. Most experts agree that CMOS offers greater noise immunity, but debate the degree of superiority. The voltage noise immunity of CMOS is usually $V_{cc}/2$. For bipolar technology, this estimate is usually several hundred millivolts. However, bipolar proponents stress that this comparison is deceiving since energy noise (thermal and shot) is often more damaging than man-made voltage noise (EMI pickup, mechanical vibrations converted to electrical disturbances) and erratic noise (effects of electrical storms, sudden and unexpected voltage changes). When comparing the noise sources, lower levels of energy noise will drive a CMOS gate into a false state because CMOS logic inputs have a higher input impedance than bipolar logic. Also, CMOS logic thresholds are set by the supply voltage and ground, whereas bipolar thresholds depend primarily on ground. Hence, bipolar devices are less susceptible to power supply noise. Designers using CMOS point out that ground noise can be substantially reduced by connecting a capacitor between troublesome signal lines and ground. With this common-mode technique, noise in the ground plane is coupled into the signal line and canceled out.

There is less controversy about CMOS' noise immunity superiority over NMOS'. Unlike NMOS circuits, transistor widths used in CMOS logic are not critical. Ratioless is the term often given to this characteristic. Operating currents do not have to be delicately balanced between the transistor pairs. NMOS transistor widths and lengths are chosen to balance currents between the transistors and ensure that this balance does not deviate with varying operating temperatures.

When interfacing TTL to CMOS, the result is an increase in

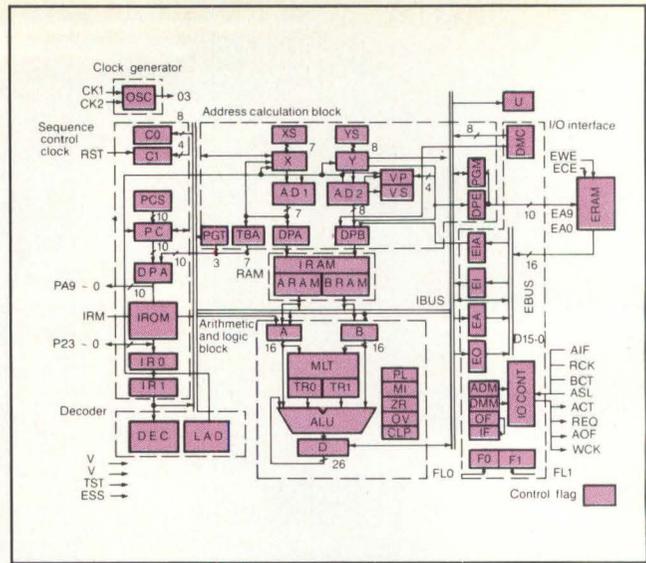


Figure 4: Fujitsu's CMOS MB8764 single-chip digital signal processor uses pipelining to increase speed. In a single 100 nsec instruction cycle, the MB8764 loads both a coefficient and data sample into the array multiplier's inputs, multiplies previously loaded inputs together, accumulates partial products and increments index registers.

power dissipation and a decrease in noise immunity. Higher power dissipation occurs when one of the two transistors in the CMOS device remains slightly on when being driven by a TTL level. In a CMOS to CMOS interface, one transistor of the driven pair is turned either completely on or completely off since the voltage swing extends from V_{cc} to ground. With a TTL to CMOS interface, a TTL voltage swing is approximately 0.1V to 3.6V. Consequently, when a TTL logic high is driving a CMOS gate, the n-channel transistor is on, and the p-channel device is slightly activated.

Architectural Considerations

Integrated circuit architectures can be divided into two categories: local communication and global communication. Local communication chips have internal elements communicating primarily with neighboring functional elements. Because of the short signal paths within the chip, little internal drive current is necessary. CMOS readily lends itself to this category of architectures. Multiplier chips, whose speeds are critical, are an example of this architecture.

Global communication ICs are those whose internal functions communicate with each other over buses or long distances. Processors and controller chips make up the bulk of this category. Because of its limited drive capability, internal CMOS logic is not well suited to this kind of architecture. When the same device is implemented in both CMOS and bipolar, the architecture of the two chips may be slightly different. Semiconductor manufacturers must often modify a bipolar chip's design when fabricating the same function in CMOS.

Converting an existing NMOS part to CMOS also requires some modifications. In particular, the number of interconnections drastically increases. In NMOS, n-type polysilicon and n-type drain or source regions are easily connected with buried contacts, but this is not feasible with CMOS. The nature of NMOS logic permits the two transistors to be connected by diffusion. But in CMOS, the transistors are separated by a well and must be connected by wiring. In addition, there are more transistors to hook-up per function in CMOS than in NMOS circuits. Semicustom chips, for example, demand maximum wir-

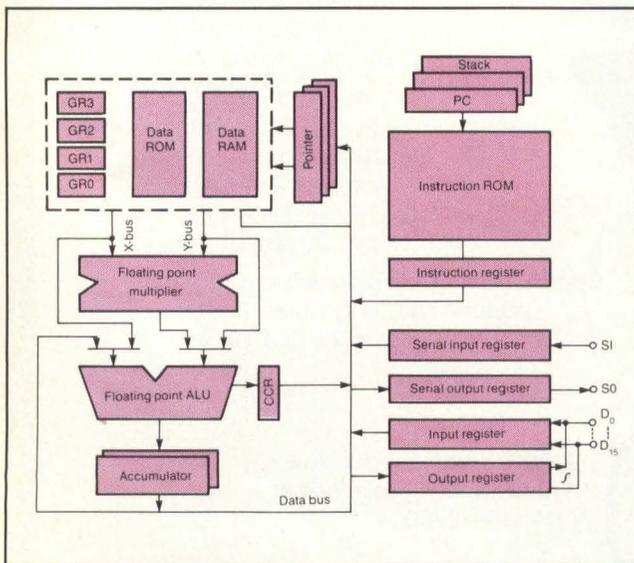


Figure 5: The CMOS HD61810 single-chip digital signal processor from Hitachi is finding use in various voiceband processing applications. The chip's features include an internal Multibus structure and a 200 x 16 two-port RAM.

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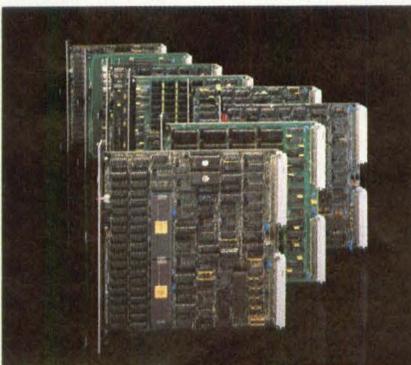
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ing flexibility, resulting in an increase in the number of interconnections.

Pipelining is one technique used to circumvent the global communication problem. VLSI CMOS chips often include pipeline registers placed at various points in data and control paths to improve throughput rates. However, this brings diminishing returns if done excessively. Intermediate calculations needed for the input to the next operation may be stuck within the arithmetic pipeline. This often occurs in pipelines between arithmetic blocks. Problems of this nature can be solved by either waiting for the intermediate data to reach the pipeline's output or overlapping other operations. But both solutions have drawbacks; waiting for the intermediate result to move through the pipeline reduces throughput, and overlapping adds to programming complexity.

Engineers designing digital signal processing systems have two hardware configuration alternatives: a single chip solution or multichip solution. Single-chip digital signal processors are growing in numbers. Fujitsu (Kawasaki, Japan) and Hitachi (Tarrytown, NY) are among the vendors focusing on this niche. Fujitsu developed the MB8764 (Figure 4) which is fabricated in 2.3-micron CMOS and includes an ALU, a multiplier, 256 words of RAM and 1K words of ROM. Using pipelining, this device provides exceptional speed, but at a price of reduced flexibility. In a single 100 nsec machine cycle, the MB8764 loads both a coefficient and a data sample from RAM into the multiplier's input stage, multiplies previously loaded inputs

CMOS presently holds 16% of the semiconductor marketshare.

together, accumulates partial products and increments index registers for the coefficient and the data sample.

With a 250 nsec instruction cycle, Hitachi's HD61810 DSP operates at lower speed than the MB8764, but provides greater flexibility. DSP performance is typically evaluated according to the speed of its repeated multiply/add operation. Voiceband signal processing applications, an area where the HD61810 is finding use, demand at least the repeat rates of the HD61810. Fabricated in 3-micron CMOS, the part (Figure 5) includes a floating point ALU and a floating point multiplier, 200×16 bits of data memory (RAM), 128×16 bits of coefficient memory (ROM) and 512×22 bits of instruction memory (ROM). To reach a 250 nsec processing speed, this device relies on a pipelined architecture, a parallel operation, a high-speed multiplier and a Multibus configuration. According to Hitachi, these elements consume more than 2W when implemented in NMOS.

Single-chip processors continue to grow in sophistication, but most still cannot handle the more demanding DSP applications. Very high-speed image processing systems and graphics workstations frequently require a multichip solution. Likewise, detecting signals buried in noise often requires high-speed cross-correlation. Discrete multibit and single-bit CMOS correlators (models TMC2221 and TMC2220) are available from TRW's LSI Products Division (La Jolla, CA).

NCR Microelectronics (Dayton, OH) is another manufacturer attacking the CMOS discrete component market. Its NCR-

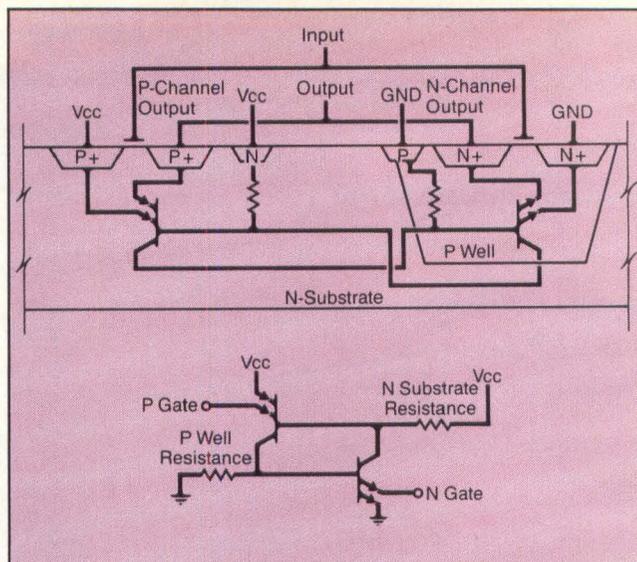


Figure 6: Latch-up has continuously plagued CMOS devices, but recent improvements in fabrication processes will significantly reduce its occurrence. A conventional silicon-controlled rectifier is activated by applying a voltage to the base of the npn transistor, but the parasitic CMOS SCR is turned on by applying a voltage to the emitter of either transistor.

45CM16 directly interfaces to a 16-bit bus without additional logic. The chip performs successive multiply-accumulate operations at a 5 MHz rate and consumes a maximum of 10 mA. NCR claims that when used in a 68000-based system, the chip's multiply-accumulate operations are executed three times faster than the same system using the 68000's internal multiply instruction.

Advanced Micro Devices plans to introduce several new CMOS ICs in the third and fourth quarters of this year. Parts to be available include the 29C101, a 16-bit processor that uses four 2901 bit-slice processors and a 2902 carry look ahead; the 27C1924, a 1 Mbit CMOS EPROM; the 29C510, a CMOS 16×16 multiplier/accumulator; the 29C116A, a 16-bit microcontroller; and two CMOS Integrated Services Digital Network chips, the 79C30 digital subscriber controller and the 79C31 digital exchange controller. The 29300 family will also be fabricated in CMOS.

Most designers using a CMOS multichip DSP solution agree that minimizing signal delay among communication devices is crucial. Ensuring the integrity of printed circuit board layout becomes critical in this situation. Similarly, communication rates among chips must keep pace with the processing speeds of the devices themselves.

Latch-Up

Latch-up is the most significant problem of CMOS. It disrupts the functional capability of the device and, in some instances, causes permanent damage. Latch-up is caused by the formation of parasitic bipolar transistors, products of the CMOS n-channel and p-channel transistors. The resulting configuration of the bipolar elements is a silicon-controlled rectifier (SCR) which acts as a short circuit between V_{cc} and ground. A schematic of the parasitic SCR is shown in Figure 6.

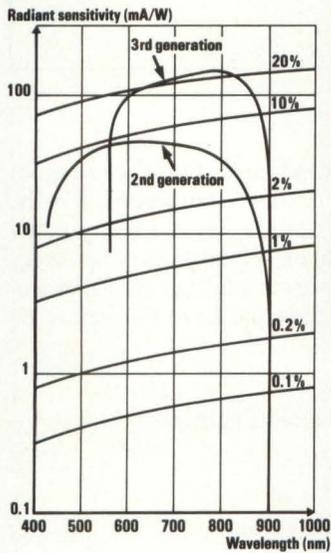
Device susceptibility to latch-up depends on the starting material of the die, the chip layout, the circuit design and the processing procedure. Several conditions trigger latch-up, and once triggered, the parasitic SCR can be disabled only by turning the power off. Operating voltages above V_{cc} or below ground, internal transients or ionizing radiation can each cause

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a current pulse that triggers the condition. The current pulse can be generated either internally or externally. When either of the base-emitter junctions are forward biased, the parasitic vertical npn and lateral pnp transistors may induce a latch-up condition. Once this occurs, the problem can spread to other sections of the chip.

Several techniques are used to combat latch-up. Careful attention is given to layout when designing the chip; manufacturers attempt to split the pnpn SCR into two independent circuits that are incapable of latching up. Separating the n-channel from the p-channel with guard rings is another method commonly used. Other isolation techniques include deep-trench and twin-well isolation.

Adding an epitaxial layer to the substrate is one of the ways to avoid latch-up. The additional layer shunts the emitter-base junctions of the parasitic transistors. In p-well CMOS devices, a thin n-layer is grown on a heavily doped n+ substrate. A lower substrate resistance is formed around the pnp transistor's emitter-base junction. By reducing the substrate resistance, voltage will not reach the levels necessary to activate the lateral pnp transistor. Intel, like several manufacturers, combines several latch-up prevention techniques, including an epitaxial layer, for maximum immunity.

The Future Of Bipolar, CMOS And NMOS

Many CMOS advocates throughout the industry claim that the death of TTL is imminent. Although it can be said that CMOS

is a formidable challenger, the widespread use of TTL makes it difficult to eliminate overnight. Most designers are comfortable with TTL logic, and changing to CMOS will probably occur only if mandated by system design requirements. Moreover, the architectural flexibility of bipolar continues to outpace CMOS in many designs. The large base of TTL-compatible systems may also slow the expected rapid growth of CMOS.

Another consideration is a new 3V CMOS power supply standard to be released by JEDEC that will require some mixed TTL/CMOS systems to include both 5V and 3V supplies. A 5V to 3V voltage converter could perform the same function, but would waste substantial amounts of power.

As for NMOS, there is little doubt that its extinction is near. CMOS has made tremendous strides forward over the past few years and is now ready to replace NMOS. The once crippling latch-up and ESD problems are becoming less of a handicap as manufacturers gain more experience with the technology. Fewer interconnections within the device is the only significant advantage that NMOS has over CMOS. An increased number of interconnections introduce more capacitance throughout the chip, which leads to deteriorating chip performance. In addition, ICs with multiple wiring levels have a greater chance of being flawed.

DD

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LETTERS

Letter To The Editor regarding "Resolution A/Ds Approach Performance Limits"

Dear Ms. Meng:

I looked forward with anticipation to the article titled "High Resolution A/Ds Approach Performance Limits" that appeared in the March 1985 issue of *Digital Design* . . .

...in our opinion, the article contained several inaccuracies regarding A/D converter error sources and definitions of terminology.

...The terms "resolution" and "precision" are often confused. Strictly speaking, resolution has nothing to do with precision; it is easy to build a 20-bit resolution A/D or D/A, but as you so correctly point out in the article, it is very difficult to build a converter accurate to the 20-bit level. Furthermore, precision refers to the ability of the converter to yield the same result from one conversion to the next, given the same input signal (or code) to convert . . .

...During the discussion of integrating A/D converters, several statements are made that must be clarified... While it is true that the accuracy of an integrating A/D is independent of the long-term stability of the clock and integrating capacitor since each affects both the signal integration and reference integration equally, short-term instabilities between the two conversion phases can cause errors. In addition, dielectric absorption in the capacitor ("memory" of the last voltage held prior to

a large signal change at the input and the subsequent conversion) can cause significant errors in the conversion process. Finally, your readers may wish to know that Analogic has been producing an integrating A/D converter for several years that provides true 17-bit accurate conversions at a throughput of 250 per second, significantly higher than the typical 3 to 100 mentioned (our Model MP8037).

Sincerely,
William H. Lundgren, Applications Engineer
Analogic Corp.
Wakefield, MA

Letter To The Editor regarding the Protection of Registered Trademark, File No. P-85-007

Dear Ms. Pingry:

I enjoyed your article entitled, "Keyboards Range From Single Components to Intelligent Input Systems," which appeared in your March 1985 issue of *Digital Design*.

Unfortunately, your article misused our registered trademark which is "Key Tronic," or "key tronic." We are not "Keytronics." The products which you referred to in your article, reed switch keyboards and the new touch pad keyboard with ports for other input devices are products produced by Key Tronic Corporation.

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DIGITAL DESIGN
SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

Effects Of Pipelining On Algorithms For The MC68020

by David Olsen, Lockheed, Sunnyvale, CA

In the past, the performance of an algorithm on a microprocessor was determined by how fast the processor ran and how many instructions the algorithm required. This has been changed by the advent of pipelining found in today's 32-bit microprocessors. Now, the order in which instructions are executed, location of the instruction on an even or odd boundary in memory and the form of the algorithm affect the performance.

The execution of instruction can be broken down into six distinct phases: instruction fetch, instruction decode, effective address calculation, operand fetching, execution and storage of data. In simpler microprocessors, all these stages will be completed before execution of the next instruction is started. The pipelining in the 68020 allows for the starting of these phases on the following instructions before the completion of the current instruction. The 68020 has three units which are responsible for these functions, the pipeline, the bus controller and the sequencer.

The pipeline has three stages; the first stage holds an operand, and the second and third stages hold an operand or an operand extension word (Figure 1). An operand extension word is the second word of a two-word instruction. For example, the instruction "MOV %FFFF, D5" shows the holding of intermediate data. The pipeline is responsible for decoding the instructions and supplying the sequencer with any operand extension words. The bus controller is responsible for all activity on the address and data bus, including instruction fetch, instruction prefetch, operand fetching, data fetching and storage of data. The sequencer is responsible for the effective address calculation,

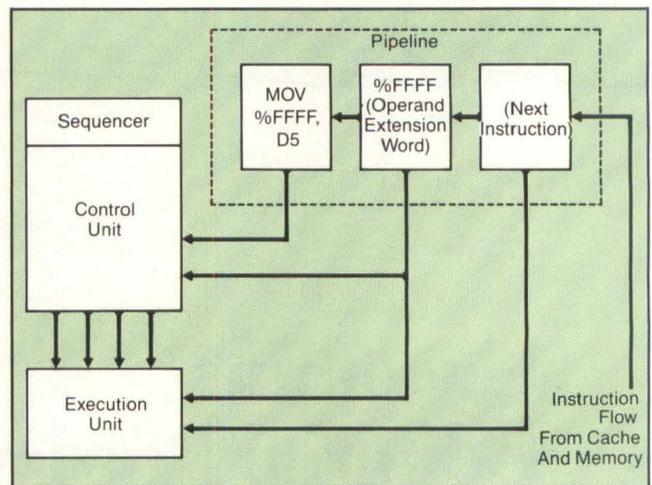


Figure 1: The pipeline of the 68020 has three stages. The first stage holds an operand, and the second and third stages hold an operand or operand extension word.

tion, that is, determining bus address for all the addressing modes and activity involving the ALU.

The 68020 differs from the 68000 in that these three units perform independently. In the 68000, the bus controller can prefetch instructions when not needed to fetch or to store operands. In the 68020, the sequencer has a degree of independence. If the

David Olsen is Associate Engineer Senior at Lockheed Space Systems Division, Sunnyvale, CA.

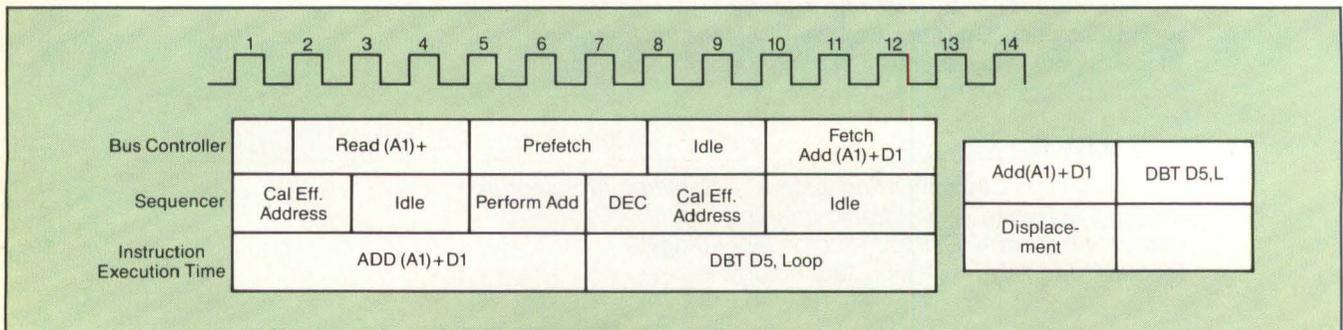


Figure 2: Timing diagram for a simple algorithm to add an array of numbers.

sequencer is finished with its required phase of an instruction, and the bus controller is finishing the last phase of instruction execution as in MOV DI,(A1), the sequencer can then look at the next instruction prefetched into the pipeline and start execution. The overlap of the bus controller finishing the last phase of an instruction and the sequencer starting its execution phase of a new instruction can be great enough that the sequencer would finish an instruction at the same time that the bus controller finishes the previous instruction. Of course, there are locks in the pipeline to prevent instruction dependent sequences

The performance of today's μ Ps is being affected by the increasing use of pipelining.

from occurring out of order.

The effect of pipelining can be illustrated by a simple algorithm for adding up an array of numbers. The most obvious way of implementing this algorithm is as follows (D5 contains the length of the array):

```

LOOP: ADD (A1)+,D1
      DBT D5,LOOP
    
```

Main Loop

The timing for these instructions running on the 68020 is shown in **Figure 2**. The times the sequencer and the bus controller are active are shown. The sequencer is idle during the first ADD instruction, clock cycle 4. This is because the ADD D1,D2 instruction requires the data be fetched from memory, (A), and loaded into register D1 before it can add D1 to D2. Therefore, the sequencer must wait for the bus controller to complete before performing the addition.

The first algorithm requires 12 clock cycles to sum an element in an array. However, to maximize the instruction overlap, this algorithm can be rewritten as follows:

```

LOOP: MOV (A1)+,D1
      ADD D3,D4
      MOV (A2)+,D3
      ADD D1,D2
      DBT D5,LOOP
      ADD D4,D2
    
```

Main Loop

The time associated with this algorithm is shown in **Figure 3**. The array is broken in half, and each half is summed separately. During the first instruction when the sequencer is finished with its task or calculating the effective address and incrementing the address register A1, the sequencer can start executing the next instruction in the pipeline (ADD D1,D2). This is at the end of clock cycle 4. Because the second instruction, ADD D3,D4, does not require the data being fetched by the first MOV instruction, there is no interlock between the sequencer and the bus controller; that is, the sequencer can continue processing instructions in the pipeline. This is called an instruction independent sequence. Compare the first two instructions of each algorithm and notice that for the first algorithm the sequencer must wait for the data being fetched before being able to continue processing instructions in the pipeline. The second algorithm eliminated idle sequencer time. By alternating the additions, the idle sequencer time, which occurs when the ADD (A1)+,D1 instruction is waiting for data to be fetched, is eliminated. The sequencer is never idle.

Performing two additions takes 18 cycles, or 9 cycles per addition of array element. This is a savings of 3 cycles, or 67% of the time required in the first algorithm. However, this requires more memory and initiation and uses two extra registers, which might require being restored if used in a subroutine. However, an array size larger than 10-15 elements is the approximate crossover point for improved performance.

One criterion for using this type of algorithm separation is that the algorithm must be highly repetitive, a loop. Also, the calculations within the repetitive part must be associative; i.e., the order in which they occur does not matter or the elements being operated on are independent of each other. It does not matter what order an array is summed or what order an array is searched for an element.

The performance of today's microprocessors is being affected by the increasing use of pipelining. The firmware programmer must gain familiarity with the effects of pipelining and how it will enable him to increase the performance of the system. For the person involved in the selection of a high level language for the microprocessor where high performance is important, the idea of pipelining must be kept in mind. New compilers will undoubtedly take advantage of the pipelining, and optimizing compilers will become available which have pipeline reorganizers.

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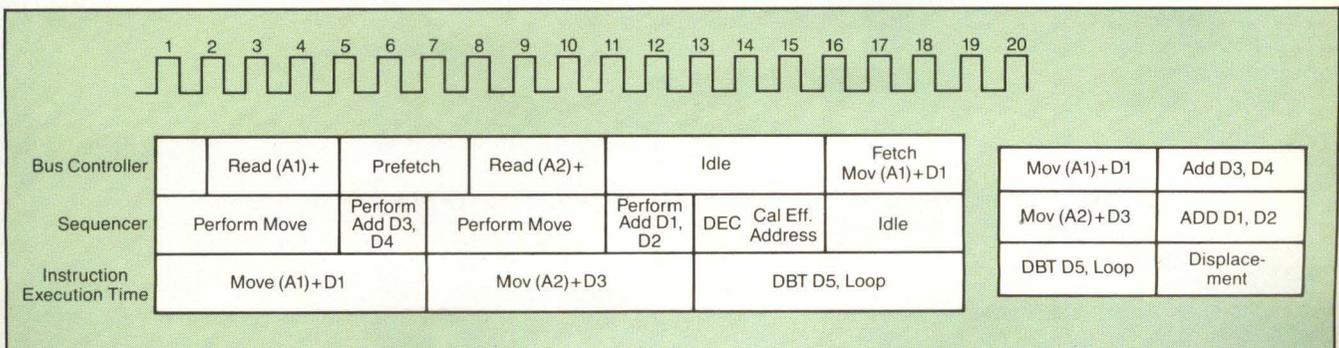
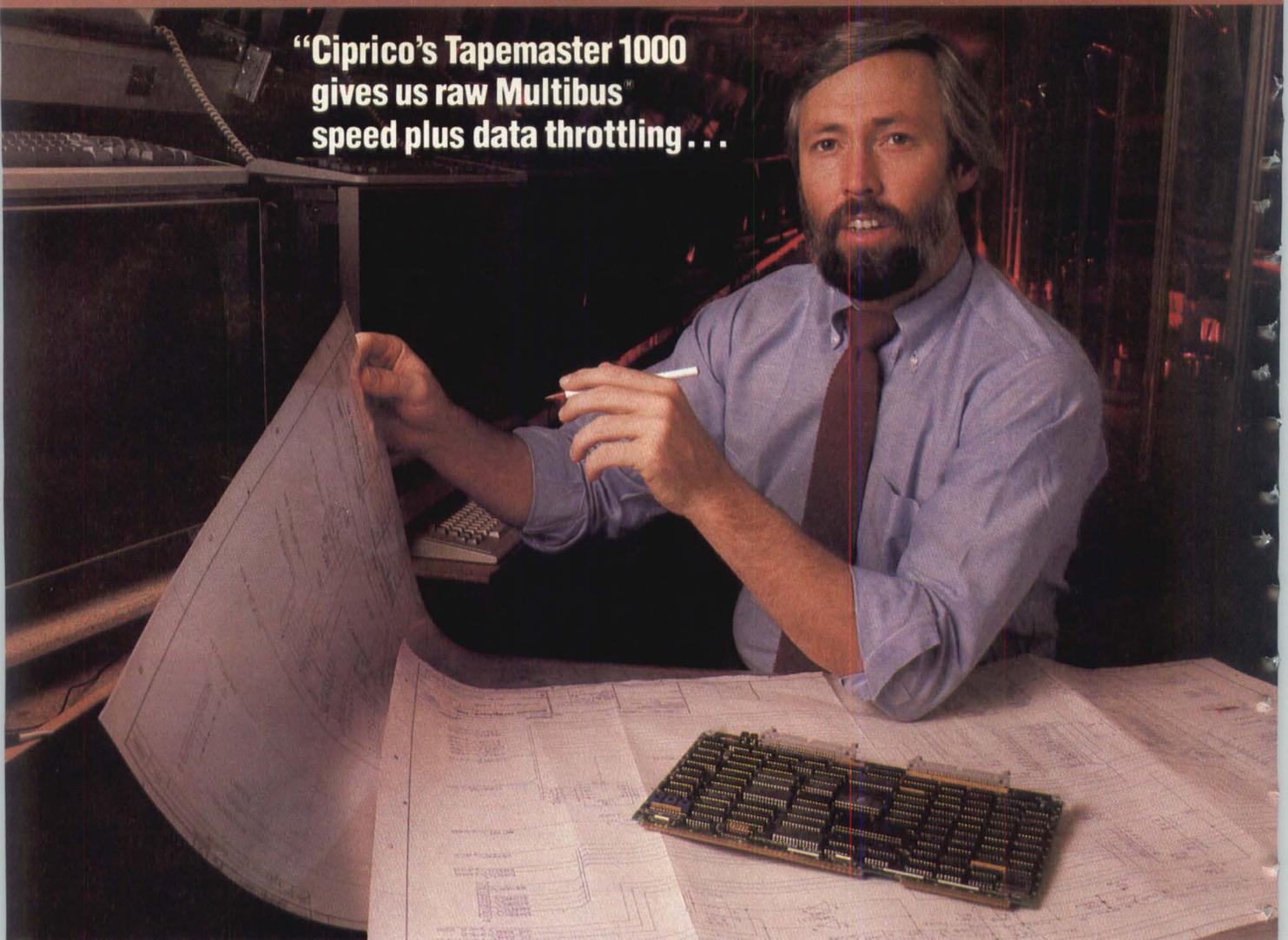


Figure 3: Timing diagram for the rewritten algorithm showing the elimination of idle sequencer time.

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Advanced Microprocessors Demand High-Level Language Support

by Joe Aseo, Western Technical Editor

From engineering workstations to image processing, the applications being considered for the current generation of 16- and 32-bit microprocessors have moved emphasis away from hand-coded assembly language routines to complex programs coded in high-level languages such as C and Pascal. Microprocessor software development has also changed in character from individual programmers working on a monolithic piece of code to teams of programmers working on individual modules for later integration into a larger program. As a result, development system vendors are scrambling to provide the appropriate tools to meet these changing needs. No single vendor has the total solution, yet the pieces are rapidly falling in place—source code symbolic debuggers, sophisticated in-circuit emulators and powerful development hosts.

To aid programmers in their efforts to develop code in high-level languages, microprocessor development system vendors are providing source code symbolic debugging with the ability to single step through not only source code statements but also entire routines. A related approach has the symbolic debugger work at the assembly language level, referencing the source code statements that generate the assembly output.

The ability to perform this task effectively requires that the symbol tables generated by the high-level language compiler be accessible by the linker, loader and symbolic debugger. For example, many compilers for the 8086 family from Intel Development Systems (Hillsboro, OR) generate an output database called the Object Module Format (OMF). This database contains such information as variable names, data types and source code line numbers. This information is preserved during the linking and loading process and allows the object module loaded into absolute addresses to be referenced to the relocat-



Figure 1: Tektronix Microcomputer Development group supports cross-development on the Digital Equipment Corp. VAX-11 series computers with compilers, linkers and loaders. Final hardware and software integration as well as software debugging occurs with the dedicated resources of the 8540 integration unit and associated in-circuit emulators.

ble source code. Other vendors using this approach for compilers include Boston Systems Office (Waltham, MA), Emulogic (Norwood, MA), First Systems (Manhattan Beach, CA), Hewlett-Packard Logic Systems (Colorado Springs, CO), Motorola Microsystems (Tempe, AZ) and Tektronix Microcomputer Development Products (Beaverton, OR).

Beyond the retention of symbolic information, source code symbolic debuggers must also have the ability to insert breakpoints at either the source code or assembly language level. This allows program execution to be halted when necessary, as well as trigger a trace history of bus transactions. Symbolic debuggers can be classified according to the type of breakpoint that they implement—software or hardware.

In general, software debuggers first insert probes, or flags, into a program and then monitor its execution until the flagged statement is reached. This class of debugger does not run at the same speed as actual CPU execution since every program statement, in addition to the flagged statement, must be examined. Likewise, such debuggers can only simulate the actual CPU state, that is, internal registers and status of the stack, since they lack the means to access this information. As a result, software debuggers are largely used to examine the program logic of individual routines. Such software debuggers include BSO/Debug from Boston Systems Office, Softscope from Concurrent Sciences (Moscow, ID), Microscope from First Systems, Pscope from Intel and csd from Mark Williams (Chicago, IL).

To monitor program execution in real time, hardware debuggers access the breakpoint and trace facilities of in-circuit emulators or hardware probes such as M-Probe or PC-Probe from Atron (Saratoga, CA). These facilities allow program execution to occur at full speed until the flagged instruction is reached. At this point, the emulator can continue to operate in a transparent fashion or to intrude into the operation of the system to examine the internal CPU state.

Transparent operation typically involves producing a trace history of instruction execution either before or after the breakpoint is reached. The emulator works in a background mode so that the target system is unaware of its operation. From the disassembly of the data and instruction accesses that occur on the bus, the internal CPU state can be inferred. With this information, software designers can garner execution times for individual routines, in addition to statistics on time spent in execution, number of intermodule references and memory usage. Development system vendors active in this area include Emulogic, Hewlett-Packard, Intel, Microtek (Gardena, CA) and Motorola. Tektronix plans to implement such timing analysis in future products.

If a closer inspection of the CPU status is required, intrusive measures, for example, forcing a hardware interrupt, can be used to dump the internal control registers. If a program is being executed instruction by instruction, the CPU must have wait states

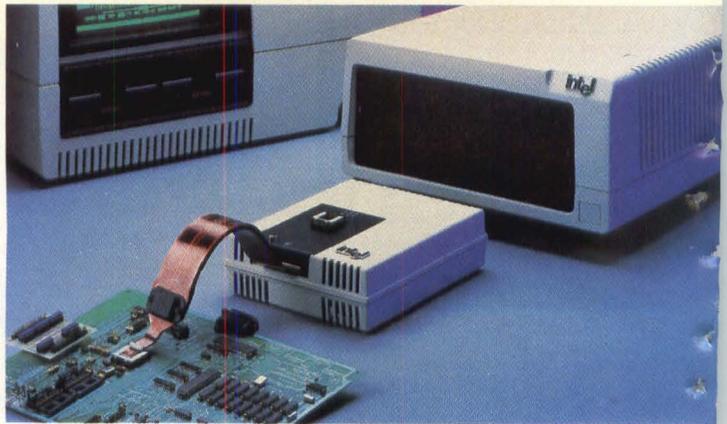


Figure 3: By borrowing the command set from its Pscope software debugger, Intel has provided a common user interface to its Integrated Instrument and In-Circuit Emulator (IICE). The unit provides timing analysis in addition to the emulation and debugging facilities of previous emulator products.

inserted so that the monitor logic can gain access to the changing CPU state. Although this procedure is much faster than the software approach, it still incurs enough overhead to not be considered real time. Still, the performance is such that several software debuggers — Microscope, Pscope, Softscope and Source Probe from Atron — are being integrated with in-circuit emulators.

Source code debugging accounts for only a fraction of the responsibilities expected of current in-circuit emulators. The process of hardware and software integration further demands that emulators become more sophisticated to monitor the activities of such complex CPU features as pipelining, on-chip cache and on-chip memory management. Single-chip microcontrollers like the Intel 8051 put additional burdens on emulators with peripheral functions such as counter/timers, serial communications and DMA control integrated on the same chip.

The most troublesome aspect of monitoring these complex processors is the inability to gain access to control registers and other functions that are seldom seen on the external bus. Many emulators can only access the information that occurs on the physical pins and reconstruct the internal CPU state via disassembly of the data and instruction cycles. However, integrated features like pipelining and instruction cache have no effect on the external bus and are totally transparent. In fact, such features must often be disabled during the debugging process.

To overcome this dilemma, semiconductor vendors such as Intel, Motorola and Zilog have plans to produce special versions of each companies' microprocessor chips that bring out these internal functions via additional bonding pads, as well as integrating the emulation logic directly on the chip (see "The Bond-Out-Based Emulator"). However, the use of bond-out devices has been restricted to each vendor's proprietary emulators. Whether they choose to supply these chips to independent development system vendors, such as Emulogic, Hewlett-Packard, Tektronix and Zax Corp. (Irvine, CA), is still undecided.

This support could be an important factor for hardware and software designers to consider as they evaluate advanced 16- and 32-bit microprocessors for new designs. For example, the iAPX286 emulator from Hewlett-Packard supports only code being transferred from other 8086-based applications and ignores protected mode features such as memory management and task switching. Although Hewlett-Packard and other universal development system vendors have plans to support all iAPX286 functions, these companies may not incorporate the features found in Intel's emulator for as long as a year.



Figure 2: Motorola Microsystems supports full 16-bit development with its VME/10 computer and the HDS-400 hardware development station. Besides hardware debugging, the company is incorporating state analysis.

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To encourage new design-ins, microprocessor vendors with bond-out chips have considered supplying them to independent vendors. However, there is controversy about this approach. Gordon Reid, marketing manager at Intel, notes that bond-out chips may not be the ideal means to support universal emulators since the chips will require the same type of application support as the production versions — support that may not be justified because of their limited volume and increased complexity.

From the perspective of the independent development system vendors, bond-out chips can prove to be more of a curse than a blessing. Roger Crooks, emulator product manager for Tektronix, states that bond-out chips may be of dubious value if they do not exactly match the current versions of the production chip (quite often they lag by one or more mask revision levels) or cannot be easily integrated into the architecture of a vendor's emulator. As a result, both sides are discussing which avenues of cooperation will provide adequate support of these advanced microprocessors without incurring additional headaches.

The very nature of microprocessor development is changing as processors and software increase in complexity. For example, emulators have changed their basic character to embrace functions formerly reserved for dedicated instruments like logic and timing analyzers. As a result, software and hardware designers have an integrated instrument that allows them to work

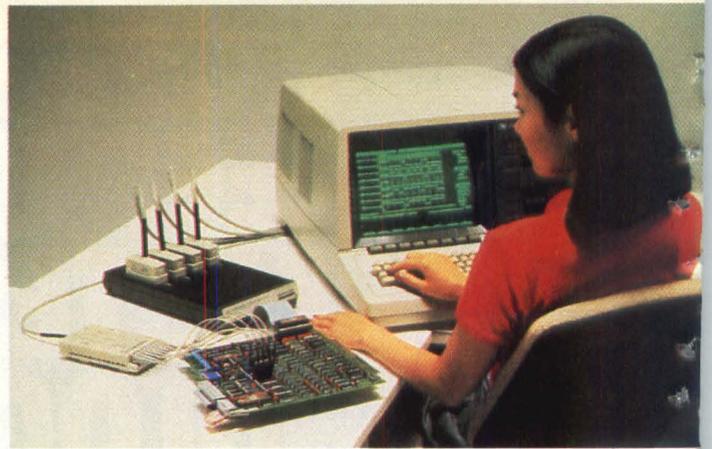


Figure 4: The HP6400 development system from Hewlett-Packard Logic Systems Division incorporates timing and state analysis in addition to the normal edit, compile and debug functions associated with such systems.

equally with source code statements as well as with waveforms.

Bruce McCreary, emulator product manager with Motorola Microsystems, notes that software designers need such analytical tools to allow them to debug and to integrate high-level language programs into the target hardware. No longer is there a one-to-one correlation between the source program and the object code and the conventional method of using logic analyzers and disassemblers falters.

The Bond-Out-Based Emulator

by Garth Eimers, Intel Corp. Development Systems Operation, Hillsboro, OR

The performance and functionality of current generations of microprocessors and microcontrollers has reached a level where only an emulator with a bond-out device can emulate all of the functions of these ICs. Current examples include the 8051 and the 80286. Projecting these trends in the future leads to an increased use of the bond-out to achieve an effective in-circuit emulator.

There are several different types of bond-out devices. The first type is typically associated with microcontrollers. Physically, on the device die, the area conventionally used for the on-chip ROM or EPROM is used to implement the appropriate emulation logic after the ROM is removed. The result is a device which is the same die size as the basic device, provides access to additional processor functions and does not disturb the basic processor layout and risk timing and functional differences between the standard microcontroller and its associated emulation device.

For example, the 8051 basic device package is 40 pins with no address or data lines brought out to its pins. Using the 4K of on-board ROM and a 64-pin package, the emulation device pro-

vides all the pin access of the basic device plus 8 pins of address and 8 pins of data, additional power and ground pins and a pin for the RESET ICE signal. ROM simulation executes the code intended to be in the missing ROM area. The limitation of this style is the absence of the implementation of the trace function on the bond-out device. The trace function is implemented in the ICE hardware externally from the bond-out.

The second distinct type is the true bond-out device. The basic microprocessor design has added functions (i.e., signals) at the die level to support the emulation function. These differences are seen at the packaging level where the emulation features are bonded-out to external pins. The result in this case is that every device carries a small overhead of die area, typically 2% to 4%, associated with the internal conductors and pads supporting the emulation features. Examples of this type of bond-out are the 80186 which brings out an extra pin supporting RESET ICE instruction and the 80286 which brings out both RESET ICE and ICE BREAK instructions associated with task switching. All trace, break and mapping functions are performed off the bond-out.

The third type of bond-out only deserves that name as a convention because it is really an emulation chip. Its design and intent are clearly to support the emulation function with the highest level of integration on the device. The device contains the microprocessor core, support for RESET ICE and ICE BREAK instructions, multiple mode control access, multiple sets of word recognizers, state machine capability and mechanics and access for trace bus. The die size is significantly larger than that of the standard microprocessor. The ICE system has the ability to track the speed enhancements of the microprocessor using the same speed enhancement applied to the emulation device.

The most important advantage of bond-out devices is the increased integration of the emulation system to the target system. This certainly maintains and, in most cases, improves the performance of the emulator. Another advantage is the ability to provide the user with emulation capability for increasingly complex microprocessors at about the same cost. Finally, use of the bond-out or emulation device allows the ICE system to keep up with the speed enhancements of associated microprocessor.

Just as the increasing use of high-level languages has put a strain on today's emulators, it has also taxed the resources of standalone development systems. The complex programs being developed for these processors often demand that superminicomputers or mainframe computers serve as the principal host for source code editing, compilation, linking and loading. The code is then transferred to a standalone development station for debugging as well as final hardware and software integration. These larger hosts also serve as a central archive for source code control to ensure that revisions can be made in an orderly manner.

Another emerging trend is the increasing use of personal computers like the IBM PC as a low-cost alternative to the standalone development system. Here, the trend is to provide each software and hardware engineer with a dedicated workstation, rather than having to share a more costly standalone development system or minicomputer. Still, personal computers could be connected to a larger host such as a Digital Equipment Corp. VAX-11/780 for source code control and master archive via RS-232 serial links or local area networks.

At issue is the proper distribution of processing power needed for the various design functions. For instance, there is wide agreement that the intensive software debugging as well as the final step of hardware and software integration work best in a dedicated environment, i.e., dedicated development systems or personal computers with in-circuit emulators. Dave Baker, president of Real-Time Control Systems, stated, "It's hard to reset a minicomputer when a program goes haywire."

However, there is wide disagreement among development system vendors about the processing requirements associated with program editing, compiling and linking. Advocates of cross-development maintain that only time-shared minicomputers or mainframes can economically serve large programmer teams (above 10 programmers). In fact, Mary Avera of First Systems estimates that a Digital Equipment Corp. VAX-11/750 can support 20 programmers at about \$5,000 per user, whereas a comparable IBM PC-AT configuration is estimated at about \$6,500 per user.

Although not disputing the apparent cost savings accrued from a time-shared system, those who advocate dedicated development workstations note that such minicomputers cannot support large numbers of concurrent users who burden the host CPU with compute-intensive compiles and links. Jerry Kirk, president of Microtec Research (Santa Clara, CA), states that such an environment would effectively limit the numbers that could be served simultaneously to about 10 (using the example discussed previously). As a result, the per-user cost tilts in favor of the personal computer approach.

The ideal development configuration is still far from being decided. Perhaps with the increased use of high-speed local area networks to link minicomputers with personal computers, such distinctions will blur as end users, hardware or software designers focus more on the development tools rather than on which host they reside.

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NEW PRODUCT FOCUS

C O M P O N E N T S

Inexpensive Fiber Optic Components Can Be Autoinserted

The HFBR-0400 family of fiber optic transmitters and receivers from Hewlett-Packard (Palo Alto, CA) are packaged in 8-pin plastic DIPs for autoinsertion and wave soldering onto PC boards. Two transmitters and two receivers handle five common fiber sizes and both analog and digital signals.

The HFBR-1402 standard transmitter is designed for 85, 100 or 200 μm core fibers. A high-performance 1404 transmitter operates with 50 and 62.5 μm core fibers. The HFBR-2402 receiver for digital transmission has 5V TTL/CMOS logic level output. Analog is addressed by the 2404 25 MHz pre-amp receiver.

Transmitters use an 820-nm GaAlAs emitter. All of the components measure 9.5 mm high, excluding pins, \times 12.7 mm wide \times 22.2 mm deep including the threaded connector port.

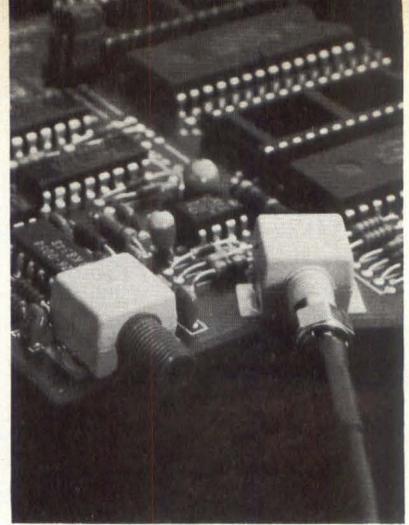
The devices are designed for large-volume production, with a special high-strength flame-retardant molded plastic for the housing. The molded housing also forms and positions leads into the device, eliminating painstaking internal alignments. A double lens system increases light coupling between the fiber and the active emitter or detector. The outer lens protects the device and is made of the same plastic as the housing, assuring a

thermal match.

In addition to increasing coupled power, the dual lens scheme combined with an efficient emitter material allows low current drive. With the resulting lower device heating, reliability increases. Reliability data is to be published in the third quarter, but HP is quoting the emitter at greater than 60,000 hours MTBF.

Quantity 1000 prices: \$18 each for the 1402 standard transmitter, \$23 each for the 1404 high-performance transmitter, \$19 each for the 2402 5 Mbaud TTL receiver and \$12.50 each for the 2404 25 MHz analog receiver.

—Pingry
Circle 230



P E R I P H E R A L S

Color Monitor Has On-Board Intelligence

The VM-8860 monitor from Vermont Microsystems Inc. (VMI) (Winoochi, VT) provides compatibility with many existing programs through its use of the IBM Professional Graphics Controller (PGC) command set. For example, the resident firmware-based graphics command interpreter allows another host, or an IBM PC, to control graphics functions in a CAD system. Advantages include better segmentation of computer functions, versatility of system design and easy upgrading.

The VM-8860 has all of the functional capabilities of the IBM PGC. PGC is important because it represents a firm and immediately functional standard for graphics primitives. The 75 commands support 2D and 3D functions as well as clipping (in 3D space), scaling, perspective and translation.

The 8860 intelligent monitor can display 256 colors from a palette of 4096, with a resolution of 640 \times 480 pixels. An 8 MHz 8088 CPU is used for display list interpretation of the PGC's graphics primitives. VMI has expanded the command set to include such extra features as cross-hair definition, blinking or any color and bit-block transfer. For high-speed data transfer, the command set can be transmitted in compressed hexadecimal or mnemonic ASCII. The enhanced command set allows 256 macros in the current display list. The command set also allows the user to define specific text areas. Of the 320K of display RAM, 300K is viewable and 20K is used for the system program. The standard low-resolution IBM color card functions are not supported. The system works in high-resolution mode only.

The VM-8860 uses a 13" monitor display with an antiglare surface. The scan rate is 60 Hz noninterlaced. BNC output connectors are provided for driving another monitor.

Communication to the monitor is through an RS-232 serial port. The system operates at baud rates up to 38.4K and has a 512 byte buffer; it slows only during display transfers. An optional parallel port is available as well as a serial port for communication with a mouse. A driver for the mouse is resident in ROM.

The intelligent monitor is targeted for use with CAD or business packages based on the PGC command set. A PC or an almost-compatible PC system may act as host and drive an intelligent display using standard commands.

—MacNicol
Circle 234

NEW PRODUCTS

ize a video source within seconds and encode it into (256 × 210 pixels) NAPLPS-standard videotex graphics. Price starts at \$35,000. **Sony**, Park Ridge, NJ **Circle 202**

Compact Modular Video Frame Freezer



A complete digital image storage system, the DR72 Microfreezer is a "functional block" that can replace large frame storage devices. It is switchable to 525 or 625 scan standards, with either single- or dual-frame capability, field or frame selectable. Frame composition is 512 pixels × 480 lines, with 7-bit (128) gray level resolution for NTSC video. With a digital sampling rate of approximately 10 MHz, memory storage capability is 256K words × 7 bits. Measuring 8" × 2" × 5" at 9 lbs., the DR72 is priced from \$3,495-3,995. **Toko America**, Skokie, IL **Circle 200**

High-End Graphics Cluster System



Operating at up to 3.6 MIPS, the GW/10000 SX Graphics Cluster System consists of two display monitors: a Dasher D460 alphanumeric data display and 1280 × 1024 pixel, 60 Hz noninterlaced graphics display. Based on the Eclipse MV/10000 SX supermini, the GW/10000 SX is available with up to 32 Mbytes of memory and can support up to four users. Price is \$283,300 with a 354-Mbyte disk and dual mode tape drive. **Data General**, Westboro, MA **Circle 209**

Integrated Workstation For VLSI IC Design

Four systems for VLSI IC design have been announced by SDA: ChipEdge, a 32-bit UNIX-based turnkey workstation for electronic design of IC and systems and full-custom physical design of ICs; CustomEdge, for full-custom physical design; CellEdge, for front end elec-

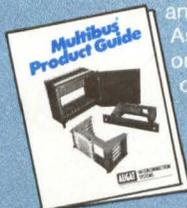
tronic and physical design with the capability of the unified schematic layout editor, unified data base, netlist processor, circuit simulator, logic/fault simulator, mixed-mode timing analyzer, a waveform editor and schematic symbol library; CircuitEdge, a two-user workstation for schematic capture and logic simulation. **SDA**, Santa Clara, CA

Circle 198

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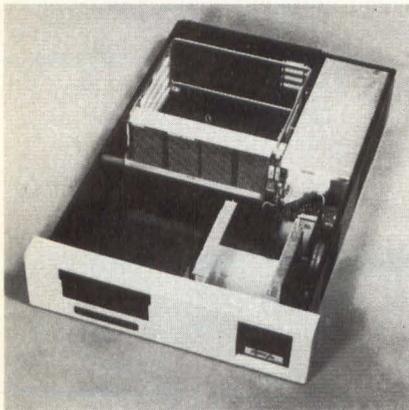
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Expansion Enclosure For Q-Bus Systems



Designed for DEC's Micro 11 and Micro VAX systems, this expansion enclosure provides a second Q-bus backplane and cage with 8 quad (16 dual) slots, a 360W power supply with +5 VDC, ± 12 VDC and +24 VDC to support additional controllers and mounting hardware for 5 1/4" or 8" internal peripherals. It can also be used with the LSI-11, PDP 11/23 and PDP 11/23 Plus. **Dyna Five**, Garden Grove, CA **Circle 206**

Video I/O Converter For Array Processors

This Video I/O Converter, the ZIPVID, digitizes an image from an RS-170 input and passes it directly to the ZIP 3216 array processor's memory via the ZIP's 40 Mbyte/sec internal bus in real time, eliminating the need for an external frame grabber. The ZIP 3216 executes algorithms such as 2D FFTs, convolution, image rotation and erosion-dilation. The ZIPVID costs \$3,000, and the ZIP 3216 is \$8,000 in single units. **Mercury Computer Systems**, Lowell, MA

Circle 210

Communications Processor

Consisting of a set of modular components that can support up to 32 full- or half-duplex communications lines and one or two host computers, this small-scale communications processor (Comten 5620) features VLSI technology and comprehensive, built-in self-test programs. Operating as a front-end processor in a small network, the Comten

5620 concentrates data at remote sites, runs COS2-based networking software and provides one to four Mbytes of main memory. Price is \$22,000. **NCR**, St. Paul, MN **Circle 207**

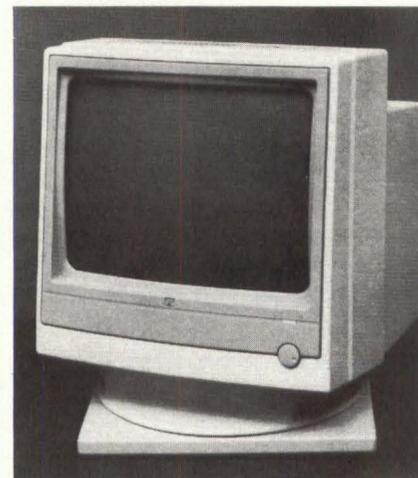
PERIPHERALS

Video Graphic Recorder

Designed for use with computer graphics systems, the VGR 5000 Video Graphic Recorder produces photographic-quality, monochrome, continuous-tone copies from monochrome or color raster scan video sources. The recorder prints images from raster scan video sources up to 1116 lines/frame, 60 Hz noninterlaced or up to 2233 lines/frame, 60 Hz interlaced. Equivalent 50 Hz refresh rates can be used. **Honeywell**, Denver, CO

Circle 165

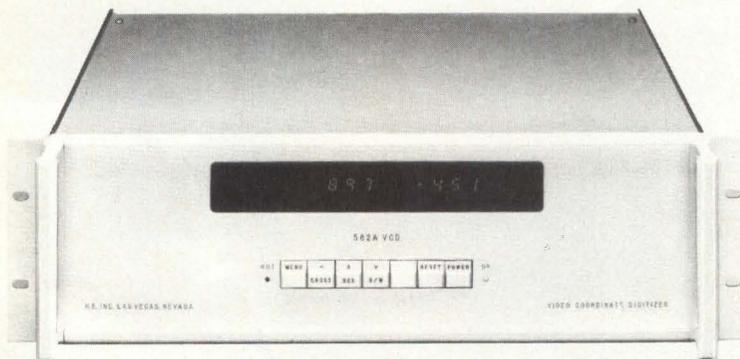
64 kHz Monitors



The latest additions to this firm's line of Patriot color monitors, these noninterlaced RGB monitors (Model 8864, 8865) provide 64 kHz operation. The Model 8864 Patriot is a 19" diagonal shadow mask CRT in a chassis or metal cabinet. The Model 8865 is available in a plastic cabinet with a tilt/swivel base mount option. The video bandwidth is 100 MHz and power consumption is typically less than 100W for both monitors. **Aydin Controls**, Fort Washington, PA

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Flat-Panel Plasma Displays

Readable from distances no greater than 115', this plasma teledisplay terminal (available in 200 different models) features alphanumeric characters that are 2" high. All TDS models are RS-232-C

NEW PRODUCTS

compatible and can be driven by many devices and protocols. They are expandable to 80 characters/line and up to 24 lines to emulate a full 1920 character CRT screen. Prices start at \$3,000. **Telegenix**, Cherry Hill, NJ **Circle 164**

MCP-Intensified Diode Array Detector



This proximity focused, microchannel plate-intensified diode array detector, the Model 1421 detector, uses a 25 mil-diameter intensifier which illuminates the entire 1024 element diode array. The resulting detector is sensitive, distortion free and can be gated at high speeds. The Model 1421 comes in red enhanced or blue enhanced versions. The MCP intensifier can be run continuous or gated to less than 10 nsec. Price is \$36,000. **EG&G Princeton Applied Research**, Princeton, NJ **Circle 153**

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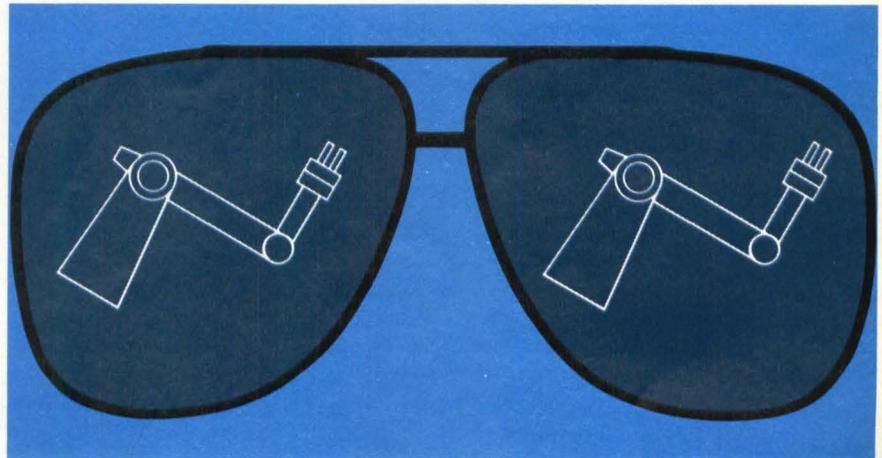
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Based on parallel transfer disk drive technology, this disk subsystem operates at transfer rates up to 9.3 Mbytes/sec to support real-time image processing and communications applications. The Concept 21 can command five channels of

disk I/O from a single drive, with each channel operating at a 1.86 Mbytes/sec peak transfer rate. Features include a steady-state transfer rate to the processor port of 8.1 Mbytes/sec, support for up to 4 PTD drives, controller supplied for formatting of drive services and host adapters for Multi, VERSA, UNI, VME, and Q-Bus. Price is \$17,700. **Storage Concepts**, Costa Mesa, CA **Circle 172**



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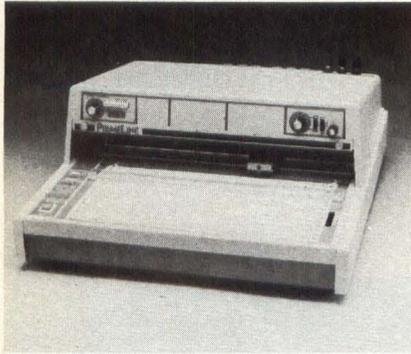
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NEW PRODUCTS

1, 2 and 3 Pen Flatbed Recorders



The PrimeLine R-OX Series of flatbed laboratory recorders uses 250 mm wide chart paper, with all pens overlapping to write the full chart width. Each channel (pen) of the R-OX Series measures signals from 1 mV F.S., for high input sensitivity applications up to 200V. With a calibrated 100% zero suppression switch and a variable attenuator for measuring signals in between standard preset ranges, the recorders feature a pen speed of 0.5 sec full scale (250 mm). **Soltec Distribution, Sun Valley, CA Circle 158**

Television LineFinder

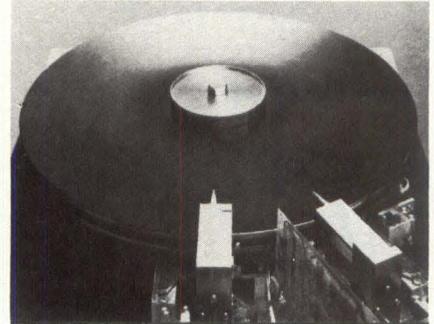
Designed for use in repair, routine maintenance and set up of video cameras, the Model II LineFinder allows digital selection of any single scan line in the raster for detailed waveform analysis on an oscilloscope. The Model II allows direct connection between the camera and the oscilloscope at all times. Housed in an aluminum cabinet and weighing approximately 5 lbs., the instrument is priced at \$495. **Visual Information Institute, Xenia, OH Circle 160**

Video Peak Store

Designed for multilayer inspection, this freeze-frame video display can be added onto the firm's Lixiscope LS-82-112 or obtained with the new LS-82-113 higher-detail resolution Lixiscope. The Video Peak Store 493G continually updates the image on the TV monitor which can then be frozen at any time. Scintillating images such as those from a low radiation level fluoroscope can be made sharp and clear, thus extending the life of the isotope. Split screen viewing is another fea-

ture of the Video Peak Store 493G. **Glenbrook, Morris Plains, NJ Circle 154**

Real Time Digital Video Recorder



Providing 60 seconds of real time digital imaging, 522 x 512 bits deep, the DR 6000 real time digital video recorder also features variable record and playback random access. The DR 6000 uses LSI components, has a sealed drive with recirculating air flow system and a proprietary protective overcoat on the disk media. In addition, the recorder's architecture provides for optional expansion of real-time storage or increased recording rate. **Oktel, Fremont, CA Circle 177**

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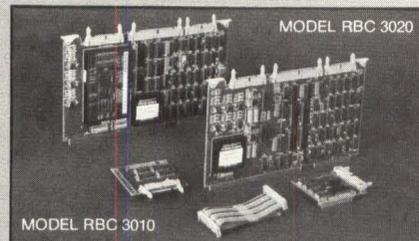
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NEW PRODUCTS

Personal Laser Printer

Printing 850 cps, achieving a speed of eight pages/minute, the LBP-8 A1 laser beam printer produces a 300 dpi resolution. Using electrophotography, laser-beam scanning technology, this desk-top size printer offers cassette feed or manual feed. Multiple fonts are available in ROM cartridges. Price is \$3,500. **Canon**, New York, NY **Circle 166**

80 MBPS LAN

Transmitting data at 80 Mbps, the ProNet-80 connects up to 240 Unibus or Multibus workstations using any combination of twinaxial or fiber optic cabling. In addition, this LAN is software compatible with the firm's original 10 Mbps network, ProNet-10. The network also contains an error detection system and a flexible addressing system. Price is \$8,000/host interface. **Proteon**, Natick, MA **Circle 169**

IBM PC Graphics System

Designed for the IBM PC and compatibles, the Sextant graphics display system includes a single-board controller and a color monitor, available in either a 14" or 19" display. The system offers a 16-color display from a palette of 4096 colors. Optional resolution of up to 1024 x 768 pixels is available. Price ranges from \$1,700 to \$2,900. **TAT Graphics Group**, Sunnyvale, CA **Circle 173**

Color Graphics Monitor With 150 MHz Bandwidth



Providing 150 MHz bandwidth, this 19" color graphics display monitor (CDI920) features automatic vertical synchronization of up to 180 Hz and .31 mm dot pitch resulting in a display of 1280 x 1024 resolution. The CDI920 can also optionally use a .25 mm dot pitch tube with 1580 x 1260 resolution. With a MTBF of over 16,000 hours, the monitor is avail-

able with a tilt/swivel base and can be electronically interfaced to any graphics generator. Price is \$2,000-\$3,500. **Amtron**, Santa Clara, CA **Circle 156**

Smart Terminal

Providing all features of the QVT-102 and emulating the Hazeltine 1500, the Lear Siegler ADM 3A/5 and the TeleVideo

910, this full-function editing terminal (QVT-101) features block mode data transmission. Offering 16 host or user-programmable functions and a 14" screen, the QVT-101 also includes a bi-directional printer port, a RS-232 interface, a nonglare green screen and foreign character sets. Terminal including a detachable keyboard is \$395. **Qume**, San Jose, CA **Circle 174**

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Winchester/Floppy Subsystem

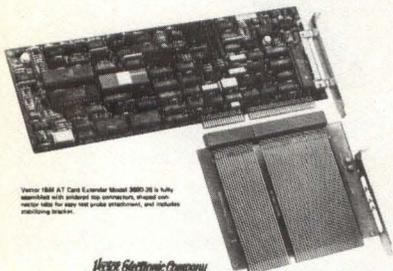
Designed for Q-Bus computers, this Winchester/Floppy subsystem, the CI-550-30W, is formatted with up to 30 Mbytes of Winchester and up to 400 Kbytes of floppy storage. Using DEC's RQDX1 controller, the CI-550 can read and write standard RX-50 floppy format, allowing media portability. The Winchester drive has an average access time of 75 msec and a transfer rate of 625 Kbytes/sec. With error detection and correction, error retry, block mode DMA and bad block mapping, the CI-550 can operate in any Q-Bus 18- or 22-bit environment. Price is \$2,595 (20 Mbytes). **Chrislin Industries**, Westlake Village, CA **Circle 226**

Tri-Density GCR Tape Subsystem

Designed to be integrated into LSI-11/ Micro 11, PDP-11 and VAX minicomputers, this tri-density tape subsystem is compatible with 800, 1600 and 6250 bpi tape. The drives are interfaced through controllers made by Emulex, Western Peripherals, Dilog or Spectra Logic. Featuring GCR technology that holds data at 6250 bpi, a standard 10.5" reel of magnetic tape can hold up to 180 Mbytes of data. Price starts at \$12,100. **California Computer Group**, Costa Mesa, CA **Circle 224**

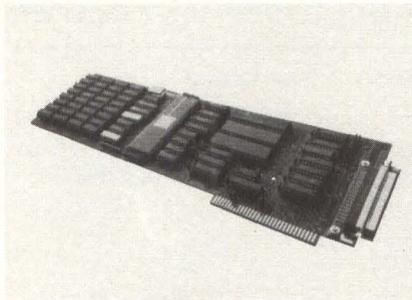
BOARDS

IBM AT Extender Board



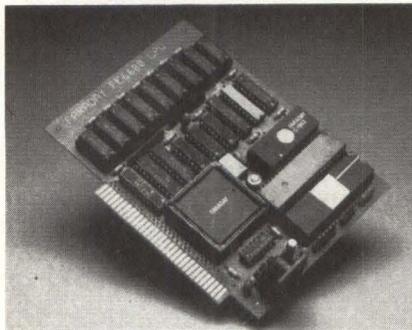
Allowing in-circuit probing of functional boards as well as providing marked test points for 98 bus lines on both card connectors, the Model 3690-26 extender board includes a heavy-duty bracket to support cards while troubleshooting. Bus-line current-ratings are 5A with 200V RMS or 300 VDC voltage ratings. In one-four piece quantities, the 3690-26 sells for \$45. **Vector Electronic**, Sylmar, CA **Circle 192**

Colors Added To Card Set



The VX/PC board set has been upgraded to a color palette of 16.8M, out of which 512 colors are concurrently displayable at a resolution of 672 x 480. The original two-card set offers a 4096 color palette. Price for the standard VX/PC is \$2,495, with the 16.8M color option \$2,995. **Vectrix**, Greensboro, NC **Circle 196**

IBM PC Bus Compatible SBC



Measuring 3.9" x 5.5", this plug-in single-board computer (Micro PC) is one-fifth the size of a standard IBM motherboard, while fully compatible. Featuring an 8088 CPU with optional 8087 coprocessor, 256K of parity RAM, 32K of user EPROM space, 4 DMA channels, 3 timer channels, 1 IBM-compatible keyboard port, 1 speaker port and 1 reset port, the Micro PC supports MS-DOS, Concurrent PC-DOS, VRTX and UNIX. Price is \$695. **Faraday Electronics**, Sunnyvale, CA **Circle 191**

Q-Bus Winchester/Floppy Controller

Compatible with DEC's MSCP software, the UDC11 dual-width Winchester and floppy disk controller is compatible with the Q-Bus. Under MSCP, the UDC11 allows the use of ST506 interface drives of any capacity. Hence, system integrators can design MicroPDP-11 and MicroVAX-I and II compatible systems with RX50 emulation. The UDC11 can

also control any combination of up to four Winchester cartridge and floppy drives. The Online Configuration Tool (OCT) allows users to configure the controller to operate any ST506-compatible Winchester or cartridge drives as well as 5 1/4" or 8" floppy drives. Price is \$1,795. **Andromeda Systems**, Canoga Park, CA **Circle 228**

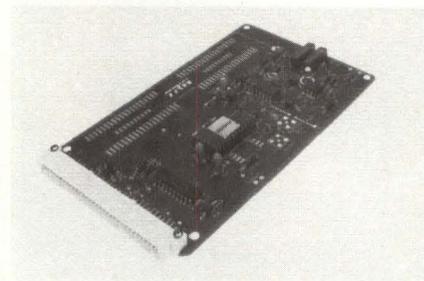
4-Mbyte Memory For VAX 11/780

Compatible with the VAX-11/780, VAX-11/782 and VAX-11/785, this 4-Mbyte (DR-278) semiconductor memory array board supports error detection and correction and is arranged on a single hex-width PCB. Installed in pairs, the DR-278 arrays provide a 64 Mbyte maximum capacity in a single VAX-11/780 cabinet. Typical access time is 200 nsec. Price is \$6,285. **Dataram**, Cranbury, NJ **Circle 189**

Monochrome Display Adapter For IBM PC

An enhancement to the IRMA family, this monochrome display adapter (IRMAvision) enables IRMA-equipped IBM PCs, XTs, ATs and compatibles to emulate IBM 3278 models 2 through 5, gaining a direct full-screen link to IBM 3270 networks. IRMAvision provides text in 80 columns x 25 lines, 139 x 29, 80 x 34 and 80 x 45 modes. Price is \$695. **Digital Communications Associates**, Norcross, GA **Circle 193**

7 And 8-Bit A/D Converter Evaluation Boards



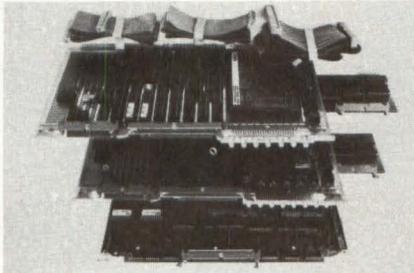
Requiring +5 and -5.2V power supplies, these Eurocard evaluation boards are designed for the firm's 7- and 8-bit A/D converters. The TDC1048EIC aids in evaluating the TDC1048 8-bit converter, while the TDC1047EIC aids in evaluating the 7-bit TDC1047. Each board includes the associated converter and circuitry for generating reference voltages, conditioning input signals and latching output data. Provisions are made for analog gain and

NEW PRODUCTS

offset adjustments. Prices are \$233 (1047 EIC) and \$365 (1048EIC) in quantities of one to nine. TRW, La Jolla, CA

Circle 178

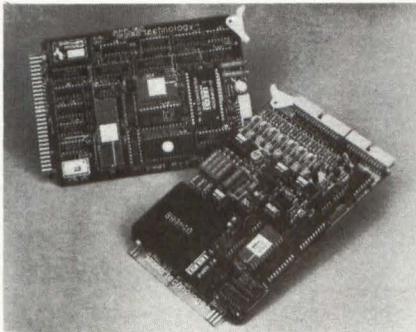
Multibus Analog I/O System



Designed for real-time simultaneous sample/hold applications, this analog I/O system achieves a combined 80K samples/sec throughput. The RBC 3010 analog input subsystem has four simultaneously sampled A/D channels with 5 nsec, aperture uncertainty, 12 bits resolution with 0.04% FSD accuracy, external clock, trigger and gate inputs. The RBC 3020 analog output subsystem is a 2 simultaneous channel D/A with 12-bit resolution, 1/2 lsb integral and differential linearity, and 2 nsec settling time to within 0.01% for a 10V step. Roy Ball Associates, Ontario, Canada

Circle 197

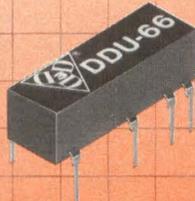
STD Bus Analog Processor/Signal Conditioning Interface



Intended for distributed processing applications, this two card set, the ST4603 Analog Input Processor and the ST4703 Analog Signal Conditioning Interface, accepts and processes signals from a range of sensor devices, such as RTDs, thermocouples, and strain gauges. The ST4703 functions at the front end for eight differential inputs. The ST4603 accepts conditioned analog signals from one to eight ST4703 units, providing the capability to interface 64 differential input channels. Price is \$800 (603) and \$1,040 (703). Applied Micro Technology, Tucson, AZ

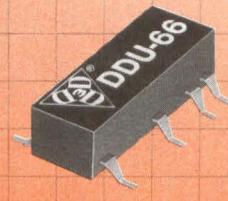
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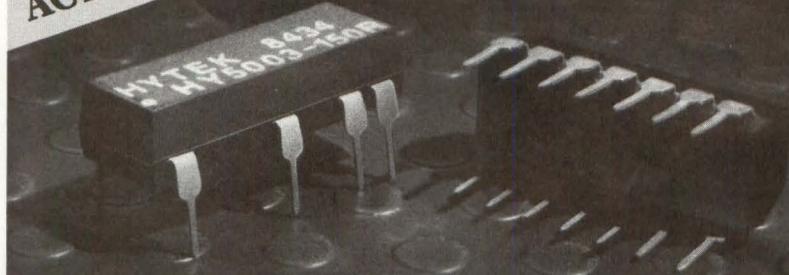
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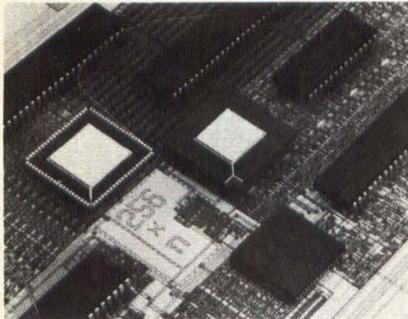
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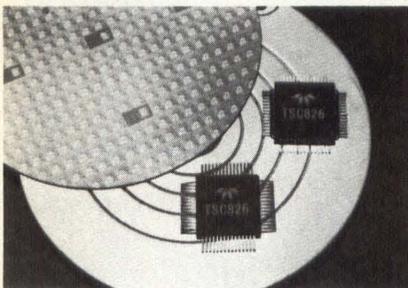
COMPONENTS

3-Micron HCMOS Standard Cell Series



This series (SA) of 3-micron, double-level metal HCMOS standard cells includes user configurable RAMs, ROMs and PLAs, basic analog functions and complex LSI cells. The devices have typical loaded on-chip gate delays of 2.5 nsec. Designs can be implemented on the SA series with the Highland 2 Design system. Package options include plastic and ceramic DIPs, pin-grid arrays, and ceramic/plastic leadless chip-carriers. **Mostek**, Carrollton, TX **Circle 144**

A/D Converter With LCD Drive



With outputs that directly drive a graphic LCD display, the TSC826 A/D converter features 40 LCD data segments that give a 2.5% resolution bar or cursor display. With the TSC826, moving point analog display movements can be replaced with solid state displays. Zero scale drift is $5\mu\text{V}/^\circ\text{C}$, and conversion rate is typically 5/sec, adjustable by a single-extended resistor. **Teledyne Semiconductor**, Mountain View, CA **Circle 138**

CMOS 32-Bit μP Development

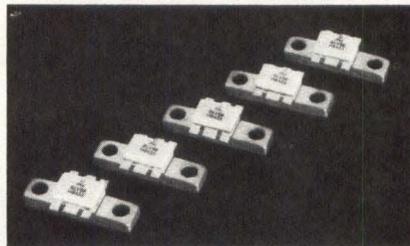
Fabricated in 1.3 micron CMOS, 2-layer metal process technology and containing over 300,000 transistors, this 32-bit microprocessor test chip operates at 5 MIPS. The Micro 32 test vehicle incorporates a proprietary pipelined system

architecture and a cache memory scheme permitting high speed interface with I/O processors and file processors. Featuring a 200 Kbit ROM with a 50 nsec cycle time and a 32-bit ALU, the chip measures 6.5 mm \times 9.0 mm. No definite packaging configuration has been chosen. **Hitachi**, San Jose, CA **Circle 219**

4K \times 4-bit SRAM

Fabricated using the silicon gate HCMOS II technology, the MCM6168 16K SRAM is available with 45, 55 or 70 nsec access times. CMOS circuitry allows 80 mA power consumption max in active mode, 5 mA max standby (TTL levels) and 2 mA max standby (CMOS input levels). Operating from a single +5V ($\pm 10\%$) power supply and packaged in a 300 mil, 20-pin plastic DIP with JEDEC standard pinout, the SRAM is priced from \$5.50- \$8.2 in 10,000s. **Motorola**, Austin, TX **Circle 223**

TV Broadcast Transistor



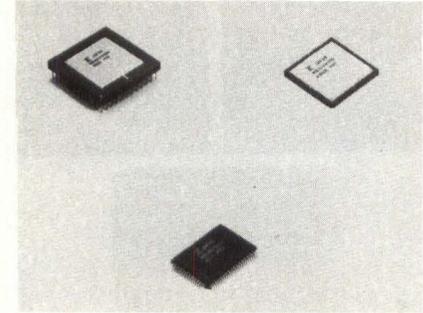
Intended for TV bands IV/V, the BLV59 transistor brings a guaranteed output power rating of 30W to small TV broadcast transmitters in remote locations. Although normally intended for single-ended circuits, two BLV59s can be used in a push-pull configuration to achieve an output power of 50W minimum. The transistor provides emitter ballasting resistors and gold metallization. At 860 MHz and a supply voltage of 25V, typical output power is 40W, power gain is typically 8 dB and collector efficiency 50%. **Philips**, The Netherlands **Circle 135**

64 Kbit PROM

Organized in 8K \times 8 bits, the AM27S49 64 Kbit bipolar PROM is available in 40 nsec and 55 nsec commercial versions. This PROM incorporates three-state outputs and features platinum-silicide fuses. Produced in this firm's proprietary IXOM-S process, a scaled, ion-implanted, oxide-isolated bipolar process, the AM27S49 has applications in high-density microprogrammed control store memory. Housed in a 24-pin 600-mil

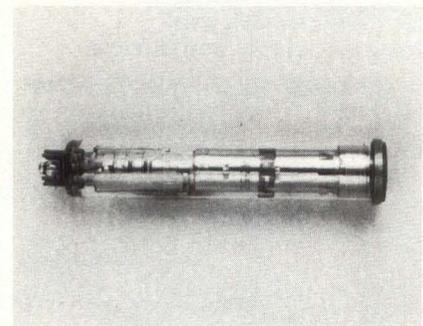
ceramic package, the 55 nsec version is priced at \$72.50 and the 40 nsec device is \$108, each in 100s. **AMD**, Sunnyvale, CA **Circle 220**

CMOS Gate Array With 1-Kbit RAM



Supported by the firm's CAD system, this 2375-gate CMOS gate array (C2300VM) has a 1-Kbit RAM block. The RAM can be configured as 256 4-bit words, 128 8-bit words, 64 16-bit words, or 32 32-bit words and can be interconnected with gates in the array to form various logic-plus RAM configurations. Operating from a single 5V supply, the C2300VM offers 2 nsec typical gate delays with power dissipation of 100 mW/chip at 10 MHz. **Fujitsu**, Santa Clara, CA **Circle 143**

Vidicon Camera Tube



Designed for closed-circuit television applications, this 2/3" vidicon camera tube, the Ultricon III, achieves nearly 100% quantum efficiency in the visible spectrum with a spectral response extending from the near-ultraviolet through the visible and into the near-infrared. The Ultricon III features no after-image or image burn-in, low lag and minimal comet-tail effects. **RCA**, Lancaster, PA **Circle 136**

16-Bit CMOS Bit-Slice Processor

Containing four processing elements that are functionally identical to bipolar 2901C 4-bit slices, this 16-bit CMOS bit-slice

NEW PRODUCTS

processor, the WS59016-C, also contains a 2902-equivalent carry look-ahead unit. Operating at a 15 MHz clock rate over the commercial temperature range and 12 MHz military, the WS59016-C consumes 150 mW at 25°C and 10 MHz. Price is \$50-\$62. **Wafer Scale Integration**, Fremont, CA **Circle 151**

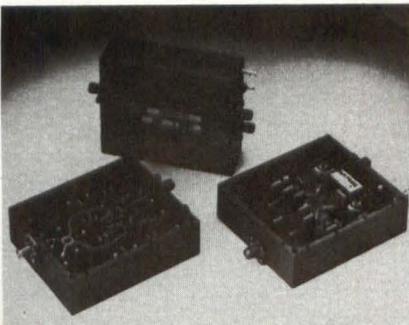
8-Bit A/D Converter With 1.5µsec Conversion Time

Using a half-flash conversion technique to achieve a 1.5µsec conversion rate, this µP-compatible 8-bit A/D converter features a built-in track and hold function enabling signals with slew rates of 100 mV/µsec to be converted without an external sample and hold. The AD7820 dissipates 75 mW max. Six versions are available: LN, CQ and UD guarantee ± ½ lsb total unadjusted error over full temperature range; KN, BQ and TD +1 lsb total unadjusted error. KN and LN operate over 0°C to +70°C. BQ and CQ operate over -25°C to +85°C and TD and UD over -55°C to +125°C range. Price starts at \$9.95 in 100s. **Analog Devices**, Norwood, MA **Circle 152**

DAC 80V Replacement

A pin-compatible addition to the DAC80V, AD DAC 80V, DAC 800V and HI-5680V Series of converters, the HI-5690V Series of 12-bit D/A converters guarantees an output swing of 20V (from +10 to -10) in under 1.5 µsec to within 0.012% of its final value. The output amplifiers feature a slew rate of 50V/µsec, yet overshoot less than 1V. The converters operate from power supplies of ±11.4 to ±16.5V and with +5V supply connector optional. **Harris Semiconductor**, Melbourne, FL **Circle 221**

Image Recovery Mixer/Preamps



Providing image rejection and noise figure in communication and radar systems.

Your view for the future



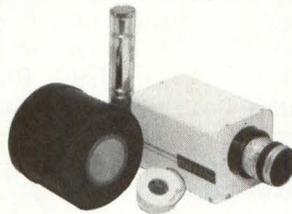
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NEW PRODUCTS

tems, these image recovery mixer preamps operate from 12.7 to 13.25 GHz with an IF frequency from 50 to 90 MHz. The Model IEM005 has a SSB noise figure of 5.5 dB max, RF/F gain of 22 dB \pm 1 dB, and 15 dB minimum image rejection. The unit is 3.25" \times 2.25" \times 1.00" with SMF female connectors. **Time Microwave**, Santa Clara, CA **Circle 133**

Digital Signal Processor

As an alternate-sourced device for the NEC μ PD7720 digital signal processor, this digital signal processor (S7720) dissipates 950 mW. The extended temperature version operates over the -40°C to +85°C range. Fabricated in NMOS, the S7720 is a complete 16-bit microcomputer with on-chip data ROM (512 \times 13 bits), on-chip RAM (128 \times 16 bits) and instructional ROM (512 \times 23 bits). **Gould**, Santa Clara, CA **Circle 150**

SOFTWARE

DASH-SPICE Circuit Simulator

Intended for designing and checking circuits combined with the DASH Schematic Design System, the DASH-SPICE Circuit Simulator brings advanced electronic circuit simulation capabilities down to the PC-level. Designed to run on IBM PC, XT or AT compatibles with 512-Kbytes memory, MS-DOS 2.1-3.0, floating point coprocessor, all printers and plotters using the HP-GL graphics language, DASH-SPICE includes SPICE-LINK, an interface translator that enables SPICE users to upload designs to SPICE already running on larger machines. Price is \$1,980 (SPICE-

LINK: \$600) **FutureNet**, Canoga Park, CA **Circle 212**

Graphics Tools For Apollo DN600, DN300

The DI-3000 device independent graphics tools package can now run on the Apollo color DN600 and monochrome DN300 workstations. DI-3000 can put each application program in a different window or treat each window as a different graphics output device for an application. DI-3000 also supports 47 software fill patterns and 64 hardware linestyles on the workstations. Based on the Core standard, DI-3000 enables graphics programmers to access the full capabilities of raster displays, pen plotters, film recorders and other output devices, without constantly having to modify the application. License for the DN300 and DN600 begins at \$5,500. **Precision Visuals**, Boulder, CO **Circle 214**

Language Compiler Optimizer

Designed to run on the firm's line of 32-bit systems, this language compiler optimizer, the Global Optimizer, looks for patterns of code, replaces them with shorter patterns, removes redundancy and applies programming guidelines and common sense to the code generation process. Depending on the application, the optimizer enhances the performance of programs written in Pascal, C, Basic, PL/I, COBOL and Fortran-77. The company also introduced two additional compiler enhancements for the Fortran-77 including two new datatypes: BYTE and Logical I. **Data General**, Westboro, MA **Circle 247**

Netlist Translator

This package of software programs can accept a netlist file independent of the language in which it is written and convert it into this firm's proprietary circuit language. The package, Flexible Interface Translator (FIT), generates a computer program that translates a user's netlist file into the proprietary BOLT circuit description language. A translator builder, FIT consists of reusable code and table-driven algorithms that can be modified to accept varying input languages. **Gould**, Santa Clara, CA **Circle 213**

PCB-Design Software

Under mutual agreement, Vectron's DNA2000 PCB design software is avail-

able with Harris' computer systems, enabling them to layout and auto route large PCBs. The software is slated to run initially on the recently introduced UNIX-based workstations. DNA2000 will also be ported to Harris superminis. **Harris**, Ft. Lauderdale, FL **Circle 216**

VAX/VMS Cross-Compiler

The Lattice iAPX86 compiler is now available as a cross-compiler for VAX/VMS systems. It corresponds to Version 2.14 of the native MS-DOS compiler and can generate code for the Intel 80186 chip. Available on a 9-track magnetic tape in VMS back-up format, the cross-compiler contains a hierarchical directory that mirrors the recommended native compiler structure. Utilities included with the cross-compiler are the Object Module Disassembler and the Function Extract Utility. Price is \$3,350. **Lattice**, Glen Ellyn, IL **Circle 248**

Electronic Component Libraries

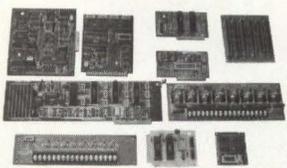
For use with the firm's CAE workstations, these libraries are software packages that provide detailed descriptions of electronic components. One covers μ Ps and peripherals, another describes HCMOS components, a third describes memory chips and the fourth covers PLA/PAL. The μ P/peripheral library includes graphic and timing representations of μ Ps such as the 68020, 80286 and the 16032. Prices are \$5,000 for μ P/Peripheral, \$5,000 for PLA/PAL and memory, \$2,500 for HCMOS. **Daisy Systems**, Mountain View, CA **Circle 217**

Communications Software For TIWAY I Network

Providing a high level interface between the TIWAY I LAN, this host support software also supports the TIWAY I universal command language that allows the host to control any TI programmable controller (P/C) over the TIWAY I. Three versions are available: VAX/VMS, PDP-11/RISX-II and TI/IBM/P/C. All three packages support multiple languages and allow the user easy access to TIWAY I data via a set of subroutines. The VAX/VMS and PDP-11 versions support FORTRAN, PASCAL and MACRO, while the TI/IBM/P/C version supports FORTRAN, PASCAL and BASIC. **Texas Instruments**, Johnson City, TN

Circle 215

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AND
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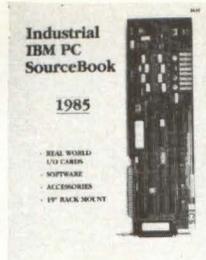


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NEW LITERATURE



Industrial PC Sourcebook. Targeted primarily at IBM PC and compatible users in industrial laboratories, factory automation and process measurement and control, the Industrial IBM PC Sourcebook offers a selection of equipment and components that can be used as solutions in industrial applications. Board-level products are listed in addition to a complete 19" rack mounted industrial IBM-compatible PC printer and monitors, PC-bus peripherals and accessories, a selection of software and literature.

ICS

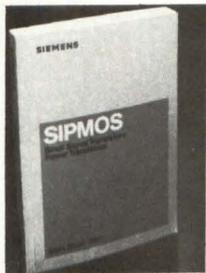
Circle 255



Flash A/D Converter Terminology Application Note. Addressing flash A/D converter terminology, this 12-page application note (TP-30), "Understanding Flash A/D Converter Terminology" from TRW LSI Products Division, defines the specifications the firm uses in its flash A/D converter data sheets. The paper serves audiences whose interests lie in digital definitions and high frequency analog problem-solving techniques.

TRW

Circle 253



1985 SIPMOS Data Book. General technical and mounting information on the SIPMOS product line is provided in this 539-page data book from Siemens Components. Included are the BUZ 300 Series of TO-218 products including standard and FREDFET (Fast Recovery Epitaxial Diode Field Effect Transistors) types, selection guides and an industry cross-reference.

Siemens Components

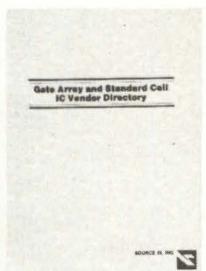
Circle 260



Procedural Elements For Computer Graphics. With an emphasis on raster scan graphics, this 430-page book written by David F. Rogers introduces computer graphics hardware and stresses the conceptual understanding of CRT displays and interactive devices. The following chapters look at raster scan graphics, including line and circle drawing, polygon filling and antialiasing algorithms, two- and three-dimensional clipping such as clipping to arbitrary convex volumes. Each topic discussion is followed by a detailed algorithm.

McGraw-Hill

Circle 251



Gate Array/Standard Cell Vendor Directory. Sixty-eight companies offering gate array and standard cell design, prototype and production devices are listed in this 48-page Gate Array And Standard Cell IC Vendor Directory from Electronic Trend Publications. The Directory is divided into three sections: Section one offers an approach to deal with vendors; it discusses minimizing first-time problems and coping with the second source issue. Section two organizes the vendor list by technology and covers both front and back end cost elements. Section three profiles the 68 companies with lead times, development costs, pricing and vendor background, services, CAD capability and future products. Minimum volumes and delivery schedules are also detailed.

Electronic Trend Publications

Circle 250

Image Compression. A series of articles on Digital Image Compression is now available from Joseph Mauro. The series, which was to have been published in *Electronic Imaging* magazine, contain information on Image Theory, Image Compression, definitions of Information and Applications of these techniques. For further information please contact: Mr. Joseph Mauro, Westgate Road, Mount Vernon, New Hampshire 03057.

The Art of Image Engineering

A Case Study: Space Shuttle Telemetry

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Application:

Real-time acquisition and analysis of high-resolution telemetry images by a ground-based computer system.

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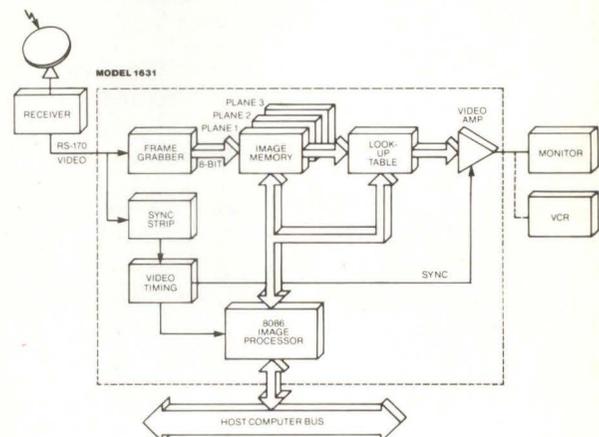
Image-by-Image manipulation (averaging) of stored frames to reduce noise and recover important picture data "lost" in transmission.

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July 1-3

Introduction to Data Communications Course. Boston, MA. (also in Wash. DC — July 10-12, New York, NY — July 24-26 and San Francisco, CA — July 24-26) Contact: Systems Technology Forum, 9000 Fern Park Dr., Burke, VA 22015. (800) 336-7409.

July 8-9

Data Communications and Networking for the IBM PC and Other Personal Computers Seminar. Atlanta, GA. (also in New York, NY—July 22-23) Contact: Software Institute of America Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

July 9-11

Principle and Applications of Fiber-Optic Communication Systems Course. San Francisco, CA. (Also in Atlanta, GA—Sept. 10-12) Contact: Lightech, 2116 E. Arapaho, Suite 515, Richardson, TX 75081. (214) 680-8227.

July 10-12

Local Area Networks for the IBM World Seminar. San Francisco, CA. Contact: Bob Beshalske, Communications Solutions Inc., 992 S. Saratoga-Sunnyvale Rd., San Jose, CA 95129. (408) 725-1568.

July 10-12

World Computer Graphics '85 Conference. New York, NY. Contact: American Communication Group Inc., 8300 Greensboro Dr., Suite 690, McLean, VA 22102. (213) 534-4250.

July 15-17

Standard Network Protocols Seminar. Atlanta, GA. (also in St. Louis, MO—July 22-24 and Boston, MA—July 29-31) Contact: Data-Tech Institute, Lakeview Plaza, P.O. Box 2429, Clifton, NJ 07015. (201) 478-5400.

July 15-18

1985 National Computer Conference. Chicago, Il. Contact: NCC '85 Registration, 1970 Chain Bridge Rd., McLean, VA 22109-0164. (800) 622-1985.

July 17

iRUG Annual International Conference. Chicago, Il. Contact: Catherine Moon, Intel Corp., 5200 N.E. Elam Young Parkway, MS/Hf2-57, Hillsboro, OR 97123. (503) 640-7038.

July 22-26

SIGGRAPH '85. San Francisco, CA. Con-

tact: Ellen Frisbie, SIGGRAPH '85 Conference Services Office, 111 East Wacker Dr., Chicago, Il. 60601. (312) 644-6610.

August 4-8

ASME International Computers in Engineering Conference. Boston, MA. Contact: Mary Benedict, American Society of Mechanical Engineers, 345 East 47th St., New York, NY 10017. (212) 705-7100.

August 12-14

Data Communications: Network Design, Integration and Applications. Los Angeles, CA. Contact: Software Institute of America Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

August 13-15

Computer Graphics '85 East. Boston, MA. Contact: National Computer Graphics Association, P. O. Box 3412, McLean, VA 22103. (800) 225-6242.

August 14-16

Structured Systems Development with 4th-Generation Languages. Denver, CO. Contact: Software Institute of America Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

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