FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

MAY 29, 1986

ELECTRONIC DESIGN®

A HAYDEN PUBLICATION

Graphics coprocessor chip creates multiple windows

ATE for fast VLSI: It's all in the timing

Inside look at NCC '86

Universal filter combines best of analog and digital worlds

featuring zero standby power and 35ns maximum propagation delay, better than anything our competition has yet offered.

What's more, our CMOS technology is going to open up a new and exciting product area for you in the months ahead. So stay tuned for another major announcement. And a celebration that'll make this one look like a PTA meeting.

Why are we doing all this, you ask?

Simply to offer you a range of speed/power options unmatched anywhere. From ECL to CMOS. Not to mention a line of bipolar ICs that stands out in any crowd.

So call or write today for our new CMOS brochure.

Monolithic Memories, 2175 Mission College Blvd., Santa Clara, CA 95054. (800) 247-6527.

But if you want to beat the crowd, you'd better hurry.

Monolithic Memories

CIRCLE 131

UPI/Bettmann

Monolithic Memories announces CMOS.

People tend to get a bit excited when they hear that Monolithic Memories is getting into CMOS.

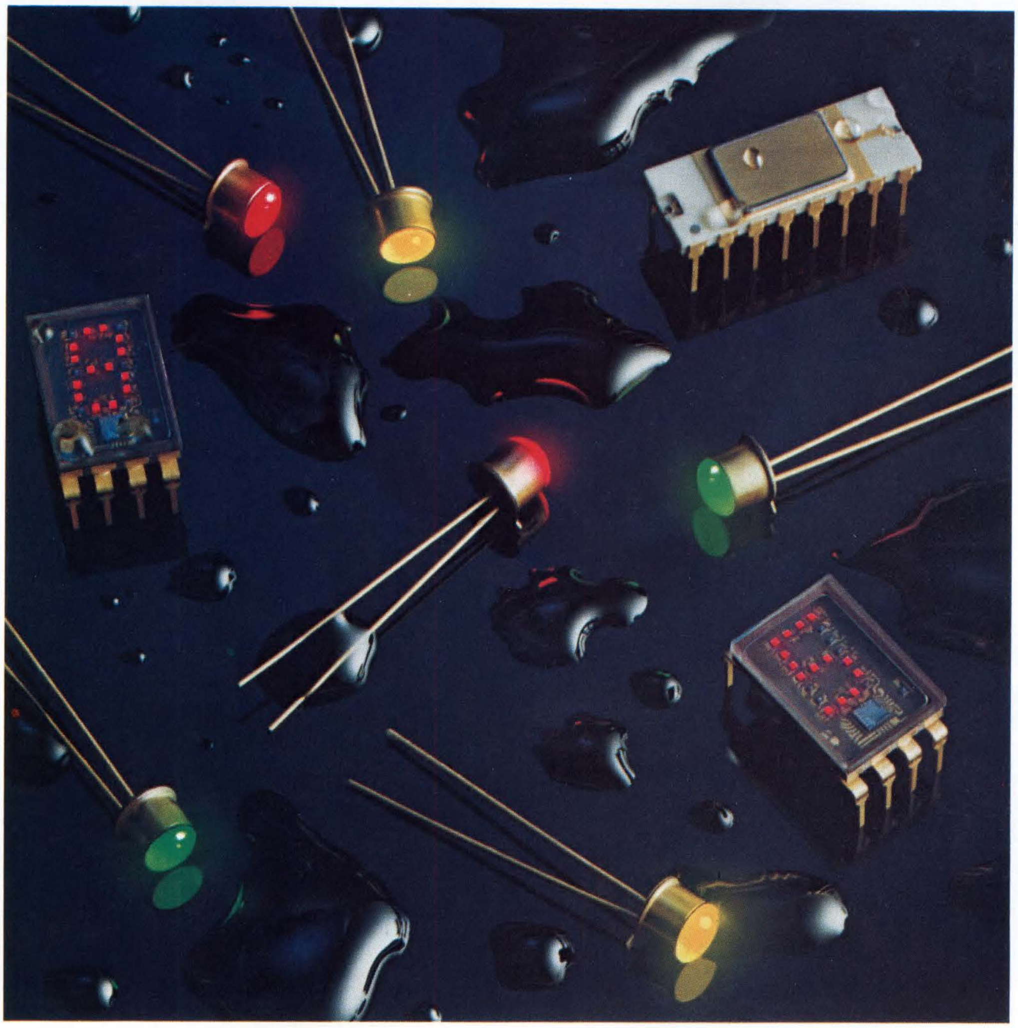
And frankly, we can't blame them.

After all, we're doing things with CMOS that no one else has done before.

For instance, we're producing Double Density Interface and ZHAL™ circuits that run at CMOS power levels, with speeds rivalling the best of bipolar. And we're shipping them in volume.

We're also bringing CMOS to our PAL® product line, beginning with ZPAL™ devices

Finally, a reason not to buy bipolar ICs from Monolithic Memories.



ELECTRONIC DESIGN

INSIDE LOOK

VLSI testing envelops designers

"Finish the design, turn it over to manufacturing, and get on with the next project. Let the guys in testing figure out how to test it; that's what they get paid for."

For a long time, that was the typical designer's viewpoint. In every company there was a design group and there was a test group. Both went about their business without much interaction, and for good reason: Circuits were so basic that the schematics spoke for themselves.

Apparently those days have gone the way of the slide rule and the vacuum-tube voltmeter. Board testing was one of the first areas to feel the change. MSI-level components made the boards so complex that only the designer could give any clue about how to test the circuits.

Now, with the steadily advancing levels of integration, testing of VLSI application-specific ICs is beginning to fall under the umbrella of the design engineer. After he designs an ASIC on a workstation in his own lab, he must make the decision to commit the design to silicon—not the semiconductor house and not the silicon foundry. Faced with that formidable responsibility, he must leave the comfort and security of the workstation-based simulator and instead deal with testing the real chips. Unfortunately, very little test equipment is now around to help him test the physical IC. But the situation is changing: hard on the heels of the booming ASIC market, appropriate testers are bound to proliferate.

Regardless of how those new testers are implemented, they will face the same problems as the test equipment we cover in this issue's ELECTRONIC DESIGN Report on page 132. Today's ATE systems, for example, must maintain timing accuracies for the high-speed signals flowing through a large number of I/O pins. To alleviate the difficulties, ATE manufacturers are banking on some interesting technology—time-domain reflectometry, for example, to measure path lengths precisely and thus to set the required timing at the test pins.

Yes, the designer's job is constantly changing. But remember, no one ever said it would be easy.

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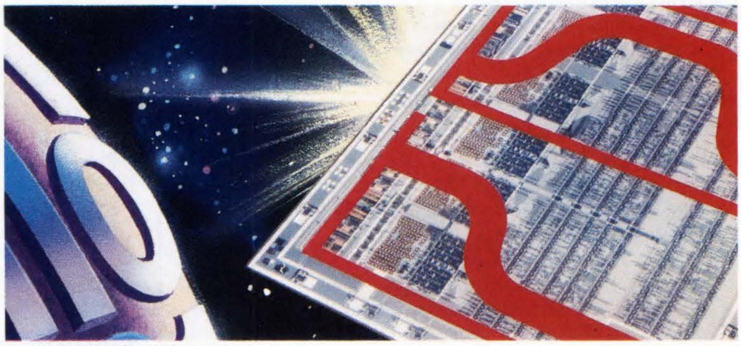
ELECTRONIC DESIGN

Departments



147 PROGRAMMABLE FILTER CHIP

News

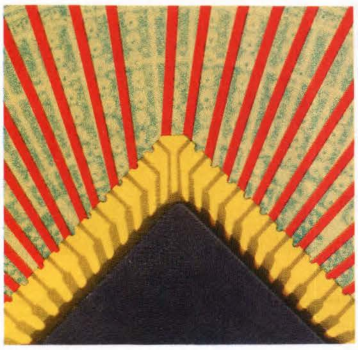
Newstrend

Industry Newsmakers

Electronic Design Report

Design Entries

1986 winner, Jesse H. Neal
Editorial Achievement Award.
Best in-depth analysis article series:
1985 Technology Forecast



132 TESTING FAST VLSI ICs

213 CONNECTORS

In The Next Issue

- ELECTRONIC DESIGN Report: ECL faces rivals subnanosecond gate arrays
- Industry Newsmaker: Twisted-pair transceiver IC reconciles trade-offs between distance and data rates
- Newstrends: X.25 boards for VMEbus, DIN keyboards
- PC AT gets board-level power for solids modeling

Design Applications

Product Report

Cover illustration by Tom Palmer

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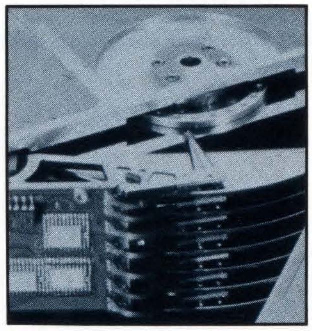
New Products

DON'T MISS THESE...

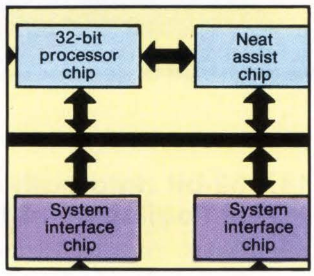
51 It used to be that a hard disk drive's cost per megabyte depended roughly on disk diameter: 14-in. drives—the largest—came in the cheapest, often making the choice easier.

No longer. Today the cost per megabyte is about the same for all sizes, so data transfer rate, access time, and power merit attention.

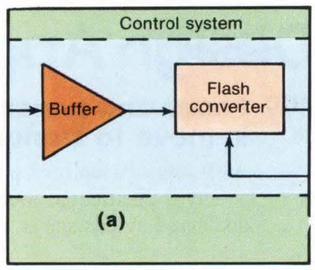


59 How do you design a computer system compatible with earlier ones but uses the latest multiprocessing technology?

NCR knows how: Specialized processors handle memory access, and the system bus gets tuned up for high-speed transmission.

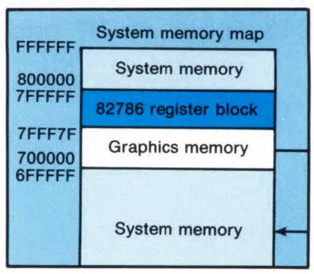


89 Video buffer amplifiers—the analog glue circuits needed for example, with high-speed flash converters—now have bandwidths up to 300 MHz while nonlinearity has fallen to 0.1%. But how? Current feedback, which also promotes variable gain.



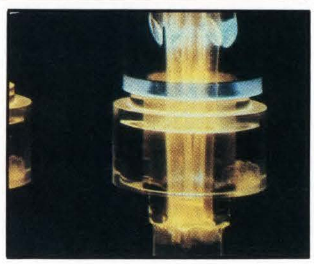
159 A single-chip graphics coprocessor gives low-end workstations the same graphics as high-priced units.

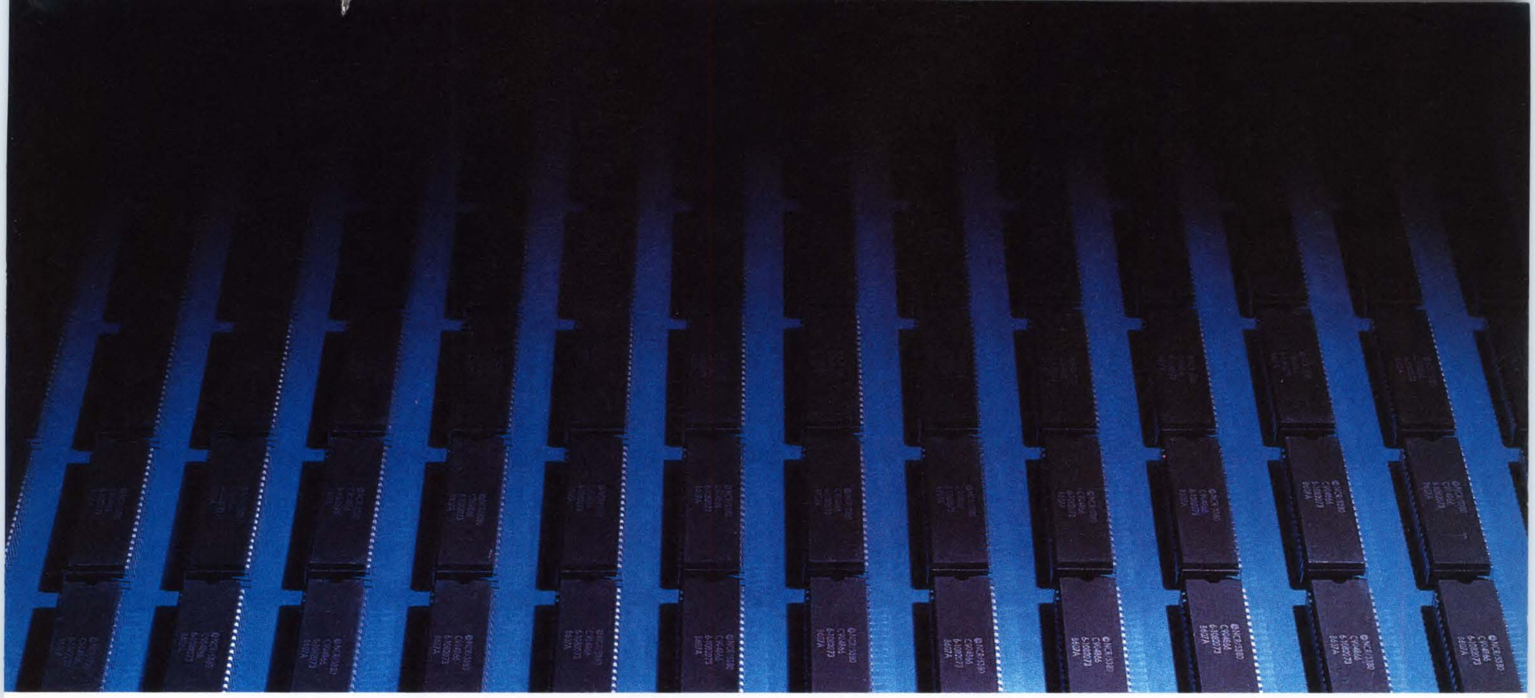
Two processors—one for drawing, the other for displaying images—combine to create windows with variable-depth pixels.



213 Contact wiping, which cleans a connector's mating surfaces, boosts the reliability of zero-insertion-force connectors.

Low-insertion force connectors also use contact wiping, but most have trouble maintaining normal-force levels.





THE MAKINGS OF A SCSI REPUTATION.

Product announcements do not a SCSI chip make. Over the years, NCR has cultivated a SCSI reputation by delivering chips. Not promises.

To date, hundreds of host and peripheral manufacturers have committed designs to our SCSI chips. We like to think that's because NCR expertise played an instrumental role defining the ANSI X3T9.2 standard from the start.

Or maybe more manufacturers design our SCSI single-chip controllers into hosts, printers, tape drives, rigid and optical disks because of the breadth of our product line.

Or perhaps it's a compatibility issue. The fact that NCR SCSI chips assure plug compatibility with hosts and peripherals regardless of manufacturer.

Or a real estate issue. The fact that NCR offers the system integrator single-chip solutions that replace multiple chips or boards.

But probably the biggest reason more companies rely on NCR SCSI chips is availability. We actually have product on the shelves. Here and now.

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- 5380 — Single-ended bus transceivers included—40 pin package; CMOS available
- 5381 — Differential pair implementation —48 pin package
- 5386S — Synchronous superset of 5385E which provides parity through the chip—samples available.

When you need more than SCSI talk, talk to NCR. We're in the shipping business.

For additional information, specifications and catalogs call your local NCR representative, 1-800-525-2252.

QUALITY, SERVICE, SUPPORT. YOU CAN EXPECT IT FROM NCR.

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NCR Microelectronics Division

CIRCLE 5

WEEK 31

Introducing the Am29331—the fastest 16-Bit Interruptible Microprogram Sequencer anywhere. It's the second member of AMD's remarkably fast, ingeniously-designed Am29300 family.

Am29331

Real time needs unreal speed.

The Am29331 has Real Time Interrupt. By building in Test Generation Logic (which no one else does), we cut down on chips and allow for faster system cycle time. Without having to wait for the additional cycle you usually need to accommodate an interrupt, you get faster throughput.

More reasons why the speed stays white hot: Errors can't get too far in the Am29331. They're detected at the source, not at the memory level. It's transparently interruptible at any microinstruction boundary, and Built-in Trap Handling insures speedy re-execution.

The Am29331 16-Bit Interruptible Microprogram Sequencer is just one of AMD's 29300 family. Other members of the family are the Am29332 32-Bit ALU and the Am29334 Four Part Dual Access Register File.

You can use the Am29331 with non-family members if you must. Just make sure the microprocessor you choose can keep up with it.

CIRCLE 6

Design and application seminars are available for this product. Write or call for information.

WEEK 32

There are two things every mother board should have: The 82C54 CMOS Counter Timer and the security of knowing there's a complete second source mother board kit to the Intel 286 PC/AT package. And AMD is proud to hold high the banner for motherhood by announcing both.

82C54

Every mother needs them.

The 82C54 is a general purpose microprocessor peripheral. With low CMOS power, dissipation is only 6% of NMOS parts. The 82C54 is also very fast—it operates at 8 and 10MHz. And naturally, it's a plug-in replacement for Intel's part.

But just as important as the 82C54 CMOS Counter Timer is the fact that you finally have a second source for the 286PC/AT mother board kit. Along with the Counter Timer, the kit contains an 82284 Clock Generator, an 82C288 Bus Controller and an 80286 CPU. But best of all, once you're in production, you don't have to worry about availability, quick delivery and all the other things you worry about when you don't have a second source.

So get up and call AMD: The mother board's little helper.

CIRCLE 7

WEEK 33

If you hate waiting around crowded registers, AMD's new Am29524 Dual 7-Deep Pipeline Register is for you. It's designed for applications that need ground or data pass-through. So now your input data can fly directly to the output or your output can be all zeroes.

Am29524

Direct flights.

The Am29524 has 14, not 16, registers like the Am29525. But it shares many of the same attributes. With the Am29524 you can dip into the data registers in any order, at any time. You could think of it as a random access register. It's programmed by microcode instructions to hold, shift or load data. Its internal ECL technology gives the Am29524 incredible speed (it has a 21ns propagation delay) and the I/O is three-state TTL compatible.

Need to get rid of some excess baggage like a register and bus buffer? The Am29524 does the work of both. And we packed it all in a 28-pin DIP package.

Flying the Am29524 isn't for just everyone. Only the people who want to travel direct.

CIRCLE 8

WEEK 34

AMD wants to put power back where it belongs: In your hands.

We're proud to announce the Am29C821 10-bit CMOS Bus Interface Register. It's a member of the high performance Am29C800 Family: The family that delivers the performance you expect from the bipolar Am29800 Family but with stingy power demands.

Am29C821

Seize power.

The register requires a low power stand-by current of 80 microAmps. But AMD promises that taking power from it won't slow it to molasses. The Am29C821 has a propagation delay of 12ns.

You can also use it in place of, or along with, the Am29800 bipolar counterpart to match your drive and power requirements. Used where an Am29821 provides 48mA drive, the Am29C821 provides 24mA drive.

Get yourself the Am29C821. And then give the leftover power to someone who can really use it. You.

CIRCLE 9

On October 1, 1985, Advanced Micro Devices told the world it would deliver fifty-two new products in one year. A new product every week. Tall order.

So where's seeking the impossible gotten us? Right where we expected. After twenty-six weeks, we're 26 for 26. Batting a cool 1,000. And here's what the world is telling us:

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INT STD 500

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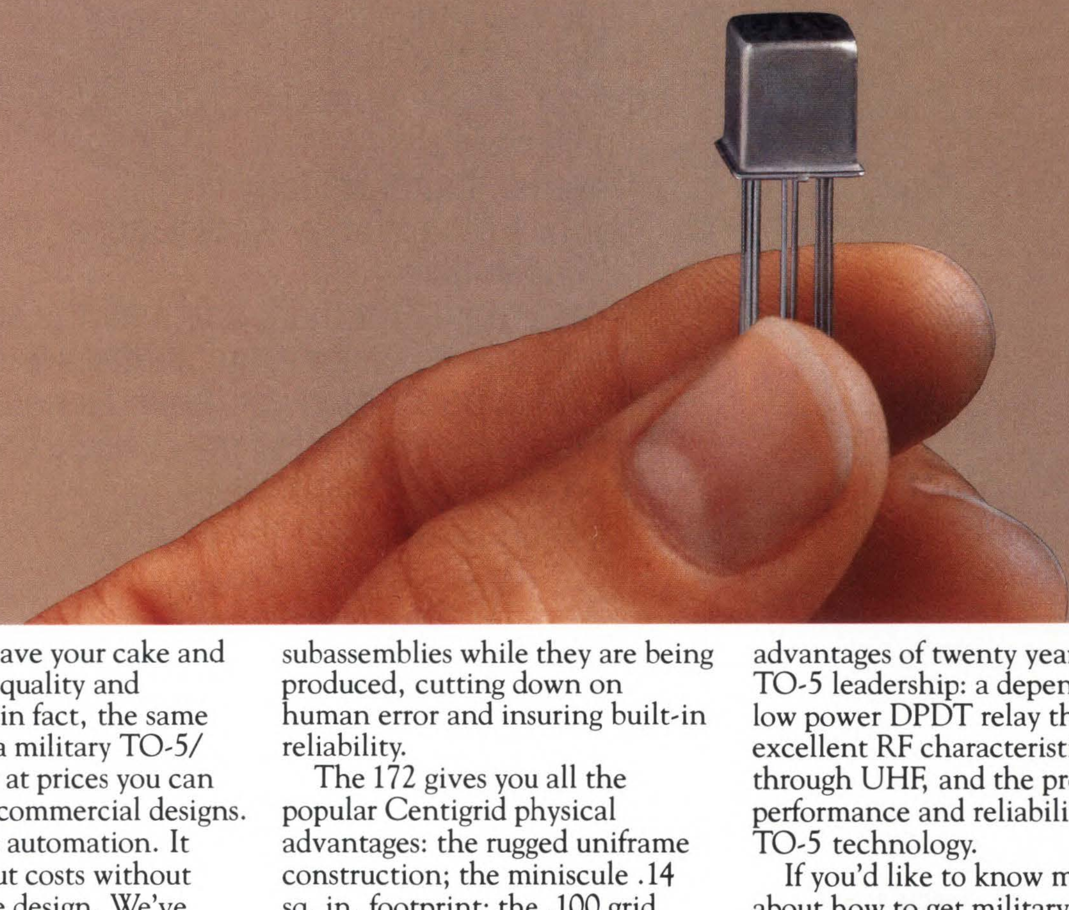
The New 172 Relay We put Centigrid® in civvies to save you money



Now you can have your cake and eat it too! The quality and performance—in fact, the same mechanism as a military TO-5/ Centigrid relay at prices you can afford for your commercial designs.

The secret is automation. It permits us to cut costs without cheapening the design. We've designed and built our unique equipment which not only speeds production, but insures quality. For example, our microprocessor-controlled header assembly system automatically tests the subassemblies while they are being produced, cutting down on human error and insuring built-in reliability.

The 172 gives you all the popular Centigrid physical advantages: the rugged uniframe construction; the miniscule .14 sq. in. footprint; the .100 grid lead spacing for direct pc board plug-in without spreader pad, which retains the low .375 in. total profile.

But perhaps even more important, you get all the technical advantages of twenty years of TO-5 leadership: a dependable, low power DPDT relay that has excellent RF characteristics up through UHF, and the proven performance and reliability of TO-5 technology.

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CIRCLE 11

PC bus for 80386 systems in the works

A uniform 32-bit bus is on the way for engineering workstations and personal computers based on the 80386. Led by **Phoenix Technologies Ltd.** (Norwood, Mass.), an industry committee—including manufacturers of computer systems and add-on peripherals cards—is hard at work on an extension of the IBM PC and PC AT buses. One design under consideration has separate slots for PC, PC XT, and PC AT cards, as well as slots for the high-density memory, analog I/O, and fast graphics processors for 32-bit systems. The committee's aim is to assign identical pinouts to specific functions. Specifications for the new bus architecture are expected by mid-June.

RISC supermini debuts for CAE

Through IEEE 802, 3 and other networking standards, **Hewlett-Packard's new HP 840 superminicomputer** can interface with the company's recently upgraded desktop workstations. A file-cabinet-size version of a machine introduced earlier this year, the TTL-based RISC runs at 4.5 MIPS and operates with a 48-bit virtual address space in a 24-Mbyte main memory. The multiuser Unix system supports up to 60 users and serves as a departmental system for CAE, software engineering, and factory automation. When running a ''Dhrystone,'' the Unix-based variation of the Whetstone benchmark, the computer is slightly more powerful than comparable superminis from Digital Equipment. HP officials hint that later versions of the machine may use 1-μm double-level metal NMOS and that lower-end models may be built with CMOS chips. HP's desktop machine can now be fitted with an optional floating-point processor and, with an 80286/80287 plug-in card, runs MS-DOS. It also interfaces with an external VMEbus. At a base price of $15,600, the Model 320 workstation costs 45% less than similarly configured HP desktop units and moves the venerable computer maker's CAE line closer to recent offerings from Apollo, Sun, and others.

Board paves way for RISC system development

Designing systems and software around a **32-bit RISC microprocessor** from **VLSI Technology Inc.** (Phoenix) is becoming easier thanks to an evaluation board that contains most of the desired support functions. Originally developed exclusively for the Acorn personal computer, the CMOS CPU executes many of its 32-bit instructions in one 125-ns cycle for an average throughput of 4 MIPS. It contains 25 general-purpose 32-bit registers and provides a 26-bit linear address space. Accompanying the chip on the 5¾-by-7¾-in. board are a 16-kbyte bootstrap and self-testing ROM, 1 Mbyte of RAM, two serial ports, and a Centronics-compatible printer port. Also included are an SCSI interface, several timers, and a controller for double-sided, double-density floppy-disk drives. Samples of the board should be available late next month.

Page-printing standard emerges

With the announcement this week of its OmniLaser 2000 series printer, **Texas Instruments Inc.'s** Peripheral Products Division (Temple, Texas) may help establish PostScript as the **de facto page-description language** for next-generation **laser printers.** Developed by **Adobe Systems Inc.** (Palo Alto, Calif.), PostScript contains high-level commands for drawing lines, circles, and polygons in the bit-mapped memory of the printer's controller. First-generation printers merely perform an inefficient screen dump to transfer page descriptions to the printer. TI's bundling of the PostScript package comes after similar moves by Apple Computer and others. In fact, it may provide the impetus for other laser printer makers to rally 'round the language rather than continue writing unique software drivers. TI's OmniLaser 2115 is controlled by a 68000 microprocessor and PostScript commands embedded in 600 kbytes of ROM. It prints 15 pages a minute, double the speed of other units in the $6000 price range.

VMEbus network 16× faster than Ethernet

A network throughput of 20 Mbytes/s is an achievement worth crowing about, especially since it leaves Ethernet rates far behind. **Integrated Solutions Inc.** (San Jose, Calif.) says it reaches that speed by connecting a cluster of workstations through a VMEbus backbone. Using proprietary protocols, the VNetworking system can **transfer data more than 16 times faster than an Ethernet-based configuration** using TCP/IP protocols. Integrated's cluster controller, assembled around a 24-slot VMEbus backplane, contains five boards. Each chassis includes a 68020 CPU card along with up to 14 Mbytes of main memory for one to four 1280-by-1024-pixel terminals. Each terminal in the cluster ties into the VMEbus chassis through standard video cable and works like a "diskless node." No terminal can be more than 100 ft from the chassis, though. For transfers between VME clusters, VNetworking also supports Ethernet or Sun Microsystems' Network File System.

'Superchips' aid floppy controllers

The push to reduce the cost and power consumption of floppy-disk drives and silicon controller chips has produced two **all-in-one drive controllers. Western Digital Corp.** (Newport Beach, Calif.) and **National Semiconductor Corp.** (Santa Clara, Calif.) each have developed CMOS "superchips" that are software-compatible with the popular NEC 765 controller.

The new chips replace dozens of passive and active elements needed with previous 765-based controllers. Western Digital's design features a digital data separator embedded in the controller chip. National Semiconductor's analog expertise helped it include a more error-free analog data separator, and the chip has write-precompensation circuitry. With either product, a designer need only add a few trim-free passive devices to build a controller.

ICs, passives on ceramic substrate

ICs and thick-film resistors can now be integrated with capacitors and other embedded passives on a multilayer ceramic substrate. **Sprague Electric Co.** (Lexington, Mass.) announced a breakthrough that could **reduce the size of small hybrids by more than 50%.** The proprietary process called Multilytics updates the traditional approach used for cofired ceramic devices. Sprague describes it as a "wet stack" approach to layering the ceramic. After the ceramic is cast in thin sheets on an inert carrier, it is dried, printed with the thick-film patterns, and then stacked while the next layer is applied. In the conventional "dry stack" method, the ceramic rests on an organic carrier and sheets are separately laminated before stacking.


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You'll find that same commitment to quality throughout Signetics. Whether we're designing a chip with a half-million bits of memory, meeting delivery schedules, double-checking the accuracy of our paperwork, or getting your name right when you phone.

So, while some companies are bragging about a standard of 500 defects, Signetics is quietly working its way toward zero. And when you put your trust in that kind of commitment, you can't lose.

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EDITORIAL

Linear designers strike out on their own

After living in the shadow of the digital world for a decade or more, the linear circuit is beginning to enjoy spectacular success. Landmark linear developments have been rather sporadic through the years, but recently some "young analog Turks" have burst on the scene, armed with a host of new linear tricks. Rather than rely on advances in semiconductor processing, some of them are resorting to clever circuit arrangements that, for the first time, take advantage of today's high levels of integration. (See our cover story, p. 147, about a smart analog filter from Crystal Semiconductor.)

In fact, "paper" designs long deemed impractical are now coming to practical fruition thanks to the impressive number of transistors, both digital and linear, that can easily fit on one chip or just a few. Pouring off the CAE drawing board are hot new data converters, op amps, filters, and other analog circuits, all sporting performance characteristics that were previously impossible—at least in affordable production quantities.

Why now? The young Turks—companies with unfamiliar names like Crystal, Cypress, Maxim, Micro-linear, and Sierra—have spotted niche market opportunities calling for mixtures of analog and digital circuitry. Not only have they captured some of the brightest talents in analog design, they also have put them to work on proprietary designs that stand little risk of competition.

The results speak for themselves—data converters with unprecedented accuracy, op amps with blazing speed and near-ideal dc performance, telecommunication chips that replace bulky inductors, and IC-like power circuits that can operate directly from the ac line. We see no slowdown in the dizzying pace of introductions, and we promise no slowdown in our efforts to cover every one of the most important new devices.

Stanley Runyon

Stanley Runyon

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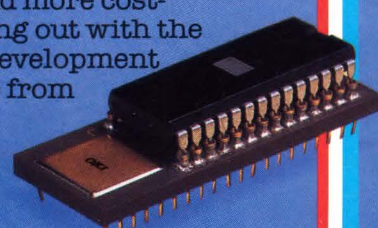
Only CMOS ICE with extended host-computer options: OKI's portable EASE 80C51/59 is totally compatible with any PCDOS, ISIS or CP/M-based system.*

And you can ease your application along even faster and more cost-effectively, by starting out with the EPROM-piggyback development chips now available from OKI for every MCU in our optimized 80C51-59 family.



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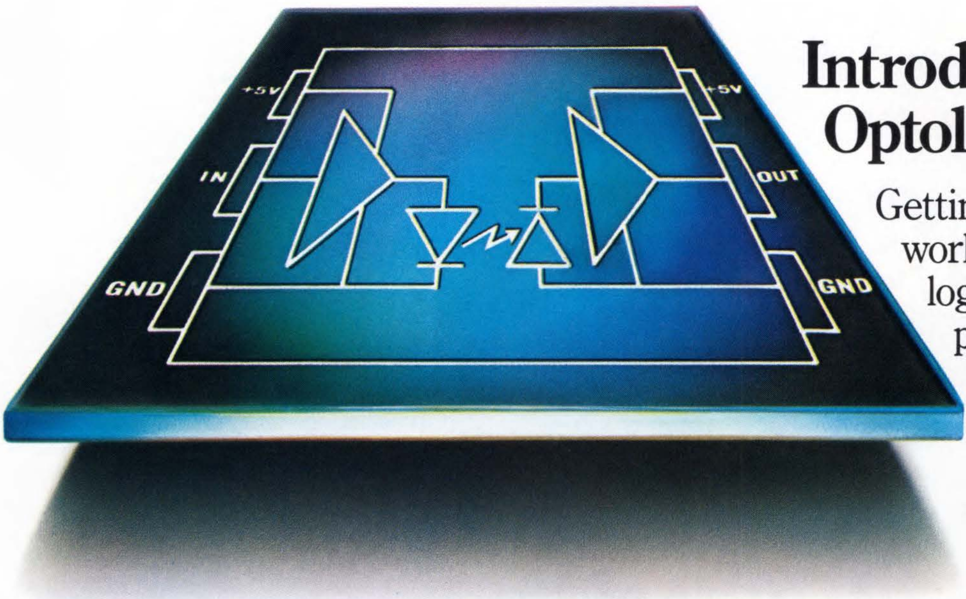

Introducing the Optologic™ Coupler.

Getting lost in the analog world is no fun for the logic designer. In the past you had to consider trade-offs between input current, LED temperature dependence, speed and many other parameters. Many of these trade-offs were figured out by trial and error. It was really time consuming. And a real pain. But now there's good news ahead.

A new concept.

Now you can achieve optoisolator protection without having to understand the analog operation of the optocoupler.

The Optologic coupler is the first general purpose, high speed optoisolator that looks exactly like any common 74-series logic gate at both input and output. This makes it extremely easy to interface between same or different logic families. The innovative use of an input amplifier ensures real LSTTL compatibility and preserves your TTL noise immunity.

The Optologic coupler will find wide use in data communications. In local area networks you can greatly improve noise immunity while utilizing the device's high input impedance in multiple bridged line receivers.

The Optologic coupler is available from these distributors:

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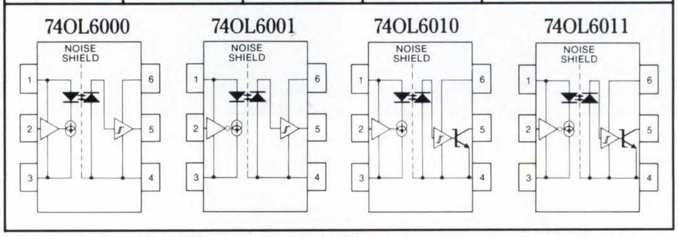
In another common application, AC/DC precision level sensing is possible because of the well-defined input threshold.

And the price is competitive with other high speed optocouplers.

PART NUMBER	LOGIC COMPATIBILITY		LOGIC FUNCTION	OUTPUT CONFIGURATION
	INPUT	OUTPUT		
74OL6000	LSTTL	TTL	BUFFER	TOTEM POLE
74OL6001	LSTTL	TTL	INVERTER	TOTEM POLE
74OL6010	LSTTL	CMOS	BUFFER	OPEN COLLECTOR
74OL6011	LSTTL	CMOS	INVERTER	OPEN COLLECTOR



There are two output versions available: one with totem pole circuit configuration for TTL compatibility, and another with open collector for interface to 4.5 V to 15 V CMOS or power transistors.

High performance and reliability.

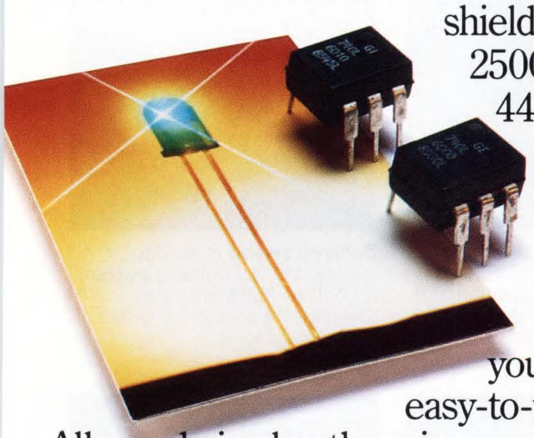
Propagation delay of the Optologic coupler is 60ns and supports datacom to 15 MBaud. The built-in internal noise shield offers 15kV/μs common mode transient rejection.

2500 VAC RMS isolation for one minute corresponds to a 440 VAC working voltage.

MTTF is 1.68 million hours at 90% confidence.

The Optologic coupler is a fool-proof device that provides a level of design integrity and security that the engineer has not had before.

If you hate leaving the digital world every time you want to optically isolate your circuits, design in the easy-to-use Optologic couplers from the LightHouse.



All you do is plug them in.

And bingo.

For samples or information about immediate volume production, contact your local distributor or General Instrument, Optoelectronics Division, 3400 Hillview Avenue, Palo Alto, CA 94304. (415) 493-0400. TWX: 470208.

GENERAL INSTRUMENT
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The LightHouse you can depend on.

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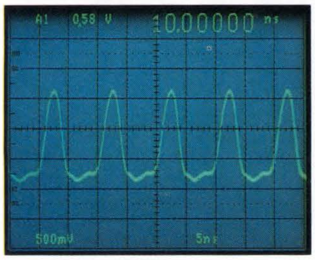
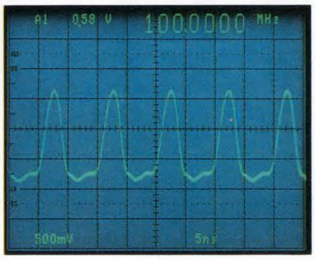
RAE ELECTRONICS

CIRCLE 14

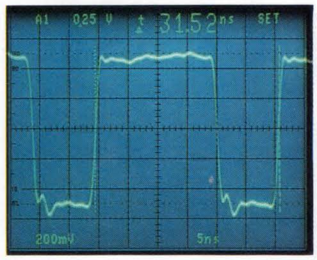
SIXTEEN TOUGH ASSIGNMENTS.



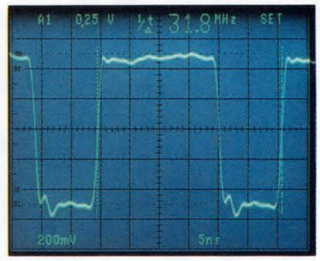
A period measurement is made on a 100 MHz clock using the extended accuracy and resolution of the Counter/Timer/Trigger in the 2465 DVS.



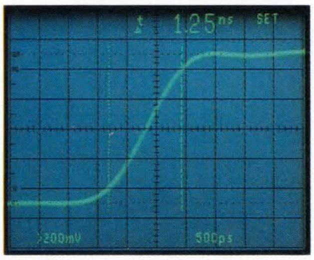
A frequency measurement is made with the same high precision. Simply press two buttons, and the period measurement on the left is converted to frequency.



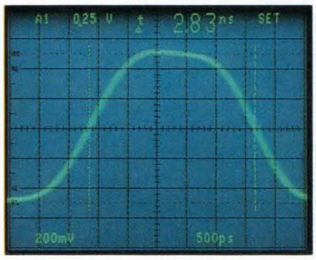
Short time intervals can be measured most accurately with the easy-to-use time cursors. They also make quick work of longer intervals, with 1% accuracy.



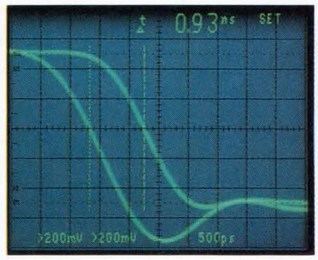
Calculated frequency takes only seconds. The time cursor measurement on the left can be converted to frequency with push-button ease and 1% accuracy.



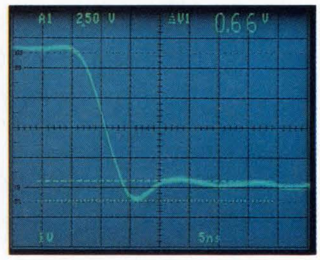
This fast-pulse rise time is nearly that of the scope. The 2465 achieves maximum bandwidth with minimum waveform aberrations. This level of pulse



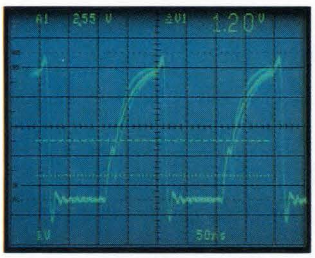
response ensures that **pulse width** and amplitude measurements on fast waveforms (above) truly reflect conditions in a circuit under test.



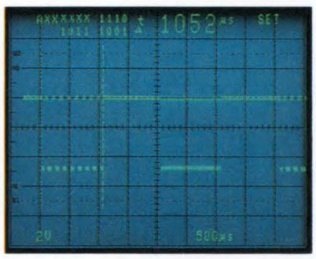
Propagation delay measurement accuracy is assured by built-in propagation delay matching. Delay between Channels 1 and 2 can be corrected to the probe tip.



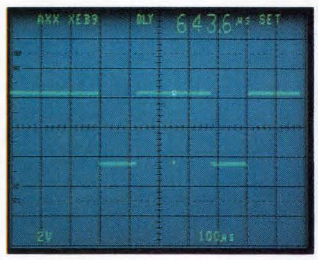
Overshoot and ringing measurement accuracy requires flat response in a probe/oscilloscope system. Tek probes and scopes are designed to work together.



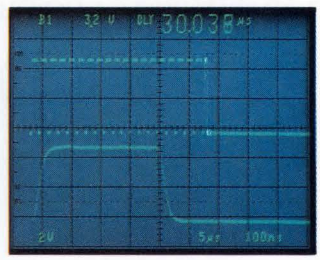
Logic-level violations can be spotted quickly on a TTL waveform (above) with measurement cursors set to define logic-level boundaries.



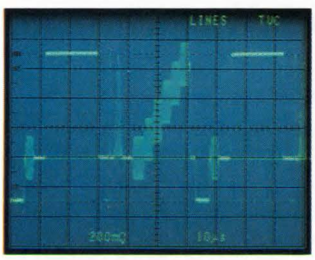
The Word Recognizer (with a binary word) is used to pick out a pulse train in a data stream. The time cursors measure pulse train duration.



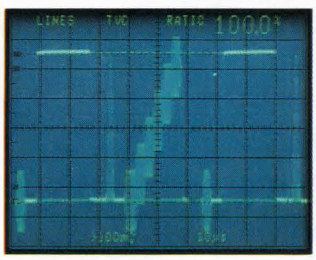
Identify a word position. The Word Recognizer (in HEX) is intensifying a word position and measuring delay relative to a waveform on another line.



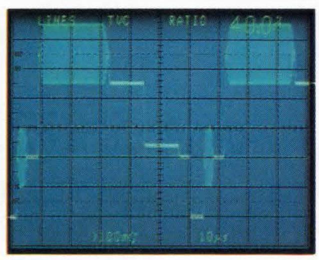
Delayed sweep is used to expand the last pulse in a pulse train. The intensified zone identifies the expanded pulse position.



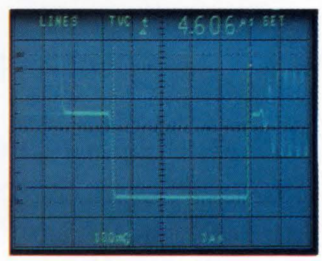
TV line trigger in the 2465 DVS displays a full-field composite test signal. The built-in TV clamp circuit removes hum and tilt on the ac-coupled video.



Calibrate cursors in IRE units with variable attenuation. Blanking level to reference white level is defined as 100 IRE units in NTSC video.



Burst amplitude should be 40 IRE units in NTSC video. The cursors quickly measure other waveform amplitudes. Field triggering checks any line.

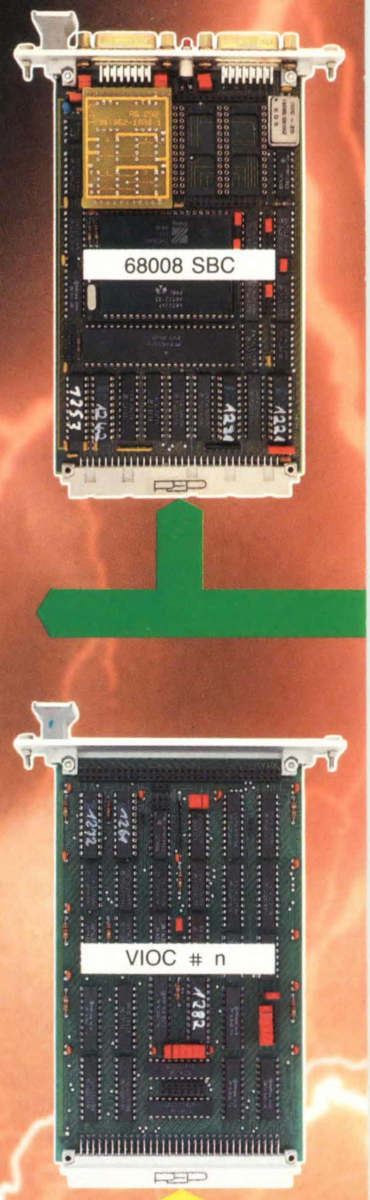


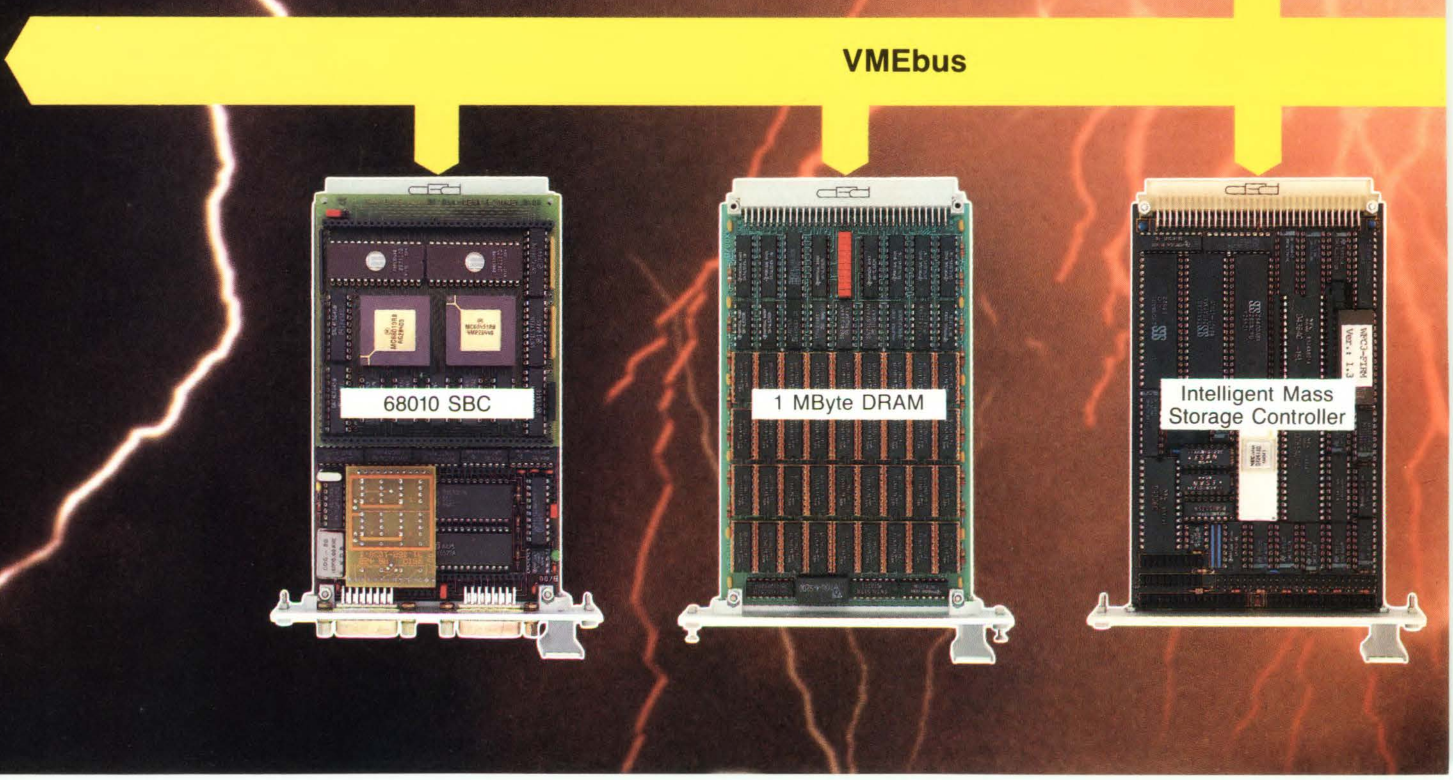
Sync width and blanking are common, easy-to-make timing measurements. Accurate time measurements can be made anywhere in a video system.

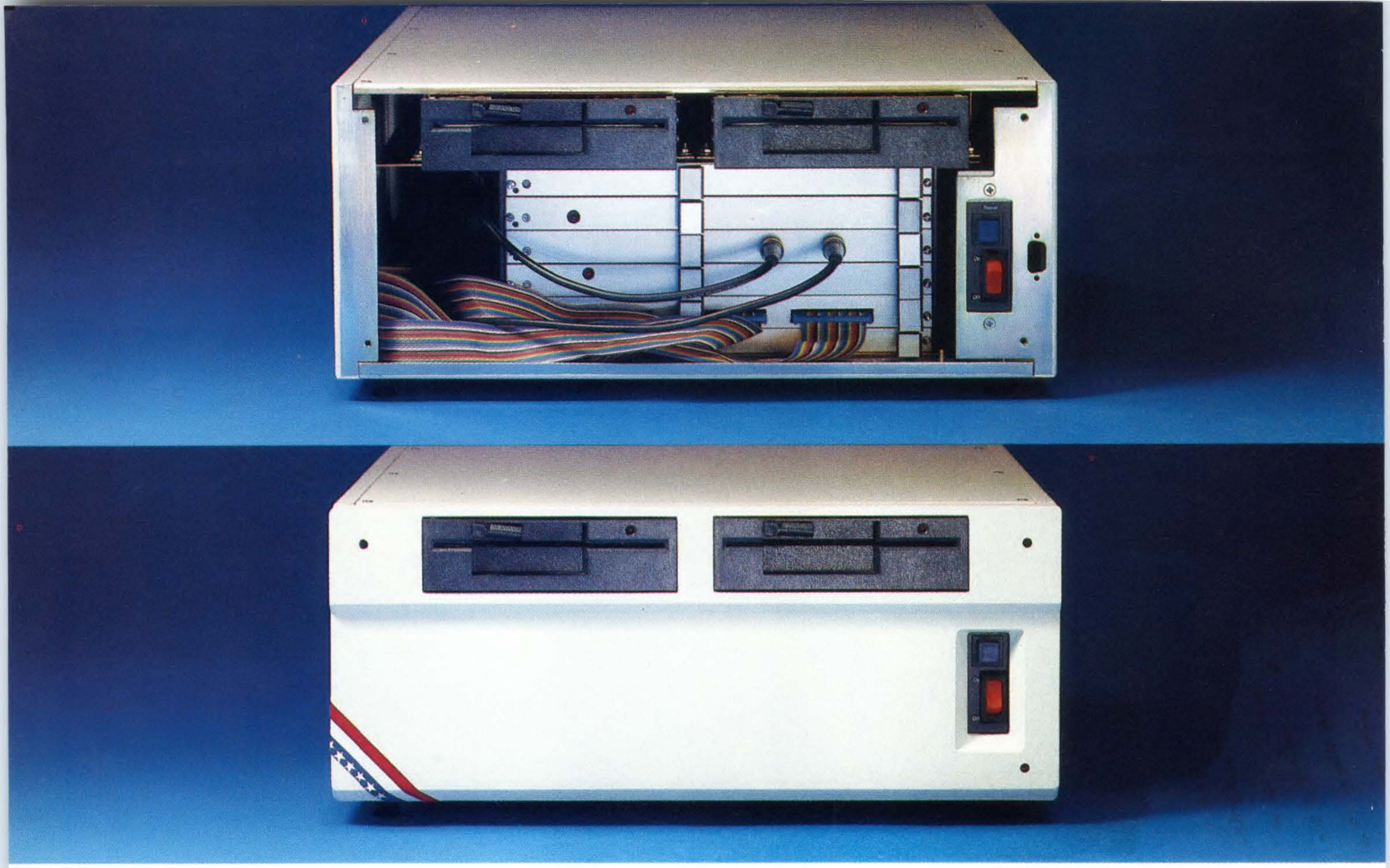
How we tailor VMEbus solutions to your industrial applications

VMEbus and Intelligent I/O Channel...

With the VMEbus finding overwhelming acceptance worldwide, PEP is now enhancing VMEbus versatility with the Intelligent I/O Channel (IIOC). The IIOC provides you with lower cost interface modules typically used in industrial applications. It can also be furnished with its own CPU which can execute tasks locally, offloading the VMEbus master CPU. The IIOC can also be used stand alone. With or without CPU, the IIOC is accessed transparently (as a 64 Kbyte memory mapped space), eliminating the need for complex multiprocessor operating systems. Furthermore, there is no limitation in the number of IIOC's on the VMEbus other than for physical space.







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If you're faced with the problem of putting a VMEbus system together, then look at the American solution to the Eurocard packaging dilemma.

Look first at the location of the VME cards. The front panels are *behind* the enclosure front panel. So you can attach cables to card fronts without having them clutter your bench or dangle down your rack.

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CIRCLE 18

Optical recording yields 6-Gbyte streaming tape

BY STEPHAN OHR

Venlo, The Netherlands—Through optical recording techniques, a 1/2-in. streaming tape may soon pack more than 6 Gbytes in a hand-held cassette—about 30 times the capacity of a comparable magnetic tape. DOCdata NV, a Dutch start-up company, blazes new trails not only with the high-density tape but also with a novel read-write mechanism—an array of 256 semiconductor lasers. The company plans to reveal at least some secrets of its brainchild at The Rothchild Optical Storage For Large Systems Conference, June 3-5 in New York City.

The writing and reading principles for the cartridge closely resemble those of the old punched-tape readers. The 1/2-in.-wide tape stops for approximately 50 μs while the laser array either burns a row of dots into the tape's surface or reads the row back. The tape then advances and stops again, with the laser repeating its actions. The format calls for 10 channels across the tape, with 256 bits in each channel. The laser array reads or writes one channel at a time.

The tape consists of a proprietary ablative (i.e., meltable) material on a 12-μm-thick transparent Mylar substrate. The recording material—neither the composition nor the source of which has been released—is somewhat transparent, so that the light from a reading laser diffuses through it.

The tape is impregnated with ablative dots in the same way that disks are prepared with grooves. Unwritten bits—that is, logic 0s—appear as gray on a light background. Since the cavity formed by ablating the heat-sensitive material deflects the reading laser's light, a logic 1—that is, a written bit—appears darker than the background.

For DOCdata, the challenge did not stop with the recording material. The designers then had to figure out how to prevent the tape from stretching before adding or removing data. A magnetic holding mechanism inside the optical reader-recorder does the trick, working with an iron clamp inside the cartridge. Each time the tape stops, two metal poles in the head are magnetized. The iron clamp flattens the tape against a glass reading-writing window (see the figure), holding it in that spot for 50 μs. During that time, the laser-array head must focus the lens, align the track, and adjust the skew of the head over the tape—using the unwritten bits as a guide.

On the write cycle, the first 250 bits of each channel are written and then rapidly checked. The remaining 6 bits go to the end of the channel, where they serve as a check-sum and a defect map for the channel.

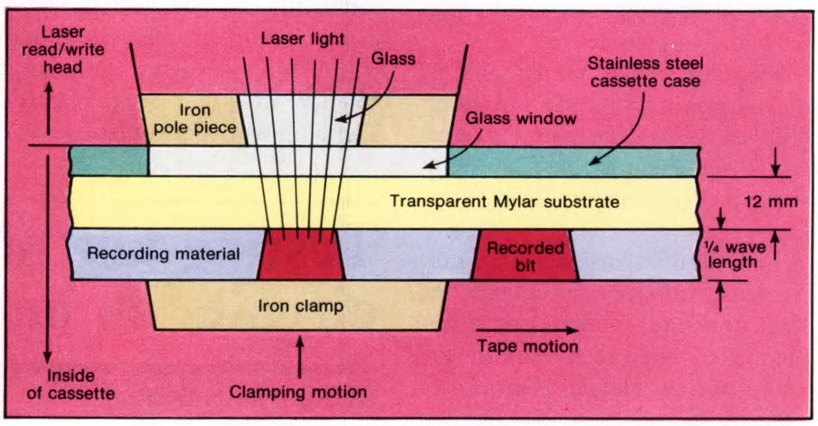
The metal spokes of the tape reels inside the cartridge are magnetically sensitive and are controlled by external magnetic coils. During each rotation, the coils pull the reel through 48 different positions. To avoid particle contamination, the cartridge is sealed inside a 110-by-55-by-15-mm nonmagnetic stainless-steel housing.

PRODUCT IN 1987

The streaming rate, 40 mm/s, yields a 200-kbyte/s reading rate and a 175-kbyte/s writing rate, both compatible with the Pertec standard. DOCdata's technical director, Joseph Beaujean, says the tape-motor controller and the read-write controller each can be implemented on two single-width Eurocards.

In its first incarnation, the tape recorder will occupy a 19-in. rack fitted with a Pertec interface. Eventually, Beaujean hopes to recast the reader-recorder for a 5 1/4-in. form factor. Beaujean projects the assembly with controller will cost less than \$200,000, and each cassette about \$200. A commercial product is not likely until 1987.□

(Newfront section continues on p. 34)



To prevent the tape from stretching during reading and writing, DOCdata sandwiches it between a glass window in the cassette and an iron clamp inside the cassette housing. Before writing or reading, a magnetic flux within the read-write head pulls the clamp flat against the tape. A 20-μW laser burns holes in the recording material through the Mylar substrate.

32-bit GaAs μP hits 200 MIPS at RCA

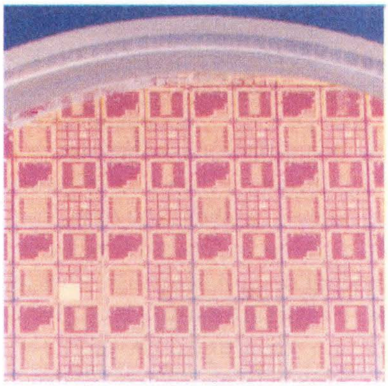
BY CAROLE PATTON

Moorestown, N.J.—A 32-bit gallium arsenide microprocessor owes its 200 MIPS speed to a reduced instruction set strategy. RISC, says the chip's developer, RCA Corp.'s Advanced Technology Laboratories, is crucial to realizing this highly mobile compound's potential for an ultrafast microprocessor—considered next to impossible in the past due to its relatively low on-chip transistor counts compared to silicon. The chip utilizes a reduced-instruction-set strategy and a 400-MHz clock rate to fetch an instruction every 5 ns.

The chip's 400 MHz clock rate enables it to fetch an instruction once every 5 ns, signficantly faster than current μPs. Chip designer Walter Helbig counted on the reduced instruction set to give the CPU its speed. But Helbig is no purist. Unlike an earlier eight-bit GaAs chip design using a 23-instruction set (ELECTRONIC DESIGN, Aug. 8, 1985, p. 27), the new 32-bit chip requires an instruction set about twice the size of its predecessor.

This time, Helbig has put some of the routines in microcode, and either dropped the op code instructions or simplified them by making them serve dual (or even multiple) functions.

For example, instead of a Subtract instruction, a register takes the first operand—normal or complemented—and then performs an addition. Says Helbig, "Obviously, taking a second operand's complement and then adding will result in a subtraction." But the same function in a field—taking the second operand's complement—turns an exclusive OR into an OR NOT.



RCA's 32-bit GaAs μP uses enhancement- and depletion-mode transistors connected by two levels of metal. The above wafer with several μPs was produced by Triquint Semiconductor Inc. (Beaverton, Ore.).

"In encoding the instructions, we are setting up fields that mean certain things," Helbig says, adding, "It allows us more options."

The chip uses enhancement- and depletion-mode transistors connected by two levels of metal. It is to be manufactured by Triquint Semiconductor Inc. (Beaverton, Ore.), using custom circuitry as well as standard-cell blocks consuming 450 mW altogether (see the figure). The chip will operate from a 2-V power supply. Helbig anticipates that the completed 32-bit design will require more than the 84 pins of the 8-bit version.

Where there seems to be enough space, silicon designers often seek higher speeds by moving computing functions into the hardware. But to build a GaAs CPU that could hit the desired 200 MIPS, RCA turned to Purdue University (West Lafayette, Ind.) for a specialized software compiler and a strategy that aggressively transplants hardware functions into software. But Purdue's Veljko Milutinovic admits, "GaAs chips will probably never match the transistor-count potential of silicon."

Another basic change in the design lies in the on-board cache memory. With the speeds available through GaAs chips, going off-chip to access external memory exacts an enormous penalty in the system's throughput. Pipelined operation avoids the delay, Milutinovic says, by overlapping instruction fetches and execution.

The on-chip cache is divided between instructions and data to set up "static prefetching," another processing shortcut. A compiler predicts the blocks of data most likely to be needed during processing and moves them into the cache ahead of time.

To correct defects in the cache's memory area, the block has a fault-tolerance validation bit—an idea borrowed from the University of California at Berkeley.□

Testing and simulating circuits on one system

BY STEPHAN OHR

Ghent, Belgium—One of the biggest obstacles in moving a board-level circuit from design to production is the test program. Even with CAE, a test engineer must convert the simulator data into real-world test parameters for automated test equipment.

The solution is obvious: Create a simulator that also behaves like a tester, and then use parametric data as the basis for simulation. The data provides realistic evaluation of the circuit while doubling as an ATE driver. Taking such an approach is a start-up company with close ties to Siemens, Expert Software Systems NV, known as E2S.

The simulator-tester just announced by E2S digests user-supplied stimulus patterns, high-level descriptions of the circuit, and parts libraries and models, as well as the particular equipment capabilities of the ATE system. The simulator gives the most realistic picture of a logic circuit short of actually constructing it.

E2S marketing director Joost Cardeon contends that the simulator will be a successor to the popular Hilo package from GenRad Inc. (Concord, Mass.). Like Hilo, the E2S simulator is event-driven—it works under test conditions specified by the user, such as setup and hold times, to perform its checks. The unit also detects spikes and race conditions. Unlike Hilo, the E2S simulator uses parametric data from the design and test data base in its test routines.

To successfully compete against Hilo and other packages, E2S must first adapt its line to more popular workstations. Currently it runs on a bit-slice processor system from ICL (London) developed by the now defunct Perq Computer Systems Inc. and currently distributed in the U.S. by Access Systems Corp. (Pittsburgh). Cardeon says the company is feverishly working on ports to Apollo, Digital Equipment, and Sun workstations.

E2S's simulator is actually part of a family of CAE tools. The philosophical approach is a hierarchical, top-down approach to system design. Unlike bottom-up design systems—schematic building blocks are entered transistor by transistor or gate by gate—the E2S's hardware development system enters information in the form of a high-level language.

The system description is split into two components: One is a description of the stimulus and the response (the inputs and outputs and the timing constraints); the other is a functional description of the circuit likely to provide the desired response patterns. A user specifies them in a Pascal-like high-level language and compiles them to simulator code descriptions.

The functional description is implemented in the highly structured functional description language. Stimulus patterns are entered in what E2S calls the external and memory description language.

To collect a usable test pattern, an internal compiler works on both the user-supplied inputs and outputs and timing constraints, as well as on the ATE data base. When the simulation is complete, the user can display them graphically on the screen as logic waveforms.

Based on the resulting waveforms and state listings, the hardware designer may revise the functional description of the design or the stimulus pattern, until the desired behavior requirements are met. This approach eliminates the need for fault simulation, Cardeon points out. The simulation specifies all the operations that were exercised.

The schematic editor is invoked only in the refinement stages as a means of defining the inner logic of the system. Further library resources not only provide circuit blocks or components, but also online design rule checks. The waveforms supplied by the simulator show the behavior of the system as a whole, along with signal lines associated with the inner logic.

In addition to circuit net lists, the simulator and tool modules produce test vectors formulated in Atlas, a standardized test-system language that originated under U.S. Department of Defense sponsorship. It is used at Siemens and ITT and elsewhere in Europe, owing to the Defense Department's influence in NATO.□

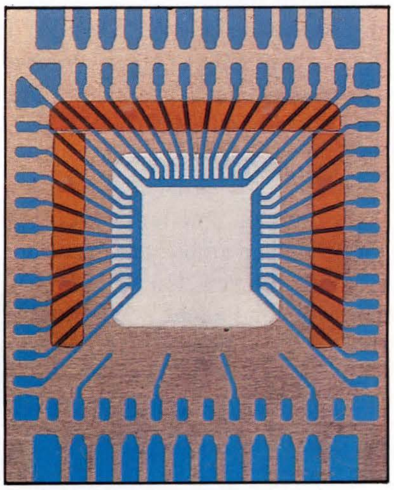
Surface-mounted packages move to higher power

BY MITCH BEEDIE

Agrate, Italy—Within Europe and the U.S. at least, the shakeout in surface-mounted packages for ICs appears to be over: Small outline (SO) packages are firmly established for chips needing up to 28 or so leads, and plastic leadless chip carriers (PLCCs) take over for higher pin counts.

However, plastic-encapsulated devices have difficulty handling dissipation above 1 W, while SO packages can handle only about 300 mW. As more intelligent power and mixed bipolar-MOS devices are incorporated into systems, the need for higher dissipation packages has become critical.

Aimed at eliminating the heat



SGS-Ates' "33 + 11" medium-power package can dissipate 2 W, twice the level of other PLCCs. It carries away chip heat through the bottom 11 leads.

problem is a group of surface-mounted packages developed by SGS-Ates Componenti Elettronici SpA. The medium-power SO and PLCC packages dissipate up to 2 W, and a new one boosts surface-mounted power dissipation to 10 W.

A CLEVER TWIST

Externally, the new PLCC and SO packages are identical. As a result, SGS can use the same manufacturing equipment for the new devices as for standard PLCCs and SO ICs. Similarly, customers can stick with their existing pick-and-place equipment.

Boasting perhaps the broadest appeal is a medium-power PLCC that uses part of its lead frame to conduct heat. A 44-pin version, for example, dedicates 33 leads to signals and the other 11 (along one side) to conducting heat into the pc board (see the figure). One end of each of the 11 leads is soldered to the board in the normal way, while other end is glued to the die bottom.

The scheme reduces the junction-to-case thermal resistance, Θ_{j-c}, to 12°C/W. When the package is mounted on a copper-clad Invar board, that figure yields a junction-to-ambient thermal resistance, Θ_{j-a}, of around 35°C/W. Standard PLCCs have a Θ_{j-a} of 60°C/W for a 44-pin package; SO packages are even worse, about 200°C/W.

SPREAD THE HEAT

Assuming a chip temperature of 130°C and an ambient temperature of 70°C, the new "33+11" PLCC can withstand about 2 W—double that of a standard PLCC. Meanwhile, SGS is evaluating a similar arrangement for SO ICs: a 16+8 package that can dissipate up to 2 W and that exhibits a Θ_{j-c} of 10°C/W.

While these types of packages work well to about 2 W, more has to be done above that figure. For its part, SGS is developing a Micro-power package, which has an integral copper heat spreader that reduces Θ_{j-c} to 5°C/W. Since this low value can practically be ignored, the main limiting factor becomes the pc board.

The package has leads on only three sides, with 3 to 17 pins on each. The same size as an SO-20, it is a standard 300 mm wide and has gull-wing leads. The package attaches to a board with a clip or conductive glue, which effectively places the chip in direct contact with the board for maximum transfer. Because one side of the package is free of leads, the contact area can be inspected easily.

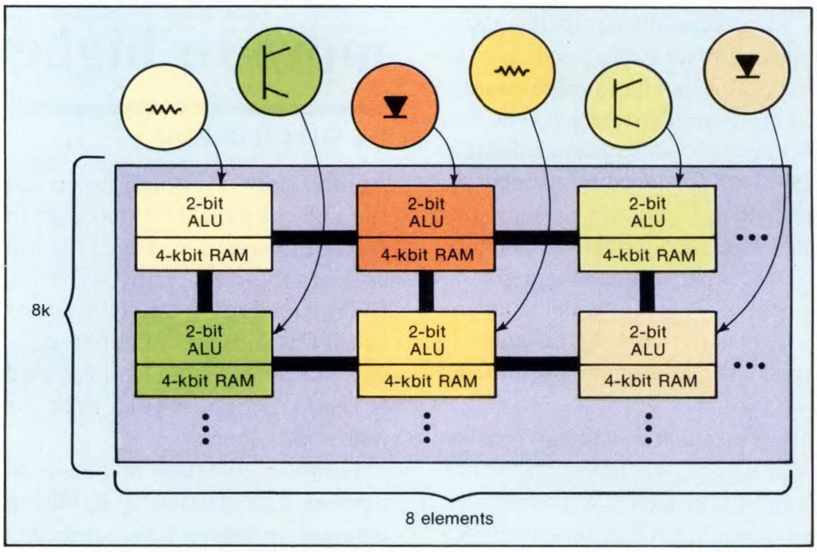
Increasingly, special pc boards are being used with surface-mounted packages. Those with copper-clad Invar cores are considered to be the best heat conductors. They can incorporate copper pillars and plated through-holes to push power up to 3 or even 5 W/in.^{2}. Consequently, power dissipation can reach 10 W.□

Adaptable computer has all elements in parallel

BY CURTIS PANASUK

Cambridge, Mass.—It is the ultimate in parallel processing: a chameleonlike computer that adapts itself to the job at hand. Thinking Machine Corp.'s Connection Machine is able to reconfigure its 65,536 parallel processor elements to fit the task before it, rather than needing the task stated in a form that suits the computer.

The machine's adaptability enables it to do in 1 hour a chip simulation that would take 10 hours on a conventional mainframe. And its landmark features are not so much its 1000 MIPS of processing



To simulate a 17-component amplifier, a very small transistor simulation program is loaded into each ALU assigned to represent a transistor in the circuit. The same is done for the resistors and diodes. Then all 65,536 ALUs run simultaneously, calculating what their corresponding component currents are and passing those results to the other ALUs.

THE BEST.

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125 MHz BW; 100 MS/s ADCs; 5 GS/s Interleaved Sampling; 128 k Waveform Memory; ± 1% Accuracy; Summation and Continuous Averaging; Arithmetic Processing; Fully Programmable.

PROGRAMMABILITY. All settings of the 9400 Digital Oscilloscope are programmable; you can operate the instrument in unattended areas or as a computer-aided testing station. You can redefine the softkeys and send messages to the display, in order to step inexperienced operators through complex test procedures. And even without a computer you can store and quickly reproduce up to *eight front-panel setups,* for your most common measurements.

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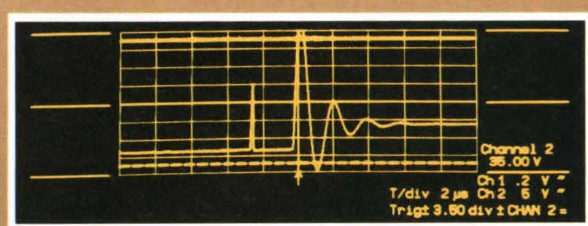

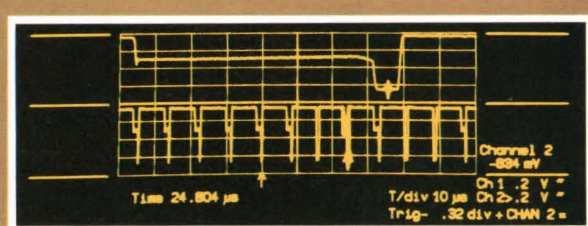

Top: Acquisition Parameters listing enables the 9400 user to precisely set and check front panel settings, all of which can be remotely controlled.

Middle: Window mode trigger set at ± 3,5 divs from center grid captures switching transient. 50% pre-trigger shows contact bounce prior to trigger moment.

Below: Crosshair marker, acting as a precise timer and DVM, gives time from trigger (arrow) and absolute voltage.

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CIRCLE 19 FOR INFORMATION
CIRCLE 20 FOR DEMONSTRATION

power or its internal data rate of 250 million 32-bit messages a second. What really boggles the mind are the 65, 536 processor elements that work simultaneously on a project's various segments—such as the simulation of a complex circuit design or the analysis of fluid dynamics.

CPU WITH BRAINS

"We found a new way to build a computer," says company cofounder Danny Hillis. "We built a computer that can fit the problems it will be asked to solve." The concept is based, he says, on the operation of the human brain (see "Common-sense Processing," below).

To understand the Hillis concept, first consider a circuit simulation of an amplifier with 17 components. In a traditional von Neumann architecture, the components' currents are calculated one by one through the single processor. When the calculations for one component are finished, the processor saves the results and moves on to the next, with 20 such iterative passes representing a single time cycle.

The Connection Machine, in contrast, calculates each component's current simultaneously on a separate processor, speeding the operation enormously. One processing element is assigned to simulate each of the 17 components (see the figure).

The processing-element approach also simplifies program writing. Once a program has been written to simulate a transistor, it is copied into every processing element that is assigned to represent a transistor. After corresponding programs have been written to represent a diode and a resistor, the amplifier simulation can run. All component currents are calculated simultaneously, and data packets carry equivalents to the currents between the processing elements.

Each element is actually an ALU, backed up by up to 4 kbits of 90-ns static RAM on separate

Common-sense processing

For nearly 20 years Danny Hillis dreamed of building a computer that could think like a human being. Inspired by the anthropomorphism of sci-fi computers, Hillis worked toward that goal during graduate studies at the Massachusetts Institute of Technology's artificial intelligence laboratory.

But he was constantly frustrated by mainframe computers that could not run his "common-sense reasoning" software. Noticing that most big problems could be divided into thousands of little ones, Hillis figured that he could apply a very small computing element to each small problem.

"I knew I had to be on the right track, because this is how the most powerful computer, the human brain, is structured," Hillis recalls. "The brain seems to derive its incredible power from computing elements called neurons that process with cycle times of only 1 ms." But even though that is mediocre compared with present-day technology—gate arrays have cycle times measured in microseconds—the 65,536 elements in Hillis's machine are well beyond existing CPUs but no match for the human brain's billions of processors.

After spending three years working on the machine's architecture, and especially the system bus, Hillis's doctoral thesis became the basis of a book, *The Connection Machine*, published last year by MIT Press.

Hillis wanted to start a company that could build a computer based on his architecture. But 10 years passed before others in the New England high-technology area heard about his work and introduced him to some venture capitalists. Finally, in 1983, the company was born. —*C. Panasuk*

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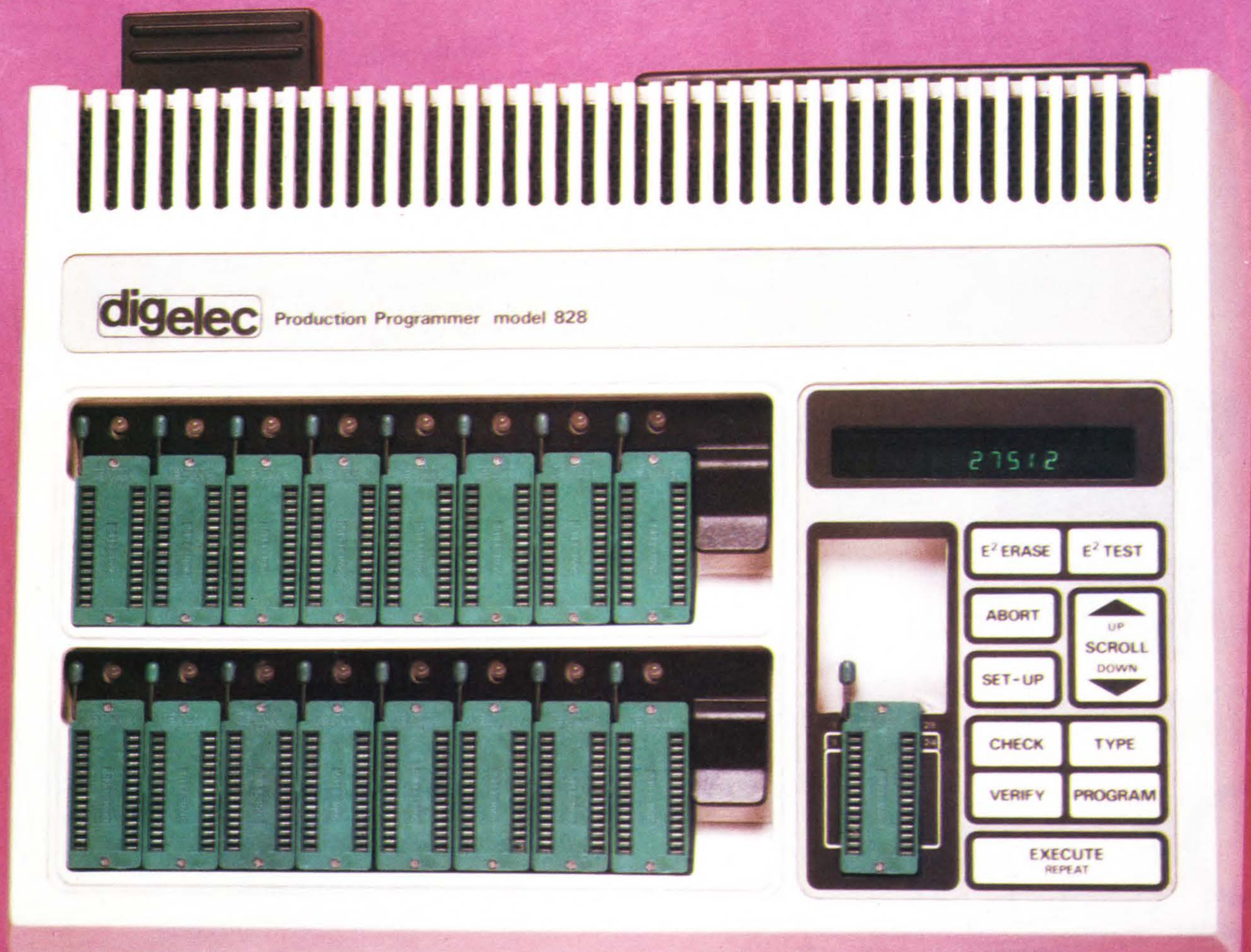

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CIRCLE 21 FOR INFORMATION

CIRCLE 22 FOR DEMONSTRATION

INDUSTRY WATCH

PC AT workstations undergoing big changes in power and price

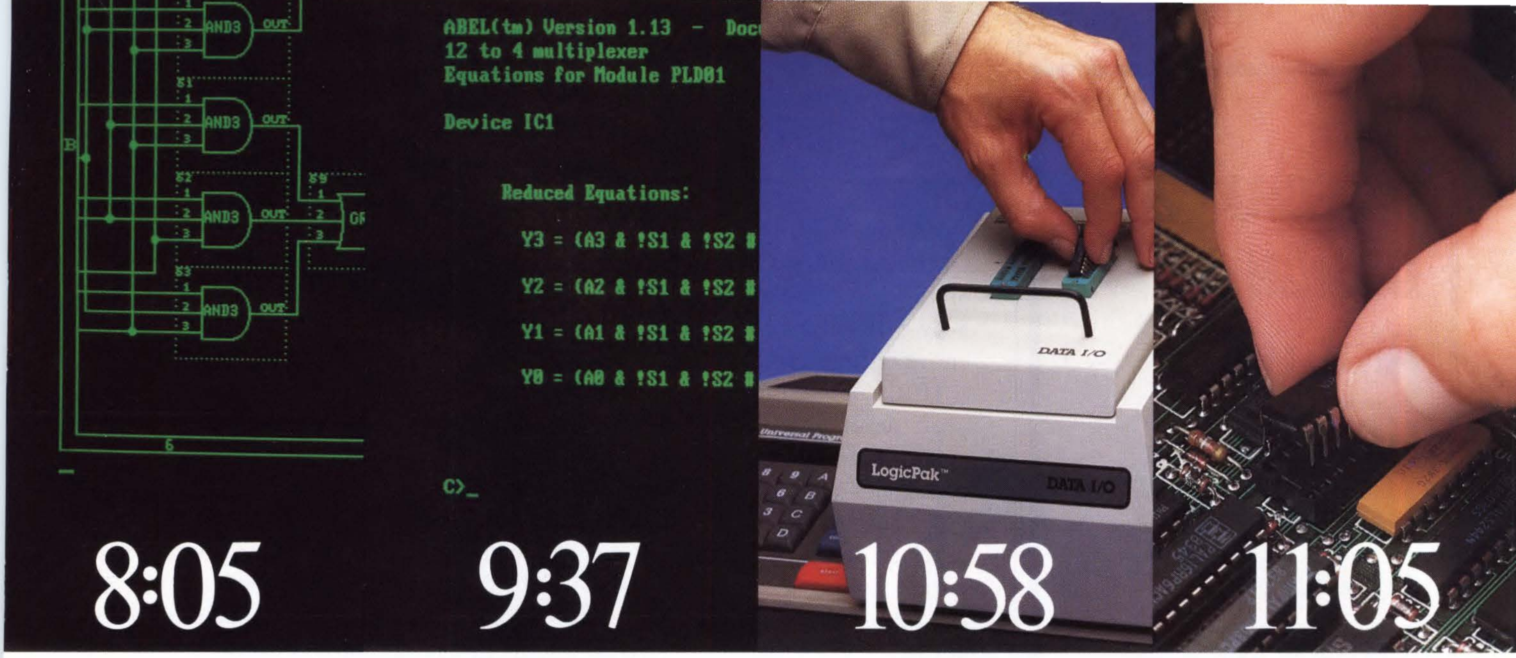
If you're hungry for more power and memory in a low-end engineering workstation, nourishment is on the way. For the past two years, the 16-bit IBM PC AT has emerged as a cost-effective tool for many basic CAE tasks. But as early as this summer, you'll have a greater choice: Stay with the 80286-based PC AT or move up to its 32-bit successor. The new system, which will be based on the 80386, will pack a megabyte of RAM, which can be upped to 4 Mbytes; a 30-Mbyte hard disk; and a 1.2-Mbyte diskette.

The exact status of 80386-based machines is difficult to determine, since most companies are understandably reluctant to comment. But from what I can gather, lots of vendors have received small quantities of 80386s from Intel and are actively developing their new systems.

Take San Jose–based Convergent Technologies, which is working on three 386-based systems. The first will be two to three times faster than the current 286 machines, packing 3 to 4 MIPS in a box priced at nearly $5000, without hard or floppy drives. After acknowledging Convergent's projects, CPU development manager Robert Schopmeyer said, "Low-end desktop systems haven't been able to run heavy computational programs quickly enough." But the virtual-mode feature of the 80386-based systems should put those concerns to rest: It will give users access to two different operating systems. Unix System V can handle complex engineering jobs while MS-DOS runs existing software.

Despite the wallop of the 386-based systems, I have no doubt that the 286-based PC AT will be around for a long time, with its prices dropping and its performance rising regularly. In just the past six weeks, the price of IBM's machine, as well as compatible units, has plunged 20% to 33%. Now you can get a 6-MHz IBM machine with 20 Mbytes of hard-disk storage and a 1.2-Mbyte diskette for $4895—down $900. Similar action comes from manufacturers of similar units, including Compaq, Zenith, Hewlett-Packard, ITT, and Cordata. Compaq, for instance, is selling its 286-based desktop unit for as little as $4000. In addition to pricing changes, some PC AT suppliers are upgrading their 6-MHz systems to 8 MHz or raising hard-disk capacity to about 30 Mbytes.

Martin Gold



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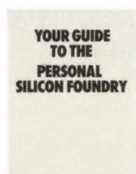

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CIRCLE 24

chips. Sixteen ALUs fit on a 2-μm CMOS gate-array chip, with 4096 of the chips packed into a 5-by-5-by-5-ft cabinet that holds the entire battery of 65,536 elements.

Hillis spent more than three years developing the communication technology that knits the processors together. The concept governing the 250 million messages a second is the subject of a patent application, so Hillis will not discuss it in detail, except to say that the average message is 32 bits long.

Because of the varying overhead demands, all of the processors may not be available for every problem. For instance, in an analog simulation the 65,536 processors might handle only 20,000 transistor chips, because the remaining processors would be needed for outputs and internal wire delays. On the other hand, since less overhead would be needed for a logic chip, the full configuration could simulate close to 65, 536 gates.

Application programs that use conventional programming languages must first be run on a front-end processor such as the Lisp machine from Symbolics or a high-end VAX from DEC.

Thinking Machines was able to sidestep the difficult problem of developing an artificial intelligence–level compiler to apportion the workload. Instead, the large number of processors makes it possible for a standard compiler to divide and spread an application program across the elements, as in the circuit simulation example.

Existing application programs do have to be modified for the computer. For instance, Do loops must be removed, as all steps occur as one. In addition, data structures must be created to define what data is to be shared among which processors. Thinking Machines has modified C and Lisp so that the programmer can replicate application programs automatically before running them on the Connection machine. □

Are LCDs winning the flat-panel display race?

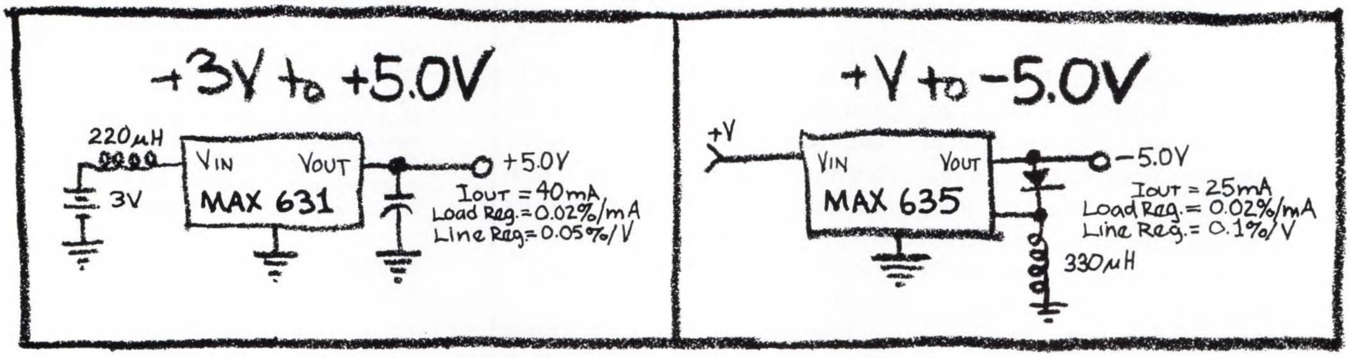
BY DAVE BURSKY

San Diego—The quest for a flat color display that rivals the resolution of today's CRTs is in its infancy. At the Society for Information Display's recent conference, speakers noted that it will be several years before the color CRT is seriously threatened as a mainstream display —even though color liquid-crystal panels have appeared in a few small consumer products and prototype color electroluminescent and plasma displays have been demonstrated.

Lawrence Tannas Jr., a consultant at Rockwell International Corp. (Anaheim, Calif.), said the size of experimental color flat-panel displays seems to be doubling every couple of years. That rate of progress should continue through the early 1990s until sizes of production models are competitive with those of large CRTs, he says.

Tannas predicts that for displays with a diagonal dimension of up to 12 in., twisted-nematic liquid crystal panels have the best chance of capturing the designer's fancy. However, the readability of LCDs is a big problem—some OEMs have resorted to backlighting. Data General and NEC recently offered emissive EL panels as an option for their laptop computers. The issue of

ANY VOLTAGE IN. ANY VOLTAGE OUT.



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MAX632	2.0V to 12.6V	+12V	Only 2 external components	$3.50
MAX633	2.0V to 15.6V	+15V	Only 2 external components	$3.50
MAX641	2.0V to 5.6V	+5V	10 Watts w/external MOSFET	$3.72
MAX642	2.0V to 12.6V	+12V	10 Watts w/external MOSFET	$3.72
MAX643	2.0V to 15.6V	+15V	10 Watts w/external MOSFET	$3.72
MAX4193	2.4V to 16.5V	Vout > Vin	Programmable output	$2.15
INVERTING CONVERTERS				
MAX634	3.0V to 16.5V	up to −20V	Programmable O/P, precision ref.	$2.90
MAX635	3.0V to 16.5V	−5V	Only 3 external components	$3.50
MAX636	3.0V to 16.5V	−12V	Only 3 external components	$3.50
MAX637	3.0V to 16.5V	−15V	Only 3 external-components	$3.50
MAX4391	4.0V to 16.5V	up to −20V	Programmable output	$2.70
STEP DOWN CONVERTERS				
MAX638	3.0V to 16.5V	Vout < Vin	Only 3 external components	$3.50

MAXIM

Maxim's family of DC-DC converters was developed under the direction of Maxim co-founder and VP of R&D, Dave Fullagar.

At Fairchild, back when giants walked the earth, Dave helped pioneer the world's first linear ICs. And he personally designed the most successful op amp ever built, the µA741.

What's more, as Intersil's first engineering director, he was responsible for the emergence of CMOS as the standard technology for analog ICs.

Add to all that the fact that Dave is 6'3." And I guess you could say that Dave is a giant in the annals of analog IC technology.

Whatever an annal is.

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CIRCLE 25

which type of display is best suited to what application prompted plenty of discussion at the session.

For active-matrix color LCDs, Tannas pointed to the largest experimental panel yet developed—a 9-in. LCD containing about 300,000 pixels and developed by Toshiba Ltd. (Kawasaki, Japan). That pixel count is a long way from the 1 million pixels of top-of-the-line color CRTs, but it does approach the resolution of the displays used in hundreds of thousands of personal computers.

Donald Pinsky, technical director of display technology at Interstate Electronics Inc. (Anaheim, Calif.), points to another development equally impressive—a 5¹/₄-in. panel

EL panels were praised by military officials for tactical uses where other displays are inappropriate.

with 211,200 pixels, in a 480 by 440 arrangement. Epson Ltd. (Fujimi, Japan) uses thin-film polysilicon transistors, fabricated on the back of the panel, to drive the pixels.

Pinsky did note an important drawback: The Epson system lacks a gray scale, which make shading impossible and so eliminates true image reproduction. However, on any panel with a gray scale, resolution is sacrificed to obtain the shading.

INHERENTLY BRIGHT

Military officials although enthusiastic about color displays, said they do not anticipate a strong demand for them in general, but praised electroluminescent panels for their inherently brighter and more reliable images. Elliott Schlam, director of the integrated devices, processing and displays division of the U.S. Army Labcom operation at Fort Monmouth, N.J., calls EL displays one of the most promising approaches for tactical systems, since reflective-type flat panels are inappropriate during combat.

Indeed, EL prototypes have so far proved that flat-panel displays are no immediate threat to color CRTs. The first color EL display, a 6-in. unit developed by Planar Systems Inc. (Beaverton, Ore.), still lacks the brightness needed to be read in high ambient light. Planar showed its display at the SID conference (ELECTRONIC DESIGN, April 17, p. 49).

The red and green phosphor Planar panel lacks a blue, which prevents it from providing the full range of colors. However, other companies at the show reported success with blue phosphors.

As for plasma panels, the cost remains high. This technology was demonstrated as early as 1979, but the sharply higher cost of manufacturing and the drive circuitry have kept it in the laboratory, according to Larry Weber, research associate professor at the University of Illinois at Urbana-Champaign. Plasma panels that combine color with gray-scale capability are possible, though. Weber predicts that they may be only a few years away, thanks to advances in glass processing and development of complex high-voltage driver chips.

In spite of the tremendous strides in flat-panel technologies, the CRT should remain dominant through the end of this century, according to Joseph Castellano, president of Stanford Resources (San Jose, Calif.).

He pointed out that flat CRTs using side-beam projection have already been developed. While their vacuum tubes may limit the size of these units, color is possible, he said. Minor details, such as beam-deflection control, a small yoke, and more tightly integrated circuitry, are all that is needed for a commercial flat CRT.□

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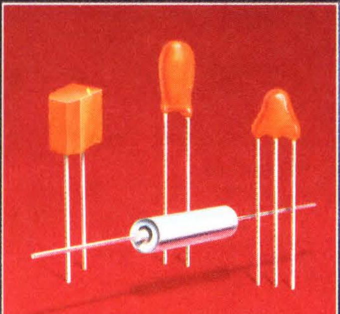

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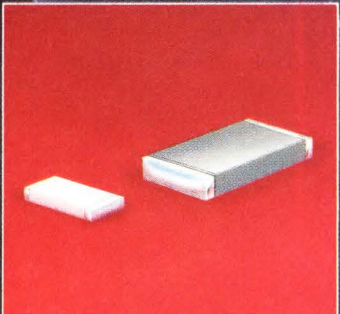

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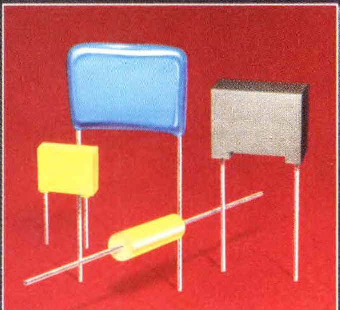

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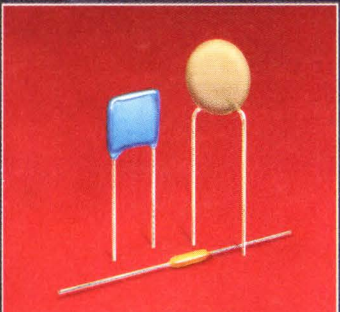

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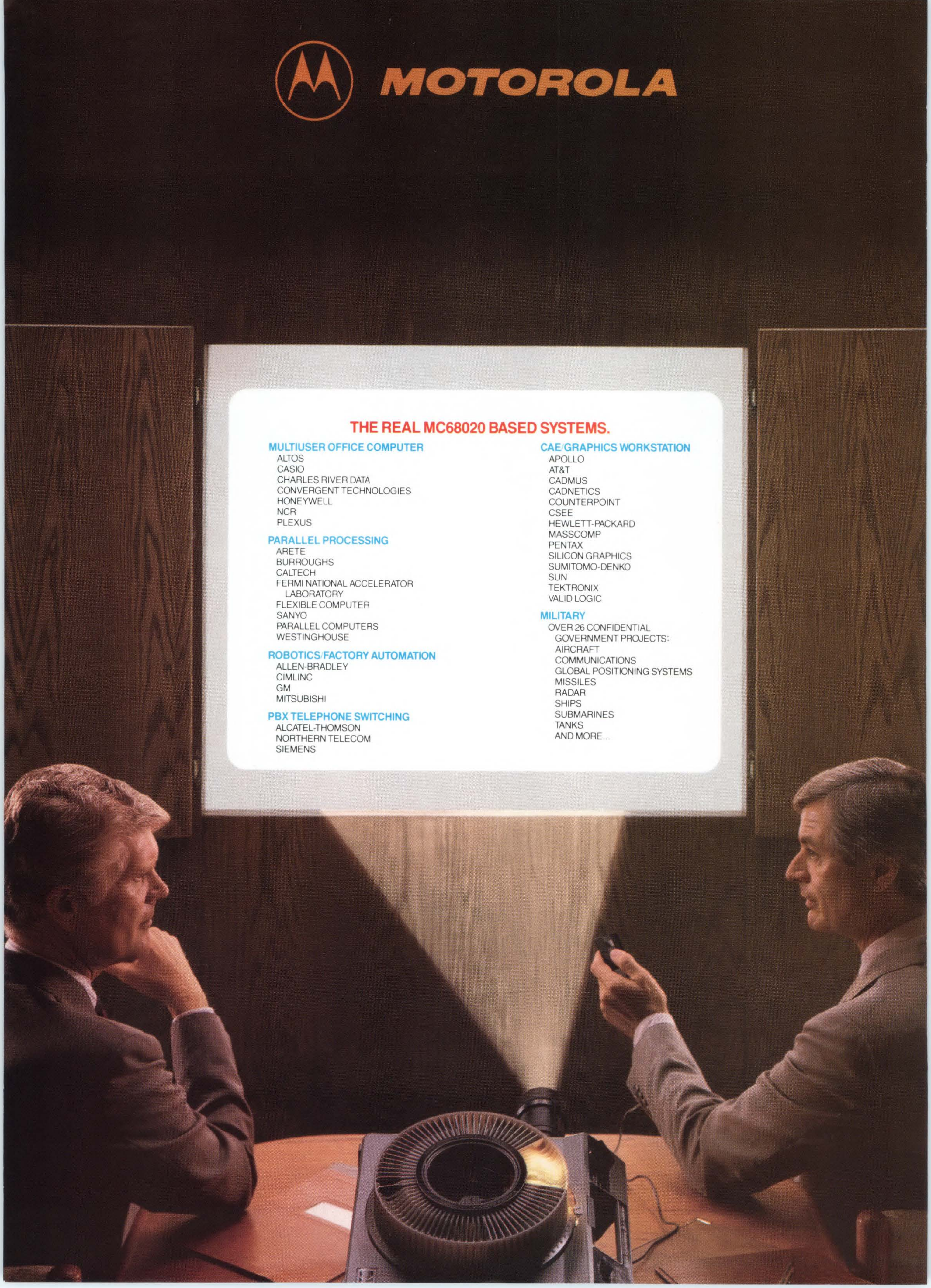
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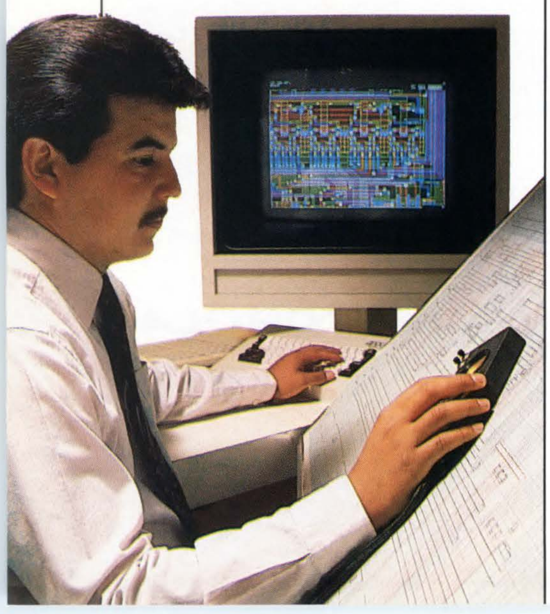

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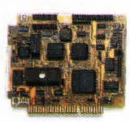

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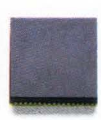

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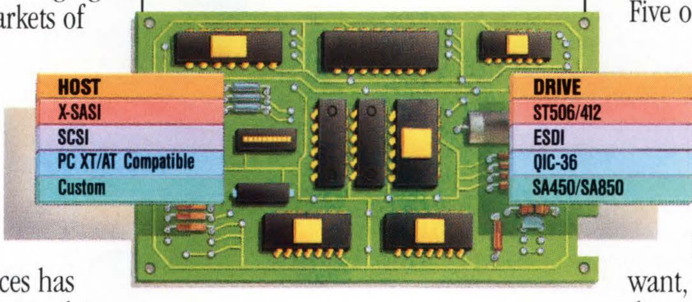

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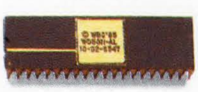
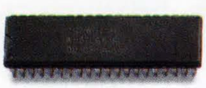
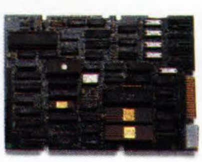


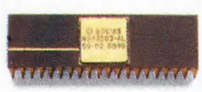
WD5011-10 ST506 Hard disk controller/formatter using 2,7 RLL encoding and on-chip 56-bit ECC.



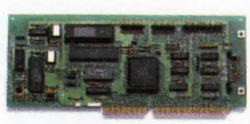
WD37C65 CMOS Floppy disk controller with on-chip digital data separator. NEC765A compatible.



WD1005-SCS SCSI interface controller for up to four ESDI drives with powerful 56-bit ECC.



WD33C93 CMOS SCSI bus interface controller with on-chip high current drivers.



WD1003-WAH 100% PC AT compatible hard disk controller for up to two ST506 drives.

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IMS1423 4K x 4	25,35,45	660	33 CMOS	CMOS
IMS1600 64K x 1	45,55,70	440	77 CMOS	CMOS
IMS1620 16K x 4	45,55,70	440	77 CMOS	CMOS

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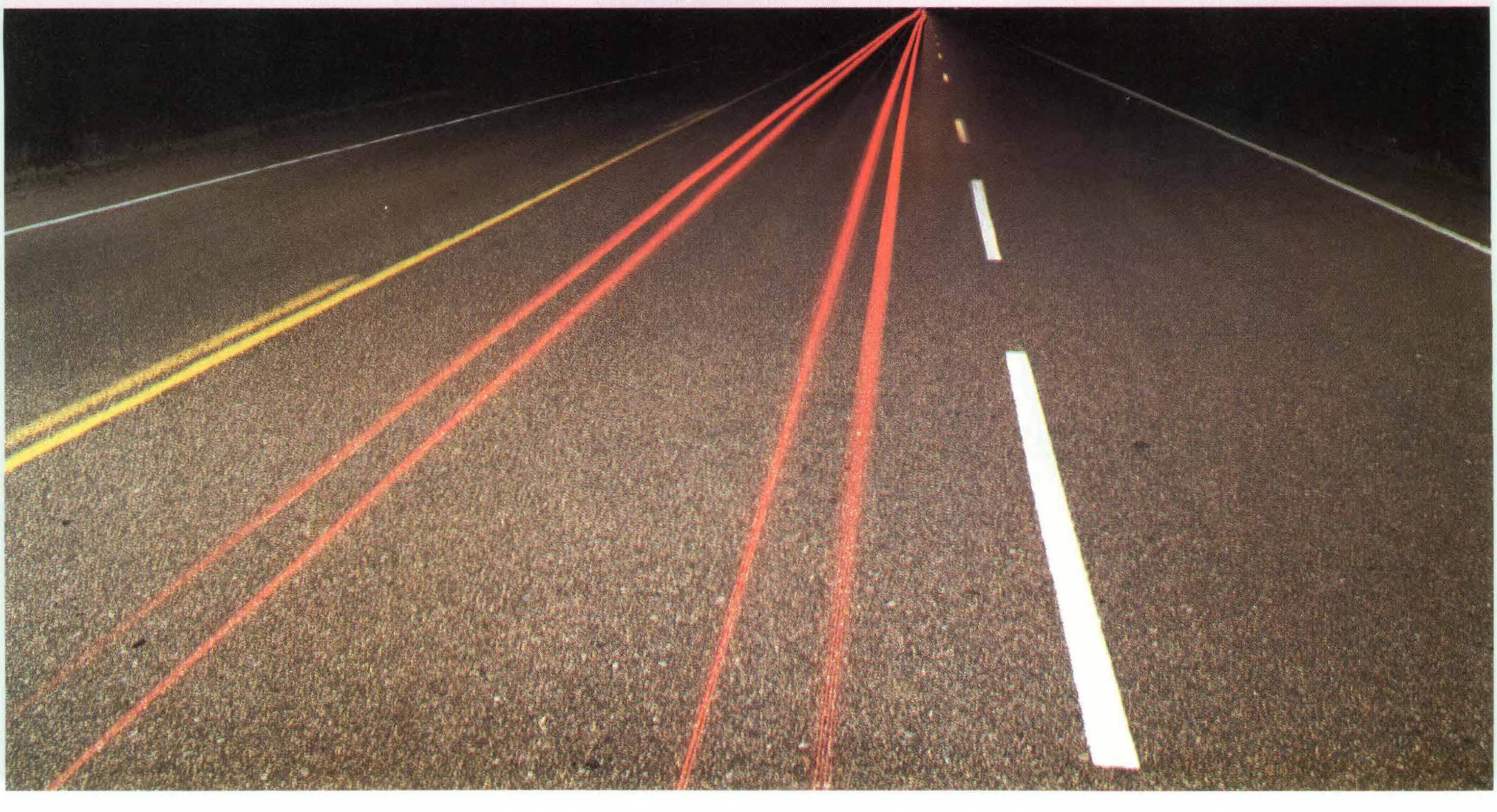
CIRCLE 28



Falling costs per megabyte will upset Winchester balance

Large hard-disk drives still dominate big-system storage, but smaller drives—at under $10/Mbyte—could put them on shaky ground.

BY TERRY COSTLOW

If you were to list the advantages of the latest-generation Winchester disk drives, fast access times, low unit costs, and unprecedented capacity would no doubt top the list. But the past months have revealed an untouted benefit that may give system designs a much bigger lift.

As the production volumes of high-capacity 5¼- and 8-in. drives rise, the price per megabyte creeps closer to the levels associated with rack-mounted 10½- and 14-in. drives. In just the past 12 months, the prices of the smaller drives have fallen below $10/Mbyte and may close the gap with rack-mounted drives next year (see the table). Suddenly, system integrators can concentrate on technological trade-offs without worrying about the financial impact.

System designers needing a gigabyte of storage now have several alternatives: a single large drive, two or three 8-in. drives, or a brace of 5¼-in. drives. William Anderson, chief executive officer of U.S. Design Inc. (Lanham, Md.), which makes disk-drive subsystems for CAD/CAM, notes that about a third of his customers choose 5¼-in. drives for applications traditionally reserved for 14-in. units. Explains Anderson, "The price per megabyte is quite often the first issue that comes up in high-end systems."

In the past, high costs eliminated smaller drives as network file servers or as minicomputer storage systems when size and floor space were not too important. "A couple of years ago, you could make the decision blindly: A big drive's cost per megabyte was always cheaper," observes Philip Goldman, manager of storage engineering at Apollo Computer Inc. (Chelmsford, Mass.).

The declining cost of storage in small drives does not, however, spell the demise of 10½- or 14-in. drives. Disk Trends Inc. (Los Altos, Calif.), scorekeeper for the disk-drive industry, reports that 10½- and 14-in. drives constitute about 87% of the 500-Mbyte-and-up market volume when captive manufacturers like DEC and Hewlett-Packard are counted along with OEMs. With captives excluded, rack-mounted drives still dominate the market: 43% of the 50,000 high-capacity drives shipped last year.

But a change is in the offing. James Porter, president of Disk Trends, notes that shipments of large drives are falling, since the units are not being designed into new systems as often as in the past. Moreover, he contends that the megabyte costs of different sized drives are converging "because there's no research and development in 14-in. drives."

REDEFINING THE 14-IN. NICHE

That contention brings a sharp retort from vendors. "Research in thin-film heads, surface mounting, and media can be applied to any size drive," insists Pat McMahon, general manager of marketing support for Control Data Corp.'s Peripheral Products Division (Minneapolis), which makes 5¼- through 14-in. drives. "There is a future for 14-in. drives, but not as general-purpose storage," he concedes. "In superminis and image processing, which need large volumes of storage, they will maintain a respectable share."

McMahon believes that the strengths of 14-in. drives deserve emphasis. For instance, large drives offer a 24-MHz data transfer rate, compared with about 15 MHz for

Disk drive price-capacity progress

Disk	1983	1985	1987
5¼-in.			
Price/Mbyte	$28	$10	$7
Typical capacity (Mbytes)	36	80	300
8-in.			
Price/Mbyte	$26	$10	$7
Typical capacity (Mbytes)	80	360	550
9-, 10.5- and 14-in. (rack mounted)			
Price/Mbyte	$18	$9	$6
Typical capacity (Mbytes)	300	800	1500

SOURCE: CONTROL DATA

8-in. drives and 10 MHz for 5¹/₄-in. units. The high speed proves extremely important when files are transferred. Furthermore, the big motors of the large drives give them better reliability. Smaller drives with slower-starting motors wear down read-write heads more quickly, he notes.

Nonetheless, the inevitable fall from grace of 14-in. drives promises a resurgence for 8-in. drives, which only a few years ago were labeled endangered species after high-capacity 5¹/₄-in. drives began appearing. Representative of the new generation of 8-in. drives is the 510-Mbyte MK-288FC from the Disk Products Division of Toshiba America Inc. (Santa Clara, Calif.). Four of the pieces can fit into the space taken by a 14-in. drive, for a total capacity exceeding 2 Gbytes. Besides offering about twice the storage of one 14-in. drive, the unit's $4315 price tag translates into $8 a megabyte, roughly equal to that of a 14-in. drive.

Many minicomputer designers are likely to pick 9-in. drives over larger ones in the immediate future. "In a file server or other area in which size isn't a key factor, I would pick a 9-in. drive for about a gigabyte of storage," says Apollo's Goldman. "Only a few 8-in. drives have reached 500 Mbytes, and they're still not mature."

Several 9-in. drives, as well as some 8-in. drives, such as the 8.8-in. 615-Mbyte AMS 571 from Century Data Systems Inc. (Anaheim, Calif.), basically have the same dimensions as 14-in. drives but only half the height. Two can fit into a rack normally dedicated to one 14-in. unit.

While large drives still dominate high-end applications, the course seems to be changing. Even designers who do not have the stringent size requirements imposed by personal computers and other compact systems can gain by using several small drives instead of fewer large drives, proponents say. Teaming 5¹/₄-in. units is becoming increasingly popular for OEM systems, as long as total capacity needs do not exceed 1 Gbyte.

"You might be able to put a gigabyte of storage in place more easily with larger drives, but it might be a poor commercial choice," says Disk Trends' Porter. "Smaller drives can be ganged together by an OEM, giving customers a number of incremental steps."

A gigabyte of storage with larger drives may be easier, but it might be a poor choice

MORE POWER NEEDED

Explains Leon Malmed, director of sales at Maxtor Corp. (San Jose, Calif.), which makes 380-Mbyte, 5¹/₄-in. drives, "With larger drives, you need more floor space per megabyte, plus you need another power supply and extra cooling."

Configurations of multiple small drives have other advantages. U.S. Design's Anderson suggests that if each drive has its own controller, I/O can be overlapped and commands queued to increase throughput—all drives run in parallel. The processing gains would vary widely, depending on the number of drives and types of accesses.

But would the risk of downtime increase if a designer relied on multiple drives? McMahon of Control Data notes that system "uptime" can be increased with multiple spindles. "If you duplicate important data in a system equipped with four or five drives, you can make breakdowns all but invisible," he says.

A SEARCH FOR BETTER SEEK

The performance limits of 5¹/₄-in. hard drives become particularly significant when system capacity hits 1 Gbyte. Apollo's Goldman notes that the average seek time is a critical factor when many users share a disk drive. It is below 20 ms for most 8- and 9-in drives, but 22 ms is the fastest for 5¹/₄-in. units.
units.

The types of files being stored can also play an important role in storage configuration. "The smaller drives are sometimes no good when the user wants to split files easily between two or three 5¹/₄-in. drives," says Mark Wilson, director of product marketing at Fujitsu America Inc.'s Storage Products Division (San Jose, Calif.). Large files of interrelated information, such as CAE projects about to be simulated and then routed, are hard to divide and manipulate on a multiuser, multidrive system.

Noticeably absent from the list of designers' options are optical disks. "Before optical technology can compete, it must solve its slow seek time," says CDC's McMahon, noting that 150 ms is quick for an optical drive. However, optical disks will be a good adjunct to magnetic storage—less than $4/Mbyte for write-once applications.

Conversely, no one views the sub-4-in. hard drives—gaining popularity as drop-in cards for PCs—as a factor in high-capacity storage, since they are not expected to rival the 100-Mbyte-plus capacity of 5¹/₄-in. drives for quite some time. A 50-Mbyte, 3¹/₂-in. drive, currently top-of-the-line, poses no threat to the 170-Mbyte 5¹/₄-in. units now considered a commodity item.□

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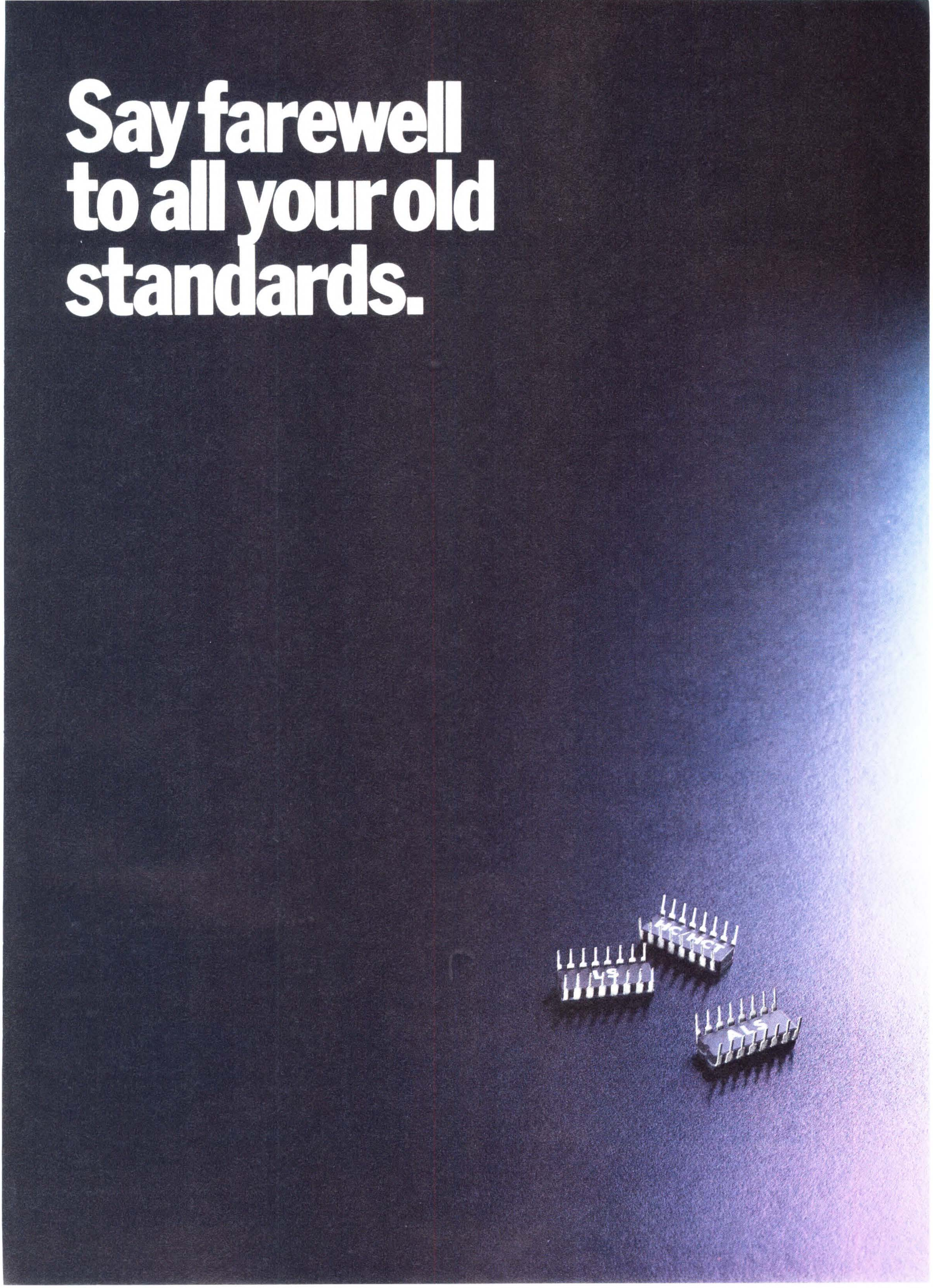

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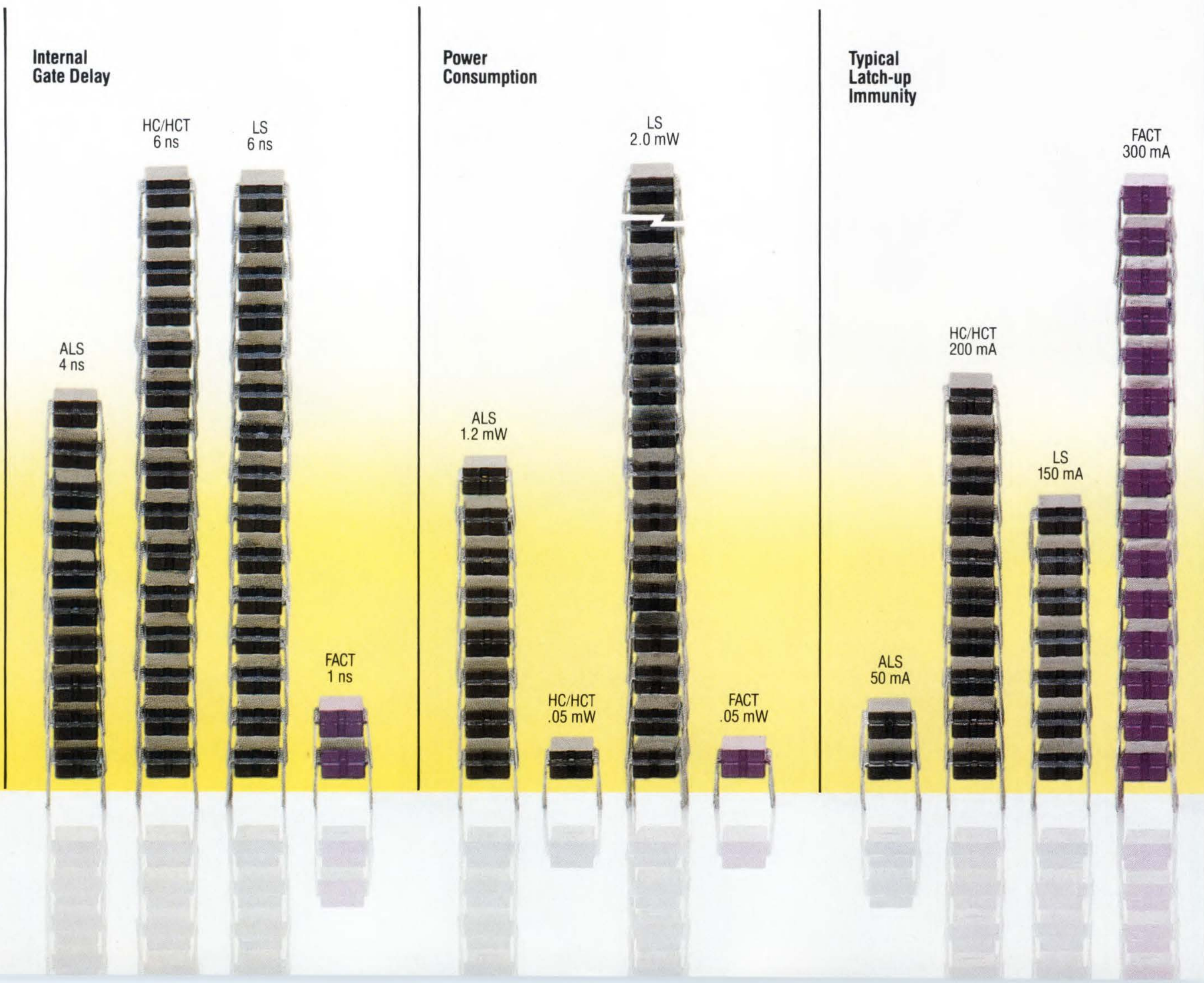

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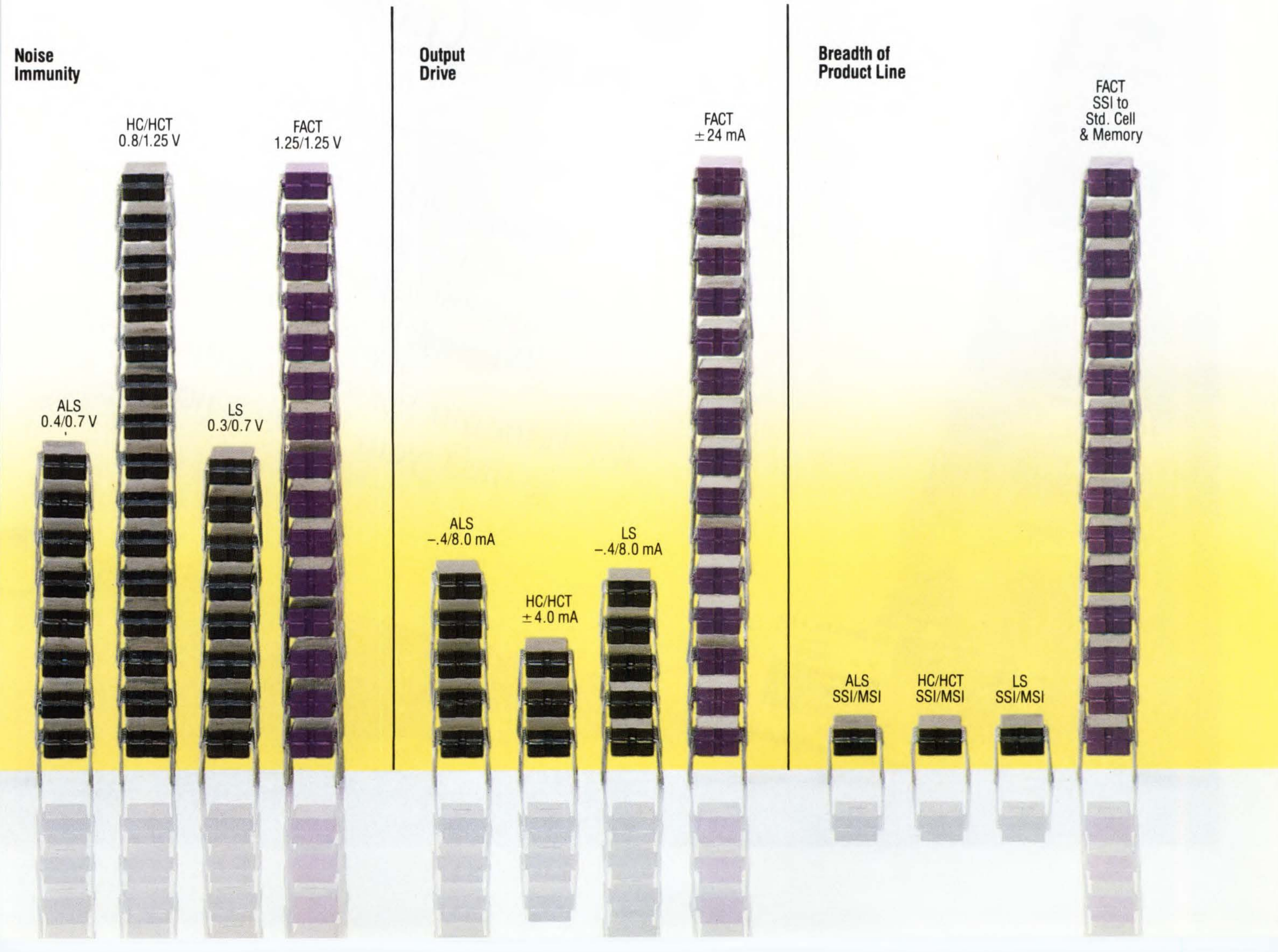

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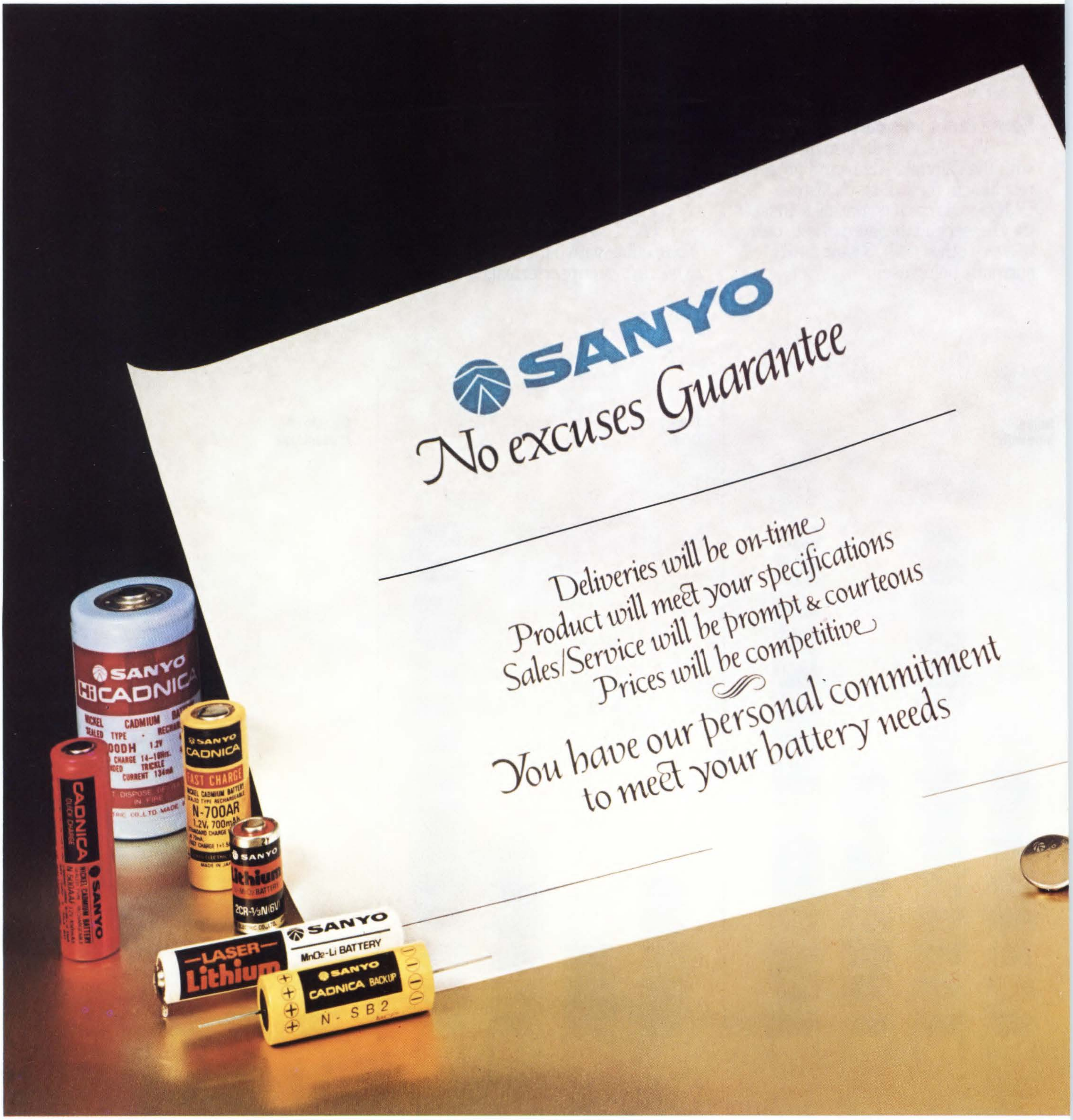
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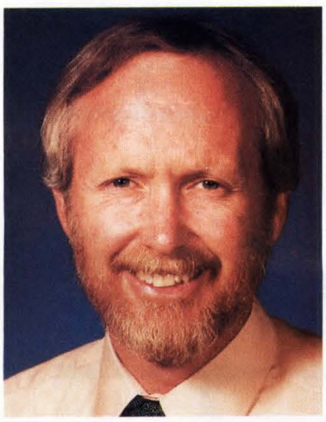
CIRCLE 31

EXCLUSIVE INTERVIEW

Design evolution leads to system revolution

Anthony Rollins

Rollins is manager of system architecture and formulation at NCR. He holds a doctorate in mathematics from the University of California at Davis.



Wayne Lewis

Lewis is manager of large-system processor development. He received a bachelor's degree in electrical engineering from California State University at Long Beach.

Designing a computer system for a well established vendor is never easy. Besides the inevitable tradeoffs, there is the problem of increasing processing power while maintaining compatibility between the new designs and the old.

Wayne Lewis and Anthony Rollins faced these challenges when they led NCR design teams at its engineering and design center in San Diego that upgraded the company's mainframe line. "In some areas of computer design you can sit and design a fast processor and then apply it to any software," says Lewis. "But when you already have a very sophisticated system architecture and must depend on existing software, you're very tightly constrained. You have to take a system approach, coming from the top and going down. And you're not solely directed by technology. We had to make sure that the new line was downwardly compatible and that future designs could evolve as well," Lewis recalls.

The result of their four-year design effort is the 9800 series, an extension of earlier architectures, such as the 8000 series and the even older Criterion machines—all of which run under NCR's VRX operating system with the Neat assembly language.

The NCR team's design made use of the emulator technology of its existing 32-bit chip set to organize a loosely coupled multiple-processor configuration that avoided the software complexities implicit in shared mass storage.

Rollins, manager of system architecture and formulation, explains that emulating the older architecture's instruction sets left the team free "to concentrate more on performance issues. By developing a multiprocessor configuration that was expandable, we could incrementally increase computing and storage resources without impacting the software.

"The chip set was the key to extending the existing architectures. It was specifically designed to emulate mainframe instruction sets. Furthermore, it was formulated with the idea of mixing a general-purpose emulation engine with one or more specialized hardware assist engines."

The team devised a Neat assist chip (NAC) to aid direct execution of the Neat assembly language in each processor. Even though the NAC directly executes less than one-third of the most frequently used Neat instructions, in an average mix the chip runs 89% of the code set, off-loading a significant amount of the processing. With so many of the instructions embedded in hardware, the NAC greatly increases processing efficiency with minimal impact on overhead software.

But the 9800 project's greatest challenge and the revolutionary solution lay in configuring a system-wide memory. With a loosely coupled multiple-processor design, the trick is to tie the mass-

Ray Weiss

storage subsystems together so that the processors can share memory as a central resource.

"Originally we started out with the idea of tightly coupling the processors, but we ran into bandwidth problems on their interconnections," Rollins recalls. "Once we had the system memory concept in place, actually implementing the software from earlier systems on the 9800 turned out to be pretty straightforward. Each processor is an independent computer system with its own local memory and shares disk space."

To make it work, the design team used the 32-bit chip set in two ways: as data system processors (here, DSPs) and as applications processors (APs). According to Lewis, "The DSPs function as system memory controllers. Existing software could migrate by allowing them to provide the glue—providing system-wide operations like process-level queues for multiprocessing."

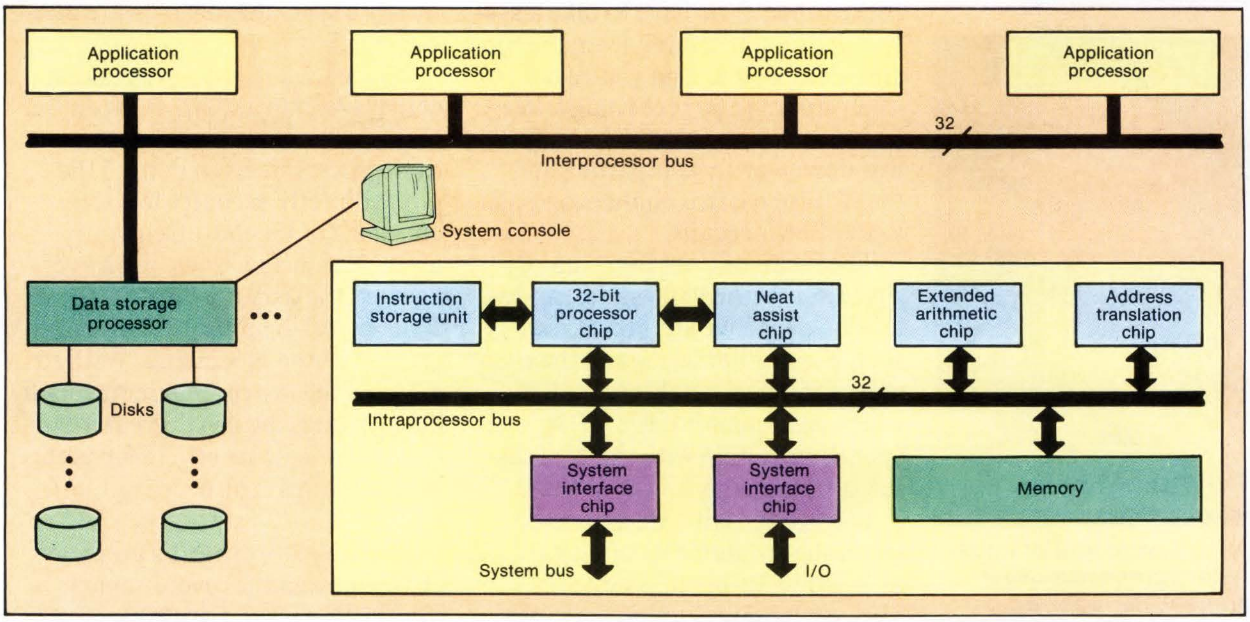
The DSPs sit below the APs, each managing a disk farm. The disk space is handled as files made up of byte streams that are addressed by logical locations. In that way, access to a file can be shared, in a structure not unlike that of the Unix operating system.

After the memory organization, the greatest hurdle was the bus design. Insists Lewis, "It was not a trivial problem to build the VLSI chips to support 24-Mbit/s serial transmission."

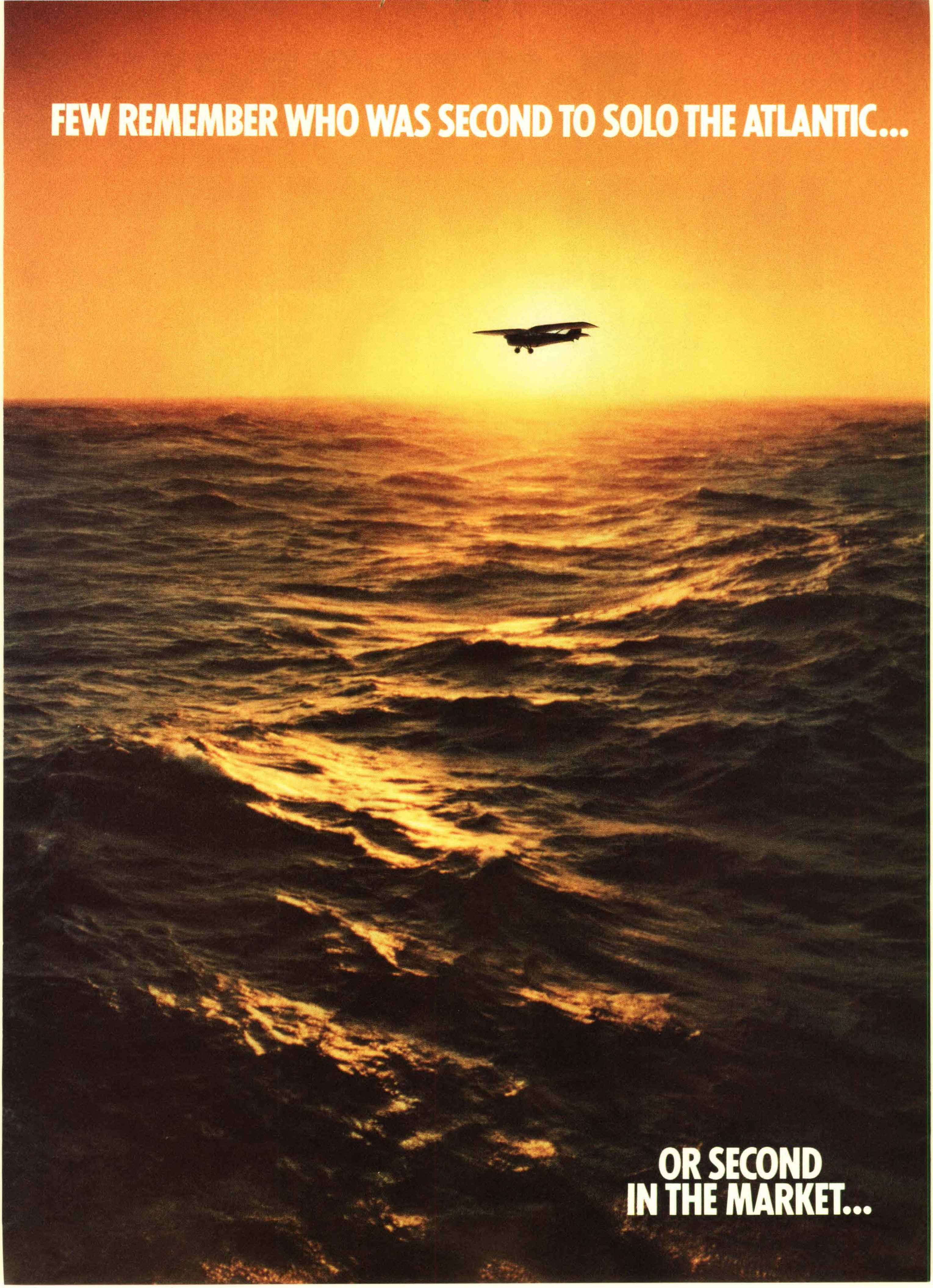
The APs are tied together with two system-wide Ethernet-class buses operating at 6 Mbytes/s. They also link the DSPs and the APs (see the figure). "By making each processor self-contained, with its own memory, the load on the system bus was kept down," Lewis explains, "allowing us to go to a more loosely coupled architecture."

In a way that is typical of large computer companies, a group of five to ten key people were charged with creating the new design. "It was a real blessing that the hardware and most of the software people were in the same location," says Lewis. "As long as we worked together on a daily basis, the problems got solved. We just had to make sure that all the right people were consulted on design issues."

And what of the future? Designers often leave things undone, postponing them until the next time around. Some even say that any design is just one step toward the next one. "What we want to do next," says Rollins, "is speed up the system by going to higher levels of integration and using smaller chip geometries." The chips are at present made with 2 μm. "We are now at a level of VLSI," Rollins adds, "at which we could combine a number of the current chips and speed our cycle time as well as reduce off-chip losses." □



Each application processor (AP) in NCR's new 9800 mainframe series operates independently with its own local memory. The upper drawing shows the processors connected by two Ethernet-class 6-Mybte/s buses. The AP's configuration (inset), including NCR's 32-bit microprocessor chip set, is linked by a memory bus to special processor chips, including a Neat assembly-language assist chip.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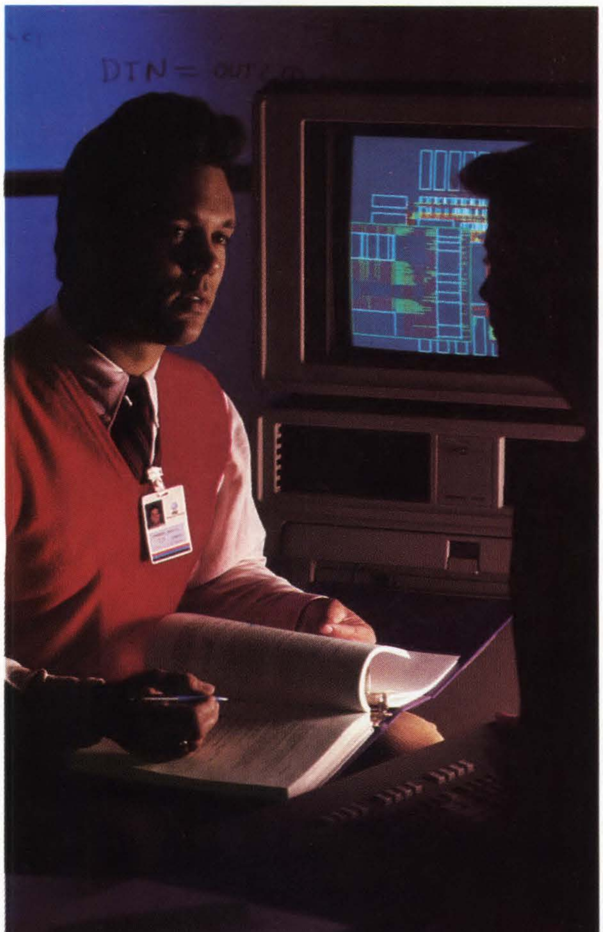

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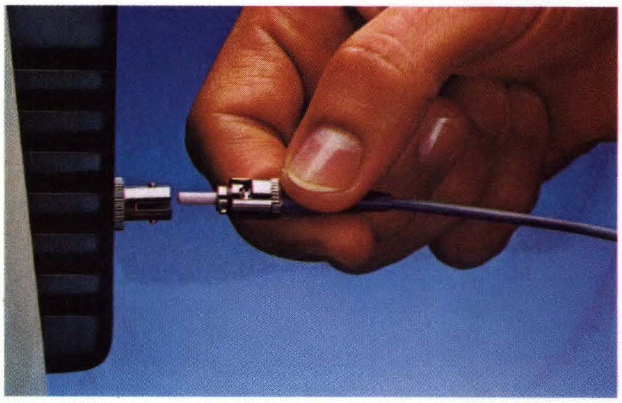

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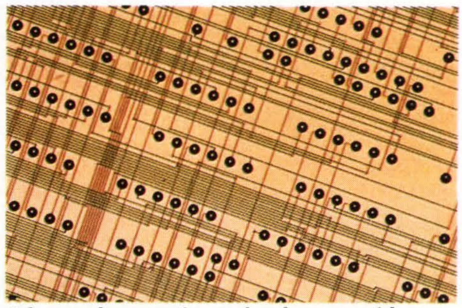

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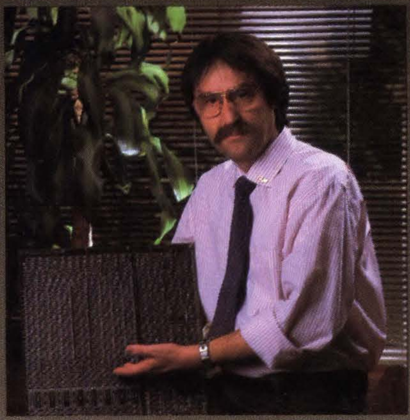
AT&T

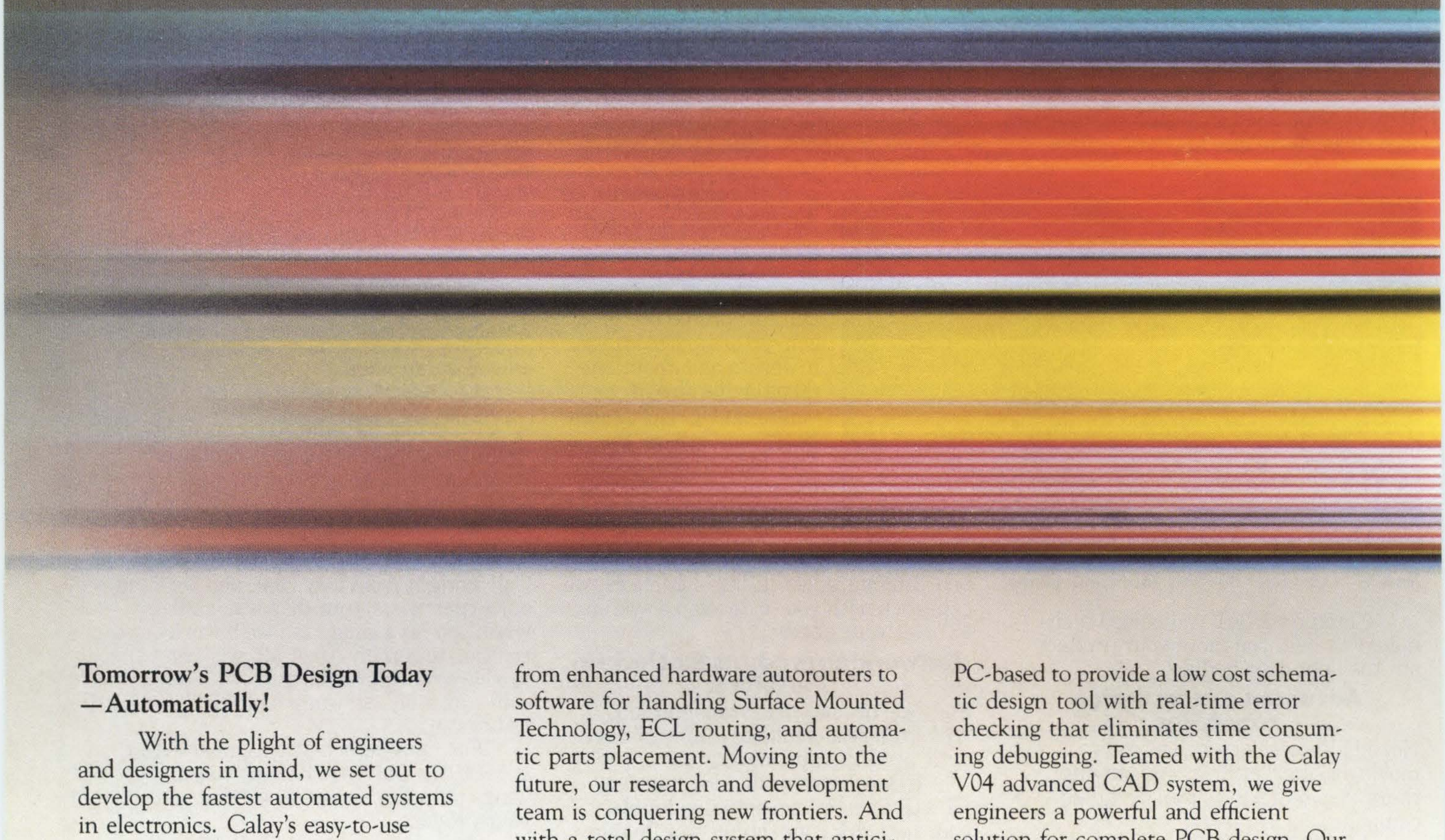
The right choice.

CIRCLE 32

Time May Be Running Out...



Richard A. Finn
President and C.E.O. of Calay Systems, Inc.



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With the Calay system every aspect of the design cycle is accelerated including the rough spots such as the unexpected but inevitable engineering change orders. Calay makes initial data

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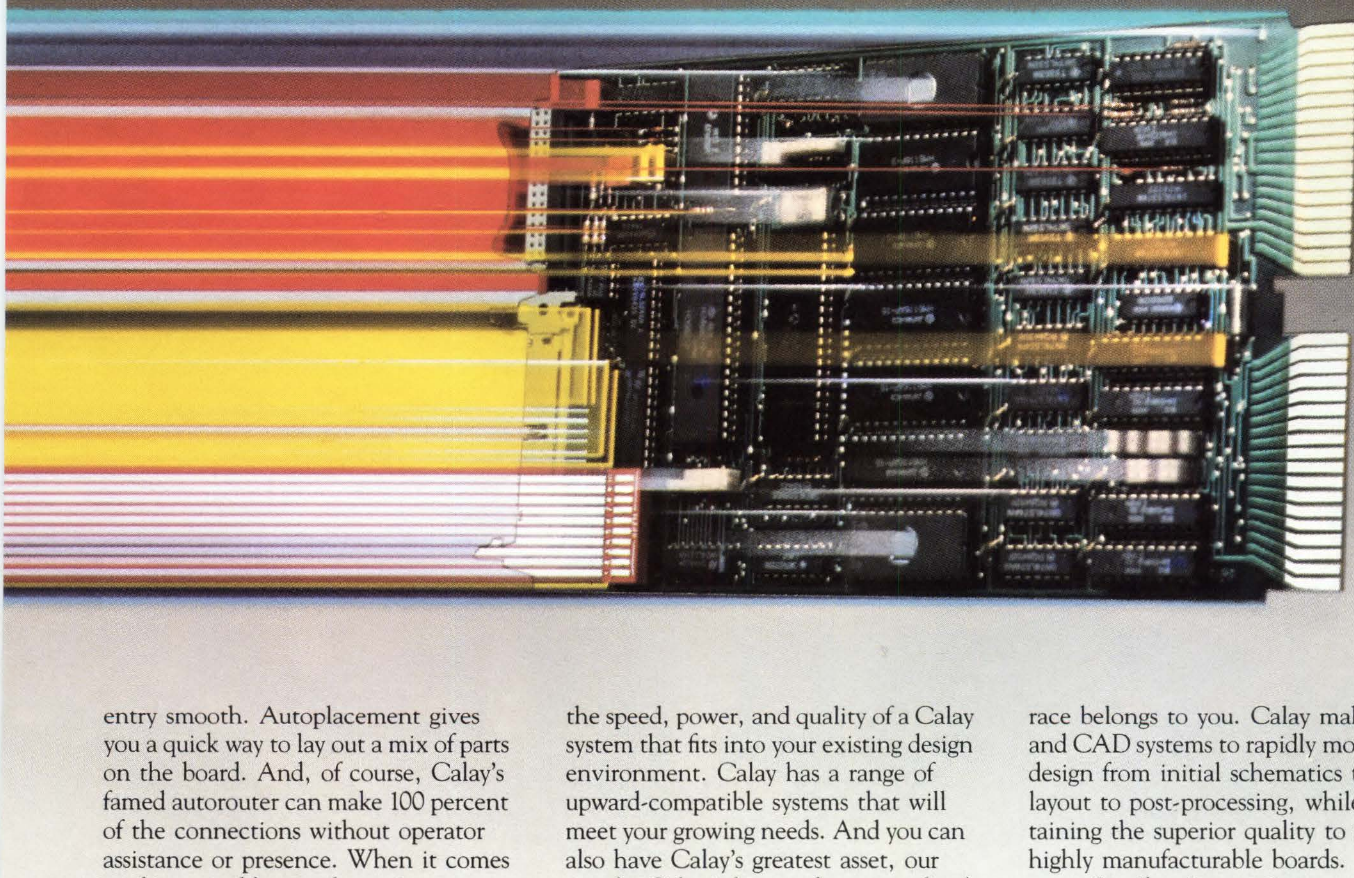

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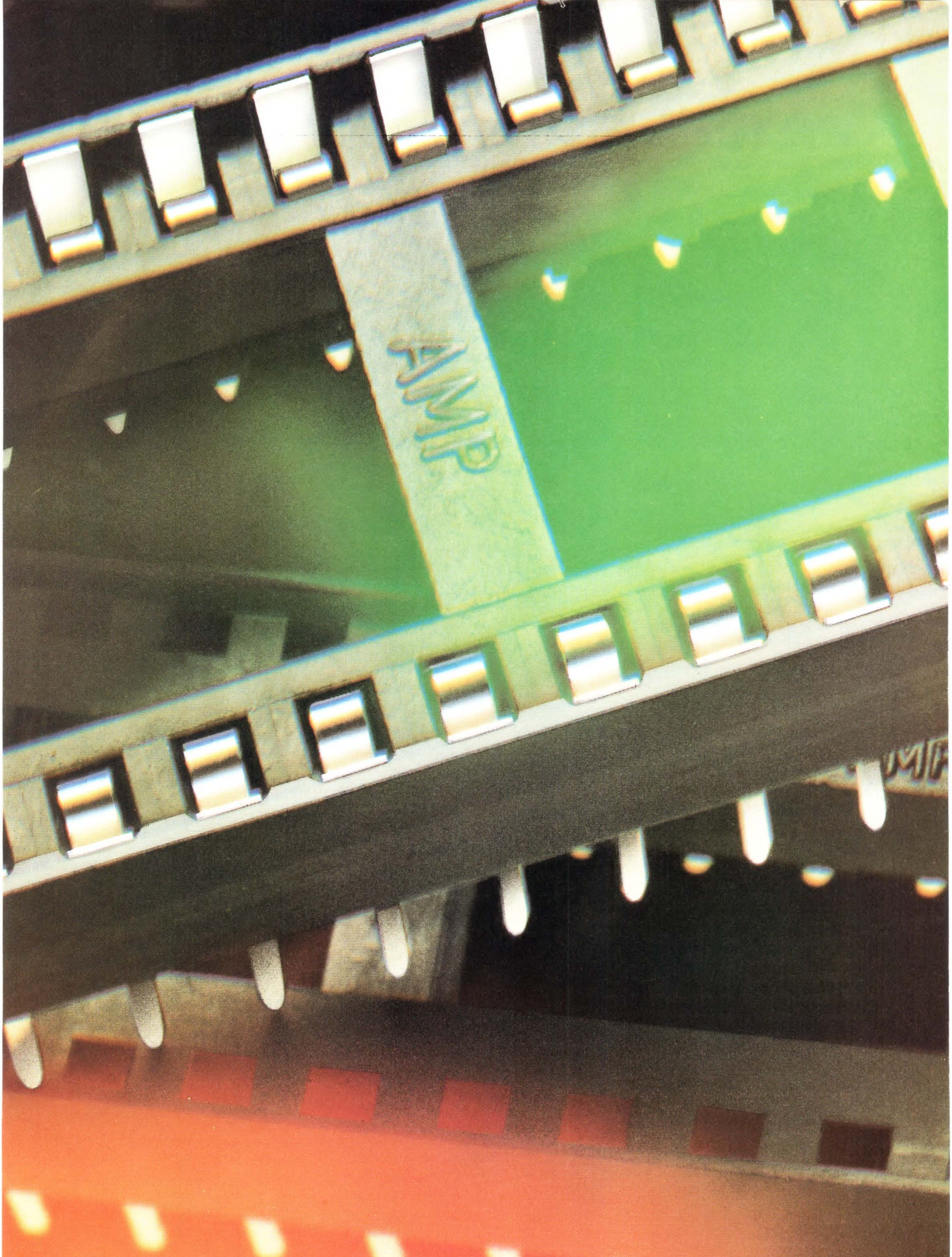
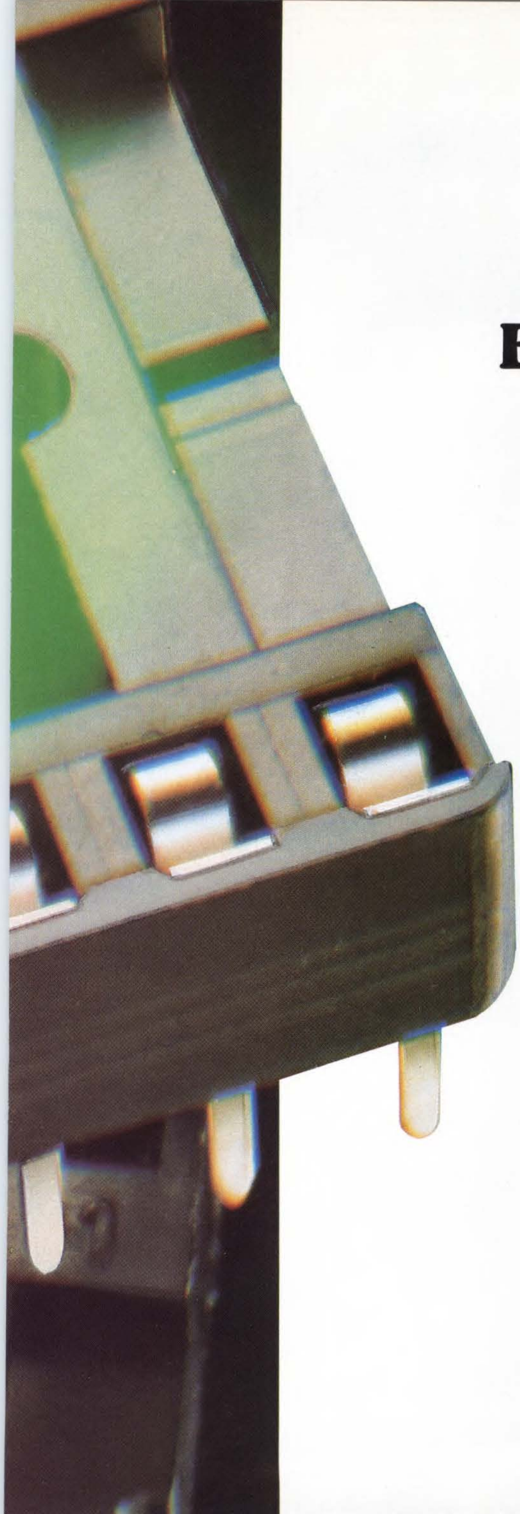
CIRCLE 33


AMP



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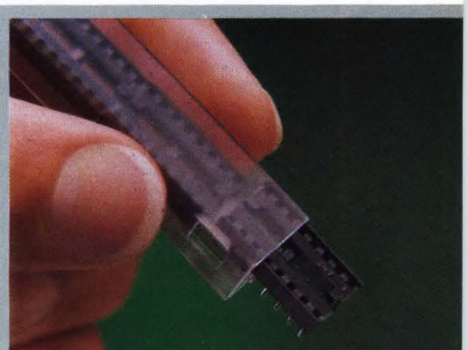
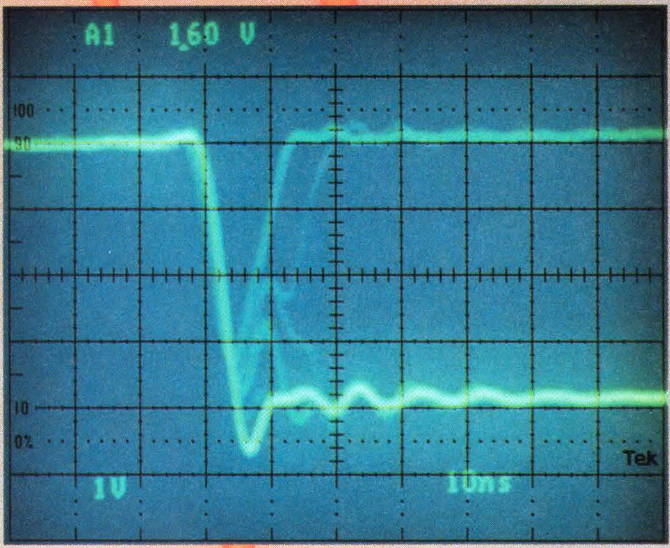


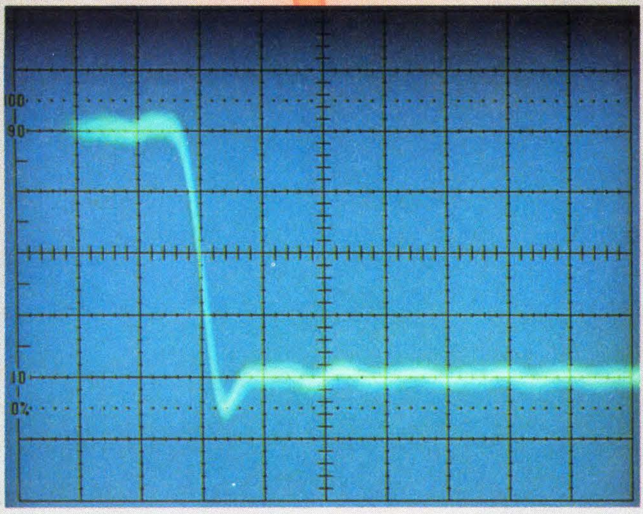
Many AMP DIP sockets have MIL-Spec qualification. All feature high reliability. High productivity, too, with fast machine application or easy hand insertion.

CIRCLE 34

IN A MATTER OF SECONDS, THE NEW TEK 2467 CAN SAVE WEEKS OF TROUBLESHOOTING.



Now. See what you've always needed to see with a portable scope. (Above) Tek's new 2467 Transient Intensifying Oscilloscope, with its exclusive microchannel-plate CRT, highlights the infrequent metastability of a flip-flop output. (Below) The same metastability is invisible on a conventional high-speed scope.



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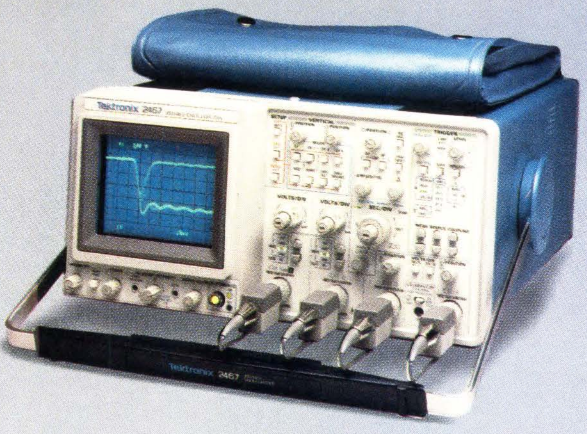

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CIRCLE 35

ELECTRONIC DESIGN EXCLUSIVE

Plug-in board speeds PC's analog I/O

The fastest analog I/O board for IBM PCs grabs 12-bit signals at 166 kHz. It also can calculate linear systems' transfer function.

BY FRANK GOODENOUGH

Though they may sport 12-bit accuracy, analog I/O boards for the IBM PC are, for the most part, slow. Most run at less than 50,000 samples/s. When superfast sampling is mandatory, the choice of boards dwindles, and the fastest model board, which samples at 130 kHz, works only with a PC AT–class host.

Now, in an innovative design he dreamed up for MicroWay Inc., consultant Douglas Rife has come up with a board for the plain-vanilla PC—as well as for its higher-performance cousins and clones—that takes 12-bit samples at the rate of 166,000 a second, giving it the new title of fastest board around.

The dual-input, $1295 A2D-160 not only combines the price and performance needed for general-purpose data-acquisition jobs, it also handles a more complex task—analysis of linear systems. A pseudorandom binary-sequence generator and floppy-disk–based software guide the PC through a fast Fourier transform to determine the system's transfer function (see "Calculating the Transfer Function," p. 70).

The board gets much of its speed from the fastest 12-bit, analog-to-digital converter chip, the AD7572 (ELECTRONIC DESIGN, Dec. 12, 1985, p. 93). Ahead of the a-d converter lie a pair of fast sample-and-hold amplifiers (3-μs acquisition time and 1-ns jitter), one for each input channel (see the figure).

And since most sampled-data systems need an antialiasing filter, the board leaves room for a pair of optional filter modules or for user-designed signal-conditioning circuitry. Optional filter modules can have both their gain and their response programmed through software.

MANY MODES TO GO

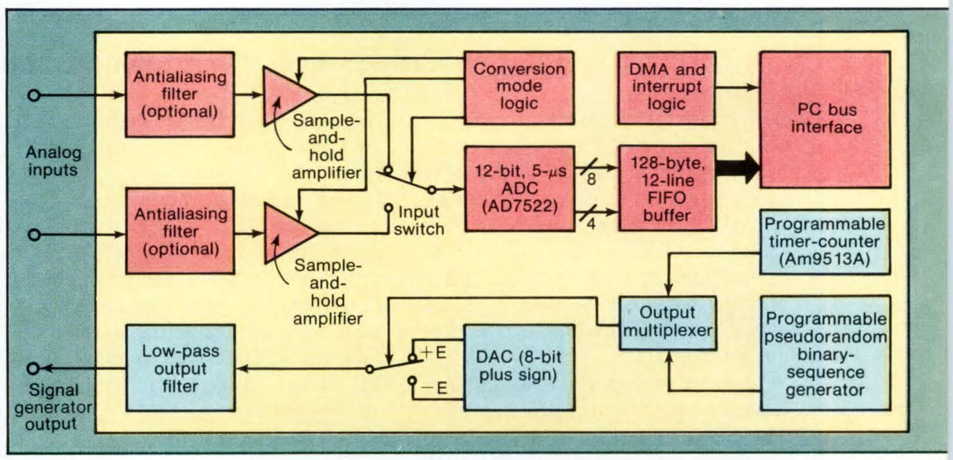
The sample-and-hold amplifiers on the two input channels can be programmed for three different modes of operation. In the first, the so-called conventional mode, an input signal is applied to either input channel, giving the board a sampling frequency of 110 kHz.

In the simultaneous-sampling mode, with a different signal tied to each input, the board samples at up to 65 kHz per channel. Signals on both inputs are grabbed at the same time, with the input switch letting first one, then the other flow to the a-d converter.

Finally, in the ping-pong mode, a single signal is connected to both inputs, affording the high-speed sampling rate of 166 kHz. In this mode, one of the channels is in hold while its signal feeds the converter. Meanwhile, the other channel is grabbing a signal. When both operations are finished, the input switch moves the converter to the newly sampled analog signal, and the second sampling amplifier goes after new data.

A 128-byte-by-12-line FIFO buffer memory sits at the intersection of the converter's output, the DMA circuitry, and the PC's interface bus. It eliminates any loss in data that might occur when switching memory segments, and it sends the data to the host over a single DMA channel.

The amount of data that can be



The A2D-160 analog I/O board uses the fastest 12-bit a-d converter available, the AD7572, and also has sites for antialiasing filters. A built-in pseudorandom binary-sequence generator helps determine the transfer function of a complex linear system.

Fast analog I/O board for PCs

acquired is limited only by the memory capacity of the host PC. In fact, the amount can reach 4 million contiguous samples, as the board's software and hardware support the Intel/Lotus expanded-memory standard. In addition, since data is written to memory through direct memory access, the board and its supporting software run in the background while the host's main application program runs in the foreground.

An elegant timing and triggering subsystem further distinguishes the board. Through this circuitry, an external event can trigger a sampling or conversion process, which continues for the number of samples set by software. Moreover, an on-board programmable timer can delay the input trigger pulse for up to 65,535 sample periods. With that delay, the a-d converter can wait until a high-speed transient occurs (at a predetermined time after the trigger) and then start digitizing samples of the transient. Thus the board does not fill the PC's memory with useless data while waiting. Furthermore, by adjusting the trigger delay and the number of samples, a designer can zero in on data of interest while ignoring the information preceding and following it.

Alternatively, a conversion sequence can commence after a trigger from software or from the on-board pseudorandom binary-sequence generator. Moreover, the hardware can be set to respond to a pulse's positive- or negative-going edge or to high or low logic levels.

ASSUMING A NEW ROLE

A delay-and-capture trigger mode permits the A2D-160 to emulate a basic sampling digital oscilloscope. Here, the trigger pulse starts the trigger-delay timer. At time-out, the capture period begins and the board takes a preset number of samples. When the next trigger pulse arrives, the process repeats, with the data stored in the next consecutive memory location. The delay and capture intervals each can last for up to 65,535 sampling periods.

The time base for the sampling clock is selected by software from one of the following: the internal 2- and 4-MHz oscillators, the a-d converter's 2.5-MHz clock, or an external pulse train between dc and 6 MHz. To develop the final sampling rate, any clock signal can be divided on board by any integer between 2 and 65,535. Thus the 2-MHz clock yields a minimum clock rate of 30.518 Hz.

The optional AFM-50 filter and signal-conditioning module for the board's front end belongs in the same class of performance as the rest of the board. Basically, the module consists of a pair of cascaded, continuous-time, second-order filters.

The sections can be programmed to form a variety of four-pole low-pass filters including Bessel, Butterworth, and Chebyshev. Their cutoff frequency varies between 0.5 and 30 kHz, their pass-band gain between 1 and 16.□

Price and availability

The A2D-160 analog I/O board goes for $1295 and the AFM-50 antialiasing filter module for $225. Small quantities are available from stock.

MicroWay Inc., P.O. Box 79, Kingston, MA 02364; Brenda Jaeck, (617) 746-7341.

CIRCLE 511

Calculating the transfer function

Besides its high-speed I/O capabilities, the A2D-160 board conducts transfer-function tests on complex linear systems. To do so, it relies on an on-board pseudorandom binary sequence (PRBS) generator. The pseudorandom binary sequences approximate white noise, the equivalent of an impulse function in the frequency domain.

A system's response to an impulse function equals its transfer function. Thus, by using a binary sequence to excite the system, the host PC, with its software, cross-correlates the digitized output with the input binary sequence and calculates the impulse response. Then the host performs an FFT to determine the transfer function.

The pseudorandom binary sequence means a higher signal-to-noise ratio and greater accuracy than would be possible if pseudo impulses (a stream of short, square pulses) were used to excite the system. In fact, the A2D-160 board and its host PC attain 16-bit resolution with a 12-bit converter. And they do so with software—not mirrors.

The PRBS generator on the A2D-160 can be set, through software, for sequence lengths of 1023, 4095, 16,383 and 65,535 points. Its amplitude output is similarly set between 0 and 5.25 V in 255 equal increments.

Normally you choose the shortest sequence that is still longer than the impulse response expected from the system under test. However, the longer the sequence, the higher the signal-to-noise ratio and the greater the accuracy.

If the situation demands it, the board can also generate approximate impulses for system stimulation. Moreover, the circuit can be configured as an 8-bit, plus-sign d-a converter, letting software generate analog test waveforms.

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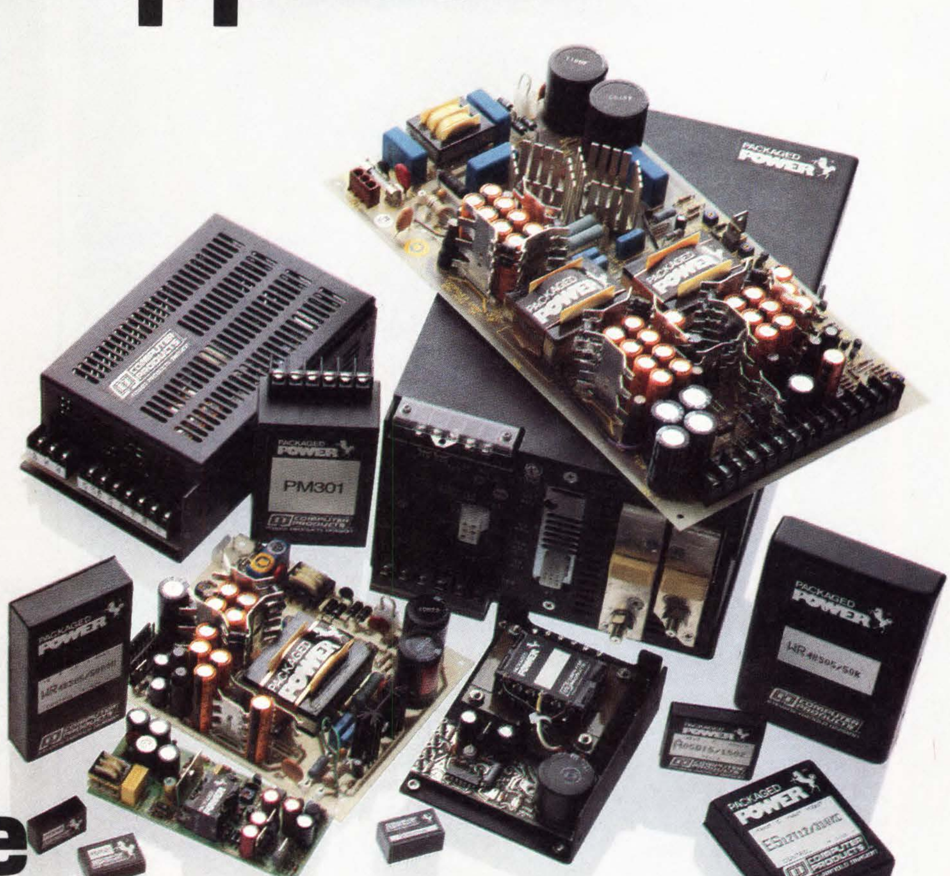

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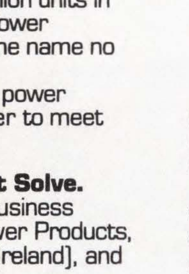

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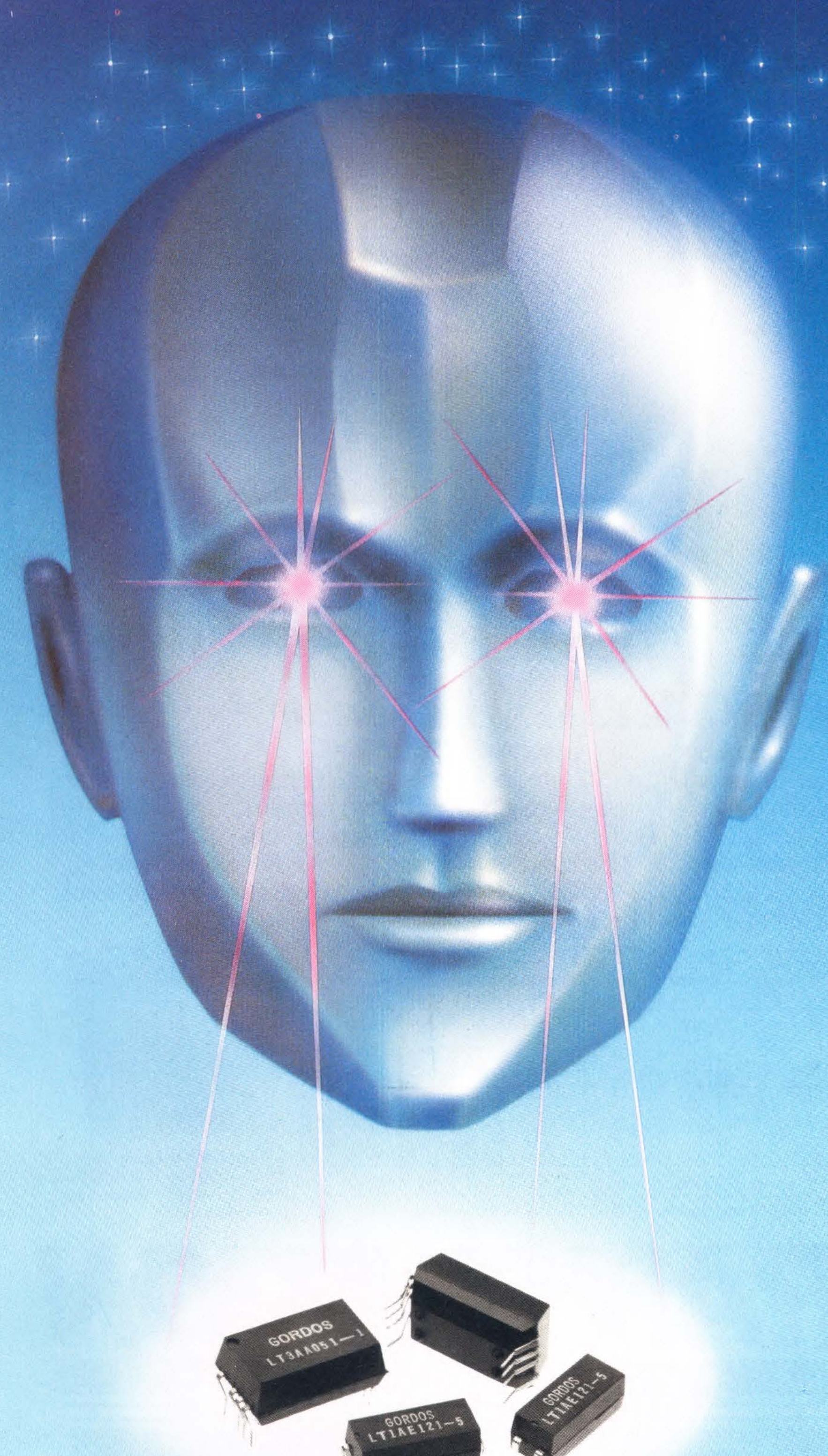
CIRCLE 36

Gordos. Low Thermal EMF Relays with the focus on innovation.



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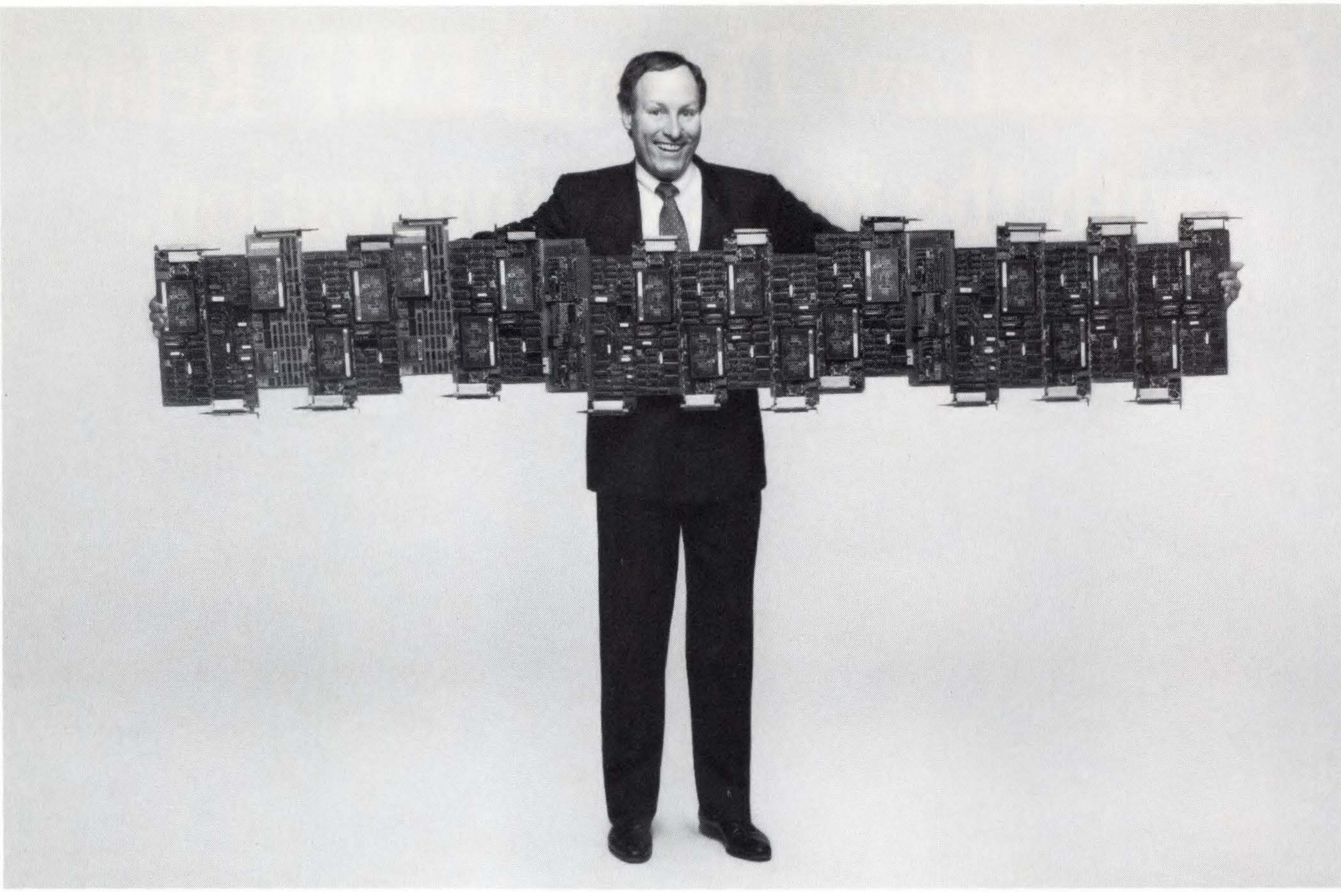
CIRCLE 38



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	General Purpose	DT2801	995-2070	4-16	12-16	13-27	2	12	16	Yes	DT707
		DT2806	295	to 80	12	20	to 24	12	to 72	Yes	DT757
		DT2808	495	16	10	3.3	2	8	16	Yes	DT707
	Low Cost	DT2814	299	16	12	25	–	–	–	Yes	DT757
OVER NIGHT DELIVERY		DT2815	399	–	–	–	8	12	–	–	DT757
		DT2817	199	–	–	–	–	–	32	–	DT758
	High Speed	DT2821	1195-2495	4-16	12-16	50-130	2	12	16	Yes	DT707

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CIRCLE 39

ELECTRONIC DESIGN EXCLUSIVE

50-W power supply fills universal need

Say good-bye to different power supplies for every design. A new assembly metes out +5, +12, and −12 V power as needed.

BY CURTIS PANASUK

Power supplies seem to multiply like rabbits, given that every new system requires its own specially rated unit. National Semiconductor may stem the proliferation with a power supply that dishes out its 50 W as needed to three outputs: +5 V, +12 V, and −12 V.

Traditionally an engineer powers up his design with bench supplies set to the required voltage and then notes the current drawn from each supply. After sifting through a pile of catalogs, he either picks a supply that delivers those currents or orders one custom-made. Either way, it means adding still another item to the inventory.

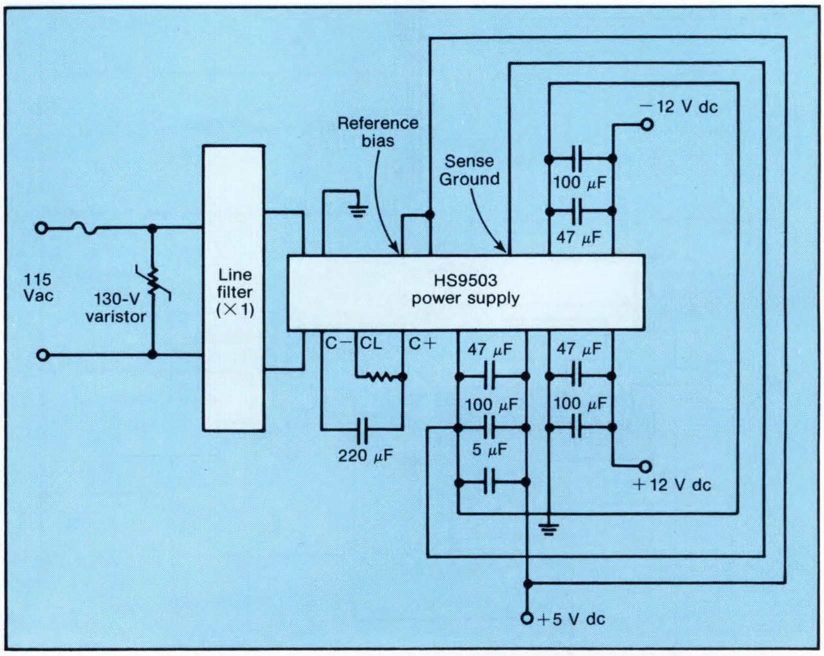
With National's approach, the engineer needs to buy only one supply, the HS9503, for all his designs, provided the total power output is less than 50 W. He will not be alone in welcoming the flexibility and convenience of the 9503. Production people will be happy, too, since they can easily transfer supplies overstocked for one line to another line. And consider the military procurement specialists: Accustomed to wading through specification documents for tens of different power supplies, they now can focus on one document.

The 9503 assembly resides in a trim, hand-sized package (4.75 by 2.75 by 0.84 in.) and it accepts line frequencies of 50 Hz to 400 Hz. The supply boasts a relatively high switching frequency of 350 kHz, a rate that gives it 80% efficiency at half load and 85% at full load. In other words, only 20% of the input power goes into heating the supply package; thus the supply can work in ambient temperatures of up to +85°C.

The leader of the National design team, Michael English, recalls, "We plowed new ground with the 350-kHz switching frequency—it was a trade-off all the way. With a lower frequency, we couldn't have combined such small size and high efficiency."

For setup, the supply's inputs must be wired to the 120-V ac line, and eight output filter capacitors must be added externally (Fig. 1). In contrast, the output filter inductors are built into the power supply. And in choosing the 350-kHz switching frequency, the supply's designers soon found that no off-the-shelf transformers could handle such a high rate; the transformers had to be customized. Luckily they did locate a controller chip that could operate at 350-kHz frequency. Built into the supply (Fig. 2), it acts on error voltages by adjusting the duty cycle of the switching waveform and hence the output voltage

Deciding not to build in the capacitors clearly saves money. Normally such hybrid parts are extremely expensive, about $10 a pop, which would have raised the unit's cost by at least 20%. When



1. To wire up the HS9503, a designer must typically add capacitors to filter each voltage output. The line filter and the varistor are optional. Since large capacitors with low equivalent series inductances could not be found, smaller capacitors are used in parallel.

50-W power supply

added by the user, however, the large discrete capacitors go for about $2 apiece.

The output filter capacitors bring the supply's output ripple down to 50 mV. Though that figure is low enough for all digital applications, it is unacceptable for op amps and other precision analog circuits. Those applications call for a linear supply with ripple on the order of 1 mV.

Inside the 9503, the three output transformer coils share the magnetic core, which acts as a power reservoir. Each coil taps the reservoir according to need.

"We thought long and hard about what voltage outputs would suit the largest number of applications," says Tom Wong, National's application manager. "The combination of +5, +12, and −12 V will work in 60% of new designs; the remaining 40% use oddball voltages, say, −5.2 V for ECL and +4.5 V and −3.5 V for gallium arsenide."

The outputs can also be mixed and matched. For instance, a +17-V output can be formed with the +12-V and +5-V outputs. Likewise, +12 V and −12 V can be combined for a 24-V output.

The convenience of divvying up 50 W comes to light in several applications. A computer board heavy with logic might demand 9A at +5 V and 0.4 A at ±12 V. In another application, the supply could serve a disk drive with a low logic load of 2 A at 5 V, coupled with the heavy 3.3-A, 12-V demands of the disk motor, and a smidgen of −12-V current for an RS-232 interface.

One of the supply's output voltages can be defined as the primary source, with a guaranteed regulation of 1%, and the other two as secondary sources, with a regulation of 10%. (Here regulation means the amount that the output voltage will vary as load current doubles.) The 1% rating exceeds the 5% requirement of TTL and custom logic and still leaves room for growth. The 10% regulation just squeaks by RS-232 application requirements.

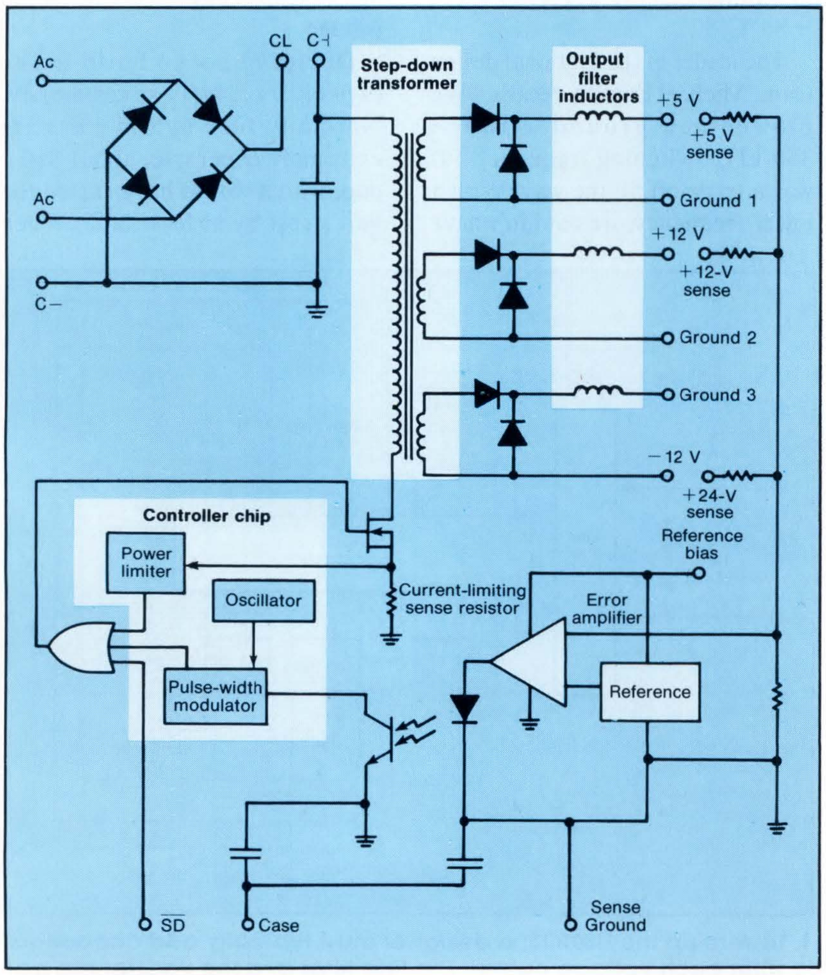
A built-in overcurrent sensor shuts down the supply should any of the three outputs draw more than rated current. The supply resumes operation when the problem clears.

The hermetically sealed metal box prevents high-frequency radio waves from escaping, making FCC certification a cinch. Output voltage feeds back internally through an optical isolator that withstands surges of up to 1600 V dc. That strength makes it easier for the engineers to get their end systems through UL and VDE channels.□

Price and availability

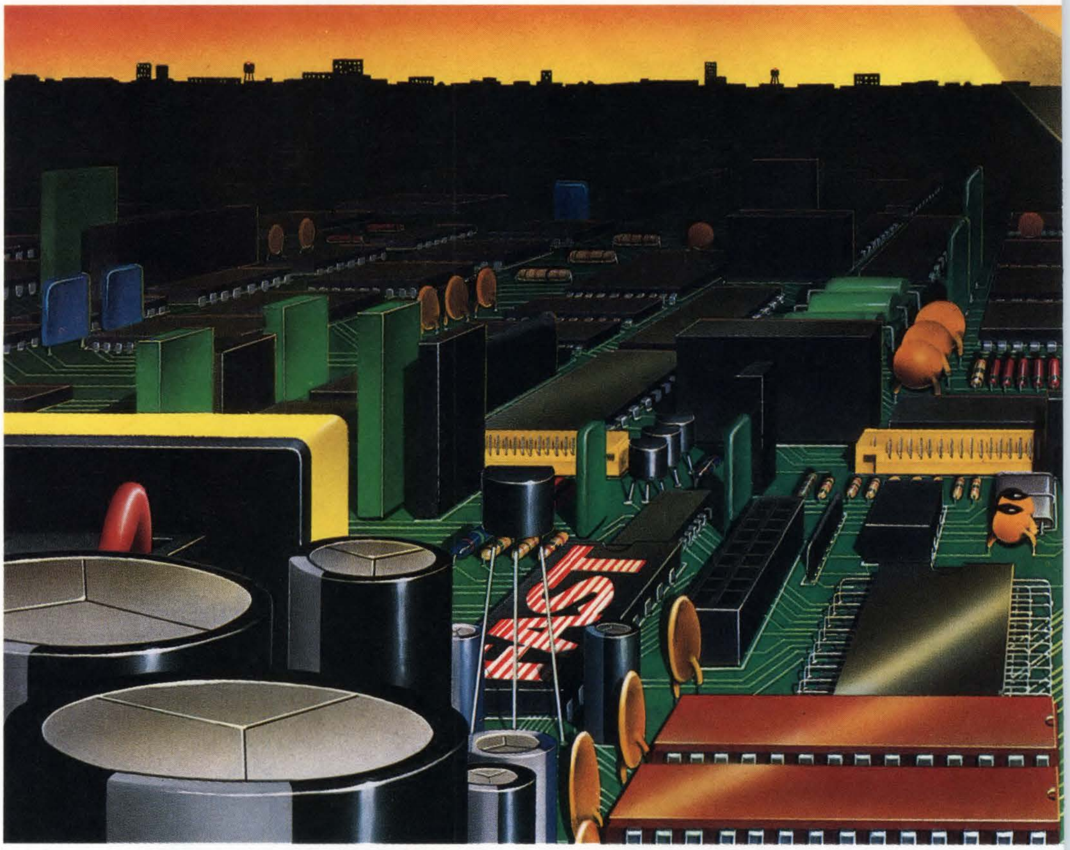
Samples of the HP9503 power supply will be released next month, with full production scheduled to begin in October. The supply sells for $200 in quantities of 100.

National Semiconductor Corp., 2900 Semiconductor Dr., M/S 16-171, Santa Clara, CA 95051; Roy Essex, (408) 721-4013. CIRCLE 512



2. Inside the power supply, a monolithic controller adjusts the switching frequency to generate the output.

Our FASTPLA devices help you get on board. FAST.



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TOSHIBA MEMORY PRODUCT SUMMARY

PART NO.	ORG.	PROCESS	SAMPLES	PROD.	SPEED SORTS AVAILABLE (ns)				PACKAGE OPTIONS
DYNAMIC RAMS									
TMM4164AP	64KX1	NMOS	YES	YES	150	200			P
TMM41256P	256KX1	NMOS	YES	YES	120	150			PT
TMM41257P	256KX1	NMOS	YES	YES	120	150			PT
TMM41464P	64KX4	NMOS	YES	YES	120	150			P
TC511000C	1MbX1	CMOS	YES	YES	100	120			C
TC511000P/J	1MbX1	CMOS	YES	2Q'86	100	120			PJ
TC511001C	1MbX1	CMOS	YES	YES	100	120			C
TC511001P/J	1MbX1	CMOS	YES	2Q'86	100	120			PJ
TC511002P/J	1MbX1	CMOS	YES	2Q'86	100	120			PJ
TC514256P	256KX4	CMOS	YES	2Q'86	100	120			P
TC514257P	256KX4	CMOS	YES	2Q'86	100	120			P
STATIC RAMS									
TMM2114AP	1KX4	NMOS	YES	YES	120	150			P
TMM2016AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2016BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2064P	8KX8	NMOS	YES	YES	100	120	150		P
TMM2063P	8KX8	NMOS	YES	YES	100	120	150		P
TC5504AP	4KX1	CMOS	YES	YES	200	300			P
TC5514AP	1KX4	CMOS	YES	YES	200	300			P
TC5516/17AP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18BP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18CP	2KX8	CMOS	YES	YES	150	200			PFY
TC5565P	8KX8	*CMOS	YES	YES	120	150			PFY
TC5565AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5563AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5564P	8KX8	CMOS	YES	YES	150	200			PY
TC55257P	32KX8	*CMOS	YES	YES	100	120	150		P
HIGH SPEED STATIC RAMS									
TMM2018D	2KX8	NMOS	YES	YES	35	45	55		D
TMM2068D	4KX4	NMOS	YES	YES	35	45	55		D
TMM2078D	4KX4	NMOS	YES	YES	35	45	55		D
TC5561P	64KX1	*CMOS	YES	YES	70				P
TC5562P	64KX1	*CMOS	YES	YES	45	55			P
EPROMS									
TMM2764D	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764DI	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764AD	8KX8	NMOS	YES	YES	150	200			D
TMM27128D	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128DI	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128AD	16KX8	NMOS	YES	YES	150	200			D
TMM27256D	32KX8	NMOS	YES	YES	150	200			D
TMM27256DI	32KX8	NMOS	YES	YES	150	200			D
TMM27256AD	32KX8	NMOS	YES	YES	150	200			D
TC57256D	32KX8	CMOS	YES	YES		200	250		D
TMM27512D	64KX8	NMOS	YES	YES		200	250		D
ONE TIME PROGRAMMABLES									
TMM2464AP	8KX8	NMOS	YES	YES	200				PF
TMM24128AP	16KX8	NMOS	YES	YES	200				PF
TMM24256AP	32KX8	NMOS	YES	YES	200				PF
TMM24512P	64KX8	NMOS	2Q'86	2Q'86	250				PF
MASK ROMS									
TC5364/5/6P	8KX8	CMOS	YES	YES	250				P28
TMM23256P	32KX8	NMOS	YES	YES	150				P28
TC53257P	32KX8	CMOS	YES	YES	200				FP28
TC53512P	64KX8	CMOS	YES	2Q'86	200				P28
TC531000P	128KX8	CMOS	YES	YES	200				P28
TC532000P	256KX8	CMOS	YES	2Q'86	200				P32

P-PLASTIC C-CERAMIC F-FLAT PACK D-CERDIP Y-DIE T-PLCC J-SOJ
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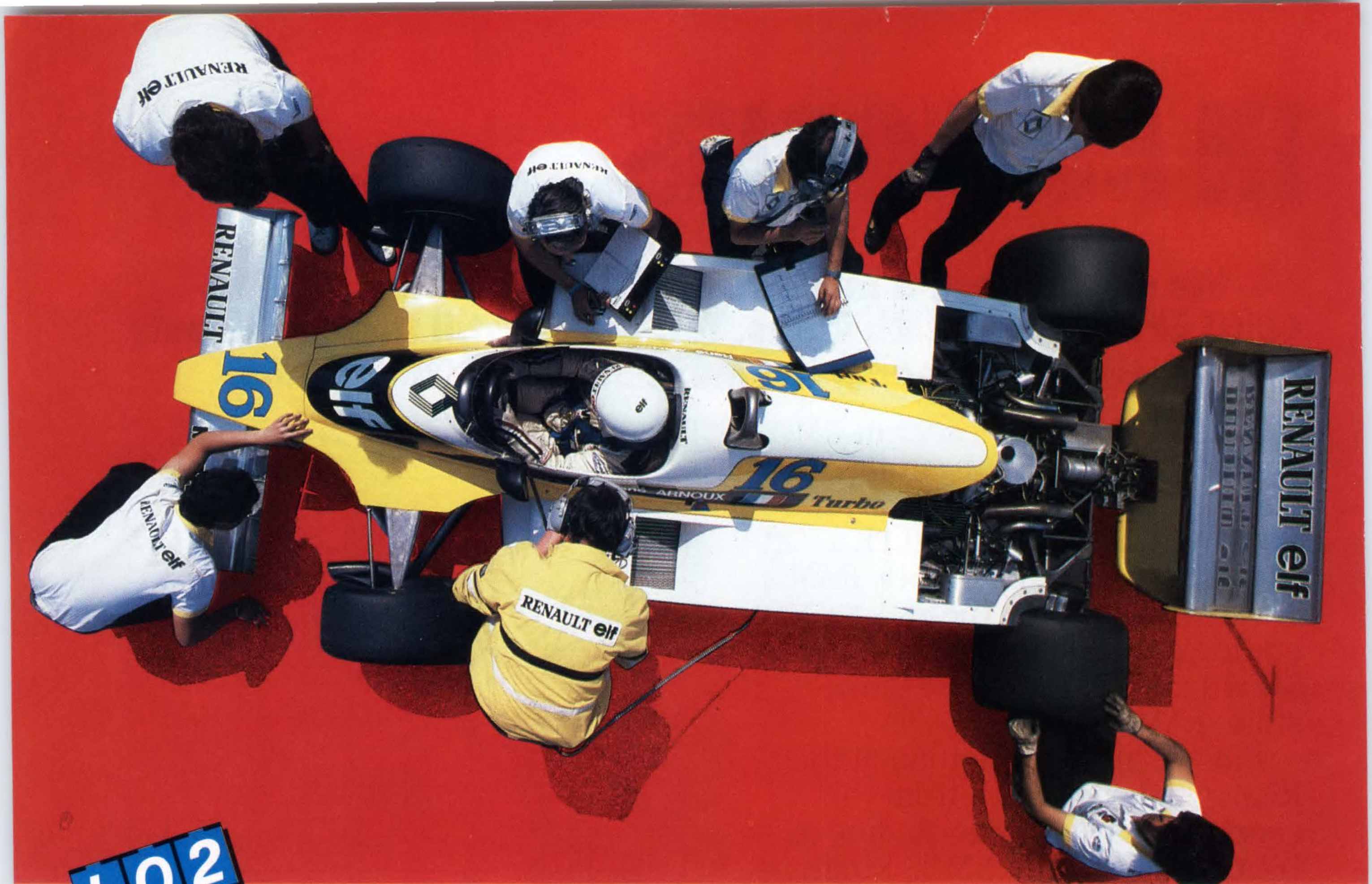
CIRCLE 42



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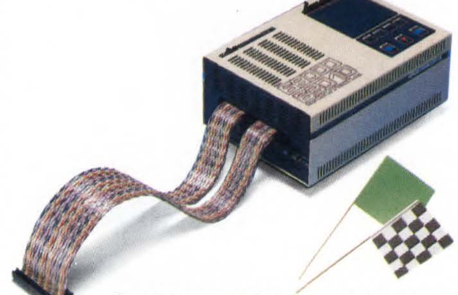

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CIRCLE 43

Video buffer amplifiers get faster and lower in distortion

The needs of flash converters and image systems have pushed buffer bandwidths up to 300 MHz and nonlinearities down to 0.1%.

BY CURTIS PANASUK

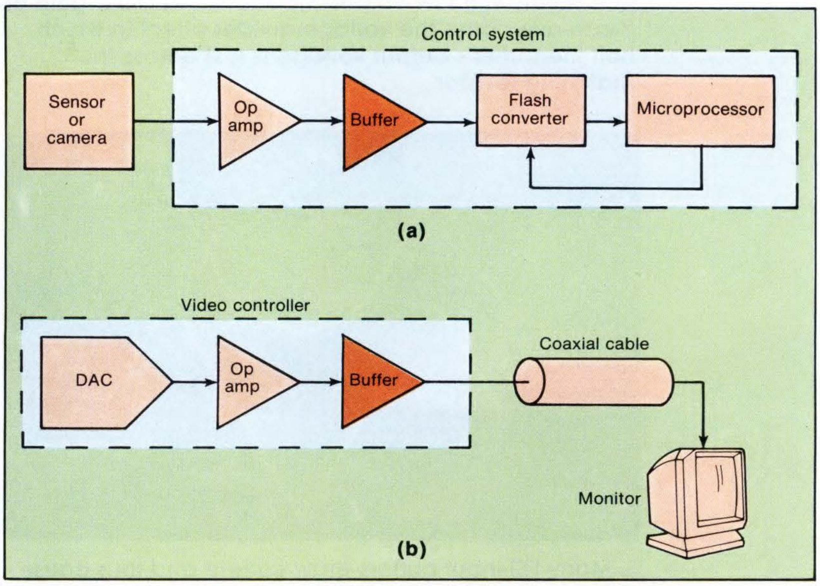
Video buffers are devices that time forgot. In an industry where parts become obsolete in a year, unity-gain power amplifiers have been boosting waveforms with frequencies up to 120 MHz for more than 15 years. Their longevity stems partly from superior design. In addition, the demands of the applications have not changed—at least until now.

Today new tasks, such as driving flash converters and handling computer-generated high-resolution graphics, are forcing improvements in these venerable parts (Fig. 1). Flash converters demand wider bandwidth, higher input impedance, and lower input offset voltage. Imaging systems similarly require wide bandwidths (up to 300 MHz in some cases), high linearity, and low differential phase response. In the not-too-distant past, buffer manufacturers paid little attention to linearity and phase response; thus, those parameters were not measured and specified. Furthermore, users of buffer amplifiers complain that the parts are too pricey.

All that is changing. Manufacturers are introducing radically new designs with improved characteristics. In some instances, such new features as adjustable gain make the buffers a cross between operational amplifiers and traditional buffer amplifiers.

In addition, makers of buffers are increasing hybrid-circuit performance and putting the parts on one chip to lower prices. The new buffers boast bandwidths of 300 MHz for crisp, high-resolution images, along with a nonlinearity of about 0.1% for true picture shading. They also exhibit maximum differential phase characteristics of under 0.1° for accurate colors. (That parameter is usually not specified because it is expensive to measure.) The improved linearity of the new chips makes possible true 6-bit accuracy in flash converters. The better characteristics will also increase the use of buffers for tester inputs and outputs, as well as for powering LEDs in fiber-optic links and driving coaxial cables.

What's more, buffer amplifiers often team up with op amps, their close kin. Voltage-amplifying devices such as op amps become unstable when driving capacitive loads, but current-boosting devices such as buffers can drive capacitance and still remain stable. Thus, to power a



1. Buffers work with incoming and outgoing signals. Signals entering a flash converter's input, which has a high capacitance, need to be buffered (a), as do signals leaving a digital-to-analog converter en route to coaxial cable (b).

Video buffers

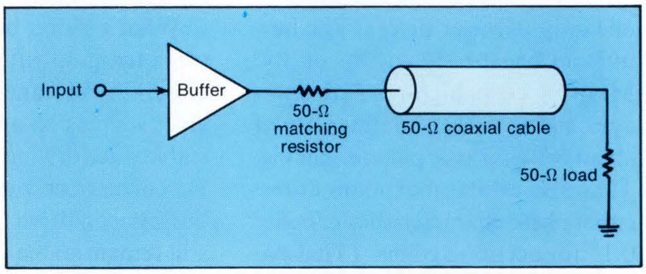
capacitive load, such as a flash converter, an op amp enlists the help of a buffer.

A linear amplifier maintains a constant gain over its operating range, regardless of the amplitude of the input signal. For good imaging performance, maximum nonlinearity is 0.1%. Until now, buffers typically had 2% nonlinearity.

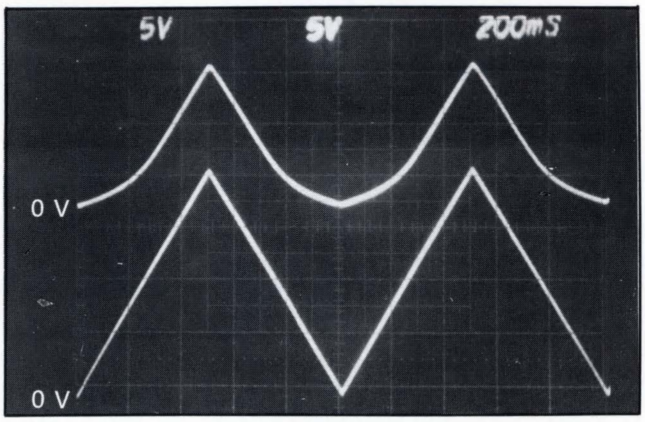
PHASE COUNTS TOO

Just as important as linearity, and also related to amplitude, is differential phase. It is defined as the maximum difference in phase shift that occurs between any two sine-wave amplitudes. For image work, differential phase should be less than 0.1°. The specification of 0.1° is required because TV colors are encoded by the relative phase of picture signals. For example, a signal shift of 5° can change flesh tones to green.

To meet the demands of the new buffer tasks, Elantec modified the monolithic EL2004 amplifier and is introducing the EL2003. Though the new unit sacrifices some of the bandwidth of the older part, it cuts the maximum nonlinearity from 2% to 0.1% and the differential phase from 2° to less than 0.1°.



2. A buffer with low output impedance set to a gain of 2 can overcome the voltage-divider effect in which half the buffer's output voltage is lost across the matching resistor.



3. Many FET-input buffers draw current and thus cause distortion on negative signal excursions (top). Maxim solves the problem by adding an additional FET to the Max460, which easily handles peak-to-peak voltages of 20 V (bottom).

Taking a different approach is Dave Nelson, who worked with signal sources for a long time at Hewlett-Packard. After designing a frequency synthesizer that created some nifty waveforms, Nelson could not find a buffer to serve as a power output amplifier. Existing buffers mangled the waveforms because of poor fidelity.

Since Nelson knew he could build better buffers and amplifiers, he founded Comlinear and dusted off an old idea: current feedback. Though common voltage feedback improves fidelity, it sacrifices bandwidth. If anything, however, bandwidth needs to be increased, since video displays are continually improving in resolution. That, in turn, means faster signals must be sent along coaxial cables.

HAVING YOUR CAKE AND EATING IT

Comlinear's patented topology gives the CLC231 buffer a bandwidth of 165 MHz. The amplifier also has a gain of 2, linearity of 0.1%, and differential phase low enough for video work (ELECTRONIC DESIGN, Nov. 28, 1985, p.125). In addition, its architecture enables the part to maintain a useful bandwidth for gains of up to 5. Since the buffer has gain adjustable—an op-amp feature—it was designated Buff-Amp.

National also has created a version of the Buff-Amp. The LH4004 combines adjustable gain from 1 to 5 with a bandwidth of 150 MHz. The chip is based on a series-shunt triple circuit, which, as with the Comlinear amplifier, uses current feedback to give high gain and wide bandwidth. The company does not specify linearity or differential

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CIRCLE 44

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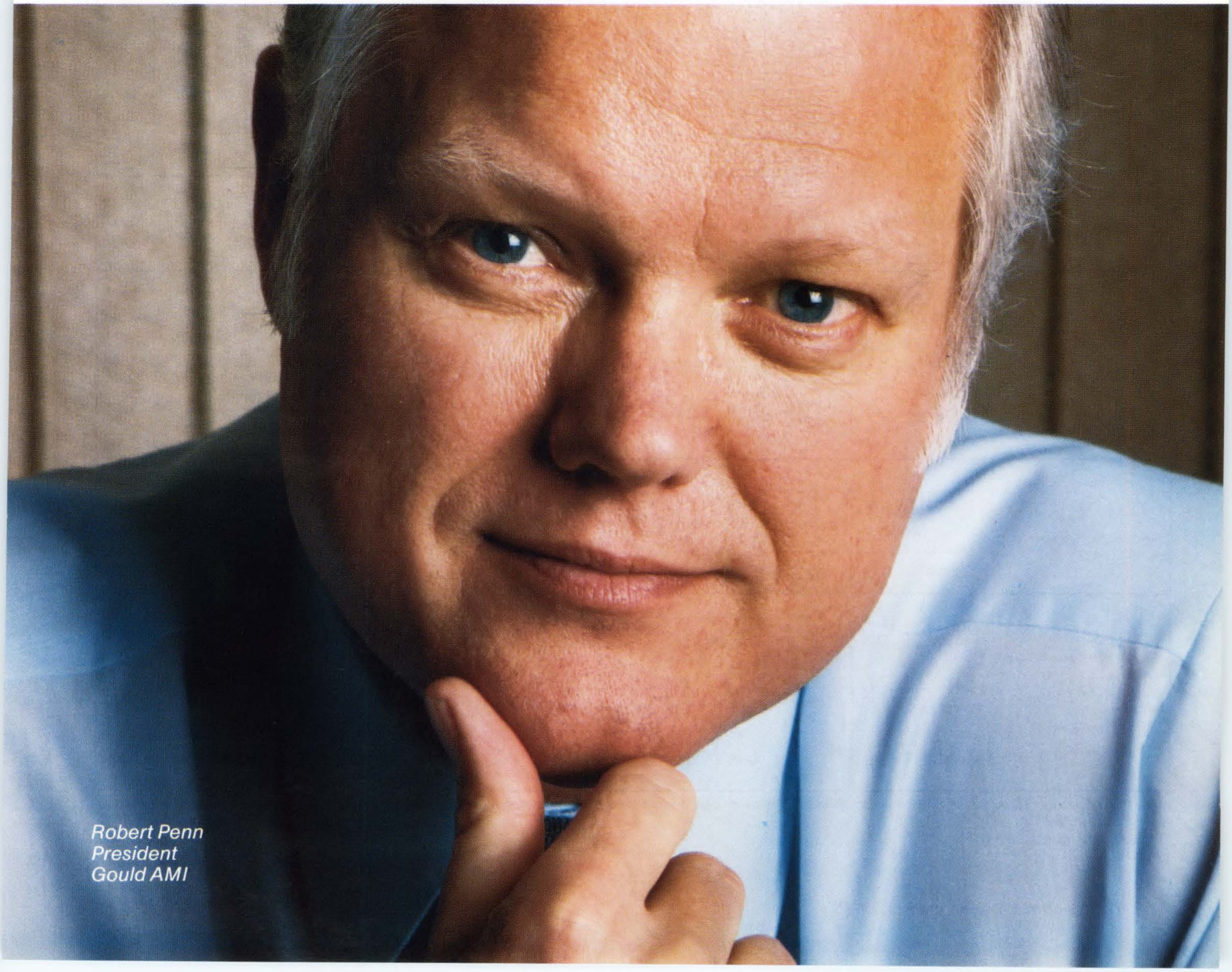

Video buffers

phase. With a FET input stage, National achieves an input resistance of $1 \times 10^{12}\ \Omega$, beating the CLC231 from Comlinear at $4 \times 10^5\ \Omega$.

In the parts from National and Comlinear, devices can be inserted in their feedback loops. National points out that a diode can be inserted to form a peak detector with one-quarter the number of components of a conventional peak detector made from an open-loop buffer. For its part, Comlinear notes that a laser diode could be included in a buffer's feedback loop. Doing so improves fiber-optic communications by enhancing the temperature stability and widening the system's dynamic range.

The adjustable gain offered by National and Comlinear solves a persistent problem in video signal distribution: the voltage-divider effect. To minimize reflections, 50-Ω matching resistor is inserted between a buffer with low output impedance and the coaxial cable (Fig. 2). With this arrangement, half the output voltage is dropped across the matching resistor so only half reaches the load. To overcome the division of the voltage and subsequent loss in transferred power,

Directory of buffer amplifiers

Company	Model	Bandwidth into 100 Ω (MHz)	Slew rate: guaranteed; typical (V/μs)	Nonlinearity	Input impedance (Ω)	Gain at 100 Ω	Continuous output drive current (mA)	Quiescent power consumption	Price in lots of 100	Features	Circle
Analog Devices Corp. Route 1 Industrial Park Norwood, MA 02062 (617) 329-4700	HOS-100	125	1000; 1500	2%	2×10^5	0.95	±100	±5–±15 V, ±13 mA	$14		451
	HOS-200	200	1100; 1500	2%	1×10^5	0.95	±100	±5 V, ±16 mA	$14		
	ADLH0033	100	1000; 1500	2%	1×10^{11}	0.98	±100	±5–±15 V, 20 mA	$16		
Burr-Brown Corp. P.O. Box 11400 Tucson, AZ 85734 (602) 746-1111	3553A	300	2000; 2500	N.s.	N.s.	0.96	±200	±5–±20 V, ±50 mA	$22.45	FET input gives high input impedance and low bias current	452
Comlinear Corp. 4800 Wheaton Dr. Ft. Collins, CO 80525 (303) 226-0500	CLC300	85	3000*	N.s.	1×10^5	±1–±40	100	±5–±15 V, ±24 mA	$39	Feedback gives variable gain	453
	CLC231	165	2500; 3000	0.1%	4×10^5	±1–±5	100	±5–±15 V, ±18 mA	$105	Feedback gives variable gain, good linearity, and good differential phase	
Elantec Inc. 1996 Tanob Ct. Milpitas, CA 95035 (408) 945-1323	EL2003	150	600; 1200	0.1%	1×10^6	0.93	100	±5–±15 V, ±15 mA	$3.45	Emphasis on keeping linearity below 0.1%; monolithic	454
	EL2004	200	2000; 2500	2%	1×10^{10}	0.92	250	±5–±15 V, ±24 mA	$21	Monolithic	
Harris Semiconductor Corp. 1025 W. Nasa Blvd. Melbourne, FL 32919 (800) 442-7747 x1750	HA-5002	110	1000; 1300	N.s.	1.5×10^6	0.97	±100	±12–±15 V, ±10 mA	$4	Monolithic	455
	HA-5033	250	1000; 1300	N.s.	1.5×10^6	0.93	±100	±12–±15 V, ±25 mA	$5	Monolithic	
	HA-2542	60	3000; 3075	0.1%	1×10^5	2 or more	±100	+15 V, ±35 mA	$6.39	Good linearity and good differential phase	

Note: This is a representative sampling of buffer amplifiers and manufacturers; it is not meant to be a definitive list.
N.s. = not specified
*Typical only; **guaranteed only

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CIRCLE 45

GOULD
Electronics

Video buffers

the Buff-Amp can be set to a gain of 2.

Though building in the 50-Ω matching resistance would seem a natural step, it would limit the device's flexibility. The part could not drive several cables at once when the parallel impedance of the cables is less than 50-Ω. A built-in resistance also interferes with applications in which high-capacitance loads must be driven. There, a series resistance would limit the current needed to quickly charge and discharge the capacitive load.

Wherever a flash converter exists, a buffer is likely to be found as well. It is well suited for driving the converter's highly capacitive input. In a sensing system, the sensor signal typically feeds through a buffer and into the converter. Sensors with weak outputs will usually pass through an op amp, then into a

Directory of buffer amplifiers (Cont'd.)

Company	Model	Bandwidth into 100 Ω (MHz)	Slew rate: guaranteed; typical (V/μs)	Nonlinearity	Input impedance (Ω)	Gain at 100 Ω	Continuous output drive current (mA)	Quiescent power consumption	Price in lots of 100	Features	Circle
Linear Technology Corp. 1630 McCarthy Blvd. Milpitas, CA 95035 (408) 942-0810	LT1010	20	75**	N.s.	1×10^5	0.90	±150	±2.5–+20 V, 9 mA	$2.85	Superlow operating voltage	456
Maxim Integrated Products Inc. 510 N. Pastoria Sunnyvale, CA 94086 (408) 737-7600	BB3553	300	2000, 6000	1%	1×10^{10}	0.93	250	±15 V, ±80 mA	$23	Current limited output	457
	MAX460	80	1000; 1500	1%	1×10^{10}	0.95	±100	±5–±15 V, 20 mA	$19.80		
	LH0063	300	2000; 6000	1%	1×10^{10}	0.93	250	±5–±15 V, ±22 mA	$23.80	Static discharge protection	
	LH0033	80	1000; 1500	1%	1×10^{10}	0.95	100	±5–±15 V, ±22 mA	$17.34		
National Semiconductor Corp. 2900 Semiconductor Dr. P.O. Box 58090 Santa Clara, CA 95052-8090; (408) 721-5856	LH4003	230	750; 900	N.s.	2×10^3	0.98	±40	±6 V, ±40 mA	$54	Feedback architecture	458
	LH4002	200	1000; 1250	N.s.	1.5×10^4	0.93	40	±5 V, ±30 mA	$18.25		
	LH4004	150	700	N.s.	1×10^{12}	±1–5	50	±12 V, ±30 mA	$67	FET input gives high input impedance; feedback gives variable gain	
	LH0033	60	850	N.s.	1×10^{12}	0.98	±100	±12–±20 V, ±20 mA	$16.50		
Teledyne Philbrick 40 Allied Dr. Needham, MA 02026-9103 (617) 329-1600	TP1359	80	1300	N.s.	1.5×10^6	0.93	±100	±12–±20 V, ±25 mA	$15	Monolithic	459
	TP0033	100	1000; 1500	N.s.	1×10^{10}	0.98	±100	±5–±20 V, ±22	$39		
	TP1490	100	N.s.	N.s.	1×10^{12}	0.99	±100	±12–±18 V, ±125	$114		
VTC Inc. 201 E. 86 St. Bloomington, MN 55420 (612) 851-5000	VA033	200	1500; 1800	0.1%	8×10^5	0.95	±100	±5 V, ±48 mA	$8.90	Surface-mountable; monolithic, using junction isolation	460

Note: This is a representative sampling of buffer amplifiers and manufacturers; it is not meant to be a definitive list.
N.s. = not specified
*Typical only; **guaranteed only

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CIRCLE 46

buffer and into the converter. For this job, the buffer must have good linearity, just as in the image operations. In the case of a 6-bit converter, the buffer must have no more than 0.78% nonlinearity to preserve the least significant bit.

SAVING POWER

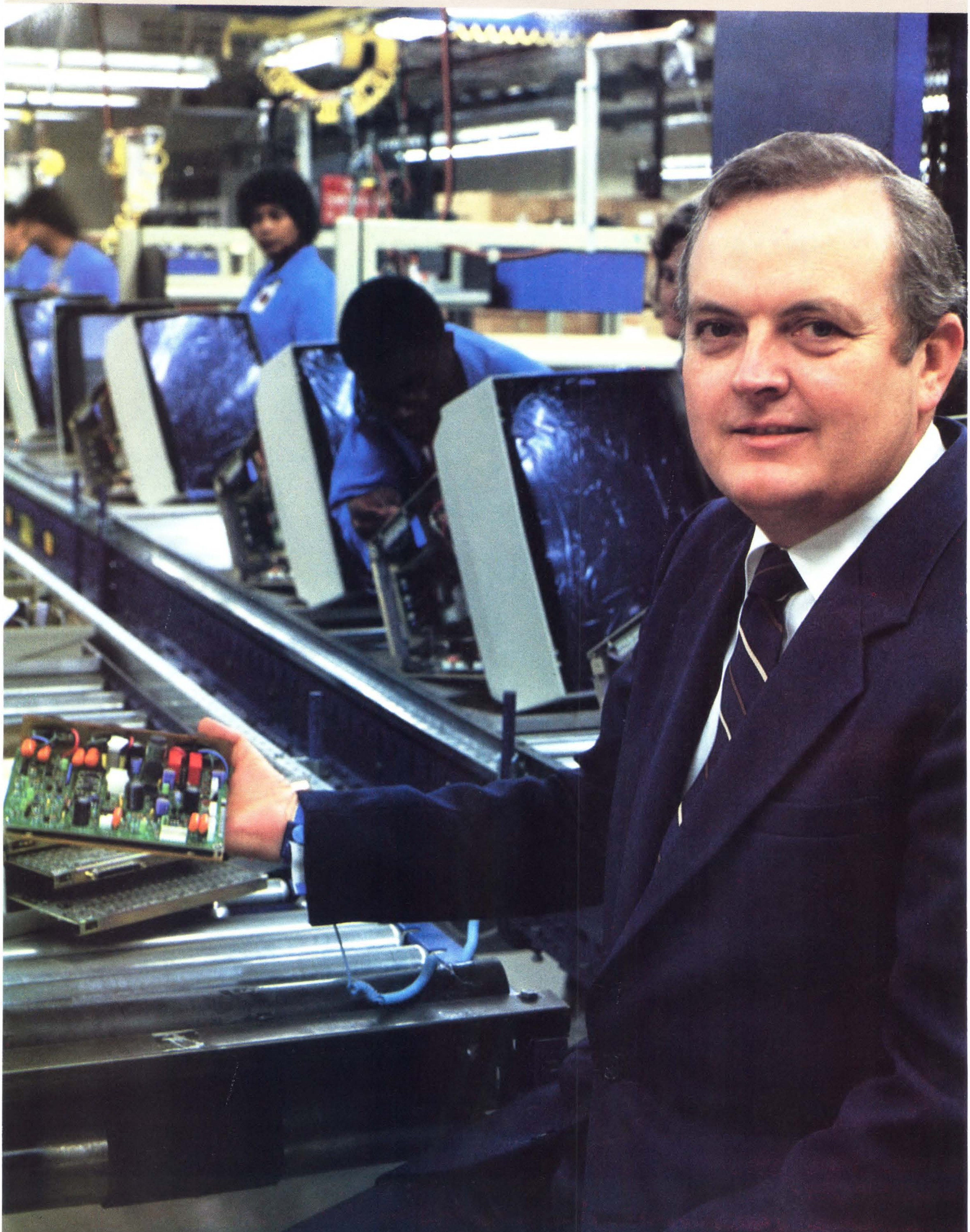
For cases where a sensor leads directly into the buffer, that buffer must exhibit an input impedance on the order of $1 \times 10^{10}\ \Omega$ to avoid disrupting the sensor operation. Several manufacturers use FET inputs on buffers to raise input impedance, but most of the parts fall short in fidelity. Maxim was the first company to recognize that FET inputs suffer excess current flow with negative voltage. This effect occurs when the gate-drain junction becomes reverse biased to the extent that negative current begins to flow (Fig. 3, top). Maxim's next-generation device, the Max460, has an extra FET to cancel the reverse-bias effect (Fig. 3, bottom).

Both Elantec and Maxim include protection circuits in the amplifiers that sense when too much current is being drawn, and shut down the device before it self-destructs. In flash conversion, the mechanisms prevent damage should a short develop on the board. For driving cables, automatic shut-off becomes even more important, since shorts are fairly common in long cables, especially if they are out in the open where they can be crushed by heavy vehicles or gnawed by rodents.

Power consumption affects all buffer applications. Since buffers are current-output devices, current cannot be reduced without impairing performance. In this case, the device's power consumption is reduced by lowering the supply voltage. Several manufacturers offer supply voltages as low as ± 5 V.

When comparing buffer specifications, buffer shoppers must be sure that the numbers reflect the same load conditions. For example, a 1% linearity for a 1-kΩ load pales in comparison with a 1% linearity for a 100-Ω load.

One-chip buffers from Elantec and Harris rely on dielectric isolation for sufficiently fast pnp transistors. Though not an inexpensive process, dielectric isolation is less costly than building a hybrid. Its widespread use may soon make buffers cheaper, as well as better. □



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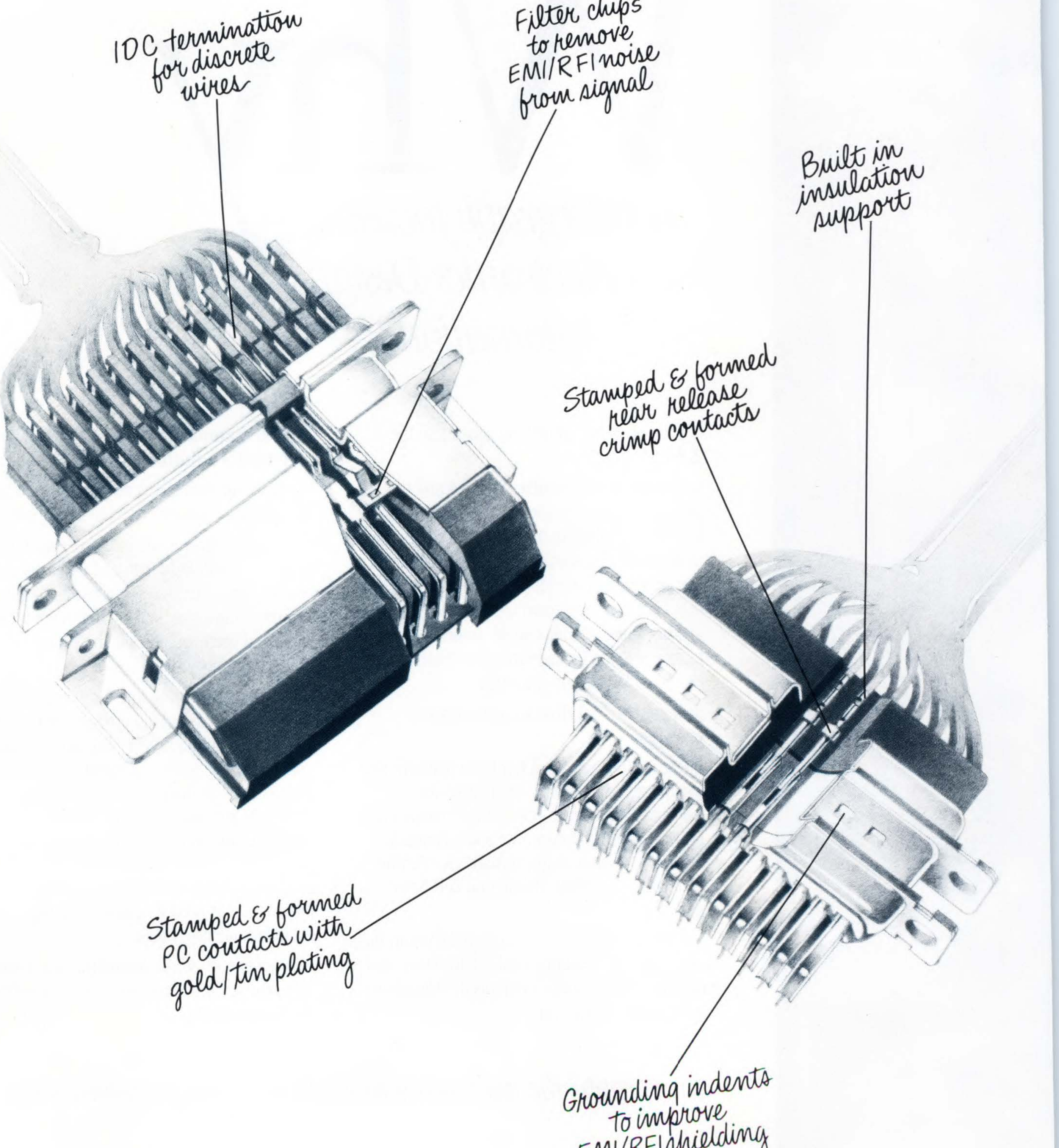
CIRCLE 50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CIRCLE 51

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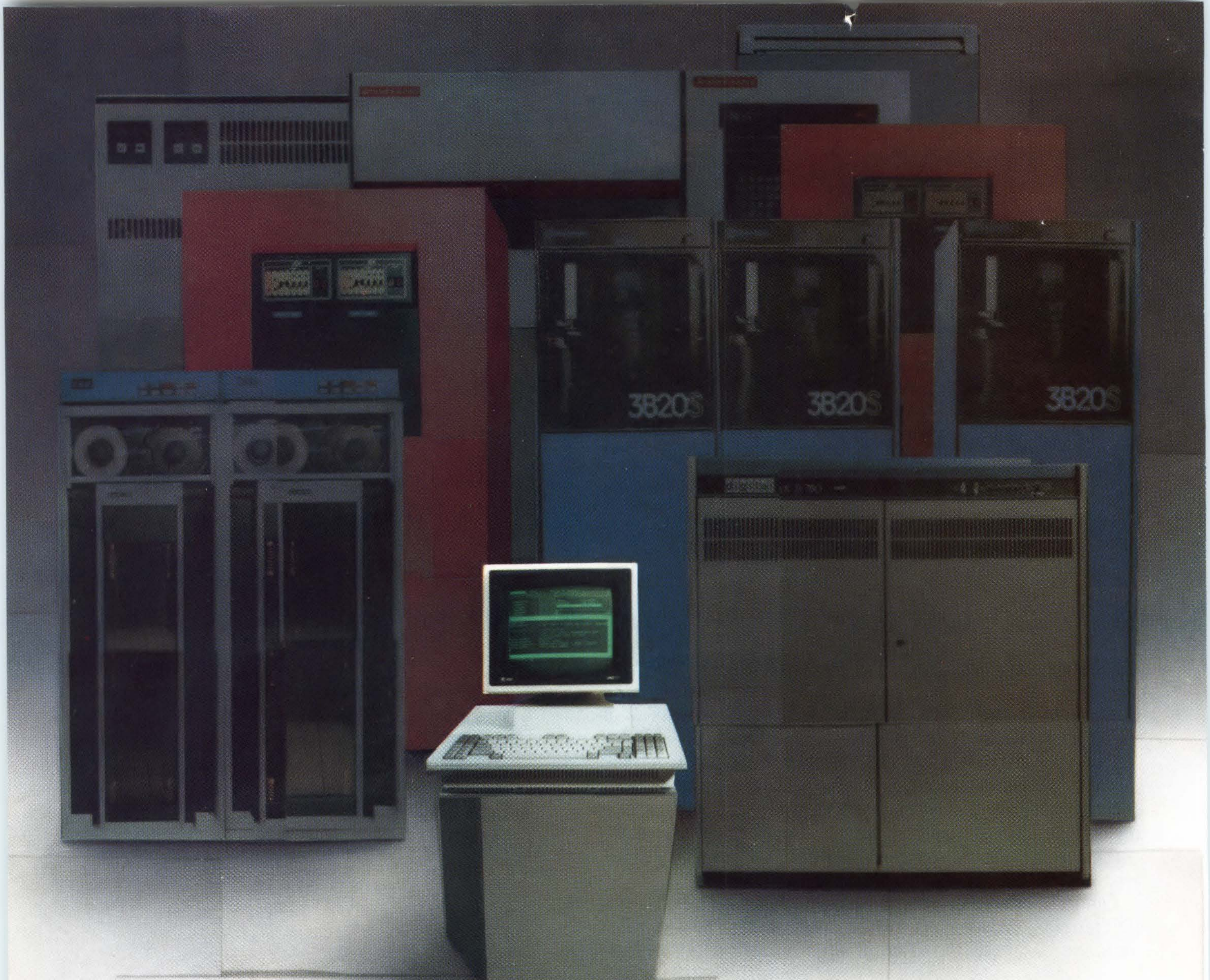
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NCC Preview

Engineers attending NCC '86 in Las Vegas, June 16–19, can pick from more than 100 technical sessions exploring the latest hardware and software. Further piquing their interest will be 500 or so exhibits at the Las Vegas Convention Center and Hilton Hotel. Following a preview of the technical sessions, a look at some exciting new products begins on p. 107.

For designers looking at the rapidly changing world of engineering workstations, it can be a bewildering view. Before them lies a staggering number of products offering everything from phenomenal performance to petty-cash prices. No wonder designers are constantly up against the question of what is best for them today and, of course, in the future.

Designers may well find some answers at this year's National Computer Conference, where sessions devoted to the trends in hardware and software should bring the workstation picture into clearer focus.

Workstations, though, are by no means the only topic that should draw attention. Also high on the agenda are sessions on mass memories, new computer architectures, graphics, local-area networks, new software,

Martin Gold

and artificial intelligence (see the table, p. 104). Designers will also get a look into the future of computer-integrated manufacturing.

Not long ago, the bulk of analytical processing was performed on mainframe computers, such as the IBM 370 series and very large systems like Control Data's 6000 series. Today, many such tasks are running on microprocessor-based workstations and superminicomputers, as well as on traditional mainframes and minicomputers. But the plethora of 32-bit microprocessors, board-level subsystems, and new memory chips and mass-memory subsystems has confused the issue of which type of system is best for a specific application.

Right now, designers can choose from three classes of workstations: high-end graphics-oriented systems, mid-range products likely to be based on a RISC architecture, and low-end systems such as today's IBM PC AT. Speakers will zero in on the price-performance trade-offs of the three classes, where overlapping now occurs and will remain for years to come.

It has been said that there will never be enough memory storage to thoroughly satisfy the appetites of all computer users. Emerging storage technologies could help fill the seemingly insatiable demand. One session in particular will focus on high-capacity rigid-disk subsystems and optical disks as well as on the trend toward mixing semiconductor and magnetic memories. Designers should get an idea of when compact-disk ROM and other types of optical memories will be ready for use in future systems.

How much computing capability is needed to handle different analytical jobs will be examined by users from several industries. They will review the newer architectures, such as parallel processing for mainframes, minicomputers, microcomputers, and microprocessor-based workstations. Moreover, they will deal with costs, connectivity between applications, evolving standards for shifting a computer system from one application to another, and the availability of software for specific types of computer systems.

Several sessions will deal with topics like local networks, international networks, cabling systems, and communication between microcomputers and mainframes. Besides going over basic design concepts, speakers will relate real-life examples.

For more general interest, engineers will kick around issues like government regulation, computers in education, and whether there will be a shakeout of existing operating systems. In some instances, panelists from various industries will relate how they solved their computing problems.

Highlighting the software segments of the program will be the so-called fourth-generation languages and application generators. Programming languages designed to establish communications between people and computers have traditionally been much more accommodating to the computer than to the programmer. Consequently, computer programming still tends to be tedious and time-consuming. One session investigates the gains in programming productivity. Another tries to answer the question: Are application programmers becoming obsolete? The futures of Unix, Ada, and Cobol come under the microscope in still another part of the program.

A cluster of sessions will weigh artificial intelligence and its application in CAD and CAM. And the question of whether expert systems can be used effectively with microcomputers will be considered.

Furthermore, designers will take an in-depth look at the languages and software techniques employed in AI-based systems. Sure to be considered are the relationships of Lisp and Prolog to conventional programming languages and high-level knowledge representation languages. □

Highlights of NCC '86 sessions

Time	Monday, June 16	Tuesday, June 17	Wednesday, June 18
8:30 a.m. to 10 a.m.		Contemporary applications of speech technology Parallelism and its use in supercomputers Expert systems in mainframes and minicomputers	Judging the real availability of emerging storage technologies and architectures Trends in graphics and workstation technology
10:30 a.m. to noon		Fourth-generation languages and application generators The implications of optical storage within the automated office	Views on future data bases and graphics Electronic mail
1:30 p.m. to 3 p.m.	Integrated Services Digital Networks (ISDNs) Local-area networks	The future of CAD/CAM productivity Cabling systems and communication between microcomputer and mainframes	Programming languages for artificial intelligence
3:30 p.m. to 5 p.m.	The marriage of expert systems and simulation Telecommunications in the information age	Semiconductor directions in connectivity AI microcomputer applications in CAD/CAM	Networking software

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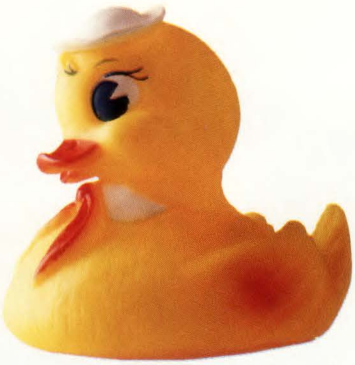

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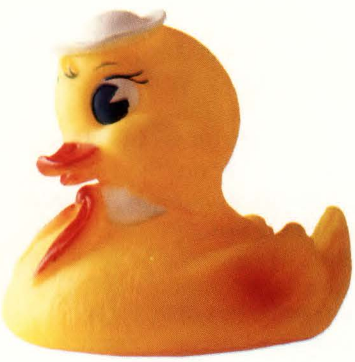

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CIRCLE 54

Cache memory, burst keep Multibus II controller on fast track

One of the first disk controllers for Multibus II systems uses a number of techniques—including caching and a burst mode—to guarantee high-speed. Ciprico's Rimfire 2200 board also controls two SMD drives, as well as up to seven SCSI-compatible tape or disk drives.

The controller for the 32-bit bus carries either a 128- or 512-kbyte cache. Using a look-ahead technique, the board selects information to be stored in the dynamic RAM cache, pulling sequential data that follows the data requested by the host. Users can determine how this data will be retrieved, calling for full disk sectors or such logical units as 4- and 8-kbyte increments. Depending on the configuration, the cache hit rate can be as high as 90%.

The 2200 employs a gate array to quickly transmit small amounts of data, keeping the bus free for other devices. This burst feature transmits up to 32 bytes at 10 Mbytes/s, much faster than the 6 Mbytes/s used for sustained transfers. In some instances, large files can be transferred in a series of short bursts, leaving the bus open part of the time instead of locking it up for a lengthy transmission at the lower rate.

To further speed system throughput, the board holds commands from the host in a queue. This technique lets the host quickly offload commands, optimizing performance by eliminating unnecessary steps. For instance, if the host calls for five sequential files, the controller will combine the five retrieval commands into one, thus minimizing head movement and communication time. An Intel 80186 handles this and other housekeeping tasks.

The card is designed for 24-MHz SMD drives but is fitted with an SCSI port to simplify integrating the tapes needed for backup. Since up to seven devices can tap into this port, both disk and tape drives can be attached.

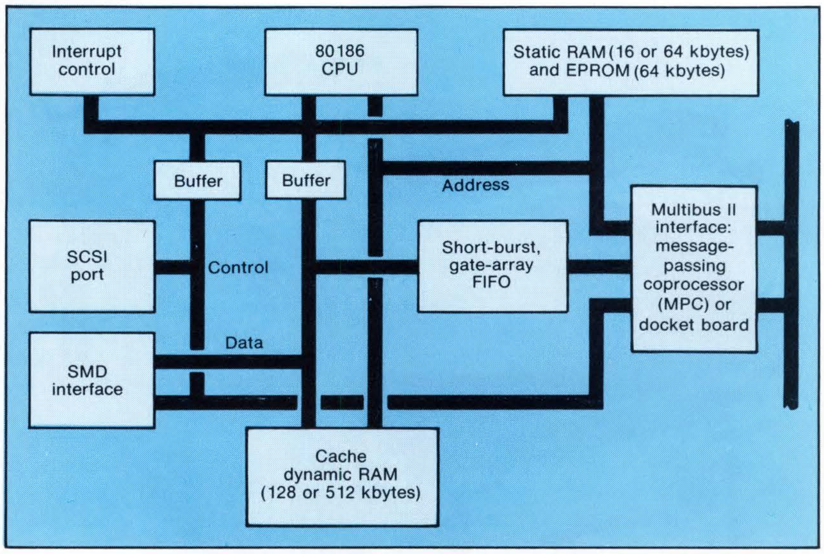
A monitor logs the number and type of commands from the host and the number of cache hits and other statistics. That information can be used to alter the system configuration to improve performance. The card also incorporates 48-bit error correction coding and the scatter/gather commands used in multitasking.

A 5-V version of the 2200 draws 10 A maximum; the 12-V model draws less than 1 A at all times. A model which uses a small daughter board for interfacing will be offered until the Message Passing Coprocessor, which is being developed specifically for Multibus II communications, becomes available later this year. Preliminary pricing is under $4000 in small OEM quantities. Production shipments will begin in July.

Ciprico Inc., 2955 Xenium La., Plymouth, MN, 55441; Stu Reile, (612) 559-2034.

CIRCLE 323

BOOTH A1852



Ciprico's Rimfire 2200 uses an 80186 processor to manage the static RAM cache and communications between the host and the board.

Terry Costlow

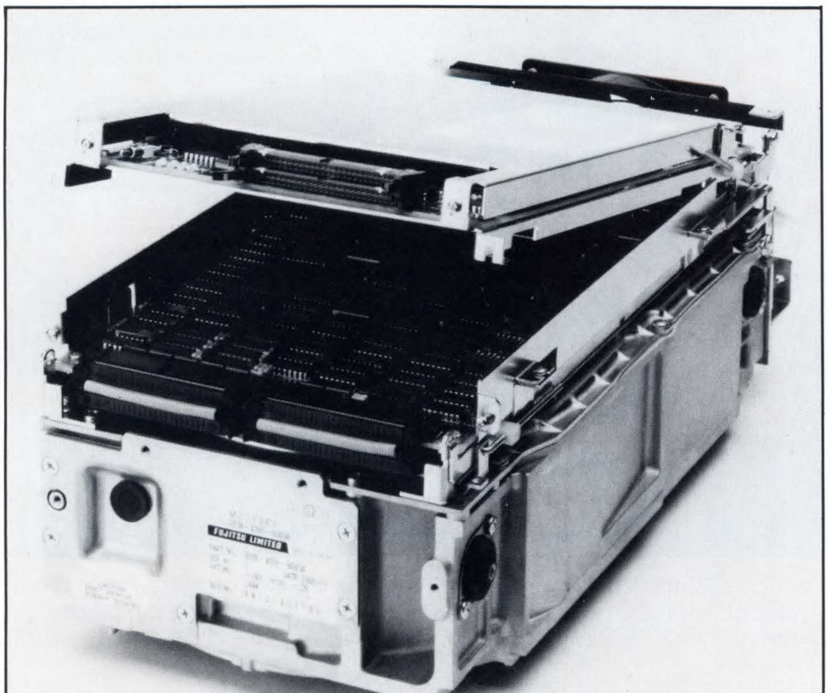
SCSI controllers have the muscle to handle 1.3 Gbytes at one node

Designers who assumed that the embedded SCSI (Small Computer Systems Interface) controllers were strictly for low-end hard-disk drives will reevaluate their opinions when they see Fujitsu America's trio of controller boards. The M1053B and M1053B-D are meant to ride piggyback on Fujitsu's M2333 hard disk drives—8-in. drives with 337 Mbytes of formatted capacity. In fact, up to four of these drives can be daisy-chained to the same controller, delivering up to 1.35 Gbytes on the same SCSI node.

Both the M1053B and M1053B-D respond to the full SCSI common command set, though the latter's differential cable drivers and receivers furnish slightly better noise immunity over longer cables. The SCSI common command set embodied in the M1053B controllers allows the disk drive to be addressed as intelligent I/O device, regardless of capacity, and to off-load data management tasks from the host computer. All devices responding to the common command set (regardless of manufacturer) will accept FORMAT, READ, WRITE, READ CAPACITY and SEND DIAGNOSTIC commands from the host. An extended read and extended write command facilitate the transfer of very large data blocks between host and disk drive.

Stephan Ohr

Engineers can select a one-to-one sector interleave (for the highest performance) or may increase the interleave up to nine times. The sectors may be set at 256, 512, or 1024 bytes. The SCSI bus transfers asynchronous data at 1.5 Mbytes/s; synchronous data is passed at up to 2.5 Mbytes/s. Between the controller and the drive is an H-SMD interface, which allows a 2.458-Mbyte/s transfer.



The M1053B and M1053B-D controllers will be available late in the summer. A version of the SCSI controller board for the popular Fujitsu Eagle XP, a 689-Mbyte $10^1/_2$-in. H-SMD drive will also be available later this year. The card, the M1053E-D enables up to four eagles to be daisy-chained, providing a record capacity of 2.75 Gbytes at one SCSI node.

Fujitsu America also will introduce an IPI-2 interface for its 337-Mbyte 8-in. drive. The new drive, the M2333-P, supplies the 16-bit data path called for in the IPI specifications and works with up to 50-meter cables. However, the M2333-P will not implement the full 10-Mbyte/s IPI transfer rate. Instead, it will settle for 2.46 Mbytes/s, the same as today's H-SMD drives.

Pricing for the SCSI controller cards was not set by press time. That information can be obtained from the company.

Fujitsu America Inc., 3055 Orchard Dr., San Jose, CA 95134; Mike Gamerl, (408) 946-8777.

CIRCLE 318

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NCC Products

Optical disk subsystem edits and revises data on write-once disks

An optical disk subsystem is proving the term "write once" something of a misnomer, since it enables the computer system in which it is installed to revise data stored on such disks. That ability enables users to side-step expensive systems that employ erasable optical disks. Further, Zetaco's LRS-10 incorporates an SCSI controller board that is compatible with most Data General systems, thereby simplifying integration with that equipment.

The controller board uses dual processors and a full megabyte of RAM to handle what is called a "scrub/append" operation, which blocks out obsolete data and places updated information on another area of the disk. When the data is changed, a flag bit is written on the disk before the unwanted data. When the drive subsequently reads the flag bit, it will check the controller's memory for the location of the revised data.

Terry Costlow

To keep throughput rates from falling sharply during those searches, the controller processes communications between the drive and the host in parallel. An 80186 handles all exchanges with the host, and a bit-slice processor manages SCSI commands. The worst-case access time is 330 ms. Single track accesses, which represent best-case scenarios, take 8 ms, and the average access time is 150 ms. The data transfer rate can reach a maximum of 1.2 Mbytes a second.

The basic subsystem stores 1 Gbyte. Capacity can be expanded by adding another drive (the controller can handle four drives) or by adding a juke box mechanism that switches platters. The latter technique lets users access data stored on up to 20 platters. In this application, the controller card will store addresses and other data for each platter. Since the controller operates with any SCSI drive, a magnetic disk can be added for storage of data that will change often.

The optical disk subsystem is compatible with Data General's Argus disk emulation software, operating under the AOS/VS, RDOS, and AOS operating systems. The first versions of the board will fit Data General's MV series computers, with versions for other systems being introduced throughout the coming year.

The controller card draws 8 A at 5 V. The drive's power consumption, as well as track density and other guidelines, will depend on the type of drive used. The optical disk package will have a maximum size of 19 by 26 by 10.5 in.

Subsystems will vary with configuration and capacity; the base price of a single LRS-10 is $25,000. OEM discounts are available. Delivery takes 30 days.

Zetaco Inc., 6850 Shady Oak Rd., Eden Prairie, MN 55344, (612) 941-9480.

CIRCLE 324

BOOTH C3544

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See us at Electro Booth #2102/2104.

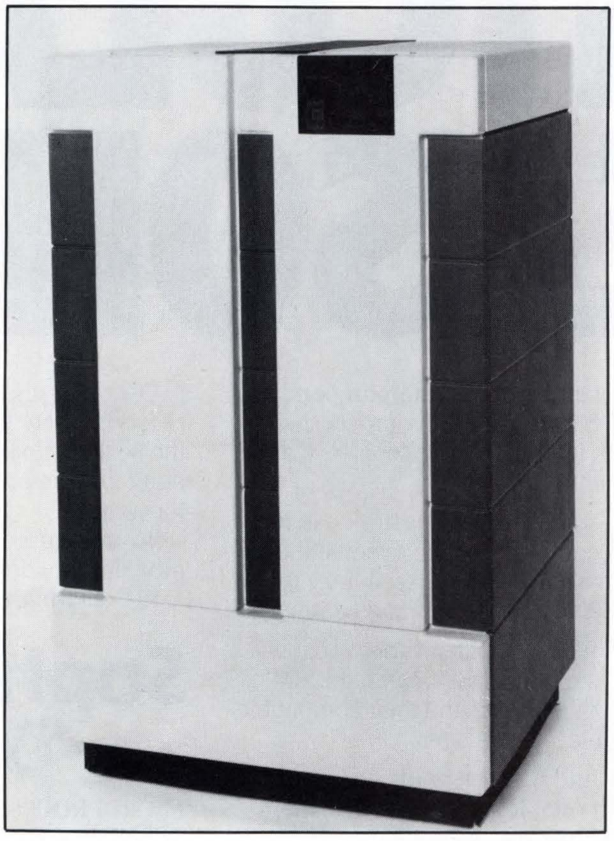
Uninterruptible regulated supply feeds computers up to 480 kVA

One of the first fully electronic uninterruptible power supplies able to compete with large motor generators, delivers from 15 to 480 kVA to mainframe and minicomputer installations. The Upstar system, designed at Modular Power, is intended for mainframes operating with 208, 220, 380, 415, 460, or 480 V ac (three-phase) at frequencies ranging from 32 to 512 Hz.

Upstar performs two functions: It regulates the line voltage to the computer system in the event of a brownout or momentary loss of power. It also converts battery power into usable ac power in the event of a complete loss of ac line voltage. The output voltage regulation is within ±2% for a 25% line power drop; ±5% for a 50% drop; and ±8% for a complete power loss.

Stephan Ohr

In the operation of the uninterruptible power supply, ac is converted to dc and back to ac again. Any power-line disturbance is corrected by a dc battery back-up. The Upstar's 50-kHz switching frequency reduces size, increases efficiency, and allows the unit to recover to 1% of the full power in 50 ms.



The supply's design eliminates line frequency transformers and uses a number of digital LSI components, thus decreasing the size and increasing the efficiency of the unit. With an overall efficiency of 94% and a power factor better than 0.96, Upstar actually wastes less line power than conventional uninterruptible power supplies or motor generators. Uninterruptible systems generally deliver an efficiency in the range of 82% to 92%, with a 0.75 or 0.80 power factor. Motor generators are 85% efficient, with a 0.50 to 0.85 power factor. On a 100-kW system, Upstar's power savings can be close to 100 megawatt-hours each year.

The units are built around 9 by 9 by 16 in. modules that furnish up to 15 kVA of power backup. Up to 32 modules can be connected for a total output of 480 kVA. The cabinets housing these modules are usually 34 in. wide and 38-in. deep, varying in height according to the kVAs required. It's ambient noise is less than 60 dB.

The Upstar carries a 200,000-hour MTBF rating and includes a microprocessor-controlled monitoring system. Changes in conditions are recorded and displayed on an integral, or remote, CRT.

Prices for the system start at $30,000. Delivery is within 90 days.

Modular Power Corp., 1150 Ringwood Ct., San Jose, CA 95131; Christine Effinger, (408) 263-7010.

CIRCLE 320

BOOTH B3316 and B3318

ROCKWELL SEMICONDUCTOR TECHNOLOGY SOLVES T-1/CEPT IMPLEMENTATION IN A CMOS CHIP.

Replace up to 100 MSI devices with the world's first single-chip PCM transceiver.

Designed for worldwide primary rate applications, the R8070 from Rockwell International is a telephony breakthrough. This single-chip solution accommodates all primary telephone carrier requirements in both North America and Europe. The R8070 T-1/CEPT operates with AT&T extended framing, Clear Channel, and European CEPT formats.

Save on power, design engineering and component costs.

As a single-chip, CMOS transceiver, the R8070 minimizes board space requirements with its VLSI implementation. It significantly reduces power consumption, saves on component costs and reduces engineering design investment as well. To find out how the R8070 can help you build your next generation T-1/CEPT communications system, talk to your Rockwell distributor or sales representative or send for complete technical literature today.

Semiconductor Products Division
Rockwell International, P.O. Box C,
M.S. 501-300, Newport Beach, CA 92658-8902
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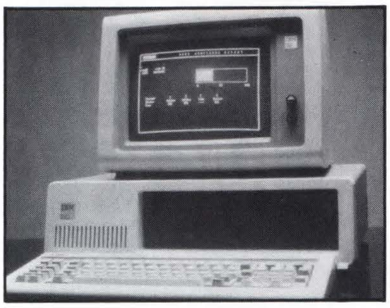
General Industries / A-B Industrial Automation

CIRCLE 57

Voice mailbox starts PC XT talking



To date, voice mailbox systems have been restricted to high-performance and expensive Multibus and VME-based designs. The cost of such systems has taken a sharp drop, thanks to Votan's 4122, a voice mailbox that can be built around an IBM PC XT. The system's price is not its only appeal: It also is the first to respond to a user's spoken commands.

The 4122 employs two Votan voice cards and handles 90 users, each making five calls a day. The 4144 is based on Sperry's IBM look-alike. It works with four cards, handling up to 250 users. Each card carries both a 6809 microcomputer and a TMS300 digital signal processor to unburden the host CPU.

The voice board is loaded with a custom chip that compresses 64-kbit/s voice streams down to 16 kbits a second. (Other manufacturers compress data streams to 32 kbits a second.) Votan's 16-kbit/s level allows the company to implement a system in a "low-performance" personal computer. It also lessens the need for disk storage systems.

The systems are available within 30 days. The 4122 is fitted with a 30 Mbyte disk that retains 7.5 hours of stored messages. It costs $11,950. The Sperry-based 4144, with its 60-Mbyte disk, stores up to 15 hours of messages and costs $19,950. An interactive phone demonstration is available by calling (415) 490-7979.

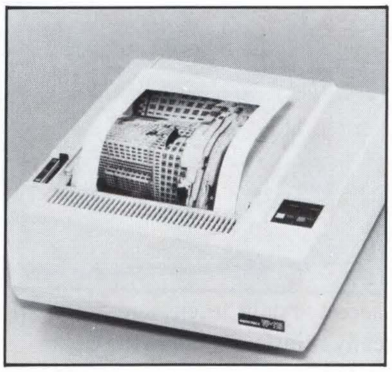
Votan Inc., 4487 Technology Dr., Fremont, CA 94538; Marilyn Wilson, (415) 490-7600.

CIRCLE 322

BOOTH C4218

Thermal printer aids CAD/CAE

One of the first thermal printers with a 64-tone gray scale fills an $8^1/_2$-by-11 in. page in about 40 seconds. The speed of Seikosha's VP-115 suits it to CAE/CAD workstation activities, computer imaging, and other graphics applications that call for rapid screen dumps.



The VP-115 inputs are raster video signals with up to 620 lines and 7-MHz scan rates. A 6-bit analog-to-digital converter changes the light intensity in the composite video into a comparable density level for thermally transferred dots.

The printer's built-in screen-dump utilities print high contrast text with a resolution of 300 dots/in. and creates images with a resolution of 75 dots/in. The highest dot density is used to represent the darkest regions of a screen, while the sparse dot regions represent light areas of the screen. Because it extracts the luminance (light level) of a video signal, it can convert composite color into a grey scale image.

The VP-115 is also intended to support x-ray, CAT-scan and other medical imaging applications. Because of its low noise level, below 45 dB ambient, the printer can fit well in quiet hospital or laboratory environments.

Priced at $4700, the VP-115 is available now from stock.

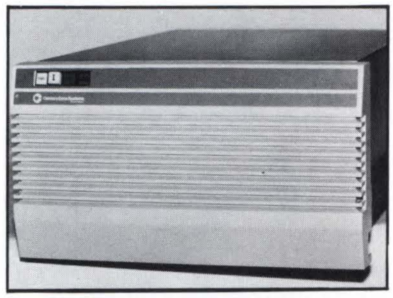
Seikosha Co. Ltd., 10080 N. Wolf Rd., SW 3/249, Cupertino, CA 95014; Phil Strong (408) 446-5820.

CIRCLE 321

BOOTH 3325

Speed, brains mark IPI-3 interface

One of the first full implementations of the IPI-3 interface is here. IPI-3 furnishes both intelligent I/O channels and high-speed data transfers for the new generation of mainframes and minicomputers. Century Data's IPI-Plus is an option for the company's AMS 600 HP, a full storage cabinet that contains an IPI-3 controller and 615 Mbytes of 14-in. disk storage.



In addition to the IPI-3 generic command set, IPI-Plus supplies a defect management system, which presents a virtually defect-free media, a look-ahead buffer, and cache memory. The look-ahead algorithm recognizes the most frequently accessed data tracks and automatically transfers these to the cache.

Data access also is improved by a data relocation algorithm that minimizes seek time by automatically positioning the read heads over the most frequently used data cylinders. The foregoing features improves throughput by 50%.

Working with the AMS 6000 HP storage subsystem, the IPI-Plus interface connects to a mainframe or minicomputer via a user-designed host adapter. Data transfers between the host and the storage subsystem take place at up to 3 Mbytes/s. Future versions of IPI-Plus will aim for 10 Mbytes/s.

The AMS 600HP with IPI-Plus costs $14,500 in 200-piece quantities. Delivery is within 30 days.

Century Data Systems, 1270 N. Kraemer Blvd., Anaheim, CA 92806; Renee Brown; (714) 999-2660.

CIRCLE 319
BOOTH B3712

CIRCLE 59

Speed and Spirit

100-350 MHz buffers from Élantec.

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Speed and spirit. The unity gain EL2003, 2004, and 2005. Blazing buffers. Tested and guaranteed minimum slew rates of 600, 2000, 1000 V/µs respectively. Available now from Elantec—your spirited supplier of high performance analog ICs.

Driving speed up and cost down. The EL2003 100 MHz video line driver boosts the output of high speed op amps and video DACs. Our proprietary dielectric isolation process makes it the lowest cost high-speed monolithic device for driving 50Ω or 75Ω video lines. And built-in short circuit protection makes it the safest.

Blazing speed. The EL2004 350 MHz FET input buffer/line driver. The fastest device to buffer inputs for applications that require high current drive (up to 250 mA) and high frequency response. Its 1.7 ns rise time also makes it an ideal pin driver for ATE.

Ultra-high input impedance. The EL2005 140 MHz FET input buffer's cascode configuration maintains constant input characteristics over the full ±10V input range. Its 1000 GΩ input impedance is ideal for test instrumentation and high speed sample and hold applications.

The spirit of '86. Elantec is revolutionizing the standards for high-rel and high quality. Our blazing buffers are available for the full military temperature range, −55° C to +125°C, with screening and quality conformance testing per MIL-STD-883 Revision C. And our facilities are among the very few that are MIL-STD-1772 certified.

To keep you in the best of spirits we offer the industry's only two-for-one guarantee. Contact Elantec, Inc., 1996 Tarob Court, Milpitas, CA 95035, (800) 821-7429. In California call (408) 945-1323.

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CIRCLE 60

OCCASIONALLY, EVERYONE WISHES HE HAD ANOTHER SHOT AT HIS DESIGN.

There are some things man was not meant to tamper with.

Semicustom circuits, for example. If you happen to have second thoughts about your design, you're powerless to do anything about them. Unless you have the luxury of lots and lots of time and money. But when you're trying to get your products to market before the competition, extra time is something you rarely have, and extra money is something you *never* have.

Fortunately, there is help: Programmable Logic Devices from Signetics. With Signetics PLDs, you can make all the changes and tweaks you like—without losing precious time. So you reduce the risk of completing your design after it's too late to compete effectively in the marketplace.

What makes Signetics PLDs the most flexible, most complete, best-supported PLD series in the industry? A unique approach to sequencer architecture, for one thing.

It not only simplifies state machine designs but also cuts the time it takes to build them.

It's frightfully easy to use Signetics Programmable Logic. We provide software—free of charge to qualified users—that turns an IBM* PC into a PLD work station. The work station helps you to define your function in terms of a Boolean equation or state transfer expression; then you use the output to program the fuses, and your circuit is ready to go.

Complete documentation and design simulation let you perfect your ideas to the nth degree. And if you have any questions, a phone call to one of our field applications engineers will get you the answers fast.

There's more you should know about Signetics PLDs. For details and specs, just send in the coupon.

Signetics Programmable Logic Devices.

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Look at all the FACTs that go into computers.

When it comes to computer designs, there's one fact you shouldn't overlook: Fairchild Advanced CMOS Technology.

The highest performance CMOS logic family available, FACT is a comprehensive, rapidly growing product line. With a number of features ideal for computer applications from PCs to minicomputers.

Features such as higher speed. FACT's high-speed propagation delays are better than 5ns for gate functions and typically don't change more than 2ns over the entire operating voltage range.

Power consumption is just as impressive – typically 10 μW per gate quiescent, the lowest in the field. In fact, FACT uses 2-3 orders of magnitude *less* power than any competing technology. So your system reliability and packing densities are enhanced, power supplies can be made smaller, and heat dissipation hardware can be significantly reduced. In some cases, it's done away with altogether.

And line driving characteristics? FACT offers I_{OH}/I_{OL} dynamic output current drive specifications of $-75/86$ mA. Which guarantees 50 Ω transmission line driving and more efficient bus driving. FACT's very low output impedance lets you drive highly capacative nodes and bus architectures common to all mini and microcomputer applications. While eliminating the need for any external or additional buffering.

There's still more:

FACT provides the highest noise immunity available. Its input protection diodes help suppress transient noise in your application. And FACT is available in SOICs, and plastic or ceramic DIPs.

FACT™

For more information and a free FACT data book, call your local sales office or distributor. Or contact The Fairchild Customer Information Center at 1-800-554-4443.

Because it's time your computer designs took advantage of all the FACTs.

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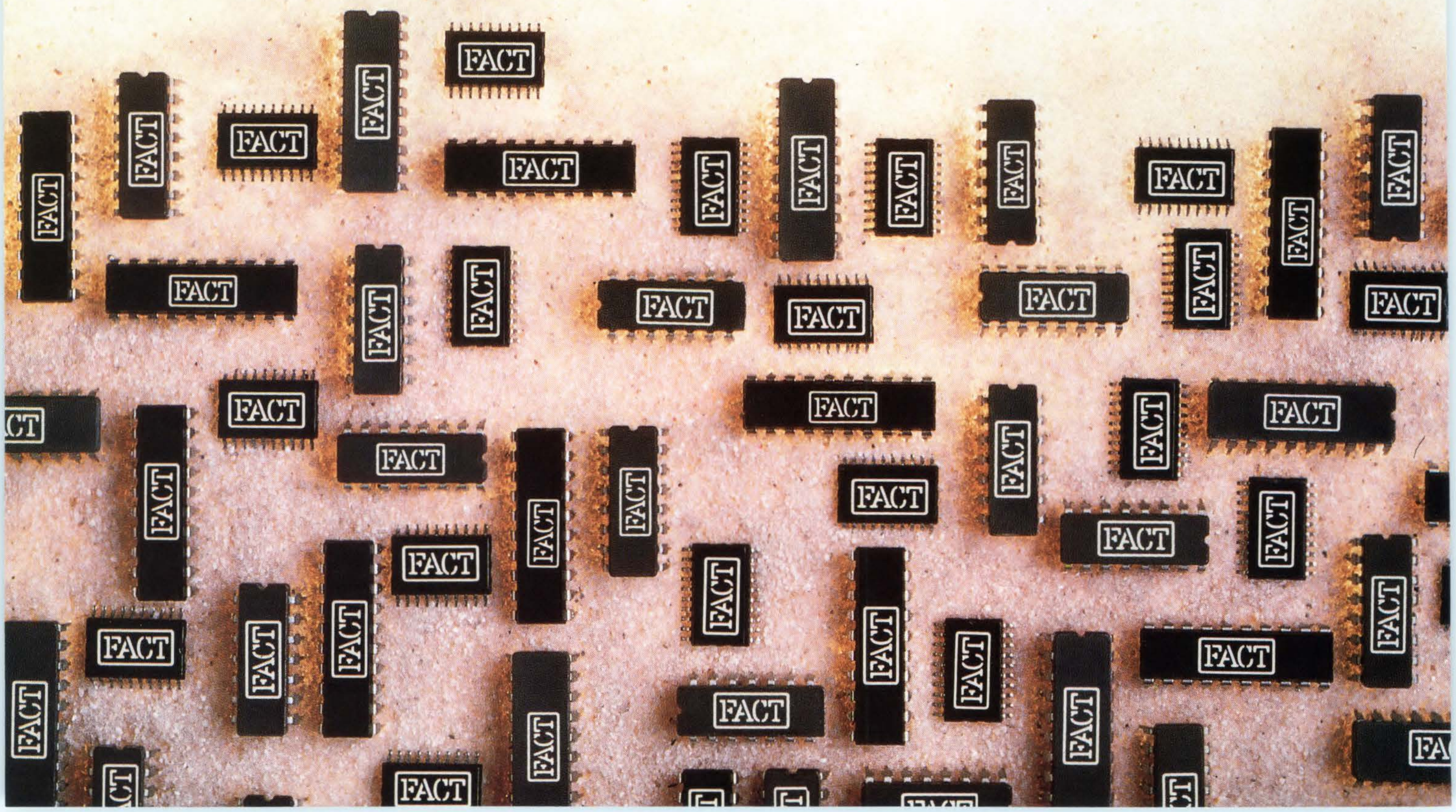
CIRCLE 62



READER FEEDBACK

Where to find names of C software suppliers

I was very interested in your March 20 Newsfront article, "Machine-driven C Steps Up Pace of Unix Parade" [p. 34]. I manage a software team that does monitor and control systems for Granger equipment using IBM PC ATs. I have been very closely following developments and new products in Computer-Aided Software Engineering and advanced methods and tools for software design.

In the article you mention that there are eight vendors offering more than a dozen software generators for C. I would appreciate it if you would send me a list of these vendors and software packages.

I will definitely continue to follow future reports in ELECTRONIC DESIGN and other publications on this topic.

Michael Winkler
GMAP Systems
Santa Clara, Calif.

The author replies: *The story mentioned several suppliers; others are listed on p. 72 of the February 20 issue. The latter group deals primarily with tools that speed up code generation, rather than with so-called applications generators.*

Excess of managers causing decline of U.S.

Carole Patton's April 3 Professional Notebook [p. 223] was superb. She has put her finger on the reason for the decline of the United States and the rise of Japan. If the engineers are out of engineering and the nitpickers and pebble-counters run things via ever-increasing layers of bureaucratic paperwork, what can be expected other than a return to the Stone Age (Early Neolithic)? The Harvard Business School maxim, "A good manager need know nothing about what he manages, only how to manage," will go on many tombstones, including those of the Challenger astronauts. When everyone is a manager, I ask, who will work? As we say, "A manager is like an artichoke; peel all the layers off and nothing remains," or "The reason managers always swim in circles is so they keep moving and stay in the same place."

Irv Barditch
Baltimore, MD

VLSI software models? Don't hold your breath

I would like to respond to the opinions expressed by Nicholas Van Brunt in your April 3 article, "Simulating Advanced ICs: Software vs Chips" [p. 48]. As I see it, the crux of Mr. Van Brunt's thesis is that physical modeling is far from perfect, is not available until the physical IC is actually available, and by its very being, diffuses the pressures that could "force chip makers to supply a software model for each chip." Modeling therefore "gets in the way of a real solution."

I contend that the user community cannot "force" IC manufacturers to supply detailed software models for use in design simulation today any more than it could nearly a decade ago, when the automatic test community first made the attempt. The problem then, as now, was that it was virtually impossible for the IC manufacturer to supply a detailed model of an IC without giving its competition the perfect tools to engineer and certify a copy. Even if IC vendors could be persuaded to part with a model, how "correct and

(continued on p. 300)

Why Ando's "New Generation" VLSI Testers Are Better

- 100MHz Speed
- 1024-Pin Testing
- Dual CPU Architecture

In the face of today's advances—like higher pin counts, faster speeds, application-specific ICs and the like—you can't afford to be left behind. That's why Ando has created our new DIC-9000 series of VLSI test systems.

They're Fast, They're Capable

With test speeds up to 100MHz and simultaneous testing of up to 1,024 I/O pins, these testers are ready for the most sophisticated R&D lab. They're also ideal for the inspection or production line, too.

They Link Up

The dual 32-bit CPU architecture means DIC-9000-series testers can be easily linked to CAD or factory automation systems, guaranteeing the utmost in overall throughput.

They Get Down to Business

Leading off is the DIC-9035 VLSI Test System, featuring testing of a full 512 I/O pins with ±500ps accuracy. Three different types of stations are available for testing high-pin-count gate arrays and scan-design ICs; high-speed MPUs up to 32 bits; ECL and GaAs; the list goes on and on. Dual CPUs, DC/pin architecture and parallel testing mean better performance and throughput, too.

Want to hear more about this remarkable new generation? Contact your nearest Ando sales office. Or better yet, come see us at Semicon West.

The DIC-9035 VLSI Test System

Test Rate 100MHz (link mode)
50MHz (normal mode)
Pin Count 512 I/O pins, 256 I/O pins, or 128 I/O pins
Test Stations General-purpose station (Driver: 12Vp-p)
Bipolar station (Driver: 2.5Vp-p, Comparator: −3 to +5V)
Low capacitance station (Driver: 7Vp-p, Input capacitance: 30pF)
Total Timing Accuracy ±500ps
Timing Generator 46 edges max.
Pattern Memory 512k words max.
Algorithmic Pattern Generator* 14X, 14Y, 18 data
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DC Measurement Universal type; 16 units/station; PMU/pin
Parallel Testing Available

*ALPG and SPG output can be connected to any tester pin via pin selector.

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CIRCLE 64

UPCOMING MEETINGS

1st Annual High Frequency Power Conversion Conference & Exhibition, May 28–30. The Cavalier Resort, Virginia Beach, VA. Sam Davis, Conference Director, c/o Intertec Communications, 2472 Eastman Ave., Bldg. 34, Ventura, CA 93003; (805) 658-0933.

40th Annual Frequency Control Symposium, May 28–30. Marriott Hotel, Philadelphia, PA. Dr. J. Vig, U.S. Army Electronics Technology & Devices Lab, ATTN: SLCET-EQ, Fort Monmouth, NJ 07703; (201) 544-1510.

1986 VLSI Technology Symposium, May 28–30. Hotel Intercontinental, San Diego, CA. Moiz M. Beguwala, Program Chairman, Rockwell International, MS 501-369, Semiconductor Products Division, 4311 Jamboree Rd., P.O. Box C, Newport Beach, CA 92660; (714) 833-4712.

1986 International Summer Consumer Electronics Show, June 1–4. McCormick Place, Chicago, IL. Allan Schlosser, Staff Vice President, Consumer Electronics Group, 2001 Eye St. N.W., Washington, D.C. 20006; (202) 457-4919.

Vision '86 Applied Machine Vision Conference & Exposition, June 2–5. Cobo Hall, Detroit, MI. Machine Vision Assoc. of the Society of Manufacturing Engineers, 1 SME Dr., P.O. Box 930, Dearborn, MI 48121; (313) 271-1500.

Advanced Infrared Detectors and Systems Conference, June 3–5. London, England. Conference Services, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England; (+44) 1 240 1871.

Circuit Expo '86 West, June 3–5. Long Beach Convention Center, Long Beach, CA. Mary Burns Sheridan, Worldwide Convention Management Co., P.O. Box 159, Libertyville, IL 60048; (312) 362-8711.

Power Europa '86, Power Supply and Conversion Conference & Exhibition, June 3–5. Rhein-Maine-Halle, Wiesbaden, West Germany. TCM Expositions Ltd., Exchange House, 33 Station Rd., Liphook, Hampshire GU30 7DN, England; (0428) 724 660.

6th International Conference on Robot Vision & Sensory Controls (RoViSeC-6), June 3–5. Paris, France. IFS Conferences Ltd., 35-39 High St., Kempston, Bedford MK42 7BT England; (+44) 234 853605.

3rd International Conference on Lasers in Manufacturing (LIM-3), June 3–5. Paris, France. IFS Conferences Ltd., 35-39 High St., Kempston, Bedford MK42 7BT, England; (+44) 234 853605.

5th European Semiconductor Industry Dataquest Conference, June 4–6. Venice, Italy. Cochrane Communications Ltd., CCL House, 59 Fleet St., London EC4Y 1JU, England; (+44) 1 353 8807.

3rd International VLSI Multilevel Interconnection (V-MIC) Conference, June 9–11. Santa Clara Marriott Hotel, Santa Clara, CA. Dr. Thomas E. Wade, General Chairman, IEEE VLSI Mutlilevel Interconnection Conference, College of Engineering, University of South Florida, Tampa, FL 33620; (813) 974-3786.

Conference on Lasers and Electro-Optics (CLEO '86), June 9–13. Moscone Convention Center, San Francisco, CA. CLEO '86, Optical Society of America, 1816 Jefferson Pl. N.W., Washington, D.C. 20036; (202) 223-0920.

14th International Conference on Quantum Electronics (IQEC '86), June 9–13. Moscone Convention Center, San Francisco, CA. IQEC '86, Optical Society of America, 1816 Jefferson Pl. N.W., Washington, D.C. 20036; (202) 223-0920.

4th European Comdex International Conference & Exposition, June 10–12. The Acropolis, Nice, France. Comdex International, The Interface Group, 300 First Ave., Needham, MA 02194; (617) 449-6600.

International Conference on Power Electronics and Variable Speed Drives, June 10–12. London, England. Conference Services, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England; (+44) 1 240 1871.

(continued on p. 124)

UPCOMING MEETINGS

(continued from p. 123)

NEPCON East '86 Electronics Packaging, Production and Testing Conference & Exposition, June 10–12. Bayside Exposition Center, Boston, MA. NEPCON East '86, Cahners Exposition Group, 1350 E. Touhy Ave., P.O. Box 5060, Des Plaines, IL 60017; (312) 299-9311.

1986 National Computer Conference & Exhibition (NCC '86), June 16-19. Las Vegas Convention Center, Las Vegas, NV. NCC '86, American Federation of Information Processing Societies (AFIPS), 1899 Preston White Dr., Reston, VA 22091; (800) NCC-1986.

ISC EXPO '86 Central, International Security Conference & Exposition, June 19–21. O'Hare Exposition Center, Rosemont, IL. ISC EXPO'86 Central, Cahners Exposition Group, Cahners Plaza, 1350 East Touhy Ave., P.O. Box 5060, Des Plaines, IL 60017; (312) 299-9311.

1986 IEEE Computer Vision and Pattern Recognition Conference & Exhibition, June 22–26. Fontainbleau Hilton Hotel, Miami Beach, FL. Dr. Linda Shapiro, Conference Chairman, Machine Vision International, 325 E. Eisenhower Pkwy., Ann Arbor, MI 48104; or IEEE Computer Society, 1730 Massachusetts Ave. N.W., Washington, D.C. 20036; (202) 371-0101.

7th Power Modulator Symposium, June 23–25. Hyatt Seattle, Seattle, WA. Leslie Gallo, Program Secretary, Palisades Institute for Research Services Inc., 2011 Crystal Dr., 1 Crystal Pk., Ste. 307, Arlington, VA 22202; (703) 769-5580.

Automatic Test Equipment (ATE) East '86 Conference & Exhibition, June 23–26. World Trade Center, Boston, MA. Morgan-Grampian Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-3976.

CPEM '86, Conference on Precision Electro-Magnetic Measurements, June 23–27. National Bureau of Standards, Gaithersburg, MD. CPEM '86 Technical Program Chairman, Norman B. Belecki, National Bureau of Standards, B146, Metrology, Gaithersburg, MD 20899; (301) 921-2715.

4th European Fiber Optics Communications & Local Area Networks Exhibition (EFOC/LAN '86), June 23–27. International Congrescentrum Rai, Amsterdam, The Netherlands. Joan Barry, Information Gatekeepers Inc., 214 Harvard Ave., Boston, MA 02125; (617) 232-3111.

Power Electronics Specialists Conference (PESC '86), June 23–27. University of British Columbia campus, Vancouver, B.C., Canada. Peter Wood, Westinghouse R&D Center, 1310 Beulah Rd., Pittsburgh, PA 15235; (412) 256-2306.

23rd Design Automation Conference & Exhibition (DAC '86), June 29–July 2. Las Vegas Hilton, Las Vegas, NV. DAC '86. Donald E. Thomas, Program Chairman, IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598.

International Workshop on Systolic Arrays, July 2–4. University of Oxford, Oxford, England. Dr. Will Moore, Secretary, Systolic Array Workshop, Dept. of Engineering Science, University of Oxford, Parks Rd., OXFORD, OXI 3PJ, England; 0865 59988.

4th Annual Personal Computer (PC '86) Exposition & Conference, July 9–11. Jacob K. Javits Convention Center, New York, NY. PC Expo, 333 Sylvan Ave., Englewood Cliffs, NJ 07632; (201) 569-8542.

British Information Technology (Britec '86) Conference & Exhibition on Engineering Software, July 14–16. Hilton Hotel at Colonial, Wakefield, MA. Dr. C. A. Brebbia, Computational Mechanics Inc., Ste. 6200, 400 W. Cummings Pk., Woburn, MA 01801; (617) 933-7374.

15th Annual International Parallel Processing Conference, Aug. 19–22. Pheasant Run Resort, St. Charles, IL. 1986 International Conference on Parallel Processing C/O IEEE Computer Society, 1730 Massachusetts Ave. N.W., Washington, D.C. 20036.

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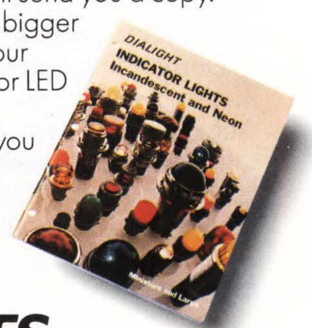

CIRCLE 69

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ELECTRONIC DESIGN REPORTS

Timing, not speed, counts the most when testing fast VLSI ICs

As VLSI devices continue to get faster and more complex, testing them at speed in a production environment has become a formidable task. Hard-pressed to keep up with today's testing needs, where 10-MHz speeds are not without their difficulties, designers of VLSI testers shudder at the testing challenges posed by gallium arsenide devices now on the drawing boards. VLSI testers are not even close to addressing that problem. Right now, the latest testers are gearing up to tackle phase I VHSIC chips, which are designed with 1.25-µm technology and operate at 80-MHz data rates. And phase II chips are already looming on the horizon. Built around 0.5-µm technology, these devices will run at 100 MHz.

However, speed is not the most important consideration. In reality, a tester's timing accuracy and resolution are the truly significant parameters to be concerned with. Today, bragging rights for these specifications are down below a nanosecond. The reason? As devices get more complex, even those operating at lower data rates have so many tasks going on inside that proper operation demands ever more stringent timing tolerances. That is, as chip complexity goes up, the maximum tolerable error in the placement of pulse edges, with respect to each other, goes down. Moreover, as tester timing accuracy gets better, smaller testing guardbands can be used, thereby increasing the window for good devices.

Demanding subnanosecond accuracies in a high–pin-count VLSI tester is one thing. Achieving it, however, is another. It is an engineering undertaking of the highest order, requiring sophisticated automatic calibration techniques. Without these techniques, generating and distributing high-speed waveform edges to, say, 256 tester pins and having them all arrive at precisely the same instant is truly a task that is beyond the capabilities of mere mortals.

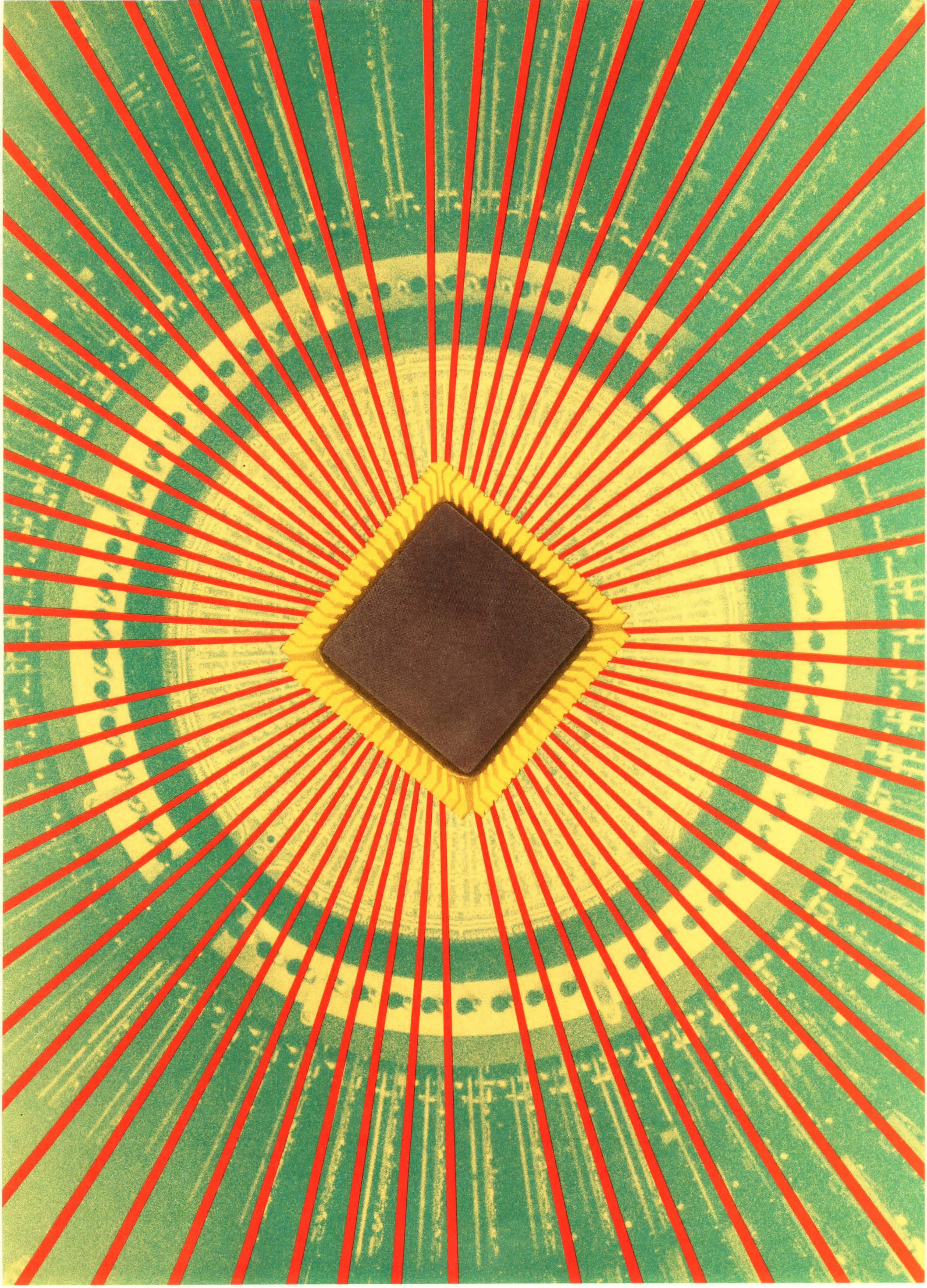
Bob Milne

Moreover, with tester speed, accuracy, and pin count under the gun, traditional shared-resource testers are facing stiff competition from systems based on the tester-per-pin architecture that may well become the de facto standard for future leading-edge VLSI testers. Testers optimized for specialized logic families like advanced Schottky TTL and HCMOS are also springing up. Beyond that, VLSI testers are being readied to cope with the demands imposed by high-speed CMOS devices. Here, reducing test-head capacitance to 20 pF and below becomes as important a factor as speed, accuracy, and pin count.

Rounding out the demands on VLSI testers is the need to test for a device's maximum operating frequency in production environments. With frequencies reaching 100 MHz and beyond, VLSI testers need a boost from external instrumentation.

Recent tester introductions clearly show the influence of the VHSIC program. This month, for instance, GenRad Inc.'s Semiconductor Test Division (Milpitas, Calif.) announced its GR180, a 288-pin tester with an 80-MHz multiplexed data rate, a 125-ps timing resolution, and an overall maximum system timing error of ±750 ps. Moreover, a special clock within the tester operates as fast as 120 MHz. The company also introduced a 144-pin tester with a 60-MHz multiplexed data rate. Its other timing specifications are the same as the GR180's.

In February, Sentry-Production Test Systems (San Jose, Calif.) took the wraps off its S15, a production-oriented, low-cost VLSI



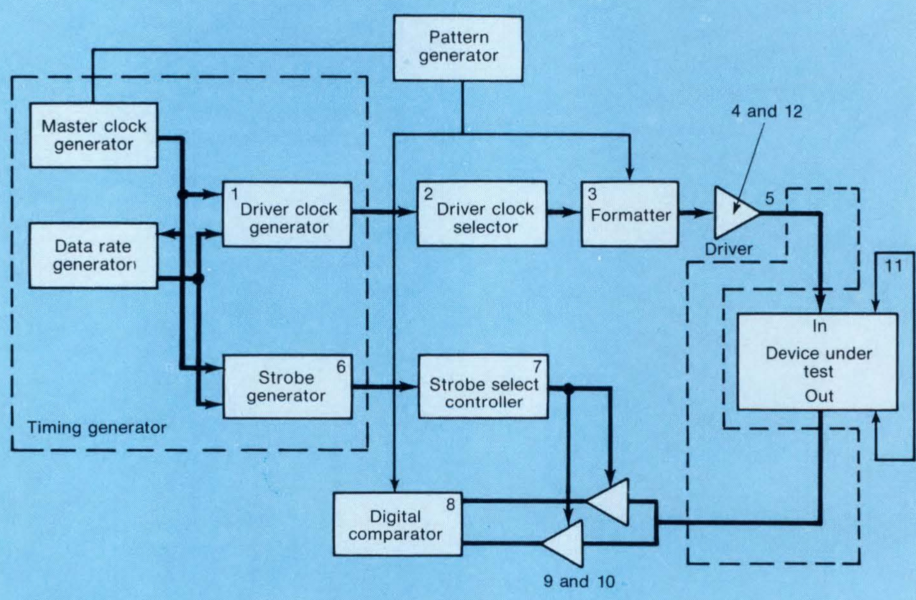
tester. Equipped with 64, 128, or 256 I/O pins, the system has a 20-MHz basic test frequency that can be boosted to 40 MHz by multiplexing pins. The timing system boasts a 60-ps resolution, 500-ps maximum driver-to-driver and comparator-to-comparator skewing, and a 700-ps maximum edge placement error. Overall timing accuracy is within ± 1.5 ns.

Although ATE manufacturers often point to an outstanding specification like driver skewing between pins, users are most concerned with the overall system timing error, which is determined simply by adding up all of its components. The trouble is that many of those error components are functions of how a particular test program allocates the tester resources.

Taking a close look at the obstacles to accuracy facing VLSI testers helps one appreciate the engineering effort required to reach today's performance levels. Anyone perusing VLSI tester data sheets should keep in mind, however, that not all ATE manufacturers define overall timing accuracy the same way.

Probably the most definitive analysis of the sources of error in a VLSI test system was conducted in 1981 by the Advantest Corp. (Saitama, Japan), formerly Takeda Rikew, and Musashino Communication Laboratories, NT&T (Tokyo, Japan). In looking at the functional blocks that make up a typical test system—pattern generator, timing generator, driver clock selector, formatter, driver, strobe select controller, and digital comparator—researchers found no fewer than 12 sources of timing errors (Fig. 1). Actual analysis revealed that timing errors in test results could reach ± 7 ns or more.

If keeping track of the effects of a dozen error sources seems complex, the real difficulty comes in maintaining acceptable timing accuracy across all the tester pins. The



Sources of error

1. Clock-positioning nonlinearity (associated with changing delay widths of driver clocks)
2. Skewing between driver clocks
3. Format-to-format skewing (associated with changing waveform formats in the driver)
4. Pin-to-pin driver skewing
5. Jitter
6. Strobe positioning nonlinearity (associated with changing delay widths of strobe timing)
7. Strobe-to strobe skewing (associated with changing choices of strobe)
8. Pin-to-pin comparator skewing (strobe timing skew between dissimilar comparator pins)
9. High or low comparator skewing (strobe timing skew between two comparators, one for high-level comparison and one for low-level comparison)
10. Ambiguous time (uncertainty of strobe timing when the device under test's output is sensed with the comparators)
11. Driver-to-comparator skewing (skewing between driver output timing and comparator strobe timing)
12. Dual thresholds (error associated with the transition time of a driver output between high and low levels)

Source: 1981 International Test Conference

1. To functionally test ICs, ATE systems typically rely on seven major functional blocks: the pattern generator, timing generator, driver clock selector, formatter, driver, strobe select controller, and the digital comparator. The bold lines indicate the paths along which timing errors may be measured.

situation is somewhat like a school coming up with one or two world-class sprinters—not easy, but within the realm of possibility. But could the school find 128 of them or maybe even 256? That is the problem faced by designers of VLSI testers.

For example, there is simply no way to make the transmission paths to 128 tester pins so nearly identical that subnanosecond timing accuracies are inherent in the system. A 1-in. difference in cable length, for instance, causes a 100-ps timing difference. Consequently, testers must compensate for the variations. In other words, they must be calibrated.

WHY CALIBRATION?

The goal of calibration is to ensure that all timed voltage transitions delivered to the pins of a device under test (DUT), and all times at which output data from the device is compared with expected data, are accurate in relation to a defined reference. The degree of this accuracy can determine the overall system accuracy.

An IC undergoing test is connected to a tester's timing source through test system channels. Signals traveling a channel path must pass through multiplexers, formatters, cables, and drivers or detectors to the pins of the DUT. Naturally, the inevitable delays through circuits and the differences in cable lengths cause timing variations from channel to channel. Thus, voltage transitions at the input pins and data detection at the output pins occur at different times even though they are supposed to be coincident. These timing variations are called skew.

Basically, calibration determines skewing in each system channel and compensates for it by means of a variable delay in each system input and output channel. Hardware, software, or a combination of the two can be used to control the compensating delay.

Two common hardware techniques are used—torque adjustment and premeasured cables. To adjust torque, channel delays are measured with an oscilloscope; a technician with a screwdriver can adjust hardware delays. When premeasured cables are used, an oscilloscope again measures delays, and a cable of appropriate length is placed in each channel path to make all of the delays equal.

However, these manual methods are time-consuming. Consequently, the trend is toward automatic calibration. Instead of using an oscilloscope, internal detectors make the measurements, and software interprets the results and applies the necessary corrections.

One way to implement automatic calibration is to employ a switch matrix, which can be built into a device interface board, to connect each of the system input driver channels to a reference detector. Each of the driver delays is adjusted to this reference detector. Then, each channel detector is excited by its associated driver and calibrated with respect to the system strobe. Because this method relies on the electrical distances being equal from the reference detector through the matrix to each channel driver, any differences in path lengths add errors to the calibration.

An automatic calibration method based on time-domain reflectometry (TDR) seems almost tailor-made for VLSI test systems. TDR is based on transmission line theory: A wave traveling through a transmission line terminated by anything other than the line's characteristic impedance, is reflected back through the line. If the line terminates with an open circuit, the reflected wave's amplitude equals that of the forward wave.

What makes TDR so attractive is that in a VLSI test system, the point of contact with the DUT pins is an open circuit when a device is not being tested. The TDR technique, therefore, can make measurements right up to the point at which the device pins are connected to the test system. No special calibration fixtures are required, and the procedure can be used whether the DUT interface is a test socket, an automatic handler, or a wafer prober.

The J941 VLSI test system from Teradyne Inc.'s Semiconductor Test Division (Woodland Hills, Calif.) uses TDR in a scheme called automatic edge lock (AEL). The company also implements the technique in its J967 and J983 VLSI test systems, achieving a ±800-ps edge placement error.

Housed in the test system mainframe, the time-domain reflectometer contains a master driver and master detector (Fig. 2). With a 50-Ω matrix, the TDR circuitry can be connected to any test system channel. During calibration, the channel driver is bypassed to allow reflected pulses to travel back to the master detector.

PUTTING TDR TO WORK

Channel deskewing begins with the TDR circuitry connected to channel 1, which subsequently serves as a reference channel. The period generator simultaneously sends a pulse through the delay circuitry for the master driver and master detector. The master detector delay is varied until the pulse through the delay circuitry arrives at the master detector coincident with the reflected pulse from the open device contact point. This procedure adjusts the master detector strobe to the round-trip time of the edge on the reference channel.

After it is adjusted, the master detector finds the time delay for each channel. This task is accomplished by connecting one channel at a time and varying the master driver delay until the reflected edge arrives at the master detector at the same time it did for the reference channel. Using the acquired delay values, the master driver sends edges at different times so that all channel inputs arrive at the device contact point at the same time.

During testing, either window or edge strobes may be used to compare DUT outputs with expected data. With the edge strobe, outputs are compared at specific discrete times. The actual placements of the strobe times are adjusted during detector calibration. The master driver, connected to the channel being calibrated, sends edges to the open point of contact. At the reference time (T = 0), these edges are reflected back to the channel detector. Using coarse and fine linear searches, the appropriate detector delay digital-to-analog converter is adjusted until the channel detector registers the edge transition at T = 0.

Once the channel detectors are calibrated, they are used to adjust three deskewing d-a converters that control the period and driver edge placement on each channel. The channel detectors are now strobed at the reference time, and the appropriate driver deskewing d-a converter is varied until the reference time condition is achieved.

BREAKING TRADITION

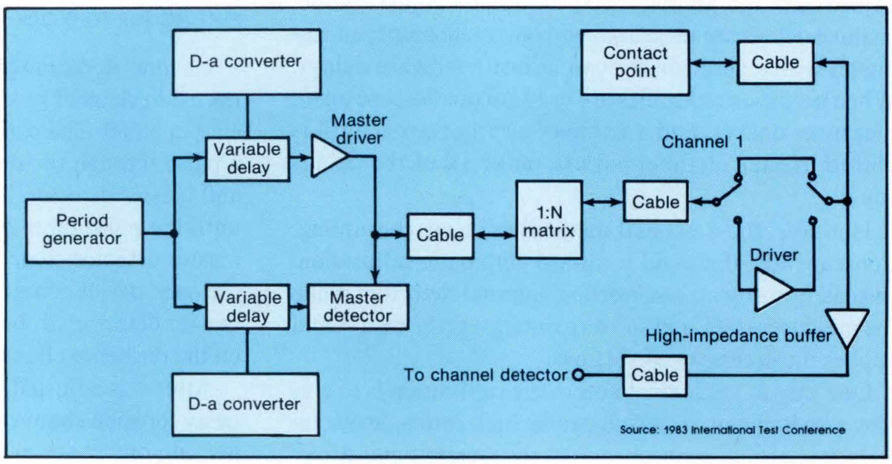
The quest for improved timing accuracy in high-pin-count VLSI testers has radically altered the basic architecture of the test system itself. Traditionally, testers have revolved around a shared-resource architecture in which a small number of central timing resources are distributed through a large switch matrix to groups of device pins (Fig. 3a). An upshot of this arrangement is the extremely complex timing path between the master clock and the DUT pins. Moreover, because the resources are shared, a separate series of timing measurements is needed to determine the accuracy of each of the combinations of resources and paths.

One way to simplify the timing chain is to place a timing generator behind each tester pin (Fig. 3b). Known as a tester per pin architecture, it was pioneered by Megatest Corp. (Santa Clara, Calif.) with its 1983 introduction of the MegaOne VLSI test system. Depending on how you look at it, the approach can be considered one of either elegance or brute force. However, one thing seems certain: The architecture seems likely to play a key role in future VLSI test systems. In fact, very few ATE manufacturers are saying anything bad about the approach—even though their current systems may be based on the shared-resource approach. The technique's biggest drawback, though, is its megabuck cost.

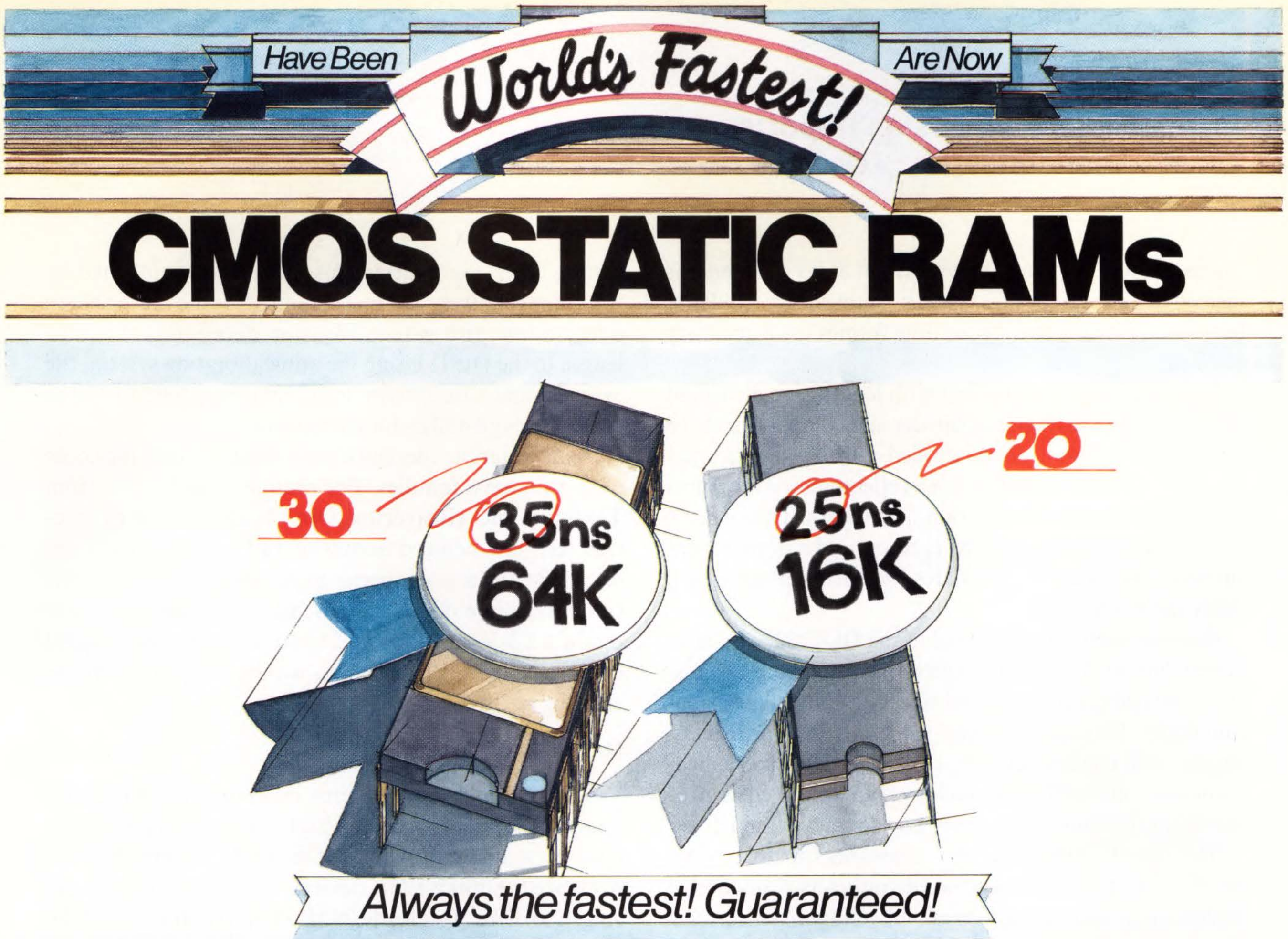
Because the tester-per-pin architecture produces a much simpler timing chain, the number of gates in the timing path is kept low. Consequently, skewing and jitter are reduced. The architecture's basic architecture, however, stems from the fact that any given timing edge follows a fixed, independent path to the DUT. Thus, the timing for each path can be precisely compensated using autocalibration data.

Since the timing path is fixed, all deskewing can be accomplished with software, employing the same delay mechanism that creates the timing in the first place (Fig. 4). The timing generator accesses the values for this delay from a register table loaded with precalibrated values. Those represent not only the times, but also the waveforms to be produced.

Data for the waveform register is obtained from a five-step automatic calibration process (Fig. 5). The system measures the autocalibration time-delay generator and constructs a compensation table. A period average measurement determines the delays, with the NBS-traceable crystal source in the master clock acting as the time base. Then, the calibration reference driver and comparator are



2. Teradyne's automatic edge-lock technique uses time-domain reflectometry to measure channel delays to the open-circuited point of contact to the device under test. During calibration, waveform edges from the master driver are sent to the point of contact where they are reflected back to the master detector. A 50-Ω matrix connects the master driver to each of the test system channels one at a time. The channel drivers are bypassed while the delays are measured.



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connected together and their resultant delay difference is measured and stored. This process establishes coincidence between the driver and strobe time frames to an accuracy of 25 ps.

In the second step, physical path lengths are measured by connecting the reference divider and comparator to the pin electronics by way of controlled-impedance relay matrix. At this point, time domain reflectometry measures the autocalibration distribution wire length. Then a relay on the pin electronics channel is closed and a similar measurement is taken that includes the wiring propagation delay to the DUT site.

Because each edge delivered to the DUT follows an independent path, the third autocalibration step exhaustively measures each path and stores its inherent propagation delay. Here, every delay value possible for drivers, strobes, and enable signals is catalogued. For these measurements, autocalibration achieves an overall edge measurement resolution of 3 ps and an accuracy within 20 ps.

The fourth calibration step measures the delay variations of the pin drivers and comparators as a function of driver rail or comparator threshold voltages. To perform these measurements, the autocalibration system must be able to resolve its own deviations from ideal performance using the autocalibration driver as a "golden" reference. The circuit design is such that its propagation delay varies less than 10 ps over its entire voltage range of −3 to +9 V. To produce separate calibration values for the exact voltages used during a test, the autocalibration comparator is calibrated against the reference driver, as are all the pin channels.

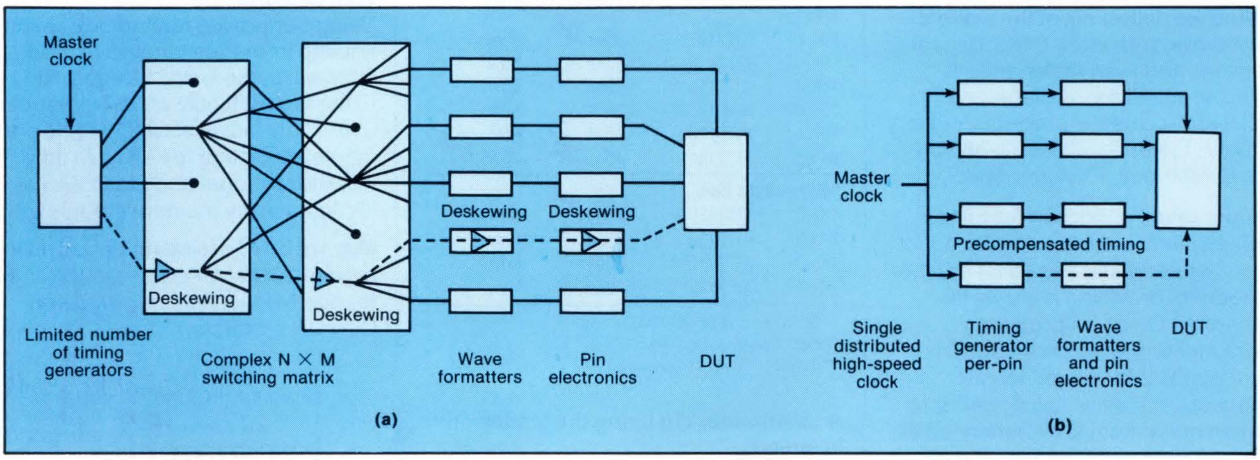
The final step involves building the precompensated timing table. Generating this table is accomplished by summing relatively few measurements—the timing chain delay minus the autocalibration delay plus the path length to the DUT. Using the autocalibration system, the overall worst-case system inaccuracies are held to 400 ps for drivers and 450 ps for comparators.

Some testers are designed specifically to meet the needs of certain logic families. For example, the S-3225 from Tektronix Inc. (Beaverton, Ore.) is tailored for production testing advanced Schottky TTL and HCMOS devices. The tester uses special high-speed drivers that feature a slew rate of at least 1 V/ns. Thus, the drivers can produce a 3-V transition in 2.4 ns or less. Moreover, signal edge placement is accurate to within 125 ps with driver skewing of 1 ns or less.

MATCHLESS MEASUREMENTS

Besides the basic problems inherent in making subnanosecond measurements, high-speed testing becomes even more difficult when MOS VLSI circuits must be evaluated. Unlike ECL devices, which are usually designed to drive 50-Ω loads, NMOS and CMOS VLSI devices are designed to work into high-impedance loads. Consequently, these devices are mismatched to the transmission lines leading back to the pin electronics, and the tester appears as a capacitive load. Test-head capacitance can typically run 50 pF or more. High-speed testing becomes a problem when the DUT sees a higher capacitance than it was designed to drive.

It is no surprise then, that capacitance gets a lot of attention in some of the newly introduced testers. For example, the T3342, a 40-MHz, 256-pin VLSI tester from the



3. In a conventional shared-resource test system, a limited number of timing generators are passed through a switch matrix to groups of device pins (a). The resultant timing paths are complex and contain many error sources. In contrast, the tester-per-pin architecture of the MegaOne tester from Megatest simplifies the timing path by dedicating a separate timing generator for each DUT pin (b).

Advantest America Inc. (Lincolnshire, Ill.), sports a test head that holds capacitance to 30 pF.

Low capacitance was also one of the primary design goals for a CMOS VLSI tester from Trillium Corp. (San Jose, Calif.). That goal was achieved with a 256-pin test head that is 20 in. in diameter and 10 in. deep. The tester pin electronics are placed in a radial pattern approximately 4 in. from the DUT pins. Connections between the DUT socket and the pin electronics card were made with a flexible waveguide circuit. Using this approach, capacitance on any of the 256 test pins measures 20 pF ± 2 pF. In a matched 93-Ω environment, the transmission line capacitance is considerably reduced.

Also based on the tester-per-pin architecture, the Trillium system has an autocalibration scheme that uses two time-domain reflectometry systems running synchronously. Through a multiplexer, one TDR pulse generator is connected to each pin card on the test head via a coaxial cable. The other TDR system supplies a reference delay against which to compare the measured pin-card delay.

Calibration begins when a reference edge is transmitted to each comparator and when the response circuitry and comparators are aligned to those edges. The driver and format circuitry associated with each comparator are then aligned. In this manner, all driver and comparator path errors are determined and calibration values for each edge are stored in a special memory. Next, using the round-trip delay vernier, the response circuitry is offset in relation to the format circuitry. The amount of offset is equal to the actual round-trip delay from the driver to the response circuitry. As the individual timing generators are programmed at run time, a high-speed hardware adder sums up the stored calibration values and the programmed values of the edges.

The autocalibration technique constrains the total error from the format circuitry to the DUT and back to the response circuitry to less than ± 25 ps per path. As a result, an overall timing accuracy of ± 250 ps is specified across all 256 tester pins.

In addition to verifying that the DUTs actually work, VLSI testers are being summoned to perform F_{max} (maximum operating frequency) testing, which recently became a requirement under MIL-STD 38510. Basically used in engineering applications, F_{max} testing is coming on strong in production environments because it can be a more meaningful indicator of device functionality in end-use situations than conventional ac parametric tests.

The F_{max} parameter is most critical in clocked logic devices. Here, F_{max} represents the highest frequency that, when applied to the device's clock input, will permit the output to switch normally. In such a state, the output pulses will track the input correctly, and the output voltage excursion will be at least equivalent to the 10% to 90% value of the logic 1 and logic 0 voltages specified at lower frequencies.

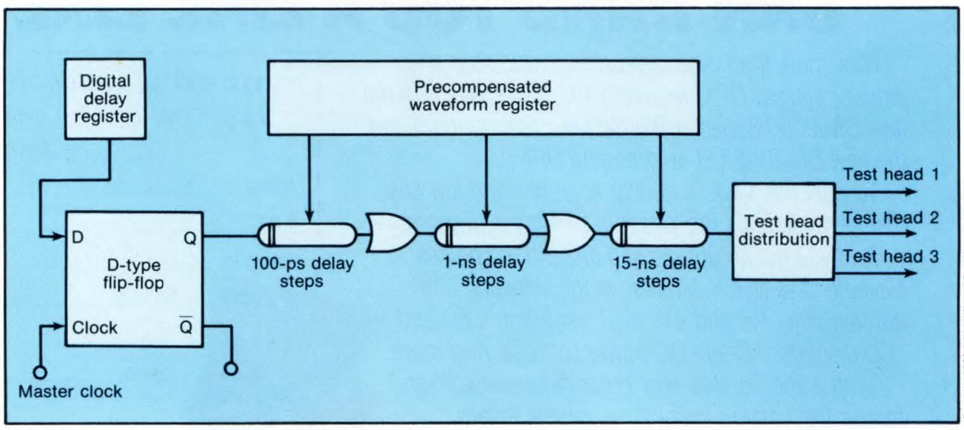
In the engineering test, device parameters such as setup and hold times are set at worst-case values. The clock input signal's duty cycle is a function of these settings. As the input signal approaches the device's maximum operation frequency, the resultant output signal begins to round out and become sinusoidal, eventually dropping below acceptable logic voltage levels.

GETTING VALID RESULTS

In the production F_{max} test, steps are being taken to ensure that other parameters do not affect the test's outcome. For instance, setup and hold times and input drive voltages are set at nominal values rather than at the extremes. The input waveform is a square wave with a 50% duty cycle and risetime characteristics optimized for the device family being tested. Device failures resulting from these conditions are usually absolute: The chip simply ceases to produce an output.

Some controversy exists, however, about the relative

4. Each of the Mega-One's timing generators has a delay that can be adjusted in 100-ps increments. A timing table in the precompensated waveform register handles channel deskewing using delay values obtained during the automatic calibration process.



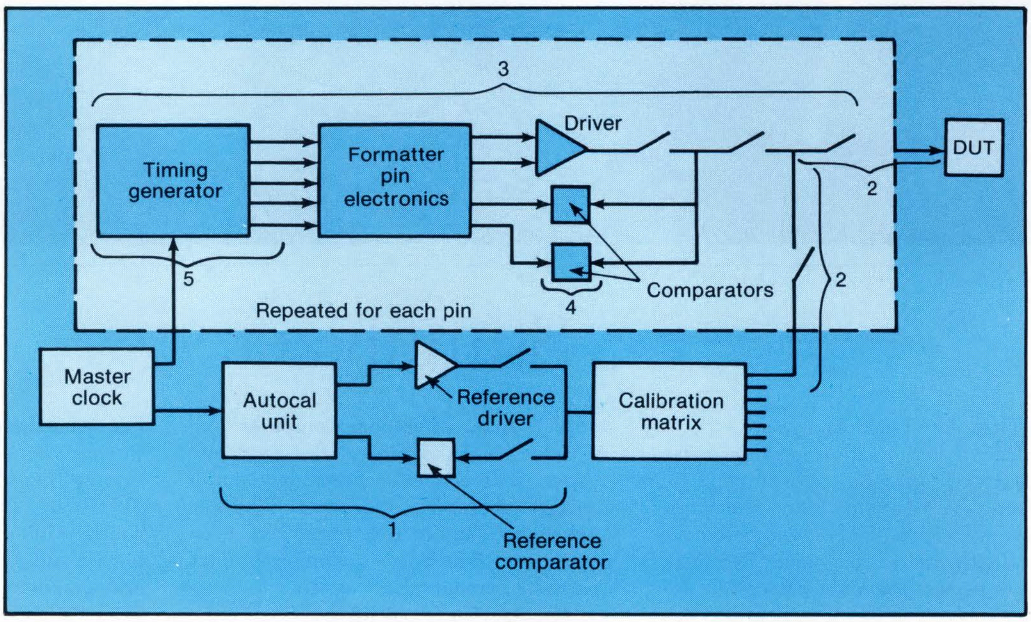
Source: 1983 International Test Conference

validity of these two approaches. The characterization test method actually tends to produce higher, and therefore more desirable, F_{max} readings. But some users are concerned about how meaningful the results are under real-world operating conditions. Granted, the chip can operate at 120 MHz, but its output at that frequency is almost a sinewave. And the next circuit in line (in the end-use environment) may not react properly to such a waveform.

A practical F_{max} test hardware implementation must meet several requirements: It must produce a square wave with very low aberrations. It must provide a low-loss, high-fidelity signal path to and from the DUT. And there must be program-controlled, switchable signal routing between the high-frequency stimulus and measurement subsystems and any device pin. Moreover, the test system and its fixturing must be able to perform all device tests—functional, ac, dc, and F_{max}—with a single insertion of the DUT (especially critical in production test applications). The fixturing has to provide the proper dc loading to the device situated close to the output pin(s). The test system must also provide isolation from unwanted loading caused by cabling and response instruments. If the test system's comparators are to be used in processing the DUT output signal, they must be capable of handling frequencies equivalent to $F_{max}/2$. The programmable pulse generator must have high resolution, accurate pulse positioning, very good timing linearity, high slew rate, and low pulse distortion. Furthermore, the response instruments (counter, digitizer, comparator) must have high resolution, accurate strobe positioning, precise voltage thresholds, and very low stray capacitance.

Two IC test systems from Tektronix—the S-3225 advanced logic tester and the S-3295 VLSI test system—come with F_{max} test options. In each case, the F_{max} option consists of a special coaxial signal path between the DUT fixture and the external rack-mounted IEEE-488 instruments, namely, the E-H Model SPG 2000 pulse generator and the Hewlett-Packard Model 5335 counter. For more critical measurements, the counter may be replaced with a Tektronix waveform digitizer.

When test time must be kept low, the preferred approach is to use the counter to measure the DUT output frequency. The system comparator detects threshold crossings and acts as a buffer and line driver between the DUT and the counter. This architecture effectively measures F_{max} frequencies up to 160 MHz. For engineering applications, the configuration most often chosen is a waveform digitizer (Tektronix Model 568 or 7912) connected directly to the DUT. With this setup, F_{max} measurements up to 200 MHz can be made; the DUT output waveforms can be recorded as well. □



5. Autocalibration in the MegaOne tester is a sequential process referenced to an NBS-traceable crystal oscillator located in the system's master clock. The procedure begins with self-calibration of the autocalibration system (1). Then measurements determine the physical path lengths (2), the timing chain propagation delay (3), and the delay variations caused by pin-electronics voltage levels (4). During the final calibration phase, a precompensated timing table is generated (5).

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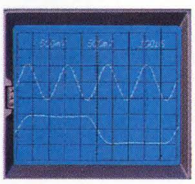

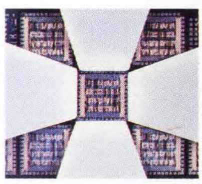

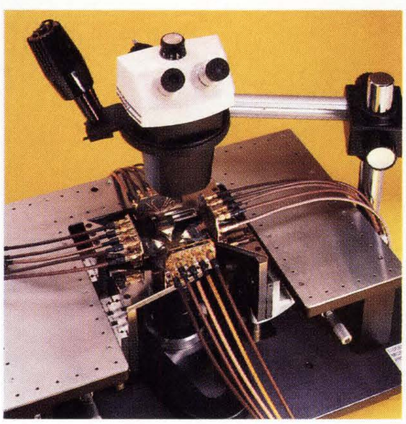

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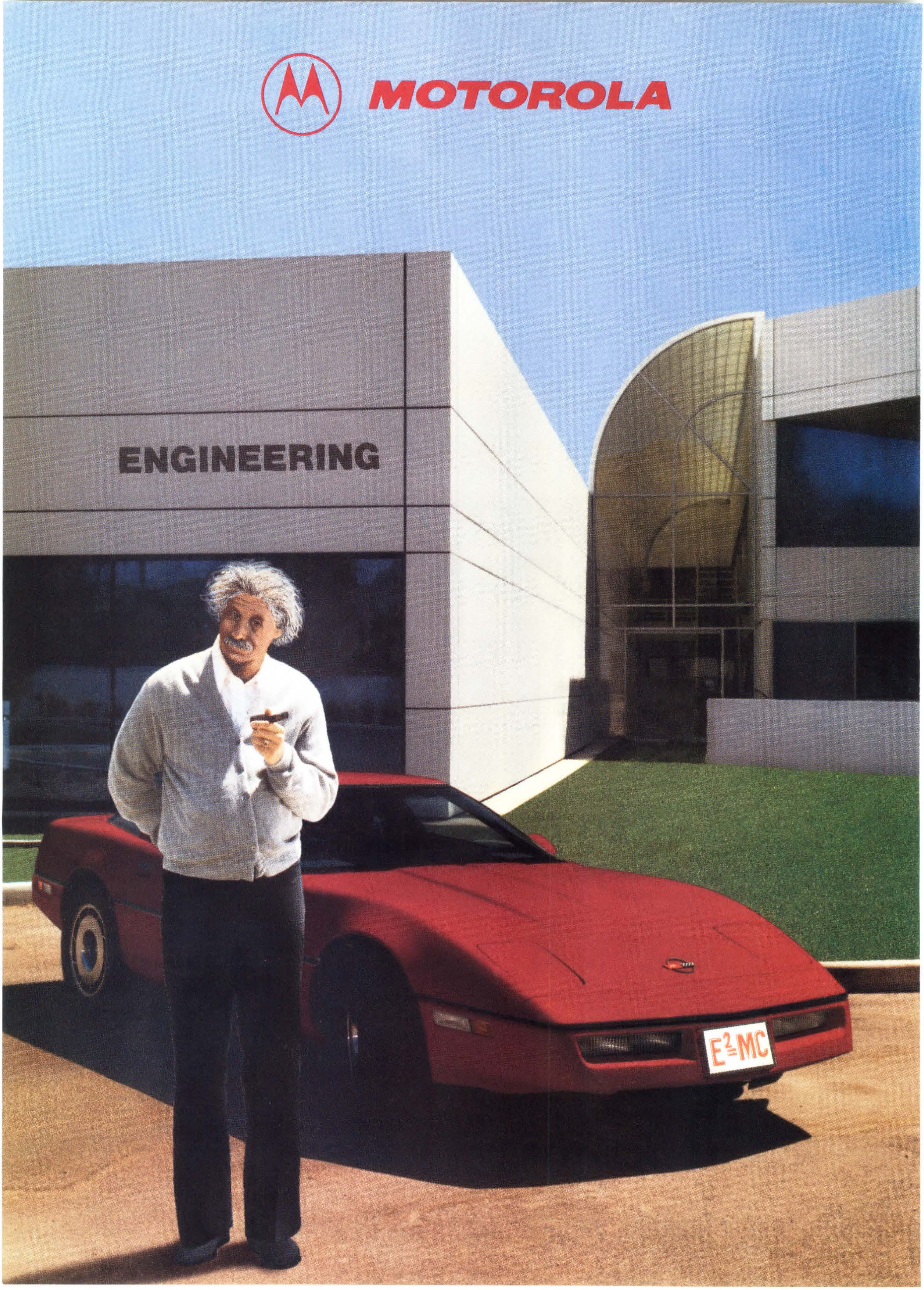
CIRCLE 73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Use this coupon or get one from your Motorola sales representative or local authorized distributor. Contest M68HC11EVBs are available only from participating distributors, so present your filled-in coupon at one of their locations and make the special $68.11 purchase that qualifies you.

Use the EVB and other contest materials to develop and debug the design of your choice. Complete and submit the design to Motorola by 11-15-86. Working prototype and all necessary documentation are required. We'll rebate the $68.11 for the contest EVB when your qualified entry is received at Motorola E^2=MC Design Contest, 6501 William Cannon Drive West, Austin, TX 78735.

Judging criteria include innovativeness of on-chip E^2PROM use, demonstrable benefit of HCMOS and application of on-chip peripherals—A/D, Asynchronous and Synchronous Serial Systems, Pulse Accumulator, Main Timer, Parallel I/O, STOP and WAIT modes, Watchdog Timer, and Variable Priority Interrupts. Judges decisions are final.

Winners will be announced and notified by 12-31-86. Design contest entries will be returned.

To purchase your Contest EVB and become eligible for the Motorola E^2=MC design contest, present the coupon to your participating Motorola distributor. If the coupon is gone, your Motorola sales representative or distributor can provide one.

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We don't offer special training just for the contest, but any designer can sign up for one of Motorola Technical Training's acclaimed MCU courses. They're scheduled regularly throughout the year.

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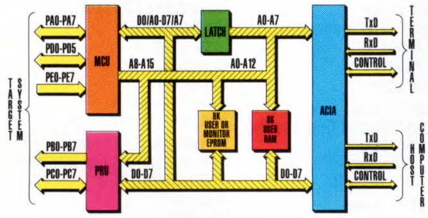
Your E^2=MC Contest EVB.



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ELECTRONIC DESIGN EXCLUSIVE

Programmable filter chip and its PC-based tools offer new analog solutions

A switched-capacitor filter chip that can be configured in software through its PC development system lets even novice designers create complex analog filters.

Thomas Dille, Douglas Holberg, and Roger Taylor
Crystal Semiconductor Corp.
2024 E. Saint Elmo Rd.
Austin, TX 78744
(512) 445-7222

When a system requires a complex filter, even an experienced analog hand can begin to pray, "please make it go away." Such a filter not only presents a difficult design job, but poses entangled cost-performance trade-offs among varied frequency responses and different circuit topologies.

Since the responses of digital filters depend completely on stored programs, they may seem ideal for tasks requiring adaptive or high-order filters. However, they need a digital input signal and thus call for analog-to-digital converters on the front end. In addition, for analog output, a companion d-a converter must join the design. Furthermore, a digital filter often requires extensive software development.

These requirements combine with the cost of the necessary digital signal processor to make a digital filter much too costly for most jobs. In fact, digital filters most often are used in systems when the DSP chip is "free"; that is, the processor already exists in the system for another purpose.

On the other hand, analog filters offer a designer a bewildering array of filter implementations. Unfortunately, each type and, consequently, each new design present an engineer with another design challenge. Since analog filters lack the flexibility of digital designs, they remain the domain of a specialist who, after weeks of painstaking trial and error and what seems to be black magic, finally produces a filter that does the job.

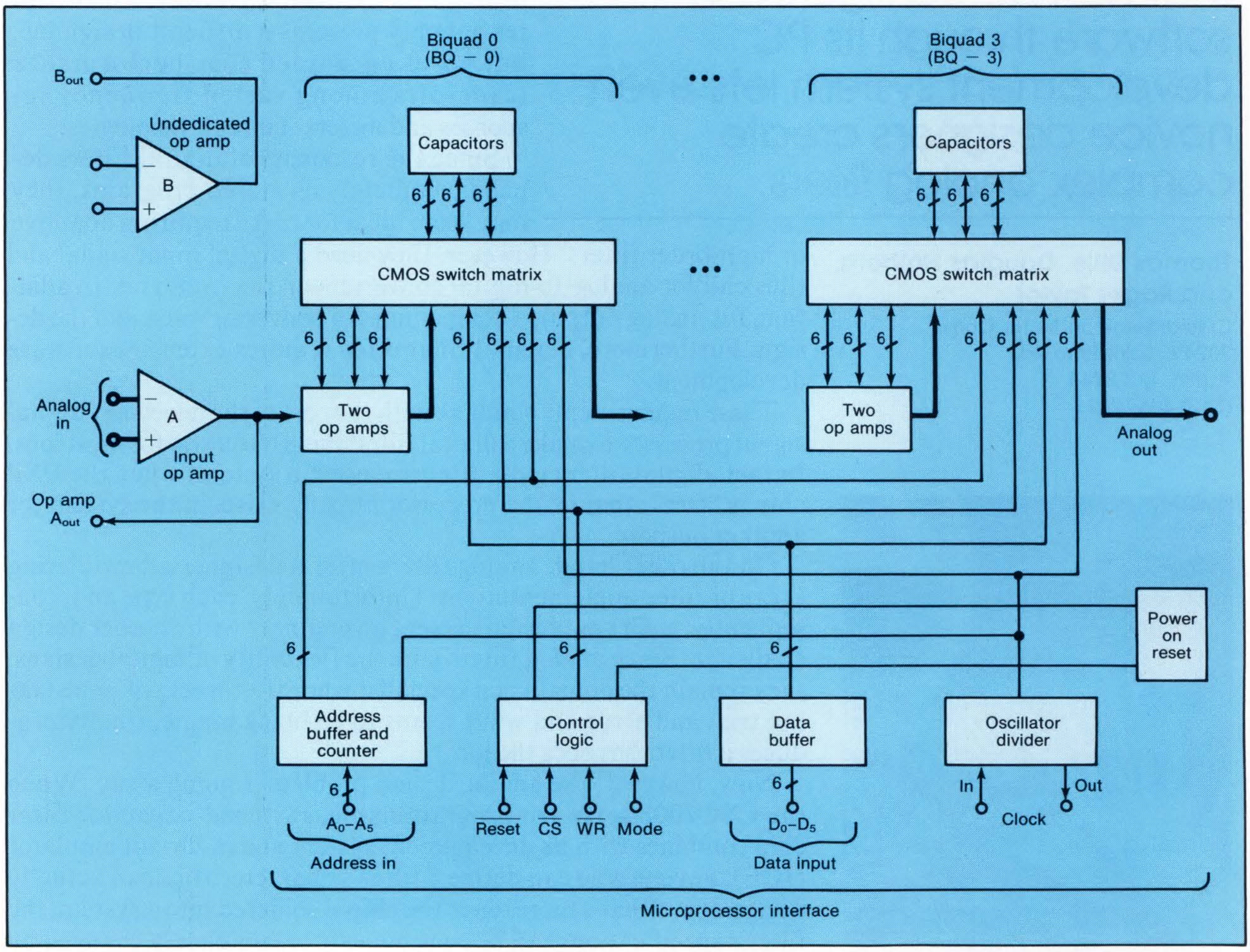
Now, however, the analog design problem is going away. When the CSC7008 software-programmable, switched-capacitor filter chip combines with its development system and in-circuit emulator (ICE), anyone who can define a filter's characteristics can actually design one. What's more, once the chip is soldered into a system, the filter's specifications can be continuously or completely changed by a host microprocessor or a simple thumbwheel switch. Or the filter can read the coefficients that determine its qualities from a special or general-purpose external memory.

The programmable filter gives an engineer the flexibility of a digital filter and the cost-effectiveness of an analog filter. Moreover, the filter needs no external passive components to define its response, thereby eliminating major manufacturing and testing problems. In addition, unlike digital filters, the chip does not require a-d or d-a converters, further reducing cost.

The filter's capability for reprogramming opens up a variety of new filter tasks that stir a designer's imagination. The choices range from realizing filters for spot noise measurement in op-amp test systems to controlling the cutoff frequency and the Q of a low-pass filter in a phase-locked loop. In a feedback loop, an external program can direct the chip to hunt for fixed signals or a family of signals.

A series of digital words programs the chip into 10^{79} different configurations. The input words turn the chip into individual or combined high-pass, low-pass, band-pass, band-stop, and all-pass filters. They also give it any response from eighth-order down, with a Butterworth, Chebyshev I or II, or elliptic form. The digital words vary the clock frequency, too.

The chip's nearly infinite flexibility makes the Crystal-ICE development system almost indispensable. The system ICE consists of software for filter synthesis and coefficient generation, as well as the emulator. The software and ICE work with an IBM PC or compatible computer equipped with an 8087 coprocessor and a high-resolution graphics card (the Hercules or its equivalent). The software generates a menu through which the designer specifies the filter completely in frequency-domain parameters. After the designer verifies the filter-response plots produced on the PC, the coefficient-generation software



1. The CSC7008 programmable, switched-capacitor filter chip can be internally connected in 2^{264} different ways by applying digital words to its microprocessor interface. CMOS switches lead the analog signal through the biquad filter sections while forming filters that range in complexity from a simple order, low-pass circuit to an eighth-order Chebyshev II band-pass design.

takes over and determines the digital words to drive the filter. The emulator is inserted between the PC and the system destined for the filter. A special emulator pod plugs into the filter's socket.

The designer then exercises the system with the filter he has just designed and specified. Unlike any previous filter design process, if the system performs below par, major or minor filter changes can be made—instantly—and at no cost. Furthermore, the standard pinout and microprocessor interface of the chip permit the system to be designed and prototyped long before the required filter response has been determined. In fact, the CSC7008 chip is treated as a microprocessor peripheral during the design stage.

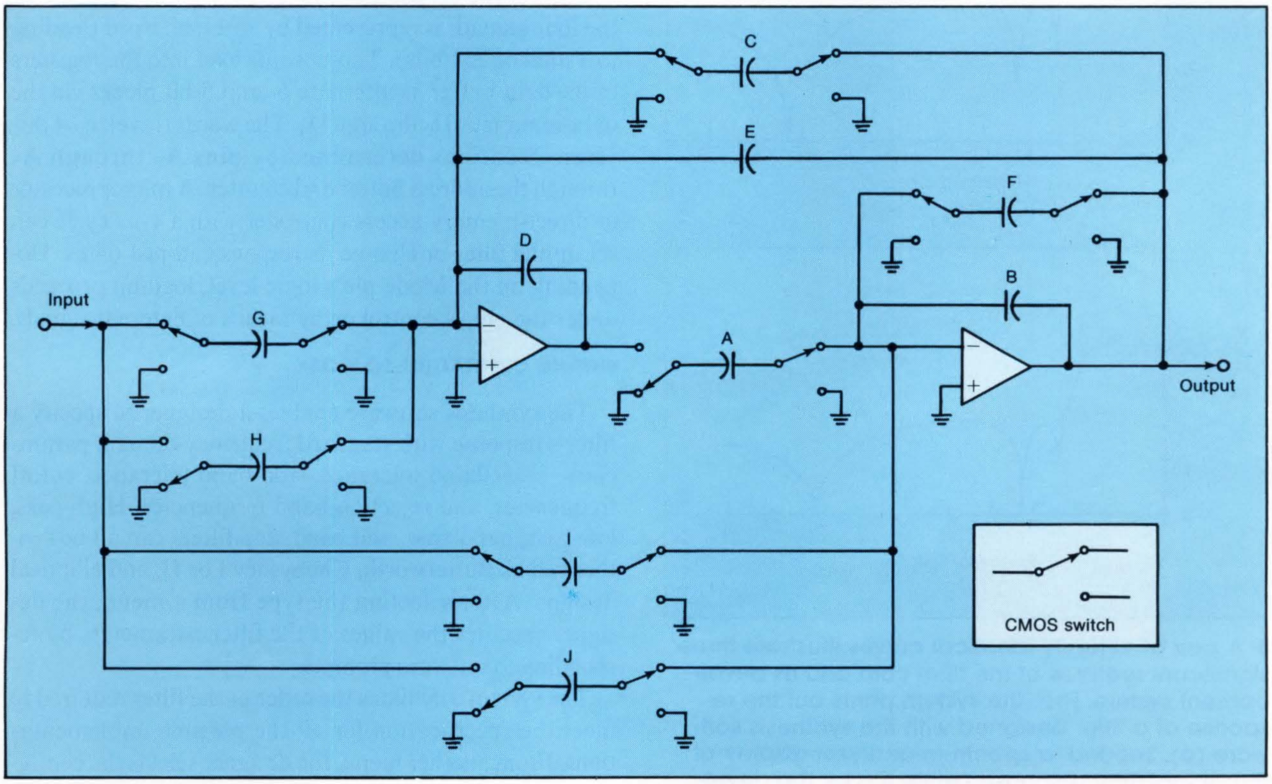
FOUR OF A KIND WINS

At the heart of the chip lie its four biquadratic filter sections, BQ-0 through BQ-3 (Fig. 1). Each biquad consists of a pair of op amps, a bank of CMOS switches (transmission gates), and a binary-weighted capacitor array. Under the direction of the input digital words presented to the chip's microprocessor interface, the switches create a specific filter by connecting the capacitors around and between the two op amps.

The signal to be filtered connects with the differential input of op amp A. That input functions with external resistors and capacitors as an antialiasing filter. Op amp A can also set signal gain. If needed, undedicated op amp B either supplies additional input filtering, or it can be added at the output to smooth the stair-step product of the biquads. Between the output of op amp A and the output of BQ-3, the digitally controlled CMOS switches direct the analog signal through one or more of the biquads. For example, an eighth-order filter requires all four biquads, while a fourth-order filter needs just two. However, biquad 3 always connects at the device's output.

Each of the four biquads emulates a Ghausi/Laker biquadratic filter (Fig. 2). With the exception of feedback capacitors B and D, which are fixed at a normalized value of 1024, the switches program all the capacitors at normalized values between 0 and 2047. (The ratio of the normalized values of pairs of capacitors in the circuit determines its frequency response.)

Selection of a J or H capacitor depends on the type of filter response required. For example, of all the filter types incorporating a bilinear Z transform, only the band-pass

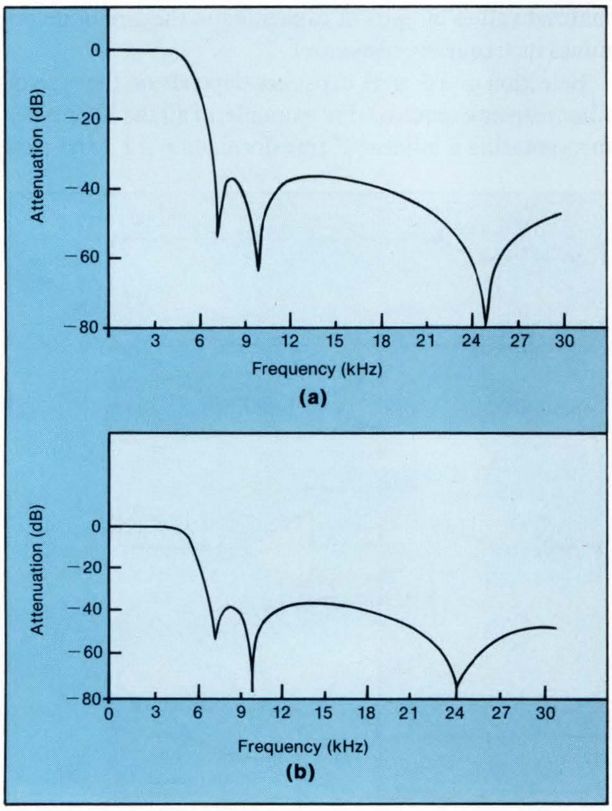


2. CMOS switches can program the 10 capacitors, A through J, in each of the chip's biquads to form Butterworth, Chebyshev, or elliptic filters. Similarly, the value of the capacitors are varied to give the filter virtually infinite resolution in frequency response from dc to 20 kHz.

circuit requires an H capacitor. To further enhance flexibility, either the circuit containing the E capacitor or that containing the F capacitor can be chosen for damping. That choice, made automatically by Crystal-ICE, minimizes quantization errors in selecting the capacitor coefficients, which in turn optimize the accuracy of the filter's response.

Scaling the dynamic range of the signals handled by the op amps also improves filter response. Crystal-ICE does the job by adjusting capacitor values so that the maximum analog voltage at the output of each op amp is the same. Thus, only the noise floor and the power-supply voltage limit the dynamic range of the filter, which is typically 70 to 80 dB.

Since a total of 264 bits configure the chip, and most of these determine the frequency response, cutoff frequency resolution is virtually continuous. Furthermore, some of these bits control the sampling frequency response by programming the oscillator divider block to divide the clock by a factor of 1 to 128 in eight binary increments. The chip can use either an external clock or a low-cost crystal tied between the two clock pins.



3. A pair of virtually identical curves illustrate three significant features of the filter chip and its development system. First, the system prints out the response of a filter designed with the synthesis software (a). Second, a spectrum-analyzer display of the actual filter response (while run by the development system), enables the designer to test the filter immediately after its design (b). Finally, the curves are nearly identical, verifying accuracy.

HOW GOOD IS IT?

To attain its versatility, resolution, and ease of use, the filter sacrifices not one bit of accuracy. When programmed to provide cutoff frequencies between dc and 20 kHz, the typical tolerance on its pass-band corner is better than 1%, and the actual Q is within 2% of the calculated Q for values under 10. Those tolerances increase slightly as the sampling frequency approaches its maximum of 270 kHz but remain under 2% for the pass-band corner and under 5% for Q.

Even more important, variation in cutoff frequency from one chip to another is negligible—less than the difference between actual and calculated values. As cutoff frequencies rise to 50 kHz, accuracy degrades somewhat, but production units will vary in cutoff frequency by less than 2%. Thus, a system demanding 50-kHz cutoff can still be manufactured in volume.

Each of the six coefficients that define the response of the four biquads is represented by an 11-bit word (leading to a total of 264 bits). Those words load into the registers in the data buffer as alternate 6- and 5-bit blocks via the data-input pins D_0 through D_5. The words travel to 64 different locations determined by pins A_0 through A_5 through the address buffer and counter. A microprocessor or direct-memory-access controller with a 1-μs cycle can set up the filter or change its response, in just 64 μs. Depending on the Mode pin's logic level, loading proceeds under the chip's control or by means of external signals.

PUTTING CRYSTAL-ICE TO WORK

The synthesis software enables a designer to specify a filter's response with standard frequency-domain parameters—pass-band tolerance, stop-band tolerance, cutoff frequencies, and rejection-band frequencies. High-pass, low-pass, band-pass, and band-stop filters can all be synthesized as Butterworth, Chebyshev I or II, and elliptical designs. After selecting the type from a menu, the designer specifies the values of the filter parameters by responding to software prompts.

The system calculates the order of the filter required to meet the specification for all the possible implementations. From another menu, the designer selects the configuration that best meets the need of the application. For evaluation, the system generates plots of magnitude vs frequency, decibels vs frequency, phase vs frequency, as

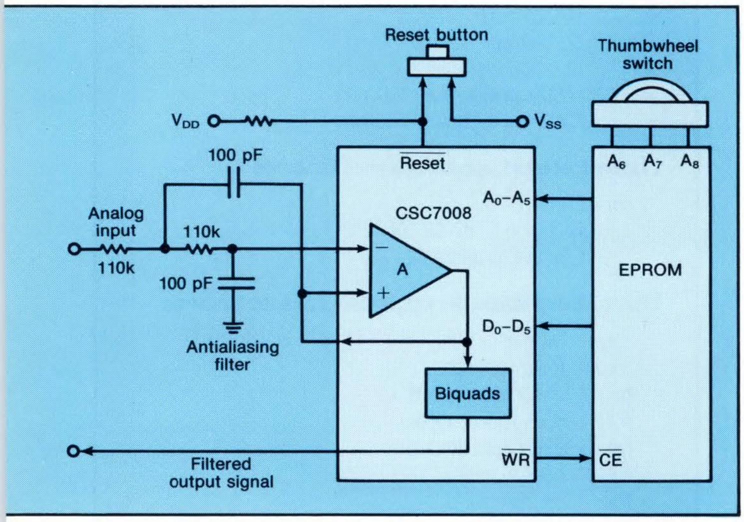
well as poles and zeros. The third menu selects the graph for display or hard copy (Fig. 3a).

Once a suitable filter response has been synthesized, the coefficient-generation software takes over. It produces both the appropriate biquadratic equations and the final filter coefficients derived from those equations. With yet another menu, the designer can obtain coefficients for the biquadratic equations, the normalized values of the capacitors in the biquads, and the final CSC7008 coefficients.

At this stage, the user can intervene to modify the development system's responses. In fact, if the system designer has already determined the biquadratic equations, he can bypass the synthesis portion of the program and enter the equations as a starting point. Unused biquads on the chip can be configured as all-pass filters for phase equalization in tasks where linear phase response is important. The unused biquads may also be used to compensate for the droop caused by sin x/x distortion when the signal frequency is very close to half the clock or Nyquist frequency.

EMULATING THE FILTER

Assuming the final system exists in breadboard form, the emulator can give the designer instant feedback on the fit of the filter response with the job's requirements. After the PC, emulator, and breadboard are connected, the coefficients are loaded into the emulator, which appears to



4. The programmable filter can build a variable-frequency filter in which a thumbwheel switch determines the frequency response. A continuous-time, antialiasing filter on its front end, built with an op amp on the chip and external resistors and capacitors, eliminates aliasing caused by the sampling nature of switched-capacitor filters.

Price and availability

The CSC7008 switched-capacitor filter chip and its Crystal-ICE filter development system are available now. In quantities of 100, the chip sells for $30 each. The development system, including software, in-circuit emulator, and a user's manual is $3599. CIRCLE 503

the designer as a functioning filter in the circuit. The complete system can now be tested in real time. If the filter needs modification, new designs can be tried immediately. A spectrum analyzer linked to the emulator pod compares the calculated response with the performance of the actual filter. The frequency-response graphs generated by the development system can be matched with the display on the spectrum analyzer (Fig. 3b).

The CSC7008 filter chip lends itself to the front end of a data-acquisition system that the user programs manually with a thumbwheel switch (Fig. 4). Such a system might be used for quality control in a food-processing plant or other factory. Various types of signals from sensors or instruments require band-limiting at one of five cutoff frequencies (in this example, at 2, 4, 6, 8, and 10 kHz).

In its self-programming mode, the filter simply clocks through successive locations in the external memory, beginning with the binary address 00000. It loads the words found in each location into its internal registers to set up the filter's configuration. That sequence is initiated either by applying power or by activating the reset button. The thumbwheel switch gives the first three address bits, selecting different blocks of memory at each position. Pressing the reset button (after positioning the thumbwheel) starts the boot-up sequence and, therefore, configures the filter to the desired response.

A simple second-order antialiasing filter, incorporating the chip's input op amp, ensures that the input signal is attenuated at least 40 dB at the Nyquist frequency (about 130 kHz) to avoid wrap around and corruption of the signal in the pass-band. Its response is set by two external 100-pF capacitors and two 100-kΩ resistors.

The pass-band amplitude must be greater than 70.7% of full scale, or 3 dB down, at the cutoff frequency. The signal should be attenuated to less than 1% of full scale, or −40 dB, at a quarter of an octave above the cutoff frequency. Although the filter should be maximally flat in the pass-band, phase response is unimportant. The development system generates filter responses meeting those criteria. A 257-kHz sampling rate exceeds the maximum pass-band frequency to simplify antialiasing, and sin x/x distortion is insignificant. The clock is implemented with

DESIGN ENTRY

Cover: Software-programmable filter

a low-cost, standard 1.544-MHz crystal.

The designer then enters other filter specifications into the development system. For example, following the prompts, he defines the 2-kHz filter by entering passband as 0.7071 of full scale, cutoff frequency as 2 kHz, rejection band as 0.01 of full scale, and upper rejection frequency as 2.5 kHz. For this application the user chooses an eighth-order Chebyshev II filter because it combines a flat pass-band characteristic with a steep roll-off.

ICING THE DEAL

After filter coefficients are calculated, the filter is tested in the data-acquisition system using the in-circuit emulator. Its response can then be modified and retested if necessary. Once a satisfactory filter is obtained, the CSC7008 coefficients are programmed into the EPROM, and the system is ready to go. Determining all coefficients and testing takes about an hour.

In an adaptive application, based on a form of system feedback, a microprocessor replaces the thumbwheel switch. For example, when the processor monitors the output of the data-acquisition system, it boosts or reduces the filter's cutoff frequency upon detecting a predetermined condition. For example, loss of signal could cause an increase in cutoff frequency; extraneous noise could bring about a decrease.

The filter synthesis software for the Crystal-ICE development system was created by Crystal Semiconductor in conjunction with the University of New Mexico in Albuquerque.

Tom Dille is a marketing manager at Crystal Semiconductor, responsible for the filter and data conversion product lines. He holds a BSEE from Rice University and an MBA from the University of Michigan.

Douglas Holberg, an IC design engineer, leads the universal filter project at Crystal Semiconductor. Before that, he designed custom ICs for biomedical applications at Texas Micro-Engineering, which formed the core of Crystal Semiconductor. He holds a BSEE from Texas A&M University.

Roger Taylor is an application engineer responsible for supporting Crystal's Smart Analog filter and telecommunication products. He received his BSEE from the University of Texas at Austin.

How valuable?	Circle
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Moderately	542
Slightly	543

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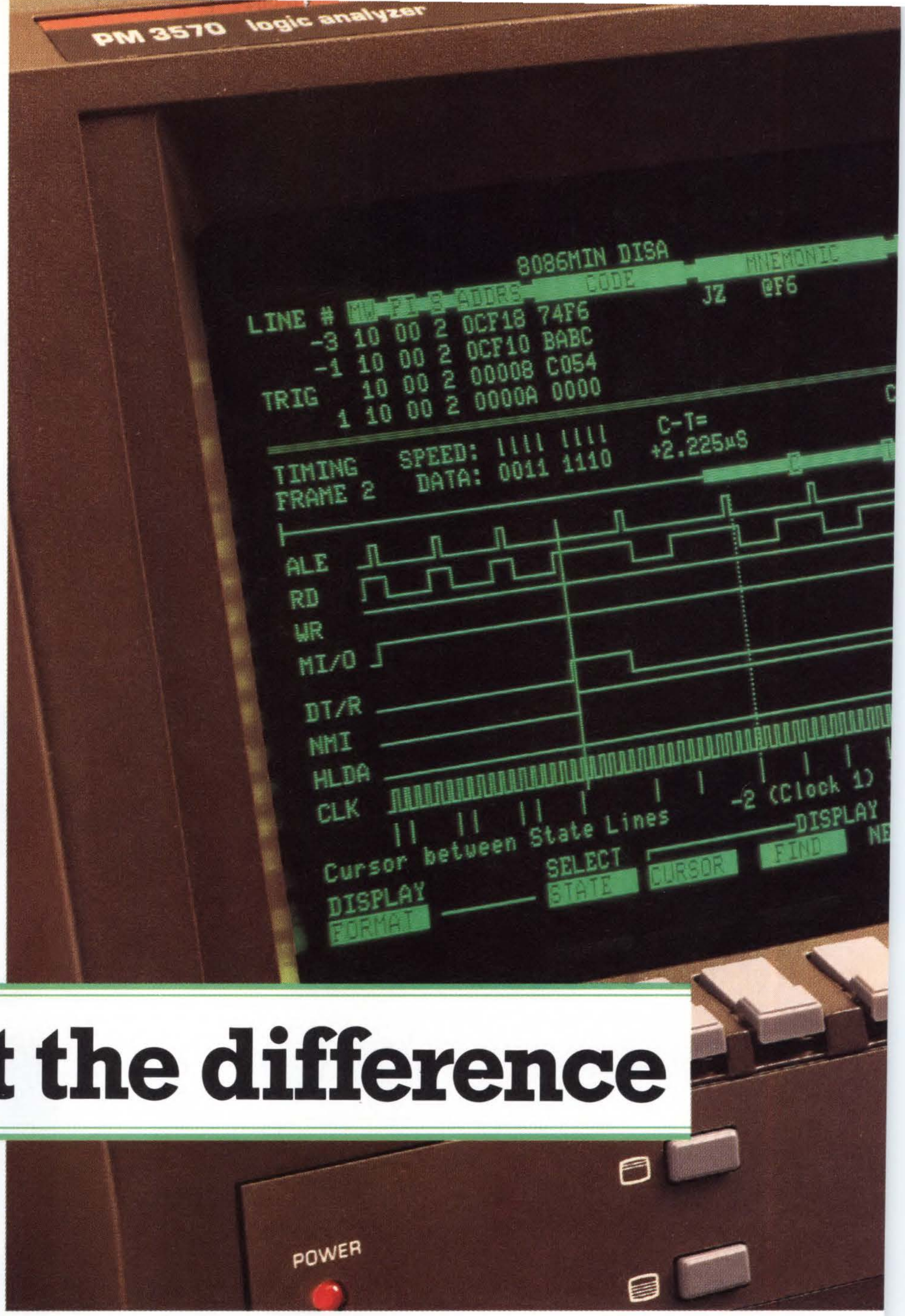

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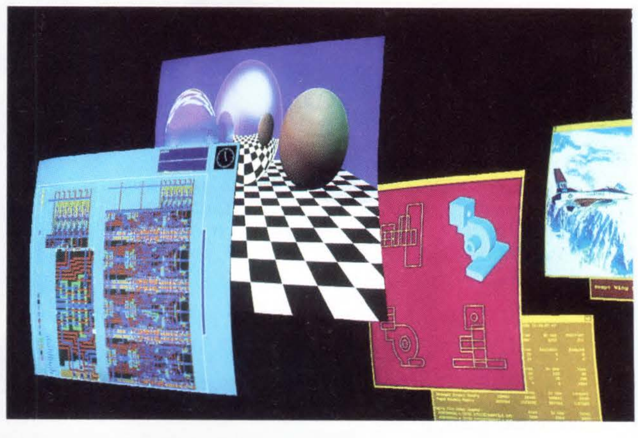

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CIRCLE 82

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CIRCLE 83

ELECTRONIC DESIGN EXCLUSIVE

Graphics coprocessor chip gives small systems a look at the big picture

With independent graphics and display processors inside, a chip creates multiple windows of variable-depth pixels. Memory and CPU demands now fall within small systems' reach.

Martin Randall and
Arun Johary
Intel Corp.
400 Encinal St.
Santa Cruz, CA 95060
(408) 429-8288

The push is on to equip personal computers and low-end workstations with the sophisticated display capabilities expected from dedicated graphics processors and expensive workstations. But complex video features—notably, windows—take a toll in small systems. Foremost, they eat up memory space. Second, the system CPU usually must execute any graphics instructions, adding to its normally heavy workload. Clearly, double duty of that sort can compromise overall performance. Worse still, graphics standards like the Virtual Device Interface (VDI) demand CPU-like intelligence, a factor that foretells an even bleaker future for small systems that shoot for tricky graphics through CPU execution.

A coprocessor chip suddenly brightens the picture. Matching the capabilities of conventional graphics boards, the 82786 combines two independently programmable processors—one for drawing images, the other for displaying them. Both sections execute instructions from a dedicated graphics memory they share.

Unlike other graphics chips, the coprocessor can address several bit maps at once; as a result, it can generate windows or update a screen instantly, without time-consuming block transfers. Moreover, because it executes instructions in parallel with the CPU, it can manipulate those windows 100 times faster than the CPU can alone. For the same reason, VDI drawing commands run 10 times faster.

Variable-depth bit maps make the chip particularly attractive for small systems, since it thus wrings out the most image data from memory. Uniquely, the coprocessor can blend pixels 1 to 8 bits deep in a single display. As a result, it can simultaneously create text from single-bit pixels and generate high-quality graphics from multiple-bit pixels—in the same display and without any unneeded bits. In contrast, other chips must store all pixels at the maximum bit depth, even those for text. Moreover, because the coprocessor's graphics memory can hold multiple bit maps, it can store more than one image. Each bit map serves as a canvas for a set of operations that draw lines, create polygons, and fill areas with color.

Although the chip carries an interface optimized to fit the 80286 microprocessor, it hooks up with other popular CPUs, like the 8-bit 8088, the 16-bit 8086, and the 32-bit 80386. Through its own arbitration logic, the coprocessor can access system memory, thereby sharing information with the CPU if necessary. In addition, its display processor sports programmable circuitry for driving not just the customary CRTs but high-resolution printers and plotters as well. The high degree of integration eliminates the need for much glue logic—a must for small system designs.

LOW POWER, HIGH INTELLIGENCE

To conserve system power, the chip is built with the identical advanced CHMOS process used for the 80386. Combined with up to 32 dynamic RAMs, it dissipates well under 1 W. Thus, the coprocessor, some graphics memory, and a CPU can comfortably occupy the same printed-circuit board (Fig. 1).

The brains of the chip, the graphics and display processors, form a versatile duo. The graphics processor executes commands from the host and updates graphics and text in the dedicated memory. The display processor, independently of its graphics partner, collects bits linearly from the memory and sends them out as pixels to a CRT, laser printer, or other output device. Thus, it goes beyond simply managing a cursor and driving a video display: It redefines the role typically associated with the display function.

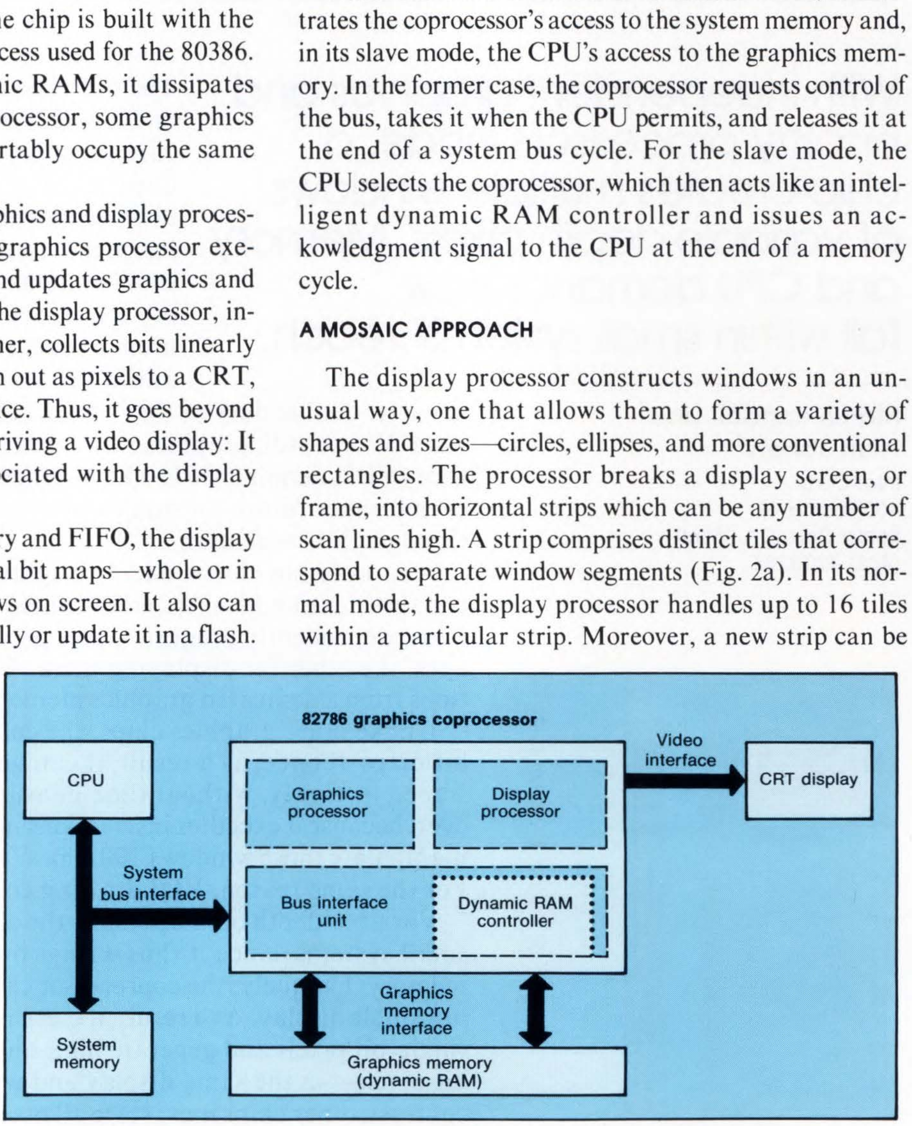
Through its formatting circuitry and FIFO, the display processor can jump among several bit maps—whole or in part—to create multiple windows on screen. It also can expand an image two dimensionally or update it in a flash. What's more, data is fetched directly from the various bit maps and sent directly to the screen, obviating the need for a frame buffer.

Along with the graphics and display processors, the coprocessor incorporates a bus interface unit. This functional block contains a dynamic RAM controller and mediates both coprocessor and CPU access to the graphics and system memories. The RAM controller reduces the overall chip count and performs burst-mode accesses as fast as 40 Mbytes/s.

When the bus interface is in its master mode, it arbitrates the coprocessor's access to the system memory and, in its slave mode, the CPU's access to the graphics memory. In the former case, the coprocessor requests control of the bus, takes it when the CPU permits, and releases it at the end of a system bus cycle. For the slave mode, the CPU selects the coprocessor, which then acts like an intelligent dynamic RAM controller and issues an ackowledgment signal to the CPU at the end of a memory cycle.

A MOSAIC APPROACH

The display processor constructs windows in an unusual way, one that allows them to form a variety of shapes and sizes—circles, ellipses, and more conventional rectangles. The processor breaks a display screen, or frame, into horizontal strips which can be any number of scan lines high. A strip comprises distinct tiles that correspond to separate window segments (Fig. 2a). In its normal mode, the display processor handles up to 16 tiles within a particular strip. Moreover, a new strip can be



1. The 82786 graphics coprocessor matches the functional capability of a board. It contains two processors—one that draws and one that drives displays—a bus interface unit and a dynamic RAM controller. Arbitration logic in the bus interface unit allows the CPU to access the graphics memory and the coprocessor to access system memory.

defined at each scan line.

The CPU sets up information about the strips and tiles as a series of descriptors in the graphics memory. Using that information, the display processor fetches pixel data from different bit maps and prepares it for the window format. During the vertical blanking period, the display processor accesses the first strip in a frame, getting the strip's address from one of a block of pointer-display control registers.

The window-strip descriptor table typically contains a header followed by as many separate tile descriptors as needed to define the strip (Fig. 2b). For a given frame, a pointer field in each header directs the display processor to the next descriptor.

To update an image, the display section simply reads a new set of tile descriptors. The pointer-link scheme allows the processor to move, scroll, and pan across an image by reading new descriptors, not by moving blocks of pixels or by redrawing a frame buffer. That scheme makes quick work of updating a screen. As for the CPU, it is needed only to change descriptors that arrange the windows in the display frame.

REGISTERS IN CONTROL

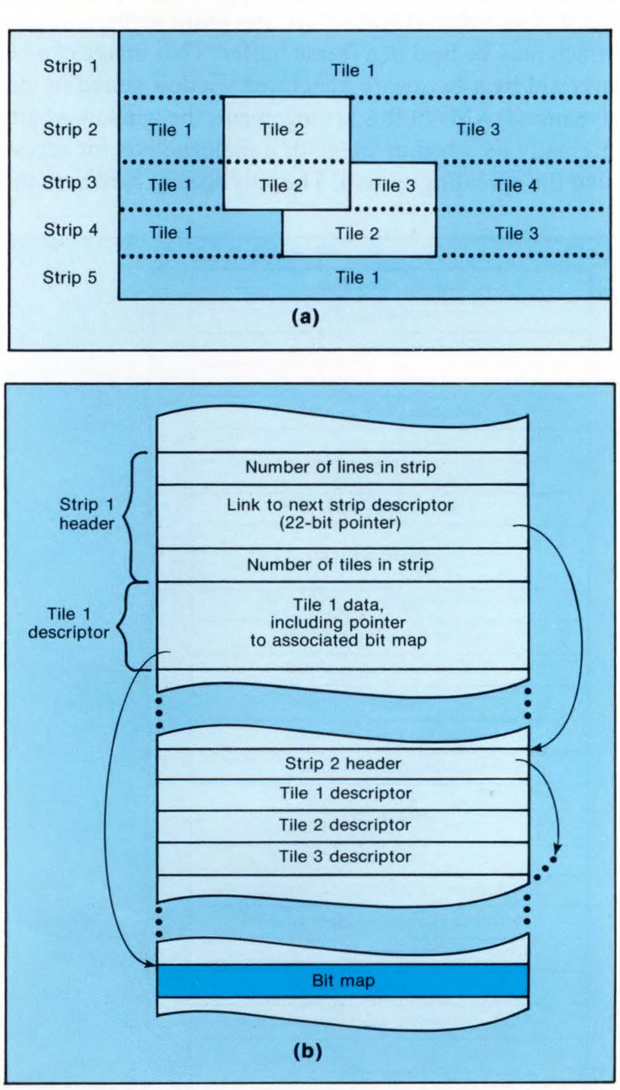
The CPU programs the chip's graphics and display sections through a 128-byte block of control registers (Fig. 3). A relocation register in the bus interface unit allows control registers to be mapped anywhere in a memory or I/O address space. The address of each register is relative to a base address in the relocation register.

The coprocessor's subsystems issue a 22-bit address to access 4 Mbytes of linear memory, which consists of the external system memory and the dedicated graphics memory. Typically, the graphics memory contains display data, character fonts, and programmed instructions for the processor sections. Also within it, bit maps can extend up to 32,000 pixels on a side. Each map has its own set of coordinates, with the upper lefthand corner defined as the origin.

Again, the bit maps can have different numbers of bits per pixel, a memory and bandwidth-saving feature. In one bit map, up to 8 bits can define each pixel of a multicolored figure; in another map, a single bit can represent each pixel of text. In all cases, however, each 16-bit word packs as many pixels as possible. Thus a bit map exists as a series of lines in the graphics memory. In contrast, other chips require a separate memory plane for each bit in a pixel, a wasteful approach that also tends to complicate the access scheme.

Standard dynamic RAM—as opposed to more expensive video RAM—makes a suitable memory building block, since the coprocessor can take advantage of the fast ripple mode to fetch and display data at up to 40 Mbytes/s. The display processor section has a maximum bandwidth of 20 MHz; hence, if the coprocessor makes 16-bit block transfers from the graphics memory, its throughput could reach 320 Mbits/s. In practice, however, the specific memory bandwidth depends on the display size and the operating mode.

In any case, the display processor uses block transfers to alleviate the load that refreshing the screen places on the memory bus, which other devices may be sharing. The

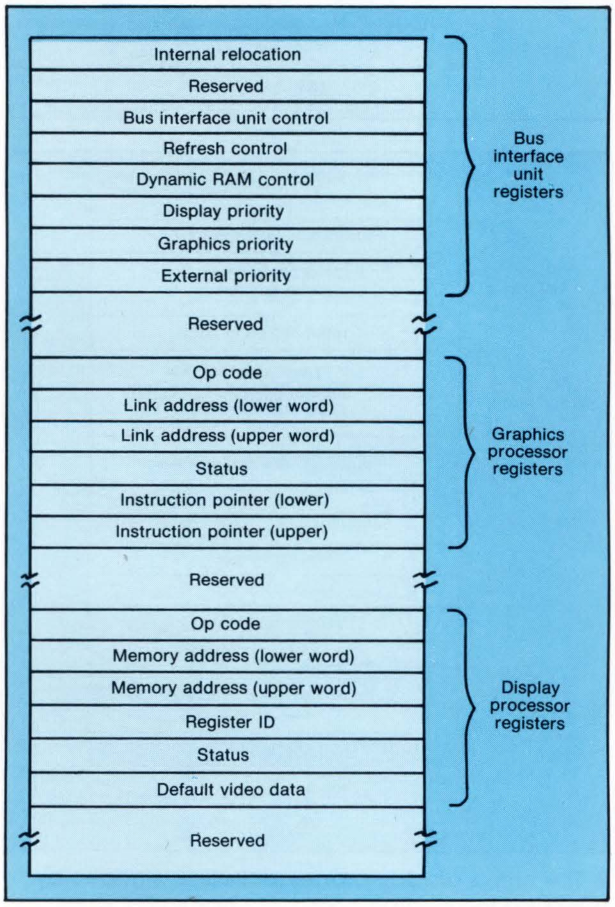


2. The chip's display processor builds windows by breaking the display frame into horizontal strips, each composed of "tiles" that correspond to separate window segments (a). A table in the graphics memory stores the tile descriptors under header information that tells the display processor where to find successive strips (b).

worst case is when 8-bit pixels are displayed at 25 MHz, the rate at which refreshing accounts for 50% of the memory bandwidth. Alternatively, the display processor can control video RAMs, passing data directly from the memory to the display. With that scheme, the processor consumes only 1% of the memory bandwidth.

MARRYING MEMORIES

Powerful though they may be alone, video RAMs and standard dynamic RAMs can combine for a high-resolution, windowed display that entails low bus overhead. The video RAMs store the main screen image, which may be held in a frame buffer. That image can be overlaid by a hardware-generated window stored in the dynamic RAM. In this arrangement, the window would normally be a pop-up menu or a dialogue box for accessing the operating system. The only special hardware involved is simply multiplexer logic to combine the data streams from the video RAM and the coprocessor.



3. A system CPU programs the graphics coprocessor through a block of 128 registers. Although the registers are physically dispersed throughout the coprocessor, they are addressed as a continuous block in an I/O or memory space.

Price and availability

The introductory price of the 82786 graphics coprocessor chip is $81.25 in quantities of 10,000. Samples are available now. CIRCLE 502

Besides the bit maps, the chip's graphics memory stores linked lists of graphics instructions and parameters that are programmed by the user. Typically, high-level software instructs the CPU to write the commands into memory for the graphics processor to execute. The commands are similar to those used with ANSI's Computer Graphics Interface (CGI), as they give programmers complete control of the bit maps' contents. For example, geometric commands can draw points, circles, polygons, and arcs in a variety of sizes. In addition, two commands transfer data blocks within a bit map or between two bit maps. One of the commands, BitBLT, transfers blocks of bits at 24 Mbits/s; the other, ChaBLT, transfers 25,000 characters/s. Executing those commands, the graphics processor manipulates windows 30 to 50 times faster than a CPU could.

Additional sets of instructions specify color and other display attributes; define a pixel-plane mask, which restricts graphics operations to only a subset of bits in a pixel; or establish logic operations that combine existing pixels with newly drawn ones. In addition, programmers can define a clipping rectangle, which limits pixels to a specified area. The rectangle can extend to a small region within a bit map or meet the overall boundaries of a bit map. In a special picking mode, the clipping rectangle accommodates a pointing device like a mouse or a puck.

BEHIND THE SCENES

Supplementing the drawing instructions are non-drawing instructions that control command fetches from memory. Link, for example, executes an unconditional jump to another command in the block; Enter Macro calls a subroutine; and Exit Macro returns from a subroutine.

Many graphics chips require a FIFO buffer, which prevents them from accepting commands in anything but a piecemeal fashion. The coprocessor, on the other hand, takes in a whole block of commands at one time from the CPU. Moreover, it can accept new commands while it executes others. Typically, the CPU builds up a block of sequential instructions in memory; the graphics processor then fetches and executes them.

The graphics processor instructions conform to a simple format: an 8-bit op code, an end-of-list flag, and a pa-

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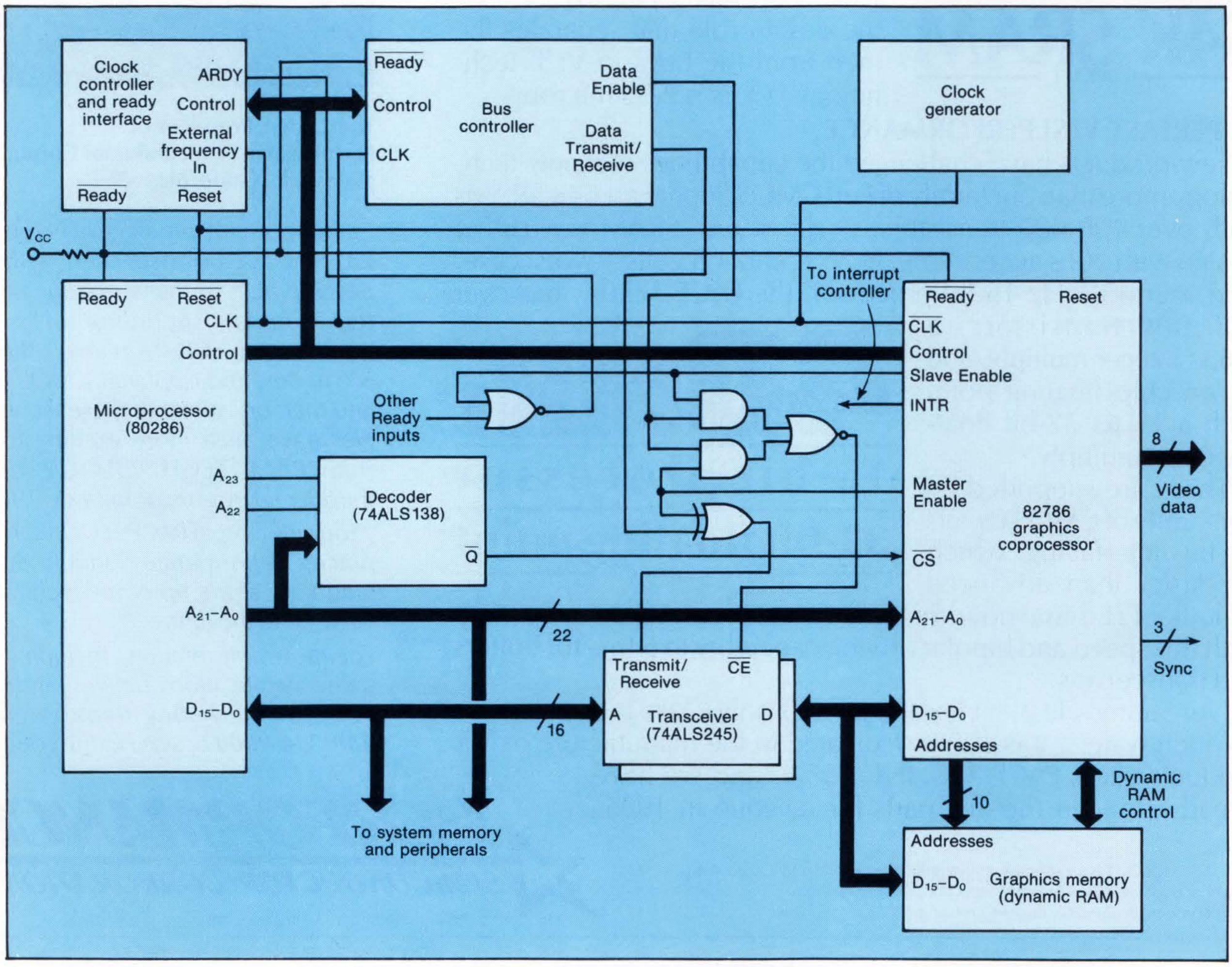
rameter list. After fetching each instruction, the processor checks to see if the end-of-list flag is set. If it is, the processor does not execute the instruction. Instead, it polls its internal registers and waits for the CPU to reset the flag, a signal to continue.

Like the graphics processor, the display processor has its own commands. They load and dump its 40 separate 16-bit registers individually or as a block. The registers specify various display modes, including cursor style and position, background and border colors, and zoom factor. One register pair holds the 22-bit address of the current window descriptor, and other registers directly control the CRT interface logic, selecting frame size, video interlacing, video speed, and other parameters. They program all of the CRT signals needed to display as many as 256 colors at rates of up to 25 MHz.

In addition, the display processor's memory-mapped registers let the CPU, say, examine a coprocessor status register or define the data appearing on the video-output pins during blanking intervals. The second capability can be used to load an external color palette quickly and without the need for an additional address path.

The display processor executes its commands during vertical blanking. Consequently, parameters are updated between frames, yielding clean and flicker-free images. In addition, the processor can be programmed to issue an in-



4. To get high-quality graphics, the coprocessor chip and standard dynamic RAMs can be added to an 80286-based system. The graphics portion displays 640-by-480-by-8-pixel images and executes VDI commands, yet it does not burden the CPU, which can thus run a multitasking operating system. Moreover, very little glue logic is needed to connect the CPU to the coprocessor.

terrupt after a specified number of frames. Thus frame-oriented features like scrolling, panning, and animation can be easily implemented, and windows manipulated almost instantaneously.

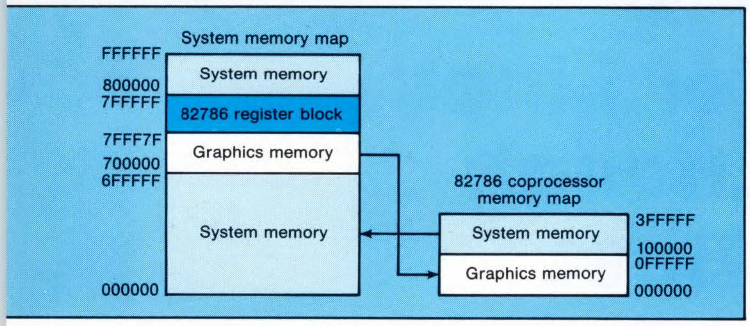
LIKE-MINDED PARTNER

Similar to the graphics processor, the display processor checks for an end-of-command flag and executes instructions only when the bit is reset. After executing an instruction, the display processor sets the bit, letting the CPU know that it can now load a new instruction. Thus, a simple handshaking mechanism ensures enough time to execute each command before the CPU issues another one.

An external 25-MHz clock generally drives the display circuitry, yet several accelerated modes trade off the number of bits in a pixel for the dot-drawing rate. For example, instead of pumping out 8-bit pixels at a 25-MHz dot rate, the coprocessor—once fitted with an 8-bit shift register and a divider—can maximize resolution by sending out 1-bit pixels at 200 MHz.

The coprocessor chip and standard dynamic RAMs can form the nucleus of a graphics subsystem in an 80286-based personal computer or professional workstation (Fig. 4). The system features a display of 640 by 480 by 8 bits, runs a multitasking operating system, and is compatible with the VDI standard.

The graphics processor updates bit maps for the different tasks, but the display processor presents only the ones of interest to the user. For example, a spreadsheet can appear on screen while the coprocessor updates graphics for electronic mail in the background; the latter is shown only on request. Changing windows takes only as long as switching frames, as the image is already in the upper part of the system memory (Fig. 5). The microprocessor need not intervene.



5. Bringing a background window into the foreground takes only as long as the time needed to switch frames. Rather than having to transfer blocks of data to create a new window, the coprocessor creates it in the upper part of system memory and then accesses it as needed for display. Similarly, the CPU can access the graphics memory through the coprocessor.

Because the coprocessor is optimized for the 80286, interface logic is minimal. Whatever logic the processor and the coprocessor do need is shared by the rest of the system. Data transceivers give the CPU access to the coprocessor chip and its memory or give the coprocessor access to system memory.

The graphics memory can also be mapped into the system's static RAM by adding address-decoding logic. The data transceivers then take on an extra function: They isolate accesses to the system and graphics memories. In this way, the CPU and the coprocessor can reach into their respective portions of memory simultaneously. At the same time, with the coprocessor in the slave mode and its bus free, the CPU can access the graphics memory. Read operations would then incur three wait states; write operations, two. If fast dynamic RAMs are used instead, the circuit modifications will reduce the number of wait states to two, regardless of the operation.

The coprocessor can also be used with IBM monochrome and color interfaces. In this case, the designer can set a special bit and thereby put a particular window into the IBM personal computer format. The least significant byte of a word appears to the left of the most significant byte; normally the least significant byte is on the right. The coprocessor also accommodates the two- and four-bank bit maps found in the IBM PC. Thus IBM-compatible application programs can display graphics alongside bit-mapped images created by the coprocessor.□

Martin Randall is a design manager for Intel's next-generation graphics products group. He served as a principal architect and design engineer for the 82786 graphic coprocessor. He has a BSc (EE) from the University of Southampton in England.

Arun Johary is an application engineer for the graphics components group at Intel. He has a BSEE from the Indian Institute of Technology in Bombay and an MSEE from the University of Southern California in Los Angeles.

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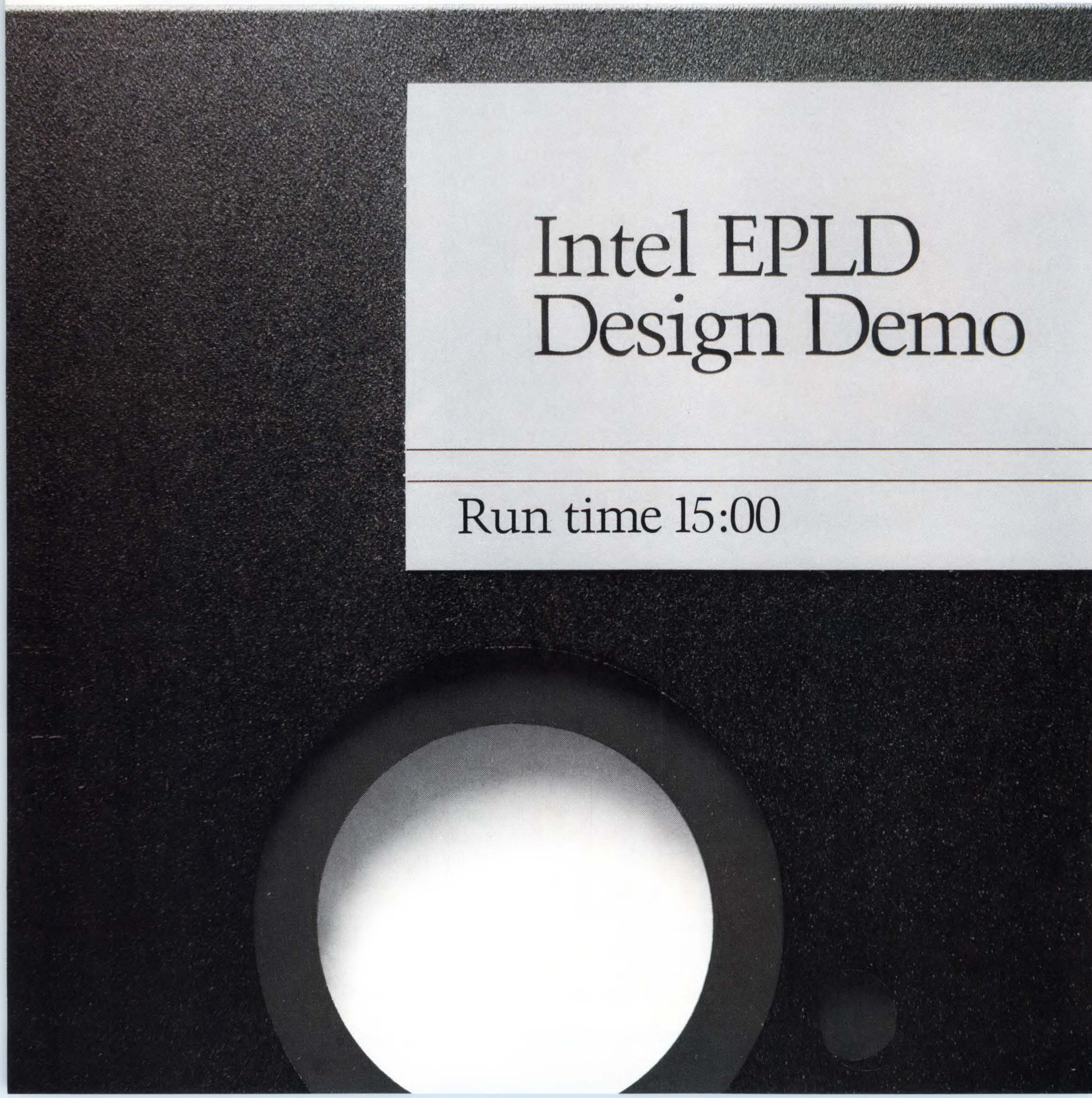

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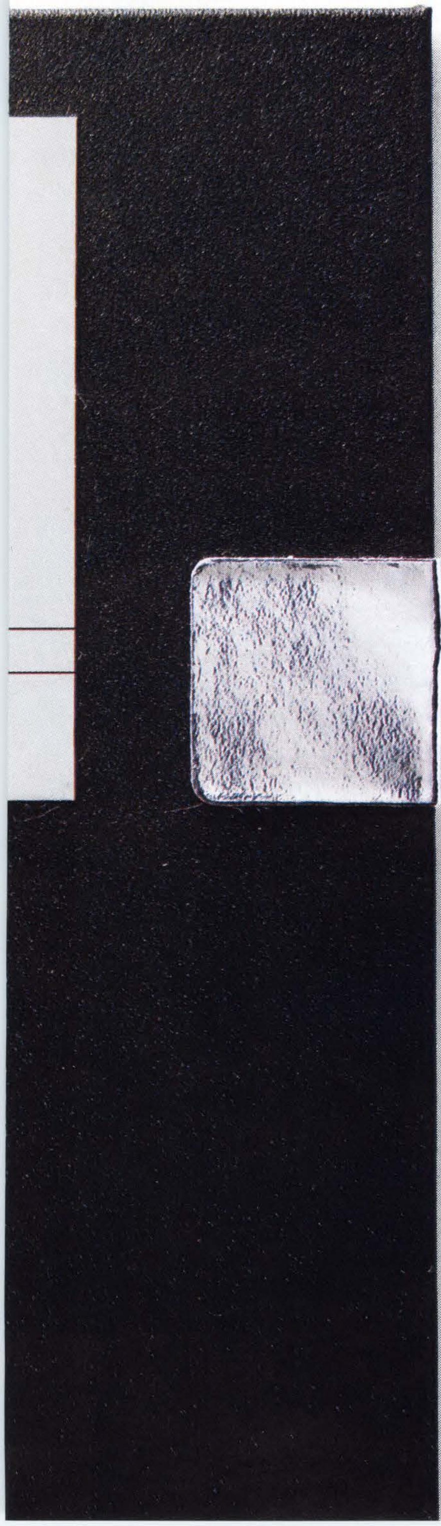

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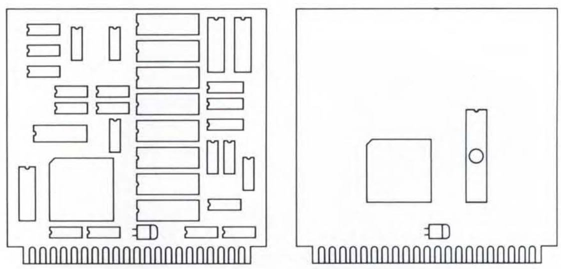

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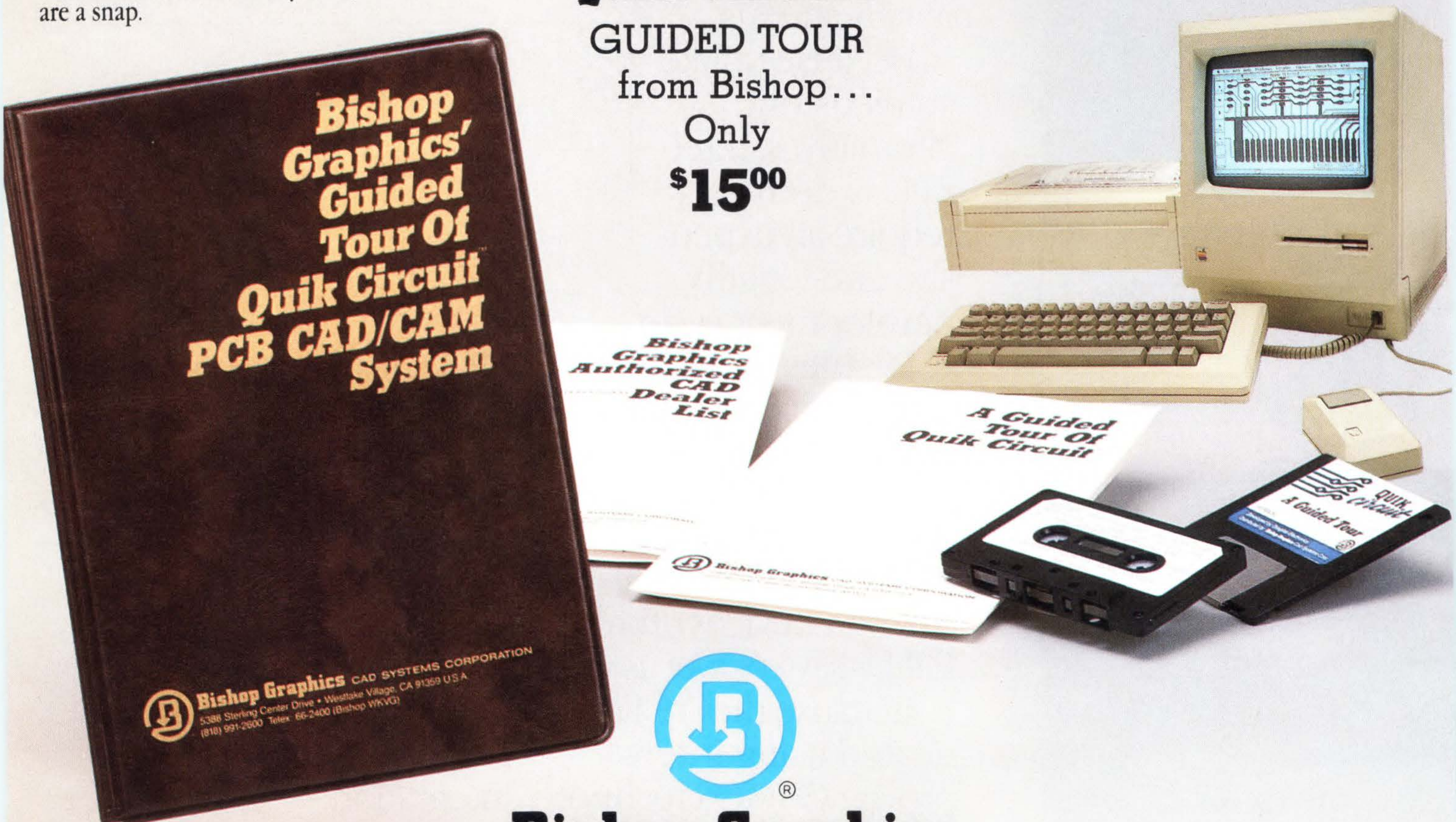

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CIRCLE 86

ELECTRONIC DESIGN EXCLUSIVE

Versatile bipolar master chip lets analog designers reap the benefits of LSI circuits

Exploiting a process similar to the one used to attain LSI levels in digital chips, designers can transform a host of separate analog components into a distinct circuit, making true analog ICs.

John S. Shier and
Richard E. Hester
VTC Inc., Microcircuits Division
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With the rapidly shrinking size of many systems today, the power and space required for analog components wreak havoc in the design. Since most systems still need many SSI-type chips, which quickly fill up a pc board, the designer must find a way to bring the benefits of large scale integration to analog systems. One approach is to create master LSI analog chips with uncommitted IC elements, enabling the user to generate custom circuitry with metal masks. Until now, however, the low-density processes that prevailed could pack only a few dozen transistors on a typical chip.

The VJ800 master chip answers the challenge of achieving high levels of analog circuit integration. The result—an LSI chip not only of moderate size, but also holding 1360 components. That component set is larger, by severalfold, than that of any previous bipolar analog master chip. It is not possible to use all of those components because of the routing restrictions arising from the chip's LSI nature. In practice, utilization of up to about 60% is possible.

To develop the VJ800 (Fig. 1), several conventional processes for making master chips were modernized: First, a dense bipolar LSI process was adopted, albeit at the expense of lower maximum supply voltages. Then a process step was added that accommodates large numbers of high-valued resistors, thus creating less power dissipation. Next, two levels of metal interconnections were used, solving the problems that occur when large amounts of circuitry are placed on a chip. Finally, Schottky diodes were added to the component set.

By paying careful attention to processing detail, packing density can be improved without compromising the excellent device-matching and low-noise characteristics of earlier analog bipolar processes.

The master chip's high component count (see the table, p. 173) permits three amplifiers, a fast differentiator, a comparator, two dc voltage generators, and very fast validation logic to be integrated on one chip. With the high performance level of the available components, the chip operates with data rates of at least 10 Mbits/s.

The amplifiers, differentiator, and comparator are located at the low-noise end of the chip; the validation logic is in the center; and the voltage reference and driver circuitry occupy the lower portion of the chip, where the large-geometry transistors are located. This arrangement holds down thermal interaction by keeping sensitive low-level circuitry away from high-power circuits.

Conceptual design errors and changes in specifications are fairly common in analog design. The master chip, though, permits rapid turnaround of chip revisions, since in many cases only a single mask layer needs to be altered. It provides a cost-effective method of implementing variations needed for several systems.

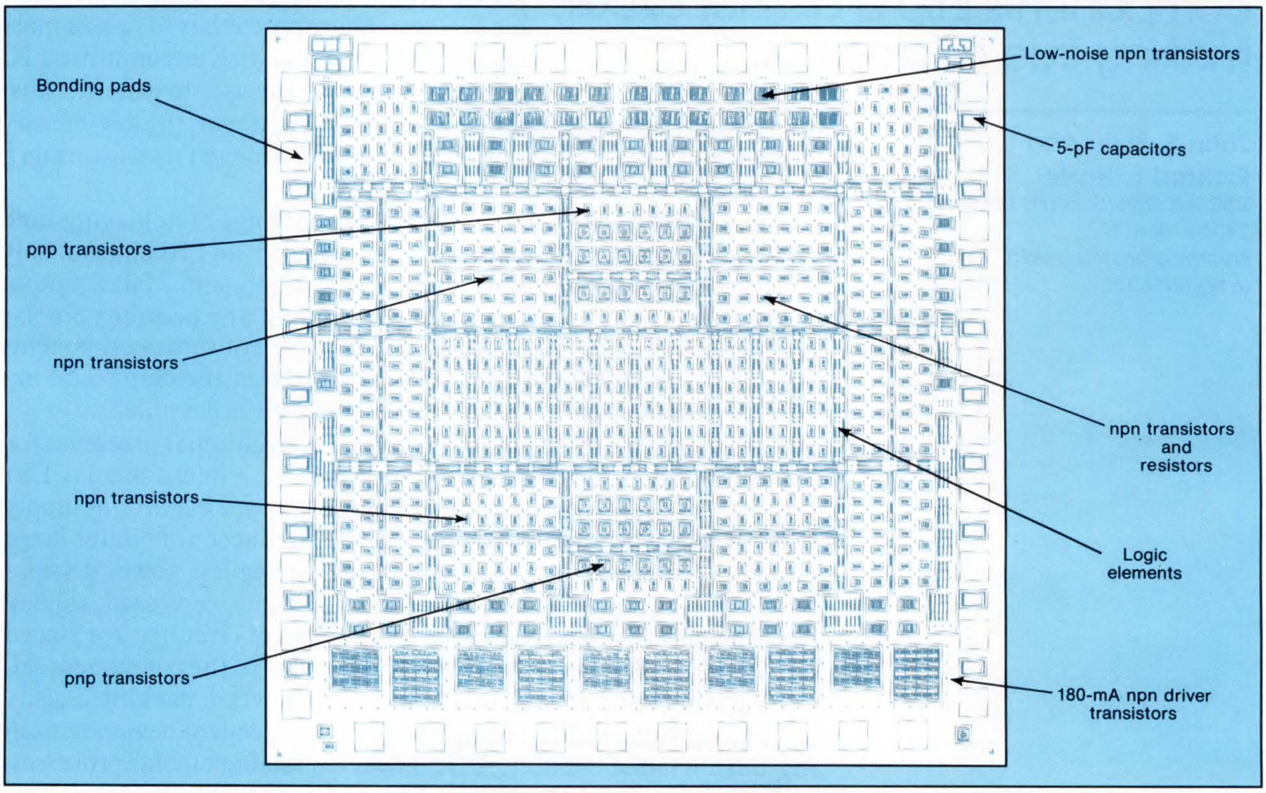
THE LSI PAYOFF

Shrinking the circuit elements yielded the usual LSI benefits. For example, the parasitic capacitance of a small npn transistor under normal bias conditions is now only about 0.2 pF, the same as the typical parasitic capacitance of resistors. Overall, the inherent frequency response of the chip's transistors was improved using shallow junctions in a bipolar structure. Even the lateral pnp transistor has an 80-MHz unity-gain frequency.

Amplifiers with bandwidths in excess of 200 MHz can be created with the master chip. Above 25 MHz, though, performance can be hindered by package parasitics and the limited frequency response of off-chip discrete parts, rather than the inherent speed of active devices on the chip.

Since less current is needed to achieve acceptable circuit performance, the total power consumption of a large, complex chip can be held within reasonable limits. Typical on-chip bias currents are 0.1 to 1 mA. And because of the large total resistance available on the master chip (more than 2 MΩ), it is practical to use many components without worrying about excessive power dissipation.

Most improved high-density IC processes involve some sacrifice of high-voltage capability; the master chip is no exception. It can be used for circuits with a nominal value up to 12 V between the most positive and most negative supply pin. Although that voltage is too low for some ap-



1. Using a dense bipolar process, the VJ800 master chip contains transistors, resistors, and capacitors that, using two levels of metal interconnections, form an analog circuit. Because of the chip's bilateral symmetry, designers can create identical duals of a given circuit.

plications, the steady drop in standard system supply voltages makes it acceptable in many new designs.

Most analog designers have some expertise in designing with discrete components. The master chip, with its small number of standardized circuit elements, allows this expertise to be transferred to chip design. Breadboarding is done not by hardware but with the widely used Spice circuit simulation program. With this tool, the designer can see the waveforms in response to various inputs and make cut-and-try improvements to achieve satisfactory results.

SIMPLIFYING SIMULATION

For designers having access to the popular Mentor CAD workstation software, the simulation task is greatly simplified. One Mentor source diskette contains model data files for all of the master chip's components. With this software, the designer can construct a circuit on a screen using standard symbols for the circuit elements. As this is done, the Spice input file is automatically constructed. Updates and changes are automatically entered in both the circuit schematic and the Spice file so that the finished design is easily and accurately documented.

Implementations of circuits using the master chip are also supported on an IBM PC using Computervision software. Spice models can be supplied to any user who has that simulation program on his computer, but without the schematic capture and other features of the CAD software.

PICK A VALUE

The master chip has the ability to custom-tailor the p^+ resistor values and ratios by placement of resistor contact windows. The user is not required to restrict the design to a limited set of resistor values, since hundreds of values and ratios are available.

A special demonstrator chip, the VJ801, shows off the master chip's power and flexibility. For instance, it contains a standard 733 video amplifier with a voltage gain of 10 and a bandwidth that extends beyond 200 MHz. Peaking, probably arising from package parasitics, occurs at about 50 MHz. The frequency response is flat within 5 dB from 100 kHz to 20 MHz (Fig. 2). The demonstrator IC also boasts a bandgap voltage reference and a 4-bit current-mode logic (CML) binary counter with I/O buffers to TTL levels.

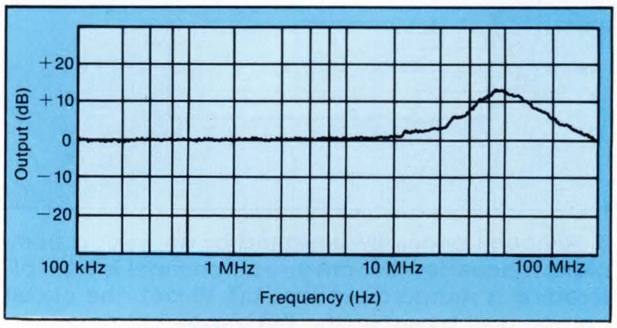
Natural partitioning of the circuitry in an analog application may include logic as well, especially when a large amount of circuitry is to be packed onto one master chip. Using CML, a central section of the chip was designed to accommodate about 60 logic gates. The logic's low switching noise avoids crosstalk with low-level analog circuits. CML is also fast, with propagation delays of only 2 ns, and can be buffered at inputs and outputs to interface with either TTL or ECL levels (or some of both on the same chip).

In custom chips for low-noise applications, the input transistors are usually designed for low base resistance. Specifically, the analog master chip contains 26 special low-noise npn transistors with base resistance of only a few ohms. Even lower base resistances can be achieved by arranging several transistors in parallel. Amplifiers built with the master chip can hold broadband input noise to less than 1 $nV/Hz^{1/2}$, with input offset voltage of approximately 1 mV, without trimming. The 1/f noise of the device's components is comparable to that of other bipolar processes and can give noise corners in the range of 20 to 50 Hz, depending on the design of the amplifier.

Analog designs commonly need high-power outputs. The master chip answers the call with 10 high-current

The VJ800 component set

Number of components	Component description
590	Small-signal npn transistors of various sizes, including Schottky transistors (typical f_T = 1 GHz)
10	180-mA high-current npn transistors, including 5 that are Schottky clamped (typical f_T = 1 GHz)
36	Double-collector lateral pnp transistors (typical f_T = 80 MHz)
74	300-Ω, p^+ resistors
153	600-Ω, p^+ resistors
112	1200-Ω, p^+ resistors
293	3200-Ω, p^- (implanted) resistors
74	1500-Ω, p^- (implanted) resistors
18	Junction capacitors (nominal 5 pF at zero bias)
40	I/O pads

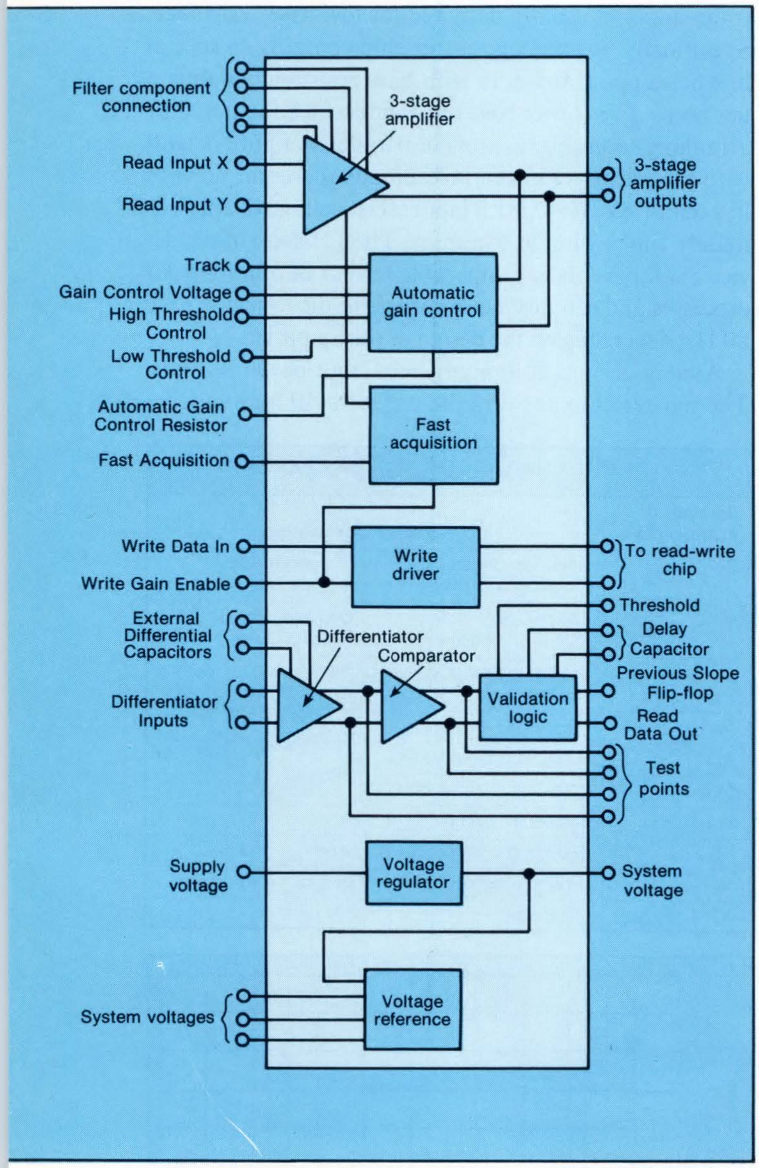


2. A 733-type video amplifier, with a bandwidth extending beyond 200 MHz, can be built using the VJ800 master chip. A frequency response flat within 5 dB from 100 kHz to 20 MHz demonstrates the chip's ability to produce high-quality circuits.

output transistors, each able to operate at collector currents up to 180 mA, with drive arrangements like push-pull and H bridge. In some cases, small motors and relays can be driven directly from the chip, which can also drive magnetic write heads for tape and disk drives. Serious power dissipation problems can occur, however, if too many such outputs are used at full rated current.

With high-current transistors and accurate bandgap voltage references, voltage regulators can be integrated on a chip. That avoids some of the noise pickup problems arising when the supply-to-chip lead on the board is capacitively or inductively coupled to nearby signal leads. The high-current transistors in the master chip also can be used to drive 50-Ω transmission lines (or 25-Ω double-terminated lines) with large signal amplitudes. The chip's ability to drive lines in combination with low-noise amplifier transistors makes it ideal for telecommunications.

In processing analog signals, characteristics such as amplitude, distortion, noise, and output level can be subtly different from one system design to another, even though the overall system function is the same. This is true, for example, in hard-disk and tape drives, where differences in heads, media, and other characteristics from different manufacturers must often be considered.



3. Although originally designed as an ASIC, a complete Winchester disk-drive read channel is now offered as a standard product, the VM542. The circuit can be built by exploiting the master chip's complement of both analog and digital components.

STANDARD PRODUCTS

The same features that make the analog master chip attractive for ASIC designs also apply in creating standard products. The chip's flexibility, for instance, lets designers create standard LSI chips for prototyping. They can then be modified quickly and at low risk to meet the needs of individual customers.

A complete Winchester drive read channel, integrated on a master chip, demonstrates what can be accomplished (Fig. 3). Originally designed as an ASIC, it is now offered as a standard product, the VM542. Several advantages of a large master chip are apparent in the read channel's design. For one, integrating considerable amounts of logic on the chip permits the use of complex validation logic, which in turn produces lower error rates. Conventional implementations of the read-channel circuit often require 5 to 10 IC packages and dozens of discrete elements. Using this LSI chip greatly reduces the parts count and board area.

The VM542 read-write channel can be used in disk drives to provide complete analog processing of readout signals from the disk. It contains a three-stage amplifier with automatic gain control and a filter for equalization, a differentiator, a fast-rise comparator, and sophisticated pulse validation logic. This circuitry delivers complete detection, digitizing, and qualification of both modified FM and run-length-limited (RLL) encoded data. It can also be used for serial data transmissions such as telecommunications.

Peak detection is accomplished by an automatic gain control with adjustable threshold levels, a differentiator,

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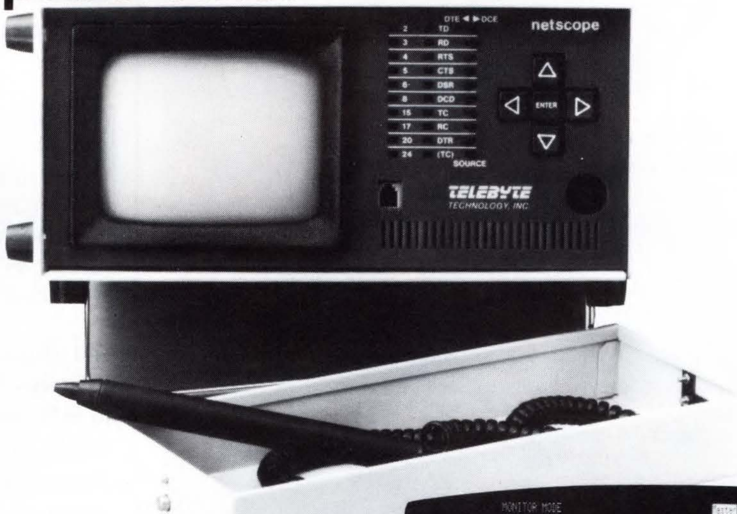

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NETSCOPE is a compact, highly versatile data line monitor, emulator and tester for RS-232 data communications circuits and devices such as terminals and printers. The NETSCOPE uses a 5" CRT display and a cursor pad for use with a series of easy-to-use set-up and input menus. An optional light pen is available as an alternate input device for use with the "soft" keyboard which appears on the CRT.

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The NETSCOPE is designed to be connected between DCE and DTE devices, but can also be used in a "T" connection if desired. Front panel switches make this, and the in-line hookup a simple process. There are two DB-25's mounted on the rear of the unit for these connections.

Reliability is keynote in the NETSCOPE design resulting in a package that is rugged, and has a reduced number of cables and connections while not sacrificing any performance.

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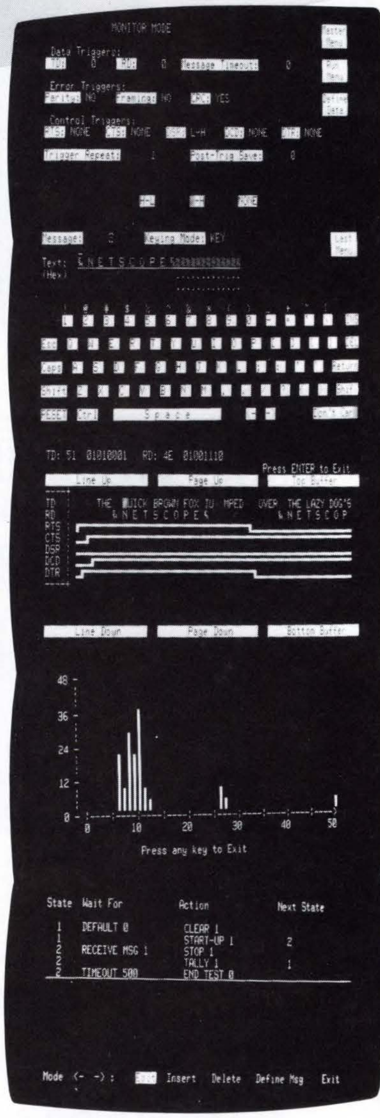

Monitor mode provides a selection of triggers for messages, errors or control lines.

Messages are entered via a "soft keyboard." The photo illustrates a message beginning with a Start-Of-Header character.

Data for both TD and RD along with the EIA control lead transitions is presented to the user in a graphical format.

Statistical data gathered and presented on a histogram chart.

State programming based on mathematical flow-charts. The states in such a diagram are specified conditions that, when met, require certain actions.

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CIRCLE 87

DESIGN ENTRY

Analog master chip

Price and availability

The nonrecurring engineering cost of the basic VJ800 is $15,000, with a lead time of 8 weeks for 15 samples. In quantities of 10,000, plastic DIPs with 24 pins are priced at $4.35. CIRCLE 504

and a fast-rise comparator that converts the peaks to zero crossings. The validation logic changes the zero crossings to valid signal pulses by checking pulse amplitude, pulse width, and previous-slope polarity. The VM542's output is a stream of TTL-compatible data pulses that correspond to valid flux reversals on the disk.

The chip operates from +5 and +12 V and ground or from +5 and +10 V and ground, and it has 40 I/O pins. The read-write channel implementation chip uses approximately 52% of the available components, ensuring that the overall chip dissipation will not be exceeded.

With this chip, most of the layout methods that have proven their worth in analog design can be used, such as symmetric layout of matched circuit elements and quads of cross-coupled transistors for low input offset voltage, among others. Since the chip has bilateral symmetry, it enables design of identically configured dual circuits.

Because of its LSI structure, the master chip is small by ordinary standards: 126 by 126 mils. Hence, it fits into a variety of SSI and LSI packages such as DIPs, flat packages, and plastic chip carriers with 18 to 40 pins (including small-outline packages with 16 pins or more). Since the chip's high frequency performance makes package parasitic elements a serious concern for designs that use the full bandwidth of the chip's active elements, careful choice of package is important. The device is also available in chip form for use in hybrid IC fabrication, which is the best type of packaging for very high frequencies.□

John S. Shier, strategic marketing manager at VTC, is in charge of planning and defining new bipolar products. He holds a BS in physics from the California Institue of Technology and a PhD in physics from the University of Illinois.

As consulting engineer at VTC, Richard E. Hester is responsible for the design of standard linear signal-processing products. He has a BSEE and an MSEE from the University of Minnesota.

How valuable?	Circle
Highly	547
Moderately	548
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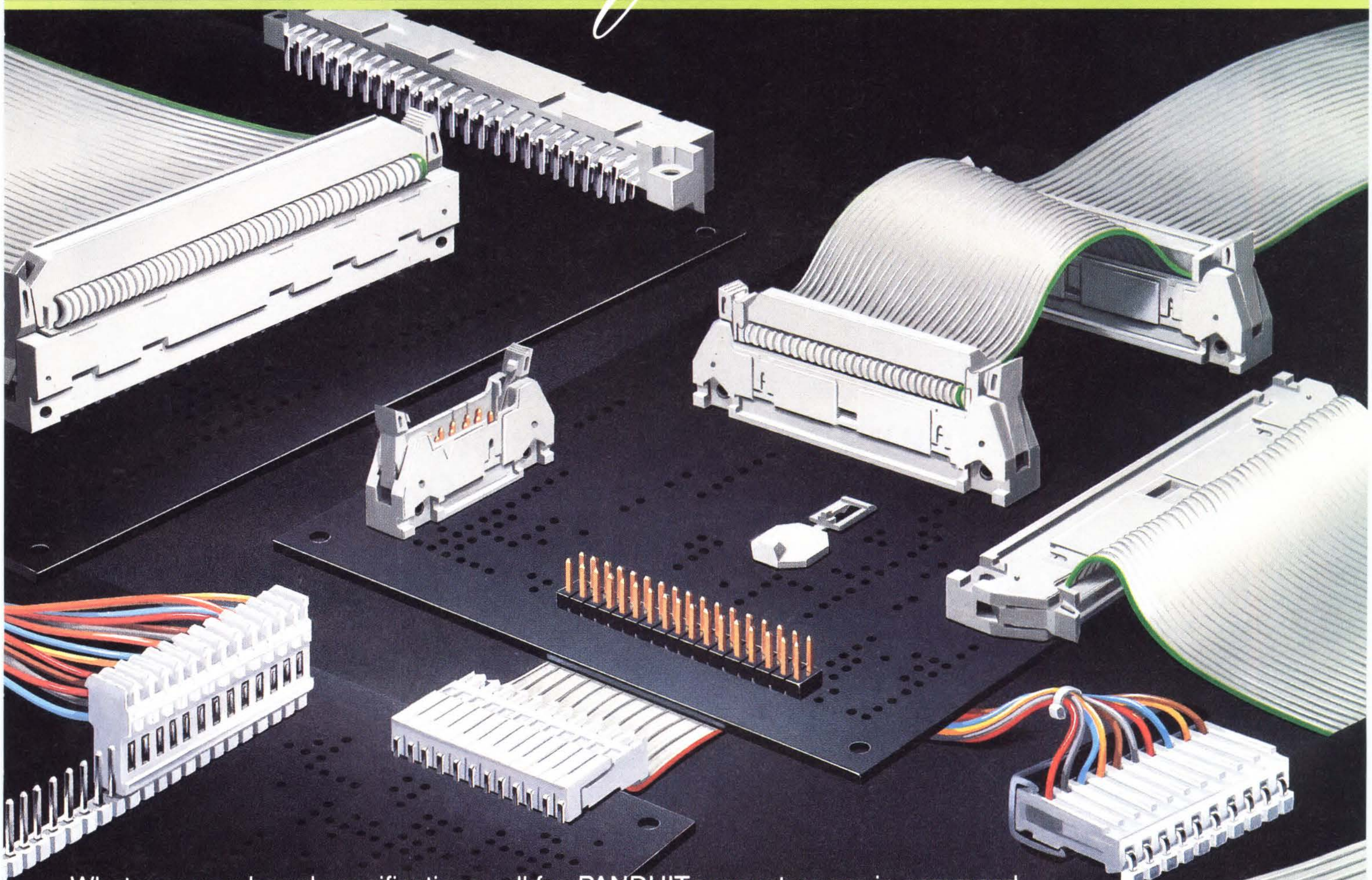

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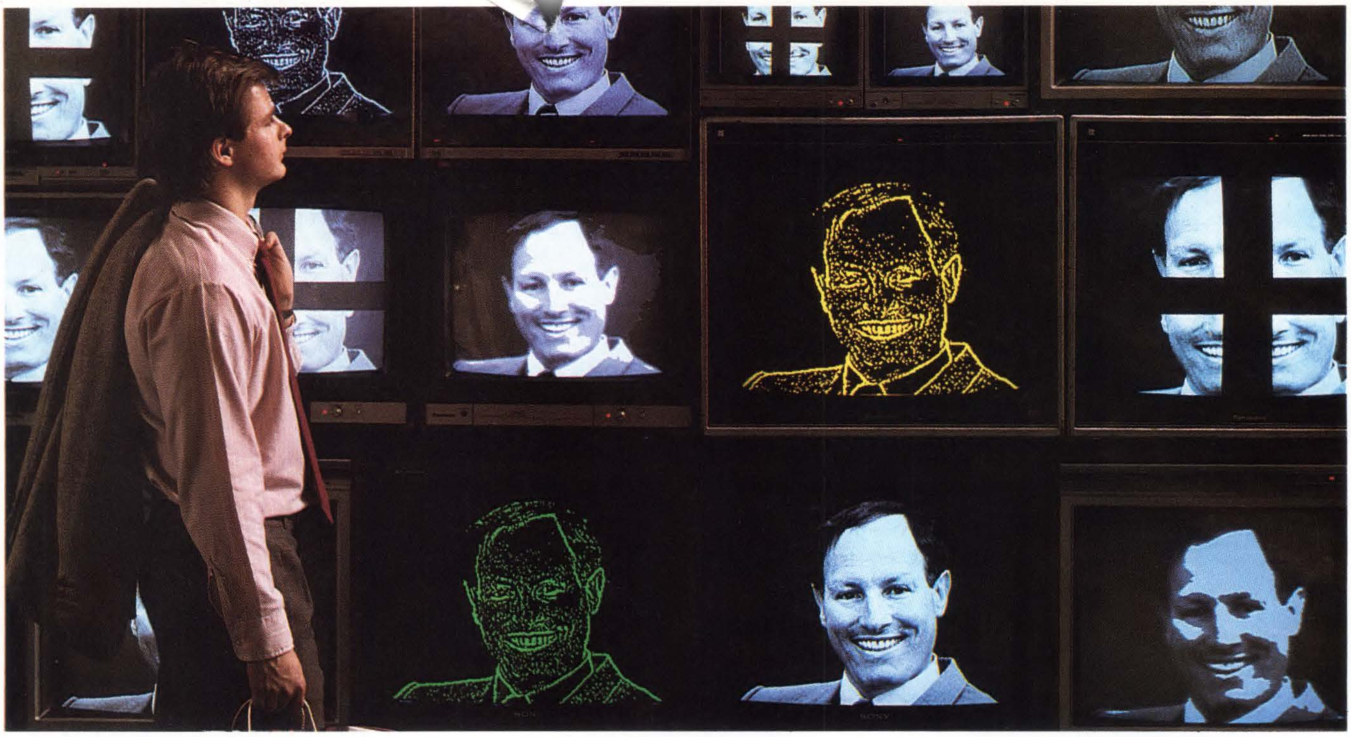

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DT2803 Low Cost Frame Grabber	IBM PC, PC XT, PC AT	256x256	64	Yes	Yes		8*	Yes	Yes	1 buffer 256x256x8 (64 Kbytes)					VIDEOLAB PC SEMPER	$1495
DT2851 + DT2858 High Resolution Frame Grabber and Auxiliary Frame Processor	IBM PC AT	512x512	256			Yes	8*			2 buffers, 512x512x8 each (512 Kbytes), and 1 buffer, 512x512x16 (512 Kbytes)	Yes	Yes	Yes	Yes	DT-IRIS	DT2851 $2995 DT2858 $1495
DT2603 Low Cost Frame Grabber	MicroVAX II	256x256	64	▼	▼		4	▼	▼	1 buffer 256x256x8 (64 Kbytes)					Coming Soon	$1895

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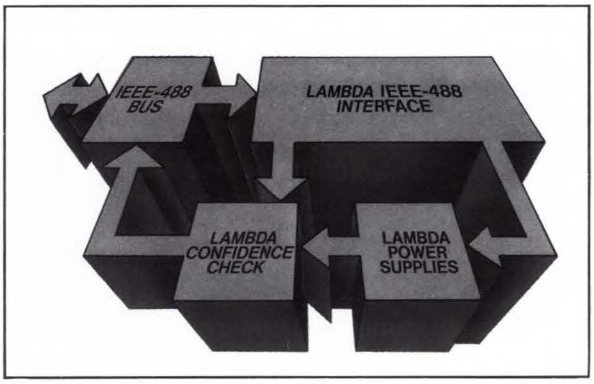


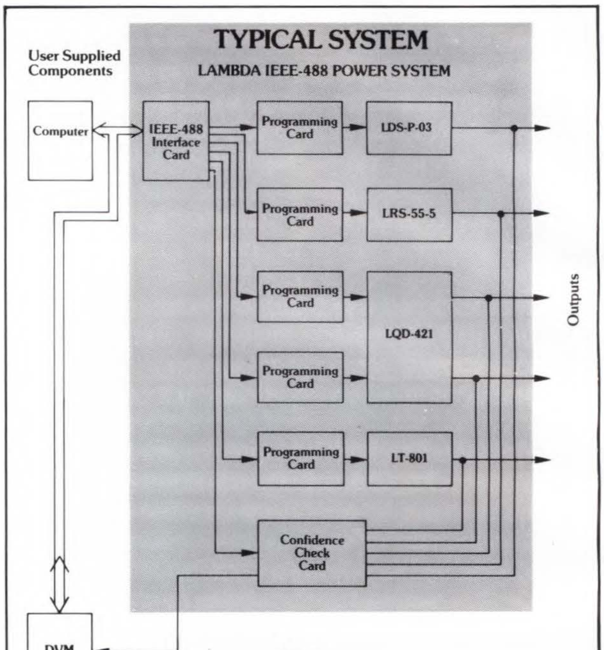


Figure 1

SYSTEM DESCRIPTION

The Lambda IEEE-488 Power Supply System provides the communication link between a control system (computer) and standard Lambda off-the-shelf power supplies. The bus protocol and timing relationships are as defined by the IEEE-488 standard.

The Lambda system is a modular design that permits maximum user flexibility in configuring a system to your specific needs and costs. Lambda will deliver a complete system fully wired and tested, including all interface wiring, within 6-8 weeks after receipt of order. System elements include Lambda standard power supplies, Lambda standard rack adapter, and the following printed circuit cards:

a. IEEE-488 Interface Card — The IEEE-488 Interface Card is a dedicated microprocessor which performs the tasks of bus communication, instruction decode and secondary address selection. One interface card is required for each primary address and controls both programming cards and the confidence check card. Up to a maximum of six secondary addresses are possible.

b. Programming Cards (one per power supply) — The programming card converts the decoded computer instructions into power supply control voltages for voltage output or current limit setting. It also provides the isolation between the bus and the power supply. All offsets and tolerances in the programmer, as well as the individual power supplies, are compensated for by factory calibration.

c. Confidence Check Card (optional) — The optional confidence check card can be configured within the system to verify that the programmed supply outputs are equal to the programmed values. (This requirement is termed "Confidence Check".) The confidence check card occupies one secondary address and is capable of routing output voltage and/or current by means of relays of up to five supplies to a user furnished digital voltmeter. Either output voltage or load current may be measured. By using an IEEE-488 compatible meter, the user is capable of machine reading the outputs. The outputs are isolated from the meter until the confidence test check is invoked.

The Lambda system features:

1. Standard — pick the system to suit your needs from off-the-shelf modules with a wide range of options.
2. Accommodates both wide range output supplies and narrow range (slot) supplies.
3. Controls Lambda standard lab and modular power supplies.
4. Confidence check — verifies the program requested.
5. One primary address controls six secondary addresses.
6. Simplicity in programming.
7. Manual/Auto mode select switch — for ease of maintenance and system set up.
8. IBM®-PC compatible — The Lambda IEEE-488 Power System and IBM®-PC have been tested with the PC-MATE™, GPIB-PC2, PC-488 and ZT-1488 interface cards.* A sample program is provided in the manual for information purposes only.

*IBM® is a registered trademark of International Business Machine Corporation. PC-MATE™ is a trademark of Techmar Inc. GPIB-PC2 is a product of National Instruments. PC-488 is a product of Capital Equipment Corp. ZT-1488 is a product of Ziatech Corp.

SYSTEM PERFORMANCE

Voltage range and output from zero to the published V_{OUT} maximum of the power supply up to a maximum V_{OUT} of 100 volts on wide range models or V_{OUT} ± 5% on narrow range models (slot supplies).

VOLTAGE REGULATOR MODE

Line Regulation/Load Regulation
Individual power supply specifications apply.

Ripple
RMS — Individual power supply specifications plus 1mV RMS for linear power supplies.
Peak to Peak — Individual power supply specifications + 3mV peak to peak for linear power supplies.

Accuracy of Programming
0.1% of scale

Resolution of Programming
0.1% of scale

Temperature Coefficient
TC of supply + .01%/°C

Overshoot
0.25 Volt maximum at turn on/turn off/recovery from short circuit.

Programming Range
00.00% to 99.99% of V_{OUT} for wide range supplies or −5.00% to +5.00% of V_{OUT} on slot supplies.

Programming Time
Voltage up programming 50 milliseconds typical.

Remote Sensing of Power Supplies
Provisions are made for remote sensing of power supplies.

CURRENT REGULATOR MODE
(not applicable on slot supplies)

Line Regulation/Load Regulation
Individual power supply specifications apply.

Accuracy
2% of programmed value plus 1% of full scale.

Resolution
1% of rated current.

INPUT DATA FORMAT

Communication is conducted in accordance with IEEE-488/1978 standards. All data is transmitted in ASCII format.

The system is capable of a listen only function.

It uses secondary addressing extensively.

The input connector is wired per IEEE-488 specifications. All communication, control and data entry are through this connector.

The following control signals are recognized: ATN, IFC, NRFD, NDAC and DAV. REN is not recognized.

Protection
In addition to all protection circuits inherent to each power supply, protection circuits are added which limit each output voltage to less than 5V in case of programmer failure.

Power on Operation
All outputs are set to zero volts. No overshoot at power on, power off or power failure.

AC Input
105-132 VAC 50/60 Hz
187-242 VAC 50/60 Hz available as an option.
205-265 VAC 50/60 Hz available as an option.

Operating Temperature Range
0 to +60°C

Storage Temperature Range
−55°C to +85°C

CONFIDENCE CHECK SYSTEM

1. A total of five power supplies may be monitored.
2. Only one power supply can be monitored at a time.
3. Only one power supply output function may be monitored at a time, either output voltage or a measure of output current.
4. Location of voltage and current measurements.
   a. Output voltage of power supply at terminals of assembly.
   b. Output current is taken across internal shunt.
5. Accuracy of output voltage measurement.

Measurement meter accuracy plus effect of 50,000 ohm internal source impedance on external meter accuracy.

6. Accuracy of current measurement.

1% plus accuracy of meter plus effect of 50,000 ohm internal source impedance on meter accuracy.

7. Switching Relay voltage insulation.
   a. Voltage rating between contacts = 200 volts.
   b. Voltage rating contact to coil = 1,000 volts.

Power On Operation
All relay contacts open.

AC Input
Same as IEEE-488 adapter card and programmer card.

Operating Temperature Range
0 to +60°C

Storage Temperature Range
−55°C to 85°C

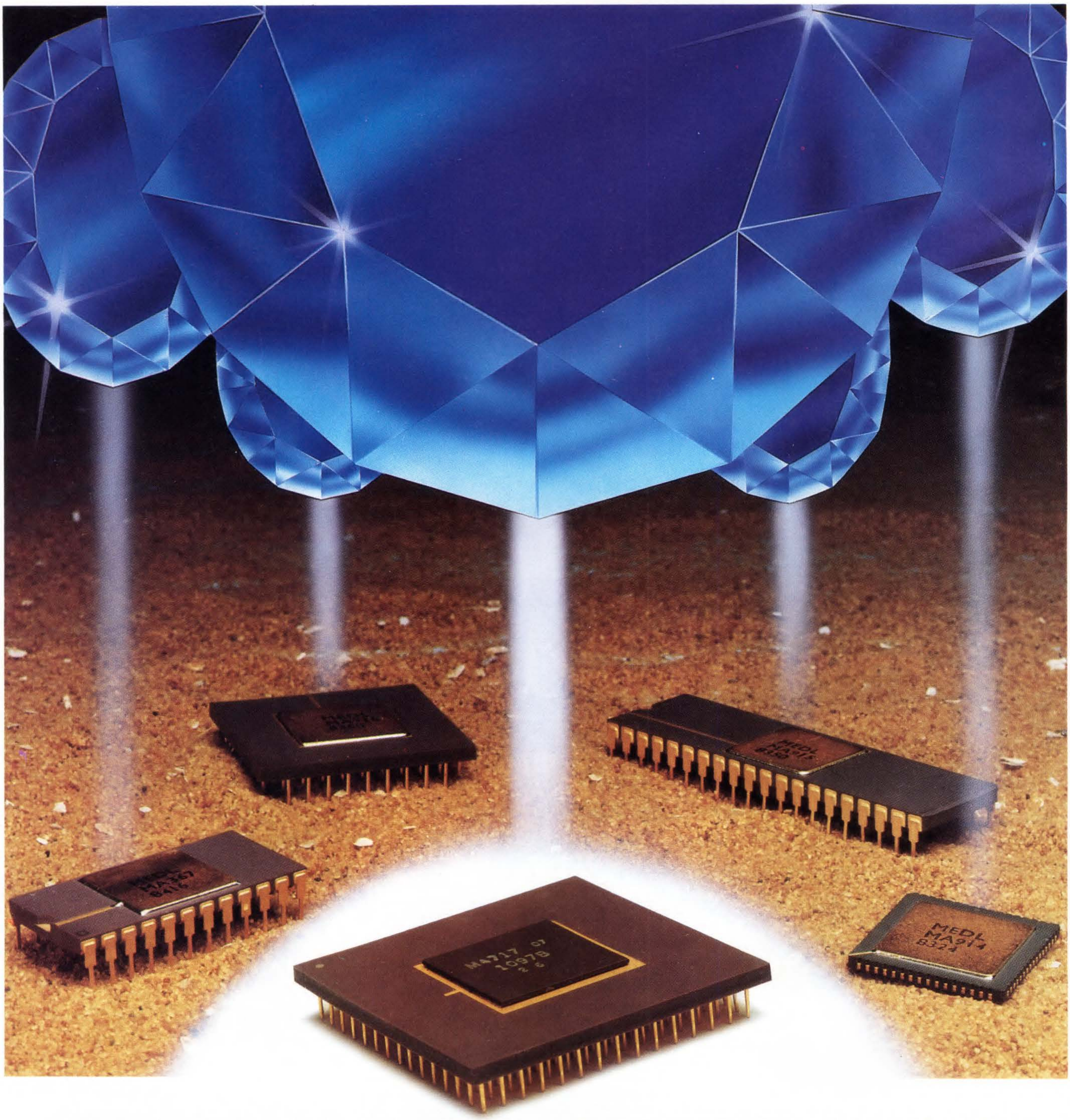
Protection
All relay contacts buffered with 25,000 ohms.

MECHANICAL CONFIGURATION

Two basic configurations are available with modular power supplies.
a. blank front panel with on/off switch, pilot light and fuse.
b. same as above with the addition of front panel voltage adjust pots and test points.

FREE APPLICATION NOTES

Send for your free copy of Lambda's computer programmable IEEE-488 Power System application notes. Call or write Lambda today.



32-bit data-path chip heralds next generation of floating-point tasks

A three-port architecture stresses simplicity, yet packs a multiplier, ALU, 32-word register file, and division circuitry. It keeps the essence of IEEE floating-point math.

Y.W. Sing, John Oxaal, and George Chu
Weitek Corp.
1060 E. Arques Ave.
Sunnyvale, CA 94086
(408) 738-8400

This article completes a three-part series exploring a family of advanced numerical processors. The first installment, which appeared in the April 17 issue (p. 137), described a 32-bit integer processor and a 32-bit sequencer. The second installment appeared May 1 (p. 213) and presented a chip that implements a memory-mapped interface between the 80386 microprocessor and the WTL1164/65 floating point coprocessor.

Floating-point arithmetic has gained the unwavering loyalty of an army of designers, and for good reason. Its intrinsic properties, namely, its dynamic range, high precision, and automatic scaling, make it ideal in applications like graphics, image processing, sonar, radar, and video special effects. First-generation floating-point chips continue to serve systems in which floating-point calculations are absolutely required. However, the high parts count, difficult programming, limited performance, and considerable power dissipation that accompany those chips have precluded their use on a broader scale.

The CMOS WTL3332 floating-point data-path chip eliminates most of the shortcomings by including three 32-bit ports, an IEEE standard 32-bit floating-point multiplier and ALU, a 32-word four-port register file, and a lookup table for division (Fig. 1). The initial version of the chip boasts a 100-ns throughput and a register-to-register latency of 300 ns for addition and multiplication. The chip's pipelined architecture completes triadic instructions—in the form $(A \times B) \pm C = D$—in a single clock cycle with a latency of only three cycles. Using these instructions, the device can implement graphics operations, fast Fourier transforms, and finite-impulse-response filters at an effective rate of 20 million floating-point operations per second (MFLOPS).

Later models of the chip will boast cycle times as fast as 50 ns for 40 MFLOPS. Thus, a simple system employing the IC as the data-path processor would have 25% of the floating-point performance of the Cray 1, a 160-MFLOPS single precision machine. Systems using current versions of the chip can be upgraded to handle

40 MFLOPS. The 100-ns part can perform over 250,000 three-dimensional vectors/s, including transformation, clipping, and perspective division; the 50-ns version will hit over 500,000 vectors/s. By comparison, high-performance graphics terminals deliver only about 100,000 vectors/s and use a huge amount of hardware to do so.

The chip performs equally well in digital signal processing (DSP). For instance, a few components placed on a 5-by-8-in. card (Fig. 2) can implement 1024-point complex FFTs in about 4 ms on the 100-ns model and 2 ms on the 50-ns unit. In such a case, the chip's performance equals that of most $80,000 array processors and is better than half the performance of many $1 million machines.

BENCHMARK EXECUTION

The IC's performance rests not only on a high-speed CMOS process and efficient circuit implementation, but also on its three-port architecture and triadic instructions. The latter two features, combined with the five internal buses and the four-port register file, let the chip execute common benchmarks in close to the theoretical minimum number of cycles (see the table, p. 194).

The WTL3132, a single-port version of the WTL3332, is useful when applications require more than one computation per I/0 transaction. Except for the I/O configuration, the single-port chip has the same features and upward compatibility as the triple-port model.

From 80% to 90% of common graphics DSP and control algorithms—such as finite- and infinite-impulse-response filters, matrix transformations, polynomial expansions, and FFTs—require multiplication and accumulation. In a finite-impulse-response (FIR) filter, for example, each output sample, Y_I, is determined by summing products:

$$Y_I = \sum_{I=1}^{N} C_I (X_{N-I})$$

where I is the sample number, N is the number of filter taps, and C is the filter coefficient.

Executing application programs efficiently, therefore, requires that the multiplication-accumulation instruction be completed in not more than one cycle. This is possible since the chip's multiplier and ALU operate simultaneously. Without the ability to execute a triadic instruction, a single instruction would eat up at least two cycles.

Many numerical-processing algorithms, such as digital filters and large-matrix operations, are too large for the on-chip register file. Consequently, two separate operands per cycle must come from off the chip. Even though the single-port chip and one input port of the triple-port model can handle two I/O transactions per cycle (two operands fed in through a single port in one cycle), such "double pumping" becomes difficult when cycle times approach 50 ns.

The high I/O speed places extreme demands upon the data memory and data address generators. Generally, the costs of meeting those demands are so high that they force designers to increase cycle times, thereby reducing chip performance. For I/O intensive applications the device's three-port architecture prevents an I/O bottleneck. Thus, almost any algorithm can run at maximum speed without undue demands upon the memory system. Data at the input ports can be used directly by the multiplier or ALU in the cycle in which it is loaded into the chip.

The IC is much easier to program than its heavily pipelined predecessors. In addition to having fewer pipeline registers to deal with, the programmer can write an entire instruction on a single line. For example, if he wanted to perform $(A \times B) \pm C = D$, the software need only specify the source for A, B, and C and the destination for D in one microinstruction. Even though storage of D occurs in the third cycle after the start of the instruction, the store is specified in the same instruction as the operation. In addition to making programming easier, this feature allows the chip to be interrupted without destroying a calculation in progress. The programmer must only remember not to attempt to use a result until three cycles after

Looking at things in perspective

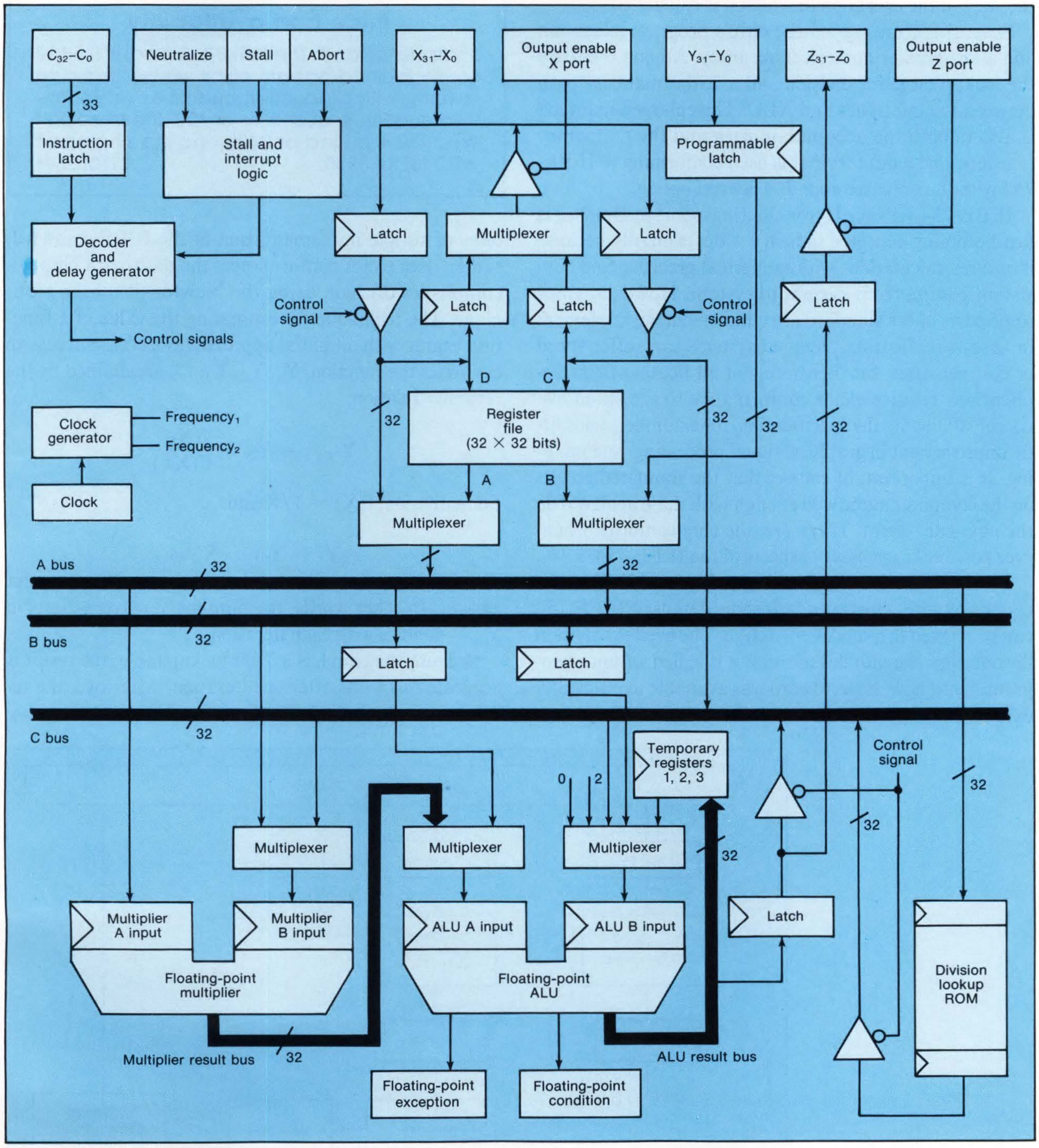
In the cross section of the canonical clip frustum, the Y and Z coordinate axes are orthogonal, while the X axis is perpendicular to the page. The viewpoint is a distance, S, from the screen, which is considered to be at Z = 0. The volume of the viewing space, or the clipping frustum, extends from Z = 0 to Z = W. As the distance from the viewpoint increases, the viewing space diverges in the same way that a human's field of view diverges as distance increases. The problem is to map all points in the viewing space onto the screen.

Consider, for example, the point X_0, Y_0, Z_0. Using similar triangles to find where Y_0 maps onto the screen:

$$\frac{Y_0}{S+Z} = \frac{Y_0'}{S}$$

$$Y_0' = \frac{SY_0}{S+Z} = \frac{Y_0}{1+Z/S} = \frac{Y_0}{W}$$

It is necessary to divide Y_0 by $(1 + Z/S)$, yielding a value known as W, or the perspective value. The W value can be used to map all points in the viewing space onto the screen.



1. The CMOS WTL3332 floating-point chip combines three 32-bit ports (X, Y, and Z), an IEEE standard 32-bit floating-point multiplier, and an ALU. Together with a 32-by-32 four-port register file and a lookup table for division, the chip attains a throughput of 100 ns.

the start of the operation in which it is calculated.

Several features speed the chip's program execution and allow greater numerical accuracy. Among them are the lookup table for division and a 25-bit mantissa path between the multiplier and ALU. The enlarged mantissa is also in both the accumulate path and the temporary registers, and a data format is used conforming to IEEE-754 with the unbiased round to nearest option.

IEEE-754 version 10 for floating-point arithmetic is fast becoming accepted industry wide, primarily because it ensures calculations with numerical precision and consistent results from system to system. However, since some parts of the standard are cumbersome to implement in hardware, floating-point subsystems can suffer speed or cost penalties. Furthermore, not all floating-point applications require exact conformance to the standard. Closely following the specification, for example, yields little improvement in graphics, signal processing, and imaging. It is important, of course, that the simulated results on the computer agree well enough with those achieved on the physical system. Therefore, the chip conforms whenever possible to necessary aspects of the IEEE-754.

Division, which a number of graphics and DSP applications require, illustrates how some details of IEEE-754 can be relaxed in a successful design. The need for division far outstrips the number of times it is called within a program. Until now, no hardware was available to efficiently execute the divide instruction. In keeping with the philosophy of simple implementation of the IEEE standard, rather than exact conformance, the data-path chip accomplishes division using the Newton-Raphson technique. The technique for estimating the value of a function begins with an initial approximation, Y_0. Successive estimates the function, $Y_1, Y_2, Y_3, \ldots$ are defined by the recursive relation:

$$Y_{N+1} = Y_N - \frac{f(X_N)}{f'(X_N)}$$

For a division, $f(X) = 1/X$ and:

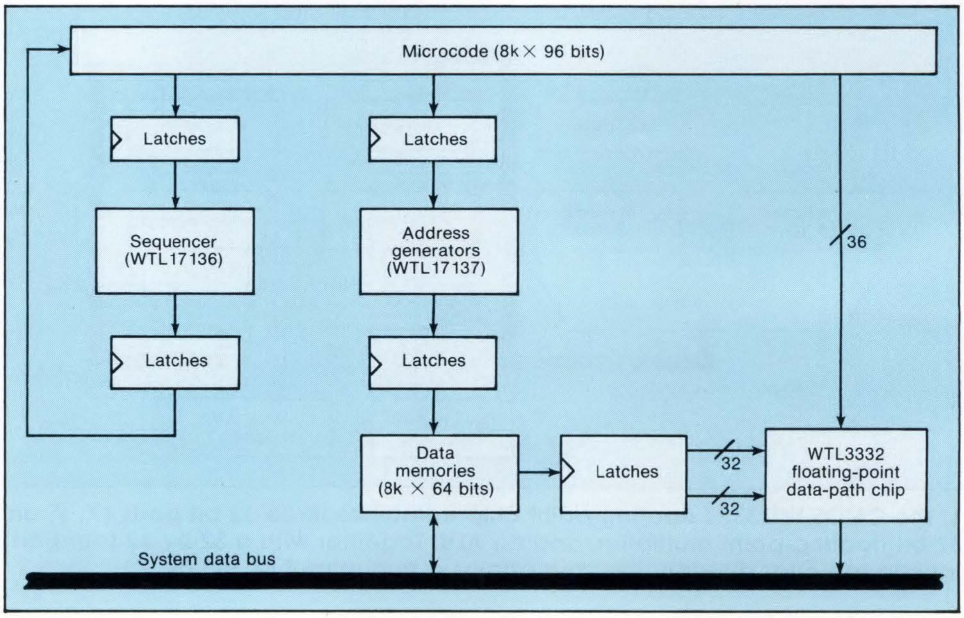
$$Y_1 = Y_0(2-XY_0)$$

The technique has second-order convergence to the exact answer. In other words, the number of correct digits in Y_{N+1} doubles with each iteration.

Because the chip has a 7-bit lookup table, the result is accurate to 14 bits after one iteration. After two, the result is accurate to 1/2 LSB. Since two iterations take only

Price and availability

Samples of both the WTL3332 and WTL3132 floating-point data-path chips will be available in June, with production quantities set for the third quarter. In quantities of 100, the three-port WTL3332 is priced at $425 and the single-port WTL3132 at $350. CIRCLE 501



2. A simple one-card system, driven by microcode, is created by linking the WTL3332 chip, a sequencer chip, and data memory. In digital signal processing, the system performs a 1024-point FFT and graphics transformation.

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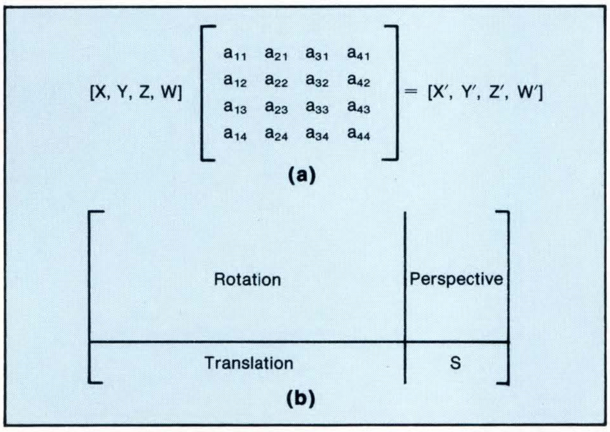
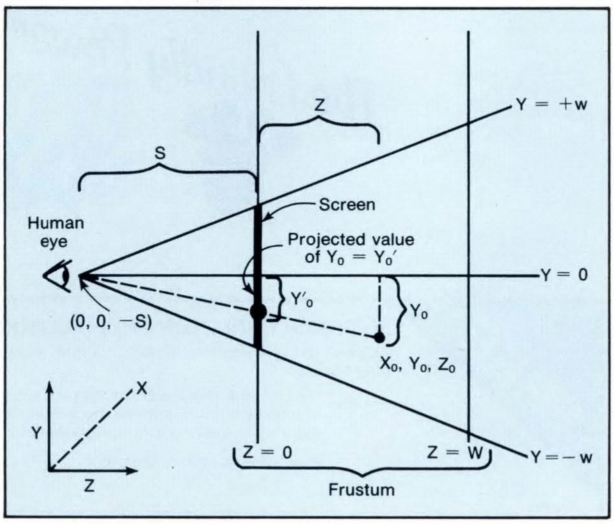
six cycles, division can be performed in 300 ns with the 50-ns chip.

It is important, of course, that the simulated results on the computer agree well enough with those achieved on the physical system. Therefore, the chip conforms whenever possible to necessary aspects of the IEEE-754. However, ease of implementation wins out over strict adherence to the standard wherever divergence from a difficult detail did not hurt numerical integrity.



3. When used in wireframe graphics, a 4 × 1 vector is transformed when it is multiplied by the 4 × 4 matrix (a). The type of transformation achieved is controlled by the position of the coefficients in the matrix (b). For example, the perspective of the displayed image is changed by the values a_{41}, a_{42}, and a_{43}.



4. Vectors that fall within the volume behind the screen extending from Z = 0 to Z = W, known as the canonical clipping frustum, are displayed on the screen. Those vectors outside the frustum are not mapped onto the screen and are rejected, a process called clipping.

The IC primarily digresses from the standard in that denormalized numbers (those at the input that are between 0 and the minimum normalized number, 2^{-126}, in single precision) are treated as 0. Further, underflow results (those between 0 and the minimum normalized single precision number) are set to 0 and the underflow flag is set high. A result that has reached an overflow condition after rounding is always treated as $+\infty$ or $-\infty$, depending upon the sign bit.

In the most important deviation from the standard, the chip's only rounding mode is rounding-to-nearest option (a format defined in the IEEE-754). That unbiased mode was used because biased formats, such as round towards infinity, cause data growth, which can destroy the results of many algorithms. The round-toward-zero mode, while unbiased, can add up to 0.999 bits rounding error per operation, which introduces an unnecessarily large noise source into the calculation. The round-to-nearest option is unbiased and adds a maximum of 0.5 bits of error per rounding operation.

Consider a wire-frame graphics transformation that executes code for transformation, perspective divide, and clipping. The operation transforms the coordinates of the end point of a vector in space from [X, Y, Z, W] to [X′, Y′, Z′, W′], where X, Y, and Z locate the point in space and W is the perspective value of the point.

In wire-frame graphics, the 4 × 1 vector is transformed by multiplying it by a 4 × 4 matrix (Fig. 3a). The coefficients in the matrix can be thought of as knobs on a TV set, with the vector being rotated and translated in space by changing the appropriate coefficients (Fig. 3b). Modifying the first three values of the fourth column changes the picture's perspective, while the picture's scaling is altered by the last entry in the last column.

To perform multiplication, the matrix coefficients a_{11}, a_{21} . . . a_{44} are stored in the chip's register file. Usually a single matrix can be used to transform a large number of points. With the three-port architecture, coefficients can be loaded into registers coincidentally with the transformation of the first point. That is, data can be simultaneously loaded into a register and used as an operand.

Once a vector is transformed it must be divided by the value for W′, so that the vector's new position is in perspective (see "Looking at Things in Perspective," p. 188). To divide each transformed coordinate, X′, Y′, and Z′, the reciprocal 1/W′ must be found and then multiplied by the coordinates. The division required to find 1/W′ requires six cycles. Notice that most operations in the divide algorithm require the result of the immediately preceding operation. Rather than wait for the three cycles required

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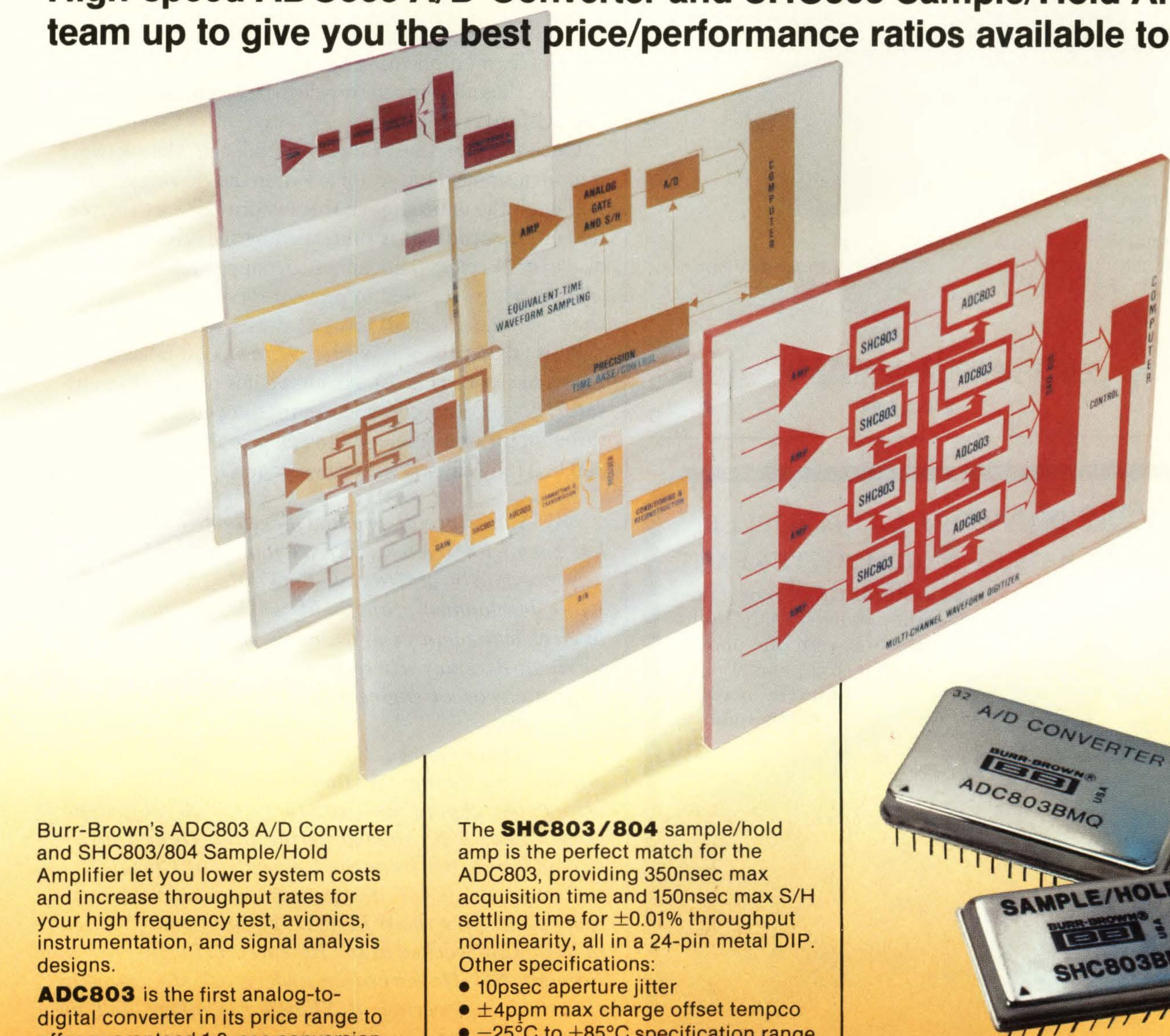

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Benchmark performance

Benchmark	Execution time* 50-ns chip
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FIR filter (per tap)	50 ns
Complex FIR filter (per tap)	200 ns
Graphics transformation, including clip	2 μs
Biquad filter section	200 ns

* Time for 100-ns chip is twice as long

to complete the multiplication-accumulation, a portion of the matrix multiplication has been interleaved with the division, thus allowing the divide to be completed in six cycles, without overhead.

Once the perspective divide is finished, the software must determine if the vector is within the viewing volume. Although the entire image is transformed, only the portion of the scene that is subtended by the screen space is displayed. Vectors that cannot be mapped into the screen space must be rejected to prevent them from wrapping back onto the screen. If any coordinate of a transformed point is greater than +W or −W, the point falls outside the screen space (Fig. 4). Assuming it is possible to transform, divide, and clip vectors in 30 cycles the overall throughput for a single 100-ns chip is about 250,000 to 300,000 fully clipped vectors a second.□

Y. W. Sing, special product development manager, has been with Weitek since its founding in 1981. He was previously at Hewlett-Packard, specializing in VLSI development. Sing holds an MSEE and a PhD in electrical engineering from the University of California at Berkeley. He received his undergraduate degree in electrical engineering from National Taiwan University.

John Oxaal joined Weitek in 1985 and manages product marketing for floating-point products. He also helps choose new products for development. Oxaal holds a BS in engineering from Duke University and an MBA from the University of Chicago.

George Chu, an IC design engineer, was instrumental in developing the WTL3332. Before joining Weitek in 1985, Chu worked at the Research Triangle Park in Raleigh, NC. He earned an undergraduate degree in electrical engineering at Shanghai College and an MSEE at North Carolina State University.

How valuable?	Circle
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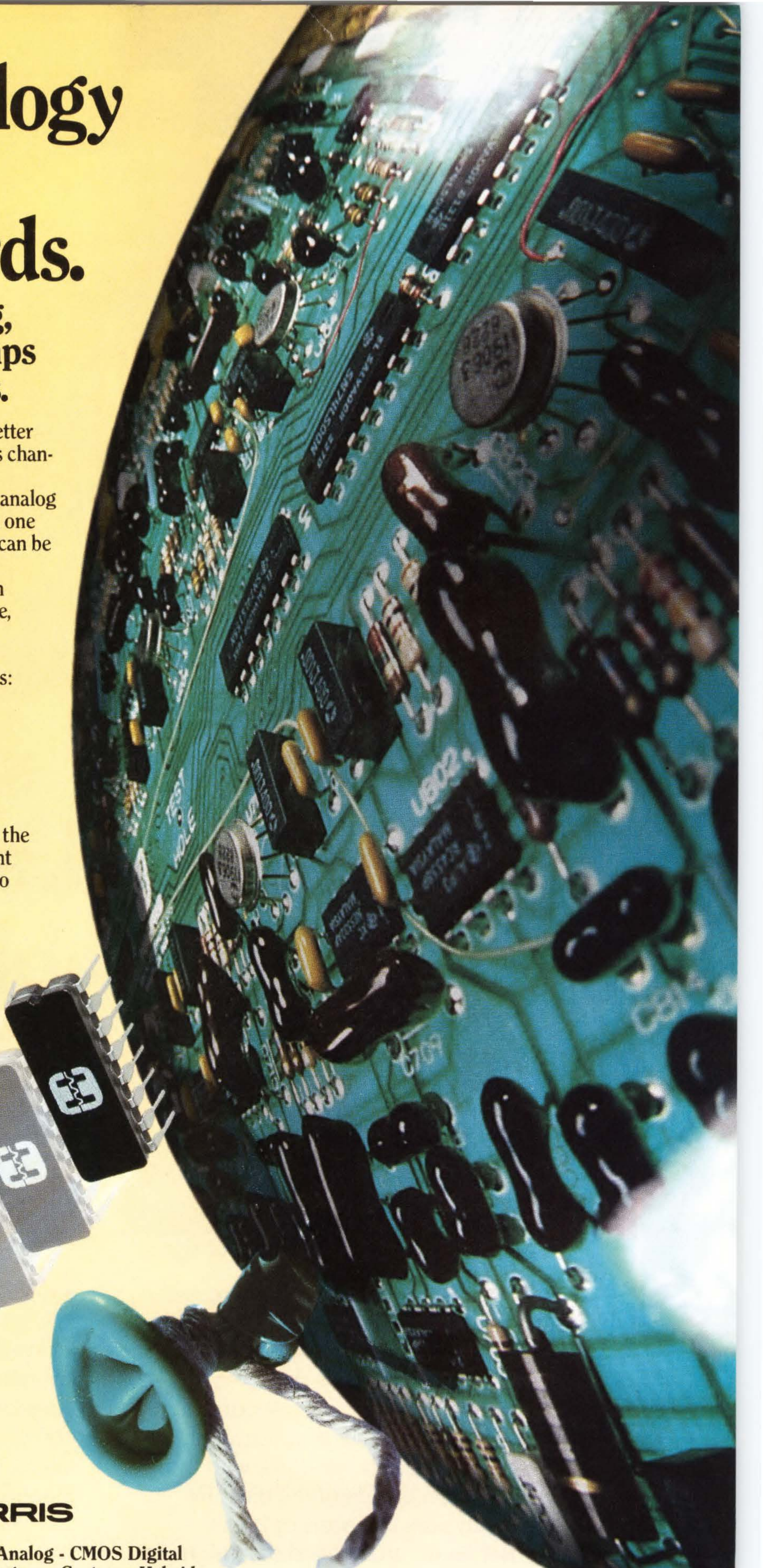

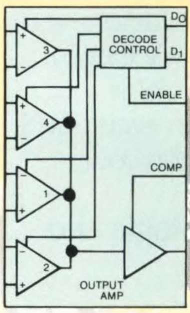

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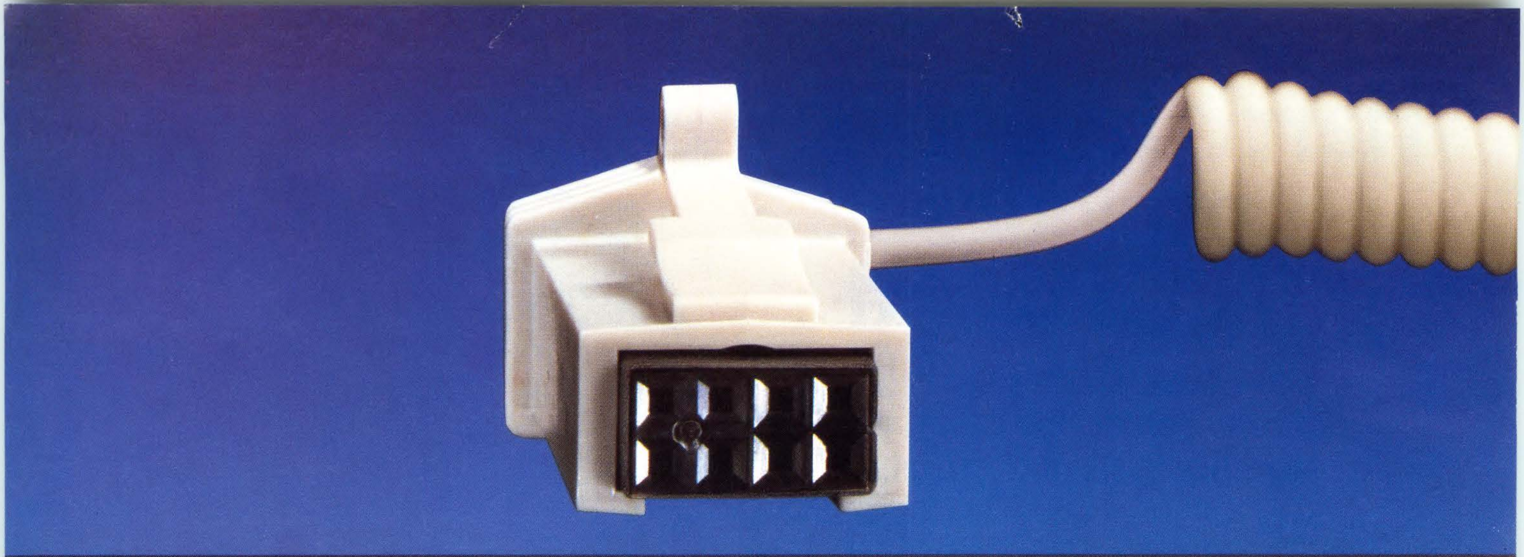

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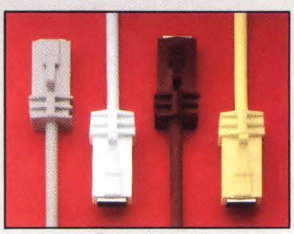

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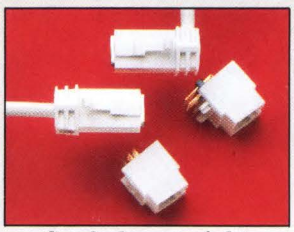

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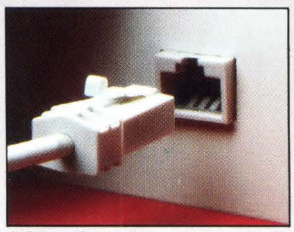

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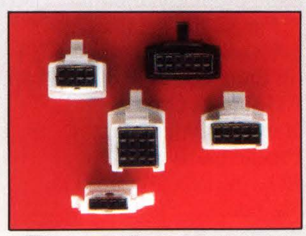

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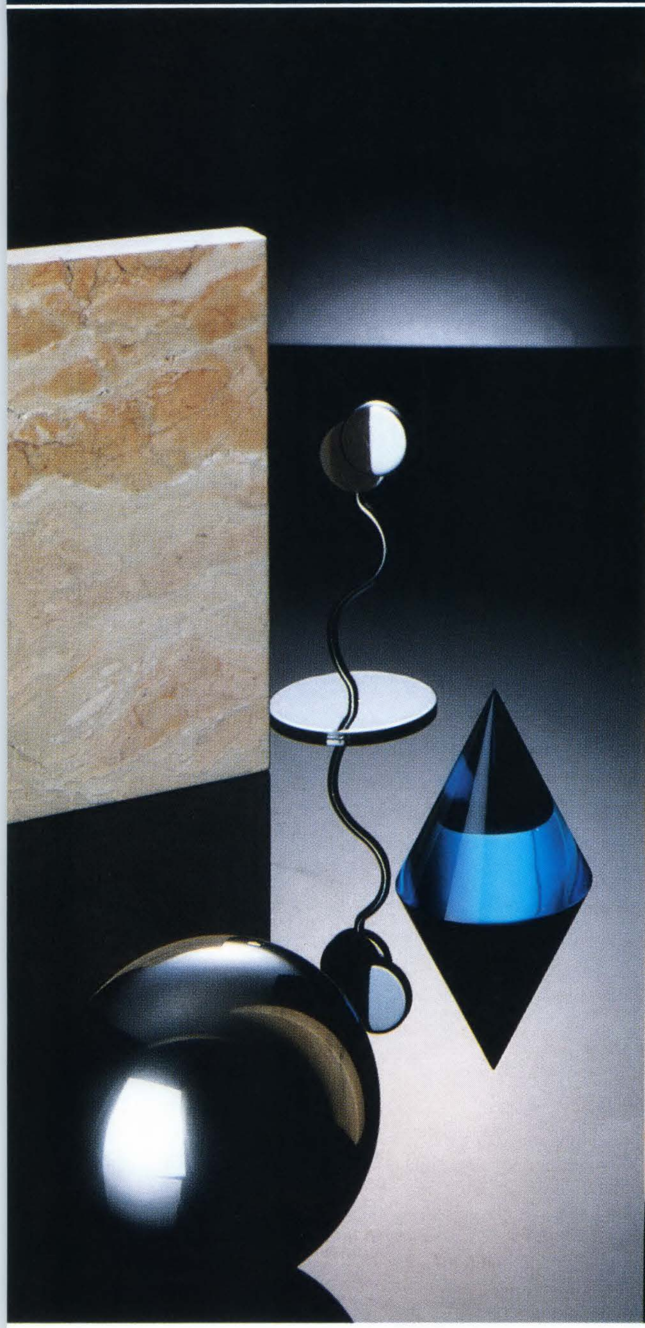

	Type No.	Generic	Feature	DIP	MINIFLAT
Single Op Amp	μPC741	μA741	General Purpose		
	μPC4081	TL081	J-FET Input		
	μPC4250	LM4250	Micropower		
			Programmable	8-pin	8-pin
	μPC4071	TL071	Low Noise J-FET Input		
	μPC4061	TL061	Low Power J-FET Input		
	μPC811	*	Low Offset, Low Drift,		
	μPC813	*	High Speed, J-FET Input		
Dual Op Amp	μPC1458	MC1458	General Purpose		
	μPC4558	RC4558	General Purpose		
	μPC4560	*	Improved 4558		
	μPC358	LM358	Single Supply		
	μPC4556	*	High Speed, Wide Band		
	μPC4082	TL082	J-FET Input	8-pin	8-pin
	μPC4072	TL072	Low Noise, J-FET Input		
	μPC4062	TL062	Low Power, J-FET Input		
	μPC4570	*	Ultra Low Noise,		
			Wide Bandwidth		
	μPC812	*	Low offset, High Stability		
			J-FET Input		
Quad Op Amp	μPC324	LM324	Single Supply		
	μPC3403	MC3403	Single Supply,		
			No Crossover Distortion	14-pin	14-pin
	μPC4741	HA4741	Low Noise, AC Application		
	μPC4074	TL074	Low Noise, J-FET Input		
	μPC4064	TL064	Low Power, J-FET Input		
Comparator	μPC311	LM311	High Speed, Single	8-pin	8-pin
	μPC319	LM319	High Speed, Dual	14	14
	μPC393	LM393	Single Supply, Dual	8	8
	μPC339	LM339	Single Supply, Quad	14	14
Others	μPC1555	555	Precision Timer	8-pin	8-pin
	μPC305	LM305	Precision Voltage Regulator	8	8
	μPC494C	TL494	Switching Regulator Control	16	16
	μPD5555	555	Precision CMOS Timer, Single	8	8
	μPD5556	556	Precision CMOS Timer, Dual	8	8

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Paper and pencil help guide initial calculations in move to standard-cell ICs

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John Pozadzides
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Decisions to integrate particular portions of a design with a standard-cell IC usually hinge on two factors: performance and cost. Performance improvements include not only greater speed, but reduced power, smaller size, and enhanced reliability, too. Despite designers' natural desire to upgrade performance, however, most also hope to cut cost with standard-cell ICs. But poor initial steps can have the opposite effect—pushing costs through the roof while forcing performance down.

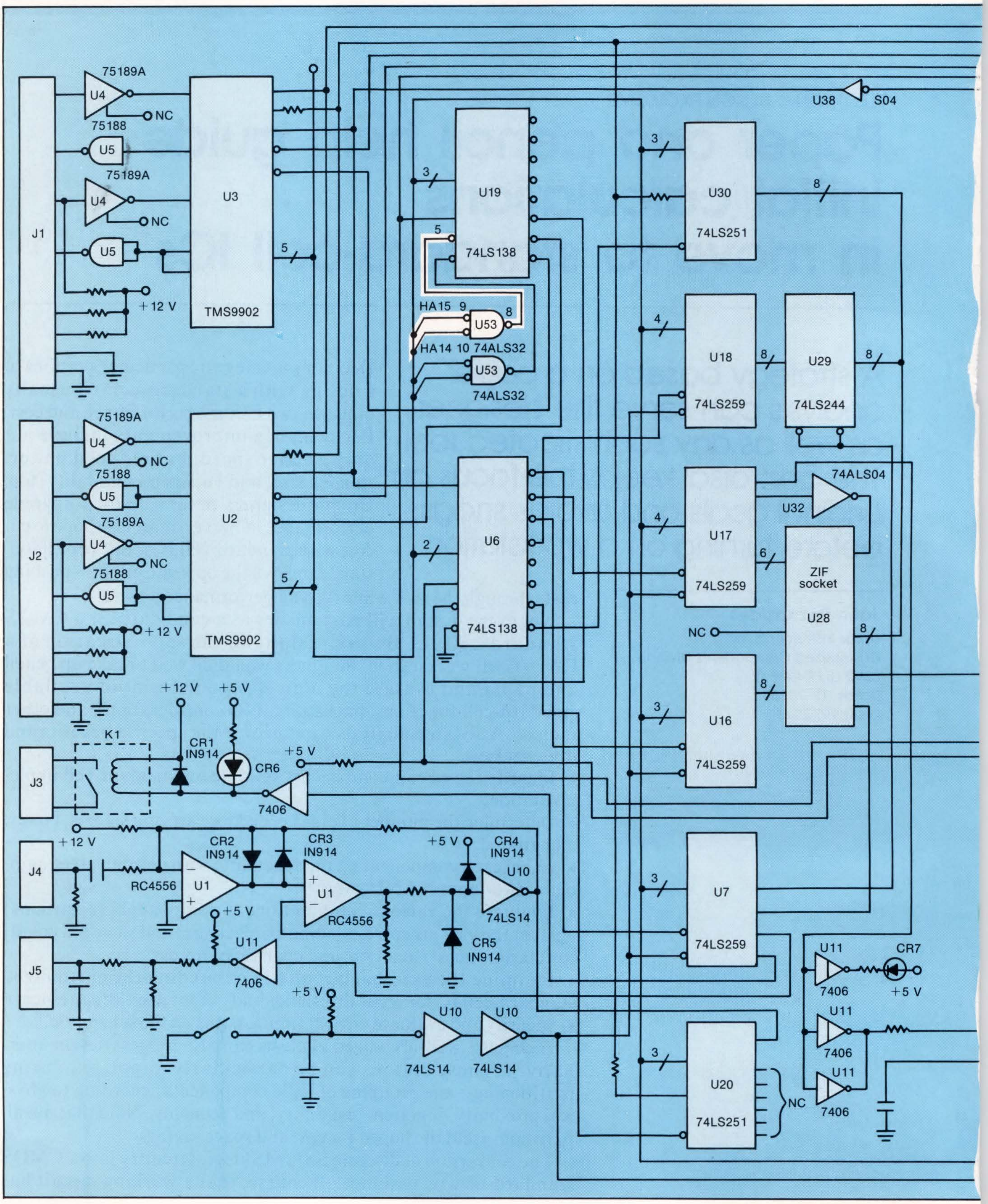
Not every design will pass muster as a candidate for a CMOS standard-cell IC. Before rushing to the sophistication of a CAD/CAE workstation, designers would do well to take up pencil and paper and evalute the logic design in terms of available standard-cell functions, packaging, I/O considerations, and other factors. A six-step analysis can uncover the specific benefits and drawbacks:

- Identify the circuit components suitable for standard-cell implementation.
- Determine the number of pins needed for carrying signals, power, and ground.
- Label each component on the schematic with its equivalent number of two-input NAND gates.
- Evaluate the various combinations of components (partitions) against the various corresponding IC packages and their pin counts to determine cost, function, and board area needs.
- Examine the external circuitry surrounding the customized standard-cell IC for input thresholds and output drive requirements.
- Identify and evaluate critical timing paths on the schematic.

A concise, well-organized analysis can also suggest design alternatives. Those options can be particularly important during partitioning—the grouping of logic components according to physical proximity, function, testability, and economy. Note that not all partitions yield the hoped for cost and space savings.

The conversion of discrete SSI/MSI logic circuitry into a CMOS standard-cell IC assumes, of course, that a working circuit has

Standard-cell strategy



already been designed and documented. During the first step, the analysis need only produce the list of candidates. Included are all 5-V TTL, LSTTL, and HC/HCT logic.

Once the candidates have been identified, thought must be given to packaging, including the different pinout limitations of standard styles. Most IC manufacturers can provide data for converting common SSI and MSI logic functions into the equivalent two-input NAND gates. The conversion establishes the total number of devices that can be built on the standard-cell chip.

MEETING NEEDS

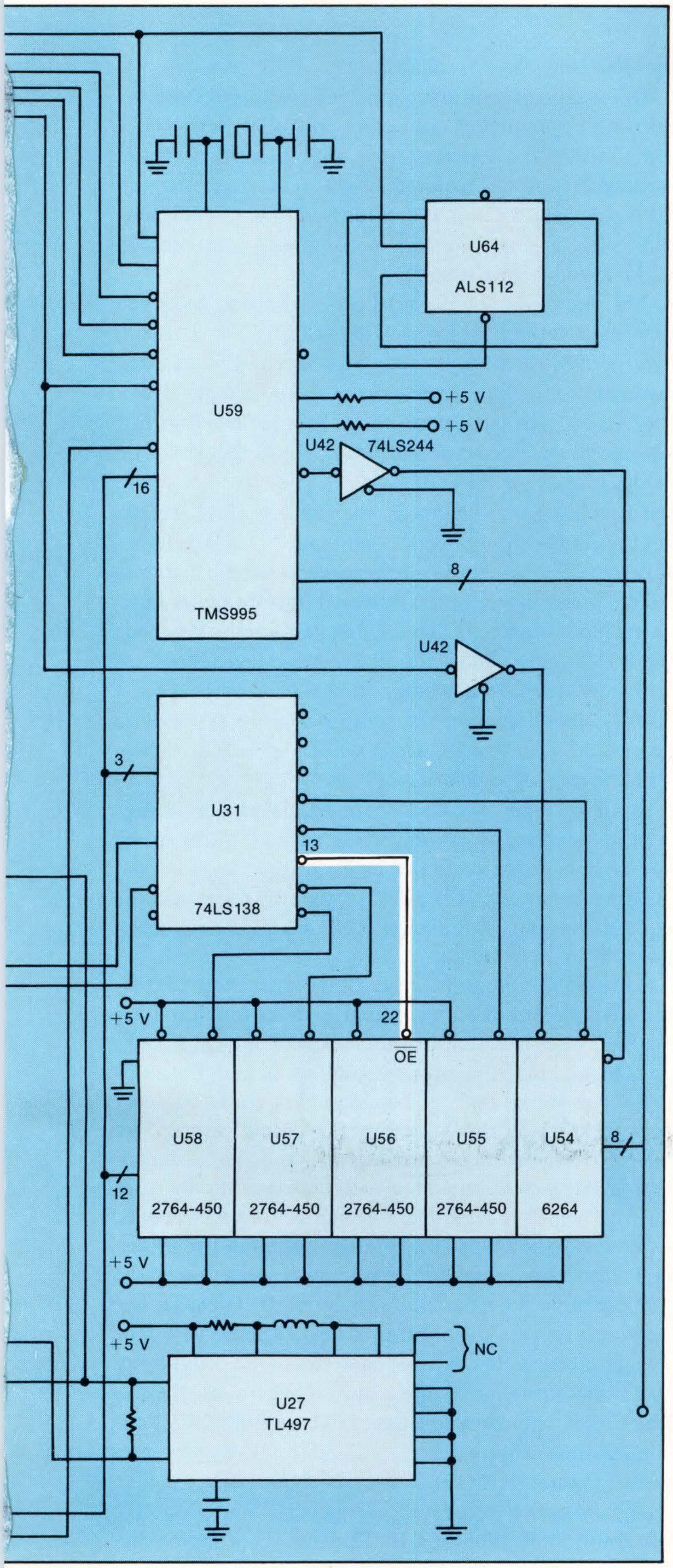
Since a standard-cell IC must interface with the outside world, the first-cut analysis must examine I/O requirements. Depending on I/O drive considerations and input buffering constraints, certain packaging options may be eliminated immediately. Depending on the design's required speed and critical timing paths, the semiconductor technology being considered may fail to meet the performance demands of the design.

Normally, total device count, I/O requirements, and package selection provide manufacturers with enough information to provide a price quote. Rather than submitting a single configuration for a price estimate, however, a prudent designer will have several partitions to give a manufacturer the opportunity to provide alternatives. The trade-offs thus presented balance total devices integrated against corresponding package types.

Any potential CMOS standard-cell implementation must pass a simple go/no-go adequacy test. For example, the maximum supply voltage mut be less than 7 V and the average propagation delay must be within the design's performance parameters. Moreover, the packaged device can have no more than 144 pins. If the design falls within the boundaries of the standard-cell family (Table 1), the designer can tag sections of the original schematic for standard-cell implementation.

THE REAL THING

An evaluation module for a DSP microcomputer, the TMS32010, can serve to illustrate the analytical process (Fig. 1). The designer selects and evaluates several blocks of circuitry within the module as candidates for standard-cell implementation. In this example, three alternatives have been identified to show the effects of different partitions on a design (Table 2). In all cases, the analysis calls



1. The integration of an existing design, here an evaluation module for a digital signal processor, into a standard-cell IC begins by identifying candidate components. Based on operating and packaging constraints, three different partitions can be identified (see Table 2).

for a 3-μm standard-cell process.

Not all of the components in the circuit have appropriate characteristics for integration. Here, 13 components offer that possibility (Solution I, Table 2). Generally, IC manufacturers offer extensive standard-cell libraries that include virtually all SSI and MSI logic functions, from simple gates and inverters, through shift registers, counters, PLAs, RAMs, ROMs, and on to microprocessors. For example, the Texas Instruments standard-cell library also contains a large collection of buffer devices that can be mixed and matched to solve a variety of drive problems.

After the appropriate circuit components have been pegged for integration, the designer determines the number of signal pins required by each alternative solution. Remember, some devices may not be fully utilized in the standard-cell version; unused circuitry and associated pins therefore can be excluded.

Of the several packaging options, a 68-pin package will maximize the number of discrete units that can be integrated within the device, thereby minimizing the number of standard-cell ICs required. On the other hand, 44- and 40-pin packages demand greater trade-offs among size, pin count, and the number of components integrated within the customized device.

The first of the solutions defined earlier uses all of the devices practical for integration (Solution I, Table 2, again); consequently, it needs 61 external pins. Adding four pins for the supply voltage, (V_{CC}) and ground gives a total of 65 pins. Therefore, the proposed device will fit within the pinout constraints of a standard 68-pin plastic leaded chip carrier (PLCC).

Continuing the evaluation, the analysis must account for the equivalent number of two-input NAND gates required by the standard-cell component corresponding to each discrete device in the proposed integration. A functional index obtained from the manufacturer will provide equivalent gate counts for all available logic functions within the standard-cell library. For the 13 components of the first design solution, the number of two-input NAND gates works out to 458, which will fit within the 68-pin PLCC previously selected.

If a particular TTL, LSTTL, or HC device does not appear in the index, an estimate must be made of the equivalent number of gates. In that case, the designer must convert the schematic of the device, gate by gate, into the equivalent standard-cell parts, while taking care to eliminate any unused circuits.

At this phase of the analysis, the designer should examine all of the partitioning options to determine the final configuration. Two considerations, silicon area and package pinout, guide the ultimate solution. In fact, the number of pins stands as the major consideration. To conserve pins, the designer should be aware of circuit features, like buses, that interconnect components but do not extend to the outside world. Enclosing such buses within the standard cell will save a considerable number of package pins.

Whereas the first solution integrates all of the 13 discrete devices possible, the second option seeks to keep the number of pins to a minimum (Solution II, Table 2). The approach reduces the number of devices replaced by the standard-cell IC to five. The equivalent gate count drops to 375 and the required pins to just 44. Therefore, the second option can use a less expensive 44-pin PLCC. Although the design will hold only 82% of the gates integrated in the first option, it saves 24 signal pins.

A third option integrates 8 components but reduces the pin count to 40 (Solution II, Table 2). That option dic-

Table 1. Allowable operating conditions

Parameter		Minimum	Nominal	Maximum
Supply voltage, V_{CC}		3.0 V	5.0 V	6.0 V
Average in-circuit propagation delay (2-input NAND), t_p	3μm 2μm	2.4 ns 1.3 ns	3.2 ns 1.7 ns	4.3 ns 2.3 ns
Clock frequency, for positive edge-triggered toggle Flip-flop	3μm 2μm	N.a.	N.a.	33MHz 60MHz
Operating free-air temperature, T_A		−55°C	+25°C	+125°C

N.a. = not applicable

Table 2. Integration solution evaluation

Unit number	Solution I External pins	Solution I Equivalent NAND gates	Solution II External pins	Solution II Equivalent NAND gates	Solution III External pins	Solution III Equivalent NAND gates
U31	9	20				
U32	0	0.5				
U38	0	0.5				
U16	8	90	9	90		
U17	8	90	9	90		
U18	5	90	1	90	5	90
U29	0	15	8	15	0	15
U7	7	90	13	90	7	90
V_{CC}	2	—	2	—	2	—
GND	2	—	2	—	2	—
U19	6	12			6	12
U6	3	16			3	16
U20	2	10			2	10
U30	9	20			9	30
U53	4	4			4	4
Totals	65	458	44	375	40	257
ICs replaced	13		5		8	

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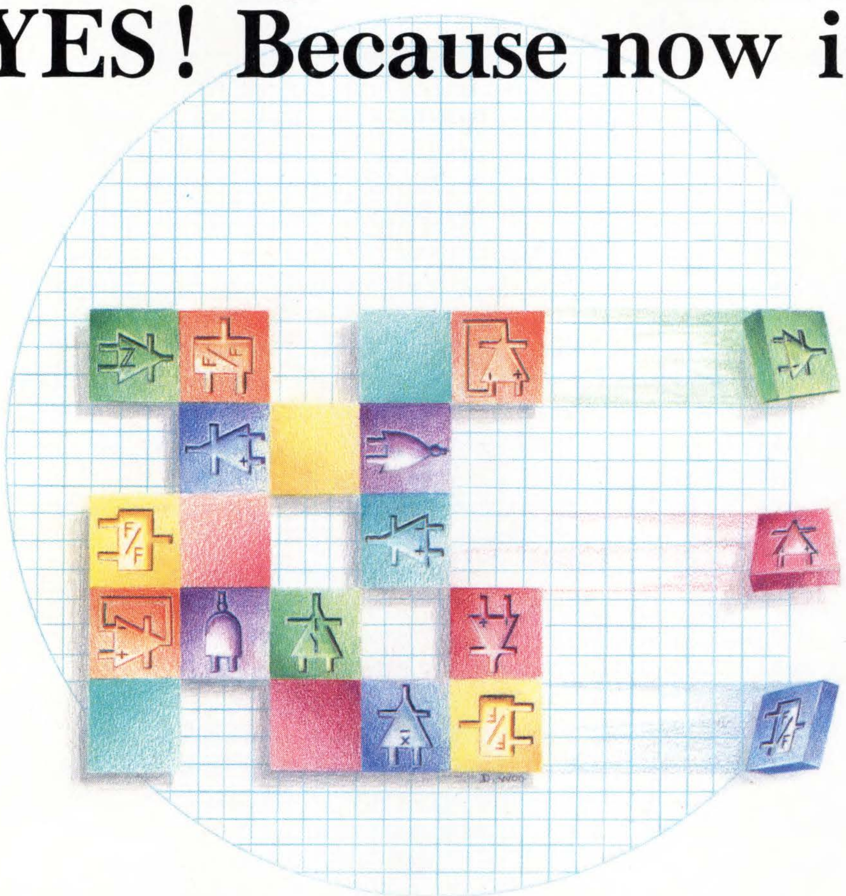

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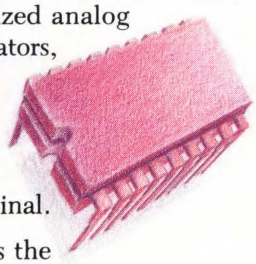

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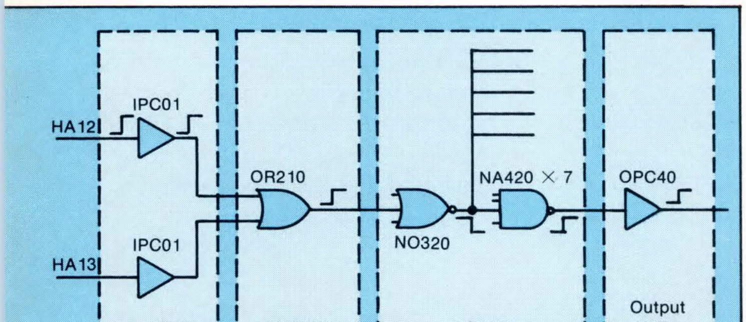
tates a change to a DIP, since only this style offers exactly 40 pins. Unfortunately, the efficiency of integration of the third option suffers: The 40-pin DIP holds only 56% of the original gates.

The area occupied on a pc board must also figure in an evaluation of package types. In general, board area estimates depend on how tightly the layout is packed. In a loose layout, board designers usually allow 1 $in.^2$ for each 14- or 16-pin DIP. If board space is at a premium, as little as 0.7 $in.^2$ may be allotted to the same devices. For purposes of evaluation, the analysis should compromise by allowing 0.9 $in.^2$ for each DIP.

The first solution provides a dramatic savings in board space. The 68-pin PLCC occupies just 1.5 $in.^2$ but replaces 11.88 $in.^2$ of discrete components in DIPs. The second solution produces less dramatic space savings. The 44-pin PLCC occupies 1 $in.^2$ while replacing five DIPs that spread across 4.68 $in.^2$. The final packaging arrangement gives the least space saving. A 40-pin DIP takes up 4 $in.^2$, but the third solution replaces discrete components that consume 7.38 $in.^2$ of board space—a saving of just under 50%. Clearly whenever possible, a PLCC should be used instead of a DIP to conserve board area.

CHECK THE INTERFACE

Since most standard-cell ICs must talk to other devices, interfacing enters into the analysis. The designer should check the external circuitry to determine input thresholds and output drive needs. The logic levels of each input and output and the maximum required dc current determine the I/O needs of any design.



2. In a critical timing path analysis, standard cell equivalents substitute for the discrete ICs in the original design. Here, a critical path in Fig. 1 (U2, U53, U19) is represented by its elements from the standard-cell library.

I/O buffers rarely appear in circuits that contain TTL ICs, but they must accompany all standard-cell designs. Therefore, the evaluation needs to consider the added propagation delays imposed by the I/O buffers. As a general rule, standard cells should be chosen over gate array if the circuitry around the device consists largely of TTL devices with relatively high drive currents. Gate-array I/O buffers have limited drive capabilities compared with standard-cell types.

Open-drain buffers in the 3-μm CMOS standard-cell family under consideration can push out 40 mA; push-pull and three-state buffers can deliver 10 mA. In contrast, many gate-array buffers are limited to just 2 mA of drive current. Moreover, the standard-cell buffers can generally be mixed and matched in a variety of combinations to solve virtually any drive difficulty.

The circuit schematic offers an example of output-buffer selection (Fig. 1, again). Pin 13 of device U31, a 74LS138 3-to-8-line decoder-demultiplexer and one of the logic elements chosen for integration in Solution 1, drives pin 22 of U56, a TMS2764 EPROM. According to the specifications for each device, pin 22 of U56 must see an input capacitance of 6 pF and pin 13 of U31 must not source more than 400 μA or sink more than 4 mA. Proper timing requires a low-to-high transition time (t_{PLH}) of 4.8 ns and a high-to-low transition time (t_{PHL}) of 18.9 ns for the signal between those units.

An analysis of the signal path of the 74LS138 (from a TTL data book) indicates that the device has an inherent t_{PLH} of 18 ns and a t_{PHL} of 32 ns from pin 1 to pin 13. (Those timing values are specified at an ambient temperature of 25°C and a supply voltage of 5 V.)

In the standard-cell library, the SN54/74SCM138 directly replaces the 74LS138. However, the chip requires a compatible input buffer, an SN54/74SC5006 noninverting type, which is also selected from the library. The total timing path of the integrated device—input buffer, SCM138, and output buffer—must match the magnitude of a discrete LS138. To select the proper output buffer, the designer must calculate its timing limits by subtracting the delays of the input buffer (the SC5006) and the SCM138 from the specified t_{PLH} and t_{PHL} of the discrete LS138. According to the specifications in the standard-cell library, the SCM138 presents a nominal delay of 6.4 ns and a worst-case delay of 8.6 ns.

Subtracting the delays of the input buffer and the SCM138 gives a maximum allowable t_{PLH} of 4.8 ns and t_{PHL} of 18.9 ns for the output buffer. The buffer chosen from the standard-cell library to meet those qualifications is the SN54/74SC5103, which possesses a t_{PLH} of 3.0 ns and a t_{PHL} of 7.0 ns. In addition, it meets the 400-μA

source current and 4-mA sink current specifications. The same worst-case analysis must be performed to select all of the output buffers within the standard-cell IC.

As a rule, the 3-μm CMOS standard-cell technology meets or exceeds the dynamic performance of the TTL, LSTTL, and HC technologies being replaced. But as in any CMOS process, the standard-cell version is quite sensitive to capacitive and dc loading conditions. Therefore, a designer needs to evaluate switching parameters in light of the loading conditions presented to the device.

CRITICAL PATH

One of the critical timing paths involves U53, a 74ALS32 quad two-input NOR gate (Fig. 1, again). The gate is driven by a TMS9902 asynchronous communication controller and in turn drives a 74LS138 decoder-demultiplexer, U19. Each of the components in the critical path from the 9902 through the output of the LS138 is modeled with the corresponding component chosen from the library (Fig. 2). Only the output drivers of the 9002 are shown as the equivalent 74SC5006. Other designations, such as IPC01, refer to the actual standard-cell elements for the components in the path.

If the dynamic timing requirements of the path can be satisfied, 3-μm technology will suffice for the design. If not, a faster 2-μm CMOS standard-cell family will be required. From the original design, the maximum permissible propagation delay through the critical path is 45 ns.

To compute the critical-path propagation delay time, a designer must consult the appropriate data sheets for each element. By simply adding the worst case propagation delay times for each element, a designer can determine the total delay time for the critical path. In this case, a total time of 42.37 ns is found for the elements chosen. Since the total does not exceed the 45-ns time required by the design, the elements in that path represent an acceptable solution. □

John Pozadzides is the internal programs manager for the application-specific IC division at Texas Instruments. He has held positions as wafer fabrication process engineer, digital circuits design and product engineer, linear circuits engineering manager, semicustom circuits engineering manager, and marketing manager. He holds a BS in applied physics from Auburn University.

How valuable?	Circle
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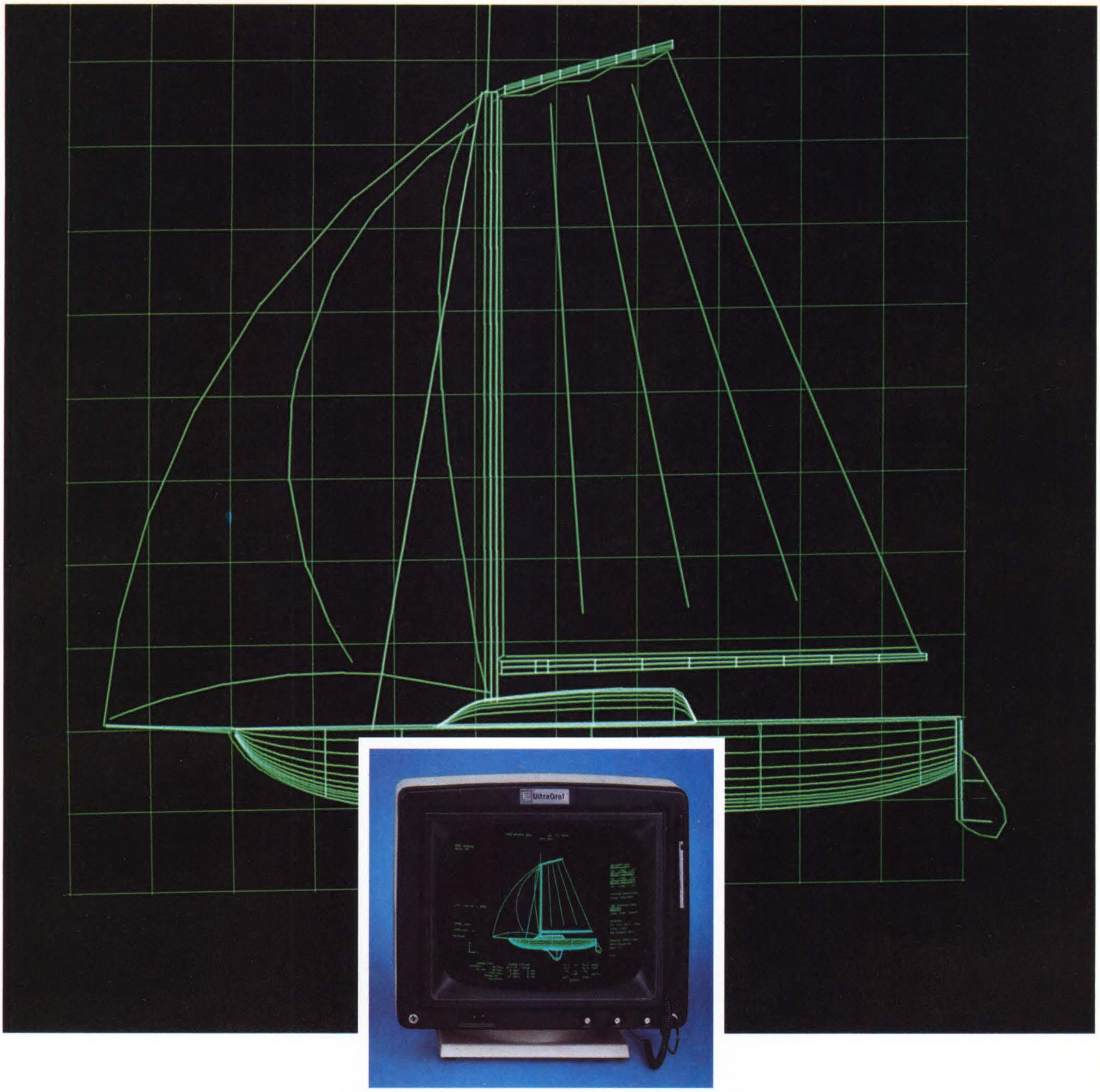

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CIRCLE 101

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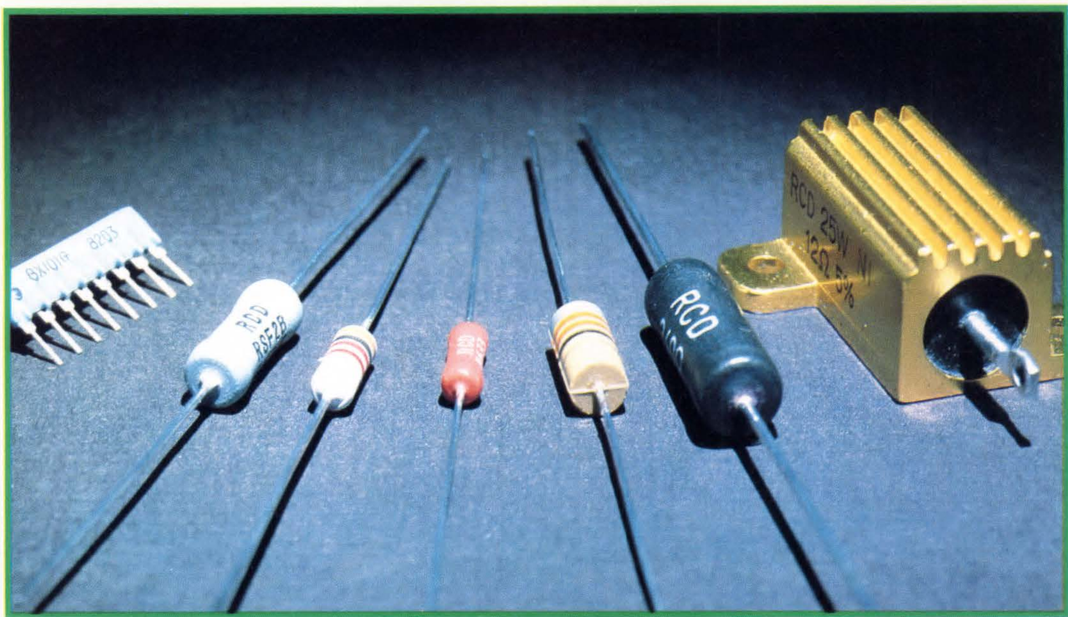

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CIRCLE 103

PRODUCT REPORT

FOCUS ON ZIF AND LIF CONNECTORS

Ian Michaels

As connector pin counts climb to the hundreds and beyond, even 5 to 6 oz of insertion force per pin means an unacceptably high overall mating force. It would take a weight lifter to squeeze such connectors together, with the likelihood that the parts would break, rather than mate, under the pressure.

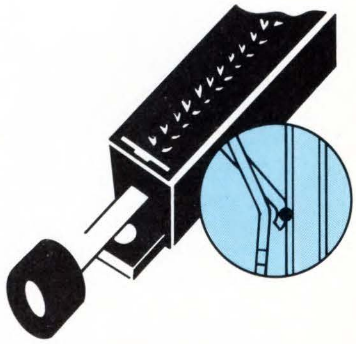
Cam-actuated zero-insertion-force (ZIF) and low-insertion-force (LIF) connectors, which need much less insertion force, both offer ways to get around the problem, but have drawbacks that may cut reliability even while easing the insertion process.

Connector contact surfaces become coated with contaminants and corrosives that must be removed or penetrated if the connectors are to be reliable. With standard connectors, wiping action and high normal forces penetrate surface films but together require a high insertion force. ZIF and LIF connectors employ a variety of means to try to maintain reliability while lowering insertion force.

Most ZIF connectors employ a very high normal force and eliminate wiping action altogether; recent designs combine a high normal force with limited wiping action (see "The Hottest Thing in ZIFs," p. 215).

Most LIF connectors, on the other hand, emphasize wiping, but employ a low normal force. In most cases, the low normal force has led to problems, and recent research has explored ways to increase normal force without a corresponding increase in insertion force. Various lubricating systems have been tried, with both good and bad side effects. Well-established types of LIF connectors with large numbers of contact points do work well, but they are costly to produce. As a result they are used mainly by the military.

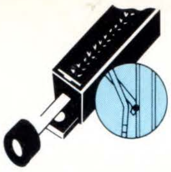
With ZIF connectors, the socket (female) portion opens up so that the plug can be inserted with no friction, no mechanical resistance, and no wiping action. After insertion, flipping a cam or lever makes the socket bear down on the plug. Since that applied normal force is the only means provided for penetrating surface films, the move calls for a rather high normal force — about 150 g. But in recent years, since connector manufacturers have cut back the use of gold on contacts, high normal force is sometimes not enough to ensure reliability. At least a limited amount of wiping action in ZIF connectors has become necessary.



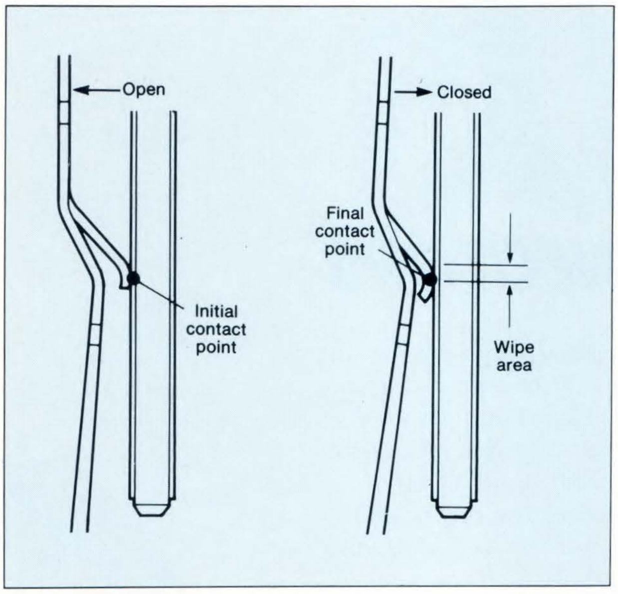
Zero-insertion-force and low-insertion-force connectors make it easy to boost pin counts, but can they do it reliably and at low cost?

Some makers have designed their cam-actuated closing mechanisms so that the contacts slide past each other slightly as they come together (Fig. 1). The wipe is a glancing arc rather than a sliding movement parallel to the pin surface, but research at Precision Connector Designs shows that as little as 1 mil of wiping provides stable contacts at any normal force of more than 150 g.

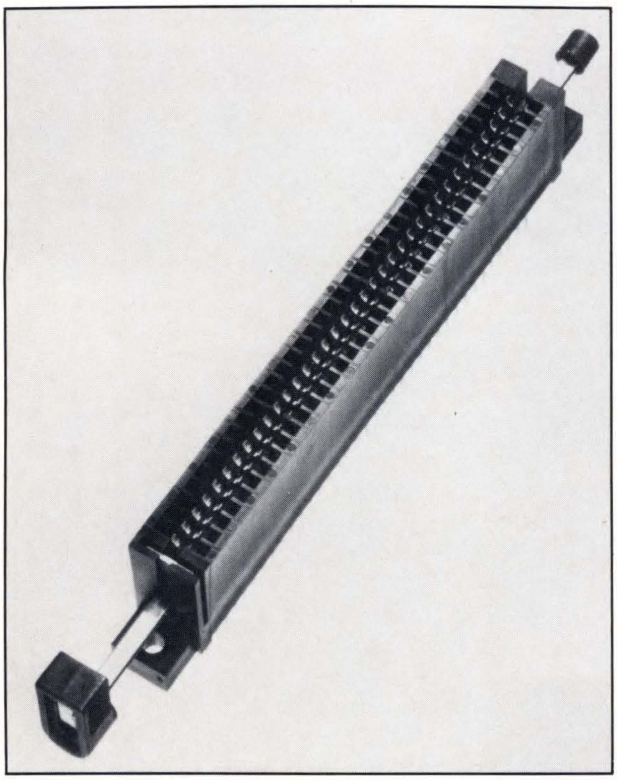
Users say, however, that a ZIF connec-



Focus on ZIF and LIF connectors



1. Contact wiping, which contributes greatly to contact stability by removing contamination, is limited by the ZIF contact's geometry. Even a very slight wiping action greatly enhances contact reliability if the normal force is high enough.



2. A linear connector from Precision Connector Design is noteworthy for a high normal force of 200 g nominal and 150 g minimum.

tor's normal force can decline with use. A connector with a nominal rating of 100 g may produce a normal force of as much as 180 g when new, but this force may soon drop to less than the rated 100 g, especially under high temperature. One connector, it is reported, had to be downrated from 105° to 85°C. While no universal solution to the declining-force problem is in sight, being aware of it is a start.

Users should shop around. Amp makes the widest line of ZIF connectors, including card-edge connectors with up to 175 dual connections, 0.1-in. contact spacing, and levers or bell cranks for actuation. Its rotary-cam edge connectors, with up to 65 dual contacts at 0.1-in. spacing, provide two important features: wiping and sequential contacting. Because the contacts move across the card-edge pads as the connector closes, wiping contacts are especially suitable where contamination is likely. Sequential contacting protects delicate circuitry by allowing power and ground circuits to make before, and break after, the signal circuits connect and disconnect. On connectors with this feature, the six pairs of contacts farthest from the cam handle close before and open after the remaining contacts when the cam is actuated. Amp produces ZIF connectors for stacking boards with up to 50 dual-position contacts.

Precision Connector Designs, whose research has shown the importance of high normal force in conjunction with even minimal wiping action, has a line of card-edge connectors with a nominal normal force of 200 g (150 g minimum). The connectors, which employ a special dual-action contact spring, are available with contacts on 0.100-in., 0.125-in., and 0.156-in. centers (Fig. 2). The company makes units with up to 130 contacts in two rows of 65.

THE WELL ROUNDED CONNECTOR

Although card-edge connectors are the primary type of ZIF device, not all ZIF connectors are linear. ITT Cannon makes a round cable-to-cable or cable-to-panel ZIF connector, which it calls RDL. When the connector is mated, the contacts pass each other without touching. But a one-eighth turn to the coupling nut locks the connector and brings the hermaphroditic contacts together with a slight wiping action. ITT Cannon's RDL ZIFs can accommodate up to 82 contacts.

Cannon also has modular rectangular ZIF connectors with up to 2496 connections. Again, plug and receptacle contacts do not touch while the connector halves are being engaged. The rectangular plug is placed over the receptacle, and a quarter turn of an actuating shaft electrically mates all contacts at once while mechanically locking the halves of the connector together.

Among solutions to the ZIF contact-wiping problem, one that does not call for a lower pin count makes use of an LIF connector, which has sliding contacts but a low insertion force. Most LIF connectors, indeed, have insertion forces of less than 3 oz per pin. Those with a force of less than 1.5 oz per pin are called very-low-insertion-force (VLIF) connectors. Conventional 0.025-in. box-and-post connectors have an insertion force of around 6 oz per pin.

LIF connector contacts do produce a sliding wipe, but cutting the insertion force from 6 oz per contact to 1 oz or less may affect the connection's stability. Lowering insertion force simply by opening up the contacts may lower the normal force to a point where the wiping does not remove enough of the oxidation to allow current to flow.

In a sliding-contact configuration, 100 g of normal force is usually enough, but contact resistance rises as normal force drops. At just under 50 g, the curve of electrical resistance vs normal force begins to climb sharply, and for some designers, 50 g of normal force comes too close to the knee of this curve. If the gold plating is very thin, still greater normal force may be required, as the base metal may diffuse. Increasing the normal force helps to seal any microscopic voids in the plating.

The hottest thing in ZIFs

ZIF connectors have no insertion force but, once locked up, most have high normal forces. One exception exists: a Metcal connector that mates with no insertion force and no normal force at all. With an integral heater, it literally solders itself together when connected to a special rf power head.

Applying the same power head melts the solder and allows the connector to be separated. Metcal says the connector can withstand hundreds of mate-unmate cycles, and is at present evaluating a prototype.

The connector has some interesting characteristics besides the shock and vibration resistance of its solder joint. Elimination of stamped parts plated with precious metal cuts the cost per circuit line. Second, the self-soldering connector requires one joint only, instead of one to the input side of the connector, one at the actual contact, and one at the output side.

The connector has integral grounding, shielding, heat sinking, and environmental sealing. Finally, since there are no 90° bends and only one lap-solder joint-reflection point, impedance matching should be easier than with other ZIF techniques.

However, insertion force can be lowered while still maintaining adequate normal force. Max Peel, president of Contech Research (Attleboro, Mass.), which studies and tests connectors and surface-mounted devices, says this is probably the most promising direction for LIF development, but one that few manufacturers are exploring. Possible approaches, says Peel, include contact geometries designed with close attention to the pin's angle of attack into the socket. A pin with a 15° ramp can as much as halve insertion force. Although there have so far been no product announcements, such new geometries are likely to reach the marketplace soon. They will, however, be two-piece contacts, and therefore more expensive than the conventional one-piece units.

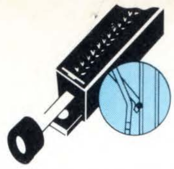
THE PROS AND CONS OF LUBRICATION

Lubrication has also been suggested as a way to reduce the amount of insertion force. Amp has a graphite-impregnated gold plating that acts as a built-in electrically conductive lubricant; other systems use extremely thin coatings of Monsanto's OS124 lubricant. Synthetic waxes have been tried, since they tend to adhere to the surface, but because they evaporate their life expectancy is unpredictable. An overall disadvantage of lubricants lies in their tendency to collect dust. Furthermore, external lubricants may not survive wave-soldering and may have to be applied at the end of the assembly process. On the other hand, lubricants sometimes compensate for thin-plating porosity by sealing microscopic voids in the plating. On the whole, lubricants have been widely discussed but not widely used.

Hughes Aircraft's Connecting Devices Division has, through carefully designed contact geometries, achieved an engagement force of 1.5 oz per pin in a 296-pin, 4-row-by-74-pin connector with center-to-center spacing of 0.100 in. Methode Electronics' MHD high-density connectors provide 3-row and 4-row 1.5-oz connectors with up to 516 contacts on a 0.100 by 0.100 in. grid.

Teradyne Connection Systems, a leading supplier of backplane interconnection systems, uses LIF techniques. The company's two-piece connector systems accomplish what it refers to as ultralow-insertion force—2 oz maximum, 1.8 oz nominal insertion—by using special male and female contact geometries. Contacts are coined and micropolished smooth after plating and then tumbled to remove all burrs.

While many LIF connectors spread their contacts to reduce insertion force, there are two special contact configurations that require very low insertion forces but do not sacrifice contact integrity. In spite of their costliness, Bendix Connector Operation's Bristle Brush Bunch and



Focus on ZIF and LIF connectors

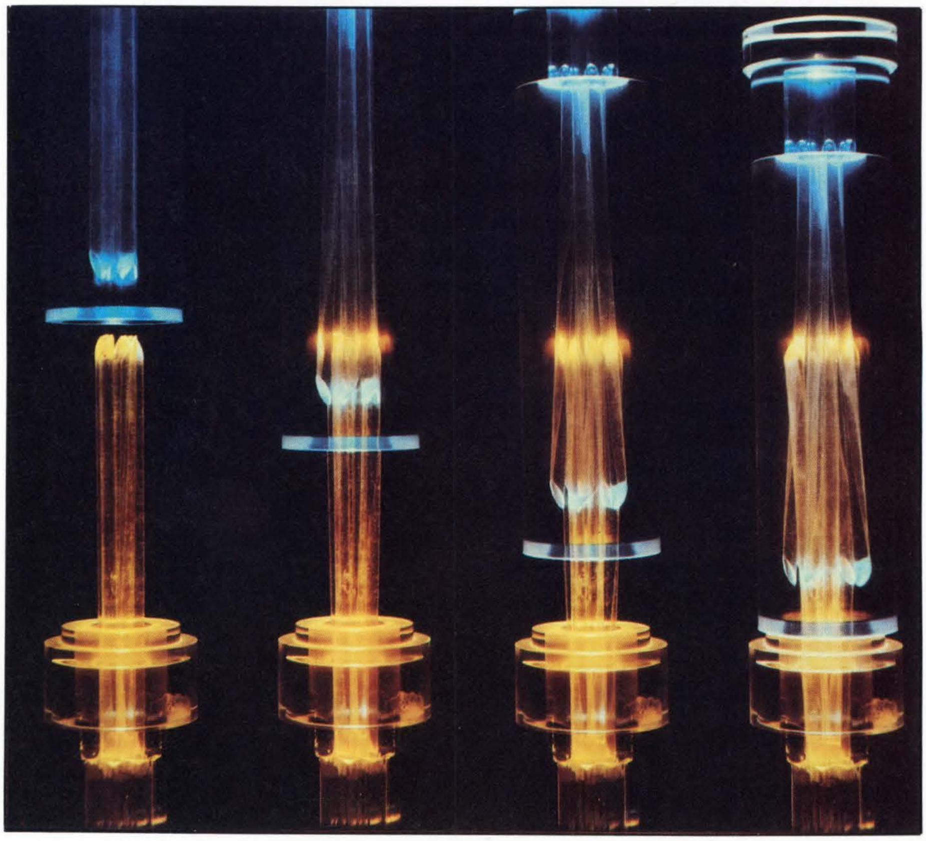
Hypertronics' Hypertac contacts, neither of them new developments, are receiving renewed attention as contact counts soar. Their remarkable performance comes from having sockets contacting the inserted pin at several points. Their cost has held back commercial interest, but both configurations have found use in demanding military applications.

Bendix pc board connectors feature Bristle Brush Bunch (B3) contacts with a mating force of no more than 0.3 oz per pin, only 10% to 30% of that needed in conventional pin-socket contacts. B3s are made of high tensile-strength wires bundled into brushlike contacts intermeshed in pairs that form a gas-tight connection. These connectors have low contact resistance and will withstand over 20,000 mating-unmating cycles (Fig. 3). B3 connectors are available in 2-, 3-, and 4-row contact configurations, with from 10 to 100 contacts per row for a maximum of 400 contacts.

Hypertacs (hyperboloid contacts), although different in principle from conventional contacts, resemble the Bristle Brush type in concept. Their distinguishing feature is the hyperboloid-shaped sleeve formed by wires strung at an angle to the socket's axis (Fig. 4). When the pin is inserted into this sleeve, the wires stretch to accommodate it, wrapping themselves around it to provide a number of linear contact paths. Since contact resistance is largely a function of contact area, these multiple paths reduce resistance.

The Hypertac's multiple-line contacts provide far greater contact area than others of comparable size. The wires' wiping action ensures a clean and polished surface, and their complete encirclement of the pin, together with the greater contact area, does away with any need for high contact forces. The spring rate and resultant stress are also greatly reduced, and the smooth insertion-extraction force is so low that even 400-pin connectors can be mated and unmated with ease. Other Hypertac advantages include higher current ratings, less wear from contact pressure, greater reliability because of contact redundancy, and good performance under shock and vibration.

Burndy is the first manufacturer to combine surface-mounting technology with both ZIF and LIF card-edge

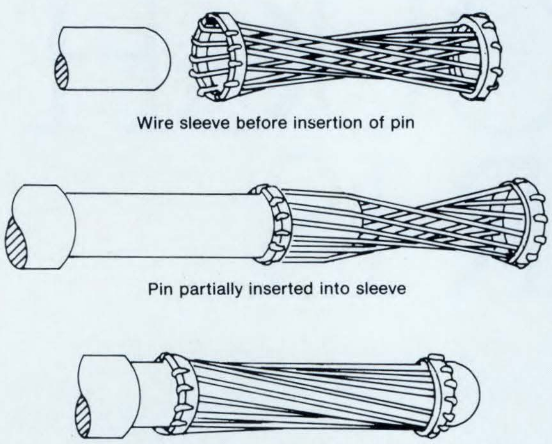


3. In Bendix's Bristle Brush Bunch contact, high-strength wires in brushlike bundles intermesh with very little force—about half an ounce per pin—to form electrically stable, gas-tight connections.

connectors. The company's 0.025-in. center-to-center Surfmate LIF connector packs 80 I/O contacts per inch along the card's edge, for up to 318 contact positions. The 0.050-in. center-to-center Ziflex model has 40 I/O contacts per inch for up to 300 contact positions, but uses a cam-actuated ZIF arrangement (Fig. 5). The real magic in both Surfmate and Ziflex lies in their having a surface-mounting interface with the backplane, instead of needing holes for the card-edge connector.

Either connector may also be bolted to the backplane. The connector to the card-edge interface is a set of gold-plated contacts, and the surface-mount connector-backplane interface is a tin-lead system. By not gold-plating the motherboard—or drilling lead holes—designers are able to cut manufacturing costs, and since through-holes present obstacles to the routing of the conductive traces, it may even be possible to reduce the number of layers in the circuit board.

The difficult process of vapor-phase soldering the surface-mounted connector is eliminated. The connector is divided into a number of floating modules, each of which can be aligned independently with respect to the backplane, using a single plastic peg that ensures the registration of many hundreds of contacts. Only one alignment hole is needed in the board for every 2 inches of connector.



Source: The Hypertronics Corporation

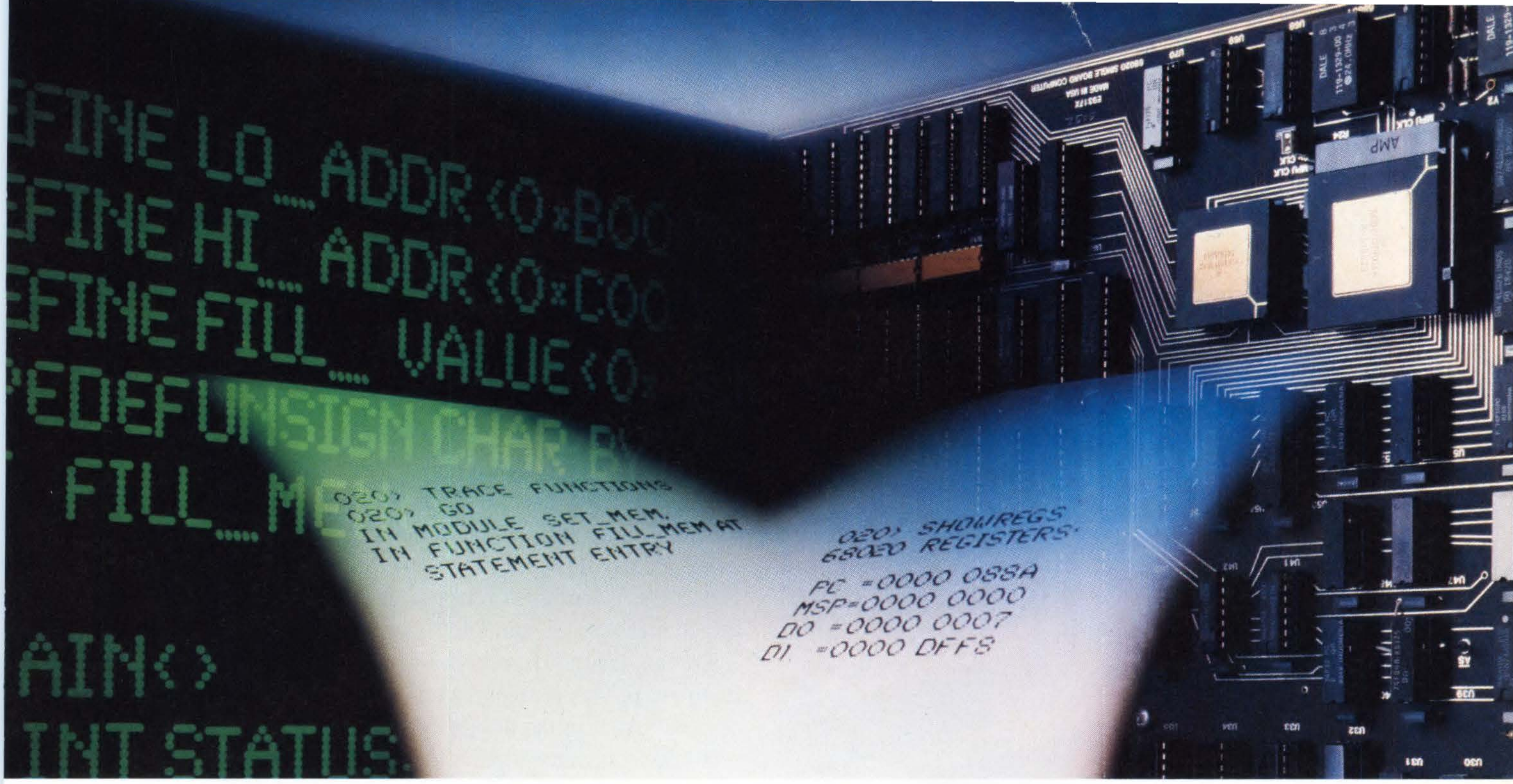
4. The Hypertronics Hypertac contact, which looks something like a Chinese finger puzzle, combines low insertion force with exceptional electrical and mechanical stability.

WHAT'S AHEAD?

Looking into the future, one trend is clear. Higher density packaging has resulted in closer pin spacing on connectors. If the number of contacts per inch is a measure of a connector's quality, the best LIF connector at present is Burndy's Surfmate, with 60 interconnection points per

Directory of ZIF and LIF connector manufacturers

Company	Model	Type	Maximum number of contacts	Center-to-center spacing (inches)	Insertion force (oz per pin)	Comments	Circle
Amp Inc. Harrisburg, PA 17105 (717) 564-0100	Amp ZIF	Card-edge	175 dual	0.100	0	Lever-activated	460
Bendix Connector Operations 40-60 Delaware St. Sidney, NY 13838 (607) 563-5324	Bristle Brunch Bunch (B3)	2-Piece	400	0.100	0.5	Brush contacts in pairs	461
Burndy Corp. Norwalk, CT 06586 (203) 852-8501	Ziflex	Card-edge	300	0.050	0	Surface-mounts or bolts to backplane	462
Hughes Aircraft Co. Connecting Devices Div. 17150 Von Karman Ave. Irvine, CA 92714 (714) 660-5701	Multipin LIF	2-piece	296	0.100	1.5		463
Hypertronics Corp. 16 Brent Dr. Hudson, MA 01749 (800) 225-9228	KA series	2-piece	320	0.100	2.0	Uses Hypertac contacts	464



NOW – A 68020 DEVELOPMENT SYSTEM FOR BOTH SOFTWARE AND HARDWARE ENGINEERS

Introducing Tek's 32-bit Multi-V Development System for the Motorola 68020 and Intel 80286: it makes the software engineer more productive without compromising the hardware engineer's needs. The next generation in microprocessor development, it is an integral part of Tek's Computer Aided Software Engineering (CASE) program, and offers Local Area Networking (LAN), real-time multi-emulation, 9 MB of program memory, "C" tools, integrated HLL debug, and much more.

Multi-V System is the software engineer's ideal development environment. Powerful C Language Development System (C-LANDS II) simplifies embedded microprocessor designs. An Integration Control System (ICS) transparently handles configuration management of prototype resources. The integrated debug system enables complex debug routines in both assembly and high level languages.

The Software Executer expands the software engineer's tools by providing a known good environment. Code runs at processor speeds with the productivity benefits of a development system. Floating point support (68881 or 80287) is standard with both software executer and emulator.

Multi-V is also the hardware engineer's ideal environment—with all the features you'd expect from Tektronix. Multiprocessor designs are easily handled by a high-speed trigger bus which ties real-time emulators together in one mainframe. For team development, multiple tools can reside in the same mainframe, and be accessed via RS-232 or LAN on any VAX™/MicroVAX™ system under ULTRIX™ or VMS™.

Multi-V—the preferred system for both software and hardware engineers—is integral to Tek's Computer Aided Software Engineering (CASE) program. This growing toolset cluster from Tek's Software Development Products Division demonstrates Tek's commitment to software technology. For more information, contact your Tek representative or call today: **1-800-342-5548.**

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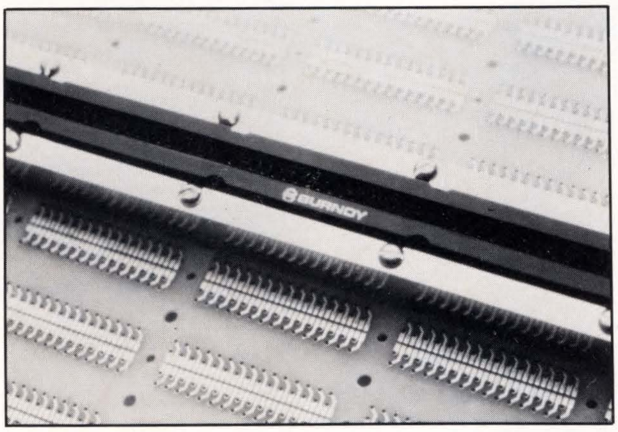
CIRCLE 105 FOR LITERATURE
CIRCLE 106 FOR SALES CONTACT

inch, in six rows with 100-mil spacing.

However, because the upper rows of contacts are set off from the board by a considerable distance, and are connected to it by simple right-angle conductors, the connector's high-frequency characteristics suffer. Even a four-row connector may have leads of approximately 1 in. with no impedance control.



5. Burndy's 300-contact Ziflex connector combines surface-mounting technology at the connector-backplane interface with ZIF technology at the interface of the card edge and its connector.

Burndy admits that a four-row version of the connector has already been rejected for some high-frequency applications. As users become more aware of the electrical effects of connectors' capacitances and inductances, and consequently demand more careful control of those parameters, introduction of connectors with controlled impedances seems bound to follow.

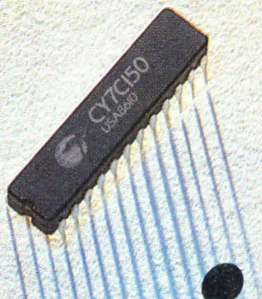
Design groups are becoming sensitive to the problems in choosing the best connector and are considering their options earlier in the design cycle. Whereas large companies have connector experts to guide the designer, smaller companies may find themselves at the manufacturer's mercy. Contech's Max Peel says: "If they had good luck with that supplier, they are probably going to believe what that supplier tells them. And then they make a commitment and hopefully are successful. In many cases they are not." Too often, by the time engineers spot a problem they are committed to a choice of connectors. The boards have already been designed.□

Directory of ZIF and LIF connector manufacturers (Cont'd.)

Company	Model	Type	Maximum number of contacts	Center-to-center spacing (inches)	Insertion force (oz per pin)	Comments	Circle
ITT Cannon 10550 Talbert Ave. P.O. Box 8040 Fountain Valley, CA 92728 (714) 964-7400	RDL series	Round 2-piece	82	0.100	0		465
Metcal Inc. 3704 Haven Ct. Menlo Park, CA 94025 (415) 366-3777	Self-soldering connector	1-piece	83	0.100	0	Self-soldering and -unsoldering; no normal force	466
Methode Electronics 7447 West Wilson Ave. Chicago, IL 60656 (312) 867-9600	MHD series	2-piece	516	0.100	1.5		467
Precision Connector Designs Inc. 5 Lowell Ave. Winchester, MA 01890 (617) 721-1280	PCD ZIF	Card-edge	65 dual	0.100	0	High normal force	468
Teradyne Connection Systems 44 Simon St. Nashua, NH 03060 (603) 889-5156	KS1025 series	Backplane	400	0.100	2.0		469

This is a representative sampling of suppliers; it is not meant to be a definitive list.

Our new, 1K × 4 static RAM.



0.8 micron CMOS shoves 4K SRAM speed down to 15ns, power down to 550mW, die size down to 6634 sq. mil, and

2.0 micron 1K × 4 SRAM, an industry standard, shown ≈ 4× larger than actual size. It goes 35ns.

shoves 2.0 micron IC competitors,

technically speaking, two years further behind.

Cypress Semiconductor. We've been shipping 1.2 micron CMOS in volume for two years. And now we have

1.2 micron Cypress Semiconductor 1K × 4 SRAM, also shown ≈ 4× larger than actual size, is smaller, runs faster, uses less power. It goes 25ns.

0.8 micron 1K × 4 SRAM, also shown ≈ 4× larger than actual size. Since we can't make electrons go any faster, we've shortened the distance they have to travel. Result: 15ns.

0.8 micron CMOS. The clear industry leader in getting small, fast . . .

Shielded Connections.

Metal Shell D-Subminiatures. Inexpensive, yet built to last.

Here's the inexpensive answer to effective shielding: Viking's new Metal Shell D-Subminiature Receptacles. They're U.L. listed and meet or exceed the most stringent EMI/RFI requirements – including FCC Docket No. 20780.

Consider the design: One-piece construction that eliminates the need for a support bracket. Open channels so impurities cannot be trapped. Rigid contact tails for ease of insertion. Generous lead-ins and chamfered edges to accommodate mismatching .

Consider the flexibility: Standard footprints. 9, 15, 25, 37 positions. More grounding methods. more mounting styles with either 4-40 UNC or metric threads. And your choice of two thicknesses of selective gold plating for reliable contact.

Consider the low price: Lower than competitive products. And still, it's a Viking connector – with the uncompromising reliability for which Viking is known. This reliability is the reason why major companies have included Viking in their accreditation, ship-to-stock, and Just-In-Time programs.

Prove it yourself. Send for complete specifications – and prices – today.

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Electronics and Defense Group
Viking Connectors Co.
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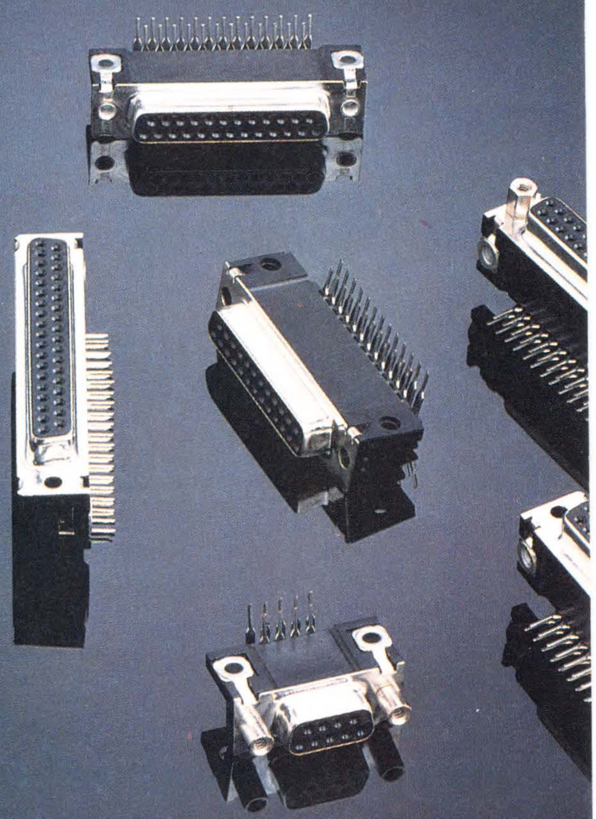
Chatsworth, CA 91311
(818) 341-4330
TWX: 910-494-2094



CIRCLE 110

NEW PRODUCTS

DIGITAL ICs

ELECTRONIC DESIGN EXCLUSIVE

Video and memory controller chips slash parts count for high-performance graphics

A graphic memory-interface chip (GMIC) teamed up with a video-attributes controller IC (GMVC) drastically reduces the number of components required to build a high-performance graphics controller. Both from the Semiconductor Division of Hitachi America, Ltd., the facile chips replace hundreds of TTL glue logic components. When used with the previously introduced Hitachi HD63484-8 advanced CRT controller (ACRTC), one GMIC and two GVACs—four chips—plus required RAM space are all you need to build a controller with 4-bit color and 640-by-400-pixel resolution.

The GMIC chip (the HD53485) comes in a 64-pin DIP (or 68-pin LCC). It serves as the interface between the graphics controller and the frame buffer of a bit-mapped display. While it derives its timing from the ACRTC (clock signals up to 64 MHz), the GMIC puts out all the row-and-column addresses, write strobes, and timing signals necessary to control a 2-Mbyte frame buffer built with high-speed dynamic RAMs. The current release of the GMIC chip controls dynamic RAMs with 250-ns cycle times. Future versions will control video RAMs.

The GMIC includes a clock divider circuit on chip that, in conjunction with the GVAC, allows the small incremental bit shifts needed to produce smooth panning, scrolling, and zooming on a CRT screen.

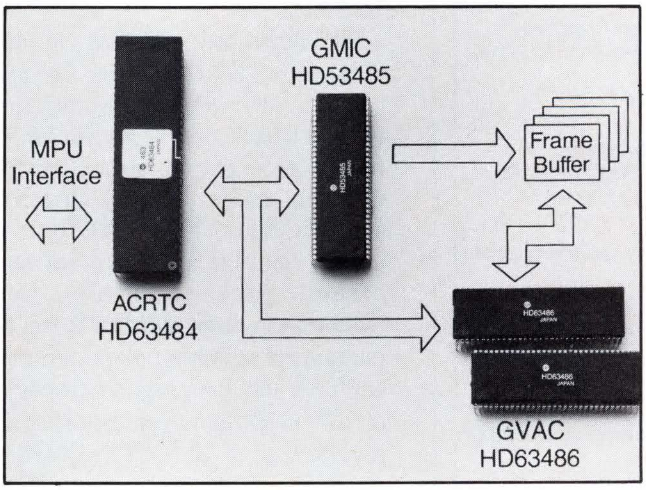
The GVAC (the HD63486) circuit is a 64-pin programmable device which regulates the transfer of data from the frame buffer to the video section of the display. It controls the number of color bits (up to 64k), as well as the dot shifts necessary to refresh the screen and produce smooth horizontal scrolling and zooming. Since each GVAC chip allows color attributes of up to 8 bits per pixel, two are required in parallel to provide full 16-bit color capability.

In addition to color control, the internal shift registers of the GVAC can be programmed for 8-, 16- or 32-bit horizontal dot shifters from frame buffer to screen. Since the chips run at 64-MHz clock rates, the usual reluctant trade-off between frame buffer refresh and fast screen paints is avoided.

The GMIC and GVAC parts are constructed with a combination of bipolar and CMOS processes yielding high packing densities and speed. All three chips in the set (the GMIC, GVAC, and the ACRTC) run about $50 in OEM quantities. Production quantities will be available in July.

Hitachi America, Ltd., Semiconductor and IC Division, 2210 O'Toole Ave., San Jose, CA 95131; James Fleury, (408) 435-8300.

CIRCLE 308



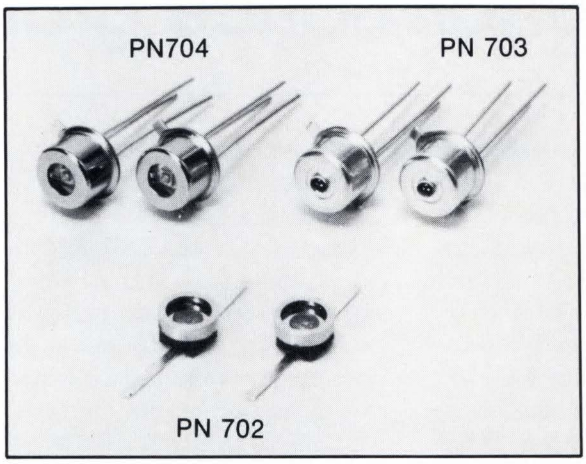
Stephan Ohr

NEW PRODUCTS

DIGITAL ICs

ELECTRONIC DESIGN EXCLUSIVE

P-i-n photodiodes keep dark current to 1 nA



Along with the lowest commercially available dark current—as little as 1 nA, typical—a family of p-i-n photodiodes also offers quantum efficiencies that reach 76%. The diodes, developed by Matsushita Electric, are intended for fiber-optic communication systems and have a spectral sensitivity that spans 900 to 1650 nm.

The three initial members in the family, the PN702, 703, and 704 all respond to the same light spectrum. However, each model comes in a different package and has a slightly different minimum dark current and efficiency. The PN702, for example, comes in a 4-mm diameter ceramic package, suitable for mounting in large hybrids. It has a guaranteed maximum dark current of 10 nA and a minimum efficiency of 70% (1300-nm operation with a reverse bias of 10 V). The PN703 comes in a TO-5 style leaded package that contains a miniature lens in the lid for more efficient light collection. It has the same maximum dark current, but a slightly lower minimum efficiency of 65%.

The third unit, the PN704, contains a much larger diode that has almost four times the active area as the previous two chips. Thus, it has a maximum dark current of 100 nA—ten times that of the other two diodes. The quantum efficiency (50% minimum) of the device is also lower.

All three diodes can operate over a −40 to +85°C range and have a cutoff frequency that extends to beyond 1 GHz. Biasing voltage for the trio can range up to 30 V, with the maximum forward current limited to 5 mA.

Prices for any of the diodes in sample quantities are the same: 20,000 yen apiece for 1 to 10 units; 15,000 yen for 11 to 99 units. Samples are available from stock.

Matsushita Electric Trading Co. Ltd., 3-15 Yagumo-Nakamachi, Moriguchi, Osaka 570 Japan; Jun Shibata, 06-909-1121.

CIRCLE 317

Dave Bursky

DIGITAL ICs

First CMOS HDLC chip debuts

The MV6001 EXP, developed by Plessey Semiconductor, is a high-level Data Link Controller (HDLC) transceiver. It was specifically designed to implement the data link level of layered protocols like ISDN and X.25. Furthermore, the chip serves as its own DMA controller, reading and writing data frames directly to memory.

Built using Plessey's CMOS MegaCell gate arrays, the 6001 consumes less than 250 mW. It is an implementation of the Data Link Control portion of the ISO's Open System Interconnection standard. As such it can handle bit-stream data packets or frames.

The chip will strip the frame from a received packet, which it picks up from the lower, physical layer. Similarly, it will build a transmission frame on request from the next higher network protocol layer.

The chip also acts as a DMA controller, transferring frame data directly to and from memory. As an aid to designers, it has a three-state interface to the system memory, allowing it to hook right up to a memory bus. It can handle frames up to 2000 kbytes long and is designed to operate with most popular types of microprocessors.

Frames may be transmitted or received at up to 64 kHz. The chip has an internal 8-MHz clock, but its transmitter and receiver both work with the external clock supplied by the frame communications link. Further, the device's transmitter and receiver can be tied together, allowing the host processor to test its own circuits with an external connection to a network.

The MV6001 EXP, housed in a 40-pin DIP, costs $17.25 each in lots of 1000. A ceramic package is available at $29.50 in the same quantity. Delivery is from stock.

Plessey Semiconductors, 3 Whatney, Irvine, CA 92718; (714) 951-5212.

CIRCLE 303

CMOS MAC speeds past bipolar parts

A 16-bit CMOS multiplier/accumulator, the LMA1043, is a direct replacement for the bipolar TRW TDC1043 and Weitek WTL 1043 but operates faster, with a worst-case processing time of 90 ns at 125 mW of power consumption. In military-specified environments, the LMA1043 performs multiplication/accumulation in 105 ns using 125 mW of power. The chip produces a 32-bit product for two 16-bit numbers and performs accumulation to full 35-bit precision. The accumulator performs full accumulation, subtraction, or rounding. The 19 most-significant accumulator bits are available at the output. Inputs and outputs are TTL-compatible.

Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, CA 94086; (408) 720-8630. $60 (plastic DIP) (100 units).

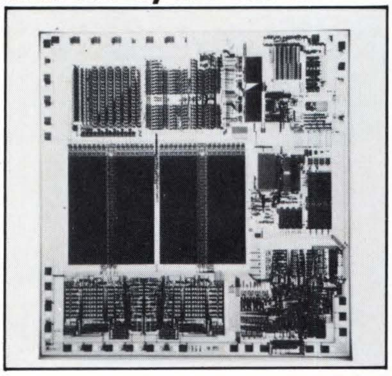
CIRCLE 325

CIRCLE 113

NEW PRODUCTS

DIGITAL ICs

DSP IC has 320-ns cycle time



Built with a 16/32-bit microprocessor architecture and instruction set optimized for voice-band digital signal processing, the DSP 128 integrated circuit offers an instruction cycle time of 320 ns. The device can be used as a stand-alone processor, cascaded on a common system bus, or interfaced with general-purpose microprocessors.

Stantel Components Inc., 636 Remington Rd., Schaumburg, IL 60195; (312) 490-7150. $88 (sample quantities).

CIRCLE 326

128k EPROM grabs data in 110 ns

With an access time of 110 ns, Intel's 27128B-110V05 128-kbit EPROM is 40 ns faster than the company's earlier 27128A-1, yet is functionally equivalent to standard 128-kbit EPROMs. By fabricating the 28-pin DIP device with its 1.2-μm HMOS II-E process, Intel was able to reduce the overall die size by 25%, thus reducing data access time and improving manufacturing yields. The device fits the standard JEDEC 28-pin site.

Intel Corp., Literature Department W-278, 3065 Bowers Ave., Santa Clara, CA 95051; (916) 351-2740. $13.30 (1000 units).

CIRCLE 327

1-Mbit EPROMs meet system needs

Three versions of a 1-Mbit EPROM are designed to meet varied application, performance, and upgrade requirements. The 32-pin 27010, 28-pin 27011, and 40-pin 27210 are manufactured in HMOS II-E, which yields access times of 200 and 150 ns.

Intel Corp., Department W-287, 3065 Bowers Ave., Santa Clara, CA 95051; (916) 351-2746. From $90 (1000 units).

CIRCLE 328

Advanced CMOS speeds logic

A family of advanced CMOS logic ICs, designated CD54/74AC/ACT, meets the needs of high-speed operation but at low power consumption. Propagation delay in ACL devices is typically just 3 ns. The parts are pin-compatible with 54/74HC devices for circuits that require the higher speed. The ICs are available in surface-mount packages, as well as in plastic and ceramic DIPs. Devices are offered for operation over the industrial and military temperature ranges.

RCA Corp., Solid State Division, Route 202, Somerville, NJ 08876; (201) 685-7460.

CIRCLE 329

NEW PRODUCTS

DIGITAL ICs

FIFOs boast 24-ns fall through

Two asynchronous 16-word FIFOs have a typical zero fall-through time of just 24 ns. Based on a dual-port RAM architecture that boosts speed by eliminating ripple-through delays, the SN54/74ALS232 and SN54/74ALS233 are approximately 50% faster than any other zero fall-through FIFO currently available. Despite their speed, the memory-storage devices require a relatively moderate supply current of 125 and 133 mA, respectively.

Texas Instruments Inc., Semiconductor Group, P.O. Box 809066, Dallas, TX 75360; (800) 232-3200. $20 in plastic DIP (100 units).

CIRCLE 330

Gate array cuts propagation delays

An 8000-gate array, designed using double-metal CMOS, offers an effective channel length of 1.3 μm. Although it uses 2-μm technology, its 1.1-ns typical internal gate propagation delay is comparable to 1.5-μm arrays. The VGC8000 has I/O buffers that contribute as much as a 10% increase in system performance over 1.5-μm arrays. A single I/O pin can drive high-capacitance, high loads directly without multiple I/O pads or external buffers.

VLSI Technology Inc., 1109 McKay Dr., San Jose, CA 95131; (408) 942-1810. $51.92 (1000 units).

CIRCLE 332

Shift register is 16 words deep

The Am29525, an 8-bit-wide, 16-word-deep microprogrammed shift register, replaces four Am29520 pipeline registers in applications that require hold, shift, or load instructions. In addition to a 70% space savings, the shift register also lowers power consumption to 1.6 W. The device's 24-mA current output drive allows the data port to be connected directly to the system bus. Both a 21-ns commercial and military version are available.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, CA 94088; (408) 982-7448. $21.95 for commercial version (100 units).

CIRCLE 333

5-V CMOS EEPROM stores 256 bits

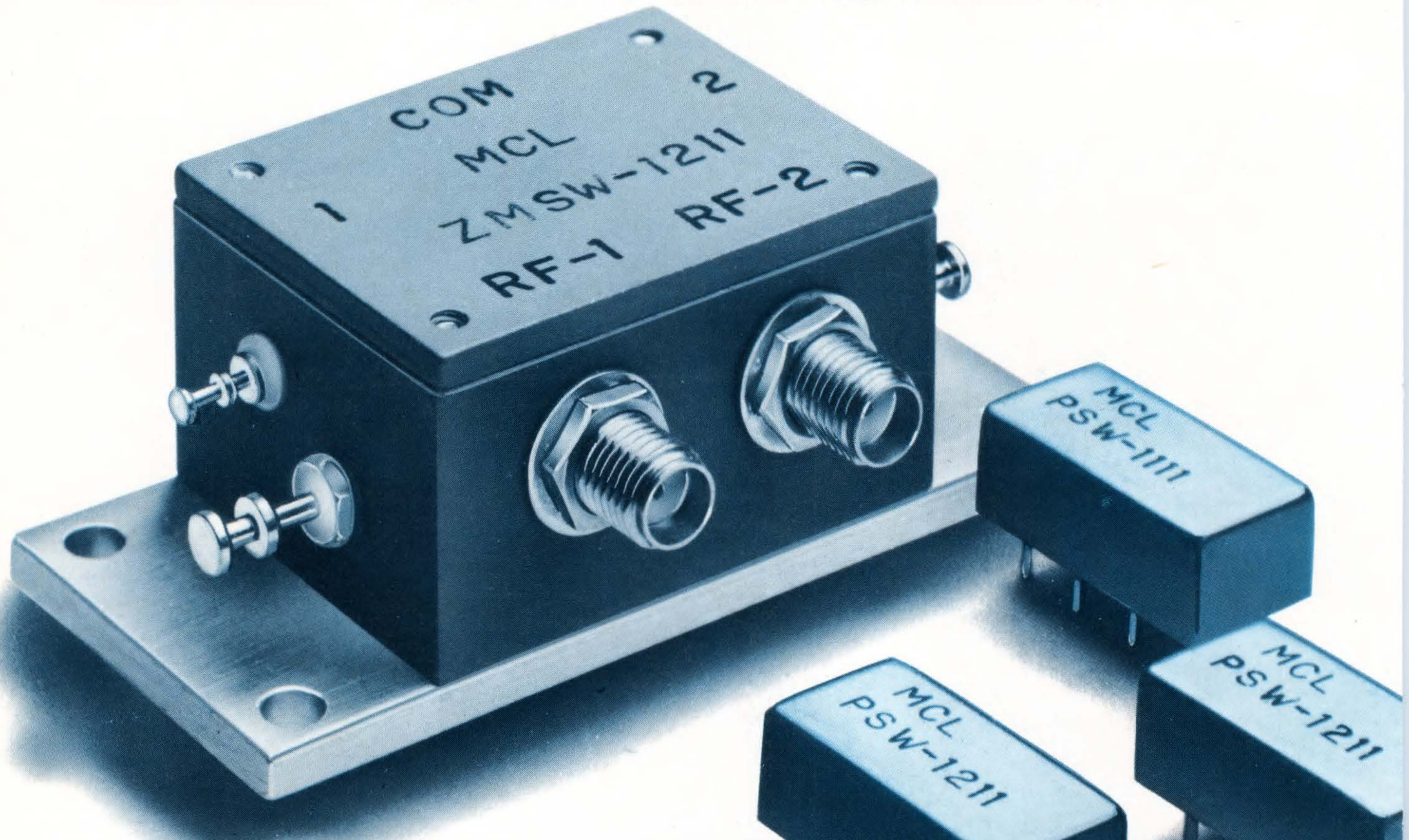
An electrically erasable PROM, the 28C256, stores up to 256 kbits. The CMOS part uses 1.25-μm technology and requires a single 5-V supply. It has a page-write mode that affords a 160-μs effective write time for a 64-byte page. In the byte-write mode, the speed is 2.5 ms/byte.

The IC also offers data polling to minimize the writing time by signaling the actual end-point of a write cycle. The chip also features automatic byte-erase-before-write and an on-chip timer and internal latches to free the microcomputer system for other tasks during writing. The chip comes in a 28-pin ceramic DIP or a 32-pin leadless chip carrier.

Seeq Technology Inc., 1849 Fortune Dr., San Jose, CA 95131; (408) 942-1990. $195 (100 units).

CIRCLE 331

RF switches



10 to 2500 MHz from $19.95 PSW 1211 (500 qty.)

Now, for your wideband systems design, under —$20.00 SPST and SPDT pin diode switches that operate over the 10 to 2500 MHz range with less than 1 dB (typ.) insertion loss at 1000 MHz, 1.5 dB at 2500 MHz.

No waiting, immediate delivery . . . with one year guarantee. Call or write for our catalog or see our catalog in the Gold Book, EBG, EEM or Microwaves Product Data Directory.

SPECIFICATIONS for
PSW 1111 (SPST) **and PSW 1211** (SPDT)
ZMSW 1111 and ZMSW 1211

FREQUENCY RANGE	10-2500 MHz
INSERTION LOSS	
10-2000 MHz	1.7 dB max.
2000-2500 MHz	2.7 dB max.
ISOLATION	
10-500 MHz	40 dB min.
500-1000 MHz	30 dB min.
1000-2000 MHz	25 dB min.
2000-2500 MHz	20 dB min.
SWR	1.5 max. ("on" state)
SWITCHING SPEED	1 μsec. (max.)
MAXIMUM RF INPUT	+20 dBm
CONTROL	+5 V (5 mA max.)
OPERATING TEMPERATURE	−54°C to +100°C
STORAGE TEMPERATURE	−54°C to +100°C

PRICE (6-24) (1-4)

PSW 1111	$29.95	ZMSW 1111	$59.95
PSW 1211	$29.95	ZMSW 1211	$59.95

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CIRCLE 116

Introducing the LH Research SM Series, a line of fully regulated, 750 to 1500 watt, switching power supplies.

Simon says: *"Call my guardian angel Joyce for price quotations on larger quantity orders."*

**23 models, 1 to 4 outputs, up to 28V, up to 300 amps.
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MODEL NUMBER	WATTS OUT	OUTPUTS* MAIN VDC/AMPS	2 VDC/AMPS	3 VDC/AMPS	4 VDC/AMPS	CASE SIZE	QUANTITY PRICING 1-9	10-49	50-99	100
SM71-1	750	5 @ 150				1	**$ 680**	**$ 610**	**$ 590**	**$ 565**
SM71-2	750	12 @ 62				1	**680**	**610**	**590**	**565**
SM71-3	750	15 @ 50				1	**680**	**610**	**590**	**565**
SM71-5	750	24 @ 32				1	**680**	**610**	**590**	**565**
SM71-6	750	28 @ 27				1	**680**	**610**	**590**	**565**
SM11-1	1000	5 @ 200				1	**750**	**675**	**655**	**625**
SM11-2	1000	12 @ 84				1	**750**	**675**	**655**	**625**
SM11-3	1000	15 @ 67				1	**750**	**675**	**655**	**625**
SM11-5	1000	24 @ 42				1	**750**	**675**	**655**	**625**
SM11-6	1000	28 @ 36				1	**750**	**675**	**655**	**625**
SM23-122	1000	5 @ 150	12 @ 10	12 @ 10		2	**1120**	**1020**	**980**	**935**
SM23-133	1000	5 @ 150	15 @ 10	15 @ 10		2	**1120**	**1020**	**980**	**935**
SMX23-122	1000	5 @ 150	12 @ 18	12 @ 5		2	**1160**	**1055**	**1015**	**970**
SM24-1221	1000	5 @ 150	12 @ 10	12 @ 10	5 @ 5	2	**1200**	**1090**	**1050**	**1000**
SM24-1122	1000	5 @ 150	5 @ 10	12 @ 10	12 @ 5	2	**1200**	**1090**	**1050**	**1000**
SM24-1225	1000	5 @ 150	12 @ 10	12 @ 10	24 @ 3	2	**1200**	**1090**	**1050**	**1000**
SM24-1133	1000	5 @ 150	5 @ 10	15 @ 10	15 @ 5	2	**1200**	**1090**	**1050**	**1000**
SM24-1335	1000	5 @ 150	15 @ 10	15 @ 10	24 @ 3	2	**1200**	**1090**	**1050**	**1000**
SM81-1	1500	5 @ 300				3	**1295**	**1175**	**1130**	**1085**
SM81-2	1500	12 @ 126				3	**1295**	**1175**	**1130**	**1085**
SM81-3	1500	15 @ 100				3	**1295**	**1175**	**1130**	**1085**
SM81-5	1500	24 @ 63				3	**1295**	**1175**	**1130**	**1085**
SM81-6	1500	28 @ 54				3	**1295**	**1175**	**1130**	**1085**

CAUTION: Total loading of all outputs not to exceed rated output power. Prices subject to change without notice.
*Many additional standard voltage/current output combinations are available; refer to 1985 General Catalog or contact factory.

Ordering Information (Typical part number encoded)

SMX 2 3 1 2Y 2Y / 115-230

Series — SMX
Model* — 2 3
Output V1 (table 1) — 1
Output V2 (table 1) — 2Y
Output V3 (table 1) — 2Y
Output V4 (table 1)
Input Voltage (115/230VAC) — 115-230

OPTIONS 400 Hz input voltage: use 115-400Hz.
EMI: Add letter A after input voltage code (not available on SM81).
Sequencing (3 to 4 output models only): Add letter B after input voltage code.
OVP (aux. output): add letter Y after auxiliary output voltage code.
*Last Digit = number of outputs.

Table 1	
0 = 2VDC	4 = 18VDC
1 = 5VDC	5 = 24VDC
2 = 12VDC	6 = 28VDC
3 = 15VDC	8 = 48VDC

Options for SM Series

DELIVERY
SM Series switching power supplies with OVP options are shipped within 48 hours after placement of your order. All other options require 3-4 weeks.

OPTIONS	QUANTITY 1*
115V, 400Hz input	$160.00
OVP on auxiliary outputs	
1 auxiliary output	22.00
2 auxiliary outputs	44.00
3 auxiliary outputs	66.00
Crowbar OVP on mainframe (SM81 only)	33.00
EMI filter to meet VDE 0871, Curve "A" and FCC Docket 20780, Curve "A" (not available on SM81)	44.00
Sequencing (only 3 & 4 output models)	28.00

*For multiple unit pricing, contact factory.

Product Specifications

OUTPUT POWER
750 to 1500 Watts maximum.

OUTPUT VOLTAGES
2, 5, 12, 15, 18, 24, 28VDC. 48VDC available on some models; contact factory.

OUTPUT CURRENT
See specific model.

NUMBER OF OUTPUTS
1 to 4.

COOLING
Fan.

INPUT VOLTAGE
92-132VAC or 184-264VAC (user selectable at front panel), 47-63Hz.

HOLD-UP TIME
20msec in regulation minimum, after removal of nominal AC input. SM81 only—35msec.

LINE REGULATION
0.4% over entire input range for all outputs.

LOAD REGULATION
0.4% from no load to full load for all outputs.

INTERACTION (CROSS REGULATION)
0.1% maximum.

PARD (RIPPLE & NOISE)
1%p-p or 50mV, whichever is higher.

CURRENT SHARE
(SM81 only). Special circuitry to ensure balanced loading when paralleling power supplies.

CURRENT MONITOR
2V analog for mainframe output. (Not available on SM81).

EFFICIENCY
Up to 80%; 70% typical.

POWER FAIL DETECTION
Upon removal of AC, the power fail signal drops to logic zero at least 2msec before loss of DC output. Upon AC turn-on, signal remains low until outputs are in regulation.

OVERVOLTAGE PROTECTION
Standard on V1. Factory set for 125% ± 5%. Optional on auxiliary outputs.

CURRENT LIMIT
All outputs have fold-back current limiting to less than 50% of full load rating under short-circuit.

REVERSE VOLTAGE PROTECTION
To 100% of rated current for main output(s).

OVERTEMPERATURE PROTECTION
Internal thermal switch turns off power supply if overheating occurs.

OVERSHOOT & UNDERSHOOT
2% maximum deviation with a load change of 25% at 5A/μsec. No overshoot or undershoot during AC turn-on or turn-off.

RESPONSE TIME
200μsec to within 1% after a 25% load change at 5A/μsec.

TEMPERATURE COEFFICIENT
±0.02%/°C from 0°C to 50°C after half hour warm-up.

OPERATING TEMPERATURE
0°C to 70°C, full power to 50°C; derates linearly to 60% power at 70°C. SM81 only—full power to 40°C; derates linearly to 50% power at 70°C.

STORAGE TEMPERATURE
−55°C to 85°C.

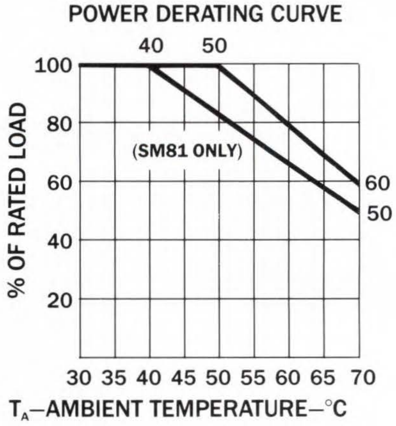
VOLTAGE ADJUST RANGE
±5% minimum, all outputs.

MINIMUM LOAD
Zero for single output models. 17% required on V1 of multiple output models to insure regulation of auxiliary outputs. Contact factory for minimum load if main output is other than 5V. Lack of minimum load will not damage supply.

OUTPUT POLARITY
All outputs are floating and may be referenced to each other or chassis ground as required. Outputs may be isolated up to 100 volts from chassis ground.

LIMITED INRUSH CURRENT
The AC input inrush current is limited to 60A rms when averaged over one cycle. SM81-62A rms.

REMOTE ON/OFF
The power supply is turned on with open circuit or TTL logic '1', and turned off by switch closure or TTL logic '0'.



REMOTE SENSE
Standard on main outputs and auxiliary outputs having 5V current rating of 10A or greater. Compensates for up to 250mV of total lead cable loss. All outputs are internally sensed if the sense leads are opened.

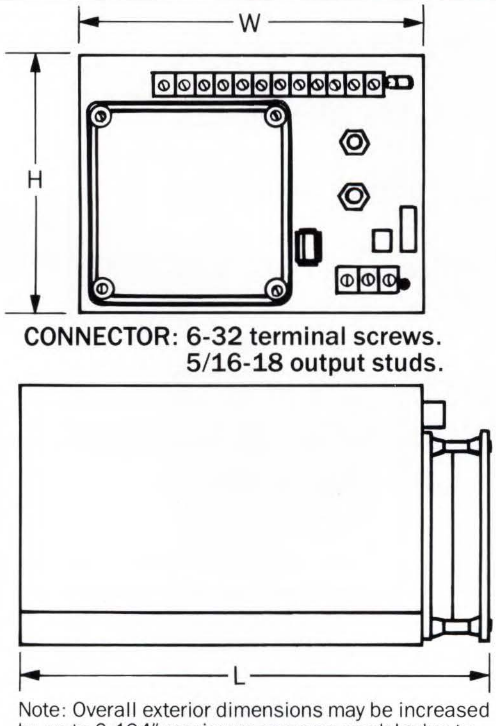
MARGINING
Remote high and low margin is ±7% of nominal for main output (except for 2V main output). SM81: ±5%.

DC 'OK' SIGNAL (SM81 ONLY)
When output is within ±5% of normal, signal is high. When output exceeds ±5%, signal goes low.

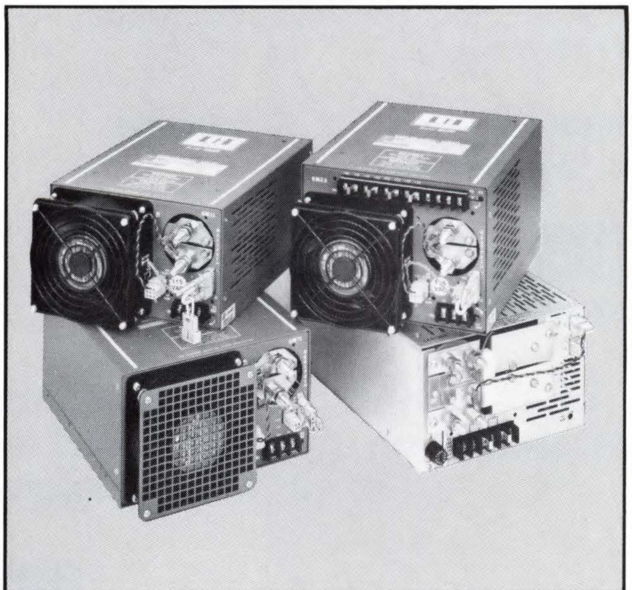
OVP ACTIVATED SIGNAL
When OVP activates, the signal goes low. (SM81 only).

SAFETY
UL recognized. CSA certified.

OPTIONS
EMI filtering (except SM81). Meets VDE 0871, Curve "A" and FCC Docket 20780, Curve "A".
Sequencing
400Hz input.



Note: Overall exterior dimensions may be increased by up to 0.194" maximum on some models due to possible protrusion of hardware.



DIMENSIONS (in./cm.)			
Case Size	L	W	H
1	11.00/27.94	8.00/20.32	5.00/12.70
2	11.00/27.94	8.00/20.32	6.00/15.24
3	15.50/39.37	8.00/20.32	5.00/12.70

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SMD Availability Chart

P/N	Current (A)	Voltage (V)	Trr	Package
General Purpose				
GL34A-M	0.5	50-1000	—	GL34
1N6478-84	1.0	50-1000	—	GL41
GL41A-M	1.0	50-1000	—	GL41
GL27A-M	3.0	50-1000	—	GL27
Fast Recovery				
RGL34A-M	0.5	50-1000	150-500	GL34
RGL41A-M	1.0	50-1000	150-500	GL41
RGL27A-M	3.0	50-1000	150-500	GL27
Ultra Fast Recovery				
EGL41A-G	1.0	50-400	50	GL41
EGL27A-G	3.0	50-400	50	GL27
Schottky				
SGL34*	0.5	20-80	—	GL34
SGL41*	1.0	20-80	—	GL41
Zener				
ZGL34*	0.5 (W)	6.8-200	—	GL34
ZGL41	1.0 (W)	6.8-200	—	GL41
ZGL27	3.0 (W)	6.8-400	—	GL27
Transient Voltage Suppressor				
TGL41*	400 (W)	6.8-200	—	GL41
TGL27*	1500 (W)	6.8-400	—	GL27

*Consult factory for availability.

GENERAL INSTRUMENT

CIRCLE 181

ANALOG

ELECTRONIC DESIGN EXCLUSIVE

Multiplexer moves charge on each element of infrared array to output

For the first time, designers of systems incorporating multi-element infrared detector arrays can obtain off-the-shelf PMOS multiplexer chips that accept parallel inputs and deliver a serial output. That is, the multiplexer sequentially transfers the charge (signal) on each element of the array to a single video output. These devices offer several advantages over the prevalent custom CCD approach. From EG & G Reticon, the M series of multiplexers contains five basic models: RL0032M, RL0064M, RL0128M, RL0256M and RA0128M.

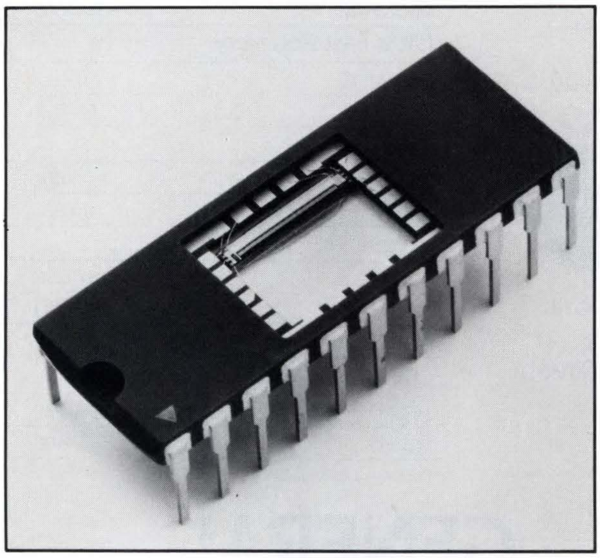
The first four models handle linear arrays containing 32, 64, 128, or 256 energy sensing elements. The fifth handles area arrays containing 128 × 128 elements.

Frank Goodenough

The multiplexers can operate with signals from arrays fabricated with all the common materials, including silicon, indium antimonide, mercury cadmium telluride, and platinum silicide. Moreover, they handle silicon sensors working in the near infrared and pyroelectric sensors operating over broad bands.

CCD type devices can also do the job, but they are custom devices, and the PMOS multiplexers are not only off-the-shelf, they offer several performance "breaks." First, charge-transfer efficiency, even after many scans, remains high.

Second, unlike CCDs, the PMOS versions avoid contributing fixed pattern noise to the output. This noise appears as annoying, often confusing, interference patterns on a CRT display. Third, the multiplexers handle a greater range of charge without saturating than CCDs. Thus accuracy is maintained over a wider range of signal amplitudes. Finally, the multiplexers cost significantly less.



The multiplexers are available in chip form or in an unlidded ceramic DIP with space left for mounting the sensor (see photo). Each input of the multiplexer is wire-bonded to a separate sensor element bonding pad. The chips are available for both left-side and right-side (mirror image) mounting when needed for interdigitated applications. When used in this manner, the sensor is mounted between a pair of multiplexers, and sensor elements are alternately connected to the left- and right-hand multiplexer.

The chips require a two-phase clock between 2 or 3 and 7 MHz. The device's dummy video output is subtracted (off-chip) from the signal video output to cancel fixed-pattern noise.

In quantities of one to five, the M series of multiplexers goes for $125, $150, $300, and $600 each for the 32, 64, 128, and 256-channel linear devices. The RA0256M area array multiplexer is $3500 in similar quantities. Small quantities are available from stock.

EG & G Reticon, 345 Potero Ave., Sunnyvale, CA 94086; Bob Maddoux, (408) 738-4266.

CIRCLE 311

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CIRCLE 104

3M

ELECTRONIC DESIGN EXCLUSIVE

25-MHz, 10-bit ADC runs at any encode rate

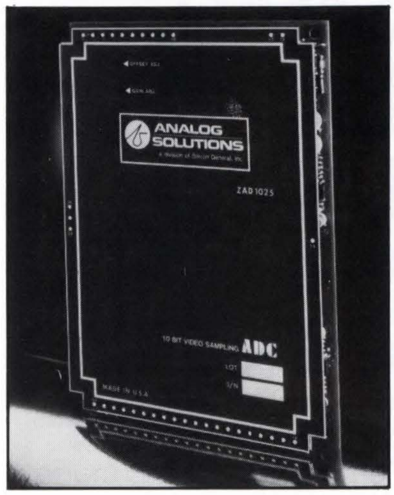
Not everyone needs a 10-bit analog-to-digital converter that can sample at a 25-MHz rate—and do it with 10-bit accuracy as well. However, for radar or imaging systems even those top specs may not be enough in themselves. On top of those, it would be quite advantageous to operate over a range of encoding, or sampling, rates, and as wide a range as possible. Ideally, the ADC should sample from dc to its top encode rate. The ZAD1025 from Analog Solutions does just that, all the way to 25 MHz.

On the other hand, previous converters (in what is becoming an industry standard configuration) require the user to specify a sampling rate falling between 50% and 100% of maximum. Full accuracy is then guaranteed within ±12% of the specified rate. However, earlier converters, when specified at half the maximum rate, can still operate down to dc and provide 10-bit-accurate data.

The wide encoding range of the ZAD1025 not only permits operation in many different types of systems (thus simplifying ordering and stocking), it permits the system of which it is part of to be tested at various speeds.

Even better, the ZAD1025 is also 25% faster than available converters and, at $2100 each in quantities of 100, costs less than others (for instance, a 40-MHz competitive device is available at twice the cost).

Like most sampling converters, the 1025 has dynamic characteristics aimed at digitizing a single, complex, video-band signal.



For example, at dc, there are no missing codes and integral linearity is ±1 LSB—both guaranteed—but ac linearity is specified too—in terms of spurious in-band signals. For inputs between dc and 1 MHz, spurious signals run at least 60 dB below full scale; between 1 and 5 MHz, 55 dB below full scale; and between 5 and 25 MHz, 50 dB below full scale.

Aperture time and uncertainty are a maximum of 5 ns and 10 ps, respectively. The converter's input bandwidth is flat (±0.2 dB) from dc to 12.5 MHz. Full-scale and small-signal bandwidths (40 dB below full scale) are 16 and 25 MHz, respectively; and both transient response and overload recovery are under 50 ns. Delivery is from stock to four weeks.

Analog Solutions, 940 Detroit Ave., Concord, CA 94518; (415) 686-6660.

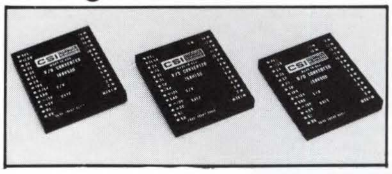
CIRCLE 309

Frank Goodenough

NEW PRODUCTS

ANALOG

RDCs boost accuracy at high speeds

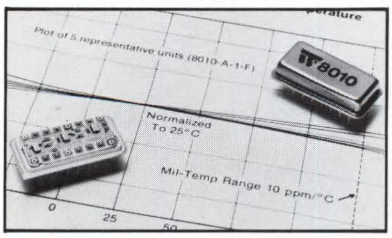


A family of 14-, 15-, and 16-bit resolver-to-digital converters offers good accuracy at high speeds. Accuracy versus velocity is ±1.0 minute at 8.3 revolutions/s for the Model 168H800, ±1.3 minutes at 16.7 revolutions/s for the 168H700, and ±2.0 minutes at 33.3 revolutions/s for the 168H600. The reference frequency is 400 to 2600 Hz. Standard input voltage is 2.5 V line to line, however units can be customized for any voltage from 2.5 to 11.8 V rms at no additional cost.

Control Sciences Inc., 9509 Vassar Ave., Chatsworth, CA 91311; (818) 709-5510. $395; 4 to 10 weeks.

CIRCLE 334

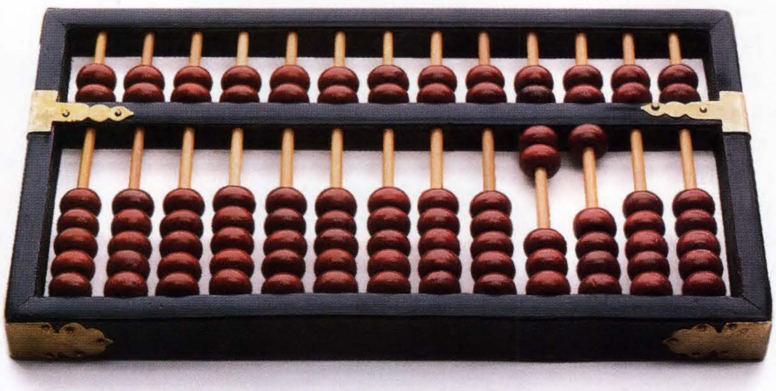
Voltage references remain stable



Dual-tracking voltage references, the 8010/8011 series, offer temperature coefficients as low as 10 ppm/°C for operation in severe environments with temperatures from −55° to +200°C. Absolute voltage tolerance ranges from 10% down to 0.1%. All standard units provide a voltage match between outputs of better than 0.2%. Tracking outputs are fully buffered; typical noise is just 1 μV pk-pk. The input range for both reference devices is ±12 V to ±18 V with a dc power supply rejection ratio of less than −100 dB. The maximum supply current requirement ranges from ±14 to ±18 mA.

White Technology Inc., 4246 E. Wood St., Phoenix, AZ 85040; (602) 437-1520. From $140 (100 units); stock to four weeks.

CIRCLE 335



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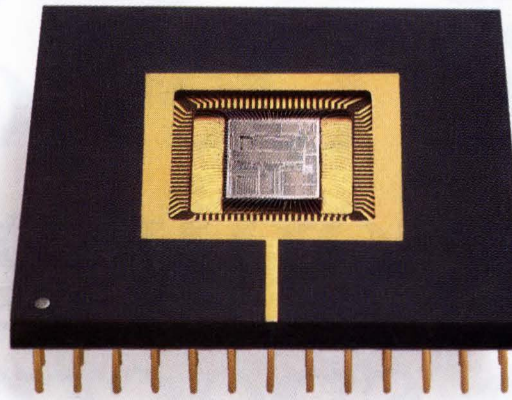

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For more details, see our ads on the following pages.

ANALOG DEVICES

CIRCLE 120

In DSP and high performance arithmetic circuits, Logic Devices is broadening the CMOS spectrum.

MULTIPLIERS				
Part No.	Type	Max. Multiply Time (ns)	Power (mW)	Equivalent
LMU08/8U	8 x 8 signed & unsigned	50	40	MPY8HJ, MPY8UHJ
LMU557/558	8 x 8 mixed	60	70	25S557/8
LMU12	12 x 12	65	100	MPY12HJ
LMU13	12 x 12 microprogrammable	65	100	–
LMU16	16 x 16	80	125	MPY16HJ; AM29516
LMU17	16 x 16 microprogrammable	80	125	AM29517
LMU18	16 x 16 32-bit output	80	150	–
MULTIPLIER-ACCUMULATORS				
Part No.	Type	Max. Multi-Accum Time (ns)	Power (mW)	Equivalent
LMA1009	12 x 12	65	100	TDC1009
LMA1010	16 x 16	90	100	TDC1010
LMA1043	16 x 16	90	100	TDC1043
PIPELINE REGISTERS				
Part No.	Type	Max. Access Time (ns)	Power (mW)	Equivalent
L29C520/521	4 x 8 bit	22	50	AM29520/521
LPR520/21	4 x 16 bit	22	50	two AM29520/521
MULTIPORT REGISTER FILES				
Part No.	Type	Max. Access Time (ns)	Power (mW)	Equivalent
LRF07	3 independent port, 8 x 8	35	40	–
LRF08	5 independent port, 8 x 8	35	60	–
ARITHMETIC LOGIC UNITS				
Part No.	Type	Min. Cycle Time (ns)	Power (mW)	Equivalent
L429C01	16-bit slice	90	150	Quad 2901 or 2901D
L4C381	16-bit adder/subtractor	34	75	Quad 54/74S381
SPECIAL-FUNCTION CIRCUITS				
Part No.	Type	Performance	Power (mW)	Equivalent
LSH32	32-bit barrel shifter	35 ns prop. delay	60	–
L10C23	64-bit digital correlator	35 MHz data rate	125	TDC1023J

No matter where your product falls in the high-performance end of the design spectrum, Logic Devices has you covered. For digital signal processing, graphics, image processing, real-time and high-speed computing, our family of high performance CMOS building blocks works together smoothly. Its clean architectures give you the kind of elegant solutions you need. Especially where throughput, physical size and cost are the critical issues.

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NEW PRODUCTS

ANALOG

Buffer amplifier drives coaxial lines

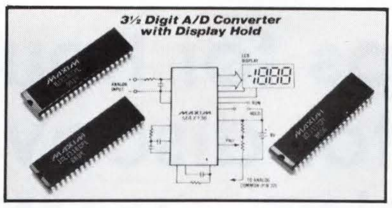
A unity-gain buffer amplifier, suitable for voltage-follower/buffer applications, drives coaxial cable with high current at frequencies from dc to 300 MHz. The BB3553 drives loads as low as 50 Ω and provides output drive of up to 400 mA. The design includes JFET input followers that show bias current of just 200 pA at 25°C. The slew rate is 6000 V/μs. The input resistance is guaranteed to be a minimum of 10^{10} Ω, and the output impedance is likewise guaranteed to be 4 Ω. Electrostatic discharge protection exceeds 2000 V. The Maxim device is the only second-source for the Burr-Brown BB3553.

Maxim Integrated Products, 510 N. Pastoria Ave., Sunnyvale, CA 94086; (408) 737-7600. $23 (100 units); stock.

CIRCLE 336

Low-power ADC drives LCD

An integrating analog-to-digital converter, the MAX136, drives a 3½ digit LCD. The CMOS device, which includes a data-hold function, operates for 8000 hours from a 9-V battery. An auto-zeroing technique shows almost no zero-offset nor common-mode rejection errors. The

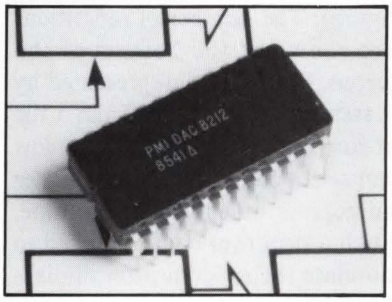


part is compatible with the industry standard ICL7116 but uses 80 μA, 10 times less supply current. Its common-mode rejection ratio is also reduced, typically just 5μV/V.

Maxim Integrated Products, 510 N Pastoria Ave., Sunnyvale, CA 94086; (408) 737-7600. $5.54 (DIP), $7.14 (chip carrier); stock.

CIRCLE 337

12-bit ADC mates with processors



A dual 12-bit multiplying analog-to-digital converter, the DAC-8212, uses internal latches for easy interfacing with microprocessors. The CMOS device accepts a 12-bit word in a single byte. It consists of two thin-film R-2R resistor ladder networks, two 12-bit latches, a 12-bit input buffer, and control logic. Operation is from a single supply of 5 to 15 V dc. Maximum dissipation with a 5-V supply is 0.5 mW.

Precision Monolithics Inc., 1500 Space Park Dr., P.O. Box 58020, Santa Clara, CA 95052-8020; (408) 727-9222. $15.26 (commercial grade), $21.15 (industrial grade), $72.00 (military grade) (100 units); stock.

CIRCLE 338

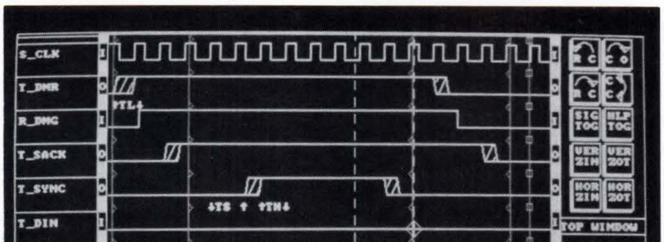
ELECTRONIC DESIGN EXCLUSIVE

Testing chips for hours lets simulator discover hidden design errors

A custom-chip simulator permits gate arrays, standard cells, and other homemade chips to be run for hours instead of seconds, hence uncovering more design flaws before production begins. The IKOS 800, from IKOS Systems, also outdoes other simulators on the software front, helping a designer create waveforms to exercise chip models. The same software also creates pictures of what the resulting waveforms should look like. A software logic analyzer compares the actual output waveforms with the desired waveforms and triggers on discrepancies down to 1 ns.

Curtis Panasuk

Instead of building the stimulus waveforms by typing in ones and zeros, the engineer can "paint" the input waveforms as well as the expected results with a mouse and an IBM PC AT. The system makes it easy to create complex waveforms: vertical lines are simply superimposed over the parts of the waveform that are to be repeated (see the figure). The number of repetitions are shown at the bottom of the screen. Data values, represented by <ssssssss>, are loaded from a file at run time. A highlighted window can select edges that will be under microprogram control at run time. Such a program could be used to simulate the random jitter of disk-drive data edges.



Employing a mouse, a user "paints" the waveform to be applied to the chip model and also paints the expected output waveform. Vertical lines are placed around waveform sections to be repeated.

Coding the waveforms into vectors would consume excessive disk space and hinder quick delivery. Thus waveforms are coded into the type of program that runs on a stimulus board. Up to four of these programs can be loaded at a time, so that four waveform channels may be applied simultaneously. A disk controller would require three such channels to simulate activity on the bus interface, the microprocessor connection, and the actual link to the disk. The stimulator board uses bit slice components and 4 Mbytes of memory (expandable to 16 Mbytes) to generate waveforms, insert data values, and apply them to the simulator. A 5-Mbit proprietary bus connects the stimulus board to the host.

The basic simulator can run 16,000 four-input, one-output primitive logic elements at 500,000 events a second. Adding three expansion boards enables the system to run up to 64,000 primitives at 2 million events a second. Further, in the unit-delay mode, a single delay value is used for all gates, boosting the number of events per second tenfold.

The IKOS 800 simulator will be shipped at the end of July. It is priced at $40,000.

IKOS Systems Inc., 1220 Crossman Ave., Sunnyvale, CA 94089; Charles Cump, (408) 734-5211.

CIRCLE 305

NEW PRODUCTS

INSTRUMENTS

VLSI test system handles 512 I/Os

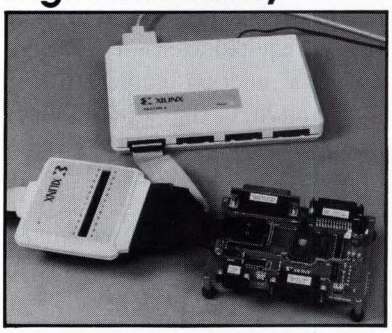
One of the first VLSI test systems to handle up to 512 I/O pins, the DIC-9035 can run those pins at speeds of up to 50 or 100 MHz. A maximum configuration of two test stations can be supported by the system, and timing measurements can be made with accuracies to within ± 500 ps.

Three versions of the system are available: A general-purpose model with a 12-V pk-pk driver swing; a bipolar version optimized for testing ECL-TTL chips with a comparative level range of −3 to +5 V and driver voltages that can be varied by 2.5 V pk-pk; and the last model, which is optimized for CMOS, offers test heads with input capacitances of 30 pF or less.

Ando Corp., 480 Oakmead Pkwy., Sunnyvale, CA 94086; (408) 738-2636. Systems will be available in the fourth quarter.

CIRCLE 339

First ICE for logic cell array



Able to cut the pattern development debugging time on the Xilinx logic cell array from several weeks to as little as a few hours, the XC-DS 24 in-circuit emulator allows new patterns to be evaluated in just a few keystrokes and a dozen milliseconds. The ICE system is the first such tool to support a programmable logic chip, and it takes advantage of special features embedded in the Xilinx XC-2064 array so that the condition of every logic cell can be observed.

When used in conjunction with the XACT design editor, the in-circuit emulator module and pod tie into an IBM PC AT, XT, or look-alike. The module connects to the computer via an RS-232-C serial port, and up to four pods can plug into the ICE. The dynamic status of all the cells in the chip can be read back, thus permitting evaluation of the instantaneous state of the chip.

Xilinx Inc., 2069 Hamilton Ave., San Jose, CA 95125; (408) 559-7778. $6300 (ICE module and one pod); additional pods cost $850.

CIRCLE 340

Scope includes sine interpolation

A dual-channel storage oscilloscope, the DSS 5040, includes sine interpolation capability. The portable analog/digital unit offers a 10-MHz single-occurrence capture capability. Function selection controls are identical to those of an analog scope. Built-in circuitry eliminates the multi-step function-select sequence common to other storage scopes. The scope captures signals with rise times of up to 64 ns in the pulse interpolation mode. Other features include automatic focusing and a 100× expansion mode. Both channels have 1 kbyte of memory.

Kikusui International Corp., 17819 S. Figueroa St., Gardena, CA 90248; (213) 515-6432.

CIRCLE 341

POWER

ELECTRONIC DESIGN EXCLUSIVE

Triple-output regulator powers and monitors 5-V microprocessor systems

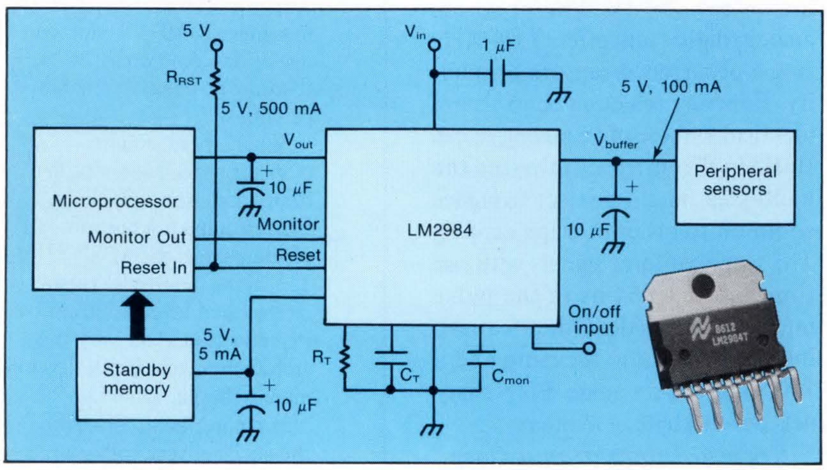
Most linear regulators just sit there and do their simple job. A few go further, providing dual outputs or indicating when they drop out of regulation. Not to be upstaged, National Semiconductor Corp.'s LM2984C Microprocessor Power Supply System does all that and still more—it monitors the system processor it powers and flags malfunctions, such as getting stuck in a loop or latchup.

For its main job, the chip provides three independent 5-V (±3%) outputs. The main output (500 mA) powers the microprocessor; a 100-mA buffer output powers peripherals such as sensors; and a 5-mA tap powers standby memory.

Designed to run from a nominal 14-V rail, the chip's low dropout circuits permit operation at rated load with just 600 mV between rail and output. The chip also runs continuously from a 26-V line and survives a 1-ms 35-V transient.

Frank Goodenough

Line regulation for all three outputs, with the supply between 7 and 26 V, is a maximum of 50 mV and typically 5 mV. Load regulation for the main and buffer outputs, from 5 mA to rated load, is also 50 mV, as is the standby supply with loads between 0.5 and 7.5 mA. In addition, all three outputs track each other within ±100 mV. (Actually the high-current outputs each track the standby output.) The two high-current outputs turn on or off according to the state of an external pin. When it is off, the chip's quiescent current is just 1.5 mA.



A logic level on pin 8 turns the 500- and 100-mA outputs of this 5-V linear regulator on and off. The 5-mA standby memory output remains on continuously.

Second, if the main output drops below 4 V or rises above 5.5 V, a reset pin drops low, indicating a fault condition. Moreover, it stays low until the fault terminates. An external resistor and capacitor can delay the return of the reset to 5 V to eliminate multiple resets in a short period of time due to transients.

The chip's watchdog timer looks at a train of square pulses from the processor (or any other source). If the pulse train disappears for longer than a time period set by an external capacitor, the reset pin signal again drops to zero and remains there until the pulses reappear.

If the supply rail exceeds 30 to 31 V, both the main and buffer outputs shut down. Large capacitors (>10 μF) between these outputs and ground can prevent rapid changes in voltage during turn-on and turn-off and are required to ensure stability.

Over a junction temperature of −40° to 125°C, the output voltages change less than ±25 mV. In its 11-pin plastic power SIP, the LM2984C regulator can dissipate up to 15 W at 125°C when mounted on an infinite heat sink and 15 W to 50°C with a 4°C/W sink.

In quantities of 100, unit price of the regulator is $4.60. Small quantities are available from stock.

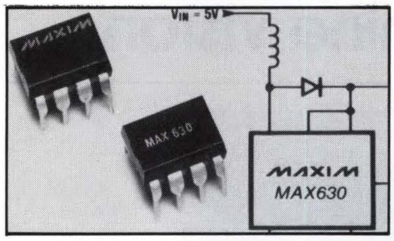
National Semiconductor Corp. 2900 Semiconductor Dr., Santa Clara, CA 95052, MS 16-71; Roy Essex, (408) 721-6527.

CIRCLE 310

NEW PRODUCTS

POWER

Dc-dc converter has 85% efficiency

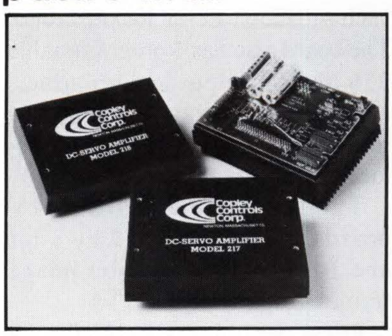


A dc-dc step-up converter offers simplicity of design and high efficiency in the 5-mW to 10-W range. The MAX630 achieves up to 85% efficiency in most applications and operates over an input supply voltage range of 2.0 to 16.5 V. An inductor, a diode, and two set resistors are all that is needed to convert a low voltage to a higher one. The device is offered in a variety of packages and temperature ranges.

Maxim Integrated Products, 510 N. Pastoria Ave., Sunnyvale, CA 94086; (408) 737-7600. Prices start at $2.80 (100 units); stock.

CIRCLE 342

Compact switchers pack 3 W/in.^{3}



Fan-cooled compact switching power supplies, the VF Series, pack power densities of more than 3 W/in.^{3}. The units, which meet all requirements of VDE, IEC, UL, DSA, BP, ECMA, and CEE, including 3750-V ac dielectric isolation, come in 500-to-1750-W versions with up to five outputs. The units comply with FCC electromagnetic interference requirements. Features include current-sharing parallel operation, no derating for parallel or redundant service, autodynamic bleed, and margining. All outputs are floating. The conversion frequency is 80 kHz, and efficiency is typically 80%.

Deltron Inc., P.O. Box 1369, Wissahickon Ave., North Wales, PA 19454; (215) 699-9261. $220 to $845 (OEM quantities); four to eight weeks.

CIRCLE 343

Compact servo amp delivers 49 W/in.^{3}

Requiring only 4 by 5 by 0.8 in. of pc board space, this compact servo amplifier delivers 750 W of continuous output and 2.1 kW of peak power for two minutes. The Model 217's ability to deliver three times the full power rating for short periods accommodates rapid servo motor acceleration and enables the amplifier to absorb the motor's regenerative energy during braking and rapid reversals. Its pulse-width-modulation design and MOSFET bridge output circuit hold heat dissipation at full load to 12 W.

Copley Controls Corp., 375 Elliot St., Newton, MA 02164; (617) 965-2410. $485; four to six weeks.

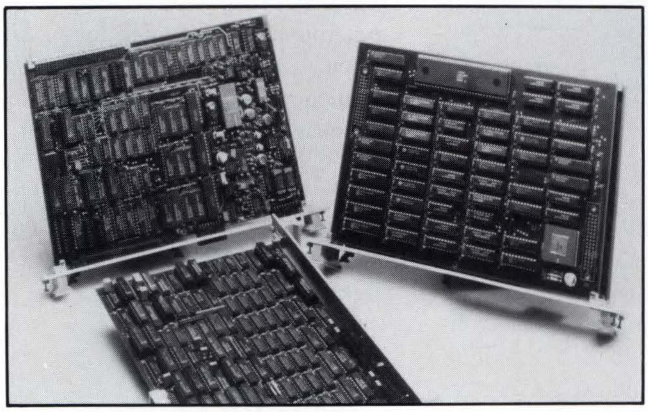
CIRCLE 344

NEW PRODUCTS

COMPUTER BOARDS

ELECTRONIC DESIGN EXCLUSIVE

VMEbus boards satisfy real-time machine vision



Thanks to the high-speed synchronous 10-MHz SV bus, the series 401V/441V vision boards may offer an innovative variety of interconnection schemes that deliver real-time (1/30 of a second) and near real-time performance to satisfy machine-vision applications. The series consists of the PX-401V pipelined image processor, the AS-401V video-input digitizer, and the DS-401V/441V storage boards. One or more PX-401Vs may be hooked to several memory boards through a single AS-401V.

Pyramid and region-growing applications, which require processing times of 1/30 to 2/30 of a second, may be satisfied with a single PX-401V working with a pair of memory boards. Typically, conventional boards take 1 s or more.

Alternatively, a pair of PX-401Vs, each working with its own memory board, can lengthen the image-processing pipeline. Thus, by essentially pipelining the pipeline, processing speed roughly doubles.

The PX-401V includes up to 3 independent SV bus ports, a pair of 18-bit counters, and a 16-bit ALU with overflow detection. It also holds a 16-bit barrel shift register with sign extension and preprocessing hardware with a 12-by-12 multiplier and a 4-by-4 lookup table.

The AS-401V digitizer handles up to 512 by 512 by 8-bit pixels. It accepts up to 4 RS-170, RS-330, or CCIR cameras and produces 3 output channels (red, green and blue), each with 256 by 8-bit lookup tables. The board also has 4 programmable 256 by 8-bit input lookup tables, automatic dc restoration, programmable gain and offset, and phase-locked-loop circuitry.

The DS-401V and DS-441V boards store 512 by 512 by 8-bit and 1024 by 1024 by 8-bit image frames, respectively.

Prices per unit are $3495 for the PX-401V; $2995 for the AS-401V; $2495 for the DS-401V; and $3495 for the DS-441V. All boards are available from stock to 30 days.

Recognition Technology Inc., 335 Fiske St., Holliston, MA 01746; (617) 429-7804.

CIRCLE 301

Roger Allan

NEW PRODUCTS

COMPUTER BOARDS

ELECTRONIC DESIGN EXCLUSIVE

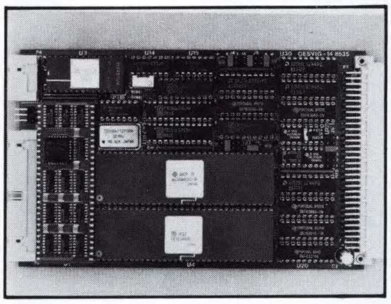
Using Eurocards, G-96 bus gets graphics

Two Eurocards are not only the first to put graphics on the G-64/G-96 backplane, they do so with a high-resolution verve—providing a 1024 by 1024 display. The GESVIG-14 and companion GESVIE-14 cards (as well as the G-64/G-96 backplane) are board products of Switzerland's Gespec S.A.

The GESVIG-14 is a graphics controller card designed around the Hitachi HD63484 advanced monolithic CRT controller. The GESVIE-14 is the companion frame buffer memory holding 2 Mbytes of dynamic random-access memory. The two cards are connected through separate ribbon cables, which allows the controller to access and refresh the frame memory without going onto the G-96 system bus.

The G-64/G-96 bus, developed by Gespac and supported by more than a dozen European manufacturers (including Thomson CSF), uses Eurocard form factors and DIN 41612 connectors that are similar to those of the VMEbus. Both G-64/G-96 and VME cards are 160-mm deep, though the 100-mm width of the G-64/G-96 card is about 17 mm narrower than a VME "half-card." Consequently, the GESVIG and GESVIE are among the densest graphics boards available today.

With the aid of its Hitachi ACRTC, the GESVIG-14 controller provides a bit map as large as 2048 by 2048, with 16 colors simultaneously available out of a palette of 256k (using the Inmos color palette chip). Other display features of the Eurocard board set include 1-to-16 zoom magnitude, line-by-line vertical scrolling, and pixel-by-pixel horizontal scrolling.



The controller includes 23 graphics drawing commands, including Line, Rectangle, Polygon, Circle, Arc, Filled Rectangle, and Copy. On a lower level, the controller handles software drawing by translating logical x-y coordinates into display memory addresses and then transferring these to the screen at a 2 million pixel/s rate.

The GESVIG-14 and GESVIE-14 board set will be less than $4000 in singles, with a steep OEM discount schedule. Production quantities will be available in June.

Gespac S.A., 3 chemin des Aulx, Plan-les-Ouates, CH-1228 Geneva, Switzerland; Marc Marinello, (022) 713400.

CIRCLE 312

Gespac Inc., 100 W. Hoover Ave., Suite 11, Mesa, AZ 85202; Cosma Pabouctsidis, (602) 962-5559.

CIRCLE 313

Stephan Ohr

NEW PRODUCTS

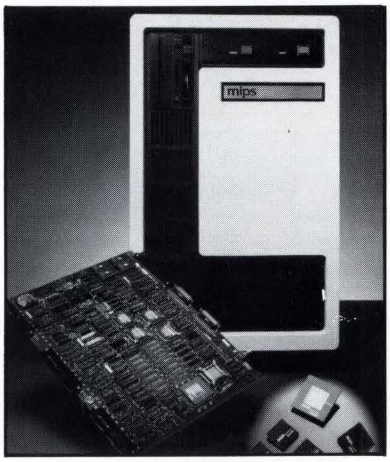
COMPUTER BOARDS

RISC μCs blaze through 5 MIPS

A set of CPU chips and board-level products based on RISC principles allows designers to build microcomputers that run at 3 to 5 MIPS—the range of today's top minicomputers. The lineup, from MIPS Computer Systems, includes two chip sets and three boards.

Each chip set comprises a proprietary CPU, a floating-point processor, and a set of four ICs known as the write buffer. The CPU is optimized for load-and-store operations and contains an on-chip MMU to speed local memory transfers. The write buffer serves as a cache coprocessor (eliminating memory wait states), and the floating-point processor performs math.

One chip set, the R2012KS, is optimized for 12-MHz operation and churns through 3 MIPS. The R2016KS runs at 16 MHz, burning through up to 5 MIPS. Samples of each set will be available in the late summer and will cost $1850. The price includes a binary copy of the Unix operating system, some software utilities (such as a monitor and debuggers), and a C compiler.

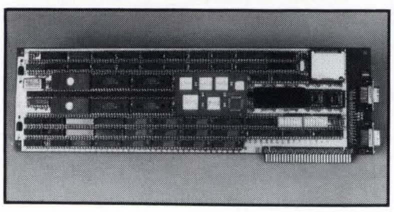


The three boards include the R2100 CPU, which has a sustained performance of 3 MIPS and a VMEbus interface. It does not carry a write buffer. The R2300 is a 5 MIPS CPU board that includes a write buffer and the manufacturer's proprietary memory access bus. (The VMEbus is used here for power and ground.) The R2600 runs at 8 MIPS. Pricing for the boards, in 500-piece lots, is $4000, $6080 and $8170, respectively. Delivery is targeted for July.

MIPS Computer Systems Inc., 930 Arques Ave., Sunnyvale, CA 94086; Christine Friedly, (408) 720-1700.

CIRCLE 307

Card gives PC access to 1553 bus



A plug-in card for the IBM PC adds a MIL-STD-1553B interface. The Model BCU/PC-1553 comes with an on-board 80186 microprocessor, 32 kbytes of RAM, and programmable DMA transfers and interrupts. Message processing and protocol definition are performed on the board, freeing the computer's processor for other tasks. Programmable operating modes allow use as a bus controller, remote terminal, bus monitor/analyzer, and diagnostic tool.

SCI Technology Inc., 8600 S. Memorial Pkwy., Huntsville, AL 35802; (205) 882-4251. $4950.

CIRCLE 345

A Microwave Collection That Stands Up To The Toughest Critics

Critique the MMICs. "Just how good are their new prescalers, transistor arrays, and amplifiers? What kind of reputation does NEC have? Do they rush products to the market before they're tested? Will they support us throughout the product cycle? What's their track record?"

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Question the GaAs FETs. "How do they stack up in performance and reliability? Can we get any custom design work? I understand NEC offers the best linearity in power FETs, but what else makes them so special?"

Scrutinize the Bipolars. "Do they have them for all of our frequency bands and in low cost packages as well as chip form? Can they provide low cost, high volume production with SMT packages?"

What about Diodes? "Can we get PIN, Varactor, and Schottky Quads? What about beam leads and GaAs IMPATTs? What's the reliability like?"

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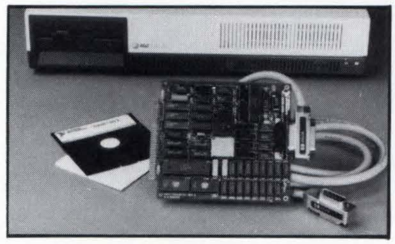
Europe: NEC Electronics GmbH 0211/650301

CIRCLE 129

COMPUTER BOARDS

Interface joins 3B2 with IEEE-488 bus

A smart interface card, the GPIB-3B2, connects the AT&T 3B2 computer family with the IEEE-488 bus. The board includes an 80186 processor plus 128 kbytes of memory. The data transfer rate is 790 kbytes/s. The architecture of the board is oriented towards high performance, real-time UNIX applications using IEEE-488 devices. The on-board processor helps off-load GPIB-related processing from the host computer. Programs can be developed in National Instruments' IEEE-488 Bus Control Language and downloaded to the board for execution. Frequently-used functions or entire applications can be developed on the computer and downloaded to the board for execution by the 80186 processor.



National Instruments, 12109 Technology Blvd., Austin, TX 78727-6204; (800) 531-4742 (outside Texas) or (800) 433-3488 (in Texas). $1795.

CIRCLE 346

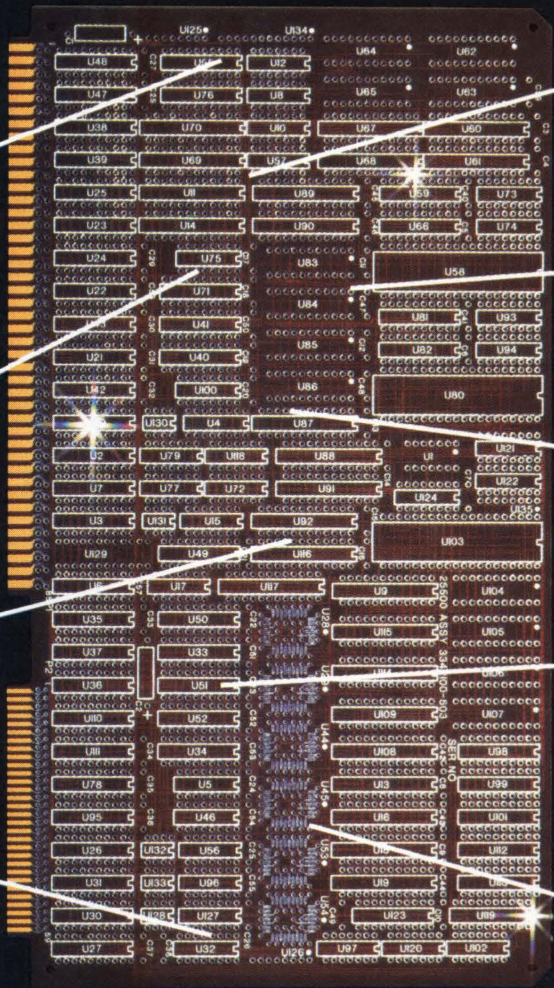
Card upgrades Apple computers

A peripheral plug-in board plus matching firmware upgrade Apple II, II+, and IIe computers. The EasyCard includes built-in programs, including desk accessories with floating-point and logical calculators, an ASCII table, a note pad, a screen dump utility, a copy program, and a clock. Additional battery-backed RAM or EPROM is available for storing DOS, ProDOS, or other files up to 192 kbytes. Light pen and mouse interfaces are optional.

Applied Technology Laboratories, 11926 Santa Monica Blvd., Los Angeles, CA 90025; (213) 477-6815. $269.95

CIRCLE 347

WHY MULTIWIRE® BOARDS FROM MULTIWIRE DIVISION ARE BETTER THAN MULTILAYER.



Computer-generated patterns of insulated wire form permanent interconnections.

Wires cross over each other without shorting. X and Y axis routed on the same plane.

Easily handles high-speed signals like ECL and FAST.

Meets or exceeds ANSI/IPC-DW-425 (DOD) and the performance requirements of MIL-P-55110.

Accommodates component densities of 0.4 square inch per IC and greater.

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Designed from as little input as a schematic or netlist.

Superior electrical characteristics. Crosstalk and impedance levels tightly controlled.

Electroplated surface features mechanically and electrically accommodate surface-mount components.

MAKE IT A POINT TO BUY MULTIWIRE® BOARDS FROM MULTIWIRE DIVISION.

Multiwire Division's electroplated circuit board construction provides surface features for surface-mount components as well as traditional through-hole-mount components. Our experience in new package types encompasses both leaded and leadless devices with pin pitches of 18 mils or more, pin grid arrays and discrete surface-mount components.

We have successfully designed and manufactured boards to accommodate pin grid arrays and chip carriers with 130 pins and greater. Because our insulated wires can be crossed without shorting, board real estate can be used for components instead of via holes. This allows increased packaging densities and decreases the need to interconnect between cards, which can result in greater system reliability and lower costs.

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Over the last 16 years, Multiwire Division has designed and manufactured thousands of Multiwire boards. We have produced boards for through-hole and surface-mount components, military and VHSIC/VLSI applications and used our expertise and experience to solve system and circuit design problems for high-speed logic and thermal management applications. Our sales, design and manufacturing centers located across the country are ready to prove to you the advantages of Multiwire boards from Multiwire Division. For a free copy of our brochure, just fill out and return the coupon.

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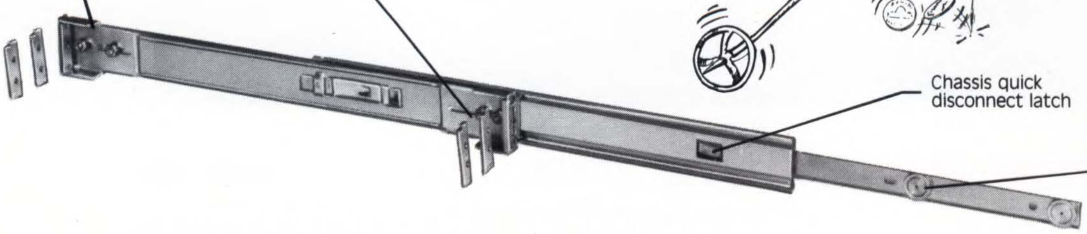
3901 East La Palma Ave., Anaheim, CA 92807 (714) 632-7770

CIRCLE 134

Great Milestones in Packaging

Rebirth of an ancient packaging series reluctantly revived by Jonathan Manufacturing Corporation



We're sure that Ma Bell had another idea in mind when she designed the original phone booth, but good olde Yankee ingenuity took over and was not about to let all that space go to waste – giving new meaning to the words "High Density". No easy in, easy out here. Jonathan saw this same situation arising in standard 19" cabinetry, as it lent itself more and more to high density chassis packaging but still contended with less than acceptable stick-slip access with friction chassis slides.

The answer to this predicament is Jonathan's new Series 375QD TRU-GLIDE® ball-bearing steel chassis slide. The replacement for the friction Accuride 830, Chassis Trak C-300, Grant SS-168 and Zero C-300 models, this new 75-lb. capacity slide is thin (3/8") enough to fit easily in a standard 19" cabinet, while providing smooth ball-bearing action and all the precise mounting, locking and chassis disconnect features you could want.

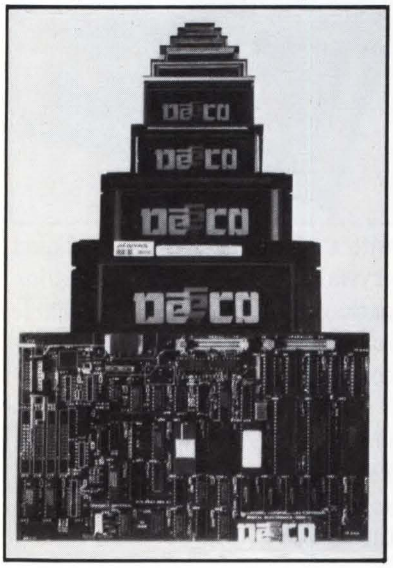
Don't fight with binding friction slides… when, for a few dollars more, you can put Jonathan's 30 years of packaging experience to work to smooth out all your access problems.

Jonathan Manufacturing Corp., 1101 So. Acacia Ave., Fullerton, CA 92634 • (714) 526-4651

CIRCLE 135

COMPUTER BOARDS

Controller links to flat-panel displays



A VDI-based graphics controller for flat-panel display applications interfaces with most electroluminescent and gas-plasma dot-matrix displays currently on the market. The C2 series is capable of handling any matrix up to 512 by 512 dots and employs a dual pipelined architecture for fast drawing speeds. Either 8-bit parallel or RS-232-C (or RS-449-interfaces are available. An IBM PC-style keyboard connector is standard.

Digital Electronics Corp., 26142 Eden Landing Rd., Hayward, CA 94545; (415) 786-0520. $895 (100 units).
CIRCLE 348

Card boosts PC video resolution

A high-resolution video display adapter boosts the maximum resolution and color on standard pre-EGA IBM color and monochrome monitors. The Hi-Res Graphics Card is 100% compatible with the IBM graphics adapter, the IBM monochrome adapter, the Hercules Graphics Adapter, and the Plantronics ColorPlus cards. The card fits in a short slot of an IBM PC and includes an IBM-compatible parallel printer port and flicker-free scrolling. The board is based on a single-chip video controller.

Paradise Systems Inc., 217 E. Grand Ave., South San Francisco, CA 94080; (415) 588-6000. $299.
CIRCLE 349

PACKAGING & PRODUCTION

Programmer handles 98 device types

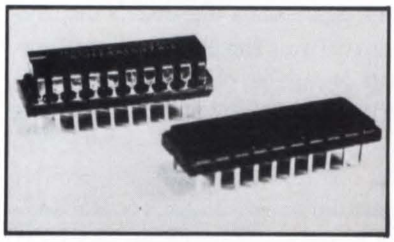
A lightweight programmer is capable of programming 98 types of EPROMs and EEPROMs. By designating the device type from the keyboard, typical memory devices ranging from 16 to 512 kbits can be accommodated using the same single socket. The EZ-PRO unit has both a serial and parallel port, along

with a 16-character-by-2-line liquid crystal display. A communication package, EZ-COM 198, is available for operation with an IBM PC or compatible computer.

Zax Corp., 2572 White Rd., Irvine, CA 92714; (714) 474-1170. $895 (programmer); $200 (PC software).

CIRCLE 350

Adapter converts DIP IC pinout



A low-profile adapter is used to reconfigure the pinout of any IC housed in a dual-in-line package. The DIP leads are soldered directly onto pads located on the top surface of the adapter. The entire assembly is then soldered directly into a DIP pattern or plugged into a standard IC socket. Together they have an overall height of only 0.245 in., including 0.125 in. nominal for a typical IC height. Once 4C Electronics has received the desired connection list, it will deliver the customized device within two weeks.

4C Electronics Inc., 9330 Progress Pkwy., Mentor, OH 44060; (216) 354-6800.

CIRCLE 351

New, VDE-approvable goodwill protection.

We've taken a few extra steps to assure that the circuit protection you design into your Europe-bound computer consoles and other control panels will be well received abroad.

Continental styling and construction.

Our new JB/S fully magnetic circuit breakers give you fine styling that invites installation up front, where their good looks can be appreciated and their ON/OFF status easily monitored.

American smarts.

And uniquely Heinemann—several JB/S breakers snap into a single panel cutout, and line up side-by-side with equal spacing between poles. No mounting holes, templates, screws, or tools. In short, a simple snap-in device that's very robot-friendly.

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Performance that goes beyond good looks and convenience. Decades ago, we eliminated the need for derating the rated current in high operating temperatures with the very first hydraulic-magnetic breakers. Today, our JB/S protectors, in UL-recognized current ratings from 0.2 through 30 amperes at 250V 50/60 Hz and 400 Hz, and through 50 amperes at 65 Vdc, offer all the special-function internal circuits and other options you'll find in our standard line of J-Series breakers.

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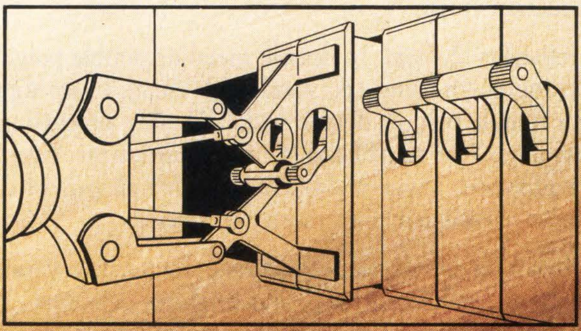
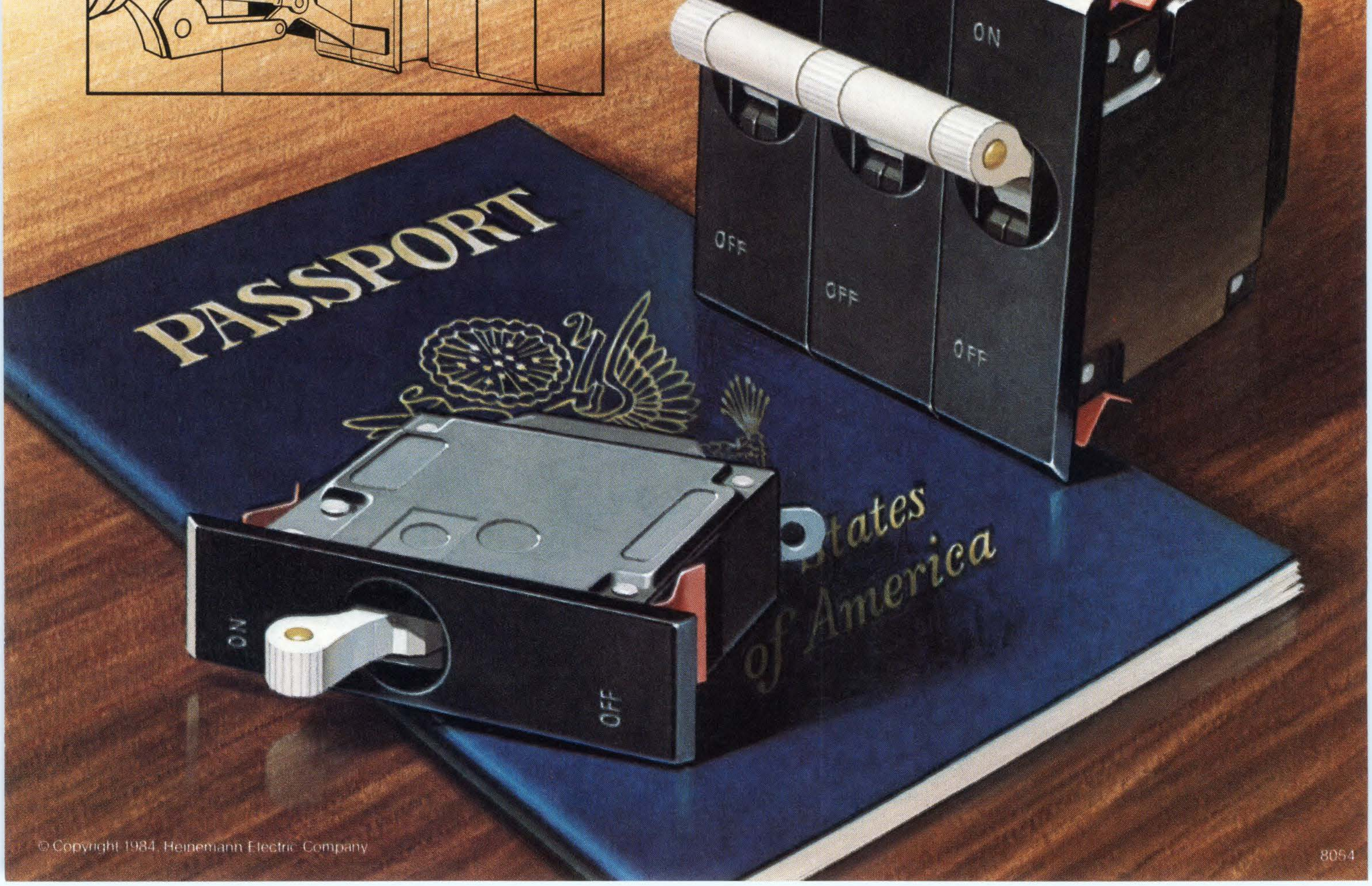
CIRCLE 139





8054

NEW PRODUCTS

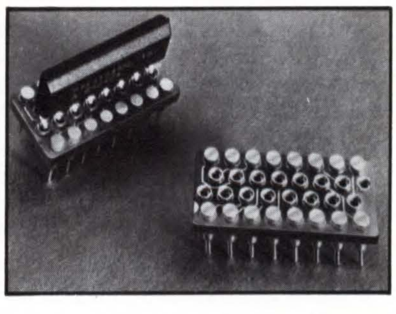
PACKAGING & PRODUCTION

Flexible heaters hold temperatures

Kapton-based flexible heaters offer precise temperature control in confined areas. Kapton is a self-extinguishing, transparent material with good physical and electrical properties. It offers thermal stability over a wide temperature range, up to and including 220°C. It allows low outgassing in high-vacuum environments and is resistant to chemicals and solvents. The heaters have a wrap-around design that suits them to controlled heating of confined areas or uneven surfaces. Both standard and custom configurations are available.

Ocean State Thermotics Inc., 107 Railroad Ave., Johnston, RI 02919; (401) 231-4640.
CIRCLE 352

Socket fits zig-zag RAMs

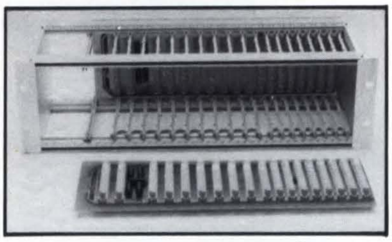


A 16-pin socket accepts ZIP (zig-zag in-line package) dynamic RAMs from Mitsubishi, Fujitsu, Panasonic, and others. The socket, part no. 16-539-10, solders into a pc board on standard 0.3-in. center, 16-pin spacing but accepts the zig-zag foot pattern of the memory IC. The socket also converts the ZIP logic to standard DIP logic by the use of a miniature pc board. No special drilling is required prior to soldering to the pc board. The socket is made of UL-94V-0 material.

Aries Electronics Inc., P.O. Box 130, Frenchtown, NJ 08825; (201) 996-6841. $9 (100 units); six to eight weeks.
CIRCLE 353

PACKAGING & PRODUCTION

Card cage holds 16 RM 65 modules

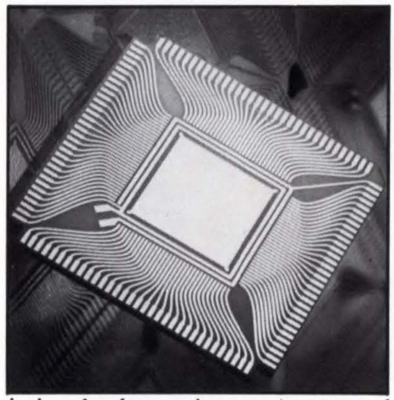


Designed to fit standard 19-in. racks, a card cage accepts up to 16 Eurocard-size modules based on the Rockwell RM 65 bus, plus a power supply. Eight slots of the RM65-7018E card cage are on standard 0.6-in. centers, while the remaining eight are on extended 0.8-in. centers. It can readily house complete systems built with RM 65-compatible modules or house an expansion of an AIM 65 microcomputer-based system.

Dynatem Inc., 19 Thomas, Irvine, CA 92718; (714) 855-3235. $350.

CIRCLE 354

Chip carriers match VLSI needs

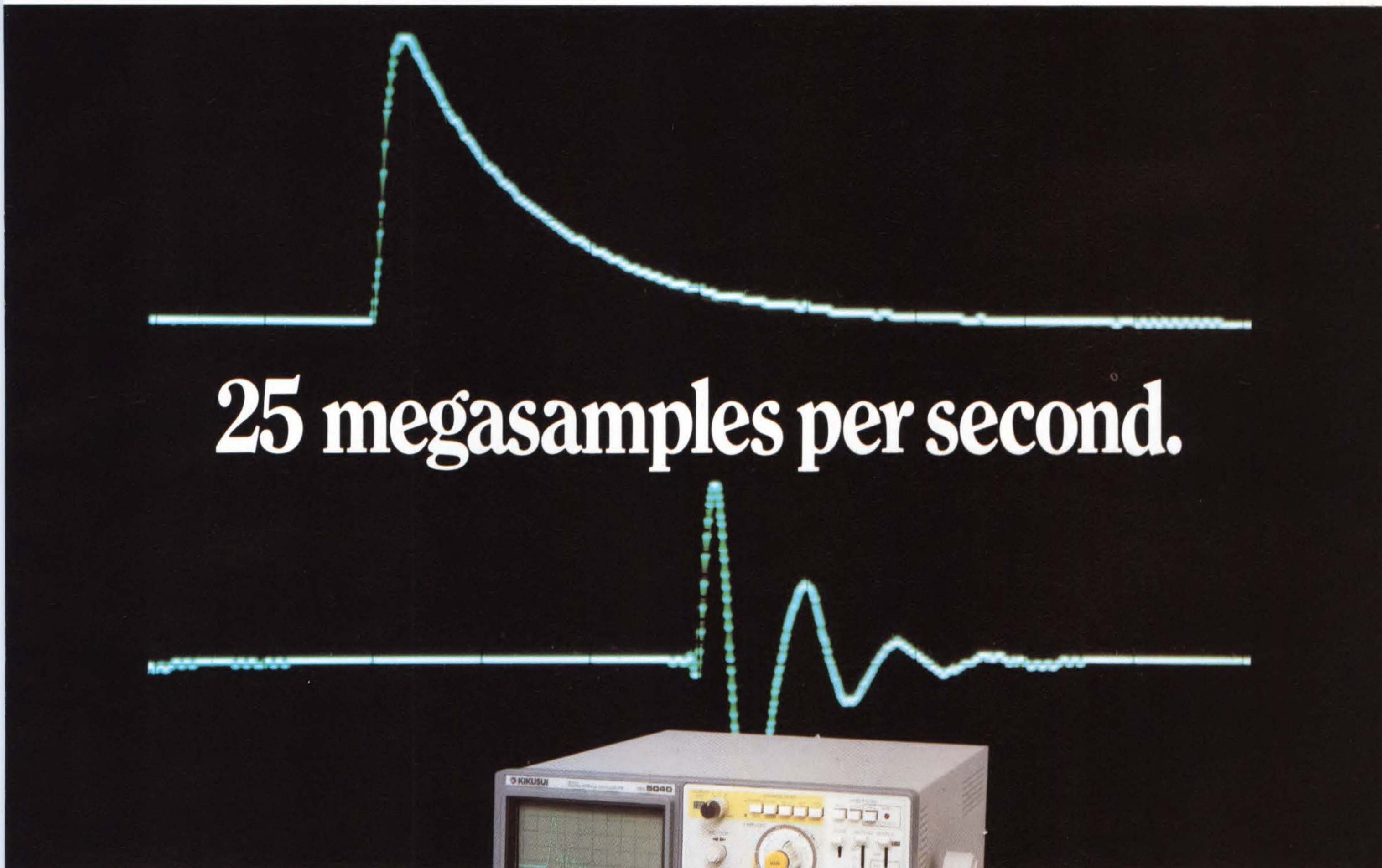


Ceramic chip carriers use pure copper metallization, protected by gold-over-nickel plating, to suit the needs of high-speed, high-density VLSI packaging. The carriers accommodate up to 320 leads on a single 0.95-by-0.95-in. 96% alumina carrier. The 0.001-in. thick copper provides low conductor resistance, and a single-sided circuit pattern minimizes lead capacitance. A patented geometry provides low-inductance lead paths, lands for an internal decoupling capacitor, and concentric power and ground buses surrounding the chip attachment area.

Amp Inc., Harrisburg, PA 17105; (717) 564-0100.

CIRCLE 355

What Tek® can't catch for $2995.



How much scope will $2995 buy you? A lot—if it's Kik's new DSS 5040.

This dual-channel portable digital storage/analog scope delivers a 10 MHz single-occurrence capture rate. That's 25 megasamples/sec for just $2995. You'd pay $1155 more to get the same sampling rate from Tek.

More performance per dollar than anyone.

The Kik DSS 5040's real-time bandwidth is 40-MHz—with a 25 MHz digitizing rate. That's megaperformance ahead of anything in its price range. And Kik's standard feature package includes Level-Lock™ automatic triggering, linear auto focus, HF reject, video synch separator, pre/post trigger data, sine/pulse interpolation, 100X expansion mode, plus 1K of memory on both channels, a channel one output and a recorder output.

The DSS 5040 is as easy to operate as it is to finance. Function controls are identical to those on an analog scope. The only additional controls are a push button selector for sine or pulse interpolation and push button controls for store, save and reference memory.

The 5040 stores up to 10 MHz in sine interpolation mode and can capture up to 64 nsec rise times in pulse interpolation mode. It has a signal "add" mode and reference signal storage capability to facilitate signal comparison.

Kik the Tek habit. Phone 800-421-5334 today.

Both the Kik DSS 5040 and its sister scope, the 5020A (with a 1 MHz digitizing rate), are backed by a two-year warranty and a 30-day return option. Service is available at over 40 Kik centers nationwide. And if you need applications assistance, it's as close as your phone. Call or write Kikusui International for more information. You can match the Kik DSS 5040 for $4150. For $2995, you won't find its equal anywhere.

KIK®

We're not riding on a reputation, we're making one.

Kikusui International Corp., 17819 S. Figueroa, Gardena, CA 90248
800 421-5334 or 213 515-6432 (in CA, HI)

See us at Electro '86, Booths Nos. 649-651.

CIRCLE 142

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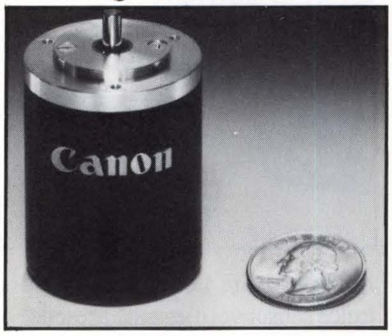
MURATA ERIE NORTH AMERICA, INC.

CIRCLE 143

FACTORY AUTOMATION

Compact encoder has high resolution

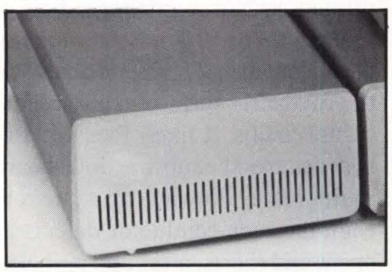


An incremental rotary encoder, which uses a semiconductor laser light source operating at 780 nm, provides 81,000 sinusoidal or square pulses per revolution in a package only 36 mm in diameter and 47.5 mm in overall length. Suitable for applications in factory automation and robotics, the optical encoder requires a ± 5-V dc power supply. Maximum response frequency is 500 kHz (6 revolutions per second).

Canon U.S.A. Inc., Components Division, 1 Canon Plaza, Lake Success, NY 11042; (516) 488-6700.

CIRCLE 356

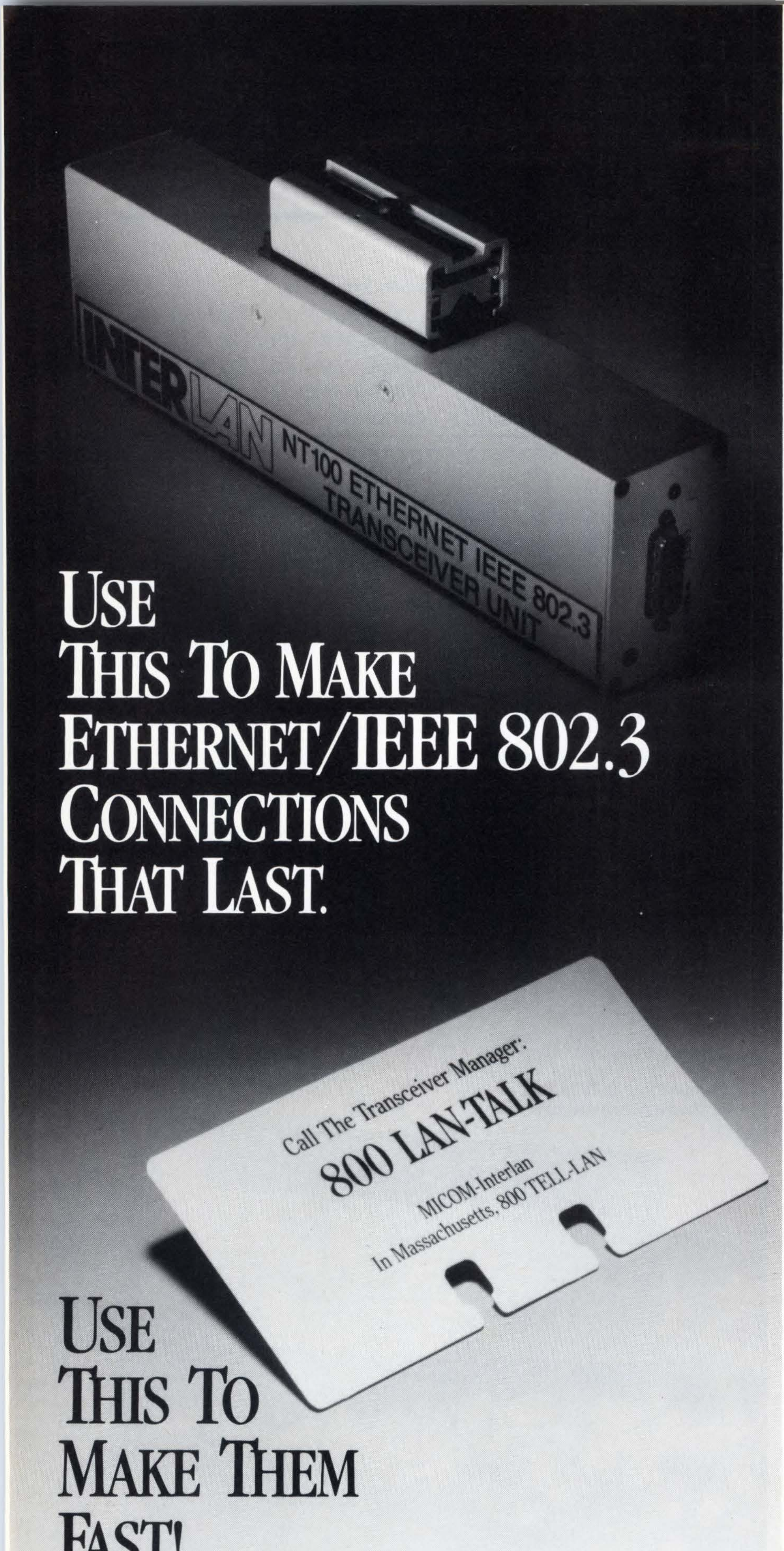
Motor controller uses IBM PC host



A multiple-axis motion control subsystem interfaces an IBM PC with up to 10 stepping, linear, or servo motor drives which accept digital step and direction commands. When combined with the appropriate driver and motor, the PC68 will generate up to 50,000 steps/revolution—even with a standard 200-step/revolution stepping motor. The standard velocity range of the PC68 is from 0 to 524,287 pulses/s, while a high-speed option permits 1,048,575 pulses/s.

Oregon Micro Systems Inc., 15075 N.W. Pioneer Rd., Beaverton, OR 97006; (503) 644-4999. $1495 (two axes).

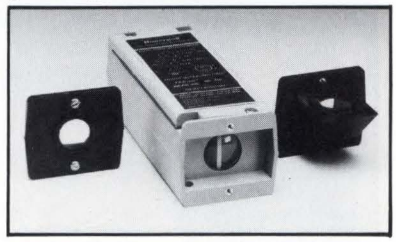
CIRCLE 357



NEW PRODUCTS

FACTORY AUTOMATION

Sensor verifies part position



A three-zone noncontacting distance sensor verifies part presence or absence and object position in manufacturing and assembly applications. The HVS 300 infrared sensor measures the distance of objects out to 30 in. and reports near/ok/far or out-of-range zones. Easy to install, the zone switching points are quickly adjusted with a screwdriver. The unit has a response time of 10 ms.

Honeywell Visitronic, P.O. Box 5077, Englewood, CO 80155; (303) 850-5050. $630.

CIRCLE 358

Optical system spots pc defects

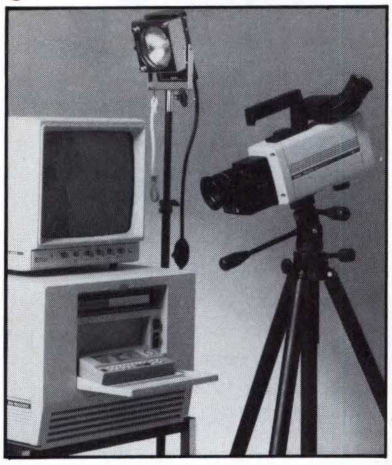
An automated optical inspection system, called the Inspector/Verifier, inspects and detects defects in printed-circuit boards regardless of surface quality. The system is not dependent on the cosmetic quality of the conductor surface to achieve accurate results. A finely focused laser beam causes the substrate of a board to fluoresce, allowing the system to examine such conductor defects as opens and shorts, nicks and pinholes, and out-of-tolerance conductor width and spacing. Information about the defects is stored in the form of a map on a floppy diskette.

Lincoln Laser Co., 234 E. Mohave St., Phoenix, AZ 85004; (602) 257-0407.

CIRCLE 359

FACTORY AUTOMATION

Motion analyzer grabs 1000 frames/s



Priced for broad market acceptance, a motion analyzer is capable of recording up to 1000 pictures/s for instant playback in various slow-motion modes. The analysis system can be used to reduce machine downtime, increase productivity, and improve quality assurance in such applications as computer-aided manufacturing and automated assembly. Data recorded by the Ektapro 1000 can be transmitted for simultaneous computer analysis or for image enhancement.

Spin Physics, 11633 Sorrento Valley Rd., San Diego, CA 92121; (619) 481-8182. $60,000 for basic configuration.

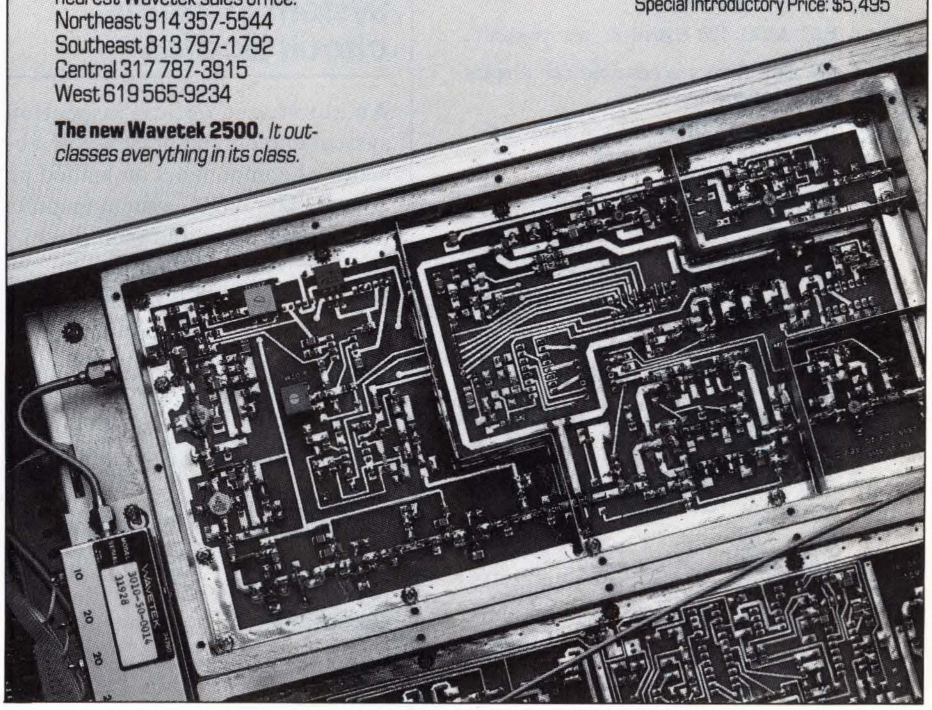
CIRCLE 360

Photosensor uses modular design

A photoelectric sensor, the Maxi-Beam, uses a modular design to allow appropriate configuration of logic and other scanning parameters. The design separates the sensor head, the power block, and the wiring base. The head rotates to four 90° positions to simplify mounting and multidirectional sensing. The sensing heads are interchangeable and allow use of retroreflective, diffuse, and opposed sensing modes, as well as fiber optics for applications with severe space or environmental limitations. Scanning ranges are 30 ft (retroreflective), 60 in. (diffuse), and 350 ft (opposed).

Banner Engineering Corp., P.O. Box 9414, Minneapolis, MN 55440; (612) 544-3164.

CIRCLE 361



System finds absolute positions

The combination of a heavy-duty position transducer and an analog-to-digital converter/interface digitize high-speed, broadband analog input signals. A parallel or serial output is available in straight binary, complementary binary, BCD, a digital readout, and/or an input to a controller. The position transducer measures absolute movement and converts linear or angular displacement into an analog signal. The signal is digitized and the information made available for interfacing or display. The system has a resolution to within 1 part in 65,535 (TAD 1600-HS) or 1 part in 4095 (TAD 1200-HS) with an accuracy to within ±0.05%. All output and control signals are TTL-compatible.

Siko Products Inc., P.O. Box 1461, Ann Arbor, MI 48106; (313) 426-3476. $600 (OEM quantities); four to six weeks.

CIRCLE 362

System inspects circuit boards

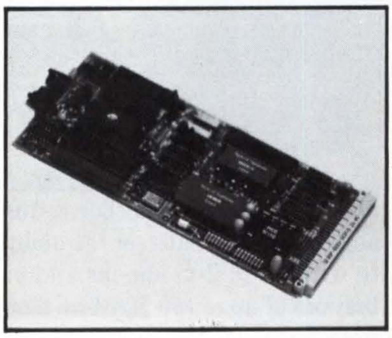
An automated optical inspection system detects the presence or absence of components on loaded pc boards. The AQIC system inspects board sizes up to and including 14 by 18 in. with a resolution of 200 points/in. (0.005 in.). This density of inspection is the equivalent of 2800 by 3600 available pixels—one of the highest pixel ratings in the industry. The turnkey system also uses a color camera to obtain greater definition.

Camsystems Inc., 2211 W. Roosevelt, Phoenix, AZ 85009; (602) 894-2689.

CIRCLE 363

FACTORY AUTOMATION

Analog module links to control network



An analog input module, the dDCM300A, provides an easy way to link analog input devices with a distributed control network environment. The Bitbus-based unit provides a standardized environment for the 8051 microcontroller architecture, supplemented with a real-time, multitasking, message-driven operating system. The module supports 16 single-ended or 8 differential analog input channels and 16 bits of digital I/O. The analog input subsystem's throughput rate is 30 kHz for full 12-bit precision. An on-board dc-dc converter allows operation of the entire subsystem from a 5-V supply.

Datem Ltd., 148 Colonnade Rd., Nepean, Ont. K2E 7R4, Canada; (613) 225-5919. $995; stock.

CIRCLE 364

Affordable camera has dual scan rate

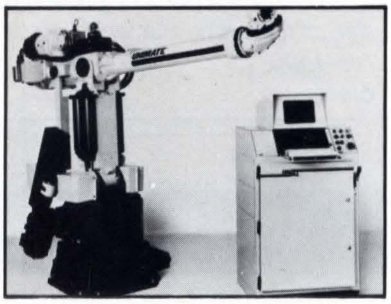
To meet the demand for machine vision at affordable prices, Sierra Scientific has introduced a one-piece tube camera for $6800. The Visioneer Model HB-3200 performs automatic data acquisition and can operate at two scan rates—525 or 1023 lines/frame. Bandwidth is automatically switched to match the scan rate selected. Bandwidths from 5 to 25 MHz may be specified.

Sierra Scientific, 1173 Borregas Ave., Sunnyvale, CA 94089; (408) 745-1500.

CIRCLE 365

FACTORY AUTOMATION

Controller directs robotic systems

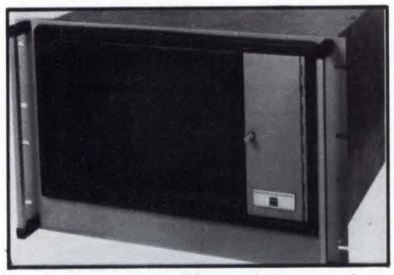


An advanced robot controller, the Unival, operates quickly with processing speeds of just 8 ms. The unit features all-digital servo and torque control, the VAL III programming language, and two plug-in vision system options. The unit is compatible with standard local area networks, such as MAP, SECS III, and the Intel Bitbus. The controller's speed results in smooth robot arm motion at low speeds. Trajectory updates are doubled for high-speed path following. An open architecture allows easy integration into any manufacturing environment.

Unimation Inc., Shelter Rock Ln., Danbury, CT 06810; (203) 796-1069.

CIRCLE 366

NEMA enclosure protects CRT



A 12-in. CRT display is housed in a rack-mounted NEMA 12 enclosure for tough factory environments. The NEMA 12 rating specifies protection against splashes and dripping moisture, as well as airborne dust and dirt. It also calls for the ability to withstand 2-G shocks and vibrations of up to 150 Hz. Two monitors are offered in the NEMA 12 steel enclosure: The 1003 is a monochrome display (priced at $895), while the 1004 is an RGB color display (priced at $1395).

Texas Microsystems Inc., 10618 Rockley Rd., Houston, TX 77099; (713) 933-8050.

CIRCLE 367


Ford

NEW PRODUCTS

COMPUTER-AIDED ENGINEERING

ELECTRONIC DESIGN EXCLUSIVE

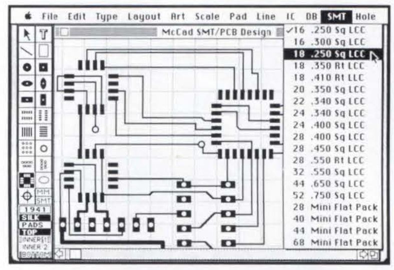
McCAD ready to go for SMT layout

Taking a shortcut to pc-board design, engineers have been relying on their own personal computers instead of layout specialists or complex computer systems. The high-resolution Apple Macintosh, which has already proved effective in such cases, has just received a boost. A new package, McCad SMT/PCB, applies the Macintosh to surface-mount technology with line resolutions of 0.001 in. or 0.0254 mm. Developed by Vamp, the package delivers interactive layout for small to mid-size boards.

With McCAD SMT/PCB, a user can lay out a multilayer board with special mounting patterns for surface-mounted devices. Up to six layers, including power and ground, can be defined and viewed individually or in combination. Loaded with the software, a Macintosh can support a board described in up to four D-size drawings. Board layout times can be reduced from weeks and months to days and weeks. In addition to surface-mount designs, McCAD can be used for standard through-hole PCBs or hybrid layouts.

Variable layout grids, a centered zoom, a precision x-y locator, and a standard library of layout objects ease the designer's task. Up to 27,000 different objects, each of which can be used more than once, can be handled for a single board.

The surface-mount patterns are made up of a set of properly oriented pads. The system can define a number of different pad shapes including square, round, rectangular, and oval shapes. Up to 18 sizes are carried for each shape.



The Macintosh and SMT/PCB delivers an interactive environment. Pull down menus (top of screen—SMT menu selected) make function and component selection easy. The vertical menu (left side) shows the art elements available as well as specifies the layers displayed.

The McCAD library contains over 2000 art items. Among those items are standard DIP patterns ranging from 8 to 40 pins. Also, the library includes 9-, 15-, 25-, and 37-pin DB connectors.

McCAD runs on any Macintosh with 512 kbytes of memory. It also runs on the earlier Lisa or XL machines and drives a number of pen plotters and output devices.

McCAD Metric/SMT/PCB design sells for $595. An SMT evaluation disk is available for $25. Software support is provided for the first 30 days. Extended support, which includes program updates, is available for an annual fee of $95. A pcb Gerber-type photoplotter driver is also optional, at $145.

Vamp Inc., P.O. Box 411, Los Angeles, CA 90028; (213) 466-5533.

CIRCLE 304

Ray Weiss

A New Phasemeter with "Lab Standard Accuracy"

At half the price you'd expect

Ultra-precise phase angle measurements from 1Hz to 10MHz—that's what Krohn-Hite's Model 6620 programmable phasemeter offers. Accuracy so exact that this phasemeter will serve in countless labs as a secondary standard.

Typical accuracy is .02 degrees and resolution is .01 degree. The Model 6620 has automatic ranging, AMC™ (Auto Meter Correct), and a reference mode for deviation measurement. A five digit LED display provides continuous direct readout. And Krohn-Hite offers the phasemeter in three configurations so you can choose exactly what you want and not pay for more than you need.

IEEE-488

- ☐ The super-accurate, fully programmable (IEEE-488) Model 6620 for $3695.
- ☐ The non-programmable Model 6610 with equal accuracy for $2995.
- ☐ The Model 6600 for users with limited demands for $2295.
- ☐ RS 232 optional.

These phasemeters accept a wide range of input signal levels (10 millivolts to 320V RMS). A five digit LED display provides continuous direct readout.

For more information on our product lines, look in EEM or Gold Book. **Or call, toll free, 1 800 582-1660.**

KROHN-HITE CORPORATION

Avon Industrial Park, Avon, MA 02322
(617) 580-1660 TWX: 710 345 0831

CIRCLE 184 OR CALL 1-800-582-1660

PRODUCT NEWS

RUN INTEL SOFTWARE ON IBM PC'S

Transform an IBM PC, or compatible into a totally integrated Intel Micro Development Station capable of running all 8 bit ISIS-II, and 16 bit ISIS-III software. the MICRUN80, and MICRUN86 Universal Development Interfaces (UDI), will allow you to increase your development capabilities with faster, more reliable, and more affordable PC based development stations. Both (UDI)'s come complete with a communications program for transferring Intel software to your PC. Micro Interfaces Corporation, 6824 N.W. 169th St., Miami, Fl 33015 (800) 637-7226 or (305) 823-8088 $450 each.

CIRCLE 186

RUN CP/M-80 SOFTWARE ON IBM PC'S

New CP/M to MS-DOS interface combines hardware and software to provide PC's with the ability to execute CP/M80 software. RUN/CPM comes with an NEC V-20 microprocessor which replaces the PC's 8088 chip and provides dual 8 bit/16 bit processing ability. Software features include, terminal emulation, ability to run CP/M programs from hard disks or RAM disks, logical drive assignments, ability to run 8 bit or 16 bit programs from the same prompt, and a disk emulation feature which allows your PC's floppy disk drives to directly read, write, and format approx. 100 CP/M disks. Micro Interfaces Corporation, 6824 N.W. 169th St., Miami, Fl 33015 (800) 637-7226 or (305) 823-8088 $99.95

ADVERTISEMENT

CIRCLE 187

NEW PRODUCTS

CAE

Graphic stations rival IBM 5080

Designed for mainframe-based CAD/CAM users, two color graphic workstations provide higher-performance IBM 5080-compatible graphics functions. These include a 45-ns pixel write time and the ability to identify occurences of coincident, intersecting, or overlapping geometries in a design and to make changes to them quickly and easily. Compatibility with the advanced 5080 instruction set is also provided. Prices for the CGX 2033 Model 1A and Model 2 start at $19,400 and $20,900, respectively.

CGX Corp., 43 Nagog Pk., Acton, MA 01720; (617) 263-3222.

CIRCLE 368

PC program builds microwave filters

Two software programs for the IBM PC and compatibles, designated ECS and ECM, simplify the design of edge-coupled strip-line and microstrip filters. All that the engineer is required to bring to the program are the basic electrical specifications, and the program prompts for the rest. Filters are then designed within seconds.

EEsof Inc., 31194 La Baya Dr., Westlake Village, CA 91362; (818) 991-7530.

CIRCLE 369

CAE

System designs VLSI devices

An integrated system, the SuperSet 5000, ties together the complete integrated-circuit design cycles, from conceptual design to final chip layout. Based on Apollo Domain workstations, the system consists of BaseSet, an infrastructure module; StrucSet for schematic capture; SimuSet for mixed-mode/multilevel and analog simulations; TopSet for symbolic hierarchical topological design; GeoSet for geometric design; and GluSet and PlaSet for automatic layout generation. BaseSet consists of an integrated design data-base management system and a system-wide inter-applications communication module.

Clarity Systems Inc., 710 Lakeway St., Suite 290, Sunnyvale, CA 94086; (408) 730-1381. $80,000 (average per-set price).

CIRCLE 370

IC CAE/CAD pack uses expert system

A CAE/CAD system for IC design and layout, ESP/C, provides designers with expert-system help for use on an IBM PC AT. The package uses advanced design techniques and knowledge-based methods for full-custom or semi-custom design, layout, analysis, and verification. Included are schematic capture, logic simulation and testing, layout design and editing, interactive design rule checking, and electrical rule checking. Designs may then be uploaded to a MicroVAX II.

Factron Electronic Design Automation, 269 Mount Hermon Rd., Scotts Valley, CA 95066; (408) 438-2880. From $25,000.

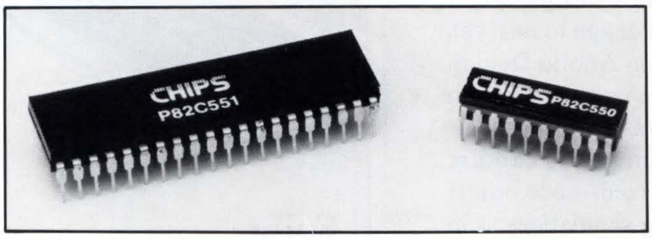
CIRCLE 371

CIRCLE 188

COMMUNICATIONS

ELECTRONIC DESIGN EXCLUSIVE

Pair of CMOS ICs eliminates 140 devices for Starlan link



Two CMOS chips—a serial interface IC and a hub controller—simplify links to AT&T's Starlan local-area network. The pair, from Chips and Technologies, respectively replace roughly 60 and 80 devices, reducing the cost of connecting a node to the $100 to $200 range that Starlan is targeted at.

Starlan is a star-shaped logical bus network derived from Ethernet. The draft specification is compatible with the IEEE-802.3 standard, uses CSMA/CD accessing, and transfers at 1-Mbit/s over twisted-pair wiring.

The 82C550 serial interface IC carries Manchester encoding and decoding circuitry that puts data into an NRZ format. It also packs a transceiver circuit. The chip detects Manchester-code bit violations as well as message collisions. It tolerates up to 125 ns of jitter on the received data and features a diagnostic loopback circuit that isolates the chip and detects faults.

The 82C550 connects directly to an Intel 82586 local network coprocessor. The serial interface chip also works with other popular data-link controllers and can, if necessary, drive external transceivers.

The chip responds to an external slew-rate control signal that allows it to produce differential outputs. It is available with either a CMOS or an RS422/485-level driver/receiver at the channel interface.

The 82C551 hub controller works with one upstream and up to eight downstream nodes. Five such controllers may be cascaded. The IC detects message collisions and generates collision-presence signals. It also retimes received data and retransmits it after removing accumulated jitter.

The controller's jabber circuit detects faulty transmissions that last longer than 65 ms, ignoring the communications until they cease. That ability helps isolate faulty nodes from the rest of the network.

The 82C550 is available in a 20-pin plastic DIP, and the 82C551 is available in a 40-pin plastic DIP. The former is priced at $15.60 each and the latter at $56.70 each, both in hundreds. The devices are available from stock in sample quantities.

Chips and Technologies Inc., 521 Cottonwood Dr., Milpitas, CA 95035; (408) 434-0600.

CIRCLE 302

Roger Allan

Controller puts PCs on DECnet

IBM PCs, XTs, and ATs can now participate in a DECnet—Digital Equipment's Ethernet local area network—using the Micom-Interlan NI5010 data link controller. Used in conjunction with DECnet-DOS software, the NI5010 plugs into the PC's internal bus to provide reliable 10-Mbits/s data communications. Versions of the controller are available with or without an on-board transceiver, priced at $650 and $550, respectively.

Micom Systems Inc., 4100 Los Angeles Ave., Simi Valley, CA 93062; (805) 583-8600.

CIRCLE 372

OSI software for Sun workstations

SunLink OSI is a networking package that supports the protocols of the ISO Open Systems Interconnect (OSI) reference model for multivendor communications. With it, users of Sun workstations in engineering, office, or factory environments can communicate with other vendors' equipment over an open network. The software product is based on the TOP (Technical and Office Protocol) specification and uses the IEEE 802.3 physical connection.

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, CA 94043; (415) 960-7533. $950.

CIRCLE 373

LAN controller serves VMEbus

Using carrier-band data transmission over the IBM cabling system, the NETPC/VME controller implements a token bus local area network for the VMEbus. It is especially useful for real-time applications where fast response times (under 10 ms) are required for many simultaneous transactions, such as data acquisition and control systems. The board includes a 68008 CPU and resident firmware.

Beal Communications, 9794 Forest Ln., Suite 246, Dallas, TX 75243; (214) 340-2044. $1795; stock to three weeks.

CIRCLE 374

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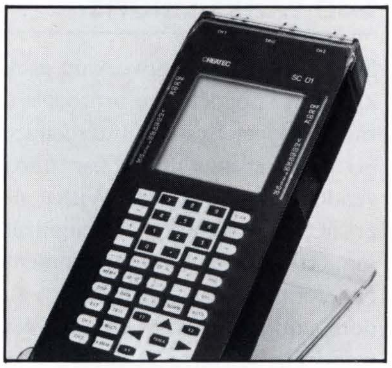
Electronic Design
P. O. Box 1036
Southeastern, PA 19398

20-MHz scope can be held in the hand

Weighing 700 g, a 20-MHz handheld digital oscilloscope measures 260 by 105 by 39 mm, consumes 3 W, and costs just DM 2500—around half that of the cheapest bench types. The two-channel scope, the SC01, from CPT Createc GmbH, shows its measurements on a 57.6-mm square, 128-by-128-pixel LCD readout.

The SC (Signal Computer) 01 has a single-shot mode and two trigger modes. It resolves 7 bits vertically, and gives a choice of 11 measurement ranges between 0.01 and 20 V/div. The vertical accuracy is within 1% ±1 LSB, and the linearity is ±1 LSB. The horizontal resolution ranges between 1 hour/div to



50 ns/div (for periodic signals) or 1 μs/div (single shot).

The instrument doubles as a transient recorder and an rms meter—between 1 Hz and 6 MHz, the typical accuracy is 0.06%. It can produce power diagrams, and can display true-RMS voltages.

Each of the input channels has a measurement amplifier that operates from dc to 10 MHz. These are followed by a flash converter that samples at 20 MHz and three digital processing controllers. The instrument features auto-calibration to ensure long-term reliability and accuracy, and there is a quartz-controlled time reference. The input impedance is 1 MΩ. The complete memory contents are held for three months by two NiCd batteries.

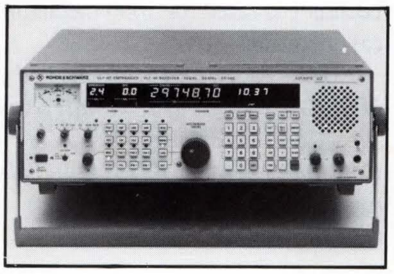
CPT Createc GmbH, Limburger Strasse 42, D-1000 Berlin 65, West Germany; (±49) 30 453 5083; Telex: 186 335 crea d.

CIRCLE 314

Receiver has 130-dB dynamic range

A VLF-HF receiver that can "hop" among 100 stored frequencies in the 10-kHz to 30-MHz band boasts a 130-dB dynamic range—thus working with an input voltage range three times higher than previous systems. In addition, Rohde & Schwarz's EK 085 tolerates signals up to 100 V on the input.

Aiming at communications and radio-monitoring, the unit receives amplitude-modulated, single-sideband and telegraphy (Morse and FSK) transmissions. It suits fixed or mobile receiving stations. The receiver tunes to each stored frequency within 50 ms, in a fixed order, with an accuracy down to 10 Hz.



Optional interfaces connect to teletypes and weather-chart and facsimile recorders; the unit can therefore print halftone pictures from satellites and weather stations. It stands alone, or fits easily into computer-controlled systems, across V.24, 20-mA current-loop, and X.21 interfaces. Optional are IEEE-488 and MIL-STD-1553B buses.

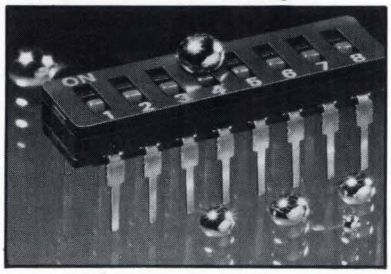
For time-programmed operation, the EK 085's integral digital clock lets channels be selected individually or automatically in a continuous sequence. Alternatively, a rotary knob can set the receive frequencies over the entire range in 10-Hz, 100-Hz, 1000-Hz, or user-programmable steps. A single receiver can address up to 99 others across a remote-control interface.

The unit accepts 100, 120, 220, or 240 V (47 to 420 Hz) or works from a 19-to-31-V dc supply.

Rohde & Schwarz GmbH & Co. KG, Muhldorfstr. 15, Postfach 80 14 69, D-8000 Munich 80, West Germany; (±49) 89 41292625; Telex: 523703.

CIRCLE 315

Immersible switches eliminate taping



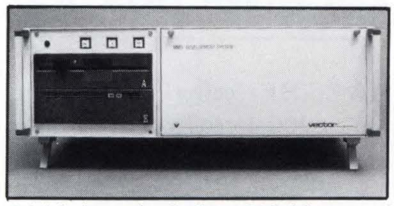
A range of subminiature DIP switches needs no protective taping during immersion cleaning. The Omron A6D switches have an inner rubber seal, and the cover and housing are joined by ultrasonic welding. There are 4-, 6- and 8-way versions of the switches, which may be top-or side-actuated. All device types have bifurcated self-cleaning movable contacts. The devices switch 100 mA at 50 V dc, and their life expectancy is rated for 5000 mechanical operations.

IMO Precision Controls Ltd., 1000 North Circular Road, Staples Corner, London NW2 7JP, England; (+44) 1 452 6444; Telex: 28514.

CIRCLE 375

Development system costs BFr 250 000

Costing from only BFr 250 000, a range of Concurrent CP/M-86 based development systems use 8088-based single-height Eurocards. The MMD16-DDS88 development system takes up to eleven



16-bit boards. It has 512 kbytes of RAM and two 800-kbyte microfloppies (one of which can be replaced by a 10-Mbyte hard disk). There is an extensive range of a-d and d-a converters, parallel I/Os, and other industrial cards, an optional EPROM programmer, as well as Basic, Fortran, and Pascal compilers.

Vector International nv., Research Park, B-3030 Leuven, Belgium; (+32) 16 20 24 96; Telex: 26202 vector b.

CIRCLE 376

INTERNATIONAL

Photoelectrics have built-in amps

A family of photoelectric switches with built-in amplifiers offers versions that use transmission, retroreflection, or direct-reflection methods for signal detection. Each unit in the G series is just 13 by 23 by 40 mm and is available in either a "head-on" or "side-on" mounting scheme. The detectors provide either light-on or dark-on operating modes via a switch setting and include a sensitivity adjustment.

All switches use an infrared LED light source and operate from a 12-to-24-V dc power source, consuming from 30 to 38 mA total, depending on model. The GT2 transmission type permits a distance of up to 3 meters between transmitter and detector units, while the retroreflection units (GR2) work over distances of 0.1 to 2 meters (using the company's K-2 reflector). The GR02 direct-reflection unit can operate at distances of up to 200 mm. The GT2 has a response time of 1 ms (max), while the other two respond in as little as 0.7 ms. All units can tolerate foreign light sources of up to 5000 lux and come standard with open-collector npn outputs, but pnp outputs can be specially ordered.

Takenaka Electronic Industrial Co. Ltd., 20-1 Narano-cho, Shinomiya, Yamashina-ku, Kyoto, Japan 607, (075) 581-7111, Fax (075) 501-6944. From ¥15,300 to ¥16,500 in small quantities.

CIRCLE 377

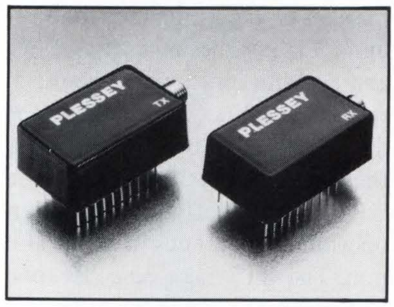
Card reads supply voltage/current

Voltages and currents of power supplies connected to the company's PC4400 controller system are read by a functional card that has a 12-bit a-d converter connected to a six-channel relay multiplexer. The PC4430 accepts a maximum input voltage of 500 V dc. It has two relays that can be used independently of the multiplexers to activate processes and to switch loads. The power supplies are controlled manually or across an RS-232-C or IEEE-488 interface.

Powerbox AB, Box 148, S-154 00 Gnesta, Sweden.

CIRCLE 378

Fiber-optic data link costs £90.

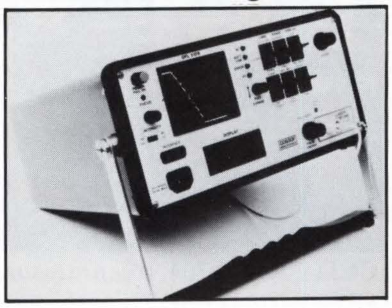


Transmitting at 50 Mbits/s using Manchester encoding and 125 Mbits/s using NRZ, a fiber-optic data link works over distances up to 2 km. The P35-8800 transmitter and receiver pair costs just £90 in quantities of 10,000 and suits local area networks, point-to-point data communications, computer links, and inter-rack telecommunications links. Each device has a hermetically sealed custom IC with either an LED or p-i-n photodiode housed in a 20-pin DIP. FMA interfaces allow a choice of optical fibers.

Plessey Optoelectronics, Wood Burcote Way, Towcester, Northants NN12 7JS, England; (+44) 327 51871; Telex: 312428.

CIRCLE 379

Cable fault locator has 20-dB range



The 20-dB dynamic range of an optical-cable fault locator is wide enough to attach to 24 miles of 130-nm single-mode fiber. The locator, which is designated the Model 2135, has an accuracy better than ±0.1 dB. It is portable, and its rechargeable batteries provide at least three hours of continuous use. The instrument performs splice- or connector-loss measurements automatically.

Cossor Electronics Limited, The Pinnacles, Elizabeth Way, Harlow, Essex CM19 5BB, England; (+44) 279 26862; Telex: 81228.

CIRCLE 380

Current source remains stable

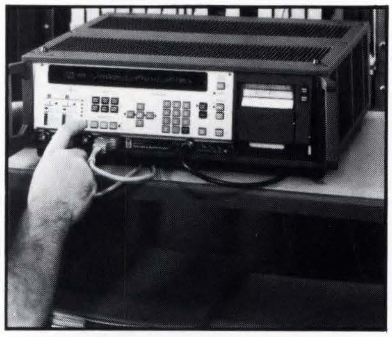
The KS-03 constant-current generator provides a precision voltage reference between 1 μV and 200 mV. The instrument's accuracy suits it to laboratories. It offers a stability of 30 ppm/day and a temperature coefficient of 20 ppm/°C. A 10-turn potentiometer is used to adjust the current between 0 and 199.9 mA in three ranges, to an accuracy of ±0.1% + 1 digit. At the 200-mA maximum current, the current-generator's output voltage is at least 25 V. At 2 mA, this rises to 40 V, allowing it to test relays and small dc motors. The instrument can also be controlled by devices that generate a 0-to-2-V signal, such as stepping motors. The output current is shown on a 3½- digit LED display. Additionally, there is an overload warning light.

Datasem GmbH, Richthausener Str. 2, 8501 Winkelhaid, W. Germany; (+49) 9187 3222; Telex: 179187812 dasem+.

CIRCLE 381

Frame analyzer monitors two signals

Monitoring two 2.048-Mbit/s multiplexed signals simultaneously, a frame analyzer allows a wide range of testing, monitoring, and signal generation; it can also print out error events. The PRA-1 has two independent receiver sections and works with signals having a frame structure according to the



CCITT Rec.G.704. It can measure all important telephone channel parameters and can monitor acoustic channels and signal alarms. An integral generator section makes loop–through measurements while the instrument is in service. The instrument measures input voltages between 30 mV to 3 V and consumes 120 VA maximum.

Wandel & Goltermann, Postfach 45, Muehleweg 5, D-7412 Eningen, West Germany; (+49) 7121 891570.

CIRCLE 382

Adapter gives IBM PC 16 colors

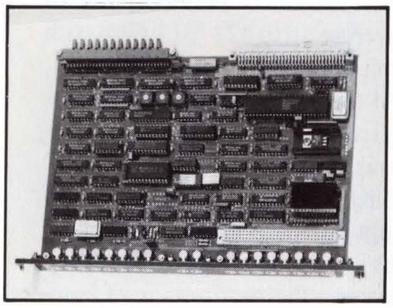
An IBM-PC graphics controller board offers the choice of 640-by-350-line monochrome, 320-by-200 or 640-by-200 16-color graphics, or 640-by-350 16-color enhanced graphics. Any color attribute can be mapped to the EGA (Enhanced Graphics Adapter), and the RAM-based character generator stores up to 512 character codes. Smooth horizontal and vertical scrolling are provided in hardware, as are split-screen displays. The board costs $450.

Multitech Industrial Corp., Chien Kuo North Road, Taipei, Taiwan, R.O.C.; (+886) 2 501 0055 Telex: 19162/23756 MULTIIC.

CIRCLE 383

CIRCLE 197

Board extends color range



A VMEbus board converts an 8-bit video input (from a suitable graphics board) into an output of up to 256 colors from a 256,000-color palette. The ULUT1/68K has pixel rates up to 55 MHz and features a variety of functions that suit animation and overlays. The board can synchronize graphics hardware to an external CCIR-compatible source. In stand alone mode, it supplies the sync signal itself. The board has a hardware look-up table, while a programmable interrupt controller can generate interrupts, either synchronized to the horizontal or vertical pulses, or under timer control. There is a buffered RS-232 port.

Eltec Elektronik GmbH, Galileo-Galilei-Strasse 11, D-6500 Mainz 42, West Germany; (+49) 6131 50031.

CIRCLE 384

Rotary switch offers sequential switching

A subminiature rotary code switch provides any number of binary, binary complement, hex, and hex-complement coded outputs. Types with 10-, 12- and 16-position indexing will soon follow, allowing sequential switching from 1-pole 11-way up to 3- and 4-pole 8-way. The SRC switch is rated at 50 V and 500 mA; with a maximum load of 10 VA, it offers an initial contact resistance of under 50 mΩ. The switch can be mounted on a pc board or attached to a panel using a threaded bush. It comes in a polycarbonate enclosure, has gold-plated contacts, and sports a shaft and bush of stainless steel.

Ledex Inc., P.O. Box 427, 801 Scholz Dr., Vandalia, OH 45577; (513) 898-3621; Telex: 28-8228.

CIRCLE 385

Lucas NSF Ltd., Ingrow Bridge Works, Ingrow La., Keighley, W. Yorks BD21 5EF, England; (+44) 535-661144; Telex: 51270.

CIRCLE 386

Meters eliminate ground loops

Eliminating ground-loop interference from voltage and phase measurements, two instruments work on the IEEE-488 instrumentation bus and show readings on a 3½ digit display. The 2432 digital voltmeter has a frequency response between 5 Hz and 25 kHz that is linear to within ±0.15 dB, with a −0.5 dB limit at 2 Hz and 500 kHz. The instrument shows rms or peak voltages in volts or decibels. It can also be used as a calibrated amplifier when it amplifies the input signal in steps of 20 dB ±0.02 dB. The 2977 phase meter's display and dc outputs are scaled in radians or degrees and there are center- and end-zero phase ranges. The meter can be triggered by signals only 1.4-mV strong with a trigger delay of up to 163.8 ms.

Bruel & Kjaer, 18 Naerum Hovedgade, 2850 Naerum, Denmark; (+45) 2 800500; Telex: 37316 bruka dk.

CIRCLE 387

COMPUTERS & PERIPHERALS

Vector-scalar processor runs at 424 MFLOPS

Parallel vector processing is no longer limited to small numbers of parallel processors. Intel's iPSC hypercube architecture now can accommodate up to 64 nodes, each containing a scalar processor and a vector processor, making up a complex computing surface. With 64 nodes, the iPSC-VX is capable of delivering up to 424 MFLOPS with 64-bit precision.

At the node level, users can automatically partition Fortran programs into scalar and vector processing portions. Thus, the speed of computationally intensive applications can be significantly increased. However, the partitioning of computations into parallel or concurrent processes brings the real potential for improved speed. Similar processes can be executed concurrently on the iPSC-VX's nodes. Many problems, like circuit simulation, matrix manipulation, and large-scale modeling, lend themselves to division into concurrent processes.

Three versions of the iPSC-VX are available: a 16-node, a 32-node, and a 64-node system. Within each node, the scalar processor consists of an Intel 80286 processor, a communications interface to the processing network, and a common 1.5-Mbyte node memory. Each node's vector processor supports a 128k by 64-bit vector data memory which drives a floating-point arithmetic unit.

Each processor is contained on a single Multibus board, with the individual units connected via the iLBX backplane interface. The 80286 serves as the node controller and communicates with the iPSC-VX system via its nearest neighbors.

A 16-node system with a host controller is priced at $250,000; a 32-node system, at $450,000; and a 64-node system, at $850,000. Delivery will be in the third quarter of this year.

Intel Scientific Computers, 1520 N.W. Greenbrier Parkway, Beaverton, OR 97006; (503) 629-7629.

CIRCLE 306

NEW PRODUCTS

COMPUTERS & PERIPHERALS

Computer develops 1750A programs

An add-on to an IBM PC XT or AT, the MKS1750/AT, develops and debugs application programs built around the MIL-STD-1750A 16-bit instruction-set architecture used by the U.S. Air Force. The standard is mandatory for all avionics systems, including aircraft, missiles, munitions, and their associated test equipment. The IBM computer acts as the host. Programs developed on that computer are downloaded to the MKS1750/AT for testing and debugging using Mikos Systems' proprietary software.

Mikros Systems Corp., 3828 Quakerbridge Rd., Mercerville, NJ 08619; (609) 890-0440. $12,500.

CIRCLE 388

Backlight brightens computers' LCDs

A backlighting system, which can be retrofitted to most name-brand portable computers with liquid-crystal displays, allows the display to be easily read under any lighting condition. The retrofit consists of a thin-film electroluminescent panel, control electronics, and where appropriate, conversion of the computer's battery pack to rechargeable NiCads. Installation of the Thin E/L backlight is performed at Axonix, with a guaranteed turnaround time of one week.

Axonix Corp., 417 Wakara Way, Salt Lake City, UT 84108; (801) 582-9271. From $200 to $350, depending on computer.

CIRCLE 389

Touch screen gives 96 discrete pads

A capacitance touch screen offers 96 discrete pads arranged in custom layouts or a standard 8-by-12 grid. A controller for the screen facilitates dynamic baseline adjustments and includes a watchdog timer, automatic baud-rate detection, a test mode, 500-μs scan time/pad, an external reset, and a valid-touch feature. Screens are available for most monitors from 12 to 19 in., both spherical and cylindrical, as well as flat-panel displays.

RGB Dynamics Inc., 419 Wakara Way, Salt Lake City, UT 84108; (801) 584-2550. From $150 to $795.

CIRCLE 390

Minicomputer bests VAX-11/780 speed

A new member of the VAX minicomputer family, the VAX 8500, offers enhanced performance but at the same price as its predecessors, the VAX-11/780 and VAX-11/785. The new computer comes in a compact package that occupies just 5.6 ft^2 of floor space, or one-third the footprint of the VAX-11/785. The 32-bit system uses the VMS operating system and comes with the VAXBI interconnect bus. One VAXBI channel is standard.

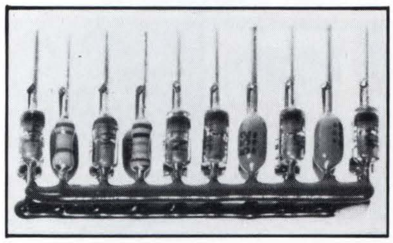
Digital Equipment Corp., 146 Main St., Maynard, MA 01754; (617) 897-5111. From $260,000.

CIRCLE 391

COMPONENTS

Simple solution terminates ECL

Emitter Coupled Logic (ECL) delivers high speeds, but demands careful use. To prevent excessive ringing during its relatively low logic swings, many designers are forced to use termination networks. Until now, effective termination required expensive Schottky diodes to clamp both swings of a logic signal. RPM has developed a termination network, DM310BT-100, that uses standard diodes.



By forward biasing the diodes, switching speeds can match the fast, but more expensive, Schottky diodes. The SIP network supplies six ECL terminations, each composed of two biased diodes tied to the two common voltage rails. The voltage rails, one for logic high and one for logic low, use resistors to forward bias the diode pairs that form the termination, thus clamping the ECL logic signal and linking the rails. The rails are decoupled with capacitors to reduce crosstalk and switching noise.

Because these termination networks are made up of off-the-shelf parts, turn around times for delivery are very short, averaging two weeks or less. For the same reason, custom termination networks can be put together in the same time frame with small variations in cost.

A termination for a 10K ECL circuit, with signal run length of 6 in., will consist of: two pair of resistors (50 ohms and 100 ohms), a group of capacitors (0.01 pF each), and 6 sets of paired diodes (1N4150).

The DM310BT-100 sells for $2.50 each in 1,000 lot quantities. They are delivered within two to three weeks of an order.

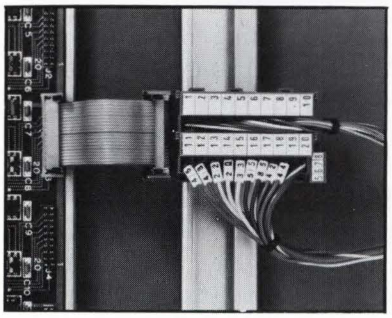
RPM Enterprises, 1583 Saint Gertrude Pl., Santa Ana, CA 92705; (714) 556-8940.

CIRCLE 316

NEW PRODUCTS

COMPONENTS

Terminal unit links pcb to hard wiring



A series of plug-in modular terminal blocks permits quick connect/disconnect of pc board electronics to discrete hard wiring. The WKB2.5ST/U series can be assembled to any standard DIN asymmetrical or symmetrical rail. It mates standard electrical circuits (up to 12 AWG) with pc board electronics through the use of a flat ribbon cable connector (20- and 40-pole versions) or a plug-in mating connector (10-pole version). All metal parts are deeply recessed or completely enclosed for dead-front safety. No covers or lugs are required.

Electrovert Inc., 466 Main St., New Rochelle, NY 10801; (914) 633-0222. $29.34 (100 units); stock.

CIRCLE 392

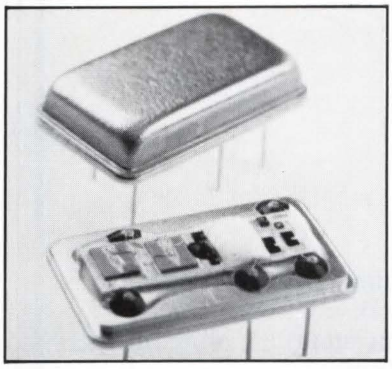
P-i-n diodes switch in <3 ns

The HPND-4028 and -4038 beam-lead p-i-n diodes are designed for fast switching at microwave frequencies. Switching speeds of 2.6 and 2.4 ns are combined with low resistances of 2.3 and 1.5 Ω (4028 and 4038, respectively), while operating at a low bias of 10 mA. With a reverse voltage of 30 V at 1 MHz, capacitance is 0.045 and 0.065 pF maximum for the 4028 and 4038, respectively. Their breakdown voltage is 60 V with reverse current less than or equal to 10 μA.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, CA 94303; call local sales office. $8 (4028) and $7.60 (4038) in lots of 1000 units.

CIRCLE 393

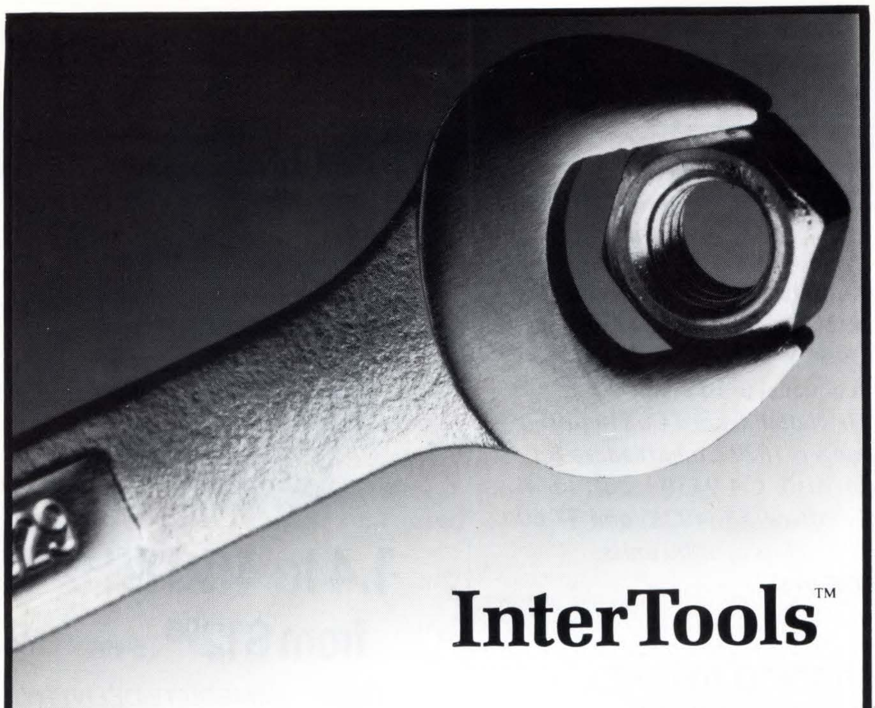
Switching hybrid replaces relays



High-speed, optically-coupled switching hybrids, the M855VF-1 and M85VF-2, use power-FET outputs to minimize on-state resistance and eliminate the bipolar offset voltages normally associated with solid-state relays. The devices are designed for low-level switching applications and use an optically-isolated input and output to protect delicate TTL-compatible logic circuits from voltage transients. Typical rise times are 0.43 to 0.80 μs; fall times are as fast as 0.2 μs. The M85VF-1 is rated at 0.75 A at 60 V dc. The M85VF-2 handles 1.35 A at 60 V dc. Both are housed in hermetically-sealed 14-pin DIPs.

Teledyne Solid State, 12525 Daphne Ave., Hawthorne, CA 90250; (213) 777-0077. $117.50 to $126.75 (250 units); four to six weeks.

CIRCLE 394



NEW PRODUCTS

COMPONENTS

Internal seals save DIP switches

Internal sealing in the A6D and A6DR subminiature DIP switches protect the devices during soldering and the immersion cleaning process. Prior taping is unnecessary. The A6D is a top-actuated switch that comes in 2-to-10-pin versions and can be magazine-loaded for automatic insertion. It stands just 0.13 in. above a board. The A6DR is a side-actuated switch available in 4-, 6-, and 8-pin versions. It has a 0.29-in. above-board height. All models feature bifurcated, self-cleaning, nickel-plated beryllium-copper contacts with a switching capacity of 100 mA at 5 V dc and 30 mA at 30 V dc.

Omron Electronics Inc., One E. Commerce Dr., Schaumburg, IL 60195; (800) 626-6766. From $1.02 (4-pin) (1000 units); stock.

CIRCLE 395

LIF connector has spring-pin contacts

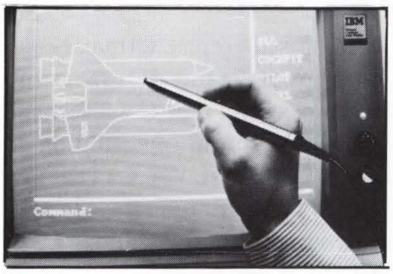
Microminiature connectors with proprietary spring-pin contacts require less than half the insertion force than connectors with twist-pin contacts. The Mite-Y-Pin stamped contact employed in the Microcon rectangular-D, strip, and circular connectors provides a uniform nose design not possible with the welded-wire bundles of the twist-pin contact. Pricing for a typical configuration is $0.62 per position for a two-row, 25-position EP series (plastic D, class P) connector with harness wire (lots of 1000).

Elco Corp., Huntingdon Industrial Pk., Huntingdon, PA 16652; (814) 643-0700.

CIRCLE 396

SOFTWARE

Light pen control comes to AutoCad



A driver program, called PenCad, adds light-pen control to the popular computer-aided design program AutoCad. The driver allows users to draw with precision directly on the display monitor. A file can be retrieved simply by touching the pen to the file name on the screen. The software requires 10 kbytes of memory. PenCad works in conjunction with the Phaser One single-pixel resolution converter card. The device converts the light-pen port on a graphics adapter card for such improved resolution.

Warp Speed Computer Products Inc., 5555 S. Inglewood Blvd., Los Angeles, CA 90230; (800) 874-4315 or (213) 822-0647. $99.99 (PenCad); $99.99 (Phaser One); stock.

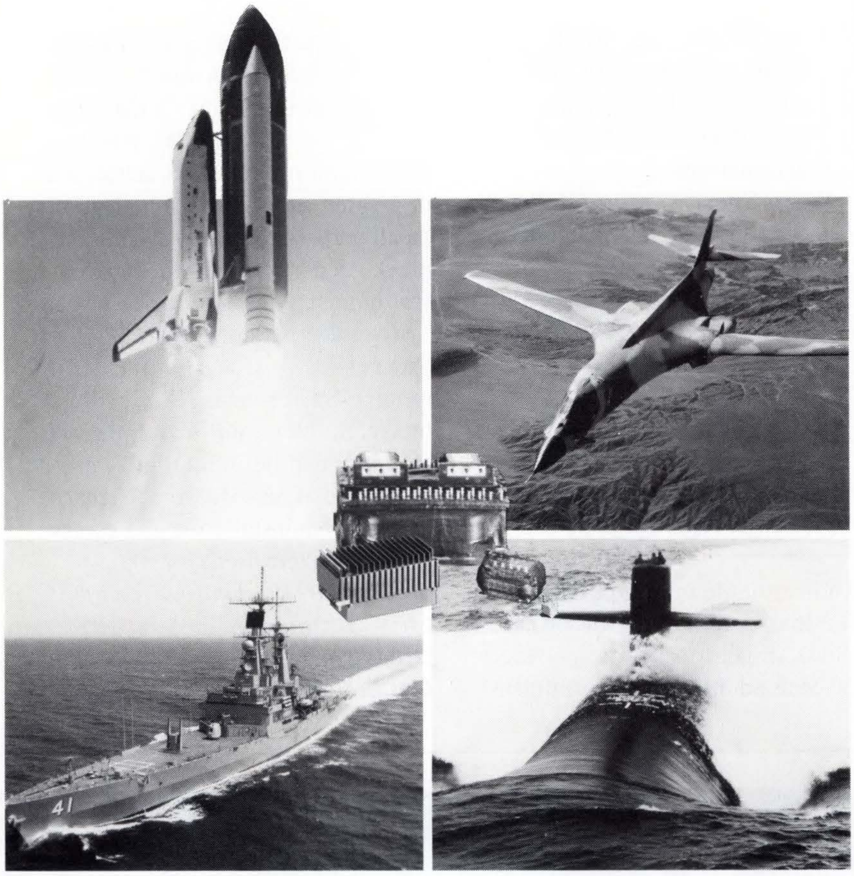
CIRCLE 397

Interrupt driver adds serial ports

An installable interrupt driver for multiple serial-port expansion cards allows standard software packages to access additional ports on an IBM PC or compatible computer by simply using COM3 through COM8 (instead of the usual COM1 and COM2) names. ID8000, which is suitable for use under PC-DOS 2.0 or greater, supports communication on all ports simultaneously (full duplex). All ports support modem control handshaking. Interrupt levels can be selected, along with I/O port addresses and transmit- and receive-buffer sizes. Baud rates, bits/character, and the number of stop bits can be individually programmed. The software features menu-driven installation and comes with a complete user's manual.

Star Gate Technologies, 33800 Curtis Blvd., Suite 109, Eastlake, OH 44094; (216) 951-5922.

CIRCLE 398



NEW PRODUCTS

SOFTWARE

Emulator gives PC access to VAX

A PC-based graphic terminal emulator gives circuit designers full desktop control over Case Technology's CAE programs running on VAX or MicroVAX systems. Called G Term/E Term, the software lets designers use an IBM PC, XT, or AT as a graphics window into the VAX or MicroVAX-based system. The full computational power of the VAX can be used to perform design compilation, simulation, and automatic routing, while the results are viewed interactively on the PC.

Case Technology Inc., 633 Menlo Ave., Menlo Park, CA 94025; (415) 322-4057. $2500 per terminal.

CIRCLE 399

Software aids icon development

Called Icon Builder, this software package helps define graphic images, or icons, that can be printed, overlayed on the surface of a digitizing tablet, and used to construct icon-oriented user interfaces. The program provides a template editor for defining arbitrary rectangular regions on the digitizer-tablet surface that will be associated with keystroke sequences that are returned to any standard MS-DOS application program when a rectangular region is selected by the user. The program comes in four modules: the graphics editor, the template editor, a template installation program, and an overlay print program.

White Sciences Inc., P.O. Box 24756, Tempe, AZ 85282; (602) 967-8257. $79.95.

CIRCLE 400

SOFTWARE

Compiler-simulator aids PLD design

Perfect, a programmable logic compiler and timing simulator, offers high-level design flexibility for all popular programmable logic devices. With it, designers may define complex designs via Boolean logic entry, state machine syntax, truth table input, or schematic entry via Valley Data's Vista PLD/CAD software. It also permits accurate modeling of both asynchronous and synchronous circuits.

Perfect is available as a standalone product for the IBM personal computer family at $995 and for Unix 4.2 BSD systems at $2495. It may also be purchased bundled with the Vista software package starting at $3650.

Valley Data Sciences, 2426 Charleston Rd., Mountain View, CA 94043; (415) 968-2900.

CIRCLE 401

Program compares theory and practice

The KIT-MAS software program transfers modal analysis results from an ANSYS finite element model to the data base of the SMS Structural Analysis System (SAS 3.0). By moving the mainframe- or minicomputer-based ANSYS results to an SAS data base on the HP 9000 Series 200 or 300 desktop computer, users may compare both the analytical and the experimental modal data. A side-by-side comparison of the shapes is accomplished using the real-time display features of SAS. Users may also analytically modify the finite element model in a fraction of the time it would take to rerun the entire model.

Structural Measurement Systems Inc., 645 River Oaks Pkwy., San Jose, CA 95134; (408) 263-2200.

CIRCLE 402

Program exchanges PC, HP files

With File/Swap PC, IBM PC users can move their MS-DOS files to a Hewlett-Packard computer without having to port the data serially. The program enables the IBM machine to format 5¼-in. disks that the entire range of HP technical/LIF family computers can recognize. It writes either interchange or native language for the target HP system, automatically recognizing files produced by most word processors in MS-DOS and HP environments. It also allows HP CP/M files to be copied to MS/PC-DOS.

A Gentle Wind Inc., P.O. Box 3103, Albany, NY 12203; (518) 482-9023. $189.

CIRCLE 403

Ada compiler runs on IBM PC

An Ada compiler for IBM PC, XT, AT, and compatible computers is now available for $895. The compiler meets virtually all of the latest DOD specifications for Ada, except tasking, and it requires at least 384 kbytes of memory. Hard-disk mass storage is recommended for the development of larger applications. The package includes a compiler, full-screen editor, interpreter/debugger, linker, library manager, and A-code (pseudo-code) disassembler. The latter allows sophisticated debugging with single-step trace and display of registers and data, plus breakpoints on specific source lines.

Artek Corp., 100 Seaview Dr., Secaucus, NJ 07094; (201) 867-2900.

CIRCLE 404

READER FEEDBACK

(continued from p. 121)

final" would that model have been before samples of the IC were available?

If the IC manufacturer will not provide the models, the user community is back to where the functional automatic test community had been for years—model it yourself.

The need for LSI models was first felt in the ATE community in the mid-1970s, when LSI was born. Designers could be taught to use an 8080, but the ATE community, which had gotten used to simulation and fault simulation, began to feel frustrated. In fact, I believe that the lack of available LSI models was one of the key factors in the growth of in-circuit pc board ATE at the expense of the functional technique.

The first attempts at physically modeling a device by using the device itself began about 1976 when Richard Hartman, and others at Pacific Applied Systems, worked with the TASC simulator. They had limited success, due to the state of hardware and computing power available then.

Modern implementations, such as the CATS-Dynamic Hardware Modeler that we at HHB Systems have developed, allow modeling as a hybrid between the physical IC's performance and a surrounding software "shell", which mitigates the interface to the software simulator. This gives the user the ability to begin with the basic IC and then progress by adding increasingly sophisticated software functions as the need requires (and time allows) to handle "X" or unknown states—the bane of hardware modelers. A physical IC never has an unknown state; it will always yield an answer of logic zero, one, or three-state, even if there is no prejustification for the state, such as a memory cell that was never written to.

The software that surrounds the physical model can be trained to handle these cases to whatever level of sophistication that the user needs. The net result is a usable model that is quick to produce and does deal with more than just the "ones and zeros."

It is just this "temporary fix" of physical modeling that has enabled us to simulate and fault-simulate the IBM PC XT motherboard using five physical models concurrently in a full simulation of the circuit. We find that we can produce a basic model of a VLSI IC in as few as four man-days, while the average for models of mercantile quality is three man-weeks.

While I agree that Intel should ideally supply the world with complete models of all of these ICs, I fear that Mr. Van Brunt and I will probably retire first.

James E. Scharf
Vice President of Advanced Research
HHB Systems
Mahwah, N.J.

Mr. Van Brunt replies: *There is no perfect or universal modeling system. Designers must address their modeling requirements as dictated by their designs, the design methods employed, and the design tools available. By selecting suitable modeling methods—including behavioral, physical, structural, and switch-level, or a combination of these methods—designers are able to accurately simulate the logic and faults of their designs and to deliver quality products. Good modeling is one of the remaining large unsolved problems in electronic design. Let us hear from others on these modeling issues.*

PRODUCT NEWS

Publishing firm offers first software

To bridge the gap between independent software developers and end-users, **Graham Software Corp. (Toronto, Ont., Canada)** provides a vehicle for which these companies can market and distribute their products worldwide. The international software publishing firm has released two software programs that are already receiving wide market acceptance: Alice: The Personal Pascal and Intellisys. The latter allows users to develop applications for DEC processors without having to write programs or learn a programming language. The former is a complete programming system for developing personal computer applications. It is marketed through Graham's wholly owned subsidiary, Software Channels Inc.

CIRCLE 405

IBM LAN expands connectivity

Enhancements to **IBM Corp.'s (Rye Brook, NY)** token-ring local area network allow users to share the resources of a wider range of information processing equipment, including IBM System/370 host processors and System/36 computers. They also extend the distances over which networks can operate and allow multiple token-ring networks to be linked together. The company also announced a price reduction for IBM PC Network adapter cards—from $645 to $595—as well as enhancements that allow two PC Networks to be connected.

CIRCLE 406

Enhancements optimize touch display

A second generation of its totally integrated touch terminal, called Touch Information Display (TID), allows **Electro Mechanical Systems Inc. (Champaign, IL)** to offer a greatly enhanced design without increasing the price. Previously unavailable features include a Screen Saver function for longer CRT life, expanded terminal and touch commands, and built-in diagnostics and maintenance routines. New options include 16 pages of downloadable display memory and an RS-422 port for noisy environments. Single unit prices start at $1400, plus $150 for optional memory.

CIRCLE 407

8-bit microcontroller is second-sourced

Now in production as an alternative source, **Advanced Micro Devices Inc. (Sunnyvale, CA)** offers a plug-in replacement for Signetics' 8X305 8-bit microcontroller. Like the 8X305, the Am29X305A supports a 200-ns cycle time. The company is producing the device using its bipolar IMOX technology and will provide both ceramic and plastic DIP versions. In ceramic, the microcontroller costs $29.70 in lots of 100 units.

CIRCLE 408

ELECTRONIC DESIGN

ELECTRONIC DESIGN's function is:
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PRODUCT NEWS

Plastic DSP components prove reliable

A line of digital signal processing components is now available in plastic packages and provides reliable performance at competitive prices. **Analog Devices Inc.** (**Norwood, MA**) has developed an overcoat process which protects the device against damaging moisture effects, thus increasing the reliability of plastic-packaged monolithic parts. The components have proven reliable in 1000-hour life tests at 85% humidity and 85°C temperatures. The company has also priced some models as much as 21% below their ceramic-packaged counterparts. The plastic-packaged ADSP-1010A is now priced as low as $75 in lots of 100, compared to $95 for ceramic versions.

CIRCLE 409

Second source named for octal UART

Digital Equipment Corp. has licensed **Standard Microsystems Corp.** (**Hauppauge, NY**) as a second source for its 78808 octal UART (universal asynchronous receiver transmitter). Standard Microsystems will market the device under the part number COM78808. The octal UART is assembled in a proposed JEDEC-standard 68-pin chip carrier.

CIRCLE 410

Computer option wards off power problems

To ensure continuous performance in the event of a power outage, surge, or sag, **L/F Technologies Inc.** (**Carson City, NV**) has developed an uninterruptible power supply option for its line of multiuser microcomputers and terminals. Called L/F-Power, the option provides battery-stored backup power—for up to one hour—from within the 30-user microcomputer. L/F-Power II is built into each terminal and maintains power to the keyboard and screen. Together, they give users plenty of time to transfer data from main memory to disk.

CIRCLE 411

Silicon software supports 68020

Expanding its support for the Motorola MC68000 family, **Software Components Group** (**Santa Clara, CA**) has released pSOS, pROBE, and pHILE silicon software components for the MC68020 32-bit processor. Each component is a plug-in object code module free of any dependencies on target hardware, memory location, or application. The pSOS multitasking kernel, pROBE system debug/analyzer, and pHILE file system manager are available on PROM, disk, or tape and are upward compatible with versions that support the 68000 and 68010 microprocessors. Each development package costs $3000, which includes 10 binary copies.

CIRCLE 412

Plastic drive components

Over 12,000 off-the-shelf inch and metric drive components are contained in a 304-page handbook (No. 762) of plastic components. Thirty-five pages are devoted to design procedures for spur, helical, bevel, and worm gears. A useful series of tables covers American/metric gear equivalents, decimal and metric equivalents, plus conversion of both small inch and metric measurements. Product sections describe plastic gears, couplings, and universal joints; belt and chain drives; miscellaneous components; and fasteners.

Designatronics Inc., Stock Drive Products, 2101 Jericho Tpke., New Hyde Park, NY 11040; (516) 328-3330.

CIRCLE 413

Epoxy selector guide

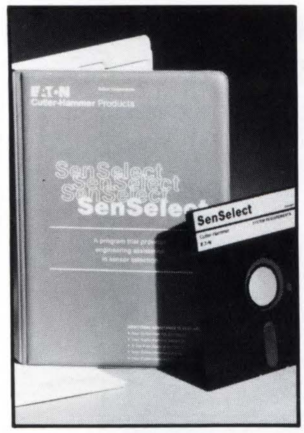
A selector guide for casting, embedding, and adhesive materials features over 50 well-defined, easy-to-select one- and two-component epoxy systems with typical electrical, thermal, physical, and processing properties. Test methods used in determining properties are given. Two full pages are devoted to troubleshooting, giving causes, effects, and corrective actions for more than a dozen common problems. Another section offers information on cleanliness, mixing, deairing, application, storage, and packaging.

Furane Products Co., 5121 San Fernando Rd. W., Los Angeles, CA 90039; (818) 247-6210.

CIRCLE 414

Free software aids sensor selection

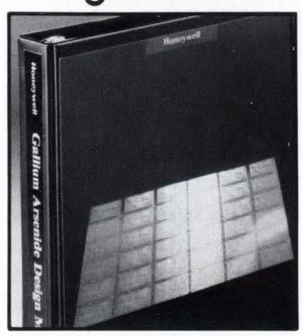
A free software package provides a complete menu of application considerations to simplify the selection of proximity and photoelectric sensors. Called Senselect, the floppy-disk software runs on IBM PC and compatible computers. It leads the user through a series of steps to make complex selection decisions understandable. Users can even input "what if" alternatives.



Eaton Corp., Cutler-Hammer Products, 4201 N. 27th St., Milwaukee, WI 53216; (414) 449-6000.

CIRCLE 415

GaAs IC design manual



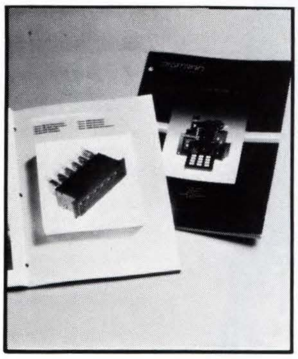
Honeywell is offering a design rule manual to help potential foundry users design GaAs integrated circuits. The manual (HGD-1000) documents minimum geometries needed to yield functional devices. Basic device structures are also detailed to aid in the construction of circuit elements.

Honeywell Inc., Gallium Arsenide IC Product Center, 830 E. Arapahoe Rd., Richardson, TX 75081; (303) 577-3511. $500, including updates for two years.

CIRCLE 416

NEW LITERATURE

Digital switches



Digitran's design catalog covers one of the most complete lines of digital switches in the industry, including Digiswitch, Minilever, Digivider, and Digidecade families, as well as Minikey keypad systems. The guide to military and commercial switch selection provides a features and options chart, truth tables by product series, and engineering parameters and layout drawings for thumbwheel switches, lever/toggle switches, push buttons, custom products, and accessories.

Digitran Co., 3100 New York Dr., Pasadena, CA 91107; (818) 791-5600.

CIRCLE 417

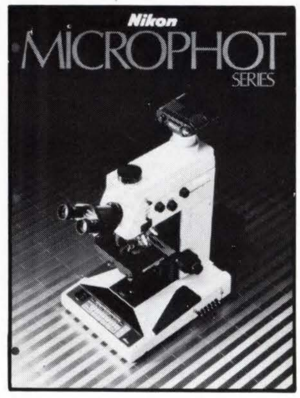
Burn-in/test sockets, carriers

The 1986 Welcon catalog provides detailed specifications on a line of burn-in and test sockets, contactors, and carriers. New products include a family of leadless and plastic leaded chip carrier sockets, a 132-lead quad pack contactor and carrier, DIP sockets, and carriers molded of ESD. These products are available in numerous body and contact materials, as well as platings.

Wells Electronics Inc., 1701 S. Main, South Bend, IN 46613; (219) 287-5941.

CIRCLE 418

Research microscopes



An eight-page color brochure details the optical, mechanical, and electronic features of Nikon's Microphot series of advanced research microscopes. Also featured is a wide assortment of interchangeable accessories.

Nikon Inc., Instrument Group, Inquiry Response Center, P.O. Box 52, Oceanside, NY 11572; (516) 222-0200.

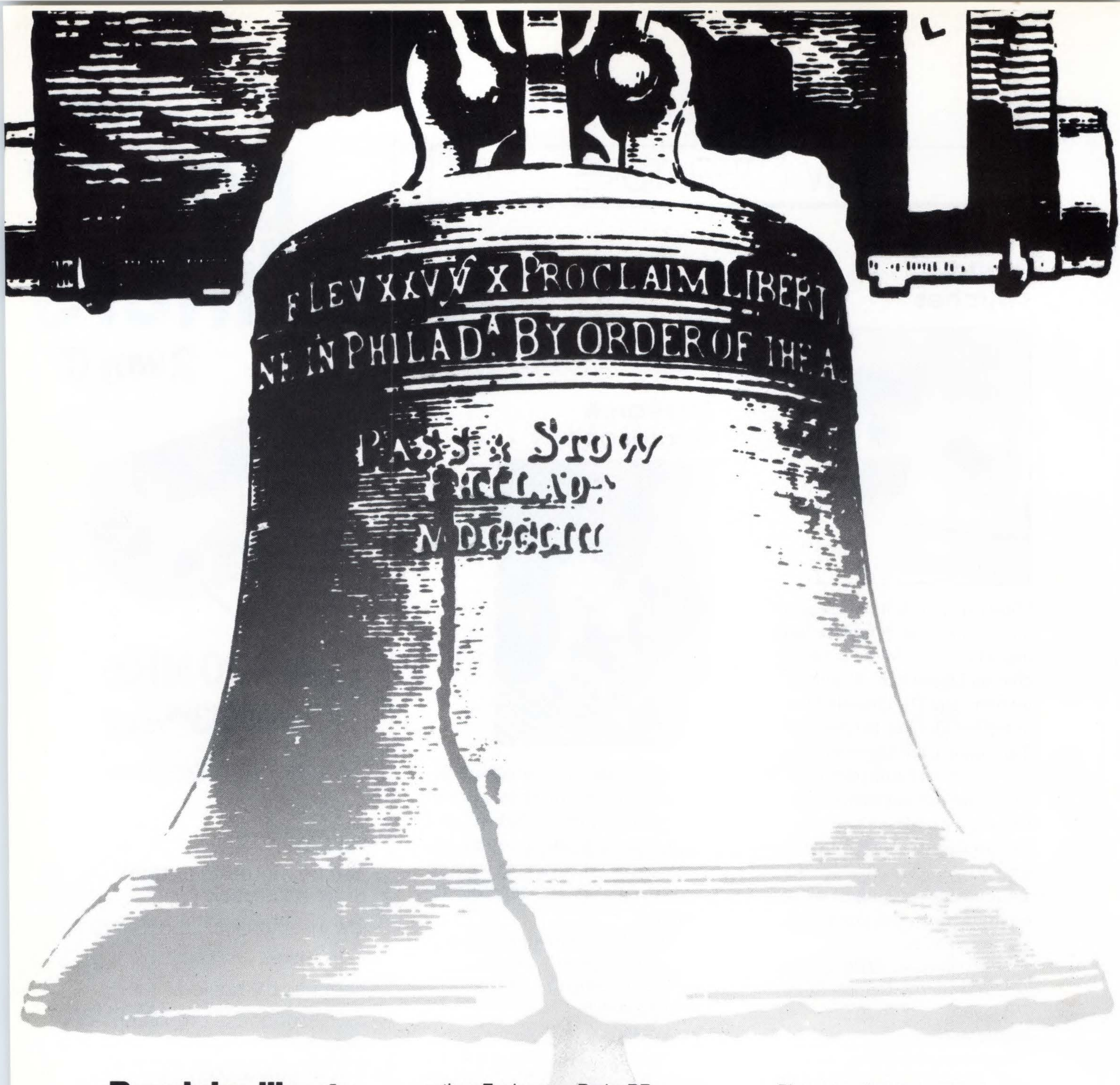
CIRCLE 419

Time delay relays

Magnecraft's latest catalog provides a complete specification section that is common for all time delay relays. To ease the selection process, an index includes the most relevant information, eliminating information that is standard on all the time delays.

Magnecraft Electric Co., 5575 N. Lynch Ave., Chicago, IL 60630; (312) 282-5500.

CIRCLE 420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PROFESSIONAL NOTEBOOK

CAROLE PATTON

You can't teach an old dog new tricks . . . just ask any old dog

A stereotype, says my copy of Webster's, is a standardized mental picture held in common by members of a group and representing an oversimplified opinion. Consider, for example, the following stereotypes:

***Young engineers:** They are eager to work and anxious to please—a pleasure to manage. They bring new and up-to-date technology to an organization. They cost less, tend to work harder, and are more creative, than their senior cohorts.*

***Middle-aged engineers (ages 35–50):** They suffer from burnout because they haven't realized their career expectations. They don't get raises as often as they used to. They have trouble learning how to use complicated new devices like engineering workstations.*

***Older engineers (50–60):** They don't necessarily want higher levels of responsibility or salary; job success is not as important as personal lifestyle. They do not want to work long hours or weekends. They are intolerant of younger managers and even of younger engineers. Management must figure out either how to move them into new situations or how to move them out of the organization altogether. In fact, older engineers cause so many problems that managers really do earn their high salaries just figuring out how to cope with them.*

In the past, I've pondered how stereotypes like these originate, how they infiltrate our minds and attitudes like poison-pen letters. Two weeks ago, at a joint conference between the IEEE and the National Council on Aging, Grumman vice president of personnel Dan Knowles lent his insight: Discrimination based on age, Knowles said is more insidious than other types because it is perpetuated by older workers themselves.

Knowles added that people are rarely aware they are discriminating against older workers. "There are no significant differences between older and younger workers; the belief that differences exist is the biggest myth of all, " he stated flatly. But what an unfathomable waste of ability and potential. Does it all boil down to a "Pepsi generation" mentality? Is biological bigotry worth the cost?

By the way, the quaint views paraphrased above, vividly describing how eager-beaver youths differ from burned-out relics, have their origins at the same age discrimination conference. I drew the descriptions from a speech called "The Impact of Technical Vitality on Managing Professional Careers." Its author, Robert Tanner—a "vintage" engineering manager—believes vitality is the stronghold of youth. And so, the myth is perpetuated.

Supermarket sweeps may soften U.S. trade deficit

Remember the TV game shows in which contestants madly raced against the clock to fill their shopping carts? In TV-land, the winner was the shopper whose checkout bill totaled the most. Wasn't it fun to watch those housewives grabbing for the roast beef?

What a shame that we didn't get to view the latest 1980s version of a supermarket sweep—an $80 million spending spree by Hitachi. It wasn't televised, but here is the scenario: On April 17 a 16-member purchasing team led by Hitachi executive vice president Shiro Kawado set off on a 10-day U.S. shopping tour. No one-stop shoppers among them, Kawado's group made a whirlwind tour of 51 companies in 18 states. At a press conference, Kawado called the trip part of Hitachi's commitment to spend $1 billion in the U.S. by 1987; a promise totaling $400 million in U.S. goods for 1986 alone. (Incidentally, the Hitachi itinerary included stops at U.S. semiconductor manufacturers "to explore IC purchases," Kawada said.)

Recall that shortly before this shopping-spree extravaganza, the U.S. Department of Commerce had ruled that certain Japanese companies—NEC, Toshiba, Mitsubishi, Fujitsu, and Hitachi—were guilty of "dumping" electronic products like EPROMs and 256-kbit dynamic RAMs at less than fair-market value. Recall also that last month, the House Ways and Means Committee voted 33–2 to send its telecommunication trade bill (HR 3131) to the House floor. The bill gives the administration six months to determine whether foreign nations are providing reciprocal market access to U.S.-made telecommunication products. If they are not, the bill threatens to shut U.S. markets completely .

Golly, isn't it fun to watch those shopping carts fill up?

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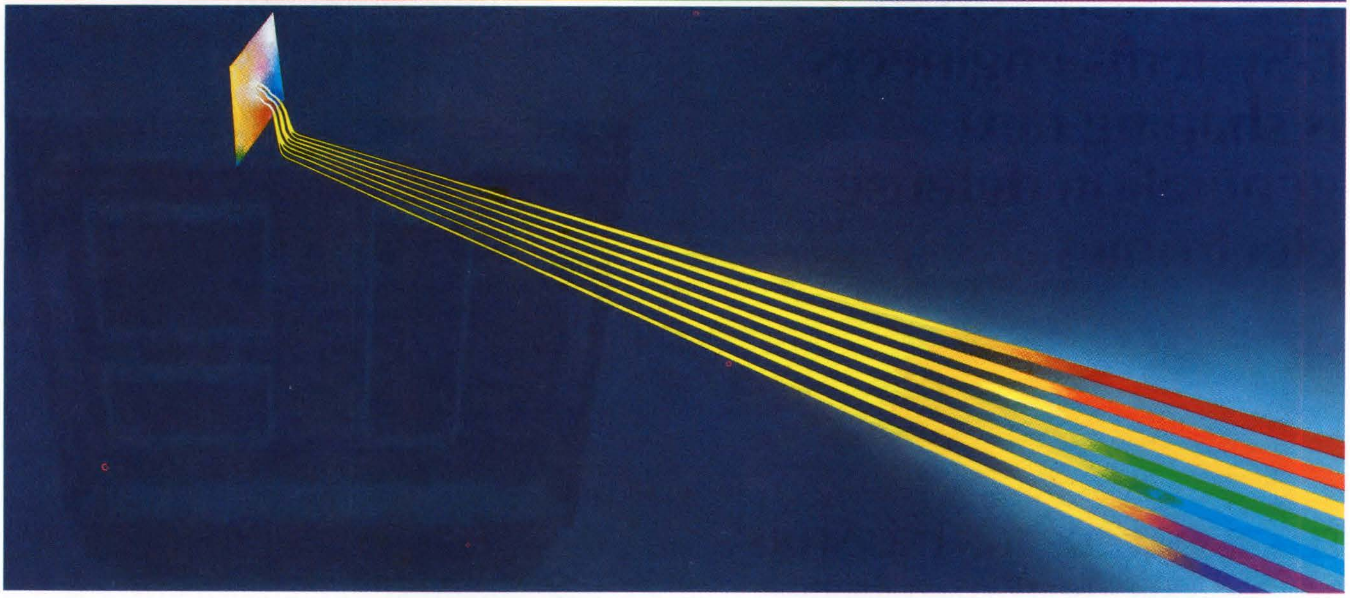

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Digital Signal Processing Engineer—BSEE/MSEE with 4-8 years experience in DSP, time domain equalizers, 256 QAM modulation, multi-level modulation, passive filters and FIR digital filters required.

High Speed Digital Engineers—BSEE with 2-4 years experience in high speed digital design using ECL logic design, multiplex circuits, demultiplex circuits required. Knowledge of impediance matching and load termination desirable. Prior analog circuit experience very helpful. Expertise in LSI, SPICE, CAD, helpful. Position involves design of digital multiplex/demultiplex modules for high capacity lightwave transmission equipment.

DIGITAL CROSS-CONNECT DESIGNERS

Software Project Leaders—BSEE/CS or MSEE/CS with a minimum of 5 years experience in communications protocol interfaces, 68000/68HC11 microprocessor memory, VME Bus and Processor system peripherals. Experience in microprocessor assembly language and "C" level language required.

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Control Subsystem Project Leaders—BSEE or MSEE with minimum of 6 years in communications protocol, interfaces, 68000/68HC11 microprocessors, VME Bus and Processor system peripherals. "C" language desirable.

Switching Matrix Project Leaders—BSEE/MSEE with minimum of 6 years experience in DS1, DS2, DS3 hierarchial rate MUX/DEMUX, input/output conditioners, space matrix modules and interconnect subsystems and knowledge of microprocessors.

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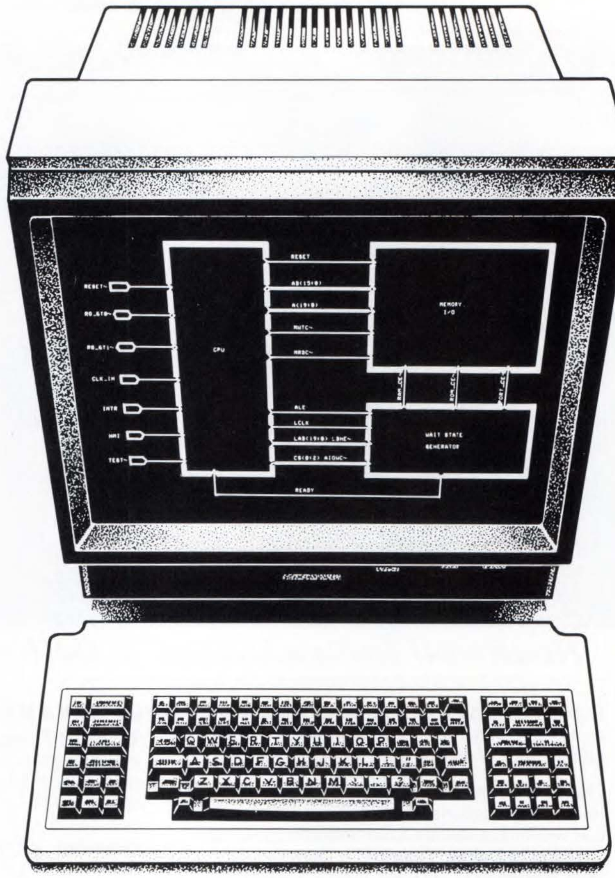

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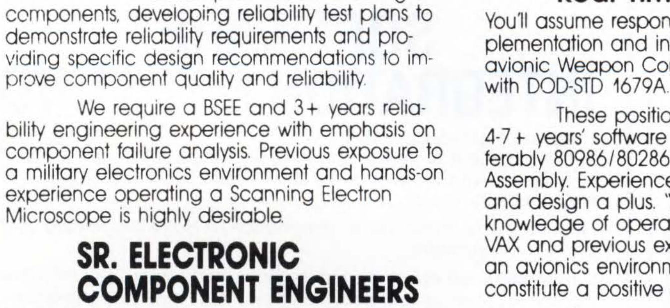

Your qualifications should include a BSEE or the equivalent and 5+ years' experience working with MIL-Standards (i.e., 38510, 19500, 883C). Similar experience in commercial design companies will also be considered.

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You'll assume responsibility for overall systems architecture and details for systems changes, weapon interface and hardware/software integration. This will require reviewing the preparation of systems design and test specifications, preparing systems specifications for Built-In Test, and testing systems and major software functions. You will also be involved in customer interface, technical reviews of software designs, and coordinating and reviewing solutions for systems integration and flight test problems.

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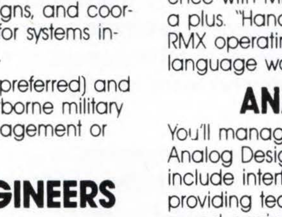
You'll assume responsibility for the design, implementation and integration of software for avionic Weapon Control Systems in conformance with DOD-STD 1679A.

These positions require a BSEE/BSCS with 4-7+ years' software design experience, preferably 80986/80286 systems using "C" and Assembly. Experience with structured analysis and design a plus. "Hands-on" knowledge of operating systems, VAX and previous experience in an avionics environment would constitute a positive asset.



Software Test:

Your primary responsibilities will include the design and implementation of Test software for avionic Weapon Control Systems in conformance with DOD-STD 1679A

These positions require a BSEE/BSCS and 4-7 years' experience in either testing of real-time software, or the development of Test-Set operational and simulation software. Previous experience with MIL-STD's, and knowledge of hardware a plus. "Hands-on" experience with 80986/80286, RMX operating systems, "C", PLM-86 and Assembly language would be highly desirable.

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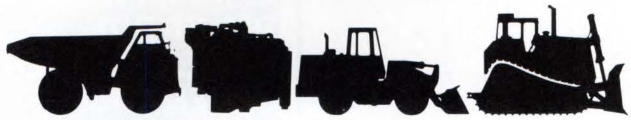

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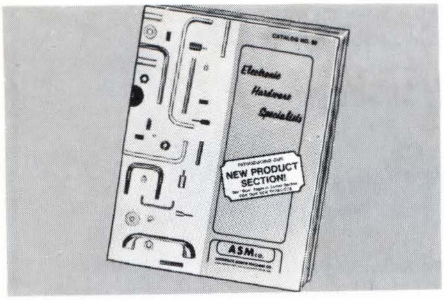

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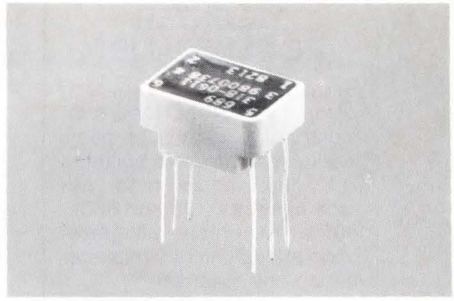

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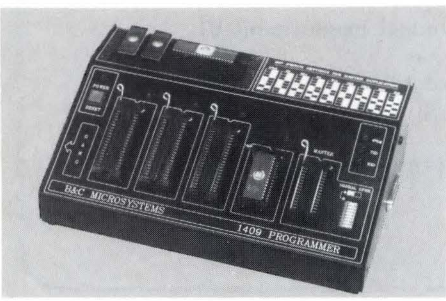

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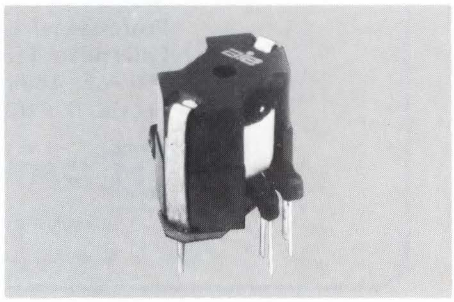

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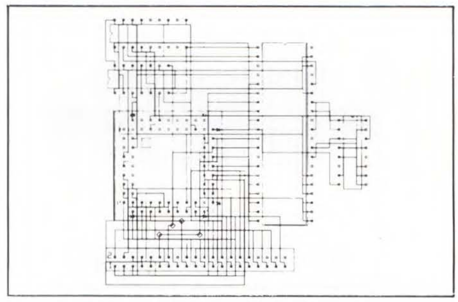

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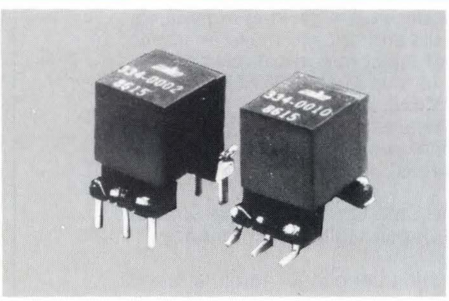

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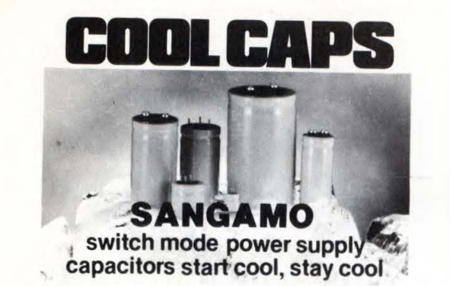

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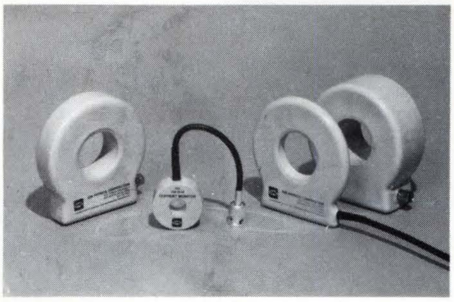

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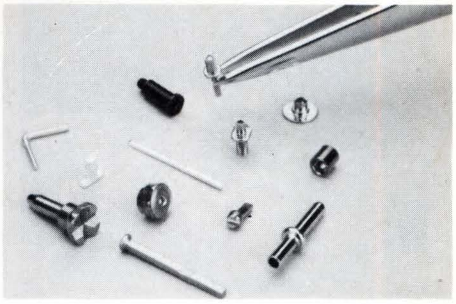

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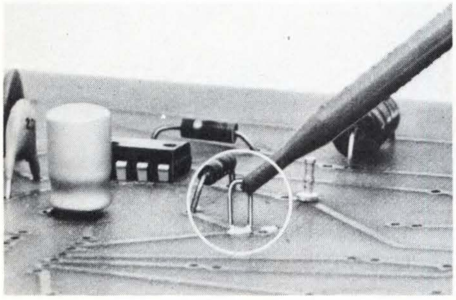

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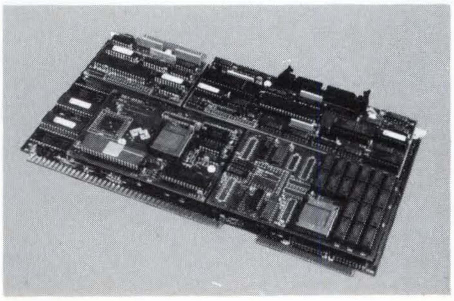

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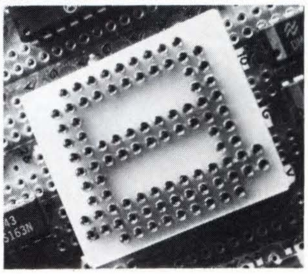

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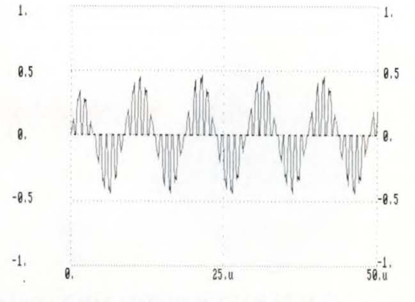
IBM PC/XT/AT ENGINEERING SOFTWARE for the ELECTRONIC PACKAGING INDUSTRY

. . . . THERMAL ANALYSIS SOFTWARE . . . . HEAT85: Program package determines from power and geometry inputs electrical component, assembly and enclosure temperature distributions. Price $875. **COLDPLT:** Design parameters for compact heat exchangers. Price $225. **. . . . VIBRATION/WEIGHT ANALYSIS SOFTWARE . . . . NATFRE:** Vibration analysis of Printer Circuit Boards. Price $295. **WT:** Weight analysis of electronic equipment. Price $185. **EMP Engineering**, P.O. Box 1000, Nesconset, NY, 11767, (516) 361-8921.

SOFTWARE **267**



Electronic Circuit Analysis ECA 2.2 is a high performance analog circuit simulator, with AC, DC, Transient & Fourier analysis. It is a full non-linear simulator, including nonlinear capacitors and inductors. Parts can vary with time or frequency. It includes a worst-case analysis, Monte-Carlo analysis, macro-models, complex y-parameters, transmission lines, & the ability to sweep components. It can analyze circuits bigger than 500 nodes. **ECA-2.2** costs $450. **EC-Ace**, a subset of **ECA 2.2** costs only $95. Call for a free demo disk. **Tatum Labs, 33 Main Street, Newton, CT 06470. 203-426-2184.**

ELECTRONIC CIRCUIT ANALYSIS **268**

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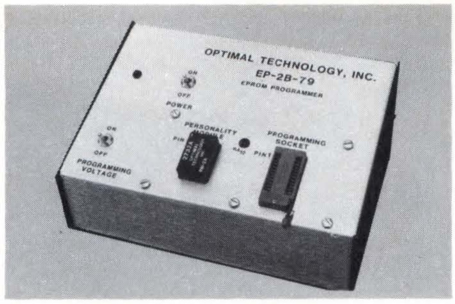
INTEGRATED SOFTWARE PACKAGE **269**



EPROM PROGRAMMER MODEL EP-2B-79 with software MS-DOS, CP/M, Apple, Atari Pet, AIM-65, SYM-1, VIC-20, C-64, H-8, H-89, SS-50 TRS-80 (1&3), and S-100, Programs 2708, 2716, TMS2716, 2732, 2732A, 2532, 2764, 2564, 27128, 27128A, 27256, 27512 and MCM68764 EPROMs; 2816A, 2864A, EEPROM; 8751, 38E70, 8748 MPU Price $179 with personality modules $17 to $35, Software $21 to $40. **Optimal Technology**, Earlysville, Va. 22936 804-973-5482

EPROM PROGRAMMER **270**

The Great SoftWestern Company, Inc.

AUTO-BOARD SYSTEM

The Auto-Board System is an AutoCAD™ companion addressing the tasks of printed circuit board design. The package contains library drawings, basic menus and software. The AutoBoard System features schematic capture, component layout and auto-routing. Contact The Great SoftWestern Company at (800) 231-6880 for more information. **The Great SoftWestern Company, Inc.** 207 W. Hickory St. Ste. 309, Denton, TX. 76201

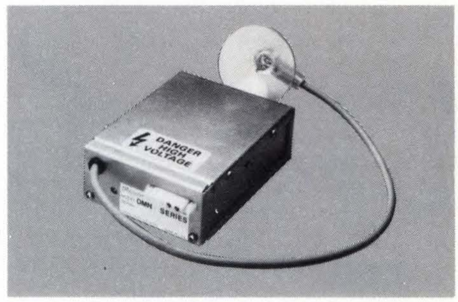
AUTO-BOARD SYSTEM **271**

15 W TRIPLE OUTPUT DC CONVERTER ICI's MT02812T provides regulated isolated outputs of +5 VDC at 2 & ±12 VDC at 208 mA from input of 16-40 VDC. Housed in metal, hermetically-sealed package, this thick-film hybrid unit measures 1.95″ × 1.35″ × 0.50″ with typ. efficiencies of 80%. Operating case temp. range −55- +85°C.ICI offers over 100 models of miniature DC-DC converters. **Integrated Circuits**, 10301 Willows Rd., Redmond, WA 98052. 206/882-3100.

INTEGRATED CIRCUITS 272

Our M-984 detects: • SIT's (Special Information Tones) • OCC (Other Common Carrier) dial tone (400 Hz) • Many international call progress tones. Low-power CMOS in 14-pin plastic DIP package for use with 5-V supply and 3.578 MHz control crystal. Provides 30 dB dynamic range and tri-state outputs. **Teltone Corporation**, 10801 120th Ave N.E., Kirkland, WA 98033. (206) 827-9626

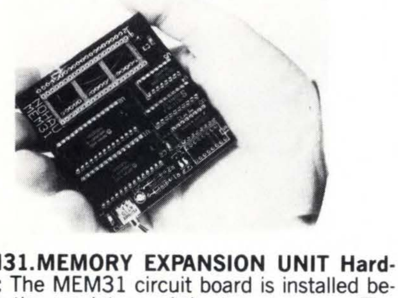
DETECT TELEPHONE INTERCEPT RECORDINGS **273**



NEW HIGH VOLTAGE POWER SUPPLY The **DISCOM DMN** series high voltage CRT power supply design for high resolution monochrome displays. **100KHz CONVERSION FREQUENCY** for lower ripple (0.01%), faster response (0.5mS). HYBRID SURFACE MOUNT REGULATOR for superior performance, smaller size, enhanced reliability. ANODE VOLTAGES TO 20KV. **HIGH EFFICIENCY**, through use of MOSFET oscillator and premium ferrite core and resin. **DISCOM INC.,** 334 Littleton Rd., Westford, MA 01886. (617) 692-6000.

HIGH VOLTAGE POWER SUPPLY **274**

MEMORY EXPANSION FOR INTEL EMV51 and ICE51



MEM31.MEMORY EXPANSION UNIT Hardware: The MEM31 circuit board is installed between the emulator and the target system. The MEM31 board contains 16K of R/W memory. The memory can be expanded up to 64K. No external power supply is needed. **Software:** The MEM31 software automatically splits your object file into emulatory loadable units. They are then loaded into the MEM31 via the emulator. The price is $495 which includes PCB, floppy disk and documentation. **NOHUA CORPORATION,** 164 Calle Larga, Los Gatos, CA 95030 (408) 374-1594

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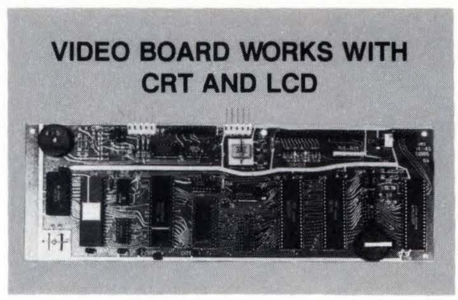
ARE YOUR PRODUCTS RELIABLE? The RelCalc 2 Software Package predicts the reliability of your system using the part stress procedure of MIL-HDBK-217D, and runs on the IBM PC and full compatibles. Say goodbye to tedious, time consuming, and error prone manual methods! RelCalc 2 is very easy to use, and features menu windows, library functions, global editing for what-if? trials, and clear report formats. $1500. Demo package for $50. **T-Cubed Systems**, 31220 La Baya Drive #110, Westlake Village, CA 91362. (818) 991-0057.

AUTOMATE MIL-HDBK-217D **276**

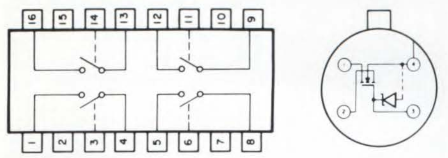


The ITB-85 is a stand-alone video terminal board. Characters may be displayed on a CRT and/or 2x40 LCD. Operating parameters are accessible thru the keyboard with an on-screen setup menu; selected settings may be stored in nonvolatile memory. The ITB-85 emulates Zenith Z19/Z29, ADM 3A, Hazeltine 1500 and ANSI terminals. RS-232C port has selectable baud rate to 38.4 kbaud. ITB-85 is designed to mount under a keyboard. IMS offers a keyboard for use with the ITB-85. **INTELLIGENT MICROSYSTEMS 254 Madison Road Parsippany, NJ 07054 (201) 428-0051**

VIDEO TERMINAL BOARD **277**

Analog DMOS FETs

SD5000 and SD200 Series Arrays

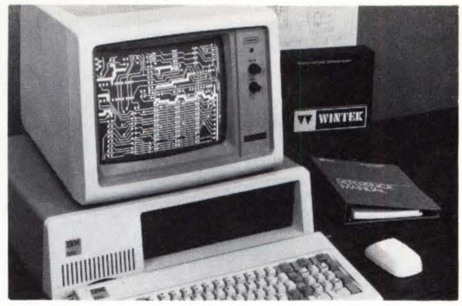


Analog switching elements manufactured with DMOS process exhibit high breakdown voltage, very short propagation delays (600 psec with 680 Ω), low capacitance and low on resistance (19 Ω). Industrial and commercial grade devices are available. All devices are also available in a die form ex-stock. The prices start at $0.69 for 10,000 up units. **Calogic Corp.** 237 Whitney Place Freemont, CA. 94539, 415-656-2900

ANALOG SWITCHING ELEMENTS **278**

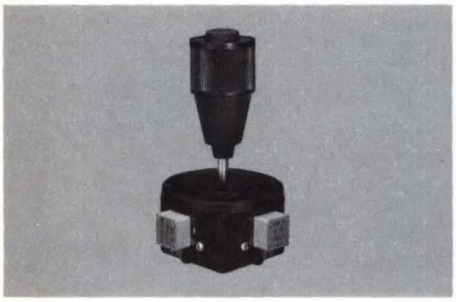
6800-Family Software. Software for 6800/01/05/09 microprocessors. SOFTWARE: C compiler Pascal, multitasking DOS, macro-assemblers, FORTRAN, 16K BASIC, FIRMWARE: Fantom monitor/debugger, math library, 4K BASIC. CROSS SOFTWARE: Assemblers, PL/W Compilers, Linker, Simulators. **Wintek Corporation** 1801 South Street, Lafayette, IN 47904-2993. (317) 742-8428, (800) 742-6809

SOFTWARE **279**



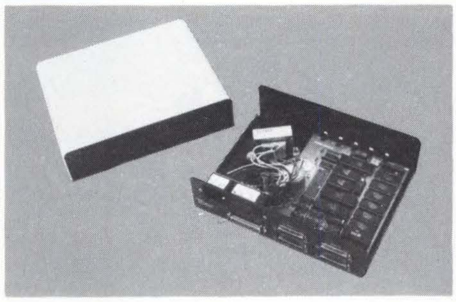
smARTWORK® Circuit-Board-Artwork Software. For only $895, **smARTWORK®** lets the design engineer create and revise printed-circuit-board artwork on the IBM Personal Computer. Forget the tedium of taping it yourself or waiting for a technician, draftsman, or the CAD department to get to your products. With **smARTWORK®** to keep complete control over your circuit-board artwork from start to finish. Call or write to **Wintek Corporation,** 1801 South Street, Lafayette, IN 47904-2993. (317) 742-8428, (800) 742-6809

PCB ARTWORK SOFTWARE **280**



NEW MINIATURE JOYSTICK The New Miniature Series Analog Joystick has been designed for applications which have a limited amount of space available. It is a panel mount unit which requires 2 × 2 × 1 inches of space below the mounting surface. It provides linear infinite resolution voltage signal output and is available as a two-axis, two-axis with push button or as a three-axis joystick. $20 ea./1000. **CH Products,** 1558 Osage Street, San Marcos, CA 92069 (619) 744-8546

CH PRODUCTS **281**



NEW Z80 PROCESS CONTROL OR STORE-AND-FORWARD COMPUTER The DSB-3200 features four RS-232 serial ports, a Centronics printer port and eight Bytewide memory sockets that accept any combination of static RAM, EPROM, or EEPROM. Battery backed up RAM and a non-interrupting clock calendar are options. Integral power supply operates on 100, 120, 200 or 240VAC. Five LEDs on front panel show POWER ON and activity on the serial lines. **DAVIDGE CORPORATION** P. O. Box 1869E, Buellton, CA 93427 (805) 688-9598

DAVIDGE CORPORATION **282**

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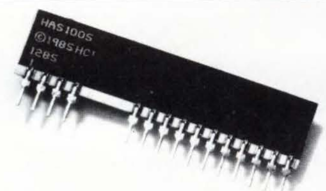
SCHEMATIC DESIGN TOOL **283**

ANALOG PLL DATA SEPARATOR



- **Small Size** . . . .
- **SIP Configuration** . . . .
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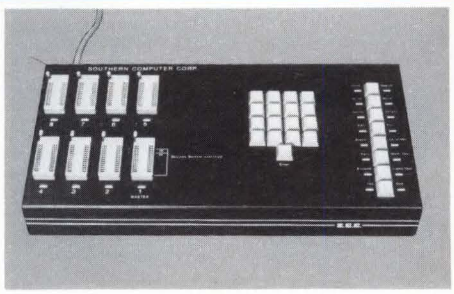
- **No Additional Analog Circuitry Required** . .

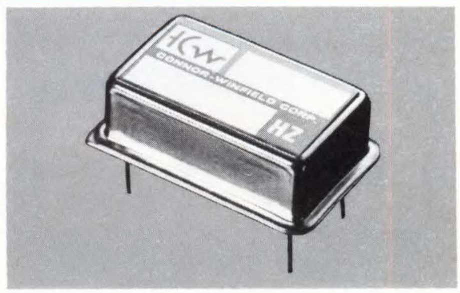
The HAS1005 is a complete analog subsystem: an analog phase lock loop specifically designed for 5 Mb/s Winchester data separation. It has TTL-level digital inputs and outputs. And it's laser trimmed so you get repeatable accuracy. Yet it is less than 1.8 inches long by .45 inches high. **Hybrid Circuits Inc.** 760 San Aleso Avenue Sunnyvale, California 94086 (408) 745-0950

HYBRID CIRCUITS **284**



The SCC Cost Efficient Programmer for EPROMS/EEPROMS. Basic System **$1,195** includes: Keypad, serial port, display, 8 gang programming, set programming, and device menu—**no personality modules**. 256K byte memory option—program 512 devices. UV Eraser $395. **Southern Computer Corporation** 3684 Clearview Avenue Atlanta, Georgia 30340 **404/455-8018**

PROGRAMMER **285**



HIGH SPEED OSCILLATORS! Connor-Winfield has a new line of HCMOS oscillators available up to 25 MHz. ECL logic oscillators are available up to 200 MHz. Both types are enclosed in hermetically sealed 14 pin DIPs. Also, LOW COST TTL DIP clocks are available for IMMEDIATE delivery at the following MHz frequencies: 1, 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, 40 and 70 MHz. (+/− .01% or .005%, 0 − 70 C). Call or write for our new catalog. **Connor-Winfield Corp.,** 114 W. Washington St., P.O. Box L, West Chicago, IL 60185. (312) 231-5270.

OSCILLATORS **286**

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Power Tester By using state of the art technology, this power supply tester earns the highest return on investment. The Cherub comes with four 20 ampere loads and two 350 VA AC/DC sources. The Cherub's 20 test, easy to program software makes it unique. Auto-calibration, self-diagnosis and integrated fixturing provide trouble-free operation. **Angel Labs**, 12 Avis Dr., Latham, NY 12110 (518) 783-1377 Ex-475

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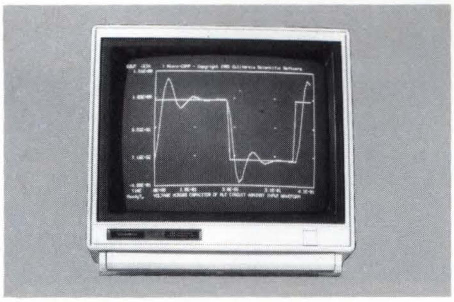

Engineering Software: Micro-CSMP simulates any system including • Control and Servo systems • Robotics • High Order Filters • Chemical Processes • Stress & Strain. A full implementation of IBM's S/360 CSMP, Micro-CSMP produces graphical results in minutes, typically requiring 10-20 lines of input. **LSAP analyzes linear systems** producing Bode, Nyquist, and Transient Response plots, and Root-Locus diagrams. Micro-CSMP is $900, LSAP is $450 for PC-DOS or MS-DOS systems. **California Scientific Software** 25642 Hazelnut, El Toro, CA 92630 (714) 581-7654

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high voltage diodes, cartridges and assemblies

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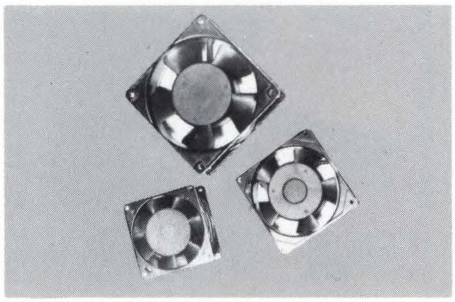
ELECTRONIC DEVICES **290**



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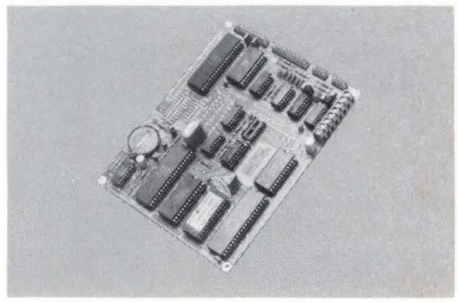
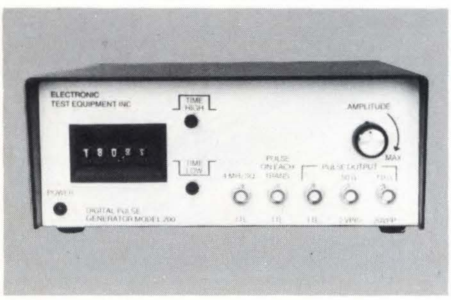
BRUSHLESS FANS AC/DC **291**



65/9028 VIDEO TERMINAL BOARD emulates ANSI, H19, and ADM-3A • Uses IBM PC, parallel ASCII or serial ASCII keyboards • Supports soft keys and answer-back message • Provides smooth or jump scroll • RS-232C data and printer ports • Baud rates to 19.2k • 80x25 hash free display with non-scrolling status row • Composite or separate video with 50/60Hz vertical sync. • Nonvolatile on-screen set-up • 5x6.5 inch card • This is a video solution for only $99.95/kit. $139.95/A&T. **Digital Research Computers,** P.O. Box 381450 Duncanville, TX 75138 (214) 225-2309.

VIDEO TERMINAL BOARD **292**



CRYSTAL CONTROLLED PROGRAMMABLE PULSE GENERATOR Thumbwheel switch controlled **ACCURATELY CALIBRATED** high and low periods easily dialed in on front panel OR down loaded from any computer's RS-232 port. 128 ETE instruments controllable from 1 port. pulse timing 250ns to 999.75 minutes, duty cycles up to **239 BILLION** to **1. PULSE GENERATOR $335, RS-232 INTERFACE $185** CALL **1 (800) EASY-TST ELECTRONIC TEST EQUIPMENT INC** 44-28 Old State Rd. New Milford Ct. 06776 in Ct. (203) 354-4828

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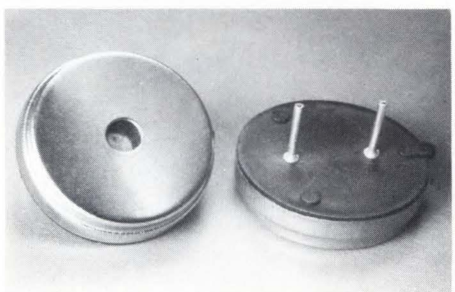
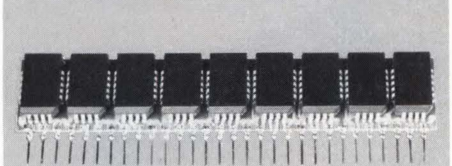


LOW COST PIEZO SOUND TRANSDUCERS MS-3 sound transducers are pre-assembled & pre-tested—for PC board insertion. Stainless steel & glass-filled polyester constr. Exclusive soldered crystal contacts for max reliability. Generates 70 to 80 dBA (2-5 kHz) at 2 ft. Freq., volume & mode are functions of drive circuitry you supply. .930″ dia. × .255″. Made in USA. 42¢ ea/1000 qty. **Floyd Bell Inc.,** 987 Higgs Ave., P.O. Box 12327, Columbus, OH 43212. 614/488-3193.

FLOYD BELL **294**

Innovative Modules



Single-in-line, Dual-in-line, and custom modules are readily available from INMOD Innovative Modules. INMOD dynamic RAM Single-in-line Memory Modules (SIMMs) offer more than twice the density possible with surface mounted PLCCs. Each memory device is individually decoupled with on-board capacitor. For custom, surface mount or hybrid modules, INMOD provides electrical and physical design service, as well as prototype and volume manufacturing. INMOD, 14375 Saratoga Ave. Saratoga, CA 95070, 408-741-1420

INNOVATIVE MODULES **295**

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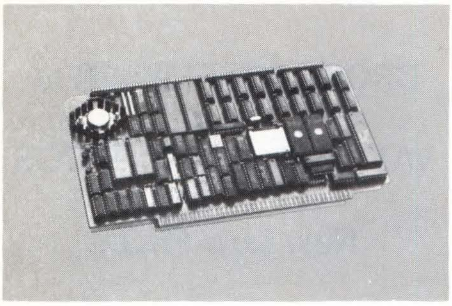

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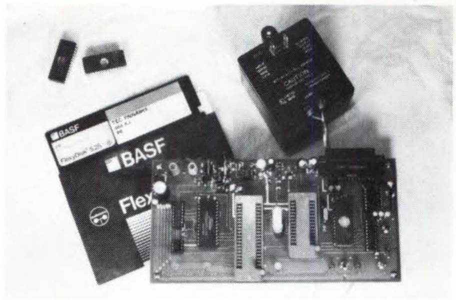

MICROCOMPUTER DEVELOPMENT SYSTEM ... TEC announces a price/perf breakthrough. Use the IBM PC/XT/AT or true compatibles to develop products based on Motorola MC68705 P3, P5, R3, R5, U3, U5 single chip micros. Complete integrated system includes a cross assembler, a simulator/debugger and a programming board with driver software for Intel Hex or Motorola S record files. One serial port required. Complete sys.—$495, Prog. Board with driver s/w—$349 **TEC** PO Box 53 West Glover, Vt. 05875 Phone (802) 525-3458

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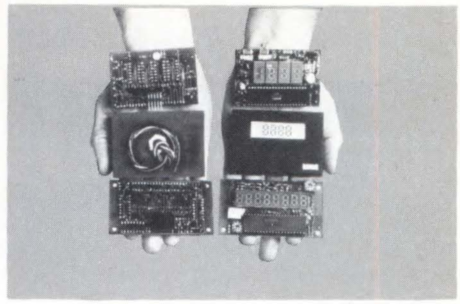

D.P.M.s ARE ONLY ½″ DEEP Models for VDC, RPM, RTD & THERMOCOUPLE TEMPERATURE, up/down COUNTERS, RPM, RATE PERIOD, TIME, EVENT, INTEGRATION (Analog Totalizers) and more, 14 models all available in 3 packages, FLATPACK (encased) NAKED p.c. mount and NAKED panel mount. L.E.D. or L.C.D. displays from 3½ to 8 digits. Our prices and quality are unbeatable, specials are our standards. Prices in the teens for large OEMs orders. **I.M.C.** 4016 E. Tennessee Street Tucson, AZ 85714 (602) 748-7900

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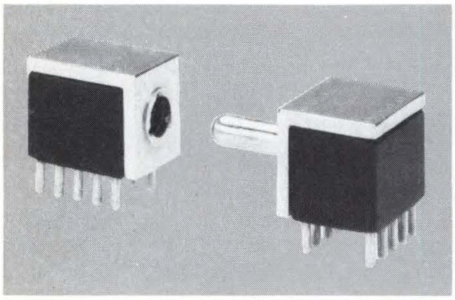
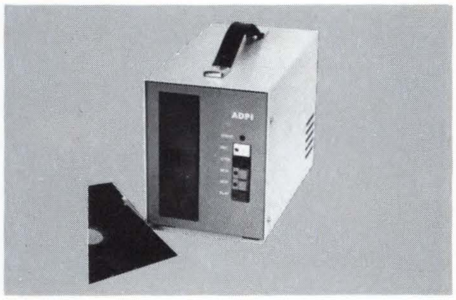


ICCON™ MOTHER BOARD/DAUGHTER BOARD INTERCONNECTS. New power distribution system allows reliable & consistent performance while providing quick board connect & disconnect. Less than 6 mV drop at 75 amp rating • 90° or 180° mounting configurations • 10-pin DIP mounting in single or bussed configurations • Low profile, minimum board space • Complaint-pin or wave-solder styles. Call (415) 490-4200 or write: **Elcon Products International Co.** P.O. Box 1885, Fremont, CA 94538 TWX 910-381-7026.

MOTHER/DAUGHTER BOARD INTERCONNECTS **299**



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68020

—QT 20x—

• Supports from 4 to 28 users
• 2 to 14 Megabytes of RAM

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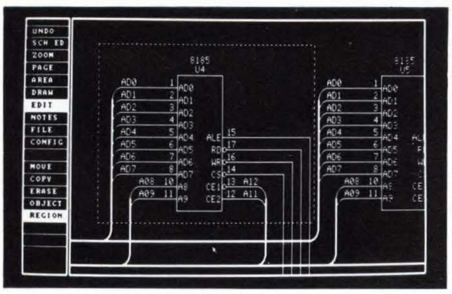

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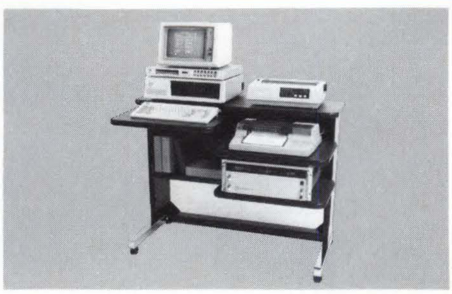

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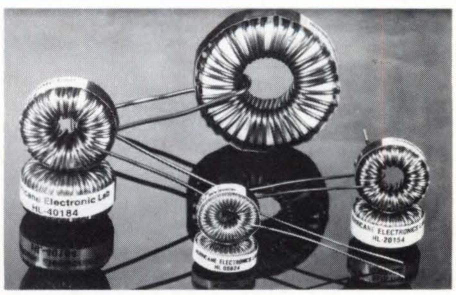

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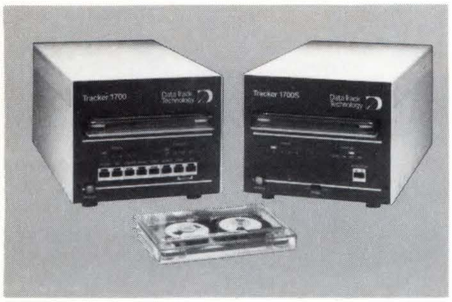

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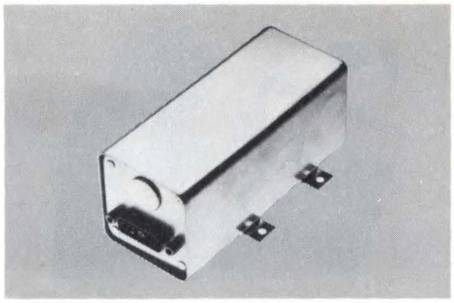

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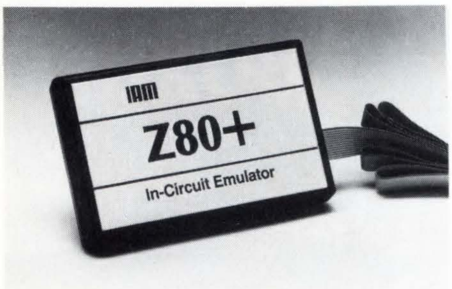

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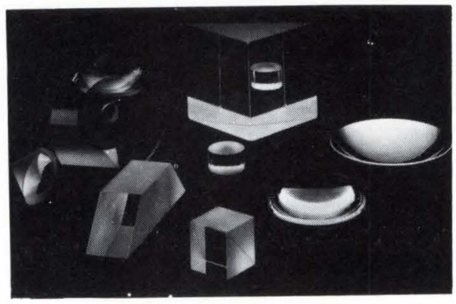

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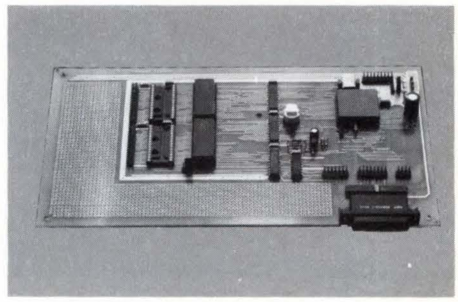

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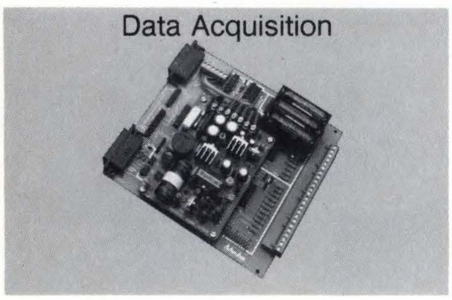

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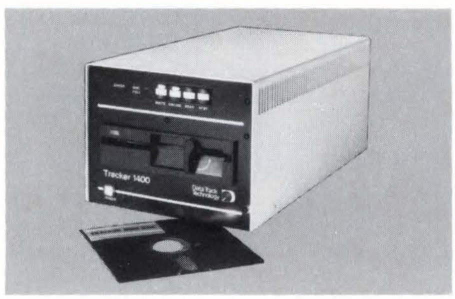

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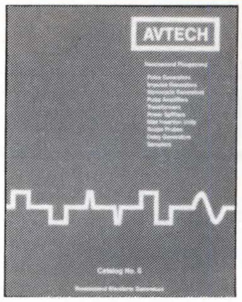

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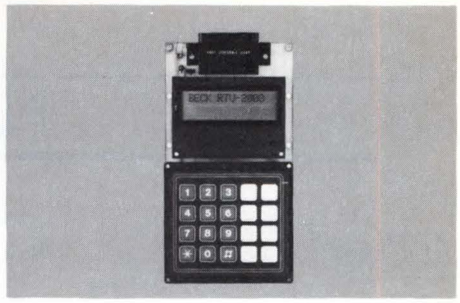

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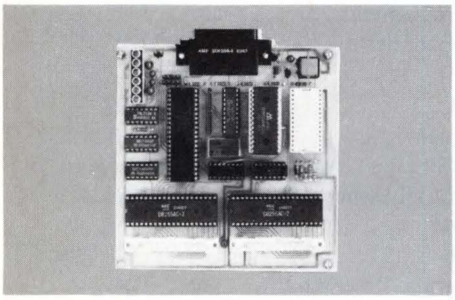

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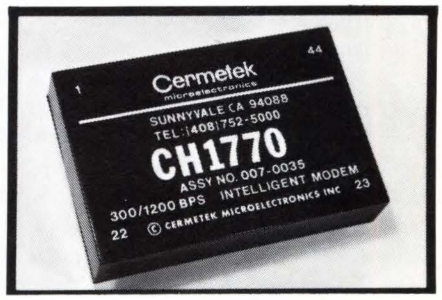

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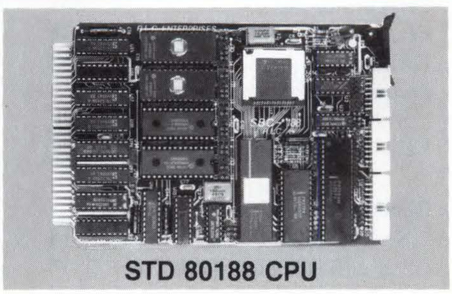

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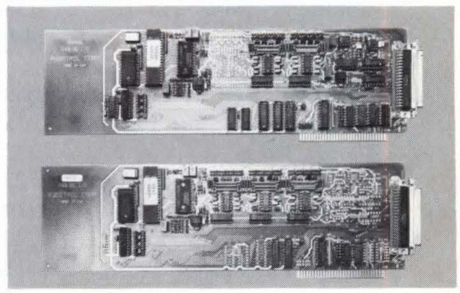

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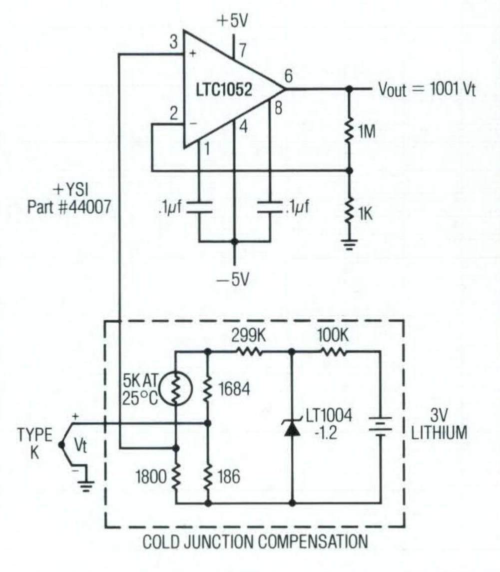

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