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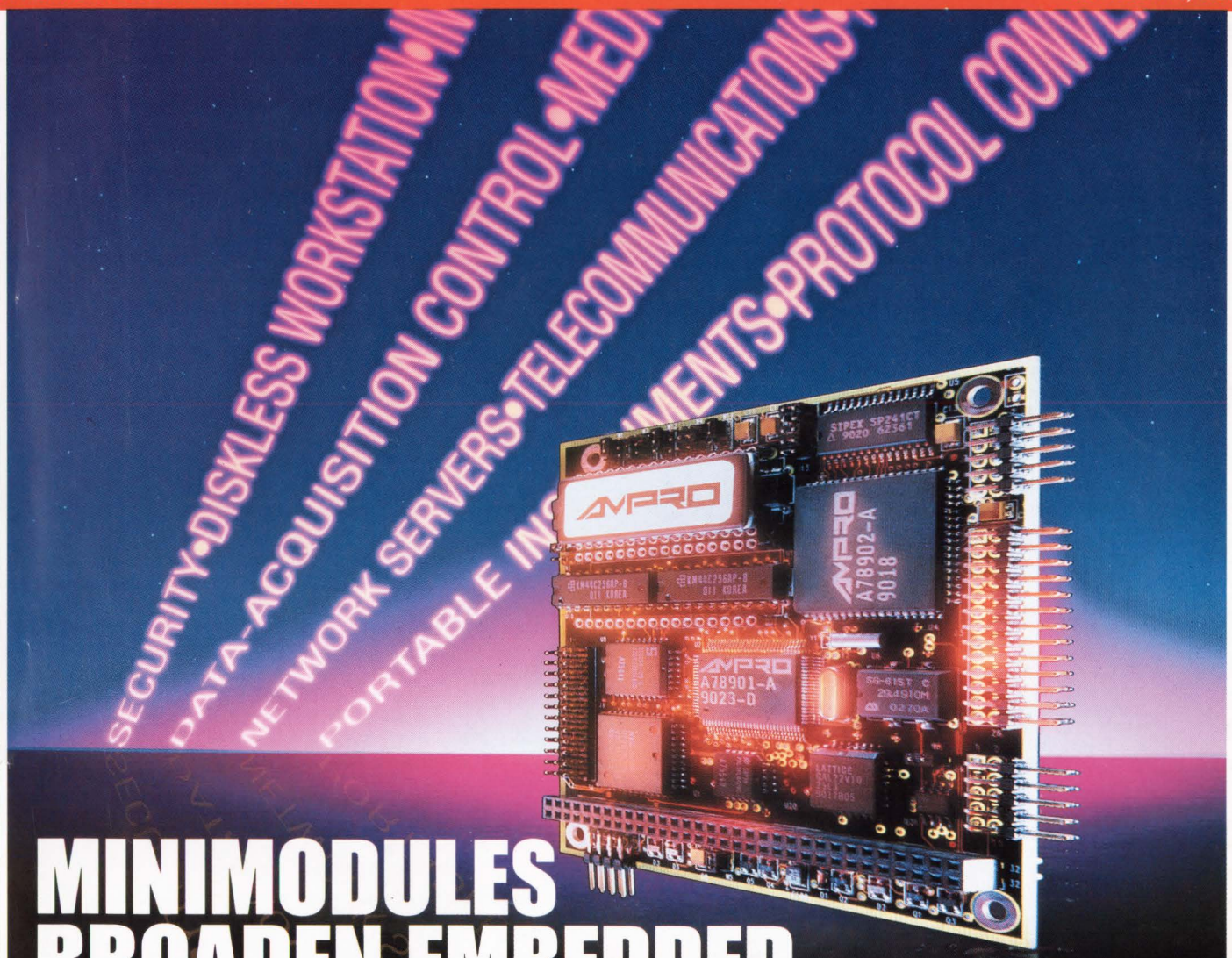
ELECTRONIC DESIGN

A PENTON PUBLICATION U.S. $5.00

OCTOBER 11, 1990

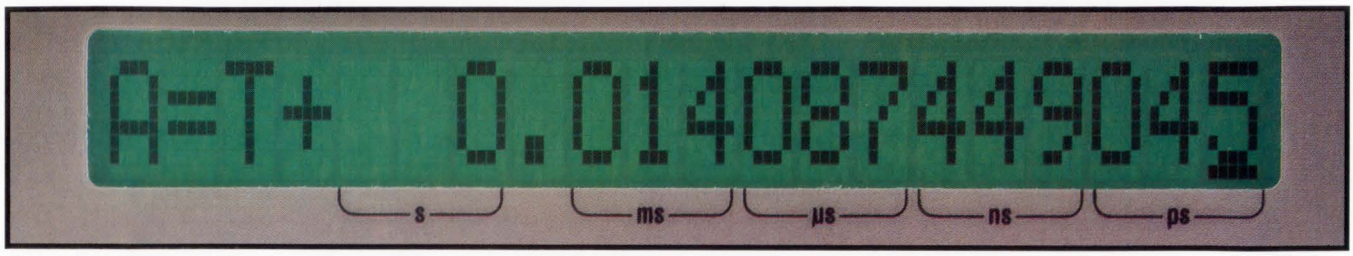


MINIMODULES BROADEN EMBEDDED USES OF PCs

• PRODUCT REPORT: PLD TOOLS KEEP PACE WITH DEVICES

QUICKLOOK
PAGE 97

Go ahead ... add 5 psec



Picoseconds are no problem for the DG535 Precision Pulse & Delay Generator.

The DG535 provides 4 edge (delay) and 2 pulse (delay and width) outputs, all with 5 ps resolution, 1000 sec range, 50 ps rms jitter, and adjustable output levels. The outputs drive 50 Ohms or high impedances to 4 Volts with a slew rate of 1 V/ns - just right for driving TTL or ECL or even high speed analog circuits. Throw in the 35 Volt output option and you can trigger almost anything. For even greater accuracy and stability, add the 1 ppm optional timebase .

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On the bench or in a test environment, the DG535 has the accuracy, stability, precision, and reliability you need to solve your tough timing problems - all at a price you can afford. Call SRS for more information on the DG535, even if you don't need picosecond resolution.

DG535	$3500

- 4 delay, 2 pulse channels
- 5 ps delay resolution
- 50 ps rms jitter from trigger
- Adjustable output levels to 4 Volts
- 0 to 1000 sec delay range
- Internal/external trigger to 1 MHz
- Internal/external timebase
- 9 location set-up memory
- GPIB interface standard
- ±35 Volt output option
- 1 ppm timebase option
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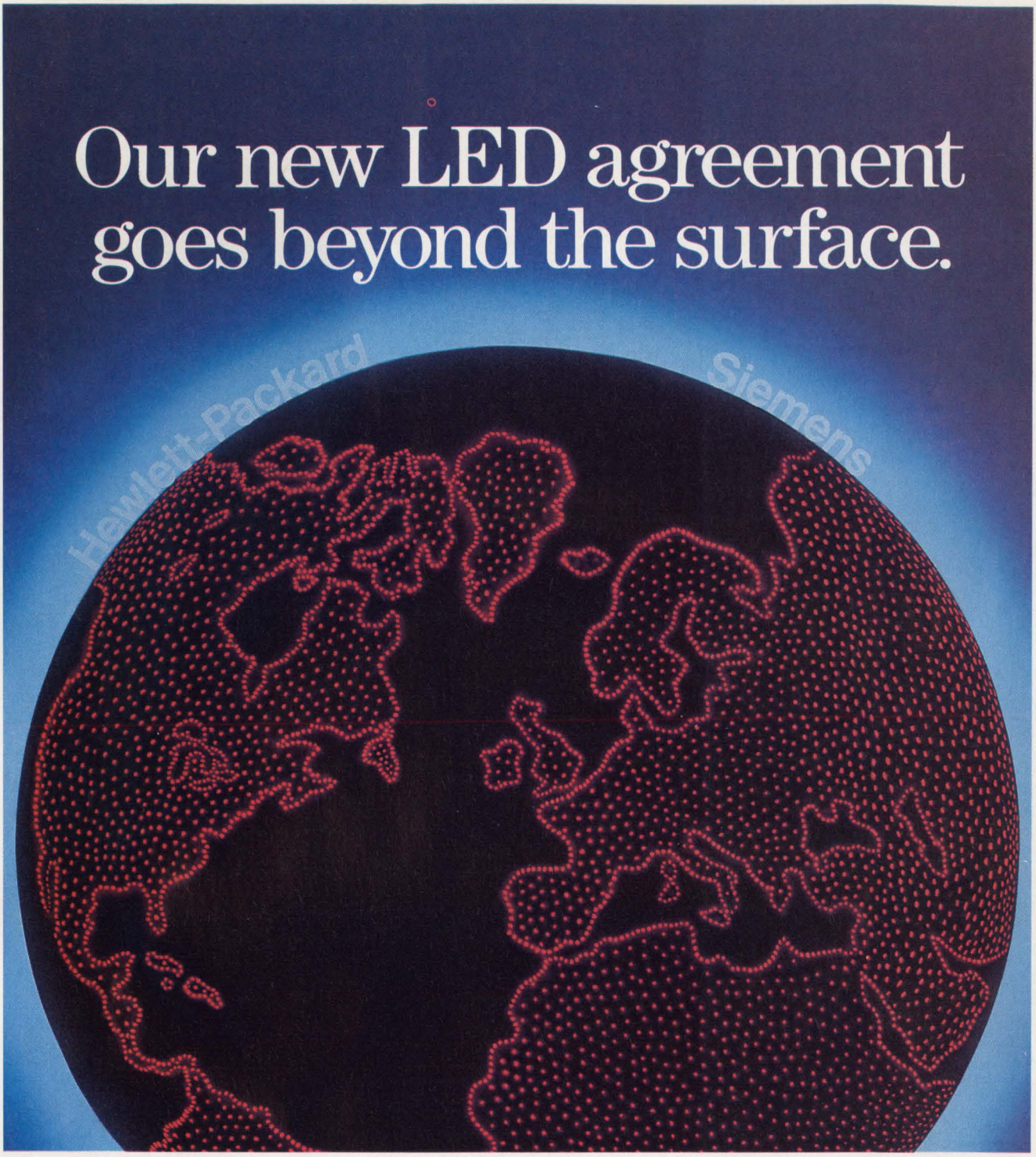

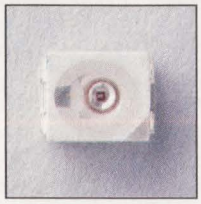

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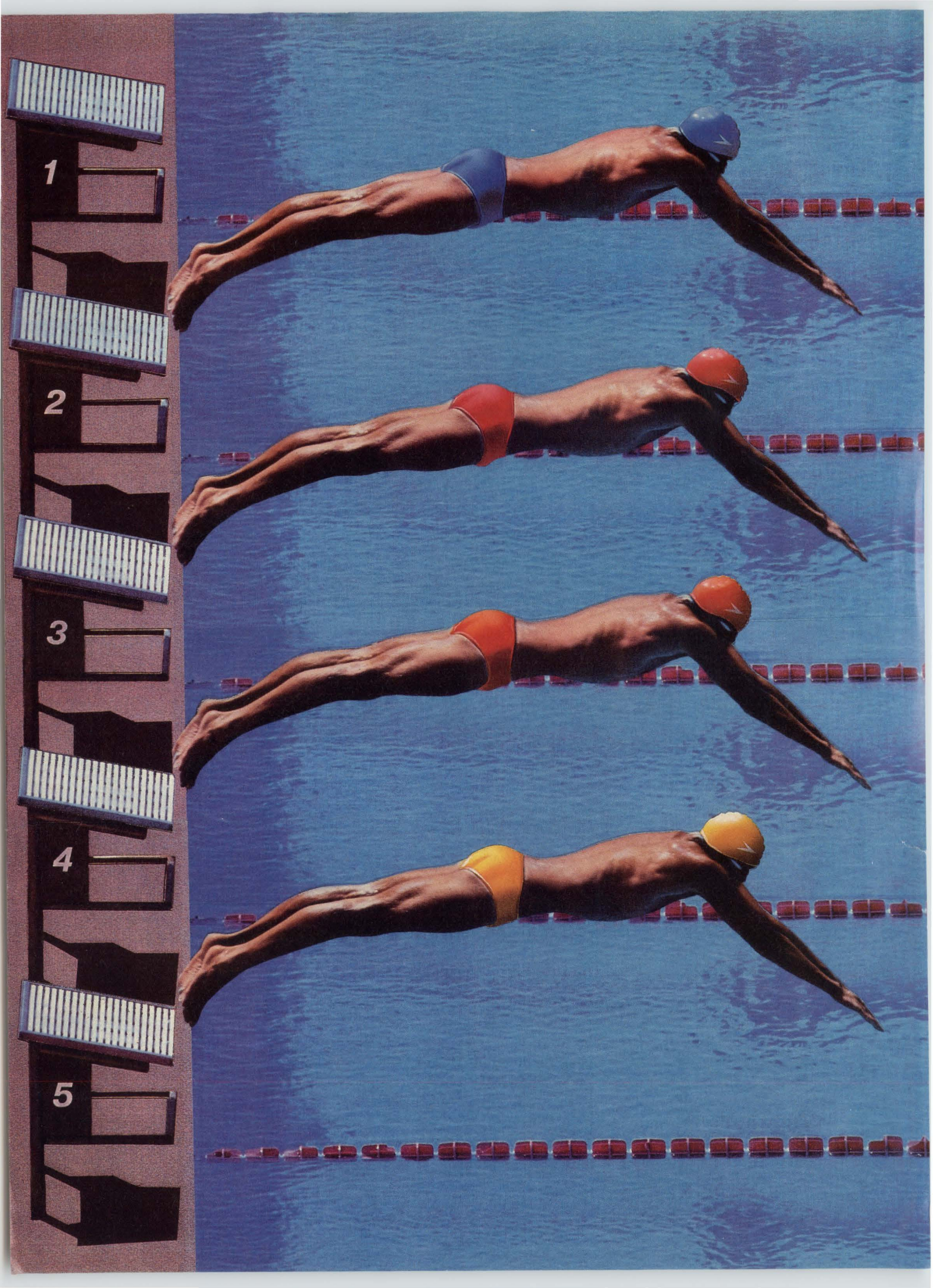
1
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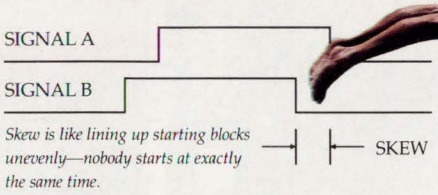
A Precision Start, Every Time.

Motorola's Low-Skew Clock Drivers for Precision Control and Timing of High Speed RISC and CISC Designs

Record setting performance for high speed processor designs depends on perfect timing, perfect control from start to finish.

If your high speed CISC or RISC processor flies off the blocks at 25MHz, 33 MHz or faster, clock signal skew from ordinary clock drivers can result in false starts for devices in close proximity. And, you may also require very exact 50% duty cycle waveforms.



Skew is like lining up starting blocks unevenly—nobody starts at exactly the same time.

Either way, without precise operation, performance suffers. Worst case? You blow your race to production and the entire design could be disqualified.

A Precision Start

To get all of your board's devices off to a precision start for critical events, Motorola's low-skew clock drivers are setting the target pace.

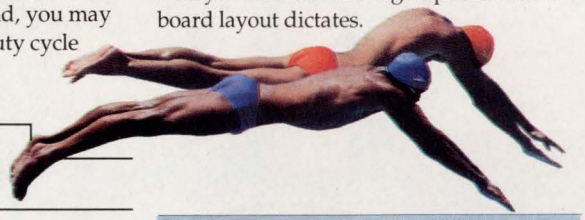
Offering 200% to 300% less output skew than ordinary clock drivers, typical delay skews are as low as 0.1 nS in ECL and 0.5 nS for TTL or 0.5 nS for CMOS outputs.

When you design with low-skew clock drivers, you don't need to handicap your high speed circuits with delay chips that compromise power and speed. And you can avoid trial and error tests with other high speed logic devices you had hoped would sooner or later work.

Instead, Motorola's line of low skew clock drivers let you design for optimum speed control from the beginning, with high performance dependability part-to-part and tight clock duty cycles.

Programmable Time Delays

For really difficult timing requirements, your design can also incorporate Motorola's Programmable Time Delays. Along with Low Skews, MC10E/100E195 (20 pS steps) or 196 (80 pS steps) ECL input delays provide you with more design options when board layout dictates.



Part #	Input Levels	Output Skew (nS)	Output/Input Freq. Ratio	Max. Input Freq. (MHz)	Output Levels
F803	TTL	1	+2	70	TTL
H640	TTL or ECL	0.5	+2 and +4	135	TTL
H641	ECL	0.5	1X	100	TTL
H642	TTL or ECL	0.5	+2 and +4	135	TTL
H643	ECL	0.5	1X	100	TTL
E111	ECL	0.1	1X	1000	ECL
MC88913	TTL	1	+2	110	CMOS
MC88914	TTL	1	+2	110	CMOS
MC88915	TTL	0.5	1X, 2X, and 4X	70MHz*	CMOS

*MC88915 is a PLL Clock Driver, therefore 70MHz is the maximum output frequency.

CMOS Skews of 0.5-1 nS and Phase-Locked Loop Capability

For multiple synchronous outputs, the MC88913 Clock Driver (skew 1.0 nS) and MC88914 CMOS Clock Driver with Reset (1.0 nS skew) provide high speed, low power hex divide by two capability. The MC88915 Low-Skew Phase-Locked Loop Clock Driver locks output frequency and phase into the input reference clock — and can synchronize several boards. It also functions as a frequency multiplier that can double or quadruple the input frequency. Skew is 0.5 nS.

FAST Schottky TTL Low-Skew Clock Drivers

For quad D-type flip-flop applications requiring matched propagation delays, the MC74F803 Clock Driver provides 1.0 nS skew.

68030/040 0.5 nS Skew ECL/TTL Clock Driver

Motorola's MC10H640 series Clock Drivers generate clock output for 68030/040 and are warranted to meet all clock specs required by these microprocessors.

ECL Clock Driver with 9 Differential Outputs

The MC10E111 is a low-skew differential driver designed with clock distribution in mind — nine outputs and .1 nS skew.

Full Microprocessor Support

Motorola's clock drivers support the full 68000 CISC and 88000 RISC MPU lines. They also can drive Intel CISC and RISC MPUs, AMD, SPARC, MIPS, and Clipper MPUs.

Start your drive for the finish

If you want the best in clock drivers for fast processor designs, begin your drive for the finish with a perfect start. Specify Motorola Clock Drivers to win at any pace.

To get off the blocks fast, call toll free for more information: **1-800-521-6274**. Or, fill out and return the coupon below.

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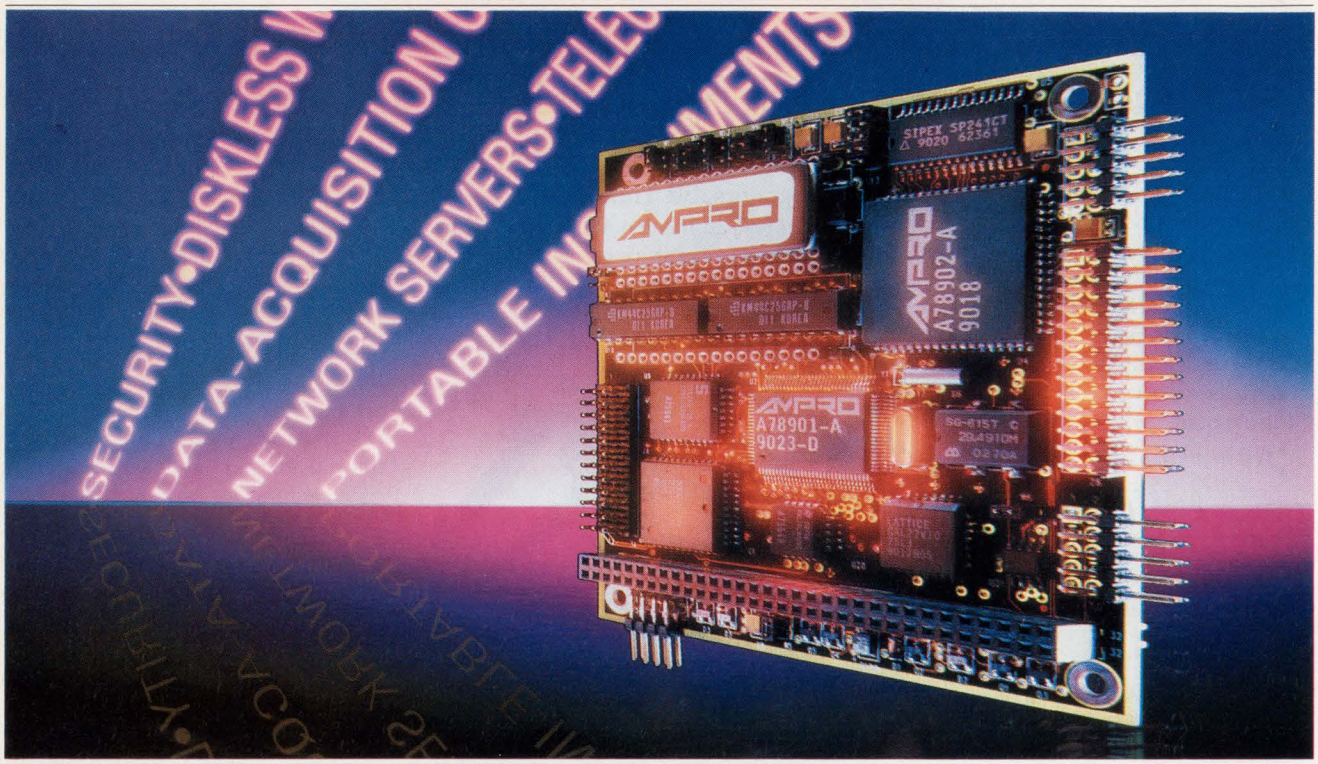

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- A preview of Electronica 90 in Germany
- Op-amp macromodels that mimic real parts
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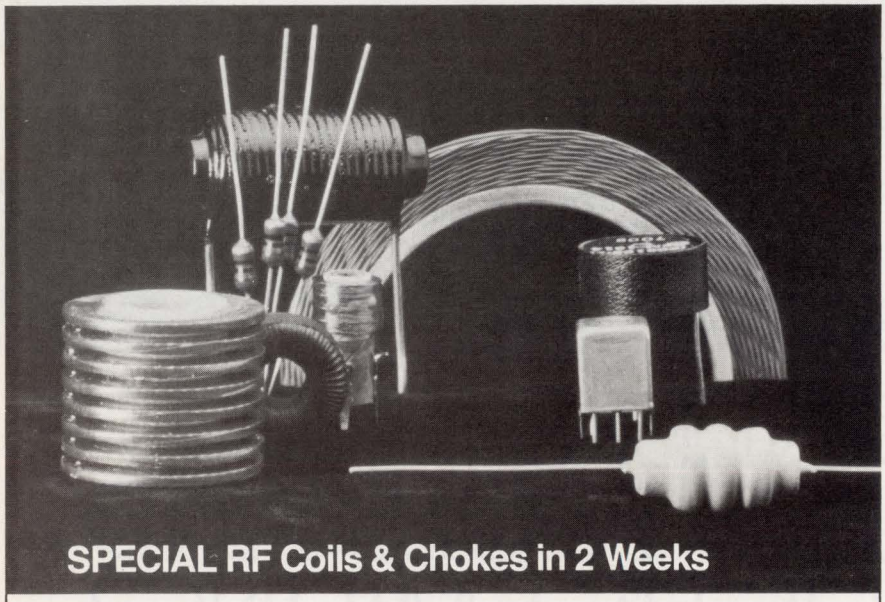

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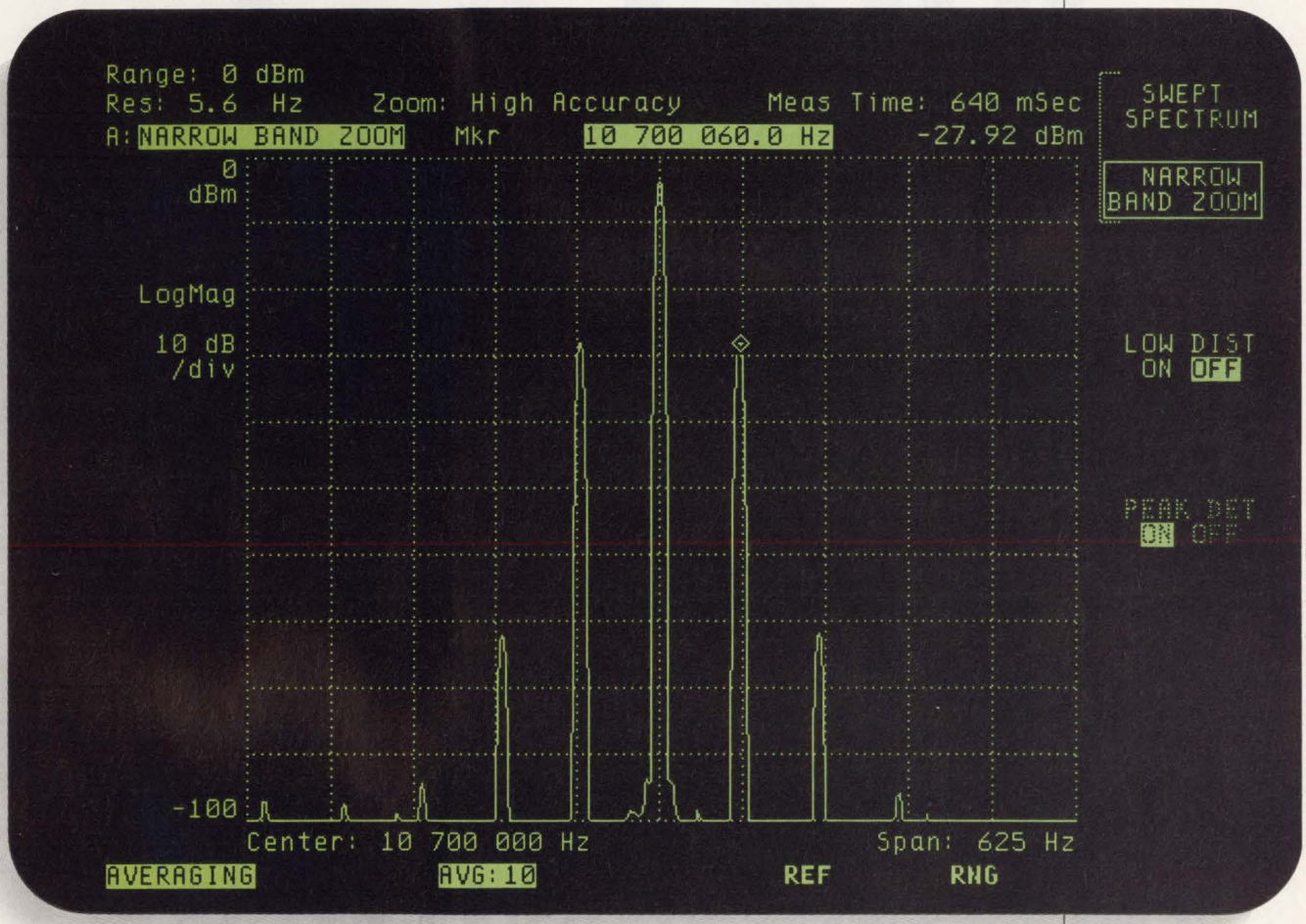

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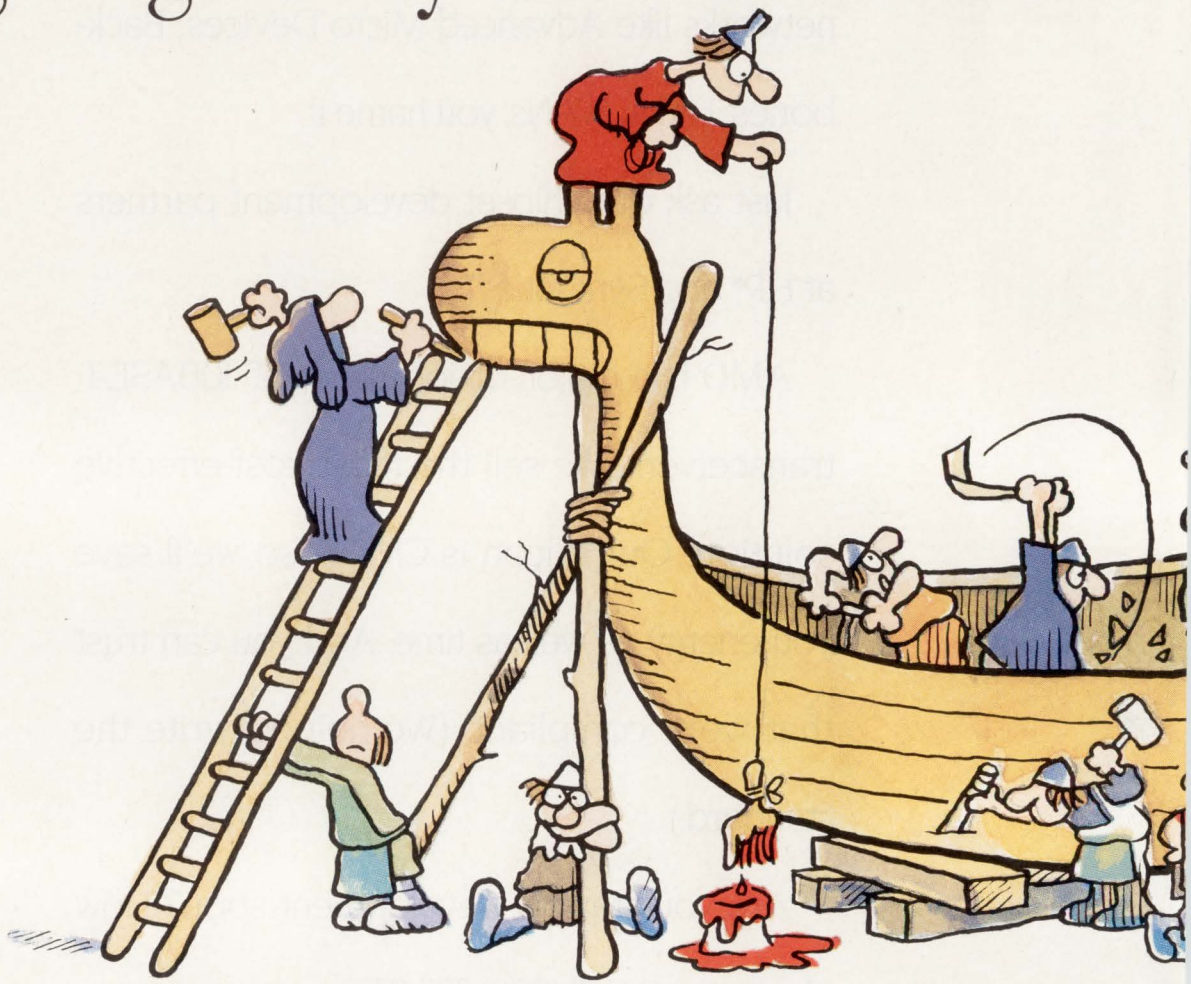

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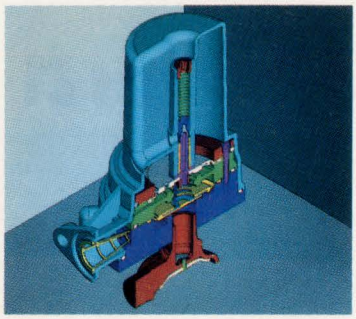

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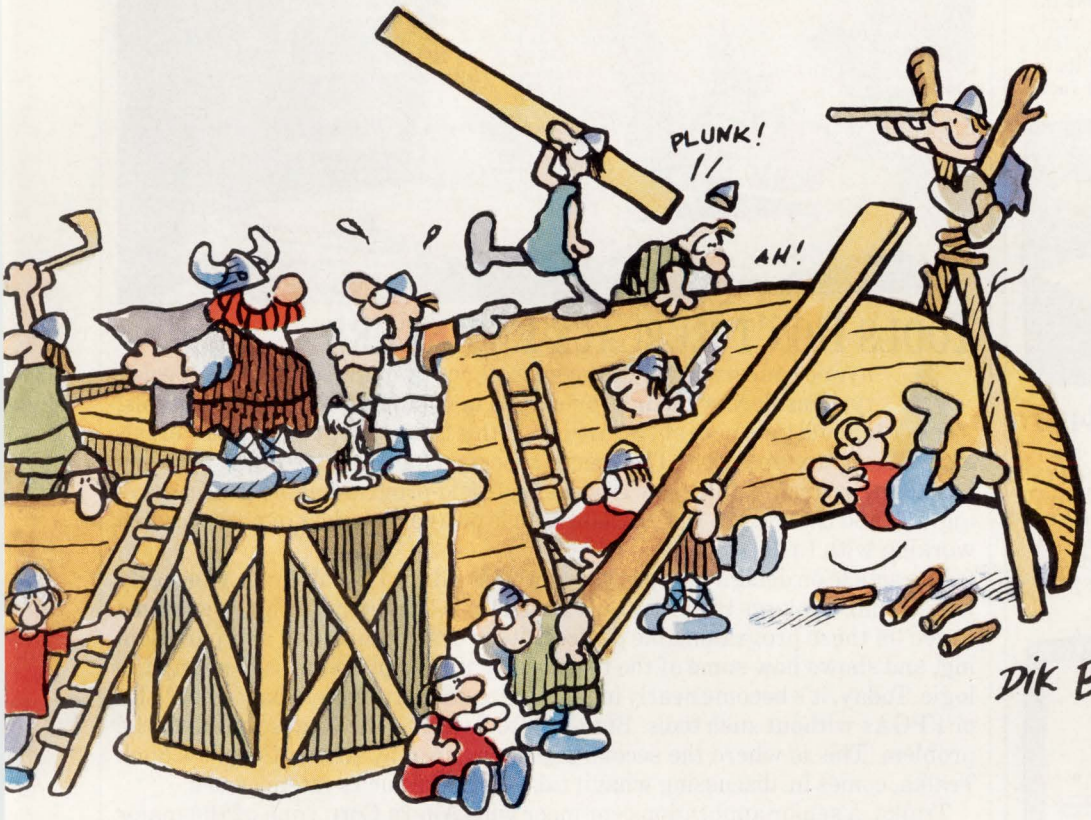
6000™ family.
will seem downright primitive.



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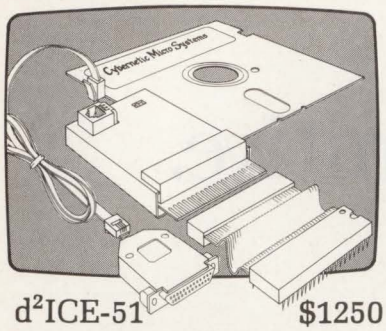
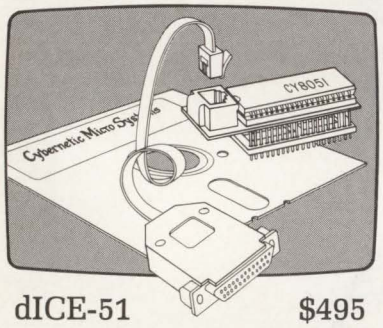


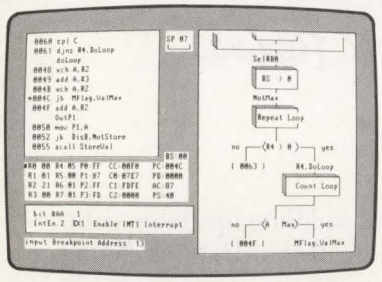
d²ICE-51 **$1250**

This Real-Time emulator is low cost and smallest sized full speed 8051 in-circuit emulator. Full access to hardware I/O. Includes all debugging features of Sim and dICE below. Fits in shirt pocket. Cross Assembler incl.



dICE-51 **$495**

This reduced-speed in-circuit 8051 debugger provides full access to I/O but will not run real-time. With the same user interface features as Sim8051 below, dICE-51 generates execution profiles during reduced speed execution. (CMOS and MIL also available.)



Sim8051 **$395**

This software Simulator/debugger allows 'no-circuit', debugging of 8051 code on IBM-PCs. All Cybernetics 8051 debug tools offer multi-window source code displays, symbolic access to data, single key commands, breakpoints, trace, full speed and single step execution, execution profiler, and more.

Other 8051 tools include:

Cross Assembler	$195
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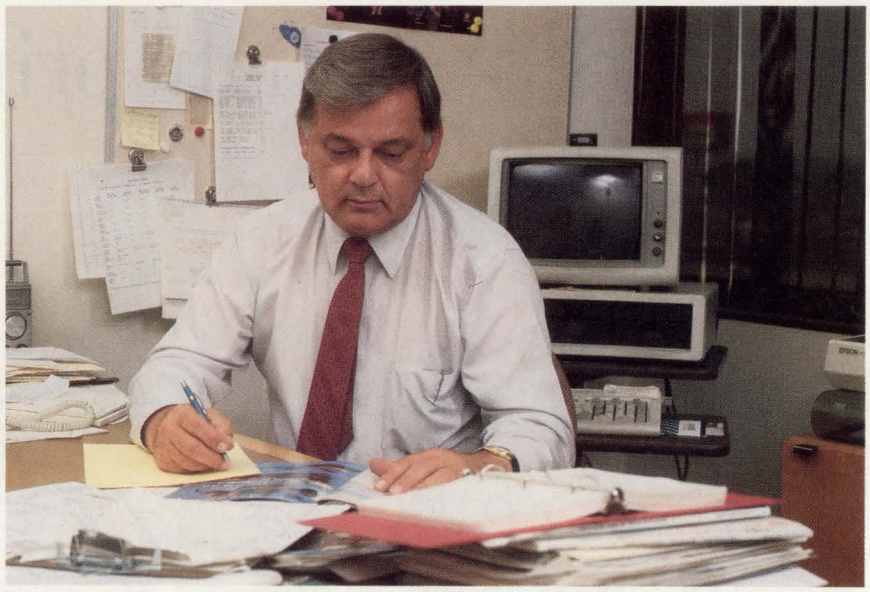
CIRCLE 88



TOOLS DON'T REPLACE ENGINEERS

Anyone concerned about the importance of engineering as a specialty, considering the improvements in computer-based design tools, should take note of two articles in this issue that present an interesting juxtaposition: The special report on tools for designing systems based on programmable logic devices and field-programmable gate arrays (pg. 55), and the Design Applications article on avoiding design pitfalls when working with PLDs (pg. 75).

The article on design tools, written by CAE Editor Lisa Maliniak (formerly Lisa Gunn), explores the many automated tools that help configure systems based on these programmable devices. It covers optimization and partitioning, and shows how some of the tools use synthesis procedures to set up the logic. Today, it's become nearly impossible to design a system based on PLDs or FPGAs without such tools. But those tools aren't the total solution to the problem. This is where the second article, written by Altera Corp.'s Chuck Tralka, comes in, discussing what it takes to make such systems work.

Tralka, a senior applications engineer with Altera Corp., one of the major suppliers of PLDs, bases his article on the many phone calls he has handled from designers struggling with system timing problems, glitches, ground bounce, etc.—the real-world problems that arise when the printed-circuit board prototype is assembled. Engineers are needed to solve these problems—that's what they get paid for. And, as far as we can see, they will continue to be needed for many years to come.

One final note: As much as engineers will be needed in the future, our salary survey on page 125 shows, we believe, that they're entitled to still more concrete recognition of their efforts. Simply stated, they deserve better pay. One of our readers, in his response to our survey form, commented that the farther away someone within the company is from the hands-on part of the project, the more they seem to get paid. We would like to hear your thoughts on the figures we cite in our survey. Fax us your opinions to 201-393-0637 or write to us at 611 Route 46 West, Hasbrouck Heights, NJ 07604.

Stephen E. Scrupski
Editor-in-Chief

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SPDT switch dc to 5GHz with built-in driver

Truly incredible…a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

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RF input, max dBm (no damage)	22	22	26
VSWR (on), typ		1.4	
Video breakthrough to RF, typ (mV p-p)		30	
Rise/Fall time, typ (nsec)		3.0	

*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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CIRCLE 101

A Look Ahead At TAB In The 1990s

DAVID MALINIAK
COMPONENTS & PACKAGING

As interconnection densities and data rates surge upward, component and circuit packaging must strive to keep pace or risk performance bottlenecks. Tape-automated bonding (TAB), which had its humble origins in low-cost watches and calculators, is a packaging technology that's now fulfilling its promise of high-I/O potential. At last month's SMTCON West Conference and Exhibition, Santa Clara, Calif., industry experts gathered to share their insights on the directions TAB technology will take in the 1990s.

A peek into TAB's future reveals a technology poised to spread into a myriad of applications. That's the main thrust of a paper by Howard E. Evans of IBM Corp., Austin, Texas, and Paul R. Hoffman of Olin Interconnect Technologies, Santa Clara, Calif. TAB requires a smaller die size than wire bonding for a given number of inputs and outputs. Its relative cost curve also crosses under that of quad flat packs once I/O count exceeds about 200. TAB also yields great benefits in IC testing and handling. For those reasons, among others, TAB is expected to fuel the accelerating trend toward greater packaging density.

Even as overall TAB usage grows, a trend toward use in more sophisticated system applications is apparent. The technology's expanding use in both low- and high-end computer systems will mean more TAB ASIC packages requiring more I/O, ground planes, and improved thermal performance. According to Evans and Hoffman, major ASIC vendors who aren't producing very-high-I/O, fine-pitch TAB ASIC packages have them in the works. Within the next two years, implementations will reach 500 or more leads with 0.25-mm outer-lead-bond pitches.

Ground planes for enhanced electrical performance up to near 100 MHz are also on the way. At least one major manufacturer of TAB film, Rogers Corp., Chandler, Ariz., has announced two-metal-layer TAB tape that incorporates a ground layer for improved impedance matching (ELECTRONIC DESIGN, *Sept. 27, p. 202).* 3M Corp., Austin, also offers a two-layer tape. Such tapes will pave the way for TAB's use in multichip modules for high-end system applications. These applications are being advanced by ongoing work at the Microelectronics and Computer Technology Corp. (MCC), an Austin-based consortium, and at Motorola Inc., Phoenix, Ariz., among others.

Still other applications harking back to TAB's consumer-product infancy will continue to exploit its low profile and light weight. For example, the volume of smart cards is expected to expand significantly. TAB is also replacing stamped lead frames in pin-grid-array and quad flat packages as their size, electrical characteristics, and thermal needs outstrip the limits of wire-bonding technology. Another burgeoning application for TAB is in stacked memory modules. These modules can take advantage of TAB's mounting density compared with wire bonding.

For flip-TAB applications, where chips are attached face down, integrated heat sinks will become more common, state Evans and Hoffman. Area-array TAB, which involves bonding to the active chip areas instead of to bonding pads at their edges, will also come into play to further decrease package size and cost. 3M's area-TAB tape incorporates through-holes that correspond to bumps placed on the chip. The result is high I/O counts without significantly increased die sizes.

Finally, to further aid TAB's widespread acceptance and universality, design guidelines were established under a joint EIAJ (Electronic Industry Association of Japan)/Jedec proposed standard. U.S. TAB vendors are now rallying around the standard, which includes compatibility with metric quad flat-pack sizes. Standardization will help drive TAB proliferation as new users will have access to available packages and their associated tooling.

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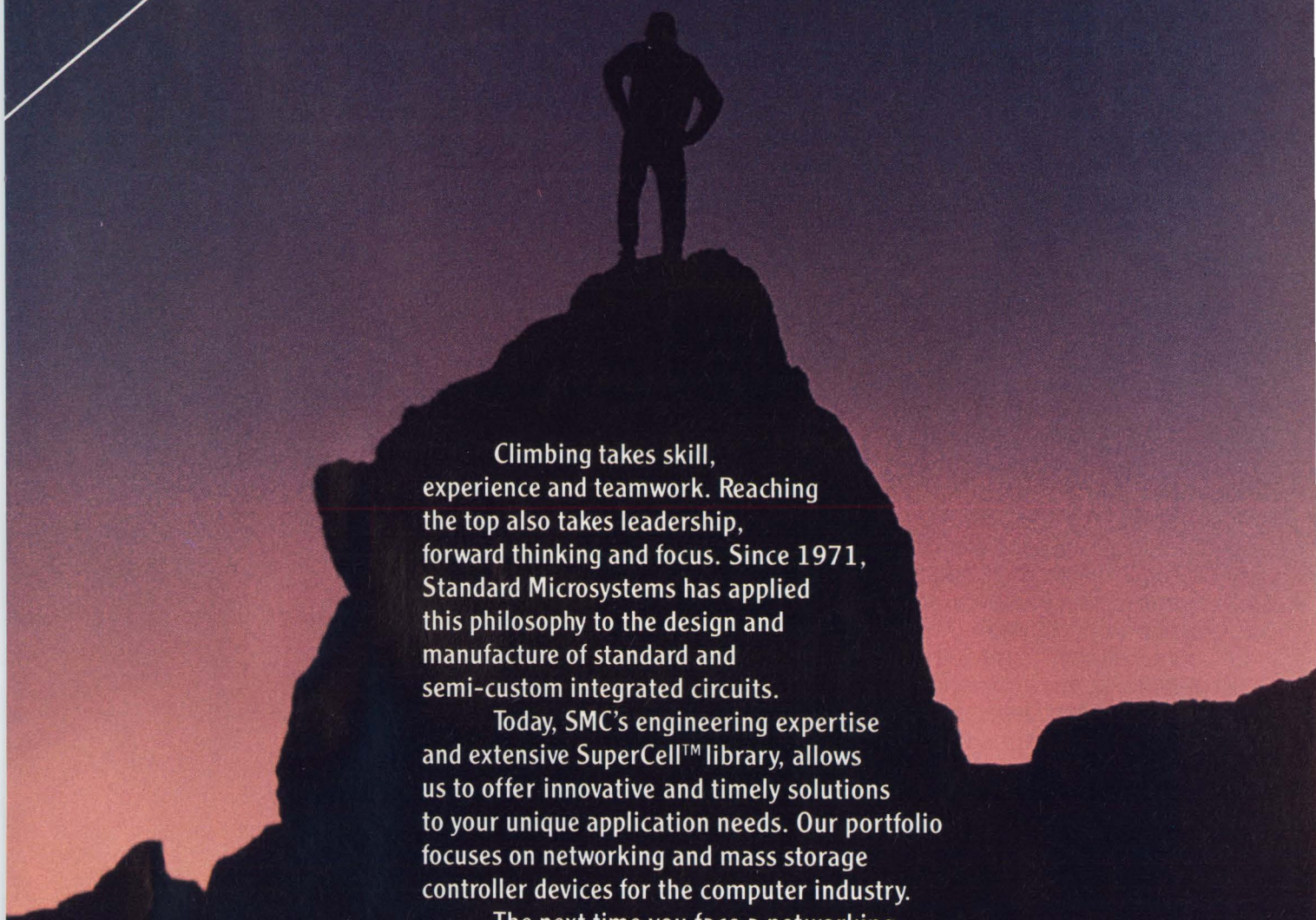

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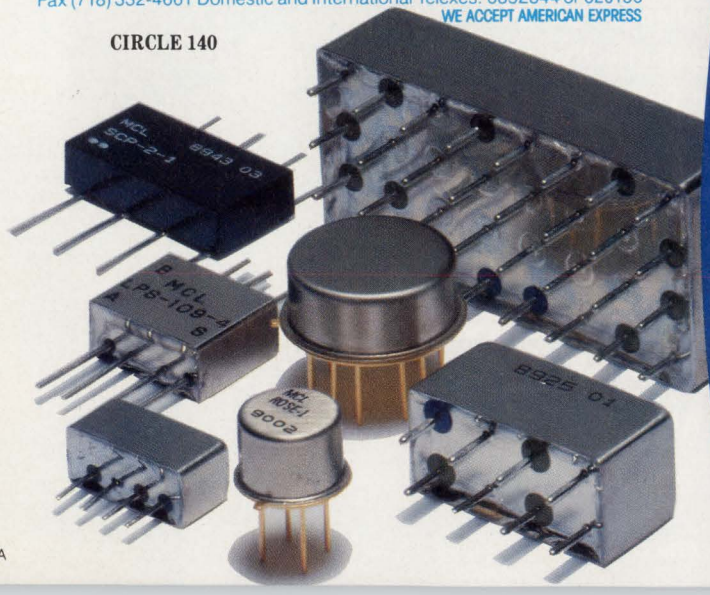

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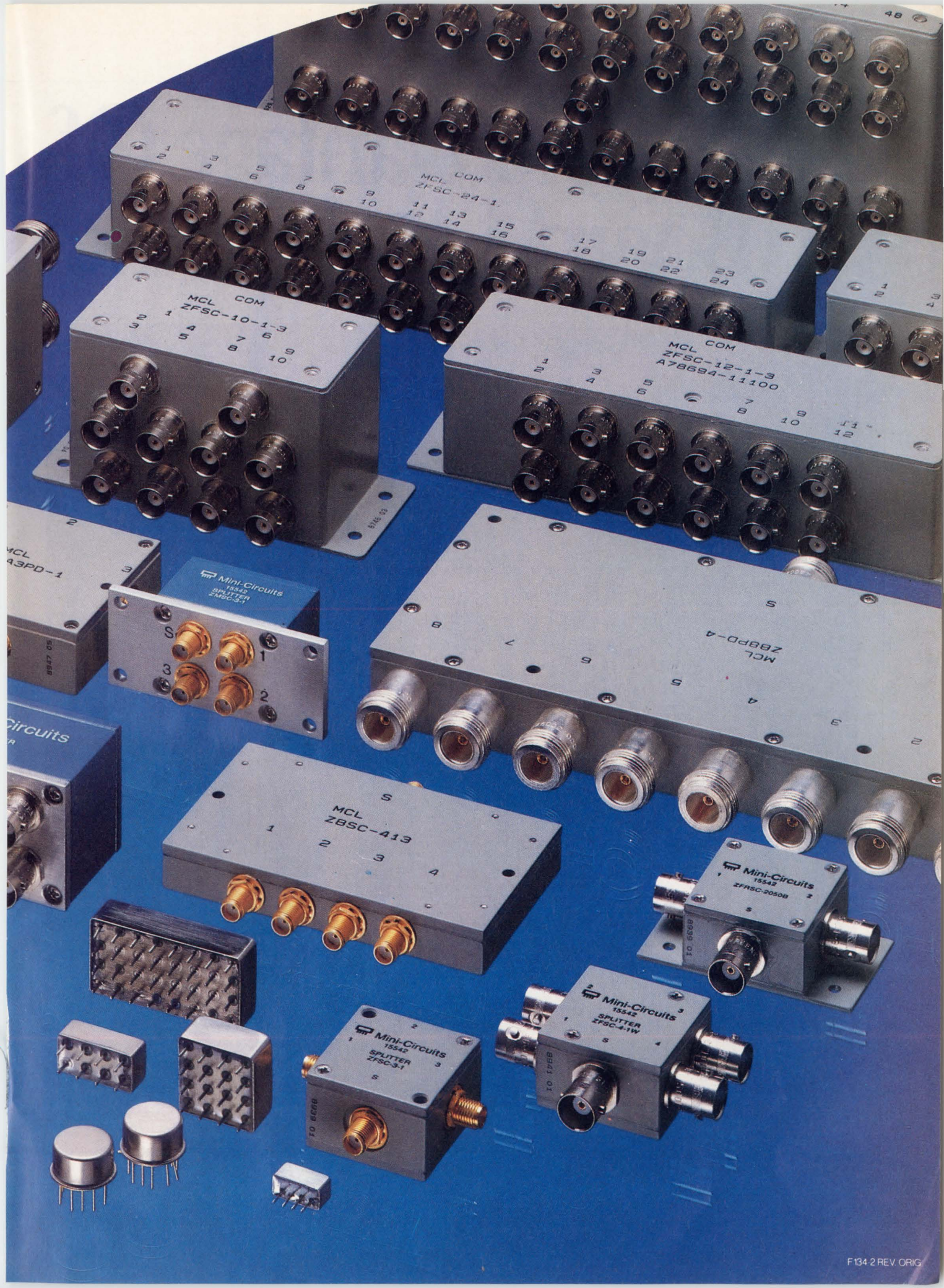

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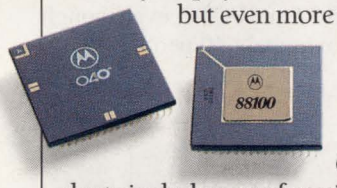

Our products include more functionality with a higher level of integration to accelerate your development efforts. And because of Six Sigma quality control you can be assured that our products will work right out of the box. It all adds up to the fact that getting you to market sooner is a promise only a company with the resources of Motorola can make good on.

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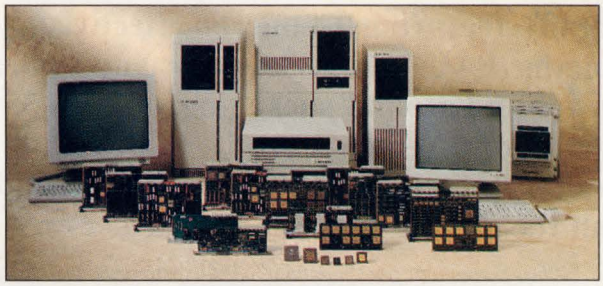

And we'll support you during the entire development process. Every board in our product line includes a full suite of board diagnostics available in both a run-time and a source package. This degree of flexibility also extends to our nationwide customer service programs, which run the gamut from total on-site maintenance to self-maintenance support packages.

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These days, openness has become something of a buzz word, and everybody seems to have a different idea on what is and isn't "open." To us, it's no big mystery. Openness means open architectures, open software, open networking. And open standards like UNIX,® as indicated by our role in founding 88open. It means we're open to helping solve problems with your point of view in mind, not just ours. And it's been that way ever since we helped introduce VME back in 1982.

That's why Motorola is committed to supporting official and de facto industry standards, interoperable computing between multiple vendors, and non-proprietary open system architectures. It's why we created VMEexec:™ to facilitate the interoperability of different real-time software modules within a common UNIX environment. And it's why we support virtually every networking protocol, including XNS, TCP/IP, DECnet,™ MAP/TOP/OSI, SNA, BSC, X.400, and X.25.

This philosophy of openness is the same reason we offer as many VME boards, products and services as we do. It's to our mutual benefit, and after all, isn't that what partnerships are for?

MOTOROLA
Computer Group

CIRCLE 112

3.3V Technology Breaks 5V Speed Barrier

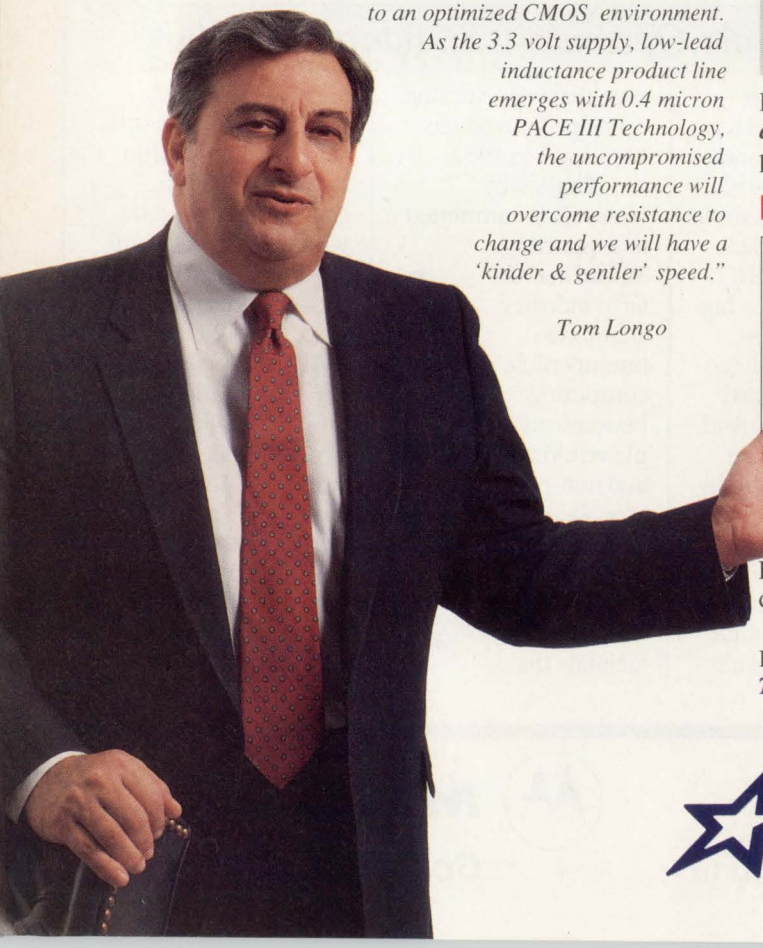
31 Logic Parts 35% Faster Than FCTA

A New Generation of 3.3 Volt CMOS Center-Pin Power and Ground Products with TTL-Like I/O.

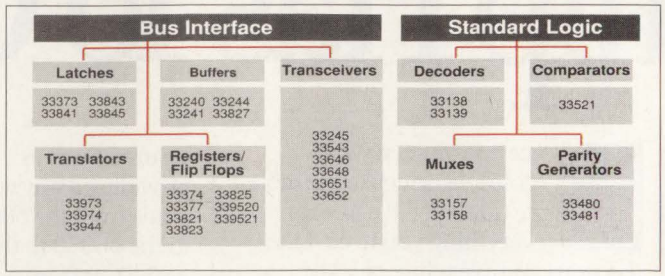
Performance's NEW 3.3V PCTD Logic Family, featuring 0.4 micron effective gate lengths (PACE III Technology) and center power and ground packaging, offers a 35% speed improvement over 5V FCTA, with dramatically lower power dissipation and half the ground bounce.

"It has been clear for some time that the primary consideration which could limit the use of future generations of CMOS technology in the highest speed applications were issues associated with constraints that have been hangovers from bipolar TTL circuit implementations. If those constraints are not removed, then either performance will be compromised or serious application problems will result. It is easy to see the value of the changes that are needed to take maximum advantage of the attributes of the fine-line CMOS technology in the sub half-micron regime (PACE III). Therefore, we have decided to invest a significant part of our Company's technical and marketing resources to help make the transition from a TTL environment to an optimized CMOS environment. As the 3.3 volt supply, low-lead inductance product line emerges with 0.4 micron PACE III Technology, the uncompromised performance will overcome resistance to change and we will have a 'kinder & gentler' speed."

Tom Longo

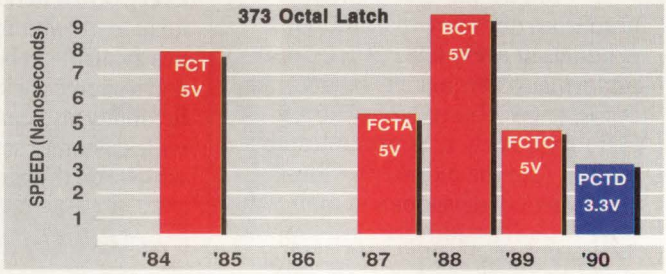


Performance's 3.3 Volt Logic Family



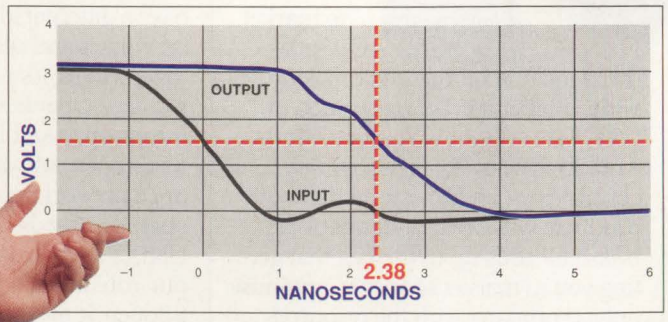
Twenty-five product types are available now with six more available by November, 1990. Included are buffers and latches designed for 5V to 3.3V logic-level translation without speed loss. Future superfast products, using center-pin power and ground with a 3.3V power supply, will include SCRAMs with 64 Kbit to 256 Kbit densities and PACEMIPs RISC processor products such as CPU, FPA and Wrap Functions.

CMOS Logic Performance Trends



Featuring TTL-like I/O, Performance's PCTD logic ***dramatically outperforms*** FCTA, BCT and FCTC, even though power dissipation is reduced approximately 40 percent.

P74PCT33373D 3.1ns (WC) Specification



Performance's P74PCT33373D offers a typical propagation delay of 2.4ns with extremely low noise.

For more information or to order Performance's PCTD Logic, call ***The Marketing Hotline: (408) 734-9000*** or write . . .

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CIRCLE 122

DISK-DRIVE GROUP FORGES TEST STANDARDS

A newly formed organization, the Post-HDA (head-disk assembly) Testing Consortium, will try to resolve the issue of a lack of test-data correlation for hard-disk drives. Hard-disk drives are one of the few computer peripherals that can't be field-tested accurately. The consortium has over 30 member companies and is open to major disk-drive makers and users, value-added resellers, test-equipment manufacturers, third-party service companies, and chip- and board-level controller firms. Spearheaded by FlexStar, a test-equipment manufacturer in San Jose, Calif., the Consortium will meet on Oct. 3 at the Sheraton Hotel in Milpitas, Calif., to agree on subcommittee recommendations for test definitions, testing methodologies, detailed test parameters, and test prioritization. Ultimately, the de facto standards will be submitted to the American National Standards Institute and other standards organizations to incorporate into their standards. Following the establishment of the test standards, associate membership will be available to those not directly involved in the manufacture, sale, or integration of hard-disk drives. Interested parties contact Mike Witte, FlexStar, 2040 Fortune Dr., #101, San Jose, CA 95131-1823; (408) 433-0770. *ML*

AUTOMOTIVE SYSTEMS MEET SILICON

With a view to cut the time-to-market and further improve product definition, Silicon Systems, Tustin, Calif., well-known for its disk-drive and modem chips, will team with Intelligent Controls Inc. (ICI), Novi, Mich., to develop advanced automotive electronic products. Over the last few years, Silicon Systems has designed custom signal-conditioning and data-acquisition ICs for automotive systems, including ignition, fuel-injection, anti-skid braking, and active-suspension applications. ICI, recognized in the automotive community for its system-engineering expertise and a leader in electronic engine-control system design, will aid in the design and evaluation of Silicon Systems' products and mixed-signal design capability for the automotive industry. For information call Lana Perry (Silicon Systems) at (714)731-7110, or Jerry Bricker (ICI) at (313)471-5000. *FG*

WORKGROUP COMPUTING GAINS SPARC PLATFORM

A combination of hardware and software will make it possible for millions of desktop computers distributed over large distances to share data quickly and easily. Xerox Corp., Palo Alto, Calif., in a joint designing effort with Sun Microsystems Corp., Mountain View, Calif., unveiled a Sparc-based workstation that handles the complex network environments. It also showed off an add-in coprocessor board for IBM and compatible PCs, and a proprietary workgroup software package it calls GlobalView. The software and underlying plug-in hardware can turn PCs into multitasking networked workstations. Those workstations, plus the new Sparc-based workstations, can be linked to form an enterprise-wide environment, potentially encompassing more than 30 million desktop computers. Contact Joseph McGrath (213) 333-7000. *DB*

SUPERSCALAR SUPPORT GROUP SETS STANDARDS

To ensure future software compatibility of systems using the Intel i860 superscalar RISC chip, a cooperative organization called MASS860 has been formed. The MASS860 will promote software development with a standard application binary interface (ABI). The organization was founded by Intel Corp., Santa Clara, Calif., and a number of concerned systems suppliers—Alliant, IBM, Oki, Olivetti, and Samsung. One of its goals is to reduce redundant development costs and shorten the time to market. The group's activities include forming open and published standards, creating an i860-based reference design, developing a suite of programs to test application packages for compliance to ABI, and establishing and supporting software libraries for ABI, operating-system, and graphical user-interface development. Intel will provide the hardware and software reference models. System-vendor members will supply the hardware porting platforms, software porting assistance, as well as perform the verification of ABI compliance. The program will be administered by Intel, offering in-depth education on the i860 through video tapes and classes. Intel also set up a porting center at one of its offices in Santa Clara, where technical support and compatibility testing will be supplied. *DB*

RISC CPUS SPAN HIGH- TO LOW-END SYSTEM NEEDS

To get more of its chips into embedded-control applications, Intel Corp., Chandler, Ariz., last month unveiled two low-cost versions of its i960 RISC processor—the i960SA and SB. In 80-lead quad-sided flat packages, they'll sell for a mere $19.20 and $25.00, respectively, in 1000-unit lots. To get the prices that low, the external 32-bit data bus of the standard i960 processor was shaved down to 16 bits. But the

chips still have a 32-bit CPU core with 32 32-bit registers. They hold the minimum four sets of local internal register cache (256 bytes total), a small, 512-byte internal instruction cache, and a simple, expandable, interrupt controller. The SA and SB are basically the same, except that the SB also includes an 80-bit IEEE-compatible floating-point unit. Even with a lower price, the performance remains respectable. The SA and SB operate at 10 or 16 MHz, and claim a Vax-comparable throughput of 5 MIPS (at 16 MHz). The SB's floating-point unit is rated at 0.5 MFLOPS. To move data into and out of the chip with minimal overhead, a special memory-bus interface assembles 16-bit transfers automatically into 32-bit words and vice-versa. An interface burst mode enables four sequential 32-bit words to be transferred in just 10 clock cycles. For higher performance, a 40-MHz 35-Vax-MIPs version of the 33-MHz i960CA was released. Contact Alan Steinberg (602) 554-8080. *DB*

IMAGE PROCESSING CARD ENHANCES NeXT COMPUTER

Adding image processing and compatibility with the Joint Photographic Experts Group standard, an add-in card for the NeXT personal computer combines both an image-compression processor and a 64-bit superscalar RISC processor. The card, developed by NeXT Computer Inc., Redwood City, Calif., is the first add-in card for any computer to employ the CL550 image-compression processor from C-Cube Microsystems, San Jose, Calif. It operates in tandem with the i860 processor from Intel Corp., Santa Clara, Calif. The NeXTdimension image-processing card plugs into one of the original NeXT cubes. It adds 32-bit true color, sophisticated drawing, image manipulation, rendering, and display capabilities to the computer. With the CL550, users can compress still images in real time and display full-motion video at up to 30 frames/s. Compression can be done at ratios of up to 100:1, depending on the application and the desired decompression quality. In addition to the new card, NeXT has also released a couple of new computer systems based on the 68040: an upgraded version of the 68030-based cube and a less-expandable desk-top configuration that sells for under $5000. In addition, C-Cube Microsystems unveiled Apple Macintosh NuBus and IBM PC/AT image-compression/expansion add-in cards that employ the CL550. The cards, which will sell for less than $1000, enable designers to experiment with still- and motion-video compression and expansion. *DB*

BIPOLAR SILICON KEEPS CHASING GaAs FETs

At the recent Bipolar Circuits and Technology Meeting in Minneapolis (Sept. 17-18), a number of bipolar silicon ICs containing transistors with f_ts beyond 15 GHz were divulged. A few of the highlights included:

A joint paper from Bellcore, Red Bank, N.J., and Avantek, Newark, Calif., described a parallel-processing 11-GHz decision circuit for next-generation SONET (Synchronous Optical Network) telecommunications systems. This speed represents an increase from 8 GHz for a nonparallel circuit. A decision threshold of 100 mV was obtained at 10 GHz. The circuit, which is a hybrid, employs master-slave D-type flip-flops made on Avantek's self-aligned silicon-nitride ISOSAT process. The process has 0.6-μm-wide arsenic-doped emitters, a 4-μm base-to-base pitch, trench isolation, a 2-μm-thick field-oxide isolation, polysilicon resistors, and two-layer Titanium-tungsten-gold metal. Transistor f_ts run 10-15 GHz and f_{max}s at 20 GHz.

If Signetics, Sunnyvale, Calif., has its way, PLD speed won't be limited by CMOS technology. In a technical presentation, Signetics described a PLD chip compatible with both 10K and 100K ECL, and able to run at clock rates of over 200 MHz, with gate delays under 4 ns. The PLD's core represents a two-level logic element with a 90-by-40 fuse-programmable AND array feeding 8 OR gates. In addition to 11 fixed inputs, the 12th doubles as a global clock signal. Eight output-logic macrocells, each containing an edge-triggered D-type flip-flop, along with output-select and feedback-select multiplexers, are also fuse programmable.

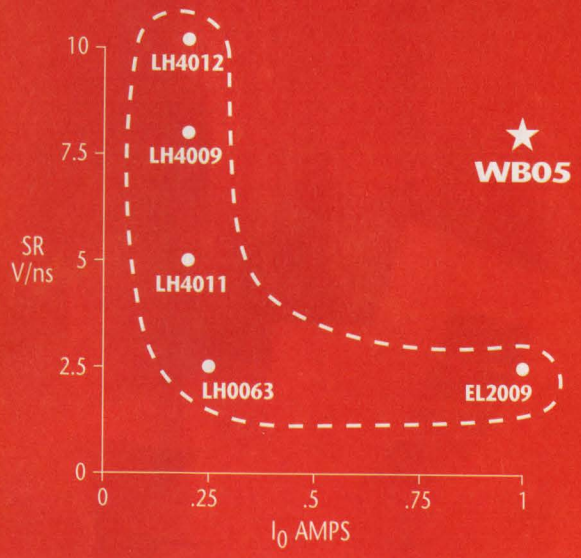
IBM hasn't been idle in this area either. A paper from their Yorktown Heights, N.Y., laboratory added what's probably the fastest JFETs to a 0.8-μm ECL process whose npn's sport f_{ts} of 25 GHz. The active JFETs replace the passive pull-down resistors in the ECL outputs. As the integration level of ECL circuits rises, the power required by each gate must be reduced. When operating in a low-power mode, the pull-down process tends to be slower than the pull-up routine in the typical resistor-load emitter-follower. The FET pull-down stage operates as a push-pull follower. It enhances the speed and drive of a 1-mW ECL gate by 25 and 50%, respectively. Moreover, not only is the FET smaller than the resistor, no process additions are required. For copies of the conference proceedings contact Jan Jopke, (612) 934-5082. *FG*

High-Speed Amplifiers

WB05

CURRENT BUFFER

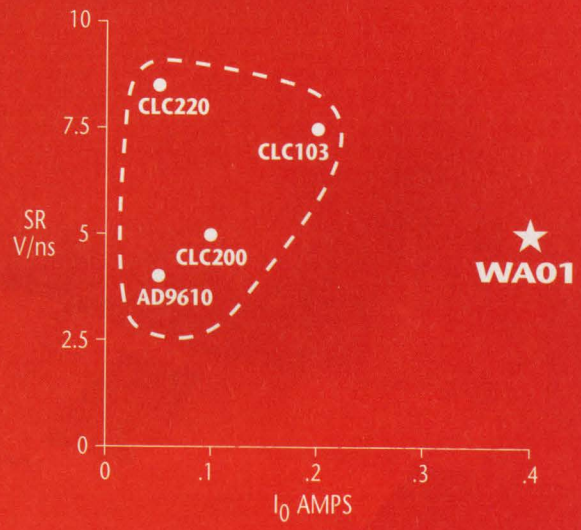
- 10,000 V/µs Slew Rate
- 1 Amp Output (1.5 A Pulse)
- ±5 to ±15 Supply
- 70 MHz Full Power Bandwidth
- Up To 15 Watts Dissipation



WA01

TRANSIMPEDANCE AMPLIFIER

- 4,000 V/µs Slew Rate
- 400 mAmp Output
- ±12 to ±15 Supply
- 40 MHz Full Power Bandwidth
- Up To 10 Watts Dissipation



APPLICATIONS

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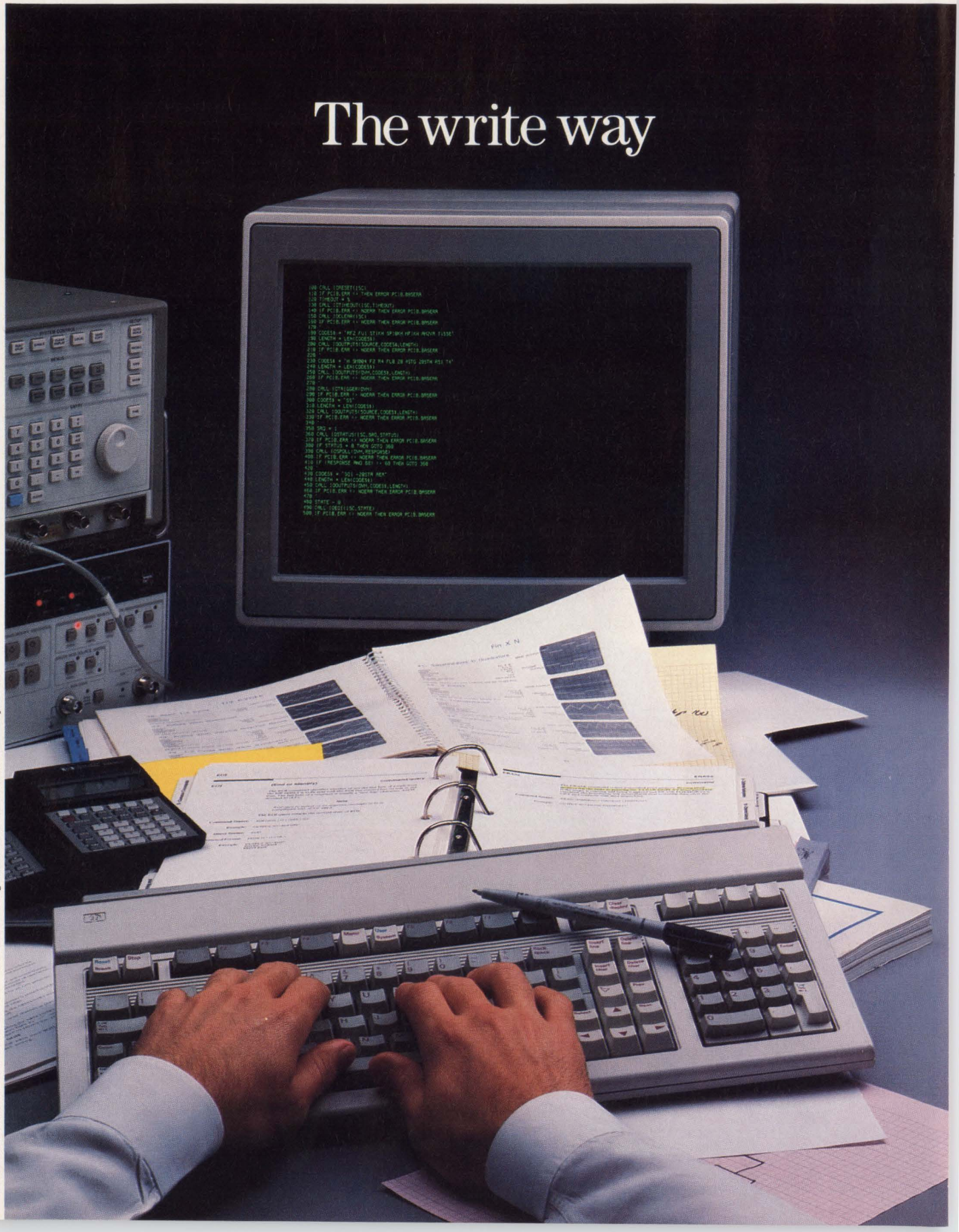
CIRCLE 174

Test development today:



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Now, HP's Interactive Test Generator delivers faster, easier test development on PCs, too.

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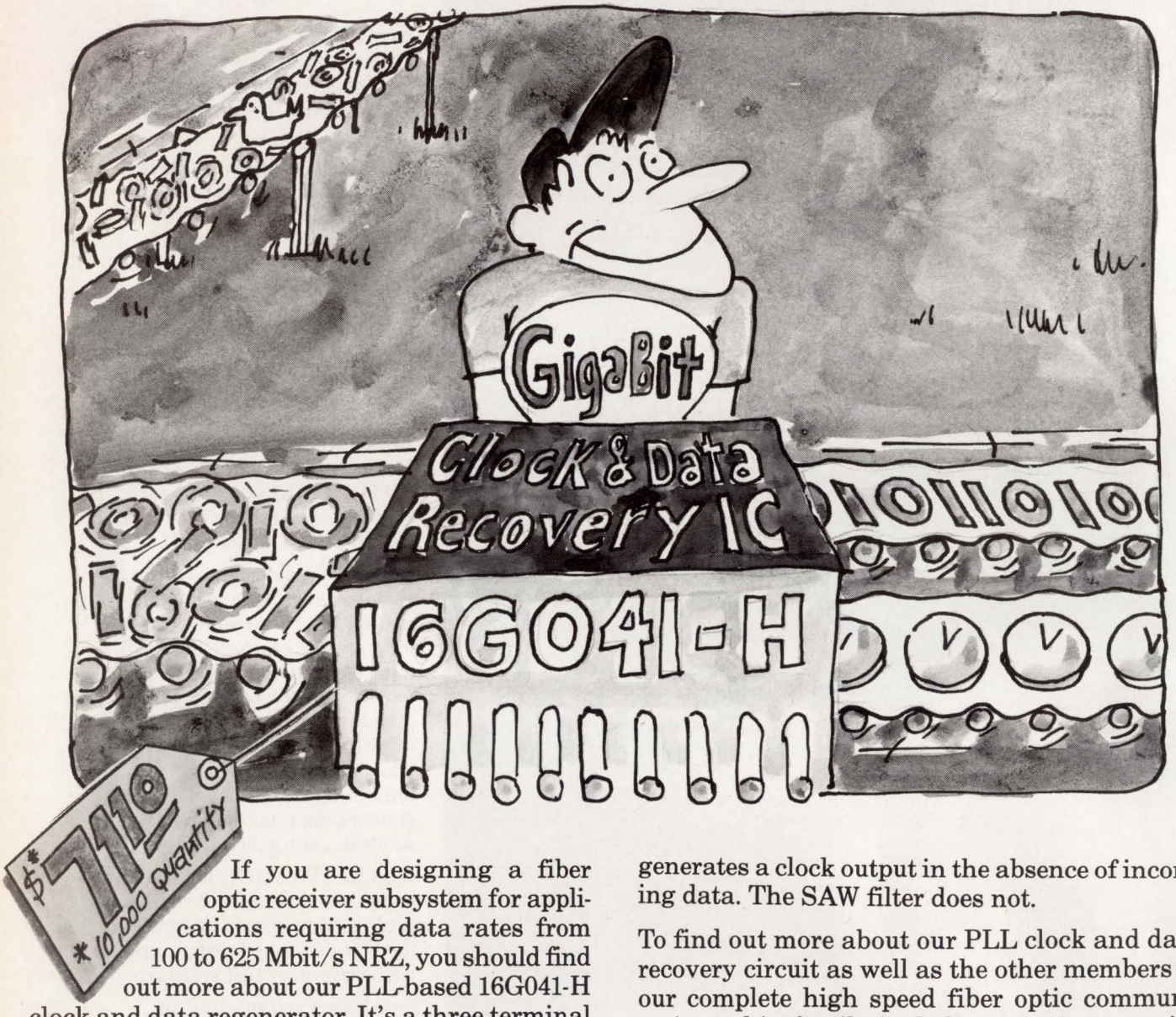
CIRCLE 93

From OC-3 to OC-12...

Regenerate your SONET signals with our PLL clock and data recovery IC.



If you are designing a fiber optic receiver subsystem for applications requiring data rates from 100 to 625 Mbit/s NRZ, you should find out more about our PLL-based 16G041-H clock and data regenerator. It's a three terminal (data in, clock and data out) device in a compact 1.25 inch x 1.25 inch flatpack package.

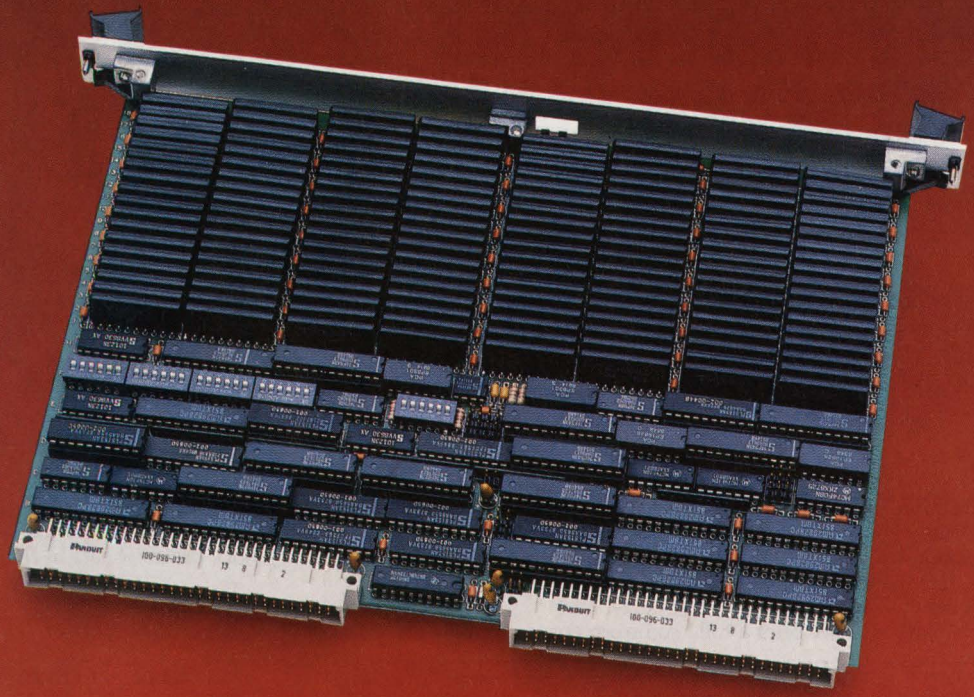
The 16G041-H synchronizes an internal VCO directly to an incoming data stream and simultaneously retimes and regenerates the data, unlike SAW filter clock recovery circuits which first filter the clock signal from incoming data and then retime it. Moreover, the 16G041-H generates a clock output in the absence of incoming data. The SAW filter does not.

To find out more about our PLL clock and data recovery circuit as well as the other members of our complete high speed fiber optic communications chip family including 16x16 crosspoint switch, limiting amplifier, transimpedance amplifiers, laser diode driver, LED driver, MUX and DEMUX, call us today. United States and Canada: (805) 499-0610, FAX (805) 499-2751; Europe: GIGA, at +45 4343 1588, FAX +45 4343 5967.

GBL GigaBit Logic

CIRCLE 166 FOR PRODUCT INFO.
CIRCLE 167 FOR CAREER INFO.

The Highest Density, Fastest, VME-Compatible Memory



Clearpoint, of course!

Advanced Chip Technology and Design

Get up to 64 MB of fast, VME-compatible memory in a single slot. Designed with state-of-the-art 4 Mb DRAM technology, Clearpoint's VMERAM-FP1 assures higher reliability through lower component count. Each of Clearpoint's VME-compatible boards supports all VMEbus addressing and data transfer types–block mode (BLT), unaligned (UAT), and address only (ADO).

The Fastest Byte Parity

The VMERAM-FP1, available in 4 to 64 MB, provides the fastest sustained block transfer timing available. Typical operating speeds boast 100 ns read and 74 ns write.

Our company-wide pledge to deliver reliability and performance.

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Quality Commitment

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Error Detection and Correction Options

Clearpoint offers several EDC boards for the VMEbus and the VSB subsystem bus. Our proprietary second generation EDC chip set with "extra bit" automatically replaces a bad DRAM and re-maps the array to include the new location.

- VMERAM-EC1: EDC with 64-bit cache and Clearpoint's exclusive "extra bit" technology, the VMERAM-EC1 includes 24- and 32-bit addressing, 8-, 16-, and 32-bit data transfers, and is available in 2 to 64 MB densities.
- VMERAM: The VMERAM is the low-cost alternative for EDC memory, with pricing comparable to parity memory. The VMERAM is available in 2 to 16 MB densities.
- VSBRAM-EC1: Features include "extra-bit" EDC and dual 64-bit caches for simultaneous transfer capabilities. Dual-ported for the VMEbus and VSB subsystem bus, the VSBRAM-EC1 is available in 2 to 64 MB densities.

The Clearpoint Difference

Clearpoint is a leading vendor in the VME marketplace, with the most comprehensive service program available. All Clearpoint memory products are covered by a lifetime warranty and a toll-free technical support hotline. Dedicated inventory in multiple locations worldwide support our 24-hour replacement program.

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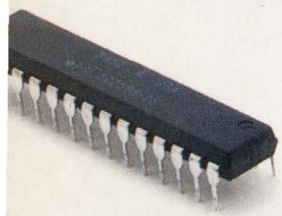
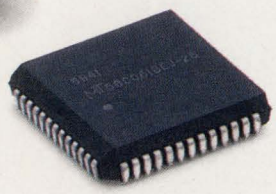
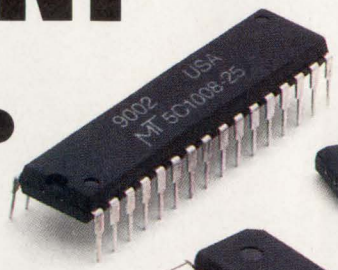
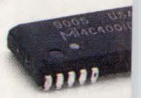
CIRCLE 121

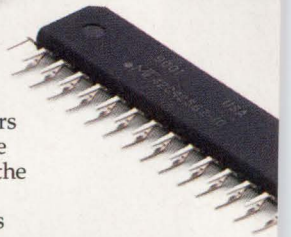
WE APPROACH THE MEMORY BUSINESS FROM ONE POINT OF VIEW...











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At Micron Technology, we offer a full line of leading-edge RAM components in speeds and packages for virtually any application.

But the memory business is more than just parts — it's people.

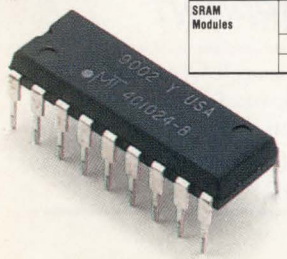
That's why we offer a total commitment to service and support, and a team of engineers and technical support personnel that are the most experienced memory professionals in the industry.

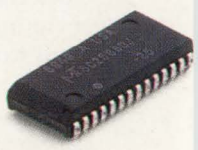
Because in the memory business there's only one point of view that counts. Yours.

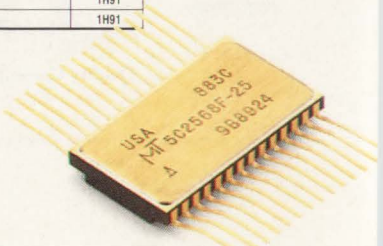
Component Product Family	Memory Size (Total)	Org. (Bits)	Speed (ns)	Package						Special Features	Availability	Military Qualified
				DIP	ZIP	SOJ	PLCC	TSOP	PQFP			
SRAMs	1MEG	x1,x4,x8	25-45	X		X				x4 option: OE	Now	2H90
	256K	x1,x4,x8	20-45	X	X	X				x4 option: OE	Now	X
	64K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
	16K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
Cache Data SRAMs	288K	x9	14-34				X			486 Compatible, Self-timed write, Fast toe 7ns, 486 Burst and extended burst support	Samp: 1H91, Prod: 2H91	
	144K	x18	20-35				X		X	386/486 Compatible, Fast toe 8ns, Auto write completion, Parity bits	Now	
	128K	x16	20-35				X		X	386 Compatible, Fast toe 8ns	Now	
Synchronous SRAMs	288K	x18	15-25				X			Registered address, chip enables and write control; Data latch, Fast toe 6ns, Byte write capability	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-25				X					
SRAMs with Address Latch	288K	x18	15-35				X			Address, data and chip enable latches; Byte write capability, Fast toe 6ns, 3.0 Volt output buffer option	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-35				X					
	16K	x8	100	X		X				Intel 8051 and 8096 compatible	Now	X
	16K	x8	15-35	X		X				Compatible with high end micro controllers	Now	X
FIFOs	18K	2Kx9	15-35	X			X			Family options: 300 mil DIP package, Programmable flags	Samp: 1H91	2H91
	9K	1Kx9	15-35	X			X				Samp: 1H91	2H91
	4.5K	512x9	15-35	X			X				Samp: 1H91	2H91
DRAMs	4MEG	x1,x4,x8,x16	60-100	X	X	X		X		x4,x8 options: Write per bit x16 options: 2 WE/1CAS; 1WE/2CAS and 1WE/1CAS with write per bit	x1,x4 Samp: Now, Prod: 1H91; x8,x16 Samp: 1H91	Samp: 1H91
	1MEG	x1,x4,x16	70-120	X	X	X		X		x16 options: Byte write or write per bit	Now	X
	256K	x1,x4	100-120	X	X	X	X				Now	X
	64K	x1	100-150	X			X				Now	X
Quad CAS DRAMs	4MEG	x4	60-100			X				Separate CAS control for each DQ input/ output, Enhanced write per bit capabilities	Samp: 1991	
	1MEG	x4	70-100			X					Now	
Pseudo Static DRAM	1MEG	x8	80-120	X		X		X		Unmultiplexed addresses, Simple refresh control	Samp: 2H90, Prod: 1H91	
Dual Port DRAMs (VRAMs)	1MEG	x4,x8	80-120		X	X				CMOS, Fully static SAM, Serial input, Split read transfer	Now	Samp: 1H91
	256K	x4	100-120	X	X					CMOS, Fully static SAM, Serial input	Now	X
Triple Port DRAMs	1MEG	x4,x8	80-120			X	X			CMOS, Two fully static SAMs, Transfer mask, Split transfers, Functional superset of 1MEG VRAM	Samp: Now, Prod: 2H90	

Module Product Family*	Word Size (Words)	Org. (Bits)	Speed (ns)	Package						Special Features	Availability	Military Qualified
				DIP	ZIP	SIP	SIMM					
DRAM Modules	2MEG,1MEG, 512K,256K	x36	70-120		X		X			Industry standard pin-out	256K, 512K: Now; 1MEG, 2MEG Samp: 2H90	
	4MEG,1MEG, 256K	x9	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
	4MEG,1MEG, 256K	x8	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
SRAM Modules	256K, 128K, 64K, 16K	x32	15-45		X					Industry standard pin-out with OE	16K, 64K: Now; 128K,256K: 2H90	1H91
	64K,32K	x16	30-45	X						Industry standard pin-out with OE	Now	1H91
	128K	x8	30-45	X						Compatible with 1MEG monolithic	Now	1H91

* Custom module and board-level product manufacturing services available.







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CIRCLE 141

DEVELOPMENT TOOL SIMULATES COMPLEX ICS VERY FAST

A development tool from Siemens AG simulates complex ICs up to 50 times faster than the universally used Spice (Simulation Program with Integrated Circuit Emphasis) program developed at the University of California at Berkeley in the late 1970s. The new tool, called Titan, drastically reduces the time to analyze a circuit. For instance, Titan can simulate a circuit with, say, 5000 transistors in just two hours, a job that would take Spice up to 100 hours.

Titan can also cope with much larger circuits. Whereas Spice was designed for devices with up to 500 transistors, the Siemens tool is targeted at circuits with more than 5000 transistors. These are analyzed with the same accuracy as Spice's: simulated and measured waveforms agree with each other to within 1%. Titan supports all types of circuits—bipolar, MOS, CMOS, GaAs, and others.

Titan's development was prompted by the challenges of ever-increasing circuit complexities. The critical path of a 4-Mbit DRAM, for example, contains some 6000 transistors. To analyze a read/write/read cycle in this case would take Spice more than a day of computing time on a large mainframe computer.

Moreover, Spice can't always come up with an initial solution and easily simulate strongly oscillating nonlinear circuits. It also lacks the flexibility needed for transistor modeling, and is difficult to maintain.

In shaping Titan, software specialists at the Siemens research labs in Munich, Germany, pursued four goals: improving performance by at least one order of magnitude, developing new analysis methods, creating the appropriate software, and designing a flexible model interface.

Titan runs on workstations, vector processors, and mainframes. But top speed and efficiency for large circuits is achieved with vector processors, Siemens says. That's because all algorithms and data structures are designed for best vectorization effects. What's more, a multidimensional table model for MOS transistors was developed, avoiding most of the problems associated with classical analytical models.

In addition to vectorization, Titan's high speed is derived from its exploitation of latency. Ordinarily, not all parts of a circuit in large devices are equally active at the same time. The Siemens program determines these differences in degree of activity and latency, and uses different computing time steps in the various circuit parts: Latent or less active parts are computed in time steps that are larger than those used in more active parts.

Siemens engineers believe that Titan is among the most efficient circuit simulation tools developed so far. Not only does it speed up the simulation process and handle larger circuits, it also has a high degree of universality. Therefore, classical algorithms can be used. The tool is now being employed by a number of design groups at Siemens. Eventually, the tool may be offered to outside customers.

JOHN GOSCH

IC PROMISES MORE COMPACT, RELIABLE ATE

In the real world, a design's success depends not only on the performance it achieves, but also on how well that performance matches users' needs and at what cost. In a classic case of balancing these engineering and product definition trade-offs, Brooktree Corp., San Diego, Calif., combined the load, driver, and comparator functions of automatic-test-equipment (ATE) pin electronics into one integrated circuit.

ATE LOAD, DRIVER, COMPARATOR OPTIONS

	Chip-and-wire hybrid	PCB, packaged MSI solution	Bt698
Pc-board real estate	3 in.^{2}	5 in.^{2}	2.5 in.^{2}
Quiescent power	3+ + W	2.5 W	1.6 W
IC count	10+	5	1
Reliability	Low	Medium	High
Heatsinking	Yes	Yes	No
Labor	Very high	Medium	Low
Price (100s)	$150-$200	$130-$175	$130

The resulting IC, the Bt698, has a high level of integration that offers ATE designers greater reliability, as well as the obvious savings in board space. The chip will make it easier to build the high-pin-count testers with tester-per-pin architectures that are in increasing demand.

To save space in the test head, designers previously resorted to making use of chip-and-wire hybrid assemblies. But these techniques raised both costs and power-dissipation levels *(see the table)*.

The main considerations that went into the Bt698 were a need for 100-MHz performance, low power dissipation, and small die size. The 100-MHz speed is a de facto standard for high-performance ATE. The low power requirement and small die reduce cost because a standard economical package can be used and an adequate yield can be delivered.

The key trade-off that resulted was an unusual partition of the load function that distributes power to six low-cost transistors off the chip. This unusual partitioning of the load function means that the Bt698 needs no exotic heatsinking or cooling scheme. It also means that the Bt698's worst-case load power of 250 mW permits the use of a 44-pin PLCC package.

Moving these transistors off chip increases the IC's reliability by lowering junction temperature. It also reduces the die size substantially. Including the transistors on the chip would raise power-dissipation levels to 4 W and add about $75 to the IC's price, which is $130 each in 100-piece lots, according to Brooktree.

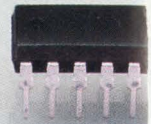
To further reduce the die

IN THE ERA OF MegaChip™ TECHNOLOGIES

APPLYING TI's BiCMOS

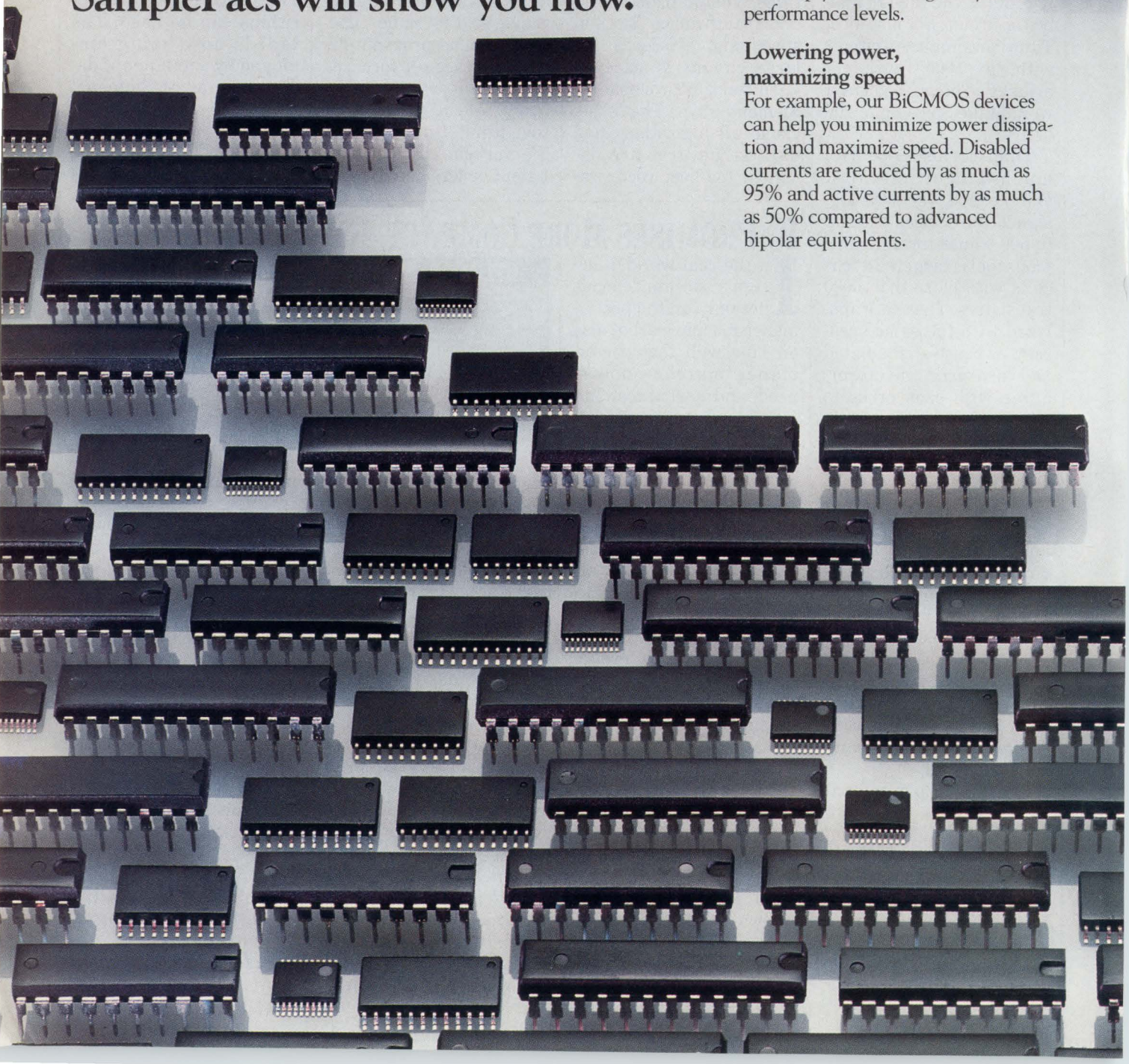
With more than 50 BiCMOS logic functions from Texas Instruments, you can beat tough bus-interface design challenges. Our free SamplePacs will show you how.

Specially designed for use in bus-interface applications, our growing BiCMOS logic family can make the difference in getting data on and off the bus faster. These advanced functions that combine the best of bipolar and CMOS can help you attain higher system performance levels.



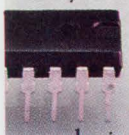
Lowering power, maximizing speed

For example, our BiCMOS devices can help you minimize power dissipation and maximize speed. Disabled currents are reduced by as much as 95% and active currents by as much as 50% compared to advanced bipolar equivalents.



DIFFERENCE

In fact, your system power savings can amount to more than 25%, and you should experience reduced switching noise as well.



Yet you can maximize system speed. Switching speeds are comparable to advanced bipolar devices and provide the high drive current required for today's industry-standard buses (48/64 mA commercial, 24/48 mA military).

Gaining even greater performance

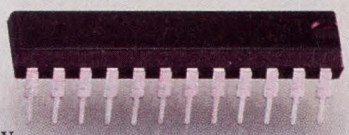
If you need even lower power and higher speeds, our submicron Advanced BiCMOS (ABT) family is the choice for you. Planned devices include 8-, 9-, and 10-bit buffers/drivers, transceivers, latches, registers, and registered and latched transceivers.

Our broad BiCMOS family also includes unique functions that can help you more quickly meet the design challenges involved with incident wave switching, driving MOS memories, and system testability.

Assuring incident wave switching

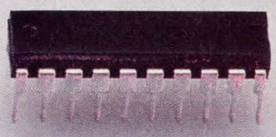
Wider word widths and additional cards on backplanes are requiring higher drive currents to assure incident wave switching.

Our BiCMOS family delivers. With our low-impedance line drivers, you get more "instantaneous" current even when impedances are as low as 25 ohms. You minimize transition "flat" spots that can degrade speed or cause oscillation at the receiving devices.



Managing MOS memory loads

MOS memory array interfaces create the high-capacitive loading environments that can result in overshoot and undershoot conditions. As a result, system reliability suffers. To handle this situation, our BiCMOS memory drivers incorporate a series damping resistor output structure that delivers advanced system performance when driving 256K, 1M, and 4M DRAMs.



Building in testability with SCOPE

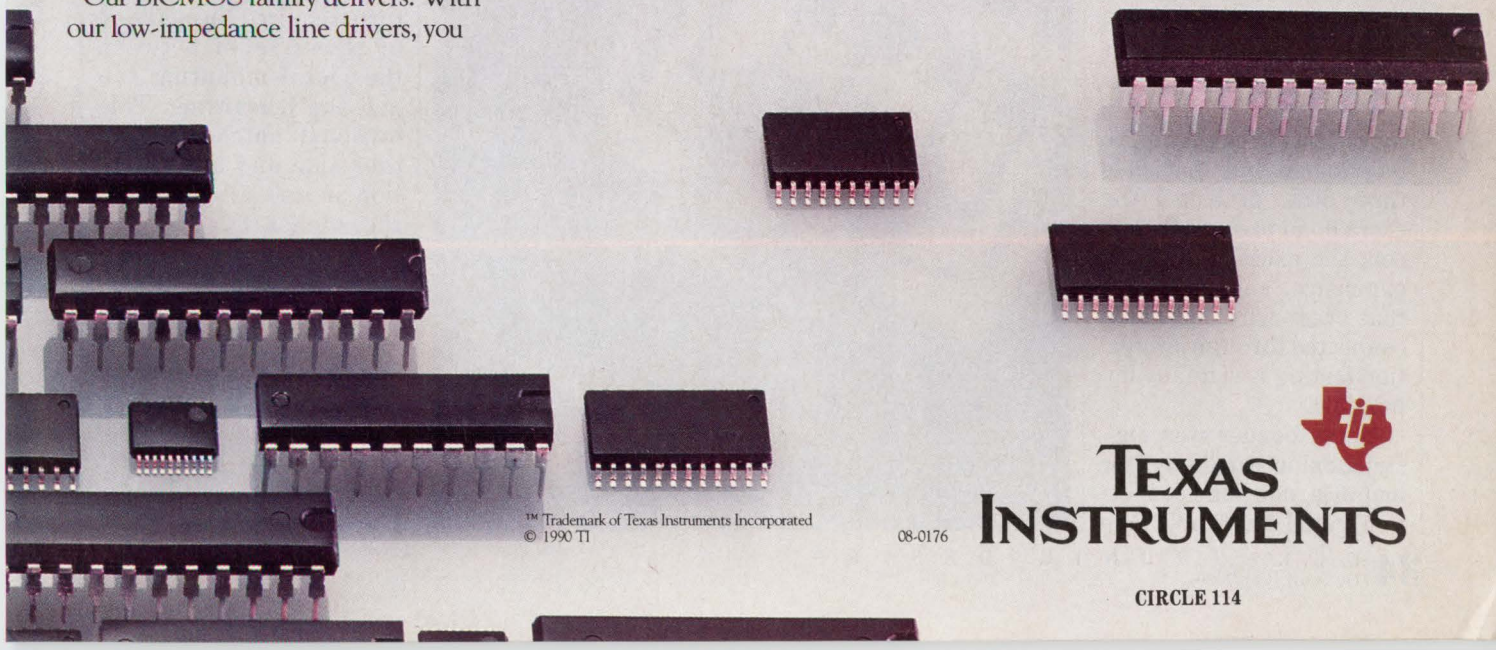
It is becoming more difficult to accurately test today's highly integrated boards and systems, but TI's BiCMOS family contains your solution: SCOPE™ (System Controllability and Observability Partitioning Environment) octals.

Used in place of standard octals, SCOPE devices allow specific circuitry within an assembled module, board, or system to be isolated for verification and debugging without manual probing. Currently, our BiCMOS family includes an octal buffer, transceiver, D-type latch, and D-type flip-flop.

TI's SCOPE products are the first to conform to the Joint Test Action Group (JTAG) specifications adopted by the IEEE 1149.1 Test Standards Committee.

Get your free SamplePac and sample our BiCMOS difference; call 1-800-336-5236, ext. 3008

You can take your choice of our BiCMOS SamplePacs containing a free BiCMOS device, our latest advanced logic brochure, plus appropriate product data. Just call the number given above, or use the return card to let us know which SamplePac you need to begin applying TI's BiCMOS difference.



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08-0176

TEXAS INSTRUMENTS

CIRCLE 114

size while optimizing performance, Brooktree did its own custom layout. A semicustom chip would not reduce the size enough to produce the yield, and the resulting cost, needed to make the Bt698 viable, the company says.

Brooktree also had to pay close attention to maintaining flexibility, because it could be sacrificed to achieve higher integration. Consequently, the Bt698's comparator logic permits window or edge-strobed comparisons, or both. Also, the digital inputs are differential, so they can be driven by ECL, TTL, or CMOS devices. Finally, the load section's variable gain optimizes the load's transfer function, so the chip needs no external op amps or buffers.

JOHN NOVELLINO

MIXING GOLD AND ALUMINUM BOND WIRES ON POWER ICS CUTS COST AND UPS RELIABILITY

A mixed-bonding technology development from SGS-Thomson, Agrate, Italy, and Phoenix, Ariz., enables power ICs to handle unusually high currents. The development involves combining thick aluminum and thin gold bond wires on the same chip.

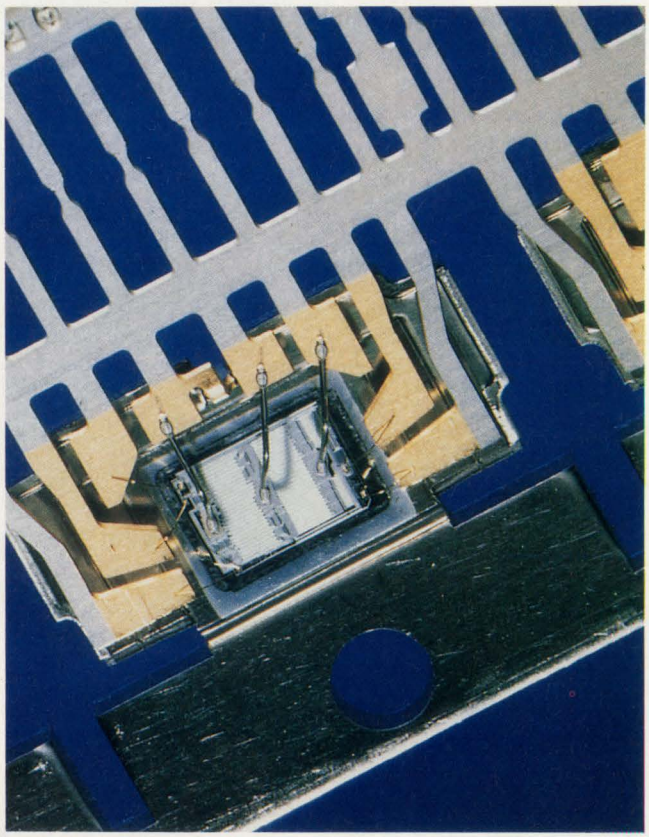
Putting power ICs into practical packages offers numerous challenges to IC-package designers. One key challenge is to get high currents, as well as diagnostic and control signals on and off the chip, and in and out of the package.

Fine, gold bond wires typically used for ICs can't handle high currents. Using multiple gold wires may allow more current to be handled, but that adds three other problems: the extra bond pads waste silicon, the excessive gold is expensive, and to ensure that every wire is reliably connected through production testing is virtually impossible.

If the bonder was malfunctioning randomly (for instance, one bond connection could have only one wire while all of the others have two, assuming that all connections are doubled), the cost of using redundant bond wires wouldn't help. Even thick gold wires aren't the answer—they add to the cost problem and are difficult to bond (however, multiple bonds distributed over an IC's power transistors eliminate the need for multiple, extra-wide, metal traces to bring all of the current from each power device to single bond pads).

Thick aluminum bond wires, similar to those used on power transistors, solve the current-handling problem. Yet they can't be used for the signal connections because of the large die area needed for each bond. Hence, SGS-Thomson tried mixing thin gold and thick aluminum bond wires, and they made it work by incorporating a few tricks *(see the figure)*.

For example, because gold is one of the few metals that will weld to aluminum, the copper leadframe is gold-plated. Moreover, apart from reasons of cost, gold must be used selectively, which means only on the portions of the frame within the molded package. In addition, if the complete leadframe were to be gold-plated, it would contaminate the tinning bath in which the pins are dipped, leading to possible reliability problems.



The mixed-bonded chip shown in the photo, a half-bridge motor driver, is to be used in an automotive multiplexing system and can handle 20 A while driving a window-lift motor. The technology has also been used with a 10-A switching regulator IC.

The package, called the Multiwatt-8, is an advanced version of the basic Multiwatt package developed by SGS-Thomson over ten years ago. This version has 8 in-line leads on 0.1-in. centers, rather than the usual two rows of staggered leads. Eight leads are used for high-current applications where extra-wide printed-circuit metal tracks must handle the current without the penalty of an appreciable voltage drop.

The new package also has a larger die flag to accommodate today's large chips. The large die flag, in turn, required the addition of stress relief between the metal mounting tab and the leadframe. This involved notches on either side and a convolution in the tab between the notches.

These two features ensure dependable adhesion between the leadframe and molding compound and isolate the die mechanically from the tab.

For additional information call, Tom Hopkins at (602) 867-6288.

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New Directions for MIPS RISC

An IDT RISC Technology Seminar

Seminar Outline
8:30 a.m. — 1:00 p.m., lunch included

I. **RISC Technology and Application Trends**
- Workstations and embedded applications

II. **Performance Analysis**
- SPEC™ benchmarks
- Embedded processor comparisons: 960 and 29K

III. **R3000 Architectural Overview**
- CPU and floating-point

IV. **New Directions for the MIPS Architecture**
- IDT RISController™ family:
  - R3001
  - R3051™/52™ and supporting chip set
- IDT RISCore™
- Next-generation MIPS R4000

V. **Applications Examples**
- Workstations
- Embedded processing
- Multiprocessing

VI. **Time-to-Market Strategies**
- Evaluation and prototype boards
- Development platforms
- RISC modules

VII. **IDT Future Roadmap**

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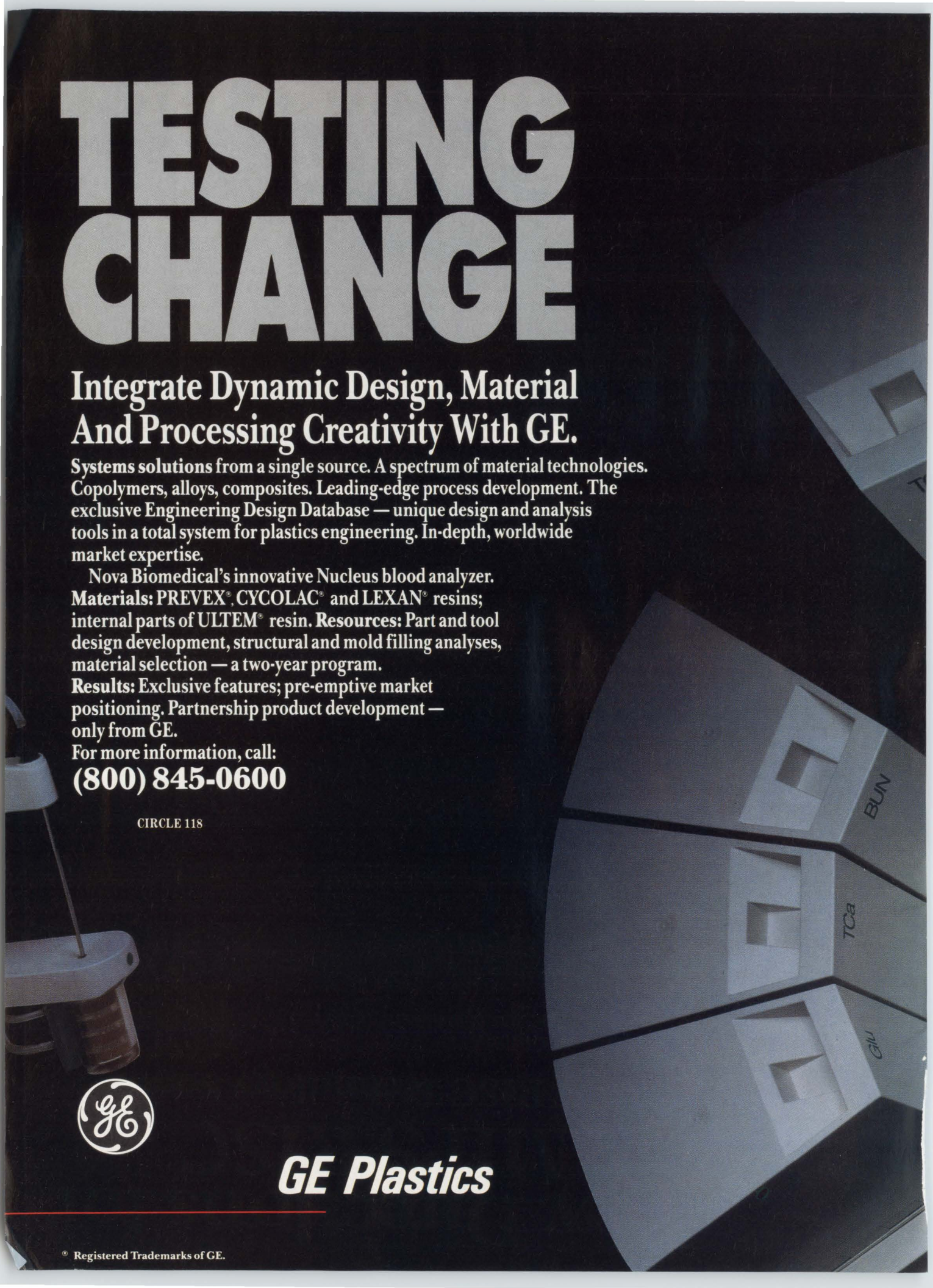

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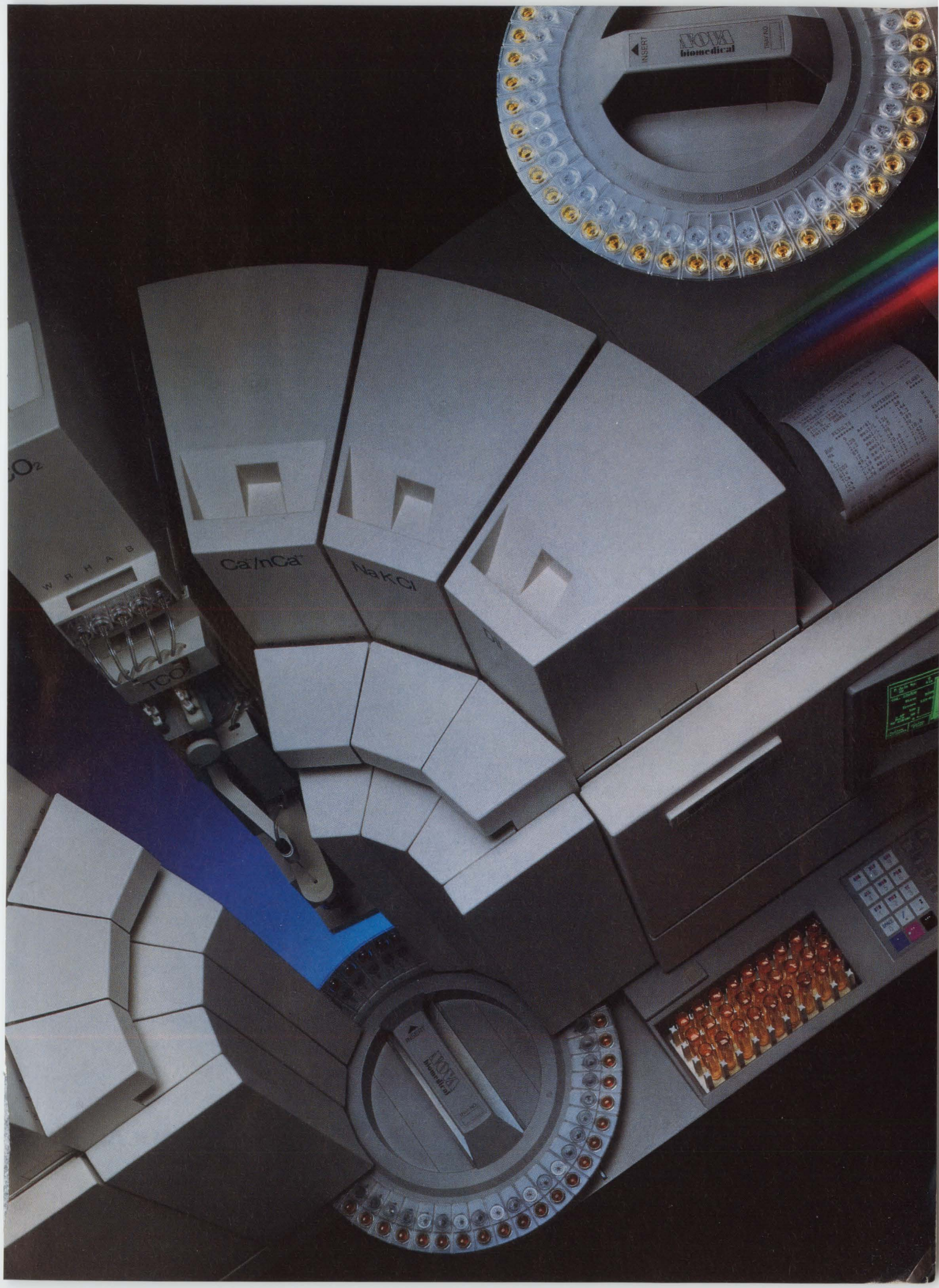
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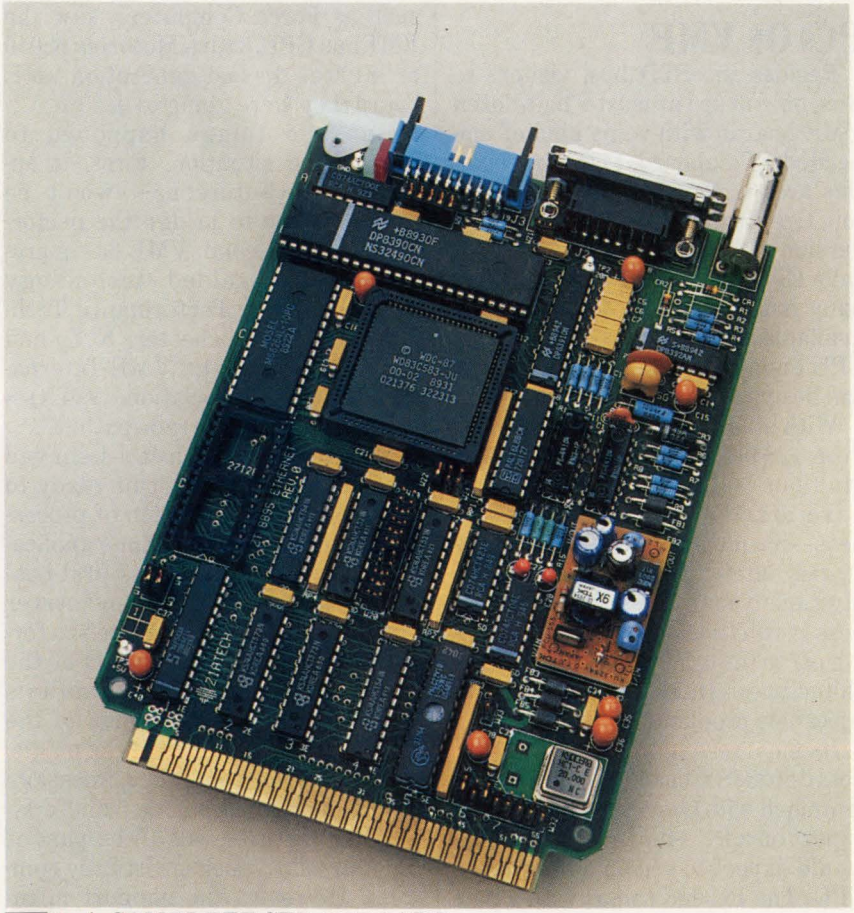
BUSCON PREVIEW: MORE POWERFUL BOARDS COMING

VME 64, STD 32, MULTIBUS I AND II, AND FUTUREBUS+ BOARD MAKERS EMPHASIZE "TOTAL" SOLUTIONS

ELECTRONIC DESIGN STAFF



1. A COMPLETE STD 32 BOARD, with a newly designed connector, is coming from Ziatech—the ZT 8895 Ethernet interface for the STD bus. Compatible with 5- and 8-MHz 8088 series products, it supports true 16-bit I/O and 20- and 24-bit memory addressing, as well as thick (802.3 10BASE5), thin (802.3 10BASE2), and pre-802.3 interfaces. The board comes with a PROM socket and is compatible with many software drivers.

This year's Buscon promises a broad spectrum of advanced board-level technologies. They range from the modest 8-bit I/O cards to 50+ MIPs cards sporting RISC processors, lots of memory, onboard SCSI, and the capability of transferring data in 64-bit blocks at close to 80 Mbytes/s. This Buscon also marks a turning point for the board-level industry: It's emerging from an industry with a handful of small companies assembling and selling boards, to one where companies must offer customers complete solutions—including software.

While Futurebus+ will be at Buscon, it's not going to steal the show as it has for the past few years. In fact, it's unexpected that any one technology will dominate the show floor—or seminars. Instead, we'll be looking at some of the early offspring of ideas announced at previous shows. Most notably, a rash of VME 64 hardware is expected from almost a dozen different vendors. In addition, the STD 32 bus will make its formal debut now that the connectors are commercially available.

Though many of the vendors will

bid on the traditional real-time instrumentation and control business, a growing faction is eyeing the workstation and Unix-based server business. Both Digital Equipment Corp., Maynard, Mass., and Sun Microsystems Inc., Mountain View, Calif., have staked out space in the Marlboro, Mass. exposition hall, underscoring the heavy systems implications in the board-level business.

Furthermore, many board companies or divisions have swung over to the systems business. Representatives of Intel Corp., Hillsboro, Ore., for example, will sport "Intel Systems"name tags. Motorola's Microcomputer Division (MCD) switched to systems in dramatic fashion earlier this year with its VMEbus-based workstation announcement.

But despite the efforts of board makers in the software area, there's a perpetual shortfall of software as new hardware emerges. A strong trend over the past year-or-so is to include some kind of PC-compatible machine on the standard buses. This lets system designers take advantage of all the software at hand for DOS-based machines. It also greatly simplifies the job of supplying a friendly human interface to the system. In the case of the STD Bus, vendors adopted the bus and DOS operating system in total, simply exchanging the ISA bus for the STD.

This led to the early adoption of a multiplexing scheme for the 8-bit bus so that it could be fully PC/AT-compatible, handling 16-bit transfers. But the multiplexing scheme wasn't totally accepted; only a handful of STD board makers adopted it. Meanwhile, Ziatech Corp., San Luis Obispo, Calif., developed a fully compatible extension of the bus, allowing for full 32-bit transfers.

Since its introduction one year ago, the STD 32 bus has been the subject of much controversy among STD board makers. So far, only a small group of vendors has committed to the bus and have banded together under the title of Task Group 32. The group has finalized the specification, settled some potentially nagging legal questions, and contracted for the manufacture of the special connector. Tooling on the connector is completed, and Ziatech, among others, will show the first real STD 32 systems this month with a working connector *(Fig. 1)*.

Ziatech reports that at least nine products from three manufacturers will take to the show floor. Pivotal to the new products is a processor board from Ziatech with a 286-like processor designed as a multibus master using STD32's EISA-like protocols. Other products debuting include a high-performance ADC board—the first full 16-bit peripheral ever to emerge on STD, a digital I/O card, a 16-bit Arcnet card, and an arbitration board for the slot-zero function. Jim Eckford, Ziatech's vice president of marketing, hints that a full-blown 32-bit processor card with an Intel 960 is in the works, but won't be ready at show time.

PCs On VME

Besides the STD bus, visitors to Buscon will see at least a half-dozen VME boards with some kind of embedded PCs aboard. One pioneer in this area is RadiSys Corp., Beaverton, Ore. The firm developed its own version of a mezzanine bus, which it calls EPC (embedded PC). The company has a number of EPC boards available as well as a selection of CPU engines. Some new EPC magic can be expected from RadiSys.

With all of the talk of 32-, 64-, and even 128-bit buses, it's obvious that Multibus I—generally considered to have started the open-bus business—hasn't been headlining many stories lately. But Intel and other Multibus I makers report that business is still brisk despite a slight falling off to the other more "flashy" architectures. Intel continues to release new products.

Its most recent product is a single-board 80386SX-based PC *(Fig. 2)*. It's crammed with everything one would expect on a PC—and everything one would expect to see on a Multibus I CPU. The PC end comes with a pair of serial ports, a parallel port, floppy- and hard-disk controllers, keyboard and mouse connections, a math coprocessor socket, and a piggyback VGA graphics board. On the Multibus I side, there's full Multibus I interface and control circuitry, dual-ported memory, and an iSBX expansion port.

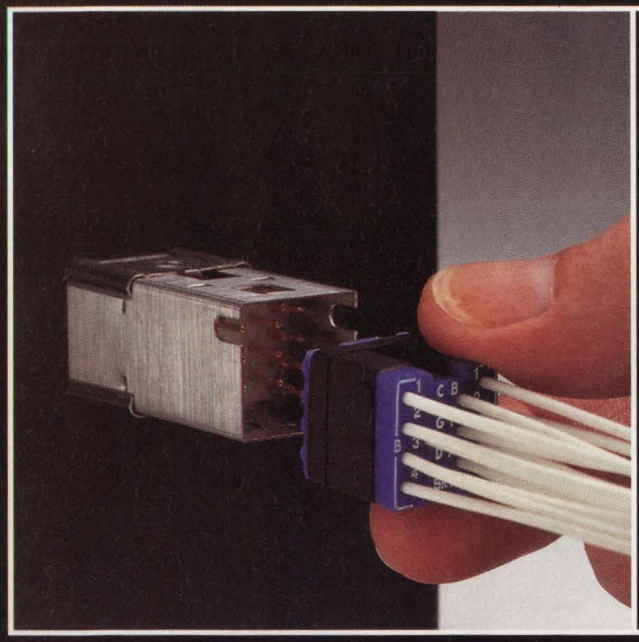
Intel points out that one of the more important aspects of the board concerns how it adapts to a real-time environment. The board can run DOS as a task in its iRMX real-time operating system. Obviously, the DOS task takes a low priority so that the real-time performance isn't impaired. And while DOS performance suffers as the system gets involved in higher-priority tasks, for most applications there's little penalty.

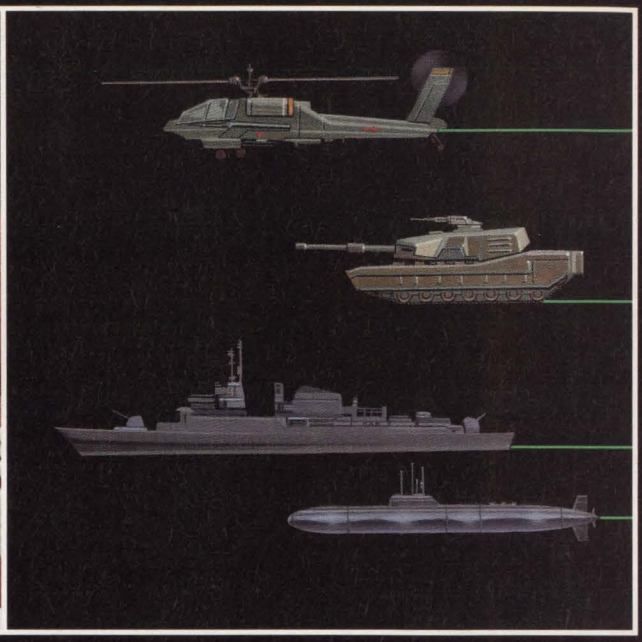
As one part of the board community looks at PC compatibles, others face the next generation in performance. As recently as last Buscon in February, optimists looked to Futurebus+ as the next step in standard-board performance. Many leaders, such as Force Computers, saw the VMEbus CPU with a Motorola 68040 or 88100 as the last-generation VME board they were going to design.

But two things happened to change the situation. First, it appears that Futurebus+ won't be ready in time to bridge the performance gap. Second, VME 64—a previously unheralded technology spearheaded by Performance Technologies Inc., Rochester, N.Y., and now adopted by the VME International Trade Association (VITA)—provides a VME upgrade path.

Moreover, though it's believed that Futurebus+ won't be ready to serve the next generation of processor technology for real-time applications, it's likely to have its first trial in advanced workstation and server applications. DEC is expected to formally announce its profile B of the P896.2 specification. The B profile is a stripped-down I/O version of the bus that removes much of the magic, such as cache coherency, message passing and packet-mode transfers.

These features will all be part of the A profile, which is virtually complete. However, the support infrastructure for the bus hasn't yet emerged. With the aggressive stance of both DEC and Sun Microsystems in the Futurebus+ arena, it was widely believed that semicon-





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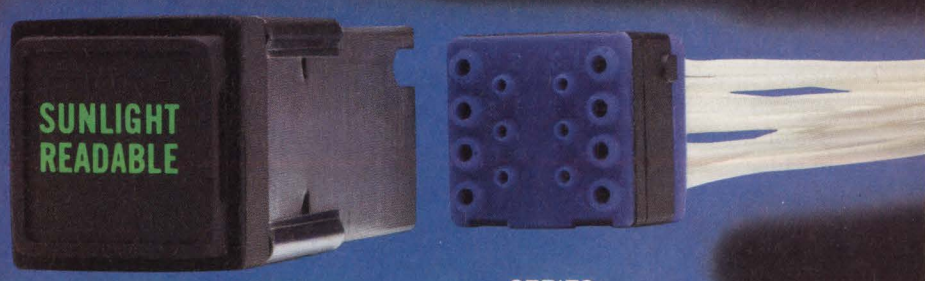

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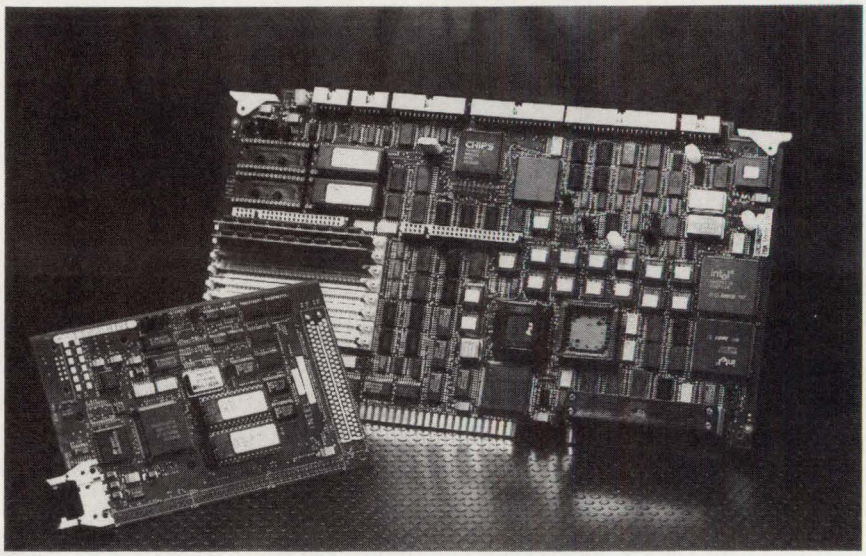
ductor makers would jump on the bandwagon immediately and offer a broad selection of controller and interface chips. Instead, the major manufacturers have played their cards very close to the vest and developed custom interface and controller chips, rather than look to the IC makers for standard products.

Texas Instruments Inc., Dallas, National Semiconductor Corp., Sunnyvale, Calif., and the Philips Components-Signetics Co., Sunnyvale, Calif., have said they'll produce standard chips. But only an interface chip from National and samples of a chip set from Signetics have emerged (ELECTRONIC DESIGN, *May 10, p. 63*). Indications are that some new introductions will be made, but chip makers have stood back a bit to see where the market will go.

The hiccup in the reality schedule of Futurebus+ left a gap in performance for VMEbus systems developers. VMEbus has been stretched in performance through various approaches, and there's little room to add more. On one side, performance was increased by applying very high-performance mezzanine buses, such as Heurikon's CoreBus; Matrix' DBus; the EVSB bus from Motorola Semiconductor Products, Phoenix, Ariz.; and Radstone Technology's APEX bus. In addition, the VSB bus standard on the P2 connector was also used to enhance performance.

On the other side, vendors added multiple on-board local buses to do as much processing on the main CPU card as possible, leaving only I/O functions on the main system bus. Still, VMEbus system performance can't keep up with the demands of newer processors. The response is to expand the bus through the clever use of the existing address lines during block transfers.

Because addresses aren't needed in block transfers where sequential addresses are transmitted, the VME 64 approach uses the address lines to transfer data after the starting address is sent. This approach is fully compatible with existing VME hardware, yet provides a full 64-bit data path for boards in the system using VME 64. Data-transfer rates close to the theoretical 80 Mbytes/s have been achieved, and they promise to carry VME at least through another processor generation.



2. THIS SINGLE BOARD (background) from Intel, the iSBC 386SX, has everything one would expect from an 80386SX Multibus I PC. The iSBC 272 graphics module (foreground) piggy-backs onto the main board to provide VGA graphics.

While the VME community is stirring up its customers with 64-bit transfers, Multibus II is seeing a revitalization. Like their VME cousins, Multibus II manufacturers envision Futurebus+ as a path to higher performance. However, its model considers the bus as a high-performance, cache-coherent processor-to-memory architecture, and not as an I/O bus. Intel, the industry's leading Multibus II manufacturer, is billing Multibus II as the I/O of Futurebus+. Intel is capitalizing on some of the activity surrounding Futurebus+ by demonstrating that Multibus II already has many of the advanced features of Futurebus+, such as autoconfiguration, and it's available now. Intel also claims that when Futurebus+ is available, it will provide a smooth bridge for performance enhancements.

Multibus II also got a boost earlier this year when Siemens, the largest Multibus II maker in Europe, decided to market its products here, to join the Multibus II Manufacturer's Group, and to share technical information with U.S. Multibus makers. The move gives Multibus a leg up in a badly needed area, which is having a critical mass of products available. Multibus II sales have steadily increased over the past year, but still fall far behind VMEbus.

Ten years ago, the board business began as a standard way of adding memory to a processor system because there wasn't enough room on one board. Today, open-architecture systems battle it out against proprietary bus systems for control of real-time applications, workstations, and servers. Traditionally, proprietary buses have held the lead.

But that may soon change. The two hot areas to look for exceptional sales increases of board-level products are in workstations and servers. Most industry leaders are already looking at standard buses; DEC is turning to Futurebus+, VME, and TurboChannel, while Sun is taking a similar stance, replacing TurboChannel with its own SBus. IBM Corp., Armonk, N.Y., is sticking to its for its RISC-based workstation. And other workstation and minicomputer makers have begun to take a long, hard look at open, standard-architecture buses.□

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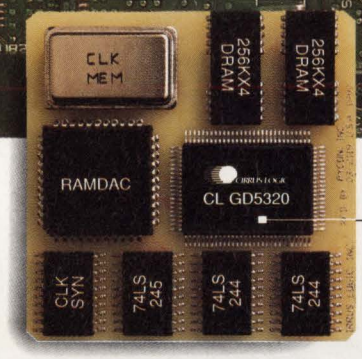

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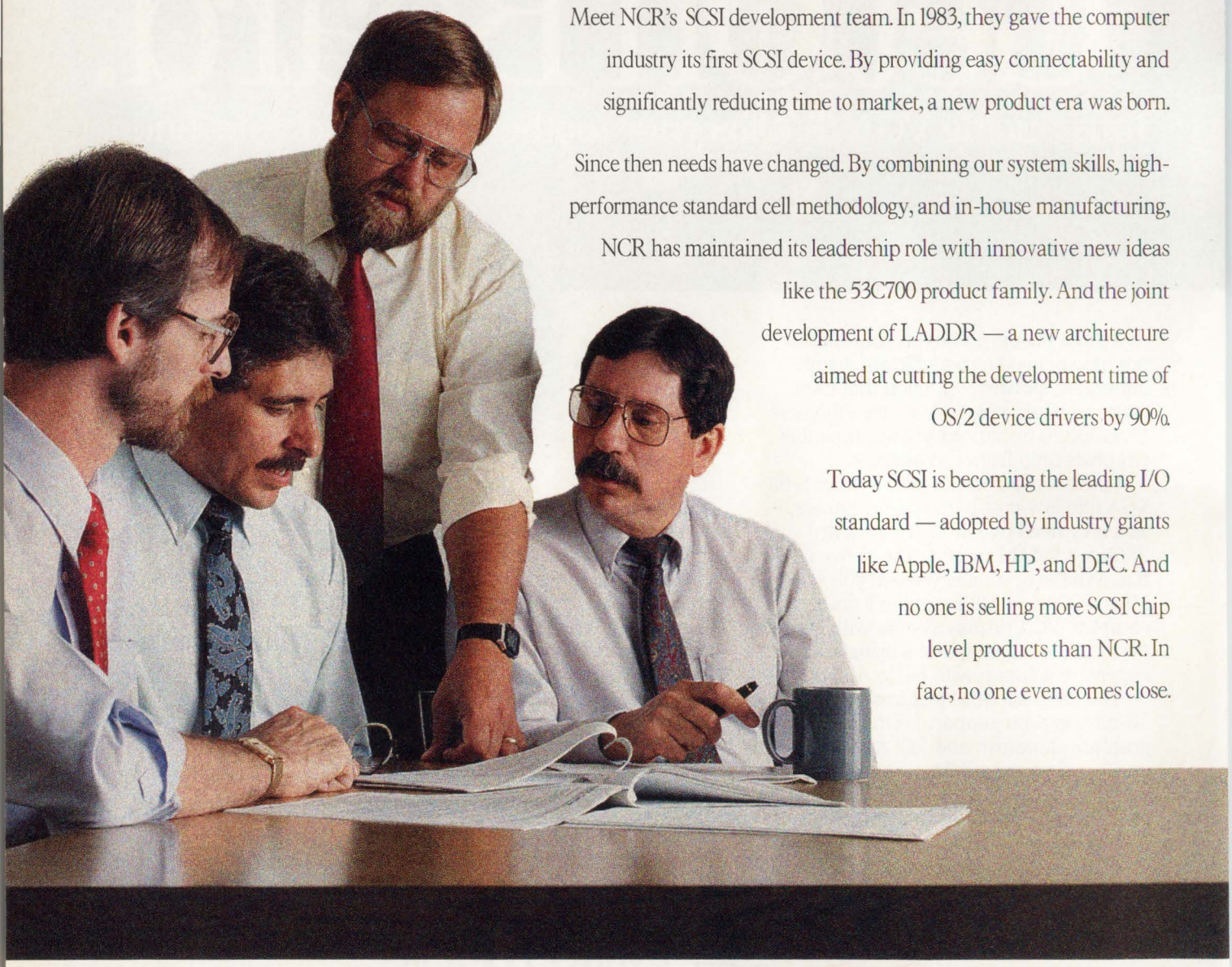

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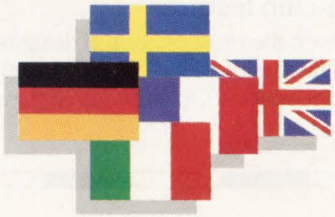

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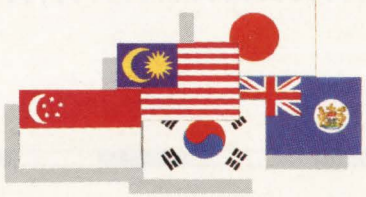

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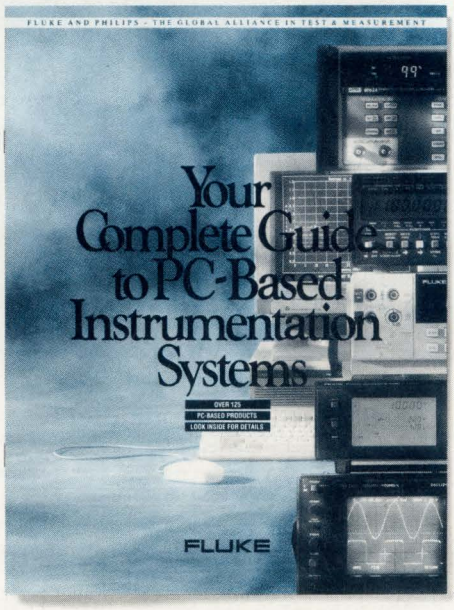

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MODULES CAN BE PIECED TOGETHER FOR DIFFERENT CONFIGURATIONS, UP TO 386SX

TINY MODULES FORM COMPLETE EMBEDDED PCS

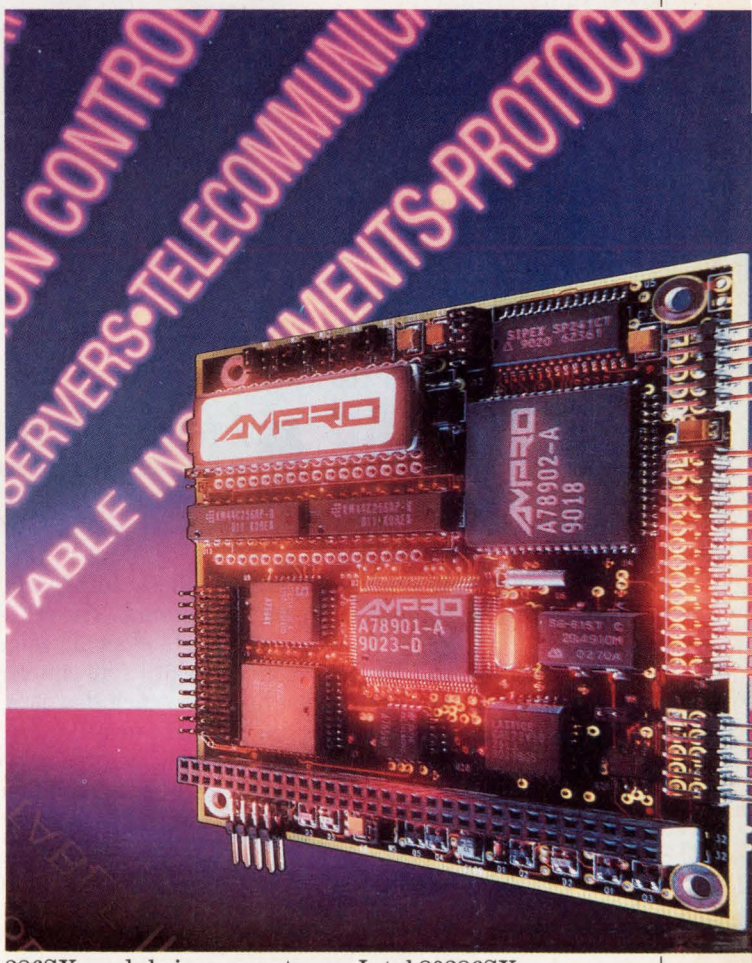
RICHARD NASS

The growing popularity of the PC as an embedded intelligent controller has spawned many single-board industrial-grade PCs. The applications for these PCs run the gamut of performance requirements, from simple data preprocessing and coordination to complex data handling and heavy-duty number-crunching. Such PCs are typically implemented on cards using the STDbus, AT-bus, and several proprietary formats. However, because industrial PCs are both power- (heat) and board-area limited, the boards are often housed in sealed enclosures with little or no ventilation. In addition, the space available to hold the boards may be restricted.

To meet the diverse requirements of most industrial applications, a trio of reduced-size computer boards from Ampro Computers, the CoreModule/XT, /286, and /386SX, deliver desktop computing power in palm-sized 3.6-by-3.8-in. modules that are only 0.6-in. thick *(Fig. 1)*. All of the boards include an expansion pin-and-socket connector arrangement that allows additional boards to be stacked on top of each other, somewhat resembling building blocks. Those additional boards might typically include I/O lines, communication ports, IEEE-488 interfaces, and so on.

The XT version, whose performance is about four times that of the original IBM PC, is IBM PC/XT-compatible and runs all compatible software. It contains a 10-MHz NEC V20 microprocessor, similar to the 8088 processor.

The 286 version, based on the 80286 microprocessor, runs at 16 MHz. The high-end



386SX module incorporates an Intel 80386SX processor that also runs at a minimum of 16 MHz. The XT-version can hold from 256 kbytes to 2 Mbytes of RAM. EMS (Extended Memory Specification) 4.0 is built into the board's chip set. The boards can also hold either 256-kbyte-by-4-bit or 1-Mbyte-by-4-bit DIP DRAMS.

There are two sockets on board for solid-state memory, which can be either EPROM,

flash EPROM, or SRAM. These sockets will support up to 512 kbytes of memory each. Additional sockets are available on an expansion board. With the solid-state memory, these devices can be accessed just as a floppy disk would.

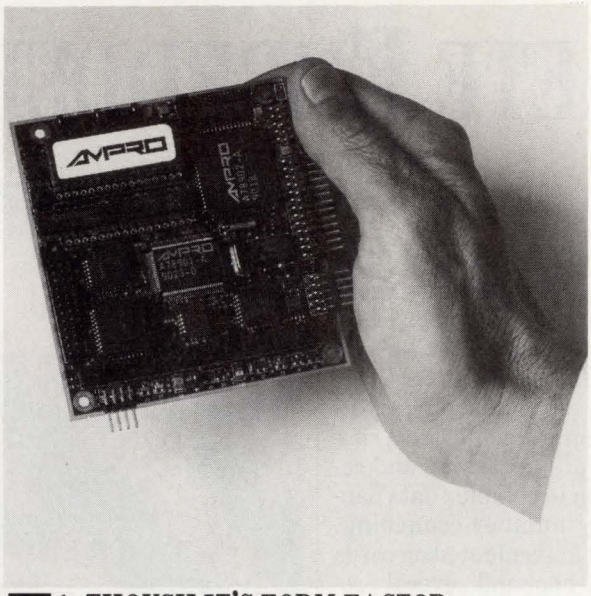
A small header is used to connect a coprocessor daughterboard for floating-point math. On-board are a parallel and serial port, as well as a real-time clock. The clock is run by the system power supply. A battery back-up helps keep the clock running after the system power shuts down.

Each module contains a bus header, rather than an edge connector, for connection to other devices. This is because Ampro didn't want to resort to using a backplane or card cage. Other modules can be added to the base module by simply stacking them directly on top of each another. A female header is located on the component side of the board, with a male header on the back. Two plastic or metal standoffs sit on the edges of the boards opposite the connector to form a sturdy construction, and to add resistance to shock and vibration. By stacking multiple modules, users can configure a complete system *(Fig. 2)*.

A later release will have all connections done with straight-out male headers. Users can then mount the board, component-side down, and plug it into another pc board, making a basic PC engine. A good example comes while building a piece of equipment containing lots of external logic, such as additional digital or parallel I/O or some other type of interface that would drive various pieces of equipment within an embedded system. Users could build a PC board containing all of the required application-specific logic. Then, with the female headers, the board could be plugged in as if it were a big chip. In this case, the board acts as a component, rather than a board-level product.

Modules can also be used with other Ampro peripheral boards. The XT board will have a companion product called the MiniModule/FSS. The FSS stands for floppy, serial, and SCSI because it contains a floppy-disk controller, a second serial port, and a SCSI interface.

In all, there are 12 module boards. The first few started as display controllers for CGA, EGA, and VGA systems. The VGA controller supports electroluminescent and liquid-crystal flat panels as well as CRTs. Also included is a CGA-compatible LCD controller.



1. THOUGH IT'S FORM FACTOR is quite small, the CoreModule boards contain all of the functionality of full-size PCs. The high-end board holds an 80386SX processor. Shown is the CoreModule/XT with its NEC V20 processor.

One controller works with the Private Eye, a miniature 1-in.^{2} CGA-compatible display from Reflection Technology, Waltham, Mass., that's used for portable applications. Other modules include a dual serial-parallel board for I/O expansion, an Arcnet network controller, a 2400-baud modem, and a recently announced IEEE-488 minimodule. Ampro will soon announce a send-only fax version of the 2400-baud modem. One last module is an IDE (Integrated Drive Electronics) interface. However, it's incompatible with the CoreModule/XT because it requires a 16-bit I/O bus.

Applications for the boards span a vast range and more continue to emerge. "It's almost easier to think of the few applications that can't use the modules than those that can," says Paul Rosenfeld, vice president of marketing for Ampro. Applications appear anywhere that space is at a premium. A standalone device on a network, such as a printer, is one particular application that stands out. A PC is needed to tie into the network, then the printer is connected to the PC. With the CoreModule, the PC could exist inside the printer, because the display, keyboard, and other components aren't required.

Another board application involves portable devices. A portable data-entry terminal is a good place for a space-saving module, one where users walk through a warehouse entering data. The data can be stored temporarily and later downloaded to another system. Other applications where space needs to be conserved include any type of portable test or medical equipment, as well as portable communications.

The boards have a high reliability factor built-in. Aside from the solid-state disk capability on the board, there aren't any sockets. All components are surface-mounted to the board. No backplane exists and there's nothing to plug into. As a result, there's no worry of anything falling out or getting loose from movement. All components are of the very-low-power CMOS variety. The actual power consumption is less than 1.25 W.

The boards operate over a 0-to-70°-C temperature range, so fans or cooling devices aren't required. Although mean-time-between-failure calculations haven't arrived, similar boards are running with MTBFs in the 100,000-to-200,000-hour range.

XT products typically can't store configuration information. This capability is critical for embedded configurations, so that if the system re-

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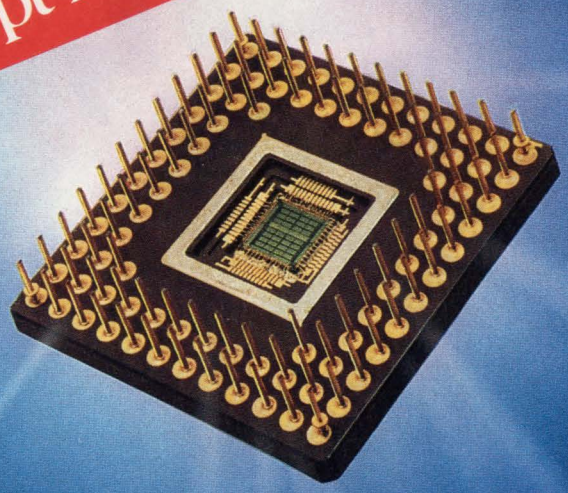

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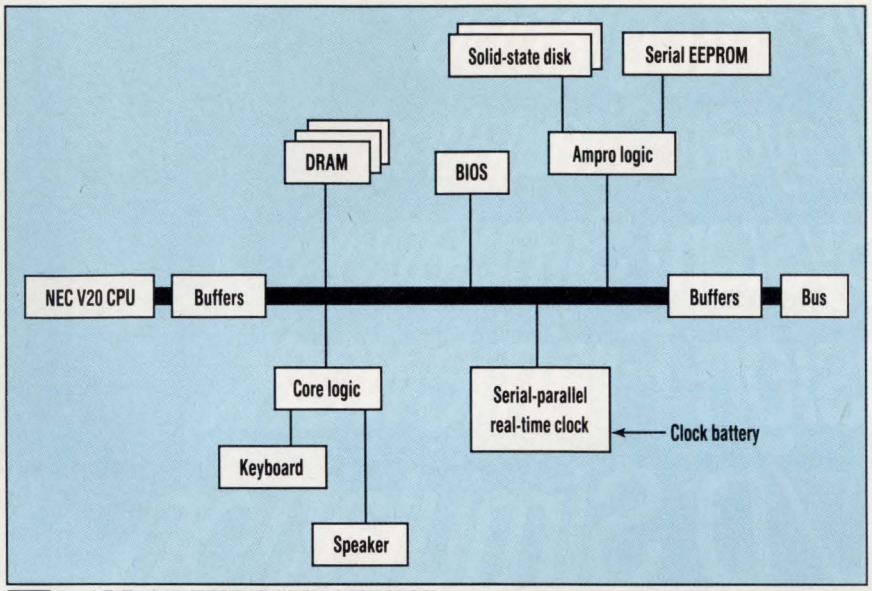

2. ALL OF THE COMPONENTS that make up the CoreModule are placed on a system bus. Here, the keyboard and speaker are external devices. Other modules can be added to form a complete embedded PC.

boots itself, it won't lose track of the system configuration that it's operating within. As a result, Ampro built a small serial EEPROM (1 kbits) into the device to store that configuration information. The EEPROM is accessible to users—they can go right to the configuration information and read it back whenever it's needed.

CUSTOMIZING THE BIOS

Extending the BIOS is an important consideration for OEMs. That's why Ampro put a standard PC/XT and PC/AT BIOS on-board with a number of Ampro extensions. One extension is for built-in SCSI support. During system initialization, the BIOS checks for the another extension called "OEM hooks," which are commonly referred to as either extensions or patches.

For these extensions, a unique 2-byte OEM extension ID indicates at when the particular extension should be executed in the ROM-BIOS power-up/reset sequence. The extensions can either be placed in an on-board byte-wide socket or on an expansion memory board.

Using the patches method, a table of 16 pointers is developed that starts at address F000 at the beginning of the ROM-BIOS EPROM. For each OEM hook, the ROM-BIOS executes code located at a particular memory address. This is the address that's patched into the ROM-BIOS EPROM at the location corresponding to the OEM hook. But this only occurs if the default value in the table has been altered. This feature allows the OEM code to be located directly within the system's ROM-BIOS EPROM.□

PRICE AND AVAILABILITY

The XT CoreModule is now in a beta version, with production scheduled for January. The 286 board will be in production around the middle of next year, and the 386SX module should be in production in the fourth quarter of 1991. The XT will sell for under $100 in volume quantities; prices on the other two products haven't been set. The CoreModule/XT will also be available in a development kit consisting of the XT module, the MiniModule/FSS, and the MiniModule/VGA. Cables, a manual, and DR DOS 5.0 are also included. The kit will sell for $995.

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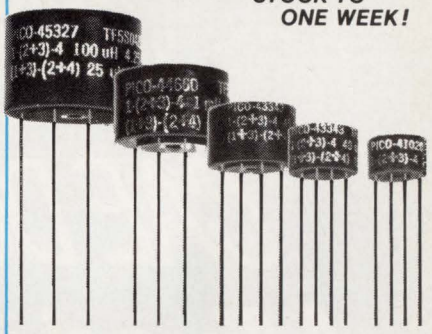

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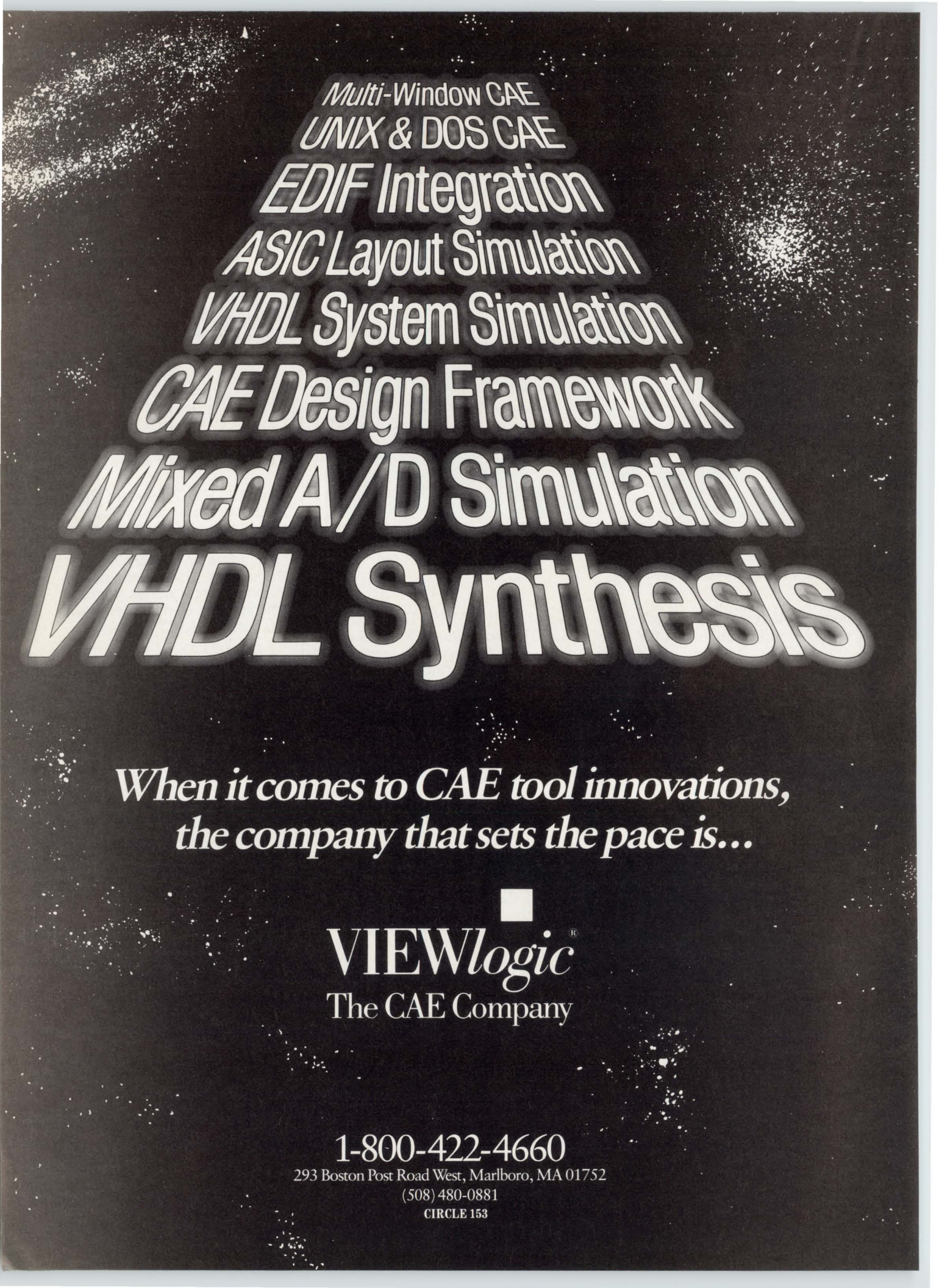
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PLD DESIGN TOOLS MATURE

BETTER FEATURES AND INTERFACES HELP DESIGN TOOLS KEEP PACE WITH COMPLEX PLDS AND FPGAS.

LISA MALINIAK

Cutthroat competition has manufacturers lining up in what's become a blistering race to get products to market faster. As a result, engineers concerned with a fast time-to-market often use programmable-logic devices (PLDs) and field-programmable gate arrays (FPGAs), devices that deliver the benefits of an ASIC without an ASIC's long turnaround time.

All of the advantages of PLDs and FPGAs are lost, however, without the proper design tools. Not only must these design tools be easy to use, reliable, and efficient, they must also mature along with the various devices.

Such tools split into two main groups: universal and device-specific *(see "Windows on PLD/FPGA design tools," p. 62)*. Universal tools enable users to design without a particular device in mind—designers can pick the device that best fits their needs. On the other hand, users of device-specific tools must know the chip that will be used before starting the design. Device-specific tools are usually offered by the semiconductor manufacturers. These manufacturers argue that, because they know the device better than third-party vendors, their tools will best utilize the device's resources.

Many users choose to employ universal tools to avoid locking into one device manufacturer too early in the process. In most cases, their design can be completed with universal tools before choosing any device at all. And they can examine trade-offs between devices. In addition, universal-tool users need only learn a design language once to design with many different devices *(see "Open tools optimize PLD design," p. 60)*. With device-specific tools, users must learn a new tool each time a different manufacturer's device is needed.

The key concern of universal PLD and FPGA tool users is device support *(Fig. 1)*. Engineers want their tools to support many devices, and they want that support as soon as the devices are introduced.

Many issues regarding users of PLD and FPGA design software, however, apply to both the device-specific and universal tools. For instance, engineers want easy-to-use user interfaces. In addition, they want the tools to integrate smoothly with the rest of their design environment. System-level simulation, which is becoming essential with today's complex systems, isn't possible unless all of the design tools mesh.

It's particularly important that PLD design tools be well-integrated with the rest of the board-design environment. For instance, functional simulation with the rest of the board is important to uncover errors. Moreover, timing problems uncovered during critical-path analysis may dictate using faster devices. And board layout and thermal analysis may require packaging or power changes.

OPTIMIZE AND PARTITION

As programmable logic is used for bigger designs, the tools must handle both optimization and device partitioning. Engineers are pushing PLD and FPGA technologies with large circuits that were implemented previously with ASICs. These large designs can't always fit into one device. Therefore, the design tools must efficiently partition the design into multiple devices.

Users are also looking for an easy and efficient way to input designs. Many newer design tools allow for such input methods as the VHSIC hardware description language (VHDL) and waveforms *(Fig. 2)*. Furthermore, users should be able to mix different entry methods within a single overall design description.

Programmable-logic design tools run on various hardware. In a survey of users of all types of design tools conducted by Data I/O, PCs were by far the most popular platform choice. And although the survey found that PC usage is tapering off, it'll continue to be

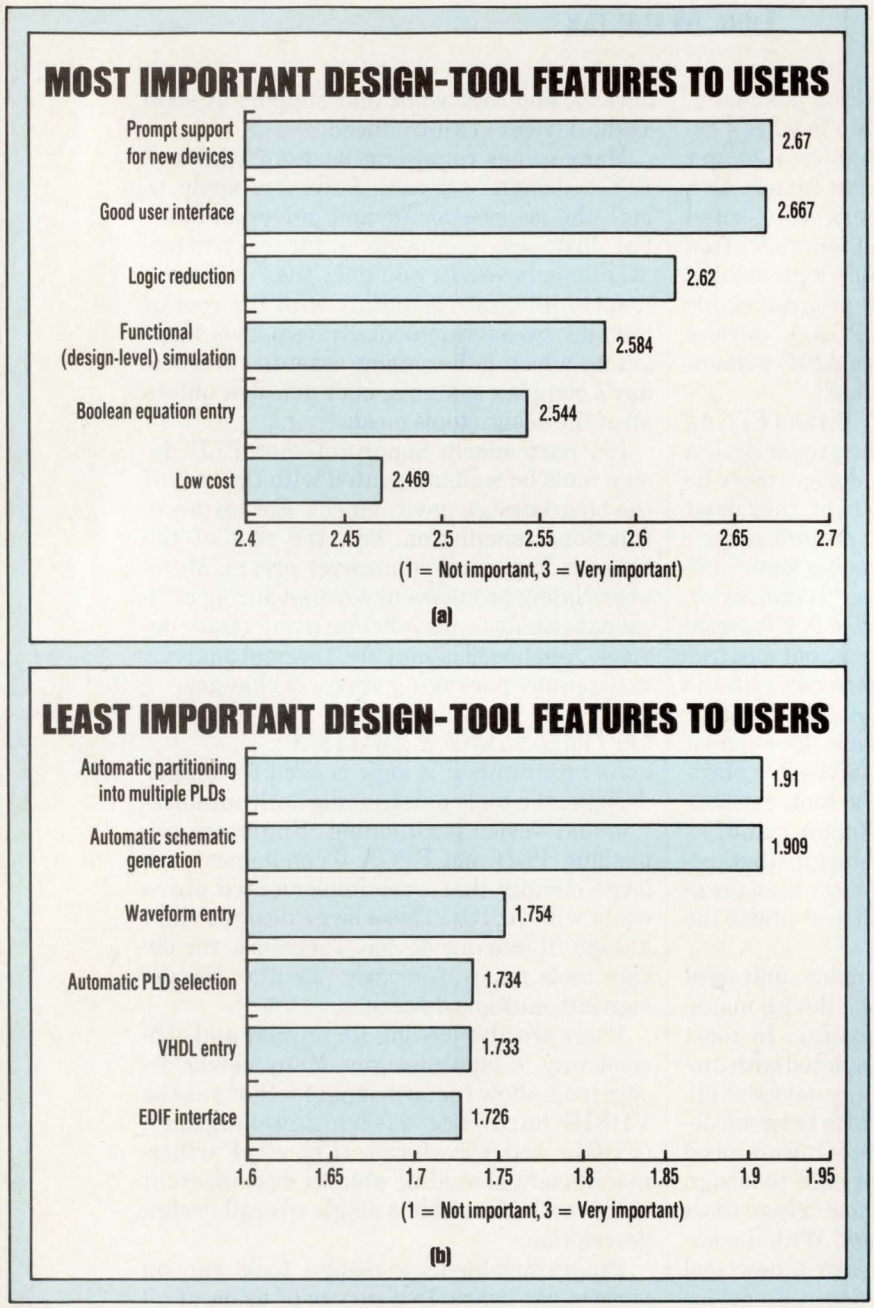
the hardware of choice for some time. The use of workstation-based tools, on the other hand, is growing rapidly.

The design-tool industry is doing its best to keep up with the increasing complexity of programmable-logic design. The past several months have seen major introductions for universal PLD and FPGA design tools. For instance, Logical Devices just introduced the latest revision of its PLD design system, CUPL 4.0. One unique CUPL feature is its ability to minimize logic on a pin-by-pin basis.

The new CUPL has many improvements, including expanded device support. The biggest change is the addition of automatic device selection. With this feature, users can enter a device-independent design. The software then produces a list of devices that are able to take the design. From this list, users can select a suitable device without knowing all of the details of its internal structure.

CUPL 4.0 also features more simulation capabilities than previous versions. Users can arbitrarily change the order in which simulation waveforms are displayed. In addition, the software can display ten waveforms at once. Users can also combine up to eight waveforms to form a bus with a hex output. Pricing for CUPL 4.0 hasn't been set.

Logical Devices' PLPartition tool takes a design that was created and compiled by CUPL and fits it into one or more PLDs. The tool reads the CUPL output, enables the engineer to select the desired PLDs, and offers a list of design solutions. Solutions can be sorted according to several criteria: cost, power consumption, propagation delay, or number of devices. The Logical Devices products run on PCs and DEC, HP/Apollo, and Sun workstations. PLPartition costs $995.



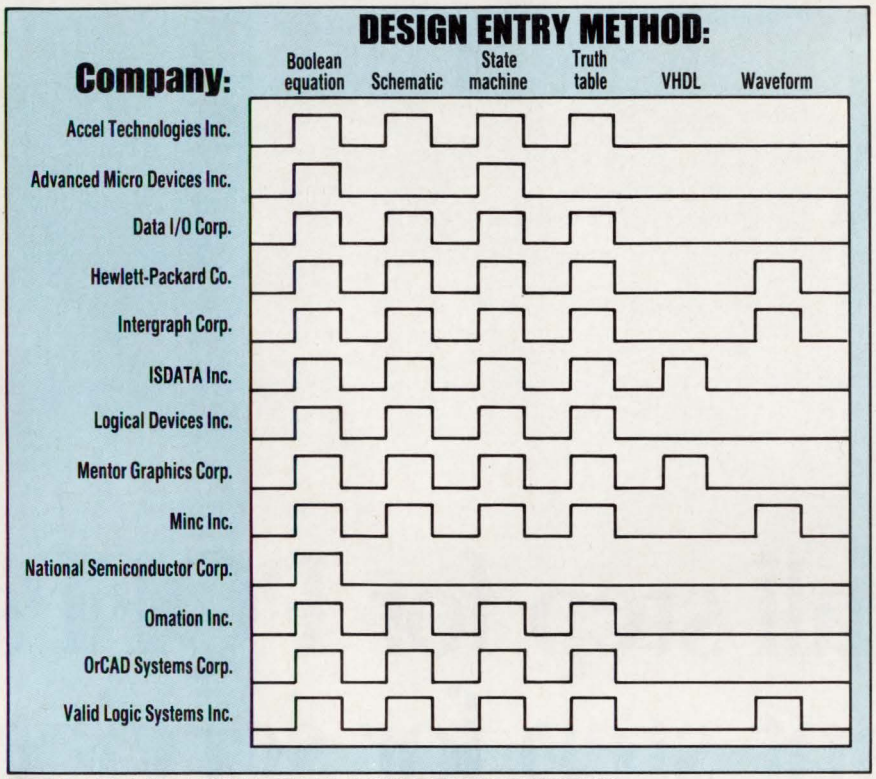
1. SURVEY RESULTS SHOW the features of programmable-logic design tools that are most important (a) and least important (b) to users. These numbers, obtained from a Data I/O Corp. survey, questioned not just users of Data I/O tools, but users of all types of design tools.

ABLE ABEL

Last month, Data I/O unveiled its newest version of Abel—Abel-4 (ELECTRONIC DESIGN, *Sept. 13, p. 107)*. The PLD and FPGA design software feature a windows-based interactive interface, Open-Abel fitters, and device- and system-level simulation. The new user interface provides context-sensitive help for whatever item the cursor is on. An auto-update feature tracks the design and processes only the necessary portions. All messages and error notifications are interactively reported.

Also included with Abel-4 is the enhanced version of the Abel hardware description language (HDL). Abel-HDL is device- and architecture-independent, which makes it possible for users to enter and verify designs without knowing the target device. Abel-4 costs $1995 for IBM PC/XT/AT, and PS/2 computers and com-

PROGRAMMABLE-LOGIC DESIGN TOOLS



2. PROGRAMMABLE-LOGIC DEVICES USERS can choose from a wide assortment of design-entry methods. VHDL and waveform input are a few of the newest methods.

patibles; $2695 for Sun workstations; and $4115 for VAX VMS computers.

Data I/O's Open-Abel concept gives users the advantage of a universal language without sacrificing device support. Specialized algorithms called fitters are written by the device manufacturer to fully optimize the architecture. Actually, the fitters written for Open-Abel will interface with any PLD or FPGA design tool that outputs in the Berkeley-PLA format.

During the Design Automation Conference late last June, Minc Inc. made two major announcements: design software for FPGAs and a strategic partnership with Texas Instruments. Minc added the PGADesigner family of software to its PLDesigner family of PLD design software.

PGADesigner builds on the device-independent design-description capability of the PLDesigner family. Users can target FPGA architectures as well as PLDs with one source description.

PGADesigner will combine several design description methods (truth table, equations, and so on) into one system description. In that way, users can choose the efficient method to specify each portion of the design. In addition, they can still use functional simulation for system-level logic verification. The system is then partitioned into the technology of choice: one FPGA, multiple PLDs, or directed combinations. PGADesigner, which runs on PCs and Sun workstations, costs between $2500 and $14,000 depending on the configuration.

LINKS TO GATE ARRAYS

An agreement between Minc and TI calls for Minc to write software that generates programmable-logic descriptions automatically for PLDesigner or PGADesigner tools directly from TI's TGC100 gate-array designs. The software, called ASICPrototyper, will run in the Mentor Graphics and Valid Logic Systems CAE environments. Under the

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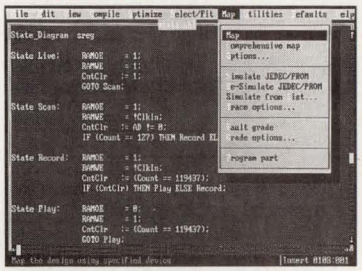

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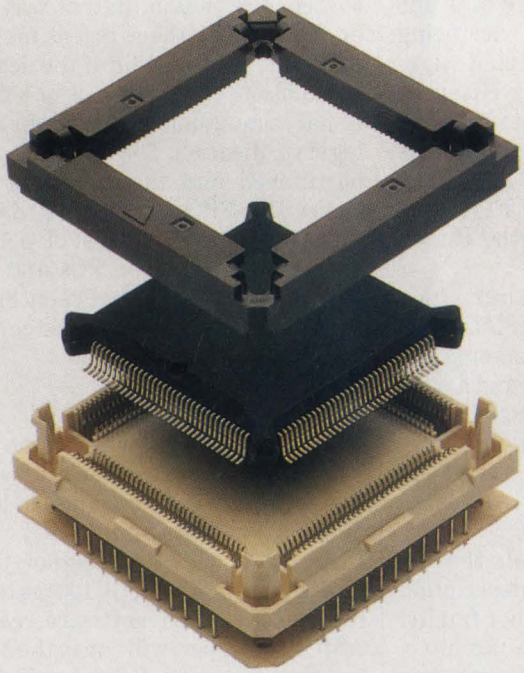

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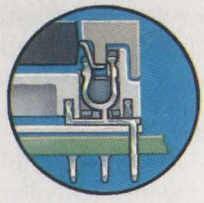

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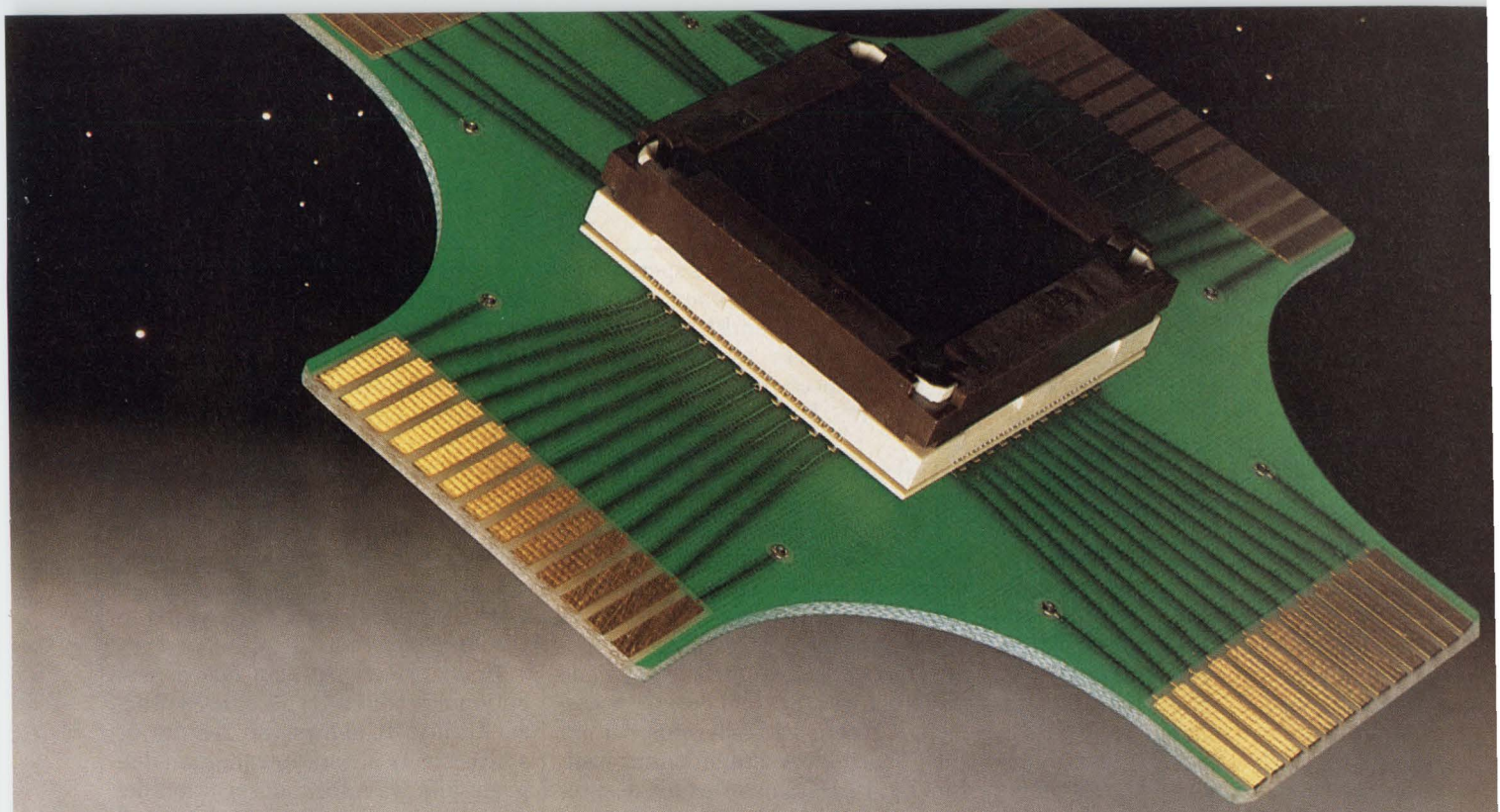

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For technical literature and more information, call the AMP Product Information Center at 1-800-522-6752 and ask about Micro-Pitch Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP **Interconnecting ideas**

CIRCLE 115

agreement, Minc will also write software, called ASICPath, which automates the process of migrating programmable-logic design from its tools into the TI ASIC design environment. Delivery of the ASICPrototyper will begin in the fourth quarter; ASICPath will ship in the first half of 1991. Pricing hasn't been set for either product.

Valid Logic entered into the programmable logic market last month with the SystemPLD and SystemPGA tools, which are based on technology from Minc (ELECTRONIC DESIGN, *Sept. 27, p. 179).* With these tools, users can mix PLD and FPGA logic throughout system-level schematics, perform system-level simulation before device selection, and combine or retarget PLDs and FPGAs automatically without design description changes.

A number of design-entry methods can be combined hierarchically in the same schematic. Design entry is both technology- and device-independent. The software simplifies device selection by letting users specify certain rules or constraints *(Fig. 3).* Pricing for SystemPLD and SystemPGA starts at $13,500 and $19,500, respectively. Both products run on DEC, IBM, and Sun workstations.

This month, Hewlett-Packard Co. is unveiling its newest PLD software version—HP PLD Design System (PLDDS) 4.0. The company feels its design software has three key benefits. With PLDDS, users can create and implement their designs independent of their knowledge of PLD architectures. System designers can include their PLD designs within their board-level simulations as well. Finally, PLDDS has flexible design-entry methods. Users can abstract their designs in the same way that they're conceptualized.

HP PLDDS 4.0 enhances the previous software as an integrated, system-level tool. With the new version, users can perform remote compilation from multiple editors. Any workstation with an editor can use the compiler on another workstation. Software cost is thus minimized by purchasing one compiler with many editors.

Moreover, new schematic-editor enhancements include "rubber band" movement of primitives with wires. Version 4.0 does a better job of informing users of design errors. The compiler supplies a window explaining compiling misses caused by design errors *(Fig. 4).* In addition, over 100 new devices were added to the library.

Hewlett-Packard also has a new optional product—the Logic Synthesis Utility. It shows the results of synthesis from state-transition-diagram and waveform-description design inputs as logic equations and schematics. Users can then transfer these to non-PLD technologies, such as gate arrays. The HP tools, which are designed to run on the company's workstations, cost between $5600 to $13,700.

Mentor Graphics Corp.'s PLDSynthesis tool will take on a new

OPEN TOOLS OPTIMIZE PLD DESIGN

Today's systems designers are rarely able to fully optimize advanced programmable-logic-device (PLD) architectures. In fact, they often complain that a particular device doesn't have enough product terms to properly fit a design. It may be the design tools that are at fault because they either don't synthesize a portion of the design efficiently or don't synthesize it at all. For example, the right synthesis software can exploit a device's T flip-flop emulation capabilities to capture a seemingly large design into one device. Other tools may choose multiple devices for the same design, giving a non-optimal solution.

Frustration continues to grow among the system designer ranks. The reason is simple: Proliferating PLD architectures is at odds with the vast assortment of design tools flowing from proprietary tool vendors and semiconductor manufacturers.

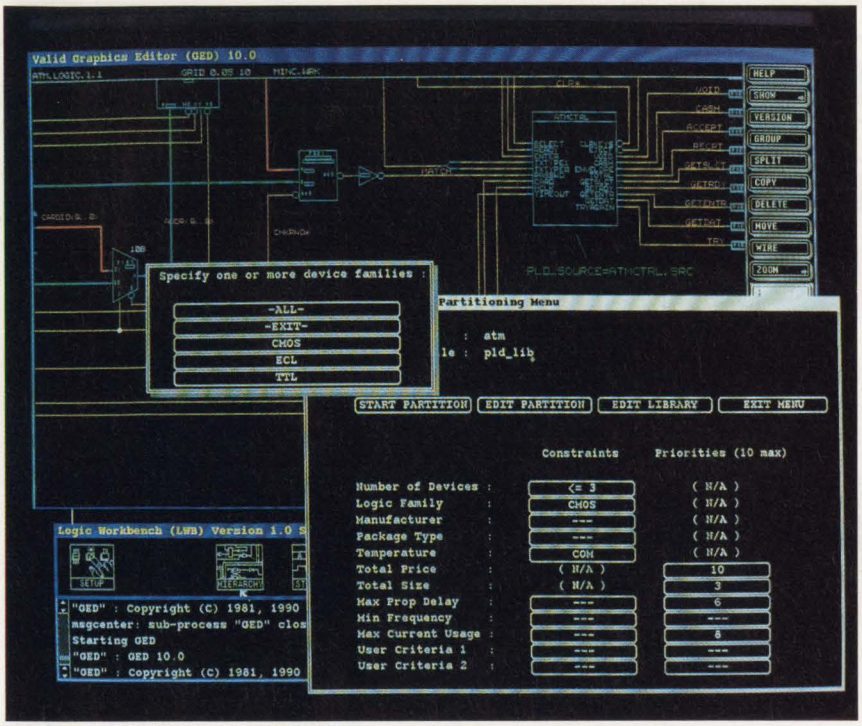
Several factors contribute to the aggravation. First, consider that each chip maker's PLD architecture requires unique software and synthesis algorithms. Then systems designers populate boards with greater numbers of complex PLDs. Sun Microsystems Inc., Mountain View, Calif., for example, puts up to 150 PLDs on some boards. It isn't productive for these designers to use proprietary tools for every PLD architecture they design with. Designers need one tool that does everything efficiently.

One solution is to develop intelligent algorithms for each architecture, and then integrate them with a common language and user interface so that everything is transparent to system designers. This wasn't such a problem years ago when the industry dealt with simple, two-level sum-of-products devices. Those were easily categorized as PROMs, PALs, and FPLAs. Back then, a tool could simply be created by using one or two synthesis algorithms.

But to comply with today's demand for higher performance, innovative chip makers offer more access to key device technologies, spawning an increasing number of new and different architectures. Today, systems designers must contend with a maze of architectural features, such as multiple flip-flop types, buried nodes, XOR gates, and folded arrays. Completely new generations of devices are also entering the market. The most notable is the FPGA, which presents itself in at least two programming configurations—RAM- and fuse-based.

In essence, systems engineers experience an embarrassment of PLD riches, but haven't been able to capitalize on them. PLDs usually have more flexibility than designers can handle. And PLDs are

PROGRAMMABLE-LOGIC DESIGN TOOLS



3. DEVICE SELECTION and automatic partitioning across devices is driven by user-specified constraints with Valid Logic System's SystemPLD and SystemPGA. These constraints include manufacturer, PLD type, speed, cost, power, and logic family.

role when it's delivered in the 8.0 environment early next year. The PLDSynthesis product is also based on technology from Minc. Within 8.0, PLDSynthesis will be closely integrated with Mentor's Design Consultant (a VHDL design-synthesis tool) and ASIC Consultant products. The integration between these tools will enable users to move easily between programmable-logic devices and ASICs. Mentor feels that VHDL will be a big factor in PLD design, especially as the designs expand in complexity.

The Mentor environment meshes the PLDSynthesis tool tightly with its board-level tools. This is because PLD designs are driven by board requirements rather than by individual design functions. The tool's partitioning capabilities can be fully utilized if the board's PLD functions are combined before synthesis. PLD implementations often require fewer and less expensive devices than what designers would have decided on.

FPGA design will be supported in just the beginning: FPGAs, still in their infancy, continue increasing in gate densities.

One way to exploit these programmable IC (PIC) technologies is through such high-level behavioral design languages as Abel. With high levels of abstraction, designers can quickly and effectively deal with complex device functions.

These high levels of abstraction, however, must not come at the expense of optimization and partitioning. Newer, more complex architectures require those advanced algorithms that efficiently divide logic into the right-size blocks and then do the routing among those blocks.

Hardware description languages and logic synthesis, plus today's growing trend toward open tools, alleviate design barriers and OEM concerns over depending on multiple sources for device-tool support. The open-tools concept, in particular, contributes to design optimization and assures systems houses of good device support. The open-tools approach bodes well for the chip maker and the universal tool vendors who open up their proprietary design tools.

Specifically, the concept allows an ASIC or PLD vendor to take advantage of a well-established design language. It also supplies system designers with device-specific synthesis algorithms, place-and-route routines, and optimization procedures through one HDL. Designers have one language that supports multiple devices efficiently.

One example is extending the popular Berkeley PLA file format so that PLD suppliers can tack on their own device-specific software. This format describes logic functions to be mapped into a PLD, and provides a compact way to transfer logic descriptions between various tools. As a superset of the Berkeley PLA format, it also gives chip makers the green light to many circuit-optimization tools, such as Espresso or MIS.

Open software is attractive to many ASIC and PLD vendors because it gives them direct control. They can write their own device- and architecture-specific algorithms, known as "fitters," can control delivery schedules, engineering due dates, and they still exploit standard tools.

For designers, open tools mean a major step toward tool integration, virtually comprehensive device support, and a considerably tighter PLD design cycle. There are also more choices, greater design flexibilities, and the new power to exercise a design in various device options.

Contributed by Mike McClure, a product manager at Data I/O Corp., Redmond, Wash.

PROGRAMMABLE-LOGIC DESIGN TOOLS

WINDOWS ON PLD/FPGA DESIGN TOOLS

DEVICE-SPECIFIC TOOLS

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AT&T
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Plessey Semiconductors
Scotts Valley, Calif.
(408) 439-6074
CIRCLE 302

Plus Logic Inc.
San Jose, Calif.
(408) 293-7587
CIRCLE 303

Xilinx Inc.
San Jose, Calif.
(408) 559-7778
CIRCLE 304

PLD

Altera Corp.
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CIRCLE 305

Cypress Semiconductor Corp.
San Jose, Calif.
(408) 943-2600
CIRCLE 306

Exel Microelectronics Inc.
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Gould AMI Semiconductors
Pocatello, Ida.
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Integrated CMOS Technology Inc.
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Intel Corp.
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Minc Inc.
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Phase Three Logic Inc.
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Mentor Graphics Corp.
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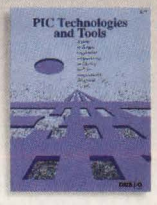

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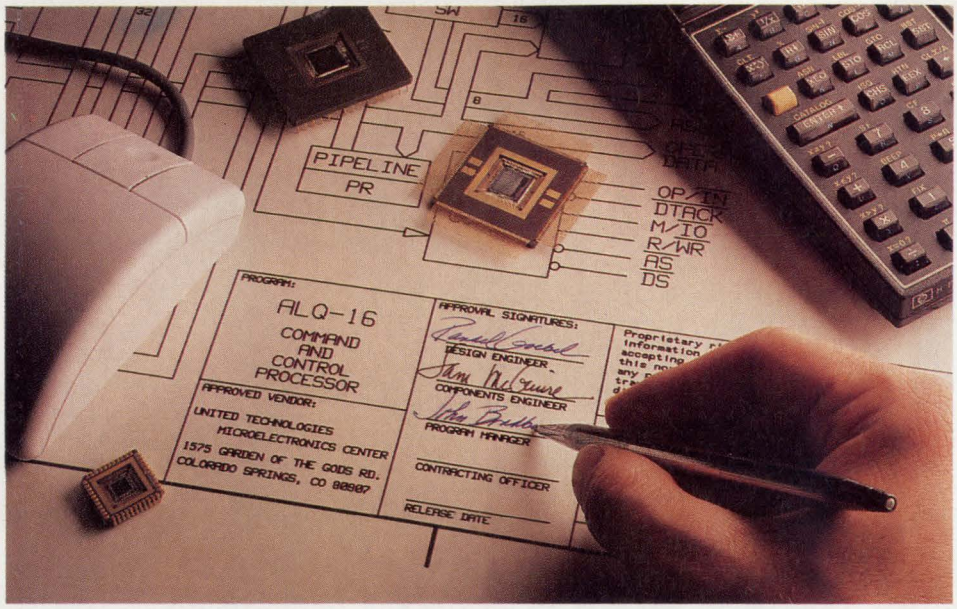

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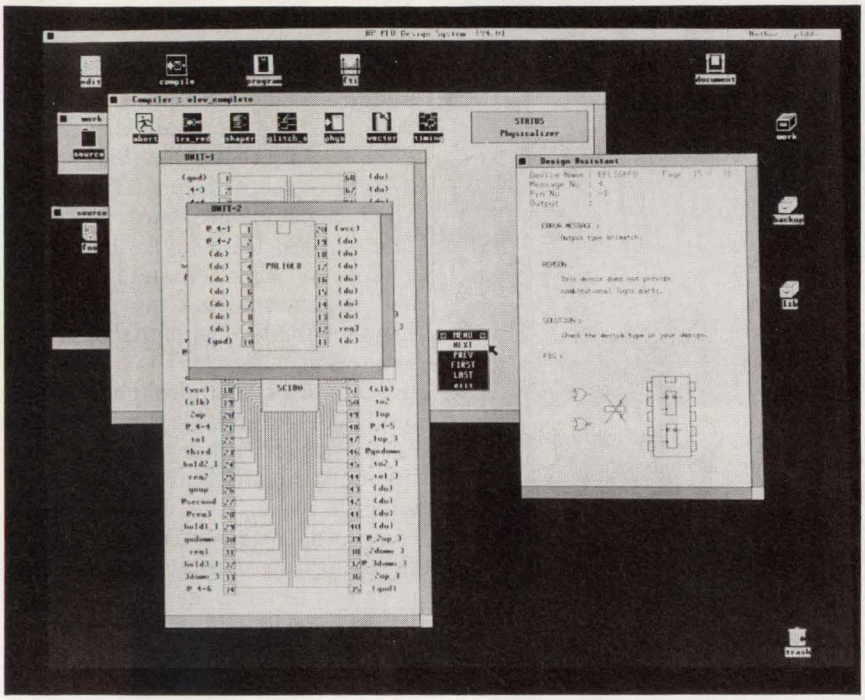


4. THE NEWEST version of Hewlett-Packard's PLD Design System lets users know when a design error occurs. A window (left side of screen) explains compiling misses caused by design errors.

Mentor's 8.0 environment with design kits supplied by the FPGA vendors. Users will enter the design with Mentor's front-end tool. The back-end tool, or the design kit, will then optimize and implement the design into a device.

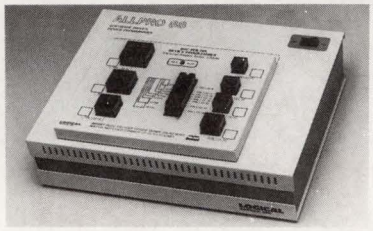
Interactive partitioning and a VHDL compiler are the newest additions to ISDATA Inc.'s LOG/iC development software. LOG/iC Perfect is a synthesis tool that interactively partitions large designs among several PLDs. The partitioner is controlled through menus, and involves users in the decision-making process. Different partitioning sessions can be stored in a stack and called in for review or implementation at any time. The final result is a number of Jedec or HEX files to program the selected components.

The new software also sports the benefits of automatic test-vector production. Input syntax underwent improvements that incorporate recent technological developments. For example, JK or RS flip-flops can now be defined for PLDs. LOG/iC Perfect runs on PCs and workstations, and costs $3987 (for the PC version) and $6777 (for the workstation version).

ISDATA also just released Hint, a software package that links the company's design system to the VHDL world. Hint works as a preprocessor to define state machines and combinatorial circuits in VHDL, and automates state reduction and state assignment for finite-state-machine designs. Hint, which runs on PCs, costs $2380.

Tango-PLD, a universal tool from Accel Technologies Inc., designs and simulates PLDs. With the software, users can enter and simulate designs before device selection. A combination of input methods are possible with the Tango Design Language. Tango-PLD runs on IBM PC/XT/

Program It All!



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CIRCLE 113

PROGRAMMABLE-LOGIC DESIGN TOOLS

AT, and PS/2 computers and compatibles. It costs $495.

PLD users can purchase another design system for $495 from Omation Inc. The company's Schema-PLD is a logic compiler that's structured to accept output from Omation's schematic-capture software. The tool's high-level language makes it possible for users to bypass logic equations and move directly from schematic design to PLD implementation.

Schema-PLD approaches multiple PLD systems by compiling the entire design rather than considering individual PLD architectural elements. When the compilation is complete, the resources needed by the design are displayed to the engineer. Engineers can then select PLDs, considering such factors as speed, availability, and cost. Schema-PLD runs on IBM PC/XT/AT and 80386-based computers and compatibles.

OrCAD Systems Corp.'s OrCAD/PLD also costs $495. The OrCAD/PLD library contains over 2400 parts. The design software allows for numerous input methods, including numerical maps, schematics, and indexed equations. In addition, it's integrated with OrCAD's other design tools. OrCAD/PLD runs on IBM PC/XT/AT, and PS/2 computers and compatibles.

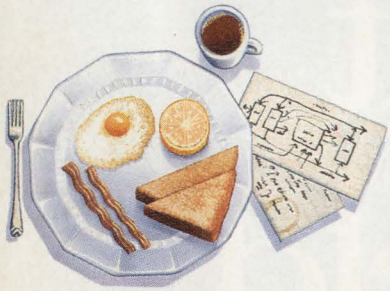
Intergraph Corp.'s PLD design tool—PLDesigner Plus—is based on Minc's PLDesigner. The PLDesigner Plus software, coupled with the Intergraph user interface, runs on Intergraph workstations. Entry methods can be mixed within one design, and functional simulation verifies that a design works properly before device implementation.

Automatic design partitioning and device selection separates the design phase from the design-implementation phase. Device selection from a library of over 3000 parts is based on user-specified criteria.□

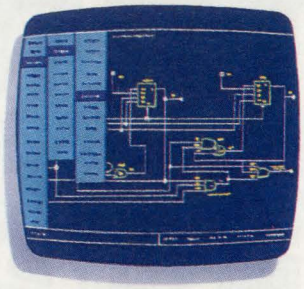
How Valuable?	Circle
Highly	544
Moderately	545
Slightly	546

Food For Thought About Field Programmable Gate Arrays.

Be Brilliant At In Productio

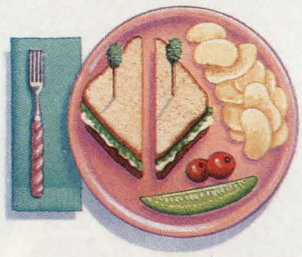


7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

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And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

Actel FPGA Product Family		1010A	1020A
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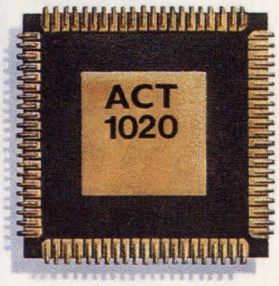
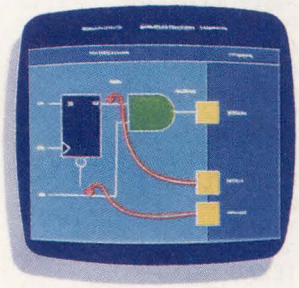
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

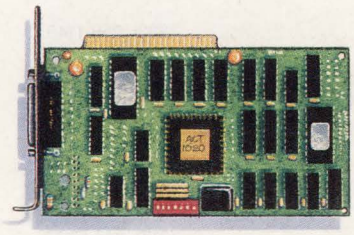
Breakfast And n By Dinner.



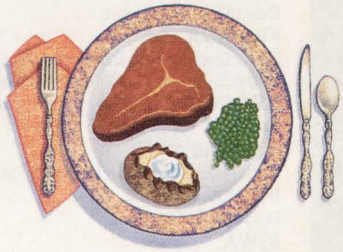
1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.



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CIRCLE 120

RISC CPU MODULE PACKS ALL LOGIC

A 3.5-BY-3.5-IN. RISC-CPU MODULE GIVES DESIGNERS A COMPLETE MIPS PROCESSOR WITH CACHE AND FLOATING POINT.

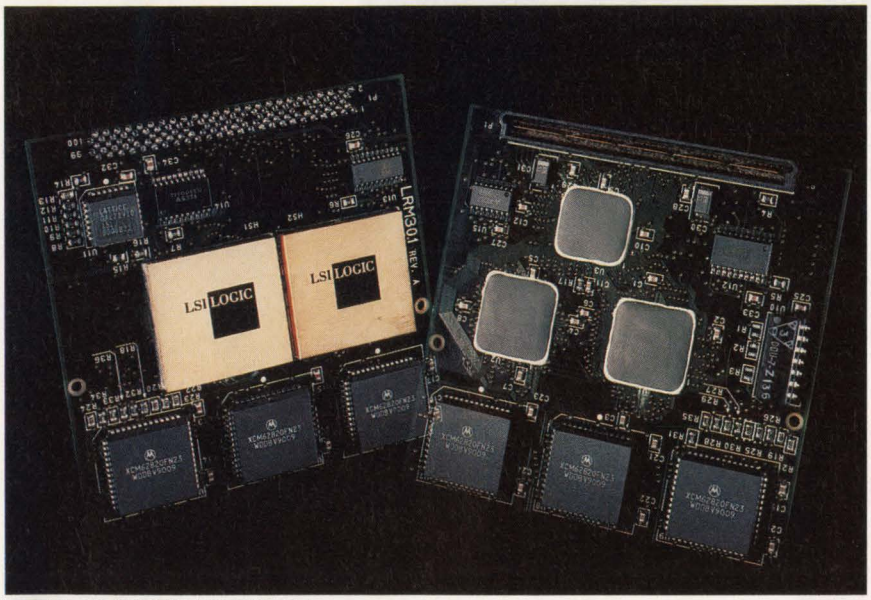
DAVE BURSKY

With higher integration levels, the performance and functionality of reduced-instruction-set computers has elevated to new heights. However, off-chip support, such as cache memory, read and write buffers, and clock-generation logic, often handcuffs system performance due to wiring delays of mismatched components. One answer to these limitations comes in the form of a small circuit board, the RPM3010 Mips Ngine from LSI Logic, which integrates all of the critical functions to form a complete CPU subsystem. The board takes the headache out of designing the timing-critical portion of a system based on the R3000 RISC processor from Mips Computer Systems Inc., Sunnyvale, Calif.

Even though LSI sells the R3000 chips as standalone components, the tight timing margins of the chips requires that system designers spend a fair amount of time developing and debugging a prototype CPU subsystem. The Ngine module cuts that time to almost zero. On one 3.5-by-3.5-in. module, designers at LSI have combined the following: the LR3000 32-bit integer processor; the LR3010 floating-point unit; the LR3220, a six-word-deep read-write buffer with parity checking and generation logic, plus address- and data-bus buffers; dual 32-kbyte instruction and data caches; five registered interrupt inputs; and clock-generation and reset circuits. A 100-pin connector provides the I/O interface and ample power-supply and ground lines *(see the figure)*.

Modules will be manufactured with maximum operating frequencies of 20 or 25 MHz. At top speed, they'll have worst-case power consumption of about 22 W. The onboard circuits eliminate the need for any complex external timing. And they provide programmable block refilling for data or instruction caches, instruction streaming, and system configurability. Such a CPU module can be used during system prototyping to shorten the hardware design phase considerably. Or it could be employed as a complete embedded central processor subsystem, even in low-volume production stages of a project.

To squeeze all of the logic and cache memory onto such a small card, designers employed a hybrid and dual-sided surface-mount combination. The CPU and floating-point



A COMBINATION OF chip-on-board and standard surface-mount technology make this 3.5-by-3.5-in. RISC CPU module possible. Crammed into just over 12 square in. are the 32-bit LR3000 CPU, the 3010 floating-point unit, the 3220 read-write buffer, 64 kbytes of cache, and clock-generation and bus-interface circuits.

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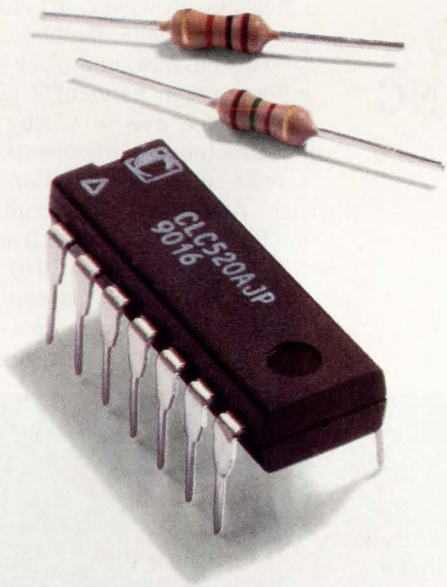

CIRCLE 155

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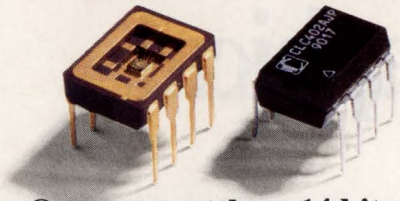

Op amps settle to 14 bits in 32ns max.

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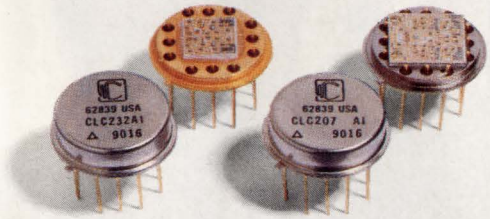
CIRCLE 156



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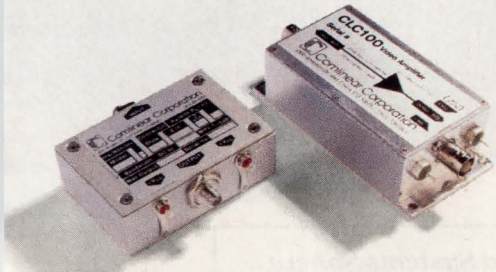
CIRCLE 157



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CIRCLE 158

RISC CPU MODULE

unit are mounted as unpackaged chips directly onto the combination heatsink and pc board. They're then covered with an encapsulant for environmental protection. The read-write buffer chip is also mounted directly to the pc board, but its power is considerably lower and need not be mounted on a heatsink. Such a direct-attach approach eliminates the expensive pin-grid packages, reduces wire lengths and inductances from chip to chip, and improves the heat removal. Consequently, chip reliability is enhanced.

Pulling Out The Heat

The heat-sink for the CPU and floating-point unit consists of a high-thermal-conduction copper-tungsten slug, with its coefficient of expansion matched to that of silicon. The slug is mounted to the top-side of the module. An opening is cut in the module pc board so that the chip can be mounted onto the slug and then wire-bonded to the pc board.

Not only does the scheme have all of the benefits mentioned in the previous paragraph, but it also improves manufacturing yield. In some designs, tight timing parameters for various CPU control signals, delays caused by packages, and long pc-board wire traces can often cause devices in a CPU system with marginal timing specifications to not work together. the inability to work together comes from the slight timing mismatches caused by longer-than-desired wiring delays. By reducing the delays, the chance of a timing mismatch is reduced and the manufacturing yield of the subsystem goes up substantially.

The rest of the active components are housed in small-outline or plastic leaded chip carriers and are mounted with standard surface-mount manufacturing techniques. Passive components, such as the bypass chip capacitors and pull-up chip resistors, are surface-mounted directly to the pc board. To minimize chip count, each cache was implemented with just three 8-kword-by-20-bit static RAMs to form dual 8-kword-by-60-bit caches.

The LR3000 integer unit manufactured by LSI is a direct alternate source of the R3000 created by Mips. It consists of two tightly coupled processors—the 32-bit RISC integer processor and a system-control processor that handles the memory management thanks to an on-chip 64-entry translation-look-aside buffer. The floating-point unit is tightly coupled to the CPU and conforms fully to the IEEE floating-point standard for single- and double-precision calculations.

A custom-created write-buffer chip, the LR3220, offers six-level-deep write buffering to prevent pipeline stalls during a write operation. A special clock-generator chip creates the four clock signals required by the LR3000 CPU from a single-phase clock input to the module. With reset logic on the module, various user-selectable modes can be set during the initialization period. The modes are set by controlling the state of the interrupt inputs during initialization.

Of the 100 pins available on the user-interface connector, 32 are assigned for the data bus, 30 for the address bus (plus several bus-control lines), 5 for interrupt inputs, and 4 for byte read and write masks. Three are assigned to indicate branch conditions and others are for the system clocks. Additional lines handle module control and error signaling, and seven lines are reserved for future use. Power and ground pins are actually separate from the two rows of signal pins. The 100-pin Amp μStrip connector has five metal plates positioned between the two rows of 50 pins. The plates form low-resistance power and ground connections. □

Price And Availabilty

The LRM3310 Mips Ngine is available in sample quantities from stock. In lots of 5000, the card sells for less than $1000.

LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035; Pamela Aratani, (408) 954-4655. CIRCLE 511

How Valuable?	Circle
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CIRCLE 2

AVOID DESIGN PITFALLS WHEN WORKING WITH PLDS

PROGRAMMABLE LOGIC DEVICES GIVE A BIG BOOST TO SYSTEM INTEGRATION, BUT CERTAIN DESIGN PRACTICES MUST BE FOLLOWED.

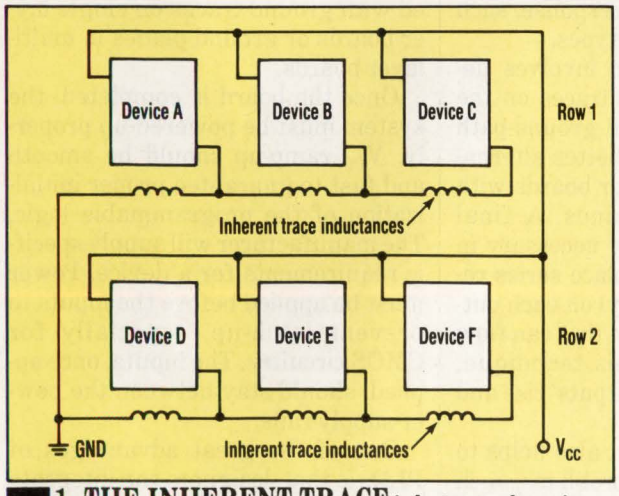
CHUCK TRALKA
Altera Corp., 2610 Orchard Pkwy., San Jose, CA 95134-2020; (408) 984-2800.

To integrate programmable logic devices into designs successfully, engineers must approach PLDs as both components in a board-level system and as discrete devices. In addition to the same board-level design concerns they face with discrete logic, designers must contend with timing and architectural considerations specific to PLDs. Because large logic blocks are integrated into one PLD, problems that initially appear to be device related often result from improper logic design. Consequently, care must be exercised in designing the PLD logic, the board logic, and the board layout.

At the board level, PLDs behave much like other digital logic ICs. Nonetheless, as programmable logic increases in speed and density, designers must pay more attention to proper board design and layout to ensure that the PLD will function correctly in the system. Good layout practices take into account loading, decoupling, and crosstalk.

The designer's first concern should be that the device pins are connected properly to the rest of the circuit on the board. PLDs usually have a set of dedicated-input pins and a set of I/O pins. The I/O pins can be configured as inputs or outputs, and may provide feedback for internal ("buried") logic functions. It's not uncommon for some pins to be left unused.

Typically, unused dedicated inputs should be tied to ground. Otherwise, they might float to an arbitrary voltage level where they can toggle between a logic one and a logic zero, inducing noise and consuming unnecessary current. In some cases, the PLD manufacturer recommends that all unused I/O pins also be tied to ground for the same reasons. In other instances, unused I/O pins may actually be used internally for feedback, or the design software may cause the pins to be tied to some internal logic level. If so, these pins must be left floating for proper device operation. Designers should always follow the manufacturer's recommendations.



1. THE INHERENT TRACE inductances shown in these two separate ground paths can cause ground-bounce problems when several outputs on a device switch simultaneously. Incorrect logic levels may result.

The next consideration is the resistive and capacitive loads driven by the PLD outputs. Resistive loads limit the output's fan-out. For example, with an output pin at 0 V (a worst-case value) a 1-kΩ pull-up resistor tied to a V_{CC} of 5 V will draw 5 mA [(5 – 0)/1000]. Consequently, a pin that can sink 8 mA can control only one such load and remain within the specified maximum current limit.

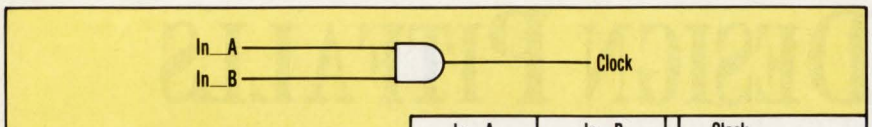
Unlike resistive loads, purely capacitive loads don't affect fan-out, but instead limit the rise and fall times of the PLD output signals. This is because:

$$I = dQ/dT \text{ and } Q = CV$$

where I is the output drive current, Q is the charge, T is time, C is the load capacitance, and V is the voltage change of the output. As a result,

$$dT = d(CV)/I$$

WORKING WITH PLDS



	In_A	In_B	Clock
Original state	0	1	0
Transition state	1	1	1 (Glitch)
Desired next state	1	0	0

2. IF A CLOCK SIGNAL IS GATED, even with a single AND gate, a glitch can result if the inputs don't change at the exact same time. In this case, Input A changed slightly before Input B. A momentary "one-one" state ensued, causing a glitch.

Thus, rise and fall times increase with greater load capacitance and decrease with greater output current drive capability.

The fast switching times of today's PLDs create the potential for another current-related problem—ground bounce. Ground bounce can occur when multiple outputs on a fast device switch at the same time, causing a large transient current to flow through the device's ground path. The rapidly changing current combines with the inherent trace inductance to temporarily raise the ground voltage [$V = L(dI/dT)$] for other devices that share the same ground line. Because their reference voltage has risen, the output voltage levels from these devices may also rise. In the worst case, a logic-low voltage can rise enough to be seen by devices that don't share that portion of the ground line as a logic high.

An example is a typical printed-circuit board with three digital devices (A through C) tied to one ground line and three more devices (D through F) tied to a second ground line *(Fig. 1)*. If several outputs on device C switch at the same time, the resulting current transient can also raise the ground voltage-reference level for devices A and B. If the output of one of these components feeds a device in the second row (D, E, or F), a low output can be interpreted incorrectly as a high signal. The illegal high level can then propagate through the system, causing incorrectly clocked or cleared registered functions and creating glitching in combinatorial logic.

Some PLDs contain output drivers specially designed to reduce this problem. Board designers, however, can also take steps to reduce ground bounce. The most obvious precaution is to decouple the device's power and ground pins using the capacitor values recommended by the device manufacturer. Decoupling capacitors supply a reservoir of charge that buffers the board power and ground lines from the large transient currents that digital ICs can draw. Each pair of V_{CC} and ground pins should be decoupled with a separate capacitor placed as close to the device leads as possible.

The board itself should be decoupled with two capacitors in parallel, located as close as possible to the point where power and ground arrive at the board. One should be a large capacitor (typically around 33 μF) that dampens large, low-frequency current fluctuations. The other should be a small capacitor (usually about 0.1 μF) that does the same for high-frequency current fluctuations. Use capacitors that have good frequency response, such as monolithic ceramic types.

Another precaution involves designing large ground traces on the board to minimize the ground-path impedance. An even better alternative is using multilayer boards with complete ground planes. A final measure, usually only necessary in extreme cases, is to place series resistors (100 Ω typically) on each output to limit the current that can flow through the pin. This technique, however, slows the outputs' rise and fall times.

Proper board layout also helps to avoid other common problems, such as signal reflection and crosstalk. To minimize reflection, trace lengths should be short compared to the rise and fall times of the signals. If the signal's propagation time down the length of the trace is more than half of the rise or fall time, designers should treat the trace as a transmission line.

Transmission lines have a characteristic impedance, which is determined by inherent resistances, inductances, and capacitances. To eliminate reflection, this impedance must match the load impedance. Matching is usually done with a pair of resistors at the load device. One resistor is tied from the signal to V_{CC} and the other from the signal to ground. Many texts explain the derivation of the resistor values.

Another problem related to traces on the boards is crosstalk. Crosstalk is caused by inductive and capacitive coupling between parallel traces. Inductive coupling results when current flowing in one trace generates a magnetic field that induces a current in another trace. Capacitive coupling occurs when two parallel traces behave like the plates in a capacitor and attempt to maintain a constant voltage between themselves.

To minimize crosstalk, designers should avoid running long traces parallel to one another. If they must be parallel, the traces should be as far apart as possible and should alternate with ground traces. Particularly noisy lines (such as system clocks) should be as distant as possible from other signals and surrounded with ground traces on single-layer boards or ground planes in multilayer boards.

Once the board is completed, the system must be powered-up properly. V_{CC} ramp-up should be smooth and fast to guarantee proper initialization of the programmable logic. The manufacturer will supply specific requirements for a device. Power must be applied before the inputs to prevent latch-up, especially for CMOS circuitry. The inputs, once applied, should stay between the power-supply rails.

One of the great advantages of PLDs is that designers can integrate entire subsystems into one device, decreasing component counts and increasing system reliability. Howev-

er, potential problems can also occur in the PLD. In systems that use discrete logic, these design problems appear at the board level. But in PLD-based systems, they seem to be device problems.

Not surprisingly, then, many PLD problems are related to logic design practices at the device level. A number of these problems can be avoided by careful design practices. Thorough simulation, using the software simulators that PLD manufacturers and third-party vendors supply, will also lessen logic design flaws.

Clock timing is one source of these problems. Nearly all digital designs include some registered logic and, thus, a clocking scheme. Often, one or more clocks are controlled by a logic function in another part of the design. The function may be as simple as one gate, such as a NAND, AND, or NOR gate, or may include more complex logic. Although designers are usually careful about creating and checking the clock's Boolean function, they sometimes overlook potential timing hazards.

For example, intermediate states during logical transitions can cause glitches at the gated function's output. The glitches may last only a few nanoseconds, but that's long enough to clock edge-sensitive functions. Clocks that come from single gates will be reliable if no more than one input changes within the time required for the gate's output to settle to the correct value. If two or more inputs change within this period, the potential for glitching exists.

Even a simple AND gate is susceptible to glitching. If the gate's two inputs change value simultaneously from "zero-one" to "one-zero," the gate's output should theoretically remain at zero. But if the inputs pass through state "one-one" on the way to their final state, the gate will output a one during that period *(Fig. 2)*. The incorrect output will be very short, but it may be long enough to clock a flip-flop.

Clocks controlled by more complex logic are difficult to implement reliably in discrete logic, yet are even tougher in PLDs. The problem concerns complex functions that may get implemented in multiple levels of logic within the PLD. Because inputs to such a function can feed different levels simultaneously, designers must allow for a settling time as the signals propagate through all levels. During this time, the function's output may change state, making the function unsuitable as a clock.

The situation is further complicated because designers seldom have precise control over how the PLD design software will minimize the logic. Consequently, the problem can't be avoided by controlling the timing of the inputs to the clock-controlling function.

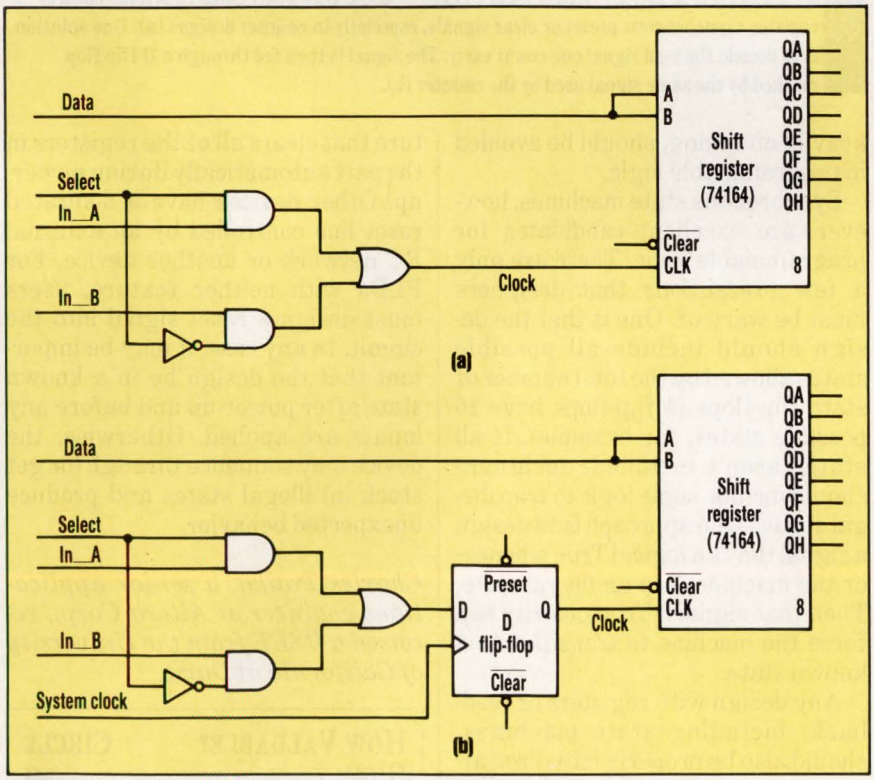
The best way to eliminate this hazard is to avoid complex gated clocks. One synchronous clock can control all of the registered functions in the design. Then designers can create the appropriate logic (D, T, J, K, etc.) for the register data inputs, which aren't edge-sensitive and must be qualified by the system clock.

For example, designers can convert the output of a multiplexer from a potentially hazardous clock signal to a clean clock signal by adding a flip-flop. The multiplexer's output becomes the D input of the flip-flop, whose Q output clocks the original function, which in this case is a shift register *(Fig. 3)*. The system-clock line clocks the flip-flop, thus qualifying the multiplexer's output. The design must include enough set-up time between the changing of the multiplexer inputs and the system clock's arrival.

Gated functions can cause a similar problem when they control register asynchronous preset or clear signals. The same type of glitch that's a nuisance for clock functions can incorrectly preset or clear a register.

Counter designs are particularly susceptible to this problem. For example, one common practice is to decode the output of a counter to check for some terminal count. The decoded output is then used to asynchronously load the same counter, employing preset and clear controls on the counter flip-flops.

This design practice creates two potential hazards. First, designers



3. CLOCKS CONTROLLED BY COMPLEX LOGIC can cause glitches because of timing problems (a). Connecting the gated function to a flip-flop that's clocked by a synchronous system clock avoids such problems (b).

WORKING WITH PLDS

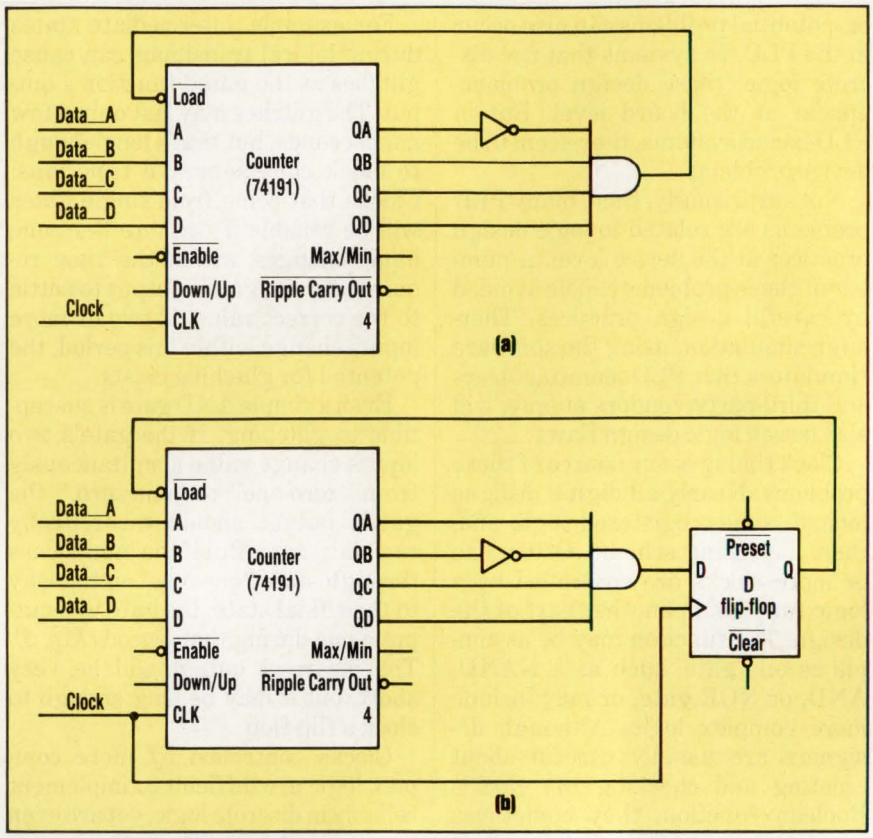
can't ensure that all flip-flops change state at exactly the same time, so the decoded output may glitch. A glitching output may load an incorrect value into the counter. While the counter is loading, the decoded "load" signal starts to become false, possibly trapping the counter in some intermediate state.

One solution is to use synchronously loaded counters and design the appropriate load logic. Another option is to retain the asynchronously loaded counters but decode the load signal from the counter outputs one count early. This result is fed into the data input of a D flip-flop, which is clocked by the same clock used for the counter *(Fig. 4)*. Finally, the Q output of the flip-flop becomes the counter's asynchronous load input. This design ensures that the counter has a valid load signal for one clock cycle.

PLDs also engender other timing issues. For instance, designers occasionally use an even number of inverters to create delays. But PLD design software minimizes logic without regard for timing, so two series inverters become just a wire. As a result, delay elements should generally be avoided in PLDs.

The completed design's timing should be examined to ensure that it doesn't exceed the device's maximum speeds. Most manufacturers supply timing models and parameters to aid in this design verification. Sophisticated timing analysis tools are also available for higher-density PLDs. To make sure that the largest PLDs operate properly, designers must perform complete functional and timing simulations with software supplied by the manufacturer or third-party vendors.

Not all designs lend themselves to PLD implementation. For instance, PLDs can accommodate designs that rely on combinatorial feedback if they don't require precise timing control. But many programmable device architectures are unable to handle combinatorial feedback within a logic array, so designers must consume a macrocell feedback. And asynchronous state machines, whose proper operation depends heavily on timing, should be avoided in programmable logic.



4. TIMING PROBLEMS CAN ALSO OCCUR when gated functions control register asynchronous preset or clear signals, especially in counter designs (a). One solution is to decode the load signal one count early. The signal is then fed through a D flip-flop clocked by the same signal used by the counter (b).

Synchronous state machines, however, are excellent candidates for programmable logic. There are only a few precautions that designers must be wary of. One is that the design should include all possible states allowed by the total number of state flip-flops (4 flip-flops have 16 possible states, for example). If all states aren't included, designers should include some logic to trap illegal states. One approach is to design a signal that's a logical True whenever the machine is in an illegal state. Then that signal's True polarity can force the machine to transition to a known state.

Any design with registers or feedback, including state machines, should also be properly initialized after power-up. Some PLDs, such as Altera's EP and EPM families of devices, include a power-on reset feature that clears all of the registers in the part automatically during power-up. Other devices have a dedicated reset line controlled by an external RC network or another device. For PLDs with neither feature, users must design a reset signal into the circuit. In any case, it may be important that the design be in a known state after power-up and before any inputs are applied. Otherwise, the device may sequence through (or get stuck in) illegal states and produce unexpected behavior.

Charles Tralka, a senior applications engineer at Altera Corp., received a BSEE from the University of California at Davis.

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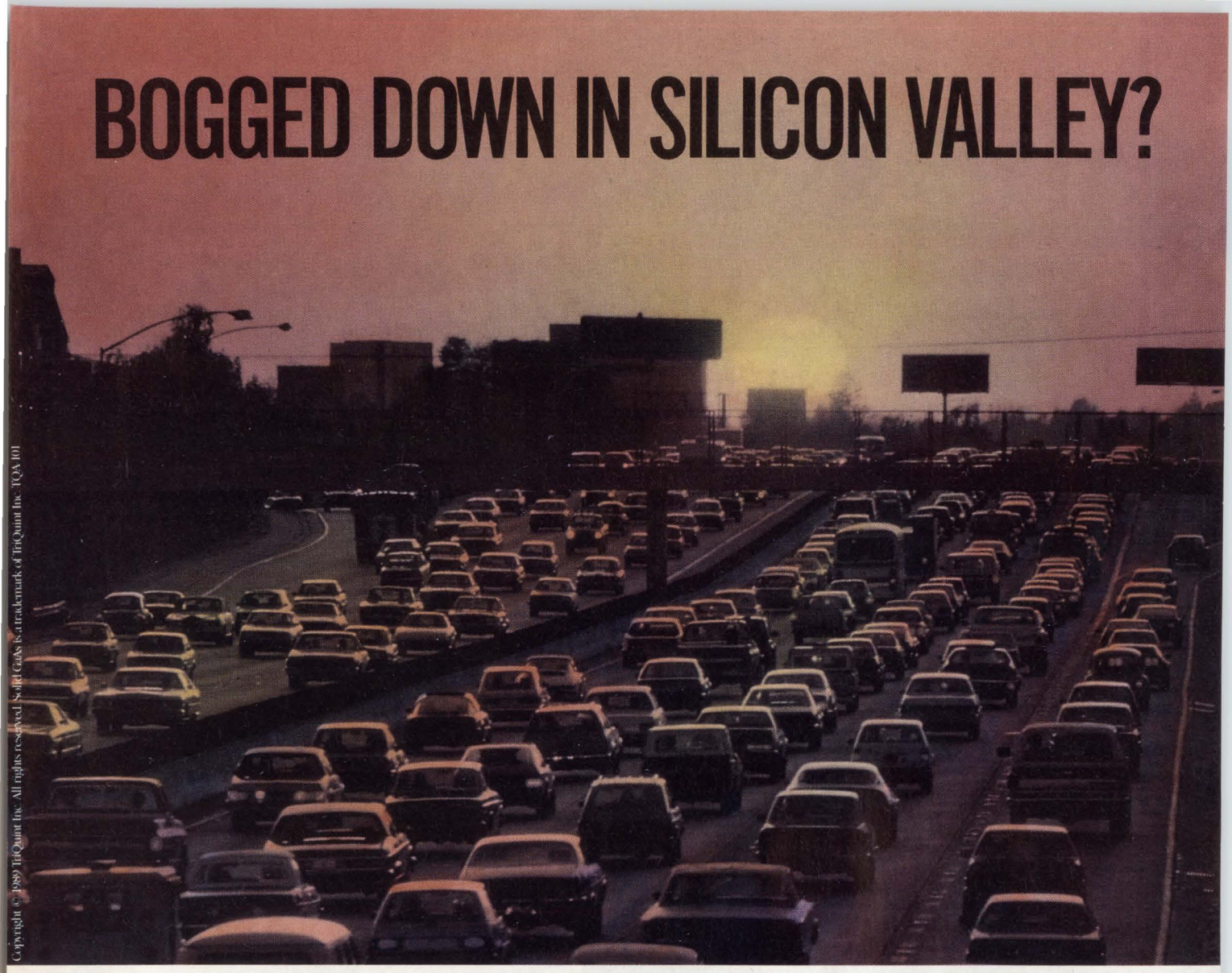

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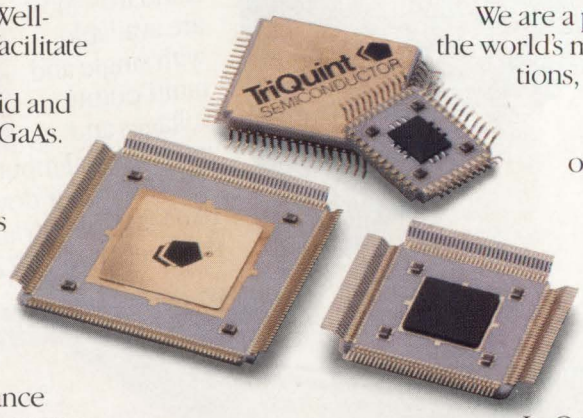

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CIRCLE 167

Designing For PC SYSTEMS

UNDERSTAND EISA BUS-CYCLE TRANSLATIONS

CREATE FLEXIBLE EISA-BASED SYSTEMS BY MATCHING 8-, 16-, OR 32-BIT EXPANSION CARDS TO THE BUS

The enormous popularity of the IBM personal computer, introduced in 1981, and its successor, the PC/AT in 1984, has led to the computer's expansion bus architecture as an accepted de facto industry standard. Billions of dollars have been invested by system and peripheral manufacturers in hardware and software to duplicate and enhance what's commonly known as the Industry Standard Architecture (ISA) bus. For its time, the ISA offered system users a reasonable amount of expansion capability and performance, with a 24-bit address path, a 16-bit data bus, and an 8-MHz peripheral bus. Moreover, attachments for the bus were relatively simple to develop.

In 1988, a consortium of computer companies developed the Extended Industry Standard Architecture (EISA) bus *(see "A Snapshot of the EISA bus", p. 86)*. The EISA bus, which is a superset of the ISA bus, gives designers a 32-bit architecture that has a 32-bit address path and uses an 8-MHz system bus clock. The bus architecture supports conventional slave-mode expansion boards and multiple-bus-master capability. Bus-master cycles and DMA operations achieve data-transfer rates of 33 Mbytes/s using a burst-mode feature included in the EISA definition.

EISA is fully backward compatible, which makes it possible to use old or new ISA add-in boards and software with the more powerful EISA-based systems. At the same time, the specification doesn't require that EISA boards comprehend ISA bus cycles. As a result, EISA card designs can be implemented more easily. The system motherboard hides the complicated details of interfacing to ISA devices from the EISA devices, and translates bus cycles between the two architectures for card-to-card transfers.

The EISA architecture enhances the interupt scheme by allowing interrupt sharing. The interrupt lines can be individually programmed to the ISA-compatible, edge-triggered mode or EISA-sharable, level-triggered mode.

By thoroughly understanding the cycle translation mechanisms, EISA buses can be built to accept 8-, 16-, and 32-bit expansion boards. To keep the expansion-card design as simple as possible, the EISA bus logic incorporated on the system

AMARESH KUMAR
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DESIGN APPLICATIONS

UNDERSTANDING EISA BUS CYCLES

motherboard significantly eases the data transfer between devices of different data sizes. EISA bus masters don't need to run multiple cycles if the slave board's data bus is smaller; the data byte resequencing is handled by the system board. In the original 8-bit PC architecture, there was no provision for bus masters—the system-board CPU or DMA chips always controlled the bus. When the PC/AT arrived on the scene, it introduced the concept of asynchronous 16-bit bus masters and 8- or 16-bit slave cards.

And now that EISA has arrived, 32- and 16-bit synchronous slave modes are also defined. They have the option of supporting burst cycles.

Smart Bus Masters

Bus masters can control the bus, then select the desired operation and control the cycles on their own. They don't require using the main system CPU as a controller during data transfers, as do less intelligent slave boards.

The system CPU can operate in parallel, resulting in increased system performance. Even more intelligent bus masters would have a local CPU that can preprocess data, further reducing the burden on the main CPU. Bus masters serve in various applications, such as graphic or network controllers.

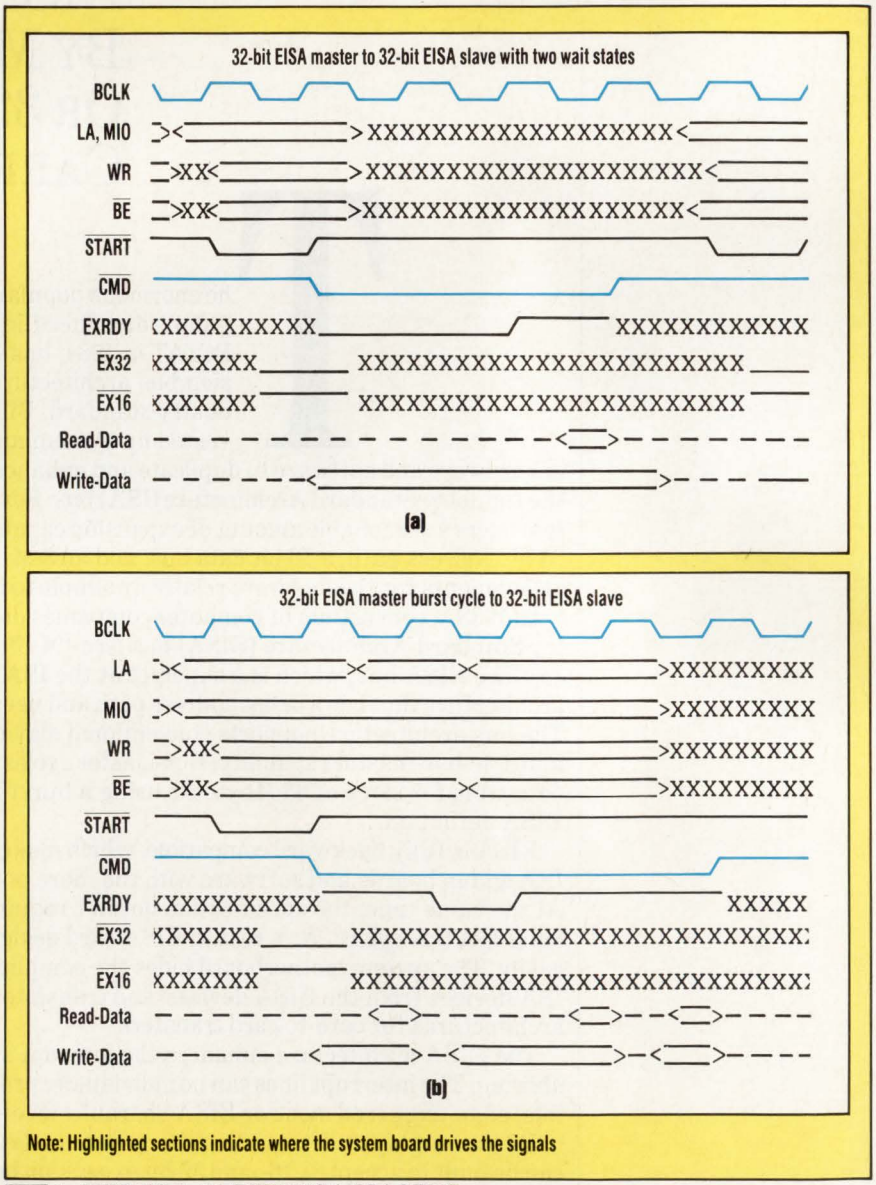
In addition to supporting relatively low-transfer-speed asynchronous ISA bus masters, the EISA bus permits synchronous bus masters to burst-transfer data at 33 Mbytes/s. Such burst transfers are only possible if both the EISA master and slave cards support the burst mode, and the slave's data-path size is equal-to or greater-than that of the master. This would seem to rule out 32-bit EISA masters from running burst cycles to 16-bit EISA slaves. However, 32-bit bursting EISA masters can be designed to "downshift" their size. As a result, they would shift on-the-fly to appear as a 16-bit card, and then run burst cycles to a 16-bit slave.

Because the EISA bus talks to different sizes of both masters and slaves, it must translate bus cycles if the master and slave types don't match. Furthermore, the bus controller on the system board must determine which master controls the bus by decoding the EXMASTER, MASTER16 and MSBURST signals *(Table 1)*.

The control starts when the EXMASTER signal is generated by the system-board arbiter after an EISA master is granted the bus. In return, if the board is a 16-bit or EISA master, the MASTER16 signal is driven by the board. (MASTER16 is also driven by 16-bit ISA masters when they control the bus.

MASTER16 is usually valid before the start of the cycle. But, if the signal is sampled and is high at the beginning of the START signal and low at the end of START, the master is a 32-bit bursting master that will downshift to 16 bits if a 16-bit bursting slave responds.

The system board decodes the EISA and ISA slave-size signals (EX32, EX16, M16 and IO16) so that



1. WHEN A 32-BIT EISA MASTER communicates with a 32-bit EISA slave, the system board keeps the CMD line active for the length of the non-burst transfer cycle, which requires two BCLK cycles (a). With a burst-cycle transfer, data can be read or written on every BCLK cycle, improving the system's overall data-transfer rate (b).

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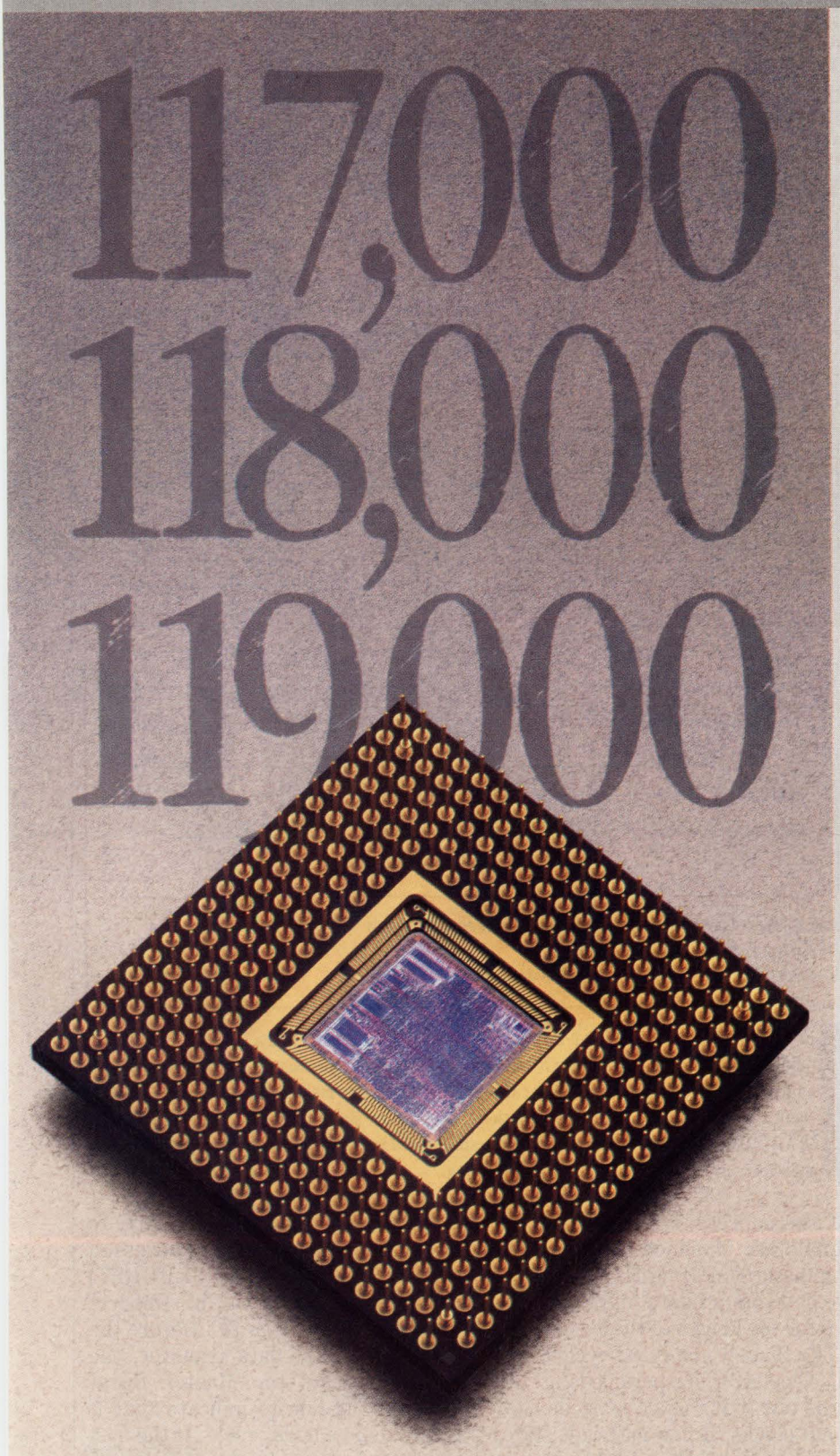

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CIRCLE 172

DESIGN APPLICATIONS

UNDERSTANDING EISA BUS CYCLES

it can determine the type and size of the slave *(Table 2)*.

The different masters and slaves result in varied combinations of cycles *(Table 3)*. If the master and slave types don't match (the master and slave aren't both EISA or ISA), then the system board will translate control signals from EISA to ISA or vice-versa.

If an EISA master happens to be addressing a slave of smaller size, then the system board will copy the data between byte lanes and, if necessary, run multiple cycles.

The type of cycle executed by the bus master depends on the data width of the master and slave, and whether they're ISA or EISA compatible. Consider the case of a 32-bit EISA master. The master must first request control of the EISA bus by asserting its Master Request ($\overline{\text{MREQ}}$) signal. The system board arbitrates between the different requests.

When its turn comes, the bus is granted to the master and its Master Acknowledge ($\overline{\text{MAK}}$) signal is asserted. The master then drives the Unlatched Address (LA) lines and the Memory-I/O (MIO) signal. It then pulses $\overline{\text{Start}}$ low for one bus clock and drives the Byte Enable ($\overline{\text{BE}}$) and Write-Read (WR) signals. Halfway through $\overline{\text{START}}$, the system board copies the address on the LA lines onto the Latched System Address (SA) lines.

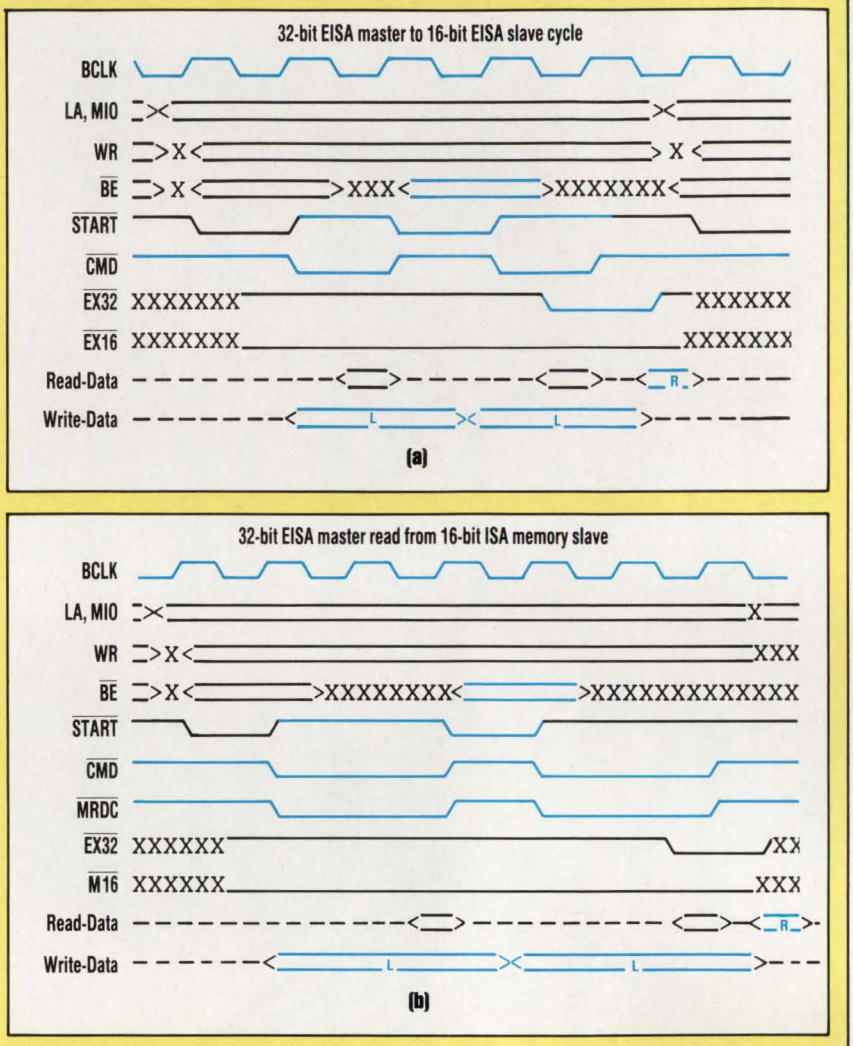
DECODING

EISA and ISA slaves then decode the address, and the addressed slave responds. The 32-bit EISA master doesn't care which slave responded, it just samples $\overline{\text{EX32}}$ to see if it found a matching-size slave. If a match occurred, the cycle proceeds without the need for anyparticipation from the system board. A 16-bit master must sample both $\overline{\text{EX32}}$ and $\overline{\text{EX16}}$. If either one is active, it decodes a match. Consequently, a 16-bit master cycle to a 32-bit EISA slave is defined as a match. Moreover, the system board handles routing the data between the upper and lower word, if necessary.

In a 32-bit matched non-burst cycle, the address, $\overline{\text{BE}}$, MIO, and WR signals are pipelined *(Fig. 1a)*. The Command ($\overline{\text{CMD}}$) signal is generated by the system board and is kept active for the length of the cycle.

The fastest non-burst cycle is two Bus Clock (BCLK) periods long. If it turns out that the slave needs additional clocks, it can add wait states by negating the EISA Ready ($\overline{\text{EXRDY}}$) signal.

The burst cycle starts similarly to a non-burst cycle. The addressed slave drives Slave Burst ($\overline{\text{SLBURST}}$) active to indicate that it supports burst transfers *(Fig. 1b)*. Before the end of the first data transfer, the master asserts the Master Burst ($\overline{\text{MSBURST}}$) line to indicate that it wants to do a burst cycle. If the system board samples both $\overline{\text{MSBURST}}$ and $\overline{\text{SLBURST}}$ active, and if the mas-



2. THE DATA TRANSFER between a 32-bit EISA master and a 16-bit EISA slave requires more signals to be driven by the motherboard. This is because the 32-bit data must be sent in 16-bit sections to the 16-bit card (a). When the same master exchanges data with a 16-bit ISA memory slave card, the operations require more time, as shown by the longer $\overline{\text{START}}$, $\overline{\text{CMD}}$, and $\overline{\text{MRDC}}$ signals (b). The system board must also do more work to translate the EISA bus cycles to ISA cycles and vice versa.

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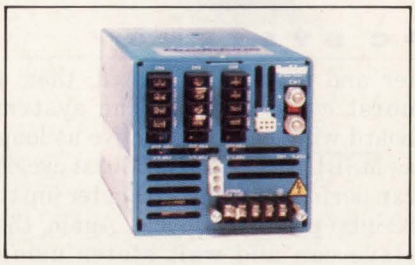

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DESIGN APPLICATIONS

UNDERSTANDING EISA BUS CYCLES

ter and slave sizes match, then a burst cycle results. The system board will keep $\overline{CMD}$ active as long as $\overline{MSBURST}$ is active. Burst cycles can perform one data transfer (up to 32 bits) per BCLK cycle. Again, the slave can add wait states using $\overline{EXRDY}$.

If no matching slave responds (for example, the slave size isn't equal to or greater than the master's size, or the slave isn't an EISA slave), the master "backs off" the bus and enables the system board to complete the cycle. The system board takes over the $\overline{START}$ signal and the Byte Enables ($\overline{BE}$), and runs multiple cycles to the smaller slave. If the slave was an ISA slave, the system board also generates ISA control signals. For write cycles, the system board latches the data from the master before it backs off, and redrives the data onto the appropriate byte lanes to match the slave size. For read cycles, the system board latches the data from the slave in smaller pieces, and at the end redrives the assembled data for the master. After this sequence is done, the system board signals the EISA master by driving $\overline{EX32}$ active ($\overline{EX16}$ for 16-bit masters).

The $\overline{EX32}$ and $\overline{EX16}$ lines thus serve dual functions: they provide the slave-size decode at the beginning of a cycle, and signal the end of

TABLE 1: MASTER SIZE AND TYPE DETERMINATION

Master size	$\overline{EXMASTER}$	$\overline{MASTER16}$	$\overline{MSBURST}$
32-bit non-bursting EISA master	0	1	1
16-bit non-bursting EISA master	0	0	1
32-bit bursting EISA master	0	1	0
32-bit bursting EISA master (with downshift)	0	1-0 (pulse)	0
16-bit bursting EISA master	0	0	0
16-bit ISA master	1	0	X

Note: 1) X – signal not decoded
2) $\overline{EXMASTER}$ is generated by the system arbiter when an EISA master controls the bus.

A SNAPSHOT OF THE EISA BUS

Because the EISA bus is a superset of the signals on the popular ISA (PC/AT) bus, this overview of EISA assumes a basic knowledge of the signals on the standard ISA connector. The EISA connector is rather unusual, in that it contains two rows of contacts for each side of the expansion card that slips into the connector. The upper set of connector contacts contains all of the ISA signals and is used when an ISA card is plugged into the connector. The lower rows of contacts mate to the new contacts included on the EISA cards, nearly doubling the number of contacts.

The major signals on the EISA connector include a 32-bit data bus; a latched 20-bit address bus; a segmented, unlatched address bus; and many new control signals. The following is a simplified description of each signal and the bus it's associated with:

BCLK (ISA signal) Bus Clock. Signal frequency can range from 6 to 8.33 MHz. This clock synchronizes events on the bus. Its period can be extended (or "stretched") by the system board. This increases performance in some applications.

D[15:0] (ISA signal) Data bus. These are the lower 16 lines that duplicate the 16-bit ISA data bus.

D[31:16] (EISA signals) Data bus. These include the upper 16 bits that provide the EISA bus extension to 32 bits.

SA[19:0] (ISA signals) System Address. These are the lower-20 latched bits of the system address lines and are valid throughout a bus cycle.

$\overline{SBHE}$ (ISA signal) System Bus High Enable. This line indicates whether the upper byte of a word is involved in a transfer. Along with SA0, it allows ISA masters to do byte or word accesses. For example if SA0 = 0 and $\overline{SBHE}$ = 0, the master is accessing the entire word; if SA0 = 1 and $\overline{SBHE}$ = 0, only the upper byte is being addressed. Similar to the SA bus, $\overline{SBHE}$ is valid throughout the cycle.

$\overline{LA[31:24]}$ LA[16:2] (EISA signals) Unlatched Address. In addition to the latched system LA[16:2] addresses, the ISA bus provides unlatched upper (EISA signals) address bits LA[23:17] (latchable address). The EISA bus extends the LA bus to the entire 32-bit-addressing range. The latchable addresses may be pipelined from one cycle to the next, and can be latched at the trailing edge of $\overline{START}$. Note that the upper 8 bits are inverted logic, making it possible for pull-up resistors to force their value to one. This results in the upper address being zero.

LA[23:17] (ISA signal) Unlatched Address. Upper ISA address bits.

$\overline{BE[3:0]}$ (EISA signal) Byte Enable. There are four signals, one for each byte in the data path. The signals access different portions of the 32-bit double word. For example, $\overline{BE[3:0]}$ = 0011 indicates that the upper word is being accessed. Byte enables are pipelined like the LA address bus.

AENx (ISA signal) Slot specific Address Enable signal for slot x. When this signal is low, it indicates that the I/O slave may respond to the bus cycle. The signal selectively addresses I/O cards in their slot-specific address range. During DMA cycles, it's driven high by the system board to prevent I/O slaves from responding to the I/O control strobes being generated for the DMA device.

$\overline{MSBURST}$ $\overline{SLBURST}$ (EISA signals) Master and Slave Burst. $\overline{MSBURST}$ is asserted by an EISA master to indicate that the master wants to do a burst cycle. If the slave can support burst cycles, it asserts $\overline{SLBURST}$ before the end of $\overline{START}$. If both $\overline{MSBURST}$ and $\overline{SLBURST}$ are asserted and the master's data bus size is smaller-than or equal-to the slave's data bus, or if the master downshifts its size tp match the slave size, then a burst cycle results. The burst cycle continues until $\overline{MSBURST}$ is de-asserted.

UNDERSTANDING EISA BUS CYCLES

system board's handling of a mismatched cycle *(Fig. 2)*.

In the case of a 32-bit master sending data to a 16-bit EISA slave, the change in the EX32 signal indicates that a 32-bit EISA card is finishing a transfer cycle to a 16-bit EISA slave *(Fig. 2a)*. A 32-bit communication with a 16-bit ISA slave starts much the same, but the cycles are longer to meet the ISA slave requirements *(Fig. 2b)*.

When a 16-bit EISA master communicates with a 16-bit ISA slave, the bus interfaces are considered to be mismatched even though the sizes match. This is done so that the EISA master doesn't have to drive ISA signals—the system board does the translation.

ISA masters arbitrate for the bus using the DMA Request (DRQ) signal, and the system board grants the bus by activating the corresponding DMA Acknowledge (DAK) signal. The master presents the SA and LA address, and then drives the ISA command strobe—Memory Read, Memory Write, I/O Read, or I/O Write (MRDC, MWTC, IORC or IOWC). The system board samples the slave signals to see what kind of slave responded.

If both EX32 and EX16 are inactive, the master is addressing an ISA slave. The only role the system board plays in this case is to copy the data

TABLE 2: SLAVE SIZE AND TYPE DETERMINATION

Slave	EX32	EX16	M16	IO16
32-bit EISA	0	X	X	X
16-bit EISA	1	0	X	X
16-bit ISA (memory cycle)	1	1	0	X
16-bit ISA (I/O cycle)	1	1	X	0
8-bit ISA (memory cycle)	1	1	1	X
8-bit ISA (I/O cycle)	1	1	X	1

Note: 1) X – signal not decoded

EX32, EX16 (EISA signals) EISA Slave Size. The system board uses these signals to determine the data width of the expansion card. It also uses them to signal the end of a cycle translation to an EISA master.

M16, IO16 (ISA signals) ISA Memory, and I/O Slave Size signals. ISA slaves generate these signals without using MIO. The master or system board samples the appropriate signal.

EXRDY (EISA signal) EISA Slave Ready signal. Used by EISA slaves to add wait states to the standard 2-BCLK cycle, or to the 1-BCLK-per-data-transfer burst cycle.

CHRDY ISA (ISA signal) Ready signal. Used by ISA slaves to add wait states to the standard cycle length.

NOWS (ISA signal) No Wait State signal. Used by ISA slaves to remove the default wait states from an ISA cycle, and by EISA slaves to run 1.5 BCLK compressed cycles.

START, CMD (EISA signal) Start and Command - These are timing-control signals for EISA cycles. START is asserted for one BCLK after the LA bus becomes valid. CMD is asserted by the system board when START is negated and remains active for the length of the cycle.

WR (EISA signal) Write/Read. A status signal that identifies cycles as either Read or Write. It becomes valid after START goes active.

MIO (EISA signal) Memory-I/O. A status signal that indicates whether the cycle is Memory or I/O. It has the same timing as the LA address bus.

IORC, IOWC, MRDC, MWTC, SMRDC, SMWTC, (ISA signals) ISA Read and Write strobes. IORC and IOWC are I/O read and write strobes, while MRDC and MWTC are for memory read and writes. SMRDC and SMWTC are asserted only when the address range is in the 00000000 (h) to 000FFFFF (h) range.

LOCK (EISA signal) Bus Lock. This signal is asserted by masters to gain exclusive access to memory or I/O resources. Lock allows test-and-set operations on semaphores to be run as a unit, without another master gaining access in between.

BALE (ISA signal) Bus Address Latch Enable. This signal, which indicates that the LA bus is valid, is used by ISA slaves to latch the address. It's recommended that EISA slaves use START or CMD and not BALE to latch the address.

MREQx, MAKx (EISA signals) Master Request and Acknowledge lines for slot x. EISA bus masters use MREQ to request the EISA bus. The system board arbiter acknowledges that the bus was granted using MAK.

DRQ[7:5][3:0], DAK[7:5][3:0] (ISA signals) DMA Request and Acknowledge. The DRQ signals are used by DMA devices and ISA masters to request control of the EISA bus. The system board responds that the bus was granted using DAK.

T-C (ISA signal) Terminal Count. This signal is used in two modes. As an output, it's asserted by the DMA controller on the system board to indicate end of a DMA transfer count. As an input, it's used by the DMA device to terminate the DMA cycle.

MASTER16 (ISA signal) Master Size. This signal is asserted by EISA or ISA masters.

REFRESH (ISA signal) Refresh. This signal indicates that a refresh cycle is in progress.

OSC (ISA signal) Oscillator. A 14.31818-MHz clock for timing applications.

RESDRV (ISA signal) Hardware Reset. This signal resets all boards on the bus.

IRQ[15:14] [12:9][7:3] (ISA signal) Interrupt Request lines. These lines can be used to interrupt the system CPU.

IOCHK (ISA signal) I/O Check. This signal is asserted by an EISA or ISA board to indicate a serious error.

DESIGN APPLICATIONS

UNDERSTANDING EISA BUS CYCLES

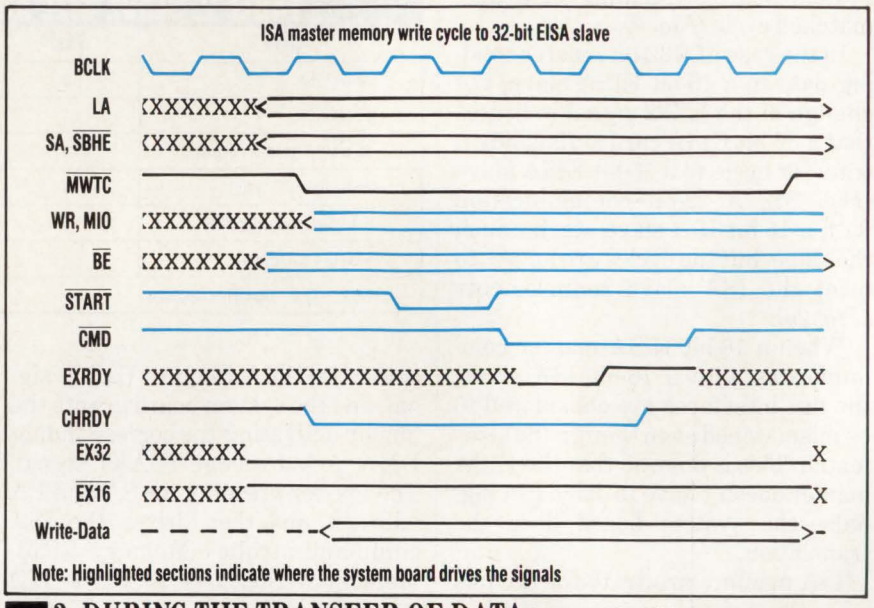
between the two lower data byte lanes, if necessary. For example, if the 16-bit ISA master writes one byte to an 8-bit ISA slave at an odd address (SA0 = 1), then the system board will copy data from D[15:8] to D[7:0].

However, if $\overline{EX32}$ or $\overline{EX16}$ is active, the master is addressing an EISA slave and the system board translates the ISA command strobe into EISA signals, $\overline{START}$ and $\overline{CMD}$ *(Fig. 3)*. The system board also drives MIO and WR to the appropriate value depending on which ISA command is active. While the translation is being done, the system board puts the ISA master on hold by pulling the Channel Ready (CHRDY) low. After the EISA cycle is done, CHRDY is released and the master terminates its cycle.

Intel's 82350 EISA chip set makes it easy to design a system board that performs the aforementioned cycle translations. The chip set compresses most of the motherboard logic down to three basic chips—the 82352 bus buffer, the 82357 integrated system peripheral (ISP), and the 82358 EISA bus controller (EBC). A fourth chip, the 82355 bus master interface controller (BMIC), was designed for expansion cards and reduces the design complexity of bus master add-in cards *(Fig. 4)*. The 82352 bus buffer chip could be used as many as three times in a system, buffering the address bus, data bus, and local DRAM storage.

The EBC is the bridge between different masters and slaves. It performs all of the cycle translations required to talk to ISA and EISA boards with different data widths. Furthermore, it can tie into either 80386 or 80486 CPUs and control the address and data bus buffers between the host bus and EISA bus. One special feature of the EBC is its ability to allow host slaves to stretch the bus clock period. As a result, slower host slaves responding to bus master cycles don't have to add full BCLK wait states, but can stall the master for periods in increments of the host CPU clock.

The ISP, like the standard PC chip



3. DURING THE TRANSFER OF DATA from a 16-bit ISA memory master card to a 32-bit EISA slave card, the system board pulls the CHRDY line low to put the ISA master on hold until the cycle translation is finished. When the line is released, the master terminates the transfer cycle.

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No. 4

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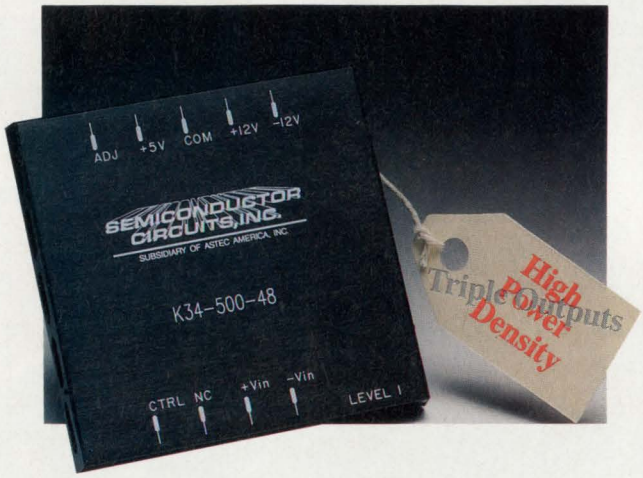

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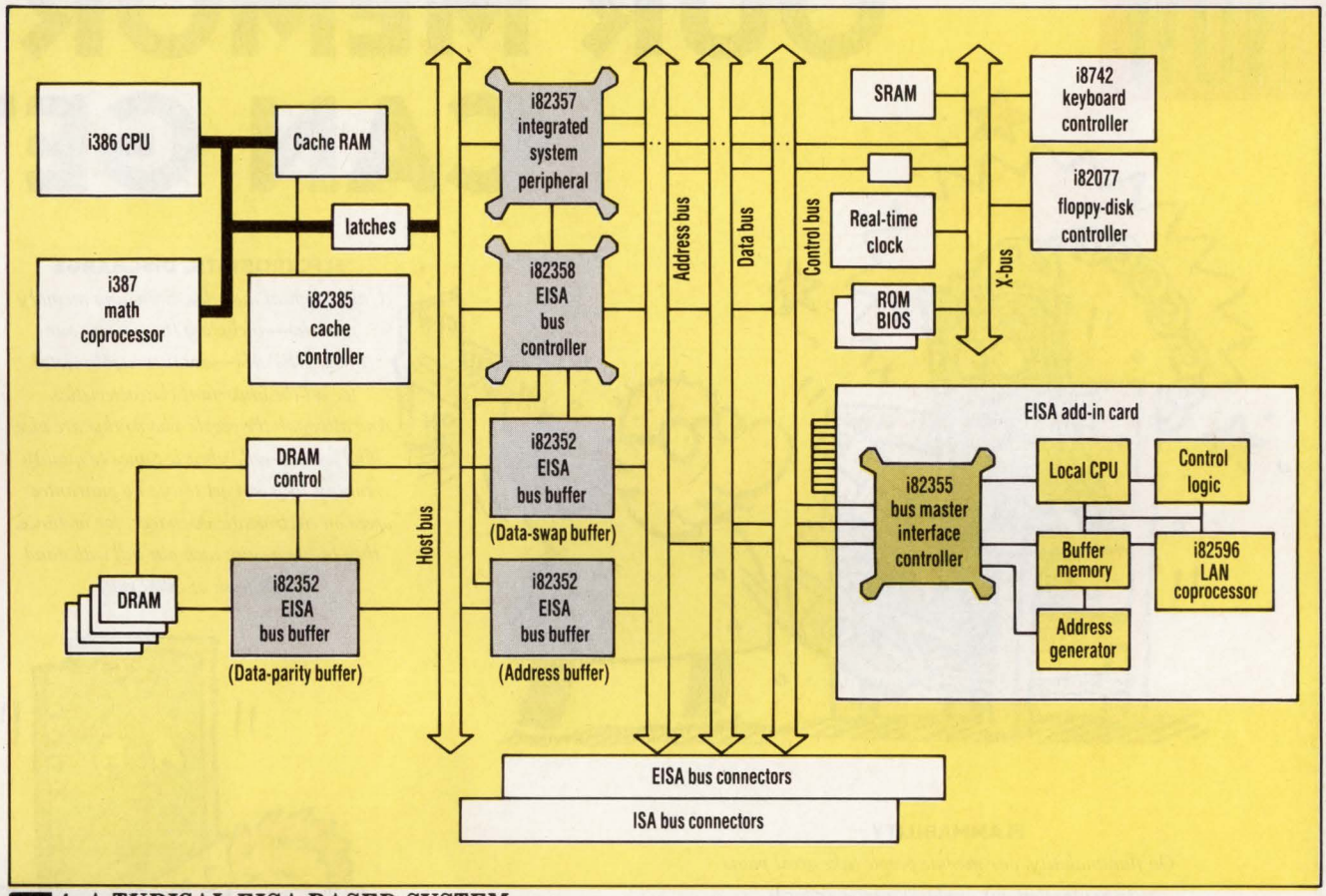
CIRCLE 108

UNDERSTANDING EISA BUS CYCLES



4. A TYPICAL EISA-BASED SYSTEM implemented with Intel's 82350 motherboard chip set enables either EISA- or ISA-compatible cards to plug into the expansion bus. Bus-master EISA cards, such as a smart LAN card, might typically use the 82355 bus-master interface controller.

sets, integrates the commonly required system resources. Those resources include seven 32-bit DMA channels, two 8-channel interrupt controllers, five 16-bit timer/counters, and refresh control and arbitration logic. The buffer chip includes bus buffers for a 32-bit path of the EISA bus. Lastly, the BMIC chip simplifies the design of bus-master expansion cards and has automatic downshifting to enable direct, burst transfers to occur with both 32-bit and 16-bit EISA slave cards.□

Amaresh Kumar, the design project manager for Intel's EISA bus control products has been with the company for five years. He received a BSEE from the Indian Institute of Technology, Kanpur, India, in 1983 and an MSEE from Syracuse University in New York in 1985.

TABLE 3: ROLE OF THE SYSTEM BOARD BUS CONTROLLER

Master type	Cycle type	Slave type			
		32-bit EISA	16-bit EISA	16-bit ISA	8-bit ISA
32-bit EISA (no downshift capability)	non-burst	—	BO, MC, DC	BO, MC, DC, CT	BO, MC, DC, CT
	burst	—	X	X	X
32-bit EISA (downshift capable)	non-burst	—	BO, MC, DC	BO, MC, DC, CT	BO, MC, DC, CT
	burst	—	—	X	X
16-bit EISA	non-burst	DC	—	BO, CT	BO, MC, DC, CT
	burst	DC	—	X	X
16-bit ISA	non-burst	DC, CT	CT	—	DC

BO = Master Backs Off, letting the bus controller complete the cycle
MC = The system board may have to run Multiple Cycles
DC = The system board may have to do Data Copying between byte lanes
CT = The system board performs Cycle Translations from EISA signals to ISA signals or vice versa
X = Cycle isn't possible

Note: 1) For compatibility, the system board doesn't translate a 16-bit cycle from an ISA master to two 8-bit cycles for an 8-bit ISA slave. The master takes care of this itself. The system board only does the necessary data copying.

2) ISA devices don't support burst cycles.

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MODERATELY	548
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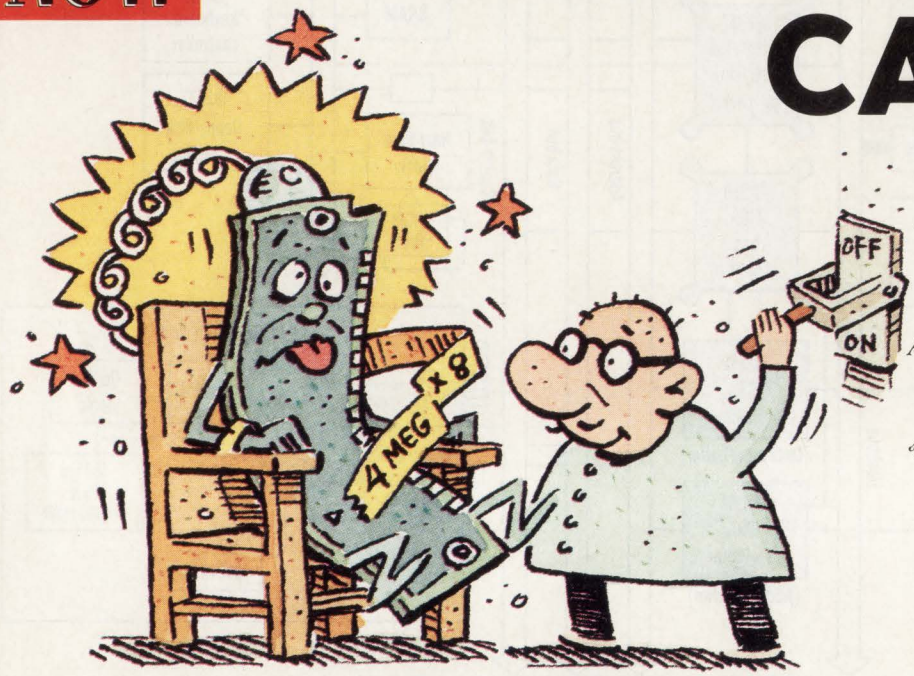

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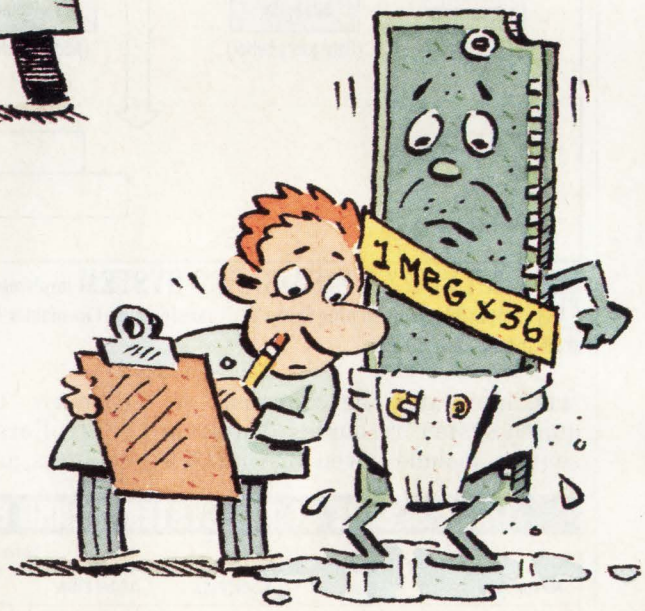

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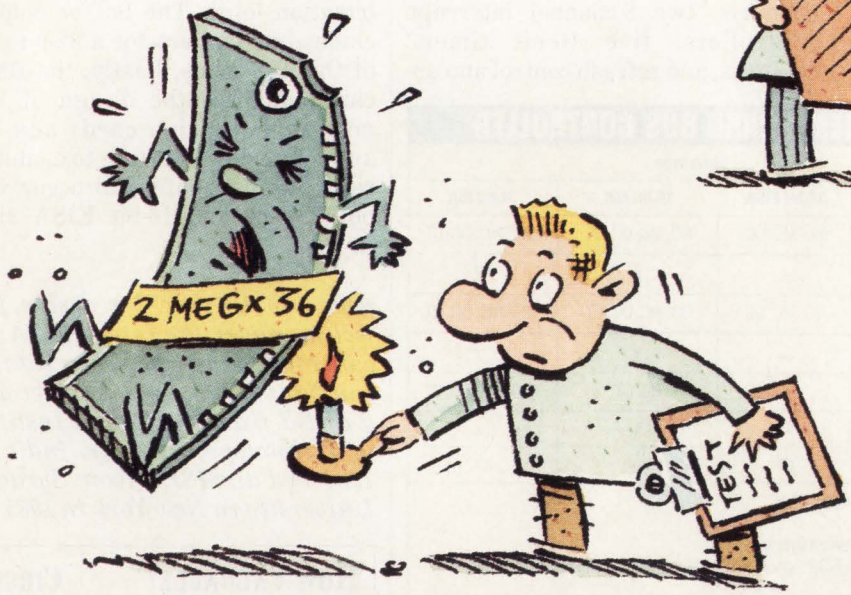

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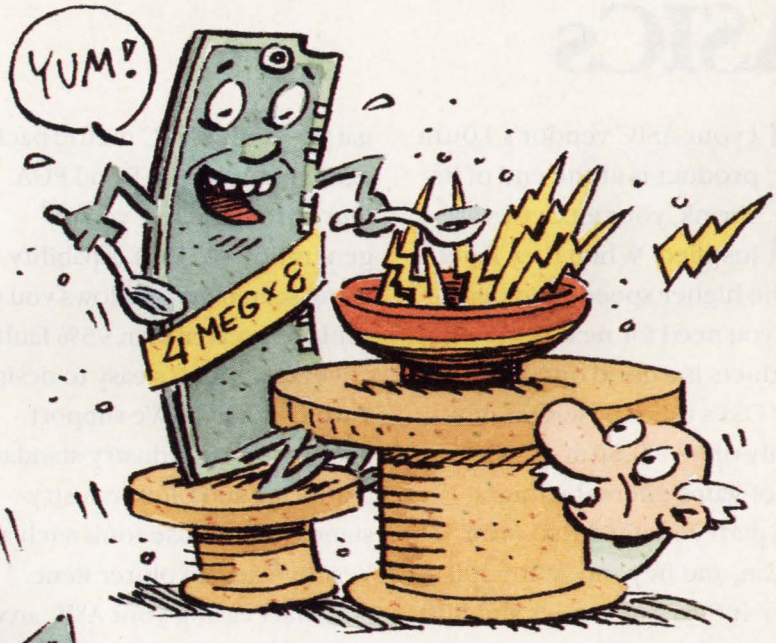

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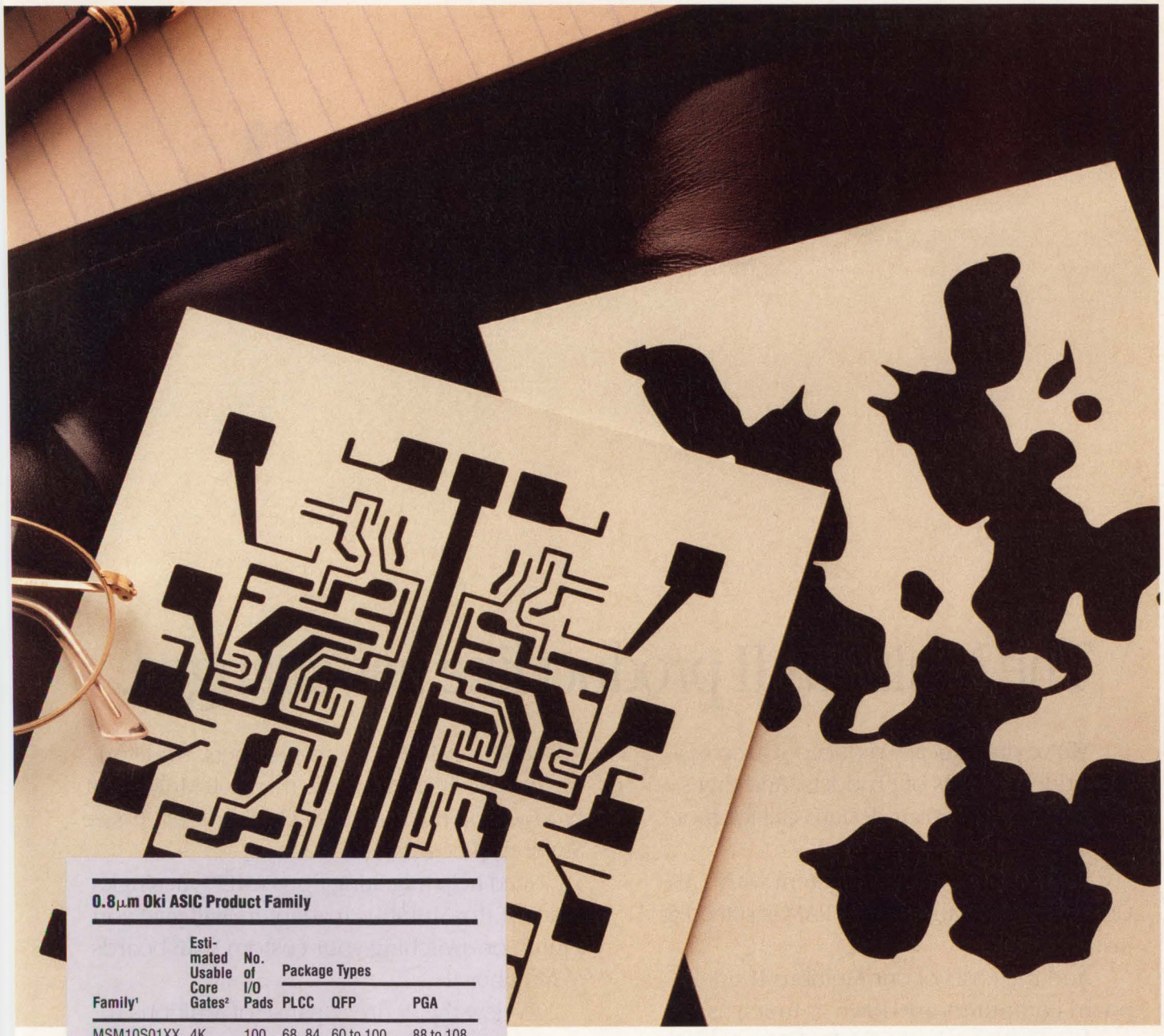

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MSM10S05XX	22K	208		120 to 208	108 to 208
MSM10S09XX	36K	272		144 to 272*	108 to 256
MSM10S11XX	47K	304		144 to 304*	132 to 301
MSM10S18XX	72K	384		144 to 304*	208 to 340
MSM10S23XX	92K	424		144 to 304*	240 to 340

[1]Other products are under development
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QUICKLOOK

1-MINUTE OPINIONS

What do you think about the education that young engineers are getting these days? How strong a role should humanities courses play?

My opinion is that our engineers forgot the basics.

The humanities courses represent in my opinion a very important subject in the social development of young engineers, based on the fact that we do not want to have robots. We want to have engineers with elastic minds, able to understand all aspects of life and production. In that way, they are able to develop systems and products that are more cost effective.

Yes, education is only a starting point. On-the-job training is the adhesive between theory and practical application. Therefore, I consider it necessary for new graduates to work directly in production for one or two years after college—not in the office—directly on the production line. In this way, when they get a job with responsibilities, they have production experience and are able to design products that are profit-oriented. **Ed Anghel,** *Amityville, N. Y.*

Are you aware of the technocratic, mercenary microchips that are coming from this country's engineering schools? A college education used to mean that the degree holder had at least a rudimentary idea of who he was, where he came from, and some fundamentals in living that come from those "excess" humanities classes.

When we decry the demise of ethics, empathy, and honesty in this country, let's first look at what we teach our students. Let's put the post-Sputnick paranoia to bed and help our students be good people first and good engineers second. If that takes five years, so be it. **Name withheld.**

From the starting gate, it is my feeling that many come out of school not ready—and in more ways than one. For many graduates, the fact that it is their first working experience doesn't help much. Those initial steps are often most critical, for they indeed place individuals on tracks that they perhaps have a vague notion of. I have seen this utterly destroy the potential of many. Coupled with often inadequate interpersonal skills and the bottom-line driven nature of American business as a whole, and you wonder why anyone would pursue such a career.

For engineering to receive the respect it deserves, help must come from all quarters. The educational system might consider a revised degree system, differentiating various skill levels to a far greater granularity than currently exists. Industry can assist by recognizing this and by giving the various engineering titles only to those who are indeed engineers by training. There is a huge difference, but this often is ignored, and engineers get lumped in with all kinds of people who often do not even come close to them in terms of the rigorous education they have gone through.

Engineers themselves could use a dose of common sense as well. The attitude that being organized is beneath them has got to stop—it doesn't bother medical doctors one bit to be a part of the AMA. Engineers should recognize that being organized does not mean old style unions but does mean achieving the clout they deserve in the professional climate in which they should exist. It will only be under circumstances such as these that engineers achieve the stature they deserve and the recognition that they are often the backbone of many businesses. **John A. Nevin,** *Middle Village, N. Y.*

What's your opinion on the education of today's young engineers? Which areas are being under- or over-emphasized? What role should humanities courses play in engineering education? Are four years enough to give young engineers a good foundation? Send your opinions to our fax (201) 393-0637 or to Compuserve address 75410,3624. Or mail your responses to *Electronic Design,* Reader Opinions, 611 Route 46 W., Hasbrouck Heights, NJ 07604.

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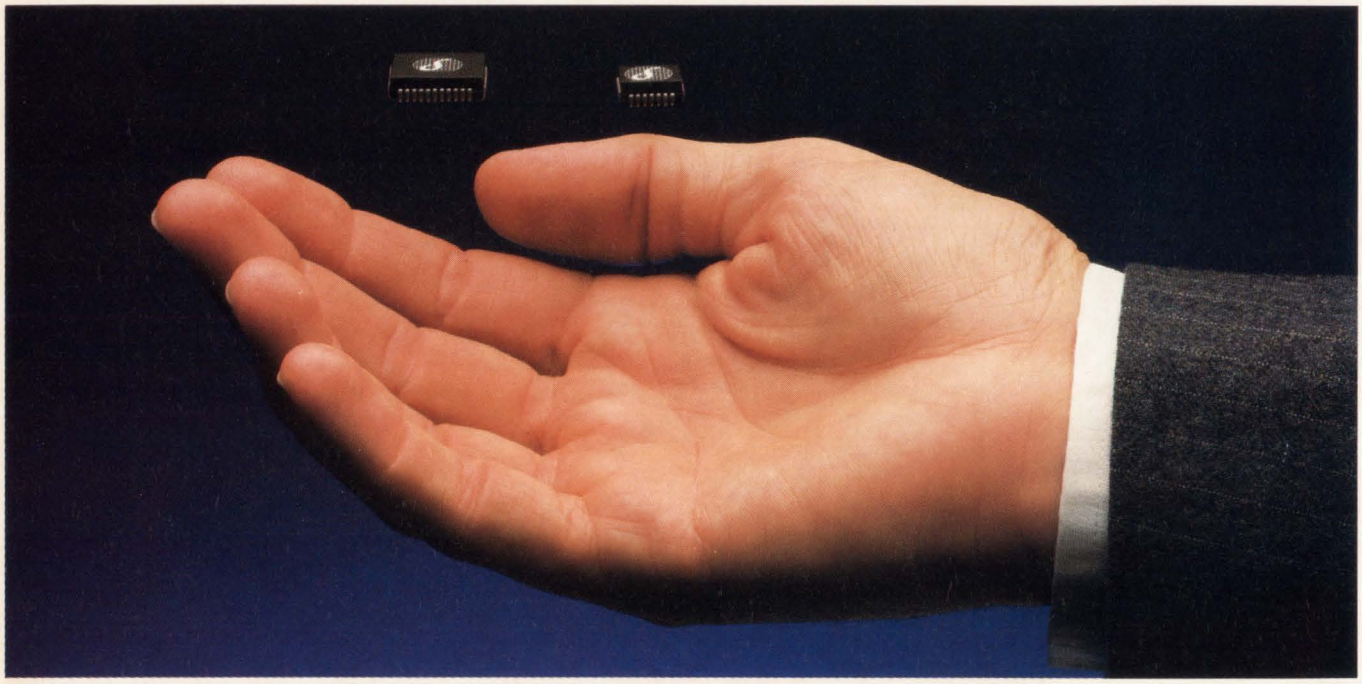

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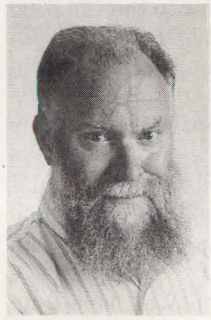
WHAT'S ALL THIS NOISE STUFF, ANYHOW? (PART II)

To circumvent the noise-testing problems discussed in my last column, I decided to build up my own test fixture for measuring transistor base-current noise. First I made up a schematic *(see the figure)*. As a sanity check, I showed it to a bunch of people. One guy did spot that I was violating the common-mode (CM) range of the LM627 main amplifier. So I told him *thank you* and added a couple of 1N914 diodes to bring the common-mode range down to a legal level (I could have bluffed and told him, I made that mistake on purpose, to see if anybody was paying attention, but I figured that this wasn't the right time to play that game, as it wasn't true....).

People asked me, "Aren't you going to run it on batteries? You need low-noise supplies to see a low noise, don't you?" Answer, no. Modern power supplies are pretty quiet, and this balanced (differential) amplifier (Q_{1A} and Q_{1B}) doesn't need any more help than that. Also, it has a pretty good power-supply rejection ratio (PSRR).



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

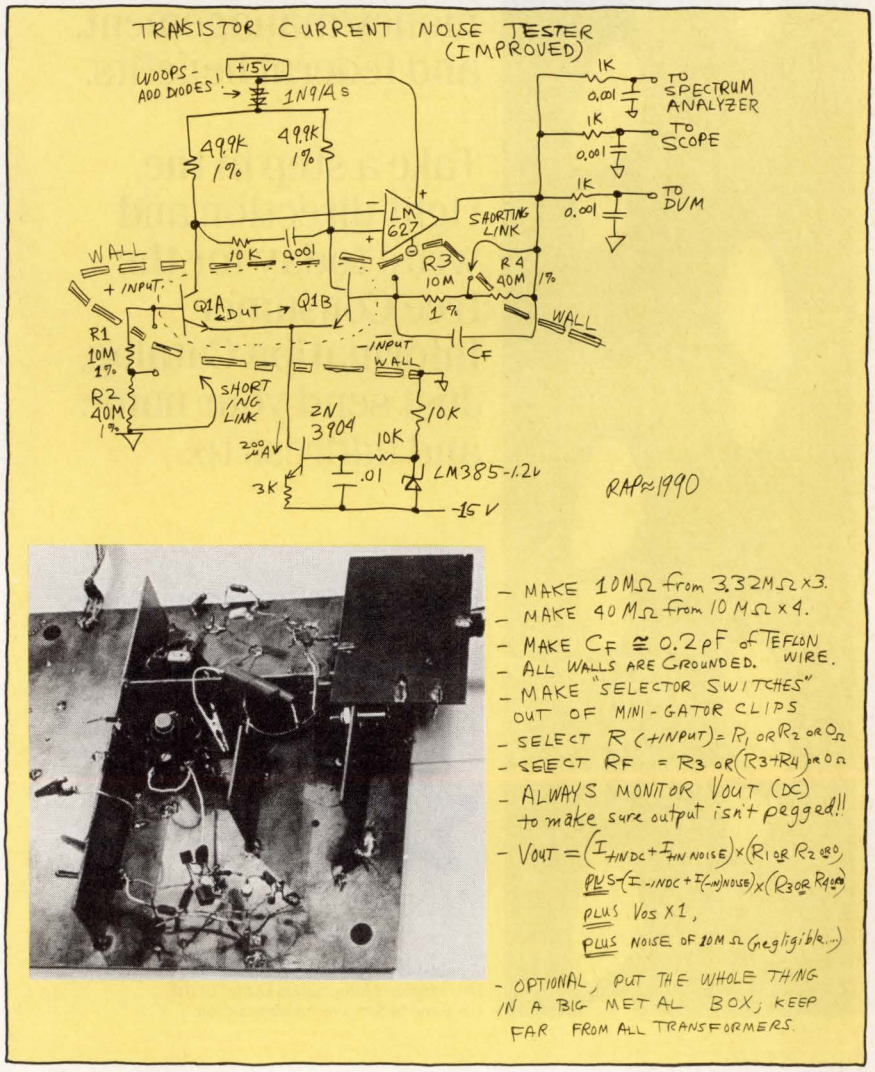
Then they said, "Aren't you going to put the fixture in a big sealed box?" No, that's not necessary. In fact, usually I just run it out in the open, without even a cover, right on my bench.

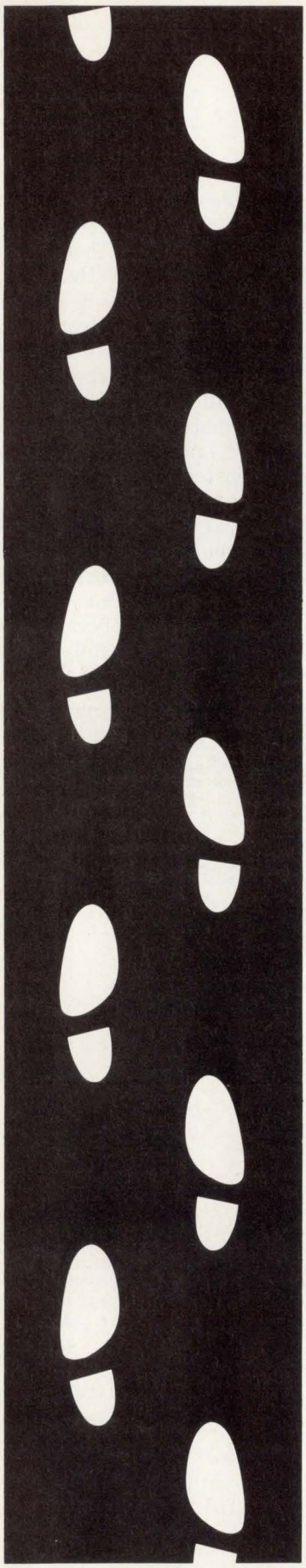
Usually, I do have to turn off the soldering iron to get decent results. I also have to move it away from various instruments whose power supplies spray flux all around.

The first thing I did with this fixture was add a label that said you have to monitor the dc output level. That's to ensure that if the output pegs (hits the supply rail), you don't want to believe the output noise levels. The next disclaimer I added stated that the bandwidth is indeterminate and depends on the layout—even a fraction of a picofarad of stray capacitance has major effects.

We fired it up and it gave us pretty reasonable data. It told us that the transistors' base current noise was down around the theoretical levels, at least above 100 Hz. We've been too busy recently to devote time to getting the spectrum analyzer running down at 10 Hz, but that can wait. Then we checked on the high end of the frequency range. I started out with a feedback capacitor (C_F) made out of about 2 inches of twisted pair, (around 2 pF) and unwound it.

As the capacitance decreased, the bandwidth got up above 10 kHz, up toward 20 kHz. That means our feedback capacitor is less than 1/3 pF. We worked to get that because we built the feedback resistor out of three 3.32-MΩ resistors, so their in-





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PEASE PORRIDGE

herent capacitances would be put in series and thus decreased. Also, we built "walls" out of copper-clad pc board to prevent any stray capacitance between the output and the input. Heck, the output can't even *SEE* the input. To connect a 0.5-pF capacitor from the output to the input, we require it to climb over one of those walls.

We haven't used the 50-MΩ feedback resistor yet (which is made out of five 10-MΩ resistors in series), but that approach will give us good resolution when the transistors run a mere 4 to 12 μA of emitter current. Note, this circuit is just about the same as we would use to measure the base-current (bias current) noise of any op amp. But when you do that, the stray capacitance of the socket makes it pretty hard to get less than 0.5 pF from the output to the input, especially when you're using dual or quad amplifiers.

With an op amp, you may even have to run your test with one of the pins pulled out of the socket, for evaluation. For production, you make a pc-board layout with guarding between the pins. Refer to the LMC660 data sheet (printed after June 1990) for information on guarding techniques.

Therefore, we confirmed that it is possible to make low-noise measurements. If you're careful, you can just build up a simple circuit with a simple amount of shielding. And you can check at all times to see if there are 60 Hz or 120 Hz or 5 MHz noises intruding into your circuit.

One thing is certain, blind trust is definitely out of place here; thinking is required at all times. We also confirmed that the transistors really *were* low-noise. In fact, they were close to the noise floor, with fewer noisy ones than usual. So, that's encouraging.

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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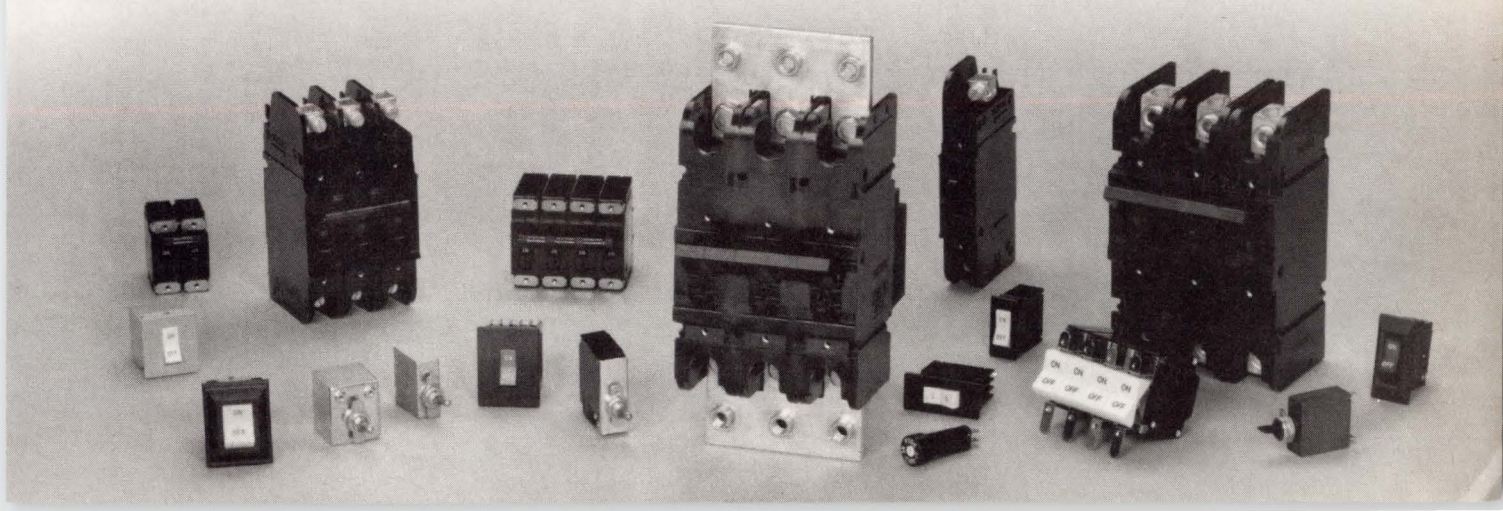

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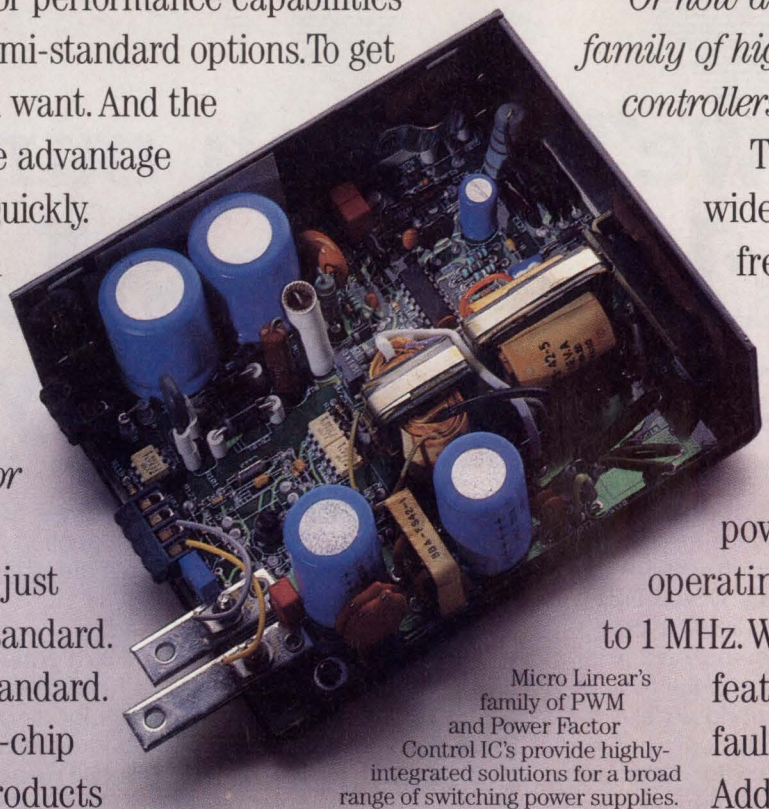

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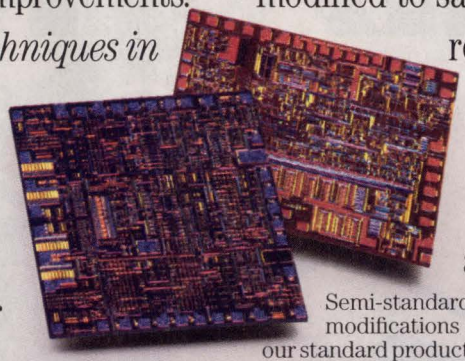

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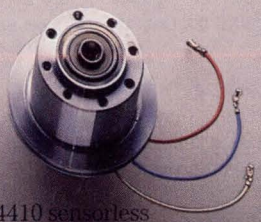

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The SCM-1 spans 1 to 500MHz and the SCM-2 covers 10 to 1,000MHz. Housed in a rugged, non-hermetic 0.4 by 0.8 by 0.3 in. high (maximum dimensions) plastic/ceramic package. Spacing between connections is 0.2 in. The mixer is offered with leads (SCM-L) or without leads (SCM-NL) to meet a wide range of pc board mounting configurations.

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FREQ. RANGE (MHz)		
LO,RF	1-500	10-1000
IF	DC-500	DC-500
CONVERSION LOSS (dB)		
Midband	6.3 dB	6.5 dB
Total Range	7.5 dB	8.0 dB
ISOLATION (dB)	(L-R)(L-I)	(L-R)(L-I)
Low-Band	60 45	45 35
Mid-Band	45 40	35 30
High-Band	40 35	25 20
PRICE	$3.30 (1000 qty) $4.25 (1-9)	$4.15 (1000 qty) $5.45 (1-9)

Units are shipped in anti-static plastic "tubes" or "sticks" for automatic insertion.

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CIRCLE 521

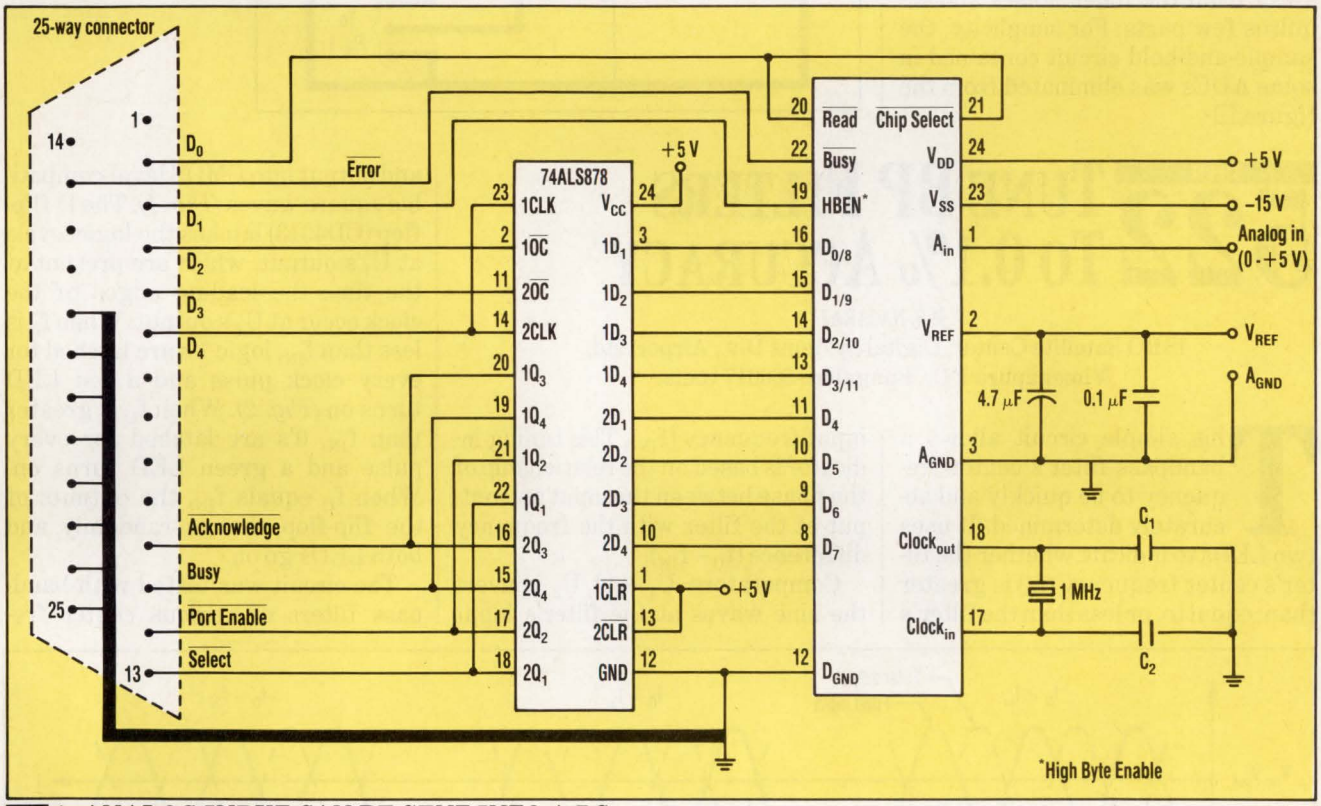
CONNECT ADC TO PC'S I/O PORT

LIN JUN
University of Leicester, Dept. of Engineering, Leicester LE1 7RH, U.K.

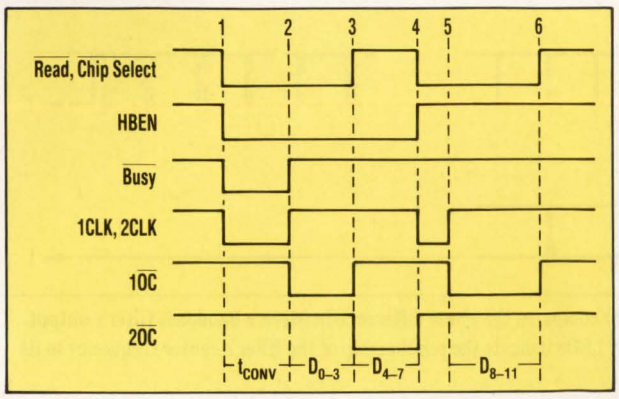
A standard IBM PC isn't equipped with any obvious unallocated general-purpose I/O ports. Therefore, to connect an analog-to-digital converter (ADC) to a PC, a plug in a-d card must be placed in one of the PC's expansion slots. However, it would be more convenient to connect the ADC to the PC without opening the machine, and imperitive if either all of the slots are filled or it contains no slots.

Most PCs—from 8088-based laptops to the latest 80386-based machines—are equipped with a parallel printer port, supplying a standard hardware interface and a place to connect an ADC. An a-d card using this approach requires only two ICs and is based on the PC/XT/AT 25-pin D-type socket *(Fig. 1)*. The 12-pin a-d converter (AD7572, MAX162, or MAX172) is controlled by the PC's data-output port 378H, and the 12-bit conversion result is read through port 379H's status input lines.

Only five pins of the 25-way connector are connected to port 379H.



1. ANALOG INPUT CAN BE SENT INTO A PC by connecting an ADC and a D flip-flop to the PC's parallel port. The ADC is controlled by the output of the PC's port 378H.



2. SIGNAL d_0 from the 25-way connector controls the a-d converter's Read and Chip Select inputs, while D_1 controls the High—Byte Enable. D_{2-4} are connected to 1OC, 2OC, and 1CLK and 2CLK.

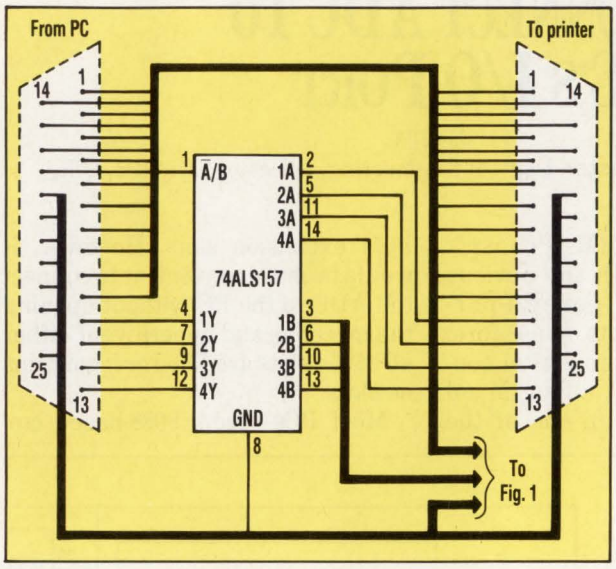
Therefore, 12-bit data must be read three times through the port. This can be done by controlling the D-type flip-flop, 74ALS878. All signals except the Busy signal are generated by port 378H's output *(Fig. 2)*.

Connecting the a-d converter to the PC carries some flexibility—certain components can be substituted for others. For example, two 74HCT374's can take the place of the 74ALS878 and the 12-bit ADCs can be replaced by 10- or 8-bit parts. Fur-

thermore, an ADC with more than 12 bits can be connected. The unused bits of port 378H can be employed to control the multiplexer. In addition, eight channels can be easily expanded for this circuit.

If a printer is connected to the port at the same time as the a-d converter, use a 74LS157 to switch the input lines of port 379H *(Fig. 3)*. Here, the select signal is connected to the SLCT IN of port 37AH.

If the speed isn't very high, the described method works better than a plug-in card because it's further away from the inner noises and requires few parts. For simplicity, the sample-and-hold circuit contained in some ADCs was eliminated from the figure.□



3. A printer can be connected to the port at the same time as the a-d converter. In this case, a 74LS157 is used to switch the input lines of port 379H.

CIRCLE 522

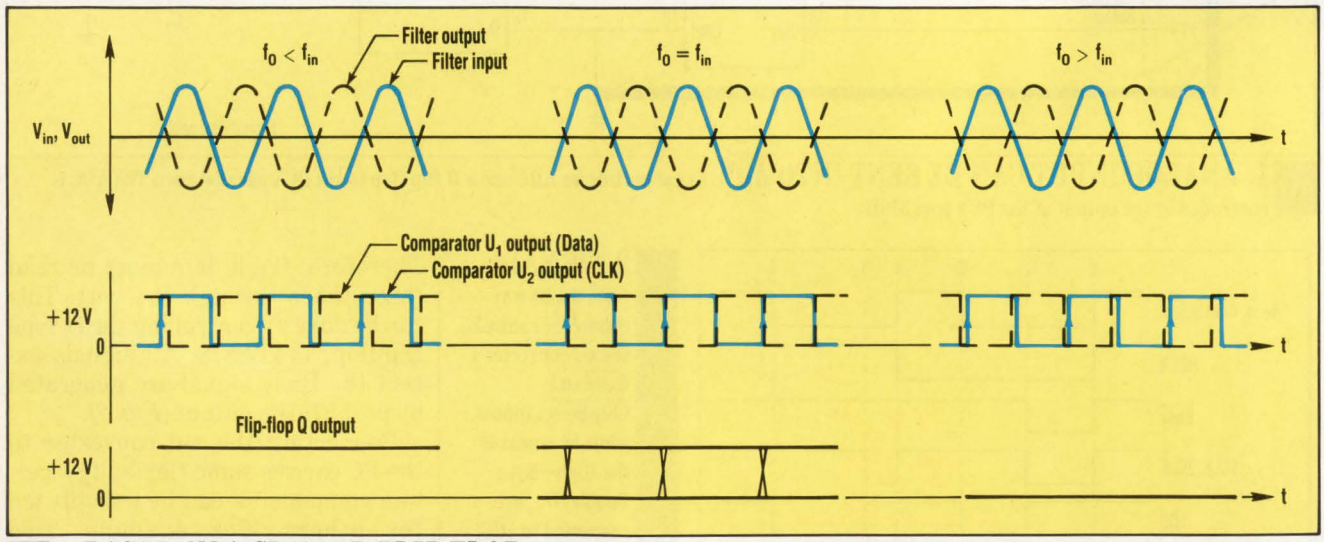
TUNE BP FILTERS TO 0.1% ACCURACY

M.S. NAGARAJ
ISRO Satellite Center, Digital Systems Div., Airport Rd.,
Vimanapura P.O., Bangalore 560017 India.

This simple circuit allows a bandpass filter's center frequency to be quickly and accurately determined. It uses two LEDs to indicate whether the filter's center frequency (f_0) is greater than, equal to, or less than the filter's input frequency (f_{IN}). This tuning indicator is based on the relationship of the phase between the input and output of the filter with the frequency difference ($f_0 - f_{IN}$).

Comparators U_1 and U_2 convert the sine waves at the filter's input and output into CMOS level-compatible square waves *(Fig. 1)*. The D flip-flop (CD4013) latches the logic levels at U_1's output, which are present at the time the leading edges of the clock occur at U_2's output. When f_0 is less than f_{IN}, logic 1's are latched for every clock pulse and a red LED turns on *(Fig. 2)*. When f_0 is greater than f_{IN}, 0's are latched for every pulse and a green LED turns on. When f_0 equals f_{IN}, the outputs of the flip-flop change randomly and both LEDs go on.

The circuit was tested with bandpass filters of various center fre-



1. BASED ON A CD4013 D FLIP-FLOP, this tuning indicator compares the phase difference between a bandpass filter's output and input. The Q and $\overline{Q}$ outputs drive red and green LEDs, respectively. The LEDs indicate the relationship of the filter's center frequency to its input frequency.

CLEARPOINT

NEW PRODUCT REVIEW

Fall, 1990 The more information you have, the better we look . . . Clearpoint. Vol.1 No. 2

Five reasons to buy a CPU for your memory-hungry VME-based system with limited memory

Graphics and image processing, MRI imaging, huge number crunching jobs– all typical VMEbus applications and all memory intensive. Designers of VME-based systems need to evaluate performance, features, and cost requirements of the overall system, not just the CPU. Adding minimal memory to the CPU and additional memory to the backplane offers several advantages, including:

Improved System Performance

High speed processors that include memory are a poor utilization of hardware. Since memory is packed onto the CPU card, any access to memory from the VMEbus ties up the CPU, slowing system performance.

Lower Cost

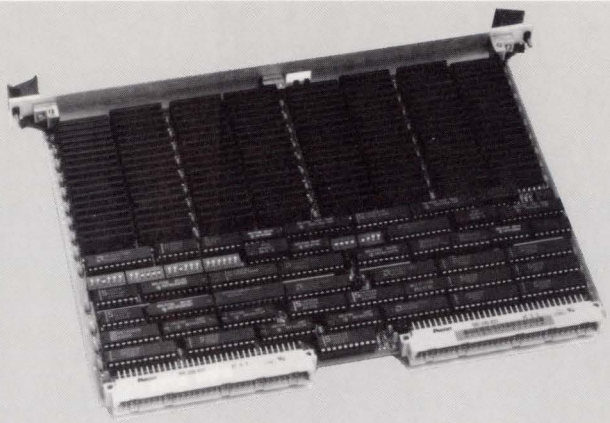
Most memory-intensive applications require more memory than is available on a CPU card. Users can cut system costs by buying the CPU and memory individually. Memory can be added as needed, and systems do not suffer because of CPU limitations.

CONTINUED ON PAGE 2

Guaranteed by a Lifetime Warranty

All Clearpoint's memory products are backed by a fully-transferable, lifetime warranty. Clearpoint offers the most extensive warranty and service program available for VME-based open-architecture memory, including:

- 24-hour toll-free technical support hotline
- Next-day repair or replacement policy



The VMERAM-FP1 (shown), and all Clearpoint memory products, are supported by a lifetime warranty.

High density, fast VME-compatible memory . . . Guaranteed!

Hardware designer Leo Cierpial on memory design for the VMEbus: "The goal of the VMERAM-FP1 design was to make the fastest memory possible with today's technology. Equally important, we wanted to fully implement the many features and options of the VMEbus specification, and conform to all of its rules under worst-case conditions."

The VMERAM-FP1 is an engineering innovation from Clearpoint Research Corporation. Available in 4 to 64 MB densities, the VMERAM-FP1 boasts block transfer cycles of 100 ns for reads and 74 ns for writes. Increased performance is achieved using fast page-mode access of DRAMs during block-transfer cycles. Fast random access and cycle times are achieved, in part, by decoding the address in parallel with the start of the memory cycle. This technique increases the possible gains in system performance by VME MASTERS using address pipelining.

The 4, 8, 12, and 16 MB boards are designed with 70 ns, 1 megabit DRAMs; 32, 48, and 64 MB boards use 80 ns, 4 megabit DRAMs. When 4 megabit DRAMs become available in 70 ns speeds, our highest density boards will use the improved technology.

The VMERAM-FP1 supports all VMEbus addressing and data transfer types–block mode (BLT), unaligned (UAT), and address only (ADO). Supporting 32-, 16-, and 8-bit data transfers, the VMERAM-FP1 can be configured for 32- and/or 24-bit addressing.

The VMERAM-FP1 offers byte-wide parity protection; if an error is detected during a read cycle, a VMEbus "BERR*" may be issued over the bus. Control bits are provided in the control-status register (CSR) to enable or disable reporting of a parity error via the BERR* signal line of the VMEbus.

The CSR is a Motorola-compatible, 8-bit hardware register, which allows users to control and access parity error status information. It is assigned a user-configurable address in the I/O page and may be accessed by system software. Other features include CAS-before RAS refresh, and battery back-up capability.

VMERAM-FP1 . . . the design engineer's memory choice!

Speed vs. Specmanship: Data Transfer in the Fast lane

The VMEbus specifications allow system integrators to configure systems using products from various manufacturers. The specifications are said to describe a maximum data transfer rate of 40 MB/second. Some board manufacturers claim that this theoretical maximum is the actual data-transfer speed of their VME product. Unfortunately, it is not easy to judge these claims, either because all the needed product specifications are not made available, or they are not presented clearly. In short, there's a lot of room for "specsmanship" when statements are made about the speed of a VMEbus product. A closer look at a real VME system data transfer will clear up some of the smoke surrounding the VME specs.

For the buyer of bus system devices, there are ways to avoid being mislead by specsmanship and to assure that your system is maximizing its data transfer rate potential.

- Examine every component in the system – All systems have a weak link, but the speed of your system can be seriously limited by an out-of-date device or by one which doesn't match the capabilities of your master devices. Swap out devices to isolate system bottlenecks. By trying various combinations of devices, you can find the optimum combination for your system.
- Get the real numbers – There can be a significant difference between minimum cycle times (the sum of which gives the maximum speed of the system) and actual cycle times. Adding up the timing of every part of the system will give you the speed of a configuration.
- Do software benchmarking – This will give you empirical evidence of system performance under actual operating conditions, and will also provide a standard for comparison.

CONTINUED FROM PAGE 1

Getting the Right Memory

Memory installed on VME-based processors rarely offers the range of features required for today's applications. Buying memory separately allows you to choose the memory features you need – fast or slow, parity or EDC – without paying a premium for those options you don't require.

Space Savers

Real estate on VME-based CPU cards is a valuable commodity. Memory installed directly on processor cards often takes space from processing functions which cannot be added elsewhere in a VME system. Buying a CPU with memory can mean sacrificing CPU functionality; adding memory separately leaves space for the functionality you need.

Avoid the Double Whammy

In multiprocessor systems, memory on the CPU can cause significant loss of overall system performance. When one CPU needs memory information from the other processor, both get tied up performing a single bus cycle.

Clearpoint's VMERAM-FP1 offers speed, density, and flexibility to meet your open-architecture needs.

About Clearpoint

Clearpoint was founded in 1982 on the premise that memory is a unique component of a computer system, requiring a different set of capabilities for production. Since its inception, Clearpoint has focused first and foremost on engineering. Core product offerings include add-in memory for VME, DEC, Sun, HP/Apollo, IBM, Compaq, and Apple Macintosh.

In 1989 Clearpoint expanded this expertise to the storage market with its high performance SCSI-based storage subsystem. Memory or storage – Clearpoint's innovative designs provide compatibility, value, and performance now while laying the foundation to serve you well into the future.

Our company-wide pledge to deliver reliability and performance

QC CLEARPOINT

Quality Commitment

VME-Compatible EDC Memory

Clearpoint offers several single-bit error correction and double-bit detection memory boards for the VMEbus and the VSB subsystem bus. Our entire VME/VSB product line supports all VMEbus addressing (24- and 32-bit) and data transfer (8-, 16- and 32-bit) types – block mode (BLT), unaligned (UAT), and address only (ADO).

VMERAM-EC1–Providing from 2 to 64 MB in a single slot, the VMERAM-EC1 is the unsurpassed open-architecture solution. The enhanced EDC chip set supports Clearpoint's exclusive 'extra bit' technology. If the VMERAM-EC1 detects 16 single-bit errors in a location, the board automatically replaces the bad DRAM with the on-board spare DRAM. Registers in the chip set monitor the error count and re-map the array to include the new location.

VMERAM–VMERAM is the low-cost alternative for EDC memory, with pricing comparable to parity memory. The VMERAM features Clearpoint's original proprietary EDC chip set, and stands as the only VME Laboratories-certified memory board available. The VMERAM insures high reliability by correcting and removing bad data from the DRAM and replacing it with the correct data. The VMERAM is available in 2 to 16 MB densities.

VSBRAM-EC1–The VSBRAM-EC1, available in densities of 2 to 64 MB, offers true dual-porting and data transfers between the VMEbus and VSB subsystem bus. 64-bit data caches make simultaneous transfers a reality. Designed with the enhanced EDC chip set, VSBRAM-EC1 also features automatic bad-bit replacement. (See the description of VMERAM-EC1 for details.) VMERAM-EC1 is compatible with VSB subsystem bus specification Rev. C, and VMEbus specification Rev. C.1.

VERSARAM–The VERSARAM shows Clearpoint's commitment to advanced technology for the VERSAbus. Available in 1 to 16 MB densities, the VERSARAM includes special-order "ruggedized" boards.

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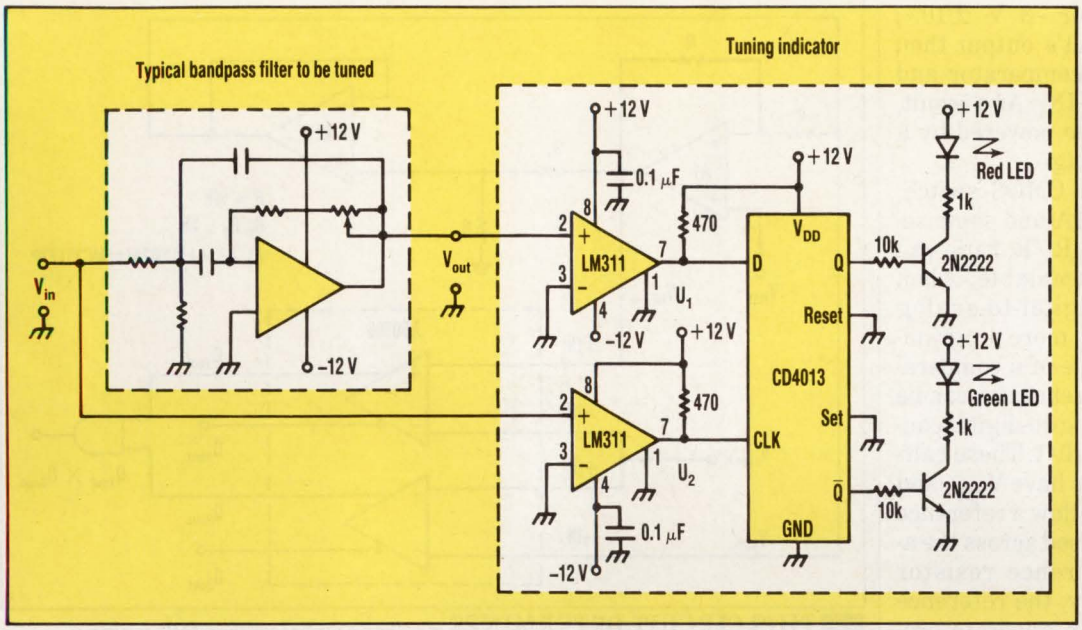


2. WHEN F_o is less than F_{in}, logic 1's are latched at the output of comparator U1 and the red LED lights. The green LED lights when F_O is greater than F_{IN} and logs are latched at U1's output. When F_O equals F_{IN}, both LEDs flicker.

quencies up to 128 kHz and the tuning indication was found to be better than 0.1%. The tuning indication is valid for all sine-wave input frequencies. Though the indication for square and triangular wave inputs are misleading for a few cycles around the subharmonics of f_O, the tuning indication is better than 0.1% at f_O. Hence, this indicator is useful for tuning the filters that convert the square or triangular inputs to sine waves.

The waveforms shown and LED indications mentioned are for inverting types of bandpass filters. For the noninverting bandpass filters, the two LEDs should be interchanged.□

CIRCLE 523

WINDOW COMPARATOR TRACKS VOLTAGE

JOHN WYNNE
Analog Devices, One Technology Way, P.O. Box 9106,
Norwood, MA 02062; (617) 329-4700.

In many applications, determining when a signal's voltage level falls within or outside a particular voltage range is essential. Automatic test equipment (ATE), communication receivers, and other equipment all require this type of information. To get this data, a simple tracking window comparator can be built that combines high speed, TTL compatibility, and wide versatility *(see the figure)*.

Op amps A1 and A2 form an implicit feedback circuit that accepts a positive input reference voltage (V_{REF}) and generates two positive reference voltages, V_{REF+} and V_{REF-}. The two generated voltages are equally spaced above and below the original input reference level. They're used as the upper and lower threshold voltages by the AD9698 dual TTL comparator to establish a window for the signal. When the signal resides inside the window, the AND gate's output is high. When the signal is outside the window, the output is low. An indication of a signal above or below the reference levels can be monitored at the comparators' complementary outputs.

$\overline{Q_{1\,out}} = 1$ when $V_{signal} > V_{REF+}$.

$Q_{1\,out} \times Q_{2\,out} = 1$ when $V_{REF-} < V_{signal} < V_{REF+}$.

$\overline{Q_{2\,out}} = 1$ when $V_{signal} < V_{REF-}$.

The window's width is determined by the ratio of R_1 to R_2. It's value is a fixed percentage of the input reference voltage, and stays the same percentage independent of the reference voltage's actual value. Consequently, the window tracks the reference value and can therefore be placed around an expected signal level of interest. If the width of the window, V_{window}, equals the difference between the threshold levels,

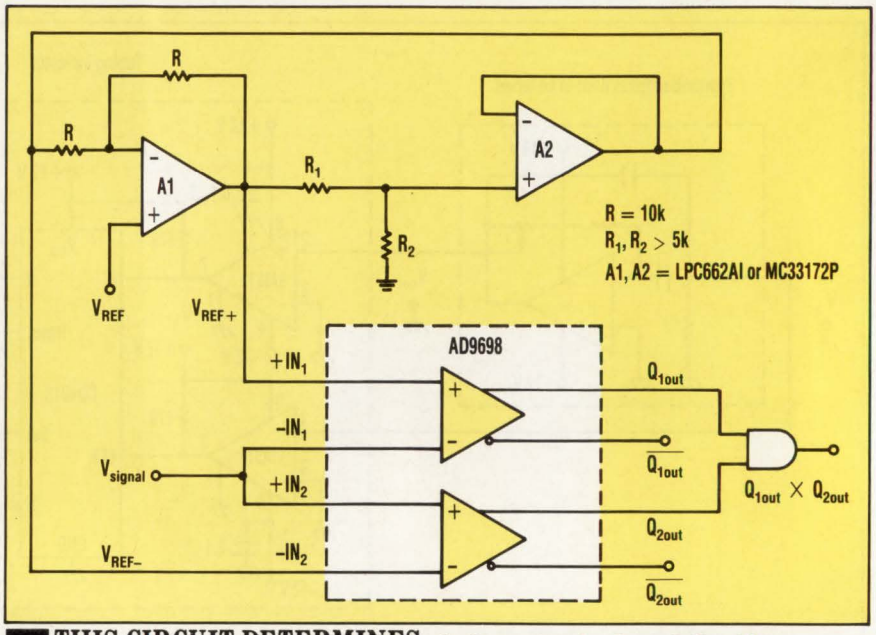
$V_{window} = V_{REF+} - V_{REF-}$. Then
$V_{window} = 2V_{REF}/[1 + 2(R_2/R_1)]$,
$V_{REF+} = V_{REF} + V_{window}/2$, and
$V_{REF-} = V_{REF} - V_{window}/2$.

For example, assume that a signal level to be monitored is valid if it's between 2.7 and 3.3 V, or 3.0 V ±10%. The required window is would be 0.6-V wide with V_{REF} equal to 3.0 V. The required ratio of R_2/R_1 is found by solving the equation containing that ratio. In this case, $R_2/R_1 = 4.5$, $V_{REF+} = 3.3$ V, and $V_{REF-} = 2.7$ V. To monitor a different voltage—for instance, 2.0 V ±10%—just change V_{REF} to 2.0 V. For a different tolerance, change the R_2/R_1 ratio. Note that the circuit only requires a single supply.

The circuit can also monitor negative voltages. But, because V_{REF+} must always be more positive than V_{REF-}, the connections must be

changed. To monitor –3 V ±10%, V_{REF} is now –3 V. A1's output then drives $-IN_2$ of the comparator and A2's output drives $+IN_1$. As a result, the op amps must be powered by a negative supply voltage.

By using a quad CMOS switch, such as the ADG201A and some selected resistors, the R_2/R_1 ratio can be digitally programmable. Also, adding a CMOS digital-to-analog converter gives even more programmable ratios. In place of a comparator, the V_{REF+}-V_{REF-} generator can be used with such analog-to-digital converters as the AD7820/1. These half-flash 8-bit converters have V_{REF+} and V_{REF-} inputs, which allow a reference voltage to be impressed across the a-d converter's reference resistor string. Consequently, the reference generator circuit can generate programmable ratiometric levels to effectively increase the a-d converter's resolution.□



THIS CIRCUIT DETERMINES whether a signal voltage falls within a predetermined window around a reference voltage. If the output of the AND gate is high, then the signal falls within the range. The $\overline{Q_{1\,out}}$ and $\overline{Q_{2\,out}}$ outputs can determine whether the voltage is above or below the specified reference levels.

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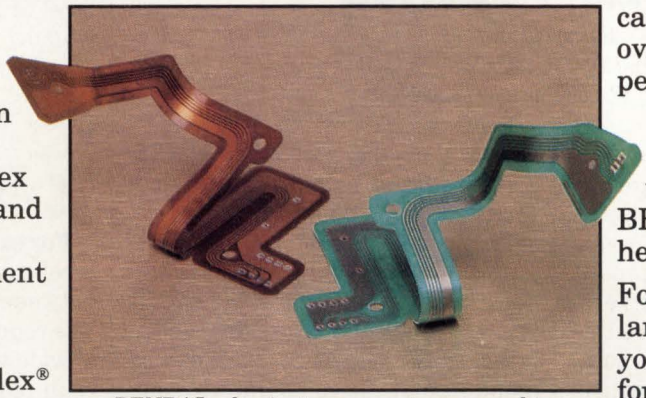

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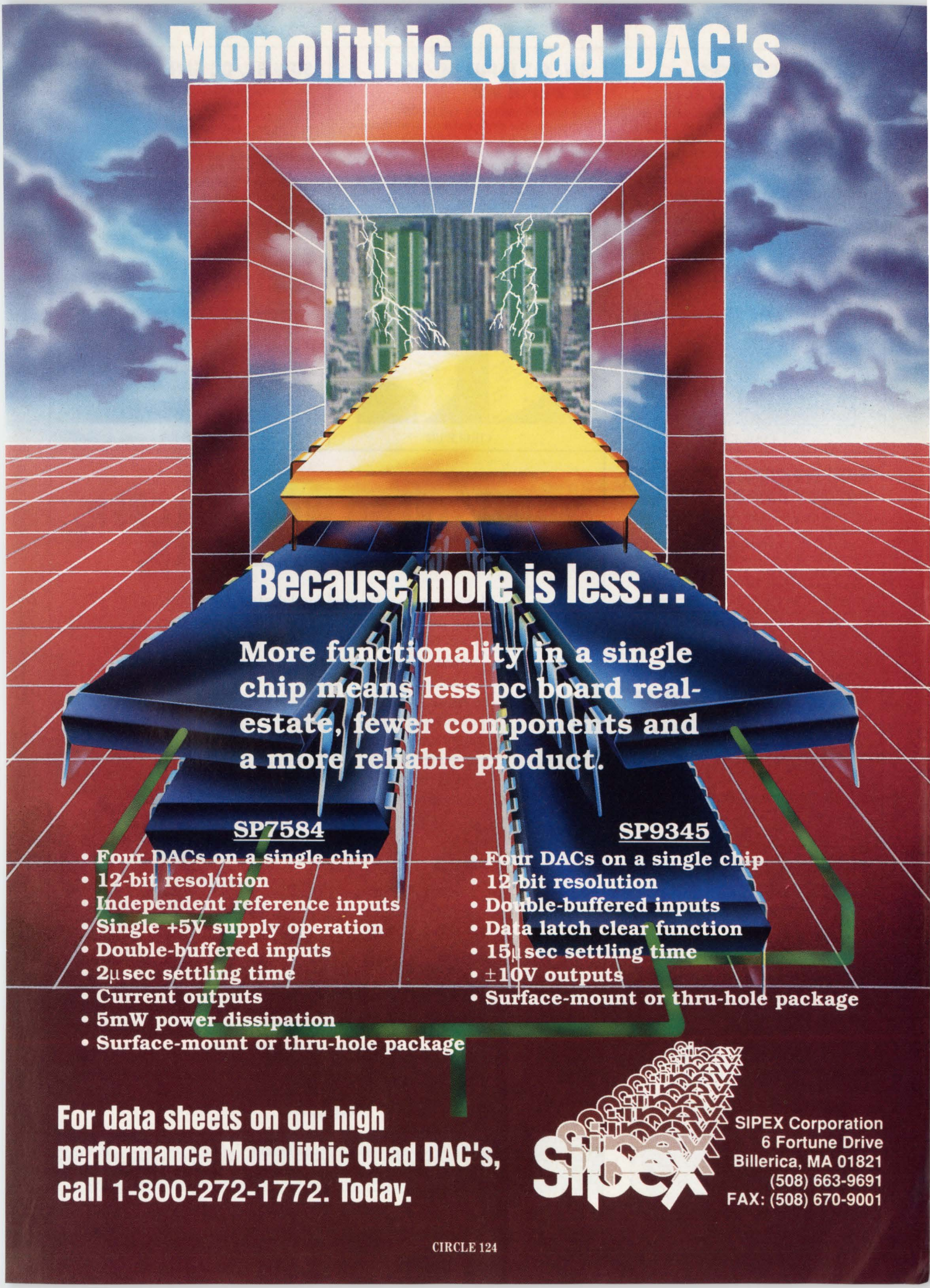
CIRCLE 107

Monolithic Quad DAC's



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NEW DC/DC OFFERS 10:1 INPUT, 80...720W

The PSK Series offers nine single outputs of 5...42VDC at 16...20A (25A for 5V) with input ranges as wide as 8...80VDC and efficiencies from 82...94%. Standard features include input filtering, remote on/off, true current sharing, remote sense, and adjustable output from 0...110% of nominal. Line and load regulation is 0.5%, output ripple is as low as 30mVpp, and load transient recovery is 40µS. Available options include in-rush current limiting, output crowbar for OVP, and an output potentiometer. Units are suitable for chassis or 3U rack-mount. For more information, contact MELCHER at (508)881-4715 or FAX(508)879-8669

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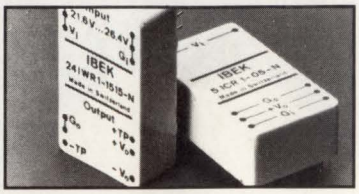

CIRCLE 132

50W DC/DC GIVES 5:1 INPUT

The M family (AM,BM,CM,DM,EM) of DC/DC converters provides up to 3 outputs at 50W with an input range of 5:1 (8...35V, 14...70, 28...140, 44...220, and 67...385VDC). They are suitable for any battery powered, telecommunication, SCADA, or transit system. Each unit offers protection against severe transients, continuous open and short circuits, input and output overvoltages, and 2500V isolation. Mechanically, each product is protected from shock and vibration per MIL STD 810D and offers an operating temperature range of -40...95°C (case) to withstand the most severe environments. For more information, contact MELCHER at (508)881-4715 or FAX (508)879-8669.

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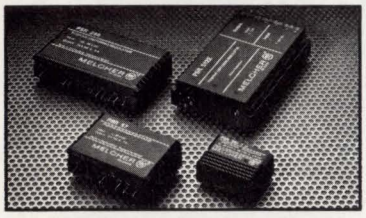
The PSR family is ideally suited to battery powered systems with its 90% conversion efficiency, ultra-wide input range (8...80 for 5V) and small size. Available in single outputs of 5,12,15,24 and 36V at 2.5,4,8, and 10A, these units can work from 12,24,36,48 or 60V batteries and provide complete protection against short and open circuits as well as step-load changes and harsh environments. They are suitable for PCB, chassis or rack-mounting and many options are available. For more information, contact MELCHER at (508)881-4715 or FAX(508)879-8669.



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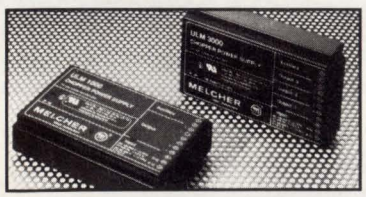
The 50 watt LM Series accepts any input voltage from 85...264VAC and provides up to 3 independently regulated outputs over the entire temperature range of -40...71° C (ambient). Standard features include remote on/off, short/open circuit protection, line and load regulation <1%, and output ripple below 70mV. The unit can be mounted in a 3U rack or chassis and meets MIL STD 810D for shock, bump, vibration and humidity. Many options are available including low leakage currents for medical apparatus (IEC601.1/UL544). For more information, contact MELCHER at (508)881-4715 or FAX(508)879-8669.



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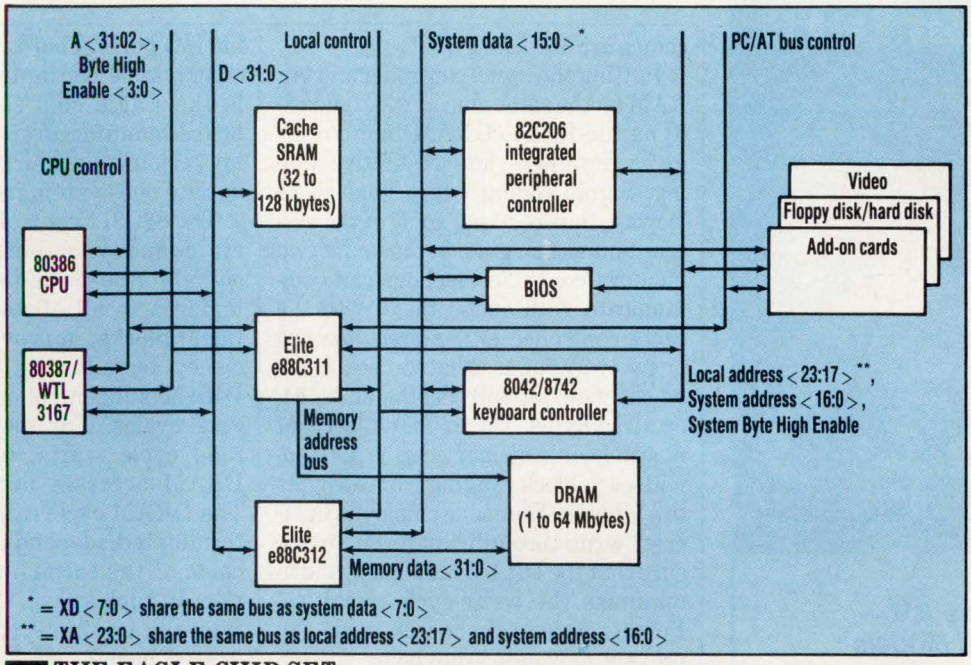

THE EAGLE CHIP SET reduces PC motherboard logic to less than 25 chips by merging the cache controller and cache tag RAM into the logic chip. Not only is the chip count cut down, but system efficiency is also improved because DRAM and cache access cycles can be overlapped.

PC CHIP SET EASES DESIGN OF CACHE-BASED COMPUTERS

DAVE BURSKY

Currently, designers of PC-clone hardware can choose from over two dozen chip sets that allow systems to be built at a small cost with minimum functionality, such as the base-line PC/AT-class motherboard. However, as system CPUs get more powerful, the base-level of system features must increase so that users can take advantage of the enhanced performance with minimal additional hardware. This vision led designers at Elite Microelectronics Inc. to define the Eagle chip set, a pair of chips that enables system designers to build cache-based motherboards operating at clock speeds of up to 33 MHz.

With the Eagle chip set, an entire 80386DX-based PC motherboard can be built with as few as 25 components. The only other devices needed are the CPU, BIOS memory, keyboard controller, an integrated peripheral controller (such as the widely available 82C206), and a few TTL chips *(see the figure)*. To round out the motherboard, just the cache RAMs and the main dynamic-RAM-based memory must be added. To make that possible, the two chips in the Eagle chip set include one key function that's usually optional chips in previous systems, such as a cache controller. The e88C311 is the main system logic chip and comes in a 184-lead plastic quad-sided flat package (PQFP). The e88C312 handles memory-transfer operations and

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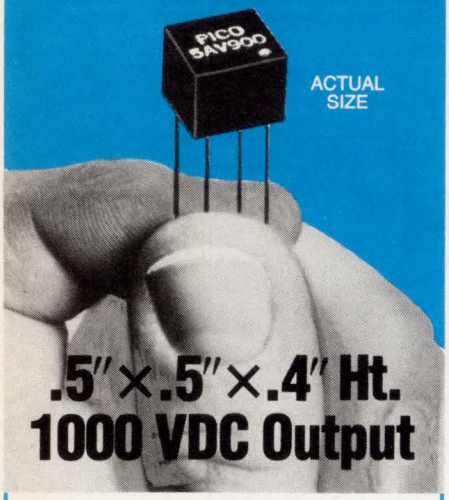

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CIRCLE 100

CACHE-BASED PC MOTHERBOARD CHIP SET

comes in a 160-lead PQFP.

Putting the cache controller and tag RAM on the same chip as the standard dynamic-RAM (DRAM) controller gives designers less restrictive timing. Signal timing edges have more leeway, thus relaxing some of the system timing margins, because the two memory controller sections can communicate with each other. With the cache controller, either direct-mapped or two-way set-associative caches can be constructed with depths of 32, 64, or 128 kbytes. Up to four blocks of noncacheable memory can be defined, with each block ranging from 4 kbytes to 4 Mbytes. The cache employs a buffered write-through approach to ensure that the DRAM is updated, and to minimize the write-cycle penalties. Furthermore, a cache-lock mode can prevent new data from being written into the cache when frequently used program code is held in the cache.

The companion DRAM controller can address up to 64 Mbytes of system memory and DRAMs with capacities of 256 kbits and 1 or 4 Mbits. Both page and page-interleaved operating modes are possible. Three refresh schemes can keep data in the RAMs—hidden, burst, and PC/AT style. To ensure fast system operation at minimal cost, up to 256 kbytes of the DRAM are able to serve as shadow memory for BIOS information usually held in slow EPROMs. A sophisticated memory remapping technique allows designers to maximize the use of installed physical memory. Finally, the controller achieves zero-wait-state operation for both pipelined and nonpipelined cache misses or page hits.

The chip set has several similarities to other commercially available motherboard logic chips. It supports both the Intel 80387 and Weitek WTL3167 math coprocessors and provides the Fast GateA20 and Fast Reset signals needed for maximum OS/2 performance. Moreover, the chip set supplies a programmable PC/AT bus clock that permits both synchronous and asynchronous operation, and designers can select the system configuration for two serial and one parallel port, and chip-select logic for two software-programmable I/O ports. There are 60 software-controllable configuration registers in the Eagle chip set that motherboard manufacturers can use to set up various configurations to differentiate one system from another.

The 88C311 controller, which generates and synchronizes each control signal for buses and manages the interfaces to all of its internal functional blocks, improves system efficiency by allowing the cache and DRAM subcontrollers to share access cycles. For instance, when a read cycle starts, both cache and DRAM accesses occur in parallel. The DRAM cycle can continue or be terminated, depending on the outcome of the cache hit-or-miss detection. In such a case, the time penalty typically encountered by a nonintegrated cache and DRAM architecture is reduced. This is because the DRAM need not wait for the hit/miss signal from the tag-RAM directory to start the DRAM operation.

Along with the DRAM and cache control blocks, the 88C311 includes reset and shutdown logic; CPU, local memory, cache, and AT-bus state machines; arbitration logic; address buffers and latches; and configuration registers. The 88C312, which controls the interface between the CPU data bus and the various board-level buses (AT-bus, local system bus, memory data bus, ROM interface, and so on), also implements the byte-alignment and byte-swapping logic needed when data transfers occur between boards of different data widths. Parity logic included on the 88C312 generates and writes parity into the DRAM array during main-memory write cycles.□

PRICE AND AVAILABILTY

The Eagle chip set sells for $168 in lots of 1000; samples and production quantities are available immediately. Evaluation boards are also available.

Elite Microelectronics Inc., 711 Charcot Ave., San Jose, CA 95131; Arun Kumar, (408) 943-0500. CIRCLE 516

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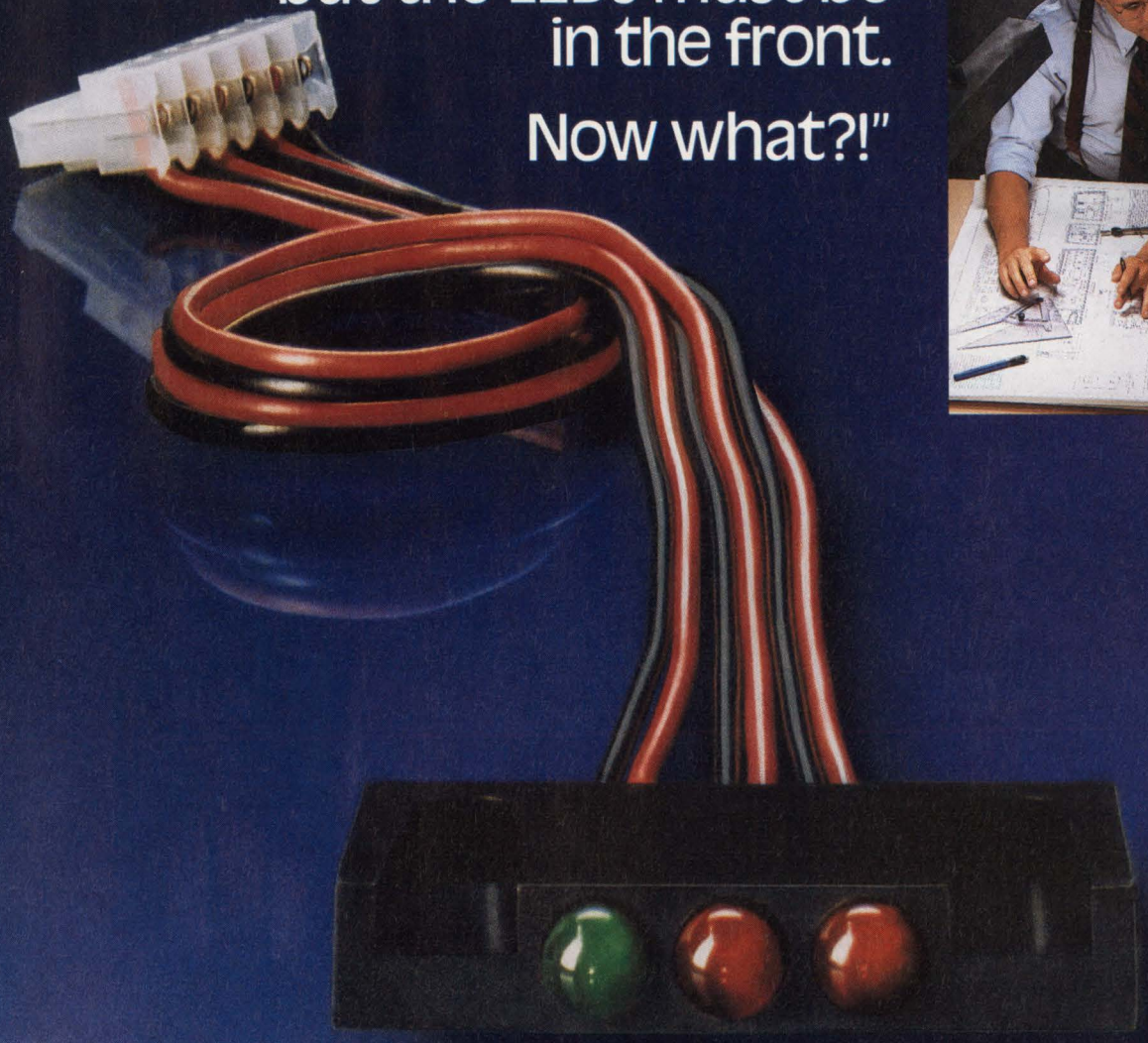

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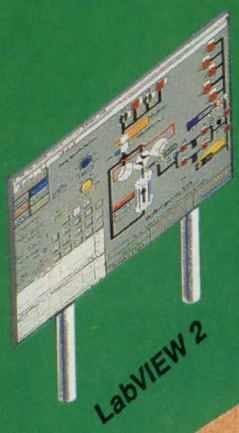

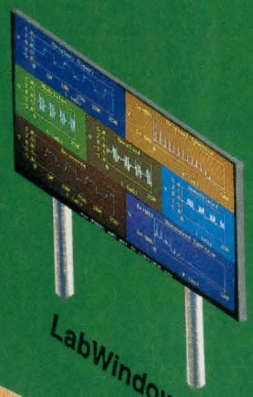

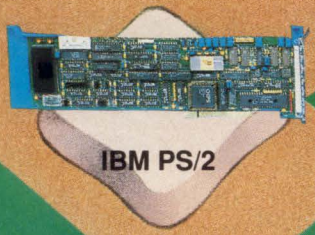

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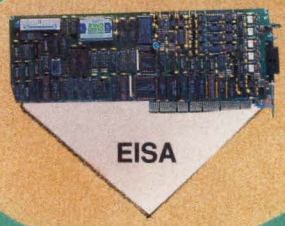

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Lab-SE	Macintosh SE	8	125k	8	2	24	3	–
AT-MIO-16	PC/AT	16	100k	12	2	8	3	√
MC-MIO-16	IBM PS/2	16	100k	12	2	8	3	√
NB-MIO-16X	Macintosh II	16	55k	16	2	8	3	√
NB-A2000	Macintosh II	4	1M	12	–	–	–	√
EISA-A2000	EISA	4	1M	12	–	–	–	√

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FRANK GOODENOUGH

Move over 0820 8-bit 1.5-μs ADC, because five new 10-bit devices have arrived. The venerable, standard 8-bit ADC, with its low-cost half-flash architecture in CMOS, has prevailed for over eight years. But overwhelming demand called for 10-bit ADCs with similar performance and price, for applications as diverse as disk drives and mobile radio. Unlike their 8-bit predecessor, several of the new 10-bit devices have Nyquist rates commensurate with their throughput rates thanks to a high-speed sampling capability. And all but one can sample 100-kHz sine waves to 9-bit accuracy.

Two of the converters, the ADC10061 and the ADC1061, are from National Semiconductor. The remaining three—the MAX151, ML2271 and MP7695—are from Maxim Integrated Products, Micro Linear, and Micro Power Systems, respectively. Minimum conversion times for the five run 0.8, 1.8, 2.5, 1.45, and 0.5 μs, respectively. Micro Linear recently announced a drop-in for the 0820, which can sample a 250-kHz sine wave to 8-bit accuracy *(*ELECTRONIC DESIGN, *April 12, 1989, p. 28 and 212).*

Each ADC has its own set of features and specifications *(see the table).* All employ two-step architectures, except for the ML2271, which uses three steps. In addition, similar to its recent 8-bit sibling and unlike the other four, the ML2271 employs digital error correction. The

10-BIT ADC SPECIFICATIONS

Specifications[1]	MAX151A	ML2271B	MP7695	ADC10061B	ADC1061
1) Conversion time (μs)	2.5	1.45	0.5	0.9	1.8
2) Maximum input frequency for 10-bit performance (kHz)	40 t	300 t	10 t		60 t
3) Differential nonlinearity			(all, no missing codes at dc)		
4) Integral nonlinearity (±LSB)	na	1/2	1.25	1.1	1.5
5) Total unadjusted error (±LSB)	1	3/4	na	1.5	2
6) Signal-to-noise ratio (dB/bits)	55/8.8	60/9.7 t	na	60/9.4 t	na
7) (f_s/f_{in}(kHz))	40/300	150/600		512/160	
8) Total harmonic distortion (-dB/bits)	60/9.7	60/9.7 t	na	0.08% t/na	na
9) (f_s/f_{in} (kHz))	40/300	150/600		512/160	
10) Intermodulation distortion (dB)	na	-60 t	na	na	na
11) (f_s/f_{ina},f_{inb}(kHz))		600/150, 148			
12) Full power bandwidth (kHz)	5 MHz t	na	na		na
13) Slew rate (V/μs)	na	4.7	na		2.5
14) Supply voltage, current (V, mA)	±5, 45	5, 32 mA	5, 6 t	5, 47	5, 47
15) Package(s) and features (see footnotes)	2,3,4	5,6,9	2	5, 6, 7, 8	5
16) Cost each in 100s	$16.66	$17.00	$24.95	$17.90	$11.90

Footnotes: 1)All specifications minimums/maximums over temperature unless noted otherwise. t=typical, na=not available. 2)24-pin DIP 3)24-pin, wide-body SOIC. 4)Reference. 5)20-pin, DIP. 6)20-pin, wide-body SOIC. 7)ADC10062, two inputs, 24-pin DIP and SOIC. 8)ADC10064, four inputs, 28-pin DIP and SOIC. 9) A "C" grade with an INL of ±1 LSB and a total unadjusted error of ±1.5 LSB goes for $11.80 each.

SUB-2.5-μS-CONVERSION-TIME, 10-BIT, IC ADCS

MAX151, on the other hand, laser-trims thin-film resistors in the flash ladders to achieve 10-bit accuracy.

All five CMOS ADCs guarantee "no missing codes" over their operating-temperature ranges. Each employs the autozeroed comparators that use switched-capacitor techniques, which are virtually mandatory for CMOS ADCs. The architecture of all but the MP7695 take full advantage of these circuits' inherent ability to sample fast-changing waveforms. However, this sampling ability doesn't come free. The ADCs' input circuits—the array of comparators forming the flash converters—look to the input signal like a rapidly-changing (at the sampling rate) capacitance. Therefore, if operated at high sampling rates, the analog input must be driven from a low-impedance source at high-frequencies.

The MAX151 is the only one with an on-chip reference—a buried Zener circuit with a drift of 60 ppm/°C. It's also the only device that needs both plus and minus 5-V supplies; the others require only +5 V. However, it can handle a 0-to-10-V input or ±5 V, while the others are limited to 0 to 5 V. The MP7695 is the fastest of the group, converting in 0.5 μs, a function of its 2-μm, molybdenum-gate (rather than poly-gate) CMOS process. It's also the lowest in power consumption, typically just 25 mW. The others consume about ten times that, from 180 mW for the ML2271 to 275 mW for the MAX151.

Despite its speed, the MP7695 is limited to sampling signals accurately below 10 kHz or those slewing at less than 2 V/μs. With a high-speed multiplexer on the front end, it's ideal to digitize many slow signals at high speed, particularly in portable equipment.

In their 20-pin DIPs, the ML2271, ADC10061, and ADC1061 have functionally identical pinouts. Therefore, they're theoretically interchangeable. And along with the MAX151, they interface with most microprocessors easily—their parallel three-state outputs appear as memory locations or I/O ports. In addition, while in larger packages, National ADC's 10062 and 10064 versions have two and four input channels, respectively, and an internal multiplexer *(see table footnotes)*. Channels are selected through one- or two-bit input words for the two- or four-channel device, respectively. Both converters sport a speed-up pin. Putting a resistor between that pin and ground halves conversion time.

The dynamic specifications of these converters represent a major difference between these chips and their 8-bit forerunners. When handling ac signals, particularly in digital-signal-processing applications, the MAX151, ML2271, and ADC1006 take full advantage of their sampling ability. As a result, they're specified dynamically as well as statically, providing values for signal-to-noise ratio, total harmonic distortion, and intermodulation distortion specifications *(see the table, again)*. Also, the MAX151 specifies a full-power bandwidth of 5 MHz.□

PRICE AND AVAILABILTY

Versions of the MAX151 and MP7695 are only available for the commercial-temperature range. Grades of the ADC1061 and ADC10061 can be had for both the extended-industrial and military temperature ranges. ML2271 grades are available for commercial, extended-industrial, and military temperature ranges. The devices specified in the table are for the highest-performance and lowest-temperature grades. Prices are given in the table.

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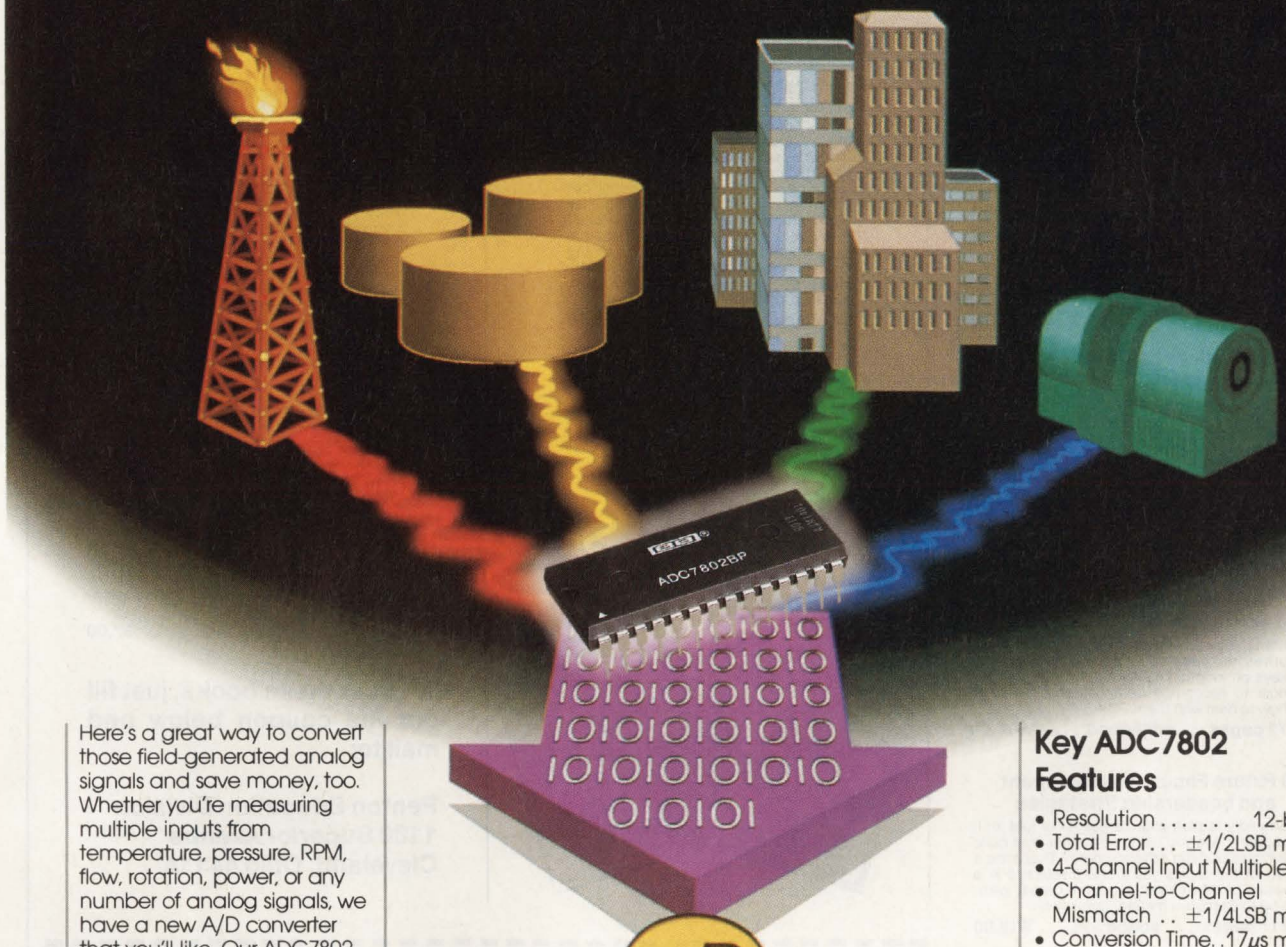

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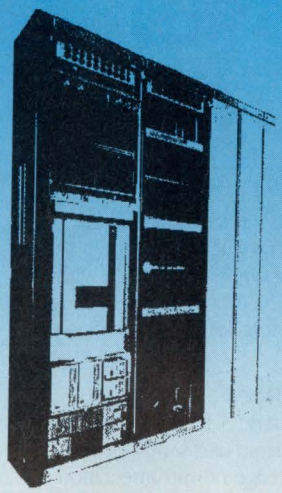

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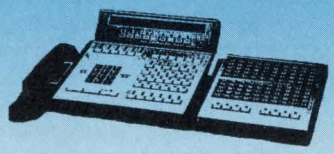

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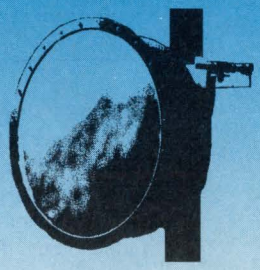

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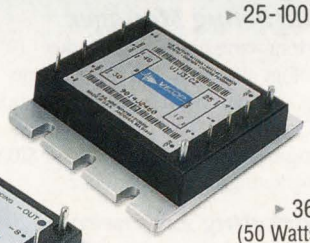

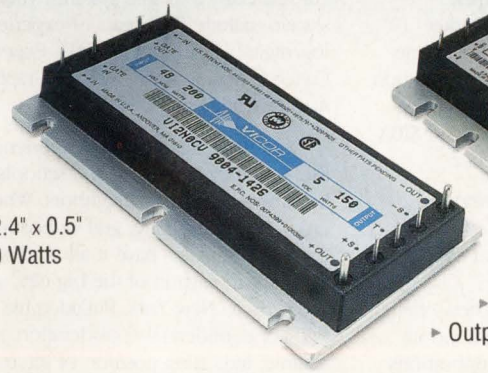

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SALARY SURVEY

PAY INCREASES ARE HARDER TO COME BY THIS YEAR

BY SHERRIE VAN TYLE

Engineers are making more money than ever. But this year's salary picture is far from rosy. Raises earned in the past 12 months were skimpier than in the preceding 12-month period. And better than one in three engineers thinks that his salary has hit a plateau. Most engineers also say their salaries are comparable to those of others in the same field.

These findings come from a survey of 1500 *Electronic Design* readers in August. Here's the picture that emerges from tabulating the survey's 354 responses: the average reader is male, 39.7 years old, and makes $51,646 a year. He has 13.7 years of engineering experience. His salary increased 6.08% in the past 12 months compared with 6.73% in the previous 12 months. With the title of design engineer, he works for a company that does $380 million worth of business annually. On the average, he supervises three other engineers.

With almost 14 years in the profession, the average engineer has plenty to say about career issues—especially salary plateaus, the survey finds. Entry-level salaries for engineering graduates are often higher than for other professionals. After a decade in the workforce, though, the initial salary advantage erodes. And with an equal years number of years in their professions, engineers tend to make less than lawyers, doctors, and scientists.

As one reader put it, "Due to the high level of continuing education required, salary ceilings for engineers are having a negative impact on morale and productivity, causing many engineers to leave the technical field for the higher paid management and business fields."

About 38% of the readers surveyed believe that their salary has hit a ceiling. These readers fixed that plateau at an average of $59,492.

Of these respondents, 65 commented on salary plateaus. One engineer remarked, "We would like to delude ourselves that ceilings, like age discrimination, don't exist. They both do, unfortunately."

Salary ceilings, some readers pointed out, could push some engineers out of the profession. Ceiling pressure hits older engineers hardest. And one quarter of readers surveyed (24%) have 21 or more years of engineering experience. In the words of one engineer: "I'm worried that I will hit [a salary ceiling] soon. It may lead to a career change." Another engineer wrote, "Salary ceilings force older, experienced engineers out of the field. It is a nervous, insecure feeling being at, or near the ceiling." Along similar lines, another engineer warned, "If you're over 45, get out of the profession."

Still, 62% of the engineers surveyed didn't feel their salaries have hit a ceiling. But just a handful commented. One reader attributed a lack of salary limits to his industry: "Salary ceilings are not a problem for good engineers in the disk-drive industry." For another reader, merit helps lift salary ceilings: "I don't believe ceilings exist for good engineers."

Questions of merit aside, average raises shrank from 6.73% for the previous 12-month period to 6.08% for the most recent 12 months. That 0.65% difference, on a $50,000 salary,

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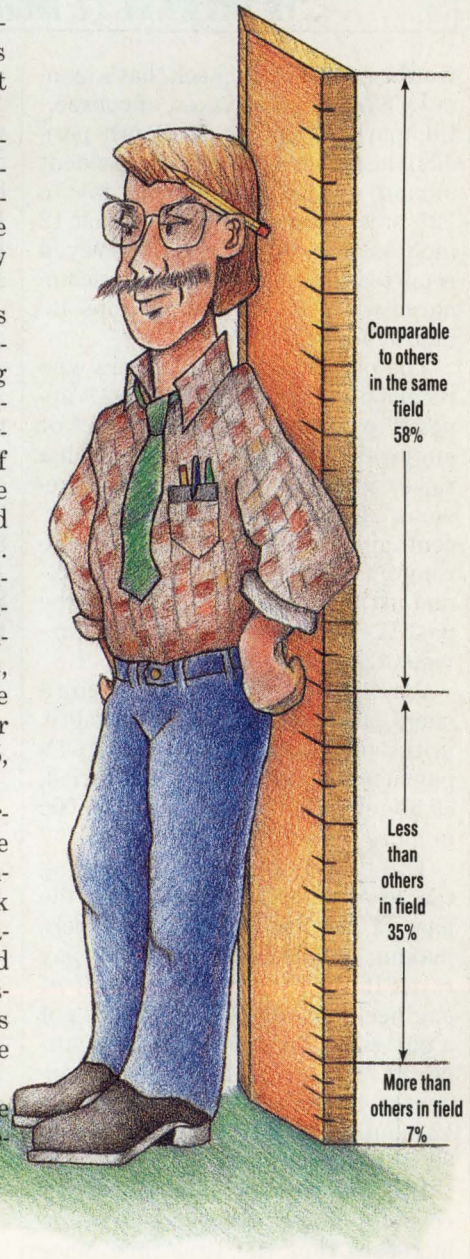
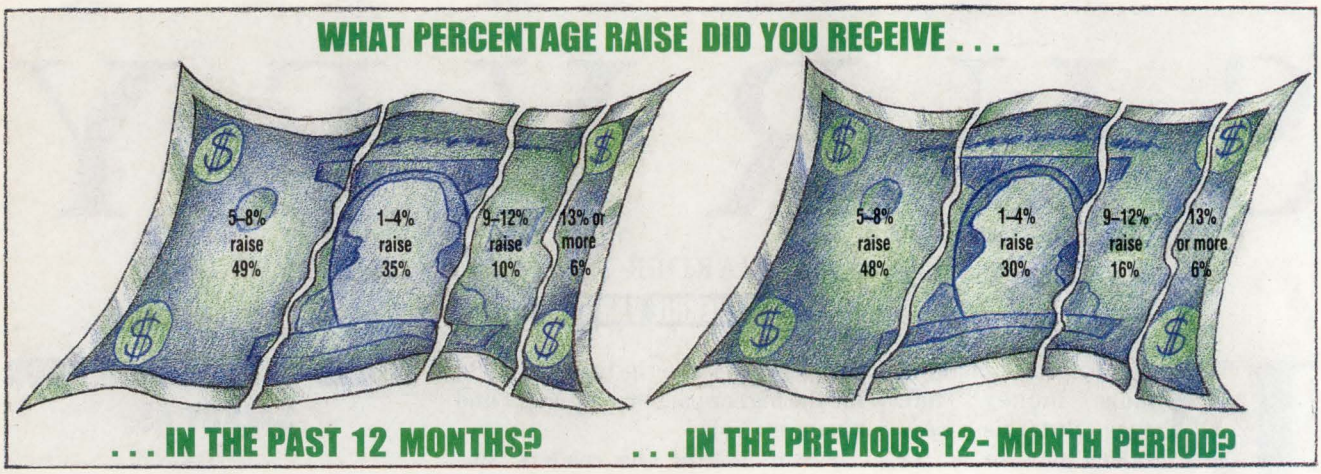




would mean a raise check that's leaner by $325—before taxes, of course. Comparing the two 12-month periods, the smaller raise is most evident among engineers receiving 9% to 12% salary increases. In the past 12 months, 9.7% of engineers surveyed reported that range of increase compared with 16% for the previous 12-month period.

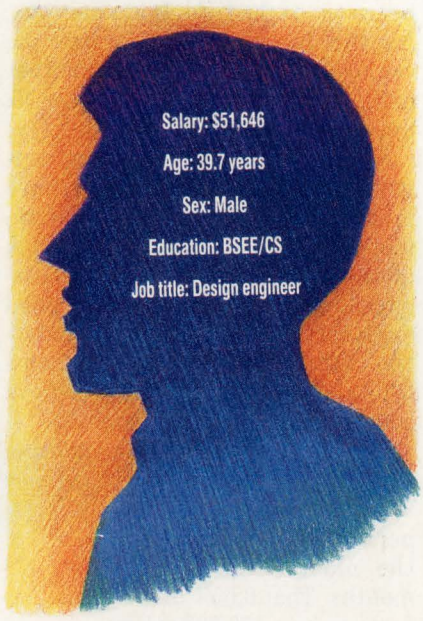
The percentage of engineers who received scant raises of 1% to 4% appears to be on the rise. About 35% of engineers surveyed reported such a raise compared with 30% for the previous 12-month period. Still, the percentage of engineers receiving mid-range pay increases of 5% to 8% remained about the same: 48.6% for the past 12 months vs. 48.3% for the previous 12-month period.

Among the highest paid engineers, those making $60,000 or more, in the past 12 months, 79.1% got a pay increase. In the previous period, 89.3% of engineers making $60,000 or more got a raise.

This trend was reversed among the lowest paid engineers. In the past 12 months, 76.9% of engineers making $40,000 or less got a pay raise. In the previous period, 68% of engineers making $40,000 or less got a pay raise. Among all readers surveyed, the percentage of respondents who got raises in the previous 12 months was 80.4% compared with 80.7% for the preceding period.

Defense cutbacks and a slowing economy augur even smaller wage increases. For the first time since 1980, salary increases in 1991 may trail inflation, reports *The Wall Street Journal*. For instance, a survey of 3,000 companies shows an average 5.4% pay raise in 1991, down a bit from an average of 5.5% in 1990. In comparison, the Consumer Price Index rose 4.4% in 1988; 4.6% in 1989; and 5.9% in 1990 (through August)

For the most part, engineers with many years of experience clustered at the top of the salary range. For instance, among those surveyed making $70,000 or more, 44% had 21 or more years of experience. Of the engineers making $65,000 to $69,999, 38% had 21 years in the field, with another third having 17 to 20 years. And among engineers making $60,000 to $64,999, 38% had 21 or more years of experience while 24% had 17 to 20 years in the field.



One way to break through the salary ceiling is to become a manager, said survey respondents. One engineer noted, "It is difficult to advance—i. e., have increased recognition and salary—while staying in a strictly technical career track." Another reader said, "Non-management engineers have a definite top-end salary." Along similar lines, another reader wrote, "The engineering salary levels off after about $40,000, but the manager's path goes to $60,000." Another respondent set the plateau higher—"For a design engineer, it's about $50,000 without being a manager." And the survey bore out this finding—the top of the salary ladder has many more managers than in the lower salary rungs. Among highly paid engineers, those making upward of $70,000, 31% supervise 10 or more engineers. Another 23% of these engineers supervise 6 to 10 engineers. And 29% supervise one to five people.

Nearly two-thirds of engineers making $45,000 to $49,999 aren't supervisors. The salary edge for managers starts to show up in the $50,000 to $54,999 range—here, 46% of respondents supervise one to five engineers while 43% aren't managers.

Higher salaries may propel some engineers to move into management—but not all of them are happy about it. And several engineers pointed to lack of career advancement for engineers who stay on the technical track:

• "There is not enough career growth

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potential for an engineer who remains in a technical capacity as opposed to an engineering management path."

- "It seems that once an engineer reaches the salary ceiling, he must move into management. I enjoy engineering."
- "You must get into management to increase your salary above the $60,000 or $70,000 range, which may be a problem if one really enjoys design work."
- "Companies need to provide more non-management career paths for engineers."
- "The best engineers make less than mediocre managers. It is unfortunate that engineers who create market opportunities for their employers must quit engineering to progress in salary."
- "It is a shame that the management side tends to earn more for what I believe is less skill."
- "I've never seen a 2:1 difference in pay at the same level, but I have seen 2:1 differences in quality and productivity. Ceilings are a crutch for uncomprehending managers."
- "It seems that the farther away one works from the 'hands-on' of a product, the more money one earns. For example, engineers design and develop the hardware/software and mechanical aspects of the product. However, the marketing, sales, and accounting people seem to draw bigger paychecks. Engineering must start paying more to keep engineers in the important design role."

Updating The Resume

Besides moving into management, another way to avoid hitting salary or career plateaus is to change jobs. Says one respondent, "I recently got a $6,000 salary increase by quitting the company I worked for for 11 years and going elsewhere. Companies always seem more willing to pay higher wages to hire people than they are to keep them."

Some job changes aren't voluntary, of course. One respondent said, "Engineering is one of the few professions where you can have too much experience. Most companies hire few (or no) experienced engineers to eliminate highly paid engineers."

Another singled out foreign owned corporations as having "generally low ceilings." Yet another engineer wrote that "supply and demand dictates supply. I see rollbacks in salary because of excess supply."

Another way to lift salary ceilings is to link salaries to profits engineers generate for the company. Along these lines, one respondent said, "I feel that engineers as a whole need to organize and push for salaries commensurate with the profit-making potential of the products they create—including but not limited to guaranteed royalties and residuals enjoyed by artists and writers."

A reader wrote, "I think engineers should be given a small percentage of the profits they generate through the products they create." Another said, "Engineers should be paid more directly for their proven abilities rather than their credentials. My efforts have a tremendous effect on company profitability, yet I am paid considerably less than degreed engineers of comparable experience."

Some engineers surveyed had no complaints about their salaries. In the words of one engineer: "I'm not concerned about money. If they knew how much fun I have at work, they would likely charge me for the privilege of working here." One respondent said, "For the work that I do, I am ridiculously overpaid."

For some, other career concerns overshadowed salary issues. For example, one engineer said, "I have accepted a lower salary to obtain a position I believe I have learned more from." Another wrote, "The more I learn about our own [U. S.] engineering history and the present condition of foreign engineers, the more convinced I am that most of us may be overpaid for what we do."

A Matter Of Degree

Yet another way to break through the salary ceiling for engineers is to earn an advanced degree. And the survey showed a predictable correlation between post-graduate work and higher salaries. One-third of those surveyed had BSEE/CS degrees; nearly 11% have taken post-graduate engineering courses; 9% have an MA/MS degree; about 17% have an MSEE/CS degree; and nearly 4% have a doctorate. In contrast, engineers with BSEE degrees make up 44% of those in the $40,000 to $44,999 range and 48% of those in the $45,000 to $49,999 range. Among engineers earning $60,000 to $64,499, 17% have a doctorate, 24% have master's degrees, 17% have done post-graduate work, and 28% have a BSEE/CS.

Most survey respondents thought their salaries are on a par with others in the field. Overall, 57.6% of respondents felt their salary was comparable to others in the same field with 35% saying their salary was lower; just 7% felt they earned more. Not suprisingly, most of respondents making less than $35,000 described their salary as being less than others in the same field.

A turning point comes at about $35,000; respondents at that salary responded more positively—62% of those in the $35,000 to $39,999 salary believe that they are paid comparably to others in the same field. Among engineers making $40,000 to $44,999, the belief that one is being paid comparably drops to 45.8%, with 50.0% feeling that they are paid less than others in the same field.

Of the engineers surveyed, the most common job description is design engineer (17.3%), followed by senior engineer (15.6%), and project engineer (14.5%). The number of respondents involved with computers and peripherals was 45.4%; test and measurement and instruments, 31.4%; military/aerospace, 30.8%; and components and subassemblies, 29.1%; communications equipment, 22.7%; and industrial controls and equipment, 17.1% (total is more than 100% because respondents could indicate more than one category).

Only 11 women participated in the salary survey, accounting for 3% of the respondents. Among engineers employed, women make up about 6% of the workforce. With so few responses from women, no solid conclusions about salary based on gender can be drawn.□

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TEXAS INSTRUMENTS

CUSTOM ICS SHRINK A 1-GHZ SCOPE TO A PORTABLE, AFFORDABLE SIZE

JOHN NOVELLINO

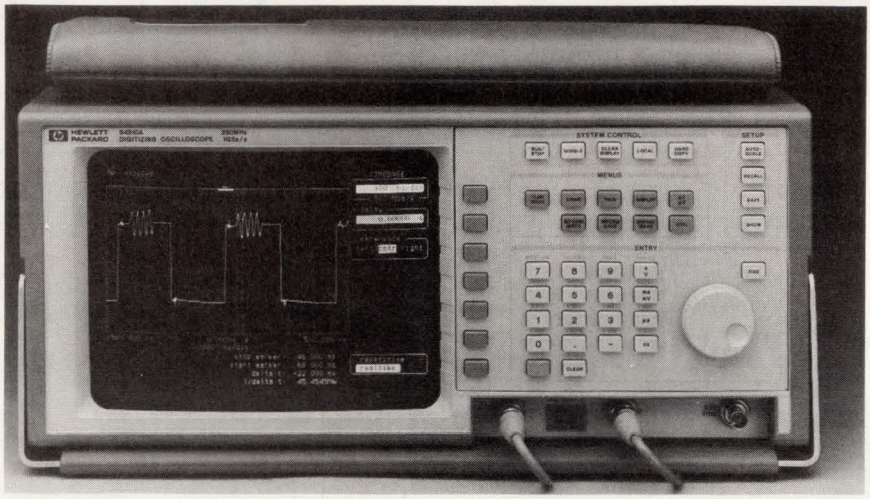
Thanks to a handful of custom ICs, the size and cost of 1-GHz digital oscilloscopes need no longer be intimidating. The HP 54510A packs two channels, each with a 1-Gsample/s digitizing rate and 8-bit vertical resolution, into a portable package 16.75 by 14.3 by 7.65 in. Price is less than $11,000.

The scope has a horizontal (timing) accuracy of 100 ps and a vertical (voltage) accuracy of 1.25% of full scale. Record length is 8 ksamples. In accordance with HP policy, front-end filters limit the one-shot bandwidth to 250 MHz, one-fourth the sample rate, to avoid aliasing.

For high-throughput applications, the HP 54510A uses a segmented-memory scheme called the successive single-shot mode. In this mode, the instrument automatically captures, stores, and labels a waveform, then re-arms the trigger. The scope can capture 300 512-point waveforms at rates up to 400 waveforms per second. When it has captured and stored the specified number of waveforms, the 54510A transfers the data to an external computer.

Each channel has its own flash analog-to-digital converter. These custom bipolar devices were chosen because they offer lower noise, higher vertical accuracy, and better linearity than the charge-coupled devices commonly used in very fast scopes, HP says. Six other custom ICs replace whole boards full of components in memory, time-base, triggering, processing, and other circuitry. The analog-to-digital memory IC, for example, reduces board space for that function by 98% and cost by 50%. And the 25,000-device time-base IC slashes space and cost for that function by 90% and 85%, respectively.

As a result, one board holds all the scope's acquisition and processing circuitry. Overall, the HP 54510A takes up one-tenth the board space that would be needed by conventional circuitry. The drastic reduction in component count should greatly increase reliability, with HP estimating a 30,000-hr. mean-time-between-failure rate. The company provides a three-year warranty.



Instead of a peak-detection circuit for glitch capture, the HP 54510A employs a time-qualified trigger that can grab even one-shot glitches down to 1.75 ns. The trigger specifies a "pattern present less than..." statement. The user selects a time slightly smaller than the nominal length of the pulse being studied.

The instrument's advanced logic triggering, including state triggering, helps designers uncover complex digital problems. For instance, the user can specify a pattern on any two of three inputs, with the third input used as a clock. The qualification may call for a trigger on the rising or falling edge of the clock input, and when the pattern is or is not present, as desired.

Another trigger option is event-delayed mode, in which the user qualifies the trigger by an edge, pattern, time-qualified pattern, or state. The delay can be a number of occurrences of a rising or falling edge of any of the three inputs (channels 1 and 2 and the external trigger). The delay can be from one to 16 million occurrences, and the maximum edge counting rate is 70 MHz. TV triggering is also available.

The HP 54510A contains the features designers have come to count on in digital scopes. Autoscaling sets up the instrument with one keystroke. The unit makes 17 automatic pulse-parameter measurements, including peak-to-peak voltage, pulse width, period, and delay. The results can be displayed as a snapshot, or can be continuously updated, or continuously updated with statistics. In the statistical mode, the display shows the maximum, minimum, average, and most recent values.

Users can choose from two forms of limits testing. They can create waveform templates in a controller and store them in the scope's memory for later recall and comparison against live waveforms. Or they can set numerical limits on any three selected parameters. The scope will compare input waveforms to the preset limits, without the need for an external controller. If a discrepancy occurs, the unit will save the waveform, output the screen to a hard-copy device, or flag a controller.

The HP 54510A sells for $10,950, with availability estimated at 8 weeks after receipt of an order.

Hewlett-Packard Co., Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80901-2197; (800) 752-0900. **CIRCLE 331**

SCSI-To-GPIB Interfaces For Sun-3, VAX 3100

Two IEEE-488 interface kits let users control up to 14 IEEE-488 instruments through the SCSI ports of the Sun-3 or the DEC VAXstation 3100 and MicroVAX 3100 workstations. The GPIB-Sun3-S kit includes the NI-488M multitasking software package, a set of fast, high- and low-level functions that are installed in the operating system as a Unix device driver. Similarly, the GPIB-VAX3100-V kit includes the GPIB11 software, which is installed in the VAX operating system. Both interfaces come with the GPIB-SCSI con-

troller box with a 64-kbyte RAM buffer. This external box is an 8-bit microcomputer that implements the full range of IEEE-488 controller functions. The buffer stores data from the SCSI port so the SCSI bus is free to do other tasks while the box communicates with another device. The GPIB-Sun3-S kits costs $1420. The GPIB-VAX3100-V package sells for $1420 with driver software on a 3.5-in. diskette, and $1520 with software on a TK50 cartridge tape.

National Instruments, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100.
CIRCLE 332

Benchtop ASIC Testers Feature 50-MHz Clocks

A pair of benchtop ASIC verification systems offer 50-MHz clock rates, 16 programmable timing generators with 500-ps resolution, per-pin programmability, and 2-ns pin-to-pin skew. The ETS 200 (to 192 pins) and the ETS 270 (to 512 pins) handle multiple formats, including window and edge compare, and allow continuous edge placement with no dead zones. Users can program split-cycle I/O operation on all pins. Standard vector memory is 16 kwords, with 64 kwords optional. The units are available 60 days after receipt of an order. Prices vary with pin count and options. A 128-pin ETS 200 with 16-kword vector memory, programmable power source, DUT board, and software interface simulators, costs less that $39,000.

Hilevel Technology Inc., 31 Technology Dr., Irvine, CA 92718; (714) 727-2100. CIRCLE 333

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CIRCLE 127

TOOL MONITORS, MANAGES COMPANY'S ACTIVITIES

By combining graphics, text, and an object-oriented database on a PC, the Mind's Eye software tool lets users monitor such activities as financial modeling, statistical analysis, and drafting and engineering activities. The tool, from Mind's Eye Inc., runs on an IBM-compatible PC with a minimum of 512 kbytes of RAM and 5 Mbytes of hard-disk space.

The computer-aided management (CAM) tool fulfills all the functions of a support manager. It stores information in its database that helps to make management decisions, either at the time of entry or at some later date. Any information entered can be used for all operations. Hence, data never has to be reentered in other parts of the program.

An example of how the tool can be used is in a manufacturing plant. Assume that a compound is the result of mixing some ingredients. The percentage of each ingredient is fixed, but each has a little leeway. Mind's Eye can monitor the percentage of each ingredient and, if any falls outside its allowable range, the tool could either stop the process or signal a manager to let him know about the situation.

The same tool can be used to keep track of all the employees in a company. It can keep a hierarchical tree of all employees so the manager knows what all the employees' job functions are and who they report to. It can also keep track of the company's financial information. By entering the costs of certain data, whether it's materials, labor, or something else, Mind's Eye makes sure that the manager is always on top of the situation.

Mind's Eye uses standard interface methods to select functions. The first method is through a border menu. This menu typically invokes a pop-up menu or dialogue box to carry out commands. The dialogue box lets the user enter data prior to invoking the function. Then the information can be reused without being retyped. A user-programmable hot-key can also invoke a command.

Mind's Eye contains an extensive set of context-sensitive, on-line help functions. These can be invoked at any point in the system by simply hitting one of the function keys. It will retrieve help information pertaining to the task from which it was called.

Data, including macros, can be imported from other programs such as Lotus 1-2-3 and dBase. Images can be drawn directly in the tool's editor with a mouse and a built-in component library.

Minimum system requirements include an 80286-based PC running at 12-MHz, MS-DOS 3.3, a color EGA monitor, and a two-button mouse. Most printers and plotters are supported. Mind's Eye is available in either custom or shrink-wrap versions. The shrink-wrap tool costs $995 and will be available in the first quarter of 1991.

Mind's Eye Inc., *36 Commerce Way, Woburn, MA 01801; (617) 935-2679.* **CIRCLE 334**

■ *RICHARD NASS*

We'll help you find those little critters.

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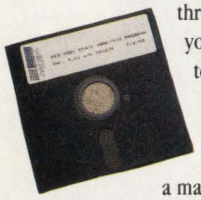

Our newest product, the PED4500, is a laptop portable SCSI bus analyzer. It guides you through the menu-driven setup, capture and display. SCSI bus changes are time-stamped and stored in the 32,768 word SRAM buffer. Captured data is displayed as a signal listing, timing wave form, or as easy-to-understand SCSI commands, status and messages.

With optional emulation installed, you can use the PED4500 as SCSI initiator or target.

The PED4500 laptop analyzer features a 16Mhz 286 processor, 40 MB hard drive, VGA-compatible gas plasma display, and 101-key keyboard. Or, if you wish, you can buy the analyzer as a drop-in card and software and install it in your own PC. The choice is yours!

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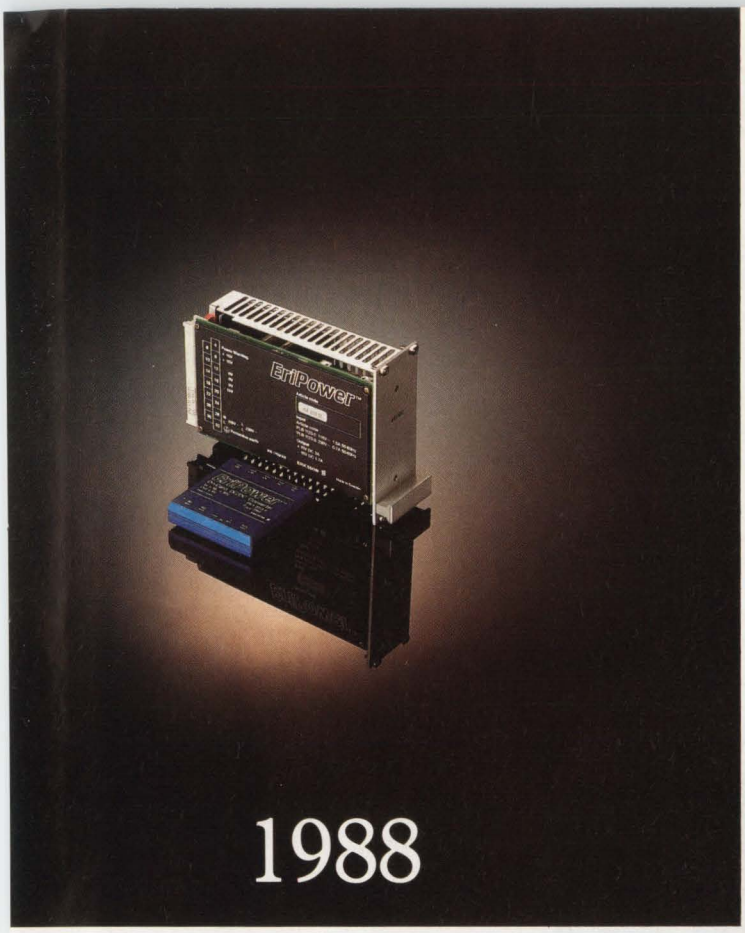
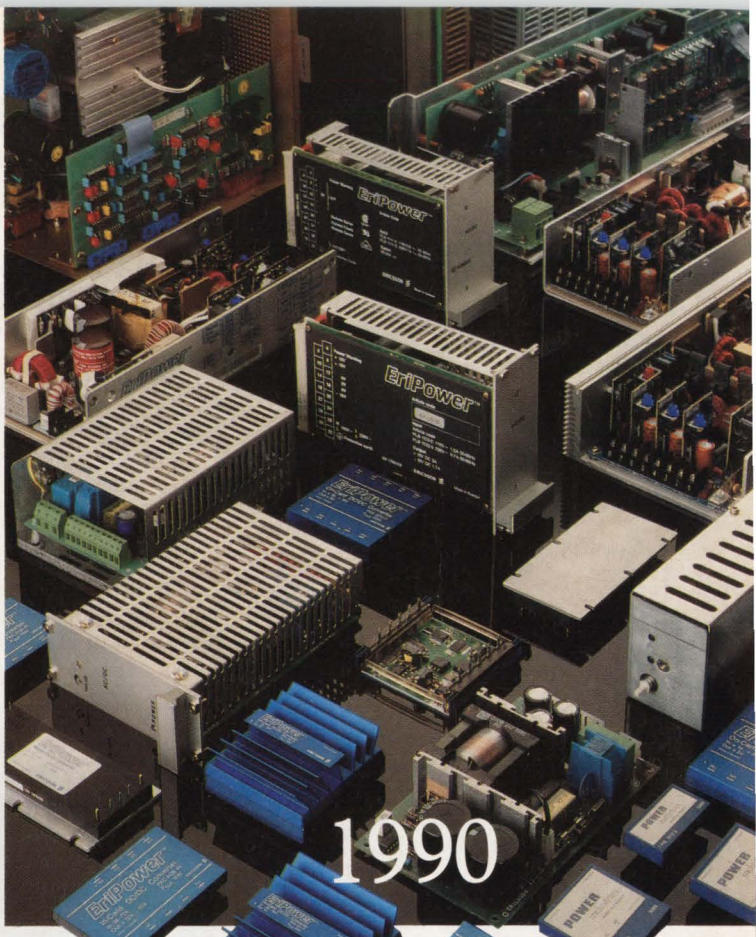
CIRCLE 138





The power product range from Ericsson has been putting on weight recently

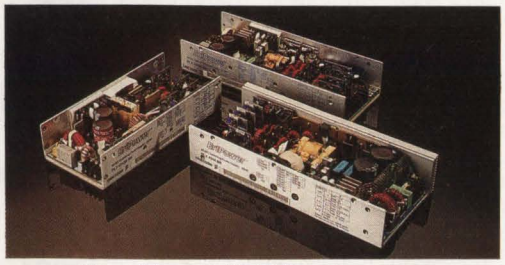
Right up to 1988, the Ericsson range of high reliability power supplies was limited - Eurocard PLB switchers, and the remarkable PKA miniature, high frequency DC/DC converters. Remarkable, because they marked the advent of the power component concept as complete modules which can be used to realize distributed power architecture.

Since then things have changed.

Today the EriPower™ range includes DC/DC converters from 0.3Watts to 200Watts. And most of them are also designed to be paralleled for system upgrading.

What's more, the AC/DC power supply range covers 60 Watt to 400 Watt requirements with Eurocard and open frame power supplies. When necessary, there's even a full custom design facility for high volume users.

In short, the EriPower™ range has put on a lot of weight, and there's now a product for almost every need.



The new PLY: versatile 150-400W open frame switchers

PKY: 30-200W modules have standard pinning/ footpring (Note: Only available in Europe)

But one or two things haven't changed. For example, EriPower™ power supplies still meet or exceed international standards for safety and RFI/EMI emission. They all represent the very latest technology of their kind. And they all feature the demanding MTBF performance you'd expect of products from Ericsson - over 200 years in some cases. After all, as a part of one of the world's leading telecommunications companies, reliability is a vital part of our culture.

As you've probably realized, the EriPower™ range is expanding fast. Simply get in touch and we promise to keep you up to date, as we continue putting on weight.

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CIRCLE 104

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ROMABLE OS SIMPLIFIES EMBEDDED PC DESIGN

Providing MS-DOS 3.2 functionality, a ROM-DOS operating system, ROM-DOS, can operate from within ROM or boot a system from a floppy- or hard-disk drive. The software can easily be modified to optimize the package for a particular application and includes support for ROMable EXE files. The RXE option allows users to take EXE files generated by most software languages and place the file in ROM and execute from within the ROM; only the program data is loaded into RAM. Since most DOS programs are composed of 80 to 90% code, running a program as an RXE file uses much less RAM than running standard EXE programs. The ROM-DOS ROMable operating system requires minimal memory space. For example, with all functions included, it takes about only 34 kbytes of ROM; and when running, it needs just 14 kbytes of RAM. A mini-BIOS that requires just 3 kbytes of ROM is also available for embedded-systems applications. The mini-BIOS provides support for a remote console (via a serial port). It also features a hardware timer and serial ports. A ROM-DOS developer's kit is also available from Datalight. The developer's kit sells for $495. Unit prices for the ROM-DOS ROMable operating system are $6 per copy in quantities of 5000.

Datalight Inc., 17505 68th Ave NE, Suite 304, Bothell, WA 98011; Roy Sherrill, (206) 486-8086. CIRCLE 336

ADA DEBUGGER JOINS FORCES WITH EMULATOR

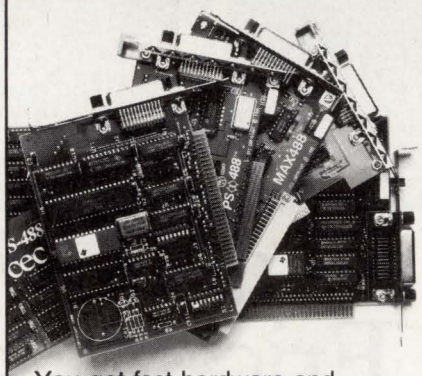
Merging debugging and emulation into one package, the TEKDB/Ada source-level debugger has been integrated with the Tektronix MV6820 emulator and TekDB monitor. This integration now makes it possible for the product to provide a real-time execution environment for testing and debugging Ada software. With all of the emulator's features incorporated into TekDB/Ada, extensive monitoring and control of the target environment is now possible. One of TEKDB/Ada's most powerful features, the Performance Analyzer can be used to quickly pinpoint hot spots in the Ada run-time code. Each performance run is summarized with a histogram showing the relative amount of execution time for each Ada module or memory range. Since the program executes in real time, modifications can be made quickly and evaluated. TekDB/Ada uses the IEEE-695 common-object format to transfer object modules that are output from a cross compiler. The TEKDB/Ada source-level debugger is available on VAX/VMS, VAX/Ultrix, and Sun-3 host-computer systems. Prices for the VAX version of TEKDB/Ada range between $3850 and $7900. The Sun version of the TEKDB/Ada source-level debugger is priced at $3850. Delivery takes two weeks after receipt of order.

Tektronix Inc., Microprocessor Development Products, P.O. Box 12132, Portland, OR 97212; (800) 245-2036. CIRCLE 337

VGA SOFTWARE IN PUBLIC DOMAIN

Software that compares the performance of VGA adapters fitted to IBM PC AT and compatible computers has been placed in the public domain by New Dimension International Ltd. The program was created using the firm's "Superscape Alternate Realities" 3D and "walk-through" image-generation system, and presents an automated 3D sequence of color images that rotate and move independently on screen. While the 100-s sequence is running, a timer determines the screen refresh rate, and at the end of the cycle calculates the average number of screen updates the computer system has achieved in one second. The result is presented in frames/s—the higher the number the better the system's performance. The company hopes its "3D-Bench" program will be adopted as a standard benchmark. It says that the benchmark is dependent on a number of factors, including the processor type such as 80286, 80386 or 80486, its clock speed, the use of cache memory, the internal architecture of the PC, whether an 8- or 16-bit bus is used, and the efficiency of the VGA card. The presence of a floating-point co-processor doesn't affect the result. The program is non-interactive, thus the reference point used to create the benchmark is fixed. No restrictions have been placed on use of the program which may be bundled with hardware or used by manufacturers to provide a continuous display during exhibitions or in showrooms. New Dimension also offers to write customized demonstrations and environments to order.

New Dimension International Ltd., Zephyr One, Calleva Park, Aldermaston, Berkshire, RG7 4QW, United Kingdom; 44 734 810077. CIRCLE 335



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CIRCLE 90

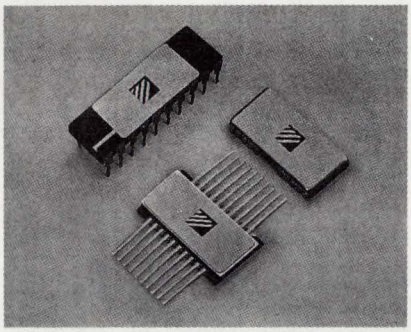
CIRCLE 97 →

SPEEDY MILITARY DRAM ACCESSES IN 70 NS

Compliant with Mil-Std.-883C, the EDI44256Cxxx and 411024Cxxx dynamic RAMs offer the shortest access times of any military-grade CMOS DRAM. The 44256 comes in a 256-kword-by-4-bit organization, while the 411024 versions are 1-M-by-1 devices. Both can access in as little as 70 ns. Additional speed grades of 80-, 100-, 120- and 150-ns access times are also available.

The by-4 memory can be housed in either a 20-pin 300-mil sidebrazed ceramic DIP or a ceramic small-outline J-leaded package. Double the number of package options are available for the by-1 version of the CMOS DRAM—in addition to the 20-lead SOJ package, the chip can be had in an 18-lead sidebrazed ceramic DIP, 20-pin ceramic zig-zag in-line package, or a 20-lead ceramic flatpack.

Both versions of the megabit chip include three refresh modes—row-address-strobe (RAS) only, hidden refresh, and column-address-strobe before RAS. The DIP-housed version of the by-1 memories also offers a test-enable function that reduces chip test time.



When the function is activated, the memory array is divided into four quadrants that can be tested in parallel. All inputs and outputs are TTL-compatible. The chips operate from a standard 5-V power supply.

Samples of all versions are available from stock. Prices for the military units start at $253 in 100-unit lots.

Electronic Designs Inc., *42 South St., Hopkinton, MA 01748; Kay Ritter, (508) 435-2341* **CIRCLE 338**

■ *DAVE BURSKY*

CHIP SET TRIMS BOARD SPACE FOR MIPS CPU

Aimed at replacing 40 or more standard logic circuits, a five-chip set provides most of the support logic required by the R3000 CPU from Mips Computer Systems to implement a workstation-like motherboard. The MIPSET chips from LSI Logic operate at clock frequencies of either 20 or 25 MHz and directly support the LR3000 CPU and its associated 3010 floating-point math unit.

Included in the chip set are the LR3201 reset and interrupt controller, the LR3202 bus controller, LR3203 DRAM controller, LR3204 DRAM data controller, and the LR3205 block-transfer controller. Although there are five basic chips, multiple copies of the 3204 DRAM data controller are required since each of the chips contains only an 8-bit slice of the data bus. The DRAM controller supports from 2 to 64 Mbytes of 80-ns memory and 2-way interleaving.

The block-transfer controller includes a 16-bit direct-memory-access channel for an Ethernet support chip. It also includes three 8-bit channels for SCSI, parallel, and floppy-disk-drive I/O support.

Each channel includes an 8-word by 32-bit bidirectional FIFO for data buffering. By separating the direct CPU control from the rest of the system, LSI has created a local expansion bus it calls the L-bus, to which the memory and various I/O functions can be are attached.

Additional support chips are required to add serial I/O ports and a real-time clock. A complete 10-chip set—the five chips plus three additional 3204s as well as the R3000 CPU and 3010 FPU—sells for $704 (20-MHz) or $1097 (for the 25-MHz version) in 1000-set lots.

LSI Logic Inc., *1551 McCarthy Blvd., Milpitas, CA 95035; Brian Halla, (408) 433-8000.* **CIRCLE 339**

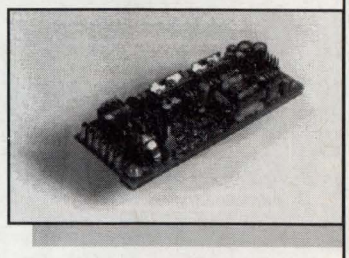
■ *DAVE BURSKY*

1- AND 2-KBIT EEPROMS OFFER 10-YR GUARANTEE

A guarantee that data will be retained for ten years after 1,000,000 read-write cycles per word is offered by SGS Thomson Microelectronics (STM) for its ST93CS56 and ST93C46A serial EEPROMs. They have capacities of 1 kbits and 2 kbits, respectively. The devices are made with STM's specially developed CMOS-F3, a 1.5-μm, single-metal, single-polysilicon process. Extra process stages are added to allow implementation of non-volatile memory cells. The 8-pin-packaged chips include built-in electro-static protection, with all inputs designed to withstand 2 kV as prescribed by test method 3015 of MIL-STD 883. Operation is from a single 5-V supply. Suggested applications include TV and radio tuners, telephone dialer memories, and cordless-phone sets.

SGS Thomson Microelectronics Ltd., Planar House, Globe Park, Marlow Bucks, SL7 1YL United Kingdom.

CIRCLE 340



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CIRCLE 144

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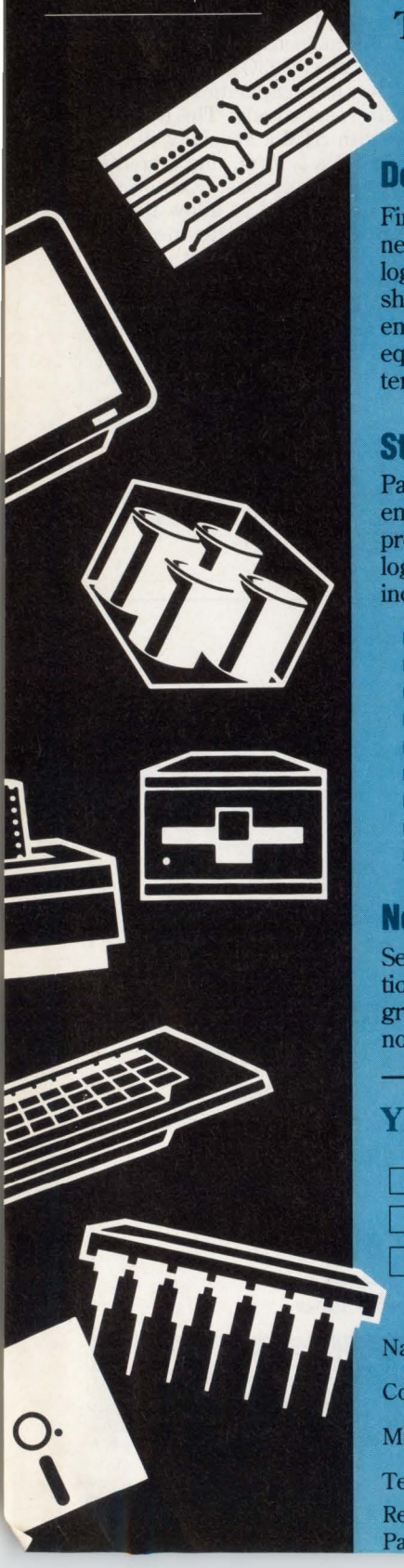

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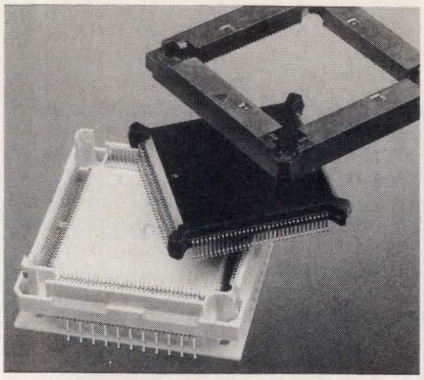
HIGH-DENSITY SOCKETS EASE PQFP HANDLING

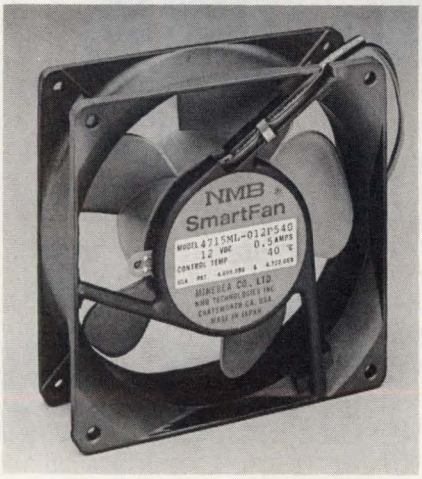
Two-piece sockets for plastic quad flatpack (PQFP) ICs feature 0.025-in. contact centerline spacing and a low 0.375-in. profile above the board. The PQFP is easily inserted into the cover, which contains protective slots for aligning



and separating IC leads. The cover subassembly is then snapped into place over the housing. Sockets come in 100- and 132-position sizes. A 100-position socket costs about $8.62 in lots of 1000. The 132-position version costs about $10.35 in similar quantities. Delivery is in four to six weeks.

AMP Inc., P.O. Box 3608, Harrisburg, PA 17105-3608; (800) 522-6752.
CIRCLE 341

SMART COOLING FAN VARIES RPMS WITH TEMP

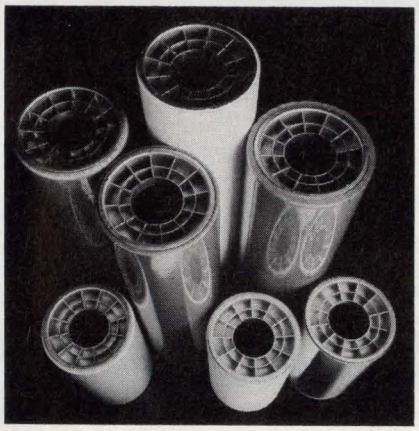


Containing a closed-loop temperature-regulating system, the SmartFan automatically controls the cooling air flow. That lets the fan hold the temperature within an equipment enclosure relatively constant against fluctuations in room temperature, system power dissipation, flow resistance, and altitude. Since most systems, especially computers, are rarely packed to maximum capacity, the fans would typically run at less than maximum speed, and thus last longer and produce less noise. Dc powered, the SmartFans can be had in four sizes—4.7-in.^{2} by 1.5-in. thick, as well as others that are 3.1-, 3.6- or 4.7-in.^{2}, all with a thickness of 1 in. Price for the 4.7-in.^{2}-by 1.5-in. unit is $15 in quantities of 5000. Delivery is from stock.

NMB Technologies Inc., 9730 Independence Ave., Chatsworth, CA 91311; (818) 341-3355. **CIRCLE 342**

FLEX-CIRCUIT MATERIAL WITHSTANDS HARSH USES

Harsh, high-temperature environments are no match for R/flex 1100 flexible-circuit material. The polyimide-based circuits reduce space and

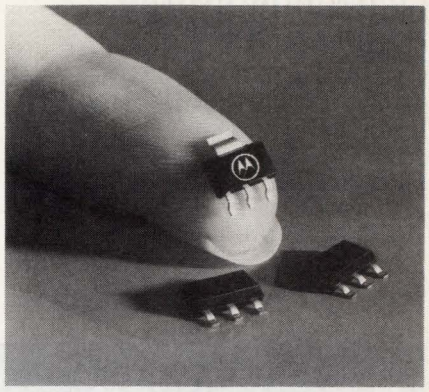


weight requirements as well as improve system reliability in many applications. Thanks to their high chemical resistance, low moisture absorption, and good dimensional stability, the materials withstand very adverse conditions. Two roll widths—24 in. by 250 ft. and 500 mm by 250 ft.—are available. Typical availability is three weeks. Pricing is based on configuration and quantity.

Rogers Corp., Circuit Materials Div., Box 4000, Chandler, AZ 85244; (602) 786-8284. **CIRCLE 343**

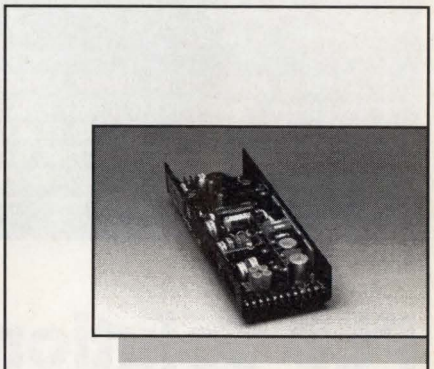
PACKAGE BOOSTS SMT FOR POWER TASKS

With the addition of a surface-mounted package with medium-power capability, Motorola hopes to accelerate the use of surface-mounted technology in applications such as small motors, disk drives, switching-power-supply drivers, and others. The SOT-223 package is



capable of 800-mW power dissipation on an FR-4 glass-epoxy pc board, and up to 1.6 W on ceramic substrates or aluminum-backed boards. The package ensures level mounting, which means better thermal conduction. Several small-signal transistors are planned for the package now, with more by 1991. Call the company for pricing and delivery.

Motorola Inc., MD Z201, 5005 E. McDowell Rd., Phoenix, AZ 85008; (602) 244-3742. **CIRCLE 344**



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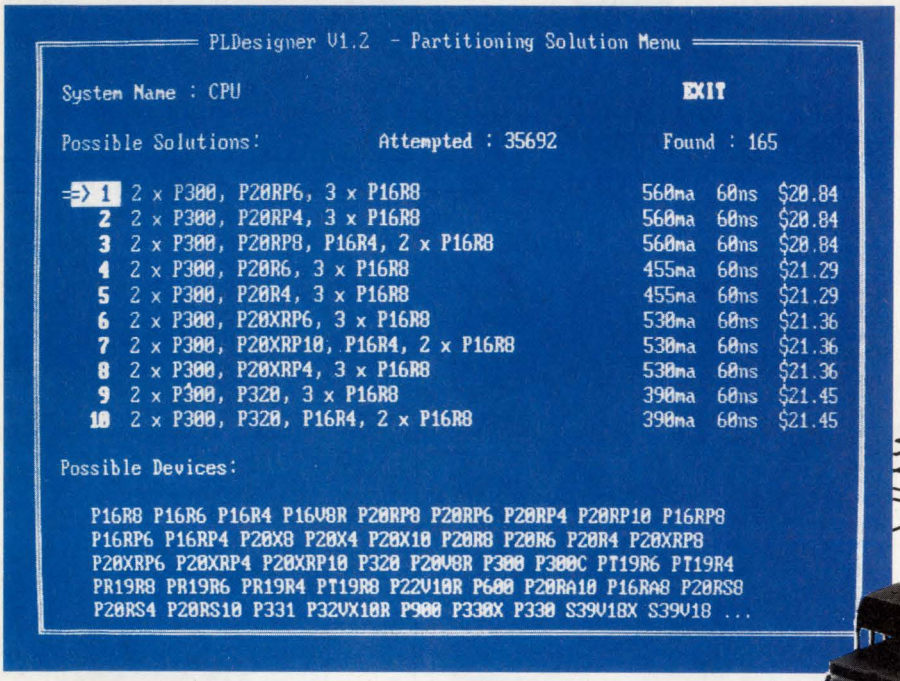
LIGHTGUIDE SYSTEM PROTECTS OPTICS

Fiber-optic cable can now be routed and protected properly with the use of the Lightguide enclosure system that is available from the Tyton Corp. The Lightguide enclosure system prevents accidental cuts and kinks of the cable as well as the signal losses that result from such cuts and kinks. Included with the enclosure system are connectors with the correct bend radii and various horizontal and vertical transitions. These included connectors ensure effective signal transmission while using minimum space. The connectors feature quick-release covers. This handy feature provides users with simple reentry into the system. Call the manufacturer for pricing and availability.

Tyton Corp., P.O. Box 23055, 7930 N. Faulkner Rd., Milwaukee, WI 53223; (414) 355-1130 CIRCLE 345



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CIRCLE 98

HIGH-LEVEL 4-20-MA XMTR OFFERS 0.25% ACCURACY—EXTRA FEATURES

The process-control industry will not abandon its love for the 4-20-mA analog data and control signal loops. As a result, Analog Devices is adding the AD694 high-level 4-20-mA IC transmitter to complament the AD693. The AD694 takes a high-level control signal (0-to-2 V or 0-to-10 V), usually from a computer-driven DAC, and converts it to a 4-20-mA current loop. Typically, in these applications, it will be transmitting a control signal to a linear actuator. Its mate, the AD693, takes millivolt-level signals from sensors and transmits them as 4-20-mA signals to a host processor's analog front-end data-acquisition system. (By letting 4 mA equal signal-zero, the host can differentiate between no-signal and signal-zero.)

Total error—over temperature—as a percent of span runs a maximum of 0.45% for the premium B grade, twice that for the A grade. Maximum nonlinearity runs 0.005% and 0.015% for the two grades, respectively. The chip offers a number of features not previously availible on an IC transmitter. They include the ability to run off single or split supplies from a minimum of 4.5 V to a maximum of 36 V—and output compliance voltage is within 2 V of the supply. An input amplifier buffers the signal and can provide gain or convert the output current (from a current-output DAC) to a voltage. The chip's reference can provide either 2 or 10 V via pin-strapping. Internally, the chip creates the 4-mA offset which may be turned off for those who prefer 0-to-20-mA operation. In addition, the transmitter's open-collector alarm circuit warns of open-loop conditions or noncompliance of the output voltage. While not mandatory, the IC may be operated with an external pass transistor to minimize self-heating. Depending on performance grade, and whether for the commercial- or industrial-temperature range, the price each in 100s runs between $3.50 and $7.85 each.

***Analog Devices Inc.**, 181 Ballardvale St., Wilmington, MA 01887; (508) 658-9400.* CIRCLE 346

■ *FRANK GOODENOUGH*

LVDT/RVDT CONVERTER FITS IN UNDER 1 IN_2

A 12-bit, tracking LVDT or RVDT (linear variable differential transformer or rotary variable differential transformer) to digital converter has been squeezed into a 26-pin hermetically sealed package just 0.8 in. by 1.0 in. From ILC Data Device Corp. (DDC), the DTC-19305 will handle either type of transducer in the feedback loop of position-control systems. Accuracy runs 0.15% of fullscale + 1 LSB, and repeatability and differential linearity are maximums of 1 and 0.5 LSB, respectively. Closed-loop bandwidth is 47 Hz and settling time for a half-scale step is 120 ms max. The converter interfaces easily with microprocessors, provides an output flag for converter malfunction as well as over and underrange conditions. Power drain is 15 mA max. from ±5-V. In quantities of 1-9, the commercial-grade unit is $245.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; Bill Cullum (516) 567-5600. CIRCLE 349

FASTEST ANALOG MUX SETTLES IN 30 NS

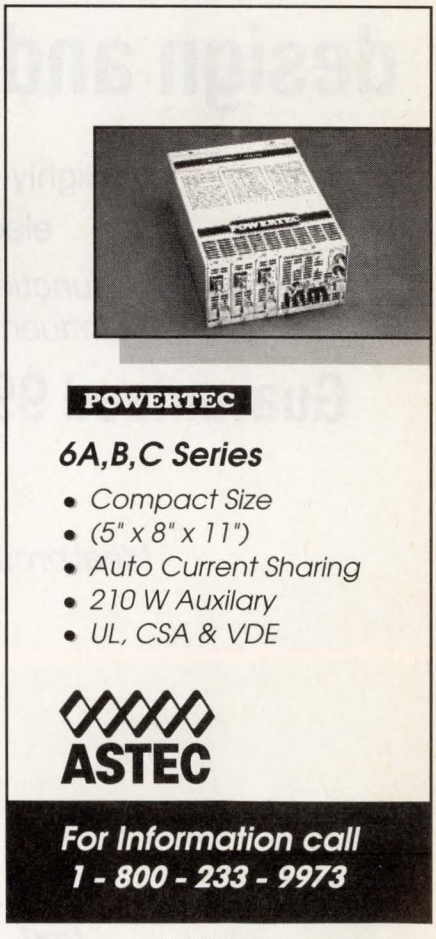
The MX-850 analog multiplexer from Datel is 12 times faster than any other available device. Although most designers take multiplexers pretty much for granted, Datel saw a demand for fast precision devices—with guaranteed specifications—in applications ranging from imaging to multi-channel analog I/O boards. Their MX-850 is a hybrid, and switches 20-V pk-pk input signals at up to 10 MHz and settles the output to within 0.1% of final value in 35 ns maximum. Crosstalk at 10 and 1000 kHz for 20-V pk-pk signals runs -100 and -92 dB maximum, respectively. It drops to -71 dB for 10 MHz with 5-V pk-pk inputs, and -62 dB for a 3-V pk-pk 20-MHz signal. Large-signal 3-dB bandwidth is 80 MHz minimum and nonlinearity is 0.001% of full scale. Power dissipation is a linear function of switching rate: 300 mW at 2 MHz and 1500 mW at 10 MHz. In quantities of 100, the commercial-grade MX-850MC goes for $90 each. The military grade is $15 more.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; Bob Leonard. (508) 339-3000. CIRCLE 347

DUAL COMPARATOR RESPONDS IN 14 NS

Aimed for use as a dual-line receiver for system backplanes, the LT1015 dual high-speed comparator sports a propagation delay of just 10 ns with 20 mV of overdrive. However, this device in its 8-pin DIP also lends itself to other fast comparator applications such as high-speed differential line receivers, pulse-height/pulse-width discriminators, and timing and delay generators. It can also operate as a window comparator. The chip's output-stage design virtually eliminates power-supply glitching during transitions, minimizing instability and crosstalk in multiple-line use. A true latch-pin, with a set-up time of only 2 ns, lets the comparators capture data much faster than the actual flow-through response time. Moreover, unlike earlier TTL-output comparators, it can slew slowly. The LT1015 uses 70 mA maximum from a single 5-V supply. In quantities of 100, the commercial-grade device in a plastic DIP goes for $4.20 each.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bill Reutelhuber (408) 432-1900.
CIRCLE 348



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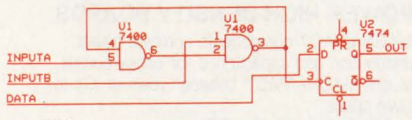

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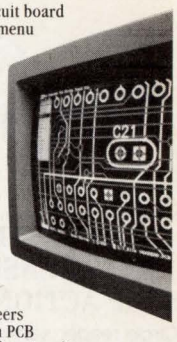

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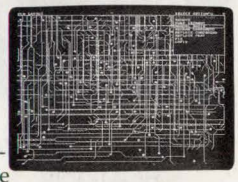

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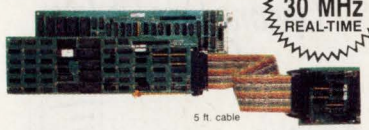

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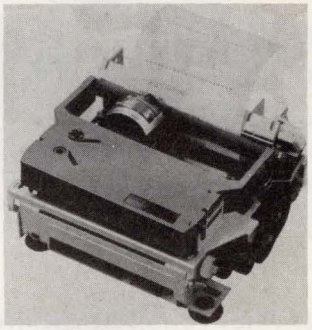

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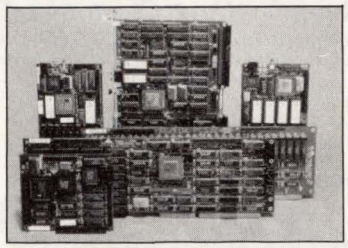

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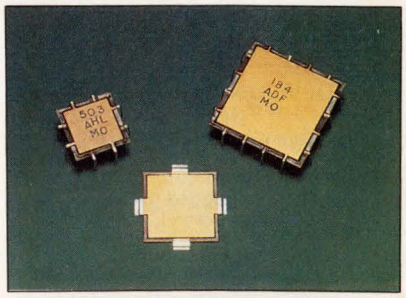

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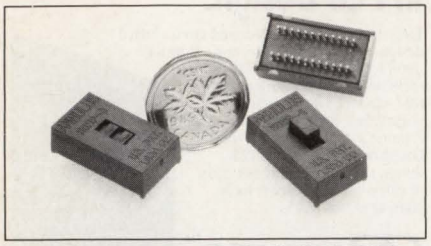

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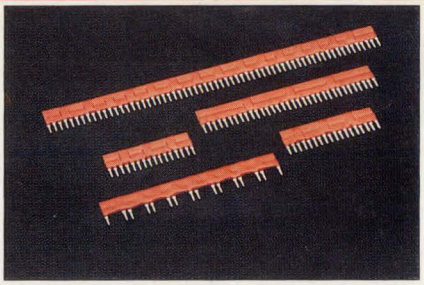

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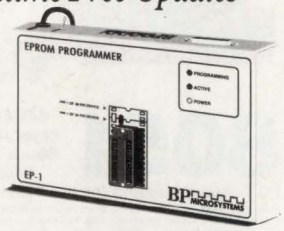

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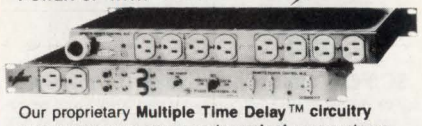

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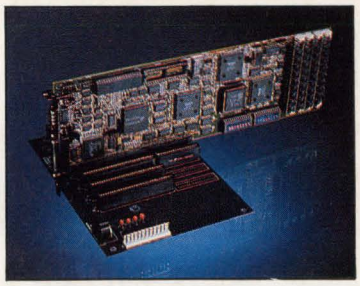

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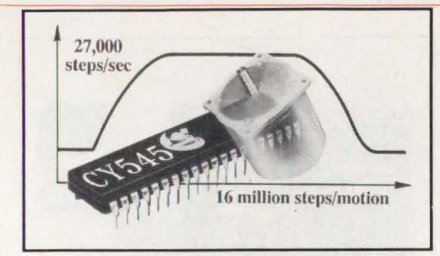

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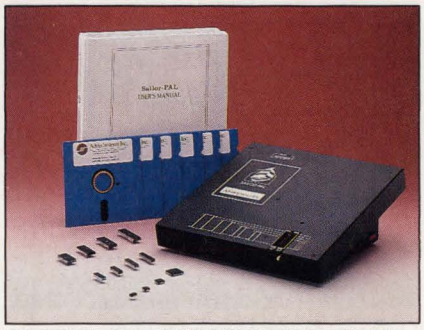

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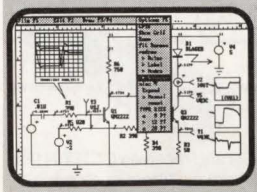

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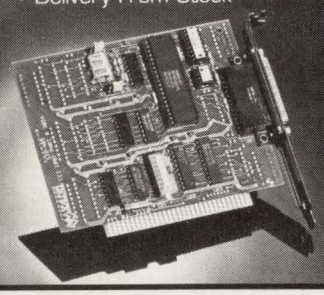

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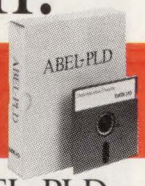

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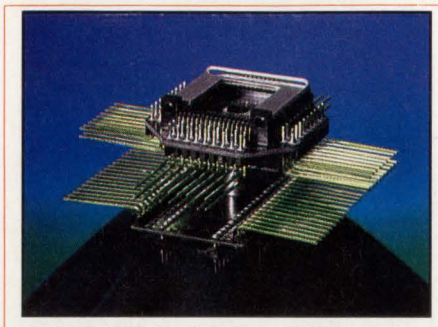

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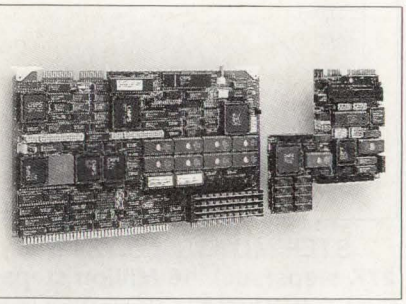

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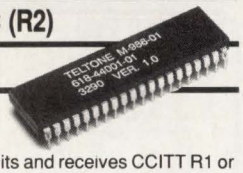

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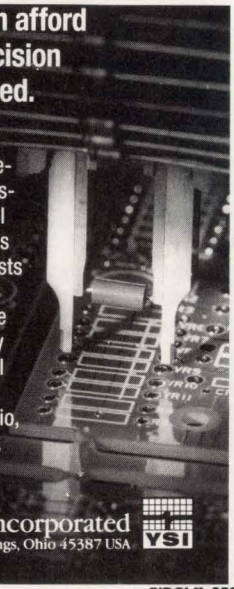

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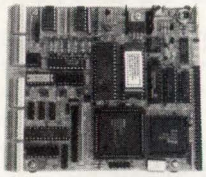

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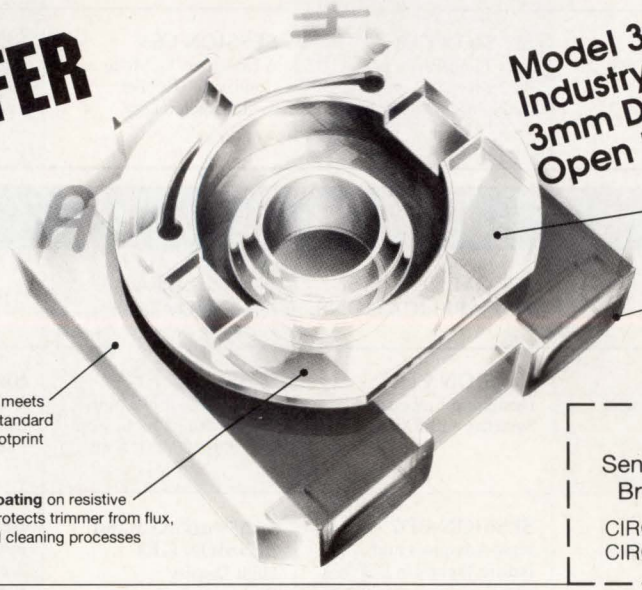

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	COMPONENTS/ MEMORIES	COMPONENTS/ BUS	ELECTRONIC DESIGN AUTOMATION/ASICS	COMPONENT MICROPROCESSORS	SPECIAL PLD DAY W/DEMOS
9 a.m. - 11 a.m.	**SESSION CM1** Advances in Smart Memories Boost System Performance	**SESSION CB1** BiCMOS Technology – a Process for System Bus Interface Requirements	**SESSION EA1** The Realities of ASICs	**SESSION MP1** Floating Point Processing Techniques	**SPECIAL SESSION 1A** Needs and Implications for Very High Speed PLDs for Next Generation Microprocessor System Designs
Noon - 2 p.m.	**SESSION CM2** Designing High Performance Memory Systems for the 1990s	**SESSION CB2** Integrated Systems Solutions to Futurebus+ (IEEE 896)	**SESSION EA2** ASIC Prototyping Alternatives for Systems Level Design Validation	**SESSION MP2** New Developments in 8/16 Bit Microcontrollers	**SPECIAL SESSION 1B** Recent Advances in Innovative, High Density PLD Architectures and Their Benefits for System Designs
3 p.m. - 5 p.m.	**SESSION CM3** Advanced Cache Architectures	**SESSION CB3** FDDI (Fiber Distributed Data Interface) A 100Mb/s Fiber Optic Local Area Network	**SESSION EA3** VLSI Testable Design and Fault Coverage	**SESSION MP3** Making Practical Use of Microprocessor Benchmarks	**SPECIAL SESSION 1C** DEMONSTRATIONS Development Tools for High Density PLDs **2 p.m. - 5 p.m.**

WEDNESDAY ■ NOVEMBER 14, 1990

	CAE DAY	COMPONENT/ EMBEDDED SYSTEMS/CONTROLLERS	COMPONENT/ SEMICONDUCTOR	INTERNATIONAL	SPECIAL SESSIONS
9 a.m. - 11 a.m.	**SESSION CA1** EDA Directions in the 90s: The Enabling Technology for Competitive Electronics Systems	**SESSION CE1** Embedded Systems Design Considerations	**SESSION CS1** Utilizing Reprogrammable PROMs in System Designs	**SESSION IN1** Industrial Strength-Education and Training in the 1990s	**SPECIAL SESSION 2** Neural Networks
Noon - 2 p.m.	**SESSION CA2** VHDL in all Phases of the Design Cycle	**SESSION CE2** Software Disciplines for Embedded Systems	**SESSION CS2** Monolithic Microwave Integrated Circuits (MMICs) and Subsystems	**SESSION IN2** Protecting and Marketing in a Competitive International Market	
3 p.m. - 5 p.m.	**SESSION CA3** Designing with PCs or Workstations: Where to Draw the Line	**SESSION CE3** Very High Performance Processors for Embedded Control	**SESSION CS3** A Designers Guide to Conductive Rubber Switch Technology	**SESSION IN3** Internationalization of O/S and Languages	

THURSDAY ■ NOVEMBER 15, 1990

	CAE DAY	COMPONENTS/ DSP APPLICATIONS	GENERAL/ POWER	INTERNATIONAL
9 a.m. - 11 a.m.	**SESSION CA4** Software Development Environments	**SESSION CD1** Designing Embedded Systems with DSPs	**SESSION GE1** Compliance for Commercial Electromagnetic Compatibility Requirements	**SESSION IN4** Issues of Privacy, Security and Safety Part I
Noon - 2 p.m.	GENERAL/ COMMUNICATIONS **SESSION GE2** Emerging New Rules for Mil-Std Communication Boards	**SESSION CD2** New Advances and Future Trends in DSP ICs and Development Systems	GENERAL/PACKAGING **SESSION GE3** High Density Packaging and Interconnect	**SESSION IN5** Issues of Privacy, Security and Safety Part II

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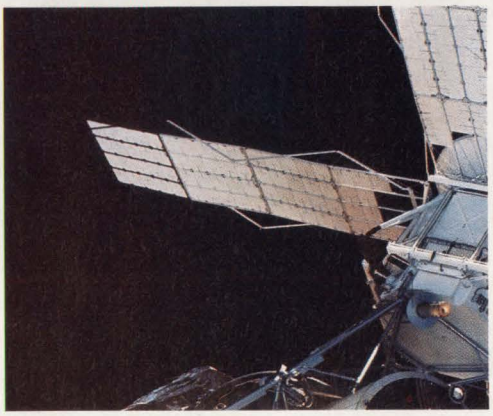

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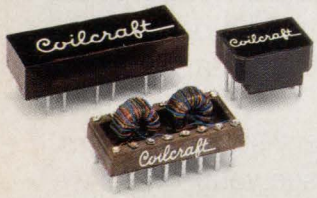

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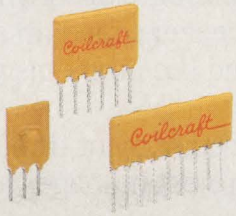

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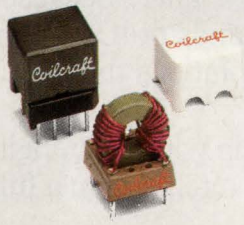

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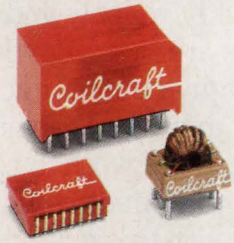

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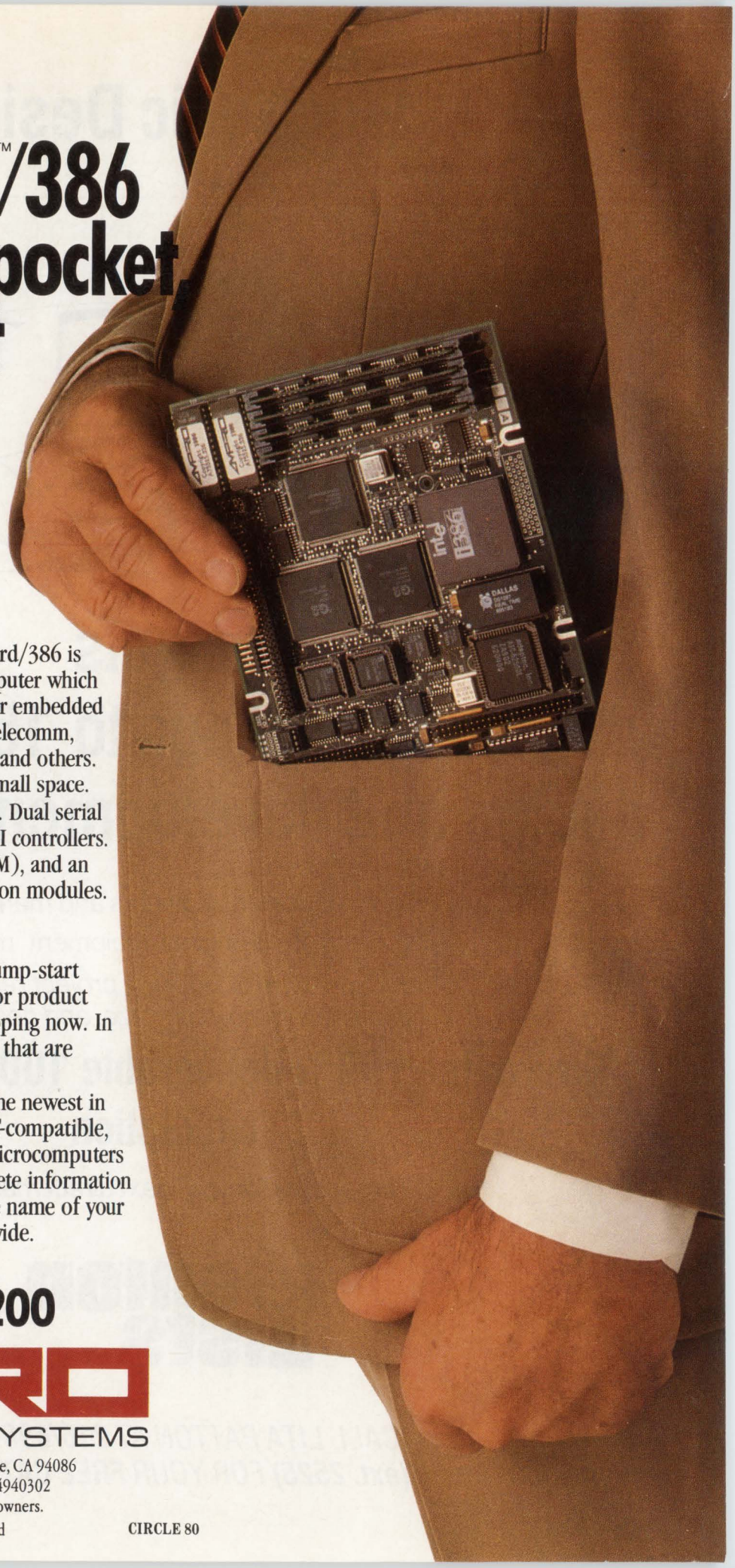

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MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
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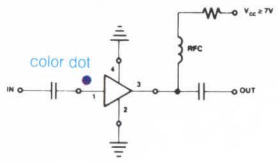

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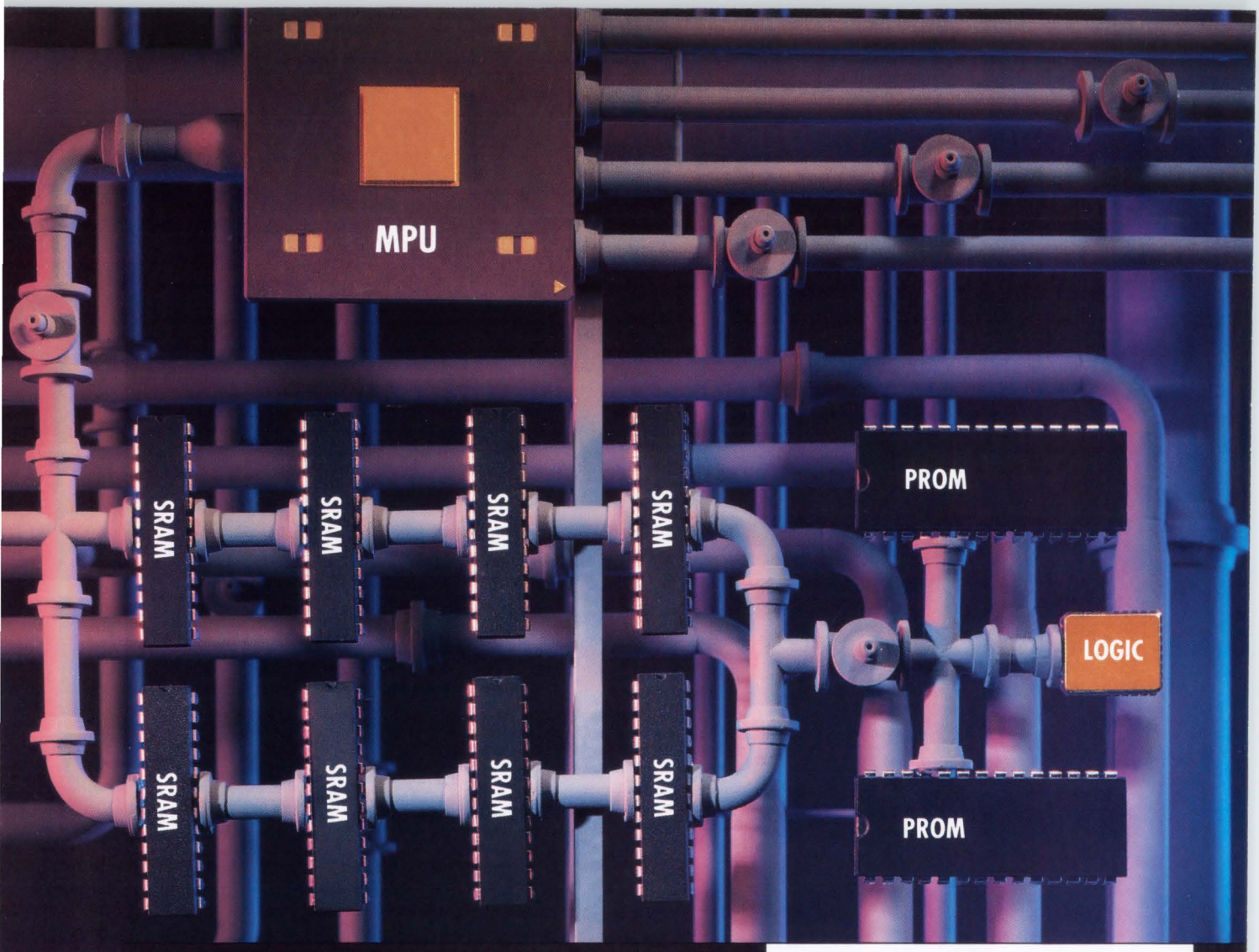

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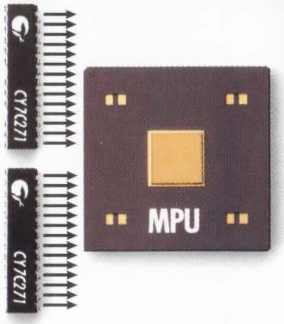

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