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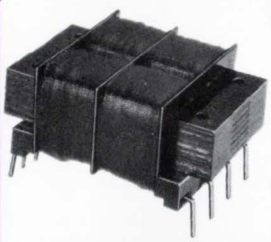

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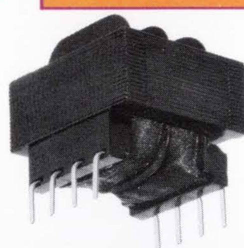

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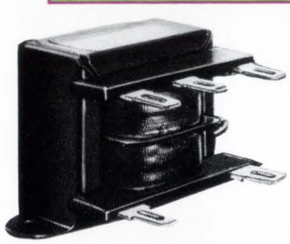

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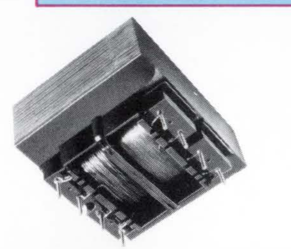

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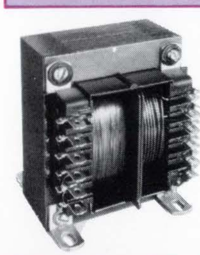

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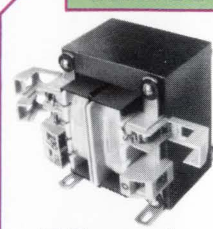

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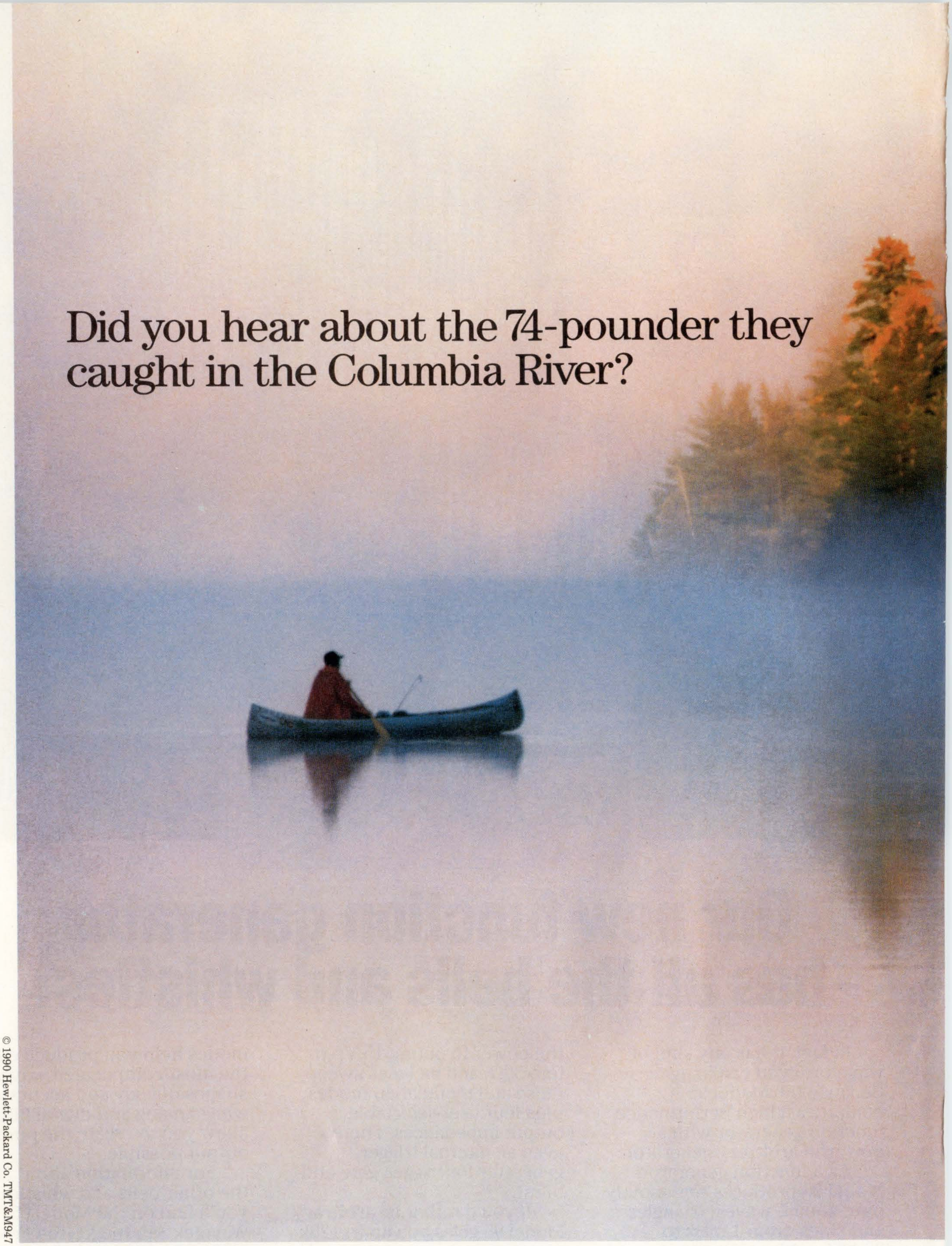
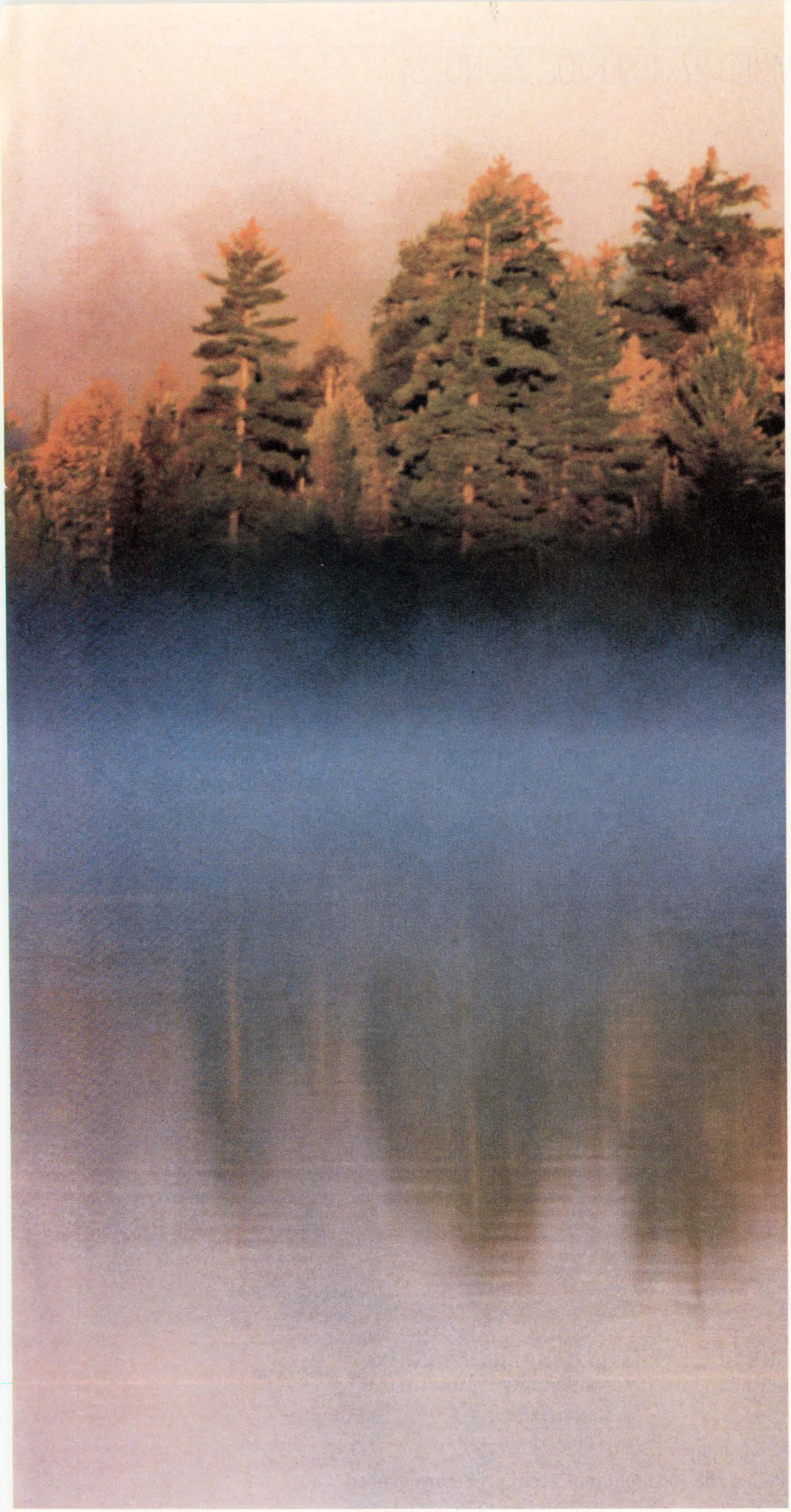
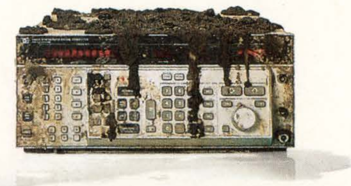
- Available with 110/220V or 220/440V dual secondary
- Taps on primary and secondary allow ± 15% output voltage adjustment

CIRCLE 129


Did you hear about the 74-pounder they caught in the Columbia River?





It worked without a snag.

This is a story about the one that got away. And then came back as reliably as ever.

In 1987, bandits stole four HP signal generators from a truck in Spokane, Washington. Luckily, police managed to recover three of them. But the last one disappeared without a trace.

Six months later, a man fishing the Columbia River hauled in a heavy metal box. Well, within a few days, we had the missing signal generator back. There was mud in every nook and cranny.

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Stories like this underscore why HP rates highest for reliability among engineering managers. We're still not satisfied. In fact, in 1979 we started a Total Quality Control program to increase quality ten-fold in 10 years. We'll reach that goal this year.

It just goes to show you that when design and manufacturing productivity are at stake, there is no reliable substitute for HP. And that sometimes the best fish stories are actually true.

There is a better way.

HEWLETT PACKARD

CIRCLE 131

DECEMBER 27, 1990 VOL. 38, NO. 24

ELECTRONIC DESIGN

Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
Achievement Awards

COMING NEXT ISSUE

Electronic Design's Annual Technology Forecast: The emergence of the renaissance design team
- Proper teamwork is the key to concurrent design
- Design teams face testability
- Concurrent engineering meets design automation
- Designing for reliability
- Outrunning the pack in rapid product development
- Will CASE arrive in the 1990s?
- Faster, more capable PLDs will increase design flexibility
- Standards, distributed processors pace real-time operating systems
- Low-voltage supplies: winds of change are blowing
- Packaging trends in the 1990s
- Systems look to maximize I/O density for fewest dollars
- Passives take on high-tech roles

Introducing a new section: Designing PC systems
- Boost a PC's floating-point speed with an add-on DSP coprocessor
- PC Newsletter
- Products for PC systems

PLUS: A look at the upcoming ISSCC

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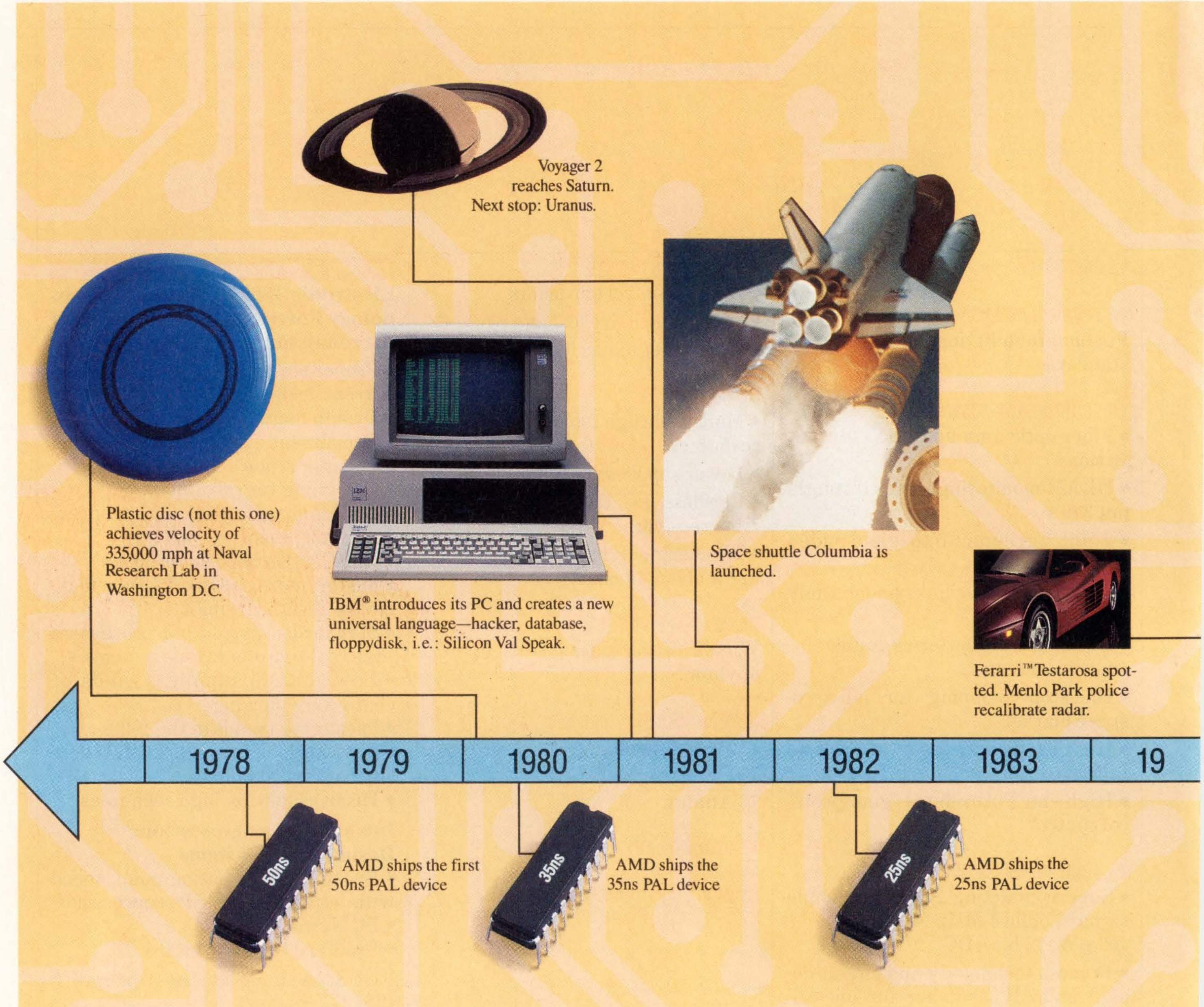

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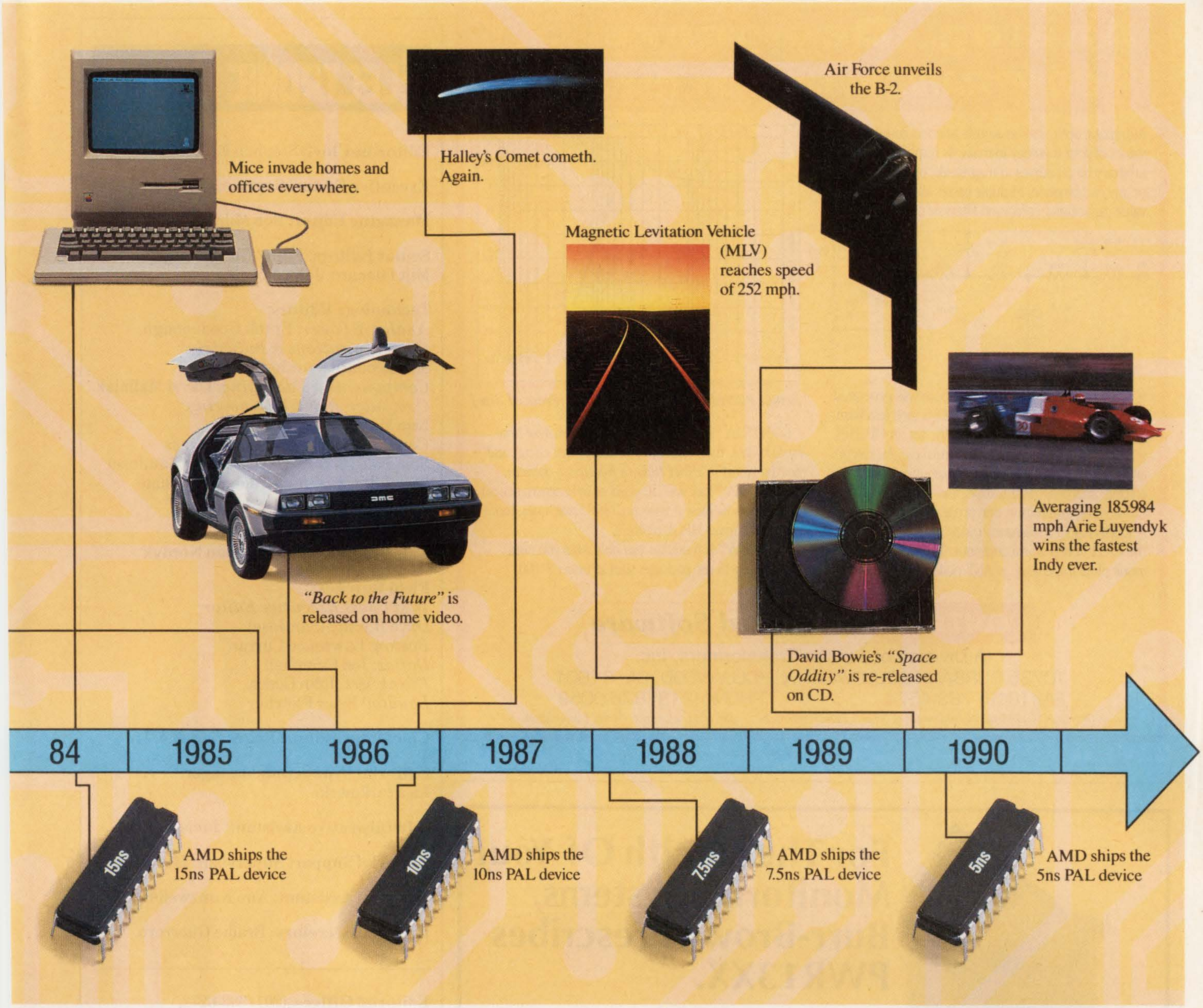

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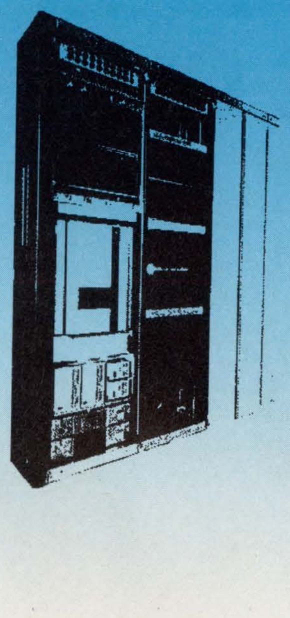
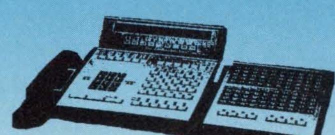
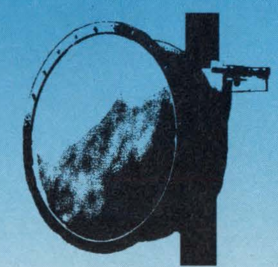


Customer Premises Equipment



Remote Cell Site



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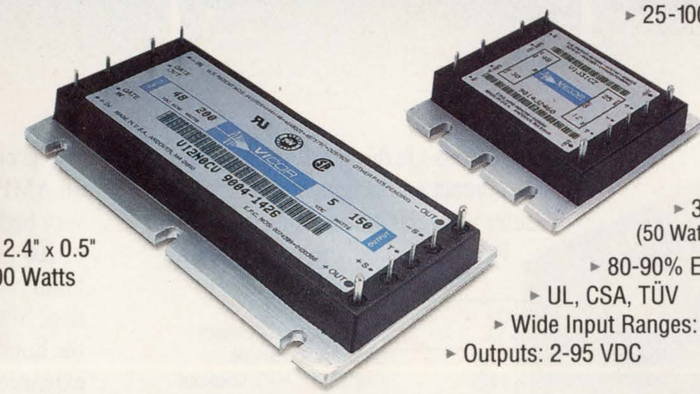

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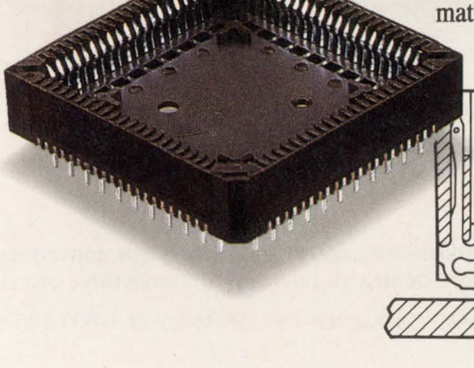
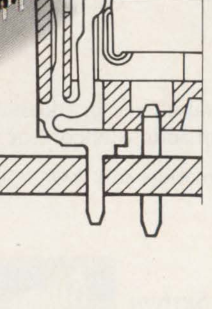
CIRCLE 107

A chip carrier socket that won't play "pop goes the circuit."



Our sockets are designed to get solidly into contact and stay in contact. No matter what the outside influences.

Pop-out is simply not a problem.



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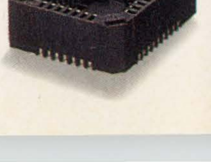
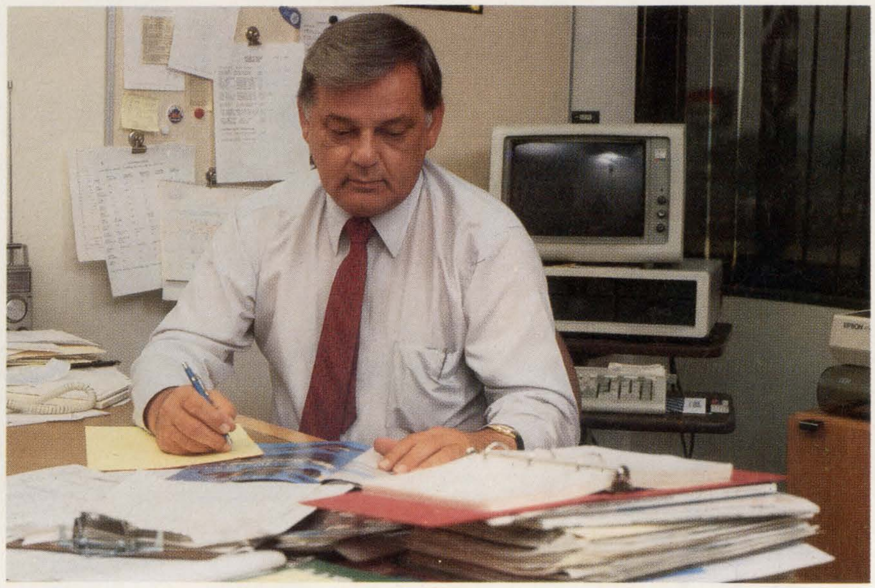
The contacts are High Pressure Tin, an AMP proprietary design that creates very high normal forces — a minimum of 200 grams per contact — for maximum retention and reliable interconnection. Short-signal-path contacts float in the housing to accommodate thermal expansion.

Two basic styles of sockets are available: square or 32-position rectangular. Both come in solder tail or surface



Seven socket sizes are available, with carrier extraction tools provided for each size.



GLANCE AT THE PAST, STUDY THE FUTURE

Traditionally, when any year comes to a close, you reminisce about your accomplishments during the past 12 months. Looking ahead to the future is usually saved for the beginning of the new year. In this issue, we look back by summarizing what we think are the 100 most important products that we've covered in 1990. This gives our readers another look at the most significant developments of the year, while also recognizing the innovation of those manufacturers whose products we mention.

However, in this fast-paced industry, none of us can afford to dwell on the past. It's what's happening now and in the future that counts. In fact, it's possible that some of the products that we covered early in 1990 have already been superseded by others that offer better price-performance characteristics. We fully expect that many of the products covered during 1990 will be obseleted by others during the coming year—that's simply the nature of our industry. Today's products seem to take their place in the sun for ever briefer periods.

Looking ahead, we see product lifetimes shortening even further and an intensifying pressure to hit the narrowing windows of market opportunity with new products. In the Technology Forecast in our January 10, 1991 issue, we'll focus on the changes in design methodology that are bringing about fundamental changes in the makeup of the design team. The well-structured design team of the future will include more than just design engineers. In the effort to avoid loopbacks in the design process, other experts will have to participate from the beginning—test engineers, manufacturing engineers, marketing experts, and even customers themselves will have strong inputs into design configurations before any prototypes are made.

So join us in this issue's review of the highlights of 1990, and then stay tuned as 1991 unfolds.

Stephen E. Scrupski
Editor-in-Chief

SPDT switch dc to 5GHz with built-in driver

Truly incredible...a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

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SPECIFICATIONS YSW-2-50DR	dc-500MHz	500-2000MHz	2000-5000MHz
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ(dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ		1.4	
Video breakthrough to RF, typ (mV p-p)		30	
Rise/Fall time, typ (nsec)		3.0	

*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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CIRCLE 104

PUSHING FOR A PC INSTRUMENT STANDARD

JOHN NOVELLINO
SENIOR EDITOR

The trend toward increased standardization has gained much attention in the test-and-measurement field of late. The VXIbus, which enhanced the VMEbus for instrument use, has been well accepted; hundreds of VXI products have been introduced. Moreover, a level of software protocols, IEEE-488.2, has made the general-purpose interface bus (GPIB) easier to use. And the boundary-scan standard (IEEE-1149.1), unveiled this year, promises more thorough and easier testing of complex, high-density pc boards.

On the heels of this string of successes comes a call for a standard involving modular personal-computer-based instruments and data-acquisition systems. The scheme envisions PC cards mounted in enclosed modules that plug into multislot mainframes using the PC/AT bus. At first glance, the system, which was proposed by Tom Bardeen, president of Seattle-based Rapid Systems Inc., looks much like the VXIbus. The proposed standard's name, PCXI, was obviously meant to invoke such a comparison. Bardeen says PCXI is needed because the PC is a questionable environment for plug-in instrumentation. He cites noise, power, and cooling as the primary concerns. PCXI's shielded modules take aim at the noise problem. The standard would also document the compatibility between the mainframe output power and the modules' power needs to ease integration. And a cooling specification would enable users to determine interoperability between mainframes and modules. Bardeen sponsored a meeting in Anaheim last month (the day after Wescon) to organize a consortium to write a formal PCXI specification. Although nine companies had signed letters of intent, Rapid Systems was the only one to join the consortium. A second meeting, to be held next month, will be open only to companies who have joined the group and have sent in their membership check.

The idea of a technical standard for PC instruments is certainly worth discussing. But is the need really great enough to warrant the effort, and is this proposal really headed in the right direction? The PC environment is already highly standardized, and many manufacturers make plug-in cards for the bus. While the inside of a PC may not be the best location for instrumentation, outboard mainframes are available. Rapid Systems offers mainframes and plug-in CPUs already. A more significant question is software standards, and PCXI has yet to address that issue.

Another significant concern that hasn't been discussed is configuration, notes Richard House, data acquisition product manager for National Instruments, Austin, Texas. "On the AT bus, our customers for data acquisition and GPIB boards always have trouble getting address levels, interrupt levels, and DMA levels right," says House. "So if there's a way to standardize all that and make it easier for the customer, I'd say, yes, there's a need for those type of standards." But while House acknowledges that noise, power, and cooling are important issues, he says National rarely gets customer calls complaining about them.

The PCXI proposal received a cool reception from MetraByte Corp., Taunton, Mass. (a subsidiary of Keithley Instruments). MetraByte just isn't convinced of the technical need for a formal standards process. The company did not attend the November meeting and right now is in a "noncommittal mode," according to Bob Judd, vice president of marketing. "I'm certainly willing to listen to any argument, although I don't necessarily see the need for a standard," he says. Interestingly, Judd comments that, "We see so many consortiums that we are asked to join that we're kind of slow to jump in. First, we like to see whether or not it's our customers that are the driving force behind them." It remains to be seen whether there's enough interest to drive PCXI beyond the initial planning stages.

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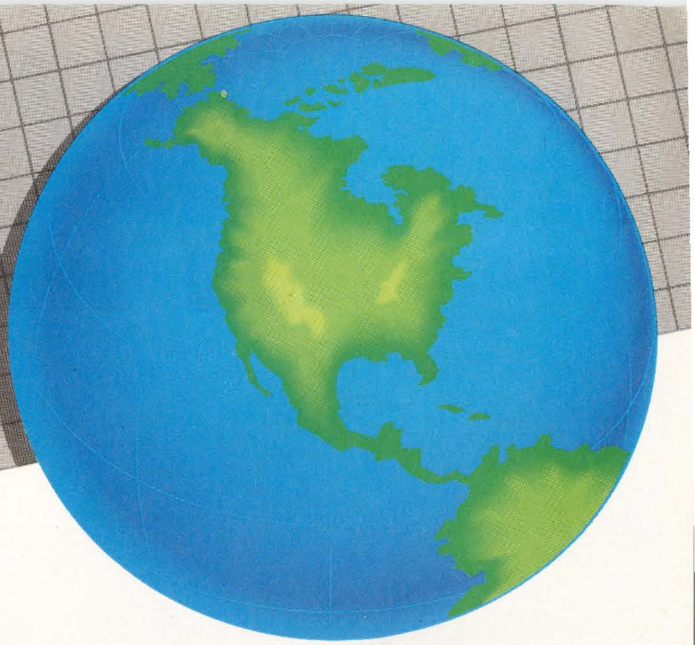
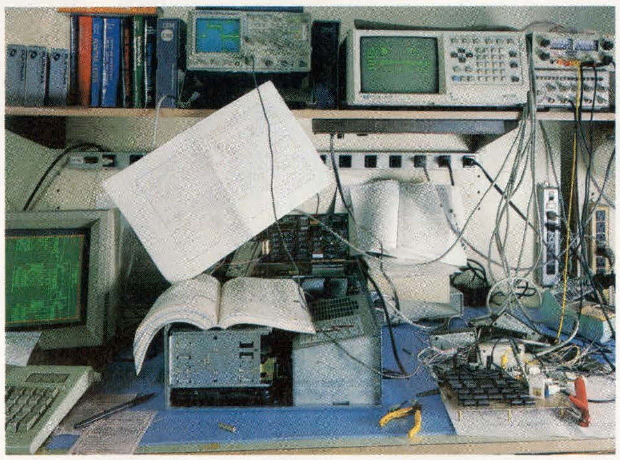


There Are Two Ways to Do DSP!



The Hard Way

- Time consuming
- Incompatibilities due to multiple vendors
- Unclear path from prototype to production
- Steep learning curve for software and hardware
- Uncertain results—room for doubt?

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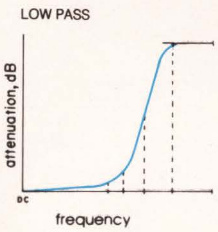
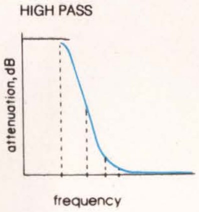


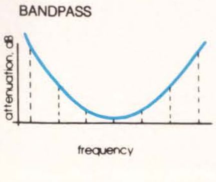
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	STOP BAND, MHz Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz



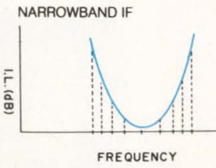
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	PASSBAND, MHz Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	(loss > 10 dB) Max. F4	(loss > 20 dB) Min. F5	(loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	STOP BAND, MHz I.L. > 20dB F6	STOP BAND, MHz I.L. > 35dB F7	STOP BAND, MHz I.L. > 35dB F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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F132-2 REV. ORIG.

FIBER-OPTIC AMP UPS CATV OUTPUT 10 TIMES

By using an erbium-doped fiber-optic amplifier, engineers at the Research Center of Standard Elektrik Lorenz AG (SEL) of Stuttgart, Germany (a subsidiary of France's Alcatel NV communications group), boosted an analog cable-TV transmitter's output 10-fold. The output is now 20 mW (or +13 dBm) compared to the 2 mW achieved for transmitters with conventional fiber-optic amplifiers. The high optical output power will enable cable-TV users to share the costly optical CATV transmitter with many subscribers or remote terminals. The CATV signal used by the SEL engineers encompassed 35 AM TV channels and 30 FM stereo broadcast channels in the 47-MHz-to-450-MHz band. Their experimental setup fulfilled the specifications of an equivalent broadband coaxial-cable system, namely a signal-to-noise ratio equal to or better than 52 dB, a composite second-order figure of –65 dBc, and a composite triple-beats figure also of –65 dBc. In an earlier experiment, SEL used the same type of amplifier to transmit 20-Gbit/s signals over a 115-km-long dispersion-shifted fiber (ELECTRONIC DESIGN, *Nov. 22, p. 23). JG*

DRAM MONITORING RAISES THROUGHPUT 300%

A memory control scheme that employs standard dynamic-memory chips promises to boost system throughput by as much as 300%. The approach requires that the commonly used DRAM control circuitry, and the connections to the memory chips, be modified. Described in a patent recently awarded to Gilbert Hyatt, La Palma, Calif. (he also recently received the patent for the microcontroller, among others), the memory speed-up scheme can be incorporated into DRAM controller chips and system motherboards. The enhancement scheme doesn't clock the memory chips any faster. Rather, it implements what might be referred to as a hierarchical memory addressing architecture that eliminates as many of the slow column-address-strobe (CAS) addressing cycles and slower row-address-strobe (RAS) cycles as possible. That's accomplished by a memory-address-detector circuit in the modified memory controller. That circuit determines the nature of the memory cycle needed to access the data. The controller simultaneously accesses data from multiple blocks of memory and determines if the memory address is located in a currently addressed row and column in one of those blocks. If it is, then the data can be accessed by chip selection alone, eliminating the need for a RAS or CAS cycle. If the memory address isn't in a currently addressed row and column, the controller then checks if the data is in the currently addressed row. If the memory address is there, then a CAS cycle starts and chip selection picks the right data block; if it isn't in the row, then a full RAS/CAS cycle occurs followed by a chip-select operation. Contact Charles McHenry (503) 772-2382. *DB*

JOINT AGREEMENT TO YIELD VIDEO CHIPS

A joint venture to develop a line of next-generation video-processing devices has been agreed to by Philips Components-Signetics, Sunnyvale, Calif., and VLSI Technology Inc., San Jose, Calif. The devices will incorporate VLSI's design tools and Philips' desktop video expertise. The planned product line will include ASICs and application-specific standard IC building blocks. The devices will be used to manipulate and digitize video signals in desktop video applications, such as graphics design, publishing, desktop presentations, and training. Under the agreement, VLSI will use its 1.0-μm libraries and design tools while Philips will contribute its video design know-how and specialty cell library. Users will be able to process video data from various sources, including VCRs, laser disks, video cameras, and broadcast signals stored in video RAM, magnetic, or optical-storage devices. Typical feature-processing capabilities will include warping, windowing, and special effects. *ML*

SUPERCONDUCTIVE LINKS UNDER STUDY FOR ICS

Because superconductors behave similar to metal conductors but have the advantage of zero resistance, digital designers have dreamed of the benefits that super-fast circuits could reap from interconnects made from such materials. Now, thanks to a Defense Advanced Research Project Agency (Darpa) research contract, a practical study on the subject is underway. The Darpa-funded study will examine the applicability of superconducting interconnects in VLSI chips and systems. The potential rewards of using high-temperature superconductor (HTS) interconnects will be weighed by balancing performance enhancements against development costs. In addition, potential risks, such as yield degradation, will come under scrutiny. The research will also pinpoint the specific applications that can realize improvements in system timing and signal quality through use of HTS interconnects. Finally, the study will look at the superconductor-material characteristics that must be achieved to meet the low resistivity and other requirements of these applications. The Darpa contract has been awarded to Quad Design Technology Inc., Camarillo, Calif., because of its expertise in analyzing and simulating interconnections in high-speed digital designs. *DM*

RECHARGEABLE BATTERIES DOUBLE ENERGY CONTENT

A battery chemistry formed by a nickel/metal-hydride combination promises to double the energy storage in the same-sized packages as nickel-cadmium (NiCd) cells. The cells are more "environmentally friendly" because they don't require the production of cadmium electrodes. As a result, they won't pollute when thrown away. Already, Toshiba Corp., Tokyo, Japan, and Sanyo Electric Co. Ltd., Osaka, Japan, are manufacturing nickel/metal-hydride cells and have started to incorporate them into portable computers and cellular telephones, where battery life is one of the primary system concerns. The new batteries will be easy to retrofit into older systems because they have similar charge and discharge characteristics to those of NiCds. The first U.S. firm with similar batteries, Gates Energy Products Inc., Gainesville, Fla., just released C-, AA-, and 7/5f-size cells that provide 2.3, 1.1, and 2.3 ampere-hours, respectively. Prices for the new cells will initially be about twice those of NiCd cells. *DB*

ONE-STOP SHOPPING FOR MIL-AEROSPACE MARKET

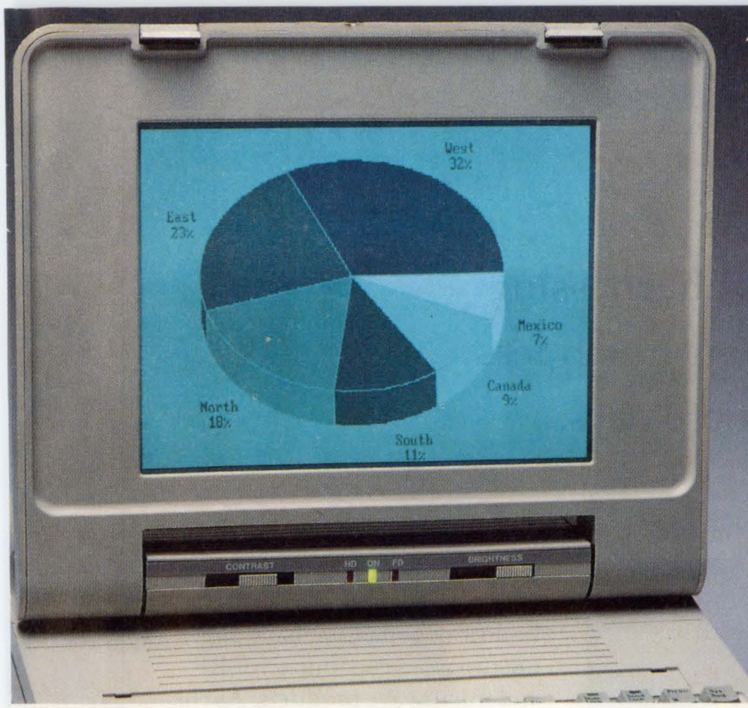
With plans for more Class S parts, Precision Monolithics of Santa Clara, Calif., together with its recent parent Analog Devices, Norwood, Mass., expects to become a single source for all certification levels of analog and mixed-signal ICs in military, aerospace, and satellite applications. By 1994, PMI expects to have Class S digital- and analog-signal processors, as well as voltage-to-frequency and resolver-to-digital converters. That would raise PMI's total of Class S parts from 27, which now includes amplifiers, data converters, voltage references, and comparators, to 60. PMI's Class S certification levels, which exceed all other high-reliability compliance levels, now include MIL-STD-38510 and MIL-STD-883 for space applications. ADI is a leading supplier of standard analog and mixed-signal ICs and ASICs certified to MIL-STD-883, Class B. The combined product portfolios of ADI and the PMI Div. now exceed 720 certified devices. *ML*

HIGH-BANDWIDTH LASER IS EASY TO FABRICATE

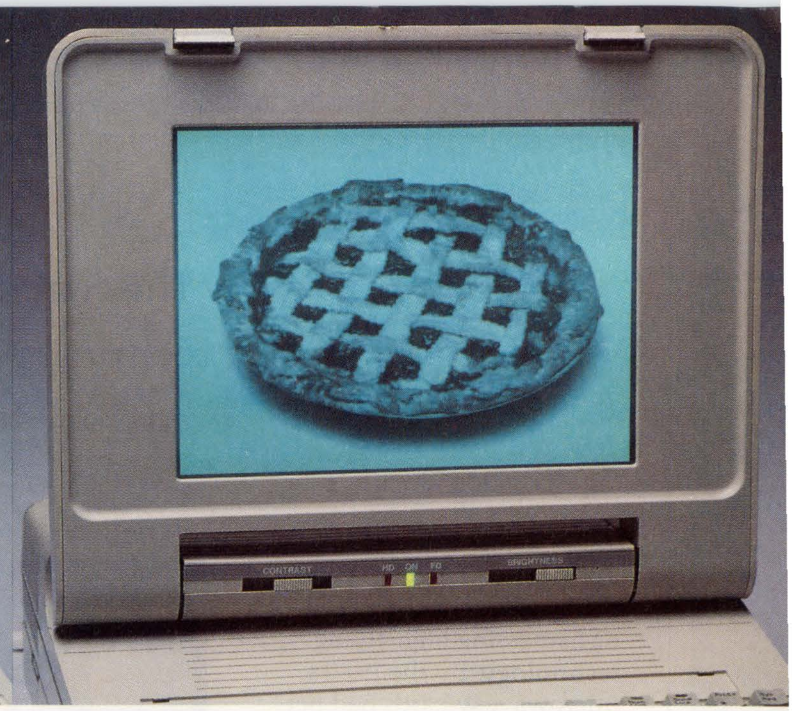
A gallium aluminum arsenide laser aimed at volume applications as a small-signal optical transmitter boasts a modulation bandwidth of 14 GHz. Developed at the Central Research Laboratories of Siemens AG in Munich, Germany, the laser also sports high efficiency and low power consumption: At threshold currents between 10 and 15 mA, the efficiency checks in at 0.4 mW/mA and the electrical power consumption at a low 60 mW for 10 mW of optical power. Because the laser is based on well-established semiconductor technology, it's easy to fabricate in volume. Key to the relatively high bandwidth and the other characteristics is the way the layers in the light-emitting zone are structured. This zone consists of three 7.5-nm GaAs layers separated by two 8-nm GaAlAs layers, forming so-called quantum wells. This "sandwich" is enclosed between n- and p-conducting GaAlAs layers of a semiconductor diode. *JG*

HIGH-END FUTUREBUS+ GETS PROTOCOL CONTROL

A mutual development between Force Computer Inc., Campbell, Calif., and Texas Instruments Inc., Dallas, promises to yield a highly integrated parallel protocol controller (PPC) for Futurebus+. The controller will reduce the board area required for the bus-interface circuitry to less than 30% of what's currently required. It will also implement hierarchical cache coherency to solve the cache-validity problem when multiple processors share the bus. As planned, the chip will implement a 64-bit-wide slice of the data bus and all of the logic to control both the Futurebus+ bus and the local bus (called the H-bus) that will be implemented on the board. TI designers estimate that the chip will require 70,000 to 80,000 gates, give or take about 20%, and will replace close to 40 currently used programmable logic devices. As yet undefined is the H-bus—the general TTL host interface that designers will tie their on-board logic into to communicate over Futurebus+. H-bus details will be released about the middle of next year so that board-level designs can be ready when the chip is released in late 1991. The PPC chip will also have an alternate source: In a deal TI previously inked with Philips Components-Signetics Corp., Sunnyvale, Calif., the latter will alternate-source several TI-designed Futurebus+ chips, including the PPC. TI will also alternate-source a number of Futurebus+ chips already released by Philips/Signetics. Contact Harrison Beasley, (214) 995-6611, ext. 700. *DB*



Cirrus Logic monochrome LCD controllers have given laptop leaders tastier looking graphics displays.



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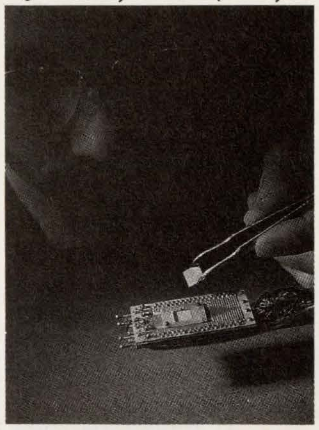
CLOSING THE GAP

SUPERCONDUCTING SQUIDS SAMPLE SIGNALS, BUILD 4-MHZ-NYQUIST, 100-μW, 12-BIT ADC

Not everyone needs an analog-to-digital converter that can digitize dc-to-4-MHz signals, with 12-bit resolution, running on less than 100 μW of power. This is particularly the case if it must be immersed in liquid helium at 4.2K. However, it's just what you need if you want to put the converter inside an infrared camera riding on a satellite, and the helium is free. Such a device has been built out of superconductive quantum interference devices (SQUIDs) by a team at the Westinghouse Electric Corp.'s Science and Technology Center, Pittsburgh, Pa. *(see the photo).*



The converter architecture is very basic—a delta modulator followed by a clocked counter. The quantizer (comparator) and each of the flip-flops forming the counter consist of two-junction SQUIDs employing Josephson junctions *(see the figure, a).* In addition, each stage of the counter is read by a second SQUID. A flux-lobe diagram illustrates circuit operation *(see the figure, b).* Each lobe corresponds to a given state of the SQUID's magnetic flux. Lobe spacing is one quantum of flux (Φ), or $\Phi = h/2e = 2.07$ multiplied by 10^{-15} volt-seconds, where e is the quantity of charge and h is Planck's constant.

The quantizer consists of a single-turn washer-type SQUID with a 50-turn input coil. A signal current to the input coil applies flux to the quantizer, inducing voltage pulses across the output junction of the washer SQUID. A pulse occurs every time a lobe boundary is crossed. Because the lobe spacing is one flux quantum, a least-significant bit of the ADC is quantum-mechanically fixed at Φ/M, where M is the mutual inductance between the input coil and the quantizer SQUID.

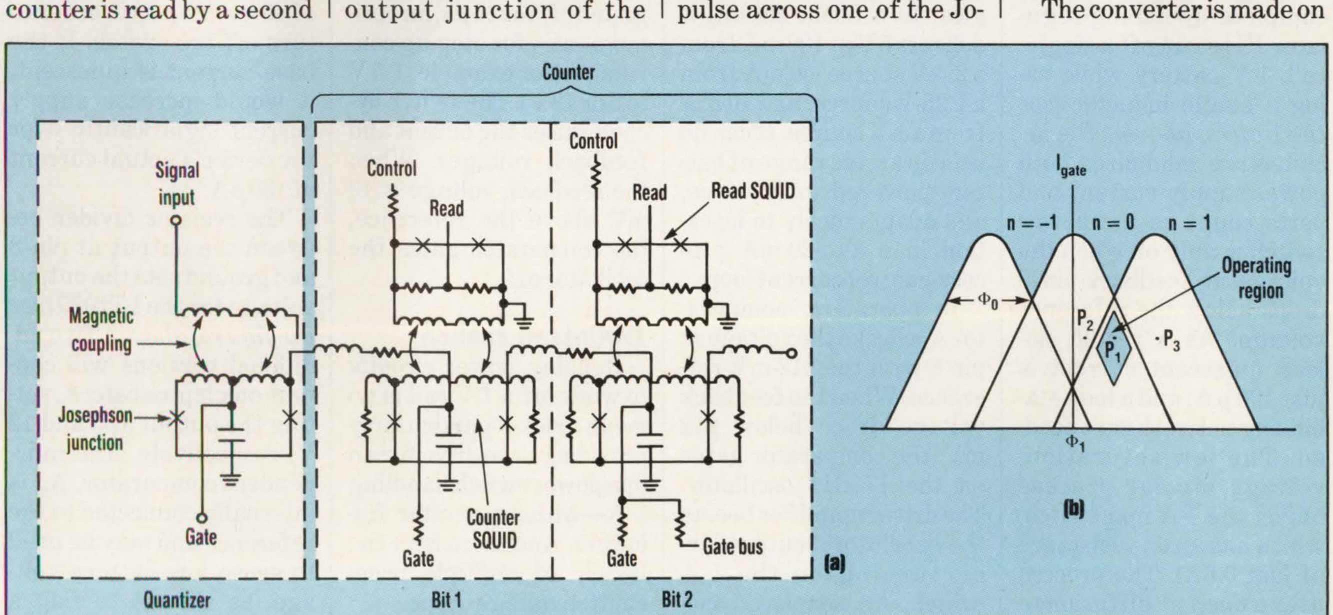
Each counter stage is biased to a point just below a lobe crossing, for example P_1. This point, which lies under both the $n = 0$ and $n = 1$ lobe, is bistable *(see the figure, b).* The flux applied at P_1 induces a circulating current in the SQUID loop that's roughly proportional to the displacement of P_1 from the center of the lobe. The two counter states are then characterized by the direction of this circulating current. A counterclockwise current designates a 0, a clockwise current designates a 1.

When biased this way, a clock pulse on the counter gate induces a lobe crossing, producing a voltage pulse across one of the Josephson junctions and reversing the circulating current's direction. In a 0-to-1 transition, the left junction pulses; in a 1-to-0 transition, the right junction pulses, sending a pulse to the next counter stage. Cascading n stages builds an n-bit, binary counter. The counter is reset by biasing each stage to a point where a 0 is the only stable state, point P_2. A read SQUID, which is also bistable, is magnetically coupled to each counter stage to sense its state.

A full-scale input current of 6 mA to the ADC results in a conversion that's linear and monotonic within $\pm 1/2$ LSB to 9 bits. The counter runs at a phenomenal 50 GHz—essentially producing its 4000 counts in 80 ns. Moreover, it can be read on-the-fly. Full-power bandwidth is about 4 MHz.

Though the ADC dissipates only 100 μW of power, available silicon ADCs with similar performance need several watts of power. However, the latter don't need liquid helium.

The converter is made on

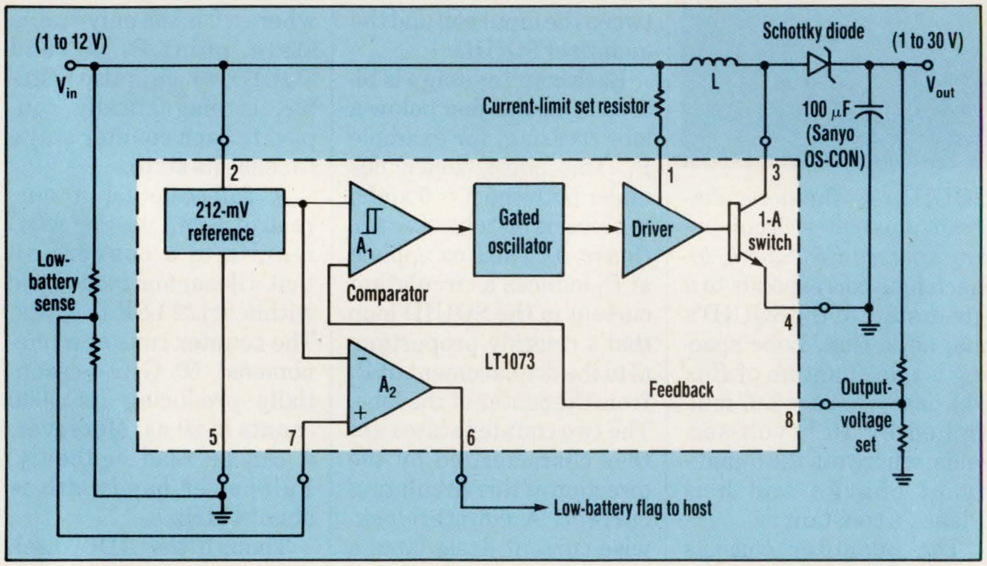


a ten-level, niobium-based process. The process includes seven lift-off levels, two reactive-ion-etching levels, and one anodization level.

A self-aligned anodization technique was used for the small read-SQUID junctions. Reactive-ion etching was employed for the counter junctions where control of critical currents was important. For additional information, call John Przybysz at (412) 256-1421.

FRANK GOODENOUGH

PROCESS TECHNOLOGY AND CIRCUIT DESIGN BUILD IC SWITCHER FOR ONE-CELL BATTERIES



By combining a gated-oscillator architecture with a low-voltage process, designers at Linear Technology, Milpitas, Calif., built the first complete switching-regulator IC to run off a single-cell, 1-V battery while using a single inductor *(see the figure, above)*. The architecture minimizes both power-supply current and parts count as the power switch is only on when the voltage at feedback-pin 8 drops below the reference voltage. As a result, no-load quiescent current is just 130 µA, and a loop-stabilizing network isn't needed. The low-saturation-voltage bipolar process builds the 1-A npn switch, which has an on-resistance of just 0.6 Ω. The process uses a deep p^+ diffusion to build low-saturation-voltage lateral pnp transistors Q_4 and Q_8 in the switch-drive circuit *(see the figure, p. 28)*.

The chip can operate in both boost and buck topologies. In a boost circuit, it delivers 5 V at 100 mA from a 2.4-V source, 40 mA from a 1.25-V source, and 10 mA from a 1-V source. It can be used in a wide range of battery-powered applications, and adapts nicely to insertion in a 4-to-20-mA process-control current loop.

In operation, comparator A_1 checks the voltage at pin 8 with the 212-mV reference. When the feedback voltage drops below 212 mV, the comparator gates on the 17-kHz oscillator. The driver amplifier boosts the oscillator's output level, turning on the 1-A switch. An adaptive base-drive circuit senses switch current and provides just enough drive to ensure saturation without overdriving the switch and wasting current *(see the figure, p. 28)*. The switch is on for 40 µs and off for 16 µs, an optimum ratio for step-up conversion (for example, 1.5 V to 5 or 12 V). The switch cycling raises the output and feedback voltages. When the feedback voltage is 10 mV above the reference, the comparator gates the oscillator off.

BOOSTING BASES

Building power circuits to work off a 1-V rail is no mean trick—particularly providing base drive for an npn power switch handling 1 A—without emitter followers. And there isn't the luxury of multiple base-emitter voltage drops.

One approach is an adaptive base-boost scheme. At the start of a switch-cycle, Q_1 turns on and saturates. This turns off Q_2, allowing 2 µA to be mirrored from Q_3, by Q_4 and Q_5, into the base of the power switch Q_6. Inductor current starts to flow through the switch and increases at a rate equal to V/L. As the base-emitter voltage of the switch increases, Q_7's collector current also increases and is mirrored by Q_4 and Q_5. The ratio of silicon area of Q_6 and Q_7 is set at 40:1, determining minimum beta to keep the switch in saturation.

At the end of the switch cycle, Q_1 is turned off. This allows the collector current of Q_8, which has also been rising in proportion to the current through the switch, to flow into the base of Q_2, turning Q_2 on. Then Q_6 and Q_7 turn off, collapsing the boost. Base boost for Q_2 is necessary because at the maximum switch current of 1 A, Q_5 is operating at a collector current of 25 mA. Q_2 needs a minimum base current of 25 mA, divided by its beta of 40 (or 625 µA) in order to turn off the switch. If the base current is quiescent, it would increase supply current significantly over the device's actual current of 130 µA.

The resistor divider between the output at pin 8 and ground sets the output voltage for the LT1073 *(see the figure, above)*. Two additional versions will contain on-chip resistors, setting the output at 5 and 12 V, respectively. The independent comparator, A_2, is internally connected to the reference and may be used to sense low battery voltage (as shown) to flag a host and/or to supply un-

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The small package size, high power density of 4 watts/in., high peak current for motor starting, and cooling options, make the MAX-750 the power supply of choice for VMEbus systems, workstations, file servers and mini-computer systems. The switcher provides 120 amps of +5 volts for logic and memory, and features up to three auxiliary outputs providing high efficiency, tightly regulated 12 volts or −5.2 volts at up to 20 amps. Designed for world wide use, the series offers AC power fail, AC autoline select, and meets International Safety standards and Class A RFI requirements of FCC and VDE 0871.

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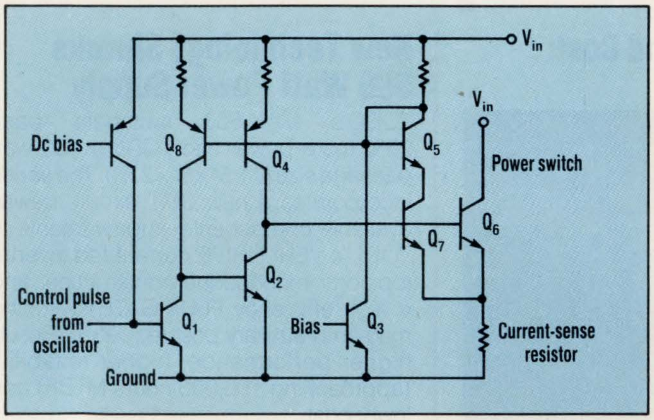


dervoltage lockout. Alternatively, it can be used as a linear post-regulator to reduce ripple. In addition, low equivalent-series-resistance (ESR) capacitors must be used. Linear Technology recommends the use of Sanyo organic-semiconductor OS-CON devices, which offer lower ESR values than equivalent aluminum or even tantalum electrolytics. In quantities of 100, the switchers start at $3.15 each in miniDIPs. For additional information, call Bob Scott at (408) 432-1900.

FRANK GOODENOUGH

OVEN-LESS CRYSTAL OSCILLATOR STABILIZES SATELLITES

Long-term stability is an important parameter in the crystal oscillators used to stabilize very-small-aperture-terminal (VSAT) personal-satellite networks. The satellites typically work the 14-GHz Ku band for their uplink and the 11-GHz C band for their downlink. To generate those carrier frequencies, they use cascaded, synthetic oscillators to elicit the carriers from a 10-MHz crystal oscillator. The oscillator must be extremely stable—better than ±0.2 ppm per year over temperature.

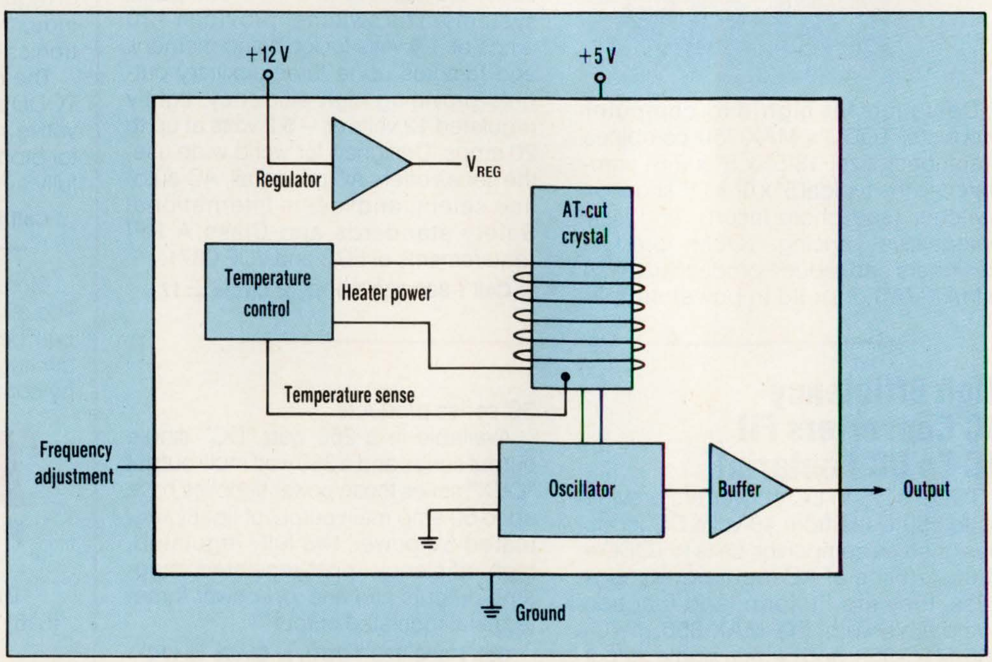
Oven-controlled crystal oscillators can maintain that kind of stability, but they become very heavy—often weighing in at 5 oz. or more. To make matters worse, they're also bulky. And because the oscillators house their crystals in resistance-wire-wound ovens, they consume up to 10 W or more. Obviously, these characteristics aren't very desirable in an orbiting system.

To address these problems, Raltron Electronics Corp., Miami, Fla., devised an oven-controlled crystal oscillator without an oven. The model 65010-B oscillator has its resistance-heating wire wrapped directly around the device's AT-cut crystal *(see the figure)*. This eliminates the physical volume and the thermal mass, load, and impedance of a conventional oven. With no surrounding oven to retard heating, the oscillator consumes just 3 W to reach thermal equilibrium in less than 4 minutes, with a corresponding steady-state frequency stability of better than ±0.05 ppm. Only 1.5 W is required to maintain that stability. Long-term stability, or aging, is better than ±0.2 ppm per year, from –10 to +60°C. The package is smaller than 1.5 in.^{3}.

To develop a direct-heated crystal resonator, designers had to overcome the Q-destroying effects of physical contact between the resistance wire and the crystal. And with no conventional oven to contain the crystal and its temperature sensor, they also needed to come up with a means to embed the sensor within the crystal, which also adversely affects the device's Q specification. The embedded sensor reacts to temperature changes in real time with no hysteresis. Consequently, temperature stability is enhanced.

Other specifications for the oscillator include short-term frequency stability (taken at room temperature at one-second intervals) of better than $\pm 8 \times 10^{-10}$ ppm. Phase noise (jitter) is specified at –123 dBc at 100 Hz. Compensation adjustment for the characteristic aging slope is provided by an external 20-kΩ potentiometer, or by applying an external voltage with a vernier-adjustment sensitivity of 16.65 Hz (out of 10 MHz) per volt. Adjustment range is up to ±6 ppm for 10 years of aging. Other timing uses for the device include TV broadcasting and navigation.

DAVID MALINIAK



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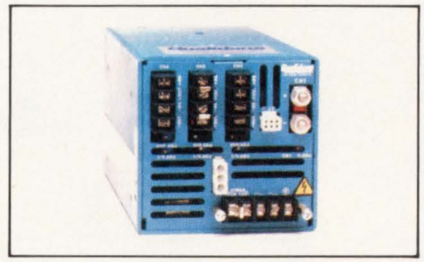

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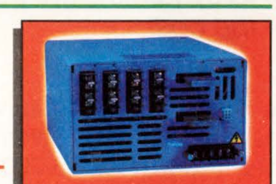

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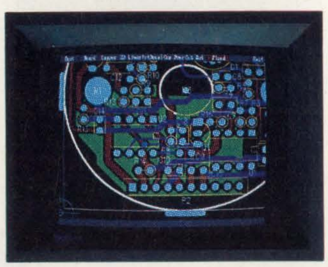

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CIRCLE 98

Controller Chip Unites Standard Architectures To Simplify PC Interface To Multiple Protocols.

Serial Packet Controller Takes On Fast Peripherals

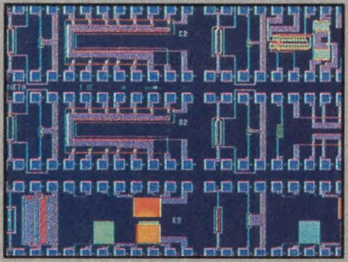
Milt Leonard

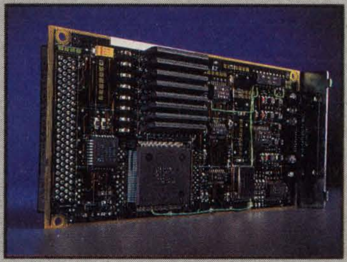
One nasty problem involved in computer-board design is communicating at high data rates with open-architecture operating systems, such as OS/2, while presenting a uniform interface between the host computer and communications controller for multiple communications protocols. A computer's CPU and the local processor and support cards on a CPU card share several responsibilities. They execute communication protocols, and read, packetize, and convert data between serial and parallel formats. The time spent performing these chores has begun to compromise the speed of fast communication devices, such as V.42 modems. In the past, this problem was treated with a mix of universal asynchronous receiver/transmitters (UARTs), communication controllers, and glue logic. Now, a deceptively simple solution does the job with one piece of silicon that allows all-parallel read and write operations between the host CPU and peripherals.

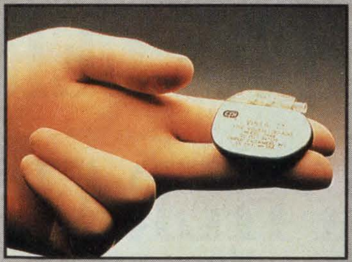
The 73M650 serial packet controller from Silicon Systems is a multifunctional synchronous/asynchronous communications chip that simplifies high-speed packetized serial communications in the PS/2 or PC bus environment. The unique chip architecture is partitioned as two main function blocks *(Fig. 1)*. Channel A is an enhanced version of one channel of an 8530 serial communications controller (SCC). The 550 register block contains the control and FIFO registers of a 16550A UART.

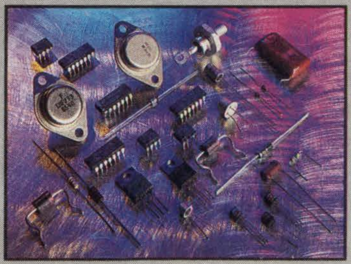
Thus to the PC host, the 73M650 looks like a common 550-type asynchronous UART. But to a device communicating with the PC, the controller can emulate virtually anything, including an 8530-type asynchronous UART.

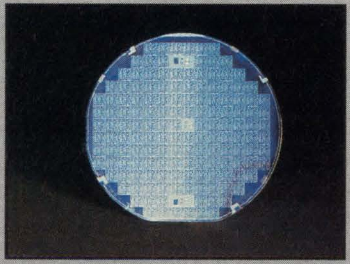
The SCC block performs asynchronous data transfers and packetized synchronous protocols, like monosync, bisync, high-level data link control (HDLC), and synchronous data-link control (SDLC). Included in the SCC are a baud-rate generator and a digital phase-locked loop for clock recovery. A 3-byte FIFO buffer is also incorporated in the SCC trans-

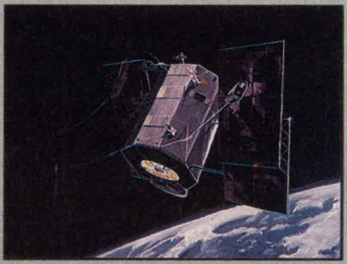












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Pacemaker photo courtesy of Cardiac Pacemakers, Inc. Satellite photo courtesy of NASA. Use of PC board courtesy of Sun Microsystems, Inc.

CIRCLE 91

mit and receive paths to reduce host CPU overhead during data transfers. The channel-A register set, which is similar to that of the 8530, controls the asynchronous and synchronous serial port. Although the SCC block implements the 8530's channel-A operation, improvements in the 73M650 may require modifications in the software now available for the 8530.

Channel A also performs nonreturn to zero (NRZ), nonreturn to zero inverted (NRZI), frequency modulation (FM), and Manchester data encoding. In addition, a 32-bit cyclic-redundancy-check function, which is compatible with the V.42 error-correction standard of the Consultative Committee for International Telegraph and Telephony (CCITT), allows the transfer of compressed data across local-area networks.

The UART register block is register-compatible with a 16550A UART. The registers also provide a high-speed parallel interface to a local communications controller. This block runs most existing software packages written for the 16550A. Channel B is the local controller's interface to the UART register block. Several user-configurable operating modes offer functions for fitting various application requirements. For example, one mode enables bits to be added into the main-processor UART registers to control power-down and other features. This power-down mode extends battery life in laptop or portable PC applications. Another mode makes all channel-B registers accessible to a second processor. With this unique feature, which isn't available in standard products, a software package or a second processor can modify channel-B registers and data FIFO buffers to perform high-speed data compression and/or error correction.

A two-port scratch-pad register in channel B makes it possible to communicate between the host CPU and a local processor or microcontroller. An additional register controls a clock prescaler and oscillator shutdown. An on-chip programmable prescaler allows the crystal rate to be as high as 20 MHz. All registers are supported by internal interrupt logic blocks.

Multiple Modes

This device architecture enables the 73M650 to operate in either a single- or dual-processor environment. When a local processor isn't needed, the controller is configured in the single-processor mode by connecting the mode-select pin to +5 V *(Fig. 2)*. This lets the host CPU access all the registers using one data bus, one read strobe, and one write strobe.

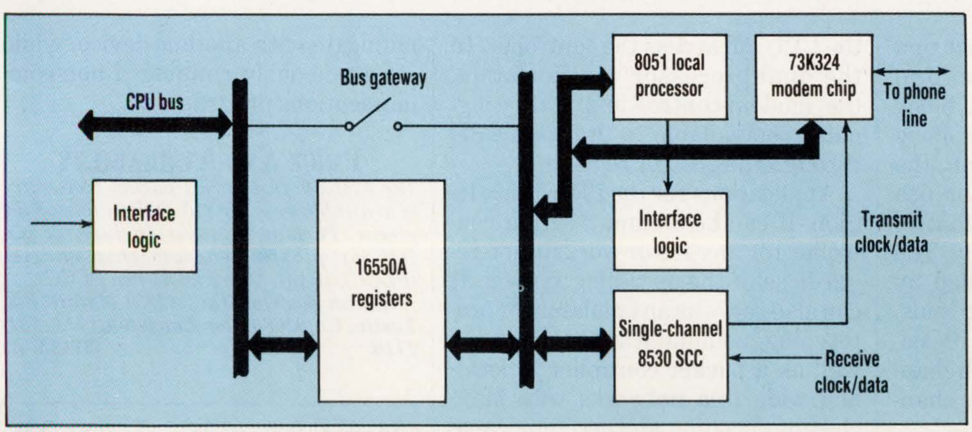
For maximum firmware compatibility with 16550A/8530 operation, the address and chip-select pins supply host-CPU access to 16550A main-port registers, or to channels A and B. For maximum performance, the same pins take the controller into the single-chip-select mode, which is the only mode for the 28-pin version (73M1650) of the device. In this mode, new bits are added to the 16550A registers to supply firmware control of power-down, transmit FIFO trigger-level control, DMA transmit and receive status bits (available only in the 44-pin version), programmable access to the three register sets, and access to an external device in two clock cycles. This latter feature greatly simplifies the required hardware to connect a PC bus to a local device or peripheral.

With a mailbox mode, the host CPU can access the 16550A and SCC blocks independently. This mode is used, for example, when a separate PC program executes the communications protocol. Here, the controller has the same internal setup as the dual-processor configuration, but the hardware access to different registers is through only one data bus. The mailbox mode enables the CPU to replace the function of a local protocol controller while maintaining the standard asynchronous interface. It also makes it possible for users to develop software drivers so that the CPU can access and modify data transmitted or received by a standard software package. This is useful in multitasking applications.

An interrupt can be sent to the CPU to start executing an auxiliary software package whenever data is transferred by the main processor. The auxiliary software can then read the data FIFO buffers, modify the data by compression or error correction, and transmit the new data using the SCC block.

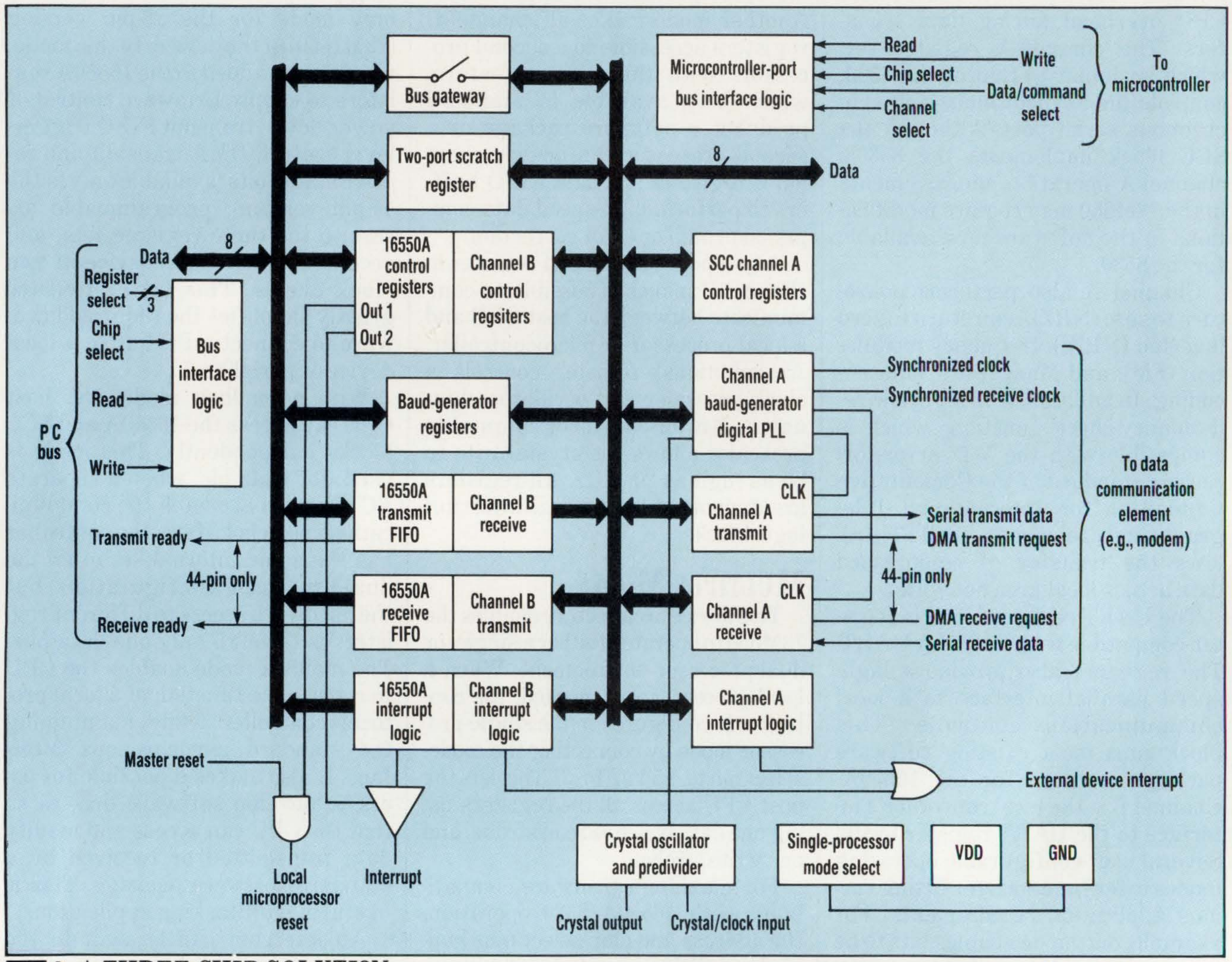
In the non-mailbox mode, the controller can access either the 16550A or SCC block. The controller behaves as either a 16550A or a single-channel 8530 in the same package—always operating as the block that was last selected.

Dual-processor operation is obtained by grounding the mode-select pin. This mode has two parallel interface ports: one to connect to



1. IN THE DUAL-PROCESSOR MODE, one parallel data port of the 73M650 serial packet controller (SPC) links with the host PC bus, and a second port connects to an external protocol controller. The software-controlled bus gateway contributes to the SPC's reconfigurable architecture by linking the PC bus to either the 16550A register set, the 8530 register set, or both.

MULTIPROTOCOL COMMUNICATIONS CONTROLLER



2. A THREE-CHIP SOLUTION **for a modem application uses the 73M650 SPC, an 8051 microprocessor, and a 73K324 2400-baud modem chip. The SPC performs synchronous packetizing of parallel data taken from the PC bus. Modem control functions are supplied by the 8051, which also translates the AT command set into the V.42bis protocol. The modem chip is the data pump that connects to the twisted-pair-wire telephone line.**

a CPU and the other to connect to a local protocol controller. The local controller can then use the SCC block for synchronous or asynchronous protocols. In this configuration, the main CPU and local processor use separate address, data, and control pins to access the controller. The 16550A registers are controlled by the CPU. By using separate pins, some of these registers are accessible to a local processor through channel B. The local processor uses channel A for serial-data transfer.

Upon any change in the 16550A register contents and FIFO buffer status, an interrupt can be generated to notify the local processor that the CPU did access the controller. In the dual-processor configuration, the modem-control and status signals are available to the main CPU through the 16550A registers.

Applications for the 73M650 are legion. It can be an input/output controller for any PC or workstation regardless of the operating system. It can also serve as an emulator for prototyping communications links, as well as a packet controller in local- and wide-area networks with Manchester encoding and decoding capabilities. It can even be used with fiber-optic communications links. It also supports multitasking applications, allowing the host PC to communicate with another device, while simultaneously running a non-communications program.□

PRICE AND AVAILABILTY

The 73M650/1650 serial packet controller is available now for $15 each in lots of 100 pieces. Package options include 28-pin DIP or plastic leadless chip carrier (PLCC), 40-pin DIP, and 44-pin PLCC.

Silicon Systems, Inc., 14351 Myford Rd., Tustin, CA 92680; Don Langston, (714) 731-7110. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
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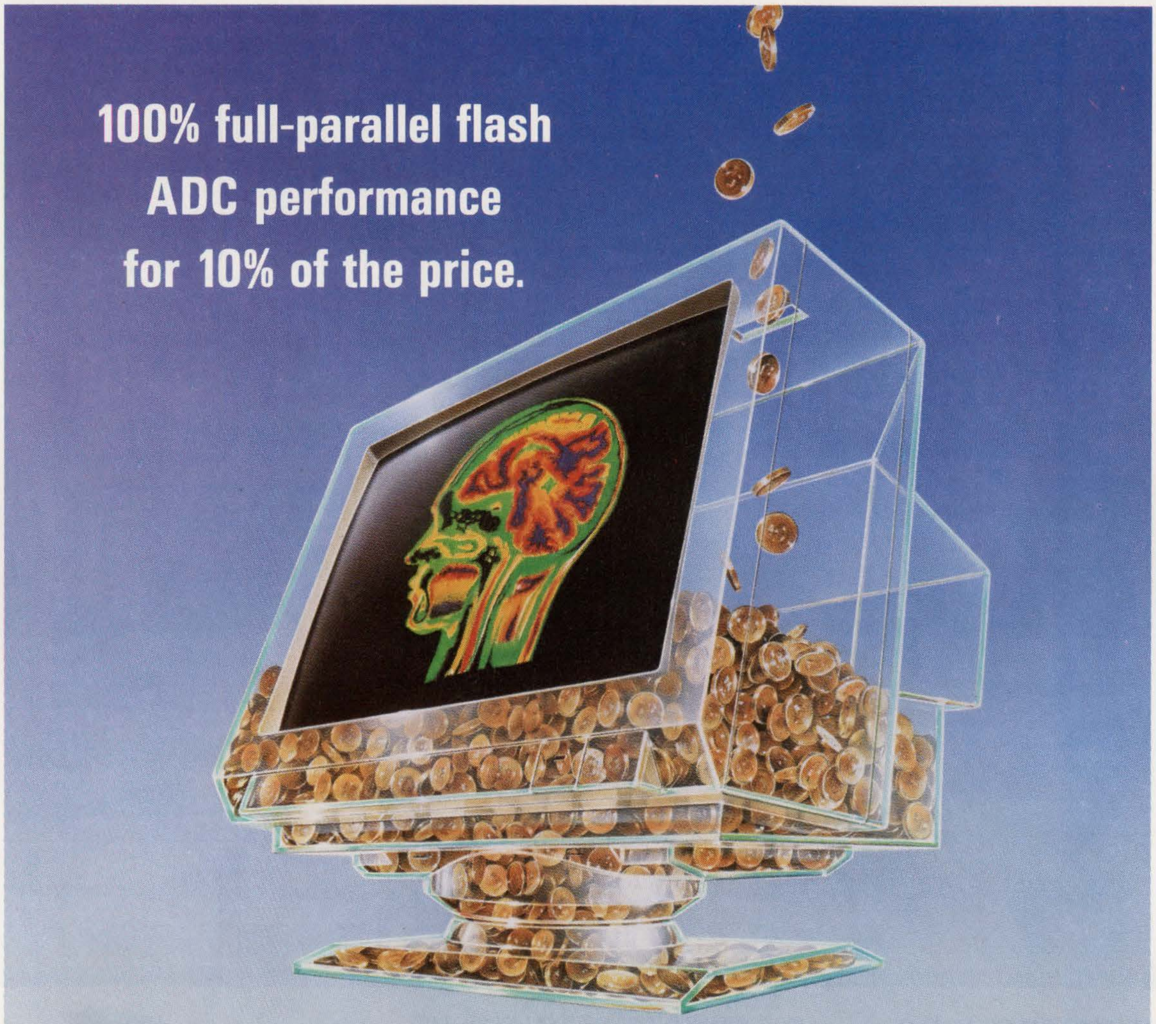
MODERATELY	545
SLIGHTLY	546



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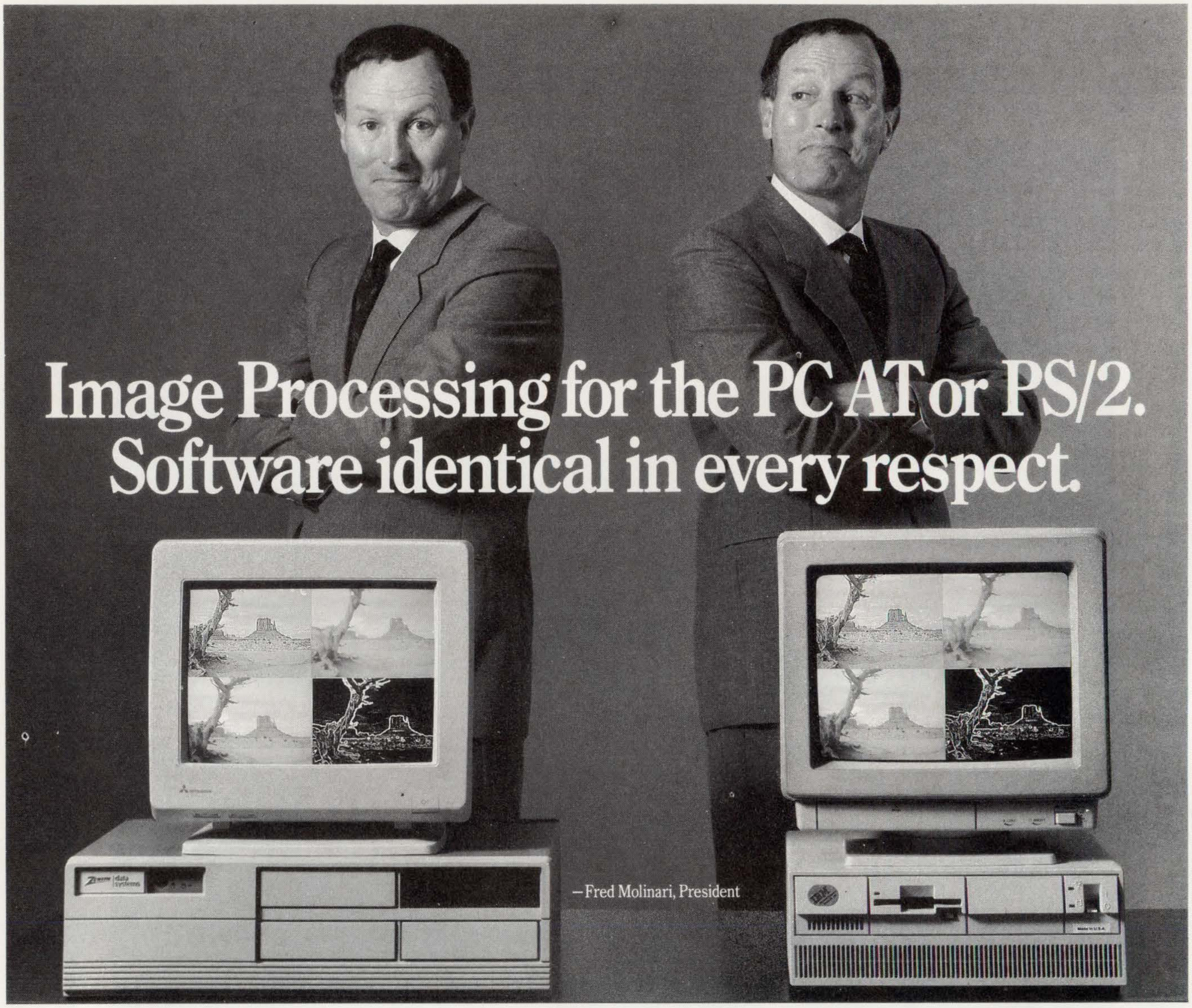

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The Best of '90

Once again, the editors of ELECTRONIC DESIGN select the best 100 products covered in the magazine's pages during the year. And, again, the most difficult part of the job is limiting the list to just 100. 1990 was an excellent year for innovative products introductions, and, in reviewing our pages, we found many other candidates that might have been included.

The product write-ups are organized into eight categories: digital semiconductors; analog; computer-aided engineering; power; test and measurement; computers, peripherals and boards; communications; and packaging and production.

For more details on any of "The Best of '90," refer to the issue in which it appeared. The issue date and page number are at the end of each product description.

This report was compiled by Dave Bursky, Frank Goodenough, Lisa Gunn, John Novellino, Milt Leonard, Richard Nass, and Dave Maliniak.

DIGITAL SEMICONDUCTORS

SCSI CONTROLLER MOVES DATA AT 10 MBYTES/S

A highly integrated SCSI controller, the AIC9110, contains a powerful command interpreter, programmable state-controller logic, buffer-management logic, and bus-interface drivers. Data transfers can take place at up to 10 Mbytes/s synchronous, 5 Mbytes/s asynchronous. An internal 48-word state-machine sequencer allows the chip to handle any peripheral control task. The CMOS chip comes in a 100-lead quad-sided flat package.

ADAPTEC INC., *691 S. Milpitas Blvd., Milpitas, CA 95035 (408) 945-8600 Electronic Design, Apr. 12, p. 195*
Circle 300

HIGH-DENSITY PLDS DON'T FORSAKE SPEED

The Mach 1 and Mach 2 families of electrically-erasable PLDs offers densities ranging from about 900 to 3600 equivalent gates. The chips have pin-to-pin worst-case delays of 15 ns, making it possible to use them in systems with clock rates of up to 50 MHz. The centralized switch matrix on each chip offers full communication between PAL blocks, receiving its inputs from all sources—dedicated inputs, input/output lines, and feedback paths from macrocells—and automatically routes appropriate signals to the PAL blocks. The smallest Mach 1, the model 110, comes in a 44-lead package.

ADVANCED MICRO DEVICES INC., *901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088-3000 (408) 732-2400; Electronic Design, Mar. 8, p. 105* **Circle 301**

ONE-CHIP PC MAKES BUILDING SYSTEMS A SNAP

Achieving close to the ultimate in integration for a personal computer's motherboard, the Am286ZX or LX high-integration microprocessors not only include the 80C286 central processor, but the DMA controllers, timer-counters, interrupt logic, DRAM controller, real-time clock, and EMS 4.0 support logic. Thus, with no other logic chips—just add memory and peripheral controllers—the new chip comes close to replacing the motherboard. Samples of the 286ZX or LX come in either 12- or 16-MHz grades; production will be in the second quarter of 1991.

ADVANCED MICRO DEVICES INC., *5204 E. Ben White Blvd., MS-522, Austin, TX 78741 (512) 462-4700; Electronic Design, Sept. 27, p. 40*
Circle 302

HIPPI CHIP SET HANDLES FULL CHANNEL CONTROL

The first chip set to offer simplex source and destination functions for the high-performance parallel interface (HiPPI)—the 32-bit S2020 and S2021—deliver an equivalent single-channel data rate of 800 Mbits/s. The S2020 accepts 32 bits of single-ended TTL data and delivers the same number of differential ECL signals, while the S2021 accepts the differential ECL signals and provides the 32 TTL channels. Dataflow control and diagnostic modes are included on both biC-MOS chips.

APPLIED MICROCIRCUITS CORP., *6195 Lusk Blvd., San Diego, CA 92121 (619) 450-9333; Electronic Design, June 28, p. 132* **Circle 303**

FLOATING-POINT MATH CHIP DELIVERS 200 MFLOPS

Containing a full 64-bit floating-point processor, the B3130 raises computational throughput to a new high—200 MFLOPS peak. The bipolar chip is optimized for vector operations, but can also deliver the fastest scalar throughput of any chip. In addition, on-chip circuits check incoming parity and generate parity for outgoing results. A scan path included on the chip allows all internal registers to be tied into a system or board-level scan ring for testing.

BIPOLAR INTEGRATED TECHNOLOGY INC., *1050 N.W. Compton Dr., Beaverton, OR 97006 (503) 629-5490; Electronic Design, Feb. 22, p. 51*
Circle 304

CHIP SET SIMPLIFIES MULTIPROCESSOR DESIGN

A five-chip set, the CS8239, eases the design of tightly coupled multiprocessor systems and directly supports the 80486 microprocessor. The five chips include a cache director comparator, a system control unit, a DMA controller, a processor data switch, and a cache control unit. A typical processor subsystem would require two data switch chips, one cache controller, a cache-directory comparator, and fast static memory. The remaining chips handle I/O operations and provide the interface to the main shared memory.

CHIPS AND TECHNOLOGIES INC., *3050 Zanker Rd., San Jose, CA 95134 (408) 434-0600; Electronic Design, Mar. 22, p. 125* **Circle 305**

SINGLE CHIP UPGRADES COLOR FLAT-PANEL DISPLAYS

By adding the GD6340 color LCD interface controller, a standard 8-color VGA-compatible LCD panel can produce as many as 256 simultaneous colors, radically improving image quality. The chip includes shading logic to generate LCD gray scales and color, a programmable interface that ties into most LCD panels, and the RAMDAC. A unique frame accelerator helps to store and transfer data from the shading-logic output to the LCD interface at an increased data-transfer rate for dual-panel displays—helping to minimize display flicker.

CIRRUS LOGIC INC., *1463 Centre Pointe Dr., Milpitas, CA 95035 (408) 945-8300; Electronic Design, July 28, P. 43* **Circle 306**

INDUSTRIAL CONTROL NET KEEPS NODES SIMPLE

Unlike data networks designed for high data throughput, the local operating network (LON) is designed for control applications. It consists of intelligent nodes, interconnected by communication media, and sharing a common, message-based communication protocol. Two basic chip types form a LON node—a Neuron processor and a media interface transceiver. Interface chips have been defined for various wiring and wireless media. The protocol is optimized for control applications—it handles short messages, multiple media types, and offers high reliability and message authenticity.

ECHELON SYSTEMS CORP., *4015 Miranda Ave., Palo Alto, CA 94034 (415) 855-7400; Electronic Design, Dec. 13, p. 129* **Circle 307**

MORE, NOT FEWER, CHIPS GIVE PCS FLEXIBLE OPTIONS

A family of more than a dozen chips from which designers can build PC motherboards gives system implementers unheralded flexibility to hit multiple system performance and price points. The chips tackle I/O bottlenecks by using a hierarchical bus structure that decouples the CPU subsystem and peripheral functions from the I/O channels. Part of that hierarchy is a special chip-level bus called the Advanced Chip Interconnect (ACI) bus, which improves the system modularity.

S3 INC., *2933 Bunker Hill Ln., Santa Clara, CA 95054; (408) 986-8144; Electronic Design, May 24, p. 79*
Circle 308

SPEEDY MEGABIT EEPROM DELIVERS ERROR-FREE DATA

The 28C010, a full-function EEPROM that accesses in 120 ns, provides 128 kbytes of data storage with on-chip error checking and correction to ensure that the data stays error free. The chip carries four extra bits with every byte to implement a modified Hamming code. In addition, a 128-byte page register improves the chip's store time by permitting up to 128 bytes to be loaded in at the read-access-time—120

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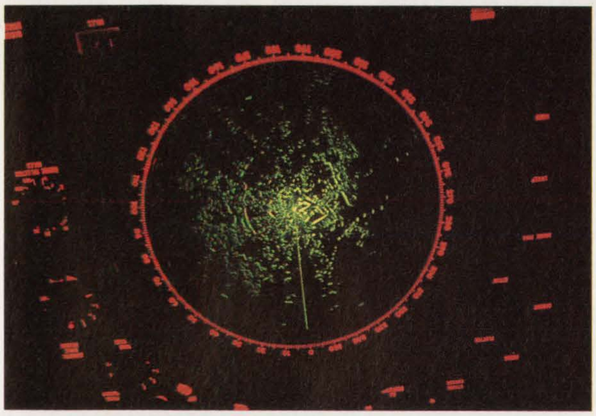
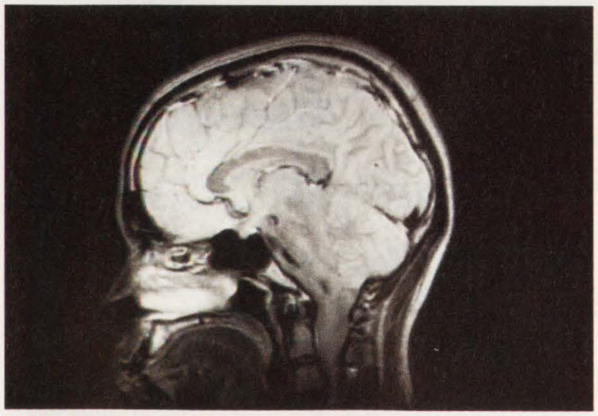


The use of the AD1382 is soaring in radar applications, thanks to its higher level of integration and guaranteed dynamic performance.



With its wide dynamic range and low noise, the AD1382 has a great image with people working in magnetic resonance imaging applications.

The AD1382 delivers guaranteed 100% production tested SNR, THD and peak distortion performance at three input frequencies and over two input ranges – testing that gives you the confidence to design for the best possible noise performance in your system.

You can also feel confident about the cost-effectiveness of the AD1382. It offers a higher level of integration with on-board track/hold and reference.

And since it's a single package, it's easier to design in and uses less board space than more expensive modular or multipackage solutions.

For a better picture of what the AD1382 can do for you, contact Analog Devices at 1-800-262-5643. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

AD1382

A 16-bit 500 kSPS SADC, the AD1382 provides excellent dynamic and static performance in a dual inline ceramic package.

Guaranteed (@25°C, ± 5 V input range):

SNR
- **5 kHz 90 dB min**
- **100 kHz 90 dB min**
- **200 kHz 88 dB min**

THD & Peak Distortion
- **5 kHz – 90 dB min**
- **100 kHz – 88 dB min**
- **200 kHz – 82 dB min**

DC specifications include:
0.0015% FSR INL, 0.0006% FSR DNL and NMC guaranteed to 16-bits

Other features include:
Zero offset autocalibration
± 5 V, ± 10 V Bipolar input range

An evaluation board for the AD1382 is available.

ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Offices and applications support available worldwide.

CIRCLE 110

DIGITAL SEMICONDUCTORS

ns/byte—and then store all of the bytes simultaneously in about 10 ms.

SEEQ TECHNOLOGY INC., *1849 Fortune Dr., San Jose, CA 95131 (408) 432-7400; Electronic Design, June 28, p. 125* **Circle 309**

GAAS GATE ARRAYS HIT 100,000+ GATES PER CHIP

The FX family of GaAs gate arrays offers designers as many as 100,000 usable gates per chip—the largest gate count to date on any family of GaAs gate arrays. Such a large number of gates now puts GaAs arrays on close to an even footing with biCMOS and ECL arrays for complexity and speed, while cutting the power consumption by 50% or more over that of ECL. The gates deliver 2 to 3X the performance of biCMOS and are price competitive with ECL.

VITESSE SEMICONDUCTOR CORP., *741 Calle Plano, Camarillo, CA 93010 (805) 388-3700; Electronic Design, Nov. 8, p. 152* **Circle 310**

RISC-BASED CONTROLLER ACCELERATES PAGE PRINTERS

The XL-8220 HyperScript processor integrates most system control and support functions required by laser and other page printers, permitting the area required by the subsystem to be cut by 67% over most current designs. Contained on the CMOS chip is a 32-bit proprietary RISC CPU that executes more than one instruction per cycle and efficiently executes Postscript or other page-description languages. Along with the processor and its 33-level return stack, the chip contains a 4-kbyte code cache, a two-word load-store queue, a DRAM controller, and a 4-kbit FIFO memory.

WEITEK CORP., *1060 E. Arques Ave., Sunnyvale, CA 94086 (408) 738-8400; Electronic Design, June 14, p. 103* **Circle 311**

CHIP SET SIMPLIFIES FUTUREBUS+ DESIGN

The first chip set solution to reduce the complexity of building Futurebus+ systems contains more than half-a-dozen biCMOS and bipolar chips. Those chips perform all of the bus communication functions—bus arbitration (FB2010), protocol control (FB2000), packet data buffering (FB2020), as well as address, data and tag buffering, and bus interfacing. Thus, a typical Futurebus+ interface can be reduced to about 8 in.^{2}—about one-third the board space general-purpose logic chips.

PHILIPS COMPONENTS-SIGNETICS CO., *811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409 (408) 991-2000; Electronic Design, May 10, p. 63* **Circle 312**

DIGITAL COMM ICS TACKLE TOUGH APPLICATIONS

Tackling such demanding applications as digital sonar and radar systems, as well as secure communications systems, the PDSP16256 digital filter and the PDSP16350 amplitude-and-phase-modulator operate at sampling rates up to 20 MHz. The 16256 is a programmable, variable-length finite-impulse-response filter. By multicycling the data, the chip can provide from 16 to 128 filter stages. The 16350 is a direct digital synthesizer and is the first chip to pack an I/Q splitter that performs quadrature heterodyning to obtain the in-phase and quadrature components of a waveform.

PLESSEY SEMICONDUCTORS CORP., *1500 Green Hills Road, Scotts Valley, CA 95066 (408) 438-2900; Electronic Design, Sept.27, p. 189* **Circle 313**

ENHANCED SCSI PROCESSOR UPS SYSTEM PERFORMANCE

Enhancements enable the 53C710 to serve as a superset of the previously released 53C700 SCSI Scripts processor. The new chip executes, without processor intervention (except at the end of an I/O operation), multithreaded I/O algorithms, such as the ones found in workstation and file-server environments. Another feature is a 32-bit bus-master DMA channel capable of 80-Mbyte/s data transfers (about 50% faster than the previous chip). The chip also has a byte-ordering control pin that swaps the byte order to match the word structure of the host processor.

NCR MICROELECTRONICS INC., *1635 Aeroplaza Dr., Colorado Springs, CO 80916 (719) 596-5795; Electronic Design, Sept.13, p. 101* **Circle 314**

PIPELINED CISC PROCESSOR EXCEEDS RISC THROUGHPUT

Dual on-chip caches, an integrated floating-point unit (FPU), and improved instruction efficiencies let the 68040 microprocessor deliver between 19 and 21 MIPS—nearly triple the throughput of its 32-bit predecessor, the 68030. The on-chip FPU delivers 3.5 MFLOPS of sustained throughput (double-precision). Both the 4-kbyte instruction and data caches have 4-way set associativity. They're coupled with a write buffer and twin memory-management units, cache refill time can be kept minimal, as can the chance of a pipeline stall.

MOTOROLA INC., *Microprocessor Products Group, 6501 William Cannon Dr. W., Austin, TX 78735-8598 (512) 891-2839; Electronic Design, Jan. 25, p. 91* **Circle 315**

TRIPLE-PORT DYNAMIC RAM ACCELERATES DATA MOVES

By adding a second, independent serial access port to a standard dual-ported video-RAM chip, the MT43C4257 triple-port memory opens up new applications in video imaging, networking, disk control, and DSP subsystems. The CMOS memory has a standard 256-kword-by-4-bit RAM interface and two 512-word-by-4-bit serial access ports. Each port operates independently and asynchronously. Each serial port can transfer data bidirectionally at 25 ns/nibble, while the DRAM port requires 80 ns per access.

MICRON TECHNOLOGY INC., *2805 East Columbia Rd., Boise, Idaho 83706 (208) 368-4000; Electronic Design, May 24, p. 37* **Circle 316**

ELIMINATE SIGNAL SKEWS WITH GAAS CLOCK CHIPS

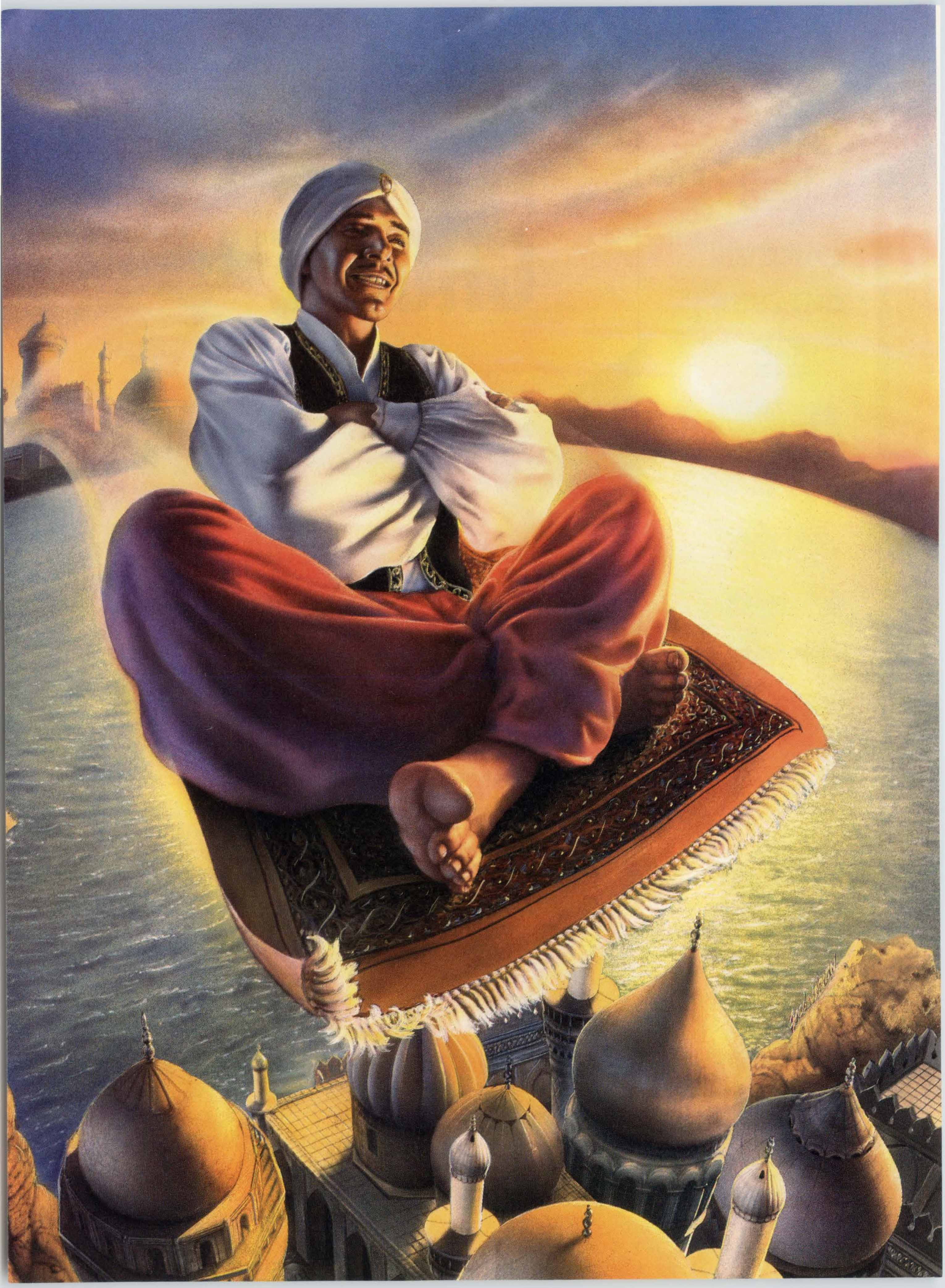
A pair of GaAs-based chips offer flexible and programmable control of TTL timing-signal edges for systems with clock frequencies of from 25 to 50 MHz, or provide double-frequency clocks of up to 100 MHz, both with signal skews of less than 500 ps. The GA1110 generates up to five clocks that are phase- and frequency-synchronized to a master clock, and can adjust the clock edges in 2-ns steps. The GA1210 delivers multiple low-skew clocks at twice the frequency of the input clock; 1X clocks are also generated. All are phase-aligned to the master clock. Both chips come in 16-pin DIPs and are available from stock. Commercial-temperature-range versions of the 25- and 33-MHz grades sell for $28.50 in 1000-unit loads.

GAZELLE MICROCIRCUITS INC., *2300 Owen St., Santa Clara, CA 95054 (408) 982-0900; Electronic Design, Aug. 9, p. 39* **Circle 317**

COMM-TARGETED DSP ICS RENDER TOP THROUGHPUT

A digital decimation filter (the HSP43220) and a combination numerically controlled oscillator and modulator (the HSP45116) handle the filtering and tuning operations of communications systems. The chips form the heart of a digital receiver with an out-of-band attenuation of 96 dB and a tuning accuracy of 0.006 Hz (30-MHz sampling rate). With the two CMOS chips, applications such as i-f channels for satellite data links, radar and sonar data gathering, narrowband spectrum analysis, and others can be simplified.

HARRIS SEMICONDUCTOR CORP., *1301 Woody Burke Rd., Melbourne, FL 32902 (407) 724-3868; Electronic Design, Oct. 25, p. 117* **Circle 318**



DIGITAL SEMICONDUCTORS

HIGHLY INTEGRATED RISC CPU PACKS I/O AND CACHE

The LR33000 CMOS Mips-compatible RISC processor from LSI Logic combines the equivalent of about 20 chips into one device that can reduce system size, power, and cost. Along with the R3000-compatible integer processor, the chip includes an 8-kbyte instruction cache, a 1-kbyte data cache, a dynamic-RAM refresh controller, three counter-timers, a one-word-deep write buffer, and other features. Versions of the CPU will operate at 25, 33, or 40 MHz, and consume a maximum of 2 W at 25 MHz.

A second family of integrated Mips-compatible processors, the R3051 and 3052 from Integrated Device Technology, also offer on-chip caches. However, by multiplexing the address and data buses designers have cut the pin count to 84 leads. The R3051 packs separate 4-kbyte instruction and data caches, and the R3052 has double the instruction cache.

LSI LOGIC CORP., *MIPS Div., 1525 McCarthy Blvd., Milpitas, CA 95035 (408) 954-4789; Electronic Design* **Circle 319**

INTEGRATED DEVICE TECHNOLOGY INC., *3236 Scott Blvd., Santa Clara, CA 95052 (408) 492-8631; Electronic Design, Oct. 25, p. 106* **Circle 320**

OPTIMIZED CPUS TACKLE IMAGING, COMMUNICATIONS

A trio of 32-bit CPUs optimized for various multimedia applications simplify the design of such systems as page printers, digital copying machines, fax systems, and graphics terminals. The NS32CG160 includes a 16-bit multiplier to accelerate integer calculations, dual 8-bit DMA control channels, an interrupt controller, three counter-timers, and enhanced instructions for image manipulation. The 32FX16 includes a block optimized for DSP functions, while the 32GX320 is a big brother of the CG160 and has 32-bit DMA controllers, a 512-byte instruction- and a 1024-byte data-cache.

NATIONAL SEMICONDUCTOR CORP., *2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090 (408) 721-5000; Electronic Design, May 24, p. 76* **Circle 321**

FAST MATH, ON-CHIP CACHES SUIT SPARC FOR CONTROL

The Sparclite CPU, the first Sparc RISC processor designed specifically for embedded control applications, contains many system functions that were previously separate chips. One chip includes instruction and data caches, a dynamic-RAM controller, and an enhanced integer processor. A support chip contains the interrupt controller, multiple counter-timers, and two serial ports. The processor has new Multiplication, Division and Scan instructions that speed many time-consuming control and math-based algorithms.

FUJITSU MICROELECTRONICS INC., *Advanced Products Div., 50 Rio Robles, Bldg. 3, M/S 356, San Jose, CA 95134-1806 (408) 922-9722; Electronic Design, November 8, p. 57* **Circle 322**

VIDEO-ARRAY PROCESSOR BREAKS SPEED RECORD

A CMOS processor that can deliver a peak performance of 4 billion operations/s promises to simplify the image processing required in image data compression, television, and other systems. The Datawave chip has a sustained throughput of 750 Mbytes/s through the use of a 125-MHz clock and 16 pipelined superscalar 12-bit RISC processors on the chip all working in parallel. The chip is general-purpose and has programmable data paths.

ITT INTERMETALL GMBH, *P.O. Box 840, D7800 Freiburg, Germany; (0049) 761-5170. In the U.S., contact ITT Semiconductors, 55 Merrimack St. P.O. Box 749, Lawrence, MA 01843; (508) 688-1881; Electronic Design, July 12 p. 133* **Circle 323**

ANALOG

FIRST DELTA-SIGMA DAC RESOLVES 18-BITS

Delta-sigma a-d converters have become main-stream. Now there's a d-a converter that employs a similar architecture—the CS4328, a dual 18-bit device for digital audio. Thus, it offers a low-cost high resolution DAC that can update at 50 kHz. Moreover, its serial output is a natural for DSP applications. Like many delta-sigma ADCs, it uses two chips, one for the analog circuits in 3-μm CMOS, and one for the digital in 1.5 μm CMOS.

CRYSTAL SEMICONDUCTOR CORP., *P.O. Box 17847, Austin, TX 78760 (512) 445-7222; Electronic Design, August 23, p. 51* **Circle 324**

DSP PROCESSES ANALOG SIGNALS ACCURATELY

Analog signals can be processed with digital accuracy by adding a 16-bit a-d and a 16-bit d-a converter to a powerful digital signal processor. Application areas include telecom systems, such as digital cellular radio, passive sonar systems for the military, vibration monitoring systems and noise cancellation. The chips can perform spectrum analyisis, auto- and cross-correlation and ultraprecise filtering. The DAC can generate a wide range of test and simulation signals.

ANALOG DEVICES INC., DIGITAL SIGNAL PROCESSING DIV., *P.O. Box 9106, Norwood, MA 02062-9106 (617) 481-3074; Electronic Design, April 12, p. 40* **Circle 325**

DACS AND ADCS TIE TO DSPS WITHOUT GLUE LOGIC

Typical DACs and ADCs take between one and three dozen glue-logic chips to tie to a typical general purpose digital signal processor. Burr-Brown has taken its 18-bit dual audio DAC IC and ADC IC and put each in a plastic DIP with a gate array—the DSP202 and DSP102, respectively. Each device links with the four most common DSP families (TMS320, DSP32, DSP56001, ADSP2101) without any glue logic. Because they're designed for audio use, the converters carry the dynamic specifications needed for DSP applications.

BURR-BROWN CORP., *P.O. Box 11400, Tucson, AZ 85734 (800) 548-6132; Electronic Design, November 8, p.159* **Circle 326**

16-BIT ADCS SAMPLE AT 500 KHZ AND 1 MHZ

Hybrid, 16-bit a-d cnverters, long thought of as belonging strictly in the realm of low-frequency signal handlers, for example process control applications, have joined the real world of dynamic signals. Datel's chip-and-wire hybrid, the ADS-930, samples 250-kHz sine waves at 500 kHz (Nyquist). Analogic's somewhat larger surface-mount hybrid module doubles those frequencies. Applications for these converters range from infrared imaging systems for the military to medical scanners.

DATEL INC. *11 Cabot Blvd., Mansfield, MA 02048-6356 (508) 339-3000* **Circle 327**
ANALOGIC CORP. *360 Audubon Rd., Wakefield, MA 01880 (508) 977-3000* **Circle 328**; *Electronic Design, September 13, p.37.*

INSTRUMENTATION AMPS GET PRECISION, SPEED

Although the instrumentation amplifer (IA) goes back to vacuum tube days, up to now they've never been chopper stabilized. However, the LTC1100 fills that void. It offers an offset voltage drift of just 0.1 μV/°C. The JFET input LT1102 is both the fastest IC IA and offers the lowest bias current—21 V/μs and 40 pA, respectively. Both IAs can operate from a single-supply rail, are packaged in 8-pin DIPs and have jumper-selectable gains of 1 and 10.

LINEAR TECHNOLOGY CORP., *1630 McCarthy Blvd., Milpitas, CA 95035-7487 (408) 432-1900; Electronic Design June 28, p. 111* **Circle 329**

8-INPUT WATCHDOG IC MONITORS SYSTEMS

A watchdog chip, the ADC0858, can monitor the performance of eight system-voltages to 8-bit accuracy. It has an eight-input multiplexer, an eight-bit ADC, a 16-by-8 RAM, a serial host interface and miscellaneous logic. High and low limits for each input are stored in RAM. The circuits continuously scan and digitize the 8 inputs and compare their results with the values in RAM. If the limits are exceeded, the host is notified. It then polls the chip to determine which channels crossed the limits and by how much. The input multiplexer can be programmed for any mix of single- or double-ended inputs.

NATIONAL SEMICONDUCTOR CORP., *P.O. Box 58090, Santa Clara, CA 95052-8090 (408) 721-5307; Electronic Design, July 12, p. 129* **Circle 330**

VARIABLE VOLTAGE TUNES LINEAR FILTER

Until now, if a programmable filter was desired, it usually wound up being noisy switched capacitor techniques offering a maximum signal frequency of about 150 kHz. However, the IMP4250 7-pole bessel low-pass circuit is a voltage-programmable, linear time filter that handles input frequencies to 13 MHz. Each stage consists of an op-amp integrator in which the input resistor consists of a MOS transistor. Changing the voltage on the gate of the FET changes its resistance, and the circuit's bandwidth. For most applications, just one external frequency source can be used for all four phase-locked loops.

INTERNATIONAL MICROELECTRONIC PRODUCTS INC., *2830 N. First St., San Jose, CA 95134 (408) 432-9200; Electronic Design, February 8, p. 43* **Circle 331**

10-BIT ADCS CONVERT IN UNDER 0.5, 2.5 MS

A pair of 10-bit ADCs sport two-step architectures derived from the classic 0820 8-bit ADC: The MAX151 and MP7695 convert in 0.5 and 2.5 μs, respectively. Micro Power Systems' MP7695 is the faster, but its sampling is limited to signals below 10 kHz and ac specifications aren't available. Maxim's 151, on the other hand, can sample signals approaching Nyquist and provides ac specifications. The MAX 151 also has a reference, but needs 275 mW. The MP7695 needs just 25 mW of supply power.

MAXIM INTEGRATED PRODUCTS INC., *120 San Gabriel Dr., Sunnyvale, CA 94086 (408) 737-7600* **Circle 332**

MICRO POWER SYSTEMS INC., *P.O. Box 58090, Santa Clara, CA 95054-0965 (408) 727-5350* **Circle 333**; *Electronic Design, October 11, p. 121*

ANALOG ICS TARGET TESTER PIN CIRCUITRY

Users of digital IC testers are demanding higher testing speed in order to economically handle ever higher IC pin counts. In addition, they're demanding the ability to handle clock rates to 200 MHz. A solution may lie in two families of analog ICs for the pin-electronic circuits now filled by hybrids. One family is from Brooktree, the other from Analog Devices. Each family includes pin drivers, dynamic loads, high-speed comparators, and variable solid-state delay lines for deskewing test signals.

BROOKTREE CORP., *9950 Barnes Canyon Rd., San Diego, CA 92121 (619) 452-7580* **Circle 334**

ANALOG DEVICES INC., *831 Woburn St., Wilmington, MA 01887 (617) 937-1590* **Circle 335**; *Electronic Design, June 14, p. 91.*

CIRCLE 116

ANALOG

10-BIT ADCS SAMPLE SIGNALS TO 150 kHz

The ML2271 from Micro Linear and the ADC10061 from National are 10-bit ADCs with conversion times of 1.45 and 0.9 μs, respectively. The former uses a three-step design; the latter a two-step. Both are true samplers that can grab signals above 150 kHz to 10-bit accuracy and provide the dynamic specifications needed by DSP applications. Their 20-pin DIPs share similar pinouts and both need only a 5-V supply rail, so potentially they're interchangable. Two- and four-input versions of the ADC10061 are also available.

MICRO LINEAR CORP., *2092 Concourse Dr., San Jose, CA 95131 (408) 433-5200* **Circle 336**

NATIONAL SEMICONDUCTOR CORP., *P.O. Box 8090, Santa Clara, CA 95052-8090 (408) 721-2273* **Circle 331**; *Electronic Design, October 11, p. 121*

12-BIT ADC SAMPLES AT 20 MHZ, A 14-BIT AT 10

Ultra-fast, high resolution a-d converters have come of age. Pushed first by the military to capture radar threat signals, these ADCs are now finding applications ranging from digital oscilloscopes to CAT scanners. Moreover, they're all sampling devices, providing both ac and dc specifications. Comlinear's 12-bit CLC936 grabs 10-MHz sine waves at 20 MHz. Analog Devices 14-bit AD9014, designed for telecommunications applications, samples inputs at 10 MHz. The 12-bit device is a single hybrid, while the 14-bit is configured as a pair of hybrids on a pc board.

COMLINEAR CORP. *4800 Wheaton Dr., Fort Collins, CO 80525 (303) 226-0500* **Circle 338**

ANALOG DEVICES. *P.O. Box 9106, Norwood, MA 02062-9106 (919) 668-9511* **Circle 339**; *Electronic Design, September 13, p. 37.*

LINEAR TIME FILTER IS VOLTAGE PROGRAMMABLE

While aimed at high-end disc-drive read-channel circuits, a voltage-programmable linear time filter can be adapted to other applications. The 32F8010 is a 7th-order, Bessel low-pass design and can handle inputs to 100 MHz. It employs a technique called G_m/C. A dc voltage at one input of an analog multiplier varies the effective RC time constant of the multiplier's output/load-impedance, in turn setting the bandwidth seen by the multiplier's signal input.

SILICON SYSTEMS INC., *14351 Myford Rd., Tustin, CA 92680 (714) 731-7110; Electronic Design, February 8, p. 43* **Circle 340**

COMPUTER-AIDED ENGINEERING

FRAMEWORK LINKS TOOLS FOR MIXED A/D SIMULATION

Two mixed-signal simulators, one for ICs and one for systems, were created by linking a logic simulator with two analog simulators. For ICs, Cadence mixed its Verilog digital simulator with its Spice simulator. For systems, it mixed Verilog with Analogy's Saber simulator. Both combinations were linked through the Cadence framework. In addition, the tools are tightly coupled through a communication system. Cadence Spice/Verilog is integrated into the company's Analog Artist system, while Saber/Verilog is a standalone tool.

CADENCE DESIGN SYSTEMS INC., *555 River Oaks Pkwy., San Jose, CA 95134 (408) 943-1234; Electronic Design, Aug. 23, p. 103* **Circle 341**

VHDL TOOLS ADDRESS SIMULATION, ANALYSIS

The SimPlus design tools address simulation and analysis in VHDL design. The SimPlus System Designer is a set of analysis and software tools. Its behavioral environment accepts full VHDL as its primary input. The SimPlus Model Developer supports the writing and debugging of models created from any VHDL construct. The SimPlus ASIC Designer is a gate-level environment for ASIC engineers. And the SimPlus Universal Designer combines the features of all three.

ZYCAD CORP., *1380 Willow Rd., Menlo Park, CA 94025 (415) 688-7400; Electronic Design, June 14, p. 56 (Now available from Synopsys Inc., 1098 Alta Ave., Mountain View, CA 94043 (415) 962-5000* **Circle 342**

SIMULATOR MIXES VHDL, GATE-LEVEL MODELS

The QuickSim II logic simulator is used for function and performance verification of large, submicron ASICs and complex pc-board designs. The key to the package's fast, accurate simulation is the development of sophisticated simulation algorithms and advanced modeling techniques. Modeling methods include support for any combination of VHDL, hardware, behavioral, and gate-level models, and Mentor Graphic's advanced modeling process. That process supports timing equations for submicron accuracy.

MENTOR GRAPHICS CORP., *8500 S.W. Creekside Pl., Beaverton, OR 97005 (503) 626-7000; Electronic Design, June 14, p. 41* **Circle 343**

SOFTWARE SIMULATES A HARDWARE PROTOTYPE

Using the MultiSim Interactive Designer schematic-capture and simulation package, pc-board designers can perform in software many activities they've traditionally done with hardware prototypes. In addition, the Interactive Designer's simulation and worst-case timing analysis identify errors that board designers can't find with prototypes. Based on simulation results, engineers can add and delete components and make cuts and jumps, all directly on the schematic.

TERADYNE INC., *321 Harrison Ave., Boston, MA 02118 (617) 482-2700; Electronic Design, June 28, p. 45* **Circle 344**

FAST, ACCURATE SIMULATOR TAKES ON SUBMICRON ASICS

Submicron ASICs and high-speed board designs are no problem for the RapidSim digital simulator. RapidSim has one of the highest levels of modeling accuracy of any standard logic simulator. The simulator has the speed and capacity needed for large gate-level simulations. ASIC vendors can customize the simulator's modeling equations to define technology-dependent delay characteristics specific to their silicon process. The tool also works within the company's Logic Workbench framework.

VALID LOGIC SYSTEMS INC., *2820 Orchard Pkwy., San Jose, CA 95134 (408) 432-9400; Electronic Design, Apr. 12, p. 183* **Circle 345**

SOFTWARE ANALYZES POWER DEMANDS FOR DIGITAL ICS

The need for a fast, accurate method of calculating power-related parameters sparked the development of the PowerMill analysis tools. PowerMill analyzes power requirements for CMOS and biCMOS digital circuits. Designers can now predict such problems as current surges and electromigration. The tool can display instantaneous current through power and ground for any transistor or functional block, or for the entire chip. It can also display instantaneous voltage for every signal node.

EPIC DESIGN TECHNOLOGY INC., *2900 Lakeside Dr., Suite 205, Santa Clara, CA 95050 (408) 988-2944; Electronic Design, Apr. 26, p. 129* **Circle 346**

FRAMEWORK EASES TOOL ENCAPSULATION

The Integrator, an independent framework, neatly meshes computer-aided engineering (CAE) tools and other software packages in a networked environment. The framework, which uses object-oriented database technology, manages workflow through automatic tool sequencing and a point-and-click user interface. Tools are quickly tied into the system using the Tool Encapsulator, which simplifies tool integration with a graphical editor and data templates that instruct the user.

INTERACT CORP., *417 Fifth Ave., New York, NY 10016 (212) 696-3700; Electronic Design, July 26, p. 75* **Circle 347**

GRAPHICAL, INTERACTIVE TOOL DEBUGS VHDL MODELS

A graphical, interactive user interface is a key feature to the Debug 1076 VHDL debugging tool. It improves designer productivity by quickly isolating modeling problems. The menu-driven package includes convenient button icons for commonly used commands. In addition, the debugger supports the design concurrency that's characteristic of VHDL. Breakpoints can be set for subprocesses, subprograms, source-code line numbers, or for simulation time points generated by the main simulation.

VANTAGE ANALYSIS SYSTEMS INC., *42840 Christy St., Suite 201, Fremont, CA 94538 (415) 659-0901; Electronic Design, June 14, p. 56* **Circle 348**

ASIC TOOL GENERATES DATA PATHS FROM VHDL

With the ASIC Synthesizer, engineers can take a hardware-description-language representation of a design and convert it to layout silicon. That's because the tool can synthesize a chip's logic from behavioral descriptions, and it automatically generates any required data paths from behavioral description. The data paths are synthesized as minimum-area blocks that are consistent with the necessary performance constraints. The ASIC Synthesizer accepts both Verilog and VHDL.

VLSI TECHNOLOGY INC., *1109 McKay Dr., San Jose, CA 95131 (408) 434-3000; Electronic Design, June 14, p. 55* **Circle 349**

DESIGN TOOLS TACKLE PROJECTS IN PARALLEL

Concurrent design is now possible with the Concurrent Design Environment (CDE), which combines all design tools and data into one continuous, flexible process. CDE is built on the Falcon Framework, industry standards, and the entire suite of Mentor Graphics' design tools. Across all disciplines, the new concurrent environment supports every level of system design throughout the entire design cycle. A dataflow engine that uses a spreadsheet-like interface enables engineers to create their own software applications.

MENTOR GRAPHICS CORP., *8500 S.W. Creekside Pl., Beaverton, OR 97005 (503) 626-7000; Electronic Design, Apr. 12, p. 201* **Circle 350**

ONE TOOL VERIFIES SYSTEM AND SOFTWARE

Teamwork/SIM is a system and software simulator that tightly couples real-time simulation with the company's teamwork family of computer-aided software engineering (CASE) tools. The simulator makes it possible for users to analyze system behavior (hardware and software) well in advance of costly prototypes. Engineers can interactively create graphical structured analysis and real-time models, and then animate these models to verify behavior and estimate system performance early in the design cycle.

CADRE TECHNOLOGIES INC., *222 Richmond St., Providence, RI 02903 (401) 351-5950; Electronic Design, Nov. 22, p. 57* **Circle 351**

OBJECT-ORIENTED DATABASE FILLS ENGINEERING NEEDS

Designed for engineering applications, the Objectivity/DB database management system (DBMS) combines object-oriented design principles with advanced database features. The database system consists of several subsystems integrated in a layered architecture. All types of Objectivity/DB, which is targeted at design-automation tools, can fill the requirements for compatibility among tools that share data. It models complex data structures and relationships, and also supports dynamically varying data size.

OBJECTIVITY INC., *800 El Camino Real, Menlo Park, CA 94025 (415) 688-8000; Electronic Design, Apr. 12, p. 189* **Circle 352**

HARDWARE MODELER EXPLOITS CONCURRENCY

The CATS simulation server is a networked platform that combines Sun Microsystems' Sparcserver 330 RISC machine with Racal-Redac's innovative hardware-modeling technology for quick simulation of complex systems. The new hardware-modeling technology uses ECL gate arrays and 1-Mbyte memories. It concurrently runs multiple hardware models and software that share hardware-model memory. At the same time, it ensures the accuracy of worst-case timing analysis. The hardware server runs the Cadat 2000 simulator.

RACAL-REDAC INC., *1000 Wyckoff Ave., Mahwah, NJ 07430 (201) 848-8000; Electronic Design, June 28, p. 115* **Circle 353**

VHDL SYSTEM TAKES USERS FROM CONCEPT TO SILICON

Moving designers from concept to silicon under one umbrella, the Silicon 1076 VHDL environment tackles high-level design of ASICs. The components of the environment include source-code entry, a native simulator and debugger, synthesis, analysis and sign-off tools, and libraries with test benches. Among the major features are a master environment and user interface; a design-flow methodology with "what-if" analysis; and access to LSI Logic's technologies, software tools, and databases.

LSI LOGIC CORP., *1501 McCarthy Blvd., Milpitas, CA 95035 (408) 433-6801; Electronic Design, June 14, p. 51* **Circle 354**

VHDL SYNTHESIS MESHES WITH CAE ENVIRONMENT

VHDL synthesis is tightly integrated into Viewlogic's Workview series of CAE tools with the addition of Viewdesign. It consists of the VHDL Designer logic-synthesis tool and the Viewgen schematic generator. Viewdesign makes it possible for designers to bypass gate-level design work. The Viewdesign synthesis environment uses native VHDL for both synthesis and simulation. With the tool, users can combine structural logic with synthesized VHDL descriptions on one schematic.

VIEWLOGIC SYSTEMS INC., *293 Boston Post Rd. West, Marlboro, MA 01752-4615 (508) 480-0881; Electronic Design, June 14, p. 52* **Circle 355**

POWER

RUGGED ON-LINE UPS SYSTEM CAN HANDLE BROAD INPUT

Combining a BCE battery charger-power supply with its ACE sine-wave inverter, an on-line ruggedized UPS handles a broad range of input voltages and line disturbances. Extended brownout conditions as low as 83 V and frequency fluctuations from 40 to 440 Hz pose no problems. Neither do inputs from 90 to 250 V. The inverter generates a sine wave with less than 1% total harmonic distortion. Its fixed-frequency output is crystal-controlled to better than 0.1% stability.

TRANSISTOR DEVICES INC., *85 Horsehill Rd., Cedar Knolls, NJ 07927 (201) 267-1900; Electronic Design, Aug. 9, p. 128* **Circle 356**

RELIABILITY, POWER DENSITY SPUR DC-DC CONVERTER

Although it doesn't break ground in terms of converter topology, the UHD-150 series of dc-dc converters represents breakthroughs in mechanical and packaging design that yield power densities of up to 36 W per

POWER

cubic inch. The forward-converter devices incorporate a "pseudo-current-mode" control technique that provides precise (0.02%) output-voltage regulation. Military components are used throughout.

LAMBDA ELECTRONICS, *515 Broad Hollow Rd., Melville, NY 11747 (800) 526-2324; Electronic Design, Apr. 26, p. 117* **Circle 357**

SWITCHING REGULATOR BOASTS 200-W/IN.³ DENSITY

Efficiency of better than 90%—without a heat sink—and power densities of up to 200 W per cubic inch are featured in a 1.5-A line of three-terminal integrated switching regulators. The 1-MHz devices, which include an inductor as well as short-circuit and over-temperature protection, are as easy to use as any three-terminal linear regulator. Thanks to their small size, (0.85-by-0.85-by-0.25 in.), they easily fit into tight spots and are available in surface-mounted packages.

POWER TRENDS INC., *1020 Carolina Dr., West Chicago, IL 60185 (708) 231-5505; Electronic Design, March 22, p.137* **Circle 358**

DESIGN CUSTOM BICMOS POWER/HIGH-VOLTAGE ICS

To date, there's been only one option for a personalized high-voltage or power IC—a full custom chip. However Harris, in a joint program with its customer IBM, has developed the HPA1000 library of standard cells for just that purpose. Now in beta sites, it will soon be generally available. The 4-μm double-metal, single polysilicon bipolar-MOS process builds 16-V bipolar and CMOS transistors, and 60-V DMOS devices that can switch 20 A. Moreover, one chip can carry more than one power device.

HARRIS CORP, SEMICONDUCTOR SECTOR, *P.O. Box 13996, Research Triangle Park, NC 27709 (919) 361-1603; Electronic Design, July 12, p. 43* **Circle 359**

CONVERTER AND FILTER PAIR GET MIL-STD-883C NOD

With its process certified to MIL-STD-883C standards, the MHF dc-dc converter and FMC-461 emi filter give designers the reliability of military components. The 883C-certified tandem dramatically increases tolerance to temperature extremes and acceleration. Input range for the converter is 16 to 40 V dc. It produces closely regulated outputs of 5, ±12, or ±15 V dc in single or dual configurations up to a maximum output of 12 W. The package takes up just 1.6 in. square of board space.

INTERPOINT CORP., *P.O. Box 97005, Redmond, WA 98073-9705 (206) 882-3100; Electronic Design, Aug. 9, p. 128* **Circle 360**

SWITCHING-REGULATOR IC FITS IN WALL PLUG

A complete 3-W PWM switching power supply, built with the PWR-SMP3 IC, can run off the 115 V rectified ac line, and is small enough to fit in an ac line plug. The CMOS chip contains a complete controller with an off-line pre-regulator, reference, clock, protection circuitry, and the 200 V/16 Ω switch. It takes just a few diodes and a handful of passive parts to build the supply. The chip comes in a 16-pin power DIP. A similar chip rated at 20 W off the 115 V line, and another rated at 10 W off the 220 V line are now available.

POWER INTEGRATIONS INC., *411 Clyde Ave., Mountain View, CA 94043 (415) 960-3572; Electronic Design, March 22, p. 35* **Circle 361**

100-W DC-DC CONVERTERS BOOST DISTRIBUTED POWER

The concept of distributed power is now practical in systems calling for more than 50 to 100 W of power, thanks to the MiniMod family of dc-dc converters. The 2.75-in.³ devices can convert, regulate, and put out 25 to 100 W of dc at from 2 to 95 V. Output currents range from 20 A at 2 V to 1 A at 95 V; typical efficiency runs 85%. The supplies' high density results from rigorous packaging engineering combined with careful component selection and downsizing of the largest parts.

VICOR CORP., *23 Frontage Rd., Andover, MA 01810 (508) 470-2900; Electronic Design, Jan. 25, p. 29* **Circle 362**

SAVE LIVES WITH GROUND FAULT INTERRUPTER

Underwriters Laboratories has edicted that all hair dryers sold in the U.S. after 1990 must contain GFIs (ground fault interrupters). They open the ac line to the dryer in less than 24 ms if the appliance is dunked in water. A low-cost IC GFI, the RV4140, can be embedded in the line cord with a few passive parts, saving expensive alterations to dryers.

RAYTHEON COMPANY, SEMICONDUCTOR DIV., *350 Ellis St., Mountain View, CA 94039-7016 (415) 968-9211; Electronic Design, October 25, p. 101* **Circle 363**

TEST AND MEASUREMENT

SOFTWARE WRITES VECTORS FOR SEQUENTIAL LOGIC

Test Design Expert (TDX) generates test vectors automatically for combinatorial logic and for sequential circuits. To do so, TDX employs both a structural description of the circuit, the net list, and a behavioral description written in VHDL-T, a register-transfer level subset of the VHDL 1076 standard. As an open system, TDX works with any design methodology, CAE software, foundry process, or test equipment, and with or without any design-for-testability scheme.

EXPERTEST INC., *2101 Landings Dr., Mountain View, CA 94043 (415) 969-0701; Electronic Design, May 10, p. 119* **Circle 364**

PRECISE PULSE GENERATORS HELP CHARACTERIZE ICS

Three models in the HFS 9000 series of precision pulse generators use a new type of pulse synthesis architecture to achieve excellent accuracy at repetition rates to 600 MHz. The generators, which offer pulse widths down to 400 ps, can test various logic families. Four channels are standard and six are optional. Edge placement resolution is 10 ps. Users can program the location of rising and falling edges, delay, width, and duty factor, and can individually set each channel's output level.

TEKTRONIX INC., *P.O. Box 19638, Portland, OR 97219-0638 (800) 426-2200; Electronic Design, Nov. 8, p. 156* **Circle 365**

COMPACT ASIC TESTER PACKS PER-PIN FLEXIBILITY

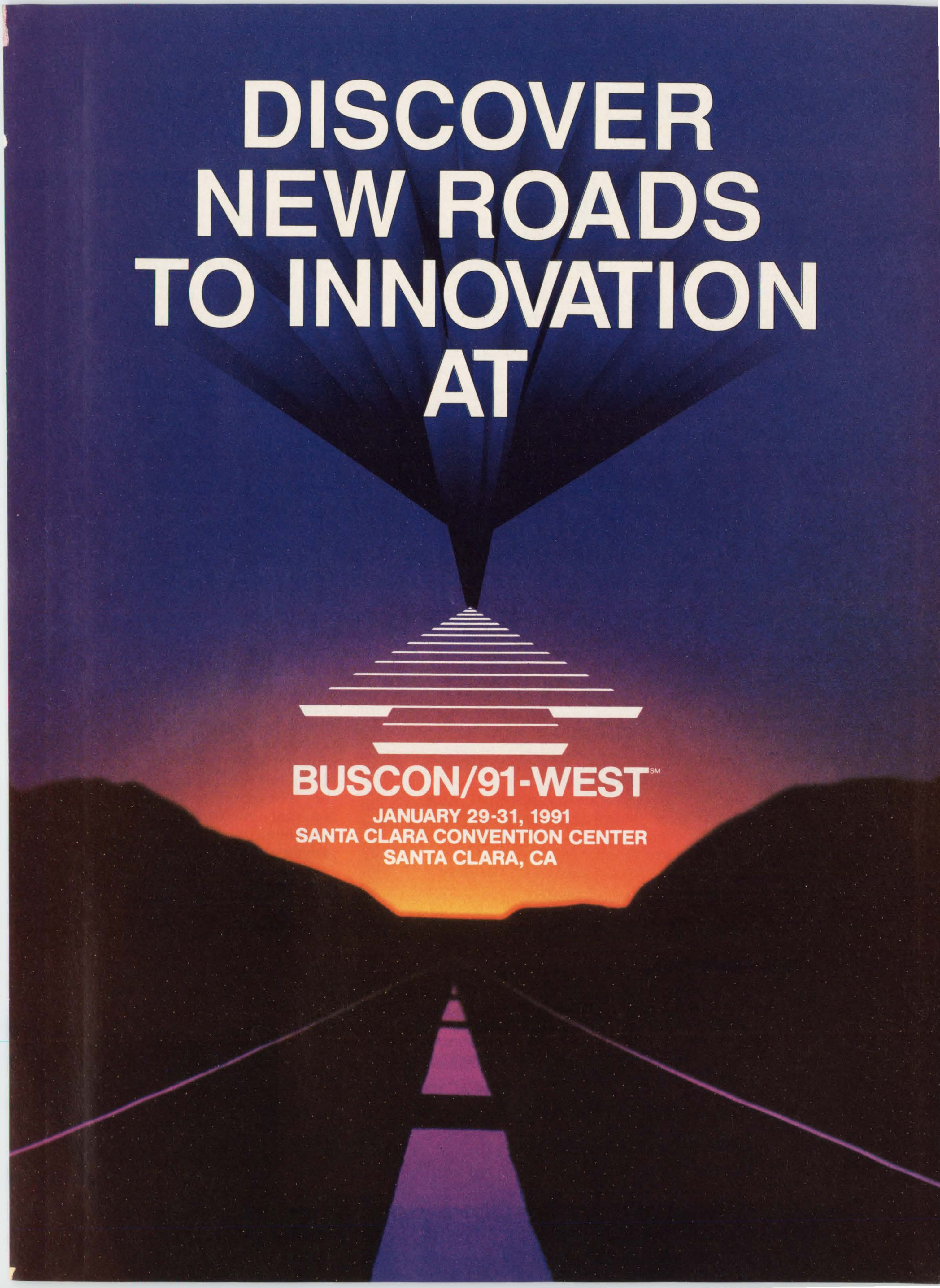
The SC212 offers full-function ASIC and chip-set testing in a compact package. The system does functional tests at up to 50 MHz and operates at 100 MHz in the nonreturn-to-zero mode. Configurations run from 64 to 304 bidirectional pins with pin vector memories from 32 to 128 kwords. The highly integrated circuitry, including a fully custom VLSI device that supplies a dual-channel "tester on a chip," cuts the tester's size to 11 in. high by 24 in. wide by 38.8 in long without monitor and server.

CREDENCE SYSTEMS CORP., *47211 Bayside Pkwy., Fremont, CA 94538 (415) 657-7400; Electronic Design, May 10, p. 212* **Circle 366**

THERMAL IMAGING TOOL LOCATES BOARD HOT SPOTS

The Compix 6000 thermal imaging system uses a simplified version of sophisticated infrared scanning techniques to create thermal pictures or temperature maps. Designers can use the system to spot thermal problems on board or system prototypes. The Compix 6000 generates a complete thermogram of an operating board in under a minute and is non-invasive. The system measures temperatures between 17°C and 150°C and records differences as small as 0.2°C. Spatial resolution is 15 mils.

COMPIX INC., *Box 885, Tualatin, OR 97062-0885 (503) 639-8496; Electronic De-*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An Open Letter to Engineering Management

These are challenging times for the computer and electronics industries. Markets are maturing, and business, industry and the military have all been forced to reduce spending. At the same time, it has become increasingly costly to develop new products, or product enhancements. To survive and remain competitive, you and your staff must be more productive and innovative than ever before.

That's why it makes more sense than ever before to send your design engineers to Buscon West. They'll learn up close and in detail about the major technologies and system architectures (including Futurebus+) – from the experts who developed them. They'll see hundreds of new hardware and software products that will help them solve design problems, reduce production costs and enhance performance.

They'll join in the open exchange of ideas, and be inspired by some of the leading minds of the industry. And they can accomplish more in terms of research at Buscon than in months or weeks of leafing through catalogs and product literature.

Clearly, sending your staff to Buscon West is one of the best investments you can make. When the going gets tough, the tough go to Buscon. It's where innovation shifts into high gear. See you at the show!

Sincerely,

David Caplin
Group Show Director

THE BUSCON BASH

Doubletree Hotel • Wednesday, January 30, 1991 • 6:00 p.m. to 8:00 p.m.

After an intense day in the technical sessions or exploring the Buscon exhibit floor, you've earned a break. Sponsored by *Computer Design* Magazine and leading manufacturers, the BASH is your chance to relax, unwind and network with your peers in an upbeat, informal atmosphere. Enjoy the live music, hot and cold hors d'oeuvres and fine spirits free of charge: your Buscon West badge is your admission ticket.

While you're there, you'll want to witness the prestigious Buscon Industry Achievement Award, presented to an individual who has made an outstanding contribution to the board level industry. Judges for this coveted award include Jon Titus, editor of *EDN*; John Miklosz, editor of *Computer Design;* David Lieberman, editor of *EE Times*; David Wilson, editor of *OEM Integrator*; and Warren Andrews, editor of *Infobus Report*.

You'll gain valuable perspective on the needs and nature of this dynamic industry, and have the chance to discuss today's most compelling issues with people who have developed major technologies, defined trends and set the pace for innovation. So don't miss this rare opportunity to meet and mingle with industry heavyweights.

GET A GRASP ON THE FUTURE IN OVER 150

The Buscon West exhibit floor is literally an education in itself. Because Buscon is the only comprehensive bus board and systems architecture exhibit on the west coast, you'll find the largest array of new products, vendors and technologies west of the Mississippi. You'll get a first glimpse of the latest advances in bus technology, boards, components and systems software, and identify new suppliers. And you'll expand your design options with hundreds of new products and technologies, including:

Analog input/output	Workstations
Backplanes	BiBus
Card racks	BitBus
Central Processor Units	VME
Chips	STD
Communications/ Serial I/O	STE
Extender boards	NuBus
High density memory systems	MultiBus I
Image processors	MultiBus II
Multifunction boards	Q-Bus
Parallel/Serial I/O Expansion	SCSI
Peripheral controllers	PcBus/ Microchannel
Software	CIMBus
VXI	G-64/96
	Exorbus
	RISC
	...and many more.

Expanded exhibit hall hours: Come early, stay late!

This year, we've made it easier than ever to explore the Buscon exhibits, even if you can't take an entire day away from the office. On Tuesday, January 29th, the exhibit hall will remain open until 8:00 p.m. so that even the busiest design and electronics engineers can have the opportunity to see the very latest technical innovations first-hand. Because in the swiftly-changing world of systems and bus architecture, you've got to keep pace with the leaders to survive.

Exhibit Hours

Tuesday, January 29
2:00 p.m. to 8:00 p.m.
Wednesday, January 30
10:00 a.m. to 6:00 p.m.
Thursday, January 31
10:00 a.m. to 4:00 p.m.

BUSCON/91–WEST EXHIBITORS

(Complete as of 9/1/90)

ASSOCIATIONS
STDBUS Manufacturers Group
Multibus Manufacturers Group
VITA,VFEA International Trade Assoc.
VXI Consortium

BITBUS
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Micro Industries
Micro/Sys, Inc.
Siemens AG Auto Group Simicro
Xycom, Inc.

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Pro-Log Corp.
Rockwell CMC
Systran Corp.
SBE, Inc.
Themis Computer

EXORBUS
General Micro Systems, Inc.
Micro Industries

FASTBUS
Elma Electronic, Inc.
Mupac Corp.

FUTUREBUS
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Mupac Corp.
National Semiconductor Corp.
Nissho Electronics
Software Components Group
Texas Instruments

G-64/96
Bicc-Vero Electronics, Inc.
Eyring, Inc.

GRAPHICS
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Integrated Soultions
Ironics, Inc.
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Nova Graphics International Corp.
Parallax Graphics
Themis Computer
Uniflex
VIGRA, Inc.

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Ciprico, Inc.
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Diversified Technology, Inc.
Elma Electronic, Inc.
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Micro Industries
Micro Memory, Inc.
Micro/Sys, Inc.
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Omnibyte Corp.
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Performance Technologies, Inc.
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Prototek, Inc.
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Ziatech Corp.
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NUBUS
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I-Bus
Ironics, Inc.
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Matrix Corp.
Micro Industries
Mupac Corp.

MANUFACTURERS' EXHIBITS.

Optima Enclosures
Prototek, Inc.
Rittal Corp.
Schroff, Inc.
Zendex Corp.
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PC BUS

Alacron
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Elma Electronic, Inc.
Entron Computer
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Micro Memory, Inc.
Minc, Inc.
Nissho Electronics
Parallax Graphics
Phoenix Contact
Prototek, Inc.
Rockwell CMC
Siemens Ag Auto Group Simicro
Software Components Group
Texas Microsystems, Inc.
Trend Circuits, Inc.
Xycom, Inc.
Yarc Systems
Zendex Corp.
Zoltech Corp.

PUBLICATIONS

CMP Publications
Cahners Publishing Co.
Computer Design, Computer Design News Edition
Computer Technology Review
Control Engineering
Chilton Co. (*IAN, I&CS*)
Electronic Component News
Embedded Systems Programming
Penton Publishing (*Electronic Design, Electronics* Magazine)
SUPERMICRO Journal
Unixworld
VMEbus Systems Magazine

Q-BUS/BIBUS

Augat, Inc.
Bancomm, Div. of Datum, Inc.
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Chrislin Industries, Inc.
Clearpoint Research Corp.
Hybricon Corp.
Inmos Corp.
Integrated Solutions
Performance Technologies, Inc.
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Zoltech Corp.

S BUS

Sigma Information Systems
Sun Microsystems
Themis Computer

SCSI

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Digital Equipment Corp.
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GreenSpring Computers, Inc.
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Interphase Corp.
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Mizar, Inc.
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Datricon Div. of Scientific Technologies, Inc.
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Performance Technologies, Inc.
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Concurrent Computer Corp.
Dawn VME Products
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Eyring, Inc.
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VTC, Inc.
Wind River Systems
Xycom, Inc.
Xylogics, Inc.
Yarc Systems
Zoltech Corp.

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VMETRO, Inc.

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Pro-Log Corp.
Quantum Software Systems
Radstone Technology
Ready Systems
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Ziatech Corp.

OS-9

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Themis Computer

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Mizar, Inc.
Nissho Electronics
Nova Graphics International Corp.
Radstone Technology
Rockwell CMC
Siemens AG Auto Group Simicro
Software Components Group
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Systran Corp.
Texas Microsystems, Inc.
Themis Computer
Uniflex
Wind River Systems
Xylogics, Inc.
Zoltech Corp.

MS-DOS

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Nissho Electronics
Pro-Log Corp.
RadiSys Corp.
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WinSystems, Inc.
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Zoltech Corp.

PDOS

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DEBUG TOOLS AND ADAPTORS

Emulation Technology, Inc.
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THE INDUSTRY'S MOST PRESTIGIOUS TECHNICAL CONFERENCE.

The Buscon West Technical Program is definetly in a class by itself. No other industry conference features such an outstanding array of distinguished industry experts, or draws such consistently high praise from attendees. Under the expert guidance of Warren Andrews, editor of *InfoBus Report*, the conference has earned a reputation as a major information clearing house, with speakers who not only know the technologies, but actually participated significantly in their development.

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THE GREAT REAL-TIME OPERATING SYSTEM DEBATE

Tuesday, January 29, 5:00 p.m. - 7:00 p.m.

Since the advent of the 386 AT class computer, OEMs have turned towards the Intel 386 architecture to solve applications that once required minicomputer power. Real-time operating system vendors have not been slow to recognize that the low-cost 386 platform provides an opportunity for real-time applications that they cannot afford to miss out on. Many such vendors are now looking to provide real-time operating systems in multiprocessing environments. In such applications, a single operating system could harness the power of multiple 386 or 486 processors in a single system to provide an inexpensive, yet highly powerful solution to real-time problems. In the next Great Debate, a host of operating system vendors will get a chance to discuss future trends in the 386 real-time arena.

Possible contenders at this time include:

1) Wind River Systems
2) Ready Systems
3) Lynx Real-Time Systems
4) Software Components Group
5) Venturecom

And from the press:

Warren Andrews, *CD/Infobus Report*
Dave Lieberman, *EE Times*
Dave Wilson, *The OEM Integrator*
John Gallant, *EDN*
John Black, *VME Systems*
Steven Scrupski, *Electronic Design*

A blue ribbon panel helps set the agenda

A distinguished panel of industry experts and innovators helps to set the agenda for Buscon West. They provide valuable insights on the major issues and concerns facing the bus and board level industry, and forecast the direction that new innovation is likely to take. Their guidance and expertise ensures that the Buscon West seminars address the needs and interests of the entire industry.

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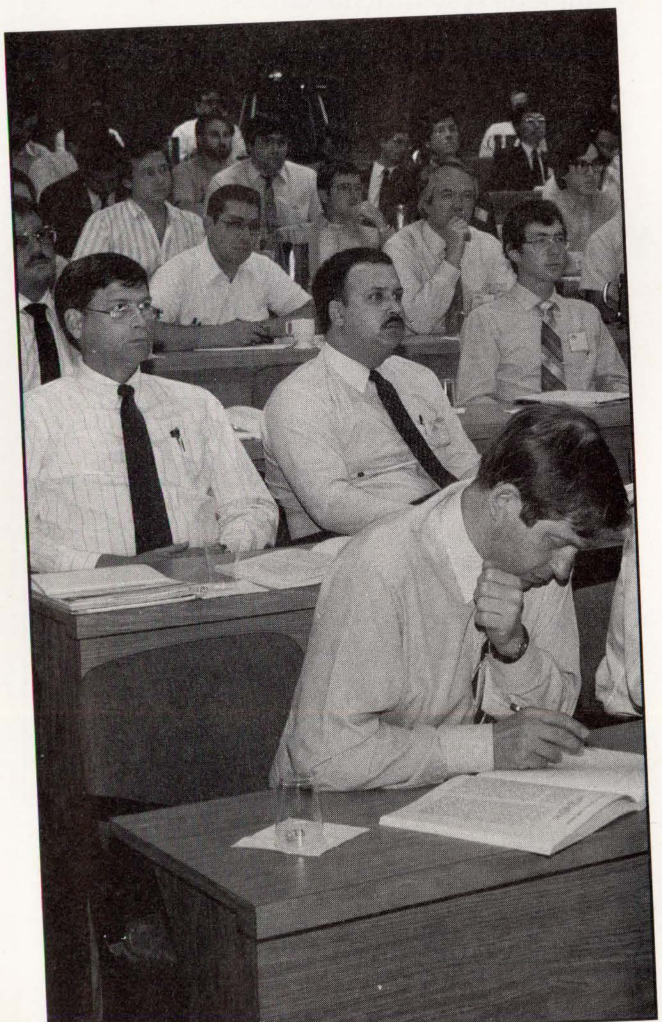
BUSCON TECHNICAL SEMINARS

Monday, January 28, 1991

Futurebus+ rates a day all its own!

Futurebus+, which promises to become the next major bus architecture, merits special emphasis at this year's Buscon West. We've scheduled a special pre-show Futurebus+ seminar to allow as many as possible to participate in this exciting advanced technical seminar. Coordinated by VITA, this day-long session offers a full examination of this new technology and its incorporation into current applications. Attendees will come away with a complete overview, specifications, and insights into how VME and Multibus II will bridge to Futurebus+. Seating for this one-of-a-kind program is limited, so sign up today!



Futurebus+
8:30 a.m. - 5:00 p.m.

Futurebus+ Seminar

Futurebus+ is the most likely candidate for the standard bus architecture of the future. Learn about it now, and get a head start on tomorrow's applications!

This unique seminar, sponsored by VITA and *Computer Design* Magazine, is the most comprehensive seminar on this advanced bus available to the general public. This is a rare opportunity to learn about the specification, protocols, mechanisms and features of the bus from the leaders who developed and finalized the specification. Because there is such a wide interest in Futurebus+, we've devoted an entire day – Monday, January 28 – so that all who wish to attend can do so without scheduling conflicts. Demand will be high and seating is limited, so sign up today!

Morning:
- Comprehensive overview: bus specifications & profiles
- Mechanical considerations
- Electrical characteristics of the BTL backplane
- CSR architecture
- Mechanisms for live insertion/hot-swap

Afternoon:
- Futurebus+ parallel protocol
- Arbitration protocol
- Cache Architecture
- Message-passing protocols
- Question-and-answer period

Futurebus+ Speakers (at press time):
Ray Alderman, VITA; Harrison Beasley, Texas Instruments; Jay Cantrell, Texas Instruments; Paul Dixon, Mizar, Inc.; Wayne Fischer, Force Computers; Joe George, Nanotek; Mike Humphry, BICC-VERO; John Hyde, Intel Corp.; Christopher Koehle, National Semiconductor: Bill Mahusen, Performance Technologies; Thanos Mentzelopoulos, Ironics Inc.; Mike Thompson, Mupac

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Tuesday, January 29, 1991

VMEbus
8:30 a.m. - 5:00 p.m.

VMEbus Seminar

VMEbus has changed and is changing – fast! Learn how to take advantage of the most recent developments.

This day-long seminar, sponsored by *VMEbus Systems*, will explore the direction vendors and system architects are taking to enhance the performance of VMEbus-based systems.

Morning:

- Review of VMEbus architecture and theory
- Enhancing performance with hardware extensions
- The emerging VME 64 standard
- High-performance mezzanine buses
- Multicrate configurations
- Multiprocessing configuration (single and multiple operating systems)
- Development environments

Afternoon:

- Using interface chips to enhance system performance
- Performance benefits of advanced CISC and RISC processors as performance enhancers
- Comparative advantages of VME vs. other buses

VMEbus Speakers (at press time):
Dave Baasch, RadiSys Corp.; John Black, *VMEbus Systems*; Robert Fine, VTC Incorporated; Wayne Fischer, Force Computers; Gerry Gipper, Motorola Computer Group; Bob Griener, Motorola Computer Group; Clarence Peckham, Heurikon Corp.; Fred Rehhausser, Force Computers; Ed Schulman, Ironics, Inc.; Joel Silverman, Radstone Technology

Multibus II
8:30 a.m. - 5:00 p.m.

Multibus II Seminar

Multibus II offers many advanced features that you can use *today*. Learn why this bus architecture is rapidly gaining in popularity.

Recent surveys indicate increasing use of Multibus II in a variety of applications. This seminar takes a fresh look at Multibus II, its capabilities, applications and performance enhancements. Sponsored by *Electronic Design*.

Morning:

- Overview and discussion of MBII theory
- How MBII can benefit advanced applications
- Multibus system achitectures, implementations and applications examples
- Advanced performance alternatives
- Multiprocessing in MBII using a distributed client/server architecture with a message-passing OS

Afternoon:

- The latest bus interface options
- Cost-effective implementations for non-intelligent I/O
- Intelligent I/O alternatives
- Bus extension options
- MBII as a microprocessor development environment
- Other development tools
- Panel discussion
- Question and answer period

Multibus II Speakers (at press time):
Mike Curran, Micro Industries; Daniel Frank, Quantum Software Systems, Ltd.; John Hyde, Intel Corp.; John Mahoney, Heurikon Corp.; Manfred Peitnegger, Siemens; Len Schulwitz, MMG

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Wednesday, January 30, 1991

PC Bus Platforms
8:30 a.m. - 5:00 p.m.

PC Bus Platforms Seminar

Discover how you can bring the powerful benefits of PC Bus architecture to the industrial arena!

This seminar is geared for design engineers and systems integrators either using, or looking to use, personal-computer platforms in industrial applications. Sponsored by *EE Times*.

Morning:

- Discussion of ISA, EISA and MCA architectures
- Advances in the operating system
- Advantages of the latest in Embedded DOS, Real-Time DOS, and other industrial alternatives to the conventional disk-based MS/PC DOS approach
- Ready-made applications environments
- Technical dissertation: development environments

Afternoon:

- Mechanical implementations of PC bus platforms
- Industrial-hardened PC's
- PC buses riding on other bus architectures (form factors) in the industrial arena
- The latest 32-bit implementations of the PC architecture on other platforms, including STD 32
- The latest chip sets for increasing performance, including EISA chip sets and those for bus mastering and data streaming mode on MCA
- Relative merits of each of the personal computer architectures
- Question and answer period

PC Bus Platforms Speakers (at press time): Steve Cooper, RadiSys Corp.; Rene Coressel, Lab-Tech; Brandon Crowe, Applied Physics; Michael Curran, Micro Industries; Rob Davidson, Ziatech Corp.; Doug Finn, National Instruments; Daniel Frank, Quantum Software Systems, Ltd.; David Lieberman, *EE Times*; Jim Ready, Ready Systems; Roy Sherrill, Datalight; Randy Wilhelm, Intel Corp.; Rex Zerger, Texas Microsystems

Embedded Systems Programming
8:30 a.m. - 5:00 p.m.

Embedded Controller /Systems Programming Seminar

Today's real-time operating systems have become more important, and much more complex. Learn how you can save time and effort, and avoid pitfalls in embedded systems design.

Engineers, systems designers and architects looking for real-time embedded programming solutions will gain valuable insights from the rich assortment of speakers in this session. *Embedded Systems Programming* is the sponsoring publication for this seminar.

Morning:

- General introduction to embedded systems programming
- Definitions of real-time software, kernels and operating systems
- Discussion: how to partition a problem
- Fitting a kernel to specific hardware and application
- Solving multiple CPU problems

Afternoon:

- Optimizing compilers and system performance
- Development tools, including debuggers
- Operating in a multiprocessor environment
- Panel Discussion
- Question and answer period

Embedded Controller/Systems Programming Speakers (at press time): James Bairey, Ready Systems; Greg Buzzard, Ready Systems; John Hyde, Intel Corp.; Clarence Peckham, Heurikon Corp.; Ed Rathje, JMI Software; Kim Rowe, Multiprocessor Toolsmiths; Linda Thompson, Software Components; Tom Williams, *Computer Design*; Dalibor Vrsalovic, Ready Systems Corp.

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Thursday, January 31, 1991

Emerging Architectures 8:30 a.m. - 2:00 p.m.

Emerging Bus Architectures Seminar

Designing for the workstation environment? Then you can't afford to miss this seminar. Catch up with the very latest innovations from DEC, SUN, IBM and others!

The overwhelming trend toward incorporating open standards has resulted in the emergence of at least two major bus architectures – SBus and TURBOChannel – and the improvement of MCA in IBM's 6000 workstation and new protocols promising to push NuBus to greater heights. And, EISA backers also promise to bus enhancements to participate in the workstation business. Its been estimated that this market segment will grow at over 250% over the next four years. Join industry leaders who will discuss the technical details and other merits of these buses. Seminar sponsor publication is *Control Engineering*.

Seminar highlights:

- Introduction technical description: SBus and TURBOchannel
- Protocols, operant mechanisms, arbitration and special features
- Design and development issues, including company-supplied tools and special aids
- Bridges to other buses, such as VMEbus and Futurebus+
- Unique opportunities for using I/O workstation channels
- Panel Discussion

Emerging Bus Architecture Speakers (at press time): Dr. Paul Borrill, Sun Microsystems; Tony Levy, Digital Equipment Corp.; Jim Lyle, Sun Microsystems; Dr. Michael K. J. Nielsen, Digital Equipment Corporation

Military Applications 8:30 a.m. - 2:00 p.m.

Military Applications Seminar

The armed forces are looking for standardized buses that can replace their costly proprietary systems. Get the information you need to develop cost-effective alternatives.

The complexion of military systems in the U.S. is changing dramatically as increasingly more standard-architecture components become the foundation of many systems in all branches of the service. Attendees at this seminar will have the opportunity to learn first-hand how some of these changes are occurring and what some future military requirements will look like. Sponsored by *Defense Electronics*.

Seminar highlights:

- Future military computer/electronic requirements
- Military push to NDI (non development items)
- Ruggedized vs. Mil-STD
- Providing transparent commercial development environments for military programs
- Enhanced performance in military computers
- Mil Futurebus+

Military Applications Speakers (at press time): John Haystead, *Defense Electronics*; Ralph Lachanmaier, U.S. Navy; Herb Marks, Intel Corp.; Doug Patterson, Radstone Technology; Michael Schmidt, Lockheed Sanders Inc.; Duncan Young, Radstone Technology

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Now that you've made the decision to attend Buscon/91–West, be sure to mark the show dates on your calendar. Make this important industry event a priority in your schedule. Pre-register to save time and avoid long lines: you'll save money, too.

It's important to take a little time now to plan your visit. Target the specific vendors and products that you want to see. Register early to ensure a seat in the technical sessions you want to attend. And don't forget about the special events including the Buscon Bash.

Advance Registration – Seminars

Take advantage of our 24% early bird discount. Complete and return the registration form on page 12 today. Mail it with your check or fax it to us with your credit card information. The fax number is **203-857-4075**. You can even register by phone by calling toll-free **1-800-243-3238.** Be sure to have your credit card handy when you call. But whichever way you choose to register, remember that January 4 is the cut-off date for the early bird discount. If you have any questions, please call us at **203-852-0500**. We'll be happy to speak with you.

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Even if you don't plan to attend the Buscon Technical Seminars, it still makes sense to register early. Complete the registration form on page 12 and mail or fax it to us today. Your badge will be waiting for you in the registration area at the show, so you can avoid long registration lines and get the most out of your visit to Buscon.

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* Substitutions may be made until January 15, 1991. After this date all changes must be made at the conference.

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The following special rates have been negotiated for Buscon/91–West attendees.

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Note: Make all cancellations in writing on the confirmation form and return it directly to the hotel. Changes can be made by calling the hotel directly. Refer to the hotel confirmation for check-in and -out times and guarantee policies.

	Single	Double
Doubletree Hotel at Santa Clara (Headquarter Hotel) 5101 Great America Parkway Santa Clara, CA 95054 408-986-0700 (Connected to Convention Center)	$106	$116
Santa Clara Marriott 2700 Mission College Boulevard Santa Clara, CA 95054 408-988-1500 (Short cab ride to Convention Center)	$107	$107
Days Inn Hotel 4200 Great America Parkway Santa Clara, CA 95054 408-980-1525 (Short walk to Convention Center)	$77	$77

Airline

American Airlines has been selected as the official Buscon/91–West air carrier. You can save 50% off regular coach fares or 5% off any already discounted fare. To take advantage of the special rates, contact Travel Planners at 800-221-3531 (9 a.m. – 5 p.m. EST) in NY call 212-473-4688. Identify yourself as a Buscon/91–West attendee. When making your reservations with Travel Planners, you automatically receive drink/movie coupons and flight insurance.

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1. ☐ President, Owner, Vice President
2. ☐ Project Manager, Sr. Engineer
3. ☐ System Engineering Manager
4. ☐ Other Engineering & Engineering Support
5. ☐ Purchasing
6. ☐ Educator
7. ☐ Consultant
8. ☐ Sales/Marketing
9. ☐ Other ______

Main Company Activity (Check all that apply)
2. ☐ Board Manufacturer
3. ☐ Systems Manufacturer
4. ☐ Systems Integrator
5. ☐ Subsystem Manufacturer
6. ☐ Board/System Market
7. ☐ Surface Mount Devices
8. ☐ Industrial Automation
9. ☐ Scientific/Computation
10. ☐ Commercial
11. ☐ Medical
12. ☐ Communications
13. ☐ Government/Military
14. ☐ Consultant
15. ☐ Other (please specify) ______

III. Type(s) of Bus Interest: (Check all that apply)
16. ☐ PC
17. ☐ Multibus I
18. ☐ Multibus II
19. ☐ VME Bus
20. ☐ NuBus
21. ☐ Q-Bus
22. ☐ FutureBus
23. ☐ STD
24. ☐ S-100
25. ☐ STE
26. ☐ G-54
27. ☐ FastBus
28. ☐ VersaBus
29. ☐ SMP
30. ☐ Exorbus
31. ☐ BitBus
32. ☐ UniBus
33. ☐ SCSI
34. ☐ Other ______

35. Number of Employees in Company: (Check one)
1. ☐ 1-50
2. ☐ 51-100
3. ☐ 101-250
4. ☐ 251-500
5. ☐ 501-1,000
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4. ☐ 1.1 million-5 million
5. ☐ 5.1 million-10 million
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	— OR — EMBEDDED CONTROLLER/SYSTEMS PROGRAMMING		$ 215	$ 245
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TEST AND MEASUREMENT

sign, July 12, p. 136
Circle 367

CUSTOM IC BOOSTS GPIB BOARD TO NEW STANDARD

A custom chip that takes advantage of the expanded IEEE-488.2 standard gives advanced features to a 16-bit IEEE-488 interface for IBM PC/AT computers. The chip's contribution to the AT-GPIB board includes an enlarged command set that reduces software driver overhead and code size, while boosting data-transfer rates to 1 Mbyte/s on writes as well as reads. The board works with driver and application programs written for most popular older-generation GPIB controller ICs.
NATIONAL INSTRUMENTS CORP., *6504 Bridge Point Pkwy., Austin, TX 78730-5039 (512) 794-0100; Electronic Design, June 14, p. 99* **Circle 368**

VERSATILITY AND ECONOMY HIGHLIGHT IC PROGRAMMER

The Model 2900 programmer retains the universal pin drivers of the top-of-the-line Unisite model, but costs less than a third as much. The 2900 accepts 28-pin devices, with optional support for 44-pin ICs. Data I/O estimates that the programmer handles 75% of all available programmable devices in various packages, both DIP and surface-mounted. A new socketing technology accommodates PLCC surface-mounted packages without the need for different adapters, which can cost from $50 to $200.
DATA I/O CORP., *10525 Willows Rd. NE, P.O. Box 97046, Redmond, WA 98073-9746 (206) 881-6444; Electronic Design, Apr. 26, p. 119.* **Circle 369**

FEATURES HIGHLIGHT LOWER-COST DIGITAL SCOPE

The Model 9410 digital oscilloscope has several features not usually found in its price range. For the $6900 price tag, the instrument has a 5-by-7-in. high-resolution (4096-by-4096-point) vector-scan display and a trigger system that offers pulse-width, interval-width, logic-pattern, state, time/event, and TV triggering. The 10-kword acquisition memory helps the 100-Msample/s scope maintain a high, usable bandwidth and good timing resolution, even for fast signals.
LECROY CORP., *700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499 (914) 578-6097; Electronic Design, Aug. 23, p. 108* **Circle 370**

FULL PER-PIN FLEXIBILITY ENHANCES 100-MHZ TESTER

An innovative cooling system and surface-mounting technology help create a functional production tester with a full tester-per-pin architecture in less than half the space of first-generation tester-per-pin systems. The Polaris 100's 100-MHz base data rate and other features enable users to test the most complex devices. Each pin has its own timing generator, and edges can be placed anywhere in a four-cycle span. In addition, an 8-million vector memory ensures high fault coverage for even the densest VLSI chips.
MEGATEST CORP., *880 Fox Ln., San Jose., CA 95131 (408) 437-9700; Electronic Design, Mar. 8, p. 108.* **Circle 371**

SPECTRUM ANALYZER BOOSTS SPEED AND RESOLUTION

Taking advantage of the latest developments in digital-filter and fast-Fourier-transform technology, the HP 3588A breaks the resolution-vs.-speed bottleneck in swept spectrum analysis. The analyzer delivers resolution bandwidths from 20 kHz down to only 0.0045 Hz while boosting sweep speed by a factor of 100 or more, depending on the application. Frequency spans of 10 Hz to 150 MHz are available, and broadband accuracy is better than 0.5 dB for both signal and noise measurements.
HEWLETT-PACKARD CO., *Lake Stevens Instrument Div., 8600 Soper Hill Rd., Everett, WA 98205-1298 (800) 752-0900; Electronic Design, Jan. 11, p. 201* **Circle 372**

BENCHTOP ASIC VERIFIER SPORTS BIG-TESTER FEATURES

Packing many capabilities of high-end production testers, the benchtop ETS 7000 Engineering Test Station verifies ASIC designs at a cost of less than $1000 per pin. Maximum vector rate is 100-MHz, pin-to-pin skew is ±500-ps, and timing resolution is 100 ps. With a vector depth ranging from 493,000 for a 32-pin system to 155,000 for 128 pins, designers should be able to perform most tests in one pass without time-consuming disk accesses.
HILEVEL TECHNOLOGY INC., *31 Technology Dr., Irvine, CA 92718 (714) 727-2100; Electronic Design, Mar. 22, p. 132* **Circle 373**

ANALYZER CAPTURES STATE AND TIMING IN ONE PASS

The goal of the Fluke/Philips PM 3580 logic analyzer is to be so easy to use that even inexperienced operators can be up and running in under 30 min. To accomplish this, the instrument uses not only pop-up menus and VGA graphics, but also a dual-analyzer-per-pin architecture. With only one set of probes, each of the 3580's 96 channels can collect both state and timing information simultaneously. The unit does 50-MHz state analysis and 200-MHz timing analysis and has 2 kbits of memory per channel.
JOHN FLUKE MFG. CO., *P.O. Box 9090, Everett, WA 98206-9090 (206) 347-6100; Electronic Design, Oct. 25, p. 66* **Circle 374**

DEEP MEMORY HIGHLIGHTS 100-MHZ LOGIC ANALYZER

The Centurion, a logic analyzer card for the DAS9200 digital-analysis system, earns its name by delivering 100-MHz sampling, clocking, triggering, and time stamping on 100 channels (96 data and 4 clock). Two versions are available with either 8- or 32-kbit memories. To ensure signal fidelity, the Centurion's probes use the same passive compensation technique found on Tektronix's high-end oscilloscopes. One DAS mainframe can hold three cards, and expansion units can create a maximum-size system of 16 cards.
TEKTRONIX INC., *Logic Analyzer Div., P.O. Box 12132, Portland, OR (800) 245-2036; Electronic Design, Oct. 25, p. 65* **Circle 375**

100-MHZ LOGIC-ANALYZER CARD IMPROVES INTERFACE

Plugged into the HP16500A logic-analyzer mainframe, the HP 16540A master card supplies 16 channels of 100-MHz state and timing analysis with full-speed triggering across all channels. Up to four 48-channel HP 16541A expansion modules can be added to make a 208-channel system. The analyzer cards include 4-kbit/channel memories and full-speed time or event tagging. In addition, an improved interface lets users control the analyzer through the built-in color touchscreen or an optional mouse, trackball, or ASCII keyboard.
HEWLETT-PACKARD CO., *Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80907-2197 (800) 752-0900; Electronic Design, Oct. 25, p. 68* **Circle 376**

ICS REDUCE SIZE, COST OF 1-GHZ DIGITAL SCOPE

Six custom ICs in the HP 54510A replace boards full of components, yielding a portable 16.75-by-14.3-by-7.65-in. package. The custom ICs also slash component count, so reliability should be very high. HP estimates mean-time-between-failures at 30,000 hours. The HP 54510A has a horizontal (timing) accuracy of 100 ps and a vertical (voltage) accuracy of 1.25% of full scale. Record length is 8 ksamples. The scope measures 17 pulse parameters automatically.
HEWLETT-PACKARD CO., *Colorado Springs Div., P.O. Box 2197, Colorado Springs,*

← CIRCLE 87

TEST AND MEASUREMENT

CO 80901-2197 (800) 752-0900; Electronic Design, Oct. 11, p. 131 **Circle 377**

COMBINED LOGIC ANALYZER-SCOPE SPEEDS DEBUGGING

As useful as logic analyzers are for debugging digital circuits, they're often only part of the solution. For that reason, the Model 1600 Logic/Oscilloscope combines the features of logic analyzers and digital oscilloscopes. The instrument's 16 channels can be switched between a 200-MHz logic analyzer mode and a 350-MHz, 100-Msample/s digital mode. Designers don't have to double-probe or reprobe the circuit. With up to nine 16-channel expansion modules, 160 analyzer/scope channels are possible.

OUTLOOK TECHNOLOGY INC., *200 Hacienda Ave., Campbell, CA 95008 (408) 374-2990; Electronic Design, Apr. 26, p. 57* **Circle 378**

COMPUTERS

68040 AND 68020 APPEAR ON SAME BOARD

By putting a 68040 and a 68020 processor on the same board, the 68-41 Single-Board Computer does the job of two boards. The 68020 is used for I/O functions, such as controlling the high-performance SCSI, Ethernet, and on-board serial I/O subsystems. This frees up the 68040 chip to process data without being interrupted. The VMEbus board's 68040 processor operates at 40 MHz, using 8 kbytes of cache memory. The dedicated I/O processor can handle up to 4 Mbytes of dynamic RAM. Included are four serial ports, an advanced-processor extension (APEX) bus interface where custom modules can be added, and 2 kbytes of battery-backed static RAM.

RADSTONE TECHNOLOGY, *20 Craig Rd., Montvale, NJ 07645 (201) 391-2700; Electronic Design, Nov. 22, p. 149* **Circle 379**

REAL-TIME OS UPGRADE EXTENDS KERNEL

Upgrading to an earlier version of the real-time operating system, VxWorks 5.0 increases the software's kernel performance, I/O functions, connectivity support, debugging, and graphics. The kernel improvements include higher speed—benchmarks on 25-MHz 68020-based target boards have clocked wind-context switches at 16 µs and interrupt latency at 8 µs. The software includes serial-line interface protocol and high-security login and remote login capabilities. Target configurations can range from a 60-kbyte, standalone, real-time kernel to a 465-kbyte full-scale development system.

WIND RIVER SYSTEMS INC., *1351 Ocean Ave., Emeryville, CA 94608 (415) 428-2623; Electronic Design, Sept. 13, p. 113* **Circle 380**

TINY MODULES FORM COMPLETE EMBEDDED PCS

A trio of reduced-size computers delivers desktop computing power in palm-sized 3.6-by-3.8-in. modules that are only 0.6 in. thick. The CoreModule/XT, /286, and /386SX include an expansion pin-and-socket connector arrangement that allows additional boards to be stacked on top of each other. Those additional boards may include I/O lines, communication ports, and IEEE-488 interfaces. A small header connects to a coprocessor daughterboard. The XT version contains a 10-MHz NEC V20 processor, similar to an Intel 8088. The 286 and 386SX models run at 16 MHz. They can hold from 256 kbytes to 2 Mbytes of RAM.

AMPRO COMPUTERS INC., *990 Almanor Ave., Sunnyvale, CA 94086 (408) 522-2100; Electronic Design, Oct. 11, p. 49* **Circle 381**

386-BASED LAPTOP USES CACHE MEMORY

The latest challenge toward desktop PCs comes from the 386SX-based SLT 386s/20 laptop computer. System performance is enhanced by adding a 4-kbyte, 4-way set associative cache memory; high-speed fixed disk drives; a high-performance 16-bit graphics controller; and support for an 80387 math coprocessor. The system comes standard with 2 Mbytes of enhanced page memory that's expandable to 14 Mbytes as well as a 3-1/2-in. 1.44-Mbyte floppy disk drive. The laptop also adds other features including multitasking and windowing environments. The system's 32-bit processing capabilities add compatibility with software designed for the 386.

COMPAQ COMPUTER CORP., *P.O. Box 692000, Houston, TX 77269 (800) 231-0900; Electronic Design, Aug. 23, p. 106* **Circle 382**

80386SX PROCESSOR TURNS UP IN NOTEBOOK PC

The TravelMate 3000 notebook PC is part of the latest wave that surfaced with 80386SX microprocessors. It features a 20-MHz processor; a 10-in. diagonal black-on-white VGA display; a 1.44-Mbyte, 3.5-in. floppy drive; and a 20- or 40-Mbyte hard drive. All of this fits in a box that measures just 8.5-by-11-by-1.8 in., and weighs 5.7 lbs. with the battery. The removable battery holds a charge for about three hours. The 32-gray-scale VGA display employs triple supertwist LCD technology. The PC comes standard with 2 Mbytes of RAM that's expandable to 6 Mbytes in 2-Mbyte increments.

TEXAS INSTRUMENTS INC., *Information Technology Group. P.O. Box 202230, ITG-065, Austin, TX 78720 (800) 527-3500; Electronic Design Nov. 8, p. 43* **Circle 383**

WINDOWS 3.0 TOOL DEBUTS

In 1990, the latest version of Microsoft's windowing tool, Windows 3.0, was unveiled. This icon-based release includes improvements to the memory-management system. It maximizes the protected mode of 80286 and 80386 microprocessors to supply added memory for both the environment and the applications running within Windows 3.0. Color and design enhancements add to the polished user interface. Many developers have already ported their software to Windows 3.0. A visual shell was added for completing directory, application, and file-management tasks.

MICROSOFT CORP., *One Microsoft Way, Redmond, WA 98052 (800) 323-3577; Electronic Design, Aug. 9, p. 118* **Circle 384**

SUPERCOMPUTER ACTION AT MINICOMPUTER PRICE

The MP-1 Series of parallel-processing computers can supply supercomputer performance for the cost of a minicomputer. The systems deliver up to 30,000 MIPS and 1250 MFLOPS by applying up to 16,384 processors in one instruction-multiple data architecture (SIMD). Users can increase the amount of processors in their systems as the demand for computational power heightens. The operating system used by the computers is based on Ultrix, DEC's version of AT&T's Unix. The series consists of eight models. All the systems come with a high-resolution, 19-in. monitor.

MASPAR COMPUTER CORP., *749 N. Mary Ave., Sunnyvale, CA 94086 (408) 736-3300; Electronic Design, Jan. 25, p. 131* **Circle 385**

HIGH-END IMAGE-PROCESSING TOOLS DELIVER 300 MOPS

Supercomputer capabilities can be introduced into image computing with the VITec-50 computer. With the addition of a C compiler and expandable memory modules, users can perform virtual-image and floating-point processing at speeds up to 18 MFLOPS. All this technology is squeezed onto one 9U-form factor board. The VITec-50's open architecture supports C, Unix, and X-Windows, and has VMEbus and Ethernet capabilities. The parallel architecture performs address and data functions separately and simultaneously.

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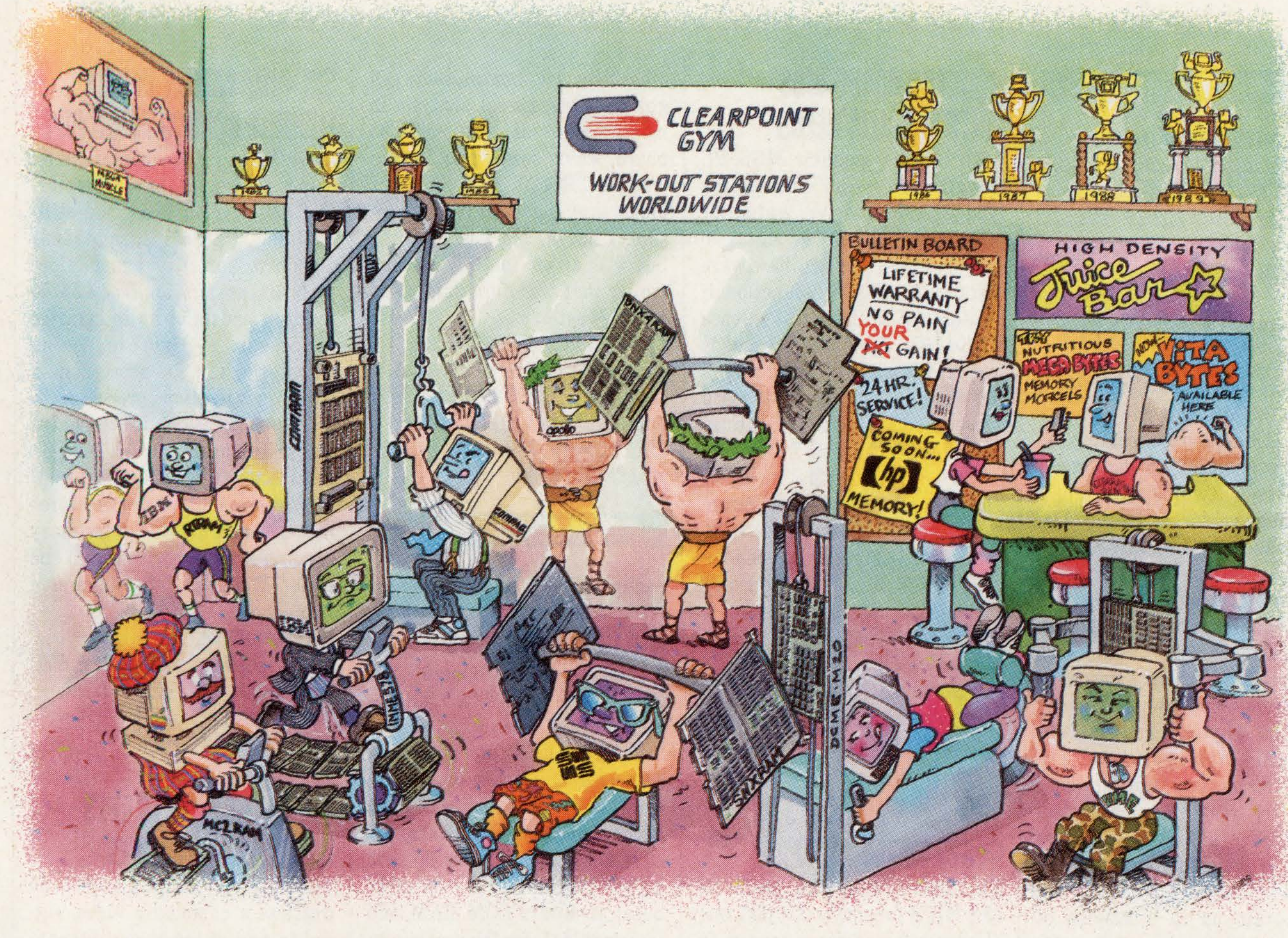

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CIRCLE 126

COMPUTERS

VISUAL INFORMATION TECHNOLOGIES INC., *3460 Lotus, Plano, TX 75075 (800) 325-6467 or (214) 596-5600; Electronic Design, Feb. 8, p. 119*
Circle 386

68040-BASED VMEBUS CPU BOARD PUMPS OUT 13.5 MIPS

Designed around Motorola's 68040 32-bit microprocessor, the HK68/V4F boasts a maximum clock frequency of 25 MHz and a sustained performance of 13.5 MIPS and 3.6 MFLOPS. The board is based on Heurikon's Corebus local-bus architecture, which enables users to customize their systems. This architecture employs a 50-MHz synchronous design featuring transfer speeds up to 200 Mbytes/s and supporting multimaster arbitration. The board maintains upward compatibility with the 68020 and 68881/68882 processors. Two or eight Mbytes of static RAM comes standard. The board can incorporate up to 2 Mbytes of EPROM, with support for 64-kbyte-by-8, 128-kbyte-by-8, and 512-kbyte-by-8 devices.

HEURIKON CORP., *3201 Latham Dr., Madison, WI 53713 (608) 251-8715; Electronic Design, Jan. 25, p. 95*
Circle 387

SCANNER EMPLOYS OPTICAL POSITIONING

Using a dual optical positioning system, the PageBrush full-page scanner can also double as a mouse or a digitizer. The scanner's positioning system reads the lines of a grid that's placed on top of the scanned document and computes its position. The scanner, which looks like a typical mouse, enables users to "paint in" full-page hard-copy text and images to a host computer. The scanned image's size is limited only by the host computer's memory.

MOUSE SYSTEMS CORP., *47505 Seabridge Dr., Fremont, CA 94538 (415) 656-1117; Electronic Design, Aug. 9, p. 115* **Circle 388**

MODULAR 80486 BIOS SUITS SPECIFIC NEEDS

With the i486 modular BIOS, PC manufacturers can choose the type of cache, drive, video, or prewritten software modules to support specific 80486 hardware features. The BIOS is functionally identical to the latest release of the IBM PC/AT BIOS and is compatible with OS/2 and Novell NetWare. It can support on-board cache memory and a floating-point coprocessor. Extensive power-on self-test is included. The optional modules and extensions include EGA, VGA, SCSI, Intel 8242, Chips and Technologies 82C605/6, and ROMed disk caching.

AWARD SOFTWARE INC., *130 Knowles Dr., Los Gatos, CA 95030 (408) 370-7979; Electronic Design, Jan. 11, p. 216* **Circle 389**

15.8-MIPS WORKSTATION COSTS UNDER $10,000

The SparcStation IPC performs 15.8 MIPS for under $10,000, one of many that were released in 1990 in this price range. The IPC costs about half of what a PC with similar features would cost, and it runs faster, has more storage, and has a larger, higher-resolution monitor. It comes with a 16-in. color monitor, 8 to 24 Mbytes of RAM, a 207-Mbyte hard disk drive, and two Sbus expansion slots. Sun's built-in Open Look graphical user interface makes the system simple to use. In addition, more than 2100 software applications are available for the Sparc architecture.

SUN MICROSYSTEMS INC., *2550 Garcia Ave., Mountain View, CA 94043 (415) 960-1300; Electronic Design, Sept. 27, p. 205* **Circle 390**

DSP BOARD MAKES MAC II A 33-MFLOPS WORKSTATION

The NB-DSP2300 digital-signal-processing (DSP) board turns the Macintosh II into a 33.33-MFLOPS workstation that can handle numerically intensive calculations. Combining this power with the I/O functions of other NB-series boards, users can get real-time signal analysis in measurement applications. The board, which uses Texas Instrument's TMS320C30 DSP chip, plugs into the Mac II's Nubus, supporting the block mode of the bus with an on-board DMA controller that transfers data at up to 33.7 Mbytes/s.

NATIONAL INSTRUMENTS CORP., *6504 Bridge Point Pkwy., Austin, TX 78730-5039 (800) 433-3488 or (512) 794-0100; Electronic Design, Apr. 26, p. 132* **Circle 391**

COMMUNICATIONS

SMART COMM CHIP HANDLES MULTIPLE PROTOCOLS

An intelligent peripheral has DMA capability and four full-duplex channels, each with user-selectable protocols for linking to data-communication equipment from different vendors. Each channel receives and transmits at up to 64 kbaud. On the chip are a 10-MIPS RISC CPU with three buses, firmware ROM, RAM, and interface logic for the host microprocessor. On-chip protocol-handling is controlled by the firmware ROM.

CIRRUS LOGIC INC., *1463 Centre Pointe Dr., Milpitas, CA 95035 (408) 945-8300; Electronic Design, Feb. 22, p. 157* **Circle 392**

FDDI CHIP SET VIES FOR FDDI BACKBONES

Targeted for FDDI backbone applications, the DP82300 chip family consists of a basic media-access controller (MAC), a physical-layer controller, a clock-recovery device, a clock distribution device, and the system interface device for the basic MAC. The chip set has a 32-bit interface that connects to such popular computer buses as the S-Bus, MCA, VME, EISA, and AT. Synchronous operation runs up to 25 MHz.

NATIONAL SEMICONDUCTOR CORP., *2900 Semiconductor Dr., Santa Clara, CA 95052-8090 (408) 721-3848; Electronic Design, May 10, p. 113* **Circle 393**

SIX-CHIP FAMILY FORMS FLEXIBLE COMPRESSION PIPE

A 40-MHz image-compression chip set supplies the architectural flexibility to track the still-evolving JPEG, MPEG, and H.261 standards for still- and motion-picture transmission. The L64700 family consists of an interframe processor, a discrete cosine transform (DCT) processor, a DCT quantization processor, a motion-estimation processor, a variable-length encoder, and an error-correcting encoder-decoder. Access to bus architectures makes it possible for proprietary compression algorithms to be added. External data-conversion is required.

LSI LOGIC CORP., *1525 Mc Carthy Blvd., Milpitas, CA 95035 (408) 433-8000; Electronic Design, Sept. 27, p. 173* **Circle 394**

COLOR DECODER IC EYES MULTIMEDIA DESIGNS

The SAA7151 video decoder can digitize a composite video signal in any of the three international broadcast standards: NTSC, PAL, and SECAM. Key to the device's capability is a line-locked clocking technique that synchronizes to the analog signal's line-sync pulse rather than to its color-burst signal. This allows for clean digital conversions from video broadcasts, VCRs, video disks, and still-video cameras.

PHILIPS COMPONENTS-SIGNETICS, *811 E. Arques Ave., Sunnyvale, CA 94088-3409 (408) 991-4577; Electronic Design, May 10, p. 130*
Circle 395

ARCNET CONTROLLER TRIMS LAN NODE CHIP COUNT

To bring the benefits of networked office environments to the factory floor, the COM20020 universal LAN controller incorporates the 2.5-Mbit/s Arcnet token-passing protocol in a 24-pin package that reduces node chip count by one-fifth. The device includes a microsequencer, a 2-kword-by-8-bit

COMMUNICATIONS

dual-port buffer RAM, an assortment of registers, bus-arbitration circuitry, a generic microcontroller interface, a flexible media interface, and a transceiver. Networks can be configured in star, bus, or tree topologies using twisted-pair, coaxial, or fiber-optic cable as the interconnection medium.

STANDARD MICROSYSTEMS CORP., *35 Marcus Blvd., Hauppage, NY 11788 (516) 273-3100; Electronic Design, Nov. 8, p. 147* **Circle 396**

ISDN CONTROLLER USES TELEPHONE-LINE POWER

During a power outage, the Am79C30A ISDN digital-subscriber controller disables its unused circuits and adjusts its clock frequency to suit traffic conditions. This enables its host ISDN terminal equipment to continue operating on telephone-line power in accordance with CCITT power specifications. The controller integrates an S/T interface transceiver, a LAPD controller, a microprocessor interface, a B-channel multiplexer, a serial port, and an audio codec filter.

ADVANCED MICRO DEVICES, *901 Thompson Pl., Sunnyvale, CA 94088-3000; Electronic Design, May 10, p. 130* **Circle 397**

MULTIMEDIA PROCESSOR COMPRESSES VIDEO, AUDIO

The UVC7710 multimedia processor is the first to integrate video and audio compression, video timing, and memory- and bus-control functions on one chip. Typical compression ratios range between 20:1 and 30:1. A real-time high-compression mode is for applications that need ratios of 500:1 or greater. The controller includes all required compression-code tables, and has JTAG boundary-scan testability.

UVC CORP., *16800 Aston St., Irvine CA 92714 (714) 261-5336; Electronic Design, Dec. 13., p. 43* **Circle 398**

SERIAL PACKET CONTROLLER EASES HIGH-SPEED DATACOM

For high-speed packetized serial communications in the PS/2 or PC bus environment, the 73M650 is configured as two main blocks. A 16550A main processor UART links to software written for 16450/16550A UARTs. A serial communications controller is an enhanced version of one channel of an 8530. With its flexible architecture, the device can be controlled by a host CPU and local protocol controller, or by one CPU that can access and modify transmitted or received data for multitasking applications.

SILICON SYSTEMS INC., *14351 Myford Rd., Tustin, CA 92680 (714) 731-7110; Electronics Design, Dec. 27, p. 31* **Circle 399**

CODEC CHIPS SEND VIDEO BY PHONE

Consisting of a discrete cosine transform processor and a motion-estimation device, the Videocodec chip set offers a 400:1 adaptive compression ratio for sending video images over telephone wire. This compression ratio reduces the bandwidth needed for video by four orders of magnitude. The chips operate with external loop filters, analog-to-digital converters, error-correction circuits, and memory.

SGS-THOMSON MICROELECTRONICS INC., *1000 E. Bell Rd., Phoenix, AZ 85022-2699 (602) 867-6279; Electronic Design, June 28, p. 129* **Circle 400**

REPEATER IC ADAPTS TO LINE CONDITIONS

A repeater IC needs only an external crystal and other components to complete a repeater design for restoring pulse-code-modulated signals distorted by transmission lines. The LXT312 is a dual repeater for North American T1 (1.544-MHz) applications, and the LXT313 is for European E1 (2.048-MHz) systems. Each chip has an automatic line build-out function to match 6300 ft. of 22 AWG cable.

LEVEL ONE COMMUNICATIONS INC., *105 Lake Forest Way, Folsom, CA 95630 (916) 985-3512; Electronic Design Nov. 22, p. 169* **Circle 401**

PACKAGING AND PRODUCTION

CONNECTORS PASS PULSES WITH TINY RISE TIMES

By maintaining a 50-Ω interconnection impedance, the MicroStrip connector acts as a digital transmission line to speed signals from board to board with a minimum of noise and distortion. Crosstalk is limited to less than 4% at 1-ns rise times. That means circuit runs in fast digital systems can be longer with less related ground noise. In addition, the connector crams 40 signal contacts into each linear inch of length, making for high effective density compared with conventional connectors. That's good news for designers of supercomputers, superminicomputers, minicomputers, workstations, high-end desktops, and high-end memory modules.

AMP INC., *P.O. Box 3608, Harrisburg, PA 17105-3608 (800) 522-6752; Electronic Design, Nov. 8, p. 164* **Circle 402**

TWO-METAL TAB TAPE INCLUDES GROUND PLANE

Controlled impedance and reduced crosstalk die makes a two-metal-layer TAB film right for attachment of high-lead-count, high-speed digital ICs. Fabricated using an additive process, the film is in production with 360 or more leads with 0.002-in. lines and spaces. The film is made using dimensionally stable materials and circuits are manufactured in panel form, which ensures correct part size and configuration. The film also facilitates device testing at or close to full speed. Current production products have 360 or more leads with 0.002-in. lines and spaces. Prototypes are in the 700-lead-plus range with 0.0015-in lines and spaces.

ROGERS CORP., MICRO-INTERCONNECTION DIVISION, *2001 W. Chandler Blvd., Chandler, AZ 85244 (602) 963-4584; Electronic Design, Sept. 27, p. 202* **Circle 403**

LASER-TAB BONDER QUICKLY BONDS COMPLEX ICS

Up to 65 leads per second are gently bonded by the model 7100 laser-TAB system. The system produces metallurgical bonds with consistent high quality without subjecting the IC to extreme mechanical and thermal stress. With laser TAB, bond pitch is limited only by the laser-beam diameter. Single-point bonders are physically limited by their tool size and gang bonders by their maximum pressure capability. Because laser bonding is a non-contact methodology, the bond pressure is extremely low—about 2 grams/lead. In addition, bond temperature is kept to a minimal 22°C. Also, the system can be changed over from one die to another in seconds by means of software control.

ELECTRO SCIENTIFIC INDUSTRIES INC., *13900 N. W. Science Park Dr., Portland, OR 97229-5497 (503) 641-4141; Electronic Design, Sept. 27, p. 202* **Circle 404**

SCANNED-LASER SYSTEM IMPROVES LITHOGRAPHY

More than 50% reduction in minimum feature size and a four-fold improvement in edge-placement resolution, compared with mask and reticle writing systems, is offered by the CORE-2500 scanned-laser lithography system. The system meets producers' needs for 250,000- and 500,000-gate arrays and 4- and 16-Mbit dynamic RAMs. To achieve submicron minimum feature size and edge-resolution gains, a high numerical-aperture (0.6), 20X post-scan lens yields a minimum address size of 0.025 μm. The system is capable of writing high-quality 1X reticles and 1X projection masks.

ATEQ CORP., *9100 Gemini Dr., Beaverton, OR 97005 (503) 626-3051; Electronic Design, Feb. 8, p. 131* **Circle 405**

Consider Testability In Your Next Design

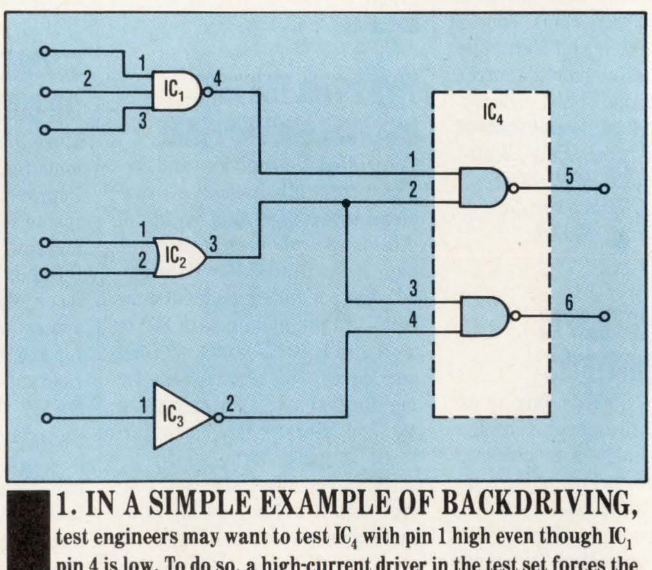
A Test Engineer Shares Some Valuable Design-For-Test Tips In This Heart-To-Heart Talk With Designers.

As circuit cards become more complex and densely packed, testing them becomes more difficult, elevating the importance of design-for-testability (DFT) rules. From a test engineer's perspective, however, DFT rules often take second place to circuit functionality or timing considerations in the parts being used. But if circuit designers learn more about the problems of testing completed circuit cards, they may be more concerned with implementing DFT rules in their designs.

That's why test engineers are always eager to open a dialogue between their counterparts involved in circuit design. This article represents one test engineer's approach to opening such a dialogue.

The most obvious way to test cards is to plug them into a golden (known-good) system and see what happens. If the system works, the card is okay; if not, the card is defective. That's easy. The problem in circuit-card testing is isolating the faults in the defective cards. Fortunately, automatic test equipment (ATE) is available that not only performs go/no-go tests on circuit cards, but also isolates faults in defective cards.

There are two basic ways to test circuit cards using ATE: functional testing and in-circuit testing. Functional, or edge-connector, testing involves plugging the card into the ATE and running programs that check out the circuit's operation. In-circuit ATE tests the card by making electrical contact with every net (sometimes referred to as a node) of the circuit using a fixture called a "bed of nails." The fixture is so named because it carries hundreds, or even thousands, of probes.



1. IN A SIMPLE EXAMPLE OF BACKDRIVING, test engineers may want to test IC_4 with pin 1 high even though IC_1 pin 4 is low. To do so, a high-current driver in the test set forces the desired input high.

In-circuit ATE has many advantages over functional ATE. For instance, in-circuit ATE can use "canned" programs (that is, a device library) to test parts of a board. In addition, this technique offers excellent short-circuit detection and fault isolation down to the defective part in most cases. As a result, in-circuit testing is the preferred approach.

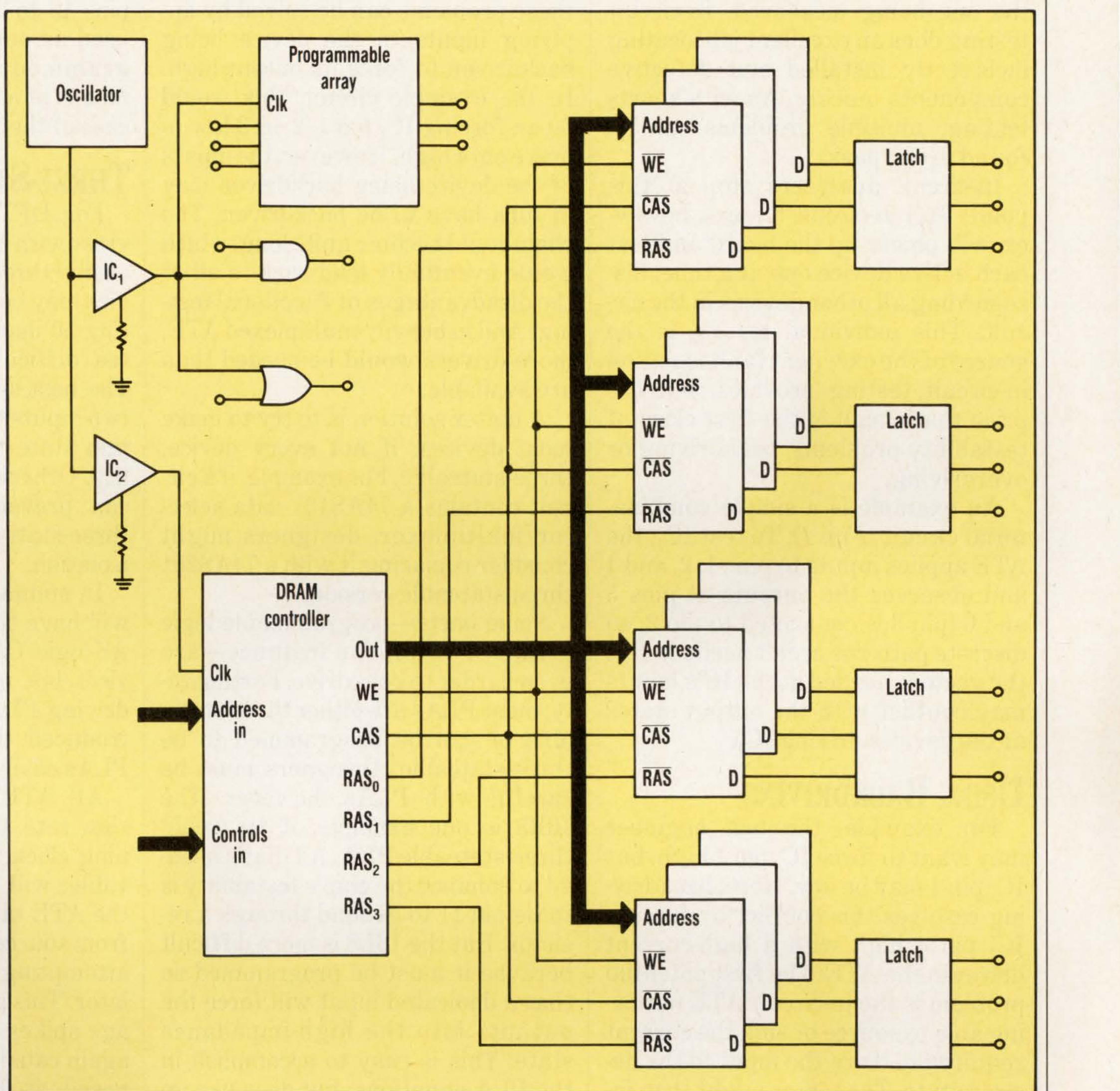
By its nature, however, in-circuit ATE contacts the circuit board in places that were never meant to be contact points and backdrives devices on the card to states where they weren't intended to be. Because of these peculiarities, in-circuit tests can sometimes be inconsistent. Although test engineers are aware of this problem, they know that the technique's advantages far outweigh the disadvantages.

The proliferation of surface-mounted devices, which are difficult to probe, may make continued use of in-cir-

SOL L. BLACK
AT&T Network Systems,
6200 E. Broad St., Columbus, OH 43213; (614) 860-5605.

cuit testing impossible. Most manufacturers are urging designers to employ DFT rules so that conventional in-circuit ATE can still be used. In some cases, using cluster testing can avoid especially difficult situations on parts of a board. Thus, it's advisable for in-circuit ATE to have some combinatorial testing ability.

Boundary - scan techniques may also play a part in the future of card testing. It's unclear yet whether boundary scan will be able to easily diagnose short circuits or if the boundary-scan test will follow an abbreviated in-circuit test. Hardware standards for boundary-scan designs have been established (IEEE-1149.1), but the software needed for designing with scan and for testing and fault isolation with scan is still in its early stages. In any event, it appears that in-circuit testing will be around for a long time.



2. DESIGNERS MAY HAVE TO SPLIT a clock output to permit proper in-circuit testing. In this circuit, the addition of three-stateable buffers (IC_1 and IC_2) enables the tester to keep the DRAM controller clock running while the clock to other devices is turned off.

For in-circuit testing, the tester first ensures that every probe makes electrical contact with its node. One approach is to force a small current through every probe. The ATE then looks for a forward diode junction drop caused by either a diode on a semiconductor somewhere on the node or by the substrate itself. If no drop is present on any given net, that probe can't be tested for contact. But this problem usually occurs on only a few nets in any given circuit.

Another way to test for contact is to force one node on a card high (or low) and tie all of the other nodes to the opposite state through a load. If the nodes are making proper contact, they should all go to the driving node's state. If a production board fails this fixture test, the test is aborted and the ATE operator looks for a problem, such as a dirty board or a stuck fixture probe.

Looking For Shorts

If the fixture test passes, the tester performs a shorts test from every net to every other net. If yields at this stage are high, the shorts test may be done only on boards that fail other in-circuit test steps. Quick and accurate detection of shorts is one of the outstanding features of in-circuit testing. The ATE locates even multiple shorts on a card in one pass. On some ATE, a form of artificial intelligence guesses the most likely location of a detected short. If one or more shorts are found, the tester aborts the sequence and generates a list of shorts for the repair station.

After the shorts test comes power-down component tests, which usually include resistors, transformers, capacitors, inductors, and diodes. The ATE tests these parts one at a time using dc and ac sources and detectors. A technique called guarding is often used to cancel the effect of other components in parallel with

DESIGN-FOR-TEST TIPS

the one being measured. In-circuit testing does an excellent job locating incorrectly installed and defective components quickly. As with shorts testing, multiple problems can be found in one pass.

In-circuit analyzers stop at this point. Full in-circuit testers, however, will power-up the board and test each active device one at a time, disregarding all other devices in the circuit. This individual testing is the source of the excellent fault isolation in-circuit testing provides, but the price that's paid is the first class of testability problems, backdriving or overdriving.

An example is a simple combinatorial circuit *(Fig. 1)*. To test IC_4, the ATE applies inputs to pins 1, 2, and 4 and observes the outputs at pins 5 and 6 (pin 3 is connected to pin 2, so discrete patterns aren't needed). But the vectors needed at the IC's inputs may conflict with the output states of the devices driving IC_4.

USING BACKDRIVING

For example, the test engineer may want to force IC_4 pin 1 high, but IC_1 pin 4 may be low. Here, backdriving resolves this conflict by forcing IC_1 pin 4 high with a high-current driver in the ATE. The first potential problem is the in-circuit ATE not being able to source or sink the current required to drive the input to the desired state. The tester might then indicate that a good device is defective.

Moreover, the potential for device damage limits current sourcing and sinking. Most ATE restricts backdriving so that it doesn't damage devices. Protection might take the form of hardware, software, or a combination of both. Most in-circuit testers also account for the differences in backdriving various types of devices. For example, AS- and F-type TTL parts are more difficult to backdrive than ALS or LS parts.

In addition, it's easier to backdrive TTL outputs to a low state from a high state rather than drive from high to low. Therefore, some of these problems can be solved by applying inputs to the device being backdriven to force its output high. In the example circuit, this would mean forcing IC_1 pin 1, 2, or 3 low to make pin 4 high. However, the inputs of the device being backdriven may in turn have to be backdriven. The chain could become quite long, which would eventually lead back to all of the disadvantages of functional testing. And in heavily multiplexed ATE, more drivers would be needed than are available.

A better solution is to try to make most devices, if not every device, three-stateable. For example, if a circuit contains a 74AS151 data selector/multiplexer, designers might consider replacing it with a 74AS251 three-stateable version.

Some parts—programmable logic arrays (PLAs), for instance—are even harder to backdrive. Fortunately, most PLAs are either three-stateable or can be programmed to be three-stateable. Designers must be careful with PLAs, however. The 16R8 is one example of an easily three-stateable PLA. All that's needed to enhance the chip's testability is to tie pin 11 to ground through a resistor. But the 16L8 is more difficult because it must be programmed so that a dedicated input will force the outputs into the high-impedance state. This is easy to accomplish in the PLA equations, but does use up one device input.

On the other hand, the 16R6 can be misleading. Although pin 11 is a three-state lead, it only three-states pins 13 to 18. If pins 12 and 19 are used as outputs, they must be programmed to be three-stated by means of a dedicated input, as in the case of the 16L8.

THREE-STATE PARTS

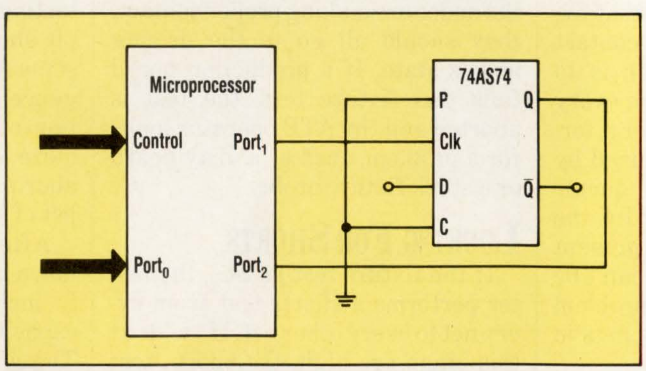
For DFT purposes, then, all devices with outputs on a bus must be easily three-stateable. A VLSI device may be three-stateable by inputting 50 lines of code to it, but this is too difficult for in-circuit testing. The best situation is to have one or two inputs that can be placed in a certain state to ensure three-stateability. Otherwise, errors in the circuit can prevent a good device from three-stating and cause false fault isolation.

In summary, some in-circuit ATE will have trouble backdriving F and AS logic. Others can handle these devices but might have trouble backdriving PLAs. Some newer ATE, introduced this year, can backdrive PLAs easily.

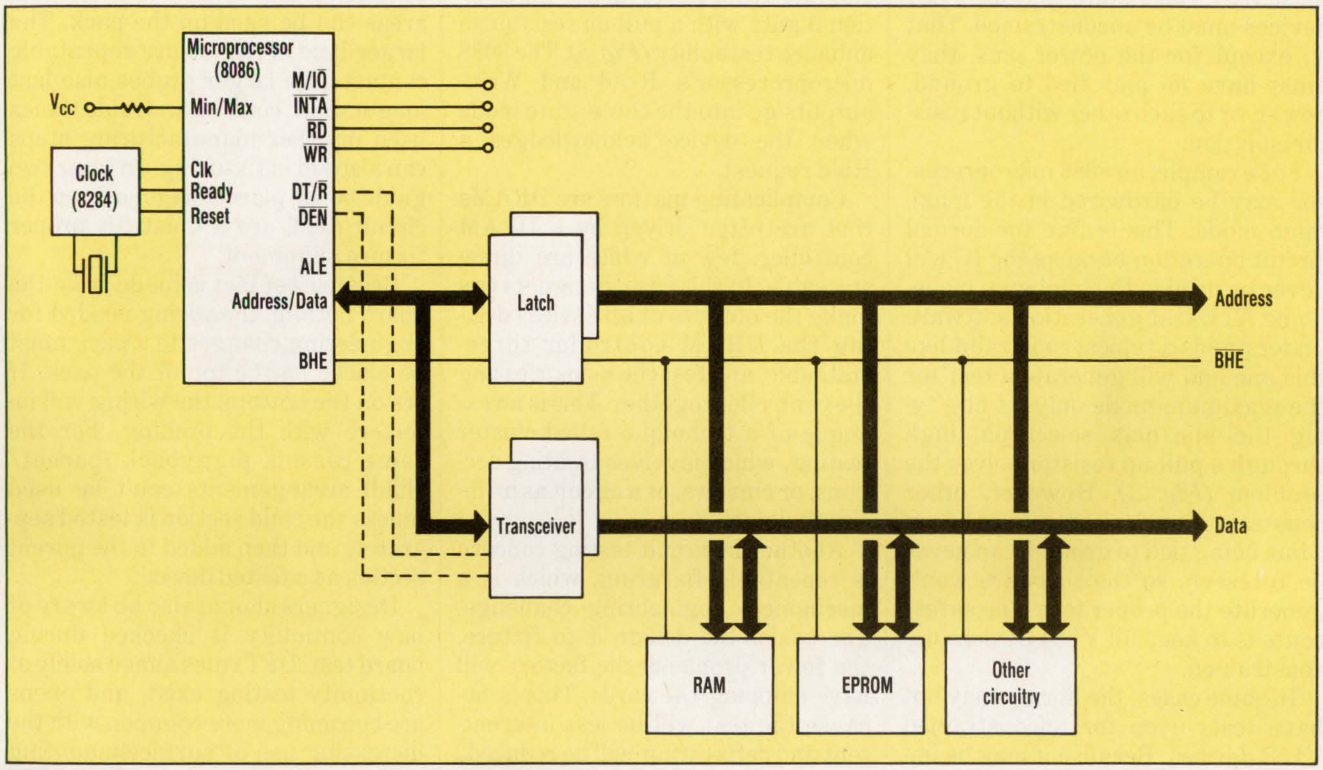
All ATE, however, has a finite slew rate. Consequently, a free-running clock, even one that's backdrivable, will cause problems because the ATE takes some time to change from source to sink and back again in attempting to keep up with the oscillator. This phenomenon creates voltage spikes on the board under test, again causing good parts to be diagnosed as bad. Edge-triggered devices are particularly susceptible. As a result, the circuit card must provide for turning off oscillators. Oscillators that are three-stateable are the best for this purpose.

Sometimes, however, oscillators must be kept running in order to keep certain devices, such as dynamic RAMs (DRAMs), three-stated, but must be turned off to test the rest of the devices on the board. In this case, designers must split the oscillator output so part of it can be turned off while the other part runs.

An example of this problem is a circuit in which one oscillator is shared with a DRAM bank driven by a



3. FEEDBACK LOOPS, **which can be difficult to spot in complex circuits, can hinder in-circuit testing. In this example, when the 74AS74 is tested, its Q output will change, affecting the microprocessor's input. This changes the tested device's input.**



4. SOME ATE SOFTWARE CAN ACCOMMODATE typical constraints placed on components by designers. In this example, an 8086 microprocessor is hardwired in the maximum mode with the min/max select pin tied high through a pull-up resistor. Test-generation software that understands this constraint will create a test for the maximum mode only.

DRAM controller, and with some other clocked circuitry *(Fig. 2)*. The ATE must supply the clock during testing of the non-DRAM circuitry, so the board's clock must be three-stated. Three-stateable buffer IC1 accomplishes this while the clock to the DRAM controller and bank remains free running. When the ATE tests the DRAM bank, the memory's portion of the clock output must be three-stated. Another three-stateable buffer, IC_2, performs this task.

Feedback Problems

Feedback loops can cause a similar problem. If the tested device's output feeds a device whose output goes to the input of the tested device, that feedback path must be broken during the test. This can be done by three-stating or otherwise quieting the device in the feedback path or by breaking the path by using some other method.

A simple example of a feedback problem is a 74AS74 in a loop with a microprocessor. The microprocessor feeds the 74AS74, whose Q output is fed back to the microprocessor *(Fig. 3)*. When the 74AS74 is tested, its output will change, causing the microprocessor's input to change, which in turn changes the microprocessor's output to the 74AS74. The glitch that occurs when the ATE attempts to go from source to sink, or vice versa, may falsely trigger the 74AS74 under test and cause a good device to appear defective. One way to break this feedback loop is to insert a gate in the loop for testability purposes.

Feedback loops are difficult to spot, especially in large circuits covering many pages. Often the loop extends over several pages and isn't immediately obvious. Some vendors offer software that detects these problems.

As noted, one advantage of in-circuit testing is that test programs can be stored in a library for later reuse. For example, once a test for a 74LS00 gate is written, every time this device occurs on a board, the tester's automatic test generator program retrieves this test from the library. A hitch occurs when designers use a device in an unexpected way, creating what's called a constraint.

For example, the designer may tie pins 1 and 2 of the 74LS00 together to create an inverter. Some automatic test generators will understand this constraint and attempt to generate a test. Others will search through their library and try to find a test written specifically for this constraint. If the ATE can't do these things, then the test engineer must write a test for this specially constrained device.

Avoid Constraints

This isn't a challenge for the 74LS00, but writing a new test for a VLSI device, such as a 68000, might be a major problem. Tests for VLSI devices take several months to write and are worth several thousand dollars. Therefore, most available test programs are written for devices with no constraints. For this reason,

DESIGN-FOR-TEST TIPS

most DFT rules state that all VLSI devices must be unconstrained. That is, except for the power pins, they must have no pins tied to ground, power, or to each other without resistor isolation.

For example, an 8086 microprocessor may be hardwired in the maximum mode. This is fine for normal circuit operation because the IC will never be used in the minimum mode. Some ATE test generation software understands a typical constraint like this one and will generate a test for the maximum mode only. If not, tying the min/max select pin high through a pull-up resistor solves the problem *(Fig. 4)*. However, other constraints, such as an unused line in a bus being tied to ground, can never be foreseen, so the software won't generate the proper test. The safest route is to keep all VLSI devices unconstrained.

In some cases, the library may not have tests even for unconstrained VLSI devices. Because it may be impractical for engineers to write these tests, any self-testing capability, particularly if it can pinpoint a part of the circuit, is useful. This capability will prevent the passing of a defective card containing a device that's untested.

At AT&T Columbus, every cell of a dynamic RAM is usually tested, employing in-circuit techniques. Even at 2 or 3 MHz, this testing takes at least several milliseconds. Therefore, to prevent excessive backdriving, designers are asked to use only devices with three-stateable outputs to drive DRAMs.

In a typical example, the 8282 latch used for the address bus and the 8286 transceiver used for the data bus are both made three-stateable. The latch requires only a pull-down resistor on the output enable lead. But the transceiver needs an additional gate with a pull-up resistor to enhance testability *(Fig. 5)*. The 8088 microprocessor's Read and Write outputs go into the three-state mode when the device acknowledges a Hold request.

Complicating matters are DRAMs that are often driven by a DRAM controller, few of which are three-stateable. In this case, designers can make the outputs of all devices driving the DRAM controller three-stateable, and test the memories and the controller together. This is an example of a technique called cluster testing, which involves treating sections, or clusters, of a circuit as an in-circuit device.

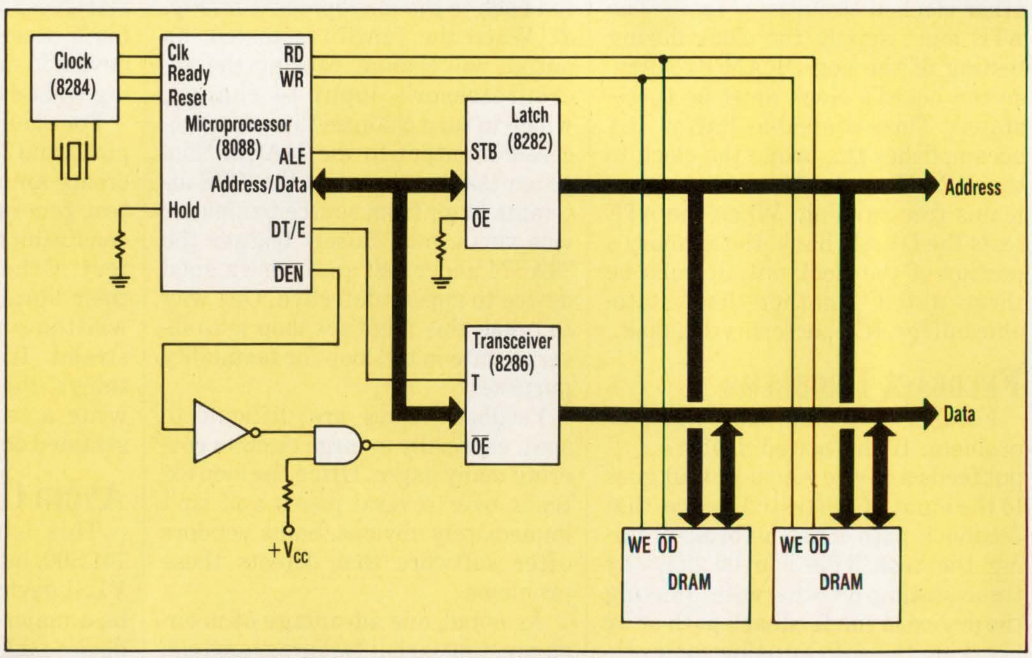
Another in-circuit testing concern is repeatable fixturing, which is a mechanical engineering challenge. The easier the design is to fixture, the fewer problems the factory will have shipping the cards. This is because the test will be less intermittent and refixturing will be reduced.

One fixturing decision that needs to be made is probe size. Although there are fixture probes that will fit on 50-mil or smaller centers, most vendors recommend using 100-mil centers so that 40-mil-diameter land areas can be used on the pack. The larger land areas ensure repeatable contact. The larger probes also last longer and cost less. Guide holes used in other manufacturing steps can also aid in fixturing. At least two guide holes, placed diagonally on the circuit card, are a must for proper fixture alignment.

Because contact is made from the board bottom, the wiring needed for engineering changes to a pack must be placed on the top of the pack. If it's on the bottom, the wiring will interfere with the probing. For the same reason, piggyback (parent/child) arrangements can't be used unless the child section is tested separately and then added to the parent section as a tested device.

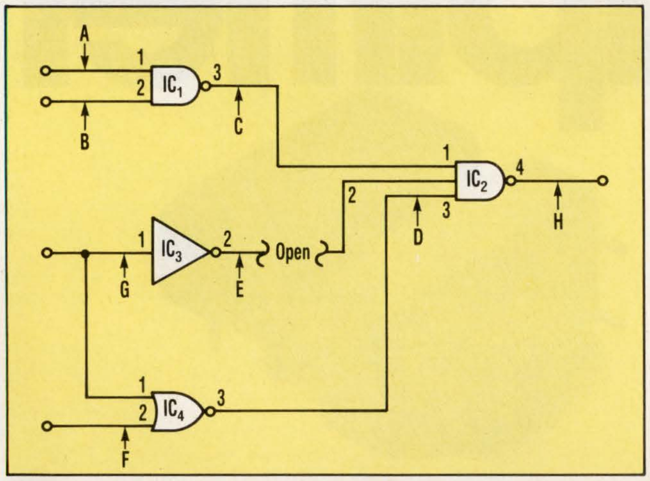
Designers should also be aware of how continuity is checked during board test. DFT rules aimed solely at continuity testing exist, and opens are becoming more common with the increasing use of surface-mounting technology.

If a device fails its test, the ATE software asks the operator to touch a grounded probe to every lead on the device. The ATE knows which of



5. TO PREVENT EXCESSIVE BACKDRIVING during memory testing, DRAMs should be driven by three-stateable devices, such as the 8282 latch and 8286 transceiver in this circuit. The latch requires only a pull-down resistor on the output enable lead, while the transceiver needs an additional gate with a pull-up resistor.

its probes are connected to the nodes going to each of the device's leads, so the tester looks for a ground occurrence at these probes. If a ground occurrence is found at every probe, the ATE assumes the device is wired correctly and generates a fault-isolation message telling the operator that the device is bad. If, however, one or more of the designated probes doesn't go to ground, the failure message signals an open path (or a defective solder joint).



6. CONTINUITY PROBLEMS, such as the open circuit in this example, are detected by probing failing devices from the top of the board. Most device packages offer access for this probing, but pin-grid packages are one type that doesn't.

An example is a circuit with an open between IC_3 pin 2 and IC_2 pin 2 *(Fig 6)*. The fixture places one ATE probe on each net. If IC_3 is good, it will pass its test because both the probes associated with that test make good contact with IC_3. But the IC_2 test will fail because probe E doesn't make contact with IC_2 pin 2. When the operator touches each pin of IC_2 with a grounded probe, the ATE finds ground occurring at probes C, D, and H, but not at E. Therefore, the software reports that there's an open wire at IC_2 pin 2. The cause could be a broken path, a defective solder joint, or a bent lead.

This continuity checking technique is called "scratch probe" or "etch probe" by various vendors. The procedure not only allows in-circuit testing to get away with only one probe per node or net, but also provides excellent fault isolation for open paths.

For the technique to work, every lead of every device must be accessible from the top of the board. This isn't a problem with conventional DIP packages or even most surface-mounted packages. And ZIP and SIP packages can be probed with special probes resembling dental tools. Pin-grid packages, however, are among those that simply can't be probed from the top. Some devices, such as many from AT&T Microelectronics, have pads on top of the device for this probing. These pads are also useful in troubleshooting the circuit using other test techniques.

The most important thing to remember is that in-circuit DFT rules change with the type of test equipment used, the test strategy employed on the circuit board, and the experience of the test engineer involved. Furthermore, the rules evolve as test engineers learn more about techniques and as new device and packaging technologies are introduced. Therefore, the test engineer and the design engineer must work together as a team from the very beginning of the design stage. Changes made after a DFT review must be discussed with the test engineer to see how testing is affected.□

Sol L. Black, a senior test engineer at AT&T's Network Systems plant in Columbus, Ohio, received his degree from the University of Cincinnati's OMI College of Applied Science in 1963.

HOW VALUABLE?	CIRCLE
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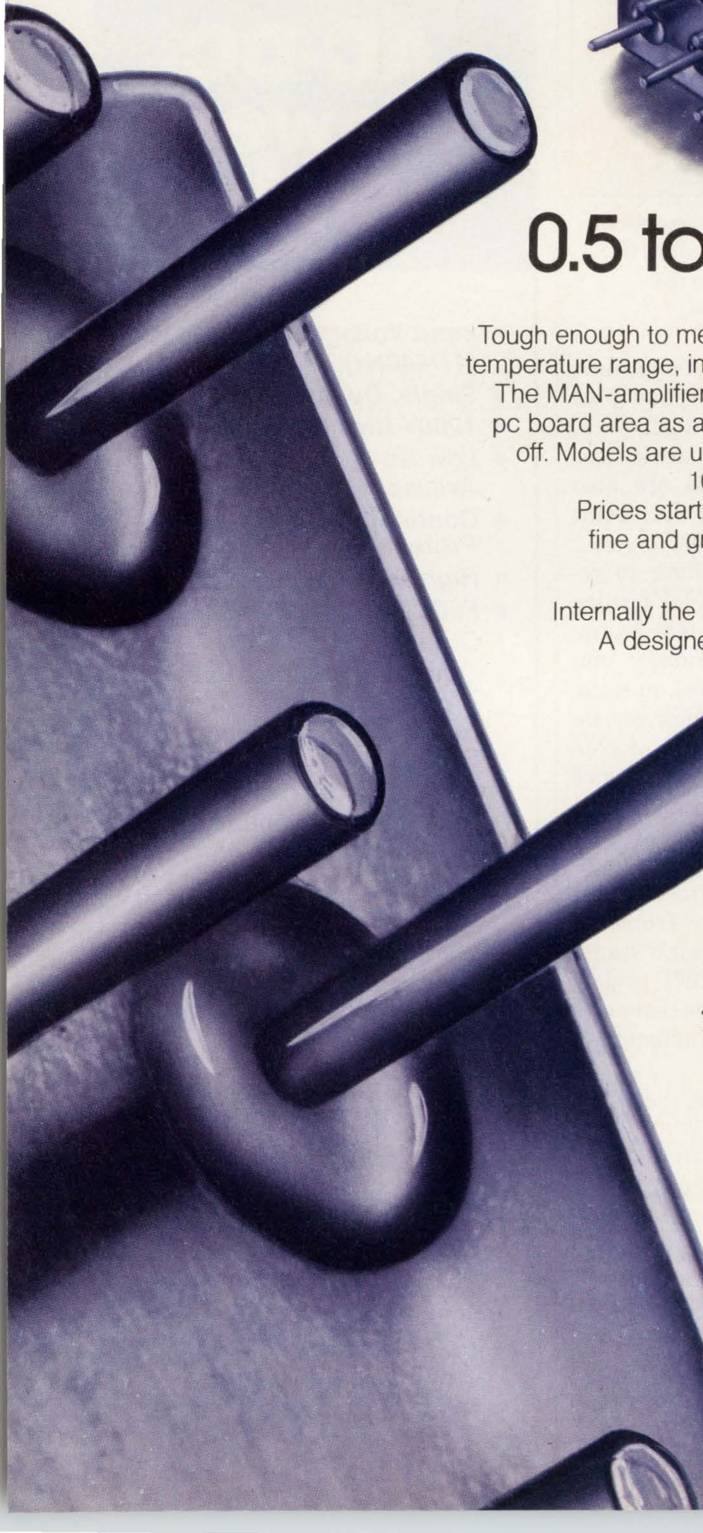

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◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
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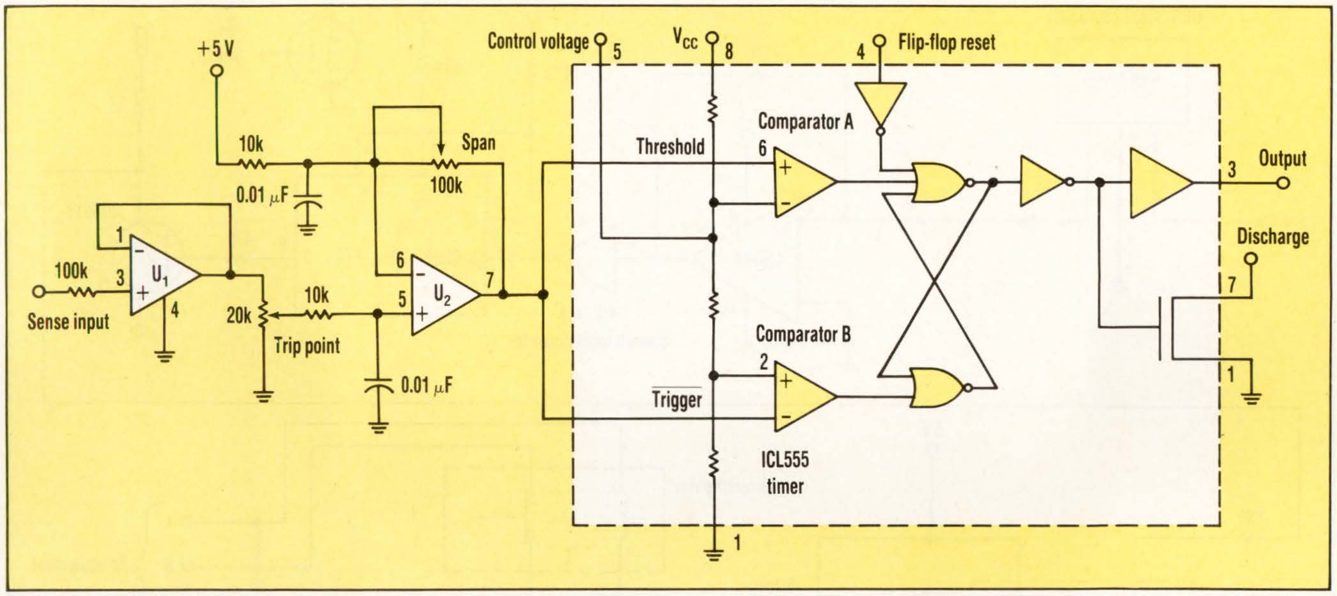
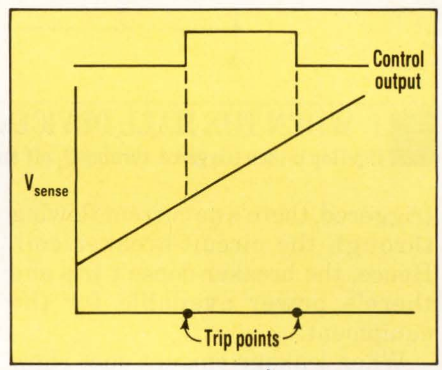
CIRCLE 105

C118 REV. E



1. BUILT AROUND A 555 timer, this circuit senses analog signals and controls digital signals.



2. THE CIRCUIT'S CONTROL output changes state when a trip point is detected.

CIRCLE 521

DETECT, CONTROL TRIP POINTS

GARY KNIPPER
Harris Semiconductor, 1101 Perimeter Dr., Suite 600, Schaumburg, IL 60195; (708) 240-3495.

Many applications require that analog signals be sensed and digital signals be controlled. A way to detect these points is by using a 555 timer in an unconventional configuration. This method will also add hysteresis to the circuit and guard against oscillation. The 555 supplies two comparators and a flip-flop. The flip-flop eliminates the oscillation. Using this classical timer in the new configuration also reduces the component count.

The circuit shows the 555's trigger and threshold pins tied together *(Fig. 1)*. This enables the comparators to set and reset the flip-flop. Op amp U_2 supplies both the trip-point setting and a way to adjust the hysteresis for on and off points *(Fig. 2)*.

One application where this circuit would be useful is in a NiCd battery-charge controller.□

CIRCLE 522

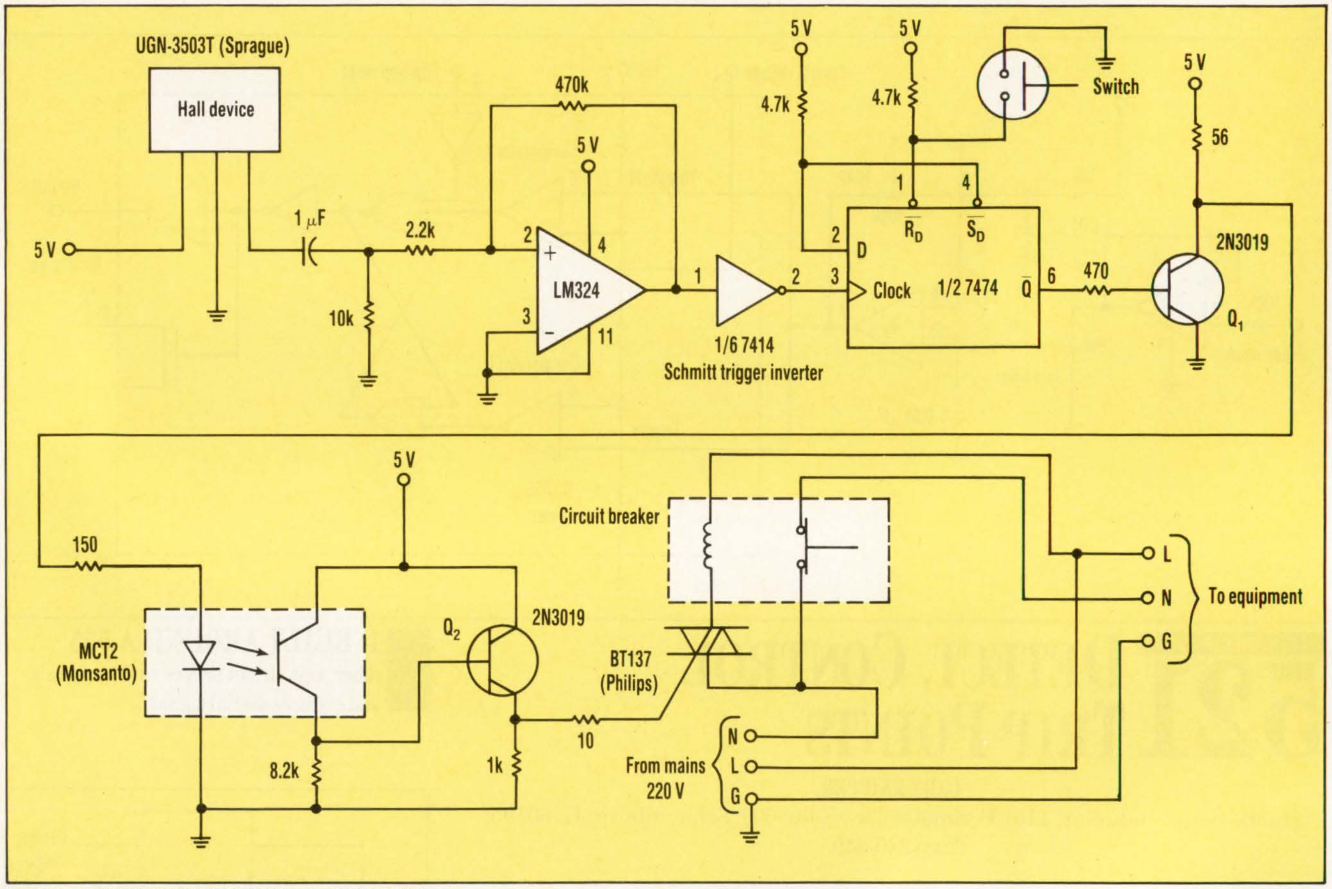
DETECT EARTH-LINE LEAKAGE CURRENT

V. LAKSHMINARAYANAN
Centre for Development of Telematics, Sneha Complex, 71/1 Miller Road, Bangalore 560 052 India.

A very low cost Hall-effect sensor can be used to build an earth-line current-leakage detector that has no physical contact with the ac lines. The detector can also trip the power supply when a leakage is detected in the earth line, preventing shock hazards.

The circuit uses a Sprague Hall-effect linear sensor (UGN-3503T) that can sense relatively small changes in the magnetic field around the device *(Fig. 1)*. The sensor's output is capacitively coupled to an op amp (1/4 LM324) whose output is made logic compatible and shaped using a Schmitt trigger inverter.

When there's no current leakage, transistor Q_1 is on (when the D flip-flop is in the reset condition) and the optocoupler transistor is off. This turns off Q_2 and takes away the gate drive to the triac. Since the triac isn't

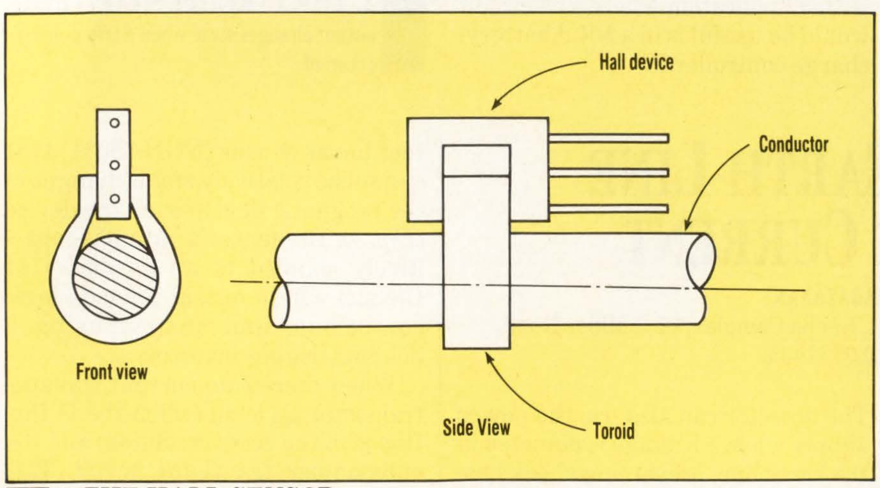


1. WHEN THE HALL DEVICE senses a magnetic field, a voltage appears at the sensor's output and is amplified by the op amp. The flip-flop is then triggered, turning Q_1 off and Q_2 on. This causes Current to flow through the breaker's coil, tripping the breaker.

triggered, there's no current flowing through the circuit-breaker coil. Hence, the breaker doesn't trip and there's power available for the equipment.

When leakage current does show up in the earth line due to some type of fault, a magnetic field is caused around the conductor which affects the Hall sensor. Hence, a voltage appears at the sensor's output. The op amp amplifies this voltage causing the Schmitt trigger to switch state. The transition triggers the D flip-flop at the rising edge and sets its Q output high. The flip-flop's state change turns Q_1 off and the opto-coupler transistor and Q_2 on. This causes the triac to be triggered by the gate drive and a current to flow through the circuit-breaker coil, tripping the breaker and isolating the equipment's ac supply from the ac main supply. This process will prevent a shock hazard.

The Hall sensor is mounted around the earth conductor to detect the leakage current *(Fig. 2)*. An appropriate-diameter toroid is formed from a mild steel material of suitable size. The ends are formed to fit on each side of the central portion of the sensor. Because the circuit is very simple and low cost, it can be used in an assortment of applications where prevention of shock hazard is of importance.□



2. THE HALL SENSOR is in such a way as to detect the leakage current. The toroid, made of steel, fits around the conductor and is magnetically coupled to the sensor.

CIRCLE 523

OP AMP REGULATES ITS OWN SUPPLY

M.S. NAGARAJ
ISRO Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore 560017 India.

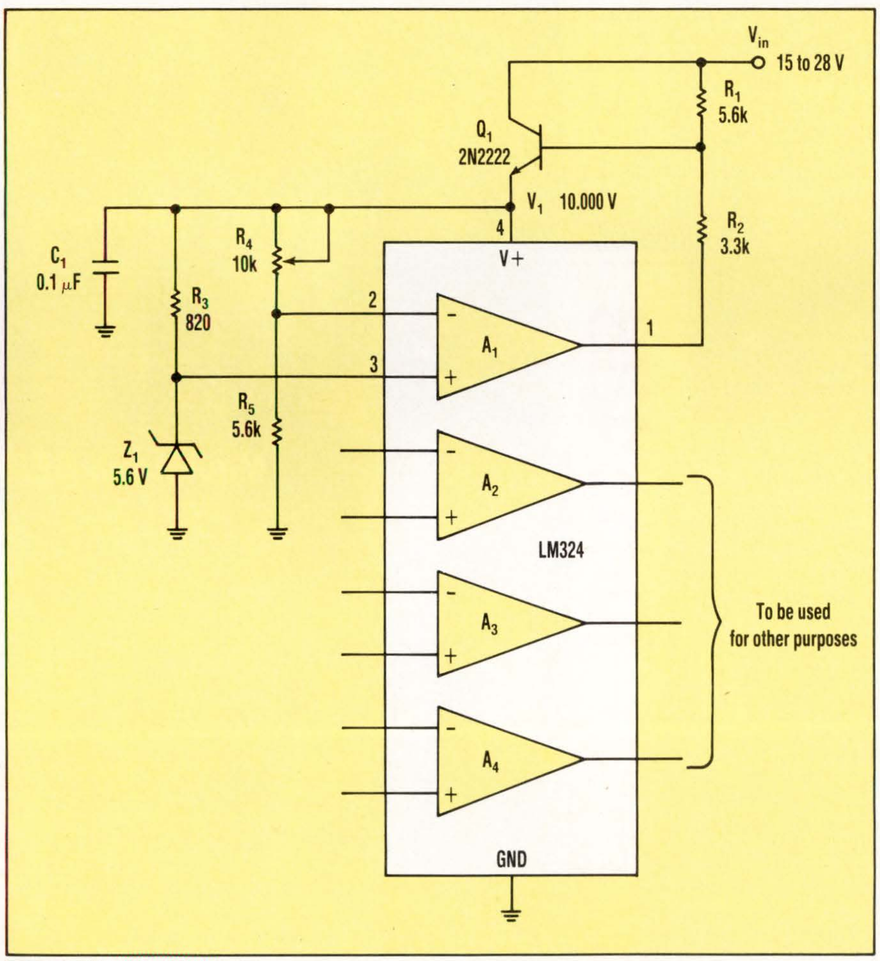
To function properly, analog comparators and their potential dividers that provide reference voltages should be powered by well-regulated supplies. In many cases, quad comparators or quad op amps used as comparators are operated in single-supply mode and are energized by three-pin regulator ICs.

A quad comparator or op amp and its associated circuits can be powered by a precision supply with a line regulation of better than 0.05%. This is done by adding a transistor, a Zener diode, and a few resistors to one of the four amps on the same IC. It's also possible to trim the precision power-supply voltage.

This op-amp circuit offers a straightforward method of developing a single-polarity stable voltage source *(see the figure)*. Transistor Q_1 gets a base drive through resistor R_1, and conducts to develop a voltage (V_1) across the IC's supply pins. Amp A_1, R_2, and Q_1 form a positive-feedback closed loop along with R_3 and the Zener diode. A_1, R_2, and Q_1 also form a negative-feedback closed loop with R_4 and R_5. The effect of positive feedback is predominant as the noninverting input receives V_1 while the inverting input receives only $V_1 \times [R_5/(R_4 + R_5)]$. This happens until the Zener comes into play. When the voltage at the inverting input exceeds the voltage at the noninverting input, A_1's output takes away Q_1's base current through R_2, reducing V_1. Hence, an equilibrium condition is reached. Now,

$V_1 = V_Z(R_4 + R_5)/R_5$.

When tested in practice, V_1 was trimmed to 10.000 V and stayed at that value for an input voltage variation from 15 to 28 V. Besides energizing the IC, it was also determined that the circuit can source 30 mA, which is more than enough to energize the potential dividers. It's also enough to drive control circuits, such as relay and lamp drivers associated with other amps on the same IC.□



ONE OP AMP on this quad op-amp IC regulates the reference voltage for the whole chip. A_1, along with a transistor, a Zener diode, and a few resistors can precisely supply the chip's reference voltage, even when V_{in} varies from 15 to 28 V.

Correction: In the November 22 Ideas for Design section, Fig. 2 for "Derive Stable dc from ac Current" should have had a connection from the cathode of D_2 to the bottom of C_1.

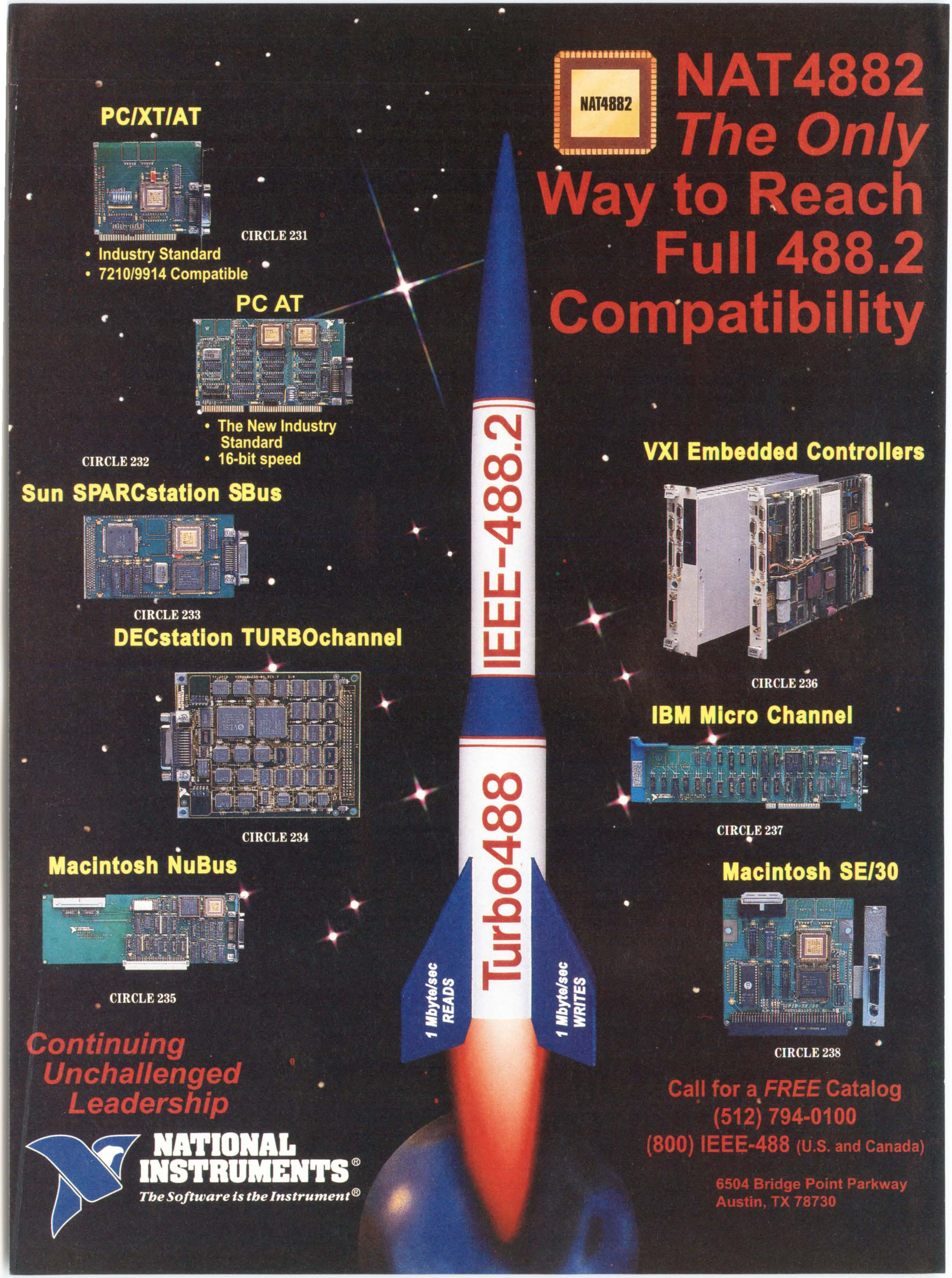
IFD WINNER

IFD Winner for August 23

Vittal Rao, Isro Satellite Centre, Digital Systems, Div., Airport Rd., Vimanapura P.O., Bangalore, India 560 017. His idea: *"Daisy Chaining Saves A DMA Chip."*

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.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QUICK LOOK

EDITED BY SHERRIE VAN TYLE

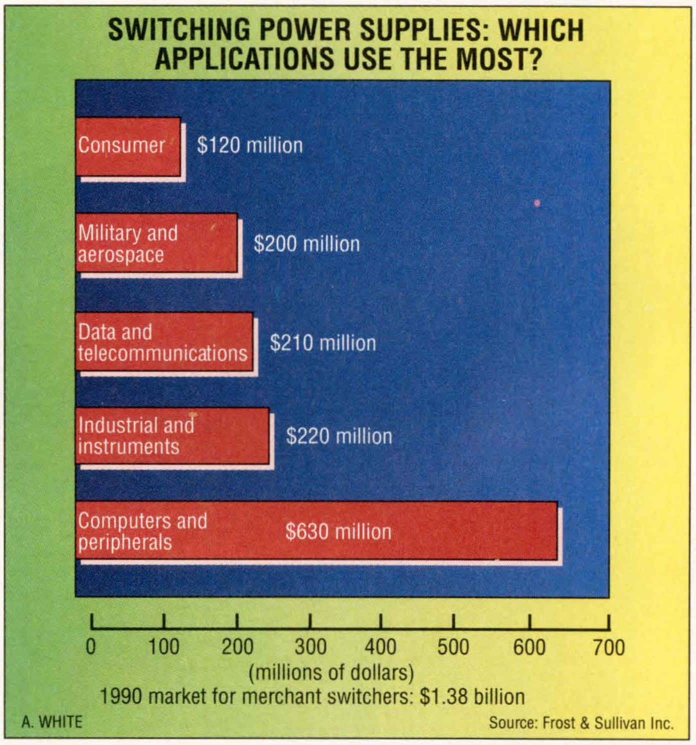
MARKET FACTS

To keep pace with electronic equipment, the humble power supply has changed shape. Linear supplies, which consist of a transformer, rectifier, filter, and linear regulator, can't keep up. Into the gap steps the switching power supply.

Switchers commanded just 17% of the power-supply market in 1979. By last year, they had taken the lead from linear supplies to snare 63% of the market. The total switching market, worth $3.5 billion, should nearly double, reaching $6.9 billion by 1995. That's the word from New York market researchers Frost & Sullivan Inc.

More and more supplies are tapping resonant power conversion for lower power losses during the switching transition. As in other electronic devices, designers are trimming footprints and packing more power into the supplies.

Many system and equipment makers build their own supplies. As a result, the captive share of the switcher market stood at 65% last year, the merchant share at 35%. By 1995, merchant share is expected to grow to 38%, spurred by growth in custom designs. Fastest growing in the merchant sector are medium power switchers of 150 to 500 W for applications such as point-of-sale systems and industrial and process control. Also look for a bigger emphasis on marketing techniques as the merchant supply sector becomes even more customer-driven.



OFFERS YOU CAN'T REFUSE

A programmer's reference manual describes how to program the new SL Superset, Intel's chip set for notebook computers built around the 386SL microprocessor. *The 386SL Microprocessor SuperSet Programmer's Reference Manual* explains the workings of the 386SL and the 82360SL peripheral controller, which make up the chip set. The manual sells for $25.95.

The *386SL Microprocessor SuperSet System Design Guide* gives hardware information and design tips. Intended for readers familiar with microprocessor operating principles, the manual begins with an outline of the SuperSet architecture. The guide then gives details and design examples for each of the set's system bus interfaces. The manual sells for $24.95. For additional information, call (800) 548-4725.

HOT PC PRODUCTS

A cordless mouse works up to four feet away from its receiver, linked by infrared light. Since Zen Mouse uses two-wheel direct drive, it doesn't become clogged with dirt and debris, says its maker, Zeny Computer Systems Inc. In addition, no mouse pad is needed. Zen mouse lists for $129; the OEM price is $55. For more information, contact the company at 4033 Clipper Ct., Fremont, CA 94538; (415) 659-0386; fax (415) 659-0468.

Toggling between DOS and Unix applications is becoming more common. Unix is moving onto the desktop as users continue to run DOS applications. ICE.TEN software links the two operating systems. Deja Vu, the program's terminal emulator, lets a PC double as a terminal on a Unix system. Users can switch between DOS and Unix with a pair of keys. UCOPY transfers files over a serial line connecting a DOS computer and a host. ICE.TEN is $295 per Unix system (286 or 386 Unix or Xenix) and up to eight DOS PCs can be attached to that system. For more information, contact the James River Group Inc., 125 N. First St., Minneapolis, MN 55401; (612) 339-2521.

A computer alarm concealed in the case senses a PC being moved and blasts a siren. A potential thief cannot snip a cable or break a lock to silence the alarm, which resets in 30 seconds. The PC Screamer, which is 3 3/4 by 2 3/8 by 1 in., attaches to the inside of the PC's case. Then the power cable is plugged in line with a disk drive power cable. From Vantage Point Technologies, the unit sells for $39. For more information, contact the company at 1318 East Mission Road, Suite 376, San Marcos, CA 92069 (619) 565-1863; fax (619) 278-3773.

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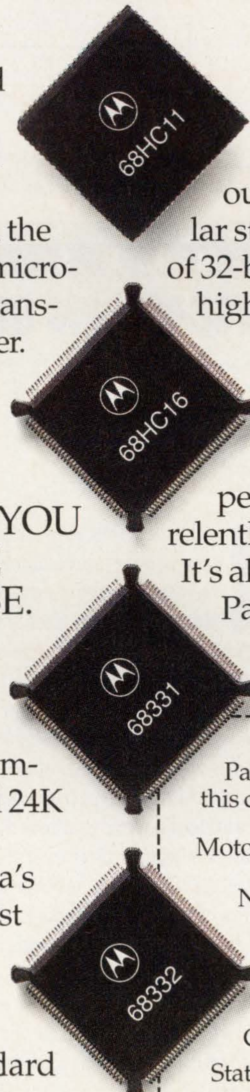

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QUICKLOOK

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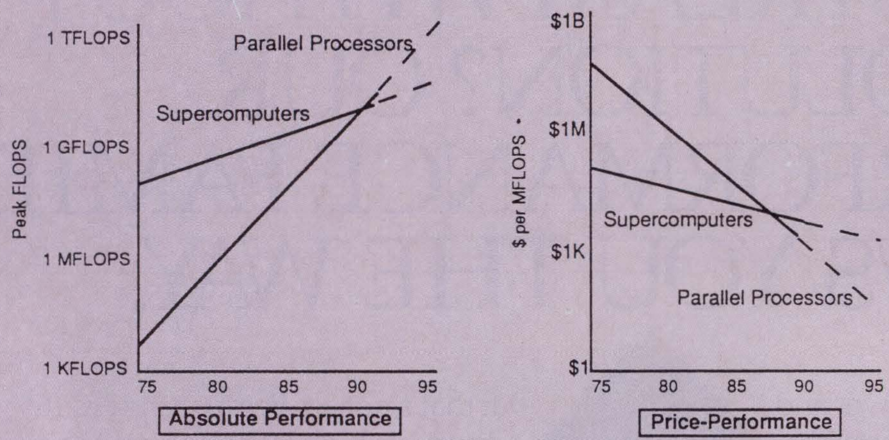


Source: Bolt Beranek and Newman Inc.

Parallel systems are outstripping traditional supercomputers in performance and the price-performance ratio. RISC microprocessors supply critical floating-point punch. The performance gap will keep widening as parallel microprocessor-based systems become faster and cheaper, according to Bolt Beranek and Newman Inc. The Cambridge, Mass., computer maker showed this slide at the recent Supercomputing '90 conference in New York.

1-MINUTE OPINIONS

What do you think about the education that young engineers receive these days?

Humanities play a major role in any curriculum, not only in engineering. Many students from all majors seem to have difficulty understanding the need to take these courses because they don't appear to be relevant. In addition, schools place little emphasis on the need to learn about ethics, morals, values, and the human condition in general.

And no wonder. Adolescents have little to emulate in a society that is fraught with scandals, lawsuits, and the worship of greed. Could this explain why our colleges graduate more lawyers than any other profession? It is indeed difficult in today's litigious society to justify learning the humanities.

Presumably one earns a degree in order to enter the business world. Why, then, don't we produce engineers who possess business sense? I don't mean marketing strategies on how to screw your competitors. I mean integrity and plain-dealing.

The curricula should be adjusted to accommodate these courses and if that means a five-year degree, so be it. Ultimately, though, we who hire these engineers must show the need and set the example. **Robert Schroeder**, *Trenton, N. J.*

What's your opinion on the education of today's young engineers? Fax your opinion to (201) 393-0637 or mail to Electronic Design, Reader Opinions, 611 Route 46 W, Hasbrouck Heights, NJ 07604.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458

Available tools, especially costly ones and those crucial to new-product development, need to be managed as scarce resources. Acquiring tools will be based on use and the asset's economic performance. It will be necessary to justify the true cost of the capital investment. The definition matrix, defined in the Sept. 27 column, and the new product development process (NPDP) matrix, described in the Oct. 11 column, set the stage for making the financial justification a simple mathematical exercise. Payback period, average return on investment, or discounted cash flow can be computed for each tool choice being considered as the tool's effect on project time to market is assessed.

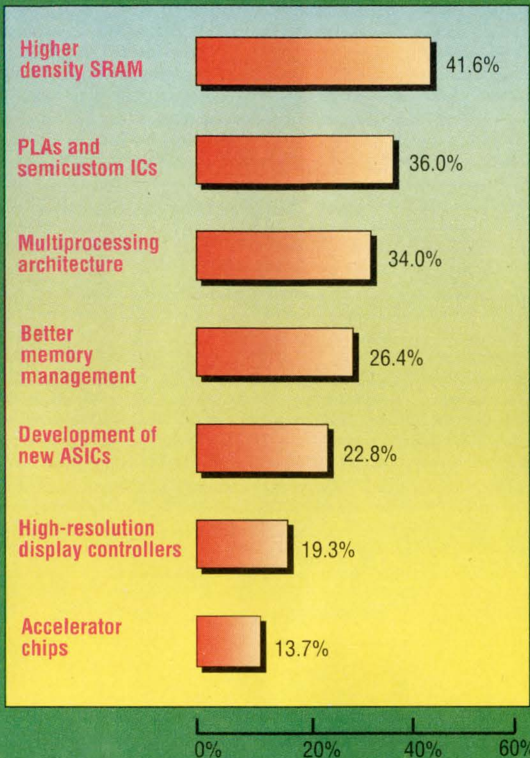
Working through the matrices makes time to market a very visible parameter. Additionally, the matrices ensure that tool decisions are evaluated from a cross-functional perspective to gain insight on their overall impact. Generally speaking, tools that shave quarters and months off the time to develop a new product are easy to justify. Those that produce improvements of only a few weeks can also be found to have solid financial benefit.

Individuals who think particular design systems are in short supply can be asked to perform the financial justification based on the overall time to market impact. You'll want them to work with teammates in other functions to keep the evaluations impartial and balanced in perspective. A cross-functional time-to-market view makes it possible to accurately determine the returns a tool will produce. Obviously, speeding up a portion of the new product development process that is not on the critical path offers little benefit in the reduction of time to market. Critical path times need to be reduced first so they are no longer critical path elements. As reductions are made, other critical paths emerge that will call out for attention. The definition and NPDP matrices help segregate process zones where tools help reduce time to market from those where the tools won't have an effect.

The phenomenon described above, while coarsely visible in the definition phase, becomes very clear in the planning phase. Those tools that can be shown to affect the critical path and greatly reduce time to market can be acquired during the definition phase. Where possible, justification of tools whose impact is not immediately obvious should wait until a detailed project network emerges and the planning phase is nearly complete.

MICROPROCESSOR SURVEY

TO DESIGN WITH 32-BIT MICROPROCESSORS, WHICH PRODUCTS OR TECHNOLOGIES WILL YOU NEED?



Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.
A. WHITE

DID YOU KNOW?

. . . that while the New England region is slumping, the fastest growing region for technology in the U. S. is the Pacific Northwest. Last year's net employment gain was 12.6%. The 114 companies in Oregon reported 12.4% growth. Also reporting growth: California, Minnesota, Pennsylvania, and Texas.

CorpTech Focus

. . . that software engineers in Silicon Valley with four to five years of experience earn $44,900 annually on average. That's 13% more than the national average. Salaries remain high because of a stable market and steady demand for experienced software engineers.

Source Services Corp.

. . . that foreign market share for semiconductors in Japan is now about 13.3%, up from 8.5% when the 1986 U.S.-Japan Semiconductor Trade Agreement was signed. U. S. sales will add about $137 million in new R&D, $130 million in capital investment, $80 million in tax revenue, and nearly 5,500 in semiconductor jobs. Still, Japan's full compliance with the agreement would double the amount of revenue and jobs. The agreement is set to expire in July 1991.

Semiconductor Industry Association

TIPS ON INVESTING

As we celebrate the holidays and welcome in 1991, it's customary to cast a look back over the past 12 months. During 1990, events in the Middle East and in financial markets grabbed the spotlight. And with these events in mind, it's a better idea than ever to take a closer look at various types of stocks and what engineering investors should know about them.

Some of today's blue chips are mature, but still growing, companies. Other companies, such as those in the steel and auto industries, can be expected to grow no faster than the overall economy. (Some older "smokestack" industrial companies are no longer considered blue chips; many have fallen on hard times and their credit ratings have been downgraded.) Growth stocks are of three distinct types:

- New issues from brand new companies that have recently gone public are often in high-tech areas, such as biotechnology or communications. These companies have little or no financial track record. Investing in them is considered risky.
- Emerging growth companies are a few years old, with sales in the range of $25 million to $100 million. Typically, these companies have high rates of growth in sales and earnings per share, pay low or no dividends, and have a fairly heavy debt load.
- Maturing growth companies are large companies that are growing faster than the market as a whole, although not as fast as when they were smaller. They may pay dividends, though rarely more than the Standard & Poor's average dividend. These companies still reinvest most of their earnings into the business.
- Income stocks comprise companies in established industries and may pay dividends above the Standard & Poor's average. Examples include gas and electric utilities, gas pipeline companies, and healthy money-center banks. Like all investors, engineers should distribute their stocks over several industries. They can achieve a good diversification with as few as seven stocks, provided each is in a different sector of the economy. Industry classifications may vary. But generally they are capital goods and technology, consumer cyclicals (for example, autos and retailing), consumer staples and health care, divesified companies (conglomerates), financial companies (banks, brokerage houses, insurance companies, and so on), and utilities.

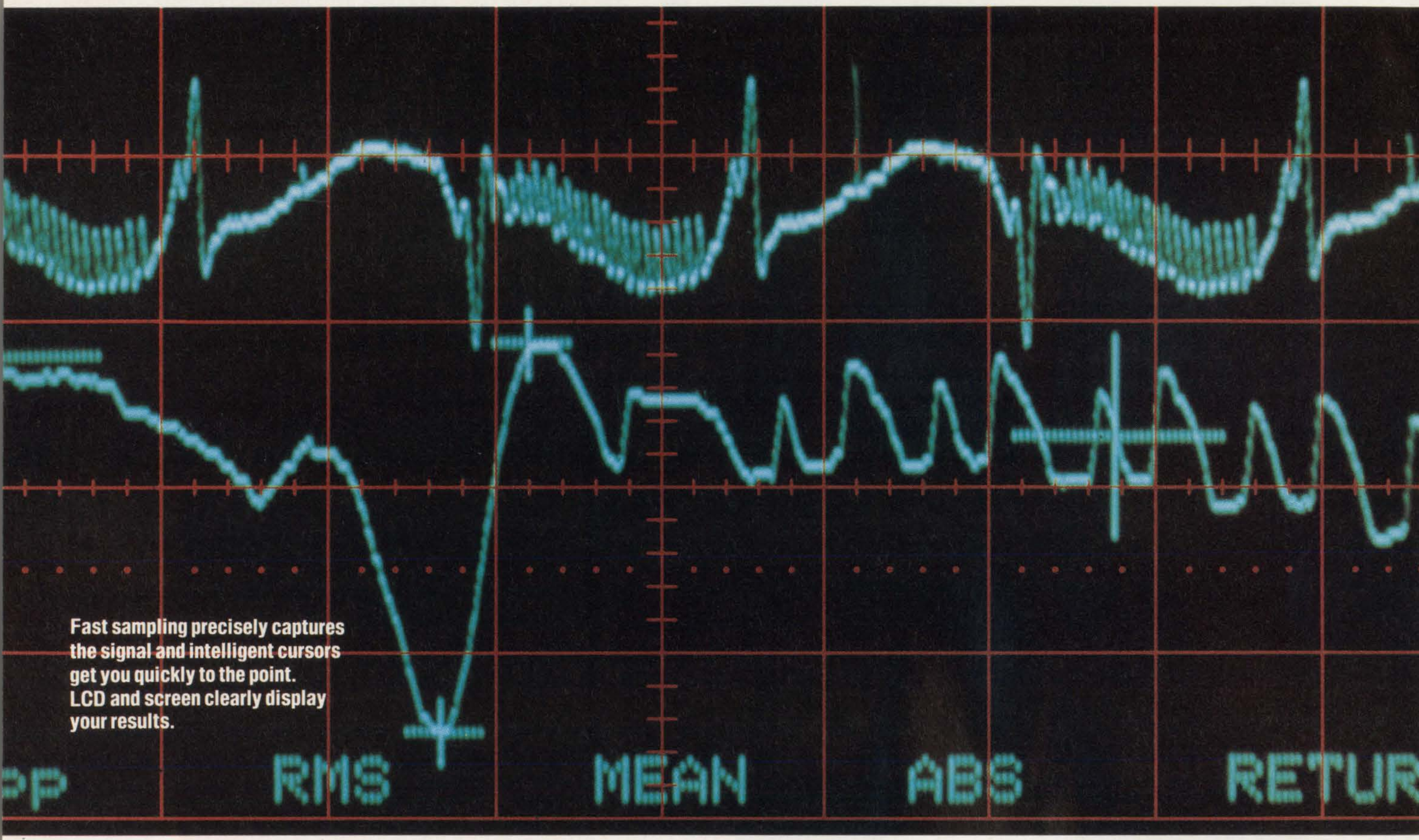
Obviously, every investment portfolio differs according to an engineer's needs, goals, and risk tolerance. Besides stocks, for instance, an engineer should have a liquid reserve for ready cash and a portion of funds in bonds for consistent income.

To illustrate, let's take the case of a young engineer with $25,000 to invest. The primary goal is to accumulate capital without taking much risk. The portfolio would be weighted toward common stocks, perhaps as follows: 5% ($1,250) liquid reserve of bank accounts or money-market funds; 30% ($7,500) five- or 10-year bonds, taxable or tax-free, depending on tax bracket; and 65% ($16,250) common stocks in these proportions—$10,000 in high-quality maturing growth companies, those in or near the blue-chip category (these are the portfolio's core holdings); $2,500 in utilities; $2,500 in food companies; $1,250 in financial companies.

With the volatile Middle East situation affecting all markets, the help of a financial consultant is crucial in making investment decisions. Although categories of stock and individual issues can vary, the result should be a balanced, diversified portfolio that can be fine-tuned as objectives change over the years.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, Shrewsbury, N. J. and a qualified pension coordinator. He invites questions and comments, which should be addressed to the news editor, Electronic Design.

FLUKE



Fast sampling precisely captures the signal and intelligent cursors get you quickly to the point. LCD and screen clearly display your results.

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When it comes to medium frequency DSOs, how much you see depends on how much you can capture, how well you can analyze it, and how easily you can do the job.

Digital Storage Oscilloscopes from Fluke see things a little differently than DSOs from HP or Tek for one simple reason.

They see more.

Thanks to the fastest real time sampling speeds available under $5,000, the new PM 3375 not only gives you full analog capabilities, it also lets you capture fast single shot events — with exceptional resolution.

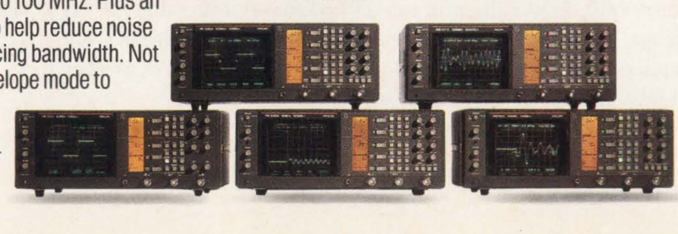
But DSOs from Fluke don't just show you more. They also tell you more, by giving you the analytical power you need to extract a wealth of extra information from your signals.

Twice the sampling speed. Twice as easy.

Take our new medium frequency PM 3375, for example. With real time sampling at 250 MS/s, the PM 3375 samples every waveform more than 2½ times faster than any HP or Tek scope in its price range. So now you can accurately capture more types of signals, more precisely. Even fast single-shot events to 25 MHz (@ 10 samples per period), with resolution to a full 4 ns.

You also get repetitive sampling to capture recurrent signals to 100 MHz. Plus an averaging mode to help reduce noise without also reducing bandwidth. Not to mention an envelope mode to monitor extremes of signal variation, such as tracking signal jitter or AM/FM modulation depth.

And like every DSO from Fluke, the PM 3375 is remarkably easy to operate. You can switch from digital to analog operation any time you want at the push of a button. AUTOSET lets you find your signal and fully set up your scope automatically. You can store up to 64 front panel setups in non-volatile memory. Even full remote is available.



Starting at just $2,350, Fluke DSOs stop at nothing to deliver superior performance.

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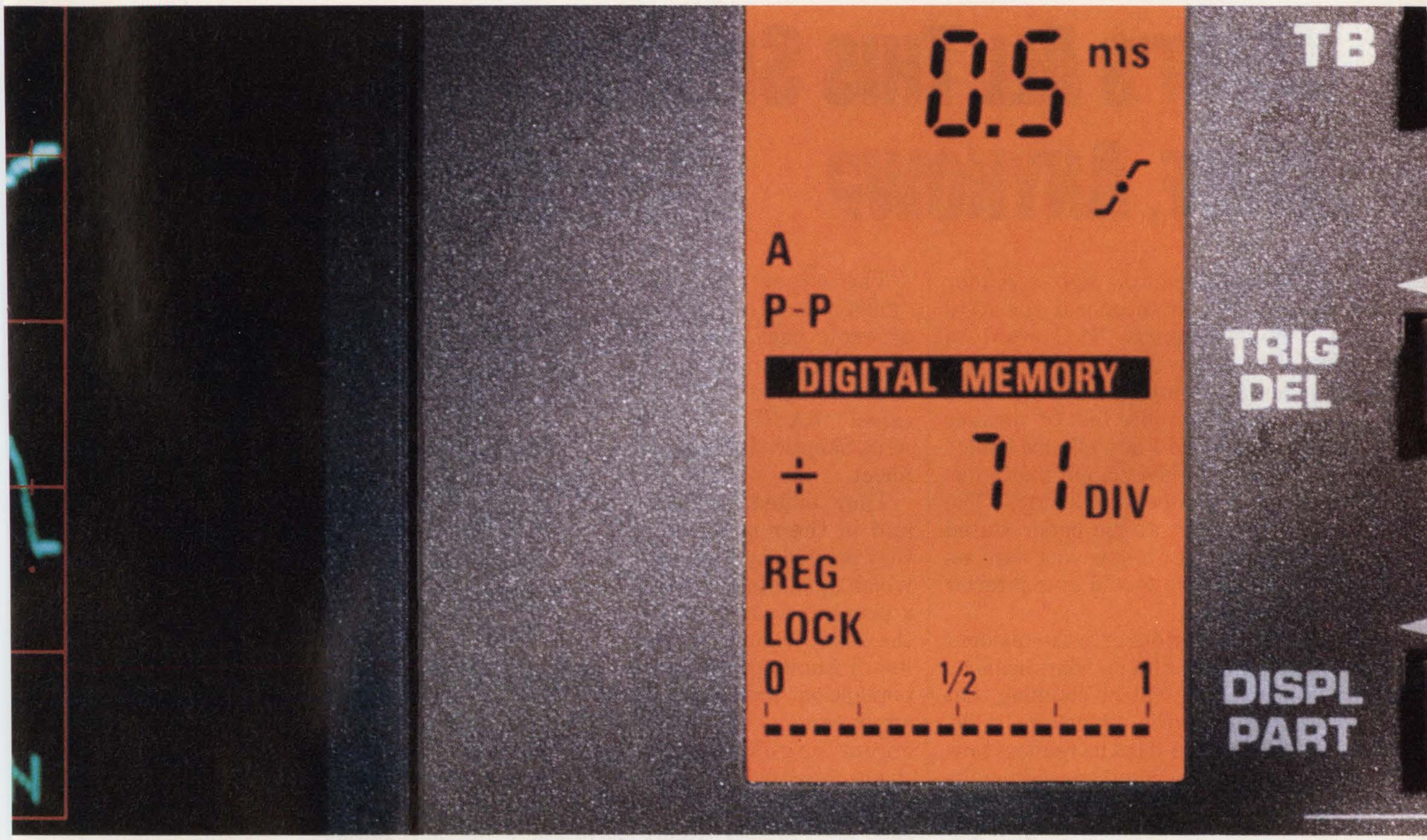
PHILIPS



ect HP® and Tek® DSOs, a little differently.

Better analysis. Better value.

Of course the real advantage of DSO technology isn't just seeing and capturing waveforms. It's analyzing waveforms.

Here, DSOs from Fluke really stand out. Smart cursors take you far beyond mere dV and dt measurements, to automatically calculate V_{pp}, V_{rms}, V_{mean}, Frequency, Period, Pulsewidth, Rise- and Fall-times and more.

Get the whole picture on video. Free.

With prices ranging from $2,350 to $5,390, medium frequency DSOs from Fluke offer superior specs for unparalleled performance and value. Compare all five, including our high frequency DSOs, to HP & TEK by sending for our full comparison chart. Or watch them in action in our free video titled "DSOs With a Difference: Chapter III." Just call **1-800-44-FLUKE ext. 77.**

Features	Fluke PM 3375	Tek® 2232	HP® 54501A
Analog + Digital	Yes	Yes	No
Analog Bandwidth	100 MHz	100 MHz	Not available
Max. Captured Freq.			
Single Shot Sig.*	25 MHz	10 MHz	1 MHz
Repetitive Sig.	100 MHz	100 MHz	100 MHz
Sampling Rate (real time)	250 MS/s	100 MS/s	10 MS/s
Calculated Measurements	Yes**	No	Yes
AUTOSET	Yes	Beamfinder Only	Yes
Setup Memory	64	None	4
Remote	Full	Data Only	Full

*at 10 samples per period   **with automatic adjustment for probe factor

John Fluke Mfg. Co., Inc. P.O. Box 9090, M/S 250C, Everett, WA 98206-9090. U.S. (206) 356-5400. Canada (416) 890-7600. Other countries: (206) 356-5500. Ad no. 0101-P3350. Tek® and HP® are registered trademarks of Tektronix, Inc., and Hewlett-Packard, Inc.

FLUKE

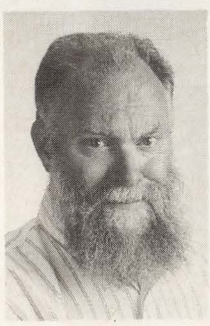
CIRCLE 96

PEASE PORRIDGE

What's All This Splicing Stuff, Anyhow?

Several months ago, a reader wrote in to one of the local newspapers, "If I want to move my speakers a few feet further from my amplifiers, can I splice in a few more feet of speaker cable, or should I buy all new cable? My brother-in-law claims that splicing would hamper the sound." The resident expert at the paper stated that the brother-in-law was wise, as the spliced wire would give inferior audio results.

I promptly wrote in to the resident expert, asking him on what basis he could say this. Was he claiming that *he* could *hear* the difference? I demanded that he show us readers how the spliced wire could possibly make any difference. I challenged him to listen to any music, under any audio conditions, and I would swap in various pieces of speaker wire (enclosed in boxes, on a double-blind basis) that had 0 or 1 or 2 or 6 or 12 splices. How, short of clairvoyance, could he tell which wire had the splices, using ordinary audio-frequency signals? Of course, if you used an impedance analyzer with a bandwidth of several gigahertz, you could "see" some of the splices. But, for good high-fidelity audio, there's no way you could discern this, especially as a splice may make the wire's impedance lower or higher or unchanged.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

The expert, with his "golden ears" and all, never wrote back. So, I sent my criticism to one of the local skeptic's groups called "BASIS," the Bay Area Skeptics Information Sheet.

They edited it lightly, and in their newsletter, they printed my complaint, which amounted to this: If a person claims to talk to the dead, or summon spirits, or show extrasensory perception, then we must apply some skepticism so as not to encourage gullible persons to invest their money in these hoaxes.

How, short of clairvoyance, could he tell which wire had the splices using ordinary audio-frequency signals?

But if a person who is endorsed as the "high-fidelity expert" says that you can hear the difference between spliced and unspliced wires, then we, as technical people, have an obligation to express our doubts and our skepticism. Why should a hi-fi salesman be able to sell a bright-eyed yuppie a $50 hank of speaker wire, (or $100 or $200 or $400 or more, which is where the really high-end speaker wire is priced these days—believe it or not) just because an "expert" says it's *better* to buy new wires rather than splice on a few extra feet? Obviously, ethics in technical electronics and science is involved here.

Many hi-fi experts, with their "golden ears," claim that they can hear differences in sophisticated speakers, expensive amplifiers, or just fancy wires, that I can't possibly discern or detect. It might take many thousands of dollars to just buy the equipment and duplicate the experiment. And, their ears might be correct—much more discerning than mine, more than I could imagine. But, when the "expert" talks about wire and splices, then I find myself compelled to comment and raise doubts. There *are* some experiments that even I can propose and that I could conduct, that would be decisive, if the "expert" did not duck the challenge.

Now, there are many persons who have *golden ears* and will claim that they can easily distinguish between *good*, *better*, and *best-quality* speaker cables. However, when these persons are invited to a double-blind test, they usually have a strong tendancy to demur. Some people like to call this the *the shyness factor*. Other people liken this to the tendency of cockroaches to scuttle into a dark corner when the lights are turned on.

I was only slightly concerned about how to conduct the test, because to do a fair test, you might have to change back and forth from, say, speaker wire #1 to speaker wire #2 or #6. If you do that with screwdrivers and pliers, it might take a long time to make the changes; a critical listener's judgment might be affected by long delays, and it would be unfair to ask for good judgment under those conditions. But if I proposed to use a number of selector switches, the man with the "golden ears" might argue that the switch's impedance would be worse than the splices, so a switch would be suspect! No, you can't use switches when you want to do an A-B comparison!

But in the last few weeks, the hi-fi review column of this "expert" was discussing how he compares different speakers: He said to change from one set of speakers to another, he uses switches! I just hope the switches don't cloud his judgment, as if they were (God forbid) *splices*.

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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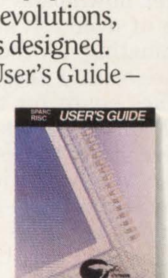

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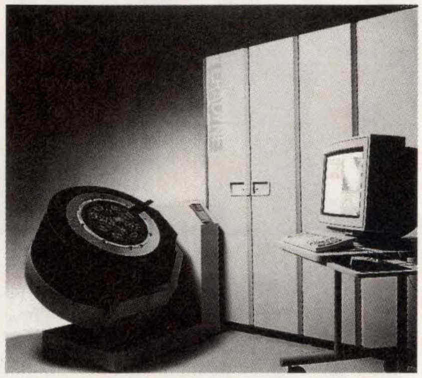
ECL, CMOS COMBINATION MAKES TESTER ECONOMICAL

A modular architecture and an unusual combination of ECL and CMOS technology help make the J971 VLSI test system very flexible and economical. Channel counts from 64 to 512 are available in 32-channel increments. The maximum operating frequency is 200 MHz and maximum data rate is 400 Mbaud. The system aims at the full range of device testing, from engineering and silicon debugging through characterization and production testing.

A J971 system consists of a number of Integrated System Cells, which are selected by the user to deliver the specific performance desired. Users can order plug-in performance cells as needs change. The system-level combination of ECL and CMOS technologies, which Teradyne calls E/MOS, optimizes performance and economy. The design includes an innovative timing and formatting system that lets 90% of the circuitry use low-cost CMOS devices. The final output stage, where maximum performance is needed, employs ECL technology.

The J971 comes with the IG900+, a follow-on to the IG900 interactive graphics software. Built on a database foundation, the IG900+ separates the process of defining device test parameters and test data from the creation of program code. With IG900+ tools, engineers can describe test data (voltages, timing, vectors, and so on) either in ASCII format or as tables of values and waveforms.



The J971 system cells can be configured into more than 1000 versions to suit specific applications. Prices range from $400,000 to $4 million, with deliveries scheduled to start this month.

***Teradyne Inc.**, Semiconductor Test Div., 30801 Agoura Hills Rd., Agoura Hills, CA 91301; (818) 991-2900.* CIRCLE 420

■ *JOHN NOVELLINO*

EMULATOR SUPPORTS 80386 SYSTEMS TO 33 MHZ

The CodeStalker 386 offers full-speed emulation at clock rates to 33 MHz for 80386-based systems. Because the emulator inserts no wait states, it works nonintrusively, even in systems with cache memory. A fiber-optic communications link supplied with the CodeStalker downloads code at a sustained rate of over 250 kbytes/s, essentially eliminating download delays. The unit comes with a short-slot fiber-optic interface board for use in PCs. Overlay RAM of 448 kbytes can be mapped anywhere in the processor's 32-bit address space to a resolution of 4 kbytes. The CodeStalker's 4-kword-deep trace memory captures machine cycles at full speed. CodeStalker 386, which includes Softaid's source-level debugger that works with virtually any C compiler, costs $9995.

Softaid Inc., 8930 Rte. 108, Columbia, MD 21045-2101; (800) 433-8812 or (301) 596-1852. CIRCLE 421

ANALYZER/EMULATOR EVALUATES SCSI BUSES

The OZ-201 SCSI bus analyzer/emulator can simultaneously or independently act as a bus analyzer and as a bus initiator or target device. As an analyzer, the instrument captures 32k-traces of bus activity in either synchronous or asynchronous modes to 20 MHz. Each 56-bit-wide trace saves data, control-line status, event flags, and a 50-ns-resolution time stamp. The OZ-201 simulates SCSI devices in both single or multi-initiator or target environments, using the NCR53C80 protocol. Emulation procedures are written in SCOL, Biomation's SCSI Control-Oriented Language. SCOL offers 72 predefined emulation sequences so that custom programming is minimized. The unit is controlled by a user-supplied PC/AT computer. The OZ-201 costs $5995, and is available from stock.

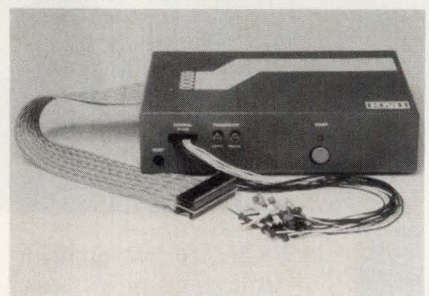
Biomation Corp., 19050 Pruneridge Ave., Cupertino, CA 95014; (800) 538-9320 or (408) 988-6800. CIRCLE 422

LOGIC ANALYZER ADDS 80960 DISASSEMBLY

The 80960CA microprocessor support package offers mechanical connections and full software disassembly for the Intel i960 on the ML4400 logic analyzer. The package's Target Interface Adapter plugs into the 80960's PGA socket on the board under test. The processor then plugs into the Adaptor. Disassembly is implemented by the proprietary User-Defined Disassembler, which supports all instructions. The display shows each data cycle below the instruction with which it's associated. Also available for the ML4400 is an optional Expanded-Memory Capture Module. The card supplies 65,000 storage locations when run at 50 MHz synchronously on 40 channels. Four cards ganged together provide 160-channel operation. The i960 package costs $1995 and the memory card sells for $3995. Both are available immediately.

Arium Corp., 1931 Wright Circle, Anaheim, CA 92806-6052; (714) 978-9531. CIRCLE 423

REAL-TIME EMULATION FOR THE 68HC001



An adapter kit for the HMI-200-68000 offers 8- and 16-bit support for the Motorola 68HC001 microprocessor. The instrument provides real-time emulation, four complex break-and-trigger points, two 4k-by-72-bit trace buffers (including 16 external trace bits), and 32-bit time tagging. Emulation memory of 256 kbytes is standard, and 1 Mbyte is optional. Other software that can be added includes HMI's SourceGate, a windowed, high-level-language debugger that works with C, Pascal, and PL/M compilers from more than a dozen manufacturers. Also available is a performance analyzer. The 68HC001 adapter costs $950; the basic emulator sells for $7500. SourceGate for the IBM PC family is $1500, and the performance analyzer costs $2495.

Huntsville Microsystems Inc., 4040 S. Memorial Pkwy., Huntsville, AL 35802; (205) 881-6005. CIRCLE 424

OCTAL LOW-SIDE IC SWITCH DRIVES RELAYS

Designed to control up to 8 lamps, relays, or solenoids in automotive applications, the SGS-Thomson L 9822 octal low-side switch could be just as useful in data-processing equipment, office machines, and appliances. Copiers, for instance, are a natural. This power IC contains eight low-side DMOSFET switches, each rated for 750 mA continuously but current limited at 1.2 A. Each switch's output is protected by a Zener clamp set at 34 V. Any or all of the switches can be turned on or off by a host processor through a 4-wire serial bus employing the Serial Peripheral Interface protocol. The voltage level at each switch's output is returned to the host via the same bus. Output saturation voltages are monitored by comparators, and if they exceed 1.5 V for an ON switch, the switch is turned off and the host is notified. The comparators also tell the host, via the bus, if a switch in the OFF state is connected to an open circuit. The L 9822 comes in a 15-lead power IC package, meets its specifications from –40 to 125°C, and goes for just $3.50 each in 100s.

SGS-Thomson Microelectronics, 1000 E. Bell Rd., Phoenix, AZ 85022; Serban Coss, (313) 462-4030. **CIRCLE 425**

DMOSFET IN TO-220 OFFERS 10-MΩ R_{DS}ON

Offering a maximum on-resistance (R_{DS}ON of just 10 mΩ, Siliconix's 30-V, 60-A (continuous) SMP60N03-10L provides the lowest on-resistance of any power MOSFET in a TO-220 package. Designed for switching power supplies and power management in laptop computers and their peripherals, it offers more efficient and cooler operation than available FETs. Fans, and potentially even heat sinks, can be eliminated, cutting both space and cost. The FET also lends itself to controlling motors in battery-powered hand tools. Moreover, it may gain ultimate fame as the long-awaited switch that will make synchronous rectification feasible—replacing Schottkys in low-voltage switching power supplies. At 10 A, its forward drop is just 0.1 V—which is less than that of many relays or any Schottky.

Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, CA 95054; (800) 554-5565, ext. 1800. **CIRCLE 426**

DMOSFETS OPEN 28-V, 30-A LINE IN UNDER 10 μS

When you think of circuit breakers, you typically envision large electromechanical devices. However, the SSP-21110 from ILC Data Devices will change that notion. This true I^2T breaker employs power MOSFET switches (the time-to-break for an I^2T breaker is a function of the square of the current passing through it). Rated for 30 A at 28 V, the SSP-21110 comes in a hermetic metal package just 2.3 by 1.3 by 0.3 in. Nominal trip time at 30 A when triggered by an external logic pulse runs 25 μs. The breaker won't trip at overloads to 110% of rating. Trip time is 100 seconds for overloads between 110% and 145% of rating, which drops exponentially to under 10 μs for overloads of 1200%. Aimed initially at electrical load-management systems in aircraft, it doesn't suffer from the arcing and contact bounce of conventional devices, and it reports its status back to a host. In 100s, it goes for $255 each.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; (516) 567-5600 ext. 381. **CIRCLE 427**

SWITCHER CHANGES –48 V TO 5 V AT 250 MA

Aimed at products that attach to, and are powered from the telephone line, Maxim's MAX650 switching supply converts –48 V to +5 V at 250 mA. Housed in a 14-pin DIP, it needs only a half-dozen resistors, several capacitors, a Schottky diode, and an inductor-transformer to do the job. This complete IC switcher operates at a nominal 20 kHz and employs a pulse-skipping flyback topology to simplify feedback-loop stabilization, instead of the more common pulse-width-modulated topology. An on-chip pnp-transistor switch is rated at 140 V. Features include adjustable soft start, a shutdown pin, current limiting, and a low-supply voltage detector with adjustable hysteresis. A and B versions offer ±5 and ±10% tolerance on the output voltage, respectively. The B version can be set to trip at any negative voltage and turn off the supply. In quantities of 1000, pricing starts at $3.16 each.

Maxim Integrated Products Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; Doug Vargha (408) 737-7600. **CIRCLE 428**

3 R-TO-D CONVERTERS COME IN 40-PIN TDIPS

For the first time, three 16-bit or 1.3-arc-minute-accurate resolver-to-digital converters are available in one 40-pin triple-width hybrid DIP. From Natel, the HRD1346 contains type-II servo-loop tracking converters with zero velocity error. Designed for military avionics systems, the triple converter is also useful in robotic systems, simulators, and computer-controlled machine tools. Power drain is just 30 mA from a 5-V rail. Pricing for the converter starts at $1345 each.

Natel Engineering Co. Inc., 4550 Runway St., Simi Valley, CA 99063; Tom Guerriere, (805) 581-3950. **CIRCLE 429**

DELAY LINE SOLVES VIDEO TIMING PROBLEMS

A programmable digital delay line IC solves a wide range of video-speed timing problems. Because the IMSA113 can delay a 9-bit word (one byte plus a flag) from 6 to 1318 clock cycles at 20 MHz, it's an excellent device for video-speed circuit designers confronted with pipelining or general timing problems. Delay times are set by a binary data word applied to 11 input pins on the IC, a method that's both simple and flexible. Moreover, several IMSA113s may be cascaded or paralleled to increase the delay time or word width. The single-chip solution is an economical alternative to standard high-speed FIFOs in such applications as image processing, ghost and echo cancellation, radar-beam forming, and digital TV. It may also be used in many lower-bandwidth applications, like audio processing. Housed in a 44-pin PLCC, the IMSA113 is a high-speed static CMOS IC with TTL-compatible inputs. The chip consumes less than 250 mW from a single 5-V supply. Samples are available.

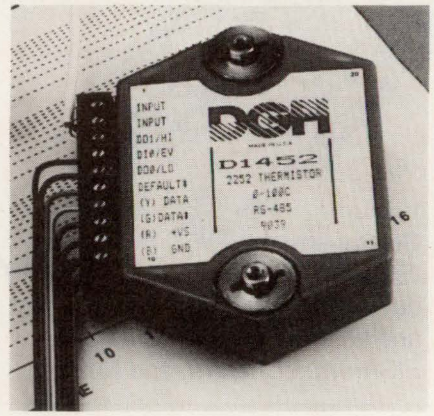
SGS-Thomson Microelectronics, I-20014 Agrate Brianza, Italy; phone (0039) 39-6555-597. **CIRCLE 430**

AMPLIFIER BUILDS SIMPLE, PRECISE PGA

The INA120 instrumentation amplifier permits building an accurate programmable-gain amplifier (PGA) just by adding a multiplexer. The IC handles signals from thermocouples, strain gages, and RTDs. Its thin-film resistors pin-strap gain to tight accuracies of within 0.1%, 0.2%, 0.5%, and 1%, at gains of 1, 10, 100, and 1000, respectively (AP grade). At similar gains, gain temperature coefficient (TC) runs 20, 40, 60, and 100 ppm/°C, and gain nonlinearity is within 0.01%, 0.01%, 0.02%, and 0.1% of full scale. Offset voltage and its TC at a gain of 1000 run 200 μV and 40 μV/°C, respectively (AP model). Specifications for two higher grades run 2 to 10 times better. All grades come in an 18-pin DIP. In 100s, prices are $5.90 to $14.80 each.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; John Conlon, (800) 548-6132 or call the bulletin board at (602) 741-3978, (300/1200/2400 8,N,1) **CIRCLE 431**

SMALL MODULE TIES THERMISTOR TO HOST



Buried in the D1452 small sensor-to-host interface screw-down module lie all of the electronic circuits needed to tie a 2252-Ω thermistor to a host computer. The module includes signal conditioning circuitry needed to link a sensor to an on-board 12-bit ADC, a microcontroller, and an RS-232 or RS-485 interface port. Up to 124 of the 7.5-in^3 packages can be strung on a single twisted-pair cable. Sensor types from thermocouples and strain gages to RTDs and silicon pressure sensors can be mixed. The D1451 handles temperatures over a range of 0 to 100°C. Its resolution is within 0.01°C and accuracy within ±0.1°C. Its data rate is 8 conversions/s. Price per module is $250.

DGH Corp., P.O. Box **[need number],** ***Manchester, NH 03108; Bob Glines, (603) 622-0487.*** **CIRCLE 432**

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Processors

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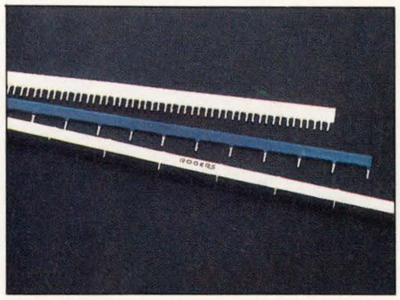

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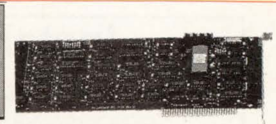

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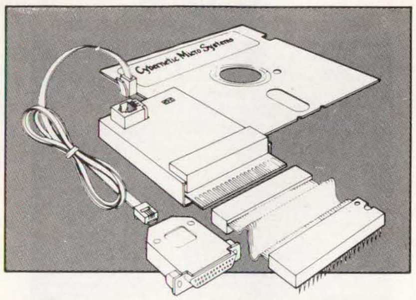

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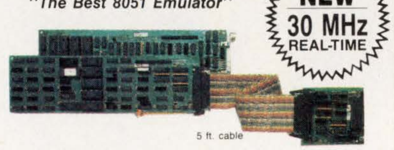

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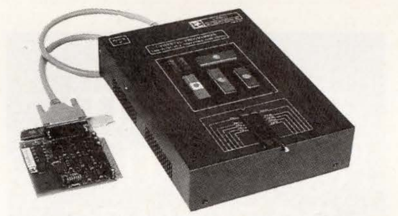

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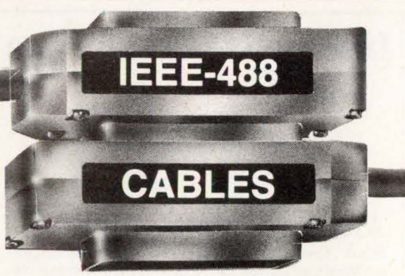

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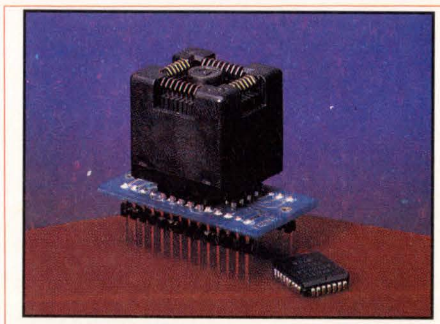

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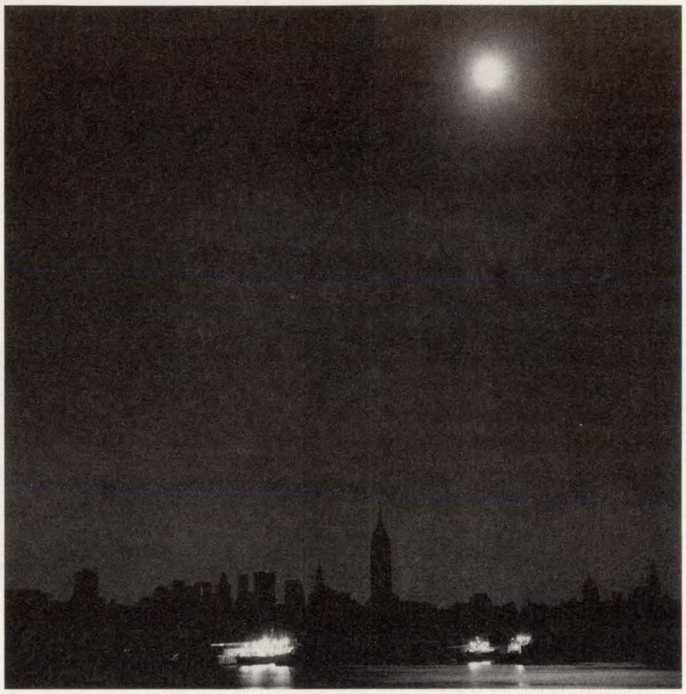

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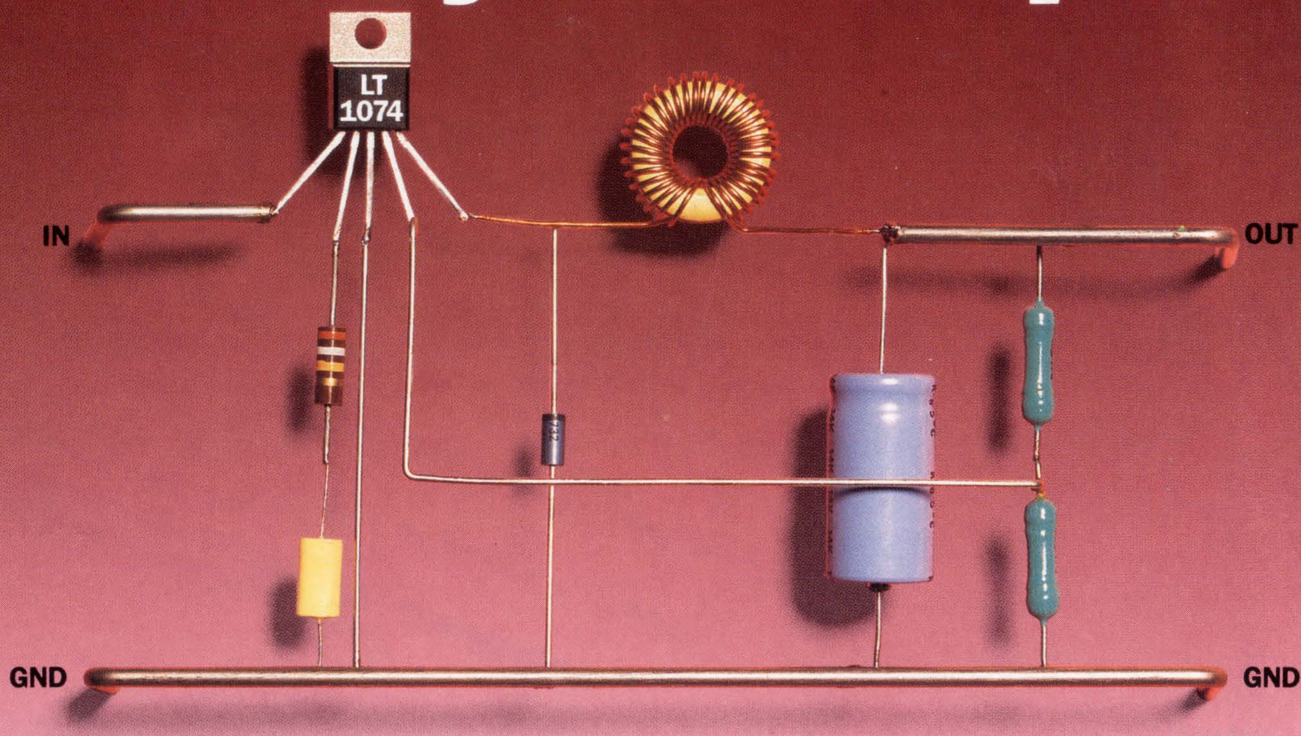

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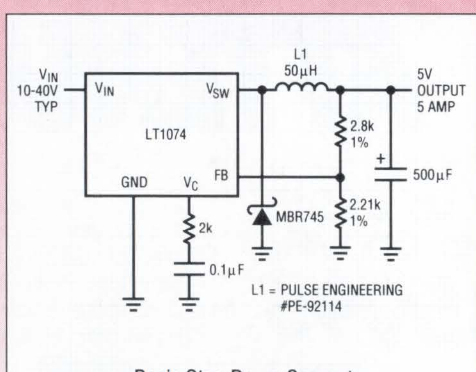

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