


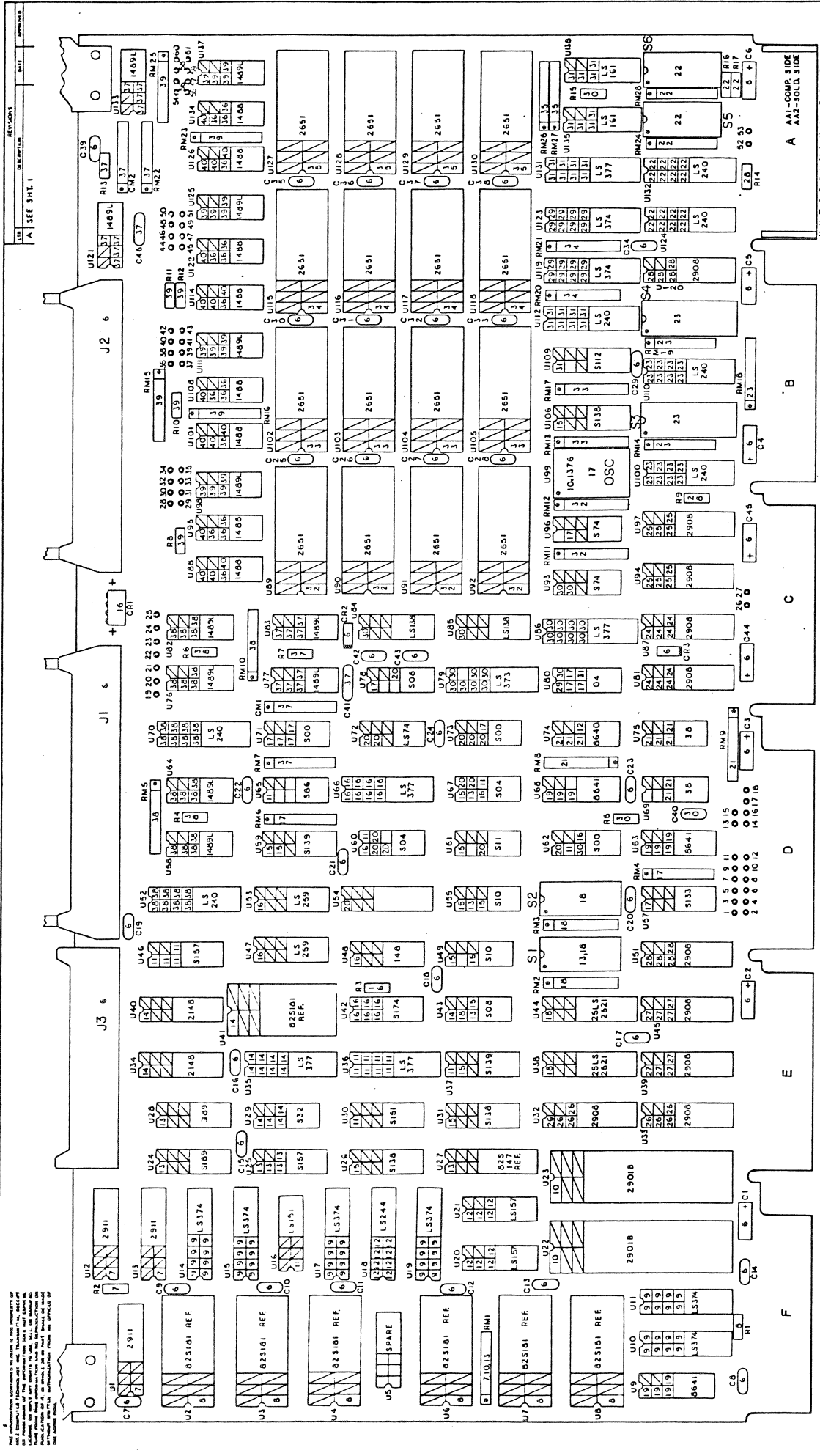
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REVISIONS		
LTR	DESCRIPTION	DATE
A	PROD. REL. PER E.O. 298	4-16-81

APPROVED	<i>[Signature]</i>
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REF. ONLY

 ABLE COMPUTER TECHNOLOGY	
SCHEM-16 CH ASYNC DMA COM CNTRLR	
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ± ± ±	SCALE SIZE DRAWING NO.
APPROVALS DRAWN CHECKED DATE	APPROVALS DATE 25-2-81 4-16-81 4-16-81
DO NOT SCALE DRAWING	SHEET 1 OF 40



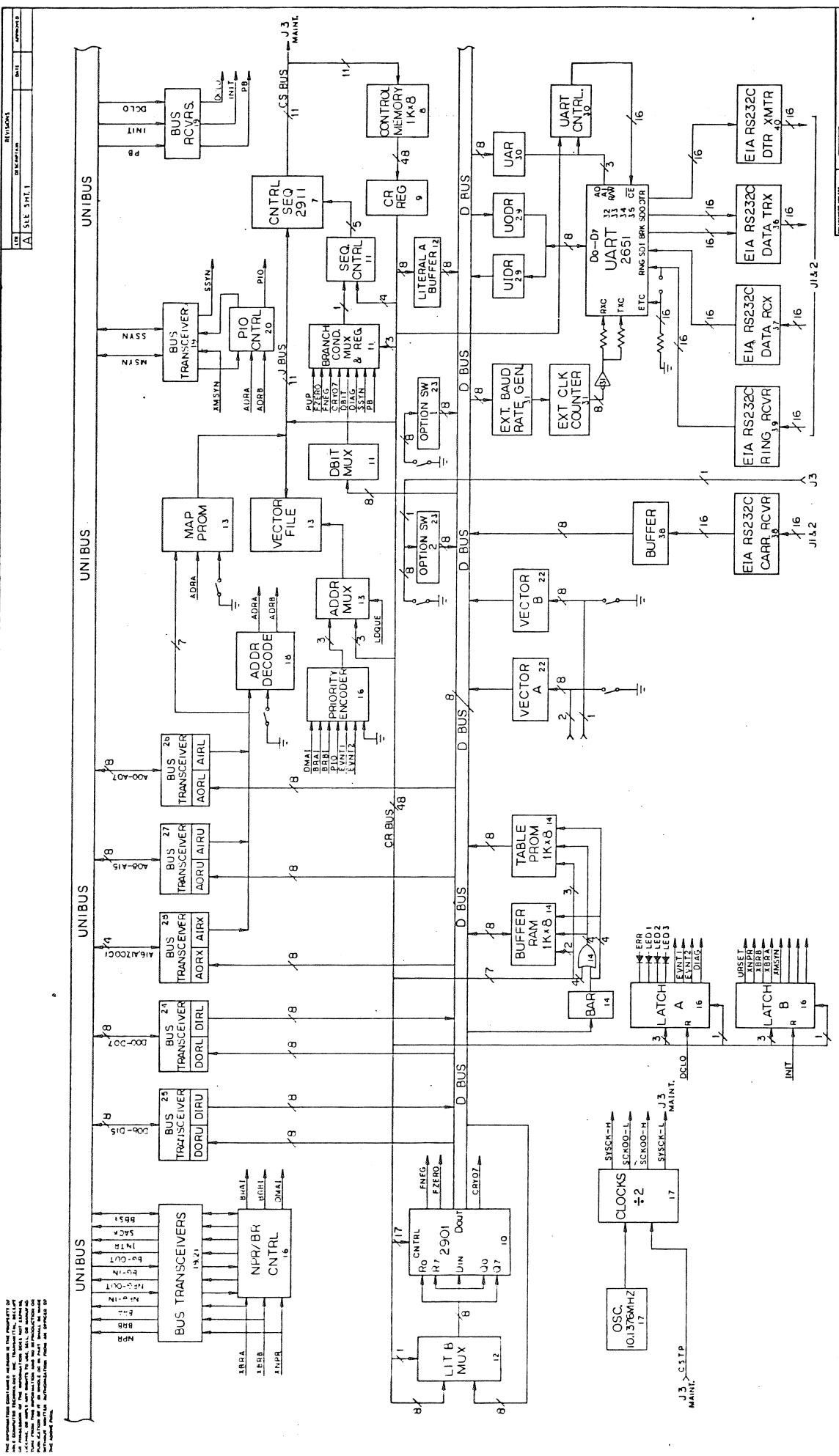
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 DIMENSIONS OF THIS DRAWING ARE TO BE TAKEN FROM THE CENTER OF THE COMPONENT UNLESS OTHERWISE SPECIFIED.

REFERENCE DESIGNATION CHART

TYPE	LAST USED	NOT USED
IC	U139	U5, 30, 35, 07, 03, 04, 09
RES. MOD.	RM26	
CAP. MOD.	CM2	
DIODE	CR3	
CAPACITOR	C46	
RESISTOR	R17	

ACT All Circuitry To Be Done
 SCHEM-16 CH ASYNC.
 DMA COM CNTLRL
 D 10103003

SEE SMT. 1
 A 11-13-77
 RM25
 RM22
 RM23
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 RM100



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2901 DATA PATH PHRASE				DBUS PHRASE				ORDER PHRASE				SEQUENCE CONTROL PHRASE						
D	+	S	C	A		B		D/S		LO		T		S		LIT B / RESUME DATA		
				FILE	FILE	D DEST.	D SRCE.	ORDER	ADDR.	D	T/F	TEST	SEQ.	BRANCH	ADDRESS			
2901 CONTROL				C		R		Y		D		D		D		AD		
DEST.	ALU	SOURCE	R	S	FILE	FILE	D	DEST.	D	SRCE.	ORDER	ADDR.	D	T/F	TEST		SEQ.	BRANCH
Q	R + S	A	Q	Ø	Ø	Ø	Ø	DBUS	LITA	NULL	NULL	RO-DATA UNSET	Ø	-GOTO	LITB	Ø	Ø	Ø
NOD	S - R	A	B	1	1	1	1	BRR	TPRM	REL_PIO	REL_PIO	WRT-DATA LED1 XNPR	1	-ALUZ	RETURN	1	1	1
(BYPASS)	R - S	Ø	Q	2	2	2	2	DORL	MEM	SET_INTR	SET_INTR	RO-STAT LED2 XBRB		-ALUNEG	GOTO	2	2	2
B	R OR S	Ø	B	3	3	3	3	DORU	MVR	RESUME	RESUME	N/A LED3 XBRB		-CRY	CALL	3	3	3
BQ RIGHT	R AND S	Ø	A	4	4	4	MAR	ALU	ALU	NOT USED	NOT USED	RO-MODE NOT USED XMSIN		-DBIT	MAP_PIO	4	4	4
B RIGHT	R AND S	D	A	5	5	5	UODR	UIDR	UIDR	UART	UART	WRT-MODE NOT USED		-NO-DIAG	N/A	5	5	5
BQ LEFT	R XOR S	D	Q	6	6	6	UAR	DIRL	DIRL	A LATCH	A LATCH	RO-CMD NOT USED		-SSYN	VECTOR	6	6	6
B LEFT	R XNOR S	D	Ø	7	7	7	MEM	DIRU	DIRU	B LATCH	B LATCH	WRT-CMD NOT USED		-PB	N/A	7	7	7
				8	8	8	AORL	AORL	N/A	N/A	N/A			GOTO		8	8	8
				9	9	9	AORU	AORU	N/A	N/A	N/A			ALUZ		9	9	9
A				10	10	10	AORX	AORX	N/A	N/A	N/A			ALUNEG		A	A	A
B				11	11	11	NOT USED	NOT USED	N/A	N/A	N/A			CRY		B	B	B
C				12	12	12	N/A	N/A	N/A	N/A	N/A			DBIT		C	C	C
D				13	13	13	N/A	N/A	N/A	N/A	N/A			NO-DIAG		D	D	D
E				14	14	14	N/A	N/A	N/A	N/A	N/A			SSYN		E	E	E
F				15	15	15	N/A	N/A	N/A	N/A	N/A			PB		F	F	F

PRIORITY	EVENTS
7	PIO
6	DMAI
5	BRAL
4	BRBI
3	NOT USED
2	EVNT2
1	EVNT1
0	SCAN

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 and for the correct use of the equipment.

SHT	I	A	2	SHT
		A	+5V	6
		B		
		C	GND	6
		D		
		E		
		F		
		H		
		J		
		K		
		L		
		M		
28	BUS-A21-L	N		
28	BUS-A20-L	P		
		R		
6	GND	S		
		T		
		U		
		V		

SHT	I	C	2	SHT
21	BUS-NPG-IN-H	A	+5V	6
21	BUS-NPGO-H	B	-15V	6
		C	GND	6
		D	BUS-D15-L	25
		E	BUS-D14-L	25
		F	BUS-D13-L	25
25	BUS-D11-L	H	BUS-D12-L	25
		J	BUS-D10-L	25
		K	BUS-D09-L	25
		L	BUS-D08-L	25
		M	BUS-D07-L	24
19	BUS-DCLO-L	N	BUS-D04-L	24
		P	BUS-D05-L	24
		R	BUS-D01-L	24
19	BUS-PB-L	S	BUS-D00-L	24
6	GND	T	BUS-D03-L	24
6	+15V	U	BUS-D02-L	24
		V	BUS-D06-L	24

SHT	I	E	2	SHT
		A	+5V	6
		B		
27	BUS-A12-L	C	GND	6
28	BUS-A17-L	D	BUS-A15-L	27
19	BUS-MSYN-L	E	BUS-A16-L	28
26	BUS-A02-L	F	BUS-C1-L	28
26	BUS-A01-L	H	BUS-A00-L	26
19	BUS-SSYN-L	J	BUS-CO-L	28
27	BUS-A14-L	K	BUS-A13-L	27
27	BUS-A11-L	L		
		M		
		N	BUS-A08-L	27
27	BUS-A10-L	P	BUS-A07-L	26
27	BUS-A09-L	R		
		S		
6	GND	T		
26	BUS-A06-L	U	BUS-A04-L	26
26	BUS-A05-L	V	BUS-A03-L	26

SHT	I	B	2	SHT
		A	+5V	6
		B		
		C	GND	6
		D		
28	BUS-A19-L	E	BUS-A18-L	28
		F		
		H		
		J		
		K		
		L		
		M		
		N		
		P		
		R		
		S		
6	GND	T		
		U		
		V		

SHT	I	D	2	SHT
		A	+5V	6
		B		
		C	GND	6
		D	BUS-BR7-L	21
		E	BUS-BR6-L	21
		F	BUS-BR5-L	21
		H	BUS-BR4-L	21
		J		
		K	BUS-BG7-IN-H	21
19	BUS-INIT-L	L	BUS-BG7-OUT-H	21
		M	BUS-BG6-IN-H	21
		N	BUS-BG6-OUT-H	21
		P	BUS-BG5-IN-H	21
		R	BUS-BG5-OUT-H	21
		S	BUS-BG4-IN-H	21
6	GND	T	BUS-BG4-OUT-H	21
		U		
		V		

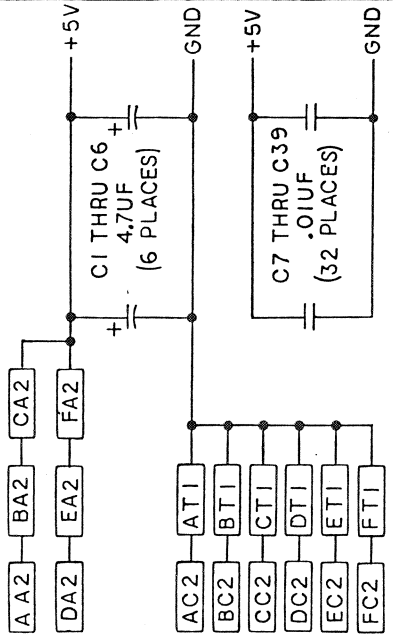
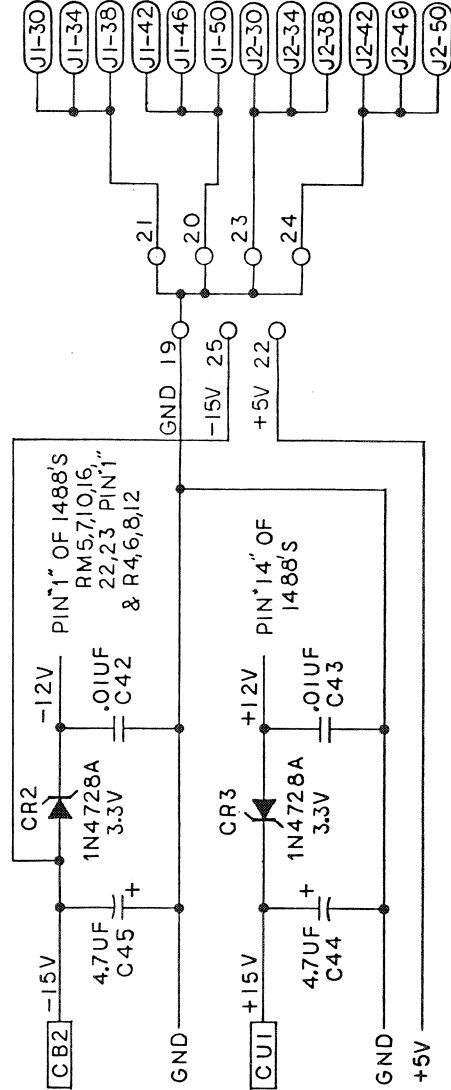
SHT	I	F	2	SHT
		A	+5V	6
		B		
		C	GND	6
19	BUS-BBSY-L	D		
		E		
		F		
		H		
19	BUS-NPR-L	J		
		K		
		L		
19	BUS-INTR-L	M		
		N		
		P		
		R		
		S		
6	GND	T	BUS-SACK-L	19
		U		
		V		

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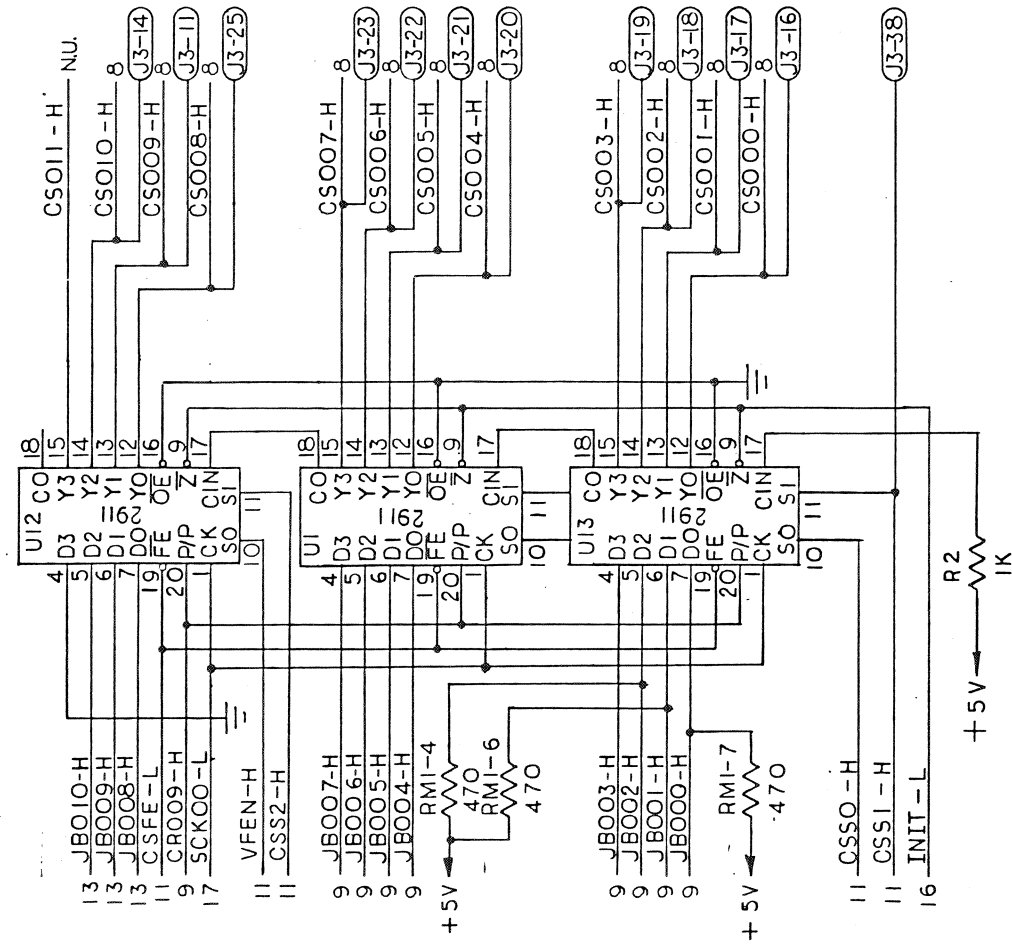
SHT	J 1	SHT
40	DTR00-H 1 2 CARRO0-H 38	38
40	DTR01-H 3 4 CARRO1-H 38	38
40	DTR02-H 5 6 CARRO2-H 38	38
40	DTR03-H 7 8 CARRO3-H 38	38
40	DTR04-H 9 10 CARRO4-H 38	38
40	DTR05-H 11 12 CARRO5-H 38	38
40	DTR06-H 13 14 CARRO6-H 38	38
40	DTR07-H 15 16 CARRO7-H 38	38
23	MAIN-H 17 18 GND 36	
36	TXD00-H 19 20 RING00-H 39	
37	RXD00-H 21 22 GND 36	
36	TXD01-H 23 24 RING01-H 39	
37	RXD01-H 25 26 GND 36	
36	TXD02-H 27 28 RING02-H 39	
37	RXD02-H 29 30 GND 36	
36	TXD03-H 31 32 RING03-H 39	
37	RXD03-H 33 34 GND 36	
36	TXD04-H 35 36 RING04-H 39	
37	RXD04-H 37 38 GND 36	
36	TXD05-H 39 40 RING05-H 39	
37	RXD05-H 41 42 GND 36	
36	TXD06-H 43 44 RING06-H 39	
37	RXD06-H 45 46 GND 36	
36	TXD07-H 47 48 RING07-H 39	
37	RXD07-H 49 50 GND 36	

SHT	J 2	SHT
40	DTR08-H 1 2 CARRO8-H 38	38
40	DTR09-H 3 4 CARRO9-H 38	38
40	DTR10-H 5 6 CARR10-H 38	38
40	DTR11-H 7 8 CARR11-H 38	38
40	DTR12-H 9 10 CARR12-H 38	38
40	DTR13-H 11 12 CARR13-H 38	38
40	DTR14-H 13 14 CARR14-H 38	38
40	DTR15-H 15 16 CARR15-H 38	38
36	GND 17 18 GND 36	
36	TXD08-H 19 20 RING08-H 39	
37	RXD08-H 21 22 GND 36	
36	TXD09-H 23 24 RING09-H 39	
37	RXD09-H 25 26 GND 36	
36	TXD10-H 27 28 RING10-H 39	
37	RXD10-H 29 30 GND 36	
36	TXD11-H 31 32 RING11-H 39	
37	RXD11-H 33 34 GND 36	
36	TXD12-H 35 36 RING12-H 39	
37	RXD12-H 37 38 GND 36	
36	TXD13-H 39 40 RING13-H 39	
37	RXD13-H 41 42 GND 36	
36	TXD14-H 43 44 RING14-H 39	
37	RXD14-H 45 46 GND 36	
36	TXD15-H 47 48 RING15-H 39	
37	RXD15-H 49 50 GND 36	

SHT	J 3	SHT
	GND 1 2 DB000-H 24	24
24	DB001-H 3 4 DB002-H 24	24
24	DB003-H 5 6 DB004-H 24	24
24	DB005-H 7 8 DB006-H 24	24
24	DB007-H 9 10 GND	
7	CS009-H 11 12	
	+5V 13 14 CS010-H 7	7
	GND 15 16 CS000-H 7	7
7	CS001-H 17 18 CS002-H 7	7
7	CS003-H 19 20 CS004-H 7	7
7	CS005-H 21 22 CS006-H 7	7
7	CS007-H 23 24 GND	
7	CS008-H 25 26	
17	MINIT-L 27 28	
17	MDCLO-L 29 30	
17	CSTP-L 31 32	
17	SYCK-L 33 34 GND	
22	SSW1-L 35 36 SSW2-L 22	22
22	SSW3-L 37 38 CSS1-H 7	7
	+5V 39 40	



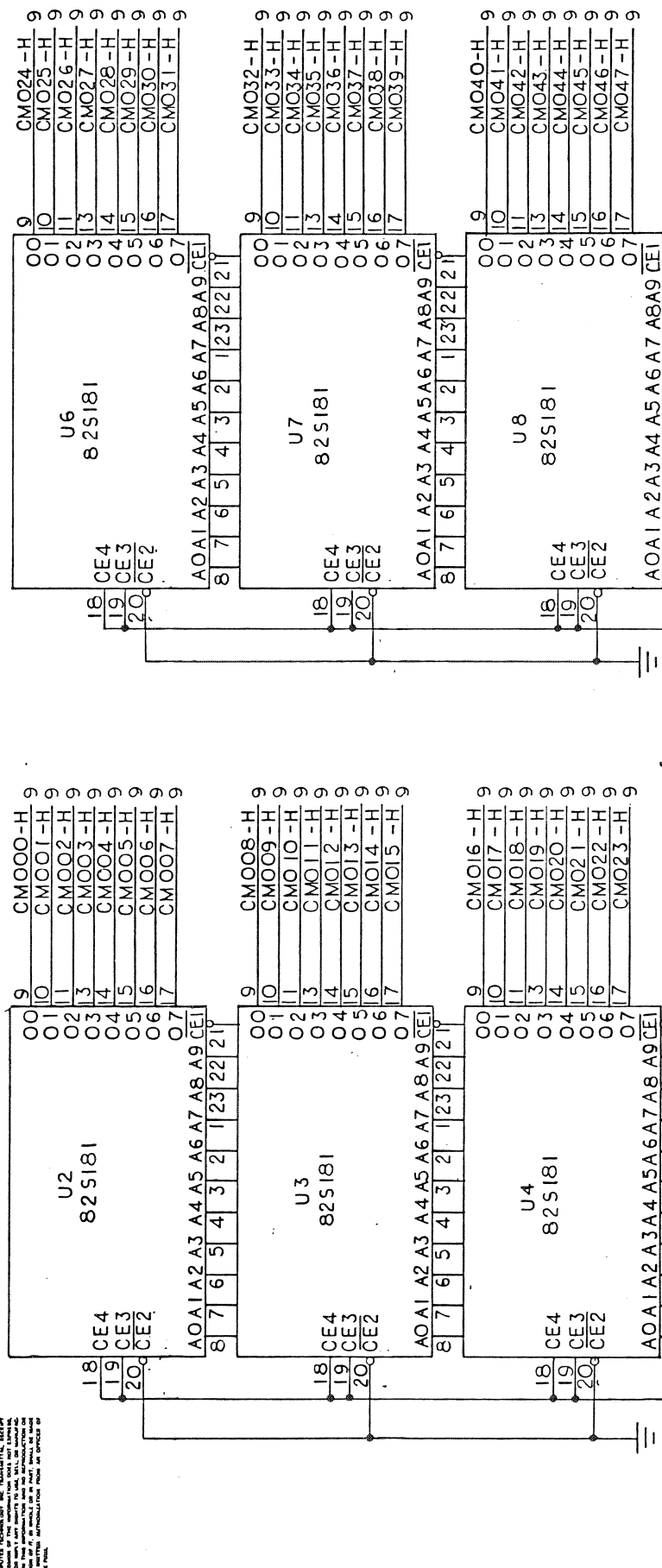
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SI	SO	OPERATION
0	0	INCREMENT
0	1	NOT IMPLEMENTED
1	0	RETURN
1	1	GOTO/MAP/CALL/VECTOR

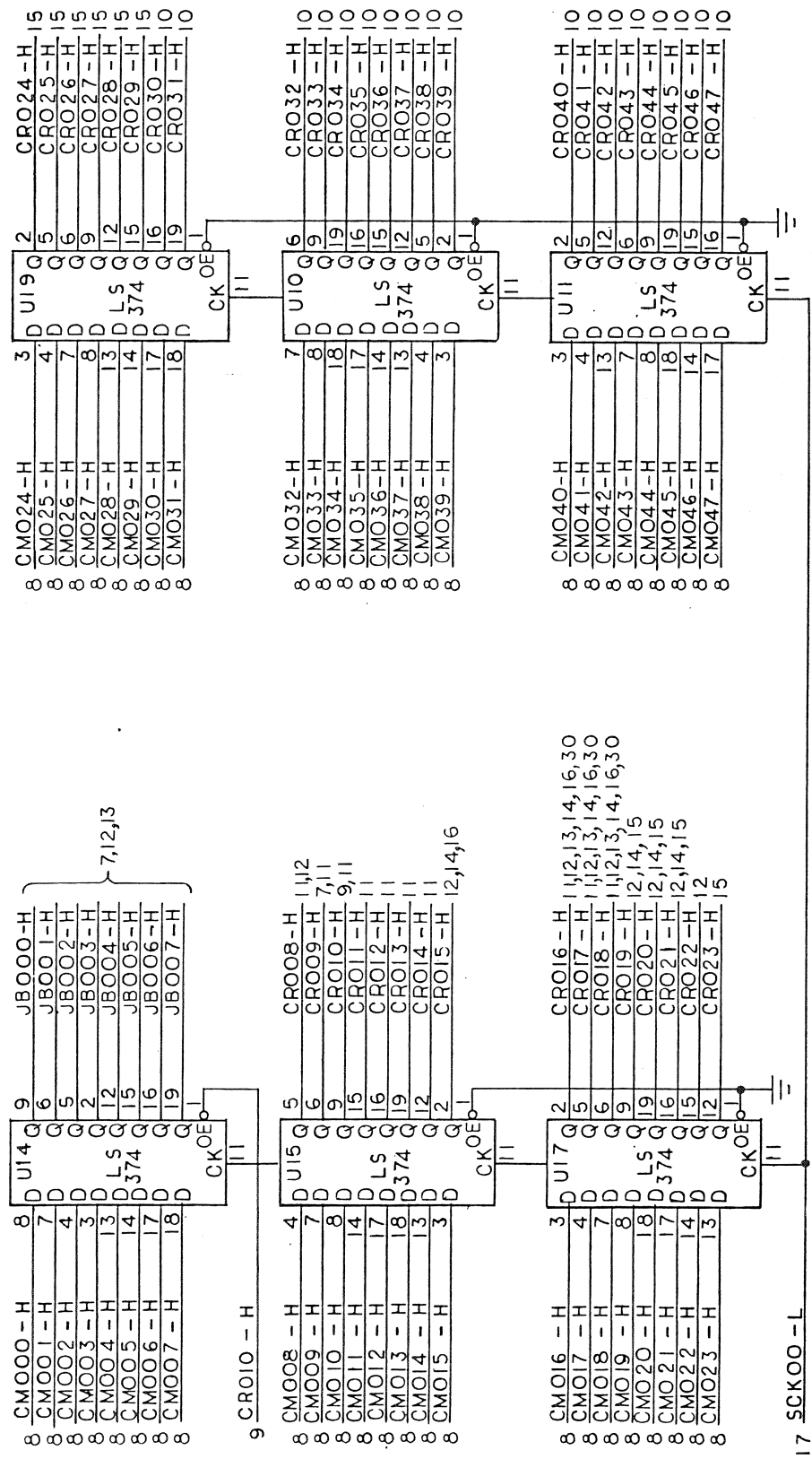
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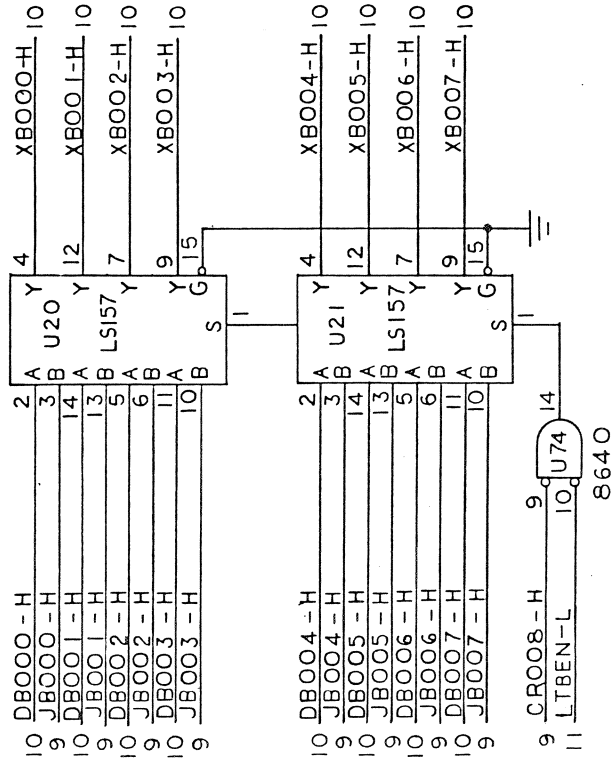
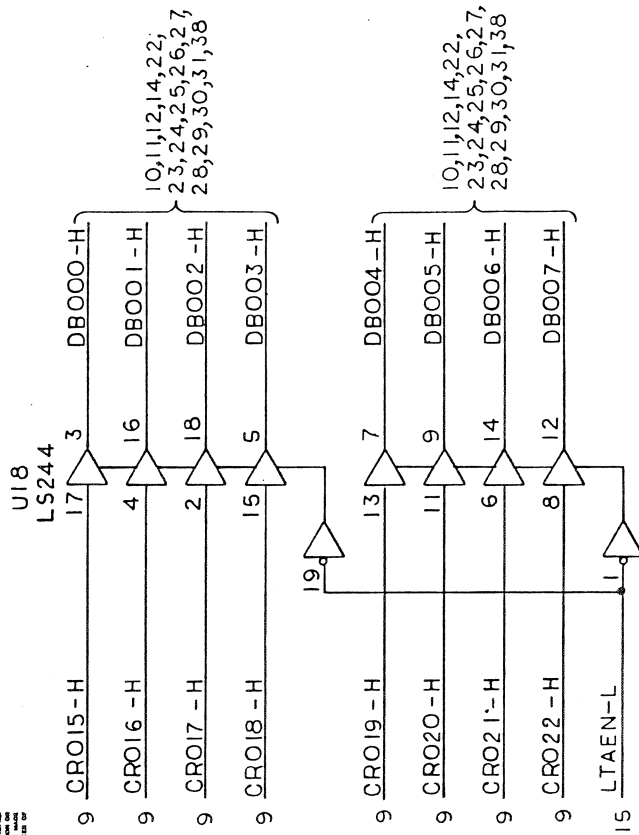
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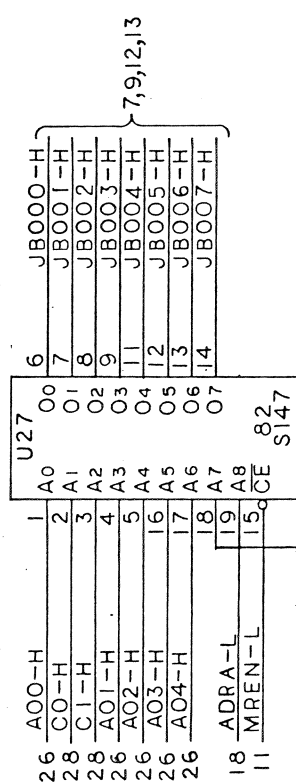
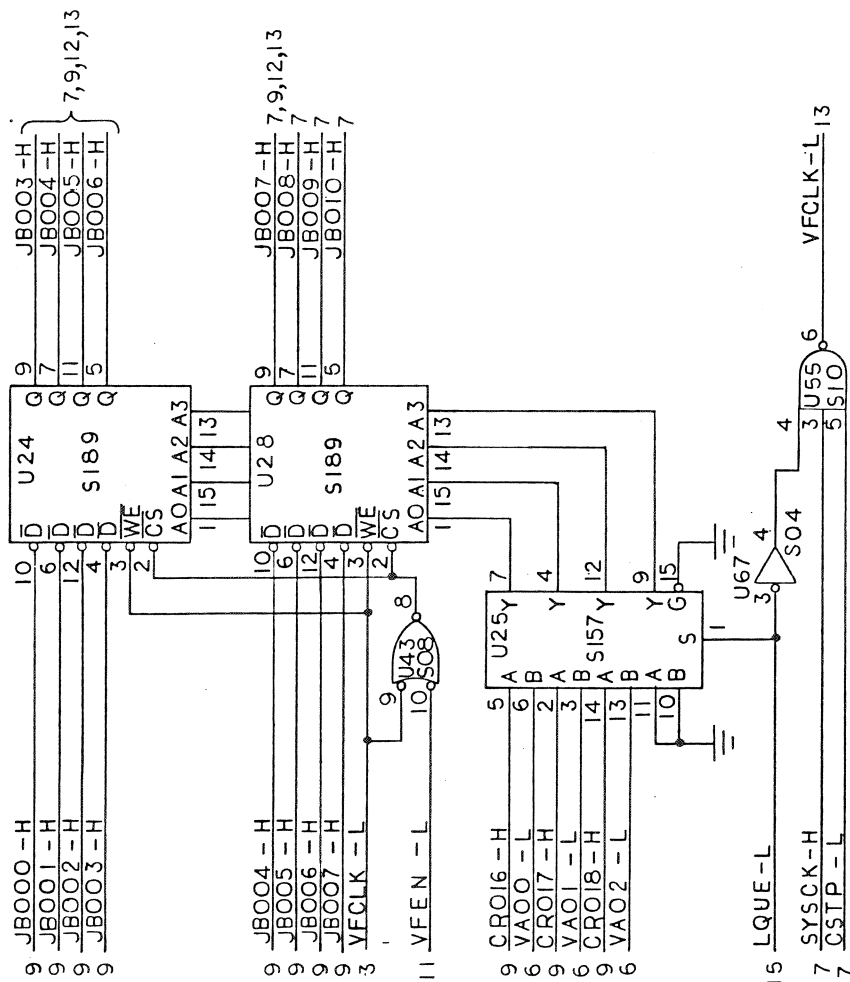


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MAP PROM

VECTOR FILE

DO NOT SCALE DRAWING
 SIZE DRAWING NO. B 10103003
 SHEET 14 OF 40

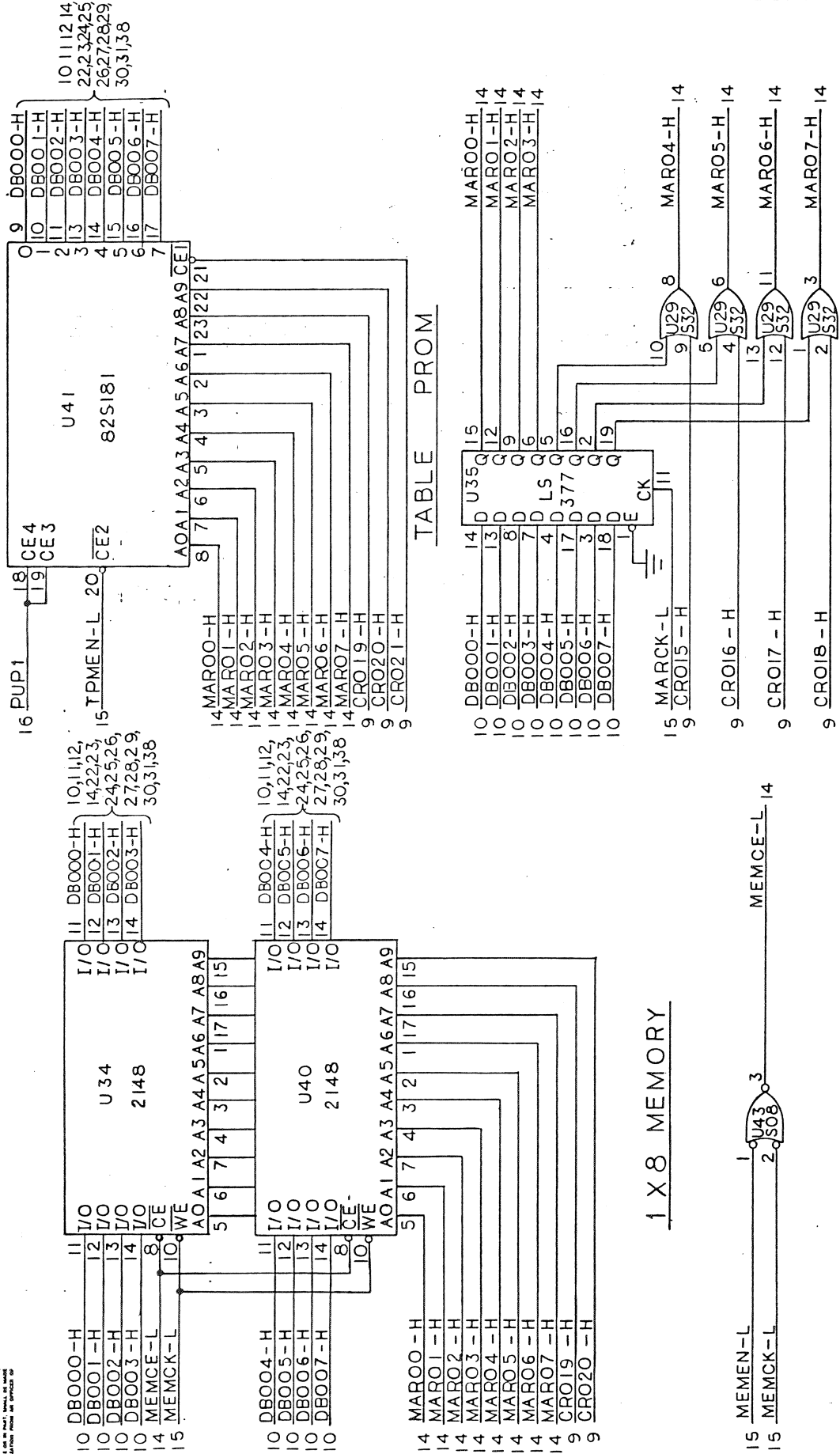


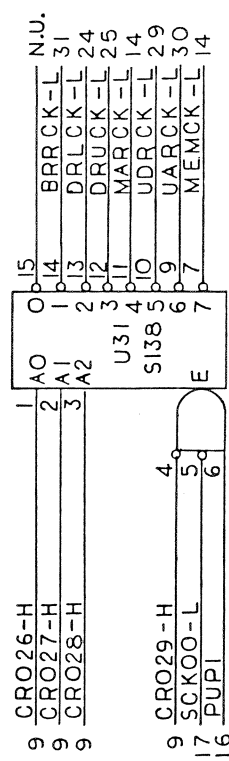
TABLE PROM

1 X 8 MEMORY

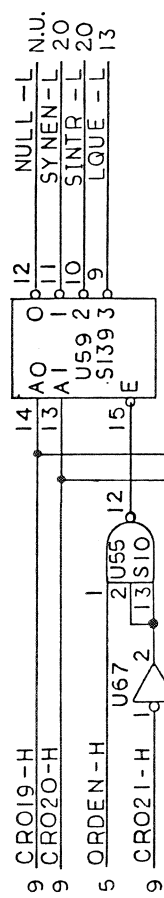
MEMORY ADDRESS REGISTER

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 SIZE DRAWING NO. B 10103003
 SHEET 14 OF 40

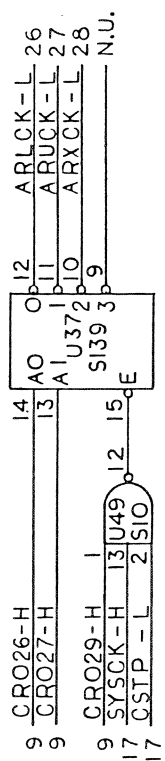
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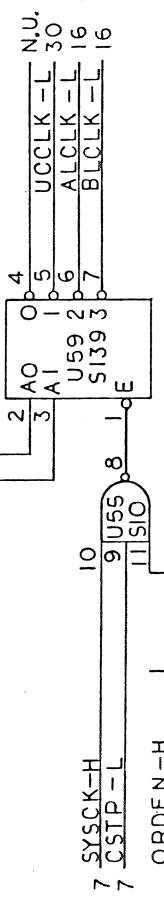
SOURCE ENABLES



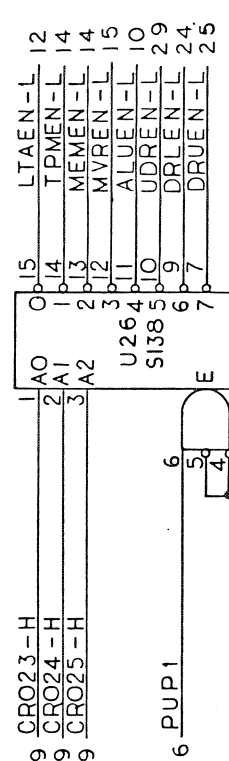
VECTOR AND CARRIER ENABLES



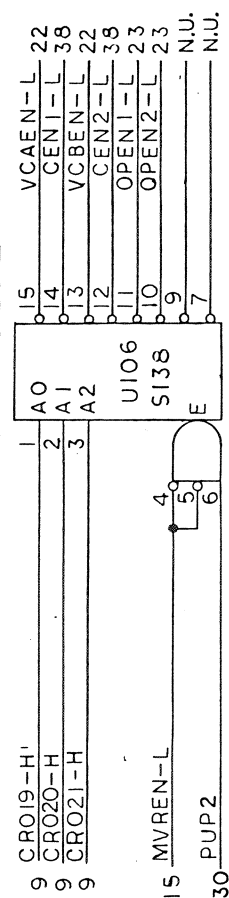
DESTINATION CLOCKS



ORDER DECODE

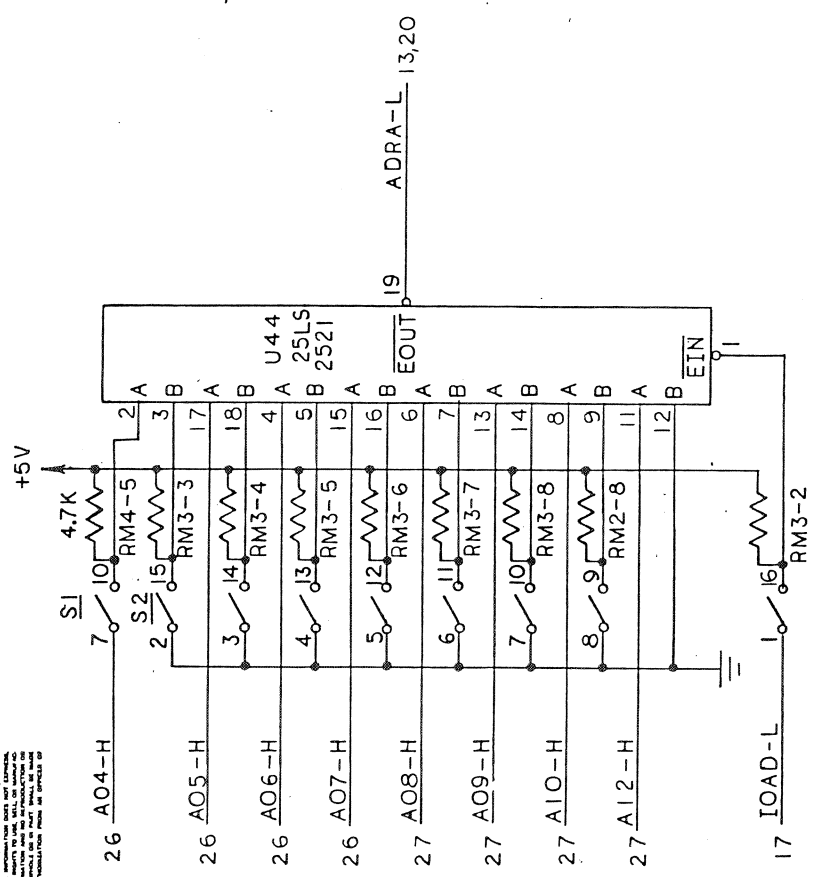


ORDER ENABLES

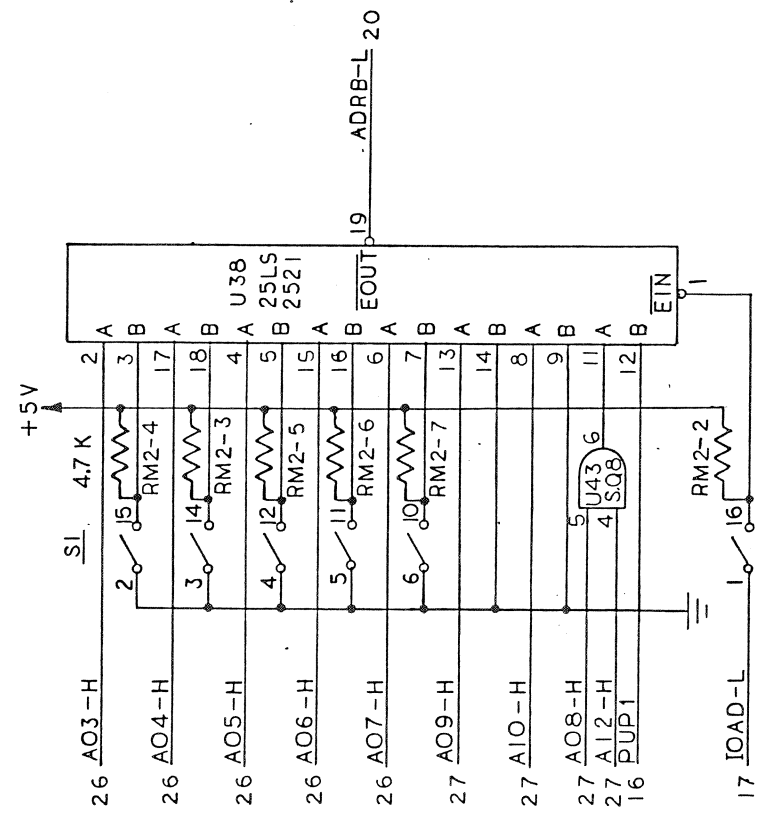


ORDER DECODE

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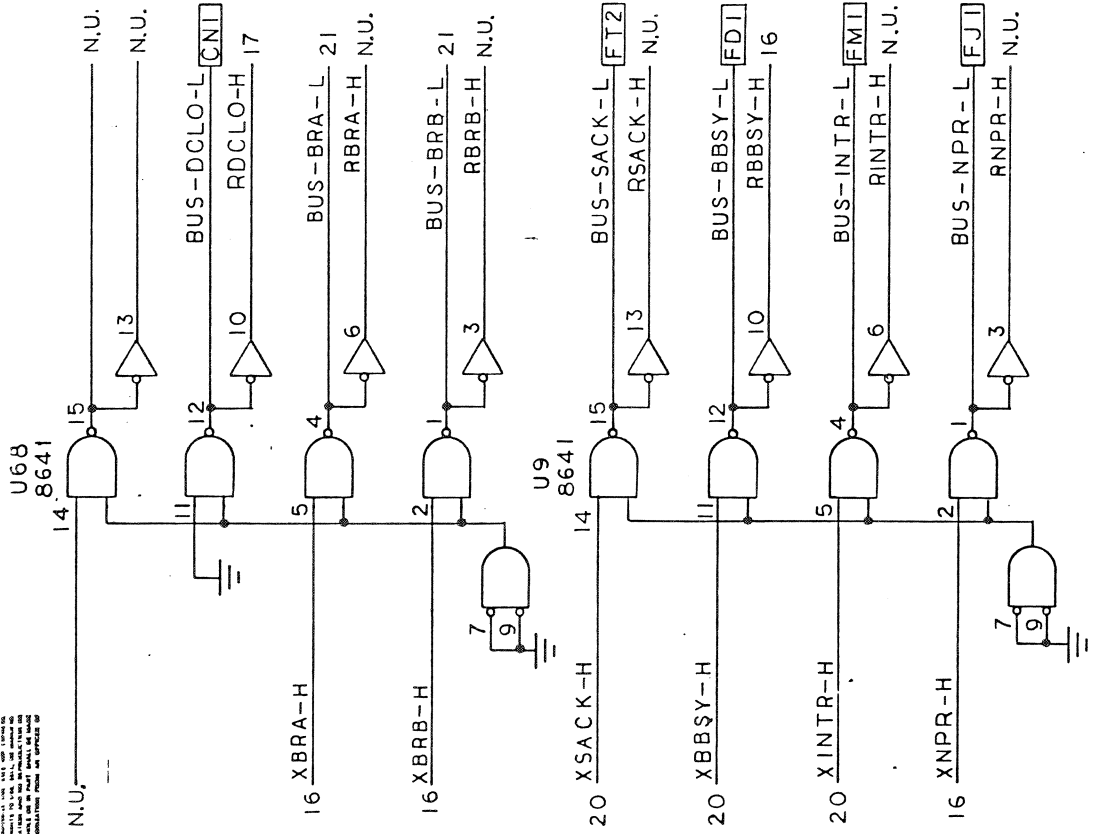


ADDRESS SELECT A

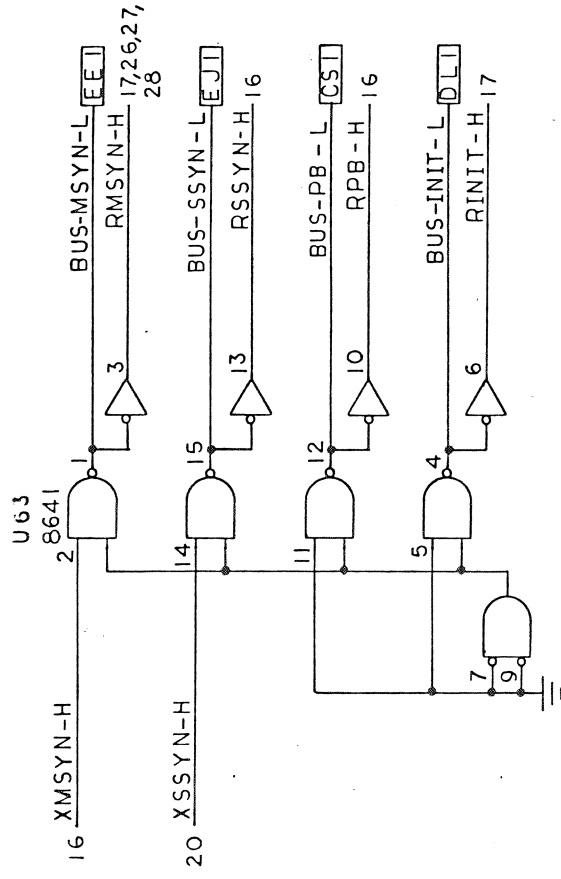


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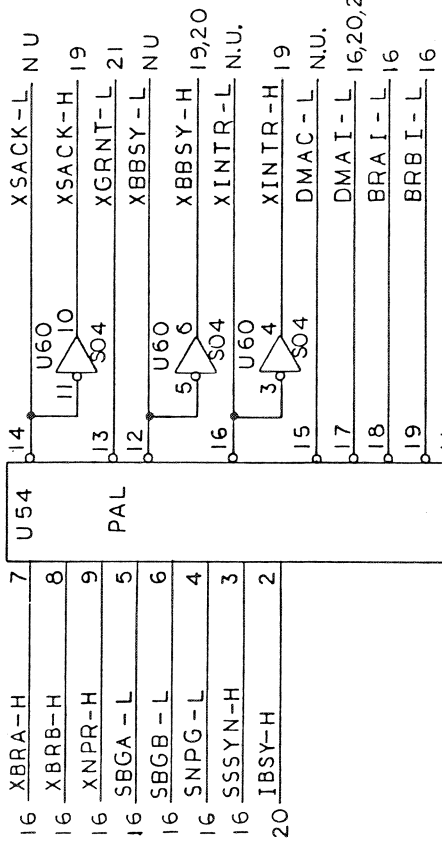


BUS TRANSCEIVERS

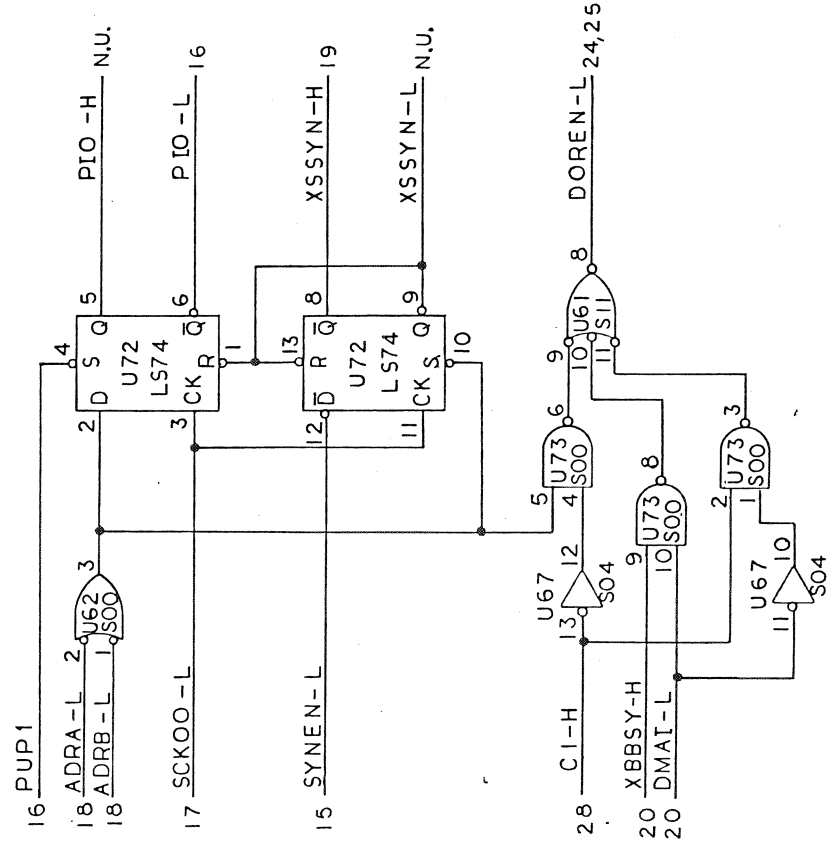


BUS TRANSCEIVERS

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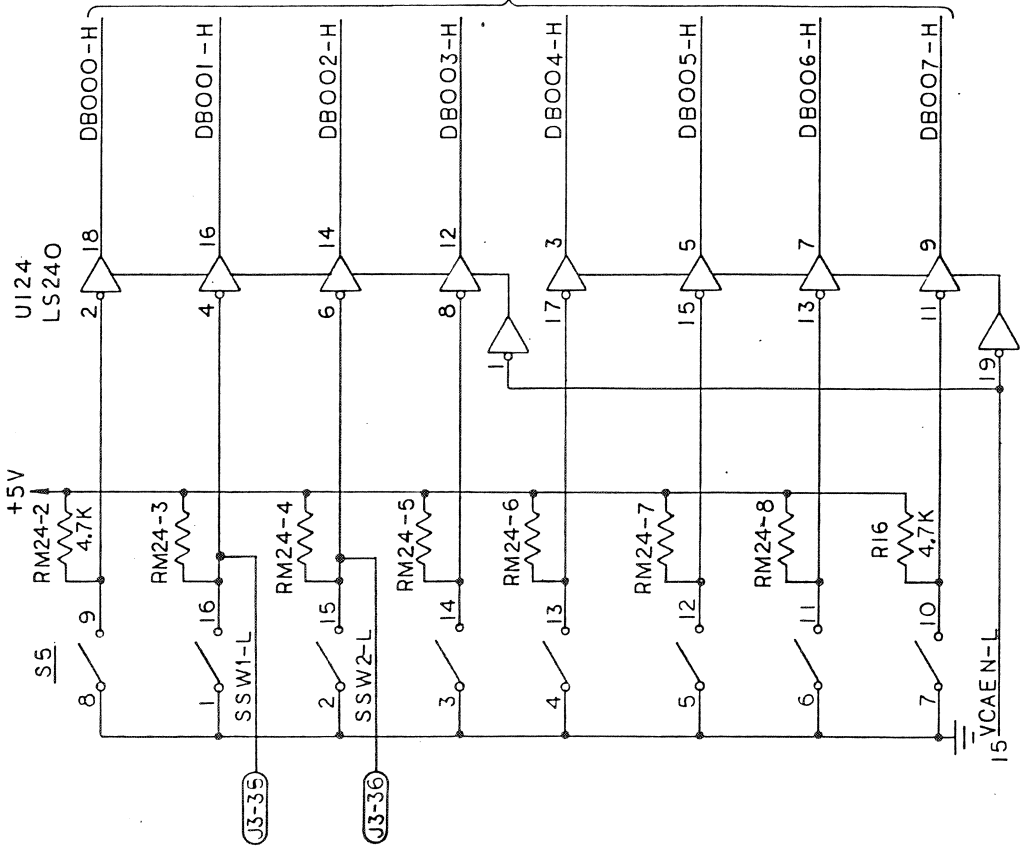


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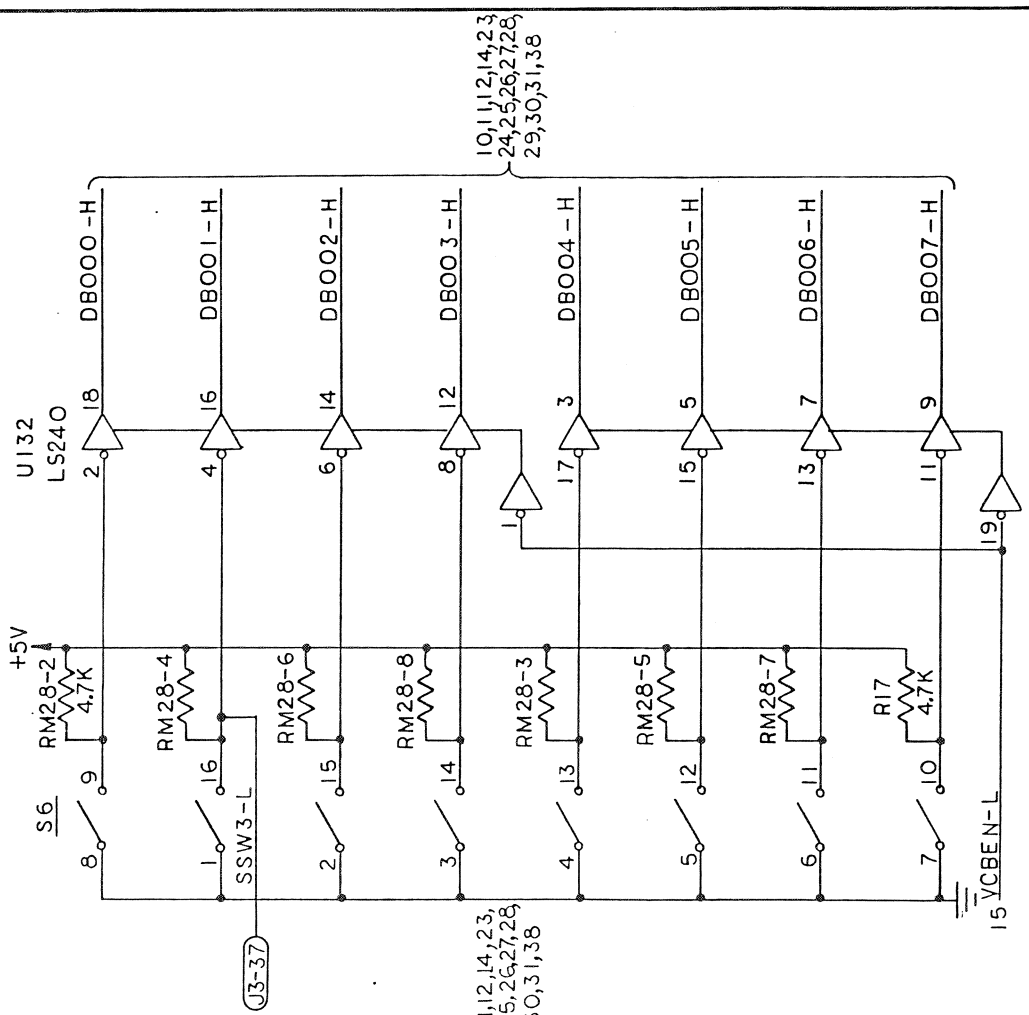


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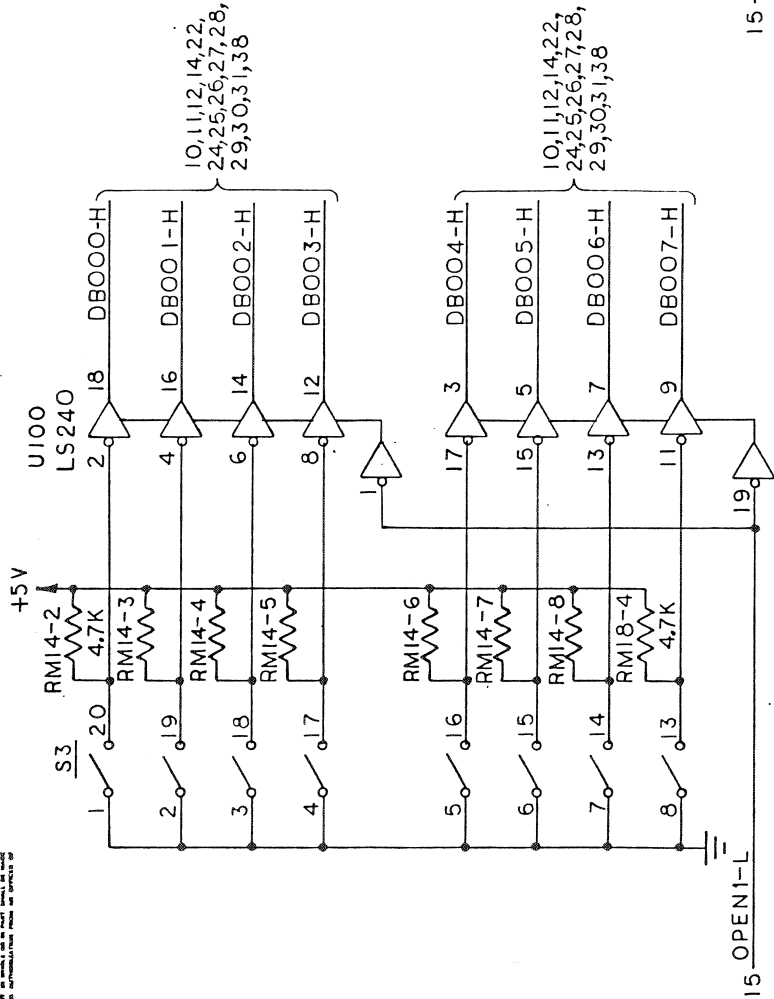


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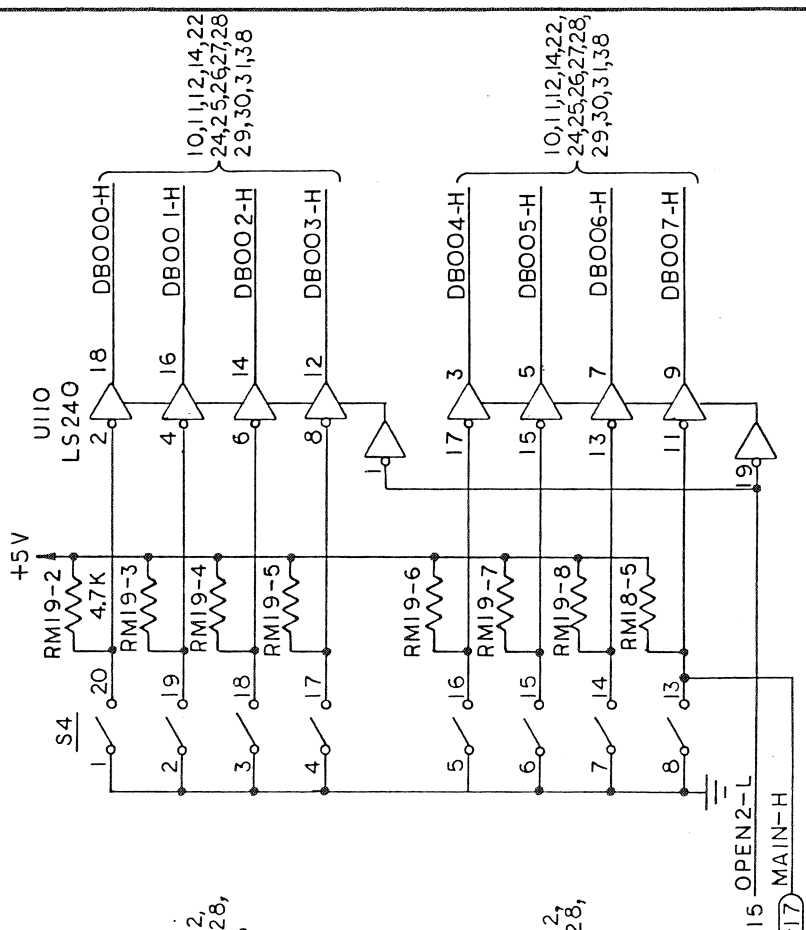
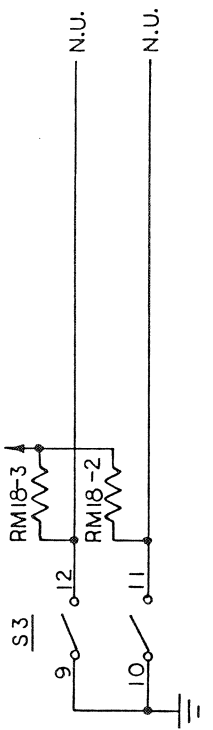


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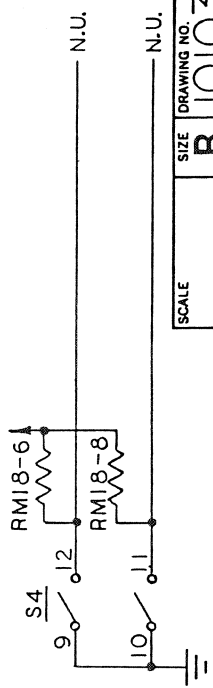
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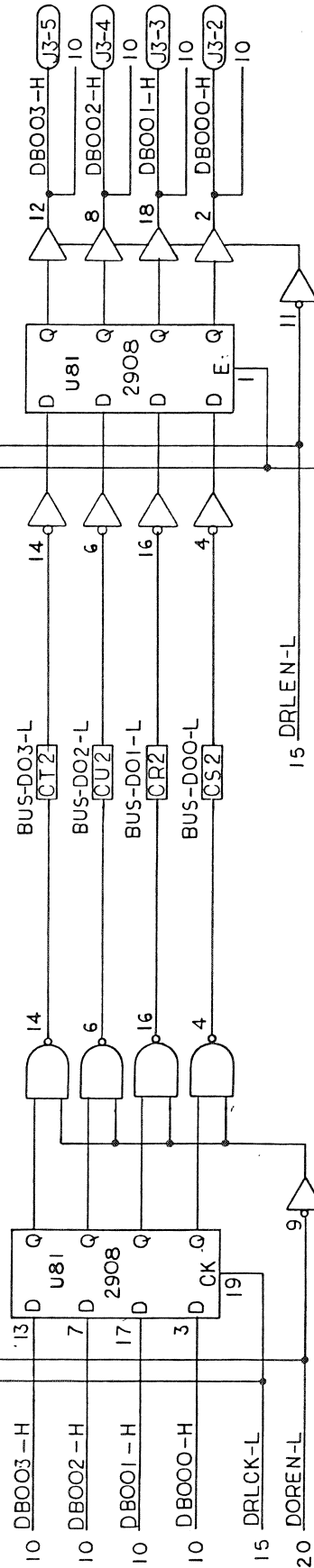
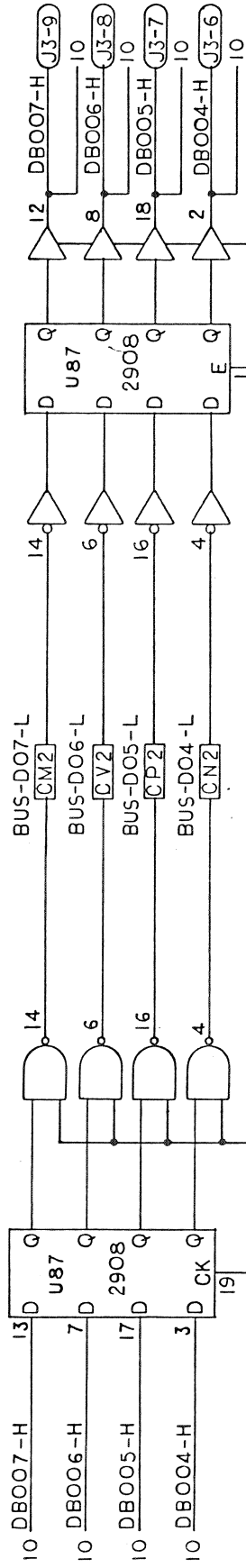
OPTION SWITCHES GROUP 1



OPTION SWITCHES - GROUP 2



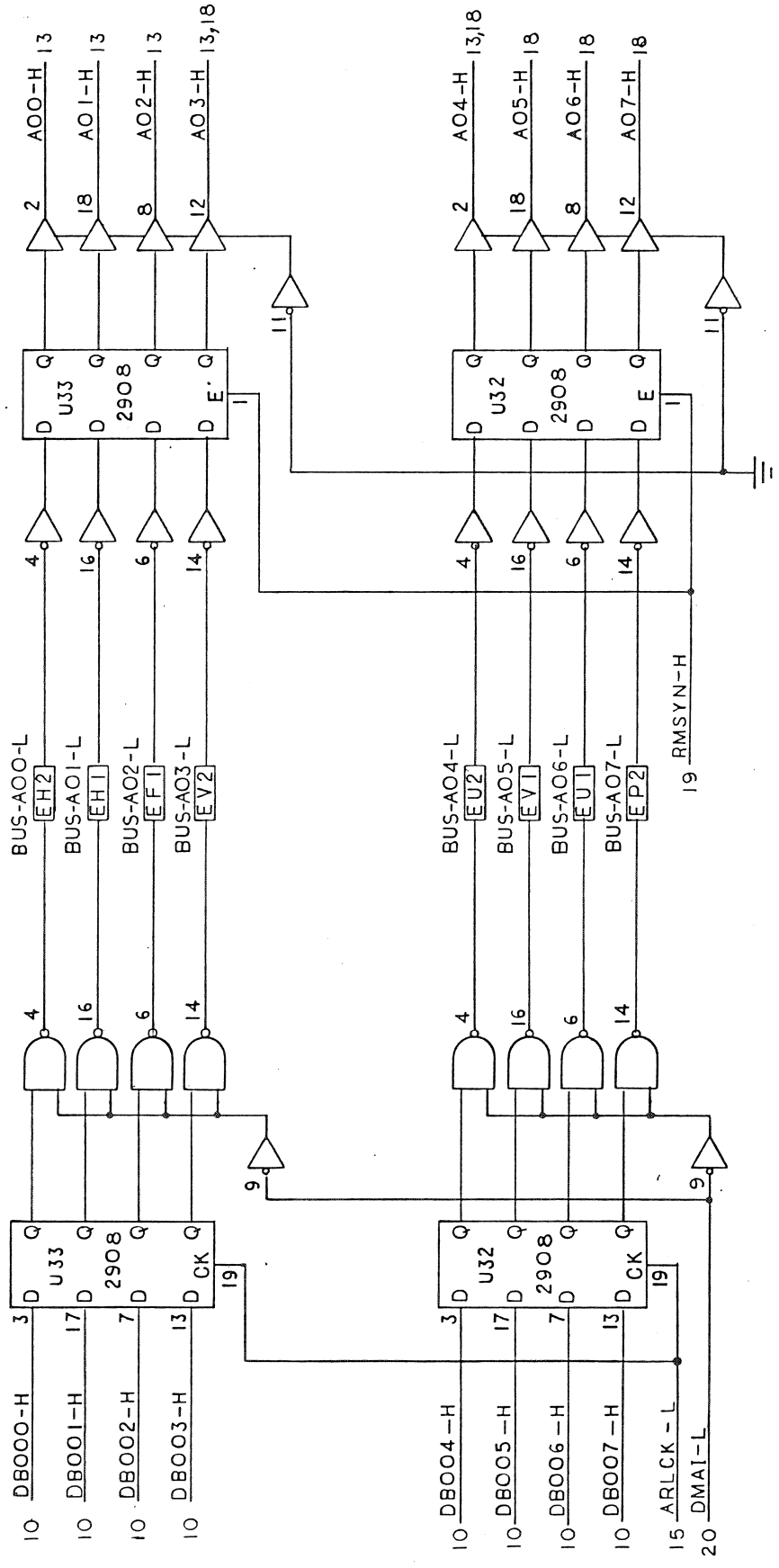
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 LOW BYTE

DATA INPUT REGISTER
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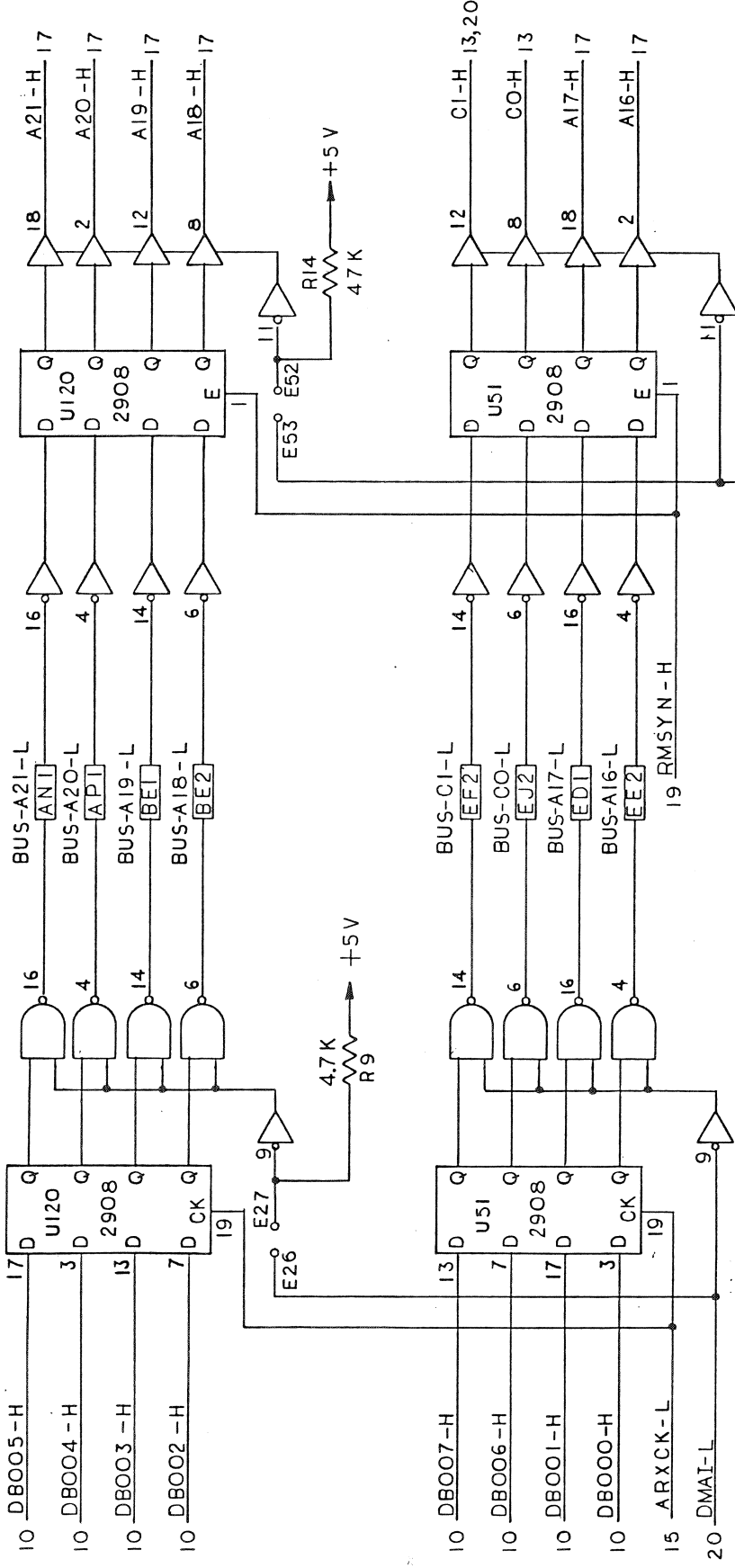
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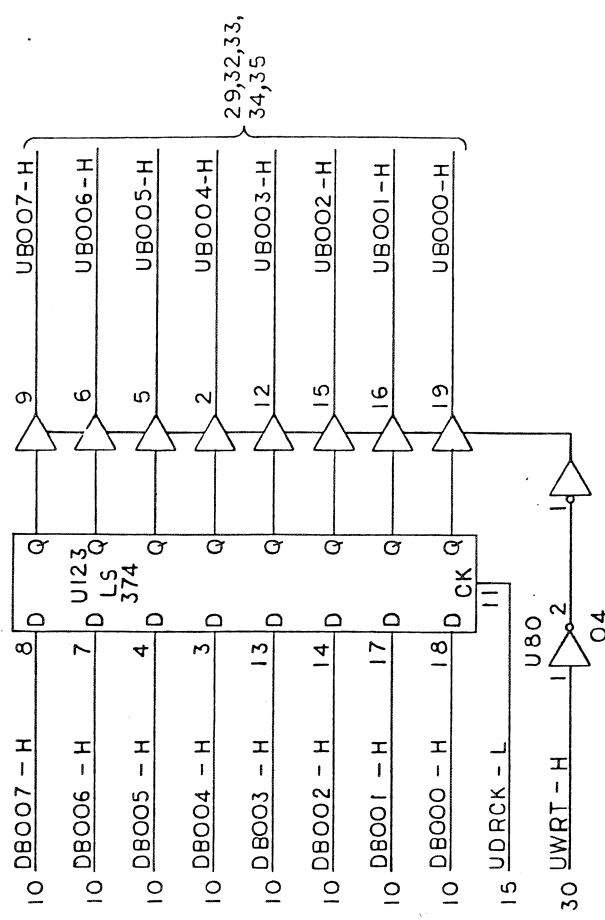
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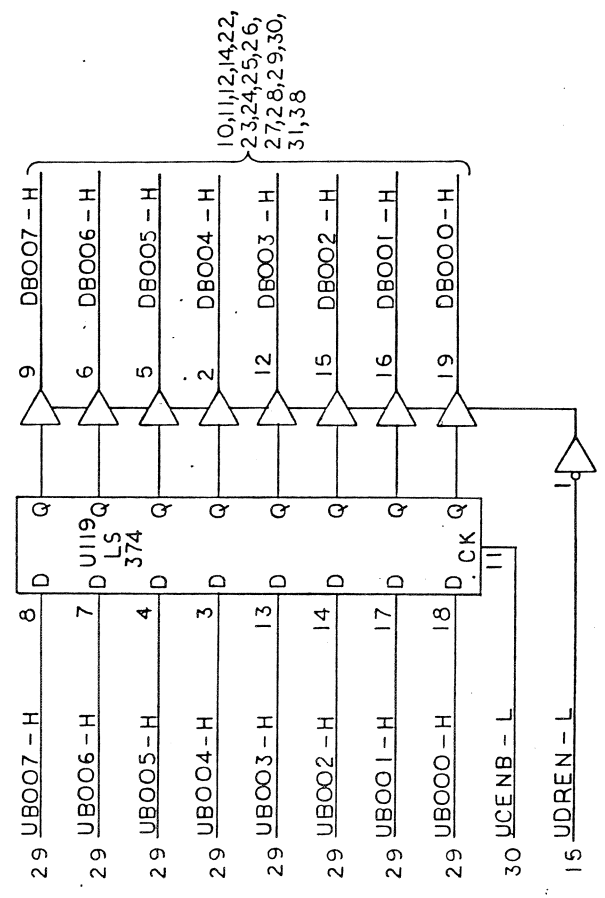
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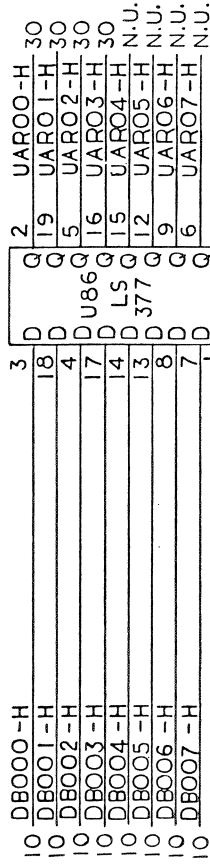
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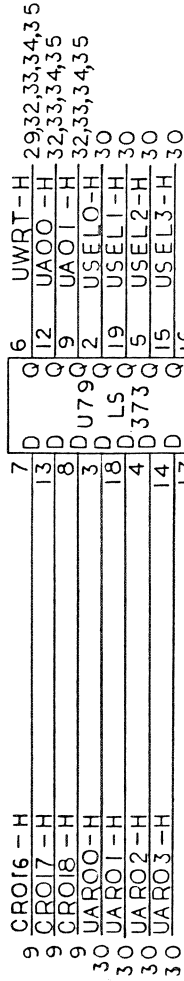
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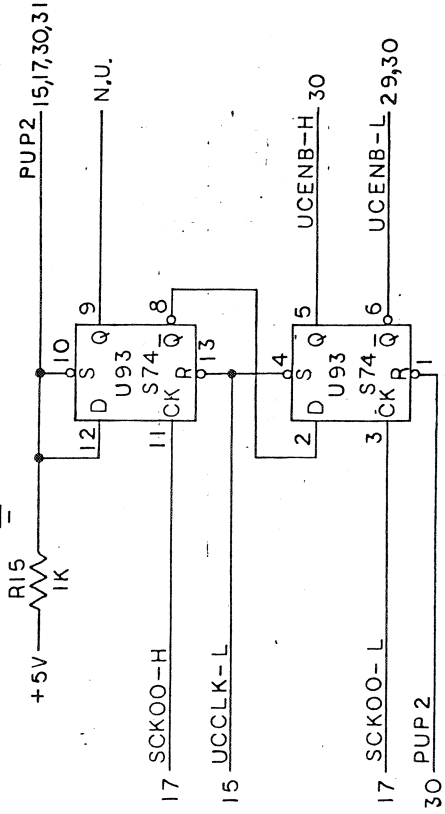
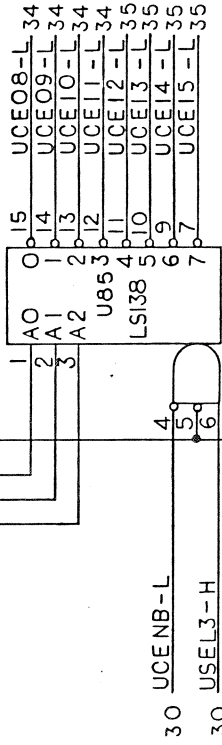
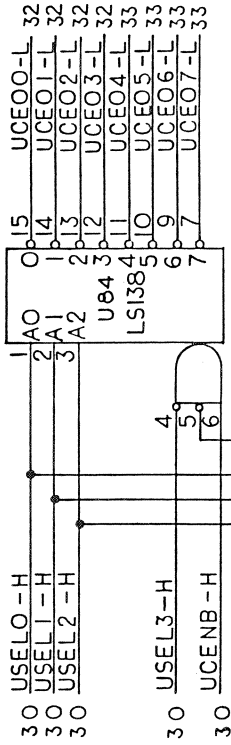
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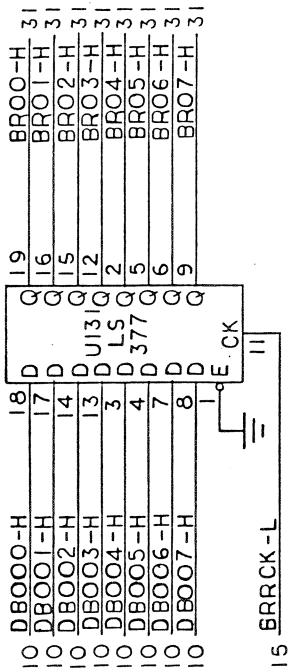


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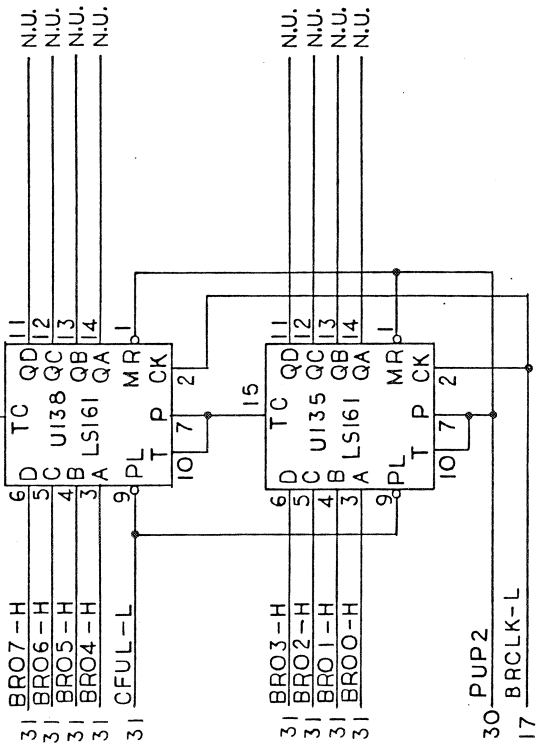
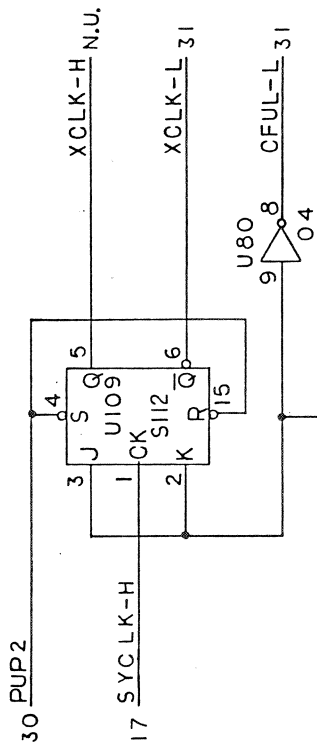
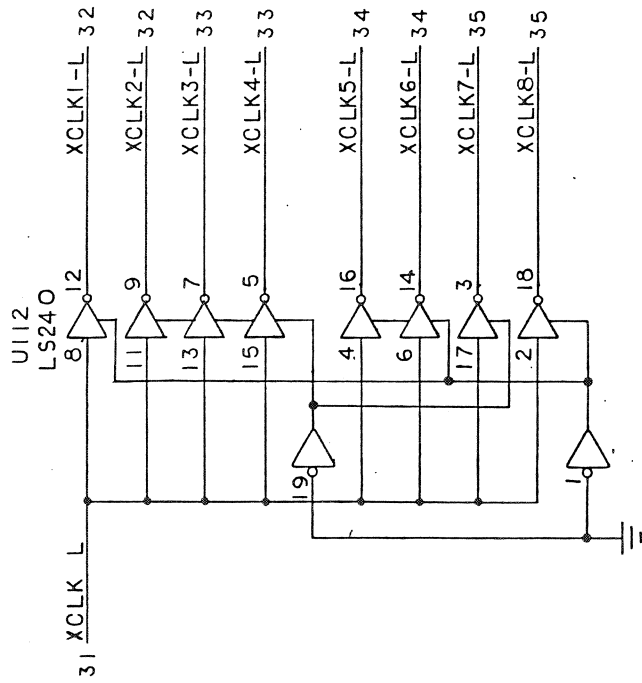


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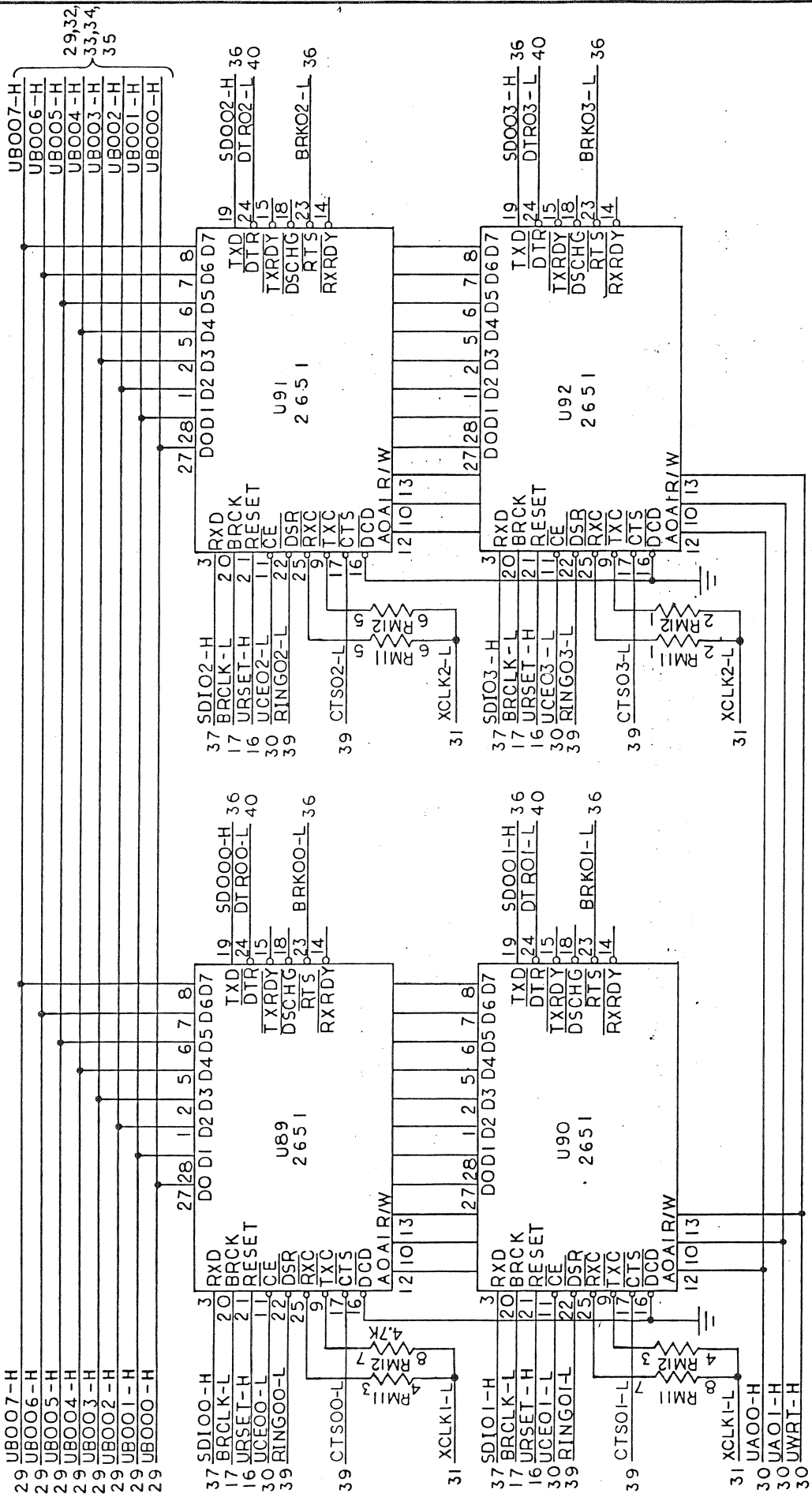


EXT. BAUD RATE REGISTER



UART EXT. CLOCK GENERATOR

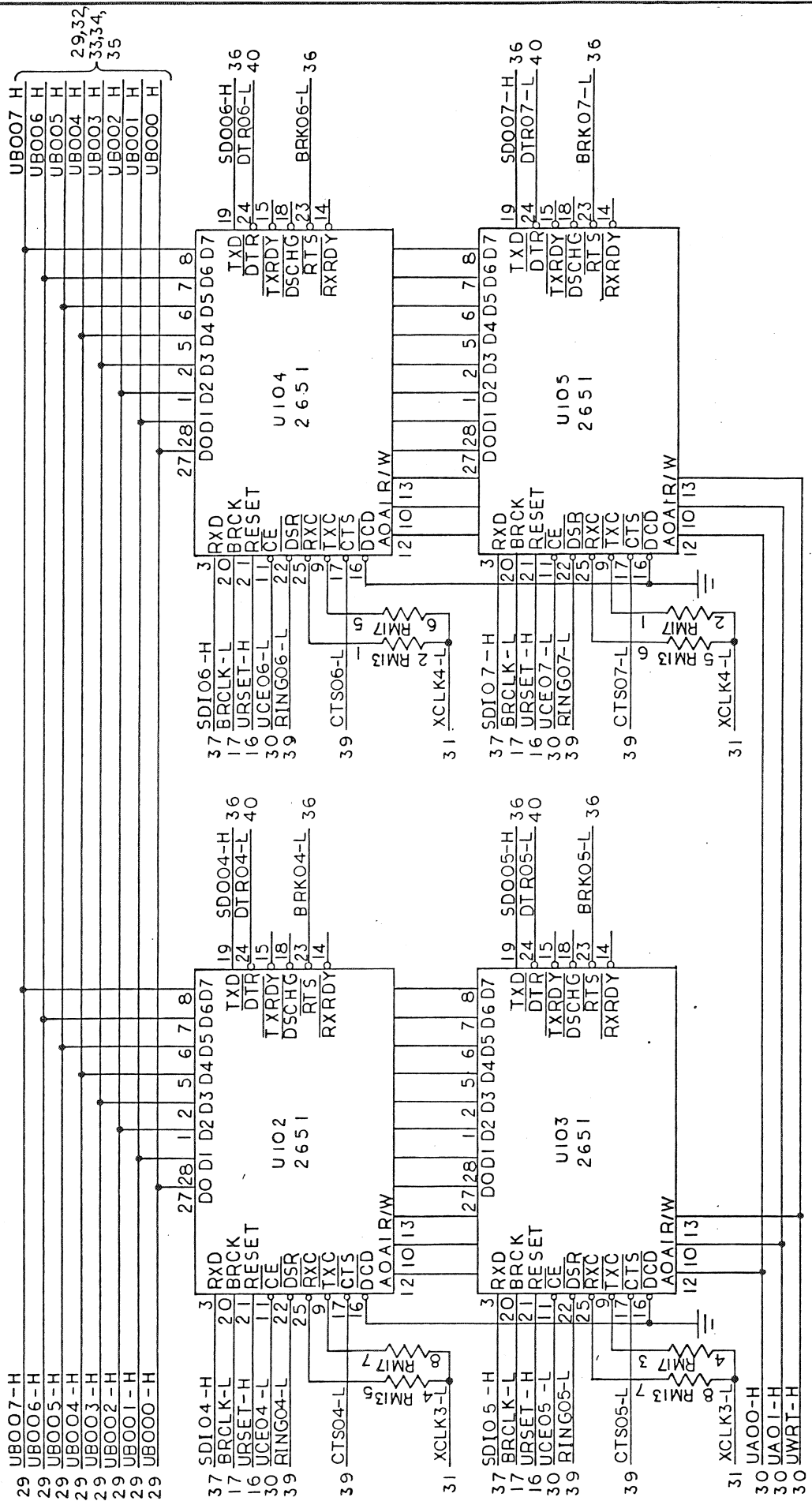
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UART CH0 AND CH1

UART CH2 AND CH3

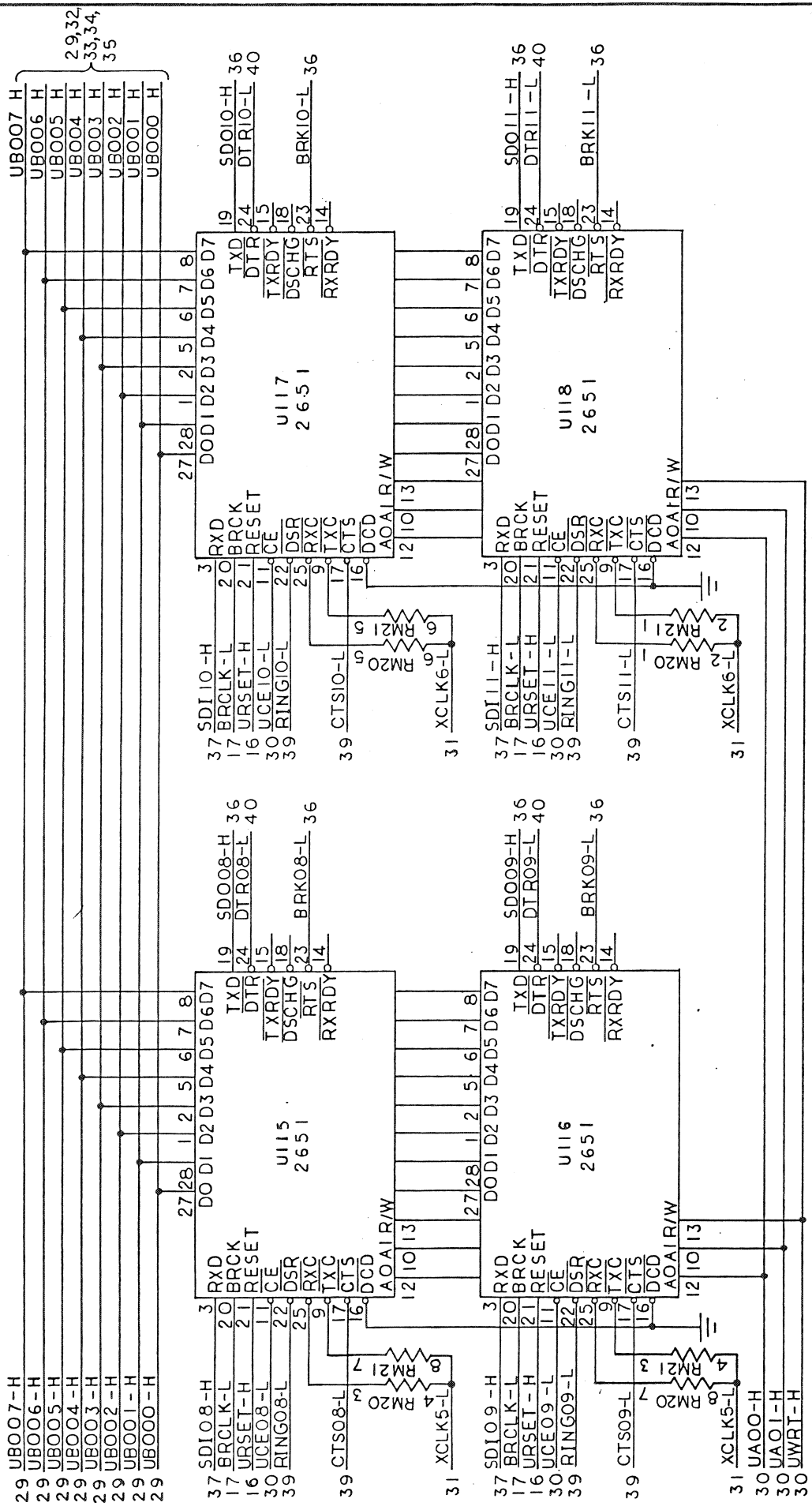
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UART CH4 AND CH5

UART CH6 AND CH7

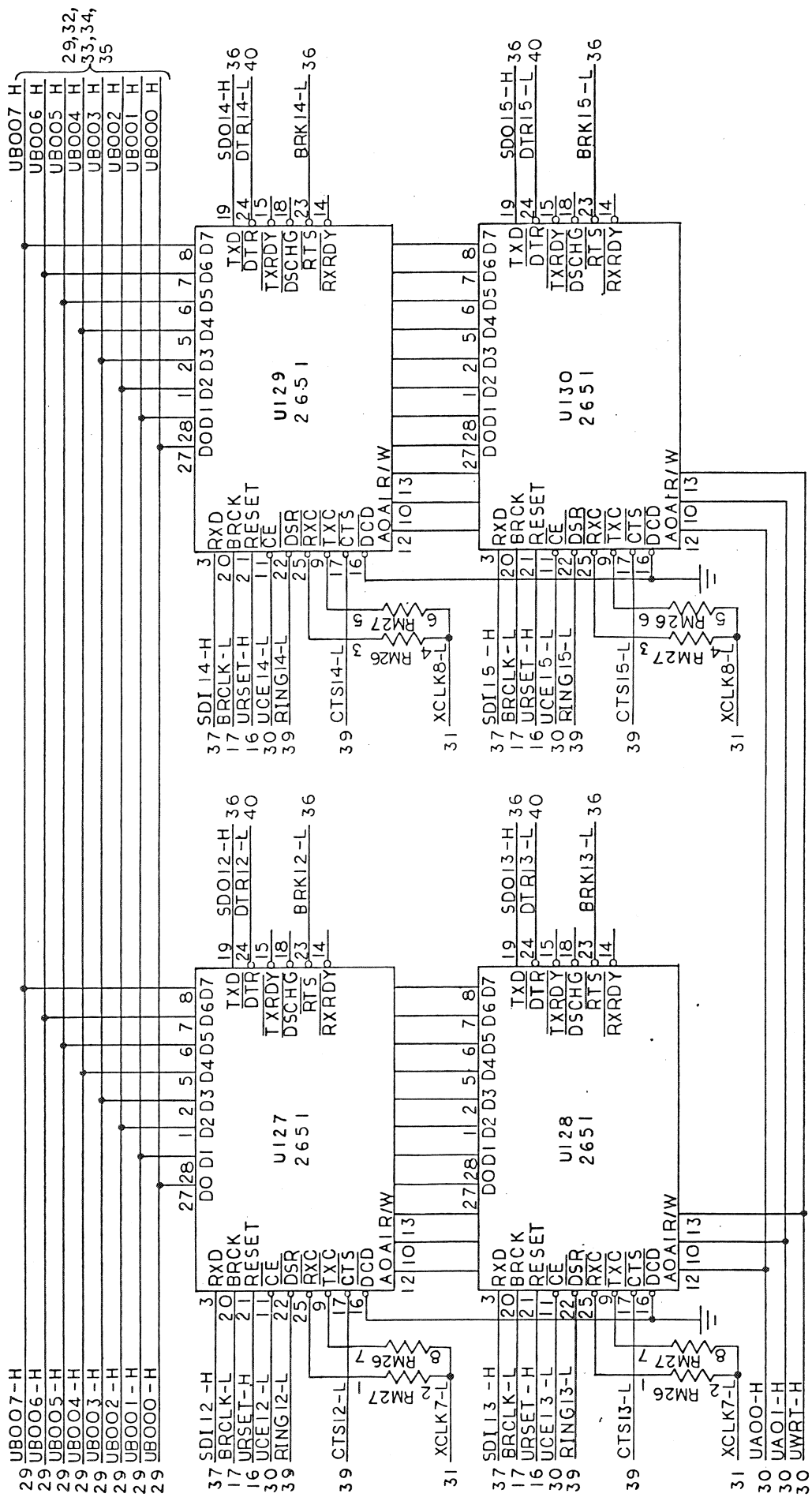
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UART CH8 AND CH9

UART CIO AND CH11

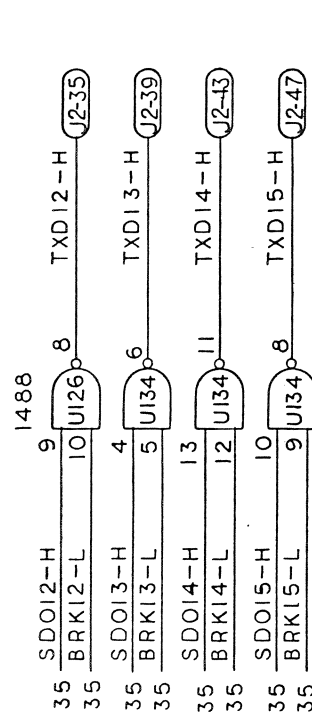
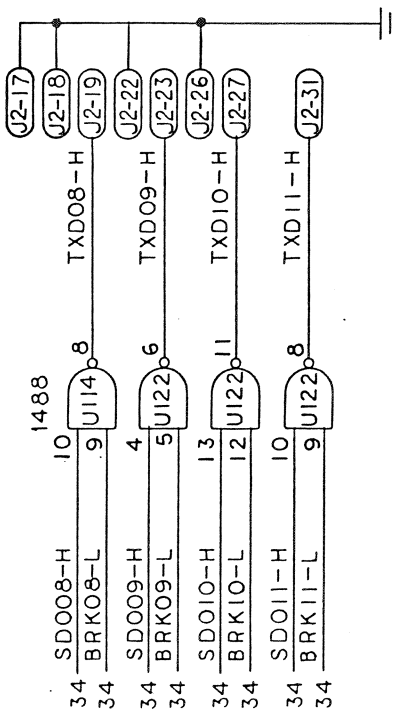
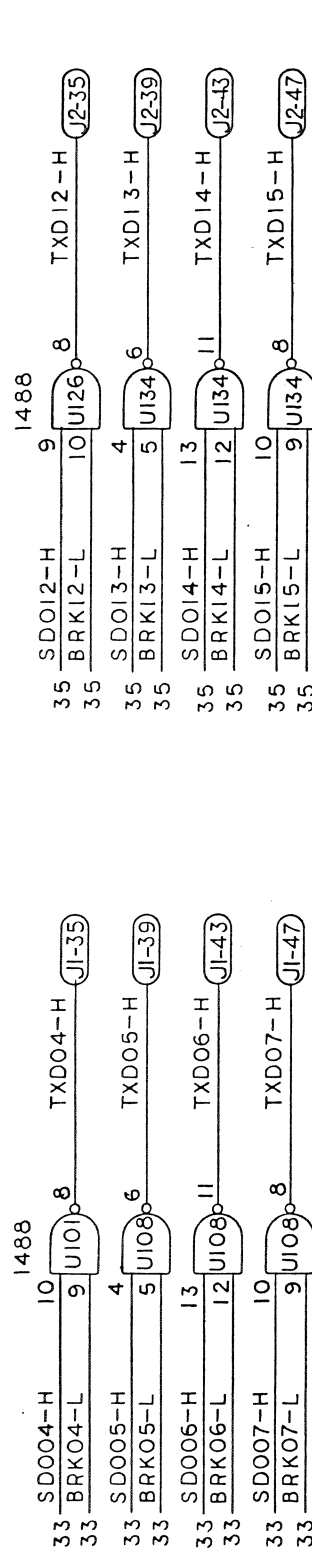
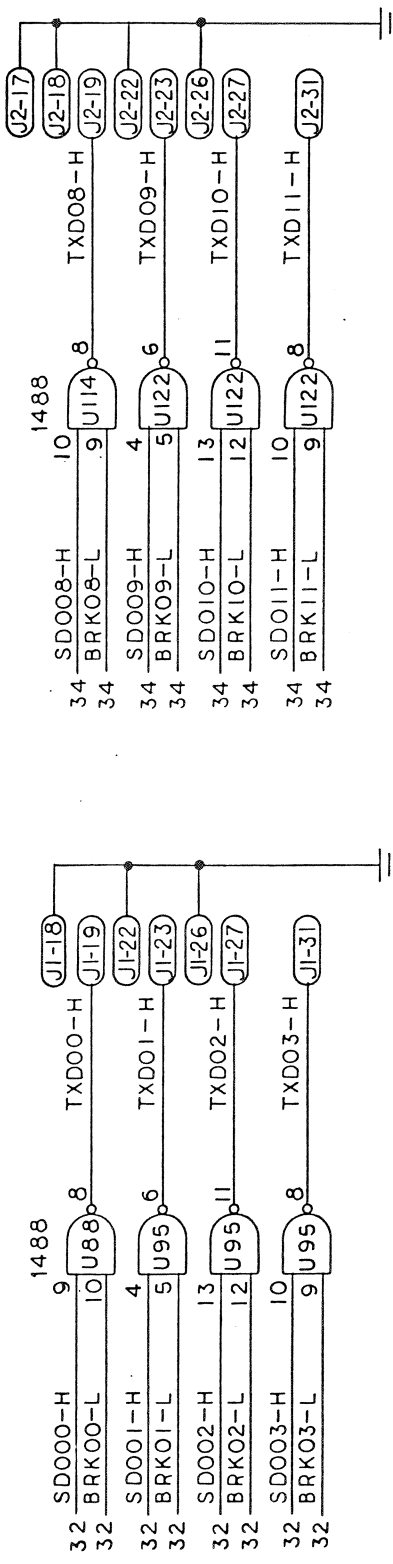
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UART CHI2 AND CHI3

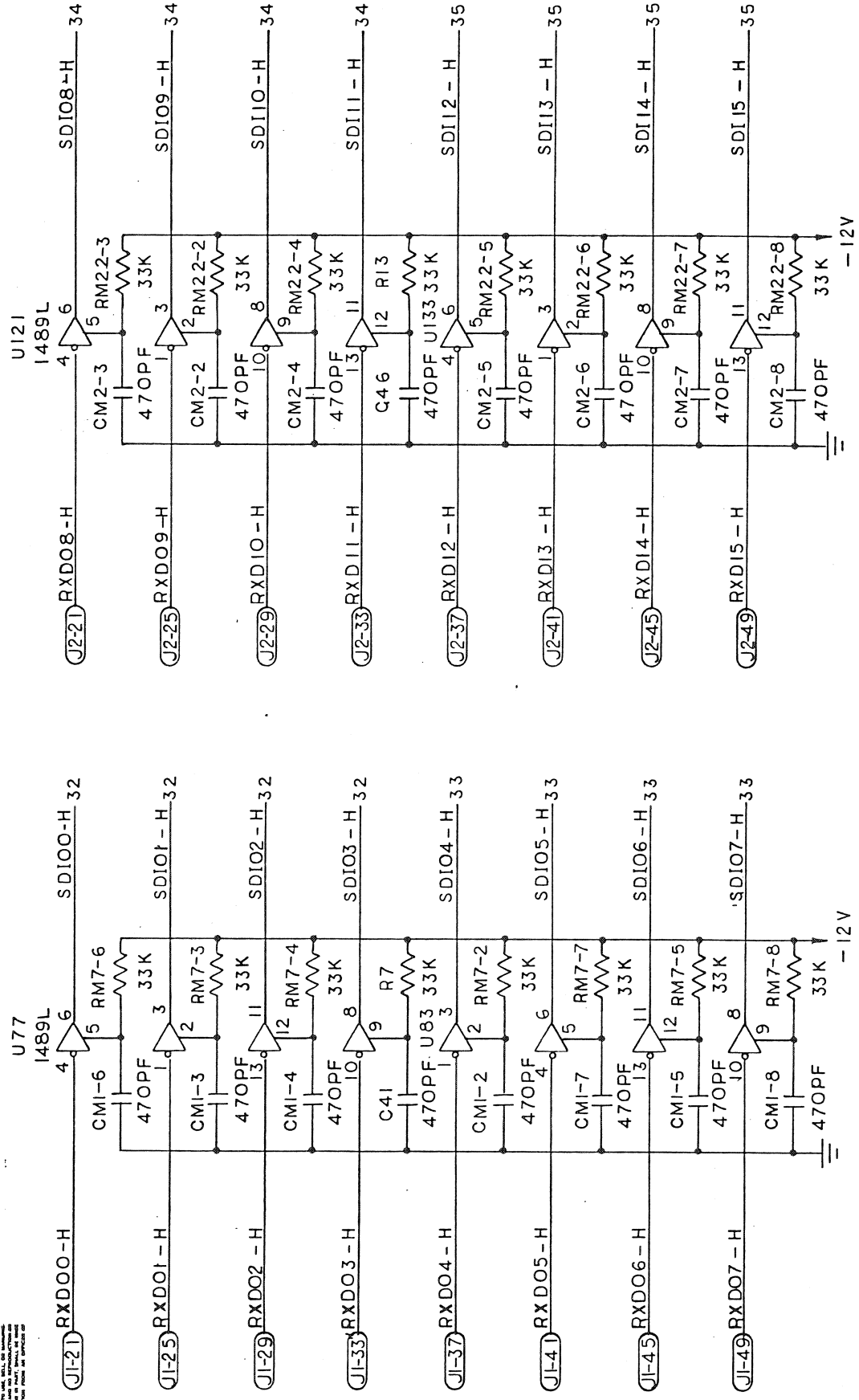
UART CHI4 AND CHI5

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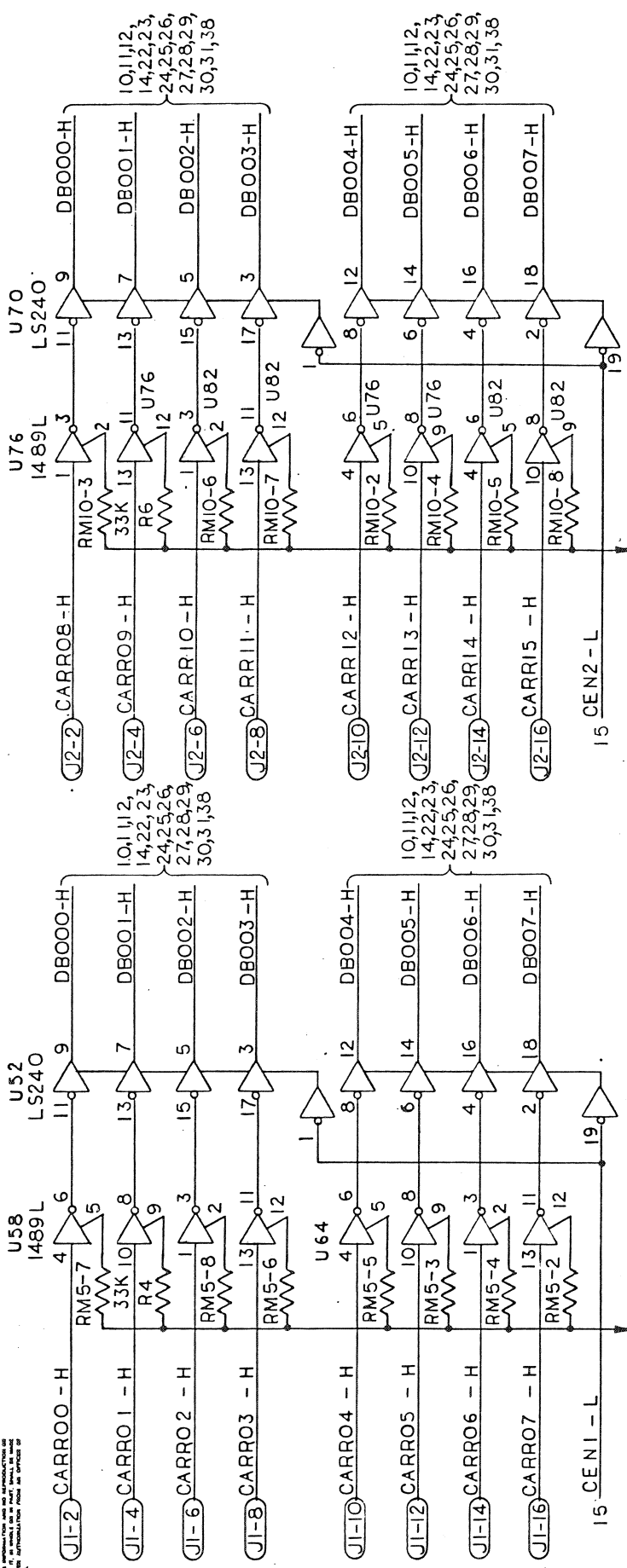


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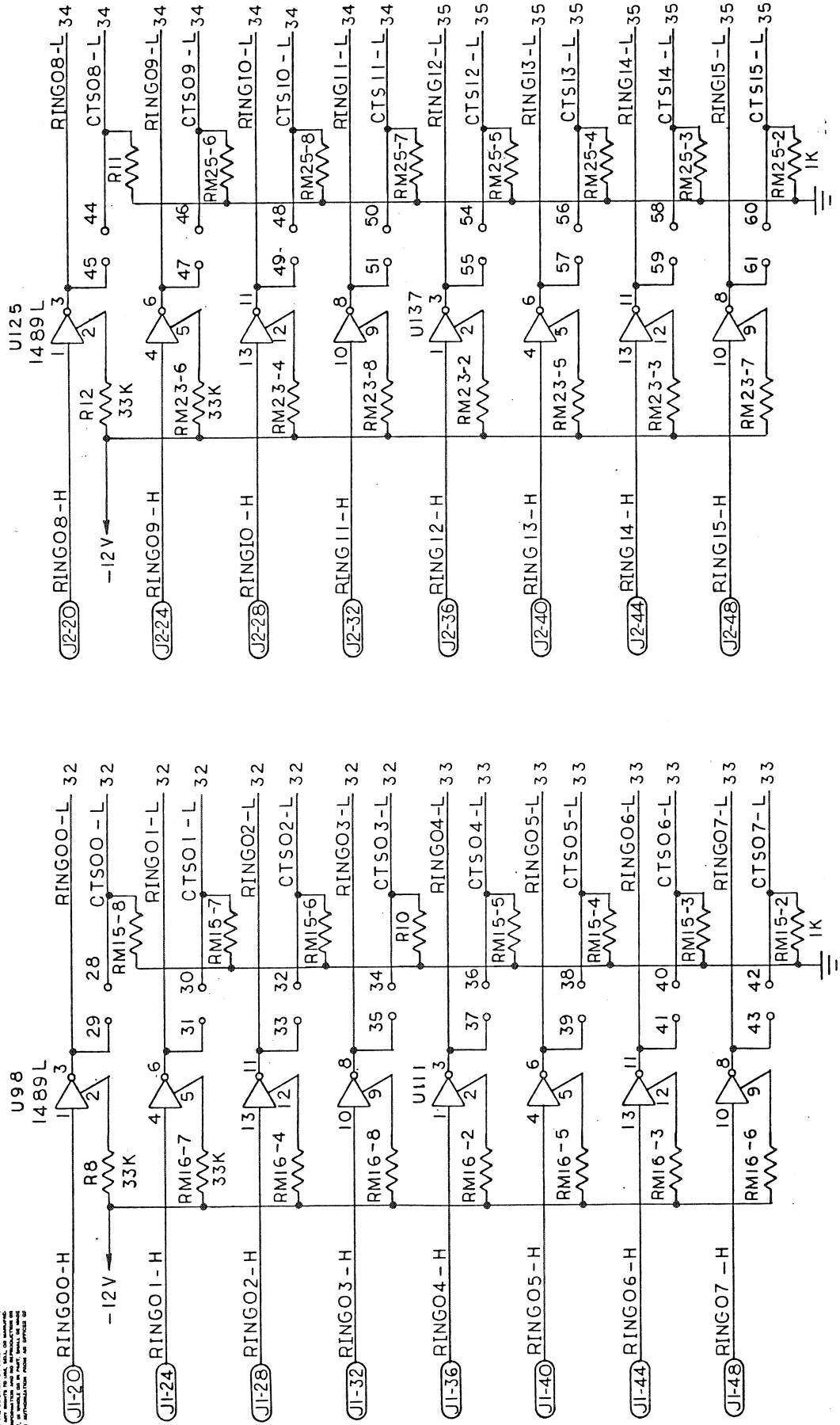


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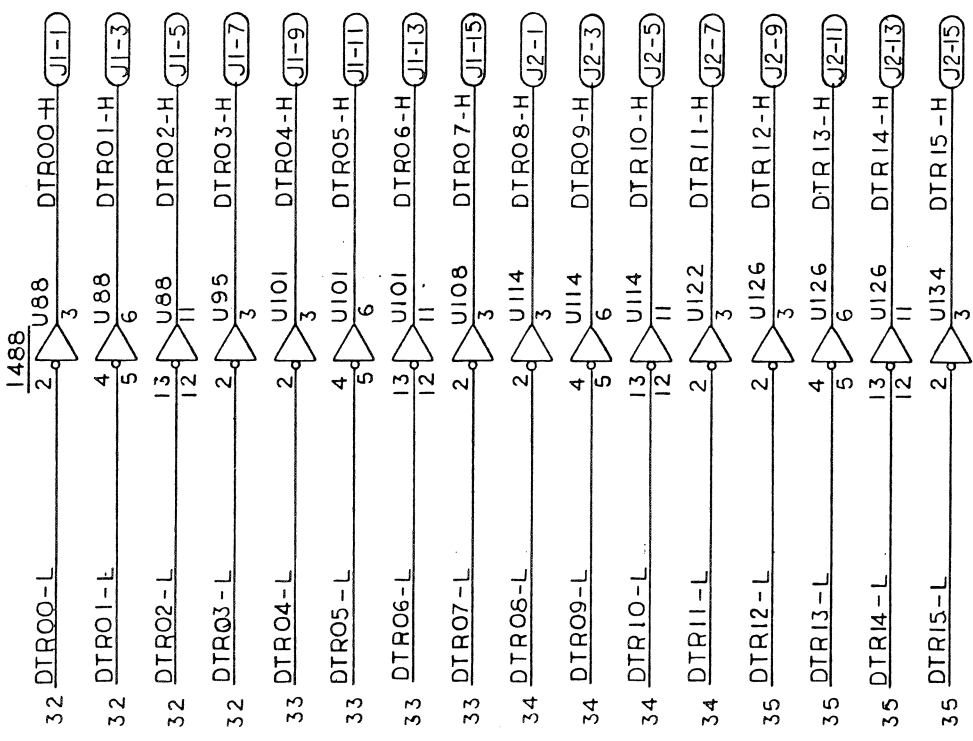
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