D A T A S H E E T

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AIC-33C93C

Enhanced SCSI Bus Interface Controller

adaptec®

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1.0 Features

Note: Change bars indicate document changes between the AIC-33C93B and AIC-33C93C Data Sheets.

- All functions and timings are current with the proposed SCSI-3 Parallel Interface standard X3T9.2/91-010R8, November 10, 1992.
- Implements full 8-bit single-ended SCSI bus features: arbitration, disconnect, reconnect, parity generation and checking on both data ports, soft reset, and synchronous data transfers.
- Includes 48 mA drivers for direct connection to the SCSI bus.
  - Data bus pins ($\overline{SDB}$[0..7] and $\overline{SDP}$) utilize active-negation drivers for improved noise immunity.
  - $\overline{REQ}$ and $\overline{ACK}$ pins have 57mA active-negation drivers to accommodate high-current terminators.
- Includes a high-performance SCSI bus receiver to afford 800 mV (typ) of hysteresis to reject most reflection-induced noise.
- Operates in both initiator and target roles.
- Operates as both a SCAM level one master or a SCAM level two slave.
- Synchronous offset selectable from one to twelve bytes.
- Programmable time-out for selection and reselection.
- SCSI-2 features:
  - Synchronous transfer rates up to 10 Mbytes/s for Fast SCSI transfers; up to 5 Mbytes/s for standard SCSI transfers.
  - Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands support queue tag messages and target routine identify messages.
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Burst data transfers of up to 4096 bytes.
- Data transfer options include polled I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Improved host interface timings to support faster CPUs.
- Single +5 V supply.
- Available in 44-pin chip carrier.
- Low-power CMOS design.

2.0 Description

2.1 General Description

The AIC-33C93C, a CMOS/VLSI device, operates from a single 5 Volt supply and is available in a 44-pin chip carrier. All inputs and outputs are TTL compatible.

The AIC-33C93C is intended for use in systems which interface to the Small Computer System Interface (SCSI) Bus. The AIC-33C93C can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the AIC-33C93C interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor issues a command to the AIC-33C93C to select the desired target. The AIC-33C93C then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying and notifies the host when it has succeeded by generating an interrupt. At this point, the AIC-33C93C is operating in the initiator role. When the peripheral requests a SCSI command from the host, the AIC-33C93C interrupts the host. The host responds to this interrupt by issuing a Transfer Info command and supplying SCSI command bytes to the AIC-33C93C. The AIC-33C93C transfers the SCSI command to the peripheral and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The AIC-33C93C also offers high-level Select-and-Transfer commands which eliminate the interrupt handling otherwise required between each SCSI bus phase.

When the AIC-33C93C is used in a peripheral system, the AIC-33C93C operates primarily in a target role. It interfaces with a local processor and the SCSI bus in this environment just as it does when used in a host adapter. The target-role command set enables the AIC-33C93C to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically.

The AIC-33C93C has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

2.2 *Differences between the AIC-33C93A, AIC-33C93B, and AIC-33C93C*

The AIC-33C93B delivers the same functionality as the AIC-33C93A and incorporates several enhancements to support SCSI-2 and improve system operation and reliability. In most applications, unless configured with the REALLY ADVANCED FEATURES bit in the OWN ID register set, the AIC-33C93B is backwardly compatible to the AIC-33C93A and hence may replace the AIC-33C93A with no modifications to hardware or firmware.

The AIC-33C93C, except for lacking the Translate Address command, is a drop-in replacement for the AIC-33C93B. In addition, it provides commands to implement the SCSI automatic configuration (SCAM) protocol.

The AIC-33C93B and AIC-33C93C products include several improvements to the AIC-33C93A design intended to bolster system performance and reliability:

- To reduce overhead during polled I/O transfers, the AIC-33C93B/C reports the FIFO status via the FIFO FULL/EMPTY bit in the AUXILIARY STATUS register. As its name suggests, this bit reflects the full or empty state of the FIFO depending on the direction of the transfer. If the host is writing data to the FIFO, the AIC-33C93C sets this bit when the FIFO is empty, indicating that the host may write up to twelve bytes to the FIFO without having to poll the DATA BUFFER READY bit before writing each byte. Similarly, when the host is reading data from the FIFO, the AIC-33C93B/C sets this bit when the FIFO is full, indicating that the host may read the DATA register twelve times without polling DATA BUFFER READY before each read.
- To support Fast SCSI transfers without increasing the signal reflection problem, the $\overline{\text{REQ}}$, $\overline{\text{ACK}}$, $\overline{\text{SDP}}$, and SCSI data pins utilize Active Negation Drivers, instead of the open-drain drivers that the AIC-33C93A uses. These drivers actively pull signals up to a high (negation) level instead of relying on the terminators to do so and allow better control of rise times and of the negation level. Active negation drivers, moreover, can source more current to the bus to help the terminators reduce bus reflections.
- To improve system reliability, the AIC-33C93B/C design expands the group of features enabled by configuring the device with the REALLY ADVANCED FEATURES bit set. In addition to features shared with the AIC-33C93A, the AIC-33C93B/C detects and reports violations of the data transfer protocol and unexpected disconnects from the SCSI bus when operating as a target.

The AIC-33C93B and AIC-33C93C also possess various enhancements designed to support SCSI-2:

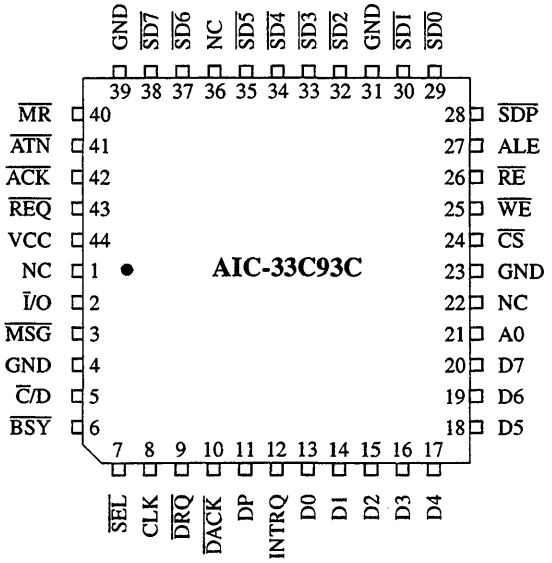
- The combination commands Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive optionally send or receive Queue-tag messages at appropriate points in the SCSI phase sequence. The processor via two bits in the DESTINATION ID register and by way of the QUEUE TAG register supplies information which the first two commands use to generate and check these messages. Wait-for-Select-and-Receive, through the same locations, reports the type of Queue-tag message received, including whether or not the initiator sent a message, and the actual queue tag.
- These commands also support the LUNTAR bit in the Identify message. By setting the corresponding bit in the TARGET LUN register, the host enables the Select-and-Transfer and Reselect-and-Transfer commands to send a target routine Identify message. In the case of Select-and-Transfer, setting this bit also enables the AIC-33C93B/C to accept automatically an Identify message with the LUNTAR bit set. The host also has the option to let the Wait-for-Select-and-Receive command receive a target routine Identify message and proceed to the next phase or to interrupt the host so that it may reject the message when the application does not support target routines.
- The AIC-33C93B/C can perform Fast SCSI transfers. When the AIC-33C93B/C has an input clock between 16 MHz and 20 MHz, by controlling the FAST SCSI SELECT bit in the SYNCHRONOUS TRANSFER register, the host can select between normal synchronous transfers which reach a maximum transfer rate of 5 MB/s and Fast synchronous transfers with a peak rate of 10 MB/s on both the SCSI and host DMA interfaces.

The AIC-33C93C, to support the SCAM protocol, provides a set of new commands consisting of both high-level and low-level commands. This combination simplifies implementation of SCAM features but allows flexibility for non-standard applications.

- The Enable SCAM Tolerant Timings command modifies the interpretation of the Time-out Period register so that the maximum selection time-out is four milliseconds and delays the response to selection so that the AIC-33C93C responds only after the selection phase has persisted for at least four milliseconds. These timings allow a SCAM device to identify other SCAM devices on the bus.
- The Enable SCAM Selection command allows the AIC-33C93C to respond to a SCAM selection.
- The SCAM Select command allows the AIC-33C93C to SCAM select another SCAM device.
- The SCAM Transfer command causes the AIC-33C93C to perform a SCAM transfer cycle.
- The Read SCSI Bus command allows the processor to sample the signals on the SCSI bus for diagnostic purposes or for implementing the SCAM protocol using low-level commands.
- The Set Phase command provides a means for the processor to set the phase lines.
- The Set Data command allows the processor to place a value onto the SCSI data bus.

3.0 AIC-33C93C Pinout

44-pin Chip Carrier



NOTE: PINS IN PARENTHESES ARE FOR TEST PURPOSES ONLY AND SHOULD BE LEFT UNCONNECTED FOR NORMAL CHIP OPERATION.

4.0 Pin Descriptions

4.1 Processor/DMA Interface

All I/O pins have tri-state push-pull drivers unless otherwise noted.

Abbreviation: PWO = Pulsed Wired OR[1]

Table 4-1 CPU / DMA side Pins

Name	I/O	Function
CLK	I	8-20 MHz square wave clock.
$\overline{MR}$	I	Master Reset is an active-low input which causes the AIC-33C93C to enter an idle state and release all SCSI signals.
INTRQ	O	Interrupt Request to the external microprocessor indicates a command completion/termination or a need to service the SCSI interface. Reading the SCSI STATUS register clears this bit.
$\overline{RE}$	I/O	Read Enable is an active-low input used with $\overline{CS}$ to read a register or with $\overline{DACK}$ to access the DATA register in DMA mode. In AIC- Bus mode, it is an output used to read data from a sector buffer.
$\overline{WE}$	I/O	Write Enable is an active-low input used with $\overline{CS}$ to write a register or with $\overline{DACK}$ to access the DATA register in DMA mode. In AIC- Bus mode, it is an output used to write data to a sector buffer.
$\overline{CS}$	I	Chip Select is an active-low input which qualifies $\overline{RE}$ and $\overline{WE}$ when accessing a register. This signal must be inactive during a DMA cycle ($\overline{DACK}$ active in DMA and Burst DMA mode or $\overline{RCS}$ active in AIC- Bus mode).
A0	I	Address pin A0 is used to access the internal registers for non-multiplexed address/data busses. The address of the desired register is loaded into the ADDRESS register during a write cycle with A0=0. The selected register is then accessed when A0=1. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired AIC-33C93C register from the data bus. For indirect addressing, the ALE pin should be grounded. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
$\overline{DACK}$ or $\overline{RCS}$	I/O PWO	DMA Acknowledge is an active-low input used for interfacing to an external DMA controller (e.g. 8237). When $\overline{DACK}$ is low, all bus transfers are to or from the DATA register regardless of the contents of the ADDRESS register. In AIC- Bus mode, this pin, an open-drain output, functions as a RAM Chip Select to the sector buffer. $\overline{RE}$ and $\overline{WE}$ are outputs when $\overline{RCS}$ is active. Regardless of the host DMA mode selected, this pin should be pulled via external circuitry (e.g. a pull-up resistor) to an inactive state and should not be left floating.

Table 4-1 CPU / DMA side Pins (Continued)

1. A Pulsed Wired OR driver actively drives during the signal rise, then turns off the pull-up device to become an open drain driver. An external pull-up is required but may be a large value (~ 10KΩ)

Table 4-1 CPU / DMA side Pins (Continued)

Name	I/O	Function
$\overline{DRQ}$ or DRQ	I/O PWO	Data Request is an active-low output when used for interfacing to an external DMA controller and an active-high input when in AIC- Bus mode. In the first case, $\overline{DRQ}$ and $\overline{DACK}$ form the handshake for the DMA data transfers. In Burst mode, $\overline{DRQ}$ remains low so long as there is data to transfer; in Single-byte DMA mode, $\overline{DRQ}$ toggles for each byte. Since this pin is an open drain output, a pull-up resistor may be required when operating in these modes. In AIC- Bus mode, this pin becomes the DRQ input. A high level on this pin enables the AIC-33C93C to perform burst transfers; a low level inhibits transfers by releasing $\overline{RCS}$ and disabling the $\overline{RE}$ and $\overline{WE}$ outputs.
D7-D0	I/O	Processor data bus.
DP	I/O	Data Parity is used only for checking and generating parity during data transfers.

4.2 SCSI Interface

All pins are bidirectional, and except as noted, they all have open-drain output drivers.

Abbreviation: AND = Active Negation Driver

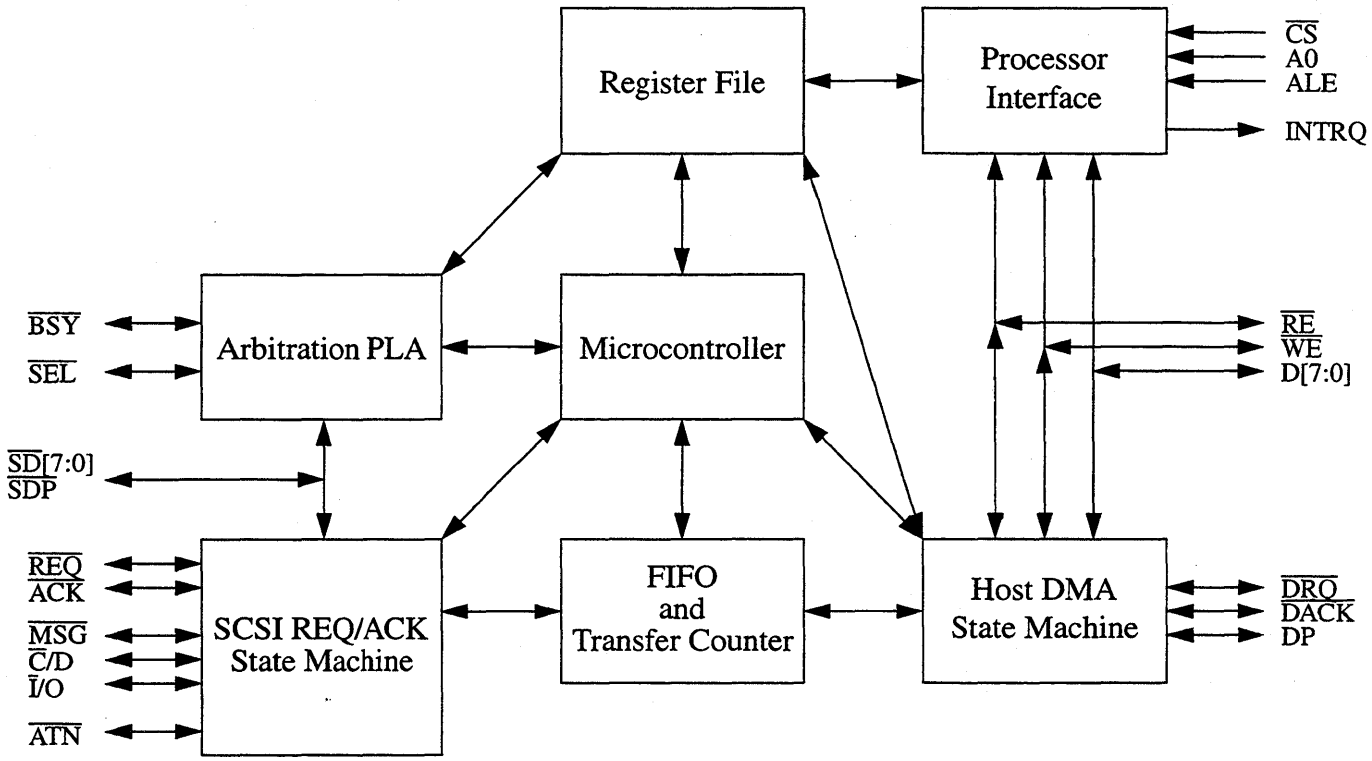
Table 4-1 SCSI Interface Pins

Name	I/O	Function
$\overline{ATN}$	I/O	$\overline{ATN}$ is an output in the initiator role and an input in the target role. Its assertion indicates the ATTENTION condition.
$\overline{REQ}$	I/O AND	$\overline{REQ}$ is an input in the initiator role and an output in the target role. Its assertion indicates the target's request for a transfer.

Table 4-1 SCSI Interface Pins (Continued)

Name	I/O	Function
$\overline{ACK}$	I/O AND	$\overline{ACK}$ is an output in the initiator role and an input in the target role. It indicates an acknowledgment of a data transfer.
$\overline{MSG}$	I/O	$\overline{MSG}$ is an input in the initiator role and an output in the target role. The target asserts this signal when requesting message information.
$\overline{C}$/D	I/O	$\overline{C}$/D is an input in the initiator role and an output in the target role. It specifies whether CONTROL or DATA information is on the SCSI data bus.
$\overline{I}$/O	I/O	$\overline{I}$/O is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an initiator.
$\overline{SD7}$-$\overline{SD0}$	I/O AND	SCSI data bus.
$\overline{SDP}$	I/O AND	SCSI data bus parity.
$\overline{BSY}$	I/O	$\overline{BSY}$ is asserted when the AIC-33C93C is attempting to arbitrate for the SCSI bus or when connected as a target.
$\overline{SEL}$	I/O	$\overline{SEL}$ is asserted when the AIC-33C93C is attempting to select or reselect another SCSI device

5.0 AIC-33C93C Block Diagram



6.0 AIC-33C93C Registers

6.1 Register Map

A0	Addr	R/W	Register Name
0	1F	R	Auxiliary Status Register
0	XX	W	Address Register
1	00	R/W	Own ID Register or CDB Size Register
1	01	R/W	Control Register
1	02	R/W	Timeout Period Register
1	03	R/W	CDB1 Register or SCSI Control Bus Register
1	04	R/W	CDB2 Register or SCSI Data Register
1	05	R/W	CDB3 Register
1	06	R/W	CDB4 Register
1	07	R/W	CDB5 Register
1	08	R/W	CDB6 Register
1	09	R/W	CDB7 Register
1	0A	R/W	CDB8 Register
1	0B	R/W	CDB9 Register
1	0C	R/W	CDB10 Register
1	0D	R/W	CDB11 Register
1	0E	R/W	CDB12 Register
1	0F	R/W	Target LUN Register
1	10	R/W	Command Phase Register
1	11	R/W	Synchronous Transfer Register
1	12	R/W	Transfer Count Register (MSB)
1	13	R/W	Transfer Count Register (2nd)
1	14	R/W	Transfer Count Register (LSB)
1	15	R/W	Destination ID Register
1	16	R/W	Source ID Register
1	17	R	SCSI Status Register
1	18	R/W	Command Register
1	19	R/W	Data Register
1	1A	R/W	Queue Tag Register

NOTES:

1) All unused bits of a defined register are reserved and must be zero.

2) Reading an undefined or unavailable register results in an all-ones data bus output.

3) Register addresses are determined by the ADDRESS register bits AR4 through AR0.

4) When using a multiplexed address/data bus with ALE, the A0 pin is ignored, and the ADDRESS register is loaded with ALE. In this mode, the AUXILIARY STATUS register is mapped at 1F hex.

6.2 Register Descriptions

6.2.1 Auxiliary Status Register

The AUXILIARY STATUS register, a read-only register, contains general status information not directly associated with an interrupt condition. The host may access the AUXILIARY STATUS register at any time except during DMA accesses, i.e. $\overline{\text{DACK}}$ asserted in DMA/Burst mode or $\overline{\text{RCS}}$ asserted in WD Bus mode.

Table 6-1 Auxiliary Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	LCI	BSY	CIP	0	FFE	PE	DBR

Bit 0 DBR DATA BUFFER READY indicates to the processor whether or not the DATA register is available for reading or writing. During a Send command or a Transfer Info command which transmits data over the SCSI bus, the AIC-33C93C sets this bit when ready to take a byte from the host; it resets this bit when the processor writes the byte to the

DATA register. During a Receive command or a Transfer Info command which receives data over the SCSI bus, the AIC-33C93C sets DATA BUFFER READY when it receives a byte and resets the bit when the processor reads the byte from the DATA register.

Bit 1 PE PARITY ERROR status indicates that the AIC-33C93C received a byte with even parity during a transfer. SCSI parity checking is always enabled; host parity checking is enabled via the ENABLE HOST PARITY bit in the OWN ID register. Detection of a parity error will set this bit regardless of the state of the HALT on HOST PARITY ERROR or HALT on SCSI PARITY ERROR bits in the CONTROL register. Issuing a command clears this bit.

Bit 2 FFE FIFO FULL/EMPTY indicates when the FIFO is full or empty depending on the direction of the transfer. (see 6.2.18)

Bit 4 CIP COMMAND IN PROGRESS indicates that the AIC-33C93C is interpreting the last command entered into the COMMAND register. The processor can access the COMMAND register only when this bit is reset.

Bit 5 BSY BUSY indicates that a command is currently executing. When this bit is set, the host has access to the COMMAND register if COMMAND IN PROGRESS is reset, the DATA register if DATA BUFFER READY is set, and the AUXILIARY STATUS register, but it can not access any other registers.

Bit 6 LCI LAST COMMAND IGNORED indicates that the AIC-33C93C ignored a command because the host issued it just prior to or concurrent with a pending interrupt.

Bit 7 INT INTERRUPT PENDING reflects the state of the INTRQ pin. When set, the host should read the SCSI STATUS register to clear INTRQ prior to issuing any commands.

6.2.2 Address Register

The ADDRESS register, a 5-bit write-only register, holds the address of the register to be accessed. Registers in the AIC-33C93C may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In this mode, the falling edge of the ALE signal latches the contents of the host data bus into the ADDRESS register. The $\overline{CS}$ and $\overline{WE}$ or $\overline{RE}$ signals typically follow to access the selected register. When using direct addressing, the A0 pin should be connected to ground, and the AUXILIARY STATUS register is located at address 1F hex.
- Indirect addressing (separate address/data busses). This method, enabled by tying ALE to ground, requires two separate cycles for a register access. The first cycle loads the desired address into the ADDRESS register by writing to the AIC-33C93C with A0=0. The second cycle, with A0=1, then reads or writes the selected register. Every cycle with A0=1 increments the ADDRESS register except when accessing the DATA or COMMAND registers. The AUXILIARY STATUS register is accessed by performing a read with A0=0.

6.2.3 Own ID Register

The OWN ID register stores information which the Soft Reset command uses to configure the device. Following a hardware reset and before issuing any other command, the host must initialize this register and issue the Reset command to set the clock divisor and the SCSI bus ID of the device, to enable various sets of features, and to enable host bus parity checking.

Table 6-2 Own ID Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FS1	FS0	RAF	EHP	EAF	ID2	ID1	ID0

Bits 0-2 IDn SCSI ID bits 0-2 set the SCSI bus ID that the AIC-33C93C uses during arbitration, selection, and reselection.

Bit 3 EAF ENABLE ADVANCED FEATURES, when set, enables the set of functions described in section 7.5.

Bit 4 EHP ENABLE HOST PARITY enables odd parity checking on the host bus. The

PARITY ERROR bit in the AUXILIARY STATUS register will then also indicate parity errors detected on the host bus, and the HALT on HOST PARITY ERROR bit in the CONTROL register will have effect during transfers. When host parity is disabled, the PARITY ERROR bit is not set when a parity error occurs on the host bus, and the HALT on HOST PARITY ERROR bit must be set to zero. NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this control bit.

Bit 5 RAF REALLY ADVANCED FEATURES, when set, enables the features described in section 7.6.

Bits 6-7 FSn FREQUENCY SELECT 0-1 choose the divisor that is applied to the input clock. The divided clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and the corresponding divisors. An incorrect divisor for the input clock may result in violation of SCSI bus timing specifications. NOTE: A clock rate between 10 MHz and 12 MHz should not be used as the resulting SCSI bus clear delay may violate SCSI specifications.

Input Clk Frequency (MHz)	FS1	FS0	Resulting Divisor
8 - 10	0	0	2
12 - 15	0	1	3
16 - 20	1	0	4
xx	1	1	4

6.2.4 CDB Size Register

Table 6-3 CDB Size Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	CS3	CS2	CS1	CS0

Bits 0-3 CSx CDB SIZE bits 0-3 specify the SCSI CDB size for the Select-and-Transfer and Wait-for-Select-and-Receive commands when the command group is not 0, 1, or 5. This mode is enabled only when advanced features have been selected.

6.2.5 Control Register

The CONTROL register consists of option bits which affect the response to parity errors and to the SCSI attention condition, suppress certain interrupts, allow command chaining, and select the mode of DMA transfer.

Table 6-4 Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP The HALT on SCSI PARITY ERROR bit enables the AIC-33C93C to terminate a command if a parity error occurs on an incoming SCSI data byte. Asynchronous transfers check parity on every byte; synchronous data transfers check parity on 4096-byte boundaries in most cases. In the initiator role, the AIC-33C93C responds to a SCSI parity error by leaving the $\overline{ACK}$ pin asserted to inhibit any additional data transfers requests by the target and to facilitate error handling with the target. If Immediate Halts are enabled, a SCSI parity error during a synchronous Receive or Reselect-and-Receive command will abort the transfer before the 4096-byte boundary.

Bit 1 HA The HALT on ATTENTION bit (target mode only) enables the AIC-33C93C to terminate a command if the initiator asserts $\overline{ATN}$. The AIC-33C93C normally tests for the $\overline{ATN}$ condition before the start of a phase and on 4096-byte boundaries during data transfers. If the Immediate Halt feature

is enabled, an the AIC-33C93C will issue an abort command upon recognizing the attention condition. These rules apply to both synchronous and asynchronous transfers.

Bit 2 IDI The INTERMEDIATE DISCONNECT INTERRUPT bit, when set in the initiator role, causes the AIC-33C93C to terminate a Select-and-Transfer command and generate an 85 hex interrupt upon a proper target disconnect. When this bit is reset, the AIC-33C93C continues command execution and does not generate an interrupt. This feature combined with the Resume SAT command provides support for overlapped SCSI operations. In the target role, the INTERMEDIATE DISCONNECT INTERRUPT bit selects combination command execution options.

Bit 3 EDI The ENDING DISCONNECT INTERRUPT bit, when set, delays the 16 hex interrupt which normally follows receipt of the Command-Complete message during a Select-and-Transfer command until after the target disconnects and eliminates the 85 hex interrupt. This bit also enables chaining between certain target-role combination commands to reduce host system overhead.

Bit 4 HHP The HALT on HOST PARITY ERROR bit allows the AIC-33C93C to terminate a Send or Transfer Info command if a parity error occurs on an incoming host data byte. The AIC-33C93C checks for host parity errors according to the same rules it uses when checking for SCSI parity errors. However, a host parity error will not leave the $\overline{ACK}$ signal asserted.

Bit 5-7 DMx The DMA MODE SELECT bits 2-0 select the host bus transfer mode to be used during a Data phase. The following table describes the different DMA modes and specifies the bit settings used to choose each mode:

Table 6-5 DMA Modes

DM2	DM1	DM0	DMA mode selected
0	0	0	**POLLED I/O MODE** or no DMA enabled. The host must poll for DATA BUFFER READY in the AUXILIARY STATUS register and then, depending on the direction of the transfer, read or write the DATA register.
0	0	1	**BURST MODE** or demand-mode DMA. In this mode, the $\overline{DRQ}$ signal will remain active so long as data or space exists in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting $\overline{DACK}$ and pulsing $\overline{RE}$ or $\overline{WE}$ to transfer the data.
0	1	0	**WD-BUS MODE** or Direct Buffer Access (DBA) mode. In this mode, the AIC-33C93C acts as a bus master, and all data access signals reverse their directions. The $\overline{DRQ}$ pin becomes the DRQ input, which when high, enables the AIC-33C93C to drive the buffer control signals. The $\overline{DACK}$ pin becomes the $\overline{RCS}$ output and serves as a chip select for the buffer. The $\overline{RE}$ and $\overline{WE}$ pins become outputs which drive the read and write functions of the RAM buffer. Transfers will continue in a burst manner until the transfer is complete or until the external buffer logic pauses the transfer by negating the DRQ signal. One transfer may occur after DRQ drops and then the $\overline{DACK}$, $\overline{RE}$, and $\overline{WE}$ signals will tristate.
1	0	0	**DMA MODE** or Single-byte DMA. In this mode, a $\overline{DRQ}$/$\overline{DACK}$ handshake occurs for each byte. The DMA controller transfers the byte by asserting $\overline{WE}$ or $\overline{RE}$ while asserting $\overline{DACK}$.

6.2.6 Time-out Period Register

The value in the TIME-OUT PERIOD register specifies the time-out period for selection and reselection attempts and sets the minimum length of a AIC-33C93C-initiated SCAM selection phase.

The time-out period specifies how long the AIC-33C93C will wait for a response, i.e. assertion of the $\overline{BSY}$ signal, after it has begun a reselection or selection phase, i.e. $\overline{SEL}$ asserted and $\overline{BSY}$ negated, before terminating the command. Loading this register with zero disables the time-out feature.

During normal operation, the AIC-33C93C interprets the contents of the Time-out Period register according to the following equation:

$$\text{register value} = \frac{T_{per} \times F_{iclk}}{80}$$

where T_{per} is the time-out period specified in milliseconds and F_{iclk} is the input clock frequency in megahertz.

When SCAM-tolerant timings are in effect, the relation becomes:

$$\text{register value} = \frac{125T_{per} \times F_{iclk}}{54}$$

The SCAM Select command also uses the contents of this register to determine how long the selection phase should last according to the following equation:

$$\text{register value} = \frac{T_{per} \times F_{iclk}}{20}$$

The constants scale the units of the equations, as it is based on an internal microcontroller cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the minimum time requirement is met.

6.2.7 Command Descriptor Block Registers

The COMMAND DESCRIPTOR BLOCK registers store the SCSI command bytes to be sent during Command phase of a Select-and-Transfer command and hold the command bytes received during the Command phase of a Wait-for-Select-and-Receive command.

The Reset command places the microcode revision number in the CDB1 register when really advanced features are enabled.

The Send-Status-and-Command-Complete command uses the contents of the CDB11 register as the returned status and determines the type of the Command-Complete message to send from the contents of the CDB12 register.

6.2.8 SCSI Control Bus Register

Table 6-6 SCSI Control Bus Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BSY	SEL	RAI	RAO	ATN	MSG	C/$\overline{D}$	I/$\overline{O}$

The SCSI Control Bus register will reflect the state of the SCSI bus lines $\overline{BSY}$, $\overline{SEL}$, $\overline{MSG}$, $\overline{C}$/D, $\overline{I}$/O, and $\overline{ATN}$ upon completion of a low-level SCSI I/O command. The bits RAI and RAO indicate the state of $\overline{REQ}$ in and $\overline{ACK}$ out if the AIC-33C93C is in the Connected-as-a-Target state or in the Connected-as-a-SCAM-device state; otherwise, they indicate the state of $\overline{ACK}$ in and $\overline{REQ}$ out. If a bit is set, the corresponding SCSI control line is asserted. If a bit is not set, the internal microcontroller detected that the corresponding SCSI control line was negated, perhaps due to a wired-or glitch. It is the responsibility of the host processor to debounce the signals.

This register is also used to specify the phase to be set by the Set Phase command.

6.2.9 SCSI Data Bus Register

The SCSI Data Bus register, in most cases, will reflect the state of the SCSI data bus upon completion of a low-level SCSI I/O Command. If a bit is set, the corresponding SCSI data bus line is asserted. If a bit is not set, the internal microcontroller detected that the corresponding SCSI data line was negated, perhaps due to a wired-OR glitch. It is the responsibility of the host processor to debounce the signals.

If the Read SCSI Bus command is executed while in the Connected-as-an-Initiator state, this register will contain the value of the data latched on the last $\overline{REQ}$ pulse if the phase was an in phase. If the previous $\overline{REQ}$ pulse occurred during an out phase, the value returned in this register is unpredictable.

The SCAM Transfer and Set Data Bus commands place the contents of this register onto the SCSI data bus. The SCAM Transfer command also uses this register to return the data it latches during the transfer cycle.

6.2.10 Target LUN Register

The TARGET LUN register holds the Logical Unit Number (LUN) and other target status information during various AIC-33C93C commands and sequences.

The Select-and-Transfer commands use the contents of this register and the SOURCE ID register to generate and check Identify messages. In addition, these commands also store the returned status byte from the target in this register. For proper operation of the Select-and-Transfer commands, the host should not set the TARGET LUN VALID bit in this register.

In advanced mode, the Select-and-Transfer commands, in the event of an unexpected reselection, place the logical unit number or the target routine number of a reselecting target in this register. The TARGET LUN VALID and DISCONNECTS OK bits will be zero.

The Wait-for-Select-and-Receive command places a copy of a received Identify message in this register. If the TARGET LUN VALID bit is zero, the initiator did not send a valid Identify message. If the TARGET LUN VALID bit is one, the initiator sent a valid Identify message, and the DISCONNECTS OK bit will then indicate whether or not the initiator has enabled disconnects. The Wait-for-Select-and-Receive command will accept an Identify message with the TARGET ROUTINE bit set only if the host issues the command with the SINGLE BYTE TRANSFER bit in the COMMAND register set.

The Reselect-and-Transfer commands use only the LUN portion and the TARGET ROUTINE bit of this register to generate the Identify message. The TARGET LUN VALID and DISCONNECTS OK bits are not used.

Table 6-7 Target LUN Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TLV	DOK	TRN	0	0	TL2	TL1	TL0

Bit 0-2 TLx Target LUN bit x

Bit 5 TRN Target Routine

Bit 6 DOK Disconnects OK

Bit 7 TLV Target LUN valid

6.2.11 Command Phase Register

The COMMAND PHASE register indicates which phases of a combination command have completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and decide how to respond to it.

When resuming a combination command, the contents of this register specify from which point to restart the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

Table 6-8 Command Phase Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Bit 0-6 CPx Command Phase bit x

6.2.12 Synchronous Transfer Register

The contents of the SYNCHRONOUS TRANSFER register specify the maximum transfer rate and the transfer mode for a SCSI data phase.

For information phases other than a Data phase or when the selected offset is zero (OF3=OF2=OF1=OF0=0), the AIC-33C93C performs asynchronous transfers. A non-zero offset value, which should be twelve or less, selects synchronous data transfers and determines the effective FIFO depth. This value is typically determined through negotiation (as defined in the SCSI standard) with the other SCSI device.

The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI data transfers and, in WD-Bus mode, the transfer period and the width of the $\overline{RE}/\overline{WE}$ strobes for host transfers; for non-data transfers, the transfer period defaults to six periods. The period is defined in terms of the internal clock cycle time, which depends upon the input clock, the divisor selected in the OWN ID register, and the setting of the FAST SCSI SELECT bit.

The FAST SCSI SELECT bit has effect only when operating with an input clock frequency of 16-20 MHz, i.e. the divisor set to 4. Setting this bit enables Fast SCSI transfers, doubling the maximum transfer rate for synchronous transfers. For example, with a 20 MHz input clock and a transfer period of 2, the normal maximum transfer rate would be 5 MB/s; the Fast

SCSI transfer rate would be twice this value or 10 MB/s. The FAST SCSI SELECT bit does not affect the rate of asynchronous transfers.

Table 6-9 Synchronous Transfer Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSS	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0-3 OFx The OFFSET bits specifies the desired offset according to the following table:

OF3	OF2	OF1	OF0	Selected Offset
0	0	0	0	Asynchronous Data Transfers
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	X	X	12

Bit 4-6 TPx The TRANSFER PERIOD bits select the desired transfer period according to the following table:

TP 2	TP 1	TP 0	T_p[a]	REQ/ACK Pulse width
0	0	X	8 Tcyc	4 Tcyc
0	1	0	2 Tcyc	Tcyc
0	1	1	3 Tcyc	Tcyc
1	0	0	4 Tcyc	2 Tcyc
1	0	1	5 Tcyc	3 Tcyc
1	1	0	6 Tcyc	4 Tcyc
1	1	1	7 Tcyc	4 Tcyc

a. T_p is the SCSI/WD Bus Transfer cycle time

Tcyc is the period of the internal data transfer clock. For asynchronous transfers or for synchronous transfers when the input clock frequency is less than 16 MHz, it is calculated as follows:

$$T_{cyc} = \frac{\text{DIVISOR(fromOWNID)}}{2 \times \text{Input Clock Frequency (MHz)}} \quad (\mu s)$$

When the input clock frequency is 16 MHz or greater, the cycle time for synchronous transfers is calculated as follows:

$$T_{cyc} = \frac{2}{(\text{FSS} + 1) \times \text{InputClockFrequency(MHz)}} \quad (\mu s)$$

Bit 7 FSS The FAST SCSI SELECT bit under the conditions mentioned above enables the doubling of the internal clock frequency resulting in a synchronous transfer rate up to 10 MB/s. It applies only to the synchronous transfer phase.

Note: The Fast SCSI mode cycle time applies to synchronous data transfer phase only. For all asynchronous transfer phases including command, message and data, the first equation applies. Also note that if FAST SCSI SELECT mode bit is set, it affects the host side DMA timing as well. See section 9.2 for detailed timings.

6.2.13 Transfer Count Register

The TRANSFER COUNT register, a 24-bit register, stores a preset value for the internal transfer counter. A Send, Receive, or Transfer Info command causes the AIC-33C93C to load this

preset value into the internal transfer counter, which then decrements as each data byte is transferred over the SCSI bus and causes a "successful completion" interrupt when it reaches zero.

Loading the TRANSFER COUNT register with zeros prior to issuing these command or issuing the command with the SINGLE BYTE TRANSFER bit set in the COMMAND register disables the counter function. If the counter is disabled, the Send, Receive, or Transfer Info command will complete when a single byte has been transferred.

In combination commands, this register specifies the number of bytes to be transferred during a Data phase. A zero value indicates the lack of a Data phase.

After the completion of any successful transfer, unless the command was issued in Single Byte Transfer mode (see 6.2.17), the TRANSFER COUNT register will be zero.

When a transfer halts because of an error condition, a SCSI bus phase change, or an abort, the TRANSFER COUNT register will contain the number of bytes NOT successfully transferred over the SCSI bus, including any bytes present in the FIFO at the time of the interruption. The FIFO clearing process may cause the TRANSFER COUNT register to differ with the host DMA controller count because some bytes may have been transferred into the FIFO but not to the SCSI bus.

6.2.14 Destination ID Register

The DESTINATION ID register stores the encoded SCSI bus ID of the device to be selected or reselected. This register also contains control bits that affect the operation of certain combination commands.

Table 6-10 Destination ID Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCC	DPD	DF	TG1	TG0	DI2	DI1	DI0

Bit 0-2 DIx Destination ID bit x

Bit 3-4 TGx The TAG MESSAGE bits select which tag message code to send during Select-and-Transfer and identify which tag message code was received by the Wait-for-Select-and-Receive command. In addition, the Reselect-and-Transfer commands send a Simple-Queue Tag message following the Identify message if either of these bits are set.

TG1	TG0	Message Received or Sent
0	0	No Message
0	1	Simple Queue Tag (20 hex)
1	0	Head Of Queue Tag (21 hex)
1	1	Ordered Queue Tag (22 hex)

Bit 5 DF DISABLE FEATURE, when set, disables Data phase direction checking in advanced mode and inhibits the normally automatic link from Send-Status-and-Command-Complete to the command fetch portion of Wait-for-Select-and-Receive when a Linked-Command-Complete message is sent.

Bit 6 DPD DATA PHASE DIRECTION, when advanced features are enabled (see 7.5), specifies the expected direction of the SCSI Data phase of a Select-and-Transfer command. When this bit is zero, the expected direction is out (to the target), and when this bit is one, the expected direction is in (from the target). An unexpected data phase error will occur if the actual direction does not match the setting of this bit.

Bit 7 SCC SELECT COMMAND CHAIN selects which command will follow a Reselect-and-Transfer command when chaining is enabled. When this bit is zero, a Send-Status-and-Command-Complete command will follow; when this bit is one, a Send-Disconnect-Message command follows.

6.2.15 Source ID Register

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the AIC-33C93C. It also contains bits that enable and control response to selection and reselection.

Table 6-11 Source ID Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ER	ES	DSP	0	SIV	SI2	SI1	SI0

Bits 2-0 SIx SOURCE ID Bits 2-0, valid only if the SOURCE ID VALID bit is set, indicate the SCSI bus ID of the device that selected or reselected the AIC-33C93C.

Bit 3 SIV SOURCE ID VALID is set to one when the AIC-33C93C is selected or reselected and the other SCSI bus device asserted its own bus ID bit during the Selection/Reselection phase. This bit is zero if only the bus ID bit of the AIC-33C93C was asserted.

Bit 5 DSP DISABLE SELECT PARITY, when set, causes the AIC-33C93C to ignore the bus parity when responding to selection or reselection.

Bit 6 ES ENABLE SELECTION, when set, allows the AIC-33C93C to respond to selection by another device on the SCSI bus.

Bit 7 ER ENABLE RESELECTION, when set, allows the AIC-33C93C to respond to reselection by another device on the SCSI bus.

6.2.16 SCSI Status Register

The SCSI STATUS register, a read-only register, holds a value which indicates the cause of the most recent INTRQ assertion. The AIC-33C93C asserts INTRQ whenever a condition occurs that requires intervention by the host. For example,

- the AIC-33C93C has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

After assertion of INTRQ, the contents of this register will not change until the host reads the register or until the AIC-33C93C has been reset.

Table 6-12 SCSI Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0-3 SSx SCSI STATUS bits 0-3 are status qualifiers with meanings that depend upon the upper (4-7) status bits.

Bit 4-7 SSx SCSI STATUS bits 4-7 define the type of interrupt that occurred. The following table describes the various types:

Status Code	Group Meaning
0000 xxxx	The AIC-33C93C is in a reset state.
0001 xxxx	A AIC-33C93C command has completed successfully.
0010 xxxx	A AIC-33C93C command has paused or was aborted.
0100 xxxx	A AIC-33C93C command has been terminated prematurely due to an error or other unexpected condition.
1000 xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the state---Disconnected, Target, Initiator, or SCAM---from which the Status Code can occur. The MCI field refers to the signals that define a SCSI bus information transfer phase: $\overline{MSG}$, $\overline{C}$/D, and $\overline{I}$/O. A bit set to one indicates that the signal is asserted on the SCSI bus; a zero indicates negation. The table below summarizes the meaning of the MCI field:

Table 6-13 MCI Field Meaning

MCI Code	Meaning
000	Data Out Phase
001	Data In Phase
010	Command Phase
011	Status Phase
100	Unspecified Info Out Phase
101	Unspecified Info In Phase
110	Message Out Phase
111	Message In Phase

Table 6-14 Reset State Interrupts

Status Code (hex)	State	Specific Meaning
00	DTIS	33C93 Reset. The device has been hard reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the AIC-33C93C is disconnected.
01	DTIS	AIC-33C93C Reset. The device has successfully completed a Reset command with advanced features enabled. The new state of the AIC-33C93C is disconnected.

Table 6-15 Successful Completion Interrupts

Status Code (hex)	State	Specific Meaning
10	D	A Reselect command completed successfully. The new state of the AIC-33C93C is connected as a target.

Table 6-15 Successful Completion Interrupts

Status Code (hex)	State	Specific Meaning
11	D	A Select command completed successfully. The new state of the AIC-33C93C is connected as an initiator.
12	D	A SCAM Select command completed, and a SCAM master is present on the bus. The new state of the AIC-33C93C is connected as a SCAM device.
13	T	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or Send-Disconnect-Message command completed successfully ($\overline{ATN}$ is not asserted)
14	T	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, or Send-Status-and-Command-Complete command completed successfully ($\overline{ATN}$ is asserted).
15	S	A SCAM Transfer command completed successfully.
16	DI	A Select-and-Transfer command completed successfully.
17	D	A SCAM Select command completed, and a SCAM master did not respond. The state of the AIC-33C93C is Disconnected.
18 +MCI	I	A Transfer Info (non-Message-In phase) command completed successfully. MCI defines the new information type (SCSI bus phase) requested.

Table 6-16 Paused or Aborted Interrupts

Status Code (hex)	State	Specific Meaning
20	I	A Transfer Info (Message In phase) command has paused with $\overline{ACK}$ asserted, giving the host the opportunity to reject the message.
21	DI	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer
22	D	A Select, Reselect, or Wait-for-Select-and-Receive command aborted.
23	T	A Receive or Send command aborted, or a Wait-for-Select-and-Receive aborted because of an error in the Identify message. ($\overline{ATN}$ is not asserted).
24	T	A command aborted or halted due to assertion of $\overline{ATN}$, or a Wait-for-Select-and-Receive aborted because of an error in the Identify message. ($\overline{ATN}$ is asserted).
25	T	A transfer has aborted because of a violation of the data transfer protocol, possibly corrupting the data.
26	DI	An I/O process with a queue tag which did not match the value in the QUEUE TAG register reselected the AIC-33C93C. $\overline{ACK}$ has been left asserted, and the received tag is in the QUEUE TAG register.

Table 6-16 Paused or Aborted Interrupts

Status Code (hex)	State	Specific Meaning
27	DI	A target whose SCSI bus ID does not match the ID in the DESTINATION ID register reselected the AIC-33C93C or the following Identify message did not match the LUN in the TARGET LUN register. $\overline{ACK}$ has been left asserted following the Identify message, and the bus ID and LUN of the reselecting target are available in the SOURCE ID and TARGET LUN registers. This status only occurs when executing a Select-and-Transfer in advanced mode.
28 +MCI	-	Reserved for future use.

Table 6-17 Terminated Interrupts

Status Code (hex)	State	Specific Meaning
40	DTIS	An invalid command was issued
41	TI	An unexpected disconnect occurred. The new state of the AIC-33C93C is disconnected.
42	D	A time-out occurred during a Select or Reselect command. The state of the AIC-33C93C is disconnected.
43	TI	A parity error caused a command to terminate ($\overline{ATN}$ is not asserted). The transfer direction determines whether it was a SCSI or host parity error.
44	T	A parity error caused a command to terminate ($\overline{ATN}$ is asserted). The transfer direction determines whether it was a SCSI or host parity error.

Table 6-17 Terminated Interrupts (Continued)

Status Code (hex)	State	Specific Meaning
45	S	The AIC-33C93C detected the negation of $\overline{C}/D$ at the beginning of a SCAM Transfer command. The new state of the AIC-33C93C is disconnected.
46	DI	A target whose SCSI bus device ID does not match the bus ID set in the DESTINATION ID register has reselected the AIC-33C93C during a Select-and-Transfer command. This interrupt occurs when the AIC-33C93C is not in advanced mode. The state of the AIC-33C93C is connected as an initiator.
47	DI	A status byte with a parity error was received during a Select-and-Transfer command.
48 +MCI	DI	An unexpected information phase was requested. MCI defines the SCSI bus phase requested. This interrupt typically occurs when the phase changes before the Transfer Count reaches zero during a Transfer Info command or when an unexpected phase sequence occurs during a Select-and-Transfer command.

Table 6-18 Service Required Interrupts

Status Code (hex)	State	Specific Meaning
80	D	The AIC-33C93C has been reselected. The new state of the AIC-33C93C is connected as an initiator.

Table 6-18 Service Required Interrupts

Status Code (hex)	State	Specific Meaning
81	D	The AIC-33C93C has been reselected in advanced mode. The Identify message from the target must be read from the DATA register. The $\overline{ACK}$ signal is asserted. The new state of the AIC-33C93C is connected as an initiator.
82	D	The AIC-33C93C has been selected ($\overline{ATN}$ was not asserted). The new state of the AIC-33C93C is connected as a target.
83	D	The AIC-33C93C has been selected ($\overline{ATN}$ was asserted). The new state of the AIC-33C93C is connected as a target.
84	T	The $\overline{ATN}$ signal has been asserted.
85	TI	The target has disconnected. The new state of the AIC-33C93C is disconnected.
86	D	The AIC-33C93C has been SCAM selected. The new state of the AIC-33C93C is connected as a SCAM device.
87	D	The Wait-for-Select-and-Receive command has paused because the incoming CDB is not of a known command group. The host can examine the opcode stored in the CDB1 register to determine the number of command bytes expected. The new state of the AIC-33C93C is connected as a target. (Advanced mode only)
88 +MCI	I	The REQ signal has been asserted while the AIC-33C93C was in an idle initiator state. The information phase type should be examined. MCI defines the information phase (SCSI bus phase) requested.

6.2.17 Command Register

The COMMAND register is used to issue the AIC-33C93C commands. The host should never write to this register when the COMMAND IN PROGRESS or INTERRUPT PENDING bits in AUXILIARY STATUS register are set and should never issue a Level II command when the BSY bit is set.

The SINGLE BYTE TRANSFER bit in the COMMAND register affects the Send, Receive, and Transfer Info commands by disabling the TRANSFER COUNT register and specifying that only one byte is to be transferred. The original contents of the TRANSFER COUNT register are preserved.

The SINGLE BYTE TRANSFER bit also affects the Wait-for-Select-and-Receive command. Normally, this command does not accept as valid an Identify message with the LUNTAR bit set, which occurs when the initiator wishes to communicate with a target routine. Issuing the command with the SINGLE BYTE TRANSFER bit set allows it to accept an Identify message for a target routine.

The SINGLE BYTE TRANSFER bit also selects whether the AIC-33C93C behaves as a level 1 SCAM master (SBT=0) or as a level 2 SCAM slave (SBT=1) when executing a SCAM Select command.

All other commands ignore the setting of this bit.

Refer to the COMMANDS section for a description of the commands and their corresponding command codes.

Table 6-19 Command Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

6.2.18 Data Register

The DATA register provides an interface between the internal twelve byte FIFO and the host. During any type of information phase, the host may access this register with the processor, and during a SCSI Data phase, the host may also access this register through the DMA interface.

The processor, except in one case, should only access the DATA register when the DATA BUFFER READY bit in the AUXILIARY STATUS register is true. The exception occurs when the AIC-33C93C is reselected while operating in **advanced mode: the processor must retrieve the Identify message from the target by reading the DATA register.**

The FIFO FULL/EMPTY bit in the AUXILIARY STATUS register enables the host to avoid polling DATA BUFFER READY in some cases. This bit, when the host writes to the FIFO, acts as a FIFO empty indicator; thus, when set, the host can safely write up to eleven bytes to the FIFO without polling for DATA BUFFER READY between each write. Similarly, when the transfer direction is to the host, the FIFO FULL/EMPTY bit indicates the FIFO full condition, and the processor can safely read twelve bytes from the FIFO without checking for DATA BUFFER READY before each read. In both cases, the host should consider the FIFO FULL/EMPTY bit valid only when DATA BUFFER READY is set.

Two exceptions do exist, however, when writing to the DATA register. First, after the initial setting of the FIFO FULL/EMPTY and DATA BUFFER READY bits in response to a Transfer Info or Send command, the host may write twelve bytes to the FIFO without causing a FIFO overrun.

Second, because the AIC-33C93C splits a Transfer Info command into two separate transfers when responding to a message out phase, the host must not write the last message byte to the DATA register until the AIC-33C93C specifically requests that byte. For instance, if the host wishes to send a (five-byte) Synchronous Data Transfer Request message, the first set of writes should contain only the first four bytes of the message. The host must then poll for DATA BUFFER READY before writing the final byte.

Care should be taken when transferring a large block of data (more than 4 KByte) using FIFO FULL/EMPTY bit to guarantee the maximum burst length. **The AIC-33C93C empties FIFO at every 4,096 byte boundary in order to match the number of bytes transferred on the SCSI bus and the host bus.** If, for example, during the data read (from the SCSI bus) operation, data bytes are in the FIFO but not full at the 4,096 byte boundary, FIFO FULL/EMPTY bit will not be set, and the SCSI transfer halts until these bytes are read out.

The processor normally should not access the DATA register during a Data phase unless the host has selected polled I/O mode by setting all of the DMA MODE SELECT bits in the CONTROL register to zero. In exceptional cases, such as aborting a transfer, the host may wish to switch to polled I/O accesses. In this case, the processor may access the DATA register but must guarantee that the DMA interface is

inactive, i.e. $\overline{DACK}$ inactive in the DMA and Burst DMA modes and $\overline{RCS}$ negated in AIC- Bus mode.

6.2.19 Queue Tag Register

The QUEUE TAG register holds the second byte of the Tag messages associated with the Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands.

The Select-and-Transfer and Reselect-and-Transfer commands send the contents of this register as the second byte of the Tag message during the Tag message out phase.

The Select-and-Transfer and Wait-for-Select-and-Receive commands place the received queue tag byte into this register during the Tag message in phase. The Select-and-Transfer commands, furthermore, compare the received byte with the contents of the register and generate an interrupt in the case of a mismatch.

6.3 Reset Conditions

6.3.1 Hardware Reset

A hard reset, caused by assertion of the $\overline{MR}$ signal, will result in the following conditions:

- The AUXILIARY STATUS register is reset to zero. The INTERRUPT PENDING bit and the INTRQ pin are set when the hardware reset completes.
- The OWN ID register is reset to zero.
- The advanced and really advanced modes are disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI STATUS register is reset to zero.
- The SCSI bus signals are released.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.

The hard reset does NOT affect the following host-accessible registers:

- Registers 01 hex through 15 hex;
- SOURCE ID (16 hex) register bits 0-3;
- COMMAND register (18 hex);

NOTE: The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to reset the AIC-33C93C (for example, logically or the host power-on reset signal with the received SCSI bus reset ($\overline{RST}$) signal). The host may examine the registers that are not affected by the $\overline{MR}$ signal to recover from the SCSI reset condition.

6.3.2 Software Reset

A soft reset, caused by executing the Reset command, will result in the following conditions:

- The DATA BUFFER READY bit in the AUXILIARY STATUS register is reset to zero. The INTERRUPT PENDING bit and INTRQ pin are set when the Reset command is complete.
- The SCSI bus signals are released.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The clock divisor, host parity, and operating mode are configured according to the contents of the OWN ID register.
- The registers 01 hex through 16 hex are reset to zero. The COMMAND register (18 hex) is also reset to zero.
- The SCSI STATUS register is set consistent with the setting of the ENABLE ADVANCED FEATURES bit in the OWN ID register.

7.0 Commands

7.1 Command List

Cmd Code (hex)	Command	Valid States	Level
00	Reset	DTIS	I
01	Abort	DT	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	TIS	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-ATN-and-Transfer	DI	II
09	Select-without-ATN-and-Transfer	DI	II
0A	Reselect-and-Receive-Data	DT	II
0B	Reselect-and-Send-Data	DT	II
0C	Wait-for-Select-and-Receive	DT	II
0D	Send-Status-and-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	DTI	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
20	Transfer Info	I	II
28	Set Phase	S	I
29	Set Data Bus	S	I
2A	Read SCSI Bus	DTIS	I
2C	Enable SCAM Tolerant Timings	D	I
2D	Enable SCAM Selection	D	I
2E	SCAM Select	D	II
2F	SCAM Transfer	S	II

AIC-33C93C states:

D = Disconnected
T = Connected as a target
I = Connected as an initiator
S = Connected as a SCAM device

Command Levels:

I = Level I command
II = Level II command

7.2 AIC-33C93C Command Types

The AIC-33C93C command set consists of two types of commands: Level I and Level II commands. Level I commands, except for the Reset and Abort commands, do not generate interrupts upon their completion; Level II commands always terminate with an interrupt. The host may issue some Level I commands while a Level II command is executing. The AIC-33C93C will ignore a Level II command issued while another Level II command is already executing.

The AIC-33C93C operates in one of four states at any one time: disconnected, connected-as-a-target, connected-as-an-initiator, or connected-as-a-SCAM-device. In each state, the AIC-33C93C recognizes only certain commands as valid, as indicated in the command list above. An attempt to issue a Level II command invalid for the present AIC-33C93C state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

There are two types of Level II commands. 'Simple' Level II commands perform a single operation (e.g. selection) or

single phase (e.g., Command phase). 'Combination' Level II commands combine multiple phases into a single AIC-33C93C command to minimize interrupt overhead.

The initiator combination commands expect the target to follow common SCSI bus phase sequences. Any deviation causes an interrupt.

The ENDING DISCONNECT INTERRUPT and INTERMEDIATE DISCONNECT INTERRUPT bits in the CONTROL register and the SELECT COMMAND CHAIN bit in the DESTINATION ID register enable and control chaining of target combinations command. Linking commands further decreases interrupt overhead by creating longer phase sequences. When using command chaining, the host must initialize all commands in the chain prior to starting the sequence.

7.3 Differentiating between the AIC-33C93 and the AIC-33C93C

The AIC-33C93C incorporates two sets of features, both of which cause it to be incompatible with the original 33C93 design. Upon completion of a hardware reset, both sets of features are disabled. The host enables them by soft resetting the AIC-33C93C with the ENABLE ADVANCED FEATURES and REALLY ADVANCED FEATURES bits in the OWN ID register set appropriately. An advanced mode reset results in a 01 hex being loaded into the SCSI STATUS register instead of the 00 hex which normally results from a reset. This difference gives the host a method to deduce that a AIC-33C93C is installed as opposed to a AIC-33C93.

7.4 Differentiating between the AIC-33C93A, the AIC-33C93B, and the AIC-33C93C

All three devices implement two of the features included in the set of really advanced features. However, the AIC-33C93B and AIC-33C93C implement additional features which result in interrupts which would not occur when using the AIC-33C93A, hence making the two devices incompatible with the AIC-33C93A.

By inspecting the microcode revision, the host can deduce which type of device is installed.

7.5 Advanced Mode Features

7.5.1 Unexpected Reselection

When in normal (33C93) mode, a reselection when idle or a reselection during a Select-and-Transfer command by an target whose ID does not match the one in the DESTINATION ID register causes an interrupt immediately after the reselection handshake finishes. In advanced mode, the AIC-33C93C will continue to the Message In phase to fetch the Identify message. If the AIC-33C93C was idle, the SCSI STATUS register will be set to 81 hex, and **the Identify message will be in the DATA register. This byte must be read out.** If the AIC-33C93C was executing a Select-and-Transfer command, the SCSI STATUS register will be set to 27 hex, and the logical unit number will be in the TARGET LUN register. In both cases, the SOURCE ID register will contain the SCSI bus ID of the reselecting target, and the ACK signal remains asserted so that the Identify message may be rejected if desired.

Any message other than a valid Identify message will result in an unexpected message in phase interrupt. If the unexpected reselection occurs during a Select-and-Transfer command, a parity error will cause an unexpected message in phase interrupt only if the halt-on-SCSI-parity-error feature is enabled. If reselected from an idle state, the AIC-33C93C will halt on a parity error regardless of the setting of the HALT on SCSI PARITY ERROR bit. The host can retrieve the byte with the Transfer Info command.

7.5.2 Unknown SCSI Command Groups

The length of a SCSI Command Descriptor Block is determined by the group code, found in bits 7-5 of the first command byte. The SCSI standard (X3.131-1986) defines Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands respectively as six, ten, and twelve byte commands. All other command groups are undefined by that standard. In normal mode, the AIC-33C93C assumes a length of six bytes for these undefined groups when executing a Select-and-Transfer or Wait-for-Select-and-Receive command. In advanced mode, the AIC-33C93C behaves as follows:

- Select-and-Transfer: When sending a command from an unknown group, the host must load the expected command length into the CDB SIZE register before issuing the Select-and-Transfer command. The AIC-33C93C uses this

value to make sure the correct number of bytes are transferred in the Command phase.

- Wait-for-Select-and-Receive: When receiving the CDB from the initiator, the AIC-33C93C examines the first CDB byte to determine the command group. An undefined group results in an interrupt with the SCSI STATUS register set to 87 hex and the COMMAND PHASE register set to 31 hex. The host may examine the byte, available in the CDB1 register, to determine the TOTAL command length, which it then places into the CDB SIZE register, before resuming the Wait-for-Select-and-Receive command.

  After this interrupt, the AIC-33C93C will only accept a Resume Wait-for-Select-and-Receive, Abort, Disconnect, or Reset command. All other commands are invalid. While the host processes the interrupt, the AIC-33C93C continues to transfer the first six bytes of the SCSI command into its internal FIFO.

7.5.3 Data Phase Direction

Normally during a Select-and-Transfer command, the target solely determines the direction of the Data phase. The AIC-33C93C will not detect a mismatch between this direction and the one expected by the host and will proceed with the transfer. In advanced mode, the AIC-33C93C compares the DATA PHASE DIRECTION bit in the DESTINATION ID register with the state of the I/O signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with an 'unexpected phase' status in the SCSI STATUS register. Setting the DISABLE FEATURE bit in the DESTINATION ID register disables this feature.

7.6 Really Advanced Features

7.6.1 Microcode Revision

The AIC-33C93C will load the revision number of the microcode into the CDB1 register during the reset sequence when really advanced features are enabled.

7.6.2 Immediate Halt

The AIC-33C93C normally checks for parity errors during a synchronous transfer and for the attention condition during both asynchronous and synchronous transfer on 4096-byte boundaries. With really advanced features enabled, the AIC-33C93C during a Receive command continuously checks for these conditions and upon detecting one issues an Abort command.

7.6.3 Data Transfer Protocol Error

The AIC-33C93C, if it detects a possible transfer corruption caused by noise on the $\overline{REQ}$ and $\overline{ACK}$ signals, will abort a Send or Receive command and generate a 25 hex interrupt. The detection scheme can not catch all possible failures due to the nature of the SCSI transfer protocols; however, this feature does provide some protection against data integrity faults.

7.6.4 Unexpected Bus Free Interrupts

The AIC-33C93C will generate either an 85 hex interrupt or a 41 hex interrupt in the event that a glitch on the $\overline{SEL}$ signal causes the device to disconnect from the SCSI bus.

7.7 Level I Commands

7.7.1 Reset (00 hex)

The Reset command initializes the AIC-33C93C according to the contents of the OWN ID register and as described in the RESET CONDITIONS section. The host may issue the Reset command while in any state, forcing the AIC-33C93C into a disconnected state; any command executing at that time will terminate. Upon completion of the Reset command, the AIC-33C93C will generate an interrupt with the SCSI STATUS register containing a 00 hex or a 01 hex depending upon the contents of the OWN ID register at the time of the reset.

7.7.2 Abort (01 hex)

The Abort command is valid in the disconnected and connected-as-a-target states. The effect of the command depends on the current state and the command that is currently executing, as described below:

- Disconnected State: In this state, the Abort command will halt a selection or reselection attempt of a Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command or will halt the Wait-for-Select-and-Receive command before selection. Aborting a selection or reselection attempt before the AIC-33C93C has won arbitration

immediately returns the AIC-33C93C to an idle state and generates a "paused/aborted" interrupt. If the AIC-33C93C has already won arbitration, the Abort command causes the AIC-33C93C to remove the Bus ID bits from the SCSI bus while maintaining assertion of $\overline{SEL}$. If the target does not respond within at least 200 us by asserting $\overline{BSY}$, the AIC-33C93C will go to a Bus Free condition and generate a "paused/aborted" interrupt. If the target does respond within this time period, a "successful completion" interrupt will result instead.

The Abort command, in addition, will terminate a Select-and-Transfer command if the target has disconnected from the bus. The AIC-33C93C will generate an 85 hex interrupt and will be in the Disconnected state. If the target is still connected at the time the Abort command is recognized, the command will be ignored.

- Target State: In this state, the Abort command will terminate a Receive or Send command or the Data phase portion of a Reselect-and-Transfer command. The following rules apply when aborting a transfer:
  - During a Send or Reselect-and-Send command, the AIC-33C93C removes the data request ($\overline{DRQ}$ or the DATA BUFFER READY bit) at an arbitrary time during the abort procedure. The host must NOT service any data request once it has written the Abort command to the COMMAND register until the AIC-33C93C generates an interrupt. Abort processing will not complete until the contents of the FIFO are flushed to the SCSI bus.
  - During a Receive or Reselect-and-Receive command, the host must CONTINUE to service any data request from the AIC-33C93C. Abort processing will not complete until the contents of the FIFO are flushed to the host.

After completion of the Abort command, the TRANSFER COUNT register contains the number of bytes that were not transferred across the SCSI bus. The AIC-33C93C remains in the connected-as-a-target state and will accept any target mode command, including a resume of the aborted command.

7.7.3 Disconnect (04 hex)

The Disconnect command, valid in the initiator, target, and SCAM states, causes the AIC-33C93C to release all SCSI signals and return to the disconnected state, and in the initiator and target states, it will immediately terminate an active Level II command. In the target and SCAM roles, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the initiator role, this command can be used to release the bus following a time-out condition.

7.7.4 Assert ATN (02 hex)

The Assert ATN command, valid only when connected as an initiator, allows the initiator to inform the target that it has a message pending. The target should respond with a Message Out Phase. ATN is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the AIC-33C93C to assert $\overline{ATN}$ automatically prior to the release of $\overline{SEL}$.

7.7.5 Negate ACK (03 hex)

The Negate ACK command causes the AIC-33C93C to release $\overline{ACK}$ which for some reason it has held active. Holding $\overline{ACK}$ active allows the host to respond to information it has just received before the target continues the current phase or proceeds to the next one. The AIC-33C93C, therefore, does not negate $\overline{ACK}$ before generating an interrupt in the following cases:

- after successful completion of a Message-In Transfer Info command;
- after detection of a parity error on any received SCSI information when the HALT on SCSI PARITY ERROR bit is set;
- after unexpected reselection in advanced mode;
- after reception of a save-data-pointer message during a Select-and-Transfer command;
- after reselection by a process with a queue tag which differs from the contents of the QUEUE TAG register; and

- after reception of a status byte with a parity error during a Select-and-Transfer command.

$\overline{ACK}$ negates automatically for all initiator transfers other than Message In transfers. Host parity errors, moreover, do not affect the $\overline{ACK}$ signal.

Before completing a Message In phase, the initiator, upon examining the message, may decide to reject it and send a "MESSAGE REJECT" message to the target or, upon detecting a parity error in the message, may decide to send a "MESSAGE PARITY ERROR" message to the target. Similarly, if a parity error causes a transfer command to terminate, the initiator may wish to send an "INITIATOR DETECTED ERROR" message to the target. In all cases, the initiator signals its intent to send a message by asserting ATN before issuing the Negate ACK command.

7.7.6 Set IDI (0F hex)

The Set IDI command provides support for overlapped SCSI operations in the initiator role. The host may start a SCSI operation with the INTERMEDIATE DISCONNECT INTERRUPT bit reset, allowing the AIC-33C93C to handle target disconnects and reconnects and thus minimizing the interrupt handling overhead. When it wishes to start a second operation, the host issues the Set IDI command so that if the current target disconnects and releases the SCSI bus, the AIC-33C93C will produce an interrupt. The host may now start the second operation without having had to wait for the first operation to complete.

7.7.7 Set Phase (28 hex)

The Set Phase command, valid in the SCAM state, sets the SCSI bus phase pins $\overline{MSG}$, $\overline{C}/D$, and $\overline{I}/O$ as specified by the value in the SCSI Control Bus register. It ignores bits 3 through 7 of the register.

7.7.8 Set Data (29 hex)

The Set Data command, valid in the SCAM state, places the data specified in the SCSI Data Bus register onto the SCSI data bus, with the proper parity.

7.7.9 Read SCSI Bus (2A hex)

The Read SCSI Bus command, valid in all states, returns the state of the SCSI bus control lines and in most cases the SCSI bus data lines in, respectively, the SCSI Control Bus register and the SCSI Data Bus register.

If the Read SCSI Bus command is executed while in the Connected-as-an-Initiator state, the SCSI Data Bus register will contain the value of the data latched on the most recent REQ pulse if the phase was an in phase. If the pulse occurred during an out phase, the value returned in the register is unpredictable.

7.7.10 Enable SCAM Tolerant Timings (2C hex)

The Enable SCAM Tolerant Timings command alters two timings involved during the reselection and selection phases. First, the AIC-33C93C will not respond to a normal SCSI selection or reselection until after a valid selection or reselection phase has lasted for more than four milliseconds. Second, the AIC-33C93C changes its interpretation of the Time-out Period register so that the maximum selection and reselection time-out is on the order of four milliseconds. These timings stay in effect until the AIC-33C93C is reset.

7.7.11 Enable SCAM Selection (2D hex)

The Enable SCAM Selection command enables the AIC-33C93C to respond to a SCAM selection. Resetting the device disables the response to SCAM selection.

7.8 Simple Level II Commands

7.8.1 Select-with-ATN (06 hex)

Select-with-ATN, valid only in the disconnected state, instructs the AIC-33C93C to select a target. Before issuing this command, the host should write the SCSI Bus ID of the target device into the DESTINATION ID register. The Select-with-ATN command causes the AIC-33C93C to begin bus arbitration. If another device selects or reselects the AIC-33C93C during arbitration, the Select-with-ATN command aborts and a "service required" interrupt (8x hex) will occur.

Should the AIC-33C93C win the arbitration, it asserts $\overline{SEL}$ and $\overline{ATN}$, places the target and initiator Bus IDs on the SCSI

data bus, and then negates $\overline{BSY}$. At this time, a time-out sequence begins, its length determined by the value in the TIMEOUT PERIOD register. If the target does not respond with $\overline{BSY}$ within the allotted time, the AIC-33C93C begins a selection abort sequence as described in the Abort command description. If the target has not responded by the end of this sequence, the Select-with-ATN command terminates. If the target responds before the time-out period has elapsed or before the selection abort sequence completes, the AIC-33C93C negates the $\overline{SEL}$ signal, enters the connected-as-an-initiator state, and generates a "successful completion" interrupt.

A successful abort of Select-with-ATN, either through a time-out or through the Abort command, leaves the AIC-33C93C disconnected from the SCSI bus and results in a "paused/aborted" interrupt.

7.8.2 Select-without-ATN (07 hex)

The Select-without-ATN command is identical to the Select-with-ATN command except that $\overline{ATN}$ is not set during the Selection Phase.

7.8.3 Reselect (05 hex)

The Reselect command is identical to the Select-without-ATN command except that the $\overline{I}$/O signal is asserted upon completion of the Arbitration phase. Successful completion of the Reselect command results in the AIC-33C93C being connected as a target.

7.8.4 Receive (10-13 hex)

The four Receive commands---Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out---differ from each other only by the state of the $\overline{C}$/D and $\overline{MSG}$ pins and the type of data that is transferred. These commands, valid only in the target role, correspond to those SCSI information phases where the $\overline{I}$/O pins is not asserted; the type of the Receive command selected determines the state of the $\overline{C}$/D and $\overline{MSG}$ outputs according to the following chart (1=asserted):

Table 7-1 Receive Command

Receive Command Type	Op Code	MSG	C/D	I/O
Command	10	0	1	0
Data	11	0	0	0
Message	12	1	1	0
Unspecified Info	13	1	0	0

A Receive command will complete or terminate under any of the following conditions:

- The host has read the specified number of bytes from the DATA register;
- The AIC-33C93C detects a parity error on one of the received data bytes when Halt-on-SCSI-Parity is enabled;
- The AIC-33C93C detects $\overline{ATN}$ when Halt-on-ATN is enabled;
- The AIC-33C93C detects a transfer protocol error;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The AIC-33C93C resets because of a Reset command or assertion of $\overline{MR}$.

Any conclusion of a Receive command, except those due to a Disconnect command or a Reset, leaves the AIC-33C93C in a connected-as-a-target state and the number of bytes not yet transferred in the TRANSFER COUNT register.

In the case of a Receive Data command, the AIC-33C93C evaluates the contents of the SYNCHRONOUS TRANSFER register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers.

The AIC-33C93C also examines the CONTROL register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

7.8.5 Send (14-17 hex)

The four Send commands---Send Status, Send Data, Send Message, and Send Unspecified Info---like the four Receive commands, differ from each other only by the state of the $\overline{C}$/D and $\overline{MSG}$ pins and the type of data that is transferred. These commands, valid only in the connected-as-a-target state, correspond to those SCSI phases where the $\overline{I}$/O pin is asserted; the type of Send command selected determines the state of the $\overline{C}$/D and $\overline{MSG}$ outputs according to the following chart (1=asserted)

Table 7-2 Send Commands

Send Command Type	Op Code	MSG	C/D	I/O
Status	14	0	1	1
Data	15	0	0	1
Message	16	1	1	1
Unspecified Info	17	1	0	1

A Send command will complete or terminate under any of the following conditions:

- The initiator has acknowledged receipt of the specified number of bytes;
- The AIC-33C93C detects a parity error on one of the received data bytes when Halt-on-Host-Parity is enabled;
- The AIC-33C93C detects $\overline{ATN}$ when Halt-on-ATN is enabled;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The AIC-33C93C resets because of a Reset command or assertion of $\overline{MR}$.

Any conclusion of a Send command, except those due to a Disconnect command or a Reset, leaves the AIC-33C93C in a connected-as-a-target state and the number of bytes not yet transferred in the TRANSFER COUNT register.

In the case of the Send Data command, the AIC-33C93C evaluates the contents of the SYNCHRONOUS TRANSFER register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers. The AIC-33C93C also examines the CONTROL register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

7.8.6 Transfer Info (20 hex)

The Transfer Info command allows the host to send and receive data, command, status, and message information when operating in the connected-as-an-initiator state.

The first $\overline{REQ}$ assertion following connection as an initiator results in a "service required" interrupt. The processor should examine the SCSI STATUS register to determine the type and direction of information transfer requested by the target, and then issue a Transfer Info command in response. The AIC-33C93C will also generate an interrupt each time the target device requests a new type of information transfer phase.

The processor either should initialize the TRANSFER COUNT register prior to issuing this command or issue the command with the SINGLE BYTE TRANSFER bit in the COMMAND register set. Also, if responding to a request for a Data phase, the processor should set the DMA MODE SELECT bits in the CONTROL register and specify the offset and transfer period in the SYNCHRONOUS TRANSFER register before issuing the Transfer Info command.

Behavior of the DATA BUFFER READY status bit during Transfer Info depends upon the direction of the transfer. When the bytes move from the initiator to the target, i.e. an out phase, the DATA BUFFER READY bit is set whenever the FIFO can accept additional data from the host. When the transfer proceeds in the opposite direction, DATA BUFFER READY set indicates that the FIFO contains data available for the host to read.

The Transfer Info command normally terminates or pauses after the specified number of bytes has been sent or received. For a non-Message-In transfer, the AIC-33C93C will generate a "successful completion" interrupt after the target asserts $\overline{REQ}$ to begin a new phase. For a message-in transfer, the AIC-33C93C does not wait for the next phase but instead leaves $\overline{ACK}$ asserted and generates a "paused/aborted" interrupt. The

processor can then assert $\overline{ATN}$ if it intends to reject the message before negating $\overline{ACK}$.

The Transfer Info command may terminate for a number of different reasons which are listed below:

- The host issues a Disconnect command;
- The AIC-33C93C resets in response to the assertion of $\overline{MR}$ or the Reset command;
- The target negates the $\overline{BSY}$ signal;
- The target unexpectedly changes phase, i.e. before the specified number of bytes have been transferred; or
- The incoming data has a parity error and the corresponding halt-on-parity-error bit is set.

The Disconnect command, the hard and soft resets, and the negation of $\overline{BSY}$ will leave the AIC-33C93C in a idle, disconnected state, and in these cases, the value in the TRANSFER COUNT register will not accurately reflect the number of bytes that did not transfer across the SCSI interface. Except for the issuance of the Disconnect command, these occurrences will result in an interrupt.

The AIC-33C93C checks for a parity error on each byte it receives however, for synchronous transfers, the internal microcontroller will not recognize an error until the transfer reaches a 4096-byte boundary. The response to the parity error, furthermore, depends upon the direction of the transfer. If the parity error occurs on received SCSI data, the AIC-33C93C will halt the SCSI interface, leaving $\overline{ACK}$ asserted to halt the target, and generate a "terminated" interrupt once the host has flushed any remaining bytes from the FIFO. Similarly, if the error occurs on data received on the host interface, the AIC-33C93C will halt the host interface and generate a "terminated" interrupt after any bytes remaining in the FIFO are flushed to the SCSI bus; the $\overline{ACK}$ signal, however, will not remain asserted. In both cases, the TRANSFER COUNT register will indicate the number of bytes that did not successfully transfer to or from the target.

If it detects a parity error but the appropriate halt-on-parity-error bit is not set, the AIC-33C93C will indicate the error by setting the PARITY ERROR bit in the AUXILIARY STATUS register but will not terminate the Transfer Info command.

An unexpected phase change will cause a "terminated" interrupt, and as in the case of a parity error, the TRANSFER COUNT register contains the number of bytes yet to be transferred. If an unexpected phase change occurs during a SCSI synchronous transfer, the host should test the PARITY ERROR bit in the AUXILIARY STATUS register, as the phase change most likely occurred before the internal microcontroller recognized the parity error. In the asynchronous case, the AIC-33C93C stops on the byte with the error; therefore, it will always detect a parity error before a phase change in this mode.

Note if this command is used in Message In phase, the COMMAND PHASE register will contain 00 at the completion of its execution.

7.8.7 SCAM Select (2E hex)

The SCAM Select command causes the AIC-33C93C to perform a SCAM selection. The setting of the SINGLE BYTE TRANSFER bit determines whether the AIC-33C93C behaves as a level 2 SCAM slave device (SBT=1) or as a level 1 SCAM master device (SBT=0).

The AIC-33C93C will arbitrate for the bus upon detecting the bus free condition. If acting as a SCAM master, it will arbitrate with an ID; if acting as a SCAM slave, it will arbitrate without an ID. If it loses arbitration, the AIC-33C93C will release all SCSI signals and will wait for the bus free condition before beginning the process over again. Once the AIC-33C93C has won arbitration, it will proceed with SCAM selection.

The length of the SCAM selection phase is determined by the value in the Time-out Period register. (With a 20 MHz input frequency, the value of the Time-out register equals the SCAM selection time in milliseconds.)

The AIC-33C93C will generate an interrupt, upon completion of the selection attempt. If a SCAM master is present, i.e. C/$\overline{D}$ is asserted, the AIC-33C93C will generate a 12 hex interrupt and will be in the Connected-as-a-SCAM-device state.; otherwise, the AIC-33C93C will generate a 17 hex interrupt and will be in the Disconnected state.

7.8.8 SCAM Transfer (2F hex)

The SCAM Transfer command is valid only in the Connected-as-a-SCAM-device state. It causes the AIC-33C93C to perform a SCAM transfer cycle using the data stored the SCSI Data Bus register. The latched data is returned via the SCSI

Data Bus register. For both the data to be sent and the latched data, only the five least-significant bits of the register are valid.

The AIC-33C93C samples $\overline{C}/D$ before performing a transfer, and if it detects that $\overline{C}/D$ has been released, it will terminate the command with a SCAM-Disconnect-Occurred interrupt and release all SCSI lines. The AIC-33C93C will be in the Disconnected state.

If $\overline{C}/D$ is asserted, the AIC-33C93C will perform the transfer and then generate a Successful-SCAM-Transfer-Cycle interrupt. The AIC-33C93C will be in the Connected-as-a-SCAM-device state.

7.9 Combination Level II Commands

7.9.1 Select-and-Transfer (08 and 09 hex)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the AIC-33C93C's internal microprocessor to manage the low-level SCSI protocol. Use of these command may result in as few as one interrupt per SCSI operation. Select-and-Transfer commands, used when in an initiator role, typically consist of at least the following SCSI phases: an Arbitration phase, a Selection phase, a Command phase, a Status phase, and a Command-Complete Message phase. These commands optionally include Data and additional Message In phases.

The Select-and-Transfer commands expect the target to follow a certain sequence of SCSI bus phases, and any deviation from this expected protocol results in a "terminated" interrupt. As the different phases complete, the AIC-33C93C updates the COMMAND PHASE register, so upon termination of the command, the host processor may examine this register to identify the cause of the termination and the state of the SCSI operation.

The two Select-and-Transfer commands differ from each other only by whether or not the AIC-33C93C asserts $\overline{ATN}$ pin during the Selection phase. The ability to assert $\overline{ATN}$ during Selection supports the SCSI message protocol which calls for an Identify Message Out phase following the selection. This is mandatory for SCSI-2 compliance. When executing a Select-with-ATN-and-Transfer command, the AIC-33C93C expects the target to request a Message Out phase immediately following selection, whereas for a Select-without-ATN-and-Transfer command, it expects the target to begin the Command phase once selection completes.

The AIC-33C93C begins the Select-and-Transfer command by arbitrating for the bus and selecting a target just as during a Select command. If the target does not respond before a time-out occurs, the Select-and-Transfer command halts and generates an interrupt.

Failure to complete the Selection phase is also indicated by the fact that the COMMAND PHASE register contains all zeros. If the selection is successful, no interrupt is generated, and the COMMAND PHASE register will be set to a 10 hex.

After completing the Selection phase, the AIC-33C93C begins a Message Out phase if $\overline{ATN}$ has been asserted or a Command phase if not. When the target requests a Message Out phase, the AIC-33C93C responds by automatically sending an Identify message byte, which it generates by exclusive-ORing the contents of the TARGET LUN register with 80 hex if the ENABLE RESELECTION bit in the SOURCE ID register is reset or with C0 hex if the bit is set. After it has sent the Identify message, the AIC-33C93C will set the COMMAND PHASE register to 20 hex.

Normally, bit 6 of the Identify message mirrors the state of the ENABLE RESELECTION bit; however, the host may occasionally wish to allow the AIC-33C93C to respond to a reselection attempt but not enable target disconnects during another SCSI operation. Therefore, when reselections are enabled, setting the DISCONNECTS OK bit of the TARGET LUN register allows the AIC-33C93C to respond to reselection but results in an Identify message byte which does not enable target disconnects.

Following the Identify message out, if bits 3 or 4 of the DESTINATION ID register specify a tag message and if $\overline{ATN}$ is asserted, the AIC-33C93C expects the target to request the first byte of a tag message. It responds to this request by sending the selected tag message code and incrementing the COMMAND PHASE register. The AIC-33C93C now expects the target to ask for the second byte and services this request by sending the contents of the QUEUE TAG register and incrementing the COMMAND PHASE register to 22 hex.

The AIC-33C93C expects a Command phase to follow the Message Out phase or, if $\overline{ATN}$ is not asserted during selection, the Selection phase. The AIC-33C93C obtains the SCSI command from the internal COMMAND DESCRIPTOR BLOCK registers and sends either six, ten, or twelve bytes of command information depending on the first byte of the SCSI command. The Select-and-Transfer commands support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands. The length of any other

command defaults to six bytes unless advanced mode is enabled (see 7.3.1). The COMMAND PHASE register, set to 30 hex before the first Command byte is sent, increments with each byte transferred, so for a twelve-byte CDB command, the COMMAND PHASE register will contain 3C hex when all bytes of the CDB have been transferred.

After the Command phase, the AIC-33C93C anticipates a Data phase if the TRANSFER COUNT register contains a non-zero value, a Status phase if this register contains zero, or, in either case, a Message In phase if the ENABLE RESELECTION bit is set and the DISCONNECTS OK bit is not. The AIC-33C93C assumes a pending disconnection if the target requests a Message In phase. Thus, when enabled, the AIC-33C93C expects to receive either a Save-Data-Pointer message (02 hex) or a Disconnect message (04 hex). If a message byte has a parity error and the HALT on SCSI PARITY ERROR bit is set or if the target sends an unsupported message, the AIC-33C93C will generate a "terminated" interrupt, alerting the processor of this fact and allowing it to retrieve the message byte via the Transfer Info command.

Reception of a correct Save-Data-Pointer message results in a "paused/aborted" interrupt, terminating the Select-and-Transfer command with the COMMAND PHASE register set to 41 hex. The processor can then save the SCSI data pointer before resuming the Select-and-Transfer command.

A Disconnect message, on the other hand, will not cause an interrupt; instead, command execution continues with the COMMAND PHASE register set to 42 hex and with Bus Free as the next expected phase. The AIC-33C93C updates the COMMAND PHASE register to 43 hex when the target actually disconnects and, if the INTERMEDIATE DISCONNECT INTERRUPT bit is set, suspends the Select-and-Transfer command with an 85 hex interrupt. If, however, the INTERMEDIATE DISCONNECT INTERRUPT bit is reset, the AIC-33C93C sits in an idle state, waiting for the target to reconnect. Reselection by the original target generates no interrupt and increments the COMMAND PHASE register to 44 hex; reselection by a different target will cause a "terminated" interrupt. In advanced mode, this interrupt will not occur until the AIC-33C93C has also received the Identify message from the target and placed the logical unit number in the TARGET LUN register.

Following the original target reselection, the AIC-33C93C expects an Identify Message In phase from the target. This single-byte message should be of the binary form: 10r00ttt, where r and ttt match the corresponding bits in the TARGET LUN register. If it does not match, the AIC-33C93C will generate a 4F hex interrupt. The Identify message must be read out from DATA register. Failure to do so may result in the transfer count mismatch in the subsequent data phase. See sections <Angle>6.2.18 on page 19 and <Angle>7.5 on page 22 for more details. Successful completion of this phase results in the COMMAND PHASE register being updated to 45 hex or 70 hex depending upon whether or not a tag message is expected as deduced from the settings of bits 3 and 4 of the DESTINATION ID register.

The target, in the latter case, should send a SIMPLE QUEUE tag message immediately after the Identify message. Upon receiving and validating the message byte, the AIC-33C93C increments the COMMAND PHASE register and awaits the second message byte from the target. When it receives this byte, the AIC-33C93C sets the COMMAND PHASE to 45 hex and then compares the byte to the contents of the QUEUE TAG register. If the two values match, command execution proceeds; if the two values differ, the AIC-33C93C stores the received byte in the QUEUE TAG register, generates a "Different Process Reselected" interrupt (26 hex) and terminates the Select-and-Transfer command.

In case the target send out a non-simple queue tag message (a SCSI Interlocked Protocol violation) or a message other than queue tag, the AIC-33C93C will generates a 4F hex interrupt (unexpected Message In phase - meaning the device is confused). If this happens, a Transfer Info command should be used to read the message one byte at a time, since you do not know the nature and length of the message. It is important to perform an explicit Negate ACK operation before repeating the Transfer Info command, or the bus protocol will deadlock. Once all the messages are received, you can resume SAT command at command phase set at 45 hex, to start data transfer phase.

The AIC-33C93C anticipates a data phase immediately after the Command phase or after successfully receiving the proper messages after reselection. To handle the Data phase, the Select-and-Transfer command effectively performs a Transfer Info command. The contents of the TRANSFER COUNT register determines the number of bytes to transfer; the value in the SYNCHRONOUS TRANSFER register specifies the type and minimum period of the transfers on the SCSI interface; and the DMA MODE SELECT bits in the CONTROL register specify the protocol to follow on the host interface.

Any number of disconnection/reconnection cycles may occur during the data transfer so long as the target follows the

defined message protocol. The COMMAND PHASE register will cycle through the disconnect phases (41-45,70,71) with each disconnection and subsequent reconnection until all of the data has been transferred, at which point it is set to 46 hex. During the data transfer, a disconnection will cause an interrupt regardless of the setting of the INTERMEDIATE DISCONNECT INTERRUPT bit to allow the host to reinitialize the external DMA controller.

The start of the Status phase, assuming the transfer count has reached zero, advances the COMMAND PHASE register to 47 hex. If the status byte has no parity error or if the HALT on SCSI PARITY ERROR bit is not set, the internal microcontroller places the byte in the TARGET LUN register and updates the COMMAND PHASE register to 50 hex. If the byte contains an error, a 47 hex interrupt will occur, and the command will terminate with $\overline{ACK}$ asserted.

The AIC-33C93C expects the target to send a Command-Complete message (00 hex) to indicate that the SCSI operation has completed. Upon receiving this message, the AIC-33C93C sets the COMMAND PHASE register to 60 hex, and if the ENDING DISCONNECT INTERRUPT bit is reset, generates "successful completion" interrupt. The processor should then read the TARGET LUN register to examine the target status. Another interrupt will occur when the SCSI bus goes to the Bus Free state or when the target again asserts $\overline{REQ}$ to begin a new information transfer phase (as in SCSI linked commands). Setting the ENDING DISCONNECT INTERRUPT bit suppresses the "successful completion" interrupt until the target disconnects from the SCSI bus.

Another interrupt will occur when the SCSI bus goes to the Bus Free state or when the target again asserts $\overline{REQ}$ to begin a new information transfer phase (as in SCSI linked commands). Setting the ENDING DISCONNECT INTERRUPT bit suppresses the "successful completion" interrupt until the target disconnects from the SCSI bus.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Select-and-Transfer commands and their meanings relative to command termination:

Table 7-1 Command Termination

Cmd Phase	Meaning
00	No SCSI bus device has been selected. The AIC-33C93C is in the disconnected state.
10	The target has been selected. The AIC-33C93C is now in the connected-as-an-initiator state.
20	An Identify message has been sent to the target.
21	The Tag message code has been sent to the target.
22	The Queue tag has been sent to the target.
30	Command phase has started; no bytes transferred.
3x	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI Bus Free) following a successful transfer of a Disconnect message. The AIC-33C93C is now in the disconnected state.
44	The AIC-33C93C has been reselected by the target with a SCSI bus ID which matches the value in the DESTINATION ID register. The AIC-33C93C is now in the connected as an initiator state.
45	The AIC-33C93C has received an matching Identify message and, if expected, a matching Tag message from the target.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to or from the target during the Data phase.
47	The target has begun a Receive Status phase.
50	The AIC-33C93C has successfully received a Status byte from the target and stored it in the TARGET LUN register.

Table 7-1 Command Termination (Continued)

Cmd Phase	Meaning
60	The AIC-33C93C has successfully received a Command-Complete message from the target.
70	The AIC-33C93C has received an Identify message from the target, and the Logical Unit Number matches the value in the TARGET LUN register. A tag message is expected.
71	The AIC-33C93C has received a Simple-Queue Tag message.

The host processor may resume a Select-and-Transfer sequence by issuing the command when the AIC-33C93C is in the Connect-as-an-initiator state. When resuming the Select-and-Transfer, the AIC-33C93C examines the COMMAND PHASE register to determine where to restart execution of the command. This feature, in conjunction with the INTERMEDIATE DISCONNECT INTERRUPT bit, supports multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the COMMAND PHASE register when resuming a Select-and-Transfer command:

Table 7-2 Select-and-Transfer Command

Cmd Phase	Resuming Select-and-Transfer Cmd
10	Resume after target selection is complete.
20	Resume after Identify message out. Command or message phases are expected; an implied Negate ACK occurs.
22	Resume after Tag message out. Command phase is expected; an implied Negate ACK occurs.
30	Resume when Command phase has begun ($\overline{REQ}$ asserted).
41	Resume after Command phase or after a Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.

Table 7-2 Select-and-Transfer Command (Continued)

Cmd Phase	Resuming Select-and-Transfer Cmd
44	Resume after reselection by a target. An Identify Message In expected.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the Data phase has completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the target; an implied Negate ACK occurs.
70	Resume to receive a Simple-Queue Tag message. An implied Negate ACK occurs.

7.9.2 Reselect-and-Transfer (0A and 0B hex)

The Reselect-and-Transfer commands consist of the Reselect-and-Receive-Data and the Reselect-and-Send-Data commands. These commands cause the AIC-33C93C to execute certain common SCSI bus phase sequences as a target following a Reselection phase. These phases, determined by which command is sent and the setting of the ENDING DISCONNECT INTERRUPT bit in the CONTROL register and the SCC bit in the DESTINATION ID register, are summarized below. Refer to the descriptions of the Send-Status-and-Command-Complete and Send-Disconnect-Message commands for details on those sequences.

- Reselect-and-Receive command, EDI=0, and SCC = don't care:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Completion interrupt.
- Reselect-and-Send command, EDI=0, and SCC = don't care:

- Reselection phase;
- Send Message In;
- Send Data In phase;
- Completion interrupt.

- Reselect-and-Receive command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Status-and-Command-Complete;
- Reselect-and-Send command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Chain to Send-Status-and-Command-Complete;
- Reselect-and-Receive command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Disconnect-Message;
- Reselect-and-Send command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Chain to Send-Disconnect-Message;

The Message In phase consists of an Identify message and, if bits 3 and 4 in the DESTINATION ID register are not both zero, a Simple-Queue Tag message. The commands send the contents of the QUEUE TAG register as the second byte of the Tag message.

If the reselection attempt times out during a Reselect-and-Transfer command, if $\overline{ATN}$ is asserted and the HALT on ATTENTION bit is set, or if a parity error is detected on a incoming data byte and the relevant halt-on-parity-error bit is set, the command will terminate with the appropriate status. In this case, the COMMAND PHASE register will indicate the last successfully completed phase. If these conditions do not occur and all phases complete normally, the command will end with a "successful completion" interrupt at this point if the ENDING DISCONNECT INTERRUPT bit is reset. However, if the bit is set, no interrupt is generated and command chaining occurs (as described above).

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Reselect-and-Transfer commands and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

Table 7-3 Command Phase Register

Cmd Phase	Meaning
00	No SCSI bus device has been reselected. The AIC-33C93C is in the disconnected state.
10	The AIC-33C93C has successfully reselected the initiator. The AIC-33C93C is now in the connected as a target state.
20	The Identify message has been successfully sent to the initiator.
46	The requested data transfer has been completed.

The host processor may resume a Reselect-and-Transfer sequence by issuing the command when the AIC-33C93C is operating in the connected-as-a-target state. When resuming, the AIC-33C93C examines the COMMAND PHASE register to determine where to restart the Reselect-and-Transfer command. This feature in conjunction with the capability to chain to other combination commands allows longer SCSI bus sequences to be performed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Reselect-and-Transfer command:

Table 7-4 Reselect-and-Transfer Command

Cmd Phase	Resuming Reselect-and-Transfer Cmd
10	Resume after initiator reselection is complete; start with Identify Message Out.

Table 7-4 Reselect-and-Transfer Command

Cmd Phase	Resuming Reselect-and-Transfer Cmd
20	Resume after Identify message out; start with data transfer phase. If TRANSFER COUNT is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

7.9.3 Wait-for-Select-and-Receive (0C hex)

The Wait-for-Select-and-Receive causes the AIC-33C93C to idle until it is selected by an initiator, at which time the AIC-33C93C will enter the target mode and automatically request message and command information. Optionally, the AIC-33C93C will then disconnect if it receives a SCSI read command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase and minimizes bus-connect time during SCSI read commands.

If the initiator asserts $\overline{ATN}$ during the Selection phase, the AIC-33C93C first executes an implied "Receive Message Out" command to get the Identify message and the Tag message, if any, from the initiator. The AIC-33C93C stores the Identify message byte in the TARGET LUN register; it encodes the Tag message code into bits 3 and 4 of the DESTINATION ID register and places the queue tag into the QUEUE TAG register. Normally, the Wait-for-Select-and-Receive command rejects an Identify message with the LUNTAR bit set; however, issuing this command with the SINGLE BYTE TRANSFER bit in the COMMAND register set allows the AIC-33C93C to accept an Identify message for a target routine.

The AIC-33C93C executes an implied "Receive Command" following the Selection phase or Identify Message In phase and stores the SCSI command information in the CDB registers. It determines the number of command bytes to request from the SCSI group code in the first byte of the CDB.

At this point, a "successful completion" interrupt normally will occur to allow the local processor to interpret the SCSI CDB. However, by setting the ENDING DISCONNECT INTERRUPT bit prior to issuing a Wait-for-Select-and-Receive command, the host enables the AIC-33C93C to perform an automatic disconnect when it receives a SCSI read command. Thus, when the ENDING DISCONNECT INTERRUPT bit is set and the 1st CDB byte received contains a six, ten, or twelve-byte read command code, the AIC-33C93C will suppress the interrupt and chain to the Send-Disconnect-Message command. Completion of this sequence causes an interrupt and normally indicates a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If the message or command information received from the initiator is invalid, the Wait-for-Select-and-Receive command will be terminated and the appropriate status reported. As usual, the COMMAND PHASE register will indicate which phases of the command completed before the error condition occurred.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Wait-for-Select-and-Receive command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

Table 7-5 Wait-for-Select-and-Receive Command

Cmd Phase	Meaning
00	The AIC-33C93C has not been selected. The AIC-33C93C is in the disconnected state.
10	The AIC-33C93C has been successfully selected by the initiator. The AIC-33C93C is now in the connected-as-a-target state.
20	The AIC-33C93C has received a message byte (Identify) from the initiator. The TARGET LUN register holds the byte.
21	The AIC-33C93C has received a message byte (Tag code) from the initiator. The QUEUE TAG register contains the byte.
22	The AIC-33C93C has received a message byte (Queue Tag) from the initiator. The QUEUE TAG register contains the byte.
30	The AIC-33C93C is ready to begin Command phase. The SCSI bus phase lines and $\overline{REQ}$ have not been asserted.

Table 7-5 Wait-for-Select-and-Receive Command

Cmd Phase	Meaning
31	The AIC-33C93C has transferred one command byte from the initiator. The SCSI STATUS may indicate the need for the host to load the command size into the OWN ID register.
3x	The AIC-33C93C has transferred x command bytes from the initiator.

A "paused/aborted" interrupt in conjunction with command phases 20 and 21 indicate that the respective message byte was not valid. A parity error in the Identify message results in the appropriate interrupt and the COMMAND PHASE register set to 10 hex. This combination allows the host to retry the transfer by merely reissuing the command to resume the operation from the proper phase. A parity error in the other two message bytes results in a command phase of 21 or 22, indicating which byte contained the error.

The host processor may resume the Wait-for-Select-and-Receive command by issuing the command when the AIC-33C93C is operating in the connected-as-a-target state. When resuming this command, the AIC-33C93C examines the COMMAND PHASE register to determine where to restart the Wait-for-Select-and-Receive command. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Wait-for-Select-and-Receive command:

Table 7-6 Wait-for-Select-and-Receive Command

Cmd Phase	Resuming Wait-for-Select-and-Receive Cmd
10	Resume after selection by the initiator is complete. Start with Identify Message Out if ATN is asserted; otherwise, start with Command phase.
20	Resume after a Message Out; check the received message in the TARGET LUN register for a valid Identify message.

Table 7-6 Wait-for-Select-and-Receive Command

Cmd Phase	Resuming Wait-for-Select-and-Receive Cmd
21	Resume after Identify message verified. Start with Tag Message Out if ATN is asserted; otherwise, start with Command phase.
30	Resume after Identify Message Out. Start with Command phase.
31	Resume after the AIC-33C93C has transferred one command byte from the initiator. This resume point is used only when an unknown group code has been detected in advanced mode and the command size has been loaded into the OWN ID register.

7.9.4 Send-Status-and-Command-Complete (0D hex)

The Send-Status-and-Command-Complete command, valid in the target role, combines the Status and the Command-Complete Message phases used to complete a SCSI operation into one command. This command also supports linked SCSI operations by optionally sending a Linked-Command-Complete message after the transferring the status byte. Bits in the CDB12 register corresponding to the standard linked command control bits in the CDB control the choice of Linked-Command-Complete messages.

Before issuing this command, the host loads the status byte into the CDB11 register and the link control bits from the current CDB into the CDB12 register. Note that the bits used by the AIC-33C93C are identical in meaning to the SCSI standard link control bits. Consequently, the host processor may simply load the control byte from the current SCSI command into CDB12 to obtain the correct function. As the command execution progresses, the COMMAND PHASE register will update to indicate the last phase completed.

The possible sequences caused by this command are as follows:

- CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex), followed by a transition to bus free. A "successful completion" interrupt now occurs.

- CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked-Command-Complete message (0A hex). If the DISABLE FEATURE bit in the DESTINATION ID register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. AIC-33C93C command execution proceeds as described for that command.
- CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked-Command-Complete-with-Flag message (0B hex). If the DISABLE FEATURE bit in the DESTINATION ID register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. AIC-33C93C command execution proceeds as described for that command.

The assertion of $\overline{ATN}$ when the HALT on ATTENTION bit is set, the assertion of $\overline{MR}$, or the execution of a Disconnect or Reset command will terminate this command.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Send-Status-and-Command-Complete command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

Table 7-7 Send-Status-and-Command-Complete Command

Cmd Phase	Meaning
00	No operation occurred; typically, $\overline{ATN}$ was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

The host processor may resume the Send-Status-and-Command-Complete command by loading the appropriate value into the COMMAND PHASE register prior to issuing the command. This feature, in conjunction with the capability to chain to other combination commands, allows for a single command to invoke longer SCSI bus sequences.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Send-Status-and-Command-Complete command:

Table 7-8 Send-Status-and-Command-Complete Command

Cmd Phase	Resuming Send-Status-and-Command-Complete Cmd
50	Resume after status phase. Start with command complete message. May chain to command fetch if selected to do so.

7.9.5 Send-Disconnect-Message (0E hex)

The Send-Disconnect-Message command, a target-mode command, instructs the AIC-33C93C to send a Disconnect message and then to deassert the $\overline{BSY}$ signal, causing a logical disconnection of the device from the SCSI bus. Also, a Save-Data-Pointer message will precede the Disconnect message if the host sets the INTERMEDIATE DISCONNECT INTERRUPT bit prior to issuing this command.

The assertion of $\overline{ATN}$ when the HALT on ATTENTION bit is set, the assertion of $\overline{MR}$, or the execution of a Disconnect or Reset command will terminate this command. The following table summarizes the possible values that the COMMAND PHASE register can assume during the Send-Disconnect-Message and their meanings relative to command termination.

Table 7-9 Send-Disconnect-Message Command

Cmd Phase	Meaning
00	No operation occurred; typically, $\overline{ATN}$ was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The AIC-33C93C is now in the disconnected state.

8.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to GND.... -0.5V to +7.0V

Operating temperature.....0 to 70°C

Storage temperature .....-55 to +125°C

Power dissipation 500mW

Input static discharge protection .....2,000V pin to pin

Table 8-1 DC Operating Characteristics

Symbol	Characteristics	Min	Max	Units	Conditions
I_{IL}	Input Leakage		10	µA	$V_{IN} = V_{CC(Max)}$
I_{OL1}	SCSI Pins Output Leakage (Inactive or Power off)		50	µA	$V_{OUT} = V_{CC(Max)}$
I_{OL2}	Output Leakage (Tri-State)		10	µA	$V_{OUT} = V_{CC(Max)}$
V_{IH}	Input High Voltage (All non-SCSI pins)	2.0		V	
V_{IL}	Input Low Voltage (All non-SCSI pins)		0.8	V	
V_{IHS}	SCSI pins Input High Voltage	2.0		V	
V_{ILS}	SCSI pins Input Low Voltage		1.0	V	
V_{IHYS}	Schmitt Trigger Input Hysteresis (All SCSI Pins)	600		mV	700mV typical
$I_{OHS(ON)}$	AND driver pins[a] output high current DC Limit		-20	mA	$V_{OHS} \geq 2.00V$
V_{OLS}	SCSI Output Low Voltage ($\overline{REQ}$, ACK pins) ($\overline{BSY}$,$\overline{SEL}$,$\overline{ATN}$,$\overline{MSG}$,$\overline{C/D}$,$\overline{I/O}$ pins)		0.5 0.5	V V	I_{OL} = 57.0 mA I_{OL} = 48.0mA
V_{OH}	Output High Voltage (All non-SCSI pins)	2.4		V	I_{OH} = -400 µA
V_{OL}	Output Low Voltage (All non-SCSI pins)		0.4	V	I_{OL} = 4.0 mA
V_{CC}	Power Supply Voltage	4.75	5.25	V	0°C ≤ Ta ≤ 70°C
I_{CC}	Supply Current		36	mA	See Below[b]

a. "AND driver pins" include $\overline{REQ}$, $\overline{ACK}$, $\overline{SD7}$ through $\overline{SD0}$, and $\overline{SDP}$.

b. Clock frequency at $1/(tcp)_{min}$, VCC = VCC_{Max}, All Outputs Open, All Inputs at negation level, Ta = 25°C

9.0 Timing Characteristics

Timing characteristics are valid over the entire operating temperature (0 to 70 deg. C) and voltage (4.75 to 5.25 Volts) ranges, and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. All outputs are assumed to have a load capacitance of 50 picofarads. Additionally, open-drain outputs $\overline{DRQ}$ and $\overline{DACK}$ are tested with 10 mA current source pull-ups as loads.

9.1 General

9.1.1 Special Circumstances

The SCSI asynchronous timings, furthermore, assume that the minimum assertion and deassertion times specified for the chosen transfer period have been met. For example, with a transfer period of four, the AIC-33C93C, clocked at 20MHz, acting as a target, will assert $\overline{REQ}$ for at least 200 ns. If the initiator takes more than 200 ns from the leading edge of $\overline{REQ}$ to assert $\overline{ACK}$, then the AIC-33C93C will release $\overline{REQ}$ within 175 ns (9.3.7 talrh). However, if the initiator responds with $\overline{ACK}$ within 200 ns of $\overline{REQ}$, the AIC-33C93C may not meet the specification in order to meet the programmed transfer period.

These timings, moreover, apply only during a burst and assume that the FIFO has space or data available to allow the burst to continue. For instance, 9.3.6 trlal for the first byte of a new phase or of a 4096-byte burst will depend on the time needed by the AIC-33C93C and possibly the host microprocessor to respond to the new phase or to set up for the next 4096-byte block. Clearly, the AIC-33C93C can not meet the 175 ns timing in these situations. In addition, the internal microcontroller controls the handshaking of messages bytes, like the Identify and Disconnect messages, during execution of the combination commands, and again, in these cases, the AIC-33C93C will not meet the asynchronous transfer timings given in the following tables.

9.1.2 SCSI Transfer Phase Timings (How to deal with T_{cyc} specification)

Many of the timing parameters that follow are defined in terms of an internal transfer clock cycle time Tcyc. The cycle time depends upon the input clock frequency, the clock divisor selected, and, for synchronous transfers and if the input clock frequency is 16 MHz or greater, the setting of the FAST SCSI SELECT bit in the SYNCHRONOUS TRANSFER register. Section 6.2.12 provides the details on calculating Tcyc for a given set of these parameters. For normal SCSI transfers, the resulting clock has a frequency from 4 MHz to 5 MHz; for fast SCSI transfers, the frequency falls in the range from 8 MHz to 10 MHz. **For non-transfer timings, such as those pertaining to arbitration and bus release, Tcyc corresponds to the value for normal SCSI transfers.**

When Synchronous transfer is chosen with the FAST SCSI SELECT bit set, the Tcyc parameter not only affects the SCSI bus side, but also the host side DMA timings. Care should be taken at the time of the application design, so the AIC-33C93C synchronous timing will not violate the host side hardware timing requirements.

9.1.3 Table Entry Conventions

Symbol	Characteristic	R/S	Min	Max	Units
♦talbh[a]	A low setup time prior to B high[b]	R[c]	0		µs[d]

a. Symbolic name for the timing. The convention is: t(pin1)(llhlvli)(pin2)(llhlvli) _(mode)
where (pin1),(pin2) are 1 character designation of pins,
(llhlvld) are code for the reference edges;
l: Low going edge
h: High going edge
v: The state becomes valid
i: The state going invalid
(mode) is an associated operation mode of the device for the specification.
e.g., hri = Host Read Indirect,
dw = DMA Write, etc.

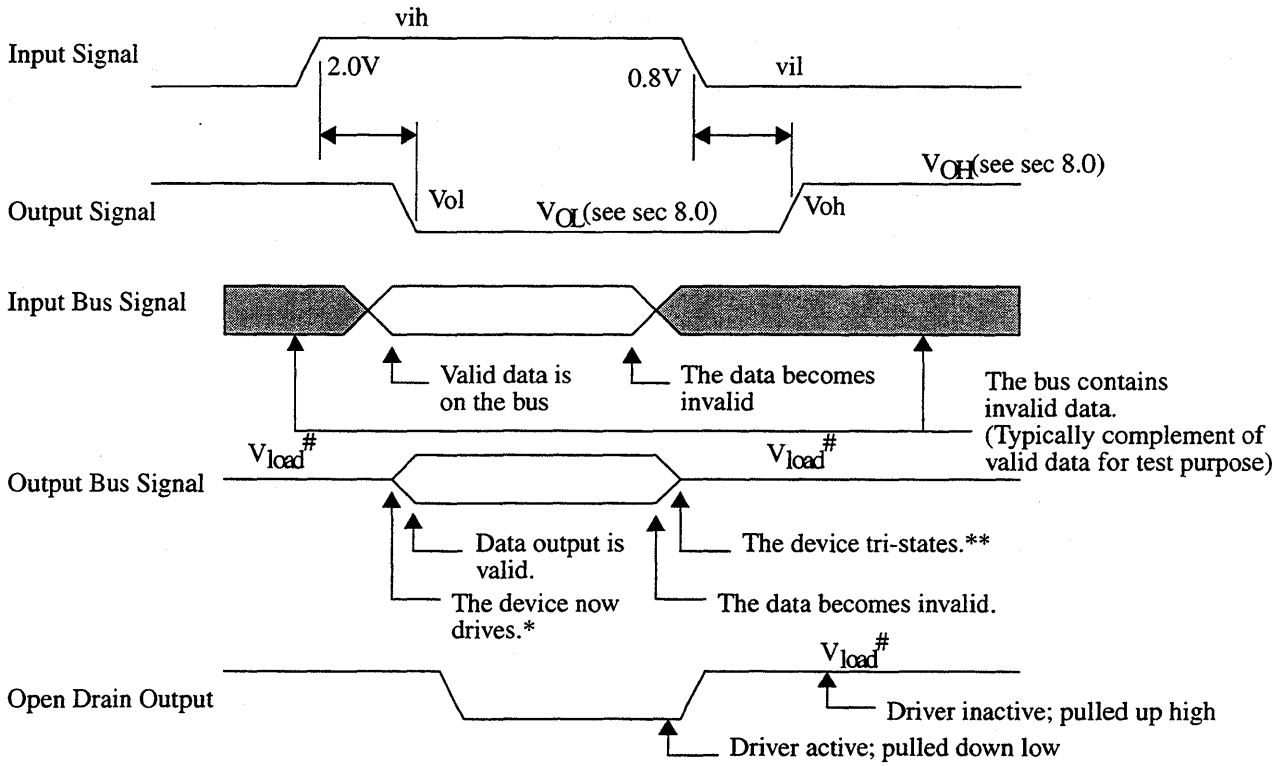
- For example, tclwl_hw might mean "In the Host (direct) Write operation, the time between $\overline{CS}$ pin going low to $\overline{WE}$ pin going low".
- The timings with ♦ mark are only functionally tested. The min/max value are guaranteed by design. Exact timings may depend on a given applications and circumstances.

b. Textual description of the timing. It describes whether the timing is setup time, hold time, input to output, output to input delay time, input or output relative time, etc.

c. Timing classification code: R is a requirement for the part of user, for the device to function correctly.
Minimum specification means "must be at least this much for normal operations".
Maximum specification means "must not take more than this to expect the specified behavior".
S is a guaranteed I/O timing for the device under proper operating condition.
Minimum specification means "it takes at least this much time".
Maximum specification means "it responds within this much time".

d. The timings are specified in either (a) absolute scale (ns, µs, etc.) or (b) clock cycle sliding scale (Tcyc). In type (b) specification, "2-10ns Tcyc" means "2 transfer clock cycle time minus 10 ns". Refer to section 6.2.12 for the definition of Tcyc.

9.1.4 AC Timing Test Conditions



For the AC timing testing purpose, the input signals are overdriven between vil and vih as specified below. The timing are measured at V_L=0.8V and V_H= 2.0V (inputs), V_L = Vol and V_H= Voh (outputs) as specified in the table below.

*The device is defined as "driving" when the voltages moves from Vload (natural hold voltage of the load) by 150mV.

**The device is defined as "tri-stated" if the signal level moves from VOH/VOL by 150mV under specified load condition (C_L, I_{OH}, I_{OL}).

#Vload for all host side pins are at 1.5V, and all SCSI side pins are 3.3V.

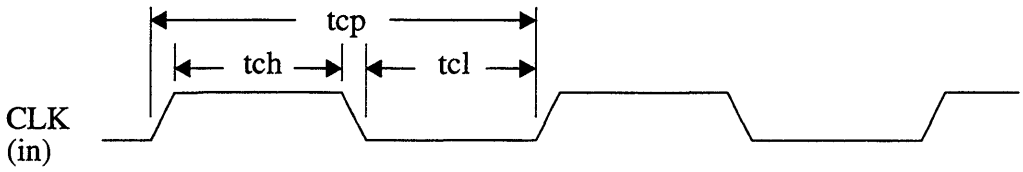
Table 9-1 Test Voltages sorted by Pins

Pins	Vil	Vih	Vol	Voh	Driver Types
$\overline{MR}$, MCK, A0, $\overline{CS}$, ALE	0.4	2.4	-	-	Input only
$\overline{RE}$, $\overline{WE}$, D[7..0], DP, INTRQ	0.4	2.4	0.8	2.0	Full Tri-State Drivers
DRQ, $\overline{DACK}$	0.4	2.4	1.0	2.0	Pulsed Wired OR Drivers
$\overline{ATN}$, $\overline{SEL}$, $\overline{BSY}$, $\overline{C/D}$, $\overline{I/O}$, $\overline{MSG}$	0.4	2.4	0.8	1.6	High Current Open Drain Drivers
$\overline{REQ}$, $\overline{ACK}$	0.4	2.4	1.0	1.8	Active Negation Drivers (57mA)
$\overline{SD}$[7..0], $\overline{SDP}$	0.4	2.4	0.8	1.6	Active Negation Drivers (48mA)

9.2 Processor / DMA Interface

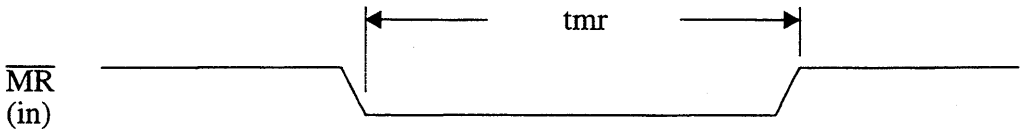
9.2.1 Clock

Symbol	Characteristic	R/S	Min	Max	Units
tcp	Clock Period	R	50	125	ns
tch	Clock high time	R	20		ns
tcl	Clock low time	R	20		ns



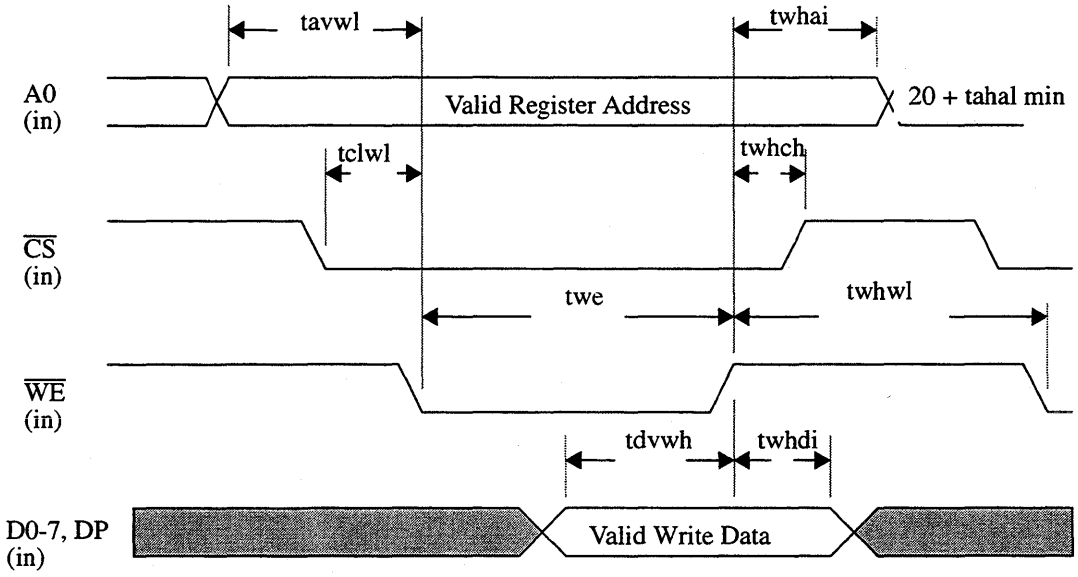
9.2.2 Master Reset

Symbol	Characteristic	R/S	Min	Max	Units
tmr	$\overline{MR}$ pulse width	R	8		tcp



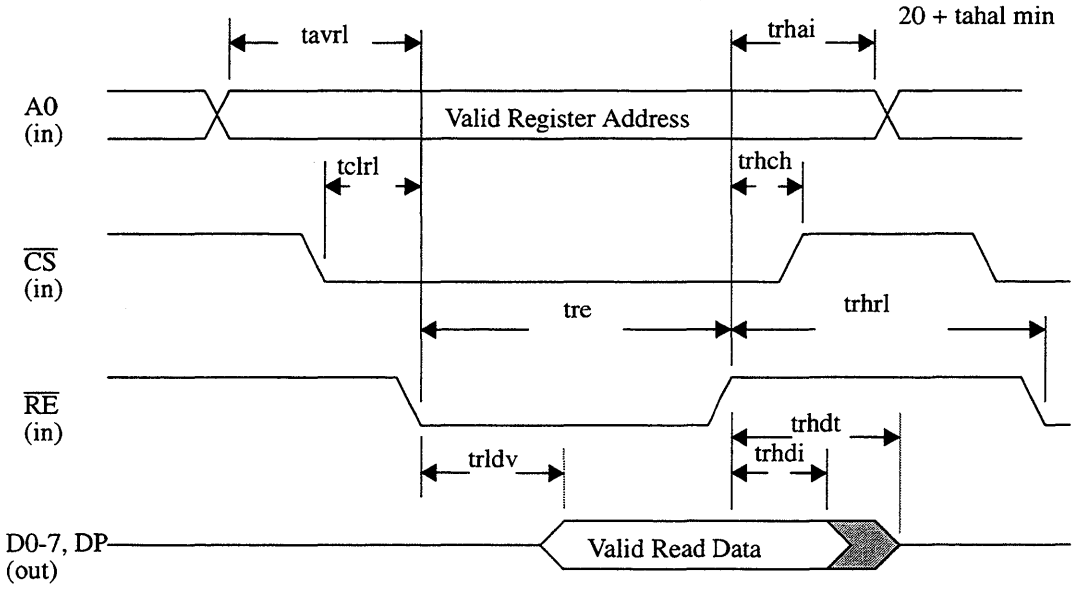
9.2.3 Processor Write (Indirect Addressing)

Symbol	Characteristic	R/S	Min	Max	Units
tavwl_hwi	A0 setup time prior to $\overline{WE}$ low	R	0		ns
tclwl_hwi	$\overline{CS}$ setup time prior to $\overline{WE}$ low	R	0		ns
twe_hwi	$\overline{WE}$ pulse width	R	60		ns
tdvwh_hwi	Data setup time prior to $\overline{WE}$ high	R	35		ns
twhai_hwi	A0 hold time after $\overline{WE}$ high	R	0		ns
twhch_hwi	$\overline{CS}$ hold time after $\overline{WE}$ high	R	0		ns
twhdi_hwi	Data hold time after $\overline{WE}$ high	R	0		ns
twhwl_hwi	$\overline{WE}$, $\overline{RE}$ recovery time after $\overline{WE}$ high	R	40		ns



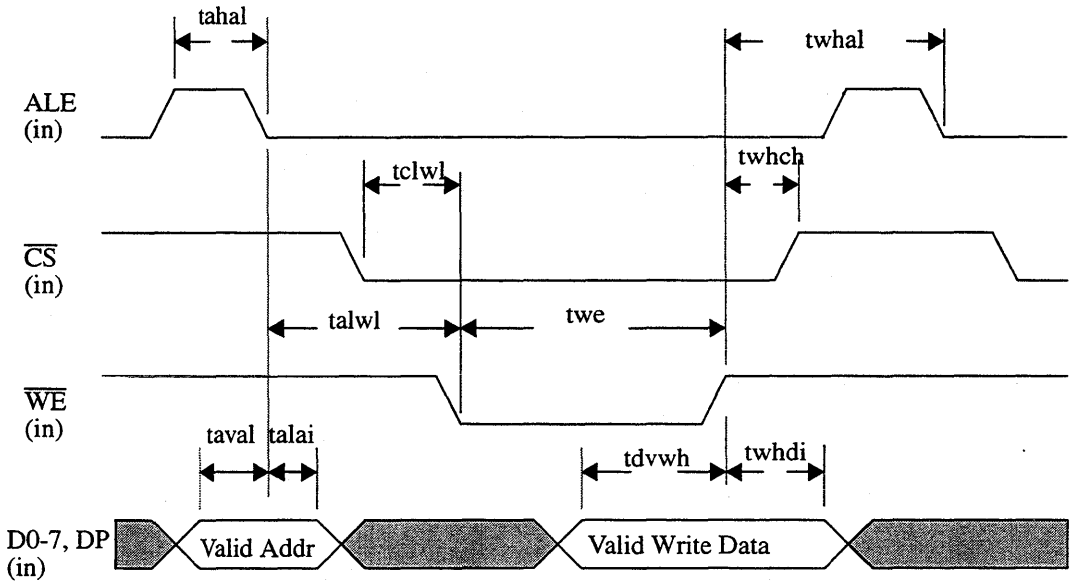
9.2.4 Processor Read (Indirect Addressing)

Symbol	Characteristic	R/S	Min	Max	Units
tavrl_hri	A0 setup time prior to $\overline{RE}$ low	R	0		ns
tclrl_hri	$\overline{CS}$ setup time prior to $\overline{RE}$ low	R	0		ns
tre_hri	$\overline{RE}$ pulse width	R	90	10000	ns
trldv_hri	Data valid delay from $\overline{RE}$ low	S		90	ns
trhch_hri	$\overline{CS}$ hold time after $\overline{RE}$ high	R	0		ns
trhdi_hri	Data output hold time after $\overline{RE}$ high	S	5		ns
trhdt_hri	Data bus tri-state after $\overline{RE}$ high	S		25	ns
trhrl_hri	$\overline{RE}$, $\overline{WE}$ recovery time after $\overline{RE}$ high	R	40		ns
trhai_hri	A0 hold time after $\overline{RE}$ high	R	0		ns



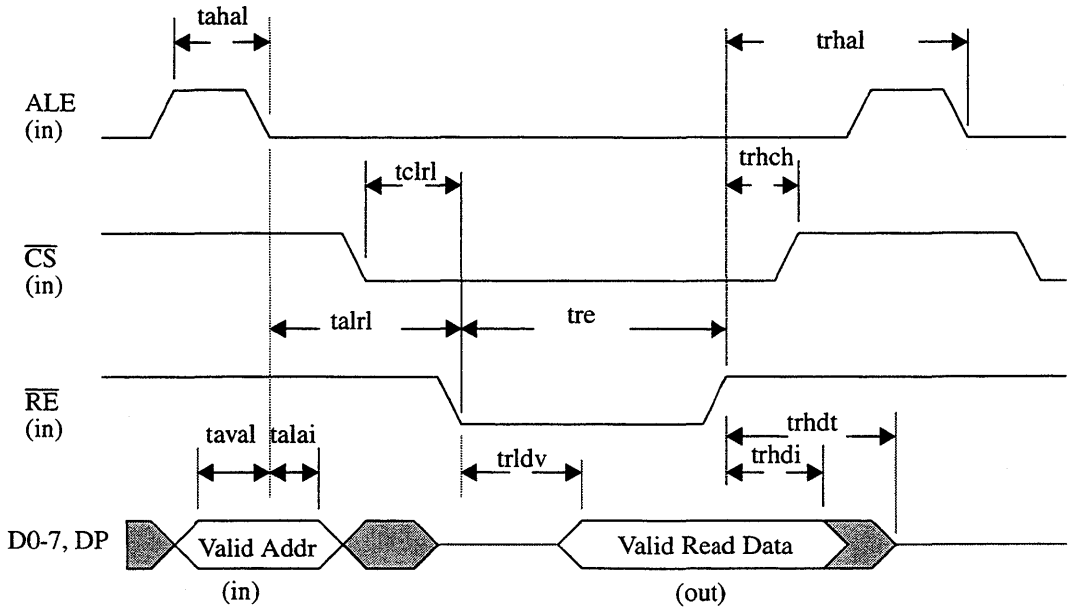
9.2.5 Processor Write (Direct Addressing)

Symbol	Characteristic	R/S	Min	Max	Units
taval_hw	Address Setup time prior to ALE falling edge	R	15		ns
talai_hw	Address hold time after ALE falling edge	R	5		ns
talwl_hw	Recovery time, ALE falling edge to $\overline{WE}$ low	R	40		ns
tclwl_hw	$\overline{CS}$ Setup time prior to $\overline{WE}$ low	R	0		ns
twe_hw	$\overline{WE}$ pulse width	R	60		ns
tdvwh_hw	Data Setup time prior to $\overline{WE}$ high (see 9.2.3 tdvwh_hwi)	R	35		ns
twhch_hw	$\overline{CS}$ hold time after $\overline{WE}$ high	R	0		ns
twhdi_hw	Data hold time after $\overline{WE}$ high	R	0		ns
twhal_hw	Write cycle recovery time after $\overline{WE}$ high	R	tahal + 20 ns min		
tahal_hw	ALE pulse width	R	20	1000	ns



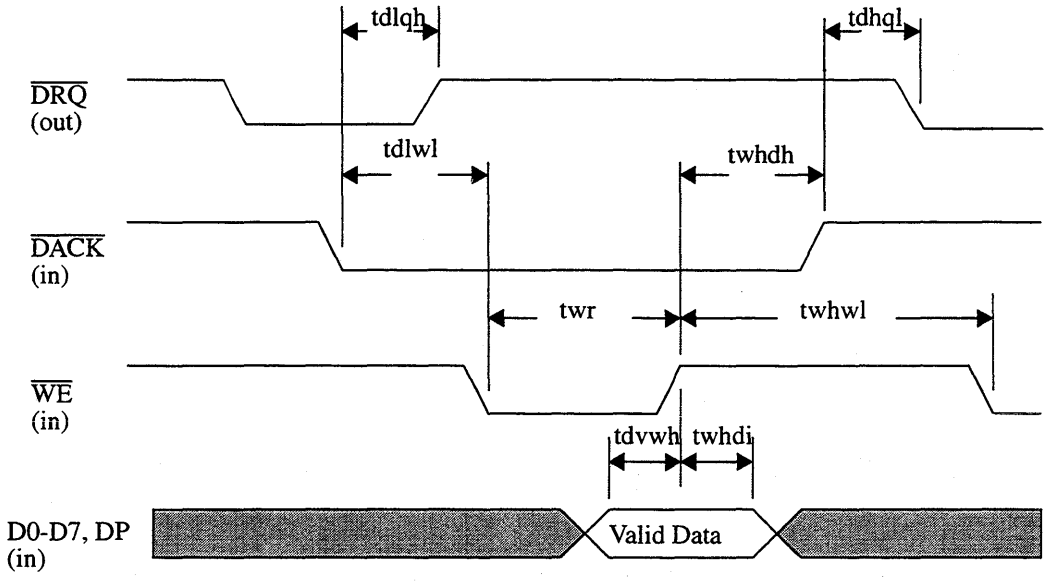
9.2.6 Processor Read (Direct Addressing)

Symbol	Characteristic	R/S	Min	Max	Units
taval_hr	Address Setup time prior to ALE falling edge	R	15		ns
talai_hr	Address hold time after ALE falling edge	R	5		ns
talrl_hr	Recovery time, ALE falling edge to $\overline{RE}$ low	R	40		ns
tclrl_hr	$\overline{CS}$ Setup time prior to $\overline{RE}$ low	R	0		ns
tre_hr	$\overline{RE}$ pulse width	R	90		ns
trldv_hr	Data valid delay from $\overline{RE}$ low	S		90	ns
trhch_hr	$\overline{CS}$ hold time after $\overline{RE}$ high	R	0		ns
trhdi_hr	Data output hold time after $\overline{RE}$ high	S	5		ns
trhdt_hr	Data bus tri-state after $\overline{RE}$ high	S		25	ns
trhal_hr	Read cycle recovery time after $\overline{RE}$ high	R	tahal + 20 ns min		
tahal_hr	ALE pulse width	R	20	1000	ns



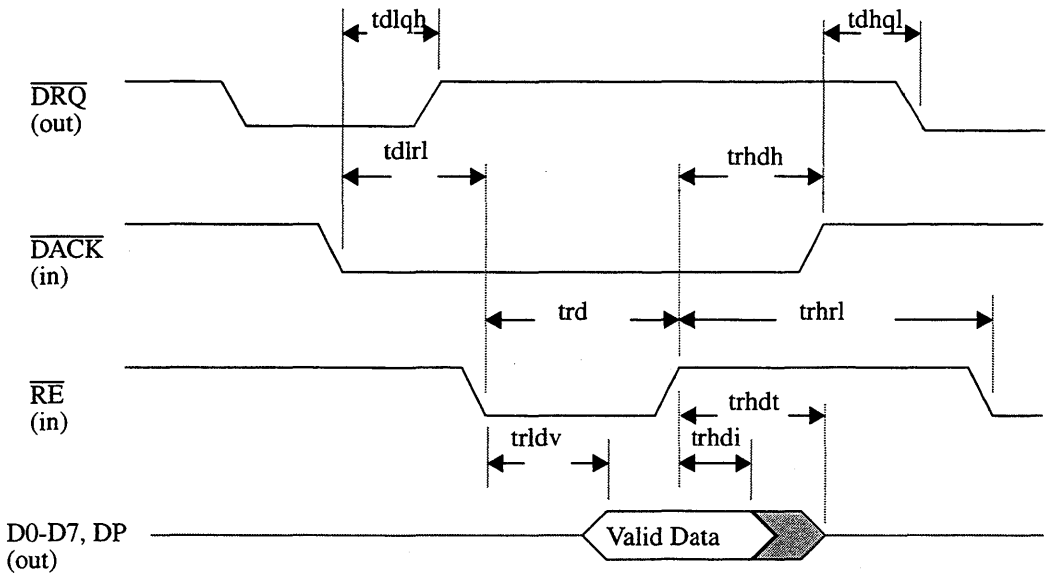
9.2.7 DMA Write

Symbol	Characteristic	R/S	Min	Max	Units
tdlwl_dw	$\overline{DACK}$ input setup time prior to $\overline{WE}$ input low	R	0		ns
tdlqh_dw	$\overline{DRQ}$ output clear time after $\overline{DACK}$ input low	S		75	ns
twr_dw	$\overline{WE}$ input pulse width	R	50		ns
twhwl_dw	$\overline{WE}$,$\overline{RE}$ recovery time after $\overline{WE}$ input high	R	40		ns
tdvwh_dw	Data setup time prior to $\overline{WE}$ input high	R	25		ns
twhdh_dw	$\overline{DACK}$ hold time after $\overline{WE}$ input high	R	0		ns
twhdi_dw	Data hold time after $\overline{WE}$ input high	R	10		ns
♦tdhql_dw	$\overline{DRQ}$ assertion delay after $\overline{DACK}$ negation	S	0		ns



9.2.8 DMA Read

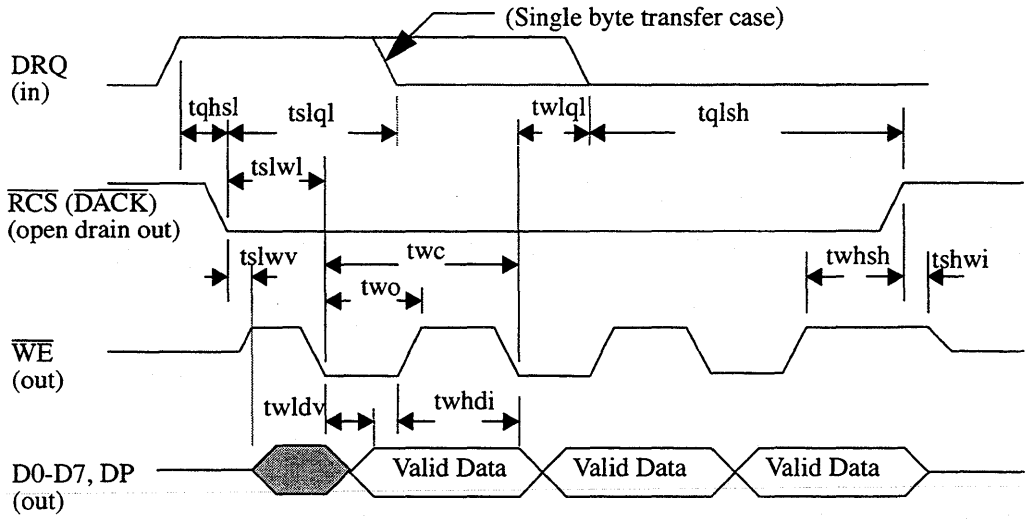
Symbol	Characteristic	R/S	Min	Max	Units
tdlrl_dr	$\overline{DACK}$ setup time prior to $\overline{RE}$ low	R	0		ns
tdlqh_dr	$\overline{DRQ}$ clear time after $\overline{DACK}$ low	S	75		ns
trd_dr	$\overline{RE}$ pulse width	R	50		ns
trhrl_dr	$\overline{WE}$,$\overline{RE}$ recovery time after $\overline{RE}$ high	R	40		ns
trldv_dr	Data valid delay after $\overline{RE}$ low	S		50	ns
trhdh_dr	$\overline{DACK}$ hold time after $\overline{RE}$ high	R	0		ns
trhdi_dr	Data output hold time after $\overline{RE}$ high	S	5		ns
trhdt_dr	Data output tri-state delay after $\overline{RE}$ high	S		25	ns
♦tdhql_dr	$\overline{DRQ}$ assertion delay after $\overline{DACK}$ negation	S	0		ns



9.2.9 WD-Bus Buffer Write

Symbol	Characteristic	R/S	Min	Max	Units
tqhsl_ww	DRQ high to $\overline{RCS}$ low latency	S	0	40	ns
tslwv_ww	$\overline{RCS}$ setup prior to $\overline{WE}$ driving	S	-5	20	ns
two_ww	$\overline{WE}$ output pulse width	S	1 - 10 ns		Tcyc
twc_ww	Write cycle time	S	1		T_p[a]
twldv_ww	$\overline{WE}$ low to Data output valid	S		0	ns
twhdi_ww	Data output hold time after $\overline{WE}$ high	S	10		ns
tqlsh_ww	DRQ low to $\overline{RCS}$ inactive (high impedance) latency	S	8	10	Tcyc
tshwi_ww	$\overline{RCS}$ inactive to $\overline{WE}$ high impedance delay	S		100	ns
twhsh_ww	$\overline{WE}$ clear time prior to $\overline{RCS}$ inactive	S	0		ns
tslwl_ww	$\overline{RCS}$ low setup time prior to $\overline{WE}$ low	S	2 - 40 ns		Tcyc
twlql_ww	DRQ low after $\overline{WE}$ falling edge[b] (DMA throttling)	R	T_p - Tcyc min 2 T_p - Tcyc - 40 ns max		
tslql_ww	DRQ low after $\overline{RCS}$ falling edge (single byte transfer)	R	2 T_p + Tcyc - 85 ns		

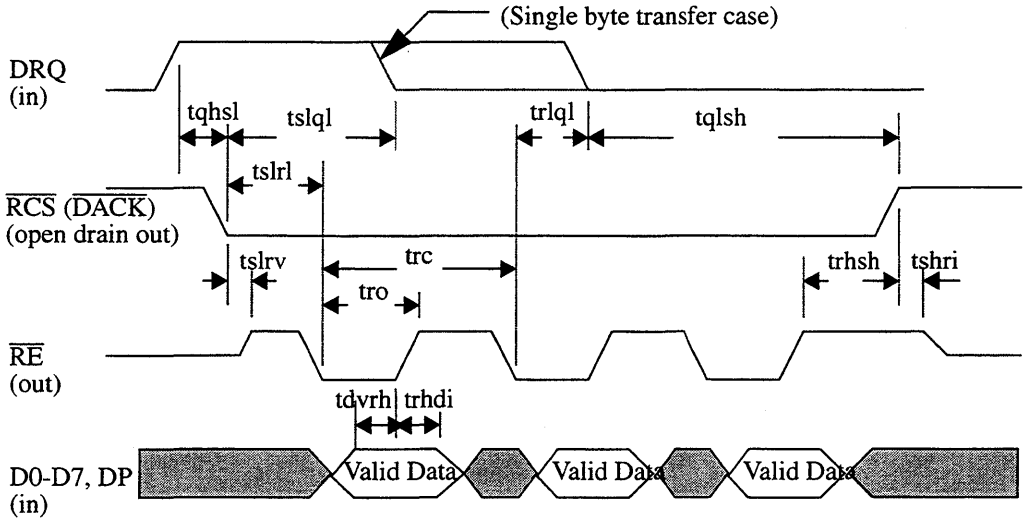
a. T_p is the Bus Transfer Cycle period specified in the SYNCHRONOUS TRANSFER register (see 6.2.12).
b. to guarantee that only one more byte will be transferred.



9.2.10 WD-Bus Buffer Read

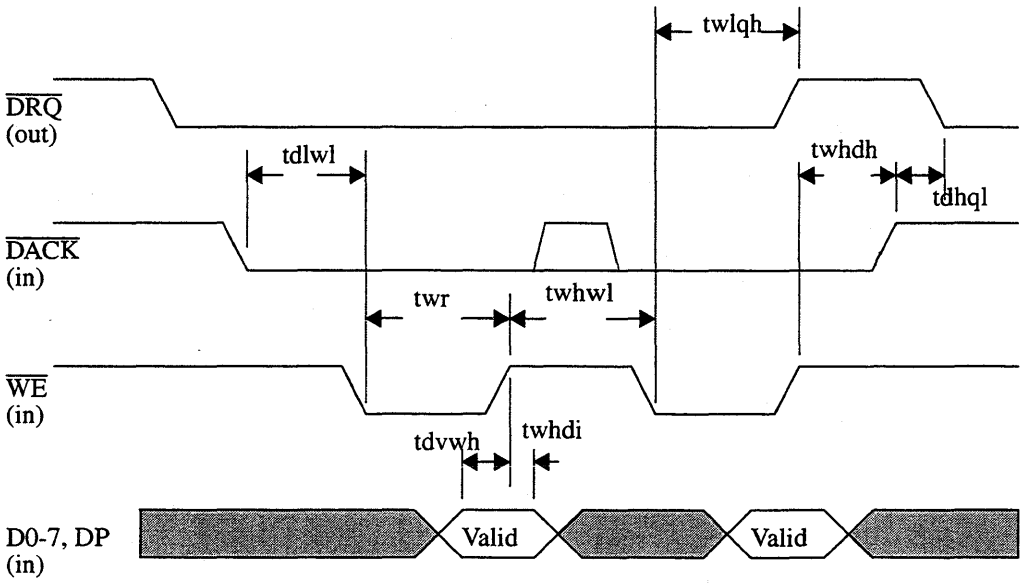
Symbol	Characteristic	R/S	Min	Max	Units
tqhsl_wr	DRQ high to $\overline{RCS}$ low latency	S	0	40	ns
tslrv_wr	$\overline{RCS}$ setup time prior to $\overline{RE}$ driving	S	-5	20	ns
tro_wr	$\overline{RE}$ output pulse width	S	1 - 10 ns		Tcyc
trc_wr	Read cycle time	S	1		Tp
tdvrh_wr	Data setup time prior to $\overline{RE}$ high	R	20		ns
trhdi_wr	Data hold time after $\overline{RE}$ high	R	10		ns
tqlsh_wr	DRQ low to $\overline{RCS}$ inactive latency	S	8	10	Tcyc
tshri_wr	$\overline{RCS}$ inactive to $\overline{RE}$ high impedance delay	S		100	ns
trhsh_wr	$\overline{RE}$ high setup time prior to $\overline{RCS}$ inactive	S	0		ns
tslrl_wr	$\overline{RCS}$ low setup time prior to $\overline{RE}$ low	S	2 - 40 ns		Tcyc
trlql_wr	DRQ low after $\overline{RE}$ falling edge[a] (DMA throttle)	R	Tp - Tcyc min 2 Tp - Tcyc - 40 ns max		
tslql_wr	DRQ low after $\overline{RCS}$ falling edge (single byte transfer)	R	2 Tp + Tcyc - 85 ns		

a. to guarantee that only one more byte will be transferred



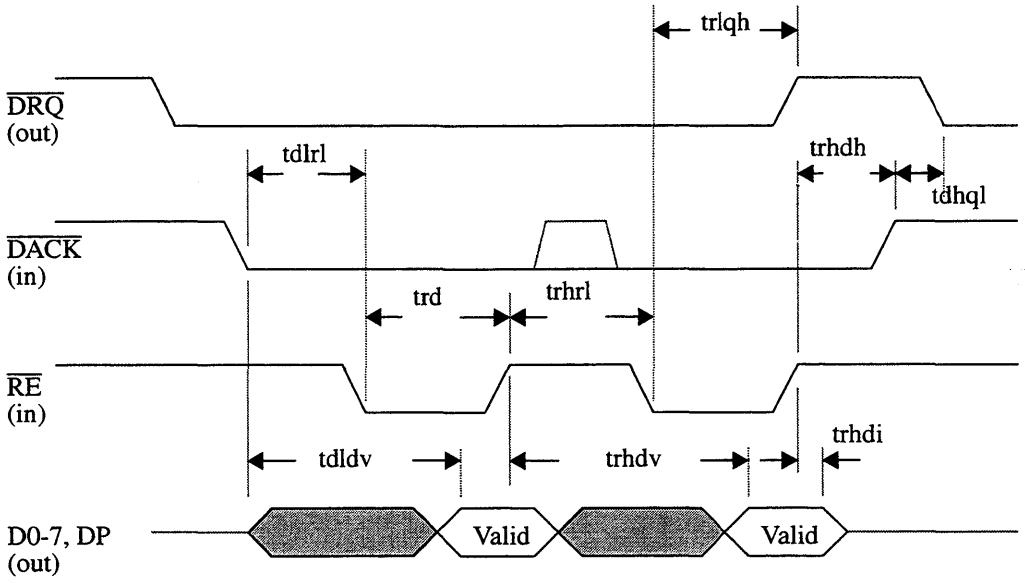
9.2.11 Burst DMA Write

Symbol	CharacteristicCharacteristic	R/S	Min	Max	Units
tdlwl_bw	$\overline{DACK}$ setup time prior to $\overline{WE}$ low	R	0		ns
twlqh_bw	$\overline{DRQ}$ clear time after $\overline{WE}$ falling edge	S		40	ns
twr_bw	$\overline{WE}$ pulse width	R	30		ns
twhwl_bw	$\overline{WE}$ recovery time	R	35		ns
tdvwh_bw	Data setup time prior to $\overline{WE}$ high	R	18		ns
twhdh_bw	$\overline{DACK}$ hold time after $\overline{WE}$ high	R	0		ns
twhdi_bw	Data hold time after $\overline{WE}$ high	R	5		ns
♦tdhql_bw	$\overline{DRQ}$ assertion delay after $\overline{DACK}$ negation	S	0		ns



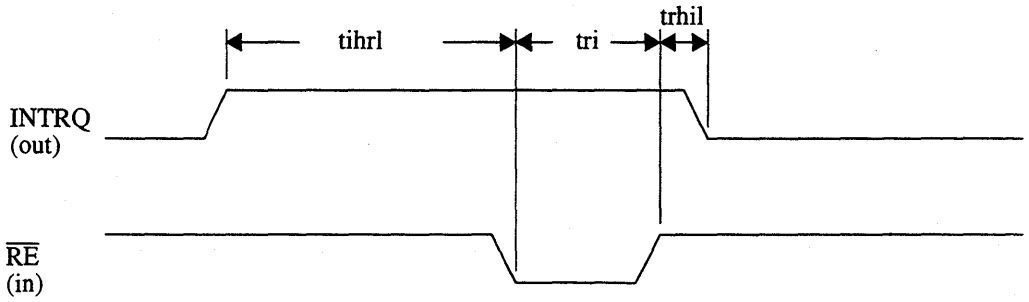
9.2.12 Burst DMA Read

Symbol	Characteristic	R/S	Min	Max	Units
tdlrl_br	$\overline{DACK}$ setup time prior to $\overline{RE}$ low	R	0		ns
tdldv_br	$\overline{DACK}$ low to first byte Data valid delay	S		50	ns
trlqh_br	$\overline{DRQ}$ clear time after $\overline{RE}$ falling edge	S		40	ns
trd_br	$\overline{RE}$ pulse width	R	30		ns
trhrl_br	$\overline{RE}$ recovery time	R	30		ns
trhdv_br	$\overline{RE}$ high to next Data valid delay	S		90	ns
trhdh_br	$\overline{DACK}$ hold time after $\overline{RE}$ high	R	0		ns
trhdi_br	Data output hold time after $\overline{RE}$ high	S	5	40	ns
♦tdhql_br	$\overline{DRQ}$ assertion delay after $\overline{DACK}$ negation	S	0		ns



9.2.13 Interrupt Request

Symbol	Characteristic	R/S	Min	Max	Units
♦tihrl	INTRQ setup time prior to $\overline{RE}$ low	R	0		ns
tri	$\overline{RE}$ pulse width	R	90	10000	ns
trhil	INTRQ clear time after $\overline{RE}$ high	S	0	100	ns



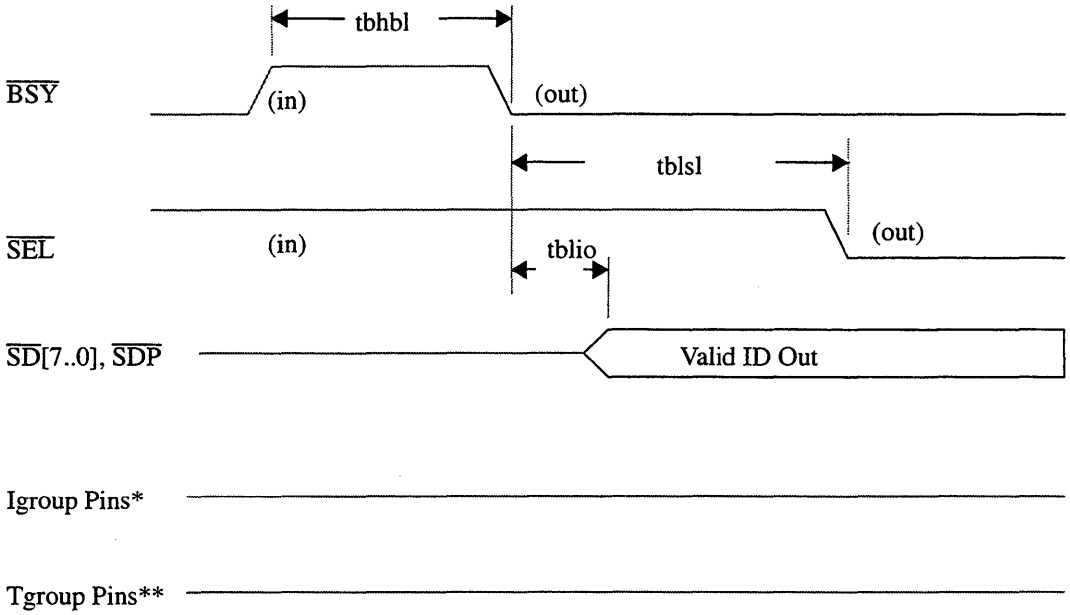
NOTE: This read cycle signifies a read from the SCSI STATUS register.

9.3 SCSI Interface

9.3.1 Arbitration Won

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tbhbl	$\overline{BSY}$, $\overline{SEL}$ input negation to BSY out assertion	S	12	16	Tcyc	1.2 µs min
tblio	$\overline{BSY}$ out assertion to Bus ID out	S		3	Tcyc	-
tblsl	$\overline{BSY}$ output assertion to $\overline{SEL}$ out assertion	S	2.4	&	µs	2.4 µs min

& These timings are microcode driven; exact timing may vary depending on the circumstances.



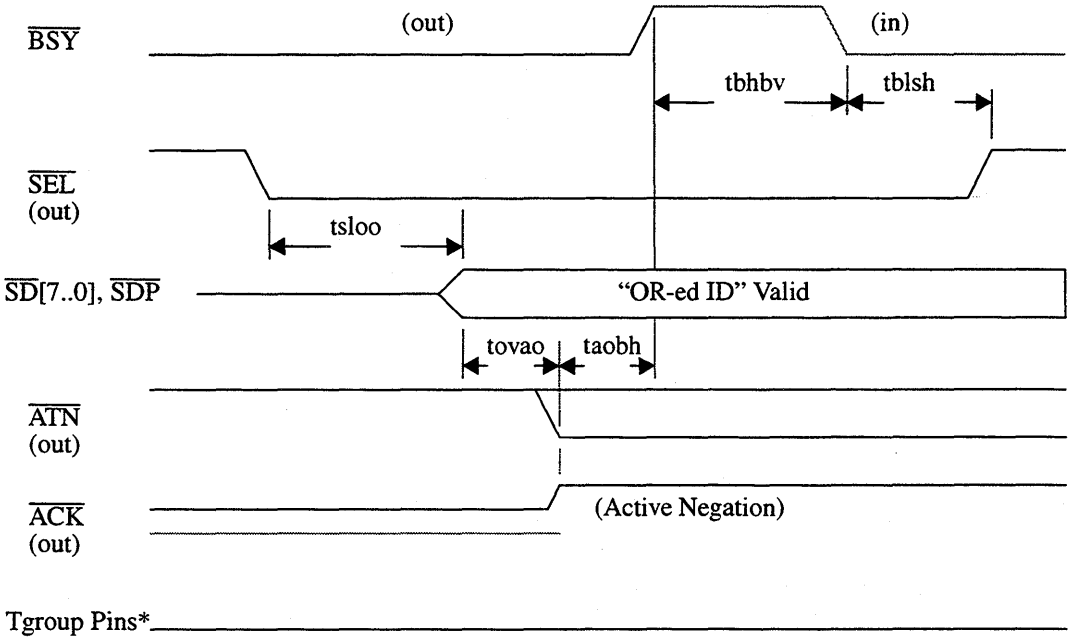
*Igroup Pins are driven by the initiator; includes $\overline{ATN}$, $\overline{ACK}$

**T group Pins are driven by the target; includes $\overline{I}$/O, $\overline{C}$/D, $\overline{MSG}$, $\overline{REQ}$

9.3.2 Selecting a Target (As an Initiator)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tsloo	$\overline{SEL}$ out assert to "OR-ed ID" out valid	S	1.2		µs	1.2 µs min
tovao	"OR-ed ID" out valid to $\overline{ACK}$, $\overline{ATN}$ out	S	100	&	ns	0 ns min
taobh	$\overline{ACK}$, $\overline{ATN}$ out valid to $\overline{BSY}$ out negation	S	100	&	ns	90 ns min
tbhbv	$\overline{BSY}$ out negation to $\overline{BSY}$ in assertion	R	400		ns	400 ns min 200 ms max
tblsh	$\overline{BSY}$ in low to $\overline{SEL}$ out high (to Information transfer phases)	S	100	&	ns	-

& These timings are micro code driven; Exact timing may vary depending on the circumstances.

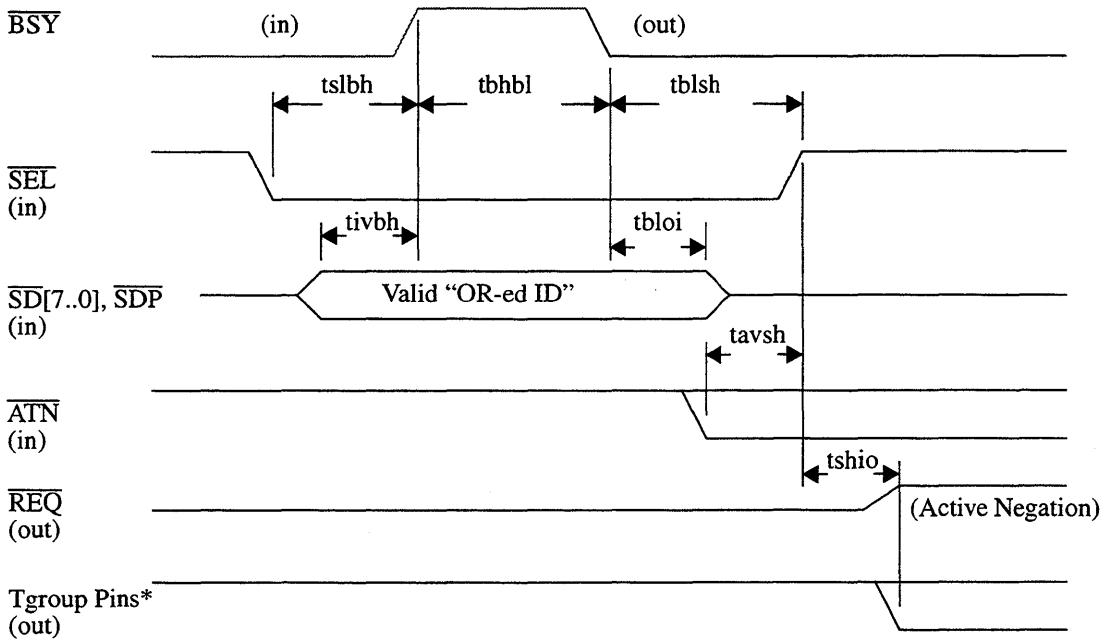


* Tgroup Pins are driven by the target; includes $\overline{I}$/O, $\overline{C}$/D, $\overline{MSG}$, $\overline{REQ}$

9.3.3 Response To Selection (As a Target)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tslbh	$\overline{SEL}$ in assertion (with valid ID) to $\overline{BSY}$ in negation	R	0		ns	1.29 µs min
tivbh	"OR-ed ID" setup time prior to $\overline{BSY}$ in negation	R	0		ns	90 ns min
tbhbl	$\overline{SEL}$ in assertion, ID valid, and $\overline{BSY}$ in negation to $\overline{BSY}$ assertion	S	0.4	200	µs	400 ns min 200 ms max
tbloi	"OR-ed ID" hold time after BSY out assertion	R	0		ns	0 ns min
tblsh	$\overline{BSY}$ out asserted to $\overline{SEL}$ in negated (end of Selection phase)	R	0		ns	90 ns min
tavsh	$\overline{ATN}$ valid input prior to $\overline{SEL}$ in negate	R	0		ns	-
tshio	$\overline{SEL}$ input negate to Tgroup pins valid	S	100	&	ns	-

& These timings are micro code driven; Exact timing may vary depending on the circumstances.

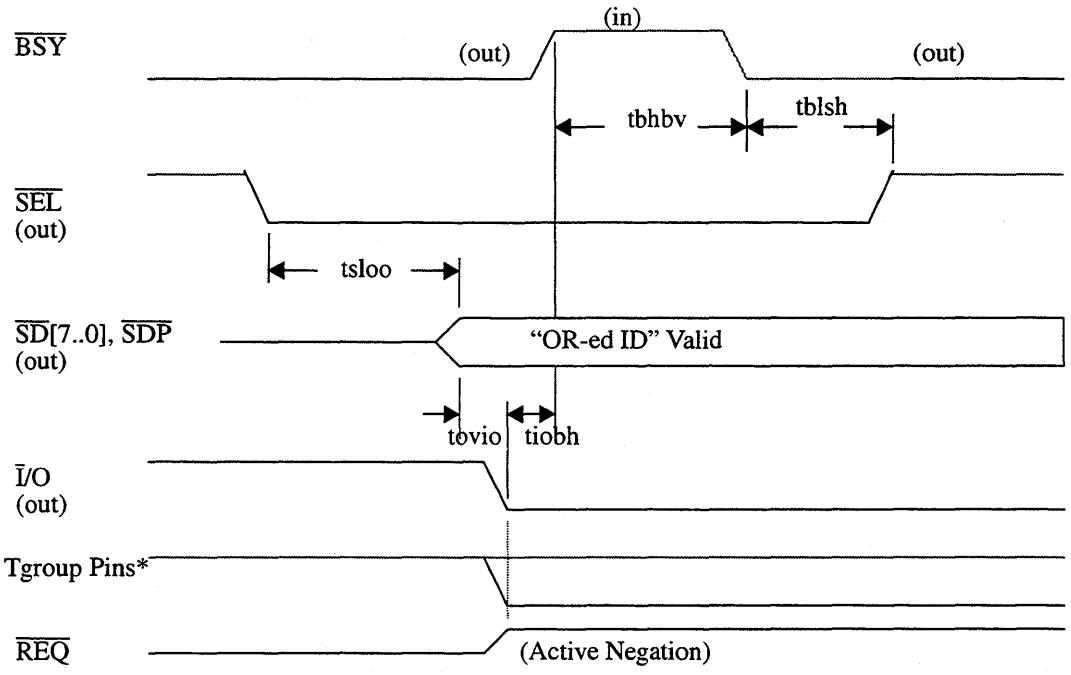


*Tgroup Pins are driven by the target; includes I/O, C/D, MSG

9.3.4 Reselecting an Initiator (As a Target)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tsloo	$\overline{SEL}$ out assertion to "OR-ed ID" output valid	S	&		µs	1.2 µs min
tovio	"OR-ed ID" out valid to $\overline{I}$/O and Tgroup pins out valid	S	100	&	ns	-
tiobh	Tgroup pins out valid prior to $\overline{BSY}$ out negate	S	100	&	ns	90 ns min
tbhbv	$\overline{BSY}$ out negation to $\overline{BSY}$ input assertion valid	R	400		ns	400 ns min 200 ms max
tblsh	$\overline{BSY}$ input assert to $\overline{SEL}$ and $\overline{BSY}$ out valid	S	100	&	ns	90 ns min

& These timings are micro code driven; Exact timings vary depending on circumstances.

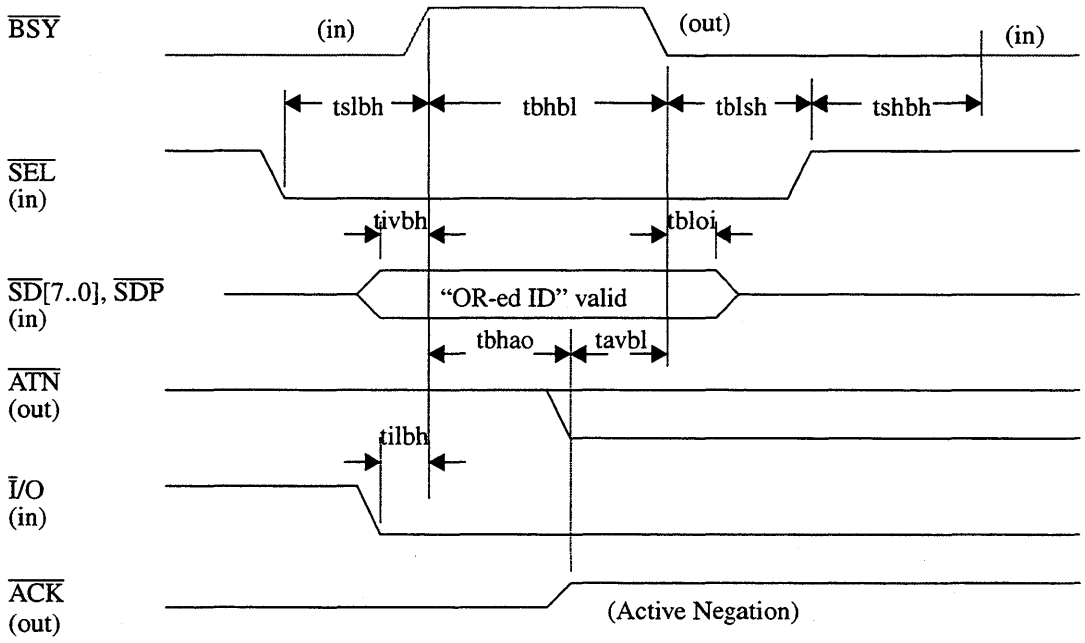


*Tgroup Pins are driven by the target; includes $\overline{C}$/D, $\overline{MSG}$

9.3.5 Response to Reselection (As an Initiator)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tslbh	$\overline{SEL}$ in assert prior to $\overline{BSY}$ input negate	R	0		ns	1.2 µs min
tivbh	"OR-ed ID" setup time prior to $\overline{BSY}$ input high	R	0		ns	90 ns min
tilbh	$\overline{I}$/O input assertion prior to $\overline{BSY}$ input high	R	0		ns	90 ns min
♦tbhao	$\overline{SEL}$ in low, ID valid, $\overline{BSY}$ in high to $\overline{ATN}$, $\overline{ACK}$ driving	S	100		ns	-
♦tavbl	Igroup ($\overline{ATN}$, $\overline{ACK}$) driving to $\overline{BSY}$ out assertion	S	100		ns	-
tbhbl	$\overline{BSY}$ in high to $\overline{BSY}$ out low9.3.3	S	0.4	200	µs	400 ns min 200 ms max
♦tbloi	"OR-ed ID" hold time after $\overline{BSY}$ out assertion	R	0		ns	0 ns min
♦tblsh	$\overline{BSY}$ out low prior to $\overline{SEL}$ input high (end of reselection phase)	R	0		ns	90 ns min
♦tshbh	$\overline{SEL}$ input high to $\overline{BSY}$ out high	S	0	&	ns	0 ns min

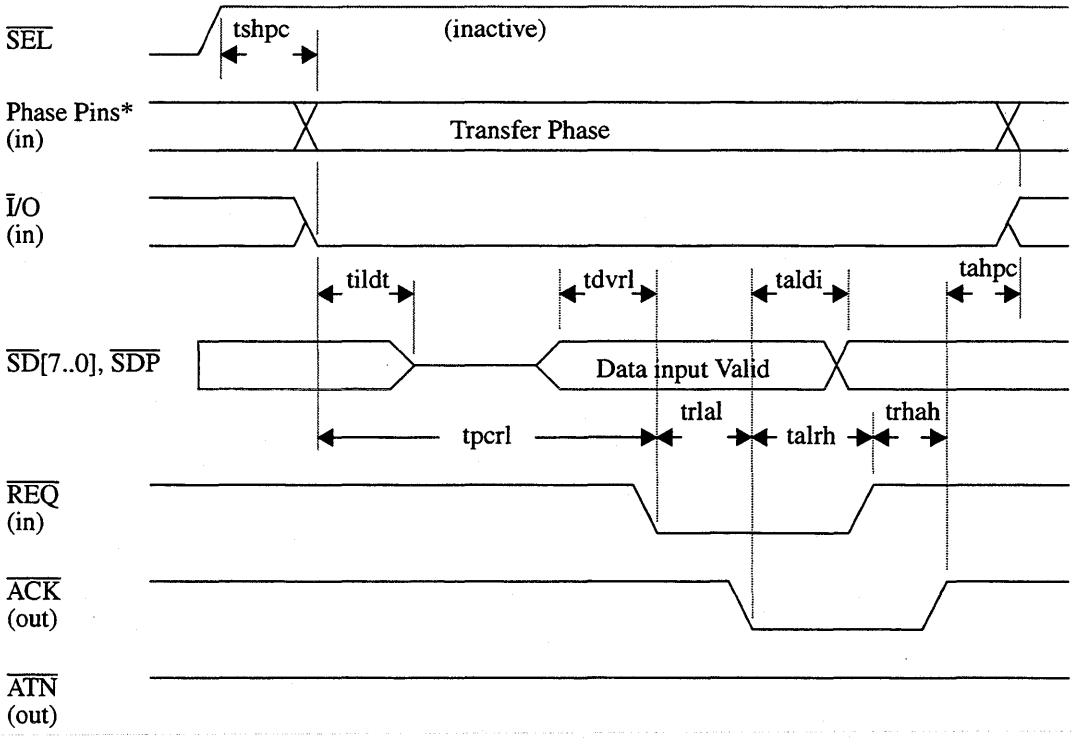
& These timings are micro code driven; Exact timings vary depending on circumstances



9.3.6 Receive Asynchronous Information Transfer In (Acting as an Initiator)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦tshpc_iar	$\overline{SEL}$ input high to Phase pins valid	R	0		ns	0 ns min
tildt_iar	Tri-state delay on Data bus from $\overline{I}$/O pin low	S	0	125	ns	400 ns max
♦tpcrl_iar	Transfer phase valid to the first $\overline{REQ}$ input assertion	R	400		ns	400 ns min
tdvrl_iar	Data input valid setup time prior to $\overline{REQ}$ input low	R	5		ns	12 ns min
♦trlal_iar	$\overline{ACK}$ out low response time from $\overline{REQ}$ input low	S	0	&	ns	0 ns min
taldi_iar	Data input hold time after $\overline{ACK}$ out low	R	0		ns	22 ns min
talrh_iar	$\overline{REQ}$ input clear time after $\overline{ACK}$ out low	R	0		ns	0 ns min
trhah_iar	$\overline{ACK}$ output clear time after $\overline{REQ}$ input high	S	0	&	ns	0 ns min
♦tahpc_iar	Phase change after the final $\overline{ACK}$ out high	R	0		ns	0 ns min

& These timings may be driven by microcode; Exact timings vary depending on circumstances.

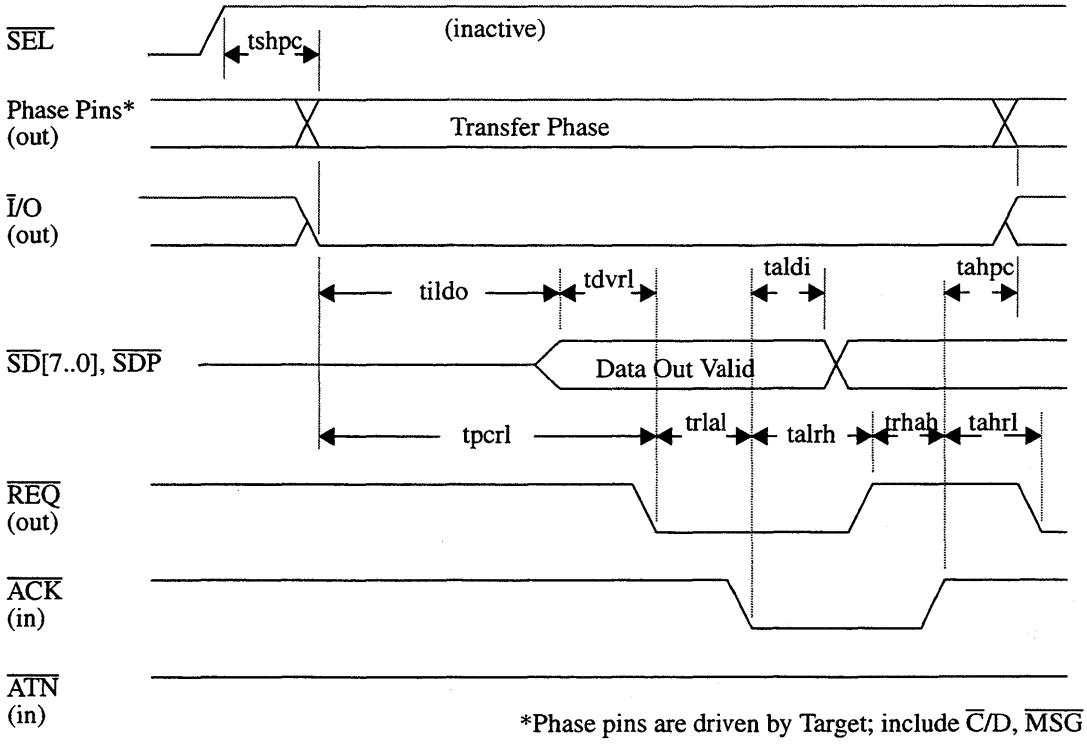


*. Phase Pins are driven by Target; include $\overline{C}$/D, $\overline{MSG}$, $\overline{I}$/O

9.3.7 Send Asynchronous Information Transfer In (Acting as a Target)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦tshpc_tas	$\overline{SEL}$ input high (inactive) to Phase pins output valid	S	100	&	ns	0 ns min
♦tildo_tas	Data output valid delay from $\overline{I}$/O output low	S	800	&	ns	-
tdvrl_tas	Data output setup time prior to $\overline{REQ}$ output low	S	55		ns	25 ns min
♦tpcrl_tas	Transfer phase valid prior to $\overline{REQ}$ output low	S	500	&	ns	400 ns min
trlal_tas	$\overline{REQ}$ out low setup time prior to $\overline{ACK}$ input low	R	0		ns	0 ns min
talrh_tas	$\overline{REQ}$ out clear time after $\overline{ACK}$ input low	S	0	&	ns	0 ns min
taldi_tas	Data output hold time after $\overline{ACK}$ input low	S	20		ns	0 ns min
trhah_tas	$\overline{ACK}$ input clear after $\overline{REQ}$ output high	R	0		ns	0 ns min
♦tahpc_tas	Phase change after the final $\overline{ACK}$ high	S	100	&	ns	0 ns min
tahrl_tas	$\overline{ACK}$ input high to next $\overline{REQ}$ out low	S	0	&	ns	0 ns min

& These timings are micro code driven; Exact timing may vary depending on the circumstances.

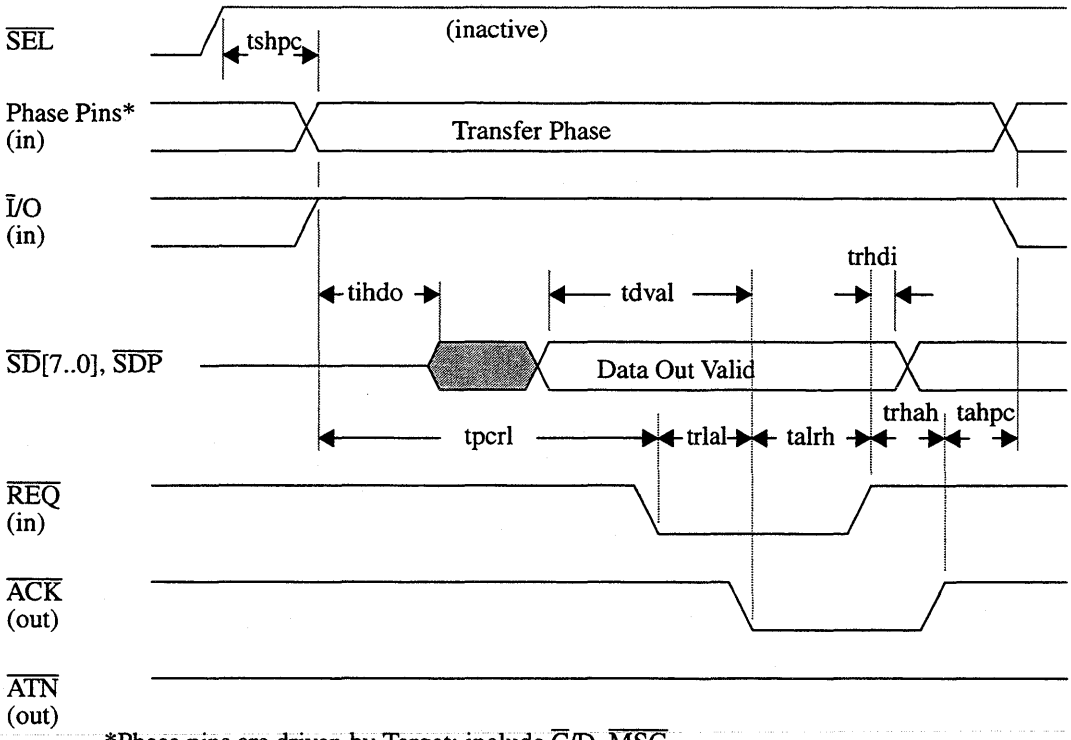


*Phase pins are driven by Target; include C/D, MSG

9.3.8 Send Asynchronous Information Transfer Out (Acting as an Initiator)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦tshpc_ias	$\overline{SEL}$ input high to Phase pins valid	R	0		ns	0 ns min
♦tihdo_ias	$\overline{I/O}$ input high to Data Out driving	S	0		ns	-
♦tpcrl_ias	Phase valid to the first $\overline{REQ}$ in low	R	400		ns	400 ns min
trlal_ias	$\overline{ACK}$ out low delay from $\overline{REQ}$ in low	S	0			0 ns min
tdval_ias	Data out valid prior to $\overline{ACK}$ out low	S	55	&	ns	25 ns min
talrh_ias	$\overline{REQ}$ input clear time after $\overline{ACK}$ out low	R	0			0 ns min
trhah_ias	$\overline{ACK}$ out negation after $\overline{REQ}$ input high	S	0			0 ns min
trhdi_ias	Data output hold time after $\overline{REQ}$ input high	S	25		ns	-
♦tahpc_ias	Phase change after the final $\overline{ACK}$ out high	R	0		ns	0 ns min

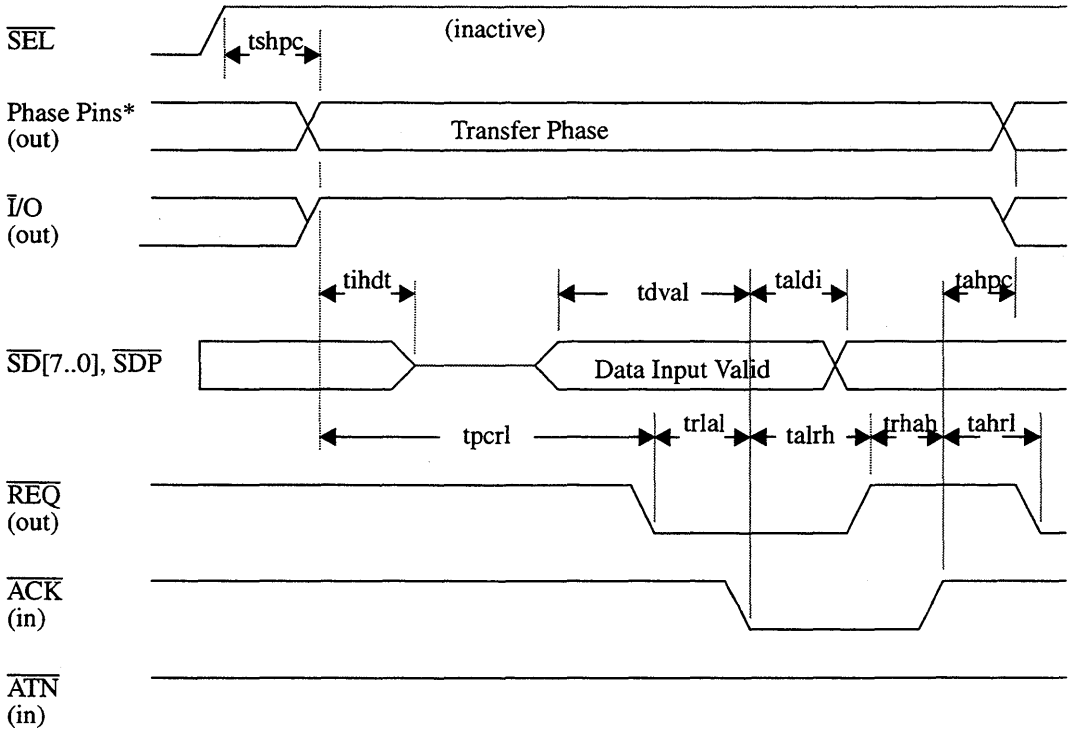
& These timings are micro code driven; Exact timings vary depending on circumstances



*Phase pins are driven by Target; include $\overline{C/D}$, $\overline{MSG}$

9.3.9 Receive Asynchronous Information Transfer Out (Acting as a Target)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦tshpc_tar	$\overline{SEL}$ input high to Phase pins output valid	S	100		ns	0 ns min
♦tihdt_tar	Tri-state delay on data bus from $\overline{I}$/O out high	S		0	ns	400 ns max
♦tpcrl_tar	Phase valid prior to $\overline{REQ}$ output low	S	500		ns	400 ns min
trlal_tar	$\overline{ACK}$ input low after $\overline{REQ}$ out low	R	0		ns	0 ns min
tdval_tar	Data input valid setup time prior to $\overline{ACK}$ input low	R	5		ns	12 ns min
talrh_tar	$\overline{REQ}$ out clear after $\overline{ACK}$ input low	S	0		ns	0 ns min
taldi_tar	Data input hold time after $\overline{ACK}$ input low	R	10		ns	-
trhah_tar	$\overline{ACK}$ input clear after $\overline{REQ}$ out high	R	0		ns	0 ns min
♦tahpc_tar	Phase change after the final $\overline{ACK}$ high	S	100		ns	0 ns min
tahrl_tar	$\overline{ACK}$ input high to next $\overline{REQ}$ out low	S	0		ns	0 ns min

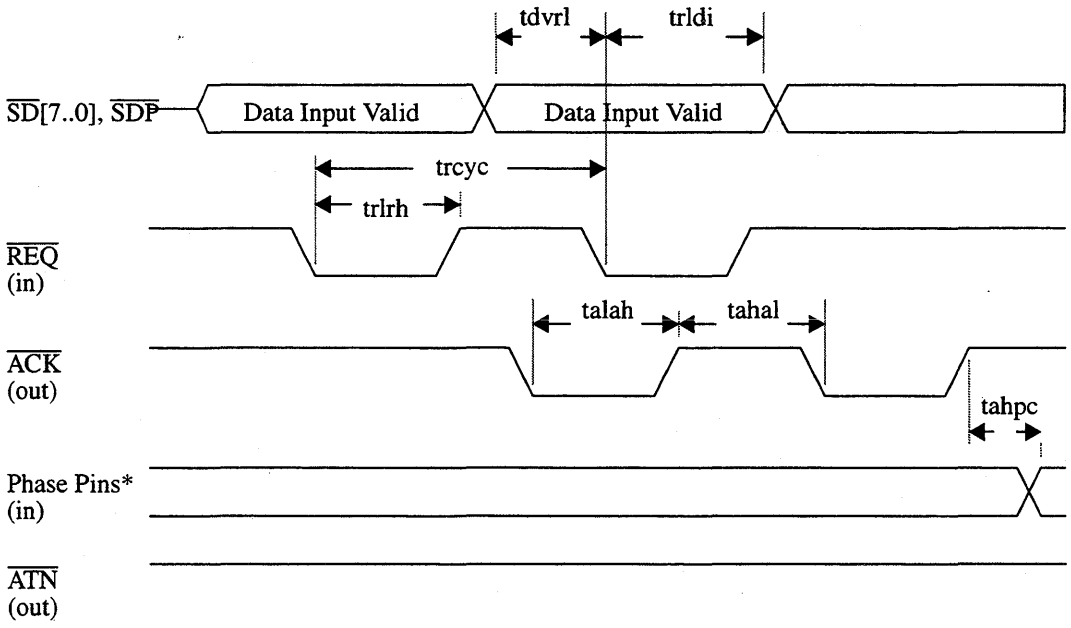


9.3.10 Receive Synchronous Information Transfer In (Acting as an Initiator)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tdvrl_isr	Data input setup time prior to $\overline{REQ}$ input low	R	5		ns	12 ns min
trldi_isr	Data input hold time after $\overline{REQ}$ input low	R	15		ns	22 ns min
trcyc_isr	$\overline{REQ}$ input cycle time	R	2		Tcyc	200 ns min 100 ns min[a]
trlrh_isr	$\overline{REQ}$ input low pulse width	R	30		ns	30 ns min
talah_isr	$\overline{ACK}$ output low pulse width[b]	S	1 - 10 ns		Tcyc	90 ns min 30 ns min[a]
♦tahal_isr	$\overline{ACK}$ output recovery time[b]	S	1 - 10 ns		Tcyc	90 ns min 30 ns min[a]
tahpc_isr	Phase change after $\overline{ACK}$ out high	R	0		ns	0 ns min

a. Fast SCSI timing. Applicable to 10MB/s transfer.

b. tahal and talah are complementary timings; they always add up to an integral multiple of Tcyc, depending on the programmed value in the SYNCHRONOUS TRANSFER register (see 6.2.12).



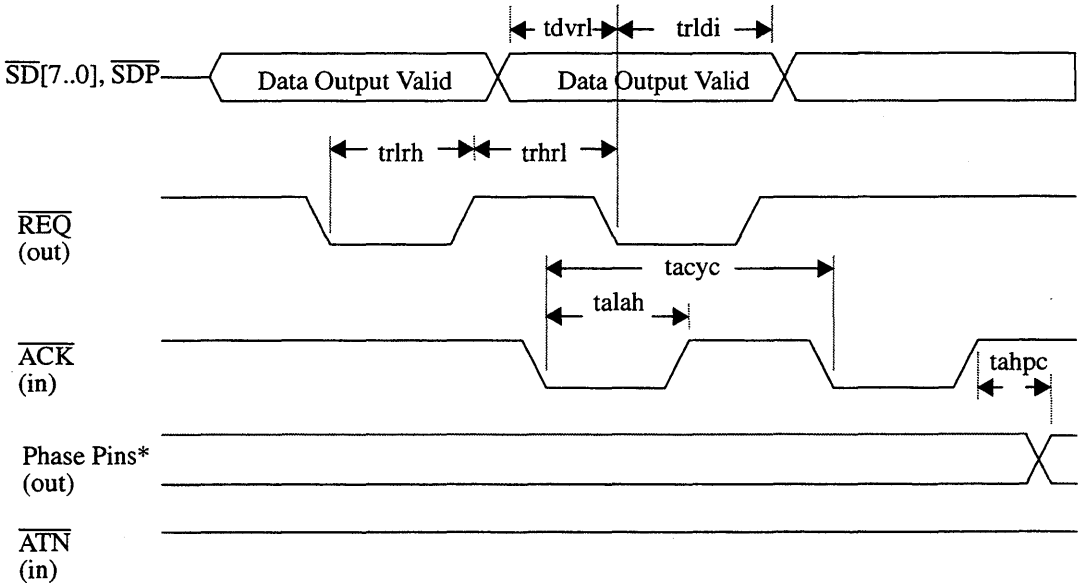
* Phase pins are driven by Target; include $\overline{C}$/D, $\overline{MSG}$, $\overline{I}$/O

9.3.11 Send Synchronous Information Transfer In (Acting as a Target)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tdvrl_tss	Data output setup time prior to $\overline{REQ}$ output low	S	1 - 20 ns		Tcyc	25 ns min
trldi_tss	Data output hold time after $\overline{REQ}$ output low	S	1 - 15 ns		Tcyc	35 ns min
trlrh_tss	$\overline{REQ}$ output low pulse width[a]	S	1 - 10 ns		Tcyc	80 ns min 30 ns min[b]
trhrl_tss	$\overline{REQ}$ output recovery time[a]	S	1 - 10 ns		Tcyc	80 ns min 30 ns min[b]
tacyc_tss	$\overline{ACK}$ input cycle time	R	2		Tcyc	200 ns min 100 ns min[b]
talah_tss	$\overline{ACK}$ input pulse width	R	30		ns	80 ns min 30 ns min[b]
♦tahpc_tss	Phase change after the final $\overline{ACK}$ high	S	100		ns	0 ns min

a. trlrh and trhrl are complementary timings; they always add up to 2 x Tcyc or higher, depending on the programmed value in the SYNCHRONOUS TRANSFER register (see 6.2.12).

b. Fast SCSI timing. Applicable to 10MB/s transfer.

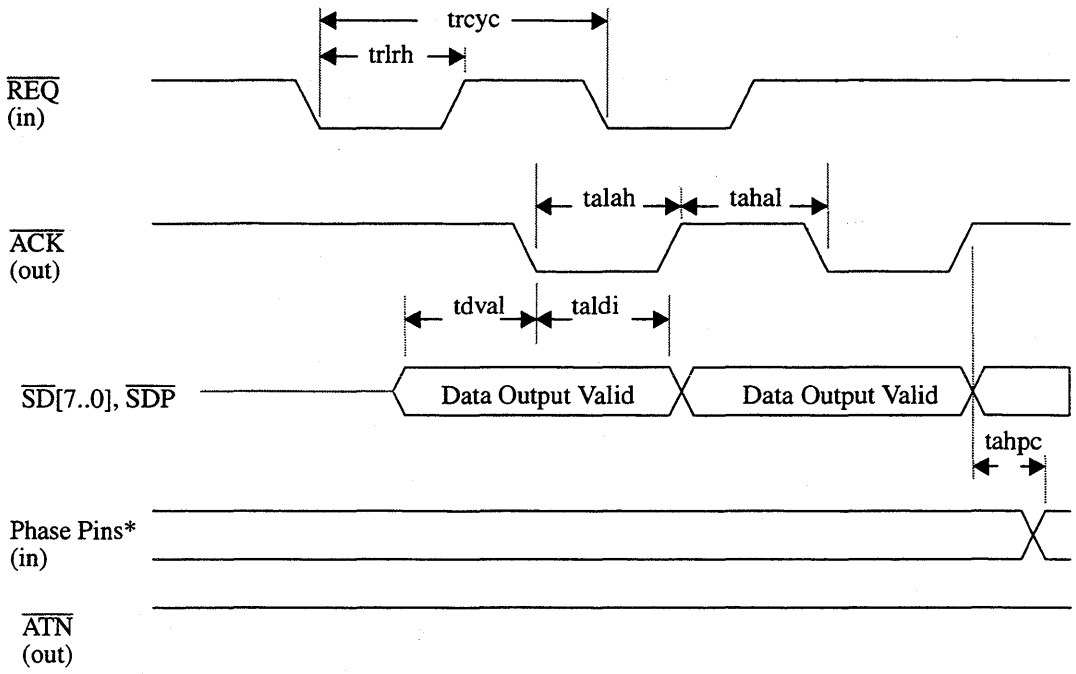


* Phase pins are driven by Target; include C/D, MSG, I/O

9.3.12 Send Synchronous Information Transfer Out (Acting as an Initiator)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tdval_iss	Data output setup time prior to $\overline{ACK}$ output low	S	1 - 25 ns		Tcyc	25 ns min
taldi_iss	Data output hold time after $\overline{ACK}$ output low	S	1 - 15 ns		Tcyc	35 ns min
trcyc_iss	$\overline{REQ}$ input cycle time	R	2		Tcyc	200 ns min 100 ns min[a]
trlrh_iss	$\overline{REQ}$ input low pulse width	R	30			30 ns min
talah_iss	$\overline{ACK}$ output pulse width	S	1 - 10 ns		Tcyc	80 ns min 30 ns min[a]
tahal_iss	$\overline{ACK}$ output recovery time	S	1 - 10 ns		Tcyc	80 ns min 30 ns min[a]
♦tahpc_iss	Phase change after the final $\overline{ACK}$ out high	R	0		ns	0 ns min

a. Fast SCSI timing. Applicable to 10MB/s transfer.

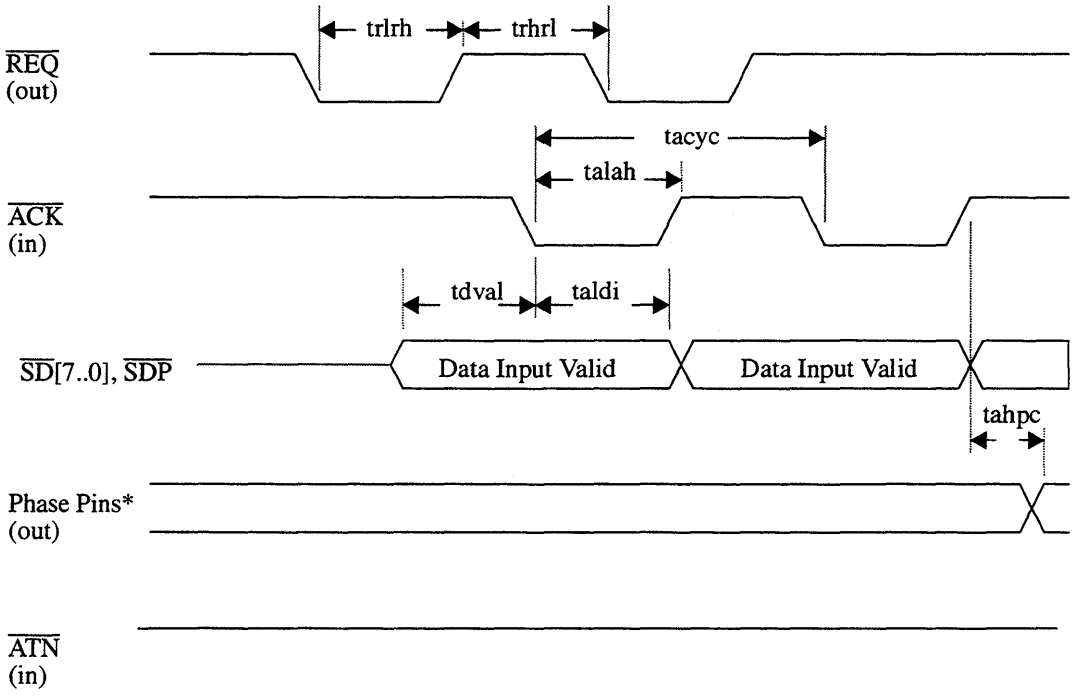


* Phase pins are driven by Target; include $\overline{C}$/D, $\overline{MSG}$, $\overline{I}$/O

9.3.13 Receive Synchronous Information Transfer Out (Acting as a Target)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
tdval_tsr	Data input setup time prior to $\overline{ACK}$ input low	R	5		ns	12 ns min
taldi_tsr	Data input hold time after $\overline{ACK}$ input low	R	15		ns	22 ns min
trlrh_tsr	$\overline{REQ}$ output low pulse width	S	1 - 15 ns		Tcyc	80 ns min 30 ns min[a]
trhrl_tsr	$\overline{REQ}$ output recovery time	S	1 - 10 ns		Tcyc	"
tacyc_tsr	$\overline{ACK}$ input cycle time	R	2		Tcyc	200 ns min 100 ns min[a]
talah_tsr	$\overline{ACK}$ input low pulse width	R	30		ns	90 ns min 30 ns min[a]
♦tahpc_tsr	Phase change after the final $\overline{ACK}$ high	S	100		ns	0 ns min

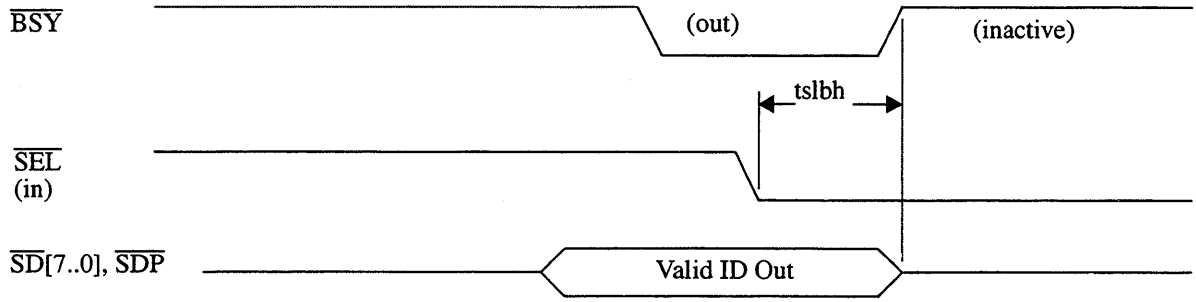
a. Fast SCSI timing. Applicable to 10MB/s transfer.



* Phase pins are driven by Target; include $\overline{C}$/D, $\overline{MSG}$, $\overline{I}$/O

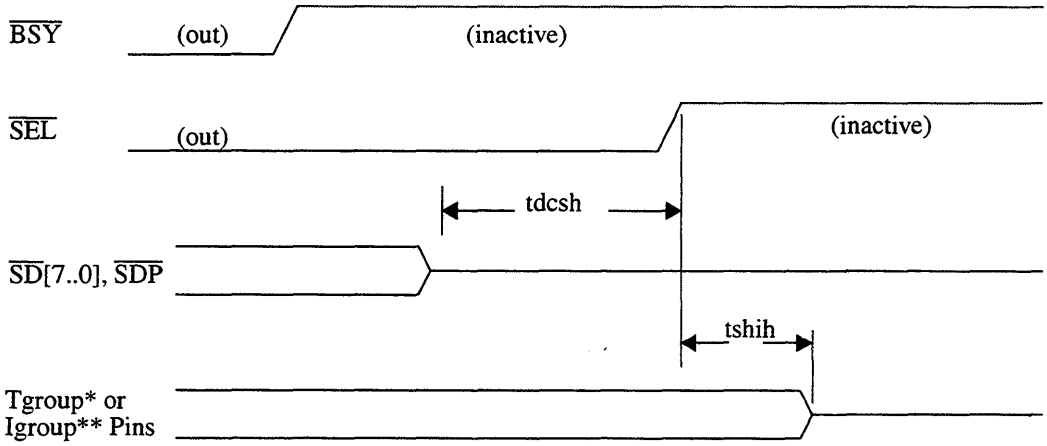
9.3.14 Arbitration to Bus Free (Arbitration Lost)

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦tslbh	$\overline{SEL}$ input low to $\overline{BSY}$, Data bus inactive (tri-state)	S		6 + 75 ns	Tcyc	800 ns max



9.3.15 Selection / Reselection Timeout to Bus Free

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦ttadc	Timeout or abort to data bus cleared	S	0		ns	-
♦tdcsh	Data bus cleared to $\overline{SEL}$ out negation	S	200		µs	200 µs min
♦tshih	$\overline{SEL}$ out high to T / I group pins tri-state	S		10	ns	-

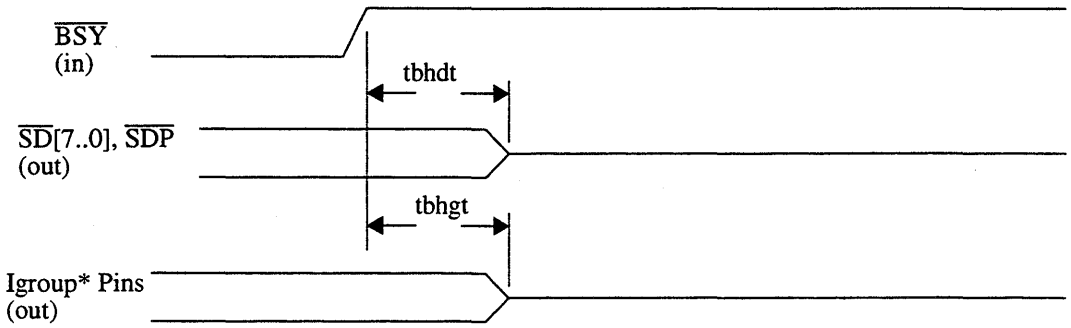


* Tgroup pins are driven by Target; include $\overline{I}$/O, $\overline{C}$/D, $\overline{MSG}$, $\overline{REQ}$

** Igroup pins are driven by Initiator; include $\overline{ATN}$, $\overline{ACK}$

9.3.16 Connected-as-an-Initiator to Bus Free

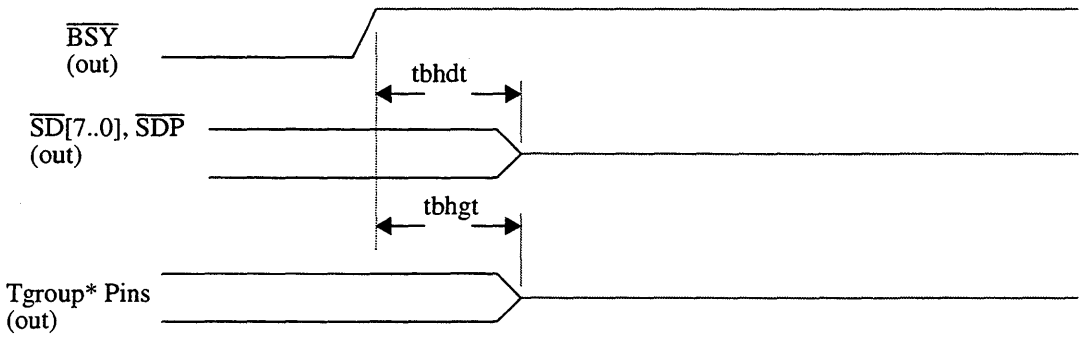
Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦tbhdt	$\overline{BSY}$ input high to Data bus tri-state	S		8 + 75 ns	tcp	1.2 µs max
♦tbhgt	$\overline{BSY}$ input high to Igroup pins tri-state	S		8 + 75 ns	tcp	1.2 µs max



* Igroup pins are driven by an initiator, including $\overline{ATN}$ and $\overline{ACK}$

9.3.17 Connected-as-a-Target to Bus Free

Symbol	Characteristic	R/S	Min	Max	Units	SCSI Spec
♦tbhdt	$\overline{BSY}$ out high to data bus tri-state	S		8 + 75ns	tcp	1.2 µs max
♦tbhgt	$\overline{BSY}$ out high to Tgroup pins tri-state	S		8 + 75ns	tcp	1.2 µs max



* Tgroup pins are driven by Target; include $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

Appendix A - SCAM Specific Features

This section describes the differences between the AIC-33C93B and the AIC-33C93C products.

A.0 New and Modified Register Definitions

A.1 Time-out Period Register (address = 02 hex)

When SCAM-tolerant timings are enabled, the AIC-33C93C will interpret the contents of the Time-out Period Register when selecting or reselecting another device according to the following equation.

$$\text{register value} = \frac{125 T_{per} \times F_{iclk}}{54}$$

where T_{per} is the time-out period specified in milliseconds and F_{iclk} is the input clock frequency in megahertz.

During a SCAM selection, the contents of this register specify how long the selection attempt should last, according to the following equation.

$$\text{register value} = \frac{T_{per} \times F_{iclk}}{20}$$

where T_{per} is the time-out period specified in milliseconds and F_{iclk} is the input clock frequency in megahertz.

A.2 SCSI Control Bus Register (address = 03 hex)

7	6	5	4	3	2	1	0
BSY	SEL	RAI	RAO	ATN	MSG	C/$\overline{D}$	I/$\overline{O}$

The SCSI Control Bus Register will reflect the state of the SCSI bus lines $\overline{BSY}$, $\overline{SEL}$, $\overline{MSG}$, $\overline{C}$/D, $\overline{I}$/O, and $\overline{ATN}$ upon completion of a low-level SCSI I/O command. The bits RAI and RAO indicate the state of $\overline{REQ}$ in and $\overline{ACK}$ out if the AIC-33C93C is in the *Connected-as-a-Target* state or in the *Connected-as-a-SCAM-device* state; otherwise, they indicate the state of $\overline{ACK}$ in and $\overline{REQ}$ out. If a bit is set, the corresponding SCSI control line is asserted. If a bit is not set, the internal microcontroller detected that the corresponding SCSI control line was negated, perhaps due to a wired-or glitch. It is the responsibility of the host processor to debounce the signals.

This register is also used to specify the phase to be set by the Set Phase command.

A.3 SCSI Data Bus Register (address = 04 hex)

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

The SCSI Data Bus Register, in most cases, will reflect the state of the SCSI data bus upon completion of a low-level SCSI I/O Command. If a bit is set, the corresponding SCSI data bus line is asserted. If a bit is not set, the internal microcontroller detected that the corresponding SCSI data line was negated, perhaps due to a wired-or glitch. It is the responsibility of the host processor to debounce the signals.

If the Read SCSI Bus command is executed while in the *Connected-as-an-Initiator* state, this register will contain the value of the data latched on the last $\overline{REQ}$ pulse if the phase was an in phase. If the previous $\overline{REQ}$ pulse occurred during an out phase, the value returned in this register is unpredictable.

This register is also used to specify the data value to be driven onto the SCSI data bus by the AIC-33C93C during the SCAM Transfer and Set Data Bus commands.

B.0 New or Modified Interrupts

B.1 SCAM Selection Completed, and a SCAM Master Responded (12 hex)

A SCAM Select command completed, and a SCAM master is present on the bus. The state of the AIC-33C93C is *Connected-as-a-SCAM-device.*

B.2 SCAM Transfer Cycle Completed Successfully (15 hex)

A SCAM Transfer command completed successfully. The state of the AIC-33C93C is *Connected-as-a-SCAM-device.*

B.3 SCAM Selection Completed, and a SCAM Master Did Not Respond (17 hex)

A SCAM Select command completed, and a SCAM master did not respond. The state of the AIC-33C93C is *Disconnected.*

B.4 SCAM Disconnect Has Occurred (45 hex)

The AIC-33C93C detected the negation of $\overline{C}$/D at the beginning of a SCAM Transfer command. The state of the AIC-33C93C is *Disconnected.*

B.5 SCAM Selection Occurred (86 hex)

The AIC-33C93C responded to a SCAM selection attempt and found a SCAM master present. The AIC-33C93C is in the *Connected-as-a-SCAM-device* state.

C.0 New or Modified Commands

C.1 Reset (00 hex)

This command functions as before but is now also valid in the *Connected-as-a-SCAM-device* state.

C.2 Disconnect (04 hex)

This command functions as before but is now also valid in the *Connected-as-a-SCAM-device* state.

C.3 Low-Level SCSI I/O Commands

- All low-level SCSI I/O commands implicitly execute a Read SCSI Bus command after the specified action is performed.
- Except for the Read SCSI Bus command, the low-level commands are valid only in the *Connected-as-a-SCAM-device* state.

C.3.1 Set Phase (28 hex)

This command sets the SCSI bus phase pins MSG, C/$\overline{D}$, and I/$\overline{O}$ as specified by the value in the SCSI Control Bus Register. Bits 3 through 7 of the register are ignored by this command. No interrupt is generated upon completion of this command.

C.3.2 Set Data (29 hex)

This command forces the data specified in the SCSI Data Bus Register onto the SCSI data bus lines, with the proper parity. No interrupt is generated upon completion of this command.

C.3.3 Read SCSI Bus (2A hex)

This command returns the state of the SCSI bus control lines and the SCSI bus data lines in, respectively, the SCSI Control Bus Register and the SCSI Data Bus Register. No interrupt is generated upon completion of this command. This command is valid in all states.

C.4 SCAM Support Commands

C.4.1 Enable SCAM Tolerant Timings (2C hex)

This command alters two timings involved during the reselection and selection phases. First, the AIC-33C93C will not respond to a normal SCSI selection or reselection until after a valid selection or reselection phase has persisted for more than four milliseconds. Second, the AIC-33C93C changes its interpretation of the Time-out Period Register so that the maximum selection and reselection time-out is four milliseconds. These timings are in effect until the AIC-33C93C is reset. No interrupt is generated upon completion of this command.

C.4.2 Enable SCAM Selection (2D hex)

This command enables the AIC-33C93C to respond to a SCAM selection. Resetting the device disables the response to SCAM selection. No interrupt is generated upon completion of this command.

C.4.3 SCAM Select (2E hex)

This command causes the AIC-33C93C to perform a SCAM selection. The setting the SBT bit determines whether the AIC-33C93C behaves as a level 2 SCAM slave device (SBT=1) or as a level 1 SCAM master device (SBT=0).

Upon detecting the bus free condition, the AIC-33C93C will arbitrate for the bus. If acting as a SCAM master, it will arbitrate with an ID; if acting as a SCAM slave, it will arbitrate without an ID. If it loses arbitration, the AIC-33C93C will release all SCSI signals and will wait for the bus free condition before beginning the process over again. Once the AIC-33C93C has won arbitration, it will proceed with SCAM selection.

The length of the SCAM selection phase is determined by the value in the Time-out Period register. (With a 20 MHz input frequency, the value of the Time-out register equals the SCAM selection time in milliseconds.)

Upon completion of the selection attempt, the AIC-33C93C will generate an interrupt. If a SCAM master is present, i.e. C/$\overline{D}$ is asserted, the AIC-33C93C will generate a 12 hex interrupt and will be in the *Connected-as-a-SCAM-device* state. Otherwise, the AIC-33C93C will generate a 17 hex interrupt and will be in the *Disconnected* state.

C.4.4 SCAM Transfer (2F hex)

This command is valid only in the *Connected-as-a-SCAM-device* state. It causes the AIC-33C93C to perform a SCAM transfer cycle. The data to be transferred is specified in the SCSI Data Bus Register, and the data latched is returned in the SCSI Data Bus Register. For both the data to be sent and the latched data, only the five least-significant bits of the register are valid.

The AIC-33C93C samples C/$\overline{D}$ before performing a transfer, and if it detects that C/$\overline{D}$ has been released, it will terminate the command with a SCAM-Disconnect-Occurred interrupt (45 hex) and release all SCSI lines. The AIC-33C93C will be in the *Disconnected* state.

If C/$\overline{D}$ is asserted, the AIC-33C93C will perform the transfer and then generate a Successful-SCAM-Transfer-Cycle interrupt (15 hex). The AIC-33C93C will be in the *Connected-as-a-SCAM-device* state.

D.0 Level 1 SCAM Master

Power-up:

Bus Reset

Bus Reset:

Int 00	⇒	Write Hard ID to Own ID register
		Soft Reset
		Enable SCAM Tolerant Timings
		Categorize IDs using configuration parameters, if any

Select ID State:

Uncategorized ID	⇒	Select-and-Transfer
Int 16	⇒	Target responded; ID in use
		Go to Select ID state
Int 42	⇒	Target did not respond; ID not in use
		Go to Select ID state
No uncategorized IDs	⇒	Go to Assign ID state

Assign ID State:

SCAM Select
SCAM Transfer (as many as needed)
Disconnect
Repeat Assign ID state, if necessary
Soft Reset
Go to Normal Operation

E.0 Level 1 or 2 SCAM Slave

- *Italicized text applies only to SCAM devices with a default ID.*
- **Bold text applies only to Level 2 SCAM Slave devices.**

Power-up or Bus Reset:

Int 00	⇒	*Set Own ID to Default ID*
		Soft Reset
		Enable SCAM Tolerant Timings
		Enable SCAM Selection
		Enable Reselection

Monitor State:

		Wait for Select and Receive
Int 13	⇒	*Normal SCSI Selection; ID confirmed*
		Process SCSI command
		Soft Reset
		Go to Normal Operation
Int 80/81	⇒	*Reselected; ID confirmed*
		Process reselection
		Soft Reset
		Go to Normal Operation
Int 86	⇒	SCAM selected
		Disable response to selection and reselection
		Go to Assignable Transfer state
Time-out	⇒	**Time to initiate SCAM selection**
		Go to *Abort state* or Select state

Abort State:

		Abort Wait-for-Select-and-Receive
Int 13	⇒	***Normal SCSI Selection; ID confirmed***
		Process SCSI command
		Soft Reset
		Go to Normal Operation
Int 22	⇒	***Wait-for-Select-and-Receive aborted***
		Go to Time-out state
Int 80/81	⇒	***Reselected; ID confirmed***
		Process Reselection
		Soft Reset
		Go to Normal Operation
Int 86	⇒	***SCAM selected***
		Disable response to selection and reselection
		Go to Assignable Transfer state

Select State:

		SCAM Select
Int 12	⇒	**SCAM master responded**
		Go to Assignable Transfer state
Int 17	⇒	**SCAM master did not respond**
		Go to Monitor State
Int 80/81	⇒	***Reselected; ID confirmed***
		Process reselection
		Soft Reset
		Go to Normal Operation
Int 82/83	⇒	***Selected; ID confirmed***
		Resume Wait-for-Select-and-Receive (10)
		Process SCSI command
		Soft Reset
		Go to Normal Operation
Int 86	⇒	**SCAM selected**
		Disable response to selection and reselection
		Go to Assignable Transfer state

Assignable Wait State:

Int 86	⇒	SCAM selected
		Go to Assignable Transfer state

Assignable Transfer State:

		SCAM transfer
Int 15	⇒	Successful transfer
ID assigned	⇒	Disconnect
		Soft Reset
		Go to Normal Operation
ID not assigned	⇒	Go to Assignable Transfer State
Int 45	⇒	SCAM master ended the connection
		Go to Assignable Wait State

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