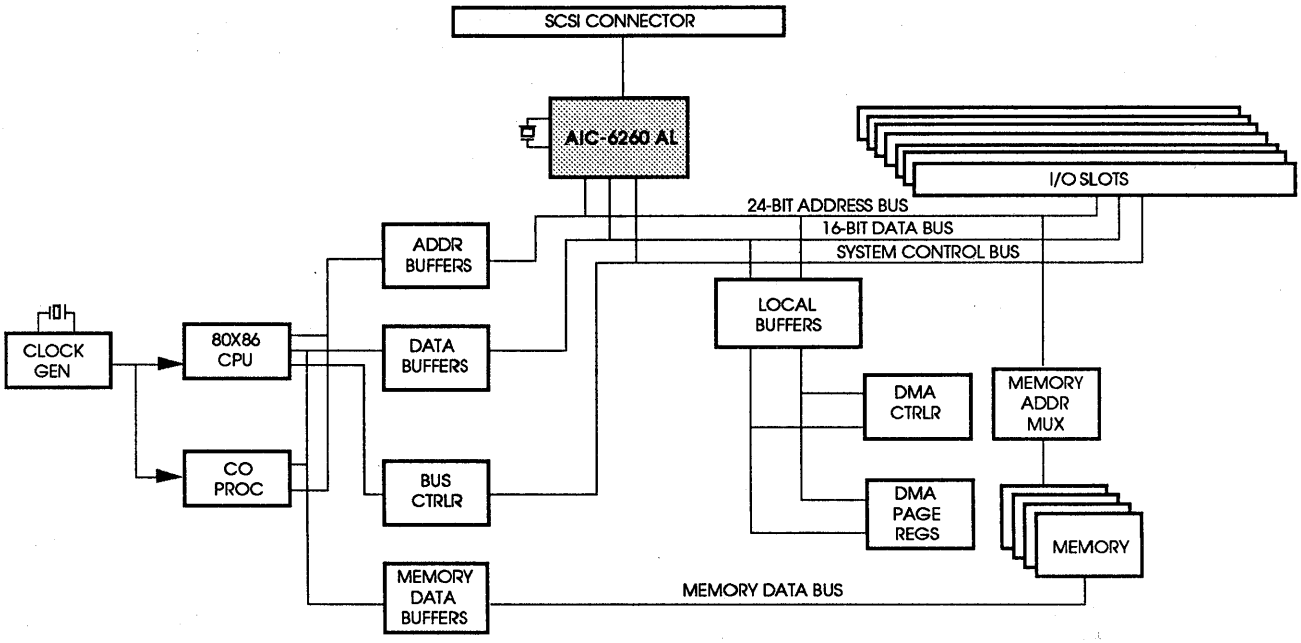
adaptec

AIC-6260

Single-Chip PC AT-to-SCSI I/O Processor

Data Sheet
Rev. 3
May, 1991



FEATURES

- Single-chip PC AT-to-SCSI host adapter
- Low-cost connectivity to multiple SCSI peripherals
- 8-bit DMA or 16-bit PIO transfers supported
- Average data transfer rates up to 4 megabytes/second
- 128-byte FIFO for data buffering
- Synchronous and asynchronous SCSI devices supported
- Multitasking driver software available now
- Up to eight simultaneous I/O tasks supported
- BIOS available now
- 68-pin PLCC or 80-pin QFP packages
- CCS and SCSI-2 supported

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Section One Overview

The AIC-6260 is a single-chip SCSI solution for PC AT and microprocessor-controlled peripherals applications. The AIC-6260 provides all of the functionality necessary to implement a multiple-unit SCSI in one 68-pin PLCC or 80-pin QFP package. Typical applications include laptops, portables, and low-end desktop computers.

The AIC-6260 is a single-chip PC AT bus to SCSI bus controller, designed to bring the power and connectivity of SCSI to the computer system motherboard.

The power of SCSI is demonstrated by a sustained data transfer capability of up to 4 megabytes per second. SCSI bus connectivity gives the system the ability to hook up to any of the growing number of SCSI compatible peripherals available, from hard drives to high–capacity floppy drives, tape drives, CD-ROM, DAT and removable drives.

Embedding the AIC-6260 increases reliability, reduces cost and eliminates the need for a traditional host adapter card. This makes the chip an ideal I/O solution for both desktop and laptop systems.

The AIC-6260 supports second party DMA transfers or programmed I/O. The chip contains a 128-byte data buffer to increase PIO performance. Synchronous or Asynchronous SCSI transfer is supported. A built-in "sleep" mode saves power.

Adaptec cuts the system designer's job in half by supporting the AIC-6260 with a full complement of SCSI driver software.

The ASW-1210 is a multitasking ASPI (Advanced SCSI Programming Interface) manager for DOS, and contains features such as Disconnect/Reconnect on the SCSI bus. This frees the host CPU while peripherals execute time-consuming functions such as Seeks. Up to eight simultaneous I/O tasks can be run in the background, and the driver also allows interrupts from the host CPU. Automatic Request Sense can be done in the event of a "Check Condition" status from a SCSI target LUN. This ensures that valuable status data is not lost.

Configuration Options are programmable and can be set by software during system power up. No need for jumpers!

Configurable options are:

- Enable/Disable Disconnect
- AT Bus ON/OFF Time
- Selection Time Out
- Parity Checking Disable
- DMA/PIO
- SCSI ID
- Synchronous Negotiation

BIOS code is available to allow booting from the SCSI hard drive and to emulate DOS hard disk calls.

Compatibility is assured by support of the ANSI Common Command Set and SCSI-2.

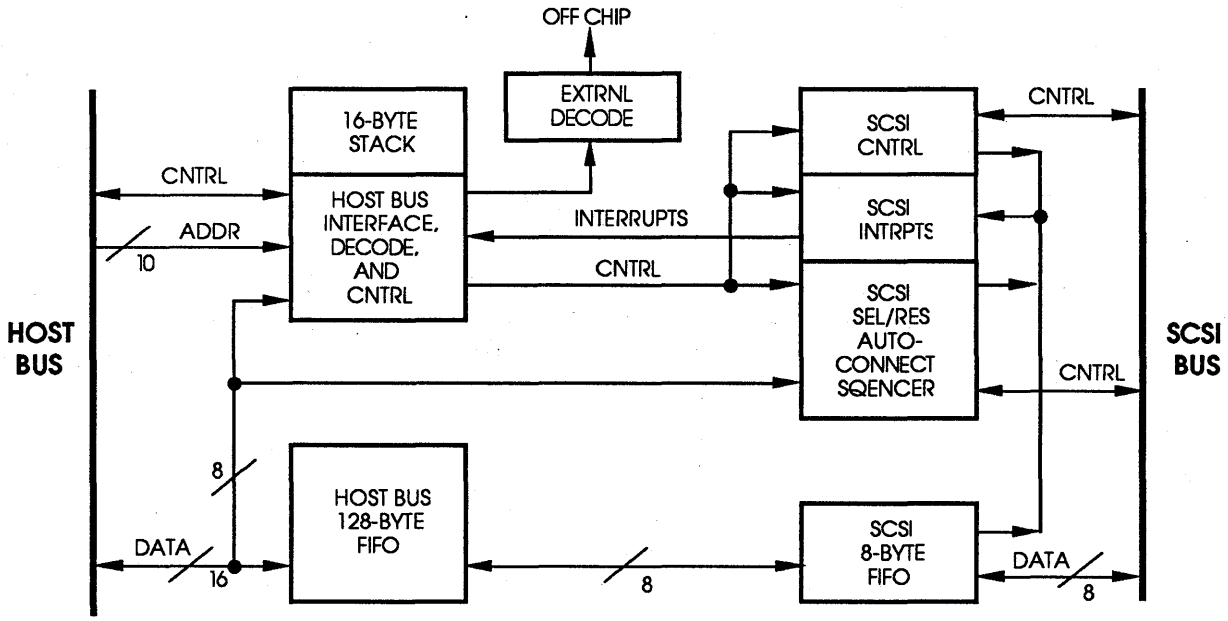


FIGURE 1-1. AIC-6260 FUNCTIONAL BLOCK DIAGRAM

2.1 PIN DESCRIPTIONS

The AIC-6260 is available in a 68-pin PLCC or 80-pin Quad Flat Pack. Figure 2-1 shows the 68-pin PLCC pinout while Figure 2-2 shows the 80-pin QFP. Table 2-1 defines the pin assignments for the AIC-6260.

All SCSI lines utilize open collector drivers (IOL=48mA, input hysteresis=.2V).

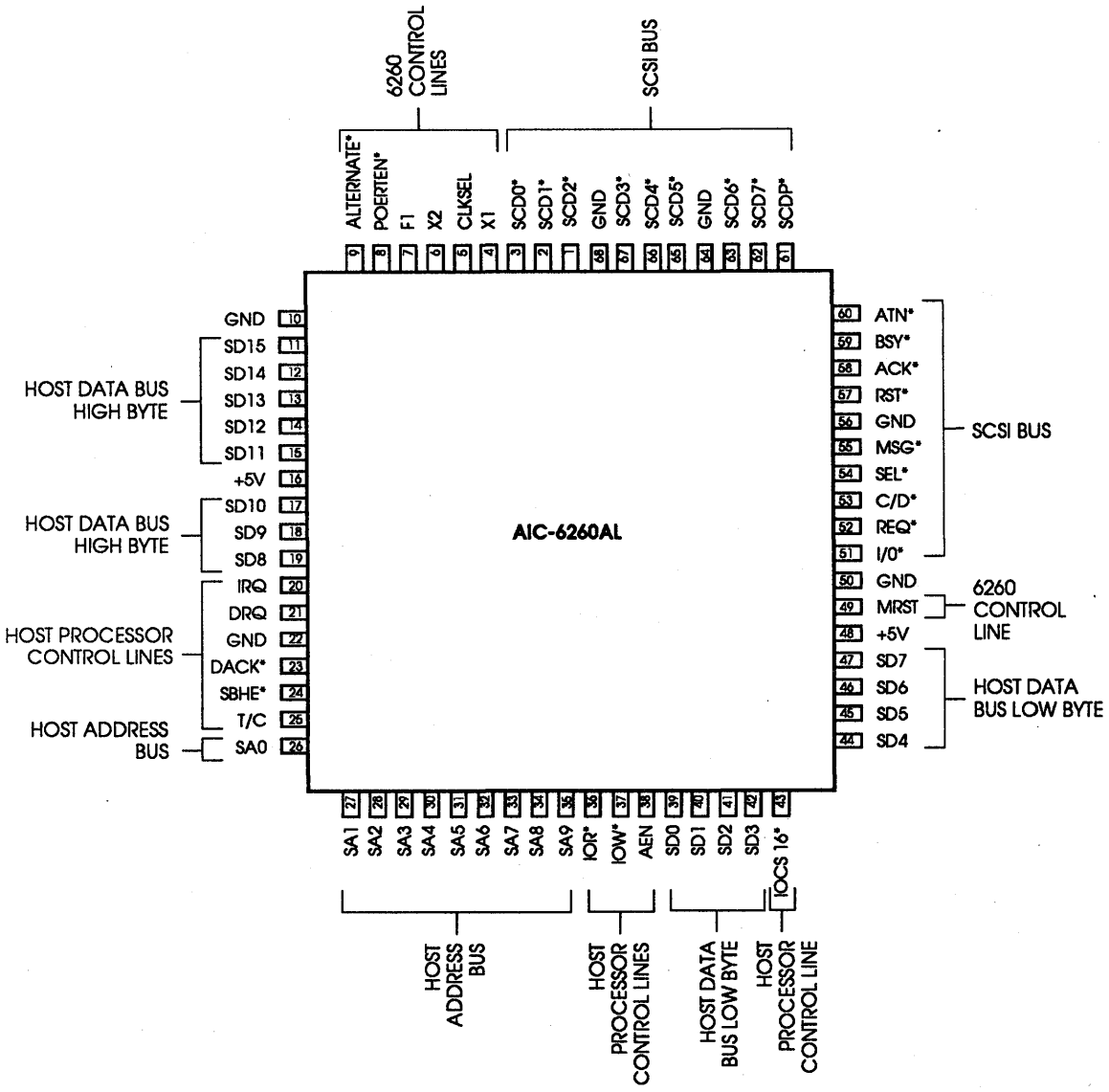


FIGURE 2-1. AIC-6260AL 68-PIN PLCC LOCATIONS

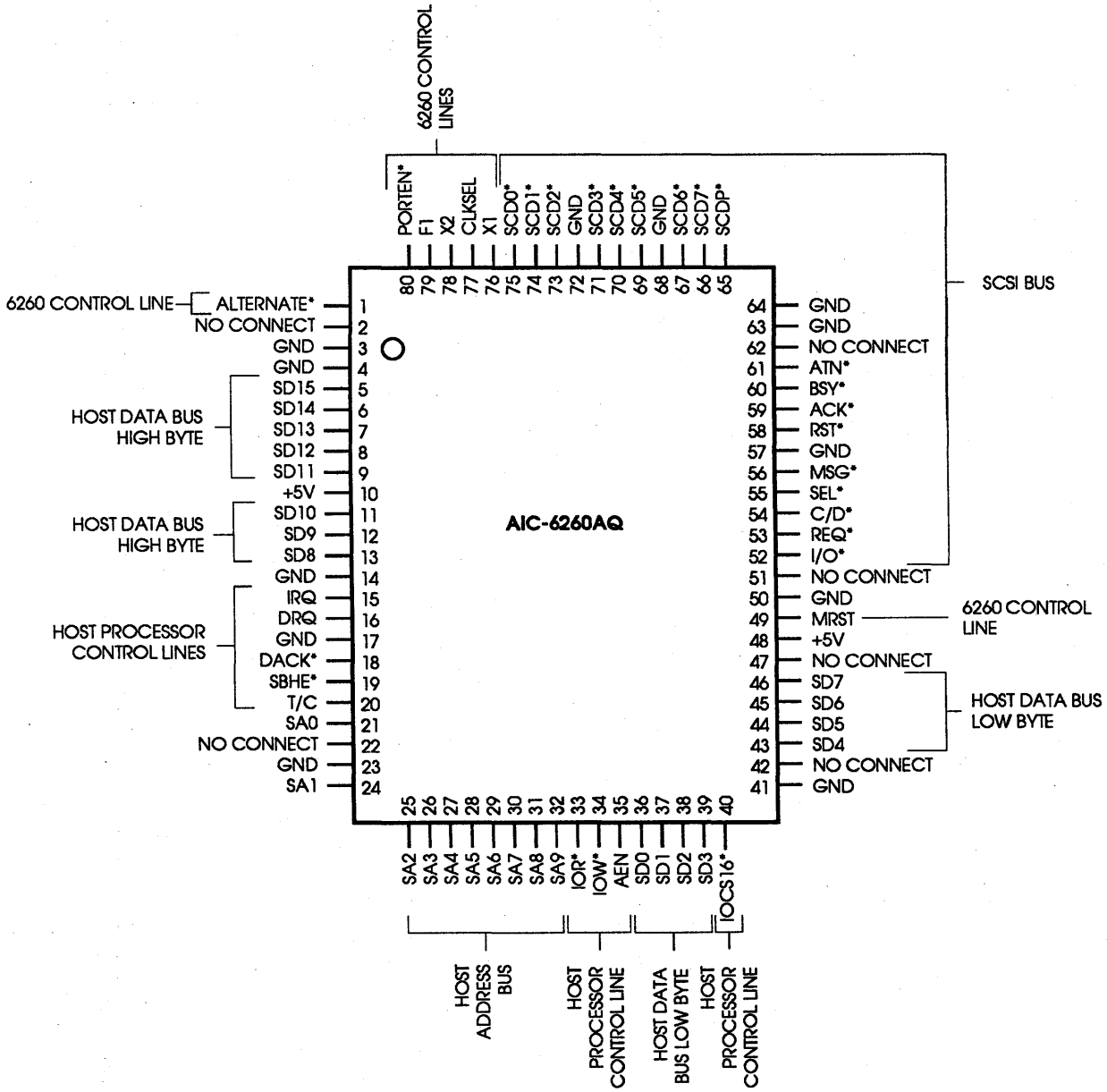


FIGURE 2-2. AIC-6260AQ 80-PIN QUAD FLAT PACK LOCATIONS

TABLE 2-1. AIC-6260 PIN DESCRIPTIONS

SYMBOL	*6260AL PIN NO.*	*6260AQ PIN NO.*	*TYPE*	*DESCRIPTION*
SA0–SA9	26-35	21, 24-32	I	System Address Lines. A 10-bit bus used to load addresses into the AIC-6260 from the host. Chip addresses are decoded at 340_h with ALTERNATE* tied high, and at 140_h with ALTERNATE* tied low.
AEN	38	35	I	Address Enable. A control signal used to indicate the type of transfer taking place across the Host bus. This signal is low for I/O access and high for DMA transfers.
ALTERNATE*	9	1	I	Alternate I/O Address Decode. When tied high, chip addresses are decoded from 340_h. When tied low, chip addresses are decoded from 140_h.
SD0–SD7	39–42 44–47	36-39 43-46	I/O	System Data Lines, Low-Order Byte. An 8-bit data bus used to transfer data between the host and the AIC-6260. Data transfers include register values and data. The host data bus utilizes tri-state drivers (IOH = –8mA, IOL= 24mA).
SD8–SD15	17–19 11–15	5-9, 11-13	I/O	System Data Lines, High-Order Byte. An 8-bit data bus used to transfer data between the host and the AIC-6260 in 16-bit mode. The host data bus utilizes tri-state drivers (IOH = –8mA, IOL= 24mA).
DRQ	21	16	O	DMA Request. A data transfer control signal used to indicate that the AIC-6260 has data to send or is ready to receive data. This signal forms half of the DMA handshake. It is valid for DMA mode transfers only. DRQ utilizes a two-state driver (IOH = –8mA, IOL= 24mA).
DACK*	23	18	I	DMA Acknowledge. A data transfer control signal used to indicate that the host is ready for a DMA transfer. This signal forms half of the DMA handshake. It is valid for DMA mode transfers only.
IRQ	20	15	O	Interrupt Request. A control signal used to indicate the occurrence of a condition requiring host intervention. This is the signal used for all SCSI interrupts. Only interrupts which have been enabled can assert this signal. IRQ utilizes a two-state driver (IOH = –8mA, IOL= 24mA).
IOR*	36	33	I	I/O Read. A control signal used to indicate direction of data transfer across the Host bus. When asserted (active low), indicates data is being read out of the AIC-6260.
IOW*	37	34	I	I/O Write. A control signal used to indicate direction of data transfer across the Host bus. When asserted (active low), indicates data is being written into the AIC-6260.

T/C	25	20	I	Terminal Count. A control signal used to indicate the completion of a DMA transfer. This signal is driven by the host DMA controller.
SBHE*	24	19	I	System Bus High Enable. This signal indicates that data on the SD8–SD15 lines is valid.
IOCS16*	43	40	O	I/O Chip Select 16. This signal is driven low when the current I/O data transfer is 16 bits (one word) wide. Open collector driver, IOL = 24 mA.
MRST	49	49	I	Master Reset. A control signal is used to restore the AIC-6260 to its start-up condition. This signal is active high at power up or hard reset. This signal has hysteresis for noise immunity. (1.5V <Vth+ <2.0V; .6V <Vth – <1.1V; Vth + – Vth – = .4V)
SCD0-7*	1–3 62, 63, 65–67	66,67 69-71, 73-75	I/O	SCSI Data Bus. An 8-bit data bus used to transfer data between the AIC-6260 and devices on the SCSI Bus. Data transfers include SCSI commands, Status, Messages and user data. Open collector driver, IOL = 48mA, input hysteresis .2V.
SCDP*	61	65	I/O	SCSI Data Parity. A control signal used to check for data transfer errors on the SCSI bus. This signal with SCSI data always generates odd parity when the AIC-6260 is driving the SCSI Bus. This signal is tested when the AIC-6260 is receiving and parity checking is enabled. Open collector driver, IOL = 48mA, input hysteresis .2V.
RST*	57	58	I/O	SCSI Reset. A control signal used to restore devices attached to the SCSI bus to their start-up condition. This signal is driven under programmed control. When detected, RST* may cause the assertion of IRQ. Open collector driver, IOL = 48mA, input hysteresis .2V.
ATN*	60	61	I/O	SCSI Attention. A control signal used to indicate that an initiator wishes to send a Message out to a Target. ATN* is driven when the AIC-6260 is in initiator mode and detected when the AIC-6260 is in target mode. Open collector driver, IOL = 48mA, input hysteresis .2V.
BSY*	59	60	I/O	SCSI Busy. A control signal used for bus arbitration and device selection on the SCSI bus. Open collector driver, IOL = 48 mA, input hysteresis .2V.
SEL*	54	55	I/O	SCSI Select. A control signal used for device selection on the SCSI Bus. Open collector driver, IOL = 48mA, input hysteresis .2V.
C/D*	53	54	I/O	SCSI Command/Data. A control signal driven by the target to indicate the type of transfer taking place across the SCSI bus (SCD0–7). C/D* is driven when the AIC-6260 is in target mode and detected when it is in initiator mode. Open collector driver, IOL = 48mA, input hysteresis .2V.

I/O*	51	52	I/O	SCSI Input/Output. A control signal driven by the target to indicate the direction of transfer across the SCSI bus (SCD0–7 and SCDP). When driven low, indicates data is being passed from the target to the initiator. When driven high, indicates data is being passed to the target from the initiator. I/O* is driven when the AIC-6260 is in target mode and is detected when the AIC-6260 is in initiator mode. Open collector driver, IOL = 48 mA, input hysteresis .2V.
MSG*	55	56	I/O	SCSI Message. A control signal driven by the target to indicate the type of transfer across the SCSI Bus (SCD0–7* and SCDP). MSG* is driven when the AIC-6260 is in target mode and is detected when the AIC-6260 is in initiator mode. Open collector driver, IOL = 48mA, input hysteresis .2V.
REQ*	52	53	I/O	SCSI Request. A data transfer control signal used to indicate that the target has data to send or is ready to receive data. This signal forms half of the SCSI data transfer handshake. REQ* is driven when the AIC-6260 is in target mode and is detected when the AIC-6260 is in initiator mode. Open collector driver, IOL = 48mA, input hysteresis .2V.
ACK*	58	59	I/O	SCSI Acknowledge. A data transfer control signal used to indicate that the initiator has sent or received data. This signal forms half of the SCSI data transfer handshake. ACK* is driven when the AIC-6260 is in initiator mode and is detected when it is in target mode. Open collector driver, IOL = 48mA, input hysteresis .2V.
PORTEN*	8	80	O	Port Enable. This is an address decode for an external port driver. Address bits 1–9 are included in this signal decode along with AEN. Address bit 0 must be decoded externally with IOR and IOW. (Two-state driver: IOH = –2 mA, IOL = 2 mA.)
+5V	16,48	10,48	I	5-Volt Power Supply. ±5% max. variation. Two pins.
GND	10,22, 50,56, 64,68	3,4,14, 17,23,41, 50,57,63, 64,68,72	I	Ground. Six pins.
X1	4	76	I	Crystal Input. 20 MHz crystal input for internal oscillator.
X2	6	78	O	Crystal Output. 20 MHz crystal output for internal oscillator.
F1	7	79	I/O	Clock In/Out. This pin is either a clock input or output, depending on the condition of CLKSEL. If CLKSEL is tied high, it is a clock output. If CLKSEL is left to float, it is the clock input for the AIC-6260.
CLKSEL	5	77	I	Clock Select. This pin selects the clock source. If tied to +5 VDC, the internal oscillator circuit is selected as the clock. In this case, CLKSEL provides V_{dd} for the internal oscillator. If left to float, CLKSEL is internally pulled down thereby selecting F1 as the clock source.

This section contains information on the AIC-6260's internal registers. Each register is described under its own heading, identified by name and address.

There are 32 registers, normally decoded from 340_h through $35E_h$. If ALTERNATE* is asserted (low), the registers are decoded from 140_h. Registers are written and read by the host processor via the host bus, in I/O address space.

The following conventions are used throughout this section:

- **set:** Indicates that the target bit was loaded with a 1.
- **clear:** Indicates that the target bit was loaded with a 0.
- **(0):** Indicates that the associated bit is set to 0 after a hard reset.
- **(1):** Indicates that the associated bit is set to 1 after a hard reset.
- **(x):** Indicates the state of the bit after a hard reset is undefined.

Table 3-1 is an address map of the AIC-6260 registers.

TABLE 3-1. AIC-6260 REGISTER ADDRESS MAP

340_h SCSISEQ	341_h SXFRCTL0	342_h SXFRCTL1	343_h SCSISIGO	343_h SCSISIGI	344_h SCSIRATE
R/W	R/W	R/W	W	R	W
7 TEMODEO	7 SCSIEN	7 BITBUCKET	7 CDO	7 CDI	7 RSVD
6 ENSELO	6 DMAEN	6 SWRAPEN	6 IOO	6 IOI	6 SXFR (2)
5 ENSELI	5 CH1/CH2	5 ENSPCHK	5 MSGO	5 MSGI	5 SXFR (1)
4 ENRESELI	4 CLRSTCNT	4 STIMESEL (1)	4 ATNO	4 ATNI	4 SXFR (0)
3 ENAUTOATNO	3 SPIOEN	3 STIMESEL (0)	3 SELO	3 SELI	3 SOFS (3)
2 ENAUTOATNI	2 RSVD	2 ENSTIMER	2 BSYO	2 BSYI	2 SOFS (2)
1 ENAUTOATNP	1 CLRCH1	1 BYTEALIGN	1 REQO	1 REQI	1 SOFS (1)
0 SCSIRSTO	0 RSVD	0 RSVD	0 ACKO	0 ACKI	0 SOFS (0)

345_h SCSIID	345_h SELID	346_h SCSIDAT	347_h SCSIBUS	348_h STCNT0	349_h STCNT1
W	R	R/W	R	R/W	R/W
7 RSVD	7 SELID 7	7 DB (7)	7 SDB (7)	7 STCNT (07)	7 STCNT (15)
6 OID (2)	6 SELID 6	6 DB (6)	6 SDB (6)	6 STCNT (06)	6 STCNT (14)
5 OID (1)	5 SELID 5	5 DB (5)	5 SDB (5)	5 STCNT (05)	5 STCNT (13)
4 OID(0)	4 SELID 4	4 DB (4)	4 SDB (4)	4 STCNT (04)	4 STCNT (12)
3 RSVD	3 SELID 3	3 DB (3)	3 SDB (3)	3 STCNT (03)	3 STCNT (11)
2 TID (2)	2 SELID 2	2 DB (2)	2 SDB (2)	2 STCNT (02)	2 STCNT (10)
1 TID (1)	1 SELID 1	1 DB (1)	1 SDB (1)	1 STCNT (01)	1 STCNT (09)
0 TID (0)	0 SELID 0	0 DB (0)	0 SDB (0)	0 STCNT (00)	0 STCNT (08)

$34A_h$ STCNT2	$34B_h$ CLRSINT0	$34B_h$ SSTAT0	$34C_h$ CLRSINT1	$34C_h$ SSTAT1	$34D_h$ SSTAT2
R/W	W	R	W	R	R
7 STCNT (23)	7 SETSDONE	7 TARGET	7 CLRSELTIMO	7 SELTO	7 RSVD
6 STCNT (22)	6 CLRSELDO	6 SELDO	6 CLRATNO	6 ATNTARG	6 RSVD
5 STCNT (21)	5 CLRSELDI	5 SELDI	5 CLRSCSIRSTI	5 SCSIRSTI	5 SOFFSET
4 STCNT (20)	4 CLRSELINGO	4 SELINGO	4 RSVD	4 PHASEMIS	4 SEMPTY
3 STCNT (19)	3 CLRSWRAP	3 SWRAP	3 CLRBUSFREE	3 BUSFREE	3 SFULL
2 STCNT (18)	2 CLRSDONE	2 SDONE	2 CLRSCSIPERR	2 SCSIPERR	2 SFCNT (2)
1 STCNT (17)	1 CLRSPIORDY	1 SPIORDY	1 CLRPHASECHG	1 PHASECHG	1 SFCNT (1)
0 STCNT (16)	0 CLRDMADONE	0 DMADONE	0 CLRREQINIT	0 REQINIT	0 SFCNT (0)

$34E_h$ SCSITEST	$34E_h$ SSTAT3	$34F_h$ CLRSERR	$34F_h$ SSTAT4	350_h SIMODE0	351_h SIMODE1
W	R	W	R	R/W	R/W
7 RSVD	7 SCSICNT (3)	7 RSVD	7 RSVD	7 RSVD	7 ENSELTIMO
6 RSVD	6 SCSICNT (2)	6 RSVD	6 RSVD	6 ENSELDO	6 ENATNTARG
5 RSVD	5 SCSICNT (1)	5 RSVD	5 RSVD	5 ENSELDI	5 ENSCSIRST
4 RSVD	4 SCSICNT (0)	4 RSVD	4 RSVD	4 ENSELINGO	4 ENPHASEMIS
3 SCTESTU	3 OFFCNT (3)	3 RSVD	3 RSVD	3 ENSWRAP	3 ENBUSFREE
2 SCTESTD	2 OFFCNT (2)	2 CLRSYNCERR	2 SYNCERR	2 ENSDONE	2 ENSCSIPERR
1 RSVD	1 OFFCNT (1)	1 CLRFWERR	1 FWERR	1 ENSPIORDY	1 ENPHASECHG
0 STCTEST	0 OFFCNT (0)	0 CLRFRERR	0 FRERR	0 ENDMADONE	0 ENREQINIT

352_h DMACNTRL0	353_h DMACNTRL1	354_h DMASTAT	355_h FIFOSTAT	356_h DATAPORTL	356_h DATAPORTH
R/W	R/W	R	R	R/W	R/W
7 ENDMA	7 PWRDWN	7 ATDONE	7 FCNT (7)	7 DATAL (07)	15 DATAH (15)
6 8BIT/-16BIT	6 RSVD	6 WORDRDY	6 FCNT (6)	6 DATAL (06)	14 DATAH (14)
5 DMA/-PIO	5 RSVD	5 INTSTAT	5 FCNT (5)	5 DATAL (05)	13 DATAH (13)
4 RSVD	4 RSVD	4 DFIFOFULL	4 FCNT (4)	4 DATAL (04)	12 DATAH (12)
3 WRITE/-READ	3 STK (3)	3 DFIFOEMP	3 FCNT (3)	3 DATAL (03)	11 DATAH (11)
2 INTEN	2 STK (2)	2 RSVD	2 FCNT (2)	2 DATAL (02)	10 DATAH (10)
1 RSTFIFO	1 STK (1)	1 RSVD	1 FCNT (1)	1 DATAL (01)	9 DATAH (09)
0 SWINT	0 STK (0)	0 RSVD	0 FCNT (0)	0 DATAL (00)	8 DATAH (08)

358_h BRSTCNTRL	35A PORTA	35B PORTB	$35C_h$ REV	$35D_h$ STACK	$35E_h$ TEST
W	R/W	R/W	R	R/W	W
7 BON (3)	7 PADAT (7)	7 PBDAT (7)	7 RSVD	7 STKDAT (7)	7 RSVD
6 BON (2)	6 PADAT (6)	6 PBDAT (6)	6 RSVD	6 STKDAT (6)	6 BOFFTMR
5 BON (1)	5 PADAT (5)	5 PBDAT (5)	5 RSVD	5 STKDAT (5)	5 BONTMR
4 BON (0)	4 PADAT (4)	4 PBDAT (4)	4 RSVD	4 STKDAT (4)	4 STCNTH
3 BOFF (3)	3 PADAT (3)	3 PBDAT (3)	3 RSVD	3 STKDAT (3)	3 STCNTM
2 BOFF (2)	2 PADAT (2)	2 PBDAT (2)	2 REV (2)	2 STKDAT (2)	2 STCNTL
1 BOFF (1)	1 PADAT (1)	1 PBDAT (1)	1 REV (1)	1 STKDAT (1)	1 SCSIBLK
0 BOFF (0)	0 PADAT (0)	0 PBDAT (0)	0 REV (0)	0 STKDAT (0)	0 DMABLK

3.1 SCSI SEQUENCE CONTROL (SCSISEQ)

Register Type: R/W
Register Address: 340_h

This register controls the Selection/Reselection process for the AIC-6260. Each bit in this register enables a different portion of the Selection/Reselection process. This register can be read, allowing bit manipulation instructions without saving a register image in local scratch RAM. All bits, except SCSIRSTO (bit 0), are cleared by a SCSI Reset.

Bit	Field Name
7	TEMODEO
6	ENSELO
5	ENSELI
4	ENRESELI
3	ENAUTOATNO
2	ENAUTOATNI
1	ENAUTOATNP
0	SCSIRSTO

7 (0) **TEMODEO:** TARGET Enable Mode Out. TEMODEO is used in conjunction with ENSELO (bit 6). If TEMODEO is set, setting ENSELO initiates a Reselection Out sequence. If TEMODEO is cleared, setting ENSELO initiates a Selection Out sequence.

6 (0) **ENSELO:** Enable Selection Out. When ENSELO is set, the AIC-6260's SCSI logic performs either a Selection Out, or a Reselection Out, based on the state of TEMODEO. ENSELO is cleared by the processor or by a hard reset of the host.

5 (0) **ENSELI:** Enable Selection In. When ENSELI is set, it allows the AIC-6260 to respond to valid Selection In attempts.

4 (0) **ENRESELI:** Enable Reselection In. When ENRESELI is set, it allows the AIC-6260 to respond to valid Reselection In attempts. ENRESELI is reset by clearing it.

3 (0) **ENAUTOATNO:** Enable Auto Attention Out. When ENAUTOATNO is set, ATN is asserted during a Selection Out sequence (ENSELO=1, TEMODEO=0). This procedure is used when the AIC-6260 is the initiator and wants to follow Selection with a Message Out Phase. The processor can deassert ATN by setting CLRATNO (bit 6, $34C_h$, W). A Bus Free state on the SCSI bus also deasserts ATN. Clearing ENAUTOATNO does not deassert ATN.

2 (0) **ENAUTOATNI:** Enable Auto Attention In. With ENAUTOATNI set, ATN is asserted during a Reselection In sequence (ENRESELI=1). This procedure is used when the AIC-6260 is the initiator and wants to follow reselection with a Message Out phase. The processor can deassert ATN by setting CLRATNO (bit 6, $34C_h$, W). A Bus Free state on the SCSI bus also deasserts ATN. Clearing ENAUTOATNI does not deassert ATN.

1 (0) **ENAUTOATNP:** Enable Auto Attention Parity. When both ENAUTOATNP and ENSPCHK (bit 5, 342_h) are set, ATN is asserted if a parity error is detected on SC0–SC7 during the Data In, Message In, or Status In phases. The processor can deassert ATN by setting CLRATNO (bit 6, $34C_h$, W). A Bus Free state on the SCSI bus also deasserts ATN. Clearing ENAUTOATNP does not deassert ATN.

0 (0) **SCSIRSTO:** SCSI Reset Out. When SCSIRSTO is set, RST is asserted on the SCSI bus. The processor must deassert RST by clearing SCSIRSTO.

3.2 SCSI TRANSFER CONTROL 0 (SXFRCTL0)

Register Type: R/W
Register Address: 341_h

SCSI Transfer Control 0 to enables transfers between the SCSI bus and the host, via the SCSI and host FIFOs. This register also controls the selection of SCSI PIO mode as the transfer mode and enables the SCSI FIFO and SCSI transfer counter to clear.

Bit	Field Name
7	SCSIEN
6	DMAEN
5	CH1/CH2
4	CLRSTCNT
3	SPIOEN
2	RSVD.
1	CLRCH1
0	RSVD.

7 (0) **SCSIEN:** Transfer Enable. When SCSIEN is set, data can be transferred between the SCSI bus and the SCSI FIFO. Transfers are terminated by clearing SCSIEN. SCSIEN must be read back as a low before the transfer is considered halted. Synchronous data transfers are enabled whenever SOFS (bits 3–0, 344_h) is non-zero.

6 (0) **DMAEN:** FIFO Transfer Enable. When DMAEN is set, transfers between the SCSI FIFO and host FIFO are enabled.

5 (x) **CH1/CH2:** Channel Select. CH1/CH2 should always be set.

4 (0) **CLRSTCNT:** Clear SCSI Transfer Counter. When CLRSTCNT is set, the SCSI transfer count (SCXFRCNT, 348_h–$34A_h$) is set to 000000_h. The AIC-6260 generates a clear pulse, making it necessary to reset CLRSTCNT. CLRSTCNT is always read back as 0.

3 (0) **SPIOEN:** SCSI PIO Enable. When SPIOEN is set, SCSI PIO mode is used as the transfer mode. Once a SCSI PIO transfer is started, SPIOEN must remain set throughout the entire transfer. If SPIOEN is cleared at anytime during the transfer, the transfer will be halted without corrupting valid data in the data latch at 346_h.

2 (0) **RSVD:** RSVD. This bit always reads as 0.

1 (x) **CLRCH1:** Clear Channel 1. When CLRCH1 is set, the AIC-6260 generates a pulse to clear the SCSI FIFO, (bits 3–0 of $34E_h$), and the SCSI transfer count (348_h–$34A_h$).

0 (0) **RSVD:** RSVD. This bit always reads as 0.

3.3 SCSI TRANSFER CONTROL 1 (SXFRCTL1)

Register Type: R/W
Register Address: 342_h

SCSI Transfer Control 1 enables various transfer controls associated with SCSI transfers. This register controls the Selection/Reselection timer, byte alignment, and parity checking.

Bit	Field Name
7	BITBUCKET
6	SWRAPEN
5	ENSPCHK
4 3	STIMESEL
2	ENSTIMER
1	BYTEALIGN
0	RSVD.

7 (x) **BITBUCKET:** SCSI Bit Bucket Mode. When BITBUCKET is set, it allows the AIC-6260 to read data from the SCSI bus and throw it away, or supply 00h write data. In BITBUCKET mode, data is not saved and FIFO full or FIFO empty conditions do not cause transfer halts. BITBUCKET is enabled in initiator mode only.

6 (x) **SWRAPEN:** SCSI Wrap Enable. When SWRAPEN is set, the transfer count (registers $348_h - 34A_h$) can wrap past 0. This allows the transfer count to exceed a 24-bit value. When a transfer count wrap occurrs, SWRAP (bit 3, $34B_h$,R) is set. SWRAPEN is valid only in target mode.

NOTE: If the transfer counter has wrapped, and it is not the final wrap for the current transfer, clear SWRAP by setting CLRSWRAP (bit 3, 34Bh) and wait for it to be set again (indicating another counter wrap). When the last wrap has occurred, clear SWRAP by setting CLRSWRAP (bit 3, 34Bh), and clear SWRAPEN. Wait for SDONE to be set, indicating the transfer is complete.

5 (x) **ENSPCHK:** Enable Parity Check. When ENSPCHK is set, parity checking is enabled on the SCSI Bus. When ENSPCHK is cleared, SCSIPERR (bit 2, $34C_h$, R) always reads 0.

4–3 (x) **STIMESEL:** Set Selection Timeout. STIMESEL contains the selection timeout code. The selection timeout codes are defined in Table 3-2.

TABLE 3-2. STIMESEL VALUES

STIMESEL Bit 4	STIMESEL Bit 3	Timeout
0	0	256 ms
0	1	128 ms
1	0	64 ms
1	1	32 ms

2 (x) **ENSTIMER:** Enable Selection Timer. When ENSTIMER is set, the hardware selection timer is enabled. When the internal selection timer exceeds the timeout limit during a Selection Out or Reselection Out sequence, SEL is deasserted and SELTO (bit 7, $34C_h$, R) is set. If ENSELTIMO (bit 7, 351_h, R) is cleared, SEL will continue to be asserted until deasserted by the processor.

1 (x) **BYTEALIGN:** Byte Align. When BYTEALIGN is set, it forces a handshake between the host FIFO and the SCSI FIFO. Any data passed for this handshake is discarded. This procedure is used to align data when an odd byte boundary disconnect occurs during a write operation.

0 (0) **RSVD:** Reserved. This bit always reads as 0.

3.4 SCSI SIGNAL IN (SCSISIGI)

Register Type: R
Register Address: 343_h

This register reflects the current state of the SCSI control lines on the SCSI bus.

Bit	Field Name
7	CDI
6	IOI
5	MSGI
4	ATNI
3	SELI
2	BSYI
1	REQI
0	ACKI

7 (x) **CDI:** Command/Data In. The CDI bit reflects the state of the CD signal on the SCSI bus.

6 (x) **IOI:** Input/Output In. The IOI bit reflects the state of the IO signal on the SCSI bus.

5 (x) **MSGI:** Message In. The MSGI bit reflects the state of the MSG signal on the SCSI bus.

4 (x) **ATNI:** Attention In. The ATNI bit reflects the state of the ATN signal on the SCSI bus.

3 (x) **SELI:** Selection In. The SELI bit reflects the state of the SEL signal on the SCSI bus.

2 (x) **BSYI:** Busy In. The BSYI bit reflects the state of the BSY signal on the SCSI bus.

1 (x) **REQI:** Request In. The REQI bit reflects the state of the REQ signal on the SCSI bus.

0 (x) **ACKI:** Acknowledge In. The ACKI bit reflects the state of the ACK signal on the SCSI bus.

3.5 SCSI SIGNAL OUT (SCSISIGO)

Register Type: W
Register Address: 343_h

This register controls the actual or expected state of the SCSI control lines, depending on whether the AIC-6260 is in target or initiator mode. All bits in this register are cleared by Bus Free, SCSI Reset, or Hard Reset conditions.

bit	Field Name
7	CDO
6	IOO
5	MSGO
4	ATNO
3	SELO
2	BSYO
1	REQO
0	ACKO

7 (0) **CDO:** Command/Data Out. In target mode, CDO drives C/D on the SCSI bus. In initiator mode, CDO is the state of C/D expected for the next REQ pulse.

6 (0) **IOO:** Input/Output Out. In target mode, IOO drives I/O on the SCSI bus. In initiator mode, IOO is the state of I/O expected for the next REQ pulse.

5 (0) **MSGO:** Message Out. In target mode, MSGO drives MSG on the SCSI bus. In initiator mode, MSGO is the state of the MSG expected for the next REQ pulse.

4 (0) **ATNO:** Attention Out. In target mode, ATNO is not used. In initiator mode, driving ATNO high asserts ATN on the SCSI bus. ATN is deasserted by driving CLRATNO (bit 6, $34C_h$, W) high.

3 (0) **SELO:** Selection Out. When SELO is set, the AIC-6260 asserts SEL on the SCSI bus. This bit may be used to deassert SEL on the SCSI bus.

2 (0) **BSYO:** Busy Out. When BSYO is set, the AIC-6260 asserts BSY on the SCSI bus. This bit may be used to deassert BSY. BSYO is also set by the AIC-6260's SCSI logic during a Selection Out or Reselection Out sequence.

1 (0) **REQO:** Request Out. When REQO is set, the AIC-6260 asserts REQ on the SCSI bus. REQO is disabled in initiator mode.

0 (0) **ACKO:** Acknowledge Out. When ACKO is set, ACK is asserted on the SCSI bus. ACKO is disabled in target mode.

3.6 SCSI RATE CONTROL (SCSIRATE)

Register Type: W
Register Address: 344_h

The rate control register is used to control the timing and offset parameters for synchronous SCSI transfers. If SOFS is set to zero, SCSI transfers are asynchronous.

Bit	Field Name
7	RSVD
6 5 4	SXFR
3 2 1 0	SOFS

7 (0) **RSVD:** Reserved.

6–4 (x) **SXFR:** Synchronous Transfer Rate. SXFR is the synchronous transfer rate code. Table 3-3 defines the transfer rates and associated timing parameters for all valid transfer rate codes. Timing parameters are given for a 20MHz clock. For clock rates other than 20MHz, timing parameters are given in clock periods (T). Transfer rates at less than 2.22Mbs must be made in asynchronous mode.

TABLE 3-3. SXFR CODES

Code	REQ/ACK	PERIOD	RATE
0 1 0	100ns (2T)	200ns (4T)	5.00MbS
0 1 1	100ns (2T)	250ns (5T)	4.00MbS
1 0 0	100ns (2T)	300ns (6T)	3.33MbS
1 0 1	100ns (2T)	350ns (7T)	2.86MbS
1 1 0	100ns (2T)	400ns (8T)	2.50MbS
1 1 1	100ns (2T)	450ns (9T)	2.22MbS

3-0 (x) **SOFS:** SCSI Offset. SOFS contains the synchronous transfer offset. When SOFS is set to 0000_h, the SCSI transfer mode is asynchronous. Any other value is the offset for a SCSI synchronous transfer. SOFS must be loaded with the values derived from the SCSI synchronous transfer request negotiations. The AIC-6260 supports offsets of 1–8 bytes.

3.7 SELECTION/RESELECTION ID (SELID)

Register Type: R
Register Address: 345_h

When the AIC-6260 has been selected or reselected, the SCSI ID bits of the target and the initiator are set in this register.

Bit	Field Name
7	SELID7
6	SELID6
5	SELID5
4	SELID4
3	SELID3
2	SELID2
1	SELID1
0	SELID0

7–0 (x) **SELID:** Selection ID. These bits directly correspond to the SCSI IDs.

3.8 SCSI ID (SCSIID)

Register Type: W
Register Address: 345_h

This register contains the SCSI IDs of the AIC-6260 and the other unit (target or initiator) involved in the SCSI operation. Bits 6–4 always contain the AIC-6260's ID and bits 2–0 always contain the other unit's ID. This is true regardless of which unit is the initiator and which is the target.

Bit	Field Name
7	RSVD
6 5 4	OID
3	RSVD
2 1 0	TID

7 (0) **RSVD:** Reserved.

6–4 (x) **OID:** Own ID. OID is the AIC-6260's SCSI ID number .

3 (0) **RSVD:** Reserved.

2–0 (x) **TID:** Other ID. TID is the other unit's SCSI ID number.

3.9 SCSI LATCHED DATA (SCSIDAT)

Register Type: R/W
Register Address: 346_h

This register is the data latch used for manual or SCSI PIO data transfers. Data outbound from the AIC-6260 is written to this register. Data inbound to the AIC-6260 is read from this register.

Bit	Field Name
7	DB (MSB)
0	DB (LSB)

7–0 (x) **DB 7–0:** Data Bits 7–0. DB 7–0 are loaded with SCSI data. DB 7 is the most significant byte (MSB), and DB 0 is least significant byte (LSB).

3.10 SCSI DATA BUS (SCSIBUS)

Register Type: R
Register Address: 347_h

This register reflects the current state of the SCSI bus data lines. It is used during manual selection or reselection.

Bit	Field Name
7	SDB (MSB)
0	SDB (LSB)

7–0 (x) **SDB 7–0:** SCSI Data Bits 7–0. SDB 7–0 are loaded with SCSI data. SDB 7 is the MSB, and SDB 0 is the LSB.

3.11 SCSI TRANSFER COUNT 2–0 (STCNT0, STCNT1, STCNT2)

Register Type: R/W
Register Address: 348_h–$34A_h$

The transfer count register actually comprises three 8-bit registers, SCSI Transfer Count 0, 1, and 2. This register contains the data transfer count for the current SCSI operation. The LSB is loaded at 348h. The MSB is loaded at $34A_h$.

In target mode, this register is loaded with the number of bytes to be transferred. The transfer counter counts down from the value loaded for each REQ pulse asserted.

In initiator mode, this register counts the number of bytes sent or received, counting up for each ACK pulse received. For transactions involving disconnection and reconnection, this register can be loaded with the current (remaining) transfer count of the transaction.

bit	Field Name
23 16	STCNT2 ($34A_h$)
15 8	STCNT1 (349_h)
7 0	STCNT0 (348_h)

23–16 (x) **STCNT2:** Most Significant Byte. STCNT2 contains the most significant 8 bits of the SCSI transfer count.

15–8 (x) **STCNT1:** Middle Byte. STCNT1 contains the middle 8 bits of the SCSI transfer count.

7–0 (x) **STCNT0:** Least Significant Byte. STCNT0 contains the least significant 8 bits of the SCSI transfer count.

3.12 SCSI INTERRUPT STATUS 0

Register Type: R
Register Address: $34B_h$

This register reflects the state of eight SCSI status bits. If the interrupts corresponding to these status bits are enabled, Interrupts are generated when the status bits are set. Interrupts are enabled using the SIMODE0 register (350_h) and cleared using the CLRSINT0 register ($34B_h$). The status bits in this register are available regardless of the condition of the enable bits. Clearing an interrupt does not necessarily clear the status bit; the means by which a status bit may be cleared is specified for each bit. The clear bits also state specifically when they clear the associated status bit.

The TARGET bit is a status bit; no interrupt is generated when TARGET is set.

Refer to the discussion of interrupts in Section 4 of this manual for more information on the interrelation of status, interrupt, enable, and clear bits.

Bit	Field Name
7	TARGET
6	SELDO
5	SELDI
4	SELINGO
3	SWRAP
2	SDONE
1	SPIORDY
0	DMADONE

7 (x) **TARGET:** Target. When TARGET is set, the AIC-6260 is the target. TARGET is only valid after a selection or reselection has completed and before Bus Free.

This condition does not generate an interrupt.

6 (x) **SELDO:** Select Out Done. SELDO is set when the AIC-6260 has successfully completed Selection Out or Reselection Out. The state of TARGET determines whether the sequence was Selection Out or Reselection Out. When TARGET is cleared, SELDO indicates that a Selection Out sequence was completed. When TARGET is set, SELDO indicates that a Reselection Out sequence was completed.

SELDO is cleared by Bus Free.

This condition generates an interrupt if ENSELDO (bit 6, 350_h) is set.

5 (x) **SELDI:** Selection In Done. SELDI is set when the AIC-6260 has been selected or reselected. The state of TARGET determines whether the sequence was Selection In or Reselection In. When TARGET is set, SELDI indicates that a Selection In sequence was completed. When TARGET is cleared, SELDI indicates that a Reselection In sequence was completed. This condition generates an interrupt if ENSELDI (bit 5, 350_h) is set.

To enable clearing SELDI, CLRSELDI must first be set. A Bus Free condition will then clear SELDI. Note that CLRSELDI must be set to enable Bus Free to clear SELDI, whether or not ENSELDI has been set. This feature allows the initiator (target) to recognize that a Reselection (Selection) in sequence occurred, even if Bus Free occurred before it reads SELDI status.

4 (x) **SELINGO:** Selection Initiated Out. SELINGO is set when the AIC-6260 begins a Selection Out or Reselection Out sequence. SELINGO is set upon successful arbitration of the bus, and remains set throughout the Selection Out or Reselection Out sequence. When the Selection Out or Reselection Out sequence has completed, SELINGO is cleared.

This condition generates an interrupt if ENSELINGO (bit 4, 350_h) is set.

3 (x) **SWRAP:** Transfer Counter Wrap. SWRAP is set when the transfer counter (348_h–$34A_h$) wraps past 0.

In TARGET mode, SWRAPEN (bit 6, 342_h) must be set in order for the counter to wrap. SWRAP is set when the transfer counter decrements from 000001_h to 000000_h.

In Initiator mode, SWRAP is enabled at all times. SWRAP is set when the transfer counter increments from $FFFFFF_h$ to 000000_h.

SWRAP is cleared by setting CLRSWRAP (bit 3, $34B_h$).

This condition generates an interrupt if ENSWRAP (bit 3, 350_h) is set.

2 (x) **SDONE:** SCSI Done. SDONE is set when the transfer counter (348_h–$34A_h$) has counted down to 000000h, unless SWRAPEN (bit 6 of 342h) is set, in which case a transfer counter wrap occurs and the transfer continues. SDONE can be set by setting SETSDONE (bit 7, $34B_h$, W).

SDONE is never set in initiator mode, unless it was set prior to entering initiator mode.

SDONE is cleared by setting CLRSDONE (bit 2, $34B_h$).

To prevent false transfers, SCSIEN (bit 7, 341_h) must be cleared before SDONE is cleared.

This condition generates an interrupt if ENSDONE (bit 2, 350_h) is set.

1 (x) **SPIORDY:** SCSI PIO Ready. SPIORDY is set when data is ready to be transferred on the SCSI bus. In initiator mode, SPIORDY is set when REQ is asserted. In target mode, SPIORDY is set when ACK is asserted.

On outbound transfers, SPIORDY is cleared on a write to the SCSI data latch (346_h). On inbound transfers, SPIORDY is cleared on a read from the SCSI data latch (346_h).

This condition generates an interrupt if ENSPIORDY (bit 1, 350_h) is set.

0 (x) **DMADONE:** DMADONE is only valid in DMA mode. For transfers to the SCSI bus, DMADONE is set when both the SCSI FIFO and the host FIFO are empty, and terminal count (T/C) has been asserted by the host DMA controller. For transfers from the SCSI bus, DMADONE is set when terminal count (T/C) has been asserted by the host DMA controller.

This condition generates an interrupt if ENDMADONE (bit 0, 350_h) is set.

3.13 CLEAR SCSI INTERRUPTS 0 (CLRSINT0)

Register Type: W
Register Address: $34B_h$

This register (except for bit 7) clears the interrupts associated with the status bits in SSTAT0 ($34B_h$). Setting any of these bits clears the corresponding interrupt and deasserts IRQ. IRQ may not be deasserted if there are other interrupts active. A clear bit does not need to be cleared before it can be set again. Writing a zero to any bit in this register has no effect.

Bit 7 of this register is used to generate the SDONE interrupt.

Clearing an interrupt does not necessarily clear the status bit associated with the condition which caused the interrupt.

Bit	Field Name
7	SETSDONE
6	CLRSELDO
5	CLRSELDI
4	CLRSELINGO
3	CLRSWRAP
2	CLRSDONE
1	CLRSPIORDY
0	CLRDMADONE

7 (1) **SETSDONE:** Set SCSI Transfer Done. When SETSDONE is set, SDONE (bit 2, $34B_h$, R) is set and, if ENSDONE is set, IRQ is asserted.

6 (1) **CLRSELDO:** Clear Selection Out Done. When CLRSELDO is set, the SELDO interrupt is cleared.

5 (1) **CLRSELDI:** Clear Selection Done In. When CLRSELDI is set, the SELDI interrupt is cleared.

4 (1) **CLRSELINGO:** Clear Selection. When CLRSELINGO is set, the SELINGO interrupt is cleared.

3 (1) **CLRSWRAP:** Clear Wrap. When CLRSWRAP is set, the SWRAP interrupt is cleared. Also clears SWRAP status bit ($34B_h$, bit 3).

2 (1) **CLRSDONE:** Clear SCSI Done. When CLRSDONE is set, the SDONE interrupt is cleared. Also clears SDONE status bit ($34B_h$, bit 2).

1 (1) **CLRSPIORDY:** Clear SCSI PIO Ready. When CLRSPIORDY is set, the SPIORDY interrupt is cleared.

0 (1) **CLRDMADONE:** Clear DMA Done. When CLRDMADONE is set, the DMADONE interrupt is cleared.

3.14 SCSI STATUS 1 (SSTAT1)

Register Type: R
Register Address: $34C_h$

This register reflects the state of eight SCSI status bits. If the interrupts corresponding to these status bits are enabled, interrupts are generated when the status bits are set. Interrupts are enabled using the SIMODE1 register (351_h) and cleared using the CLRSINT1 register (34Ch). The status bits in this register are available regardless of the condition of the enable bits. Clearing an interrupt does not necessarily clear the status bit; the means by which a status bit may be cleared is specified for each bit. The clear bits also state specifically when they clear the associated status bit.

Refer to the discussion of interrupts in Section 4 of this manual for more information on the interrelation of status, interrupt, enable, and clear bits.

Bit	Field Name
7	SELTO
6	ATNTARG
5	SCSIRSTI
4	PHASEMIS
3	BUSFREE
2	SCSIPERR
1	PHASECHG
0	REQINIT

7 (0) **SELTO:** Selection Timeout Expired. SELTO is set when a Selection Out or Reselection Out timeout has occurred and ENSTIMER (bit 2, 342_h)is set.

SELTO is cleared by setting CLRSELTIMO (bit 7 of $34C_h$).

This condition generates an interrupt if ENSELTIMO (bit 7, 351h) is set.

6 (0) **ATNTARG:** Target Attention. ATNTARG is only valid in target mode. ATNTARG is set when the initiator has asserted ATN.

ATNTARG is cleared when the initiator deasserts ATN.

This condition generates an interrupt if ENATNTARG (bit 6, 351_h) is set.

5 (0) **SCSIRSTI:** SCSI Reset In. SCSIRSTI is set when a bus reset occurs on the SCSI bus. SCSIRSTI remains set until cleared by setting CLRSCSIRSTI (bit 5, $34C_hW$) high.

This condition generates an interrupt if ENSCSIRST (bit 5, 351_h) is set.

4 (0) **PHASEMIS:** Phase Mismatch. PHASEMIS is only valid in initiator mode. PHASEMIS is set when the expected phase loaded in the SCSISIGI register (bits 7–5, 343_h) does not match the phase active on the SCSI bus. PHASEMIS is qualified by REQINIT (bit 0 of this register).

PHASEMIS is cleared when the phase active on the SCSI bus matches the expected phase loaded in the SCSISIGI register.

This condition generates an interrupt if ENPHASEMIS (bit 4, 351_h) is set.

3 (0) **BUSFREE:** Bus Free. BUSFREE is set when both BSY and SEL have been negated for 400 nsec (8T).

BUSFREE is cleared by setting CLRBUSFREE (bit 3, $34C_h$).

This condition generates an interrupt if ENBUSFREE (bit 3, 351_h) is set.

2 (0) **SCSIPERR:** Parity Error. SCSIPERR is set when a parity error is detected during an inbound Information Transfer phase and ENSPCHK is set. If ENSPCHK (bit 5, 342_h) is cleared, SCSIPERR is always 0.

In target mode, parity is sampled on the leading edge of ACK.

In initiator mode, parity is sampled on the leading edge of REQ.

SCSIPERR is cleared by setting CLRSCSIPERR (bit 2, $34C_h$, W). After driving CLRSCSIPERR high, SCSIPERR reflects the parity of the last byte transferred on the bus.

This condition generates an interrupt if ENSCSIPERR (bit 2, 351_h) is set.

1 (0) **PHASECHG:** Phase Change. PHASECHG is only valid in initiator mode. PHASECHG is set when the expected phase loaded in the SCSI Signal In register (bits 7–5, 343_h) does not match the phase active on the SCSI bus.

PHASECHG is cleared by setting CLRPHASECHG (bit 2, $34C_h$, W).

This condition generates an interrupt if ENPHASECHG (bit 1, 351_h) is set.

0 (0) **REQINIT:** REQ Initiated. REQINIT is only valid in initiator mode. REQINIT is set when the AIC-6260 detects the leading edge of REQ.

REQINIT is cleared by setting when ACK is asserted on the bus, or when CLRREQINIT (bit 0, $34C_h$, W) is set.

This condition generates an interrupt if ENREQINIT (bit 0, 351_h) is set.

3.15 CLEAR SCSI INTERRUPTS 1 (CLRSINT1)

Register Type: W
Register Address: $34C_h$

This register clears the interrupts associated with the status bits in SSTAT1 ($34C_h$). Setting any of these bits (except bit 6) clears the corresponding interrupt and deasserts IRQ. IRQ may not be deasserted if there are other interrupts active. A clear bit does not need to be cleared before it can be set again. Setting bit 6 clears ATN. Writing a zero to any bit in this register has no effect.

Clearing one of these interrupts *does* clear the status bit associated with the condition which caused the interrupt.

Bit	Field Name
7	CLRSELTIMO
6	CLRATNO
5	CLRSCSIRSTI
4	RSVD.
3	CLRBUSFREE
2	CLRSCSIPERR
1	CLRPHASECHG
0	CLRREQINIT

7 (1) **CLRSELTIMO:** Clear Selection Timeout. When CLRSELTIMO is set, the SELTO interrupt and the SELTO status bit (bit 7, $34C_h$, R) are cleared.

6 (1) **CLRATNO:** Clear Attention Out. When CLRATNO is set, ATN is cleared.

5 (1) **CLRSCSIRSTI:** Clear SCSI Reset In. When CLRSCSIRSTI is set, the SCSIRSTI interrupt and the SCSIRSTI status bit (bit 5, $34C_h$, R) are cleared.

4 (0) **RSVD:** Reserved. This bit always reads as 0.

3 (1) **CLRBUSFREE:** Clear Bus Free. When CLRBUSFREE is set, the BUSFREE interrupt and the BUSFREE status bit (bit 3, $34C_h$, R) are cleared.

2 (1) **CLRSCSIPERR:** Clear SCSI Parity Error. When CLRSCSIPERR is set, the SCSIPERR interrupt and the SCSIPERR status bit (bit 2, $34C_h$, R) are cleared.

1 (1) **CLRPHASECHG:** Clear Phase Change. When CLRPHASECHG is set, the PHASECHG interrupt and the PHASECHG status bit (bit 1, $34C_h$, R) are cleared.

0 (1) **CLRREQINIT:** Clear REQ Initiated. When CLRREQINIT is set, the REQINIT interrupt and the REQINIT status bit (bit 0, $34C_h$, R) are cleared.

3.16 SCSI STATUS 2 (SSTAT2)

Register Type: R
Register Address: $34D_h$

This register reflects the status of the SCSI FIFO.

Bit	Field Name
7 6	RSVD
5	SOFFSET
4	SEMPTY
3	SFULL
2 1 0	SFCNT

7 (0) **RSVD:** Reserved.

6 (0) **RSVD:** Reserved. This bit always reads as 0.

5 (x) **SOFFSET:** SCSI Offset. If SOFFSET is set, it indicates that the REQ/ACK offset for a synchronous SCSI transfer is non-zero. When SOFFSET is cleared, it indicates that the REQ/ACK offset is zero (meaning the full transfer count has been sent or received).

4 (x) **SEMPTY:** SCSI FIFO Empty. If SEMPTY is set, it indicates that the SCSI FIFO is empty.

3 (x) **SFULL:** SCSI FIFO Full. If SFULL is set, it indicates that the SCSI FIFO is full.

2–0 (x) **SFCNT:** SCSI FIFO Count. SFCNT is loaded with a count of the number of bytes in the SCSI FIFO. If SFCNT is 000_h, the SCSI FIFO Full or SCSI FIFO Empty bits determine whether the SCSI FIFO is full or empty.

3.17 SCSI STATUS 3 (SSTAT3)

Register Type: R
Register Address: $34E_h$

This register contains status information on the state of the current synchronous SCSI transfer.

WARNING: DO NOT READ THIS REGISTER UNLESS ALL TRANSFERS ARE STOPPED.

Bit	Field Name
7 6 5 4	SCSICNT
3 2 1 0	OFFCNT

7–4 (0) **SCSICNT:** Count Difference. SCSICNT is loaded with the difference in the value of SFCNT and OFFCNT.

3–0 (0) **OFFCNT:** Offset Count. OFFCNT contains the current value of the offset counter. This is a count of the number of REQs received for which no ACKs have been issued.

3.18 SCSI TEST CONTROL (SCSITEST)

Register Type: W
Register Address: $34E_h$

This register is used to initiate test modes in the internal AIC-6260 SCSI logic.

WARNING: DO NOT WRITE TO THIS REGISTER DURING NORMAL OPERATION.

Bit	Field Name
7 6 5 4	RSVD
3	SCTESTU
2	SCTESTD
1	RSVD
0	STCTEST

7–4 (x) **RSVD:** Reserved.

3 (x) **SCTESTU:** SCSI Transfer Count Up. When SCTESTU is set, the SCSI transfer counter counts up at the input clock rate.

2 (x) **SCTESTD:** SCSI Transfer Count Down. When SCTESTD is set, the SCSI transfer counter counts down at the input clock rate.

1 (0) **RSVD:** Reserved.

0 (x) **STCTEST:** SCSI Transfer Count Test. When STCTEST is set, a stage-to-stage carry true is forced in both the transfer and select abort counters, which causes both counters to run at the clock rate. During the transfer count test, the counter contents can be monitored by reading the desired stage. If STCTEST and ENSTIMER (bit 2, 342_h) are both high, then the SCSI Transfer Count read register (bits 5–0, 348_h) is reassigned to the Select Abort Counter in the following manner:

TABLE 3-4. STCTEST TRANSFER COUNT READ REGISTER (bits 0–5) TO SELECT ABORT COUNTER REASSIGNMENTS

Bit	Assignment
5	Stage 6 (/2, output)
4	Stage 5 (/2, output)
3	Stage 4 (/10, output)
2	Stage 3 (/10, carry out)
1	Stage 2 (/256, carry out)
0	Stage 1 (/256, carry out)

3.19 SCSI STATUS 4 (SSTAT4)

Register Type: R
Register Address: $34F_h$

This register contains status information on error conditions for the current SCSI transfer.

Bit	Field Name
7 6 5 4 3	RSVD
2	SYNCERR
1	FWERR
0	FRERR

7–3 (0) **RSVD:** Reserved. This field always reads as 0000_h.

2 (0) **SYNCERR:** Synchronous Transfer Error. SYNCERR is set for one of the following two conditions:

1) At the beginning of an inbound synchronous transfer, when the SCSI FIFO is not empty prior to the transfer of the first byte off the SCSI bus. This condition may cause the SCSI FIFO to overflow, as SCSICNT (bits 7–4, $34E_h$, R) is not correct.

2) At the beginning of a synchronous transfer, SOFFSET (bit 5, $34D_h$) is set. This condition indicates that the previous transfer did not complete successfully.

1 (0) **FWERR:** FIFO Write Error. FWERR is set when more than one source is enabled to write to the SCSI FIFO. This error can arise under the following condition:

The transfer path is set up to send data from the host FIFO, through the SCSI FIFO, onto the SCSI bus, with the AIC-6260 reselected as an Initiator and the target driving I/O such that data is enabled SCSI bus-to-SCSI FIFO (Data In phase).

0 (0) **FRERR:** FIFO Read Error. The FRERR bit is set when more than one source is enabled to read from the SCSI FIFO.

3.20 CLEAR SCSI ERRORS (CLRSERR)

Register Type: W
Register Address: $34F_h$

This register clears the error condition status bits in SSTAT4 ($34F_h$). Setting any of these bits clears the corresponding status bit. A clear bit does not need to be cleared before it can be set again. Writing a zero to any bit in this register has no effect.

Bit	Field Name
7 6 5 4 3	RSVD
2	CLRSYNCERR
1	CLRFWERR
0	CLRFRERR

7–3 (0) **RSVD:** Reserved.

2 (0) **CLRSYNCERR:** Clear Synchronous Transfer Error. When CLRSYNCERR is set, the SYNCERR status bit is cleared (bit 2, $34F_h$, R).

1 (0) **CLRFWERR:** Clear FIFO Write Error. When CLRFWERR is set, the FWERR status bit is cleared (bit 1, $34F_h$, R).

0 (0) **CLRFRERR:** Clear FIFO Read Error. When CLRFRERR is set, the FRERR status bit is cleared (bit 0, $34F_h$, R).

3.21 SCSI INTERRUPT MODE 0 (SIMODE0)

Register Type: R/W
Register Address: 350_h

This register enables the interrupts associated with the status bits in SSTAT0 ($34B_h$). Setting any of these bits enables the corresponding interrupt. If an event occurs that causes a status bit to be set, and the enable bit for that condition is set, IRQ is asserted.

Clearing an enable bit causes the interrupt associated with the condition to be masked. However, the status bit associated with the condition is still set, regardless of the state of the enable bits.

Bit	Field Name
7	RSVD
6	ENSELDO
5	ENSELDI
4	ENSELINGO
3	ENSWRAP
2	ENSDONE
1	ENSPIORDY
0	ENDMADONE

7 (0) **RSVD:** Reserved. This bit always reads as 0.

6 (x) **ENSELDO:** Enable Selection Done Out Interrupt. If ENSELDO is set, the SELDO interrupt is generated when SELDO (bit 6, $34B_h$, R) is set.

5 (x) **ENSELDI:** Enable Selection Done In Interrupt. If ENSELDI is set, the SELDI interrupt is generated when SELDI (bit 5, $34B_h$, R) is set.

4 (x) **ENSELINGO:** Enable Selection Initiated Out Interrupt. If ENSELINGO is set, the SELINGO interrupt is generated when SELINGO (bit 4, $34B_h$, R) is set.

3 (x) **ENSWRAP:** Enable Wrap Interrupt. If ENSWRAP is set, the SWRAP interrupt is generated when SWRAP (bit 3, $34B_h$, R) is set.

2 (x) **ENSDONE:** Enable SCSI Done Interrupt. If ENSDONE is set, the SDONE interrupt is generated when SDONE (bit 2, $34B_h$, R) is set.

1 (x) **ENSPIORDY:** Enable SCSI PIO Ready Interrupt. If ENSPIORDY is set, the SPIORDY interrupt is generated when SPIORDY (bit 1, $34B_h$, R) is set.

0 (x) **ENDMADONE:** Enable DMA Done Interrupt. If ENDMADONE is set, the DMADONE interrupt is generated when DMADONE (bit 0, $34B_h$, R) is set.

3.22 SCSI INTERRUPT MODE 1 (SIMODE1)

Register Type: R/W
Register Address: 351_h

This register enables the interrupts associated with the status bits in SSTAT1 ($34C_h$). Setting any of these bits enables the corresponding interrupt. If an event occurs causing a status bit to be set, and the enable bit for that condition is set, IRQ is asserted.

Clearing an enable bit causes the interrupt associated with the condition to be masked. However, the status bit associated with the condition is still set, regardless of the state of the enable bits.

Bit	Field Name
7	ENSELTIMO
6	ENATNTARG
5	ENSCSIRST
4	ENPHASEMIS
3	ENBUSFREE
2	ENSCSIPERR
1	ENPHASECHG
0	ENREQINIT

7 (x) **ENSELTIMO:** Enable Selection Timeout Interrupt. If ENSELTIMO is set, the SELTO interrupt is generated when SELTO (bit 7, $34C_h$, R) is set.

6 (x) **ENATNTARG:** Enable Target Attention Interrupt. If ENATNTARG is set, the ATNTARG interrupt is generated when ATNTARG (bit 6, $34C_h$, R) is set.

5 (x) **ENSCSIRST:** Enable SCSI Reset Interrupt. If ENSCSIRST is set, the SCSIRSTI interrupt is generated when SCSIRSTI (bit 5, $34C_h$, R) is set.

4 (x) **ENPHASEMIS:** Enable Phase Mismatch Interrupt. If ENPHASEMIS is set, the PHASEMIS interrupt is generated when PHASEMIS (bit 4, $34C_h$, R) is set.

3 (x) **ENBUSFREE:** Enable Bus Free Interrupt. If ENBUSFREE is set, the BUSFREE interrupt is generated when BUSFREE (bit 3, $34C_h$, R) is set.

2 (x) **ENSCSIPERR:** Enable SCSI Parity Error Interrupt. If ENSCSIPERR is set, the SCSIPERR interrupt is generated when SCSIPERR (bit 2, $34C_h$, R) is set.

1 (x) **ENPHASECHG:** Enable Phase Change Interrupt. If ENPHASECHG is set, the PHASECHG interrupt is generated when PHASECHG (bit 1, $34C_h$, R) is set.

0 (x) **ENREQINIT:** Enable REQ Initiated Interrupt. When ENREQINIT is set, the REQINIT interrupt is generated when REQINIT (bit 0, $34C_h$, R) is set.

3.23 DMA CONTROL 0 (DMACNTRL0)

Register Type: R/W
Register Address: 352_h

This register contains the basic controls for PIO and DMA transfer modes. The bits which enable a mode may be set at the same time as the bits configuring the mode.

Bit	Field Name
7	ENDMA
6	8BIT/–16BIT
5	DMA/–PIO
4	RSVD
3	WRITE/–READ
2	INTEN
1	RSTFIFO
0	SWINT

7 (0) **ENDMA:** Enable DMA. When ENDMA is set, data transfer between host main memory and the host FIFO in either PIO or DMA mode is enabled.

Clearing ENDMA also clears ATDONE (bit 7, 354_h).

6 (x) **8BIT/–16BIT:** 8-Bit/–16-Bit Mode. When this bit is set, transfers between host main memory and the host FIFO are 8 bits wide and utilize SD0–SD7. When this bit is cleared, transfers between host main memory and the host FIFO are 16 bits wide and utilize SD0–SD15. Transfers utilizing host DMA mode are 8 bits wide.

5 (x) **DMA/–PIO:** DMA/–PIO Mode . When this bit is set, transfers between host main memory and the host FIFO are in DMA mode. When this bit is cleared, transfers between host main memory and the host FIFO are in PIO mode.

NOTE: When changing from PIO to DMA with ENDMA = 1, any direction change must be done first (bit 3 below.)

4 (0) **RSVD:** Reserved. This bit always reads 0.

3 (x) **WRITE/–READ:** Transfer Direction. When this bit is set, data is transferred from host main memory to the host FIFO . When this bit is cleared, data is transferred from the host FIFO to host main memory.

2 (x) **INTEN:** Master Interrupt Enable. INTEN controls the assertion of the IRQ pin. If INTEN is set, interrupts function normally. If INTEN is cleared, all interrupts are masked.

1 (x) **RSTFIFO:** Reset FIFO Counter. When RSTFIFO is set, the FIFO counter (bits 7–0, 355_h) is cleared. RSTFIFO is a self-clearing bit.

0 (x) **SWINT:** Software Interrupt. If INTEN is set, setting SWINT asserts IRQ. This bit is provides for software-generated interrupts.

3.24 DMA CONTROL 1 (DMACNTRL1)

Register Type: R/W
Register Address: 353_h

This register is used to set the power-down feature and write the stack offset pointer.

Bit	Field Name
7	PWRDWN
6 5 4	RSVD
3 2 1 0	STK

7 (0) **PWRDWN:** Power Down. When PWRDWN is set, the internal clock is stopped to conserve power. Once the clock is stopped, the AIC-6260 is not operational.

6–4 (0) **RSVD:** Reserved.

3–0 (x) **STK:** Stack Offset Pointer. STK contains the stack offset pointer. This field is write-only.

3.25 DMA STATUS (DMASTAT)

Register Type: R
Register Address: 354_h

This register reflects the real-time status of the current DMA or PIO transfer.

Bit	Field Name
7	ATDONE
6	WORDRDY
5	INTSTAT
4	DFIFOFULL
3	DFIFOEMP
2 1 0	RSVD

7 (x) **ATDONE:** host Done. ATDONE is used in DMA mode only. This bit is set when the host DMA controller has transferred the last byte or word and asserted T/C. While ATDONE is set, the internal host DMA logic is disabled; the host DMA logic remains disabled until this bit is cleared. ATDONE is cleared when ENDMA (bit 7, 352_h) is cleared.

ATDONE does not generate an interrupt.

6 (x) **WORDRDY:** Word Ready. WORDRDY is used in PIO mode only. When WORDRDY is set, a 16-bit word is ready for transfer to or from the host FIFO. If the transfer count for a particular transfer does not equal or end on a 128-byte boundary, the host must transfer data into or out of the host FIFO one word at a time; this bit is used to control that process.

5 (x) **INTSTAT:** Interrupt Status. INTSTAT is the OR of all enabled interrupts. INTSTAT may be read at any time, whether or not interrupts have been enabled via INTEN. This provides a means to poll for interrupts.

4 (x) **DFIFOFULL:** host FIFO Full. DFIFOFULL is set when the host FIFO is full. DFIFOFULL is used during SCSI-to-host PIO transfers.

3 (x) **DFIFOEMP:** host FIFO Empty. DFIFOEMP is set when the host FIFO is empty. DFIFOEMP is used during host-to-SCSI PIO transfers.

2–0 (0) **RSVD:** Reserved.

3.26 FIFO STATUS (FIFOSTAT)

Register Type: R
Register Address: 355_h

This register provides a count of the current number of bytes in the host FIFO.

Bit	Field Name
7	FCNT (MSB)
0	FCNT (LSB)

7–0 (x) **FCNT:** FIFO Count. FCNT contains a count of the of bytes in the host FIFO.

NOTE: The host FIFO is 128 bytes deep. Under some circumstances, the host FIFO may hold up to 4 additional bytes (132 bytes). FCNT contains the correct count in these circumstances.

3.27 DATA PORT (DATAPORTL and DATAPORTH)

Register Type: R/W
Register Address: 356_h

Data transfers between the AIC-6260 and the host take place via this register in both DMA and PIO mode. DMA transfers are 8-bit only. host PIO transfers are 8- or 16-bit, as defined by the state of SBHE. If SBHE is not active, 8 bits will be transferred via the low order data byte; if SBHE is active, 16 bits will be transferred.

Bit	Field Name
15	DATAH (MSB)
14	
13	
12	
11	
10	
9	
8	DATAH (LSB)
7	DATAL (MSB)
6	
5	
4	
3	
2	
1	
0	DATAL (LSB)

15–8 (x) **DATAH:** High-Order Data Byte. This byte is valid only if 8BIT/–16BIT (bit 6, 352_h) is cleared or SBHE is asserted.

7–0 (x) **DATAL:** Low-Order Data Byte.

3.28 BURST CONTROL (BRSTCNTRL)

Register Type: R/W
Register Address: 358_h

This register controls the burst on and burst off times for DMA transfers. The AIC-6260 will run as many Burst On/Burst Off cycles as necessary to transfer all data. To disable the BON and BOFF timers, load both BON and BOFF with 0000_h.

Bit	Field Name
7 6 5 4	BON
3 2 1 0	BOFF

7–4 (x) **BON:** Burst On. BON contains the maximum value, in microseconds, of the transmission (burst) period. The AIC-6260 bursts data for the duration of BON, or until all data has been sent, whichever is less. BON may range from 0 (none) to 15 microseconds.

3–0 (x) **BOFF:** Burst Off. BOFF contains the minimum value, in microseconds, of the off-line (down) period. The AIC-6260 will not request DMA service for at least the duration of BOFF. BOFF may range from 0 (none) to 15 microseconds.

3.29 PORT A (PORTA)

Register Type: R/W
Register Address: $35A_h$

This register provides an external 8- or 16-bit port which may be accessed at any time. Port A is user-defined.

3.30 PORT B (PORTB)

Register Type: R/W
Register Address: $35B_h$

This register provides an external 8- or 16-bit port which may be accessed at any time. Port B is user-defined.

3.31 REVISION (REV)

Register Type: R
Register Address: $35C_h$

This register gives the revision level of the chip in bits 2–0. Revision level 1 returns a value of 0_h.

3.32 STACK (STACK)

Register Type: R/W
Register Address: $35D_h$

This register is a 16-byte stack for general purpose memory use. The stack port may be addressed by writing to the lower 4 bits of DMACNTRL1 (353h). The offset points to the first location in the stack to be read from or written to. This allows the software to directly access any byte in the stack. Successive reads or writes access the next higher location in the stack.

3.33 TEST REGISTER (TEST)

Register Type: W
Register Address: $35E_h$

This register is used for test purposes only, and should not be written to during normal operation. During testing, either SCSIBLK or DMABLK should be set, but not both bits. To operate a specific test, one bit of bits 6–2 may be set.

Bit	Field Name
7	RSVD
6	BOFFTMR
5	BONTMR
4	STCNTH
3	STCNTM
2	STCNTL
1	SCSIBLK
0	DMABLK

7 (0) **RSVD:** Reserved.

6 (x) **BOFFTMR:** Buffer Off Timer. When BOFFTMR is set with either SCSIBLK or DMABLK set, the BOFFTMR [7:0] to SCD [7:0] test path is enabled.

5 (x) **BONTMR:** Buffer On Timer. When BONTMR is set with either SCSIBLK or DMABLK set, the BONTMR [7:0] to SCD [7:0] test path is enabled.

4 (x) **STCNTH:** SCSI Transfer High Count. When STCNTH is set with either SCSIBLK or DMABLK set, the SCSI transfer counter [23:16] to SD [15:8] test path is enabled.

3 (x) **STCNTM:** SCSI Transfer Mid Count. When STCNTM is set with either SCSIBLK or DMABLK set, the SCSI transfer counter [15:8] to SD [15:8] test path is enabled.

2 (x) **STCNTL:** SCSI Transfer Low Count. When STCNTL set with either SCSIBLK or DMABLK set, the SCSI transfer counter [7:0] to SD [15:8] test path is enabled.

1 (x) **SCSIBLK:** SCSI Block. When SCSIBLK is set, the internal AIC-6260 SCSI logic is configured for testing. Pin redefinitions are given in Table 3-5.

0 (x) **DMABLK:** DMA Block. When DMABLK is set, the DMA logic is configured for testing. Pin redefinitions are given in Table 3-6.

TABLE 3-5. SCBLK TESTR PIN REDEFINITIONS

AT Pins	Type	Test Pins	Module
SA[9:0]	INPUT	—	—
AEN	INPUT	WRITE1	INPUT-SCSI
PRIMARY	INPUT	DACK1	INPUT-SCSI
SD[15:8]	BIDI	DW/DR[7:0]	INPUT/OUTPUT SCSI
SD[7:0]	BIDI	—	
DACK	INPUT	—	
IOR	INPUT	—	
IOW	INPUT	—	
T/C	INPUT	HOSTDONE	INPUT-SCSI
SBHE	INPUT	DMAEMPTY	INPUT-SCSI
RESET	INPUT	—	
X1	INPUT	—	
DRQ	OUTPUT	—	
IRQ	OUTPUT	—	
PORTA	OUTPUT	SFAVAIL	OUTPUT-SCSI
PORT B	OUTPUT	DMAEN	OUTPUT-SCSI
X2	OUTPUT	—	
F1	OUTPUT	—	

TABLE 3-6. DMABLK TESTR PIN REDEFINITIONS

SCSI Pins	Type	Test Pins	Module
SCD[7:0]	BIDI	DW/DR[7:0]	INPUT/OUTPUT DMA
SCDP	BIDI	WRITE1	OUTPUT-DMA
RST	BIDI	DACK1	OUTPUT-DMA
ATN	BIDI	DMAEMPTY	OUTPUT-DMA
BSY	BIDI	INTL	INPUT-DMA
SEL	BIDI	DMAEN	INPUT-DMA
C/D[1]	BIDI	SFAVAIL	INPUT-DMA
I/O[2]	BIDI	ENABLE	INPUT-DMA
MSG	BIDI	ENABLE	INPUT-DMA
REQ	BIDI	—	
ACK	BIDI	—	

[1] I/O: In addition to setting bit 0, I/O must be set to enable DW1[7:0] on SCD [7:0]. The enable is only used when transferring data from the host to SCSI.

[2] MSG: MSG is used to enable WRITE1, DACK1, and DMAEMPTY.

The AIC-6260 is a single-chip SCSI Host Adapter with which the features and advantages of SCSI can be realized on the motherboard in PC AT systems. The AIC-6260 is an appropriate choice in systems ranging from laptops and notebooks all the way up to workstations.

The AIC-6260 has everything necessary to implement a SCSI interface in a single package. Through its register based host interface, it can be configured to operate as either a SCSI initiator or target with asynchronous or synchronous SCSI data transfers. To offload the host processor, SCSI data transfers may be performed with little or no host intervention using "SCSI Normal" transfer mode. Alternatively the host may have complete control over SCSI data transfers by selecting "SCSI Manual PIO" or "SCSI Automatic PIO" transfer mode.

Data transfers over the host bus may be accomplished using either "Host PIO" or "Second Party DMA" transfers. The AIC-6260 can be configured to generate interrupts for all timing critical SCSI operations. The AIC-6260 also provides a decoded address output simplifying the setup of 2 general purpose I/O ports(A and B). To aid in programming, the chip features a 16-byte stack accessible and controllable by the host processor.

4.1 GENERAL FUNCTIONAL DESCRIPTION

This section describes the general operation and major components of the AIC-6260. Figure 4-1 is a simplified block diagram of the device.

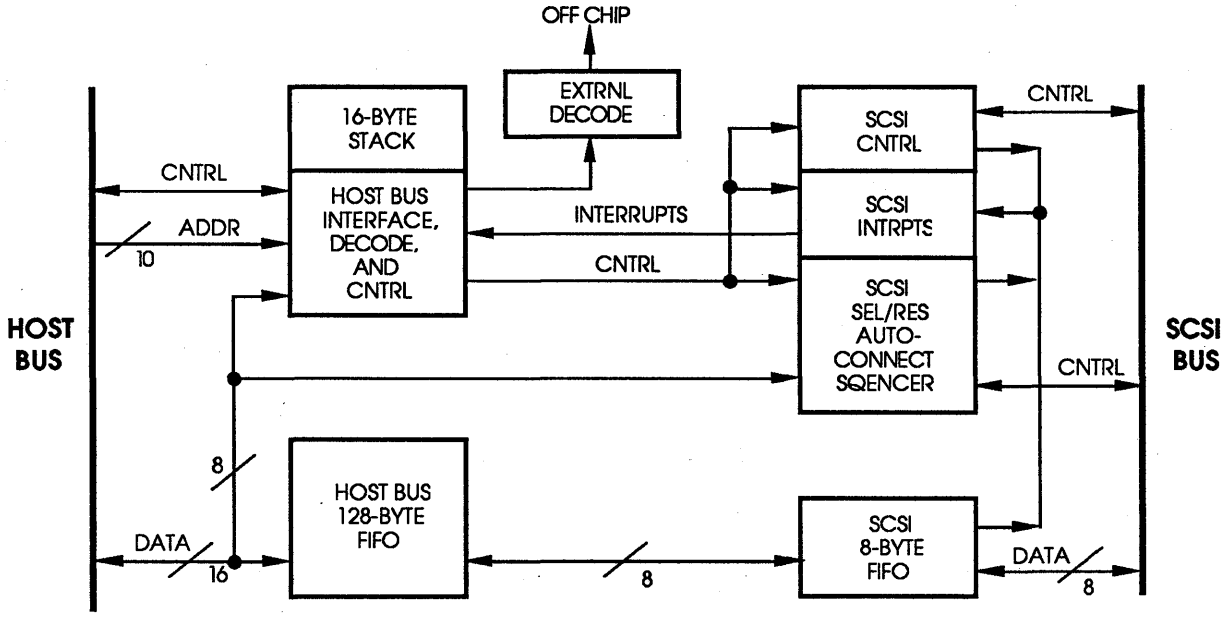


FIGURE 4-1. AIC-6260 SIMPLIFIED BLOCK DIAGRAM

4.1.1 SCSI Controller

The SCSI controller manages the interface to the SCSI bus, including control of SCSI data transfers and sequencing of all SCSI control signals. Through its intelligence, it can offload from the host processor most of the lower level responsibilities necessary to run the SCSI bus. However if desired, it can allow the host processor to directly manage and control the SCSI bus signals. The controller comprises the bulk of the AIC-6260's circuits including most of the control registers in the chip.

4.1.2 SCSI Interrupts

Interrupts are available for all timing critical SCSI operations. The interrupt circuitry provides the ability to individually mask, clear or poll the status of any interrupt condition. For detailed information on interrupts in the AIC-6260, see "Interrupts" later in this section, and the descriptions of the status, mask and clear registers in Section 3.

4.1.3 SCSI Selection/Reselection Autoconnect Sequencer

This section of the SCSI Controller provides the ability to have the AIC-6260 automatically Arbitrate for the SCSI bus and perform either a Selection or Reselection sequence. By taking advantage of this capability, the host processor can considerably simplify the task of running the SCSI interface.

Triggering of these automatic sequences is accomplished by setting appropriate bits in the SCSI SEQUENCE CONTROL REGISTER, 340h. However prior to starting an autoconnect sequence, the target/initiator IDs must first be set in the SCSI ID Register, 345h.

4.1.4 SCSI FIFO

The SCSI FIFO is an 8-byte data buffer used during "SCSI Normal" data transfers. Its main purpose is to buffer data during synchronous data transfers, allowing synchronous offsets of up to 8. The SCSI FIFO is not used when "SCSI Manual PIO" or "SCSI Automatic PIO" data transfer mode is selected as these transfer modes are typically used for SCSI Message, Status or Command phases where synchronous operation is prohibited. The status of the SCSI FIFO can be monitored by reading the SCSI STATUS 2 Register, 34Dh.

4.1.5 Address Mapping and External Decode

The AIC-6260 automatically maps itself onto the PC AT I/O bus by decoding 10 I/O address bits input to the chip for one of two I/O address ranges, 340h-35F or 140h-15Fh. This self mapping ability allows the AIC-6260 to directly connect to the PC AT I/O bus with no other support chips required. The selection of which range to decode for is under control of the ALTERNATE* input. Through these I/O address locations, the host processor controls all AIC-6260 operations and data transfers.

As part of the address mapping function, the decode logic also generates an off chip signal, PORTEN*, which is active low whenever either address 35Ah or 35Bh is valid (15Ah or 15Bh if the alternate address range is chosen).

The PORTEN* signal combined with some off chip logic as shown in "External Port Decode" later in this section, gives the user an easy means to implement two general purpose I/O ports.

4.1.6 Stack

To facilitate programming, a 16-byte stack in the AIC-6260 is available to the host processor. The stack pointer is located in register 353H and stack data may be written/read at register 35Dh.

4.1.7 Host Interface

The host interface consists of 32 read/write register locations internally mapped by the AIC-6260 as described earlier. Through them, the host may control all aspects of AIC-6260 operation.

4.1.8 Host FIFO

To facilitate data transfer performance, the AIC-6260 features an internal 128-byte data FIFO to buffer data between the host and the AIC-6260. The Host FIFO is used during either "Host PIO" or "Host DMA" data transfers provided that "SCSI Normal" data transfer mode is also selected. Otherwise if "SCSI Manual PIO" or "SCSI Automatic PIO" transfer modes are selected, host data is sent directly to/from the data latch at register 346h. The Host FIFO is 8 bits wide with conversions to 16-bit words performed as required by internal data path logic. Host FIFO operations may be monitored by reading the DMA STATUS Register, 354h and FIFO STATUS Register, 355h.

4.2 SCSI DATA TRANSFERS

The AIC-6260 can be programmed to operate as either a SCSI initiator or SCSI target by loading the SCSI SEQUENCE CONTROL REGISTER(340h) with the correct values. Note that some functions behave differently between initiator and target modes. To configure the chip for either initiator or target modes see Section 5.0, "Application Notes". The AIC-6260 can support both asynchronous and synchronous data transfers across the SCSI bus. To assist in data transfer control, a 24-bit transfer counter is available (Registers 348h, 349h, 34Ah) which will count each SCSI bus REQ/ACK handshake and generate an interrupt or status condition when terminal count is reached.

Data transfers through the AIC-6260 to the SCSI bus can be performed using one of three data transfer modes. Note that operational status in each mode can be monitored through interrupts or by polling for status.

- **SCSI Manual PIO:**
  In this mode, the host processor controls all aspects of the SCSI interface with the AIC-6260 acting merely as a bus buffer.

- **SCSI Automatic PIO:**
  In this mode, the host processor provides most of the control with the AIC-6260 providing automatic SCSI bus REQ/ACK handshaking.

- **SCSI Normal:**
  Utilizing the intelligence of the AIC-6260, this mode allows the host processor to offload the SCSI transfer operation to the AIC-6260. The AIC-6260 will run the SCSI interface and keep track of the transfer count after being initially set up by the host processor. This mode allows use of the AIC-6260 internal FIFOs for maximum transfer performance.

4.2.1 SCSI Manual PIO Mode

In SCSI manual PIO mode, the host processor reads or writes directly to the SCSI data bus via the latch at 346h and can monitor or control the SCSI bus control lines via the register at 343h. In this mode, the AIC-6260 is essentially a bus buffer having no control functions. Note that SCSI Manual mode supports asynchronous SCSI transfers only and that the internal data FIFOs are not used. This mode is typically used for SCSI Command, Message or Status phases where decision making and control are of primary importance rather than data transfer speed. To select this mode set SPIOEN=0 and DMAEN=0 (bits 3 & 6) in the SCSI Transfer Control 0 Register, 341h.

4.2.2 SCSI Automatic PIO Mode

In SCSI automatic PIO mode, the host processor writes or reads from the SCSI data bus via the latch at 346h, with the AIC-6260 handling the REQ/ACK handshaking to transfer data across the SCSI bus. The SPIORDY bit in the SCSI Interrupt Status 0 register at 34Bh signals transfer completion and can be polled or set to generate an interrupt. This mode supports asynchronous SCSI transfers only and bypasses the internal data FIFOs.

This mode is typically used for SCSI Command, Message or Status phases where decision making and control are of primary importance rather than data transfer speed. To select this mode, set SPIOEN=1 and DMAEN=0 (bits 3 & 6) in the SCSI Transfer Control 0 Register, 341h.

4.2.3 SCSI Normal Mode

In SCSI normal mode, the AIC-6260 will automatically handle the SCSI data transfer and provide the fastest transfer performance. In this mode, the internal FIFOs are used and the data path through the chip is from the host bus, through the host FIFO, through the SCSI FIFO and finally out onto the SCSI bus. This mode will support both asynchronous and synchronous SCSI transfers. This mode is usually used during the Command and Data phases on the SCSI bus. To select this mode set SPIOEN=0 and DMAEN=1 (bits 3 & 6) in the SCSI Transfer Control 0 Register, 341h. The controls for Synchronous SCSI transfers are located in the SCSI RATE CONTROL Register, 344h.

4.3 HOST PROCESSOR DATA TRANSFERS

Data transfers between the host bus and the AIC-6260 can take place using either of the following two modes:

- **Host PIO:**
  Through Programmed I/O the host processor handles the data transfer into/out of the AIC-6260.

- **Host DMA:**
  Data transfers between the host and the AIC-6260 are run by a DMA controller in the host system.

Selection of host data transfer mode is controlled through the DMA CONTROL 0 Register, 352h.

4.3.1 Host PIO Mode

In host PIO mode, the host processor writes to or reads from the 128 byte host FIFO via the 16-bit data register at 356h. By taking advantage of the Repeat Instring instruction found in 286/386/486 processors, very high data transfer rates are possible.

4.3.2 Host DMA Mode

In host DMA mode, the host processor sets up the data transfer operation by loading a system DMA controller with a memory pointer and the transfer count. The host DMA controller then writes or reads data to or from the AIC-6260 host FIFO via the data register at 356h. Once begun, host DMA transfers run to completion without further host processor intervention.
In the AIC-6260, only 8-bit DMA transfers are available.

4.4 INTERRUPTS

The AIC-6260 can be configured to generate interrupts for all transfer critical conditions. Interrupts are controlled through a set of internal registers as shown in Table 4-1. Each interrupt condition has a readable status bit and controlling enable and clear bits.

TABLE 4-1. INTERRUPTS

Status Bit Name	Status Bit	Status Register Address	Enable Bit	Enable Register Address	Clear Bit	Clear Register Address
SELDO	Status 6	$34B_h$ r	Enable 6	350_h	Clear 6	$34B_h$ w
SELDI	Status 5	$34B_h$ r	Enable 5	350_h	Clear 5	$34B_h$ w
SELINGO	Status 4	$34B_h$ r	Enable 4	350_h	Clear 4	$34B_h$ w
SWRAP	Status 3	$34B_h$ r	Enable 3	350_h	Clear 3	$34B_h$ w
SDONE	Status 2	$34B_h$ r	Enable 2	350_h	Clear 2	$34B_h$ w
SPIORDY	Status 1	$34B_h$ r	Enable 1	350_h	Clear 1	$34B_h$ w
DMADONE	Status 0	$34B_h$ r	Enable 0	350_h	Clear 0	$34B_h$ w
SELTO	Status 7	$34C_h$ r	Enable 7	351_h	Clear 7	$34C_h$ w
ATNTARG	Status 6	$34C_h$ r	Enable 6	351_h	Clear 6	$34C_h$ w
SCSIRSTI	Status 5	$34C_h$ r	Enable 5	351_h	Clear 5	$34C_h$ w
PHASEMIS	Status 4	$34C_h$ r	Enable 4	351_h	n/a	n/a
BUSFREE	Status 3	$34C_h$ r	Enable 3	351_h	Clear 3	$34C_h$ w
SCSIPERR	Status 2	$34C_h$ r	Enable 2	351_h	Clear 2	$34C_h$ w
PHASECHG	Status 1	$34C_h$ r	Enable 1	351_h	Clear 1	$34C_h$ w
REQINIT	Status 0	$34C_h$ r	Enable 0	351_h	Clear 0	$34C_h$ w
SWINT	Status 0	352_h	Enable 2	352_h w	Clear 0	352_h w

The status bit reflects the current state of the interrupt source independent of interrupts being enabled. It may be read by the host processor at any time to obtain a real time indication of the condition. Removing the condition that caused the status bit to be latched does not always clear the status bit. Refer to the descriptions of the status bits and their corresponding clear bit to determine the exact conditions under which they are cleared.

The enable bit gates the entry of the status bit into the interrupt processing chain and essentially serves as an interrupt mask. In order for a condition to cause an interrupt, its enable bit must be set, otherwise the interrupt associated with the condition is suppressed.

The clear bit resets the interrupt latch corresponding to the particular interrupt condition. The interrupt latch will be set if the corresponding enable bit was set allowing the status bit condition to propagate. By clearing the interrupt latch, the interrupt condition will be removed from generation of the interrupt signal output on the IRQ pin. In some cases, the clear bit will also clear the status bit, but not always. Refer to the descriptions of each status bit to determine the exact conditions under which they are cleared.

All of the interrupt sources shown in Table 4-1 are logically ORed to form the signal output on the IRQ pin. The OR of all these sources is available for monitoring on the INSTAT status bit in the DMA Status register at 354h. A master enable is also available to gate the signal going out on the IRQ pin. If the INTEN bit of the DMACNTRL0 register at 352h is reset, no interrupts will be output on the IRQ pin. INSTAT is valid even if the INTEN bit is reset.

4.5 EXTERNAL PORT DECODE

As described previously, the AIC-6260 self maps its internal registers to an I/O address space of 340h to 35Fh(140h to 15Fh if ALTERNATE* is low). Within this range, the chip enables for two addresses, 35Ah and 35Bh(15Ah & 15Bh if ALTERNATE* is low) are output on the PORTEN* pin instead of being used internally, in order to provide a convenient way to add general purpose I/O ports external to the AIC-6260. These external ports may be used for control outputs or configuration input, in conjunction with general AIC-6260 SCSI operation. By combining the active low PORTEN* output with the I/O bus IOW*, IOR* and SA0 as shown in Figure 4-2, select signals for up to two read and two write bus transceivers are easily generated.

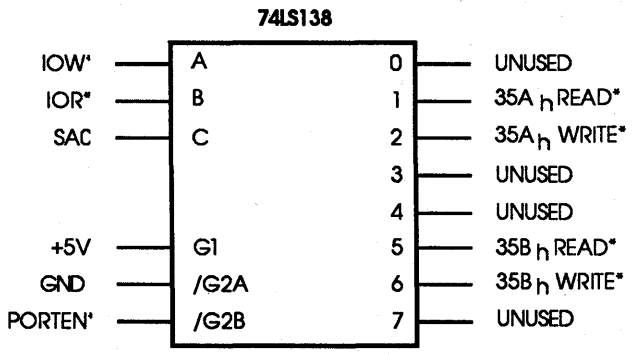


FIGURE 4-2. TYPICAL EXTERNAL LOGIC CIRCUIT

4.6 CLOCKING

The AIC-6260 requires a clocking source of up to 20 MHz in order to operate. It may be supplied externally or the internal crystal oscillator circuit in the AIC-6260 may be used. The advantage of using an external source is that power savings of up to one-third of total AIC-6260 power consumption may be realized by shutting down the internal oscillator circuits.

To use the internal oscillator, the CLKSEL pin must be tied to +5 VDC in order to supply a power source to the internal oscillator circuits. In addition, a crystal of up to 20 MHz must be connected to the X1, X2 pins. The generated clock signal will also be output on the F1 pin for use elsewhere if desired.

To input an external clocking signal, the internal oscillator circuits must be powered down by disconnecting the CLKSEL pin. Internally, CLKSEL will be grounded by a pulldown resister, or more preferably should be externally grounded. By powering down the oscillator circuits, the direction of the F1 buffer is changed, allowing the input of the external clocking source. The external clocking source should ideally have a 50% duty cycle with a minimum of 40/60 acceptable. Voltage input requirements are TTL levels.

The AIC-6260 may operate with a clock frequency of less than 20 MHz although all timing parameters must be derated for the slower operation.

4.7 Power Management

A unique feature of the AIC-6260 is the ability to allow the user to manage chip power consumption. Power consumption in the AIC-6260 can be functionally organized as three major components as shown in Figure 4-3. Power component A is used to operate the onboard crystal oscillator circuit and nominally draws about 9 mA. It can be avoided entirely by using an external clock source input on the F1 pin. Power component B(nominally 15 mA) is drawn by the bulk of the AIC-6260 circuits and may be turned off during periods of inactivity by activating the Powerdown-Sleep mode of operation. Power component C is made up of current used to maintain the Host Processor interface in order to allow constant access to the AIC-6260 control registers by the Host Processor. It's nominally about 6 mA and is the minimum amount the chip can draw while still maintaining Host Processor control and access.

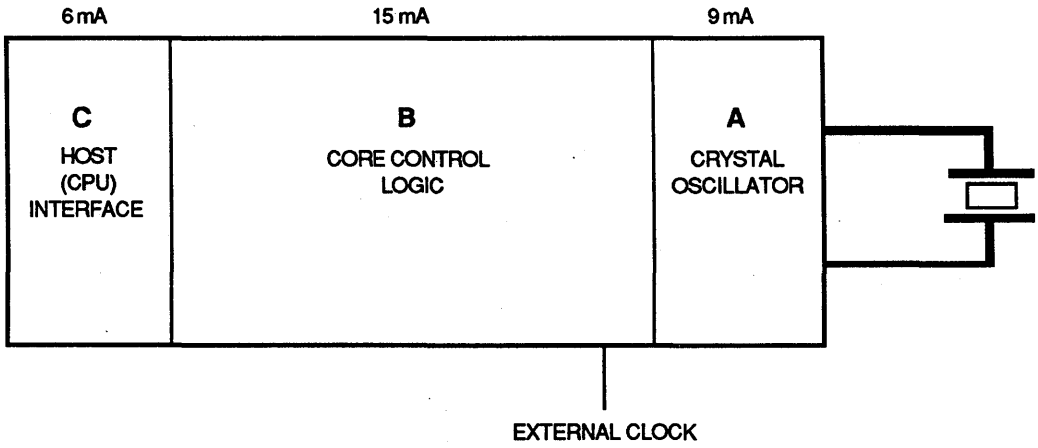


FIGURE 4-3. AIC-6260 POWER COMPONENTS

4.7.1 Powerdown-Sleep Mode

During periods of inactivity, the AIC-6260 may be shut down by the Host Processor to achieve power savings. Powerdown-Sleep Mode works by shutting off the clock to the bulk of the AIC-6260 circuits as depicted in Figure 4-4. Removing the clock reduces power to a static level, saving power component B. Powerdown is entered by setting bit 7 of the DMACNTRL1 register (353h) and exited by either resetting the bit or performing a chip master reset. Note that during power-down, the AIC-6260's Host Processor interface circuits are still active, allowing manipulation of the AIC-6260 register set by the Host Processor. If no AIC-6260 operations at all are expected, the chip may be shut down entirely by turning off all clock sources to the chip. As long as the power supply voltage is maintained, the AIC-6260 will statically maintain all register values. Note that during powerdown, no SCSI operations can be performed or responded to. For this reason, any pending operations must first be cleared before going into powerdown. To minimize power consumption, the AIC-6260 software device driver and BIOS available from Adaptec implement Powerdown as described.

4.8 TESTING

To assist in test development, the AIC-6260 features two test control registers — SCSI TEST CONTROL, 34Eh and TEST REGISTER, 35Eh. Through these registers, the internal counters can be more easily tested and access afforded to internal logic points.

This section provides basic information on using the AIC-6260. It includes a set of task descriptions for running data transfers and a simple applications drawing.

5.1 SELECTION/RESELECTION SEQUENCES

The AIC-6260 can perform Selection/Reselection In or Out sequences automatically. The following sections describe the tasks you must perform to run automatic Selection/Reselection In or Out sequences.

5.1.1 Selection Out Sequence

1) Load the SCSIID (345_h) and SCSIRATE (344_h) registers.

2) Set the expected phase in the SCSISIGO (bits 7–5, 343_h) register. All other controls must be cleared.

3) Load the SXFRCTL1 register (342_h) with the desired values.

4) Set CLRCH1 in the SXFRCTL0 register (bit 1, 341_h); this clears the transfer counter and channel one.

   NOTE: If the transfer mode is SCSI PIO, it is not necessary to clear channel one. However, you should do it anyway, as the target might respond with an unexpected phase, such as Data In Synchronous when you are expecting Message Out.

5) Reset TEMODEO and set ENSELO in the SCSISEQ register (bits 7 and 6, 340_h); this enables the Selection Out sequence.

   NOTE: If you are using either the auto-attention out or the auto-attention parity options, you should set ENAUTOATNO and/or ENAUTOATNP (bits 3 and 1, 340_h). If you are using the auto-attention out option, the expected phase set in the SCSISIGO register (bits 7–5, 343_h) in Step 2 should be Message Out; the target determines whether this phase is supported.

6) Set ENSELDO, ENSELDI, or ENSELINGO in the SIMODE0 register (bit 6, 5, or 4, 350_h).

7) Wait for SELINGO or SELDO to be set in the SSTAT0 register (bits 4 or 6, $34B_h$), or for SELTO to be set in the SSTAT1 register (bit 7, $34C_h$).

NOTE: If the hardware selection timer is disabled and SELINGO is set, start a timer and wait for the timer to expire, or for SELDO to be set in the SSTAT0 register (bit 6). TARGET (bit 7, 34B$_h$) should be cleared.

8) When SELDO is set in the SSTAT0 register (bit 6, 34B$_h$), the target has been selected and you may initiate an information transfer phase.

9) In order to detect a passing Bus Free condition during selection, follow this sequence:
   a) Clear the BUSFREE interrupt at the CLRSINT1 register (bit 3, 34C$_h$).
   b) Clear ENSELO in the SCSISEQ register (bit 6, 340$_h$).
   c) Clear ENSELTIMEO in the SIMODE0 register (bit 7, 351$_h$).
   d) Mask the SELDO interrupt by clearing ENSELDO in the SIMODE0 register (bit 6, 350$_h$).
   e) Look at SELDO status. If still active, a Bus Free condition has not occurred since selection.

5.1.2 Selection In Sequence

1) Load the OID field in the SCSIID register (bits 6–4, 345$_h$).

2) Set ENSELI in the SCSISEQ register (bit 5, 340$_h$); this enables the Selection In sequence.

   NOTE: You may also set ENATNTARG in the SIMODE1 register (bit 6, 351$_h$) to generate an interrupt if the initiator asserts ATN.

3) Wait for SELDI and TARGET to be set in the SSTAT0 register (bits 5 and 7, 34B$_h$).

   NOTE: If TARGET is set, you have been reselected by a target.

4) Check the SELID register (345$_h$) for the SCSI ID of the initiator.

5) Load the SCSIRATE register (344$_h$) as appropriate.

6) When SELDI and TARGET are set in the SSTAT0 register (bits 5 and 7, 34B$_h$), you have been selected by an initiator and may continue with an information transfer phase.

5.1.3 Reselection In Sequence

1) Load the SCSI IDs in the SCSIID register (345$_h$).

2) Set ENRESELI in the SCSISEQ register (bit 4, 340$_h$); this enables the Reselection In sequence.

NOTE: You may also set ENAUTOATNI in the SCSISEQ register (bit 2, 340h) to automatically assert ATN on reselection.

3) Wait for SELDI to be set and TARGET to be cleared in the SSTAT0 register (bits 5 and 7, 34Bh).

NOTE: If TARGET is set, you have been selected by an initiator.

4) Load the expected SCSI phase in the SCSISIGO register (bits 7–5, 343h).

5) Load the SCSIRATE register (344h) as appropriate.

6) When SELDI is set and TARGET is cleared in the SSTAT0 register (bits 5 and 7, 34Bh), you have been reselected and may continue with an information transfer phase.

5.1.4 Reselection Out Sequence

1) Load the SCSIID (345h) and SCSIRATE (344h) registers.

2) Set the SCSI phase to enter after reselection in the SCSISIGO (bits 7–5, 343h) register. All other controls must be cleared.

3) Set TEMODEO and ENSELO in the SCSISEQ register (bits 7 and 6, 340h); this enables the Reselection Out sequence. The auto-attention options must both be cleared.

4) Wait for SELINGO or SELDO to be set in the SSTAT0 register (bits 4 or 6, 34Bh), or for SELTO to be set in the SSTAT1 register (bit 7, 34Ch).

NOTE: TARGET (bit 7, 34Bh) should be set. If it is not, you have initiated a Selection sequence.

5) Load the SXFRCTL1 register (342h) with the desired values.

6) Load the STCNT register (348h–34Ah) with the transfer count.

7) Set CLRCH1 in the SXFRCTL0 register (bit 1, 341h); this clears the transfer counter and channel one. Then set SXFRCTL0 for the proper channel and SCSI Transfer enabled.

NOTE: If the transfer mode is SCSI PIO, it is not necessary to clear channel one. However, you should do it anyway, as the target might respond with an unexpected phase, such as Data In Synchronous, when you are expecting Message Out.

8) When SELDO and TARGET are set in the SSTAT0 register (bits 6 and 7, 34Bh), you have reselected an initiator; you may initiate an information transfer phase.

5.2 SCSI PIO DATA TRANSFERS

Use the SCSI PIO data transfer modes whenever you require host processor intervention during the transfer, such as during message exchanges. SCSI PIO is asynchronous only. There are two types of SCSI PIO, manual and automatic.

- **Manual** The host processor writes directly to the SCSI data bus via the latch at 346_h and reads or drives the SCSI bus control lines via the register at 343_h. In manual mode, the AIC-6260 is essentially a bus buffer having no control functions. Manual mode supports asynchronous SCSI transfers only.

- **Automatic** The host processor writes directly to the SCSI data bus via the latch at 346_h, while the AIC-6260 performs SCSI bus control automatically. Automatic SCSI PIO transfers can be monitored by interrupt or polling status. Interrupt configuration for the AIC-6260 is controlled by the interrupt mode registers at 350_h and 351_h. Polling mode is driven off the SPIORDY status bit in the SSTAT0 register (bit 1, $34B_h$). SCSI PIO mode supports asynchronous SCSI transfers only.

The following sections describe the tasks you must perform to accomplish automatic SCSI PIO transfers as an initiator or target.

5.2.1 Initiator Data Transfer: Host to SCSI

1) Set SPIOEN in the SXFRCTL0 register (bit 3, 341_h).

2) Wait for SPIORDY to be set in the SSTAT0 register (bit 1, $34B_h$).

3) Write data to the SCSIDAT register (bits 7–0, 346_h).

4) If you have more data to transfer, repeat Steps 2–4. If not, proceed to Step 5.

5) Clear SPIOEN in the SXFRCTL0 register (bit 3, 341_h).

5.2.2 Initiator Data Transfer: SCSI to Host

1) Set SPIOEN in the SXFRCTL0 register (bit 3, 341_h).

2) Wait for SPIORDY to be set in the SSTAT0 register (bit 1, $34B_h$).

3) Read data from the SCSIDAT register (bits 7–0, 346_h).

4) Test PHASEMIS in the SSTAT1 register (bit 4, $34C_h$). If PHASEMIS is cleared, there is more data to transfer; repeat Steps 2–4. If PHASEMIS is set, there is no more data to transfer; proceed to Step 5.

5) Clear SPIOEN in the SXFRCTL0 register (bit 3, 341_h).

5.2.3 Target Data Transfer: Host to SCSI

1) Set the SCSI phase in the SCSISIGO register (bits 7–5, 343_h).

2) Set SPIOEN in the SXFRCTL0 register (bit 3, 341_h).

3) Wait for SPIORDY to be set in the SSTAT0 register (bit 1, $34B_h$).

4) Write data to the SCSIDAT register (bits 7–0, 346_h); this action asserts REQ.

5) If you have more data to transfer, repeat Steps 3–5. If not, proceed to Step 6.

6) Clear SPIOEN in the SXFRCTL0 register (bit 3, 341_h).

5.2.4 Target Data Transfer: SCSI to Host

1) Set the SCSI phase in the SCSISIGO register (bits 7–5, 343_h).

2) Set SPIOEN in the SXFRCTL0 register (bit 3, 341_h); this action asserts REQ.

3) Wait for SPIORDY to be set in the SSTAT0 register (bit 1, $34B_h$).

4) Read data from the SCSIDAT register (bits 7–0, 346_h); REQ is de-asserted when the initiator de-asserts ACK, and another REQ is automatically asserted.

5) If the current byte is not the last byte to be transferred, repeat Steps 3–4. If the current byte is the last byte to be transferred, go to Step 6.

6) Clear SPIOEN in the SXFRCTL0 register (bit 3, 341_h) *before* reading data from the SCSIDAT register (bits 7–0, 346_h).

5.3 NORMAL MODE DATA TRANSFERS

Use the normal data transfer modes for normal SCSI data transfers (commands and data). Normal mode uses two types of Host transfer modes:

- **Host PIO** The host processor writes to or reads from the 128-byte host FIFO via the data register at 356_h. Host PIO transfers are driven off the status bits in the status register at 352_h.

- **Host DMA** The host processor sets up the data transfer operation by loading its DMA controller with a memory pointer and the transfer count. The host DMA controller writes/reads transfer data to/from the 128-byte Host FIFO via the data register at 356_h. Once begun, host DMA transfers run to completion without further host processor intervention.

The following sections describe the tasks you must perform to accomplish normal mode SCSI transfers as an initiator or target.

5.3.1 Initiator Data Transfer: Host to SCSI in Host PIO Mode

1) Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343_h).

2) Clear the transfer count and the SCSI and host FIFOs.

3) Set up the host processor registers for transfer count and address.

4) Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, $34C_h$).

5) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

6) Set ENDMA and WRITE/–READ, and clear DMA/–PIO in the DMACNTRL0 register (bits 7, 3, and 5, 352_h).

7) Wait for DFIFOEMP or INTSTAT to be set in the DMASTAT register (bits 3 and 5, 354_h).

8) If DFIFOEMP is set and INTSTAT is cleared in the DMASTAT register (bits 3 and 5, 354_h), use REP OUTSW to write 128 bytes (64 words).

9) Adjust host processor transfer count.

10) Test for the end of the transfer in the host processor; repeat Steps 7–10 until all data has been written.

11) When all data has been written, clear ENDMA in the DMACNTRL0 register (bit 7, 352_h).

5.3.2 Initiator Data Transfer: SCSI to Host in Host PIO Mode

1) Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343_h).

2) Clear the transfer count and the SCSI and host FIFOs.

3) Set up the host processor registers for transfer count and address.

4) Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, $34C_h$).

5) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

6) Set ENDMA, and clear WRITE/–READ and DMA/–PIO in the DMACNTRL0 register (bits 7, 3, and 5, 352_h).

7) Wait for DFIFOFULL or INTSTAT to be set in the DMASTAT register (bits 4 and 5, 354_h).

8) If DFIFOFULL is set and INTSTAT is cleared in the DMASTAT register (bits 4 and 5, 354_h), use REP INS to read 128 bytes (64 words).

9) Adjust host processor transfer count.

10) Test for the end of the transfer in the host processor; repeat Steps 7–10 until all data has been read.

11) When all data has been read, clear ENDMA in the DMACNTRL0 register (bit 7, 352_h).

5.3.3 Initiator Data Transfer: Host to SCSI in Host DMA Mode

1) Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343_h).

2) Clear the transfer count and the SCSI and host FIFOs.

3) Set up the host DMA controller for address, byte count, and transfer mode.

4) Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, $34C_h$).

5) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

6) Set ENDMA, 8BIT/–16BIT, WRITE/–READ, and DMA/–PIO in the DMACNTRL0 register (bits 7, 6, 3, and 5, 352_h).

7) Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

5.3.4 Initiator Data Transfer: SCSI to Host in Host DMA Mode

1) Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343_h).

2) Clear the transfer count and the SCSI and host FIFOs.

3) Set up the host DMA controller for address, byte count, and transfer mode.

4) Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, $34C_h$).

5) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

6) Set ENDMA, 8BIT/–16BIT, and DMA/–PIO and clear WRITE/–READ in the DMACNTRL0 register (bits 7, 6, 5, and 3, 352_h).

7) Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

5.3.5 Target Data Transfer: Host to SCSI in Host PIO Mode

1) Set the SCSI phase in the SCSISIGO register (bits 7–5, 343_h).

2) Load the SCSI transfer count in the STCNT register (bits 7–0, 348_h–$34A_h$).

3) Load the SXFRCTL0 and SXFRCTL1 registers (341_h and 342_h) with the desired values.

4) Clear the SCSI and host FIFOs.

5) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

6) Set ENDMA and WRITE/–READ and clear DMA/–PIO in the DMACNTRL0 register (bits 7, 3, and 5, 352_h).

7) Wait for DFIFOEMP or INTSTAT to be set in the DMASTAT register (bits 3 and 5, 354_h).

8) If DFIFOEMP is set and INTSTAT is cleared in the DMASTAT register (bits 3 and 5, 354_h), use REP OUTSW to write 128 bytes (64 words).

9) Adjust host processor transfer count.

10) Test for the end of the transfer in the host processor; repeat Steps 7–10 until all data has been written.

11) When all data has been written, clear ENDMA in the DMACNTRL0 register (bit 7, 352_h).

12) When the command has completed, clear the SCSISIGO register (bits 7–0, 343_h); this forces Bus Free.

5.3.6 Target Data Transfer: SCSI to Host in Host PIO Mode

1) Set the SCSI phase in the SCSISIGO register (bits 7–5, 343_h).

2) Load the SCSI transfer count in the STCNT register (bits 7–0, 348_h–$34A_h$).

3) Load the SXFRCTL0 and SXFRCTL1 registers (341_h and 342_h) with the desired values.

4) Clear the SCSI and host FIFOs.

5) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

6) Set ENDMA, and clear DMA/–PIO and WRITE/–READ in the DMACNTRL0 register (bits 7, 5, and 3, 352_h).

7) Wait for DFIFOFULL or INTSTAT to be set in the DMASTAT register (bits 4 and 5, 354_h).

8) If DFIFOFULL is set and INTSTAT is cleared in the DMASTAT register (bits 4 and 5, 354_h), use REP INS to read 128 bytes (64 words).

9) Adjust host processor transfer count.

10) Test for the end of the transfer in the host processor; repeat Steps 7–10 until all data has been read.

11) When all data has been read, clear ENDMA in the DMACNTRL0 register (bits 7, 352_h).

12) When the command has completed, clear the SCSISIGO register (bits 7–0, 343_h); this forces Bus Free.

5.3.7 Target Data Transfer: Host to SCSI to Host in DMA Mode

1) Set the SCSI phase in the SCSISIGO register (bit 7–5, 343_h).

2) Load the SCSI transfer count in the STCNT register (bits 7–0, 348_h–$34A_h$).

3) Load the SXFRCTL0 and SXFRCTL1 registers (341_h and 342_h) with the desired values.

4) Clear the SCSI and host FIFOs.

5) Set up the host processor DMA controller for address, byte count, and transfer mode.

6) Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, $34C_h$).

7) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

8) Set ENDMA, 8BIT/–16BIT, WRITE/–READ, and DMA/–PIO in the DMACNTRL0 register (bits 7, 6, 3, and 5, 352_h).

9) Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

10) When the command has completed, clear the SCSISIGO register (bits 7–0, 343_h); this forces Bus Free.

5.3.8 Target Data Transfer: SCSI to Host in Host DMA Mode

1) Set the SCSI phase in the SCSISIGO register (bits 7–5, 343_h).

2) Load the SCSI transfer count in the STCNT register (bits 7–0, 348_h–$34A_h$).

3) Load the SXFRCTL0 and SXFRCTL1 registers (341_h and 342_h) with the desired values.

4) Clear the SCSI and host FIFOs.

5) Set up the host processor DMA controller for address, byte count, and transfer mode.

6) Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, $34C_h$).

7) Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341_h); this enables the AIC-6260 SCSI logic.

8) Set ENDMA, 8BIT/–16BIT, and DMA/–PIO and clear WRITE/–READ in the DMACNTRL0 register (bits 7, 6, 5, and 3, 352_h).

9) Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

10) When the command has completed, clear the SCSISIGO register (bits 7–0, 343_h); this forces Bus Free.

5.4 DIAGNOSTICS

The host FIFO can be tested using the wrap-around feature. Transfers are accomplished in the normal manner, using host DMA or host PIO mode.

To check the FIFO, ensure that DMAEN and SCSIEN in the SXFRCTL0 register (bits 6 and 7, 341_h) are cleared. Set WRITE/–READ in the DMACNTRL0 register (bit 3, 352_h) and begin the transfer. To read the data back, clear WRITE/–READ in the DMACNTRL0 register (bit 3, 352_h).

5.5 INITIATOR MESSAGE HANDLING

Messages are intended to be handled by SCSI PIO transfer. Certain special cases to consider are messages after selection, multiple messages, or parity errors. If messages after selection are to be handled by the initiator, ATN is asserted on the bus. The target responds with the Message Out phase at this time. The first message is the ID message, and after this, the initiator has the option of sending a multiple-byte message such as a synchronous data transfer request. ATN remains asserted during Message Out transfers, until cleared by setting CLRATNO in CLRSINT1 (bit 6, $34C_h$). In order to maintain SCSI protocol, ATN should be cleared before the last ACK of a message sequence, or in the case of automatic SCSI PIO, the last write to SCSIDAT. In the case of an error condition, ATN should be cleared after the first REQ of the Message Out phase and before the last ACK of the message sequence. If a parity error occurs on Message In, ATN is asserted before ACK, and the message should be retransmitted.

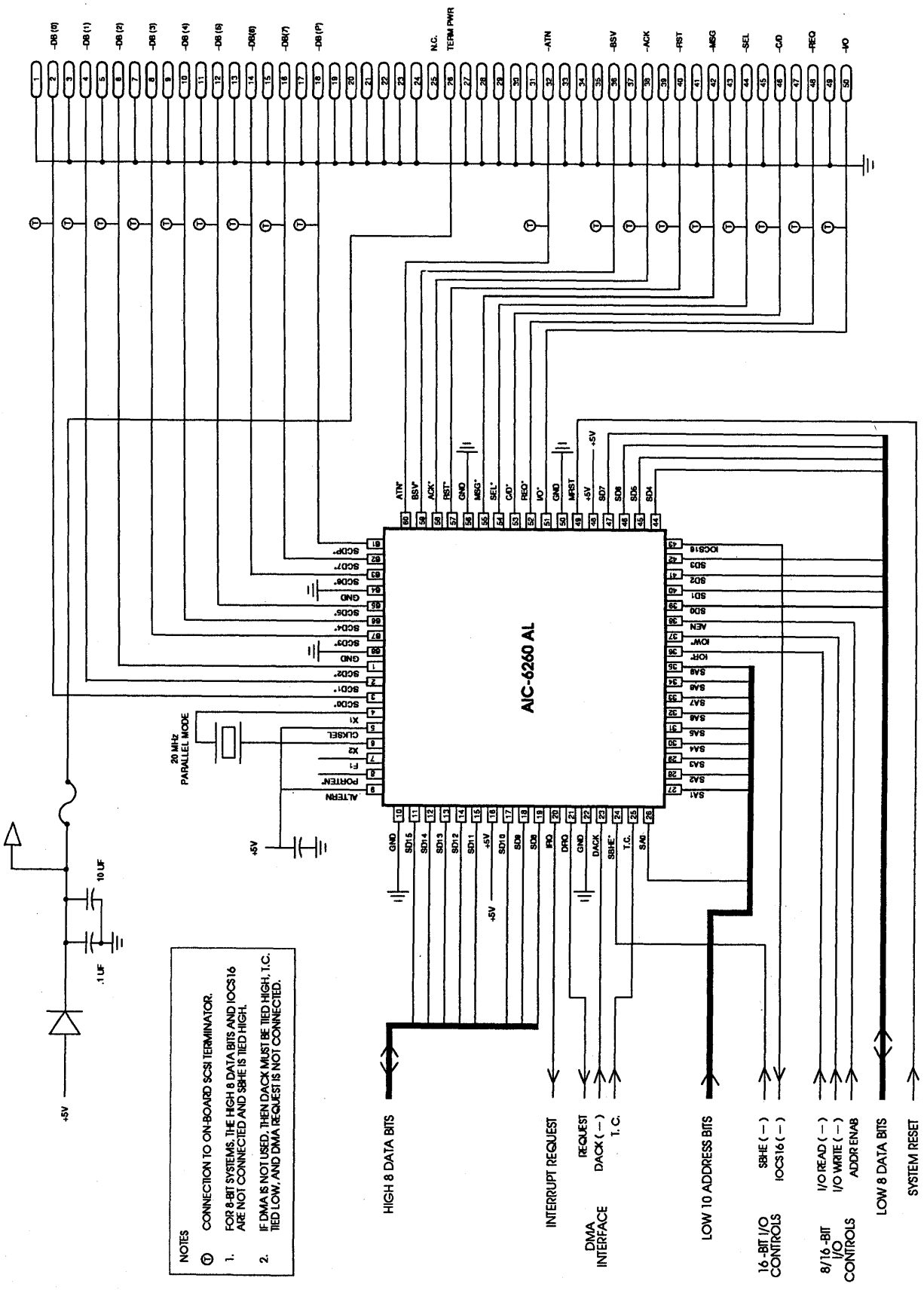


FIGURE 5-1. SAMPLE AIC-6260 APPLICATION DRAWING

NOTE: The following is advanced information and subject to change without notice.

6.1 ABSOLUTE MAXIMUM RATINGS (NONOPERATING)

Storage Temperature: -65° C to 150° C
Power Supply Voltage: 0 to 7 Volts
Voltage on any pin: -0.5 to Vcc+0.5 Volts

6.2 OPERATING CONDITIONS

Ambient Temperature Under Bias: 0° C to 70° C
Supply Voltage (Vcc): 4.75 to 5.25 Volts

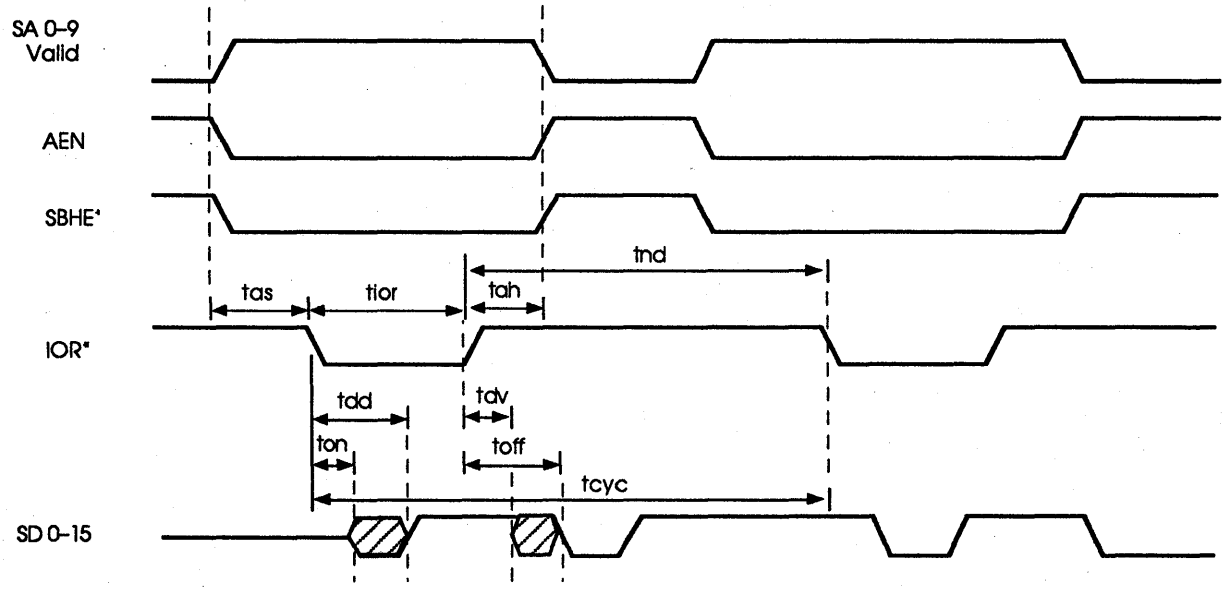
6.3 DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{il}	Input Low Voltage, All Pins				0.8	V
V_{ih}	Input High Voltage, All Pins		2.0			V
V_h	Input Hysteresis, SCSI Signals Only		200			mV
V_{ol1}	Output Low Voltage, PORTEN*	I_{ol} = 2 mA			0.5	V
V_{ol2}	Output Low Voltage, SD0-15, DRQ, IRQ, IOCS16*	I_{ol} = 24 mA			0.5	V
V_{ol3}	Output Low Voltage, All SCSI Signals	I_{o1} = 48 mA			0.5	V
V_{oh1}	Output High Voltage, PORTEN*	I_{ol} = –2 mA	2.4			V
V_{oh2}	Output High Voltage, SD0-15 DRQ, IRQ	I_{o1} = –8 mA	2.4			V
I_{o2}	Output Leakage for Tristate and Open Collector drivers	$V_{dd} \geq Vin \geq GND$		±40		µA
I_{dd1}	Operating Current Consumption	20 MHz External Clock		19.8	25	mA
		20 MHz Internal Crystal Oscillator		29.0	35	mA
I_{dd2}	Powerdown Current Consumption	20 MHz External Clock		5.8	10	mA
		20 MHz Internal Crystal Oscillator		14.2	20	mA
I_{dd3}	Static Current Consumption	$V_{IN} = V_{DD}$, Pin F1 = V_{DD}		1.5	5	mA
C_{IN}	Input Capacitance	F_c = 1 MHz			10	pF
C_{OUT}	Output Capacitance				15	pF

6.4 SYSTEM TIMING

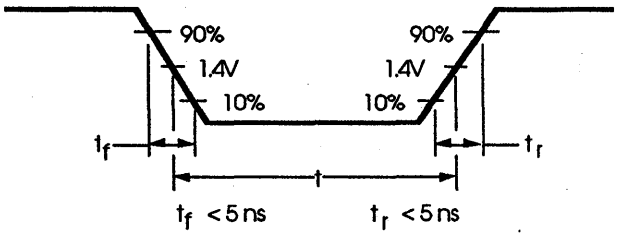
This section contains AC Timing information on the AIC-6260. All timing presumes operation with a 20 MHz clock.

6.4.1 Host Processor PIO Data Read Operation

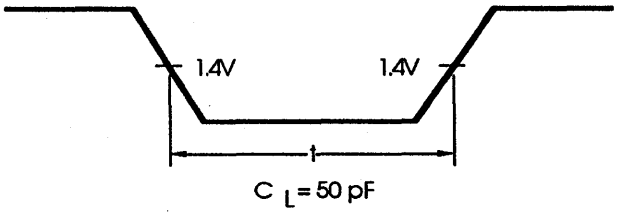


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip Clock period	50			ns
tas	Address setup time to IOR* low	25			ns
tah	Address hold time from IOR* high	25			ns
tdd	Data valid delay from IOR* low, Note 2	6		60	ns
tdv	Data valid hold time from IOR* high, Note 3	4			ns
tnd	Time between consecutive IOR*	2 ttc			
toff	Driver off time from IOR* high, Note 4			25	ns
ton	Driver on time from IOR* low, Note 1	6		25	ns
tcyc	Cycle time	4 ttc + 20 ns			
tior	IOR* pulse width	100			ns

A.C. INPUT CONDITIONS



A.C. OUTPUT TIMING CONDITIONS

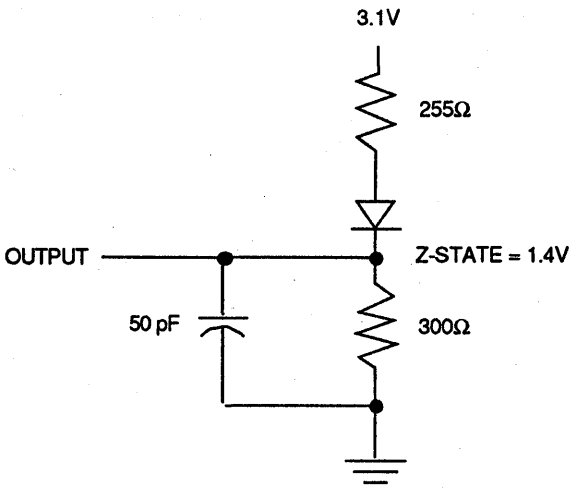


Note 1: ton is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tri-state bias voltage level of 1.4V.

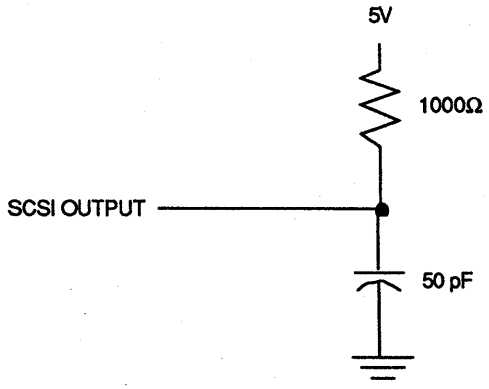
Note 2: tdd is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.

Note 3: tdv is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.

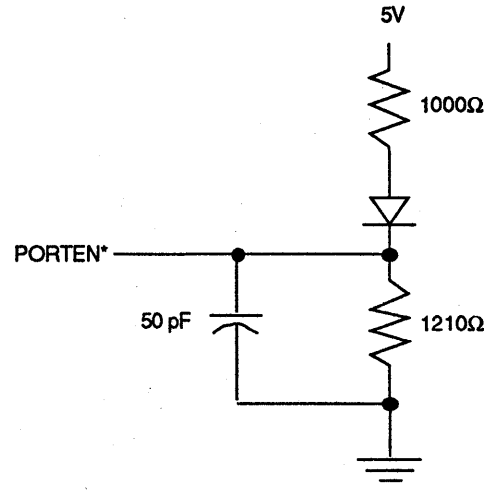
Note 4: toff is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.



AC Test Load for all Outputs Except SCSI and PORTEN*

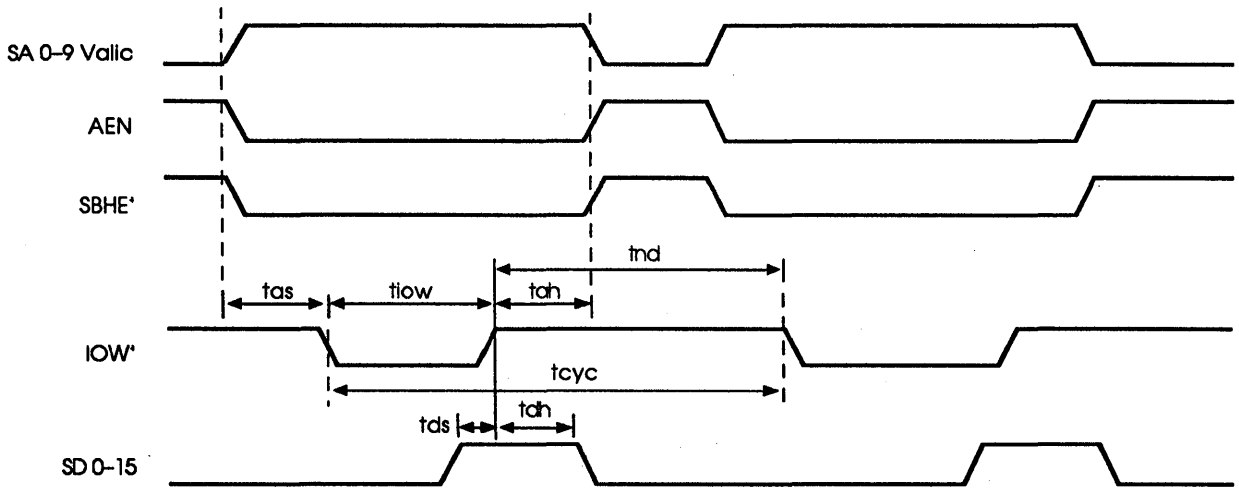


AC Test Load for SCSI Outputs



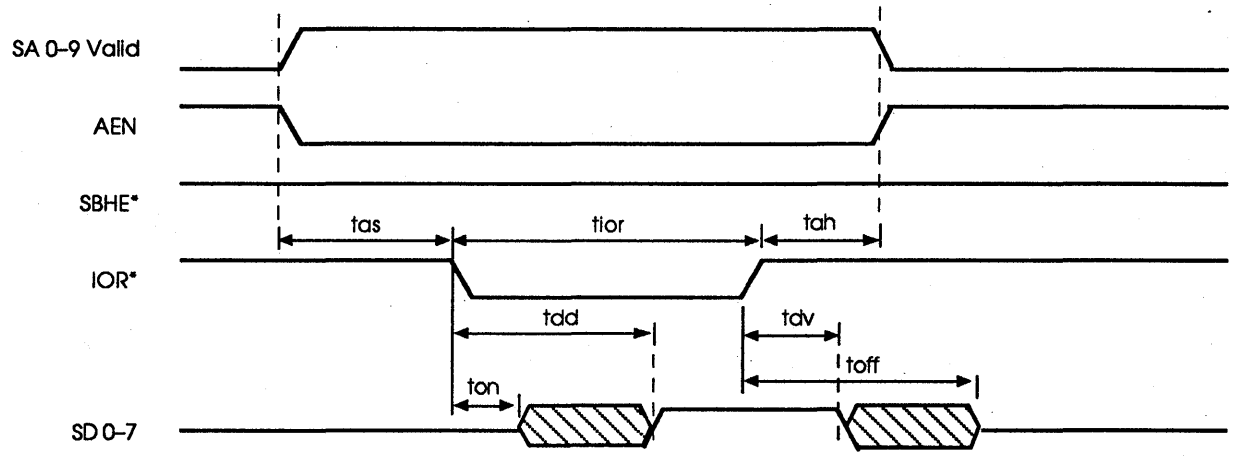
AC Test Load for PORTEN* Output

6.4.2 Host Processor PIO Data Write Operation



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip clock period	50			ns
tas	Address setup time to IOW* low	25			ns
tah	Address hold time from IOW* high	25			ns
tds	Data setup time to IOW* high	5			ns
tdh	Data hold time from IOW* high	15			ns
tnd	Time between consecutive IOW*	2ttc			
tcyc	Cycle time	4ttc + 20 ns			
tiow	IOW* pulse width	100			ns

6.4.3 Host Processor I/O Read Operation



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip clock period	50			ns
tas	Address setup time to IOR* low	25			ns
tah	Address hold time from IOR* high	25			ns
tdd	Data valid delay from IOR* low, Note 2	6		60	ns
tdv	Data valid delay hold time from IOR* high, Note 3	4			ns
toff	Driver off time from IOR* high, Note 4			25	ns
ton	Driver on time from IOR* low, Note 1	6		25	ns
tior	IOR* pulse width	100			ns

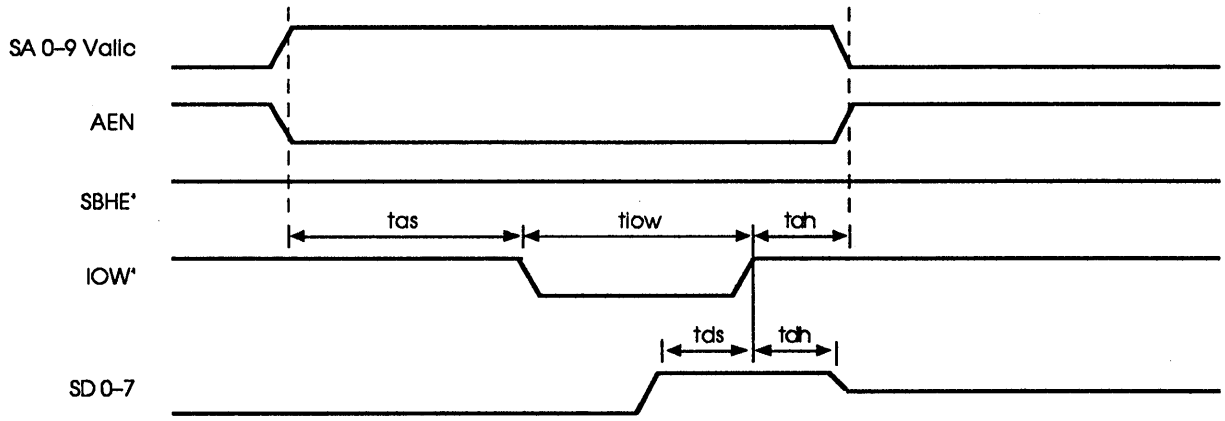
Note 1: ton is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tri-state bias voltage level of 1.4V.

Note 2: tdd is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.

Note 3: tdv is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.

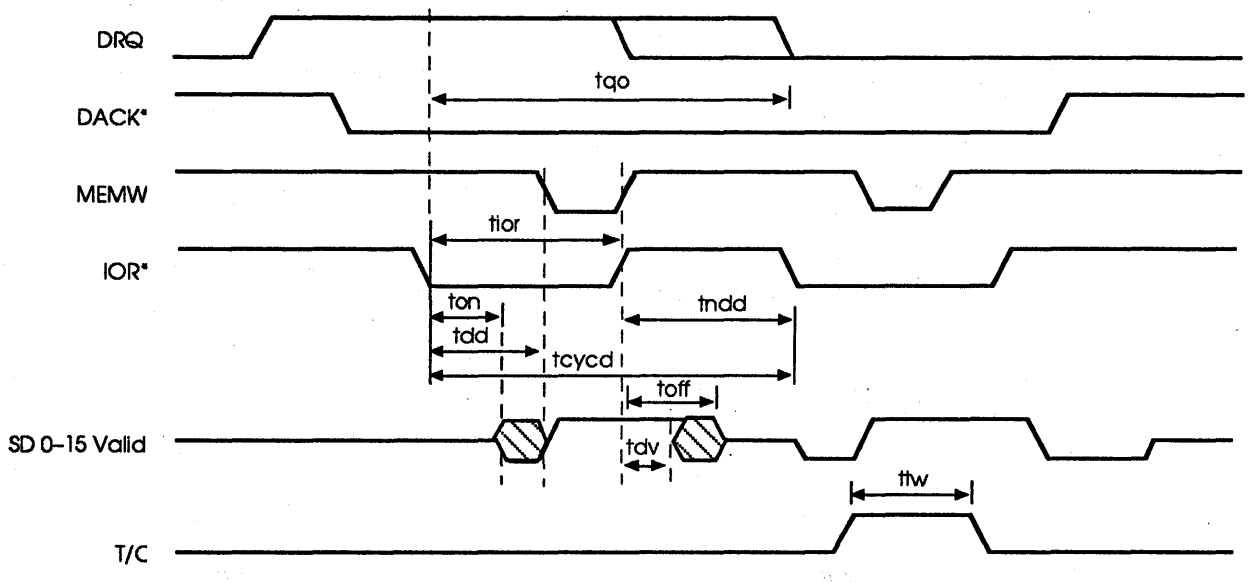
Note 4: toff is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.

6.4.4 Host Processor I/O Write Operation



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip Clock period	50			ns
tas	Address setup time to IOW* low	25			ns
tah	Address hold time from IOW* high	25			ns
tds	Data setup time to IOW* high	5			ns
tdh	Data hold time IOW* high	15			ns
tiow	IOW* pulse width	100			ns

6.4.5 Host Processor DMA Read Operation



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip clock period	50			ns
ton	Driver on time from IOR* low, Note 1	6		25	ns
toff	Driver off time from IOR* high, Note 4			25	ns
tndd	Time between consecutive DMA IOR*	4ttc			
tqo	DRQ off time from IOR*			1ttc + 25 ns	ns
tcycd	DMA read cycle time	8ttc			
ttw	Terminal count pulse width	50			ns
tdd	Data valid delay from IOR* low, Note 2	6		60	ns
tdv	Data valid hold time from IOR* high, Note 3	4			ns
tior	IOR* pulse width	100			ns

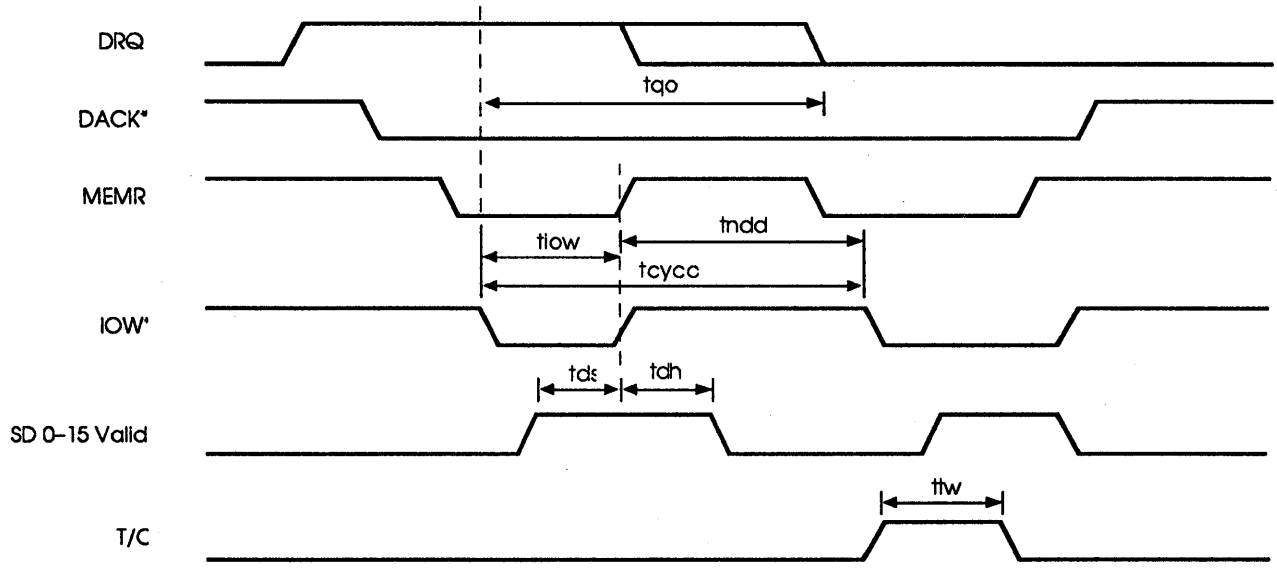
Note 1: ton is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tri-state bias voltage level of 1.4V.

Note 2: tdd is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.

Note 3: tdv is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.

Note 4: toff is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.

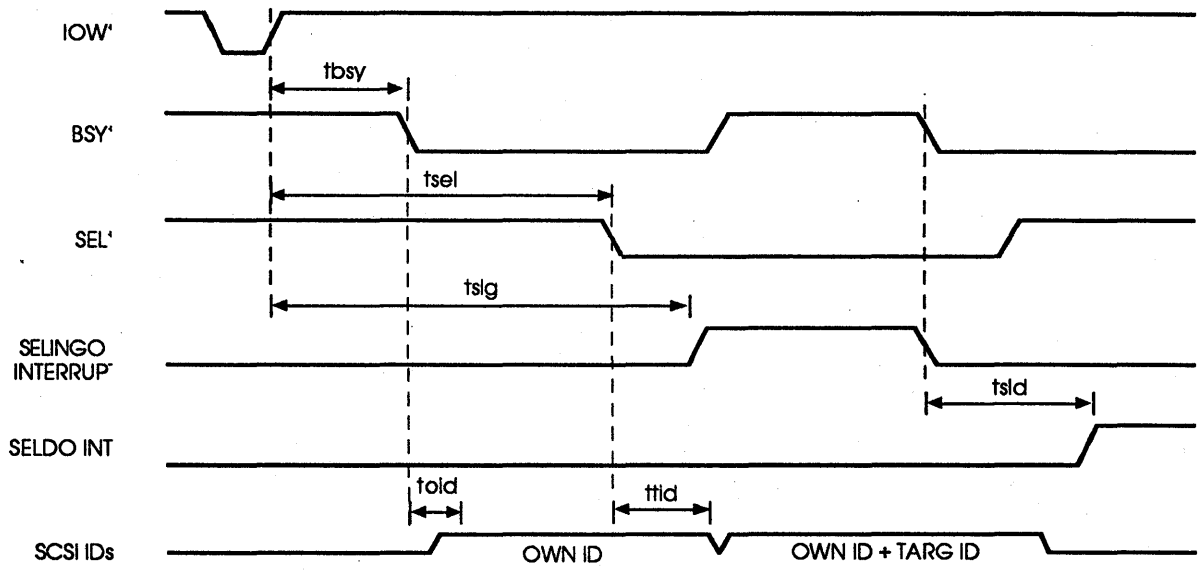
6.4.6 Host Processor DMA Write Operation



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip clock period	50			ns
tds	Data setup time to IOW* high	5			ns
tdh	Data hold time from IOW* high	15			ns
tndd	Time between consecutive DMA IOW*	4ttc			
tqo	DRQ off time from IOW* high			1ttc + 25 ns	ns
tcycd	DMA write cycle time	8ttc			
ttw	Terminal count pulse width	50			ns
tiow	IOW* pulse width	100			ns

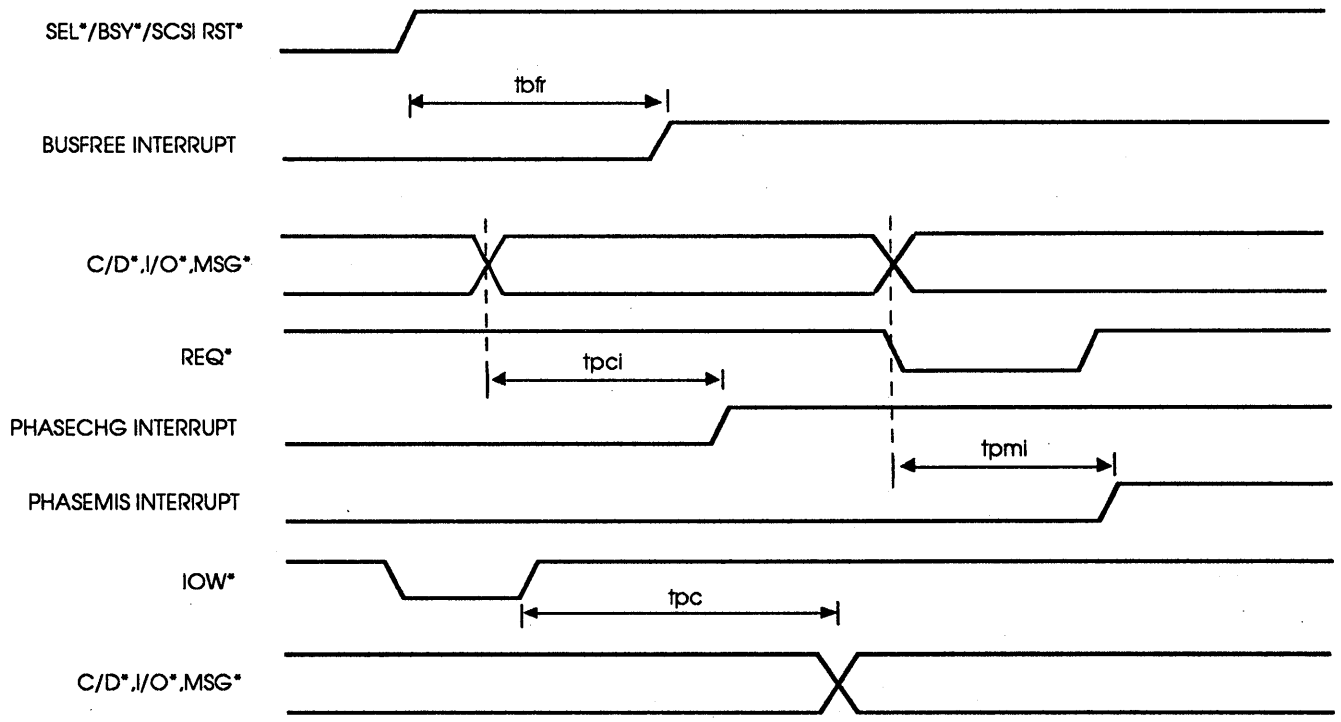
6.5 SCSI BUS TIMING

6.5.1 Arbitration/Selection



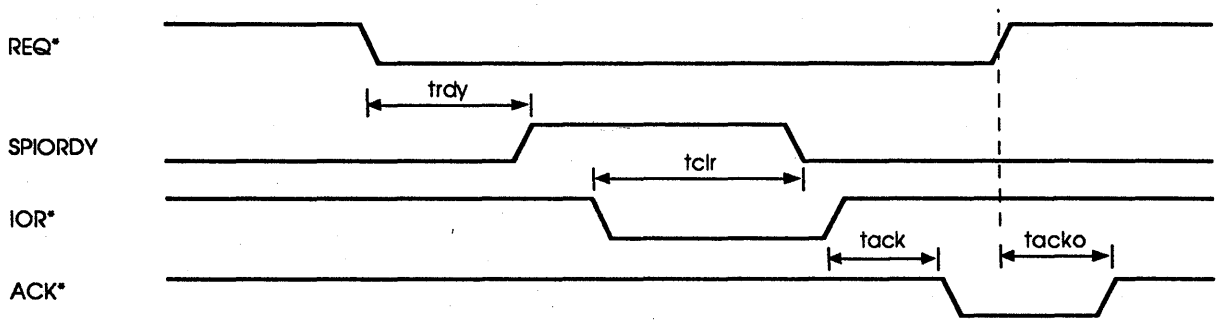
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip clock period	50			ns
tbsy	ENSELO bit set to BSY* true			16ttc + 60	ns
tsel	ENSELO bit set to SEL* true			64ttc + 60	ns
tslg	ENSELO bit set to SELINGO interrupt			92ttc + 60	ns
tsld	Target BSY* to SELDO interrupt			4ttc + 60	ns
toid	BSY* assertion to own ID			20	ns
ttid	SEL* assertion to target ID	24ttc			

6.5.2 SCSI Bus Free Detection



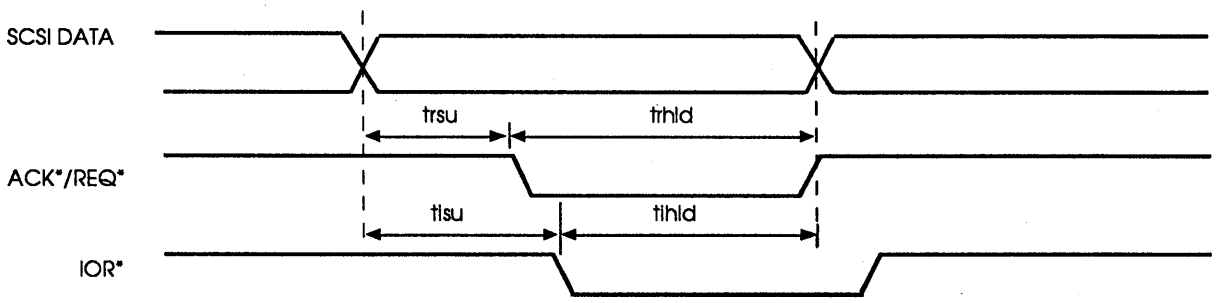
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip clock period	50			ns
tbfr	SEL*,BSY*,SCSI RST* to BUS FREE interrupt			9ttc + 40	ns
tpci	Phase change to interrupt			37	ns
tpmi	Phase change and REQ* to interrupt			40	ns
tpc	IOW* to phase change (target mode)			46	ns

6.5.3 SCSI PIO



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
ttc	Chip clock period	50			ns
trdy	REQ* true to SPIORDY interrupt			3ttc + 35	ns
tclr	IOR* true to SPIORDY cleared			60	ns
tack	IOR* false to ACK asserted			3ttc + 35	ns
tacko	REQ* false to ACK false			2ttc + 62	ns

6.5.4 SCSI Data Setup and Hold. Latched Data and PIO

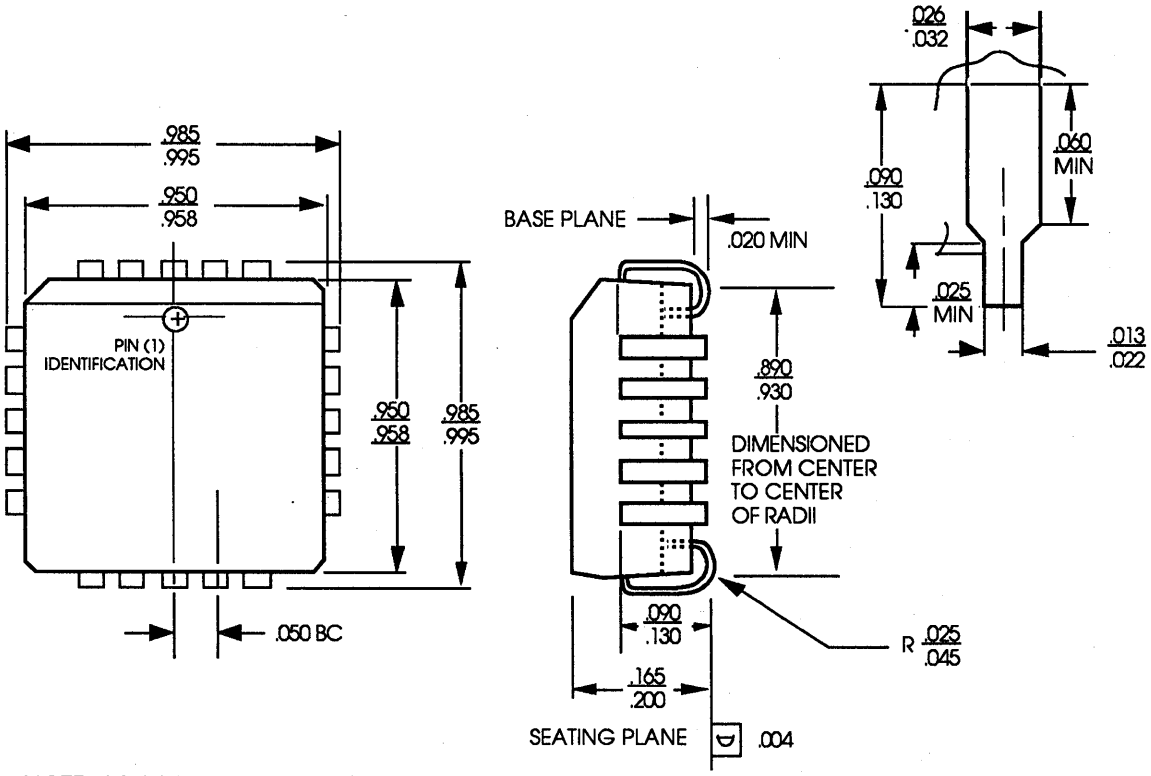


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
trsu	SCSI data setup to REQ* or ACK*[1]	5			ns
trhld	SCSI data hold from REQ* or ACK[1]	15			ns
tisu	SCSI data setup to IOR[2] low	15			ns
tihold	SCSI data hold from IOR*[2] low	5			ns

[1] Initiator mode uses leading edge of REQ to latch data, and Target mode uses leading of ACK. These times apply to synchronous, asynchronous, and auto PIO modes of operation.

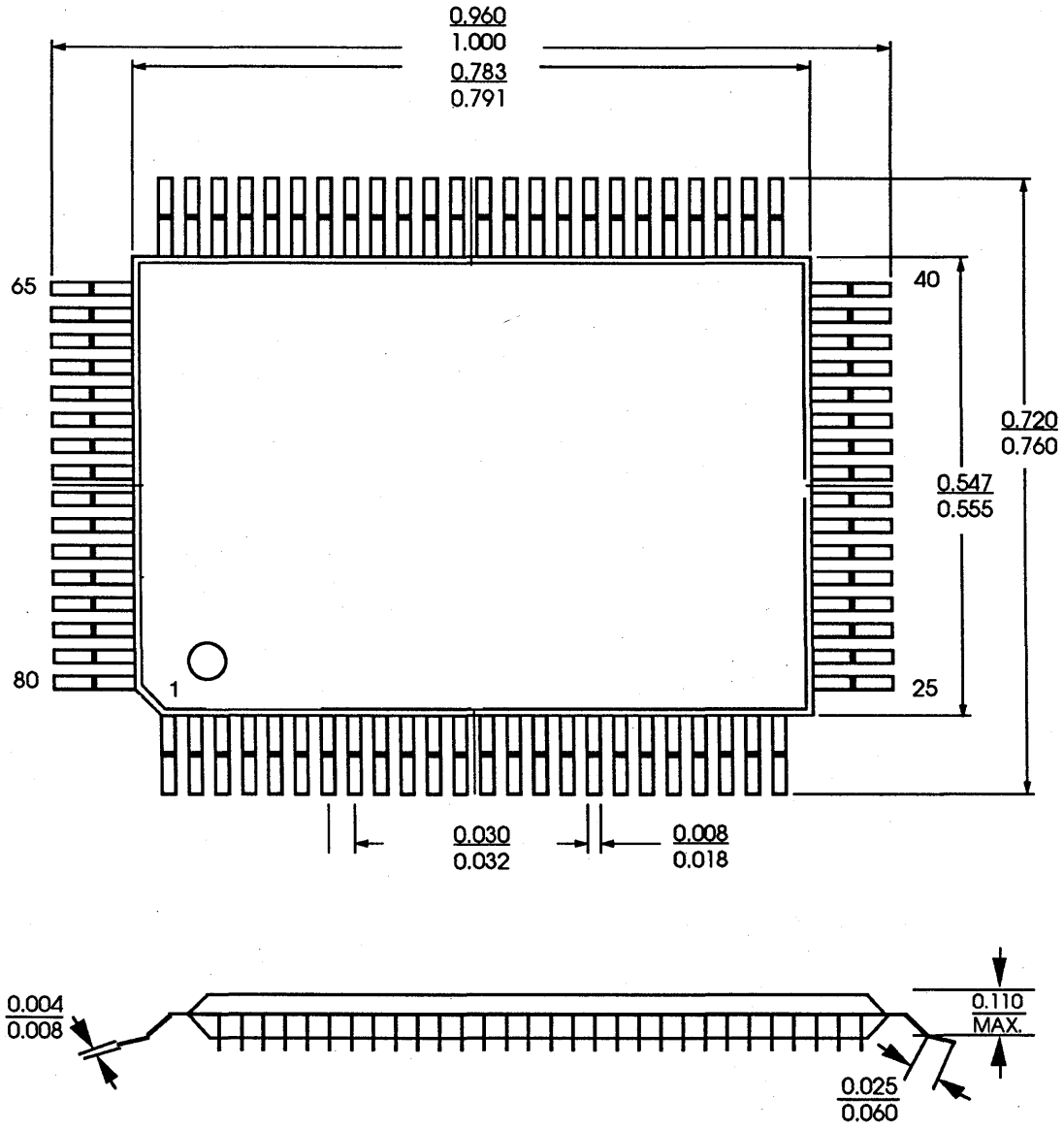
[2] These times apply to SCSI PIO when reading port 347h.

7.1 68-PIN PLCC



NOTE: Mold flash shall not exceed 0.010

7.2 80-PIN QUAD FLAT PACK



NOTE: Units are in inches

Appendix A Data Transfer Rate Calculations

This appendix describes methods for calculating the data transfer rate of the AIC-6260. It also includes examples of the different data rates for various speeds of computers, system memories and host buses.

Each example includes the following information:

286/386 The type of CPU has a direct impact on transfer rate calculations, as each processor runs at a different clock rate and requires a different number of cycles to run the same instruction.

Clock Rate This is the advertised speed at which the CPU runs.

Wait States This is the number of wait states inserted by the CPU. This number varies according to computer design and memory speed.

Host Bus Time This is the time inserted during the READ or WRITE strobe during host bus I/O cycles.

Bytes This is the size of the FIFO.

Loop Time This is the time required to execute a software loop during data transfer.

Data Rate This is the average data rate.

A.1 BURST RATE

To calculate the burst rate for any computer, use the repeat instruction time calculation and divide that into the number of bytes (128).

A.2 PIO TRANSFER RATE CALCULATION

This is a brief description of how to calculate the data transfer rate using the PIO method of transfer. The basic method is to loop looking for a full or empty FIFO (depending on direction) and to transfer data with the 286/386 repeat string I/O instructions.

The data transfer may be calculated according to the following equation when the driver is used. When the BOIS is used, there is excessive program loop time due to additional wait states added during op code fetches.

data rate = #bytes/time

# bytes = 128 by design
time = program loop execution time
+ (repeat instruction time)(#cycles)
+ (host bus time per I/O cycle)(#cycles)

#cycles = 64 (2 bytes per cycle)
program loop time (286) = (42 + (20 * w)) * clk
program loop time (386) = (49 + (20 * w)) * clk
repeat instruction time (286) = (4 * (2 * w)) * clk
repeat instruction time (386) = (6 * (2 * w)) * clk
w = wait state
clk = CPU clock period

host bus time = host bus wait states, design dependent, must be 200ns minimum total cycle time.

A.3 PIO TRANSFER RATE EXAMPLES

The following are examples of data transfer rates using the equation given in Section A.2.

A.3.1 80286 Rates

Clock Rate: 8.0Mhz
Wait States: 2
Bus Time: 600ns
Bytes: 128 Loop Time: 1.13e-004 Data Rate: 1.14e+006

A.3.2 80286 Rates

Clock Rate: 8.0Mhz
Wait States: 0
Bus Time: 250ns
Bytes: 128 Loop Time: 5.33e-005 Data Rate: 2.40e+006

A.3.3 80286 Rates

Clock Rate: 10.0Mhz
Wait States: 0
Bus Time: 250ns
Bytes: 128 Loop Time: 4.58e-005 Data Rate: 2.79e+006

A.3.4 80286 Rates

Clock Rate: 10.0Mhz
Wait States: 0
Bus Time: 125ns
Bytes: 128 Loop Time: 3.78e-005 Data Rate: 3.39e+006

A.3.5 80386 Rates

Clock Rate: 16.0Mhz
Wait States: 1
Bus Time: 250ns
Bytes: 128 Loop Time: 5.23e-005 Data Rate: 2.45e+006

A.3.6 80386 Rates

Clock Rate: 20.0Mhz
Wait States: 1
Bus Time: 250ns
Bytes: 128 Loop Time: 4.51e-005 Data Rate: 2.84e+006

A.3.7 80386 Rates

Clock Rate: 33.0Mhz
Wait States: 1
Bus Time: 250ns
Bytes: 128 Loop Time: 3.36e-005 Data Rate: 3.81e+006

A.3.8 80386 Rates

Clock Rate: 33.0Mhz
Wait States: 0
Bus Time: 250ns
Bytes: 128 Loop Time: 2.91e-005 Data Rate: 4.40e+006

A.3.9 80386 Rates

Clock Rate: 33.0Mhz
Wait States: 0
Bus Time: 100ns
Bytes: 128 Loop Time: 1.95e-005 Data Rate: 6.56e+006

Appendix B Example PIO Transfer Loop

READ OPERATION

```
            mov     es,pointer      Set up ES:DI for memory pointer
            mov     di,pointer
            mov     dx,ioaddr       Set up DX with port address

            sub     totcnt,count    See if count is large enough
            jm      mostdne
            mov     cx,count
start:      in      DMASTAT         Get status
            test    INSTAT
            jnz     intrpt          Jump if SCSI interrupt
            test    DFIFOFULL
            jz      start           Jump if not ready
            rep     insw            Transfer data, cx=count, dx=I/O address
            sub     totcnt,count    Adjust total count
            jm      mostdne         Jump if nearly finished
            mov     cx,count        Set up for next transfer
            jmp     start

mostdne:                            Transfer remaining bytes if any

intrpt:                             Handle SCSI condition
```

WRITE OPERATION

```
            mov     ds,pointer      Set up DS:SI for memory pointer
            mov     si,pointer
            mov     dx,ioaddr       Set up DX with port address

            sub     totcnt,count    See if count is large enough
            jm      mostdne
            mov     cx,count
start:      in      DMASTAT         Get status
            test    INSTAT
            jnz     intrpt          Jump if SCSI interrupt
            test    DFIFOEMP
            jz      start           Jump if not ready
            rep     outsw           Transfer data, cx=count, dx=I/O address
            sub     totcnt,count    Adjust total count
            jm      mostdne         Jump if nearly finished
            mov     cx,count        Set up for next transfer
            jmp     start

mostdne:                            Transfer remaining bytes if any

intrpt:                             Handle SCSI condition
```

Appendix C PC AT DMA Setup

The on-board DMA controller is used for second party DMA operations. The DMA controller is used in demand transfer mode, using 8-bit transfers. The standard AT DMA channels offer 8-bit DMA on channels 0–3. The operations necessary for setting up the DMA controller in an AT system are outlined below.

To use a channel for DMA transfer, the address and byte count must be loaded, the mode register must be set for demand mode and the proper direction, and the mask bit must be cleared. The mask bit is set after each terminal count, and must be cleared for the next transfer. The low-order and mid-order address bytes are loaded in that sequence in the address port. The high-order address byte is loaded in the page register. The byte count is loaded by writing first the low-order then the high-order count into the count port.

Channel	Port Name	Port No.	Data	Comments
0	Mode	0B	04	Read Op
			08	Write Op
	Clear FF	0C		Initialize for address or count write
	Address	00	A7–A0	First write
			A15–A8	Second write
	Page	87	A23–A16	D7-D0
	Count	01	C7–C0	First write
			C15–C8	Second write
	Mask	0A	04	Set mask bit
			00	Clear mask bit

Appendix D PC AT Interrupt

D.1 INTERRUPT INITIALIZATION

The host adapter drives one of several interrupts in the AT system. The particular interrupt used must be set up on power-up initialization, and must be properly managed during usage. The AT interrupts of interest to the host adapter driver, along with their corresponding vector locations are summarized below. All these interrupts are handled by a slave interrupt controller. The master controller handles all system interrupts such as keyboard, timer, etc., and is assumed to be correctly initialized to allow interrupts by the slave controller. Upon receiving an interrupt, the processor is vectored to the contents of the corresponding vector location.

Hardware Interrupt		Software Interrupt Vector Location (hex)
int 9	—	INT 71
int 10	—	INT 72
int 11	—	INT 73
int 12	—	INT 74
int 13	—	INT 76
int 14	—	INT 77
int 15	—	INT 78

The interrupt is initialized by clearing the corresponding interrupt mask bit in the slave controller. The mask register is a write/read register, and only the bit of interest should be cleared. The port address is A1 hex Bit definitions follow.

Interrupt Mask Bit Definition
(port address A1 hex)

bit 0	—	int 8
bit 1	—	int 9
bit 2	—	int 10
bit 3	—	int 11
bit 4	—	int 12
bit 5	—	int 13
bit 6	—	int 14
bit 7	—	int 15

D.2 INTERRUPT RESPONSE

When an interrupt occurs, the interrupting hardware and the slave interrupt controller must be properly serviced. To do this, remove the IRQ signal from the AT bus, reset the interrupt logic in the slave controller by issuing an end of interrupt command (EOI), and reset the interrupt logic in the master-interrupt controller with an EOI command. The order of the setps differs depending on whether the system is using edge-triggered interrupts or level-triggered interrupts.

The standard AT uses edge-triggered interrupts. In this case, service the master interrupt controller first by writing a 20H (EOI value) to port 20H. Then service the slave controller by issuing a 20H to port A0H. Then service the board which caused the interrupt to remove it. This sequence prevents another interrupt from the board being missed.

If level-triggered interrupts are used in a system, the board should be serviced first, then the slave controller, then the master controller. This sequence prevents a double response to the same interrupt.

Single-Chip PC AT-to-SCSI I/O Processor

Data Sheet Errata
July, 1991

Data Sheet Corrections

1. Pin 48 of the PLCC package was incorrectly shown to be a ground on the 2/91 and 5/91 editions of the data sheet. It should be connected to +5V.

2. In the SCSI Rate Control Register (344h) the bit order for the Synchronous Transfer Rate is Bit 6=0, Bit 5=1, Bit 4=1 for a 4.00 MB/s rate. In the first edition of the data sheet, the bit order was misleading, but was clarified starting with the 2/91 edition of the data sheet.

3. In Section 5.1.1, Step 5, of the Application Notes chapter, the TEMODE0 bit should be reset. The first edition of the data sheet incorrectly stated that it should be set. It was corrected starting with the 2/91 edition of the data sheet.

4. In the description of the CLRCH1 bit in the SCSI Transfer Control 0 register (341h), it incorrectly states that it clears the SCSI Transfer Counter (348h-34Ah). To clear the SCSI Transfer Counter, use the CLRSTCNT bit in the same register.

Operational Clarifications and Bugs

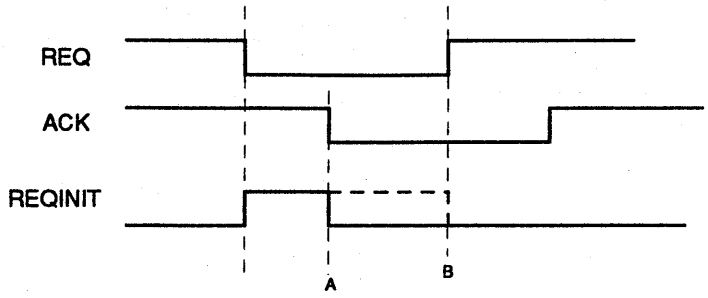
1. The REQ interrupt (REQINIT), instead of turning off upon assertion of ACK (point A), clears itself on deassertion of REQ (point B). See the attached timing diagram.

2. If programming the AIC-6260, the SCSI Test Control (SCSITEST) and Test Registers must be cleared before beginning programming. They are registers 34Eh and 35Eh, respectively.

3. When reading data from a SCSI Target, the DFIFOFULL bit in the DMA Status Register (354h) is set when there are 132 bytes ready to be read by the host. This is due to host bus holding registers which account for four additional bytes.

4. The FIFO counter (FIFO STATUS Register, 355h) cannot be read dynamically. It can only be reliably read when all data transfer activity has ceased, such as when a SCSI Phase change has occurred.

5. The Parity Error Status Bit (SCSIPERR) in the SSTAT1 register (34Ch) does not operate correctly when a SCSI bus parity error occurs. The problem is that this bit is the logical OR of two latches, one of which contains the parity status of the previous phase (OLD-PARITY STATUS), and the other, the current parity status (CURRENT-PARITY STATUS) of the SCSI bus. If a parity error occurs while the SCSI bus is in the data in-direction (DATA-IN, STATUS, or MESSAGE-IN Phases), the CURRENT-PARITY STATUS latch would become set. Immediately the Target would change the SCSI bus to the data-out direction and the OLD-PARITY STATUS latch would be set. Upon seeing a parity error, the software would try to clear SCSIPERR by using the CLRSCSIPERR control in register 34Ch. However, this control will only clear the OLD-PARITY STATUS latch while the CURRENT-PARITY STATUS latch can only be cleared by receiving in good parity in the data-in direction or turning off parity checking entirely. Because of this, SCSIPERR cannot be cleared, making detection of the phase in which the parity error occurred difficult.



REQINIT Timing

ALTERNATE=5V Primary Register Address	**ALTERNATE=0V** Secondary Register Address	Read Register	Write Register
340	140	SCSISEQ	SCSISEQ
341	141	SXFRCTL0	SXFRCTL0
342	142	SXFRCTL1	SXFRCTL1
343	143	SCSISIGI	SCSISIGO
344	144	None	SCSIRATE
345	145	SELID	SCSIID
346	146	SCSIDAT	SCSIDAT
347	147	SCSIBUS	None
348	148	SICNT0	STCNT0
349	149	STCNT1	STCNT1
34A	14A	STCNT2	STCNT2
34B	14B	SSTAT0	CLRSINT0
34C	14C	SSTAT1	CLRSINT1
34D	14D	SSTAT2	None
34E	14E	SSTAT3	SCSITEST
34F	14F	SSTAT4	CLRSERR
350	150	SIMODE0	SIMODE0
351	151	SIMODE1	SIMODE1
352	152	DMACNTRL0	DMACNTRL0
353	153	DMACNTRL1	DMACNTRL1
354	154	DMASTAT	None
355	155	FIFO STAT	None
356	156	DATAPORTL/H	DATAPORTL/H
357	157	None	None
358	158	BRST CNTRL	BRST CNTRL
359	159	None	None
35A	15A	PORT A	PORT A
35B	15B	PORT B	PORT B
35C	15C	REV	None
35D	15D	STACK	STACK
35E	15E	None	Test
35F	15F	None	None

AIC-6260 Register Map

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