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AHA-1740A / 1742A / 1744
EISA-to-Fast SCSI Host Adapter

Technical Reference Manual

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NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in residential installations. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

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- Move the equipment away from the receiver
- Plug the equipment into an outlet on a circuit different from that to which the receiver is powered
- If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions

CAUTION: Only equipment certified to comply with Class B (computer input/output devices, terminals, printers, etc.) should be attached to this equipment, and must have shielded interface cables.

Finally, any change or modifications to the equipment by the user not expressly approved by the grantee or manufacturer could void the user's authority to operate such equipment.

Each AHA-1740A/1742A/1744 is equipped with an FCC compliance label which shows only the FCC Identification number. This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

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Preface

This Technical Reference Manual provides technical information for Adaptec's AHA-1740A/1742A/1744 EISA-to-Fast SCSI Host Adapters. It is prepared for customer technical personnel requiring detailed information on the operation of the board at a register and command protocol level. Documentation of board schematics, integrated circuits, microcode and BIOS routines is not provided.

Programmers writing device drivers for specific perpherals are strongly advised to use the Advanced SCSI Programming Interface (ASPI) specification appropriate to the operating system chosen. This will allow flexibility across all boards complying with ASPI Manager modules and prevent obsolescence. Please contact Adaptec Corporate Communications for copies of ASPI specifications. Software managers are documented and sold separately.

Every effort has been made to ensure the technical accuracy of this reference manual. If you believe that inaccuracies exist, please communicate this information in writing to your local field applications support personnel or directly to the product manager.

Conventions

The following typographic conventions are used throughout this Technical Reference Manual.

bold
Used for keystrokes (.. press the **Enter** key ..) and screen selection fields (.. select **Backup Device** and ..).

Helvetica
Used for operator entry that must be typed exactly as shown
(.. device=c:\cdrom\cdrom.tsd ..) and for screen messages (.. Enter Password ..).

Helvetica Italics
Used as a placeholder for text you must determine and type in (.. enter *nn* for number ..). Also used for program and file names in body text (.. the *autoexec.bat* file ..).

Italics
Used for emphasis (.. is *only* supported ..) and document reference (.. refer to Chapter Three, *Installation* ..).

ALL CAPITALS
Used for acronyms (..the SCSI device..).

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Chapter One

Introduction

Document Scope

This manual provides information on installation and defines the program interfaces of the AHA-1740A/1742A/1744 intelligent host adapters in EISA bus-based systems. Programming peripheral drivers directly to the hardware interface of the board is not recommended. The ASPI (Advanced SCSI Programming Interface) specifications provide a simpler and more flexible interface which is protected against changes, upgrades and obsolescence of the boards.

Purpose

The Adaptec AHA-1740A/1742A/1744 provides a powerful multitasking interface between the Extended Industry Standard Architecture (EISA) bus and the Small Computer System Interface (SCSI) bus.

The AHA-1740A/1742A/1744 is a high-performance intelligent host adapter which supports a maximum asynchronous SCSI rate of 2.0 MBytes/second and a synchronous transfer rate of 10.0 MBytes/second. It supports multithreaded I/O operations, allowing simultaneous operations on multiple targets/LUNs. Disconnect/Reconnect support maximizes bus utilization for multiple target systems. Target mode operation allows the AHA-1740A/1742A/1744 to receive information from other host adapters. Scatter/Gather allows high performance even in systems with fragmented memory buffers.

The AHA-1740A/1742A/1744 provides a solution for system applications requiring very high performance, configuration flexibility, multithreaded I/O capability, and system redundancy. The Adaptec BIOS also allows the AHA-1740A/1742A/1744 to be used in place of a standard hard disk controller.

The AHA-1740A/1742A host adapter provides high-performance host adapter circuitry connected to the more common single-ended SCSI bus. The SCSI specification recommended maximum cable length for 5 MBytes/second synchronous data transfer is 6 Meters, or about 20 feet.

The AHA-1744 host adapter provides identical host adapter circuitry, but connects to a differential SCSI bus. The SCSI specification recommended maximum cable length for 5 MBytes/second synchronous data transfer is 25 Meters, or about 82 feet.

AHA-1740A/1742A/1744 Product Features

EISA Features

The AHA-1740A/1742A/1744 is a full-performance EISA board offering the highest performance available across the bus. It takes advantage of first-party DMA operations, also known as bus mastering, which allow data transfers to proceed at high data rates without system processor intervention. The main EISA functions which come standard on the board include:

- Auto Configuration Support
- High-performance Bus Master transfers with burst cycles which provide a data rate of 33 MBytes/second
- 32-bit data path
- 32-bit address space
- Even or odd starting address and byte count handling
- 1K FIFO for efficient data transfer
- Interrupts enabled/disabled through I/O port write
- Interrupts configurable for either edge or level trigger
- Dual Control Interface, AHA-1540 family-compatible (Standard Mode) or EISA-SCB compatible (Enhanced Mode)

SCSI Features

Adaptec has long been a supplier of leading edge SCSI products and the AHA-1740A/1742A/1744 is no exception. The board uses industry-standard protocol ICs which fully comply with the 1990 ANSI SCSI specification, including:

- Maximum synchronous SCSI transfer rate of 10.0 MBytes/second (Fast SCSI)
- Asynchronous and synchronous peripherals supported simultaneously
- Disable synchronous negotiation independently on each target as a configuration option
- Disable disconnection independently on each target as a configuration option
- Supports Modify Data Pointer message (Zero Latency Reads)
- High-density SCSI-2 connector
- Non-destructive current limit on terminator power supply

- Internal and external SCSI connectors
- Initiator and target modes of operation fully supported
- Differential SCSI (AHA-1744 only)
- SCSI-1 and SCSI-2 compatible
- Tagged queuing

Board Features

In addition to extensive functions on the two main interfaces of the board, the intelligence built into the board microcode and BIOS software allows a number of additional functions to be offered, including:

- Scatter/Gather operation
- Boot from any target (set as configuration option)
- Compatible with existing AHA-1540 family driver software (ASW-1400 series managers)
- True multithreaded operation supporting up to 255 tasks simultaneously
- Programmable mailbox architecture
- Bootable BIOS for standard hard disk emulation
- Floppy Diskette Controller (AHA-1742A only)

While all versions of the board fully support all of the above features, they are distinguished by:

- AHA-1740A Fast SCSI-to-EISA Host Adapter
- AHA-1742A Fast SCSI-to-EISA Host Adapter with floppy diskette controller
- AHA-1744 Fast differential SCSI-to-EISA Host Adapter

The AHA-1740A/1742A/1744 microcode is available *in two separate versions which coexist simultaneously in the onboard PROM*, but must be configured into one of the two available modes:

- Standard Mode
- Enhanced Mode

The modes cannot operate simultaneously. The EISA Configuration Utility (ECU) must be run to select one of the modes (Refer to Chapter Three, *Installation*). The

mode dictates the software manager revision which can support the board, but has no effect on the SCSI or host bus hardware connections.

Standard Mode allows software drivers written for the AHA-1540 or AHA-1640 families to run unaltered on the AHA-1740 family. There is no performance penalty for this on the EISA bus. The AHA-1740A/1742A/1744 still performs 32-bit transfers at speeds up to 33 MBytes/second.

Enhanced Mode allows the board to take advantage of a number of features which were not available on earlier host adapters. These include:

- Fast SCSI data transfer
- 32-bit addressing capability
- Ability to access all EISA board registers
- Single fast mailbox handling
- Tagged queuing (SCSI)
- Fully configurable SCSI bus options for each SCSI target ID

Configuration Diskette and Installation Guide (ASW-C174)

As with other EISA boards, the AHA-1740A/1742A/1744 is configured by the EISA Configuration Utility (ECU) that came with your EISA computer. The ASW-C174 diskette contains the configuration and overlay files required by the ECU for the AHA-1740A/1742A/1744. In addition, the ASW-C174 contains a utility for checking the version of microcode in your AHA-1740A/1742A/1744 and for low-level formatting of hard disks.

> Note
> The AHA-1740/1744 stores microcode in an E^2PROM. You can download microcode to it by using the *adl.exe* download utility included on the ASW-C174. The AHA-1740A/1742A stores microcode in an EPROM. The A version boards do *not* support the download feature.

Product Specifications

Physical Dimensions	
Length	13-3/8 inches
Width	5/8 inch
Height	5 inches
Standard EISA-compatible form factor.	
Power Requirements	
+5.0 +/- 0.25 Volts at 2.9 Amps maximum.	
Environmental Requirements	
Temperature 0-55° C (operating or storage)	
Reliability Information	
Mean Time Between Failures: 100,000 hours (calculated per Mil Handbook 217E, ground benign, 40° C)	
Mean Time Between Failures: (calculated)	
1740A	61,466 hours
1742A	60,589 hours
1744	54,856 hours
Mean Time to Repair: 30 minutes	

Extended Industry-Standard Architecture Interface

Standard EISA Bus Electronic and Physical Interface

Driver Output Signals		
V_{OL}	0 volts minimum	0.4 volts maximum
I_{OL}	24 mA	
V_{OH}	2.4 volts minimum	5.25 volts maximum
I_{OH}	8 mA	
Receiver Input Signals		
V_{IL}	0.8 volts maximum	
V_{IH}	2.0 volts minimum	

Connector configuration as specified by manual of Extended Industry Standard Architecture host computer.

SCSI Interface

Electrical Interface for AHA-1740A/1742A

As specified by ANSI X3.131-1986 for single-ended operation.

Output Signals

All signals use open collector or three-state drivers. Each signal driven by a SCSI device has the following output characteristics when measured at the SCSI device's connector:

Signal	Definition	Characteristics
V_{OL}	Low-level output voltage	0.0 to 0.5 volts DC at 48 mA sinking (signal assertion)
V_{OH}	High-level output voltage	2.5 to 5.25 volts DC (signal negation)

Input Signals

SCSI inputs meet the following electrical characteristics on each signal (including both receivers and passive drivers):

Signal	Definition	Characteristics
V_{IL}	Low-level input voltage	0.0 to 0.8 volts DC (signal true)
V_{IH}	High-level input voltage	2.0 to 5.25 volts DC (signal false)
I_{IL}	Low-level input current	-0.4 to 0.0 mA at V_I = 0.5 volts DC
I_{IH}	High-level input current	0.0 to 0.1 mA at V_I = 2.7 volts DC
Minimum input hysteresis = 0.2 volts DC. Maximum input capacitance = 25 pF (measured at the device connector closest to the stub, if any, within the device).		

Electrical Interface for AHA-1744

As specified by ANSI X359.2/86-109 Rev. 10h for differential alternatives.

Output Signals

Each signal driven has the following output characteristics when measured at the SCSI device's connector:

Signal	Definition	Characteristics
V_{OL}	Low-level output voltage	1.7 volts DC maximum at I_{OL} (low-level output current) = 55 mA)
V_{OH}	High-level output voltage	2.7 volts DC minimum at I_{OH} (high-level output current) = -55 mA)
V_{OD}	Differential output voltage	1.0 volts DC minimum with with common-mode voltage ranges from -7 to +12 volts DC
V_{OL} and V_{OH} are measured between the output terminal and the SCSI device's logic ground reference.		

Input Signals

SCSI inputs meet the following electrical characteristics on each signal (including both receivers and passive drivers):

Signal	Definition	Characteristics
I_I	Input current on either input	+/- 2.0 mA maximum
Maximum input capacitance = 25 pF. The I_I requirement is met with the input voltage varying between -7 and +12 volts DC, with power on or off, and with the hysteresis equaling 35 millivolts, minimum.		

Internal Connector

Unshrouded 50-pin header, compatible with unshielded alternative 1 connector as specified in ANSI X3.131-1986 (Figure 4-1).

For connector pin out and drawing of the connector, see Appendix B.

Partial list of compatible connector plugs (for reference only):

Manufacturer	Model	Part Number
3-M	N.A.	3425-6000
T&B Ansley	N.A.	609-5000M

The cable for the internal SCSI connector should be good quality 50-conductor flat cable with 26- or 28-gauge conductors and a characteristic impedance (Z_0) of 100 +/-10 ohms. Cable shielding is necessary if extremely noisy circuitry or extremely noise-sensitive circuitry is present inside the host computer frame.

External Connector

Shielded 50-pin high density (Alternative 1) connector as specified in proposed ANSI standard X3T9.2/86-109 Revision 10h, Section 4, Figure 5.

For connector pin out, see Appendix B.

Partial list of compatible connector plugs or cable assemblies (for reference only):

Manufacturer	Model	Part Number
AMP	Connector	749111-4
	Back Shell	749193-1
Fujitsu	Connector	FCN-237R050-G/F
	Back Shell	FCN-230C050-D/E or -C/E
Honda	Connector	PCS-XE50MA
	Back Shell	PCS-E50LA

Cable for external SCSI connector should be good quality 100% shielded round cable with 25 twisted pairs. Each pair should have a characteristic impedance (Z_0) between 90 ohms and 135 ohms. Wire gauge may be 26 or 28 AWG. All pairs should have the same impedance and should have the same delay per length of cable. Cables meeting these requirements will normally operate correctly in any SCSI configuration and should normally meet all FCC requirements.

For best results, the SCSI committee recommends that SCSI connectors should not be placed less than one foot apart on internal (ribbon) cable or on external cable when using Fast SCSI 10 Mbytes/second data transfers.

Cable material which meets this specification is available from a number of vendors, including:

Manufacturer	Part Number	Phone
C&T	16035	
Madison	4099	(508) 752-7320

Complete cable assemblies are available from a number of manufacturers. Among them are:

Manufacturer	Phone
Amphenol Interconnect Products	(607) 786-4370
Lynn Products Inc.	(800) 634-5093
Quitec Interconnect Systems	(408) 272-8000
Icontec	(408) 945-7766
Enhance Cable Technology	(408) 293-2425

Floppy Disk Interface

Standard Electronic and Physical interface

Driver Output Signals		
V_{OL}	0 volts minimum	0.5 volts maximum
V_{OH}	Open collector	5.25 volts maximum
I_{OL}	60 mA	
I_{OH}	0.1 mA	
Receiver Input Signals		
V_{T-}	1.0 volts maximum	
VT+	1.4 volts minimum	
Tied to +5 volt supply through 150 ohm resistors. Schmidt Trigger with 0.8-volt hysteresis		

Connector

Unshrouded 34-pin header. Partial list of compatible connector plugs (for reference only):

Manufacturer	**Model**	**Part Number**
3-M	N.A.	3414-6000
T&B Ansley	N.A.	609-3400M

The cable for the floppy connector should be good quality 34 conductor flat cable with 28 gauge conductors. Addressing of the second drive may be generated by twisting connector signals 10 through 16 or by changing jumpers in the floppy disk drives.

Radiation Immunity

Meets radiation limits specified for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules. See FCC Compliance notes and recommendations in preface of this document.

Reference Documents

- EISA Specification, v3.11 from BCPR Services
- Intel 82355 (BMIC) functional data sheet Revision 2.5 or later
- Small Computer System Interface, ANSI X3T9.2/86-109 Revision 10h, American National Standards Institute

- Adaptec AHA-1740A/1742A/AHA-1744 Host Adapter Installation Guide Using the ASW-C174
- Intel® 82077A Floppy Disk Controller Data Sheet

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Chapter Two

Architecture

Hardware

The hardware of the AHA-1740A/1742A/1744 products is based on the latest VLSI technology for maximum performance in a minimum of board space. Where commercial products with sufficient performance and functionality were not available, Adaptec has developed custom circuits using its long experience in high-performance silicon design for peripheral control applications. These parts are assembled on a multilayer printed circuit board in Adaptec's volume manufacturing plant and subjected to a number of functional and mechanical inspections and tests.

The general architecture of the board is shown in Figure 2-1.

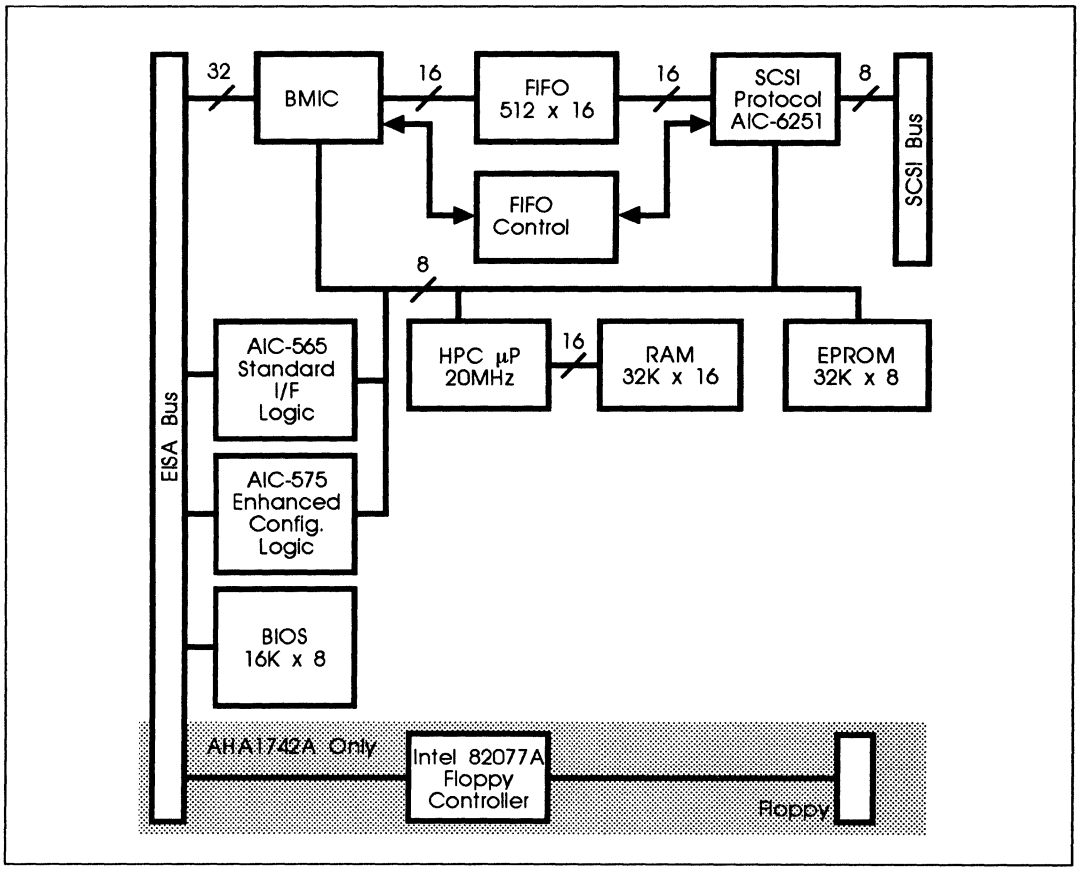

Figure 2-1. AHA-1740A/1742A Block Diagram

Bus Master DMA

The AHA-1740A/1742A/1744 controls the host EISA bus as a master and transfers data directly to and from main system memory. This implementation is known as Bus Master DMA. Bus Master DMA greatly reduces the host software overhead because the host CPU is no longer required to maintain the DMA channel's address pointers and word counts. Bus Master DMA also reduces the number of interrupts generated per I/O command. The Intel BMIC includes the functions of the DMA controller.

Adaptec's implementation of Bus Master DMA can achieve a 33 MByte/second burst data rate. This speed is especially valuable in multitasking systems where the tasks execute on a time shared basis. Appendix A, *Memory Cycle Timing Diagram* shows a diagram of the timing required to achieve the DMA rates that are supported by the AHA-1740A/1742A/1744.

The host adapter uses burst cycles on the EISA bus if the memory supports the transfer by asserting SLBURST*. If not, the host adapter will use 32-bit wide data transfers with the normal 2 cycle timing. The adapter relies on system translation logic when reading or writing 16-bit expansion board memory in nonburst mode.

The AHA-1740A/1742A/1744 DMA hardware will handle both odd-byte and odd-memory address data transfers with no performance degradation. The adapter has the ability to align bytes when the starting address is not a multiple of four or the byte count is an odd value. It will transfer 1, 2, or 3, bytes at the beginning or end of the transfer so that 32-bit burst cycles may be used.

The adapter will also be an 8-bit I/O slave with registers for use during setup and operation. Two modes of operation are defined which are mutually exclusive. The two modes are the AHA-1540 Standard Mode and the AHA-1740 Enhanced Mode. The current AHA-1540 ISA register set is implemented for software compatibility. The I/O address is selected by programming a configuration register. AHA-1740 Enhanced Mode is implemented to give extended addressing ability as well as additional SCSI-2 features not available in Standard Mode. Several configuration registers are implemented in EISA I/O space to allow autoconfiguration.

The user may program the adapter to use interrupts 9, 10, 11, 12, 14, and 15. The interrupt may also be programmed to a high or low level. When the high level is used, the board will be compatible with the ISA implementation, and current drivers. When the low level is used, the interrupt may also be shared and EISA drivers may be written to use multiple boards on the same interrupt.

SCSI Interface and Protocol Chip (AIC-6251)

The host adapter supports SCSI functions that are a superset of Adaptec's AT® (AHA-1540 family) and Micro Channel® (AHA-1640) host adapters. The AHA-1740 supports new SCSI-2 features such as tagged queuing and 10 MBytes/second data transfers (Fast SCSI). In particular, the adapter supports synchronous negotiation to 10 MBytes, up to an offset of seven, and it will support the Modify Data Pointers extended message, Tagged Queuing, and Contingent Allegiance. Note that fast,

synchronous and asynchronous peripherals can be freely mixed on a cable connected to the AHA-1740A/1742A/1744.

In addition, the host adapter has the ability to select particular targets during configuration to initiate synchronous negotiation, enable parity checking, send start-up, and allow disconnection. The current limiting fuse on other host adapters has been replaced with a thermistor to allow nondestructive current limiting of terminator power supplied to the SCSI cable.

The AHA-1740A/1742A/1744 utilizes the Adaptec AIC-6251 Fast SCSI protocol chip to maximize the SCSI bus utilization. The AIC-6251 is an Adaptec VLSI development of the popular AIC-6250 device which allows the AHA-1740A/1742A/1744 to achieve greater than 2.0 MBytes/second asynchronous SCSI data transfer rates, and up to 10 MBytes/second synchronous data transfer rates. The AIC-6251 will also enable the AHA-1740A/1742A/1744 to operate simultaneously as both an initiator and as a processor target device.

Through a 16-bit interface internal to the board, the AIC-6251 reduces bus busy time during data transfer by allowing a bursting data across the EISA bus at up to 33 MBytes/second. The AIC-6251 has separate data buses for the local microprocessor and for the system data bus. This further increases the performance of the AHA-1740A/1742A/1744 by reducing the overhead associated with SCSI commands.

8- and 16-Bit Memory and Odd Byte Data Transfers

The AHA-1740A/1742A/1744 will automatically shift to 8- or 16-bit data transfers as indicated by the control lines on the EISA bus. Bus master data transfers into 8- or 16-bit wide memory are fully supported as are full 32-bit wide data transfers.

During normal DMA operations, nearly all transfers to and from memory are 32-bit transfers. At the very end, or the very beginning of an odd address boundary, an 8-bit, 16-bit, or 24-bit transfer may occur.

Bus Auxiliary Interface Chip (AIC-565)

This highly integrated ASIC (Application Specific Integrated Circuit) device developed by Adaptec is also used with the AHA-1540B host adapter family. It provides the Standard Mode programming interface and implements the following main functional blocks:

- Bus control interface for Standard Mode
- Host adapter microprocessor interface
- BIOS decode logic

The bus control interface section decodes the possible base addresses for the board I/O port address, including a select external to the board. It also provides all registers used to communicate between the host adapter and the motherboard which are accessed through the bus in Standard Mode. This ensures full compatibility with software written for the AHA-1540/1542 family of AT Bus Master Host Adapters.

EISA Configuration Chip (AIC-575)

The host adapter provides a number of options which may be programmed at configuration time. They are summarized below:

- AHA-1540 base port address
- Bus on time after preempt
- Interrupt definition and selection
- Synchronous negotiation enable/disable per target
- Disconnection enable/disable per target
- Boot drive identification for DOS
- BIOS enable, location, and options

The following versions of the ASW-1400 family of software managers support these features:

- ASW-1410, v3.0 and later
- ASW-1420, v1.3 and later
- ASW-1440, v3.0 and later
- ASW-1450, v1.0 and later

BMIC Bus Interface Chip (82355)

This highly integrated ASIC device from Intel controls and interfaces to the EISA bus. It implements the following main functional blocks:

- 32-bit bus interface
- Adapter FIFO interface
- EISA bus protocol logic

Floppy Disk Controller (AHA-1742A Only)

This is implemented by a 82077A single-chip floppy disk drive controller. All drive control signals are fully decoded and have 40 mA drive buffers with selectable polarity. Signals returned from the drive are sent through on-chip input buffer with hysteresis for noise immunity. The integrated analog data separator needs no external compensation yet allows for a wide motor speed variation with exceptionally low soft error rates. The microprocessor interface has a 12 mA drive buffer on the data bus plus 100% hardware register compatibility for standard systems. The 16-byte FIFO with programmable thresholds is extremely useful in multimaster systems, or

systems with a large amount of bus latency, typically found in performance EISA systems.

Standard Mode Firmware

The AHA-1740A/1742A/1744 support multithreaded SCSI initiator operation through a simple mailbox protocol. The firmware accepts as many Command Control Blocks (CCBs) as required and executes them from its local RAM. The firmware controls all of the SCSI activity that a task may require, including:

- Arbitration
- Selection
- Disconnection
- Reconnection
- Command completion

Using the same mailbox protocol, the AHA-1740A/1742A/1744 can operate as a processor-type device serving as a multitasking target to other initiators. This feature allows high bandwidth communication between multiple hosts.

In addition, the AHA-1740A/1742A/1744 firmware cooperates with the BIOS installed on the host adapter to emulate the standard DOS BIOS calls. This allows booting operations and the execution of standard DOS operations from attached SCSI disks, allowing the SCSI subsystem to completely replace the usual internal disk functions.

A multiuser, multitasking operating system issues a large number of I/O tasks in a rapid sequence. The architecture of the AHA-1740A/1742A/1744 makes management of this activity very easy and straightforward for the operating system and its associated I/O drivers. This section briefly explains the interaction between the system and the AHA-1740A/1742A/1744 required to accomplish an I/O task in standard mode.

Mailboxes

The AHA-1740A/1742A/1744 Standard Mode uses a mailbox architecture for task communication between the host and host adapter. This allows the host adapter to perform multithreaded operations with a minimum of host intervention. The mailboxes are located in main system memory. Each mailbox entry is four bytes long. After power-up sequencing, host initialization procedures, and the boot procedure are completed, the host issues an initialization command to inform the host adapter of the mailbox location. There is always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). MBIs are located immediately after the MBOs.

A typical mailbox structure is:

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example there are four MBOs and four MBIs. The first byte of each MBO contains the MBO Command byte. The remaining three bytes point to a Command Control Block (CCB). The CCB provides all the rest of the information needed to complete a task. An MBO is available to accept a new entry if the first byte is zero.

The first byte of each MBI contains the status of a completed task. The remaining three bytes point to the CCB of the completed task. An MBI is free if the Status byte is zero. Mailboxes may point to CCBs controlling initiator tasks, controlling target tasks, or controlling error recovery tasks.

Command Control Block

A Command Control Block provides the information required to control a SCSI command sequence. The block contains pointers to the data area to be used by the command. It contains areas for presenting status of both the host adapter and the addressed SCSI device. In addition, it contains the SCSI Command Descriptor Block defining the action to be taken by the addressed SCSI device. An error information buffer area is also provided.

A Command Control Block is also used to service an operation requested by another initiator when the AHA-1740A/1742A/1744 is being addressed as a SCSI Processor device. The CCB is defined completely in Chapter Five, *Standard Mode Firmware Description.*

A typical CCB is shown below:

Byte 0	Command Control Block Opcode			
+1	Tar/Init	Data Out	Data In	LUN
+2	SCSI Command Length = m			
+3	Returned Sense Info Length = n			
+4	Data Length (MSB, MID, LSB)			
+7	Data Pointer (MSB, MID, LSB)			
+10	Link Pointer (MSB, MID, LSB)			
+13	Command Link ID			
+14	Host Status			
+15	Target Status			
+16	Reserved			
+17	Reserved			
+18	SCSI Command Bytes (m Bytes)			
18 + m	Allocated for Sense Data (n Bytes)			

Command Descriptor Block

The Command Descriptor Block (CDB), a part of the Command Control Block, is a standard format command packet that is transmitted to the addressed SCSI device. It contains all the command information required by the SCSI device to perform the desired operation. The Command Descriptor Block contains the command Operation Code followed by a Logical Unit Number (LUN), command parameters if required, and a control byte. A typical Group 0 6-byte CDB is shown below:

	Bit 7	6	5	4	3	2	1	0
Byte 0	Operation Code							
1	LUN			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	Vendor Unique			Reserved			Flag	Link

Please refer to the *SCSI specification ANSI X3.131*, the *Common Command Set (CCS) revision 4B,* and the *SCSI-2 draft* for additional information on Command Descriptor Blocks.

Principles of Operation

At power-up, the host must inform the host adapter of the location and number of mailboxes. To start a task, the host builds a CCB and stores its memory address into a free mailbox. A nonzero Mailbox Out command byte is then written to indicate that the mailbox entry is full and valid. The host then writes to an I/O port (see Chapter Four, *Hardware Functional Description*) to indicate that the host adapter should scan the MBO area. When a full MBO is found, the host adapter copies the mailbox's CCB pointer into its internal RAM and clears the mailbox entry by writing a zero to the MBO command byte. This frees the MBO so that it can be used to start another task.

After completing a task, the host adapter scans the MBI area for a free mailbox. When one is found, it is updated with the task's completion status and CCB pointer. The CCB pointer identifies the completed task. An MBI stored interrupt is generated to notify the host that a task has been completed. The host scans the MBI area searching for a nonzero Status byte. When one is located, the host obtains the CCB pointer and frees the MBI by writing a zero into the Status byte. The host then examines the contents of the CCB to determine that the command was successfully completed. The freed MBI can now be used to indicate the completion of another task. The host adapter fills the MBI area and scans the MBO area in a round-robin fashion. If the host saves the position of the last active MBI entry, it can determine the MBI of a new entry immediately without searching, since a new entry will be in the next MBI location.

The host adapter transmits a new MBO Available or MBI Full interrupt to the host whenever all non-mailbox interrupts have been cleared and serviced by the host. The host should analyze the interrupts and clear them as soon as possible so that the host adapter can post any new interrupts quickly. The host adapter will not wait until an interrupt can be transmitted to the host before processing an MBO entry or creating a new MBI entry. Thus, in processing a single MBI interrupt, the host may find several MBI entries waiting by the time the interrupt processing is finished. Similarly, a later MBI interrupt for the last of the later MBI entries may find nothing to service because the MBI entry was examined and processed as a result of the first MBI Full interrupt. If the interrupts are reset quickly by the host, the probability of an interrupt occurring when no MBI entry is available is much lower, providing an important performance improvement. If the MBI entries are emptied by the host in a round-robin order, the scan for the next full entry is very simple, since it is always the next MBI entry in the mailbox area.

Task Queuing

Multiple tasks may be started against a target/LUN or against multiple targets/Logical Units. Since only one task can be active against any one LUN at a time, all other tasks for the same LUN are queued. Other LUNs may have active tasks at the same time.

The host adapter dequeues on a first in, first out (FIFO) basis for each target/LUN combination. However, due to the optimization algorithm used by the host adapter, a task may sometimes be started earlier in spite of its late entrance in the queue on multiple target/LUN systems. Task queuing should not be used where changes in the order of command execution may cause data integrity failures.

Enhanced Mode Firmware

The Enhanced Mode is an interface architecture which allows the AHA-1740A/1742A/1744 to take full advantage of the EISA bus facilities. It utilizes a distinct hardware interface control logic, implemented in the AIC-575 device. This permits features such as full 32-bit addressing and the entire EISA register set to be used. This mode is not compatible with older versions of the ASW-1400 series of software managers.

The following levels of manager revision are capable of operating with the AHA-1740A/1742A/1744 in Enhanced mode:

- ASW-1410 v3.0 and later (ASPI DOS Manager)
- ASW-1420 v1.3 and later (LADDR SCSI Support for OS/2®)
- ASW-1440 v3.0 and later (ASPI Manager for Novell NetWare®)
- ASW-1450 v1.0 and later (SCSI Manager for SCO UNIX® and Open Desktop)

In order to use the Enhanced Mode, the AHA-1740A/1742A/1744 must be correctly reconfigured. Use the EISA Configuration Utility (EISA) that came with your EISA system and the EISA configuration files on the ASW-C174 diskette provided with the AHA-1740A/1742A/1744. The AHA-1740A/1742A/1744 are not capable of simultaneous operation in Standard and Enhanced Modes.

The firmware in this mode uses a different architecture to the Standard Mode. The firmware is interrupt driven by events on the host and SCSI side. It uses only a single mailbox, unlike the Standard Mode which uses up to 255. This does not result in any bottleneck or performance impairment, due to the fast processor used on the AHA-1740A/1742A/1744 and the servicing algorithm used.

The control block is a 48-byte structure created and maintained in shared memory by software in the system unit. It is used to convey requests to the host adapter.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
Command Word																00
Flag Word 1																02
Flag Word 2																04
																06
Data or Scatter/Gather List Pointer																08 0A
Data or Scatter/Gather List Length																0C 0E
Status Block Pointer																10 12
Chain Address																14 16
																18
																1A
Sense Information Pointer																1C 1E
CDB Length								Sense Length								20
Data Checksum																22
CDB Byte 1								CDB Byte 0								24
CDB Byte 3								CDB Byte 2								26
CDB Byte 5								CDB Byte 4								28
CDB Byte 7								CDB Byte 6								2A
CDB Byte 9								CDB Byte 8								2C
CDB Byte 11								CDB Byte 10								2E

A full description of the control block and its operation is provided in Chapter Six, *Enhanced Mode Firmware Description.*

Onboard BIOS Operation

A host adapter BIOS is provided to emulate the standard hard disk BIOS and boot functions. With this BIOS, the host adapter can be used in lieu of a standard hard disk controller on any ISA-compatible system.

The BIOS is compatible with the standard hard disk BIOS. This allows DOS to access up to two hard disk devices on the SCSI bus without a driver. All normal I/O functions are supported including system booting. Single-threaded operation and multithreaded operation do not operate simultaneously. Single-threaded operation cannot be requested until all multithreaded operations are completed. Similarly, all multithreaded operations must be complete before a single-threaded operation can be requested. For most multitasking operating systems, such as Xenix® and OS/2, single-threaded operation is normally used only for the early part of the boot operation, after which multithreaded drivers take over all control of the SCSI operations.

During system boot, the BIOS will scan for the availability of configuration information in the free-form data area of system RAM. If it finds the correct data format, it will use this data to configure both the board parameters and parameters associated with the peripherals on the SCSI bus. If data cannot be found or correctly recognized, the BIOS will configure the board to a default set of parameters. Refer to Chapter Three, *Installation* for details.

Power-Up Diagnostics

After power on, the host adapter initializes the firmware to 16-bit RAM for execution. After the firmware is running, the Extended ID is written to the registers. Several onboard diagnostics are then performed.

- RAM is verified
- Write/Read registers are checked for proper operation
- The data path is checked for correct internal operation

The red Light-Emitting Diode (LED) on the host adapter indicates the result of the self diagnostic process. When power is first applied to the board, the LED turns on. If the board is operating normally, the light will soon go off and stay off until SCSI or I/O port activity is requested by the host. If the board is not operating correctly, a flash code number is flashed on the LED to indicate which test failed. The flash code number is indicated by a series of one to three closely spaced flashes, followed by a longer pause, or a continuous series of flashes. The flash code is repeated continuously until the board is powered off or reset. The SCSI interface should be disconnected if these diagnostic tests are being run for fault isolation purposes. At least one set of terminators must remain installed or the LED will stay on, indicating that the AHA-1740A/1742A/1744 is receiving an active RST signal. The flash code and associated failure modes are indicated in the following table.

Flash Code	Possible Meanings of Flash Code
LED Remains On	Host Adapter Control Processor inoperative, terminators missing or not powered, or card enable has not been asserted after reset.
1 Flash	RAM test failed.
2 Flashes	AIC-6251 SCSI protocol chip verification failed.
3 Flashes	FIFO write/read data path test failed.
Continuous Flashes	EEPROM has not been programmed.

ASW-C174 Configuration Diskette

The AHA-1740A/1742A/1744 is normally supplied with configuration software, product number ASW-C174. This includes 5.25-inch and 3.5-inch high-density diskettes and an installation guide. The two diskettes contain identical information. The functions of the files on the diskette may be supplied as part of the system utilities for the host system in which the AHA-1740A/1742A/1744 is installed. The configuration diskette contains the following files:

- *!adp0000.cfg* - Configuration file for the AHA-1740 (older version of the AHA-1740A)
- *!adp0400.cfg* - Configuration file for the AHA-1744
- *!adp0001.cfg* - AHA-1740A/1742A with floppy disabled
- *!adp0002.cfg* - AHA-1742 with floppy enabled
- *!adp0100.cfg* - AHA-1540B/1542B configuration file
- *!adp0000.ovl* - Configuration overlay file for SCSI bus parameters
- *adl.exe* - Microcode download utility, including low-level format utility
- *standard.hex* - Current production release of Standard Mode microcode (AHA-1740/1744 only)
- *enhanced.hex* - Current production release of Enhanced Mode microcode (AHA-1740/1744 only)

Earlier versions of ASW-C174 may not contain all features listed. Operation of the utilities is described in Chapter Three, *Installation* and Chapter Ten, *Problem Determination*. If the board has no ASW-C174 accompanying it, or the utility is incomplete and the system utilities do not include the function needed, either contact the board vendor for a copy or query the Adaptec bulletin board for a download copy of the files.

> Note
> The Adaptec bulletin board number is (408) 945-7727. Use 8 data bits, 1 stop bit, no parity, 1200, 2400, or 9600 baud.

The utility disk will also include copies of the microcode files for the AHA-1740/1744 to be downloaded by the download utility. These are normally not required, except in the case of microcode upgrade. The AHA-1740A/1742A do not have downloadable microcode.

The configuration overlay file uses a freeform data area. This freeform data area is used to configure the SCSI bus and the specific structure within the freeform data area and is not specified by the EISA specification. Adaptec uses a data structure for each device (SCSI ID #n) consisting of two bytes, shown in the following table:

Byte 2n+1	Description	Byte 2n	Description
bits 7-3	Reserved	bit 7	Reserved
bits 2-0	Maximum sync Xfer rate	bit 6	More than 1 LUN supported
000	10.0 MBytes/second	bit 5	Parity check enable
001	6.67 MBytes/second	bit 4	Send start command
010	5.0 MBytes/second	bit 3	Sync negotiation enabled
011	4.0 MBytes/second	bit 2	Disconnection enabled
100	3.33 MBytes/second	bit 1	Ignore error if device not present
101-111	Reserved	bit 0	Enable disk BIOS support

If your EISA system (and ECU) do not support the freeform data area, the AHA-1740A/1742A/1744 can still be used, but only at the default settings for the SCSI bus as shown in Chapter Three, *Figure 3-5, Standard Mode SCSI Configuration Screen*, and *Figure 3-6, Enhanced Mode SCSI Configuration Screen.*

❑

Chapter Three

Installation

Unpacking and Inspection

The carrier is responsible for damage incurred during shipment. In case of damage, have the carrier note the damage on both the delivery receipt and the freight bill, then notify your freight company representative so that the necessary insurance claims can be initiated.

After opening the shipping container, use the packing slip to verify receipt of the individual items listed on the slip. Retain the shipping container and packing material for later use should return of the equipment to the factory be necessary.

> CAUTION
> The AHA-1740A/1742A/1744 is carefully designed to resist the effects of static electricity. However, like all electronic equipment, it can be damaged or its life can be shortened by unusual static discharges. Please take the proper precautions when handling the board. Keep the board in its conductive wrapping until it is ready to be installed in your system. Be sure that the host computer and the personnel handling the board are properly grounded while installing the board.

Installation

The following section details the installation procedure for the Adaptec AHA-1740A/1742A/1744 EISA-to-SCSI host adapter. The installation of the board consists of unpacking the board, preparing the SCSI devices, installing the correct terminations, inserting the board into a full-length EISA-compatible connector, and connecting a SCSI cable from the onboard connector to a SCSI target. The system is then powered up, the microcode downloaded and the board configured for operation.

The Adaptec AHA-1740A/1742A/1744 EISA-to-Fast SCSI host adapter has been designed to operate as shipped in standard EISA class computers. The board (or the system in which it is installed) is normally shipped with a configuration diskette which permits the board to be configured to the actual slot location in which it is installed. Unlike AT/ISA boards, but like Micro Channel boards, EISA boards do not normally require hardware jumpers.

Ensure that you have the correct version of the AHA-1740A/1742A/1744 for your system. The AHA-1740A/1742A support the more common single-ended SCSI interface. The AHA-1744 supports the differential interface, more common on SCSI peripherals on minicomputers. While the two use the same signal protocol, they are *not electrically compatible.*

> WARNING
> Connection of a single-ended board to a differential drive or vice versa may cause permanent electrical damage to one or both devices.

System Configuration Background for Standard Mode

The DOS operating system and standard BIOS supports two hard disk drives; drive *C* and drive *D*. If two standard hard disk drives are installed, they are the only hard disk drives accessible from the operating system. If one standard hard disk drive is installed, the AHA-1740A/1742A/1744 BIOS allows DOS to access the SCSI drive with the Target:LUN address of 0:0 as the second of the two supported drives (drive *D*). If no standard hard disk drives are installed, the AHA-1740A/1742A/1744 BIOS allows DOS to access the SCSI drive with the address of 0:0 as the first of two supported drives (drive *C*) and the SCSI drive with the address of 1:0 as the second drive (drive *D*).

System booting is performed from the floppy drive if a floppy diskette is installed. If no floppy is installed, system booting is attempted from the drive chosen as drive *C* through the above process, whether the drive is a standard hard disk or a SCSI hard disk. The AHA-1740A/1742A/1744 BIOS fully supports the extended partitioning capabilities of DOS for up to two drives. Adaptec supplies a range of products based on the Advanced SCSI Programming Interface (ASPI) architecture that allow the support of more than two physical or logical devices under DOS. Many other operating systems, including SCO Xenix and Unix, also have this feature and will allow the access of any number of attached SCSI devices. Refer to Chapter Eight, *Device Drivers* for more details. Peripheral devices such as SCSI tape, DAT, CD-ROM and others require device driver software to be installed.

Standard hard disk refers to the disks attached to the system by a standard ISA non-SCSI disk controller. These standard hard disks can be set to the installed or not installed state by the Setup program that is supplied with each host computer. The Setup program allows the user to select the number of standard hard disks that are recognized by the system regardless of whether they are physically installed.

Preparation

Few preparatory steps need to be taken to install the host adapter in the host computer. The floppy controller enable/disable jumper on the AHA-1742A is the only configuration jumper. If you already have a floppy controller in your EISA system, disable the floppy controller on the AHA-1742A by removing the right-most jumper on jumper block J6.

SCSI bus terminators must be installed in the correct SCSI devices and the correct SCSI addresses must be assigned to each peripheral device. Each board is shipped (default) with termination resistors installed. Unless connecting both internal and external peripherals to the same board, there is no need to remove the terminating resistors from the AHA-1740A/1742A/1744.

Each EISA system is shipped with a configuration utility to assign parameters such as port addresses and interrupt priorities to boards installed in the system. This must be used to identify and configure the board in your system. The details vary from vendor to vendor. Refer to the system documentation for details.

The Adaptec AHA-1740A/1742A/1744 32-bit EISA bus-to-SCSI bus host adapter has been designed to operate as shipped in the majority of EISA class computers. A board direct from the factory is normally shipped with the ASW-C174 Configuration Utility. This utility permits parameters associated with the board and the SCSI bus to be set up through the system keyboard and CRT.

Termination

The SCSI bus must be terminated correctly to assure proper operation. The first and last physical SCSI devices on the SCSI cable must have terminators installed. All other SCSI devices must have terminators removed. The host adapter is shipped with terminators which are three Serial In-line Packages (SIPs) located near the 50-pin internal SCSI flat ribbon connector at locations RN3, RN4, and RN5. The internal and external connectors connect to the same SCSI bus, so both internal and external cabling must be considered in determining where terminators are installed.

If only one cable (either internal or external) is connected to the host adapter, the terminators must remain installed in the host adapter. Terminators must also be installed on the device at the farthest end of the cable from the host adapter. Terminators must be removed from all other attached SCSI devices.

If both an internal and external cable are connected to the host adapter, remove the terminators on the host adapter and install terminators on the devices at the farthest end of each cable. Terminators must be removed from all devices except the device at the end of each cable. The instruction manuals for each SCSI device will indicate how the terminators can be removed or replaced.

SCSI Addressing (ID)

The SCSI target address for each SCSI device to be attached must be selected by setting the proper jumpers or switches on the device in Standard Mode. The SCSI device that is to be used as the boot disk must have a SCSI address of zero. In Enhanced Mode, you can boot to any SCSI ID. Refer to the section titled *Enhanced Mode SCSI Configuration* for further details.

SCSI Addresses 0 and 1 should be reserved for SCSI hard disk drives. Each installed peripheral must have a different SCSI address. The host adapter's default SCSI ID is 7. Duplicate SCSI addresses will cause errors that are extremely difficult to identify.

Any jumpers that control operating modes must also be properly set. If there is a jumper that enables synchronous transfer and/or synchronous negotiation, the jumper should be set to enable synchronous.

SCSI Parity

Check all SCSI devices to ensure that they generate parity. If any SCSI device does not generate parity, then *all* SCSI devices should be set to disable parity checking. If all SCSI devices generate parity, it is recommended that parity checking be turned on for all devices. Please note that generating parity and checking parity are two separate functions. The AHA-1740A/1742A/1744 configuration overlay can be used to enable/disable parity checking for each SCSI ID.

Hardware Installation

The Adaptec AHA-1740A/1742A/1744 EISA-to-Fast SCSI host adapter has been designed to operate as shipped in standard EISA class computers. The board (or the system in which it is installed) is normally shipped with a configuration disk which permits the board to be configured to the actual slot location in which it is installed. Unlike AT/ISA boards, but like Micro Channel boards, EISA boards do not normally require hardware jumpers. An exception is configuration of the floppy disk controller on the AHA-1742A (a description follows).

Ensure that you have the correct version of the AHA-1740/1744 for your system. The AHA-1740A/1742A supports the more common single-ended SCSI interface. The AHA-1744 supports the differential interface, more common on SCSI peripherals for minicomputers. While the two use the same signal protocol, they are *not electrically compatible.*

> **WARNING**
> The AHA-1740/1740A/1742A require single-ended devices. The AHA-1744 requires differential devices. Failure to match drive types can result in electrical damage to the board and the peripherals.

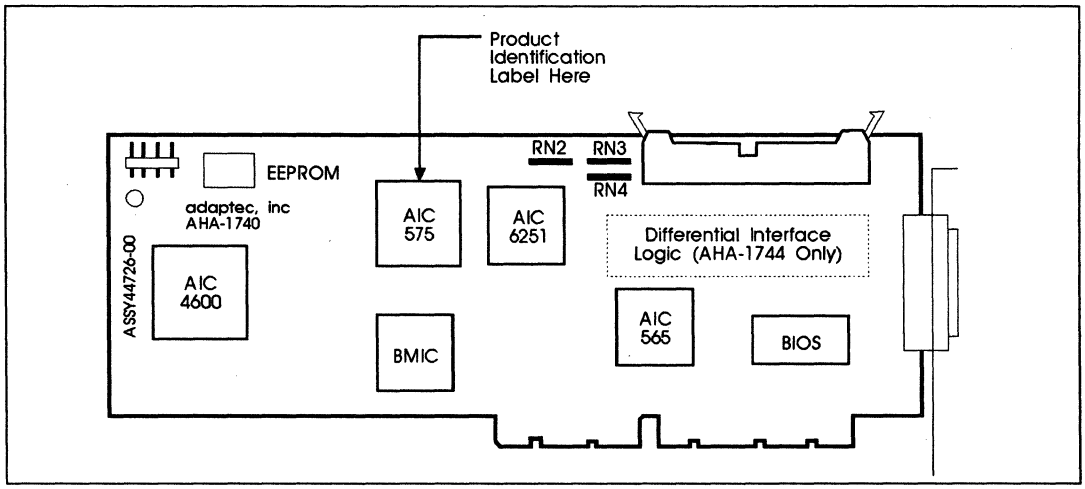

Figure 3-1. AHA-1740/1744 Board Layout

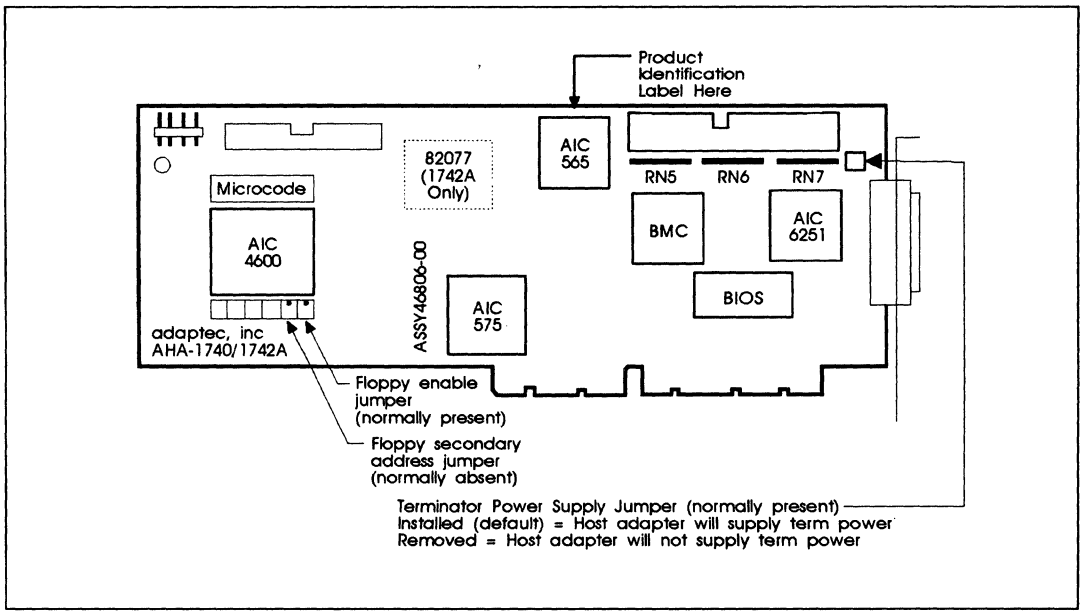

Figure 3-2. AHA-1740A/1742A Board Layout

To perform hardware installation:

1. Turn off the power to the computer system.

2. Remove the cover of your EISA personal computer to expose the EISA bus slots on the motherboard.

3. Locate an unused EISA slot in your system which supports bus master operations. Refer to the host system documentation for details.

4. Remove the corresponding system expansion slot cover by turning the screw that secures it from the top, counterclockwise.

5. Examine the board to be installed. If it is an AHA-1742A, and your system already has a floppy disk controller, disable the floppy disk controller on the AHA-1742A by removing the rightmost jumper from jumper block J6 in the lower left corner of the board.

6. If both internal and external devices are to be connected, remove the three terminator resistor packages near the internal connector. Only the two devices at either end of a SCSI cable should have terminators installed. On the AHA-1740 and AHA-1744, these are RN2, RN3, and RN4, located to the side of the internal SCSI connector. On the AHA-1740A and AHA-1742A, these are RN5, RN6, and RN7, located below the internal SCSI connector.

7. Align the EISA bus connector on the bottom of the AHA-1740A/1742A/1744 to the open chassis slot with the slot cover removed. Ensure the external connector and bracket pass cleanly through the cutout in the rear wall.

8. Firmly plug the board into the slot. Use the screw from the corresponding expansion slot cover to secure the board bracket to the system frame.

9. If an internal SCSI peripheral is to be used, install a 50-pin SCSI ribbon cable to the host adapter. This cable must be oriented correctly. Pin 1 of the SCSI cable is designated by a red stripe. Multicolor 50-pin ribbon cables signify pin 1 with a brown color. Most cables and the corresponding sockets are keyed to ensure correct orientation. Pin 1 on the host adapter 50-pin SCSI header is located on the lefthand side, farthest from the installation bracket. After locating pin 1 on the host adapter and on the SCSI cable, carefully insert the connector located at the end of the long end of the cable into the host adapter connector. On the AHA-1740A/1742A/1744, firmly seat the connector to the board such that the locking ears snap into place to hold the cable firmly. If it is ever necessary to remove the cable, gently push the two locking ears horizontally outwards along the axis of the board until the cable connector is pushed upward and free.

10. If an internal SCSI device is also being installed, it should be installed in the drive bays in accordance with the directions on the peripheral at this time. The proper power supply connection also must be made to the SCSI peripheral device.

11. The 50-pin SCSI ribbon cable can now be attached to each internal SCSI device. Refer to the device's installation instructions to ensure proper pin 1 orientation. Pin 1 orientation must be consistent throughout the system. Keep the ribbon cable neatly dressed away from the ventilation slots in the computer system. Keep the ribbon cable dressed away from possible electrical noise sources or noise sensitive components, particularly large microprocessors, memory boards, switching power supplies, and analog data acquisition boards. If the internal configuration requires the cable to come near noise sensitive circuits, make sure that the cable crosses the boards at right angles and is near the noise sensitive circuits for the shortest distance possible.

12. Carefully reinstall the cover of the computer.

13. If an external SCSI subsystem is being installed, it can now be cabled to the External SCSI Connector projecting from the shielding bracket on the back of the AHA-1740A/1742A/1744 host adapter. The external connector on the AHA-1740A/1742A/1744 is a small form factor SCSI alternate-2 D shell connector that ensures correct pin 1 orientation on the host adapter. The correct shielded SCSI cable must be used for proper operation. Ensure that the external device drive types all correspond with the single-ended/differential marking on the bracket of the AHA-1740A/1742A/1744 respectively.

    Note that a cable with the appropriate connector at each end is all that is required to connect a SCSI alternate-2 D-shell with a Centronics-type or vice versa. There is no electrical or signal difference although the connectors are different sizes.

    The subsystem, cables, and SCSI terminators must be installed in accordance with the directions provided with the external SCSI subsystem. The addresses

selected for external SCSI devices must not overlap with the addresses of the host adapter or any other SCSI devices attached internally.

Generally speaking, there can be no more than seven other SCSI devices attached, each with its own unique address and the total cable length must not exceed 20 feet for single-ended and 80 feet for differential.

Checklist

Before applying power to your system, the following items should be completed and checked:

- The 50-pin SCSI ribbon cable is connected to the host adapter with proper pin 1 orientation.
- The host adapter is firmly seated in the host computer's adapter slot.
- The correct SCSI addresses are selected on all attached SCSI devices. Address 0 is reserved for the boot hard disk and address 1 is used for a second hard disk.
- The correct operating modes are selected on all attached SCSI devices.
- Terminators are installed or removed on the drives and host adapter as required.
- External SCSI devices are properly installed and cabled.

Terminators

The SCSI bus must also be terminated correctly to ensure proper operation. The first and last physical SCSI devices on the SCSI cable must have terminators installed. All other SCSI devices must have terminators removed. The AHA-1740A/1742A/1744 host adapter is usually the first device on the SCSI Bus and has terminators installed at the factory.

System Configuration

When it is being installed in an EISA system, the AHA-1740A/1742A/1744 requires an EISA system configuration file. This may be part of the system software or may be supplied on a separate diskette. If it is separate, installation is easier if the contents of the separate diskette are copied onto the main bootable system configuration disk.

To perform system configuration:

1. Place the bootable configuration diskette in an operative drive and reset the system to boot from this diskette. This configuration diskette is normally supplied by the EISA system vendor.

2. Ignore any error which indicates that an unknown board has been detected in the system. Selection of board configuration varies with the configuration utility supplied with the EISA system. There are two main types, supplied by MCS and Phoenix. The type may be obscured by the screen banner used by the system vendor. Follow the procedure which is closest to your environment. In the case of the MCS configuration, type **cf**. For Phoenix configuration type **ptlecu**. Select board configuration and press the **Enter** key.

3. If the main configuration disk does not contain files for the AHA-1740A/1742A/1744, copy the contents of the ASW-C174 diskette with the AHA-1740A/1742A/1744 configuration files to the boot floppy and run the configuration program.

   !adp0000.cfg for the AHA-1740
   !adp0001.cfg for the AHA-1740A
   !adp0002.cfg for the AHA-1742A
   !adp0400.cfg for the AHA-1744

   In addition, run *adp0000.ovl* for all boards. The configuration utility will usually allow selection among a number of options, including copying new configuration files. Select this last option to install the appropriate files from the ASW-C174 floppy disk. To select the configuration utility on a system already running, insert the system configuration disk, select that drive and enter **cf** or **ptlecu** (see above).

The program will autoconfigure the system and display a diagram of the motherboard showing which boards have been configured into which slots.

MCS Configuration

For configuration under MCS, select the slot in which the AHA-1740A/1742A/1744 is installed and press **Enter**. The screen will display the System Configuration Detailed View. These settings should normally not be changed for Standard Mode operation. Use the cursor arrows to make selections and the **Enter** key to enter the selection. When installing multiple boards in Standard Mode, ensure that none share the same configuration parameters for port address. The configuration utility normally automatically ensures that there is no conflict. SCSI ID can be the same provided that the boards do not share the same SCSI bus. Normally, the host adapter is given address 7. A typical selection detailed view is shown in Figure 3-3. Use the arrow keys to move around in a selection and the **Enter** or **Return** key to choose a highlighted selection. If a mouse is installed, it may also be used.

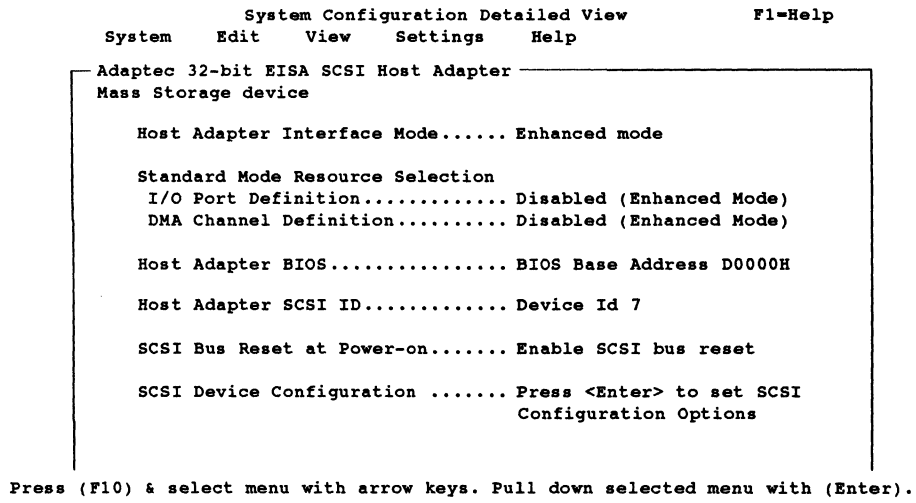

Figure 3-3. System Configuration Detailed View Screen

Normally, it is not necessary to alter any settings for configuration. Selection of the appropriate interrupt request will also select between Standard and Enhanced Mode. If selecting Enhanced Mode, it is not necessary to alter the system resource selection, but if resources are left selected, they will be allocated, even if not used.

Select the AHA-1740A/1742A/1744 installation configuration as follows:

1. Select the host adapter interface mode. There are two available. Standard Mode allows software written for the AHA-1540 or AHA-1640 families to run the AHA-1740 Family. Enhanced Mode allows a higher-performance interface to be used.

   When Standard Mode is selected, the host adapter interrupt level can be selected by pressing **Enter** when the **Host Adapter Interface Mode** is highlighted.

When Enhanced Mode is selected, IRQ 11 is used by default. By default, if multiple AHA-1740 family host adapters are in the system in Enhanced Mode, all will use IRQ 11. For the MCS EISA Configuration Utility, this can be shown by selecting **Change System Resources** under the Edit pull down menu (or entering **Ctrl-R**) when the **Host Adapter Interface Mode** is highlighted. To increase system performance, select a different IRQ for every AHA-1740 family host adapter in the system.

> Note
> The IRQ cannot be shared with ISA mode SCSI host adapters such as the AHA-1540 and AHA-1520 series adapters. If those host adapters are in the system, they must be assigned unique IRQs.

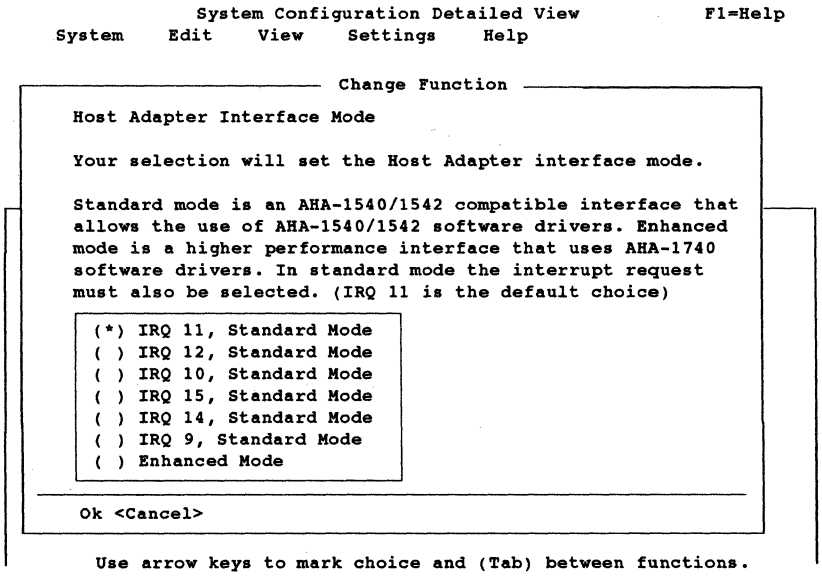

Figure 3-4 Interface Mode & Interrupt Selection Screen

2. If Standard Mode is selected, choose both the host adapter port address and DMA channel. For Enhanced Mode, both should be disabled. Booting is supported from any port address.

3. Select the base address of the bootstrap BIOS on the host adapter.

4. Select the device address for the host adapter on the SCSI bus.

5. Select whether the host adapter generates a reset on the SCSI bus at power-on or reset.

6. If required, select the device configuration to select parameters on the SCSI bus. A pop-up window appears. Select the host adapter interface mode chosen in Step 1.

Standard Mode SCSI Configuration

The view for Standard Mode is a simple selection for those variables which apply to all SCSI peripherals connected. This is shown in Figure 3-5. Normally, the default of one device at SCSI ID 0 with normal default parameters is selected.

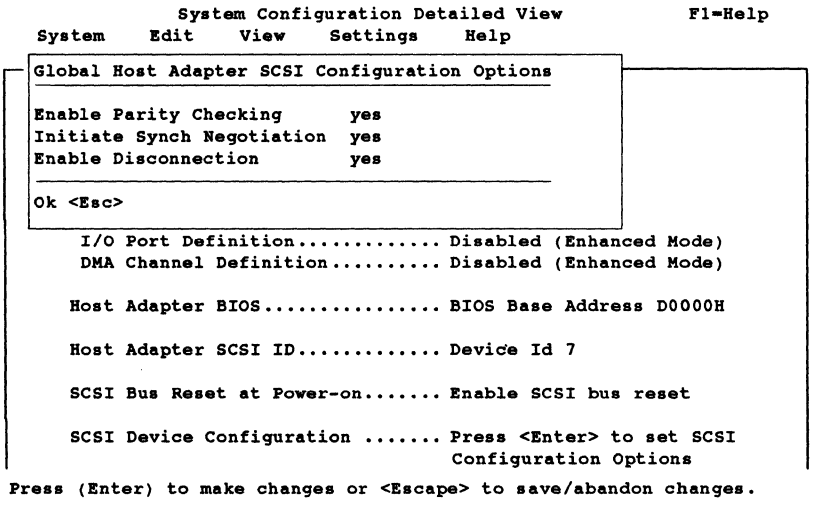

Figure 3-5. Standard Mode SCSI Configuration Screen

Select **Enable Parity Checking** to allow the host adapter to generate parity on data sent and check parity on data received on the SCSI bus.

Select **Initiate Synch Negotiation** to allow the host adapter to attempt to use the faster synchronous protocol for data transfers on the SCSI bus. The host adapter will negotiate for a data transfer rate of 5 MBytes/second and an offset of 7. If deselected, the transfers will use the asynchronous protocol, unless the SCSI drive itself requests synchronous negotiation. If the SCSI drive negotiates for synchronous transfers, the host adapter will respond with a 5 MBytes/second data transfer rate and offset of 7, or the data transfer rate and offset suggested by the peripheral device, whichever is lower.

Select **Enable Disconnection** to allow a peripheral to go off-line while it completes a lengthy operation like a seek. This allows the host adapter to perform other operations on the SCSI bus while the device is temporarily disconnected.

Enhanced Mode SCSI Configuration

The view for Enhanced Mode allows more flexible selection and is shown in Figure 3-6.

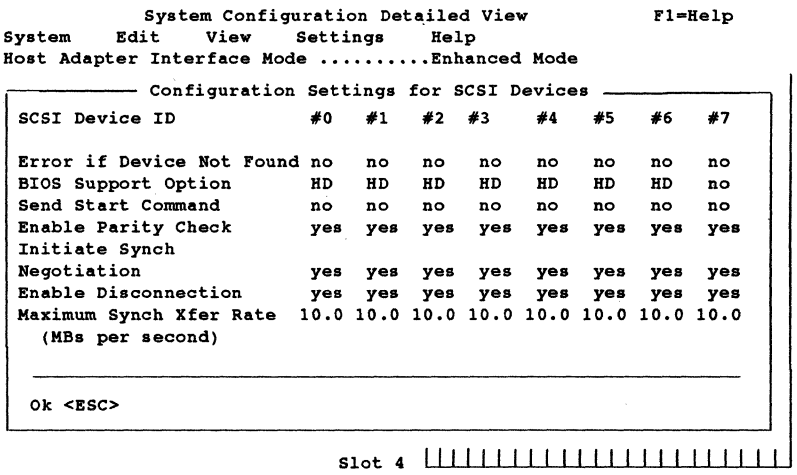

Figure 3-6. Enhanced Mode SCSI Configuration Screen

The enhanced mode offers a greater selection of SCSI configuration options. Use the **Tab** or **Cursor** keys or a mouse to highlight a particular selection and press **Enter** to toggle between no and yes. Each device can have a number of parameters selected individually.

Error if Device Not Found selects whether the operator will be notified if the BIOS is unable to find the device during the boot procedure.

BIOS Support Option allows up to two devices attached to the SCSI bus to be recognized by the host adapter BIOS and installed as devices on the system without the need for driver software. Only fixed and removable hard disks are supported under the BIOS, with default for hard disks only. Select this option to allow removable support or to remove any disk support for each SCSI address. Note that support for removable disks does not allow the disk media to be removed during operation only use of a removable disk as if it were a fixed disk.

When this option is selected, use the cursor keys to move among the options shown in Figure 3-7.

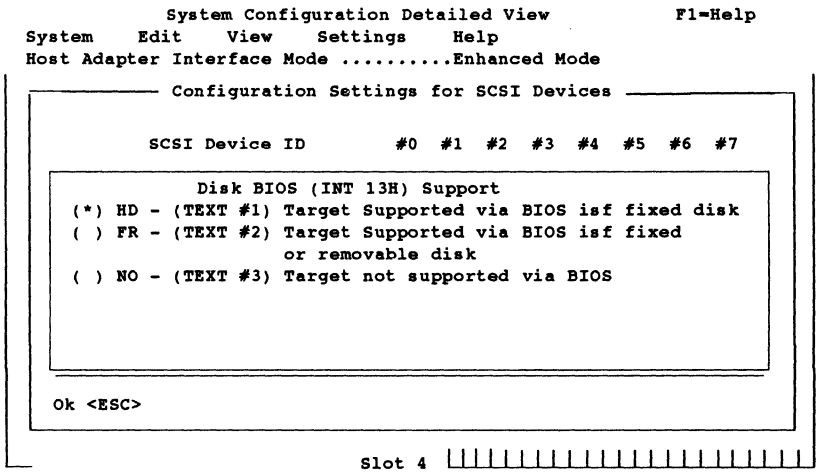

Figure 3-7. BIOS Support Selection Screen

Send Start Command is used for devices which require a command to start up after power on. Most devices do not require this.

Enable Parity Check is similar to Standard Mode where the host adapter will generate and check for parity on SCSI bus data.

Initiate Synch Negotiation is similar to Standard Mode and allows the host adapter to attempt to communicate with the device using the faster synchronous SCSI protocol. Most disk drives support synchronous protocol.

Enable Disconnection is similar to Standard Mode. It allows the device to go offline while performing an operation, freeing up the SCSI bus and host adapter for other operations in parallel.

Maximum Synch Transfer Rate allows selection of the highest data transfer speed that the host adapter will attempt with that peripheral. The AHA-1740A/1742A/1744 support rates up to the Fast SCSI maximum of 10 MBytes/second.

When the selection is completed, press **Esc** to reach the SCSI configuration exit menu shown in Figure 3-8.

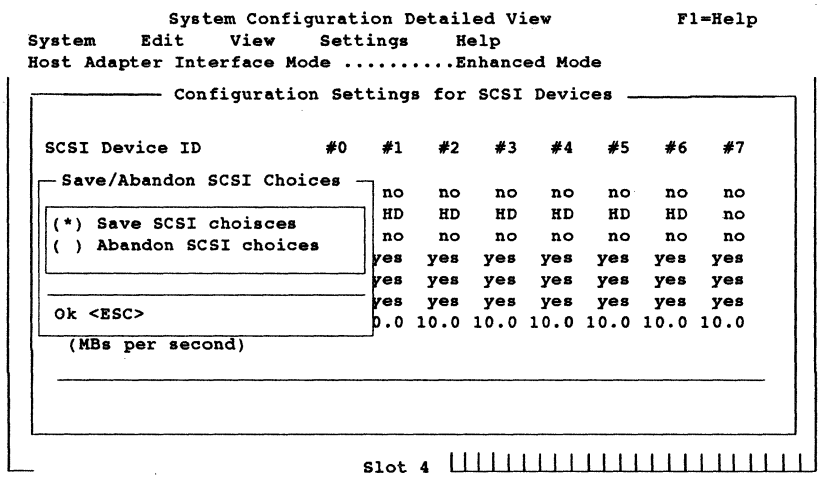

Figure 3-8. Enhanced Mode Configuration Exit Screen

Use the cursor keys or mouse to select whether to make the changes or abandon all changes made on this attempt. When the correct line is highlighted, press **Esc** to select.

Exit the configuration utility by pressing **Ctrl + x**

Select the **Save Configuration and Exit** option using the cursor arrows and press the **Enter** key.

Reboot from the original boot diskette.

Multiple Adapters Sharing Same SCSI Bus

Installation of multiple 1740A/1742A/1744s in an EISA system is common and presents no problems. When two or more 1740A/1742A/1744s in Enhanced Mode are installed in a system sharing the same SCSI bus, they must manually be set to different interrupts using the system configuration utility. In the MCS EISA Configuration Utility, press **Ctrl-R** to view and edit the choices of available interrupts. The default is Int 11. When multiple 1740A/1742A/1744s are not attached to the same SCSI bus, then sharing of interrupts in Enhanced Mode is acceptable.

Phoenix Configuration

Configuration using the Phoenix utility is similar to that under MCS. Use the arrow keys to select the board to configure after entering the Configuration menu, selecting function choices and pressing **Enter**. Press **Enter** when the appropriate board slot is highlighted.

Selection among the available system options is made by using the up/down arrows. Press the **Spacebar** at the option to allow for a toggling among options available. There is no facility for selection of peripheral options under Phoenix. To exit, skip to the bottom of the page and press **Enter** when **OK** is highlighted.

Floppy Disk Configuration

The AHA-1742A is normally shipped with its floppy disk controller enabled. This may be disabled to prevent conflict with an existing floppy disk controller already in the system by removing the rightmost jumper from J6 on the lower left of the board. If the jumper is removed, the board will return the identity of an AHA-1740A to any software inquiry command. This allows software to use the appropriate configuration file for the main part of the board, as described previously.

The floppy disk can reside at one of two address blocks. Normally, it uses addresses 3F0h-3F6h as the primary address. A secondary address of 370h-376h can be selected by placing a jumper on block J6 in the second position from the right, next to the floppy enable jumper described above.

ADL Utility

The microcode with which the AHA-1740/1744 is equipped has two components.

- Standard Mode (*standard.hex*)
- Enhanced Mode (*enhanced.hex*)

Both are permanently stored on the AHA-1740A/1742A/1744 simultaneously. Selection between these modes affects the software manager required to support the board. It has no effect on the SCSI or host bus hardware. The firmware download can either be used to configure the board for one of the two main modes, or to upgrade the board to a later revision of firmware for a particular mode (AHA-1740/1744 only).

The Standard Mode allows software drivers written for the AHA-1540 or AHA-1640 families to run unaltered on the AHA-1740 family. There is no performance penalty for this on the EISA bus. The AHA-1740 performs 32-bit transfers at speeds up to 33 MBytes/second.

The Enhanced Mode allows the board to take advantage of a number of features which were not available on earlier host adapters. These include:

- 32-bit addresssing capability
- Single fast mailbox handling
- Contingent allegiance (SCSI)
- Tagged queueing (SCSI)
- 10 MBytes/second Fast SCSI data transfer

Adaptec's AHA-1740/1744 *adl* utility is used for three main features:

- Download firmware (AHA-1740/1744 only)
- Firmware information
- Low-level disk format

ADL Operation

Insert the ASW-C174 configuration diskette into drive *A*. Change to the *download* directory on the diskette by entering:

```
a:\cd download
```

At the DOS prompt, enter **adl** to bring up Adaptec's AHA-1740/1744 *download* utility. The following will describe the procedures and the screen display. During the operation, **F1** can be pressed to display help messages and **Esc** to exit the current message box and the utility. If using a monochrome or gray-scale monitor, enter **adl -m** to improve viewing contrast.

List of Adapters

When the utility is first loaded, a list of installed host adapter(s) is displayed at the upper left corner of the screen. Along with each installed host adapter is its configured mode. (Note that the user must run the *System Configuration* utility in order to change the mode in which the host adapter is selected to operate). If more than one host adapter is installed, use the up and down arrow key to choose the host adapter. When the host adapter to be selected is highlighted, press **Enter** to select.

The **Esc** key can be used to exit the utility. When using other parts of the utility, return to this screen to exit. If either the *Download Firmware* or *Low-level Format* utility has been used, the system will reboot automatically to allow correct configuration.

Main Menu

After selecting the host adapter, a main menu will appear. The following three options are provided:

- Download Firmware
- Firmware Information
- Low-Level Format

Use the up and down arrow key to choose the operation. Press **Enter** to start an operation. Following is a description of each operation.

Download Firmware (AHA-1740/1744 Only)

The AHA-1740/1744 (not the AHA-1740A or AHA-1742A) have the unique flexibility of allowing firmware to be altered or upgraded while the board is installed in a system. This is done by using a utility on the ASW-C174 and either the firmware files supplied or new files supplied with ASW-M174.

> Note
> It is not necessary to perform a download when installing a system for the first time or when switching between Standard and Enhanced Modes.

Firmware download causes the host adapter to overwrite its program memory with microcode supplied by the user from an external source like the ASW-C174 or ASW-M174. After the data is written to the host adapter's internal RAM, and a successful checksum test done by the host adapter, the host adapter will then reprogram its EEPROM with the new firmware. In order to change the host adapter current interface mode, you must reconfigure the system memory by running the EISA Configuration Utility (ECU) that was supplied with your EISA system.

To download firmware to the 1740/1744, select **Download Firmware**. Have the new firmware ready on a floppy diskette or copy it onto the internal hard disk drive. New firmware on the ASW-M174 will come with its checksum value on the floppy diskette label. Firmware on the ASW-C174 will correspond to major revisions of the AHA-1740A/1742A/1744 product. If using an older version of either software, it is unlikely that the firmware that it contains will be a current revision.

First, an edit form will pop up when this operation is chosen. Use the arrow keys to move from field to field, or within the field. Enter the firmware file name (e.g., *a:\standard1.hex*) that is going to load into the host memory, and choose the mode (Standard or Enhanced) that is going to download by toggling with the **+/-** key. Press **Esc** to exit the form and continue.

After exiting from this screen the new firmware file will be automatically loaded into the host memory. The checksum will be calculated and displayed if the firmware file is loaded successfully. At this point, verify the displayed checksum with the checksum on the floppy label. Press **Esc** to cancel the operation. Press **Y** to continue. This will issue the Download Firmware command to the host adapter. The whole process may take up to 45 seconds. A message will indicate the success or failure of downloading the new firmware.

Subsequently, a confirm message window will be displayed to allow verification of the download operation. If the displayed information is valid, press **Esc** to continue and return to the main menu.

Firmware Information (AHA-1740/1744/1740A/1742A)

For any of the AHA-1740/1744/1740A/1742A boards, this menu selection is an easy way to check the versions of microcode currently installed.

Firmware Information is used to obtain release information and revision level of the host adapter's firmware. Use this selection to ensure that proper firmware is installed or to confirm the mode in which the board is currently operating.

This operation queries the board for the release, revision, and checksum information of microcode currently on the host adapter. If the command is successfully completed, all information that is retrieved from the host adapter will be displayed. Otherwise, an error message will be displayed. After reading the host adapter information, Press **Esc** to continue.

Have this information available when contacting Adaptec with questions about firmware or upgrades.

If multiple host adapters are installed, the **Esc** key can be used to select another host adapter from the List of Host Adapters menu.

Low-level Format

Low-level format is used to reformat a hard disk and erase all previous information stored on the disk. This is usually not necessary with SCSI disks as they are low-level formatted by their manufacturer with comprehensive surface scans and defect mapping. However, it is occasionally desirable to again low-level format a SCSI disk.

Choosing this option will display a list of device(s), which contains the list of all attached SCSI device(s) on the previously selected host adapter. Press **Esc** to return to the main menu or **Enter** to select the SCSI drive to be formatted. Note that the only devices currently supported are hard disks.

After choosing a SCSI device, a menu will be displayed to allow the user to choose either the Format and Verify option, or the Wipe Boot Sector option. Press **Enter** to select. A warning message will be displayed to alert the user that this particular operation will result in losing the data content that is stored on the drive. The user can either press **Y** to continue the operation or **Esc** to abort the operation.

Appropriate messages for successful or unsuccessful completion of the operation are displayed. Simply press **Esc** to continue and return to the main menu.

❑

Chapter Four

Hardware Functional Description

Hardware Overview

This section provides a description of the AHA-1740A/1742A/1744 hardware funtional interface to the EISA host software.

The hardware consists of:

- Custom SCSI protocol chip
- AIC-6251
- EISA Interface Controller
- Intel 82355
- FIFO buffer
- Set of I/O ports
- Controlling microprocessor
- AIC-565 Standard Mode control interface
- AIC-575 AHA-1740 mode interface

The DMA control logic in the 82355 controls the bus arbitration and data transfer handshaking. During DMA data transfers, the AHA-1740A/1742A/1744 becomes a bus master. The DMA logic supports odd- and even-byte and odd- and even-word starting addresses. For odd-byte starting addresses, the first transfer will be an 8-bit transfer, For odd-word starting address, the first transfer will be a 16-bit transfer.

The SCSI port is controlled by the AIC-6251, and Adaptec SCSI protocol device for fast (10.0 MBytes/second transfers) which supports arbitration, selection, and reselection with a minimum of processor intervention. This VLSI device also supports target mode (simultaneous to initiator mode) and synchronous SCSI transfers.

Standard Mode I/O Port Interface

The I/O port interface consists of three address locations. These three port addresses are decoded in the AT I/O address space. They form the primary communications channel between the host and the host adapter. The I/O ports are eight bits wide.

The base port is for control and status, the second port for command and data transfer, and the third port for interrupt flags.

I/O Port Interface Bit Definition

Port Address = Base + 0

WRITE: Control Register		READ: Status Register	
Bit 7	Hard Reset (HRST)	Bit 7	Self Test in Progress (STST)
Bit 6	Soft Reset	Bit 6	Internal Diagnostic Failure (DIAGF)
Bit 5	Interrupt Reset (IRST)	Bit 5	Mailbox Initialization Required (INIT)
Bit 4	SCSI Bus Reset (SCRST)	Bit 4	SCSI Host Adapter Idle (IDLE)
Bit 3	Reserved (0)	Bit 3	Command/Data Out Port Full (CDF)
Bit 2	Reserved (0)	Bit 2	Data In Port Full (DF)
Bit 1	Reserved (0)	Bit 1	Reserved (Undefined)
Bit 0	Reserved (0)	Bit 0	Invalid H A Command (INVDCMD)

Port Address = Base + 1

WRITE: Command/Data Out		READ: Data In	
Bit 7	Command/Data Out Bit 7	Bit 7	Data In Bit 7
Bit 6	Command/Data Out Bit 6	Bit 6	Data In Bit 6
Bit 5	Command/Data Out Bit 5	Bit 6	Data In Bit 6
Bit 4	Command/Data Out Bit 4	Bit 4	Data In Bit 4
Bit 3	Command/Data Out Bit 3	Bit 3	Data In Bit 3
Bit 2	Command/Data Out Bit 2	Bit 2	Data In Bit 2
Bit 1	Command/Data Out Bit 1	Bit 1	Data In Bit 1
Bit 0	Command/Data Out Bit 0	Bit 0	Data In Bit 0

Port Address = Base+ 2

WRITE: Reserved, do not write		READ: Interrupt Flags	
Bit 7		Bit 7	Any Interrupt
Bit 6		Bit 6	Reserved
Bit 5		Bit 5	Reserved
Bit 4		Bit 4	Reserved
Bit 3		Bit 3	SCSI Reset Detected (SCRD)
Bit 2		Bit 2	HA Command Complete (HACC)
Bit 1		Bit 1	MBO Available (MBOA)
Bit 0		Bit 0	MBI Full (MBIF)

Control and Status Port

Writing a one to the bits of the Control Port initiates certain special host adapter operations. There is no requirement to return the bits to the zero state, since they are reset automatically after the requested operation is initiated. Read operations to the Status Port address return host adapter status information.

Base+0 Port, Write: Host Adapter Control Port

Bit 7 - Hard Reset (HRST)
The setting of the Hard Reset bit to one forces the host adapter into a state identical to a normal power-on state. Diagnostic functions are executed and all status for ongoing SCSI operations is lost. A Reset Condition is generated on the SCSI bus. While the reset is being processed, the Self Testing in Progress bit (Host Adapter Status Port bit 7) is set. When the reset is complete, that bit is reset and the Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set, indicating that the AHA-1740A/1742A/1744 mailbox structure must be reinitialized and that no other operations are active on the host adapter. See the section on *Reset Functions* for a description of the overall reset structure.

Bit 6 - Soft Reset (SRST)
The Soft Reset bit clears all ongoing SCSI and host adapter commands. All Command Control Blocks are abandoned and all queued commands are abandoned. Mailbox In and Mailbox Out entries must be cleared by the host. No diagnostic functions are executed. No Reset Condition is generated on the SCSI bus. The Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set when the reset processing is completed. This indicates that the AHA-1740A/1742A/1744 mailbox structure must be reinitialized and that no other operations are active on the host adapter. See the section on *Reset Functions* for a description of the overall reset structure.

Bit 5 - Interrupt Reset (IRST)
The setting of this bit clears the interrupt port of all bits that have been set and resets the interrupt line. The host adapter manages the interrupt presentation to minimize the possibility of incorrectly resetting an interrupt. MBOA and MBIF interrupts are presented immediately unless an SCRD or HACC interrupt has not yet been cleared. An SCRD or HACC will only be presented after any interrupt bit has been cleared and DF is zero, indicating an operation is fully completed. The prompt resetting of MBOA and MBIF interrupts minimizes the chance of a reset of one also resetting the other. Host programs should, however, be aware that there is a small chance of falsely resetting a new MBIF reset while clearing an MBOA interrupt. This can be resolved by periodically scanning the MBIF entries when activity is expected on the host adapter or by not enabling the MBOA interrupt.

Bit 4 - SCSI Bus Reset (SCRST)
The setting of this bit causes a SCSI Bus Reset to be generated on the SCSI bus. The SCSI Bus Reset is triggered at the time the SCRST bit is set to one and raises the RST line on the SCSI Bus for the architected 25 microsecond period. The reset is managed as a SCSI Soft Reset and will allow partially completed operations to

continue after the reset occurs. See the section on *Reset Functions* describing the overall reset structure.

Bits 0-3 - Reserved
Reserved bits must be set to zero to avoid compatibility problems with future extensions of the control register.

Base+0 Port, Read: Host Adapter Status Port

Bit 7 - Self Testing in progress (STST)
This bit, when one, indicates that the host adapter is performing self-initialization and internal diagnostics. The bit is asserted after a power-on or hard reset (Control Port Bit 7 HRST = 1). When diagnostic operation is complete, the STST bit is set to zero and bit 5 or bit 6 is set to indicate the successful or unsuccessful completion of the diagnostics. If bit 7 remains on, it indicates that the initialization or diagnostic could not be completed. The error condition can be determined as described in Chapter Ten, *Problem Determination.* In most cases, bit 6 (DIAGF) will be set to indicate that an internal diagnostic failure occurred.

Bit 6 - Internal Diagnostic Failure (DIAGF)
This bit, when one, indicates that the self-testing process has completed and that an error was detected. The host adapter must be reset by setting the Hard Reset bit (bit 7 of the Control Port) to clear the error. If the AHA-1740A/1742A/1744 again detects an error, troubleshooting procedures must be performed to identify and correct the error condition. The diagnostic LED will usually present a flash code that indicates the nature of the failure. Chapter Ten, *Problem Determination* describes the corrective procedures.

Bit 5 - Mailbox Initialization Required (INIT)
This bit, when one, indicates that the self-testing process has completed successfully and that the AHA-1740A/1742A/1744 is ready for mailbox initialization to be performed. The base memory address of the mailbox area must be established by execution of the Mailbox Initialization command. After execution of the Mailbox Initialization command and any other desired initialization operations, the AHA-1740A/1742A/1744 is ready for full operation.

Bit 4 - SCSI Host Adapter Idle (IDLE)
This bit, when one, indicates that the host adapter is in the idle state. The host adapter has no outstanding adapter commands or SCSI commands. The host processor must wait for the idle state before executing any adapter command except the Start SCSI (02) and Enable Mailbox Out Interrupt (05) commands.

Bit 3 - Command/Data Out Port Full (CDF)
The host uses the CDF bit to synchronize command and data transfers to the host adapter. An adapter command byte or an outbound parameter byte can be placed in the Command/Data Out Port when the port is empty, indicated by the CDF bit being zero. When a byte is placed in the Command/Data Out Port, the CDF bit is set to one and remains one until the host adapter has obtained and processed the byte. When the CDF bit returns to zero, the next Command or parameter byte can be placed in the port.

Bit 2 - Data In Port Full (DF)
The host uses the DF bit to synchronize transfers of data from the host adapter to the host. When the DF bit is set to one, the host adapter has placed a byte in the Data In Port for the host to remove and process. When the host performs a read to the Data In Port address, the DF bit is set back to zero automatically and not set to one again until a new data byte has been placed in the Data In Port by the host adapter for the host.

Bit 1 - Reserved
This bit is zero.

Bit 0 - Invalid Host Adapter Command (INVDCMD)
The Invalid Host Adapter Command bit is set to one if an invalid command or parameter byte was received in the Command/Data Out Port. After sending a command byte or data byte, the host software determines that the next byte is ready to send by waiting for the CDF bit to be reset. If the command byte or parameter byte is not valid, the command sequence will instead be terminated by the host adapter. The host adapter always terminates a command by raising the Host Adapter Command Complete (HACC) interrupt. If the HACC interrupt is set to one and the INVDCMD bit is not set, the command terminated normally. If the INVDCMD bit is also set to one, the command or parameter bytes were determined to be invalid and the command terminated abnormally. The INVDCMD bit is only valid from the time the HACC interrupt is set until the HACC interrupt is reset. The bit's value is not predictable until a new HACC interrupt is set for a new adapter command.

Command/Data Out and Data In Port

The second I/O port address is used by the host to write adapter command bytes and accompanying parameter data bytes to the host adapter. It is also used by the host adapter to send parameters back to the host to be read. The Command/Data Out Port is used by the host to send host adapter initialization and management commands and parameters that cannot be sent by the standard mailbox protocol. Information requested by the adapter commands placed in the Command/Data Out Port is returned through the Data In Port. The host should understand the format and number of bytes to be transmitted for each command so that extra invalid bytes are not passed across the interface. Bytes in addition to those required by the particular command are likely to be interpreted as invalid, although they may instead cause the execution of valid commands that were not supposed to be performed.

The host should only write to the Command/Data Out Port when CDF is zero. This allows time for the host adapter to process a previously written command or parameter byte. CDF is automatically set to one when the host writes to the port and is reset to zero after the host adapter removes the byte from the port.

If an adapter command needs additional data bytes, the host waits until CDF is zero before writing the additional bytes to the Command/Data Out Port. Just as in the command transfer case, each parameter byte written will set the CDF. The host can write additional data bytes only after CDF is again zero. The HACC interrupt will indicate when the command has terminated, normally or abnormally. If INVDCMD is also set, the host adapter found either the command or data bytes to be invalid and

terminated abnormally. The use of CDF as a handshaking bit is required to prevent the transfer of invalid data.

If an adapter command requires data transfer from the host adapter, the host adapter will place the data bytes in the Data In Port and set the DF bit (Status Port bit 2) to indicate that the requested parameter is ready for the host to read. When the host reads the Data port, DF is automatically reset. The host should wait until DF is again set before attempting to transfer the next parameter byte. The use of the DF bit to control the handshaking process is required to prevent the transfer of invalid data. After the last data byte has been transferred, the HACC interrupt bit will be set indicating command completion. If the Adapter Command was invalid, the HACC interrupt will occur before all data bytes have been transmitted and the INVDCMD bit will be set.

Interrupt Flag Port

The Interrupt Flag Port contains bits that indicate the reason that an interrupt was provided to the host from the host adapter. The host adapter uses the interrupt to notify the host that the host adapter is ready for immediate service from the host. The Interrupt Flag Port is a read-only port. When an interrupt bit is set by the host adapter to indicate that the host should respond, the Any Interrupt bit and the interrupt line are both also set. When the host begins to examine the returned registers and mailboxes to determine the cause of the interrupt and to perform the operations needed to service the interrupt, the host will first read the Interrupt Flag Port to record which interrupts must be serviced. The host will then clear the interrupts by setting the IRST bit (Host Adapter Control Port bit 5). The host adapter presents MBOA and MBIF interrupts immediately unless there is already an SCRD or HACC interrupt present. If the SCRD or HACC is present, the MBOA and/or MBIF interrupt will be posted after the SCRD or HACC interrupt is cleared. An SCRD or HACC interrupt will only be presented if the Any Interrupt signal is zero and the DF signal is zero, indicating the completion of all pending interrupt presentation. It is recommended that the MBOA interrupt be enabled only when required by the host. This prevents the possible presentation and resetting of MBIF interrupts before they are processed. Other reset operations will also reset the Interrupt Flag Port and the interrupt line, including the Hard Reset bit (HRST), the Soft Reset bit (SRST), and the power-on reset issued by the motherboard.

Base+2 Port, Read only: Interrupt Flag Port

Bit 7 - Any Interrupt
This bit, when one, indicates that the interrupt to the host has been established. The interrupting condition is identified in bits 0 to 3.

Bit 6 - Reserved
Returned as zero.

Bit 5 - Reserved
Returned as zero.

Bit 4 - Reserved
Returned as zero.

Bit 3 - SCSI Reset Detected (SCRD)
This bit, when one, indicates that a SCSI Reset has been received on the SCSI bus. The Any Interrupt bit and the AT interrupt signal will also be set. The host adapter supports SCSI Soft Reset (see Section 4.3). Any ongoing target or initiator activities will continue normally after first clearing the SCSI bus. In some rare cases, host intervention will be required to restart a SCSI command that was aborted by the reset operation. The host can convert the SCSI Soft Reset to a SCSI Hard Reset by setting the Control Register Soft Reset (Bit 6) to one, clearing all ongoing operations in the host adapter. In this case, the host must recognize that any operations not yet completed will never be completed and must perform appropriate error recovery operations. See the section on *Reset Functions* describing the overall reset protocol. The SCRD bit is not set for host-initiated SCSI Reset conditions caused by the setting of the HRST bit or the SCRST bit, since the host is already aware of the actions it has requested. If the Any Interrupt signal or DF signal is present, the SCRD interrupt will not be presented until the interrupts already present are cleared.

Bit 2 - Host Adapter Command Complete (HACC)
This bit, when one, indicates that an adapter command has been completed, normally or abnormally. The Any Interrupt bit and the AT interrupt signal will also be set. If the command was completed normally, only the HACC bit will be on. If the command was completed abnormally or was aborted before it was completed, the HACC bit will be one and the Invalid Command Bit (Status Register bit 5) will also be one. During parameter transfers to or from the host adapter, the HACC bit should be examined to verify that the command is still being processed and has not been ended abnormally. If the Any Interrupt signal or DF signal is set, the HACC interrupt will not be presented until the interrupts already presented are cleared.

Bit 1 - Mailbox Out Available (MBOA)
This bit, when one, indicates that an outbound mailbox entry is now available for use by the host. The Any Interrupt bit and the AT interrupt signal will also be set. Most operating systems will choose to leave this interrupt disabled to avoid the generation of extra interrupts. The host adapter will normally empty Mailbox Out entries to its local RAM so rapidly that round-robin filling of the Mailbox Out entries will assure that a Mailbox Out entry will already be empty by the time the host is ready to fill it again.

If the host finds that all Mailbox Out entries are full, it can enable the Mailbox Out Available interrupt by executing an Enable Mailbox Out Interrupt command through the I/O Command Port. The Enable Mailbox Out Interrupt command is one of the two commands that can be executed without waiting for the IDLE state of the host adapter. As soon as any Mailbox Out entry is cleared by the host adapter, an MBOA interrupt will be generated to indicate to the host that an MBO entry is available. An MBOA interrupt is generated after that each time a Mailbox Out entry is cleared by the host adapter until an Enable Mailbox Out Interrupt command is executed to force the reporting of MBOA interrupts to be disabled. If the SCRD or HACC interrupts are present, the MBOA interrupt is not presented until they are cleared. At all other times, MBOA is presented immediately.

Bit 0 - Mailbox In Full (MBIF)
This bit, when one, indicates that an entry has been placed by the host adapter in the Mailbox In. The interrupt should be reset as soon as possible so that any subsequent interrupts can be detected. The host adapter may return information in other

Mailbox In entries, so the host should check the next entry to determine if more than one set of information has been provided. The MBI entries are filled in round-robin order, so the host should simply check the next MBI entry after the last one that was found when a new MBIF interrupt occurs.

If an MBIF interrupt is set and other Mailbox In entries are made before the interrupt is cleared, then all the entries can be scanned as found. The new MBIF interrupt will be presented if the SCRD and HACC interrupts are cleared. A new MBIF interrupt will be presented regardless of the state of the MBOA interrupt bit. It is important to clear and record each interrupt as soon as possible to avoid the possible accidental resetting of a valid interrupt. In addition, it is desirable to enable the MBOA interrupt as rarely as possible. The host system software must be ready to scan for MBI entries even if no MBIF interrupt occurred.

Reset Functions

The reset functions provided by the AHA-1740A/1742A/1744 are extensive to allow the fullest flexibility and architectural consistency, both with SCSI and with the Industry Standard Architecture.

Hard Reset Operations

Resets may be generated by the hardware through two mechanisms. The RESET signal from the ISA socket is generated by the system board to reset or initialize all installed adapters upon power-on or during a low line voltage condition. The system can also activate this signal under host program control. In addition to the RESET signal, the setting of the HRST bit (bit 7 of the Host Adapter Control Port) will force a hardware reset to the AHA-1740A/1742A/1744. Regardless of the source, a Hard Reset forces the following actions on the AHA-1740A/1742A/1744.

- All internal registers of the AHA-1740A/1742A/1744 are returned to their reset condition.
- The host adapter's microprocessor returns all internal information and parameters to their initial state.
- The host adapter performs all required internal diagnostics.
- A standard SCSI Reset condition is generated to all other attached SCSI devices.

During the Hard Reset process, the AHA-1740A/1742A/1744 will indicate to the attached host that self-testing is in process by raising the STST bit in the Host Adapter Status Port. After the Hard Reset process is complete, the AHA-1740A/1742A/1744 will indicate that initialization parameters are required from the host by raising the INIT bit in the Host Adapter Status Port.

SCSI Reset Operations

The SCSI Reset condition is defined in the SCSI Standard, X3.131-1986, Section 5.2.2. A SCSI Reset condition may be forced by any SCSI device on the bus. The condition is forced by the assertion of the SCSI Reset signal.

The AHA-1740A/1742A/1744 has four mechanisms which may force a SCSI Reset condition. The SCSI Reset condition may be invoked from the host software if the software sets the SCRST bit (Bit 4 of the Host Adapter Control Port). In this case, the normal SCSI Reset operations will be performed by the host adapter and the SCSI Reset signal will be asserted on the SCSI bus. In addition, the SCRD bit (Interrupt Flag Port bit 3) will not be set, since the host itself caused the reset.

The SCSI Reset is invoked if a Hard Reset is generated, either by the system board RESET signal or by the setting of the HRST bit. This reset is described in the *Hard Reset Operations* section.

The SCSI Reset condition may be invoked by the AHA-1740A/1742A/1744 as part of the recovery mechanism for a bus phase error. Bus phase errors may include detection of an invalid information transfer phase or detection of an impossible phase sequence (Command Phase after a Data Phase in the same command). In this case, the normal SCSI Reset operations will be performed and the SCSI Reset signal will be asserted on the SCSI bus. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate interrupt signal to be presented.

The SCSI Reset condition may be invoked by another SCSI device attached to the AHA-1740A/1742A/1744 as part of the other device's recovery mechanism or initialization procedure. In this case, the normal SCSI Reset operations will be performed. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate ISA interrupt signal to be presented.

SCSI Soft Reset Option

The SCSI standard indicates two optional methods of handling the normal SCSI Reset operations. The AHA-1740A/1742A/1744 implements the Soft Reset option, described in Section 5.2.2.2 of the SCSI specification. The Soft Reset option is designed to allow a SCSI Reset signal to correctly clear the SCSI bus, but to allow ongoing system operations to continue without any major interruptions. When the SCSI Reset occurs, any activity on the SCSI bus is immediately halted and all bus lines are cleared from the bus. After the Reset condition ends, any operations in progress are again allowed to start up in the normal manner. No status or pointer information is destroyed. All disconnected commands are allowed to reselect and continue in the normal manner. This Soft Reset function allows a multiple initiator system to use reset to clear certain types of bus failures without damaging ongoing tasks from any initiator.

The SCSI Soft Reset option is useful in multitasking systems that cannot tolerate the overhead of a complex reconfiguration and reinitialization after a normal reset operation. For the SCSI Soft Reset option to operate correctly, all SCSI devices that communicate on the SCSI bus must support the Soft Reset option. If any SCSI devices support the Hard Reset option, it is likely that operations will be terminated without warning and the system will have to time out and monitor the requirement to restart some activities.

SCSI Hard Reset Option

The Hard Reset option is designed to restore all attached SCSI devices, including both hosts and peripheral devices, to their power-on reset state. All system activities that have not been recorded on a nonvolatile memory device or through another SCSI path are completely lost and must be restarted. The system must be completely reinitialized. For certain types of systems that frequently do back-up or check point their transactions, that reinitialize quickly and easily, or that infrequently do resets, the Hard Reset option is appropriate. The AHA-1740A/1742A/1744 responds to a SCSI Reset condition by executing only the Soft Reset option, but it notifies the host whenever a SCSI Reset condition has been established by causing an interrupt to the host. The host then has the option of converting the Soft Reset to a Hard Reset by forcing the host adapter to clear all the ongoing operations and return to its initial state. The host requests this by raising the SRST bit (bit 6 of the Host Adapter Control Port). The host must raise the SRST bit within 300 microseconds to disable the restarting of operations according to the rules of Soft Reset. The raising of the SRST bit causes the host adapter to abandon all CCBs and prepare itself to begin accepting new instructions from the host. No secondary SCSI Reset signals are activated. The mailbox initialization and all normal SCSI initial conditions are reset by the SRST bit, so that reinitialization is required to restart the system. Of course the system still has the right at any time that the IDLE bit (bit 4 of the Host Adapter Status Port) is on to execute any of the adapter commands and modify the mailbox address or the SCSI initial conditions.

If the host requires that the SCSI be reset according to the SCSI Hard Reset option, the host raises the HRST bit. The host adapter will then set a SCSI Reset condition on the SCSI Bus and clear all its CCB and status information, thus performing a SCSI Hard Reset with a single load to the Host Adapter Control Port. Reinitialization will be required.

EISA Expansion Identifiers

Expansion board identifiers is a term used in the EISA specification for the parameters used to integrate an add-in card into an EISA host system. These identifiers are used by the system ROM during configuration to recognize the information provided in the configuration file. The configuration file is provided as a part of the system software or in the separate ASW-C174 Configuration software package.

This automatic configuration eliminates the need for switches or jumpers and replaces them with programmable registers. It also resolves conflicts between system

resources such as interrupt levels and DMA channels when they are assigned. Refer to the EISA Specification, Section 2.6 and Section 3.3 for more information.

There are five groups of addressable hardware used to interface the host adapter with the host system across the EISA bus:

- Board ID registers
- Configuration registers
- BIOS EPROM
- Standard Mode (Group 1) I/O ports (used in Standard Mode)
- Enhanced Mode (Group 2) I/O ports (used in Enhanced Mode)

Only the Board ID and Configuration registers are accessible after a power on reset (RESDRV). The I/O port Standard Mode (Group 1) registers are accessible when the CDEN bit on the board is set. The BIOS EPROM is accessible when both the CDEN and BIOSEN bits are set.

The board IDs are required for EISA board configuration. The ID is used by the system ROM at power up initialization to locate the adapter and determine the slot in which it is installed. After the RESDRV signal indicates power on, HID0 is set to 7Xh to indicate not ready. The IDs are loaded by the local processor. The interrupt level, I/O port base address, BIOS base address, and SCSI initialization parameters are programmed in the Configuration registers. All of these registers may be written or read at any time.

Expansion Board ID Registers

The expansion board identifier registers are always available for access on the bus by the host system. They are used to transfer basic information on the identity of the board and its revision level from the AHA-1740A/1742A/1744 to the host.

Host ID 0 (HID0, zC80, R)

HID0 is the first byte of the expansion board ID. It is written by the local processor and read by the system processor. HID0 is initialized to 7Xh on RESDRV. HARDST or SOFTRST has no effect.

Bit	Definition
7	Reserved (0).
6-2	First compressed character of a manufacturer's ID. Bit 6 is the most significant bit. This character is always "A" wihch results in a compressed code of '00001'B.
1-0	Most significant two bits of the second compressed character of manufacturer's ID. Bit 1 is the most significant bit. The character is continued in register HID1. The character is always "D," which is represented by '00100'B.

Host ID 1 (HID1, zC81, R)

HID1 is the second byte of the expansion board ID. It is written by the local processor and read by the system processor. RESDRV, HARDST or SOFTRST has no effect.

Bit	Definition
7-5	Least significant three bits of the second compressed character of manufacturer's ID. The most significant two bits are found in register HID0. The character is always "D," which is represented by '00100'B.
4-0	Third compressed character of manufacturer's ID. Bit 6 is the most significant bit. This character is always "P" which results in a compressed code of '10000'B.

Host ID 2 (HID2, zC82, R)

HID2 contains the adapter's product number. It is written by the local processor and read by the system processor. RESDRV, HARDST or SOFTRST has no effect. Bit 7 is the significant bit. The AHA-1740/1740A/1742A products number is 00h and the AHA-1744 is 01h.

Host ID 3 (HID3, zC83, R)

HID3 contains the revision level of the firmware resident on the board. This is used to identify the capabilities of the board to the manager and other software. The revision level may be changed during the firmware download process described in Chapter Three, *ADL Utility*. It is written by the local processor and read by the system processor. RESDRV, HARDST or SOFTRST has no effect. The revision code for the AHA-1740/1744 is 00h, the AHA-1740A is 01h and the AHA-1742A is 02h.

Board Configuration Registers

These registers are used by the host process to define parameters on the board necessary for normal operation. This function was normally provided by jumpers or on-board DIP switches in ISA boards. These registers are accessible at any time.

Expansion Board Control Register (EBCTRL, zC84, W/R)

EBCTRL is used by the system software to control the host adapter hardware. Bit 2 is write only, 1 is read only and bit 0 is write/read.

Bit	Definition
7-3	Unused. (0)
2	ERRST When this bit is set, HAERR and CDEN are reset to 0. (0)
1	HAERR When this bit is one, the host adapter has detected a serious error. Further operation will produce unreliable results. This bit is set by the local processor. (0)
0	CDEN When this bit is cleared, the host adapter is held disabled. During this time only expansion board registers can be accessed. (0)

I/O Port Address (PORTADDR, zCC0, W/R)

PORTADDR selects the base address for the I/O port interface. It is compared with the system address every cycle. If a match occurs, data will either be driven or sampled on the bus. PORTADDR is initialized with a value provided in the configuration file during configuration.

Bit	Definition
7	ENHANCED INTERFACE When set, the host adapter will power up in Enhanced Mode. It will use the EISA I/O address space for command execution. When cleared, the host adapter will power up in Standard Mode. When in this mode, the host adapter will use ISA space for command execution.
6	CONFIGURE When set, the host adapter is instructed to program the local EEPROM with the data to be defined in the next CCB.
5-3	Reserved
2-0	ADR 2-0. Port address selection bits. These bits select the base address of the host adapter I/O register and should be written according to the chart below.

I/O Port Address Table	
ADR bits 2 1 0	**Port Address (hex)**
0 0 0	Disable
0 0 1	N/A
0 1 0	130
0 1 1	134
1 0 0	230
1 0 1	234
1 1 0	330
1 1 1	334

BIOS Control

The onboard BIOS EPROM is available as the third set of addressable information. It is a system processor read access only and is independent of the local processor. After RESDRV system processor access is not allowed. CDEN and BIOSEN must be set to 1 (see *Expansion Board Control Register*).

The BIOS is provided to allow the user to use the host adapter in lieu of, or in addition to a standard hard disk controller. The BIOS has at its disposal 2KBytes of 8-bit wide system RAM which overlays the last 2KBytes of the BIOS. This RAM is writeable when WRTPRT (BIOSADDR bit 7) is zero, and may only be read when RAMEN (BIOSADDR bit 6) is set.

The BIOS will take on the personality of the firmware that is activated. If the Standard Mode is selected at configuration time, the Standard Mode BIOS will run, and conversely for the AHA-1740 mode, the AHA-1740 BIOS will run.

BIOS Address Register (BIOSADDR, zCC1, W/R)

The BIOSADDR register maps the BIOS to one of 12 locations between C0000h and EFFFFh at 16K boundaries. In addition, the BIOS has the last 2 KBytes of address space as overlaid RAM. The RAM may be written to when enabled by setting the RAMEN bit and clearing the WRTPRT bit. The RAM may be read by setting the RAMEN bit. On power-up, the RAM is disabled.

Bit	Definition
7	WRTPRT When set, write protects the RAM.
6	BIOSEN Enables the BIOS on this board to respond to system reads in the selected address space.
5	RAMEN When set, enables the BIOS RAM overlay. When cleared, disables the RAM overlay writing or reading.
4	Reserved
3-0	BIOSSEL These bits select the starting address of the system BIOS according to the following table.

BIOS Address Table	
BIOSSEL bits 3 2 1 0	**BIOS Address (hex)**
0 0 0 0	Not used
0 0 0 1	Not used
0 0 1 0	C8000
0 0 1 1	CC000
0 1 0 0	D0000
0 1 0 1	D4000
0 1 1 0	D8000
0 1 1 1	DC000
1 0 0 0	E0000
1 0 0 1	E4000
1 0 1 0	E8000
1 0 1 1	EC000
1100-1111	Not used

Interrupt Definition (INTDEF, zCC2, W/R)

An interrupt channel may be selected from one of several on the EISA bus. The interrupt may be programmed as high true or low true. When high true, the interrupt is a two state signal and acts like an edge triggered interrupt, and may not be shared with another board. If the interrupt is on and disabled, it will go to the low state, and back again to the high state when enabled again.

When programmed as low true, interrupt is an open collector signal and may be shared with another board that also has an open collector interrupt. If the interrupt is on and disabled, it will turn off, and then to an on low state when enabled again.

Bit	Definition
7-5	Reserved
4	INTEN When set, enables interrupts to occur on the EISA bus.
3	INTHIGH When set, the interrupt is programmed to high true state.
2-0	INTSEL These bits select the interrupt channel to be driven on the EISA bus according to the following table.

Interrupt Channel Table	
INTSEL bits 2 1 0	**Interrupt Channel**
0 0 0	9
0 0 1	10
0 1 0	11
0 1 1	12
1 0 0	Not used
1 0 1	14
1 1 0	15
1 1 1	Not used

SCSI Definition (SCSIDEF, zCC3, W/R)

Programming this byte sets up basic SCSI parameters.

Bit	Definition
7-5	Reserved (0)
4	RSTPWR When set, the host adapter will generate a SCSI Reset on power up and on a Hard Reset. When cleared, the host adapter will not generate a SCSI Reset on power up or on a Hard Reset to the board.
3-0	HSCSIID These bits define the SCSI ID of the host adapter. Bit 3 is the MSB.

SCSI ID Table	
HSCSIID bits 3 2 1 0	**SCSI Address**
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1000-1111	Reserved

Bus Definition (BUSDEF, zCC4, W/R)

This register allows the configuration of certain EISA bus features supported by the AHA-1740A/1742A/1744.

Bit	Definition
7-4	Reserved
3-2	DMA Channel for Standard Mode **Bit 3** **Bit 2** **DMA Channel Returned** 0 0 0 0 1 5 1 0 6 1 1 7
1-0	BUSON These bits are written in order to set the time that the AHA-1740 stays on the bus when preempted by another device. **Bit 1** **Bit 2** **µs before ending transfer** 0 0 0 0 1 4 1 0 8 1 1 Not used

Reserved Registers

The following registers are reserved for future use.

- Reserved 0 (RESV0, zCC5, W/R)
- Reserved 1 (RESV1, zCC6, W/R)
- Reserved 2 (RESV2, zCC7, W/R)

I/O Port Register Standard Mode (Group 1)

The I/O Control Standard Mode (Group 1) registers form the primary communication channel between the system and the adapter for Standard Mode operation. When power is initially applied, these registers will not respond to system accesses. EBCTRL, bit 0, must be set before access is allowed.

These registers are not writable or readable until the CDEN bit in the control register is set. Refer to the section titled *Expansion Board Control Register*. The eight-bit port registers form the primary communications channel and are addressed with reference to a base address, plus offset. There are three I/O ports which reside in ISA I/O address space. The base address is selected by writing to the PORTADDR register.

Base+0 Control and status
Base+1 Command and data
Base+2 Interrupt information

The Control/Status Port controls the host adapter. The bits can initiate hardware or firmware operation directly. The Control Port allows the system to control the host adapter hardware, such as executing a hardware reset. The Status Port provides status about the state of the host adapter firmware and hardware.

The host adapter supports commands sent directly to I/O address space through CMD/DAT. LAVAIL indicates that the write port is full and should be sampled for zero before writing to CMD/DAT. HAVAIL indicates that the read port is full and should be sampled for one before reading from CMD/DAT. The low-level commands are executed by placing the appropriate command byte followed by any additional parameters into CMD/DAT. Parameters are then transferred from the host adapter through port I/O or into the system through Bus Master transfers to provide the information necessary to complete the command.

In response to a reset, if the host adapter passes diagnostics, then the local processor will set POCIP (LSTAT bit 7) to zero and INITRQD (LSTAT bit 5) to one. These bits are available in the system STATUS register and this state means that mailbox initialization may proceed. Additional parameters are passed via the CMDDAT register.

If the host adapter fails diagnostics, then the local processor will set POCIP (LSTAT bit 7) to zero and POCFAIL (LSTAT bit 6) to one. These bits are available in the

system STATUS register and this state means that a hardware error has occurred on the board.

Control Port (CNTRL, Base address + 0, W)

The Control Port is written by the system at the Base address. It is used to control the hardware directly.

Bit	Definition
7	HARDRST When set, the host adapter will be put in a power on state. The firmware will be loaded from EEPROM to RAM and power on diagnostics will be run. This bit is self-clearing and need not be reset by the system. (0)
6	SOFRST When set, the soft reset interrupt will be generated and presented to the local processor. POC diagnostics will not be run, but the host adapter hardware will be initialized and all commands will be cleared from the internal queue. This bit is cleared by a local processor write to CLRINT. (0)
5	CLRINT When set, the EISA interrupt line IRQx and the interrupt status register are reset. This bit is self-clearing and need not be reset by the system. (0)
4	SCSIRST When set, the SCSI Reset interrupt will be generated and presented to the local processor. This bit is cleared by a local processor write to CLRINT. (0)
3-0	Reserved. (0)

Status Port (STATUS, Base address + 0, R)

Data read on the Status Port does not reflect data that was written to Control Port; although, they share the same address space. The Status Port is written by the local processor to present host adapter information. Bits 3 and 2 are set by hardware, and bit 7 is set by hardware on power up only.

Bit	Definition
7	POCIP Power On Confidence in Progress. When this bit is one, it indicates that the host adapter is performing internal diagnostics. It is cleared by the firmware when POC diagnostics are finished. This bit is set by the local processor when it writes a one to bit 7 of HASTAT. (1)
6	POCFAIL Power on Diagnostics Failed. When this bit is one, it indicates that the power on diagnostics failed. This bit is valid when bit 7 is zero. This bit is set by the local processor when it writes a one to bit 6 of HASTAT. (0)
5	INITRQD Initialization Required. When this bit is one, it indicates that the host adapter has successfully completed self-diagnostics and initialization data is required. Initialization data will be passed via the Command/Data, Base + 1 register. This bit is set by the local processor when it writes a one to bit 5 of HASTAT. (0)
4	HAIDLE Host Adapter Idle. When this bit is one, it indicates that the host adapter is in the idle state. This bit is set by the local processor when it writes a one to bit 4 of HASTAT. (0)
3	LAVAIL Command/Data Available to local processor. When this bit is one, the system has loaded CMD/DAT (Base + 1) with a command or parameter. This bit is polled by the local processor to determine if a byte is ready. It is cleared when the local processor reads the LCMDDAT register. (0)

Bit	Definition
2	HAVAIL Information is Available to the system. When this bit is one, the local processor has loaded CMD/DAT (Base + 1) with data. It is cleared when the system reads CMD/DAT. This bit is also read by the local processor. (0)
1	Reserved. (0)
0	INVCMD Invalid Host Command. When this bit is one it indicates that the command or parameter received from the Local Command/Data register is illegal. This bit is set by the local processor. (0)

Command/Data (CMD/DAT, Base address + 1, W/R)

This register gives the system a path by which it can communicate with the host adapter. Commands and parameters are sent by the system and status is received through this port. HAVAIL and LAVAIL provide the handshake for accessing this register.

System Interrupt (INTRPT, Base + 2, R)

The interrupt register provides further status regarding why an interrupt was generated. The interrupt status is written by the local processor via Local Interrupt register (LINTRG). It is reset by the system by setting CLRINT (bit 5 in CNTRL) to one. Bit 7 must be set along with the interrupt status bit for the interrupt to be generated. When bit 7 is set, IRQx is asserted on the EISA bus.

Bit	Definition
7	ANYINT When this bit is one, a host interrupt is generated. It is set when local register LINTRG bit 7 is set. (0)
6-4	Reserved (0).
3	SCSIRD SCSI Reset Detected. When this bit is one, it indicates that the host adapter received a reset from the SCSI Bus. Set when local register LINTRG bit 3 is set. (0)
2	HACC Host Adapter Command Complete. When this bit is one, it indicates that the host adapter has completed the command that was sent through the CMD/DAT register. Set when local register LINTRG bit 2 is set. (0)
1	MBOAVAIL Mailbox Out Available. When this bit is one, it indicates that at least one mailbox out area is available for the host to use. Set when local register LINTRG bit 1 is set. (0)
0	MBISTRD Mailbox In Stored. When this bit is one, it indicates that the host adapter has completed a command from the Mailbox Out area and has placed the completion status to the Mailbox In area. (0)

I/O Port Register Enhanced Mode (Group 2)

These registers are used for operating in Enhanced Mode and may be used at any time. They consist of mailbox out, mailbox in, control, status, attention, interrupt 1 status, and interrupt 2 status. The mailbox out and in are used for general data transfer and represent either an address or Immediate command parameters. Control, status, attention and the interrupt registers are used for general operation.

The host should start operation by testing for the Mailbox Out Empty status bit to be set and the Busy bit to be cleared to see if the Mailbox Out registers are available for a CCB address or Immediate command. If Mailbox Out Empty is set and Busy is cleared, the host must write to the address which will clear the Mailbox Out Empty status bit and write the appropriate code into the Attention register. Writing to the Attention register will set the Busy bit, and will set the local processor interrupt. The local processor will then read the Attention register in response to the interrupt which will clear the Busy bit. The OP Code in the Attention register must indicate that a CCB address is present in the mailbox out. The local processor will then read the mailbox out address and set the Mailbox Out Empty bit. The host processor may then load another address into the mailbox out.

When the adapter has completed the command, it will sample the EISA interrupt status line. If cleared, then the mailbox in will be loaded with the CCB pointer of the command which has just finished. The adapter will then load the appropriate interrupt status code which will set the EISA interrupt.

The host responds to the interrupt by reading the interrupt status 1 register to determine if the command completed with or without error, and reads the Mailbox In register to get the pointer of the command which has just finished. The host then clears the interrupt by writing to G2CNTRL register with bit 6 set. When the EISA interrupt is cleared, the EOI local interrupt is generated which tells the local processor that the Mailbox In is free and another CCB may be posted.

When Immediate commands are to be executed, the OP Code of the command is written to the LSB of the Mailbox Out register. Additional data will be placed in the rest of the Mailbox Out registers in order of incrementing address. The host will set the Host Ready bit and write the Attention register with the Immediate command code. The adapter reads the Mailbox Out registers and determines the Immediate command and the amount of data to follow, and then clears the Host Ready bit. If more data is needed, the host monitors the Host Ready bit and when it is cleared, loads the next group of data into the Mailbox Out. The host then sets the Host Ready bit. The adapter monitors the Host Ready bit, reads the data from the Mailbox Out registers and clears the Host Ready bit. This process repeats until all data is received. The adapter then executes the command and posts status in the Mailbox In registers. The adapter clears the Host Ready bit, loads the appropriate status in the Interrupt 1 Status register and interrupts the host. The host reads the interrupt status and reads the information from the Mailbox In registers. If more than four bytes are to be returned, the host sets the Host Ready bit and the adapter loads the next data group in the Mailbox In registers. The adapter clears the Host Ready bit, and the host may then read the mailbox in data. This process repeats until the transfer is complete.

In response to a reset, if the host adapter passes diagnostics, then a value of 00H will be loaded in MBOXIN0. ATTN will also be read to clear the Busy bit. If the host

adapter fails diagnostics, then the local processor will load the value appropriate for the failure in MBOXIN0, according to the following list, and read ATTN to clear the busy bit.

Reset Codes	
00	No Error
01	Microprocessor ROM Test failure
02	RAM test failure
03	Power Protection device error
04	Microprocessor internal peripheral test failure
05	Buffer control chip failure
06	Reserved
08	SCSI interface chip failure
Soft Reset Status	
07	Hardware failure

Mailbox Registers

Mailbox out byte 0 (MBOXOUT0, zCD0, W/R)
This is the least significant byte of a 32-bit address pointer to a CCB or the OP Code of an immediate command.

Mailbox out byte 1 (MBOXOUT1, zCD1, W/R)
This is the least middle significant byte of a 32-bit address pointer to a CCB or additional data for an immediate command.

Mailbox out byte 2 (MBOXOUT2, zCD2, W/R)
This is the most middle significant byte of a 32-bit address pointer to a CCB or additional data for an immediate command.

Mailbox out byte 3 (MBOXOUT3, zCD3, W/R)
This is the most significant byte of a 32-bit address pointer to a CCB or additional data for an immediate command.

Mailbox in 0 (MBOXIN0, zCD8, R)
This is the least significant byte of a 32-bit address pointer to a CCB or additional data for an immediate command.

Mailbox in 1 (MBOXIN1, zCD9, R)
This is the least middle significant byte of a 32-bit address pointer to a CCB or additional data for an immediate command.

Mailbox in 2 (MBOXIN2, zCDA, R)
This is the most middle significant byte of a 32-bit address pointer to a CCB or additional data for an immediate command.

Mailbox in 3 (MBOXIN3, zCDB, R)
This is the most significant byte of a 32-bit address pointer to a CCB or additional data for an immediate command.

Attention (ATTN, zCD4, W/R)

Bit	Definition
7-4	OP Code Operation Code. Defines the contents and usage of the mailbox out registers. All codes not named will be ignored. 1 = Immediate command 3 = Reserved 4 = Start CCB 5 = Abort CCB E = Reserved F = Reserved
3-0	Target ID Contains the SCSI ID of the device or host adapter for which this command pertains.

Enhanced Mode (Group 2) Control (G2CNTRL, zCD5, W/R)

Bit	Definition
7	Hard Reset Resets hardware. When set, holds hardware reset and sets the Busy bit in the status regsiter. This bit should be set for a minimum of 10 microseconds. When cleared, the reset line is released.
6	Clear EISA interrupt When set, this bit clears a pending EISA interrupt. At the same time, it sets the EOI interrupt to the local processor, to indicate the end of interrupt processing. It is self-clearing.
5	Set Host Ready This bit sets the Host Ready status bit in G2STAT2 register.
4-0	Unused

Enhanced Mode (Group 2) Interrupt Status (G2INTST, zCD6, R)

Bit	Definition
7-4	Interrupt Status 4 bits 1 = CCB completed with success 5 = CCB completed with success after retry 7 = Adapter hardware failure A = Immediate command completed with success C = CCB completed with error D = Asynchronous event notification E = Immediate command completed with error
3-0	Target ID SCSI ID of command

Enhanced Mode (Group 2) Status (G2STAT, zCD7, R)

Bit	Definition
7-3	Reserved
2	Mailbox out empty Set to one by firmware when it is done with the mailbox out. Cleared by software writing to any mailbox out location.
1	Interrupt pending Reflects the state of the EISA interrupt line from the Enhanced Mode (Group 2) interrupt before the enable/disable logic.
0	Busy Set by a write to the Attention register or a hard reset. Cleared when the firmware reads the Attention register.

Enhanced Mode (Group 2) Status 2 (G2STAT2, zCDC, R)

Bit	Definition
7-1	Unused
0	Host Ready This bit is set by the host (G2CNTRL bit 5) to indicate that it has loaded the next data group into the mailbox out or that it has read the data group from the mailbox in. This bit is used during Immediate command execution and need not be set during normal operation. It is cleared by the adapter when all pending information is processed.

Diskette Registers

The host communicates with the floppy disk controller via the set of registers defined below:

I/O Address Primary (hex)	Secondary (hex)	Read	Write
3F2	372	—	Digital Out
3F4	374	Main status	Main status
3F5	375	Diskette data	Diskette data
3F7	377	Digital input	Diskette Ctrl

Digital Output Registers (Write 3F2)

The digital output register (DOR) is a write-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line.

> Note
> Channel reset clears all bits.

The bit definitions follow:

Bit	Definition
7	Reserved (set to 0)
6	Reserved (set to 0)
5	Drive *B* Motor Enable
4	Drive Motor Enable
3	Enable diskette interrupts and DMA
2	Diskette function reset
1	Reserved (set to 0)
0	Drive Select: A "0" on this bit indicates that drive *A* is selected.

Diskette Controller Registers (Read/write 3F4 and 3F5)

The diskette controller has two main system processor accesses; a status register and a data register. The 8-bit status register (3F4h), has the status information about the diskette and may be accessed at any tim. The 8-bit data register (3F5h), which actually consists of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, and pareameters, and provides diskette-drive status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command. The main status register may only be read and is used to facilitate the transfer of data between the processor and diskette controller. The bits in the main status register (3F4h) are defined as follows:

Bit	Definition
7	Request for Master (RQM) The data register is ready to send or receive data to or from the processor.
6	Data Input/Output (DIO) The direction of data transfer between the diskette controller and the processor. If this bit is a 1, transfer is from the diskette controller's data register to the processor; if it is a 0, the opposite is true.
5	Non-DMA mode (NDM) The diskette controller is in the non-DMA mode.
4	Diskette Controller Busy (CB) A read or write command is being executed.
3	Reserved (set to 0)
2	Reserved (set to 0)
1	Diskette Drive B Busy (DBB) Diskette drive *B* is in the seek mode
0	Diskett Drive A Busy (DAB) Diskette drive *A* is in the seek mode.

The diskette controller can perform eleven different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the diskette controller and the processor, each command can be considered to consist of three phases:

- Command Phase: The processor issues a sequence of write commands to the diskette controller that direct the controller to perform a specific operation.
- Execution Phase: The diskette controller performs the specified operation.
- Result Phase: After completion of the operation, status and other housekeeping information is made available to the processor through a sequence of read operations from the data register.

Digital Input Register (Read 3F7)

The digital input register is an 8-bit, read-only register used for diagnostic purpose. The following are bit definitions for this register.

Bit	Definition
7	Diskette Change
6	Tri-state (hard disk function)
5	Tri-state (hard disk function)
4	Tri-state (hard disk function)
3	Tri-state (hard disk function)
2	Tri-state (hard disk function)
1	Tri-state (hard disk function)
0	Tri-state (hard disk function)

Bit 7 sets when power goes on or a diskette is removed from the drive. Bit 7 resets when the drive detects a diskette in the drive or a step pulse occurs while the drive select signals are true. Only the 1.2 MByte, 5.25-inch and 1.44 MByte, 3.5-inch diskette drives drive this signal.

Diskette Control Register (Write 3F7)

Bit	Definition
7	Not used
6	Not used
5	Not used
4	Not used
3	Not used
2	Not used
1	DRATESEL
0	DRATESEL

Default precompensation delay values depend upon the data rate selected as shown in the following table:

Data Rate	Delay
1 Mps	83.00
500 Kps	125.00
300 Kps	125.00
250 Kps	125.00

DRATESEL Data Rate Select

These bits select the data transfer rate. Reset clears these two bits. Data rates get selected as follows:

Bit		Data Rate (bits/second)	
1	0	MFM	FM
0	0	500	250
0	1	300	150
1	0	250	125
1	1	1000	Not defined

Firmware Download (AHA-1740/1744 Only)

The AHA-1740A/1742A permanently stores both Standard and Enhanced Mode firmware in an EPROM. A microcode upgrade consists of replacing that EPROM with another, and is seldom required. Please contact Adaptec for further information.

The AHA-1740/1744 permanently stores both Standard and Enhanced Mode firmware in an E^2PROM.

The local processor will download the firmware from EEPROM and will run from RAM. In order to promote maximum data integrity, the firmware calculates checksums for itself while not executing commands. The firmware is interrupt driven by events on the host and SCSI side.

The firmware is programmed into the EEPROM by setting the Enable Prom Write bit in the PORTPH register. When this is done, reads will come from the RAM and writes will go to the EEPROM. The firmware is enabled to reprogram when the CONFIG bit in PORTADDR is set and the firmware download command is given. The AHA-1740 INTERFACE bit in PORTADDR indicates which code to program. Provision is also made for loading of new firmware without programming. This definition is in the AHA-1740 Configuration document.

Hardware Configuration Requirements

The following host adapter configuration options must be defined prior to setting the card enable bit in register zC84:

- The BIOS location must be set to an address which does not conflict with other system resources. It may also be enabled or disabled for the particular board.
- The interrupt channel needs to be selected and enabled. In addition, the interrupt may be chosen to be high or low-level true.
- The I/O port needs to be selected. The AHA-1740/1744 has two options, the 1540 interface or 1740 interface. If the 1540 interface is chosen, then the base address must be set to the proper value. The default value should be 330h.
- The AHA-1740/1744 can stay on the bus for a programmable amount of time after preemption. The default value should be 2.
- After these registers are programmed, the Card Enable bit, as defined in the EISA specification, must be set. This indicates to the adapter that the registers are valid.

SCSI Configuration

To initialize the SCSI interface, first set the SCSI ID. Then the host adapter needs to be told whether to issue a SCSI Reset on power-on. In order to facilitate power-up, the BIOS needs information about the SCSI bus physical devices. It may be necessary for the firmware to know this for future enhancements, so it is included in this definition. This information is not key to operation, and is loaded separately by the BIOS. Up to 16 devices are allowed for future expansion.

- Send a SCSI Start command
- Device supports more than one LUN
- Enable/disable SCSI parity
- Enable/disable synchronous negotiation
- Maximum synchronous transfer rate
- Enable/disable disconnection
- Error condition if device not installed
- Enable disk BIOS support
- Include removable media in disk BIOS support

BIOS Driver Needs

At power-on time the BIOS needs information about the SCSI bus to aid in minimum power-on time and confidence in a complete working system. The information given tells the BIOS that a device is, or is not, installed; if intalled and a selection error occurs, to wait for no error, or report the error after a timeout; if installed and a selection error occurs, to not report the error and continue with power-on initialization.

SCSI Subsystem Configuration

Due to a limitation of the hardware, there are only a few registers that may be loaded at power-up time. Some information not directly controlling hardware may be loaded independently of the normal EISA Configuration program that runs at power-on time. The BIOS will program the AHA-1740 on power-up using the Initialize SCSI Subsystem command with this additional information. The hardware configuration registers will still be programmed by the configuration program. The definition of the command and data structure follows.

Initialize SCSI Subsystem Command (Standard Mode)

The command to initialize the SCSI Subsystem in Standard Mode is an additional host adapter command. This command is sent in the normal manner described in the AHA-1540 manual using the LAVAIL status bit in the status register. The command byte (10h) is followed by one data byte which describes the global setting of parity enable, synchronous transfer, and disconnection. The definition is as follows:

Bit	Definition
7	Reserved (set to 0)
6	Reserved (set to 0)
5	Enable parity check
4	Reserved (set to 0)
3	Enable synchronous transfer
2	Enable Disconnection
1	Reserved (set to 0)
0	Reserved (set to 0)

Initialize SCSI Subsystem Command (Enhanced Mode)

The command to initialize the SCSI Subsystem is a standard 48-byte command using the AHA-1740 I/O interface. The definition of the command is given in Chapter Six, *Enhanced Mode Firmware Description.*

FlagWord 1 Options

Disable Status Block (bit 14) is supported. Setting this bit will disable the writing of the termination status block if no error occurs. All other bits should be set to zero.

Refer to Appendix D, *EISA Free-Form Data* for the initial SCSI subsystem data structure.

Configuration Byte Description and Defaults

The following describes the SCSI device configuration byte format. Firmware default values are also given. These defaults are used by the firmware to interface with the various targets in the event that no Initialize SCSI Subsystem command has been received by the host adapter.

Byte 0

Bit 7 - Allow removable media in BIOS disk scan
This bit is used by the host adapter BIOS only, it does not affect operation. When this bit is set, the BIOS will include a removable media device in the scan for devices to support under Int 13h.

> Note
> This feature does not support removal or exchange of the media. The drive is treated as a fixed media drive only. This is primarily intended to allow boot from a removable media disk drive.

Bit 6 - More than one LUN supported
This bit is used by the host adapter BIOS only. When set, this bit indicates that the target will support more than one LUN. In the default state, only LUN 0 is supported for each SCSI target.

Bit 5 - Parity Check enable
When set, parity will be generated and checked. When cleared, parity will be generated but not checked. By default, parity checking is enabled for all targets.

Bit 4 - Send Start command
This bit is used by the host adapter BIOS only. When set, the BIOS will send a Start Stop Unit SCSI command to the target after a Test Unit Ready command returns a check condition and reports a not ready status. The Start Stop Unit command will set the Immed and Start bits and will clear the LoEj bit as defined in the SCSI 2 specification. By default, this feature is disabled for all targets.

Bit 3 - Synchronous Negotiation enable
When set, the host adapter will initiate synchronous negotiation with this target. When cleared, the host adapter will not initiate negotiation, but will respond if the target initiates negotiation. Default is to initiate synchronous negotiation with all targets.

Bit 2 - Disconnection enable
When set, the host adapter will allow disconnection to occur with this target by setting the Allow Disconnection bit in the ID Message. When cleared, the Allow Disconnection bit will be cleared. By default, disconnection is enabled for all targets.

Bit 1 - Ignore error if device not present
This bit is used by the BIOS only, and does not affect firmware operation. When set, this bit indicates that the DIOS should not display an error message if an installed device does not respond with ready status during the BIOS target scan. When cleared, the BIOS will follow its normal error reporting algorithm.

Bit 0 Enable disk BIOS support
This bit is used by the BIOS only, and does not affect firmware operation. If the bit is set, the BIOS will attempt to install the target at this address as an Int 13h addressable disk, following the normal disk scan algorithm. When cleared, the device is ignored.

Byte 1

Bit 7-3 Reserved

Bits 2-0
These bits set the maximum SCSI synchronous transfer rate that the host adapter will allow when synchronous transfers are enabled.

Bits 2-0	Maximum Synchronous Transfer Rate (MBytes/second)
000	10.0
001	6.67
010	5.0
011	4.0
100	3.33
101-111	Reserved

SCSI Subsystem Configuration Data Storage

The Initialize SCSI Subsystem data block is generated by the AHA-1740A/1742A/1744 EISA configuration file and overlay when the host adapter is installed in an EISA system. The data is generated based on selections (and/or default values) made by a user from a list of options for each SCSI target device. The data block is stored as function configuration information in free-form format in the motherboard non-volatile RAM. This information can be retrieved by the AHA-1740A/1742A/1744 BIOS, and/or drivers, via an Int 15h Read Function Configuration Information call (AH=D8, AL=01 or 81).

The free form data block stored in configuration RAM is prefixed with a length code (required by EISA specification) and a signature that identifies the data as valid SCSI subsystem configuration information. The format of the configuration data block and free form data structure containing the SCSI subsystem configuration is shown below. Note that the free form data block begins at offset 73h of the data returned by the EISA INT 15h call. The name of the function type for this data is stored by the configuration utility at offset 23h. This type string must be the eight-character ASCII string SCSIDEVS. Additional information on the function configuration information data block is given in the EISA specification.

Function Configuration Information Data Block for SCSI Subsystem Data	
Byte Offset	**Description**
22h	Function Information Byte B6 = 1 to indicate free from data
23h	Type and Subtype ASCII string "SCSIDEVS"
73h	Length of the following data block
74h	ASCII string "AHA-174x"
7C-7Fh	Reserved
80h	SCSI device 0 byte 0
81h	SCSI device 1 byte 1
82h	SCSI device 2 byte 2
83h	SCSI device 3 byte 3
. . .	. . .

❑

Chapter Five

Standard Mode Firmware Description

Host Adapter Command Overview

Standard Mode is the mode in which the AHA-1740A/1742A/1744 can operate in order to run existing software for earlier Bus Master host adapters. In Standard Mode, the AHA-1740A/1742A/1744 supports two types of commands: SCSI and adapter commands. SCSI commands are issued using the mailbox protocol and a Command Control Block (CCB). When SCSI commands are used, the AHA-1740A/1742A/1744 is operating in true multithreading mode. In this mode of operation, the AHA-1740A/1742A/1744 is capable of executing multiple commands for multiple targets concurrently. The AHA-1740A/1742A/1744 maximizes the I/O transaction throughput by managing SCSI disconnection and reconnection.

Adapter commands are issued by writing to the Command/Data Out port and most commands cannot be issued when there are outstanding SCSI commands. Adapter commands are used to initialize the host adapter and to establish control conditions within the host adapter. Adapter commands are also used to transmit the special parameters for communication between the BIOS and the host adapter for the execution of Interrupt 13 operations.

Following is a list of the adapter command operation codes (hex):

Code	Command
00	No Operation
01	Mailbox Initialization
02	Start SCSI Command*
03	Start PC AT BIOS Command
04	Adapter Inquiry
05	Enable Mailbox Out Available Interrupt*
06	Set Selection Time Out
07	Set Bus-On Time
08	Set Bus-Off Time
09	Set Transfer Speed
0A	Return Installed Devices
0B	Return Configuration Data
0C	Enable Target Mode
0D	Return Setup Data
10	Initialize SCSI Subsystem
11	Return Firmware Checksum
1A	Write Adapter Channel 2 Buffer
1B	Read Adapter Channel 2 Buffer
1C	Write Adapter FIFO Buffer
1D	Read Adapter FIFO Buffer
1F	Echo Command Data

20 Adapter Diagnostic
21 Set Host Adapter Options

*This command can be issued when the host adapter is executing a SCSI command.

All adapter commands except Start SCSI (02) and Enable Mailbox Out Available Interrupt (05) must be executed only when the IDLE bit (Status bit 4) is one. Many commands require additional parameter bytes which are then written to the Command/Data Out I/O port (base + 1). Before each byte is written by the host to the host adapter, the host must verify that the CDF bit (Status bit 3) is zero, indicating that the command port is ready for another byte of information. The host adapter usually clears the Command/Data Out Port within 100 microseconds. Some commands require information bytes to be returned from the host adapter to the host. In this case, the host monitors the DF bit (Status bit 2) to determine when the host adapter has placed a byte in the Data In I/O port for the host to read. The DF bit is reset automatically when the host reads the byte. The format of each adapter command is strictly defined, so the host adapter and host system can always agree upon the correct number of parameter bytes to be transferred during a command.

All Adapter Commands except Return Installed devices, Start SCSI, and Start PC AT BIOS typically require less than 200 microseconds to complete. Return Installed Devices will typically complete in less than three seconds. Start SCSI and Start PC AT commands completion times will vary with the SCSI device and the command issued.

No Operation (Operation Code 00)

No host adapter action is taken, but HACC is set indicating command completion. No additional information bytes are exchanged.

Mailbox Initialization (Operation Code 01)

This command is used to specify the number of mailbox locations used by the host adapter and to specify the base memory location of the mailbox area. The host adapter requires that four bytes of outbound data follow the command byte. The definition of those four bytes is shown below.

Byte	Definition
0	Mailbox count - Must be greater than zero.
1	Mailbox address (MSB)
2	Mailbox address
3	Mailbox address (LSB)
Mailbox address: Location of the first byte of the mailbox area.	

When the Mailbox Initialization command and parameters are received, the host adapter will then assume that the specified number of Mailbox Out entries and the same number of Mailbox In entries will be assigned beginning at the Mailbox address. The total number of bytes reserved for the mailbox area will be eight times the

Mailbox Count. If the Mailbox Count is zero, the INVDCMD bit will be set with HACC to indicate that the parameter is invalid.

At command completion, HACC will be set to one and INIT will be reset to zero. HACC will be reset as specified in the *Interrupt Flag Port* section of Chapter Four, *Hardware Functional Description.*

Start SCSI Command (Operation Code 02)

This command indicates that the host has made at least one Mailbox Out entry and that the host adapter should begin to scan for active MBO entries. Once scanning has been started, it continues until all MBO entries have been serviced, either by beginning the requested operations or by queuing the activities for later execution. Since it is not easy for the host to determine that scanning is still taking place, the host should normally issue this command every time a Mailbox Out is filled. This command does not require additional data bytes. To avoid unnecessary interrupts, HACC is NOT set after command completion. HACC will be set with INVDCMD if the mailbox was not yet initialized.

Start PC AT BIOS Command (Operation Code 03)

This command is used by the Adaptec BIOS to communicate with the host adapter firmware. The command is not available for use by programs other than the Adaptec BIOS.

Adapter Inquiry (Operation Code 04)

After receiving this command, the host adapter returns four bytes of data describing the host adapter firmware revision level. After completing the transfer of the four bytes of inbound data, the HACC interrupt is set indicating normal command completion. The bytes contain the following information:

Byte	Description	Value	Meaning
00	Board Identification (ID) The value in this byte allows software supported on both the PC AT and on the Micro Channel to distinguish the type of supporting host adapter.	00h	Board is an AHA-1540 with 16-Head BIOS
		30h ('0' ASCII)	Board is an AHA-1540 with 64-Head BIOS
		41h ('A' ASCII)	Board is an AHA-1540/1542, 64-Head BIOS
		42h ('B' ASCII)	Board is an AHA-1640, 64-Head BIOS
		43h ('C' ASCII)	Board is an AHA-1740A/1742A/1744
		All Others	Reserved

Continued

Byte	Description	Value	Meaning
01	Special Options Identification The value in this byte indicates what special options are supported on the AHA-1740A/1742A/1744 host adapter. Other host adapters use other values in this byte.	41h ('0' ASCII)	Board is standard model
		All Others	Reserved
02	Firmware Revision Level (First byte) This value indicates an ASCII value from 0-9, that indicates the first digit of the firmware base code revision installed in the AHA-1740A/1742A/1744.		
03	Firmware Revision Level (Second byte) This value indicates an ASCII value from 0-9, that indicates the second digit of the firmware base code revision installed in the AHA-1740A/1742A/1744.		

After completing this command, HACC will be asserted, indicating normal completion.

Enable Mailbox Out Available Interrupt (Operation Code 05)

The Enable Mailbox Out Available Interrupt command specifies that a Mailbox Out Available interrupt should be generated whenever a Mailbox Out entry has been cleared by the host adapter. One byte of outbound data is transmitted to indicate whether the interrupt should be enabled or disabled.

Byte 0 — Enable/Disable Parameter: The Enable/Disable parameter byte must be either 00h or 01h. If the Enable/Disable parameter byte is 00h, the Mailbox Out Available interrupt is not returned. If the Enable/Disable parameter byte is 01h, the Mailbox Out Available interrupt is returned as soon as a Mailbox Out has been cleared by the host adapter.

After completing this command, HACC will NOT be asserted to avoid generating additional interrupts. If the data byte is neither 00 nor 01, INVDCMD will be asserted indicating an invalid command. In this case, HACC will also be asserted.

The Mailbox Out Available interrupt is normally intended to be used by the host as an indicator that a Mailbox Out entry is available. This function should only be enabled if all Mailbox Out entries have been found full by the host. It should be disabled soon afterward. If used in other ways, the interrupt may generate a large number of relatively useless interrupt handling activities.

Set Selection Time out (Operation Code 06)

This command sets the SCSI selection time out value. The SCSI Selection time out value is used to determine whether a SCSI selection was successful. If the SCSI BSY signal is not returned within the specified time out value, the selection will be terminated and an appropriate error message posted with the returned CCB. This command expects four outbound data bytes to be provided as defined below:

Byte	Description
00	Enable/Disable Selection Time Out This parameter byte specifies whether the selection time out will be used. If the byte is set to 00h, no time out will be performed. If the byte is set to 01h, the time specified in bytes 02 and 03 will be used as the selection time out by the SCSI. The default value established by the reset process is 01h, indicating the time out is enabled.
01	Reserved (00) This byte must be zero.
02	Time Out Value (MSB) This two-byte value specifies the time in milliseconds that will be used for the selection time out. The default value is 250 milliseconds
03	Time Out Value (LSB) This two-byte value specifies the time in milliseconds that will be used for the selection time out. The default value is 250 milliseconds

After completing this command, HACC will be asserted, indicating normal completion. INVDCMD will be asserted if the data byte 0 is neither 00 nor 01 or if byte 1 is not zero, indicating an invalid command.

Set Bus On Time (Operation Code 07)

> Note
> This command is not used by the AHA-1740A/1742A/1744 but is supported in order to be compatible with software written for earlier host adapters, such as the AHA-1542B.

This command specifies the time that the host adapter spends on the bus when transferring data. The bus on duration is adjustable from 2 to 15 microseconds. The default setting is 11 microseconds. One data byte is passed out to the host adapter to indicate the bus on duration in microseconds.

Byte 0 Bus On Time (2 to 15 microsecondss)

After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 15. The valid range is 2 to 15 decimal. Due to the internal differences between the AHA-1740A/1742A/1744 and earlier host adapters, the data is not actually used but is saved and returned in the Return Setup Data command. The command is accepted only for compatibility.

Set Bus Off Time (Operation Code 08)

> Note
> This command is not used by the AHA-1740A/1742A/1744 but is supported in order to be compatible with software written for earlier host adapters, such as the AHA-1542B.

This command sets the time that the host adapter will spend off the bus during a data transfer. The bus off duration is adjustable from one to 64 microseconds. The default setting is four microseconds. After receiving this command, the host adapter expects one byte of data which specifies the bus off time in microseconds.

Byte 0 Bus Off Time (1 to 64 microseconds)

After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 64. The valid range is four to 64 decimal. The actual time implemented by the host adapter is rounded down to the next 4-microsecond step at or below the specified value. The minimum value is approximately one microsecond. Due to the internal differences between the AHA-1740A/1742A/1744 and earlier host adapters, the data is not actually used but is saved and returned in the Return Setup Data command. The command is accepted only for compatibility.

Set Transfer Speed (Operation Code 09)

> Note
> This command is not used by the AHA-1740A/1742A/1744 but is supported in order to be compatible with software written for earlier host adapters, such as the AHA-1542B.

This command adjusts the Bus Master DMA circuitry to a specified maximum AT bus transfer speed to and from the host memory. Several speeds may be selected by setting the jumper configuration as explained in the *System Configuration* section in Chapter Three, *Installation*. The selected jumper speeds are overridden if the Set Transfer Speed command is executed. The single data byte transmitted after the command byte either sets the read and write speed together, or establishes separate values for each. Appendix A gives the timings that result from the selected values. The default setting is the value set by the jumpers. The I/O Channel Ready signal automatically slows the system further if required by the host memory.

Data Byte 0	AT Bus Transfer Speed
00	5.0 MBytes/second
01	6.7 MBytes/second
02	8.0 MBytes/second
03	10 MBytes/second
04	5.7 MBytes/second

Data Byte 0	AT Bus Transfer Speed		
80-FFh	Bit		Custom Transfer Speed
	7	1	
	6-4	000	Read Pulse Width (ns) = 100
		001	Read Pulse Width (ns) = 150
		010	Read Pulse Width (ns) = 200
		011	Read Pulse Width (ns) = 250
		100	Read Pulse Width (ns) = 300
		101	Read Pulse Width (ns) = 350
		110	Read Pulse Width (ns) = 400
		111	Read Pulse Width (ns) = 450
	3	0	Strobe off time = 100ns
		1	Strobe off time = 150ns
	2-0	000	Write Pulse Width (ns) = 100
		001	Write Pulse Width (ns) = 150
		010	Write Pulse Width (ns) = 200
		011	Write Pulse Width (ns) = 250
		100	Write Pulse Width (ns) = 300
		101	Write Pulse Width (ns) = 350
		110	Write Pulse Width (ns) = 400
		111	Write Pulse Width (ns) = 450

Due to the internal differences between the AHA-1740A/1742A/1744 and earlier host adapters, the data is not actually used but is saved and returned in the Return Setup Data command. The command is accepted only for compatibility.

After completing this command, HACC is set indicating normal completion.

Return Installed Devices (Operation Code 0A)

This command returns information about which SCSI Targets and Logical Units (LUs) are installed on the SCSI bus. The host adapter issues the SCSI Test Unit Ready command to each target/LUN combination and reports the results using eight bytes of data returned through the Data In register. A bit having a value of one indicates that the associated LU is installed. Each byte is associated with the corresponding target. Each bit within a target byte is associated with a particular Logical Unit, bit 7 indicating the presence of LU 7 and so forth. The state of the target is analyzed using the SCSI Test UnitReady command, analyzing the returned data to determine if the addressed LU is available.

After receiving this command, the host adapter returns eight bytes of information which specify the installed configuration as shown below:

Byte	Configuration	Bit	
Byte 0	Target 0 Configuration	Bit 7	LU 7 Installed
		Bit 6	LU 6 Installed
		Bit 5	LU 5 Installed
		Bit 4	LU 4 Installed
		Bit 3	LU 3 Installed
		Bit 2	LU 2 Installed
		Bit 1	LU 1 Installed
		Bit 0	LU 0 Installed
Byte 1	Target 1 Configuration		
Byte 2	Target 2 Configuration		
Byte 3	Target 3 Configuration		
Byte 4	Target 4 Configuration		
Byte 5	Target 5 Configuration		
Byte 6	Target 6 Configuration		
Byte 7	Target 7 Configuration		

If, during the execution of this command, a target reports a status of busy, the host adapter will continue reissuing the command until either the drive reports not Busy, or one minute of time elapses. Commands will be reissued at 0.25-second intervals. The byte associated with the SCSI device identifier of the host adapter will always be zero. After completing the information transfer, the HACC bit will be set to indicate normal completion.

Return Configuration Data (Operation Code 0B)

The DMA arbitration priority, the Interrupt channel, and the SCSI ID of the adapter are returned by this command. The three bytes of information are returned in the following format:

Byte	Description	Bit	
0	DMA Arbitration Priority	Bit 7	Channel 7
		Bit 6	Channel 6
		Bit 5	Channel 5
		Bits 4-1	Reserved (0)
		Bit 0	Channel 0

Byte	Description	Bit	
1	Interrupt Channel	Bit 7	Reserved (0)
		Bit 6	Interrupt channel 15
		Bit 5	Interrupt channel 14
		Bit 4	Reserved (0)
		Bit 3	Interrupt channel 12
		Bit 2	Interrupt channel 11
		Bit 1	Interrupt channel 10
		Bit 0	Interrupt channel 9
Byte 2	SCSI Identifier	Bits 7-3	Reserved (0)
		Bits 2-0	Binary value of SCSI Identifier

After completing this command, HACC will be set indicating normal completion.

Enable Target Mode Command (Operation Code 0C)

A special host adapter command (0C) enables and disables target mode. The host adapter requires that two bytes of outbound information follow the command byte. The information bytes contain the following information:

Byte 0 — Enable/Disable Target Mode: This parameter specifies which operating modes the host adapter will use. If the byte is set to 00h, the AHA-1740A/1742A/1744 will operate only in Initiator Mode. If the byte is set to 01h, the host adapter will operate both as an initiator and as a processor-type target SCSI device. Any other value is invalid. The default value after a Hard Reset, Soft Reset, or Power-On Reset is 00h (Initiator only).

Byte 1 — Logical Unit Mask: This parameter byte contains an 8-bit mask indicating the Logical Units which will respond in Target Mode. Bit 7 corresponds to LU 7, and so forth. If the bit is one, the corresponding LU will be treated as installed. If the bit is zero, the LU will be treated as not installed.

If the AHA-1740A/1742A/1744 does not have the Target Mode feature installed, the host adapter will indicate an invalid host adapter command. If an attempt is made to change from target mode while there are still target mode CCBs being processed by the host adapter, the host adapter will post an invalid host adapter command indication.

If the command disables Target Mode, the Logical Unit Mask byte will be ignored. If the command enables Target Mode, the Logical Unit Mask byte must contain at least one bit, indicating the presence of at least one Logical Unit.

The SCSI Inquiry command will provide an indication to other initiators that the Logical Unit is installed or not installed in byte 1 of the returned inquiry data.

If target mode is not enabled, the host adapter will behave on the SCSI interface as if it were an ordinary SCSI initiator. Any attempt to select the host adapter will result in a SCSI selection time out. Most reset operations, including Soft Reset, Hard Reset, and Power-On Reset will return the AHA-1740A/1742A/1744 Target Mode to the disabled state. SCSI resets, generated either by the host or by other SCSI devices, will not change the previously established enabled or disabled state of Target Mode.

Return Setup Data (Operation Code 0D)

This command returns information describing the setup of the host adapter. The information returned reflects either the values supplied by previous host adapter commands or default values. The command is followed by an outbound data transfer and an inbound data transfer. The outbound transfer is a 1-byte parameter indicating the length of the required inbound data transfer. The inbound data transfer contains from zero to 255 bytes of information describing the setup of the host adapter. The inbound information normally transferred will be truncated or padded with zeros as necessary to transfer the requested number of bytes. The number of bytes normally transferred by the AHA-1740A/1742A/1744 is 17.

Byte	Description		Meaning
Outbound Data Byte			
00	Data In Length The number of data bytes requested can be from 0 to 255. A value of zero will be accepted and 256 bytes will be returned.	Bit 0	If this bit is zero, synchronous data transfer negotiation will not be initiated by the host adapter, but will be responded to if requested by an attached SCSI device. If the bit is one, synchronous data transfer negotiation will be initiated by the host adapter under those conditions which require such negotiation. The state is set from jumper J1.
		Bit 1	If this bit is zero, parity checking on inbound SCSI transfers has been disabled. If this bit is one, parity checking on inbound SCSI transfers is enabled. The state is set from jumper J1.
		Bit 2-7	Reserved (0)
Inbound Data Summary			
00	SDT and Parity Status		
01	Transfer Speed		This byte returns the value passed in to the host adapter by the Set Transfer Speed command (see *Set Transfer Speed* in this chapter)
02	Bus On Time		Indicates the Bus On Time in microseconds (see *Set Bus On Time* in this chapter))

Byte	Description		Meaning
03	Bus Off Time		Indicates the Bus Off Time specified by the Bus Off Time Value in microseconds (see *Set Bus Off Time* in this chapter)
04	Number of Mailboxes		The number of Mailboxes established by a previous Mailbox Initialization command will be returned in this byte. This number will be 00h if the Mailbox Initialization command has not yet been successfully completed.
05	Mailbox Address (MSB)		The base address of the Mailbox area established by a previous Mailbox Initialization command will be returned in these bytes. The most significant byte is byte 5. These bytes have no meaning if Mailbox Initialization has not yet been successfully completed.
06	Mailbox Address		
07	Mailbox Address (LSB)		
08-0F	Synchronous Transfer Agreements Returns information about the synchronous negotiation with Target 0. The byte will be 00H for the address of the host adapter.	Bit 7	Set to one if synchronous transfer has been negotiated. Set to zero negotiation has not occurred.
		Bits 6-4	These bits contain a value between 0 and 7 that defines the synchronous transfer period according to the following equation. Period = 200 + 50 (value) nanoseconds
		Bits 3-0	These bits contain the negotiated offset value. The value will normally be between 1 and 7. A value of 0 indicates asynchronous transfer.
09	Sync Neg, Target 1 Same as byte 8, for target 1		
0A	Sync Neg, Target 2 Same as byte 8, for target 2		
0B	Sync Neg, Target 3 Same as byte 8, for target 3		
0C	Sync Neg, Target 4 Same as byte 8, for target 4		
0D	Sync Neg, Target 5 Same as byte 8, for target 5		
0E	Sync Neg, Target 6 Same as byte 8, for target 6		
0F	Sync Neg, Target 7 Same as byte 8, for target 7		

Continued

Byte	Description		Meaning
10	Disconnection Option		Each bit corresponds to a SCSI device, e.g., bit 0 corresponds to the device at SCSI address 0. When set to one, the host adapter will prevent the SCSI device from disconnecting.
11-FF	Reserved (00)		

If the command completes normally, the HACC interrupt will be set to one. If the mailbox area has not been properly initialized, all 17 bytes are still requested by the host. If byte 4, the Number of Mailboxes, is zero, bytes 5-7 must be ignored.

Initialize SCSI Subsystem (Operation Code 10)

After receiving this command, the host adapter expects one byte from the host to configure the SCSI bus.

Enable/Disable Disconnect/Reconnect
Enable/Disable Synchronous Negotiation
Enable/Disable SCSI Bus Parity

Return Firmware Checksum (Operation Code 11)

After receiving this command, the host adapter passes two bytes to the host which reflect the checksum of the Standard Mode micromode. Note that this checksum is not marked on the board. The checksum on the EEPROM reflects an aggregate of the Enhanced Mode, Standard Mode and download utility microcodes.

Write Adapter Channel 2 Buffer (Operation Code 1A)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to will be transferred to the host adapter's channel 2 buffer using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the indicated buffer area to the host adapter, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Read Channel 2 Buffer command for host adapter diagnostics. The channel 2 buffer is used for transmission of all information except the actual data field between the host adapter and the host system.

Byte 0 Buffer area address, Most significant byte

Byte 1 Buffer area address

Byte 2 Buffer area address, Least significant byte

Read Adapter Channel 2 Buffer (Operation Code 1B)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to will be used as a buffer to receive 64 bytes of information transferred from the host adapter's channel 2 buffer to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the channel 2 buffer to the indicated host memory area, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Write Channel 2 Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte

Byte 1 Buffer area address

Byte 2 Buffer area address, Least significant byte

Write Adapter FIFO Buffer (Operation Code 1C)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to will be transferred to the host adapter's FIFO buffer using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the indicated buffer area to the host adapter, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Read Adapter FIFO Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte

Byte 1 Buffer area address

Byte 2 Buffer area address, Least significant byte

Read Adapter FIFO Buffer (Operation Code 1D)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to will be used as a buffer to receive 54 bytes of information transferred from the host adapter's FIFO to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the FIFO to the indicated buffer area, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Write Adapter FIFO Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte

Byte 1 Buffer area address

Byte 2 Buffer area address, Least significant byte

Echo Command Data (Operation Code 1F)

This command is used to test the Command/Data Out Port, the Data In Port, and the associated control bits in the other I/O Ports. After receiving this command, the host adapter expects one byte of outbound information to be transferred through the Command/Data Out Port. The host adapter then sends (Echos) the same data value back to the host through the Data In Port. After the host has read the data value provided on the Data In Port, the host adapter will generate the HACC interrupt to indicate normal command completion.

Byte 0 Out	Outbound echo value
Byte 0 In	Returned echo value

Adapter Diagnostic (Operation Code 20)

Unlike other Adaptec host adapters, this command does not cause the host adapter to perform its internal self-diagnostic. A host adapter Hard Reset is not executed, nor is a SCSI bus reset. The host adapter need not be reinitialized after this command before resuming normal operation. No actual diagnostics are performed, although internal flags are reset to the default state.

Set Host Adapter Options (Operation Code 21)

Unlike other Adaptec host adapters, this command does not provide the host a mechanism for specifying certain host adapter configuration options. Configuration parameters sent to the host adapter via a parameter list following the command OP Code are ignored.

Mailbox Overview

The AHA-1740A/1742A/1744 uses a mailbox architecture for task communication between the host and the host adapter when executing SCSI commands. This allows the host adapter to perform multithreaded operations with a minimum of host intervention. The mailboxes are located in main system memory. Each mailbox entry is four bytes long. At power-up, the host issues an initialization command to inform the host of the mailbox location. There are always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). The MBIs are located immediately after the MBOs. Initiator operations and target operations use the same mailboxes. Both initiator and target operations may be in process at the same time. A typical mailbox structure follows.

This command is provided only for compatibility. Refer to the section titled *Initialize SCSI Subsystem* for a discussion of operation code 10, which provides these functions.

Base Addr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBO 0
+20	Status	CCB 1 Pointer	MBO 1
+24	00	Free Entry	MBO 2
+28	00	Free Entry	MBO 3

In this example, there are four MBOs and four MBIs. The Mailbox Count in the Mailbox Initialization command was set to four. The base address is the address specified by the Mailbox Address field.

> Note
> The Adaptec BIOS initializes the AT DMA controller to accommodate Bus Master DMA. If the host adapter BIOS is removed or disabled, the host DMA controller must be initialized, via software, for Bus Master DMA operation. See the section titled *Description of Operation*.

Mailbox Out Definition

The first byte of each MBO contains the mailbox status byte. The remaining three bytes contain an address pointer to the first byte of a Command Control Block (CCB). The CCB provides additional task control information. An MBO is free if the first byte is zero. The host can make an entry in any free MBO and indicate that it is filled out or completed by placing the proper MBO command in the first byte of the MBO. After the MBO has been examined by the host adapter and all relevant information obtained by the host adapter, the host adapter sets the MBO command byte back to zero to allow the host to fill it again. For a multitasking operating system, it is desirable that the number of mailboxes be sufficient to allow at least one mailbox for each active independent task or activity.

The MBO format is described in detail below:

Byte	Description	Value	Meaning
0	MBO Command This byte specifies the state of the MBO entry.	00h	Mailbox Out is free
		01h	SCSI or Host Adapter command is to be started. CCB pointer indicates location of CCB to be processed.
		02h	SCSI or Host Adapter command is to be aborted. CCB pointer indicates location of CCB to be terminated.
1	CCB Pointer (MSB)		
2	CCB Pointer		
3	CCB Pointer (LSB)		

For values of byte 0 other than those listed above, the host adapter will simply set byte 0 to 00h and ignore the Mailbox Out (MBO) entry. No corresponding Mailbox In will be generated.

The use of Mailbox Out (MBO) entries to pass pointers to CCBs is identical for target and initiator modes. The appropriate target mode CCB may be prepared early and posted to the host adapter in preparation for an operation that is expected to happen. If a SCSI operation occurs before the CCB is prepared, the host adapter processes as much of the transaction as possible, then requests a CCB from the host through the MBI. The host is fully responsible for preparing the correct CCB from the information provided through the MBI.

In Target Mode, one CCB may be presented for each unique combination of LUN, Initiator, and direction. If a second CCB to the same LUN and initiator with the same direction bit is sent to the AHA-1740A/1742A/1744, the CCB will be returned with a host status of 19h, Duplicate CCB Received.

Initiator-type CCBs may be queued for a LUN and target. The host adapter will always search for new MBO entries in a round-robin order, beginning with the entry after the last MBO entry that was processed. By always placing the MBO entries in the MBO area consecutively, the host can assure that the SCSI commands will be started with a minimum scan overhead. Initiator CCB queuing must be used with caution, since under some circumstances it is possible for CCBs to be executed out of order.

If the Mailbox Out Available interrupt is enabled by execution of adapter command 05 (Enable Mailbox Out Available Interrupt), the host adapter will take one of the following actions after each MBO entry is freed by the host adapter:

1. If the Any Interrupt bit in the Interrupt Flag Port is zero, indicating that there are no interrupts pending, the host adapter will set the Mailbox Out Available Interrupt and the Any Interrupt bit and indicate a hardware interrupt to the host.

2. If the Mailbox Out Available interrupt has been set to one by the previous clearing of a Mailbox Out entry and the interrupt has not yet been cleared by the host, the

host adapter will not change the MBOA interrupt bit and will continue to scan for other stored MBO entries.

3. If interrupts other than the Mailbox Out Available interrupt are pending, the host adapter will wait for the pending interrupts to be cleared before setting the Mailbox Out Available Interrupt. This guarantees that the MBO Available interrupt will not be cleared accidentally by clearing another interrupt.

Mailbox In Definition

The Mailbox In entries are used to pass completion information concerning a task from the host adapter to the host. In addition, requests for Target Mode CCBs are passed to the host using MBI entries. The first byte of each MBI contains the MBI Status byte, summarizing the type of information being passed from the host adapter to the host. The remaining three bytes contain specialized information that provides more detail about the information. In the case of a CCB Completed MBI, the bytes contain a pointer to the completed CCB. In the case of a CCB Required MBI, the bytes contain the information necessary for the host to prepare an appropriate CCB. Only those MBIs with an MBI status that is nonzero have information for the host. When the host returns the MBI status byte to zero, the MBI Free state, the host adapter is allowed to place a new set of information in the MBI entry.

When a SCSI command completes or if a new CCB is required, the host adapter scans the first byte of an MBI entry to find a free mailbox. If one is found, the host adapter will update the MBI's status byte with a nonzero value and update the following bytes with the appropriate required pointers or parameters. The valid MBI formats are defined below:

Mailbox In Format for CCB Complete

Byte	Description	Value	Meaning
0	MBI Status This byte specifies the state of the MBI entry.	00h	Mailbox In is free
		01h	CCB completed without error. CCB pointer indicates location of successfully completed CCB.
		02h	CCB aborted by host. CCB pointer indicates location of CCB that was aborted.
		03h	Aborted CCB not found. CCB pointer indicates the supposed location of the CCB that was to have been aborted. It is likely that the CCB was already presented to the host before the Abort CCB MBO entry was completed.
		04h	CCB Completed with Error. The CCB fields indicate the details of the error condition. This code allows normal CCB completion to be processed without bothering to examine the completion codes in the CCB.
1	CCB Pointer (MSB)		
2	CCB Pointer		
3	CCB Pointer (LSB)		

Mailbox In Format for CCB Required

Byte	Definition	Value	Meaning
0	MBI Status This byte specifies the state of the MBI entry.	10H	SCSI Target command received with no CCB available. The host must prepare an appropriate CCB and place it in the MBO to complete the SCSI command. The remaining three bytes of the MBI specify the information necessary to prepare a SCSI command.
1	Initiator and LUN	Bits 7-5	Binary address of initiator that selected the host adapter in Target Mode.
		Bit 4	The SCSI Target command received was a Receive command. A CCB must be prepared to transmit data to the Initiator.

Byte	Definition	Value	Meaning
		Bit 3	The SCSI Target command received was a Send command. A CCB must be prepared to transmit data from the Initiator.
		Bits 2-0	Binary address of the logical unit of the Target Mode host adapter that was addressed by the Initiator.
2-3	Data Length		The high-order two bytes of the data length specified in the Send or the Recieve command. A CCB must be prepared to transmit this amount of data plus up to 256 more bytes. It is assumed that the data fields are self-defining or of a known length in such protocols.

The CCB Required Mailbox In entries are only generated when a command has been received by the host adapter in Target Mode. For the CCB Required Mailbox In entries, byte 0 takes on a distinctive value of 10h, indicating the MBI entry is filled and the MBI entry is being presented to request a CCB appropriate to service a SCSI transaction for which no CCB was available. The host adapter will have disconnected on the SCSI after receiving the initiator and LU addresses and after having received either a SCSI Send or a Receive command. If the LU address is enabled by the logical unit mask, the MBI will provide the addresses in bits 7-5 and bits 2-0 and will indicate by setting either bit 3 or bit 4 that a SCSI Send or Receive command was accepted from the initiator. The host system is then expected to prepare a CCB suitable for processing the Send or Receive command. The information in bytes 2 and 3 is a copy of bytes 2 and 3 of the Send or Receive command CDB. This provides the host an approximation of the length of the requested data transfer. This length is used by the host to allocate the correct amount of buffer to accept data in a Send command or to control the maximum amount of data that can be transferred in a Receive command. If the LU address received is disabled, no MBI will be presented and a check condition will be posted to the Initiator. A subsequent Request Sense command will recover an invalid LUN error indication.

After each Mailbox In entry is stored by the host adapter, it will indicate that Mailbox In scanning must be performed in the following manner:

1. If the Any Interrupt bit is not set to one in the Interrupt Flag port, indicating that no interrupts are pending, the host adapter will set the Mailbox In Full interrupt bit, the Any Interrupt bit, and raise the hardware interrupt line to indicate that there is at least one Mailbox In entry to be examined by the host system.

2. If the Mailbox In Full interrupt bit has already been set to indicate that an entry was made in the Mailbox In area and if that interrupt has not yet been cleared by the host, no further notification is provided by the host adapter.

3. If interrupts other than the Mailbox In Full interrupt are pending, the host adapter will wait for all pending interrupts to be cleared before setting the Mailbox In Full interrupt.

Note

Careful host Target Mode software design is necessary to prevent ambiguity in the notification process. If a CCB was just prepared but the MBO has not yet been searched by the host adapter at the time the MBI entry is made to the host, the host may choose to examine the MBI entry and not act on it, having already provided the needed CCB. The host should also examine the entire MBI space to be sure that a previously supplied CCB which should have been able to service the notification MBI entry was not already used for a previous operation that had been posted by the host adapter but not yet serviced by the host. Proper care in host system design will prevent these overlapping operations from becoming a problem.

Command Block Definition

The CCB specifies detailed information about a SCSI command. The format of a CCB is shown below. Each of the fields is separately explained following the table.

Command Control Block Format

Byte	Description	Value	Meaning
0	Command Control Block Operation Code	00h	SCSI Initiator command
		01h	Target Mode command
		02h	SCSI Initiator command with Scatter/Gather
		03h	SCSI Initiator command, residual data length returned
		04h	SCSI Initiator command with Scatter/Gather, residual data length returned
		81h	Bus Device Reset
1	Address and Direction Control	Bits 7-5	CCB OP Code = 00, 02, 03, 04: SCSI Target Id CCB OP Code = 01: SCSI Initiator Id
		Bit 4	Outbound data transfer, length is checked.
		Bit 3	Inbound data transfer, length is checked.
		Bit 2-0	Logical Unit Number
2	SCSI Command Length		
3	Request Sense Allocation Length/Disable Auto Sense		
4-6	Data Length (Byte 4 most significant)		

Byte	Description	Value	Meaning
7-9	Data Pointer (Byte 7 most significant)		
10-12	Link Pointer (Byte 10 most significant)		
13	Command Linking Identifier		
14	Host Adapter Status (HASTAT)		
15	Target Device Status (TARSTAT)		
16-17	Reserved (00)		
18-n	SCSI Command Descriptor Block (Length specified by byte 2)		
n-m	Reserved for Request Sense information bytes (Length of reserved space in byte 3)		

The standard format of the Command Control Block is shown in the following diagram:

Byte 0	Command Control Block Opcode			
1	Tar/Init	Data Out	Data In	LUN
2	SCSI Command Length = m			
3	equest Sense Allocation			
4	Data Length (MSB, MID, LSB)			
7	Data Pointer (MSB, MID, LSB)			
10	Link Pointer (MSB, MID, LSB)			
13	Command Link ID			
14	Host Status			
15	Target Status			
16	Reserved			
17	Reserved			
18	SCSI Command Bytes (m Bytes)			
18+m	Allocated for Sense Data (n Bytes)			

The bytes of the CCB are defined further below:

Byte 0: Command Control Block Operation Codes

The AHA-1740A/1742A/1744 supports six CCB operation codes. The valid command values are shown below:

00h	SCSI Initiator Command Control Block
01h	SCSI Target Command Control Block
02h	SCSI Initiator Command Control Block with Scatter/Gather
03h	SCSI Initiator Command, residual data length returned
04h	SCSI Initiator Command with Scatter/Gather, residual data length returned
81h	SCSI Bus Device Reset

If the operation code value is 00h or 03h, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed Target /LUN. The other fields of the CCB support the required initiator functions of the

AHA-1740A/1742A/1744. Operation codes 00h and 03h differ only in the updating of Bytes 4, 5, and 6, following completion of the command.

If the operation code value is 01h, the CCB is intended to service a Send or Receive command sent to the host adapter as a target from another initiator. The values in the other fields are used to service the Target Mode operation. If an operation code of 01h is specified to a host adapter that has not had its Target Mode enabled, the host adapter returns a host status indication of 18h, Invalid CCB Parameter.

If the operation code value is 02h or 04h, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed Target/LUN. The definition of the data length and the data pointer is modified to support the Scatter/Gather function. Operation codes 02h and 04h differ only in the updating of Bytes 4, 5, and 6 following the completion of the command.

If the value is 81h, a Bus Device Reset message will be sent to the addressed target. This command forces the host adapter to abort all outstanding tasks against the selected target. All remaining CCB bytes are ignored. The host adapter will generate a Bus Device Reset message out to the specified target.

Any other command value generates a Host Adapter Detected Error (Host Status byte of 16h).

Byte 1: Address and Control Byte

This byte identifies the address of the devices that will be serviced and provides information about the expected direction of data flow.

If the CCB is an initiator CCB, this byte identifies the target SCSI device in bits 7, 6, and 5. If the CCB is a target CCB, the byte identifies the initiator which the CCB will serve.

Bits 4 and 3 are set to determine the direction of data transfer. For an initiator CCB, the direction of data transfer will be established by the SCSI command being executed independent of the value of bits 3 and 4. For a target CCB, if neither bit is set or both bits are set, the CCB will be returned with an indication of Invalid CCB Parameters (18h) in the Host Status field, since each Target CCB must be identified as to whether it will service a Send or a Receive command. If both bits are set for an initiator CCB, the command must perform no data transfer. If only bit 3 is active, the data transfer will be to the host adapter and from the external SCSI device. If the CCB is a target CCB, the data transfer will be required to be a Data Out phase, while if the CCB is an initiator CCB, the data transfer will be required to be a Data In phase. If only bit 4 is active, the data transfer will be from the host adapter and to the external SCSI device. If the CCB is a target CCB, the data transfer must be a Data In phase, while if the CCB is an initiator CCB, the data transfer will be a Data Out phase.

If bits 3 or 4 are set for an initiator CCB, the data length will be checked. If the amount of data transferred exceeds the specified amount, the CCB Host Status field will contain an indication of Data Over/Under Run (12h). For a processor Target

Mode CCB, the handling of incorrect lengths is described in *Incorrect Length Management for Target Mode Operation* in Chapter Nine, *SCSI Features*.

If a data underrun/overrun condition occurs for an operation that accesses the drive's media (Read/Write, Extended Read/Write, Write and Verify) and the direction bits are set to zero, the host adapter will complete the operation without error. However, some or all of the data specified by the host may not be transferred.

> CAUTION
> The appropriate direction bit should be set for all operations that access the drive's media.

This enables the host adapter to check the length of the data transfer and if a data underrun/overrun condition occurs, the CCB will be returned with an indication of Data Underrun/Overrun (12h) in the Host Status field. For operations that do not access the drive's media, the direction bits should be set to zero unless transfer length checking is desired. Setting both direction bits to one should be used only when no data transfer is expected or suppression of data transfer is desired for Read operations.

If the CCB is an initiator CCB, bits 2, 1, and 0 define the target Logical Unit which will be addressed. If the target accepts an Identify message out, the value in bits 2, 1, and 0 will be provided in the LUN field of the message byte. The LUN field in the SCSI Command Descriptor Block (CDB) is expected to be zero. If the target does not accept an Identify message out, the LUN field in the SCSI CDB must contain the correct Logical Unit address. SCSI devices with conformance level 2, including Common Command Set (CCS) disk drives and all SCSI-2 devices will always accept the Identify message out. The few SCSI devices not meeting those requirements must be examined on a case-by-case basis to determine whether the logical unit address should be placed in CCB Byte 1 or in the CDB.

Byte 2: SCSI Command Length

This byte establishes the length, in bytes, of the SCSI Command Descriptor Block.

Byte 3: Request Sense Allocation Length

When a SCSI device terminates an operation with Check Condition status, it means that the device has error or status information as a result of execution of the operation. The SCSI specification indicates that a Request Sense command must be executed before any other command is executed in order for the host initiator to be sure of obtaining the error information. Since the AHA-1740A/1742A/1744 host adapter has the capability of queuing commands for execution, the host adapter itself must take charge of generating the Request Sense command. The automatic generation of Request Sense is inconvenient for some specialized operating systems, so the function can be disabled by installation of a jumper in J9 (see the section titled *MCS Configuration* in Chapter Three, *Installation*). If the jumper is not installed, the function can also be disabled by specifying a value of 01h for the Request Sense Allocation Length.

This byte indicates the length, in bytes, of the area reserved for information that may be obtained by a Request Sense command. A value of 00h indicates that an allocation length of 14 bytes is to be used, sufficient to capture the sense key and error code of all normal extended sense type devices. A value of 01h requests that no automatic Request Sense be executed. The values from 02h to 07h are reserved. Values from 08h to FFh are valid allocation lengths. The value is used to notify the host adapter that the specified number of bytes have been reserved at the end of the CCB to receive possible Request Sense data bytes. The Request Sense also uses the indicated allocation length as its byte count in the Command Descriptor Block generated by the host adapter.

If an operation that treats the AHA-1740A/1742A/1744 as a Target Mode device fails and presents a check condition status byte, the Initiator should return a Request Sense command. The AHA-1740A/1742A/1744 will return appropriate sense information in response to the command. If the command that originally failed was a Send or a Receive command, the same Request Sense information bytes that will later be sent to the initiator are also sent to the host when the CCB is returned. The sense information is placed in the specified request sense allocation area with a length not exceeding the request sense allocation length.

Bytes 4, 5, 6: Data Length

These bytes determine the length, in bytes, of the data transfer. CCB host adapter error 12h is posted if a data overrun occurs.

If the CCB specifies a Scatter/Gather operation, the Data Length field contains the total number of bytes in the Data Segment List.

If the operation code value is 00h or 02h, these bytes remain unchanged upon completion of the command. If the operation code value is 01h, these bytes will be set by the host adapter upon completion of the command to the number of bytes actually transferred. If the operation code value is 03h or 04h, these bytes will be set by the host adapter upon completion of the command to the difference between the original data length, as specified by the host, and the actual number of bytes transferred across the SCSI bus. In the event of data overrun, these bytes will be set to zero. For operation code 04h, the original data length is the sum of all segment data lengths.

Bytes 7, 8, 9 : Data Pointer

These bytes specify the real address of the first byte of the data area to be used during the data phase of the SCSI command.

If the CCB specifies a Scatter/Gather operation, the Data Pointer field contains the pointer to the first byte of the data segment list.

Bytes 10, 11, 12: Link Pointer

These bytes are used when a SCSI command contains a Link or Link With Flag bit in the command. When a linked command is completed, the host adapter will use the contents of this field as a pointer to the next CCB to execute. If the Linked Flag bit is

set, an interrupt will be generated before the next command is started. A completed CCB is always reported back in an MBI, but MBIF interrupts are only reported if the linked set of commands is finished or if a Link with Flag message is presented. There must be enough MBI entries to receive the entire set of linked commands.

Target Mode does not support the linking function.

Byte 13 : Command Link ID

This byte is used in conjunction with linked commands. It is set by the host to identify commands in a command chain.

Linking is not supported in Target Mode.

Byte 14 : Host Status

This byte is used to report the host adapter status (HASTAT) ans defined as follows:

Value	Definition
00h	No host adapter detected error The CCB was completed normally.
11h	Selection time out The initiator selection or target reselection was not complete within the set SCSI selection time out period.
12h	Data Overrun/Underrun The target attempted to transfer more data than was allocated by the Data Length field or the sum of the Scatter/Gather Data Length fields
13h	Unexpected bus free The target dropped the SCSI BSY at an unexpected time.
14h	Target bus phase sequence failure An invalid bus phase or bus phase sequence was requested by the target. The host adapter will generate a SCSI reset condition, notifying the host with a SCRD interrupt.
16h	Invalid CCB Operation Code The first byte of the CCB was invalid. This usually indicates a software failure.
17h	Linked CCB does not have the same LUN A subsequent CCB of a set of linked CCBs does not specify the same logical unit number as the first.
18h	Invalid Target Direction received from Host The direction of a Target Mode CCB was invalid.
19h	Duplicate CCB Received in Target Mode More than one CCB was received to service data transfer between the same target LUN and initiator SCSI ID in the same direction.
1Ah	Invalid CCB or Segment List Parameter A segment list with a zero length segment or invalid segment list boundaries was received. A CCB parameter was invalid.

Byte 15: Target Status

For an initiator CCB, this byte is used to return the SCSI status byte sent to the host adapter from the initiator. If a SCSI command returns with Busy status, the normal recovery process is to execute the command again. The AHA-1740A/1742A/1744 takes that burden off the host and periodically restarts the command automatically until the command completes with a status other than busy.

For a Target Mode CCB, this byte is used to indicate to the host what status the host adapter returned to the initiator.

Target Status may have the following values in target mode:

00h	Good Status
02h	Check Status (See Request Sense byte area)
08h	LUN Busy

Byte 16: Reserved (must be 0)

Byte 17: Reserved (must be 0)

Byte 18: n: SCSI Command Descriptor Block

This field holds the SCSI Command Descriptor Block (CDB) as described in the SCSI specification. The length of this command is described in byte 02. For initiator mode CCBs, the CDB provided by the host is transmitted to the target. For Target Mode CCBs, the CDB provided from the initiator is returned to the host in this space.

Byte 18+n - 18+n+m : Allocated for Sense Data

If a check status condition is detected by the AHA-1740A/1742A/1744 as it completes an operation on the SCSI bus, the host adapter automatically executes a Request Sense command with the data length specified by request sense allocation length. The actual bytes returned, up to the maximum indicated by the request sense allocation length, are placed in the area allocated for sense data. If the request sense allocation length was 01h, no Request Sense command is executed.

If the Request Sense command completed without a check status condition, the target status will be set to check status, and the host status will be set to 00h. If the Request Sense command completed with check status, the target status will be set to check status, and the host status will be set to 14h.

If a check condition is detected by the AHA-1740A/1742A/1744 while it is operating in processor Target Mode, the same information that will later be recovered by the initiator that received the check status is also placed in the area allocated for sense data so that the host processor is also aware of the failure.

Scatter/Gather List Definition

Using the normal CCB operation codes of 00h and 01h (SCSI Initiator and SCSI Target CCBs), the CCB itself contains a pointer to the first byte of a contiguous area of data of a specified length. The direction of transfer with respect to the data area and the checking of the length of the data transfer to the data area are both managed by the AHA-1740A/1742A/1744 according to the requirements of the particular mode and control bit set-up.

Using the Scatter/Gather Operation Code of 02h or 04h, the CCB instead contains a pointer to a list of data segments and an indication of the length of the list of data segments. The data segment list contains pointers to the actual location in host memory of the data segments to be transferred as well as a precise indication of the length of each data segment. Each data segment list entry contains a 3-byte pointer to the location of a data segment and 3-byte length indicator telling how long that particular data segment shall be. The data segment list is arranged in the order in which data will be gathered or distributed, the first pointer in the list being used first.

A typical data segment list is shown in the following table. The data segment list describes the distribution of 4096 bytes distributed in four separate locations within the memory. The beginning of the data segment list is indicated by the data segment list pointer. The length of the data segment list (24 bytes) will be contained in the data segment list length field of the CCB.

	3 Bytes	3 Bytes
	(MSB) (LSB)	(MSB) (LSB)
Data Segment List Pointer	Segment 0 L=1024	Data Segment 0 Pointer
	Segment 1 L=2	Data Segment 1 Pointer
	Segment 2 L=2046	Data Segment 2 Pointer
	Segment 3 L=1024	Data Segment 3 Pointer

A data segment list can have from one to 17 segments. A list with zero segments or a list with more than 17 segments causes an invalid segment list error to be posted in the Host Status field.

The AHA-1740A/1742A/1744 has certain constraints in the data segment address boundaries and lengths that are allowed. If these boundaries are violated, an invalid segment list error will be posted in the Host Status field of the CCB. The simplest way to assure that these boundaries are not violated is to require all boundaries between segments to be on even word boundaries. The first segment may begin on any boundary and the last segment may end on any boundary. All segments but the first and last should have even byte counts.

The actual boundary limitation is somewhat less restrictive. If the binary values of the starting address of a segment, the byte count of that segment, and the starting address of the next segment are all exclusive OR'd together, and the result of that exclusive OR is an even number, the boundary between those two segments is valid. Another way to express the limitation is to require that the ending boundary of one segment must be the same as the beginning boundary of the next segment. If a segment ends on a word boundary, the next segment must begin on a word boundary. Similarly, if a segment ends on an odd-byte boundary, the next segment must begin on an odd-byte boundary.

Description of Operation

This section describes the interface operations required to invoke the desired SCSI behavior. The AHA-1740A/1742A/1744 must be properly initialized before any of these operations can be performed.

After system initialization is done, the I/O Command Port initialization commands must be executed. The Mailbox Initialization command must be executed to assign the mailbox area. The Enable Target Mode command may optionally be executed if Target Mode is to be allowed.

Execution of Initiator Mode Operations

To begin an Initiator Mode SCSI command, the host first allocates a data buffer area. A CCB is then created to perform the desired operation to the correct peripheral device and a pointer to the data buffer area is placed in the CCB. Once the CCB is completely defined, the host places a pointer to the CCB in an empty MBO location, places an MBO full status in the MBO status byte, and transmits a Start SCSI command to the I/O command port. If it is not already scanning the MBO for an active MBO entry, the Start SCSI command to the I/O port causes the host adapter to begin scanning for such an entry.

After finding an active MBO entry, the AHA-1740A/1742A/1744 copies the MBO Command field contents and CCB pointer into its internal RAM and clears the MBO Command byte, freeing the mailbox. Up to 16 initiator CCBs and 16 target CCBs can be stored in the host adapter's internal RAM concurrently. The AHA-1740A/1742A/1744 maximizes the SCSI bus utilization by starting the next available CCB as soon as the bus is free. Disconnection and reconnection on the bus are automatically taken care of by the AHA-1740A/1742A/1744. As the host adapter starts the SCSI operation, it will first determine if the addressed target/LUN is busy. If the target/LUN is busy, the command will be placed in the task queue to be tried again later.

Commands are removed from the queue in the order they were received, establishing a First In First Out (FIFO) command execution order. Of course, the order of task completion may vary due to the different amounts of time required to process and complete different commands. If the target/LUN is not busy, the new command is started at the next bus free phase. If Busy status is received by the AHA-1740A/1742A/1744, the CCB is placed at the end of the FIFO queue to be restarted later.

If a check condition status is received from the target, the AHA-1740A/1742A/1744 will issue a Request Sense command to get the sense data. The sense data is stored in the CCB after the SCSI command data. The driver software must reserve the allocated number of bytes at the end of the CCB to hold the sense data which is returned as result of a receiving a check status. Automatic request sense can be optionally disabled by jumpers or by using the CCB.

If the MBO command is to abort a SCSI command, the host adapter first searches the active and queued CCBs. If the CCB is found, the task is aborted at the earliest possible moment and an MBI entry is made to indicate that the CCBs execution was successfully terminated. If the CCB is not found among the active or queued CCBs, the AHA-1740A/1742A/1744 completes the command and reports that fact in the MBI Status byte. The CCB may not be found because it has previously been aborted, because an intervening reset occurred, or because the CCB was already finished normally and returned.

The AHA-1740A/1742A/1744 scans the MBOs in a round-robin fashion. This is to ensure that all of the mailboxes will be scanned with equal probability. A host can minimize the AHA-1740A/1742A/1744 MBO scan time by using MBOs sequentially.

When executing a Start SCSI command, the AHA-1740A/1742A/1744 does not verify that the new CCB resides in an unused memory area. Therefore, the host must not reuse a CCB location until it has been returned through a Mailbox In entry and the host has examined all the pertinent information in the CCB. CCB addresses are used by the AHA-1740A/1742A/1744 as task identifiers.

Execution of Target Mode Operations With a Prepared CCB

Typical target operation is managed in the following way by the host software. After power-on initialization is complete, the host sends an Enable Target Mode command to the host adapter to enable processor Target Mode. After that, the host, from previous configuration knowledge, generates a pair of CCBs for each likely initiator and for each LUN supported by the host. One CCB is for outbound data from the initiator using the Send command, while the other is for inbound data from the target to the initiator using the Receive command. The Send command CCB defines a data buffer for the expected network-type command from the initiator. The Receive command CCB defines a set of data which is known and expected by the initiator, typically a welcome or configuration-type message packet. The host adapter tests to be sure that duplicate CCBs are not provided by the host.

As the initiator finishes its initialization procedure, it requests availability and configuration information using the Test Unit Ready, Request Sense, and Inquiry commands. Finally, it may choose to address Send and Receive commands to the targets it has located to transmit or request information packets.

When the initiator executes a Send or a Receive command, the target accepts the selection on the SCSI bus, accepts the command from the initiator, and executes the proper data transfer to or from the area specified by the proper CCB. When all SCSI activity is finished successfully, the CCB is posted back to the host program by an entry in the MBI. The host adapter updates the CCB byte count and CDB field contents to correctly reflect the operation performed. The host is notified that there is an entry

in the MBI by an interrupt from the host adapter. The host then prepares a new CCB to control the target's next activity expected from the initiator.

Execution of Target Mode Operations Without a Prepared CCB

Alternatively, the processor-type device may be addressed by an initiator when no CCB has yet been prepared for use by the host adapter. If the host adapter command enabling target mode has not yet been executed, the host adapter will act like any initiator. It will not accept any selection sequence and any attempts to select it by its target ID will cause the initiator to detect a selection time out.

If the host adapter has been enabled as a processor target by a host adapter command, any selection to the host adapter's target address will be accepted. The availability commands and identification commands (Test Unit Ready, Request Sense, and Inquiry) will be executed completely and normally. If a Send or Receive command is received and if a CCB is not active, either because the host has not completed its program initialization or because the host has not finished analyzing the results of previous data transfers and has not generated a new CCB, the processor target will accept the selection, obtain the Identify Message Out to determine what logical unit has been selected, input the CDB from the SCSI, and then disconnect. The CDB will be partially interpreted so that the proper MBI can be generated to notify the host that a new CCB with a certain address, direction, and data length must be generated. When the new CCB is passed to the host adapter by an MBO entry, the CCB is filled up with the command information, the SCSI is reconnected, and the command is completed as described above.

DMA Channel Initialization (with Host Adapter BIOS Disabled)

The DMA circuitry must be set to a special state to allow the Bus Master operation of the AHA-1740A/1742A/1744 to operate correctly. This state is normally established by the BIOS during initialization so that no other activity is required. If a DMA channel other than the default channel is being used or if the DMA channel is manipulated by other programs, the circuitry must be initialized in the following way before the AHA-1740A/1742A/1744 can be used.

For the DMA channel being used, two bytes of data must be written to the DMA controller port specified to initialize the host DMA controller for Bus Master DMA operation. The following table specifies these values in hex.

DMA Channel	DMA Controller Port	Data
0	0B 0A	0C 00
5	D6 D4	C1 01
6	D6 D4	C2 02
7	D6 D4	C3 03

Interrupt Initialization

This setup procedure is normally completed by the BIOS during initialization so that no other activity is required. If modifications to the interrupt handler are required, this information together with the programming information provided by the host system should be sufficient to properly set up the interrupt vectors.

The host adapter will drive one of several interrupts in the AT system. The particular interrupt used must be set up on power-up initialization and be properly managed during usage. A summary of the AT interrupts of interest to the host adapter driver along with their corresponding vector locations follow. All of these interrupts are handled by a slave interrupt controller. The master controller handles all system interrupts such as keyboard, timer, etc. and is assumed to be correctly initialized to allow interrupts by the slave controller. Upon receiving an interrupt, the processor will be vectored to the contents of the corresponding vector location.

Hardware Interrupt	Software Interrupt Vector Location (hex)
IRQ 9	Int 71
IRQ 10	Int 72
IRQ 11	Int 73
IRQ 12	Int 74
IRQ 14	Int 76
IRQ 15	Int 77

> Note
> IRQ 13 is not one that is available on this board.

The interrupt is initialized by clearing the corresponding interrupt mask bit in the slave controller. The mask register is a read/write register, and only the bit of interest should be cleared. The port address is A1h, and bit definitions follow:

Interrupt Mask Bit Definition (Port Address A1h)	
Bit	**Interrupt**
0	Int 8
1	Int 9
2	Int 10
3	Int 11
4	Int 12
5	Int 13
6	Int 14
7	Int 15

❑

Chapter Six

Enhanced Mode Firmware Description

Introduction

The Enhanced mode is an interface architecture which allows the AHA-1740A/1742A/1744 to take full advantage of the EISA bus facilities. It utilizes a distinct hardware interface control logic, known as the configuration chip. This permits features such as full 32-bit addressing and the entire EISA register set to be used. This mode is not compatible with versions of the ASW-1400 series of software managers before version 3.0. In order to use the Enhanced Mode, the AHA-1740A/1742A/1744 must be correctly reconfigured by using the configuration utility described in Chapter Three, *Installation*. The AHA-1740A/1742A/1744 is not capable of simultaneous operation in Standard and Enhanced Modes.

Operations using the Enhanced Mode utilize a mailbox interface which is substantially different from the Standard Mode. The principal difference is the use of a single mailbox structure which is serviced at a rate that prevents overwriting. The mailbox structure is described in detail in the section on *EISA Expansion Identifiers* in Chapter Four, *Hardware Functional Description*. The components of the mailbox are:

zCD0	Mailbox Out Pointer
zCD1	Mailbox Out Pointer
zCD2	Mailbox Out Pointer
zCD3	Mailbox Out Pointer
zCD4	Attention Register
zCD5	Enhanced Mode Control Register
zCD6	Interrupt Status Register
zCD7	Enhanced Mode Status Register
zCD8	Mailbox In Pointer
zCD9	Mailbox In Pointer
zCDA	Mailbox In Pointer
zCDB	Mailbox In Pointer

Operations using the mailbox begins with the host assembling an Enhanced Control Block (ECB) in memory. The host then stores the pointer to the ECB in the Mailbox Out, provided that bit 2 of the SCD7 Status register (MBO empty) is true. Due to the speed with which the AHA-1740A/1742A/1744 services the mailbox, the MBO will almost always be empty.

The host then checks the busy bit (Bit 0) in zCD7 to ensure that the AHA-1740A/1742A/1744 has serviced any previous requests placed in the Attention register. If the bit is false, which will almost always be the case, the host writes a byte into the attention register with the format:

Command	SCSI ID

The command will be either a Start command (4), Immediate command (1), or Abort command (5). Writing to this register causes an internal interrupt to the host adapter, which will then examine the command and the SCSI ID for which it is destined and then use the MBO to access the ECB associated with the command. Both MBO empty and busy are cleared in zCD7 to allow other commands to be sent.

While the board is busy executing the command, the host may monitor zCD6 Interrupt Status register to look for completion of the command. When any command completes, this register will be loaded with

Completion Code	SCSI ID

and the MBI (zCD8-B) loaded with pointers to any host adapter data in the ECB area of memory. At the same time, the Interrupt Pending bit is set in zCD7. This is reset when the host writes the Clear EISA Interrupt bit in the control register zCD5.

Multitasking is achieved by setting up multiple commands through the mailbox before the first has been completed. The microcode maintains control of up to 64 commands executing simultaneously in the host adapter.

Control Block

The control block is a 48-byte structure created and maintained in shared memory by software in the system unit. It is used to convey requests to the host adapter.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
Command Word																00
Flag Word 1																02
Flag Word 2																04
																06
Data or Scatter/Gather List Pointer																08 0A
Data or Scatter/Gather List Length																0C 0E
Status Block Pointer																10 12
Chain Address																14 16
																18
																1A
Sense Information Pointer																1C 1E
CDB Length								Sense Length								20
Data Checksum																22
CDB Byte 1								CDB Byte 0								24
CDB Byte 3								CDB Byte 2								26
CDB Byte 5								CDB Byte 4								28
CDB Byte 7								CDB Byte 6								2A
CDB Byte 9								CDB Byte 8								2C
CDB Byte 11								CDB Byte 10								2E

Fields that are empty are reserved and should be set to zero.

Command Word

The command word is a 16-bit structured field used to identify the operation to be performed by the host adapter.

Command Word Structure

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	Options							Operations Code							

Operation Code

Code (hex)	Description
00	No Operation
01	Initiator SCSI Command
05	Run Diagnostic Test
06	Initialize SCSI Subsystem
08	Read Sense Information
09	Download Firmware
0A	Read Host Adapter Inquiry Data
10	Target SCSI Command

Option Flags

The option flags (bits 14-12) are used to modify the meaning of the operation code and/or the control block fields associated with the operation code. The meaning of these flags are dependent upon the operation code that uses them.

Flag Word 1

Flag word 1 is a 16-bit structured field used to specify execution parameters for this control block.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
A	D		S		S			D							C
R	S		/		E			I							N
S	B		G		S										E

Fields that are empty are reserved and should be set to zero.

Flag	Name and Function
CNE	Chain No Error The Chain No Error flag (bit 0) indicates whether control block chaining is enabled. If this bit is set to one, chaining is enabled. Upon successful completion of the control block, the host adapter will fetch the next control pointed to by the chain address. In the event of an error, chaining is halted. When set to zero, chaining is disabled and the chain address field in the control block is ignored by the host adapter. This option is available only for Initiator SCSI and No Operation commands. For all other commands, setting this flag to one will result in a specification check.
D I	Disable Interrupt The Disable Interrupt flag (bit 7) indicates whether the host is to be interrupted when the control block is completed. If this bit is set to one, the host is not interrupted upon successful completion of the control block. In the event of an error, the host adapter ignores this bit and interrupts the host. If this bit is set to zero, the host is interrupted when the control block is completed. The use of this flag is recommended only when control block chaining is enabled.
SES	Suppress Error on Underrun This flag (bit 10) indicates whether the host adapter should consider a data underrun as an error. A data underrun occurs when the amount transferred is less than the amount specified by the data length field in the control block or Scatter/Gather list. If this bit is set to one, the host adapter will not report a data underrun as an error. Information relating to the data underrun (i.e., residual byte count) will still be stored in the status block if storing of the status block is enabled (bit 14 set to zero). If this bit is set to zero, the host adapter will treat the data underrun as an error condition. Information relating to the data underrun will be stored in the status block, control block chaining (if enabled) will be halted, and the host will be interrupted.
S/G	Scatter/Gather Flag (bit 12) indicates whether Scatter/Gather should be implemented for this control block. If this bit is set to one, then the data pointer field contains the address of a list of data pointers and lengths. the data length field contains the length of the list in bytes. If this bit is set to zero, then the data length field contains the number of bytes to be transferred to or from memory starting at the address in the data pointer field. This option is available only for Initiator and Target SCSI commands. For all other commands, setting this flag to one will result in a specification check.

Continued

Flag	Name and Function
DSB	Disable Status Block The Disable Status Block flag (bit 14) indicates whether the status block is to be stored. If this bit is set to one, then the host adapter does not store the status block if the control block is completed without error. In the event of an error, the status block will be stored. If this bit is set to zero, then the status block is stored unconditionally upon completion of the control block. This flag should be set to one for most operations.
ARS	Automatic Request Sense This flag (bit 15) indicates whether the host adapter is to automatically issue a Request Sense command to the target if the target responds to the control block operation with a check condition. If this bit is set to one, then the host adapter will automatically issue a Request Sense command to the target immediately following a check condition (Target Status = 02), and prior to interrupting the host. The number of bytes of sense information the host adapter requests is specified in the sense length field. The host adapter stores the bytes to the memory address pointed to by the sense information pointer. If this bit is set to zero, then the host adapter ignores the sense length and sense information pointer fields. This option is available only for Initiator SCSI commands. This flag will be ignored for Target SCSI commands. For all other commands, setting this flag to one will result in a specification check.

Flag Word 2

Flag word 2 is a 16-bit structured field used to specify execution parameters for this control block.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
N	R			C	S	D	D		N	T	T	T	L	L	L
R	E			H	T	I	A		D	T	T	A	U	U	U
B	C			K		R	T					G	N	N	N

Fields that are empty are reserved and should be set to zero.

<table>
<tr><th>Flag</th><th>Name and Function</th></tr>
<tr><td>LUN</td><td>Logical Unit Number

This field (bits 2-0) specifies the logical unit number of the target for which the command is to be executed.</td></tr>
<tr><td>TAG</td><td>Tagged Queuing

This flag (bit 3) indicates whether tagged queuing should be implemented for this control block.

If this bit is set to one, the host adapter will send a 2-byte tag queue message to the target immediately following the Identify message. The first message byte contains the tag code and specifies the type of ordering that is desired for this command. The contents of this byte is determined by the Tag Type flags (bits 4 and 5). Table 1 gives a description of the Tag Queuing and Tag Type flags. The second message byte is a unique Tag ID assigned by the host adapter.

If this bit is set to zero, Tagged Queuing is not implemented for this control block.</td></tr>
<tr><td>TT</td><td>Tag Type

These flags (bits 4 and 5) are used by the host adapter to determine which tag code (tag queue message byte 1) to send to the target. These flags are ignored by the host adapter if the Tag Queuing flag (bit 3) is set to zero..

X means "don't care"
<table>
<tr><th colspan="2">TT</th><th>Tag</th><th>Description of Tag Queuing Option Flags</th></tr>
<tr><td>X</td><td>X</td><td>0</td><td>Tagged Queuing not implemented for this command.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>A Simple Queue Tag (Tag Code = 20h) followed by a unique Tag ID will be sent to the target immediately after the identify message.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>A Head of Queue Tag (Tag Code = 21h) followed by a unique Tag ID will be sent to the target immediately after the identify message.</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>An Ordered Queue Tag (Tag Code = 22h) followed by a unique Tag ID will be sent to the target immediately after the identify message.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Invalid. Specification error.</td></tr>
</table></td></tr>
<tr><td>ND</td><td>No Disconnect

The setting of this flag (bit 6) prevents the target from disconnecting during command execution.

If this bit is set to one, the host adapter overrides the target's configuration setting and instructs the target, via the identify message, not to disconnect during command execution.

If this bit is set to zero, the host adapter uses the target's configuration setting to determine whether disconnection should be allowed.</td></tr>
</table>

Continued

Flag	Name and Function
DAT	Data Transfer - Check Direction This flag (bit 8) determines whether the host adapter should verify the direction of the expected data phase for this command. If this bit is set to one, the host adapter expects the target to enter a data phase during command operation. The host adapter will check the Direction flag to determine the direction of the expected data phase (Data In or Data Out). It will also check the Suppress Transfer flag to determine whether to suppress the data transfer. Table 6-2 shows the relationship between this flag and the Direction and Suppress Transfer flags. Although a data phase is expected, no invalid phase error will be reported if the target does not enter a data phase. (This situation, however, does not preclude a data underrun error.) If this bit is set to zero, the host adapter ignores the Direction and Suppress Transfer flags. If a data phase occurs, the host adapter will not check the direction and proceed with the transfer. This bit should be set to zero if no data transfer is expected. Although not necessary, this bit should be set to one for commands that access the target's media (i.e., Read, Write, Write with Verify).
DIR	Direction of Transfer This flag (bit 9) indicates the expected direction of the data transfer. This flag will be ignored if the Data Transfer flag (bit 8) is set to zero. Table 6-2 shows the relationship between this and the other data option flags. If this bit is set to one, the host adapter expects the target to enter data in phase during the command (Read operation). If a data out phase is detected, the host adapter will abort the command and report an invalid phase error. The invalid phase error will not be reported if no data phase is detected. If this bit is set to zero, the host adapter expects the target to enter data out phase during the command (Write operation). If a Data In phase is detected, the host adapter will abort the command and report an invalid phase error. The invalid phase error will not be reported if no data phase is detected.

<table>
<tr><th>Flag</th><th colspan="4">Name and Function</th></tr>
<tr><td>ST</td><td colspan="4">Suppress Transfer to Host Memory

This flag (bit 10) indicates whether an incoming data transfer is to be suppressed. This flag will be ignored if the Data Transfer flag (bit 8) is set to zero.

If this bit is set to one, the host adapter will accept data from the target, but will not transfer it to host memory.

If this bit is set to zero, data transfer is not suppressed.</td></tr>
<tr><td></td><td colspan="4">Relationship between Data Transfer Option flags</td></tr>
<tr><td></td><td>ST</td><td>dir</td><td>dat</td><td>Description of data transfer option flags</td></tr>
<tr><td></td><td>X</td><td>X</td><td>0</td><td>No data transfer expected or direction of transfer not checked. If a data phase is detected, the direction is determined by the phase and not the Direction flag.</td></tr>
<tr><td></td><td>0</td><td>0</td><td>1</td><td>Data out phase expected. If data in phase is detected, transfer will be suppressed and invalid phase error reported. Invalid phase error is not reported if no data phase is detected.</td></tr>
<tr><td></td><td>0</td><td>1</td><td>1</td><td>Data in phase expected. If data out phase is detected, transfer will be suppressed and invalid phase error reported. Invalid phase error is not reported if no data phase is detected.</td></tr>
<tr><td></td><td>1</td><td>0</td><td>1</td><td>Invalid. Specification error.</td></tr>
<tr><td></td><td>1</td><td>1</td><td>1</td><td>Data in phase expected and suppress transfer. Same as above except data received from target is not transferred to host memory.</td></tr>
<tr><td></td><td colspan="4">X means "don't care"
Setting the Suppress Transfer bit differs from setting the data length field to 0. If the data length equals 0 and a data phase is detected, the host adapter will automatically suppress data transfer and report a data overrun error. If the Suppress Transfer bit is set, the host adapter will accept data from the target but not transfer it to host memory. The amount of data received will be compared to the value stored in the data length field.</td></tr>
<tr><td>CHK</td><td colspan="4">Calculate Checksum on Data

This flag (bit 11) is used to verify the integrity of the data being transferred.

If this bit is set to one, the host adapter performs a checksum of the data as it is transferred. The checksum algorithm is a simple 2-byte sum of the data. If the checksum is not equal to the value supplied in the checksum field in the control block, an error will be reported.

If this bit is set to zero, no checksum will be performed on the data and the checksum field in the control block will be ignored by the host adapter.

This option is currently available only for the Download Firmware command. For all other commands, setting this flag to one will result in a specification check.</td></tr>
</table>

Continued

Flag	Name and Function
REC	Error Recovery This flag (bit 14) is used by the host to perform error recovery procedures while the associated target is in a state of extended contingent allegiance. A state of extended contingent allegiance exists as long as the host adapter returns this status (Status Word 1, bit 14) in the status block. The condition is cleared by issuing a Resume immediate command. If this bit is set to one, and the target is in a state of extended contingent allegiance, the host adapter will execute the command. If the target is not in a state of extended contingent allegiance, the host adapter will reject the control block and report a specification check. The control blocks will also be rejected with a specification check if the Tagged Queuing flag (bit 3) is set. If this bit is set to zero, and the target is in a state of extended contingent allegiance, the host adapter will accept the command but not execute it until the condition is cleared. If the target is not in a state of extended contingent allegiance, the control block will be executed normally. This option has been defined for future versions of SCSI-2 subsystems. For current versions, this flag should always be set to zero.
NRB	No Retry on Busy Status This flag (bit 15) determines whether or not the host adapter will automatically retry an Initiator SCSI Command if the target returns Busy status. If this bit is set to one, the host adapter will terminate the command upon detecting busy status from the target. The host will be notified that the command completed with error. The target status field in the status block (byte 03) will reflect that a Busy status code (08h) was returned. If this bit is set to zero and the target returns busy status, the host adapter will retry the command indefinitely until the target completes the command successfully or until the command is aborted by the host via an Immediate command.

Data or Scatter/Gather List Pointer

This 32-bit field contains the physical memory address (least significant byte first) of the first byte of the host memory data area to be used during the data phase of the SCSI command.

If the Scatter/Gather flag (Flag Word 1, bit 12) is set to one, this field contains the physical address of the first byte of list of data pointers and lengths to be used during the data phase of the SCSI command. The number of 8-byte segments is limited to 128 (one pointer and one length), but the host adapter will only store a maximum of 17 segments in its internal memory at a time. The diagram below describes the structure of the Scatter/Gather list.

1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Data Pointer 1																															
Data Length 1																															
Data Pointer 2																															
Data Length 2																															
. . .																															
Data Pointer n																															
Data Length n																															

The data lengths must be less than 4 MBytes and the total length of the transfer must be less than 16 MBytes.

Data or Scatter/Gather List Length

This 32-bit field contains the length in bytes (least significant byte first) of the data transfer. The host should always store a value in this field (even if data transfer is to be suppressed), if a data phase is expected during the SCSI command. Otherwise, a data overrun error will occur. If no data transfer is expected, this field should be set to 0. The data lengths must be less than 4 MBytes.

If the Scatter/Gather flag (Flag Word 1, bit 12) is set to one, this field contains the length in bytes of the Scatter/Gather list. This value must be nonzero and a multiple of eight (8), otherwise, a specification error will be reported by the host adapter. The length of the Scatter/Gather list is limited to 1 KByte.

Status Block Pointer

This 32-bit field contains the physical memory address (least significant byte first) of the status block. The status block is written to by the host adapter and used by the host to determine the completion status of a control block operation.

The length of the status block is always 32 bytes, though the number of bytes stored by the host adapter may be less.

This field is required for all control blocks. However, the host adapter will bypass writing to the status block if the control block completes without error and the Disable Status Block flag (Flag Word 1, bit 14) is set to one.

Chain Address

This 32-bit field contains the physical memory address (least significant byte first) of the next control block to be processed by the host adapter.

This field is optional and used only when the Chain No Error flag (Flag Word 1, bit 0) is set to one. Control block chaining will only occur when the current control block operation completes without error.

Sense Information Pointer

This 32-bit field contains the physical memory address (least significant byte first) of the first byte of the host memory data area where the target's sense information is to be stored.

This field, along with sense length, must be supported if the Automatic Request Sense flag (Flag Word 1, bit 15) is set to one, or if the operation code in the command word specifies a Read Sense Information command. The number of bytes transferred will not exceed the value specified in the sense length field.

Sense Length

This 8-bit field specifies the maximum number of sense information bytes the host adapter will transfer. The actual number of bytes transferred may be less. The supported values are from 0 to 256 bytes. If a value of zero is stored in this field, no bytes will be transferred and the sense information will be lost. The actual number of bytes transferred will be stored in the status block (byte 14).

CDB Length

This 8-bit field specifies the length in bytes of the SCSI CDB to be sent to the target. The supported values for this field is 6, 10 and 12 bytes.

Checksum of Data

This 16-bit field contains the checksum (least significant byte first) of the data to be transferred by the host adapter.

This field is optional and used only when the Calculate Checksum on Data flag (Flag Word 2, bit 11) is set to one. The host adapter will transfer the number of bytes specified in the data length field and add the bytes together resulting in a 16-bit checksum. The host adapter will then verify the result with the value specified in this field. If the two values do not compare, an error will be reported.

> Note
> This option is currently available only for the Download Firmware command.

SCSI Command Descriptor Block

This 6-, 10-, or 12-byte field contains the actual CDB to be sent to the target during command phase.

Status Block

The status block is a 32-byte structure created in shared memory by software in the system unit. Information is placed into this structure by the host adapter to report completion status of a control block.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
Status Word																00
Target Status								HA Status								02
Residual Byte Count																04 06
Residual Buffer Address																08 0A
Additional Status Length																0C
								Sense Length								0E
																10
																12
																14
																16
CDB Byte 1								CDB Byte 0								1A
CDB Byte 3								CDB Byte 2								1C
CDB Byte 5								CDB Byte 4								1E

Fields that are empty are reserved and should be set to zero.

Status Word

The status word is a 16-bit structured field used to hold flags indicating how the command for the associated control block is completed.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	E		M	I		S	A	I	C	D	S	Q		D	D
	C		E	N		N	S	N	H	O	C	F		U	O
	A			I		S	A	T							N

Fields that are empty are reserved and will be set to zero.

Flag	Name and Function
DON	Command Done - No Error The Command Done flag (bit 0) indicates whether the control block completed successfully. If this bit is one, the control block completed without error. If this bit is zero, the other flags in this word as well as the host adapter and target status bytes should be analyzed to determine the completion status of the control block. When this flag is zero, the status block is stored unconditionally by the host adapter and an interrupt is generated, regardless of the settings of the Disable Interrupt and Disable Status Block flags (Flag Word 1, bits 7 and 14, respectively).
DU	Data Underrun The Data Underrun flag (bit 1) indicates whether the amount of data transferred was less than the amount specified by the data length field in the control block. If this bit is one, a data underrun occurred. the residual byte count and residual buffer address fields are valid. If the Suppress Error on Underrun flag (Flag Word 1, bit 10) was set to one, then the Command Done flag will also be set to one, indicating that the underrun condition was not considered an error. If the Suppress Error on Underrun flag was set to zero, then the Command Done flag will be set to zero and the Major Error/Exception flag will be set to one. If this bit is zero, no underrun condition was detected.
QF	Host Adapter Queue Full The Queue Full flag (bit 3) indicates that the host adapter was not able to accept the control block. If this bit is set to one, the host adapter has rejected the control block because its internal storage area is full. No action is taken on the control block. The host should reissue the control block after an outstanding control block completes or after an appropriate time delay.

Flag	Name and Function
SC	Specification Check The Specification Check flag (bit 4) indicates that the host adapter detected an error in the control block. If this bit is set to one, the host adapter has rejected the control block due to an error in one of the control block's fields (i.e., unsupported operation code). No action is taken on the control block. The host adapter status byte contains additional information regarding the error.
DO	Data Overrun The Data Overrun flag (bit 5) indicates whether the target attempted to transfer more data than was specified by the data length field in the control block. If this bit is one, a data overrun occurred. the residual byte count and residual buffer address fields are valid, and the Major Error/Exception flag will be set to one. If this bit is zero, no overrun condition was detected.
CH	Chaining Halted The Chaining Halted flag (bit 6) indicates that a chain of control blocks was terminated prematurely due to an error. This bit is set to one when the Command Done flag is zero (control block terminated with error) and the Chain No Error flag (Flag Word 1, bit 0) is one.
INT	Interrupt Issued for SCB The Interrupt flag (bit 7) indicates whether an interrupt has been issued for the associated control block. This bit is always set to one if the control block terminated with an error (Command Done flag is zero) or if the target is in a state of extended contingent allegiance (Extended Contingent Allegiance flag is one). This bit is also set to one if the control block completed without error (Command Done flag is one) and the Disable Interrupt flag (Flag Word 1, bit 7) is set to zero. If this bit is set to zero, no interrupt was issued for the associated control block.
ASA	Additional Status Available This flag (bit 9) is used to indicate that additional status in bytes 14 through 31 are available. If this bit is set to one, then the additional status length field contains the number of additional status bytes that are available, starting at byte 14 of the status block. If this bit is set to zero, then additional status is not available and the additional status length field is invalid.
	Continued

Flag	Name and Function
SNS	Sense Information Stored The Sense Information Stored flag (bit 9) indicates whether the target's sense information has been stored in host memory pointed to by the address in the sense information pointer field. If this bit is set to one, the sense information data area for the associated control block contains the target's sense data. The additional status length field will contain a value of at least one, and the sense length field will contain the actual number of sense information bytes transferred. If this bit is set to zero, no data has been stored in the sense information data area.
INI	Initialization Required This flag (bit 11) indicates that the host adapter needs to be initialized by the host before it can perform any normal control block operation. If this bit is set to one, the host adapter has rejected the control block because some sort of initialization is needed to complete the command; either firmware needs to be downloaded or configuration data needs to be supplied to the host adapter. The host adapter status byte contains additional information regarding what type of initialization is required.
ME	Major Error or Exception Occurred This flag (bit 12) indicates whether a major error or exception occurred on the SCSI subsystem. A major error is one that prevents the host adapter from initiating or completing a control block operation. For instance, a host adapter hardware failure, a selection timeout, or an invalid bus phase change would be considered major errors. A major exception is one that changes the configuration of the subsystem, such as a SCSI bus reset. If this bit is set to one, the host adapter has detected a major error or exception. The host adapter status byte contains additional information regarding the error. If this bit is set to zero, the implication is that any error associated with this control block does not impact the host adapter's ability to communicate with the target. A target returning a check condition status (Target Status = 02) is generally not considered a major error or exception.
ECA	Extended Contingent Allegiance This flag (bit 14) indicates whether the associated target is in a state of extended contingent allegiance. If this bit is set to one, all outstanding operations for the associated target queued in the host adapter and/or the target is suspended. While the extended contingent allegiance condition exists, any control blocks issued for the associated target that have the Recovery flag (Flag Word 2, bit 14) set to one will be executed. While the extended contingent allegiance condition exists, any control blocks issued for the associated target that do not have the Recovery flag set to one will be accepted and queued by the host adapter, but not executed until the condition is cleared. The condition is cleared by issuing a Resume command for the associated target. It is also cleared by resetting the host adapter or by issuing a Bus Device Reset to the associated target. This flag is set to one for every control block completed while the extended contingent allegiance condition exists.

Host Adapter Status

This 8-bit field contains additional error information pertaining to the host adapter or SCSI subsystem in general. This field is valid when the Command Done flag is set to zero and one of the following flags is set to one: Specification Check, Initialization Required, or Major Error/Exception.

Code	Description	Associated Status Flag
00	No Host Adapter Status Available	
04	Command Aborted by Host	Major Error/Exception
05	Command Aborted by Host Adapter	Major Error/Exception
08	Firmware Not Downloaded	Initialization Required
0A	Target Not Assigned to SCSI Subsystem	Specification Check
11	Selection Timeout	Major Error/Exception
12	Data Overrun or Underrun Occurred	Major Error/Exception
13	Unexpected Bus Free Occurred	Major Error/Exception
14	Invalid Bus Phase Detected (SCSI Reset)	Major Error/Exception
16	Invalid Operation Code	Specification Check
17	Invalid SCSI Linking Operation	Major Error/Exception
18	Invalid Control Block Parameter	Specification Check
19	Duplicate Target Control Block Received	Specification Check
1A	Invalid Scatter/Gather List	Specification Check
1B	Request Sense Command Failed	Major Error/Exception
1C	Tagged Queuing Message Rejected by Target	Major Error/Exception
20	Host Adapter Hardware Error	Major Error/Exception
21	Target Did Not Respond to Attn (SCSI Reset)	Major Error/Exception
22	SCSI Bus Reset by Host Adapter	Major Error/Exception
23	SCSI Bus Reset by Other Device	Major Error/Exception
80	Program Checksum Failure	Major Error/Exception

Target Status

This 8-bit field contains the data byte returned by the target during status phase. If the command operation terminated before the target was able to transfer a status byte, this field will be set to zero and the host adapter status will be nonzero.

Code	Description
00	Good Status or No Target Status Available
02	Check Condition
08	Target Busy
	Continued

Code	Description
04	Condition Met (For Search Data and Pre-Fetch SCSI Commands)
10	Intermediate (For Linked SCSI Commands)
14	Intermediate Condition Met
18	Reservation Conflict

When this field contains 02 (check condition) and the Sense Information Stored flag (Status Word, bit 9) is set to zero, a state of contingent allegiance exists for the target. All outstanding operations for the associated target queued in the host adapter and/or the target is suspended. Any control blocks for the associated target received after contingent allegiance occurred and before the Read Sense Information command will be accepted and queued by the host adapter, but not executed until the condition is cleared. The contingent allegiance condition is cleared by sending a read sense information control block for the associated target. It is also cleared by resetting the host adapter or by issuing a bus device reset to the associated target.

If the target returns busy status (Code = 08h), the host adapter will retry the command indefinitely. This status will be reported only when the command was aborted by the host while the host adapter was attempting retries.

If the target returns queue full status (Code = 28h), the host adapter will queue the command internally, therefore, this status will never be reported to the host. If the host adapter's internal memory is full, the control block will be rejected with Host Adapter Queue Full status (Status Word, bit 3).

Residual Byte Count

The residual byte count is a 32-bit field (least significant byte first) that contains the number of bytes that remain to be written from, or read into, the host memory buffer most recently used to transfer data. This field is valid only if the Data Underrun or Data Overrun flags (Status Word, bits 1 and 5, respectively) are set to one. If the Data Overrun flag is set to one, this field will be set to zero.

If Scatter/Gather was enabled for the associated control block, then this field contains the number of remaining bytes for the most recently used segment in the Scatter/Gather list.

If Scatter/Gather was not enabled for the associated control block, then this field contains the number of remaining bytes for the entire transfer count specified in the data length field of the control block.

Residual Buffer Address

The residual buffer address is a 32-bit field (least significant byte first) that contains the physical host memory address identifying the buffer last read from or written to. This field is valid only if the Data Underrun or Data Overrun flag (Status Word, bits 1 and 5, respectively) is set to one.

If Scatter/Gather was enabled for the associated control block, then this field contains the address of the data pointer in the Scatter/Gather list that was most recently used to transfer data.

If Scatter/Gather was not enabled for the associated control block, then this field contains the address specified in the data pointer field of the control block.

Additional Status Length

This 16-bit field specifies the number of additional bytes of status that is available. This field is valid if the Additional Status Available flag (Status Word, bit 8) is set to one. The value of this field will range from 0 to 18 (decimal) bytes. Byte 14 supplies the number of bytes transferred during a Request Sense command. Bytes 15 through 23 of the status block are reserved for future use. Bytes 24 through 31 supply information pertaining to a target mode command (either Receive or Send) received by the host adapter from another SCSI initiator.

If this field is zero, then no additional status is available and the the values in bytes 14 through 31 are invalid.

Sense Length

This 8-bit field contains the number of sense information bytes actually transferred. This number can be used to determine which bytes in the Sense Information data area are valid.

This field is valid only when the Sense Information Stored flag (Status Word, bit 9) is set to one.

Target Mode CDB

These six bytes are stored by the host adapter following the completion of a Target SCSI Command control block. They provide to the host the actual SCSI command descriptor block received by the host adapter from another initiator device on the SCSI bus.

Byte 26 contains the command opcode (08h = Receive, 0Ah = Send). Bytes 28 through 30 contain the number of bytes (most significant byte first) the initiator wanted to be transferred.

Control Block Commands

Control block commands utilize a fully multitasking delivery interface. The address of the control block is stored into the Mailbox Out registers, least significant byte first. The Attention register is then stored with the following value:

7	6	5	4	3	2	1	0
0	1	0	0	SCSI ID			

The SCSI ID specifies either the SCSI address of a particular target or initiator, or the SCSI address of the host adapter. The host adapter's ID can be found in bits 3-0 of the SCSI Definition register. Multiple control blocks or chains of control blocks can be issued for a single SCSI ID.

When the Attention register is written to, the host adapter is interrupted. When the command is completed, the host adapter (if enabled) will interrupt the host by writing to the Enhanced Mode (Group 2) Interrupt Status register. The Mailbox In registers will contain the address of the completed control block.

Following are the control block commands described in alphabetical order.

Download Firmware

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	Options			0	0	0	0	0	0	0	0	1	0	0	1	00
Flag Word 1																02
Flag Word 2																04
																06
Pointer to firmware																08 0A
Length of firmware																0C 0E
Status Block Pointer																10 12
																14
																16
																18
																1A
																1C
																1E
																20
Checksum of Data																22
																24
																26
																28
																2A
																2C
																2E

Fields that are empty are reserved and should be set to zero.

This command causes the host adapter to overwrite its program memory with data supplied by the host. The host adapter will, if enabled, perform a checksum on the data after it is written to its internal RAM, and compare the checksum to the value stored in the control block. If the two values miscompare, the host adapter will report an error and will reject all subsequent commands except a Download Firmware command.

After a Hard Reset, the host adapter will default to the firmware stored in its EEPROM.

If the Configure flag (PORTADDR register, bit 6) is set to one, the host adapter will reject all commands (control block and immediate) other than a Download Firmware command. After receiving this command, the host adapter will download the firmware into its internal RAM as described above. After successfully overwriting its program memory, the host adapter will then reprogram its EEPROM with the new firmware and perform a checksum on the new data in the EEPROM. If this checksum fails, the host adapter will report an error.

Supported Options

- Flag Word 1 - Disable Interrupt (bit 7) and Disable Status Block (bit 14) are supported. All other flags should be zero.
- Flag Word 2 - The Calculate Checksum option (bit 11) should be used. All other flags should be zero.

Initialize SCSI Subsystem

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	00
Flag Word 1																02
																04
																06
Pointer to Initialization Configuration Data																08 0A
Length of Initialization Configuration Data																0C 0E
Status Block Pointer																10 12
																14
																16
																18
																1A
																1C
																1E
																20
																22
																24
																26
																28
																2A
																2C
																2E

Fields that are empty are reserved and should be set to zero.

This command allows the host to place a copy of the configuration information pertaining to the SCSI subsystem (stored in system CMOS RAM) into the host adapter's internal RAM.

The data pointer field contains the physical memory address (least significant byte first) from which the host adapter will read the configuration data. The data length

field contains the number of bytes available to the host adapter. The maximum number of bytes read by the host adapter will be 32.

If this command is not sent, the host adapter will use its default settings. After a Hard Reset, any configuration data sent prior to the reset will be lost and the settings will revert to their default state.

The configuration data consists of two bytes per possible SCSI device (up to 16 devices) and is read from host memory in the following format.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
SCSI Device 0 (MSB) bits 2-0: Maximum synchronous transfer rate 000 — 10.0 MB/S 001 — 6.7 MB/S 010 — 5.0 MB/S 011 — 4.0 MB/S 100 — 3.3 MB/S 101 — 2.9 MB/S 110 — 2.5 MB/S 111 — 2.2 MB/S								SCSI Device 0 (LSB) bit 5: Parity Check enable bit 3: Synchronous Negotiation enable bit 2: Disconnection enable (For these bits, 1 means enabled and 0 means disabled)								00
SCSI Device 1 (MSB)*								SCSI Device 1 (LSB)**								02
SCSI Device 2 (MSB)*								SCSI Device 2 (LSB)**								04
SCSI Device 3 (MSB)*								SCSI Device 3 (LSB)**								06
SCSI Device 4 (MSB)*								SCSI Device 4 (LSB)**								08
SCSI Device 5 (MSB)*								SCSI Device 5 (LSB)**								0A
SCSI Device 6 (MSB)*								SCSI Device 6 (LSB)**								0C
SCSI Device 7 (MSB)*								SCSI Device 7 (LSB)**								0E
SCSI Device 8 (MSB)								SCSI Device 8 (LSB)								10
SCSI Device 9 (MSB)								SCSI Device 9 (LSB)								12
SCSI Device 10 (MSB)								SCSI Device 10 (LSB)								14
SCSI Device 11 (MSB)								SCSI Device 11 (LSB)								16
SCSI Device 12 (MSB)								SCSI Device 12 (LSB)								18
SCSI Device 13 (MSB)								SCSI Device 13 (LSB)								1A
SCSI Device 14 (MSB)								SCSI Device 14 (LSB)								1C
SCSI Device 15 (MSB)								SCSI Device 15 (LSB)								1E
* Same as byte 1, ** Same as byte 0																

All bits not defined above are ignored by the host adapter and may be set to either 0 or 1.

The Disconnection Enable bit (least significant byte, bit 2) determines whether the host adapter will allow the specified target to disconnect during a SCSI operation. If the enable bit is one, then disconnection is allowed for that device. The default is disconnection enabled for all devices.

The Synchronous Negotiation enable bit (least significant byte, bit 3) determines whether the host adapter will initiate synchronous negotiation with the specified target. If the enable bit is one, the host adapter will initiate synchronous negotiation for that device. If the enable bit is zero, the host adapter will not initiate negotiation, but will respond if the target initiates synchronous negotiation. The default is synchronous negotiation enabled for all devices.

The Parity Check enable bit (least significant byte, bit 5) determines whether the host adapter will check parity on incoming (SCSI to host) data transfers for the specified target. If the enable bit is one, then the parity will be checked for that device. The default is parity checking enabled for all devices.

The maximum synchronous transfer (most significant byte, bits 2-0) determines the maximum rate at which the host adapter will negotiate with the target for synchronous transfers. The default is 10 MBytes/second for all devices.

Supported Options

- Flag Word 1 - Disable Interrupt (bit 7) and Disable Status Block (bit 14) are supported. All other flags should be zero.
- Flag Word 2 - None of the options in Flag Word 2 are supported by this command.

Initiator SCSI Command

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	Options			0	0	0	0	0	0	0	0	0	0	0	1	00
Flag Word 1																02
Flag Word 2																04
																06
Data or Scatter/Gather List Pointer																08 0A
Data or Scatter/Gather List Length																0C 0E
Status Block Pointer																10 12
Chain Address																14
																16
																18
																1A
Sense Information Pointer																1C 1E
CDB Length								Sense Length								20
																22
CDB Byte 1								CDB Byte 0								24
CDB Byte 3								CDB Byte 2								26
CDB Byte 5								CDB Byte 4								28
CDB Byte 7								CDB Byte 6								2A
CDB Byte 9								CDB Byte 8								2C
CDB Byte 11								CDB Byte 10								2E

Fields that are empty are reserved and should be set to zero.

This command causes the host adapter to initiate a SCSI command to a target. The SCSI address of the target is supplied in bits 3-0 of the Attention register. The logical unit number of the target is supplied in bits 2-0 of Flag Word 2.

Supported Options

- Flag Words 1 and 2 - All options are supported except for the Calculate Checksum option (Flag Word 2, bit 11).

No Operation

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	Options			0	0	0	0	0	0	0	0	0	0	0	0	00
Flag Word 1																02
Flag Word 2																04
																06
																08
																0A
																0C
																0E
Status Block Pointer																10 12
Chain Address																14 16
																18
																1A
																1C
																1E
																20
																22
																24
																26
																28
																2A
																2C
																2E

Fields that are empty are reserved and should be set to zero.

If the SCSI ID specified in the Attention register specifies the SCSI address of the host adapter, then this command is intended for diagnostic purposes to test whether the transfer of control blocks and their associated interrupts are working properly. It can also be used to test whether control block chaining is working properly. The Logical Unit Number (Flag Word 2, bits 2-0) is ignored.

If the SCSI ID specified in the Attention register specifies the SCSI address of a particular target, then this command is intended to queue an interrupt to signal a progress point in a chain of control blocks.

Supported Options

- Flag Word 1 - Chain No Error (bit 0), Disable Interrupt (bit 7) and Disable Status Block (bit 14) are supported. All other flags should be zero.
- Flag Word 2 - Logical Unit Number (bits 2-0) are supported. All other flags should be zero.

Read Host Adapter Inquiry Data

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	Options			0	0	0	0	0	0	0	0	1	0	1	0	00
Flag Word 1																02
																04
																06
Destination Pointer of inquiry data																08 0A
Length of inquiry data																0C 0E
Status Block Pointer																10 12
																14
																16
																18
																1A
																1C
																1E
																20
																22
																24
																26
																28
																2A
																2C
																2E

Fields that are empty are reserved and should be set to zero.

This command can be used to obtain release information and revision level of the host adapter's firmware. It also provides information regarding parameters of the host adapter.

The data pointer field contains the physical memory address (least significant byte first) to which the host adapter will store the configuration. The data length field contains the maximum number of bytes allocated for the status block. The maximum

number of bytes this command supports is 256. The host adapter may not transfer the total number of bytes allocated, therefore, the Suppress Error on Underrun flag (Flag Word 1, bit 10) should be set to one.

Supported Options

- Flag Word 1 - Disable Interrupt (bit 7), Suppress Error on Underrun (bit 10) and Disable Status Block (bit 14) are supported. All other flags should be zero.
- Flag Word 2 - None of the options in Flag Word 2 are supported by this command.

The information is written into host memory in the following format.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
SCSI Device Type																00
SCSI Support Level																02
No. of LUNs								Additional Lng								04
Flags								No. of CBs								06
Vendor Verification																08 0A 0C 0E
Product Identification																10 12 14 16
Firmware Type																18 1A 1C 1E
Firmware Revision Level																20 22
Release Date																24 26 28 2A
Release Time																2C 2E 30 32
Firmware Checksum																34
Reserved																36
Reserved for Information on SSCI Peripherals . . .																30 5E
Reserved . . .																60 FE

The SCSI device type word contains the following information.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	Reserved							0	T	T	0	0	0	1	1
									M	M					
									S	D					

Bits 4-0 will be set to a value of 03 indicating that the host adapter is a processor type. Bit 5 indicates whether the host adapter is enabled for Target Mode. If this bit is zero, then Target Mode is enabled. Byte 5 specifies the number of LUNs the host adapter has enabled for Target Mode. If this bit is one, then Target Mode is disabled and byte 5 will be zero. Bit 6 indicates whether Target Mode is supported by this version of firmware. If this bit is zero, then Target Mode is supported. If this bit is one, then Target Mode is not supported. Bit 5 will always be set to one if bit 6 is one. Bits 14-8 are reserved for flags indicating support for special features the firmware may incorporate. All other bits will be set to zero.

The SCSI support level word contains the following information.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
A	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
E															
N															

Bits 2-0 indicate that this firmware version supports SCSI-2. Bit 15 indicates whether this firmware version can accept asynchronous event notifications from a target. If this bit is one, the host adapter supports this feature. If this bit is zero, then the host adapter will reject any asynchronous event notification messages. All other bits will be set to zero.

The additional length byte indicates the number of bytes of additional information the host adapter has available. This value will not be truncated if the data length field is smaller than the amount of valid information.

Byte 5 indicates the number of LUNs the host adapter has enabled for Target Mode. The actual LUNs supported start at LUN 0 (e.g., if this byte contains a 3, then LUN 0, 1 and 2 are enabled.)

Byte 6 indicates the number of control blocks the host adapter can store internally before responding with a queue full status.

The flags byte contains the following information.

7	6	5	4	3	2	1	0
0	0	W	S	L	D	0	0
		I	Y	N	I		
		D	N	K	F		

Bit 2 indicates whether the board SCSI electrical interface is Single-Ended/AHA-1740A/1742A (bit reset) or Differential/AHA-1744 (bit set). Bit 3 indicates that the host adapter supports SCSI-linked commands and will always be set to one. Bit 4 indicates that the host adapter supports synchronous transfers and will always be set to one. Bit 5 indicates whether the SCSI bus supports 8- or 16-bit data transfers. If this bit is one, then the SCSI data bus is 16 bits wide. If this bit is zero, then the SCSI data bus is 8 bits wide. All other bits will be set to zero.

The vendor identification field contains eight bytes of ASCII data identifying the vendor of the host adapter (e.g., Adaptec).

The product identification field contains eight bytes of ASCII data identifying the product name of the host adapter (e.g., AHA-1740A/1742A).

The firmware type field contains eight bytes of ASCII data indicating whether the firmware is a standard product or a special version (e.g., Enhanced).

The firmware revision level contains four bytes of ASCII data identifying the release level. The release level starts at "A" for each firmware type.

The release data contains eight bytes of ASCII data identifying the date that the firmware was released.

The release time contains eight bytes of ASCII data identifying the time of day that the firmware was released.

Read Sense Information

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	0	0	0	0	0	0	0	0	0	0	0	1	0			00
Flag Word 1																02
Flag Word 2																04
																06
																08
																0A
																0C
																0E
Status Block Pointer																10 12
																14
																16
																18
																1A
Sense Information Pointer																1C 1E
Sense Length																20 22
																24
																26
																28
																2A
																2C
																2E

Fields that are empty are reserved and should be set to zero.

This Command causes the host adapter to issue a Request Sense command to the target. The SCSI address of the target is supplied in bits 3-0 of the Attention register. The logical unit number of the target is supplied in bits 2-0 of Flag Word 2. This command must be issued when an Initiator SCSI command with Automatic Request Sense disabled (ARS = 0) returns a check condition (Target Status = 02) in the status block. After completion of this command, the host adapter and the target will release contingent allegiance and resume operation for any queued commands. If extended

contingent allegiance was reported in the status block of the Initiator SCSI command, this command must be followed by a Resume command to release extended contingent allegiance.

Supported Options

- Flag Word 1 - Suppress Error on Underrun (bit 10) and Disable Status Block (bit 14) are supported. All other flags should be zero.
- Flag Word 2 - Logical Unit Number (bits 2-0) and No Disconnect (bit 6) are supported. All other flags should be zero.

Run Diagnostic Test

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	Options			0	0	0	0	0	0	0	0	0	1	0	1	00
Flag Word 1																02
Write FIFO Data Pointer																04 06
Read FIFO Data Pointer																08 0A
Test FIFO Data Length																0C 0E
Status Block Pointer																10 12
																14
																16
																18
																1A
																1C
																1E
																20
																22
																24
																26
																28
																2A
																2C
																2E

Fields that are empty are reserved and should be set to zero.

This command causes the host adapter to perform certain diagnostic routines. The actual tests performed are dependent upon the setting of the option flags in the command word, as described below. Any value of these bits not defined below may result in a specification check.

Value	Meaning
000	Self-Test The host adapter performs a subset to its self-diagnostic routines that it normally performs at power-up. The two data pointer fields and the data length field is ignored.
001	Test FIFO The host adapter will transfer data from the address in the write FIFO data pointer field (least significant byte first) to its internal FIFO. The host adapter will transfer the number of bytes specified in the test FIFO data length field (up to 1024 bytes). After writing to the FIFO, the host adapter will then transfer the contents of the FIFO to the address in the read FIFO data pointer field (least significant byte first), whereupon the host may compare the data.

Supported Options

- Flag Word 1 - Disable Interrupt (bit 7) and Disable Status Block (bit 14) are supported. All other flags should be zero.
- Flag Word 2 - is replaced by the write FIFO data pointer for this command.

Target SCSI Command

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	00
Flag Word 1																02
Flag Word 2																04
																06
Data or Scatter/Gather List Pointer																08 0A
Data or Scatter/Gather List Length																0C 0E
Status Block Pointer																10 12
																14
																16
																18
																1A
Sense Information Pointer																1C 1E
Sense Length																20 22
																24
																26
																28
																2A
																2C
																2E

Fields that are empty are reserved and should be set to zero.

This command enables the host adapter to complete a SCSI Command initiated by another SCSI device. The SCSI address of the initiator is supplied in bits 3-0 of the attention register. The logical unit number of the host adapter is supplied in bits 2-0 of Flag Word 2.

Supported Options

- Flag Word 1 - Scatter/Gather (bit 12) is supported. Suppress Error on Underrun (bit 10) should be used with care since the exact length of the transfer may not be known. Disable Status Block (bit 14) should also be used with care since the status block will return information regarding the actual command received. The Automatic Request Sense flag (bit 15) is ignored - if the host adapter returns the initiator a check condition, the sense information will automatically be stored in host memory pointed to by the sense information pointer. If the host has no need for the sense information, a zero should be stored in the sense length field. All other flags should be zero.

- Flag Word 2 - Logical Unit Number (bits 2-0), Data Transfer (bit 8) and Direction of Transfer (bit 9) are supported. All other flags should be zero. The following table shows the relationship between the Data Transfer and Direction flags.

Direction	Data Transfer	Description
X	0	Invalid. Specification error.
0	1	Receive command expected. The host adapter will enter a data in phase. (Data transfer from host memory to initiator.)
1	1	Send command expected. The host adapter will enter a data out phase. (Data transfer from initiator to host memory.)
X indicates don't care		

Aborting Control Block Commands

The Attention register provides a means for aborting an outstanding control block operation. The address of the control block to be aborted is stored into the Mailbox Out registers, least significant byte first. The Attention register is then stored with the following value:

7	6	5	4	3	2	1	0
0	1	0	1	SCSI ID			

The SCSI ID specifies the SCSI address of a particular target or initiator.

When the Attention register is written to, the host adapter is interrupted. The host adapter then scans its internal control block queue for a control block that has an address that matches the one stored in the Mailbox Out registers. If the associated control block is not found, the abort is ignored and no interrupt will be posted back to the host. If the associated control block is found, the host adapter will take the following action based on the current progress of the operation.

Control Block is Queued for Operation

A control block is queued for operation when it has not yet initiated any activity on the SCSI bus. The host adapter will terminate the control block and place it on the interrupt queue. When the host is interrupted for this control block, the Enhanced Mode (Group 2) Interrupt Status register will report control block complete with error. The Mailbox In registers will contain the address of the aborted control block. The status block will report a major error/exception and the host adapter status will indicate that the control block was aborted by the host. If chaining was enabled for this control block, the chain will be halted.

Associated Target for the Control Block is Disconnected

If the command had been initiated, but the target had disconnected, the host adapter will terminate the control block as described above. When the target reconnects, the host adapter will issue an Abort (or Abort Tag) message.

> Note
> Even though the control block will be terminated and reported back to the host, the host adapter must maintain a history of the control block in its internal RAM in order to send the Abort message when the target reconnects. It is possible that the target may never reconnect. If this happens, the host adapter will continue to operate normally, but that portion of internal RAM will be lost as a resource until a Device Reset or Host Adapter Reset is issued.

Control Block is Currently Active on the SCSI Bus

If the command had been initiated and the target was currently active on the SCSI bus, the host adapter will assert the Attention signal. If the target responds to Attention with Message Out phase, the host adapter will issue an Abort (or Abort Tag) message which forces the target to go bus free. If the target goes bus free either from the Abort message, disconnection, or command completion, the host adapter will terminate the control block as described above.

If the target does not go bus free within 250 milliseconds, the host adapter will reset the SCSI bus to force the target off the bus. The control block will be terminated as described above except that the host adapter status byte in the status block of the control block will reflect that the target did not respond to Attention.

Control Block in the Interrupt Queue

If the command had already been completed and an interrupt was pending to the host for the associated control block, the host adapter will report the completion of the control block normally. The abort operation will have no affect.

> Note
> There is no interrupt associated with the abort operation. Its sole purpose is to prematurely terminate any control block queued or in progress.

Asynchronous Event Notification

An asynchronous event occurs when the host adapter detects an unexpected condition on the SCSI subsystem.

Asynchronous Event Conditions

- A SCSI bus reset has occurred
- The host adapter was selected by another initiator

The host adapter notifies the host of an asynchronous event via an interrupt. When the host detects the interrupt, the Interrupt Status register will contain the following value:

7	6	5	4	3	2	1	0
1	1	0	1	SCSI ID			

The SCSI ID specifies either the SCSI address of a particular device on the subsystem, or the SCSI address of the host adapter. The host adapter's ID can be found in bits 3-0 of the SCSI Definition register.

Prior to interrupting the host, the host adapter will store additionl information in the Mailbox In registers.

SCSI Bus Reset

If a SCSI bus reset has occurred, the SCSI ID in the Interrupt Status register will be the host adapter's ID. The Mailbox In registers will contain the following information:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
																						Reset Code									

The least significant byte contains the reset error code. The three most significant bytes will be zero. Possible Reset error codes:

Code	Description
22	SCSI Bus Reset by Host Adapter
23	SCSI Bus Reset by Other Device

For more information on how the host adapter handles SCSI resets, refer to the section titled *SCSI Bus Reset Handling.*

Host Adapter Selected by Another Initiator

If the host adapter is selected by another initiator on the SCSI subsystem, the host adapter will respond as a processor-type target. If the command received by the initiator requests a data transfer (Send or receive command) *and* the host adapter does not already have a prepared Target SCSI command from the host, the host adapter will disconnect from the selecting initiator and interrupt the host with an Asynchronous event notification. The SCSI ID in the Interrupt Status register will be the ID of the selecting initiator. The Mailbox In registers will contain the following information:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
D				LUN			CDB Byte 2									CDB Byte 3							CDB Byte 4									

The first three bytes of the Mailbox In registers contain the number of bytes (least significant byte first) that was requested to be transferred by the selecting initiator. These bytes rflect the values of bytes 2-4 of the command descriptor block that was sent by the selecting initiator.

The most significant byte of the Mailbox In registers, bits 2-0, contains the logical unit number of the host adapter that was specified in the identify message received from the selecting initiator.

The most significant byte of the Mailbox In registers, bit 7, contains the direction of the requested data transfer. If this bit is set to one, then a Send command was issued by the selecting initiator (data transfer from initiator to host memory). If this bit is set to zero, then a Receive command was issued by the selecting initiator (data transfer from host memory to initiator).

The remaining bits in the most significant byte of the Mailbox In registers will be set to zero.

Upon detecting the interrupt, the host can use the information in the Interrupt Status and Mailbox In registers to create a Target SCSI command control block that will enable the host adapter to complete the data transfer.

Immediate Commands

Immediate commands are non-control block operations that will be processed by the host adapter immediately. They use the same delivery interface as control block commands. Instead of a control block address, a 32-bit immediate command is stored into the Mailbox Out registers, least significant byte first. The Attention register is then stored with the following value:

7	6	5	4	3	2	1	0
0	0	0	1	SCSI ID			

The SCSI ID specifies either the SCSI address of a particular target, or the SCSI address of the host adapter. The host adapter's ID can be found in bits 3-0 of the SCSI Definition register.

When the Attention register is written to, the host adapter is interrupted. When the command is completed, the host adapter (if enabled) will interrupt the host by writing to the Enhanced Mode (Group 2) Interrupt Status register. If the immediate command completed with an error, the first byte of the Mailbox In registers will contain the appropriate error code.

Supported Immediate Commands

- Reset (80h)
- Resume (90h)

The control block commands are described below in alphabetical order.

Reset

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
								1	0	0	0	0	0	0	0	00
												A	D			02

Fields that are empty are reserved and should be set to zero.

This command allows the host, via software control, to reset a particular target or the host adapter.

This command will always interrupt the host upon completion. The host should wait until the interrupt is posted in order to determine if the reset was completed successfully.

Reset Device

If the Attention register contains the ID of a SCSI target, then this command is intended to reset the associated device to a known state with minimum impact to other devices on the bus.

On receiving this command, the host adapter will clear its internal memory of all outstanding control blocks for the associated target. It will also clear any queued interrupts for the associated target. A queued interrupt occurs when a control block

completes, with or without error, and the host adapter has not yet issued the interrupt to the host. The action taken on the target depends on the setting of the Device Reset Option flag (byte 3, bit 2).

If the Device Reset Option flag is set to zero, the host adapter will attempt to issue a bus device reset to the target. The host adapter will attempt to select the target with Attention and send a bus device reset message. If the target does not respond to selection, an error will be reported. If the target is currently active on the bus, the host adapter will assert the Attention signal. If the target does not respond to the Attention signal within 250 milliseconds, the host adapter will reset the bus and report an error.

If the Device Reset Option flag is set to one, the host adapter will attempt to abort all outstanding operations for the target without resetting the device. If the target is currently active, the host adapter will assert the Attention signal and send an Abort message. If the target does not respond to the Attention signal within 250 milliseconds, the host adapter will reset the SCSI bus and report an error. If the target reconnects with an operation that was cleared by this command, the host adapter will respond with an Abort (or Abort Tag) message.

The Adapter Reset Option flag (byte 2, bit 3) is ignored by the host adapter for device reset operations.

Possible errors:

Code	Description
08	Firmware not downloaded
11	Selection timeout
20	Host adapter hardware failure
21	Target did not respond to attention: SCSI Bus reset by host adapter

If the host adapter resets the SCSI bus because the device did not respond to Attention, the host adapter will perform the following sequence:

1. Report Immediate Command Complete with Error.

2. Flush Interrupt Queue for all Other Devices. The host adapter will post back any commands for devices other than the one reset that completed prior to the SCSI Bus Reset.

3. Interrupt the host with Asynchronous Event Notification. The host adapter will interrupt the host with Asynchronous event status. The SCSI ID in bits 3-0 of the Interrupt Status register will contain the SCSI ID of the host adapter. The least significant byte of the Mailbox In registers will contain a value of 22 (hex) signifying that the SCSI bus was reset by the host adapter.

4. Post completion status of all outstanding commands received prior to the host acknowledgment of the Asynchronous Event Notification interrupt. Any commands that were outstanding when the SCSI Bus Reset occurred *and* any commands received between the reset and the host acknowledgment of the Asynchronous Event Notification interrupt will be returned with error status. The status

returned will reflect that the command was aborted by the host adapter (error code = 05). Any commands received after the acknowledgment of the Asynchronous Event Notification interrupt will be operated on normally.

Reset Host Adapter

If the Attention register contains the SCSI ID of the host adapter, then this command is intended to reset the SCSI subsystem to a known state.

On receiving this command, the host adapter will clear its internal memory of all outstanding control blocks and queued interrupts for all targets on the SCSI bus. The action taken on the SCSI bus depends on the setting of the Adapter Reset Option Flag (byte 2, bit 3).

If the Adapter Reset Option flag is set to zero, the host adapter will assert the Reset signal on the SCSI bus, thus initializing all devices on the bus.

If the Adapter Reset Option flag is set to one, the host adapter will attempt to abort all outstanding operations for all targets without resetting the SCSI bus. If a target is currently active, the host adapter will assert the Attention signal and send an Abort message. If the target does not respond to the Attention signal within 250 milliseconds, the host adapter will reset the SCSI bus and report an error. If a target reconnects with an operation that was cleared by this command, the host adapter will respond with an Abort (or Abort Tag) message.

The Device Reset Option flag (byte 2, bit 2) is ignored by the host adapter for host adapter reset operations.

Possible errors:

Code	Description
08	Firmware not downloaded
20	Host adapter hardware failure
21	Target did not respond to Attention: SCSI Bus reset by host adapter

If the host adapter resets the SCSI bus because the device did not respond to Attention, the result of the command will be as if the host adapter reset was issued with Adapter Reset Option Flag set to zero.

Resume

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Byte Offset
								1	0	0	1	0	0	0	0	00
										1						02

Fields that are empty are reserved and should be set to zero.

This command is used to clear an extended contingent allegiance condition. The host adapter notifies the host that a target is in a state of extended contingent allegiance by setting bit 14 in the status word. After issuing this command, all queued operations for the target specified in the Attention register will no longer be suspended and normal operation is resumed.

If the host adapter receives this command for a target that is not in a state of extended contingent allegiance, this situation is not considered an error, and the command is treated as a No-Op.

Bit 5 in byte 2 provides the option of whether an interrupt should be issued upon completion of this command. Setting this bit to one, disables the interrupt. If this bit is set to zero, an interrupt will be reported.

Possible errors:

Code	Description
08	Firmware not downloaded
20	Host adapter hardware failure

SCSI Bus Reset Handling

A SCSI bus reset can occur in several ways. The following describes what can cause the reset and how the host adapter will respond to the condition.

Reset Initiated by the Host

Hard Reset. When the host adapter is reset via hardware control and the RSTPWR flag (SCSIDEF Register, bit 4) is set to one, the SCSI bus will be reset by the host adapter as part of its power-on sequence. There will be no notification of the SCSI reset since it is implied by the Hard Reset.

Soft Reset. When the host adapter is reset via software control (Immediate Reset command) and the Adapter Reset Option flag is set to zero, the SCSI bus will be reset by the host adapter as part of its reinitialization. There will be no notification of the SCSI reset since it is implied by the Soft Reset.

Reset Initiated by the Host Adapter

The host adapter will reset the bus if it encounters an error on a SCSI operation that it cannot recover from. Some examples include: the target goes to an invalid bus phase, the host adapter cannot force the target to go bus free when attempting to abort a command, or the host adapter cannot send a bus device reset message. After resetting the bus, the host adapter will perform the following sequence:

1. Flush Interrupt Queue. The host adapter will post back all commands that completed prior to the SCSI Bus Reset.

2. Interrupt the host With Asynchronous Event Notification. The host adapter will interrupt the host with asynchronous event status. The SCSI ID in bits 3-0 of the Interrupt Status register will contain the SCSI ID of the host adapter. The least significant byte of the Mailbox In registers will contain a value of 22h.

3. Interrupt the host with Completion Status of the command that caused the SCSI Bus Reset.

4. Post completion status of all outstanding commands received prior to the host acknowledgment of the Asynchronous Event Notification interrupt. Any commands that were outstanding when the SCSI Bus Reset occurred and any commands received between the reset and the host acknowledgment of the Asynchronous Event Notification interrupt will be returned with error status. The status returned will reflect that the command was aborted by the host adapter (error code: 05). Any commands received after the acknowledgment of the Asynchronous Event Notification interrupt will be operated on normally.

> Note
> If the host adapter resets the SCSI bus when attempting a device or host adapter reset (via an Immediate command) the action taken by the host adapter differs from that described above. Refer to the Immediate command descriptions for more detail.

Reset Initiated by Another SCSI Device

If the host adapter detects a SCSI Bus Reset, it will perform the following sequence:

1. Flush Interrupt Queue. The host adapter will post back all commands that completed prior to the detection of the SCSI Bus Reset.

2. Interrupt the host with Asynchronous Event Notification. The host adapter will interrupt the host with asynchronous event status. The SCSI ID in bits 3-0 of the Interrupt Status register will contain the SCSI ID of the host adapter. The least significant byte of the Mailbox In registers will contain a value of 23h.

3. Post completion status of all outstanding commands received prior to the host acknowledgment of the Asynchronous Event Notification interrupt. Any commands that were outstanding when the SCSI Bus Reset was detected and any commands received between the reset and the host acknowledgment of the

Asynchronous Event Notification interrupt will be returned with error status. The status returned will reflect that the command was aborted by the host adapter (error code: 05). Any commands received after the acknowledgment of the asynchronous event notification will be will be operated on normally.

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Chapter Seven

Onboard BIOS Interface

Introduction

The AHA-1740A/1742A/1744 BIOS operates in two different modes which correspond to the two possible firmware configurations. The two modes supported by the BIOS are Standard Mode (communicates with the adapter via the standard compatible interface) and the Enhanced (EISA) Mode (communicates with the adapter via the enhanced interface). In each mode the responsibilities of the BIOS are the same:

- Perform any power-up initialization needed for either the AHA-1740A/1742A/1744 or SCSI devices connected to it.
- Support the standard Interrupt 13h interface for SCSI disk drives on the SCSI bus. This support enables use of drives attached to the adapter under real mode operating systems such as DOS without a device driver. The limit for Int 13h supported drives is set at two (80h-81h). Future revisions of the BIOS will support more than two drives, a feature which can be used by DOS 5.0 and later.
- Provide capability for booting from a fixed disk installed on the AHA-1740A/1742A/1744.

Operation with the Standard Interface

The AHA-1740A/1742A/1744 BIOS resides on the host adapter board. It provides support for up to two SCSI Common Command Set (CCS) disk drives under DOS. If SCSI devices other than CCS disk drives, or if support for more than two disk drives is required under DOS, the Adaptec DOS Driver, ASW-1410 must be used. The BIOS provides a very simple single-threaded capability that does not make use of the Mailbox Interface used by more sophisticated programs. This capability allows the host system to boot from a SCSI disk drive and to support standard DOS calls from any standard program.

The BIOS communicates with the host adapter through a special set of commands passed under the I/O Command Port command 03 (Start PC AT BIOS Command). These commands are not available to any programs except the Adaptec BIOS. The Adaptec BIOS provides a standard BIOS interface. The DOS interface to the standard BIOS is described in this section.

In many machines, up to two hard disks are supported by the BIOS resident on the motherboard. Any other drives must be managed through the Mailbox Interface using an appropriate driver. The operation of the AHA-1740A/1742A/1744 BIOS on

attached SCSI devices depends on the number of standard hard disks installed directly on the system.

No Standard Hard Disks Installed

In this case, two SCSI drives can be supported by the AHA-1740A/1742A/1744 BIOS. SCSI target 0 Logical Unit Number (LUN) 0 is designated as drive 0 (drive *C*). Either SCSI target 0 LUN 1 or SCSI target 1 LUN 0 may be designated as drive 1 (drive *D*). This set of addresses allows the use of two drives with either embedded controllers or bridge controllers. Booting is only performed from SCSI Target 0 LUN 0. When no standard hard disks are installed, the AHA-1740A/1742A/1744 BIOS is operating in nonconcurrent mode.

One Standard Hard Disk Installed

In this case, the internally installed hard disk is designated as drive 0 (drive *C*). SCSI device 0 LUN 0 is designated as drive 1 (drive *D*). Booting is performed from the internally installed hard disk. This mode of operation is called concurrent operation, indicating that the internally installed drive and one SCSI drive can operate together under the BIOS.

Two Standard Internal Hard Disks Installed

In this case, all the disks that can be supported by the BIOS are directly installed. The AHA-1740A/1742A/1744 BIOS will not support any SCSI drives. A device driver must be installed to access the SCSI drives.

Enhanced Interface Operation

Hardware

The BIOS occupies 16KBytes of system ROM space at one of a number of optional physical locations. These hex locations are CC000, D0000, D4000, D8000, DC000, E0000, E4000, E8000 and EC000. 2KBytes of this space is R/W shadow RAM, enabling the BIOS to store critical information without risking compatibility by using system data areas. The BIOS is coded using the 386 instruction set.

Initialization

The system BIOS recognizes the AHA-1740A/1742A BIOS by the standard ROM signature information in the first four bytes of the EPROM. This signature includes an offset to an initialization routine which is subsequently called by the system BIOS. When the AHA-1740A/1742A BIOS gains control, the following steps will be taken:

1. The BIOS will search the EISA slots for the adapter onto which it is installed. The correct adapter can be identified by matching the current code segment with the

BIOS base address in the boards setup registers. In the case where the board is not functioning properly, the BIOS will display the message:

Unable to initialize SCSI host adapter!

and the BIOS will fail initialization. The failure will be flagged to the system via the BP register so that the system BIOS can halt system initialization until the user strikes a key (**F1** on most systems).

2. The BIOS will normally reset the adapter. Using the configuration utility, the BIOS may be configured not to reset the adapter. This adapter reset may also result in a reset of the SCSI bus. The BIOS will wait two seconds before proceeding with initialization, as many SCSI devices are unable to communicate properly shortly after a SCSI Reset.

3. Having found and reset the board, the BIOS will proceed to setup and test the onboard shadow RAM. If diagnostics on this RAM fail, the message:

   SCSI host adapter shadow RAM diagnostic failure!

   will be displayed, and initialization will fail. If the RAM is ok, the BIOS then performs a diagnostic check on the adapter hardware to ensure that it is functioning properly. If not, the message:

   SCSI host adapter diagnostic failure!

   will be displayed. If there is any failure, it will be flagged to the system.

4. The BIOS will pull adapter configuration information out of system CMOS RAM via Int 15h and will download this configuration information to the host adapter.

5. The BIOS will determine configuration information regarding installed SCSI devices from the information acquired from CMOS RAM.

A BIOS support option set to **fr** indicates that the BIOS should attempt to support the device under Int 13h. If the device is not installed or not SCSI device type 0 or 7 (byte 0 of Inquiry info), the drive will not be supported under Int 13h. A BIOS support option of **hd** is the same as **fr** except that removable hard drives are not considered hard drives and are not eligible for Int 13h support.

A BIOS support option of **no** disables Int 13h support for the device. The default setting will be **hd** for all devices. The net effect of the defaults is to cause the BIOS to scan the entire SCSI bus looking for fixed hard drives to support via Int 13h. If the user ever changes a device to **fr** a warning screen should appear informing the user of the issues involved with BIOS support for removable media.

Other Changes

The BIOS is interrupt driven in Enhanced Mode and fully supports Int 15h allowing operation with various write caching programs. The BIOS supports drives 80h on one board and 81h on the next board with both boards sharing the same interrupt.

The BIOS also supports a new Interrupt 13h call to identify which Int 13h drives (80h and 81h) correspond to which host adapter and SCSI ID. Note that *aspiedos.sys, afdisk.exe* and *aspidisk.sys* files in the current ASW-1410 have been changed to support this function. This eliminates the requirement on previous Adaptec host adapters that Int 13h devices may only be at targets 0 and 1.

> Note
> In Standard Mode, the BIOS will stop scanning for devices as soon as a device is indicated as not present. This is done to be compatible with the AHA-1540 which requires the first SCSI drive to be at target 0, the second at target 1, etc.

The AHA-1740A/1742A BIOS will perform the steps necessary to support Int 13h on the SCSI drives which were assigned Int 13h IDs. This includes the building of drive tables in shadow RAM for drives 80h and 81h and updating drive table pointers at interrupt vector locations 41h and 46h, respectively. The drive tables are not actually used by the AHA-1740A/1742A BIOS during normal operation, but are merely provided for compatibility. The AHA-1740A/1742A BIOS will revector Interrupt 13h so that all calls for disk I/O can be filtered by the AHA-1740A/1742A BIOS. Requests for non-SCSI drives are passed on to the original Int 13h vector which is stored in shadow RAM. The system drive count (40:75) is updated to reflect the new system drive count. See the *Onboard BIOS Operation* section in Chapter Two, *Architecture* for more information on Int 13h functionality.

Once initialization is complete and all appropriate data structures have been setup in shadow RAM, the BIOS will write protect the shadow RAM so that further access is prohibited. Because an outside agent can always move the BIOS into write protected area, no write access is made to this area after initialization. Systems which move the BIOS into such an area before initialization will not work with the AHA-1740A/1742A BIOS.

Boot Issues

Traditionally, systems have booted from drive 80h (often referred to as drive *C*). For ISA systems, Adaptec SCSI BIOS ROMs were forced to intercept Interrupt 19h in order to provide booting capability from a SCSI drive. This was due mainly to the fact that many motherboard BIOS products did not properly issue Int 13h calls to perform the boot. It is currently not the case with EISA systems. Therefore, the AHA-1740A/1742A BIOS will not contain any booting code and Int 19h will be left alone. The system BIOS is free to implement any boot algorithm it chooses, and SCSI drives will be supported by such schemes as long as Int 13h calls are used to read the boot sector(s). On systems which will only boot from drive 80h (this is very typical) then booting from SCSI will be limited to a SCSI drive assigned as drive 80h. Note that this excludes booting from SCSI if there is already a standard controller in the system. The user can control the boot drive by mapping out drives via the

AHA-1740A/1742A CMOS configuration so the desired boot drive is the first drive found by the system.

Interrupt 13h Interface Functionality

Disk I/O requests are passed from the operating system to the BIOS through software interrupt 13h. CPU registers are used to pass a function code as well as the associated parameters for the function. The AHA-1740A/1742A BIOS supports SCSI drives under Int 13h by intercepting each request and routing the request based on the drive number. If the drive number corresponds to a SCSI drive, the AHA-1740A/1742A services the request through the AHA-1740A/1742A. If the drive number specifies a floppy or non-SCSI hard drive, the request is passed to the original Int 13h vector for processing. Most Int 13h requests use the following registers for parameter passing:

Register	Function
AH	BIOS Function Code
AL	Sector Count
CH	Low Byte of Cylinder Number
CL (Bits 7,6)	High Bits of Cylinder Number
CL (Bits 5-0)	Sector Number (1-based)
DH	Head Number
DL	Drive Number
ES:BX	Data Buffer Address

Physical to Logical Block Address Translation

As shown above, the starting sector addresses for read, write and verify requests is passed as a physical address including a 10-bit cylinder number, an 8-bit head number, and a 6-bit sector number (which is 1-based so the maximum sector number is 63 instead of 64). SCSI devices are addressed by logical block address without regard to the physical geometry of the drive. For this reason, all SCSI devices are defined as drives with 64 heads and 32 sectors/track. An appropriate number of cylinders is used to provide the full capacity of the drive using this physical to logical translation. Each cylinder is exactly one megabyte in size using this scheme and the physical to logical translation can be described by the following simple algorithm:

LBA = Cylinder (10 bits) | | Head (6 bits) | | (Sector-1) (5 bits)

This provides 21 bits of addressing, which is equivalent to one gigabyte given that the Int 13h interface assumes a block size of 512 bytes/sector.

Virtual to Physical Buffer Address Translation

A data buffer address is passed to the BIOS via ES:BX. This virtual address can be easily translated into the physical address needed by a Bus Master device when the

system processor is in real mode. Because this is the case at system boot time and under normal DOS operation, simple segment arithmetic is normally used to convert ES:BX to a physical address usable by the AHA-1740A/1742A:

Physical address = (Segment * 16) + Offset

The 386 processor, however has given rise to a large number of software products which use the 386 memory management feature to provide virtual 8086 operation. The address passed in ES:BX still appears valid to the BIOS, but the processor is not in fact in real mode, and normal segment arithmetic will not yield the correct physical location of the data buffer. This issue has been addressed by IBM® and Microsoft® in a specification known as Virtual DMA Services (VDS). This specification provides a method to the ROM BIOS for determining the physical location of a buffer given the selector:offset as well as its layout (it may not be contiguous). The AHA-1740A/1742A BIOS will fully support the VDS specification so that 386 memory management programs will be able to run without a driver as long as they are VDS compliant. In ISA Standard Mode, however, VDS will not be supported and a driver will be necessary to support VDS.

BIOS Command Return Codes

Any Int 13h request, upon completion, returns control to the requestor with a return code set in the carry flag and a status code placed in AH. The carry flag is set as follows:

CF=1	Error or unusual condition. Status is nonzero.
CF=0	Command completed normally. Status is zero.

Status code definitions returned in register AH, as well as the mapping from SCSI error conditions, are provided in the following table:

AH (Hex)	Definition
00	No Error: Operation completed successfully
01	Invalid Function Request: The Int 13h function code provided was not valid or the drive number was out of range.
02	Unable to Read Address Mark: One of the following additional sense codes (SCSI ASC) was presented in the sense information returned by the target: 12h - No AM Found on Data Field 21h - Illegal Logical Block Address
03	Write Protect Error: Returned SCSI ASC: 27h - Data Protect
04	Read Error: Returned SCSI ASC: 14h - No Record Found 16h - Data Sync Error
10	Uncorrectable ECC Error: Returned SCSI ASC: 10h - ID ECC Error 11h - Unrecovered Read Error

AH (Hex)	Definition
11	ECC Corrected Data Error: Returned SCSI ASC: 17h - Recovered Read Error without ECC 18h - Recovered Read Error with ECC
20	General Controller Failure: Returned SCSI ASC: 01h 03h 05h 06h 07h 08h 09h 1Bh 1Ch 1Dh 40h 41h 42h 43h 44h 46h 47h 48h 49h
40	Seek Operation Failed: Returned SCSI ASC: 15h - Seek Positioning Error 02h - No Seek Complete
80	Time-out: Host adapter not responding to BIOS
AA	Device Not Ready: Returned SCSI ASC: 04h - LUN not ready 28h - Unit Attention, Ready 29h - Unit Attention, Power on 2Ah - Unit Attention, Mode Select Change
BB	Undefined error occurred: A SCSI ASC other than those listed was returned by the target.
CC	Write Fault: Not returned by AHA-1740A/1742A BIOS
FF	Sense Operation Failed: An error occurred issuing the SCSI request sense command to the target.

Hardware BIOS Commands

(AH) = 00h - Reset Disk System
This function does nothing to SCSI drives. Regardless of drive number, this request is passed to the original Int 13h vector so that floppy and non-SCSI drives may be reset.

(AH) = 01h - Read Status of Last Operation
The status of the last operation performed is returned. The status is reset to zero.

(AH) = 02h - Read Desired Sectors into Memory
The sectors requested are read from the disk to system memory. A Read (Extended) command (SCSI Operation Code 28h) is used to execute this function.

(AH) = 03h - Write Desired Sectors from Memory
The sectors requested are written from system memory to the disk. A Write (Extended) command (SCSI Operation Code 2Ah) is used to execute this function.

(AH) = 04h - Verify Desired Sectors
The sectors requested are verified to be correctly written on the SCSI disk. A Verify command (SCSI Operation Code 2Fh) with the byte check bit set to zero is used to execute this function. If the verify function is not supported by the selected disk, a Read (Extended) command is used and the data is thrown away.

(AH) = 06 - Identify SCSI Devices
This is a special call that is used to return the first supported SCSI drive. If there are only SCSI drives, then the return value will be 80h. If there is a SCSI and a standard controller, then the return value will be 81h.

The ID of the first supported drive is returned in BL. If an error code is returned (C is set) on this call, it indicates that the SCSI adapter BIOS is not in the Int 13h chain at all. No SCSI drives are supported by the BIOS.

(AH) = 08h - Read Drive Parameters
A SCSI Read Capacity command is used to determine the maximum logical block of the selected SCSI drive. This information is then used to calculate the proper number of cylinders to be returned to the host system. The number of heads returned will always be 64 and the number of sectors per track will always be 32. The number of drives will reflect the value in 40:75 (system hard drive count). The capacity is rounded to the nearest full megabyte, and the cylinder count is returned as the number of megabytes (as each cylinder is a megabyte). The output of this function is defined as follows:

Register	Function
AH	Status of Operation
DL	Number of Hard Drives Supported by Int 13
DH	Maximum Value of Head Number = 63
CH	Low Byte of Cylinder Number
CL (Bits 7,6)	High Bits of Cylinder Number
CL (Bits 5-0)	Sector Number (1-based)
CF	Return Code

(AH) = 09h - Initialize Drive Pair Characteristics
This command does nothing to SCSI drives, since they are self-configuring.

(AH) = 0Ch - Seek
A Seek (Extended) command (SCSI Operation Code 2Bh) is used to perform this function. As the Seek command is not mandatory for SCSI, an invalid command error will not be reported back to the system, but instead the command will complete normally. Any other error will be reported as usual.

(AH) = 0Dh - Alternate Disk Reset
This function does nothing to SCSI drives. Regardless of drive number, this request is passed to the original Int 13h vector so that non-SCSI hard drives may be reset.

(AH) = 10h - Test Drive Ready
A Test Unit Ready command (SCSI Operation Code 00h) is used to execute this function.

(AH) = 11h - Recalibrate
A Rezero command (SCSI Operation Code 01h) is used to execute this function. As the Rezero command is not mandatory for SCSI compliance, an Invalid command error will not be reported back to the system, but instead the command will complete normally. Any other error will be reported as usual.

(AH) = 15h - Read DASD Type
A SCSI Read Capacity command is used to determine the maximum logical block of the selected SCSI drive. This information is returned to the host along with the DASD type of the target which will always be 03h for hard disk.

The output of this function is defined as follows:

Register	Function
AH	Status of Operation
DL	00h - Drive not present or invalid DL 03h - Fixed Disk Present 01h, 02h - Reserved
CX	Number of blocks on disk
CF	Return Code

The following function codes are not supported by the AHA-1740A/1742A BIOS:

(AH) = 05h Format Desired Cylinder
(AH) = 06h Format Desired Cylinder and Set Bad Sector Flags
(AH) = 07h Format Drive Starting at Desired Cylinder
(AH) = 0Ah Reserved
(AH) = 0Bh Reserved
(AH) = 0Eh Reserved
(AH) = 0Fh Reserved
(AH) = 12h Reserved
(AH) = 13h Reserved
(AH) = 14h Reserved
(AH) = 16h Reserved
(AH) = 17h Reserved
(AH) = 18h Reserved
(AH) = 19h Park Heads
(AH) = 1Ah Format Unit
(AH) = 1Bh-FFhReserved

An invalid command error is returned for any of these function codes.

Int 15h Functionality

After issuing an I/O command to the host adapter, the AHA-1740A/1742A BIOS will make use of the Int 15 Device Busy (function 90h) to inform the operating system that the BIOS is about to wait for a device.

When the AHA-1740A/1742A interrupts indicating that the I/O is complete, an Interrupt Complete (function 91h) will be issued by the BIOS indicating that the wait is complete.

Differences Between Operating Modes

- VDS is supported in Enhanced Mode only
- In EISA mode, the BIOS will scan for Int 13h devices

- In Standard Mode, disk devices must be installed sequentially starting at target 0

Multiple Adapter Support

When multiple SCSI adapters are installed, the BIOS should be enabled on all boards. Each BIOS is responsible for initializing the board on which it resides. This has the following advantages:

- Full 2KBytes of shadow RAM is available for each board
- Facilitates mixing of different versions of adapter in same system because each board is initialized by the BIOS belonging to that board

If you disable the BIOS on one of the boards (such as for driver development debugging), the system will use the default SCSI Device Configuration options. Any SCSI device configuration information saved by the EISA Configuration Utility (ECU) will be ignored.

During system boot, BIOSs load in order of the BIOS address, regardless of the EISA slot number. For example, with four host adapters with BIOSs at hex addresses of CC000, DC000, EC000, and D0000, the BIOSs will install in the order of CC000, D0000, DC000, and finally EC000.

In Standard Mode, you can install a maximum of four AHA-1740A/1742A/1744 host adapter cards. The limiting factor is the number of available ISA DMA channels (5, 6, 7, and 0). Each card must be set for a unique DMA channel, I/O port address, BIOS address, and interrupt channel.

The EISA architecture is capable of supporting up to 15 EISA Bus Master cards. In Enhanced Mode, it is therefore possible to install 15 AHA-1740A/1742A/1744 cards in an EISA system. The actual number is limited by the number of slots in your EISA system that support bus master and the number of other Bus Master cards used. Most users have the capability to install more AHA-1740A/1742A/1744 host adapter cards than can be used.

Although interrupts can be shared in Enhanced Mode, set each board to a unique interrupt for maximun performance. Use the ECU that came with your system to configure your system and any installed boards.

If using MCS ECU to change the interrupt selection when in Enhanced Mode, enter **Ctl+R** to change system resources when the **Host Adapter Interface Mode** selection is highlighted.

Refer to Chapter Three, *Installation* for further information.

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Chapter Eight

Device Drivers

DOS Operation without Drivers

The SCSI host adapter operates with very high performance characteristics using drivers that directly access its multitasking interface. In addition, the AHA-1740A/1742A/1744 series host adapters and their BIOSs support the Interrupt 13 interface used by MS-DOS®. The Adaptec BIOS supports only two hard disk drives total per system under MS-DOS without the use of special driver programs.

Standard Mode

If no standard hard disk drives (ST506/412, ESDI, or IDE) are installed in the host computer system, the SCSI drive at SCSI address 0, and LUN 0 (0:0) is used as drive *C*, the boot hard drive. If a drive is installed at SCSI address 1, LUN 0 (1:0), it will be used as drive *D*, the second hard drive. If one internal hard disk drive is installed in the computer system, that drive is assigned as drive *C*. In that case, the SCSI disk drive at address 0:0 will be assigned as drive *D*. If two internal hard disk drives are installed in the computer system, any SCSI disk drives can be accessed only by a special software driver.

Enhanced Mode

If no standard hard disk drives are installed, then a SCSI disk drive will be the boot hard drive *C*, and a second SCSI disk drive can be *D*. If one standard hard disk is installed, then that disk is the boot drive *C* and a SCSI disk drive can be used as *D*.

> Note
> In Enhanced Mode you can control which hard drives are installed by the BIOS via the EISA Configuration Utility (ECU). Although the default configuration is the same as Standard Mode, this can be modified. Refer to the *Enhanced Mode SCSI Configuration* section in Chapter Three, *Installation.*

System Configuration

Standard AT motherboard BIOS supports up to two floppy disk drives and two hard disk drives under DOS. DOS uses Interrupt 13 to access the floppy and hard disk services. Interrupt 13 refers to the first and second floppy disk as 0 and 1, respectively, and refers to the first and second hard disks as 80 and 81, respectively. Floppy disk drive 0 is assigned drive letter *A* and floppy disk drive 1 is assigned drive letter *B*. The first partition on hard disk drive 0 is assigned drive letter *C* and the first

partition on hard disk drive 1 is assigned drive letter *D*. If there is only one physical hard disk, *D* refers to the second partition on that drive. To permit the use of more than two hard disks in your system, Adaptec provides a software driver that is loaded via the *config.sys* file. (Refer to the section titled *Managers*)

AT computers or compatibles come with a *Setup* utility either on floppy diskette or included in the motherboard BIOS. This *Setup* utility is used to store the configuration of your system in low-power CMOS memory powered by a battery. It is, therefore, saved when your computer is turned off. The presence of standard hard disks should be reflected in this Setup utility. The presence of SCSI hard disks is *not* entered in *Setup*.

A standard hard disk refers to a disk that uses an ST-506/412 (MFM or RLL) or an ESDI interface. A standard hard disk controller refers to an adapter card that controls one or two standard hard disks and uses the standard AT hard disk register set 1F0 1F7 (i.e., WD 1003 or Adaptec ACB-2300 series).

To boot from a SCSI hard disk, the *Setup* utility must indicate that no hard disks are installed, must have a bootable SCSI hard disk at SCSI ID 0, and there must not be a floppy diskette in floppy disk drive *A*.

Low-Level Format

Most SCSI drives are shipped from the factory with a complete low-level format. In the rare event that your SCSI disk drive requires a low-level format, refer to that menu selection in the *ADL* utility (see *Low-Level Format* in Chapter Three, *Installation*). Unlike the AHA-1540/1542 family of host adapters, there is no low-level format utility built into the BIOS of the AHA-1740A/1742A/1744.

A newer low-level format utility (*154xfmt.exe*) that supports additional drives (magneto optical or erasable optical disk drives) is available on the Adaptec bulletin board. These utilities can be downloaded from the Adaptec bulletin board at (408) 945-7727 using 1200/2400/9600 Baud, 8 data bits, 1 stop bit, and no parity.

Installation and Initialization Under DOS

Hard disks must be initialized with the proper DOS structures by executing the DOS initialization programs *fdisk* and *format*.

Run the DOS *fdisk* program to partition the disk for the number of cylinders to be used by DOS. When using DOS 3.2 or under, it is generally a good idea to select one less cylinder than the maximum allowable per partition according to DOS. This eliminates the possibility of exceeding the 32 MByte limit. Activate the first DOS partition before leaving the *fdisk* program if it is to be the boot partition. If you are not sure if a DOS partition exists, use the menu entry in *fdisk* to display partition data.

CAUTION

If the drive you are using was previously formatted or partitioned with a different host adapter or disk controller, a DOS partition may already exist. If such a partition does exist it should be deleted and recreated using this host adapter. If this precaution is not followed, erratic system operation may result.

After the DOS partition has been created and activated, the drive is ready for a DOS format. Refer to your DOS manual for the format options that are available. If the system is going to boot from a SCSI disk, it is usually easiest to transfer the hidden system files to that disk during the DOS format by using the /S option:

```
format c: /s
```

The host adapter and SCSI disks are now ready for normal DOS operation.

Adaptec host adapter families(AHA-1520/1540/1640/AHA-1740) are DOS format compatible. Any disk initialized with one board can be connected to any other board with 100% compatibility (if the normal default translation scheme is used).

Managers

The AHA-1740A/1742A/1744 operates under DOS with up to two hard disk drives without a dedicated software driver through the onboard code embedded in the BIOS EPROM.

For optimal use of the features and benefits of this high-performance board, the following suggest that a driver is required:

- Use of a DOS application that runs in a Protected Mode (such as the Enhanced Mode used by Microsoft Windows®)
- Use of an operating system other than DOS
- Use of more than two hard disks
- Use of SCSI peripherals other than disk
- Any combination of the above

Adaptec has developed an architecture called Advanced SCSI Programming Interface (ASPI), which is available as a standard to all companies. ASPI divides the driver problem into two levels with a pass-through ASPI layer interface between. The driver component above the layer is called a module and is peripheral-specific. The driver component below the layer is called a manager and is host adapter-specific. Since the ASPI layer is a standard, different modules can work with different managers in a plug-and-play manner. Note that ASPI details are specific to a given operating system.

Only an overview of the managers available is provided. For complete information, refer to Adaptec's ASPI and ASW software documentation. Drivers available at time of printing include:

- ASW-1410 ASPI Manager and ASPI Disk Module for DOS
- ASW-210 ASPI Tape Module and Sytron SY-TOS™ for tape for DOS
- ASW-310 ASPI Tape Module and Sytron Sytos Plus™ for tape for DOS
- ASW-410 ASPI CD-ROM Module for DOS
- ASW-1420 ASPI Manager and Disk Module for OS/2
- ASW-220 ASPI Tape Module and Sytron SY-TOS for tape for OS/2
- ASW-1440 ASPI Manager and Disk Module for NetWare 286/386
- ASW-1450 ASPI Manager Enhanced Mode driver and improved Standard Mode driver for SCO Unix
- SCO Unix driver support in kernel
- SCO Xenix driver support in kernel
- Interactive Unix driver support in kernel
- Everex ESIX support in kernel
- Banyon Vines support

DOS Manager

A DOS manager is available that enables the AHA-1740A/1742A/1744 in Standard Mode to access additional SCSI devices on the SCSI bus. When operating under DOS, a device driver is needed to access more than two hard disks or to access tape devices and other types of SCSI peripherals. If all DOS operations will be confined to two SCSI disks or to one internal and one SCSI disk, a device driver is not needed. The onboard BIOS will successfully manage the SCSI disk drives in those cases.

See the documentation supplied with the DOS driver for instructions on the procedure for installing and enabling the driver program.

The following table shows how hard disks in a system are addressed:

Number of Hard Disks	C	D	Device Driver
2	1st Standard Disk	2nd Standard Disk	SCSI Devices
1	Standard Hard Disk	SCSI 0/0 Disk	Other SCSI Devices
0	SCSI 0/0 Disk	SCSI 1/0 Disk	Other SCSI Devices

The Adaptec DOS Manager supplies a number of services, including support for a special version of the *fdisk* program called *afdisk*. *afdisk* is needed to partition and high-level format the third, fourth, etc., hard disk in your system. Use DOS *fdisk* and *format* for your first two hard disks. *afdisk* performs both the *fdisk* and the *format* function for disk drives beyond the first two. In addition, the DOS driver supplies an interface suitable for ASPI modules such as the ASW-310, Sytos Plus by Sytron.

Microsoft Windows 3.0 and Extended Memory Managers

The use of high-performance 32-bit first-party (a.k.a. Bus Master) Direct Memory Access (DMA) on the AHA-1740A/1742A SCSI host adapters may require a driver to be compatible with software applications using the Protected Mode of the 80386 microprocessor. A common example of this is the Standard and Enhanced Modes of Microsoft Windows 3.0 (not to be confused with the Standard and Enhanced Modes of the AHA-1740 series host adapters), Quarterdeck QEMM™, and Qualitas 386MAX™. The driver provides either VDS (Virtual DMA Services) support or adds a buffer for double buffering to allow these Protected Mode programs to work.

The Adaptec DOS driver for the AHA-1740 series host adapters is *aspi4dos.sys* (1740 Standard Mode) and *aspiedos.sys* (1740 Enhanced Mode). Both of these drivers provide VDS support. The AHA-1740 BIOS also provides support for VDS when the AHA-1740 is configured for the Enhanced Mode.

VDS is a software specification developed by Microsoft and adhered to by the major software vendors. It allows the Bus Master host adapter to obtain the physical address to transfer data when the program is running in Protected Mode. When this method is used, a separate data buffer is not required (which takes up memory). Current versions of MS Windows 3.0, QEMM, QRAM™, 386MAX, MOVE'EM™, and Digital Research DOS conform to the VDS specification.

A separate buffer can also be allocated for those programs that do not conform to the VDS specification. Such a program is MS Windows 386 2.x. The buffer can be allocated with a switch on *aspi4dos.sys* (i.e., Device=aspi4dos.sys /w). Consult the *ASW-1410 User's Manual* for complete details. *scsiha.sys* is available for the AHA-1740 series adapters in Enhanced Mode.

The buffering device driver, *scsiha.sys*, is available free of charge from the Adaptec BBS at (408) 945-7727.

OS/2 Manager

The ASW-1420 OS/2 manager for the AHA-1740A/1742A/1744 allows the board to achieve its full multitasking potential under OS/2. Earlier versions of the manager were compatible with OS/2 v1.1. Versions will be available which will run under

v1.21 and v2.0 and support the LADDR specification. Tape support is also available via the ASW-220.

Novell NetWare Manager

The ASW-1440 Novell NetWare manager provides a vehicle for running the AHA-1740A/1742A/1744 in the latest industry-standard network operating system; NetWare 386, as well as the earlier NetWare 286.

Unix/Xenix Manager

By working closely with the software vendors, Adaptec has arranged for full driver support of the AHA-1740A/1742A/1744 in the kernel of SCO Unix/Xenix® and Interactive System's Unix. No other software drivers are necessary. Refer to the relevant vendor documentation.

- SCO Unix driver support in kernel
- SCO Xenix driver support in kernel
- Interactive Unix driver support in kernel
- Everex ESIX support in kernel
- Banyan Vines support

The ASW-1450 is the ASPI manager for the AHA-1740 series host adapters (Enhanced Mode) for SCO Unix. This driver is currently available. Eventually, Enhanced Mode AHA-1740 series support will be embedded into the SCO Unix kernel.

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Chapter Nine

SCSI Features

Initiator Mode SCSI Description

The AHA-1740A/1742A/1744 provides a very high performance SCSI interface connection. The host adapter meets the ANSI Standard X3T9.2/86-109 Revision 10c, describing the SCSI. The host adapter additionally meets conformance level 2 of the specification by implementing the following SCSI options:

- Accepts or manages the following messages:

  Command Complete

  Disconnect

  Message Reject

  Identify

  Save Data Pointer

- Performs arbitration

The following alternatives are selected for the AHA-1740A/1742A/1744 SCSI interface connection from those described by X3.131-1986:

- Single-ended SCSI driver/receivers are used.
- The termination power is supplied through a removable fuse, allowing the user to select whether termination power is provided by the host adapter at installation time.
- Parity is always generated. Parity checking can be disabled through the jumper selection.
- The Soft Reset option is always performed by the AHA-1740A/1742A/1744. If the user desires the Hard Reset, an interrupt servicing program that detects the SCSI Reset Detected interrupt in the Interrupt Flags Port must set the Soft Reset bit in the Control Port. This bit forces the host adapter to clear all SCSI-related operations, but does not require execution of the diagnostic functions. If the Soft Reset bit has been set, the host software must reinitialize the AHA-1740A/1742A/1744.
- Synchronous data transfer is supported. Negotiation for the synchronous transfer initiated by another SCSI device will be accepted by the

AHA-1740A/1742A/1744 at any time. If the jumper has been set to allow it, the AHA-1740A/1742A/1744 will also initiate synchronous data transfer negotiation when it has detected that such negotiation may be required.

- Multitasking is fully supported.
- Modify Data Pointers is supported to allow Zero Latency Read operations.

In addition to these SCSI functions, the SCSI Common Command Set at level 4B is also supported. While this document was never made a standard, it describes a widely available set of disk drive functions which are supported by the host adapter. The host adapter BIOS commands are all mapped into SCSI CCS commands to allow the proper support of all the most common SCSI disk drives. The adapter command Return Installed Devices also uses CCS commands to determine which devices are available.

The draft ANSI standard for SCSI-2 has been used as a reference for the implementation of all SCSI functions with the expectation that the host adapter will be fully compatible with the final version of the SCSI-2 standard. In particular, the processor-type device command set has been selected from the SCSI-2 manual for Target Mode operation.

Linked SCSI Commands

The AHA-1740A/1742A/1744 supports linking of SCSI commands in initiator mode. When the link bit in the SCSI command control byte is set, the target will present either a 0Ah or 0Bh message at command completion. The AHA-1740A/1742A/1744 uses the link pointer in a CCB to fetch another CCB. At the same time, the completed CCB status and address are stored in an MBI. If the target returns a 0Bh or 00h message, the AHA-1740A/1742A/1744 generates an interrupt to inform the host of the full MBI. If the target returns a 0Ah message, the MBIF interrupt is not posted until all linked commands are completed. The linked CCBs must address the same target and LUN since the target is not reselected.

Zero Latency Read Operation

The AHA-1740A/1742A/1744 implements zero latency operation through the use of modify data pointer messages. Zero latency can eliminate rotational latency, depending on the length of the data transfer, by supporting out of order data transfers. This advanced feature is currently only implemented on the ACB-4525Z SCSI-to-ESDI controller, and is supported transparently to the user.

After seeking to the target track, the drive will begin reading block IDs. If the first block ID is within range of the data transfer, but not the last block of the the data transfer, the drive will begin reading the subsequent blocks into its buffer. Before transferring data the drive will issue a Modify Data Pointer message to the AHA-1740A/1742A/1744. This supplies a positive argument that is added to the value of the current data pointer. The drive will now send this portion of the data transfer to the host. The drive will resume reading data into its buffer as soon as the first block of the data transfer is detected. Before sending this data to the host, the drive will issue a second Modify Data Pointer message to the AHA-1740A/1742A/1744 which

supplies a negative argument. This returns the data pointer to its original position. This guarantees that a data transfer of one track or less will never require more than a single revolution since data can now be transferred out of order.

SCSI Messages

The AHA-1740A/1742A/1744 host adapter supports a number of special messages in addition to the messages required by meeting conformance level 2. Those messages are described in detail in the SCSI specification, X3.131-1986, and in this section where they are used. The messages are summarized in the following table:

Function	Message	Cause
Standard Messages	Command Complete	Normal Sequencing
Error Management	Message Reject Bus Device Reset Abort	Invalid Messages Special CCB Special MBO
Disconnect/Reconnect	Identify Disconnect Save Data Pointer Restore Pointers	Normal Sequencing Normal Sequencing Normal Sequencing Special Sequencing/ZLR
Synchronous Transfer	Synchronous Data Transfer Request	Initialization Sequencing
Zero Latency Operation	Modify Data Pointers	ZLR Sequencing
Linked Commands	Linked Command Complete Linked Command Complete With Flag	Command Linking Command Linking

Target Mode SCSI Description

Initiator Conformance Level Requirements

Initiators that execute commands against an AHA-1740A/1742A/1744 operating in Target Mode are required to have the following conformance levels, as described in Appendix E of the SCSI Specification, ANSI X3.131-1986. Conformance must be present with respect to each of the following items:

- The initiator must use single-ended drivers.
- Termination power may optionally be provided by the initiator, but must meet the SCSI specification in both its over-current protection and its reverse current diode protection. The terminators may be installed on the AHA-1740A/1742A/1744 board or installed as in-line terminators at the cable connectors.
- The implementation of parity is optional, but desirable.
- The initiator may support either Hard Reset or Soft Reset. All attached devices must support the same type of reset.

- The initiator must meet the requirements of conformance level two. In particular, all LUN addressing must be performed by the Identify message, not by the LUN field in the CDB. Disconnection and reconnection must be supported.

- The initiator and target functions have the same SCSI ID.

Synchronous Transfer Support

Synchronous transfer is supported by the AHA-1740A/1742A/1744 in target mode without any instruction or support from the system processor. If an initiator invokes a synchronous transfer negotiation, the AHA-1740A/1742A/1744 will complete the negotiation of the required transfer offset and period. If the proper jumper has been set, the AHA-1740A/1742A/1744 will also attempt to negotiate synchronous transfer during the initial selection period of the first command after an initialization or after a SCSI reset.

SCSI Target Operation in Processor Target Mode

When the AHA-1740A/1742A/1744 has been set to respond in Processor Target Mode, the host adapter appears on the SCSI bus as a normal processor-type device as defined by the SCSI specification. From one to eight LUNs may be supported, depending on the LUN mask byte in the Enable Target Mode command. Five SCSI commands are accepted:

- Test Unit Ready

- Request Sense

- Inquiry

- Send

- Receive

All other commands are rejected with Check Condition status. The sense information will indicate a Sense Key of 05h (Illegal Request) with a Sense Code of 20h (Invalid Command Operation Code).

The commands that do not perform data transfer to or from the host are handled completely by the AHA-1740A/1742A/1744 with no CCB communication with the host system. Those commands are the Test Unit Ready, Request Sense, and Inquiry commands. The Send and Receive commands must have a CCB from the host with the proper direction bits, the proper initiator address, and the proper LUN number to complete the SCSI operation. The Send and Receive CCBs may be provided to the host adapter before a command is received on the SCSI or may be requested after the command is received.

Each time an initiator activates a command to the AHA-1740A/1742A/1744, an internal subchannel is activated to manage the command. The subchannel is dedicated to that particular LUN-initiator transaction until all operations associated with the

command are completed. Such operations include disconnection to obtain a CCB, pending error conditions, and linked operations. If all subchannels are busy, a selection to the AHA-1740A/1742A/1744 will result in the AHA-1740A/1742A/1744 accepting the command and then generating Busy status immediately. If this occurs, the initiator must reissue the command later.

Test Unit Ready

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Test Unit Ready Operation Code (00h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Reserved (00)							
5	Reserved (00)						Flag	Link

The Test Unit Ready command follows the SCSI specification in all respects. If the AHA-1740A/1742A/1744 has been initialized by the Enable Target Mode command to the Processor Target Mode, the command will finish normally with Good status and a Comand Complete message. The host adapter supports the normal definition of Unit Attention on the first operation after power-on, after a SCSI reset, or after a Bus Device Reset.

If a Test Unit Ready command is executed against an LUN which was not allowed by the Enable Target Mode command, then Check Condition status will be presented with sense data of Sense Key 5 (Invalid Request) and an Error Code of 25h (Invalid LUN). In order to minimize interference with peripheral devices. Test Unit Ready commands are issued only every 250 microseconds when waiting for a device to come ready.

Request Sense

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Request Sense Operation Code (00h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

If the AHA-1740A/1742A/1744 has returned Check Condition status to a previous command, the Request Sense command will obtain the sense information associated with the error. The sense information will be sent in the extended sense format according to the SCSI standard. The data format is given in the following table:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Error Code (70h or F0h)							
1	Reserved (0)							
2	00		ILI	0				
3-6	Information Bytes (Residue)							
7	Additional Sense Length (06)							
8-11	Reserved (00000000h)							
12	Additional Sense Code							
13	Additional Sense Code Qualifier							

The following errors are detected and presented by the AHA-1740A/1742A/1744 while operating in Processor Target Mode:

Error	Sense Key (hex)	Additional Sense Code (hex)
No Sense Data	00	00
Invalid Command Operation Code	00	20
Invalid LUN	05	25
Invalid Command Parameter	05	26
Power-Up Attention	06	29
Reset Attention	06	29
Interface Parity Error	0B	47
Initiator Detected Error	0B	48
Dumb Initiator	05	2B

One set of error data may be buffered for each initiator-LU association possible, up to a total of 56 sets of sense data. No Contingent Allegiance or Extended Contingent Allegiance state is established.

The Error Code (Byte 0) will be F0h if the residue field is valid and 70h if the residue field has no information.

The Incorrect Length Indicator (ILI) will be set if an incorrect data transfer length is executed as described in a section titled *Incorrect Length Management for Target Mode Operation*.

The residue is set equal to the transfer length requested in the initiator CDB minus the target host's specified data length specified as a 4-byte, two's complement number.

Inquiry

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Inquiry Operation Code (12h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

The Inquiry command provides the information necessary to uniquely identify the Adaptec AHA-1740A/1742A/1744 as a processor-type device. The information is returned in the SCSI-2 format. The following information is returned to any selecting initiator from any selected AHA-1740A/1742A/1744 logical unit:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Peripheral Qualifier			Processor Device Type (03h)				
1	Reserved (00)							
2	Reserved (00)					ANSI v(02)		
3	Response Data Format (02h)							
4	Additional Length (1Dh)							
5	Reserved (00)							
6	Reserved (00)							
7	0	0	0	Sync = 1	Link = 1	0	0	0
8-15	Vendor Identification (ASCII) ADAPTEC *bbb*							
16-31	Product Identification (ASCII) AHA-1540*bbbbbbbb*							
32-35	Product Revision Level (ASCII)							

If the Inquiry command is attempted against a logical unit that has not been enabled as a target, byte 0 is returned as 23h, indicating that the LUN is not installed, but would be a processor device if it were installed. The remaining bytes are returned normally.

If a length shorter than the required 36 bytes is specified by the Inquiry command, the number of bytes specified by the command is transferred. If a length longer than 36 bytes is specified, the command will only transmit 36 bytes.

Send

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Send Operation Code (0Ah)							
1	LUN (unused = 00)			Reserved (00)				
2	Transfer Length (MSB)							
3	Transfer Length							
4	Transfer Length (LSB)							
5	Reserved (00)						Flag	Link

The Send command has the format specified by the SCSI standard. The Send command transfers data from the initiator to the target. The information is placed in the area specified by the appropriate CCB. If an appropriate CCB has not already been provided to the host adapter by the host software, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI until the CCB is made available to the host adapter through the MBO protocol. An appropriate CCB must have the same initiator address, target LUN, and direction as is required to complete the command.

The transfer length in the Send command specifies the length in bytes of data that is sent during the Data Out phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in the section titled *Incorrect Length Management for Target Mode Operation.*

The CDB information is included in the returned CCB so that the receiving host programming can determine whether the information transmitted by the Send command was application data or asynchronous event notification data.

Receive

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Receive Operation Code (08h)							
1	LUN (unused = 00)			Reserved (00)				
2	Allocation Length (MSB)							
3	Allocation Length							
4	Alloaction Length (LSB)							
5	Reserved (00)						Flag	Link

The Receive command has the format specified by the SCSI standard. The Receive command transfers data from the target to the initiator. The information is taken from the area specified by the appropriate CCB. If an appropriate CCB has not already been provided to the host adapter host software, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI bus until the CCB is made available to the

host adapter through the MBO protocol. An appropriate CCB must have the same initiator address, target LUN, and direction as is required to complete the command.

The transfer length in the Receive command specifies the length in bytes of data that is sent during the Data In phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in the next section, *Incorrect Length Management for Target Mode Operation.*

Incorrect Length Management for Target Mode Operation

The messages transmitted using the Send and Receive commands are normally expected to have a length that has previously been agreed to by the initiator system software and by the target system software. If the transfer length specified by the command is equal to the transfer length specified by the CCB, normal operation takes place and no errors are posted.

If the transfer length specified by the initiator's command is shorter than the space defined by the target CCB, all data bytes expected and required by the initiator will be transmitted. The target AHA-1740A/1742A/1744 will indicate Good status on the SCSI at the end of the transfer. The target system's software, however, must be notified that the entire area of data defined by the CCB was not transmitted. A Target Status of Good will be presented in the returned CCB. At the same time, the Incorrect Length Indication bit (bit 5 of byte 2) will be set in the CCB Request Sense data area. Bytes 3 through 6 of the Request Sense data area will contain the residue in two's complement notation of the length requested in the initiator command minus the length of the data area defined by the CCB. In this case, the residue will be a negative number, since the requested length was less than the area specified by the CCB. The HA status stored in the CCB will be 12h, indicating a Data Over/Under Run. The MBI Status Byte will be set to 04h to indicate that the CCB was completed with an error.

If the transfer length specified by the initiator's command is longer than the space defined by the target CCB, only those bytes contained within the CCB's data transfer area will be transmitted. The target AHA-1740A/1742A/1744 must indicate, with an error condition to the initiator, that not all the requested bytes could be transferred. The target AHA-1740A/1742A/1744 presents a SCSI status of Check Condition at the end of the data transfer. The Request Sense information transmitted to the initiator as a result of an immediately following Request Sense command indicates that an Incorrect Length Indication is present by setting bit 5 of byte 2. Bytes 3 through 6 of the Request Sense information transmitted to the initiator will contain the residue in two's complement notation of the length requested in the initiator command minus the length of the data area defined by the target CCB. In this case, the residue will be a positive number, since the requested length was greater than the available area. The target system's software must also be notified that the transfer length requested by the initiator exceeded the assigned buffer area. A Target Status of Check Condition will be presented in the returned target CCB. A Host Status of 12h will be returned indicating a Data Over/Under Run. At the same time, the information that will later be posted to the initiator by the Request Sense command will be posted to the target system in the CCB Request Sense data area. This includes both the Incorrect Length Indicator and the Residue. The MBI Status Byte will be set to 04h to indicate that the CCB was completed with an error.

Aborting Target Mode Commands

The target host may abort a command by sending an MBO command of 02h to the host adapter. If execution of the command has not already been completed, the CCB will be aborted and a MBI Status of 02h will be returned to the host. Otherwise, an MBI status of 03h will be returned.

The initiator may also abort commands by sending an abort message to the target. All CCBs, either received or requested from the target host for the current initiator and LUN, and corresponding to commands received from that initiator, will be aborted. An MBI status of 03h will be aborted. Any CCB provided by the target host for which a corresponding initiator command has not been received will not be aborted.

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Chapter Ten

Problem Determination

Self Diagnostic Capability

The AHA-1740A/1742A/1744 executes self diagnostics upon power-up or after a Hard Reset. These diagnostics test the CPU operation, perform a sum check on the EPROM, and check the data transfer paths on the board. The host system has the option of exercising more extensive diagnostics involving reads and writes to memory.

The red light emitting diode (LED) on the host adapter indicates the result of the self diagnostic process. When power is first applied to the board, the LED turns on. If the board is operating normally, the light will soon go off and stay off until SCSI or I/O port activity is requested by the host. If the board is not operating correctly, a flash code number is flashed on the LED to indicate which test failed. The flash code number is indicated by a series of one to three closely spaced flashes followed by a longer pause. The flash code is repeated continuously until the board is powered off, reset, or repaired. The SCSI interface should be disconnected if these diagnostic tests are being run for fault isolation purposes. At least one set of terminators must remain installed or the LED will stay on, indicating that the AHA-1740A/1742A/1744 is receiving an active RST signal. Continuous execution of the diagnostics can also be forced by inserting the diagnostic jumper (pin pair 2 in jumper J1). The flash code and associated failure modes are indicated in the following table.

Flash Code	Possible Meanings of Flash Code
LED Remains On	Host adapter control processor inoperative/terminators missing or not powered or card enable has not been asserted after reset.
1 Flash	RAM test failed.
2 Flashes	AIC-6251 SCSI protocol chip verification failed.
3 Flashes	FIFO write/read data path test failed.
Continuous Flashes	EEPROM has not been programmed.

If any of these failure conditions is identified, the host computer should be powered-down, the host adapter removed, and the host adapter inspected for physical damage. Such damage can include EPROMs that are not correctly installed or not firmly seated, broken wires, missing or damaged components, or conductive debris on the board. If no such physical damage is found, the AHA-1740A/1742A/1744 should be returned for repair.

All boards are fully tested, burned in, cleaned, and inspected before they are shipped. Care should be taken to keep the board in its protective conductive wrapping until it is installed. With these simple precautions, mechanical damage can normally be avoided.

Indicators

The red LED on the AHA-1740A/1742A/1744 is used to provide the fault isolation information described above. In addition, the LED indicates when the host adapter is performing activities on the host interface and the SCSI interface. The LED is such a useful activity indicator that a connector is made available on the host adapter to allow the cable to an externally visible LED to be attached.

As an activity indicator the LED is turned on from the time an adapter command is transmitted to the host adapter until the HACC interrupt is generated to indicate that the adapter command is complete. In addition, the LED will be turned on whenever SCSI bus activity is occurring. This is roughly the same period of time the SCSI BSY signal is present on the SCSI bus. If the light stays on when no activity is expected to be present on the bus, it is possible that the bus is hung, the processor has failed, unexpected activity is occurring, or the SCSI cables are incorrectly installed. If the SCSI cables are installed reversed, the host adapter is forced into a solid SCSI reset state which halts normal operation.

Problems Detected During Operation

The information in this section is not intended for routine users of the AHA-1502B/1542B. It is intended to provide a reference for programmers preparing device drivers, error recovery procedures, and error information presentation programs.

Operation of the I/O Port interface is controlled and monitored by host system software. Two bits in the Status Port (Base + 0), described in the *Control and Status Port* section in Chapter Four, *Hardware Functional Description*, are provided to indicate unusual conditions in the host adapter.

Internal Diagnostic Failure (Status Port, bit 6)
This bit indicates that the self-testing process after either a Hard Reset or a power-on operation was terminated by an error condition. The error indicates that a critical failure was found in the AHA-1740A/1742A/1744 control circuitry or data paths. The error should be presented to the host video display to indicate that diagnostic actions are required. The diagnostic action uses the host adapter diagnostic flash codes to determine if the AHA-1740A/1742A/1744 is failing. The host system should be powered off, then opened so the LED can be observed. All SCSI cables, both external and internal, should be removed from the host adapter. The system should then be powered on. If the LED flashes once and turns off, the host adapter has passed its diagnostics and should be accessible again. If the LED flashes one of the error flash codes, the AHA-1740A/1742A/1744 should be replaced. If the LED remains on and does not turn off, the host adapter is not able to begin operation at all. The host system may be holding the AHA-1740A/1742A/1744 in the reset state or the host adapter may have failed or the card may not have been enabled. To distinguish these two cases, the AHA-1740A/1742A/1744 should be replaced and the new host adapter operation should be verified. Be sure to power-down the host system when removing or replacing the host adapter. If the diagnostics indicate that the AHA-1740A/1742A/1744 must be replaced, it should be sent to an authorized service facility for repair.

Invalid Host Adapter Command (Status Port, bit 0)
This bit is set to indicate that a command or parameter transmitted to the host adapter was invalid. This is an indication that the host software, usually an operating system, special application program, or device driver, has generated an invalid request. The responsible programming organization should be notified so that the invalid sequence or parameter can be corrected.

HA Status Error Indications and Corrective Actions

The host adapter status indications, in addition to indicating several normal completion states, indicate three general groups of errors. One set describes software errors in the requests made to the host adapter. Even though most of these errors are caused by software design problems, the AHA-1740A/1742A/1744 may need to be replaced as an isolation step, since there exists a small chance that hardware failures in the AHA-1740A/1742A/1744 cause the appearance of a software error.

A second set describes errors detected by the host adapter firmware in the host adapter hardware. The most likely failing component in this case is the AHA-1740A/1742A/1744, although certain system or cable failures may generate the appearance of a host adapter hardware error.

A third set describes the appearance of unexpected or incorrect sequences executed by the attached SCSI devices. In this case, the cables are the most likely failure point, with the peripheral device second and the AHA-1740A/1742A/1744 third. The host adapter status code should be returned to the host video display to indicate to the operator what errors have occurred and under what conditions the errors occurred.

The following table describes those host adapter status indications that indicate an error.

Number	Type	Error	Description and Corrective Action
11h	SCSI	No	Selection Time Out: The SCSI attempted to select a device that was not installed or that did not respond to selection due to a power, parity or addressing failure. Verify correct address values set to SCSI devices. Verify that SCSI cable routing includes the required devices. Verify SCSI cable integrity by replacement of cables. Verify that SCSI Selection Time-Out value has been correctly established by Adapter command.
12h	Host	No	Data Over Run/Under Run: Data length or direction specified by CCB did not agree with the data length actually provided by the attached peripheral device. Often a normal error or accompanied by a check condition indicating transfer truncation. Verify program requested correct length or direction. Verify peripheral provided expected data length, number of blocks, or block length.
			Continued

Number	Type	Error	Description and Corrective Action
13h	SCSI	Yes	Unexpected Bus Free: The target dropped BSY without executing the proper messages first. This normally indicates that the BSY and/or other portions of the SCSI bus failed or that the target encountered such an invalid sequence that no recovery was possible. Some targets may have sense information available to qualify the error condition. Verify SCSI cable integrity. Verify SCSI cables are all properly connected. Replace SCSI cables. Replace peripheral. Replace AHA-1740A/1742A/1744.
14h	SCSI	Yes	Target bus phase sequence failure: The initiator detected an invalid phase or an invalid phase sequence. If this occurs, it is likely that the host adapter forces a SCSI reset on the bus as the first phase of the recovery process. Verify SCSI cable integrity. Verify SCSI cables are all properly connected. Replace SCSI cables. Replace peripheral. Replace AHA-1740A/1742A/1744.
15h	Host	Yes	MBO Command Byte invalid: This indicates a software failure or bug in the host's development of the MBO entry. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-1740A/1742A/1744. Replace the host computer system. Contact the software developer for design support.
16h	Host	Yes	Invalid CCB Operation Code: This indicates a software failure or bug in the host's development of the CCB. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-1740A/1742A/1744. Replace the host computer system. Contact the software developer for design support.
17h	Host	Yes	Linked CCB does not have same LUN: This indicates that the host software generated an invalid combination of link commands. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-1740A/1742A/1744. Replace the host computer system. Contact the software developer for design support.
18h	Host	Yes	Invalid Target Direction Parameters received from Host: This indicates that the host software generated an invalid Target Direction Parameter. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-1740A/1742A/1744. Replace the host computer system. Contact the software developer for design support.
19h	Host	Yes	Duplicate CCB Received in Target Mode: This indicates that the host system was not keeping correct management information for target mode operation and incorrectly generated a second CCB identical to one already active. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-1740A/1742A/1744. Replace the host computer system. Contact the software developer for design support.

Number	Type	Error	Description and Corrective Action
1Ah	Host	Yes	Invalid CCB Parameter or Segment List: A segment list was presented to the host adapter with a zero length segment or invalid segment boundaries. An invalid CCB parameter was presented to the host adapter. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-1740A/1742A/1744. Replace the host computer system. Contact the software developer for design support.

SCSI Error Indications and Corrective Actions

Error conditions detected by SCSI peripherals usually cause a Check Condition status byte to be presented. When this is presented, the host adapter automatically retrieves the sense information from the SCSI peripheral by executing a Request Sense command according to the SCSI standard. The information returned is mapped for single-threaded BIOS operation into the categories of error conditions described in the *Mailbox In Definition* section of Chapter Five, *Standard Mode Firmware Description.* For multitasking (mailbox) operation, the information returned is made available in the area allocated for sense data. In either case, an intelligent attempt is made by most operating systems to retry the operation at least one time. Such retry operations may require the management of queued operations that have already started execution. This attempt to retry the operation is rarely successful, since SCSI peripheral devices have very extensive automatic retry and correction mechanisms designed to be executed before the error information is returned in the first place.

Since it is rare that such an operation is successful, the host software and operating systems should make every attempt to make available key information about the error which can be analyzed by the system operator or customer engineer. In small systems, it may be sufficient to present the important sense data together with the command that created the error. Some simpler systems may perform a preliminary analysis of the error information and generate a code or descriptive text that describes the error and indicates the corrective action. In very complex systems, a logging process may take place, allowing a customer engineer to analyze the data at some future time. In all systems, such information is very important for host program verification and for system integrity verification, even if the designers choose not to make the information available to any system users other than the design and maintenance engineers.

The SCSI Sense Data is generally self descriptive. The errors can be mapped into four major categories, each category with its own diagnostic procedure.

The first category includes those errors caused by incorrect command or parameter bytes or by incorrect sequences of commands. These errors typically are presented only during the early development stages of an operating system or device driver, since a properly operating program will not generate invalid commands.

The second category includes those sense codes associated with peripheral status presentation. Such sense codes are not truly errors, in that they inform the host program of an unusual but not unexpected condition. Such sense codes include indications that a device is not ready, that the device has just become ready, that a

device has reached the end of its media (End of Tape or Blank Check), or that the expected data length and actual data length differed. These sense codes are normally used by the device driver to execute the correct operation in response to the condition. Such sense codes are not normally presented to the system user except as text that requests some action. As one example, an End Of Tape condition may require the system user to replace the tape cartridge.

The third category of errors points to a particular hardware failure in the peripheral device or its supporting electronics. Such error conditions usually require the adjustment, repair, or replacement of the peripheral device or some of its components. In some cases, the error condition may also indicate possible cable or host adapter failures. These errors must be exposed to the system user so that the proper actions can be taken.

The fourth category of errors points to a media failure in the peripheral device. Such errors include bits that cannot be recovered from magnetic media and imperfections in the surface of optical media. Most such errors are recovered using the extensive retry and correction algorithms programmed into the peripheral device. In some peripheral device technologies, the errors may be caused by noise conditions or by marginal electronic failures in the read or write path. Those rare errors that cannot be recovered usually indicate that some data important to the operating system or application has been lost. The system must make this error information available to the system user so that the system user can replace the media or recover the data from a backup copy as required. In addition, logging of errors that were successfully recovered by the peripheral device is often useful as an indicator of the overall reliability of the device or of the requirement for periodic maintenance.

Problems Detected During Installation

This section may be useful to correct problems related to installation. The information in this section is included in the *Host Adapter Installation Guide*.

If the system will not boot from the floppy diskette drive after initial hardware installation, the following items should be checked:

- AHA-1740A/1742A/1744 internal diagnostics: The LED on the AHA-1740A/1742A/1744 should come on briefly at system power-up. If the LED begins to blink at regular intervals then the host adapter has detected an internal failure and should be returned for repair or replacement to the place of purchase. A message may also be posted to the screen.

- If the AHA-1740A/1742A/1744 LED and the SCSI drive LED are always on, the SCSI cable's pin 1 orientation has probably been reversed between the host adapter and the drive. See the *Installation* section in Chapter Three, *Installation.*

- Is the AHA-1740A/1742A/1744 BIOS message displayed on the screen? If not, the AHA-1740A/1742A/1744 BIOS is not being recognized by the system.

  Check for BIOS address conflicts between the AHA-1740A/1742A/1744 and other option boards.

  Try a different BIOS address. See the *System Configuration* section in Chapter Three, *Installation.*

  Change the BIOS wait state jumper. See the *System Configuration* section in Chapter Three, *Installation.*

- If the message:

  host adapter not found at port 330h

  is displayed, check the port address setting. Also verify that the SCSI cable is correctly installed. A forced SCSI reset caused by an inverted or displaced internal SCSI cable may cause the problem. See the *System Configuration* section in Chapter Three,
  Installation.

Problems booting the system from a SCSI drive:

- Make sure that both standard hard disks are mapped out of the system.
- Make sure that the SCSI boot drive address is set to SCSI ID 0:0. Check the drive installation manual for information about setting the SCSI ID for that device. The *Return Installed Devices* utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.
- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.
- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing Chapter Three, *Installation.*
- Power should be cycled off and on after changing any values on a host adapter, *Setup* program, or SCSI device to be sure that a DOS format operation has been successfully completed.
- Make sure that the SCSI bus is properly terminated.
- Make sure that the intended boot disk has an active DOS partition and a DOS format. See Chapter Three, *Installation* and the DOS manual for more information.
- Check the cabling.

Problems using a SCSI drive as drive *D* with a standard hard disk as drive *C*:

- Make sure that the second hard disk is mapped out of the system.

- Make sure that the SCSI drive to be used as drive *D* is set to SCSI ID 0:0. Check the drive manual for information on setting the SCSI ID for that device. The *Return Installed Devices* utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.

- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.

- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing Chapter Three, *Installation.*

- Power should be cycled off and on after changing any values on a host adapter, *Setup* program, or SCSI device to be sure that the new initial values are loaded.

- Make sure that the SCSI bus is properly terminated. See Chapter Three, *Installation.*

- Make sure that the disk has a DOS partition and a DOS format. See Chapter Five, *Standard Mode Firmware Description* and the system DOS manual for more information.

- Check the cabling.

Problems using a SCSI drive as drive *D* with another SCSI drive as drive *C*:

- Make sure that both standard hard disks are mapped out of the system with the AT *Setup* program.

- Make sure that the SCSI drive to be used as drive *D* is set to SCSI ID 0:1 or 1:0. Check the drive manual for information on setting the SCSI ID for that device. The *Return Installed Devices* utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.

- Power should be cycled off and on after changing any values on a host adapter, *Setup* program, or SCSI device to be sure that the new initial values are loaded.

- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.

- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing Chapter Three, *Installation.*

- Make sure that the SCSI bus is properly terminated. See Chapter Three, *Installation.*

- Make sure that the disk has a DOS partition and a DOS format. See Chapter Three, *Installation* and the DOS manual for more information.

System works erratically. Hangs or the host adapter can't always find the drives.

- Check SCSI parity for consistency.
- Check termination.
- Check cable length and integrity.
- If host adapter and drive light remain on during a hang condition, make sure that the SCSI drive conforms to the *Common Command Set Revision 4B* (CCS 4B).
- If only the host adapter LED remains on during a hang, it is probably a host adapter system interface problem. The system may not be capable of First-Party DMA transfers. Check with the system manufacturer for information.

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Chapter Eleven

Glossary

Glossary of Terms

Adapter Command
A command transmitted to the host adapter using the Command/Data Out Port and the Data In Port. The commands are sequenced using the Control Port, the Status Port, and the Interrupt Flag Port. Abbreviated as IOCP command.

AEN
See Asynchronous Event Notification

AHA-1540
Adaptec host adapter for connecting SCSI devices to the PC AT backplane bus. The AHA-1740A/1742A/1744 is an enhancement of the AHA-1540.

AHA-1540B
The enhanced high-performance Adaptec host adapter for connecting SCSI devices to the PC AT backplane bus.

AHA-1542B
The enhanced high-performance Adaptec host adapter for connecting SCSI devices and standard IBM-compatible floppy disk devices to the PC AT backplane bus.

AHA-1740A/1742A/1744
Either the AHA-1740A/1742A or the AHA-1744 or both.

ASPI
Advanced SCSI Programming Interface. A software architecture which permits device modules to migrate across different hardware by communicating with the hardware through a passthrough interface to a manager written to the specific hardware.

Asynchronous Event Notification
A process by which a target can send unsolicited sense information to an initiator using the Send command in order to inform the initiator about the occurrence of an important unusual occurrence.

Asynchronous Data Transfer
Data transfer performed by the SCSI interface involving the interlocking of a signal to the initiator (REQ) and a signal to the target (ACK) such that each step of the data transfer protocol must occur before the next step can begin. Characterized by a low data rate and independence of external timing constraints, including cable length and circuit response times.

AT Bus
The Industry Standard Architecture bus.

Bus Device Reset
A SCSI message that clears all activity in the target to which it is addressed.

Byte
An eight-bit unit of data. An octet. A byte is normally the smallest addressable unit of a memory and the unit of transfer on the SCSI.

CCB
See Command Control Block

CCS
See Common Command Set

CDB
See Command Descriptor Block

Command Control Block
A software object prepared by the host microcomputer software for the host adapter to provide it all the control information it needs to execute a SCSI command. Abbreviated CCB.

Command Descriptor Block
A block of information passed across the SCSI bus to provide the command, parameter, and address information necessary for the target to execute the desired functions. Prepared by the host software and placed in the CCB to be passed to the target by the host adapter. Abbreviated CDB.

Common Command Set
A defacto standard SCSI command set for communication with hard disk drives. The Common Command Set (CCS) is the basis for the SCSI-2 command set for all types of peripheral devices.

Configuration
The operation of configuring a device on the EISA bus through access of registers in the device by the host. It replaces the method of using jumpers common on ISA bus devices.

Control Microprocessor
An integrated circuit computer used to execute the software that controls the host adapter's operation.

Device Driver
A program that is linked with, or attached to, an operating system to map the software interface of the operating system to the requirements of attached peripheral devices and host adapters. Under ASPI, the main component associated with the board is known as a Manager.

DMA
See Direct Memory Access

Differential
A term referring to the electrical characteristics of the signals used on the SCSI bus interface. Differential signals occupy two conductors with a positive (+) and negative (-) polarity component of the signal. This minimizes the effect of common mode signal noise and allow the SCSI bus to operate reliably over greater distances at a higher speed.

Direct Memory Access
A mechanism that allows hardware control of the transfer of streams of data to or from the main memory of a computing system. The mechanism may require setup by the host software. After initialization, it automatically sequences the required data transfer and provides the necessary address information.

EISA
Extended Industry Standard Architecture. A superset standard of the 8- and 16-bit ISA standard which allows 32 bits of data to be transferred across the bus at up to 33 MBytes/second.

Enhanced Mode
The operation mode of the AHA-1740A/1742A/1744 to take full advantage of the addressing range and register set available under EISA. It is not compatible with earlier revisions of ASPI managers and drivers.

EEPROM
Electrically-Erasable Programmable Read Only Memory. An integrated circuit used to store the host adapter firmware, which allows both mode download and firmware upgrade while in-circuit.

EPROM
Erasable Programmable Read Only Memory. An integrated circuit used to store the host adapter BIOS.

FIFO
First In/First Out. A queuing order in which items are removed from the queue for execution in the same order in which they are placed in the queue. An integrated circuit that buffers data in such a manner that each byte placed in the buffer is removed from the buffer in the same order.

Firmware
The software that controls and manages the host adapter. It is *firm* as opposed to *soft* because it is designed into the host adapter and cannot be modified by the user.

IBM PC AT Compatible
Any computer system that emulates exactly the IBM PC AT and that uses an ISA backplane bus.

Industry Standard Architecture
The IBM PC AT functions have been duplicated by a number of manufacturers. All the IBM PC AT compatible machines use a backplane bus that very closely emulates the function of the backplane bus of the PC AT. Because of the broad usage of this bus structure, it has become known as the Industry Standard Architecture bus, even though there is no presently accepted standard for the bus.

Initiator
A SCSI device that requests an operation to be performed by another SCSI device (the target). The initiator provides all the command information and parameters required to perform the operation, but the details of the operation are actually sequenced by the target.

ISA
See Industry Standard Architecture

Host
A microcomputer in which a host adapter is installed. The host uses software to request the services of the host adapter in transferring information to and from peripheral devices attached to the SCSI bus connector of the host adapter.

Host Adapter
A hardware printed circuit board that installs in a standard microcomputer backplane and provides a SCSI bus connection so that SCSI devices can be connected to the microcomputer. A host adapter is *intelligent* if it has a simple high-level software interface to the microcomputer. A host adapter is *dumb* if the microcomputer must directly manage the SCSI protocol using the microcomputer processor.

Logical Unit
A physical or virtual device addressed through a target.

Logical Unit Number
An encoded three-bit identifier for a logical unit.

LU
See Logical Unit

LUN
See Logical Unit Number

Mailbox In
An area in main memory assigned by the host microcomputer software for communication with the host adapter. The host adapter places status and pointer information in entries in the Mailbox In (MBI) to indicate to the host microcomputer what operations have been completed or what information must be obtained from the host microcomputer.

Mailbox Out
An area in main memory assigned by the host microcomputer software for communication with the host adapter. The microcomputer software places commands and pointer information in entries in the Mailbox Out (MBO) to indicate what operations should be started by the host adapter.

Manager
The component of a driver which is specific to a particular board architecture and presents a standard ASPI pass-through interface for use by the peripheral-specific component of the driver, known as a module.

MBI
See Mailbox In.

MBO
See Mailbox Out.

Multitasking Operation
The execution of commands in such a way that more than one command is in progress at the same time, allowing the system to take advantage of overlapping activities by using resources that are temporarily not required for other operations. More than one program or more than one portion of a program may be operating in parallel.

PC AT
A family of small computers sold by IBM, also called the Personal Computer/AT family of computers. The name is trademarked by IBM.

RAM
Random Access Memory. Memory of which any byte can be accessed directly in a single memory cycle. Information can be read from and written to the memory.

SCB
SCSI Control Block. The mechanism used in emulation mode to transfer control information to and from the board. This is equivalent to the mailbox in/out system used in Standard Mode.

SCSI
Small Computer System Interface.

SCSI ASC
SCSI Additional Sense Code. Byte 12 of the extended sense information. Provides a standardized description of the condition described by the sense information.

SCSI Device
A device attached to a Small Computer System Interface bus cable. The device may be an initiator, a target, or capable of both types of operation. The device may be a peripheral device, a host device, or a device mixing both roles.

Single-Ended
A term referring to the electrical characteristics of the signals used on the SCSI bus interface. Single-ended signals occupy a single conductor and are references to a common ground carried on the cable between the SCSI components attached.

Single-Threaded Operation
Operation of the computing system such that only one program can be operating or active at a time. The computing system must wait until all resources are available before starting an operation and cannot start another operation until the first one is completed. No overlapping of latencies or program operation occurs.

Standard Mode
The operation mode of the AHA-1740A/1742A/1744 to allow software drivers written for the AHA-1540/1640 family to operate fully on the board. This has no performance limitations but does not allow addressing beyond 16 MBytes nor access to several EISA registers.

Synchronous Data Transfer
A method of data transfer on the SCSI bus involving clocking data on to the bus with a fixed-length fixed-frequency strobe pulses. The acknowledgements may be delayed several clock periods from the data requests. Synchronous data transfer can be used only for data transmission on the SCSI bus. It is prohibited for command, message, and status transmission.

Sync Data Transfer Negotiation
The message exchange between the initiator and the target that allows the negotiation of the data transfer frequency and delay between requests and acknowledgements required for synchronous data transfer. Once negotiated, synchronous data transfer parameters remain unchanged until certain reinitialization activities occur.

Target
A SCSI device that performs an operation requested by an initiator. The target may be a peripheral device performing a service for an initiator. The target may also be a host adapter performing a processor-type device service for an initiator.

Word
A 2-byte (16-bit) unit of data.

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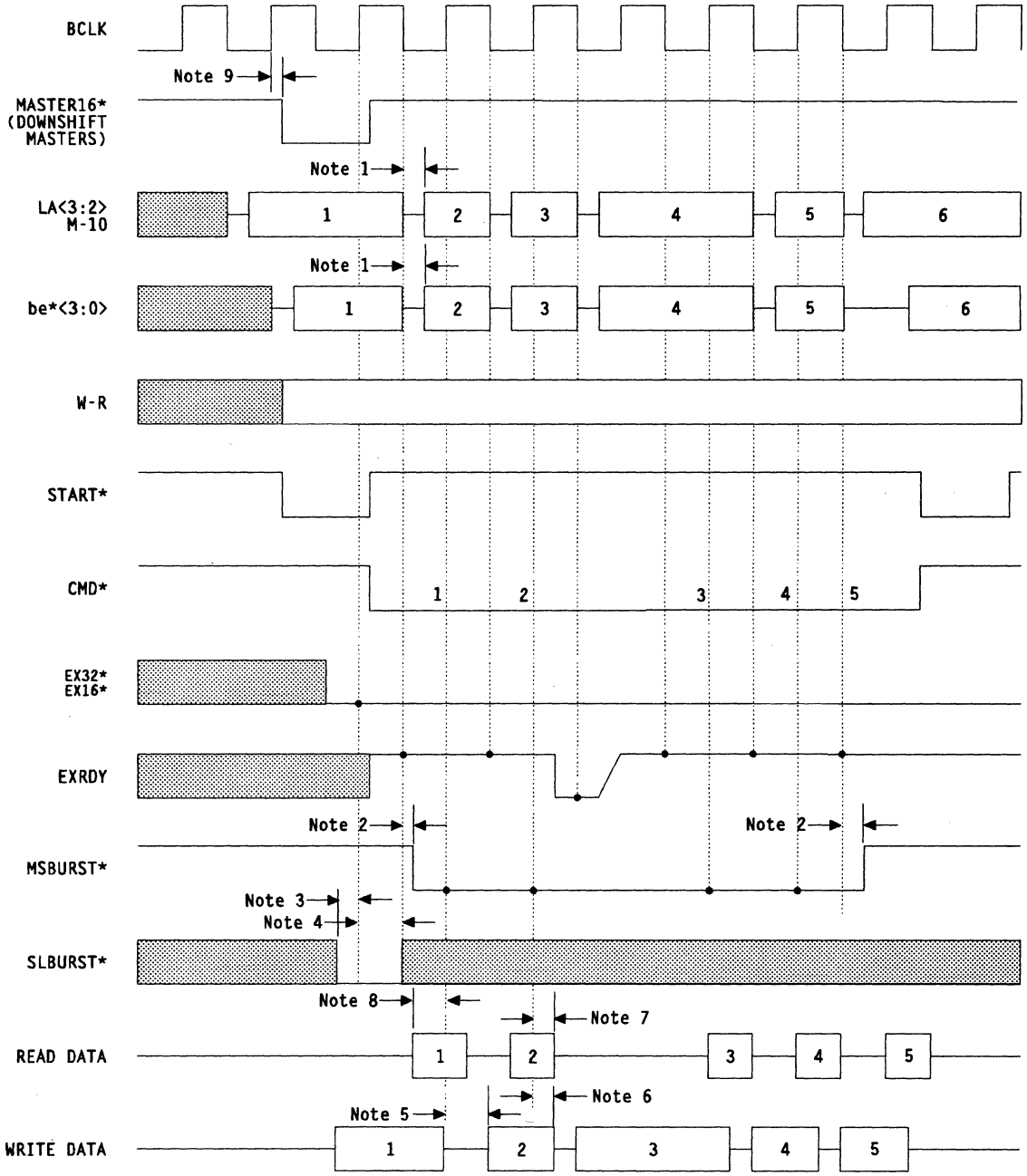
Appendix A

Memory Cycle Timing Diagram

AHA-1740A/1742A/1744 Timing Diagram



EISA Access

Number	Definition
1	EISA Standard Access (Start of Burst)
2	EISA Burst Access
3	EISA Burst Access with One Wait State
4, 5	EISA Burst Access
6	EISA Standard Access

Parameter Table

Note	Description	Minimum[1]	Maximum[1]
1	LA addr, BE* <> delay from BCLK falling	2.0	45.0
2	MSBURST* delay from BCLK falling	0.0	35.0
3	SLBURST* setup to BDLK rising	15.0	
4	SLBURST* held from BCLK rising	25.0	
5	Data delay from BCLK rising (write)	2.0	4.0
6	Data hold from BCLK rising (write)	2.0	
7	Data held after BCLK rising (read)	2.0	
8	Data setup to BCLK rising (read)	15.0	
9	MSTR16* delay from BCLK rising (downshift)	2.0	40.0

[1] nanoseconds

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Appendix B

Connector Pinout

Internal Connector Pin Assignments

AHA-1740A/1742A (Single-Ended)

Signal Name	Pin	Pin	Signal Name
Ground	1	2	-DB(0)
Ground	3	4	-DB(1)
Ground	5	6	-DB(2)
Ground	7	8	-DB(3)
Ground	9	10	-DB(4)
Ground	11	12	-DB(5)
Ground	13	14	-DB(6)
Ground	15	16	-DB(7)
Ground	17	18	-DB(P)
Ground	19	20	Ground
Ground	21	22	Ground
Ground	23	24	Ground
Open	25	26	Term Power (Fused)
Ground	27	28	Ground
Ground	29	30	Ground
Ground	31	32	-ATN
Ground	33	34	Ground
Ground	35	36	-BSY
Ground	37	38	-ACK
Ground	39	40	-RST
Ground	41	42	-MSG
Ground	43	44	-SEL
Ground	45	46	-C/D
Ground	47	48	-REQ
Ground	49	50	-I/O

AHA-1744 (Differential)

Signal Name	Pin	Pin	Signal Name
Ground	1	2	Ground
+DB(0)	3	4	-DB(0)
+DB(1)	5	6	-DB(1)
+DB(2)	7	8	-DB(2)
+DB(3)	9	10	-DB(3)
+DB(4)	11	12	-DB(4)
+DB(5)	13	14	-DB(5)
+DB(6)	15	16	-DB(6)
+DB(7)	17	18	-DB(7)
+DB(P)	19	20	-DB(P)
DIFFSENS	21	22	Ground
Reserved	23	24	Reserved
Term Power (Fused)	25	26	Term Power (Fused)
Reserved	27	28	Reserved
+ATN	29	30	-ATN
Ground	31	32	Ground
+BSY	33	34	-BSY
+ACK	35	36	-ACK
+RST	37	38	-RST
+MSG	39	40	-MSG
+SEL	41	42	-SEL
+C/D	43	44	-C/D
+REQ	45	46	-REQ
+I/O	47	48	-I/O
Ground	49	50	Ground

External Connector Pin Assignments

AHA-1740A/1742A (Single-Ended)

Signal Name	Pin	Pin	Signal Name
Ground	1	26	-DB(0)
Ground	2	27	-DB(1)
Ground	3	28	-DB(2)
Ground	4	29	-DB(3)
Ground	5	30	-DB(4)
Ground	6	31	-DB(5)
Ground	7	32	-DB(6)
Ground	8	33	-DB(7)
Ground	9	34	-DB(P)
Ground	10	35	Ground
Ground	11	36	Ground
Ground	12	37	Reserved
Open	13	38	Term Power (Fused)
Ground	14	39	Reserved
Ground	15	40	Ground
Ground	16	41	-ATN
Ground	17	42	Ground
Ground	18	43	-BSY
Ground	19	44	-ACK
Ground	20	45	-RST
Ground	21	46	-MSG
Ground	22	47	-SEL
Ground	23	48	-C/D
Ground	24	49	-REQ
Ground	25	50	-I/O

AHA-1744 (Differential)

Signal Name	Pin	Pin	Signal Name
Ground	1	26	Ground
+DB(0)	2	27	-DB(0)
+DB(1)	3	28	-DB(1)
+DB(2)	4	29	-DB(2)
+DB(3)	5	30	-DB(3)
+DB(4)	6	31	-DB(4)
+DB(5)	7	32	-DB(5)
+DB(6)	8	33	-DB(6)
+DB(7)	9	34	-DB(7)
+DB(P)	10	35	-DB(P)
DIFFSENS	11	36	Ground
Reserved	12	37	Reserved
Term Power (Fused)	13	38	Term Power (Fused)
Reserved	14	39	Reserved
+ATN	15	40	-ATN
Ground	16	41	Ground
+BSY	17	42	-BSY
+ACK	18	43	-ACK
+RST	19	44	-RST
+MSG	20	45	-MSG
+SEL	21	46	-SEL
+C/D	22	47	-C/D
+REQ	23	48	-REQ
+I/O	24	49	-I/O
Ground	25	50	Ground

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Appendix C

Register Reference

System Register Reference

Expansion Board IDs

Definition	Signal	EISA Slot	Write/Read
Host ID 0	HID0	zC80	R
Host ID 1	HID1	zC81	R
Host ID 2	HID2	zC82	R
Expansion Board Control	EBCTRL	zC84	W/R
BMIC Registers		zC88-zC9F	W/R

Group 1

Definition	Signal	EISA Slot	Write/Read
I/O Port Address	PORTADDR	zCC0	W/R
BIOS Address	BIOSADDR	zCC1	W/R
Interrupt Definition	INTDEF	zCC2	W/R
SCSI Definition	SCSIDEF	zCC3	W/R
Bus Definition	BUSDEF	zCC4	W/R
Floppy Definition	FLOPDEF	zCC5	W/R
Reserved 1	RESV1	zCC6	W/R
Reserved 2	RESV2	zCC7	W/R
Mailbox Out Byte 0	MBOXOUT0	zCD0	W/R
Mailbox Out Byte 1	MBOXOUT1	zCD1	W/R
Mailbox Out Byte 2	MBOXOUT2	zCD2	W/R
Mailbox Out Byte 3	MBOXOUT3	zCD3	W/R
Attention	ATTN	zCD4	W/R
Group 2 Control	G2CNTRL	zCD5	W/R
Group 2 Interrupt Status	G2INTST	zCD6	R
Group 2 Status	G2STAT	zCD7	R
Mailbox In Byte 0	MBOXIN0	zCD8	R
Mailbox In Byte 1	MBOXIN1	zCD9	R

Continued

Definition	Signal	EISA Slot	Write/Read
Mailbox In Byte 2	MBOXIN2	zCDA	R
Mailbox In Byte 3	MBOXIN3	zCDB	R
Group 2 Status 2	G2STAT2	zCDC	R

Control Group 1 (Programmable Location)

Definition	Signal	ISA Port Address	Write/Read
Control Port	CNTRL	Base Address + 0	W
Status Port	STATUS	Base Address + 0	R
Command/Data	CMD/DAT	Base Address + 1	W/R
System Interrupt	INTRPT	Base Address + 2	R

Local Control Registers

Definition	Signal	Address (hex)	Write/Read
PORTB	PORTB	00E2, 00E3	W/R
PORTD	PORTD	0104	R
PORTPL	PORTPL	0152	W
PORTPH	PORTPH	0153	W
Local Status Port	LSTAT	2000	W
Local Command/Data Register	LCMDDAT	2001	W/R
Local Interrupt Register	LINTRG	2002	W
Local Auxiliary Status Register	AUXSTAT	2003	R
Clear Reset	CLRRST	2003	W
Local Port Address	LPORTADDR	3000	R
Local BIOS Address	LBIOSADDR	3001	R
Local Interrupt Definition	LINTDEF	3002	R
Local SCSI Definition	LSCSIDEF	3003	R
Local Bus Definition	LBUSDEF	3004	R
Local Reserved 0	LRESV0	3005	R
Local Reserved 1	LRESV1	3006	R
Local Reserved 2	LRESV2	3007	R
Local Mailbox Out Byte 0	LMBOXOUT0	3010	R
Local Mailbox Out Byte 1	LMBOXOUT1	3011	R
Local Mailbox Out Byte 2	LMBOXOUT2	3012	R
Local Mailbox Out Byte 3	LMBOXOUT3	3013	R
Local Mailbox In Byte 0	LMBOXIN0	3014	W
Local Mailbox In Byte 1	LMBOXIN1	3015	W

Definition	Signal	Address (hex)	Write/Read
Local Mailbox In Byte 2	LMBOXIN2	3016	W
Local Mailbox In Byte 3	LMBOXIN3	3017	W
Local Group 2 Control	LG2CNTRL	3018	W
Local Group 2 Status	LG2STAT	3019	R
Local Group 2 Interrupt Status	LG2INTST	301A	W
Local Group 2 Attention	LATN	301C	R
Local Expansion Board Control	LEXBCTL	3020	W
Local Expansion Board Control	LEXBCTL	3020	R
Local Data Register	LDAT	4000	W/R
Local Index Register	LINDX	4001	W/R
Local Control/Status	LCONSTAT	4002	W/R
SCSI Control	SCSICNTRL	4004	W
EISA Word Count LSB	ECOUNTL	4005	W
EISA Word Count MSB	ECOUNTH	4006	W
SCSI Registers		5000-500F	W/R
On-Board RAM		8000-FFFF	W/R

Appendix D

EISA Free-Form Data

SCSI Subsystem Data Structure

SCSI Device	Byte	Bit Definitions
0	0	Bit 7 - Allow removable media in BIOS disk scan Bit 6 - More than 1 LUN supported Bit 5 - Parity check enable Bit 4 - Send start command Bit 3 - Synchronous negotiation enable Bit 2 - Disconnection enable Bit 1 - Ignore error if device not present Bit 0 - Enable disk BIOS support
0	1	Bits 7-3 Reserved Bits 2-0 Maximum synchronous transfer rate 000 - 10.0 MBytes/second 001 - 6.67 MBytes/second 010 - 5.0 MBytes/second 011 - 4.0 MBytes/second 100 - 3.33 MBytes/second
1	2	Same as Byte 0
1	3	Same as Byte 1
2	4	Same as Byte 0
2	5	Same as Byte 1
3	6	Same as Byte 0
3	7	Same as Byte 1
4	8	Same as Byte 0
4	9	Same as Byte 1
5	10	Same as Byte 0
5	11	Same as Byte 1
6	12	Same as Byte 0
6	13	Same as Byte 1
7	14	Same as Byte 0
7	15	Same as Byte 1
Reserved	16-47	Reserved for future use

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