7064
SN 0056
SN 0062

CO_2 Interferometer
T. Carlstrom x3552

Aeon Systems Inc.

Model 7064
64K Word Memory

Model 7064
64K Word Memory Module

INSTRUCTION MANUAL

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CHANGE RECORD

Rev.	Date	Change
A	10/84	Initial Release
B	5/85	Add Address Switches table (Section 3.2) and Module ID Command (Section 3.4)

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1. INTRODUCTION

1.1 Description

The Model 7064 is a static random access memory (RAM) module packaged in a single-width CAMAC module. All address, control and data signals connect to the 7064 through the auxiliary connector at the back of the module. The only connections to the crate's backplane are for power.

The 7064 stores 65,536 (64K) words of 12-bits each. The base address of each 7064 module can be set separately to any multiple of 64K within a total address space of 1M locations (20-bit address) by means of switches on the module. This allows flexibility for integrating the 7064 into data acquistion systems or for building large memories out of 7064 modules.

Since the memory array in the 7064 is completely static, it requires no controller overhead to maintain the data.

1.2 Front Panel Indicators

Indicator lights on the front panel show the currently selected base address by showing its most significant four bits. To calculate the base address, add the values next to each illuminated indicator. For example, if all indicators are lit, the base address is

```
 512K  (where 1K=1024)
+256K
+128K
+ 64K
------
 960K
```

or 983,040. The locations on this 7064 module have addresses from 960K to 1024K-1.

The red LOAD indicator lights whenever the 7064 executes a write operation. The UNLOAD indicator lights whenever it executes a read operation.

2. INSTALLATION

2.1 Unpacking and Inspection

The packing material in which the 7064 is shipped is specially designed to protect the module from physical damage and from damage due to electrostatic discharge. Aeon Systems recommends that you save this material in case it becomes necessary to ship the module back for repair.

Upon unpacki g, inspect the module closely for shipping damage. This coulu include broken or missing components, loose screws, etc. If you find such damage, notify the carrier immediately.

2.2 Insertion in the Crate

Inserting the 7064 module into a CAMAC crate is not difficult, but should be done with care to avoid damage to the module. Use the following procedure:

Step	Procedure
1	The 7064 can be inserted in any slot in the crate. As a practical matter, it should be mounted as close as possible to the modules reading and writing data to minimize cable length.
2	Insert the card edge into the slots and slide the module back until it stops against the connectors at the back of the slots.
3	Press firmly against the front panel of the module to seat the connector. Press only until the mounting screw on the front panel can be threaded into the hole on the front of the crate.
4	Finish seating the module into its connector by tightening the mounting screw.

3. OPERATION

3.1 Bus Connections

Data, control and address connections are made to the 7064 through a connector in the free use area at the back of the module. The connector is a 36-conductor, double-sided card edge connector with conductors on .1" centers. The conductor assignments are as follows:

Conductor	Function	Conductor	Function
1B	AB 19	1A	AB 1
2B	AB 18	2A	AB 0
3B	AB 17	3A	GND
4B	AB 16	4A	DB 11
5B	AB 15	5A	DB 10
6B	AB 14	6A	DB 9
7B	AB 13	7A	DB 8
8B	AB 12	8A	DB 7
9B	AB 11	9A	DB 6
10B	AB 10	10A	DB 5
11B	AB 9	11A	DB 4
12B	AB 8	12A	DB 3
13B	AB 7	13A	DB 2
14B	AB 6	14A	DB 1
15B	AB 5	15A	DB 0
16B	AB 4	16A	GND
17B	AB 3	17A	WRITE
18B	AB 2	18A	READ

AB - Address Bit
DB - Data Bit
WRITE - Data Load Strobe
READ - Data Unload Strobe

3.2 Address Switches

The base address selector switches are located on the left side of the module (as viewed from the front) near the top center. The switches set the most significant four bits of the 20-bit base address. The 7064 decodes the remaining 16 bits to select the correct memory location.

To set the base address, first express the required address as a 20-bit binary number. Note that the base address must be an integral multiple of 64K, so that the 16 least significant bits are always 0. The left-most switch (numbered 1) corresponds to the most significant bit, while switch 4 corresponds to the fourth most significant bit. For each bit, set the corresponding switch OFF if the bit is 1 or ON if the bit is 0. Table 3-1 shows the possible base address switch settings.

TABLE 3-1
Base Address Switch Settings
1K=1024 Words

Base Address	SW1	SW2	SW3	SW4
0	ON	ON	ON	ON
64K	ON	ON	ON	OFF
128K	ON	ON	OFF	ON
196K	ON	ON	OFF	OFF
256K	ON	OFF	ON	ON
320K	ON	OFF	ON	OFF
384K	ON	OFF	OFF	ON
448K	ON	OFF	OFF	OFF
512K	OFF	ON	ON	ON
576K	OFF	ON	ON	OFF
640K	OFF	ON	OFF	ON
704K	OFF	ON	OFF	OFF
768K	OFF	OFF	ON	ON
832K	OFF	OFF	ON	OFF
896K	OFF	OFF	OFF	ON
960K	OFF	OFF	OFF	OFF

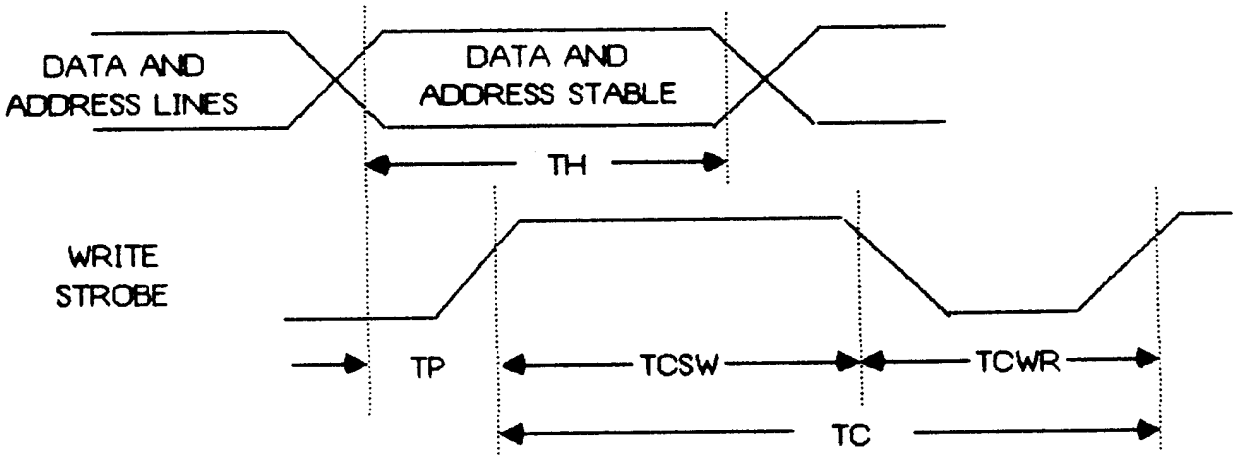
3.3 Timing

A. Write (Load) Cycle

To write data into the 7064, the address and data lines must be held stable for 130 ns, minimum. After a 30 ns delay, assert the WRITE strobe high (>3 V) for 100 ns to execute the write operation. A recovery delay of 50 ns, minimum, must follow the cycle before another read or write operation is attempted. This timing sequence is summarized in Figure 3-1.

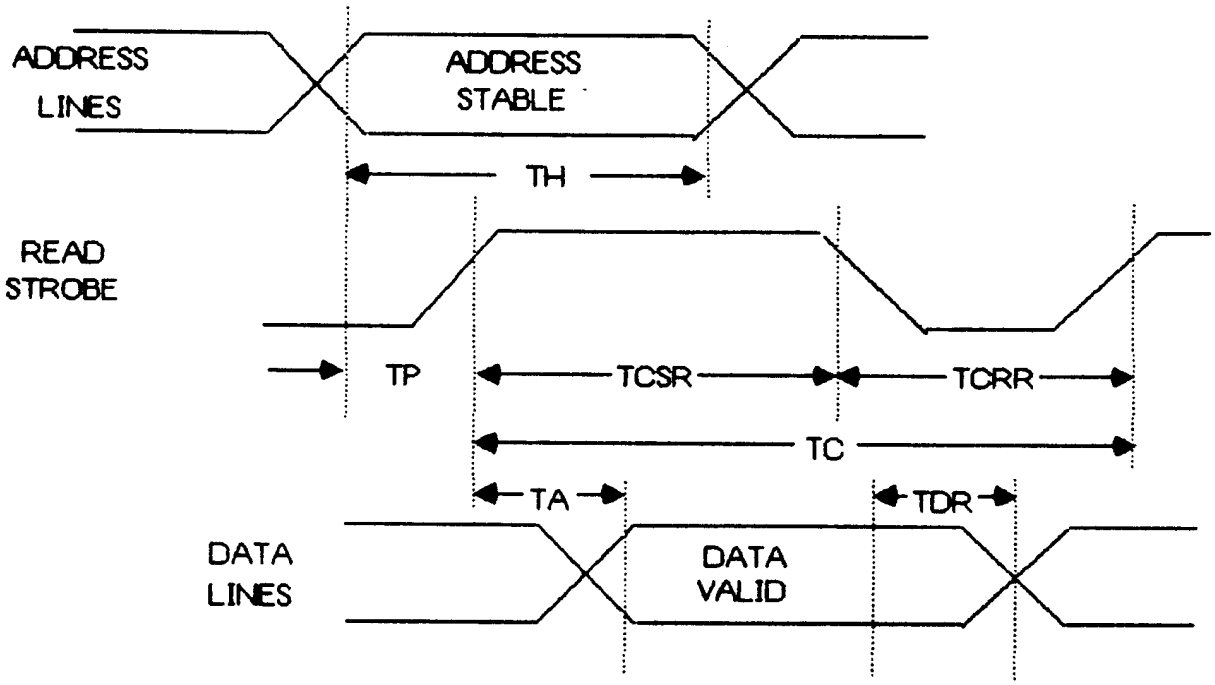
B. Read (Unload) Cycle

To read data from the 7064, the address lines must be held stable for 130 ns, minimum. After the address becomes stable, assert the READ strobe high for a minimum of 100 ns, to execute the read operation. Read data become stable on the bus 130 ns after the READ strobe. After removing the READ strobe, there must be a delay of at least 50 ns before asserting it again. The minimum time between the beginning of a read cycle and the beginning of the subsequent read or write cycle is 200 ns. Figure 3-2 summarizes this timing sequence.



Symbol	Interval	Time
TP	Set Up Time	30 ns
TH	Data and Address Hold Time	130 ns
TCSW	Write Strobe Pulse Width	100 ns
TCWR	Write Strobe Recovery Time	50 ns
TC	Write Cycle Time	200 ns

Figure 3-1. Write Cycle Timing Diagram



Symbol	Interval	Time
TP	Set Up Time	30 ns
TH	Hold Time	130 ns
TCSR	Read Strobe Pulse Width	100 ns
TCRR	Read Strobe Recovery Time	50 ns
TC	Read Cycle Time	200 ns
TA	Access Time	130 ns
TDR	Data Recovery Time	30 ns

Figure 3-2. Read Cycle Timing Diagram

3.3 Chip Designations

As a troubleshooting aid, Table 3-1 lists the RAM chip designations associated with each memory bit position.

Table 3-2
RAM Chip Designations by Bit Position

ADDRESS RANGE	CHIP NO. BITS 0 TO 3	CHIP NO. BITS 4 TO 7	CHIP NO. BITS 8 TO 11
0 TO 4095	U23	U39	U56
4096 TO 8191	U24	U40	U57
8192 TO 12287	U25	U41	U58
12288 TO 16383	U26	U42	U59
16384 TO 20479	U22	U38	U55
20480 TO 24575	U21	U37	U54
24576 TO 28671	U20	U36	U53
28672 TO 32767	U19	U35	U52
32768 TO 36863	U18	U34	U51
36864 TO 40959	U17	U33	U50
40960 TO 45055	U16	U32	U49
45056 TO 49151	U15	U31	U48
49152 TO 53247	U14	U30	U47
53248 TO 57343	U13	U29	U46
57344 TO 61439	U12	U28	U45
61440 TO 65535	U11	U27	U44

3.4 CAMAC Command

The 7064 Memory Module's ID may be read by a CAMAC command. The ID number is 964 and can be read with the following command:

F(6)•A(0) Read Module ID (Module ID = 964)