AES plus

AES-Plus
Maintenance &
Service Manual

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SECTION 1

INTRODUCTION

1. GENERAL DESCRIPTION

A text editor is presently the most effective means of converting spoken, handwritten and recorded information into typed copy for distribution. This conversion is called Word Processing. In essence, a text editor permits all information to be entered, recorded, verified, modified and edited before committing it to paper.

The AES-PLUS Text Editor brings new dimensions to the world of Word Processing. It is compact, consisting mainly of a CRT console and printing unit. It is also programmable, allowing the feasability o creating customer oriented software packages.

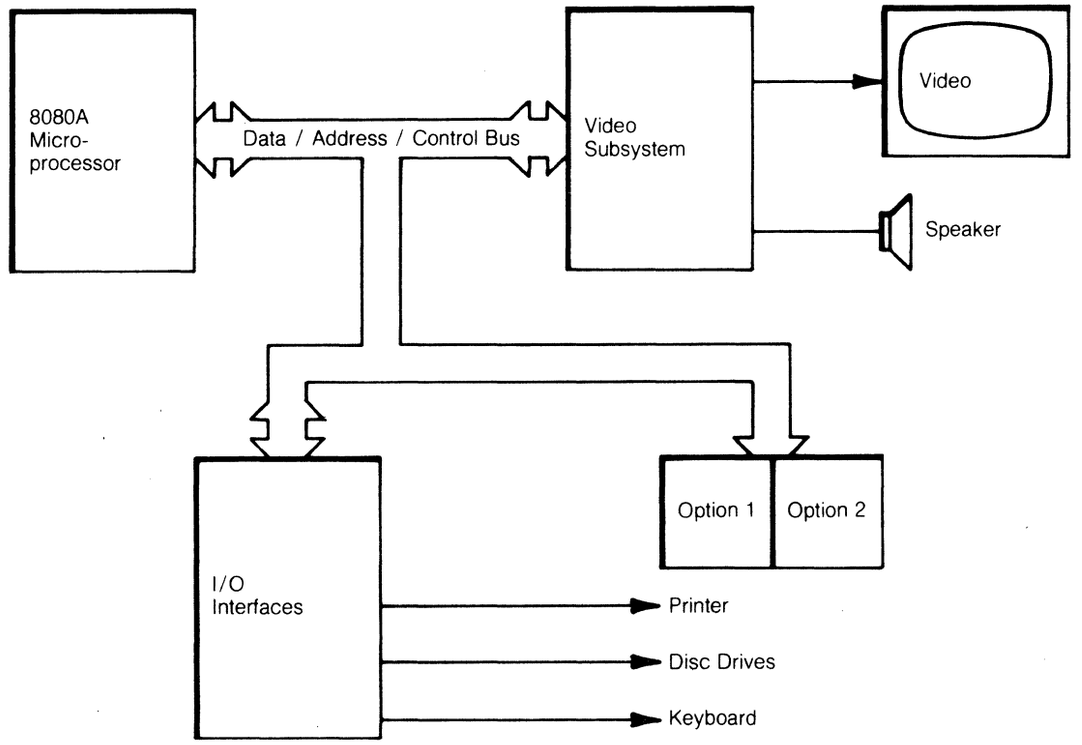
The AES-PLUS is designed around an integrated processor, the Intel 8080A, and utilizes the latest technological breakthroughs such as 16K dynamic random access memories. The design of this text editor was largely made possible by the use of software controlled functions, having an instruction memory with 32K of capacity, thus minimizing the electronics to the point where only three 12.5 x 7.5 inch printed circuit boards are needed. Two additional boards may also be added to the system as expansions where several options may be chosen.

2. SCOPE OF MANUAL

This manual contains all the necessary information on the AES-PLUS and provides maintenance procedures and field support. It contains five chapters where Chapter I outlines the Text Editor in its specifications and gives the Theory of operation. Chapter II gives a detailed description of each printed circuit board including the switching power supply. In Chapter III, a complete mechanical description is given with the aid of photographs and legends; a set of component data sheets also occupies that section.

Chapter IV gives general unpacking and installation procedures at the customer's site and also provides field maintenance and fault isolation with the aid of a diagnostic program. Chapter V concludes the manual with a detailed description of each peripheral unit.

Figure 1 AES plus Block Diagram



SECTION II

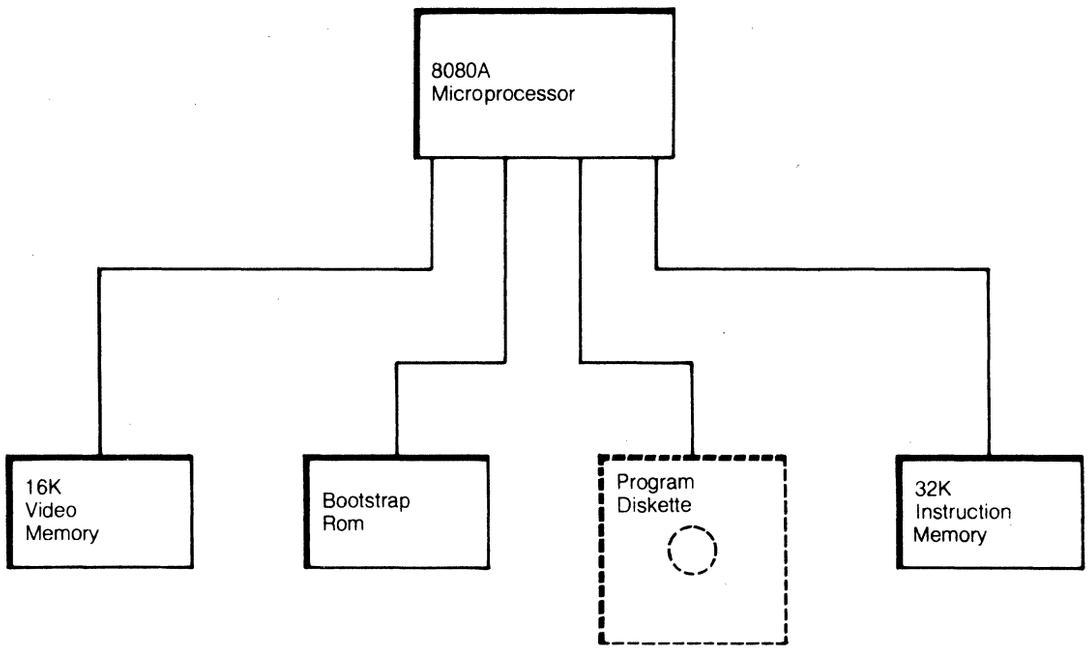
AES-PLUS TECHNICAL SPECIFICATIONS

CONFIGURATION:	Stand alone word processing system consisting of: one cabinet containing a CRT, a keyboard two magnetic mini-diskette drives and all the electronics. A high-speed printer completes the whole system.
CRT DISPLAY:	35.56 centimeter (14 inch) viewable diagonally; 100 sq. in. dark non-glare screen with P39 green phosphor.
VIDEO SCREEN CAPACITY:	2240 characters including control lines and 2080 without control lines.
KEYBOARD STRUCTURE:	One electronic keyboard consisting of standard typewriter keys and one 15-key function cluster for filing and editing.
CHARACTER REPERTOIRE:	66/70 keys for alphanumeric upper or lower case characters. Up to 53 special symbols.
CHARACTER SPACING:	Mono spaced.
SCANNING:	262.5 lines in both interlaced A and B fields (312.5 lines for Europe).
VIDEO REFRESH RATE:	60 per second (50 for Europe).
STANDARD DISPLAY FORMATS:	28 lines of up to 80 characters in a single row.
CURSOR:	Half-tone software-controlled rectangle.
CURSOR MOVEMENTS & SCROLL:	Up to 15 different movements.
FUNCTIONS:	Video format, Edit, File, Printer, dual-disc and special purpose functions.
SIZE & WEIGHTS:	52.0cm (20.5")D x 48.26cm (19")H x 60cm (24") W. 30.9 kgs (68 lbs).
POWER REQUIREMENTS:	Approximately 400 watts.
OPERATING TEMPERATURE:	0°C to 40°C.
RELATIVE HUMIDITY:	10% to 90% non condensing.
ELECTRONICS:	Standard MOS and TTL, SSI, MSI and LSI circuit
VIDEO CONSOLE CONTROLS:	Screen brightness and bell volume.
C.P.U:	8080A Integrated processor.
MEMORIES:	Instruction Memory 32K x 8. Bootstrap 512 x 8. Video Memory 16K x 9.

- The Video Memory: This memory has a capacity of 16K x 9 bits and employs 16K RAM devices. It is used to maintain keyboarded characters on the CRT at their specific location. Since a video page needs only 8K of memory, the current video page may be displayed while the additionnal 8K could contain a "background" page or any page desired. (This "background page" has not yet been included in the operating system).

NOTE:
Several ROM memories are also found in the video subsystem; these are primarly used to generate algorithms related to character locations in the video memory.

Figure 2 Memory Subsystem



2.3 Video Subsystem: The Video Subsystem consists of the CRT, the Video Memory and associated control circuits. (FIG. 3)

a) The CRT Monitor and the Video Memory: The CRT monitor displays 28 lines of information with 80 character locations per line. The top line is called "Control Line" and consists of a half-tone band on which appear messages and status indicators of the operating AES-PLUS Text Editor. The second line is the format line on which are displayed format information, tab locations, margin setting, indentation etc. The control line is not scrollable on the video screen and occupies the first Y address of the video memory. The format line, however, is scrollable from left to right on the video page, in other words it follows the video window throughout the video page in the X direction only and occupies the second Y address in the video memory.

The visible page of the display is an XY coordinate matrix. The X coordinate is divided into 80 character slots. The Y coordinate is divided into 28 lines. Thus the XY matrix determines one particular character location on the CRT by a specific number in X and Y. Each character slot is then allocated one position in the video memory and the correct character will always be displayed on the screen at the proper location.

SECTION III

THEORY OF OPERATION

This section describes the theory of operation of the AES-PLUS Text Editor. A more detailed description is given in Chapter II, where the printed circuit boards are analyzed individually.

1. CONFIGURATION

The AES-PLUS consists of 6 subsystems: the integrated microprocessor, the memories, the video, the magnetic storage, the printer and the optional communication package.

2. FUNCTIONAL DESCRIPTION

2.1 The 8080A Microprocessor: This device is a self-contained integrated CPU in a 40-pin DIP package and is designed to be interfaced with memories and I/O peripherals of all types. It is a "buss" oriented system where CPU and I/O peripherals read the data buss at certain predetermined periods. In the AES-PLUS Text Editor, it controls every operation performed from the keyboard for editing and filing of texts displayed on the video screen.

Every function is stored in a RAM memory from a program diskette when the machine is first turned on. All these functions are, however, in the form of instruction bytes which are decoded by the microprocessor. The process of loading a program into a RAM is called "BOOTSTRAP" and introduces flexibility in the machine operation. Several program Option packages are available and are tailored to meet customers requirements.

The 8080A Microprocessor Module is interfaced with a Programmable DMA Controller which handles all data transfers from memory to floppy disc. The Microprocessor communicates with the video subsystem and the printer via the address buss, the data buss and five control lines.

All I/O decoding is performed from the address buss and allows the addressing of individual peripherals. Provisions have also been made to allow for two additional expansion boards, for instance the Communications or the IBM MAG Card interfaces.

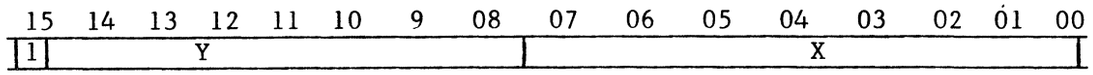
2.2 The Memory Sub-System: The AES-PLUS employs three different memories for its operation and they are:

- The Instruction Memory.
- The "Bootstrap" Memory.
- The Video Memory.

- The Instruction Memory: This memory has a capacity of 32K x 8 bits and employs 16K RAM devices. The instructions are loaded from a program diskette when the AES-PLUS is first turned on; they are then processed by the 8080A CPU, which executes these in one machine cycle of 2 microseconds. These instructions are also part of a repertoire of commands associated with the filing and editing functions of the Text Editor.

- The "Bootstrap" Memory: This memory is a ROM and consists of a 512 x 8-bit device. It contains all the program loading instructions used when the text editor is first turned on.

The video memory has a capacity of 16K x 9-bits where the lower 7-bits define the ASCII characters, the 8th bit defines the underline and the 9th bit generates the half-tone background video. The video page occupies a block of 8K of memory and, in the case of the AES-103, since 16K is available, a second video page may be accessed. The address of any location in this memory is produced by the generation of an X and a Y number, referring in that order to the character position and the line number. The address byte contains 16 bits and has the following format:



Bit 15 is decoded by the memory synchronization circuit when the CPU accesses the video memory.

b) Character Generation: Each character is generated within a 7 x 13 dot matrix where normal and descending characters may be displayed. To provide inter character and interline spacing, a character block concept is used; such a character block consists of 10 dots in the horizontal plane and 15 dots in the vertical plane (see FIG. 4).

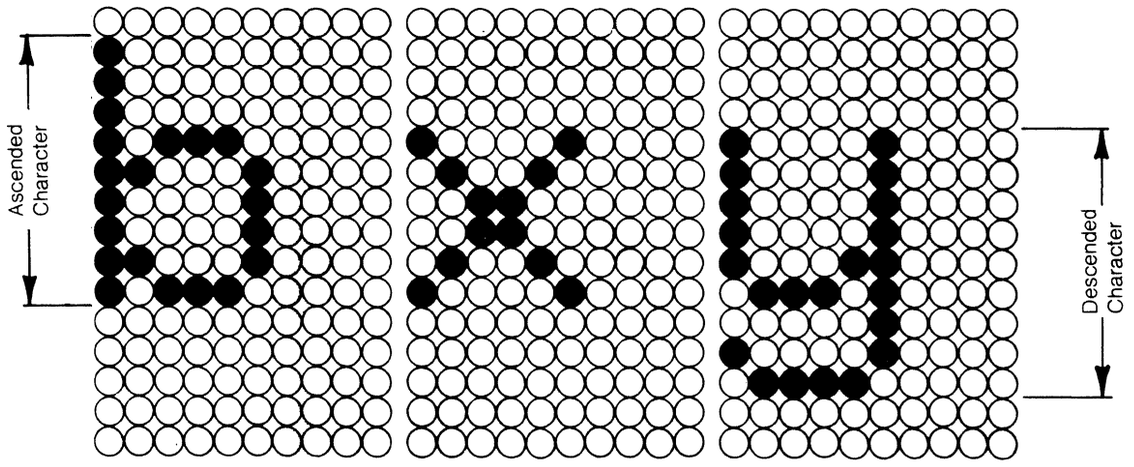


Figure 4 Inter Character & Inter Line Spacing

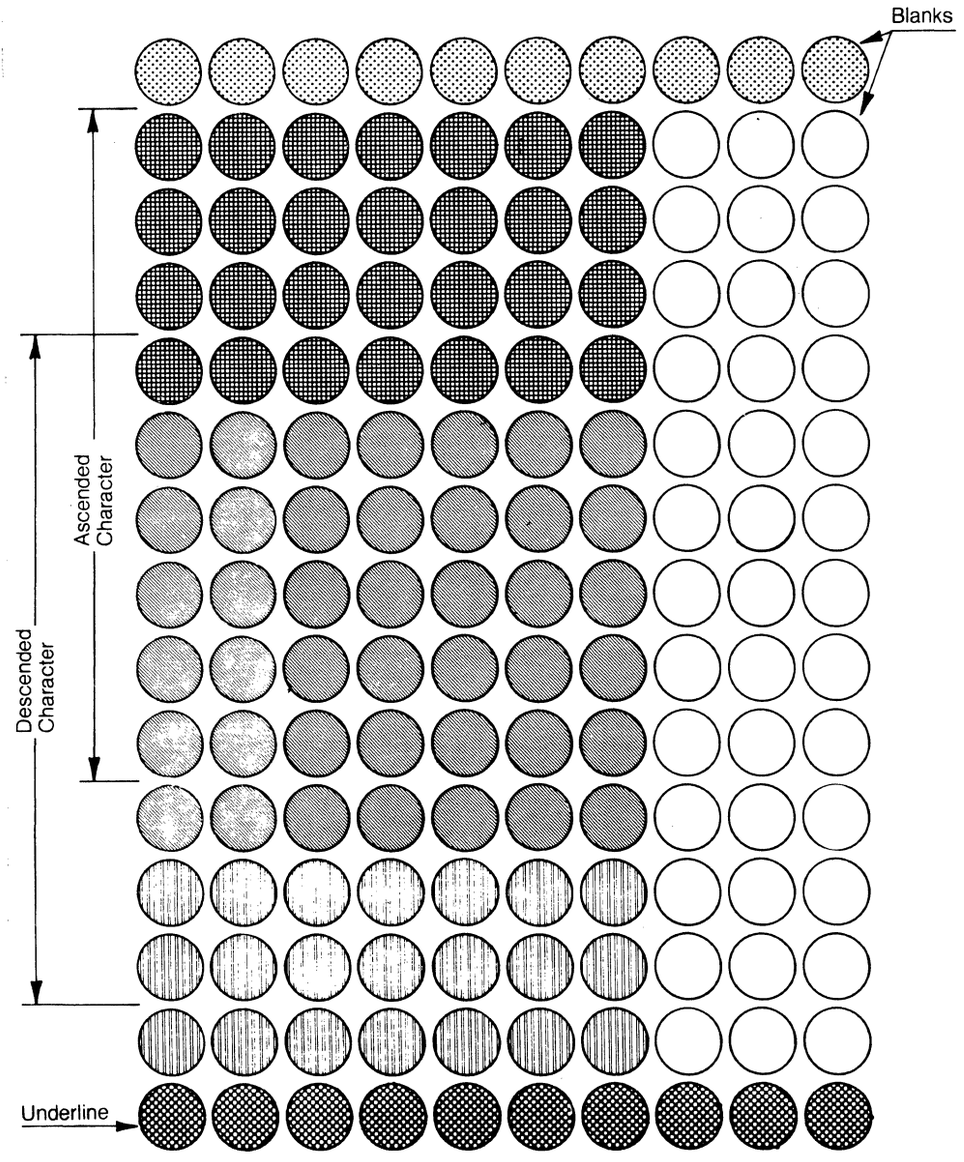
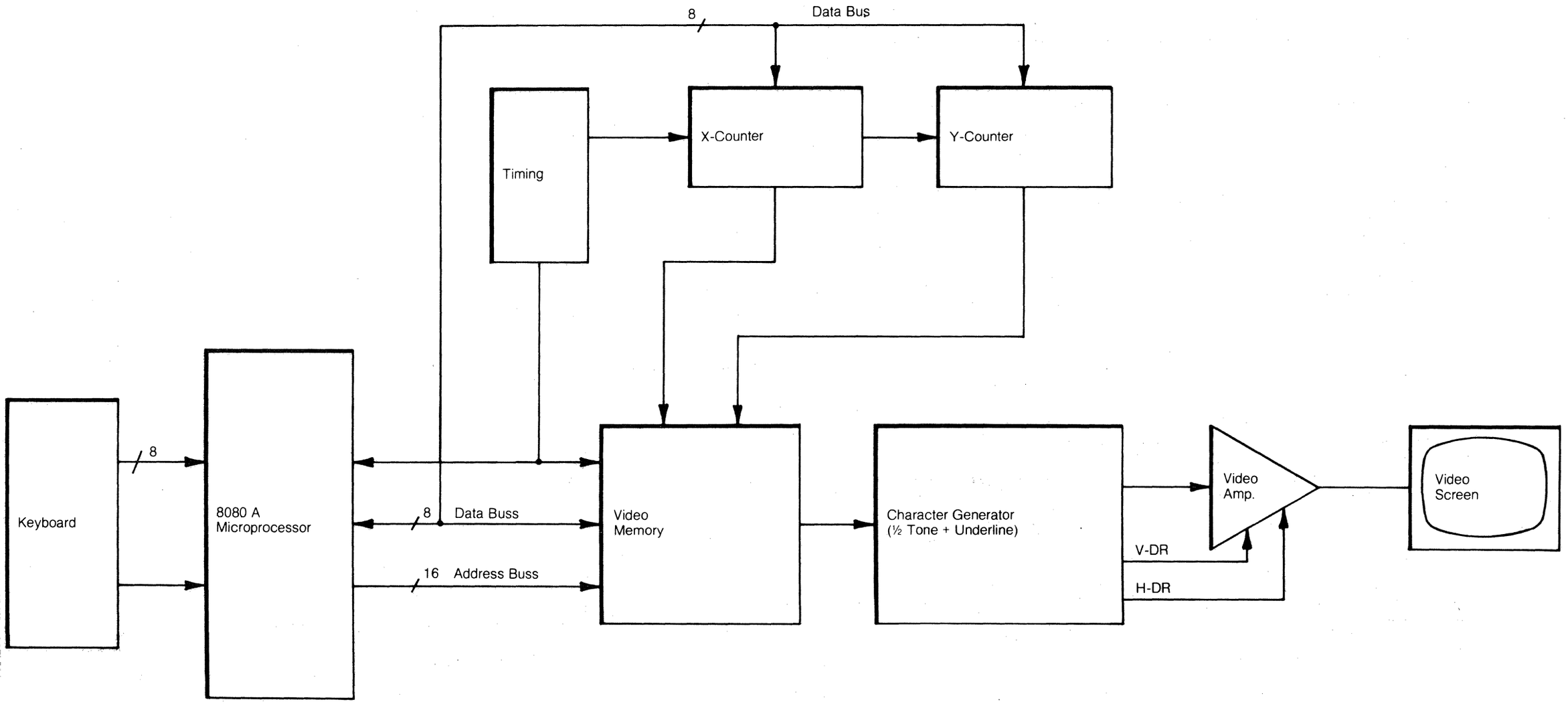


Figure 3 Video Subsystem



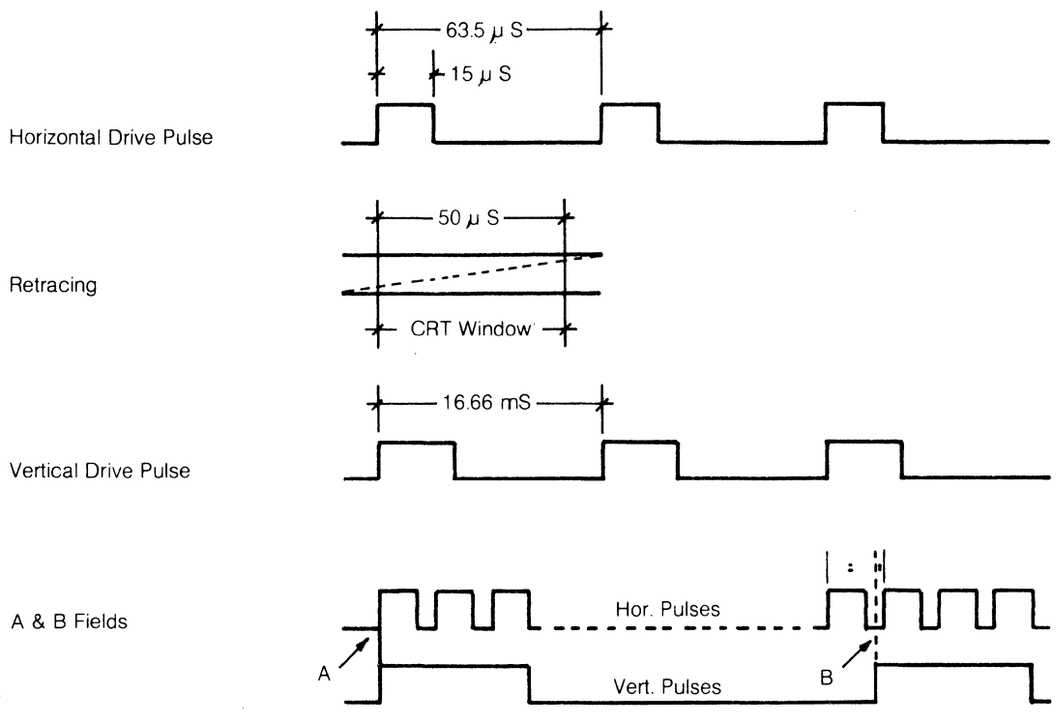
The cursor is a software controlled character and consists of a half-tone rectangle which occupies the whole 10 x 15 dot matrix.

c) Display Generation: The CRT employs the standard 525 line-per-frame display (625 for Europe). The basic element of the display is the scan line which is generated by the horizontal oscillator, pulse shaper and output amplifier of the CRT's analogue circuitry. However, the freerunning frequency of the horizontal oscillator is synchronized by the horizontal synchronization amplifier which accepts the 8 microsecond H-DR pulse issued by the timing circuitry of the video board. The scan line has a period of 63.5 microseconds which includes the 12.7 microsecond flyback period for the next scan line.

The vertical oscillator of the CRT circuitry is also free running and is synchronized in a similar manner as the horizontal oscillator. The video board generates a vertical drive signal (V-DR) which is applied to the vertical synchronization amplifier. This V-DR signal has the form of a pulse with a repetition rate of 60 per second (period of 16.66 milliseconds). The third signal involved in the display is the video pulse train and is responsible for displaying the dots on the CRT. This signal is fed directly to the cathode circuit of the CRT which modulates the electron beam.

Since the AES-PLUS employs an interlace video frame composition system, the relative occurence of the vertical and horizontal drive pulses is critical. They interact in the following manner:

Figure 5 Displays Signals



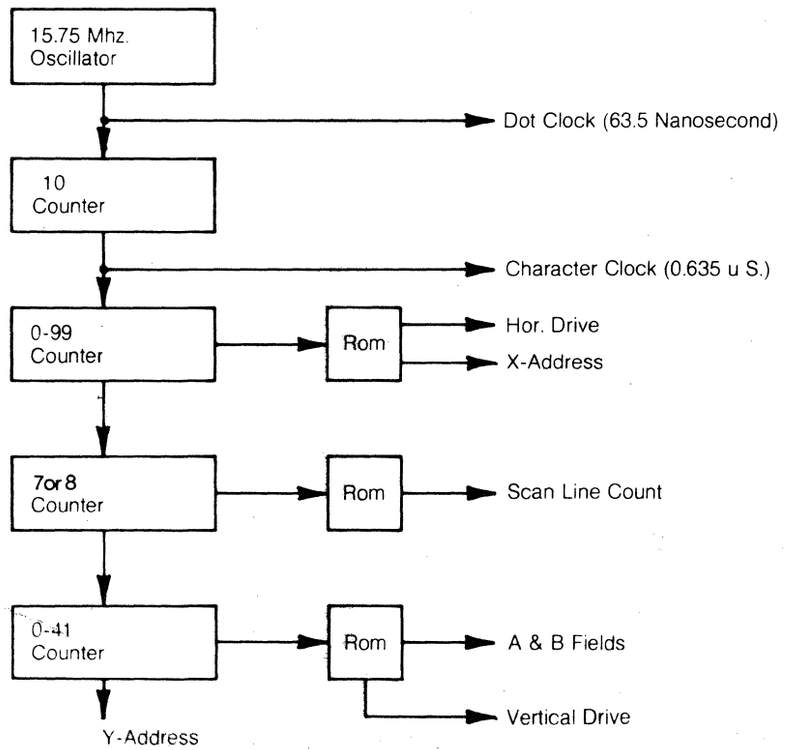
At the start of a video frame, the first vertical drive pulse appears simultaneously with a horizontal drive pulse and has a duration of 3 horizontal drive pulses. The second vertical drive pulse, however, starts halfway between two horizontal drive pulses and again has a duration of 3 horizontal drive pulses.

The simultaneous occurence of the vertical and horizontal drive pulses is called the "A" field whereas the trace where the vertical drive pulse starts midway between the three horizontal pulses is called the "B" field. Each field corresponds to 262.5 lines to form the 525 line standard frame (or 312.5 lines to form the 625 line european standard frame). Thus, interlacing provides high resolution but introduces flickering as the display is refreshed only 30 times per second. For this reason, P39 phosphor is employed to reduce this effect.

d) Timing Generation: The timing clock signals are generated from a 15.75 Mhz (15.625 for Europe) oscillator whose output is fed to a series of frequency dividers generating all the different frequencies used in the system. For example, it provides horizontal and vertical sync pulses, video pulses, block address signals and so forth (see figure 6).

Timing in video is generated in different frequencies affecting specific occurences for display purposes. The character clock for instance is derived from a ÷ 10 counter since a character is 10 dots wide. The number of block widths within a scan line constitutes the next frequency. By determining the number of characters in one scan line, the generation point of the horizontal drive pulse becomes evident. Therefore to provide an horizontal pulse of one scan period equivalent to 63.5 microseconds, a ÷ 100 counter becomes necessary.

Figure 6 Timing Generator



This counter is organized in such a way that count 0 corresponds to the left-most character position, count 1 corresponds to the second position and so forth. Consequently, the counter is used to address the memory as each character location corresponds to an X memory location. Since the video display consists of 80 characters, counts 80 to 99 are used for horizontal blanking.

In the vertical mode, a counter is also used to determine the height of the character. Thus, this counter is set to 7 or 8 scan lines, depending on whether the A or B fields are concerned or whether it will count an odd or even character line. In any case, the counter generates an output pulse each time a vertical character block has been completed.

The last required signal relates to the number of vertical character slots. In a similar manner to the horizontal system, the output pulse issued by the vertical line counter is applied to a block counter which assigns the number of blocks in the vertical field.

e) ROM Character Generator: The video signal will either turn on or off the electron beam of the CRT, allowing the display of a dot on the screen. A character on the video screen is simply a mosaic of dots whose outlines are determined by the ROM Character Generator, a single LSI integrated circuit. Within this chip, every character is stored on a line-by-line basis and is retrieved by a specific character addressing scheme. Thus, to generate a character on the screen, the video memory is addressed by the X and Y

coordinate of the specific allocated position. The resulting character from the video memory is combined with the vertical scan line count to provide an address pointer to one of the lines of the character. The specific address of that line is fed to the character generator which retrieves the required dot pattern. This dot pattern is then fed to a shift register and, being clocked by the dot frequency, becomes the serial video signal applied to the CRT monitor.

f) Microprocessor to Video Subsystem Interface: All the data to and from the Video Subsystem is channelled via the data buss. Data to be stored in the video memory is first assigned a specific address or location by the X and Y counters. The microprocessor then places a character on the data buss and sends a WRITE command to the video memory to place the character in the proper location. Special logic ensures that all Write functions are performed at the cursor position.

g) The Keyboard: The keyboard consists of standard typewriter characters, a fifteen key control function cluster located at the right and five option keys located at the left. Each time a character key is depressed, a signal is sent to notify the microprocessor and the keyboard unloads an ASCII coded character onto the data buss via a buffer.

.4 THE DISC SUBSYSTEM

In the AES-PLUS Text Editor system, the Disc Subsystem (FIG.7) may either consist of a dual or a single floppy disc storage drive and one disc interface. The main functions of the storage drive are:

a) To store text data magnetically for a later recall and, in the case of dual disc drives, the duplication of pages, texts or even entire disc files becomes possible. The dual system also incorporates a disc recovery function. This is accomplished by transferring all the good pages of the main disc to the secondary disc and systematically building a new directory with arbitrary page names.

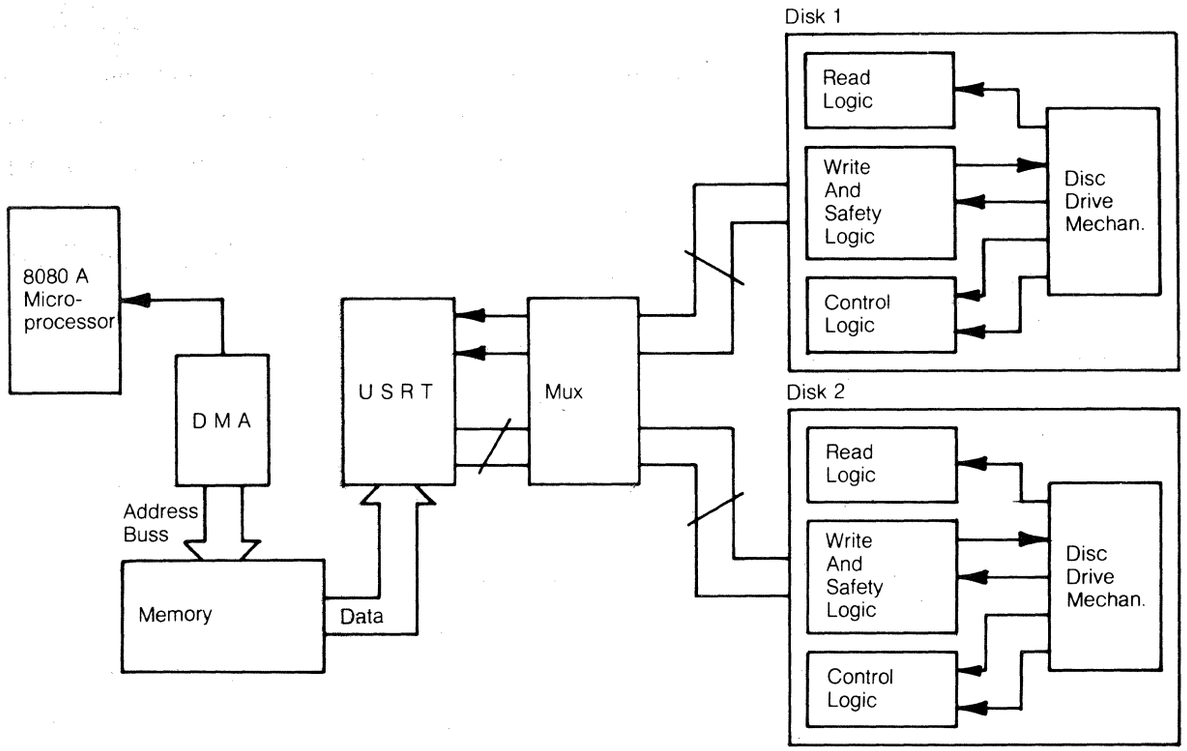
b) To buffer data to be printed so as to enable the overlapping of printing and editing.

A single Shugart SA400 Disc Storage drive provides storage for 109.4 kilobytes of data with a data transfer rate of 125,000 bits/second. The disc drive consists of a drive mechanism and a read/write head positioned by a mechanism activated by electronics. The magnetic disc is divided into 35 tracks at 3125 bytes per track, 16 sectors, one index, 16 sector holes and one file protect notch.

The smallest section of a disc recognized by the microprocessor is one track sector or 1/16 of a track, with a storing capacity of 193 bytes, and can be addressed randomly. The data recording method is a frequency modulation technique.

One SA400 mini-diskette is capable of storing up to 69 pages of text (however if all pages occupy a full 8K of memory, the minidiskette will overflow).

Figure 7 The Disc Subsystem



.5 THE PRINTER SUBSYSTEM

The Printer Subsystem (FIG.8) consists of two main units, the printer and the printer interface. It is utilized as an output device and allows the contents of the video page or the disc to be printed. The printer operates as a closed loop with the Microprocessor, accepting data only when certain flags allow it.

Printer Features: The high speed character printer is designed to interface only with automatic data systems. This printer can achieve a print rate of 45 characters per second during normal text printouts.

The most significant feature of this device is its mechanical simplicity since most mechanical functions have been replaced by electronics and the remnant inertia of the mechanism has been minimized through the use of light weight components.

Operation of the Printer: The Printer accepts signals from the Microprocessor and acknowledges by issuing feedback status signals. When the printer is being addressed, the microprocessor issues the Printer Select strobe and the printer responds immediately by the Printer Ready strobe. Any malfunction of the printer at this time will be indicated by the CHECK strobe which disables the printer.

The Paper Feed function is controlled by the P.F.RDY (paper feed ready) and the P.F.STROBE (paper feed strobe) command lines. When the P.F.RDY is set HI, the printer's paper feed logic is cleared and can therefore accept a paper feed command. The paper feed command is protected by an automatic interlock which prevents paper motion when a character print cycle is in progress.

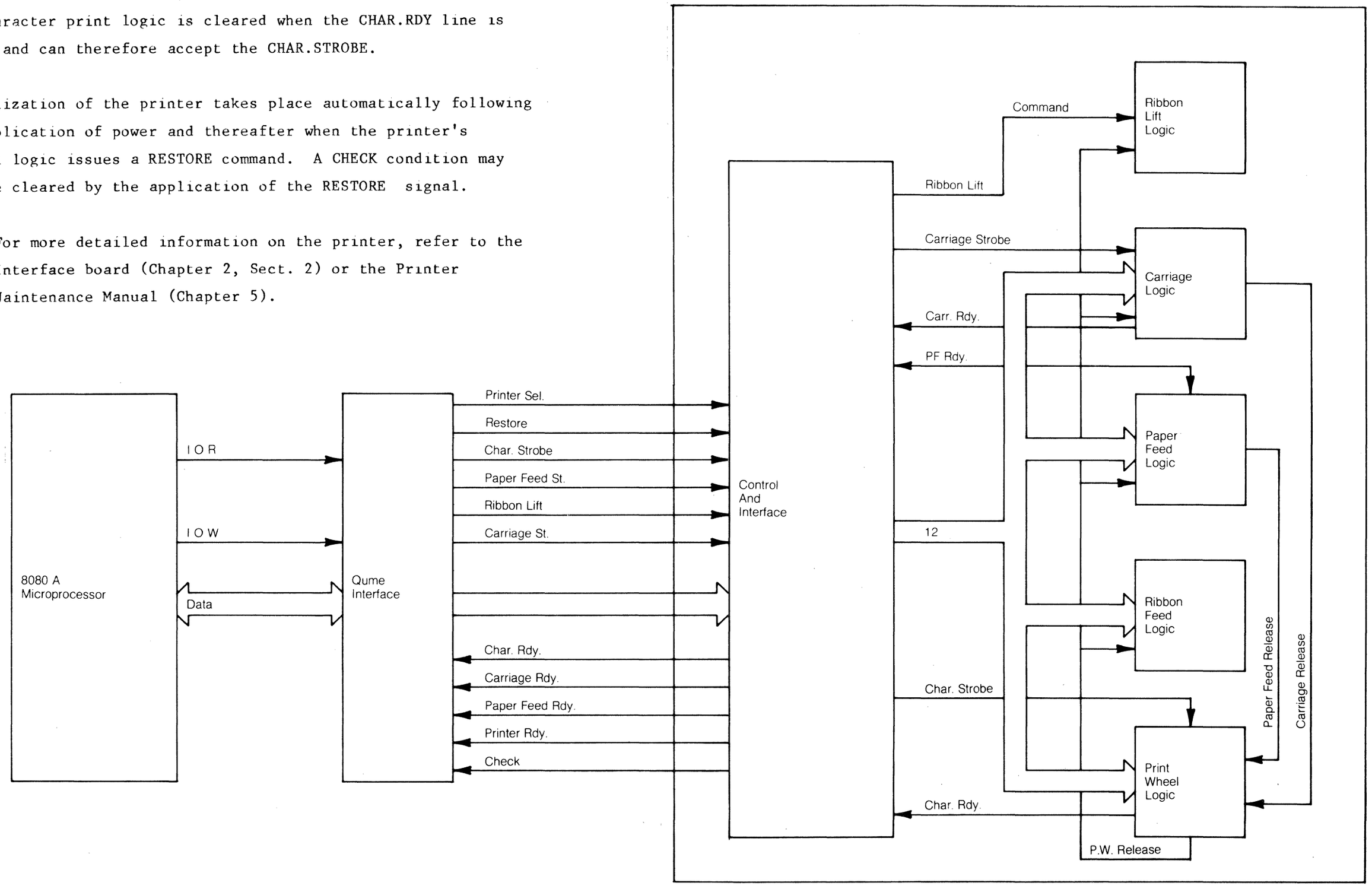
The Carriage Function is also controlled by two command lines, the CAR.STROBE and CAR.RDY. When the CAR.RDY status line is set HI, the printer carriage logic is cleared and can therefore accept a carriage strobe.

The Character Print function follows the same rule as above. Two command lines are involved, the CHAR.STROBE and the CHAR.RDY. The character print logic is cleared when the CHAR.RDY line is set I, and can therefore accept the CHAR.STROBE.

Initialization of the printer takes place automatically following the application of power and thereafter when the printer's control logic issues a RESTORE command. A CHECK condition may also be cleared by the application of the RESTORE signal.

NOTE: For more detailed information on the printer, refer to the Interface board (Chapter 2, Sect. 2) or the Printer Maintenance Manual (Chapter 5).

Figure 8 The Printer Subsystem



VIDEO BOARD (1-950-009101-00)

1. INTRODUCTION

The Video Board comprises all the logic circuits to perform the following functions:

- Timing for the instruction memory (RAM).
- Storage of a page of text in a memory.
- Generate a video signal for display purposes.
- Generate a real time clock interrupt signal.
- Generate TICK and BELL sounds.

2. CONFIGURATION

The video board is divided into 9 subgroups:

- The X counter.
- The scan line counter.
- The Y counter.
- The address linearizer
- The video memory and video output.
- The memory synchronization circuit.
- The I/O flag register
- The TICK & BELL logic.
- The timer interrupt

3. FUNCTIONAL DESCRIPTION

3.1 The X-Counter

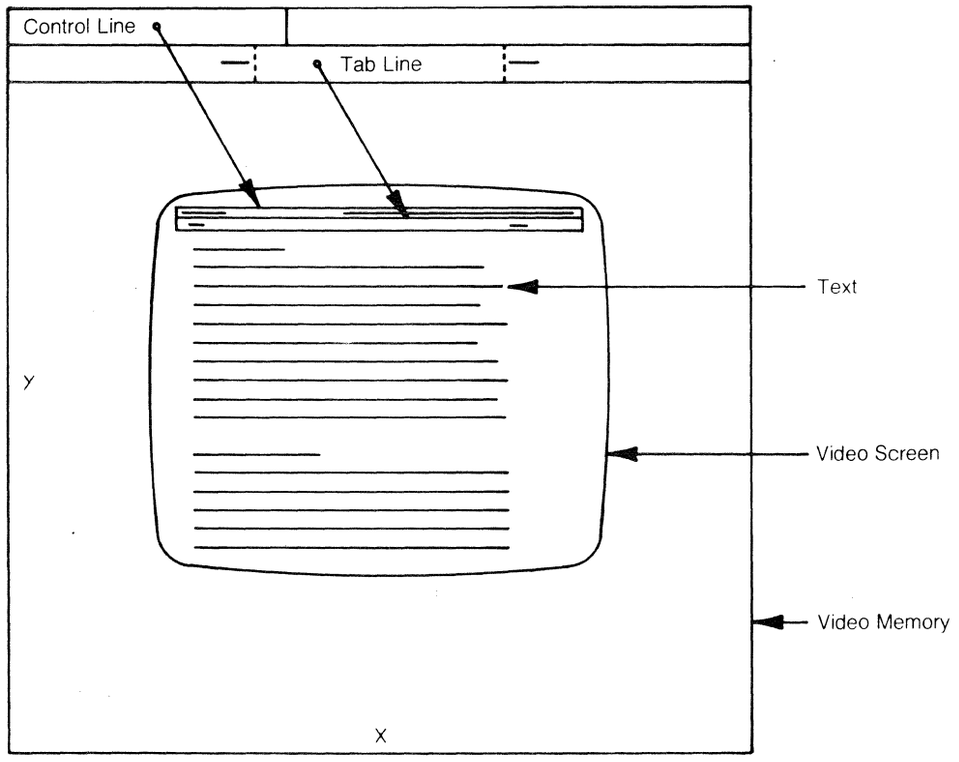
a) Clock Generator: The clock generator consists of inverters A2-B, A2-E and a 15.75 MHz crystal (16.625 MHz for PAL). The output of the generator is the CLOCK signal, which is inverted by A2-A to form the dot clock with a period of 63.5 nanoseconds and is also applied to counter A4(74160) from which successive division of the clock signal is initiated. The binary output of A4 is applied to Binary-to-Decimal converter A13(74LS42) from which clock pulses CPØ, CP3, CP5, CP6 and CP9 are produced. Clock pulse CP9 occurs every 635 nanoseconds, corresponding to the end of a character interval. Clock pulses CPØ, CP3, CP5 and CP6 are then applied to R-S latches A12 which generates three major video and CPU memory timing signals, RAS*, CAS* and ROW EN*.

b) X-Counter: The X-counter generates the X address to the display (the position of a character on a line). This counter consists of devices A20(74LS161), A11(74LS161) A49, A58(6301) A65, A38, A28, A37 and A53-B.

The input circuit of the X-counter consists of A20 and A11, forming a 7-bit serial counter, incremented by clock signal CP9. The serial counter counts from 0 to 99, giving the amount of X addresses necessary to fill the video screen. To determine the starting address of the video display, since the video page has a maximum capacity of 256 characters per line, an offset value is loaded into the X-start register from the CPU and this value is added to the X-counter value in devices A38 and A29 (4-bit full adders).

In displaying the control line, since it is never scrolled from the video display, a permanent location (address ØØØØØØØ) has been assigned for it in the memory. When a video frame is displayed, buffer A28 (DM51LS95) is enabled by the CNTRL LN-1 strobe for the first character row so as to force the offset to be zero; this scheme establishes a stationary video display for the control line. The X-Start register is enabled by the CNTRL LN-1 strobe, creating a shift in the display from addresses ØØØØØØØ of the control line to the address of the first line of text to be displayed. In figure 1, the scheme is clearly visualized.

Figure 1 Control & Tab Line Location



The tab line is, however, scrollable to the left and the right of the video page. It occupies line 1 and scrolls from X = Ø to X MAX in an 80 character segment.

c) Control Strobes: The seven bits of the X-counter are also applied to two ROM's (MMI 6301-1). These ROM's track the character count to generate 8 control strobes, which are: X-RST, XROM1, 3, 4, 5 and 6, EARLY HOR.DR and Power Supply Synch. These strobes are latched through A65(74LS73) to eliminate skewing an "glitches".

3.2 SCAN LINE COUNTER

This counter consists of devices A62, A69, A53-A and A45-A. Its purpose is to keep track of the number of scan lines per character row (15 lines) and maintain the alternate 7 and 8 scan line count for the A and B fields (interlaced display).

The input to the scan line counter consists of device A62(74SL161), configured as a binary up-counter. The horizontal drive signal (H-DR) increments the counter at the end of each scan line. The three bit binary outputs SL1, SL2 and SL3 are inverted and applied to the character generator as bits RS1, RS2 and RS3. Bit SL is a product of either bit Y-ADØ or AF*, exclusive-ored by A33-B. Bit SLØ also serves as the 7 or 8 count selector bit, fed with SL1 to SL3, EARLY H-DR*, MIDSCAN, AF, ROW 41 to a 256 x 4 bits ROM (6301). Two ROM outputs are then issued to flip-flop A45-A to form the V-DR strobe while UNDERLINE and Y-CLOCK constitute the others.

3.3 THE Y-COUNTER

This counter comprises devices A30, A39, A21, A66, A50, A48, A59 and A57. It generates the Y address of the display, meaning simply that its content corresponds to the character row count.

The basic counter consists of devices A30 and A66(74LS161) forming a 6-bit binary counter. The Y-CLK strobe, issued by scan line counter and occurring at the end of each character row, increments the counter. The Y-counter is configured similarly to the X-counter, where the Y-address of the video display is generated by the summation (A50 and A59) of the contents of Y-Start register A48(74LS374) and the contents of Y-Counter A30 and A66. The Y-Address for the control line is still located at Ø and accessed at tri-state register A57(74LS95) by strobe CNTRL LN-2. The outputs of the Y-Counter are also fed to decoding ROM A39(6301) from which are generated control strobes Y-RST, Y-ROMØ, Y-ROM1 and V-DR*. The first three strobes are latched through A21(74LS175) while V-DR* is brought to NAND gate A67-C and combined with CLR VDR, to form the V-DR pulse at flip-flop A45-A. A strapping option applied to ROM A29 selects the 525 or 625 line video display.

3.4 THE ADDRESS LINEARIZER

This subgroup comprises integrated circuits A32, A41, A61, A52,A68, A44 and A33. The purpose of this subgroup is to transform the CPU, the X and Y addresses into a "linearized" format complying with the video memory address input.

The AES-103 can display two video pages. In this case the current page occupying 8K of memory and another "background" page occupying the remaining 8K. The information format pertaining to either page to be displayed is obtained from the CPU and loaded into a holding register (A32) in a 6-bits format. The register is loaded by strobe LD XMX on the positive edge. The 6-bits are then multiplexed by A41 (74LS298), selecting whichever page is being accessed. The selected information is then fed to both ROMS (6351) as bits A7, A8 and A9. The remaining address bits AØ through A6 are issued by the X and Y address multiplexer.

At this stage, the ROMS perform a mathematical operation with the different variables appearing at its inputs, and this operation is a multiplication of the row number (Y address) by the maximum number of characters per row. The X component of the address is then added to the product by full-adders A68 and A44 (74LS293), e.g., if the maximum number of characters in a row is 80 and the row number is 57, the output of the ROM is 4560. The value of the X component may be any value between 1 and 80, so as to position a character on the video screen.

The 8 outputs (Mad 4-12) from the full-adders are then applied to the video memory controller chip. The 12th bit is issued from exclusive-or gate A33-D, being either the carry bit from A68 or A61's bit Ø4.

3.5 THE VIDEO MEMORY AND VIDEO OUTPUT

a) The Multiplexer: Consisting of devices A31, A40, A51 and A60 (74LS298), the multiplexer selects either the CPU bus address or the X and Y address lines. Each time a new character is to be displayed on the CRT, the MUX SEL strobe goes HI and allows the selection of the CPU buss address. The most significant bit of the CPU buss address is I/O FL5, called the Paging bit, which, when set, selects the video page located at the most significant addresses of the 16K video memory (one page equals 8K). The paging bit and the lower 4-bits of the multiplexer are applied directly to the refresh memory logic, that is memory controller chip A64(3442). The remaining bits are brought to the Linearizer circuit for further processing.

b) The Video Memory: This memory comprises devices A64, A17, A23, A26, A27, A35, A36, A46, A47, A18, A25 and A3. The memory employs nine 16K devices (2116), eight of which are used as video memory and one as a buffer for half-tone character display information.

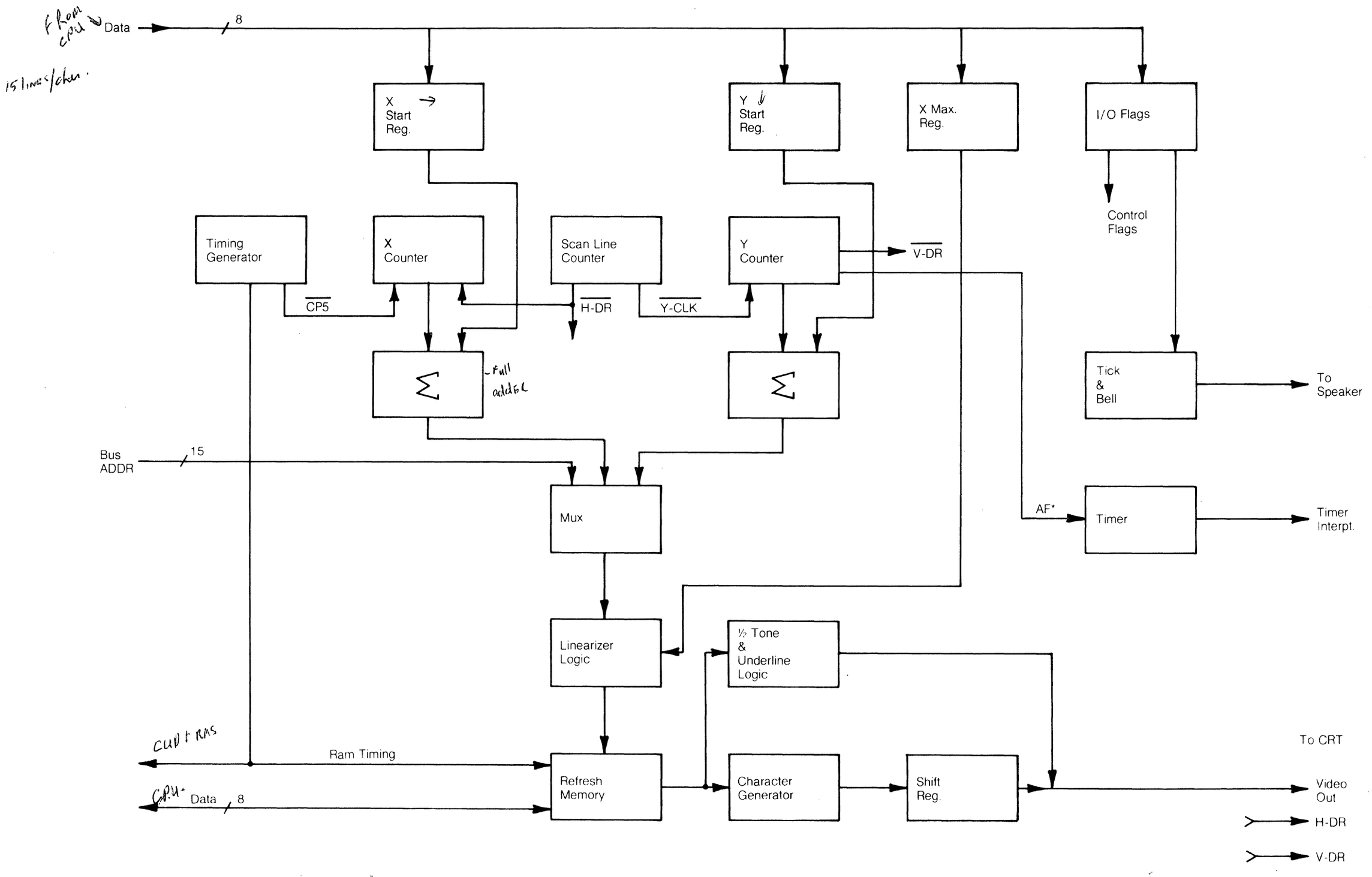
Linearized memory addresses are applied to memory controller chip A64(3242), which generates 14 addresses in 7 address segments, in a multiplexer fashion and also refresh addresses, since it contains its own refresh address counter. The memory controller is timed by three strobes called REFR, COUNT and ROWEN, all issued by the timing generator. The 16K RAM chips are strobed by RAS* and CAS*, allowing proper address loading and data transfer. The eight data bits to the RAM chips are obtained from the data buss via buss driver A25 and are written by RAM WE. The ninth RAM chip holds half-tone character information to be displayed. Its input is obtained from I/O FL7.

c) The Video Output Logic: Devices A34, A43, A71-B, A22-C A23-B, A5-C, A8-C-D-F-E constitute the video output logic.

The memory data output consists of modified ASCII to meet special characters for video and printer purposes. Output character data supplied by the video memory is fed to memory latch A34 (74LS273). The code is then applied to character generator A43(MCM6570). The scan line counter outputs are also applied to A43 at inputs RSØ, RS1, RS2 and RS3, forming a binary code used to select one of the rows of the addressed character to appear at the seven output lines. The character generator outputs are then fed to parallel-to-serial shift register A54(74165) from which the serial data is brought to the video output via exclusive-or gates A23-B and A27-C, to three-input nand gate A5-C and finally to inverter A8-E. The eighth character underline bit, contained in D flip-flop A71-B, is nanded at gate A23-B. When half-tone background is displayed, the 1/2 TONE strobe coming from flip-flop A3-B goes active low, disabling inverters A8-E. The video signal now passes through inverter A8-F and therefore voltage divider R3 and R6. The video off-state is then generated at half amplitude (2.5V), thus creating the half-tone background.

X →
Y ↓

Video Board Block Diagram



3.6 THE MEMORY SYNCHRONIZATION CIRCUIT

This circuit comprises flip-flop A24, A6 and A15; its purpose is to regulate the memory request cycle of the CPU and the refresh function.

When the CPU accesses the video memory, bit AD15 is set and strobes MEMR* or MEMW* are LO. These states are applied to A6-A, A6-D and A14F. Flip-flop A24-A D input will go LO if no Refresh cycle (PRE REFR) occurs or the video logic reads the memory (I/O FLØ 6 PRE ADDR SEL). The RAS* signal thereafter clocks the flip-flop which issues the SYNC-F strobe. The memory is then read by the CPU via the CPU buss during the period the SYNC-F strobe is HI. At the next RAS* pulse, the SYNC-F strobe goes LO which sets the memory flip-flop A24-B, issuing RDY* via inverter A8-B.

When the MEMR* or MEMW* strobes go high again, the RDY* flip-flop will be cleared.

3.7 THE I/O FLAG REGISTER

This register consists of integrated circuit A19(9334), which distributes 8 flags (I/O FLØ - FL7). Strobe LD I/O enables it when LO. The register accepts a four-bit (DBØ DB3) binary number and distributes the decoded number on 8 lines.

3.8 THE TICK AND BELL LOGIC

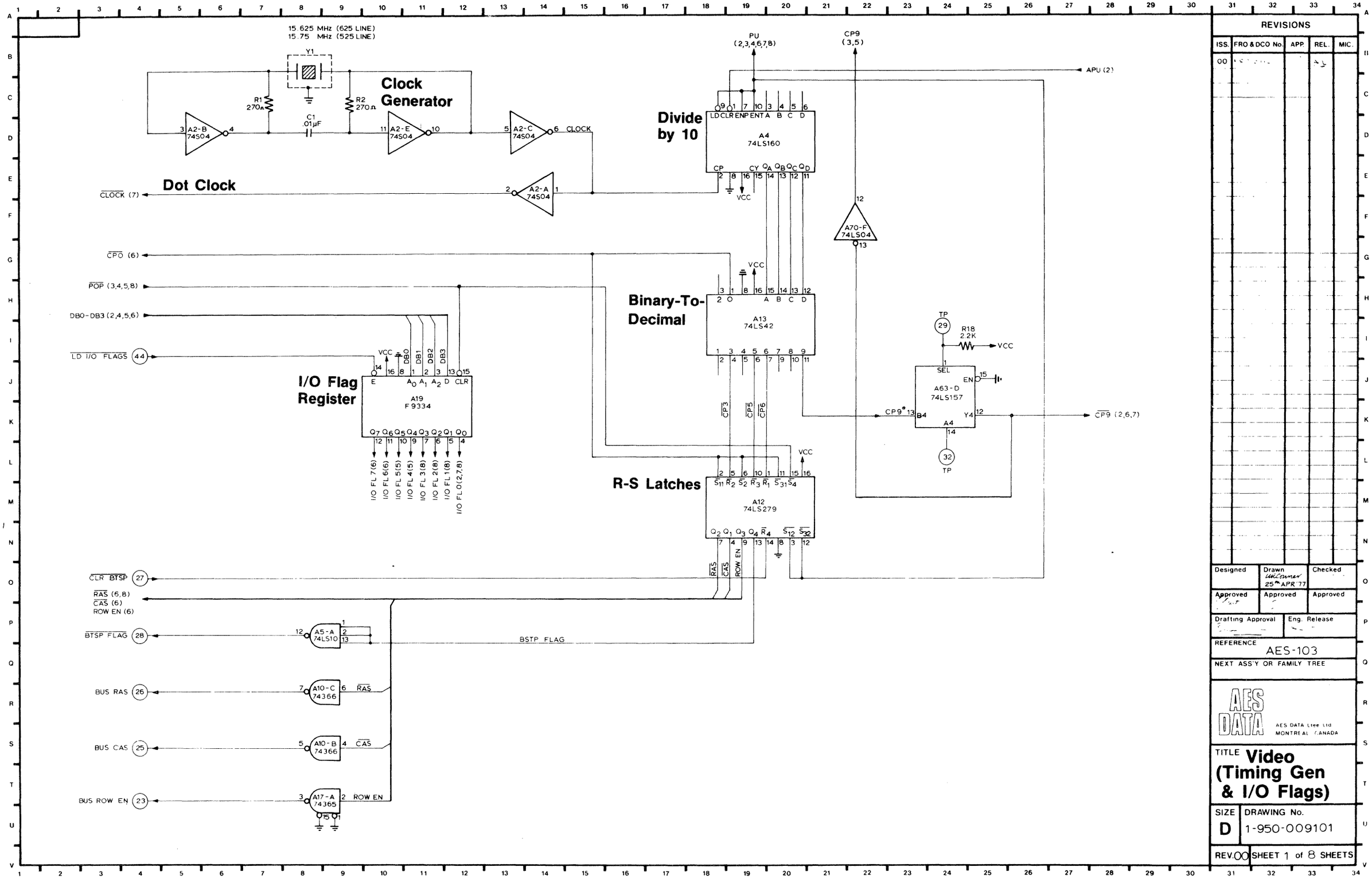
This circuit consists of dual timer device A16(3456), inverters A14-E, A14-D and A8-A and output transistors Q1 and Q2.

When BELL and TICK sounds are required, I/O flags FL2 and FL3 are caused to pulse through inverters A14-E or A14-D. Device A16 consists of a dual timer (similar to a 555) where each one is tuned to the specific pitch required for the bell and tic sounds. A 2 KHz signal appears at inverter A8-A, whose output is an open collector, connected to resistors R11 and R12. When timer output A or B goes high, the 2 KHz signal modulates the collector circuit of Darlington pair Q1 and Q2, which in turn drive the speaker.

3.9 THE TIMER

This circuit includes devices A72, A71-A, A10-F, A15-D and A15-C. Its purpose is to generate an interrupt every 200 milliseconds (used for software purposes).

The field rate, AF*, issued by the Y-counter, is introduced to decade counter A72(74LS161), enabled by I/O FL1. The output of the counter is taken at the carry output and applied to D flip-flop A71A. Strobe CLR TIME INTRPT and the rate of AF* control the flip-flop. The Q output forms the CPU interrupt, which is distributed by line driver A10-F.



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.
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Designed	Drawn [illegible] 25TH APR 77	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES-103

NEXT ASS'Y OR FAMILY TREE

AES DATA

AES DATA Ltee Ltd
MONTREAL CANADA

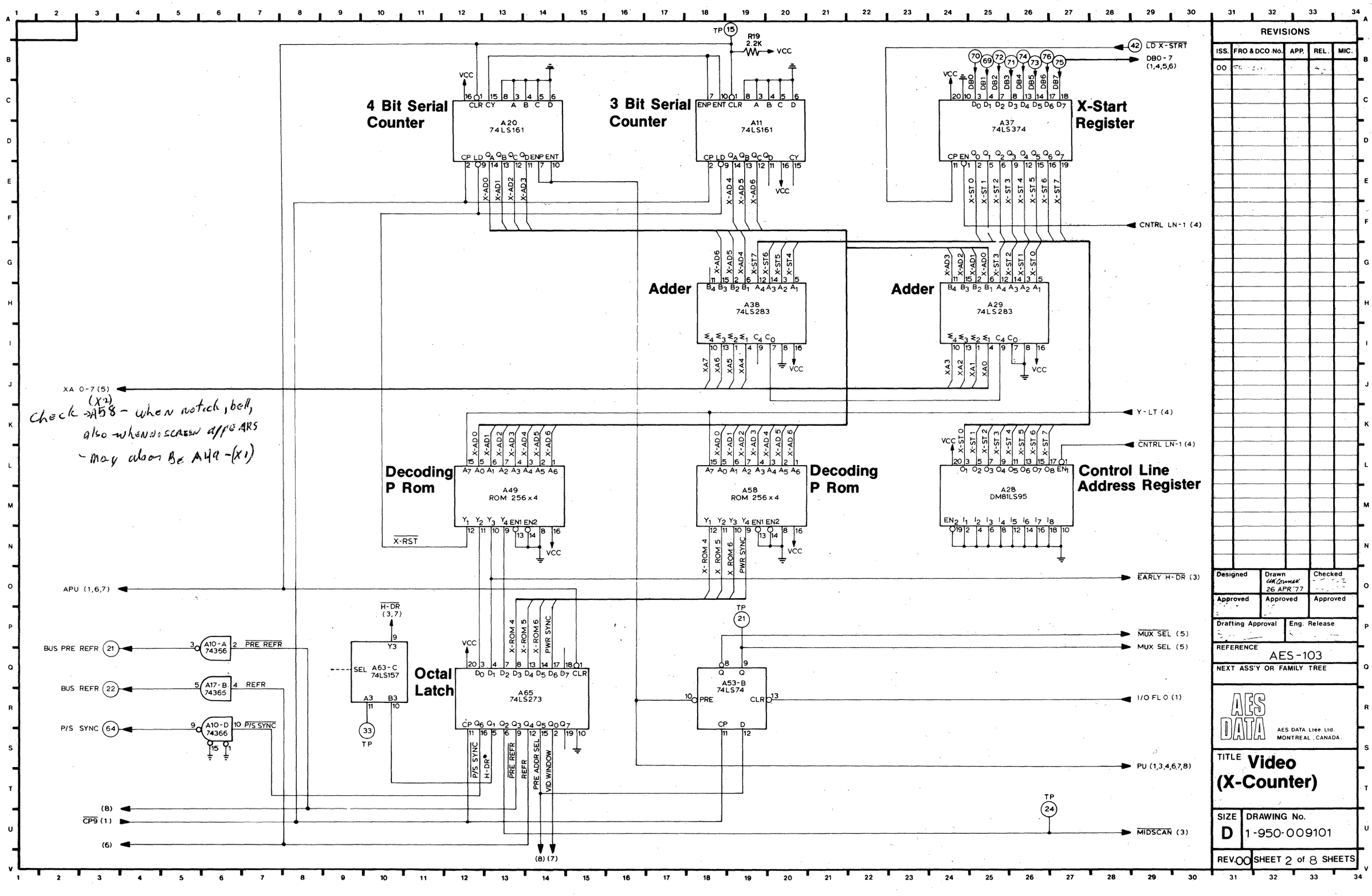
TITLE **Video (Timing Gen & I/O Flags)**

SIZE	DRAWING No.
D	1-950-009101

REV.00 SHEET 1 of 8 SHEETS

Video Schematic Diagrams

Video Schematic Diagrams



REVISIONS				
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Designed	Drawn W.R. Conner 26 APR '77	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES-103

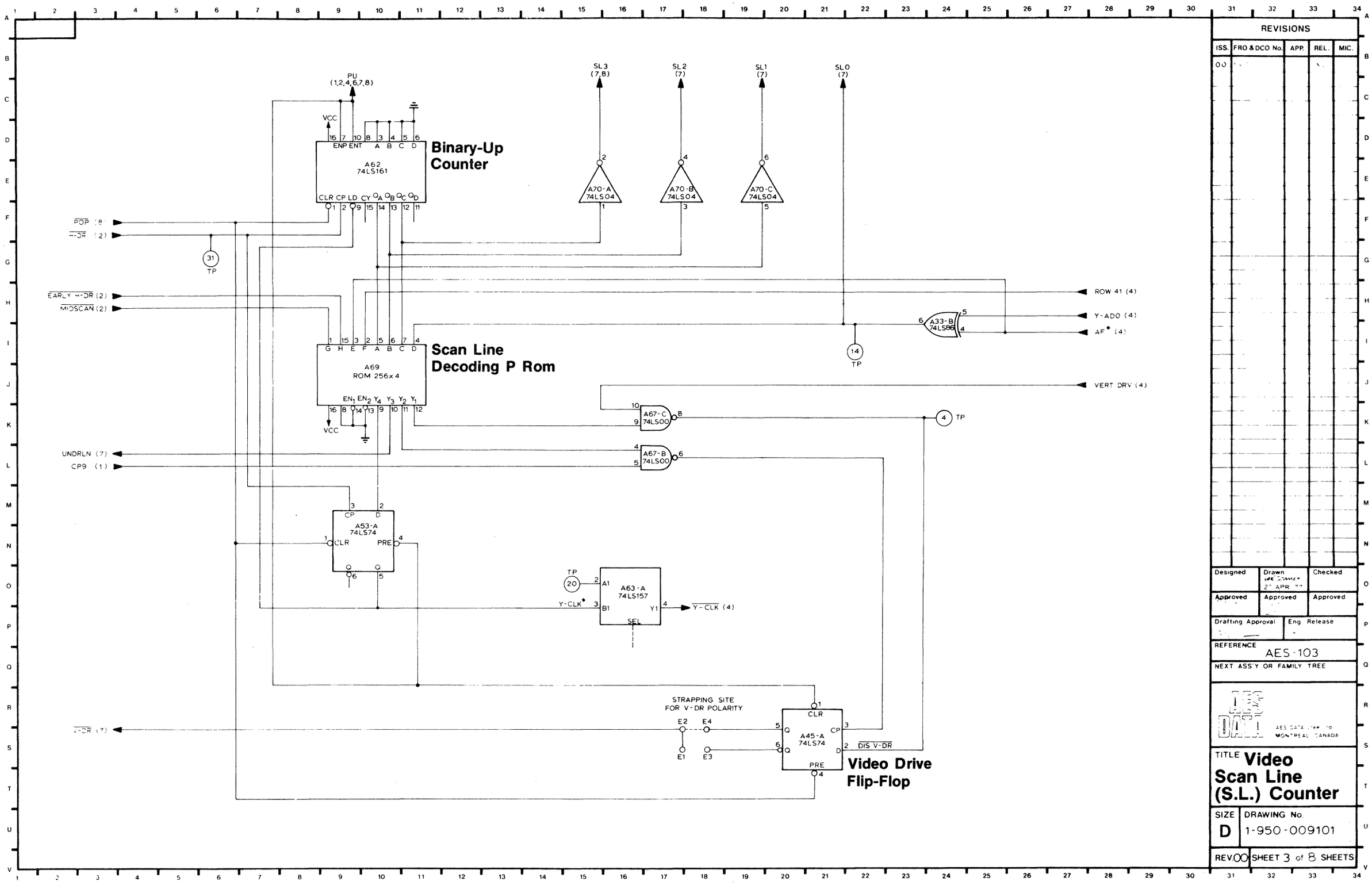
NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee. Ltd. MONTREAL, CANADA.

TITLE **Video (X-Counter)**

SIZE	DRAWING No.
D	1-950-009101

REV. 00 SHEET 2 of 8 SHEETS



REVISIONS

ISS.	FRO & DCO No.	APP.	REL.	MIC.
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Approved	Approved	Approved

Drafting Approval	Eng. Release

REFERENCE AES-103

NEXT ASS'Y OR FAMILY TREE

AES DATA (1980) LTD. MONTREAL CANADA

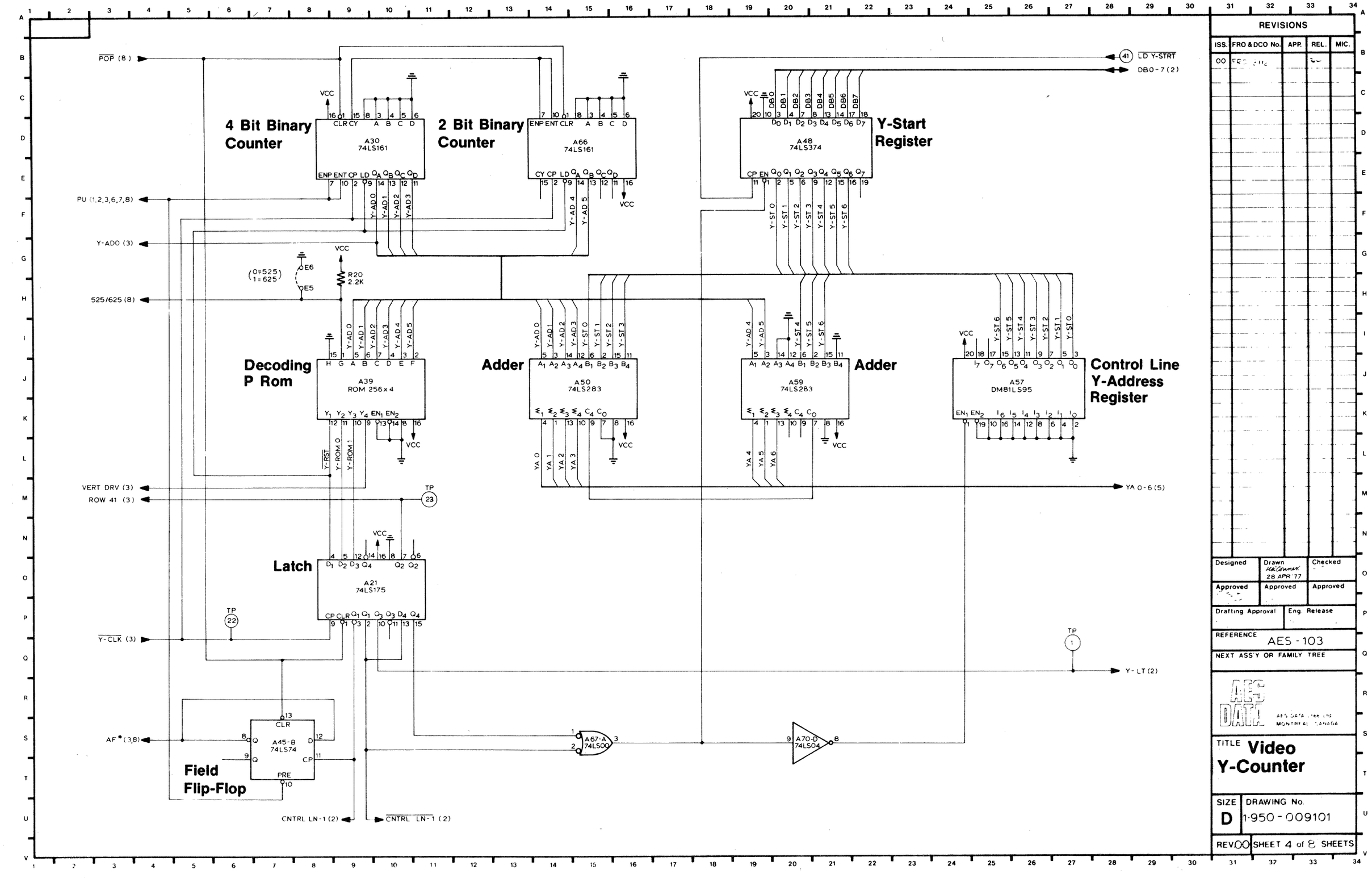
TITLE **Video Scan Line (S.L.) Counter**

SIZE	DRAWING No.
D	1-950-009101

REV. 00 SHEET 3 of 8 SHEETS

Video Schematic Diagrams

Video Schematic Diagrams



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Designed	Drawn H.R.Conner 28 APR '77	Checked
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Drafting Approval	Eng. Release	

REFERENCE AES-103

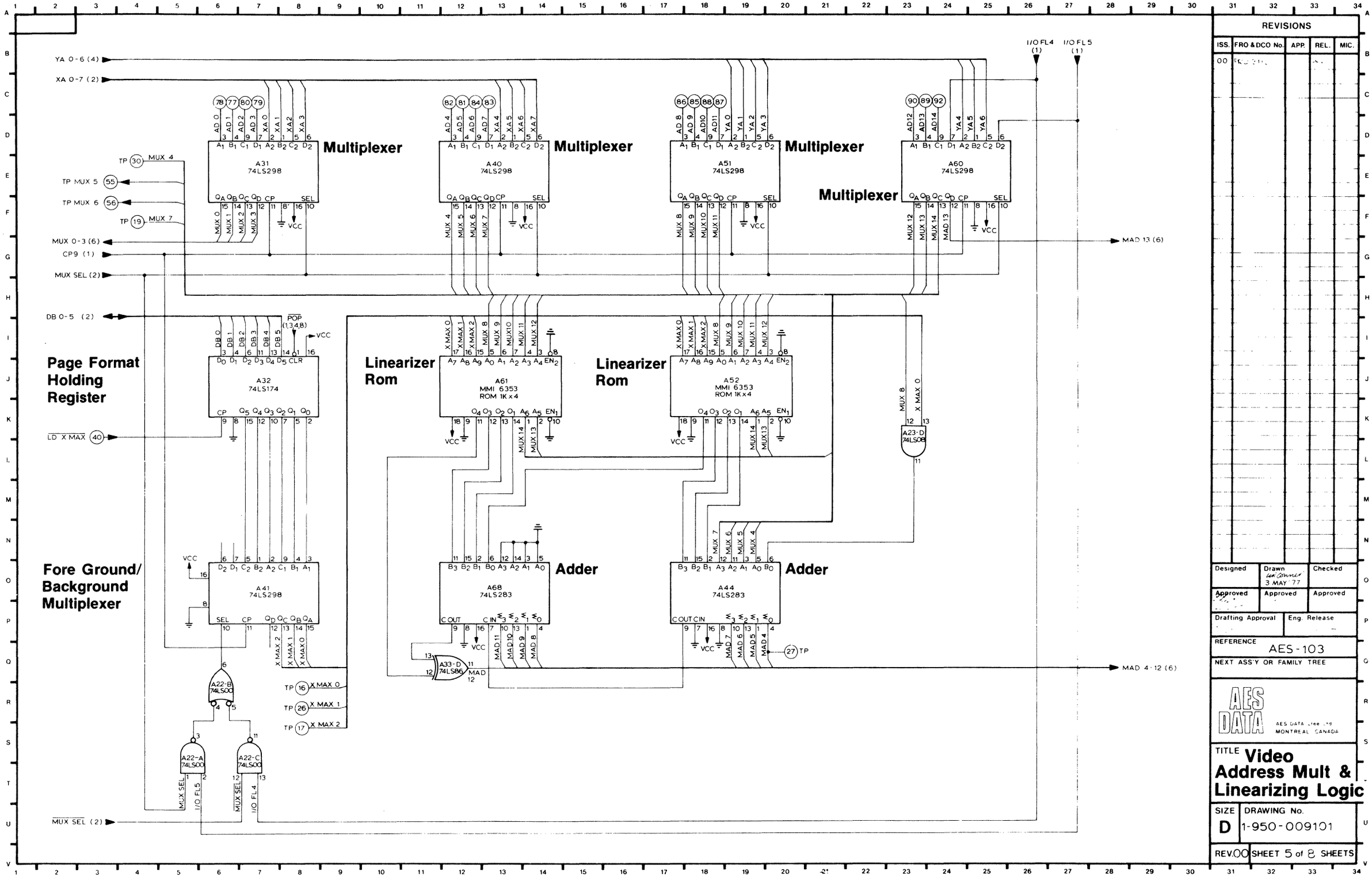
NEXT ASS'Y OR FAMILY TREE

AES DATA LTD. MONTREAL CANADA

TITLE **Video Y-Counter**

SIZE	DRAWING No.
D	1-950-009101

REV 00 SHEET 4 of 8 SHEETS



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Drafting Approval	Eng. Release	

REFERENCE AES-103

NEXT ASS'Y OR FAMILY TREE

AES DATA

AES DATA [illegible] MONTREAL CANADA

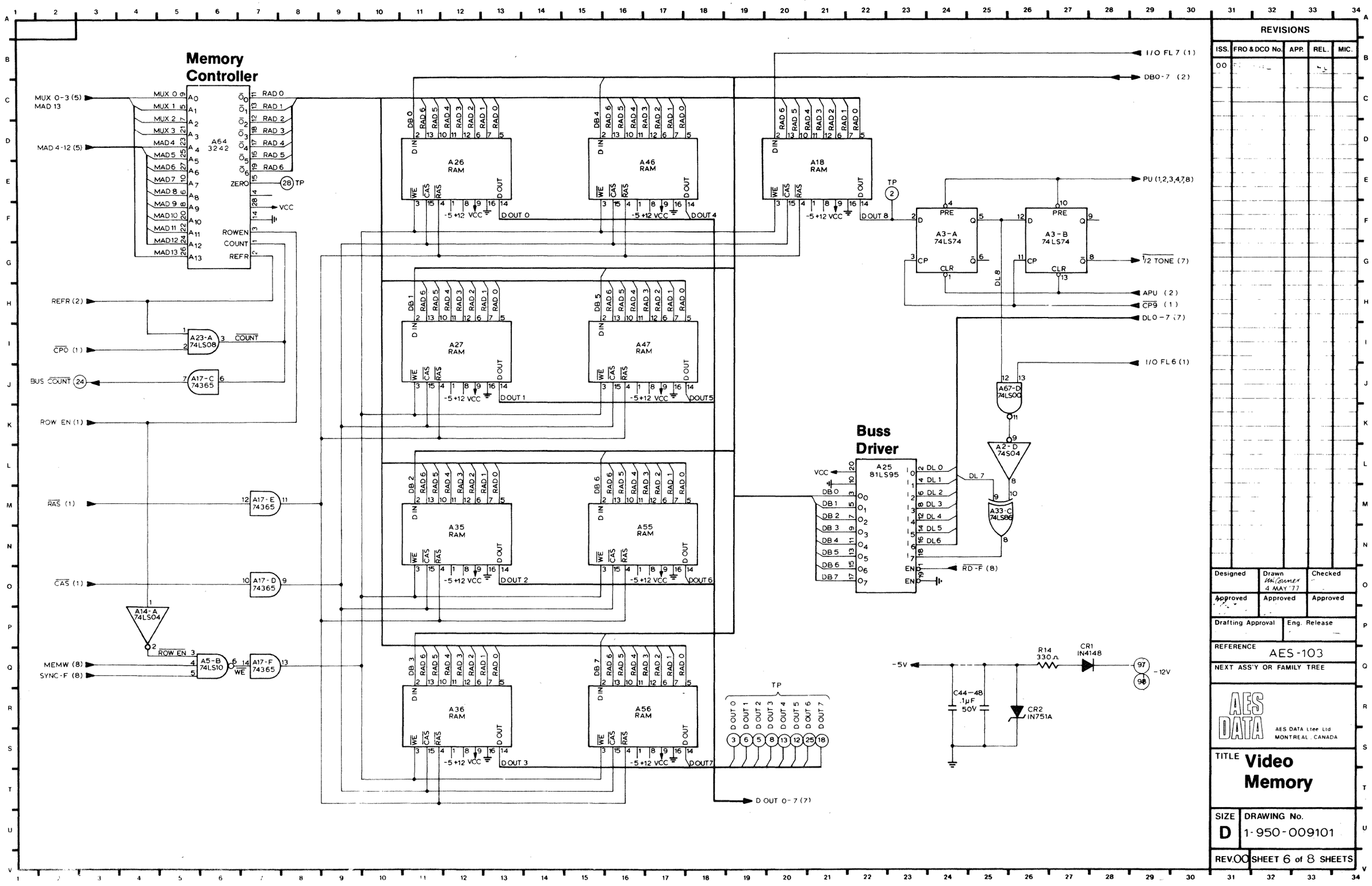
TITLE **Video Address Mult & Linearizing Logic**

SIZE	DRAWING No.
D	1-950-009101

REV.00 SHEET 5 of 8 SHEETS

Video
Schematic
Diagrams

Video Schematic Diagrams



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Designed	Drawn M Cramer 4 MAY '77	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES-103

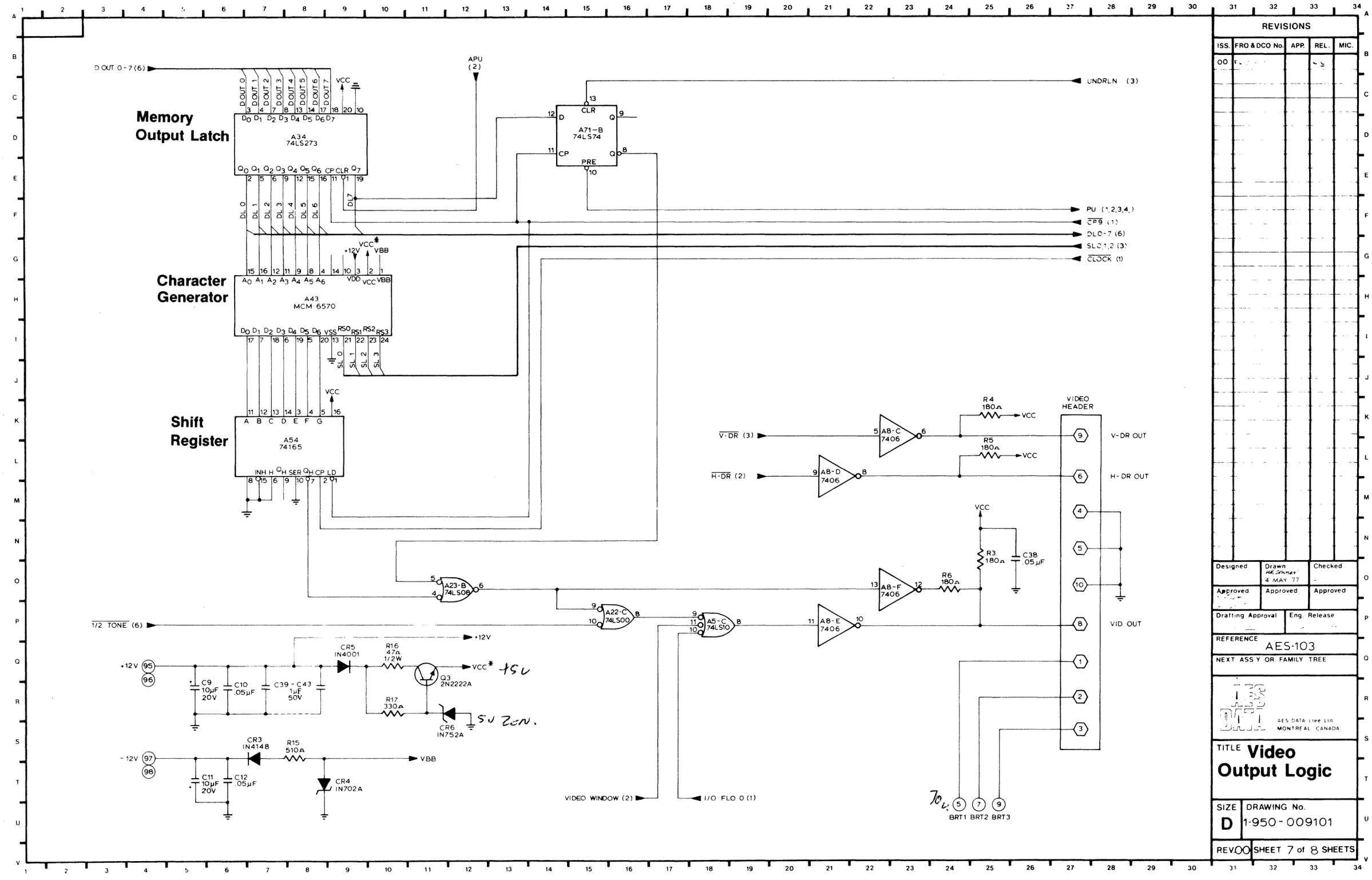
NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee Ltd MONTREAL, CANADA

TITLE **Video Memory**

SIZE	DRAWING No.
D	1-950-009101

REV. 00 SHEET 6 of 8 SHEETS



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Designed	Drawn	Checked
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Approved	Approved	Approved

Drafting Approval	Eng. Release

REFERENCE AES-103

NEXT ASS'Y OR FAMILY TREE

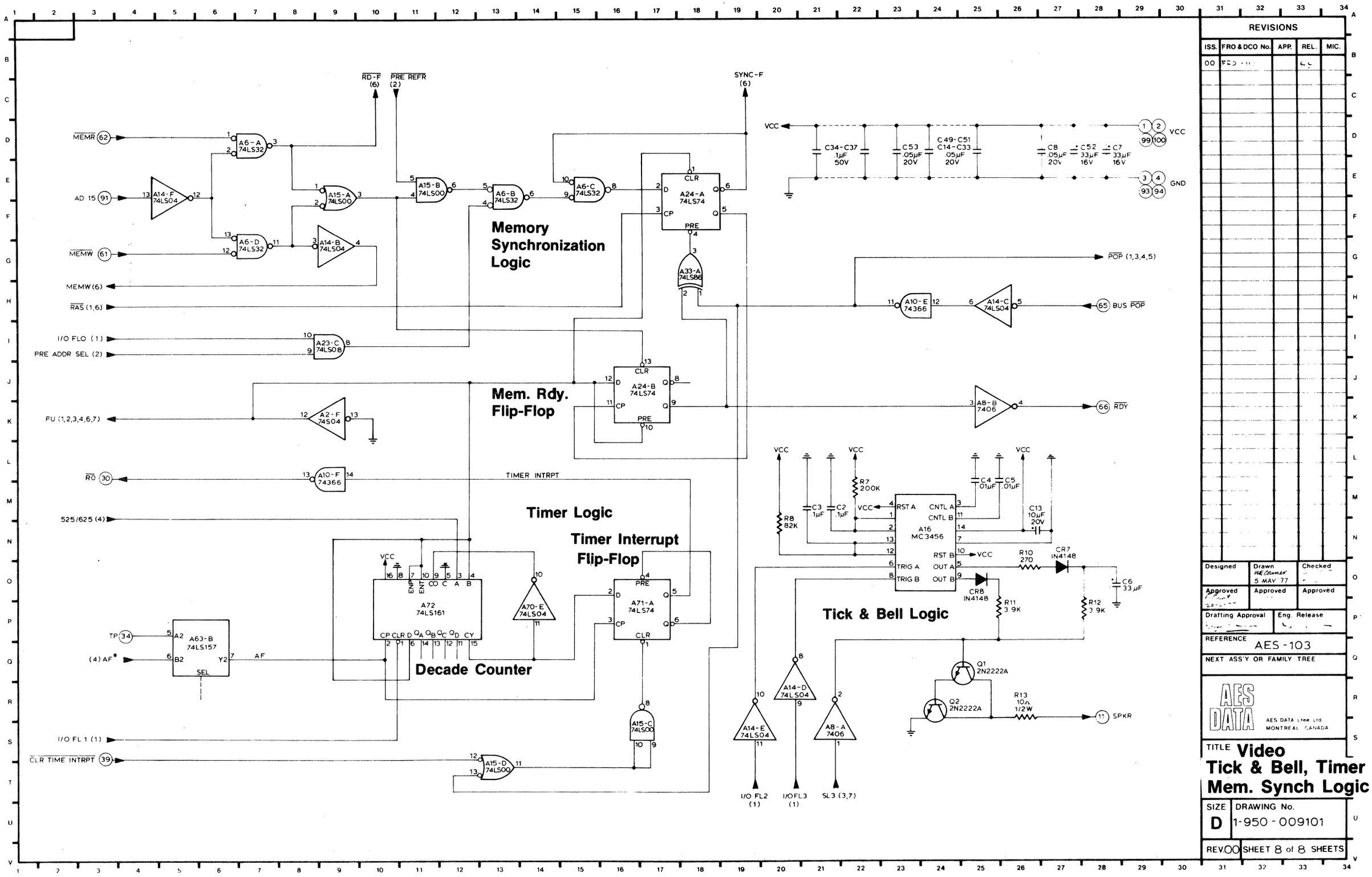
AES DATA Ltee Ltd
MONTREAL CANADA

TITLE **Video Output Logic**

SIZE	DRAWING No.
D	1-950-009101

REV 00 SHEET 7 of 8 SHEETS

Video Schematic Diagrams



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ISS.	FRO & DCO No.	APP.	REL.	MIC.
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Designed	Drawn M.E. Cramer 5 MAY 77	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES-103

NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Tech Ltd MONTREAL CANADA

TITLE **Video Tick & Bell, Timer & Mem. Synch Logic**

SIZE	DRAWING No.
D	1-950-009101

REV.00 SHEET 8 of 8 SHEETS

	01	02	03	04	05				01	02	03	04	05		
	1					P.C.B. Drilling	C6-955-009101	A31,40,41,51,60	5					SN74LS298N	660-0237
	2					P.C.B. Extractor	252-0102	A17	1					SN74365AN	660-0238
								A10	1					SN74366AN	660-0239
A18,26,27,35,36	9					Dynamic Ram	A6-937-004801	A37,48	2					SN74LS374N	660-0240
46,47,55,56								A25,28,57	3					DM81LS95N	660-0241
A49	1					Rom 256X4	6-908-001801	A64	1					3242	660-0250
A58	1					Rom 256X4	6-908-001802	A16	1					MC3456P	660-0254
A69	1					Rom 256X4	6-908-001803								
A39	1					Rom 256X4	6-908-001804	Q1,2,3	3					Transistor 2N 2222A	620-0101
A52	1					Rom 1K X4	6-908-001901								
A61	1					Rom 1K X4	6-908-001902	CR5	1					Diode IN4001	600-0112
A54	1					SN 74165N	660-0114	CR1,3,7,8	4					Diode IN4148	601-0104
A19	1					F9334	660-0121	CR4	1					Diode IN702A	602-0100
A2	1					SN74S04N	660-0145	CR2	1					Diode IN751A	602-0104
A8	1					SN7406N	660-0202	CR6	1					Diode IN752A	602-0105
A15,22,67	3					SN74LS00N	660-0208								
A14,70	2					SN74LS04N	660-0210	C9,13,52	3					Capacitor 10uF 20V. Tag.	164-0177
A23	1					SN74LS08N	660-0211	C6,7,11	3					Capacitor 33uF 16V. Tag.	164-0220
A5	1					SN74LS10N	660-0212	C8,10,12,14-33,	28					Capacitor .05uF	165-0251
A6	1					SN74LS32N	660-0215	38,49-51,53							
A13	1					SN74LS42N	660-0217	C1,4,5	3					Capacitor .01uF	165-0263
A3,24,45,53,71	5					SN74LS74AN	660-0219	C2,3,34,37,39-48	16					Capacitor .1uF	165-0347
A33	1					SN74LS86N	660-0220								
A63	1					SN74LS157N	660-0225	R3,4,5,6	4					Resistor 180 OHMS 1/4W 5%	402-0181
A4	1					SN74LS160AN	660-0226	R7	1					Resistor 200K OHMS 1/4W 5%	402-0204
A11,20,30,62	6					SN74LS161AN	660-0227	R18,19,20	3					Resistor 2.2K OHMS 1/4W 5%	402-0222
66,72								R1,2,10	3					Resistor 270 OHMS 1/4W 5%	402-0271
A32	1					SN74LS174N	660-0228	R14,17	2					Resistor 330 OHMS 1/4W 5%	402-0331
A21	1					SN74LS175N	660-0229	R12,11	2					Resistor 3.9K OHMS 1/4W 5%	402-0392
A34,65	2					SN74LS273N	660-0233	R15	1					Resistor 510 OHMS 1/4W 5%	402-0511
A12	1					SN74LS279N	660-0234	R8	1					Resistor 82K OHMS 1/4W 5%	402-0823
A29,38,44,50	6					SN74LS283N	660-0236	R13	1					Resistor 10 OHMS 1/2W 5%	411-0100
59,68								R16	1					Resistor 47 OHMS 1/2W 5%	411-0470

Video
Parts List

	01	02	03	04	05			06	07	08	09		
												P.C.B. Assy	A2-950-009101
Video Sig. J2	1					Connector 10 Pins	290-0120	1				P.C.B. Assy	A2-950-009102
Video Test J1	1					Connector 34 Pins	290-0123		1	1	1	P.C.B. Assy	A2-950-009103
A2,16	2					Socket DIL 14 Pins	698-0102	Y1				Crystal 15.75MHz (60Hz)	490-0115
A18,26,27,35,36	13					Socket DIL 16 Pins	698-0103	Y1				Crystal 15.625MHz (50Hz)	490-0117
39,46,47,49,55													
56,58,69								A43		1		Character Generator	6-907-000301
A43	1					Socket DIL 24 Pins	698-0106	A43			1	Character Generator	6-907-000201
A52,61	2					Socket DIL 18 Pins	698-0127	A43	1			Character Generator	6-907-000101
		1	1			P.C.B. Assy	A2-950-009101						
				1	1	P.C.B. Assy	A2-950-009102						
						P.C.B. Assy	A2-950-009103						
Y1		1				Crystal 15.75MHz (60Hz)	490-0115						
Y1			1			Crystal 15.625MHz (50Hz)	490-0117						
A43				1		Character Generator	6-907-000301						
A43					1	Character Generator	6-907-000201						
A43						Character Generator	6-907-000101						

THE INPUT/OUTPUT INTERFACE BOARD (D1-950-008901-00)

1. INTRODUCTION

The I/O Interface Board includes all the necessary logic circuits to interface the CPU with the various peripheral devices. These peripherals include a high-speed printer, a keyboard, one or two floppy diskette drives, several internal functions and two optional expansion boards. The board is divided into four logical groups:

- The Address Decoder
- The Keyboard Interface
- The Printer Interface
- The Disc Interface

2. FUNCTIONAL DESCRIPTION

2.1 THE ADDRESS DECODER

The decoder consist of 3-to-8 line decoders A33, A35, A17 and A41. It provides select signals for the peripherals including two sets of select lines for system expansion.

The decoder is fed by 7 address lines, AØ through A6, and two strobes, IOW and IOR. Decoder A33 issues address lines IO7, IO6, IO5 and IO4, used for system expansion, while the other three issue addresses for the printer, the keyboard and the disc drive.

2.2 THE KEYBOARD INTERFACE

This circuit includes devices A3, A4-A, A4-B, A1-C, A20-B, A19- B and A19-20.

Keyboard data is generated in ASCII code and stored in tri-state register A43(74LS374) when a key is pressed, thus generating the STROBE signal. This signal also sets one-shot multivibrator A19-B which in turn sets INTERRUPT flip-flop A20-B. The keyboard data is read when the RD KB signal goes low and at the same time the INTERRUPT flip-flop is cleared via gate A1-C(74LS08). The REPEAT key is used whenever a specific character is displayed as a string on the video screen. When pressed simultaneously with a character key, the output of A19-A goes low and is fed back to A19-B. When the STROBE signal is received, both one-shots of A19 form an oscillator, causing flip-flop A20-B to send an interrupt to the CPU every 35 milliseconds.

2.3 THE PRINTER INTERFACE

This interface allows the video memory contents to be printed. It comprises devices A9, A42, A34, A35, A36, A10, A2, A26, A43, A51, A49 and A50.

The operating principle of the interface consists of channelling data, read from the data buss, through buffers and then formatting them into the 12-bits buss required by the printer. Seven strobe signals are also fed to the printer. During the operation of the printer, ten status flags are returned to the interface so that the CPU may constantly assess the printing process.

Data bits issued by the 8080A arrive at the interface through buffers A9 and A42(8095). The first six most significant bits (PTR 8 through PTR13) are loaded first into D-type latch A34 at the positive-going edge of the LDPTR-1 strobe at which time the original 6-bits are transferred to latch A35. The following eight bits are then loaded into A34 at a second LD PTR1 strobe. The twelve bits formed are then fed to the printer via drivers A26 and A36. Strobe signals to the printer are issued by nand buffers A43 and A51. Data bit 7 is stored in flip-flop A10-B and becomes the ribbon control bit. The ten-bit status lines supplied by the printer are terminated by resistor network A50 and applied to tri-state driver A49, delivering printer status to the data buss. Status lines CHECK, PAPER FEED RDY and CHAR RDY are inverted through A18 and applied to flip-flop A10A, A2-A and A2-B. Their outputs are ored by A11-A and A1-A to issue the PTR INTRPT flag.

2.4 THE DISC DRIVE INTERFACE

The AES-PLUS Text Editor allows the use of two miniature floppy disc drives of the Shugart Model 400 type. The two disc drives are controlled by two independent interfaces where selection is accomplished by multiplexers on the I/O board itself. Each drive has its own sector counter and ready flag signals.

a) Sector Search Scheme: A photo-transducer, mounted on the disc drive mechanism, generates a pulse each time a hole appears on the magnetic disc. There are 16 holes punched on the inner circumference of the disc plus one index hole, therefore 17 pulses are generated.

The sector pulses from both disc drives arrive at the I/O board and are applied to inverters A4-E and A6-C. These pulses are then brought to one-shot multivibrator A14-A (for disc drive 1) where the specified time constant reduces their width. The separation of the index and sector pulses is produced by one-shot multivibrator A16-A in conjunction with gates A47-C, A22-B and A23-A. The Q output of A14-A is fed to pin 11 of A16-A where each pulse is stretched to 9 milliseconds at the output, due to its long time constant. Since the rotating disc creates a 12.5 millisecond period between each sector pulse and the index hole is located at midpoint between two sector holes, the output of A16-A will remain low during that entire period. The following index hole pulse is then issued by the Q output of A14-A which will clear counter A30 via gate A22-B.

The 9 millisecond pulse is applied to Nand gates A22-B and A23-A. The Q output of A14-A is also applied to A23-A which outputs clock pulses to 5-bits binary counter A30(74LS393).

Since provision has been made for a 32 sector diskette, sector counter bit SCT4-1 is applied to one section of multiplexer A5 whose output is tied to a strapping pin, allowing for the option. The outputs of counters A28 and A30 are then fed to multiplexer A29, whose output is selected by the DRIVE SEL signal, and then to 6-bit comparator (DM8160) A37 where comparison occurs between the value of the sector to be addressed, stored in sector register A38(74LS273), and the output value of the sector counter. When both values become equal, the SECT EQ signal is issued to flip-flop A12-A of the DMA (Direct Memory Access) logic. Sector register A38 also drives LED's Ø and 1, indicating the disc drive in service.

b) Track Access Logic: This circuit generates the DIRECTION signal, defining the direction of motion of the R/W head and the STEP signal which moves the head in the selected direction. The direction signal is issued by the data buss through register A52(73LS273) while the STEP signal originates from the address decoder. Both signals are issued to the disc drive by drivers A53 and A8.

c) Disc Drive Select: Selection of the disc drives is accomplished by the address decoder, multiplexer A29, data bits Ø and 1 for selecting the R/W head and bit 7 for the Drive Select strobe. After the selection, each disc drive receives its own WRT GATE, HEAD LD, MOTOR ON and WRITE DATA signals.

Each disc drive issues three status flags which are multiplexed by A5. These are the TRKØØ, the READ DATA an thed WRITE PROT. The status flag lines are terminated by resistor network A7.

Both DSK RDY strobes are derived from the sector pulse train. For instance, the output of gate A23-A is fed to one-shot multivibrator A13-B, where the pulse train is transformed into one pulse with a period of approximately 25 milliseconds and then applied to flip-flop A21-a.

d) The USRT and Associated Logic: USRT A46 (COM 2601) operates in conjunction with devices A44, A45, A54, A31, A32, A23, A39, A24, A31 and A47. This logical subsystem performs all the transmitting and receiving functions of data between the disc drive and the AES-PLUS Text Editor.

The transmitting rate of the USRT is derived from a 4 MHz crystal controlled clock oscillator, formed by inverters A56-E and A56-F, whose output is fed to flip-flop A54-A, where division by two occurs. The 2 MHz clock signal is then applied to counter A55, whose most significant output bit is inverted by A56-A and finally applied to the TCP (Transmitter Clock) input of the USRT. Data to be transmitted is fed to the USRT from the data buss and when the TSS (Transmitter Sync Strobe) input receives a high level issued by decoder A41, data is loaded into the transmitter sync register. At this moment in time, the transmitter sync register contains a header of zeroes , a flag character (DB) and data. Data transfer is inhibited until DB is transfered to the transmitter buffer register, this setting TDS. When TDS is set, data transfer is enabled. The flag character is immediately followed by a valid data byte, which is released serially from USRT serial output TSO (Transmitter Serial Output).

The data to be stored on the disk has to appear in the form of a modulated signal, usually in a dual frequency signal. This is achieved by using the three least significant bits of counter A55 and routing them to gate A31-A. Its output changes state at each count of 8 and is mixed with the USRT serial output at gate A7-B.

When the USRT is receiving data, the modulated data stream coming from the disc drive circuitry has first to be processed since it contains both the receiver clock signal and the data. This signal processing takes place at gate A23-B and A23-C, one-shot multivibrator A39 and flip-flop A32-B, where the clock signal and the data are separated. One-shot multivibrator A39 stretches the pulses coming from A23-B and feeds them to the RCP (Receiver

Clock) input of the USRT. The combined receiver clock signal and the modulated data stream are applied to gate A23-C which issues the DATAS signal to the PRESET input of flip-flop A32-B. The output of A23-B also clocks A32-B and the resulting signal at its Q output is the valid serial data fed to the RSI (Receiver Serial Input) input of the USRT. When an entire character has been received, the RDA (Receiver Data Available) output flag goes high; the character is unloaded onto the data buss and then the RDAR resets the RDA to a lowlevel. The unloading of a character on the data buss is accomplished through tri-state multiplexers A44 and A45(74LS257), which are also used for disc drive status flag drivers.

e) The DMA (Direct Memory Access) Logic: The DMA circuit informs the CPU that data is to be exchanged between the disc and the video memory. The disc drive employs two DMA channels, one for the transmit function and one for the receive function of the USRT.

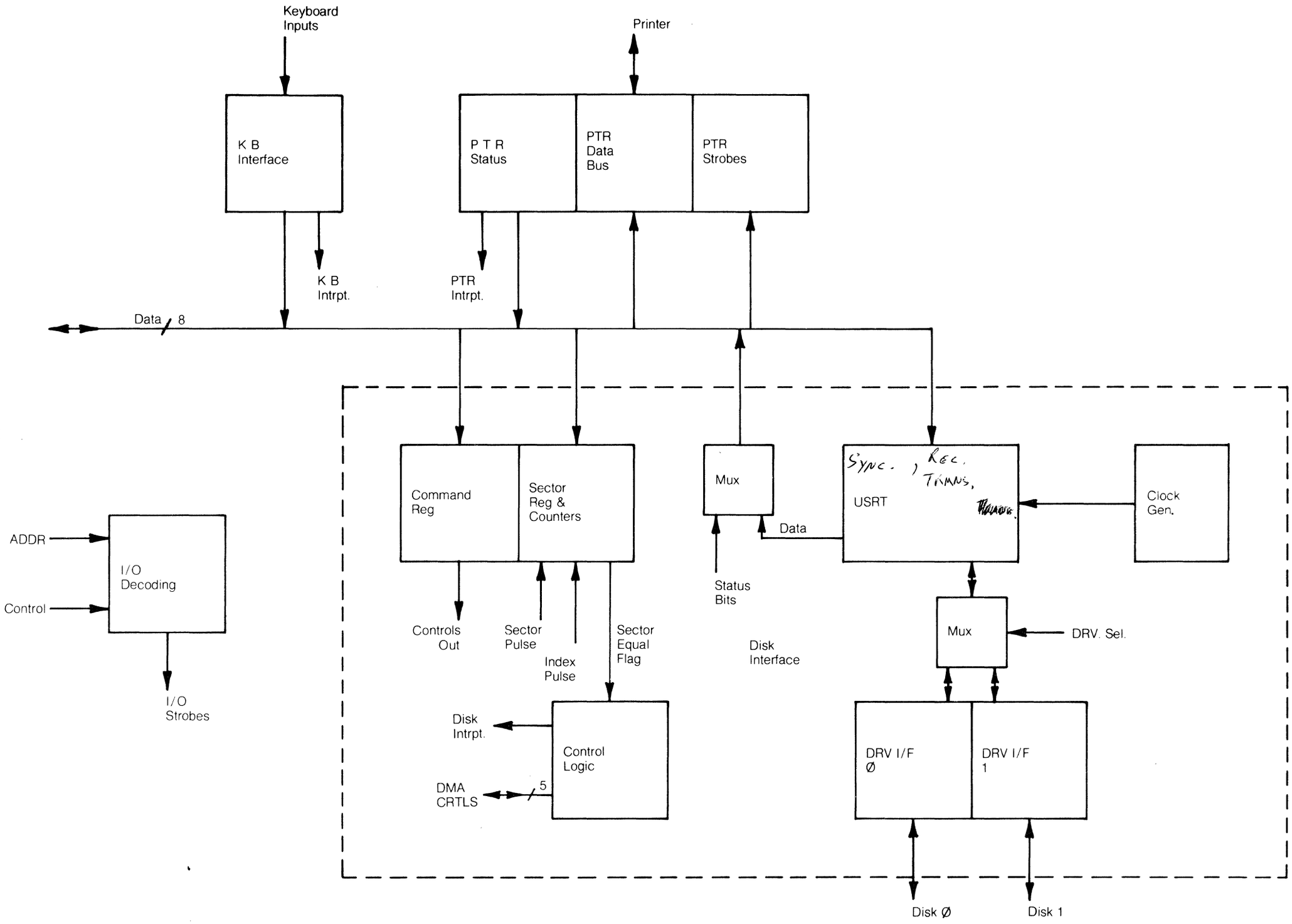
All disc activities are only allowed when the microprocessor has issued the disc activity flag. When this is so, the SECT EQ flip-flop A12-B is enabled. As soon as the SECT EQ pulse is issued from comparator A37, the SECT EQ F strobe from A12-B goes high and is fed to gate A31-B which issues the DMA Request Ø (DRQØ) to the first channel of the DMA controller on the CPU board. The DMA Request is acknowledged by the DACKØ strobe arriving at inverter A27-D and then to gate A24-A, setting high its output which is then applied to the TDS (Transmitter Data Buffer Strobe) input of the USRT. Data is then loaded into the USRT data buffer for transmission to the disc and when the required number of bytes has been transferred, the TBMT output goes low and cancels the DMA Request. The ACTIV-F flag is reset when the next sector is encountered.

In the Transmit mode, characters are loaded from the data bus into the USRT transmitter data buffer register. In this case, a character from the program memory is transferred to the USRT under the control of the DMA circuit chip on the CPU board. However, disc activities are allowed only when the CPU has set the disc activity flag (SET ACT F) via address decoder A41.

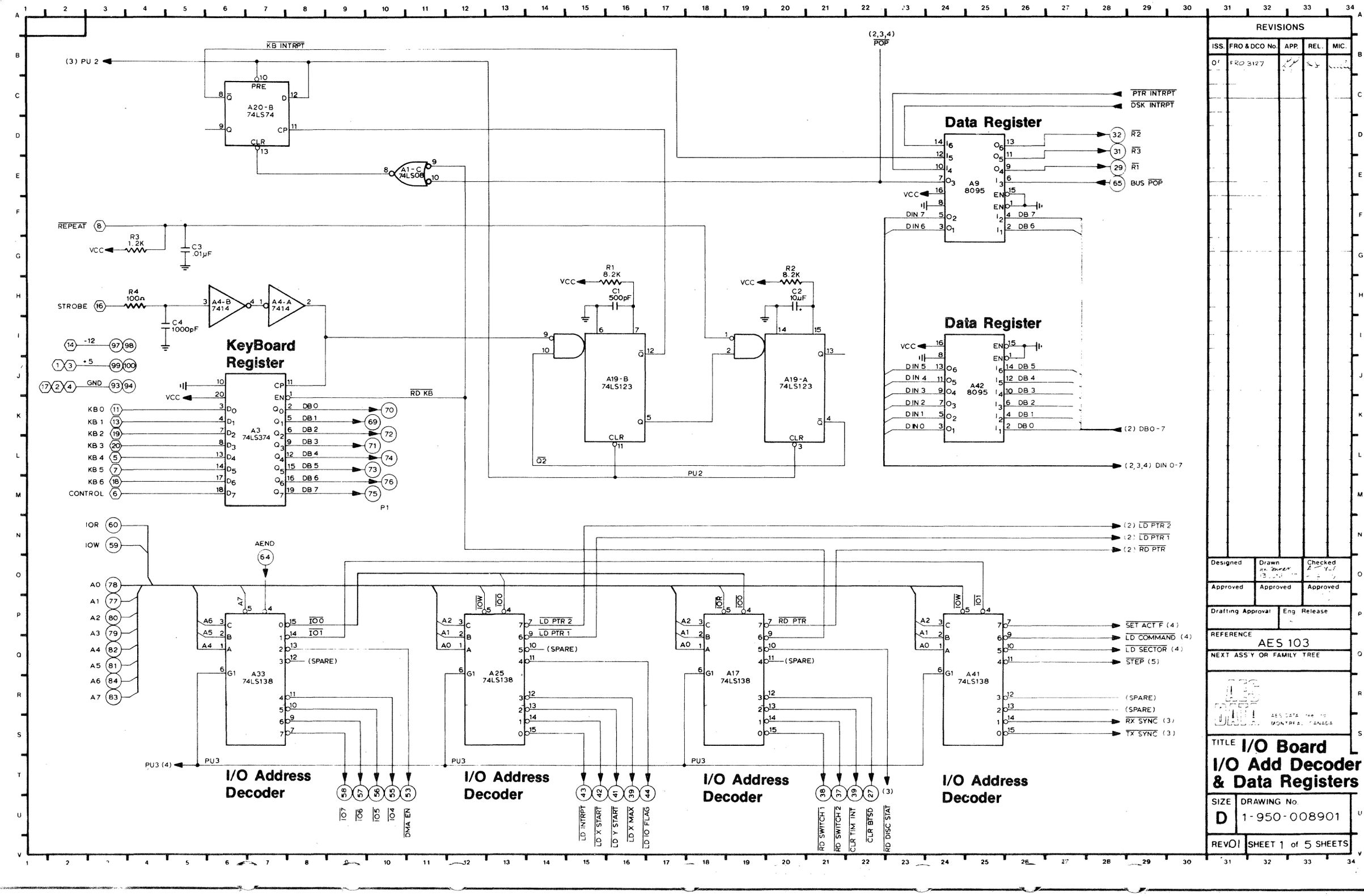
In the Receive mode, characters are retrieved from the disc sector. Once the Read function is established, the DMA cycle is initiated at the second channel (RDQ1 and DACK1) by the RDA (Receiver Data Available) output of the USRT and DMA acknowledgment is given at the RDAR (Receiver Data Available Reset) input of the USRT.

When a DMA cycle has terminated for a disc Read function, the DMA controller issues a TC (Terminal Count) flag, which appears at gate A11-C and resets the ACTIV-F strobe of flip-flop A12-A. Interrupt flip-flop A32-A is then set via gate A22-C and an interrupt flag is issued to the CPU. This flag is cleared later when the CPU reads the disc status.

I/O Board Block Diagram



Input/Output Schematic Diagrams



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.
01	FRO 3127			

Designed	Drawn	Checked
Approved	Approved	Approved
Drafting Approval	Eng Release	

REFERENCE AES 103

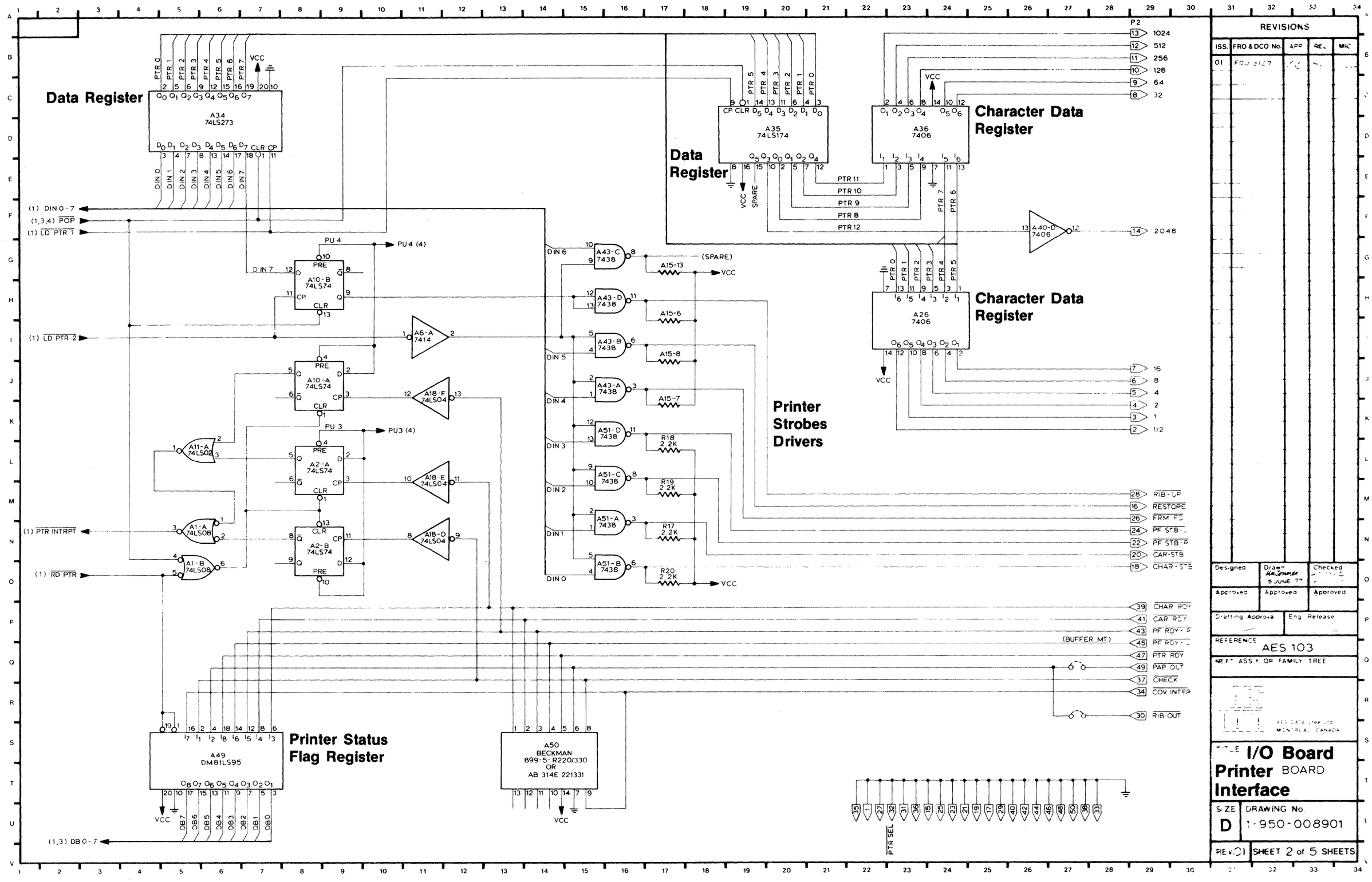
NEXT ASS'Y OR FAMILY TREE

AES DATA (1981) LTD. MONTREAL, CANADA

TITLE **I/O Board I/O Add Decoder & Data Registers**

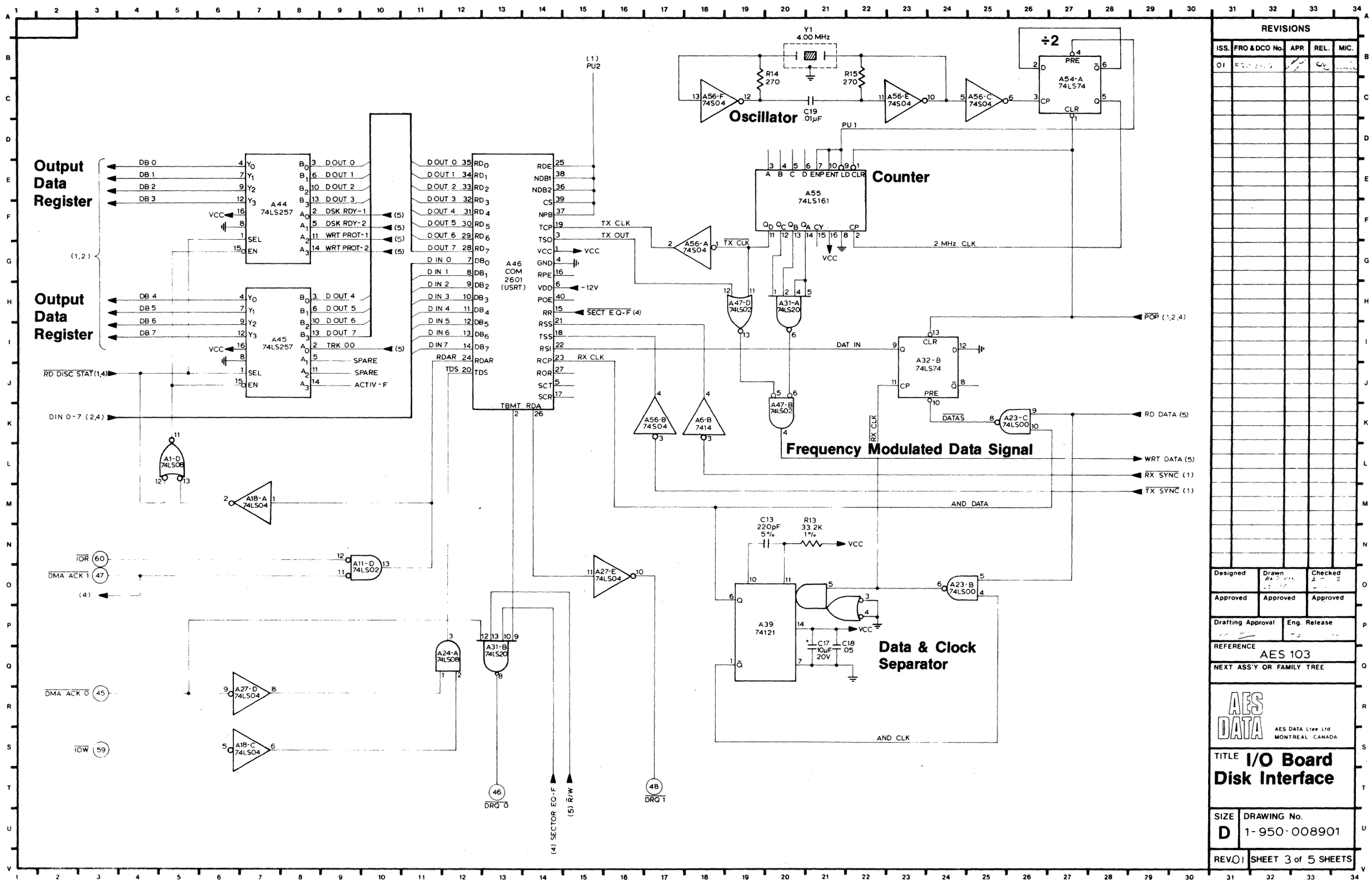
SIZE	DRAWING No.
D	1-950-008901

REV 01 | SHEET 1 of 5 SHEETS



Input/Output Schematic Diagrams

Input/Output Schematic Diagrams



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.
01	[illegible]	[illegible]	[illegible]	[illegible]

Designed	Drawn	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES 103

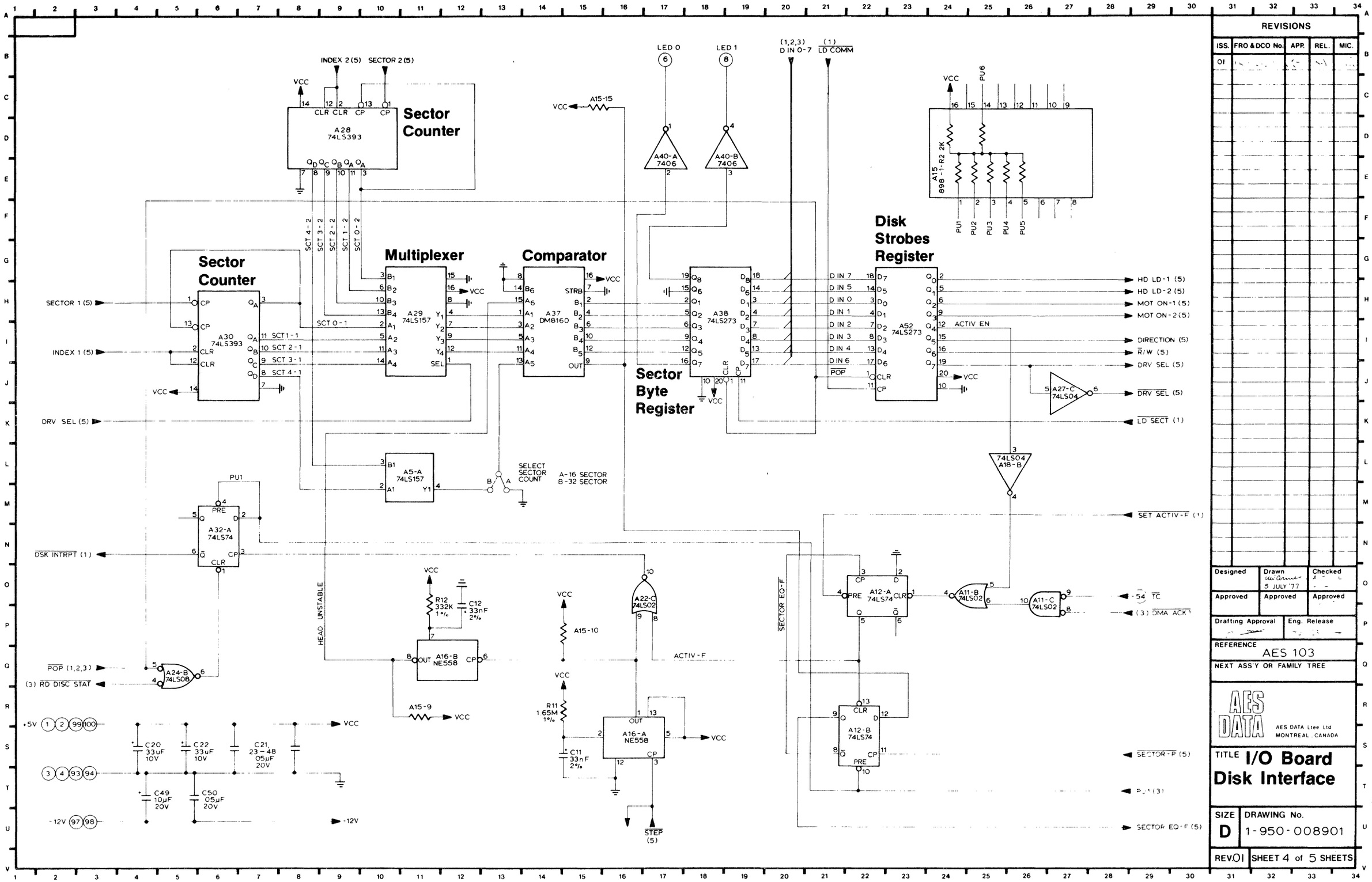
NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee Ltd MONTREAL CANADA

TITLE **I/O Board Disk Interface**

SIZE	DRAWING No.
D	1-950-008901

REV.01 | SHEET 3 of 5 SHEETS



REVISIONS

ISS.	FRO & DCO No.	APP.	REL.	MIC.
01				

Designed	Drawn 5 JULY '77	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES 103

NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee Ltd MONTREAL, CANADA

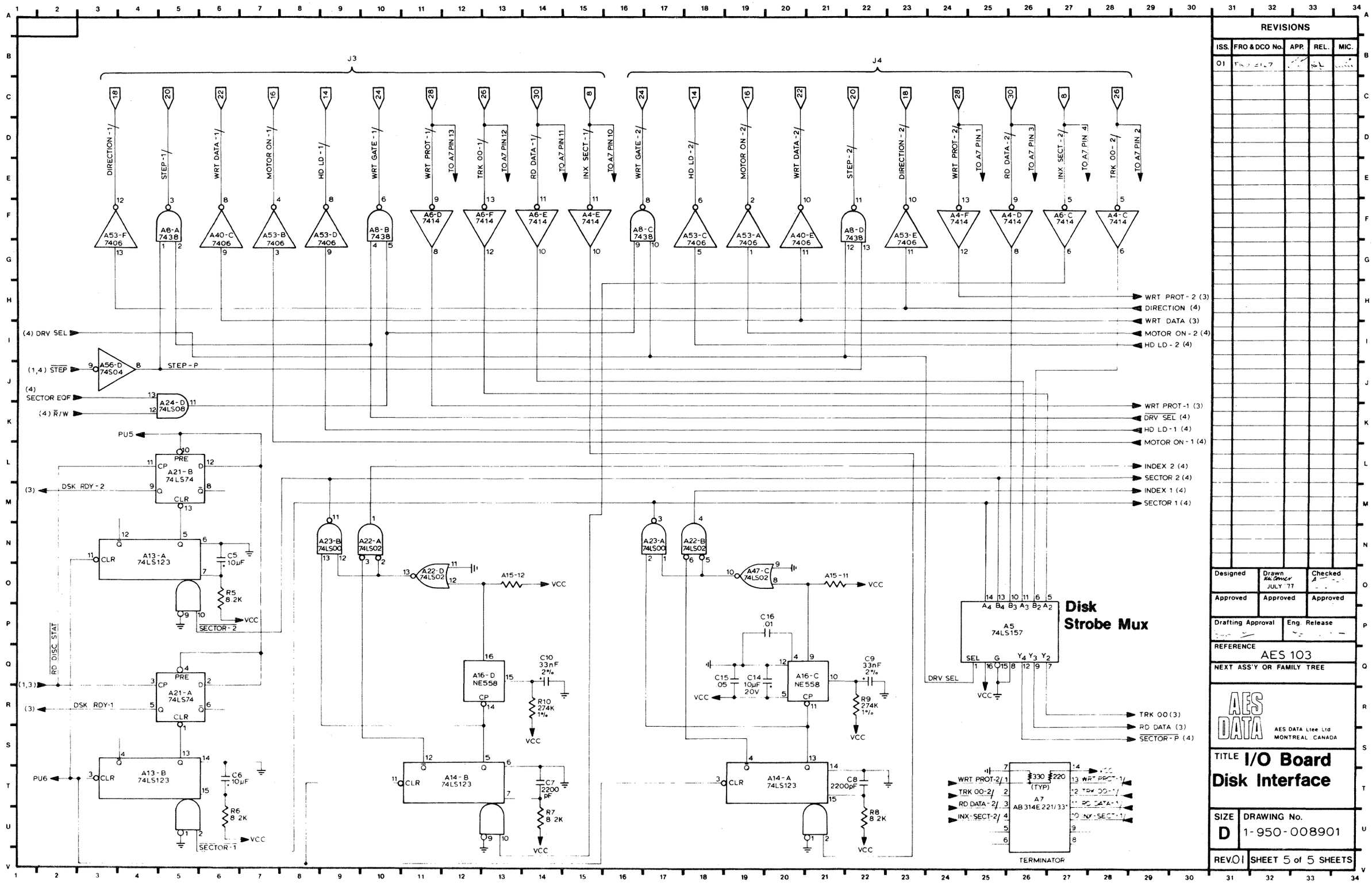
TITLE **I/O Board Disk Interface**

SIZE	DRAWING No.
D	1-950-008901

REV.01 | SHEET 4 of 5 SHEETS

Input/Ouput Schematic Diagrams

Input/Output Schematic Diagrams



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.
01	[illegible]	[illegible]	[illegible]	[illegible]

Designed	Drawn MK Dimock JULY '77	Checked [illegible]
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES 103

NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee Ltd MONTREAL CANADA

TITLE **I/O Board Disk Interface**

SIZE	DRAWING No.
D	1-950-008901

REV.01 | SHEET 5 of 5 SHEETS

	01		
	1	PCB Drilling	C6-955-008901
	2	PCB Ejector	252-0102
A56	1	SN74S04N	660-0145
A8,43,51	3	SN7438N	660-0129
A46	1	COM 2601	660-0142
A4,6	2	SN7414N	660-0162
A17,25,33,41	4	SN74LS138N	660-0192
A26,36,40,53	4	SN7406N	660-0202
A23	1	SN74LS00N	660-0208
A11,22,47	3	SN74LS02N	660-0209
A18,27	2	SN74LS04N	660-0210
A1,24	2	SN74LS08N	660-0211
A31	1	SN74LS20N	660-0214
A2,10,12,20,21 32,54	7	SN74LS74AN	660-0219
A39	1	SN74121N	660-0221
A13,14,19	3	SN74LS123N	660-0222
A5,29	2	SN74LS157N	660-0225
A55	1	SN74LS161AN	660-0227
A35	1	SN74LS174N	660-0228
A44,45	2	SN74LS257AN	660-0232
A34,38,52	3	SN74LS273N	660-0233
A9,42	2	SN74365AN	660-0238
A3	1	SN74LS374N	660-0240
A49	1	DM81LS95N	660-0241
A37	1	DM8160N	660-0255
A28,30	2	SN74LS393N	660-0256
A16	1	NE558	660-0257
A7,50	2	Resistor Pack 314E221331	485-0110
A15	1	Resistor Pack 898-1-R2.2K	485-0111

	01		
C13	1	Capacitor 220pf 5%	167-0100
C9,10,11,12	4	Capacitor .033uF 2%	162-0133
C2,5,6,14,17,49	6	Capacitor 10uF 20V. Tag	164-0177
C20,22	2	Capacitor 33uf 16V. Tag	164-0220
C1,7,8	3	Capacitor 500pf	165-0207
C15,18,21,23-48 50	29	Capacitor .05uF	165-0251
C3,4,16,19	4	Capacitor .01uF	165-0263
R4	1	Resistor 100 OHMS 1/4W 5%	402-0101
R3	1	Resistor 1.2K OHM 1/4W 5%	402-0122
R16-20	5	Resistor 2.2K OHMS 1/4W 5%	402-0222
R14,15	2	Resistor 270 OHMS 1/4W 5%	402-0271
R1,2,5-8	6	Resistor 8.2K OHMS 1/4W 5%	402-0822
R12	1	Resistor 332K OHMS 1/4W 1%	481-0651
R9,10	2	Resistor 274K OHMS 1/4W 1%	481-0730
R13	1	Resistor 33.2K OHMS 1/4W 1%	481-0551
R11	1	Resistor 1.65M OHM 1/4W 1%	481-0734
KB	1	Connector PCB 20 Pins	290-0121
J3	1	Connector PCB RT.Ang. 34 Pins	290-0122
J4	1	Connector PCB 34 Pins	290-0123
A39,A56	2	Socket DIL. 14 Pins	698-0102
A13,14,16,19	4	Socket DIL. 16 Pins	698-0103
A46	1	Socket DIL. 40 Pins	698-0118
Y1	1	Cystal 4.000 MHz	490-0112

1. INTRODUCTION

The Central Processing Unit of the AES-PLUS Text Editor is contained on a single printed circuit board. It includes an integrated microprocessor CPU (INTEL 8080), 32K of Instruction RAM (random access memory) small Bootstrap ROM (read-only memory), one 8-level priority interrupt controller and a 4-channel DMA (direct memory access) controller. Provision has been made for instruction bit parity check, in case of memory failure and also two 8 D.I.P. switch packs to determine the configuration of the system.

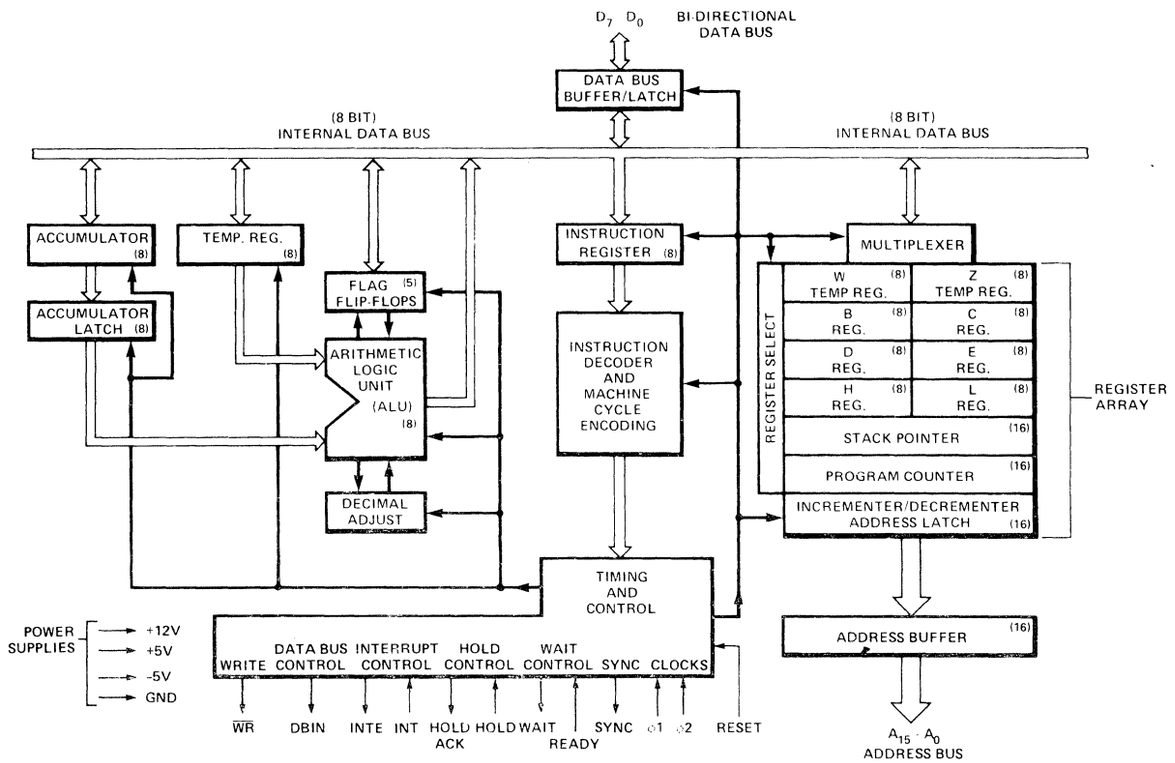
The board consists of the following subgroups:

- The 8080 Microprocessor
- The Interrupt Logic
- The DMA Controller
- The Instruction Memory
- The Memory Synchronization Circuit
- The Address Decoder
- The Program Switches
- The Parity Check Logic

2. THE MICROPROCESSOR

The basic processor consists of an Intel 8080A Microprocessor chip, (see FIG.1) associated timing circuit and a buss driver. The 8080A is a complete 8-bit parallel central processing unit supplying a 16-line address buss, a separate 8-line bi-directional data buss and all the control signals to interface with the memory and Input/Output peripherals.

Figure 1 The Microprocessor



The 8080A Microprocessor chip is interfaced with Clock Generator A5-(8224) and a bi-directional data buss driver (8228) to form the CPU module. The clock generator is a single chip device, controlled by an 18.0 MHz crystal, supplying the two-phase clock signals Ø1 and Ø2 a power-up RESET, a READY flag and advance status strobe (STSTB). The READY flag is a product of the RDY IN in sync with phase Ø2 while the STSTB strobe is formed by the SYNC strobe, issued by A30 and phase Ø1 of the clock.

The bi-directional buss driver and system controller A30 (8228) generate all the signals required to interface with the Random Access Memory and I/O. The 8228 accepts the data buss from the 808 Microprocessor and distributes it to the system. It also generates strobe signals MEMR, MEMW, I/OR, I/OW and INT ACK.

Figure 2 C.P.U. Module

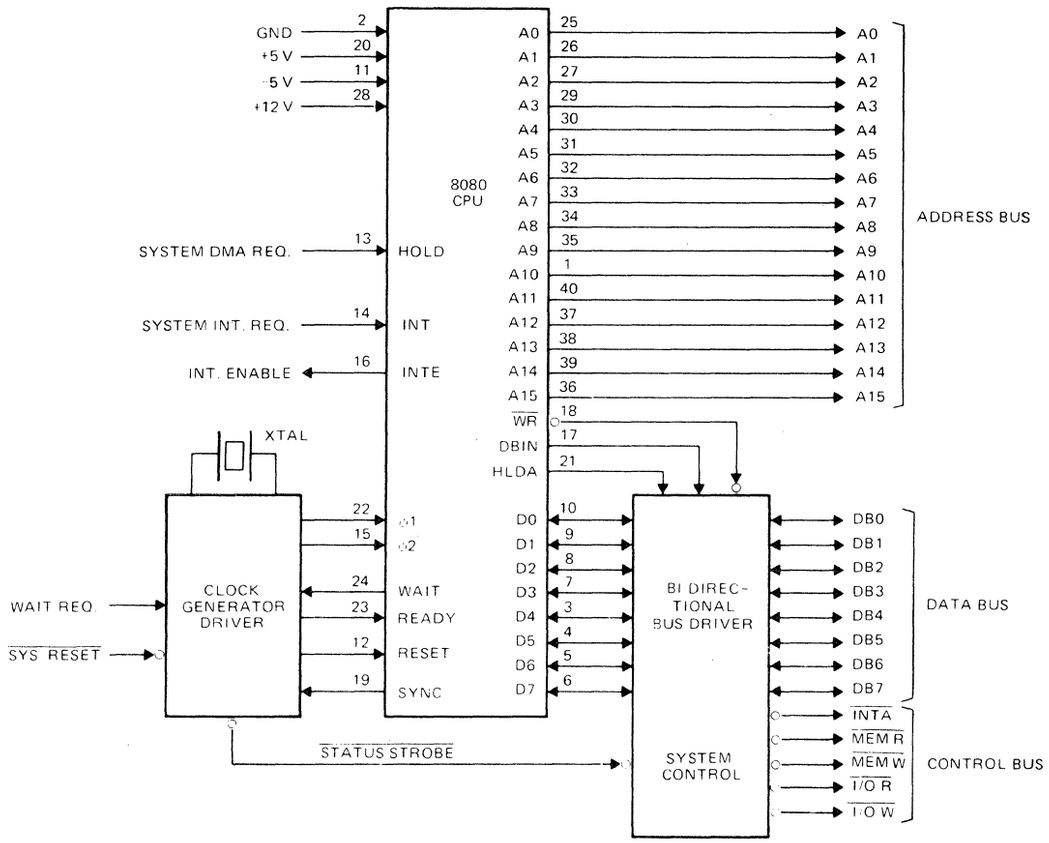


Figure 2 is representative of what constitutes the basic CPU module. The basic CPU Module communicates with the instruction memory, the DMA controller, the interrupt controller and bootstrap ROM via a 16-bit address buss, an 8-bit data buss and 5 control lines. The 16-bit address lines are buffered through A49 and A58 (81LS95) and brought to the memory logic. The eight data bits issued by A30 are buffered by drivers A57 and A48 (8216).

3. THE INTERRUPT LOGIC

The Interrupt Logic consists of devices A28(8214), being an integrated priority interrupt control unit, and A46 (8212) which is an eight bit latch with tri-state output buffers. Eight interrupt requests are applied to A28 for the timer, the printer, disk, keyboard, option 1 and option 2, COM1 and COM2. These interrupt flags are encoded and compared to the contents of a status register, fed by bits DBØ to DB3 from the data buss. An interrupt is then issued along with vector information to I/O port A46. The Interrupt Controller is clocked by the Ø2TTL signal, issued by A5 and enabled by INTE (Interrupt Enable) coming from the microprocessor.

I/O port A46 accepts the three vector bits at its DI4, DI5 and DI6 inputs and the interrupt flag. Unloading data on the data buss is accomplished by the INTA (Interrupt Acknowledge) and DBIN strobes. The interrupt flag is then brought to the 8080A.

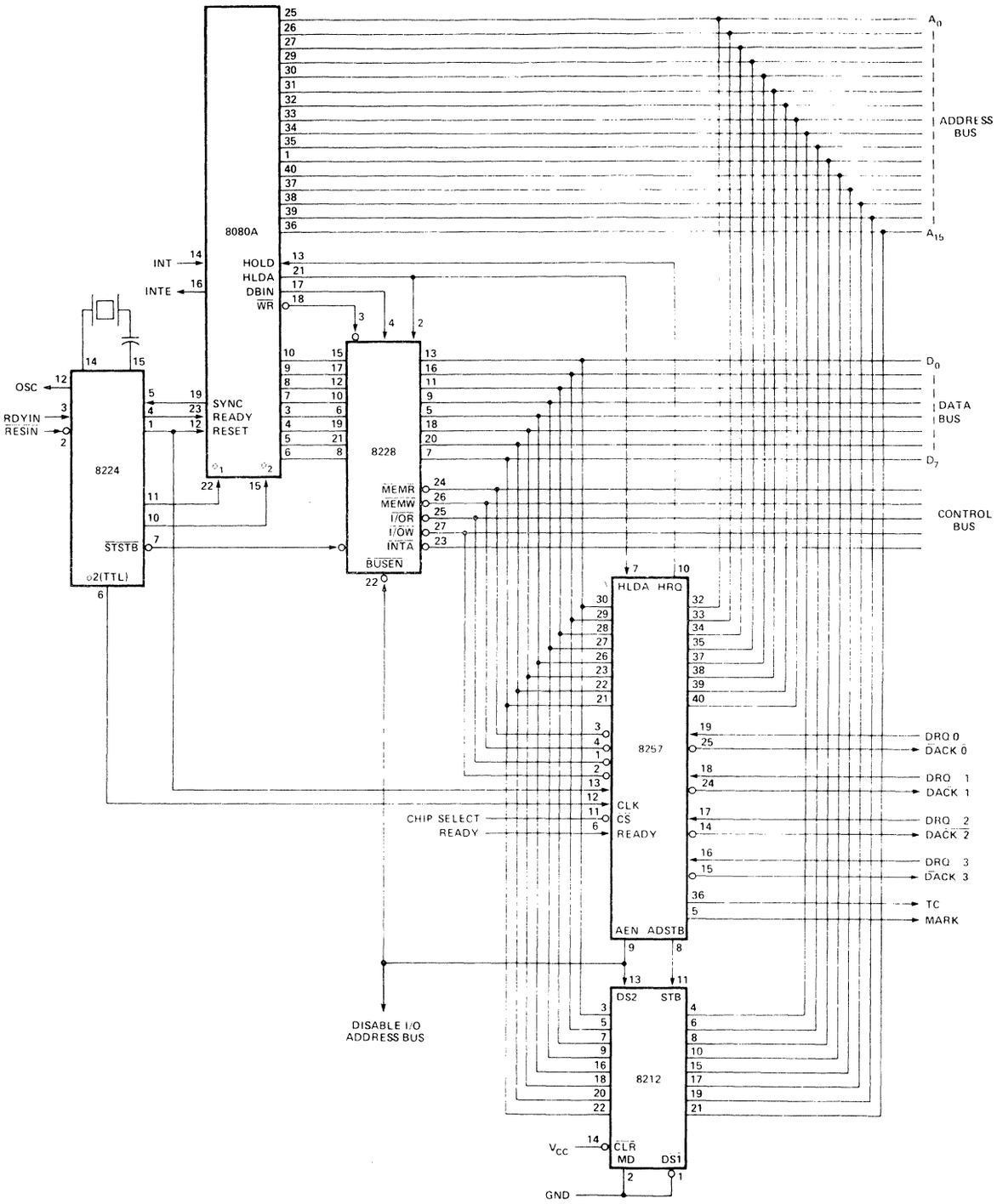
4. THE DMA (DIRECT MEMORY ACCESS) CONTROLLER

This subgroup consists of programmable DMA controller chip A3 (8257) and octal D-type latch A39(74LS374) (see FIG 3).

The DMA Controller generates a 16-bit address to the memory during the transfer of data from the memory to the disc storage media. When an I/O device requests the DMA, a priority selection occurs and a HOLD strobe is issued to the Microprocessor which responds with a HOLD ACK strobe. DMA chip A3 supplies four request channels, two of which are used for the disc Read and Write functions while the two others may be used for later expansion.

The DMA request appears in the form of a strobe signal at the DRQ Ø input of a channel and the request is then acknowledged by the return of a DACK strobe to the I/O. The 16-bit address is formed by the DMA chip, which generates the 8 least significant bits and 3-state octal latch A39, which generates the 8 most significant bits.

Figure 3 C.P.U. Module With DMA



THE INSTRUCTION MEMORY

This memory has a capacity of 32K x 9 bits and utilizes 16K RAM devices. The memory is accessed through 16 address lines, issued by the microprocessor, and unloads 8-bit instruction bytes onto the data buss. The ninth bit is used internally for parity checking (error detection). A 512 x 8-bit instruction ROM (A51-74LS472) contains program loading instructions for Bootstrapping.

The 16-bit address buss accesses the memory via latches A50 (74LS273) and A59 (74LS174), both clocked by the RAS B signal.

When the AES-PLUS Text Editor is first turned on, memory instructions have to be loaded from a program diskette into the RAM. This is accomplished by a Bootstrap Flag issued by quadruple flip-flop A12 on the video board. This flag is brought to OR gate A67-C whose output is fed to decoder A32(7442). The EN ROM signal is then issued to ROM A51, which in turn unloads instruction bytes onto the data buss. After the program is loaded into the RAM, address decoder A17 on the I/O board issues a CLR BTSP (clear bootstrap) strobe to quadruple flip-flop A12.

Henceforth, the Microprocessor has access to the 32K RAM. The 16 address bytes are then brought to address multiplexer and refresh counter chip A41(3242) which distributes addresses to the RAM chips. Memory controller A41 contains its own refresh address counter, which is enabled by BUS REFR issued by octal latch A65 of the video board. Each RAM device is controlled by two addressing strobes called RAS* (Row Address Strobe) and CAS *(Column Address Strobe) also issued by the video board.

These two strobes allow the loading of the row and column addresses in a sequential manner. The WE strobe (Write Enable) goes low during program loading.

Instruction bytes are, thereafter, loaded onto the data buss via tri-state latches A6 and A15(74LS374).

6. MEMORY SYNCHRONIZATION

This circuit consists of devices A67, A65, A55, A66 and A64. Its purpose is to control memory request from the Microprocessor between refresh cycles.

A memory request is started by bit 15 (when low) which enables gate A67-A in unison with a MEMR or MEMW strobe. If a memory PRE REFR strobe has not appeared at gate A-57D, the request is brought to flip-flop A64B which sets the SYNC-F strobe at the next edge of the RAS* signal. From this point on, the memory is read until the next edge of the RAS* signal clears the SYNC-F and sets memory flip-flop A64-A which in turn issues the MEM RDY signal on the data bus. When bit 15 of the address buss goes high again, flip-flop A64-A is cleared and the MEM RDY signal is removed.

7. THE ADDRESS DECODER

Decoder A19 is a 4-to-10 line decoder (74LS42) and accepts the SYNC-F, the WRT MEM, the BUS ROWEN and address bit 14. The decoded signals produce a Write pulse to the appropriate bank of RAM chips (WEA or WEB). Decoder A32 accepts address bit 14 and decoded bits 9, 10, 11, 12 and 13 and issues an enabling strobe (ENA or ENB) to either banks of RAM chips or the EN ROM strobe to the bootstrap ROM.

8. THE PROGRAM SWITCHES

These are two packages of 8 D.I.P switches followed by tri-state buss drivers A45 and A54(81LS95). The Microprocessor reads the switch status when strobes RD SW1 or RD SWØ are issued. The programm

SWITCH BLOCK Ø

DB Ø	Software
1	
2	
3	
4	Unallocated
5	
6	
7	

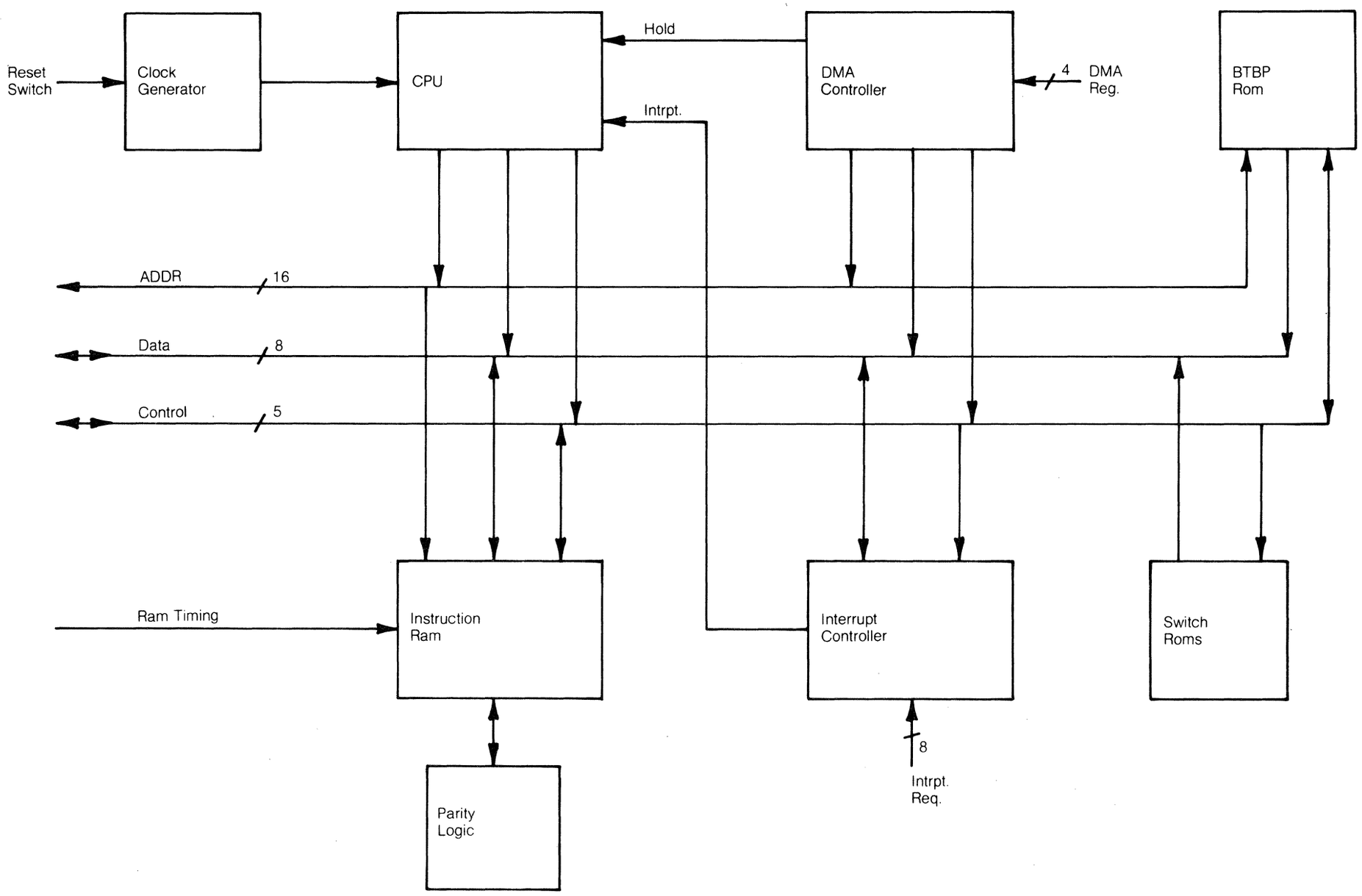
SWITCH BLOCK 1

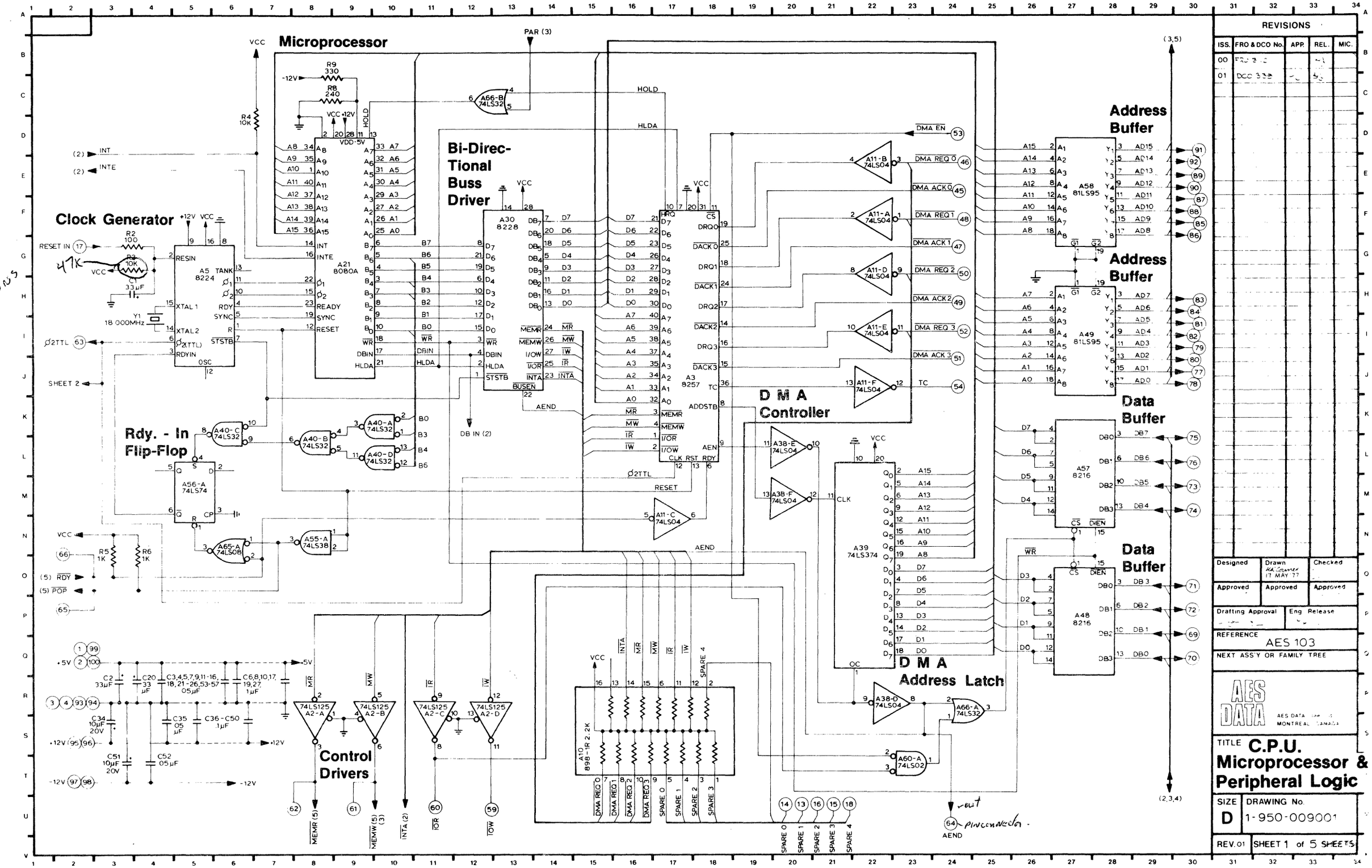
DB Ø	Unallocated
1	
2	
3	
4	
5	
6	Bootstrap Loader Enable
7	Parity Enable

9. THE PARITY CHECK LOGIC

This circuit consists of devices A33, A72, A63, A69, A60, A56-B and A55-D. Its purpose is to constantly verify the validity of data read from the memory. The heart of the circuit consists of a 9-bit odd/even parity generator/checker, device A33(74LS280), and accepts at its input the 8-bit data buss. When data is written into the memory, A33 generates a parity bit (even parity) into 9th RAM chip A72, if enabled and addressed. When data is read from the memory, the parity is also read from A72 and is applied to parity chip A33 via a multiplexer (for Parity A or B) formed by gates A60-C, A60-B and A66-D. The EVEN output of the parity chip is inverted by A55-C and brought to flip-flop A56-B, which sets its Q output if an error is detected. Flip-flop A 56-B is clocked by PAR CLK issued by A69-B. The Q output is fed to OR gate A66-B. A detected error will force a HOLD request on the Microprocessor. The request will maintain the Microprocessor in a halt mode until the system is reset. A L.E.D on the front panel of the Text Editor turns on when the system is halted.

C.P.U. Board Block Diagram





REVISIONS

ISS.	FRO & DCO No.	APP.	REL.	MIC.
00	FRO 3 [illegible]		[illegible]	
01	DCO 338	[illegible]	[illegible]	

Designed	Drawn K.A. Gruner 17 MAY 77	Checked
Approved	Approved	Approved
Drafting Approval	Eng Release	

REFERENCE AES 103

NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA [illegible] MONTREAL [illegible]

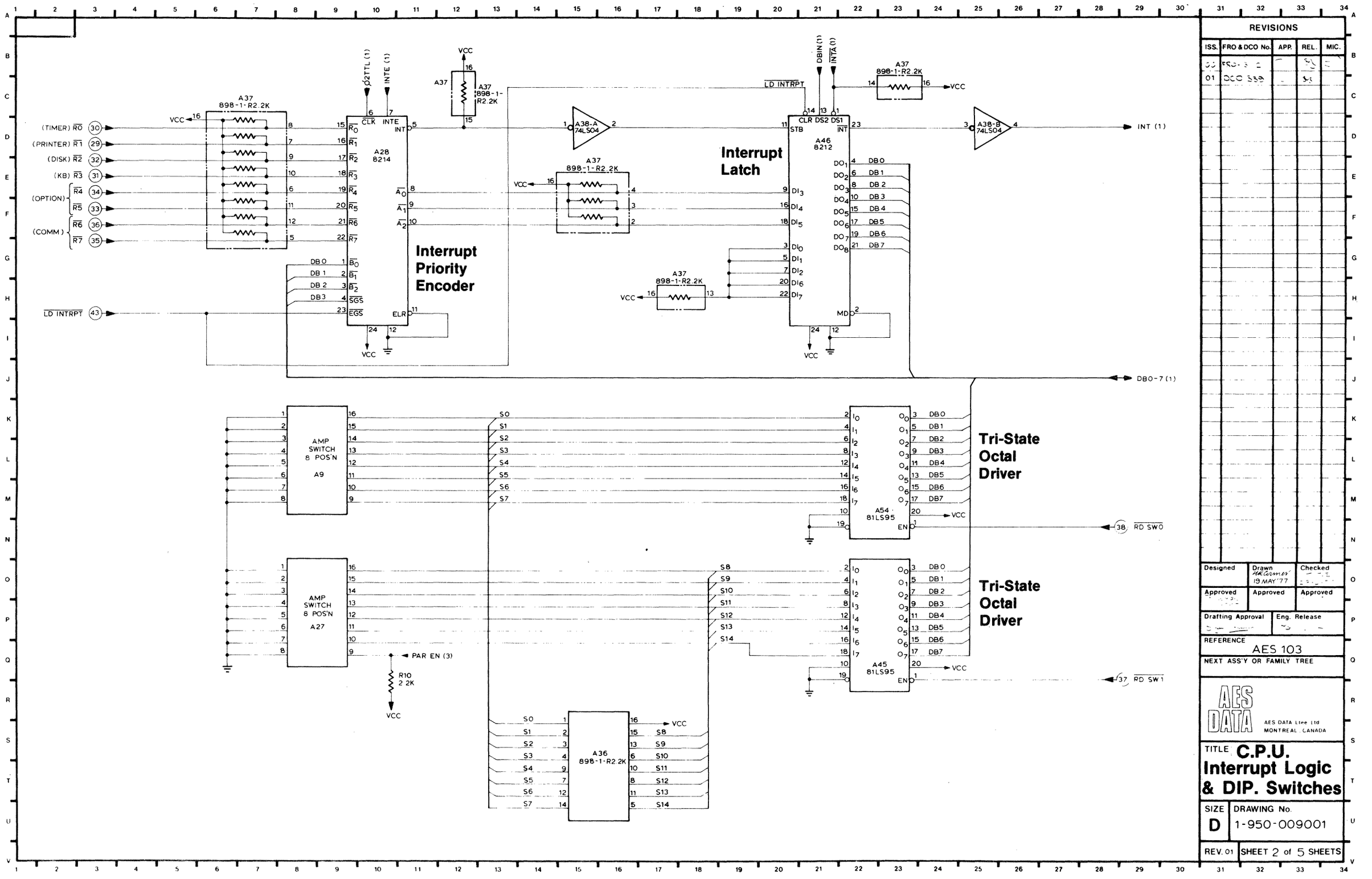
TITLE **C.P.U. Microprocessor & Peripheral Logic**

SIZE	DRAWING No.
D	1-950-009001

REV. 01 | SHEET 1 of 5 SHEETS

C.P.U. Schematic Diagrams

C.P.U. Schematic Diagrams



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.
00	FRO [illegible]			
01	DCO 339			

Designed	Drawn 19 MAY '77	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES 103

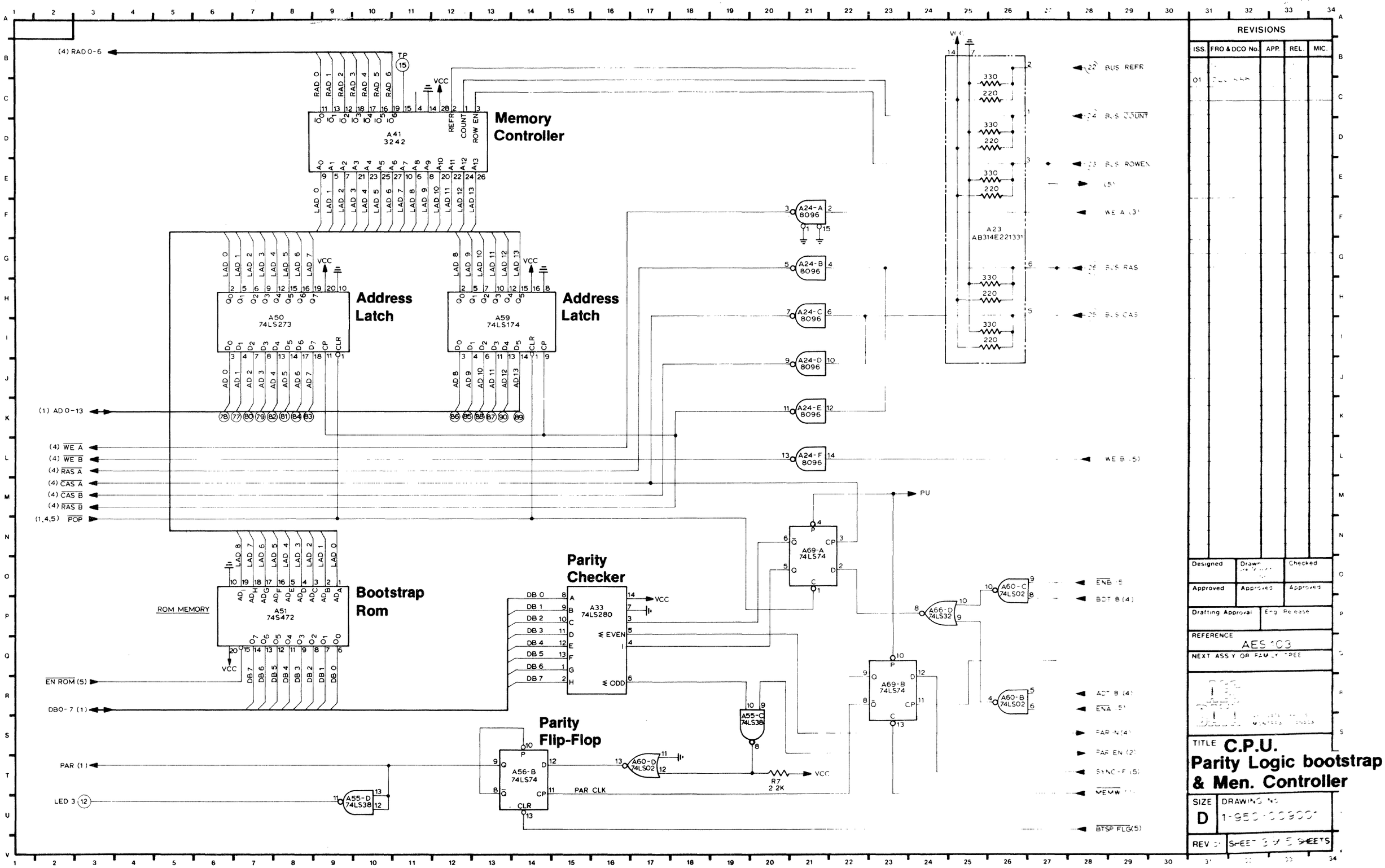
NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee Ltd MONTREAL, CANADA

TITLE **C.P.U. Interrupt Logic & DIP. Switches**

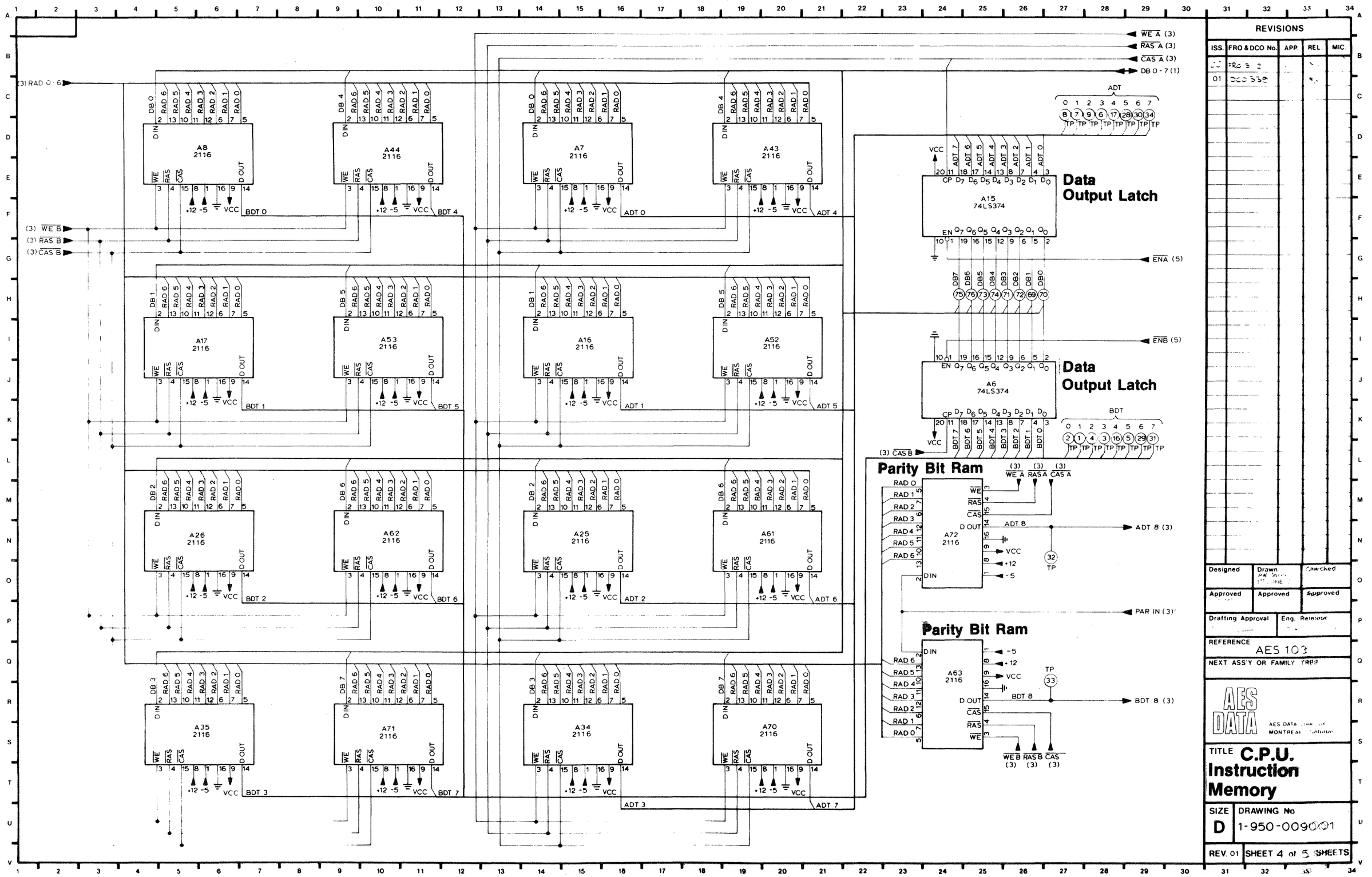
SIZE	DRAWING No.
D	1-950-009001

REV. 01 | SHEET 2 of 5 SHEETS



C.P.U. Schematic Diagrams

C.P.U.
Schematic
Diagrams



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.
00	FRO 3 2			
01	DCO 339			

Designed	Drawn	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES 103

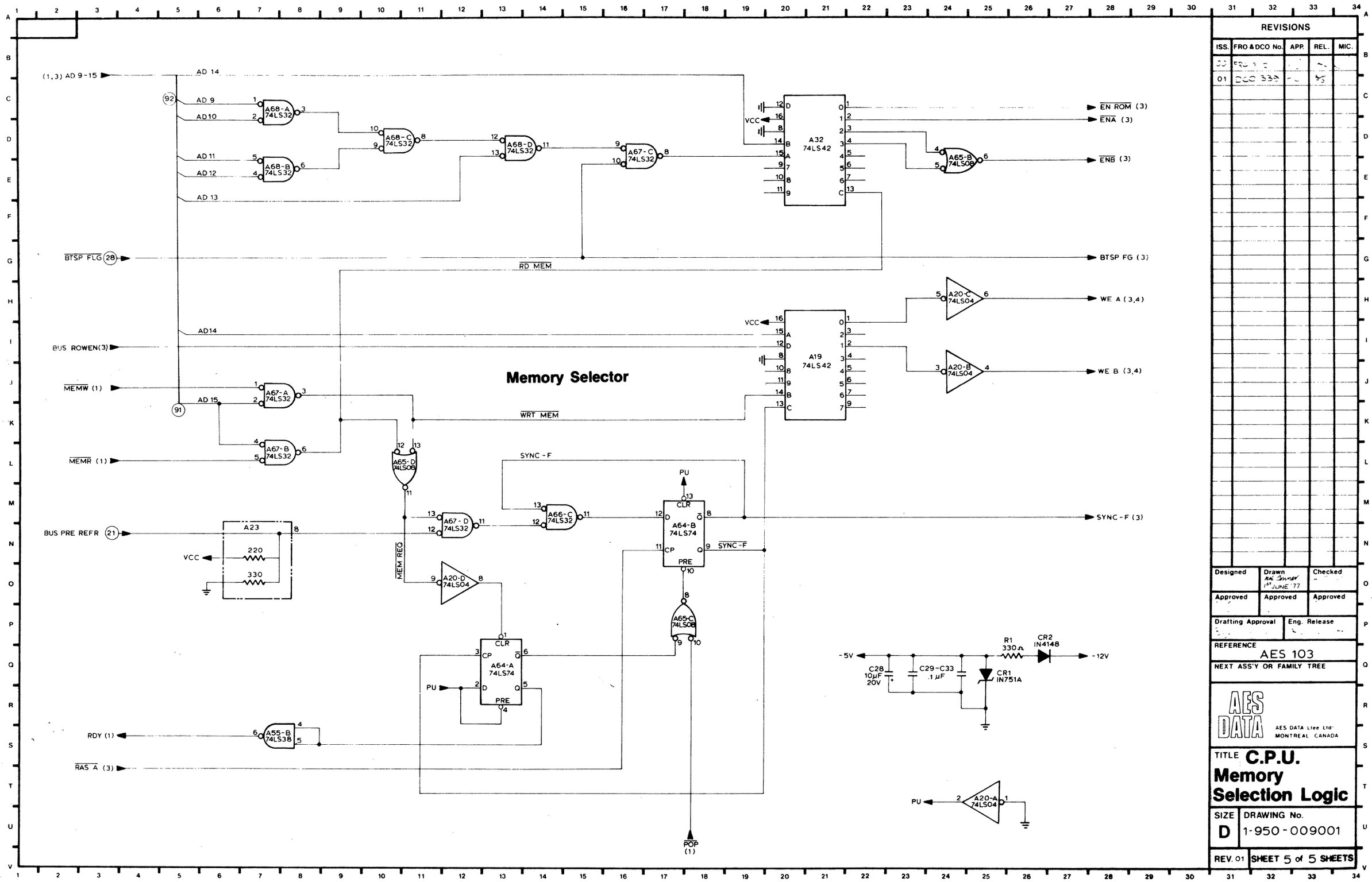
NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA (1988) INC. MONTREAL, CANADA

TITLE **C.P.U. Instruction Memory**

SIZE	DRAWING No
D	1-950-009001

REV. 01 | SHEET 4 of 5 SHEETS



REVISIONS

ISS.	FRO & DCO No.	APP.	REL.	MIC.
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01	DCO 339	[illegible]	[illegible]	

Designed	Drawn	Checked
	R.K. Bonner 1st JUNE '77	
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE AES 103

NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee Ltd: MONTREAL CANADA

TITLE **C.P.U. Memory Selection Logic**

SIZE	DRAWING No.
D	1-950-009001

REV. 01 | SHEET 5 of 5 SHEETS

C.P.U.
Schematic
Diagrams

C.P.U.
Parts List

	01		
	1	P.C.B. Drilling	C6-955-009001
	2	PCB Extractor	252-0102
A7,8,16,17,25 26,34,35,43,44 52,53,61-63,70-72	18	Dynamic Ram	A6-937-004801
A60	1	SN74LS02N	660-0209
A11,20,38	3	SN74LS04N	660-0210
A65	1	SN74LS08N	660-0211
A40,66,67,68	4	SN74LS32N	660-0215
A55	1	SN74LS38N	660-0216
A19,32	2	SN74LS42N	660-0217
A56,64,69	3	SN74LS74AN	660-0219
A2	1	SN74LS125N	660-0223
A59	1	SN74LS174N	660-0228
A50	1	SN74LS273N	660-0233
A33	1	SN74LS280N	660-0235
A24	1	SN74366AN	660-0239
A6,15,39	3	SN74LS374N	660-0240
A45,49,54,58	4	DM 81LS95N	660-0241
A21	1	8080-A	660-0243
A46	1	8212	660-0244
A28	1	8214	660-0245
A48,A57	2	8216	660-0246
A5	1	8224	660-0247
A30	1	8228	660-0248
A3	1	8257	660-0249
A41	1	3242	660-0250
A51	1	Boot, Prom	6-908-002001

	01		
A23	1	Res. Pack 314E221331	485-0110
A10,36,37	3	Res. Pack 898-1-R2.2K	485-0111
A9, 27	2	Switch Pack 8 Pos'n	533-0110
CR2	1	Diode IN4148	601-0104
CR1	1	Diode IN751A	602-0104
C28,34,51	3	Capacitor, 10uF, 20V. Tag.	164-0177
C1,2,20	3	Capacitor, 33uF, 16V. Tag.	164-0220
C3-5, 7,9,11-16 18, 21-26, 52,35	20	Capacitor, .05uF	165-0251
C6, 8, 10, 17, 19 27,29-33,36-50	26	Capacitor, .1uF	165-0347
R2	1	Resistor 100 OHMS 1/4W, 5%	402-0101
R5,6	2	" 1K OHM 1/4W, 5%	402-0102
R3,4	2	" 10K OHMS, 1/4W, 5%	402-0103
R7,10	2	" 2.2K OHMS 1/4W, 5%	402-0222
R8	1	" 240 OHMS, 1/4W, 5%	402-0241
R1,R9	2	" 330 OHMS, 1/4W, 5%	402-0331
Y1	1	Crystal 18.000 MHz	490-0120
	1	Test Header, 34 Pins	290-0123
A5,7,8,16,17 25,26,34,35,43 44,52,53,61,62 63,70,71,72	19	I.C. Socket, DIL,16 Pin.	698-0103
A3,21	2	I.C. Socket, DIL,40 Pin.	698-0118
A51	1	I.C. Socket, DIL,20 Pin.	698-0128

POWER SUPPLY (1-950-009301-00)

PURPOSE

The power supply provides all necessary voltages and currents to power the logic circuits and the printer constituting the AES-PLUS Text Editor. All the voltage supply modules are switching regulators and operate synchronously.

THEORY OF OPERATION

The power supply generates several positive and negative voltages:

- +15 volts at 13 amperes
- + 5 volts at 15 amperes
- -15 volts at 13 amperes peak
- +12 volts at 7 amperes
- -12 volts at 1 amperes

As shown in the block diagram, all the voltage supplies are fed from the +27 and -27 volt unregulated sources and synchronized by an external pulse generator.

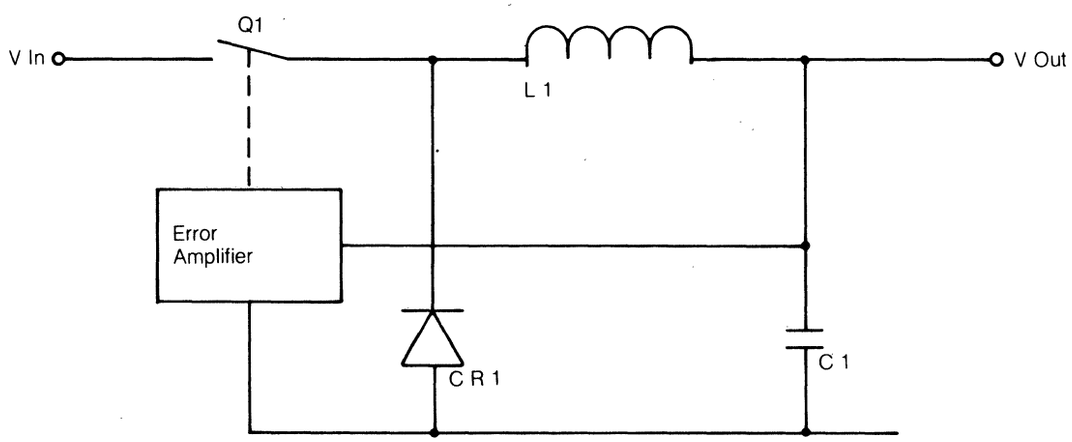
A) Line Input Transformer, Full-Wave Bridge and Filtering: The line input transformer can either operate from a 115 volt or 230 volt AC outlets. The input AC voltage is filtered through a universal line filter and applied to the primary of the transformer via a DPST switch. The power line is also distributed to cooling fan motors and to the monitor.

The secondary of the transformer is connected to a 27 ampere fullwave bridge and has its center tap connected to ground. A 10,000 microfarad capacitor filters the +27 volts and a 4,700 microfarad capacitor filters the -27 volt output.

B) The +5 Volt 15 Ampere Supply: This supply is a switching regulator and is synchronized by a 555 timer circuit. The basic switching regulator is comprised of voltage regulator (723), acting as an error amplifier, series-pass element Q1 (PIC645), coil L1 and capacitor C1 (refer to FIG 1).

The switching cycle, when not synchronized externally, begins when Q1 starts conducting and causes a nearly linear current to build up through L1. This current, less the load current, charges capacitor C1 until a maximum voltage threshold is reached at the detector (723) which immediately turns Q1 off. At this point, diode CR1 forward conducts and eventually discharges C1 through L1 to the lower threshold limit at which time Q1 is allowed to conduct again.

Figure 1 Switching Regulator Block Diagram



1. Voltage Regulation: In switching regulators, the output voltage is a function of the duty cycle of the switching waveform; voltage regulation can thus be achieved if the duty cycle is made variable. In the present regulator, the steady-state duty cycle is in the order of 20%. However, different load conditions will create voltage fluctuations which are sensed by the error amplifier (723) and immediately compensated by increasing the pulse duration at the base of Q1.

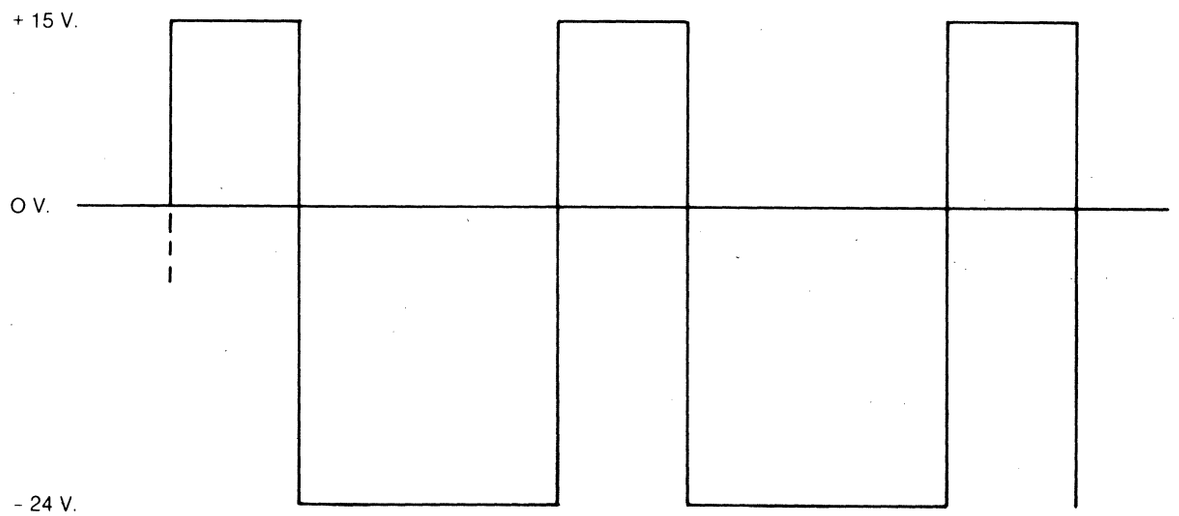
2. Current Regulation: Resistor R22 is the current sensing resistor. This resistor is connected in series with the positive terminal and also across a differential amplifier formed by transistor Q2 and the current limiting transistor in the 723 error amplifier. The two emitters of the differential pair are connected to a -8.2 volt source via a 4.7K resistor. If the output of the 5 volt supply ever becomes short-circuited, 15 amperes would flow-through R19, creating .15 volt across the differential amplifier input. This voltage would cause the transistor of the 723 to conduct and linearly reduce the duty cycle of the waveform to a point where only 3 amperes are allowed to flow through the short circuit.

3. Overvoltage Protection: The 5 volt supply is protected against overvoltage by thyristor Q3 and voltage sensing circuit R24, R25, C9 and CR5. Diode CR5 has a zener voltage of 5.6 and when this is reached, the diode starts conducting and current flows through R24 and R25. When the voltage at the junction of the two resistors equals .25, the thyristor fires and all the voltage across the output flows through it. The effect felt by the regulator is the same as a short circuit across the terminals and it would then behave accordingly. Diode CR6 protects the output against possible polarity reversals.

C) The +15 Volt 13 Ampere Supply: This switching regulator operates similarly to the 5 volt unit, having the same configuration. However, a diode and resistor network appears at the compensation input of the 723; this network, comprising CR17, Zener diode CR18 and resistor R65, maintains the base of the first transistor of the driving pair at approximately 3 volts above the output voltage to prevent Q7 from being overdriven.

D) The -15 volt 13 Ampere Supply: This negative voltage supply is fed by the -27 volt unregulated source. A 723 voltage regulator I.C. is also used as an error amplifier and operates in unison with Q2, L2 and C9 to form a switching regulator.

The Vc output of the 723 generates a square wave and is applied to the base of Q1 via a voltage divider formed by R1 and R2. The resulting output waveform at the base of Q2 is another square wave with a 39 volt swing, combining both the +15 and -27 volt components.



The -15 volt Sense line is brought to resistors R102, R100, R99 and R98, forming a voltage dividing string between the -15 volt output and a +15 volt reference source. The non-inverting input of the error amplifier is set to 0 volts at potentiometer R100 while the inverting input accepts a 2.7 volt zener reference. Resistor R95 provides hysteresis.

1. Current Regulation: The current regulator of the -15 volt supply uses a "current mirror" configuration. It comprises transistors Q12 and Q13, current sensing resistor R110 and other associated resistors and diodes. The operation of this current limiter is based on the relationship between the current flowing through R110 and R106. The current will limit when the voltage drop across both resistors becomes equal. When Q12 conducts, it pulls down the 723 positive input thus reducing the output voltage of the supply.

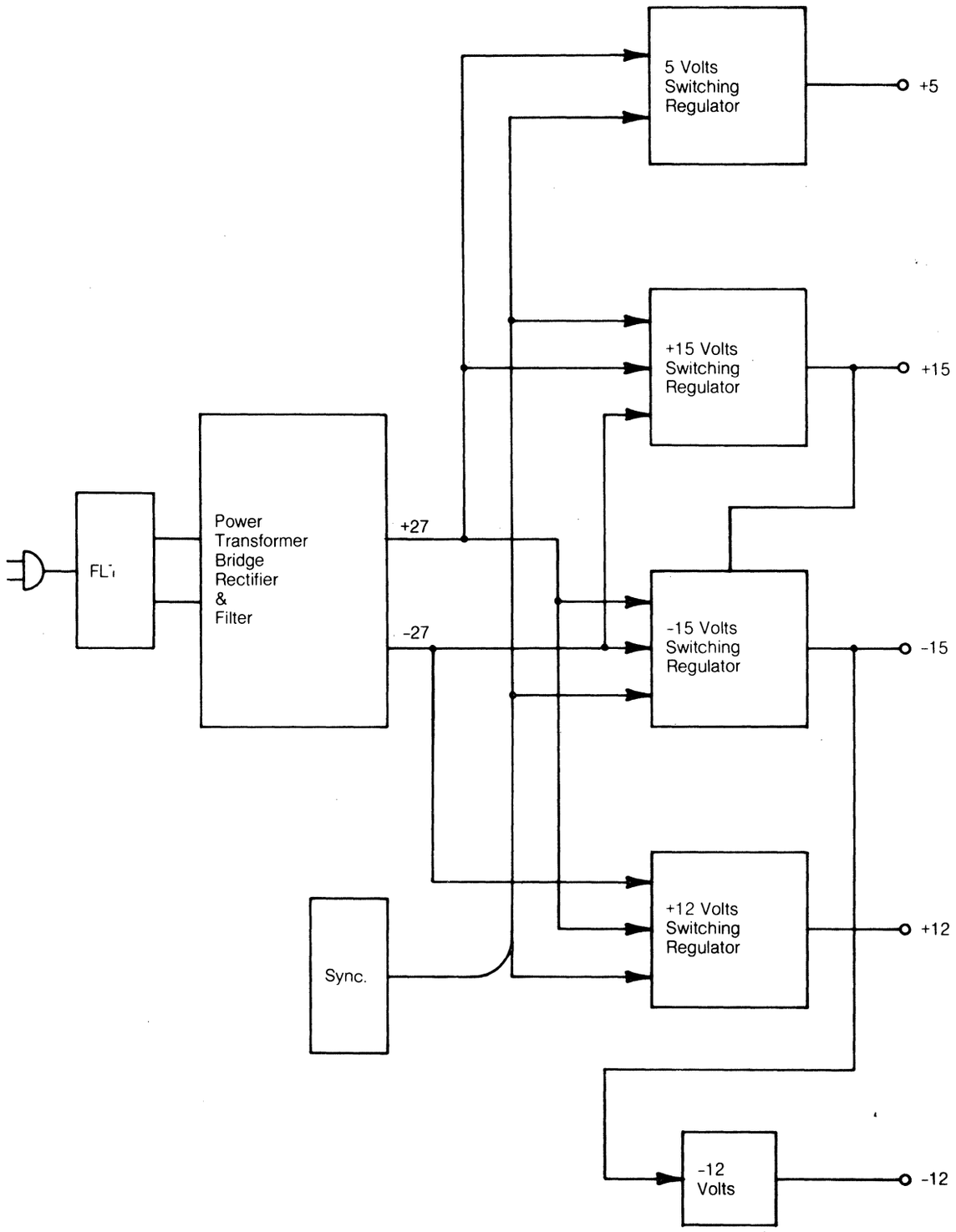
2. Overvoltage protection: The -15 volt supply is protected against overvoltage by thyristor Q14 and the voltage sensing circuit consisting of zener diode CR31, R10, R113 and C44. Diode CR32 protects the output from possible polarity reversals.

E) The +12 Volt 7 Ampere Supply: This supply is almost the exact replica of the + 15 volt unit except for R48 which adjusts the supply's output voltage.

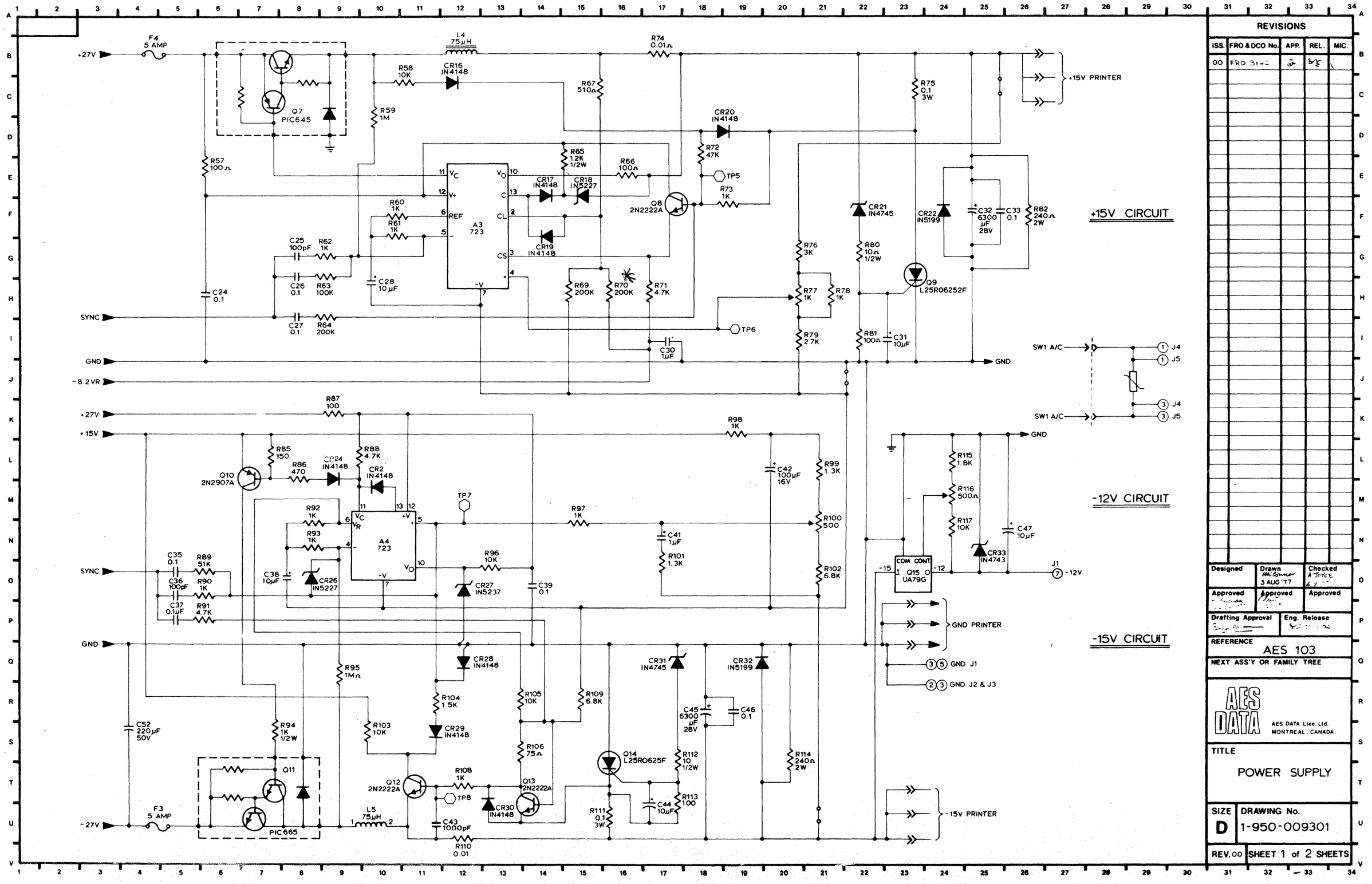
F) The -12 Volt Series Regulator: This supply is rated at 1.5 ampere and is an integrated three-terminal device.

G) External Synchronizing Oscillator: This oscillator comprises a 555 timer I.C., two transistors and associated resistors and capacitors. The frequency of operation is established by resistor R21 and capacitor C51. Transistor Q16 establishes a current source with R122 for the threshold detectors of the 555. Transistor Q17 outputs the oscillator signal by an emitter-follower configuration.

AES plus Power Supply Block Diagram



Power supply
Shematic
Diagrams



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.
00	FRO 31[illegible]			

Designed	Drawn McConnell 3 AUG '77	Checked A Joyce
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE: AES 103

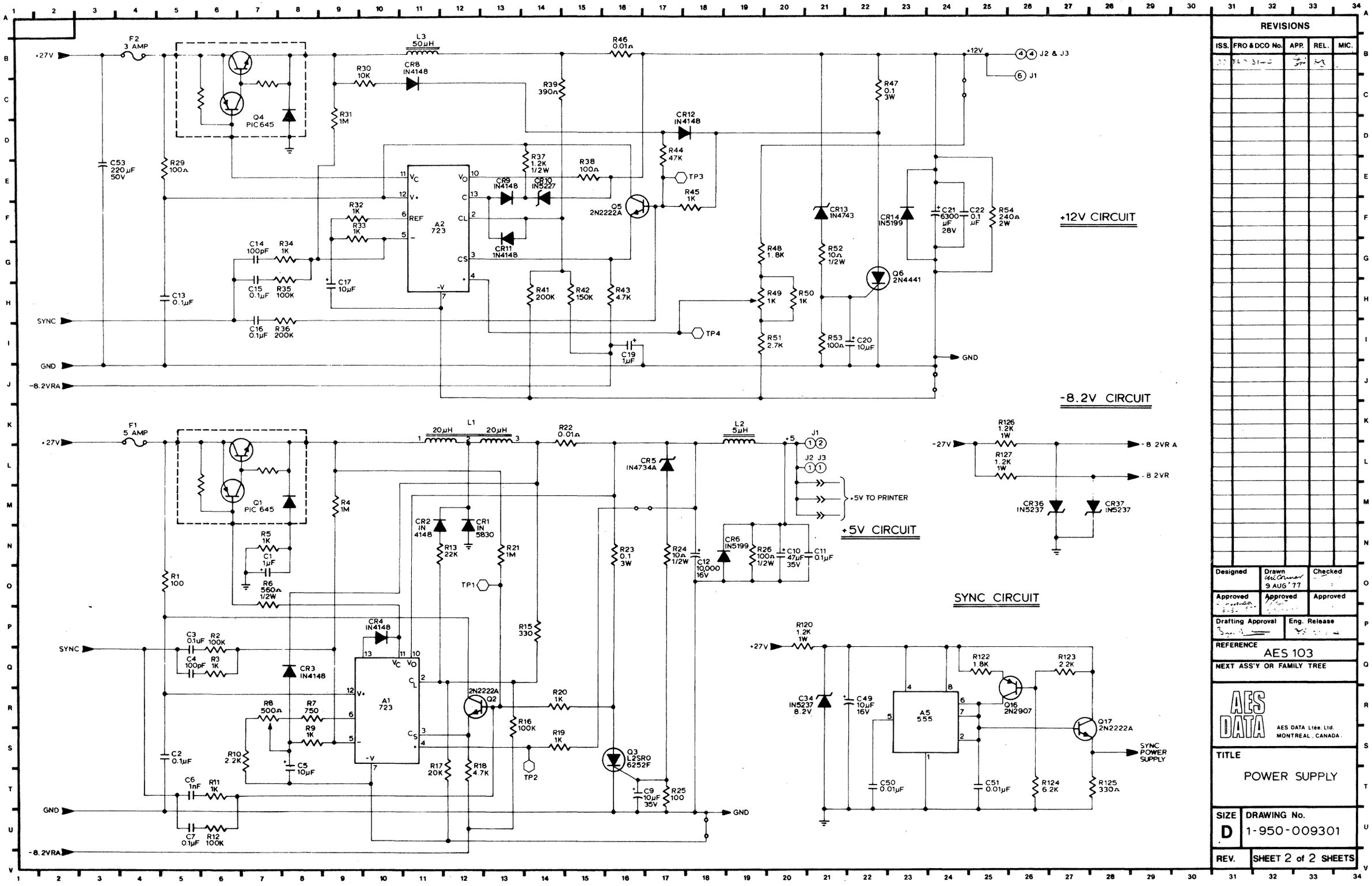
NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltee. Ltd. MONTREAL, CANADA.

TITLE: POWER SUPPLY

SIZE	DRAWING No.
D	1-950-009301

REV. 00 | SHEET 1 of 2 SHEETS



REVISIONS				
ISS.	FRO & DCO No.	APP.	REL.	MIC.

Designed	Drawn 9 AUG '77	Checked
Approved	Approved	Approved
Drafting Approval	Eng. Release	

REFERENCE: AES 103

NEXT ASS'Y OR FAMILY TREE

AES DATA — AES DATA Ltée. Ltd. MONTREAL, CANADA.

TITLE: POWER SUPPLY

SIZE	DRAWING No.
D	1-950-009301
REV.	SHEET 2 of 2 SHEETS

Power Supply Schematic Diagrams

Power Supply
Parts List

	01				01		
	1	P.C.B. Drilling	D6-955-009301	C5,9,17,20,28 31,38,44,47,49	10	Capacitor 10uF, 16V.	164-0177
				C1	1	Capacitor 1uF, 35V.	164-0207
A1,2,3,4	4	IC uA 723DC- Precision Volt Reg	650-0108	C10	1	Capacitor 47uF, 35V.	164-0229
A5	1	IC LM 555CN- I.C. Timer	660-0182	C42	1	Capacitor 100uF, 16V.	164-0257
Q2,5,8,12,13,17	6	Transistor 2N2222A	620-0101	C50,51	2	Capacitor .01uF, 100V.	165-0261
Q10,16	2	Transistor 2N2907A	621-0118	C4,14,25,36	4	Capacitor 100pF, 200V.	165-0271
				C2,3,7,8,11,13 15,16,22,24,26,27 33,35,37,39,46	17	Capacitor 0.1uF, 50V.	165-0285
				C43	1	Capacitor 1000pF, 200V.	165-0336
				C6,18,19,29,30 40,41	7	Capacitor 1uF, 50V.	165-0345
CR6,14,22,32	4	Diode IN5199	600-0104	R1,25,29,38,53 57,66,81,87,113	10	Resistor 100 OHMS, 1/4W, 5%	402-0101
CR2,3,4,8,9,11 12,16,17,19,20 24,25,28-30,35	17	Diode IN4148	601-0100	R3,5,9,11,19,20 32,33,34,45,50 60,61,62,73,78 90,92,93,97,98	22	Resistor 1K OHM, 1/4W, 5%	402-0102
CR5,21	2	Diode Zener IN4734A, 5.6V	602-0119	108			
CR31	1	Diode Zener IN4745, 16 V	602-0121	R30,58,96,103 105,117	6	Resistor 10K OHMS, 1/4W, 5%	402-0103
CR13,33	2	Diode Zener IN4743, 13 V	602-0122	R2,12,16,35,63	5	Resistor 100K OHMS, 1/4W, 5%	402-0104
CR34,36,37,27	4	Diode Zener IN5237, 8.2V	602-0129	R4,21,31,59,95	5	Resistor 1M OHMS, 1/4W, 5%	402-0105
CR10,18,26	3	Diode Zener IN5227, 3.6V	602-0130	R99,101	2	Resistor 1.3K OHMS, 1/4W, 5%	402-0132
				R85	1	Resistor 150 OHMS, 1/4W, 5%	402-0151
				R104	1	Resistor 1.5K OHMS, 1/4W, 5%	402-0152
				R42	1	Resistor 150K OHMS, 1/4W, 5%	402-0154
				R48,115,122	3	Resistor 1.8K OHMS, 1/4W, 5%	402-0182
				R17	1	Resistor 20K OHMS, 1/4W, 5%	402-0203

	01		
R36,41,64,69,70	5	Resistor 200K OHMS, 1/4W, 5%	402-0204
R10,123	2	Resistor 2.2K OHMS, 1/4W, 5%	402-0222
R13	1	Resistor 22K OHMS, 1/4W, 5%	402-0223
R51,79	2	Resistor 2.7K OHMS' 1/4W, 5%	402-0272
R76	1	Resistor 3 K OHMS, 1/4W, 5%	402-0302
R15,125	2	Resistor 330 OHMS, 1/4W, 5%	402-0331
R39	1	Resistor 390 OHMS, 1/4W, 5%	402-0391
R86	1	Resistor 470 OHMS, 1/4W, 5%	402-0471
R18,43,71,88,91	5	Resistor 4.7K OHMS, 1/4W, 5%	402-0472
R44,72	2	Resistor 47K OHMS, 1/4W, 5%	402-0473
R67	1	Resistor 510 OHMS, 1/4W, 5%	402-0511
R89	1	Resistor 51K OHMS, 1/4W, 5%	402-0513
R124	1	Resistor 6.2K OHMS, 1/4W, 5%	402-0622
R102,109	2	Resistor 6.8K OHMS 1/4W, 5%	402-0682
R7	1	Resistor 750 OHMS, 1/4W, 5%	402-0751
R106	1	Resistor 75 OHMS, 1/4W, 5%	402-0750
R24,52,80,112	4	Resistor 10 OHMS, 1/2W, 5%	411-0100
R26	1	Resistor 100 OHMS, 1/2W, 5%	411-0101
R94	1	Resistor 1K OHM, 1/2W, 5%	411-0102
R6	1	Resistor 560 OHMS' 1/2W, 5%	411-0561
R37,65	2	Resistor 1.2K OHMS, 1/2W, 5%	411-0122
R120,126,127	3	Resistor 1.2K OHMS 1W	421-0122
R23,47,75,111	4	Resistor .1 OHM 3W	450-0125
R54,82,114	3	Resistor 240 OHMS 2W	450-0241

	01		
R8,100,116	3	Potentiometer 500 OHMS	357-0567
R49,77	2	Potentiometer 1K OHMS	357-0568
R22,46,74,110	4	Wire Resistance	A6-937-005701
	8	Fuse Holder Clip	247-0201
F2	1	Fuse 3 AMP	246-0127
F1,3,4	3	Fuse 5 AMP	246-0140
J1	1	Connector, Terminal Pin-7	295-0135
J2,3	2	Connector, Terminal Pin-4	295-0146
J4,5	2	Connector, Terminal Pin-3	295-0150
TP1-8	8	Test Point	543-0234
A1-4	4	Socket DIL 14 Pin	698-0102
A5	1	Socket DIL 8 Pin	698-0123

SECTION I

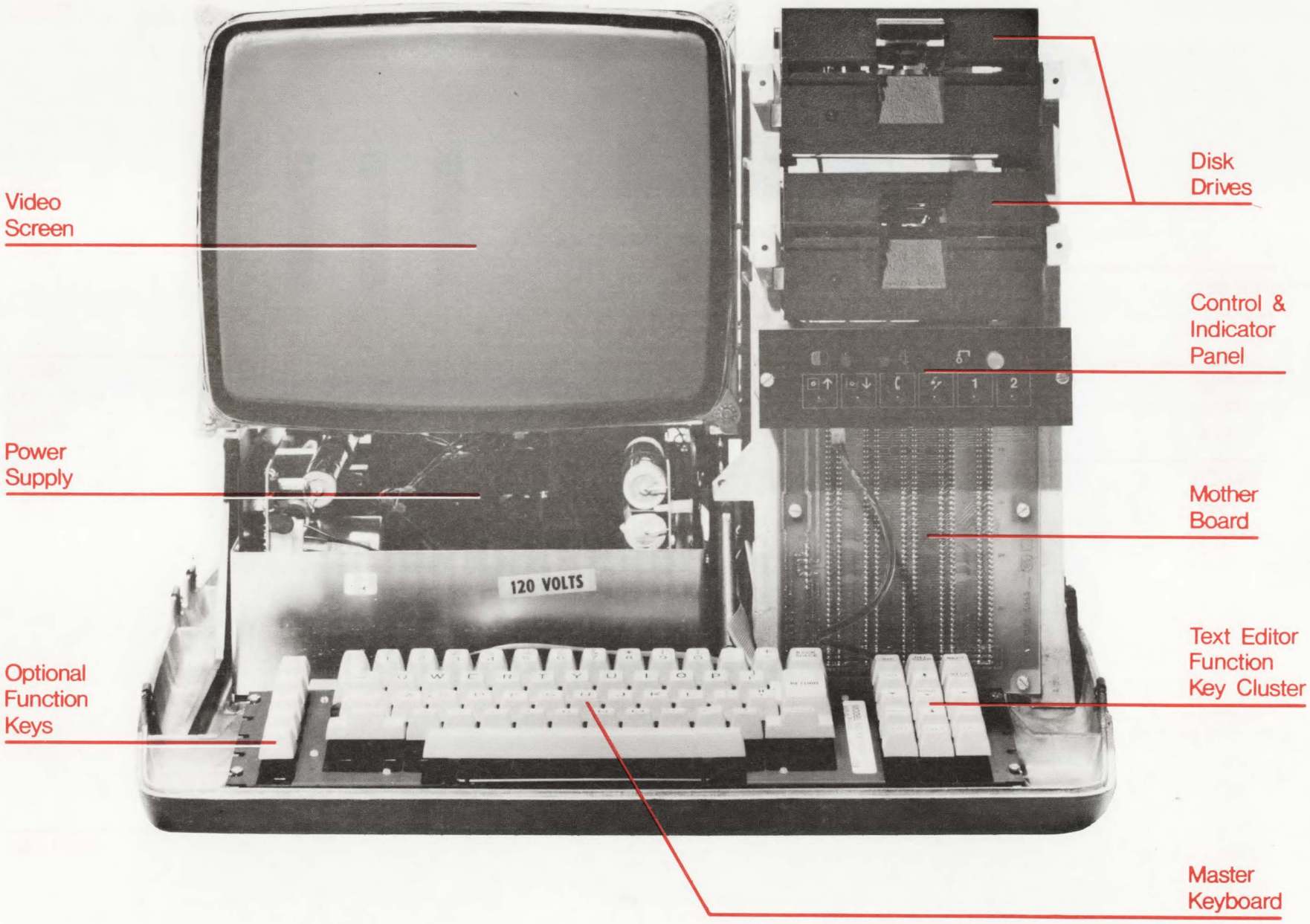
ASSEMBLY

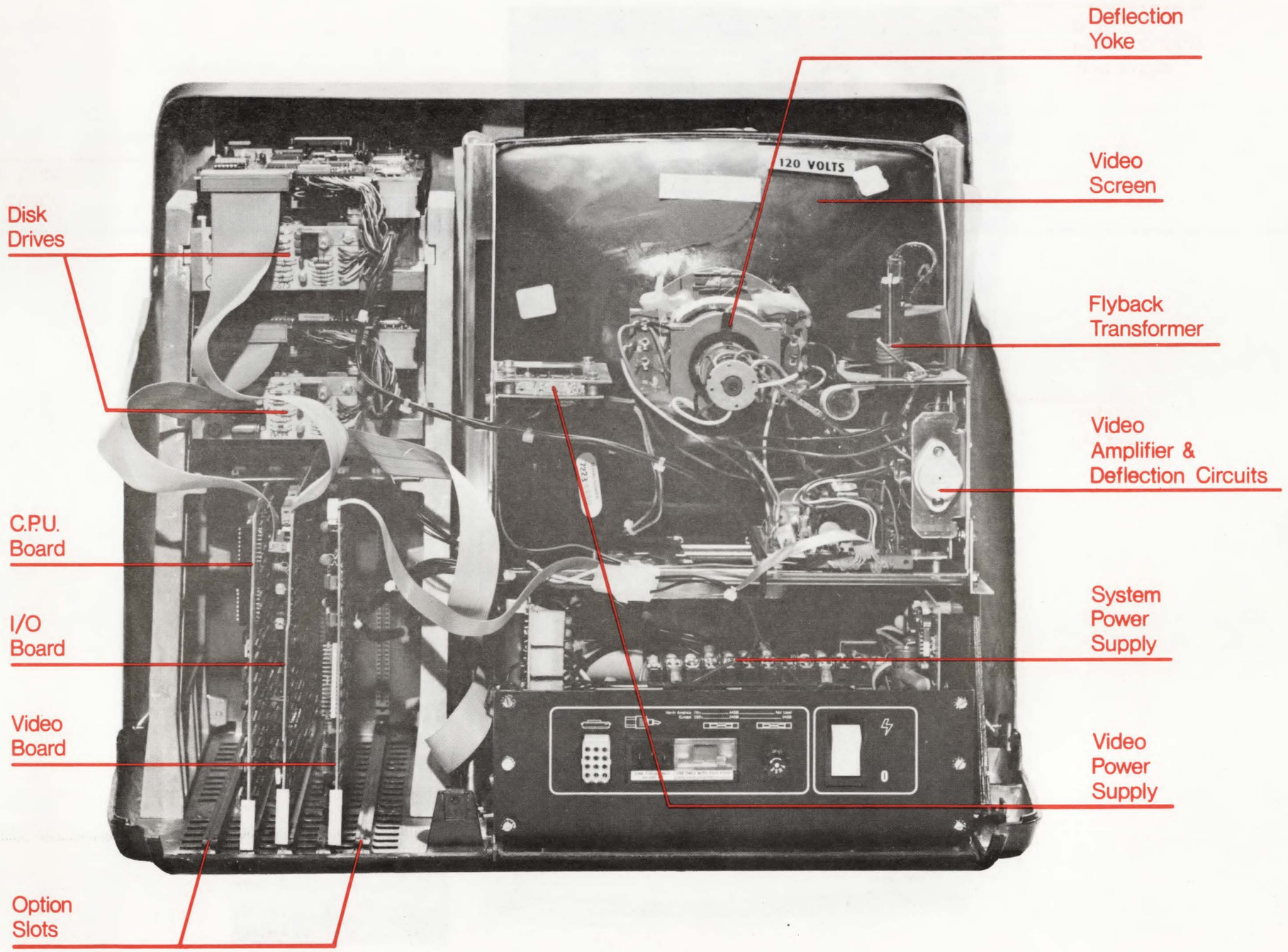
This Section describes, with the aid of photographs and legends, the mechanical configuration of the AES-PLUS Text Editor. Cabinet panels have been removed showing the whole assembly; the four main printed circuit boards are displayed giving full rendition of their topography.


Ventilation
Printer
I/O Cable
Outlet
Option
I/O Cable
Outlets
Printer
Power
Outlet
Main
Fuse
Holder
On - Off
Switch
0

Rear
View

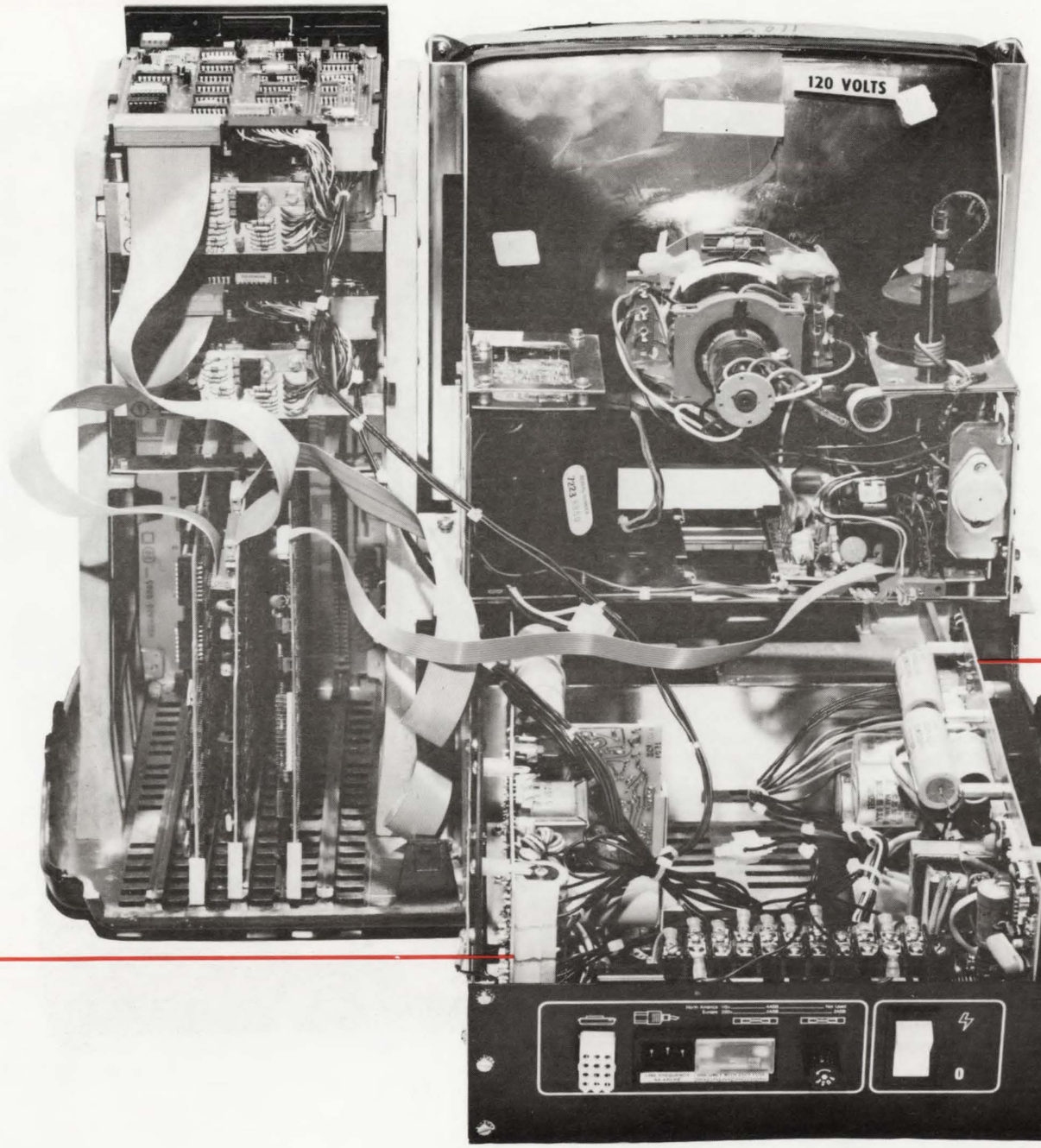
Front View
With Panel Removed

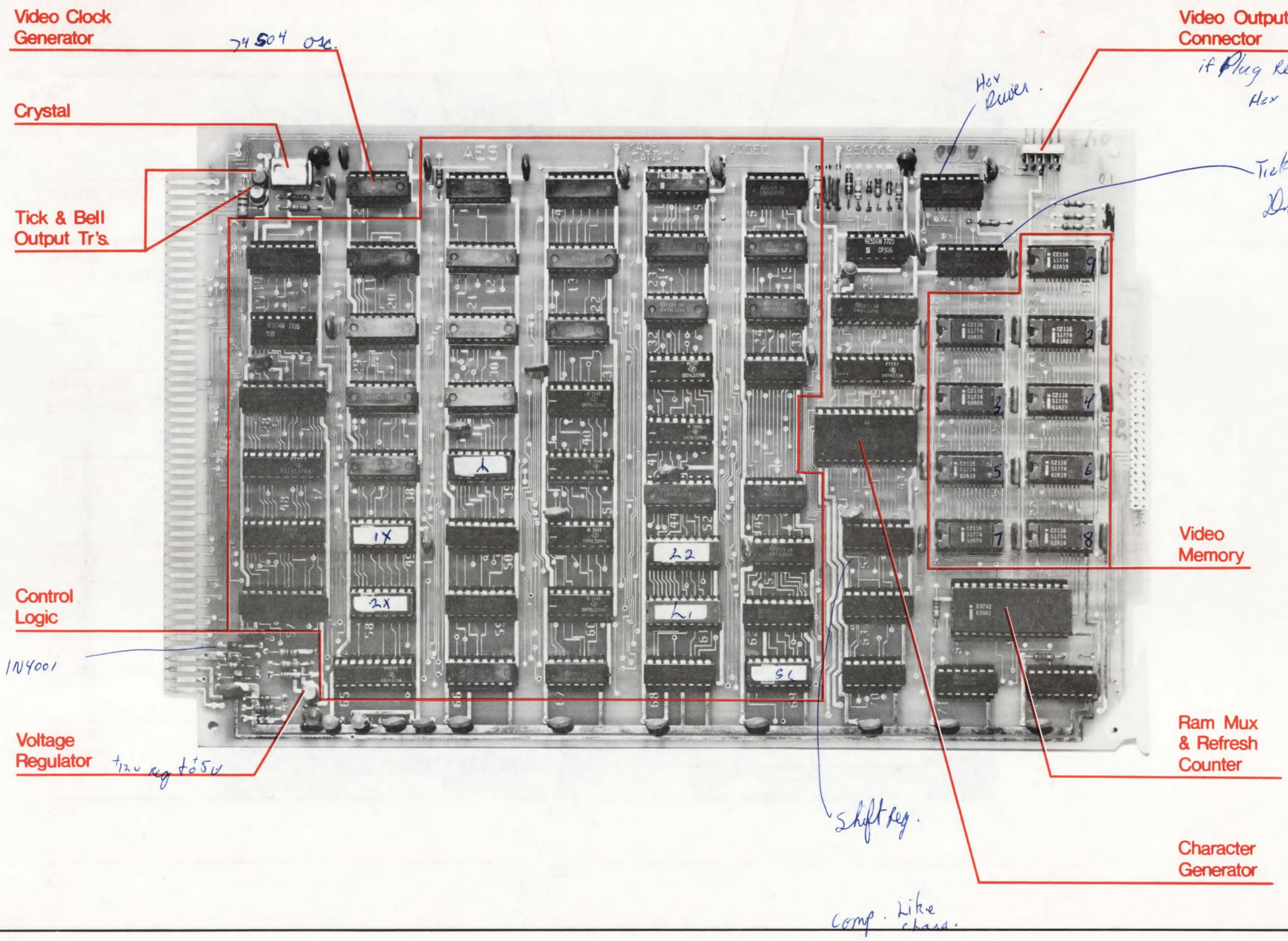




Rear View
With Panel Removed

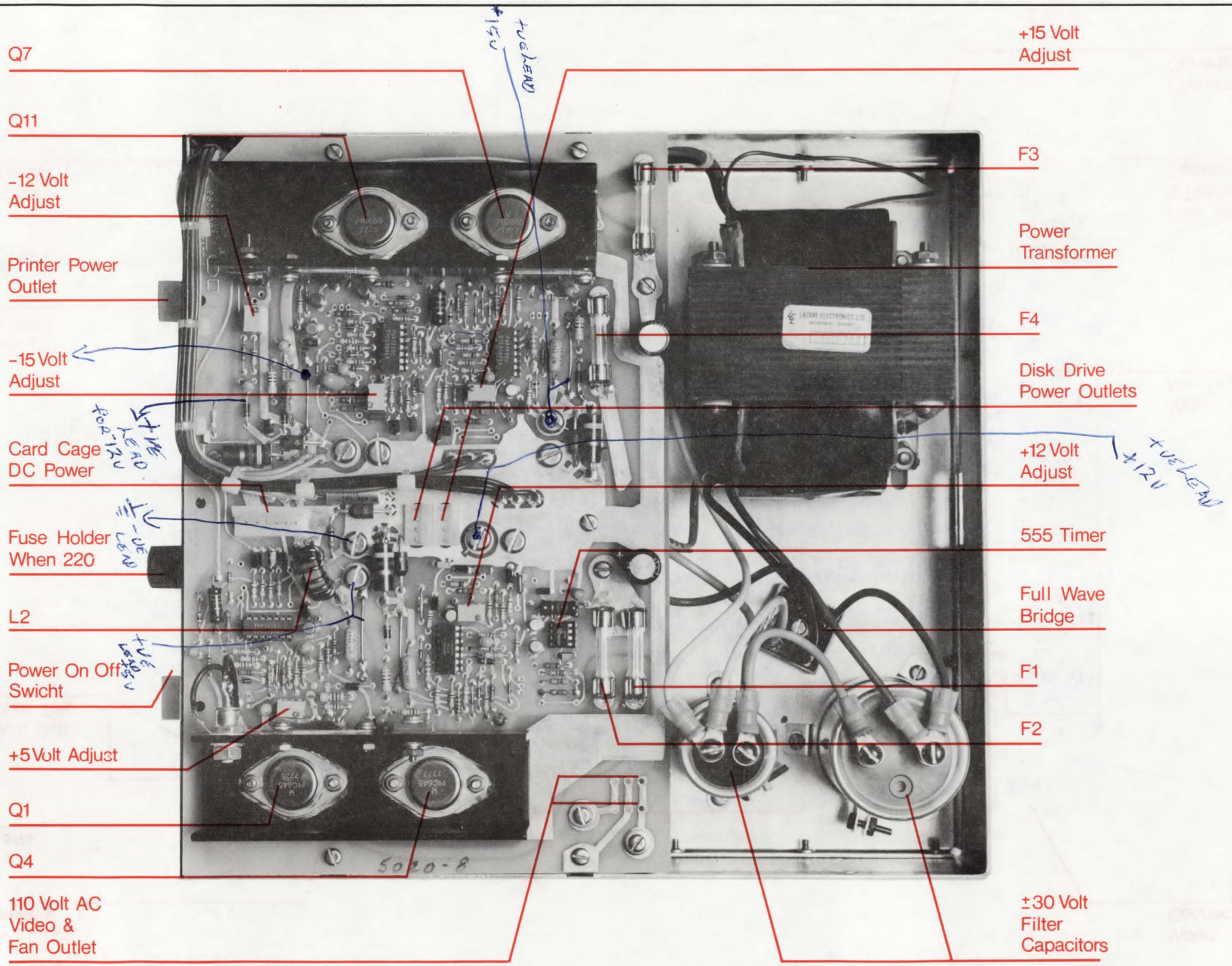
Rear View
With Power Supply
Pulled Out

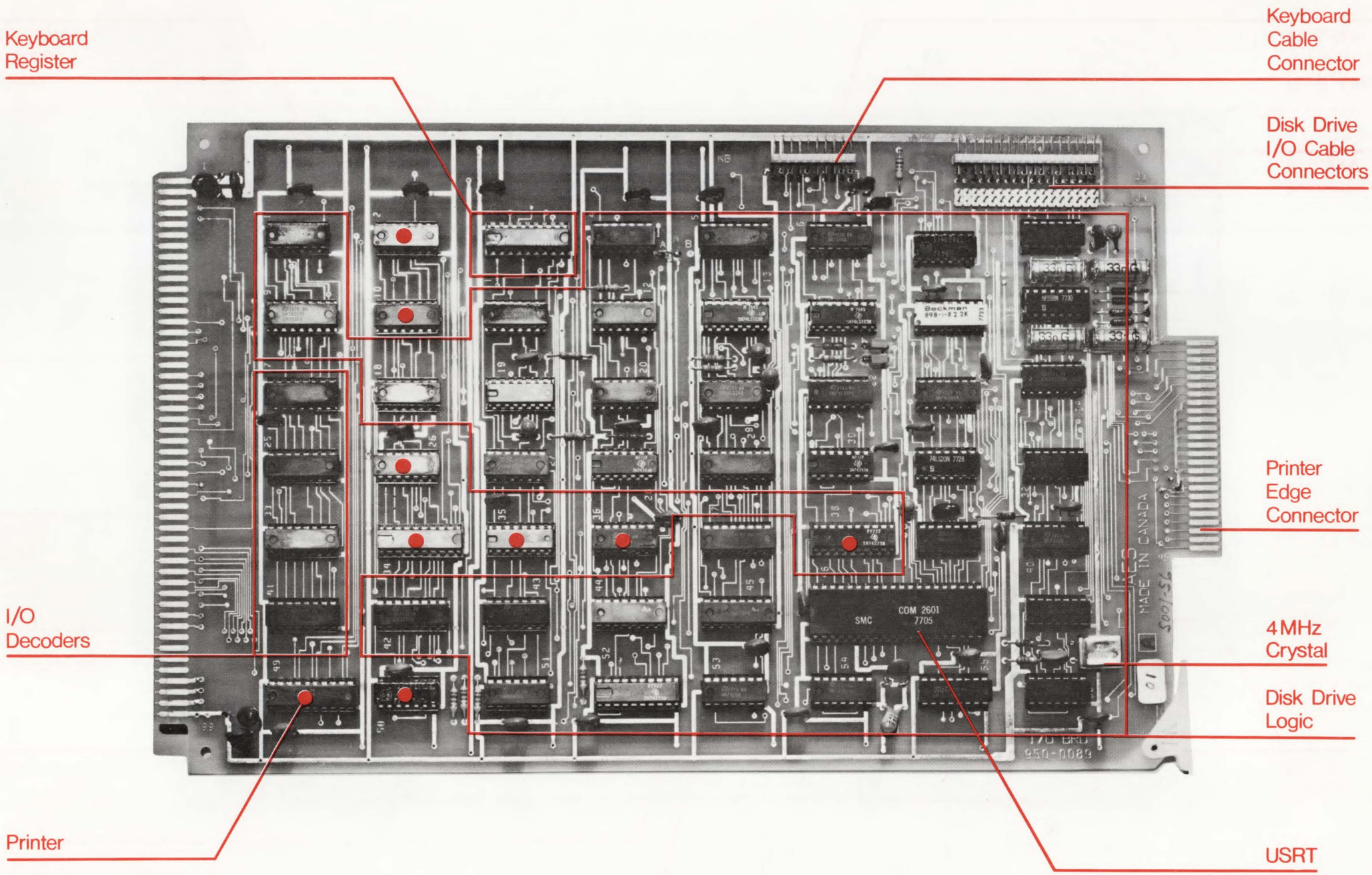



Video Clock Generator
74S04 OSC.
Crystal
Tick & Bell Output Tr's.
Video Output Connector
if Plug Reverse Hex Drive Blows.
Hex Driver.
Tick Bell Dual 555
Video Memory
Control Logic
IN4001
Voltage Regulator
±12V reg to ±5V
Ram Mux & Refresh Counter
Shift Reg.
Character Generator
Comp. like chars.

Video
Board

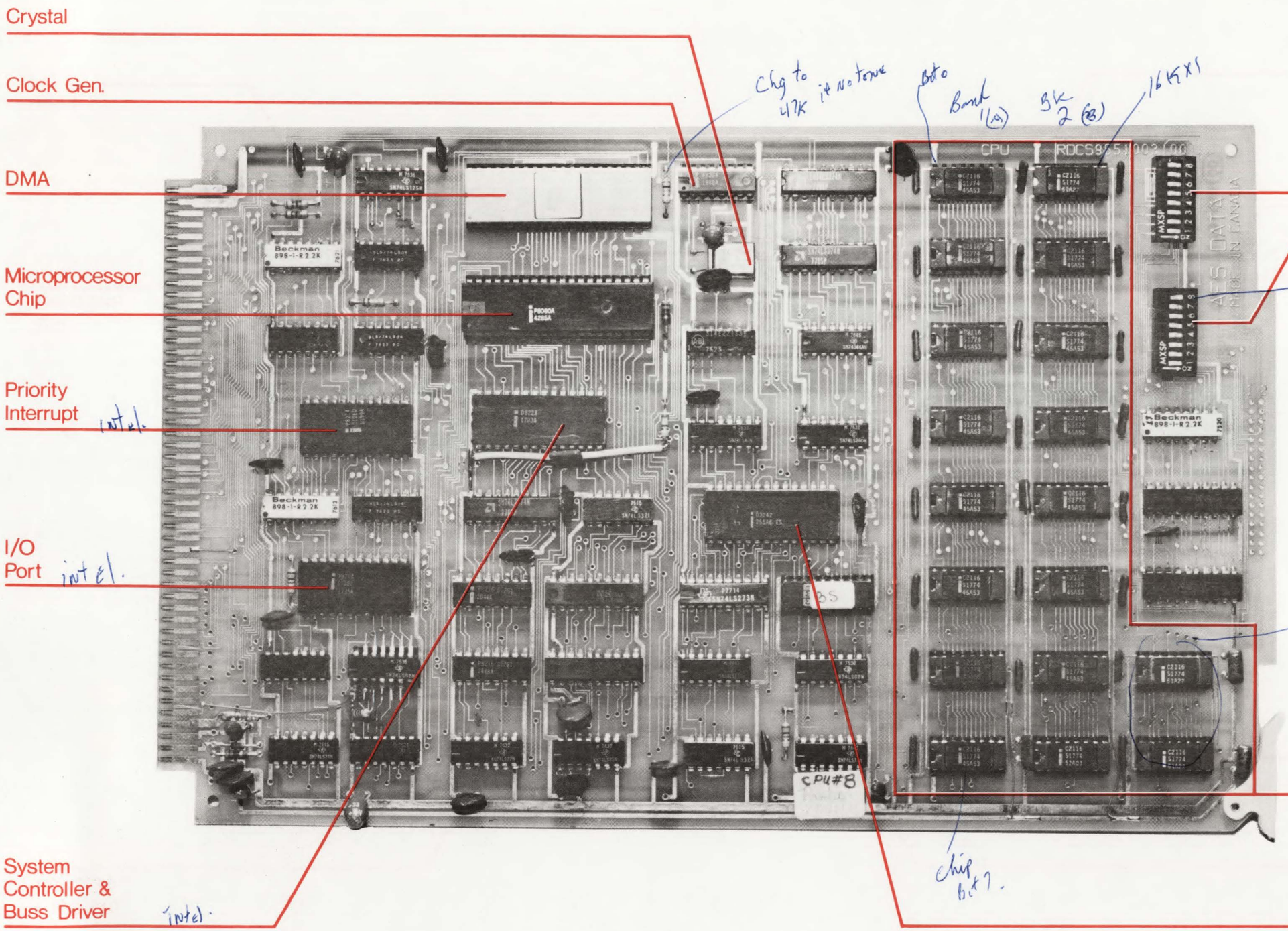
Power Supply Board




Keyboard Register
Keyboard Cable Connector
Disk Drive I/O Cable Connectors
Printer Edge Connector
I/O Decoders
4 MHz Crystal
Disk Drive Logic
Printer
USRT
KB
Beckman
SMC
COM 2601
7705
MADE IN CANADA
I/O BRD
950-0089

I/O
Board

C.P.U. Board


Crystal
Clock Gen.
DMA
Microprocessor Chip
Priority Interrupt
intel.
I/O Port
intel.
System Controller & Buss Driver
intel.
Switch Packs
8 - parity Bit.
Parity Bit. No longer there.
Instruction Memory
Ram Mux & Refresh Counter
Chip bit 7.
Chg to 47K if No tone
Bit 0
Bank 1 (A)
5K 2 (B)
16 K x 1
CPU
RDCS9
CPU #8
Beckman 898-1-R 2.2K
MXSP
AES DATA MADE IN CANADA

COMPONENTS

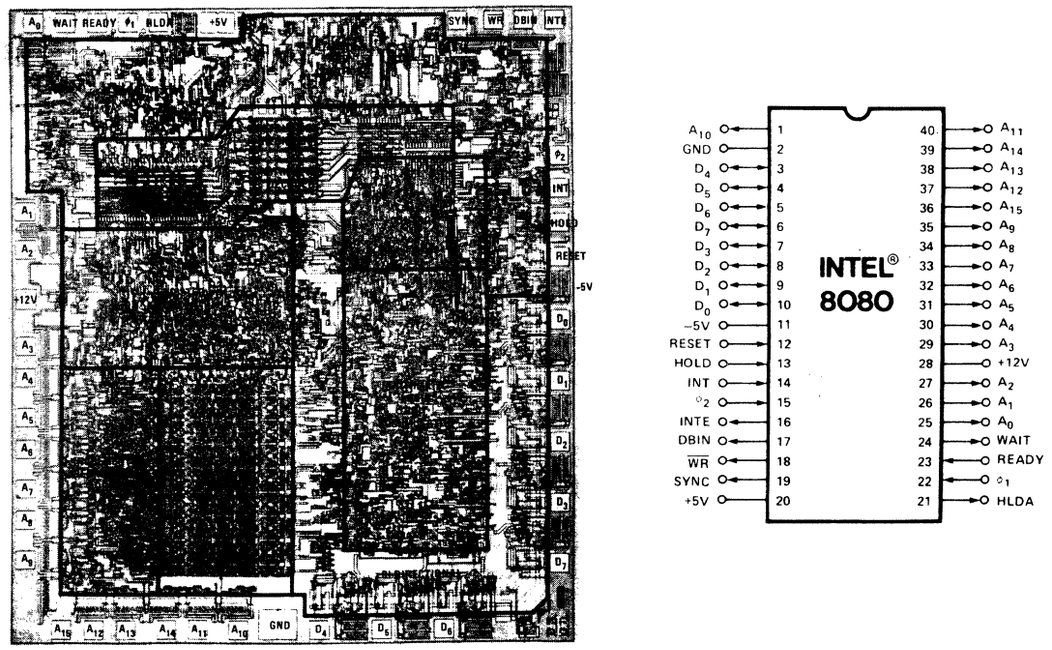
This Chapter contains data sheets of the following integrated circuits:

TTL	MOS
7442	INTEL 8080A
74125	MMI 6301
74157	6351
74160	INTEL 2116 RAM
74161	3242
74165	8212
74175	8214
74174	8216
74257	8224
74273	8228
74279	8257
74280	COM2601
74283	NE553
74298	
74365	
74366	
74374	
74393	
74472	
81LS95	
F9334	
DM8160	

THE 8080 MICROPROCESSOR

The 8080 is a complete 8-bit parallel, central processor unit (CPU) for use in general purpose digital computer systems. It is fabricated on a single LSI chip (see Figure 3-1). using Intel's n-channel silicon gate MOS process. The 8080 transfers data and internal state information via an 8-bit, bidirectional 3-state Data Bus (D_0-D_7). Memory and peripheral device addresses are transmitted over a separate 16-bit 3-state Address Bus (A_0-A_{15}). Six timing and control outputs (SYNC, DBIN, WAIT, $\overline{WR}$, HLDA and INTE) emanate from the 8080, while four control inputs (READY, HOLD, INT and RESET), four power inputs (+12v, +5v, -5v, and GND) and two clock inputs (ϕ_1 and ϕ_2) are accepted by the 8080.

Figure 2-1. 8080 Photomicrograph With Pin Designations



ARCHITECTURE OF THE 8080 CPU

The 8080 CPU consists of the following functional units:

- Register array and address logic
- Arithmetic and logic unit (ALU)
- Instruction register and control section
- Bi-directional, 3-state data bus buffer

Figure 2-2 illustrates the functional blocks within the 8080 CPU.

Registers:

The register section consists of a static RAM array organized into six 16-bit registers:

- Program counter (PC)
- Stack pointer (SP)
- Six 8-bit general purpose registers arranged in pairs, referred to as B,C; D,E; and H,L
- A temporary register pair called W,Z

The program counter maintains the memory address of the current program instruction and is incremented automatically during every instruction fetch. The stack pointer maintains the address of the next available stack location in memory. The stack pointer can be initialized to use any portion of read-write memory as a stack. The stack pointer is decremented when data is "pushed" onto the stack and incremented when data is "popped" off the stack (i.e., the stack grows "downward").

The six general purpose registers can be used either as single registers (8-bit) or as register pairs (16-bit). The temporary register pair, W,Z, is not program addressable and is only used for the internal execution of instructions.

Eight-bit data bytes can be transferred between the internal bus and the register array via the register-select multiplexer. Sixteen-bit transfers can proceed between the register array and the address latch or the incrementer/decrementer circuit. The address latch receives data from any of the three register pairs and drives the 16 address output buffers (A_0-A_{15}), as well as the incrementer/decrementer circuit. The incrementer/decrementer circuit receives data from the address latch and sends it to the register array. The 16-bit data can be incremented or decremented or simply transferred between registers.

Figure 2-2. 8080 CPU Functional Block Diagram

Arithmetic and Logic Unit (ALU):

The ALU contains the following registers:

- An 8-bit accumulator
- An 8-bit temporary accumulator (ACT)
- A 5-bit flag register: zero, carry, sign, parity and auxiliary carry
- An 8-bit temporary register (TMP)

Arithmetic, logical and rotate operations are performed in the ALU. The ALU is fed by the temporary register (TMP) and the temporary accumulator (ACT) and carry flip-flop. The result of the operation can be transferred to the internal bus or to the accumulator; the ALU also feeds the flag register.

The temporary register (TMP) receives information from the internal bus and can send all or portions of it to the ALU, the flag register and the internal bus.

The accumulator (ACC) can be loaded from the ALU and the internal bus and can transfer data to the temporary accumulator (ACT) and the internal bus. The contents of the accumulator (ACC) and the auxiliary carry flip-flop can be tested for decimal correction during the execution of the DAA instruction (see Chapter 4).

Instruction Register and Control:

During an instruction fetch, the first byte of an instruction (containing the OP code) is transferred from the internal bus to the 8-bit instruction register.

The contents of the instruction register are, in turn, available to the instruction decoder. The output of the decoder, combined with various timing signals, provides the control signals for the register array, ALU and data buffer blocks. In addition, the outputs from the instruction decoder and external control signals feed the timing and state control section which generates the state and cycle timing signals.

Data Bus Buffer:

This 8-bit bidirectional 3-state buffer is used to isolate the CPU's internal bus from the external data bus (D_0 through D_7). In the output mode, the internal bus content is loaded into an 8-bit latch that, in turn, drives the data bus output buffers. The output buffers are switched off during input or non-transfer operations.

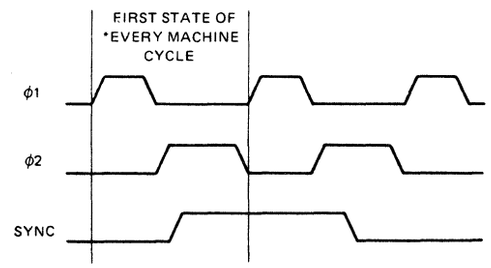
During the input mode, data from the external data bus is transferred to the internal bus. The internal bus is precharged at the beginning of each internal state, except for the transfer state (T_3—described later in this chapter).

THE PROCESSOR CYCLE

An **instruction cycle** is defined as the time required to fetch and execute an instruction. During the fetch, a selected instruction (one, two or three bytes) is extracted from memory and deposited in the CPU's instruction register. During the execution phase, the instruction is decoded and translated into specific processing activities.

Every instruction cycle consists of one, two, three, four or five machine cycles. A **machine cycle** is required each time the CPU accesses memory or an I/O port. The fetch portion of an instruction cycle requires one machine cycle for each byte to be fetched. The duration of the execution portion of the instruction cycle depends on the kind of instruction that has been fetched. Some instructions do not require any machine cycles other than those necessary to fetch the instruction; other instructions, however, require additional machine cycles to write or read data to/from memory or I/O devices. The DAD instruction is an exception in that it requires two additional machine cycles to complete an internal register-pair add (see Chapter 4).

Each machine cycle consists of three, four or five states. A state is the smallest unit of processing activity and is defined as the interval between two successive positive-going transitions of the ϕ_1 driven clock pulse. The 8080 is driven by a two-phase clock oscillator. All processing activities are referred to the period of this clock. The two non-overlapping clock pulses, labeled ϕ_1 and ϕ_2, are furnished by external circuitry. It is the ϕ_1 clock pulse which divides each machine cycle into states. Timing logic within the 8080 uses the clock inputs to produce a SYNC pulse, which identifies the beginning of every machine cycle. The SYNC pulse is triggered by the low-to-high transition of ϕ_2, as shown in Figure 2-3.



*SYNC DOES NOT OCCUR IN THE SECOND AND THIRD MACHINE CYCLES OF A DAD INSTRUCTION SINCE THESE MACHINE CYCLES ARE USED FOR AN INTERNAL REGISTER-PAIR ADD.

Figure 2-3. ϕ_1, ϕ_2 And SYNC Timing

There are three exceptions to the defined duration of a state. They are the WAIT state, the hold (HLDA) state and the halt (HLTA) state, described later in this chapter. Because the WAIT, the HLDA, and the HLTA states depend upon external events, they are by their nature of indeterminate length. Even these exceptional states, however, must be synchronized with the pulses of the driving clock. Thus, the duration of all states are integral multiples of the clock period.

To summarize then, each **clock period** marks a **state**; three to five states constitute a machine cycle; and one to five **machine cycles** comprise an **instruction cycle**. A full instruction cycle requires anywhere from four to eighteen states for its completion, depending on the kind of instruction involved.

Machine Cycle Identification:

With the exception of the DAD instruction, there is just one consideration that determines how many machine cycles are required in any given instruction cycle: the number of times that the processor must reference a memory address or an addressable peripheral device, in order to fetch and execute the instruction. Like many processors, the 8080 is so constructed that it can transmit only one address per machine cycle. Thus, if the fetch and execution of an instruction requires two memory references, then the instruction cycle associated with that instruction consists of two machine cycles. If five such references are called for, then the instruction cycle contains five machine cycles.

Every instruction cycle has at least one reference to memory, during which the instruction is fetched. An instruction cycle must always have a fetch, even if the execution of the instruction requires no further references to memory. The first machine cycle in every instruction cycle is therefore a FETCH. Beyond that, there are no fast rules. It depends on the kind of instruction that is fetched.

Consider some examples. The add-register (ADD r) instruction is an instruction that requires only a single machine cycle (FETCH) for its completion. In this one-byte instruction, the contents of one of the CPU's six general purpose registers is added to the existing contents of the accumulator. Since all the information necessary to execute the command is contained in the eight bits of the instruction code, only one memory reference is necessary. Three states are used to extract the instruction from memory, and one additional state is used to accomplish the desired addition. The entire instruction cycle thus requires only one machine cycle that consists of four states, or four periods of the external clock.

Suppose now, however, that we wish to add the contents of a specific memory location to the existing contents of the accumulator (ADD M). Although this is quite similar in principle to the example just cited, several additional steps will be used. An extra machine cycle will be used, in order to address the desired memory location.

The actual sequence is as follows. First the processor extracts from memory the one-byte instruction word addressed by its program counter. This takes three states. The eight-bit instruction word obtained during the FETCH machine cycle is deposited in the CPU's instruction register and used to direct activities during the remainder of the instruction cycle. Next, the processor sends out, as an address, the contents of its H and L registers. The eight-bit data word returned during this MEMORY READ machine cycle is placed in a temporary register inside the 8080 CPU. By now three more clock periods (states) have elapsed. In the seventh and final state, the contents of the temporary register are added to those of the accumulator. Two machine cycles, consisting of seven states in all, complete the "ADD M" instruction cycle.

At the opposite extreme is the save H and L registers (SHLD) instruction, which requires five machine cycles. During an "SHLD" instruction cycle, the contents of the processor's H and L registers are deposited in two sequentially adjacent memory locations; the destination is indicated by two address bytes which are stored in the two memory locations immediately following the operation code byte. The following sequence of events occurs:

(1) A FETCH machine cycle, consisting of four states. During the first three states of this machine cycle, the processor fetches the instruction indicated by its program counter. The program counter is then incremented. The fourth state is used for internal instruction decoding.

(2) A MEMORY READ machine cycle, consisting of three states. During this machine cycle, the byte indicated by the program counter is read from memory and placed in the processor's Z register. The program counter is incremented again.

(3) Another MEMORY READ machine cycle, consisting of three states, in which the byte indicated by the processor's program counter is read from memory and placed in the W register. The program counter is incremented, in anticipation of the next instruction fetch.

(4) A MEMORY WRITE machine cycle, of three states, in which the contents of the L register are transferred to the memory location pointed to by the present contents of the W and Z registers. The state following the transfer is used to increment the W,Z register pair so that it indicates the next memory location to receive data.

(5) A MEMORY WRITE machine cycle, of three states, in which the contents of the H register are transferred to the new memory location pointed to by the W,Z register pair.

In summary, the "SHLD" instruction cycle contains five machine cycles and takes 16 states to execute.

Most instructions fall somewhere between the extremes typified by the "ADD r" and the "SHLD" instructions. The input (INP) and the output (OUT) instructions, for example, require three machine cycles: a FETCH, to obtain the instruction; a MEMORY READ, to obtain the address of the object peripheral; and an INPUT or an OUTPUT machine cycle, to complete the transfer.

While no one instruction cycle will consist of more then five machine cycles, the following ten different types of machine cycles may occur within an instruction cycle:

(1) FETCH (M1)
(2) MEMORY READ
(3) MEMORY WRITE
(4) STACK READ
(5) STACK WRITE
(6) INPUT
(7) OUTPUT
(8) INTERRUPT
(9) HALT
(10) HALT • INTERRUPT

The machine cycles that actually do occur in a particular instruction cycle depend upon the kind of instruction, with the overriding stipulation that the first machine cycle in any instruction cycle is always a FETCH.

The processor identifies the machine cycle in progress by transmitting an eight-bit status word during the first state of every machine cycle. Updated status information is presented on the 8080's data lines (D_0-D_7), during the SYNC interval. This data should be saved in latches, and used to develop control signals for external circuitry. Table 2-1 shows how the positive-true status information is distributed on the processor's data bus.

Status signals are provided principally for the control of external circuitry. Simplicity of interface, rather than machine cycle identification, dictates the logical definition of individual status bits. You will therefore observe that certain processor machine cycles are uniquely identified by a single status bit, but that others are not. The M_1 status bit (D_6), for example, unambiguously identifies a FETCH machine cycle. A STACK READ, on the other hand, is indicated by the coincidence of STACK and MEMR signals. Machine cycle identification data is also valuable in the test and de-bugging phases of system development. Table 2-1 lists the status bit outputs for each type of machine cycle.

State Transition Sequence:

Every machine cycle within an instruction cycle consists of three to five active states (referred to as T_1, T_2, T_3, T_4, T_5 or T_W). The actual number of states depends upon the instruction being executed, and on the particular machine cycle within the greater instruction cycle. The state transition diagram in Figure 2-4 shows how the 8080 proceeds from state to state in the course of a machine cycle. The diagram also shows how the READY, HOLD, and INTERRUPT lines are sampled during the machine cycle, and how the conditions on these lines may modify the basic transition sequence. In the present discussion, we are concerned only with the basic sequence and with the READY function. The HOLD and INTERRUPT functions will be discussed later.

The 8080 CPU does not directly indicate its internal state by transmitting a "state control" output during each state; instead, the 8080 supplies direct control output (INTE, HLDA, DBIN, $\overline{WR}$ and WAIT) for use by external circuitry.

Recall that the 8080 passes through at least three states in every machine cycle, with each state defined by successive low-to-high transitions of the ϕ_1 clock. Figure 2-5 shows the timing relationships in a typical FETCH machine cycle. Events that occur in each state are referenced to transitions of the ϕ_1 and ϕ_2 clock pulses.

The SYNC signal identifies the first state (T_1) in every machine cycle. As shown in Figure 2-5, the SYNC signal is related to the leading edge of the ϕ_2 clock. There is a delay (t_{DC}) between the low-to-high transition of ϕ_2 and the positive-going edge of the SYNC pulse. There also is a corresponding delay (also t_{DC}) between the next ϕ_2 pulse and the falling edge of the SYNC signal. Status information is displayed on D_0-D_7 during the same ϕ_2 to ϕ_2 interval. Switching of the status signals is likewise controlled by ϕ_2.

The rising edge of ϕ_2 during T_1 also loads the processor's address lines (A_0-A15). These lines become stable within a brief delay (t_{DA}) of the ϕ_2 clocking pulse, and they remain stable until the first ϕ_2 pulse after state T_3. This gives the processor ample time to read the data returned from memory.

Once the processor has sent an address to memory, there is an opportunity for the memory to request a WAIT. This it does by pulling the processor's READY line low, prior to the "Ready set-up" interval (t_{RS}) which occurs during the ϕ_2 pulse within state T_2 or T_W. As long as the READY line remains low, the processor will idle, giving the memory time to respond to the addressed data request. Refer to Figure 2-5.

The processor responds to a wait request by entering an alternative state (T_W) at the end of T_2, rather than proceeding directly to the T_3 state. Entry into the T_W state is indicated by a WAIT signal from the processor, acknowledging the memory's request. A low-to-high transition on the WAIT line is triggered by the rising edge of the ϕ_1 clock and occurs within a brief delay (t_{DC}) of the actual entry into the T_W state.

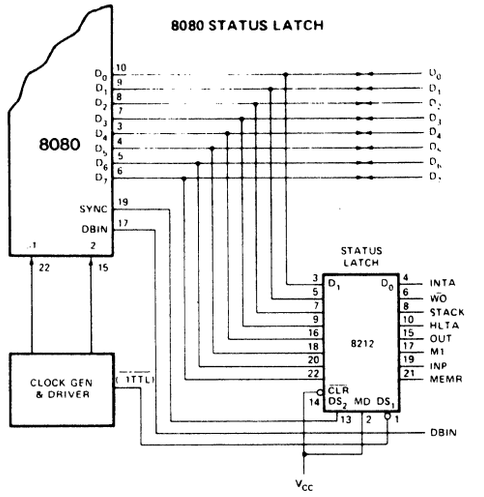
A wait period may be of indefinite duration. The processor remains in the waiting condition until its READY line again goes high. A READY indication **must** precede the falling edge of the ϕ_2 clock by a specified interval (t_{RS}), in order to guarantee an exit from the T_W state. The cycle may then proceed, beginning with the rising edge of the next ϕ_1 clock. A WAIT interval will therefore consist of an integral number of T_W states and will always be a multiple of the clock period.

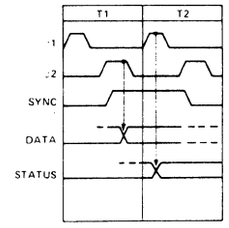
Instructions for the 8080 require from one to five machine cycles for complete execution. The 8080 sends out 8 bit of status information on the data bus at the beginning of each machine cycle (during SYNC time). The following table defines the status information.

STATUS INFORMATION DEFINITION

Symbols	Data Bus Bit	Definition
INTA*	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.

*These three status bits can be used to control the flow of data onto the 8080 data bus.

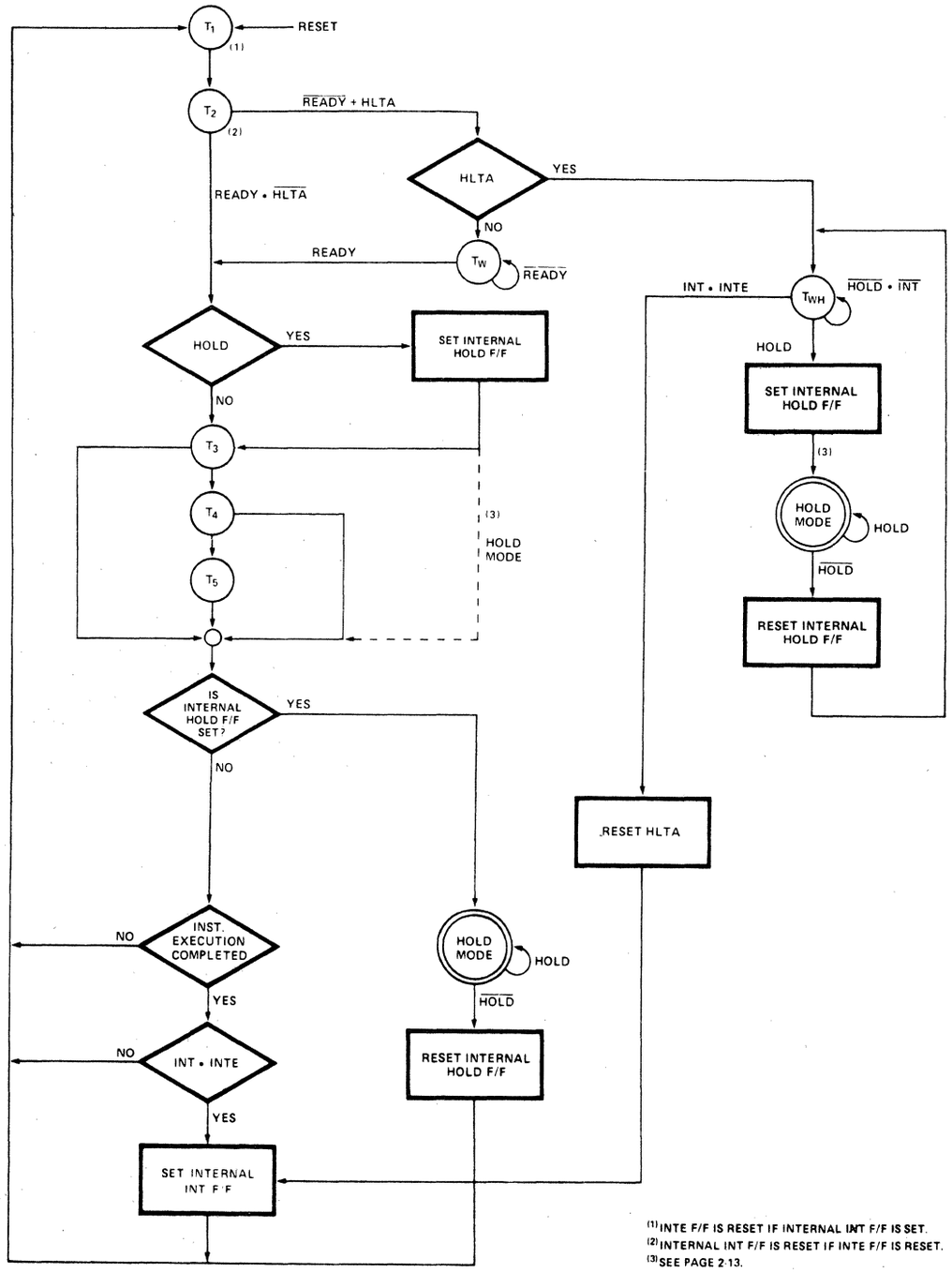




STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	TYPE OF MACHINE CYCLE: ① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INTERRUPT ACKNOWLEDGE WHILE HALT
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0
											Ⓝ STATUS WORD

Table 2-1. 8080 Status Bit Definitions



(1) INTE F/F IS RESET IF INTERNAL INT F/F IS SET.
(2) INTERNAL INT F/F IS RESET IF INTE F/F IS RESET.
(3) SEE PAGE 2-13.

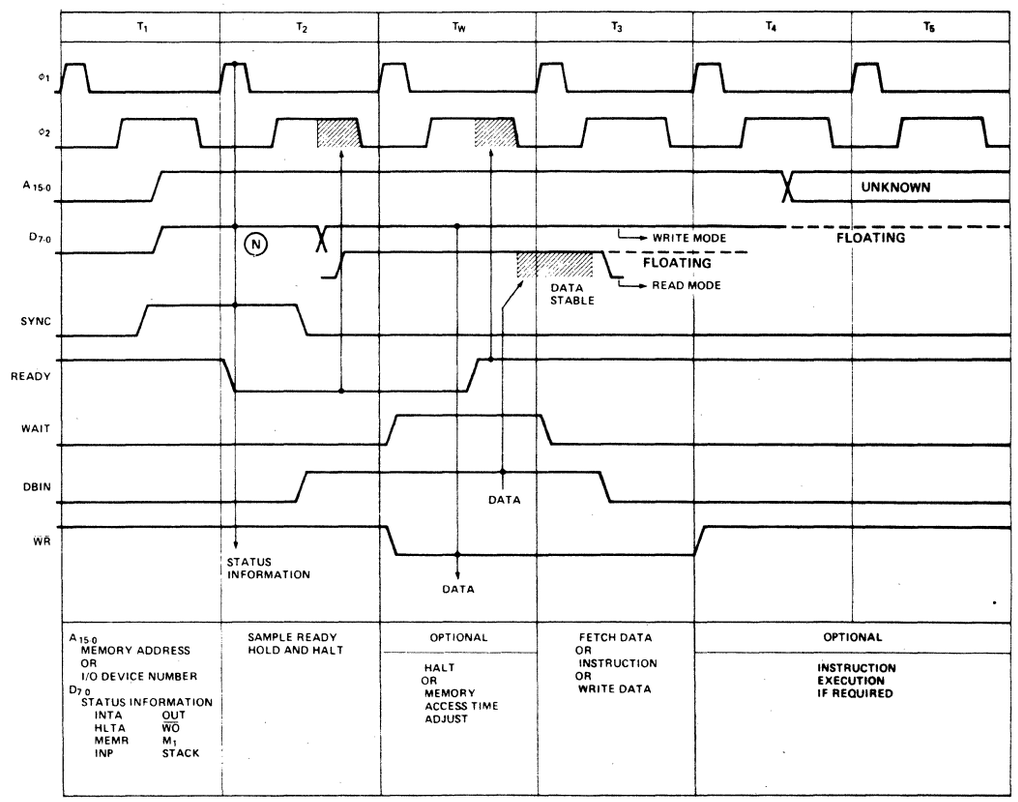
Figure 2-4. CPU State Transition Diagram

The events that take place during the T_3 state are determined by the kind of machine cycle in progress. In a FETCH machine cycle, the processor interprets the data on its data bus as an instruction. During a MEMORY READ or a STACK READ, data on this bus is interpreted as a data word. The processor outputs data on this bus during a MEMORY WRITE machine cycle. During I/O operations, the processor may either transmit or receive data, depending on whether an OUTPUT or an INPUT operation is involved.

Figure 2-6 illustrates the timing that is characteristic of a data input operation. As shown, the low-to-high transition of ϕ_2 during T_2 clears status information from the processor's data lines, preparing these lines for the receipt of incoming data. The data presented to the processor must have stabilized prior to both the "ϕ_1–data set-up" interval (t_{DS1}), that precedes the falling edge of the ϕ_1 pulse defining state T_3, and the "ϕ_2–data set-up" interval (t_{DS2}), that precedes the rising edge of ϕ_2 in state T_3. This same data must remain stable during the "data hold" interval (t_{DH}) that occurs following the rising edge of the ϕ_2 pulse. Data placed on these lines by memory or by other external devices will be sampled during T_3.

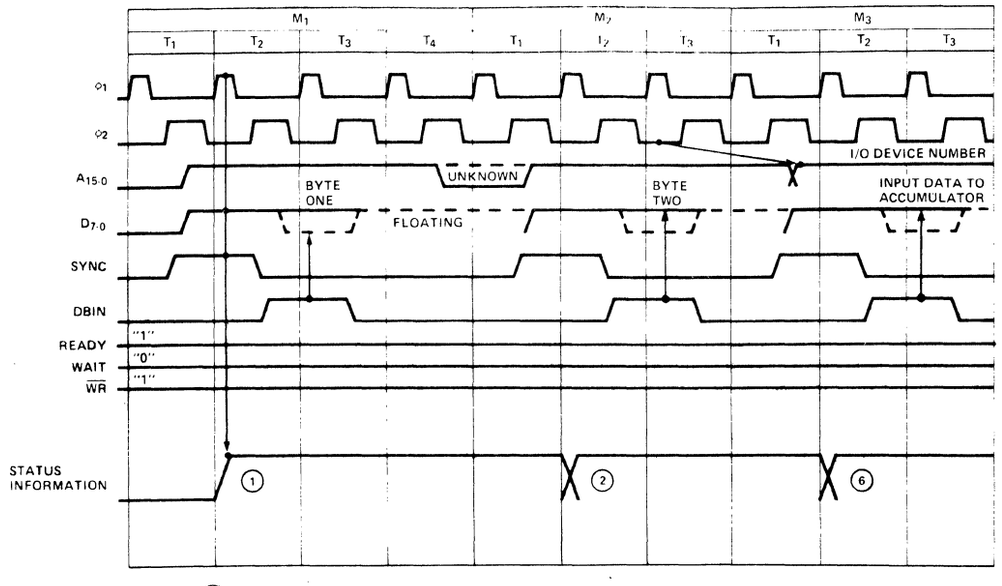
During the input of data to the processor, the 8080 generates a DBIN signal which should be used externally to enable the transfer. Machine cycles in which DBIN is available include: FETCH, MEMORY READ, STACK READ, and INTERRUPT. DBIN is initiated by the rising edge of ϕ_2 during state T2 and terminated by the corresponding edge of ϕ_2 during T_3. Any T_W phases intervening between T_2 and T_3 will therefore extend DBIN by one or more clock periods.

Figure 2-7 shows the timing of a machine cycle in which the processor outputs data. Output data may be destined either for memory or for peripherals. The rising edge of ϕ_2 within state T_2 clears status information from the CPU's data lines, and loads in the data which is to be output to external devices. This substitution takes place within the



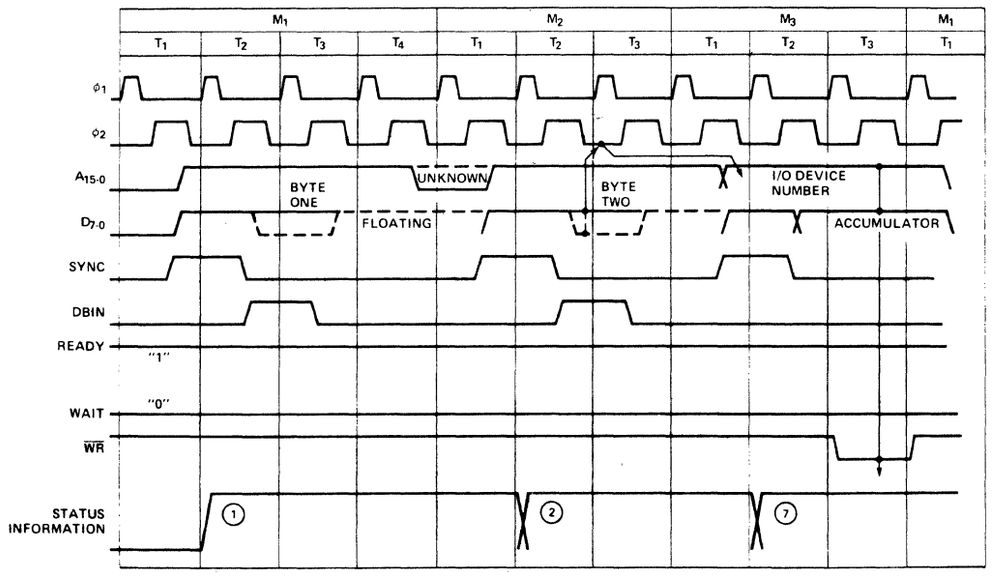
NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-5. Basic 8080 Instruction Cycle



NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-6. Input Instruction Cycle



NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-7. Output Instruction Cycle

"data output delay" interval (t_{DD}) following the ϕ_2 clock's leading edge. Data on the bus remains stable throughout the remainder of the machine cycle, until replaced by updated status information in the subsequent T_1 state. Observe that a READY signal is necessary for completion of an OUTPUT machine cycle. Unless such an indication is present, the processor enters the T_W state, following the T_2 state. Data on the output lines remains stable in the interim, and the processing cycle will not proceed until the READY line again goes high.

The 8080 CPU generates a $\overline{WR}$ output for the synchronization of external transfers, during those machine cycles in which the processor outputs data. These include MEMORY WRITE, STACK WRITE, and OUTPUT. The negative-going leading edge of $\overline{WR}$ is referenced to the rising edge of the first ϕ_1 clock pulse following T_2, and occurs within a brief delay (t_{DC}) of that event. $\overline{WR}$ remains low until re-triggered by the leading edge of ϕ_1 during the state following T_3. Note that any T_W states intervening between T_2 and T_3 of the output machine cycle will necessarily extend $\overline{WR}$, in much the same way that DBIN is affected during data input operations.

All processor machine cycles consist of at least three states: T_1, T_2, and T_3 as just described. If the processor has to wait for a response from the peripheral or memory with which it is communicating, then the machine cycle may also contain one or more T_W states. During the three basic states, data is transferred to or from the processor.

After the T_3 state, however, it becomes difficult to generalize. T_4 and T_5 states are available, if the execution of a particular instruction requires them. But not all machine cycles make use of these states. It depends upon the kind of instruction being executed, and on the particular machine cycle within the instruction cycle. The processor will terminate any machine cycle as soon as its processing activities are completed, rather than proceeding through the T_4 and T_5 states every time. Thus the 8080 may exit a machine cycle following the T_3, the T_4, or the T_5 state and proceed directly to the T_1 state of the next machine cycle.

STATE	ASSOCIATED ACTIVITIES
T_1	A memory address or I/O device number is placed on the Address Bus (A_{15-0}); status information is placed on Data Bus (D_{7-0}).
T_2	The CPU samples the READY and HOLD inputs and checks for halt instruction.
TW (optional)	Processor enters wait state if READY is low or if HALT instruction has been executed.
T3	An instruction byte (FETCH machine cycle), data byte (MEMORY READ, STACK READ) or interrupt instruction (INTERRUPT machine cycle) is input to the CPU from the Data Bus; or a data byte (MEMORY WRITE, STACK WRITE or OUTPUT machine cycle) is output onto the data bus.
T4 T5 (optional)	States T_4 and T_5 are available if the execution of a particular instruction requires them; if not, the CPU may skip one or both of them. T_4 and T_5 are only used for internal processor operations.

Table 2-2. State Definitions

INTERRUPT SEQUENCES

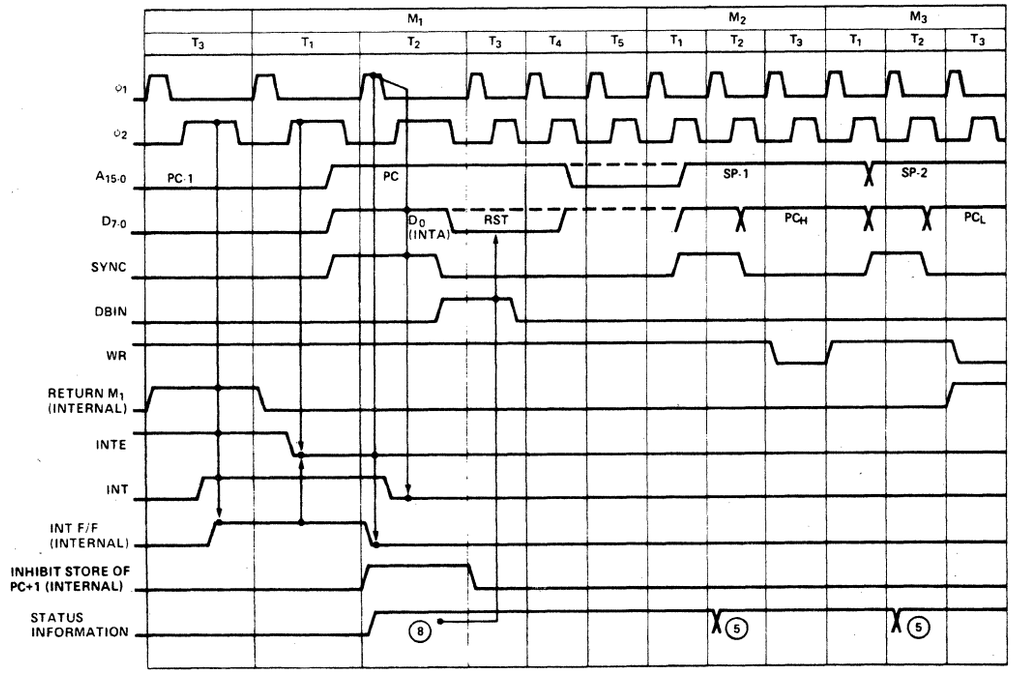
The 8080 has the built-in capacity to handle external interrupt requests. A peripheral device can initiate an interrupt simply by driving the processor's interrupt (INT) line high.

The interrupt (INT) input is asynchronous, and a request may therefore originate at any time during any instruction cycle. Internal logic re-clocks the external request, so that a proper correspondence with the driving clock is established. As Figure 2-8 shows, an interrupt request (INT) arriving during the time that the interrupt enable line (INTE) is high, acts in coincidence with the ϕ_2 clock to set the internal interrupt latch. This event takes place during the last state of the instruction cycle in which the request occurs, thus ensuring that any instruction in progress is completed before the interrupt can be processed.

The INTERRUPT machine cycle which follows the arrival of an enabled interrupt request resembles an ordinary FETCH machine cycle in most respects. The M_1 status bit is transmitted as usual during the SYNC interval. It is accompanied, however, by an INTA status bit (D_0) which acknowledges the external request. The contents of the program counter are latched onto the CPU's address lines during T_1, but the counter itself is not incremented during the INTERRUPT machine cycle, as it otherwise would be. In this way, the pre-interrupt status of the program counter is preserved, so that data in the counter may be restored by the interrupted program after the interrupt request has been processed.

The interrupt cycle is otherwise indistinguishable from an ordinary FETCH machine cycle. The processor itself takes no further special action. It is the responsibility of the peripheral logic to see that an eight-bit interrupt instruction is "jammed" onto the processor's data bus during state T_3. In a typical system, this means that the data-in bus from memory must be temporarily disconnected from the processor's main data bus, so that the interrupting device can command the main bus without interference.

The 8080's instruction set provides a special one-byte call which facilitates the processing of interrupts (the ordinary program Call takes three bytes). This is the RESTART instruction (RST). A variable three-bit field embedded in the eight-bit field of the RST enables the interrupting device to direct a Call to one of eight fixed memory locations. The decimal addresses of these dedicated locations are: 0, 8, 16, 24, 32, 40, 48, and 56. Any of these addresses may be used to store the first instruction(s) of a routine designed to service the requirements of an interrupting device. Since the (RST) is a call, completion of the instruction also stores the old program counter contents on the STACK.



NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-8. Interrupt Timing

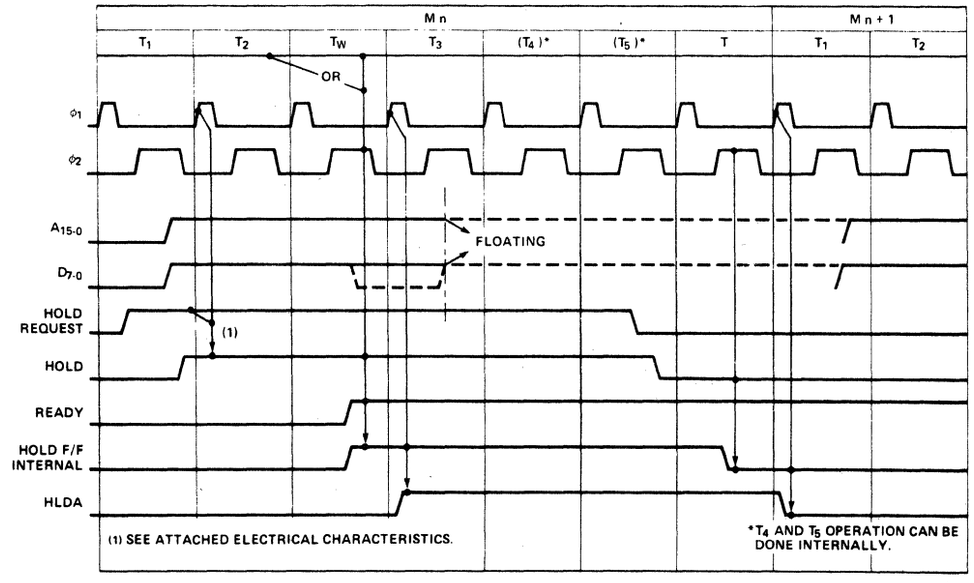


Figure 2-9. HOLD Operation (Read Mode)

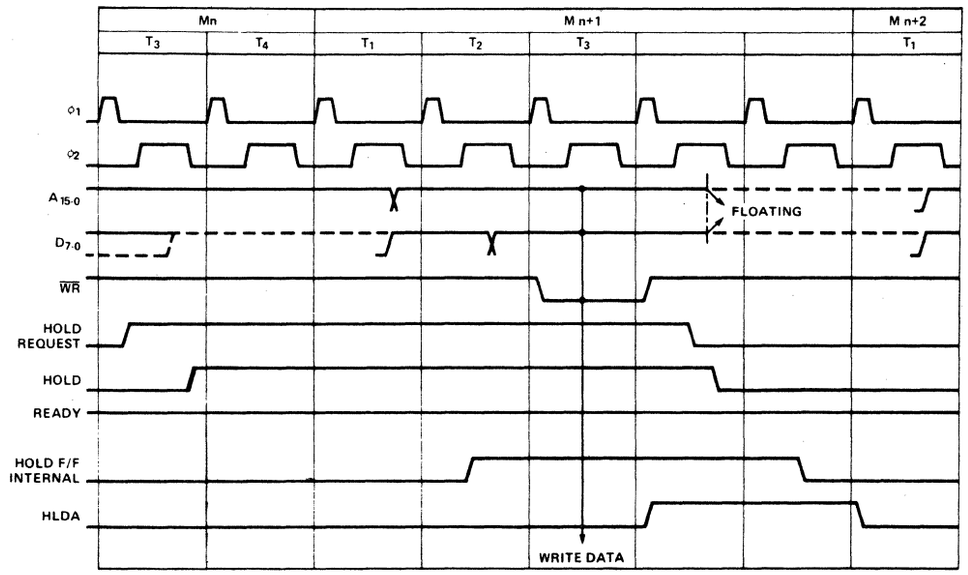


Figure 2-10. HOLD Operation (Write Mode)

HOLD SEQUENCES

The 8080A CPU contains provisions for Direct Memory Access (DMA) operations. By applying a HOLD to the appropriate control pin on the processor, an external device can cause the CPU to suspend its normal operations and relinquish control of the address and data busses. The processor responds to a request of this kind by floating its address to other devices sharing the busses. At the same time, the processor acknowledges the HOLD by placing a high on its HLDA outpin pin. During an acknowledged HOLD, the address and data busses are under control of the peripheral which originated the request, enabling it to conduct memory transfers without processor intervention.

Like the interrupt, the HOLD input is synchronized internally. A HOLD signal must be stable prior to the "Hold set-up" interval (t_{HS}), that precedes the rising edge of ϕ_2.

Figures 2-9 and 2-10 illustrate the timing involved in HOLD operations. Note the delay between the asynchronous HOLD REQUEST and the re-clocked HOLD. As shown in the diagram, a coincidence of the READY, the HOLD, and the ϕ_2 clocks sets the internal hold latch. Setting the latch enables the subsequent rising edge of the ϕ_1 clock pulse to trigger the HLDA output.

Acknowledgement of the HOLD REQUEST precedes slightly the actual floating of the processor's address and data lines. The processor acknowledges a HOLD at the beginning of T_3, if a read or an input machine cycle is in progress (see Figure 2-9). Otherwise, acknowledgement is deferred until the beginning of the state following T_3 (see Figure 2-10). In both cases, however, the HLDA goes high within a specified delay (t_{DC}) of the rising edge of the selected ϕ_1 clock pulse. Address and data lines are floated within a brief delay after the rising edge of the next ϕ_2 clock pulse. This relationship is also shown in the diagrams.

To all outward appearances, the processor has suspended its operations once the address and data busses are floated. Internally, however, certain functions may continue. If a HOLD REQUEST is acknowledged at T_3, and if the processor is in the middle of a machine cycle which requires four or more states to complete, the CPU proceeds through T_4 and T_5 before coming to a rest. Not until the end of the machine cycle is reached will processing activities cease. Internal processing is thus permitted to overlap the external DMA transfer, improving both the efficiency and the speed of the entire system.

The processor exits the holding state through a sequence similar to that by which it entered. A HOLD REQUEST is terminated asynchronously when the external device has completed its data transfer. The HLDA output returns to a low level following the leading edge of the next $\phi 1$ clock pulse. Normal processing resumes with the machine cycle following the last cycle that was executed.

HALT SEQUENCES

When a halt instruction (HLT) is executed, the CPU enters the halt state (T_{WH}) after state T_2 of the next machine cycle, as shown in Figure 2-11. There are only three ways in which the 8080 can exit the halt state:

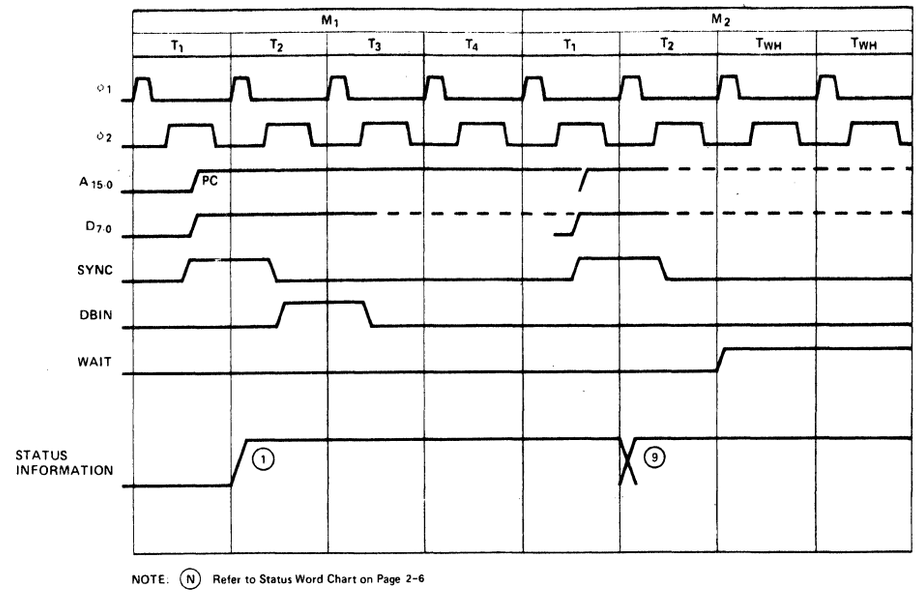
- A high on the RESET line will always reset the 8080 to state T_1; RESET also clears the program counter.
- A HOLD input will cause the 8080 to enter the hold state, as previously described. When the HOLD line goes low, the 8080 re-enters the halt state on the rising edge of the next ϕ_1 clock pulse.
- An interrupt (i.e., INT goes high while INTE is enabled) will cause the 8080 to exit the Halt state and enter state T_1 on the rising edge of the next ϕ_1 clock pulse. NOTE: The interrupt enable (INTE) flag **must** be set when the halt state is entered; otherwise, the 8080 will only be able to exit via a RESET signal.

Figure 2-12 illustrates halt sequencing in flow chart form.

START-UP OF THE 8080 CPU

When power is applied initially to the 8080, the processor begins operating immediately. The contents of its program counter, stack pointer, and the other working registers are naturally subject to random factors and cannot be specified. For this reason, it will be necessary to begin the power-up sequence with RESET.

An external RESET signal of three clock period duration (minimum) restores the processor's internal program counter to zero. Program execution thus begins with memory location zero, following a RESET. Systems which require the processor to wait for an explicit start-up signal will store a halt instruction (EI, HLT) in the first two locations. A manual or an automatic INTERRUPT will be used for starting. In other systems, the processor may begin executing its stored program immediately. Note, however, that the RESET has no effect on status flags, or on any of the processor's working registers (accumulator, registers, or stack pointer). The contents of these registers remain indeterminate, until initialized explicitly by the program.



NOTE. (N) Refer to Status Word Chart on Page 2-6

Figure 2-11. HALT Timing

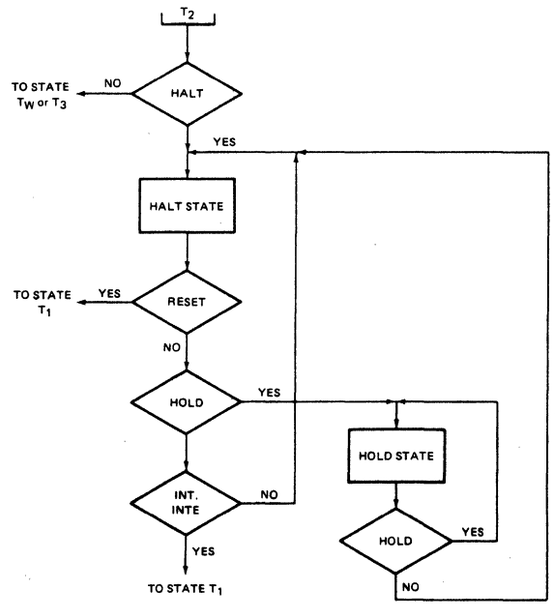
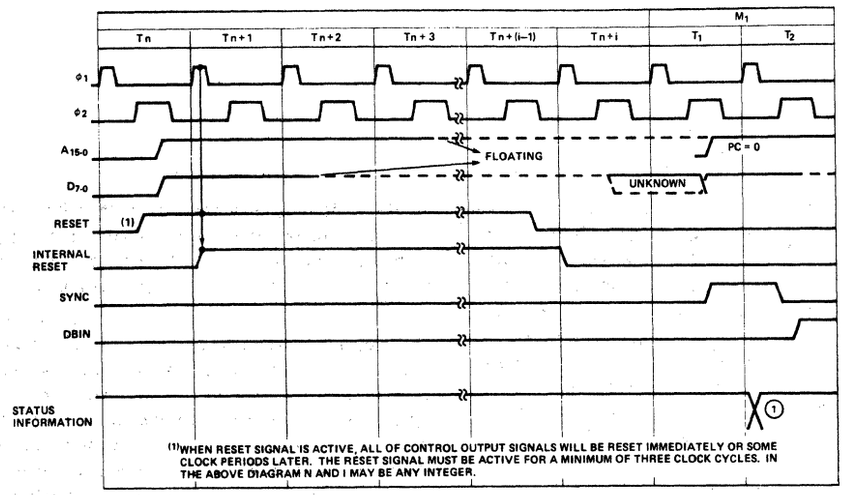


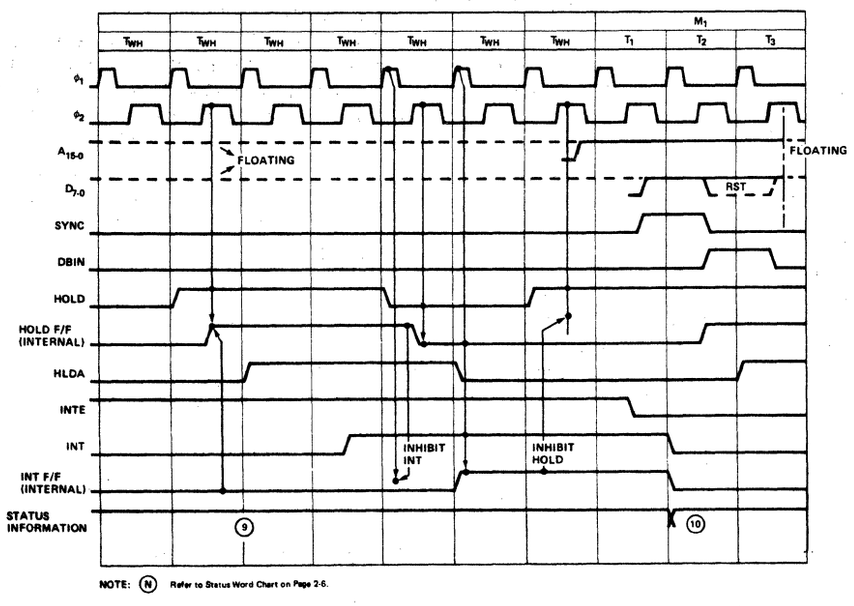
Figure 2-12. HALT Sequence Flow Chart.



(1)WHEN RESET SIGNAL IS ACTIVE, ALL OF CONTROL OUTPUT SIGNALS WILL BE RESET IMMEDIATELY OR SOME CLOCK PERIODS LATER. THE RESET SIGNAL MUST BE ACTIVE FOR A MINIMUM OF THREE CLOCK CYCLES. IN THE ABOVE DIAGRAM N AND I MAY BE ANY INTEGER.

NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-13. Reset.



NOTE: (N) Refer to Status Word Chart on Page 2-6.

Figure 2-14. Relation between HOLD and INT in the HALT State.

MNEMONIC	OP CODE		M1[1]					M2		
	$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
MOV r1, r2	0 1 D D	D S S S	PC OUT STATUS	PC = PC +1	INST→TMP/IR	(SSS)→TMP	(TMP)→DDD			
MOV r, M	0 1 D D	D 1 1 0	↑	↑	↑	X[3]		HL OUT STATUS[6]	DATA→	DDD
MOV M, r	0 1 1 1	0 S S S	↑	↑	↑	(SSS)→TMP		HL OUT STATUS[7]	(TMP)→	DATA BUS
SPHL	1 1 1 1	1 0 0 1	↑	↑	↑	(HL)	SP			
MVI r, data	0 0 D D	D 1 1 0	↑	↑	↑	X		PC OUT STATUS[6]	B2→	DDDD
MVI M, data	0 0 1 1	0 1 1 0	↑	↑	↑	X		↑	B2→	TMP
LXI rp, data	0 0 R P	0 0 0 1	↑	↑	↑	X		↑	PC = PC + 1 B2→	r1
LDA addr	0 0 1 1	1 0 1 0	↑	↑	↑	X		↑	PC = PC + 1 B2→	Z
STA addr	0 0 1 1	0 0 1 0	↑	↑	↑	X		↑	PC = PC + 1 B2→	Z
LHLD addr	0 0 1 0	1 0 1 0	↑	↑	↑	X		↑	PC = PC + 1 B2→	Z
SHLD addr	0 0 1 0	0 0 1 0	↑	↑	↑	X		PC OUT STATUS[6]	PC = PC + 1 B2→	Z
LDAX rp[4]	0 0 R P	1 0 1 0	↑	↑	↑	X		rp OUT STATUS[6]	DATA→	A
STAX rp[4]	0 0 R P	0 0 1 0	↑	↑	↑	X		rp OUT STATUS[7]	(A) →	DATA BUS
XCHG	1 1 1 0	1 0 1 1	↑	↑	↑	(HL)←→(DE)				
ADD r	1 0 0 0	0 S S S	↑	↑	↑	(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ADD M	1 0 0 0	0 1 1 0	↑	↑	↑	(A)→ACT		HL OUT STATUS[6]	DATA→	TMP
ADI data	1 1 0 0	0 1 1 0	↑	↑	↑	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→	TMP
ADC r	1 0 0 0	1 S S S	↑	↑	↑	(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)+CY→A	
ADC M	1 0 0 0	1 1 1 0	↑	↑	↑	(A)→ACT		HL OUT STATUS[6]	DATA→	TMP
ACI data	1 1 0 0	1 1 1 0	↑	↑	↑	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→	TMP
SUB r	1 0 0 1	0 S S S	↑	↑	↑	(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)→A	
SUB M	1 0 0 1	0 1 1 0	↑	↑	↑	(A)→ACT		HL OUT STATUS[6]	DATA→	TMP
SUI data	1 1 0 1	0 1 1 0	↑	↑	↑	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→	TMP
SBB r	1 0 0 1	1 S S S	↑	↑	↑	(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)-CY→A	
SBB M	1 0 0 1	1 1 1 0	↑	↑	↑	(A)→ACT		HL OUT STATUS[6]	DATA→	TMP
SBI data	1 1 0 1	1 1 1 0	↑	↑	↑	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→	TMP
INR r	0 0 D D	D 1 0 0	↑	↑	↑	(DDD)→TMP (TMP) + 1→ALU	ALU→DDD			
INR M	0 0 1 1	0 1 0 0	↑	↑	↑	X		HL OUT STATUS[6]	DATA→ (TMP)+1→	TMP ALU
DCR r	0 0 D D	D 1 0 1	↑	↑	↑	(DDD)→TMP (TMP)+1→ALU	ALU→DDD			
DCR M	0 0 1 1	0 1 0 1	↑	↑	↑	X		HL OUT STATUS[6]	DATA→ (TMP)-1→	TMP ALU
INX rp	0 0 R P	0 0 1 1	↑	↑	↑	(RP) + 1	RP			
DCX rp	0 0 R P	1 0 1 1	↑	↑	↑	(RP) - 1	RP			
DAD rp[8]	0 0 R P	1 0 0 1	↑	↑	↑	X		(ri)→ACT	(L)→TMP, (ACT)+(TMP)→ALU	ALU→L, CY
DAA	0 0 1 0	0 1 1 1	↑	↑	↑	DAA→A, FLAGS[10]				
ANA r	1 0 1 0	0 S S S	↑	↑	↑	(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ANA M	1 0 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		HL OUT STATUS[6]	DATA→	TMP

M3			M4			M5						
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5		
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)-(TMP); FLAGS											
[9]	(ACT)-(TMP); FLAGS											
PC OUT STATUS[6]	PC = PC + 1	B3 → W									WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1	B3 → W									WZ OUT STATUS[11,12]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1	B3 → W	SP OUT STATUS[16]	(PCH) → SP = SP - 1	DATA BUS	SP OUT STATUS[16]	(PCL) →	DATA BUS			WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1	B3 → W[13]	SP OUT STATUS[16]	(PCH) → SP = SP - 1	DATA BUS	SP OUT STATUS[16]	(PCL) →	DATA BUS			WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1	DATA → W									WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1	DATA → W									WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[16]	(TMP = 00NNN000) → Z (PCL) → DATA BUS										WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[16]		(rl) → DATA BUS										
SP OUT STATUS[16]		FLAGS → DATA BUS										
SP OUT STATUS[15]	SP = SP + 1	DATA → rh										
SP OUT STATUS[15]	SP = SP + 1	DATA → A										
SP OUT STATUS[15]		DATA → W	SP OUT STATUS[16]	(H) →	DATA BUS	SP OUT STATUS[16]	(L) →	DATA BUS	(WZ) →	HL		
WZ OUT STATUS[18]		DATA → A										
WZ OUT STATUS[18]		(A) → DATA BUS										

NOTES:

1. The first memory cycle (M1) is always an instruction fetch; the first (or only) byte, containing the op code, is fetched during this cycle.

2. If the READY input from memory is not high during T2 of each memory cycle, the processor will enter a wait state (TW) until READY is sampled as high.

3. States T4 and T5 are present, as required, for operations which are completely internal to the CPU. The contents of the internal bus during T4 and T5 are available at the data bus; this is designed for testing purposes only. An "X" denotes that the state is present, but is only used for such internal operations as instruction decoding.

4. Only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

5. These states are skipped.

6. Memory read sub-cycles; an instruction or data word will be read.

7. Memory write sub-cycle.

8. The READY signal is not required during the second and third sub-cycles (M2 and M3). The HOLD signal is accepted during M2 and M3. The SYNC signal is not generated during M2 and M3. During the execution of DAD, M2 and M3 are required for an internal register-pair add; memory is not referenced.

9. The results of these arithmetic, logical or rotate instructions are not moved into the accumulator (A) until state T2 of the next instruction cycle. That is, A is loaded while the next instruction is being fetched; this overlapping of operations allows for faster processing.

10. If the value of the least significant 4-bits of the accumulator is greater than 9 or if the auxiliary carry bit is set, 6 is added to the accumulator. If the value of the most significant 4-bits of the accumulator is now greater than 9, or if the carry bit is set, 6 is added to the most significant 4-bits of the accumulator.

11. This represents the first sub-cycle (the instruction fetch) of the next instruction cycle.

12. If the condition was met, the contents of the register pair WZ are output on the address lines ($A_{0\text{-}15}$) instead of the contents of the program counter (PC).

13. If the condition was not met, sub-cycles M4 and M5 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

14. If the condition was not met, sub-cycles M2 and M3 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

15. Stack read sub-cycle.

16. Stack write sub-cycle.

17.

CONDITION	CCC
NZ – not zero (Z = 0)	000
Z – zero (Z = 1)	001
NC – no carry (CY = 0)	010
C – carry (CY = 1)	011
PO – parity odd (P = 0)	100
PE – parity even (P = 1)	101
P – plus (S = 0)	110
M – minus (S = 1)	111

18. I/O sub-cycle: the I/O port's 8-bit select code is duplicated on address lines 0-7 ($A_{0\text{-}7}$) and 8-15 ($A_{8\text{-}15}$).

19. Output sub-cycle.

20. The processor will remain idle in the halt state until an interrupt, a reset or a hold is accepted. When a hold request is accepted, the CPU enters the hold mode; after the hold mode is terminated, the processor returns to the halt state. After a reset is accepted, the processor begins execution at memory location zero. After an interrupt is accepted, the processor executes the instruction forced onto the data bus (usually a restart instruction).

SSS or DDD	Value	rp	Value
A	111	B	00
B	000	D	01
C	001	H	10
D	010	SP	11
E	011		
H	100		
L	101		

M3			M4			M5				
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5
HL OUT STATUS[7]	(TMP) →	DATA BUS								
PC OUT STATUS[6]	PC = PC + 1 B3 →	rh								
	PC = PC + 1 B3 →	W	WZ OUT STATUS[6]	DATA →	A					
	PC = PC + 1 B3 →	W	WZ OUT STATUS[7]	(A) →	DATA BUS					
	PC = PC + 1 B3 →	W	WZ OUT STATUS[6]	DATA → WZ = WZ + 1	L	WZ OUT STATUS[6]	DATA →	H		
PC OUT STATUS[6]	PC = PC + 1 B3 →	W	WZ OUT STATUS[7]	(L) → WZ = WZ + 1	DATA BUS	WZ OUT STATUS[7]	(H) →	DATA BUS		
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)-CY→A									
[9]	(ACT)-(TMP)-CY→A									
HL OUT STATUS[7]	ALU →	DATA BUS								
HL OUT STATUS[7]	ALU →	DATA BUS								
(rh)→ACT	(H)→TMP (ACT)+(TMP)+CY→ALU	ALU→H, CY								
[9]	(ACT)+(TMP)→A									

MNEMONIC	OP CODE		M1[1]					M2		
	$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
ANI data	1 1 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
XRA r	1 0 1 0	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TPM)→A	
XRA M	1 0 1 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	TMP
XRI data	1 1 1 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
ORA r	1 0 1 1	0 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TMP)→A	
ORA M	1 0 1 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	TMP
ORI data	1 1 1 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
CMP r	1 0 1 1	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)-(TMP), FLAGS	
CMP M	1 0 1 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA →	TMP
CPI data	1 1 1 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2 →	TMP
RLC	0 0 0 0	0 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RRC	0 0 0 0	1 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RAL	0 0 0 1	0 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
RAR	0 0 0 1	1 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
CMA	0 0 1 0	1 1 1 1				$(\overline{A})$→A				
CMC	0 0 1 1	1 1 1 1				$\overline{CY}$→CY				
STC	0 0 1 1	0 1 1 1				1→CY				
JMP addr	1 1 0 0	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2 →	Z
J cond addr[17]	1 1 C C	C 0 1 0				JUDGE CONDITION		PC OUT STATUS[6]	PC = PC + 1 B2 →	Z
CALL addr	1 1 0 0	1 1 0 1				SP = SP - 1		PC OUT STATUS[6]	PC = PC + 1 B2 →	Z
C cond addr[17]	1 1 C C	C 1 0 0				JUDGE CONDITION IF TRUE, SP = SP - 1		PC OUT STATUS[6]	PC = PC + 1 B2 →	Z
RET	1 1 0 0	1 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	Z
R cond addr[17]	1 1 C C	C 0 0 0			INST→TMP/IR	JUDGE CONDITION[14]		SP OUT STATUS[15]	SP = SP + 1 DATA →	Z
RST n	1 1 N N	N 1 1 1			ϕ→W INST→TMP/IR	SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (PCH) →	DATA BUS
PCHL	1 1 1 0	1 0 0 1			INST→TMP/IR	(HL) → PC				
PUSH rp	1 1 R P	0 1 0 1				SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (rh) →	DATA BUS
PUSH PSW	1 1 1 1	0 1 0 1				SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (A) →	DATA BUS
POP rp	1 1 R P	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	r1
POP PSW	1 1 1 1	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	FLAGS
XTHL	1 1 1 0	0 0 1 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA →	Z
IN port	1 1 0 1	1 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2 →	Z, W
OUT port	1 1 0 1	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2 →	Z, W
EI	1 1 1 1	1 0 1 1				SET INTE F/F				
DI	1 1 1 1	0 0 1 1				RESET INTE F/F				
HLT	0 1 1 1	0 1 1 0				X		PC OUT STATUS	HALT MODE[20]	
NOP	0 0 0 0	0 0 0 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	X				

5300-1/6300-1
5301-1/6301-1

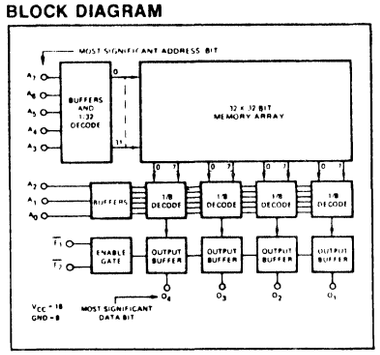
1024-Bit Bipolar (256 x 4) Programmable Read Only Memory

PRODUCT FEATURES

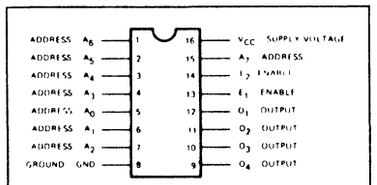
- I_{CC}–120mA max.
- T_{AA}–60 ns max.
- Very high programmability—typically 95% of all units will program to completion
- Field programmable with simple programming procedure
- Fast programming time—average of 1 ms/bit
- Pin compatible with lower cost H5200/H6200 and H5201/6201 ROMs.

	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
6300-1		X		X
6301-1		X	X	
5300-1	X			X
5301-1	X		X	

BLOCK DIAGRAM



PIN CONFIGURATION



To enable the device, $\overline{E}_1$ and $\overline{E}_2$ must be LOW

H5200/H6200
H5201/H6201

1024-Bit Bipolar (256 x 4) Read Only Memory

PRODUCT FEATURES

- T_{AA}–45 ns max. (0°C to 75°C) and ±5% voltage variation (H6200, H6201)
- T_{AA}–60 ns max. (55°C to 125°C) and ±10% voltage variation (H5200, H5201)
- I_{CC}–125 mA max. (0°C to 70°C)
- I_{CC}– mA max. (–55°C to +125°C)
- Advanced Schottky processing
- Low input current (250 μA max.)
- Single-layer metal for reliability
- Pin compatible with 5300-1/6300-1 and 5301-1/6301-1 PROMs

	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
H6200		X		X
H6201		X	X	
H5200	X			X
H5201	X		X	

Monolithic Memories INCORPORATED

4096 BIT BIPOLAR (1024x4) ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

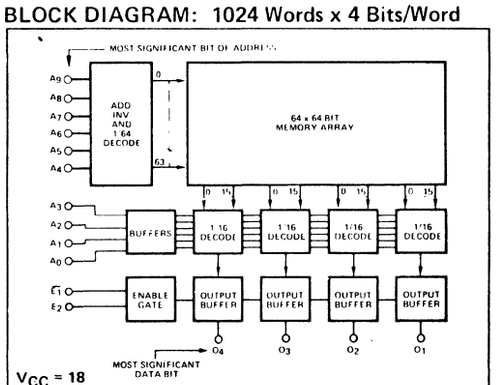
5350-1/6350-1
5351-1/6351-1

PRODUCT FEATURES

- Very High Programmability: Typically 95% of All Units Will Program to Completion
- Field Programmable with Simple Programming Procedure
- Fast Programming Time – Average of 1ms/bit
- Pin Compatible with 5250-1/6250-1-1 ROMs
- Very High Reliability
- Fully Decoded – On Chip Address Decoding
- Three-State or Open Collector Outputs
- Special On Chip Circuitry Permits V_{OL} Testing Before Programming
- Pin Configuration Allows Easy Upgrading Present 512 x 4 Designs

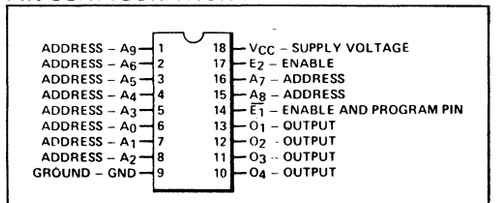
	MILITARY	COMMERCIAL	THREE STATE	OPEN COLLECTOR
5350-1	X			X
5351-1	X		X	
6350-1		X		X
6351-1		X	X	

BLOCK DIAGRAM: 1024 Words x 4 Bits/Word



V_{CC} = 18
GND = 9

PIN CONFIGURATION

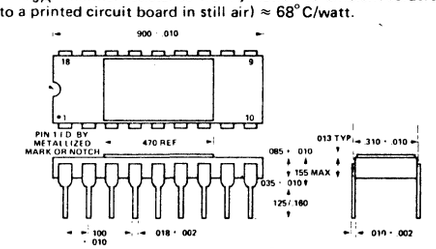


To enable the device $\overline{E_1}$ must be LOW and E_2 must be HIGH.

PACKAGE OUTLINE

18 Lead Side Brazed Ceramic DIP

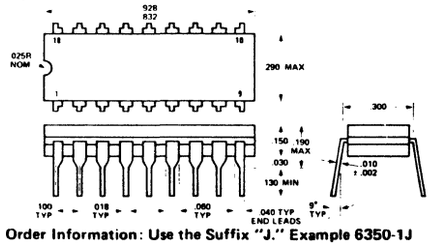
θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 68°C/watt.



Order Information: Use the Suffix "D". Example 6350-1D

18 Lead CERDIP

θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 75°C/watt.



Order Information: Use the Suffix "J." Example 6350-1J

NOTE: θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt for both packages.

Monolithic Memories INCORPORATED

1165 East Arques Avenue/Sunnyvale, California 94086 (408) 739-3535

TWX 910–339-9229

intel

2116 FAMILY

16,384 X 1 BIT DYNAMIC RAM

	2116-2	2116-3	2116-4
Max. Access Time (ns)	200	250	300
Read, Write Cycle (ns)	350	375.	425
Read-Modify-Write Cycle (ns)	400	525	595

- **Highest Density 16K RAM: Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on all Power Supplies +12V, +5V, −5V**
- **On-Chip Latches for Address and Data In**
- **Only 64 Refresh Cycles Required Every 2 ms**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**

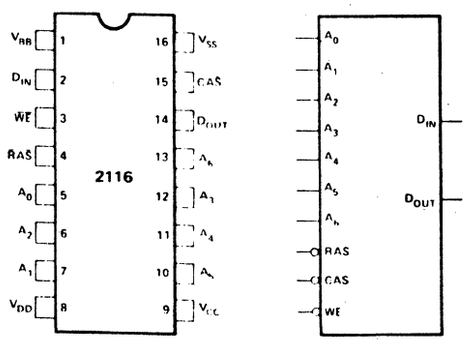
The Intel 2116 is a 16,384 word by 1 bit MOS RAM fabricated with two layer polysilicon N-MOS technology – a production-proven process for high performance, high reliability, and high functional density. The 2116 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2116 allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment. The 2116 is designed to facilitate upgrading of 2104A-type 4K RAM systems to 16K capabilities.

The use of the 16 pin package is made possible by multiplexing the 14 address bits (required to address 1 of 16,384 bits) into the 2116 on 7 address input pins. The two 7 bit address words are latched into the 2116 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing can be accomplished every 2 ms by any one of the three following methods: (1) $\overline{CAS}$ before $\overline{RAS}$ cycles on 64 addresses, A_0–A_5, (2) $\overline{RAS}$-only cycles on 128 address, A_0- A_6, or (3) normal read or write cycles on 128 addresses, A_0–A_6. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed. The output is brought to a high impedance state by a $\overline{CAS}$-only cycle or by a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

PIN CONFIGURATION

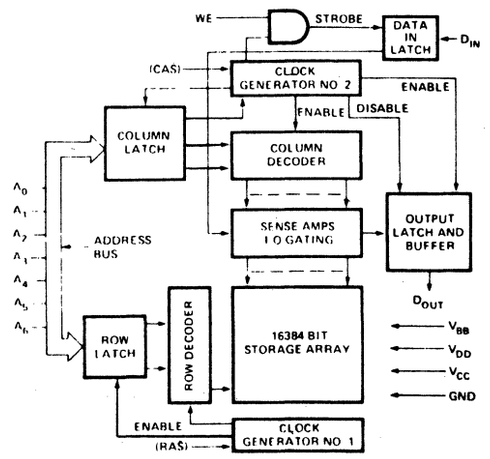


LOGIC SYMBOL

PIN NAMES

A_0 A_6	ADDRESS INPUTS	WE	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

BLOCK DIAGRAM



MCM6570 MCM6571 MCM6571A MCM6572 thru MCM6579

8192-BIT READ ONLY MEMORIES
ROW SELECT CHARACTER GENERATORS

The MCM6570 is a mask-programmable 8192-bit horizontal-scan (row select) character generator. It contains 128 characters in a 7 x 9 matrix, and has the capability of shifting certain characters that normally extend below the baseline, such as j, y, g, p, and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character – a feature previously requiring external circuitry.

A seven-bit address code is used to select one of the 128 available characters. Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7 x 9 matrix. When a specific four bit binary row select code is applied, a word of seven parallel bits appears at the output. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7 x 9 character in one of two pre-programmed positions on the 16-row matrix, with the positions defined by the four row select inputs. Rows that are not part of the character are automatically blanked.

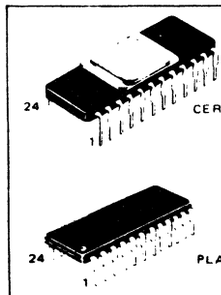
The MCM6571, MCM6571A, and MCM6572 thru MCM6579 are pre-programmed versions of the MCM6570. They contain various sets of characters to meet the requirements of diverse applications. The complete patterns of these devices are contained in this data sheet.

- Static Operation
- TTL Compatibility
- CMOS Compatibility (5 V)
- Shifted Character Capability (Except MCM6572, MCM6573)
- Maximum Access Time = 500 ns

MOS
(N-CHANNEL, LOW THRESHOLD)

8 K
READ ONLY MEMORIES

HORIZONTAL-SCAN
CHARACTER GENERATORS
WITH SHIFTED CHARACTERS



L SUFFIX
CERAMIC PACKAGE
CASE 684

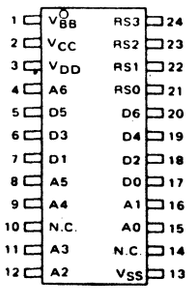
P SUFFIX
PLASTIC PACKAGE
CASE 709

ABSOLUTE MAXIMUM RATINGS (See Note 1, Voltages referenced to V_{SS})

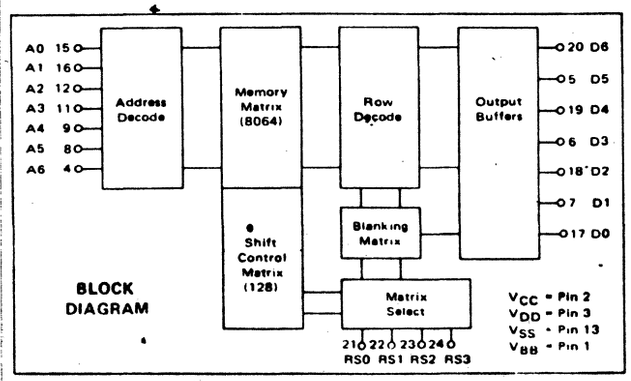
Rating	Symbol	Value	Unit
Supply Voltages	V_{CC} V_{DD} V_{BB}	-0.3 to +6.0 -0.3 to +15 -10 to +0.3	Vdc
Data Input Voltage	V_{in}	-0.3 to +15	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit

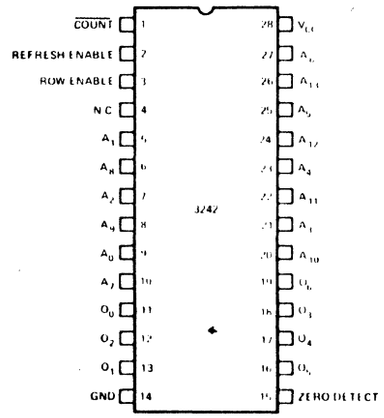
3242
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 16K DYNAMIC RAMs

- **Ideal For 2116**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 28-Pin DIP**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**
- **Address Input to Output Delay: 9ns Driving 15 pF, 25ns Driving 250pF**

The Intel® 3242 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to 7 output address pins. The device also contains a 7 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3242 makes it especially suitable for use with high speed N-channel RAMs like the 2116.

The 3242 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process and is packaged in a hermetically sealed 28 pin Type D package.

PIN CONFIGURATION



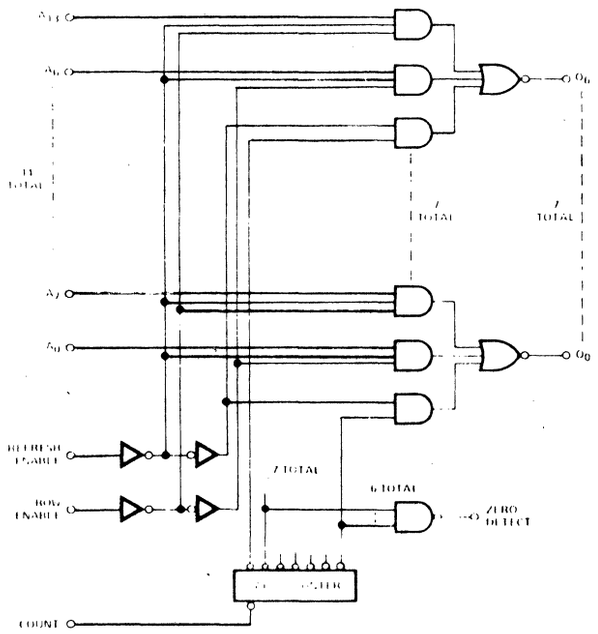
NOTE A_0 THROUGH A_6 ARE ROW ADDRESSES
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

COUNT ADVANCES INTERNAL REFRESH COUNTER
ZERO DETECT INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)

LOGIC DIAGRAM



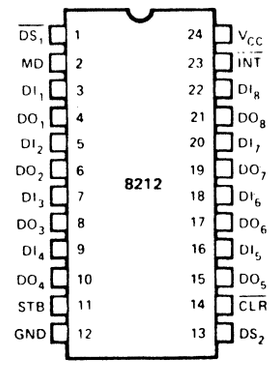
8212
EIGHT-BIT INPUT/OUTPUT PORT

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current — .25 mA Max.**
- **Three State Outputs**
- **Outputs Sink 15 mA**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

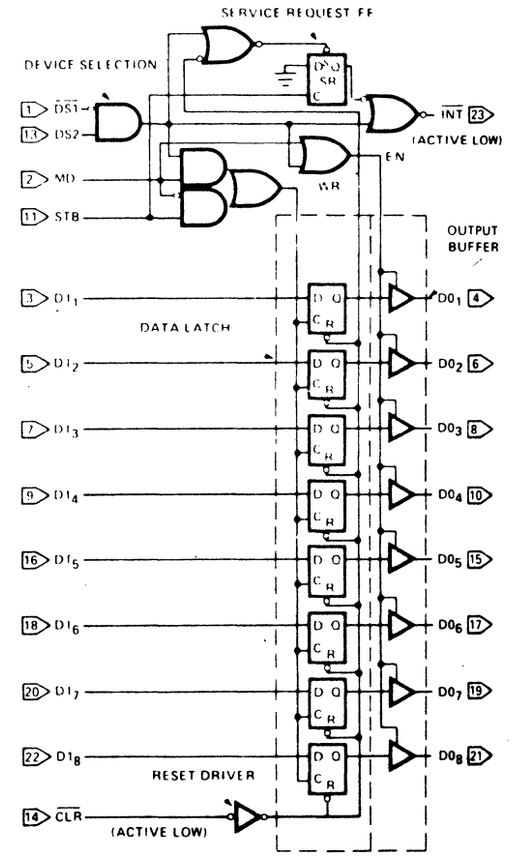
PIN CONFIGURATION



PIN NAMES

DI_1 DI_8	DATA IN
DO_1 DO_8	DATA OUT
$\overline{DS_1}$ DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



8214
PRIORITY INTERRUPT CONTROL UNIT

- **Eight Priority Levels**
- **Current Status Register**
- **Priority Comparator**
- **Fully Expandable**
- **High Performance (50ns)**
- **24-Pin Dual In-Line Package**

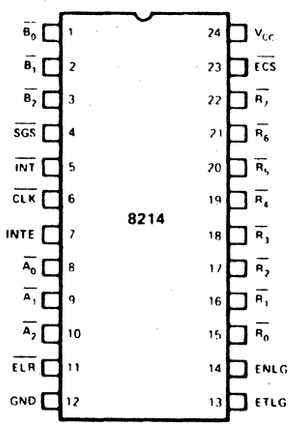
The 8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

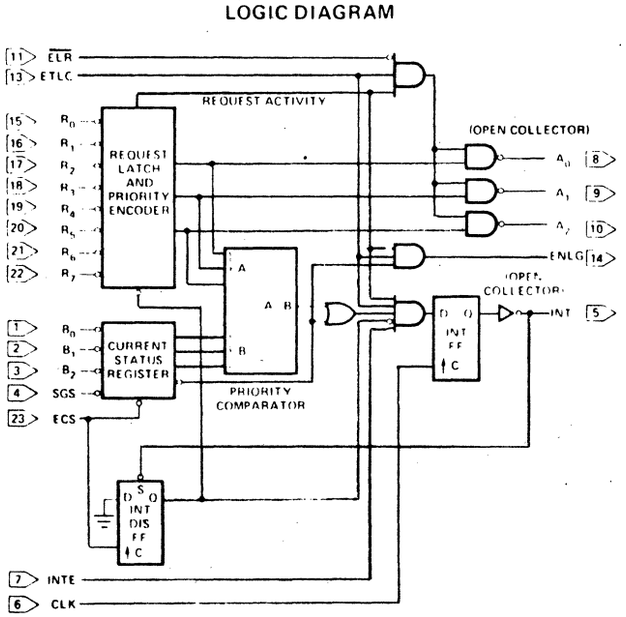
The 8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

PIN CONFIGURATION



LOGIC DIAGRAM



PIN NAMES

INPUTS	
R_0 R_7	REQUEST LEVELS (R_7 HIGHEST PRIORITY)
B_0 B_2	CURRENT STATUS
SGS	STATUS GROUP SELECT
ECS	ENABLE CURRENT STATUS
INTE	INTERRUPT ENABLE
CLK	CLOCK (INT F F)
ELR	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS	
A_0 A_2	REQUEST LEVELS (OPEN COLLECTOR)
INT	INTERRUPT (ACT LOW) (OPEN COLLECTOR)
ENLG	ENABLE NEXT LEVEL GROUP

8216/8226
4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

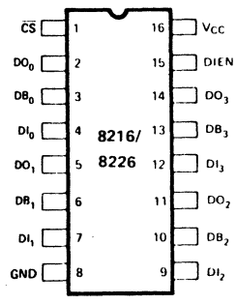
- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current — .25 mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU**
- **Three State Outputs**
- **Reduces System Package Count**

The 8216/8226 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

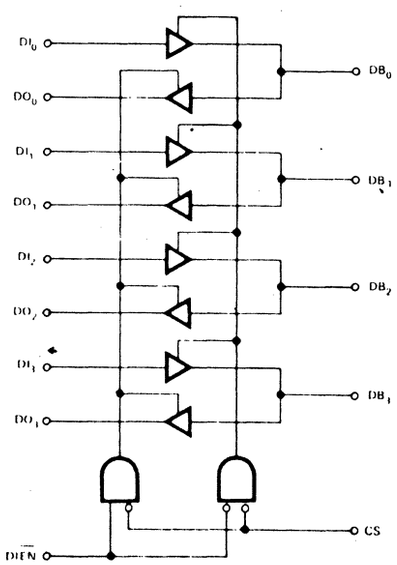
PIN CONFIGURATION



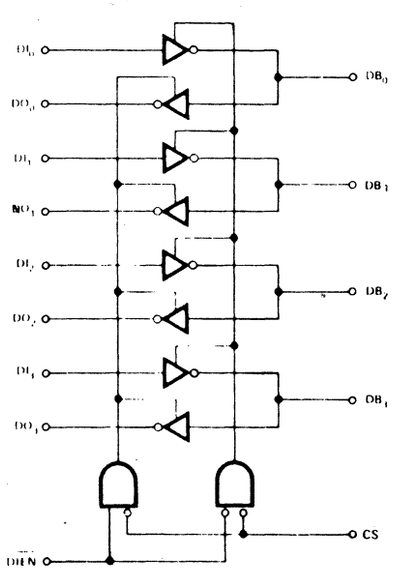
PIN NAMES

DB_0 DB_3	DATA BUS BI DIRECTIONAL
DI_0 DI_3	DATA INPUT
DO_0 DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
8216



LOGIC DIAGRAM
8226



8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

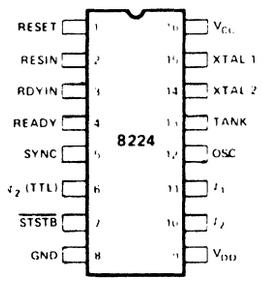
- Single Chip Clock Generator/Driver for 8080A CPU
- Power-Up Reset for CPU
- Ready Synchronizing Flip-Flop
- Advanced Status Strobe
- Oscillator Output for External System Timing
- Crystal Controlled for Stable System Operation
- Reduces System Package Count

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

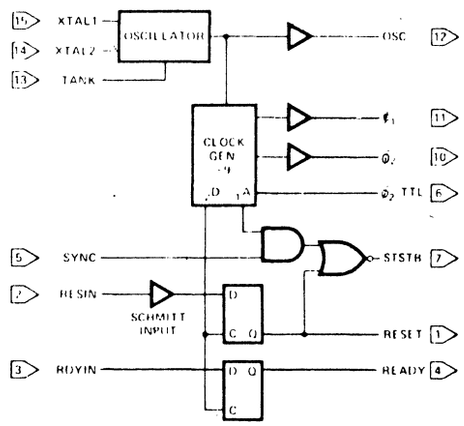
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
Φ1	8080 CLOCKS
Φ2	

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
Φ2 (TTL)	Φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

M8228/M8238
SYSTEM CONTROLLER AND BUS DRIVER FOR M8080A CPU

- Single Chip System Control for MCS-80 Systems
- Built-in Bi-Directional Bus Driver for Data Bus Isolation
- Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge
- M8238 has Advanced $\overline{IOW}$/$\overline{MEMW}$ for Large System Timing Control
- User Selected Single Level Interrupt Vector (RST 7)
- 28 Pin Dual In-Line Package
- Reduces System Package Count
- Full Military Temperature Range -55°C to +125°C
- ±10% Power Supply Tolerance

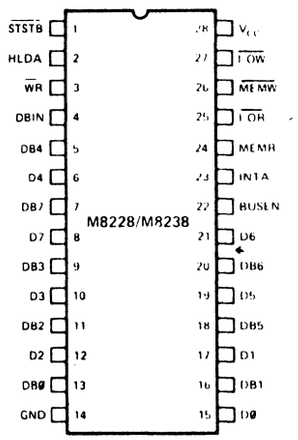
The M8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

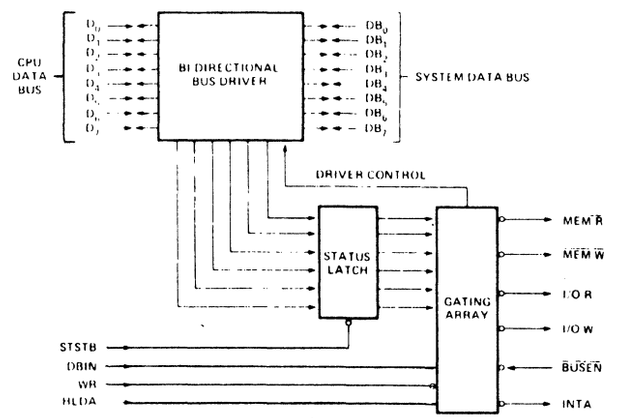
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The M8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the M8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The M8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



M8228/M8238 BLOCK DIAGRAM



PIN NAMES

D7 D0	DATA BUS (8080 SIDE)
DB7 DB0	DATA BUS (SYSTEM SIDE)
I OR	I O READ
I OW	I O WRITE
MEMR	MEMORY READ
MEMW	MEMORY WRITE
DBIN	DBIN (FROM 8080)

INTA	INTERRUPT ACKNOWLEDGE
HLDA	HLDA (FROM 8080)
WR	WR (FROM 8080)
BUSEN	BUS ENABLE INPUT
STSTB	STATUS STROBE (FROM 8224)
VCC	+5V
GND	0 VOLTS

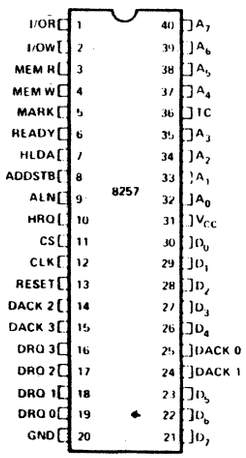
intel

8257
PROGRAMMABLE DMA CONTROLLER

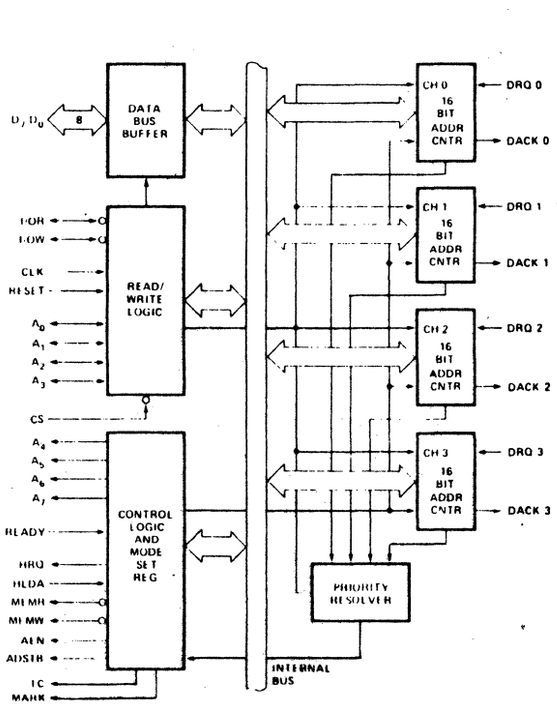
- **Four Channel DMA Controller**
- **Priority DMA Request Logic**
- **Channel Inhibit Logic**
- **Terminal Count and Modulo 128 Outputs**
- **Auto Load Mode**
- **Single TTL Clock**
- **Single +5V Supply**
- **Expandable**
- **40 Pin Dual-In-Line Package**

The 8257 is a four-channel Direct Memory Access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel Microcomputer Systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the 8080's HOLD function. The 8257 has priority logic that resolves the peripherals requests and issues a composite HOLD request to the 8080. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers and expansion to other 8257 devices for systems that require more than four channels of DMA controlled transfer. The 8257 represents a significant savings in component count for DMA-based 8080 systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7 D_0	DATA BUS
A_7 A_0	ADDRESS BUS
I/OR	I/O READ
I/OW	I/O WRITE
MEMR	MEMORY READ
MEMW	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3 DRQ_0	DMA REQUEST INPUT
$DACK_3$ $DACK_0$	DMA ACKNOWLEDGE OUT
CS	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: 510-227-8898

A Standard Microsystems Company

COM2601

Universal Synchronous Receiver/Transmitter

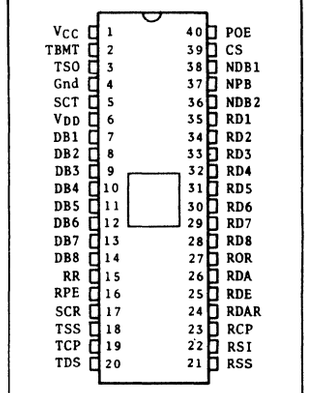
FEATURES

- **STR, BSC**—Bi-sync and interleaved bi-sync modes of operation
- **Fully Programmable**—data word length, parity mode, receiver sync character, transmitter sync character
- **Full or Half Duplex Operation**—can receive and transmit simultaneously at different baud rates
- **Fully Double Buffered**—eliminates need for precise external timing
- **Directly TTL Compatible**—no interface components required
- **Tri-State Data Outputs**—bus structure oriented
- **IBM Compatible**—internally generated SCR and SCT signals
- **High Speed Operation**—250K baud, 200ns strobes
- **Low Power**—300mW
- **Input Protected**—eliminates handling problems
- **Hermetic Dip Package**—easy board insertion

GENERAL DESCRIPTION

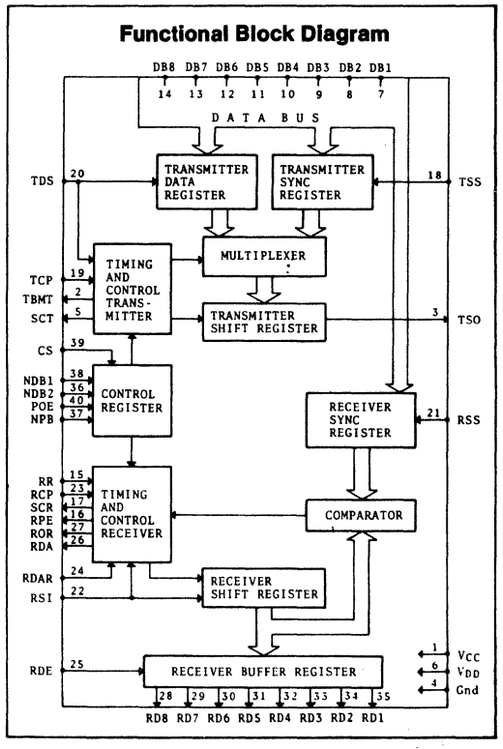
The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

Pin Configuration



PACKAGE: 40-Pin D.I.P.

Functional Block Diagram



SMC Microsystems Corporation
A Standard Microsystems Company

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	-25 V

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0-+70°C, V_{CC}=+5V±5%, V_{DD}=-12V±5%, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} =-100µA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	µA	RDE=V_{IL}, 0≤V_{OUT}≤+5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	R_{DE} = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			25	mA	
A.C. CHARACTERISTICS					T_A =+25°C
CLOCK FREQUENCY	DC		250	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			µs	RCP, TCP
Receiver reset	1			µs	RR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	TDS
Transmitter sync strobe	200			ns	TSS
Receiver sync strobe	200			ns	RSS
Receiver data available reset	200			ns	RDAR
INPUT SET-UP TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB,NDB2,NDB1,POE
INPUT HOLD TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB,NDB2,NDB1,POE
STROBE TO OUTPUT DELAY					Load =20pf+1 TTL input
Receive data enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

** Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low impedance to V_{CC}
   2) low impedance to GND
   3) high impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Symbol	Name	Function
1	V_{CC}	Power Supply	+5 volt Supply
2	TBMT	Transmitter Buffer Empty	This output is at a high-level when the transmitter data buffer register may be loaded with new data.
3	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register.
4	GND	Ground	Ground
5	SCT	Sync Character Transmitted	This output is set high when the character loaded into the transmitted shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed.
6	V_{DD}	Power Supply	-12 volt Supply
7-14	DB1-DB8	Data Bus Inputs	This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs should be at a high level* The LSB should always be placed on DB1.
15	RR	Receiver Reset	This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transitior of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register.
16	RPE	Receiver Parity Error	This output is a high-level if the received character parity bit does not agree with the selected parity.

**Parts date coded 7610 or later, no longer have this requirement.*

SMC Microsystems Corporation
A Standard Microsystems Company

Description of Pin Functions (cont.)

Pin No.	Symbol	Name	Function
17	SCR	Sync Character Received	This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character.
18	TSS	Transmitter Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register.
19	TCP	Transmitter Clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency.
20	TDS	Transmitter Data Buffer Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register.
21	RSS	Receiver Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register.
22	RSI	Receiver Serial Input	This input accepts the serial bit input stream.
23	RCP	Receiver Clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency.
24	RDAR	Receiver Data Available Reset	A high-level input resets the RDA output to a low-level.
25	RDE	Received Data Enable	A high-level input enables the outputs (RD8-RD1) of the receiver buffer register
26	RDA	Receiver Data Available	This output is at a high-level when an entire character has been received and transferred into the receiver buffer register.
27	ROR	Receiver Over-Run	This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register.
28-35	RD8-RD1	Receiver Data Output	These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
36, 38	NDB2, NDB1	Number of Data	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table:

NDB2	NDB1	data bits/character
L	L	5
L	H	6
H	L	7
H	H	8

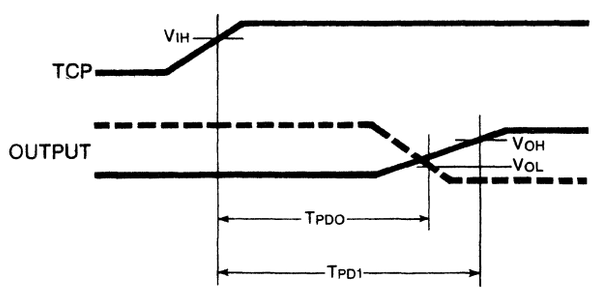
Description of Pin Functions (cont.)

Pin No.	Symbol	Name	Function
37	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE.
39	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level.
40	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity
		X=don't care

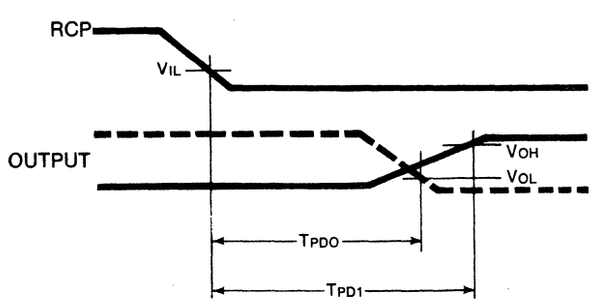
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

Transmitter



OUTPUT	TPDO	TPD1	UNITS
TBMT	NA	2.0	μs
SCT	1.0	1.5	μs
TSO	1.0	1.0	μs

Receiver



OUTPUT	TPDO	TPD1	UNITS
RDA	NA	1.0	μs
ROR	2.0	2.5	μs
RPE	2.0	2.5	μs
SCR	2.0	2.5	μs
RD1-RD8	2.5	2.5	μs

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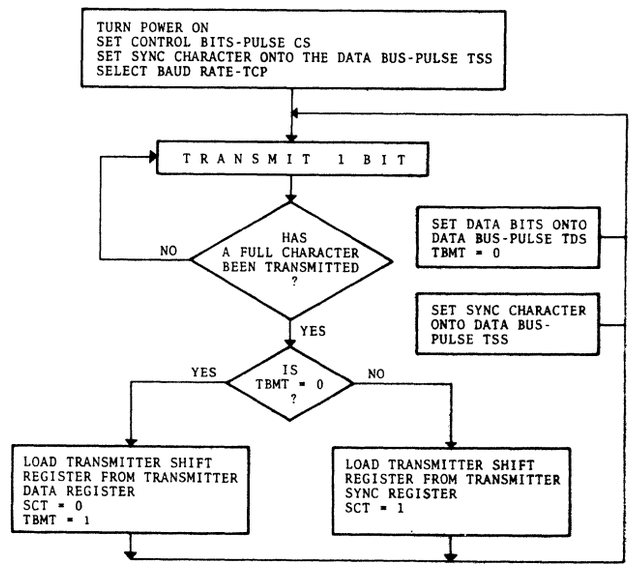
DESCRIPTION OF OPERATION - RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

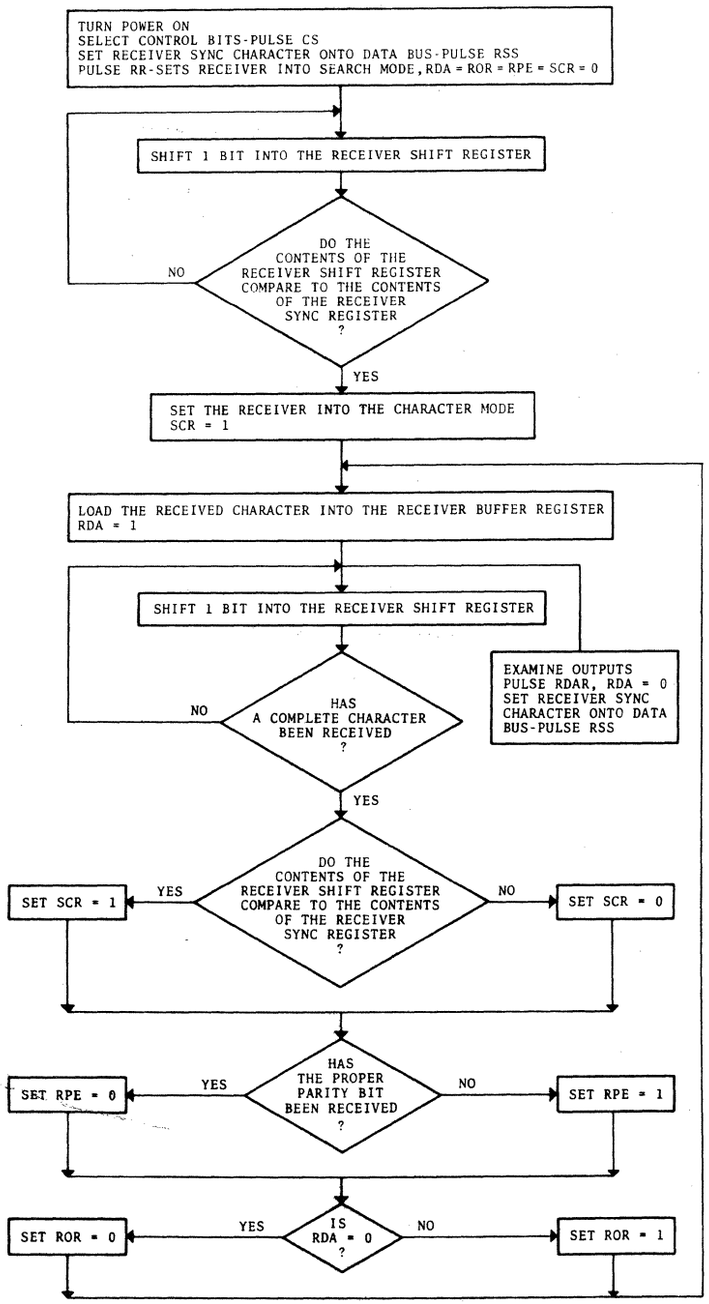
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data outputs levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

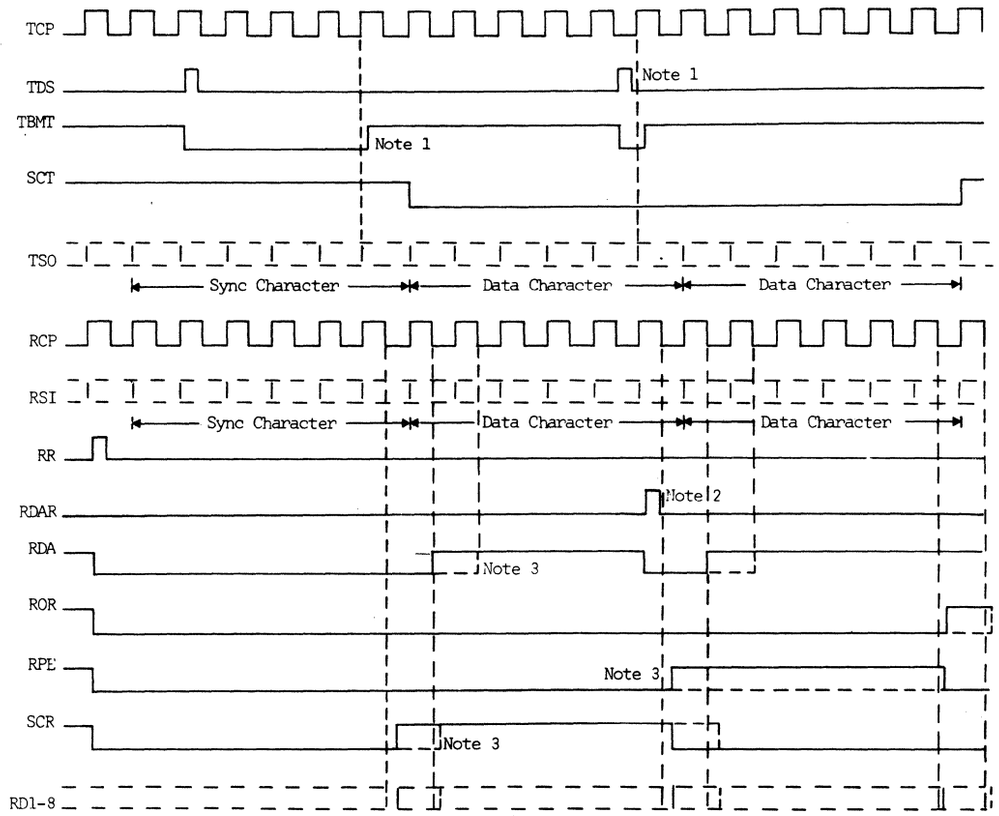
FLOW CHART - TRANSMITTER



FLOW CHART - RECEIVER



USRT TIMING DIAGRAM



NOTE 1
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

NOTE 3
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.

QUAD TIMER 553/554

SE553-BA,F • NE553-BA,F • SE554-BA,F • NE534-BA,F

FEATURES

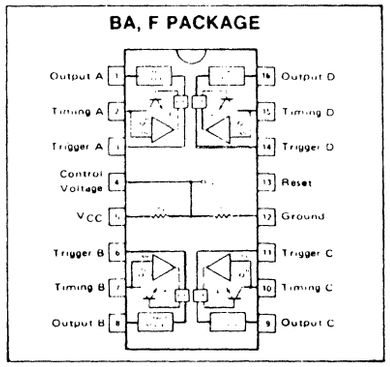
- 100mA OUTPUT CURRENT PER SECTION
- EDGE-TRIGGERED (NO COUPLING CAPACITOR)
- OUTPUT INDEPENDENT OF TRIGGER CONDITIONS
- WIDE SUPPLY VOLTAGE RANGE 4.5V TO 16V
- TIMER INTERVALS FROM MICROSECONDS TO HOURS

APPLICATIONS

SEQUENTIAL TIMING
TIME DELAY GENERATION
PRECISION TIMING
INDUSTRIAL CONTROLS
QUAD ONE-SHOT

PIN CONFIGURATION

BA, F PACKAGE



ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15V (Unless Otherwise Noted).

PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		18	27	mA
	V_{CC} = 15V, R_L = ∞		22	32	mA
Timing Accuracy	R = 2k to 100k, C = 1μF				
Initial Accuracy			1	4	%
Drift With Temperature			150		ppm/°C
Drift With Supply Voltage			0.03	0.1	%/V
Match Between Sections			0.2	0.5	%
Trigger Voltage		0.8	1.6	2.4	V
Trigger Current					
Logical "1"			10	100	nA
Logical "0"			50	100	μA
Threshold Voltage			0.63		xV_{CC}
Threshold Leakage			10	100	nA
Output Voltage (553)	I_L = 10mA		0.1	0.2	V
	I_L = 100mA		1.0	1.5	V
Output Voltage (554)	I_L = 10mA V_{CC} = 15V	13	14		V
	I_L = 100mA V_{CC} = 15V	12.5	13.5		V
Output Leakage			10	100	nA
Propagation Delay			1.0		μs
Risetime of Output	I_L = 100mA		100		ns
Falltime of Output	I_L = 100mA		100		ns

TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44, SN54LS42, SN7442A THRU SN7444A, SN74L42 THRU SN74L44, SN74LS42 4-LINE-TO-10-LINE DECODERS (1-OF-10)

TTL MSI

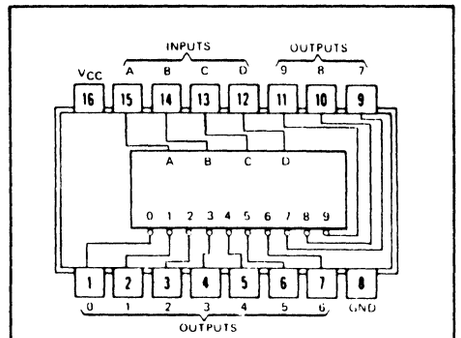
BULLETIN NO. DL-S 7611861, MARCH 1974 - REVISED OCTOBER 1976

'42A, 'L42, 'LS42 . . . BCD-TO-DECIMAL
'43A, 'L43 . . . EXCESS-3-TO-DECIMAL
'44A, 'L44 . . . EXCESS-3-GRAY-TO-DECIMAL

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
  4-Line-to-16-Line Decoders
  3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'L42, 'L43, 'L44	70 mW	49 ns
'LS42	35 mW	17 ns

SN5442A THRU SN5444A, SN54LS42 . . . J OR W PACKAGE
SN54L42 THRU SN54L44 . . . J PACKAGE
SN7442A THRU SN7444A,
SN74L42 THRU SN74L44, SN74LS42 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. D-c noise margins are typically one volt.

Series 54, 54L, and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, 74L, and 74LS circuits are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

NO.	'42A, 'L42, 'LS42 BCD INPUT D	C	B	A	'43A, 'L43 EXCESS-3-INPUT D	C	B	A	'44A, 'L44 EXCESS-3-GRAY INPUT D	C	B	A	ALL TYPES DECIMAL OUTPUT 0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L	H
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	I	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H

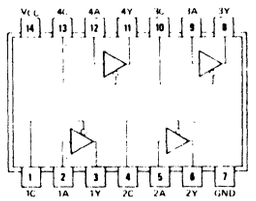
H = high level, L = low level

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

125

positive logic:
Y = A
Output is off (disabled) when C is high.

See page 6-33



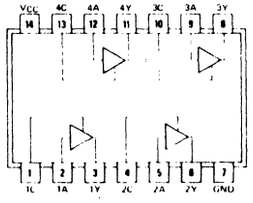
SN54125 (J, W) SN74125 (J, N)
SN54LS125 (J, W) SN74LS125 (J, N)

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

126

positive logic:
Y = A
Output is off (disabled) when C is low

See page 6-33



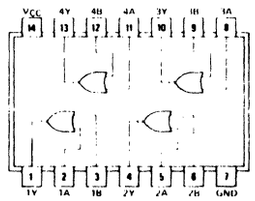
SN54126 (J, W) SN74126 (J, N)
SN54LS126 (J, W) SN74LS126 (J, N)

SN54128 . . . 75-OHM LINE DRIVER
SN74128 . . . 50-OHM LINE DRIVER

128

positive logic:
$Y = \overline{A+B}$

See page 6-22



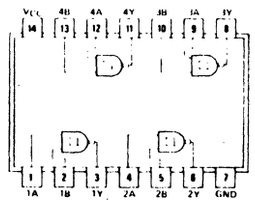
SN54128 (J, W) SN74128 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

132

positive logic:
$Y = \overline{AB}$

See page 6-14



SN54132 (J, W) SN74132 (J, N)
SN54LS132 (J, W) SN74LS132 (J, N)
SN54S132 (J, W) SN74S132 (J, N)

TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74L157, SN74LS157, SN74LS158, SN74S157, SN74S158
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611847, MARCH 1974 REVISED OCTOBER 1976

features

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

description

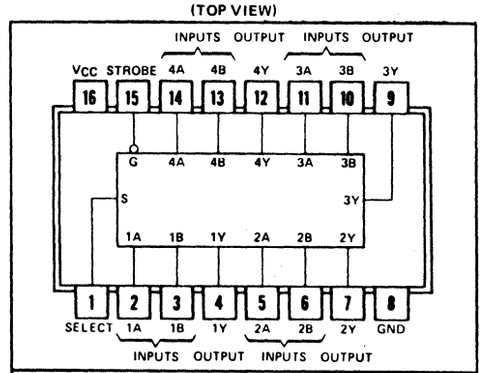
These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

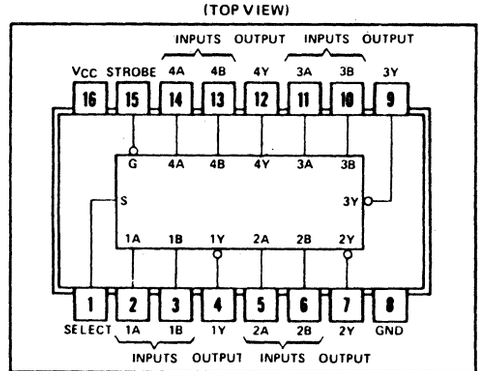
H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157 . . . J OR W PACKAGE
SN54L157 . . . J PACKAGE
SN74157, SN74L157, SN74LS157, SN74S157 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74LS158, SN74S158 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '157, 'L157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TTL MSI

TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

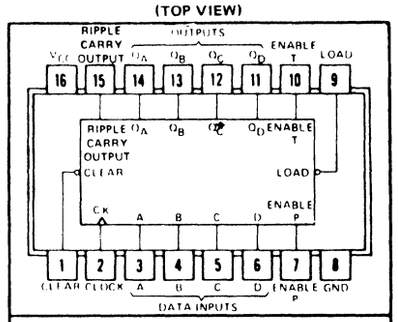
BULLETIN NO. DL-S 7611385, OCTOBER 1976

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS160A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74', 74LS', 74S' . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 or 'S163A or 'S162 should be avoided when the clock is low if the enable inputs are high at or before the transistion. This restriction is not applicable to the 'LS160A thru 'LS163A. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS160A thru 'LS163A are completely new designs. Compared to the original 'LS160 thru 'LS163, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL}.

TTL MSI

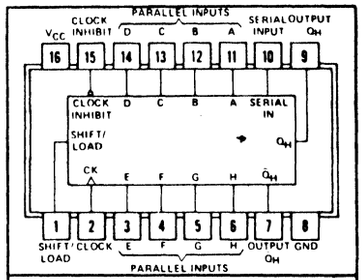
TYPES SN54165, SN54LS165, SN74165, SN74LS165 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7611375, OCTOBER 1976

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165	35 MHz	105 mW

SN54165, SN54LS165 . . . J OR W PACKAGE
SN74165, SN74LS165 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

description

The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

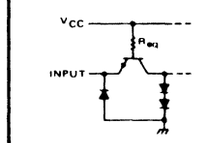
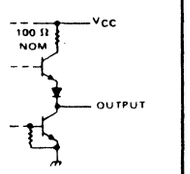
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

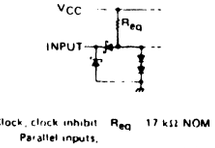
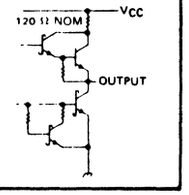
See explanation of function tables on page 3-8.

schematic of inputs and output

'165

EQUIVALENT OF EACH INPUT	TYPICAL OF BOTH OUTPUTS
	

'LS165

EQUIVALENT OF EACH INPUT	TYPICAL OF BOTH OUTPUTS
	

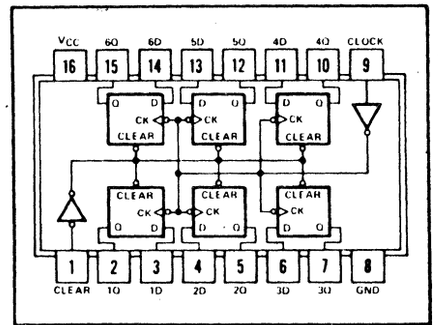
TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

BULLETIN NO. DL-S 7611803, DECEMBER 1972 REVISED OCTOBER 1976

'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

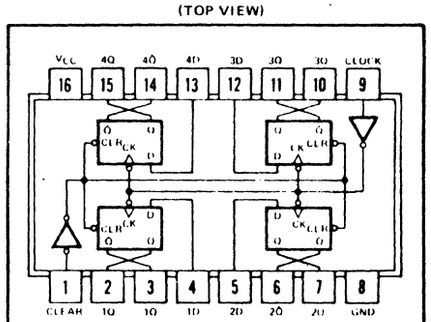
- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators

SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174, SN74LS174, SN74S174 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175, SN74LS175, SN74S175 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flops.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
† = '175, 'LS175, and 'S175 only

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

TTL MSI

TYPES SN54LS257A, SN54LS258A, SN54S257, SN54S258, SN74LS257A, SN74LS258A, SN74S257, SN74S258
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611734, OCTOBER 1976

- Three-State Outputs Interface Directly with System Bus
- 'LS257A and 'LS258A Offer Three Times the Sink-Current Capability of the Original 'LS257 and 'LS258
- Same Pin Assignments as SN54LS157, SN74LS157, SN54S157, SN74S157, and SN54LS158, SN74LS158, SN54S158, SN74S158
- Provides Bus Interface from Multiple Sources in High-Performance Systems

	AVERAGE PROPAGATION DELAY FROM DATA INPUT	TYPICAL POWER DISSIPATION
'LS257A	12 ns	60 mW
'LS258A	12 ns	60 mW
'S257	4.8 ns	320 mW
'S258	4 ns	280 mW

Off state (worst case)

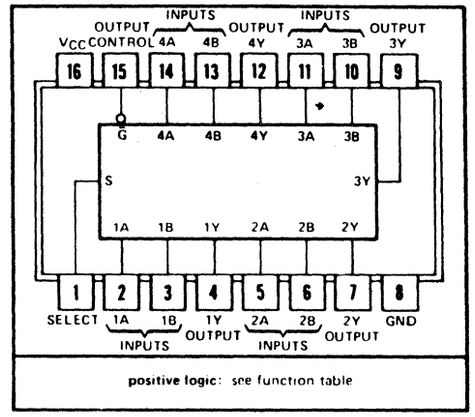
description

These Schottky-clamped high-performance multiplexers feature three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

This three state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

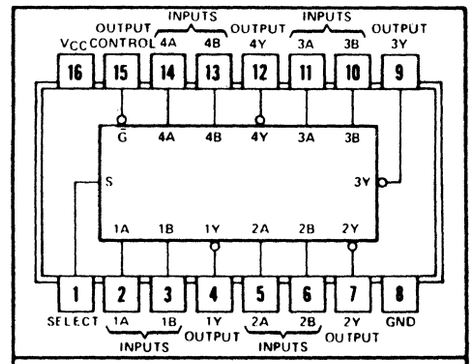
Series 54LS and 54S are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS and 74S are characterized for operation from 0°C to 70°C.

SN54LS257A, SN54S257 . . . J OR W PACKAGE
SN74LS257A, SN74S257 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS258A, SN54S258 . . . J OR W PACKAGE
SN74LS258A, SN74S258 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

FUNCTION TABLE

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	'LS257A 'S257	'LS258A 'S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

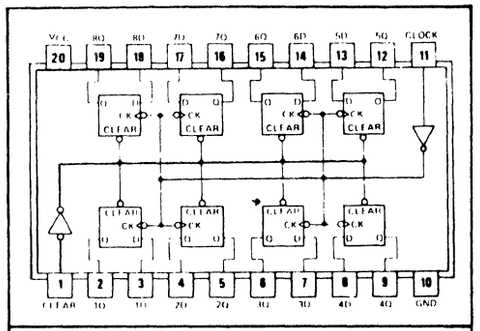
TTL MSI

TYPES SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

BULLETIN NO. DL-S 7612091, OCTOBER 1976

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54273, SN54LS273 . . . J PACKAGE
SN74273, SN74LS273 . . . J OR N PACKAGE



positive logic: see function table

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

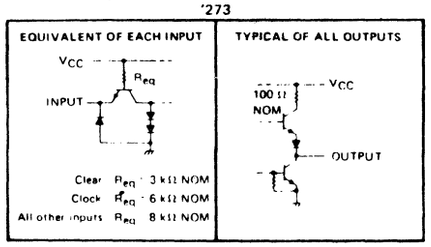
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

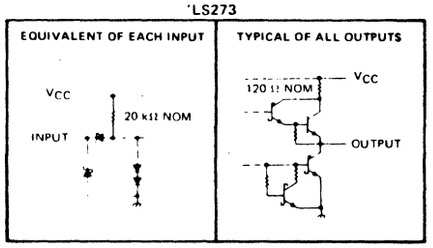
See explanation of function tables on page 3-8.

schematics of inputs and output

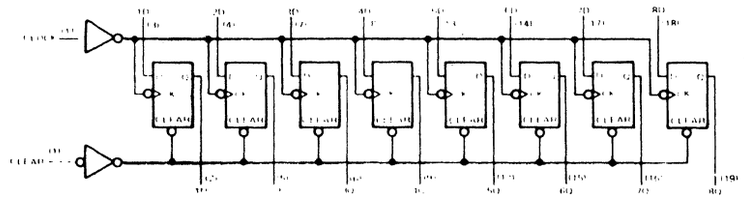
'273



'LS273

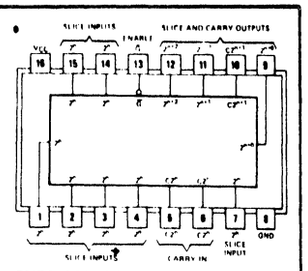


functional block diagram



7-BIT SLICE WALLACE TREES

275 3-STATE OUTPUTS

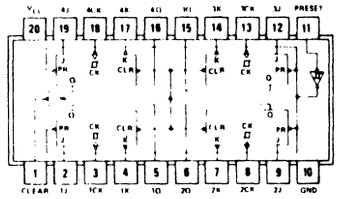


See page 7-391

SN54LS275 (J) SN74LS275 (J, N)
SN54S275 (J) SN74S275 (J, N)

QUAD J-$\overline{K}$ FLIP-FLOPS

276 SEPARATE CLOCKS
EDGE-TRIGGERING
COMMON DIRECT CLEAR

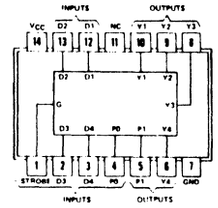


See page 7-401

SN54276 (J) SN74276 (J, N)

4-BIT CASCADEABLE PRIORITY REGISTERS

278 LATCHED DATA INPUTS
PRIORITY OUTPUT GATING



See page 7-403

SN54278 (J, W) SN74278 (J, N)

NC – No internal connection

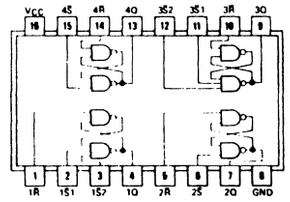
QUAD $\overline{S}$-$\overline{R}$ LATCHES

279 DIODE-CLAMPED INPUTS
TOTEM-POLE OUTPUTS

FUNCTION TABLE

INPUTS $\overline{S}$†	$\overline{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low



See page 6-60

SN54279 (J, W) SN74279 (J, N)
SN54LS279 (J, W) SN74LS279 (J, N)

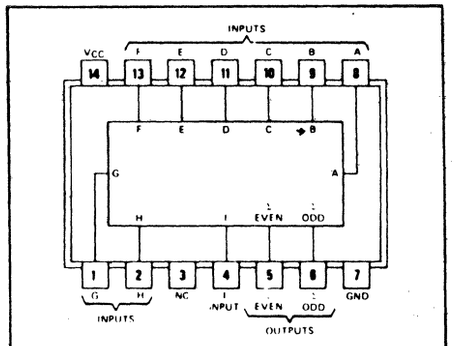
TTL
MSI

TYPES SN54LS280, SN54S280, SN74LS280, SN74S280
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-S 7611829, DECEMBER 1972 – REVISED OCTOBER 1976

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns for 'S280 and 33 ns for 'LS280
- Typical Power Dissipation:
  'LS280 . . . 80 mW
  'S280 . . . 335 mW

SN54LS280, SN54S280 . . . J OR W PACKAGE
SN74LS280, SN74S280 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

NC = No internal connection

description

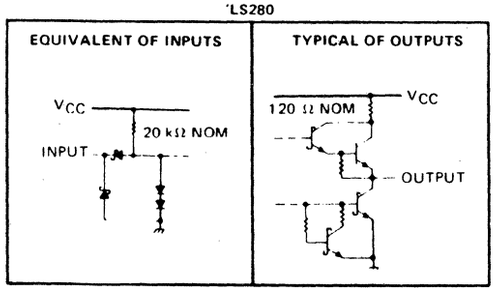
These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading as shown under typical application data.

Series 54LS/74LS and Series 54S/74S parity generators/checkers offer the designer a trade off between reduced power consumption and high performance. These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'LS280 and 'S280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'LS280 and 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'LS280's and 'S280's are mixed with existing '180's.

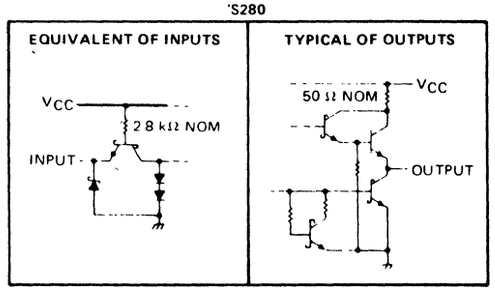
These devices are fully compatible with most other TTL and DTL circuits. All 'LS280 and 'S280 inputs are buffered to lower the drive requirements to one Series 54LS/74LS or Series 54S/74S standard load, respectively.

schematics of inputs and outputs

'LS280



'S280



TTL
MSI

TYPES SN54283, SN54LS283, SN54S283, SN74283, SN74LS283, SN74S283
4-BIT BINARY FULL ADDERS WITH FAST CARRY

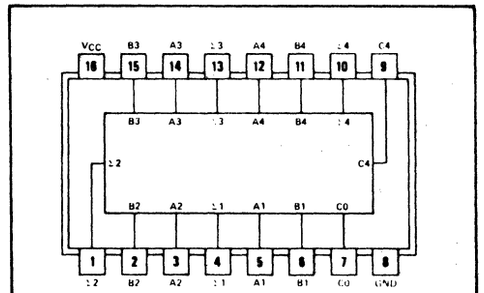
BULLETIN NO. DL-S 7611832, OCTOBER 1976

- Full-Carry Look-Ahead Across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

TYPICAL ADD TIMES

TYPE	TWO 8-BIT WORDS	TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER ADDER
'283	23ns	43ns	310 mW
'LS283	25ns	45ns	95 mW
'S283	15ns	30ns	510 mW

SN54283, SN54LS283 . . . J OR W PACKAGE
SN54S283 . . . J PACKAGE
SN74283, SN74LS283, SN74S283 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

The '283 and 'LS283 adders are electrically and functionally identical to the '83A and 'LS283, respectively; only the arrangement of the terminals has been changed. The 'S283 high performance versions are also functionally identical.

These improved full adders perform the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look-ahead across all four bits generating the carry term in ten nanoseconds, typically, for the '283 and 'LS283, and 7.5 nanoseconds for the 'S283. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full temperature range of −55°C to 125°C. Series 74, Series 74LS, and Series 74S circuits are characterized for 0°C to 70°C operation.

FUNCTION TABLE

INPUT				OUTPUT: WHEN C0 = L			OUTPUT: WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

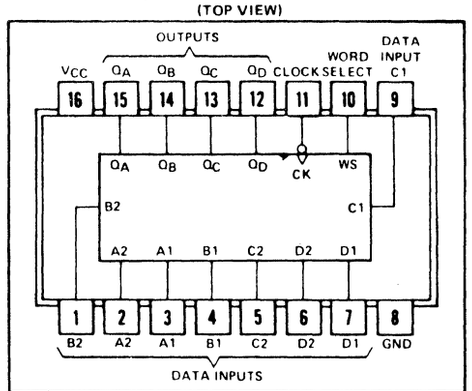
NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

TYPES SN54298, SN54LS298, SN74298, SN74LS298
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

BULLETIN NO. DL-S 7611747, MARCH 1974 REVISED OCTOBER 1976

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
  Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability
  Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities

SN54298, SN54LS298 . . . J OR W PACKAGE
SN74298, SN74LS298 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54157/SN74157 or SN54LS157/SN74LS157 and SN54175/SN74175 or SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applies to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

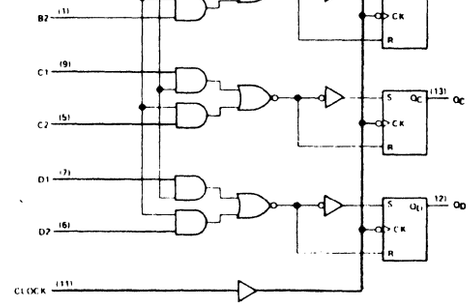
Typical power dissipation is 195 milliwatts for the '298 and 65 milliwatts for the 'LS298. SN54298 and SN54LS298 are characterized for operation over the full military temperature range of −55°C to 125°C; SN74298 and SN74LS298 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	˙H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady state input at A1, A2, etc
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input

functional block diagram

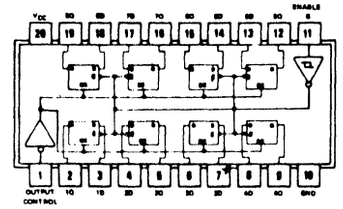


↓ . . . Dynamic input activated by a transition from a high level to a low level

OCTAL D-TYPE LATCHES

363 TRANSPARENT LATCH
3-STATE OUTPUT
COMMON OUTPUT CONTROL
COMMON ENABLE

See page 7-467

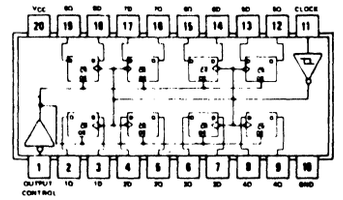


SN54LS363 (J) SN74LS363 (J, N)

OCTAL D-TYPE FLIP-FLOPS

364 COMMON CLOCK
COMMON OUTPUT CONTROL
3-STATE OUTPUTS

See page 7-467

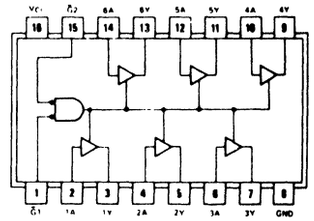


SN54LS364 (J) SN74LS364 (J, N)

HEX BUS DRIVERS

365 3-STATE OUTPUTS
NONINVERTED DATA OUTPUTS
GATED ENABLE INPUTS

See page 6-36

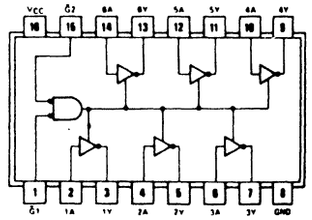


SN54365A (J, W) SN74365A (J, N)
SN54LS365 (J, W) SN74LS365 (J, N)

HEX BUS DRIVERS

366 INVERTED DATA OUTPUT
GATED ENABLE INPUTS
3-STATE OUTPUTS

See page 6-36



SN54366A (J, W) SN74366A (J, N)
SN54LS366 (J, W) SN74LS366 (J, N)

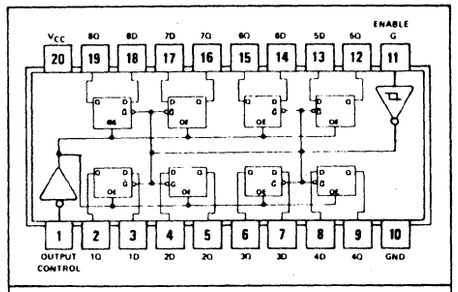
TTL
MSI

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7612350, OCTOBER 1976

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)
- SN54LS363 and SN74LS364 Are Similar But Have Higher V_{OH} For MOS Interface

SN54LS373, SN54S373 . . . J PACKAGE
SN74LS373, SN74S373 . . . J OR N PACKAGE
(TOP VIEW)

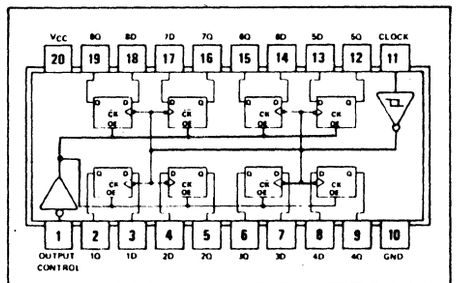


logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS374, SN54S374 . . . J PACKAGE
SN74LS374, SN74S374 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

'LS374, 'S374
FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

See explanation of function tables on page 3-8

description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

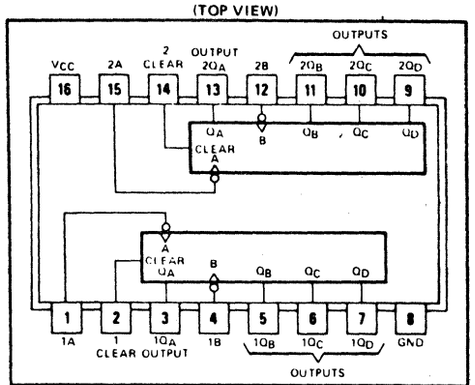
TTL

TYPES SN54390, SN54LS390, SN54393, SN54LS393, SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

BULLETIN NO. DL-S 7612099, OCTOBER 1976

- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390. . .Individual Clocks for A and B Flip-Flops Provide Dual ÷2 and ÷5 Counters
- '393, 'LS393. . .Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390, SN74LS390 . . . J OR N PACKAGE
(TOP VIEW)



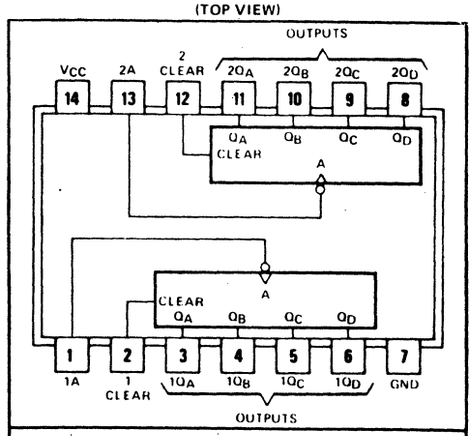
positive logic: High input to clear resets all four outputs low

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

SN54393, SN54LS393 . . . J OR W PACKAGE
SN74393, SN54LS393 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low

TTL MEMORIES

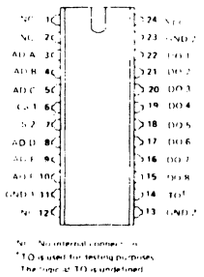
SERIES 54/74, 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

BULLETIN NO. DL-S 7512258, MAY 1975

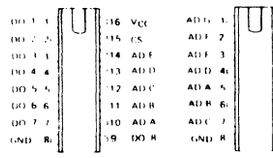
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE	OUTPUT	TYPICAL ACCESS TIME (ns)	
–55 C to 125 C	0 C to 70 C	(ORGANIZATION)	CONFIGURATION	FROM ADDRESS	FROM CHIP SELECT
SN54186(J, W)	SN74186(J, N)	512 bits (64 W x 8 B)	open collector	50	55
SN54188A(J, W)	SN74188A(J,N)	256 bits (32 W x 8 B)	open collector	30	34
SN54S188(J, W)	SN74S188(J, N)		open-collector	25	12
SN54S288(J, W)	SN74S288(J, N)		three-state	25	12
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42	15
SN54S387(J, W)	SN74S387(J, N)		open-collector	42	15
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50	20
SN54S471(J)	SN74S471(J, N)		three-state	50	20
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55	20
SN54S473(J)	SN74S473(J, N)		open-collector	55	20

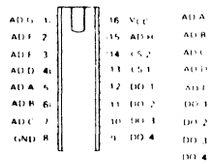
512 BITS (64 WORDS BY 8 BITS) '186



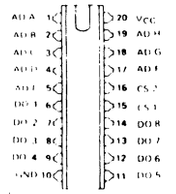
256 BITS (32 WORDS BY 8 BITS) '188A, 'S188, 'S288



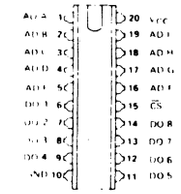
1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387



2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471



4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473



Pin assignments for all of these memories are the same for all packages

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. The Schottky-clamped versions of these PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit PROM's can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch.

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

A low level at the chip-select input(s) enables each PROM except the '186, which is enabled by a high level at both chip-select inputs. The opposite level at any chip-select input causes the outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

Proprietary

DM71/DM81LS95,LS96,LS97,LS98

TRI-STATE Octal Buffers

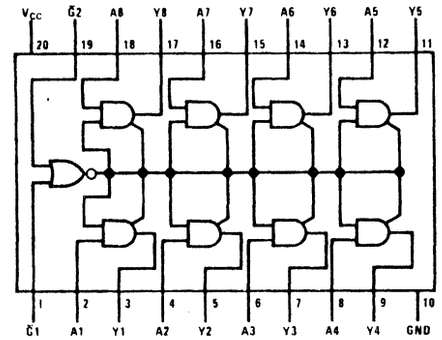
General Description

These devices provide eight, two-input buffers in each package. All employ the newest low power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all eight TRI-STATE enable lines are common, with access through a 2-input NOR gate. On the 97 and 98 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM70/8095, 96, 97, and 98 TRI-STATE hex buffers.

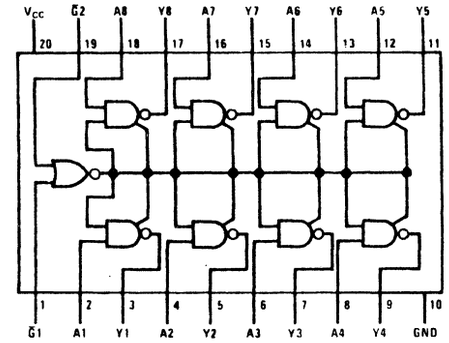
Features

- Octal versions of popular DM8095, 8096, 8097, 8098
- Typical power dissipation
  - LS95, LS97 — 80 mW
  - LS96, LS98 — 65 mW
- Typical propagation delay
  - LS95, LS97 — 13 ns
  - LS96, LS98 — 10 ns
- Low power-Schottky, TRI-STATE technology

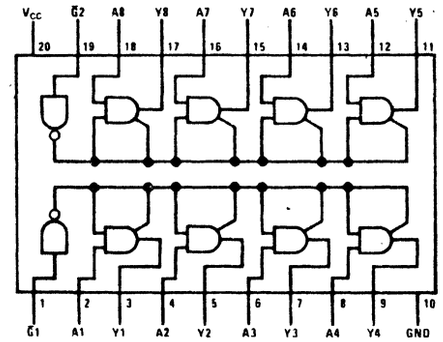
Connection Diagrams



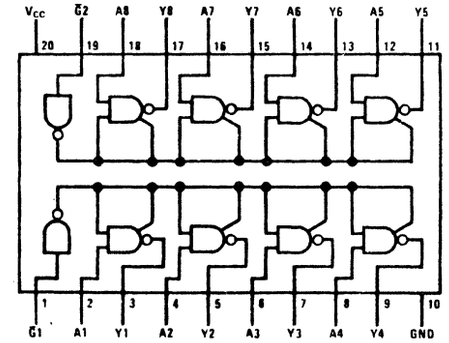
71LS95/81LS95(N)



71LS96/81LS96(N)



71LS97/81LS97(N)



71LS98/81LS98(N)

Truth Tables

LS95

INPUTS			OUTPUT
G̅1	G̅2	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

LS96

INPUTS			OUTPUT
G̅1	G̅2	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

LS97

INPUTS		OUTPUT
G̅	A	Y
H	X	Z
L	H	H
L	L	L

LS98

INPUTS		OUTPUT
G̅	A	Y
H	X	Z
L	H	L
L	L	H

TTL/MSI 9334
8-BIT ADDRESSABLE LATCH

DESCRIPTION — The TTL/MSI 9334 is a high speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active level LOW common clear for resetting all latches, as well as, an active level LOW enable. The 9334 is compatible with all members of Fairchild's TTL family.

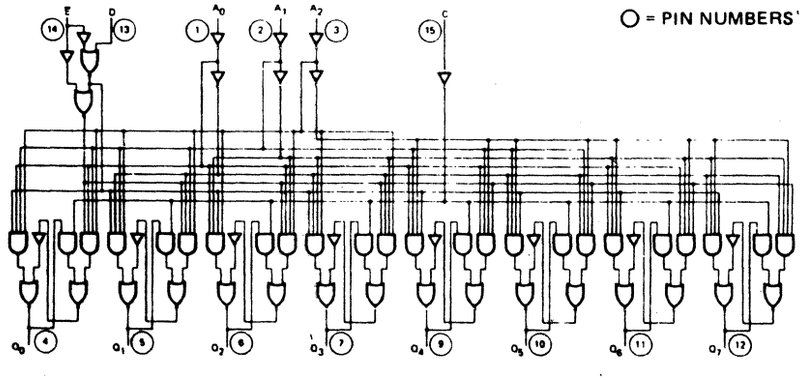
- **SERIAL TO PARALLEL CAPABILITY**
- **8 BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**

PIN NAMES

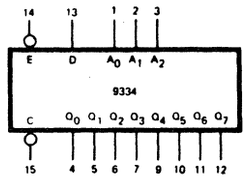
		LOADING (Note a)
A_0, A_1, A_2	Address Inputs	1 U.L.
D	Data Input	1 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	1 U.L.
Q_0 to Q_7	Parallel Latch Outputs (Note b)	6 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 6 U.L. is the output LOW drive factor and 18 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

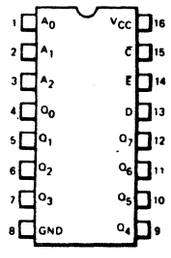


LOGIC SYMBOL

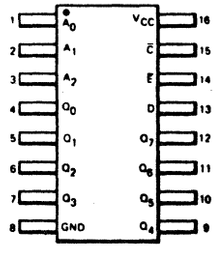


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Series 54/74

DM7130/DM8130 10-bit comparator
DM7160/DM8160 6-bit comparator

general decription

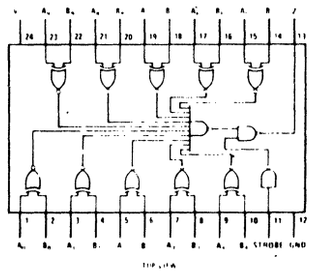
The DM7130/DM8130 and DM7160/DM8160 comparators determine equality or non equality between two binary words. The DM7130/DM8130 compares two ten bit words while the DM7160/DM8160 compares two six bit words. A strobe over ride is provided on both devices which when taken to a logical "1" will force the output to a logical "1".

features

- Series 54/74 compatible
- 20 ns typical compare delay
- Typical power dissipation
  - DM7130/DM8130 240 mW
  - DM7160/DM8160 205 mW
- Open collector outputs for expandability

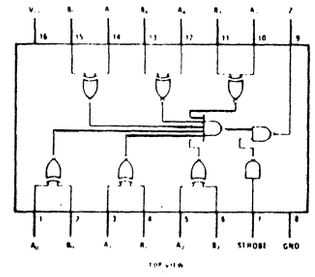
logic and connection diagrams

Dual-In-Line and Flat Package



DM7130 DM8130

Dual-In-Line and Flat Package



DM7160/DM8160

truth table

CONDITION	$\overline{\text{STROBE}}$ S	Z
A B, A / B	1	1
A B	0	1
A / B	0	0

For DM7130 DM8130

(A) A_n A_0
(B) B_n B_0

$$Z = \overline{S} \cdot [X_0 \cdot X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot X_5 \cdot X_6 \cdot X_7 \cdot X_8 \cdot X_9]$$

For DM7160/DM8160

(A) A_n A_0
(B) B_n B_0

$$Z = \overline{S} \cdot [X_0 \cdot X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot X_5]$$

where

X_0 $A_0 B_0 + \overline{A_0} \overline{B_0}$ X_1 $A_1 B_1 + \overline{A_1} \overline{B_1}$

INSTALLATION PROCEDURE

1. GENERAL UNPACKING AND INSPECTION

The AES-PLUS Text Editor is shipped in two boxes containing the CRT console and the printing unit. The CRT console is packaged in two moulded Styrofoam blocks, encasing both ends and fitted in a corrugated cardboard box. The printing unit is packaged in its original box, where it is bolted on a press-wood board and contained in a dual box (inner and outer) arrangement.

ONCE UNPACKING IS COMPLETED

- Place the unit as required at the designated customer location.
- Inspect CRT surface for cracks, scratches or other possible damages that might have resulted from shipment.
- Check all hardware for loose nuts, frayed cables, etc...
- Make sure that all printed circuit boards are firmly inserted in their edge connector.
- Check all connectors, fuses and relays for proper installation.

ALL PACKAGING MATERIAL SHOULD BE BROUGHT BACK TO AES DATA

2. INSTALLATION

CAUTION

POWER SHOULD NOT BE APPLIED BEFORE THE FOLLOWING PROCEDURES HAVE BEEN COMPLETED

- Connect the printer flat cable to the proper socket in the rear of the CRT console and the printer.
- Connect the printer power cable to the printer power supply socket located behind the CRT console.
- Connect the AC power cord to the CRT console and to the appropriate wall socket.

3. INITIAL POWER TURN-ON

After having entirely inspected the system, turn power ON as follows:

- Press the white ON-OFF switch, located in the rear of the CRT console, to the ON position.
- A continuous bell tone is heard at this moment; insert a program diskette in the upper disc drive and wait for 30 seconds.
- The control line should appear on the video display. Set the brightness and volume controls located below the disc drives.
- Verify that the printer operates by printing properly a small text from the screen.
- Set left and right margins.
- Insert a diskette in either disc drive and check all EDIT and FILE functions.
- Allow the operator to exercise the system with most of its functions.

NOTE:
If any malfunction occurs during the above procedures, refer to the MAINTENANCE section of the manual.

MAINTENANCE & DIAGNOSTIC

A) INTRODUCTION

Maintenance of the AES-PLUS Text Editor consists mainly of a system check performed on a GO-NO-GO Test Station. This system check is almost done automatically by a diagnostic program loaded into an 8K EROM Memory Board and two formatted mini-diskettes. A power supply adjustment procedure completes the system check.

B) DIAGNOSTIC PROCEDURES

The Diagnostic Program is contained in an 8K EROM Memory printed circuit board. This memory board is inserted in the lower slot of the test station and two formatted diskettes in each disk drive. At this point, it is assumed that the C.P.U. Board and the printer are operating properly.

1. System Diagnostic

The EROM Progam will test the system automatically and operator intervention will be required on a few tests only. The program is divided into twelve sub-programs:

- The Microprocessor Test
- The C.P.U. Test
- RAM Test (Instruction Memory 0-16K)
- Switch Packs Test
- RAM Test (Instruction Memory 16-32K)
- Printer Test & Exerciser
- Keyboard Test & Exerciser
- Disk Test & Exerciser
- Video Test
- Video RAM Test
- Video Format & Scroll Test (Page Ø)
- Video RAM Test (Page 1)

The tests requiring operator intervention are tests D, G, H, I and J. Proceed by:

- Turning the system power ON and check that all connections are made properly (Oume power cord ...).
- Insert paper in printer.
- Set the switch pack on the video board to the desired configuration. (All configuration have not been defined yet so place Parity switch 8 of switch pack 1 in the OFF position).
- Press the RESET button to start program execution.

1.1 The Microprocessor Test

Result: A bell sound is heard if the microprocessor passes the test.

If a failure occurs, the bell stays on and a RESET should be executed by the operator.

1.2 THE C.P.U. Tests

Result: ERROR 0 is printed if no failure occurs
ERROR 1 is printed if failure occurs.

This test verifies state of Bootstrap flag.

Result: Will print ERROR 2 or 3, 4 or 5

This test verifies the instruction memory READ/WRITE in the first 4K.

Result: ERROR 6 First address byte of channel Ø,1
ERROR 7 Second address byte of channel Ø,1

ERROR 8 First byte of Terminal count Ø & 1
ERROR 9 Second byte of Terminal count Ø & 1

*During the printing of results, the DMA channel number is included.

1.3 The RAM Tests

1. Result: **PASSED** is printed for first 16K

   If failure occurs, the original data byte is printed with the stored data byte accompanied by the error address.

   Original byte: XXXXXXXX
   Stored byte : XXXXXXXX
   Error Address: XXXXXXXXXXXXXXXX

2. Result: The same as above applies for the second 16K, the 8K of Video Page Ø and the 8K of Video Page 1.

1.4 Switch Pack Test

The automatic diagnostic stops and then the operator must place all switches in the ON position and press the EXEC key.

Result: **PASSED** is then printed.

The switches are then placed in the OFF position.

Result: **PASSED** is then printed.

If error occurs, **FAILED** is printed. The failed switch pack number (Ø or 1) is also printed followed by the switch pack binary configuration.

1.5 The Printer Test

Result: The printer prints the following string of characters

AZBYCXDWEVFUGTHSIRJOKPLOMN

abcdefghijklmnopqrstuvwxyz

0918273645

The mechanical functions of paper feed, carriage feed, ribbon and character strobes are also tested. These functions require the operator's observation since no printout is issued.

1.6 The Keyboard Test & Exerciser

This test requires the operator's assistance since characters have to be keyed from the keyboard. The operator should key several characters in upper and lower case (twelve per line as shown in the GO-NO-GO Test output).

The REPT key should be pressed simultaneously with a character so as to verify repeated interrupts. The underline is also verified by pressing a character with the SCROLL key ON.

To allow the diagnostic to continue, the operator should press the STOP key.

1.7 The Disk Drive Test & Exerciser

Result: **PASSED** is printed if no failure occurs.

ERROR 1 - if Drive Ø not ready.
ERROR 2 - if Drive 1 not ready.
ERROR 3 - if Track flag false.
ERROR 4 - if Track unaccessible.
ERROR 5 - if READ/WRITE error occurs.

1.8 The Video Test

The test consists of questions asked to the operator via the printer. These questions only require a YES or a NO given via the keyboard by a CRTL+Y for a YES and CRTL+N for NO.

Result: IS VIDEO OFF ?
IS PICTURE STABLE ?
IS V IN TOP LEFT CORNER OF SCREEN ?
IS IT A VALID CHARACTER ?
IS IT ! UPSIDE DOWN ?

The answers typed by the operator appear next to each question. If an error is generated, the error number appears beside the answer.

The following list describes the type of video error that may be incurred:

ERROR NO:	DESCRIPTION
1	The video cannot be turned off.
2	Fault ahead of scan line logic.
3	Fault after scan line logic.
4	"V" cannot be written in ADDRESS 8ØØØH.
5	"V" is written in address ØØØØH instead of 8ØØØH.
6	Video screen cannot be cleared.
7	ØØH cannot be written in 8ØØØH.
8	Non-valid character; video output or scan line counter fault.
9	Possible video output failure.
10	Video memory failure.
11	Memory output driver fault.
12	Memory output latch & underline logic.
13	Memory or output logic failure.
14	Memory output driver.
15	Half-tone Bit XOR and underline.

1.9 The Video Format & Scroll Test (Page Ø)

Result: The eight formats are verified and assigned an error number.

ERROR NUMBER			
1	FORMAT	256	FAILED
2	FORMAT	208	FAILED
3	FORMAT	160	FAILED
4	FORMAT	144	FAILED
5	FORMAT	128	FAILED
6	FORMAT	112	FAILED
7	FORMAT	96	FAILED
8	FORMAT	80	FAILED

The scroll test is performed with the aid of the operator. When a Ø appears at the left corner of the video screen, the operator must scroll right or left by using SCROLL + ⟵ or SCROLL + ⟶ . The format at this time is 256:

COLUMN Ø COLUMN 255
LINE 1

This test is ended by pressing the STOP key. To perform the UP and DOWN scroll, press SCROLL + ↑ or SCROLL + ↓ . The format becomes at this time 80:

LINE 2 Ø 80 COLUMN 79

LINE 101 101

This test is also ended by pressing the STOP Key,

This same test should also be performed on video Page 1.

EXAMPLE OF A.E.S. 103 GO-NO-GO TEST PRINTOUT

```
Microprocessor Test      **PASSED**
C.P.U. TESTS     **PASSED**
BOOTSTRAP CHECKSUM =      01010000
RAM TEST     **PASSED**

SWITCHES TEST

SET SWITCH PACKS ON      **PASSED**
SET SWITCH PACKS OFF      **PASSED**

RAM TEST     **PASSED**

PRINTER TEST & EXERCISER

AZBYCXDWEVFUGTHSIRJQKPLOMN

abcdefghijklmnopqrstuvwxyz

0918273645
```

C) Power Supply Adjustment Procedures

All power supply adjustments include an output voltage adjustment, an overvoltage protection and current limiting check.

Equipment required:

- Oscilloscope.
- Digital Voltmeter.
- A five ampere fuse shunted by a 30 ohm resistor.
- A 1 kilohm resistor with leads.

Before applying power to the unit, make sure all regulator input fuses have been removed from their P.C. board holders.

1. Synchronizing Oscillator Check

With the oscilloscope, place probe at the emitter of Q2 and check for the presence of pulses. The pulses should have a period of 33 microseconds and an amplitude of approximately 8 volts.

2. +5 Volt Adjust

- Insert fuse with 30 ohm resistor in the fuse holder situated ahead of the +5 volt pass transistor Q1.
- Check presence of sync signal at capacitors C3 or C4
- To verify the overvoltage protection circuit, apply the 1K resistor across the +27 volt and input 5 of reference amplifier A1. Check the +5 volt output response with the D.V.M.
- For the current limiting check, use same resistor and apply between the base of Q2 and ground. Check waveform at base of Q1; waveform should widen due to simulated higher load demand.
- Readjust potentiometer R8 for a 5 volt reading on D.V.M.

3. + 15 Volt Adjust

- The procedure for this adjustment is the same as described for the + 5 volt.

4. The - 15 Volt Adjust.

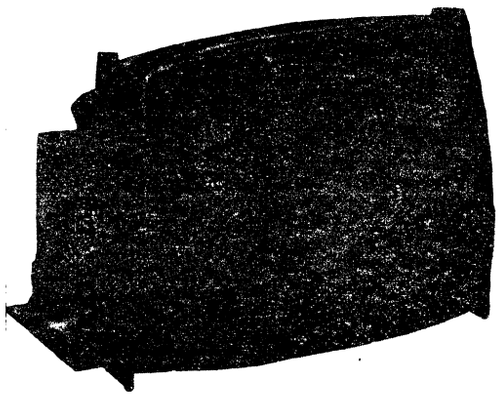
- Insert fuse with 30 ohm resistor.
- Place 1K resistor across + 5 volts and arm of potentiometer R100. Check output response with D.V.M.
- For current limiting check, place 1K resistor across base of Q13 and -27 volt source. Check response with oscilloscope at base of series-pass transistor Q11.

5. The + 12 Volt Adjust.

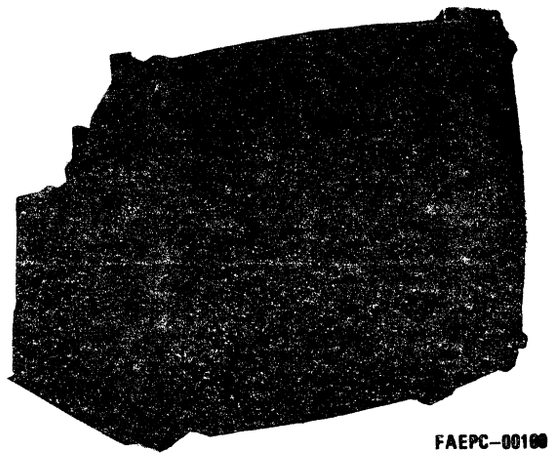
The procedure for this adjustment is the same as described for the + 5 volt adjustment procedures.

6. The - 12 Volt Adjust

This regulator consists of an integrated circuit and its 12 volt output is simply adjusted by potentiometer R116.



Model M3000 (12"–CRT)



FAEPC–00100

Model M4000 (15"–CRT)

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

TABLE OF CONTENTS

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

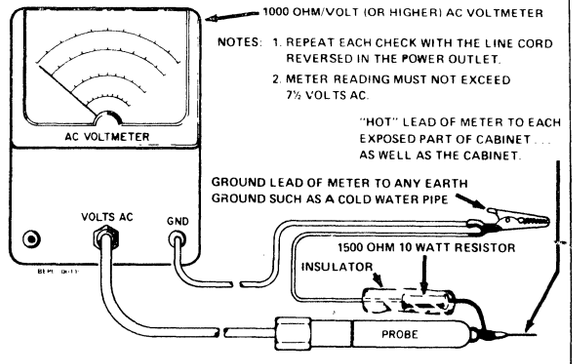
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

ELECTRICAL SPECIFICATIONS *

	MODEL M3000	MODEL M4000
PICTURE TUBE:	12" measured diagonally (305 mm); 74 sq. in. viewing area (477 sq. cm); 110° deflection angle; integral implosion protection; P4 phosphor standard	15" measured diagonally (381 mm); 100 sq. in. viewing area (645 sq. cm); 110° deflection angle; integral implosion protection; P4 phosphor standard
POWER INPUT:	115/230V AC, 60 watts (nominal), or 70V DC	
FUSES:	0.8 Amp Slo-Blo	0.8 Amp Slo-Blo
LOW VOLTAGE POWER SUPPLY:	Electronically regulated over AC inputs from 107V to 135V, or 214V to 270V	
INPUT SIGNALS:	COMPOSITE VIDEO INPUT: 0.5V to 2.5V composite P-P, sync negative (input impedance: 75 ohms terminated, 12K ohms unterminated), or TTL SEPARATE HORIZONTAL, VERTICAL, VIDEO: 2.5V to 5.0V P-P, video drive, sync positive at input (input impedance: 75 ohms to 250 ohms video termination, > 2K ohms vertical and horizontal)	
PULSE RISE TIME (TYPICAL):	30V rise in less than 20 nSec	
RESOLUTION (TYPICAL):	800 lines center, 600 lines corners	
VIDEO RESPONSE (TYPICAL):	Within −3 dB, 10 Hz to 22 MHz	
LINEARITY:	Within 2% as measured with standard EIA ball chart and dot pattern	
HIGH VOLTAGE:	14kV nominal at 20 uAmp beam current	17kV nominal at 20 uAmp beam current
HORIZONTAL RETRACE TIME:	11.0 uSec maximum at 15.75 kHz	
SCANNING FREQUENCY:	Horizontal: 15,750 Hz ±500 Hz; Vertical: 50/60 Hz	
ENVIRONMENT:	Operating temperature: 0°C to 50°C Storage temperature: −40°C to +65°C Operating altitude: 10,000 feet maximum (3048 meters) Designed to comply with applicable DHEW rules on X-Radiation Designed to enable listing under UL Specification 478	
TYPICAL DIMENSIONS:	9.12" H, 11.40" W, 8.84" D (232 x 290 x 225 mm)	10.94" H, 12.84" W, 10.22" D (278 x 326 x 260 mm)

* Specifications subject to change without notice.

GENERAL INFORMATION

The monitors described herein are fully transistorized (except CRT) and applicable for displaying alphanumeric characters. The M3000 series monitors use a 12-inch CRT and the M4000 series monitors use a 15-inch CRT. All M3000/4000 series monitors are capable of accepting a composite video signal or a non-composite video signal with separate TTL horizontal and vertical sync pulses. (See Schematic diagram.)

The CRT's employed are of the magnetic deflection type with integral implosion protection. An operating voltage of +70 volts DC is required from the regulated power supply for both models. A universal power transformer permits operating the monitor from either 115 or 230 volts AC, 50/60 Hz.

Input and output connections for the monitor are made through a 10-pin edge or header connector on the vertical/video circuit card. Inputs consist of video, horizontal/vertical sync, and signal ground. One additional input, an optional TTL level StepScan, may also be connected to the monitor via the 10-pin edge connector. Output connections are provided for an optional remote brightness control.

Circuitry consists of two stages for video amplification, five stages for vertical sync and deflection processing, five stages for horizontal sync and deflection processing, and a regulated +70 volt power supply. Both models also have available as options, dynamic focusing, vertical blanking amplifier, horizontal sync delay, and StepScan amplifier. (See Schematic diagram.)

Four etched circuit cards are utilized, containing the vertical/video circuit, horizontal circuit, differential amplifier/sync separator circuit and power supply circuit. An optional low voltage logic power supply is available when a remote power source is required for logic interface circuitry. Components are mounted on the top of the circuit cards and plating copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on the three circuit cards. Refer to Motorola Service Manual VP20, Part No. 68P25253A40 for complete service information on the low voltage logic power supplies and VP21, Part No. 68P25253A41 for complete service information for the composite video circuit card.

COMPONENT REMOVAL

Removing components from an etched circuit card is facilitated by the fact that the circuitry (copper foil) appears on one side of the circuit card only and the component leads are inserted straight through the holes and are not bent or crimped.

It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the circuit card foil due to over-heating.

The nozzle of the solder extracting gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper foil. This method is particularly suitable in removing multi-terminal components.

When replacing "plug-in" transistors, please observe the following precautions:

1. The transistor sockets are not "captive", which means that the transistor mounting screws also secure the socket. When installing the transistor, the socket must be held in its proper position.

2. When replacing a plug-in transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink and bottom of the transistor. In addition, be sure a mica insulator is positioned properly between the transistor and heat sink.

3. The transistor mounting screws must be tight before applying power to the monitor. This insures proper cooling and electrical connections. NON-COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

NOTE

Use caution when tightening transistor mounting screws. If the screw threads are stripped by excessive pressure, a poor electrical and mechanical connection will result.

SERVICE NOTES

CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the three circuit cards to facilitate circuit tracing. In addition, control names and circuit card terminal numbers are also shown and referenced on the schematic diagram in this manual.

Transistor elements are identified as follows:

E – emitter, B – base, and C – collector.

2. Remove CRT from the front of the chassis by loosening and removing four screws; one in each corner of the CRT.

REGULATOR ADJUSTMENT

NOTE

Misadjustment of the low voltage regulator, or the horizontal oscillator may result in damage to the horizontal output transistor or pulse limiter diode. The following procedure is recommended to insure reliable operation.

1. Connect the monitor to an AC line supply; then adjust supply to 120 volts (240 volts in some applications).

2. Apply test signal to proper input. Signal should be of same amplitude and sync rate as when monitor is in service.

3. Adjust HOR. SET coil L50 (on the horizontal circuit card) until display is stable.

4. Connect a DC digital voltmeter or equivalent precision voltmeter to the emitter of the regulator output transistor, Q150 (or any +70 volt test point on the power supply circuit card).

5. Adjust the 70V ADJUST. control, R158, on the power supply circuit card for an output of +70 volts. DO NOT rotate the control through its entire range; damage to the monitor may result.

6. When adjustment is complete, the AC line supply can be varied between 105 and 130 volts AC to check for proper regulator operation. With the regulator operating properly, changes in display size should be negligible.

HORIZONTAL HOLD/OSCILLATOR ADJUSTMENT

Adjust the core of HOR. SET coil L50 until the horizontal blanking lines are vertical, or the CRT display is stable (synced).

CRT REPLACEMENT

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum pressure. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. In addition, be sure to disconnect the monitor from all external voltage sources.

1. Discnarge CRT by shorting 2nd anode to ground; then remove the CRT socket, deflection yoke and 2nd anode lead.

2. Adjust DYNAMIC FOCUS coil L52 for best edge focus.

3. Alternate between adjusting R70 and L52 until overall CRT focus is optimized.

PROCEDURE NO. 2

1. Connect an oscilloscope (DC coupled) between the junction of R71 and C63 (on horizontal circuit card) and signal ground.

CAUTION

High voltage is present.

2. Adjust the oscilloscope controls until one cycle of the horizontal rate sinewave appears as shown in Figure 1.

3. Adjust the DYNAMIC FOCUS coil, L52 for a minimum sinewave amplitude of not more than 125 volts P-P.

NOTE

Be sure that the one cycle appearing on the oscilloscope is not a harmonic of the horizontal rate sinewave. This may occur if the DYNAMIC FOCUS coil, L52, is misadjusted to the extent that L52 will produce the second harmonic. The coil must be adjusted to produce the minimum amplitude of the fundamental frequency only. Confirm the preceding by momentarily connecting the oscilloscope across the primary of T50. Only one cycle or pulse should appear.

4. Observe the center of the CRT display and adjust the FOCUS control, R70, for optimum focus; then record the DC voltage (represented as amplitude "A" in Figure 1) between the DC 0 volt reference and the negative peak of the sinewave.

5. Observe the edges of the CRT display and adjust the FOCUS control, R70, for optimum focus; then record the DC voltage (represented as amplitude "B" in Figure 1) between the DC 0 volt reference and the positive peak of the sinewave .

DYNAMIC FOCUS ADJUSTMENT

The DYNAMIC FOCUS coil is factory set and should not normally require further adjustment. However, if it becomes necessary, use Procedure No. 1 for touching up the overall focus. Procedure No. 2 is provided if the CRT (V1) and/or DYNAMIC FOCUS coil (L52) is replaced in the field.

PROCEDURE NO. 1

1. Adjust FOCUS control R70 (on horizontal circuit card) for best focus in the center of the CRT.

6. Subtract the negative peak voltage from the positive peak voltage. The difference becomes the voltage value to which the DYNAMIC FOCUS coil, L52, must be adjusted.

7. While observing the sinewave, adjust the DYNAMIC FOCUS coil, L52, until amplitude "C" (see Figure 1) equals the difference voltage value determined in step 6.

8. While observing the oscilloscope, readjust the FOCUS control, R70, until the negative peak of the sinewave is positioned above the DC 0 volt reference line equal to the voltage value recorded in step 4.

Amplitude "A" – Represents adjusting FOCUS control, R70, for best CRT center FOCUS.

Amplitude "B" – Represents adjusting FOCUS control, R70, for best CRT edge FOCUS.

Amplitude "C" – Represents adjusting DYNAMIC FOCUS coil, L52, for final P-P setting that is equal to difference between amplitude "A" and "B".

NOTE: After amplitude "C" is adjusted, amplitude "A" must be reset to the original voltage value that provided best CRT center FOCUS.

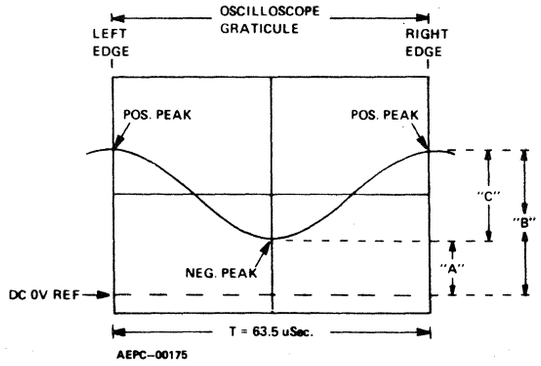


Figure 1. Adjusting Dynamic Focus with an Oscilloscope

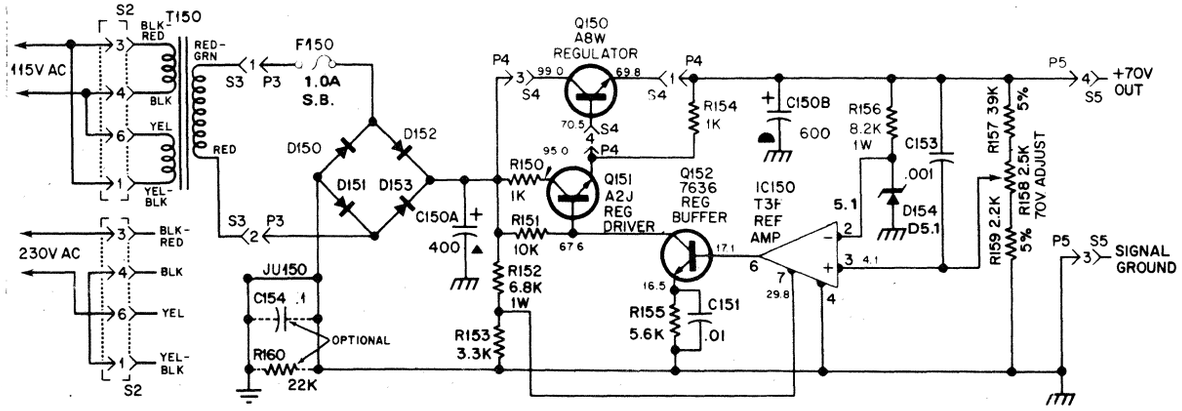
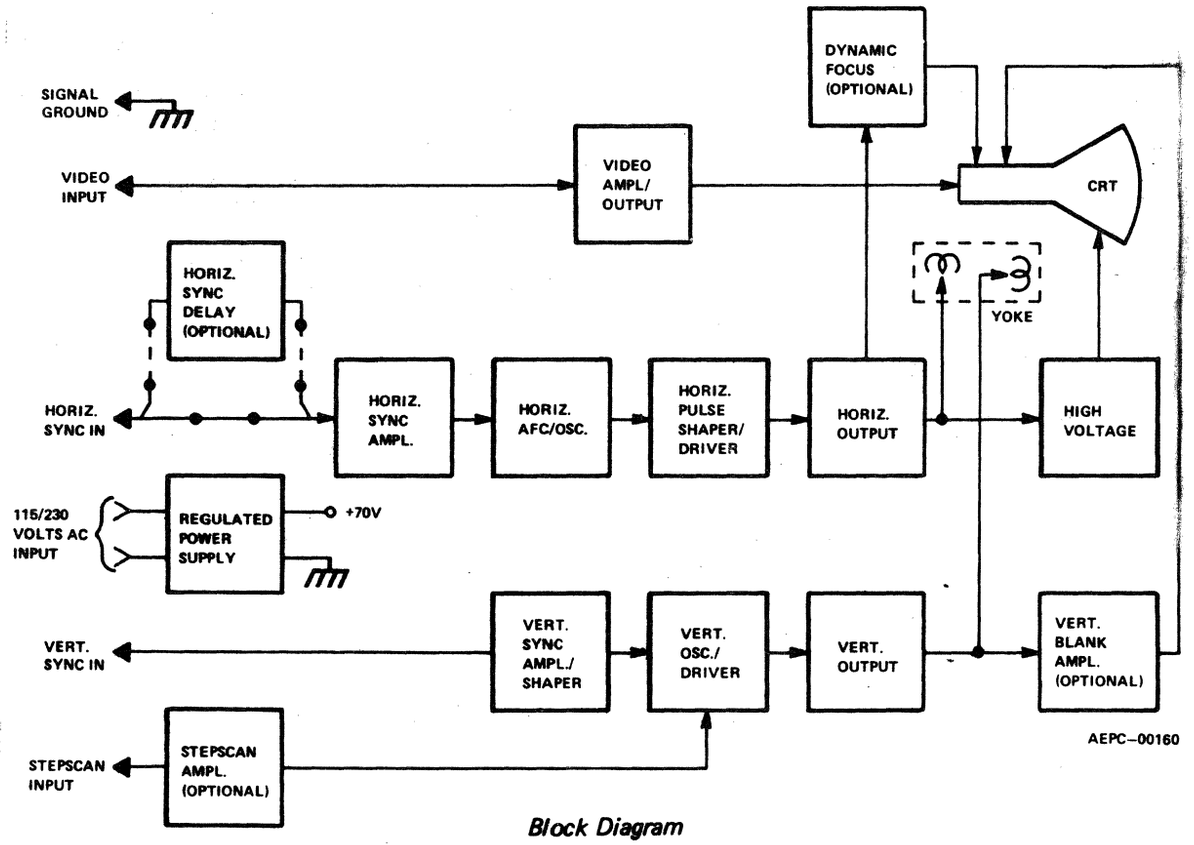


Figure 2. Power Supply Circuit



Block Diagram

THEORY OF OPERATION

POWER SUPPLY

(Refer to Figure 2.)

The power supply is a transformer operated, full wave, regulated series pass circuit that maintains a constant output voltage with line input variations of ±12.5%. Depending on how connector S2 is wired, operation from 115 or 230 volts, 50/60 Hz is possible. Integrated circuit IC150 is the reference amplifier, transistor Q152 is a regulator buffer, transistor Q151 is the regulated output driver, and Q150 is the series pass transistor.

The output voltage, +70V, appears at the emitter of Q150. This voltage is divided between R157, R158 and R159. The voltage appearing on the arm of potentiometer R158 (70V ADJ. control) is the reference input to the non-inverting input of reference amplifier IC150.

A temperature compensated zener diode, D154, establishes a fixed reference voltage at the inverting input to IC150. Resistor R156 provides a bias current for D154, which establishes its operating point. Capacitor C153 is a high frequency filter. Operating voltage for IC150 is derived from a voltage divider consisting of R152 and R153. Components R155 and C151 set the voltage gain of Q152.

An increase in output voltage will result in an increase of voltage at the base of Q152 via the non-inverting input of IC150. The change in base voltage will turn Q152 on harder, reducing its collector voltage. This reduces the forward bias to Q151, which results in less emitter current for Q150. With Q150 conducting less, the output voltage will be lowered.

Components C154 and R160 isolate the power supply common return from chassis (earth) ground. They are only required, however, when the signal input is accompanied by AC hum. If AC hum is not present, jumper JU150 is used to bypass C154 and R160. Dual-section capacitor C150 provides filtering.

VIDEO AMPLIFIER

(Refer to Figure 3.)

The linear video amplifier consists of two stages, Q100 and Q101, which are connected in a cascode configuration. This common emitter-common base arrangement greatly reduces the effect of Miller capacity (when compared to a conventional single transistor video amplifier/output stage).

A TTL compatible non-composite video signal, approximately 4.0 volts P-P, is DC coupled to the base of Q100 via R100. Resistor R112 provides proper termination for the high frequency input video signal. Capacitor C100 provides high frequency compensation to maintain a flat response when Q100 and Q101 conduct.

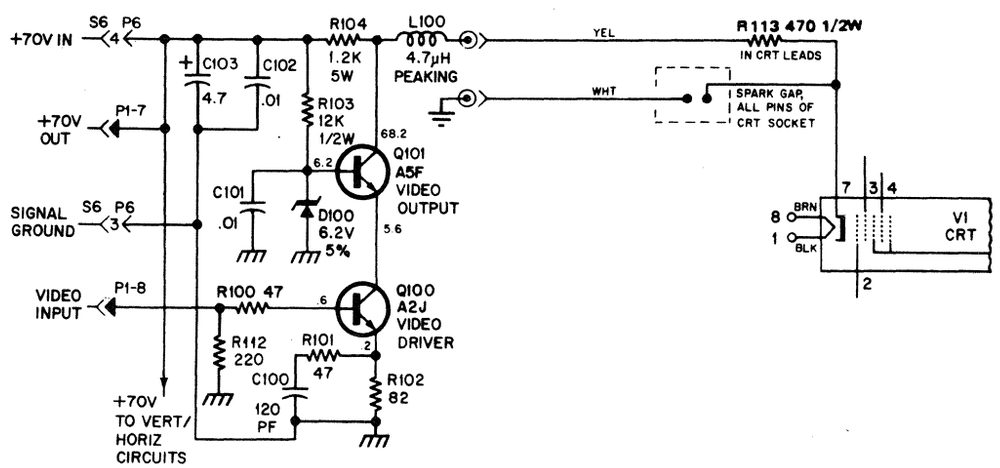


Figure 3. Video Amplifier Circuit

During no-signal conditions, Q100 is off. Transistor Q101, however, is forward biased by the 6.2 volts on its base, which is established by zener diode D100. When a video signal is applied to the base of Q100, it conducts, which causes forward biased Q101 to conduct. The resultant output is developed across R104 at the collector of Q101; then DC coupled to the cathode of V1 (CRT) via peaking coil L100 and R113. Resistor R113 isolates Q101 from transients that may occur as a result of CRT arcing. Capacitor C101 shunts to ground high frequency video that may appear on the base of Q101. Peaking coil L100 boosts the high frequencies of the video signal. Capacitor C103 provides additional filtering of the +70V, while C102 is a high frequency AC bypass capacitor.

HORIZONTAL SYNC AMPLIFIER
(Refer to Figure 4.)

The horizontal sync amplifier consists of one stage, Q50, which operates as a switch. During a no-signal condition, Q50 is off. When a positive-going horizontal sync signal, approximately 4.0 volts P-P, is applied (DC coupled) to the base of Q50, it goes into saturation. The amplified output is developed across load resistor R51, approximately 35V, which forms a voltage divider with R77. The negative-going horizontal sync pulses are AC coupled to the phase detector circuit via the R-C network consisting of R52 and C68, a high frequency pass filter.

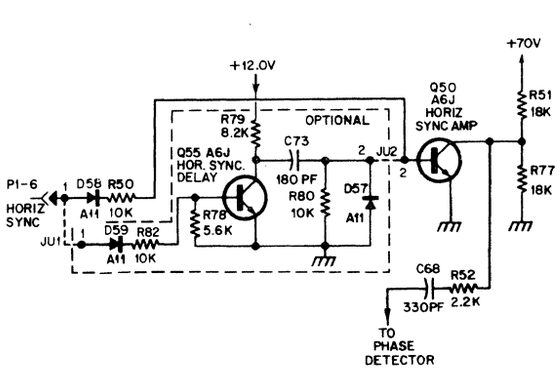


Figure 4. Horizontal Sync Amplifier and Optional Horizontal Sync Delay Circuits

OPTIONAL HORIZONTAL SYNC DELAY CIRCUIT
(Refer to Figure 4.)

This circuit is required when the input TTL level horizontal sync pulse does not have a front porch, which may occur in some systems. (For reference, Figure 5A illustrates a standard horizontal sync pulse with a front porch.) The circuit operates in conjunction with the horizontal sync amplifier, Q50. However, jumpers JU1 and JU2 must be inserted, and resistor R50 removed.

During no-signal conditions, Q55 is off. When a horizontal sync pulse (Figure 5B) is applied to the base of Q55, however, it turns on to saturation. The inverted output (Figure 5C) is developed across load resistor R79 and capacitor C73 charges through R80. When the horizontal sync pulse has completed its period, Q55 turns off causing its collector voltage to rise. The base voltage of the horizontal sync amplifier, Q50, also rises turning that device on. Transistor Q50 stays on for the duration of the charge on C73, which discharges through R80 and the base-emitter junction of Q50.

The time delay between the turn-on of Q55 and turn-on of Q50 is approximately 2.0 to 5.0 uS, or the time duration (width) of one horizontal sync pulse without a front porch (Figure 5D). Resistor R82 is for current limiting to the base of Q55. Diode D57 protects Q50 from reverse breakdown.

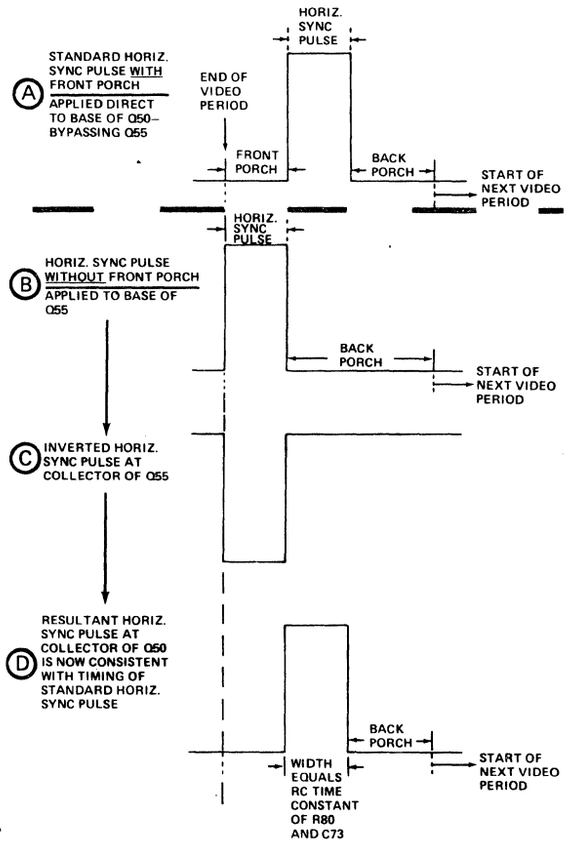


Figure 5. Horizontal Sync Delay Circuit Waveforms

PHASE DETECTOR
(Refer to Figure 6.)

The phase detector consists of two diodes (D50 and D51) in a keyed clamp circuit. Two inputs are required to generate the required output, one from the horizontal sync amplifier, Q50, and one from the horizontal output circuit, Q54. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. The horizontal output (Q54) collector pulse is integrated into a sawtooth by R56 and C69. During horizontal sync time, diodes D50 and D51 conduct, which shorts C69 to ground. This effectively clamps the sawtooth on C69 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A), the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge on C69 will be zero (waveform B). If the horizontal time base is lagging the sync, the sawtooth on C69 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C69 (waveform C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C69 will be clamped at a point positive from its AC axis. This results in a net negative charge on C69, which is the required polarity to slow the horizontal oscillator (waveform D). Components R55, C52, R58 and C53 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. Capacitor C50 times the phase detector for correct centering of the picture on the raster.

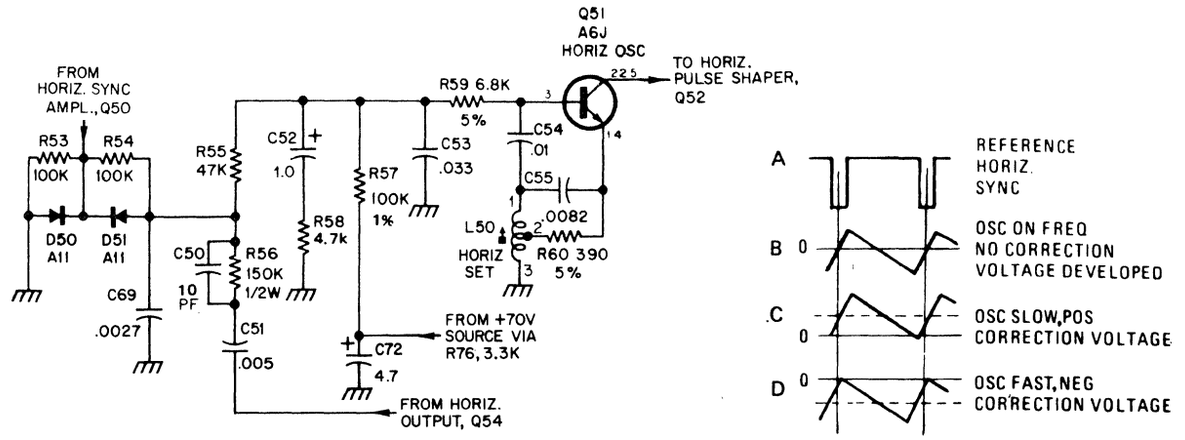


Figure 6. Phase Detector and Horizontal Oscillator Circuits

HORIZONTAL OSCILLATOR
(Refer to Figure 6.)

The horizontal oscillator consists of Q51, which is employed as a modified type of Hartley oscillator. The operating frequency of this oscillator is sensitive to its base input voltage. This permits control by the output of the phase detector. Resistor R57 provides DC bias to turn on Q51 and start the oscillator. The free-running horizontal frequency is adjusted with the HORIZ. SET coil, L50, which along with C54 are the frequency determining components. Capacitor C55 and resistor R60 are feedback components for the oscillator circuit.

HORIZONTAL PULSE SHAPER & DRIVER
(Refer to Figure 7.)

Transistor Q52 is a buffer stage between the horizontal oscillator and horizontal driver. It provides isolation for the horizontal oscillator as well as a low impedance drive for the horizontal driver. Components R62 and C56 form a time constant that shapes the oscillator output to the required duty cycle, approximately 50%, to drive the horizontal output circuitry. The horizontal driver stage, Q53, operates as a switch to drive the horizontal output transistor (Q54) through T50. Because of the low impedance drive and fast switching times furnished by Q52, very little power is dissipated in Q53. Components R66 and C57 provide damping to suppress ringing in the primary of T50 when Q53 goes into cutoff. (Reference Figure 8 – Resistor R68 provides current limiting for Q53 while C58 is an AC bypass capacitor.)

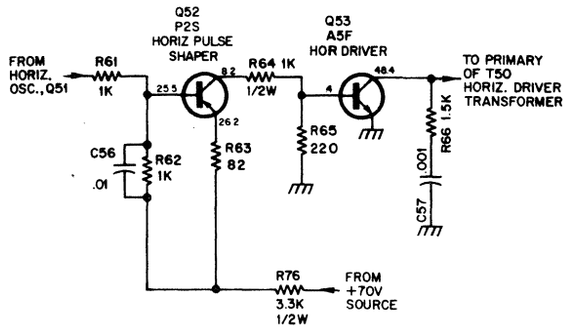


Figure 7. Horizontal Pulse Shaper and Driver Circuits

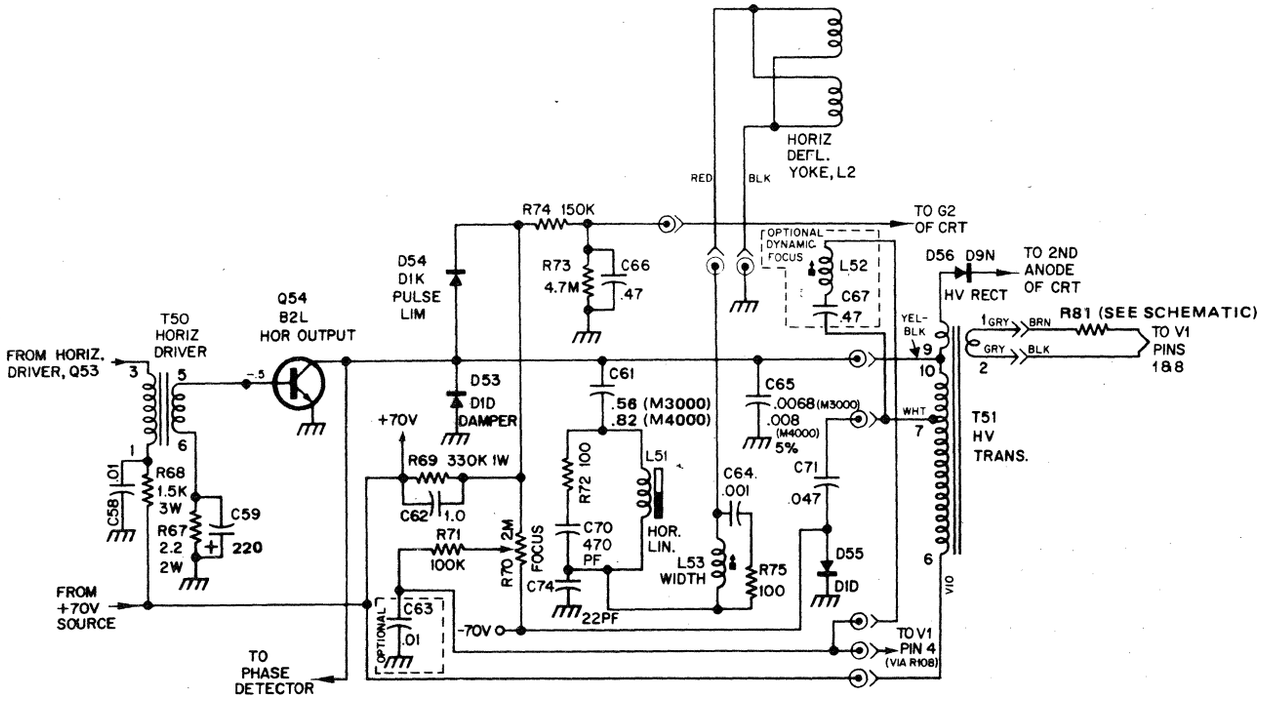


Figure 8. Horizontal Output Circuit

HORIZONTAL OUTPUT
(Refer to Figure 8.)

The secondary of T50 provides the required low drive impedance for Q54. Components R67 and C59 form a time constant for fast turn-off of the base of Q54. Once during each horizontal period, Q54 operates as a switch that connects the supply voltage across the parallel combination of the horizontal deflection yoke and the primary of the high voltage transformer. The required sawtooth deflection current (through the horizontal yoke) is formed by the L-R time constant of the yoke and primary winding of the H.V. transformer, T51. The horizontal retrace pulse charges C62 through D54 to provide operating voltage for G2 of the CRT. Momentary transients at the collector of Q54, should they occur, are limited to the voltage on C62 since D54 will conduct if the collector voltage exceeds this value.

The damper diode, D53, conducts during the period between retrace and turn on of Q54. Capacitor C65 is the retrace tuning capacitor, while C61 blocks DC from the deflection yoke. Coil L51 is a magnetically biased linearity coil that shapes the deflection current for optimum trace linearity. Coil L53 is a series horiz. width control. Components R72 and C70, C64 and R75 are damping network components for the horizontal linearity (L51) and width (L53) controls. Capacitor C71 couples horizontal sync pulses from pin 7 of T51 to diode clamp D55, which maintains the −70V reference voltage.

OPTIONAL DYNAMIC FOCUS CIRCUIT
(Refer to Figure 9.)

Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to a corner as compared to the distance traveled at the center of the CRT screen. As a result of these various distances traveled, optimum focus can be obtained at only one point. For general applications, an adequate adjustment can be realized by setting the focus while viewing some point mid-way between the center of the CRT screen and a corner, thus optimizing the overall screen focus. When an application requires a tighter specification, one of the simplest methods for improvement is to modulate the focus voltage at a horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam travel along this axis.

The AC component focus voltage is developed by a series resonant circuit consisting of L52 and C63. This voltage is an 80V P-P horizontal rate pulse coupled from a tap on the horizontal output transformer, T51, via C67. The normal DC component of the G4 focus voltage is set by adjusting the FOCUS control, R70. When the DYNAMIC FOCUS coil, L52, is optimized for best edge focus, a sinusoidal voltage of approximately 200V P-P is developed across C63. This mixed AC and DC voltage results in a waveform of proper phase and amplitude, which is coupled through isolating resistor R108 to the CRT focus anode.

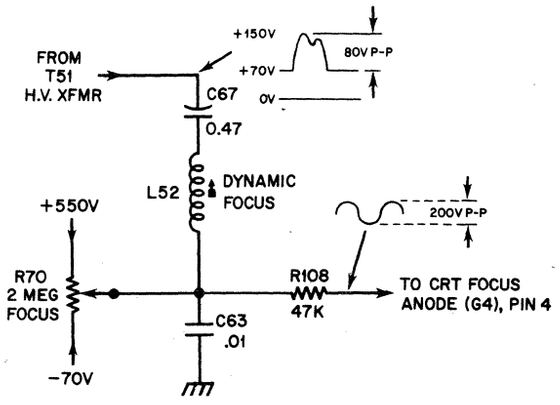


Figure 9. Simplified Dynamic Focus Circuit Diagram

VERTICAL SYNC AMPLIFIER
(Refer to Figure 10.)

The vertical sync amplifier consists of one stage, Q1, which operates as a switch. During no-signal conditions, Q1 is off. When a positive-going vertical sync signal, approximately 4.0 volts P-P, is applied (direct coupled) to the base, Q1 goes into saturation. The amplified output is developed across load resistor R3 to approximately 11 volts. Jumpers JU3, JU4, and JU5 are inserted depending on the polarity of the input vertical sync pulse; TTL NEG for negative-going and TTL POS for positive-going.

SYNC SHAPER
(Refer to Figure 10.)

The negative-going vertical sync pulses (from Q1) are direct coupled to the non-inverting input of the sync shaper stage, IC1. The combined action of an integrating network, consisting of C1, C2, C3, R5, R6, and R7, removes high frequency noise from the vertical sync pulses. Capacitor C3 performs the actual integrating, while resistors R5–R7 provide biasing for IC1. Capacitors C1 and C2 provide a bypass function.

VERTICAL OSCILLATOR
(Refer to Figure 11.)

The negative-going vertical sync pulses are AC coupled (C4) to the gate of a programmable unijunction transistor device, D1. This device turns on with each negative-going sync pulse applied to its gate. This action permits C6 and C7 to discharge very rapidly; then recharge slowly during the period that a sync pulse is not applied to the gate. The recharge path for C6 and C7 is through R12 and R13. As soon as the next sync pulse is applied to the gate of D1, C6 and C7 discharge very rapidly again. This sequence of events produces a positive-going ramp or sawtooth waveform at the anode of D1.

When no vertical sync pulses are connected to the monitor, vertical oscillator D1 is kept free-running to maintain a raster on the CRT. This is accomplished by biasing the gate of D1 in conjunction with the charge and discharge action of C6 and C7. Resistors R9 and R8 provide the proper bias for D1, which also determines the repetition rate for the charge and discharge action of C6 and C7.

In addition, during no-signal conditions, components R22 and D2 (in conjunction with D1), provide a small incremental voltage above ground to compensate for the base-emitter voltage drop of the vertical driver, Q3. This is necessary to keep the vertical output stage, Q4, from being driven into cutoff, which could result in distorted vertical linearity.

VERTICAL DRIVER
(Refer to Figure 11.)

The positive-going sawtooth waveform, from the anode of D1, is direct coupled to the base of vertical driver Q3, which operates as an emitter follower. The sharp fall time of the sawtooth is a result of the rapid discharge of C6 and C7 through D1. The amplitude of the sawtooth is varied with the HEIGHT control, R12.

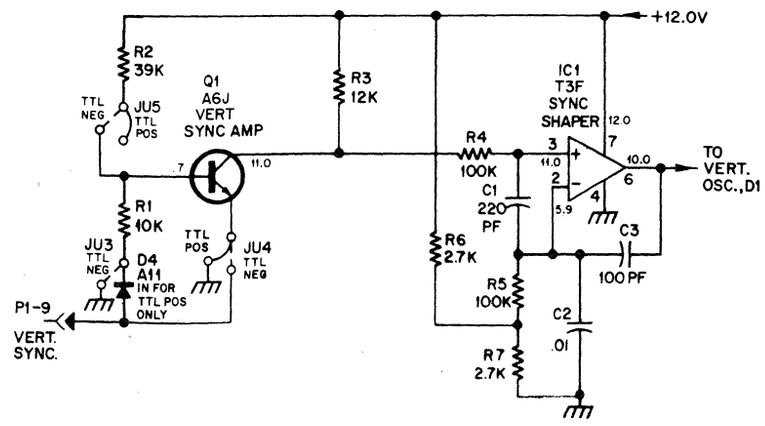


Figure 10. Vertical Sync Amplifier and Sync Shaper Circuits

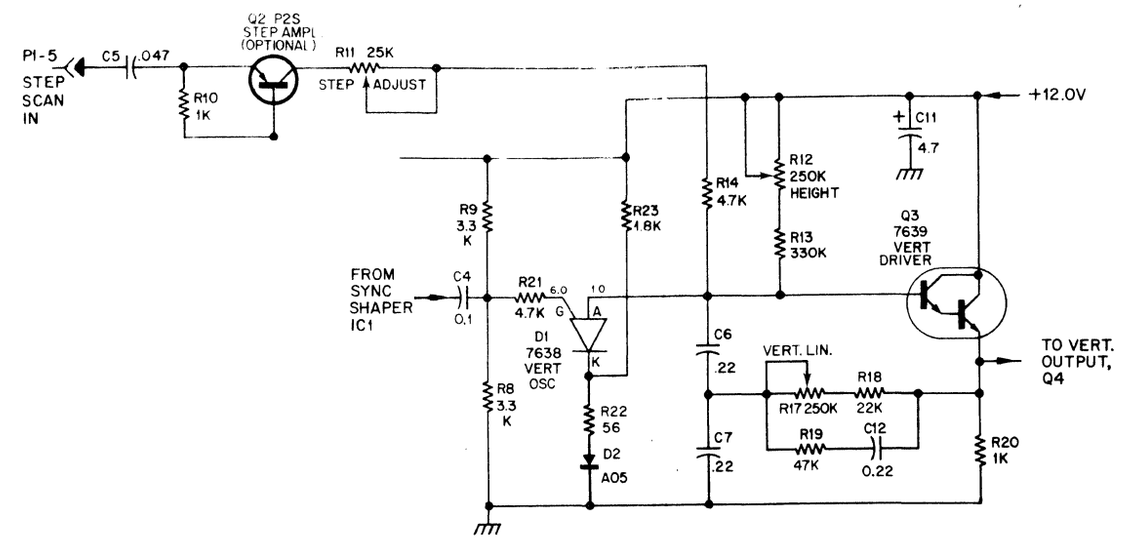
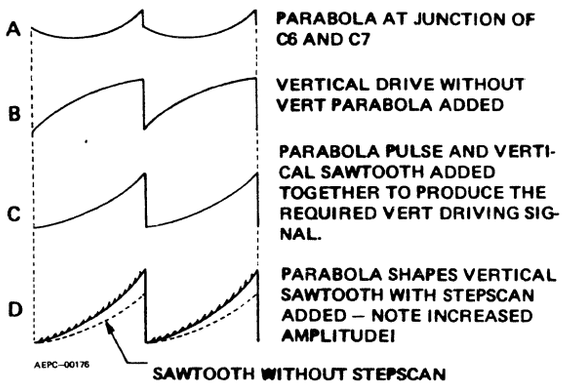


Figure 11. Vertical Oscillator/Driver and Optional StepScan Amplifier Circuits



The output sawtooth from the emitter of Q3 is direct coupled to the base of vertical output stage, Q4. Part of this sawtooth waveform, however, is also coupled back to the junction of C6 and C7 via R18 and VERT. LIN. control R17 for proper shaping. Since this path is resistive, the waveform will be integrated into a parabola waveform by C7 (waveform A). This results in a predistortion of the drive sawtooth (waveform C). (Waveform B illustrates the drive sawtooth without parabola shaping.) Parabola shaping is necessary to compensate for the non-linear charging of C6 and C7. An additional path for phase compensation is provided through C12 and R19.

VERTICAL OUTPUT

(Refer to Figure 12.)

The positive-going sawtooth waveform from the emitter of Q3 is applied to the base of vertical output stage, Q4, which conducts only during the ramp, or rise time, of the sawtooth waveform. The inverted ramp output (collector current) is the vertical trace period, which is AC coupled (via C14) to the vertical deflection yoke winding. The same collector current output is also applied to L1, which builds up a large electromagnetic field. This field will collapse very rapidly when Q4 turns off during the retrace time of the waveform applied to the base of Q4. The back EMF is in the form of a high voltage positive pulse, whose duration represents the vertical retrace period. To limit this pulse to a safe value, a varistor is connected across L1, with R26 providing damping.

Except for the vertical output stage, Q4, the vertical circuitry operates from a +12 volt source, which is derived from the +70 volt source. Resistor R27 drops the +70 volt source to the required +12V. Zener diode D3 holds the +12V constant while C11 provides additional filtering.

OPTIONAL VERTICAL BLANKING AMPLIFIER CIRCUIT

(Refer to Figure 12.)

The vertical blanking amplifier circuit is for systems that desire to blank the beam during the vertical retrace period.

Transistor Q9 turns on only when a high voltage positive pulse is applied to its base. (This positive pulse is generated for the retrace period each time the vertical output stage, Q4, turns off.) Components R35, C17 and R36 form a voltage divider to protect the base input of Q9. The inverted collector output is developed across R37, which forms a voltage divider with R38. The amplitude of the negative blanking pulse is approximately 30 volts P-P, which is AC coupled by C104 to G1 of the CRT. Capacitor C105 is a high frequency bypass for G1.

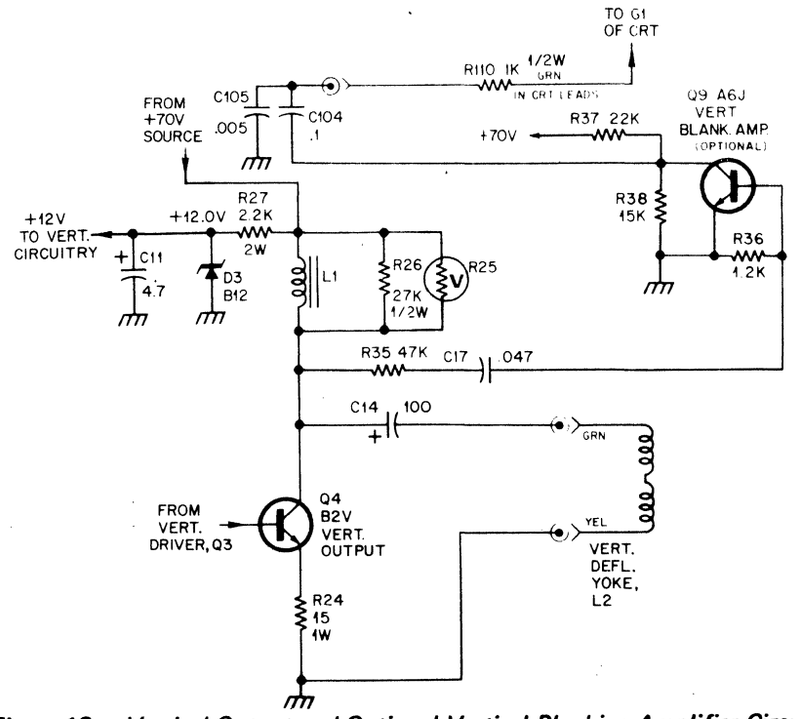


Figure 12. Vertical Output and Optional Vertical Blanking Amplifier Circuits

STEPSCAN FUNCTION

With existing logic, the number of characters that can be displayed is limited by logic speed. Anything that increases the speed at which the logic must work, will allow an increase in the number of characters displayed.

When a video monitor is used as a data display, the system bandwidth required (and logic speed) increases in direct proportion to the number of scan lines displayed. Since no data is written in the blank spaces between character rows, a method is required to speed up vertical deflection in the blank spaces to decrease bandwidth requirements. This makes the blank space height less dependent on scan time, allowing time to display more characters. This is accomplished by "stepping" the reference sawtooth between character rows so that a row to row space of from 3 to 5 horizontal lines equivalent height can be displayed in the time it takes to deflect one horizontal line. This is illustrated in Figure 13.

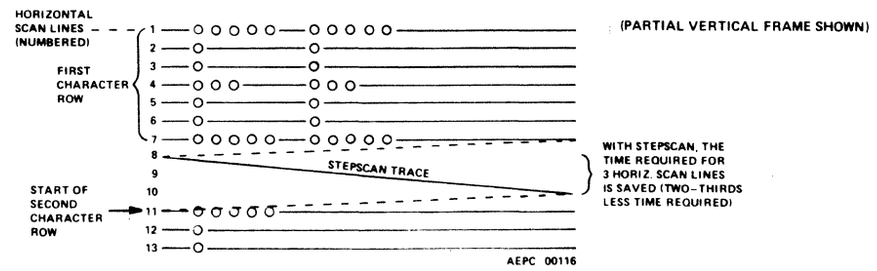
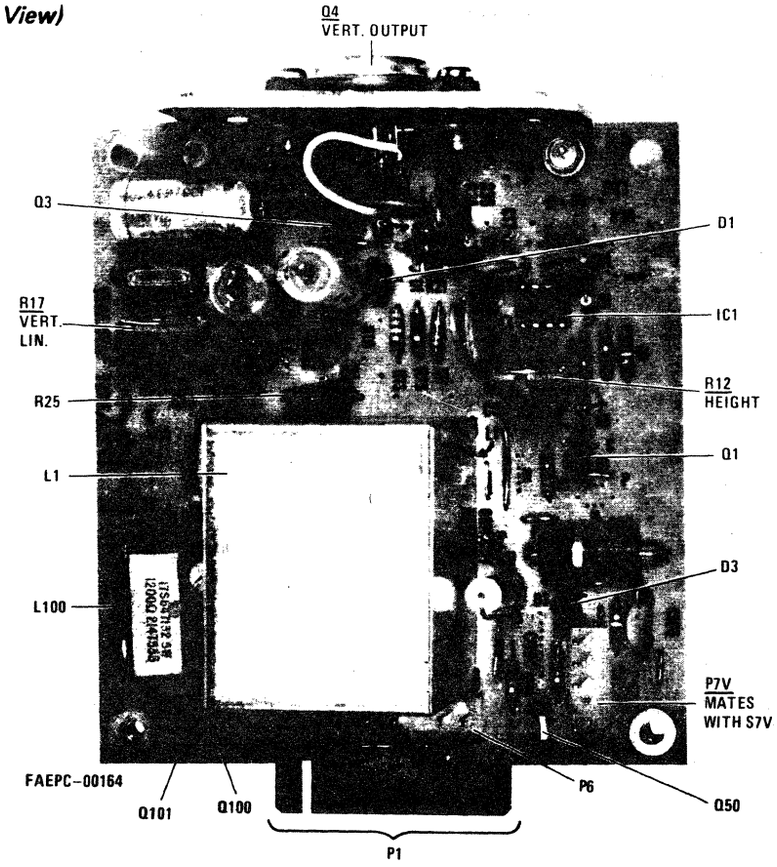


Figure 13. Displaying Characters on a Monitor with StepScan

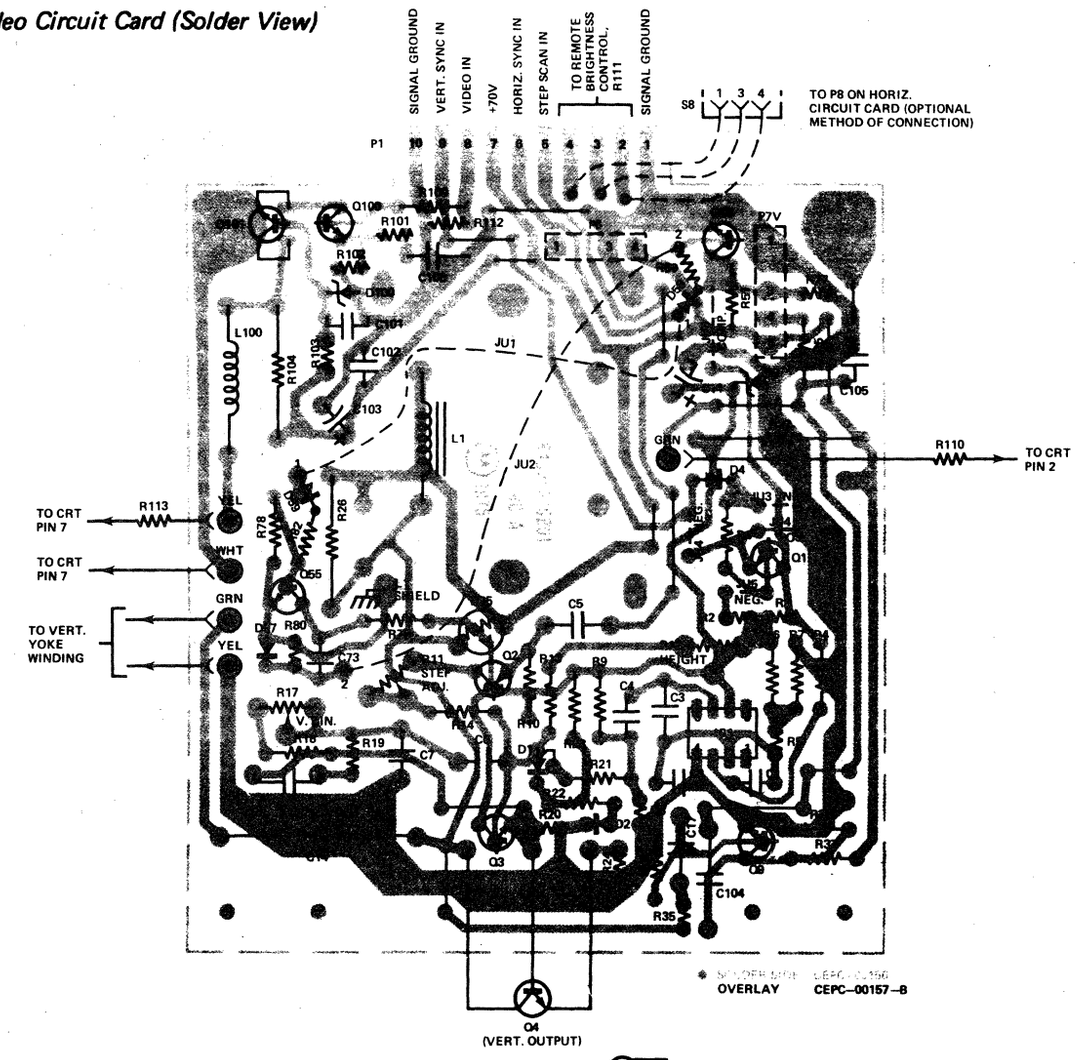
OPTIONAL STEPSCAN CIRCUIT (Refer to Figure 11.)

This circuit requires an external (approximately 4.0 volts P-P) TTL positive-going pulse. These pulses are applied to the emitter of the StepScan Amplifier, Q2, which is turned on when the emitter voltage exceeds the base voltage. The +12 volts stored on C5 is applied through Q2, R11 and R14, to the sawtooth forming capacitors C6 and C7. This momentarily increases the charge rate of C6 and C7, and the resultant action produces the stepping sawtooth shown as waveform D. The rate at which the vertical oscillator steps is determined by the repetition rate of the incoming StepScan pulses. The slope (charge rate) of the stepped portion of the sawtooth is adjustable with the STEP ADJ. control, R11, which varies the spacing from 3 to 5 horizontal scan lines. With the vertical sawtooth thus modified, the collector current of Q14 and, therefore, the yoke vertical deflection current will be "stepped" during the line between character rows chosen.

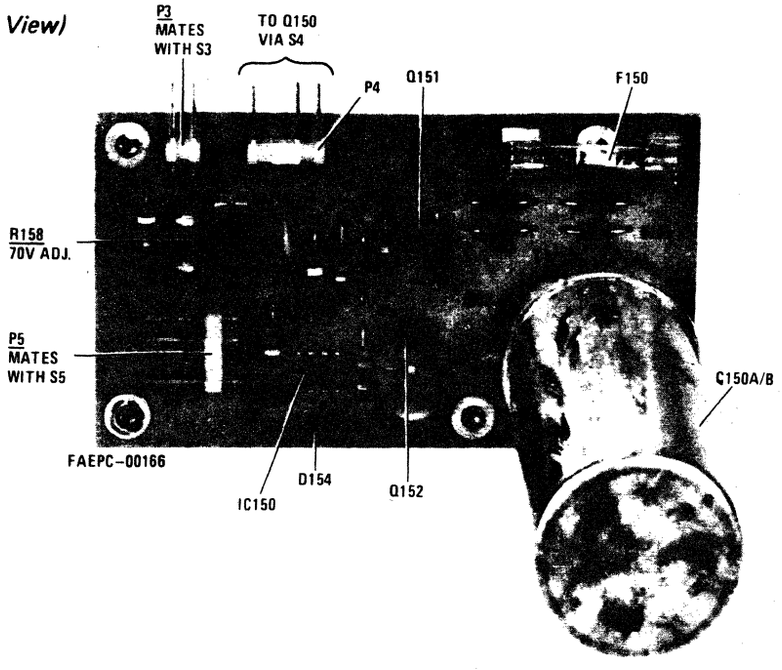
Vertical/Video Circuit Card (Component View)



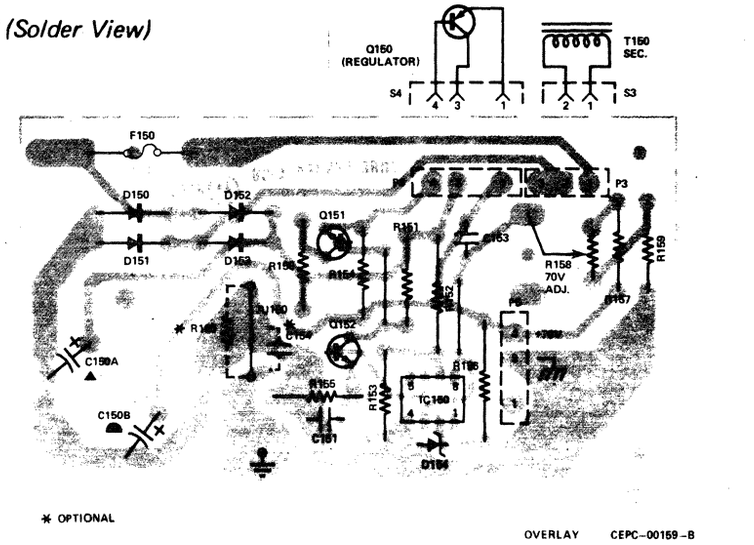
Vertical/Video Circuit Card (Solder View)



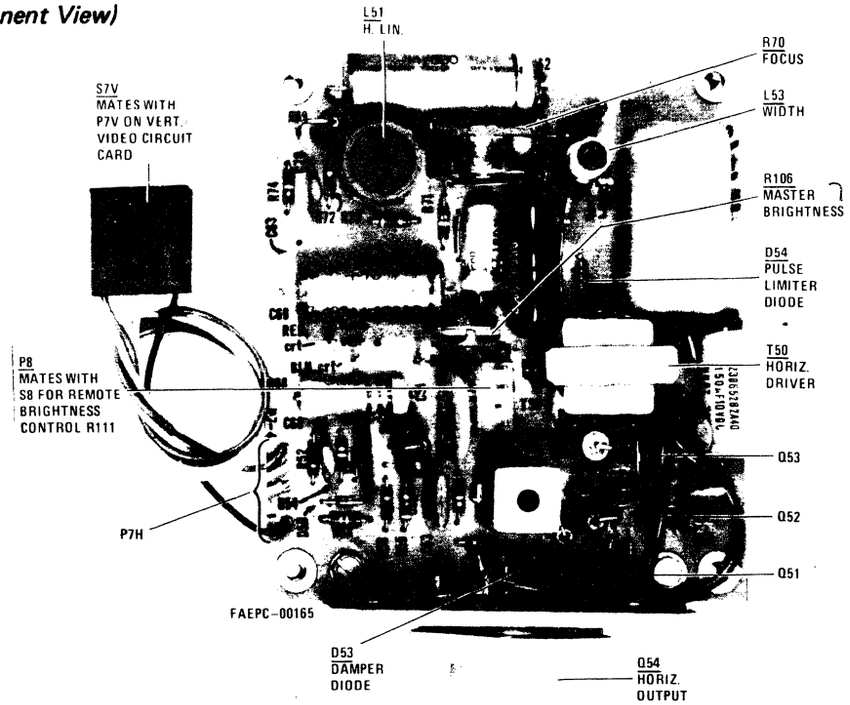
Power Supply Circuit Card (Component View)



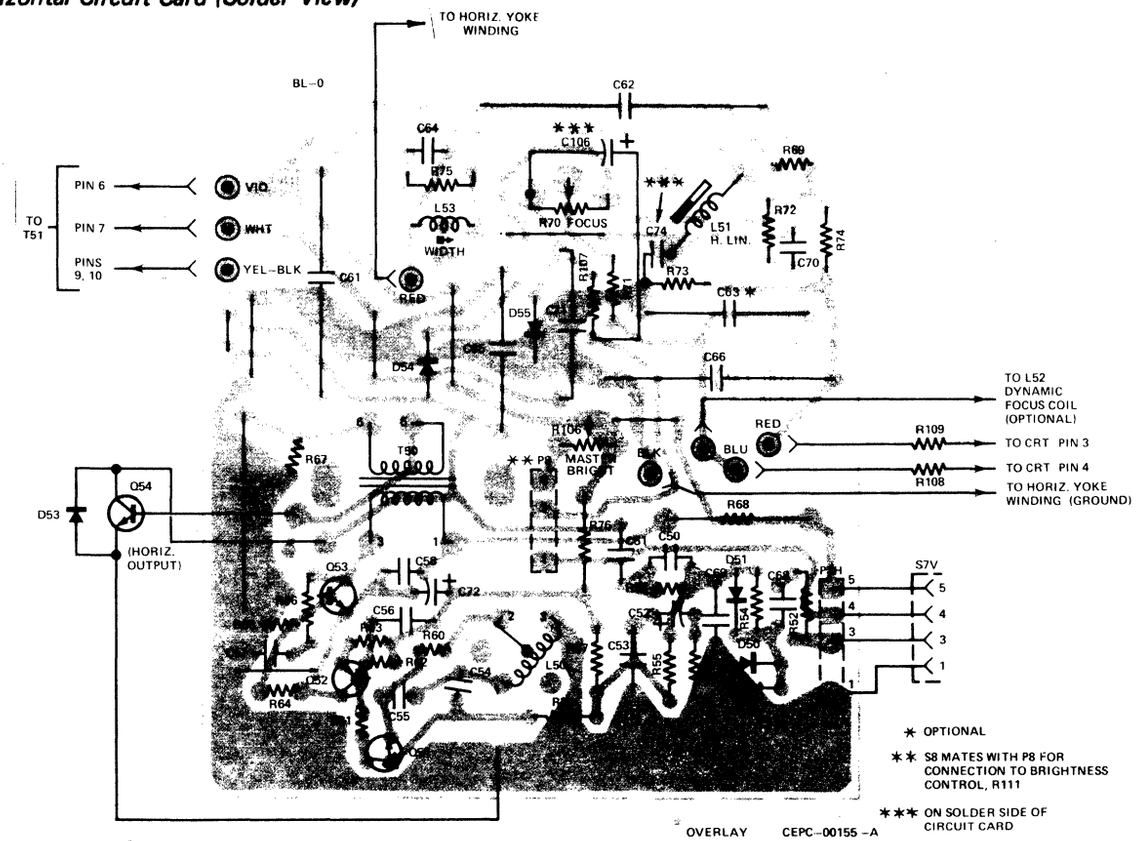
Power Supply Circuit Card (Solder View)



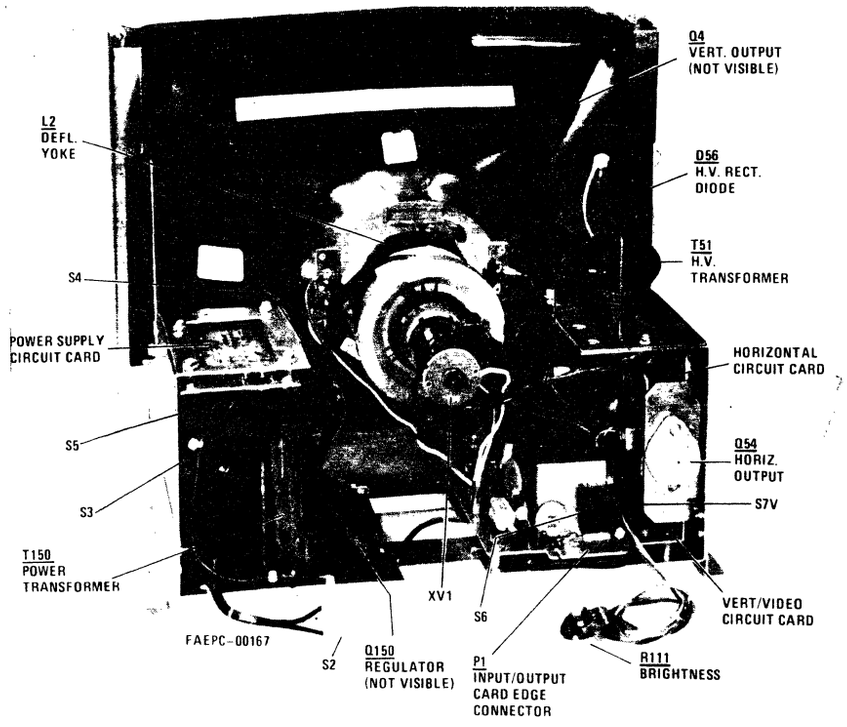
Horizontal Circuit Card (Component View)



Horizontal Circuit Card (Solder View)



Rear Chassis View – Typical of M3000/M4000

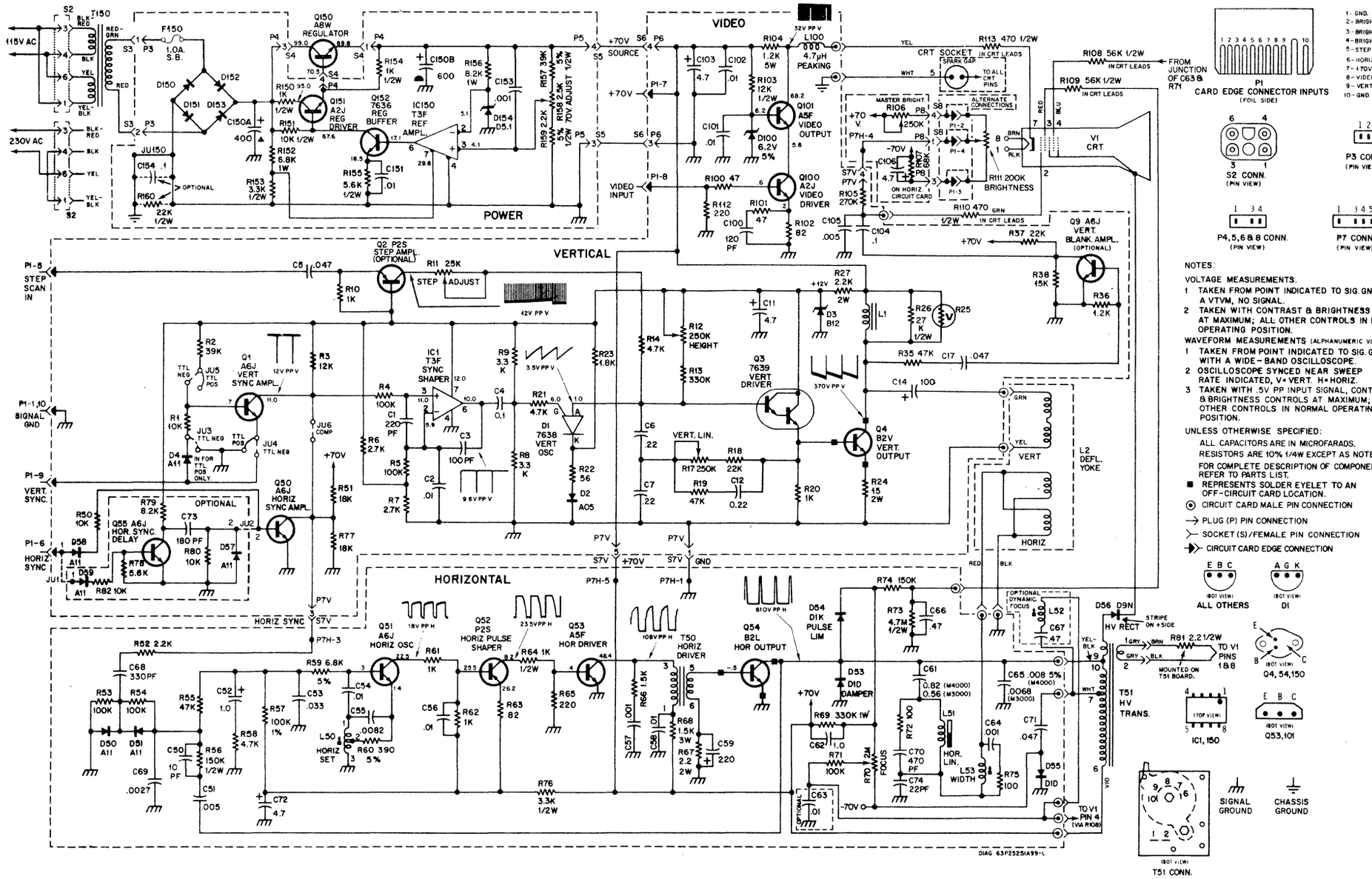


REPLACEMENT PARTS LIST

REF. NO.	PART NUMBER	DESCRIPTION
VERTICAL/VIDEO CIRCUIT CARD (COMPLETE):		
HORIZONTAL CIRCUIT CARD (COMPLETE):		
POWER SUPPLY CIRCUIT CARD (COMPLETE):		
Order by Model No. and Description		
CAPACITORS:		
(ALL VALUES ARE IN MICROFARADS UNLESS OTHERWISE NOTED.)		
C1	21S180B87	220 pF 10%,X5F,500V;Cer. Disc
C2	21S180E60	.01 +80–20%,Z5V,50V;Cer. Disc
C3	21S180C50	100 pF 5%, NP0, 500V; Cer. Disc
C4	8S10212D52	0.1 10%, 100V; Mtlz Poly
C5	8S10191B91	.047 10%, 250V; Polyester
C6, 7	8S10191B67	0.22 10%, 250V; Polyester
C11	23S10255A69	4.7, 100V; lytic
C12	8S10212C08	0.22 10%, 100V; Polyester
C14	23S10255A60	100, 63V; lytic
C17	8S10191B91	.047 10%, 250V; Polyester
C50	21S180C02	10 pF, NP0, 500V; Cer. Disc
C51	21S180D34	.005 20%, Z5F, 1 kV; Cer. Disc
C52	23S10229A32	1.0 +40–20%, 16V; lytic
C53	8S10191B90	.033 10%, 250V; Polyester
C54	8S10299A32	.01 10%, 400V; Poly Carb
C55	8S10299A33	.0082 10%, 100V; Poly Carb
C56	8S10191B98	.01 10%, 250V; Polyester
C57	21S180B51	.001 10%, X5F, 500V; Cer. Disc
C58	21S180E60	.01 +80–20%,Z5F,50V; Cer. Disc
C59	23S10255B81	150, 10V; lytic
C61	8S10571A23	0.56 10%, 250V; Polyprop (M3000–100,200,300,400)
C61	8S10299B27	0.82 10%, 400V; Mtlz Poly Carb (M4000–100, 200)
C62	8S10212A11	1.0 10%, 630V; Mtlz Mylar
C63	8S10571A06	.01 5%, 1200V; Polyprop
C64	21S180B51	.001 10%, Z5F, 500V; Cer. Disc
C65	8S10571A04	.0068 5%, 1200V; Polyprop (M3000–100, 200, 300, 400)
C65	8S10571A05	.008 10%, 1200V; Polyprop (M4000–100, 200)
C66	8S10212B53	0.47 10%, 630V; Mtlz Mylar
C67	8S10212B20	0.47 10%, 400V; Mtlz Poly
C68	21S131625	330 pF 10%, X5F, 500V; Cer. Disc
C69	21S180C41	.0027 10%, Z5F, 500V; Cer. Disc
C70	21S180B72	470 pF 10%, Z5F, 500V; Cer. Disc
C71	8S10191B07	.047 10%, 400V; Polyester
C72	23S10255B28	4.7, 100V; lytic
C73	21S180F02	180 pF 10%, Z5F, 500V; Cer. Disc
C74	21S180B55	22 pF 10%, NP0, 500V; Cer. Disc
C100	21S180E50	120 pF 5%, NP0; Cer. Disc
C101, 102	21S180E60	.01 +80–20%, Z5V, 50V; Cer. Disc
C103	23S10255A69	4.7, 100V; lytic
C104	8S10191C02	0.1 10%, 250V; Polyester
C105	21S180A62	.005 20%, Z5V, 500V; Cer. Disc
C106	23S10255B26	4.7, 63V; lytic
C150A/B	23S10255B71	400/125V, 600/100V; lytic
C151	21S180E60	.01 +80–20%,Z5V,50V; Cer. Disc
C153	21S180B51	.001 10%, X5F, 500V; Cer. Disc
C154	21S180D02	0.1 +80 10%, 100V; Cer. Disc

REPLACEMENT PARTS LIST (Cont'd)

REF. NO.	PART NUMBER	DESCRIPTION
DIODES:		
D1	48S137638	Programmable UJT, MPU–6027; Vert. Osc.
D2	48S191A05	Rectifier, Silicon; A05
D3	48D10641B12	Diode, Zener
D4,50,51	48D67120A11	Diode, Low Power; A11
D53	48S134921	Diode, D1D; Damper
D54	48S134978	Diode, D1K; Pulse Lim.
D55	48S134921	Diode, D1D
D56	48S137622	Diode, Silicon, D9N; H.V. Rect.
D57–59	48D67120A11	Diode, Low Power; A11
D100	48S10813A01	Diode, Zener 6.2V 5% (1N5234B)
D150–153	48S191A05	Rectifier, Silicon; 91A05
D154	48S10813A02	Diode, Zener 5.1V
FUSES:		
F150	65S139424	Fuse, Slow Blow 1.0 Amp.
INTEGRATED CIRCUITS:		
IC1	51S10732A01	Integrated circuit, T3F; Sync Shaper
IC150	51S10732A01	Integrated circuit, T3F; Ref. Ampl.
COILS/CHOKES:		
L1	25D25221A13	Choke, Vert.
L2	24D25261B01	Yoke, Deflection (M3000–100, 200, 300, 400)
L2	24D25261A08	Yoke, Deflection (M4000–100, 200)
L50	24D68822A01	Coil, Horiz. Set
L51	24D25248A12	Coil, Horiz. Lin.
L52	24D25248A01	Coil, Dynamic Focus
L53	24D25248B11	Coil, Horiz. Width
L100	24D25248A13	Coil, Peaking 4.7 uH 10%
TRANSISTORS:		
Q1	48S137172	Vert. Sync Ampl; A6J
Q2	48S137127	Step Ampl; P2S
Q3	48S137639	Vert. Driver; MPS–A13
Q4	48S137596	Vert. Output; B2V
Q9	48S137172	Vert. Blank Ampl; A6J
Q50	48S137172	Horiz. Sync Ampl; A6J
Q51	48S137172	Horiz. Osc.; A6J
Q52	48S137127	Horiz. Pulse Shaper; P2S
Q53	48S137093	Horiz. Driver; A5F
Q54	48S137570	Horiz. Output; B2L
Q55	48S137172	Horiz. Sync Delay; A6J
Q100	48S134952	Video Driver; A2J
Q101	48S137093	Video Output; A5F
Q150	48S137368	Regulator; A8W
Q151	48S134952	Reg. Driver; A2J
Q152	48S137636	Ref. Ampl; 7636
RESISTORS/CONTROLS:		
NOTE:		Only power or special resistors are listed. Use the description when ordering standard values of fixed carbon resistors up to 2 watts.
R11	18D25245A17	Control, Step Adjust 25k
R12	18D25245A22	Control, Height 250k
R17	18D25245A22	Control, Vert. Lin. 250k
R25	6S10201A04	Varistor, VDR 1 mA
R68	17S10130B07	1.5k 10%, 3W
R70	18C25218A14	Control, Focus 2 Meg.
R104	17S647132	1.2k 10%, 5W
R106	18D25245A22	Control, Master Brightness 250k
R111	18D25212A39	Control, Brightness 200k
R158	18D25245A21	Control, 70V Adjust 2.5k
TRANSFORMERS:		
T50	25D25221A05	Transformer, Horiz. Driver
T51	24D25240B11	Transformer, High Voltage (M3000–100,200,300,400)
T51	24D25240B13	Transformer, High Voltage (M4000–100,200)
T150	25D68164A33	Transformer, Power
MISC. ELECTRICAL PARTS:		
V1	96S233A01	12" CRT; Type ST5449A (M3000–100,200,300,400)
V1	96S219A01	15" CRT; Type ST4730C (M4000–100, 200)
MECHANICAL PARTS:		
	42B25158C01	Clamp, Deflection Yoke
	42S10240A07	Clamp (Mt. C150A/B)
	42S10122A12	Clip, Fuse
	42D25298A03	Connector, Anode
P3	28S10586A20	Connector, 2–Contact
P4, 5	28S10586A25	Connector, 3–Contact
P6	28S10586A14	Connector, 3–Contact
P7	28S10586A21	Connector, 4–Contact
P8	28S10586A14	Connector, 3–Contact
	14S10550A02	Cover, Transistor (Q54)
S2	15S10183A77	Housing, Receptacle; 6–Contact (Less Contacts)
	39S10184A64	Contact, Receptacle (4 Req'd for S2)
S3	15S10183A94	Housing, Receptacle; 2–Contact (Less Contacts)
	39S10184A72	Contact, Receptacle (2 Req'd for S3)
S4	15S10183A87	Housing, Receptacle; 3–Contact (Less Contacts)
	39S10184A72	Contact, Receptacle (3 Req'd for S4)
S5, 6	15S10183A87	Housing, Receptacle 3–Contact (Less Contacts)
	39S10184A72	Contact, Receptacle (2 ea. Req'd for S5 & S6)
S7	15S10183A88	Housing, Receptacle; 4–Contact (Less Contacts)
	39S10184A72	Contact, Receptacle (4 Req'd for S7)
S8	15S10183A87	Housing, Receptacle; 3–Contact (Less Contacts)
	39S10184A72	Contact, Receptacle (3 Req'd for S8)
	14A25393A01	Insulator, Hi–Voltage Standoff
	14A562353	Insulator,Transistor (Q150,Q54,Q4)
	2S10054A25	Nut, Spring
	3S136050	Screw, 6–20 x 1/2" Clutch Head (Mt. Q150, Q54, Q4)
	26B25137B01	Shield, Coil (L50)
	26B25348A01	Shield (Mt. w/L1)
	9D25470A02	Socket, CRT (Incl. leads and resistors R113–R110 & R81)
	9C63825A03	Socket, Transistor (Q150,Q54,Q4)
	41D65987A01	Spring, Special; CRT Aquadag Gnd
	66C68497A03	Tool, Adjust



1 - GND.
2 - BRIGHT HI
3 - BRIGHT LOW
4 - BRIGHT ARM
5 - STEP SCAN
6 - HORIZ. SYNC.
7 - +70V
8 - VIDEO INPUT
9 - VERT. SYNC.
10 - GND

NOTES:

VOLTAGE MEASUREMENTS.

1. TAKEN FROM POINT INDICATED TO SIG. GND. WITH A VTVM, NO SIGNAL.
2. TAKEN WITH CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM; ALL OTHER CONTROLS IN NORMAL OPERATING POSITION.

WAVEFORM MEASUREMENTS (ALPHANUMERIC VIDEO):

1. TAKEN FROM POINT INDICATED TO SIG. GND. WITH A WIDE-BAND OSCILLOSCOPE.
2. OSCILLOSCOPE SYNCED NEAR SWEEP RATE INDICATED, V = VERT. H = HORIZ.
3. TAKEN WITH .5V PP INPUT SIGNAL, CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM; ALL OTHER CONTROLS IN NORMAL OPERATING POSITION.

UNLESS OTHERWISE SPECIFIED:

ALL CAPACITORS ARE IN MICROFARADS.
RESISTORS ARE 10% 1/4W EXCEPT AS NOTED.
FOR COMPLETE DESCRIPTION OF COMPONENTS REFER TO PARTS LIST.

■ REPRESENTS SOLDER EYELET TO AN OFF-CIRCUIT CARD LOCATION.
⊙ CIRCUIT CARD MALE PIN CONNECTION
→ PLUG (P) PIN CONNECTION
⟩ SOCKET (S)/FEMALE PIN CONNECTION
⟩● CIRCUIT CARD EDGE CONNECTION

Schematic Diagram

OPERATION AND SERVICE MANUAL

ELECTROHOME V17 DATA DISPLAY MONITOR

Issue: September 1978

PERFORMANCE DATA AND SPECIFICATIONS

Monitor Description

The V_{17} Series Data Display Monitors provide alpha-numeric displays in 12" and 15" formats for application with non-composite TTL signal drive.

Controls

With the exception of the Width Coil, all controls are located on the single printed circuit board and are identified as:

- Vertical hold
- Vertical size
- Vertical linearity
- Vertical linearity amplitude
- Focus
- Master brightness
- Horizontal centering
- High voltage adjust

Performance Specifications

Input Signal Levels

Video:	4Vpp positive level referenced to 0	Tolerance:
* Vertical sync:	4Vpp negative level referenced to 0	0 state 0V + .4V -0.0V
Horizontal sync:	4Vpp positive level referenced to 0	1 state 4V ±1.5V

* NOTE: The V_{17} chassis will operate with positive level vertical sync without modification.

Input Impedance

Video: 220 ohms shunted by 40pf max.

Vertical sync: 4Kohm min. shunted by 40pf max.

Horizontal sync: 4Kohm min. shunted by 40 pf max.

Video Amplifier

Band width: 22 mhz at -3dB

Resolution

Center 1000 lines

Corners 800 lines

Deflection

Horizontal retrace time	8.5 µsec. max.
Vertical retrace time	800 µsec. max.
EHT	17KV

Geometry Distortion:

The outline of a full screen of characters shall approach an ideal rectangle within 1.5% of the height of the rectangle.

Power Requirements:

Input power:	60 VA max.
Input voltage:	100 to 130 V.A.C. 50/60 Hz switchable to 200 to 260 V.A.C. 50/60 Hz

The input circuit comprises a split-primary transformer.

Environmental:

Operating ambient temperature:	+5°C to +55°C
Humidity:	5% to 80% non-condensing
Altitude:	to 10,000 feet
Storage:	-40°C to +60°C

Operating and Service Information

MEASUREMENT, X-RAY, HIGH VOLTAGE AND CRT WARNINGS

1. X-RADIATION

   All cathode ray pix tubes emit some x-rays. This chassis has been designed for minimal x-radiation. However, to avoid possible exposure to soft x-radiation, ensure that EHT value is correctly set in accordance with procedures.

2. HIGH VOLTAGE

   This data monitor chassis contains HIGH VOLTAGES derived from power supplies capable of delivering LETHAL quantities of energy. To avoid DANGER TO LIFE, do not attempt to service the chassis until all precautions necessary for working on HIGH VOLTAGE equipment have been observed. In order to prevent damage to solid state devices, do not arc pix tube anode lead to chassis or earth ground.

   CAUTION: This chassis employs a high EHT (17KV) pix tube.

3. CRT HANDLING

   The picture tube encloses a high vacuum and due to the large surface area is subject to extreme force. Care must be taken not to bump or scratch the picture tube as this may cause the tube to implode resulting in personal injury and property damage. Shatter-proof goggles must always be worn by individuals while handling the CRT. Do not handle the CRT by the neck.

PRODUCT SAFETY SERVICING GUIDELINES

CAUTION

No modification of any circuit should be attempted. Service work should be performed only after you are thoroughly familiar with the following safety checks and servicing guidelines. To do otherwise increases the risk of potential hazards and injury.

SAFETY CHECKS

Subject: Fire and Shock Hazard

1. Do not install, remove, or handle the picture tube in any manner unless shatterproof goggles are worn. People not so equipped should be kept away while picture tubes are handled. Keep the picture tube away from the body while handling.

2. When service is required, observe the original lead dress. Extra precaution should be given to assure correct lead dress in the high voltage circuitry area. Where a short circuit has occurred, replace these components that indicate evidence of overheating. Always use the manufacturer's replacement component.

3. Always check high voltage for proper value and at all times use an accurate high voltage meter. The calibration of this meter should be checked periodically.

4. After servicing of the monitor, perform an A.C. leakage test on the exposed metallic cabinet to be sure the set is safe to operate without danger of electrical shock. Do not use a line isolation transformer during the test. Use an A.C. voltmeter having 1000 ohms per volt or more sensitivity in the following manner: - Connect a 1500 ohm 10 watt resistor, paralleled by a.15 mfd, AC-type capacitor between a known good

earth ground (water pipe, conduit, etc.) and the exposed metallic frame. Measure the A.C. voltage across the combination 1500 ohm resistor and .15 uf capacitor. Reverse the AC connection to the set and repeat AC voltage measurements for exposed metallic frame. Voltage measured must not exceed .3 volts RMS. This corresponds to 0.5 milliamp AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

5. Check for frayed insulation on wires including AC wiring.

Drive Signals

Apply TTL drive signals (see performance specifications) to the 10 pin edge connection on the printed circuit board P-100. The attached schematic details pin functions.

Power Connection

Connect power plug P401 to 115VAC line. Ensure that the line selection switch, SW401, is in the correct position.

Vertical hold

The vertical hold control, R205, normally needs adjustment only when the vertical scan frequency is altered (say 60 to 50Hz field rate). However, should vertical instability occur, the vertical hold control should be centered in its hold-in range.

Scan size

Vertical size is adjusted by control R_{226} and width is adjusted by width coil L_{303} (located to the rear of the left side panel).

Centering

The raster is centered vertically and horizontally on the CRT by rotating the two concentric centering magnets which are part of the yoke assembly. This is a factory adjustment and should normally need set up only for a yoke or CRT replacement.

The video or data information is centered horizontally by centering control R_{304}.

Linearity and geometry

Vertical linearity phase control, R_{227}, is adjusted for equal character height at the top and bottom of the screen while vertical linearity amplitude control, R_{225}, is adjusted for equal character height between the center and the top and bottom extremes of scan.

Horizontal linearity is fixed by polarized linearity coil L_{302} and "S" shaping capacitor C_{312}.

Other linearities and geometries are part of the static yoke compensation.

Brightness

On models wired for a 200K external brightness control, the control is advanced fully clockwise and the Master brightness control, R_{323}, is adjusted for the desired level of maximum brightness or visibility of raster.

Focus

Focus control, R_{320}, is adjusted for optimum focus between the center and corners of a full format of displayed characters for nominal brightness conditions.

High voltage adjust

Control R_{411} is preset to $+70V_{DC}$ at the factory. This setting in conjunction with the width coil setting establishes the EHT at 16.4KV $\pm$ 800V. The +70V setting also ensures operation of the monitor at line voltages as low as $100V_{AC}$.

CIRCUIT DESCRIPTION

POWER SUPPLY

Basic topology of the transformer operated power supply provides for regulated $+70V_{DC}$ for horizontal deflection and video, unregulated $+45V_{DC}$ for the vertical deflection, and $6.1V_{AC}$ for the CRT filament. It's important that the regulated supply be set to +70V rather than for $+75V_{DC}$ where operation down to $100V_{AC}$ line is required.

Full wave bridge rectifiers (D_{401} to D_{404}) and capacitor input filter C_{405A} provide a nominal $+93V_{DC}$ to a series pass regulator circuit. Q_{401} is the series pass element while Q_{403} is its current driver. Q_{404} is the voltage error amplifier that monitors changes in the regulated output (via the divider chain of R_{410}, R_{411}, and R_{412}) versus the 10 volt reference zener voltage of ZD403. Q_{402} and its biasing arrangement of R_{402}, R_{403}, R_{404}, and zener ZD402 form a constant current pre-regulator to minimize ripple in the regulated output voltage.

Nominal current demand on the regulator supply varies between 280 ma. and 350 ma. The configuration of Q_{405} and R_{408} provides for current limiting at a supply current threshold of 650 ma. The additions of resistors R_{406}, R_{407}, and R_{413} modify the current limiting into current foldback for overloads beyond 650 ma. The current foldback is non-latching in nature so that B+ is restored with the removal of the overload fault without the necessity of interrupting primary power.

Unregulated +45 volts for vertical deflection is available at the center tap of the secondary winding. D_{401} and D_{402} effect full wave rectification for this supply while C_{405B} provides filtering. A +7 volt supply for the horizontal drive delay circuit is obtained with the decoupling network of R_{401} and C_{403}.

A separate secondary winding on the power transformer provides $6.1V_{AC}$ for the CRT filament.

The dual winding primary of T401 can be switched by SW401 to parallel-connected windings for 117 volt line operation typical in North America or to a series-connected configuration for 230 volt operation typical in Europe.

VIDEO DRIVE

Positive going video drive at pin 8 of the input PCB edge connector is applied to the base of Q_{101}. Q_{101} and Q_{102} are connected in cascode with the collector signal of Q_{101} driving the emitter of Q_{102}. The base of Q_{102} is DC biased via the 6.2 volt supply of ZD201. Negative going video at the collector of Q_{102} drives the Cathode of the CRT. With full TTL video input, the Q_{102} collector output is typically $25V_{pp}$ with black level at the supply potential of +70V. L_{101}, C_{102}, and R_{102} provide high frequency compensation.

VERTICAL DEFLECTION

The vertical deflection system consists of an inverter stage Q_{201} for the TTL vertical sync drive; a reference sawtooth voltage generator of Q_{202}, Q_{203}, and Q_{204}; and a current feedback output amplifier of Q_{205} through Q_{210}.

Normally negative going TTL vertical sync (as in figure 1) is inverted by Q_{201} to provide a 6 volt positive going sync signal at its collector. The short time constant network of R_{203} and C_{201} differentiates the sync waveform and applies the resulting pulse to the base of Q_{202}. The positive going portion of this waveform that corresponds to the negative going edge of the input vertical sync pulse initiates the vertical scan retrace from the bottom of the CRT screen.

NOTE: Positive going vertical sync input may be used. The positive going portion of the differentiated waveform is then simply displaced from the sync leading edge by the width of the incoming vertical sync pulse (typically 3 horizontal line periods or 190 μsec).

Q_{202} and Q_{203} are normally off during scan with the collector of Q_{202} and the base of Q_{203} at the supply level of 6.6 volts. The positive portion of the differentiated Q_{201} collector sync signal drives Q_{202} (NPN) into conduction so that its collector voltage drops. Q_{203} (PNP) is thus driven into saturation as the base emitter junction of Q_{203} clamps the Q_{202} collector excursion to +5.9 volts. Saturation of Q_{203} brings its collector voltage up close to the emitter B+ level. The positive going pulse that occurs at the collector of Q_{203} (when it is turned on) is transferred to the base of Q_{204} through the network of R_{210} and C_{203}, with C_{203} appearing as an instantaneous short to the leading edge of the pulse. Q_{204} (NPN) is driven into saturation and its collector voltage drops to near zero. Since the emitter circuit of Q_{202} is connected to the collector of Q_{204} via R_{208}, it is also pulled down turning Q_{202} on even harder. This initial sequence is then seen to be regenerative.

Once the positive pulse at the collector of Q_{203} has occurred, C_{203} begins to charge toward the 6.6 volt supply. All three transistors stay in saturation until C_{203} has charged to approximately 6 volts through the low impedances of Q_{203}, R_{210}, and the B-E junction of Q_{204}. This charge time is shorter than the nominal 190 usec duration of the vertical sync pulse.

Once C_{203} has charged, Q_{204} begins to come out of saturation, its collector voltage rising momentarily to 6.2 volts. This positive going polarity on the emitter of Q_{202} biases this stage off followed by Q_{203}. Thus far, the short duration pulse generated at point "A" (figure 1) corresponds to the retrace period in the sequence of vertical scan.

Base and collector currents of Q_{204} now interact with the discharge of C_{203} to produce a linearly decreasing voltage ramp for vertical scan. The topology is typically that of a Miller "run-down" ramp generator - the constant collector current of Q_{204} results in a linearly decreasing voltage across C_{203}. Having Q_{202} and Q_{203} off during scan reduces the possibility of horizontal contamination on the sync line from affecting interlace.

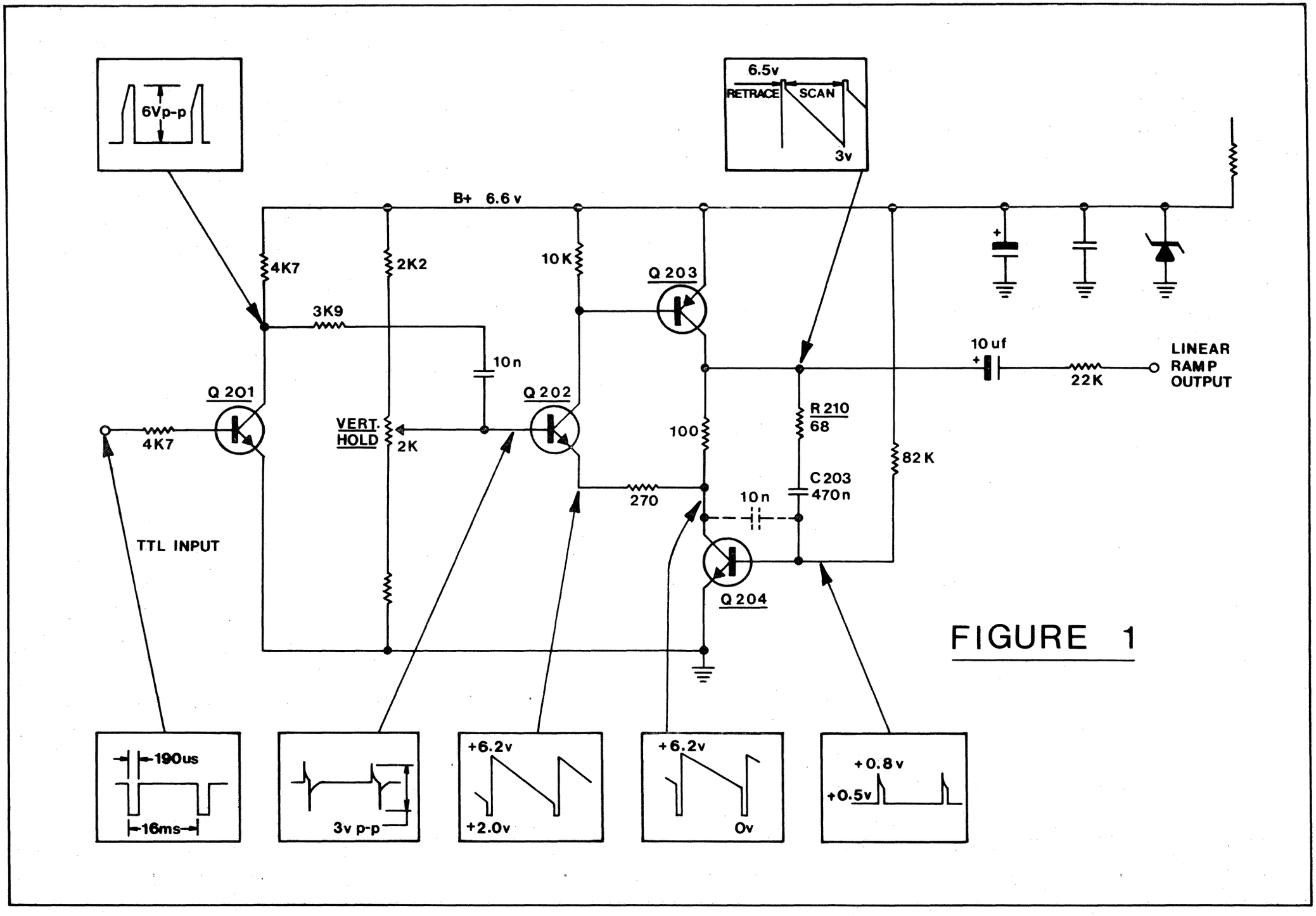

6Vp-p
6.5v
RETRACE
SCAN
3v
B+ 6.6 v
4K7
2K2
10K
Q 203
3K9
10n
10 uf
LINEAR
RAMP
OUTPUT
22K
Q 201
Q 202
R 210
68
VERT.
HOLD
2K
4K7
100
82 K
C 203
470n
270
10n
TTL INPUT
Q 204
190us
16ms
3v p-p
+6.2v
+2.0v
+6.2v
0v
+0.8 v
+0.5v

FIGURE 1

Stages Q_{205} and Q_{206} form a differential amplifier where current feedback moderates the linear voltage ramp for linearity correction and stabilization. The inverted signal at the collector of Q_{205} is applied to the base of Q_{207} (PNP).

Q_{207} through Q_{210} form a conventional quasi-complementary class B amplifier not unlike that found in an audio application. The load however, is the paralleled vertical yoke windings of 25MH inductance and 10 ohms resistance. A sawtooth of current from the amplifier produces a trapezoidal or near square wave of voltage across this inductive/resistive load.

The 110° deflection CRT locates the yoke (center of magnetic deflection) far in front of the center of curvature of the relatively flat faceplate. A linear sawtooth of vertical deflection current, then, would cause scan velocity differences between top/bottom and the center, appearing as linearity distortion. Linearity correction calls for the sawtooth of deflecting current being modified into an "S" shape. Capacitor C_{206} placed in series with the yoke provides a parabola of voltage. The network of R_{225}, C_{207} and double integrator of R_{227}, C_{208}, R_{229}, C_{209} phase shift the parabola to place the "S" correction in the proper time relationship. Control R_{225} varies amplitude of correction while control R_{227} adjusts phase.

Also in series with the yoke is current sense resistor R_{223}. The voltage across this resistor fed back to earlier stages serves to stabilize deflection. R_{226} and R_{224}, in controlling the amount of feedback, provide vertical size adjustment. The network of R_{230} and R_{228} provide for adding the "S" correction voltage and current sense resistor voltage for feedback to the base of Q_{206}. In the differential amplifier the feedback moderates the Miller ramp voltage for the desired end result.

HORIZONTAL DEFLECTION

The V_{17} uses a direct drive horizontal deflection system to process horizontal drive signals. This approach is less susceptible to timing errors due to beam current variations as compared to conventional phase-locked-loop systems. It can also accept a wide variety of data signals without sacrificing performance. When horizontal drive is not present the entire horizontal system becomes inoperative.

1C301, a dual 555 timer circuit, has both sections connected as monostable multivibrators or "one-shots" which produce a fixed delay or timing when triggered by a pulse. The first one-shot accounts mostly for the delay of the horizontal drive by a full horizontal line period. Timing adjustment is determined by R_{304} which is used to position the displayed data information on the center of the raster. The delay accommodates various circuit delays (Q_{302}, Q_{303}) as well as variations in signal format.

The second one-shot is used to generate a near symmetrical square wave which is necessary for proper switching of the horizontal deflection transistor Q_{303}.

Q_{301} accepts a positive-going horizontal drive pulse from pin 6 of the PCB connector and inverts it. The negative going edge appearing at Q_{301} collector triggers the first one-shot at pin 6. Overall timing of the first one-shot is determined by R_{304}, R_{305}, and C_{302}. The output at pin 5 consists of a pulse whose negative going edge corresponds

to the delayed-horizontal drive. This edge toggles the second one-shot at pin 8.

The second one-shot, whose timing is fixed by R_{307} and C_{306}, produces a pulse at output pin 9 of near symmetrical duty cycle. Q_{302} saturates when this pulse is positive and cuts off when it is near zero. T_{301} amplifies the collector current of Q_{301} to provide the necessary high base current (1.3A) for the horizontal deflection transistor Q_{303}.

Horizontal deflection is accomplished in a standard shunt efficiency flyback circuit.

Flyback T302 and D_{303} produce $17KV_{DC}$ for the CRT second anode. D_{301} rectifies the primary retrace pulse to supply $+500V_{DC}$ to the brightness, focus, and G_2 circuits. D_{304} rectifies a negative flyback pulse to provide a $-80V_{DC}$ supply for the brightness control circuit.

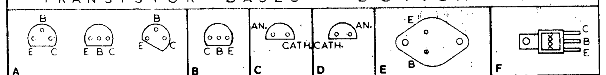
When power is switched off the negative supply is maintained by C_{313}. As the +500 volt supply falls, ZD301 drops out of its zener mode and isolates the brightness circuit from discharging C_{313} rapidly. The full $-80V_{DC}$ potential appears at G_1 ensuring that the picture tube is cut off until the filament and cathode cool sufficiently to eliminate any emission and possible phosphor burn.

Circuitry is protected from CRT arcing by spark gaps integral in the cathode and grid leads of the CRT socket. Arc energy is thus returned to the aquadag. Current limit resistors are also located in all grid and the cathode leads.

X-RADIATION HOLD DOWN CIRCUIT

An increase in B+ could lead to an increase in high voltage and X-ray emission. An x-ray protection circuit, consisting of ZD101, prevents triggering of the first "one-shot" in IC301 in the event of an increase in B+ to 82 volts $\pm$2% by pulling pin 6 positive beyond its trigger threshold. Once ZD101 is biased into its zener mode the entire horizontal system stops and no further high voltage is produced until the B+ fault is corrected.

V17 SCHEMATIC



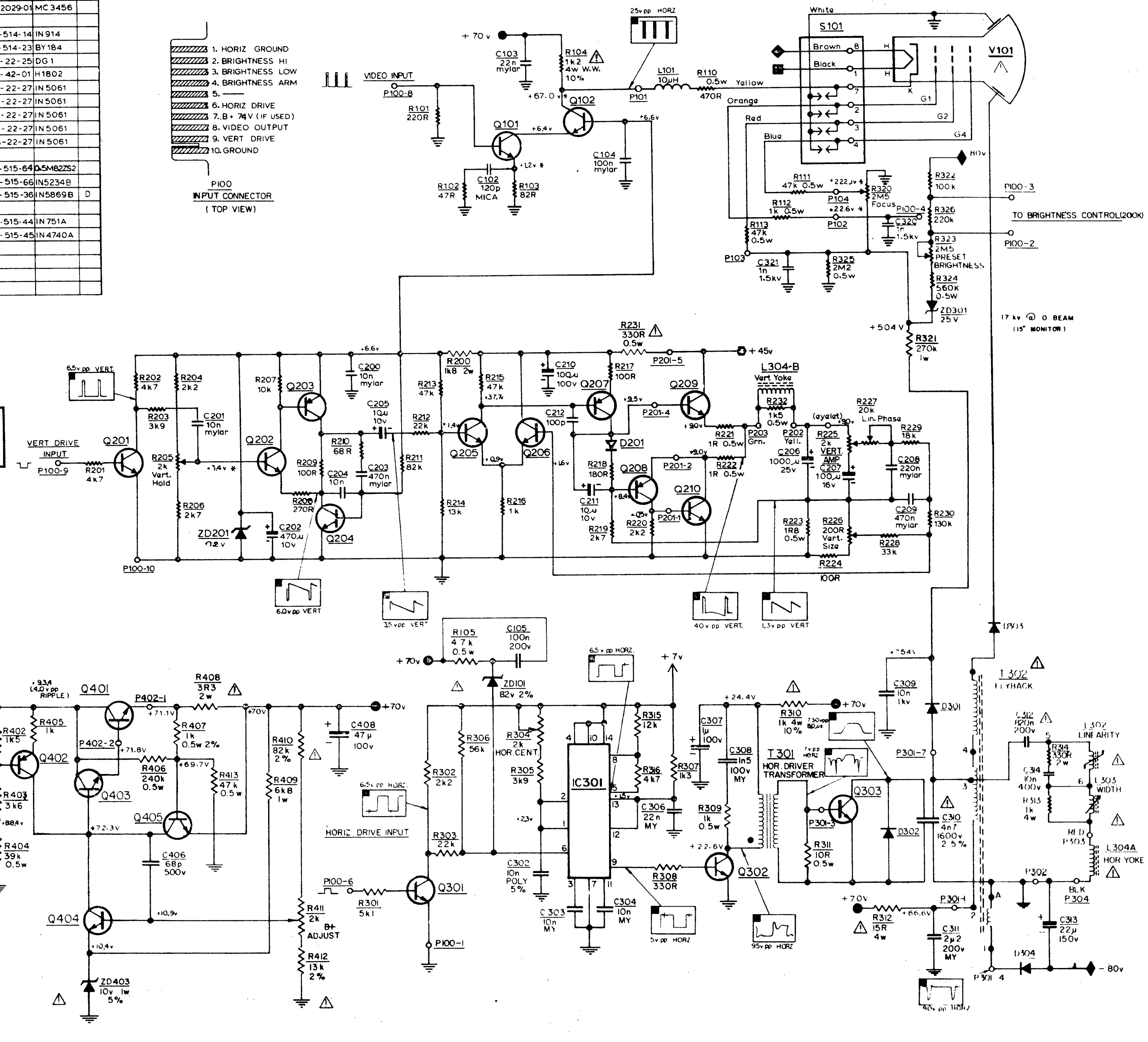
sym	FUNCTION	ELEC. PART No.	JEDEC/ HOUSE No.	type	sym	FUNCTION	ELEC. PART No.	JEDEC OR HOUSE No.	type
Q 101	VIDEO PREAMP	14-800-32	MPS6514	A	IC 301	HORIZ DELAY	14-2029-01	MC 3456	
Q 102	VIDEO OUTPUT	14-904-12	MPS U10	F					
					D 201	VERT BIAS	14-514-14	IN 914	
Q 201	VERTICAL PREAMP	14-802-12	TIS 98	A	D 301	FOCUS RECTIFIER	14-514-23	BY 184	
Q 202	VERT & TRIGGER	14-802-12	TIS 98	A	D 302	FLYBACK DAMPER	28-22-25	DG 1	
Q 203	MILLER INTEGRATOR	14-808-12	TIS 101	A	D 303	EHT RECTIFIER	28-42-01	H1802	
Q 204	MILLER INTEGRATOR	14-822-12	TIS 97	A	D304	B- FOCUS SUPPLY	28-22-27	IN 5061	
Q 205	DIFFERENTIAL AMP	14-811-32	SPS5449	B	D 401	B+ POWER SUPPLY	28-22-27	IN 5061	
Q 206	DIFFERENTIAL AMP	14-802-12	TIS98	A	D 402	B+ POWER SUPPLY	28-22-27	IN 5061	
Q 207	VERT DRIVER	14-861-12	S 24615	A	D403	B+ POWER SUPPLY	28-22-27	IN 5061	
Q 208	VERT DRIVER	14-861-12	S 24615	A	D 404	B+ POWER SUPPLY	28-22-27	IN 5061	
Q 209	VERT OUTPUT	14-601-23	SJ 5461	E					
Q 210	VERT OUTPUT	14-601-23	SJ 5461	E	ZD 101	82V HOLD DOWN ZEN.	14-515-64	0.5M82ZS2	
Q 301	TRIGGER AMP	14-802-12	TIS 98	A	ZD 201	6.2V ZENER B+	14-515-66	IN5234B	
Q 302	HORIZ DRIVER	14-904-12	MPSU10	F	ZD 301	25V SPOT KILL. ZEN.	14-515-36	IN5869B	D
Q 303	HORIZ OUTPUT	14-601-36	2SC1413	E					
Q 401	REGULATOR	14-601-26	2N5240	E	ZD402	5.1V REF. ZENER	14-515-44	IN 751A	
Q 402	PRE-REGULATOR	14-823-32	2N5400	B	ZD403	10V REF. ZENER	14-515-45	IN 4740A	
Q 403	REG. DRIVER	14-904-12	MPSU10	F					
Q 404	ERROR AMP	14-904-12	MPSU10	F					
Q 405	CURRENT LIMITER	14-802-12	TIS 98	A					

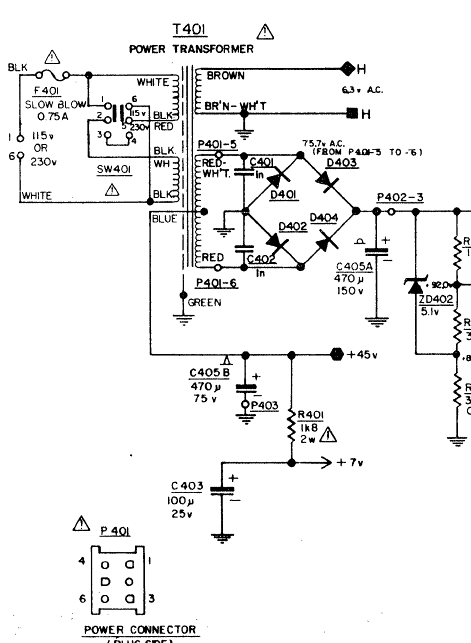
RESISTORS – RESISTANCE IN OHMS, k (KILOHMS), OR M (MEGOHMS) 1/4 WATT, 5% TOLERANCE UNLESS OTHERWISE NOTED.

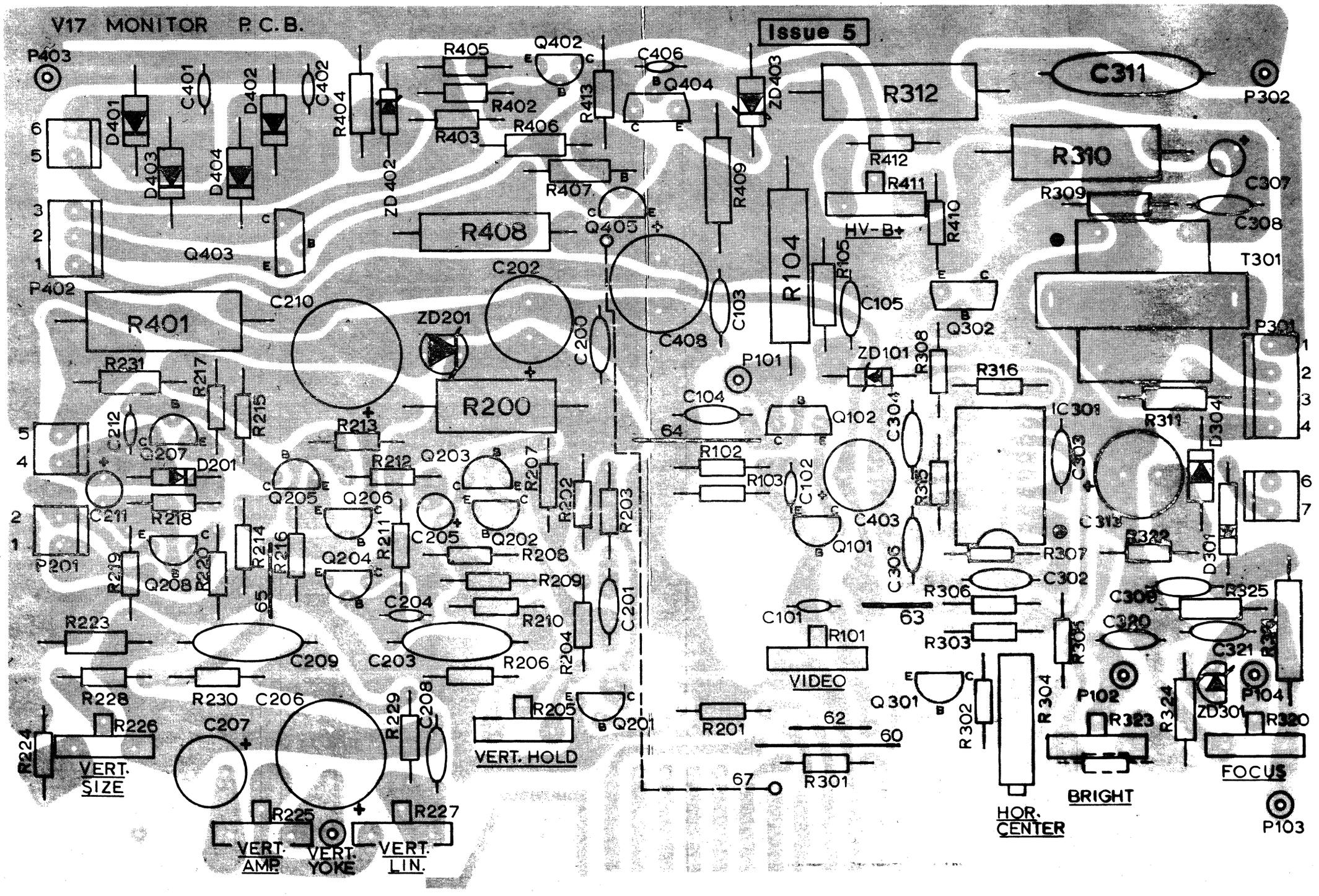
CAPACITORS – CAPACITY IN p (PICOFARADS), n (NANOFARADS), OR μ (MICROFARADS) D.C.W.V. AND TOLERANCE NOTED WHERE CRITICAL.

CAUTION FOR CONTINUED SAFETY REPLACE COMPONENTS INDICATED BY ⚠ WITH EXACT REPLACEMENT COMPONENTS ONLY. CONSULT SERVICE MANUAL PARTS LIST SECTION "SAFETY COMPONENTS"

* DEPENDS ON CONTROL SETTINGS AND / OR SIGNAL CONDITION.






V17 MONITOR P.C.B.
Issue 5
P403
P402
P201
D401
D403
D404
D402
C401
C402
Q403
R404
ZD402
R405
R402
R403
Q402
R406
R407
C406
Q404
R413
R408
Q405
ZD403
R409
R312
C311
P302
R310
R412
R411
R410
HV-B+
C307
C308
R309
T301
R104
R105
C105
C103
C408
C202
ZD201
C200
R401
C210
R231
R217
R215
R213
R200
P101
ZD101
R308
R316
Q302
P301
C104
Q102
R102
R103
C102
C403
C301
IC301
C303
R311
D304
R315
C305
Q101
C313
R322
R307
D301
C302
R306
R303
C101
R101
63
VIDEO
C309
R325
C320
C321
R321
R305
R304
Q301
R302
P102
R323
R324
ZD301
R320
P104
FOCUS
P103
BRIGHT
HOR. CENTER
62
60
67
R301
R201
Q201
R205
VERT. HOLD
C201
R204
R206
C203
C204
R208
R209
R210
C205
Q202
Q203
R212
R207
R202
R203
Q204
Q205
Q206
R211
R214
R216
65
C212
Q207
D201
R218
C211
R219
Q208
R220
R223
C209
R228
R230
C206
C207
R226
R224
VERT. SIZE
R225
R227
C208
R229
VERT. AMP.
VERT. YOKE
VERT. LIN.

SERVICE REPLACEMENT PARTS LIST

CHASSIS ASSEMBLY (02-210233-03)*

SYMBOL	DESCRIPTION	PART NUMBER
Q 209	Vertical Output Transistor, SJ5461	14-601-23
Q 210	Vertical Output Transistor, SJ5461	14-601-23
Q 303	Horizontal Output Transistor, 2SC1413	14-601-36
Q 401	Regulator Power Transistor 2N5840 select.	14-601-26
D 302	Damper Diode, DG1	28-22-25
D 303	HV Rectifier 30KV, H1802	28-42-01
F 401	.75A 125V Fuse	27-5-28
L 101	10 MH Coil	21-1400-06
L 302	Linearity Coil	21-1428-01
L 303	Width Coil	21-1427-01
L 304	Deflection Yoke	21-244-01
T 302	Flyback Transformer	21-243-01
T 401	Power Transformer	24-10197-03
SW 401	Line Switch	26-230-01
	Heat-shrinkable Sleeving, .187 ID	20-300013-04
	Heat-shrinkable Sleeving, .750 ID	20-300013-08
	Cable Tie	33-523-01
	Clip - PCB Support	33-629-01
	Fuse Holder	34-198-01
	CRT Socket	34-213-11
TS1, 2	Terminal Strip, Fire Retardent	34-491-03
	Transistor Socket	34-515-03
P 201	Connector Housing	34-549-05
P 402	Connector Housing	34-549-06
P 301	Connector Housing	34-549-07
	Crimp Terminal	34-550-01
	Anode connector with spring	34-678-01
P 401	Power connector housing	34-677-06
	Pin Terminal	34-676-21
	Transistor Cover	39-1151-01
C 405	Electrolytic 470, 470 uF/150, 75v	44-202-37
C 314	10 NF 400v capacitor	48-121034-01
C 312	820 NF 200v capacitor	49-19-26
C 310	4N7 1600v Safety Cap	49-24-06

* Not a replacement or stock item

MONITOR PCB ASSEMBLY

SYMBOL	DESCRITPION	PART NUMBER
D 201	Signal Diode, 1N914	14-514-14
D 301	Signal Diode, 1800 Piv, BY 184	14-514-23
D 304, 401, 402, 403, 404	Rectifier 1A 600v, 1N5061	28-22-27
ZD 101	82v 2% Zener Diode, 0.5M82ZS2	14-515-64
ZD 201	6.2v Zener Diode, 1N5234B	14-515-66
ZD 301	25v 5% Zener Diode, 1N5869B	14-515-36
ZD 402	5.1v 5% Zener Diode, 1N751A	14-515-44
ZD 403	10v 5% Zener Diode, 1N4740A	14-515-45
Q 101	Small Signal Transistor, MPS 6514	14-800-32
Q 201, 202 206, 301 405	Small Signal Transistor, T1S 98	14-802-12
Q 203	Small Signal Transistor, T1S101	14-808-12
Q 205	Small Signal Transistor, SPS5449	14-811-32
Q 204	Small Signal Transistor, T1S97	14-822-12
Q 402	Small Signal Transistor, 2N5400	14-823-32
Q 207, 208	Small Signal Transistor, S24615	14-861-12
Q 102, 302 403, 404	Plastic Power Transistor, MPSU10	14-904-12
IC 301	Double one-shot IC, MC3456	14-2029-01
T 301	Horizontal Buffer Transformer	24-170001-04
R 304	Cermet Trim Pot 2K	41-328-01
R 226	Carbon Trim Pot 200R	41-299-16
R 205, 225 411	Carbon Trim Pot 2K	41-299-12
R 227	Carbon Trim Pot 20K	41-299-01
R 320, 323	Carbon Trim Pot 2M5	41-299-07
R 408	Critical Safety Resistor, 3R3 5% 2W	42-63-54
R 312	15R 4W 10% Resistor	42-111501-03
R 310	1K 4W 10% Resistor	42-111021-03
R 104	1K2 4W 10% Resistor	42-111221-03
C 307	1uF 100v Electrolytic	44-310508-01
C 205, 211	10 uF 10v Electrolytic	44-310002-01
C 313	22 uF 150v Electrolytic	44-322009-05

SYMBOL	DESCRIPTION	PART NUMBER
C 408	47 uF 100v Electrolytic	44-347008-08
C 403	100 uF 25v Electrolytic	44-310104-04
C 207	100 uF 16v Electrolytic	44-310103-12
C 210	100 uF 100v Electrolytic	44-310108-06
C 202	470 uF 10V Electrolytic	44-347102-04
C 206	1000 uF 25v Electrolytic	44-310204-10
C 212	100 pF 25p 10% 50v Capacitor	46-310113-51
C 102	120 pF 5% Mica Capacitor	47-41215-05
C 204	10NF 10% Polypropelene Capacitor	48-131031-11
C 406	68 pF 10% 500v Capacitor	46-368013-02
C 401, 402	1NF 10% 25P 500v Capacitor	46-310213-06
C 320, 321	1NF 20% Z5V 1500v Capacitor	46-510228-74
C 309	10NF 1kv Capacitor	46-510311-37
C 308	1.5NF 100v Mylar Capacitor	48-171521-22
C 200, 303, 304, 201	10NF 10% 200v Mylar Capacitor	48-171032-22
C 103, 306	22NF 10% 200v Mylar Capacitor	48-172232-22
C 104, 105	100NF 10% 200v Mylar Capacitor	48-171042-22
C 208	220NF 10% 200v Mylar Capacitor	48-172242-22
C 203, 209	470NF 10% 200v Mylar Capacitor	48-174742-22
C 311	2.2, uF 20% 200v Mylar Capacitor	48-172252-51
C 302	10NF 5% Polypropelene Capacitor	48-181032-04
	Monitor P.C.B. (less components)	50-1568-01

SAFETY COMPONENTS

For continued reliability and safety, the following components should be replaced with Electrohome parts:

V 101	Picture tube, 15"	17-6152-03 or -04
R 104	1k2 4W Wirewound Resistor	42-111221-03
ZD 101	82v 2% Zener Diode	14-515-64
R 231	330R .5W 5% Carbon Comp. Res.	40-223315-13
R 310	1K 4W Wirewound Resistor	42-111021-03
R 312	15R 4W Wirewound Resistor	42-111501-03
C 310	4N7 1600v Critical Safety Cap.	49-24-06
T 302	Flyback Transformer	21-243-01
L 304	Deflection Yoke	21-244-01
F 401	.75A 125v slow-blow Fuse	27-5-28
T 401	Power Transformer	24-10197-03
SW 401	Line Switch	26-230-01
R 401	1k8 2W 5% Resistor	40-621825-01
R 408	3R3 2W 5% Resistor	42-63-54

All safety components are marked with △ on the schematic.

AES

printer

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 SCOPE AND ORGANIZATION OF THIS MANUAL

This manual provides information for installation, operation, and maintenance of the Qume Sprint Micro 3 Series Printers. Complete procedures for repair are included with schematic diagrams and an illustrated parts list to aid the maintenance technician.

This chapter provides a brief description of the printer and lists its capabilities. In Chapter II you will find descriptions for unpacking and initial installation. Chapter III describes the theory of operation in sufficient detail to allow troubleshooting and repair of the printer.

A consolidated list of support equipment is found in Chapter IV. Listed in this chapter are the special tools, test equipment, spare parts, and miscellaneous items required in routine servicing of the printer.

Chapter V outlines routine maintenance and sets forth a recommended schedule of cleaning, lubrication, and adjustment.

Troubleshooting is covered in Chapter VI. This section describes procedures for locating faults within the mechanical and electrical portions of the printer. Procedures are given to enable the service technician to isolate faults to the board level.

Repair techniques are discussed in Chapter VII. Procedures for removal and replacement of defective components are described, as well as detailed mechanical alignment.

Chapter VIII contains an illustrated parts list, showing the mechanical portion of the printer. This serves to identify parts for ordering purposes and also serves as an assembly guide during servicing of the printer.

Complete wiring and schematic diagrams are provided in Chapter IX as well as assembly drawings for the printed circuit boards.

1.1 DESCRIPTION OF THE PRINTER

The Sprint Micro 3 Series Printer is a high-performance, low-cost printer intended for use in automatic data systems. Its light weight and compactness, its ease of operation and dependability are important features in any application calling for a printer with intermediate output capacity. Such applications include small business systems in which printers constitute the principle output device, as well as larger data systems calling for a flexible terminal printer with high-quality print. The printwheel provides a full 96-character set, with a variety of optional type styles. Upper and lower case alphabetic characters are provided together with numeric and special characters.

On typical sequential text, the printer attains print speeds as high as 55 characters per second. The usefulness of the printer is not restricted to the line-sequential output, however. Both the vertical and horizontal placement of each character are under program control, with four degrees of freedom (right and left carriage movement; forward and reverse paper movement). A unique method of optical control permits accurate character placement. These features make the Sprint Micro 3 Series Printer suitable for X-Y plotting, and for applications where it is more convenient to have random output rather than conventional left-to-right or top-to-bottom operation. Character placement is done is increments of 1/120th inch horizontally and 1/48th inch vertically. Horizontal displacements up to 13.1 inches and vertical displacements up to 21.3 inches may be programmed.

Control and data interface are fully TTL-compatible. The printer uses a 13-bit weighted data bus and three unweighted strobe lines to enter the data into the printer input buffer. The strobe lines distinguish the operation to be performed and initiate the appropriate action on the part of the printer.

Miscellaneous input functions include Printer Select, Ribbon Lift, and Restore (a "reset" function following a "check" condition such as a carriage or printwheel travel malfunction or power supply failure). Status outputs are also included, allowing the external data source to monitor printer functional status.

Perhaps the most significant feature of the printer is its mechanical simplicity. Mechanical functions have been replaced by electrical functions wherever possible, and the mass and inertia of the mechanism has been minimized through the use of lightweight components. Electrical reliability is enhanced through the us of LSI (large-scale integration) components in the input and control circuits. By minimizing the number of electrical and mechanical components, Qume has produced an exceptionally fast, quiet, and reliable serial printer. Plug-in serviceability permits on-site repair and minimum downtime.

1.2 SPECIFICATIONS

TABLE 1-1

PRINT SPEED:	Qume printer speed varies according to the sequence of characters being printed and whether the various capabilities of the printer (high speed electronic tab, printing right to left, etc.) are used properly. Speeds shown below are for average English text on one line, with electronic tab over spaces between words, and are shown in characters per second (cps).

Sprint Micro 3/35:	35 cps
Sprint Micro 3/45:	45 cps
Sprint Micro 3/55:	55 cps
Sprint Micro 3/X30:	30 cps (metallized wheel)
Sprint Micro 3/X40:	40 cps (metallized wheel)
Sprint Micro 3/WideTrack:	40 cps

TABLE 1-1
(continued)

PRINT:	Full character of electric typewriter quality, printed serially: variable intensity ballistic hammer automatically adjusts to one of six intensities according to character size.
FORMS:	Single sheets and continuous forms, with or without sprocket holes. The Sprint Micro 3 printers maximum forms width is 15 inches (38.1 cm). WideTrack maximum forms width: 28 inches (71.1 cm).
FONT:	96 CHARACTER POSITIONS ON "daisy" printwheel: Wide variety of standard font styles in 10 and 12 pitch and proportional spacing.
FORMAT:	Horizontal: Sprint Micro 3: 132 columns at 10 characters per inch; 158 columns at 12 characters per inch; left or right. Electronic tabbing and carriage return up to 13.1 inches (33.3 cm). Vertical: Spacing in increments of 1/48th inch, up or down: slew rate at 5 inches (12.7 cm) per second. WideTrack slew rate: 5 inches (10.2 cm) per second.
PLOTTING:	Resolution of 5760 points per square inch.
PAPER FEED:	Pressure Platen: pin feed platens, forms tractor, optional.
RIBBON:	Easy to handle cartridge with multi-strike carbon, single strike carbon or fabric ribbon.
PRINTWHEEL:	Easily operator changeable.
OPERATOR CONTROLS:	Horizontal forms positioning; vertical forms positioning; forms thickness; ribbon advance.
TEMPERATURE:	Operating 50 to 105 degrees F (10 to 40 degrees C). Storage -40 to 170 degrees F (-40 to 76 degrees C).
HUMIDITY:	Operating 10% to 90% RH (no condensation). Storage 2% to 98% RH (no condensation).
PHYSICAL:	Sprint Micro 3 Weight: 28 pounds (12.7 kg) Width: 23.63 inches (60 cm) Height: 7.11 inches (18 cm) Depth: 13.5 inches (34.3 cm)

1.2 SPECIFICATIONS (continued)

TABLE 1-1
(continued)

PHYSICAL:	WideTrack Weight: 37.2 pounds (16.9 kg) Width: 36.5 inches (92.8 cm) Height: 7.11 inches (18 cm) Depth: 13.5 inches (34.3 cm)
DATA INPUT:	13-bit parallel TTL levels plus control lines.
POWER REQUIREMENTS:	(For all Sprint Micro 3 Models.) + 5 VDC ± 3% 3.5 amps DC +15 VDC ± 10% 4.5 amps average (14 amps peak 20 ms max.) -15 VDC ± 10% 4.5 amps average (14 amps peak 20 ms max.)
INTERFACE CONNECTORS:	Power: Molex #09-01-1121 Data and control: 3M #3415-0000 Dual 25-pin PC edge connector
OPTIONS:	End of ribbon detector Out of paper detector Top of form Bottom feed slot
ACCESSORIES:	Friction platen Pin feed platen Forms tractor Receive-only printer cover Keyboard printer cover Power supply

CHAPTER II

RECEIVING

2.0 INTRODUCTION

This chapter describes installation of the Sprint Micro 3 Series Printers, including receiving, quality assurance inspection, and electrical interface.

2.1 RECEIVING

Each printer is shipped in an individual carton. The following items are included:

Printer Assembly
Power Connector (Part number 80033)
Hole Plugs (Printer with covers only)
Interface Connector Hood (Part number 80034)

Remove the printer from its shipping carton:

(1) Inspect the container for external signs of damage. If any damage is observed, have the delivery agent note the damage on the shipping document.

(2) Open the outer container and remove the inner carton.

(3) Open the inner carton from the top and remove the cardboard spacer. The printer, bolted to its shipping pallet and wrapped in plastic, may now be withdrawn.

(4) Remove the plastic bag surrounding the printer.

(5) Using a wrench, remove the four screws securing the printer to its shipping pallet.

(6) Install hole plugs in the printer cover (if ordered) in holes vacated by pallet screws.

(7) Remove any paper wrapped around the platen.

(8) Remove the top front cover.

(9) Using diagonal cutting pliers, cut and remove the two plastic ties used to secure the paper bail during shipping.

(10) Cut and remove the plastic tie used to secure the carriage assembly to the printer chassis.

(11) Examine the packing material closely to ensure that any small items ordered have been recovered (e.g. Power Connector Assembly #80033 or Logic Connector Hood Assembly #80034).

2.1 RECEIVING (continued)

(12) Retain all packing materials for possible reshipment.

Inspect the printer for scratches, dents, loose or damaged parts or other signs of damage. Note any evidence of such damage on the invoice, and file a claim with the carrier immediately, if the condition of the unit so warrants.

Remove the middle cover of the printer, and inspect the interior of the entire unit. Look for loose or broken parts, evidence of electrical damage, or other signs of damage. Be sure that all printed circuit boards are seated securely in their sockets by pressing down on each one of the boards.

If damage that might impair printer operation is detected, do not attempt to operate the printer. Contact Qume for advice and instructions.

Install a ribbon cartridge and printwheel on the Carriage Assembly (refer to Operator's Manual). The unit is now ready for electrical inspection and testing.

2.2 INSTALLATION

The following paragraphs outline procedures for installing the printer.

2.2.1 POWER CONNECTIONS

The printer requires three power supply voltages, as listed in Table 2-1. Qume offers two power supplies (Model 530 and Model 531) that are designed to run our printers. Seperate modular power supplies having the required characteristics may be used.

TABLE 2-1

POWER REQUIRED

SUPPLY/TOLERANCE	CURRENT REQUIRED
+15 VDC ± 10%	4.5 amps avg/14 amp peaks - 20 msec max.
-15 VDC ± 10%	4.5 amps avg/14 amp peaks - 20 msec max.
+ 5 VDC ± 3%	3.5 amps

All voltages must reach 90% of their final values in no less than 4 msecs and no more than 100 msecs. The absolute values of the +15 and -15 volt input must not differ by more than 2.0 volts during their rise or fall. The +5 volt input must reach 90% of its final value within 50 msecs of the +15 and -15 volt input.

All power connections are made through a single connector (Molex #09-01-1121-1), which attaches to a corresponding connector (see Figure 2-1) on the left side of the printer, viewed from the rear. Pin allocations on the power connector are given in Table 2-2. Note that seperate lines for high and low current supply distributions must be provided for all three supplies to prevent noise from being

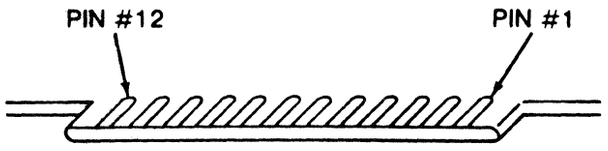
2.2.1 POWER CONNECTIONS (continued)

coupled from the carriage and printwheel motor drive circuits into the signal processing circuits. It is suggested that the recommended wire sizes (see Table 2-2) be used for installation. For proper noise isolation, the +5 V logic supply return path must be isolated from the +15 V and -15 V supply ground return paths in the power supply and the power cable.

TABLE 2-2

POWER CONNECTOR

POWER	PIN	WIRE SIZE
+15V High Current	3,4	2x18 AWG
+15V Low Current	6	1x18 AWG
-15V High Current	1,2	2x18 AWG
-15V Low Current	5	1x18 AWG
+ 5V Logic Current	7,8	2x18 AWG
+ 5V Power Current	12	1x18 AWG
Ground	9, 10, 11	3x18 AWG (or 7/32" tinned copper braid)



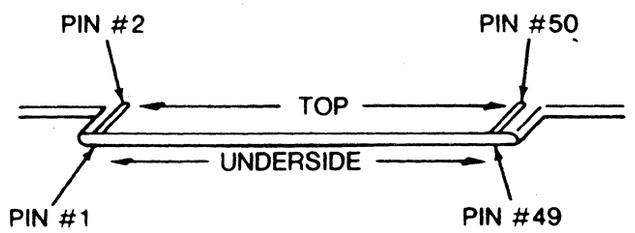
As Viewed From Rear Of Printer

FIGURE 2-1

POWER CONNECTOR (J2) ORIENTATION

2.2.2 DATA AND CONTROL CONNECTIONS

Input control and data signals are connected to the printer through J1 (right side of chassis viewed from the rear). The connector consists of a dual 25-pin edge card connector (0.1 inch contact centers). Recommended connector is 3M #3415-0000. Recommended interconnecting cable is 3M #3365, 50-conductor ribbon. Pin assignments on the control connector are given in Table 2-3 and shown in Figure 2-2.

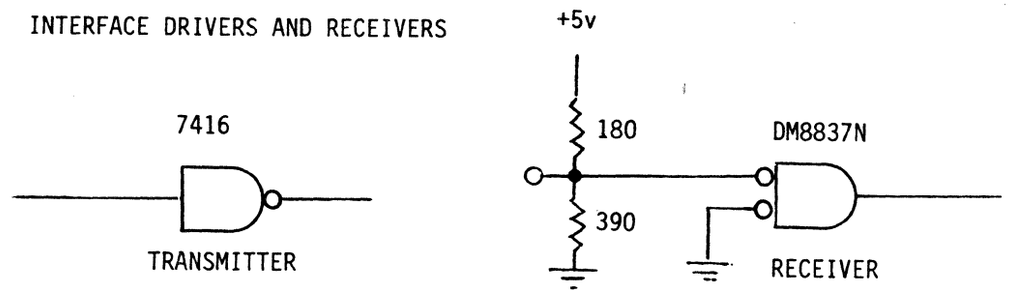


As Viewed From Rear Of Printer

FIGURE 2-2

CONTROL CONNECTOR (J1) ORIENTATION

INTERFACE DRIVERS AND RECEIVERS



All input/output signals are active low.
Logic: $\overline{<}$ 0.4V Logic: $\overline{>}$ 2.4V
Data 1/2 $\overline{\text{thru}}$ 2048 have 1K pull-up resistors and are received by 74412's.

TABLE 2-3

INTERFACE SIGNALS AND PIN ASSIGNMENTS

Connector: 3M #3415-0000

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	GND	26	TOP OF FORM (OPT)
2	DATA 1/2	27	GND
3	DATA 1	28	RIBBON LIFT COMMAND
4	DATA 2	29	GND
5	DATA 4	30	RIBBON OUT (OPT)
6	DATA 8	31	GND
7	DATA 16	32	PRINTER SELECT
8	DATA 32	33	GND
9	DATA 64	34	COVER INTERLOCK (OPT)
10	DATA 128	35	GND
11	DATA 256	36	GND
12	DATA 512	37	CHECK
13	DATA 1024	38	GND
14	DATA 2048 (OPT)	39	INPUT BUFFER READY
15	GND	40	GND
16	RESTORE	41	INPUT BUFFER READY
17	GND	42	GND
18	CHARACTER STROBE	43	INPUT BUFFER READY
19	GND	44	GND
20	CARRIAGE STROBE	45	(Not Used)
21	GND	46	GND
22	PAPER FEED MAIN STROBE	47	PRINTER READY
23	GND	48	GND
24	PAPER FEED AUXILIARY STROBE (OPT)	49	PAPER OUT (OPT)
25	GND	50	GND

NOTE

Pin 39 was previously named CHARACTER READY.
Pin 41 was previously named CARRIAGE READY.
Pin 43 was previously named PAPER FEED RIGHT READY.

These three signals have been consolated (but gate isolated) and occur simultaneously. Only one of these INPUT BUFFER READY lines needs to be tested prior to each CHARACTER, CARRIAGE or PAPER FEED STROBE.

All input/output signals are active low. Logic 1: $\leq$ 0.4Volts Logic 0: $\geq$ 2.4Volts

2.2.3 BASIC SIGNAL INPUTS

PRINTER SELECT LINE (Pin 32)

This signal is used to select the printer for operation, and enables the input and output lines in the interface. All interface lines are disabled until the select line is low.

RESTORE (Pin 16)

This signal initiates a restore sequence, normally following a printer malfunction or power failure which causes a "check" condition (see Basic Signal Outputs). The restore sequence consists of positioning the carriage at the leftmost position, synchronizing the printwheel, and resetting the carriage, printwheel, and interface logic. The internal "check" circuits are also reset.

DATA LINES (Pins 2 - 14)

These thirteen lines contain binary-coded information representing an ASCII character, a carriage movement command, or a paper feed command.

When representing an ASCII character, only the low-order seven lines (D1-D64) are used; the remaining lines are ignored. Refer to Table 2-5 for a cross-reference between printwheel addresses and ASCII inputs.

When representing a carriage movement command, the eleven low-order bits designate the distance the carriage is to be moved in multiples of 1/60th of an inch. The D-1/2 bit indicates 1/2 times 1/60th, or 1/120th of an inch. A value of six is required for one character at 10 character/inch. The high-order bit (1024) determines the direction of carriage travel. If this bit is a logic "0" the carriage travels to the right; if a logic "1" the carriage travels to the left. D2048 bit is used in the WideTrack model to represent 1024 steps.

When representing a paper feed command, the ten low-order bits designate the number of vertical position increments to be moved, in multiples of 1/48th of an inch. The high-order bit (1024) determines the direction of paper movement; a logic "0" moves the paper upward, and logic "1" moves the paper downward.

CHARACTER STROBE (Pin 18)

When this signal is pulled low with valid character data on the data lines, the character data will be transferred into the input buffer register. Timing is shown in Figure 2-3.

CARRIAGE STROBE (Pin 20)

This signal enters carriage movement data into the input buffer when pulled low.

2.2.3 BASIC SIGNAL INPUTS (continued)

RIBBON LIFT COMMAND (Pin 28)

This signal raises and lowers the ribbon. If the level on this line is high (false), the ribbon will drop to the lower position; if the level is low (true), the ribbon will be raised to the printing position.

PAPER FEED MAIN STROBE (Pin 22)

When pulled low this signal enters paper movement data into the input buffer in operations where a single platen is used, or enters righthand platen movement data when the split platen option is installed.

PAPER FEED AUXILARY STROBE (Pin 24)

When pulled low this signal enters left platen paper movement data when the split platen option is installed.

TOP OF FORM COMMAND (Pin 26) (ROM Version Only)

This signal advances the paper to its starting point at the Top Of Form. There is sixteen programmable lengths of form feed available. The length of form to be used should be programmed prior to applying the TOF strobe by initiating a character strobe co-incidental with the ASCII FF code with data bits D128, D256, D512 and D1024 determing the length of feed. See Table 2-4. If FF code is not used, the Top Of Form increment will automatically be set at eleven inches.

Character Strobe	D1	0
ASCII FF Code	D2	0
	D4	1
	D8	1
	D16	0
	D32	0
	D64	0
	*D128	A
	*D256	B
	*D512	C
	*D1024	D

TABLE 2-4

TOP-OF-FORM

DATA BITS OF FF COMMAND				FORM LENGTH (INCHES)
D1024	D512	D256	D128	
0	0	0	0	11 Note 2
0	0	0	1	3
0	0	1	0	3.5
0	0	1	1	4
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	8.5
1	0	1	0	9
1	0	1	1	10
1	1	0	0	11-2/3 (70 lines)
1	1	0	1	12
1	1	1	0	14
1	1	1	1	17

Notes:

1. Other data bits in command are (D64 to D1): 0001100.
2. Eleven inches is the default value after a Restore command.

TABLE 2-5

ASCII CODE

CHAR-ACTER	ASCII BINARY CODE	ASCII HEX CODE	DECIMAL PRINTWHEEL ADDRESS	RELATIVE HAMMER FORCE	RIBBON ADVANCE
A	1000001	41	022	5	4
B	1000010	42	016	5	4
C	1000011	43	020	4	3
D	1000100	44	044	5	4
E	1000101	45	030	4	3
F	1000110	46	018	4	3
G	1000111	47	048	5	4
H	1001000	48	034	5	4
I	1001001	49	040	4	3
J	1001010	4A	058	5	3
K	1001011	4B	056	5	4
L	1001100	4C	042	4	3
M	1001101	4D	012	6	4
N	1001110	4E	038	5	4
O	1001111	4F	036	5	4
P	1010000	50	052	4	3
Q	1010001	51	054	5	4
R	1010010	52	026	5	4
S	1010011	53	028	4	3
T	1010100	54	032	4	4
U	1010101	55	046	5	4
V	1010110	56	060	4	4
W	1010111	57	008	6	4
X	1011000	58	064	5	3
Y	1011001	59	050	4	4
Z	1011010	5A	014	4	4
a	1100001	61	168	4	4
b	1100010	62	156	4	3
c	1100011	63	158	4	3
d	1100100	64	152	4	3
e	1100101	65	166	3	3
f	1100110	66	178	3	3
g	1100111	67	148	4	3
h	1101000	68	174	4	3
i	1101001	69	170	3	3
j	1101010	6A	144	3	3
k	1101011	6B	186	4	3
l	1101100	6C	154	3	3
m	1101101	6D	142	6	4
n	1101110	6E	164	4	3
o	1101111	6F	160	4	3
p	1110000	70	180	4	4
q	1110001	71	184	4	4
r	1110010	72	162	4	3
s	1110011	73	176	4	3
t	1110100	74	172	4	3
u	1110101	75	182	4	3
v	1110110	76	146	3	4

TABLE 2-5

ASCII CODE *(continued)*

CHAR-ACTER	ASCII BINARY CODE	ASCII HEX CODE	DECIMAL PRINTWHEEL ADDRESS	RELATIVE HAMMER FORCE	RIBBON ADVANCE
w	1110111	77	000	5	4
x	1111000	78	150	4	3
y	1111001	79	188	4	4
z	1111010	7A	190	4	3
0	0110000	30	074	4	3
1	0110001	31	066	3	3
2	0110010	32	068	4	3
3	0110011	33	070	4	3
4	0110100	34	072	4	3
5	0110101	35	076	4	3
6	0110110	36	078	4	3
7	0110111	37	080	4	3
8	0111000	38	082	4	3
9	0111001	39	084	4	3
¢	0100000	20	004	4	3
!	0100001	21	136	3	2
"	0100010	22	140	2	3
#	0100011	23	092	4	3
$	0100100	24	088	5	3
%	0100101	25	094	6	4
&	0100110	26	138	5	4
'	0100111	27	108	2	2
(	0101000	28	120	4	2
)	0101001	29	116	4	2
*	0101010	2A	122	3	3
+	0101011	2B	090	3	3
,	0101100	2C	006	1	2
-	0101101	2D	086	2	3
.	0101110	2E	010	1	2
/	0101111	2F	132	4	3
:	0111010	3A	024	1	2
;	0111011	3B	062	1	2
<	0111100	3C	114	3	3
=	0111101	3D	096	3	3
>	0111110	3E	100	3	3
?	0111111	3F	130	3	3
@	1000000	40	124	6	4
[	1011011	5B	106	4	2
\	1011100	5C	126	4	4
]	1011101	5D	102	4	2
^	1011110	5E	128	2	3
_	1011111	5F	110	1	5
`	1100000	60	112	2	2
{	1111011	7B	098	4	3
|	1111100	7C	118	4	2
}	1111101	7D	134	4	3
~	1111110	7E	104	3	3
¬	1111111	7F	002	2	3

NOTE: The character set shown in the preceding pages is that of the Prestige Elite 12 character set. The character faces will change with different fonts; however, the ASCII code relationship to the printwheel address location will always remain constant.

TABLE 2-6

HAMMER INTENSITY

HAMMER INTENSITY	HAMMER "ON" TIME (ms)
1	1.60
2	1.70
3	1.85
4	2.00
5	2.25
6	2.50

TABLE 2-7

PROPORTIONAL RIBBON ADVANCE

(RIBBON MOTOR STEPS)

CURRENT CHARACTER WIDTH (Ribbon Motor Steps)	LAST CHARACTER WIDTH (Ribbon Motor Steps)			
	5	4	3	2
5	5	4	4	3
4	4	4	3	3
3	4	3	3	3
2	3	3	3	2

2.2.4 BASIC SIGNAL OUTPUTS

These signals indicate the status of internal printer functions, and can be used by the external processor as flags for initiating data and control inputs.

PRINTER READY (Pin 47)

This signal indicates that the printer is ready to accept data and control inputs.

INPUT BUFFER READY (Pin 39) Previously called CHARACTER READY.
INPUT BUFFER READY (Pin 41) Previously called CARRIAGE READY.
INPUT BUFFER READY (Pin 43) Previously called PAPER FEED RIGHT READY.

These signals indicate that the printer is ready to accept an input command. These three signals have been consolidated (but gate isolated) and occur simultaneously. The INPUT BUFFER READY line must be tested before every character, carriage, and paper feed command. The input commands are stored in a single command hardware buffer and transferred to a 15 command, software controlled, first in/first out buffer.

(Pin 45) (Not Used)

CHECK (Pin 37)

This signal indicates that one or more printer malfunctions has occurred:

1. the carriage has been commanded to move, but no movement has been detected; or
2. the printwheel has been commanded to move, but, no movement has been detected; or
3. the power supplies have failed.

Under these circumstances, the CHECK signal will be true and no input commands will be accepted until the check condition has been cleared by clearing the malfunction and initiating a "restore" sequence.

PAPER OUT (Pin 49)

This signal indicates that the printer is out of paper. In printers not equipped with the paper out option, this line will always indicate a "paper available" condition.

2.2.4 BASIC SIGNAL OUTPUTS (continued)

RIBBON OUT (Pin 30)

This signal indicates that the printer is out of ribbon. This signal does not disable the printer. The RIBBON OUT line provides a status signal to the interface. In printers not equipped with the RIBBON OUT option, this line will always indicate a "ribbon available" condition.

COVER INTERLOCK (Pin 34)

This signal indicates that the printers top cover is in place. In printers not equipped with the COVER INTERLOCK, this line will always indicate the cover is in place.

2.2.5 TIMING CONSIDERATIONS

The timing diagram shown in Figure 2-3 illustrates the relationships between the data lines, the strobe input, and the internal ready line. The illustration shown is for a character input, but, the carriage and paper feed command timing is the same.

TYPICAL CHARACTER COMMAND SEQUENCE

The commands that are sent to the printer will be executed in order of receipt. A carriage motion and paper feed may be executed simultaneously. The character command inhibits any paper or carriage motion during the second portion of its execution cycyl. The print cycle is divided into two parts:

(1) Motion of the printwheel.

(2) Firing the printhammer.

Hammer firing will be executed only when the printwheel, carriage, and paper feed are all at rest. During the hammer firing cycle, and execution of the printwheel rotation, carriage movement and paper feed is deferred until completion of the hammer firing cycle. There is no restriction on overlapping printwheel motion, carriage movement and paper feed.

A carriage strobe followed by a character strobe will cause both the carriage and printwheel to move. Printing will occur when both the carriage and the printwheel are stopped. This is termed a space before print sequence.

TIMING

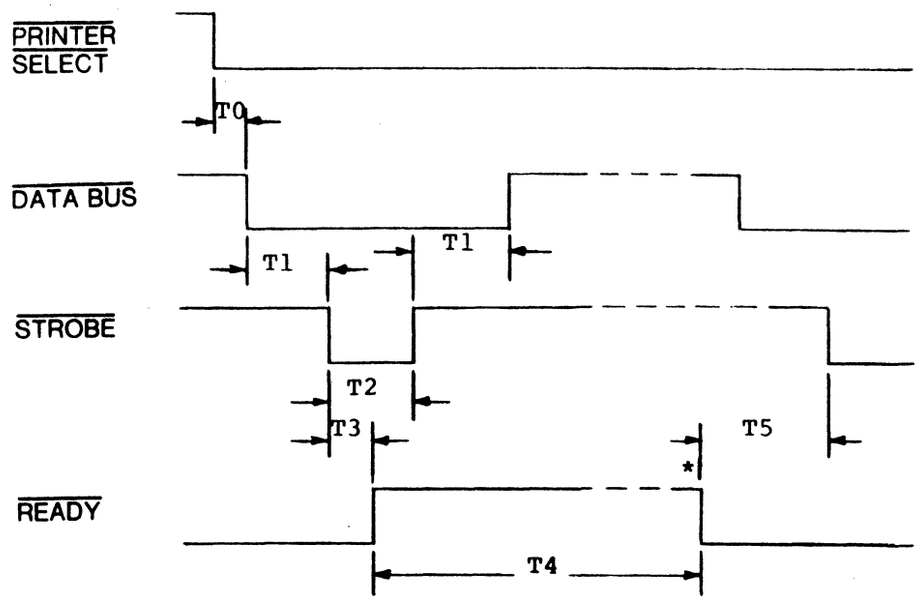


FIGURE 2-3

CONTROL TIMING

	T0 >	0 ns	
	T1 >	200 ns	
	T2 >	750 ns	*Any STROBE arriving during the time that the
250 ns <	T3 <	950 ns	INPUT BUFFER READY line is false (≥ 2.4 Volts)
	T4 >	20 usec	will be ignored.
	T5 >	000 ns	

The INPUT BUFFER READY lines will go false for 20 to 800 usec upon receipt of any strobe. If the input buffer is full, INPUT BUFFER READY lines will reamin false until completion of the command being executed. Commands are executed in order of receipt.

The Sprint Micro 3 Series Printers have a sixteen command input buffer. The character, carriage and paper feed commands are stored in a single-command hardware buffer and transferred to a 15 command software-controlled first in/first out buffer.

2.3 INITIAL PERFORMANCE CHECK

The ideal performance check is to install the printer in the system with which it will be used, and execute a suitable exercise routine.

An alternate performance test using the Qume Printer Exerciser (either bench or portable model) is described below:

(1) Connect the printer to the Power Supply. Turn power on and verify that supply voltages are within specification. On S3 printers check +5 V supply at test point indicated on P.C.B. #2; check +15 V supply at the emitters of carriage drive transistors Q2 and Q1 (Q2 and Q1 are mounted on the heat sink at the right rear of the printer frame).

+ 5 VDC ± 3%
+ 15 VDC ± 10%
- 15 VDC ± 10%

Turn power off.

Install any covers that have been removed.

(2) Connect printer to Printer Exerciser/Tester. Apply power and verify that the carriage "restores" to the extreme left limit at a moderate velocity.

(3) Press the ribbon advance switch on the printer and verify that the ribbon both lifts and advances correctly.

(4) Insert a piece of paper into the platen. Pull the feed roller release lever forward and verify that this allows the paper to be aligned. Push feed roller release lever to the rear.

(5) On printers ordered with cover assemblies and cover interlock switch, verify that removal of the top cover disables the printer (printer exerciser CHAR RDY, CARR RDY, PF RT RDY, and PF LFT RDY LED's will be OFF, only the PTR RDY LED will be ON). Replace top cover.

(6) If Top Of Form option has been ordered, verify that it works correctly. This function can be operated from the printer exerciser or, if ordered, from the "TOF" switch on the printer cover.

(7) Install a known good printwheel on the printwheel hub, making certain that the printwheel is fully seated. Secure the printwheel motor latch.

(8) Install a Qume MULTI-STRIKE carbon ribbon cartridge (Qume #80029-01) on the carriage assembly. Remove any slack in the ribbon by operating the printer's ribbon advance switch.

(9) Print one line of Test 5-1 from the exerciser. Verify that the characters are printed approximately as dark on their top and bottom, and on their right and left.

2.3 INITIAL PERFORMANCE CHECK (continued)

(10) Complete a 15 minute warm-up using printer exerciser Test 5-1 with vertical line spacing of six lines to the inch. Verify that print is equally dark through-out the printout (verifies proper ribbon advance).

In the Sprint Micro 3 Series printers the end of ribbon option does not disable the printer. The End of Ribbon option is only a status condition which provides a status signal to the interface. The Qume exerciser does not monitor this line.

An alternate check may be performed by grounding pin 2 of the 40 pin test point strip on P.C.B. #2. The printer should be powered down when securing a jumper between ground and pin 2. In this test the printer relies on a diagnostic test stored in its own micro processor memory. This test may be monitored and controlled by the Sprint Micro 3 ActivityMonitor (part #80740). For further explanation of this test and ActivityMonitor refer to chapter VI.

The diagnostic test performs the following:

(1) ROM test.

(2) I/O lines.

(3) Executes a restore.

(4) Carriage moves 114 times back and forth in diminishing movements.

(5) Printwheel moves 96 times clockwise and counter clockwise.

(6) Executes various combinations of forward and reverse paper feeds.

(7) Concludes test with "Self Test" printed vertically. Ribbon lift, hammer actuation and ribbon advance are exercised during this print cycle.

2.4 WARRANTY

Qume products are warranted free from defects in material and workmanship for a period of 90 days after delivery. Qume's obligation under this warranty is limited to replacing or repairing, at its option, at its factory, any of the products (except expendable parts thereof) that within the warranty period are returned to Qume and that are found to be defective in proper usage. Printers within warranty will be repaired at no charge. Buyer shall prepay transportation charges to the Qume factory.

Before returning materials to Qume, the customer must request a Material Return Authorization Number. Qume will only accept authorized Replacement Assemblies (see Service Policy) or complete printers for replacement or repair. Individual components will not be authorized for replacement or repair if removed from assemblies.

Qume will ship repaired or replaced assemblies to customers within 30 days from receipt of assemblies.

2.5 SERVICE POLICY

Qume will accept the assemblies listed below for repair at the charges shown. Any other parts and/or subassemblies will be accepted for repair at Qume's discretion.

FIXED FEE ITEMS:

Description	Charge
Printed circuit board (other than catastrophic failure)	$ 50.
Carriage motor encoder:	
In printer	$150.
Seperate assembly	$100.
Printwheel motor encoder:	
In carriage and in printer	$200.
In carriage only	$150.
Seperate assembly	$100.

All other items will be repaired on a time and materials basis, with time calculated at $35/hour and materials at list price.

The above prices are subject to change without notice.

TIME AND MATERIAL CHARGES:

Unless the customer advises to the contrary, Qume will request a purchase order for all estimated time and material charges before beginning any work.

SCHEDULES:

Qume will return repaired or replaced parts to customers within 30 days from receipt of parts. If the customer desires parts returned within three working days, a $50 expediting fee will be charged.

SHIPPING CHARGES:

Shipping charges will be prepaid by customer when parts are returned to Qume. Qume will return parts C.O.D.

LOCATION:

All repair work will be done at Qume's factory in Hayward, California, unless otherwise designated by Qume.

RETURN AUTHORIZATION:

Before returning materials to Qume, the customer must first request a Material Return Authorization number. The MRA number must be affixed to materials returned, as well as the shipping container.

2.6 TECHNICAL TRAINING POLICY

Training classes in the repair and maintenance of Qume printers are conducted on a regularly scheduled basis at Qume headquarters in Hayward, California.

Each scheduled class takes three days. The cost of this class is $210 per student, and covers all necessary course materials. Transportation, motel, and similar expenses are the responsibility of the student or his company.

To support its customers, Qume provides a number of free student/enrollments (one student for one three-day class) in these scheduled classes, according to the number of printers ordered:

Printers Ordered	Student/Enrollments
0 - 9	0
10 - 99	1
100 - 249	2
250 - 499	3
500 - 999	4
1000 - 1999	5

Note that these free student/classes apply only to regularly scheduled classes at Qume; they do not apply to special classes at Qume or at the customer's site.

In order to reserve an appropriate number of places in the class of their choice, customers should enroll at least three weeks in advance by contacting the Customer Training Department at Qume/Hayward. Schedules of classes are available from our local Qume salesman.

In some cases, it may be more convenient or lower in cost for the customer to schedule a special class at his location or at Qume. The following applies:

(1) Such classes will be scheduled according to the availability of a Qume instructor.

(2) Class size is limited to 12 students.

(3) Customer provides necessary training materials -- manuals, notebooks, etc., and a conference or classroom. Customer can buy our manuals or copy them for this purpose.

(4) Qume fee is $280/instructor day (class is usually 3 days) plus actual travel and living expenses (motel, car rental, meals, etc.), if any.

CHAPTER III
THEORY OF OPERATION

3.0 INTRODUCTION

This chapter describes both mechanical and electrical operating principles of the printer. The information contained in this chapter is intended to help the service technician understand the printer and thus facilitate maintenance and repair.

The description begins with the mechanisms involved in the various printer functions: paper feed, carriage motion, character selection, ribbon motion, and ribbon lift. Following this discussion is an introduction to the printer's overall operating principles and then a discussion of the electronic interface and microprocessor control section, the printwheel and carriage servosystems, and the paper and ribbon electronics. Also included is a discussion of miscellaneous functions such as the "check" circuit.

3.1 MECHANICAL OPERATION OF THE PRINTER

Mechanical operation of the printer can be compared to the operation of an office typewriter such as the Selectric® typewriter manufactured by IBM Corporation. In both the Qume printer and the Selectric® typewriter, there is a means of moving the carriage, selecting the character to be printed by rotating the type font, a way of striking the ribbon with the font, and a way of moving the paper, In the Qume printer, the means consists of rotating a "daisy" printwheel so that the correct die is alligned in the printing position, striking the die against a carbon or ink-impregnated ribbon, and creating an impression of the die on the paper. As a part of this cycle, the paper is also moved vertically as each line is printed.

®Selectric is a registered trademark of IBM Corporation.

A typewriter-style platen roller feeds paper and positions the paper vertically in front of the printing die. In the standard version of the printer, paper is held in place by pressure from spring-loaded pinch rollers mounted beneath the platen itself. The rubber surfaces of the platen and pinch rollers restrain the paper in a mechanism termed friction feed.

Pin feed and tractor feed are available optionally, as more positive methods of controlling paper movement. In the pin feed arrangement, sprocket wheels on either side of the platen engage pre-punched holes in the margins of the forms to be printed. In tractor feed printers a flexible driven belt engages the perforations in the margin of the form, replacing the platen as the driving mechanism.

Rotation of the platen moves the paper vertically, as shown in Figure 3-1. This is done manually during initial loading of paper into the printer paper feed mechanism, using the knobs provided on either side of the platen roller. Once the paper has been loaded, however, paper feed is automatic. A stepping motor and gear train mounted on the right side of the chassis engage the teeth of a drive gear attached to the platen's axial shaft. External commands, operating through the printer's electronics, control the stepping motor to move the paper in multiples of the basic 1/48th. inch increment. Each command may feed the paper up or down, a maximum of 21.3 inches in either direction.

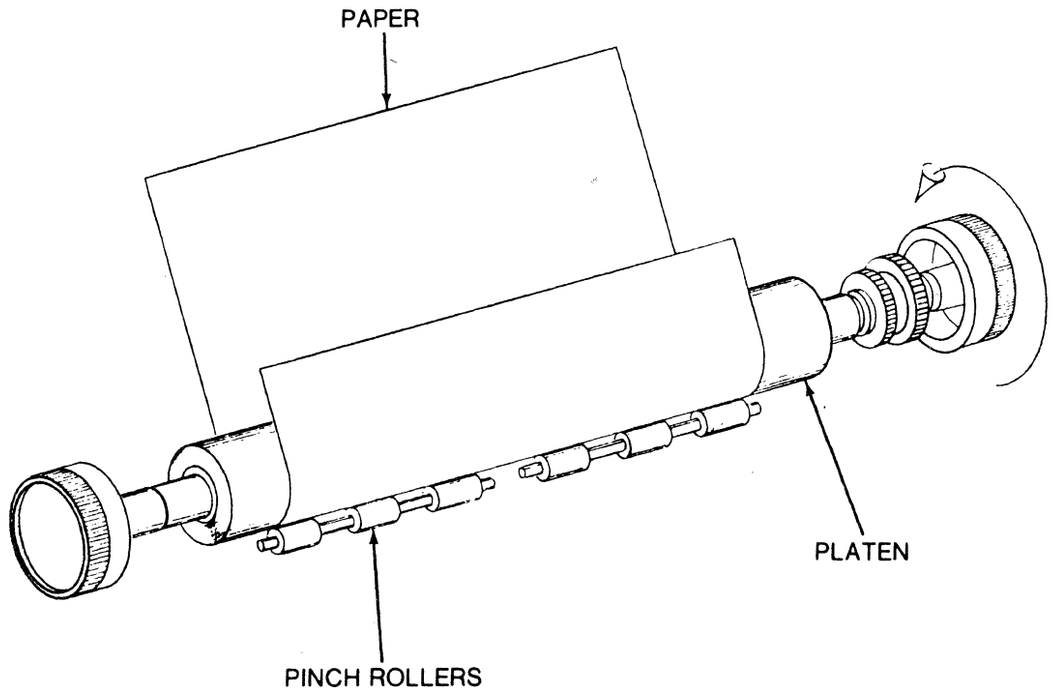


FIGURE 3-1
PAPER FEED DETAIL

An optional version of the printer provides independent left and right paper feed mechanisms. This version contains two half-width platens mounted on a common shaft, so that each may be rotated without affecting the other. The right-hand platen is driven by the standard paper feed mechanism, while the left-hand platen is driven by a similar mechanism installed on the left side of the printer chassis.

The dies used to print characters are molded into a light-weight plastic disk, called the printwheel. Ninety-six (optionally 94) spokes radiate from the center hub, and the tip of each spoke carries a relief image of one alphanumeric character. The printwheel rotates in a vertical plane that is parallel to the axis of the platen. The printwheel is positioned so that the character on the uppermost spoke is in the proper position to strike the ribbon, platen, and paper squarely (see Figure 3-2). Printing a character is accomplished by activating a solenoid-operated printhammer mounted directly behind the uppermost printwheel position. A current pulse applied to the solenoid causes the printhammer to strike the uppermost spoke, and the flexible nature of the plastic printwheel permits the die to contact the ribbon and transfer the image to the paper.

Character selection is determined by the angular position of the printwheel at the time the printhammer is activated. A servosystem, controlled by the printer electronics, positions the printwheel according to the character input command.

The printwheel motor, printwheel, and printhammer are mounted on a mechanical assembly known as the "carriage". Also mounted on this assembly is the ribbon cartridge, the ribbon drive motor, a ribbon lift solenoid, and an end of ribbon sensor.

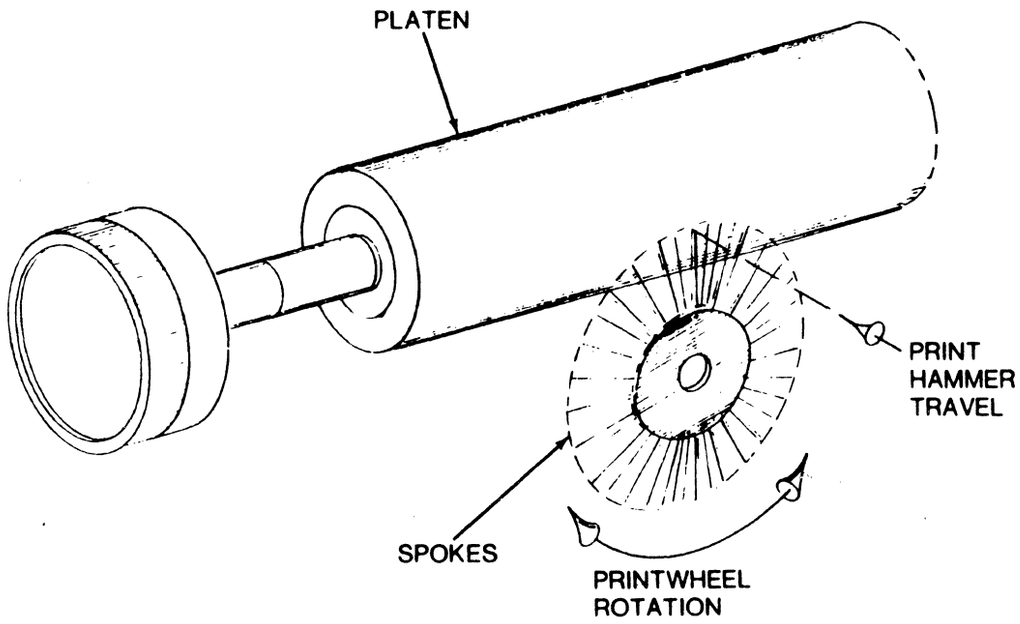


FIGURE 3-2
PRINTWHEEL DETAIL

The carriage assembly travels the width of the chassis on two rails which parallel the axis of the platen roller. A flexible cable attached to the carriage carries all drive and control signals between the carriage and the printers electronics. Rubber stops on both ends of the rail limit carriage travel, and an optical sensing unit next to the left deceleration stop indicates the left electrical limit during initialization.

The location of the carriage assembly on its guide rails determines the horizontal position of the printed character. A DC servomotor on the printer's chassis positions the carriage by means of a cable, pulley, and a tensioner arrangement, as shown in Figure 3-3. Control signals position the servomotor in response to external commands, permitting programmed bi-directional movement of the carriage up to 13.1 inches (26.2 inches in the Wide Track model). An optical encoder enables the controlling device to position the carriage in 1/120th. inch increments.

Ribbon feed and ribbon lift are controlled by individual sub-systems, although the stepper motor which controls the ribbon advance and the solenoid which lifts the ribbon into position are both located physically on the carriage assembly. The solenoid is used to lift the ribbon into printing position, between the uppermost spoke of the printwheel and the paper surface, under external program control. A drive dog on the shaft of the stepper motor engages internal splines on the hub of the drop-in ribbon cartridge, so that rotation of the stepper motor advances the ribbon incrementally, just prior to the firing of the printhammer.

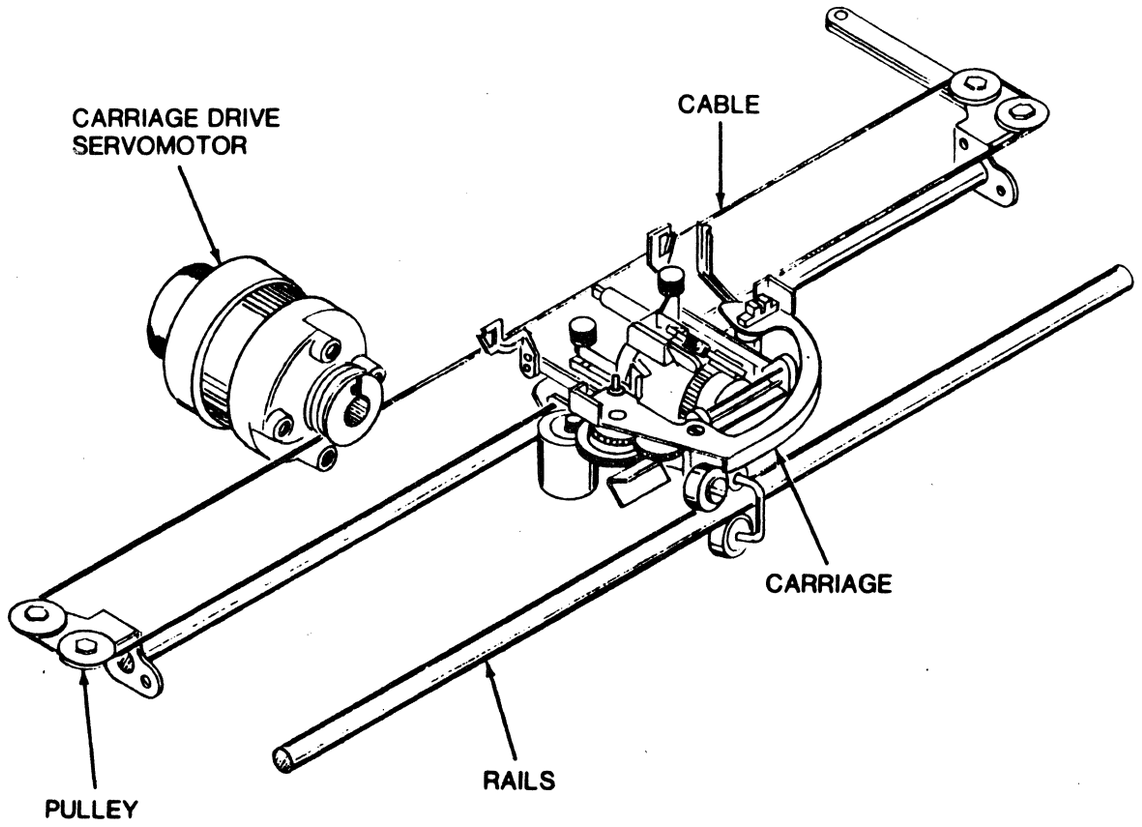


FIGURE 3-3

CARRIAGE POSITIONING

3.2 ELECTRICAL OPERATION OF THE PRINTER

An overall block diagram of the printer is shown in Figure 3-4. The printer's electronic and electromechanical circuits can be broken down into subsystems for purposes of discussion. This section will describe the electromechanical portion of the printer, giving the reader a better foundation for the discussion of control electronics that follows.

3.2.1 SPLIT-PHASE STEPPER MOTORS

Split-phase stepper motors are used in the paper feed and ribbon drive mechanisms. These motors are conventional in design and may be similar to motors that the reader has encountered already in servicing of other equipment.

The motor consists essentially of two field windings and an armature. The windings are oriented so that the magnetic field produced by each winding intersects the other's field at an angle of approximately 90 degrees. The field in the interpole cavity is thus the resultant of two fields as shown in Figure 3-5.

The armature in this kind of motor is magnetized by a current derived from the field voltages. This current is passed through a full-wave rectifier, before being applied to the field coils. As a result, the field produced in the armature is constant in its relationship to the armature's physical core. Given this observation, it will be convenient to visualize the armature simply as a strong permanent magnet.

The natural tendency of the magnetized armature is to align itself with the resultant magnetic field produced by the two field coils. Directional rotation will occur, if the current applied to the individual field coils vary in phase relationship. This rotation is shown in Figure 3-5.

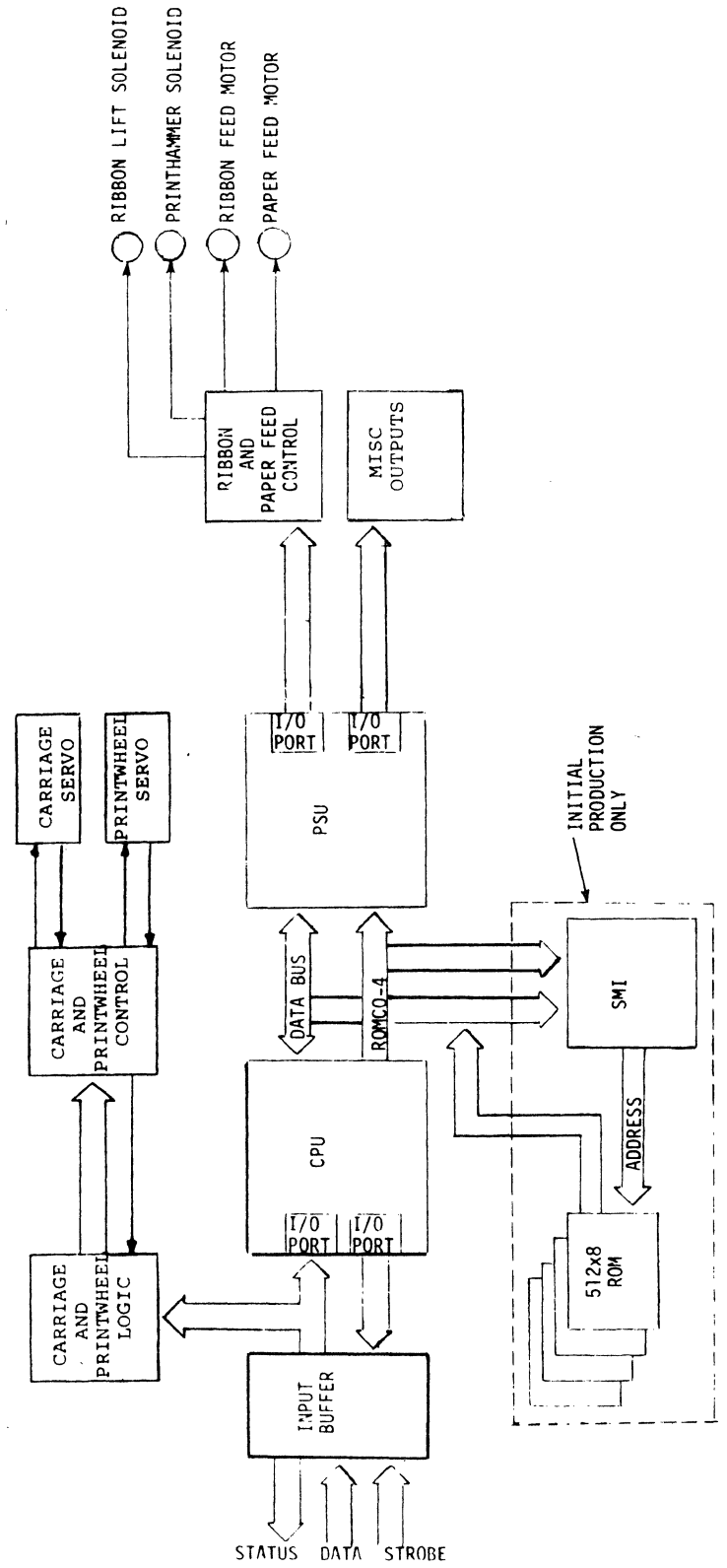
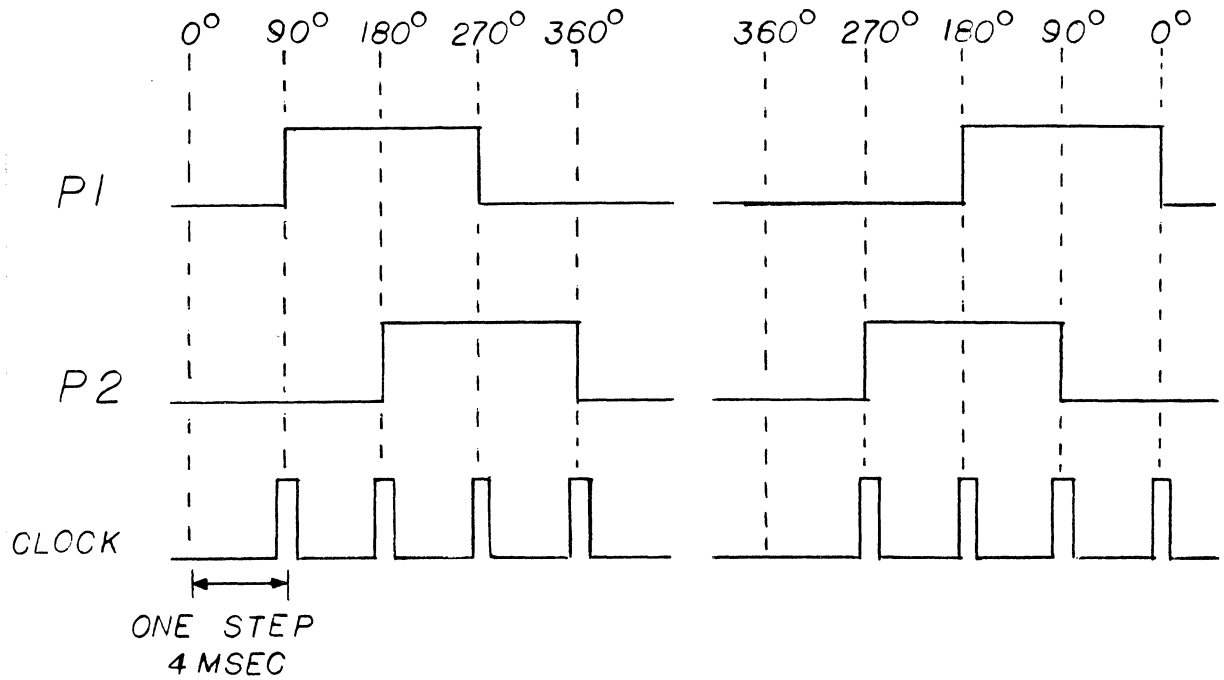


FIGURE 3-4
PRINTER OVERALL BLOCK DIAGRAM



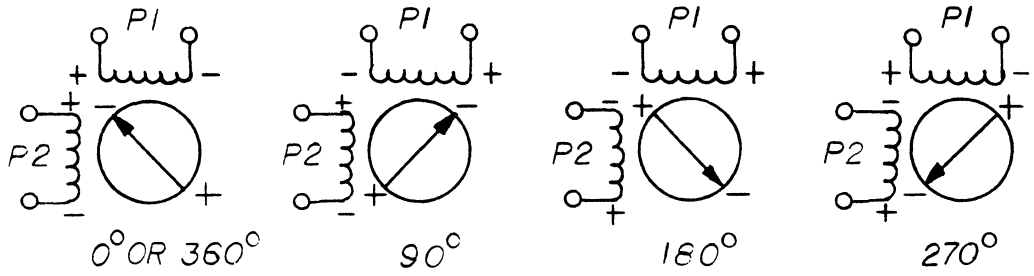


FIGURE 3-5

STEPPER MOTOR POSITIONING

The driving signals vary in quadrature, and may be thought of as being 90 degrees out of phase electrically. Under these circumstances, the motor bears resemblance to the splitphase AC induction motor. Note, however, that armature slippage in a stepper motor is abnormal, and that this kind of motor therefore never develops the large armature current and the high torque that is characteristic of induction motors.

Nevertheless, the motor's performance is quite satisfactory under light load conditions. Its chief advantage is that it lends itself to the precise positioning of light mechanisms, in fixed increments that bear a relationship to the 90 degree increment of rotation. This kind of motor is ideally suited to mechanisms such as ribbon and paper feed. In the former case, the load is extremely light. In the latter, the motions are relatively infrequent, so that the motor's slow response is not a serious disadvantage.

3.2.2 OPTICALLY POSITIONED DC SERVOMOTORS

When it comes to the printwheel and carriage positioning mechanisms, however, the weaknesses inherent in stepper motors cannot be overlooked. Both the carriage and the printwheel are in motion almost continuously during normal printing. Frequent acceleration and deceleration makes severe demands on the motor, and the rapid positioning of these relatively massive assemblies calls for a motor with a high torque.

The foregoing considerations dictate the choice of a DC motor. At the same time, however, we can sacrifice nothing in the precision of motor positioning. Actually the two mechanisms we are presently considering are even more sensitive to positioning errors than are the ribbon and paper feed mechanisms. Given the DC motor assumption, this further dictates a servomechanism of some kind, in which a position-dependent feed-back is used to control the rotation of the motor. Unfortunately, the methods available for doing this, up until now, have been both limited and cumbersome.

It was in this context that the optical positioning mechanism used in the Sprint 3 Series printers was developed. This technique relies on optoelectronic devices to generate both the rate and the position information on which the servo feed-back loops are based. The method is described briefly in the following paragraphs.

The basic DC servomotor consists of a reversible DC motor. Attached to the motor's frame is the photohead assembly which contains three photo-voltaic cells and a light emitting diode. In this simple configuration, all three cells are illuminated continuously by the light from the LED, producing output voltages which are proportional both to the light intensity and to the illuminated area of the cell.

The LED's sensitivity to temperature makes it an inherently unstable light source. And since the reliable function of the servo will depend on the stability of the output from the photohead, external means are used to ensure a stable output. Once cell (CLEAR) monitors the output from the LED. The output of this cell drives an inverting amplifier, which in turn supplies the drive current for the diode. Negative feed-back damps fluctation in the output of the LED, producing a stable reference illumination and hence a relatively stable peak voltage output from all three cells.

Attached to one end of the motor's armature shaft is an external rotating disc. Changes in the shaft's angular position are thus coupled directly to the disc. The edge of the disc extends into a slot in the side of the photohead, as shown in Figure 3-6, masking the diode, and casting a shadow on two of the three photovoltaic cells (the CLEAR cell is not affected).

This would naturally preclude any output whatsoever from the A and B photocells were it not for the fact that the opaque circumference of the disc is constructed with openings of uniform size. Rotation of the disc thus casts a varying shadow on the A and B photocells, whose output is directly proporational to the area illuminated, other factors being equal.

Dimensions of the assembly are controlled carefully, so that the electrical fluctuations produced in the output of the photocells closely approximate a sine wave. The A and B cells are placed geometrically so that the outputs produced are 90 degrees out of phase with respect to one another. These signals furnish the basis for controlling both the angular position and the speed of the servomotors. Before they can be used, however, an intermediate set of signals must be generated. This process is described below.

Raw A and B outputs from the encoder are first amplified, and translated to levels roughly symmetrical about ground, with a nominal peak-to-peak amplitude of 12 volts. Preconditioning assures the reliable operation of the subsequent circuitry.

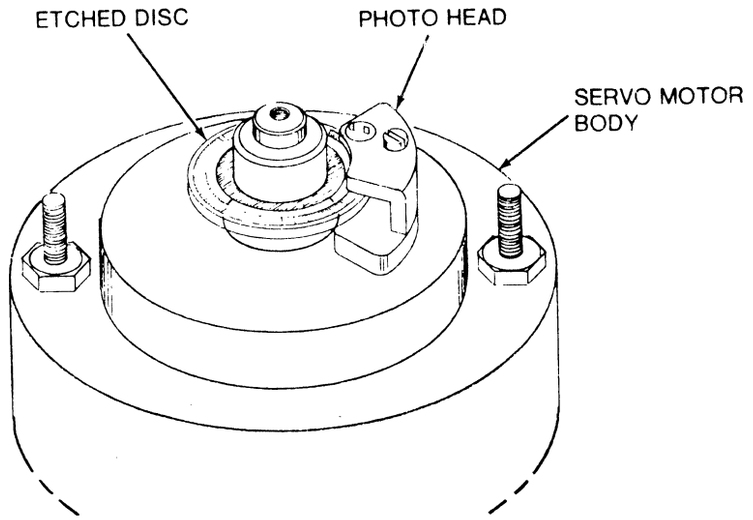


FIGURE 3-6(a)
OPTICAL ENCODER PHOTO HEAD DETAIL

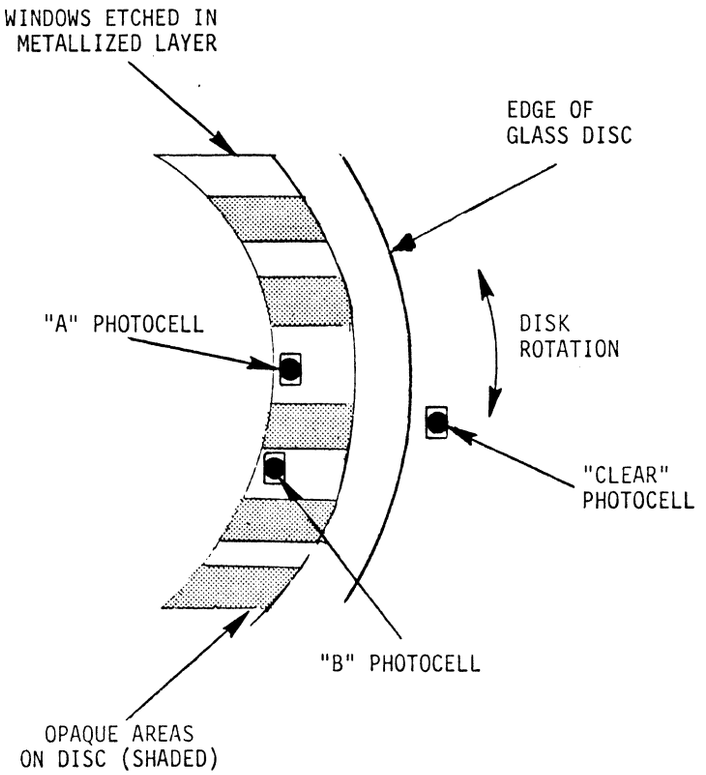


FIGURE 3-6(b)
OPTICAL ENCODER PHOTO HEAD DETAIL

As indicated, the A and B signals are applied to the inputs of three Schmitt squaring circuits. These are adjusted to trigger at specific points on the input waveforms, hence the importance of accurate signal preconditioning. The idealized outputs obtained are shown in Figure 3-7. They are labeled X, Y, and Z.

By splitting the X, Y, and Z signals and combining selected functions in suitable gates, we obtain the entire range of outputs depicted in Figure 3-7. These include the Carriage Clock signals, and the Φ1 - Φ 4 sampling signals. Together, these derived outputs permit control of the motor's speed and position.

To visualize the positioning mechanism, consider the waveforms shown in Figure 3-7. Stable positions of the armature are established at zero crossings of the encoder's A output. In the position mode, negative feedback derived directly from the A waveform causes the motor to settle in the nearest available "trough"; that is, the nearest negative-going null. Because these stable positions suggest a mechanical analogy, they are referred to as "detents". There are 192 such detents in each revolution of the printwheel, and 400 per turn of the carriage drive motor. Motors left to their own devices in the position mode will always react by seeking the closest detent.

Re-positioning of the motor requires a temporary interruption in the continuity of the positioning loop. During the time that feedback is suspended, the motor may be re-positioned accurately, by counting the intervening number of encoder impulses. When the count establishes that the motor is in the vicinity of the desired new position, the feedback loop is restored, and the motor promptly settles in the proximate detent.

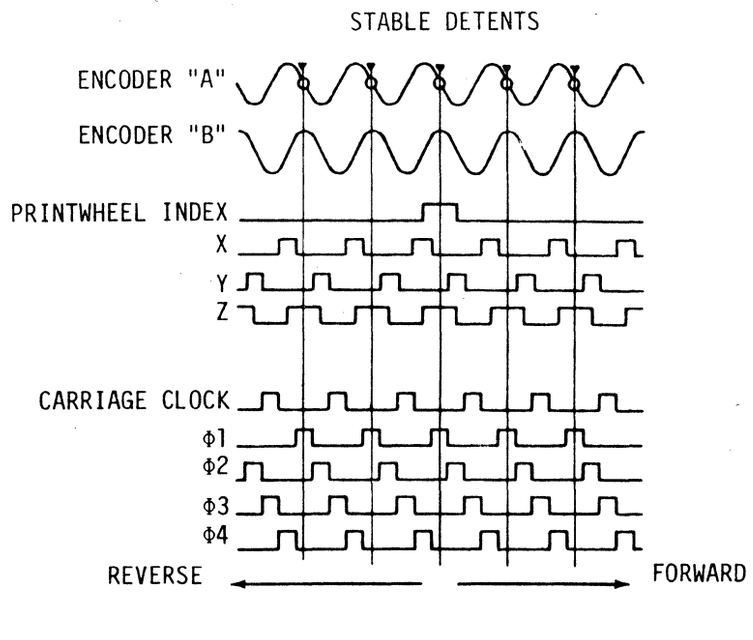


FIGURE 3-7

GATING LOGIC: IDEALIZED OUTPUTS

When it is necessary to re-position the motor, the first action taken is to suspend the position mode. We then begin by moving the servo toward its new position, counting Carriage Clock pulses as we go. Once the count indicates that the desired position has been reached, we simply re-establish the position mode. Completion of this sequence will find the motor settled in the desired angular detent.

While the positioning loop is suspended, the servomotor operated as a rate servo. In the rate mode, the servomotor's speed and direction of rotation are controlled by an external reference which is related to the gross magnitude of the position error. Negative feedback proportional to the motor's speed is combined in a summing network with the reference level input. When the two exactly cancel, the net rate error applied to the servo is zero, and the stable speed of the motor is established accordingly.

The frequency of the encoder's output is a direct indication of motor velocity. Unfortunately, simple counting would not produce a velocity indication fast enough to permit precise control of the servomotor. Other means must be used, to monitor the motor's rotational velocity.

You will observe that the change in the encoder waveform is roughly linear in the immediate vicinity of the null points. This is true over the interval which extends from about 45 degrees preceding the detent, to about 45 degrees past. Moreover, the slope of this waveform is directly proportional to the motor's angular velocity. By differentiating this portion of the encoder's output, we can obtain a voltage level which directly indicates the speed of the servomotor.

The chief problem with the differentiation technique is that the output obtained is not continuous; that is, there is an interval of 270 degrees during which we have no indication whatever of the motor's rate. This naturally defeats the kind of precise velocity control required of these servos.

To circumvent this basic difficulty, we rely on the Φ1 through Φ 4 signals derived in the gating logic. The input to the differentiator at any given time is a logical composite, formed from the coincidence of one of the Φ1 through Φ4 gating signals and one of the four encoder outputs (A, B, $\bar{A}$ or $\bar{B}$). During the interval from 315 degrees to 45 degrees, the A output is sampled, and from 45 degrees to 135 degrees the differentiator samples the B encoder output. From 135 to 225 degrees and from 225 degrees to 315 degrees, the $\bar{A}$ and $\bar{B}$ outputs, respectively, are sampled. In this way, the differentiator is able to produce an output which is continuous over the entire 360 degree interval between adjacent detents, thus enabling constant control of the motor's velocity. Velocity control systems of this kind are used in both the printwheel and carriage servos.

Note that the photohead associated with the printwheel motor contains a fourth photovoltaic cell. This cell matches a single opening in the encoder's rotating shadow mask, so that an INDEX output is produced at one particular position of the motor shaft. The ENCODER INDEX is conditioned separately, in yet another Schmitt squaring circuit, and used to indicate the motor's absolute position to the printwheel control logic. Since carriage motion is always a relative displacement, it is not necessary to know the motor's absolute angular position. For this reason the index feature is omitted from the carriage encoder.

3.2.3 PRINTWHEEL SERVO

The printwheel sub-system performs the functions immediately associated with the printing of each character. These functions include the positioning of the printwheel, and the firing of the printhammer. The printwheel logic also controls ribbon feed indirectly, by exercising control over the ribbon feed logic.

The printwheel servomotor and the printhammer solenoid are situated on the movable carriage assembly. A flexible cable carries all drive and control signals between the carriage and the printer's electronics.

Inputs to the printwheel servo include delta counter lines, position mode and direction lines. An optional END OF RIBBON input from an optical sensor on the carriage is activated whenever the ribbon cartridge is exhausted.

3.2.4 FUNCTIONAL DESCRIPTION OF THE PRINTWHEEL SERVO

Figure 3-8 shows a functional block diagram of the printwheel servo subsystem.

Between the time that a print cycle is complete and the next character strobe is received, the printwheel is static, resting in the "position" mode. In this mode, the input to the error amplifier is clamped to a level near the center of encoder signal A, forcing the printwheel servomotor to remain at rest.

The printwheel's position determines the character to be printed. Because of this, the printwheel logic must have some way of keeping track of the current printwheel address.

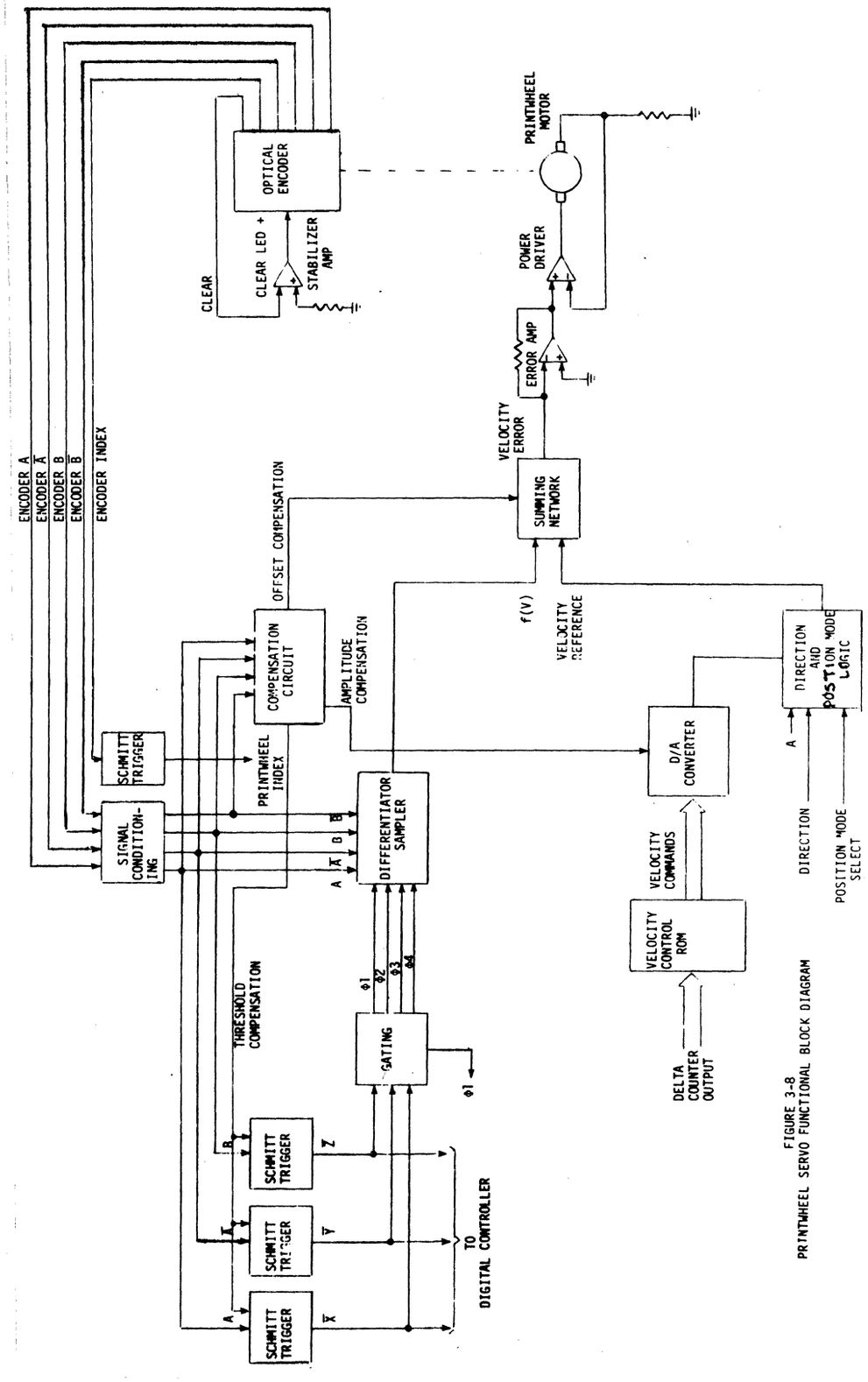


FIGURE 3-8
PRINTWHEEL SERVO FUNCTIONAL BLOCK DIAGRAM

This function is performed by the printwheel counter logic and the microcomputer sub-system. Each time there is a coincidence between the 1 and INDEX signals, the counter is reset to zero. Thereafter, each 1 signal increments or decrements the counter. By this means the counter is able to track the printwheel position at all times.

When a character has been strobed into the input logic, the printwheel cycle begins. The microcomputer sub-system performs a "table look-up" to determine the absolute address of the character to be printed. An arithmetic operation is then performed to determine the direction of rotation to reach the required address in the shortest time, and a delta count is also determined, based on the amount of rotation required.

The printwheel cycle begins when the position mode select line causes the printwheel position mode circuit to release the error amplifier input. At the same time, a velocity command is input to the D/A converter, which outputs a DC level proportional to the input command weighting. The servomotor now begins to accelerate (see Figure 3-9) until the output of the differentiator reaches the required level to stabilize the motor at the speed commanded by the D/A converter. During this time, the printwheel counter logic is counting down and reducing the delta count. This decrements the velocity commands in steps determined by the velocity deceleration profile stored in the velocity control ROM.

When the printwheel counter and logic have reached the correct address, the printwheel servosystem switches to the "position" mode. In this mode, the position switch inputs signal A to the error amplifier and brings the printwheel motor to a stop at the "detent" where the correct character spoke is at the uppermost position.

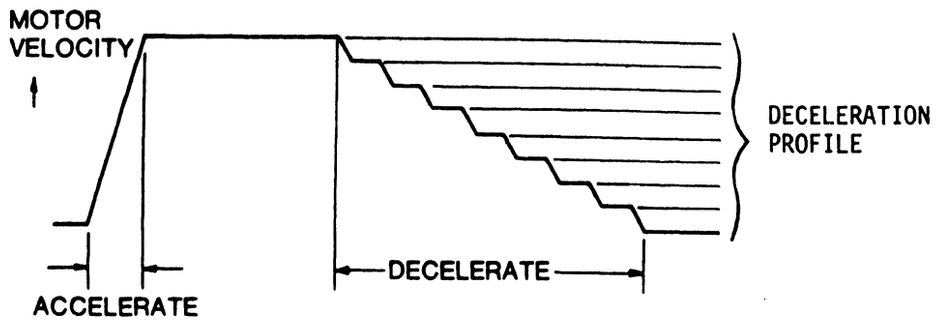


FIGURE 3-9

PRINTWHEEL ACCELERATION/DECELERATION PROFILE

Because there may be changes in photocell output due to temperature drift and changes in ambient light, a compensation circuit monitors the photocell output and applies a correction to the D/A output, the error amplifier offset, and the squaring circuit thresholds when a change is detected. The compensation circuit consists of two peak followers which track the absolute peak-to-peak output of the photocells. This circuit is followed by a sample-and-hold circuit which holds a DC level proportional to the photocell peak-to-peak output when the position mode is entered. This allows the acceleration profile to remain constant for each printwheel rotation cycle. It should be noted that the compensation circuit eliminates any adjustments by the maintenance technician and allows total interchangeability of boards between units.

3.2.5 FUNCTIONAL DESCRIPTION OF THE CARRIAGE SERVO

The carriage servo is shown in the functional block diagram of Figure 3-10. It can be seen that the diagram is very similar to the diagram of the printwheel servo. Electrically, the servomotor is a heavy-duty type, due to the larger mass of the carriage mechanism, and the driver circuits therefore must handle higher currents.

Operation of the servo is nearly identical to that of the printwheel servo. Initially, the servomotor is stopped by the action of the position circuit. When a carriage movement command is received by the servo sub-system, the D/A converter outputs a voltage level proportional to the input velocity command. At the same time, the position mode is released and the motor begins to accelerate. When the output of the differentiator matches the output of the D/A converter, the motor stabilizes at the desired speed. As the carriage counter circuits count down toward zero, the deceleration sequence begins. The velocity commands are decremented in accordance with a predetermined, stored profile. It should be noted that because of the difference in mass and velocity of the carriage mechanism, the deceleration profile used in the carriage servosystem is different from the one used in the printwheel servosystem.

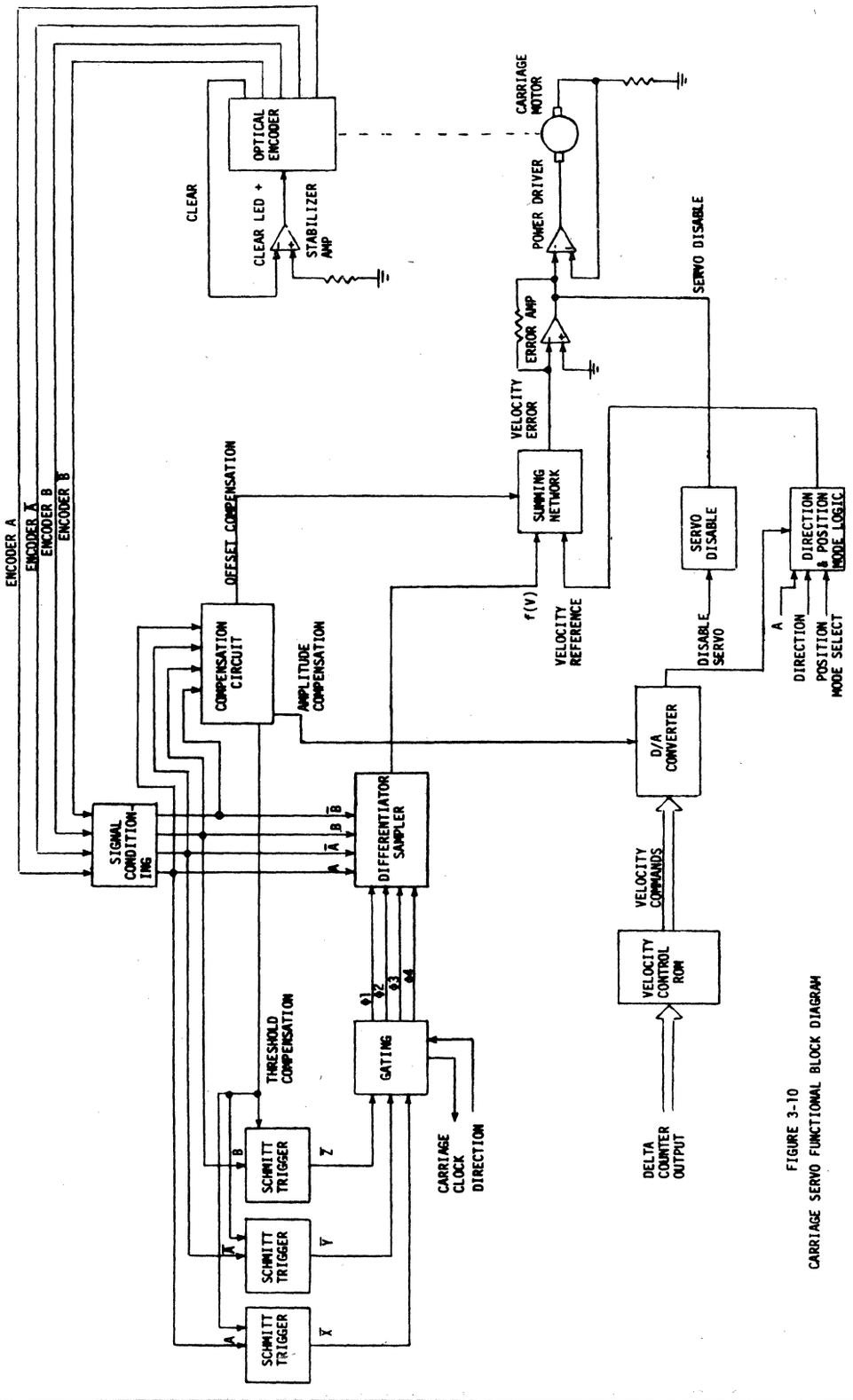


FIGURE 3-10
CARRIAGE SERVO FUNCTIONAL BLOCK DIAGRAM

As with the printwheel servo, when the carriage servo delta counter has counted down to zero, meaning that the programmed carriage movement increment has been reached, the servosystem is placed in the position mode and the motor (and carriage mechanism) comes to a stop at the selected position.

If, for some reason, a CHECK condition occurs (either through failure of the power supplies or failure of the carriage to move when commanded), the carriage servo is disabled by the servo disable circuit, which clamps the input of the servomotor power drivers to ground.

Temperature and ambient light drift compensation is employed in the same manner as the printwheel servo: peak followers and sample-and-hold circuits monitor the photocell output and apply a correction signal to the summing amplifier, Schmitt trigger circuits, and the D/A converter. In addition, LED current is also compensated for changes in photocell output in a manner similar to that used in the printwheel servo.

The carriage servo generates two signals used in timing and control. The first signal is the CARRIAGE CLOCK signal which is generated by gating the X and Y outputs from the Schmitt trigger circuit. The CARRIAGE CLOCK is the signal for the carriage counter, and is timed so that it occurs on the negative-going portion of the photocell output. It should be noted that an error in position would occur if CARRIAGE CLOCK was always in the same phase with respect to the photocell output, because the direction of carriage travel determines the phase of the two photocell outputs. Depending on the direction of travel, gating logic changes the phase of the CARRIAGE CLOCK signal so that it occurs just before the required "detent" position of the carriage.

A second signal of interest is the CARRIAGE LIMIT signal generated by a photosensor located at the extreme left position of carriage travel (this is not shown in Figure 3-10). The photosensor output triggers a Schmitt squaring circuit which generates a pulse whenever the carriage is at the left limit to signal the control logic that the limit has been reached. This is used in initialization routines and as an error flag.

3.2.6 PAPER FEED OPERATING PRINCIPLES

As shown in the block diagram of Figure 3-11, the paper feed drive consists of two driver circuits which are connected to the field coils of the paper feed stepping motor. Depending on the desired direction of paper movement, the phase of the two paper feed clock signals P1 and P2 differs. To move the paper upward, P1 leads P2 and the motor steps in one direction; to move the paper downward, P2 leads P1 and the motor steps in the other direction. It should be noted that no movement is possible unless the paper feed hold signal has dropped to a low level. It is held at a high level to hold the stepper motor in a fixed position between paper movements. When the paper feed hold is low, the motor is released to step in either direction as determined by the input clock signals.

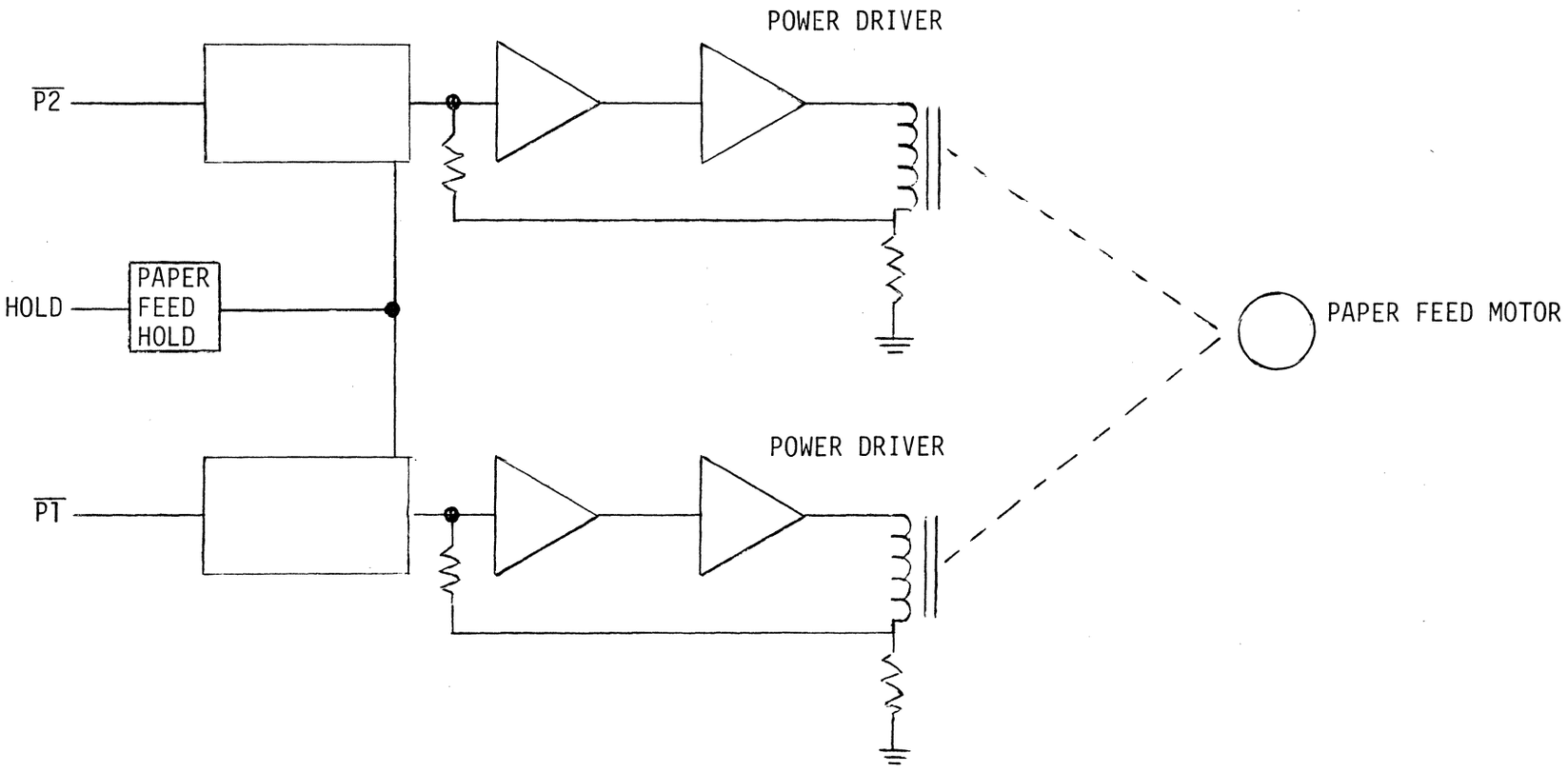


FIGURE 3-11
SIMPLIFIED BLOCK DIAGRAM, PAPER FEED DRIVE

3.2.7 RIBBON FEED OPERATING PRINCIPLES

Ribbon feed is very similar to paper feed, except that the ribbon feed motor moves only in one direction. The stepping motor is driven by ribbon feed signals R1 and R2, which alternately switch current through the motor field coils to step the motor and move the ribbon.

3.2.8 HAMMER DRIVE OPERATING PRINCIPLES

A simplified diagram of the hammer drive circuit is shown in Figure 3-12. When the HAMMER signal goes low, current will flow through the hammer solenoid and move the hammer forward to strike the ribbon. Hammer striking intensity is a function of the HAMMER pulse width, varying from approximately 1.6 ms to approximately 2.5 ms. Intensity is a function of the character to be printed, with a capital "W" having the widest pulse and a period (.) the narrowest. To protect the hammer from overheating due to logic failure, a 35 ms one-shot is triggered by the leading edge of the HAMMER pulse. If the HAMMER pulse has not terminated before the one-shot times out, the trailing edge of the one-shot output will disable the AND gate driving the hammer solenoid driver and cut off current to the hammer solenoid.

3.2.9 RIBBON LIFT OPERATING PRINCIPLES

A simplified diagram of the ribbon lift circuit is shown in Figure 3-13. When the ribbon is in the lowered position, no current flows through the ribbon lift solenoid. Initiated by a ribbon lift command and a part of the print cycle, two signals are generated: RIBBON RAISE and RIBBON LIFT HOLD. Two current levels are required: a high current to raise the ribbon and a lower current to hold the ribbon in the raised position. The higher current is generated by the action of RIBBON RAISE, which is activated at the beginning of the lift cycle. The holding current is generated by RIBBON LIFT HOLD, which remains activated to hold the ribbon in the raised position during the print cycle. Note also that the protection pulse signal prevents any ribbon lift coil from overheating due to logic failure.

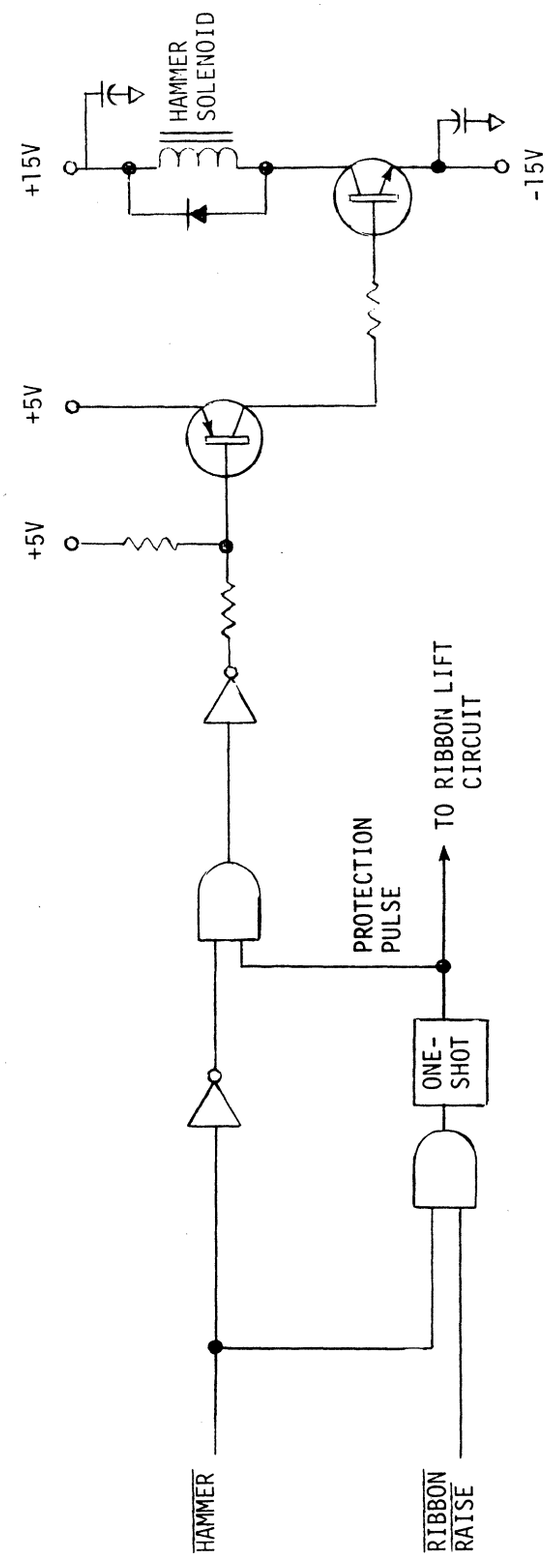


FIGURE 3-12
SIMPLIFIED SCHEMATIC, HAMMER DRIVE CIRCUIT

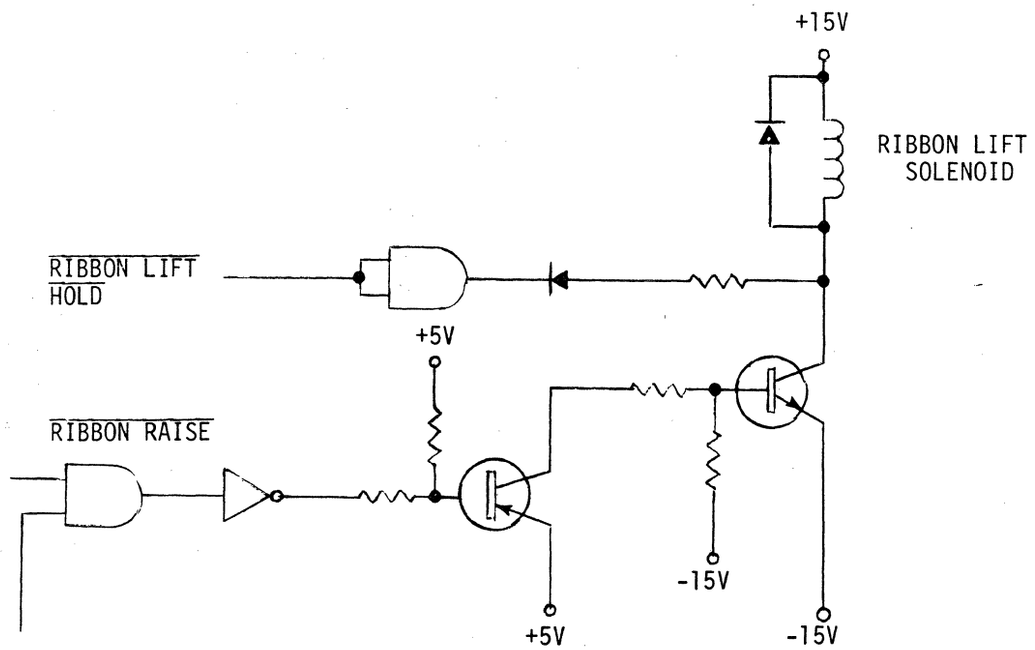


FIGURE 3-13
RIBBON LIFT SIMPLIFIED DIAGRAM

3.2.10 CHECK CIRCUIT OPERATING PRINCIPLES

The check circuit shown in Figure 3-14 monitors power supply voltages and carriage movement to ensure that improper operation of the printer due to power supply failure or carriage failure will not go unnoticed by the operator or the system.

Each of the three supplies (+15V, -15V and +5V) is monitored by comparator circuits referenced to precision Zener diodes. If the 15V supplies vary more than 2 volts for more than approximately 1.5 ms, the comparators will trigger and set the CHECK flip-flop. This output disables the carriage servo and sends a CHECK output to the system connected to the printer. In the same manner, the +5 supply is monitored by a comparator circuit with a much shorter time constant. If the +5V supply varies more than 0.5 volt for a period exceeding approximately 1 microsecond, the comparator triggers and initiates a CHECK condition.

To prevent operation with the carriage jammed or disabled in any manner, the check circuit monitors the carriage clock output after a carriage movement command has been issued. The first carriage clock pulse triggers are re-triggerable one-shot circuit. If further clock pulses are received within the time-out constant of the one-shot (8ms) the one-shot is re-triggered and stays in the triggered state. If no carriage clock pulses occur within the 15ms period, the one-shot times out and initiates a check condition.

When a check condition has been initiated by either a power supply failure or a carriage motion failure, the check flip-flop will be set and no further printer action can be accomplished until the check flip-flop is reset by the RESTORE command. If one or more of the power supplies is inoperative and a restore sequence is attempted, the check flip-flop will remain set and will not allow operation until the problem is cleared.

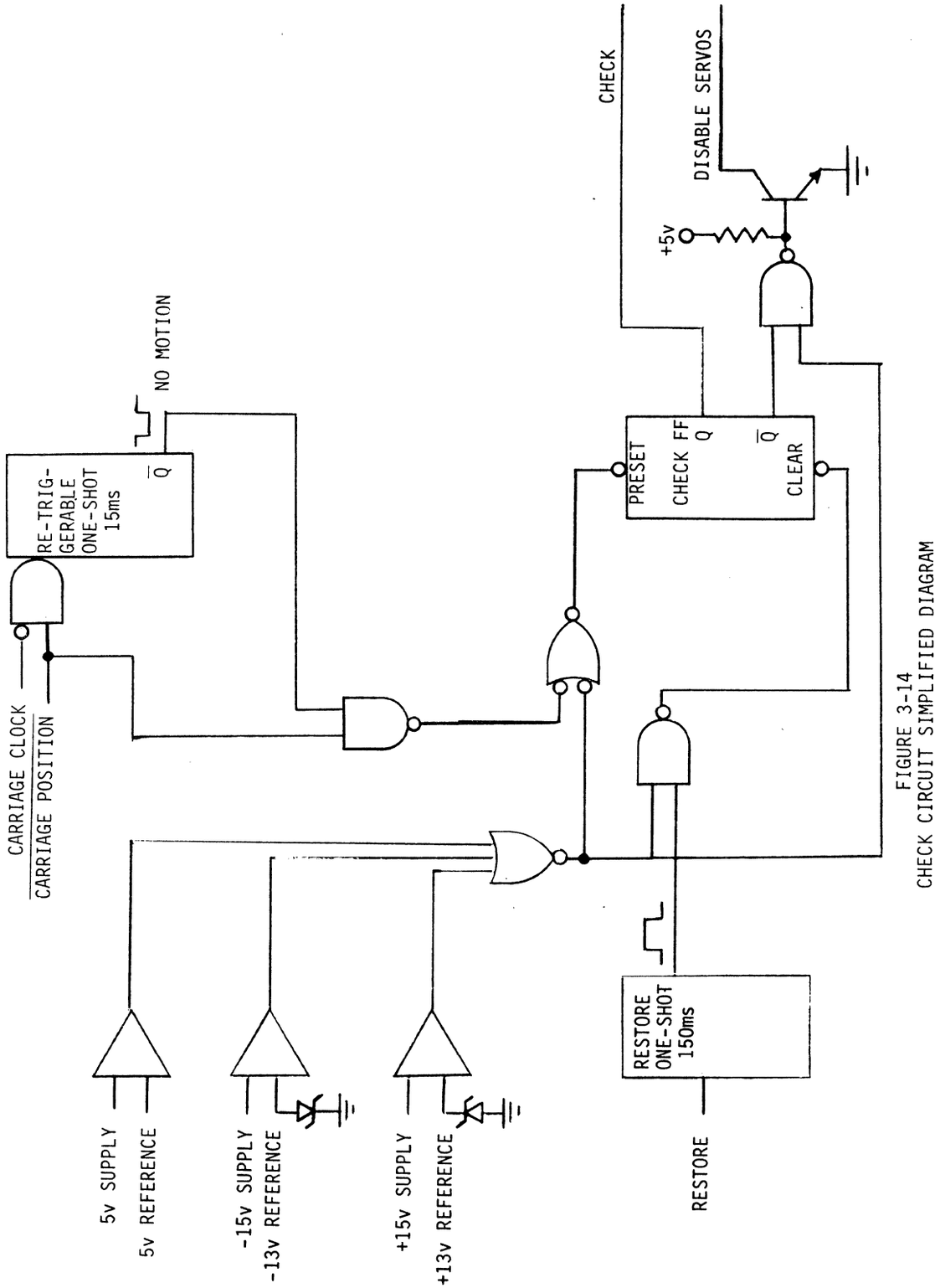


FIGURE 3-14
CHECK CIRCUIT SIMPLIFIED DIAGRAM

3.3 DIGITAL CONTROLLER

The digital control section of the printer transforms the data input to the interface to command for the analog section. The following paragraphs provide an introduction to the concept of a microprocessor and its related support devices. Refer to Figures 3-15, 3-16 and Schematic Diagram Section 9 throughout this discussion.

3.3.1 MICROPROCESSOR

The basic controller for the digital section is the 3850 CPU. This is a single 40-pin device containing the necessary computing functions necessary to perform arithmetic and logic operations on the input data and output control signals for the analog section. The 3850 also generates signals to control supporting devices used in this application (3851 Program Storage Unit, and in initial production units, a 3853 Static Memory Interface). The 3850 has two integral I/O ports and a 64 X 8 - bit "scratchpad" RAM.

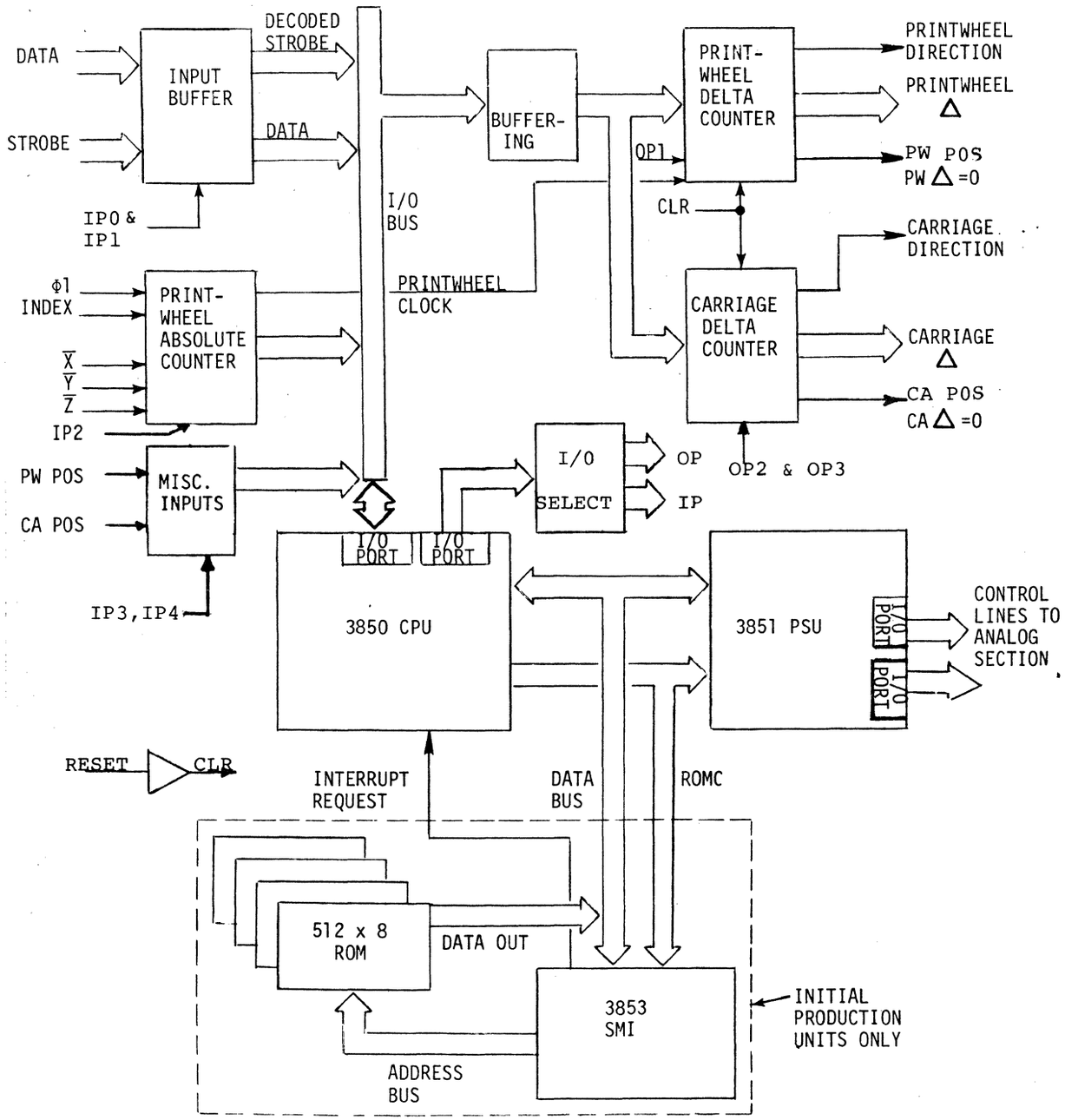


FIGURE 3-15
DIGITAL CONTROLLER BLOCK DIAGRAM

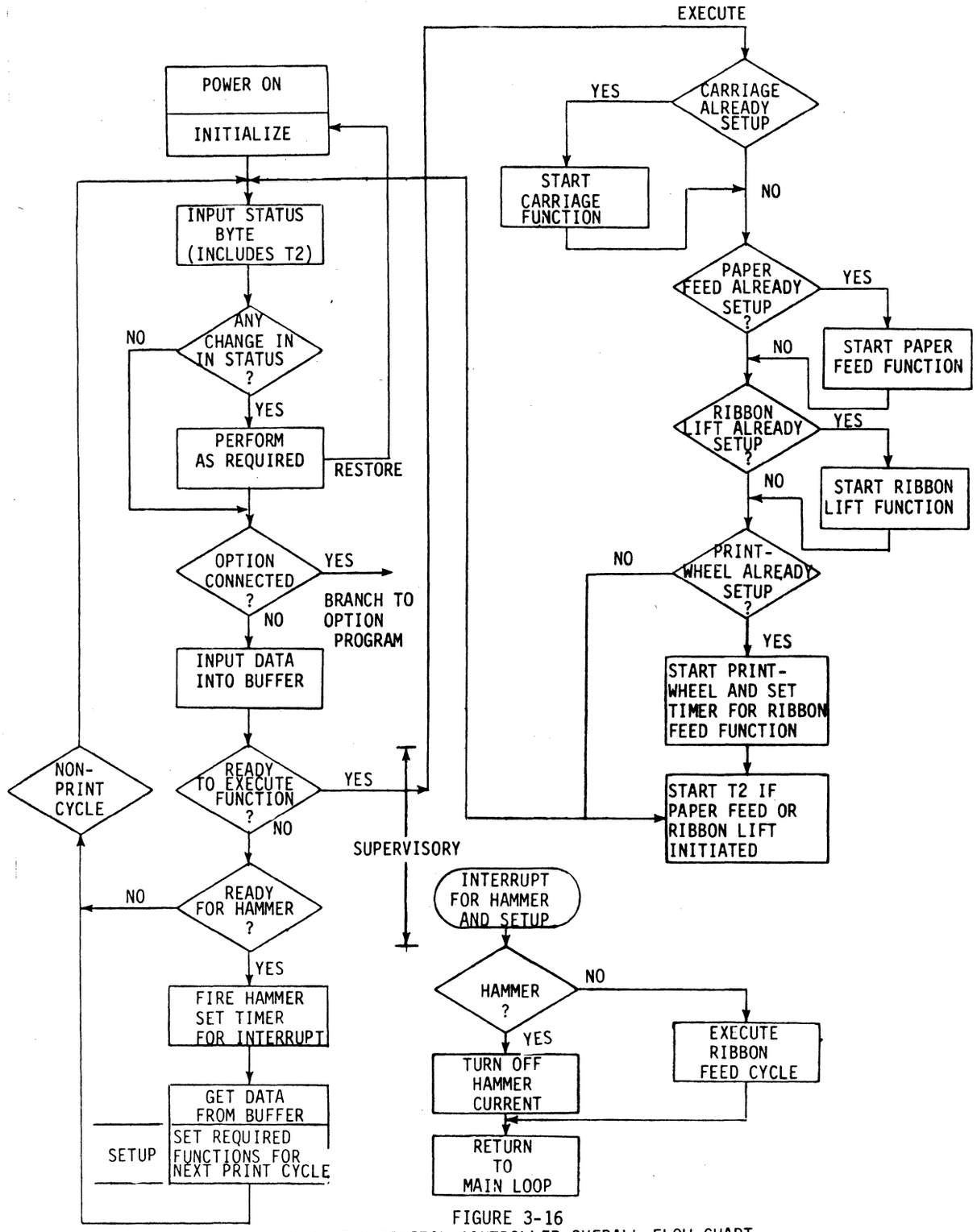


FIGURE 3-16
SPRINT 3 DIGITAL CONTROLLER OVERALL FLOW CHART

3.3.2 PROGRAM STORAGE UNIT

In initial production units, the 3851 PSU is used solely for its I/O capability. After initial production, the 3851 will be used to store 2048 eight-bit program words in its read-only memory (ROM). In initial units the printer's operating program is stored in programable read-only memory (prom) devices capable of storing 2048 eight-bit words. These devices are controlled by a 3853 Static Memory Interface (see below).

3.3.3 STATIC MEMORY INTERFACE

The 3853 SMI provides an interface between the ROM devices and the CPU. Following instructions provided by the CPU, the 3853 "addresses" the ROM devices by outputting a binary-coded word on the address bus. Each ROM has a unique set of addresses, so that for each word on the address bus, one and only one device will output the data contained at the location specified by the address. This data is forwarded to the CPU as part of a series of predetermined "instructions" on what function to perform next in the sequence of operations.

3.3.4 ROM DEVICES

Each ROM device consists of a matrix that can be visualized (although this is not actually how the device is constructed) as having eight rows and 512 columns. The eight address bits, plus, a "chip select" line are decoded to address one of the 512 columns. At the proper time in the operating sequence, the binary-coded word contained at the memory location is output on the data bus and stored in the CPU's internal data registers.

3.4 OPERATING SEQUENCE

Figure 3-16 is a flow chart of the operating sequence used by the digital controller to perform the functions required by the printer to move the carriage, lift the ribbon, and print the character. The following paragraphs describe steps in the operating sequence.

3.4.1 INITIALIZATION

When power is first applied, the states of the digital control logic are random. Therefore, an initialization sequence is performed to be certain that all functions are reset and ready for the first operating sequence. The 3850 CPU has its own power-on cycle: when power is detected, all registers are reset and the CPU asks for an instruction located in memory at address 00. This is the first instruction in an initialization sequence to be discussed later. The analog circuitry also contains a power-on reset circuit which outputs a signal designated RESET. This, in turn, generates CLR, which is a negative-going pulse with a duration of approximately 150 ms. This signal clears the input buffer and resets the printwheel and carriage delta counters to zero.

The next step in initialization is to move the carriage to the extreme left margin and establish an absolute count in the printwheel counter to determine the current printwheel address. This step is done in two stages: the first stage outputs a count to the carriage delta counter (strobed by OP2 and OP3) which results in an output from the counter of CAV4 (carriage velocity 4, an intermediate velocity), and movement in a left-hand direction. The carriage thus moves relatively slowly toward the left stop, containing an optical sensor. When the carriage reaches the sensor, the sensor outputs a signal

(CA LIMIT) to the CPU via the I/O bus after IP4 selection. The carriage then stops and moves in a right-hand direction to the first "detent".

The printwheel logic is initialized by spinning the printwheel motor at an intermediate velocity, much as the carriage was moved, until there is a coincidence between the printwheel INDEX output and the printwheel Φ1 output. This resets the printwheel absolute counter to zero. The printwheel is then allowed to coast to a stop. Meanwhile, the absolute counter, having been reset to zero, counts printwheel clock pulses and establishes the absolute position of the printwheel. RAM registers are initialized. This completes the initialization process.

3.4.2 DATA BUFFERING

All carriage, printwheel, paper feed, and ribbon lift commands are moved from the hardware buffer to a 15-character, software-controlled RAM buffer. When the printer is ready to set up another command, data is moved out of the buffer in the same order that it came in (i.e., a FIFO buffer).

3.4.3 PRINT CYCLE

When the initialization sequence is complete, the controller is ready for data input. Data is strobed into the input buffer by an accompanying strobe signal. All 16 bits are stored simultaneously, and when stored, the RDY EN line from the buffer disables the "ready" lines output to the external data source. The buffer output is now input to the CPU, eight bits at a time controlled by enabling lines IPO and IPI. During the input portion of the program, the CPU tests the I/O bus for an input. The strobe lines are encoded by the hardware and later decoded by the software to enable the CPU to determine which strobe line has been activated and to decide which portion of the program will be used to process the data.

Figure 3-16 shows a flow chart of the print cycle. It can be seen that although there is a standard sequence of events, if some functions have been performed previously, they are skipped in the flow of the program. The only constant is that the printhammer operation is the last operation in the cycle.

A typical print cycle begins with the input of carriage data. When it is ready for execution, the CPU transfers from a RAM register set up for the command, the number of carriage clock pulses for the increment of movement to the carriage delta counter. The carriage counter then outputs a velocity code to the carriage servo velocity control ROM. During the "Supervisory" portion of the program, the CPU tests the "position mode" bit of the I/O bus to determine if the carriage has reached position mode. During carriage positioning, the CPU allows new data to be entered into the buffer and executes and supervises other operations.

The second part of the normal print cycle is printwheel positioning. Printwheel data is in the form of an ASCII character which must be converted to a printwheel delta counter value. When the command is ready to be set up for execution, the CPU loads the data into internal read/write (scratchpad) memory and performs a series of operations to determine printwheel rotational direction and the number of printwheel clock pulses to be loaded into the printwheel delta counter. When these computations have been made, the CPU loads the delta counter with the required information

and the printwheel positioning cycle required begins. While the printwheel is moving, the paper feed and ribbon feed cycles are also being executed.

Ribbon feed is determined by the character to be printed, and the CPU "looks up" the character width code in ROM and outputs the number of ribbon feed clock cycles to advance the ribbon the required amount. This function is not programmed by the external data source.

Paper feed data is moved from the buffer to a RAM register which counts the required number of paper feed clock cycles. Timing is determined by a counter which counts down the system master clock (termed the Clock) to generate a square wave with a 4 ms period. The CPU outputs the paper feed clock in synchronism with this clock signal.

The last action in any print cycle is firing the printhammer. When all other functions have been performed, the CPU outputs a hammer command consisting of a pulse whose width varies with the density of the character to be printed. Timing is determined by the programmable timer which is loaded with a pulse width count and interrupts the CPU when the timer has timed out. This shuts off the hammer drive and returns the CPU to the main program.

3.4.4 TIMING

Unlike previous printers, the Sprint 3 Series digital controller is mainly software-dependent for cycle timing. The master clock for the controller is the " " clock from the CPU whose frequency is controlled by a 2MHz crystal. This signal is buffered to provide MCLK, which is used for snychronization throughout the controller.

Through software, input and output data timing signals are generated by the CPU and transmitted to the rest of the controller using CPU selector I/O port A. The data input control lines are IPO - IP4 and the output control lines are OP1 - OP3. These are decoded by a one-of-ten decoder shown in the lower right portion of the schematic diagram.

Ribbon and paper feed are similarly software-controlled. Paper feed is synchronized by a frequency divider which divides down MCLK to provide a square wave with a period of 8 ms. When a paper feed function is programmed, the software enables the frequency divider. At the first negative-going transition of the T2 clock, the paper feed clock signals are output from 3851 I/O port A. The number of clock pulses output is determined by the number of paper feed increments given in the paper feed command. Ribbon feed is accomplished by using the timer to control the duration of ribbon feed pulses.

CHAPTER IV

SUPPORT EQUIPMENT LIST

This chapter contains a consolidated listing of the supplies and equipment required to support the Sprint printers at the field service or depot maintenance levels.

4.1 TOOLS AND TEST EQUIPMENT

Table 4-1 list the tools and test equipment required for the maintenance and repair of the high-speed character printers. If equivalent items are available, they may be substituted for those listed. Repairmen on rountine field service calls should be provided with one of each of the items in Table 4-1, in addition to the normal complement of hand tools.

4.2 SPARES

Repairmen making rountine service calls should have one each of the complete subassemblies listed in Table 4-3 in addition to a spare printwheel and ribbon cartridge.

TABLE 4-1

TOOLS AND TEST EQUIPMENT

TOOLS	PART NUMBER
PCB Extractors	#80462
Printwheel Adjustment Tool, Outer Collett	#80471
Printwheel Adjustment Tool, Inner Collett	#80472
Printwheel Adjustment Tool, Disc	#80758
Platen Guage Adjustment Tool	#80751
Hammer Adjustment Tool	#80739
Printed Circuit Extender Set	#99025-03
Cable Tension Gauge	#80738
TEST EQUIPMENT	**PART NUMBER**
Printer Exerciser	#99000
Portable Exerciser	#80630
Oscilloscope	Tektronix 465
Multimeter	Simpson 260
Activity Monitor	#80740
LUBRICANTS	**PART NUMBER**
Watch Oil (Moebius Oil "Art. 8000")	#80341
Tellus Oil (Shell Oil "Tellus 25")	#80342
Polygrease	#80346
MISCELLANEOUS	**PART NUMBER**
Isopropyl Alcohol	-----
Platen Cleaning Fluid	Fedron®
Heavy Duty Degreaser	Formula 409®
Thread Locking Fluid, Loctite #222	#85160-01
Loctite #06, Super Bonder Adhesive	#85161-01
Dusting Brush, Soft Bristle	-----
Type Cleaning Brush, Stiff Bristle	-----
Lint-Free Cloths	-----

TABLE 4-2

RECOMMENDED DEPOT LEVEL SPARES

PART #	DESCRIPTION	PRINTER POPULATION		
		100	500	1000
80023	Carriage Motor Final Asy	1	3	8
80032	Cradle Asy	1	1	2
80037	Pulley Asy-Idler	1	2	3
80046	Paper Feed Motor Asy	1	2	4
80057	Clutch And Magnet Asy, Ribbon Drive	2	4	8
80142	Bail-Feed Roller	2	4	8
80160	Lever-Feed Roller Disable	1	2	3
80186	Lever-Impression Control	1	1	2
80202	Gear-Idler, Paper Drive	1	1	2
80207	Ribbon Drive, Stepper Motor	1	1	2
80336	P/W Motor-Encoded	1	4	7
80368	Photon Module-Carriage Home	2	5	8
80369	Armature Asy-Hammer	1	1	2
80374-01	Pad-P.W. Motor Stop	2	5	10
80374-02	Pad-Ribbon Bail Stop	2	5	10
80379	Coil Ribbon Lift	2	4	8
80380	Bail Asy-Ribbon Lift	1	1	2
80358	Link Asy-Guide Bearing	1	2	3
80610	Power Risistor 5 OHM	1	2	3
80686	Hammer	1	3	5
80687	Hammer Guide	1	1	2
80713	Spring Hammer	1	3	5
85127	Cable Carriage Drive	1	3	5
90612	P.C. Asy Card #1	1	3	5
90622	P.C. Asy Card #2	1	3	5
90632	P.C. Asy Card #3	1	3	5

TABLE 4-3

RECOMMENDED FIELD SERVICE SPARES

MODEL 3/35	PART #
Printed Circuit Board 1	90612-00
Printed Circuit Board 2	90622-00
Printed Circuit Board 3	90632-00
Carriage Assembly	80028-14
MODEL 3/45	**PART #**
Printed Circuit Board 1	90612-01
Printed Circuit Board 2	90622-00
Printed Circuit Board 3	90632-01
Carriage Assembly	80028-15
MODEL 3/55	**PART #**
Printed Circuit Board 1	90612-02
Printed Circuit Board 2	90622-00
Printed Circuit Board 3	90632-02
Carriage Assembly	80028-16
MODEL 3/X30	**PART #**
Printed Circuit Board 1	90612-03
Printed Circuit Board 2	90622-01
Printed Circuit Board 3	90632-03
Carriage Assembly	80028-17
MODEL 3/X40	**PART #**
Printed Circuit Board 1	90612-04
Printed Circuit Board 2	90622-01
Printed Circuit Board 3	90632-04
Carriage Assembly	80028-18
MODEL 3/WIDETRACK	**PART #**
Printed Circuit Board 1	90612-05
Printed Circuit Board 2	90622-00
Printed Circuit Board 3	90632-01
Carriage Assembly	80028-15

CARD GUIDE REGISTRATION ADJUSTMENT

The reference marks inscribed on the card guide should appear as in Figure 7-14. Registration should be re-checked following adjustment of the card guide depth, or any time that it is sufficiently imperfect to inconvenience the operator.

The easiest way to check registration is to print two consecutive lines of capital "I", at a standard spacing of six lines per inch. If the reference marks are in error, it will be necessary to adjust the card guide.

Adjustment may be made with the top cover of the printer removed. An offset screwdriver will be helpful in adjusting some printers. Later versions of the printer use socket head screws or hex head screws and require an Allen wrench or open-end wrench for the adjustment.

(1) First adjust the vertical alignment, by disabling the CARR test switch on the #1 printed circuits board, and moving the carriage to the center of the line.

(2) Loosen the two retaining screws (A) shown in Figure 7-14.

(3) Position the card guide to obtain the best alignment of the horizontal registration marks and the printed line, as shown in the diagram.

(4) Secure the card guide by re-tightening the two retaining screws.

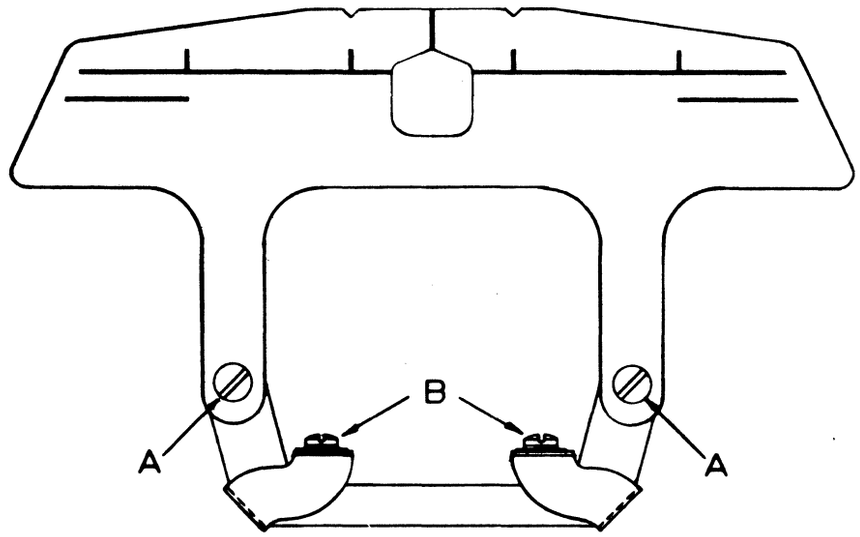


FIGURE 7-14

CARD GUIDE REGISTRATION

(5) Next adjust the lateral alignment of the guide. Move the carriage to the approximate center of the page, return the CARR test switch to its normal operating position, and print a single capital "I" for reference.

(6) If the vertical registration mark does not bisect the printed character, loosen the two retaining screws (B) shown in Figure 7-14.

(7) Position the card guide to obtain the best adjustment and secure it in place by re-tightening the two retaining screws.

(8) Again check the vertical alignment and re-adjust as necessary. This completes the registration adjustment.

7.2.5 RIBBON ADJUSTMENT

The only ribbon adjustment that requires attention in normal service is the ribbon lift height adjustment. This adjustment should be performed following replacement of the ribbon lift solenoid and following repair of replacement of damaged components. Occasionally it will be found that operator error has resulted in bending and misalignment of parts in the ribbon lift mechanism. The height adjustment should be re-checked at the time such a condition is corrected.

RIBBON LIFT HEIGHT ADJUSTMENT

The ribbon lift height adjustment should be checked by connecting the test exerciser to the printer and printing alternately the apostrophe (') and the underline (_). These two symbols represent the highest and lowest characters and should be the same distance from the top and bottom edge of the ribbon. Examine the ribbon, which should appear as in Figure 7-15, to determine whether the adjustment is necessary. If the symbols do not strike the ribbon as shown, proceed as follows:

(1) Use a screwdriver to loosen the two solenoid retaining screws (A) shown in the diagram.

(2) With the ribbon raised, position the solenoid to obtain a more favorable point of impact.

(3) Clamp the solenoid in place, by tightening the two retaining screws.

(4) Re-check the printing height, and repeat the preceding steps if necessary. This completes the height adjustment.

RIBBON DRIVE GEAR ADJUSTMENT

The drive gear on the ribbon motor must rotate freely with the large gear on the ribbon clutch and must be adjusted for minimum blacklash. Refer to 7-16.

(1) To adjust, loosen screws (B) and adjust location of motor. Tighten (B) .

(2) If insufficient adjustment is available by moving motor (Step #1) loosen fasteners (A) and adjust location of plate. Tighten fasteners (A) .

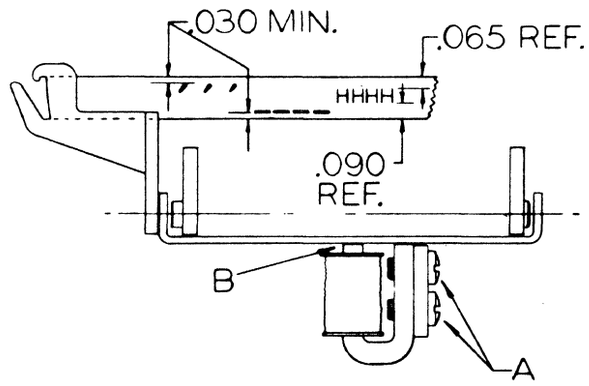


FIGURE 7-15
RIBBON HEIGHT ADJUSTMENT

7.2.6 CHASSIS

The only chassis adjustment that requires attention in normal service is the mother board alignment.

MOTHER BOARD ALIGNMENT

The mother board is aligned at the factory during assembly of the printer. It will seldom require further attention, but there may be some occasional difficulty in inserting and removing the power and interface connectors at the rear of the printer. Re-alignment is necessary in order to center the mother board's two connector tongues in the cutouts on the rear chassis panel. Proceed as follows:

(1) Remove power from the printer, and disconnect the interface and power plugs.

(2) Remove the top and middle cover sections from the printer, and withdraw the three printed circuit boards.

(3) Locate and loosen the eight pan-head screws that secure the mother board to standoffs on the printer's chassis.

(4) Re-insert the power and interface connectors in their respective positions, and tighten down the jackscrews that hold these connectors in place.

(5) Now re-tighten the eight retaining screws that secure the mother board to its standoffs. This completes the adjustment.

DUAL CARRIAGE BEARING CARRIER ALIGNMENT

The model S3-55 and the Widetrack printers are equipped with a dual carriage bearing carrier. This alignment procedure is necessary only when the carriage or bearing carrier are replaced.

To align the bearing carrier, proceed as follows:

(1) Prior to installing carriage in printer, install 1/2" carriage shaft under dual bearing carrier.

(2) Install tensioner spring loading dual bearing carrier against shaft.

(3) The centerline of the dual bearing carrier must be in line with the centerline of the carriage shaft.

(4) Move the shaft back and forth. The bearing carrier must not tilt or rock in any way. If so, bearings are not aligned properly.

(5) If alignment is necessary, grasp link with pliers at point A refer to Figure 7-17 and twist carefully until carrier is aligned properly. Repeat steps 4 and 5 until alignment is correct.

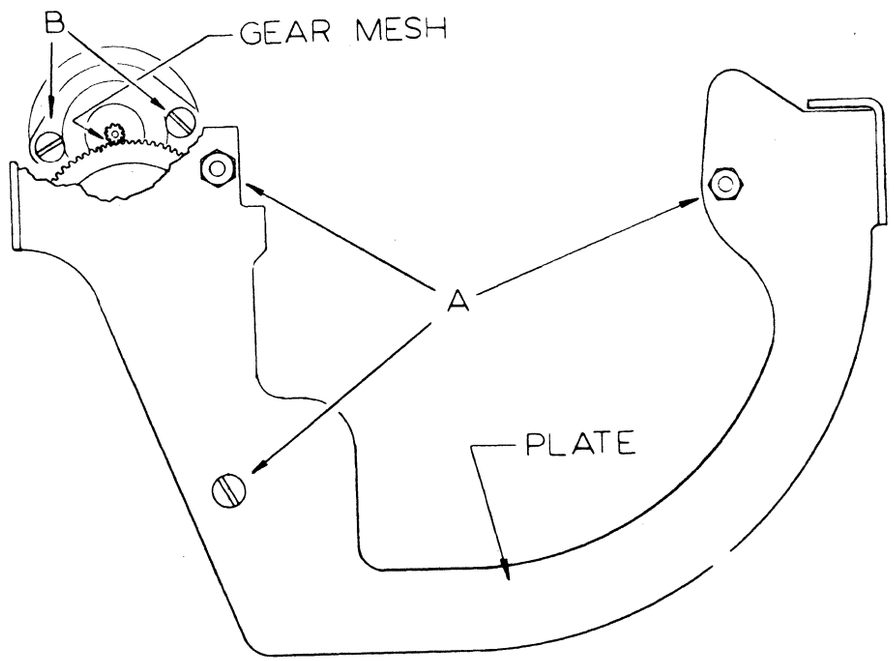


FIGURE 7-16
RIBBON DRIVE GEAR ADJUSTMENT

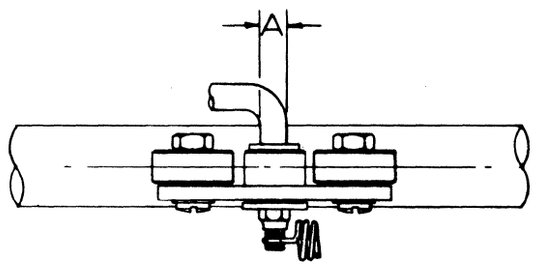


FIGURE 7-17
DUAL CARRIAGE BEARING CARRIER ALIGNMENT

CHAPTER V

MAINTENANCE

Periodic cleaning and lubrication are necessary to keep the Sprint Series printers in good working order. This chapter describes the scheduled maintenance procedures. Observe carefully all precautions with regard to the use of solvents and lubricants. Refer to Chapter IV for the Qume part numbers of maintenance items mentioned below.

5.1 MONTHLY

The printer should be checked monthly for general interior cleanliness, and the accumulated buildup of paper fibers should be removed. Use a soft-bristle brush to clean the carriage assembly carefully. Follow up with a soft cloth, using this to wipe the carriage guide rails and to mop up the interior generally. Clean up any ink residue on plastic or metal parts with a cloth moistened in FORMULA ® cleaner. DO NOT SPRAY SOLVENTS DIRECTLY INTO THE INTERIOR OF THE MACHINE, since they may contaminate lubrication points.

5.2 SEMI-ANNUALLY

Every six months, in normal operation, or after 300 hours of continuous printing use a medium grade oil (Shell "Tellus 25") to saturate the eight oiler pads of the ribbon feed drive gears. Refer to Figure 5-1.

5.3 ANNUALLY

Once a year, in normal service, the middle cover section should be removed, and the entire printer given a thorough cleaning.

Remove the printed circuit boards from their connector slots and examine them for general cleanliness and electrical integrity. Be alert for the discoloration that indicates overheating of components. Clear away any dust accumulation, using a soft-bristle brush. Grease film may be removed by rinsing in isopropyl alcohol and scrubbing gently with the brush. Take care not to get alcohol on any of the printer's rubber parts.

With the printed circuit boards removed, clean the interior of the printer. Use low velocity compressed air, if available. If not, brush-and-wipe will be sufficient. The object is to remove any dust that might clog the mechanism or impede the transfer of heat from electrical components. Test the carriage and paper feed mechanisms by hand for smoothness and freedom of operation.

Replace the printed circuit boards carefully, making sure that they have been seated properly in their mating connectors. Re-install the printed circuit board clamp, paying special attention to selecting the proper grooves to correctly space the boards. Re-install the printer's covers.

5.4 AS REQUIRED

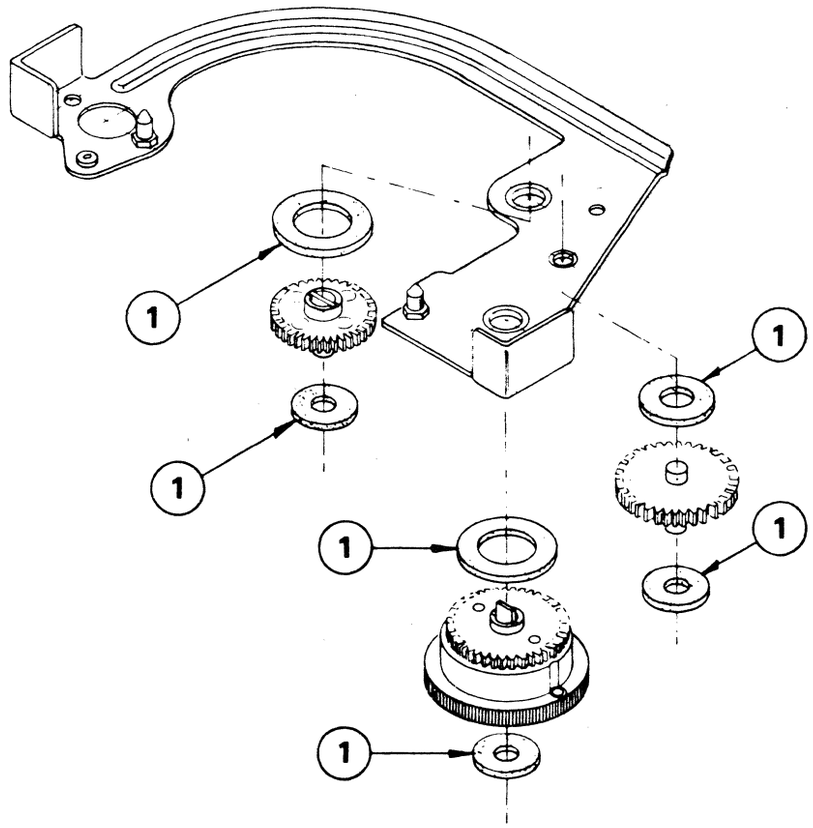
In time, ink from the ribbon will accumulate on the plastic card guide, obscuring the operator's view of the printing area. The card guide may be cleaned easily with a soft cloth moistened in FORMULA 409®. Use a clean cloth, to avoid scratching the transparent surface. If you use isopropyl alcohol to clean the card guide, avoid contact with the platen and with the paper feed rollers. Alcohol tends to harden the rubber surface, causing accelerated deterioration and erratic paper feed.

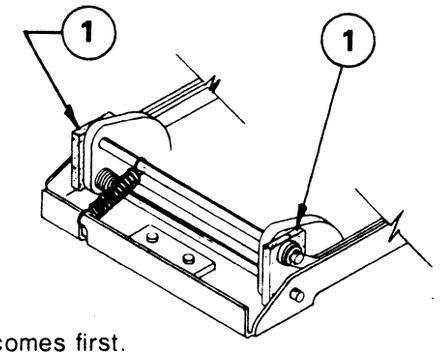
Occasional cleaning of the hammer and hammerguide may be necessary. Flush the hammer and guide with Freon or Alcohol, dry thoroughly, lubricate with a small drop of Moebius 800 (Watch Oil) at the front and rear. Caution, do not over-lubricate.

After the printer has been in service for some time, the printwheel may become clogged with ink and paper fibers. This problem is most acute in printers that use the nylon ribbon, where the printwheel die actually contacts the ribbon's inked surface during printing. Cleaning will be necessary whenever there is a noticeable deterioration in the clarity and definition of the characters printed. The need will vary, according to the severity of use and the quantity of output.

Remove the printwheel from the carriage for cleaning. Select a stiff brush with short, fine bristles (a regular type cleaning brush, or even a medium toothbrush works fine). Saturate this in FORMULA 409® cleaner, and use it to brush away all traces of greasy residue embedded in the printing dies. PROTECT YOUR CLOTHING FROM INK SPATTERS DURING THE CLEANING OPERATION. When you have finished, wipe the printwheel dry with a clean, lint-free cloth and re-install it on the carriage.

When it is necessary to clean the platen, or other rubber parts of the paper feed mechanism, use FEDRON® platen cleaner only. It is best to remove the platen entirely from the printer, to gain access to the feed rollers underneath. DO NOT GET PLATEN CLEANER ON ANY PLASTIC PARTS. Note that FEDRON® is highly flammable. Observe all precautions on the label.





(1) Saturate with 80342 Tellus Oil.

* Service is recommended every 6 months or 40 Million Print Cycles (300 hrs. continuous printing) whichever comes first.

FIGURE 5-1
LUBRICATION CHART

When the printer's plastic cover becomes soiled, it may be cleaned, using a cloth moistened with FORMULA 409® cleaner. Do not spray cleaners on the printer, since they may inadvertently get into portions of the printing mechanism.

CHAPTER VI

TROUBLESHOOTING

GENERAL

Troubleshooting is complicated by the interrelationship between printer and controller. The printer obeys the commands of the external controller without question: if the carriage is commanded to move in the wrong direction, it will do so. Before attempting to troubleshoot the printer, be sure that the controller and interface are operating properly. If it is determined that the controller and interface are operating correctly, use the procedures below to isolate the problem so that you can either replace the defective board or be advised by Qume customer service personnel what action to take to correct the problem.

DIAGNOSTIC PROCEDURES

This procedure utilitzes the optional Micro 3 Activity Indicator to isolate faults. The other equipment required is a digital voltmeter capable of measuring the power supply voltages.

(1) Remove the printer top covers.

(2) Either disable the external controller so that no data will be input during the diagnostics or disconnect the data cable from the printer.

(3) Using the digital voltmeter, measure the power supply voltages at the test points on each board. They should be within the tolerances specified in below.

+ 5V	±	3%	-	4.85V	to	5.15V
+15V	±	10%	-	13.5 V	to	16.5 V
-15V	±	10%	-	13.5 V	to	16.5 V

ACTIVITY MONITOR OPERATING INSTRUCTIONS

The diagnostic will begin running at the first test whenever the Micro 3 Activity Monitor is connected, the ON/OFF switch in "ON", and the program starts execution at location hexadecimal 0000. The program begins execution there after power up, after a Restore command is input, and when the RESTART button is depressed.

The printer exerciser may be connected when the diagnostic is run -- in fact, it is an advantage having it connected because the status lights may provide additional clues in cases of trouble, and it may be used to input a Restore command whenever necessary.

1. Turn power off. Connect the Micro 3 Activity Monitor cable connector to board 2 40 pin connector at the top of the board.

   IMPORTANT: The connector on the Micro 3 Activity Monitor must be oriented so the "FRONT" label marking is facing you when you are at the front of the printer, and the connector must be plugged in so pins 1 and 40 align on both connectors.

2. Turn the ON/OFF switch to "ON".

3. Turn on the power. The diagnostic will begin immediately.

4. If the test stops, note the TEST lights. The interpretation of these lights can be found in table 6-1 and also on the bottom of the Micro 3 Activity Monitor. The 4 test lights indicate the test that failed, see Test Light Pattern in the following table, and the 8 bit lights indicate the test mode, see Error Indicators On Error Stop.

   If the stop is in the ROM, I/O Lines, or Restore tests, the problem should be corrected before proceeding.

   If the stop is in the Carriage or Print Wheel tests, the CONTINUE button may be depressed to skip to the next test if the program stops in a tested error condition (see test descriptions above); and the bit lights will be effective in providing the reason for the stop (interpretation as in 3 above)

5. The diagnostic will automatically restart itself after finishing the Paper Feed Test. To stop the diagnostic and enable input to the printer through the I/O interface, turn the ON/OFF switch to "OFF" and depress the RESTART button. The exerciser may now be used for input.

6. To restart the diagnostic, turn the ON/OFF switch to "ON" and depress the RESTART button.

   A description of the diagnostic program can be found beginning on page 6-4.

TABLE 6-1

DIAGNOSTIC TEST PATTERN

TEST	TEST LIGHT PATTERN	OPERATION	ERROR INDICATORS ON ERROR STOP
ROM	0011	Adds all bytes of printer and diagnostic ROM programs. Sum must be zero.	Actual Sum.
I/O LINES	0001	Writes and reads each bit of I/O lines for isolation of bus line shorts. Compares written pattern to read pattern.	Actual pattern that caused error. Expected pattern can be deduced from lighting sequence.
RESTORE	0110	Executes Restore part of Printer program.	Not meaningful. Malfunctions can be seen by visual inspection.
CARRIAGE	0010	Carriage moves 114 times, back and forth, in diminishing movements, and sent to home and Limit. All bit positions of carriage delta are checked.	0 0 0 0 0 0 0 1 - Check 0 0 0 0 0 0 1 0 - Timed Out 0 0 0 0 0 1 0 0 - Limit on home 0 0 0 0 1 0 0 0 - Limit not found
PRINT WHEEL	0100	Slowly moves printwheel and stops at position 00. Printwheel moves 96 times, clockwise and counter clockwise in diminishing movements, and sent to index. All bit positions of printwheel delta are checked.	0 0 0 0 0 0 0 1 - Counter 0 0 0 0 0 0 1 0 - Timed out 0 0 0 0 0 1 0 0 - No index at end
PAPER FEED	0101	Executes various combinations of forward and reverse paper feeds and character printing. Ends with "QUME CORP" printed vertically. Test uses PRINTER program.	Does not stop. Errors seen in visual inspection.
TEST OVER	0111		

Notes: Continue test button is effective only after an error stop in either the CARRIAGE test, or the PRINT WHEEL test after the initial move to position 00.
A second RESTORE is performed just before the PAPER FEED test. Restore, Paperfeed, Ribbon Lift, Hammer, and Ribbon Advance errors are detected exclusively by visual inspection (during PAPER FEED test except RESTORE). Diagnostic does not test Ribbon Drop; nor does it test the external I/O interface which includes status lines, control lines, and data lines and associated circuitry.

TEST DESCRIPTIONS

ROM TEST

This test is to determine if the 3851 ROM* containing the diagnostic and the printer programs on board 2 is good. It adds all the bytes in the main program and the diagnostic program to develop a single-byte sum, excluding carries, which should be zero. The last byte in the diagnostic program is adjusted to be the two's complement of the sum of all the previous bytes.

Since the microprocessor is very fast, this test executes in a fraction of a second and will be seen as a fast blink on the TEST lights if the ROM is O. K.

A ROM failure causes the test to stop and the eight I/O bit lights display the actual sum. The CONTINUE button will not be active, since continuing the diagnostic may cause unusual things to occur because the main program or the diagnostic program is incorrectly stored in the ROM.

IMPORTANT: The test itself may not finish if the diagnostic program part of the ROM or the 3850 CPU or the power-up logic is defective.

I/O LINES TEST

This test is to determine if the I/O lines are operating properly. These lines are used for data communication between the microprocessor and the 74412 buffers, printwheel absolute counter, printer status, and printwheel and carriage delta counters. Any shorts to ground, +5, or each other either directly or through faulty components will cause improper operation.

The test sends out a pattern which will light a single bit light, starting with bit zero and proceeding sequentially to bit 7. After each pattern is output, it is input and compared to the pattern output. If the two patterns are different, the test stops and the bit lights display the erronous pattern input. The bit lights should be watched during the test so that if it fails the expected pattern (the pattern output), will be known. If the line is low (ground), the light lights.

The CONTINUE button will not be active because the tests following are dependent on the I/O lines working satisfactorily.

RESTORE TEST

This test is necessary at this time to establish a reference for the carriage and printwheel tests following it. It uses the actual Restore part of the printer program.

The carriage should be observed during this test. Failure to execute the Restore will cause the test to "hang up" in one of four program loops described below.

* Initial production printers use PROMS.

In the first loop, the carriage is slowly moved to the left until the carriage limit is sensed. The carriage may not move, in which case any one of a number of things can be wrong. Maybe the carriage delta counter is not receiving the data (hexadecimal 1007) or the counter output is not getting to the analog section, or the latter is inoperative, or the carriage limit sensing is faulty. If the carriage delta counter is not receiving the data, the port selection logic may be inoperative. OP2 and OP3 should be going low and high. The carriage may go in the wrong direction if the direction bit is lost. Or the carriage may travel at the wrong speed, indicating a faulty delta counter, velocity ROM, or analog section. Finally, the carriage may not find the limit and go into check, in which case maybe the carriage limit senser is faulty or selection logic IP4 is inoperative or the connection between the limit senser and the I/O lines is missing.

In the second loop, the carriage is sent to the right out of the limit. If the carriage doesn't move right, make sure it is not in check. The data output to the carriage delta counter is hexadecimal 0001.

In the third loop, a hexadecimal 07 is repeatedly sent to the printwheel delta counter until the printwheel passes position 00, the printwheel index position, at lower case "w". The printwheel may not turn, or it may turn too fast and/or it may never stop. Similar reasoning may be applied to the printwheel that was applied to the carriage. The senser in this case is the printwheel index which also uses IP4 selection.

In the fourth loop, printwheel position mode is sensed and the program loops until the condition is true. IP3 is selected for this sensing.

IMPORTANT: The CONTINUE button will not be active if the printer fails the Restore test, and the bit lights will not be relevant.

CARRIAGE TEST

This test contains two program loops. The first and main loop does the following:

1. Removes and saves the direction bit from a RAM register containing the last carriage delta output to the carriage delta counter.

2. Subtracts a constant from the resulting delta magnitude of 1 above.

3. Tests the result of 2 above. If it is less than zero, the main loop is done and the program branches to the second loop.

4. Complements the direction bit saved in 1 above and combines it with the new delta of 2 above.

5. Sets a time limit for the carriage travel.

6. Outputs the delta of 4 above.

7. Tests position mode. If true, goes to step 1.

8. Tests the elapsed time. It if is over the value set in 5 above, sets bit light value and jumps to error routine (described later).

9. Tests if check occurred. If so, sets bit light value and jumps to error routine.

10. Jumps to step 7.

Initialization for the main loop is with the first carriage delta value and a jump to step 5.

Following the successful completion of the main loop, the program outputs a carriage delta which should send the carriage almost to home position, initializes a 1/2 step counter, and then jumps into the second loop at step 2. The second loop:

1. Outputs a hexadecimal 1001 (1/2 step left) to the carriage delta counter.

2. Tests for carriage position mode and carriage limit. If both are true, exists loop. If not in position, repeats this step.

3. If in position mode but not at limit, decrements 1/2 step counter and tests it. If it is not zero, jumps to step 1.

4. If the 1/2 step counter is at zero, sets bit light pattern and jumps to error routine.

Following completion of the second loop, the 1/2 step counter is tested. If it is at the value it was initialized to, the bit light pattern is set and program jumps to error routine. The carriage should not be at the limit on the 'home'.

IMPORTANT: Notice that the second loop does not test for a check condition. After passing the first loop without a check, the chances of having a check in the second loop are remote. A check in the second loop will "hang up" the test, and the bit lights will not be relevant. Furthermore, the CONTINUE button will not be operative.

PRINTWHEEL TEST

This test also has two program loops, of which the second loop is the main one.

The first loop does one thing--send the printwheel to the index. It does this by testing whether the printwheel is in position 00, outputting a hexadecimal 01 to the printwheel delta counter if it is not at the index, briefly waiting, and then jumping to the beginning of the loop.

IMPORTANT: If the printwheel absolute position counter is faulty, the printwheel may not stop and will "hang up" at this point in the test. The bit lights will not be relevant if this happens and the CONTINUE button will not be effective.

After completion of the first loop (not necessarily proving that the printwheel is really at the index), the program initializes the first printwheel delta value and the first value of the software-controlled printwheel absolute position counter and jumps into the main loop at step 7. The main loop:

1. Removes and saves the direction bit from a RAM register containing the last printwheel delta output to the printwheel delta counter.

2. Subtracts a constant from the resulting delta magnitude of 1 above.

3. Tests the result of 2 above. If it is less than zero, the main loop is done and the program branches to the final operation in this test.

4. Complements the direction bit saved in 1 above.

5. Updates the software-controlled printwheel absolute counter using the new delta in step 2 and based on the direction bit in 4 above (either adds or subtracts the delta to/from the counter).

6. Combines the new direction with the new delta.

7. Sets a time limit for the printwheel motion.

8. Outputs the delta of 6 above to the printwheel delta counter.

9. Checks for printwheel position mode. If false, tests elapsed time. If not over the value in 7 above, repeats this step. Otherwise, sets bit light pattern and branches to error routine (described later).

10. In position mode, the printwheel absolute position counter is input and compared to its software-controlled counterpart. If the two counters are not equal, sets bit light pattern and branch to error routine.

11. Jumps to step 1.

Following successful completion of the main loop, the program outputs a printwheel delta that should send the printwheel to the index. The index is tested after position mode is established and a short delay. If the printwheel is not at the index, the bit light pattern is set and the program jumps to the error routine.

Another Restore is performed at this point to initialize the carriage to home, and to initialize the RAM registers for main printer program use for the following test.

PAPER FEED TEST

This test uses the main printer program. Just prior to the command input part of the main program, the program branches to the diagnostic program if the Micro 3 Activity Monitor is connected. The diagnostic then loads a printwheel or a paper feed command into the next available position in the software input buffer, tests the buffer to see if it is full, and sets an appropriate 'comeback code'. The diagnostic then jumps to the point in the main printer program which is just after where it stores a command into the software input buffer.

As long as the 'comeback code' is not a buffer full type, the above happens and the main program executes the commands in the buffer as though they came in through the external I/O interface.

When the software input buffer is full, the diagnostic ceases to load it until it becomes empty so it can adjust buffer pointers. It does this because four bytes at the end of that buffer are used by the diagnostic program.

The result of the paper feed test is a vertical printing of "QUME CORP" produced by a series of complex combinations of printwheel and paper feed commands. If the printer is working satisfactorily, the printing is reasonably evenly spaced (allowing for paper slippage) and spelled as above (without quote marks).

At the beginning of this test the ribbon should lift. It is not dropped at the conclusion of this test but is dropped at the beginning of the diagnostic. During the test, take note of the ribbon feed operating just prior to the printing of each letter.

IMPORTANT: This test has no internal checks and does not stop if a malfunction occurs. The results are seen during and after the test as mentioned above.

ERROR ROUTINE

This routine is used for all tested error conditions. Just before the program branches to it, it sets the bit light pattern to be displayed in the bit lights for the identification of the error, and it also sets the address of where the program may jump when the CONTINUE button is depressed. The routine displays the bit light pattern, delays, tests the CONTINUE button, and either branches to the address set if it was depressed, or branches back to the beginning of the error routine.

In the case of the ROM Test and the I/O Lines Test, the address set is the error routine so the CONTINUE button is not effective. In the Carriage Test it is the start of the Printwheel Test, and in the Printwheel Test it is the start of the Paper Feed Test.

CHAPTER VII

REPAIR

This section tells how to restore the high-speed printer to normal operation following replacement or repair of its major parts and subassemblies. Step-by-step procedures are given for the mechanical alignment of the printer.

A preliminary word of caution is in order. Despite its apparent mechanical simplicity, the printer is a highly sophisticated piece of machinery. In many cases, the tolerances and adjustments that are carefully established on the assembly line are simply not obvious to the untrained eye. Yet, failure to observe these tolerances can result in degraded output quality, in excessive stress, in accelerated wear, and in unnecessary premature failures. Only qualified personnel should attempt the repair of the high-speed character printers, and even these should be sure beforehand that they have read and understood the instructions thoroughly. At all costs, resist the impulse to tamper with adjustments or to disassemble parts of the mechanism indiscriminately. If in doubt, contact the factory service department for advice and instructions.

Every effort has been made to adjust your printer within the tolerances shown in this manual, however, individual measurement techniques and instruments vary and may indicate dimensions slightly outside of tolerances shown. This is not an indication that your printer won't perform perfectly, as generous safety margins exist outside of the tolerances. If readjustment is required every effort should be made to readjust to the specifications shown.

For the most part, the tools and equipment required for these adjustments are already available in the serviceman's tool kit. Whenever special tools, alignment fixtures, or test equipment are called for, they are noted prominently in the text. Section IV contains a consolidated listing of special tools and support equipment.

7.1 ROUTINE PROCEDURES

COVER REMOVAL

The high-speed character printer is equipped with a three-piece plastic cover. The uppermost section is a snap-on lid which protects the carriage mechanism during normal operation. To remove it simply grasp its front edge firmly, and lift upward. Removal of this cover trips an interlock switch which disables the printwheel and the carriage servomotors, protecting the operator from possible injury when changing ribbons or printwheels. Maintenance personnel may find it necessary to bypass this switch during routine servicing of the printer.

To obtain access to the interior, it will be necessary to remove the middle section of the cover. It is secured by three screws at the rear of the printer, and by several screws on the inside periphery of the cover itself. The latter are readily accessible when the top cover is removed. With the retaining screws loosened and the platen removed, the middle section may be lifted free of the printer chassis, exposing the remainder of the mechanism and the control electronics.

The bottom section is a dished cover which is bolted to the printer's chassis. Routine servicing does not require removal of the bottom cover.

REMOVAL OF PRINTED CIRCUIT BOARDS

The printer's control electronics is contained on three printed circuit boards, each having etched connector tongues which mate with corresponding slot connectors on the mother board.

For purposes of identification, these assemblies are numbered sequentially, beginning at the rear of the printer. The board at the rear of the unit is thus PCB #1; that nearest the front of the unit is PCB #3.

Removal and replacement of the electronic assemblies is routine. Use of an extractor, however, makes this task easier and minimizes the possibility of damage to the printed circuit boards. Always turn power OFF before removing or replacing any assembly. Connectors on the mother board are staggered, making it impossible to insert a printed circuit board in the wrong mother board position. When replacing printed circuit boards, be certain that they are seated firmly in their mating connectors.

7.2 MECHANICAL ALIGNMENT

Although mechanical misalignment can result in noisy operation or in damage to the equipment, the first indication is usually a visible deterioration of the print quality. Symptoms frequently observed include characters that are too light or dark, characters that are heavier at the top or at the bottom edge, characters that appear to taper and become uneven at one or both extremes of carriage travel, and characters that seem to fade out as the horizontal line is scanned. Maladjustment occasionally produces positional inaccuracies that are most evident in the smeared appearance of overprinted characters or in the ragged "picket-fence" aspect of the horizontal lines.

Misalignment of the printer is seldom the result of ordinary wear. More often it is attributable to an accident, or to physical abuse of the printer. Any unit subjected to a violent shock should be checked carefully for visible evidence of such maladjustment. However, re-adjustment will also be indicated as a matter of routine, whenever any of the following components and subassemblies are repaired or replaced:

(a) printwheel carriage
(b) printwheel servomotor
(c) printhammer solenoid
(d) ribbon lift solenoid
(e) carriage servomotor
(f) paper feed stepper motor
(g) platen, paper feed rollers, and/or platen drive gears
(h) plastic card guide

A complete re-alignment will seldom be called for, but, you must be careful to restore any and all adjustments that may have been disturbed. We therefore recommend that you read the following section carefully before beginning any repair. The preface to each procedure enumerates the conditions that make that particular adjustment necessary.

Note that the alignment procedures are grouped, as follows:

(a) printhammer adjustments
(b) platen adjustments
(c) paper feed roller adjustments
(d) carriage adjustments
(e) ribbon adjustments
(f) mother board alignment

There may be some interaction between adjustments that are grouped together, and we therefore recommend that all the procedures in a given group be performed at the same time. Observe the order of adjustments carefully, and take special note of those few cases where adjustments in one group necessitate re-checking adjustments in another.

7.2.1 PRINTHAMMER ALIGNMENT

Misalignment of printhammer adjustments usually produces characters that are too light or too dark, or characters that are uneven. Ocassionally, however, a faulty adjustment can cause noisy operation or printwheel breakage. In a few cases the serviceman will observe some slippage of the printwheel hub in relation to the servomotor's armature shaft, resulting in an uneven character impression, in chipping of the printwheel spokes, or in actual misprinting. Any of these symptoms may indicate the need for re-alignment of the printhammer. The adjustments should be performed as a group, in the order indicated below. All adjustments are performed with power OFF, except as noted.

Complete realignment of the printhammer assembly is also indicated whenever any of the following parts have been removed or replaced:

(a) printhammer
(b) printhammer actuating solenoid
(c) armature limit bumpers
(d) printwheel servomotor

PRINTHAMMER VERTICAL ALIGNMENT

Alignment may be performed with the top cover off, and with the printwheel and the platen removed from the printer. Correct adjustment requires the use of a special alignment tool (#80739). A screwdriver and a 3/16" wrench (or nut driver) will also be needed. Refer to Figure 7-1.

(1) Remove all power to the printer.

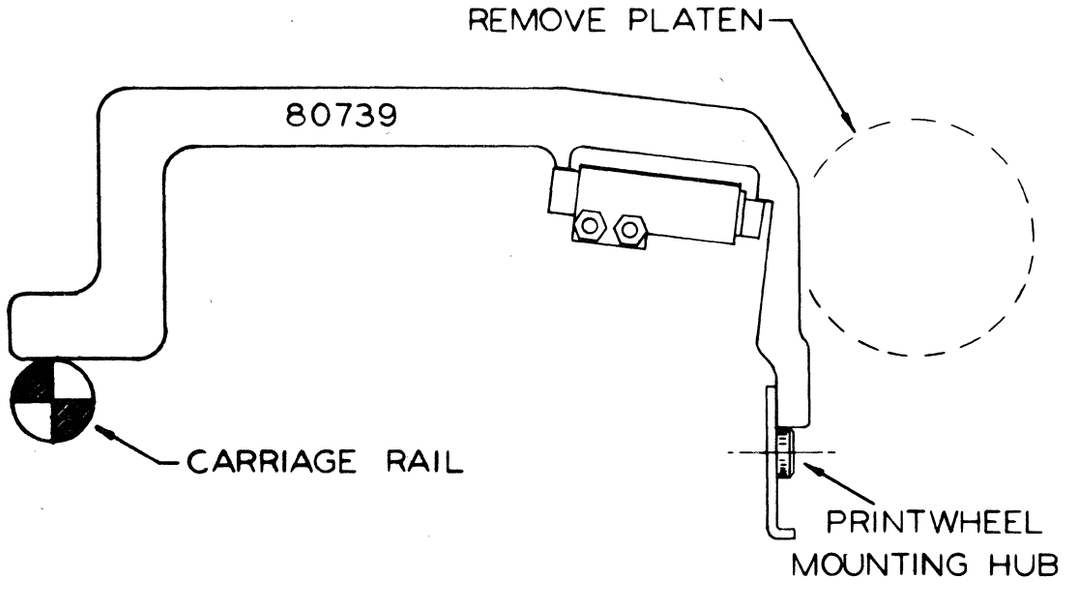
(2) Loosen the two printhammer retaining screws, which secure the printhammer housing to the carriage.

(3) Install the printhammer alignment gauge (#80739), as shown in Figure 7-1. Be certain that the upper carriage is locked in its normal operating position.

(4) Move the printhammer assembly into alignment. The movable hammer should contact the fixture lightly at both ends, as shown in the diagram.

(5) While holding the housing in this aligned position, re-tighten the two retaining screws. This completes the vertical alignment.

After adjusting the printhammer's vertical position, it is a good idea to run a print sample and check the evenness of the impression. Vertical misalignment produces characters that are darker at their top or bottom edge. If characters are heavier at the top, it may be necessary to raise the adjustment slightly, so that the hammer is more nearly horizontal. Characters that are darker at the bottom, on the other hand, suggest the need for lowering the hammer tip. Uniform appearance of the sample is the ultimate criterion to be applied.



PRINTHAMMER VERTICLE ALIGNMENT

FIG. 7-1

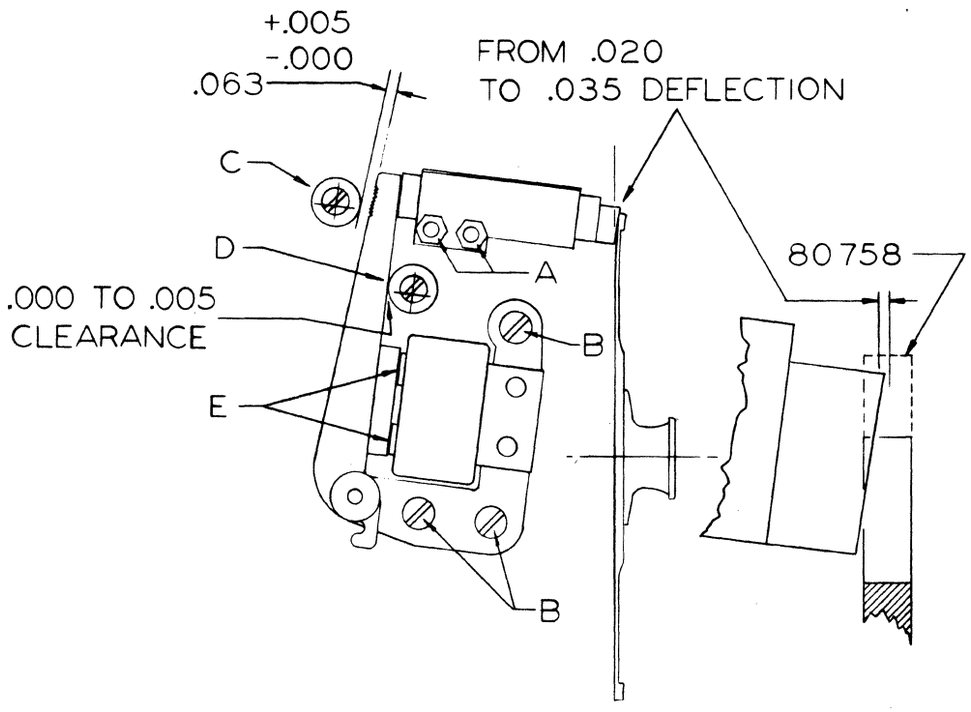


FIG. 7-1.1

Before re-adjusting the hammer, however, be sure to check the platen height adjustment as described in Section 7.2.2. Maladjustment of the platen can produce much the same result as faulty printhammer alignment, so the platen should be checked before concluding that the printhammer is to blame for a visible defect.

HAMMER ARMATURE CORE ADJUSTMENT

Adjustment may be performed with the top cover of the printer removed. This adjustment is preceded by the vertical alignment of the printhammer, as described previously. Tools required include the printwheel alignment disc and a screwdriver. Refer to Figure 7-2.

(1) Remove the printwheel from the carriage, and install the alignment disc in its place, so that the imprinted legend "THIS SIDE UP" is visible to the serviceman making the adjustment. Rotate the disc so that the round O.D. Section is near the hammer.

(2) Using a 3/16" wrench, loosen the retaining nut which secures the armature's eccentric forward limit bumper, and rotate the bumper itself to obtain maximum clearance between the bumper (D) and the armature lever. Refer to Figure 7-1.1.

(3) Now loosen the three armature core retaining screws (B) that hold the core in place.

(4) While using your left hand to pinch the armature lever against the core piece (E) , position the entire assembly so that the top of the printhammer protrudes inside the disc .020 "to .035", as illustrated in Figure 7.1.1.

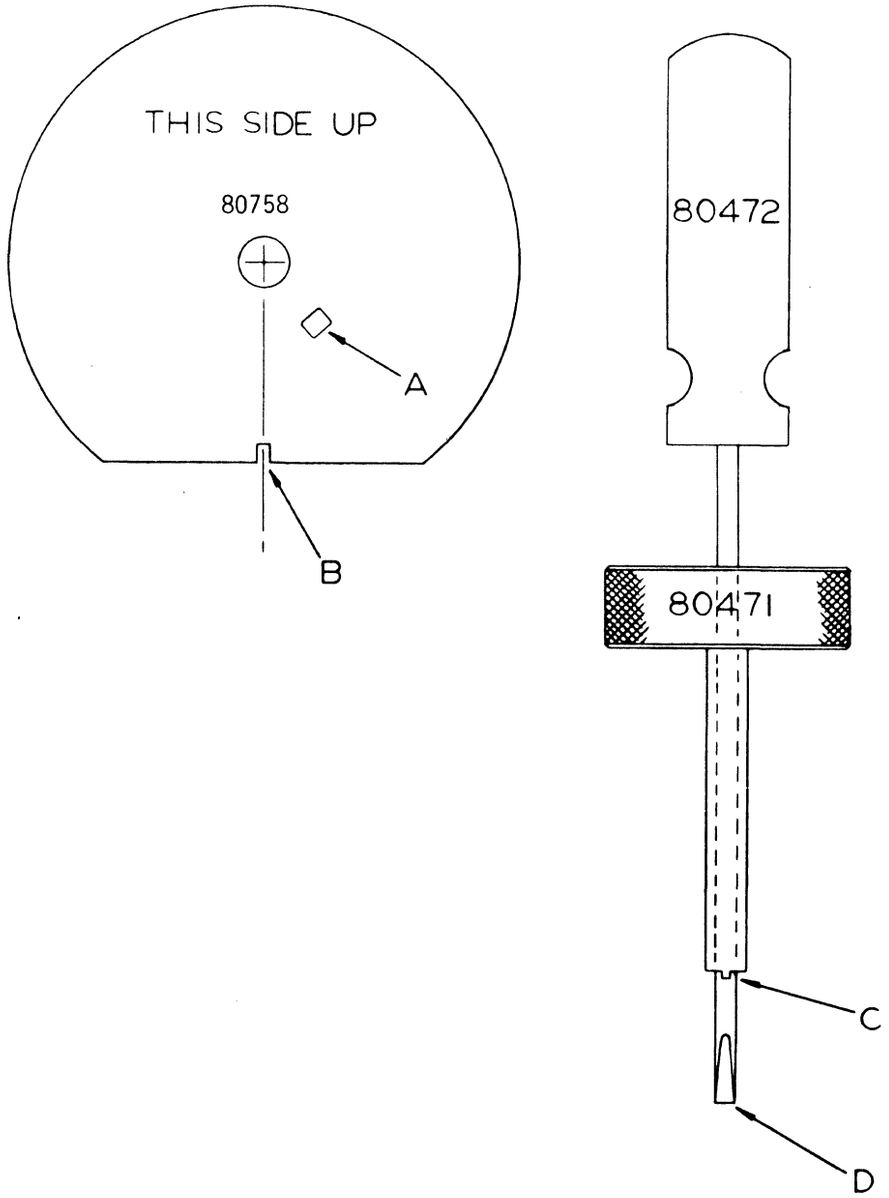


FIGURE 7-2
PRINTWHEEL ALIGNMENT TOOLS

(5) Hold the solenoid assembly in this position, and retighten the three core retaining screws. This completes the adjustment.

HAMMER ARMATURE FORWARD LIMIT ADJUSTMENT

Adjustment to the forward limit bumper is performed with the top cover removed from the printer. This adjustment should always be preceded by the armature core adjustment just described. A screwdriver and a 3/16" wrench will be required. Refer to Figure 7-1.1.

(1) Loosen the nut which retains the forward limit bumper.

(2) With one hand, pinch the armature lever to the core piece (E) .

(3) With a screwdriver, rotate the eccentric bumper, until the indicated clearance is obtained.

(4) Hold the forward limit bumper in that angular position with your screwdriver, and tighten the bumper's retaining nut. This completes the adjustment.

HAMMER ARMATURE RETURN LIMIT ADJUSTMENT

Adjustment of the hammer armature return limit bumper is accomplished with the top cover removed from the printer. This adjustment is always preceded by the forward limit adjustment, as just described. A screwdriver, a 3/16" wrench, and a .063 feeler gauge are necessary. Refer to Figure 7-1.1.

(1) Loosen the retaining nut that secures the return limit bumper (C) .

(2) With your left hand pinch the armature lever against the core. Rotate the return limit bumper to dimension shown. The feeler gauge should slide between armature bumper.

(3) Hold the bumper in this position with a screwdriver, and secure it by tightening the retaining nut. This completes the adjustment.

PRINTWHEEL INDEX ADJUSTMENT (HUB)

Although it is not technically a printhammer adjustment, printwheel alignment is normally performed at the same time as the other adjustments in that group. The printwheel's relative position can affect the accuracy with which the hammer tip strikes the uppermost spoke, and misalignment therefore produces symptoms such as uneven character impressions that are similar to those resulting from vertical misalignment of the printhammer. Extreme cases of maladjustment may result in broken spokes, or in printing of the wrong characters.

The printwheel hub adjustment is made to ensure that the printwheel mounted on the hub is in the correct angular relationship to the absolute index of the servomotor's encoder which is mounted on the other end of the shaft. Three special tools are required:

(a) hub collet adjusting tool, #80471
(b) a 1/8" diameter screwdriver, #80472
(c) reference disc, #80758

These are illustrated in Figure 7-2.

Adjustments are made with the printer energized. The printer's top cover must be removed and the cover interlock switch bypassed. Proceed as follows:

(1) Turn the printer on.

(2) Release the carriage locking lever by depressing the "0" button, and tilt the carriage all the way back.

(3) Remove the printwheel.

(4) Refer to Figure 7-3. Use the hub collet adjusting tool to loosen the hub collet. Hold the armature shaft stationary with the screwdriver handle, and twist the knurled knob counterclockwise slightly to loosen the hub collet.

CAUTION

Be extremely careful not to let the screwdriver tool slip out of the slot in the motor shaft. Insert the blade squarely, and use enough hand pressure to keep it seated firmly. If it slips, you may damage the tip of the screwdriver tool. This in turn may lead on some future occasion to a damaged armature shaft. The only alternative, once that happens, is total replacement of the printwheel motor-encoder assembly.

Never try to loosen the hub collet with an obviously damaged tool. Either obtain a new tool, or dress the

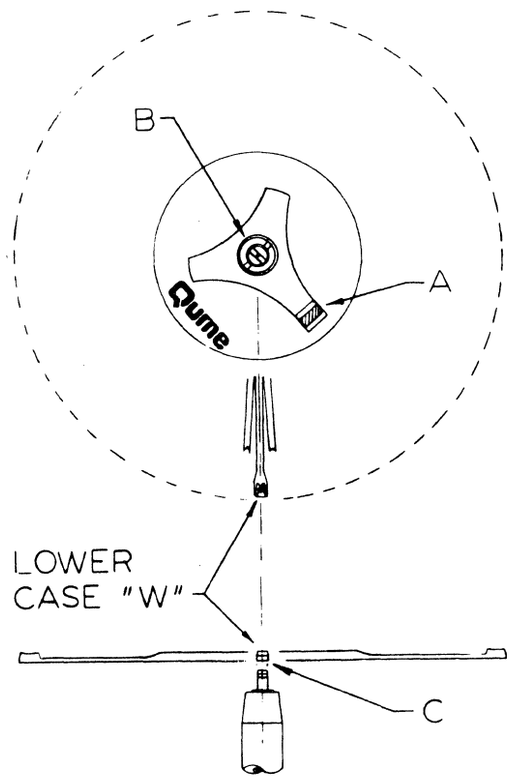


FIGURE 7-3
PRINTWHEEL INDEX ADJUSTMENT

blade carefully on a grinding wheel. If you have initial difficulty in breaking a collet loose, you would be wise to use a screwdriver with a slightly wider blade, which is less likely to slip out of the slot. The blade on the stock tool is deliberately narrower, to allow for complete removal of the collet.

(5) Use a test lead to ground pin #28 of the interface connector momentarily (the interface connector is located on the right side of the chassis as viewed from the rear. Refer to Figure 2-2 for orientation). This will cause the ribbon lift mechanism to operate briefly. When it returns to its rest position, the servomotor's shaft will be at the index (lower case "w").

(6) Mount the alignment disc on the printwheel hub, so that the imprinted legend "THIS SIDE UP" is visible to the serviceman making the adjustment.

(7) Wedge a folded bit of paper between the printhammer's armature and the spring-loaded printhammer, so that the tip of the printhammer is in an extended position.

(8) Rotate the alignment disc, and the hub, (but NOT the motor's shaft), until the extended tip of the printhammer engages the notch that is cut in the flatted edge of the disc (see Figure 7-2).

(9) Now use the collet adjusting tool to re-tighten the collet, taking care not to disturb the motor's angular position. Hold the armature stationary with the screwdriver and turn the knurled knob clockwise to secure the adjustment.

(10) Remove the alignment disc, and the paper wedge, and re-install the printwheel.

(11) Once again, use a test lead to ground pin #28 of the interface connector.

(12) Verify that the lower case "w" is in the 12 o'clock printwheel position.

(13) Move the printhammer slug forward by hand, and ensure that the tip of the slug meets the uppermost spoke squarely. Re-adjust the hub slightly, if necessary. Refer to Figure 7-3.

(14) Return the printwheel carriage to its operating position, and press the "C" button to lock it in place. This completes the hub adjustment.

7.2.2 PLATEN ADJUSTMENTS

Misalignment of the platen adjustments usually manifests itself in print quality that varies over the width of the page. Ragged lines, lines that taper, and lines that gradually fade from one side to the other are possible indications of platen misalignment. Difficulty in obtaining accurate overprinting or accurate vertical positioning may also indicate the need for platen adjustment. The platen should be re-aligned whenever any of the following are replaced:

(a) paper feed stepper motor
(b) paper feed idler gear
} adjust drive gear

(c) carriage
(d) printwheel servo motor
} adjust platen height/depth

NOTE: All adjustments are made with power OFF.

PLATEN DEPTH ADJUSTMENT

Adjustment of the platen's depth is performed to ensure that the forward surface of the platen is perfectly parallel to the rails on which the printwheel carriage travels. Misalignment produces characters that are too light or too dark, or characters that are darker on one side of the page than on the other.

The middle section of the printer's cover must be removed for access to this adjustment. Tools required include a screwdriver, a 5/8" open-end wrench, and the alignment gauge, #80751 shown in Figure 7-4.

(1) Place the forms thickness selector lever in its extreme forward position.

(2) Refer to Figure 7-5 which shows the right platen carrier side plate. Loosen the two screws (B) and (C) which secure the depth adjustment.

(3) Position the alignment gauge #80751 on the right side of the printer, as shown in Figure 7-4. The gauge rests on the printwheel hub (A) and on the forward carriage guide rail (B) and must be balanced or supported by hand Try to keep the gauge approximately perpendicular to the platen's principal axis.

(4) Use a 5/8" open-end wrench to rotate the eccentric anchor shown at (B) in Figure 7-5. Adjust this anchor so that the forward edge of the platen just touches the flattened vertical face on the alignment gauge (Figure 7-4).

CHAPTER VIII

ILLUSTRATED PARTS LIST

The following drawings show how the printer is put together. They will be a useful reference during maintenance, and will help you identify broken or missing parts. When replacing parts, always refer to the alignment instruction in Chapter VII, to be sure that you have correctly observed all the necessary adjustments.

Note that the printer mechanism has been divided into four sub-assemblies:

(a) structure (chassis)
(b) platen carrier
(c) upper carriage
(d) lower carriage

Each of these basic sub-assemblies is identified by an outline drawing in the upper righthand corner of the corresponding exploded view. The shaded portion identifies the sub-assembly and shows its relationship to the printer as a whole.

In the exploded view drawings, each part is identified by an index number, relating it to a description and to a Qume part number in the cross-reference listing. Refer to this part number and to the serial number of your machine when communicating with our customer service department.

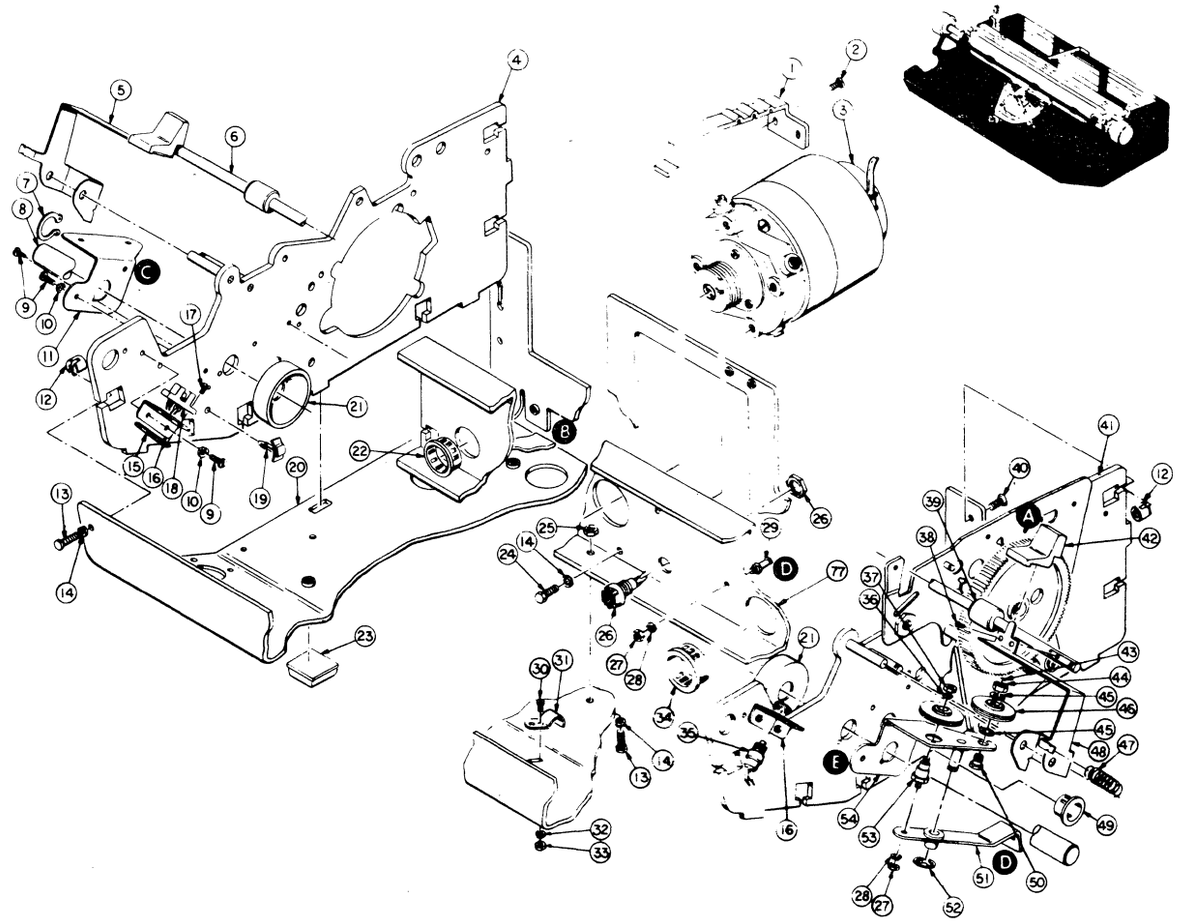
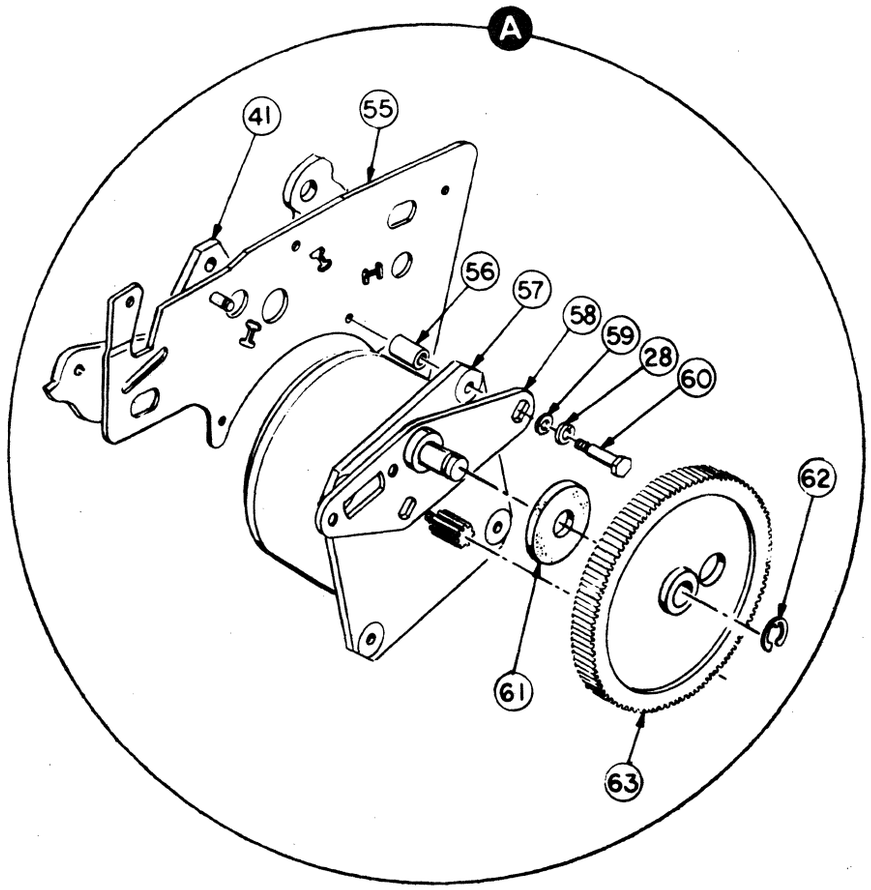
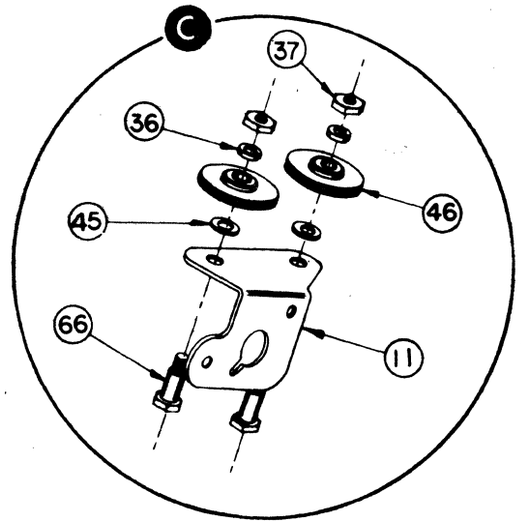


Figure 8-1. STRUCTURE ASSEMBLY





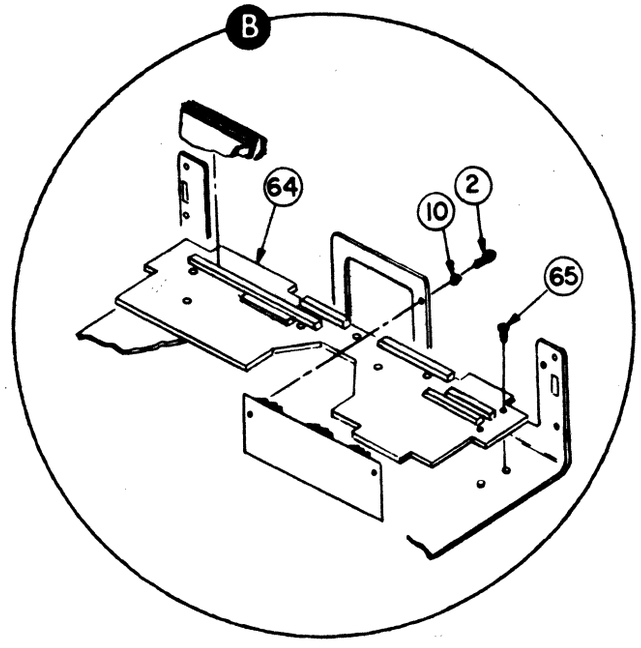
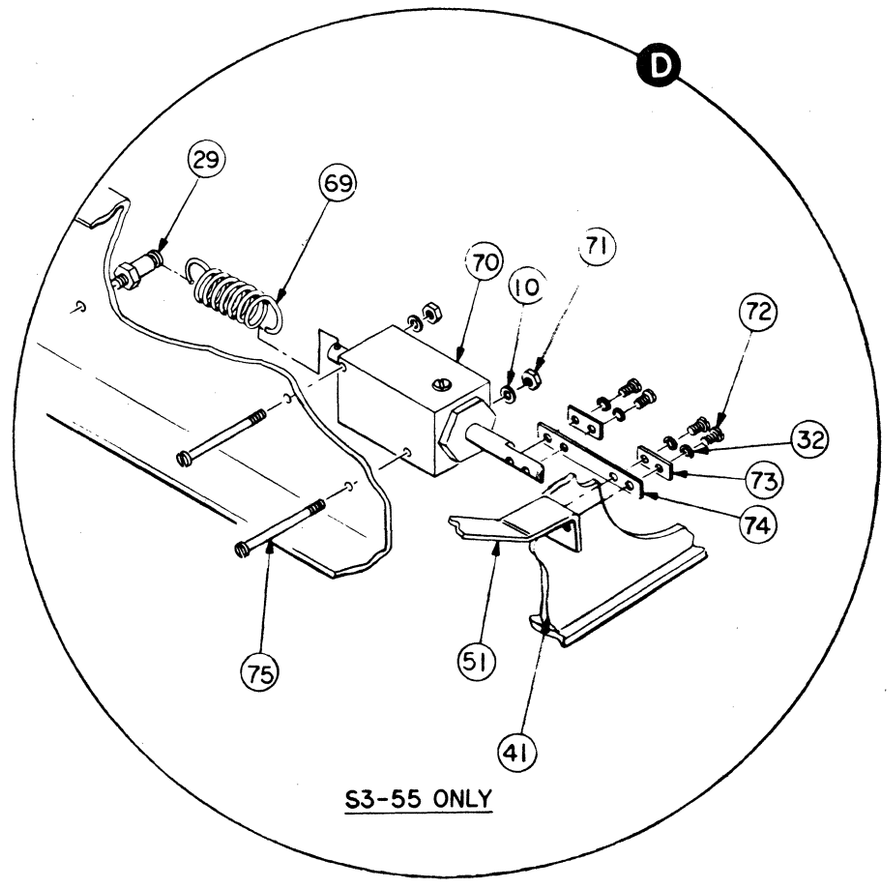


Figure 8-2. STRUCTURE DETAIL



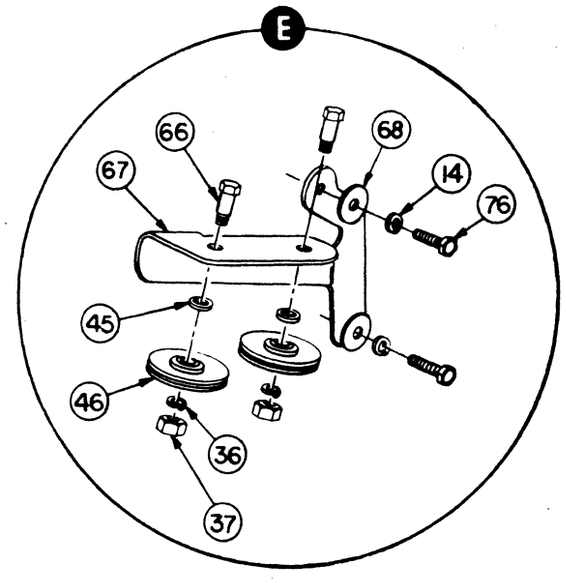


Figure 8-3. STRUCTURE DETAIL

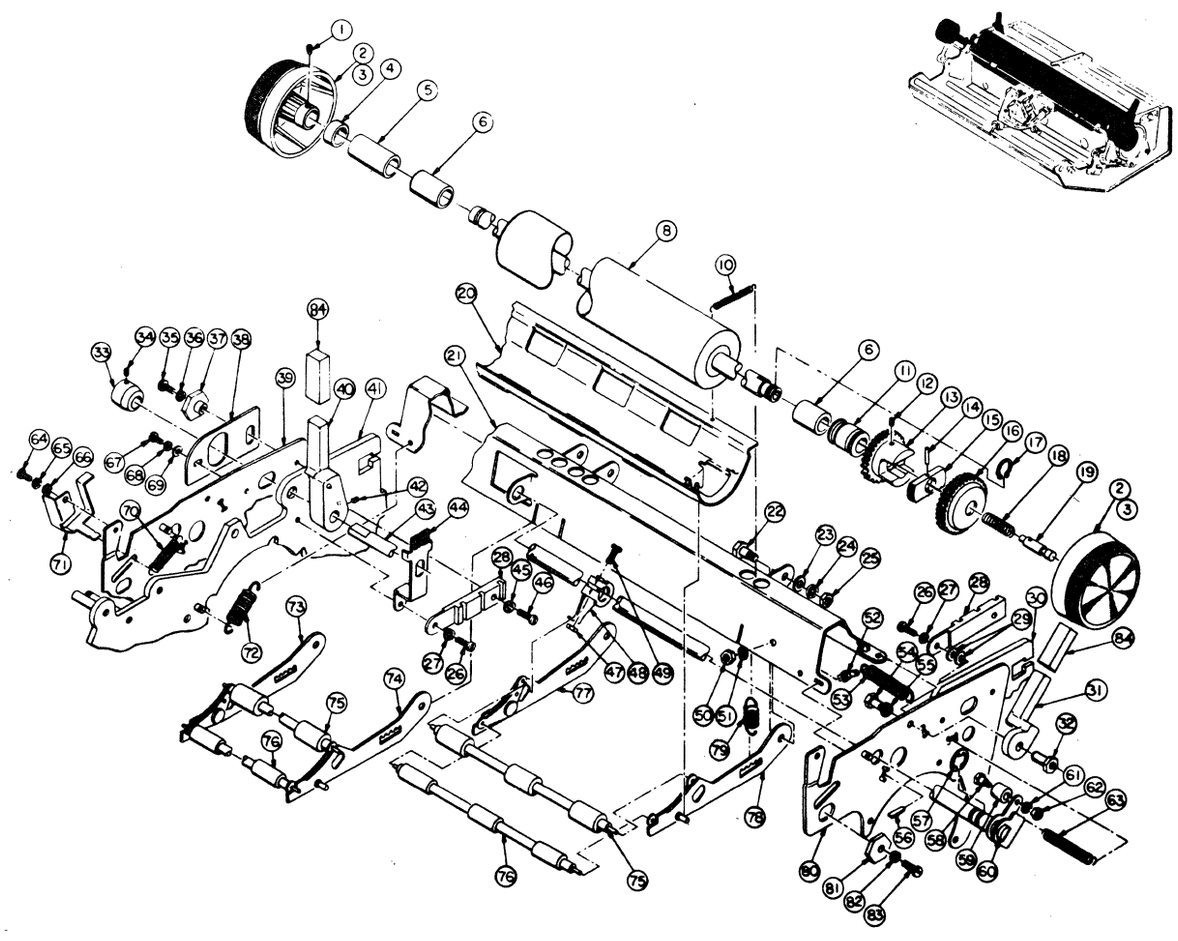
STRUCTURE ASSEMBLY

ITEM	P/N	DESCRIPTION	QTY.
1	80408	Clamp-P.C.B.	1
2	85006-05	Screw 6-32 x .312 Pan Head	4
3	80023	Carriage Drive Motor	1
4	80048	Frame Asy Left Side	1
5	80257-01	Arm Bail Roller-Left	1
6	80259	Shaft-Bail Roller	1
7	85129-50	Grip Ring	4
8	80116	Shaft-Carriage Guide	2
9	85006-04	Screw 6-32 x .250 Pan Head	10
10	85124-06	Washer #6-32 Helical-Lock	12
11	80106-02	Bracket Pulley-Left	1
12	80220	Retainer Nut	16
13	85058-10	Screw 10-32 x .625 Hex Head	15
14	85124-10	Washer #10 Helical-Lock	19
15	80405	Bar Nut-Photo Sensor	1
16	80404	Bracket-Ribbon Advance	2
17	85004-04	Screw 4-40 x .250 Pan Head	6
18	80368	Photon Module	1
19	85159	Snap Grip-Wire Fastening	2
20	80049	Pan Asy-Bottom	1
21	80719	Bumper-Carriage Deceleration	2
22	85157-02	Snap Bushing	1
23	85152-01	Foot SJ5123 Grey	4
24	85058-08	SCREW 10-32 x .5 Hex Head	4
25	85122-10	Nut 10-32	3
26	80610	Resistor Asy-Hammer 5 OHM 20W	1
27	85122-08	Nut 8-32	1
28	85124-08	Washer #8 Helical-Lock	2
29	80666	Screw Stud Platen Spring	1
30	85004-06	Screw 4-40 x .375 Pan Head	2
31	80246	Clamp-Cable	1
32	85124-04	Washer Helical-Lock #4	6
33	85122-04	Nut 4-40	2
34	85157-03	Snap Bushing	1
35	94038	Pushbutton Switch Ribbon Feed	1
36	85124-05	Washer # 5- Helical-Lock	4
37	85122-05	Nut 5-40	4
38	85074-04	Screw 4-40 X .250 Flat Head	4
39	80329	Sleeve Bail Roller	3
40	85068-10	Screw 10-32 X .625 Flat Head	4
41	80050	Frame Asy-Right Side	1
42	80320-01	Lever - Platen Bail Chrome	2*

STRUCTURE ASSEMBLY

ITEM	P/N	DESCRIPTION	QTY.
42A	80320-02	Lever-Platen Bail Charcoal Gray	2*
42B	80320-03	Lever-Platen Bail Cordovan Brown	2*
43	85138-12	Clip 5103-12	1
44	85122-10	Nut 10-32	1
45	80109	Washer R.R Pulley	4
46	80037	Pulley Asy-Idler	4
47	80237	Spring-Extension	2
48	80257-02	Arm Bail Roller-Right	1
49	85157-04	Snap Bushing	1
50	80108	Bushing R.R Pulley	1
51	80673	Link Asy S3-55	1
52	85128-25	"E" Ring	2
53	80107	Stud	1
54	80106	Bracket Asy-Pulley Right	1
55	80040	Frame Asy-Platen	1
56	80197-01	Spacer Motor Mount	3
56A	80197-02	Spacer Phillips Motor Mount	3
57	80046-01	Motor Asy-Paper Feed Low Current	1
57A	80046-02	Motor Asy-Paper Feed	1
58	80339	Plate Asy-Idler Gear	1
59	85125-08	Washer 8-32 Narrow Plain	3
60	85057-14	Screw 8-32 X .875 Hex Head	3
61	80398	Felt Washer	1
62	85128-31	E-Ring X5133-31	1
63	80202	Gear-Idler	1
64	90602	Printer Motherboard	1
65	85008-08	Screw 10-32 X .5 Pan Head	8
66	80523	Screw-Left Cable Pulley	4
67	80685	Bracket Pulley Right	1
68	85126-10	Washer #10 Plain	2
69	80664	Spring S3-55	1
70	80674	Dash Pot S3-55	1
71	85122-06	Nut 6-32 S3-55	2
72	85004-04	Screw 4-40 X .250 S3-55	4
73	80671	Plate S3-55	2
74	80665	Link S3-55	1
75	85006-20	Screw 6-32 1.250 Pan Head S3-55	2
76	85058-12	Screw 10-32 X .750 Hex Head	2
77	80223	Brace Carriage Motor Mount	1

* Optional



PLATEN CARRIER ASSEMBLY

ITEM	P/N	DESCRIPTION	QTY.
1	85207-02	Screw 8-32 x 1/8 Splined Socket	2
2	80045-01	Knob Asy Platen Charcoal Grey	2
3	80045-02	Knob Asy Platen Cordovan Brown	2*
4	80513-02	Spacer-Platen	1
5	80515	Spacer-Platen	1
6	80513-01	Spacer-Platen	2
7		Deleted	
8	80022-01	Platen, Rubber	1
9		Deleted	
10	80334	Spring, Cradle	2
11	80514	Spacer-Platen	1
12	85206-04	Screw 6-32 x 1/4 Splined Socket	2
13	80175	Gear - Tractor Drive	1
14	85237-04	Groove Pin .062 x .500	1
15	80176	Driver - Plain	1
16	80177	Gear - Platen	1
17	85129-31	Grip Ring 5555-31	1
18	80198	Spring - Compression	1
19	80594	Push Shaft - Platen	1
20	80032	Cradle Asy	1
21	80130	Brace - Platen	1
22	80159	Screw - Shoulder Feed Arm	4
23	85125-08	Washer #8 Narrow - Plain	4
24	85124-08	Washer #8 Helical - Lock	4
25	85122-08	Nut 8-32	4
26	85006-05	Screw 6-32 x .312 Pan Head	2
27	85124-06	Washer #6 Helical-Lock	2
28	80306	Guide-P.C. Board Mounting	2
29	85125-06	Washer	2
30	80050	Frame Asy Right Side	1
31	80160-01	Lever Casting - Feed Roller	1
32	80620	Shoulder Nut	1
33	80184	Eccentric - Impression Control	2
34	85206-03	Screw 6-32 x 3/16 Splined Socket	2
35	85007-06	Screw 8-32 x .375 Pan Head	2
36	85124-08	Washer #8 Helical-Lock	2
37	80181	Eccentric-Platen-Rear	2
38	80183	Platen-Impression Control	2
39	80040	Frame Asy-Platen	1
40	80186-01	Lever-Impression Control (FIN. OPS.)	1
41	80048	Frame Asy-Left Side	1
42	85207-04	Screw 8-32 x .250 Splined Socket	1
43	80185	Shaft	1
44	80187	Detent - Impression Control	1

Figure 8-4. PLATEN CARRIER ASSEMBLY

PLATEN CARRIER ASSEMBLY

ITEM	P/N	DESCRIPTION	QTY.
45	85124-06	Washer #6 Helical-Lock	2
46	85006-08	Screw 6-32 X.5 Pan Hd	2
47	85122-66	Nut 6-32 x 5/16	4
48	80142	Bail-Feed Roller	4
49	85056-10	Screw 6-32 x .312 Hex Head	4
50	85122-08	Nut 8-32	1
51	85124-08	Washer #8 Helical-Lock	1
52	80172	Screw Stud-Platen Spring	1
53	80236	Spring Extension	1
54	85056-07	Screw 6-32 x 7/16	1
55	85124-06	Washer #6 Helical-Lock	1
56	80132	Wedge	4
57	85128-37	E-Ring 5133-37	2
58	80149	Screw-Shoulder-Cam Foller	1
59	80150	Roller-Cam Foller	1
60	80036	Shaft Asy-Feed Roll Disabling	1
61	85124-06	Washer #6 Helical-Lock	1
62	85122-66	Nut 6-32	1
63	80333	Spring-Cam Follower	1
64	85006-05	Screw 6-32x .312 Pan Head	2
65	85124-06	Washer #6 Helical-Lock	2
66	80156	Eccentric-Platen Latch	2
67	85007-05	Screw 8-32 x .312 Pan Head	2
68	85124-08	Washer #8 Helical-Lock	2
69	85125-08	Washer #8 Narrow-Plain	2
70	80234	Spring	2
71	80141	Latch-Platen	2
72	80237	Spring-Extension	2
73	80041	Arm Asy Feed Roller Left-Out	1
74	80042	Arm Asy Feed Roller Left-In	1
75	80154	Shaft-Rear Feed Roller	2
76	80153	Shaft-Front Feed Roller	2
77	80044	Arm Asy-Feed Roller Right-In	1
78	80043	Arm Asy-Feed Roller Right-Out	1
79	80598	Spring Extension-Feed Roller	4
80	80040	Frame Asy-Platen	1
81	80182	Eccentric-Platen, Front	2
82	85124-08	Washer #8 Helical-Lock	2
83	85007-08	Screw 10-32 x .500 Pan Head	2
84	80707-01	Plastic Cap Charcoal Grey	2*
84A	80707-02	Plastic Cap Cordovan Brown	2*

*OPTIONAL

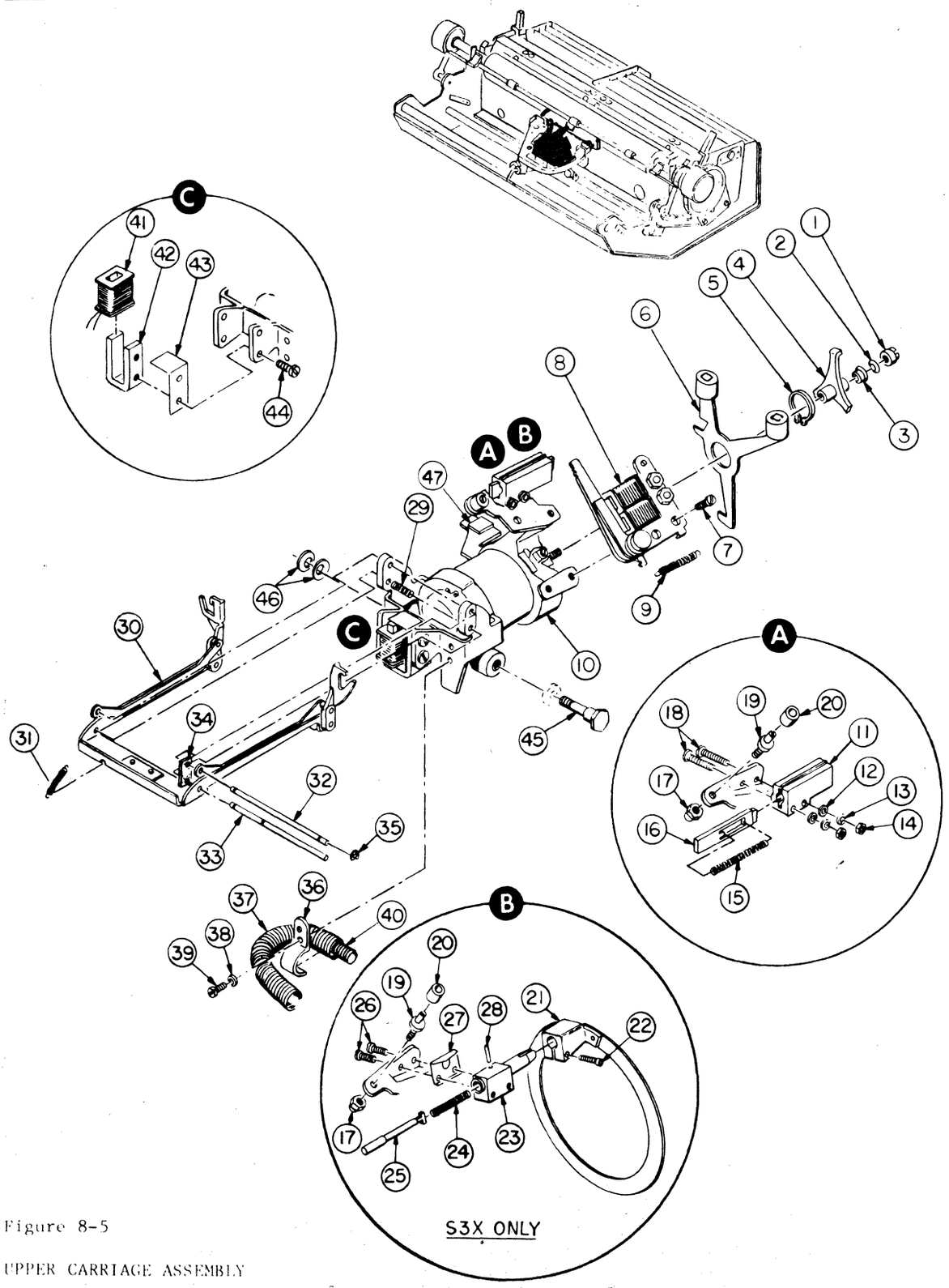


Figure 8-5

UPPER CARRIAGE ASSEMBLY

UPPER CARRIAGE ASSEMBLY

ITEM	P/N	DESCRIPTION	QTY
1	80256	Pilot-Print Wheel	1
2	85140-10	Belleville Washer AD 18.18	1
3	80407	Collet-Print Disk	1
4	80376	Hub-Printwheel Disk	1
5	85145-50	Retainer 5100-50	1
6	80375	Latch Asy-Print Motor	1
7	85004-04	Screw 4-40 X .250 Pan Head	3
8	80369-02	Armature Asy Hammer	1
9	80387	Spring Hammer Arm	1
10	80336-01	Motor/Encoder Asy Round S3-55	1
10A	80336-02	Motor/Encoder Asy Square	1
11	80687	Hammer Guide	1
12	85125-03	Flat Washer #3	2
13	85124-03	Washer #3 Helical Lock	2
14	85122-03	Nut 3-48	2
15	80713	Spring Hammer	1
16	80686	Hammer, Character	1
17	85137-05	Nut 5-40 Self Locking	2
18	85003-10	Screw 3-48	2
19	80135	Eccentric-Hammer Arm	2
20	80136	Bumper-Hammer	2
21	80729	Print Wheel Dampner S3X	1
22	85084-06	Screw S3X	1
23	80716	Hammer Guide S3X	1
24	80728	Spring S3X	1
25	85179-04	Hammer S3X	1
26	85003-05	Screw 3-48 X .312 S3X	2
27	80718	Retainer S3X	1
28	85000-01	Needle Roll .0625 X .375 S3X	1
29	80343	Spring Compression	1
30	80380	Bail Asy-Ribbon Lift	1
31	80476	Spring	1
32	80155	Shaft-Ribbon Link	1
33	80158	Shaft-Ribbon Bail	1
34	80403	Felt Pad-Ribbon Lift	2
35	85128-06	E-Ring Y5133-6	4
36	80246	Clamp Cable	1
37	80614	Spring Carriage Conductors	1
38	85124-04	Washer #4 Helical Lock	2
39	85004-04	Screw 4-40 X .250 Pan Head	2
40	80613	Spring-Inner Carriage Conductors	1
41	80379	Coil-Ribbon Lift	1
42	80147	Ribbon Magnet Core-Finished	1
43	80401	Shim-Ribbon Magnet	1
44	85004-04	Screw 4-40 X .250 Pan Head	4
45	80248	Pivot Print Motor Housing	2
46	85140-01	Belleville Washer	2
47	80374-02	Ribbon Bail Pad	1

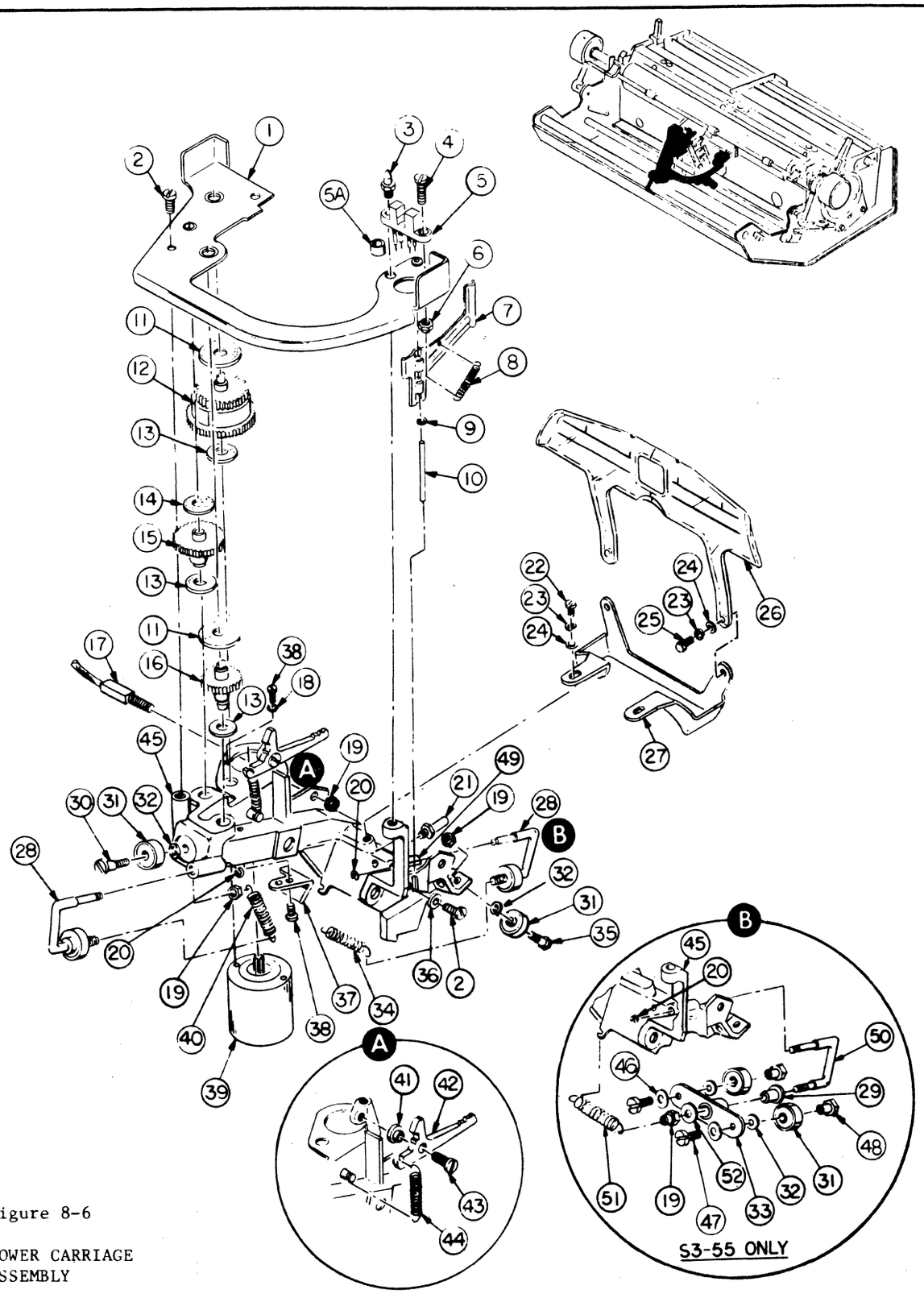


Figure 8-6

LOWER CARRIAGE ASSEMBLY

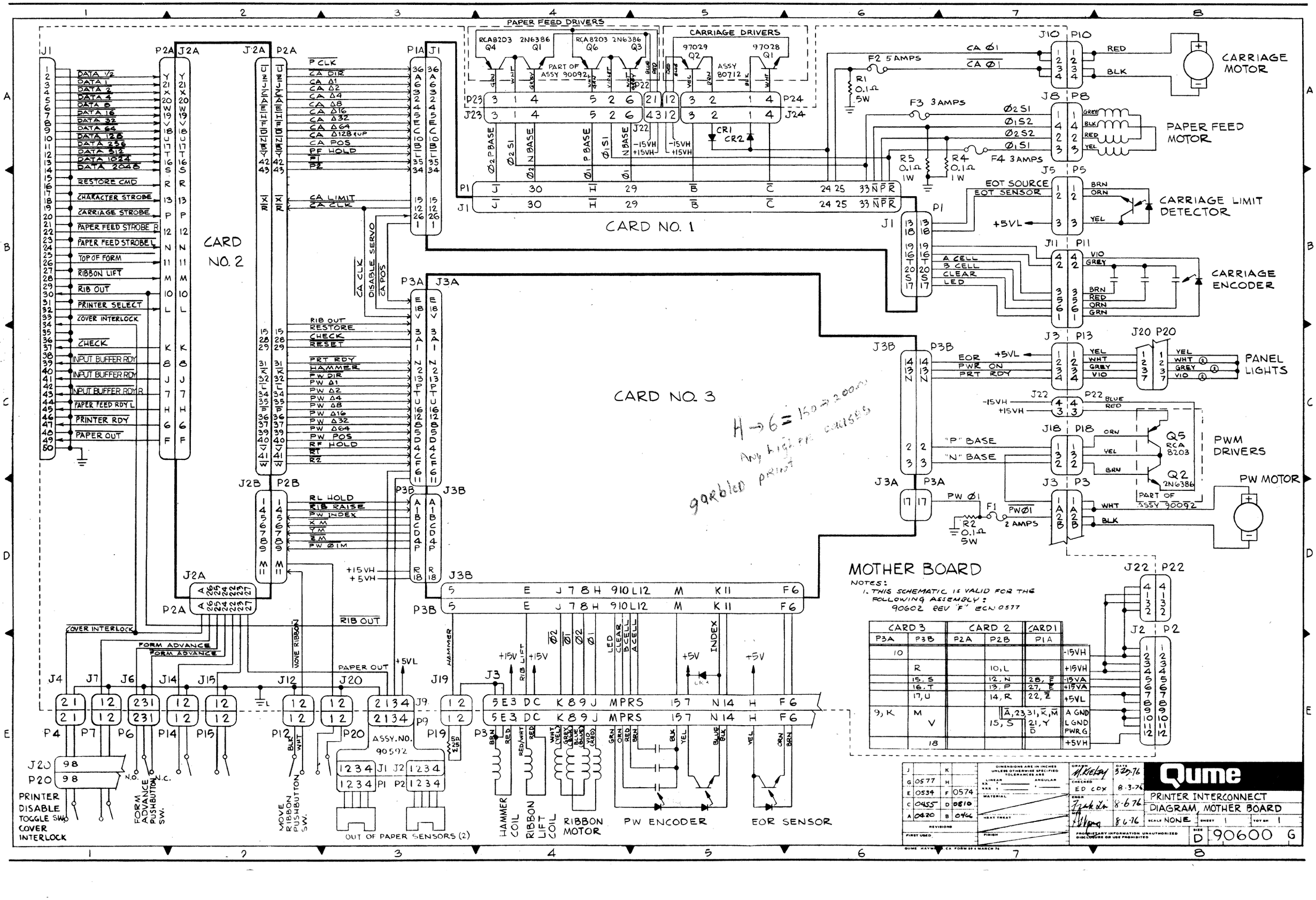
LOWER CARRIAGE ASSEMBLY

ITEM	P/N	DESCRIPTION	QTY.
1	80058	Plate Asy-Ribbon Drive	1
2	85004-04	Screw 4-40 x .250 Pan Head	2
3	80296	Screw Stud	2
4	85004-06	Screw 4-40 x .375 Pan Head	1
5	80368	Photon Module	1
5A	80465	Spacer	2
6	85137-04	Nut 4-40 Self-Locking	1
7	80315	Tension Arm Ribbon Drive	1
8	80387	Spring Ribbon Tension Arm	1
9	80386	Washer	1
10	80316	Shaft Ribbon Tension Arm	1
11	80383	Felt Washer	2
12	80057	Clutch And Magnet Asy	1
13	80385	Felt Washer	3
14	80384	Felt Washer	1
15	80218	Idler Gear-44T-Ribbon Drive	1
16	80367	Gear Asy-36 Teeth	1
17	85127	Cable Carriage Drive	2
18	85124-04	Washer #4 Helical-Lock	2
19	85137-05	Nut 5-40 Self-Locking	6
20	85138-12	Clip 5103-12	2
21	80253	Stud-Print Motor Latch	1
22	85003-04	Screw 3-48 x .250 Pan Head	2
23	85124-03	Washer #3 Helical-Lock	4
24	85125-03	Washer #3 Narrow-Plain	4
25	85053-04	Screw 3-48 x .250 Hex Head	2
26	80312	Card Guide	1
27	80357	Bracket Asy	1
28	80358	Link Asy-Guide Bearing	2
29	80657	Bushing	1
30	80104	Screw Front Guide Bearing	1
31	85144-01	Bearing	7
32	80105	Washer-Guide Roller	5
33	80655	Bearing Plate Asy	1
34	80601	Spring-Extension	1
35	80103	Screw-Guide Bearing	4
36	85125-04	Washer #4 Narrow-Plain	1
37	80406	Shutter-Photo Sensor	1
38	85004-03	Screw 4-40 x .187 Pan Head	4
39	80207	Stepper-Motor Ribbon Drive	1
40	80119	Spring-Ext Front Carriage	1
41	80217	Bearing	1
42	80219	Latch	1
43	85004-05	Screw 4-40 x .312 PAN HEAD	1
44	80304	Spring	1
45	80356	Casting	1
46	85140-10	Belleville Washer	2
47	85004-05	Screw 4-40 X .312	2
48	80114	Shoulder Nut	2
49	80374-01	Pad Print Wheel Motor	1
50	80102	Link Asy S3-55	1
51	80681	Spring S3-55	1
52	85126-05	Washer #5 S3-55	1

CHAPTER IX

SCHEMATICS AND DRAWINGS

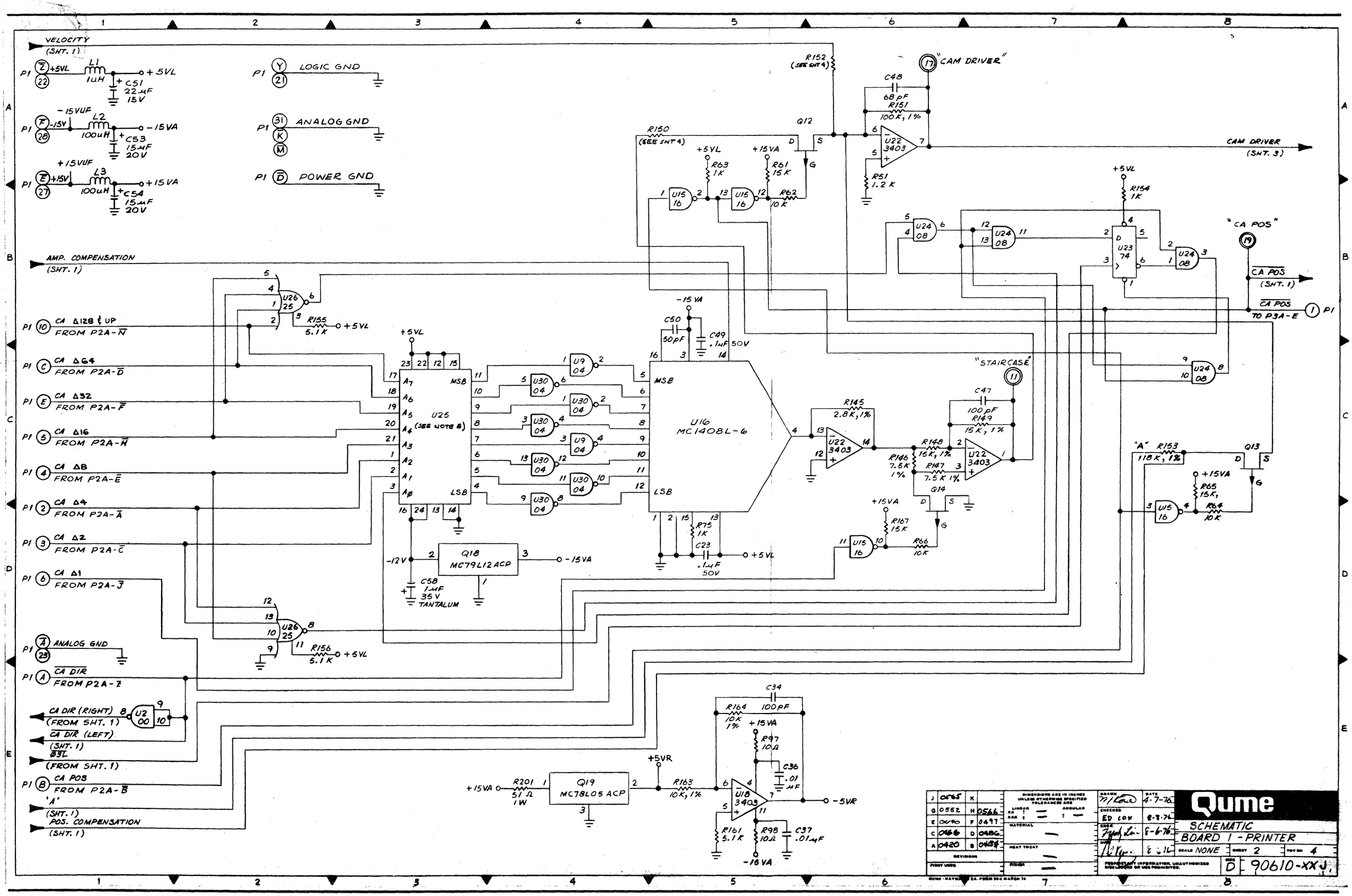
Figure 9-1 MOTHER BOARD SCHEMATIC



CARD 3		CARD 2		CARD 1	
P3A	P3B	P2A	P2B	P1A	
10					-15VH
	R		10, L		+15VH
	15, S		12, N	28, E	-15VA
	16, T		13, P	27, E	+15VA
	17, U		14, R	22, Z	+5VL
9, K	M		Ā, 23, 31, K̄, M̄		A GND
	V		15, S	21, Y D	L GND
					PWR G
	18				+5VH

Figure 9-2 PC BOARD #1 SCHEMATIC (1 OF 4)

Figure 9-3 PC BOARD #1 SCHEMATIC (2 OF 4)



J	0565	K					
G	0552	H	0566				
E	0490	F	0497				
C	0466	D	0486				
A	0420	B	0458				

REVISIONS

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE LINEAR ANGULAR .XX ± .XXX ±

MATERIAL

HEAT TREAT

FINISH

PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

DRAWN TJ Love 4-7-76

CHECKED ED LOW 8-8-76

ENGR. Tyrrell Lin 8-6-76

MFG. 8-16

Qume

SCHEMATIC

BOARD 1 - PRINTER

SCALE NONE SHEET 2 TOT SH 4

SIZE D 90610-XXJ

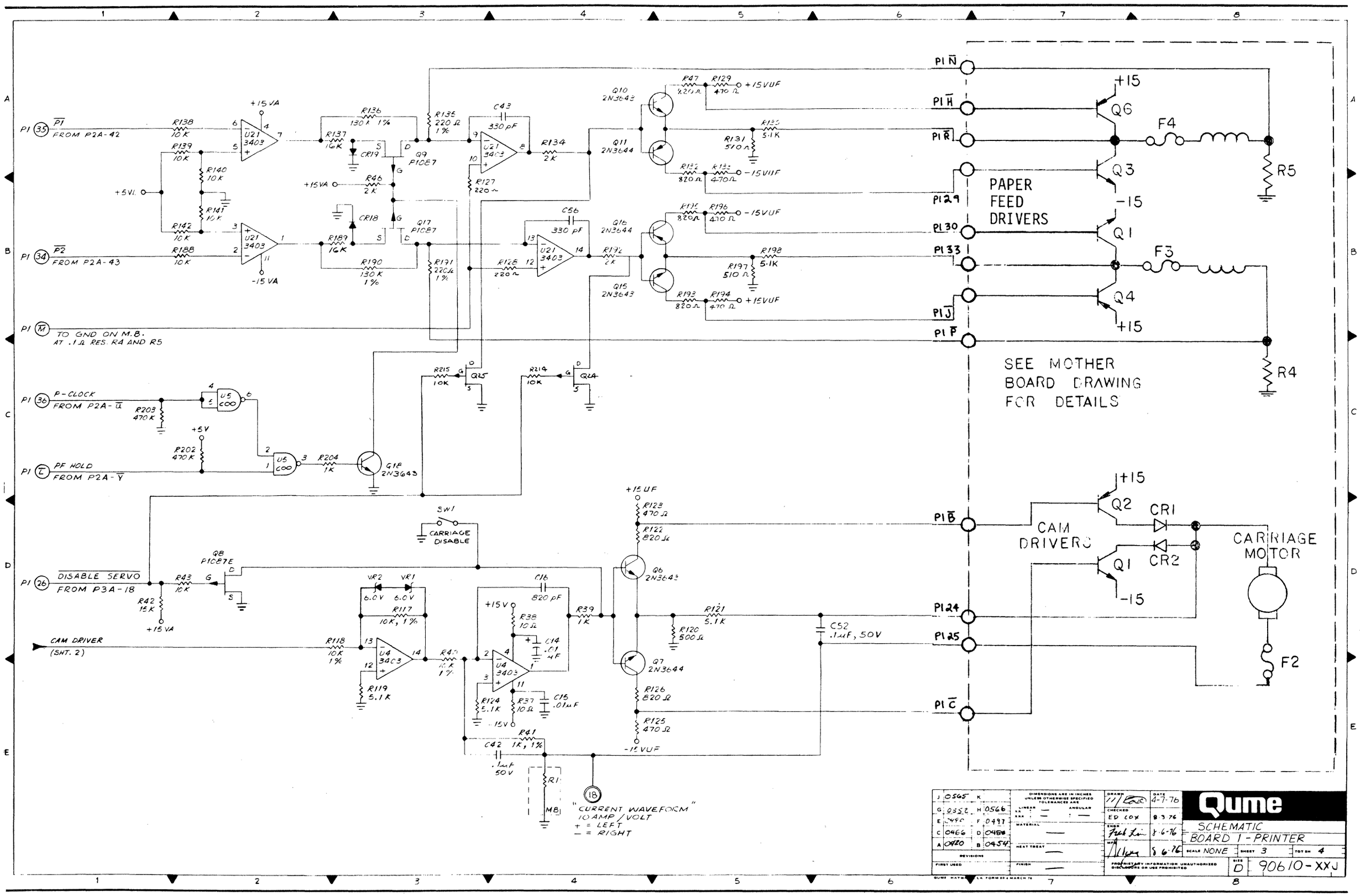
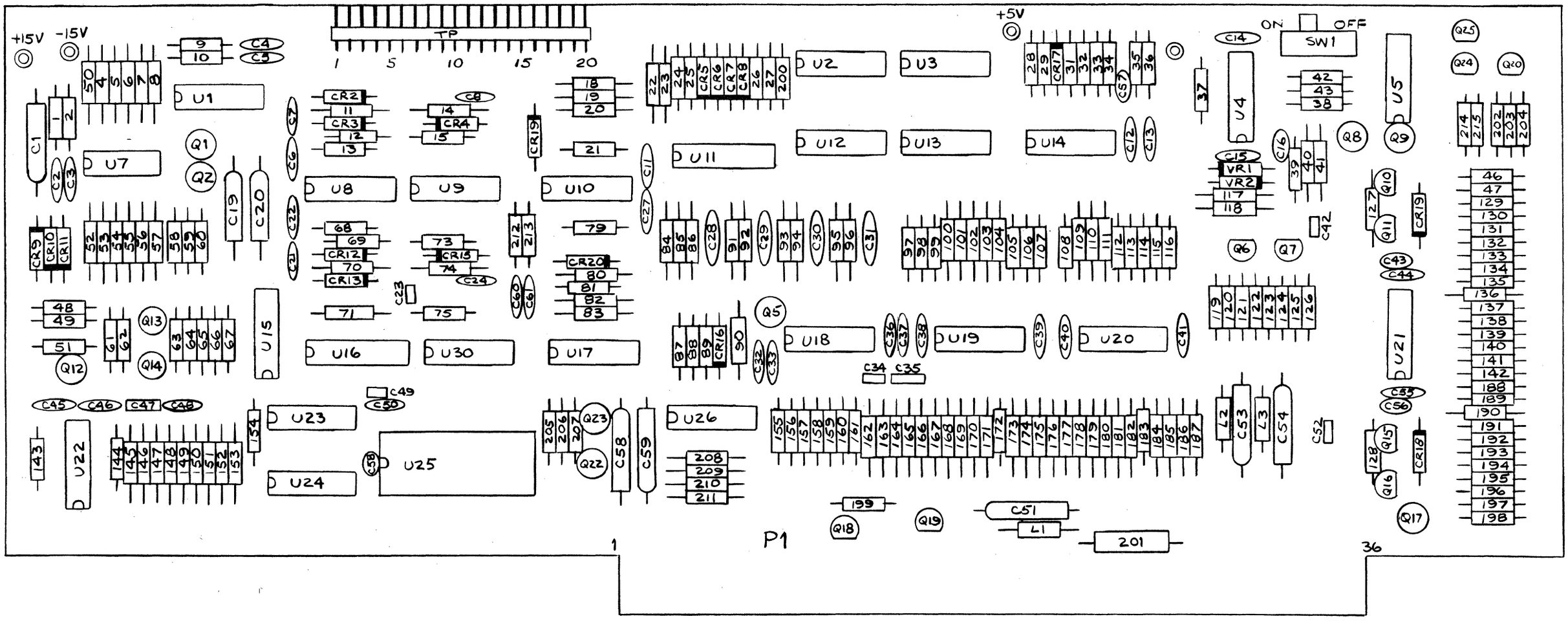


Figure 9-4 PC BOARD #1 SCHEMATIC (3 OF 4)

Figure 9-5 PC BOARD #1 ASSEMBLY DRAWING (4 OF 4)



RESISTOR CHART				
RESISTOR	53/35-00	53/45-01	53/55-02	WT40-05
R150	4.12K, 1%	4.12K, 1%	4.32K, 1%	4.32K, 1%
R152	1.33K, 1%	1.74K, 1%	1.65K, 1%	1.22K, 1%

NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL .01μF CAPACITORS ARE 25V
2. ALL RESISTORS ARE 5% 1/4W
3. ALL 1% RESISTORS ARE 1/8W
4. ALL DIODES ARE IN4154
5. ALL GROUNDS ARE ANALOG
6. ALL FETS ARE P1087E
7. THIS SCHEMATIC IS VALID FOR THE FOLLOWING ASSEMBLY:
   - 53/35 - 00 "J" ECN 0565
   - 53/45 - 01 "J" ECN 0565
   - 53/55 - 02 "J" ECN 0565
   - WT40 - 05 "J" ECN 0565
8. U25 ROM USE 95819 FOR 53/35(90612-00), 53/45 (90612-01) & WT-40 (90612-05). FOR 53/55 (90612-02) USE 95818

J	0565	K		DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE	DRAWN F.NABONNE 7-19-76
G	0552	H		LINEAR XX ± — XXX ± — ANGULAR : —	CHECKED ED COX 8-3-76
E	0490	F	0497	MATERIAL —	ENGR Frank Lin 8-6-76
C	0466	D	0486	HEAT TREAT —	MFG 8-6-76
A	0420	B	0454	FINISH —	
REVISIONS					
FIRST USED					

PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

QUME HAYWARD, CA FORM 80-4 MARCH 74

Qume

SCHEMATIC
BOARD 1 - PRINTER

SCALE NONE | SHEET 4 | TOT SH 4

SIZE D | 90610-XXJ

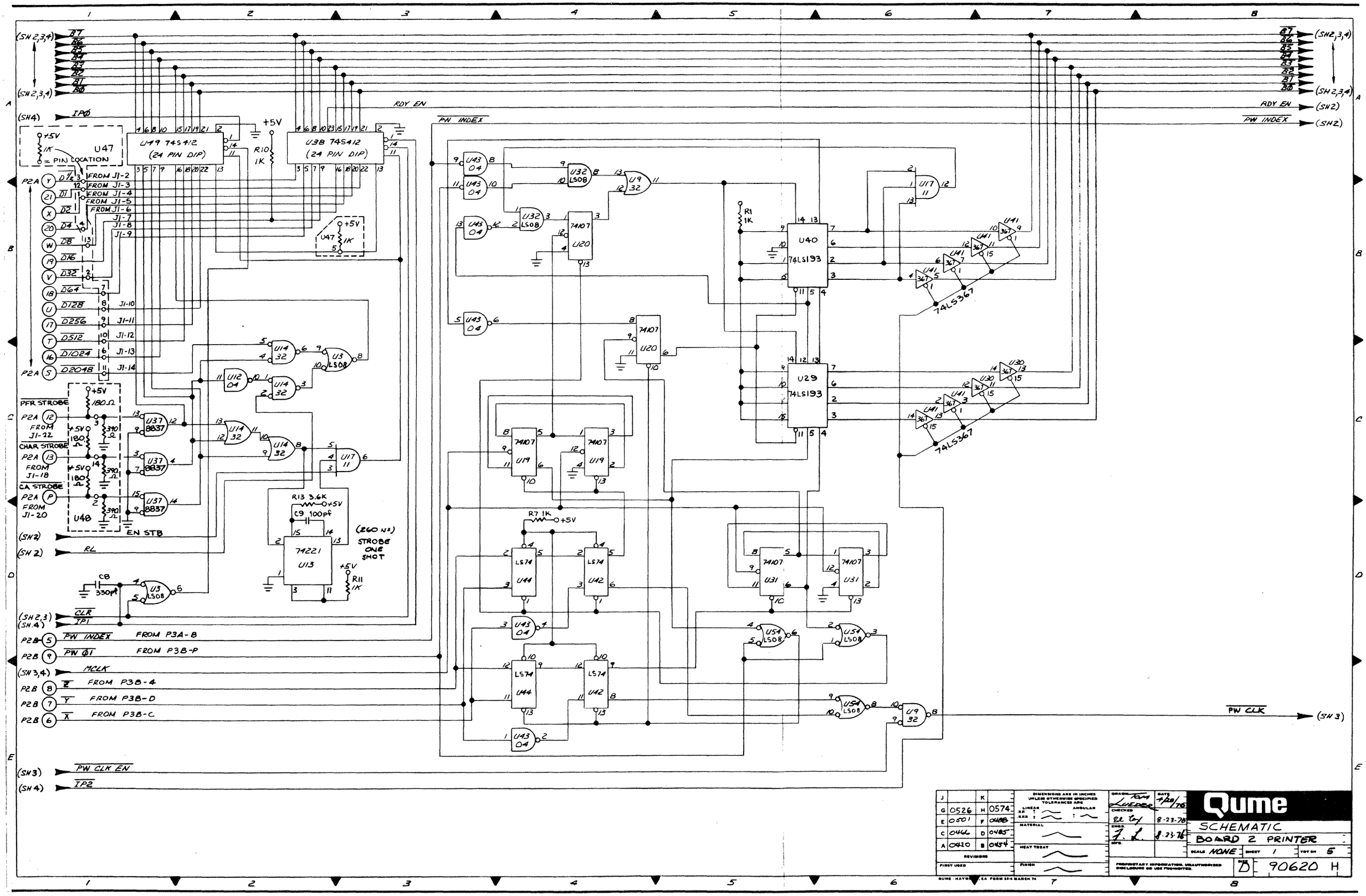
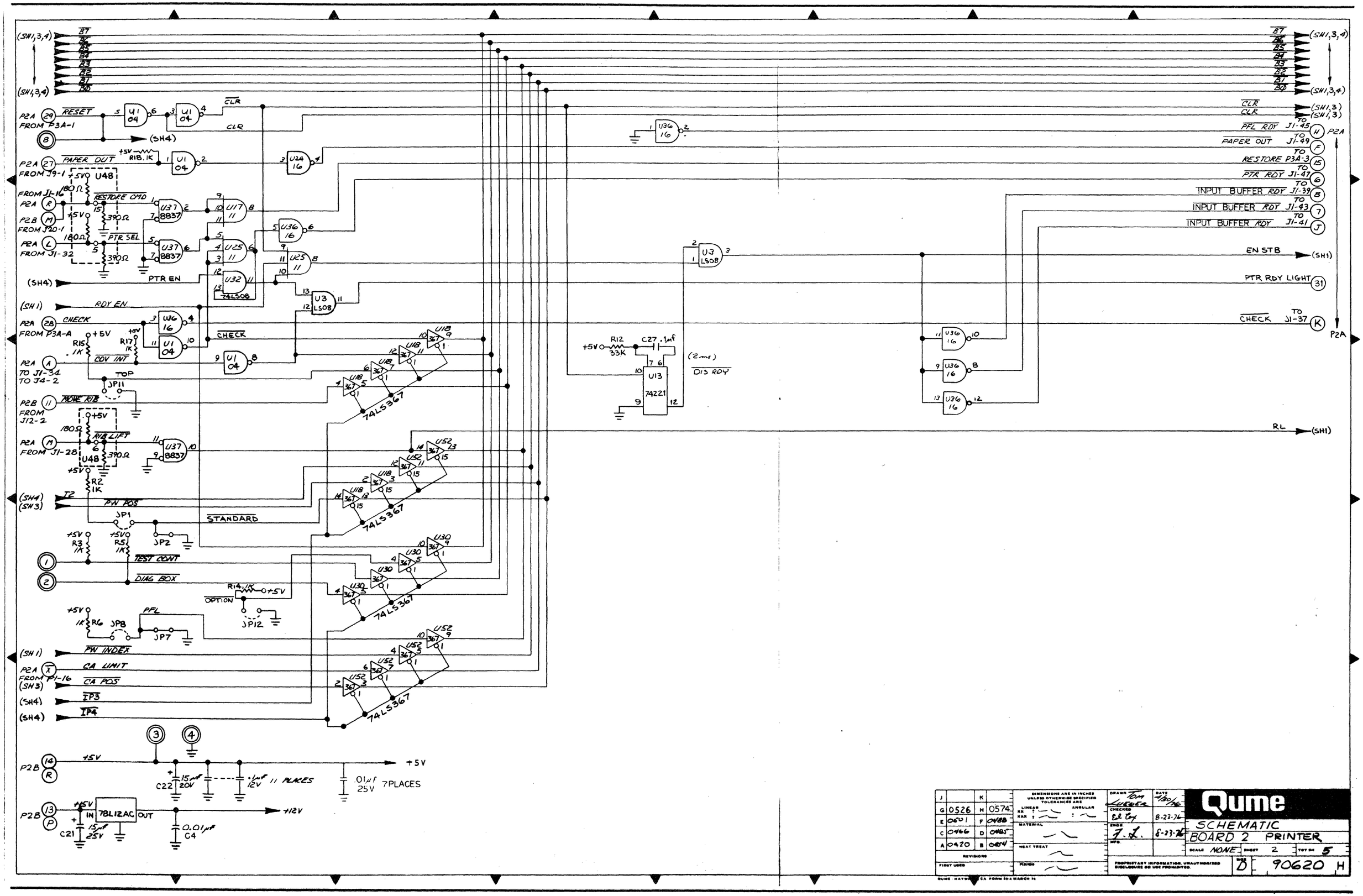


Figure 9-6 PC BOARD #2 SCHEMATIC (1 OF 5)

Figure 9-7 PC BOARD #2 SCHEMATIC (2 OF 5)



J		K	
G	0526	H	0574
E	0601	F	0488
C	0466	D	0485
A	0420	B	0484

REVISIONS
FIRST USED

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE
LINEAR .XX ± .X ± ANGULAR .XXX ±
MATERIAL
HEAT TREAT
FINISH

DRAWN Tom Lucas DATE 7/30/76
CHECKED E.E. Cy 8-23-76
ENGR J. L. 8-23-76
MFG

PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

Qume
SCHEMATIC
BOARD 2 PRINTER
SCALE NONE SHEET 2 TOT SH 5
SIZE D 90620 H

QUME - HAYWARD, CA FORM 50-4 MARCH 74

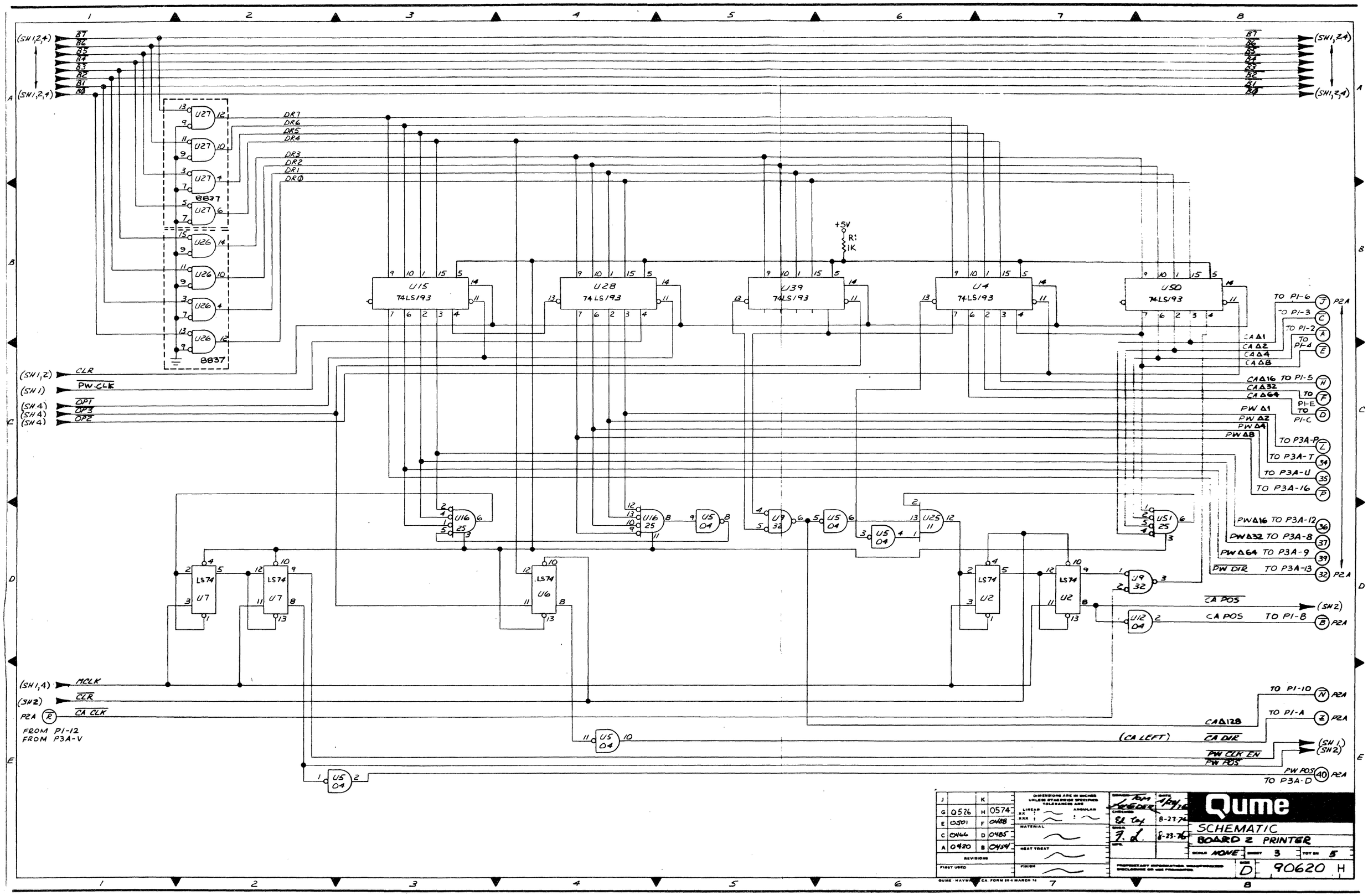
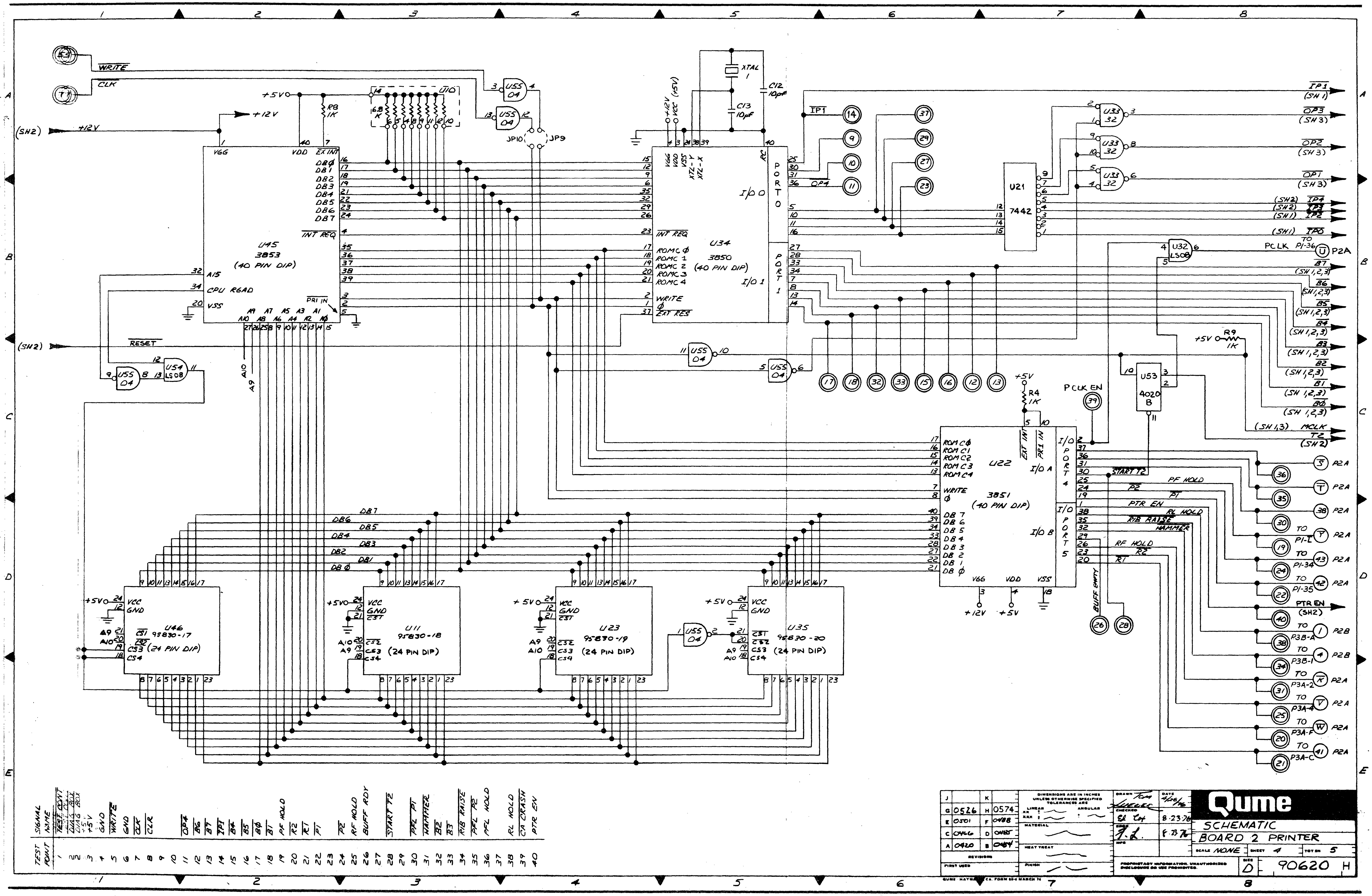
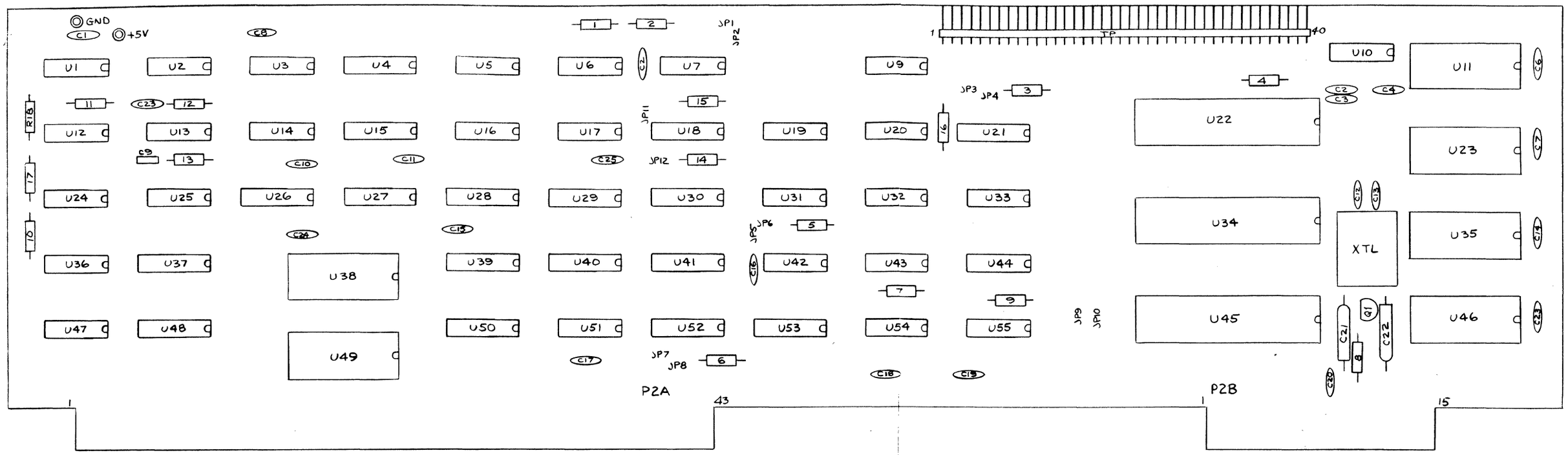


Figure 9-8 PC BOARD #2 SCHEMATIC (3 OF 5)

Figure 9-9 PC BOARD #2 SCHEMATIC (4 OF 5)





NOTES &

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTOR ARE 1/4W 5%.
2. ALL DIODES ARE IN4154.
3. ALL FILTER CAPS. .1μF, 12V.
4. THIS SCHEMATIC IS VALID FOR FOLLOWING ASSEMBLY
   REV "G" ECN 0526

J		K	
G	0526	H	0574
E	0501	F	0488
C	0466	D	0465
A	0420	B	0454

REVISIONS

FIRST USED

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE
LINEAR XX ± — XXX ± — ANGULAR ± —

MATERIAL —

HEAT TREAT —

FINISH

DRAWN	F. NABONNE	DATE 7-19-76
CHECKED		7-21-76
ENGR	J. L	8-23-76
MFG		

Qume

SCHEMATIC
BOARD 2 PRINTER

SCALE NONE | SHEET 5 | TOT SH 5

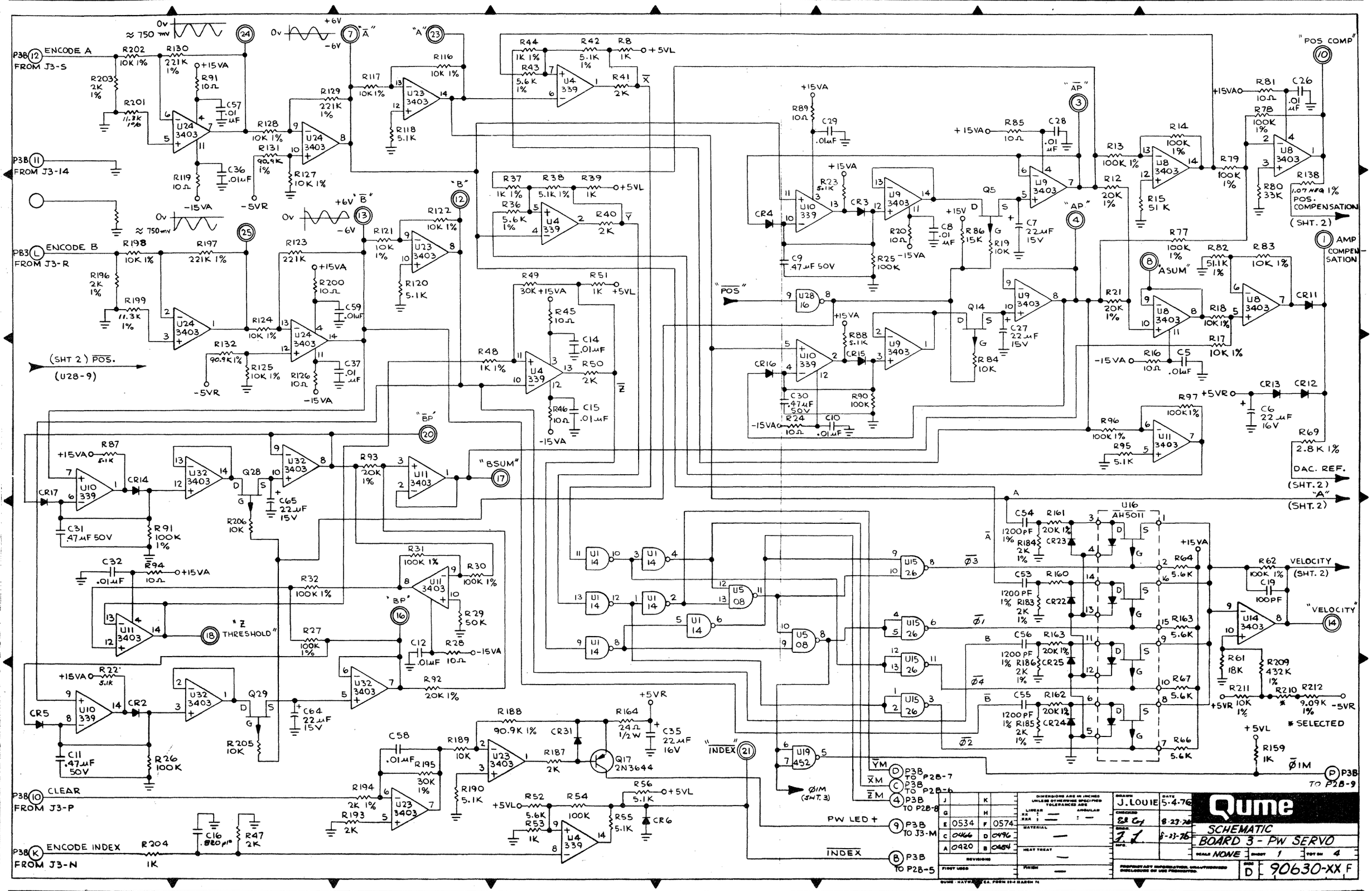
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SIZE D 90620 H

QUME HAYWARD, CA FORM 80-4 MARCH 74

Figure 9-10 PC BOARD #2 ASSEMBLY DRAWING (5 OF 5)

Figure 9-11 PC BOARD #3 SCHEMATIC (1 OF 4)



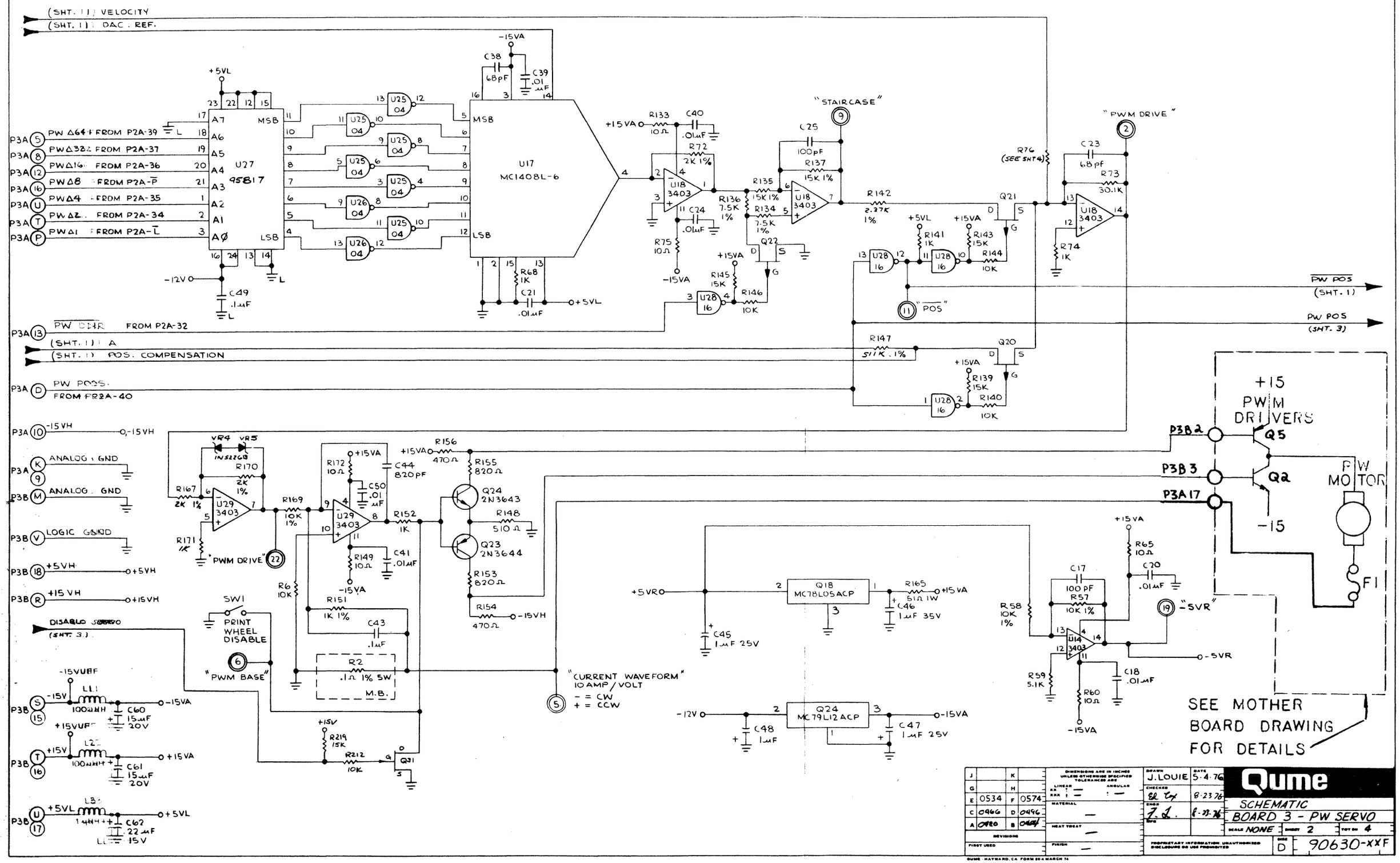
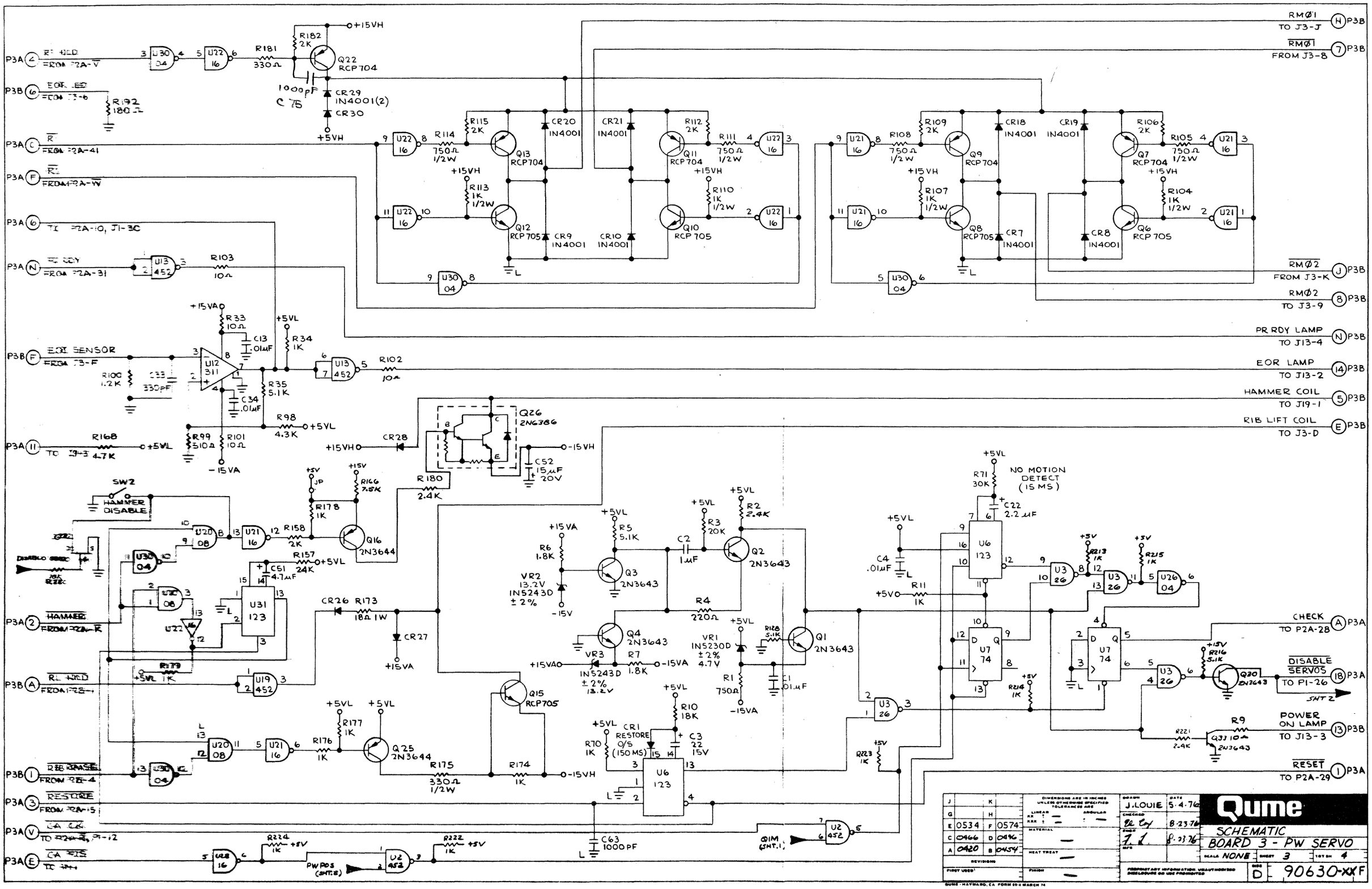
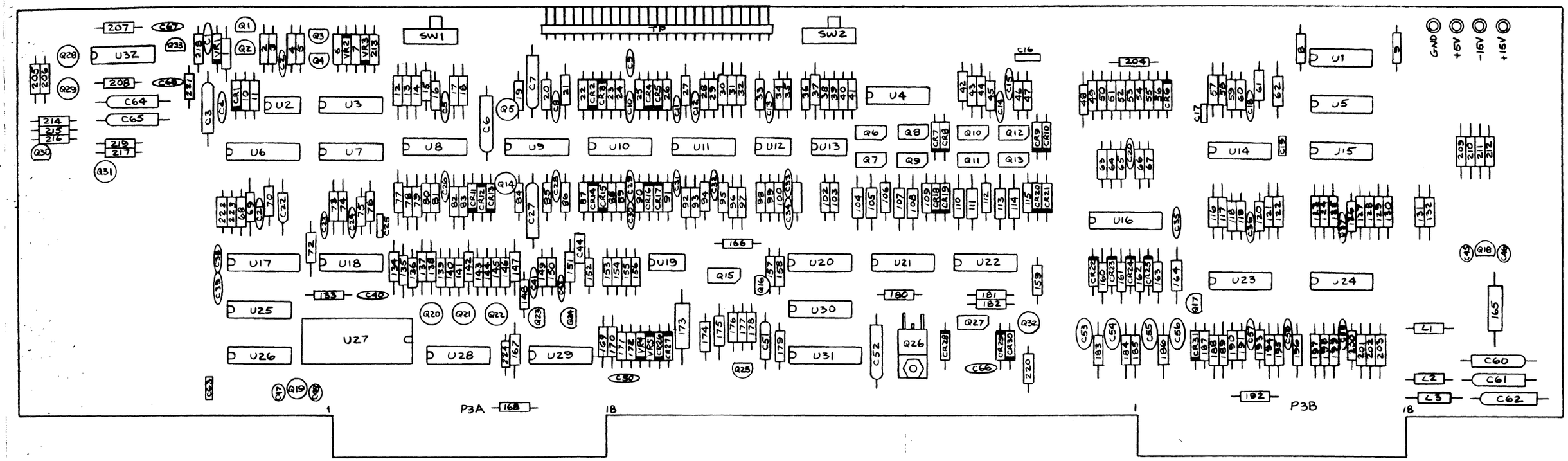


Figure 9-12 PC BOARD #3 SCHEMATIC (2 OF 4)

Figure 3-13 PC BOARD #3 SCHEMATIC (3 OF 4)





RESISTOR CHART	
UNIT	RESISTOR
53/35 -00	R76, 1.30K, 1%
53/45 -01	R76, 1.40K, 1%
53/55 -02	R76, 1.58K, 1%
53/X30 -03	R76 —
53/X40 -04	R76 —
WT40 -02	R76, 1.58K, 1%

MODIFICATIONS :
CUT TRACE FROM L1 TO Q26 EMITTER ADD JUMPER FROM P3A-10 TO R154 TOP SIDE OF BOARD.

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR IN OHM'S, 1/4W, 5%.
2. ALL DIODES ARE IN4154.
3. ALL .01μF CAPACITORS ARE 25V.
4. ALL 1% RESISTORS ARE 1/8W.
5. ALL GROUNDS ARE ANALOG.
6. ALL FETS ARE DI087E.

7. THIS SCHEMATIC IS VALID FOR THE FOLLOWING ASSEMBLYS.
53/35 -00 "E" ECN 0496
53/45 -01 "E" ECN 0496
53/55 -02 "E" ECN 0496
53/X30 -03
53/X40 -04
WT 40 -02 "E" ECN 0496

J		K	
G		H	
E	0534	F	0574
C	0466	D	0496
A	0420	B	0454
REVISIONS			
FIRST USED			

DIMENSIONS ARE IN INCHES
UNLESS OTHERWISE SPECIFIED
TOLERANCES ARE
LINEAR XX ± — XXX ± — ANGULAR ± —
MATERIAL —
HEAT TREAT —
FINISH —

DRAWN F. NABONNE 7-19-76
CHECKED Ed Coy 8-25-76
ENGR. 8-23-76
MFG.

PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

Qume
SCHEMATIC
BOARD 3 - PW SERVO
SCALE NONE SHEET 4 TOT SH 4
SIZE D 90630-XX F

QUME - HAYWARD, CA. FORM 80-4 MARCH 74

Figure 9-14 PC BOARD #3 ASSEMBLY DRAWING (4 OF 4)

AES keyboard

A6-937-0001XX

KEYBOARD SPECIFICATION

MANUFACTURER: HONEYWELL LTD.,
740 ELLESMERE ROAD,
SCARBOROUGH, ONTARIO.

OPTIONS:
TAB-01	"66 Key Version"	(KB66SD - 12 - 4 - C)
TAB-02	"70 Key Version"	(KB70SD - 12 - 4 - C)
TAB-03	"71 Key Version"	
TAB-04	"75 Key Version"	

This specification describes two basic keyboards referred to as the 66 key and the 70 key (KB66SD12-4-C & KB70SD12-4-C)versions. The two keyboards shall,be constructed using identical PCB's and keyboard encoders and shall differ only in minor assembly details, mounting plate and inthe number and placement of key modules. Tabs 03 & 04 define identical keyboards to Tabs 01 & 02, respectively, with the addition of 5 optional keys. These keyboards are referred to as 71 & 75 key versions, respectively.

All active keys shall be of the solid state "HALL-EFFECT" type, utilizing low-profile switch elements.

TERMINATION

All electrical interconnect signals shall be terminated in a standard, male, 20 conductor, flat cable header (Ref.3M#3428-1002). This header shall be oriented such that cable take-off is at right angles to the plane of the PCB.
The pin assignment shall be as defined in TABLE 1.

KEYBOARD FEATURES

1. Secretary Shift Lock: An electrical shift lock shall be provided such that a LED indicator adjacent to the shift lock key shall indicate when the "LOCK" key has been depressed. Release of the shift lock shall be accomplished immediately upon depressing either one of the two "SHIFT" keys. Either "SHIFT" or "LOCK" will place the keyboard in Mode 2 of encoding. The LED indicator mounting shall be black.

2. N-Key Roll-Over: The sequential depressing of any number of encoded keys will produce corresponding output, codes and strobes, irrespective of whether or not any other encoded key is depressed concurrently.

Where this requirement conflicts with the timed repeat function, the strobe line response shall correspond to the timed repeat requirements, and the data code at the time of the transition to the repeat strobe must represent the code of the last depressed key.

3. Styling: The keyboard construction shall be compatible with the use of stepped, sculptured keytops in the typewriter section and standard truncated keytops in the control pad area. The keyboard mounting angle will be 7°. Keys shall be spaced at .75 inches with standard offsets on each row.

4. Parity: The keyboard encoding shall incorporate odd parity.

5. Plunger Locations: The active plunger locations shall correspond to the key numbers except for keys 43,63,75 and 81 as indicated in Figs.2 & 3.

6. Support Locations: Some inactive key positions shall be reserved for support function for large keys. A support module comprises a non-encoded plunger with the plunger length reduced by the insertion depth of about .2 inch. Thus the following positions require support modules;

TAB 01	TAB 02
3	36
36	76 (see Fig.3)
64	
76	

Alternately, the support plungers may be deleted if, in the opinion of AES,the supplier's plunger design is adequate to support large keys without undue bending, warping or sticking.

7. Space Bar Mounting: The supplier shall provide the necessary hardware to adapt the AES space bar to his mounting requirements.

The AES space bar is detailed in Figs. 4 & 5. The guides are inserted by AES (or AES's subcontrator) and the supplier shall specify and provide alternate guides and cross links to adapt this space bar to his mounting requirements.

Alternately, the supplier may provide the complete mounted space bar under separate contract. This provision is conditional upon the supplier's guarantee to match the colour and texture of the AES keytops.

8. Timed Repeat: Keys 16,36,55 (Tabs 01 & 03), 56 (Tabs 02 & 04), 58,60, 79 & 81 shall generate a repeating strobe pulse if depressed for 330 mS or longer. The repeat frequency shall be 30 cps.

9. Timing: The repeat delay and repeat frequency shall be alternable by single component changes.

MOUNTING

A standard mounting flange shall be provided for mounting the keyboard 0.620 inches below the top of the enclosure panel. Details of the mounting, P.C.B. area, and header location are contained in Fig. 1, Figs. 2 & 3 reference the key modules to the mounting flange position. The P.C.B. width shall not exceed 15.55 inches.

CONFIGURATION

Two configurations will be required as detailed in the Figs 2&3. Tabs 01 and 03 will not incorporate encoded keys at positions 3, 35, 36, 56 & 64.

Keys 1,21,41,61,&89 are encoded on all keyboards but equipped only on Tabs 03 and 04.

ENVIRONMENTAL REQUIREMENTS

Temperature: The keyboard shall meet all specifications between 0 C. & 55 C.

CODING SEE TABLE II

KEYTOPS

The space bar mounting hardware shall be provided by the keyboard supplier.
Associated keytop sets are specified in the following AES drawings:

NOTE: For keytop set Dwgs, AS SHOWN BELOW. Tab .01 refers to North American Grey buttons. Tab.02 refers to European Beige buttons.

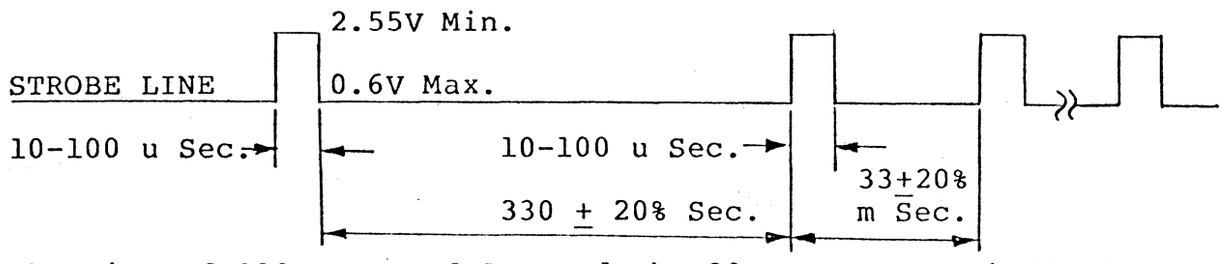
A6-938-0001XX	DENMARK (66 KEY)	A6-938-0010XX	FRENCH-CANADA(66)
A6-938-0002XX	FRANCE "	A6-938-0011XX	GERMANY (70Key)
A6-938-0003XX	GERMANY "	A6-938-0012XX	N.A. ENGLISH (66)
A6-938-0004XX	NETHERLANDS "	A6-938-0013XX	FINLAND (70Key)
A6-938-0005XX	ITALY "	A6-938-0014XX	NORWAY (66)
A6-938-0006XX	SWEDEN-FINLAND "	A6-938-0015XX	BILINGUAL CAN(66)
A6-938-0007XX	SWISS-GERMAN "	A6-938-0016XX	SWEDEN (70 Key)
A6-938-0008XX	SWISS-FRENCH "	A6-938-0017XX	Norway (70 Key)
A6-938-0009XX	UNITED-KINGDOM "	A6-938-0021XX	Symbolic N.A.E.(66)
A6-938-0026XX	SWISS GERMAN (70KEY)	A6-938-0027XX	SWISS-FRENCH (70)

TABLE 1

INTERFACE CONNECTOR

PIN	SIGNAL NAME	SIGNAL TRUE	CHARACTERISTICS FALSE
11	DATA BIT 1	+ 2.55V Min. at .12mA Source	+ 0.6V. Max. at 1.6mA Sink
13	DATA BIT 2	"	"
19	DATA BIT 3	"	"
20	DATA BIT 4	"	"
5	DATA BIT 5	"	"
7	DATA BIT 6	"	"
18	DATA BIT 7	"	"
9	PARITY BIT	"	"
8	REPEAT	.04V Max. at 4MA Sink	OPEN or 2.55V Min.
6	CODE	"	"
10	NOT USED	-	-
12	NOT USED	-	-
16	STROBE (SEE NOTE 1)	+2.55V Min. at .12mA Source	+0.6V Max. at 1.6mA Sink
1	+5V	1.5 AMP. Max.	
3	+5V		
2,15	GND.		
4,17	GND.		
14	-12V	0.5AMP. Max.	

NOTE 1: For all keys except function keys (shift, repeat, and code) the strobe shall produce a TRUE pulse output of between 10 and 100 micro seconds duration. For keys designated with the timed repeat, the strobe line shall, in addition to the above requirements, produce a repeating TRUE pulse delayed 330 milli seconds from the initial strobe pulse. This continuous TRUE level of the strobe output shall last for the duration of the time that the key is depressed.



The time of 330 m Sec. delay and the 30 Hz repeat shall be adjusted by the manufacturer within 20%.

TABLE II TAB 01 (KB66SD12-4-C) TAB 03

KEY No	KEYBOARD CODE UNSHIFTED 7654321	SHIFTED 7654321	NOTE	KEY No	UNSHIFTED 7654321	SHIFTED 7654321	NOTE
1	0011100	0011100	opt.	44	1100001	1000001	
3	NOT ACTIVE			45	1110011	1010011	
4	0110001	0100001		46	1100100	1000100	
5	0110010	1000000		47	1100110	1000110	
6	0110011	0100011		48	1100111	1000111	
7	0110100	0100100		49	1101000	1001000	
8	0110101	0100101		50	1101010	1001010	
9	0110110	1011110		51	1101011	1001011	
10	0110111	0100110		52	1101100	1001100	
11	0111000	0101010		53	0111011	0111010	
12	0111001	0101000		54	0100111	0100010	
13	0110000	0101001		55	0001101	0001101	!
14	0101101	1011111		58	0011000	0011000	!
15	0111101	0101011		59	0010111	0010111	
16	0001000	0001000	!	60	0000100	0000100	!
18	0011011	0011011		61	0011111	0011111	opt
19	0000101	0000101		63	SHIFT FUNCTION		
20	REPEAT FUNCTION			64	NOT ACTIVE		
21	0011101	0011101	opt	65	1111010	1011010	
23	0001001	0001001		66	1111000	1011000	
24	1110001	1010001		67	1100011	1000011	
25	1110111	1010111		68	1110110	1010110	
26	1100101	1000101		69	1100010	1000010	
27	1110010	1010010		70	1101110	1001110	
28	1110100	1010100		71	1101101	1001101	
29	1111001	1011001		72	0101100	0111100	
30	1110101	1010101		73	0101110	0111110	
31	1101001	1001001		74	0101111	0111111	
32	1101111	1001111		75	SHIFT FUNCTION		
33	1110000	1010000		76	NOT USED		
34	1011011	1011101		78	0000010	0000010	
35	NOT ACTIVE			79	0000000	0000000	!
36				80	CODE FUNCTION		
38	0000001	0000001		81	0100000	0100000	!
39	0010000	0010000	!	89	0001011	0001011	Opt
40	0000011	0000011		98	0011001	0011001	
41	0011110	0011110	opt	99	0011010	0011010	
43	SHIFT LOCK			100	0001100	0001100	

opt-Keys marked opt are encoded but only equipped on Tab 03
!-These keys incorporate the timed repeat functions.

TABLE II TAB 02 (KB70SD12-4-C) & TAB 04

KEY No	KEYBOARD CODE UNSHIFTED 7654321	SHIFTED 7654321	NOTE	KEY No	UNSHIFTED 7654321	SHIFTED 7654321	NOTE
1	0011100	0011100	opt.	44	1100001	1000001	
3	0000110	0010101		45	1110011	1010011	
4	0110001	0100001		46	1100100	1000100	
5	0110010	1000000		47	1100110	1000110	
6	0110011	0100011		48	1100111	1000111	
7	0110100	0100100		49	1101000	1001000	
8	0110101	0100101		50	1101010	1001010	
9	0110110	1011110		51	1101011	1001011	
10	0110111	0100110		52	1101100	1001100	
11	0111000	0101010		53	0111011	0111010	
12	0111001	0101000		54	0100111	0100010	
13	0110000	0101001		55	0001101	0001101	
14	0101101	1011111		56	0001101	0001101	!
				58	0011000	0011000	
15	0111101	0101011		59	0010111	0010111	
16	0001000	0001000	!	60	0000100	0000100	!
18	0011011	0011011		61	0011111	0011111	opt
19	0000101	0000101		63	SHIFT FUNCTION		
20	REPEAT FUNCTION			64	0001110	0001111	
21	0011101	0011101	opt	65	1111010	1011010	
23	0001001	0001001		66	1111000	1011000	
24	1110001	1010001		67	1100011	1000011	
25	1110111	1010111		68	1110110	1010110	
26	1100101	1000101		69	1100010	1000010	
27	1110010	1010010		70	1101110	1001110	
28	1110100	1010100		71	1101101	1001101	
29	1111001	1011001		72	0101100	0111100	
30	1110101	1010101		73	0101110	0111110	
31	1101001	1001001		74	0101111	0111111	
32	1101111	1001111		75	SHIFT FUNCTION		
33	1110000	1010000		76	NOT USED		
34	1011011	1011101		78	0000010	0000010	
35	0010001	0010010		79	0000000	0000000	!
36				80	CODE FUNCTION		
38	0000001	0000001		81	0100000	0100000	!
39	0010000	0010000	!	89	0001011	0001011	Opt
40	0000011	0000011		98	0011001	0011001	
41	0011110	0011110	opt	99	0011010	0011010	
43	SHIFT LOCK			100	0001100	0001100	

opt-Keys marked opt are encoded but only equipped on Tab 04
!-These keys incorporate the timed repeat functions.

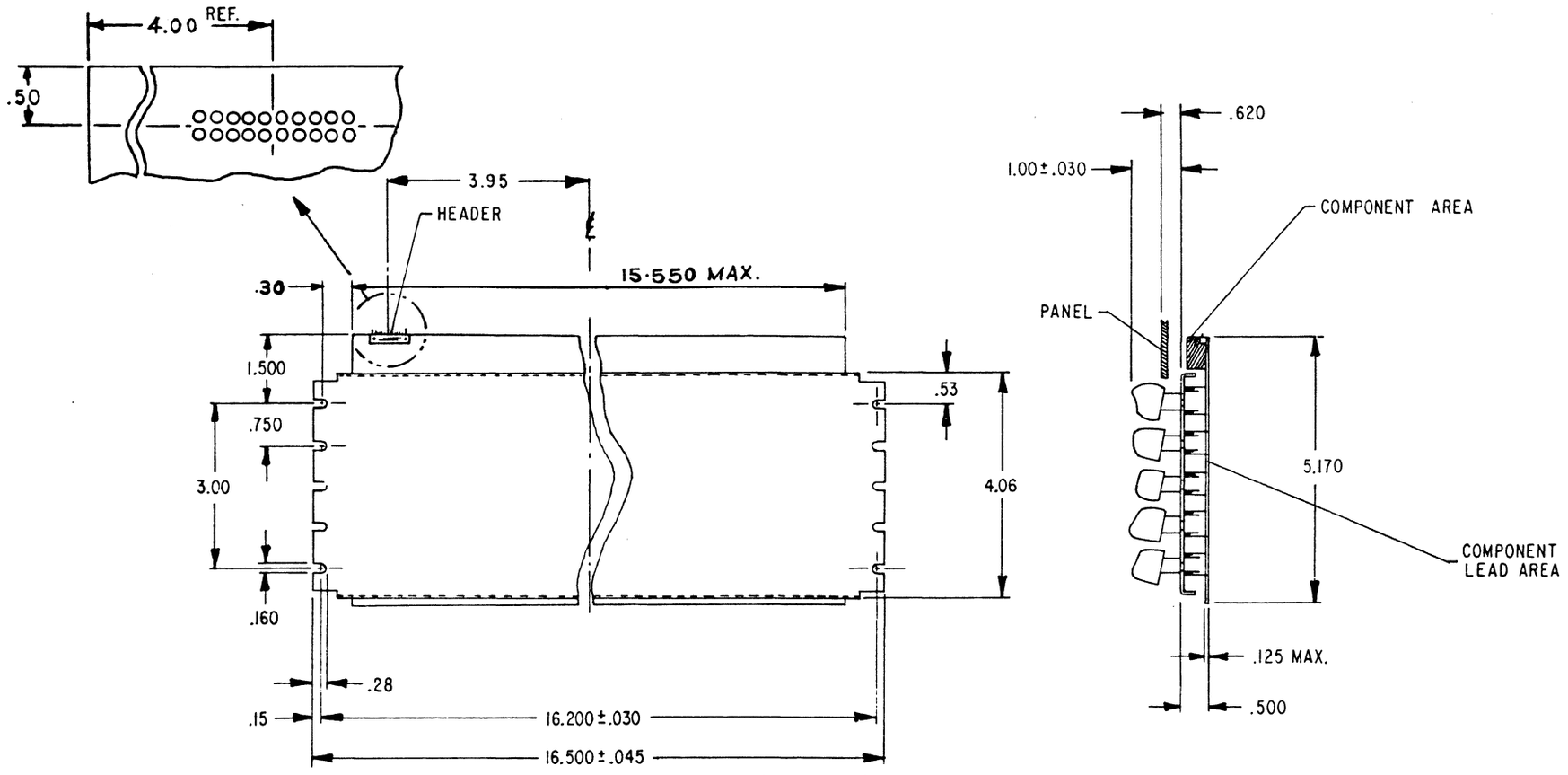
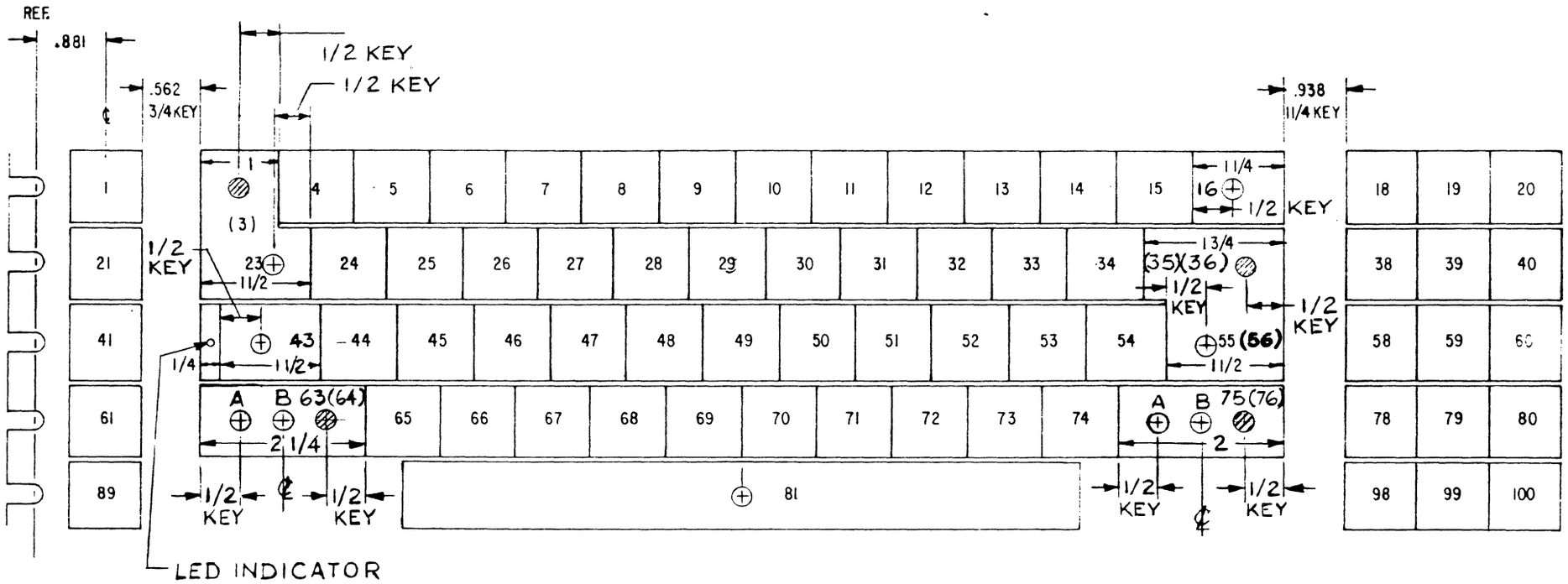


FIGURE 1 - KEYBOARD MOUNTING



NOTE: KEYS 63 AND 75 USE PLUNGER LOCATIONS A FOR MICROSWITCH SD SERIES OR EQUIVALENT PLUNGERS. ALL OTHERS USE LOCATION B.

POSITIONS 3, 35, 36, & 64 ARE NOT USED AS ACTIVE KEYS

⊕ - PLUNGER LOCATIONS

▨ - SUPPORT PLUNGER

FIGURE-2 CONFIGURATION 1 66 KEY & 71 KEY

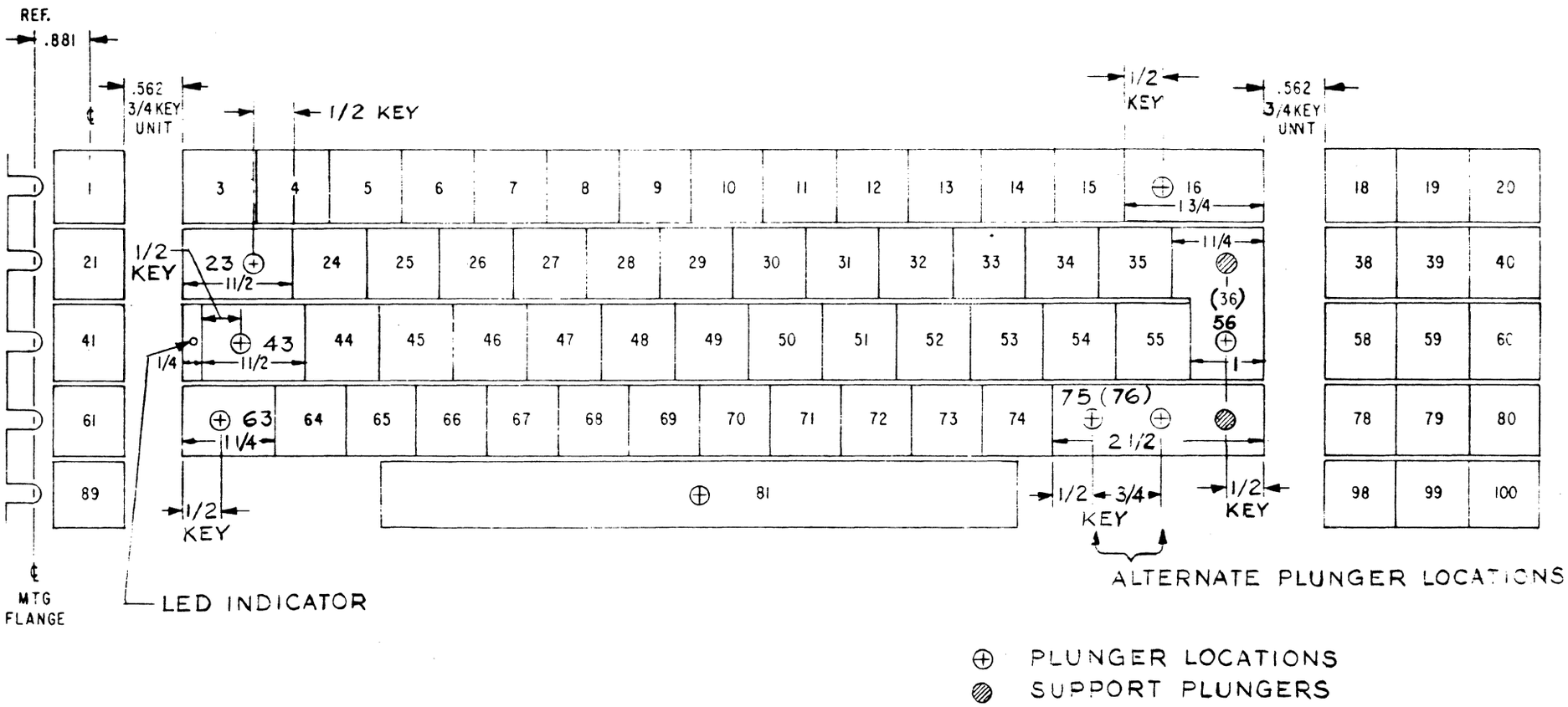


FIGURE - 3 CONFIGURATION 2-70 KEY & 75 KEY

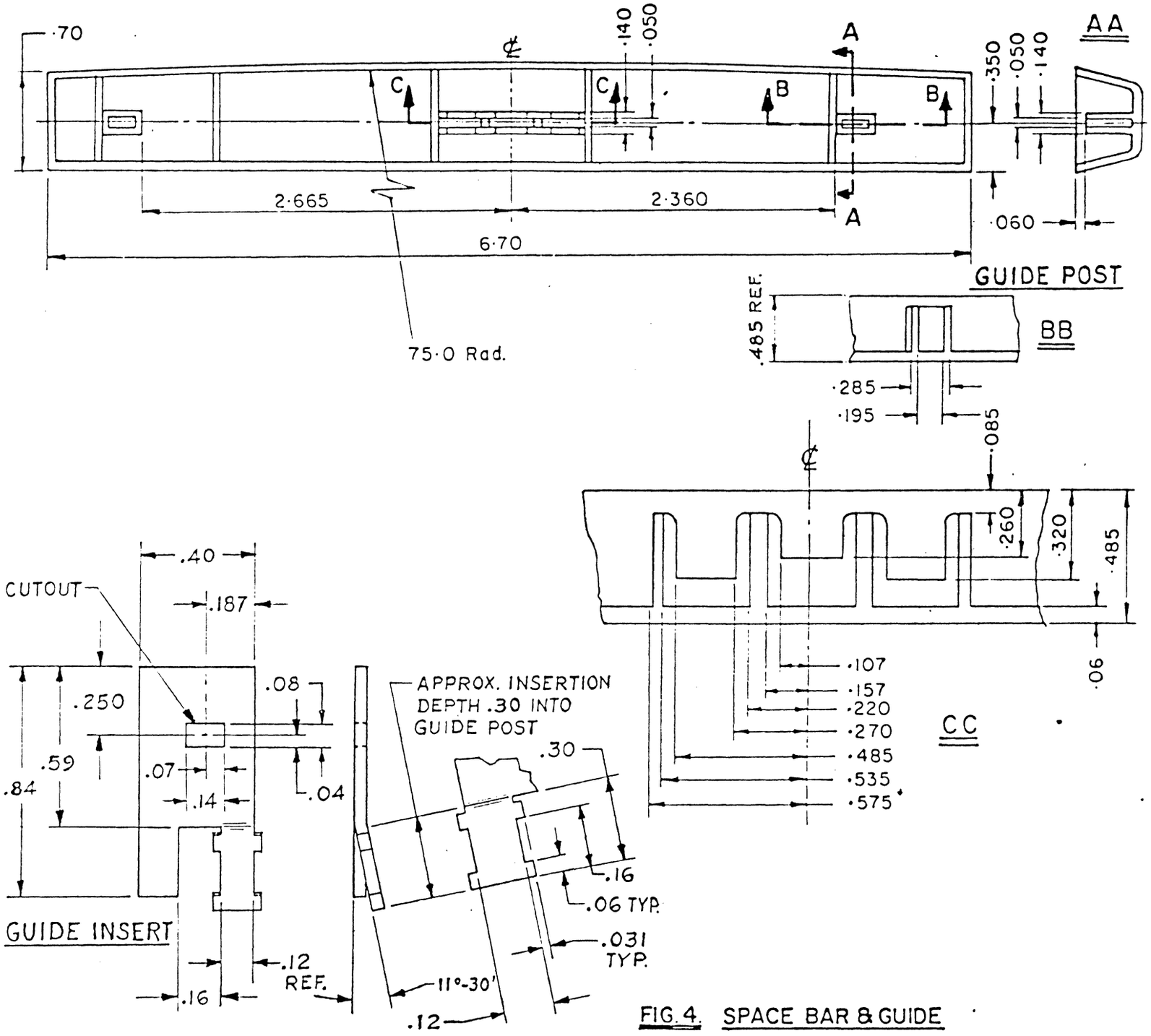


FIG. 4. SPACE BAR & GUIDE

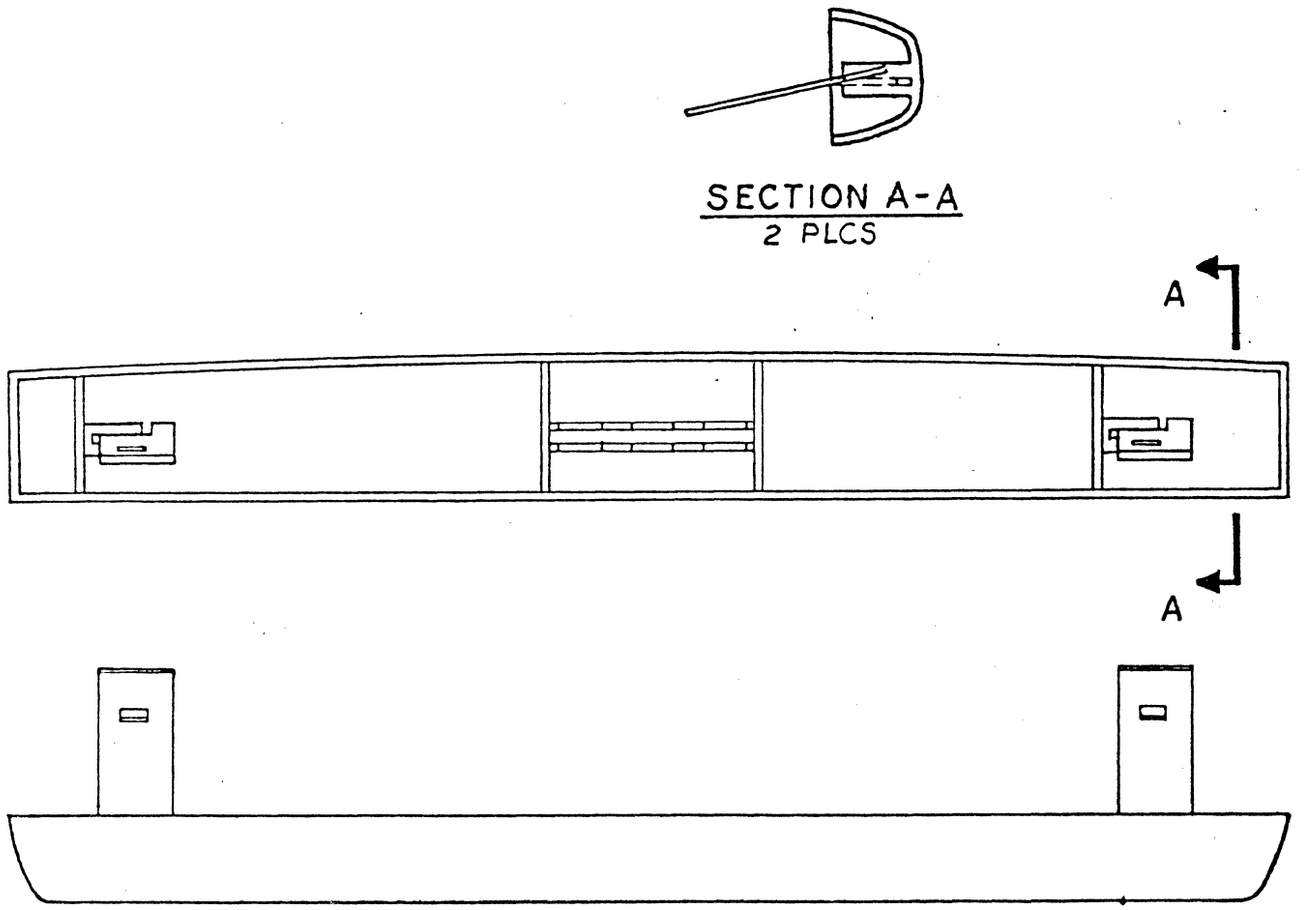


FIG. 5 SPACE BAR & GUIDE ASSEMBLY

AES

SA-400 disc drive

2.1 MAINTENANCE FEATURES

2.1.1 Alignment Diskette

The SA 124 alignment diskette is used for alignment of the SA 400. The following adjustments and checks can be made using the SA 124.

1. Read/write head radial adjustment using track 16.
2. Index photo detector alignment using track 01.
3. Track 00 is recorded with a 125 KHz signal (2F). This track is used to tell if the head is positioned over track zero when the track zero indication is true.
4. Track 34 has a 125 KHz signal (2F) recorded on it and is used to tell if the head is positioned over track 34 and for reference purposes.

Caution should be used in order not to destroy prerecorded alignment tracks. These tracks are 00, 01, 15, 16, 17, & 34. The write protect tab should always be installed on the SA 124 to prevent accidental writing on the SA 124.

2.1.2 Exerciser

The exerciser is a 800 exerciser with a special cable set. The exerciser PCB can be used in a stand alone mode or it can be built into a test station or used in a tester for Field Service.

The exerciser will enable the user to make all adjustments and check outs required on the SA 400 Mini Diskette drive.

The exerciser has no intelligent data handling capabilities but can write a 2F 125KHz signal which is the recording frequence used for amplitude check in the SA 400 drive. The exerciser can start and stop the drive motor, and enable read in the SA 400 to allow checking for proper read back signals.

2.1.3 Special Tools

The following special tools are available for performing maintenance on the SA 400.

Description	Part Number
Alignment Diskette	SA 124
Exerciser	54157
Head Cable Extender	54143

2.2 DIAGNOSTIC TECHNIQUES

2.2.1 Introduction

Incorrect operating procedures, faulty programming, damaged diskettes, and "soft errors" created by airborne contaminants, random electrical noise, and other external causes can produce errors falsely attributed to drive failure or misadjustment. Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate fault on second diskette.

2.2.2 "Soft Error" Detection and Correction

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. Usually these contaminants can be removed by the cartridge self-cleaning wiper.
2. Random electrical noise that usually lasts for a few μ seconds.
3. Small defects in the written data and/or track not detected during the write operation that may cause a soft error during a read.
4. Worn or defective load pad.
5. Improper grounding of the power supply, drive and/or host system. Refer to the SA 400 OEM manual for proper grounding requirements.
6. Improper motor speed.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten (10) times or until such time as the data is recovered.
2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.
3. Repeat step 1.
4. If data is not recovered, the error is not recoverable.

2.2.3 Write Error

In an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check". To correct the error, another write and check operation must be done. If the write operation is not successful after ten (10) attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists, the diskette should be replaced and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

2.2.4 Read Error

Most errors that occur will be "soft errors". In these cases, performing an error recovery procedure will recover the data.

2.2.5 Seek Error

1. Stepper malfunction.
2. Carriage binds.
3. To recover from a seek error recalibrate to track 00 and perform another seek to the original track or do a read I.D. to find what track the head is on and compensate accordingly.

2.2.6 Interchange Errors

This error is identified to be when data written on one drive cannot be read correctly on another drive.

Probable cause and checks:

1. Head alignment reference section 2.4.18.
2. Head amplitude low. Check on both drives per section 2.4.12.
3. Motor speed out of adjustment. Check on both drives per section 2.4.13.
4. Mis-clamping of the diskette caused by center hole damage. Replace the diskette and check the clamp hub.
5. If hard sectored check the index timing adjustment section 2.4.17.
6. If hard sectored insure the recommended sector format is being followed, reference the SA 400 OEM manual for proper format requirements.

2.2.7 Test Points SA 400

Reference figure 1.

T.P.
1. Read Data Signal
2. Read Data Signal
3. Read Data (Differentiated)
4. Read Data (Differentiated)
5. Signal Ground
6. + Read Data
7. + Index
8. – Detect Track 00
9. + Write Protect
10. Ground
11. – Head Load
12. + Gated Step Pulses
13. – Motor On

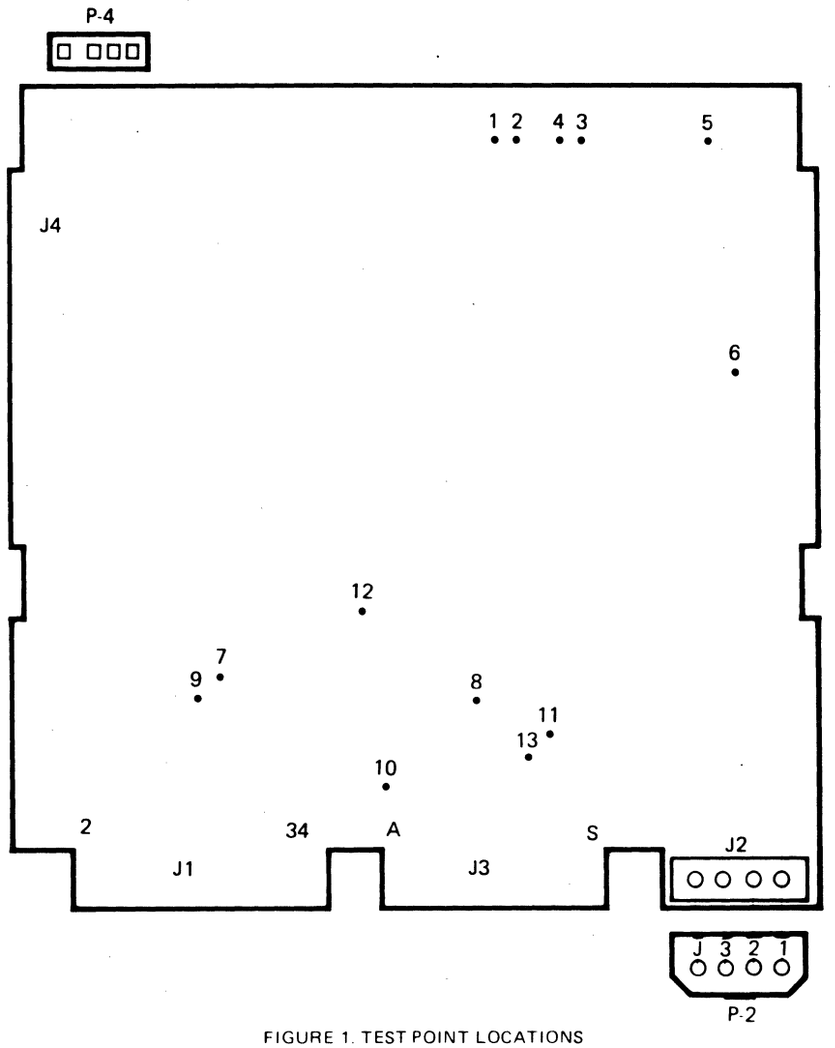


FIGURE 1. TEST POINT LOCATIONS

2.3 PREVENTIVE MAINTENANCE

Preventative maintenance is not required on the SA 400 minifloppy under normal usage.

2.4 REMOVALS AND ADJUSTMENTS

2.4.1 Face Plate: Removal and Installation

a. Open the door.

b. Remove the mounting screw on each side of the faceplate. Pull the face plate forward and away from the drive casting.

c. No re-adjustment is required after replacement.

2.4.2 Drive Motor Assembly: Removal and Installation (includes the motor and PCB)

Note: For ease of replacement it is recommended to replace the motor and PCB as an entire assembly.

a. Remove drive belt.

b. Disconnect connector P-3 from drive PCB and extract pins K (org) 13 (brn) and 14 (blk).

c. Remove drive PCB.

d. Remove the drive motor PCB and drive motor as an assembly by removing their respective mounting screws.

e. To re-install, reverse the above procedure insuring the PCB spacers and faston tab are in place.

f. Motor speed must be adjusted as per section 2.4.13.

2.4.3 Stepper Motor and Acuator Cam

These assemblies are not field replaceable.

2.4.4 Head and Carriage Assembly

a. Remove the drive PCB and disconnect the head connector from the PCB.

b. Unclamp the head cable from the drive.

c. Remove the guide rod nearest the read/write head.

d. Pivot the carriage away from the cam and off of the lower guide rod.

e. To re-install, reverse the above.

IMPORTANT: Insure that after installing the head cable there is enough slack to allow the carriage to go to track zero.

f. Readjust the carriage limiter if a new carriage is installed. Reference section 2.4.16.

g. Head alignment should not be required but if interchange problems exist check and adjust head alignment per section 2.4.18.

2.4.4.1 Read/Write Head Load Button: Removal and Installation

a. Remove drive PCB.

b. To remove the old button, hold the load arm out away from head, squeeze the locking tabs together with a pair of needle nose pliers and press forward.

c. To install load button, press the button into the arm, from the head side, and it will snap into place. Reference figure 2.

d. Adjust according to section 2.4.14.

2.4.5 Spindle Hub and Pulley/Assembly

These assemblies are not field replaceable.

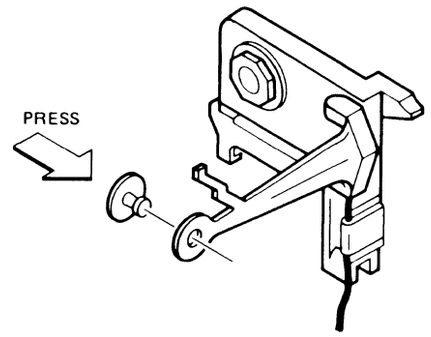


FIGURE 2. HEAD LOAD BUTTON REPLACEMENT

2.4.6 Clamp Hub Removal

a. Remove face plate, Reference section 2.4.1.

b. Remove the drive PCB.

c. Remove the E-ring from the hub shaft. The entire assembly can now be removed from the hub frame. Care should be taken not to overstress the hub frame mounting pivot springs.

d. To re-install: Place the hub clamp with spacer and spring in place onto the spindle hub. (The large end of the spring is placed against the hub frame).

e. Press the hub frame down towards the spindle until the hub shaft protrudes through its mounting hole in the hub frame.

f. Install the E-ring onto the hub shaft.

g. Re-install the face plate. Re-adjustment is not required.

2.4.7 Hub Frame Assembly Removal

Removal of this assembly is not normally required or recommended. The only time removal would be required in the field is to replace the entire assembly.

a. Remove the drive PCB.

b. Remove the 2 mounting screws that hold the pivot springs to the casting.

c. The hub frame assembly can now be lifted clear of the casting.

2.4.7.1 Hub Frame Assembly Installation and Adjustment

a. Put the hub frame onto drive and lightly tighten mounting screws removed in Step 2 of Removal Procedures.

b. Latch the hub frame closed.

c. Position the hub frame until the hub shaft is centered in its mounting hole in the hub frame Reference figure 3. Now tighten the mounting screws for the hub frame pivot springs.

d. Check that the door latch assembly does not bind in the face plate. If binding occurs loosen the door latch mounting screws and reposition until it is free of binds.

e. Reinstall the drive PCB.

f. Check and readjust the index timing if drive is used in hard sectored applications. Refer to section 2.4.17.

2.4.8 Write Protect Switch Removal

a. Remove the two mounting screws for the switch.

b. Unsolder the brown wire from the C terminal and the black wire from N/C on the switch.

c. After reinstallation adjust per section 2.4.19.

2.4.9 Index Detector Assembly Removal

a. Remove drive PCB.

b. From connector P-3 extract pins from 5 (orange) and E (red).

c. Remove the detector mounting screw from the hub frame. This will free the detector.

d. When installing a new assembly, insure the detector mounting block is flush against the side of the hub frame. Reference figure 3.

e. Re-adjust the index timing per section 2.4.17.

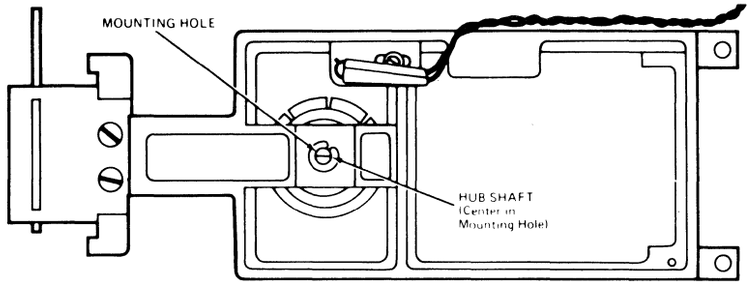


FIGURE 3. HUB FRAME ADJUSTMENT

Procedures for stepping carriage / Press "N" for track desired + carriage Return Key.

To cancel - hit cancel key.

2.4.10 Index LED Removal

a. Remove the drive PCB.

b. From connector P-3 extract the pins from 8 (blue) and J (purple).

c. Remove the platen from the base casting that the LED is mounted to.

d. Squeeze the led mounting block locking tabs together and press the assembly out of the mounting hole in the platen.

e. To re-install, reverse the removal procedure

f. When remounting the platen, insure it is flush with the machine surface on the casting. Position it laterally so a diskette can be inserted without binding when the door is closed.

g. Re-adjust the index timing per section 2.4.17 if hard sectored.

2.4.11 Track Zero Switch Removal

a. Remove the drive PCB.

b. The switch is removed by removing its two mounting screws.

c. Un-solder the wires N/C (white) N/O (yellow) and com (green).

d. To reinstall, reverse the above procedure.

e. Readjust the switch per section 2.4.15.

2.4.12 Head Amplitude Check

These checks are only valid when writing and reading back as described below. If the amplitude is below the minimum specified, the load pad should be replaced and the head should be cleaned if necessary (Reference section 2.4.21) before re-writing and re-checking. Insure the diskette used for this check is not "worn" or otherwise shows evidence of damage on either the load pad or the head side.

a. Install good media.

b. Start the motor.

c. Select the drive and step to track 34.

d. Sync the oscilloscope external on TP 7 (+ Index), connect one probe to TP-2 and one to TP-1, on the drive PCB. Ground the probes to the PCB, add and invert one input. Set volts per division to 50mv and time base to 20 M seconds per division.

e. Write the entire track with all one's.

f. The average minimum read back amplitude, peak to peak, should be 80 millivolts.

If a new load pad does not bring the amplitude to the minimum level try the following:

1. Install a different piece of media and re-check.
2. Check motor speed section 2.4.13.
3. Make sure you are getting an output from both TP-1 amd TP-2. Check with the scope in the chop mode. If the probes are OK and still one TP has no output or has less output than the other TP replace the PCB.
4. If 1, 2, & 3 are OK the head and carriage assembly will require replacement. Refer to section 2.4.4.

2.4.13 Motor Speed Adjustment

a. Install a diskette, start the motor and load the head. Step to Track 16.

b. Turn the pot R-12 located on the motor control PCB until the dark lines on the spindle pulley appear motionless. For 60 HZ use the outside ring of lines for the 50 HZ observe the inside ring. Reference figure 4.

NOTE: This adjustment can be made only in an area where there is flourescent lighting. Otherwise refer to 2.4.13.1.

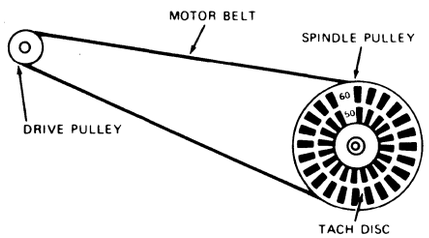


FIGURE 4. MOTOR SPEED ADJUSTMENT

2.4.13.1 Motor Speed Adjustment (using a frequency counter)

a. Install a SA104 or SA124 diskette, start the motor and load the head, step to Track 16.

b. Connect the frequency counter input to T.P. 7 (+ Index) on the drive PCB.

c. Adjust pot R-12 located on the motor control PCB for 200 HZ ±0.2 HZ.

2.4.14 Read/Write Head Load Button Adjustment

a. Insert SA124 diskette or any diskette with data on track 34.

b. Connect oscilloscope to TP 1 and 2, added differentially and sync external positive on TP 7 (+ Index).

c. Start the motor.

d. Select the drive and step carriage to track 34.

e. Observing read signal on oscilloscope, rotate the load button counterclockwise in small increments (10°) until maximum amplitude is obtained.

2.4.15 Track Zero Switch Adjustment

a. Remove the PCB from the drive, disconnect the head cable but leave the interface and drive connector installed.

b. Rotate head cam actuator until the cam follower is opposite the track zero dimple on the cam. Reference figure 5.

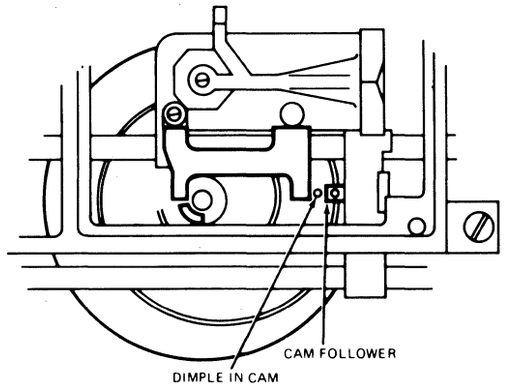


FIGURE 5. TRACK ZERO POSITION

c. Adjust the switch so it just makes by moving its mounting bracket.

NOTE: When making switch adjustments insure that the bracket is registered against the casting and the activator is located on the 45° angled portion on the rear of the carriage. Refer to figure 5.1.

d. Power up the drive being careful not to short out the PCB, and select the drive. This will energize phase A in the stepper motor. The dimple should remain within ±.050 of the cam follower and the switch should not break.

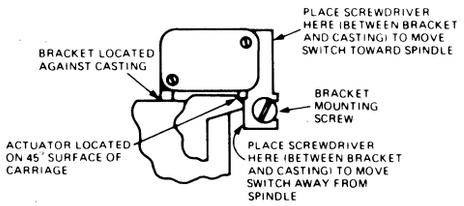


FIGURE 5.1. TRACK ZERO SWITCH ADJUSTMENT

e. Step to track 1 T.P. 8 should go high. If not readjust the microswitch.

f. Step to track 00 T.P. 8 should go low.

g. If not readjust the microswitch.

h. To check switch adjustment using a scope repeatively step between tracks zero and one. Look at TP 8 (–detect track zero). The step in and step out time should be equal within ± 2.5MS.

i. Reinstall PCB and plug in the head cable.

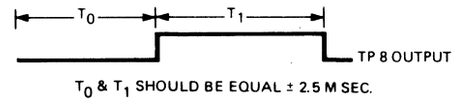


FIGURE 5.2. TRACK ZERO TIMING

2.4.16 Carriage Limiter

a. Unplug the head cable and remove the PCB from the drive leaving the interface and PCB connector installed.

b. Step to track zero, leave the drive selected.

c. Position the stop until it is flush with stop post (old style) or in the slot (new style) on the carriage assembly. Reference figure 6. Adjust the track zero cam stop horizontally and vertically until there is .020 ± .005 between the stop on the acuator cam and the stepper motor shaft. Reference figure 6.

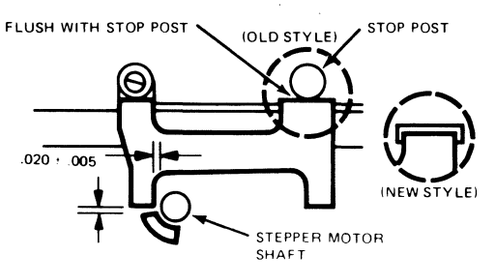


FIGURE 6. CARRIAGE LIMITER ADJUSTMENT

d. Step to track 34 and insure there is clearance between the cam stop extension and the stepper motor shaft. Reference figure 7.

e. Re-install the drive PCB and plug in the head cable.

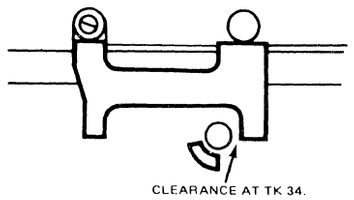


FIGURE 7. CARRIAGE LIMITER CLEARANCE

2.4.17 Index/Sector Timing Adjustment

If soft sectored, using the IBM type format:

a. Position the index detector assembly flush with the registration surface on the hub frame. Reference figure 8.

b. Position the detector assembly in the center of its mounting slot. Tighten the mounting screw, Reference figure 8.

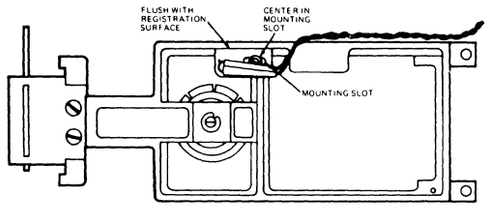


FIGURE 8. INDEX DETECTOR ADJUSTMENT

FOR HARD SECTORED APPLICATIONS:

a. Remove the PCB and install the head cable extender. Leave the PCB and interface connectors installed. Reference figure 9.

b. Insert Alignment Diskette (SA 124).

c. Start the motor and select the drive.

d. Sync oscilloscope, external positive, on TP 7 (+ Index). Set time base to 50 μsec/division.

e. Connect one probe to TP 1 and the other TP 2. Ground probes to the PCB. Set the inputs to AC, add and invert one channel. Set vertical deflection to 500 MV/division.

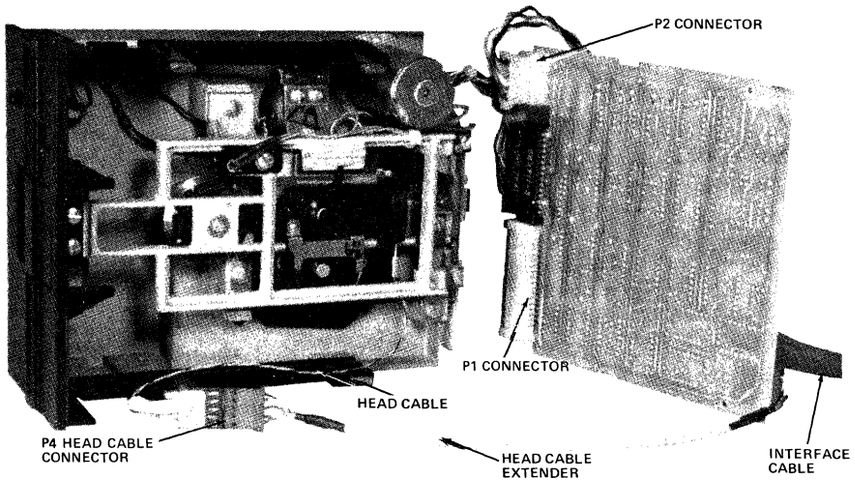
f. Observe the timing between the start of the sweep and the first data pulse. This should be 200 ± 100 μsec. If the timing is not within tolerance, continue on with the adjustment. Reference figure 10.

g. Loosen the mounting screw in the Index Detector block until the assembly is just able to be moved.

h. Observing the timing, adjust the detector until the timing is 200 ±50 μsec. Insure that the detector assembly is against the registration surface on the hub frame.

i. Tighten the mounting screw.

j. Recheck the timing.



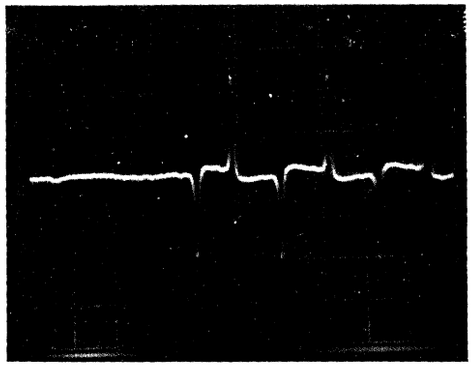


FIGURE 10. INDEX TIMING

2.4.18 Head/Radial Alignment

NOTE: This adjustment is not normally required even on head replacement due to the SA 400 pre-aligned head and carriage assembly, but if the stepper motor mounting screws are accidently loosened or if parts damage has occured or you are experiencing interchange problems use the following procedure to check and/or adjust the head radial alignment.

a. Start the motor and select the drive.

b. Load the SA 124 alignment diskette.

c. Step the carriage to track 16.

d. Sync the oscilloscope, external positive, on TP 7 (+CE Index). Set the time base to 20 Msec per division. This will display over one revolution.

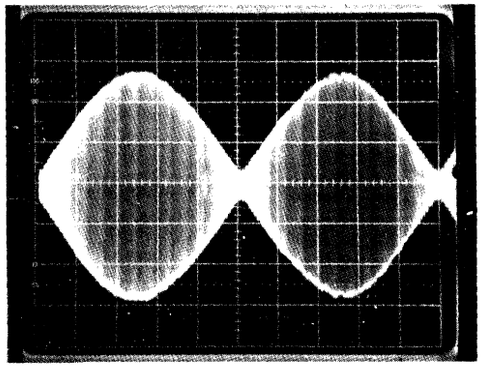


FIGURE 11. HEAD RADIAL ALIGNMENT

e. Connect one probe to TP 1 and the other to TP 2. Ground the probes on the PCB. Set the inputs to AC, add and invert one channel. Set the vertical deflection to 100 MV/dev.

f. The two lobes must be within 70% amplitude of each other. If the lobes do not fall within the specification, continue on with the procedure. Reference figure 11.

g. Loosen the two mounting screws which mount the stepper motor to the drive casting.

h. Rotate the stepper motor to radially move the head in or out. If the left lobe is less than 70% of the right, turn the stepper motor clockwise as viewed from the stepper motor side of the drive. If the right lobe is less than 70% of the left lobe, turn the stepper motor counterclockwise as viewed from the stepper motor side of the drive.

i. When the lobes are of equal amplitude, tighten the motor mounting screws. Reference figure 12.

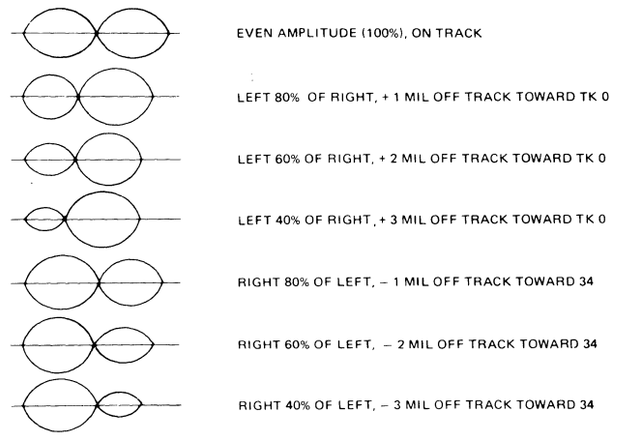


FIGURE 12. HEAD RADIAL ALIGNMENT

j. Check the adjustment by stepping off track and returning. Check in both directions and readjust as required.

k. Whenever the Head Radial Alignment has been adjusted, the carriage limiter and track zero switch adjustment must be checked (Section 2.4.15 & 2.4.16).

NOTE: (Alignment diskette should be at room conditions for at least twenty minutes before alignment).

2.4.19 Write Protect Switch Adjustment

a. Adjust the switch so that the actuator will just transfer the switch when its point is flush ±.010 within the top of the groove in the guide rail. Reference figure 13.

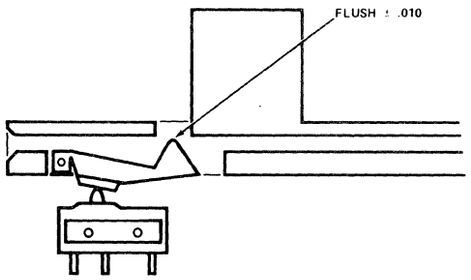


FIGURE 13. WRITE PROTECT SWITCH ADJUSTMENT

2.4.20 Head Load Bail Adjustment

a. Select the drive to load the head or ground TP 11 (–Head Load) to energize the head load solenoid.

b. Adjust the down stop screw to obtain 3/16" to 1/4" from the top flat surface of the load bail and the platen. Reference figure 14.

c. Check for a minimal clearance of .020 between the load bail and the load arm. This check is made at track zero and track 34 with the door closed and the head loaded.

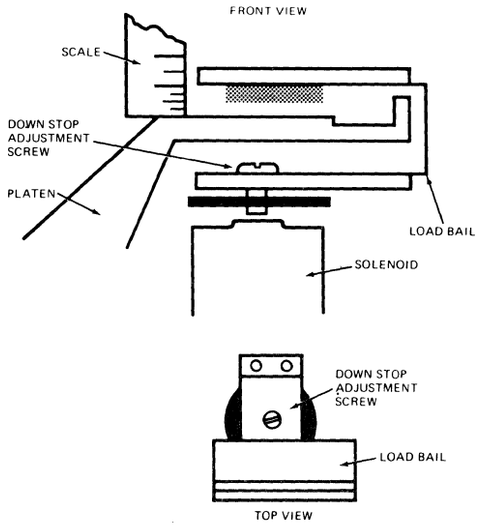


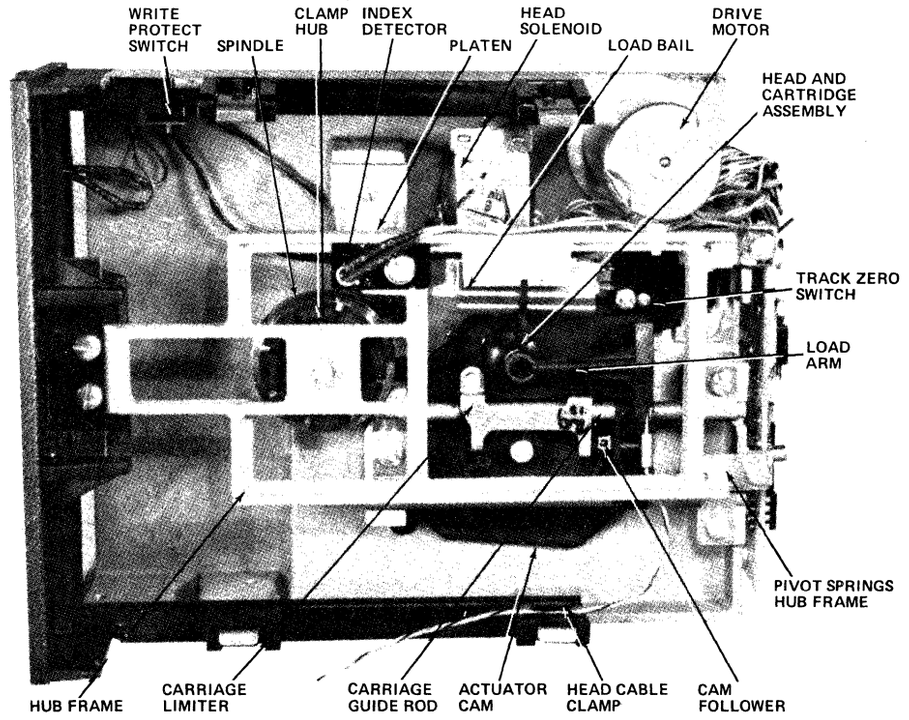
FIGURE 14. HEAD LOAD BAIL ADJUSTMENT

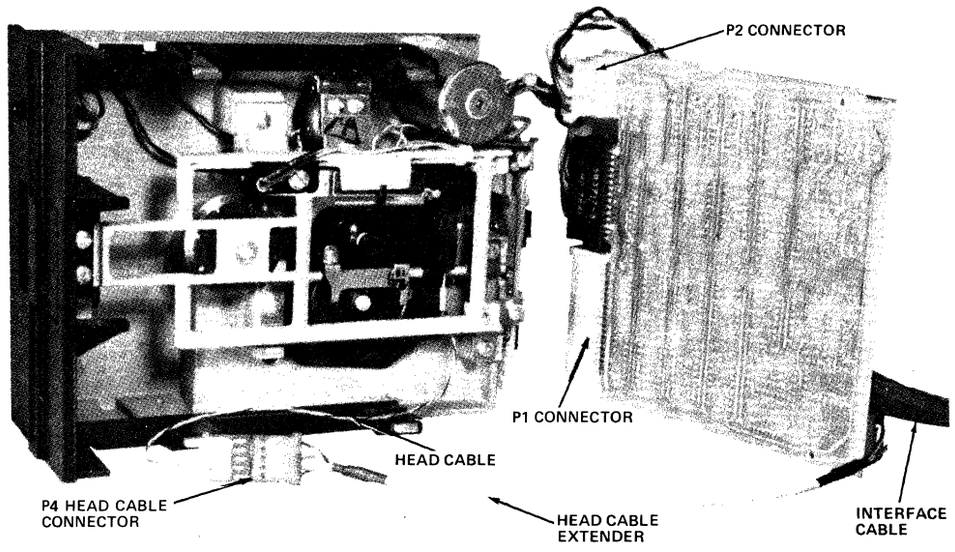
2.4.21 Read/Write Head Cleaning Procedure

The head should *ONLY* be cleaned if it has an oxide build up that is visable to the naked eye. Cleaning methods and materials other than those listed can permanently damage the head and should be avoided.

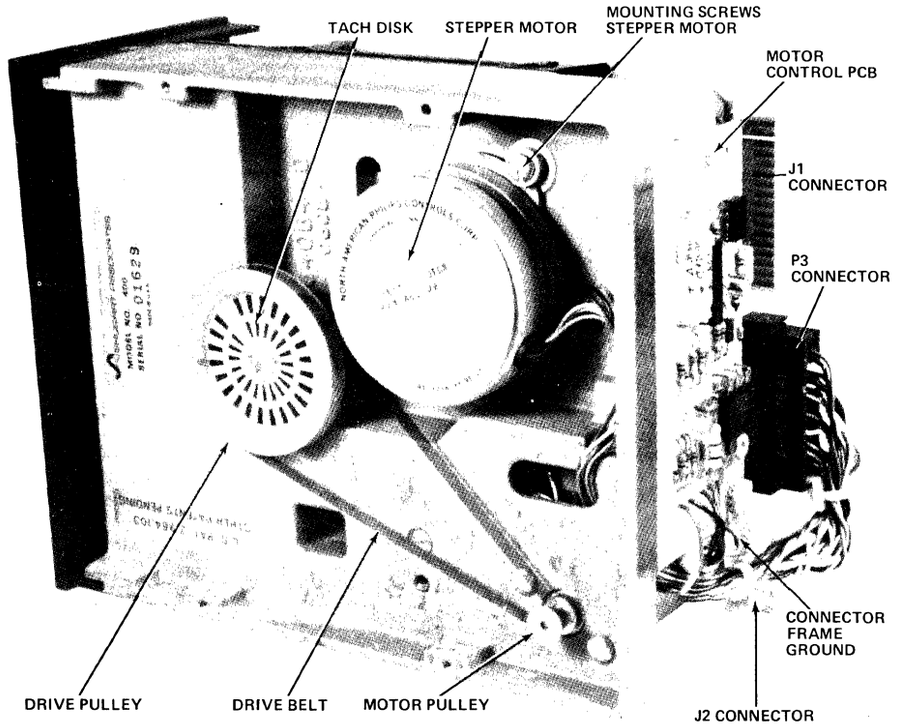
1. Lightly dampen a piece of clean lintless tissue with Isopropyl alcohol (use sparingly).
2. Lift the load arm off the head, being careful not to touch the load button.
3. Lightly wipe the head with the moistened portion of the tissue.
4. After the alcohol has evaporated, lightly polish the head with a clean dry piece of lintless tissue.
5. Lower the load arm onto the head. *Do not let it snap back.*

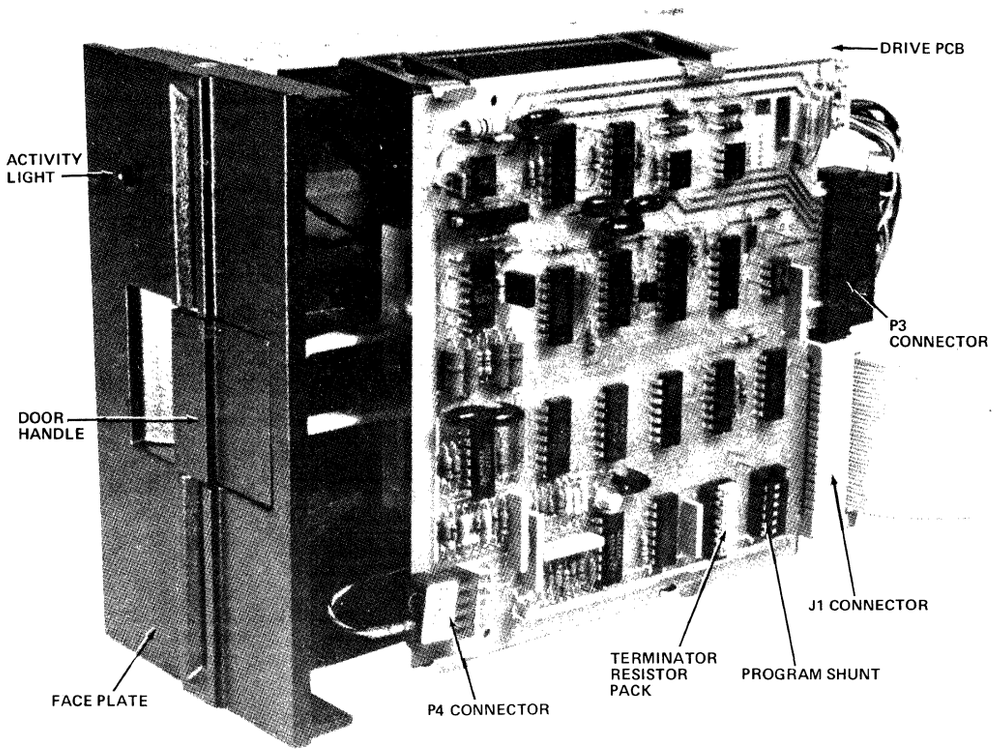
Physical Locations

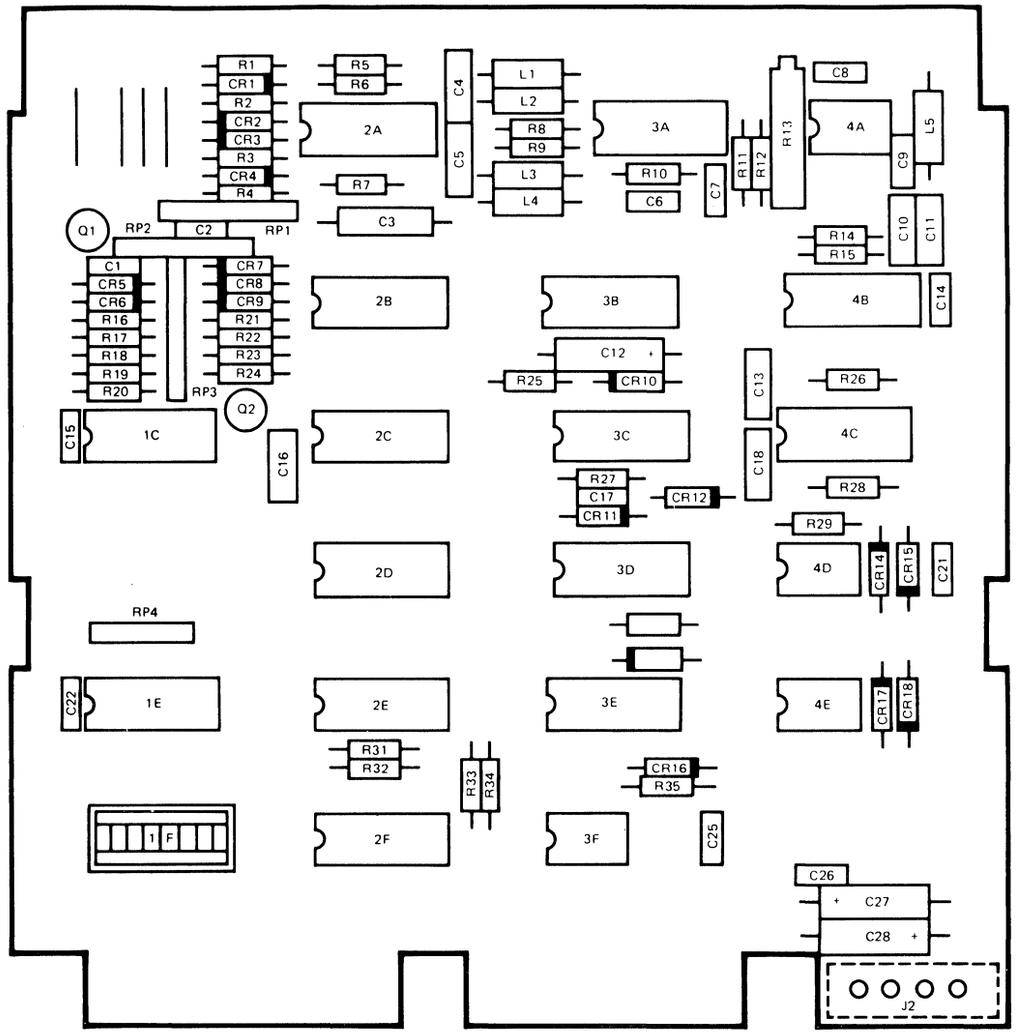




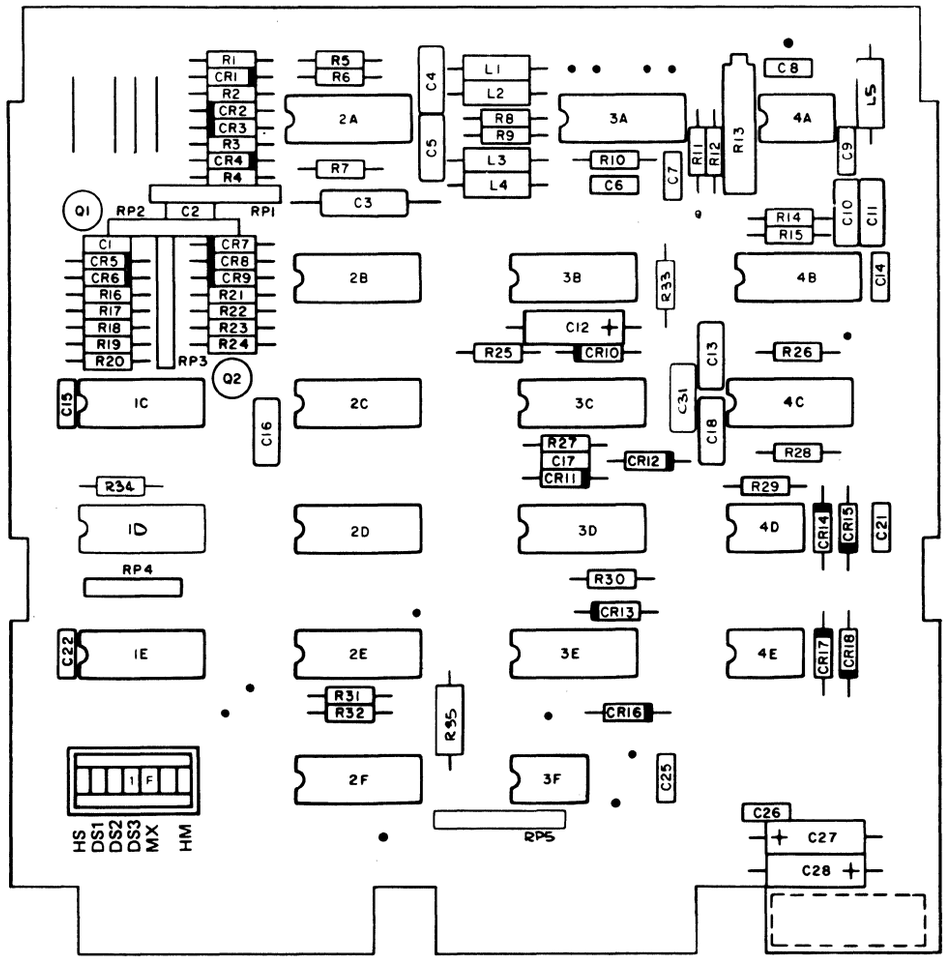
PCB Component Locations







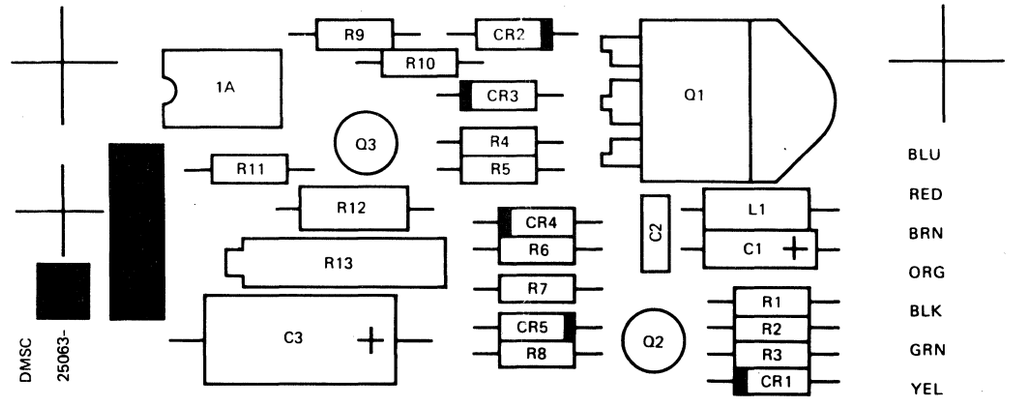
DRIVE PCB
COMPONENT LOCATIONS
BELOW E.C. 649



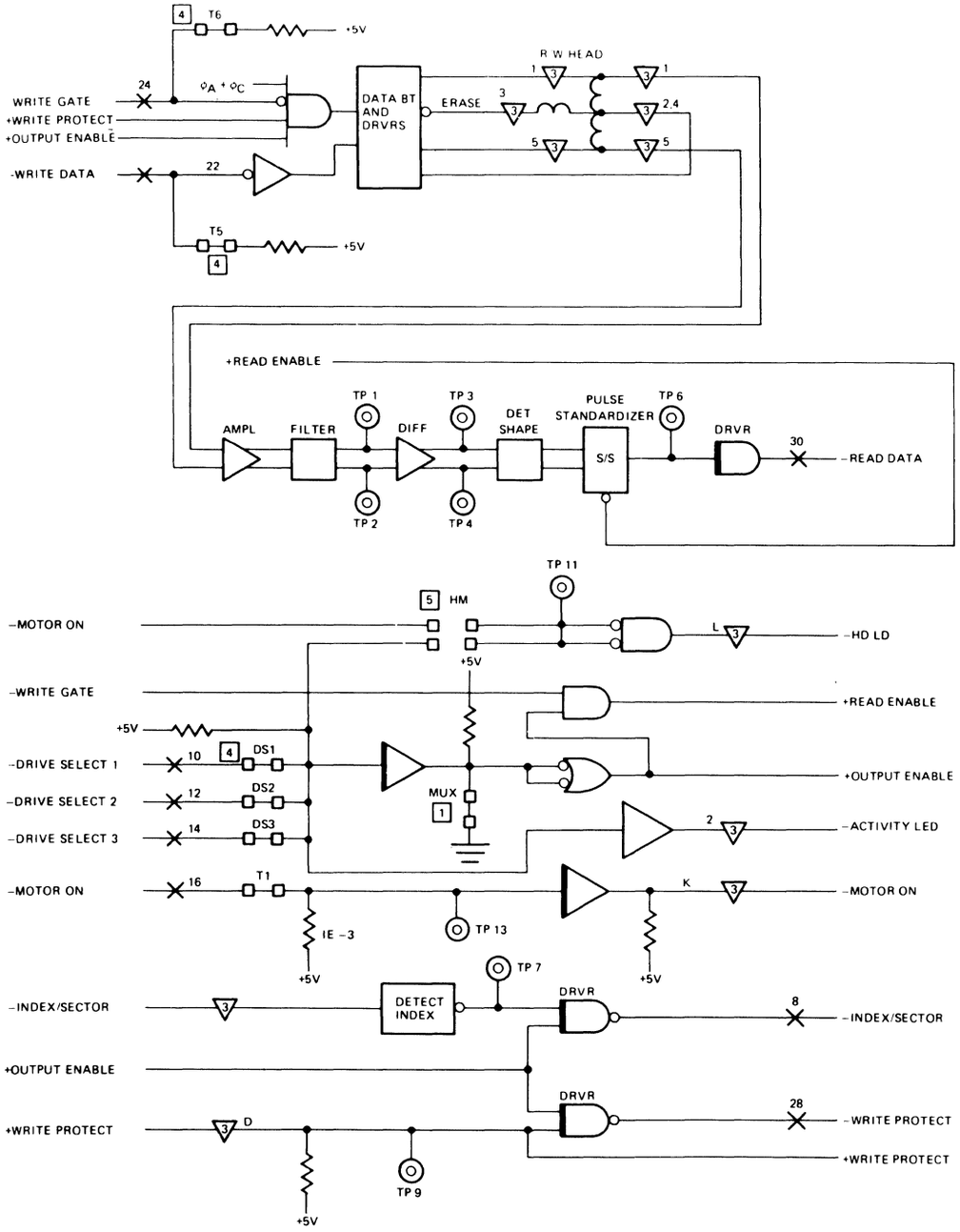
● TEST POINTS

DRIVE PCB
COMPONENT LOCATIONS

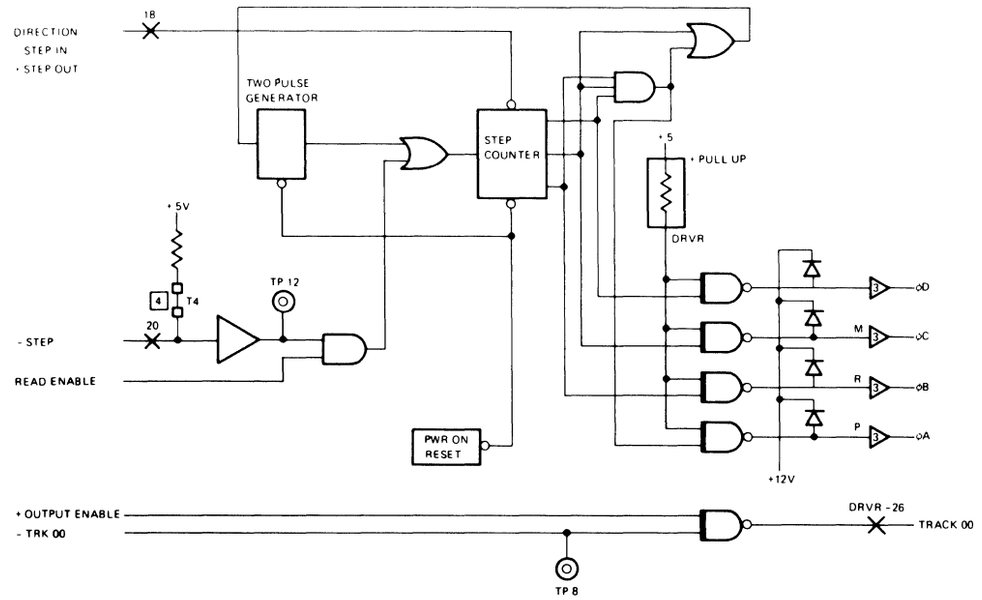
E.C. 649 AND ABOVE

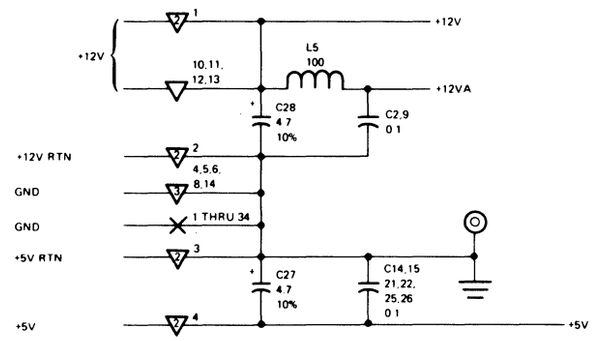


MOTOR CONTROL PCB
COMPONENT LOCATIONS



DRIVE PCB LOGIC DIAGRAM PCBP/N 25060
READ/WRITE, INDEX,
WRITE PROTECT, DRIVE SELECTION

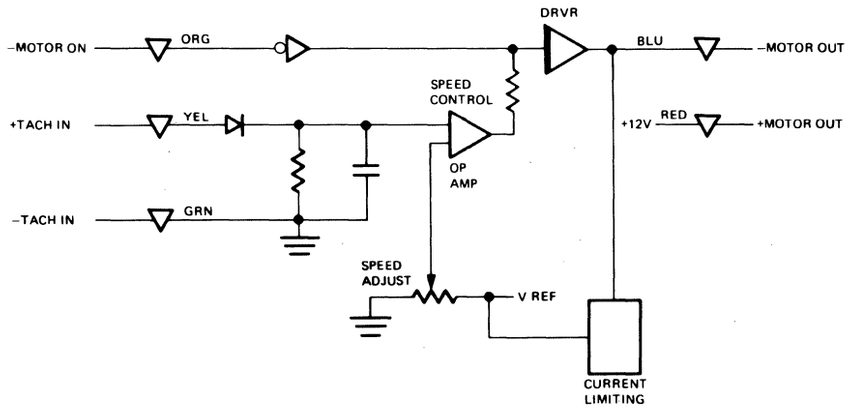


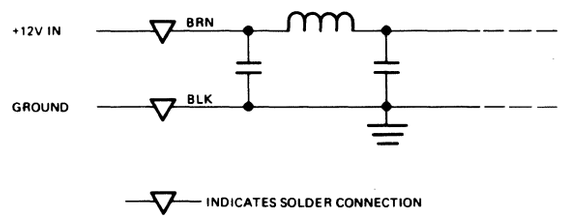


NOTES:

1. CUT TRACE OPTION FOR MULTIPLEX OPERATION
2. CONNECTOR SYMBOL REFERENCE ✕ = J1, ▽ = J2, ▽ = J3, ▽ = J4
3. ALL ODD NUMBERED PINS ON J1 CONNECTOR ARE GROUND
4. PROGRAM SHUNT
5. WITH HM SHORTED HEAD LOADS WITH -MOTOR ON
   WITH HS SHORTED HEAD LOADS WITH -DRIVE SELECT

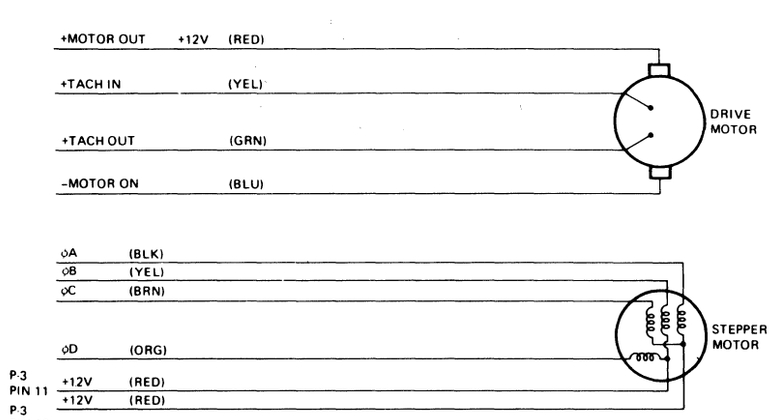
DRIVE PCB
STEPPER CONTROLS, TRACK ZERO,
POWER

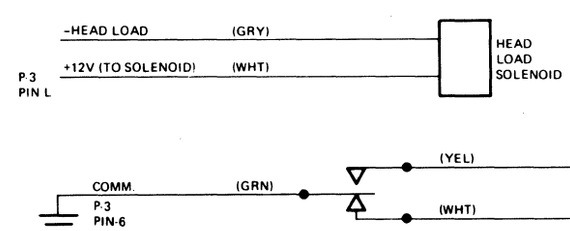


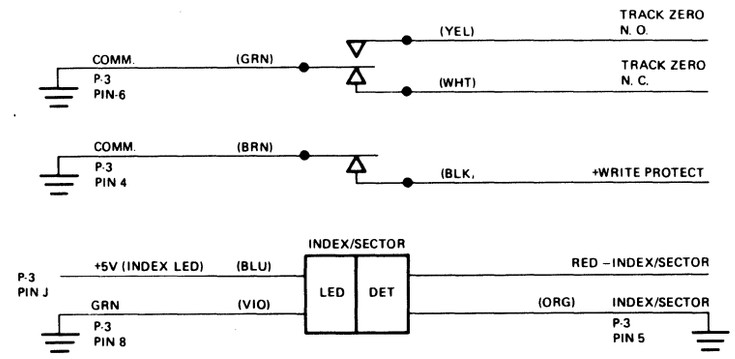


INDICATES SOLDER CONNECTION

MOTOR SPEED CONTROL PCB LOGIC DIAGRAM
AMPLITUDE MODULATION PCB P/N 25062

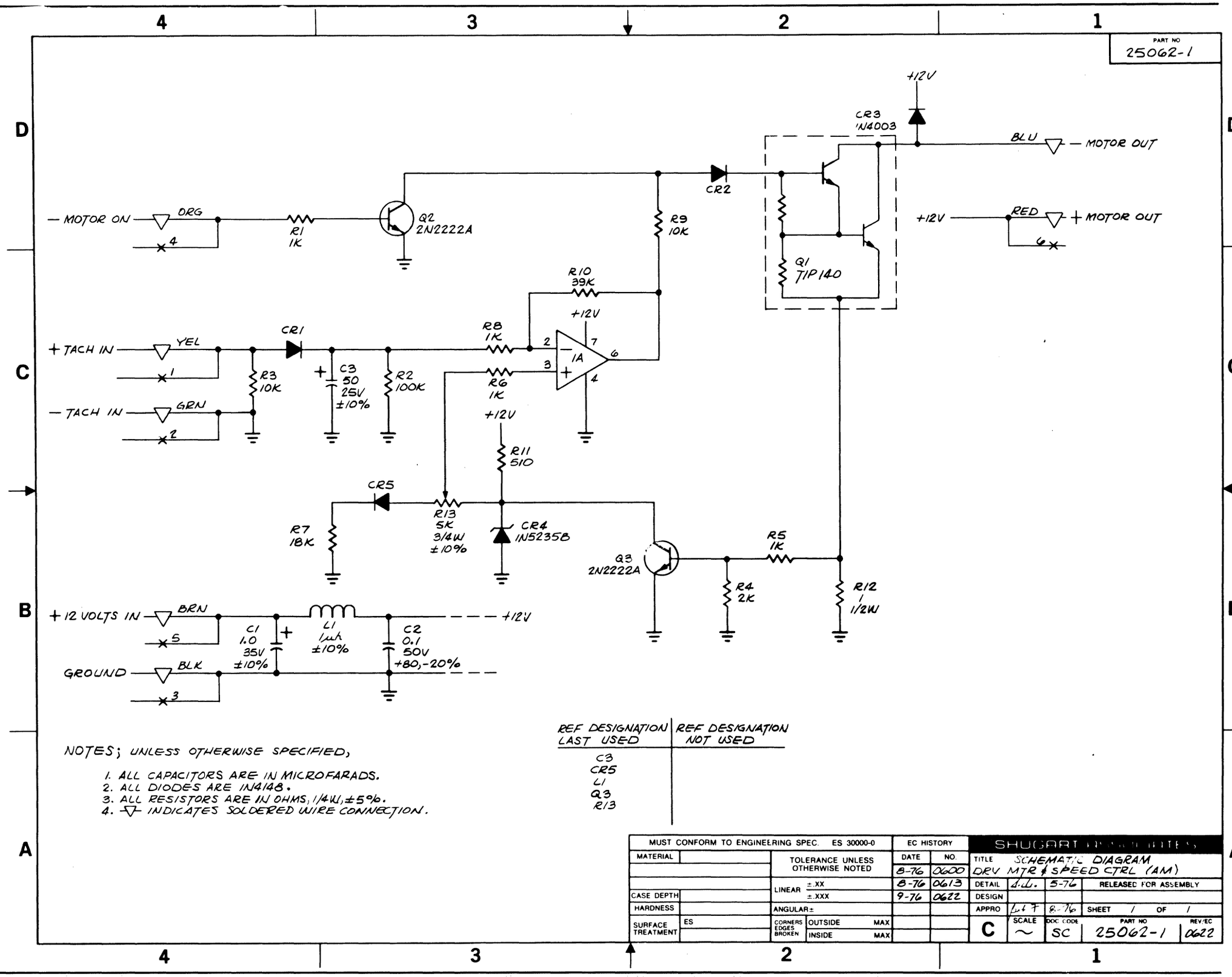






SWITCH AND MOTOR CONNECTIONS

Schematics



NOTES; UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL DIODES ARE IN4148.
3. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
4. ▽ INDICATES SOLDERED WIRE CONNECTION.

REF DESIGNATION LAST USED	REF DESIGNATION NOT USED
C3	
CR5	
L1	
Q3	
R13	

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0

MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED		
		LINEAR ±.XX		
		±.XXX		
CASE DEPTH		ANGULAR ±		
HARDNESS				
SURFACE TREATMENT	ES	CORNERS EDGES BROKEN	OUTSIDE MAX	
			INSIDE MAX	

EC HISTORY		
DATE	NO.	
8-76	0600	
8-76	0613	
9-76	0622	

SHUGART

TITLE SCHEMATIC DIAGRAM DRV MTR & SPEED CTRL (AM)

DETAIL	J.J.	5-76	RELEASED FOR ASSEMBLY
DESIGN			
APPRO	[illegible]	8-76	SHEET 1 OF 1

SCALE	DOC CODE	PART NO	REV/EC
C	~	SC	25062-1	0622

25061-1

-MOTOR ON
-WRITE DATA
-WRITE GATE
+WRITE PROT. X5400
-DRIVE SELECT 1
-DRIVE SELECT 2
-DRIVE SELECT 3
-STEP
DIRECTION
+PULL UP X5400
-TRACK ZERO N.C.
+TRACK ZERO N.C.

-MTR ON
R/W 1 X5400
R/W 2 X5400
R/W CT. X5400
-ACTIVITY LED
ACTIVITY LED
-HEAD LOAD
+READ ENABLE X5400
+OUTPUT ENABLE X5400
ERASE
-TRACK ZERO
ΦD
ΦC
ΦB
ΦA

+5V
+12V
TP13
TP12
TP11
TP8
RP1
RP2
RP3
RP4
RP5
R16 2.26K 1/8W 1%
R17 2.26K 1/8W 1%
R18 20K
R19 20K
R20 604 1/8W 1%
R21 20K
R22 274 1/8W 1%
R23 909 1/8W 1%
R24 75 1/8W 1%
R25 10K
R27 10K
R30 100
R33 300
R34 150
C1 .033 ±20%
C12 4.7 10%
C17 .1 10%
C29
C31 7500pf 300V 5%
C6 300pf 500V 5%
Q1 2N2222
Q2 2N2222
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14 IN4003
CR15 IN4003
CR16 IN4003
CR17 IN4003
CR18 IN4003
1C
1D
1E
1F
2B
2C
2D
2E
2F
3B
3C
3D
3E
3F
4B
4C
4D
4E
4-BIT SREG
DS1
DS2
DS3
MX
HM
HS

XS401

MUST CONFORM TO ENGINEERING SPEC ES 30006-0		REVISIONS	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO
CASE DEPTH	LINEAR .XX .XXX		
HARDNESS	ANGULAR		
SURFACE TREATMENT ES	(BREAK EDGES) OUTSIDE MAX INSIDE MAX		

SHUGART ASSOCIATES

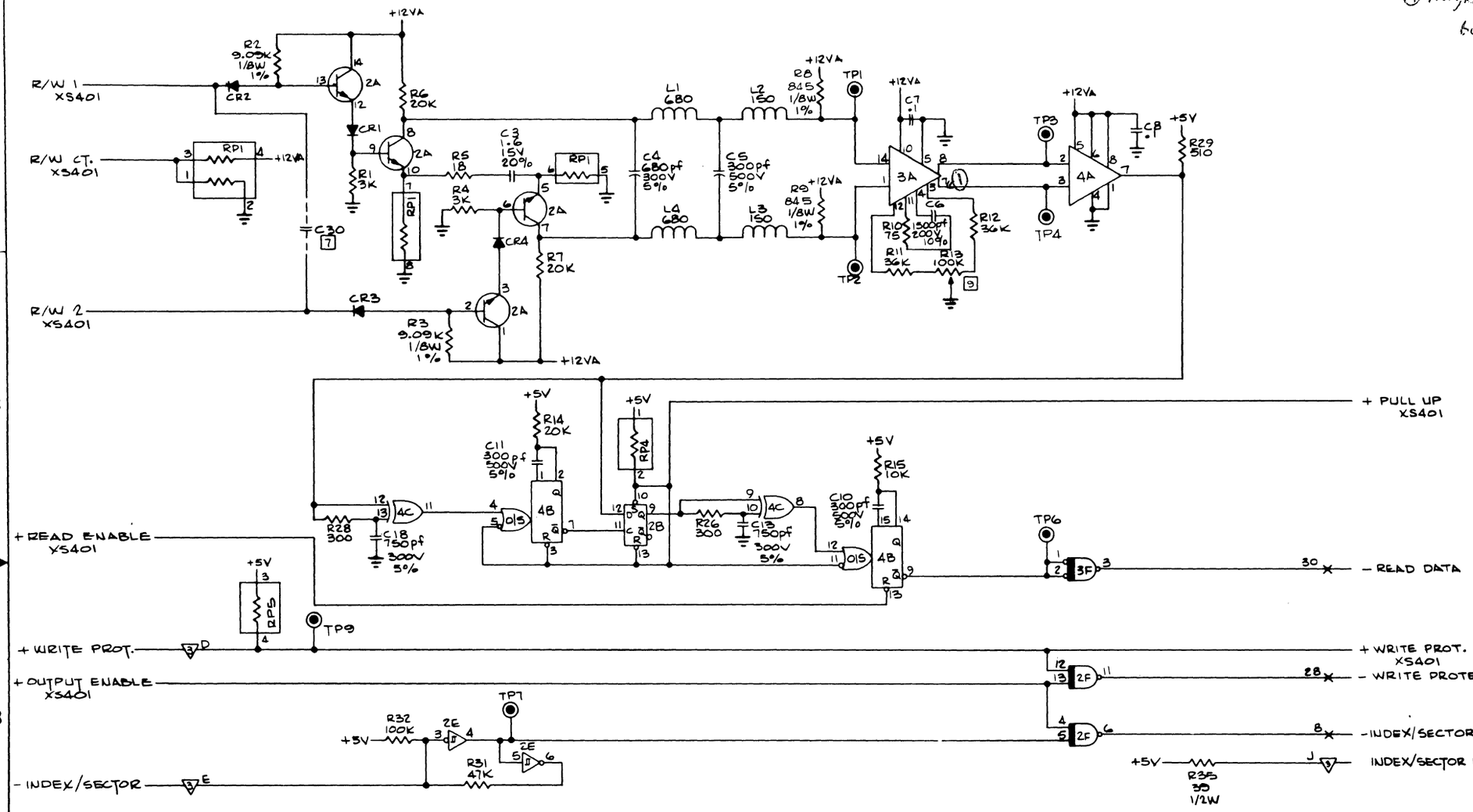
TITLE SCHEMATIC DIAGRAM DISKETTE, MINI

DETAIL	4	8-76	RELEASED FOR ASSEMBLY
DESIGN			T25061
APPRO			SHEET 2 OF

D | SCALE ~ | SC | PART NO. 25061-1 | REV. 0049

PART NO. 25061-1

① Program would not load
bad solder connection on pin 2. (IC 34)



NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80, -20%.
2. ALL DIODES ARE IN4148.
3. ALL INDUCTORS ARE IN MICROHENRIES, 10%.
4. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
5. ○—○ INDICATES CUT TRACE OPTION.
6. ✱ INDICATES J1, ▽ INDICATES J2, ▽ INDICATES J3, ▽ INDICATES J4.

[7] COMPONENT NOT INSTALLED.

8 PIN 4 OF ID IS GROUND.

[9] R13 VALUE MAY BE 50K.

RESISTOR ARRAY		
VALUE	POSITION	UNUSED
330Ω	RP2, 3	
680Ω	RP1	
150Ω	RP5	
1K	RP4	

TYPE	POS.	UNUSED	VCC (PIN)	GND (PIN)	VDD (PIN)	TYPE	POS.	UNUSED	VCC (PIN)	GND (PIN)	VDD (PIN)
7400	3E		14	7	—	75453B	3F		8	4	—
7402	3B		14	7	—	LM311N	4A		—	1	8
74LS14	2E		14	7	—	NE592A	3A		—	5	10
7407	2C	2C4	14	7	—	7486	4C	4C1, 2	14	7	—
7433	2D		14	7	—	9602	4B, 3C		16	8	—
7438	2F		14	7	—	2QT2222	2A		—	—	—
7474	2B, 1D	1D1 8	14	7	—	2QT2905	1C		—	—	—
7419S	3D		16	8	—	150Ω	1E	2	—	—	—
75452P	4D, 4E		8	4	—						

REF DESIGNATION LAST USED	REF DESIGNATION NOT USED
C31	C19, 20, 23, 24, 29, 30 (RESERVED)
CR18	
L5	
Q2	
R35	
RP5	
TP13	

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0

MATERIAL

TOLERANCE UNLESS OTHERWISE NOTED
LINEAR ± .XX, ± .XXX
ANGULAR ±
CORNERS EDGES BROKEN: OUTSIDE MAX, INSIDE MAX

CASE DEPTH

HARDNESS

SURFACE TREATMENT ES

EC HISTORY

DATE	NO.
8-76	0600
8-76	0615
9-76	0618
10-76	0628
11-76	0643
12-76	0649

TITLE SCHEMATIC DIAGRAM DISKETTE, MINI

DETAIL Yada 7-7-76 RELEASED FOR ASSEMBLY
DESIGN T25061
APPRO 8-76 SHEET 1 OF 2
SCALE NONE DOC CODE SC PART NO 25061-1 REV EC 0649

PART NO 25061-0

-MOTOR ON
-WRITE DATA
-WRITE GATE
+WRITE PROT. XS400
-DRIVE SELECT 1
-DRIVE SELECT 2
-DRIVE SELECT 3
-STEP
DIRECTION
+PULL UP XS400
-TRACK ZERO N.O.
+TRACK ZERO N.C.

-MTR ON
R/W 1 XS400
R/W 2 XS400
ERASE
R/W CT. XS400
-ACTIVITY LED
ACTIVITY LED
INDEX/SELECTOR LED
-HEAD LOAD
+READ ENABLE XS400
+OUTPUT ENABLE XS400
ϕD
ϕC
ϕB
ϕA
-TRACK ZERO

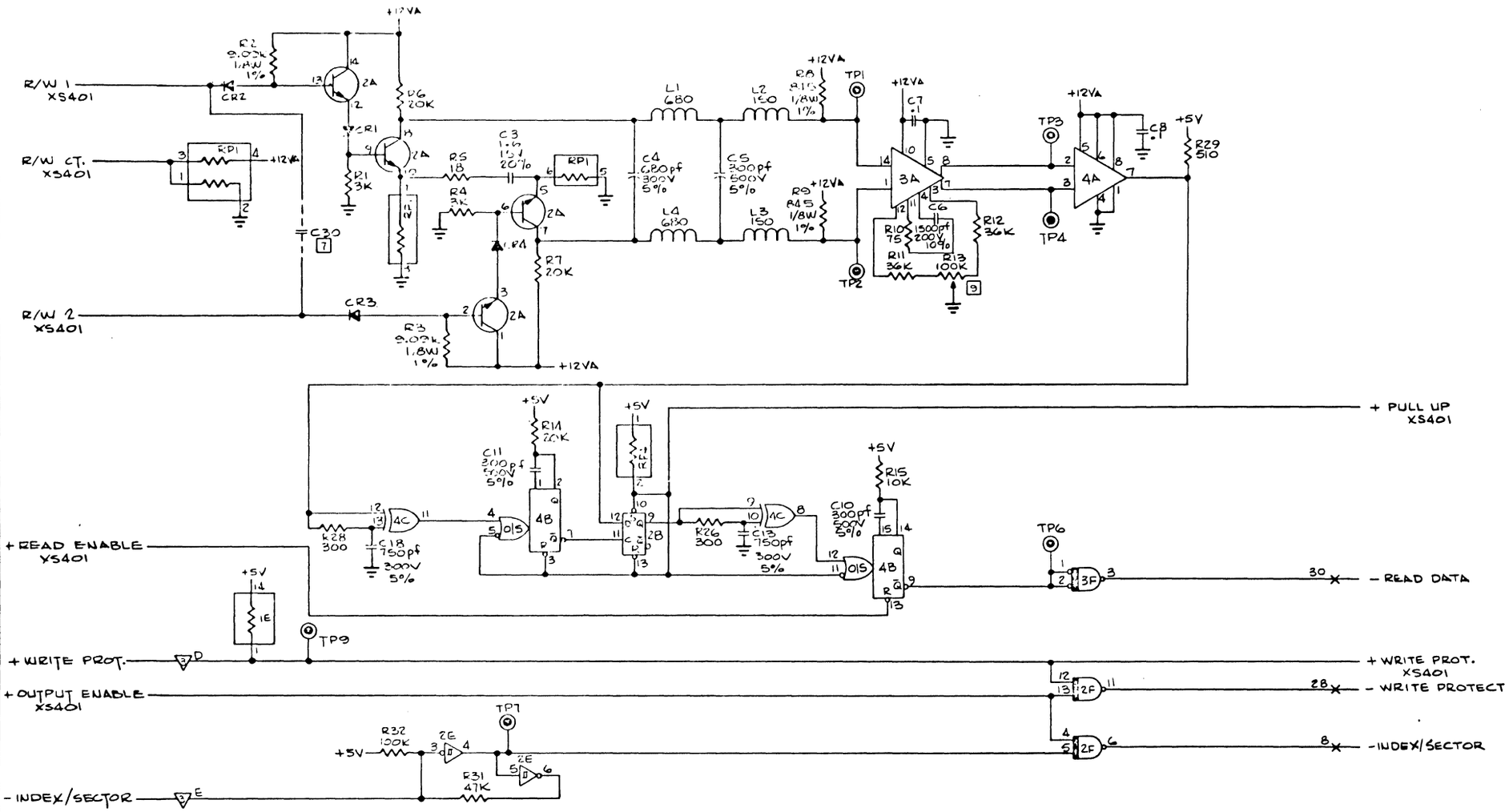
XS401

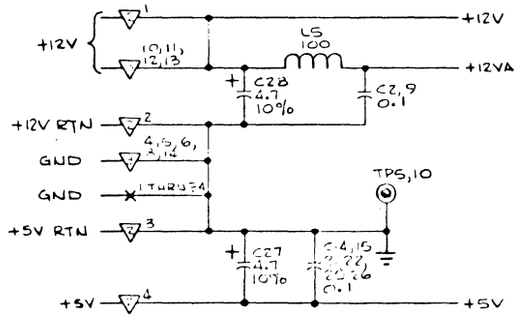
MUST CONFORM TO ENGINEERING SPEC ES 30000-0			EC HISTORY		
MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO	
CASE DEPTH		LINEAR ± XX ± XXX			
HARDNESS		ANGULAR ±			
SURFACE TREATMENT	ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			

TITLE SCHEMATIC DIAGRAM DISKETTE, MINI

DETAIL JJ SSC RELEASED FOR ASSEMBLY
DESIGN 25061
APPRO SHEET 2 OF
D SCALE ~ SYS CODE SC PART NO 25061-0 REV EC 0643

PART NO 25061-0





NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80, -20%.
2. ALL DIODES ARE IN4148.
3. ALL INDUCTORS ARE IN MICROHENRIES, 10%.
4. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
5. ⊓—⊓ INDICATES CUT TRACE OPTION.
6. ✱ INDICATES J1, ▽ INDICATES J2, ▽ INDICATES J3, ▽ INDICATES J4.

[7] COMPONENT NOT INSTALLED.

[8] RESISTOR PACK RP1 IS 680Ω, RP2 IS 330Ω, RP3 IS 330Ω, AND RP4 IS 1K.

[9] R13 VALUE MAY BE 50K.

REF DESIGNATION LAST USED	REF DESIGNATION NOT USED
C30	C19,20,23,24,29,30 (RESERVED)
CR18	
L5	
Q2	
R36	
RP4 [8]	
TP12	

TYPE	POS.	UNUSED	VCC (P.N)	GND (P.N)	VDD (P.N)	TYPE	POS.	UNUSED	VCC (P.N)	GND (P.N)	VDD (P.N)
1400	3C		14	7	—	75453B	3F		8	4	—
1402	3B		14	7	—	LM311N	4A		—	1	8
1LS14	2E		14	7	—	NE592A	3A		—	5	10
7401	2C	2C4	14	7	—	7486	4C	4C1,2	14	7	—
1423	2D		14	7	—	9602	4B,3C		16	8	—
7428	2F		14	7	—	2QT2222	2A		—	—	—
7474	1B		14	7	—	2QT2905	1C		—	—	—
1415	3D		16	8	—	150Ω	1E		—	—	—
1413 2P	4D,4E		8	4	—						

MUST CONFORM TO ENGINEERING SPEC ES 30000-0			EC HISTORY		
MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO	TITLE SCHEMATIC DIAGRAM DISKETTE - MINI
			8-76	0000	
		LINEAR .XX / .XXX	9-76	0015	DETAIL RELEASED FOR ASSEMBLY
CASE DEPTH			9-76	0028	DESIGN
HARDNESS		ANGULAR ±	10-76	0028	APPRO SHEET 1 OF 2
SURFACE TREATMENT	ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX	11-76	0043	D SCALE DOC CODE PART NO REV EC

XS400