PLURIBUS DOCUMENT 7: MAINTENANCE

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PLURIBUS DOCUMENT 7: MAINTENANCE

PREFACE

"Pluribus Document 7: Maintenance" is part of a series which provides complete documentation for the Pluribus line of computer systems. The present volume is a compendium of documentation on each of the card types which may be used to construct Pluribus systems. For each card type we include schematic diagrams and a logic description (a textual description of the gate-by-gate workings of the logic). In many cases a document is applicable to many card types. In this event the document is included in whole under one of the card types and cross-referenced in the other relevant sections. Documentation for the various Pluribus cables is also included.

By its nature, this document will be updated frequently. Accordingly, if you wish to be included in the list of people who will receive updates, please notify Julie Moore, Bolt Beranek and Newman Inc., 50 Moulton Street, Cambridge, MA 02138.

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APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/1/78	
B	ECN 327	9/18/78	EC

ALD

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER 751219

APPD FOR REL 751219

APPD (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

ALD LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		ALD-02

SCALE	REV B	SHEET OF

ALD

SUE 1240 AUTO-LOAD, GENERAL

MAINTENANCE BULLETIN M1240

1466

ALD

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PREFACE

This maintenance bulletin contains a detailed description of the SUE 1240 Auto-Load Module. Information in this bulletin is written primarily for system user and maintenance personnel with backgrounds in digital systems. Refer to Reference bulletin R1240 for a general description of this module and to SUE General System Bulletins for background information.

SUE 1240 AUTO-LOAD

MAINTENANCE BULLETIN M1240

ALD

INTRODUCTION

This bulletin describes the logic functions of the SUE 1240 Auto-Load (ALD) module as shown in the functional block diagram, figure 1. In the figure, INFIBUS interface is shown on the left and remote control of Auto-Load module and ROM numbers on the right. Figure 1 is keyed to the Auto-Load logic diagrams LD sheets 1 through 9. The respective logic diagram sheet number is shown in the upper left-hand corner of each block in the figure. In general, the logic diagrams are described as they pertain to a ROM Access Cycle, a Direct Data Transfer (DDT) cycle, and a CPU Interrupt.

ROM ACCESS CYCLE

The 1240 Auto-Load module operates in the slave mode during a ROM access cycle. Functional timing is shown in figure 2.

ADDRESS RECOGNITION AND ROM SELECTION (LD Sheets 2 and 9)

The address from the INFIBUS is received through the address bus drivers/ receivers shown on LD sheet 9. Address bits A08A through A12A (LD sheet 2) are compared to the address bits encoded in address program plug, J2. The J2 input is either pulled high or low depending on the assigned Auto-Load starting address. For the LEC standard Auto-Load starting address, FB00, the address plug inputs of A08A, A09A, A11A, and A12A are pulled high, and the input compared to bit A10A is pulled low. Address bits A12A through A15A must be high for any auto-load address. The comparators are strobed by the system

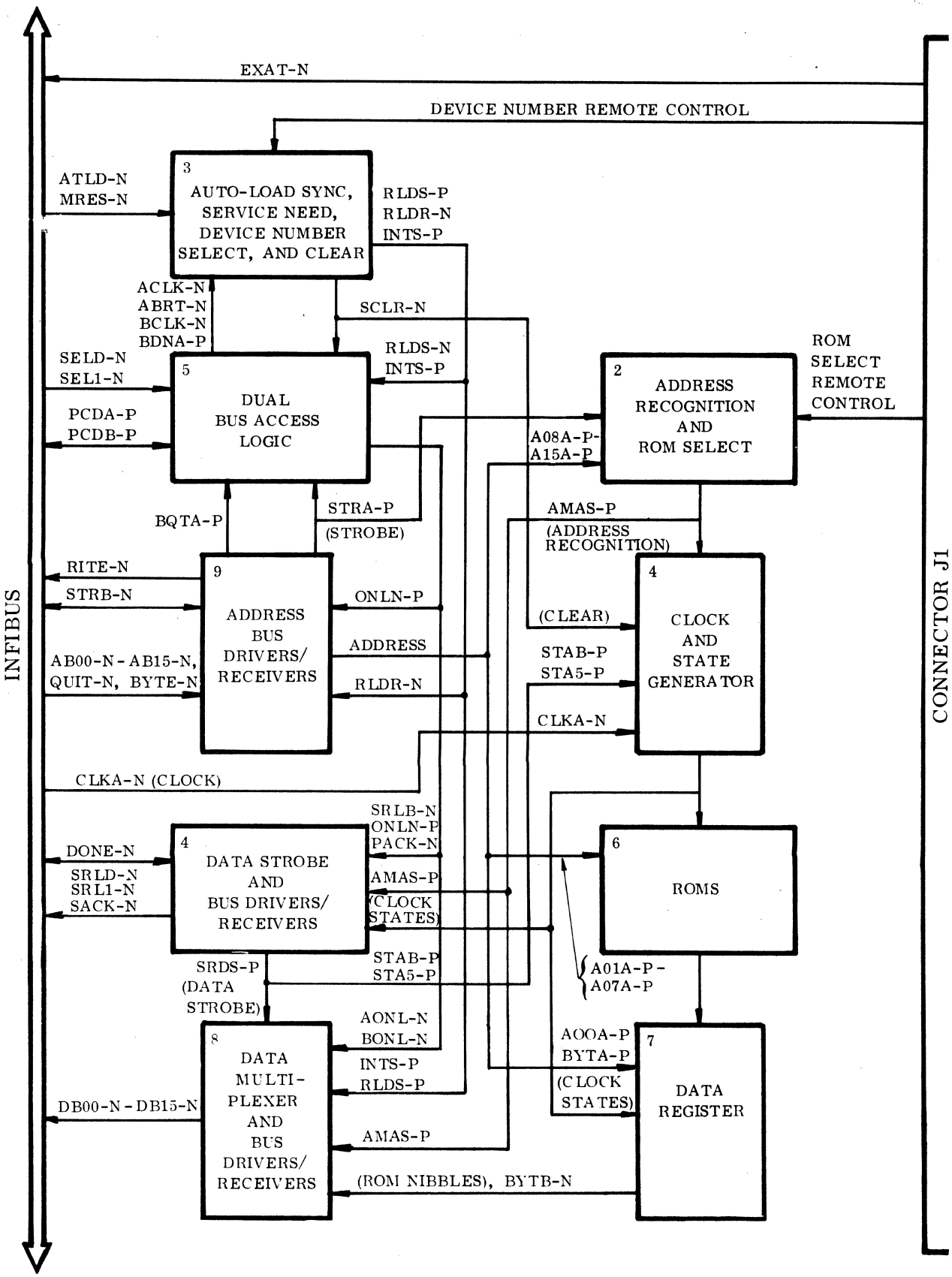


Figure 1. 1240 Auto-Load Functional Block Diagram

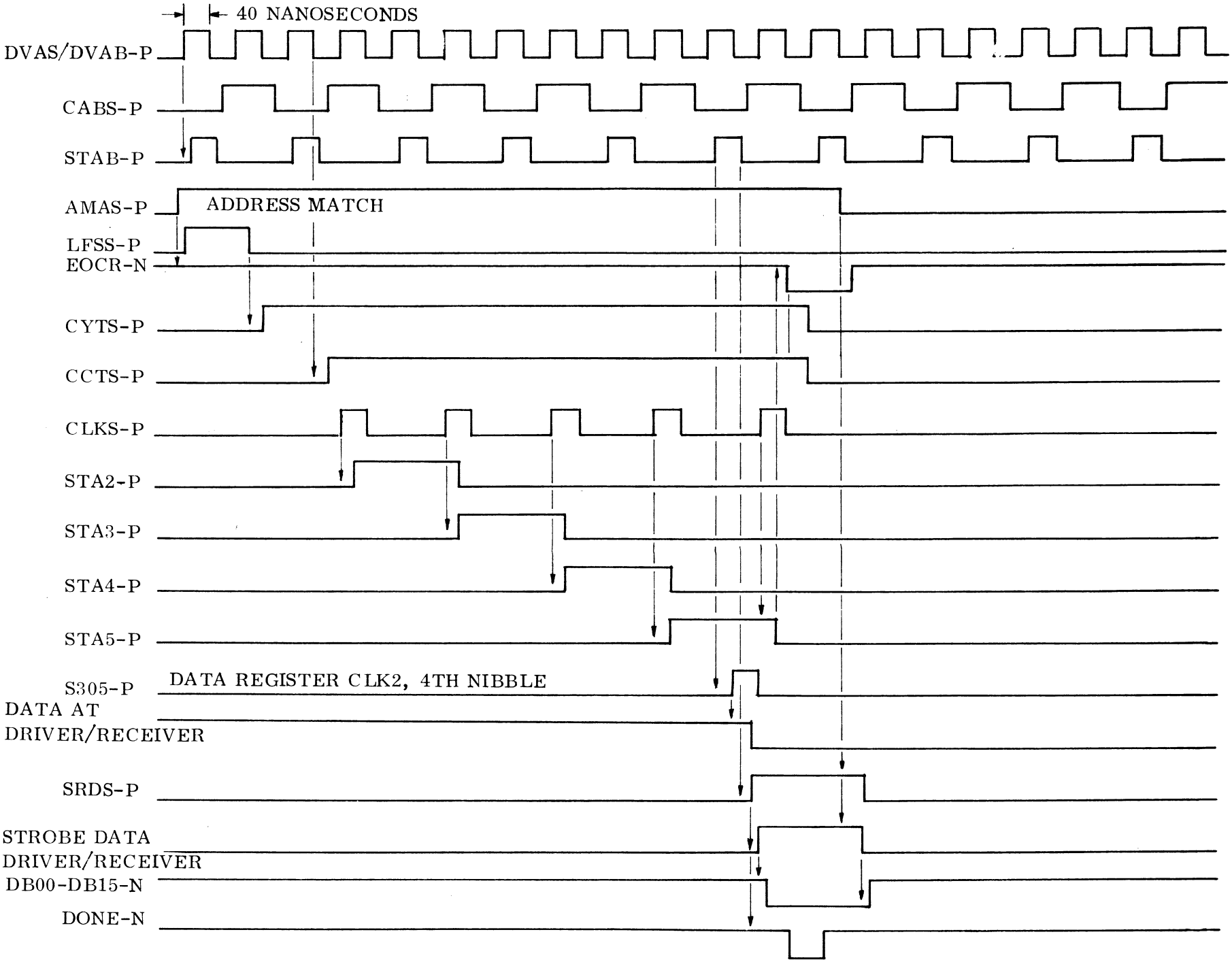


Figure 2. ROM Access Cycle

strobe through gate STRC after the address lines become stable. Normally low, a comparator output goes high when its two inputs are either both high or both low.

An address match sets flip-flop AMA and performs the following functions:

a. Signal AMAS-P enables one input of the ROM select gates ERM1 through ERM4. The other input of only one of these gates are enabled by switches SW1 and SW2.

b. Signal AMAR-N triggers 100 μsec LFS one-shot (LD sheet 4), which loads the first state of a five state shift register (STA1-P through STA5-P).

Absence of Address Match on strobe (STRB-N) negated, causes AMAS-P to be low which disables data strobe gates SRDA and EDLB (LD sheet 8). This condition:

a. Clears SRD flip-flop (LD sheet 4) to inhibit DONE-N, and

b. Clears EOC flip-flop to enable initiation of ROM access and shift register states through flip-flops CYT and CGT.

CLOCK AND STATE GENERATOR (LD Sheet 4)

When address match is detected, one-shot LFS is triggered, and its leading edge loads the first state of the shift register. The trailing edge of LFSS-P sets flip-flop CYT. This sets clock cycle time flip-flop CCT at the trailing edge of clock DVAB. Flip-flop CCT remains set, and enables the clock input of the shift register through gate CLKS, until the trailing edge of the last state (STA5-P) when end of cycle flip-flop (EOC) is set.

State B clock, STAB-P, is always present and is generated from the system 25 MHz clock CLKA-P. The clock rate at the output of gate DVAB is 6.25 or 12.5 MHz, depending on whether program jumper J4 at the input of gate SEAB is installed. STAB-P clock performs the following functions:

a. Sets strobe ROM data flip-flop (SRD) through gates SSRM during state five (LD sheet 4).

b. Clocks the data register during states two through five (LD sheet 7). In the word mode, the first nibble of the ROM is clocked into the data register through gate ST2W during state 2 and clock B; the second nibble through gate ST3W during state 3 and clock B; the third nibble through gates ST4B, ST4W and S204 during state 4 and clock B; and the fourth nibble through gates SSRM, ST5W and S305 during state 5 and clock B.

If byte signal BYTE-N is low, indicating byte mode, and address bit AB00-N is low (ONE), only the last two nibbles of the ROM are held. The third nibble is clocked into data register N300-N303 through gates ST4B, S4RB and S204 during clock B of state 4. The fourth nibble is clocked into data register N400-N404 through gates SSRM, SERB and S305 during clock B of state 5. If address bit AB00-N is high (ZERO), the first two nibbles are clocked into data register N300-N303 and N400-N403.

ROMS (LD Sheet 6)

Enable input, E1, on one of the four ROMS is always enabled by the ROM select switches and logic (LS sheet 2). Enable input, E2, is activated by address bit A07-P to allow use of 512 XY-bit (max) LSI ROM. ROM word addresses A2 through A7 are the inverted INFIBUS addresses A01A through A06A. Address bit A00A is not used for ROM addressing. ROM nibble addresses A0 and A1 are generated internally by states 2, 3, 4, and 5 as shown in table 1.

Table 1. ROM Nibble Address Generation

Nibble	Address A_1	Address A_0	State			
			2	3	4	5
1	0	0	1	0	0	0
2	0	1	0	1	0	0
3	1	0	0	0	1	0
4	1	1	0	0	0	1

DATA MULTIPLEXER AND DRIVERS/RECEIVERS (LD Sheet 8)

In word mode, data bits DB15-DB08 are asserted by the Auto-Load module from ROM nibbles one and two applied to data multiplexer U59 and U69. The multiplexers are selected by RLDS-P low, indicating absence of Direct Data Transfer. The drivers/receivers of these bits are strobed by gates SRSA or EDLB if

a. Strobe ROM Data flip-flop, SRD, is set (LD sheet 4)

b. BYTB-N is high indicating word mode data bits DB07-DB04 are ransmitted on the INFIBUS from ROM nibble three when SRD flip-flop is set. Data bits DB03-DB00 are transmitted from ROM nibble four. They are selected by the multiplexer when INTS-P is low indicating absence of CPU interrupt cycle and are strobed onto the INFIBUS when SRD flip-flop is set.

DIRECT DATA TRANSFER (DDT) (LD Sheet 3)

Direct Data Transfer timing is shown in figure 3. When the trailing edge of Auto-Load signal ATLO-N is sensed, flip-flop ALT sets to trigger a 150 ms one-shot ALD. At the end of this time, the Auto-Load lockout flip-flop (ALL) sets to disable gate ATLT from any further response to Auto-Load signals, until Master Reset is asserted. The reset side of flip-flop ALL sets DDT service need flip-flop, RLD, which serves the following functions:

a. Sets the Ready flip-flop of the DDT part of the Dual Bus Access Logic (LD sheet 5). This generates SRLA to transmit Service Request, SRLD, (LD sheet 4); blocks Precedence Chain Pulse, PCDB-P; and enables setting the Select flip-flop when signal SELD-N is received. When the Select flip-flop is set, Acknowledge signal SACK-N (LD sheet 9) is transmitted on the INFIBUS through gate PACK and the driver/receiver.

b. Enables the B inputs of the data multiplexers (LD sheet 8), bits DB15-DB08. Bits DB07-DB00 are disabled at the strobe of the driver/receiver where gates RDSA and RDSB outputs are low. The starting address of the Auto-Load is transmitted on the INFIBUS data lines and data bits DB12-DB08 can have any value depending on the program jumpers (J3) installed on B inputs of the corresponding multiplexers.

c. Enable driver/receiver (LD sheet 9) of memory address bits AB01 and AB02 (0006) where the Auto-Load starting address is to be loaded. Enable driver/receiver inputs of RITE-N signal. The strobe input of the above driver/receiver for address 0, 1 and RITE-N is enabled when the output of gate ONLN (LD sheet 5) goes high.

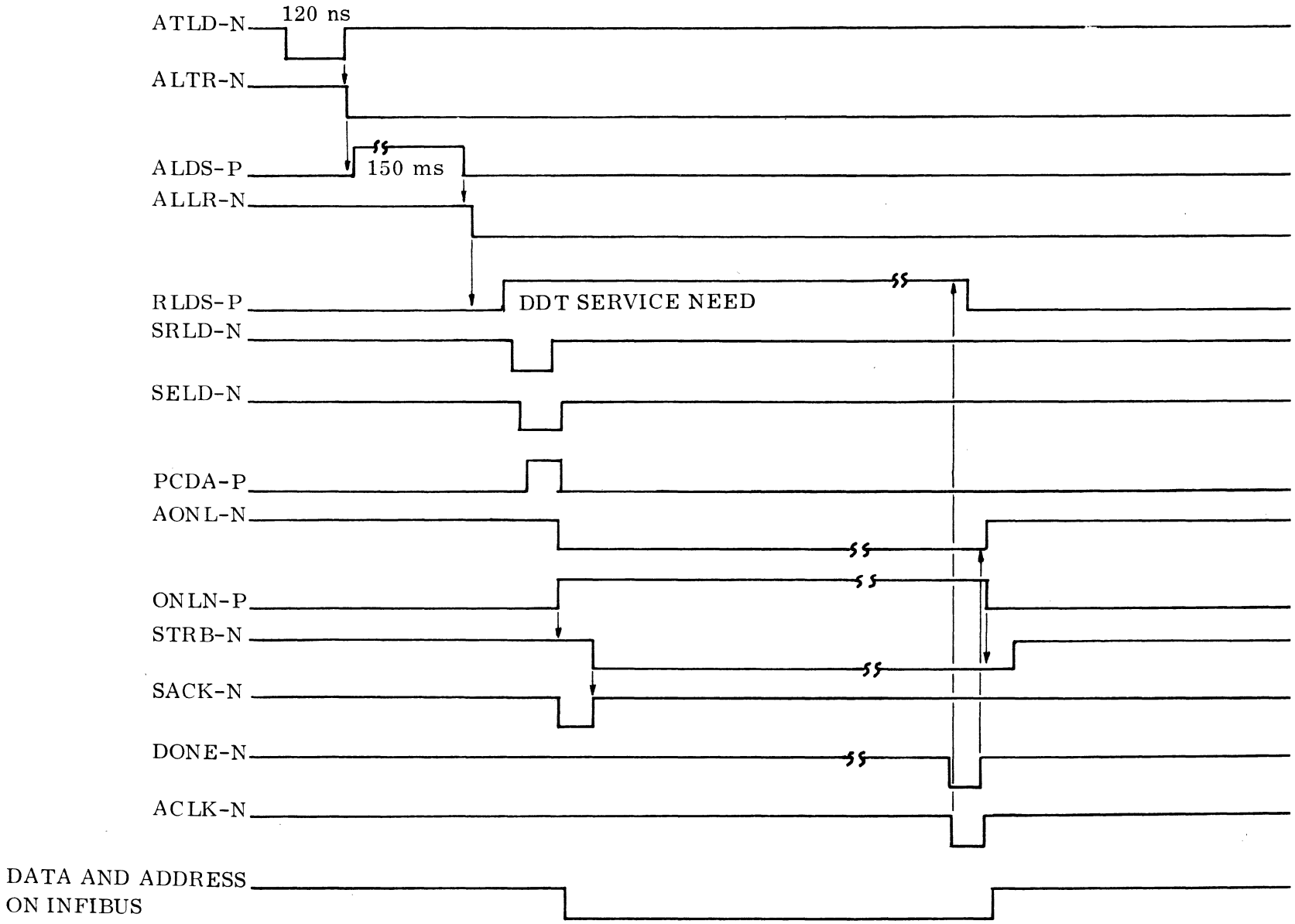


Figure 3. DDT Cycle

When the On-Line flip-flop of the DDT part of the Dual Bus Access logic is set, the output of gate AONL (LD sheet 5) goes low to enable the strobe input of the driver/receiver of data bits DB15-DB08 (LD sheet 8).

CPU INTERRUPT

When DONE-N is received from memory, ACLK-N (LD sheet 5) goes low to clear the DDT Service Need flip-flop RLD (LD sheet 3), which in turn, sets CPU Interrupt Service Need flip-flop, INT. This enables generation of SRL1-N through the CPU interrupt part of the Dual Bus Access Logic (LD sheet 5) and the drivers/receivers (LD sheet 4) and enables the B inputs of the data multiplexer (LD sheet 8) bits DB03-DB00. The device number, as selected by switches S4 and S3 (LD sheet 3) is transmitted on the INFIBUS data bits DB01-DB02. The strobe input of the drivers/receivers for bits DB15-DB08 are disabled.

DEVICE AND ROM NUMBER (LD Sheets 2 and 3)

Switches S1 and S2 are used to select one of four possible ROMs on the Auto-Load circuit card. Switches S3 and S4 select the device number assigned to the Auto-Load modules as indicated in table 2. All four of the switches have open contacts available at connector J1 for remote control.

DRAWINGS AND PARTS LISTS

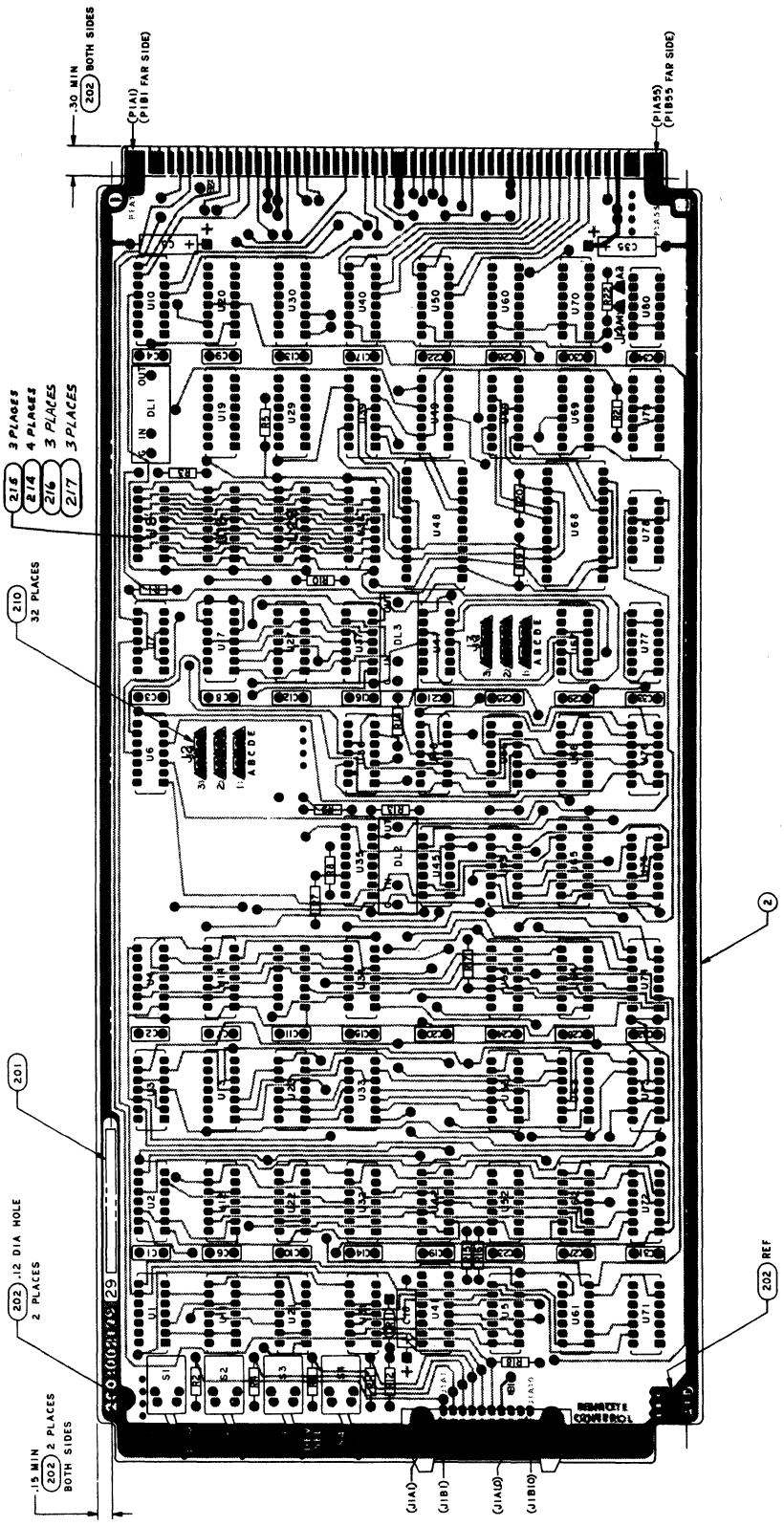
The SUE 1240 Auto-Load assembly drawing, logic diagrams, and parts lists included in this bulletin are listed below:

Title	Drawing Number	Sheet
SUE 1240 Auto-Load Circuit Card Assembly (ALD)	2001002129	1
SUE 1240 Auto-Load Logic Diagram (ALD)	LD2001002129-1	1 thru 9
Sue 1240 Auto-Load Parts List (ALD)	PL2001002129	2 thru 6

Table 2. SUE Auto-Load Modules and ROM Selection

Model	Auto-Load Description	ROM Part Numbers	ROM Numbers	ROM Location On Circuit Card Assembly	Selection Switches*				Device Number
					ROM		Device		
					S1	S2	S3	S4	
1241	Auto-Load, Teletypewriter	1005000796-13	1	U38	D	D	D	D	0000
1241	Auto-Load, Paper Tape	1005000796-13	1	U38	D	D	U	D	0002
1242	Auto-Load, Disk (Fixed)	1005000796-25	2	U8	D	U	D	D	0000
1242	Auto-Load, Disk (Removable)	1005000796-25	2	U8	D	U	U	D	0002
1243	Auto-Load, Cards	1005000796-37	3	U18	U	D	D	D	0000
1244	Auto-Load, Magnetic Tape (0)	1005000796-38	4	U28	U	U	D	D	0000
1244	Auto-Load, Magnetic Tape (1)	1005000796-38	4	U28	U	U	D	U	0004
1244	Auto-Load, Magnetic Tape (2)	1005000796-38	4	U28	U	U	U	D	0002
1244	Auto-Load, Magnetic Tape (3)	1005000796-38	4	U28	U	U	U	U	0006
1251	Auto-Load, Paper Tape/Disk	1005000796-13, -25	1, 2	U38, U8	— As Above —				
1252	Auto-Load, Paper Tape/Cards	1005000796-13, -37	1, 3	U38, U18	— As Above —				
1253	Auto-Load, Disk/Cards	1005000796-25, -37	2, 3	U8, U18	— As Above —				
1261	Auto-Load, Paper Tape/Disk/ Cards	1005000796-13, -25, -37	1, 2, 3	U38, U8, U18	— As Above —				
1271	Auto-Load, Paper Tape/Disk/ Cards/Magnetic Tape	1005000796-13, -25, -37, -38	1, 2, 3, 4	U38, U8, U18, U28	— As Above —				

*U - Up position, D - Down position

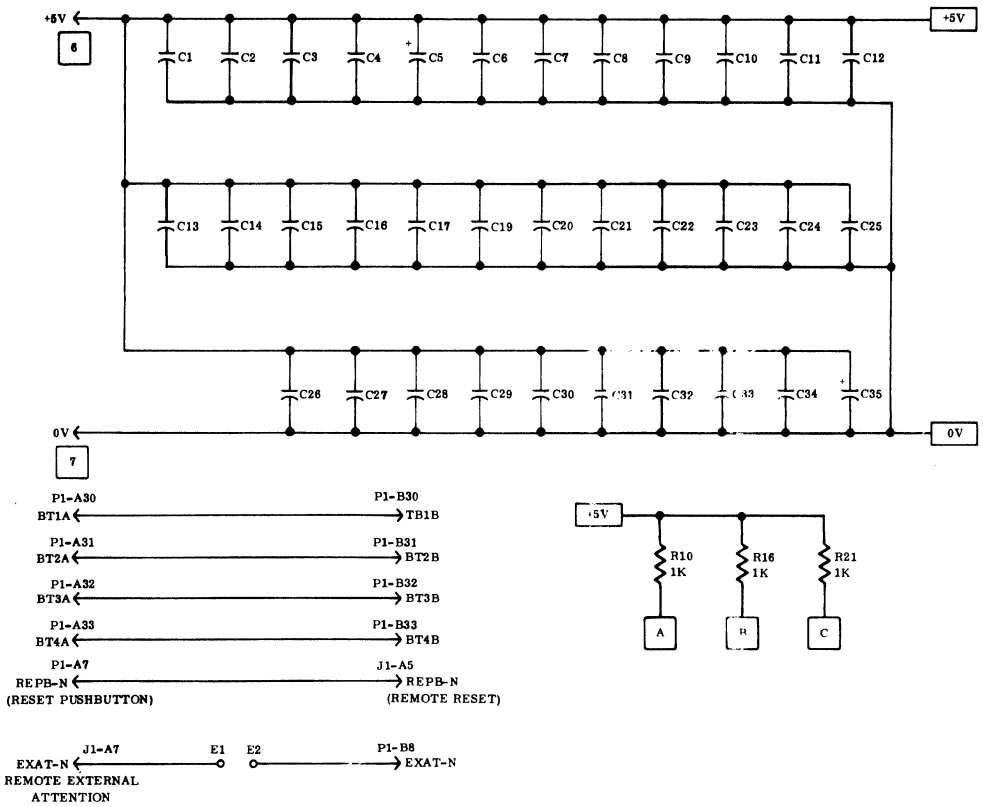


SUE 1240 Auto-Load Circuit Card Assembly (ALD)
2001002129, Rev. G, Sheet 1

NOTES:

1. ALL RESISTORS ARE IN OHMS ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1 µf, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33µf, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED. FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200-1).
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (14 PIN ICP) PIN 7 0V, PIN 14 +5V, EXCEPT T73 AND H103 PIN 11 0V, PIN 4 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V EXCEPT BDR PIN 7, 8 0V, PIN 16 +5V, T96 PIN 12 0V, PIN 5 +5V; (24 PIN ICP) PIN 7 0V, PIN 24 +5V.
6. +5V PINS ARE P1-A16, A28, A29, A51, B16, B28, B29 AND B51.
7. 0V PINS ARE P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55, J1-B1, B2, B3, B4, B5, B6 AND B7.

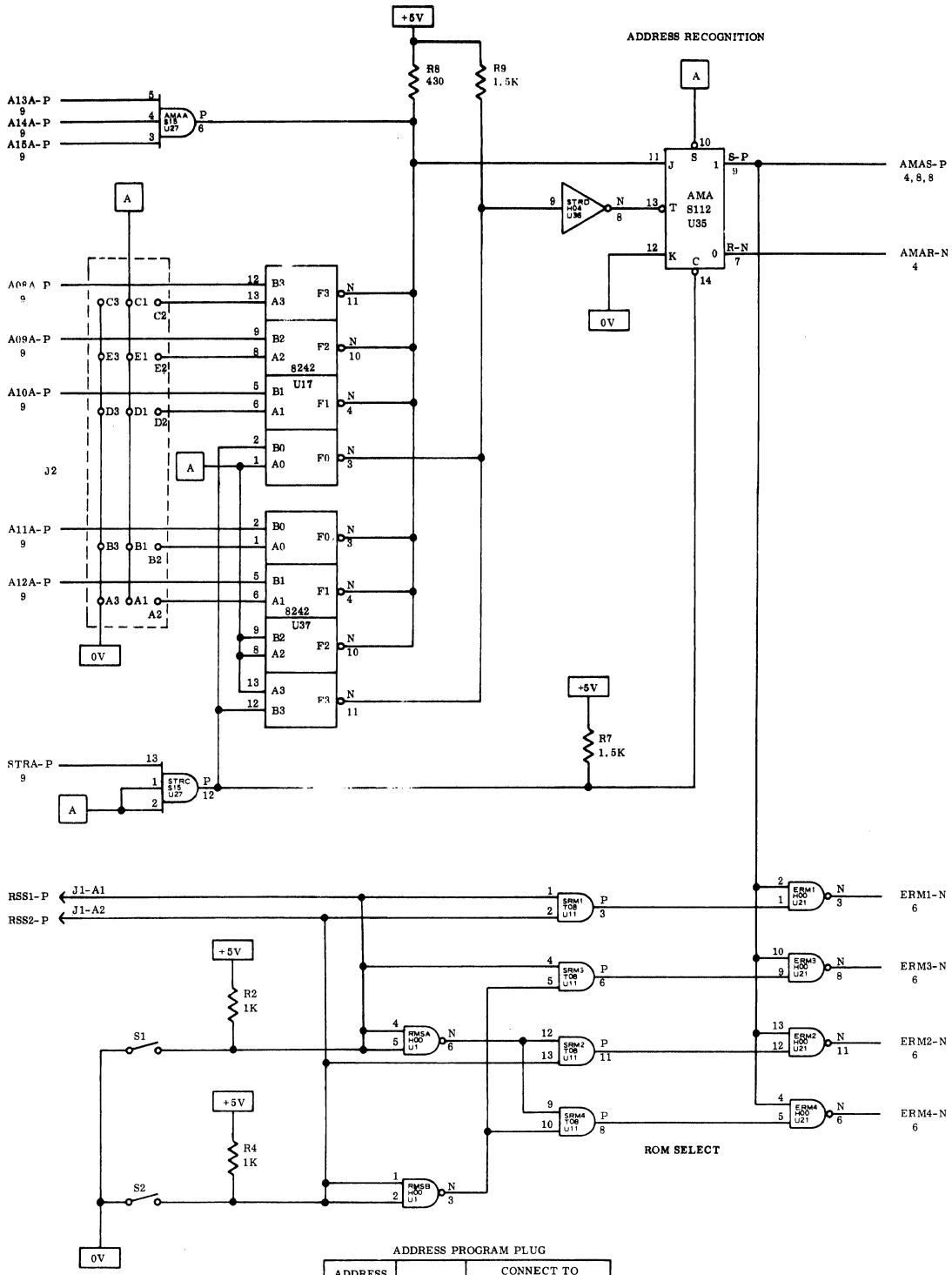
ALD



SUE 1240 Auto-Load Logic Diagram (ALD)
LD2001002129-1, Rev. C, Sheet 1 of 9

KEY SOURCE LOGIC DEFINITIONS (LD Sheet 2)

AMAS-P/AMAR-N	Address recognized, asserted when address bits A08A-P through A12A-P match the device number wired on address program plug J2.
RSS1-P, RSS2-P	Remote control ROM select lines
ERM1-N thru ERM4-N	Enable ROM signals for ROM 1 through ROM 4 when Auto-Load address is recognized. Only one ROM can be enabled at one time by setting switches S1 and S2.



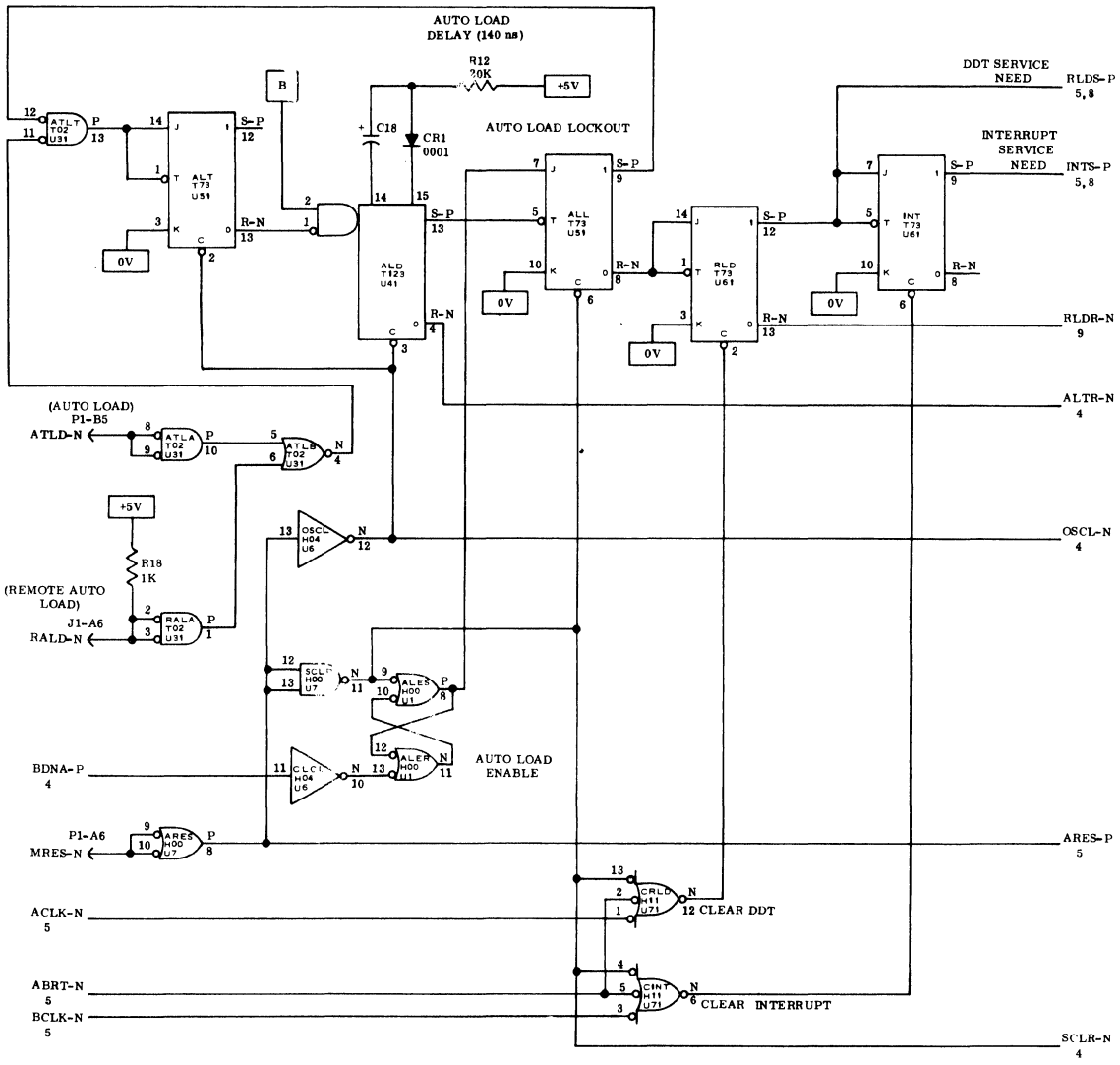
ADDRESS PROGRAM PLUG

ADDRESS BIT	FROM	CONNECT TO	
		BINARY 1	BINARY 0
8	J2-C2	J2-C1	J2-C3
9	J2-E2	J2-E1	J2-E3
10	J2-D2	J2-D1	J2-D3
11	J2-B2	J2-B1	J2-B3
12	J2-A2	J2-A1	J2-A3

SUE 1240 Auto-Load Logic Diagram (ALD)
LD2001002129-1, Rev. C, Sheet 2 of 9

KEY SOURCE LOGIC DEFINITIONS (LD Sheet 3)

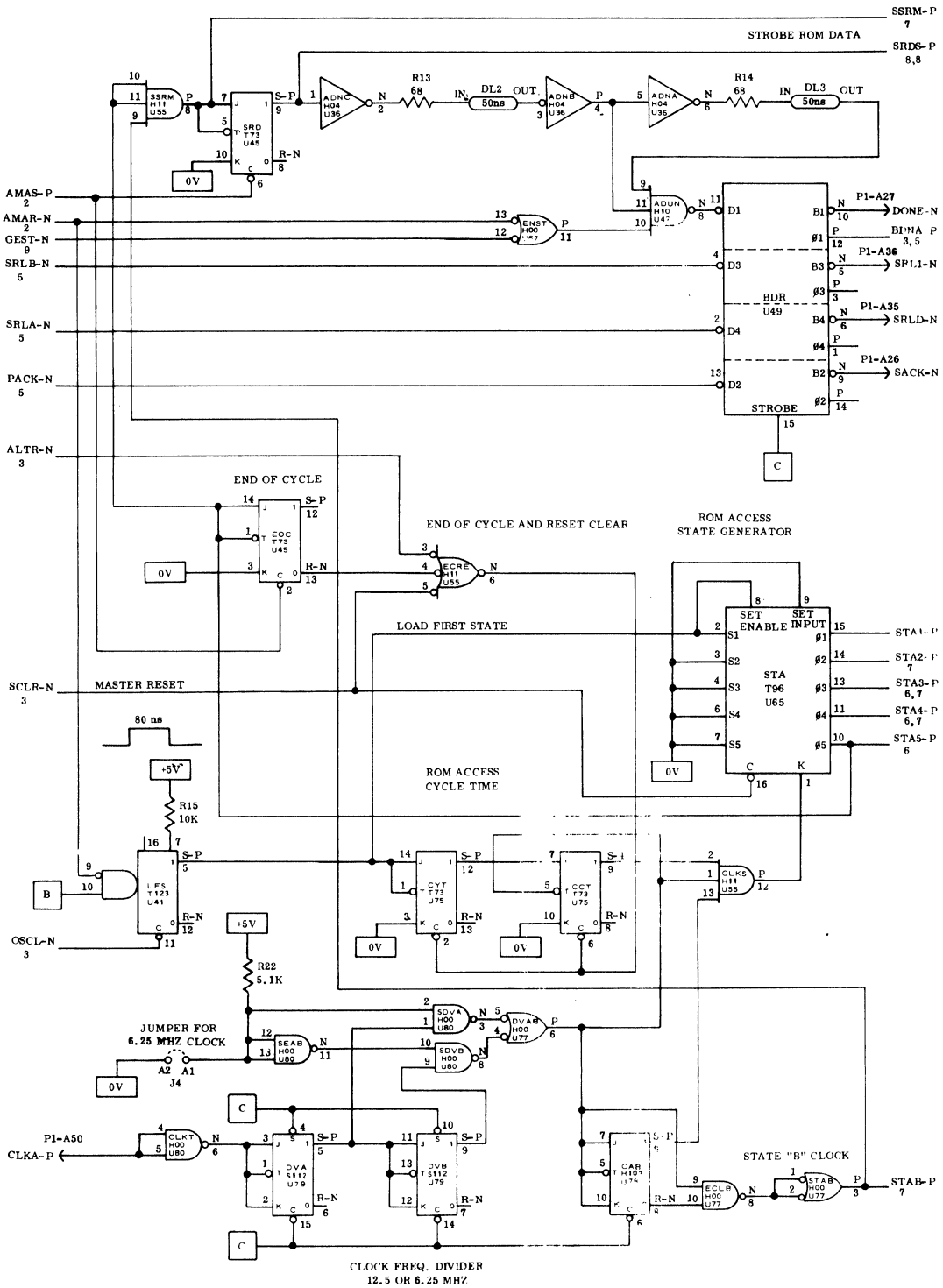
RLDS-P, RLDR-N	Direct Data Transfer (DDT) Service Need, enables the DDT part of the Dual Bus Access Logic; the B multiplexer B programmed inputs (start address) of data bits DB15 through DB08; and asserts address 0006, and RITE-N on the INFIBUS.
INTS-P	CPU Interrupt Service Need, enables the CPU interrupt part of the Dual Bus Access Logic and the multiplexer B inputs (device number) of data bits DB03 through DB00.
ALTR-N	Auto-Load delay of 150 ms from the time Auto-Load signal is detected, used as an initial disable of ROM access.
OSCL-N, ARES-P, SCLR-N	Master reset signals.
DNS3-P, DNS4-P	Device number select, remote control



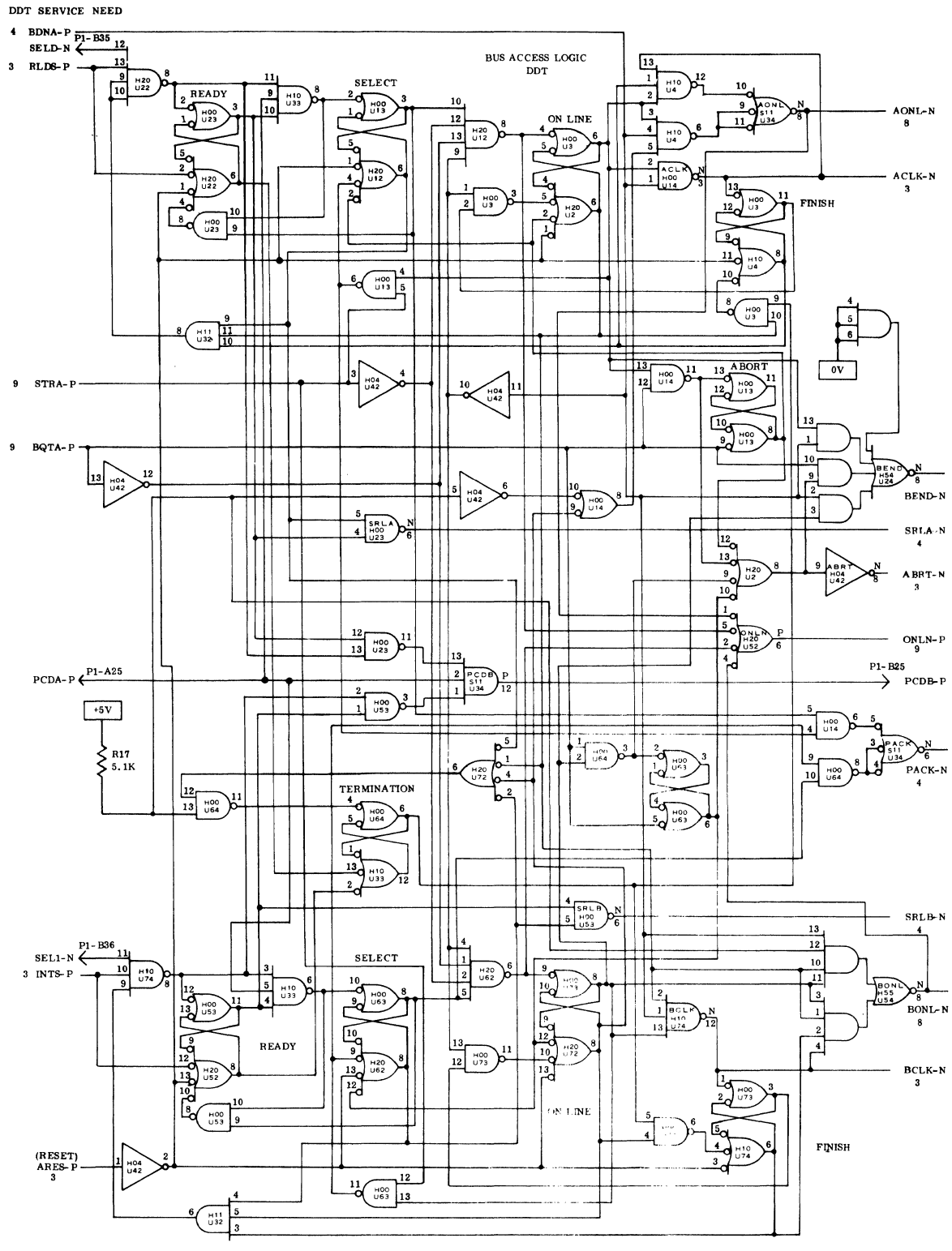
SUE 1240 Auto-Load Logic Diagram (ALD)
LD2001002129-1, Rev. C, Sheet 3 of 9

KEY SOURCE LOGIC DEFINITIONS (LD Sheet 4)

SSRM-P	Clocked last state to store the last nibble (4), strobe it into the drivers/receivers and generate DONE-N.
SRDS-P	Strobe ROM data onto the INFIBUS.
STA2-P thru STA5-P	ROM access states. The first nibble is stored in the data register during STA2-P and the fourth nibble during STA5-P.
STAB-P	6.25 MHz clock used with STA2-P through STA5-P for timing.



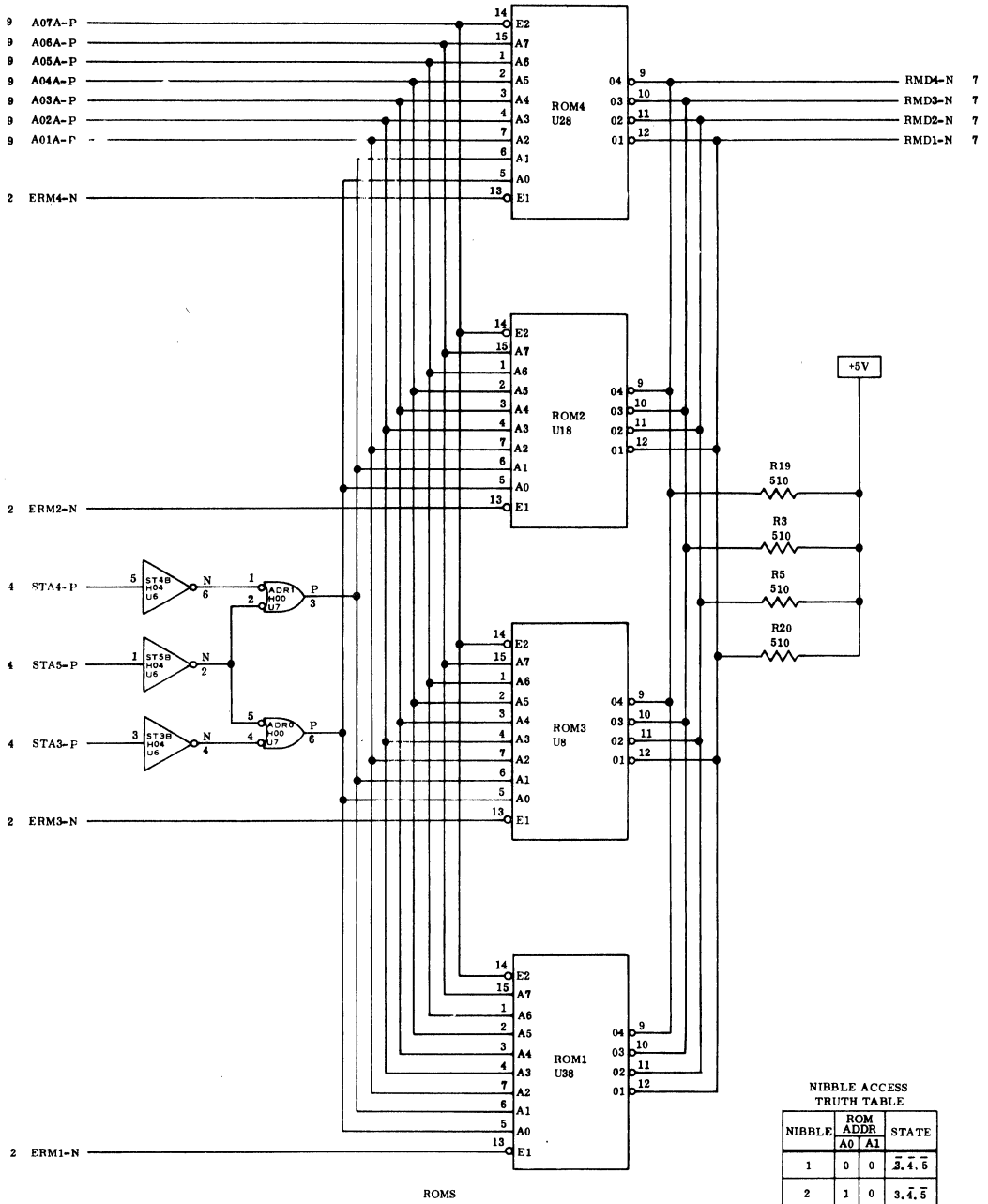
SUE 1240 Auto-Load Logic Diagram (ALD)
LD2001002129-1, Rev. C, Sheet 4 of 9



SUE 1240 Auto-Load Logic Diagram (ALD)
LD2001002129-1, Rev. C, Sheet 5 of 9

KEY SOURCE LOGIC DEFINITIONS (LD Sheet 6)

RMD1-N thru RMD4-N	OR-tied outputs of the four possible ROM output data.

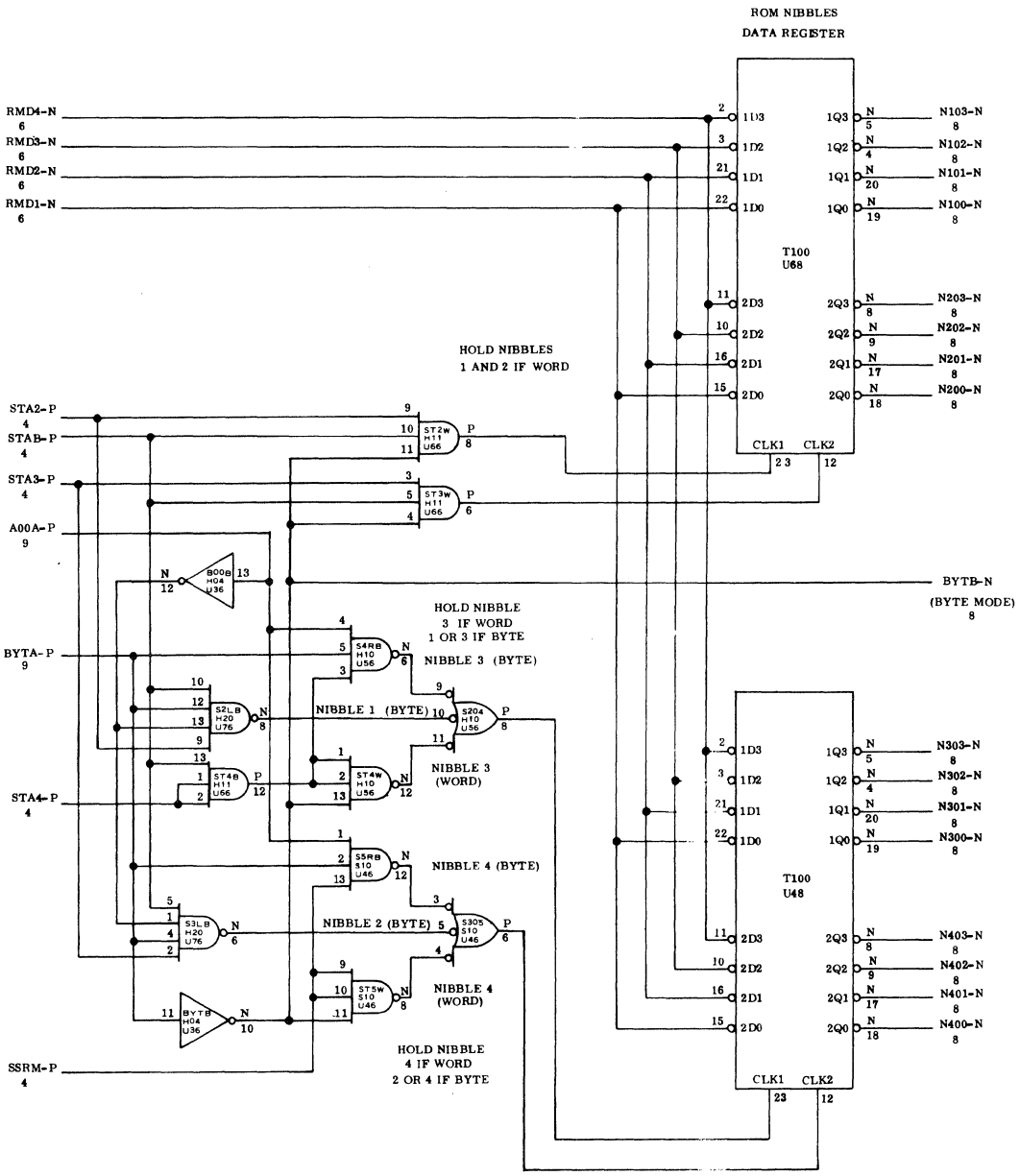


NIBBLE ACCESS TRUTH TABLE

NIBBLE	ROM ADDR A0	ROM ADDR A1	STATE
1	0	0	$\bar{3}.\bar{4}.\bar{5}$
2	1	0	$3.\bar{4}.\bar{5}$
3	0	1	$\bar{3}.4.\bar{5}$
4	1	1	x. x. 5

KEY SOURCE LOGIC DEFINITIONS (LD Sheet 7)

N100-N thru N103-N	Data register output of the first nibble (data bits DB15-DB12) in word mode only.
N200-N thru N203-N	Data register output of the second nibble (data bits DB11-DB08) in word mode only.
N300-N thru N303-N	Data register output of the third nibble (data bits DB07-DB04 in word mode; or either the first or third nibble in byte mode.
N400-N thru N403-N	Data register output of the fourth nibble (data bits DB03-DB00) in word mode; or either the second or fourth nibble in byte mode.



SUE 1240 Auto-Load Logic Diagram (ALD)
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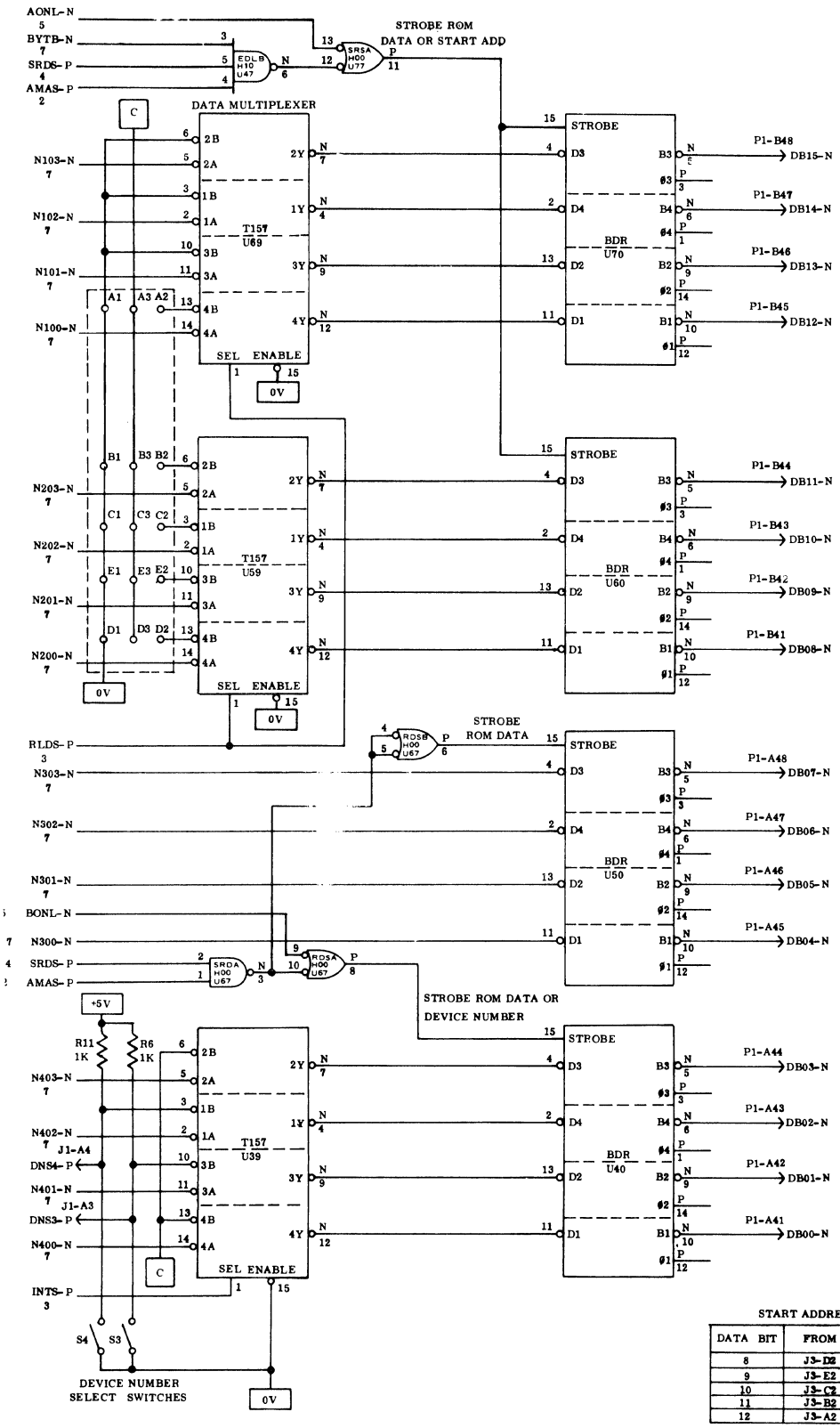

START ADDRESS PROGRAM PLUG.

DATA BIT	FROM	CONNECT TO	
		BINARY 1	BINARY 0
8	J3-D2	J3-D1	J3-D3
9	J3-E2	J3-E1	J3-E3
10	J3-C2	J3-C1	J3-C3
11	J3-B2	J3-B1	J3-B3
12	J3-A2	J3-A1	J3-A3

SUE 1240 Auto-Load Logic Diagram (ALD)
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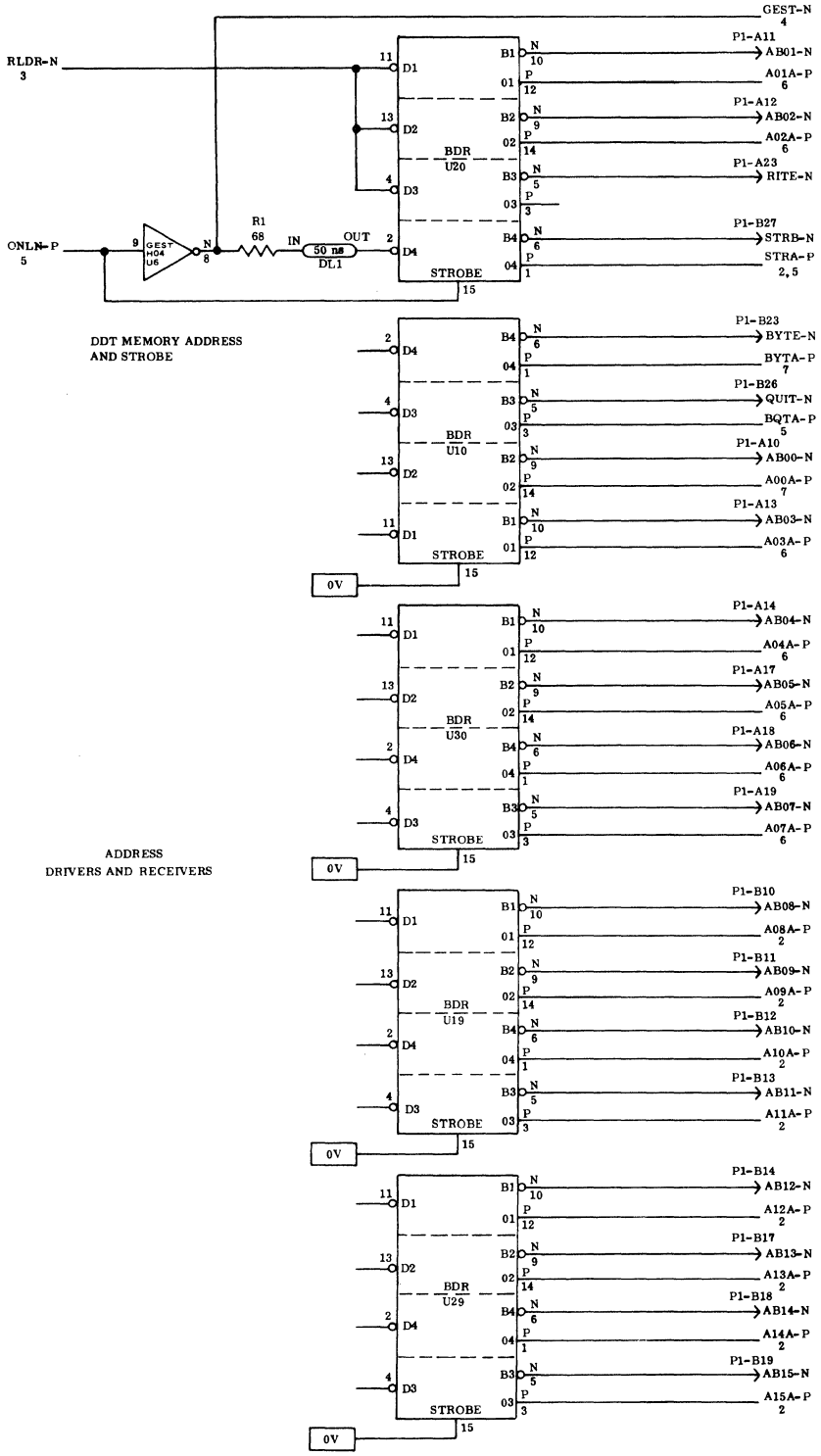


SUE 1240 Auto-Load Logic Diagram (ALD)
LD2001002129-1, Rev. C, Sheet 9 of 9

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002129-1		ALD-CKT CARD ASSY		USED ON SUE 1240	1
002		001	0001		1001004722-1		PRINTED WRG BD, ALD			2
003		000								3
004		000								4
005		000								5
006	F	032	0001		8001300101-1		CAPACITOR		C1 THRU C4, C6 THRU C17, C19 THRU C34 .25 IS	6
007		000								7
008		003	0001		8001300311-2		CAPACITOR		C5,18,35 .8 IS	8
009		000								9
010		000								10
011	F	014	0001		8001800042-1		ICP		U1,3,7,13,14,21, 23,53,63.64,67, 73,77,80 (74H00)	11
012	F	005	0001		8001800046-1		ICP		U4,33,47,56,74 (74H10)	12
013	F	001	0001		8001800074-1		ICP		U31 (7402)	13
014	F	002	0001		8001803148-1		ICP		U48,68 (74100)	14
015	F	003	0001		8001800044-1		ICP		U6,36,42 (74H04)	15
016	F	007	0001		8001800048-1		ICP		U2,12,22,52,62, 72,76 (74H20)	16
017	F	001	0001		8001803126-1		ICP		U11 (7408)	17
018	F	001	0001		8001803204-1		ICP		U27 (74S15)	18
019		000								19
020	F	004	0001		8001800098-1		ICP		U45,51,61,75 (7473)	20
021	F	001	0001		8001800058-1		ICP		U54 (74H55)	21
022	F	004	0001		8001800047-1		ICP		U32,55,66,71 (74H11)	22
023	F	001	0001		8001803155-1		ICP		U41 (74123)	23
024		000								24
025		000								25
026	F	001	0001		8001800069-1		ICP		U78 (74H103)	26
027	F	001	0001		8001800113-1		ICP		U65 (7496)	27
028	F	003	0001		8001803169-1		ICP		U39,59,69(74157)	28
029		002	0001		N8242A	18324	ICP	SIGNETICS	U17,37	29
030	F	003	0001		8001600008-1		DELAY LINE, FIXED		DL1,2,3	30
031		000								31
032		001	0001		3428-1002	26066	CONNECTOR, RT ANGLE	3M CO	J1 20 CONTACT RCPT	32
033		000								33

ALD

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
034	F	001	0001		8001803203-1		ICP		U34 (74S11)	34
035	F	001	0001		8001803202-1		ICP		U46 (74S10)	35
036		010	0001		8001800123-1		ICP		U10,19,20,29,30, 40,49,50,60,70 (BOR)	36
037	F	002	0001		8001803212-1		ICP		U35,79 (74S112)	37
038		004	0001		T8201	81640	TOGGLE SWITCH	SINGER CONTROL	S1 THRU S4	38
039		003	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R1,13,14 .5 IS	39
040		008	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R2,4,6,10,11,16, 18,21 .5 IS	40
041		001	0001		RL07S431G		RESISTOR	MIL-R-22684/1	R8 .5 IS	41
042		004	0001		RL07S511G		RESISTOR	MIL-R-22684/1	R3,5,19,20 .5 IS	42
043		002	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R7,9 .5 IS	43
044		002	0001		RL07S512G		RESISTOR	MIL-R-22684/1	R17,22 .5 IS	44
045		000								45
046		001	0001		RL07S103G		RESISTOR	MIL-R-22684/1	R15 .5 IS	46
047		001	0001		RL07S203G		RESISTOR	MIL-R-22684/1	R12 .5 IS	47
048	E	001	0001		8001100001-1		DIODE		CR1 .5 IS	48
049	F	032	0001		1005000764-1		PIN, TERMINAL		J2,3,4 NOTE 210	49
050		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		50
		REF	0001		LD2001002129-1		LOGIC DIAGRAM			51

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2001002129-2		ALD-CKT CARD ASSY		USED ON SUE 1241	1
002	000								2
003	001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004	001	0001		1005000796-13		ICP (ROM)		U38	4
								PL2001002129-3	G
001	000	0001		2001002129-3		ALD-CKT CARD ASSY		USED ON SUE 1242	1
002	000								2
003	001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004	001	0001		1005000796-25		ICP (ROM)		U8	4
								PL2001002129-4	G
001	000	0001		2001002129-4		ALD-CKT CARD ASSY		USED ON SUE 1243	1
002	000								2
003	001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004	001	0001		1005000796-37		ICP (ROM)		U18	4
								PL2001002129-5	G
001	000	0001		2001002129-5		ALD-CKT CARD ASSY		USED ON SUE 1244	1
002	000								2
003	001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004	001	0001		1005000796-38		ICP (ROM)		U28	4
								PL2001002129-10	G
001	000	0001		2001002129-10		ALD-CKT CARD ASSY		USED ON SUE 1251	1
002	000								2
003	001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004	001	0001		1005000796-13		ICP (ROM)		U38	4
005	001	0001		1005000796-25		ICP (ROM)		U8	5
								PL2001002129-11	G
001	000	0001		2001002129-11		ALD-CKT CARD ASSY		USED ON SUE 1252	1
002	000								2
003	001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004	001	0001		1005000796-13		ICP (ROM)		U38	4
005	001	0001		1005000796-37		ICP (ROM)		U18	5

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002129-12		ALD-CKT CARD ASSY		USED ON SUE 1253	1
002		000								2
003		001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004		001	0001		1005000796-25		ICP (ROM)		U8	4
005		001	0001		1005000796-37		ICP (ROM)		U18	5
									PL2001002129-20	G
001		000	0001		2001002129-20		ALD-CKT CARD ASSY		USED ON SUE 1261	1
002		000								2
003		001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004		001	0001		1005000796-13		ICP (ROM)		U38	4
005		001	0001		1005000796-25		ICP (ROM)		U8	5
006		001	0001		1005000796-37		ICP (ROM)		U18	6
									PL2001002129-30	G
001		000	0001		2001002129-30		ALD-CKT CARD ASSY		USED ON SUE 1271	1
002		000								2
003		001	0001		2001002129-1		ALD-CKT CARD ASSY			3
004		001	0001		1005000796-13		ICP (ROM)		U38	4
005		001	0001		1005000796-25		ICP (ROM)		U8	5
006		001	0001		1005000796-37		ICP (ROM)		U18	6
007		001	0001		1005000796-38		ICP (ROM)		U28	7

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARKING (IDENTIFY).			201
202		REF	0001				AREA TO BE FREE OF SOLDER.			202
203		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			203
204		REF	0001				COMPONENT HEIGHT .395 MAX.			204
205		REF	0001				PROTRUSION SIDE 2 .070 MAX. LEADS TO BE VISIBLE THRU SOLDER.			205
206		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010 INCH/INCH IN GENERAL AREA AND .005 INCH/INCH IN CONNECTOR AREA.			206
207		REF	0001				SQUARE PAD DENOTES CATHODE END (STRIPE) OF DIODE, OR POSITIVE (+) END OF CAPACITOR.			207
208		REF	0001				RECTANGULAR PAD AND DOT OR SLOTTED END OF ICP DENOTES PIN 1.			208
209		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			209
210		REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			210
211		000								211
212		000								212
213		000								213
214		REF	0001				ON -1 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING UNUSED I.C. PATTERNS ON SOLDER SIDE OF BOARD PRIOR TO SOLDERING: U8, U18, U28 AND U38.			214
215		REF	0001				ON -2 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING UNUSED I.C. PATTERNS ON SOLDER SIDE OF BOARD PRIOR TO SOLDERING: U8, U18 AND U28.			215
216		REF	0001				ON -3 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING I.C. PATTERNS ON SOLDER SIDE OF BOARDS PRIOR TO SOLDERING: U18, U28 AND U38.			216
217		REF	0001				ON -4 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING I.C. PATTERNS ON SOLDER SIDE OF BOARDS PRIOR TO SOLDERING: U8, U28 AND U38.			217
218		REF	0001				ON -5 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING I.C. PATTERNS ON SOLDER SIDE OF BOARDS PRIOR TO SOLDERING: U8, U18 AND U38.			218
219		REF	0001				ON -10 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING I.C. PATTERNS ON SOLDER SIDE OF BOARDS PRIOR TO SOLDERING: U18 AND U28.			219
220		REF	0001				ON -11 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING I.C. PATTERNS ON SOLDER SIDE OF BOARDS PRIOR TO SOLDERING: U8 AND U28.			220
221		REF	0001				ON -12 ASSEMBLY, MASK OFF HOLE PADS OF FOLLOWING I.C. PATTERNS ON SOLDER SIDE OF BOARDS PRIOR TO SOLDERING: U28 AND U38.			221
222		REF	0001				ON -20 ASSEMBLY, MASK OFF HOLE PAD OF FOLLOWING I.C. PATTERN ON SOLDER SIDE OF BOARDS PRIOR TO SOLDERING: U28.			222

ALD

LEC ALD CODE:


```
FE00/    LDA A4 L   F00

FE04/    LDA A5   0000

FE06/    HLT 0000

FE08/    BT ZE, FE12

FE0A/    CMP A5 E 0002

FE0C/    BF EQ, FE5A

FE0E/    LDA A4 L   F820

FE12/    STA A1 X4 X

FE14/    LDA A5 L   FB5E

FE18/    LDA A6 E 0000

FE1A/    JSB A2 X5 X

FE1C/    BT ZE, FE1A

FE1E/    LDA A7 X3 R

FE20/    JSB A2 X5 X

FE22/    LDA A1 X3 R

FE24/    LI L0 A1 0008

FE26/    JSB A2 X5 X
```

```
FE28/    IOR A1 X3 R

FE2A/    CMP A7 L   00FF

FE2E/    BT EQ, FE38

FE30/    JSB A2 X5 X

FE32/    STA B A A3 X1 X

FE34/    SUB A7 E 0001

FE36/    BF ZE, FE30

FE38/    JSB A2 X5 X

FE3A/    SUB A6 X3 R

FE3C/    LI LO A3 0008

FE3E/    LDA A5 X3 R

FE40/    JSB A2   FB5E

FE44/    SUB A6 X3 R

FE46/    IOR A5 X3 R

FE48/    CMP A5 X6 R

FE4A/    BF EQ, FE5A

FE4C/    CMP A7 L   00FF

FE50/    BF EQ, FE14

FE52/    STA A0 X4 X

FE54/    CMP A1 E 0000

FE56/    BT EQ, FE72
```

```
FE58/    JMP X1 X

FE5A/    HLT 0000

FE5C/    BT TR, FE12

FE5E/    LDA A3 L   0011

FE62/    STA A3 X4   0006

FE66/    LDA A3 X4 X

FE68/    BF OD, FE66

FE6A/    LDA A3 X4   0008

FE6E/    ADD A6 X3 R

FE70/    JMP X2 X

FE72/    HLT 0000

FE74/    BT TR, FE12

FE76/    HLT 0000

FE78/    HLT 0000

FE7A/    HLT 0000

FE7C/    HLT 0000

FE7E/    HLT 0000

FE80/    HLT 0000
```

BBN ALD CODE:

```
FE00/    LDA A6 E 0000
FE02/    LDA A4 X6 X          GET ALD NUMBER(0,2,4,6)
FE04/    TST A4 L FFF9        (ACCEPT ONLY THOSE)
FE08/    BF ZE, FE50          IF BAD ALD NUMBER GO TO BAD HALT
FE0A/    TST A4 E 0004        IS IT 4 OR 6?
FE0C/    BT ZE, FE12          NO, DON'T ADD
FE0E/    ADD A4 L   003D      YES, ADD 3D TO 4 OR 6
FE12/    LI LO A4 0004        SHIFT IT
FE14/      ADD A4 L   F800    AND GENERATE THE DEVICE ADDRESS (FC30 FOR PT
                              IN A4 (ALWAYS)
FE18/    STA A1 X4 X          RESET IT
FE1A/    LDA A3 E 0000        CLEAR THE "DON'T HAVE A CHAR YET" FLAG (SO
                              JUST READ 1ST CHAR ON ««
FE1C/    LDA A7 R X0          PUT FE22 IN A7 FOR LATER USE AS RETURN ADDRE
FE1E/    ADD A7 E 0004
FE20/    BT TR, FE62          AND GO READ IN THE BYTE COUNT CHARACTER
FE22/    BT ZE, FE1A          IF IT IS LEADER (A0) IGNORE IT, INDEFINATELY
FE24/    LDA A2 X3 R          NOT LEADER, INITIATE THE BYTE COUNT (IN A2)
```

```
FE26/    JSB A7 X5 X          GET AN ADDRESS WORD

FE28/    LDA A1 X3 R          INIT UP ADDRESS POINTER (IN A1) FOR LATER USE

FE2A/    BT OD, FE50          TO BAD HALT IF ODD ADDRESS READ IN FROM TAPE

FE2C/    BF ZE, FE32          IS IT A ZERO ADDRESS?  (CAN'T STORE ANYTHING

                              INTO ADDRESS 0)

FE2E/    LDA A1 X5 L   FFF4   YES, PREPARE THE GOOD HALT ADDRESS (FE54)

FE32/    CMP A2 L   00FF      IS IT A JUMP BLOCK FLAG?

FE36/    BT EQ, FE44          YES, SKIP STORING DATA IN JUMP BLOCK

FE38/    JSB A7 X5 X          GET A DATA WORD

FE3A/    STA A A3 X1 X        STORE IT IN MEMORY

FE3C/    SUB A2 E 0002        DECREMENT THE BYTE COUNT (BY 2 ALWAYS)

FE3E/    BF ZE, FE38          IF NOT ZERO, GO GET ANOTHER DATA WORD

FE40/    LDA A1 X5 L   FFA0   IF IT IS ZERO, PREPARE THE NEW BLOCK

                              ADDRESS (FE00)

FE44/    LDA A2 X6 R          SAVE OUR CHECKSUM, AND

FE46/    JSB A7 X5 X          GET THEIR CHECKSUM WORD

FE48/    CMP A2 X3 R          IS IT THE SAME AS OURS?

FE4A/    BF EQ, FE50          NO, GO TO BAD HALT

FE4C/    STA A0 X4 X          YES, RESET THE DEVICE

FE4E/    JMP X1 X             AND GO TO:  FE00, OR THE JUMP-BLOCK STARTING

                              ADDRESS OR THE GOOD-HALT ADDRESS (FE54)
```

ALD

```
FE52/    BT TR, FE00

FE54/    HLT 0000            GOOD HALT (BY DEFAULT)

FE56/    ADD A3 X5 R         PUT THE 2 BYTES TOGETHER AS A WORD (IN A3)

                             (COME HERE ON EVEN HAVE=READ=IN BYTE COUNT,

                             EXCEPT 1ST CHARACTER ON TAPE)

FE58/    LDA A5 R X0         GET ADDRESS FE60 IN A5, FOR EVERY CALL FROM NOW ON

FE5A/    ADD A5 E 0006

FE5C/    LDA A3 X3 R         (DO THIS FOR A FLAG, I GUESS)

FE5E/    JMP X7 X            AND RETURN (TO FE22 FOR THE 1ST CHARACTER ON TAPE)

                             (TO CALL + 2 OTHERWISE)

FE60/    LDA A3 E 0001       SET THE "DON'T=HAVE=A=CHAR=YET" FLAG

FE62/    LDA A5 L 0011       TURN THE READER ON

FE66/    STA A5 X4 0006

FE6A/    LDA A5 X4 X         WAIT UNTIL ITS NOT BUSY, THEN

FE6E/    LDA A5 X4 0008      GET A CHARACTER

FE72/    ADD A6 X5 R         ADD IT TO THE "CHECKSUM"

FE74/    LDA A3 X3 R         1ST OR 2ND CHARACTER?

FE76/    BF 0D, FE56         SECOND, GO USE THE ACCUMULATED WORD

FE78/    LDA A3 X5 R         SAVE IT IN 3

FE7A/    LI L0 A3 0008       MOVE IT TO THE LEFT BYTE
```

```
FE7C/    BT TR, FE62          AND GO GET THE RIGHT BYTE
```

ALD

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	5-7-74	

ALD

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

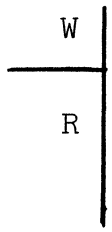
DRAWING TITLE

ALD TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		ALD-05

SCALE	REV	SHEET
	A	1 OF 4

Status - address none



Switches

ROM Select - normally both up for BBN ROM

S1	S2	ROM
down	down	1
up	up	2
down	down	3
up	up	4

ROM 3

ROM 2

ROM 4

ROM 1

Device Number Select - normally S3 up, S4 up for PTR

Device	S3	S4	Device Number
Old TTY address	down	down	0
New TTY address	down	up	1
Old PTR address	up	down	2
New PTR address	up	up	3

Jumpers

ALD Address

Address Bit	From	Connect to	
		1	Ø
8	J2-C2	J2-C1	J2-C3
9	J2- E2	J2-E1	J2-E3
10	J2-D2	J2-D1	J2-D3
11	J2-B2	J2-B1	J2-B3
12	J2-A2	J2-A1	J2-A3

Program Start Address

Data Bit	From	Connect to	
		1	Ø
8	J3-D2	J3-D1	J3-D3
9	J3-E2	J3-E1	J3-E3
10	J3-C2	J3-C1	J3-C3
11	J3-B2	J3-B1	J3-B3
12	J3-A2	J3-A1	J3-A3

Socket

J1	A1	ROM Select 1 (switch 1)
J1	B1	Ground
J1	A2	ROM Select 2 (switch 2)
J1	B2	Ground
J1	A3	Device Select 3 (switch 3)
J1	B3	Ground
J1	A4	Device Select 4 (switch 4)
J1	B4	Ground
J1	A5	Remote Reset (Reset Push Button)
J1	B5	Ground
J1	A6	Remote Autoload
J1	B6	Ground
J1	A7	Remote External Attention (Jump E1 to E2)
J1	B7	Ground

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	5-7-74	

ALD

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

ALD CARD MODIFICATION

SIZE	CODE IDENT NO.	DRAWING NO.
A		ALD-15

SCALE	REV	SHEET
	A	1 OF 5

Card Type ALD Modification Standard

Card Function: Autoload

Modification Description:

Configure with custom ROM, address recognition of FEØØ. Set switches for proper device control.

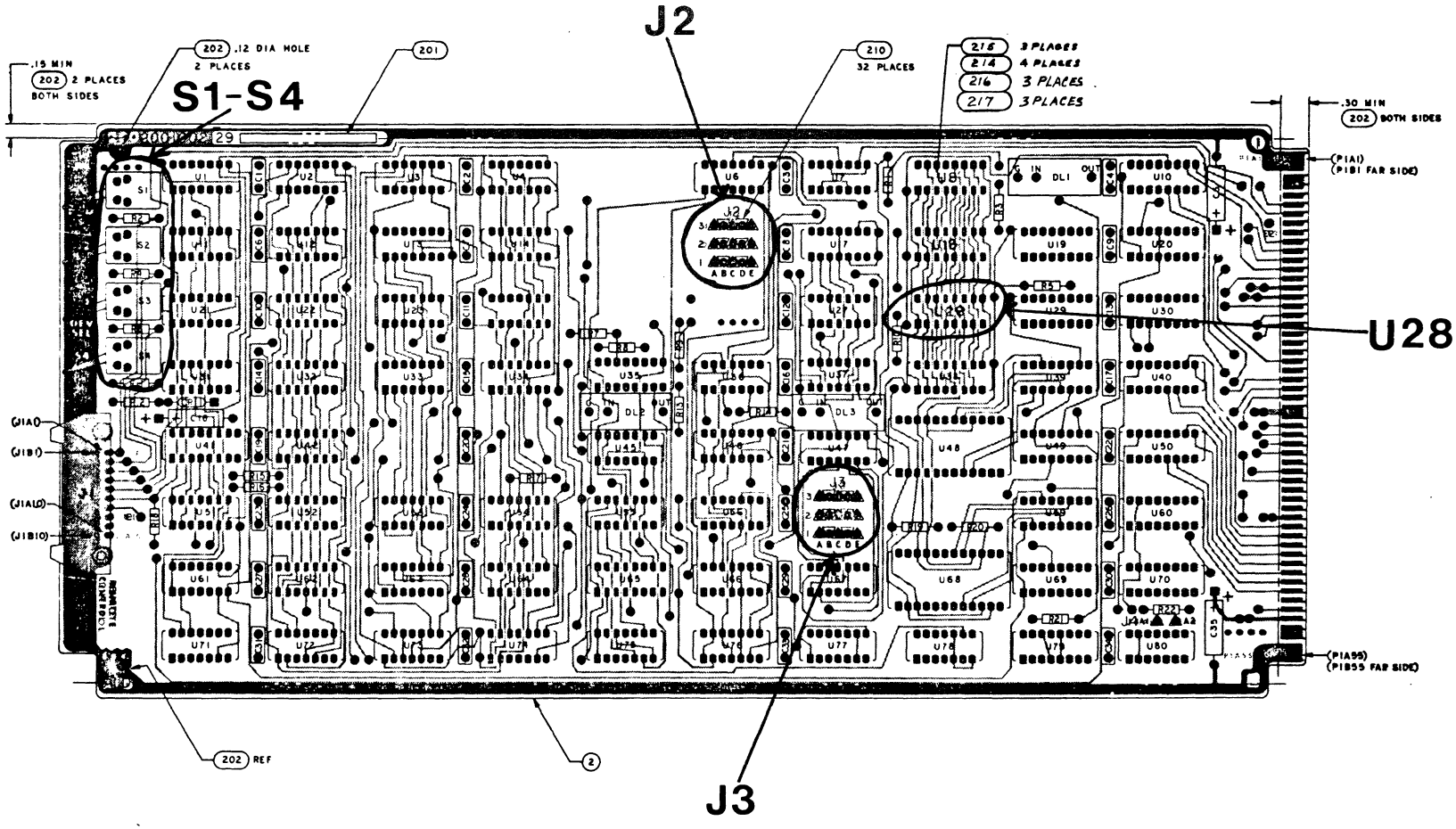
Implementation: See sketch.

Jumper with 30 ga wire wrapped as follows:

J2:	J3:
A2-A1	A2-A1
B2-B1	B2-B1
C2-C3	C2-C1
D2-D1	D2-D3
E2-E1	E2-E1

Install 16 pin IC socket at position U28. Solder all connections. Then install part number 0170 PROM IC in that socket. Make sure IC is aligned with slot to the left.

Set S1, S2, S3, S4 to the UP position.


J2
S1-S4
U28
J3
.15 MIN
202 2 PLACES
BOTH SIDES
202 .12 DIA HOLE
2 PLACES
201
210
32 PLACES
216 3 PLACES
214 4 PLACES
216 3 PLACES
217 3 PLACES
.30 MIN
202 BOTH SIDES
(P1A1)
(P1B1 FAR SIDE)
(P1A99)
(P1B55 FAR SIDE)
(J1A1)
(J1B1)
(J1A10)
(J1B10)
202 REF
2

ALD

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/1/75	

ALD

SEE ALD-Ø2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:	
DRAFTSMAN	12/9/75
CHECKER	
ENGINEER	
APP'D FOR REL	
APP'D (CUSTOMER)	

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

ALD SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		ALD-2Ø

SCALE	REV	SHEET
	A	1 OF 1

MLC Adapter

AML-Ø2 Logic Description

AML-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	9/20/77	

AML

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL 9/20/77

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

AML LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		AML - 02

SCALE	REV	SHEET
	A	1 OF 21

AML LOGIC DESCRIPTION

The MLC Adapter (AML) module is a single card which interfaces a Multiline Controller to a Pluribus. The AML functional specification describes the overall operation of the AML while this document describes operation at the gate level. All signals signed "+" are true when at a TTL high (+3V), and all signed "-" are true when at a TTL low (0V). The descriptions which follow assume that the hardware has been initially cleared, and unless otherwise noted, that the Watch Dog Timer has not timed out. Details of MLC operation and INFIBUS operation are described in other documentation.

INFIBUS Control (AML20)

The AML recognizes a block of four words. The high order six bits must be ones, as must bit 3, and the next ten bits are determined by the address recognition switches (AML23). Lines from these switches (ADS04-ADS13) are XORed with address lines 4-13 (AB04R-AB13R) with the results wire-ANDed to form ADCOM+. INFIBUS STRB (STRBR) is received and delayed by passing it through similar gating to form STRBD. This is ANDed with HOLDR (to inhibit address recognition until the fall of HOLD) to form MECLK, which strobes MLCAD into MEFFF. When the address is one of the four recognized by the AML, MECLK will set MEFFF (which is operated upside down -- when MEFFF is true, the 1 output is low).

When MEFFF comes true, a negative going transition begins to traverse the 450 ns delay line driven by a BDR. Each of the five delay line taps used is buffered by emitter followers. The 45 ns tap (STMUX) enables the decoder described below. The 90 nsec tap (PLSGO) clears MEFFF. Therefore, a negative going pulse (about 150 nsec) is now traveling along the delay line. If RITEX is false (a read operation), and SMPTY is false (IN FIFO not empty), PLSGO sets BDREN when RDNIP is true. If the input FIFO is empty on a data read, BDREN will not get set. Otherwise, BDREN is set on reads of all four registers to enable the data BDRs. BDREN is subsequently cleared by the negation of STRB on the INFIBUS. DONET comes true about 500 nsec after the rise of MEFFF.

The low order word address bits as received (AB01R, AB02R) are decoded along with RITER (INFIBUS RITE), latched by STMUX and cleared by CLMUX (the 405 ns delay tap) as follows, with all other combinations unused:

Word Address	AB02	AB01	RITE	Asserted Signal	Function
0	0	0	1	POKWD	pokes Watch Dog Timer
2	0	1	1	STOCP	assert status out control lines
4	1	0	1	STOTA	load OTA register
6	1	1	1	LDOUT	load output FIFO
6	1	1	0	RDINP	read input FIFO

The status of the input FIFO (SMPTY) and the output FIFO (SFULL) are latched on the rise of STRB (AML23) to indicate that the FIFO has no data to present or no room to accept data respectively. When SMPTY is false and RDINP comes true, LDINP comes true and input data will be unloaded from the FIFO to the INFIBUS. If SMPTY is true, this operation will be inhibited and BDREN will not come true.

MLC Control (AML21)

Emulation of the 316 I/O bus for presentation to the MLC is performed by an ROM finite state machine (FSM). This section first will describe operation of the FSM and then the sequence of the various 316 functions.

The components of the FSM are a 12-bit x 256-word ROM, three address select switches, a 5-bit address counter, 18 bits of output condition latching, and a 16-bit input condition multiplexer and latch. The ROM is programmed for both test and operation. Instruction formats, branch conditions and output latch signals are as shown in Figure 1. The high order address switch allows substitution of a pin compatible 512-word ROM.

The FSM is stepped by a two-phase 400 ns clock derived from the INFIBUS system clock (see Figure 2). GOCLK is the 2 output of a BCD counter, while SLCLK is the output of the same counter.

The positive going transition of SLCLK clocks the ROM address counter. If BRNCH is true, as might be the case for a jump or branch instruction, this will load the low order bits of the ROM data into the address counter; otherwise, the rise of SLCLK merely increments the address register. ADM00-ADM05 from

INSTRUCTIONS

DATA |11 1Ø 9 8 7 6 5 4 3 2 1 Ø|

ADDRESS |7 6 5 4 3 2 1 Ø|

IMP (BRANCH UNCONDITIONAL)

|Ø Ø Ø Ø |BRANCH ADDRESS |

BR (BRANCH CONDITION TRUE)

|CONDITION|BRANCH ADDRESS |

NOP (NO OP)

|1 1 1 |Ø Ø Ø| DON'T CARE |

OUT (OUTPUT TO LATCHES)

|1 1 1 |LATCH| CONTENTS |

BRANCH CONDITIONS (BITS 11,1Ø,9,8)

Ø Ø Ø Ø	IMP=ALWAYS TRUE
Ø Ø Ø 1	DILIN
Ø Ø 1 Ø	DILOI
Ø Ø 1 1	DILOT
Ø 1 Ø Ø	INFIFO FULL (IFULL)
Ø 1 Ø 1	OUTFIFO EMPTY (OMPTY)
Ø 1 1 Ø	OTA REQUEST (OTARQ)
Ø 1 1 1	INA REQUEST (INARQ)
1 Ø Ø Ø	DRLIN
1 Ø Ø 1	UNDEFINED
1 Ø 1 Ø	UNDEFINED
1 Ø 1 1	TEST 1
1 1 Ø Ø	TEST 2
1 1 Ø 1	TEST 3
1 1 1 Ø }	OUT-NEVER TRUE
1 1 1 1 }	

OUTPUTS

LATCH=ØØ1 (BITS 7,6,5)

5 DALIN
4 DALOI
3 DALOT
2 INB→FIFO (DSMPL)
1 FIFO→OTB (OUTDT)
Ø RRLIN (RRLND)

LATCH=Ø1Ø (BITS 7,6,5)

5 OTA INA ADDRESS 42 (OTAGO)
4 INA ADDRESS 1ØØ1 (INAGO)
3
2 OTA DATA→OTB (OTADT)
1 INB→INABUFFER (ISMPL)
9 RRLIN (RRLNI)

LATCH=1ØØ (BITS 7,6,5)

5 CLEAR OTA REQUEST (OTALL)
4 INA REQUEST (INARQ)
3 GOT DRLIN (GTDRL)
2 TEST 1
1 TEST 2
4 TEST 3

Figure 1 FSM Instructions

AML

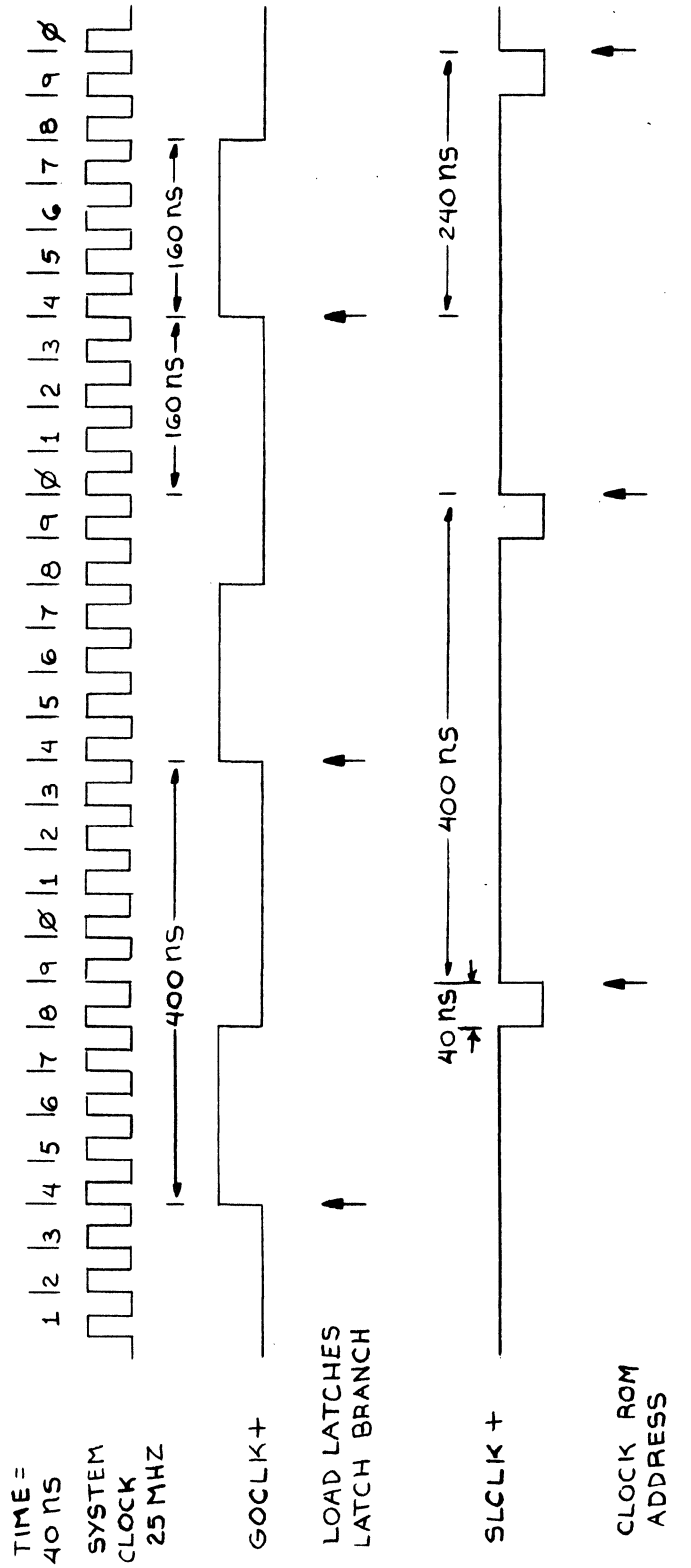


Figure 2 FSM Clock

the address counter and ADM06-ADM08 from the FSM select switches determine the address of the data that the ROM will present at its outputs. The six low order data bits (MMD00-MMD05) appear at the inputs of the output latches. The next three bits (MMD06-MMD08) appear at the enable gating for the output latch clocks (L1CLK, L2CLK, L3CLK). The high order four bits (MMD08-MMD11) select the input condition to be tested. The high order three bits (MMD09-MMD11) are gated with GOCLK to form NOTBR, which clocks the output latches on an output instruction.

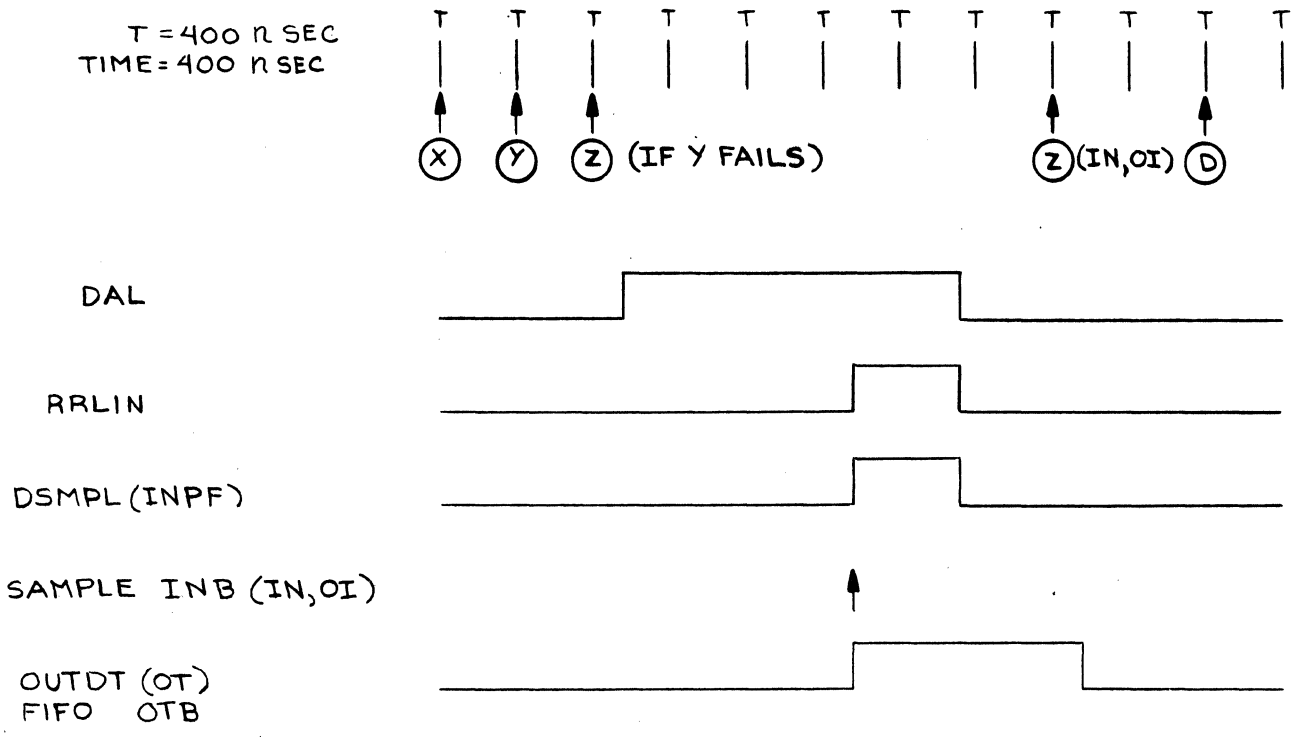
AML

The rise of GOCLK strobes the output of the condition multiplexer into BRNCH to condition the address counter load input for the next SLCLK. It also loads the low order data bits into any enabled latches (MMD06, MMD07, or MMD08 true) when MMD09-MMD11 are all true (output instruction). The sequencing of SLCLK and GOCLK allows 160 ns for the ROM to present data at its outputs and the branch condition multiplexer to be set up prior to GOCLK. Branch condition zero (jump instruction) is wired to be always true, while branch condition 111X (output or no op) is wired to be always false. TEST1, TEST2, and TEST3 are the outputs of latches that also go to on-card test points for diagnostic use.

When the FSM is operating as a 316 emulator, the ROM is programmed as described below. Figures 3 and 4 are timing diagrams for the five 316 operations to be emulated (3 DMC channels, OTA, INA). The background loop (Figure 5) of the ROM program steps through testing the five request lines (DILIN, DILOI, DILOT, OTARQ, INARQ) in a round robin manner. When a request is found to be true, the program jumps to the service routine for the operation. All timing shown in Figures 3 and 4 starts with the FSM step following this jump to the service routine time element.

With only slight exception, timing of the five operations is identical to that produced by the 316 CPU, and the exceptions are not significant. The greatest difference is that while individual operation cycles run 3.2 sec. to completion, a new cycle does not necessarily begin 3.2 sec. or a multiple thereof after the start of the previous one.

The first step of a DMC service cycle (Figure 3) is to test whether the input FIFO is full (IFULL true) for DILIN or DILOI, or the output FIFO empty (OMPTY true) for DILOT. If so, the DIL is not honored, since no transfer of data is possible, and the operation is aborted. DSMPL loads input data from the MLC to the



X - FROM FIGURE 3
Y - FIFO TEST
Z - TO FIGURE 3
D - TO FIGURE 3

	X	Z
IN	A	A
OI	B	B
OT	C	C

Figure 3 Timing for IN, OI, OUT Operations

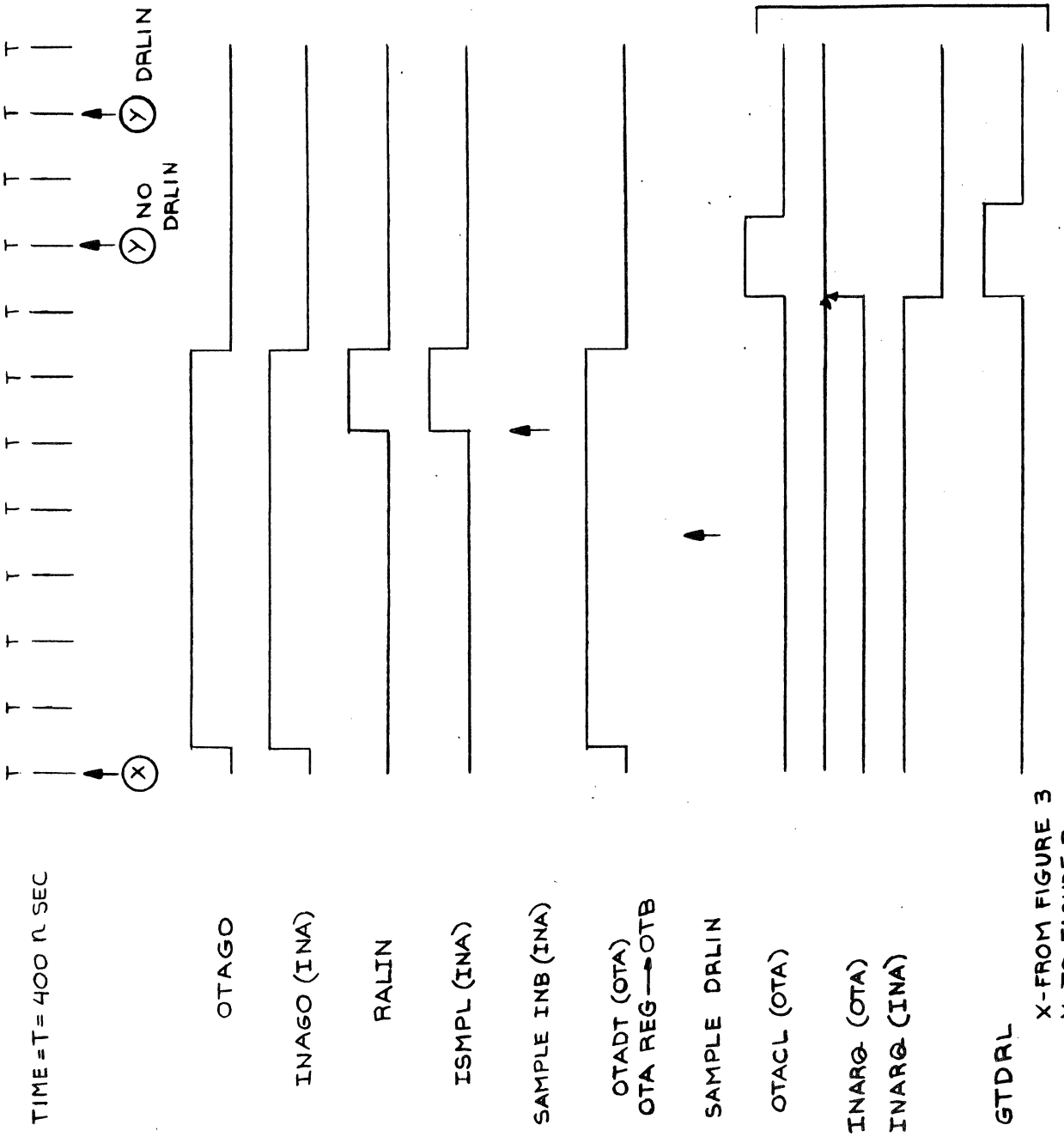


Figure 4 Timing for OTA, INA Operations

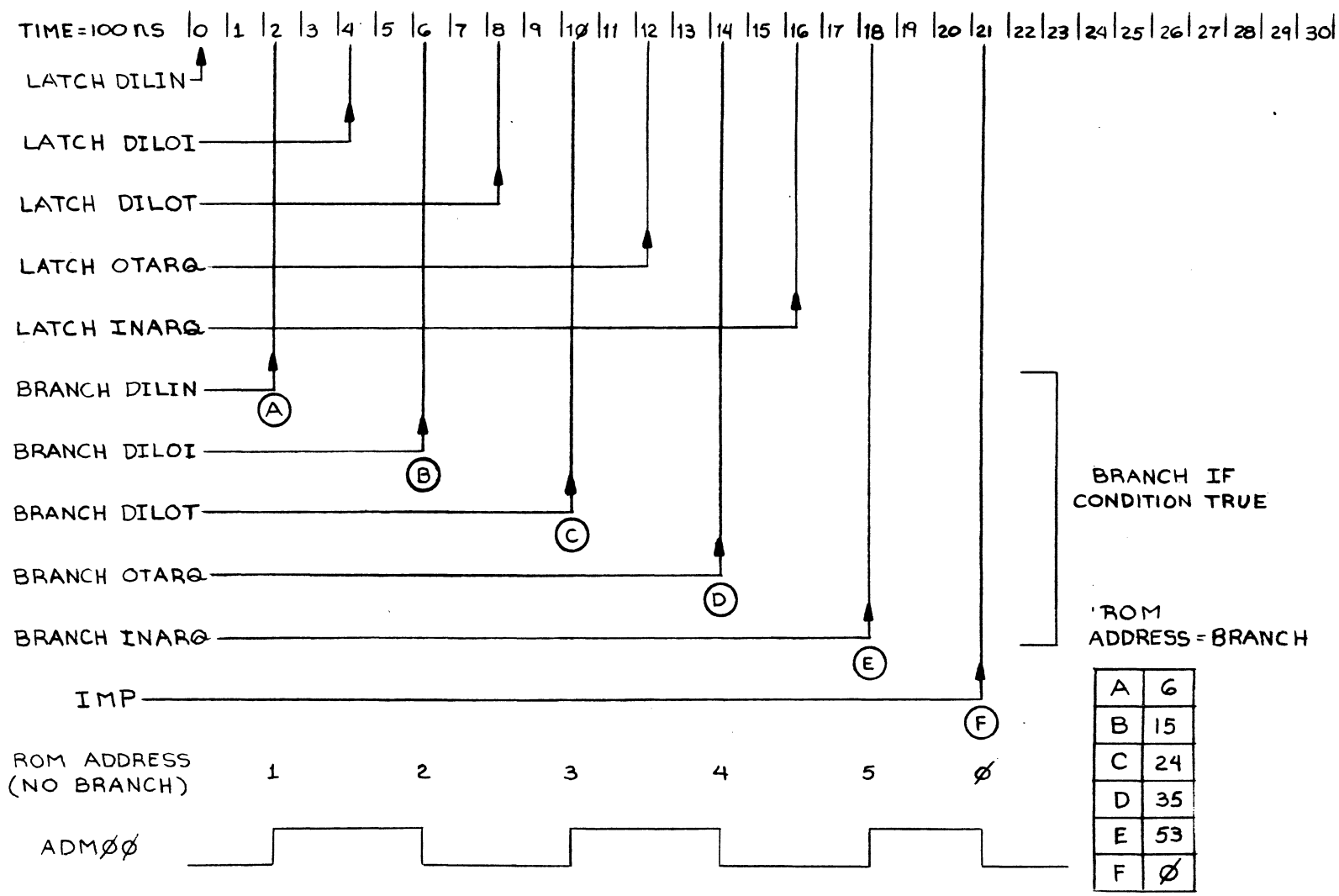


Figure 5 FSM Background Timing

input FIFO (AML22). OUTDT gates data from the output FIFO to the MLC.

In the OTA and INA cycles, two control signals set up the proper address bus lines to the MLC. OTAGO presents a 42 for the OTA instruction, while INAGO adds bits 7 and 16 for an address of 1043. Therefore, the INA cycle has both OTAGO and INAGO asserted, while the OTA cycle has only OTAGO asserted.

Within the OTA and INA cycles is a branch instruction which tests whether the MLC is asserting the DRLIN signal. For an OTA, the presence of DRLIN will cause INARQ to be set and OTARQ to be cleared (by assertion of OTACL for one step time). For an INA, DRLIN will cause GODRL to be asserted for one step time. In the absence of DRLIN, the request remains set and the operation will be attempted again.

Timing is as shown in Figure 4. OTADT gates data from the OTA register (AML22) to the MLC, while ISMPL loads data from the MLC to the INA register (AML22).

The OTARQ flop is set by STOTA (which loads data to the OTA register from the INFIBUS) and cleared by the rise of OTACL.

The timer DRLDL indicates when there has been no DRLIN from the MLC for 160 sec. following an OTA or INA. LOTGO (OTAGO) fires DRLDL, which, gated with LOTGO, prevents further retriggering of DRLDL. If GTDRL is asserted by the ROM program, indicating receipt of a DRLIN from the MLC, DRLDL is reset. Otherwise, when DRLDL times out, DRLIN is set. This signal is latched by the rise of STRB and is available as the NODRL status bit.

The ROM programs are listed as Appendix A. Timing of the ROM programs for card testing is described in the AML test procedure.

FIFOs and Registers (AML22)

Output and input data to and from the MLC passes through two 16-bit x 64-word FIFOs, one in each direction. The output data is loaded from the INFIBUS into the output FIFO on the rise of LDOUT (asserted by the INFIBUS decoder (AML20)) and emptied after the fall of OUTDT (asserted by the ROM program (AML21)). The four input ready (IR) signals are ANDed to form OFULL (output full), which when true indicates that the FIFO cannot accept more

output data. This is latched on the rise of STRB to synchronize it with the INFIBUS service cycle. Similarly, the four output ready (OR) signals are ANDed to form OMPTY (output empty) which when true indicates that the FIFO has no data to present to the MLC. This signal is tested by the ROM program.

The input data is loaded from the MLC in the input FIFO on the rise of DSMPL, which is asserted by the ROM program (AML21). Data is unloaded to the INFIBUS on the fall of LDINP, which is asserted by the INFIBUS decoder (AML20). Analogous to the signals for the output FIFO, IMPTY when true indicates that the input FIFO has no data for the INFIBUS. This signal is latched on the rise of STRB to synchronize it. Similarly, IFULL indicates when true that the FIFO cannot accept data from the MLC. This signal is tested by the ROM program. Note the input FIFO data is true when low.

The OTA register (BTA00-BTA15) holds the OTA word to be sent to the MLC. It is loaded on the rise of STOTA, which also sets the OTA request flop (OTARQ). The INA register (BNA00-15) is loaded on the rising edge of ISMPL, which is asserted by the ROM program. Note that this register is operating with data inverted (true when low).

INFIBUS Data (AML24)

The BDRs to the INFIBUS are enabled by BDREN. The BDR input signals are selected by multiplexers whose select inputs are bits 1 and 2 of the address bus. Selection is as follows:

Word Address	AB02R	AB01R	Function	Signals
0	0	0	Device type	DSW00-DSW05, hard-wired device type
2	0	1	Status bits	Various
4	1	0	INA Register	BNA02-BNA15, INARY OTARY
6	1	1	In Data FIFO	FIN00-FIN15

Those bits for which only two sources (BNA, FIN) are present use a two-way multiplexer and a separate BDR which is only enabled when AB02R is true (word addresses 4 and 6). Note that all data through the multiplexers is true when low.

MLC Data (AML25)

A two-way multiplexer selects output data from the output FIFO (FOT00-FOT15) or the OTA register (BTA00-BTA15) to send to the MLC. OUTDT selects the FIFO, while OTADT selects the register. Both signals are asserted by the ROM program (AML21). Input data is received and inverted. Drivers and receivers are described below.

Switches, etc. (AML23)

The address recognition and device-type data switches operate in the conventional manner with a value of 1 when closed and 0 when open.

The status lines for the INFIBUS side of the FIFOs (OFULL for output full, IMPTY for input empty) the INA and OTA requests (INARQ, OTARQ), the DRLIN timeout (DRLIN), and the Watch Dog Timer (WDTOK), are synchronized to the INFIBUS by latching their conditions on the rise of STRB. The subsequent interval provided by the delay of STRB and other gate delays assures that these conditions will become stabilized prior to BDREN (AML20), which gates the status bits to the INFIBUS and allows input data or output data to be transferred if the FIFO is ready to do so. The RITE latch is included with the other signals for convenience.

Notice that most of the latches are operated inverted and that OTARY (OTA READY) is inverted from OTA request, since if a request is pending, the OTA ready status should be false (OTA not ready). Similarly, INARY is inverted. GVDNE is always set on the rise of MEFFF and direct cleared when STRBR goes false (falling edge of STROBE).

The Watch Dog Timer is a retriggerable oneshot with a duration of one second. It is triggered by writing to the device-type register (WORD 0) which asserts POKWD. While the timer is running, WDTOK is true. This signal enables all the drivers to the MLC and allows operation of the FSM output latches (AML20). When it is false, the drivers are disabled and the latches are held in the clear state.

While STOCP (decoded write status - AML20) is true, three data bits will be active. Bit 8 asserts RESET (and REST2) which resets the AML card. If WDTOK is true, bit 9 asserts CLMLC, which presents Master Clear to the MLC, clearing the MLC central logic. Bit 10 aserts WDCLR, which resets the Watch Dog Timer.

In addition, INFIBUS Master Reset (MRESR) asserts RESET and WDCLR.

MLC Drivers and Receivers

All lines to and from the MLC, with the exception of DRLIN, are true when high. A cable terminator card at the MLC converts to and from the levels the MLC expects with a 316 connection. Gating ahead of the drivers to the MLC disables these drivers when WDTOK is false. In addition, the drivers go inactive when the AML card loses power.

The basic driver circuit is an emitter follower (one section of a seven transistor array) terminated in the characteristic impedance of the twisted pair cable (150) at the MLC end (see Figure 6). The basic receiver circuit is a Schmitt trigger inverter, also terminated at the MLC end. These driver and receiver elements are used at both ends of the cable.

The DRLIN signal, which is true when low, serves as a detector of abnormalities in the cable connections. Received DRLIN arrives on the first cable and is carried through a jumper connection on the second cable. If either cable is improperly connected at the AML end, the 4.7K pullup on the DRLIN receiver (AML21) assures that the FSM will never sense DRLIN as true, causing NODRL status to become true.

Multiple AML connections to a single MLC are accomplished by a Y configuration where each AML is cabled to a separate terminator card at the MLC. These terminator cards in turn connect to the MLC I/O bus lines.

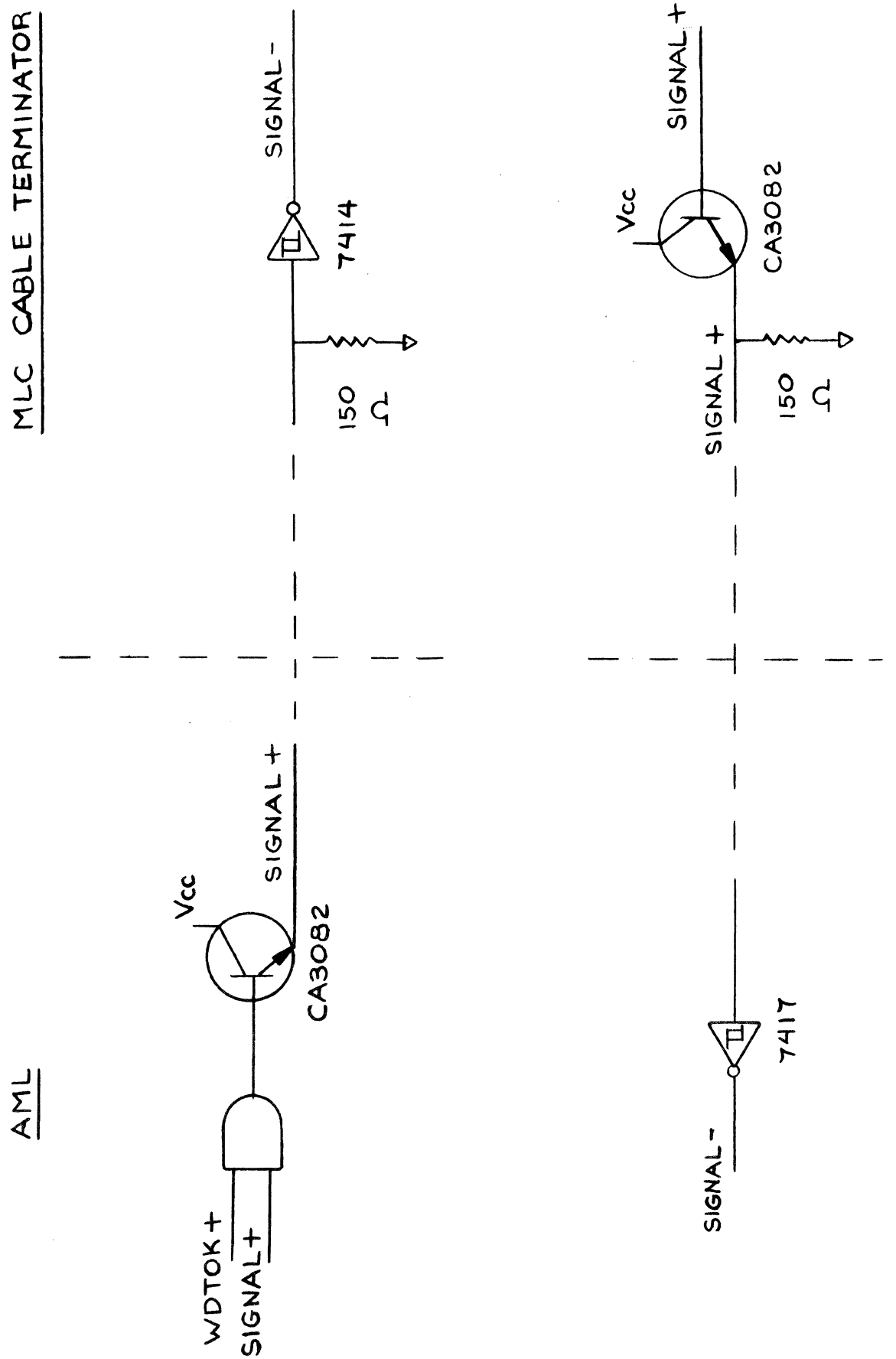


Figure 6 Basic Cable Drawing and Receiving Circuits

AML

APPENDIX A

ROM PROGRAMS

```
PAGE 1                                  ROMFMT,2,MISAN   2:37 PM 7/28/1975
000   0001 0000 0110   0406   BR 6  DILIN  /BKGND TEST REQUESTS
001   0010 0000 1101   1015   BR 15 DILOI
002   0011 0001 0100   1424   BR 24 DILOT
003   0110 0001 1101   3035   BR 35 OTARQ
004   0111 0010 1011   3453   BR 53 INARQ
005   0000 0000 0000   0000   JMP 0
006   0100 0000 0001   2001   BR  1 IFULL  /DILIN-FIFO TEST-T1
007   1110 0110 0000   7140   OUT DALIN"   /T2

010   1110 0000 0000   7000   NOP          /T3
011   1110 0000 0000   7000   NOP         /T4
012   1110 0110 0101   7145   OUT RRLIN",DSMPL"   /T1
013   1110 0100 0000   7100   OUT DALIN/,RRLIN/,DSMPL/   /T2
014   0000 0000 0001   0001   JMP 0        /T3,T4
015   0100 0000 0010   2002   BR 2 IFULL /DILOI-FIFO TEST-T1
016   1110 0101 0000   7420   OUT DALOI"   /T2
017   1110 0000 0000   7000   NOP         /T3

020   1110 0000 0000   7000   NOP         /T4
021   1110 0101 0101   7125   OUT RRLIN",DSMPL"   /T1
022   1110 0100 0000   7100   OUT DALOI/,RRLIN/,DSMPL/   /T2
023   0000 0000 0010   0002   JMP 2        /T3,T4
024   0101 0000 0011   2403   BR  3 OMPTY /DILOT-FIFO TEST-T1
025   1110 0100 1000   7110   OUT DALOT"    /T2
026   1110 0000 0000   7000   NOP           /T3
027   1110 0000 0000   7000   NOP           /T4

030   1110 0100 1011   7113   OUT OUTDT",RRLIN"   /T1
031   1110 0100 0010   7102   OUT RRLIN/,DALOT/   /T2
032   1110 0000 0000   7000   NOP             /T3
033   1110 0100 0000   7100   OUT OUTDT/      /T4
034   0000 0000 0011   0003   JMP 3
035   1110 1000 0100   7204   OUT OTADT"      /OTARQ-T1
036   1110 1010 0100   7244   OUT OTAGO"      /T3
037   1110 0000 0000   7000   NOP             /T2

040   1110 0000 0000   7000   NOP             /T4
041   1110 0000 0000   7000   NOP             /T1
042   1000 0010 0110   4046   BR 46 DRLIN       /T2
043   1110 1010 0101   7245   OUT RRLIN"    /T3-NO DRLIN
044   1110 1000 0000   7200   OUT RRLIN/,OTAGO/,OTADT/   /T4-NO DRLIN
045   0000 0000 0100   0004   JMP 4
046   1110 1010 0101   7245   OUT RRLIN"      /T3-GOT DRLIN
047   1110 1000 0000   7200   OUT RRLIN/,OTAGO/,OTADT/   /T4-GOT DRLIN

050   1111 0011 1000   7470   OUT OTACL",INARQ",GTDRL"
051   1111 0001 0000   7420   OUT OTACL/,GTDRL/
052   0000 0000 0100   0004   JMP 4
053   1110 0000 0000   7000   NOP             /INARQ-T1
054   1110 1011 0000   7260   OUT OTAGO",INAGO"   /T2
055   1110 0000 0000   7000   NOP                 /T3
056   1110 0000 0000   7000   NOP                 /T4
057   1110 0000 0000   7000   NOP                 /T1
```

```
060   1000 0011 0100   4064   BR 64 DRLIN     /T2
061   1110 1011 0011   7262   OUT RRLIN^,ISMPL^    /T3-NO DRLIN
062   1110 1000 0000   7200   OUT RRLIN/,ISMPL/,INAGO/,OTAGO/ /T4-NO DRLIN
063   0000 0000 0000   0000   JMP 0
064   1110 1011 0011   7263   OUT RRLIN^,ISMPL^     /T3-DRLIN
065   1110 1000 0000   7200   OUT RRLIN/,ISMPL/,INAGO/,OTAGO/   /T4-DRLIN
066   1111 0000 1000   7410   OUT GTDRL^,INARQ/
067   1111 0000 0000   7400   OUT GTDRL/

070   0000 0000 0000   0000   JMP 0
071   0000 0000 0000   0000   JMP 0
072   0000 0000 0000   0000   JMP 0
073   0000 0000 0000   0000   JMP 0
074   0000 0000 0000   0000   JMP 0
075   0000 0000 0000   0000   JMP 0
076   0000 0000 0000   0000   JMP 0
077   0000 0000 0000   0000   JMP 0

100   0000 0000 0001   0001   JMP 1     /COUNTER LOAD TEST
101   0000 0000 0010   0002   JMP 2     /JMP .+1
102   0000 0000 0011   0003   JMP 3
103   0000 0000 0100   0004   JMP 4
104   0000 0000 0101   0005   JMP 5
105   0000 0000 0110   0006   JMP 6
106   0000 0000 0111   0007   JMP 7
107   0000 0000 1000   0010   JMP 10

110   0000 0000 1001   0011   JMP 11
111   0000 0000 1010   0012   JMP 12
112   0000 0000 1011   0013   JMP 13
113   0000 0000 1100   0014   JMP 14
114   0000 0000 1101   0015   JMP 15
115   0000 0000 1110   0016   JMP 16
116   0000 0000 1111   0017   JMP 17
117   0000 0001 0000   0020   JMP 20

120   0000 0001 0001   0021   JMP 21
121   0000 0001 0010   0022   JMP 22
122   0000 0001 0011   0023   JMP 23
123   0000 0001 0100   0024   JMP 24
124   0000 0001 0101   0025   JMP 25
125   0000 0001 0110   0026   JMP 26
126   0000 0001 0111   0027   JMP 27
127   0000 0001 1000   0030   JMP 30

130   0000 0001 1001   0031   JMP 31
131   0000 0001 1010   0032   JMP 32
132   0000 0001 1011   0033   JMP 33
133   0000 0001 1100   0034   JMP 34
134   0000 0001 1101   0035   JMP 35
135   0000 0001 1110   0036   JMP 36
136   0000 0001 1111   0037   JMP 37
137   0000 0010 0000   0040   JMP 40
```

AML

```
140   0000 0010 0001   0041   JMP 41
141   0000 0010 0010   0042   JMP 42
142   0000 0010 0011   0043   JMP 43
143   0000 0010 0100   0044   JMP 44
144   0000 0010 0101   0045   JMP 45
145   0000 0010 0110   0046   JMP 46
146   0000 0010 0111   0047   JMP 47
147   0000 0010 1000   0050   JMP 50

150   0000 0010 1001   0051   JMP 51
151   0000 0010 1010   0052   JMP 52
152   0000 0010 1011   0053   JMP 53
153   0000 0010 1100   0054   JMP 54
154   0000 0010 1101   0055   JMP 55
155   0000 0010 1110   0056   JMP 56
156   0000 0010 1111   0057   JMP 57
157   0000 0011 0000   0060   JMP 60

160   0000 0011 0001   0061   JMP 61
161   0000 0011 0010   0062   JMP 62
162   0000 0011 0011   0063   JMP 63
163   0000 0011 0100   0064   JMP 64
164   0000 0011 0101   0065   JMP 65
165   0000 0011 0110   0066   JMP 66
166   0000 0011 0111   0067   JMP 67
167   0000 0011 1000   0070   JMP 70

170   0000 0011 1001   0071   JMP 71
171   0000 0011 1010   0072   JMP 72
172   0000 0011 1011   0073   JMP 73
173   0000 0011 1100   0074   JMP 74
174   0000 0011 1101   0075   JMP 75
175   0000 0011 1110   0076   JMP 76
176   0000 0011 1111   0077   JMP 77
177   0000 0000 0000   0000   JMP 0

200   1110 0110 0000   7140   OUT 1-1     /OUTPUT LATCH TEST
201   1110 0000 0000   7000   NOP
202   1110 0100 0000   7100   OUT 1-0
203   1110 0101 0000   7120   OUT 1-2
204   1110 0000 0000   7000   NOP
205   1110 0100 0000   7100   OUT 1-0
206   1110 0100 1000   7110   OUT 1-3
207   1110 0000 0000   7000   NOP

210   1110 0100 0000   7100   OUT 1-0
211   1110 0100 0100   7104   OUT 1-4
212   1110 0000 0000   7000   NOP
213   1110 0100 0000   7100   OUT 1-0
214   1110 0100 0010   7102   OUT 1-5
215   1110 0000 0000   7000   NOP
216   1110 0100 0000   7100   OUT 1-0
217   1110 0100 0001   7101   OUT 1-6
```

```
220   1110 0000 0000   7000   NOP
221   1110 0100 0000   7100   OUT 1-0
222   1110 1010 0000   7240   OUT 2-1
223   1110 0000 0000   7000   NOP
224   1110 1000 0000   7200   OUT 2-0
225   1110 1001 0000   7220   OUT 2-2
226   1110 0000 0000   7000   NOP
227   1110 1000 0000   7200   OUT 2-0

230   1110 1000 1000   7210   OUT 2-3
231   1110 0000 0000   7000   NOP
232   1110 1000 0000   7200   OUT 2-0
233   1110 1000 0100   7204   OUT 2-4
234   1110 0000 0000   7000   NOP
235   1110 1000 0000   7200   OUT 2-0
236   1110 1000 0010   7202   OUT 2-5
237   1110 0000 0000   7000   NOP

240   1110 1000 0000   7200   OUT 2-0
241   1110 1000 0001   7201   OUT 2-6
242   1110 0000 0000   7000   NOP
243   1110 1000 0000   7200   OUT 2-0
244   1111 0010 0000   7440   OUT 3-1
245   1110 0000 0000   7000   NOP
246   1111 0000 0000   7400   OUT 3-0
247   1111 0001 0000   7420   OUT 3-2

250   1110 0000 0000   7000   NOP
251   1111 0000 0000   7400   OUT 3-0
252   1111 0000 1000   7410   OUT 3-3
253   1110 0000 0000   7000   NOP
254   1111 0000 0000   7400   OUT 3-0
255   1111 0000 0100   7404   OUT 3-4
256   1110 0000 0000   7000   NOP
257   1111 0000 0000   7400   OUT 3-0

260   1111 0000 0010   7402   OUT 3-5
261   1110 0000 0000   7000   NOP
262   1111 0000 0000   7400   OUT 3-0
263   1111 0000 0001   7401   OUT 3-6
264   1110 0000 0000   7000   NOP
265   1111 0000 0000   7400   OUT 3-0
266   1110 0111 1111   7177   OUT 1-ALL
267   1110 0000 0000   7000   NOP

270   1110 0100 0000   7100   OUT 1-0
271   1110 1011 1111   7277   OUT 2-ALL
272   1110 0000 0000   7000   NOP
273   1110 1000 0000   7200   OUT 2-0
274   1111 0011 1111   7477   OUT 3-ALL
275   1110 0000 0000   7000   NOP
276   1111 0000 0000   7400   OUT 3-0
277   0000 0000 0000   0000   JMP 0
```

AML

```
300   1110 0111 1111   7177   OUT 1-77     /BRANCH TEST
301   1110 0000 0000   7000   NOP
302   1011 0011 1110   5476   BR 76 TEST1
303   1110 0111 1110   7176   OUT 1-76
304   1110 0000 0000   7000   NOP
305   1100 0011 1110   6076   BR 76 TEST2
306   1110 0111 1101   7175   OUT 1-75
307   1110 0000 0000   7000   NOP

310   1101 0011 1110   6476   BR 76 TEST3
311   1110 0111 1100   7174   OUT 1-74
312   1111 0000 0100   7404   OUT TEST1"
313   1011 0000 1101   5415   BR 15 TEST1
314   0000 0011 1110   0076   JMP 76
315   1110 0111 1011   7173   OUT 1-73
316   1110 0000 0000   7000   NOP
317   1100 0011 1110   6076   BR 76 TEST2

320   1110 0111 1010   7172   OUT 1-72
321   1110 0000 0000   7000   NOP
322   1101 0011 1110   6476   BR 76 TEST3
323   1110 0111 1001   7171   OUT 1-71
324   1111 0000 0010   7402   OUT TEST1/,TEST2"
325   1011 0011 1110   5476   BR 76 TEST1
326   1110 0111 1000   7170   OUT 1-70
327   1110 0000 0000   7000   NOP

330   1100 0001 1010   6032   BR 32 TEST2
331   0000 0011 1110   0076   JMP 76
332   1110 0111 0111   7167   OUT 1-67
333   1110 0000 0000   7000   NOP
334   1101 0011 1110   6476   BR 76 TEST3
335   1110 0111 0110   7166   OUT 1-66
336   1111 0000 0001   7401   OUT TEST2/,TEST3"
337   1011 0011 1110   5476   BR 76 TEST1

340   1110 0111 0101   7165   OUT 1-65
341   1110 0000 0000   7000   NOP
342   1100 0011 1110   6076   BR 76 TEST2
343   1110 0111 0100   7164   OUT 1-64
344   1110 0000 0000   7000   NOP
345   1101 0010 0111   6447   BR 47 TEST3
346   0000 0011 1110   0076   JMP 76
347   1110 0111 0011   7163   OUT 1-63

350   1111 0000 0111   7407   OUT TEST1",TEST2"
351   1011 0010 1011   5453   BR 53 TEST1
352   0000 0011 1110   0076   JMP 76
353   1110 0000 0000   7000   NOP
354   1100 0010 1110   6056   BR 56 TEST2
355   0000 0011 1110   0076   JMP 76
356   1110 0000 0000   7000   NOP
357   1101 0011 0001   6461   BR 61 TEST3
```

```
360   0000 0011 1110   0076   JMP 76
361   1111 0000 0000   7400   OUT 3-0
362   1110 1000 0000   7200   OUT 2-0
363   0000 0000 0000   0000   JMP 0
364   1110 0100 0000   7100   OUT 1-0
365   1110 0100 0000   7100   OUT 1-0
366   1110 0100 0000   7100   OUT 1-0
367   1110 0100 0000   7100   OUT 1-0

370   1110 0100 0000   7100   OUT 1-0
371   1110 0100 0000   7100   OUT 1-0
372   1110 0100 0000   7100   OUT 1-0
373   1110 0100 0000   7100   OUT 1-0
374   1110 0100 0000   7100   OUT 1-0
375   1110 0100 0000   7100   OUT 1-0
376   1110 0100 0000   7100   OUT 1-0
377   0000 0000 0000   0000   JMP 0
```

AML

AML

AML-2Ø SCHEMATICS

13	12	11	10	9	8	7	6	5	4	3	2	1	
	CA3082	7414	74151	74161	3341 [SOCKET]	3341 [SOCKET]	3341 [SOCKET]	3341 [SOCKET]	74174	74174	BDR	BDR	
	CA3082	7414	74151	74161	3341 [SOCKET]	3341 [SOCKET]	3341 [SOCKET]	3341 [SOCKET]	74174	74174	74157	BDR	B
	CA3082	7414	SWITCH FSM/ADDRESS	SWITCH ADDRESS	74196	6301 [SOCKET]	6301 [SOCKET]	6301 [SOCKET]	74174	74174	BDR	BDR	C
	CA3082 CONTROL	7414	SWITCH DEV. TYPE	RES. 4.7K	RES. 4.7K	7421	7421	74136	74153	74153	7430	BDR	D
TEST POINT 1	74174	74157 OTB	74157 OTB	7421	7474	DRES 1	DRES	74136	74153	74153	9334	BDR	E
TEST POINT 1	74174	74157 OTB	7402	7408	74S74	DELAY	74123	74136	74153	74174	74S04	BDR	F
TEST POINT 1	74174	74157 OTB	7410	7432	7400	74S00	7404	7408	74153	74175	BDR	BDR	G

REVISION			
APPD.	SYM	DESCR	DATE
	A	REL PROD	8-2-
	B	ECN 0184	1-27-76
	C	ECN 0188	2-5-76
	D	ECN 0202	4-16-76
	E	ECN 0226	8-3-76

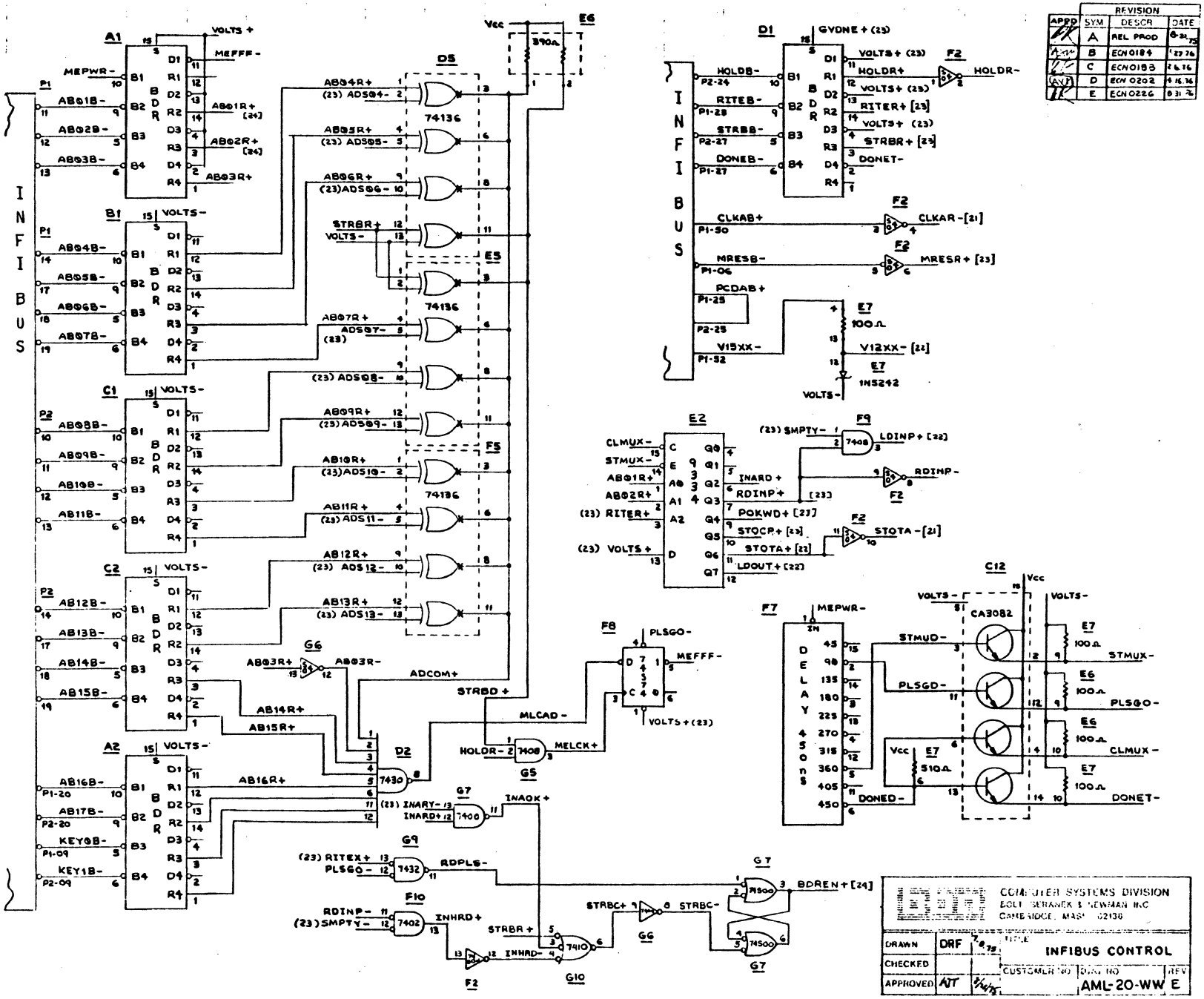
NOTES :

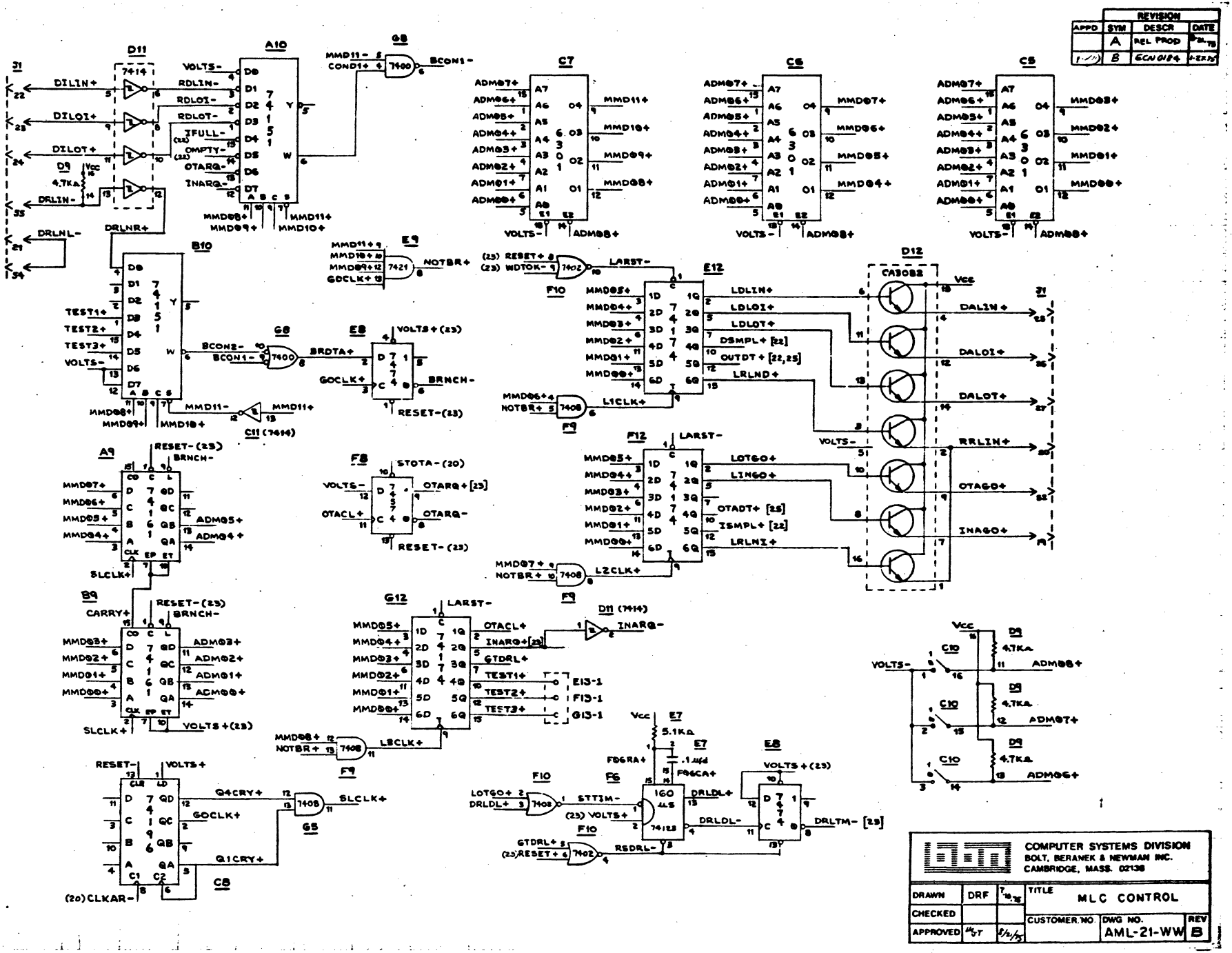
TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

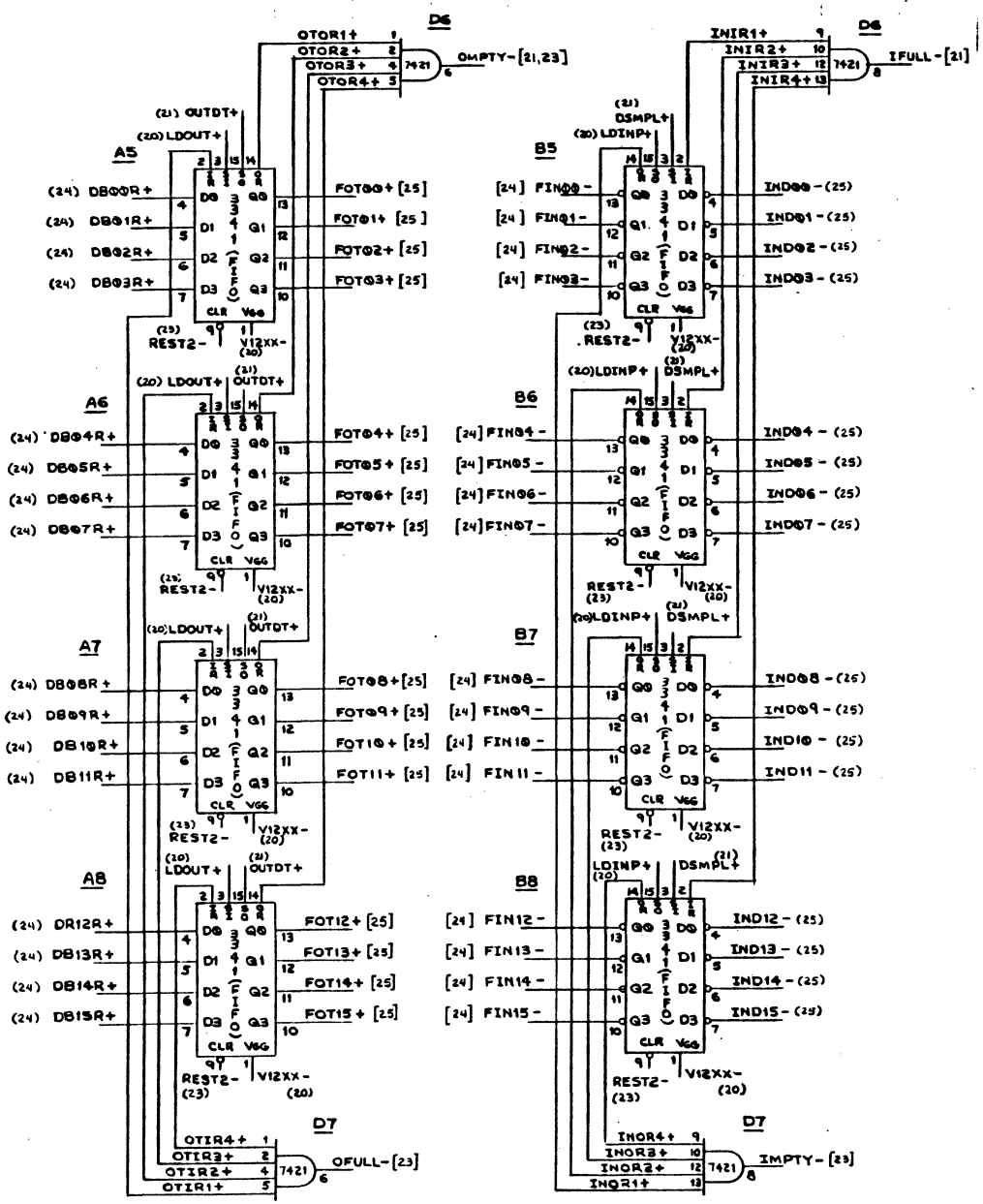
DRAWN	S.E.T.	7/25/75	TITLE: INTEGRATED CIRCUIT LAYOUT
CHECKED			
APPROVED	RWJT	8/4/75	CUSTOMER/NO.: HSM.MP; DWG NO.: AML-00-WW; REV: E

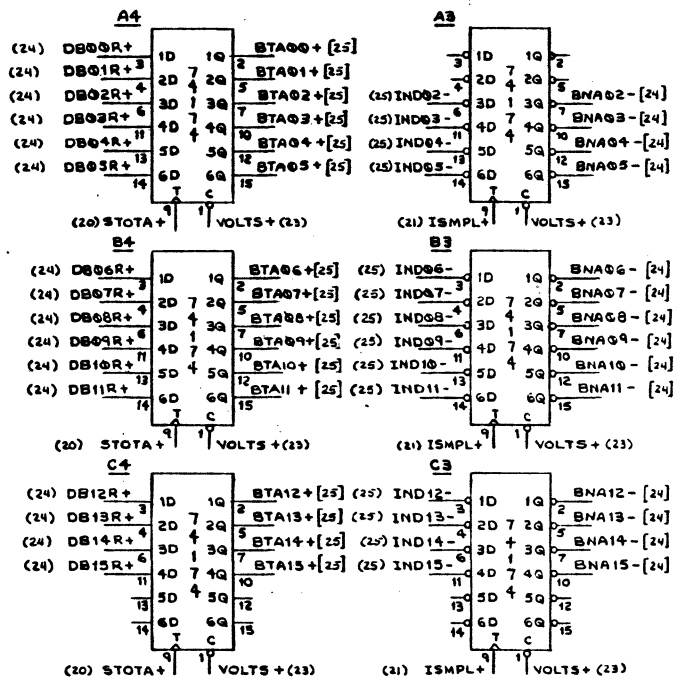
AML


INFIBUS
A1
B1
C1
C2
A2
BDR
MEPWR-
VOLTS+
MEFFF-
AB01R+ [24]
AB02R+ [24]
AB03R+
VOLTS-
AB01B-
AB02B-
AB03B-
AB04B-
AB05B-
AB06B-
AB07B-
AB08B-
AB09B-
AB10B-
AB11B-
AB12B-
AB13B-
AB14B-
AB15B-
AB16B-
AB17B-
KEY0B-
KEY1B-
P1-20
P2-20
P1-09
P2-09
D5
74136
E5
F5
Vcc
390Ω
E6
AB04R+
(23) ADS04-
AB05R+
(23) ADS05-
AB06R+
(23) ADS06-
STRBR+
VOLTS-
AB07R+
ADS07-
(23)
(23) ADS08-
AB09R+
(23) ADS09-
AB10R+
(23) ADS10-
AB11R+
(23) ADS11-
AB12R+
(23) ADS12-
AB13R+
(23) ADS13-
G6
AB03R+
AB03R-
ADCOM+
STRBD+
AB14R+
AB15R+
AB16R+
D2
7430
G7
(23) INARY-
INARD+
7400
INAOK+
G9
(23) RITEX+
PLSGO-
7432
RDPLS-
F10
RDINP-
(23) SMPTY-
7402
INHRD+
STRBR+
7410
INHRD-
F2
G10
STRBC+
STRBC-
GG
7450
BDREN+ [24]
D1
GVDNE+ (23)
HOLDB-
P2-24
RITEB-
P1-28
STRBB-
P2-27
DONEB-
P1-27
VOLTS+ (23)
HOLDR+
HOLDR-
RITER+ [23]
STRBR+ [23]
DONET-
F2
CLKAB+
P1-50
CLKAR-[21]
MRESB-
P1-06
MRESR+ [23]
PCDAB+
P1-25
P2-25
V15XX-
P1-32
E7
100Ω
V12XX- [22]
1N5242
E2
CLMUX-
STMUX-
AB01R+
AB02R+
(23) RITER+
(23) VOLTS+
INARD+
RDINP+
POKWD+ [23]
STOCP+ [23]
STOTA+ [22]
LDOUT+ [22]
(23) SMPTY-
F9
7408
LDINP+ [22]
RDINP-
STOTA- [21]
F8
PLSGO-
MEFFF-
VOLTS+ (23)
MLCAD-
HOLDR-
MELCK+
G5
F7
DELAY 450ns
MEPWR-
STMUD-
PLSGD-
DONED-
C12
CA3082
E7
100Ω
510Ω
STMUX-
PLSGO-
CLMUX-
DONET-
REVISION
APPD
SYM
DESCR
DATE
A
REL PROD
B
ECN0184
C
ECN0188
D
ECN 0202
E
ECN0226
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138
DRAWN
DRF
CHECKED
APPROVED
AJT
TITLE
INFIBUS CONTROL
CUSTOMER NO
DWG NO
REV
AML-20-WW E


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD
B | ECN 0184
J1
DILIN+
DILOI+
DILOT+
DRLIN-
DRLNL-
DRLNR+
D11
7414
A10
VOLTS-
RDLIN-
RDLOI-
RDLOT-
IFULL-
OMPTY-
OTARQ-
INARQ-
MMD08+
MMD09+
MMD11+
MMD10+
G8
7400
MMD11-
COND1+
BCON1-
C7
C6
C5
ADM07+
ADM06+
ADM05+
ADM04+
ADM03+
ADM02+
ADM01+
ADM00+
MMD11+
MMD10+
MMD09+
MMD08+
MMD07+
MMD06+
MMD05+
MMD04+
MMD03+
MMD02+
MMD01+
MMD00+
VOLTS-
ADM08+
B10
TEST1+
TEST2+
TEST3+
BCON2-
BRDTA+
BRNCH-
E9
7421
NOTBR+
GOCLK+
E8
RESET-(23)
C11 (7414)
F10
E12
F9
D12
CA3082
LARST-
LDLIN+
LDLOI+
LDLOT+
DSMPL+ [22]
OUTDT+ [22,25]
LRLND+
L1CLK+
L2CLK+
LOTGO+
LINGO+
OTADT+ [25]
ISMPL+ [22]
LRLNI+
DALIN+
DALOI+
DALOT+
RRLIN+
OTAGO+
INAGO+
A9
B9
CARRY+
SLCLK+
VOLTS+(23)
F8
STOTA-(20)
OTACL+
G12
INARQ+[23]
GTDRL+
TEST1+
TEST2+
TEST3+
E13-1
F13-1
G13-1
L8CLK+
D11 (7414)
INARQ-
RESET-
G5
Q4CRY+
GOCLK+
Q1CRY+
C8
(20)CLKAR-
E7
5.1KΩ
.1 μfd
FB6RA+
FB6CA+
160
74123
STTIM-
DRLDL+
DRLDL-
RSDRL-
DRLTM-[23]
C10
D9
4.7KΩ
ADM08+
ADM07+
ADM06+
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF
CHECKED
APPROVED
TITLE MLC CONTROL
CUSTOMER NO.
DWG NO. AML-21-WW
REV B
AML

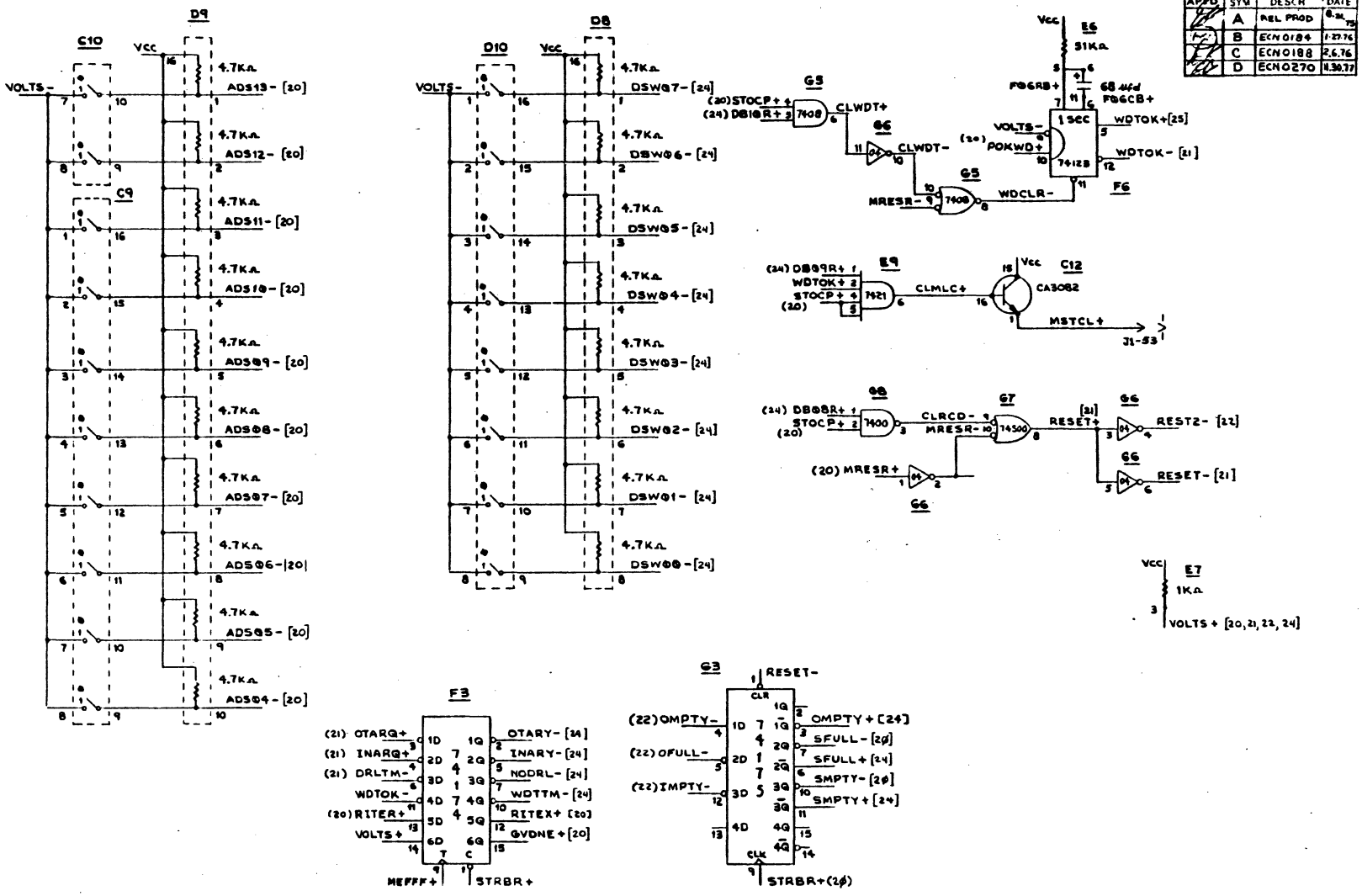
APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	4.21.75
	B	ECN 0270	4.30.77





COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	7/7/75	TITLE: FIFOS & REGISTERS
CHECKED			CUSTOMER NO. / DWG NO. AML-22-WW / REV B
APPROVED	AJT	7/11/75	



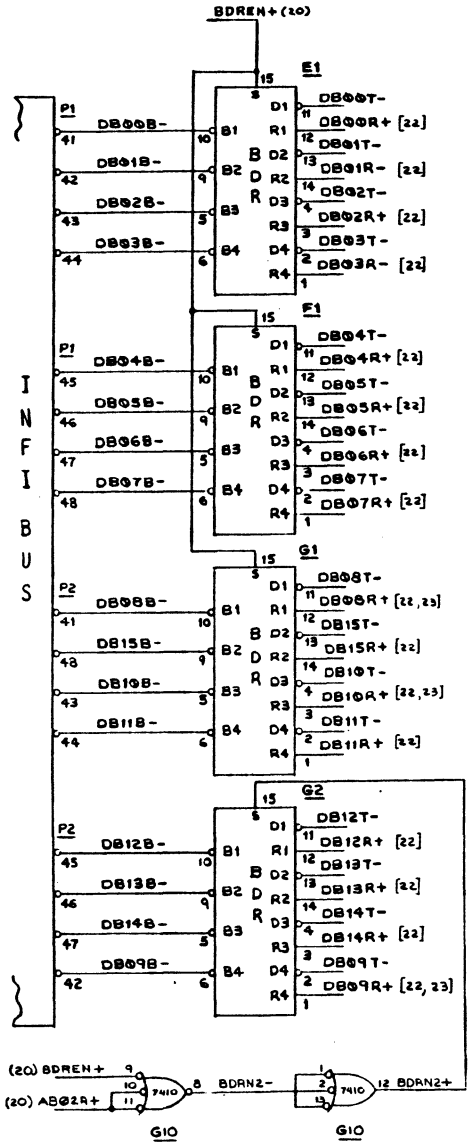
	REVISION		
APPD	SYM	DESCR	DATE
	A	REL PROD	8.24.75
	B	ECN0184	1.27.76
	C	ECN0188	2.6.76
	D	ECN0270	8.30.77

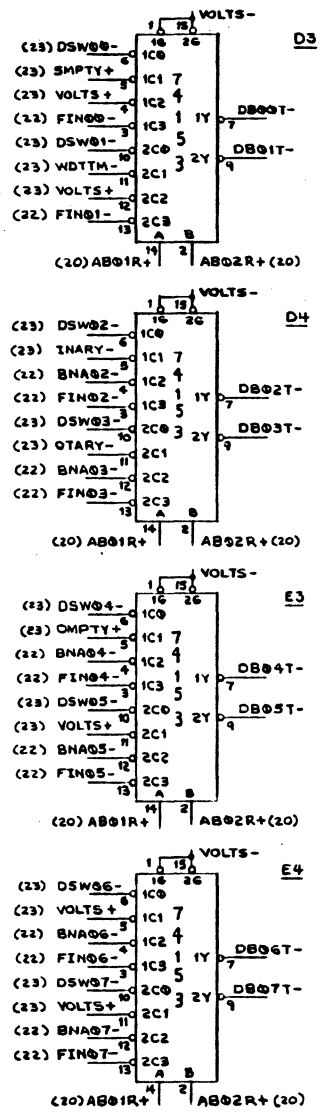
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

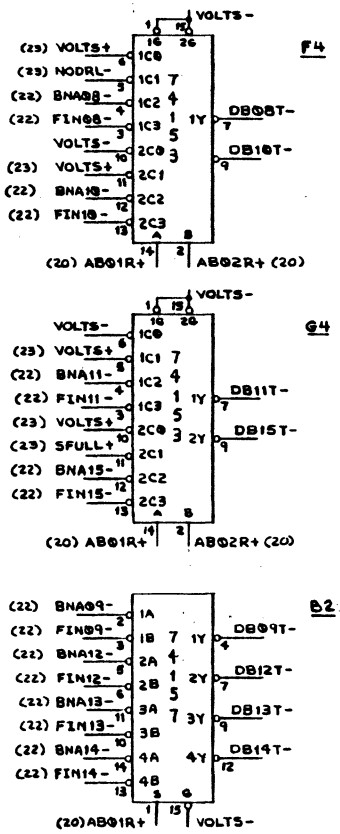
DRAWN	DRF	TITLE: SWITCHES, RESETS & SYNCRONIZERS
CHECKED		CUSTOMER NO. / BBN NO. / REV
APPROVED	JT 8/4/75	AML-23-WW D

AML

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	4-21-75
	B	ECN 0202	9.16.75
	C	ECN 0226	8 31-76
	D	ECN 0270	4.30.77

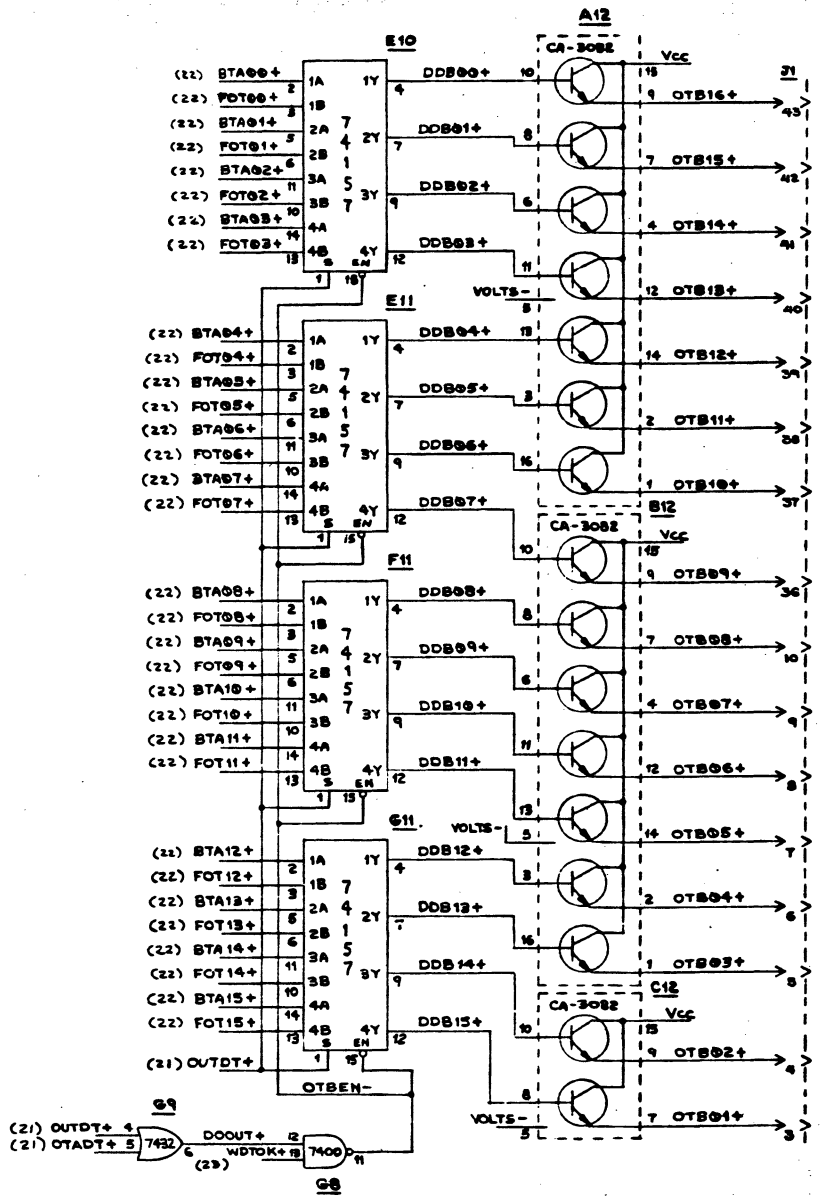






COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	7/3/75	TITLE: INFIBUS DATA
CHECKED			CUSTOMER NO. / DWG NO. / REV
APPROVED	[illegible]	[illegible]	AML-24-WW / D



REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	6-21-78

NOTES

1 - J2 1 → 55 TO VOLTS-

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	7/28	TITLE: MLC DATA
CHECKED			CUSTOMER NO.
APPROVED	[illegible]	6/6/75	DWG NO. AML-25-WW REV A

AML

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	1/19/76	

AMT

SEE _____

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 1/19/76

CHECKER

ENGINEER 2/24/76

APP'D FOR REL 2/24/76

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

AMT LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		AMT - Ø2

SCALE	REV	SHEET 1 OF 3

MLC ADAPTER TEST CARD - LOGIC DESCRIPTION

The Test Card for the MLC Adapter (AML) is a single card module (AMT) which is used to test an AML card. See the AML documentation and the AMT functional spec (HSMImp #297) for more information. All signals signed "+" are true when high, while those signed "-" are true when low. The hardware is initially assumed to be in the cleared state.

CONTROL LOGIC (AMT 20)

The three DMC enable switches SWINF, SWOIF and OTENB allow input, outin, and output operations, respectively, to take place between the AML and AMT. If output is enabled (OTENB true), FSTOT will initially be false. SLCLK (the system clock CLKAB divided by 10) increments the binary counter until MKDIL comes true. When this happens, DILEN gets set, disabling the counter, and SLCLK sets DLCLK. The next SLCLK sets LDOTF, raising DILOT to the AML. The AML will respond with DALOT which, as DDLOT, clears DILEN and DLCLK and the counter is once again enabled. DALOT also clears LDOTF. The assertion of ANYDL sets FSTOT since neither LDINF nor LDOIF is true. Now, if SWINF or SWOIF is true, the next occurrence of DLCLK allows SLCLK to set LDINF or LDOIF, respectively. These are cleared by DALIN or DALOI, respectively. Since one of these is set, ANYDL will clear FSTOT, after both LDINF and LDOIF have been cleared by being serviced by the AML. The next assertion of DLCLK sets LDOTF.

AMT

If OTENB is false initially, FSTOT is held true, and the first occurrence of DLCLK will enable setting LDINF or LDOIF, if the switches are enabled. When neither SWINF or SWDOF is true, FSTOT is held false. The FSTOT flop assures that when output is enabled, the output DMC operation will occur first and alternate with the input operations which makes possible true echoing.

The occurrence of any of the three DAL signals clears DILEN, turning off all DIL signals and enabling the counter. After 3.2

usec. MKDIL again comes true and DILEN goes true. However, if any of the three flops LDINF, LDOIF, or LDOTF is true, DLDTA will be false and DLCLK will not be set. This assures that DMC accesses will take place no more often than once every 3.2 usec, but no operation gets to repeat until all others pending have completed.

For an output, the AML asserts DALOT. When the AML asserts RRLIN, DDLOT and DORLN will both be true, raising CLKLD. The fall of this signal strobes the output data to the data register (BND$\emptyset\emptyset$-BND15 - AMT22). For an input, DDLIN true enables the data to the input bus (MUXEN, MXEN2 both true - AMT22). For an outin, DDLOI is true, enabling the high order eight data bits to the low order eight input bus bits. (MUXEN true - AMT22).

For an OTA operation, OTAGO is asserted by the AML. If the DRLIN switch is set (ENDRL true), LPDRL comes true. When RRLIN is asserted by the AML, LPOTA comes true, latching output data in the OTA register (BTA$\emptyset\emptyset$-BTA15 - AMT22). For an INA operation, INAGO will also be true, and LPINA will come true instead of LPOTA. This signal gates the OTA register to the input bus. (MUXEN and MXEN2 true - AMT21). The control logic is cleared only by MSTCL from the AML.

DATA DRIVERS AND RECEIVERS (AMT21)

Drivers and receivers are identical to those described in the AML logic description, with the exception that all lines are terminated in 150 ohms at the AMT.

Four way multiplexors feed to the low order input bus drivers. The select lines are DDLIN and DDLOI configured such that the multiplexor input 1 is unused, 2 is input data (DDLIN true), 3 is outin data (DDLOI true) and 4 is INA data (neither DDLIN or DDLOI true). The high order eight bits use two way multiplexors with LPINA as the select line. Input 1 is INA data and input 2 is input data. The multiplexors are enabled as described above.

DATA REGISTERS (AMT22)

These registers are loaded as described above. Note that both are operated with inverted input data and output taken from the $\overline{Q}$ outputs.

AMT-2Ø SCHEMATICS

12	11	10	9	8	7	6	5	4	3	2	1	
CA3082	74153	DRES	SWITCH									A
CA3082	74153	74157	74197	7404	7402							B
CA3082	74153	74175	74175	7474	7427	7408						C
TERM	74153	74175	74175	7474	7408	7408						D
TERM	7414	74175	74175	7474	7427							E
TERM	TERM	74175	74175	7411	74161							F
TERM	TERM	7414	7414	7414						74160	74504	G

REVISION

APPD	SYM	DESCR	DATE
	A	REL PROD	8-21-72

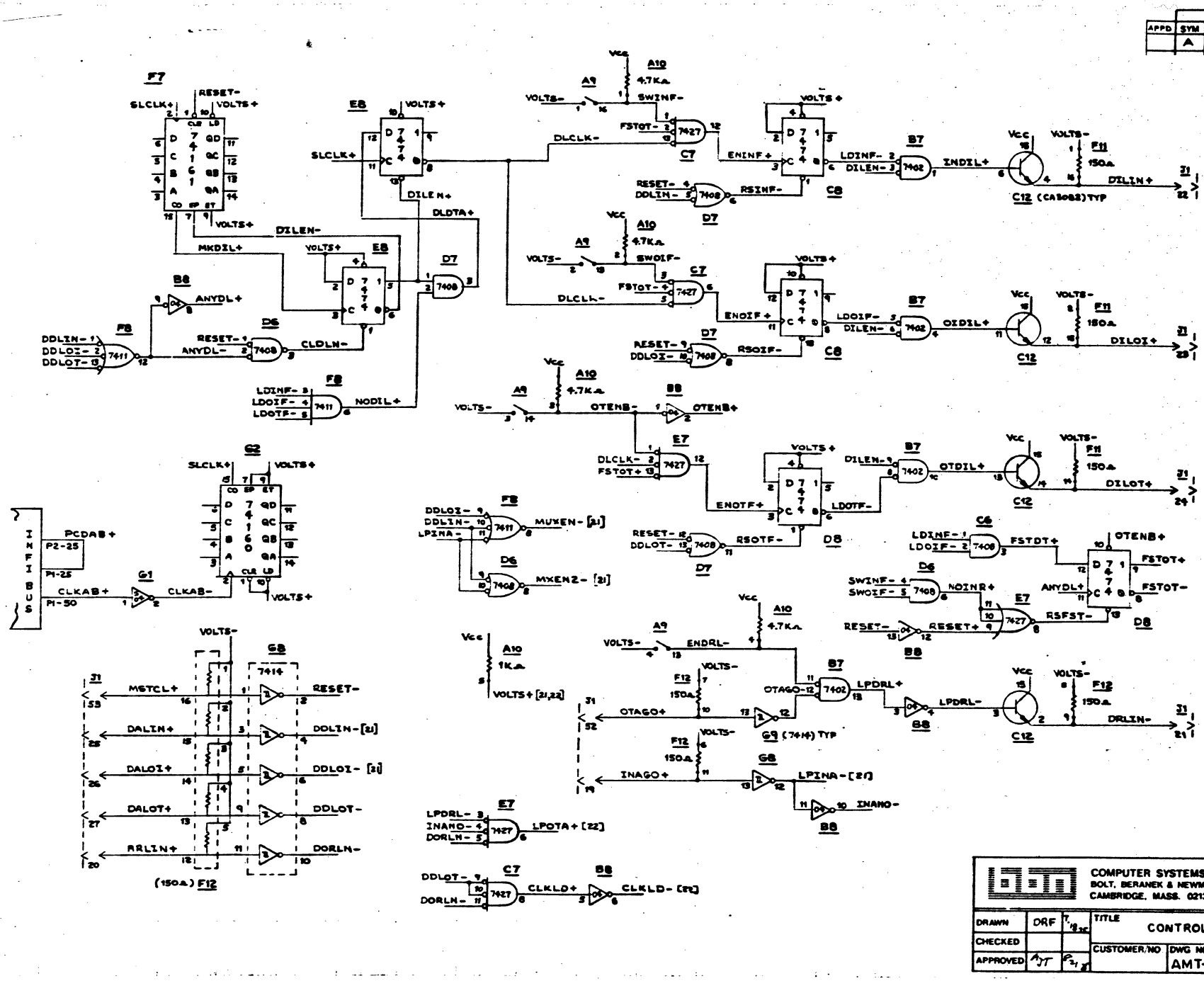
NOTES :

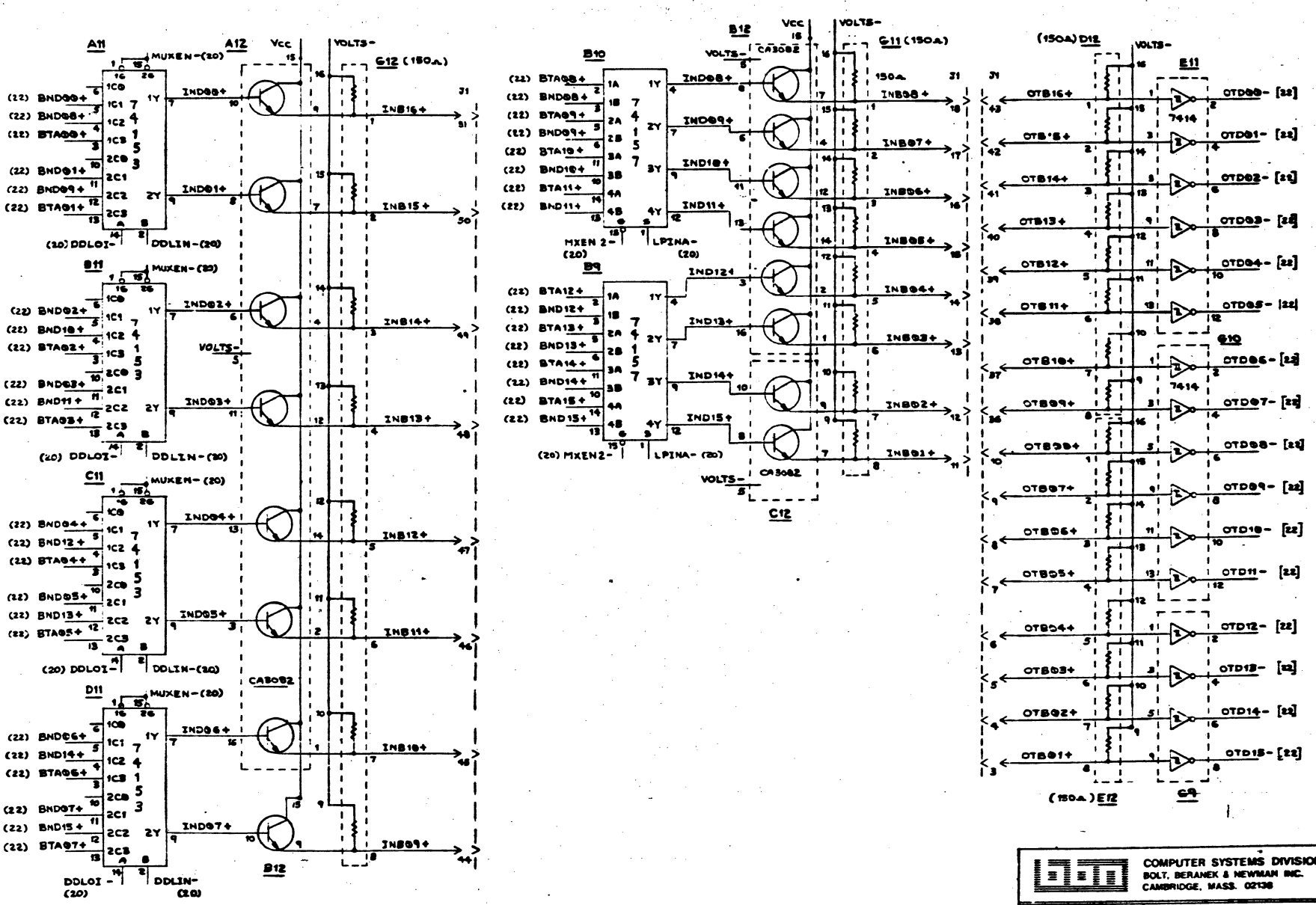
TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	S.E.T.	7/25/72	TITLE: INTEGRATED CIRCUIT LAYOUT
CHECKED			
APPROVED	RJT	7/27/72	CUSTOMER/NO. HSMIMP. / DWG NO AMTSS-WW / REV A

AMT


REVISION
APPD SYM DESCR DATE
A PEL PROD
F7
SLCLK+
RESET-
VOLTS+
DILEN-
MKDIL+
E8
DILEN+
DLDTA+
D7
7408
B8
ANYDL+
F8
DDLIN- [1]
DDLOI- [2]
DDLOT- [13]
7411
D6
RESET- [9]
ANYDL- [2]
CLDLN-
LDINF- [3]
LDOIF- [4]
LDOTF- [5]
NODIL+
A10
4.7KΩ
A9
VOLTS-
SWINF-
SWOIF-
OTENB-
OTENB+
C7
7427
DLCLK-
FSTOT- [4]
FSTOT+ [13]
E7
ENINF+
ENOIF+
ENOTF+
C8
B7
7402
LDINF- [2]
LDOIF- [5]
LDOTF- [9]
DILEN- [3]
INDIL+
OIDIL+
OTDIL+
F11
150Ω
C12 (CA3082) TYP
DILIN+
DILOI+
DILOT+
J1
22
23
24
RESET- [4]
DDLIN- [5]
RSINF-
DDLOI- [12]
RSOIF-
DDLOT- [12]
RSOTF-
G2
CLKAB+
CLKAB-
P2-25
P1-25
P1-50
INFI BUS
G1
PCDAB+
MUXEN- [21]
MXEN2- [21]
C6
LDINF- [1]
LDOIF- [2]
FSTDT+
FSTOT+
FSTOT-
D6
SWINF- [4]
SWOIF- [5]
NOINR+
ANYDL+
RSFST-
D8
RESET+
B8
ENDRL-
1KΩ
VOLTS+ [21,22]
F12
OTAGO-12
OTAGO+
INAGO+
LPDRL+
LPDRL-
DRLIN-
G9 (7414) TYP
G8
LPINA- [21]
INAMO-
LPDRL- [3]
INAMO- [4]
DORLN- [5]
LPOTA+ [22]
CLKLD+
CLKLD- [21]
MSTCL+
DALIN+
DALOI+
DALOT+
RRLIN+
RESET-
DDLIN- [21]
DDLOI- [21]
DDLOT-
DORLN-
(150Ω) F12
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF
CHECKED
APPROVED
TITLE
CONTROL LOGIC
CUSTOMER/NO
DWG NO.
AMT-20-WW
REV
A



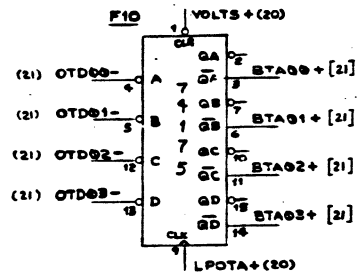
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	

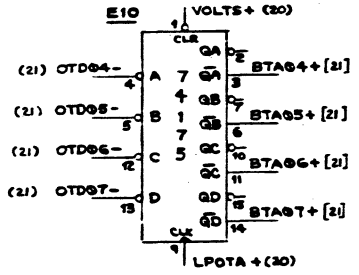
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

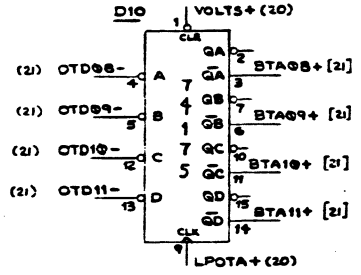
DRAWN	DRF		TITLE: DATA PATHS
CHECKED			CUSTOMER/NO.
APPROVED			DWG NO. AMT-21-WW REV A

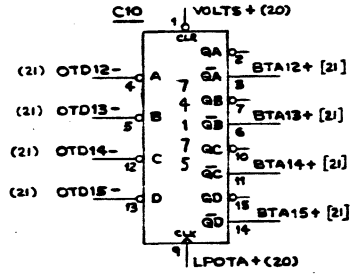
AMT

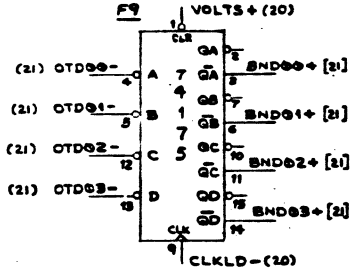
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	8-[illegible]-75

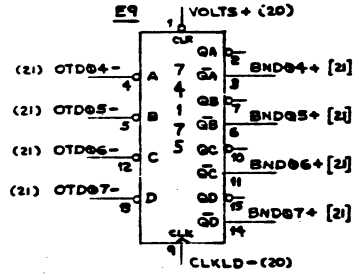


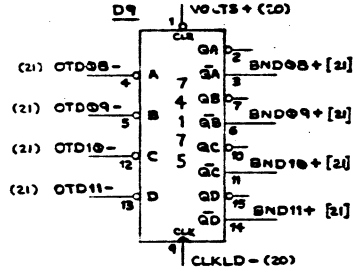


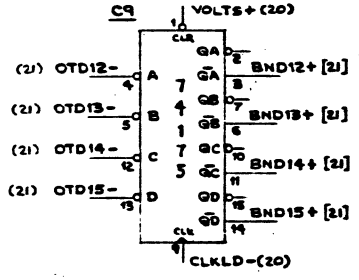












COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	7/15/75	TITLE: DATA REGISTER
CHECKED			CUSTOMER NO. / DWG NO. AMT-22-WW / REV A
APPROVED	[illegible]	[illegible]	

Bus Coupler I/O

BCI-Ø5 Technical Reference

BCI-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED FOR PRODUCTION		
B	ECN 0060	8/30/74	MFK

BCI

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER 11/6/76 AMM

APP'D FOR REL 11/6/76 AMM

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BCI TECHNICAL REFERENCE

SIZE	CODE IDENT NO.	DRAWING NO.
A		BCI-05

SCALE	REV	SHEET 1 OF 2

BCI - Bus Coupler I/O Card BBN

see BCM

Status - address none

Switches - none

Jumpers

Parity	Connect	
	From	To
WRITE SOURCE GENERATE (Classical)	F6-2 G10-1 G10-3	F6-15 G10-15 G10-14
WRITE SOURCE CHECK (Feedback)	G10-2 F6-2	G10-15 F6-15
NONE	G10-4	G10-13

BCI

BCI-2Ø SCHEMATICS

13	12	11	10	9	8	7	6	5	4	3	2	1	
TERM		BDR CAB00+ ↓ CAB03+	BDR CAB04+ ↓ CAB07+			74S64 RAB03- RAB04- RAB09- RAB00- PARHI+	74S133 IOSPC-	74S280 ABPLO+			BDR AB16- ↓ AB19-	BDR AB00- ↓ AB03-	
TERM		BDR CAB08+ ↓ CAB11+	BDR CAB12+ ↓ CAB15+			7474 QUITT-	74S175 REQST+ HCYCF+	74S00 BYT00- BOKHI+ DONET- PAROK-	74S280 ABPHI+			BDR AB04- ↓ AB07-	B
TERM		BDR CAB16+ ↓ CAB19+	BDR CPBLO+ CPBHI+			74S04 CQUTR- BYTER- LHOLD- LHCYC- CDAEN-	RESISTOR 4.1K IGPAR- CHKPR- C614+	74S86 ADPAR+ OKLO+		74S86 OKHI- DBPLO+ PARHI- PARLO-	BDR AB12- ↓ AB15-	BDR AB08- ↓ AB11-	C
TERM E PWR SENSE		BDR CDONE- CQUIT- CTREQ-	9615 PWRTS+			74S74 IDAEN+ RITE+	74S00 RDDON- RISET- DNDLA+ DNDLA-	74123 DONGO+				BDR RITE- BYTE- HCYC- STRB-	D
TERM		BDR CDA12+ ↓ CDA15+	BDR CHCYC+ CBYTE+ CRITE-								BDR QUIT- MRES- HOLD- DONE-	BDR DB03- ↓ DB00-	E
TERM		BDR CDA04+ ↓ CDA07+	BDR CDA08+ ↓ CDA11+			74S10 DLSTR- OK+ GOTDN-	RACCP 390 Ppd	RESISTOR 1K FS01+ FS02+ AS01+ AS02+ VOLTS+	7403 FS01+ FS02+ AS01+ AS02+	74S280 RPBLO+	74S280 RPBHI+	BDR DB07- ↓ DB04-	F
TERM		BDR CDA00+ ↓ CDA03+	PARITY JUMPERS CDAEN+ VOLTS- PAREN+ CDAEN- VOLTS- CHKPR- IGPAR-			74S11 STPWR+ CDAEN+					BDR DB15- ↓ DB12-	BDR DB11- ↓ DB08-	G

APPD	SYM	REVISION DESCR	DATE
	A	REL PROD	5.23.73
	B	SEE DCR 3	9.11.73
	C	ECN 0010	3.4.74
	D	ECN 0058	5.8.74
	A		
	E	ECN 0181	11.1.78

NOTES

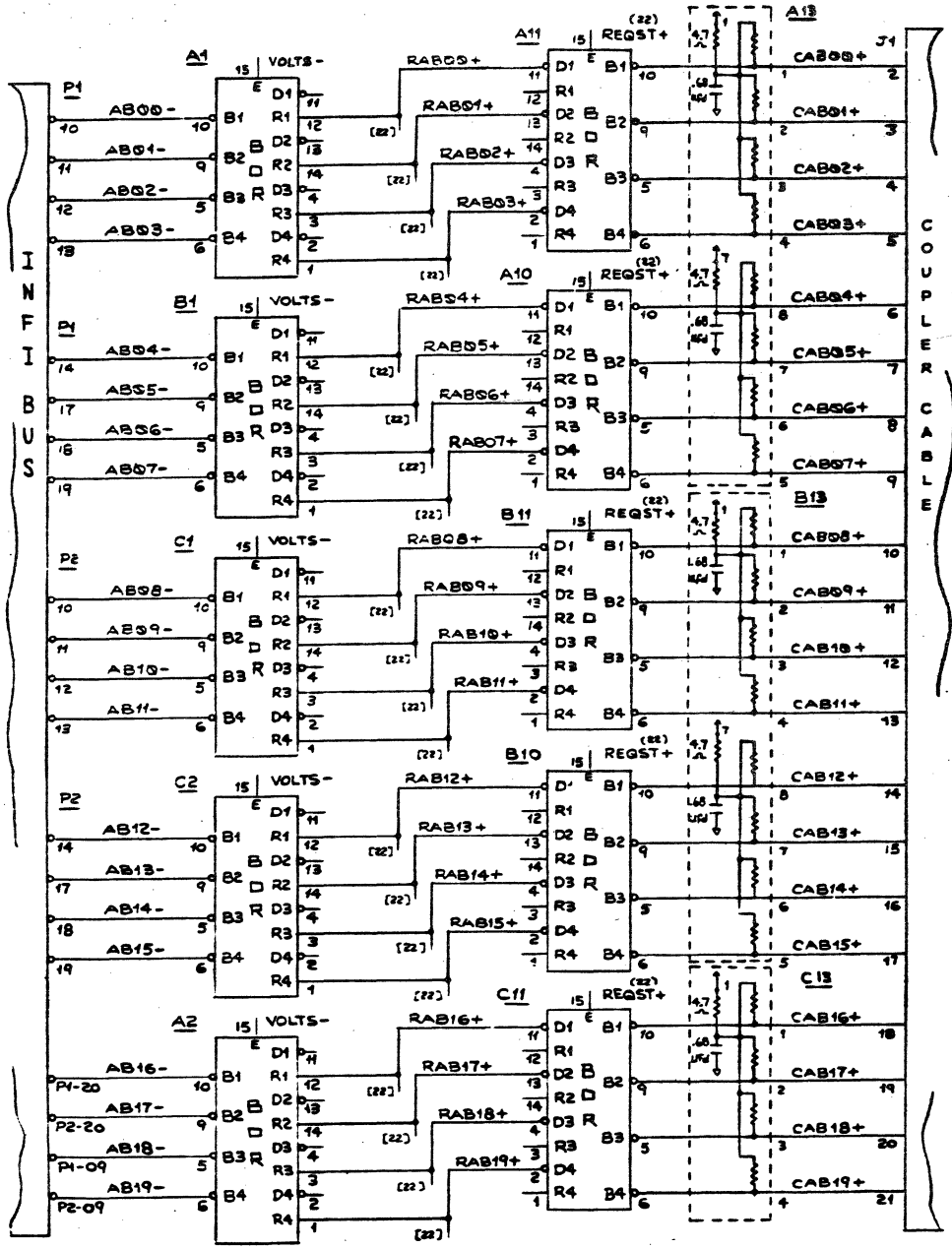
1

TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/23/74	TITLE: INTEGRATED CIRCUIT LAYOUT
CHECKED			
APPROVED		5/24/74	CUSTOMER/NO.: HSMIMP; DWG NO.: BC I-00-WW; REV: E

BCI

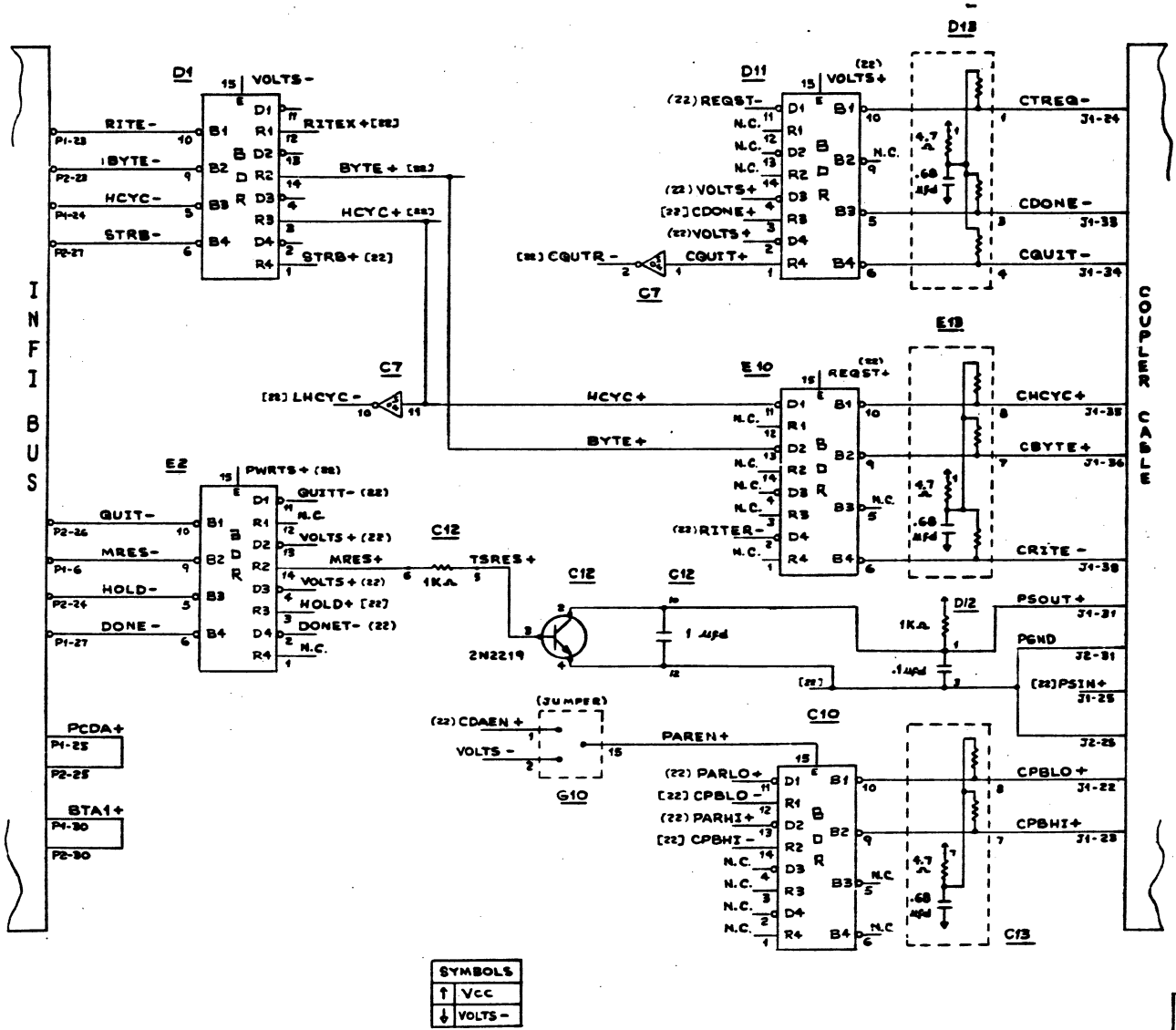


REVISION			
APPD	SYM	DESCR	DATE
	A	REL for PROD	5-23-78
	B	SEE DCR#3	7-14-78
	C	ECN#0040	8.1.79
	D	ECN#0050	9.13.79

SYMBOLS	
↑	Vcc
↓	VOLTS-

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/23/78	TITLE: B C I ADDRESS
CHECKED	DRF	7/21/78	CUSTOMER NO.: HSMIMP
APPROVED	[illegible]	5-31-79	DWG NO.: BCI-20-WW
			REV: D



REVISION			
APPD	SYM	DESCR	DATE
	A	REL for PROD	5.24.73
	B	DCR # 3	9.6.73
	C	ECN #0040	3.1.74
	D	ECN #0050	3.13.74
	E	ECN 0181	12.9.75

JUMPERS

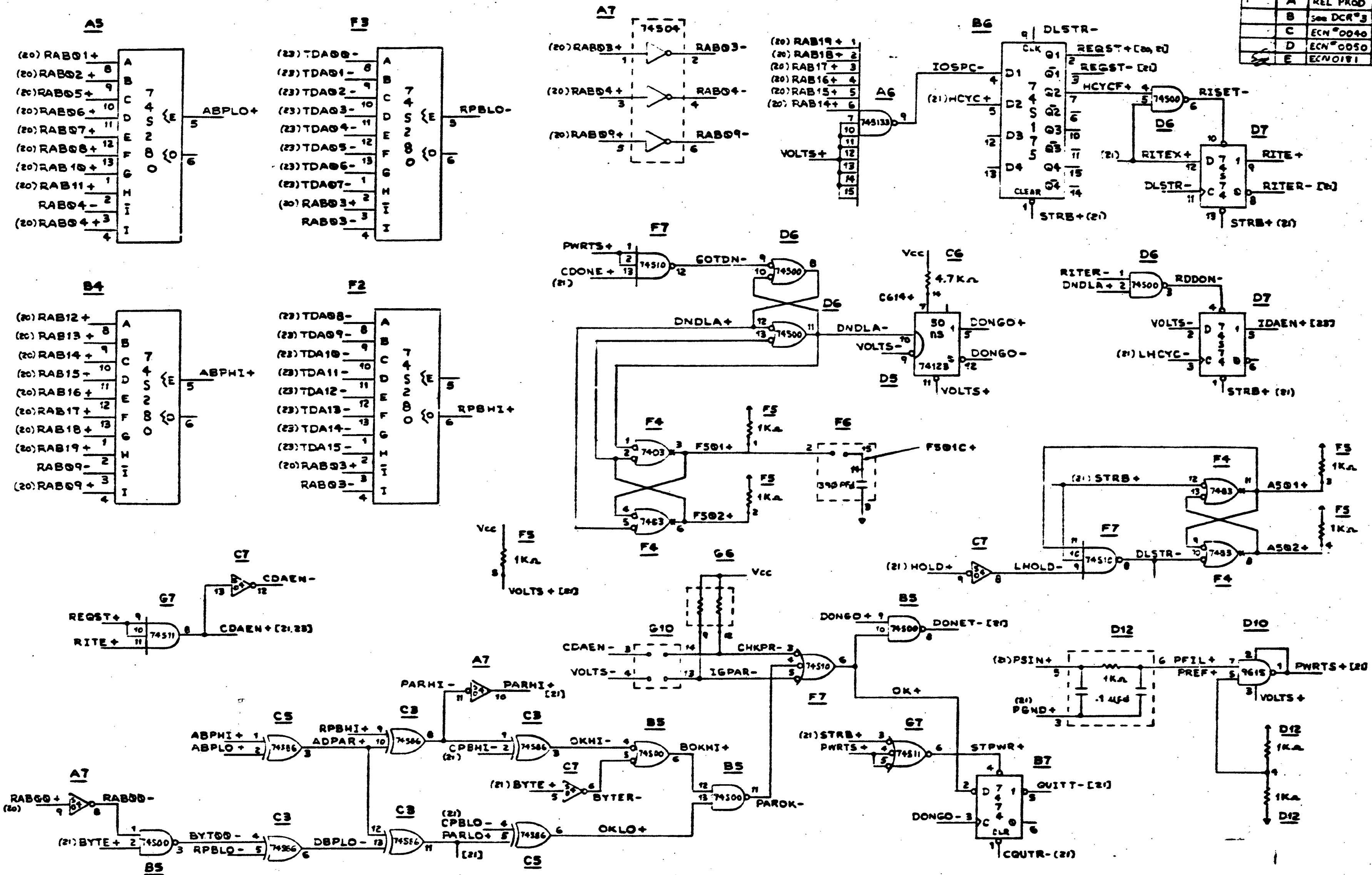
PARITY	CONNECT FROM	CONNECT TO
WRITE SOURCE GENERATE (classical)	G10-1 G10-3 F6-2	G10-15 G10-14 F6-15
WRITE SOURCE CHECK (feedback)	G10-2 F6-2	G10-15 F6-15
NONE	G10-4	G10-13

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/24/73	TITLE	BCI CONTROL LINES
CHECKED	DRF	7/31/73	CUSTOMER NO	DWG NO. / REV
APPROVED	Axm	3/3/75	HSMIMP	BCI-21-WW / E

BCI

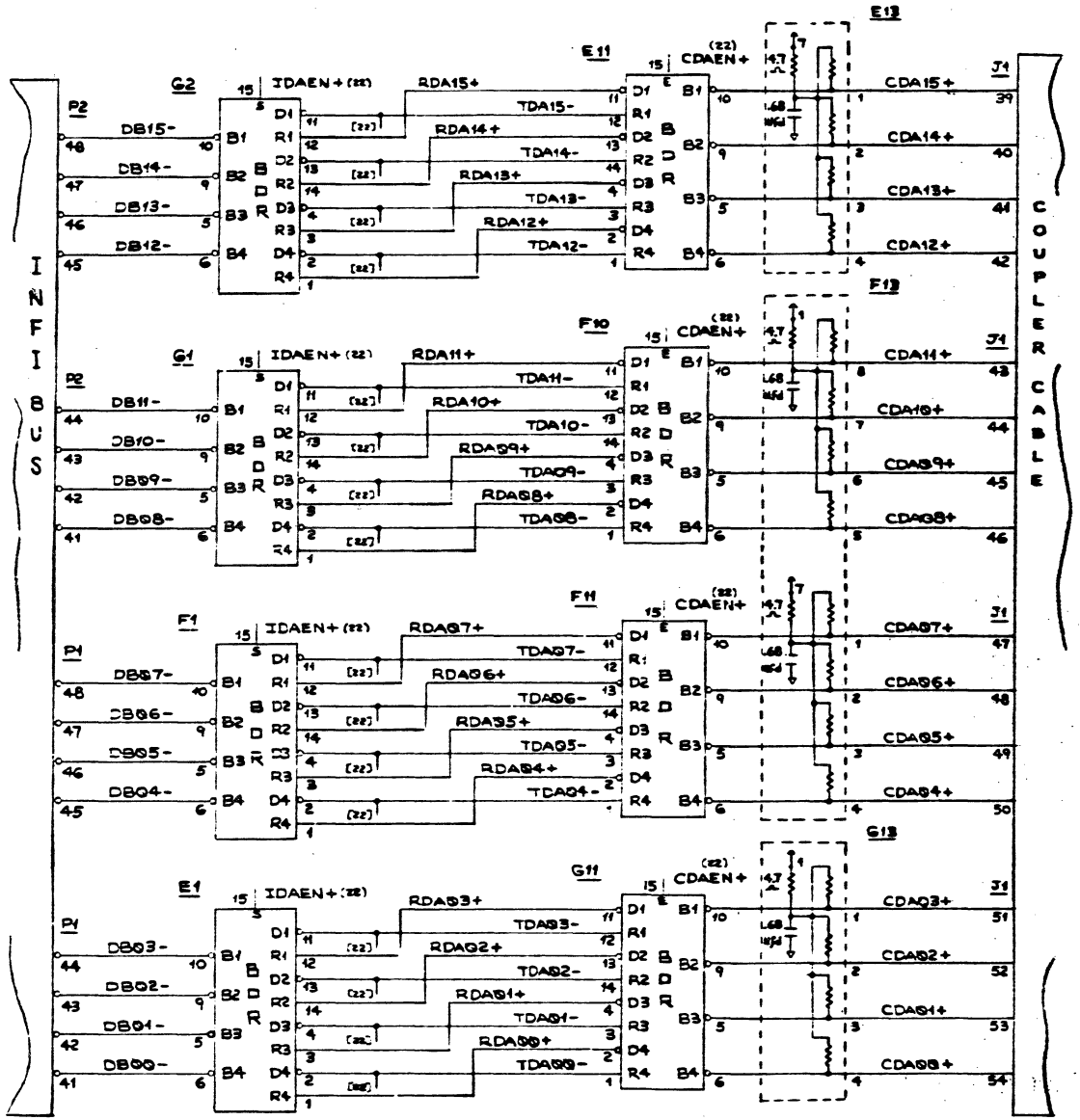
APPD	SYM	REVISION DESCR	DATE
	A	REL PROD	3.25.73
	B	See DCR #3	7.8.73
	C	ECN #0040	2.4.74
	D	ECN #0050	5.21.74
	E	ECN 0181	12.9.75



SYMBOLS	
↑	Vcc
⏚	VOLTS-

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	3/8/73	TITLE: CONTROL & PARITY LOGIC
CHECKED	DRF	3/31/73	CUSTOMER NO.: HSMIMP
APPROVED	[illegible]	3/31/73	DWG NO.: BCI-22-WW — REV E



	REVISION		
APPD	SYM	DESCR	DATE
	A	REL. PROD	5-21-73
	B	SEE DCR#3	7-6-73
	C	ECN#0040	3-4-74
	D	ECN#0050	3-22-74

SYMBOLS	
↑	Vcc
↓	VOLTS-

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	5/29/73	TITLE: DATA LINES	
CHECKED	DRF	5/31/73	CUSTOMER NO. HSMIMP	DWG NO. BCI-23-WW, REV D
APPROVED	[illegible]	3/24/75		

BCI

Bus Coupler Memory

BCM-Ø5 Technical Reference

BCM-2Ø Schematics

BCM

APPLICATION

NEXT ASSY	USED ON

LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PROJECTION		

BCM

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL 1/10/76

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BCM TECHNICAL REFERENCE

SIZE	CODE IDENT NO.	DRAWING NO.
A		BCM-05

SCALE | REV A | SHEET 1 OF 2

BCM - Bus Coupler Memory Card BBN

See BCP, BCI

Status - address none

W

R

Switches

Address Recognized

19	18	17	16	15	14	12	11	
1	1	1	1	1	1	1	1	(A)
1	1	1	1	1	1	1	1	(B)

Address Bits Checked

Bus Coupler Switch Address

6	5	4	3	2	1	x	

Set if memory bus

For each address bit position the following table applies:

Value	A	B
Ø	off	on
1	on	on
Don't care	-	off

BCM

Jumpers

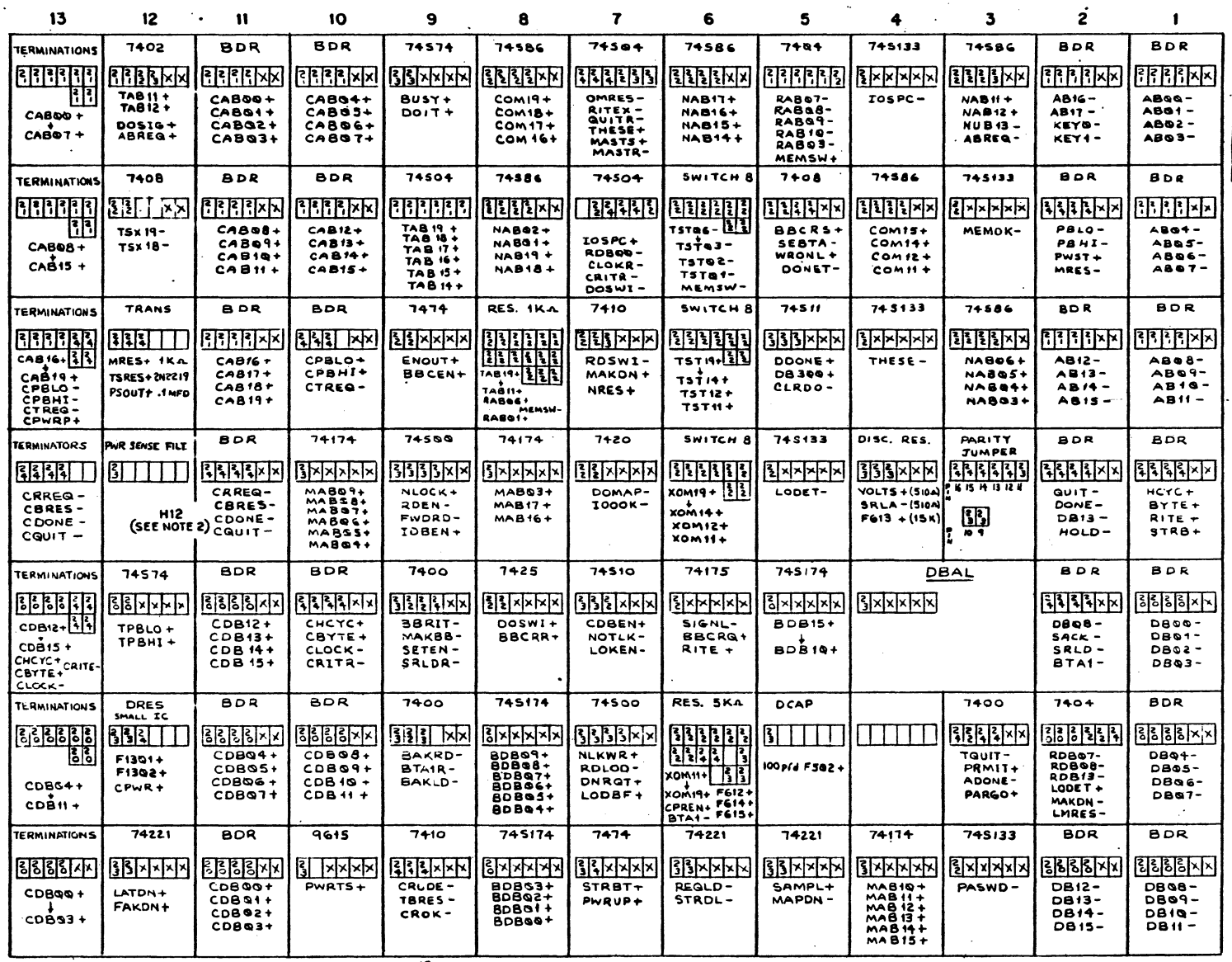
Parity	Connect From	Connect To
WRITE SOURCE GENERATE (Classical)	D3-15 D3-12	D3-16 D3-13
WRITE SOURCE CHECK (Feedback)	D3-14	D3-16

Done Pulse	Connect From	Connect To
normal	D3-11	D3-10
delayed*	D3-9	D3-10

* with the PAR card

BCM

BCM-2Ø SCHEMATICS



REVISION			
	SYM	DESCR	DATE
APPD	A	REL PROD	4.16.73
	B	DCR#1	7.25.73
	C	ECN#2	8.9.73
	D	ECN#6	8.9.73
	E	ECN#0028	2.28.74
	F	ECN#0065	4.19.74
	G	ECN 0086	10.3.74
MFK	H	ECN 0114 ECN 0115	12.18.74
MFK	I	ECN 0130	1.30.75
DK	J	ECN 0229	9.13.76

NOTES

1 - TWISTED PAIR W.W. BUS BAR, VERSION

2 - H12 (SHOWN) IS LOCATED BETWEEN D11 & D12 →

12

7408

TSX17-
TSX16-
TSX15-
TSX14-

H

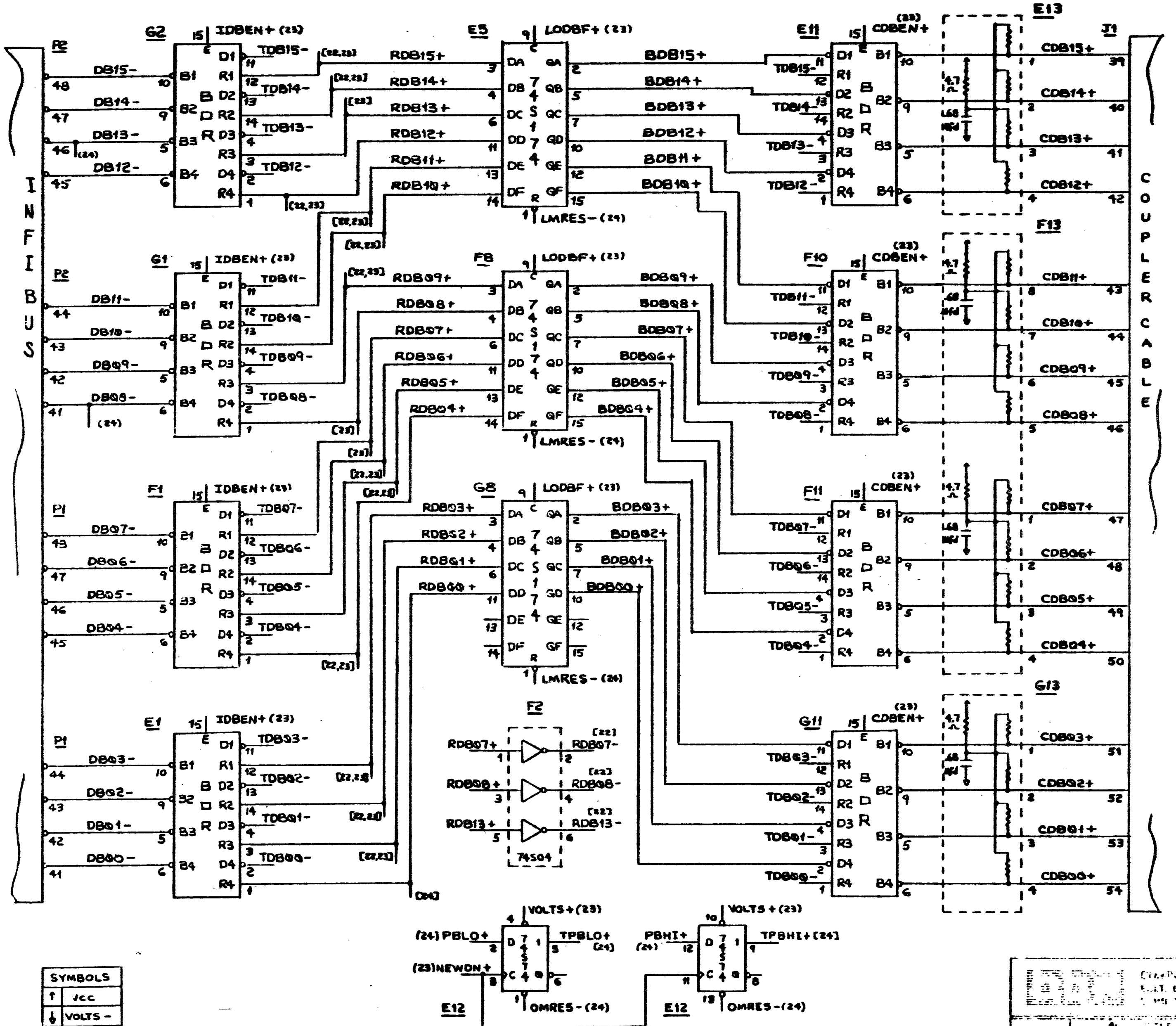
TOP VIEW

BOLT, BERANEK & NEWMAN INC.
COMPUTER SYSTEMS DIVISION
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/25/73	TITLE: INTEGRATED CIRCUIT LAYOUT
CHECKED			
APPROVED	(illegible)	8/31/73	CUSTOMER/NO.: HSMIMP; DWG NO.: BCM-00-MW; RFV: J

BCM

APPD	SYM	DESCR	DATE
[illegible]	A	REL. for PROD	4-17-73
[illegible]	B	DCR #1	7-24-73
[illegible]	C	ECN #2	[illegible]
[illegible]	D	ECN # 6	[illegible]
[illegible]	E	ECN #0025	[illegible]
[illegible]	F	ECN 0115	[illegible]
[illegible]	G	ECN 0326	[illegible]



COMPUTER SYSTEMS DIVISION

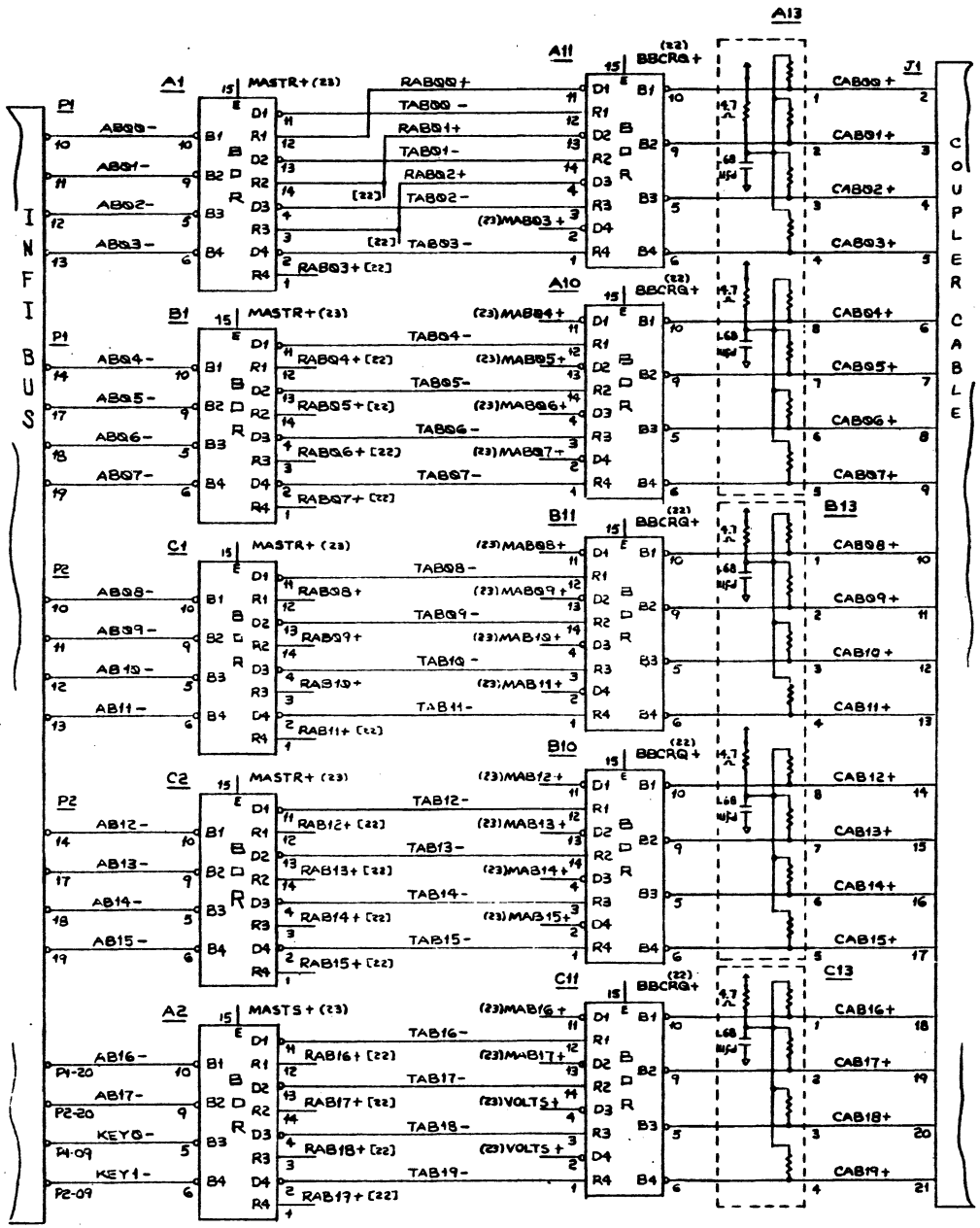
DRAWN DRF

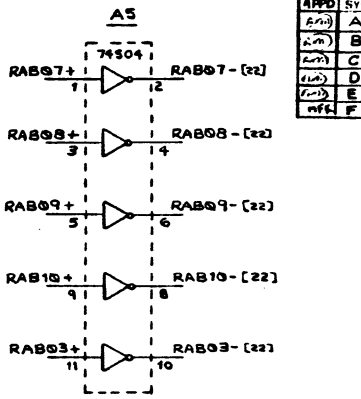
CHECKED DRF

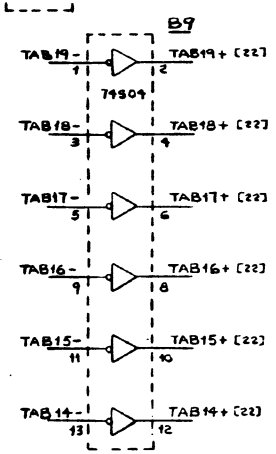
APPROVED

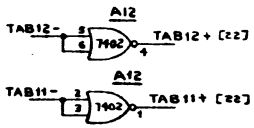
DATA BUS AND READ BUFFER REGISTER

HSMIMP BCM-20-MW G









REVISION			
APPD	SYM	DESCR	DATE
	A	REL for PROD	9.17.79
	B	DCR # 1	7-26-79
	C	ECN # 2	10.9.79
	D	ECN # 6	11.9.79
	E	ECN #0028	2.26.80
	F	ECN 0114	12.18.80

SYMBOLS	
↑	Vcc
↓	VOLTS-

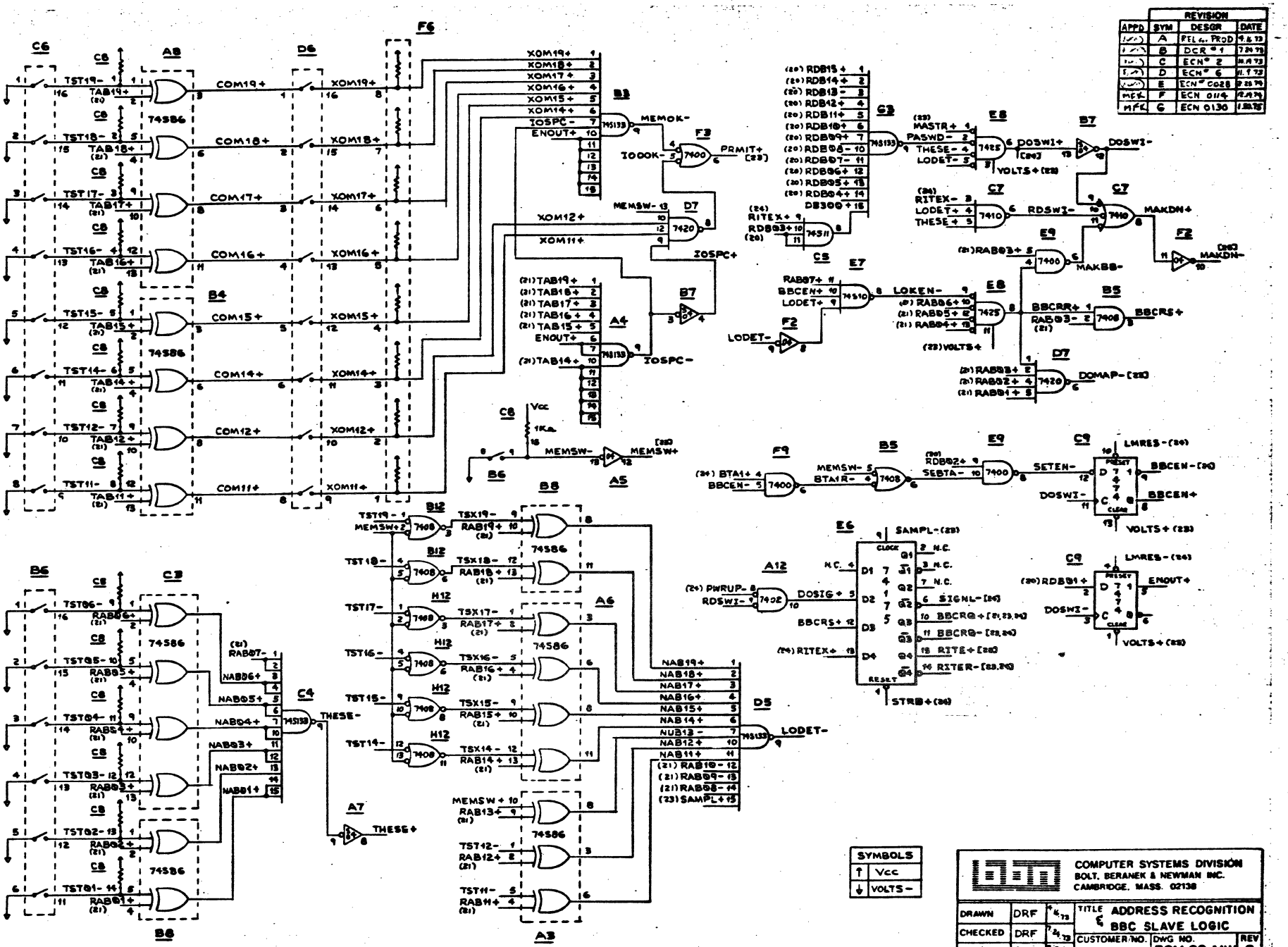
COMPUTER SYSTEMS DIVISION

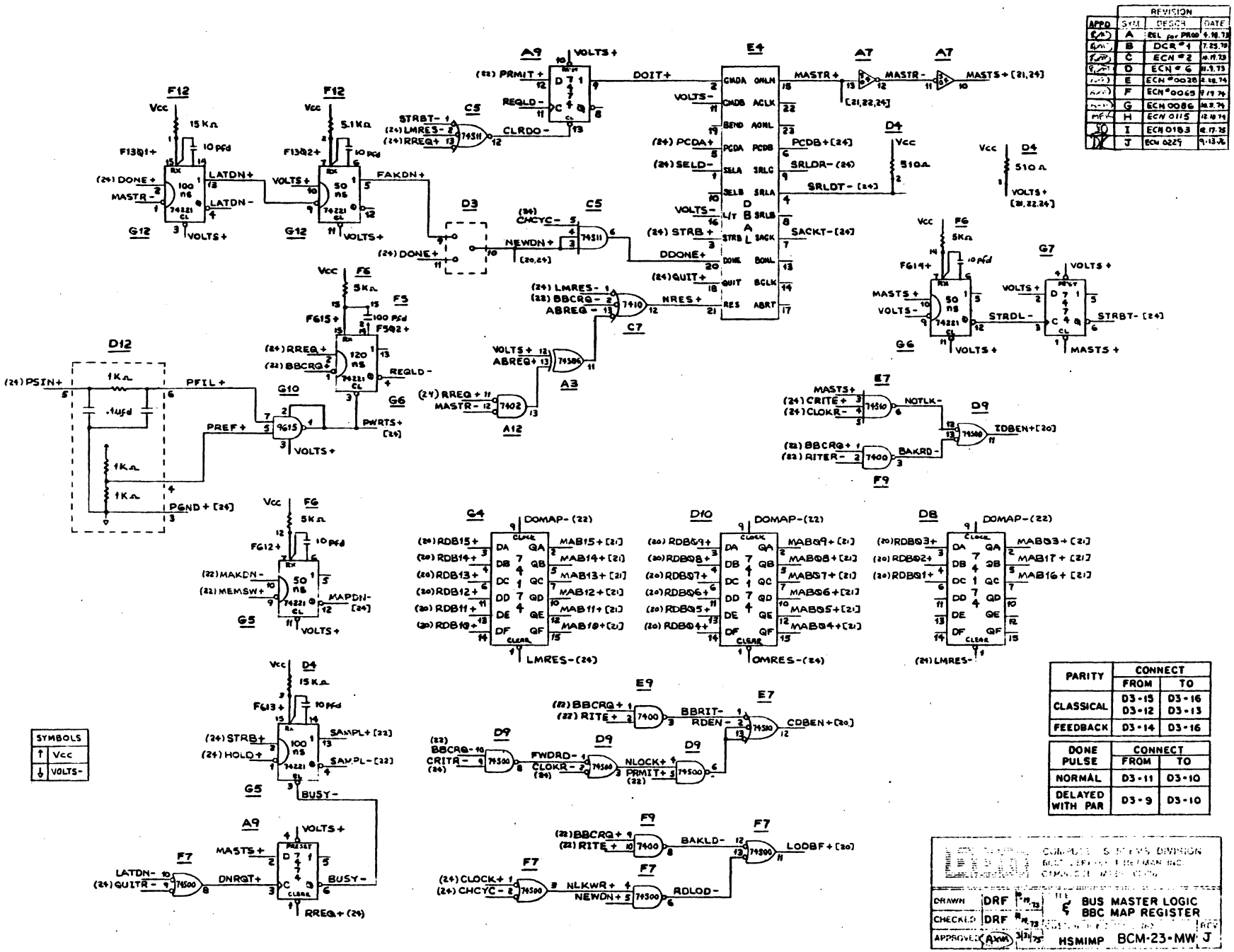
DRAWN	DRF	4/11/79
CHECKED	DRF	4/24/79
APPROVED		5/3/79

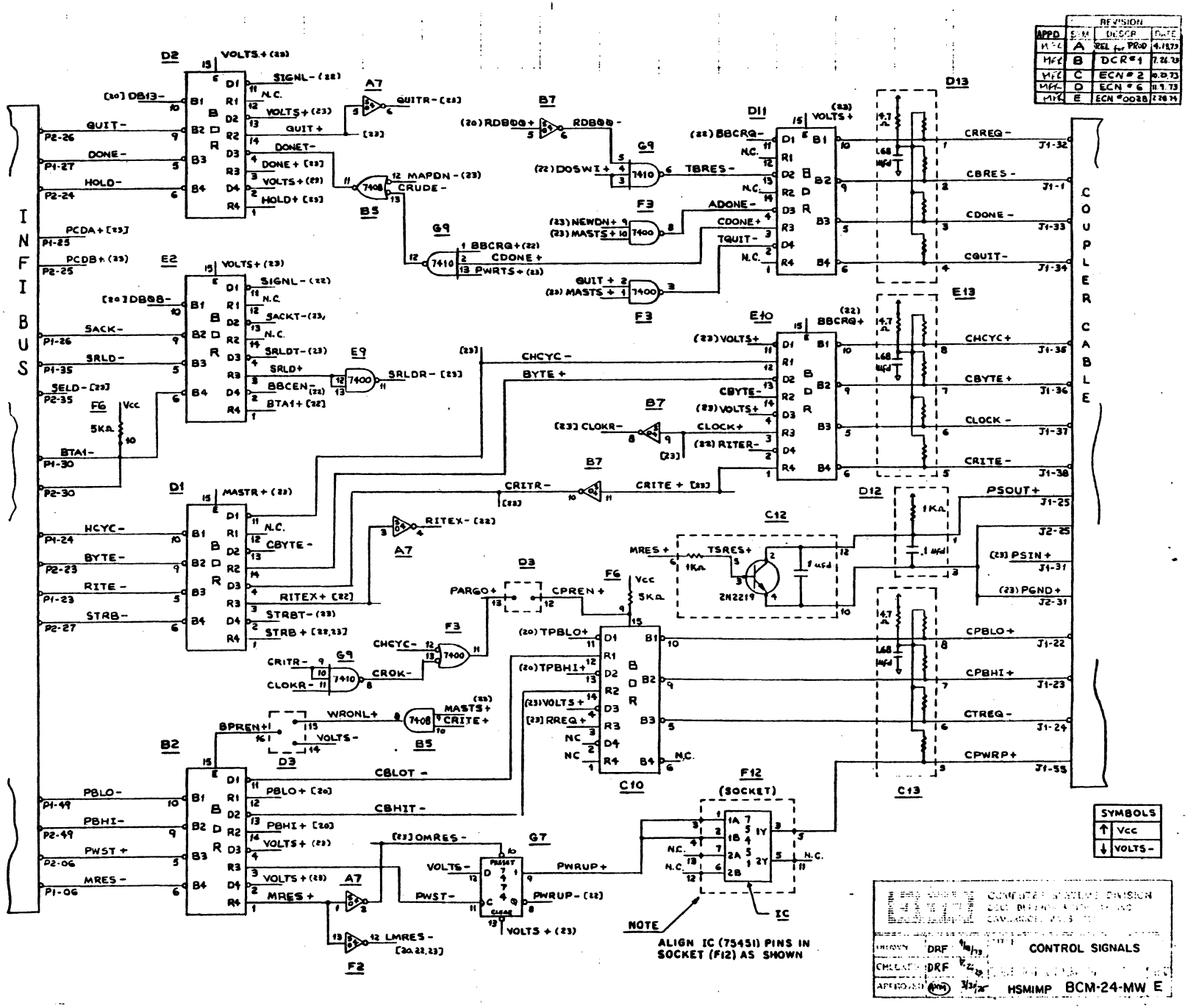
ADDRESS BUS

HSMIMP BCM-21-MW F

BCM


REVISION
APPD | SYM | DESCR | DATE
A | PRELIM. PROD | 9.6.73
B | DCR #1 | 7.24.73
C | ECN # 2 | 11.9.73
D | ECN # 6 | 11.7.73
E | ECN # 0028 | 2.25.74
MFG | F | ECN 0114 | 8.9.74
MFG | G | ECN 0130 | 1.28.75
SYMBOLS
Vcc
VOLTS-
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF 4/4/73
CHECKED DRF 7/24/73
APPROVED 3/31/75
TITLE ADDRESS RECOGNITION & BBC SLAVE LOGIC
CUSTOMER NO. HSMIMP
DWG NO. BCM-22-MW
REV G


REVISION
APPD SYM DESCR DATE
A REL for PROD 6.18.73
B DCR # 1 7.25.73
C ECN # 2 10.17.73
D ECN # 6 11.1.73
E ECN # 0026 2.18.74
F ECN # 0065 7.19.74
G ECN 0086 10.3.74
H ECN 0115 12.18.74
I ECN 0183 6.17.75
J ECN 0225 9.13.76
F12
Vcc
15 KΩ
10 pfd
F13Q1+
(24) DONE +
MASTR -
LATDN+
LATDN -
VOLTS+
G12
5.1 KΩ
F13Q2+
VOLTS+
FAKDN+
A9
VOLTS+
(22) PRMIT +
REQLD -
DOIT+
C5
STRBT- 1
(24) LMRES- 2
(24) RREQ+ 13
74S11
CLRDO -
E4
CMDA CMLN
CMDB ACLK
BEND AONL
PCDA+ (24)
PCDB
SELA SRLC
SELB SRLA
L/T B SRLB
A
L
STRB +
DONE BONL
QUIT BCLK
NRES +
RES ABRT
DOIT+
VOLTS-
SELD-
VOLTS-
STRB +
DDONE+
QUIT+
A7
MASTR+
MASTR-
MASTS+ (21,24)
[21,22,24]
D4
Vcc
510 Ω
PCDB+ (24)
SRLDR- (24)
SRLDT- (24)
VOLTS+ (21,22,24)
D3
(24) DONE +
C5
(24) CMCYC- 5
74S11
NEWDN+
(20,24)
SACKT- (24)
F6
5 KΩ
F615+
100 pfd
F5
F5Q2+
(24) RREQ +
(22) BBCRQ +
920 ns
REQLD -
G6
PWRTS+ (24)
(24) LMRES- 1
(22) BBCRQ- 2
ABREQ - 13
7410
NRES +
C7
VOLTS+ 12
ABREQ+ 13
7408
A3
(24) RREQ + 11
MASTR - 12
7402
A12
D12
(24) PSIN+
1 KΩ
.1 μfd
PFIL+
PREF+
9615
VOLTS+
1 KΩ
1 KΩ
PGND+ (24)
G10
F6
5 KΩ
FG14+
10 pfd
50 ns
MASTS+
VOLTS-
STRDL-
G6
G7
VOLTS+
STRBT- (24)
MASTS+
E7
MASTS+
(24) CRITE+ 3
(24) CLOKR- 4
74S10
NOTLK-
D9
74S00
IDBEN+ (20)
(22) BBCRQ+ 1
(22) RITER- 2
7400
BAKRD-
F9
F6
5 KΩ
FG12+
10 pfd
(22) MAKDN-
(22) MEMSW+
50 ns
MAPDN- (24)
G5
VOLTS+
G4
DOMAP- (22)
CLOCK
(20) RDB15+
(20) RDB14+
(20) RDB13+
(20) RDB12+
(20) RDB11+
(20) RDB10+
DA QA
DB QB
DC QC
DD QD
DE QE
DF QF
CLEAR
MAB15+ (21)
MAB14+ (21)
MAB13+ (21)
MAB12+ (21)
MAB11+ (21)
MAB10+ (21)
LMRES- (24)
D10
DOMAP- (22)
(20) RDB09+
(20) RDB08+
(20) RDB07+
(20) RDB06+
(20) RDB05+
(20) RDB04+
MAB09+ (21)
MAB08+ (21)
MAB07+ (21)
MAB06+ (21)
MAB05+ (21)
MAB04+ (21)
OMRES- (24)
D8
DOMAP- (22)
(20) RDB03+
(20) RDB02+
(20) RDB01+
MAB03+ (21)
MAB17 + (21)
MAB16+ (21)
(24) LMRES-
D4
15 KΩ
FG13+
10 pfd
(24) STRB+
(24) HOLD+
100 ns
SAMPL+ (22)
SAMPL- (22)
G5
BUSY-
SYMBOLS
↑ Vcc
↓ VOLTS-
E9
(22) BBCRQ+ 1
(22) RITE + 2
7400
BBRIT-
RDEN - 2
E7
74S30
CDBEN+ (20)
D9
(22) BBCRQ- 10
CRITR - 9
74S00
FWDRD- 1
CLOKR - 2
(24)
74S40
NLOCK+ 4
PRMIT+ 5
(22)
74S00
F9
(22) BBCRQ+ 9
(22) RITE + 10
7400
BAKLD- 12
F7
74S00
LODBF+ (20)
F7
(24) CLOCK+ 1
(24) CMCYC- 2
74S00
NLKWR+ 4
NEWDN+ 5
74S00
RDLOD-
A9
VOLTS+
MASTS+
LATDN- 10
(24) QUITR - 9
F7
74S00
DNRQT+
BUSY-
RREQ+ (24)
PARITY
CONNECT
FROM TO
CLASSICAL D3-15 D3-16
D3-12 D3-13
FEEDBACK D3-14 D3-16
DONE PULSE
CONNECT
FROM TO
NORMAL D3-11 D3-10
DELAYED WITH PAR D3-9 D3-10
COMPUTER SYSTEMS DIVISION
DRAWN DRF
CHECKED DRF
APPROVED
BUS MASTER LOGIC
BBC MAP REGISTER
HSMIMP BCM-23-MW J
BCM


INFIBUS
COUPLER CABLE
REVISION
APPD
SYM
DESCR
DATE
A
REL for PROD
4.18.73
B
DCR #1
7.26.73
C
ECN # 2
10.10.73
D
ECN # 6
11.9.73
E
ECN #0028
2.28.74
D2
D1
D11
D13
E2
E10
E13
D12
C12
D3
F6
F3
G9
B7
A7
B5
B2
D1
C10
C13
F12
(SOCKET)
G7
F2
E9
F5
B5
VOLTS+ (23)
SIGNL- (22)
QUITR- (22)
QUIT+ (23)
DONE+ (23)
VOLTS+ (23)
HOLD+ (23)
MAPDN- (23)
CRUDE-
RDBSO+
RDBSO-
DOSWI+
TBRES-
NEWDN+
MASTS+
ADONE-
CDONE+
TQUIT-
QUIT+
MASTS+
BBCRQ+
CDONE+
PWRTS+ (23)
BBCRQ-
VOLTS+ (23)
CRREQ-
CBRES-
CDONE-
CQUIT-
SIGNL- (22)
SACKT- (23)
SRLDT- (23)
SRLD+
BBCEN-
BTA1+ (22)
SRLDR- (23)
CHCYC-
BYTE+
CBYTE-
VOLTS+ (23)
CLOCK+
RITER-
CLOKR-
CRITE+ (23)
CRITR-
CHCYC+
CBYTE+
CLOCK-
CRITE-
MASTR+ (23)
CBYTE-
RITEX+ (22)
RITEX- (22)
STRBT- (23)
STRB+ (22,23)
PARGO+
CPREN+
MRES+
TSRES+
2N2219
PSOUT+
PSIN+ (23)
PGND+
TPBLO+
TPBHI+
VOLTS+ (23)
RREQ+
CPBLO+
CPBHI+
CTREQ-
CPWRP+
WRONL+
MASTS+
CRITE+
BPREN+
VOLTS-
CBLOT-
CBHIT-
PBLO+ (20)
PBHI+ (20)
VOLTS+ (23)
MRES+
OMRES- (23)
VOLTS-
PWST-
PWRUP+
PWRUP- (22)
VOLTS+ (23)
LMRES- (20,22,23)
NOTE
ALIGN IC (75451) PINS IN SOCKET (F12) AS SHOWN
IC
SYMBOLS
Vcc
VOLTS-
DRAWN DRF
CHECKED DRF
APPROVED
CONTROL SIGNALS
HSMIMP BCM-24-MW E

Bus Coupler Processor

BCP-Ø5 Technical Reference

BCP-15-MW BCP Standard Modification - Assembly

BCP-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	1/[illegible]	

BCP

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER 1/16/76 (AXM)

APP'D FOR REL. 1/16/76 (AXM)

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BCP TECHNICAL REFERENCE

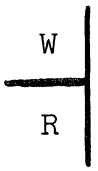
SIZE	CODE IDENT NO.	DRAWING NO.
A		BCP-05

SCALE	REV	SHEET
	A	1 OF 2

BCP - Bus Coupler Processor Card BBN

See BCM

Status - address none



Switches - none

Jumpers

Parity	Connect	
	From	To
WRITE SOURCE GENERATE (Classical)	F5-2 G10-1 G10-3	F5-15 G10-15 G10-14
WRITE SOURCE CHECK (Feedback)	G10-2 F5-2	G10-15 F5-15
NONE	G10-4	G10-13

BCP

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE FOR PROD		
		(OBS)	ECN 281		
		B	ECN 285	4/18/78	

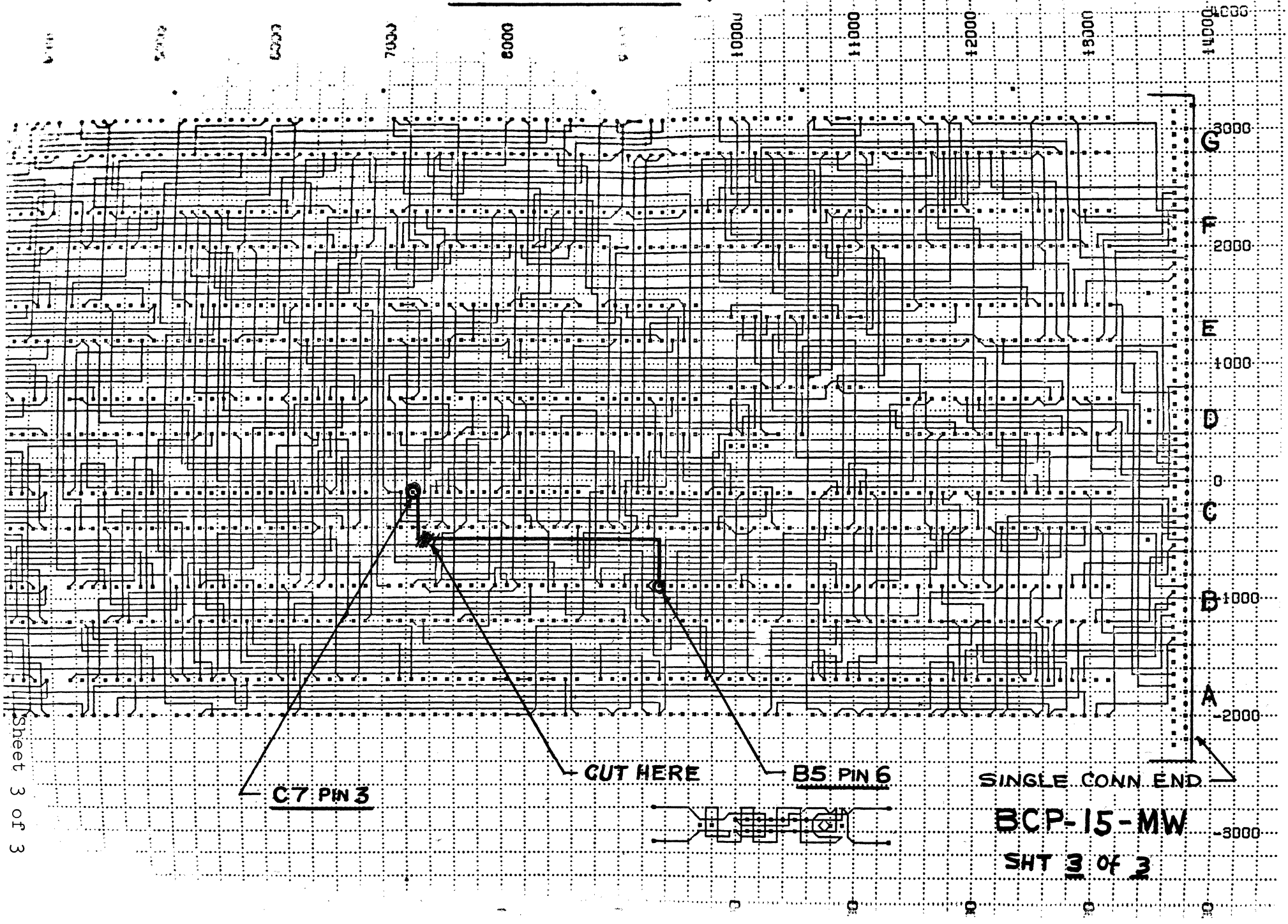
BCP

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

*	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN DRF 6/1/77	DRAWING TITLE: BCP Standard Mod - Assy.
	CHECKER	
	ENGINEER (MW) 7/7/77	
	APP'D FOR REL (AXM) 7/9/77	SIZE: A; CODE IDENT NO.: ; DRAWING NO.: BCP-15-MW
	APP'D (CUSTOMER)	SCALE: ; REV B; SHEET 1 OF 3

SOLDER SIDE (BCP MULTI-WIRE CARD)



1. This procedure applies to BCP Multiwire boards whose silkscreened revision level is shown as "A", "B", or "C".

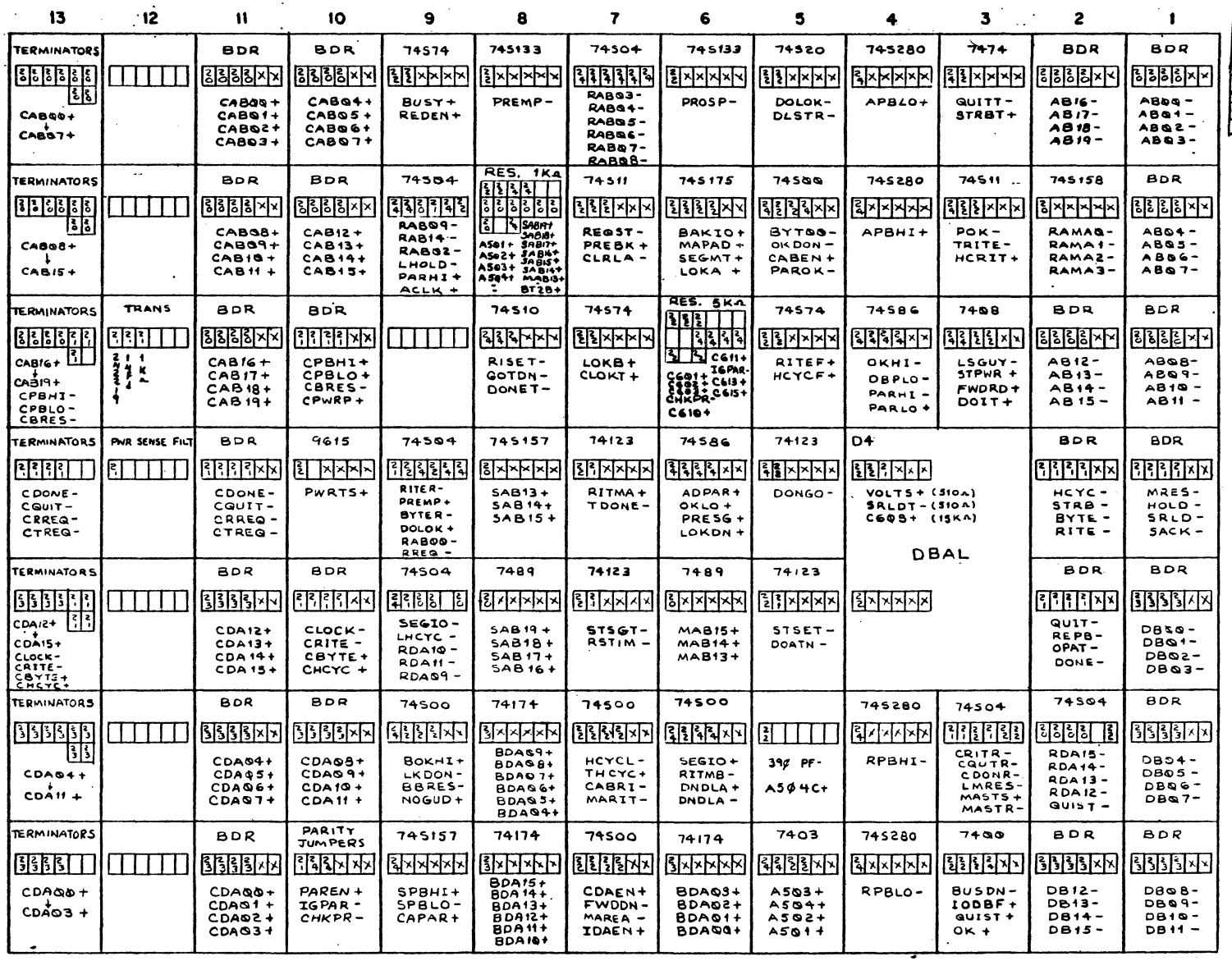
2. After the board has been assembled and soldered, make the following cut and adds:

   a. Cut wire from B5-6 to C7-3 on solder side of the board, as shown on page 3. Make the cut as shallow as possible, and remove a small portion of the wire.

   b. Add the following wires on the component side of the board, routing them under components to secure them. Terminate by soldering into the holes used by the IC leads where possible. If they do not fit into the holes, solder directly to the IC leads.

      1) B5:6 → D5:2
      2) D5:4 → C7:3
      3) D5:15 → C6:2
      4) D5:1 → D5:8
      5) D5:3 → C6:3

BCP-2Ø SCHEMATICS



REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	9.16.73
	B	DCR #2	7.23.73
	C	ECN #1	8.18.73
	D	ECN #5	11.12.73
	E	ECN #0029	2.26.74
	F	ECN #0076	7.10.74
	G	ECN #285	4.18.78

NOTES

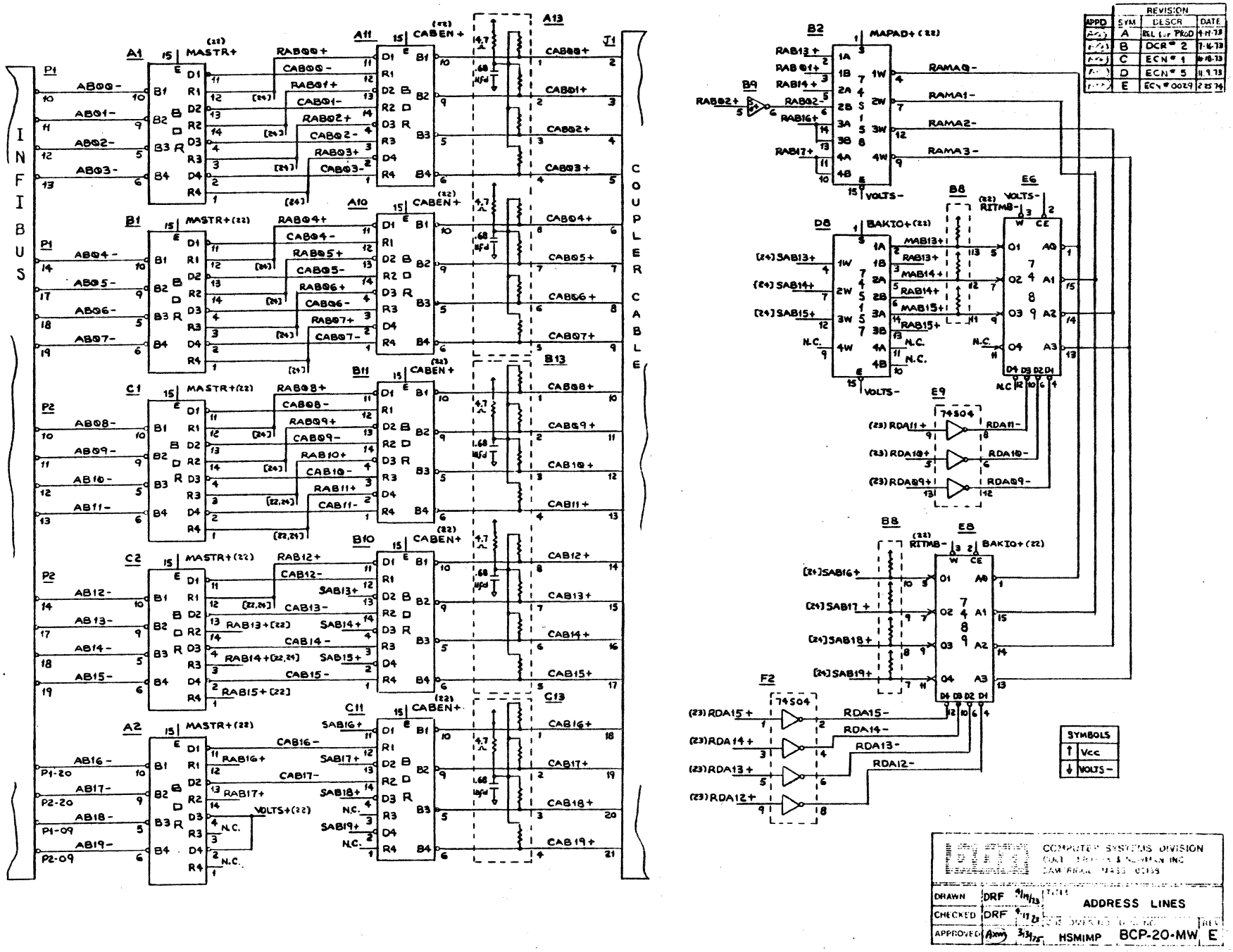
1) REV B LAYOUT FOR W W TWISTED PAIR TO CABLE

TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF		TITLE: INTEGRATED CIRCUIT LAYOUT
CHECKED	DRF		
APPROVED			CUSTOMER/NO. HSMIMP; DWG NO. BCP-00-MW; REV G

BCP

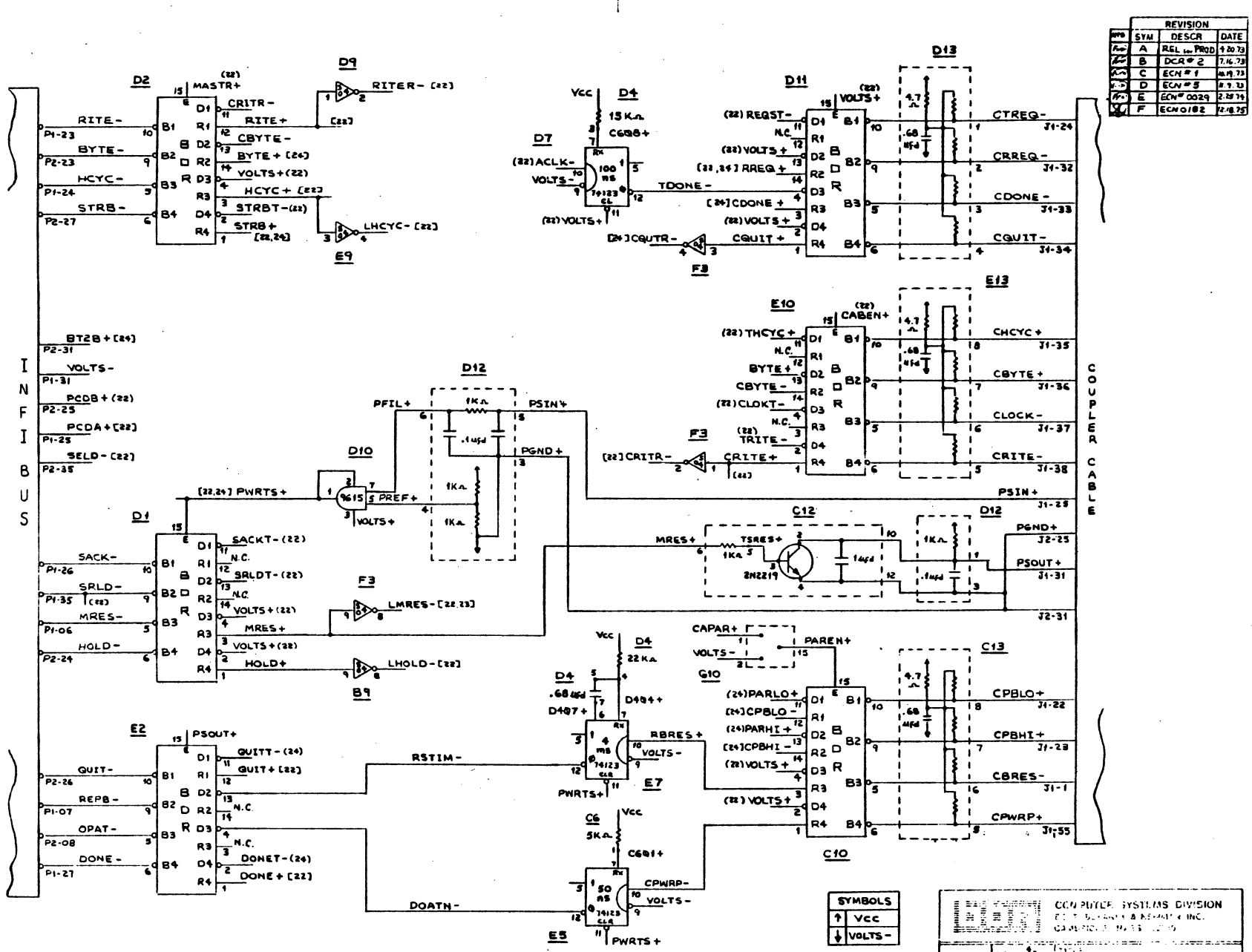


APPD	REVISION SYM	DESCR	DATE
	A	REL for PROD	4-17-73
	B	DCR # 2	7-16-73
	C	ECN # 1	10-10-73
	D	ECN # 5	11-9-73
	E	ECN # 0029	2-25-74

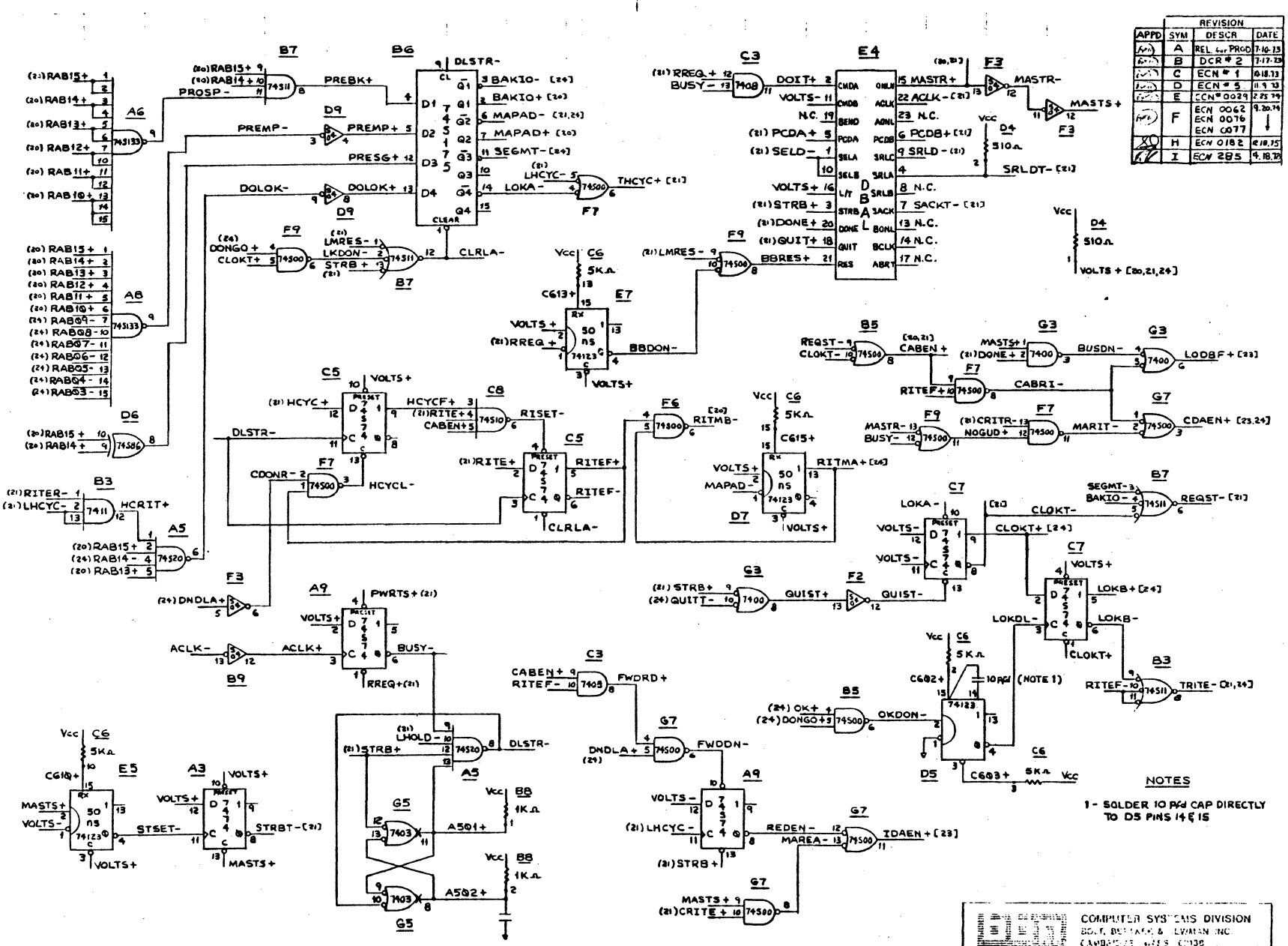
SYMBOLS
↑ Vcc
↓ VOLTS-

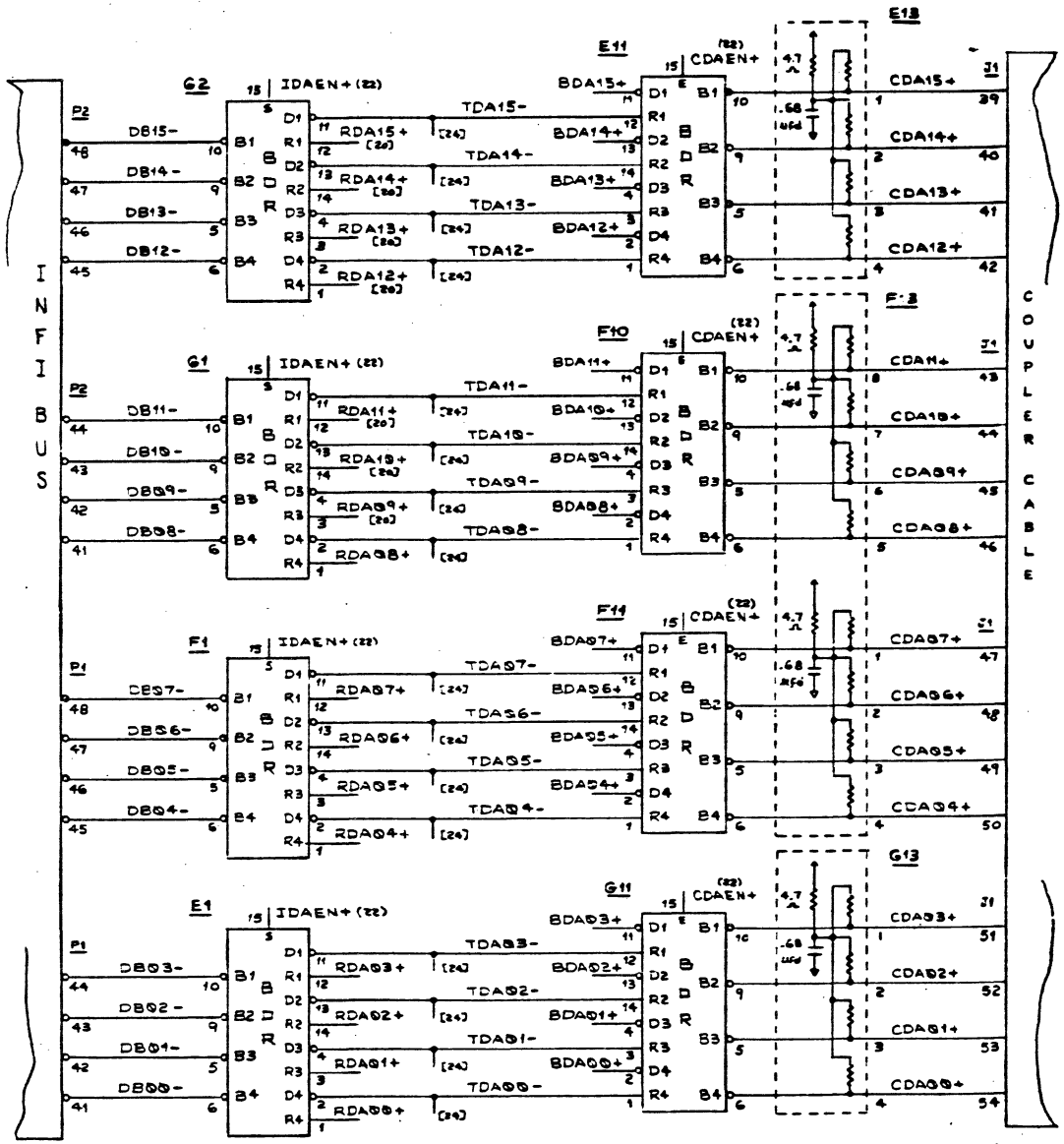
COMPUTER SYSTEMS DIVISION

DRAWN	DRF 9/11/73	TITLE	ADDRESS LINES
CHECKED	DRF 9/17/73		
APPROVED	[illegible] 3/31/75	HSMIMP	BCP-20-MW E


REVISION
SYM DESCR DATE
A REL to PROD 4-20-73
B DCR # 2 7-16-73
C ECN # 1 10-9-73
D ECN # 5 11-1-73
E ECN # 0029 2-28-74
F ECN 0182 12-18-75
INFIBUS
COUPLER CABLE
D1
D2
D4
D7
D9
D10
D11
D12
D13
E2
E5
E7
E9
E10
E13
F3
G10
C6
C10
C12
C13
RITE-
BYTE-
HCYC-
STRB-
MASTR+
CRITR-
RITE+
CBYTE-
BYTE+
VOLTS+
HCYC+
STRBT-
STRB+
RITER-
LHCYC-
BT2B+
VOLTS-
PCDB+
PCDA+
SELD-
PWRTS+
SACK-
SRLD-
MRES-
HOLD-
SACKT-
SRLDT-
LMRES-
LHOLD-
PSOUT+
QUIT-
REPB-
OPAT-
DONE-
QUITT-
QUIT+
DONET-
DONE+
RSTIM-
DOATN-
15 K.n.
100 MS
22 K.n.
5K.n.
50 MS
REQST-
RREQ+
TDONE-
CDONE+
CQUTR-
CQUIT+
CTREQ-
CRREQ-
CDONE-
CQUIT-
CABEN+
THCYC+
CLOCKT-
TRITE-
CRITE+
CHCYC+
CBYTE+
CLOCK-
CRITE-
PFIL+
PSIN+
PGND+
PREF+
MRES+
TSRES+
2N2219
PSOUT+
CAPAR+
PAREN+
PARLO+
CPBLO-
PARHI+
CPBHI-
RBRES+
CPWRP-
CBRES-
CPWRP+
SYMBOLS
VCC
VOLTS-
COMPUTER SYSTEMS DIVISION
CONTROL LINES
DRAWN DRF
CHECKED DRF
APPROVED
HSMIMP BCP-21-MW F
REV

BCP


REVISION
APPD | SYM | DESCR | DATE
A | REL for PROD | 7-10-73
B | DCR # 2 | 7-17-73
C | ECN # 1 | 8.18.73
D | ECN # 5 | 11.9.73
E | CCN # 0029 | 2.25.74
F | ECN 0062, ECN 0076, ECN 0077 | 9.20.74
H | ECN 0182 | 12.18.75
I | ECN 285 | 9.18.76
B7
B6
DLSTR-
PREBK+
PROSP-
PREMP-
PRESG+
DOLOK-
BAKIO-
BAKIO+
MAPAD-
MAPAD+
SEGMT-
LHCYC-
LOKA-
THCYC+
CLRLA-
DONGO+
CLOKT+
LMRES-
LKDON-
STRB+
C3
E4
F3
RREQ+
BUSY-
DOIT+
VOLTS-
N.C.
PCDA+
SELD-
VOLTS+
STRB+
DONE+
QUIT-
BBRES+
ACLK-
PCDB+
SRLD-
SRLDT-
SACKT-
MASTR+
MASTR-
MASTS+
D4
510Ω
F9
LMRES-
BBDON-
C6
5K Ω
C613+
E7
RREQ+
B5
REQST-
CABEN+
CLOKT-
G3
MASTS+
DONE+
BUSDN-
LODBF+
F7
RITEF+
CABRI-
MASTR-
BUSY-
CRITR-
NOGUD+
MARIT-
CDAEN+
C5
HCYC+
HCYCF+
RITE+
RITEF+
RISET-
CABEN+
DLSTR-
CDONR-
HCYCL-
CLRLA-
F6
RITMB-
C615+
RITMA+
MAPAD-
D7
B3
RITER-
LHCYC-
HCRIT+
A5
RAB15+
RAB14+
RAB13+
F3
DNDLA+
A9
PWRTS+
VOLTS+
ACLK-
ACLK+
BUSY-
RREQ+
B9
C7
LOKA-
CLOKT-
CLOKT+
SEGMT-
BAKIO-
REQST-
LOKB+
LOKB-
LOKDL-
RITEF-
TRITE-
C3
CABEN+
RITEF-
FWDRD+
G7
DNDLA+
FWDDN-
B5
OK+
DONGO+
OKDON-
C602+
10pfd (NOTE 1)
C603+
5K Ω
D5
C6
E5
A3
CG10+
MASTS+
VOLTS-
STSET-
STRBT-
B8
1K Ω
LHOLD-
STRB+
A5
G5
A501+
A502+
REDEN-
MAREA-
IDAEN+
CRITE+
NOTES
1- SOLDER 10 pfd CAP DIRECTLY TO D5 PINS 14 & 15
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE MASS 02138
DRAWN DRF 10-73
CHECKED DRF 10-73
APPROVED
CONTROL LOGIC
HSMIMP
BCP-22-MW
REV I



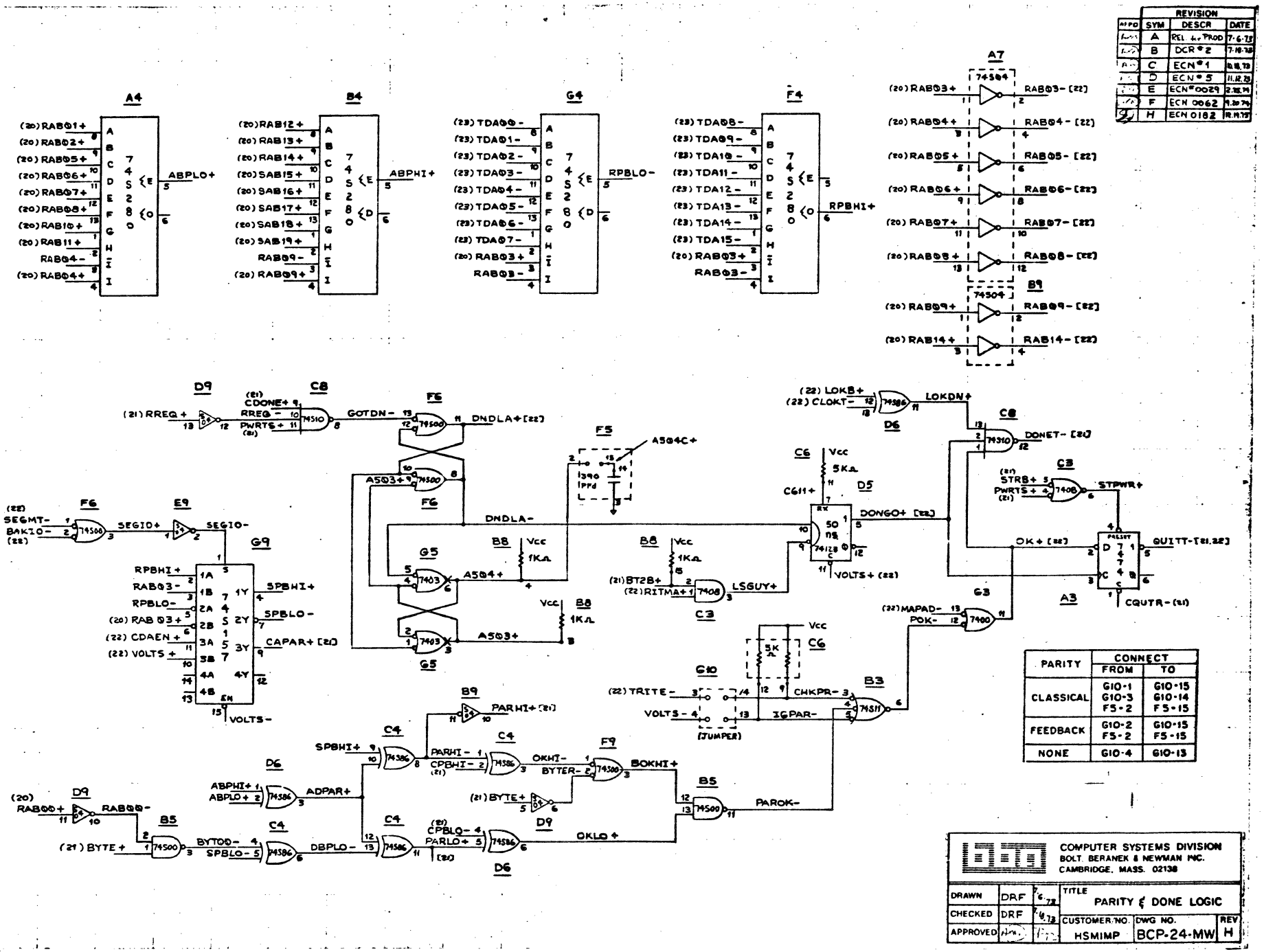
REVISION			
APPD	SYM	DESCR	DATE
	A	PEL for PROD	4.29.78
	B	DCR# 2	7.6.78
	C	ECN# 1	7.18.78
	D	ECN# 5	11.17.78
	E	ECN#0029	2.26.79

SYMBOLS	
↑	Vcc
↓	VOLTS-

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/23/78	TITLE: DATA LINES	
CHECKED	DRF	7/18/78	CUSTOMER NO. HSMIMP	DWG NO. BCP-23-MW REV E
APPROVED				

BCP


A4
B4
G4
F4
A7
B9
74S280
74504
(20) RAB01+
(20) RAB02+
(20) RAB05+
(20) RAB06+
(20) RAB07+
(20) RAB08+
(20) RAB10+
(20) RAB11+
RAB04-
(20) RAB04+
ABPLO+
(20) RAB12+
(20) RAB13+
(20) RAB14+
(20) SAB15+
(20) SAB16+
(20) SAB17+
(20) SAB18+
(20) SAB19+
RAB09-
(20) RAB09+
ABPHI+
(23) TDA00-
(23) TDA01-
(23) TDA02-
(23) TDA03-
(23) TDA04-
(23) TDA05-
(23) TDA06-
(23) TDA07-
(20) RAB03+
RAB03-
RPBLO-
(23) TDA08-
(23) TDA09-
(23) TDA10-
(23) TDA11-
(23) TDA12-
(23) TDA13-
(23) TDA14-
(23) TDA15-
(20) RAB03+
RAB03-
RPBHI+
RAB03- [22]
RAB04- [22]
RAB05- [22]
RAB06- [22]
RAB07- [22]
RAB08- [22]
RAB09- [22]
RAB14- [22]
REVISION
SYM
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REL to PROD
7-6-78
B
DCR #2
7-18-78
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10.18.78
D
ECN #5
11.12.78
E
ECN #0029
2.28.79
F
ECN 0062
4.30.79
H
ECN 0182
10.19.79
D9
C8
F6
(21) RREQ+
CDONE+
RREQ-
PWRTS+
(21)
74S10
74S00
GOTDN-
DNDLA+ [22]
A5C4C+
F5
390 PFd
A5C3+
A5C4+
A5C3+
DNDLA-
(22) SEGMT-
BAK10-
(22)
74S00
SEGI0+
E9
SEGI0-
G9
RPBHI+
RAB03-
RPBLO-
(20) RAB 03+
(22) CDAEN+
(22) VOLTS+
SPBHI+
SPBLO-
CAPAR+ [20]
VOLTS-
74S153
G5
74S03
B8
Vcc
1K Ω
C6
5K Ω
C611+
D5
74S128
50 ns
DONGO+ [22]
VOLTS+ (22)
(22) BT2B+
(22) RITMA+1
74S08
LSGUY+
C3
(22) LOKB+
(22) CLOKT-
74S86
LOKDN+
D6
C8
74S10
DONET- [21]
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(21)
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PWRTS+ 4
(21)
74S08
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G3
(22) MAPAD- 13
POK- 12
74S00
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C4
SPBHI+
74S86
PARHI-
CPBHI-
(21)
OKHI-
BYTER-
F9
74S08
BOKHI+
B5
74S09
PAROK-
D6
ABPHI+ 1
ABPLO+ 2
74S86
ADPAR+
(21) BYTE+
D9
OKLO+
(20)
RAB00+
RAB00-
B5
(21) BYTE+
74S00
BYT00-
SPBLO-
74S86
DBPLO-
CPBLO-
PARLO+
[20]
D6
C10
(22) TRITE-
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(JUMPER)
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IGPAR-
B3
74S11
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TO
CLASSICAL
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G10-3
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F5-15
FEEDBACK
G10-2
F5-2
G10-15
F5-15
NONE
G10-4
G10-13
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN
DRF
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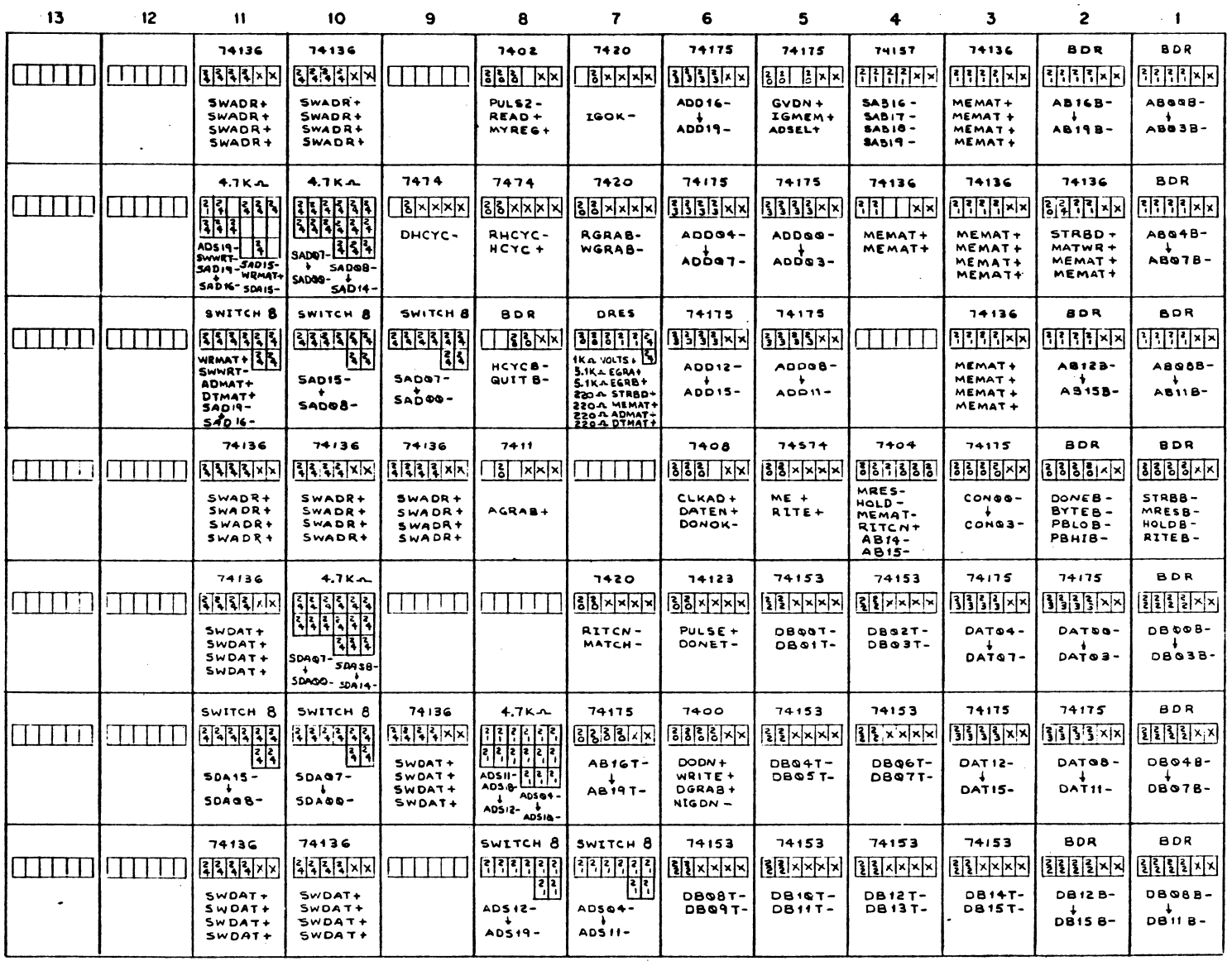
TITLE
PARITY & DONE LOGIC
CUSTOMER NO.
HSMIMP
DWG NO.
BCP-24-MW
REV
H

Bus Coupler Tester

BCT-2Ø Schematics



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APPD	SYM	DESCR	DATE
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	B	ECN 0160	8-11-74
	C	ECN 0163	9-16-74
	D	ECN 0165	9-24-74

NOTES

1

TOP VIEW

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CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/8/74	TITLE: INTEGRATED CIRCUIT LAYOUT
CHECKED		9/4/74	CUSTOMER/NO.: HSMIMP
APPROVED		9/4/74	DWG NO.: BCT-00-WW; REV: D

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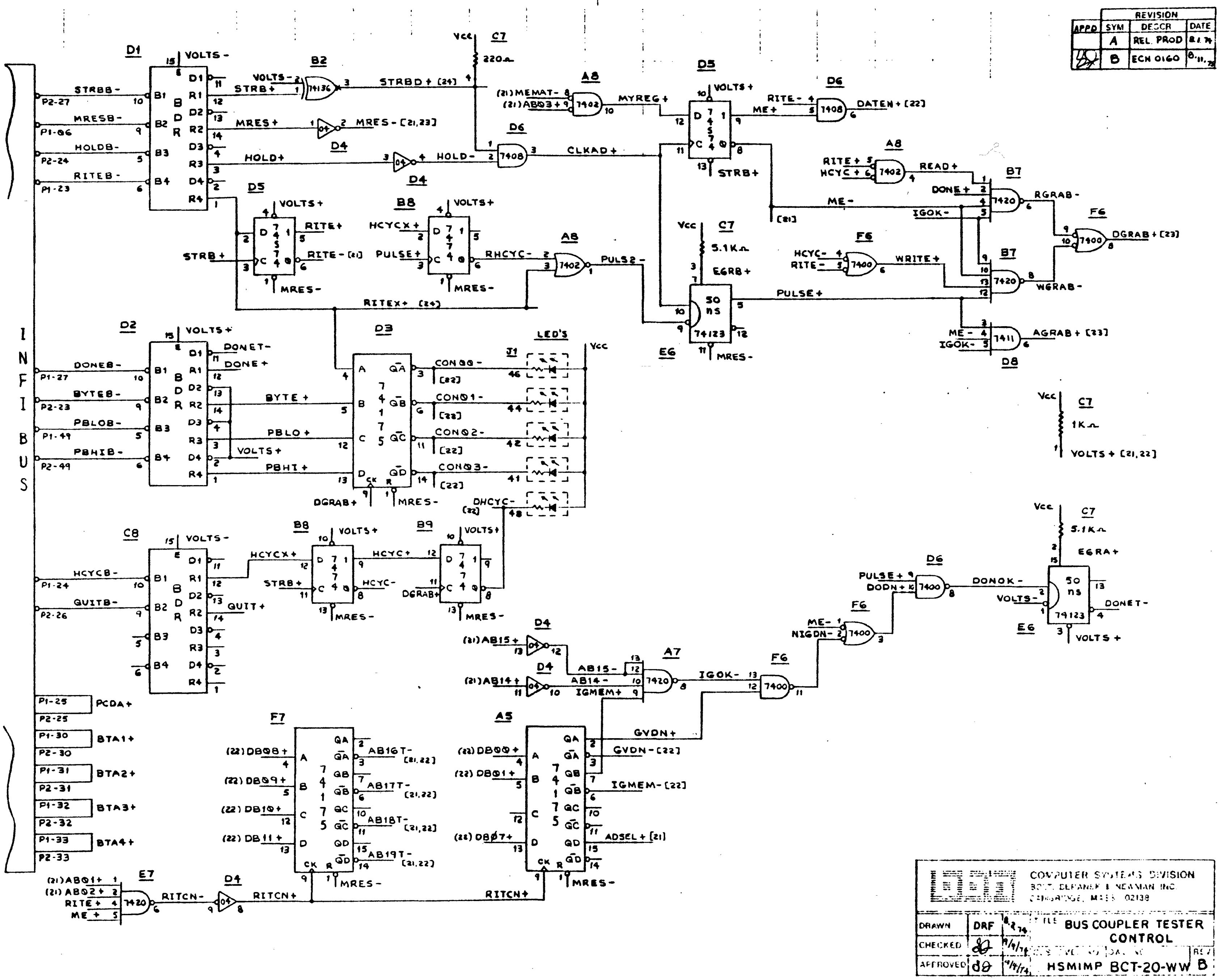

REVISION
APPD SYM DESCR DATE
A REL. PROD
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INFIBUS
D1
BDR
VOLTS -
STRBB-
MRESB-
HOLDB-
RITEB-
P2-27
P1-06
P2-24
P1-23
B2
74136
VOLTS-
STRB+
STRBD + [24]
MRES+
MRES- [21,23]
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HOLD+
HOLD-
C7
220Ω
Vcc
D6
7408
CLKAD+
A8
7402
(21) MEMAT-
(21) AB03 +
MYREG +
D5
VOLTS +
ME+
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DATEN + [22]
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READ+
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ME-
IGOK-
RGRAB-
F6
7400
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RITE-
WRITE+
WGRAB-
PULSE+
AGRAB+ [23]
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7411
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EGRB+
50 ns
74123
MRES-
E6
RITE-[21]
B8
HCYCX+
PULSE+
RHCYC-
PULS2-
STRB+
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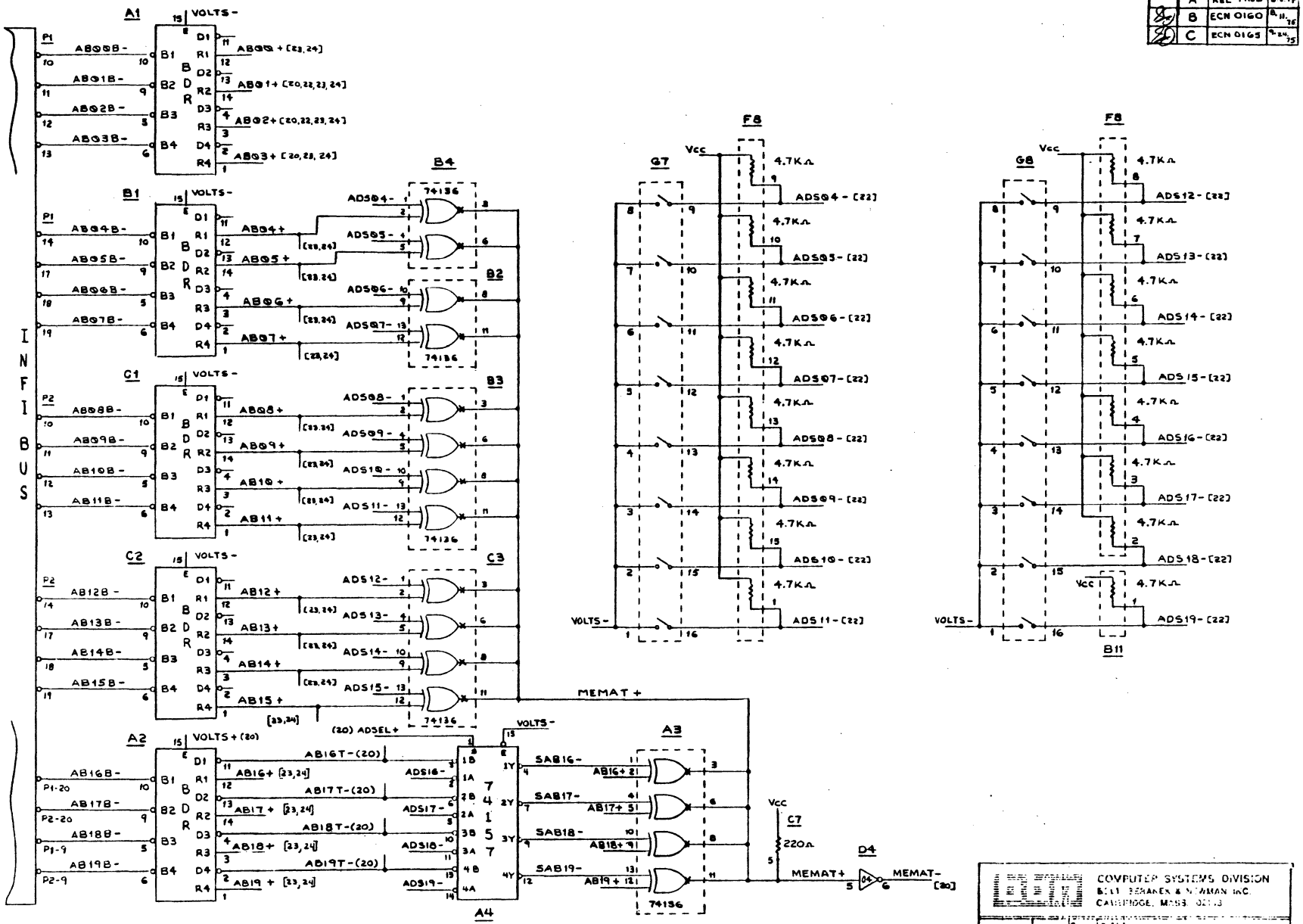
D2
DONEB-
BYTEB-
PBLOB-
PBHIB-
P1-27
P2-23
P1-49
P2-49
DONET-
DONE+
BYTE+
PBLO+
PBHI+
D3
74175
DGRAB+
CON00-
CON01-
CON02-
CON03-
DHCYC-
LED'S
J1
1KΩ
VOLTS + [21,22]
C8
HCYCB-
QUITB-
P1-24
P2-26
QUIT+
B9
HCYC+
HCYC-
DGRAB+
EGRA+
DONOK-
DODN+
NIGDN-
DONET-
A7
(21) AB15+
(21) AB14+
AB15-
AB14-
IGMEM+
IGOK-
PCDA+
BTA1+
BTA2+
BTA3+
BTA4+
F7
(22) DB08+
(22) DB09+
(22) DB10+
(22) DB11+
AB16T- [21,22]
AB17T- [21,22]
AB18T- [21,22]
AB19T- [21,22]
A5
(22) DB00+
(22) DB01+
(22) DB07+
GVDN+
GVDN- [22]
IGMEM- [22]
ADSEL + [21]
E7
(21) AB01+
(21) AB02+
RITE+
ME+
RITCN-
RITCN+
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS. 02138
DRAWN DRF
CHECKED
APPROVED
TITLE BUS COUPLER TESTER CONTROL
HSMIMP BCT-20-WW B



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CAMBRIDGE, MASS. 02138

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APPROVED	[illegible]	9/4/74	HISMIMP BCT-21-WW C

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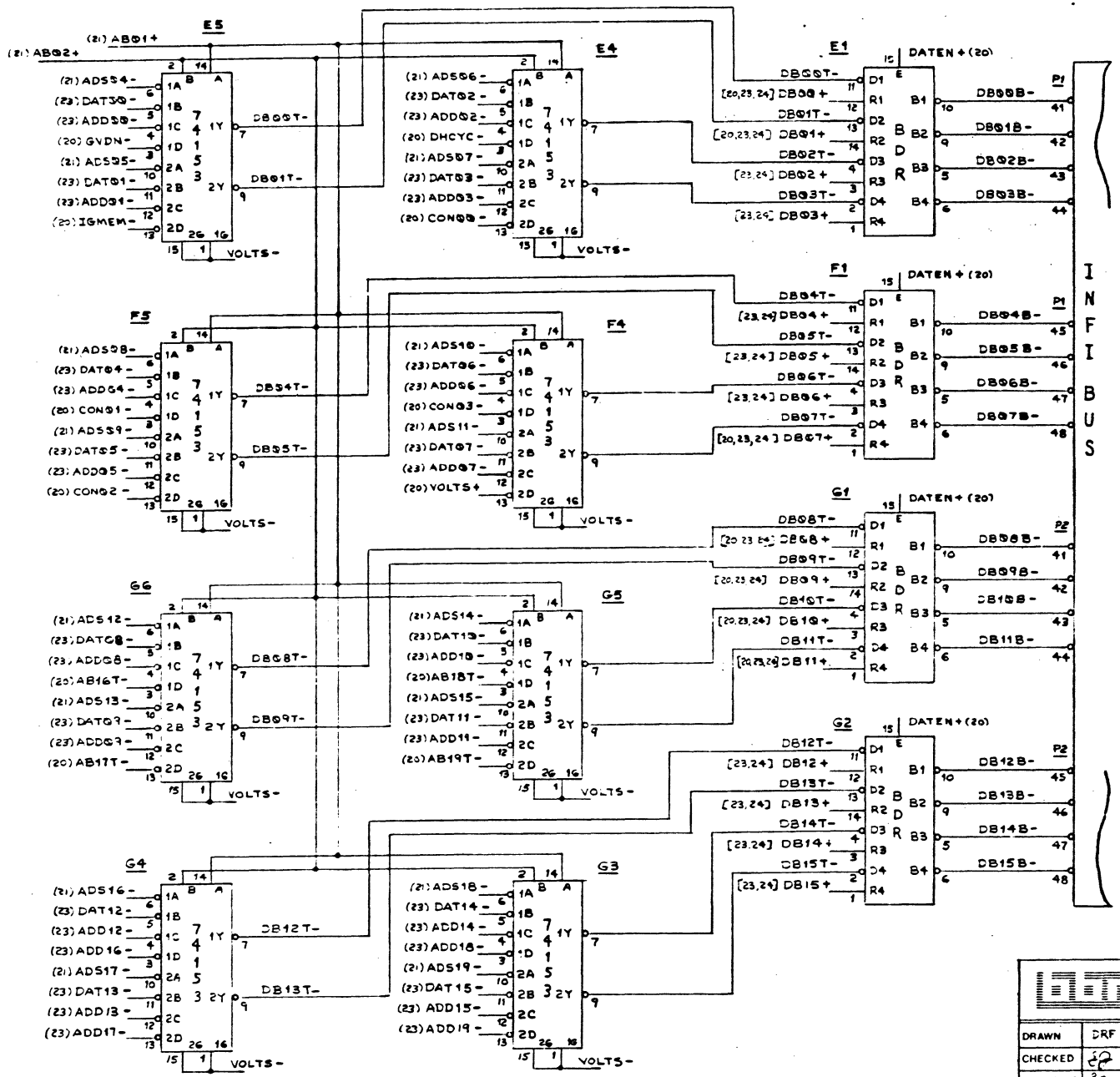

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	B	ECN 0160	8.11.74

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DRAWN	DRF	8.5.74	TITLE BUS COUPLER TESTER DATA MULTIPLEXERS
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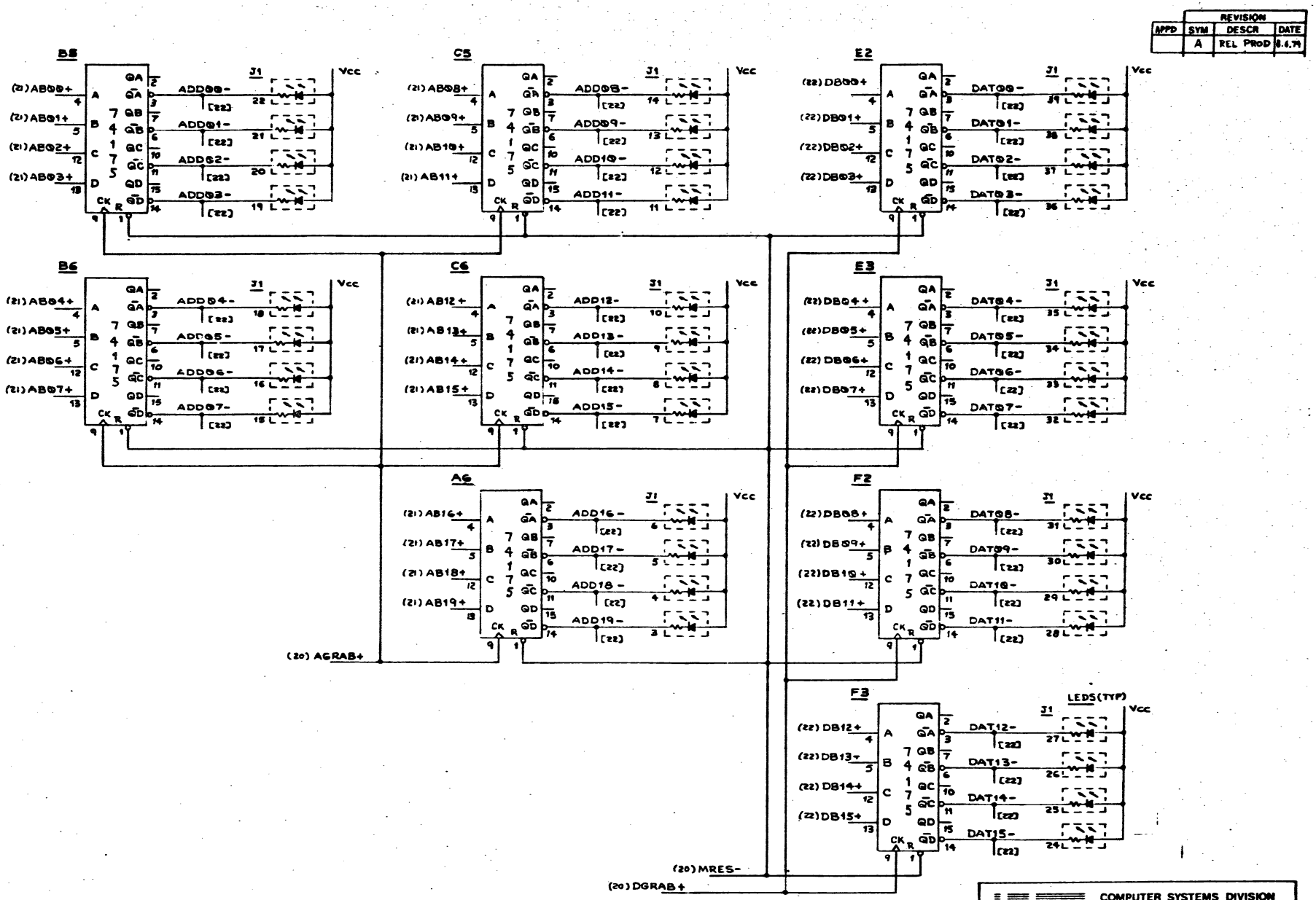
APPROVED		9/6/74	



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CAMBRIDGE, MASS. 02138

DRAWN	DRF	8.6.74	TITLE BUS COUPLER TESTER LATCHES & INDICATORS
CHECKED		9/4/74	CUSTOMER NO. HSMIMP / DWG NO. BCT-23-WW / REV A
APPROVED		9/4/74	

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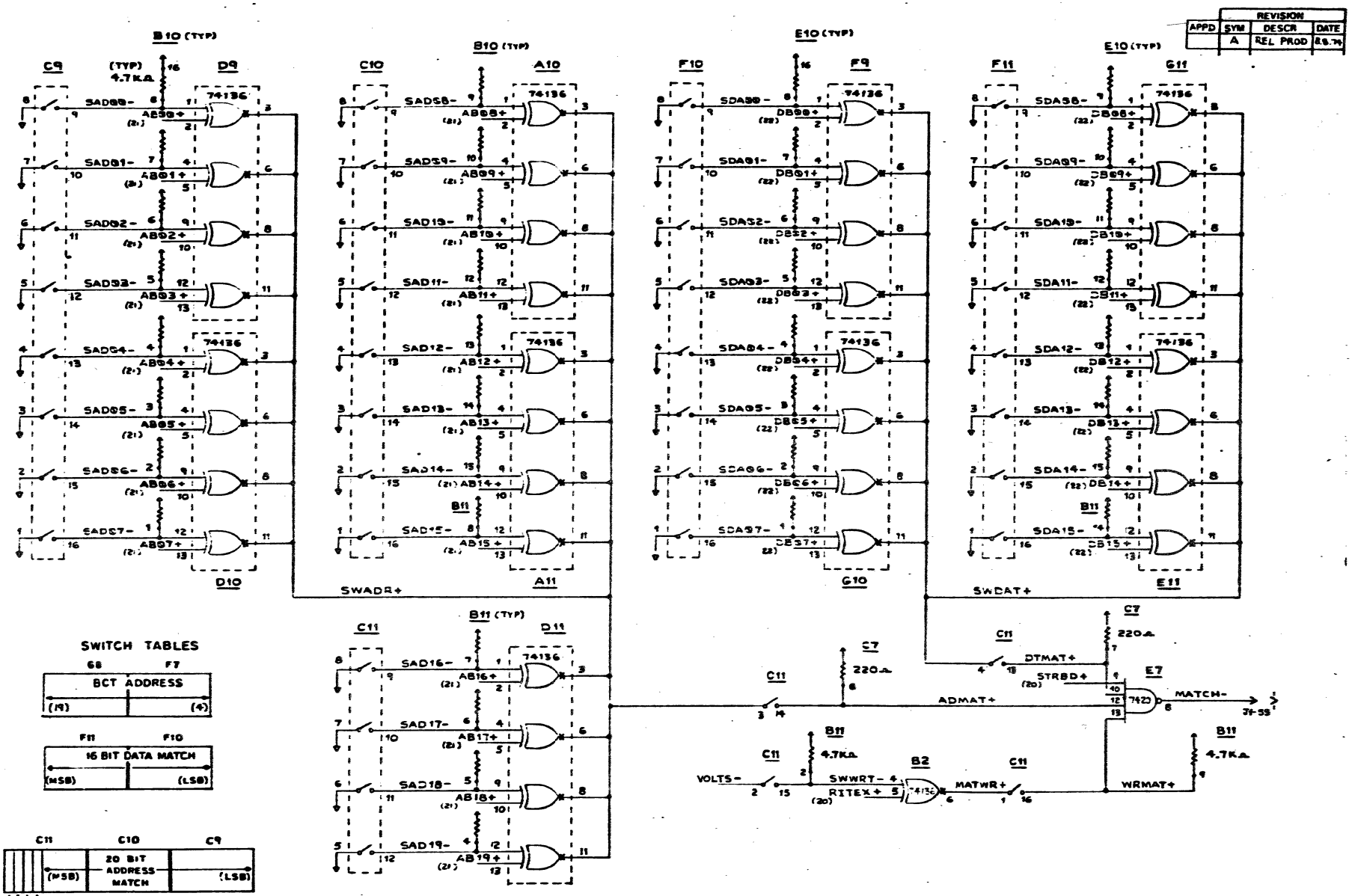
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(TYP) 4.7KΩ
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D10
74136
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SAD01-
SAD02-
SAD03-
SAD04-
SAD05-
SAD06-
SAD07-
AB00+
AB01+
AB02+
AB03+
AB04+
AB05+
AB06+
AB07+
B10 (TYP)
C10
A10
A11
SAD08-
SAD09-
SAD10-
SAD11-
SAD12-
SAD13-
SAD14-
SAD15-
AB08+
AB09+
AB10+
AB11+
AB12+
AB13+
AB14+
AB15+
B11
E10 (TYP)
F10
F9
G10
SDA00-
SDA01-
SDA02-
SDA03-
SDA04-
SDA05-
SDA06-
SDA07-
DB00+
DB01+
DB02+
DB03+
DB04+
DB05+
DB06+
DB07+
E10 (TYP)
F11
G11
E11
SDA08-
SDA09-
SDA10-
SDA11-
SDA12-
SDA13-
SDA14-
SDA15-
DB08+
DB09+
DB10+
DB11+
DB12+
DB13+
DB14+
DB15+
SWADR+
SWDAT+
B11 (TYP)
C11
D11
SAD16-
SAD17-
SAD18-
SAD19-
AB16+
AB17+
AB18+
AB19+
SWITCH TABLES
F8 F7
BCT ADDRESS
(9) (4)
F11 F10
16 BIT DATA MATCH
(MSB) (LSB)
C11 C10 C9
20 BIT ADDRESS MATCH
(MSB) (LSB)
CLOSED = MATCH CONTENTS OF DATA SWITCHES; OPEN = MATCH ANY DATA.
CLOSED = MATCH CONTENTS OF ADDRESS SWITCHES; OPEN = MATCH ANY ADDRESS.
(if enabled by left most switch closed), CLOSED = MATCH WRITE; OPEN = MATCH READ.
CLOSED = MATCH IF NEXT RIGHT SWITCH SATISFIED; OPEN = IGNORES NEXT RIGHT SWITCH SETTING.
C7
220Ω
DTMAT+
STRBD+
E7
7423
MATCH-
ADMAT+
B11
4.7KΩ
VOLTS-
SWWRT-
RITEX+
B2
MATWR+
WRMAT+
SYMBOLS
↑ Vcc
↓ VOLTS-
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BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138
DRAWN DRF 8/8/74
CHECKED 9/11/74
APPROVED 9/13/74
TITLE BUS COUPLER TESTER DATA & ADDRESS MATCH
CUSTOMER NO HSMIMP
DWG NO. BCT-24-WW
REV A

Bus Control Unit

BCU-Ø2 Logic Description

BCU-Ø5 Technical Reference

BCU-15 Standard Modification

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	/	

BCU

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER 75 12 19

APP'D FOR REL 75 12 19

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BCU - LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		BCU - Ø2

SCALE	REV A	SHEET OF

SUE 1810 BUS CONTROL UNIT

MAINTENANCE BULLETIN M1810

BCU

CONTENTS

BCU

CONTENTS (continued)

LIST OF ILLUSTRATIONS

SUE 1810 BUS CONTROL UNIT

MAINTENANCE BULLETIN

INTRODUCTION

This bulletin describes the logic functions of the SUE 1810 Bus Control Unit (BCU). Figure 1 shows the BCU functional block diagram. As indicated in figure 1, the BCU interfaces both the INFIBUS and the Central Processing Unit (CPU). The BCU and CPU are interconnected by an interconnecting module (ICM) plugged into edge connectors located on the rear edge of the respective circuit cards.

Logic diagrams in this bulletin are keyed to figure 1. The number in the upper left-hand corner of each block in figure 1 indicates the logic diagram sheet number on which the corresponding logic is represented.

SERVICE REQUEST, MASKS, AND LATCHES (LD Sheet 2)

BCU

SRL1-N through SRL4-N, SRLD-N and SRLC-N are the service request lines for INFIBUS access. Signal DNUM-P is the OR function of the power fail, power restart and line frequency internal interrupts (LD sheet 5). DN3R-N is the output of the external attention flip-flop (LD sheet 5). All the request lines mentioned above except SRLD and SRLC, have a corresponding interrupt mask as follows (see figure 2):

LB15-P (Bit 15) masks interrupts on line 4 from

a. Service request SRL4-N
b. Line frequency LFRQ-N (DNUM-N)
c. Power status PWST-N (DNUM-N)

LB14-P (Bit 14) masks interrupts on line 3 from service request SRL3-N

LB13-P (Bit 13) masks interrupts on line 2 from service request SRL2-N

LB12-P (Bit 12) masks interrupts on line 1 from

a. Service request SRL1-N
b. External attention EXAT-N (DN3R-N)

CPU INTERRUPT, NEXT-N

Assertion of any service request (1 thru 4), or internal interrupt, cause the BCU to issue CPU interrupt signal (NEXT-N). This signal is negated when the service request is negated by the selected module, or when the CPU asserts its interrupt-masks (see figure 2). Assertion of Master Interrupt Inhibit MINH-N also negates NEXT-N.

REQUEST LATCHES

Gate ENIN is enabled (output low) by

a. Assertion of CPU Permit Interrupt signal, SCM3-N (LD sheet 3) which sets Permit Interrupt flip-flop (PIN) and negates INTR-N.
b. Negation of Acknowledge Receiver signal, RSAK-P.

When gate ENIN is enabled, any new service request is gated and latched in one of the two 6-bit latches. These latches inhibit any change in their content until signal SACK is asserted, then removed, and a new request is asserted and allowed.

LOGIC DEFINITIONS

NSAK-N

Acknowledge received either from a module or generated by the BCU for internal interrupts.

RLDS-P

SRLD-N latched.

RPLS-P

Latch for the Line Frequency, Power Restart, and Power Fail internal interrupts.

RL3S-P

SRL3-N latched.

RL2S-P

SRL2-N latched.

RL1S-P

SRL1-N latched.

REXS-P

EXAT-N latched.

RLCS-P

SRLC-N latched.

SELA-P, SELB-P

Prevent any change in the contents of the two 6-bit latches of the interrupts and enables select lines on the INFIBUS when Acknowledge is negated.

SERVICE REQUEST SELECTION AND CPU INTERRUPT GENERATION (LD Sheet 3)

SERVICE REQUEST PRIORITY

Service request priority is established by the SL gates input of which comes from the 6-bit latches (LD sheet 2). The order of priority is:

a. SRLD
b. Power fail, power restart, line frequency
c. SRL4
d. SRL3
e. SRL2
f. SRL1
g. External Attention (EXAT)
h. SRLC

SELECT LINES

Gate SEL(N) corresponding with the asserted service request line, is enabled when Select Acknowledge (NSAK-N) is negated and if no other service request with higher priority is asserted.

The output of all select lines, and OR gate NINT-N, of External Attention, power, and line frequency, are ORed at gate PCDI to generate precedence chain signal PCDB-P (see LD sheet 6 and figure 3), and triggers a 1 microsecond one-shot (SAC) for pseudo-SACK generation (LD sheet 5).

INTERRUPT LEVEL FLIP-FLOPS

Inputs to interrupt level flip-flops are:

a. PLEX - for either power status, line frequency, or external attention

b. I2P4 - for either power status, line frequency, SRL2 or SRL4

c. I3P4 - for either power status, line frequency, SRL3 or SRL4

d. INTA - for either one of the above, or SRL1.

These flip-flops are cleared by gate SCRS, when either Master Reset or CPU Permit Interrupt (SCM-3) is asserted. The flip-flops are set when any of the above conditions (a, b, c, d) are true and the selected device responds with Select Acknowledge (RSAK-P).

INTERRUPT LEVEL CODE (IL0R-N, IL1R-N)

The Bus Controller sends a code to the CPU, on lines IL0R-N and IL1R-N, that corresponds to the line on which the interrupt occurred (see figure 3).

LOGIC DEFINITIONS

S11P-P	Triggers a 1 microsecond pseudo SACK generator. If SACK-N is not received from the selected device within this time, the BCU asserts its own SACK-N.
SEL1-SEL4, SELC, SELD	Select lines on the INFIBUS in response to the corresponding service request.

NNTS-P	Internal interrupt due to power fail or restart, line frequency, or external attention. The BCU generates its own Select Acknowledge to latch this flip-flop.
IL0R, IL1R	Interrupt level bit codes to the CPU.
INTR-N	Latched on any interrupt except SRLD and SRLC when Select Acknowledge is asserted.
SCLK-P	Clock pulse generated by any interrupt except SRLD and SRLC when Select Acknowledge is asserted. SCLK-P is used to 1) clock internal interrupts, DN0S through DN3S, into the device number latches, and 2) to reset DN0S through DN3S.
CYST-N	Any interrupt except SRLD and SRLC.
SCRS-N	Clear function of interrupt level and device number flip-flops, when the CPU asserts Permit Interrupt SCM3-N or Master Reset is sensed.
PINS-P	Stays set when first SCM3-N is received from the CPU. Master Reset negates this signal.
NINT-N	Any internal interrupt. Used to generate SACK-N.
PCDI-P	Any selected device SEL1-SEL4, SELD, SELC or internal interrupt. Used to generate the precedence chain signal PCDI-P.
RNIR-P	Any acknowledge service request SRL1 through SRL4, internal interrupt, or Master Reset. Used to generate DN0L-P to the CPU when strobe is received. This signal is negated when the CPU asserts Permit Interrupt signal SCM3-N.

BCU

BUS ACCESS LOGIC (LD Sheet 4)

At the end of a previous bus access, Select flip-flop (BSL) and On-Line flip-flop (BOL) are reset, consecutively, when the BCU line receivers (LD Sheet 5) sense strobe STRB-N and the trailing edge of signal DONE-N from the selected device.

Absence of any service request 1-4 or internal interrupts negates CYST-N (LD sheet 3). Asserting CPU Permit Interrupt (SCM3-N) clears interrupt level flip-flop and sets Permit Interrupt flip-flop (PIN). Thus signal INAR-N (LD sheet 3) is negated and gate BSRQ sets Ready flip-flop (BRQ). When the BCU receives any service request or senses an internal interrupt, CYST-N is asserted and the output of BSRQ goes high. When the BCU asserts any select

line in response to a service request, or senses an internal interrupt, the output of gate PCDI (LD sheet 3) goes high and generates signal PCDB-P (LD sheet 6).

The leading edge of the precedence chain signal (PCDB-P) sets Select flip-flop (BSL), and the trailing edge resets the Ready flip-flop through gate BCRQ. Once the Select flip-flop is set, and if DONE-N, STRB-N and QUIT-N (LD sheet 5) are negated, gate BSOL is enabled to set the On-Line flip-flop and to allow gate ONLN to generate STRB-N, during internal interrupts only. The Select flip-flop remains set until the selected module device asserts STRB-N. At the same time, the Post Acknowledge gate (PSAK) is low and generates the Select Acknowledge signal (SACK-N) through gates SACC and SACA (LD sheet 5) for internal interrupts only. Off-Line flip-flop (BOF) is set by gate BSOF at the leading edge of signal DONE-N received from the selected module device. BSOF is reset when the On-Line flip-flop is reset. The On-Line flip-flop is reset at the trailing edge of DONE-N by gate BCOL.

LOGIC DEFINITIONS

PSAK-N	Post Acknowledge generated by the BCU during any interrupt except SRLD and SRLC. Used to generate SACK-N during internal interrupts.
RSTN-N	Strobe signal.
DNLN-P	Enable the BCU during internal interrupts to generate STRB-N and assert the device number on the INFIBUS.

BUS DRIVERS/RECEIVERS (LD Sheet 5)

DEVICE NUMBER ON-LINE

When the CPU receives interrupt signal NEXT-N (LD sheet 2) from the BCU, the CPU responds after executing the last instruction, with allow-interrupt SCM3-N. This signal negates Device Number On-Line (DNOL-P) signal to the CPU through gate RNIR (see figure 2).

When the selected module asserts SACK-N and negates its service request, the BCU places the interrupt level codes on lines IL0R-N and IL1R-N (LD sheet 3) and enables signal RNIR-P. However, signal DNOL-P to the CPU is not asserted until the selected module device asserts its STRB-N to negate signal PSAK-N.

During internal interrupts the BCU enables, through gate EIIN (LD sheet 5), the device number to be asserted on the INFIBUS. Fifty nanoseconds later the BCU asserts STRB-N which negates PSAK-N. With PSAK-N negated and RNIR-P enabled when PSAK-N is enabled, the BCU asserts DNOL-P to the CPU.

SELECT ACKNOWLEDGE, SACK-N (LD Sheet 5)

Normally, signal SACK-N is received from a requesting device when the BCU asserts the Select and Precedence Chain signals (see figure 2). However, the BCU asserts SACK-N for internal interrupts listed as follows:

a. Line frequency, DN0 flip-flop
b. Power fail, DN1 flip-flop
c. Power restart, DN2 flip-flop
d. External Attention, DN3 flip-flop

Signal NINT-N (LD sheet 3), the OR output of the above flip-flops, is asserted, and signal PSAK-N remains asserted (due to the absence of strobe) to generate SACK-N through gates SACC and SACA.

If SACK-N is not received from any selected interrupt within 1 microsecond to negate PCDE-P, then SACK-N is generated through one-shot SAC and gates SACS and SASA.

STROBE, STRB-N

Strobe is normally generated by the selected device (see figure 2). When the output of gate NNTS (LD sheet 3) is high, however, the BCU asserts strobe in response to its internal interrupts through the Enable Internal Interrupt gate, EIIN, if signal ONLN-P (LD sheet 4) is asserted.

QUIT-N AND DONE-N (LD Sheet 5)

Receipt of DONE-N by the selected device and the BCU indicates successful completion of the bus service (see figure 2). The selected device responds by negating its strobe, STRB-N. However, if the Done signal is not received, the device keeps the strobe asserted. If the strobe remains asserted for 2 microseconds after one-shot TQN is triggered by Acknowledge signal RSAK-P, flip-flop QUT remains set. This enables gate QUTA and at the end of the 2 microseconds QUIT-N is asserted. Either DONE-N or QUIT-N causes the selected device to remove its strobe signal, resetting flip-flop QUT. Subsequently, the BCU negates QUIT-N.

INTERRUPT DEVICE NUMBER (DB00-N-DB02-N)

The BCU is not addressable, so the device numbers assigned for its Internal Interrupts are not the same as for addressable modules but are coded as follows:

Level	Device Number	Source	Description
1	0001	EXAT-N	External Attention
4	0001	LFRQ-N	Line Frequency
4	0002	PWST-N	Power Fail
4	0004	PWST-N	Power Restart

Note that the three interrupts to level 4 use separate bits. Since they are asynchronous and independent, a line frequency interrupt can be present with a power fail interrupt (see figure 3).

INTERNAL INTERRUPTS (LD Sheet 5)

EXTERNAL ATTENTION (EXAT-N)

Assertion of this line sets the External Attention flip-flop, DN3, and causes the BCU to initiate a level-one interrupt and generate a device number of 0001.

POWER FAIL INTERRUPT INHIBIT (PFIN-N)

Asserting PFIN-N disables gate DN1A and causes the BCU to inhibit interrupts attributed to power fail detection. When PFIN-N is negated, and when the power supply asserts power status PWST-N (indicating power failure), the output of gate PFID (LD sheet 6 and figure 3) goes high for 30-60 nanoseconds. This sets Power Fail flip-flop (DN1) which generates an interrupt service request on level four and a device number of 0002.

POWER RESTART INTERRUPT INHIBIT (PRIN-N/PRAL-N)

The BCU responds to Power Restart Interrupt Inhibit (PRIN-N) and Power Restart Auto Load-Interrupt Inhibit (PRAL-N) as shown in the following truth table (- means any condition).

	PRIN-N	PRAL-N
Interrupt, No Auto Load	High	High
No Interrupt, No Auto Load	Low	High
No Interrupt, Auto Load	-	Low

Asserting either PRIN-N or PRAL-N disables gate DN2A and causes the BCU to inhibit interrupts attributed to Power Restore detection. When both PRIN-N and PRAL-N are negated, and at the conclusion of a 50-millisecond Master Reset which follows negation of power status (PWST-N), 100-nanosecond PRID-P (sheet 6) sets Power Restart flip-flop (DN2). Setting DN2 causes the BCU to generate an interrupt service request on level four and a device number of 0004.

LINE FREQUENCY INTERRUPT/INHIBIT (LFRQ-N/LFIN-N)

Asserting Line Frequency Interrupt Inhibit (LFIN-N) disables gate DN0A and causes the BCU to inhibit the line frequency interrupts. When LFIN-N is negated, signal LFID-P pulses gate DN0A low once each line frequency cycle (normally 60 Hz). As a result, the line frequency flip-flop (DN0) is set which causes the BCU to generate an interrupt service request on level four and a device number of 0001.

MEMORY CYCLE INHIBIT (HOLD-N)

The Bus Controller asserting HOLD-N prevents a memory cycle from being initiated during the time the device number of a selected interrupting device is being read by the CPU. Signal ONLN-P is high during this time and is negated by DONE-N.

DEFINITIONS OF OTHER LOGIC TERMS ON LD SHEET 5

DNUM-N	Any sensed internal interrupt due to line frequency, power failure or power restart. Used to generate a level-four interrupt to the CPU. DNUM-N is negated when the BCU generates SACK-N.
DN3R-N	External Attention sensed. Generates a level-one interrupt to the CPU. The bus controller generates SACK-N to clear this signal.

LOGIC ON LOGIC DIAGRAM SHEET 6

POWER STATUS, PWST-N AND MASTER RESET, MRES-N (LD Sheet 6)

Marginal power, or a power-fail condition causes the power supply to output a pulse train of approximately 10 kHz. This pulse train triggers 2.5-millisecond one-shot COP. The trailing edge of COPR-N generates a power-fail interrupt signal through gate PFID and triggers 250-nanosecond one-shot DBR. NOP, a 190-millisecond one-shot, triggers on the leading edge of DBRS-P. Therefore, 250 microseconds after generating a power-fail interrupt, gate MREA is enabled to assert Master Reset, MRES-N (see figure 3).

RESET PUSHBUTTON REPB-N

Pushing reset on the control panel asserts REPB-N which resets flip-flop PBS to trigger one-shot COP. The trailing edge of COPR-N triggers 250-microsecond one-shot DBR and this, in turn, triggers 190-millisecond one-shot NOP. Therefore, NOPR-N disables precedence chain (PCDB-P) generation inhibiting any further bus access. This occurs 2.5 milliseconds after the bus controller senses REPB-N. Another 250 microseconds is allowed to elapse before gate MREA is enabled to assert master reset signal, MRES-N.

AUTO-LOAD, ATLD-N

If PRAL-N (LD sheet 5) is asserted at the end of Master Reset following power restart, the BCU asserts 100-nanosecond signal ATLD-N. PRAL-N can be asserted permanently by installing a program jumper between J2-1 and J2-2 in systems that contain no control panel and where Power Restart Auto-Load is required.

PRECEDENCE CHAIN, PCDB-P

The precedence chain signal is asserted by the BCU 20-40 nanoseconds after one of the select lines is asserted or one of the internal interrupts are detected at the inputs of gate PCDI (LD sheet 3). PCDB-P is a positive pulse 40-60 nanoseconds long established by delay line DL1 and gate PCDE. Precedence chain signal is inhibited 2.5 milliseconds after the BCU detects either Power Status (PWST-N) or Reset Pushbutton (REPB-N).

PROCESSOR NUMBER, CPU0-P, CPU1-P

The code corresponding to the processor number 0-3, using the INFIBUS in any one system is established by the polarity of CPU0-P and CPU4-P. Since the BCU is allocated only to CPU #0 and connected to it at the input/output connector, CPU0-P, CPU1-P are grounded on the BCU.

CLOCK, CLKA-N

A 25-MHz oscillator generates this signal in the BCU for use by other system modules.

DEFINITIONS OF OTHER LOGIC TERMS ON LD SHEET 6

PRID-P	Power restore pulse that occurs at the end of a 50 millisecond master reset, following negation of power status (PWST-N).
PFID-P	Power fail pulse generated when power status, PWST-N is detected.
PCDE-P	Any selected service request or internal interrupt.
LFID-P	A pulse generated once each line frequency (60 Hz) cycle.

BUS CONTROLLER/CPU INTERFACE

Table 1 is a list of the input/output signals to and from the Bus Controller on the input/output connector. The signals are listed in alphabetical order of mnemonics.

Table 1. Bus Controller Input/Output Signals

Signal Mnemonic	Function	I/O Connector Pin Number	Source	Logic Diagram Sheet Number
CPU0-P	CPU Code (grounded)	JA05	BCU	6
CPU1-P	CPU Code (grounded)	JB05	BCU	6
DN0L-P	Device Number on Line	JB03	BCU	5
IL0R-N	Interrupt Level Bit 0	JA06	BCU	3
IL1R-N	Interrupt Level Bit 1	JB06	BCU	3
LB12-P	Mask Level 1	JA53	CPU	2
LB13-P	Mask Level 2	JA51	CPU	2
LB14-P	Mask Level 3	JA52	CPU	2
LB15-P	Mask Level 4	JA50	CPU	2
NEXT-N	CPU Interrupt	JB04	BCU	2
SCM3-N	Permit Interrupt	JA04	CPU	3
STAT-N	Set Masking Status	JA03	CPU	2

DRAWINGS AND PARTS LISTS

This is a list of the drawings and parts lists included in this bulletin.

Title	Mnemonic	Drawing Number	Sheets
Bus Control Unit Circuit Card	BCU	2001002128-1	1
Bus Control Unit Logic Diagram	BCU	LD2001002128-1	1 thru 7
Bus Control Unit Parts List	BCU	PL2001002128-1	2,3
		PL2001002128-2	4

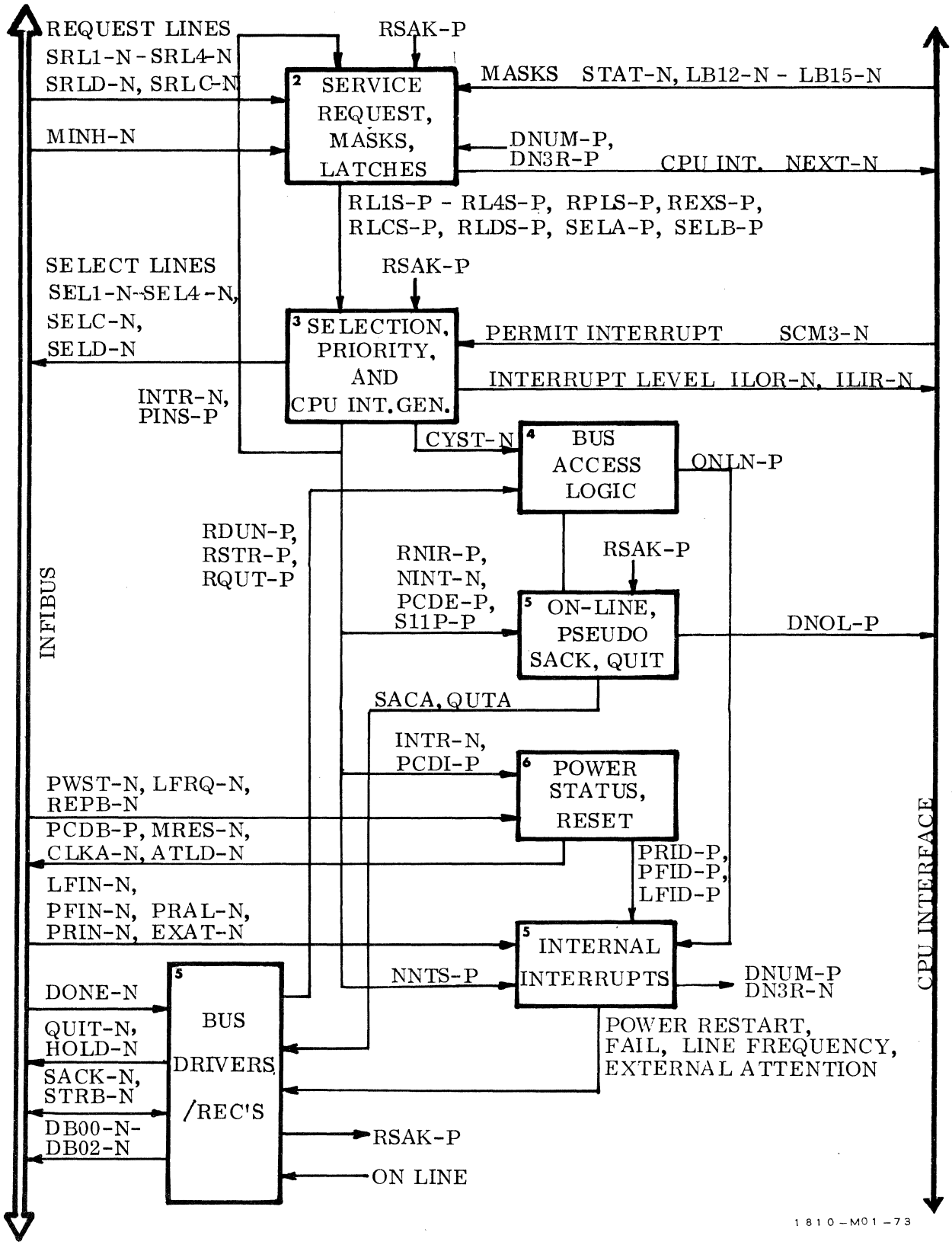


Figure 1. 1810 Bus Controller Functional Block Diagram

BCU

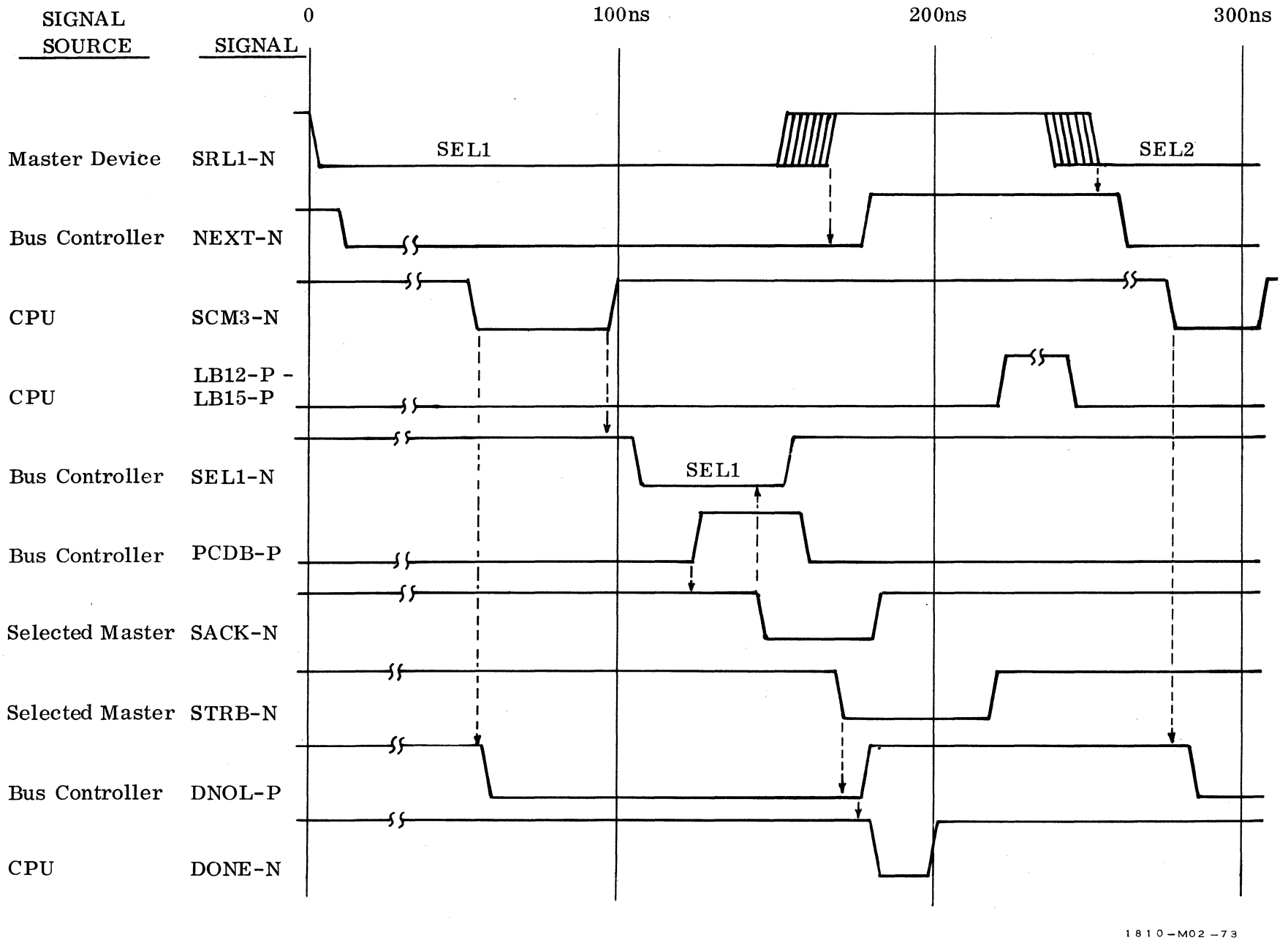


Figure 2. Bus Request and CPU Interrupt, Timing Diagram

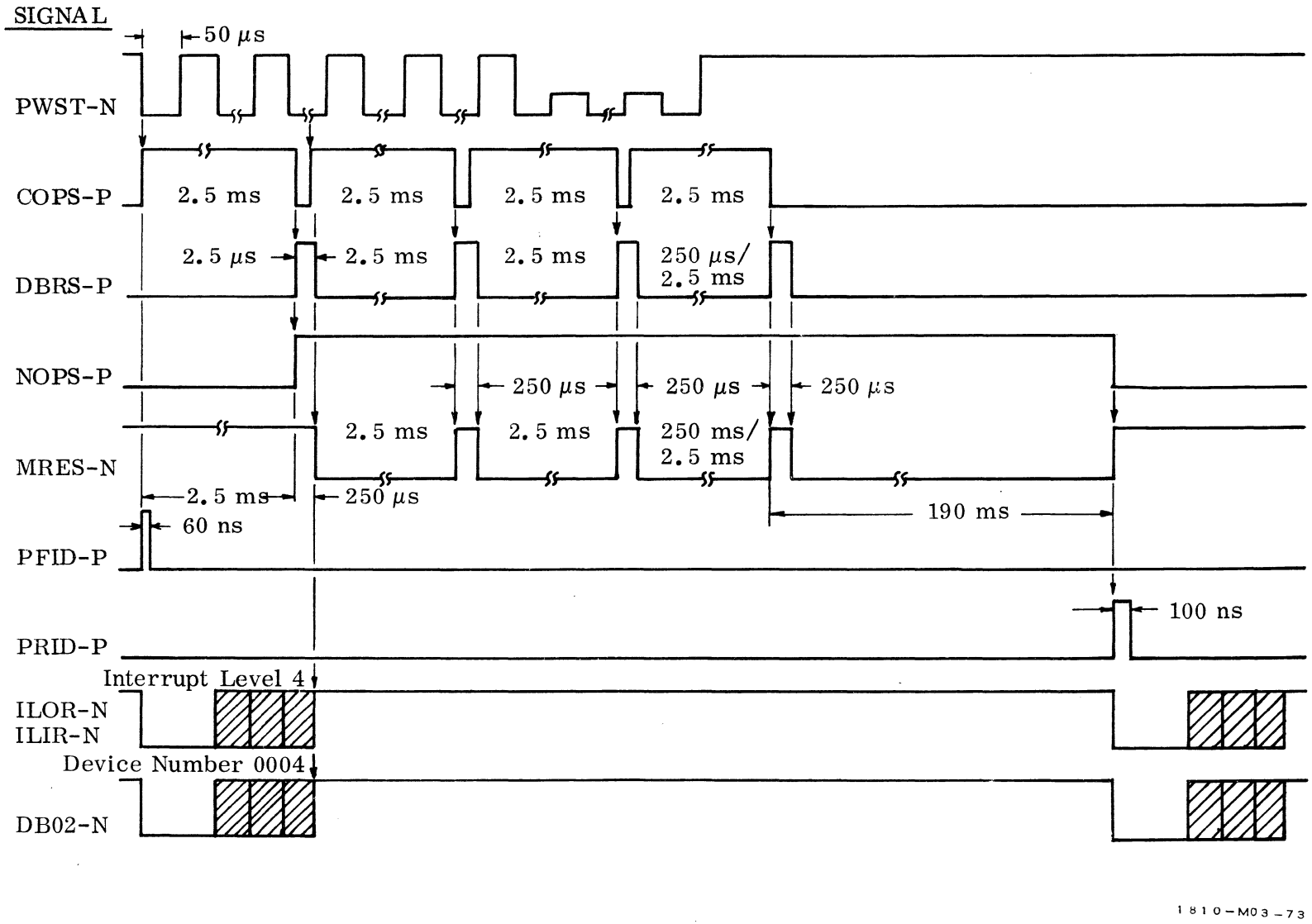
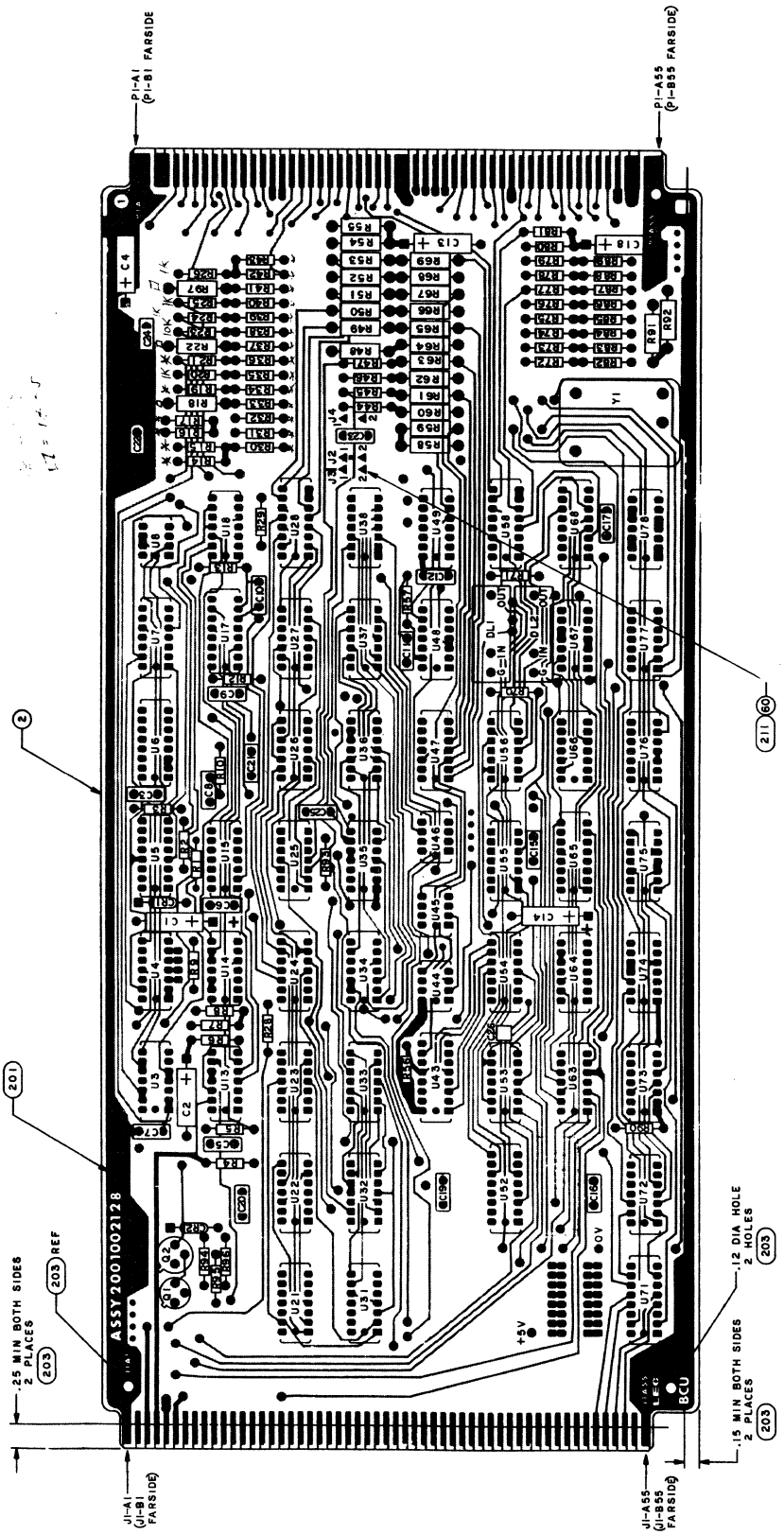


Figure 3. Power Status, Master Reset, and Interrupts Sequence, Timing Diagram



Bus Control Unit Circuit Card (BCU)
2001002128-1, Rev. G, Sheet 1

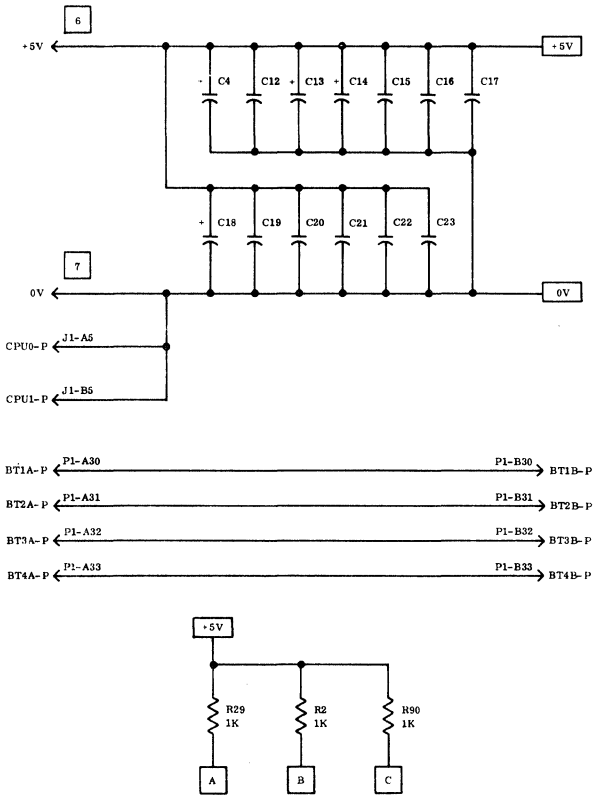
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33UF, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR PIN 7 AND 8 0V, PIN 16 +5V.

[6] +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51.

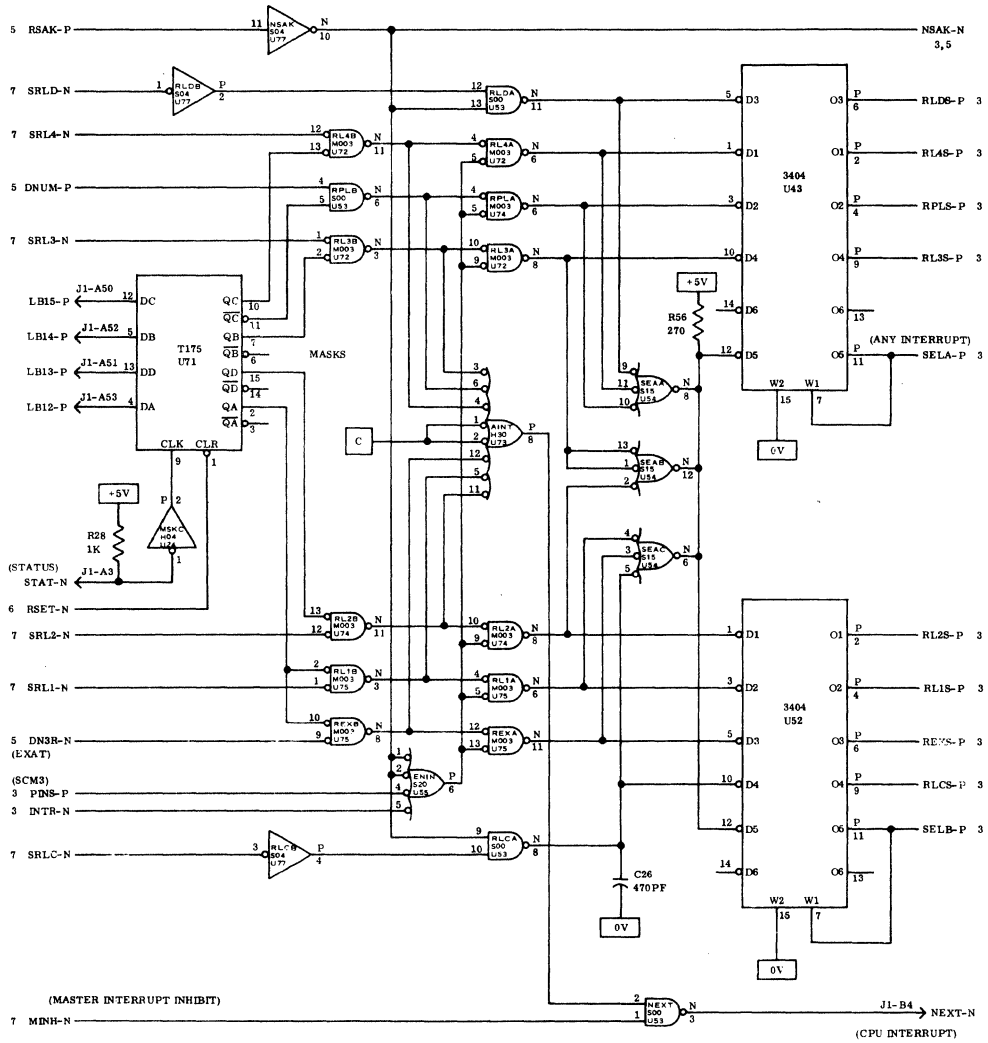
[7] 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J1-A1, A55, B1, B55.

8. ALL DIODES ARE 8001100001-1.



BCU

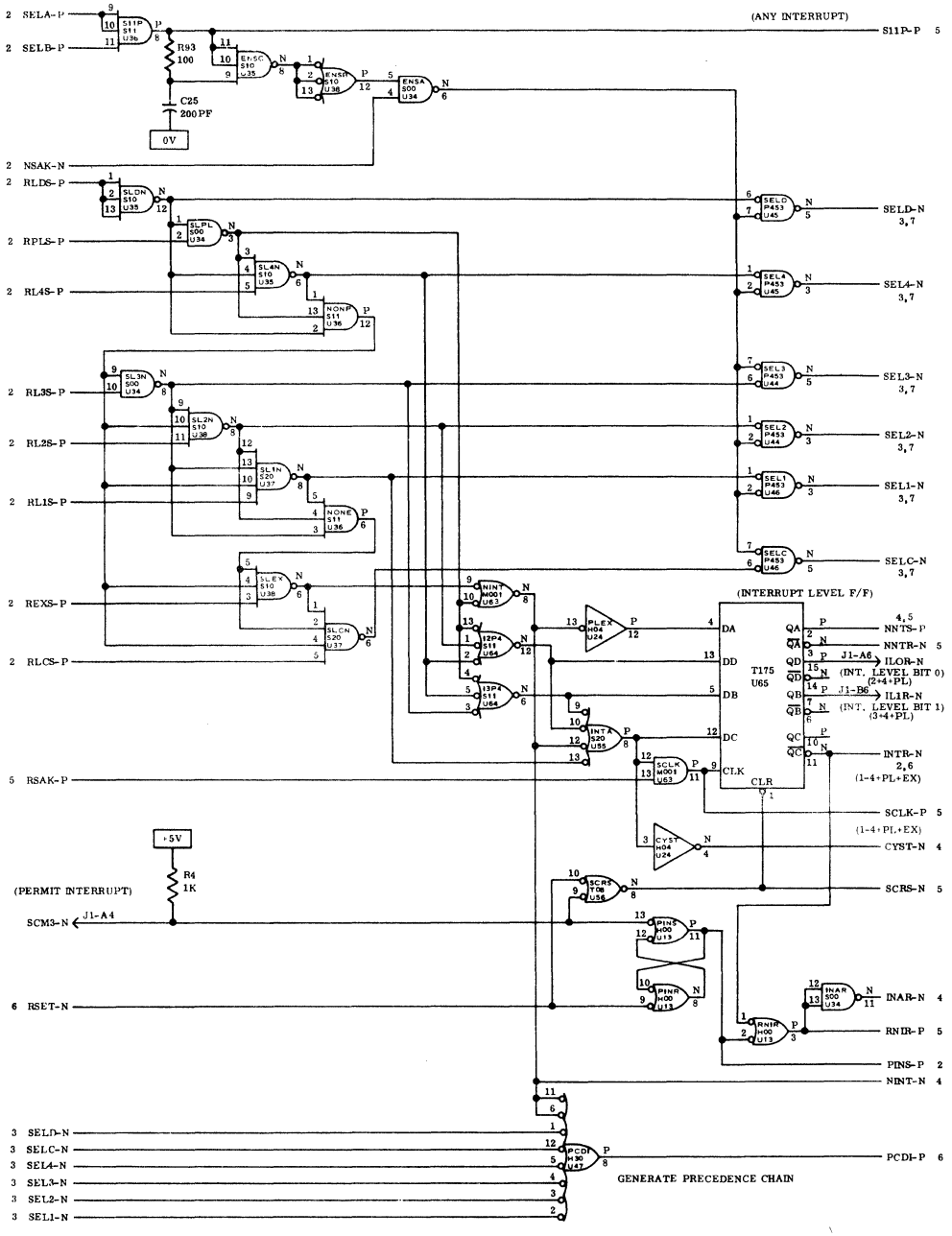
Bus Control Unit Logic Diagram (BCU)
LD2001002128-1, Rev. G, Sheet 1 of 7



SERVICE REQUEST MASKS AND LATCHES

BCU

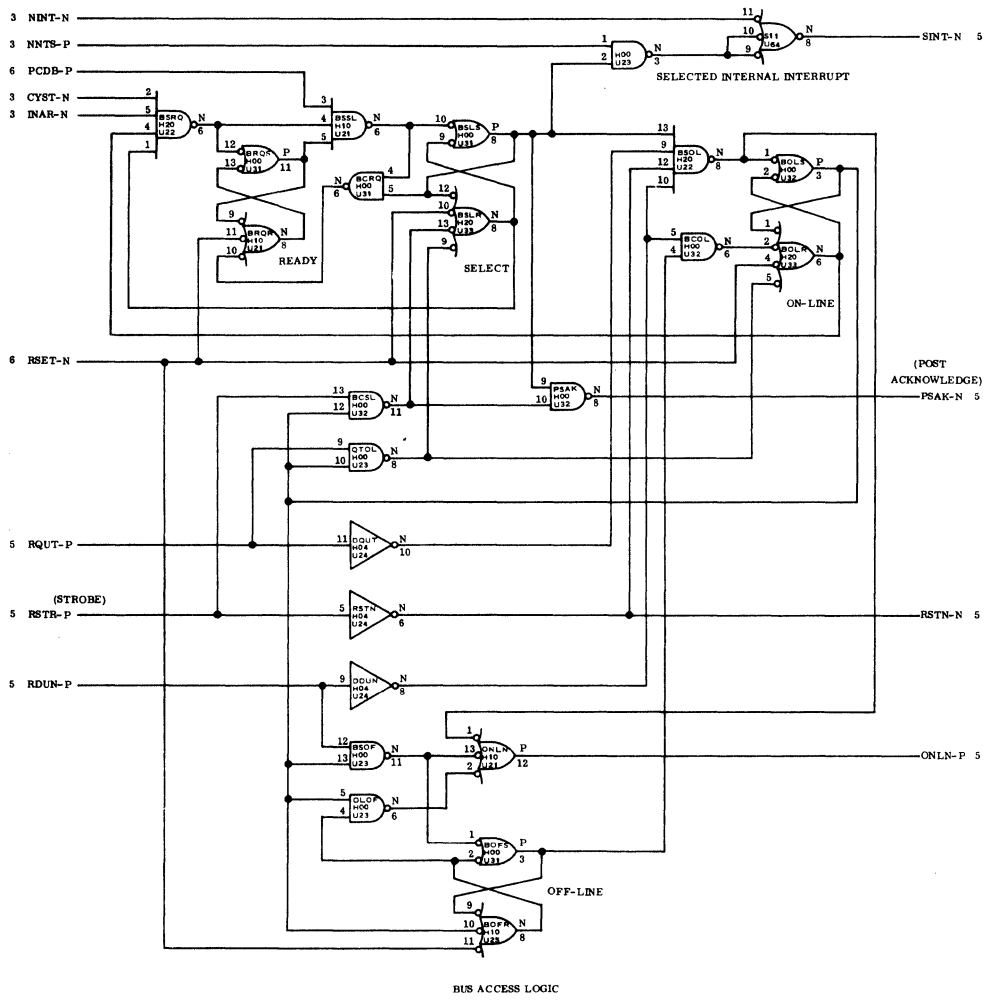
BUS Control Unit Logic Diagram (BCU)
LD2001002128-1, Rev. G, Sheet 2 of 7



SERVICE REQUEST SELECTION AND CPU INTERRUPT GENERATION

BCU

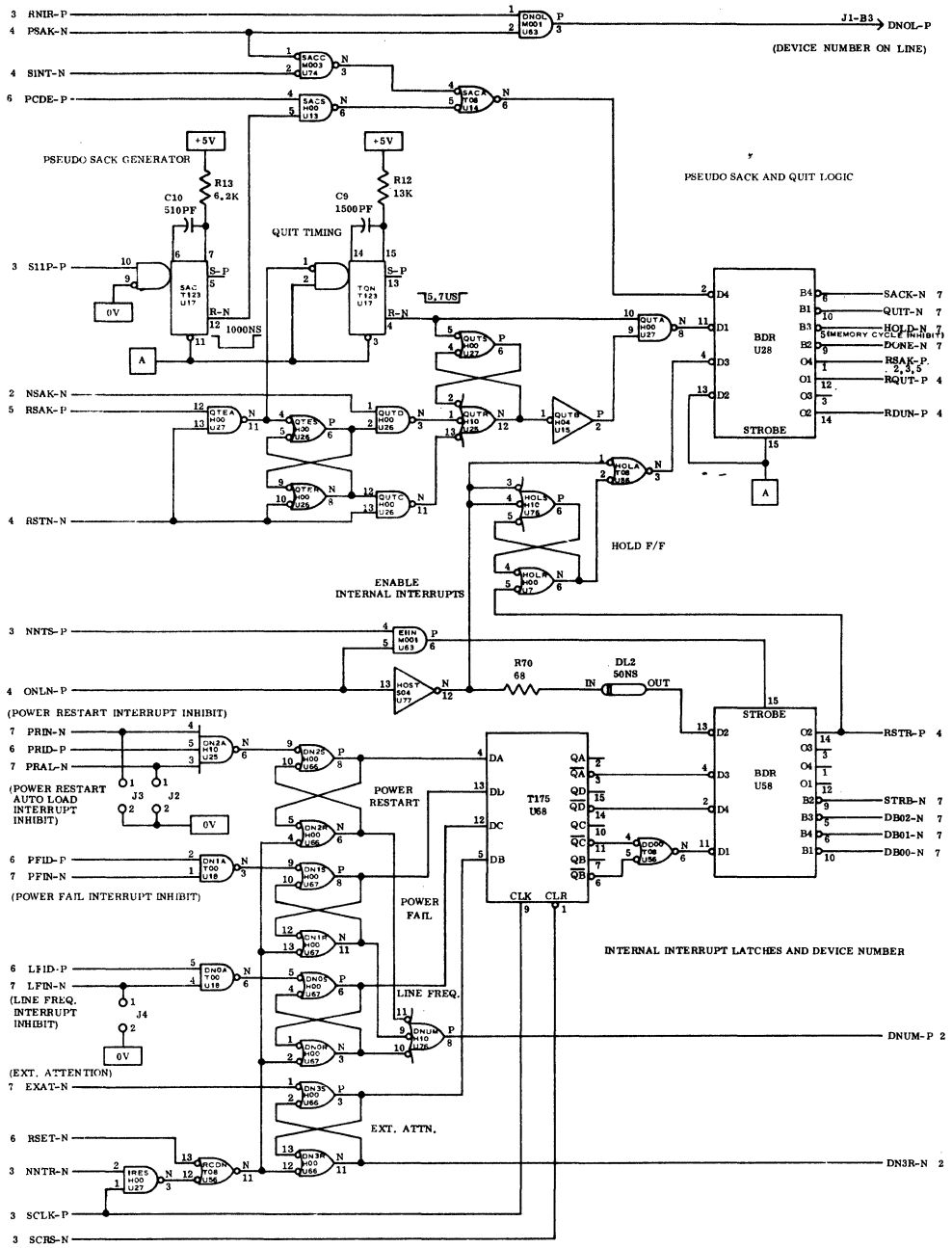
BUS Control Unit Logic Diagram (BCU)
LD2001002128-1, Rev. G, Sheet 3 of 7



BUS ACCESS LOGIC

BCU

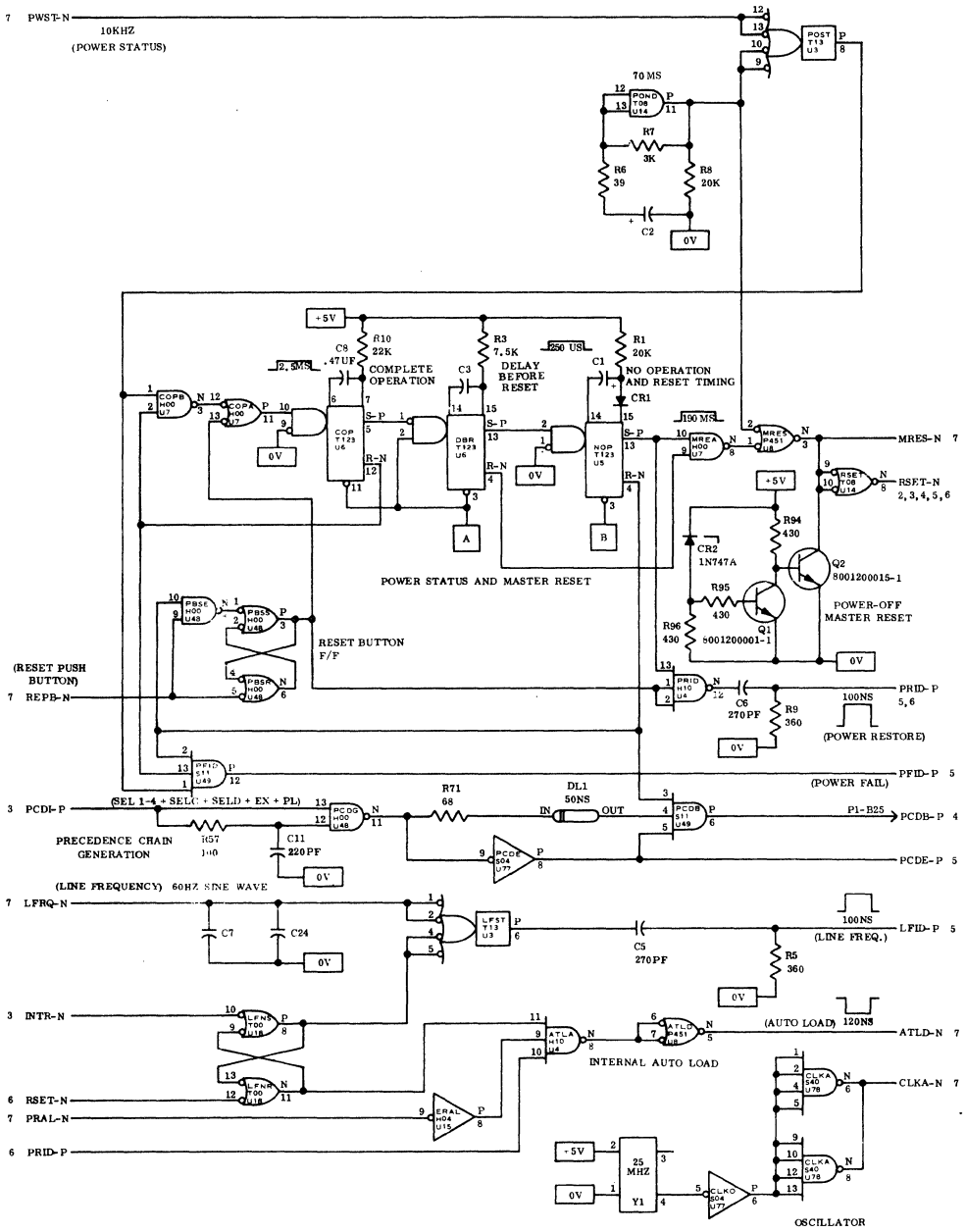
Bus Control Unit Logic Diagram (BCU)
LD2001002128-1, Rev. G, Sheet 4 of 7



DRAWING NO.	CONNECT
LD2001002128-2	J3-1 TO J3-2 J4-1 TO J4-2

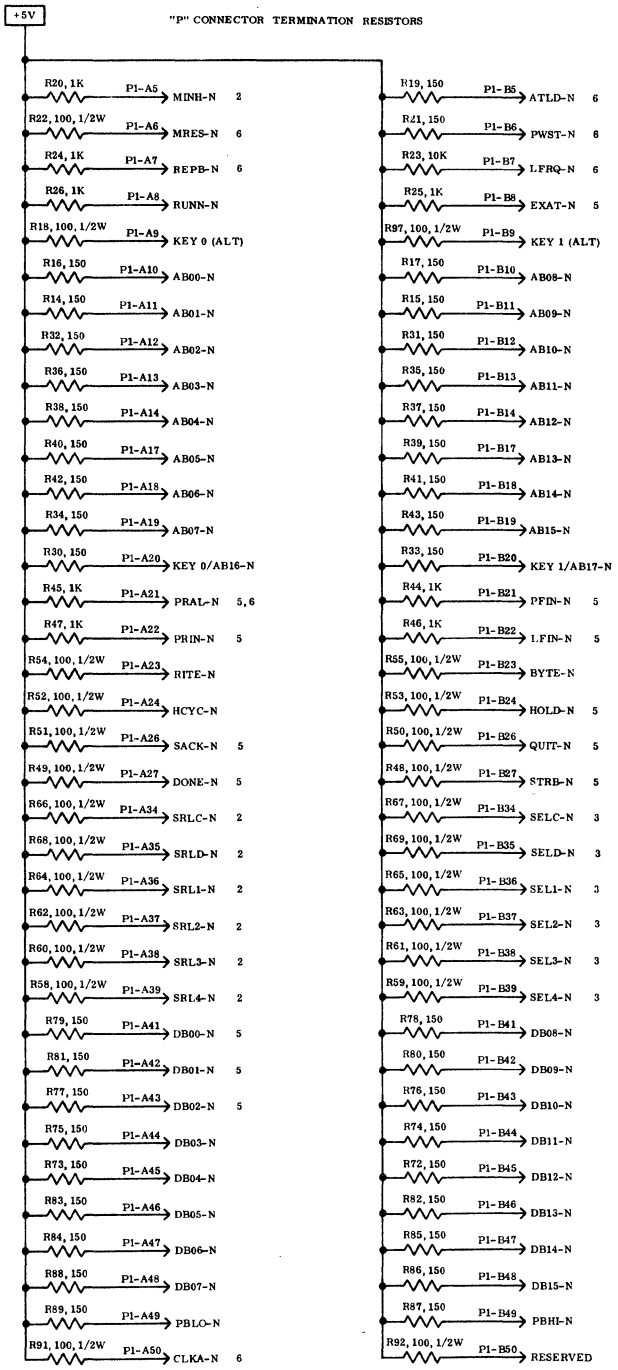
BCU

Bus Control Unit Logic Diagram (BCU)
LD2001002128-1, Rev. G, Sheet 5 of 7



Bus Control Unit Logic Diagram (BCU)
LD2001002128-1, Rev. G, Sheet 6 of 7

BCU



BCU

Bus Control Unit Logic Diagram (BCU)
LD2001002128-1, Rev. G, Sheet 7 of 7

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002128-1		BCU-CKT CARD ASSY		USED ON SUE 1810-1	1
002		001	0001		1001004721-1		PRINTED WRG BD, BCU			2
003		000								3
004		001	0001		RL07S103G		RESISTOR	MIL-R-22684/1	R23 .5 IS	4
005		001	0001		RL07S390G		RESISTOR	MIL-R-22684/1	R6 .5 IS	5
006		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R70,71 .5 IS	6
007		002	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R57,93 .5 IS	7
008		038	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R14 THRU R17, R19,21,R30 THRU R43,R72 THRU R89 .5 IS	8
009		001	0001		RL07S271G		RESISTOR	MIL-R-22684/1	R56 .5 IS	9
010		002	0001		RL07S361G		RESISTOR	MIL-R-22684/1	R5,9 .5 IS	10
011		013	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R2,4,20 R24 THRU R26,R28,29,R44 THRU R47,R90 .5 IS	11
012		001	0001		RL07S302G		RESISTOR	MIL-R-22684/1	R7 .5 IS	12
013		000								13
014		001	0001		RL07S622G		RESISTOR	MIL-R-22684/1	R13 .5 IS	14
015		001	0001		RL07S133G		RESISTOR	MIL-R-22684/1	R12 .5 IS	15
016		001	0001		RL07S752G		RESISTOR	MIL-R-22684/1	R3 .5 IS	16
017		000								17
018		002	0001		RL07S203G		RESISTOR	MIL-R-22684/1	R1,8 .5 IS	18
019		025	0001		RL20S101G		RESISTOR	MIL-R-22684/2	R18,22,R48 THRU R55,R58 THRU R69,R91,92,97 .6 IS	19
020		001	0001		RL07S223G		RESISTOR	MIL-R-22684/1	R10 .5 IS	20
021		003	0001		RL07S431G		RESISTOR	MIL-R-22684/1	R94,95,96 .5 IS	21
022		000								22
023		001	0001		8001300013-1		CAPACITOR		C26 (470 PF)	23
024	F	012	0001		8001300101-1		CAPACITOR		C3,7,12,15,16, 17,C19 THRU C24 .25 IS (.1 UF)	24
025	F	001	0001		8001300103-1		CAPACITOR		C8 .25 IS (.47 UF)	25
026		002	0001		CM05FD221J03		CAPACITOR	MIL-C-5/18	C11,25 .25 IS (220 UUF)	26
027		002	0001		CM05FD271J03		CAPACITOR	MIL-C-5/18	C5,6 .25 IS (270 UUF)	27
028		001	0001		8001300065-1		CAPACITOR		C10 .25 IS (510 UUF)	28
029		006	0001		8001300311-2		CAPACITOR		C1,2,4,13,14,18 .8 IS (33 UF)	29
030		001	0001		8001300016-1		CAPACITOR		C9 .25 IS (1500 UUF)	30

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
031		001	0001		1N747A		DIODE, ZENER		CR2 .5 IS	31
032	E	001	0001		8001100001-1		DIODE		CR1 .5 IS	32
033	F	001	0001		8001200001-1		TRANSISTOR		Q1 (TO18)	33
034	F	001	0001		1005000797-1		OSCILLATOR		Y1 (25MHZ)	34
035	E	001	0001		8001200015-1		TRANSISTOR		Q2 (TO5)	35
036		000								36
037	F	010	0001		8001800042-1		ICP		U7,13,23,26,27, 31,32,48,66,67 (74H00)	37
038	F	002	0001		8001800044-1		ICP		U15,24 (74H04)	38
039	F	004	0001		8001800046-1		ICP		U4,21,25,76 (74H10)	39
040	F	002	0001		8001800048-1		ICP		U22,33 (74H20)	40
041	F	002	0001		8001800051-1		ICP		U47,73 (74H30)	41
042	F	001	0001		8001800072-1		ICP		U18 (7400)	42
043		002	0001		8001800123-1		ICP		U28,58 (BDR)	43
044	F	002	0001		8001803126-1		ICP		U14,56 (7408)	44
045	F	001	0001		8001803129-1		ICP		U3 (7413)	45
046	F	003	0001		8001803155-1		ICP		U5,6,17 (74123)	46
047	F	003	0001		8001803181-1		ICP		U65,68,71 (74175)	47
048		001	0001		SN75451P	01295	ICP	TEXAS INSTR INC	U8	48
049		003	0001		SN75453P	01295	ICP	TEXAS INSTR INC	U44,45,46	49
050	F	002	0001		8001803198-1		ICP		U34,53 (74S00)	50
051	F	001	0001		8001803200-1		ICP		U77 (74S04)	51
052	F	002	0001		8001803202-1		ICP		U35,38 (74S10)	52
053	F	003	0001		8001803203-1		ICP		U36,49,64 (74S11)	53
054	F	001	0001		8001803204-1		ICP		U54 (74S15)	54
055	F	002	0001		8001803205-1		ICP		U37,55 (74S20)	55
056	F	001	0001		8001803207-1		ICP		U78 (74S40)	56
057		001	0001		MC3001P	04713	ICP	MOTOROLA	U63	57
058		003	0001		MC3003P	04713	ICP	MOTOROLA	U72,74,75	58
059		002	0001		P3404	34649	ICP	INTEL CORP	U43,52	59
060	F	006	0001		1005000764-1		PIN, TERMINAL		NOTE 211	60
061		000								61
062		000								62
063	E	002	0001		8001600008-1		DELAY LINE, FIXED		DL1,2 (50 NS)	63
064		REF	0001		LD2001002128-1		LOGIC DIAGRAM			64
065		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65

BCU

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002128-2		BCU-CKT CARD ASSY		USED ON SUE 1810-2	1
002		001	0001		2001002128-1		BCU-CKT CARD ASSY			2
003		002	0001		900340041 7-10		WIRE, INSUL		30AWG WHT APPROX INCH REQD	3
004		REF	0001		LD2001002128-2		LOGIC DIAGRAM			4
							WIRE LIST			
							FROM TO FIND NO.			
							J3-1 J3-2 3			
							J4-1 J4-2 3			
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARKING (IDENTIFY).			201
202		000								202
203		REF	0001				AREA TO BE FREE OF SOLDER.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205		REF	0001				COMPONENT HEIGHT .395 MAXIMUM.			205
206		REF	0001				PROTRUSION SIDE 2, .075 MAXIMUM, LEADS TO BE VISIBLE THRU SOLDER.			206
207		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010 INCH/INCH IN GENERAL AREA AND .005 INCH/INCH IN CONNECTOR AREA.			207
208		REF	0001				SQUARE PAD DENOTES CATHODE END (STRIPE) OF DIODE, OR POSITIVE (+) END OF CAPACITOR, OR PIN 1 OF XFR.			208
209		REF	0001				RECTANGULAR PAD AND DOT OR SLOTTED END OF ICP DENOTES PIN 1.			209
210		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			210
211		REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			211

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	5-20-74	
B	ECN 281	4-12-78	EC

BCU

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BCU TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		BCU-05

SCALE	REV	SHEET
	B	/ OF 3

BCU - BUS CONTROL UNIT Lockheed

Status - none

Switches - Auto Reset
S1 UP disabled
S1 DOWN enabled

Jumpers

J4-1 to J4-2	inhibits line frequency interrupts (only newer cards)
J2-1 to J2-2	at power restart do autoload otherwise do an interrupt
J3-1 to J3-2	inhibit power restart (only newer cards)
J5-1 to J5-3	60 cycle interrupt enabled after reset
J5-2 to J5-3	60 cycle interrupt disabled after reset

(J5-1 and J5-2 are near the center of the board. J5-3 is in the upper left corner.)

Card Type BCU Modification P,M,I

Card Function: Bus Controller

Modification Description:

Extend QUIT delay as appropriate for each bus type. Only one of these modifications should be present on a board.

BCU

Implementation: See drawing attached

M--no modification

P--install .1 µfd disc capacitor across C9

I--install .01 µfd disc capacitor across C9

C9 is a small capacitor mounted vertically near the center line of the board about a quarter of the way from the top.

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12-16-74	
B	ECN 0167	10-16-75	R. B[illegible]
C	ECN 0217	7/15/76	[illegible]
D	ECN 0238	2/14/77	[illegible]
E	ECN 0254	7/22/77	[illegible]
F	ECN 281	4/12/78	E. Cox
G	ECN 295	5/2/78	E. Cox

BCU

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER [illegible]

APP'D FOR REL [illegible]

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BCU ASSEMBLY (MODIFICATION)

SIZE	CODE IDENT NO.	DRAWING NO.
A		BCU-15

SCALE	REV G	SHEET 1 OF 11

BCU Assembly (Modification)

1. This modification applies to Lockheed BCU's (BBN #248) whose artwork revision levels are shown in the lower right-hand corner to be "D".

2. Additional parts required:

BBN #	QTY	ITEM
22	1	220 UFD/10V CAPACITOR
28	1	1K OHM 1/4 W 5% RES
37	1	1000 PF/1000V DISC CAP
74	1	7411 I.C.
88	1	74123 I.C.
130	1	CIT-10 TAG
165	1	T8201 SWITCH
181	1	6-32X1/4 NYLON SCREW
262	1	47K OHM 1/4W 5% RES
263	1	IN4148 DIODE
264	2	16-PIN CONTACT SOCKETS
1344	4	1/32"X3/4" NEOPRENE DOUBLE-SIDED TAPE (IN.)

3. Install plastic tag showing board type and serial number.

4. Make the following cuts on the solder side of the board as shown in Figure 3:

   a. U43:7 ⟶ U43:11

   b. U52:7 ⟶ U52:11

   c. U37:5 ⟶ U52:9

5. Make the following cuts on the component side of the board (see Figure 1):

   a. U3:9 ⟶ U3:10

   b. U18:13 (cut trace from this pin about 1/8" from the pin)

6. Remove jumpers at J2, J3, and J4 if present (see Figure 1)

7. Cut and lift the I.C. leads at U43:15 and U52:15 (see Figure 1)

8. Install the following (locations referenced in Figure 1):

   a. Wirewrap pins A, B, C, F1, F2, F3, U4:3, U4:4, U4:5, and U4:6

   b. Place two pieces of doublesided tape on the component mounting areas shown in Figure 2.

   c. Mount 16 pin sockets, 220 UFD capacitor, and switch as shown in Figure 2.

   d. Clip off the rightmost 2 posts of the socket below U52 and install 7411. This location will be referred to as U79.

   e. Install 74123 in the socket above U61. This will be referred to as U80.

   f. Solder the following as shown in Figure 2:

BCU

1. 1K ohm resistor from Pin 8 to Pin 3 of the switch (S1)

2. + (right) end of 220 UFD capacitor as low as possible on U80:9

3. - (left) end of 220 UFD capacitor as low as possible on U80:14

4. 47K ohm resistor from Pin 8 to U80:9, as low as possible.

5. IN4148 from U80:9 to U80:15, with the band toward pin 15, soldering as low as possible to the pins.

g. Install 1000 pf capacitor across C11 (see Figure 1)

9. Make the following connections:

a. Jumper U37:4 to U37:5 on the solder side of the board (see Figure 3)

b. Solder to I.C. leads (see Figure 1):

U52:15 ⟶ U52:7

U43:15 ⟶ U43:7

U52:7 ⟶ U43:7

U3:10 ⟶ U76:12

U15:3 ⟶ U47:8

U76:1 ⟶ U76:2

U76:1 ⟶ S1:3

c. Solder Wirewrap (as low as possible)

U63:7 ⟶ U79:7

U63:14 ⟶ U79:14

U34:4 ⟶ U79:1

U14:8 ⟶ U79:2

U36:8 ⟶ U79:13

U43:15 ⟶ U79:6

U15:4 ⟶ U4:3

S1:4 ⟶ Pin A

U73:1 ⟶ U80:3

U76:13 ⟶ U80:4

U3:5 ⟶ Pin F1

U18:13 ⟶ Pin F2

U18:12 ⟶ Pin F3

BCU

d. Wirewrap as low as possible:

U79:12 ⟶	U79:11	(1)
U79:10 ⟶	U79:9	(1)
U79:10 ⟶	U79:11	(2)
U79:8 ⟶	U79:5	(1)
U79:4 ⟶	U79:3	(1)
U79:5 ⟶	U79:4	(2)
Pin B ⟶	U80:16	(1)
U4:3 ⟶	U4:4	(2)
U4:5 ⟶	Pin C	(1)
U4:6 ⟶	U80:2	(1)
U80:1 ⟶	U80:8	(1)

U80,8 ——————→ Pin A (2)

e. Using wire of a different color, jumper Pin F1 to Pin F2

10. Cut any pins which are in excess of .395" from the board.

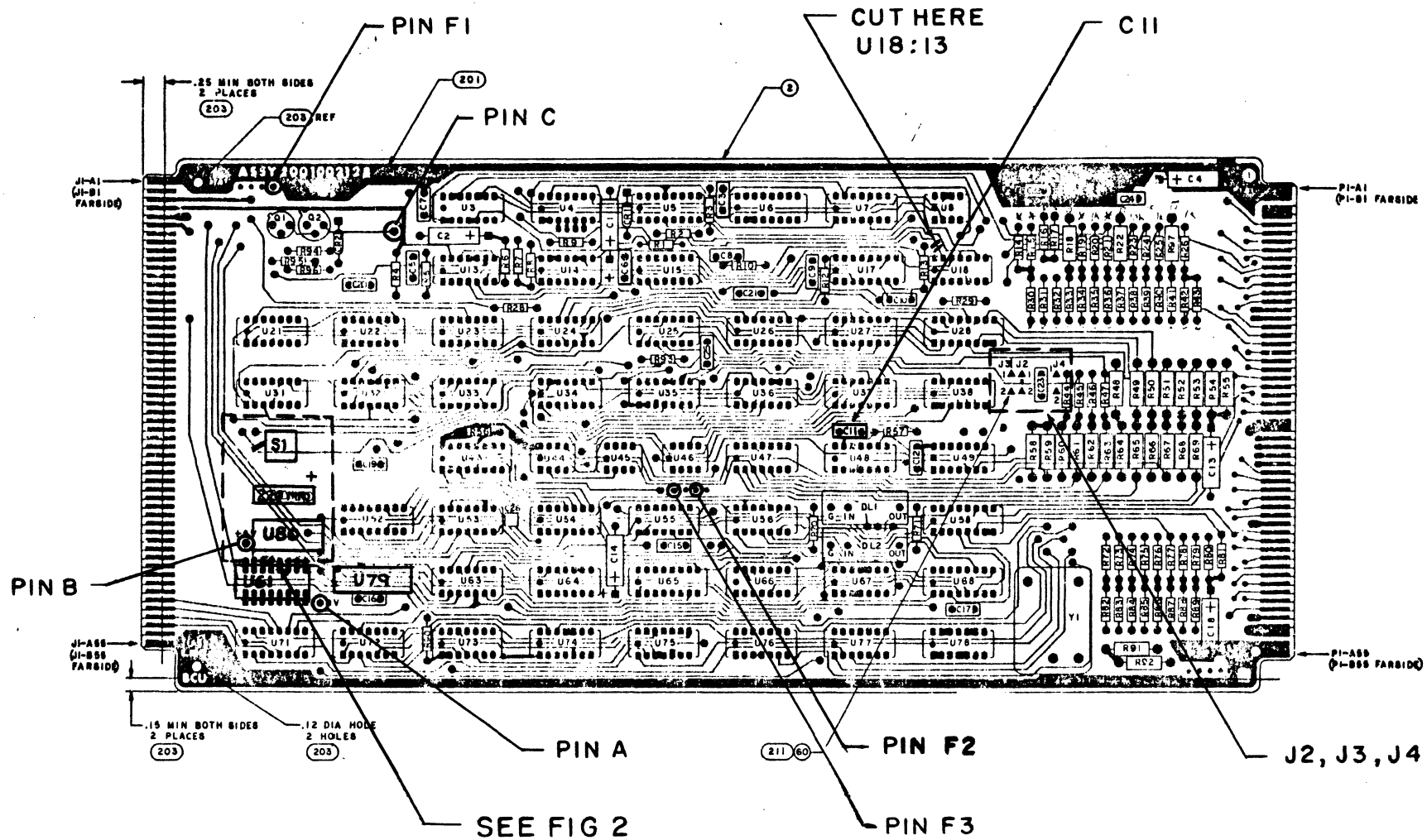

PIN F1
CUT HERE
U18:13
C11
PIN C
PIN B
PIN A
PIN F2
PIN F3
J2, J3, J4
SEE FIG 2
.25 MIN BOTH SIDES
2 PLACES
.15 MIN BOTH SIDES
2 PLACES
.12 DIA HOLE
2 HOLES
BCU

FIG 1

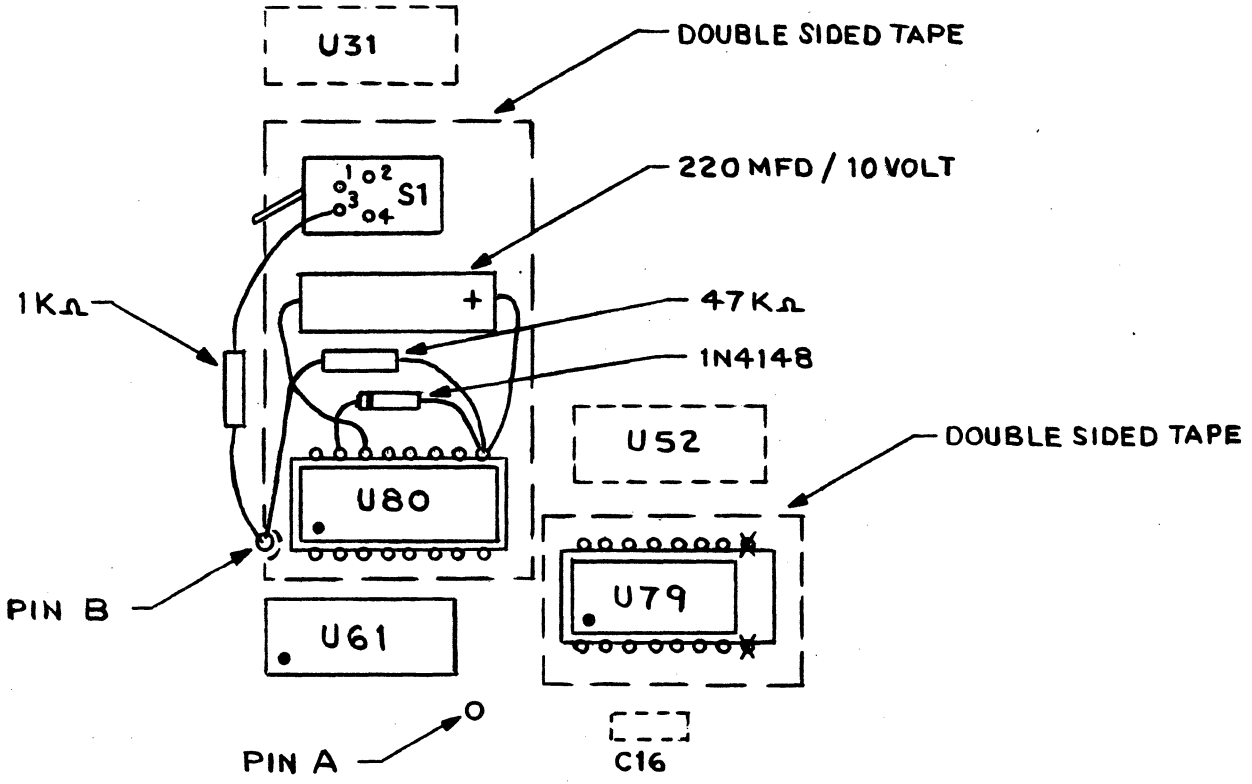

U31
DOUBLE SIDED TAPE
220 MFD / 10 VOLT
S1
1
2
3
4
+
1KΩ
47KΩ
1N4148
U52
DOUBLE SIDED TAPE
U80
U79
PIN B
U61
PIN A
C16

FIG 2

BCU-15 REV

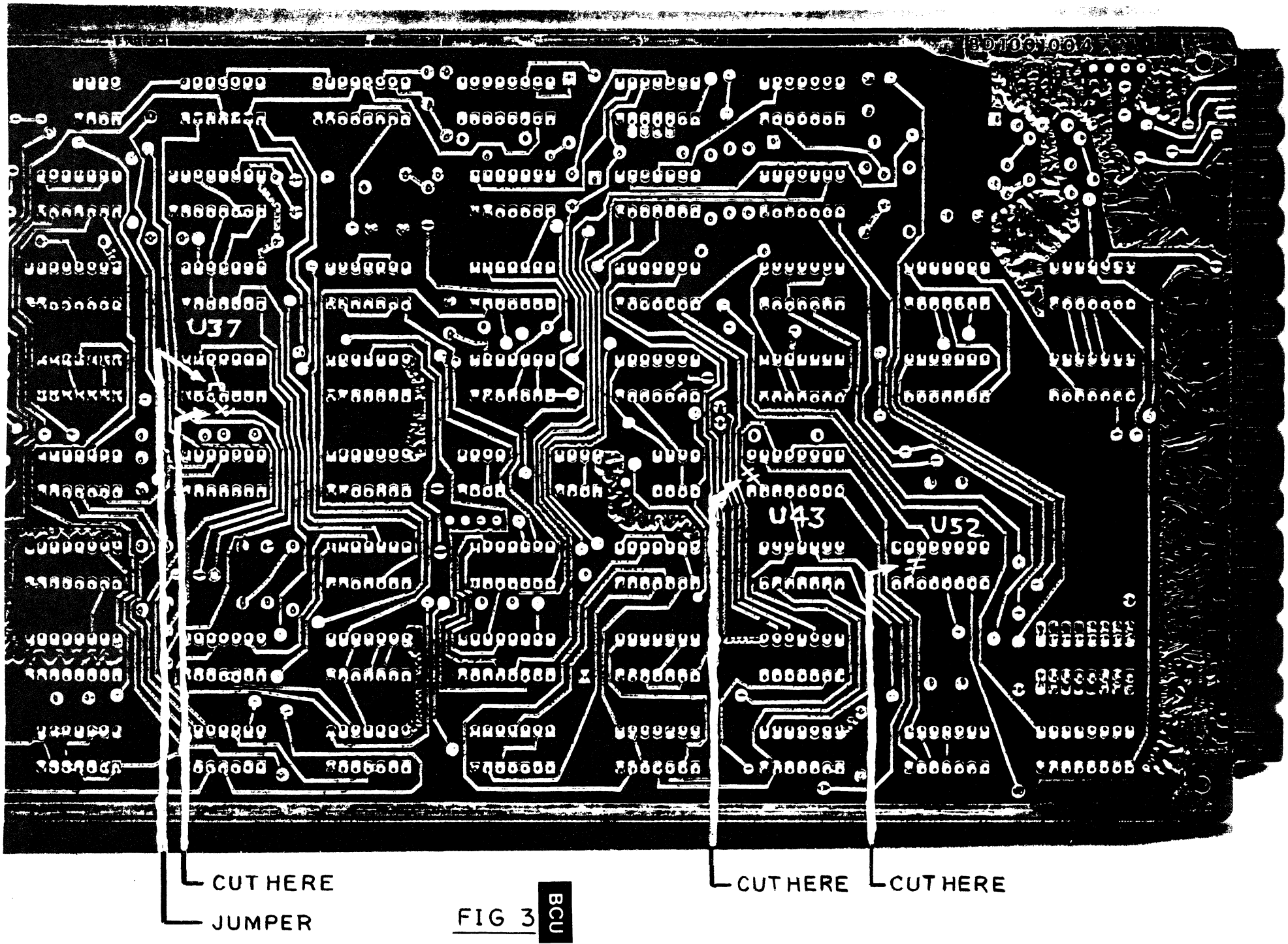
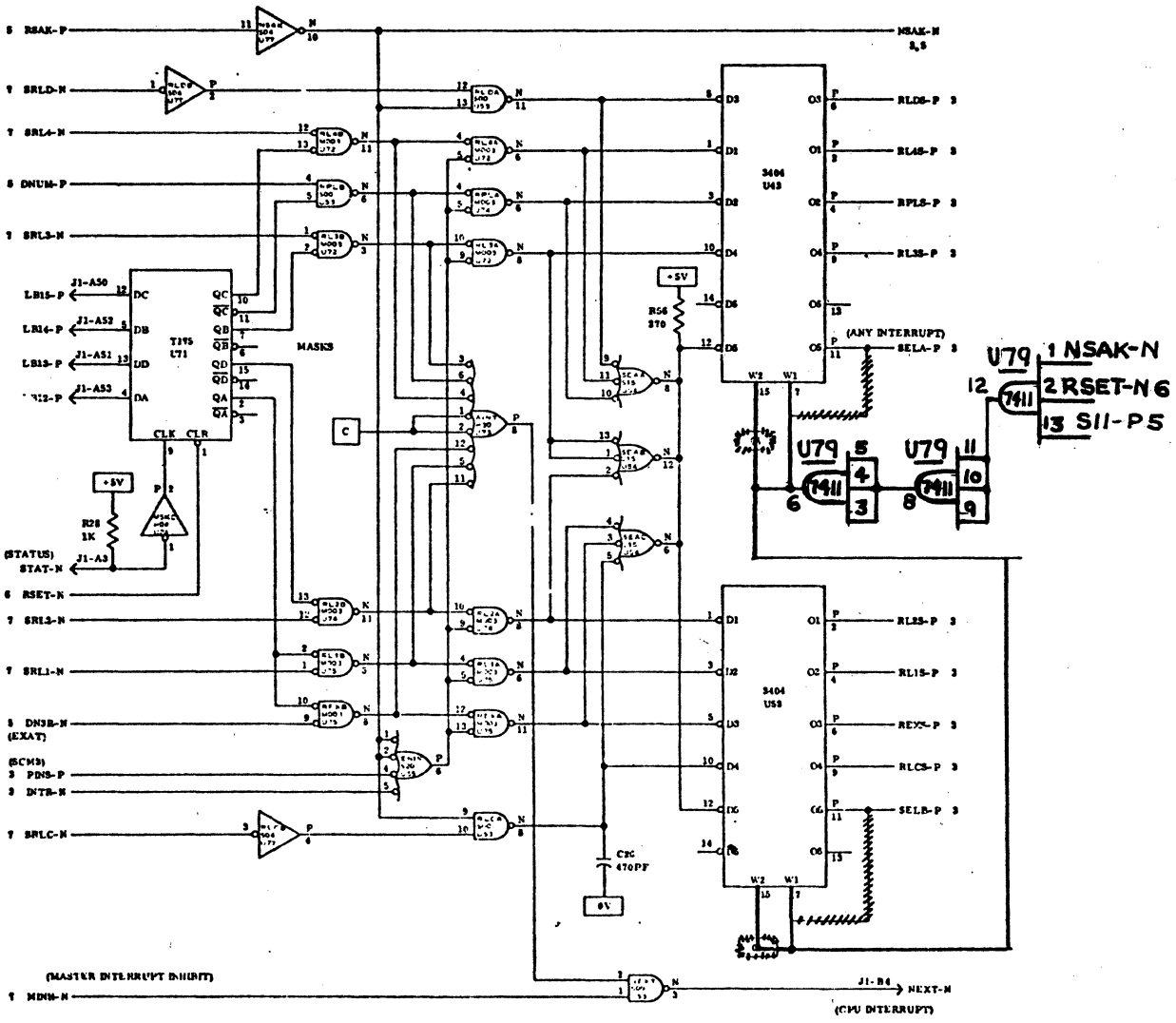


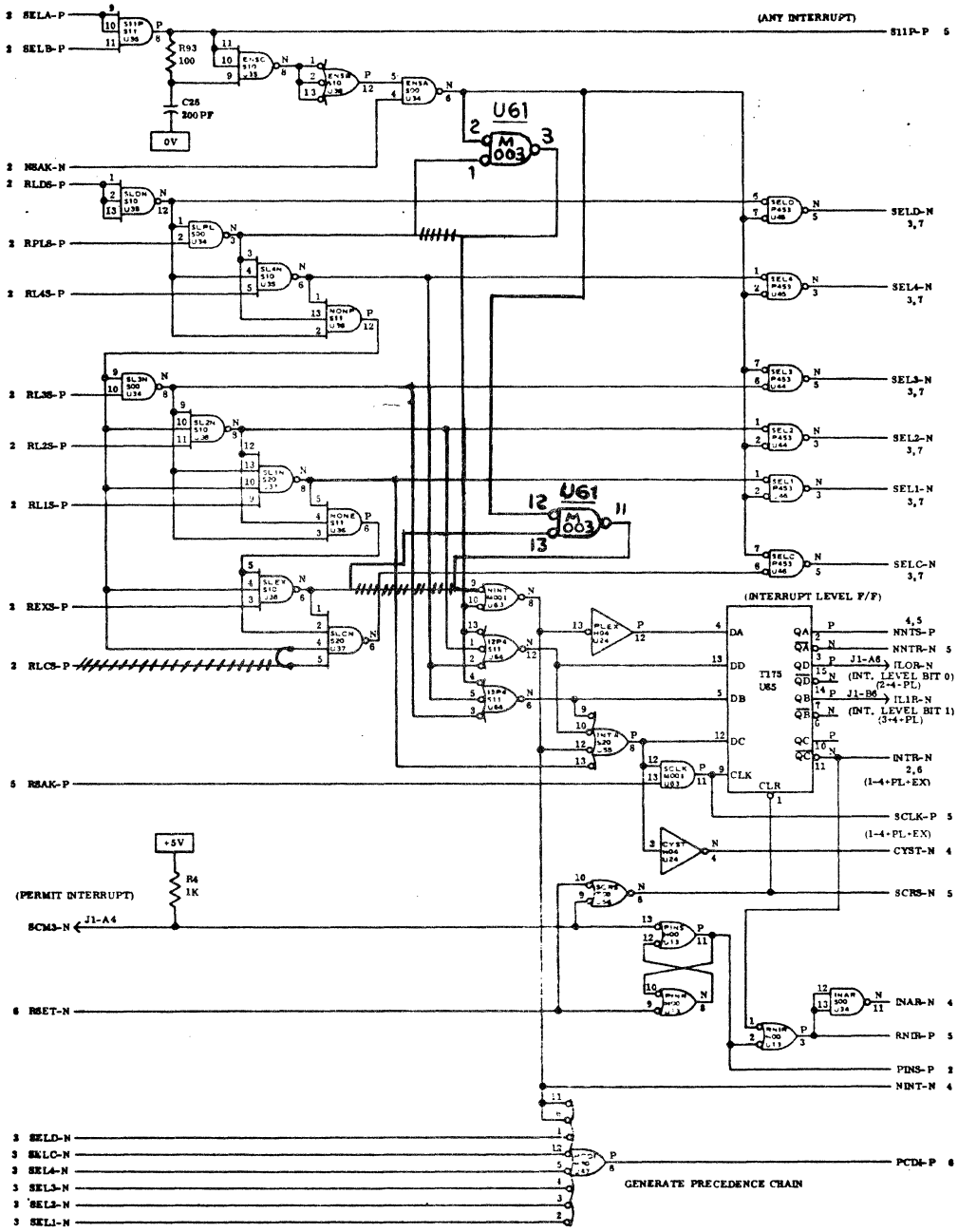
FIG 3 BCU



SERVICE REQUEST MASKS AND LATCHES

BCU-15 REV G STANDARD MOD

NOTE: U61 CHANGES PER LEC ECO# 19688



SERVICE REQUEST SELECTION AND CPU INTERRUPT GENERATION

BCU 15 REV G STANDARD MOD

BCU

Buffered Synchronous Line Interface

BLI-Ø2 Logic Description

BLI-Ø5 Technical Reference

BLI-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	8/30/77	

BLI

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN DRF

8/30/77

CHECKER

ENGINEER

APP'D FOR REL 8/30/77

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BLI LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		BLI-02

SCALE	REV	SHEET
	A	OF

BLI LOGIC DESCRIPTION

The reader is assumed to have read the functional specification for this card. In particular, the description of the "bit-map" Appendix A should be at hand while reading this logic description.

BLI20

Drawing 20 contains the logic for miscellaneous INFIBUS control signals. In the upper left, the discontinuous INFIBUS signals are carried from one side of the INFIBUS connector to the other. This includes the precedence pulse PCDAB+. The remaining four INFIBUS signals used actively in the card are the: Strobe, Done pulse, Master Reset, and Rite signals. These are interfaced in the BDR D1. The status of the Rite signal during a particular memory reference is held in a flip-flop whose outputs are RITE+ and RITE-. The upper portion of the drawing shows three 1K resistors used to generate positive logic signals for unused logic inputs throughout the card. Additionally, there are 4 single-pole switches and their associated pull up resistors used to generate signals in the Device-Type word (DT107 down through DT206). These perform no active logic function in the card but may be used to indicate baud rates or identify individual cards in a system.

BLI21

Drawing 21 shows the interface address decoding for this card. The logic is straightforward and conventional. At the left are 5 BDRs providing a direct interface to the INFIBUS. Their inputs are unused, and their outputs are used as part of the address selection logic. The switches on the card are used to select the address to be recognized by an individual card. To the right of center is a 13-input and-gate, whose output ADCOM- indicates that the address specified on the bus matches the switch settings on the card. Its inputs include bits 16-19 ungated, and bits 4-13 as selected by switches shown at the bottom of the drawing. The 7486 and 74136 bugs are exclusive-or circuits. Note 1 on the drawing indicates that a switch closure is used to specify recognition of a 1 in the corresponding address bit. It does this by grounding the 1 input of the exclusive-or circuit associated with it. For example, with ASL11- grounded by the lowest switch in the leftmost switch of A3, a positive gate output ABS11+ will occur when the second gate input AB11+ is high. This will occur when the associated BDR input is low, indicating assertion of AB11B- on the INFIBUS. The output of the 4 gates in C3 is a wired-and configuration going high only when bits 4-7 compare correctly.

At the bottom of the drawing, an additional de-skewing gate is used to delay the strobe pulse STRB+ by an amount equivalent to the delay in the individual data bits before triggering the flip-flop whose output is ME+. A gate is also provided to inhibit ADSTR+ from clocking the flip-flop if the bus HOLD signal is present. Note that until the address selection cycle is started the STRB+ pulse keeps the flip-flop in the "1" state. ME+ is a synchronized address selection signal used for all subsequent address dependent functions. Below this flip-flop is a 450 ns delay whose output ultimately generates a 60 ns DONE pulse.

In the upper right corner of the drawing is an octal decoder. Its inputs are the RITE signal, the low order address bits 1 and 3, and address bit 2 anded with MEPLS+. The octal decoder is strobed only on selection of the Data and Control words of a BLI. Each of the two independent halves of the BLI is provided with its own write-control, read-data and write-data decoded pulses. Below the octal decoder is a single and-gate whose output DRSTR+ is used to strobe the data BDRs during a read operation.

BLI22

Drawing 22 contains the data multiplexers and BDRs used to get data from the BLI to the INFIBUS. The four BDRs are shown at the left of the drawing. Logically preceding the BDRs is a set of latches (F2, G3) which are strobed with DRSTR+ at the beginning of a read cycle. Data to the latches is multiplexed by a combination of 74151s, 74153s, and 74LS158s, selected in a fashion as to optimize board real estate.

Selection of inputs to the multiplexers is accomplished by the state of the three lower address bits AB01+, AB02+, and AB03+. Reference to the functional spec bit assignment chart at this point will show which BLI bits appear on which INFIBUS data bits. The 74151s select a single bit to be latched, based on the three address bits. Their strobes are permanently enabled. Logical data input to the 74151s is true in form, and the complement output is used to match the requirement of the INFIBUS. The 74153 address selection looks only at AB03+ and AB02+, with the gate looking only at AB01-. For AB01+ false, a zero is put on DAT15+ and DAT14+ which is inverted to put a one on the INFIBUS. When AB01+ is true, the 74153 is enabled, which enables data for ST and DR. AB02+ and AB03+ select the data to be either ST and DR for one of the halves of the BLI. The 74LS158s are a bit trickier as the enable (G) is derived from a logical combination of AB01+ and AB02+ at G7. RDSEL- goes false when AB01+ and AB02+ are true, which enables the 74LS158 for data read (DR) only, presenting ones on the output when not selected.

The 74LS158s complement the data passing through them. The selection of which half of the BLI is done by AB03+ going to the S input.

BLI 23-24

Drawings 23 and 24 represent the data transmitter position of the BLI and are nearly identical with signal names differing by a "1" or a "2". The only other difference is that drawing 23 contains the 555 IC in the upper middle which generates a 9-15 Khz clock required for internal loop test (described later).

The leftmost position of the board contains the RS232 drivers and receivers which convert between the ± 15 Volt EIA levels from the modem and TTL logic levels. Signals off the board exit via two connectors mounted in positions J3 and J4. The long narrow rectangular block at the left indicates which printed circuit J1/J2 pins happen to be touched by the signals. The transmit data ENDA1- is gated on by the clear to send signal ST110+.

The BLI can be put into an internally looped mode in which transmitted data is connected to received data and the 12 Khz clock provides the transmit and receive clock. The 74157 in the center of the drawing multiplexes signals required by either of these two modes under control of the bit TEST1+ in the 74175 which signals loop test (CR9). This register is loaded during a write CR command by WCRL1+, and contains CR bits 7, 8, 9, and 10.

Located in the center of the drawing is the COM2601 USRT which is the heart of the BLI. These LSI chips (one for each half of BLI) control the transmission, reception, conversion from serial/parallel, status, and synchronization of the data from the outside world (see Appendix B for technical description). Also involved in data transmission are the FIFO and the control logic at the right hand side of the board. The FIFO is comprised of three 3341 ICs (Appendix B) in parallel which handle the eight bits of outgoing data, and two bits which indicate whether data is to be sent out in serial form or will become the new xmit or receive (or both) syn character. The FIFO is 64 characters long.

The transmit sequence is initiated by a 450 ns WDAT1+ pulse shown at the right of the drawing. This signal causes the 10 bits of data (8 bits of character plus DW8 and 9) to be loaded into the FIFO. At this point ST115+ goes false while there is a character in the queue and is available to the programmer as ST15. This bit is derived from Input Ready (IR) bits of each individual 3341. The data character falls through the FIFO under control of logic within the 3341 and reaches the end at which

time Output Ready (OR) is asserted for each 3341, resulting in OT1AV+ becoming true. When this signal is true and the USRT is ready to accept new data by asserting TBMT1+, the 400+ ns one shot at the top right of the drawing is set off, producing T1STR+. This strobe clocks the data out of the FIFO, causing OT1AV+ to go false indicating no output ready, and either TSS1+ and/or RSS1+, or TDS1+ to be pulsed. If either TB108+ or TB109+ is true, the data character will be loaded into either the transmit or receive internal USRT register. Both bits may be true simultaneously to load both registers together. Otherwise TDS1+ is pulsed to load the character into the USRT output register. This output data is serialized and sent out on TSO1+ to the multiplexer described earlier. When the character is removed from the FIFO, ST115+ goes true to indicate that the FIFO is again empty.

The USRT has a feature of being able to automatically send out a SYN character if it does not receive a data character in time. At this time SCS1+ becomes true for the duration of the SYN character and sets the 7474 in the bottom middle of the drawing. This status bit may be independently reset by CR3=1, and is reported as underrun error in ST14. The transmit FIFO may be independently reset by setting CR2=1 which generates F1RES-.

BLI25

This drawing depicts the Modem #1 and #2 receiver logic and contains two identical halves, differing only by logic signal names with either a "1" or a "2". The following description of the left half of the drawing can be applied equally to the right half.

The receiver logic contains a 32 character bit serial input FIFO (see Appendix B) coupled to the receive side of a USRT and control logic which provides timing and gating. Bit serial data enters at RCDA1+ at the upper left directly into the FIFO. The receive clock enters at RCLK1+ and is inverted to match the peculiarities of the FIFO which likes to see a rising clock when data is stable. The FIFO produces an input ready signal IRDY1- when it has room for another bit. If it is full because the user program has not emptied it through the USRT, the overrun error flip flop is set by clocking the complement of input ready IRDY1- into D6 producing RD108+ as a status bit available in DR8. This is so because IRDY1- =1 when the FIFO is full.

As the data bits trickle down the FIFO and reach the other end, OR1+ becomes true indicating output ready. If the USRT is ready to receive another byte, RDA1+ will be false. If DLCK1+ is true then all three signals combine in E6 to produce CKFU1- which sets off the one-shot producing SFT1+. SFT1+ clocks the bit out

of the FIFO and SFT1- clocks it into the USRT. When SFT1+ times out, it sets off the second one-shot in the timing loop producing DLCK1+ whose job it is to inhibit any further bit transfers for 3.6 microseconds. This is required for two reasons: first to maintain a good duty cycle on SFT1+, and second to keep the input clock frequency to the USRT below 250 Khz as required by its spec.

The USRT keeps RDA1+ low for eight bit times, and continues to accumulate bits until it receives a byte at which time it asserts RDA1+. This bit is available to the programmer as DR15, input data available. When data is read out of the USRT, RDAR1+ is strobed which resets the RDA1+, while DRSTR+ strobes the data into the buffer register as described in BLI22. When RDA1+ falls, the sequence of clocking bits from FIFO to USRT begins again.

Remaining on the drawing is the reset logic. At the bottom left of the drawing is the receiver reset one-shot which is pulsed by a signal WCRL1+ and CR0=1. This signal sets off RESR1+ for 1.2 microseconds which resets the receiver USRT. This action puts the receiver in SYN search mode in which it scans the incoming data stream for a bit pattern matching its internally stored SYN character (see BLI 23). During this process RDA1+ is low and bits are continuously clocked out of the FIFO and into the USRT. When a match is detected by the USRT it goes into byte mode, raising RDA1+.

Also available to the programmer is a bit in CR1 which allows resetting the receiver, receiver FIFO, and overrun error flop simultaneously. This pulse is initiated by WCRL1+ when CR1=1 and generates QRES1- which is coupled into the receiver reset logic by IC E6.

Further information is available to the programmer in the form of a receiver FIFO empty bit derived from Output Ready OR1+ generated by the receiver FIFO. Simply, when Output is not ready, the FIFO is empty. This bit is available in DR10. The OR1+ signal goes false after SFT1+ goes true, and therefore is a marginally useful indication of FIFO empty as the FIFO is empty for only one bit time at most which could be as little as 1 millisecond.

At the top left of the drawing is a gate at D7 which presents the RDAR1+ strobe from occurring unless data is actually available. This is necessary because the program may be hanging in a loop repeatedly reading DR looking at DR15.

FIRST UNIT	XXXØ	2	4	6	
SECOND UNIT	8	A	C	E	
BIT	DEVICE TYPE (DT)	STATUS (ST)	CONTROL (CR)	DATA READ (DR)	DATA WRITE (DW)
15	Ø	TRANS BUFFER EMPTY		INPUT DATA READY	
14	Ø	UNDERRUN ERROR		SYN RECEIVED	
13	Ø				
12	Ø				
11	1	1	1	1	
10	Ø	CLEAR TO SEND	REQ TO SEND	RCVR FIFO EMPTY	
9	Ø	CARRIER DETECT	LOOP TEST	RCVR PARITY ERROR	STORE TRANS SYN
8	Ø	DATA SET READY	DATA TERMINAL READY	RCVR OVERRUN ERROR	STORE RCVR SYN
7	BAUD RATE CODE		7 BIT-PLUS-PARITY MODE		
6	BAUD RATE CODE				
5					
4					
3			UNDERRUN ERROR RESET*		
2			TRANS FIFO RESET*		
1			RCVR FIFO, RCVR, OVERRUN RESET		
Ø			RECEIVER RESET*		

8 BIT DEVICE TYPE

INPUT DATA BYTE

OUTPUT DATA BYTE

*CRØ, CR1, CR2, CR3 WILL ALWAYS BE Ø WHEN READ

Appendix B. General Notes About Logic Drawings

1. Logic names tend to be given in their TRUE state for positive logic, e.g., when a write cycle is taking place, RITE+ will be high and RITE- will be low.

2. VOLTS- is ground (logic-low), named this way for the convenience of the program that generates the paper tape for the automatic wirewrap machine.

3. VOLTS+ similarly is logic-high, actually a 1K resistor to Vcc, driving up to 20 loads. Since several are required, VOLT1+, VOLT3+, etc., are used, designating on which drawing most of the loads are found.

4. Signals that leave a drawing show the destination drawings as [20,22], etc. On those drawings, for example, the drawing containing the logic source is designated (21).

5. INFIBUS signals usually have names ending in B, such as RITEB-.

6. The INFIBUS connector is designated P1 on the side that Lockheed calls P1A, and P2 on Lockheed's side P1B. The "outside" edge connector is designated J1 and J2 (1 through 55) for LEC's J1A and J1B respectively.

BLI

SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: 510-227-8898

A Standard Microsystems Company

COM2601

Universal Synchronous Receiver/Transmitter

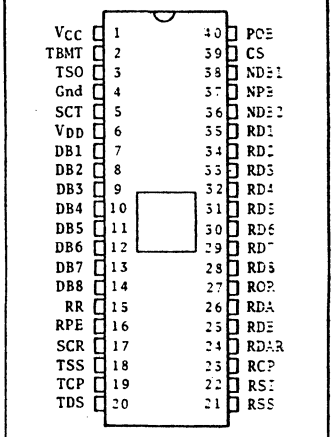
FEATURES

- **STR, BSC**—Bi-sync and interleaved bi-sync modes of operation
- **Fully Programmable**—data word length, parity mode, receiver sync character, transmitter sync character
- **Full or Half Duplex Operation**—can receive and transmit simultaneously at different baud rates
- **Fully Double Buffered**—eliminates need for precise external timing
- **Directly TTL Compatible**—no interface components required
- **Tri-State Data Outputs**—bus structure oriented
- **IBM Compatible**—internally generated SCR and SCT signals
- **High Speed Operation**—250K baud, 200ns strobes
- **Low Power**—300mW
- **Input Protected**—eliminates handling problems
- **Hermetic Dip Package**—easy board insertion

GENERAL DESCRIPTION

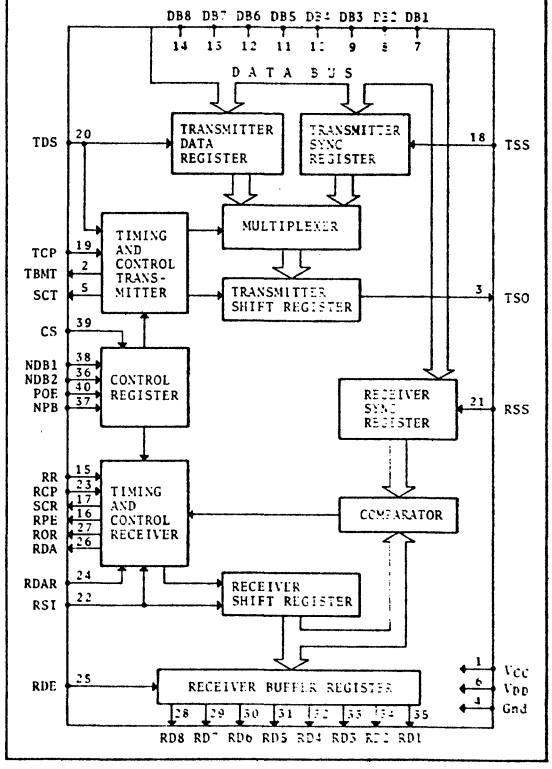
The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

Pin Configuration



PACKAGE: 40-Pin D.I.P.

Functional Block Diagram



BLI

Appendix C. COM2601 USRT Specification

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	-25 V

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0-+70°C, V_{CC}=+5V±5%, V_{DD}=-12V±5%, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} =-100µA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	µA	RDE=V_{IL}, 0≤V_{OUT}≤+5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	R_{DE} = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			20	mA	All outputs = V_{OH}
I_{DD}			15	mA	
A.C. CHARACTERISTICS					T_A =+25°C
CLOCK FREQUENCY	DC		250	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			µs	RCP, TCP
Receiver reset	1			µs	RR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	TDS
Transmitter sync strobe	200			ns	TSS
Receiver sync strobe	200			ns	RSS
Receiver data available reset	200			ns	RDAR
INPUT SET-UP TIME					
Data bits	0			ns	DB1-DB8
Control bits	0			ns	NPB,NDB2,NDB1,POE
INPUT HOLD TIME					
Data bits	0			ns	DB1-DB8
Control bits	0			ns	NPB,NDB2,NDB1,POE
STROBE TO OUTPUT DELAY					Load =20pf+1TTL input
Receive data enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

** Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low impedance to V_{CC}
   2) low impedance to GND
   3) high impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Symbol	Name	Function
1	V_{CC}	Power Supply	+5 volt Supply
2	TBMT	Transmitter Buffer Empty	This output is at a high-level when the transmitter data buffer register may be loaded with new data.
3	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register.
4	GND	Ground	Ground
5	SCT	Sync Character Transmitted	This output is set high when the character loaded into the transmitted shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed.
6	V_{DD}	Power Supply	-12 volt Supply
7-14	DB1-DB8	Data Bus Inputs	This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs should be at a high level. The LSB should always be placed on DB1.
15	RR	Receiver Reset	This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transition of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded int the receiver buffer register.
16	RPE	Receiver Parity Error	This output is a high-level if the received character parity bit does not agree with the selected parity.

Description of Pin Functions (cont.)

Pin No.	Symbol	Name	Function
17	SCR	Sync Character Received	This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character.
18	TSS	Transmitter Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register.
19	TCP	Transmitter Clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency.
20	TDS	Transmitter Data Buffer Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register.
21	RSS	Receiver Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register.
22	RSI	Receiver Serial Input	This input accepts the serial bit input stream.
23	RCP	Receiver Clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency.
24	RDAR	Receiver Data Available Reset	A high-level input resets the RDA output to a low-level.
25	RDE	Received Data Enable	A high-level input enables the outputs (RD8-RD1) of the receiver buffer register
26	RDA	Receiver Data Available	This output is at a high-level when an entire character has been received and transferred into the receiver buffer register.
27	ROR	Receiver Over-Run	This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register.
28-35	RD8-RD1	Receiver Data Output	These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
36, 38	NDB2, NDB1	Number of Data	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table:

NDB2	NDB1	data bits/character
L	L	5
L	H	6
H	L	7
H	H	8

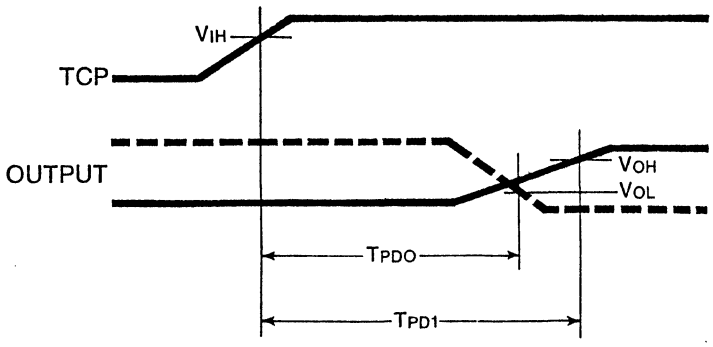
Description of Pin Functions (cont.)

Pin No.	Symbol	Name	Function
37	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE.
39	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level.
40	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity
		X=don't care

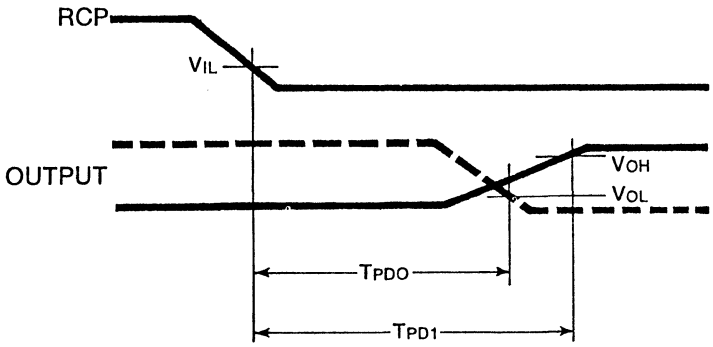
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

Transmitter



OUTPUT	TPDO	TPD1	UNITS
TBMT	NA	2.0	μs
SCT	1.0	1.5	μs
TSO	1.0	1.0	μs

Receiver



OUTPUT	TPDO	TPD1	UNITS
RDA	NA	1.0	μs
ROR	2.0	2.5	μs
RPE	2.0	2.5	μs
SCR	2.0	2.5	μs
RD1-RD8	2.5	2.5	μs

BLI

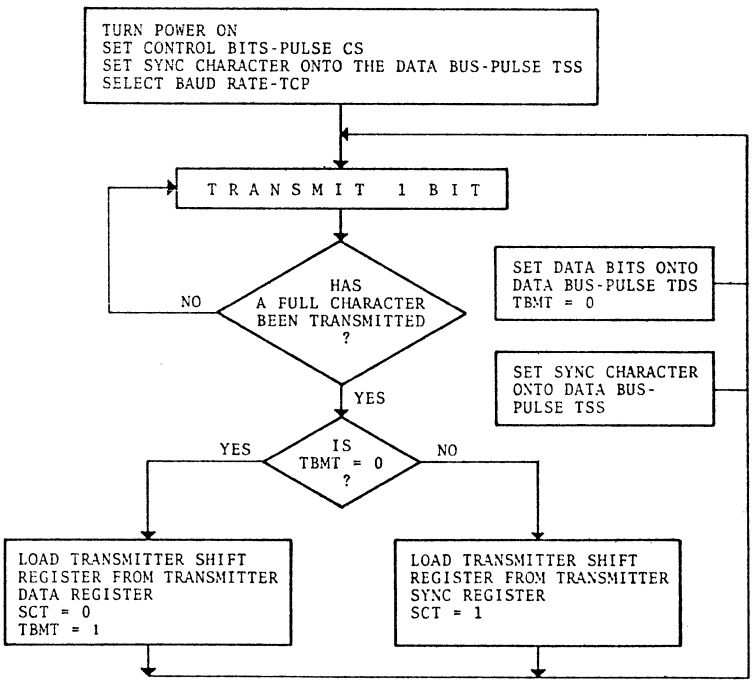
DESCRIPTION OF OPERATION - RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

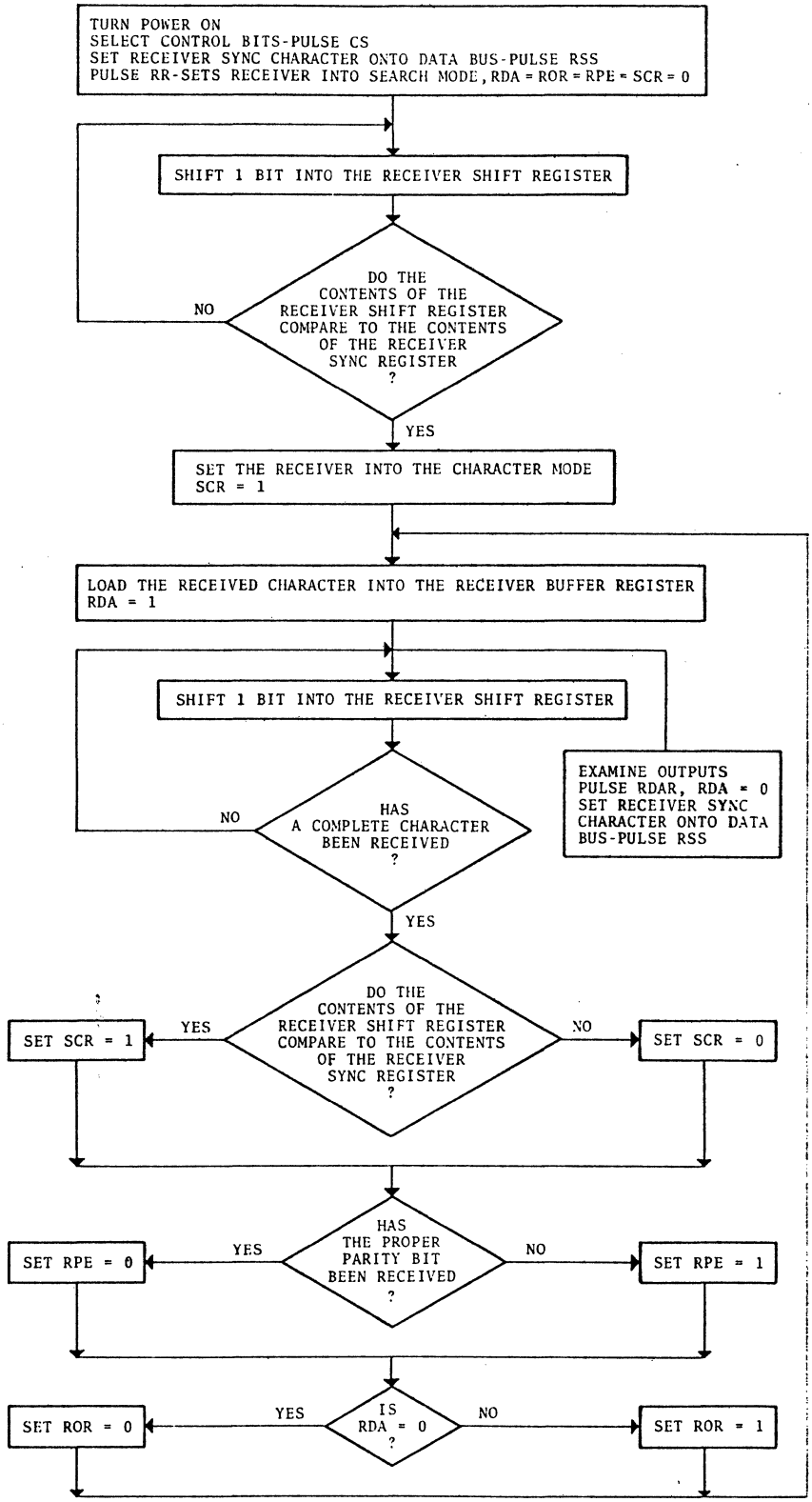
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data outputs levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

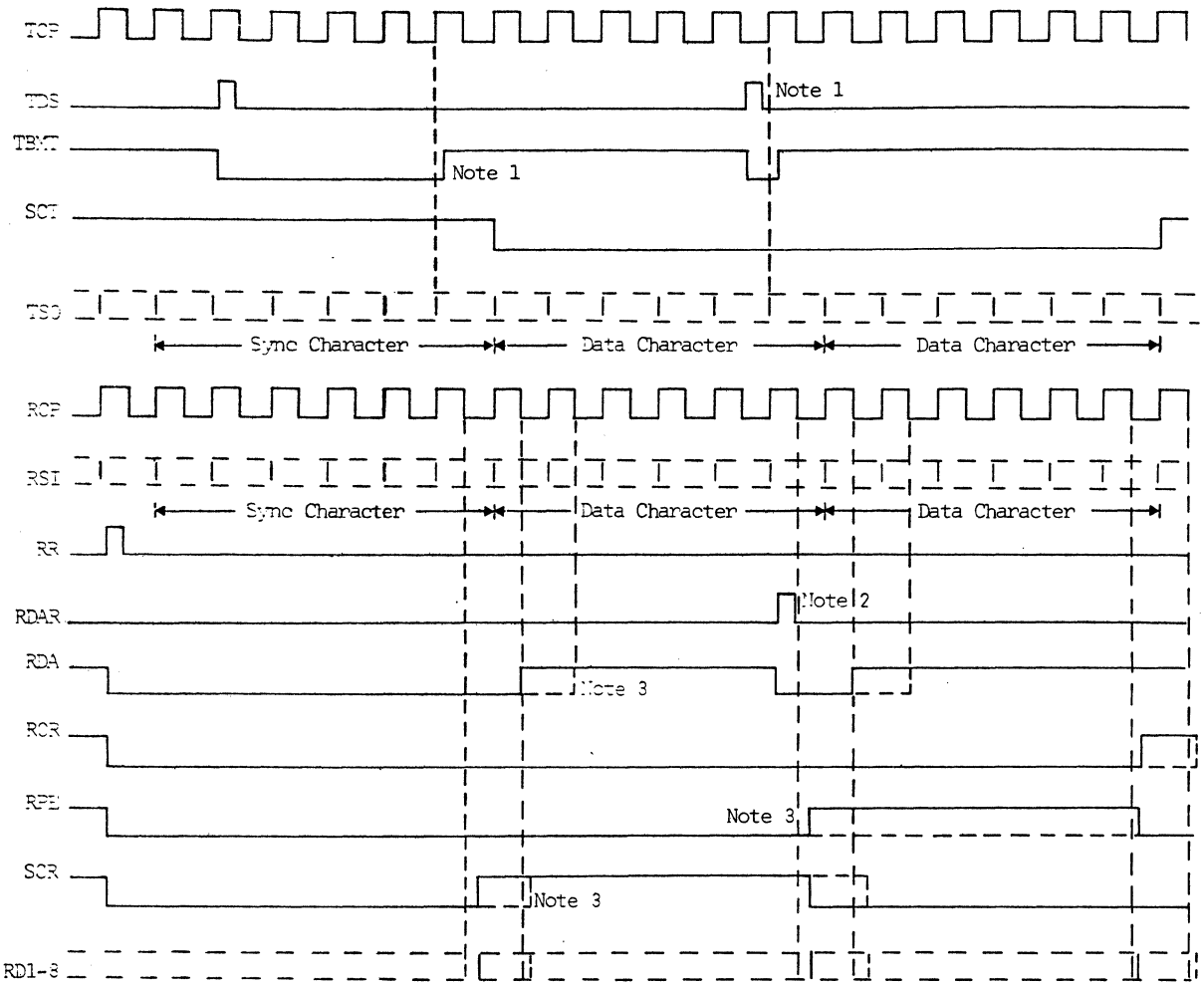
FLOW CHART - TRANSMITTER



FLOW CHART - RECEIVER



USRT TIMING DIAGRAM



NOTE 1
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

NOTE 3
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.

Am2812 / Am2812A • Am2813 / Am2813A

32 x 8-Bit and 32 x 9-Bit First-in First-out Memories

Advanced Micro Devices
Complex MOS Integrated Circuits

Distinctive Characteristics

- Completely independent read and write operations
- "Half-full" flag
- Am2812 has serial or parallel input and output
- Data rates up to 1 MHz

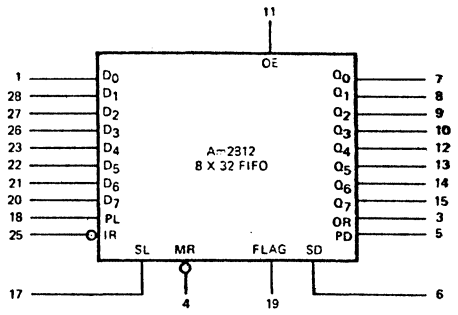
FUNCTIONAL DESCRIPTION

The Am2812 and Am2813 are 32 word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three-state outputs controlled by an output enable pin (OE). Data on the data inputs (D_i) are written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word. Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs (Q_i) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready (IR) signal indicates that the device is ready to accept data and also provides a memory full signal. Both the Am2812 and Am2813 have master reset inputs which clear all data from the device (reset to all LOWs), and a FLAG signal which goes HIGH when the memory contains more than 15 words.

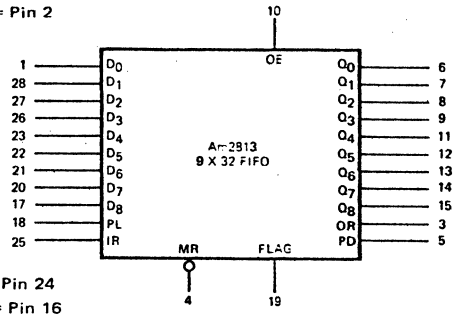
The Am2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is in reality an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the D_0 input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built-in parallel-to-serial converter, so that data can be shifted out of the Q_7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals, PL, IR, PD, and OR, are designed so that two FIFOs can be placed end to end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

LOGIC SYMBOLS



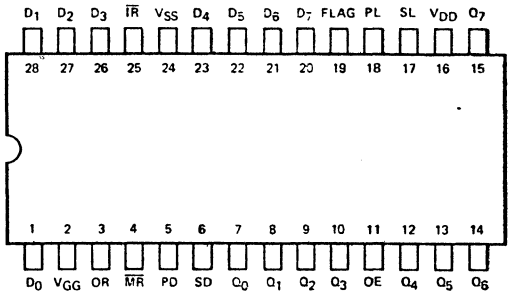
V_{SS} = Pin 24
V_{DD} = Pin 16
V_{GG} = Pin 2



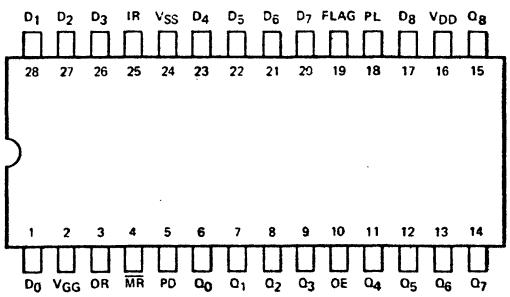
V_{SS} = Pin 24
V_{DD} = Pin 16
V_{GG} = Pin 2

CONNECTION DIAGRAMS
Top Views

Am2812



Am2813



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Frequency	Temperature Range	Am2812 Order Number	Am2813 Order Number
Hermetic DIP	500KHz	0°C to +70°C	AM2812DC	AM2813DC
Hermetic DIP	500KHz	−55°C to +125°C	AM2812DM	AM2813DM
Hermetic DIP	1MHz	0°C to +70°C	AM2812ADC	AM2813ADC
Hermetic DIP	1MHz	−55°C to +125°C	AM2812ADM	AM2813ADM

BLI

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −7V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −10V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am2812DC, Am2812ADC	0°C to +70°C	5.0V ±5%	0V	−12V ±5%
Am2813DC, Am2813ADC				
Am2812DM, Am2812ADM	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am2813DM, Am2813ADM				

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = .300mA		V_{SS} −1.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA				0.4	V
V_{IH}	Input HIGH Level			V_{SS} −1.0			V
V_{IL}	Input LOW Level					0.8	V
I_{IL}	Input Leakage Current	V_{IN} = 0V				1.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS} −1.0V		250			µA
V_{PUP}	Input Pull-up Initiation Voltage	(Note 2)	V_{SS} = MIN.			2.0	V
			V_{SS} = MAX.			2.2	V
V_{BAR}	Voltage at Peak Input Current	(Note 2)				V_{SS} −1.5	V
I_{BAR}	Maximum Input Current	(Note 2)				1.6	mA
I_{GG}	V_{GG} Current	T_A = 0°C to +70°C			14	22	mA
		T_A = −55°C to +125°C				27	
I_{DD}	V_{DD} Current	T_A = 0°C to +70°C			30	45	mA
		T_A = −55°C to +125°C				55	

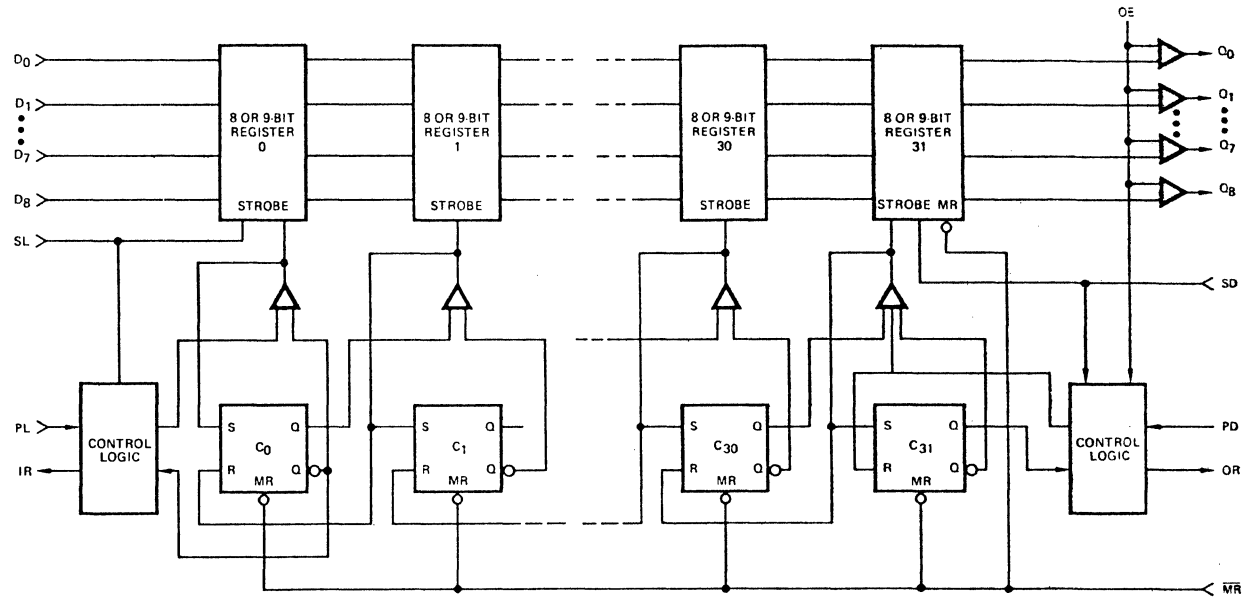
Notes: 1. Typical limits are at V_{SS} = 5.0V, V_{GG} = −12.0V, T_A = 25°C
2. Pull up circuit on Am2813 only. See graph of input V-I characteristics.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Conditions/Note	Test Conditions	Am2812 Am2813 Min.	Typ.	Max.	Am2812A Am2813A Min.	Typ.	Max.	Units
f_p	Maximum Parallel Load or Dump Frequency		0.5			1.0			MHz
t_{IR+}	Delay, PL or SL HIGH to IR In-Active		100	300	1100	80	300	450	ns
t_{IR-}	Delay, PL or SL LOW to IR Active		100	250	800	80	250	400	ns
$t_{pw}H(P)$	Minimum PL or PD HIGH Time				100			80	ns
$t_{pw}L(P)$	Minimum PL or PD LOW Time				100			80	ns
$t_{pw}H(S)$	Minimum SL or SD HIGH Time	Am2812 only			350			300	ns
$t_{pw}H(S)$	Minimum SL or SD LOW Time	Am2812 only			350			300	ns
$t_h(D)$	Data Hold Time			190	250		170	200	ns
$t_s(D)$	Data Set-Up Time	to PL			0			0	ns
		to SL			100			90	
t_{OR+}	Delay, PD or SD HIGH to OR LOW	OE HIGH	100	450	1100	100	350	520	ns
t_{OR-}	Delay, PD or SD LOW to OR HIGH	OE HIGH	100	400	850	100	300	470	ns
t_{PT}	Ripple through Time	FIFO Empty			10			8	µs
t_{DH}	Delay, OR LOW to Data Out Changing	PD = LOW	50	200		50	200		ns
t_{DA}	Delay, Data Out to OR HIGH	PD = HIGH	0	100		0	100		ns
t_{MRW}	Minimum Reset Pulse Width				400			400	ns
t_{DO}	Delay, OE LOW to Output OFF				400			400	ns
t_{EO}	Delay, OE HIGH to Output Active				400			400	ns
t_{DF}	Delay from PL or SL HIGH to Flag HIGH or PD or SD HIGH to Flag LOW			0.5	1.0		0.5	1.0	µs
CI	Input Capacitance				7			7	pF

Notes: 3. IR is active HIGH on Am2813 and active LOW on Am2812.
4. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

LOGIC BLOCK DIAGRAM



DESCRIPTION OF THE Am2812 and Am2813 FIFO OPERATION

The Am2812 and Am2813 FIFOs consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit and clearing the n^{th} control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a LOW-to-HIGH transition on the parallel load (PL) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When PL next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go active, indicating the inputs are available for another data word.

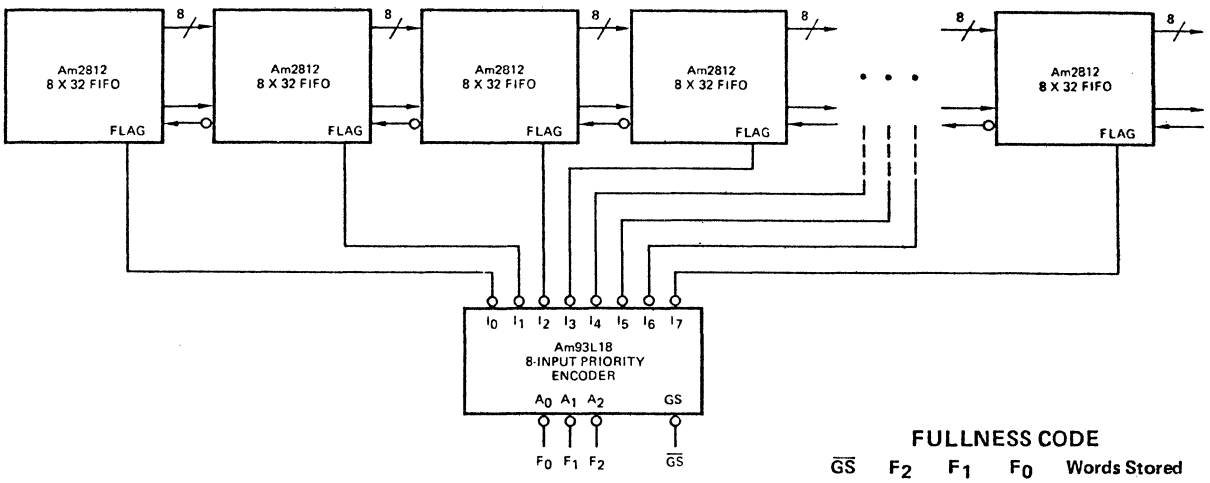
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A LOW-to-HIGH transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes HIGH, OR will go LOW as before, but when PD next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes LOW, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

Because the input ready signal is active LOW on the Am2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two Am2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n Am2812s connected end-to-end store 31n+1 words (instead of 32n). The Am2813 stores 32n words in this configuration, because IR is active HIGH and does dump the last word written into the second device.

APPLICATIONS



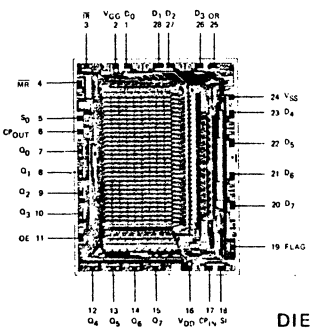
FULLNESS CODE

$\overline{GS}$	F_2	F_1	F_0	Words Stored
L	L	L	L	0 - 15
L	L	L	H	13 - 47
L	L	H	L	45 - 78
L	L	H	H	76 - 109
L	H	L	L	107 - 140
L	H	L	H	138 - 171
L	H	H	L	169 - 202
L	H	H	H	200 - 233
H	H	H	H	231 - 249

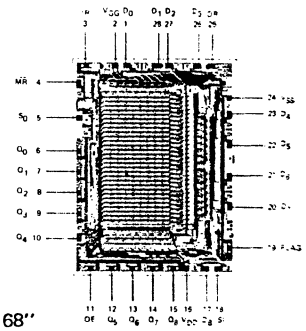
The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code F_0-F_2 indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH.

Metallization and Pad Layouts

Am2812



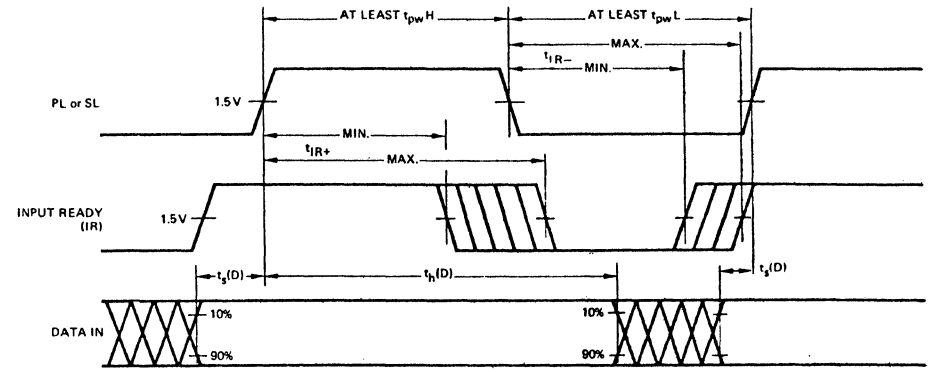
Am2813



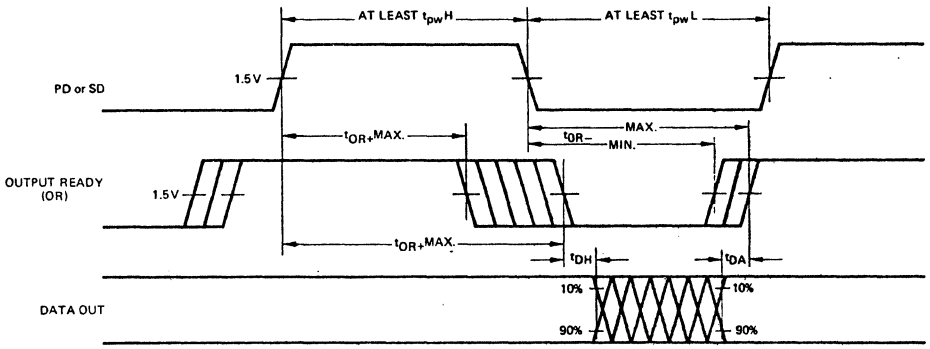
DIE SIZE .128" X 0.168"

ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

TIMING DIAGRAM



Note: IR inverted on Am2812.



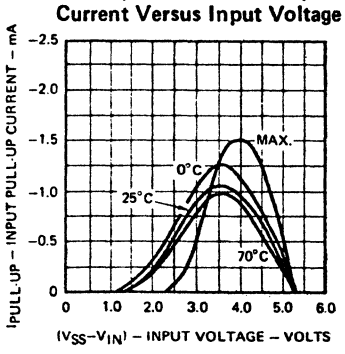
USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If PD is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{OR+}) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. $\overline{IR}$ goes HIGH and OR goes LOW. If PL is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and $\overline{IR}$ will return to the LOW state until PL is brought LOW. If PL is LOW when the master reset is ended, then $\overline{IR}$ will go HIGH but the data on the inputs will not enter the memory until PL goes HIGH.
5. The output enable pin inhibits dump commands while it is LOW and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

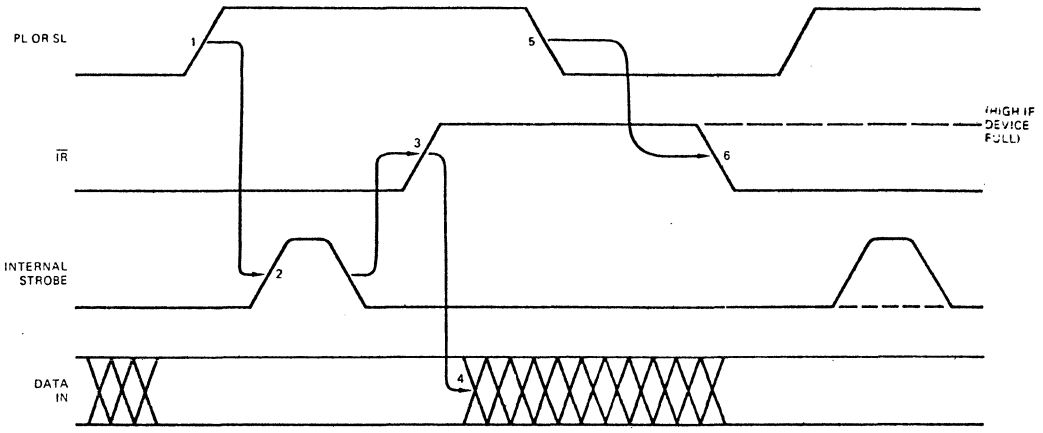
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN

Pull-up Characteristic Input Current Versus Input Voltage

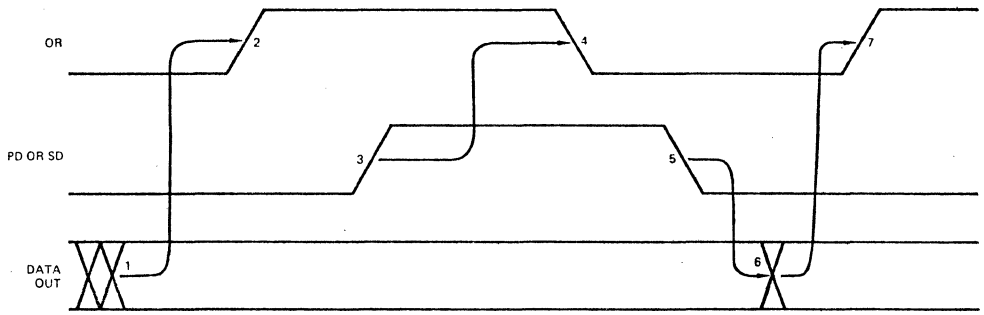


Am2812 TIMING DIAGRAM



Am2812 INPUT TIMING

When data is steady PL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.



Am2812 OUTPUT TIMING

When data out is steady (1), OR goes HIGH (2). When PD goes HIGH (3), OR goes LOW (4). When PD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

The input and output timing diagrams above illustrate the sequence of control on the Am2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The Am2813 pattern is similiar, but IR is active HIGH instead of active LOW (shown in timing diagram on next page).

FLAG OUTPUT

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 13th, 14th, 15th, or 16th word is loaded into the FIFO. It will remain HIGH until there are less than $15^{+1}/_{-2}$ words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

RESET

An over-riding master reset ($\overline{MR}$) is used to clear all control register bits and set all the outputs LOW.

SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to D_0 input. Inputs D_1–D_7 must be grounded. The SL signal operates just like the PL input, causing IR to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the O_7 output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output. OR will stay LOW if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.

FAIRCHILD MOS INTEGRATED CIRCUIT 3341

GENERAL DESCRIPTION — The 3341 is a 64-word x 4-bit memory that operates in a first-in first-out (FIFO) mode. Inputs and the output are completely independent (no common clocks) making the 3341 ideal for asynchronous buffer applications.

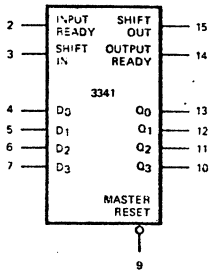
Special on chip input pull up circuits and bipolar compatible output buffers provide direct bipolar interfacing with no external components required. Control signals are provided so that both vertical and horizontal cascading may be easily achieved.

- 1 MHz SHIFT-IN SHIFT-OUT RATE
- DIRECT TTL/DTL INTERFACE AT INPUTS & OUTPUTS
- 16-LEAD DUAL IN-LINE PACKAGE
- READILY EXPANDABLE IN EITHER DIRECTION
- ASYNCHRONOUS OR SYNCHRONOUS OPERATION
- CONVENIENT LEAD ORIENTATION FOR EASY BREADBOARDING
- UNIQUE TTL INPUT STAGE

ABSOLUTE MAXIMUM RATINGS

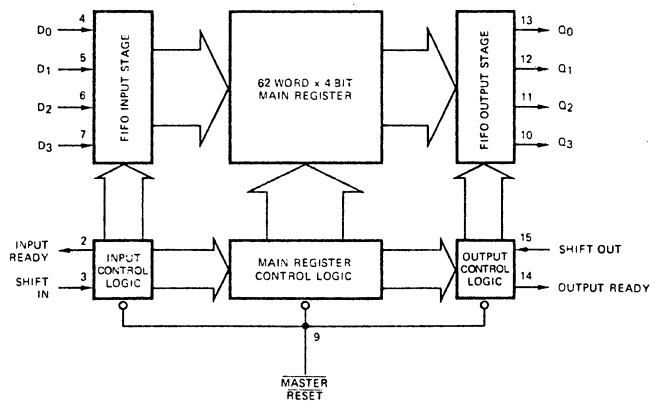
Storage Temp (T_S)	−65°C to +150°C
Operating Temp (T_A)	0° to +70°C
Voltage on all pins except outputs + V_{DD}	V_{SS} −24V to V_{SS} +0.3V
Voltage on V_{DD}	V_{SS} −7V to V_{SS} +0.3V

LOGIC SYMBOL

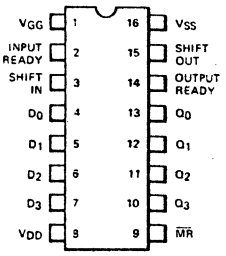


V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC BLOCK DIAGRAM



CONNECTION DIAGRAM (TOP VIEW)



BLI

FUNCTIONAL DESCRIPTION:

DATA INPUT:

The four bits of data on the D_0 . . . D_3 inputs are entered into the first bit location when both Input Ready (IR) and Shift In (SI) are HIGH ($\approx V_{SS}$). This causes IR to go LOW ($\approx$GND), but data will stay locked in the first bit location until both IR and SI are brought LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

DATA TRANSFER:

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel, from input to the output of a previously empty device.

DATA OUTPUT:

When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins O_0 . . . O_3. The transfer of data is initiated when both the Output Ready (OR) output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

SPECIAL INPUT CHARACTERISTICS:

The 3341 uses a TTL compatible input pull up circuit. When going HIGH, the TTL driver must only provide 2.2V minimum which is then internally pulled up to V_{SS}.

When going LOW, the TTL driver must overcome a current barrier of $\leq$1.6mA at 2V. Once this is overcome, the input current drops to zero.

Unused inputs are stable in the HIGH state, but must be terminated when LOW, e.g., 1MΩ to V_{GG}.

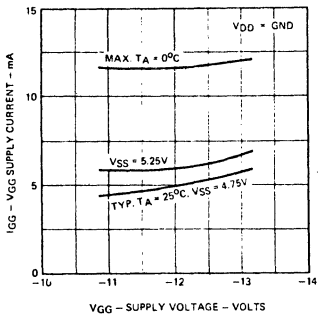
DC CHARACTERISTICS: V_{SS} = +5V $\pm$5%, V_{GG} = −12V $\pm$5%, V_{DD} = 0V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}−1.0			V	Notes 1 and 2
V_{IL}	Input Voltage LOW			0.8	V	Note 1
V_{OH}	Output Voltage HIGH	V_{SS}−1.0			V	I_{OH} = 0.3mA
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6mA
V_{PUP}	Input Pull Up Initiation Voltage			2.0	V	V_{SS} = 4.75V
V_{PUP}	Input Pull Up Initiation Voltage			2.2	V	V_{SS} = 5.25V
V_{BAR}	Peak Input Barrier Current Voltage Point			V_{SS}−1.5	V	
I_{IH}	Input Current HIGH	250			μA	Note 1, V_{IH} = V_{SS}−1.0V
I_{LI}	Input Leakage Current			1.0	μA	Note 1, V_{IN} = 0V
I_{BAR}	Input Barrier Current			1.6	mA	Note 1
I_{GG}	V_{GG} Current		7.0	12	mA	
I_{DD}	V_{DD} Current		30	45	mA	
P_D	Power Dissipation			450	mW	

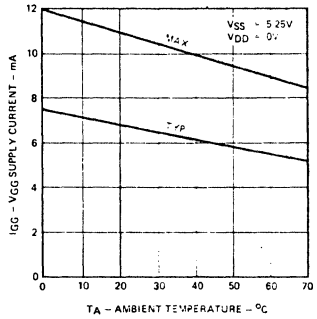
NOTES:
1. Inputs include D_0 – D_3, $\overline{\text{Master Reset}}$, Shift In, and Shift Out.
2. Internal pull up circuits are provided on all inputs to insure proper HIGH level.

ELECTRICAL CHARACTERISTICS

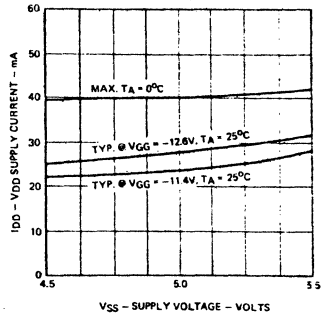
V_{GG} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



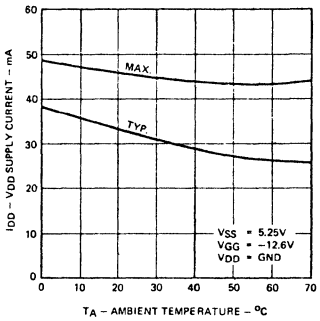
V_{GG} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



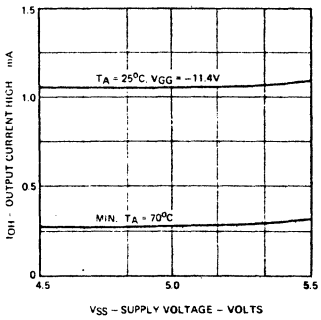
V_{DD} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



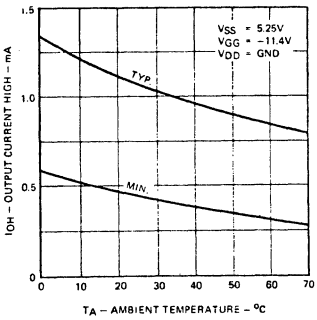
V_{DD} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



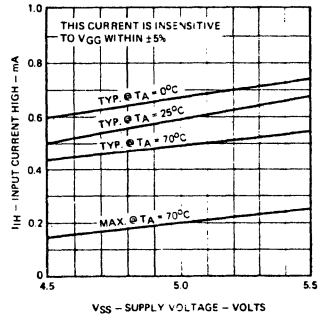
OUTPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE



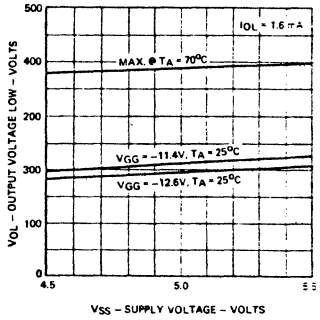
OUTPUT CURRENT HIGH VERSUS AMBIENT TEMPERATURE



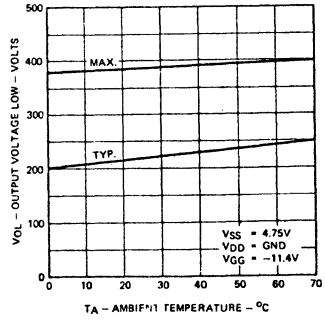
INPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE



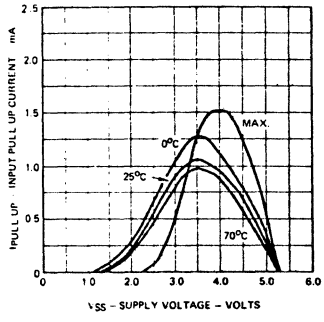
OUTPUT VOLTAGE LOW VERSUS SUPPLY CURRENT



OUTPUT VOLTAGE LOW VERSUS AMBIENT TEMPERATURE



INPUT PULL UP CURRENT VERSUS V_{SS} POWER SUPPLY CURRENT



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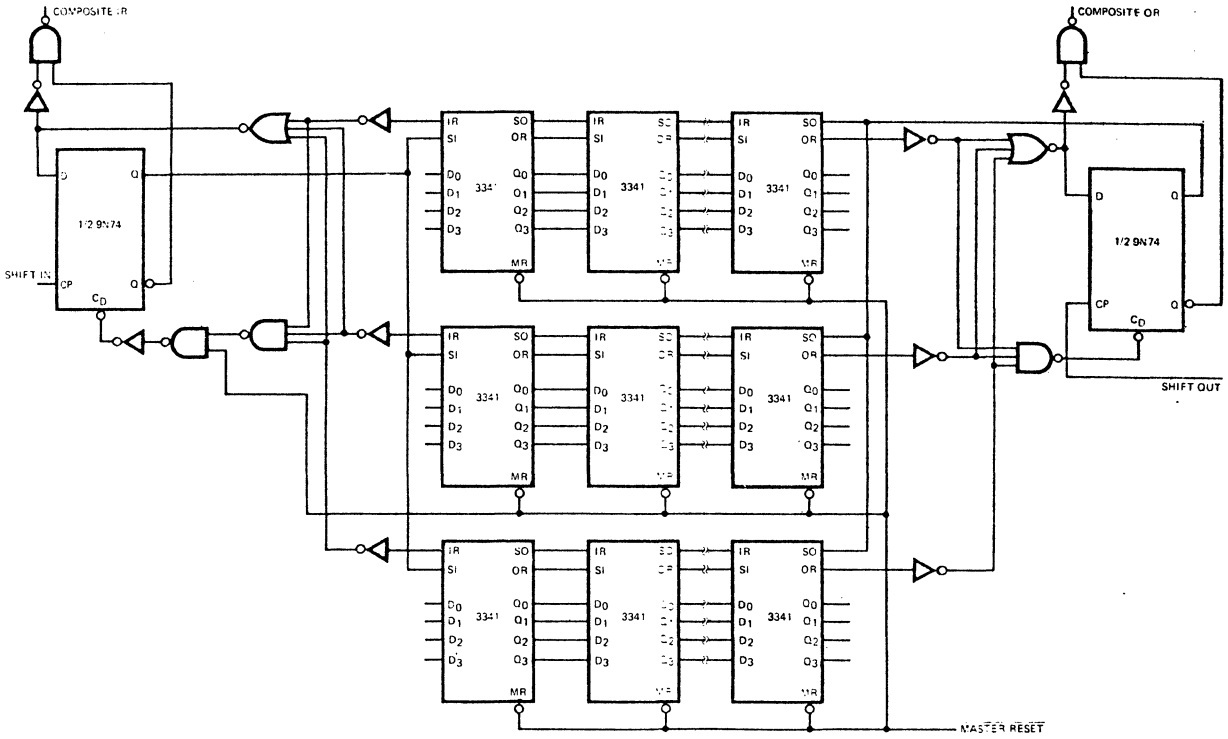
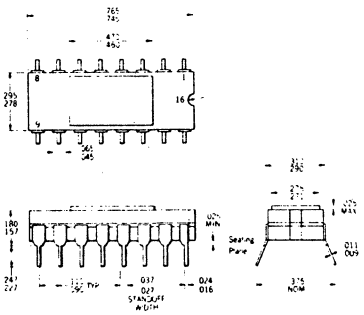
EXPANSION OF 3341 TO N-WORD BY 12-BIT FIFO



NOTE: Composite Shift In should be LOW when Master Reset goes HIGH. Input data may be changed after Composite IR goes LOW. Composite IR will not go HIGH until Composite Shift In goes LOW. When Composite IR goes HIGH FIFO's will accept new data. 3341's will operate at their highest natural speeds if these rules are followed.

PACKAGE INFORMATION

7K – 16-LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar
Lead No. 8 is internally grounded

AC CHARACTERISTICS: V_{SS} = +5V ±5%, V_{DD} = 0V, V_{GG} = 12V ±5%, T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC	0°C			70°C			UNITS	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{IR+}	Input Ready HIGH Time	90	200		155	300	550	ns	Fig. 1, Note 6
t_{IR-}	Input Ready LOW Time	138	250			300	550	ns	Fig. 1, Note 6
t_{OV+}	Control Overlap HIGH Time	70			100			ns	Figs. 1 and 2, Note 3
t_{OV-}	Control Overlap LOW Time	70			100			ns	Figs. 1 and 2, Note 3
t_{DSI}	Data Input Stable Time	400			400			ns	Fig. 1
t_{DD}	Data Input Delay Time	25						ns	Fig. 1, Note 5
t_{OR+}	Output Ready HIGH Time	90	200		155	300	500	ns	Fig. 2, Note 5
t_{OR-}	Output Ready LOW Time	170	300			450	850	ns	Fig. 2, Note 5
t_{PT}	Data Through-Put Time		10			10	32	µs	Note 4
t_{DH}	Data Hold Time	75						ns	Fig. 2, Note 5
t_{MRW}	Master Reset Pulse Width				400			ns	
t_{DA}	Data Output Available Time	0	30					ns	Fig. 2
C_I	Input Cap. of Data and Control Lines			7.0			7.0	pF	
C_{MR}	Input Cap. of $\overline{MR}$			15			15	pF	

NOTES:
3. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.
4. This parameter defines total time from the time data is present at $D_0 - D_3$ to the time it is available at $O_0 - O_3$ with FIFO initially empty.
5. 1 TTL load +20 pF.

TIMING DIAGRAMS

INPUT TIMING

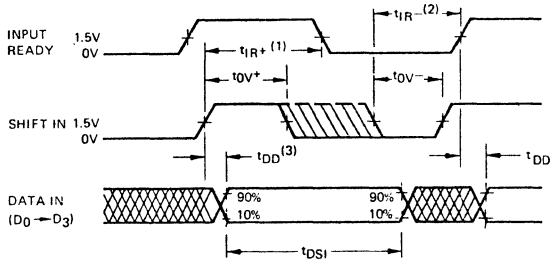


FIG. 1

Input data must remain stable during timing window t_{DSI}. Both SI and IR must be HIGH for t_{OV+}. Similarly, both SI and IR must be LOW for t_{OV-}.

NOTES:
1. t_{IR+} is referenced to the positive going edge of IR or SI, whichever occurs later.
2. t_{IR-} is referenced to the negative going edge of IR or SI, whichever occurs later.
3. t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.
4. t_{OV+} is referenced to the positive going edge of IR or SI, whichever occurs later.
5. t_{OV-} is referenced to the negative going edge of IR or SI, whichever occurs later.
6. Data must be stable for t_{SDI} or t_{IR+}, whichever is shorter.

OUTPUT TIMING

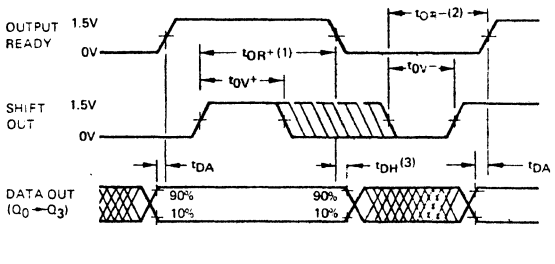


FIG. 2

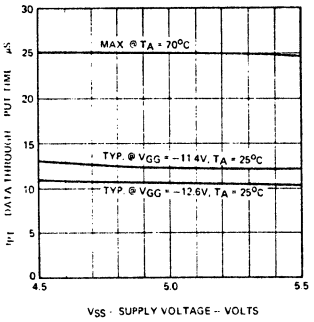
Both SO and OR must be HIGH for t_{OV+}. Similarly both SO and OR must be LOW for t_{OV-}. Data will remain stable for t_{DH} after both SO and OR are LOW.

NOTES:
1. t_{OR+} is referenced to the positive going edge of OR or SO, whichever occurs later.
2. t_{OR-} is referenced to the negative going edge of OR or SO, whichever occurs later.
3. t_{DH} is referenced to the negative going edge of OR or SO, whichever occurs later.
4. t_{OV+} is referenced to the positive going edge of IR or SI, whichever occurs later.
5. t_{OV-} is referenced to the negative going edge of IR or SI, whichever occurs later.

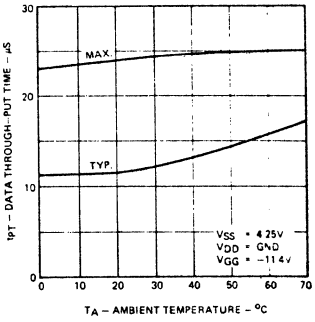
BLI

ELECTRICAL CHARACTERISTICS

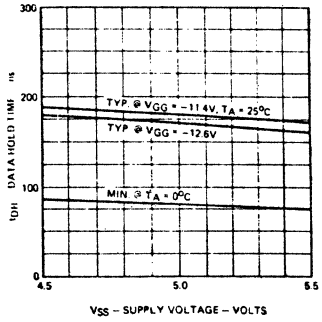
DATA THROUGH-PUT TIME VERSUS SUPPLY VOLTAGE



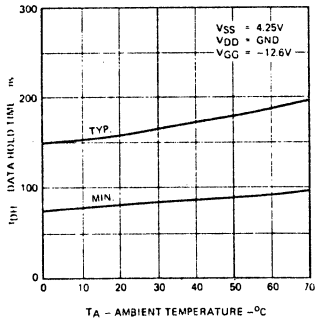
DATA THROUGH-PUT TIME VERSUS AMBIENT TEMPERATURE



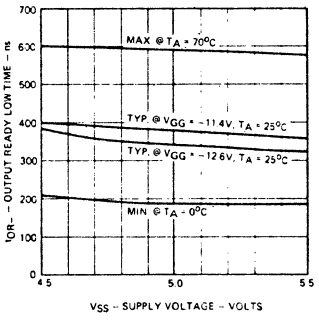
DATA HOLD TIME VERSUS SUPPLY VOLTAGE



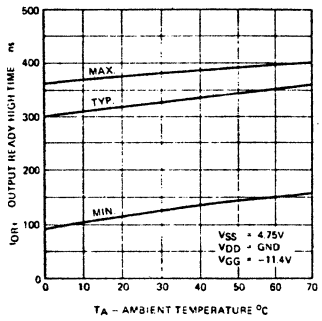
DATA HOLD TIME VERSUS AMBIENT TEMPERATURE



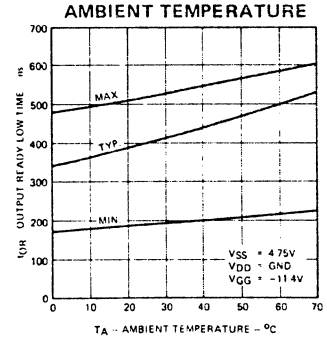
OUTPUT READY LOW TIME VERSUS SUPPLY VOLTAGE



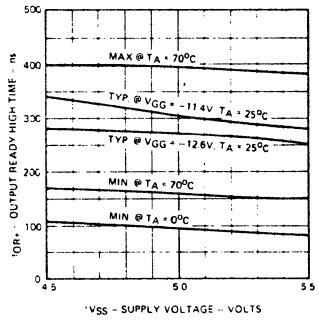
OUTPUT READY HIGH TIME VERSUS AMBIENT TEMPERATURE



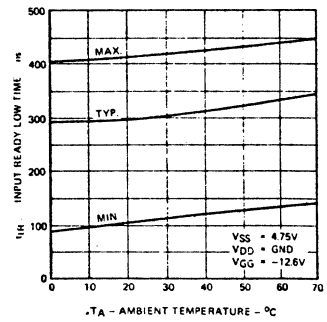
OUTPUT READY LOW TIME VERSUS AMBIENT TEMPERATURE



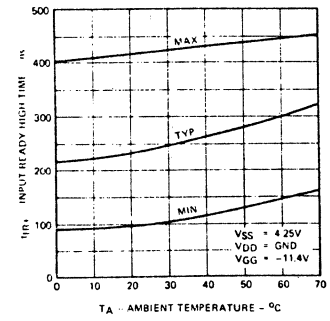
OUTPUT READY HIGH TIME VERSUS SUPPLY VOLTAGE



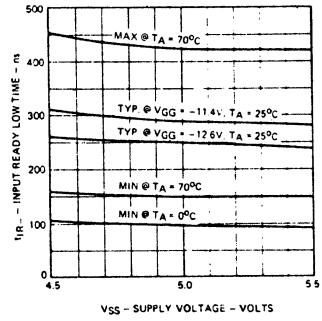
INPUT READY LOW TIME VERSUS AMBIENT TEMPERATURE



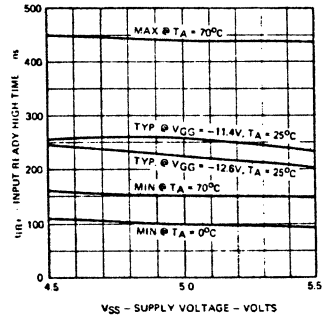
INPUT READY HIGH TIME VERSUS AMBIENT TEMPERATURE

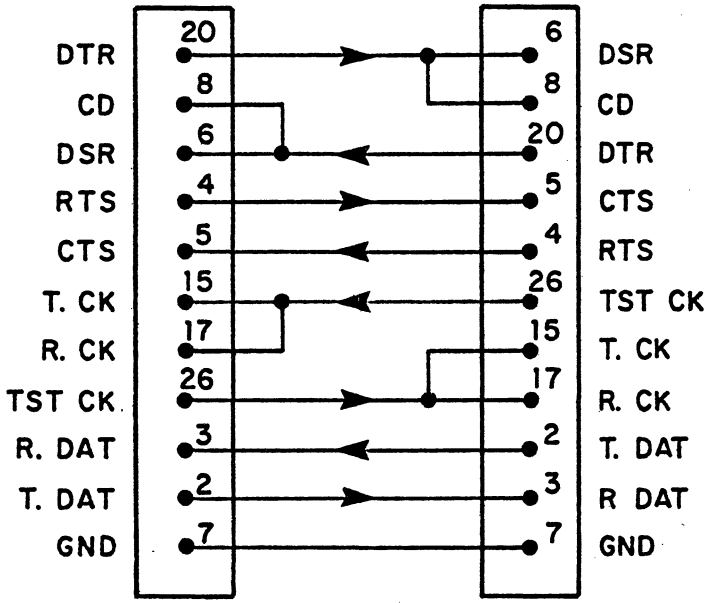


INPUT READY LOW TIME VERSUS SUPPLY VOLTAGE

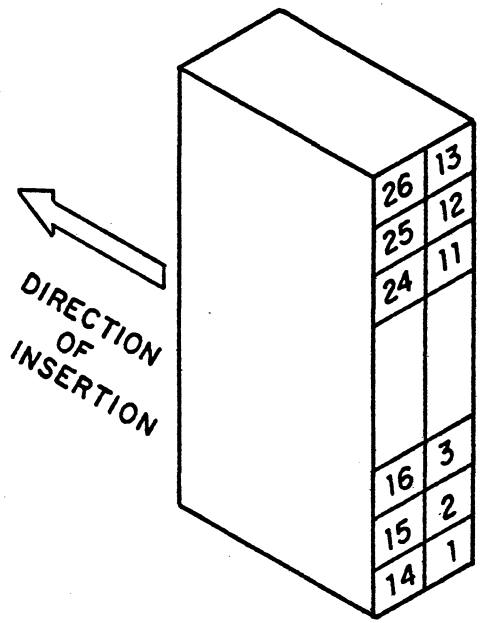


INPUT READY HIGH TIME VERSUS SUPPLY VOLTAGE



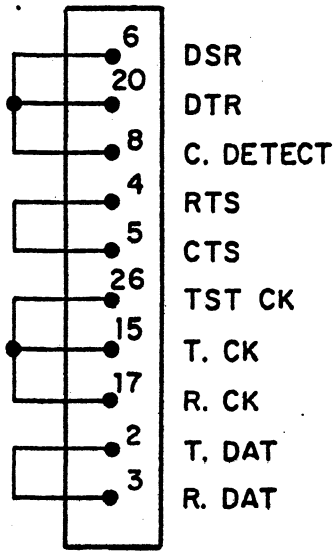


DOUBLE PLUG CONFIGURATION FOR TESTING TWO CARDS OR TWO HALVES OF SAME CARD AGAINST EACH OTHER



CONNECTOR PIN-NUMBERING

SINGLE PLUG CONFIGURATION



Appendix D. Looping Plug Configurations; BLI

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	8/30/77	

BLI

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN QRF

8/30/77

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

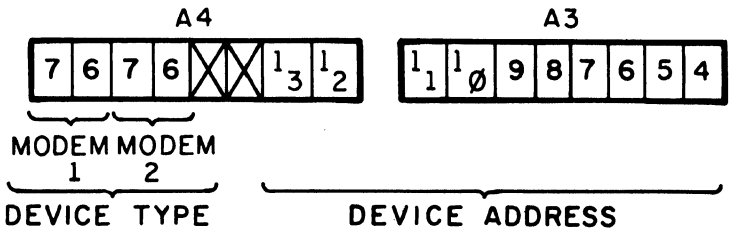
BLI TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		BLI-05

SCALE	REV	SHEET
	A	1 OF 3

BLI - BUFFERED SYNCHRONOUS LINE INTERFACE

SWITCHES



DEVICE TYPE: OFF = SWITCH OPEN POSITION = 1
DEVICE ADDRESS: ON = SWITCH CLOSED POSITION = 1
} NOTE THE DIFFERENCE

Bus (Address field)

1. For 20 bit Address Decoding (I-bus) Insert BDR in A2
2. For 16 bit Address Decoding (P-bus) Insert Jumper-Bug in A2, connecting pins 1,3,12,14 to +5 Volts through a 1K resistor to pin 16.

Connectors

Upper connector is for Modem #2 (D.T. Address XXX8)
Lower connector is for Modem #1 (D.T. Address XXXØ)

BLI

Jumpers

NONE

FIRST UNIT	XXXØ	2	4	6	
SECOND UNIT	8	A	C	E	
BIT	DEVICE TYPE (DT)	STATUS (ST)	CONTROL (CR)	DATA READ (DR)	DATA WRITE (DW)
15	Ø	TRANS BUFFER EMPTY		INPUT DATA READY	
14	Ø	UNDERRUN ERROR		SYN RECEIVED	
13	Ø				
12	Ø				
11	1	1	1	1	
10	Ø	CLEAR TO SEND	REQ TO SEND	RCVR FIFO EMPTY	
9	Ø	CARRIER DETECT	LOOP TEST	RCVR PARITY ERROR	STORE TRANS SYN
8	Ø	DATA SET READY	DATA TERMINAL READY	RCVR OVERRUN ERROR	STORE RCVR SYN
7	BAUD RATE CODE		7 BIT-PLUS-PARITY MODE		
6	BAUD RATE CODE				
5					
4					
3			UNDERRUN ERROR RESET*		
2			TRANS FIFO RESET*		
1			RCVR FIFO, RCVR, OVERRUN RESET		
Ø			RECEIVER RESET*		

8 BIT DEVICE TYPE

INPUT DATA BYTE

OUTPUT DATA BYTE

*CRØ, CR1, CR2, CR3 WILL ALWAYS BE Ø WHEN READ

BLI BLI Bit Assignments

BLI-2Ø SCHEMATICS

12	11	10	9	8	7	6	5	4	3	2	1	
7404	7404	74175	74157	7411	33A 33A IRM742A IRM742A	7404	7404	SW-8	SW-8	BDR	BDR	A
1488	3341	3341	3341	74221	7408	7474	7400	RES 4.7K	7486	7486	BDR	B
1489A	COM-2601		2812		74221	7410	7408	74S133	74136	BDR	BDR	C
1489A	COM-2601		2812		7408	7474	7400	74221	82S50	74S74	BDR	D
1489A	COM-2601		2812		74221	7410	7404	74151	74151	74151	BDR	E
1488	7404	3341	3341	3341	74221	74175	74151	7404	7404	74273	BDR	F
BT16	555	7411	7408	74157	7400	74LS158	74153	74151	74174	BDR	BDR	G

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	7.4.77

NOTES :

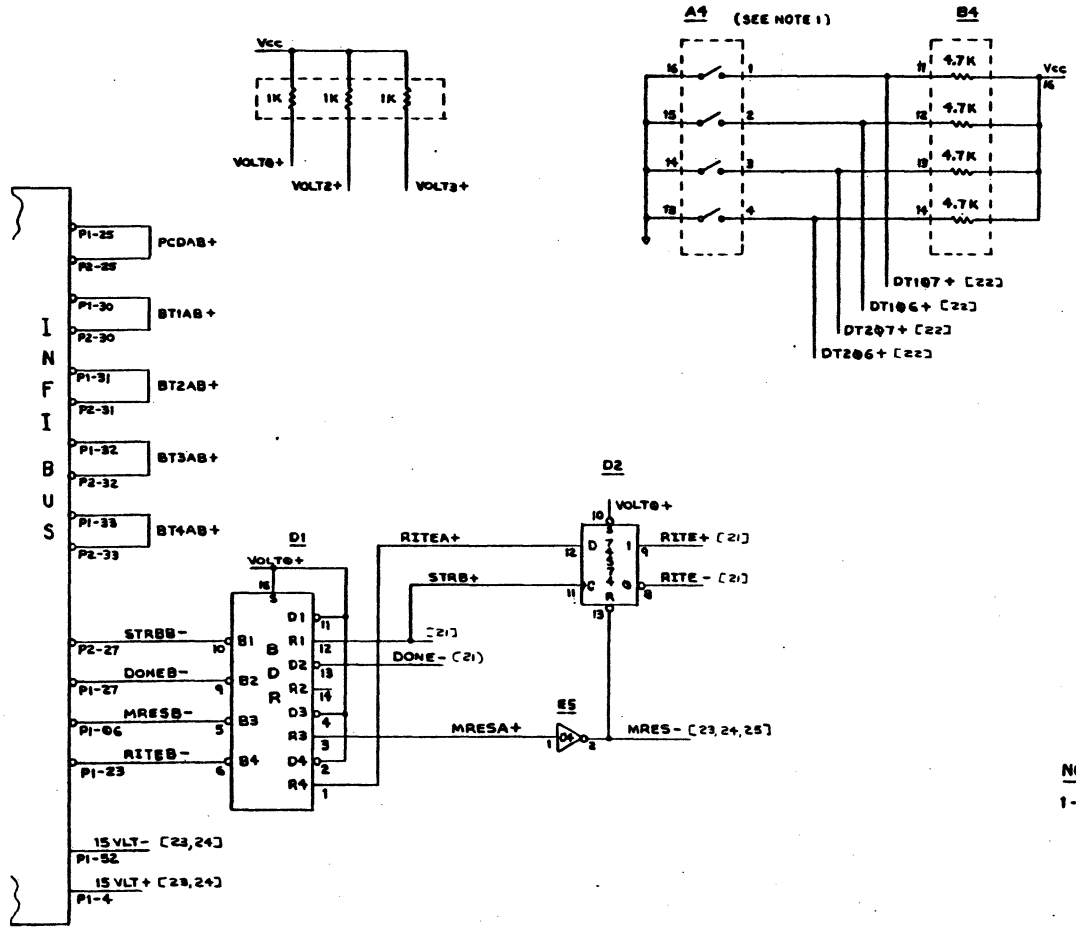
TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	12-2-76	TITLE	INTEGRATED CIRCUIT LAYOUT
CHECKED	MAW	1/14/77	CUSTOMER/NO.	DWG NO. / REV
APPROVED	MAW	1/14/77	HSMIMP	BLI-00-WW / A

BLI

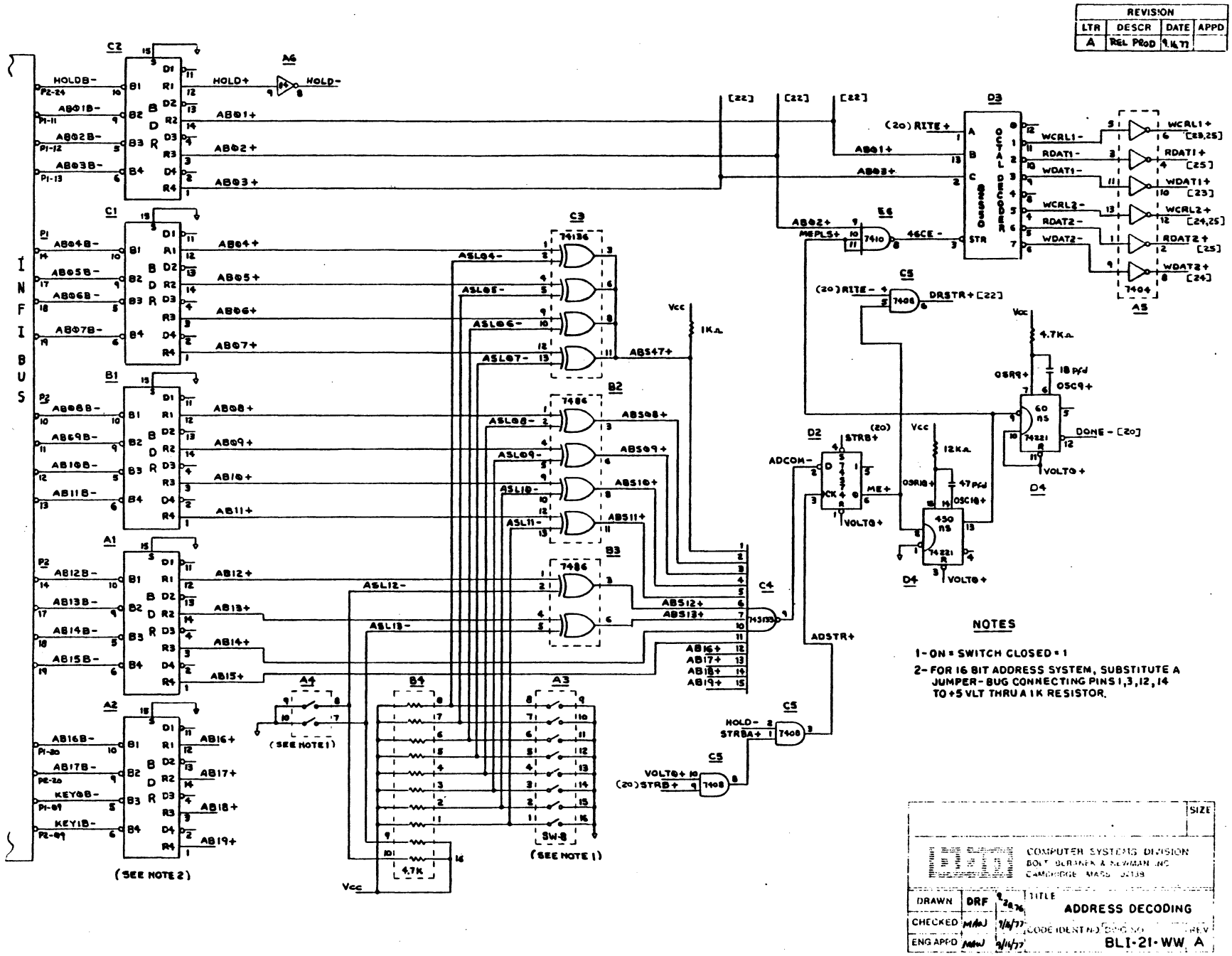
REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	9.16.77	

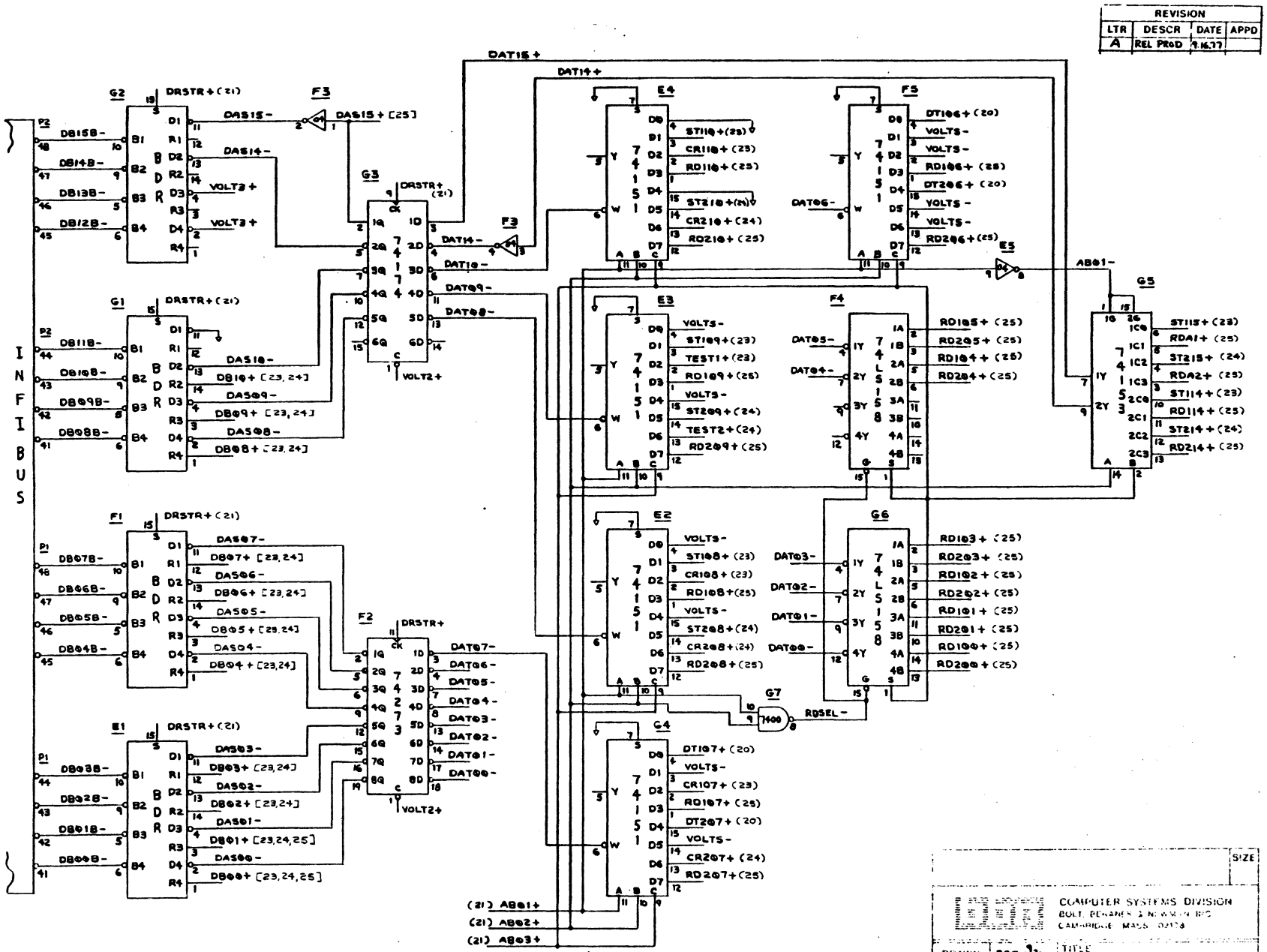


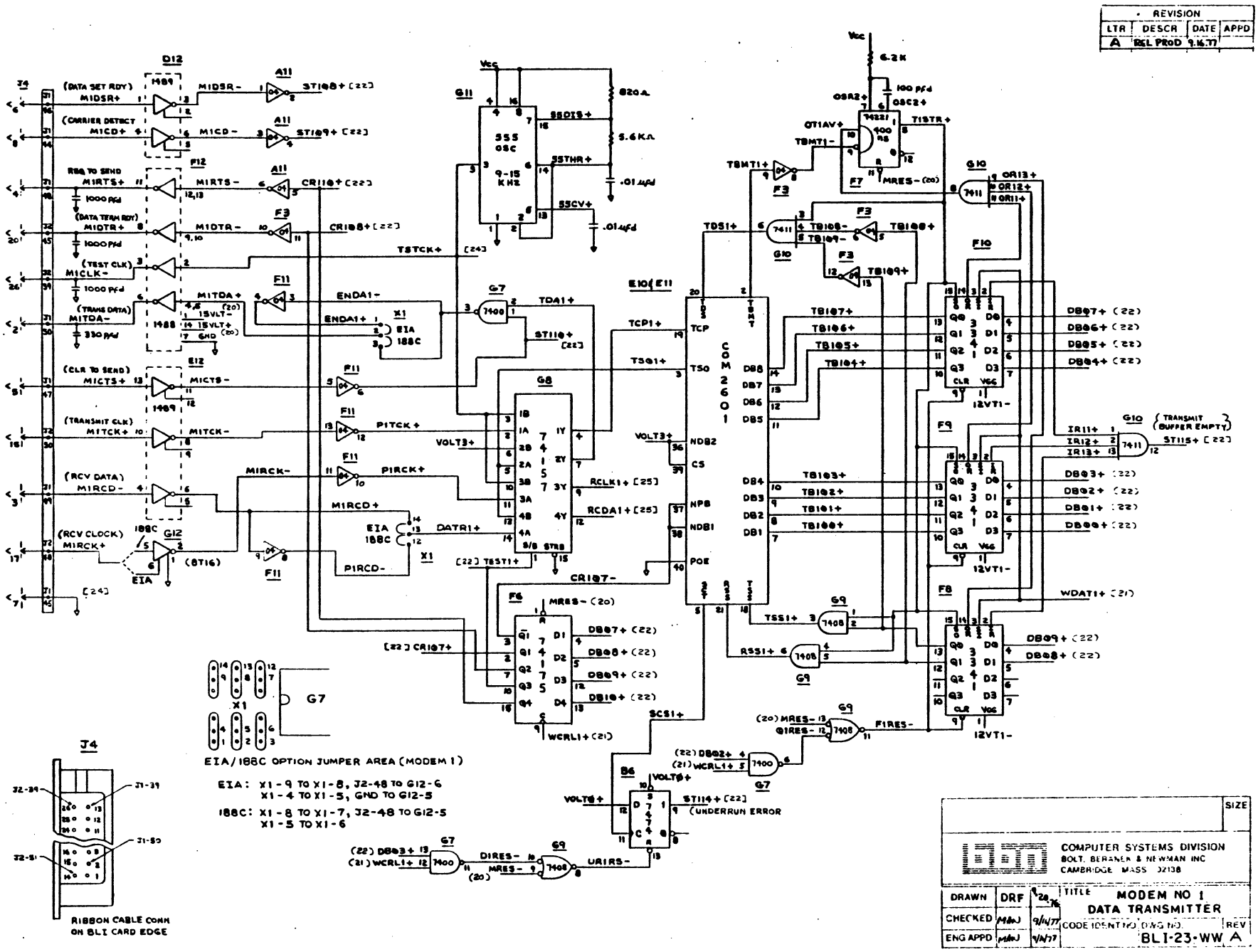
NOTES

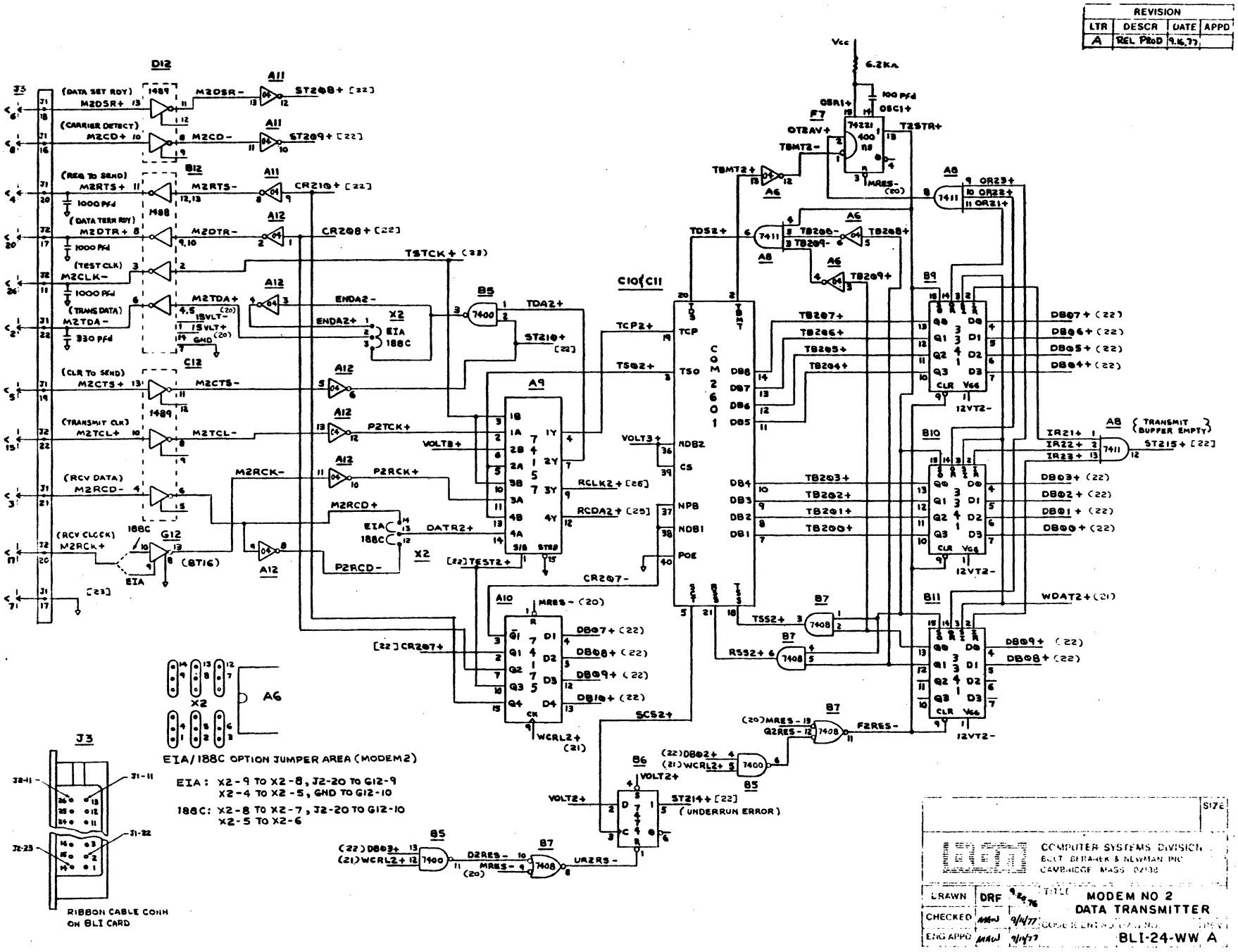
1 - OFF = SWITCH OPEN POSITION = 1

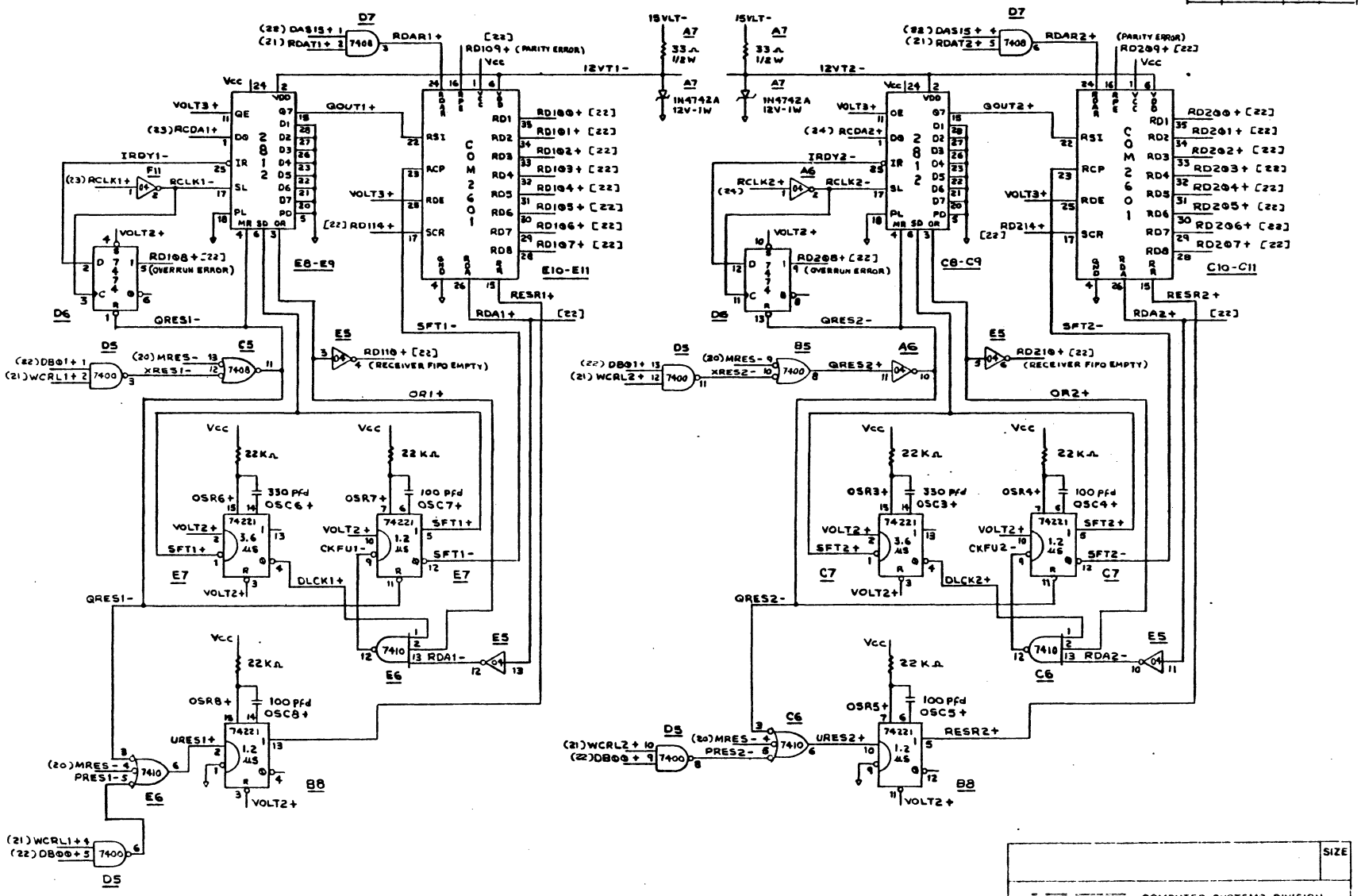
				SIZE
COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138				
DRAWN	DRF	9/4/77	TITLE MISC CONTROL SIGNALS	
CHECKED	MAW	9/4/77	CODE IDENT NO	DWG NO. REV BLI-20-WW A
ENG APPD	MAW	9/4/77		


REVISION
LTR | DESCR | DATE | APPD
A | REL PROD | 9.14.77
INFIBUS
C2
C1
B1
A1
A2
HOLDB-
AB01B-
AB02B-
AB03B-
AB04B-
AB05B-
AB06B-
AB07B-
AB08B-
AB09B-
AB10B-
AB11B-
AB12B-
AB13B-
AB14B-
AB15B-
AB16B-
AB17B-
KEY0B-
KEY1B-
HOLD+
HOLD-
AB01+
AB02+
AB03+
AB04+
AB05+
AB06+
AB07+
AB08+
AB09+
AB10+
AB11+
AB12+
AB13+
AB14+
AB15+
AB16+
AB17+
AB18+
AB19+
(SEE NOTE 2)
A6
C3
B2
B3
B4
A3
A4
ASL04-
ASL05-
ASL06-
ASL07-
ASL08-
ASL09-
ASL10-
ASL11-
ASL12-
ASL13-
ABS47+
ABS08+
ABS09+
ABS10+
ABS11+
ABS12+
ABS13+
ABS14+
ABS15+
ABS16+
ABS17+
ABS18+
ABS19+
1K.a.
4.7K
SW-8
(SEE NOTE 1)
(SEE NOTE1)
Vcc
C4
C5
ADSTR+
HOLD-
STRBA+
VOLT0+
(20)STRB+
[22]
D3
OCTAL DECODER
(20) RITE+
AB01+
AB03+
AB02+
MEPLS+
E6
7410
46CE-
STR
WCRL1-
RDAT1-
WDAT1-
WCRL2-
RDAT2-
WDAT2-
WCRL1+
RDAT1+
WDAT1+
WCRL2+
RDAT2+
WDAT2+
7404
A5
(20) RITE-
7408
DRSTR+ [22]
4.7K.a.
18 pfd
OSR9+
OSC9+
60 ns
74221
DONE- [20]
VOLT0+
D4
D2
(20)
STRB+
ADCOM-
ME+
12K.a.
OSR10+
47 pfd
OSC10+
450 ns
NOTES
1- ON = SWITCH CLOSED = 1
2- FOR 16 BIT ADDRESS SYSTEM, SUBSTITUTE A JUMPER- BUG CONNECTING PINS 1,3,12,14 TO +5 VLT THRU A 1K RESISTOR.
SIZE
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN DRF 9/28/76
CHECKED MHM 7/14/77
ENG APPD MHM 9/14/77
TITLE
ADDRESS DECODING
CODE IDENT NO
DWG NO
REV
BLI-21-WW A


REVISION
LTR DESCR DATE APPD
A REL PROD 9.16.77
INFIBUS
DAT15+
DAT14+
G2
DRSTR+(21)
F3
DAS15-
DAS15+[25]
DAS14-
VOLT3+
VOLT3+
DB15B-
DB14B-
DB13B-
DB12B-
G3
DRSTR+(21)
DAT14-
DAT13-
DAT09-
DAT08-
VOLT2+
G1
DRSTR+(21)
DAS10-
DB10+[23,24]
DAS09-
DB09+[23,24]
DAS08-
DB08+[23,24]
DB11B-
DB10B-
DB09B-
DB08B-
F1
DRSTR+(21)
DAS07-
DB07+[23,24]
DAS06-
DB06+[23,24]
DAS05-
DB05+[23,24]
DAS04-
DB04+[23,24]
DB07B-
DB06B-
DB05B-
DB04B-
F2
DRSTR+
DAT07-
DAT06-
DAT05-
DAT04-
DAT03-
DAT02-
DAT01-
DAT00-
VOLT2+
E1
DRSTR+(21)
DAS03-
DB03+[23,24]
DAS02-
DB02+[23,24]
DAS01-
DB01+[23,24,25]
DAS00-
DB00+[23,24,25]
DB03B-
DB02B-
DB01B-
DB00B-
E4
ST110+(23)
CR110+(23)
RD110+(25)
ST210+(24)
CR210+(24)
RD210+(25)
DAT06-
F5
DT106+(20)
VOLTS-
VOLTS-
RD106+(25)
DT206+(20)
VOLTS-
VOLTS-
RD206+(25)
E5
AB01-
E3
VOLTS-
ST109+(23)
TEST1+(23)
RD109+(25)
VOLTS-
ST209+(24)
TEST2+(24)
RD209+(25)
DAT05-
DAT04-
F4
RD105+(25)
RD205+(25)
RD104+(25)
RD204+(25)
G5
ST115+(23)
RDA1+(25)
ST215+(24)
RDA2+(25)
ST114+(23)
RD114+(25)
ST214+(24)
RD214+(25)
E2
VOLTS-
ST108+(23)
CR108+(23)
RD108+(25)
VOLTS-
ST208+(24)
CR208+(24)
RD208+(25)
DAT03-
DAT02-
DAT01-
DAT00-
G6
RD103+(25)
RD203+(25)
RD102+(25)
RD202+(25)
RD101+(25)
RD201+(25)
RD100+(25)
RD200+(25)
G7
7400
RDSEL-
E4
DT107+(20)
VOLTS-
CR107+(23)
RD107+(25)
DT207+(20)
VOLTS-
CR207+(24)
RD207+(25)
(21) AB01+
(21) AB02+
(21) AB03+
SIZE
COMPUTER SYSTEMS DIVISION
DRAWN DRF 9/20/76
CHECKED MAW 9/4/77
ENG APPD MAW 9/4/77
TITLE
DATA BDR'S & MUX
BL1-22-WW A


REVISION
LTR | DESCR | DATE | APPD
A | RSL PROD | 9.16.77
J4
(DATA SET RDY) MIDSR+
MIDSR-
ST108+ [22]
(CARRIER DETECT) MICD+
MICD-
ST109+ [22]
REQ TO SEND MIRTS+
MIRTS-
CR118+ [22]
(DATA TERM RDY) MIDTR+
MIDTR-
CR108+ [22]
(TEST CLK) MICLK-
(TRANS DATA) MITDA+
MITDA-
(CLR TO SEND) MICTS+
MICTS-
(TRANSMIT CLK) MITCK+
MITCK-
(RCV DATA) MIRCD+
MIRCD-
(RCV CLOCK) MIRCK+
MIRCK-
1000 pfd
330 pfd
15VLT+
15VLT-
GND
1489
1488
EIA
188C
(8T16)
[24]
TSTCK+
ENDA1+
ENDA1-
TDA1+
ST110+ [22]
PITCK+
PIRCK+
PIRCD-
DATR1+
VOLT3+
RCLK1+ [25]
RCDA1+ [25]
[22] TEST1+
CR107-
MRES- (20)
[22] CR107+
DB07+ (22)
DB08+ (22)
DB09+ (22)
DB10+ (22)
WCRL1+ (21)
SCS1+
VOLT8+
ST114+ [22]
(UNDERRUN ERROR)
(22) DB02+
(21) WCRL1+
DIRES-
URIRS-
(20) MRES-
FIRES-
RSS1+
TSS1+
TBMT1+
TBMT1-
QT1AV+
TISTR+
OSC2+
OSR2+
100 pfd
6.2K
820Ω
5.6KΩ
.01 μfd
.01 μfd
555 OSC
9-15 KHZ
SSOTS+
SSTHR+
SSCV+
COM2601
TCP
TSO
NDB2
CS
NPB
NDB1
POE
TBR
TBT
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
TS01+
TCP1+
TS01+
VOLT3+
TB107+
TB106+
TB105+
TB104+
TB103+
TB102+
TB101+
TB100+
TB108+
TB108-
TB109+
TB109-
IR11+
IR12+
IR13+
OR13+
OR12+
OR11+
12VT1-
(TRANSMIT BUFFER EMPTY)
ST115+ [22]
WDAT1+ [21]
DB03+ (22)
DB02+ (22)
DB01+ (22)
DB00+ (22)
DB09+ (22)
DB08+ (22)
DB07+ (22)
DB06+ (22)
DB05+ (22)
DB04+ (22)
EIA/188C OPTION JUMPER AREA (MODEM 1)
EIA: X1-9 TO X1-8, J2-48 TO G12-6
X1-4 TO X1-5, GND TO G12-5
188C: X1-8 TO X1-7, J2-48 TO G12-5
X1-5 TO X1-6
RIBBON CABLE CONN ON BLI CARD EDGE
J2-49
J1-49
J2-51
J1-50
SIZE
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS. 02138
DRAWN DRF 9/28/76
CHECKED 9/14/77
ENG APPD 9/14/77
TITLE MODEM NO 1
DATA TRANSMITTER
CODE IDENT NO DWG NO REV
BLI-23-WW A


REVISION
LTR | DESCR | DATE | APPD
A | REL PROD | 9.16.77
J3
D12
A11
B12
C12
G12
(DATA SET RDY) M2DSR+
(CARRIER DETECT) M2CD+
(REQ TO SEND) M2RTS+
(DATA TERM RDY) M2DTR+
(TEST CLK) M2CLK-
(TRANS DATA) M2TDA+ M2TDA-
(CLR TO SEND) M2CTS+
(TRANSMIT CLK) M2TCL+
(RCV DATA) M2RCD-
(RCV CLOCK) M2RCK+
M2DSR- M2CD- M2RTS- M2DTR- M2CTS- M2TCL-
ST208+ [22]
ST209+ [22]
CR210+ [22]
CR208+ [22]
TSTCK+ (23)
ENDA2- ENDA2+
TDA2+
ST210+ [22]
P2TCK+
P2RCK+
M2RCK-
M2RCD+
P2RCD-
DATR2+
TEST2+ [22]
CR207-
MRES- (20)
WCRL2+ (21)
DB07+ (22)
DB08+ (22)
DB09+ (22)
DB10+ (22)
[22] CR207+
SC52+
RCLK2+ [26]
RCDA2+ [25]
TCP2+
TSO2+
VOLT3+
TDS2+
TB207+
TB206+
TB205+
TB204+
TB203+
TB202+
TB201+
TB200+
TSS2+
RSS2+
DB07+ (22)
DB06+ (22)
DB05+ (22)
DB04+ (22)
DB03+ (22)
DB02+ (22)
DB01+ (22)
DB00+ (22)
WDAT2+ (21)
DB09+ (22)
DB08+ (22)
IR21+
IR22+
IR23+
ST215+ [22]
(TRANSMIT BUFFER EMPTY)
ST214+ [22]
(UNDERRUN ERROR)
(22) DB02+
(21) WCRL2+
(22) DB03+
(21) WCRL2+
D2RES-
UR2RS-
F2RES-
Q2RES-
6.2KΩ
100 PFd
OSC1+
OSC2+
T2STR+
OT2AV+
TBMT2-
TBMT2+
MRES- (20)
12VT2-
Vcc
Vee
GND
15VLT+
15VLT-
X2
EIA
188C
EIA/188C OPTION JUMPER AREA (MODEM2)
EIA: X2-9 TO X2-8, J2-20 TO G12-9
X2-4 TO X2-5, GND TO G12-10
188C: X2-8 TO X2-7, J2-20 TO G12-10
X2-5 TO X2-6
RIBBON CABLE CONN ON BLI CARD
SIZE
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN DRF 9/16/76
CHECKED MAW 9/14/77
ENG APPD MAW 9/14/77
TITLE MODEM NO 2 DATA TRANSMITTER
BLI-24-WW A


REVISION
LTR DESCR DATE APPD
A REL PROD 9.6.77
D7
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(21) RDAT1+ 2
7408
RDAR1+
[22]
RD109+ (PARITY ERROR)
15VLT-
A7
33Ω 1/2W
A7
1N4742A 12V-1W
12VT1-
Vcc
VOLT3+
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IRDY1-
(23) RCLK1+
RCLK1-
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2812
COM2601
GOUT1+
VOLT3+
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RD100+ [22]
RD101+ [22]
RD102+ [22]
RD103+ [22]
RD104+ [22]
RD105+ [22]
RD106+ [22]
RD107+ [22]
VOLT2+
RD108+ [22]
(OVERRUN ERROR)
E8-E9
E10-E11
D6
QRES1-
RESR1+
RDA1+ [22]
SFT1-
D5
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(20) MRES- 13
XRES1- 12
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C5
ES
RD110+ [22]
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OSC6+
OSR6+
100 pfd
OSC7+
OSR7+
74221
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1.2 4.6
VOLT2+
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SFT1+
DLCK1+
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E6
OSR8+
100 pfd
OSC8+
URES1+
PRES1-5
B8
(21) WCRL1+ 4
(22) DB00+ 5
7400
D5
15VLT-
A7
33Ω 1/2W
A7
1N4742A 12V-1W
12VT2-
D7
(22) DAS15+ 4
(21) RDAT2+ 5
7408
RDAR2+
(PARITY ERROR)
RD209+ [22]
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(24) RCDA2+
IRDY2-
RCLK2+
(24)
RCLK2-
A6
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COM2601
GOUT2+
VOLT3+
RD214+
[22]
RD200+ [22]
RD201+ [22]
RD202+ [22]
RD203+ [22]
RD204+ [22]
RD205+ [22]
RD206+ [22]
RD207+ [22]
VOLT2+
RD208+ [22]
(OVERRUN ERROR)
C8-C9
C10-C11
D6
QRES2-
RESR2+
RDA2+ [22]
SFT2-
D5
(22) DB01+ 13
(21) WCRL2+ 12
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(20) MRES- 9
XRES2- 10
7400
B5
A6
QRES2+
ES
RD210+ [22]
(RECEIVER FIFO EMPTY)
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22KΩ
330 pfd
OSC3+
OSR3+
100 pfd
OSC4+
OSR4+
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3.6 4.6
1.2 4.6
VOLT2+
SFT2+
CKFU2-
SFT2+
DLCK2+
C7
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13 RDA2-
C6
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OSC5+
URES2+
PRES2-
RESR2+
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7400
D5
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C6
B8
SIZE
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE MASS 02138
DRAWN DRF 2/9/77
CHECKED 9/4/77
ENG APPD 9/9/77
TITLE
MODEM NO 1 & 2
DATA RECEIVERS
CODE IDENT NO DWG NO
BLI-25-WW
REV
A

BLI

Bus Extender

BXD-Ø2 Logic Description

BXD-15 Standard Modification

BXR-15 Standard Modification

BXD-2Ø Schematic

BXD
BXR

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		
B	ECN 0227	9/15	

BXD
BXR

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BXD LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		BXD-02

SCALE | REV B | SHEET OF

SUE 1827 INFIBUS EXTENDER KIT

MAINTENANCE BULLETIN

BXD
BXR

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Oct 74

CONTENTS

SUE 1827 INFIBUS EXTENDER KIT
MAINTENANCE BULLETIN

INTRODUCTION

This bulletin contains detailed information pertaining to the SUE 1827 INFIBUS Extender Kit. SUE 1827 is designed to increase system circuit card capacity by interconnecting two SUE chassis. The kit consists of the following items:

a. SUE 1828 Bus Extender Driver (BXD)
b. SUE 1829 Bus Extender Receiver (BXR)
c. SUE 7730-1, -2, or -3 Cable Assembly.

Both the BXD and BXR are each contained on a single, standard-size SUE circuit card. The BXD is plugged into the INFIBUS of the main chassis; the BXR into the INFIBUS of the auxiliary chassis. The 7730 cable assembly interconnects the BXD and BXR at their back edge connectors, and is fabricated in one of three standard lengths to accommodate chassis location.

Cable	Length
7730-1	3 feet ± 1/2 inch
7730-2	6 feet ± 1 inch
7730-3	10 feet ± 1-1/2 inches

BXD
BXR

Special cables can be fabricated up to 20 feet.

EXTENDED LINES

Extended bus lines are interconnected on a one-for-one basis. The block diagram in figure 1 shows the bus extender interconnections and signal direction. Signal designations at the cable drivers/receivers are prefixed by the letter C but otherwise they are the same as those for the INFIBUS. Most of the extender lines are bi-directional, where a signal is driven and received on a single line

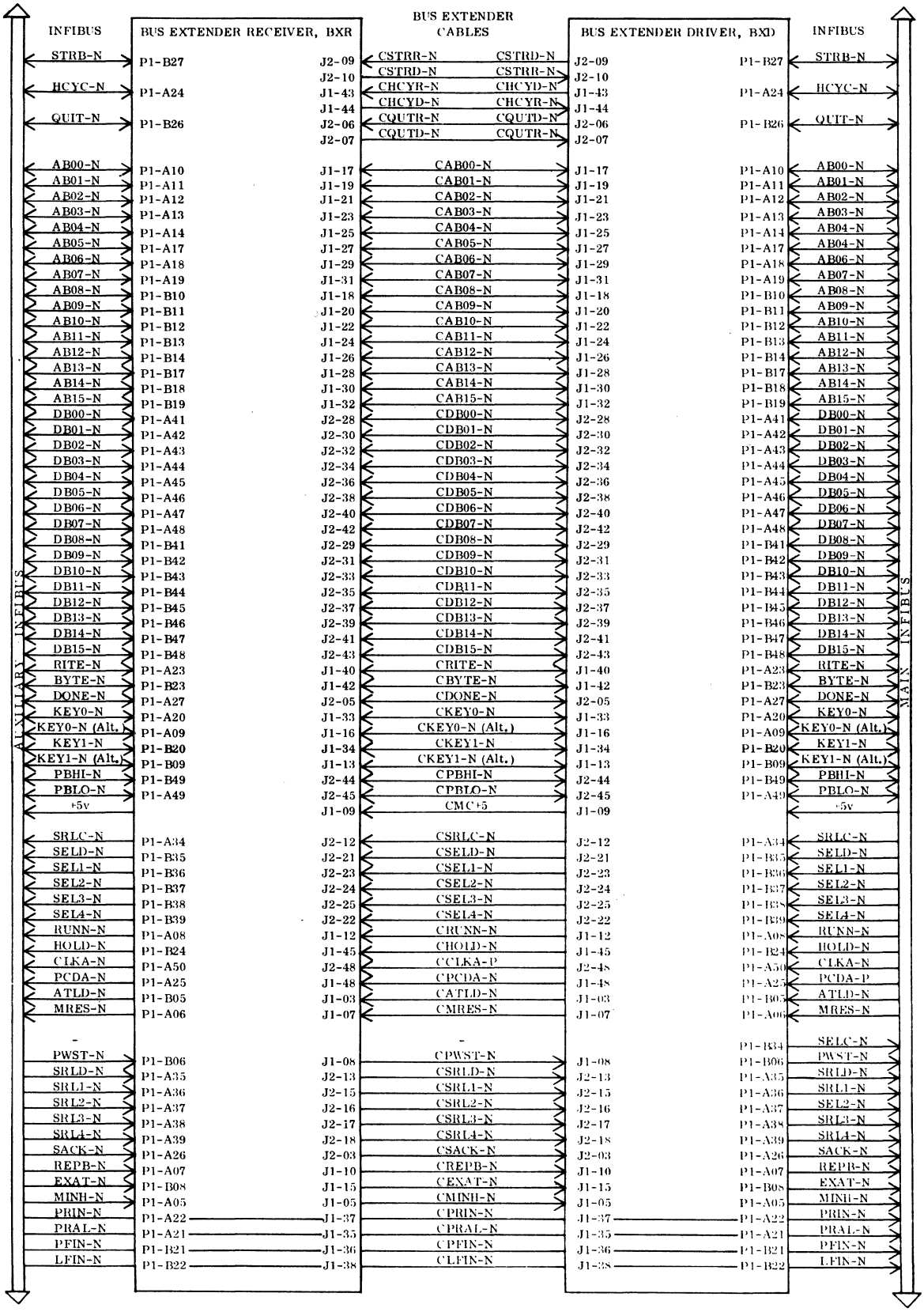


Figure 1. SUE 1827 INFIBUS Extender Kit, Block Diagram

by both the BXD and BXR. These include the address, data and mode control lines. Three extender lines, Strobe (STRB-N), Half Cycle (HCYC-N), and Quit (QUIT-N) are driven and received on separate lines by both the BXD and BXR. Another twelve lines of the extender are driven only by the BXD and received by the BXR and ten lines are driven only by the BXR and received by the BXD. Power fail/restart lines PRIN-N, PRAL-N, PFIN-N and LFIN-N are extended only and contain no drivers or receivers in either the BXD or BXR.

NON-EXTENDED LINES

Twelve lines on the INFIBUS are neither extended nor driven in the bus extender. These unused lines are not shown in Figure 1 and are listed here for reference only:

INFIBUS Line	Pin	INFIBUS Line	Pin
BT1A-N	P1-A30	BT1B-N	P1-B30
BT2A-N	P1-A31	BT2B-N	P1-B31
BT3A-N	P1-A32	BT3B-N	P1-B32
BT4A-N	P1-A33	BT4B-N	P1-B33
PCDB-N	P1-B25	LFRQ-N	P1-B07
SELC-N	P1-B34	(Reserved)	P1-B50

INSTALLATION

Install the bus extender kit as follows:

BXD
BXR

1. Plug the BXD into the next slot left of the last-occupied slot in the main chassis. The BXD must be the last circuit card in the precedence chain of the main chassis.

2. Plug the BXR into the right-most slot in the auxiliary chassis. The BXR must be the first circuit card in the precedence chain of the auxiliary chassis.

3. Interconnect the BXD and BXR at their back edge connectors using the bus extender cable assembly.

SUE circuit cards can be located in either chassis except for the bus controller, central processor, and secondary processors which must be located in the main chassis. Generally, devices that are accessed infrequently such as the control panel, auto-load, and teletypewriter are located in the auxiliary chassis. Devices requiring access more frequently such as disk controllers are located in the main chassis where they have higher precedence for bus access. Following are the restrictions for circuit card placement in two-chassis systems:

a. The bus controller, central processor and all secondary processors must be located in the main chassis.

b. All circuit cards of a device controller combined with a block transfer adapter must be located in the same chassis.

c. In systems containing a control panel and auto-load, there are two alternatives: both modules can be located in the auxiliary chassis; or the auto-load card can be located in either chassis if the control panel is in the main chassis.

LOGIC DESCRIPTION

The logic implemented in the BXD and BXR uses a master-slave arrangement to transfer signals from one INFIBUS to the other. Either the BXD or the BXR can be the master, while the other is the slave, during execution of any read or write transfer. The extender card in the INFIBUS on which Strobe (STRB-N) originates, in the presence of Select Acknowledge (SACK-N), becomes the master; the other extender card becomes the slave until the read or write half-cycle is completed. STRB-N remains asserted for a full read/modify/write cycle. The read half cycle is defined by the combination of the half-cycle signal (HCYC-N) asserted, and the write signal (RITE-N) negated. Negation of the half cycle signal after Done (DONE-N) time, ends the read half-cycle. Signal RITE-N asserted, defines the write half cycle which follows the read. Negation of STRB-N after DONE-N ends the cycle and disables the bus extender.

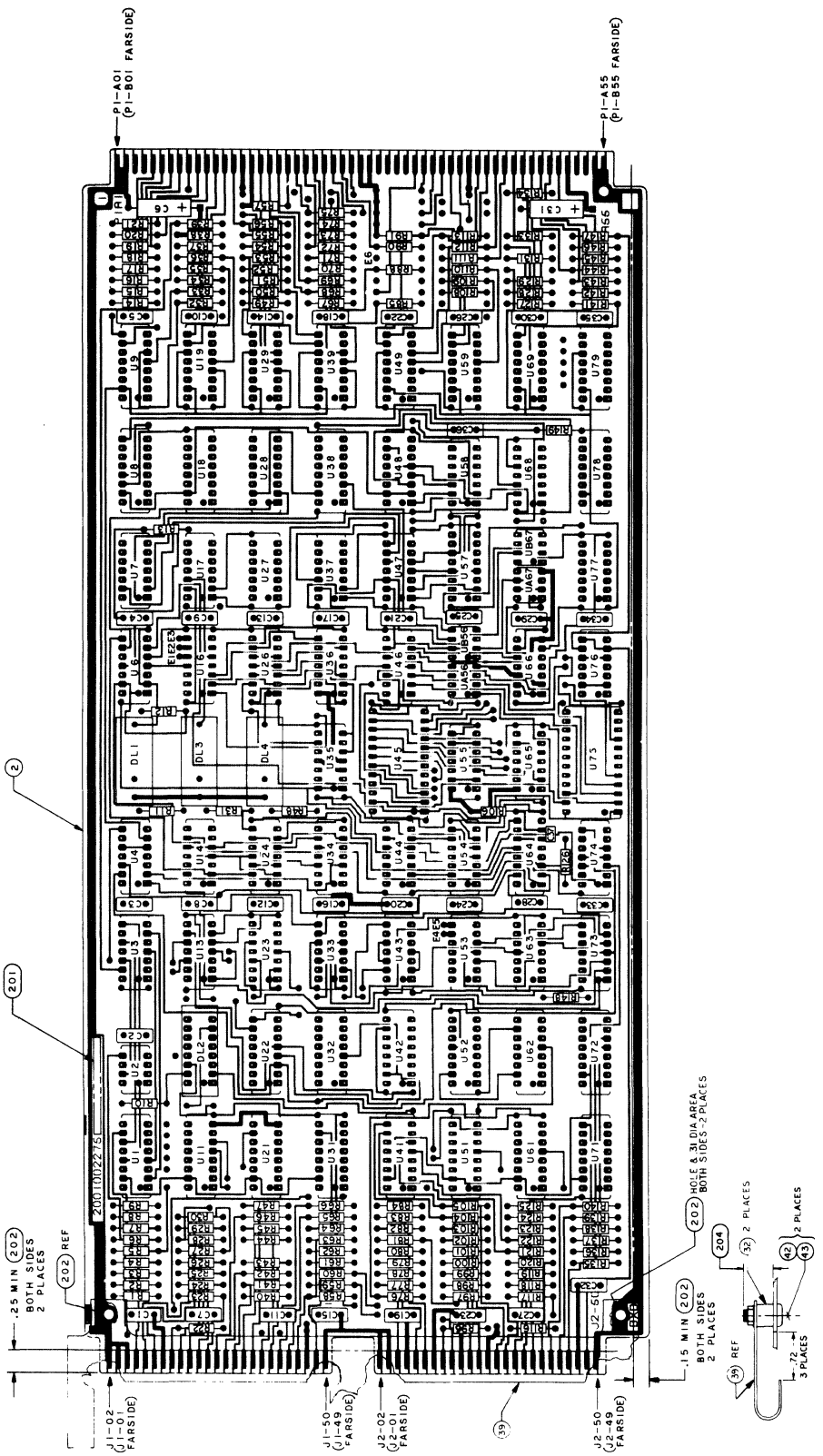
In describing the logic contained on the pages that follow, the terms master read, slave read, master write and slave write refer to the operating modes of the BXD and BXR during the read and write half cycles. For example, the BXD in the master read mode means that the BXR is in slave read mode and read data from the auxiliary INFIBUS is to be transferred through the BXR, extender cable and BXD to the main chassis INFIBUS. A selected set of gates, and cable/bus drivers/receivers are enabled in the BXD and BXR to accomplish this operation. The BXD in the master write mode means that the BXR is in the slave write mode, and data is to be transferred from the main INFIBUS and BXD, to the BXR and auxiliary INFIBUS. A different set of logic gates and drivers/receivers is enabled to accomplish this operation and those that were enabled for the read half cycle are disabled. For other read and write operations, the BXR can be the master and BXD the slave.

DRAWINGS AND PARTS LIST

The drawings and parts lists that follow in this bulletin are listed below. Each logic diagram is accompanied by a brief description that explains the purposes of the logic. Definitions of key logic terms that originate on the diagrams are provided also.

Drawing or Parts List	Drawing Number	Sheets
SUE 1828 Bus Extender Driver BXD, Circuit Card Assembly	2001002275-1	1
SUE 1828 Bus Extender Driver BXD, Logic Diagram	LD2001002275-1	1 thru 8
SUE 1829 Bus Extender Receiver BXR, Circuit Card Assembly	2001002276-1	1
SUE 1829 Bus Extender Receiver BXR, Logic Diagram	LD2001002276-1	1 thru 8
SUE 7730-1, -2, -3 Cable Assembly	2002001320	1
SUE 1828 Bus Extender Driver, Parts List	PL2001002275-1	2,3,4
SUE 1829 Bus Extender Receiver, Parts List	PL2001002276-1	2,3,4
SUE 7730-1, -2, -3 Cable Assembly, Parts List	PL2002001320	2,3,4

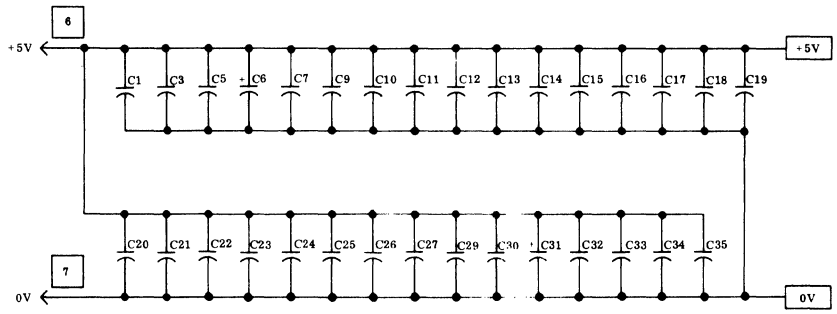
BXD
BXR

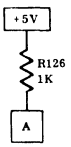


SUE 1828 Bus Extender Driver BXD, Circuit Card Assembly
2001002275-1, Rev. A, Sheet 1

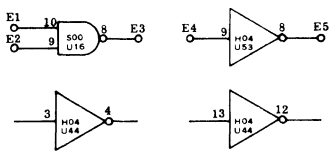
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1μf, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33μf, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V, EXCEPT H103, PIN 4 +5V, PIN 11 0V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR, PIN 7 AND 8 0V, PIN 16 +5V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V.
6. +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51.
7. 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J1-1, 2, 4, 6, 11, 14, 39, 41, 46, 47, 49, 50; J2-1, 2, 4, 8, 11, 14, 19, 20, 26, 27, 46, 47, 49, 50.
8. -15V CONNECTOR PINS ARE: P1-A52, A53, B52, B53.
9. +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4.





SPARE GATES



BXD
BXR

SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 1 of 8

READ/WRITE CONTROL AND DONE LOGIC (BXD, LD Sheet 2)

With master flip-flop MASS-P (BXD, LD sheet 3) set, and HCYC-N asserted on the main INFIBUS, Half-Cycle signal CHCYD-N is driven across the cable,and Read/Modify/Write flip-flop is set during the read half-cycle. When DONE-N is received from the Slave Controller, HCYC-N is negated and defines the end of the read half cycle. After the modify portion of the cycle the write half-cycle starts when RITE-N, address, and new data are asserted by the the master controller. Address lines remain latched during the entire half-cycle mode in the slave bus extender until STRB-N is negated. During the write half-cycle, the master bus extender allows for an inherent 75-nanosecond skew. This skew occurs between the data enable cable driver lines, delay line, and associate gates RITC, RITB, and SRMR and the write cable driver CRITN-N, the same delay line, and RITD gates.

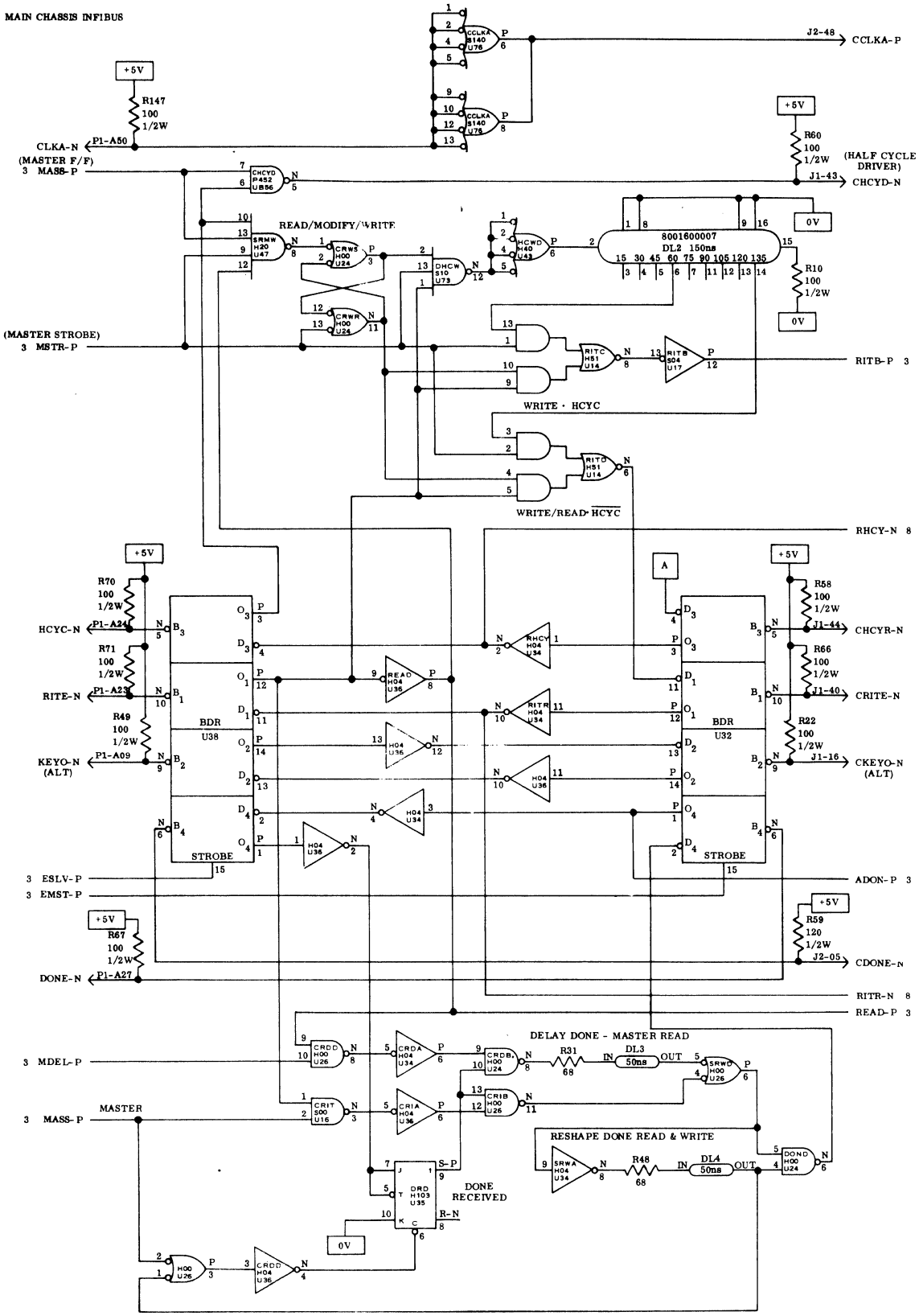
DONE LOGIC

In the master read mode, after master flip-flop MASS is set, MDEL-P (BXD LD sheet 3) enables the DONE logic when the master extender receives CDONE-N from the slave extender and Done-Received flip-flop (DRD) is set. The received Done is delayed 50 nanoseconds to allow for the data received to be stable at the receiver of the master controller before its receipt of DONE-N. Done-Received is cleared 120 nanoseconds after it has been set. DONE-N is reshaped to 50 ± 10 nanoseconds before being asserted on the master chassis INFIBUS.

In the write mode, gates CRIT and CRIB in the DONE logic are enabled and no delay in DONE-N occurs. However, DONE-N is reshaped, and the Done-Received flip-flop is cleared 60 nanoseconds after it has been set. In the slave bus extender, the Done-Received flip-flop (DRD) remains cleared by MASS-P, which is negated.

KEY SOURCE LOGIC DEFINITIONS

ADON-P	Activated with receipt of DONE-N to enable the Slave Read Done term (SRDM-N, BXD sheet 3) which clocks the data register.
CCLKA-P	The 25-MHz clock from the main chassis.
CDONE-N	The cable driver receiver for the DONE pulse generated by the receiving system module to signal the end of a read or write half cycle.
CHCYD-N	The half-cycle cable driver. HCYC-N is used by the BXD with READ-P to detect the read portion of a read/modify/write cycle.
CHCYR-N	The cable receiver of the half-cycle line received by the BXD during a slave read cycle to become RCHY-N.
CKEY0-N (ALT)	Memory Protect key transmitted with the address. See address description, BXD LD sheet 7.
CRITE-N	The cable RITE-N line that transmits and receives the write mode control signal.
READ-P	Generated when term RITE-N is not asserted on the INFIBUS. Used along with HCYC-P to define the master read mode.
RHCY-N	Received Half-Cycle from the BXR. Used in the BXD to disable the data bus drivers/ receivers at the end of a read half-cycle during slave read mode, through SRIT-N.
RITB-P	Master write derived from RITE-N and used in the BXD to enable SRDM-N which clocks the data register, and SRMR-P which enables the data cable bus drivers/ receivers.
RITR-N	Write signal received from the BXR to enable the write half cycle. Enables the data bus drivers/receivers in the BXD (through CRIT-P) during slave write mode.



BXD
BXR

SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 2 of 8

MASTER/SLAVE CONTROL, AND SELECT ACKNOWLEDGE LOGIC (BXD, LD Sheet 3)

Assertion of STRB-N and the presence of SACK-N at an INFIBUS enables the BXD or BXR on that INFIBUS to function in the master mode by setting Enable Master flip-flop ENM, latching SACK-N for 120 nanoseconds after STRB-N is sensed, and setting master flip-flop MASS. The master flip-flop functions to:

a. Enable, through gate EMST, the cable drivers of address (AB00-N - AB15-N), BYTE-N, RITE-N and HCYC-N, and to enable receipt of DONE via the cable.

b. Disable, through gate ESLV, INFIBUS drivers of STRB-N, Address, BYTE-N, RITE-N and HCYC-N.

c. Enable, through gate SWMR, the data received from the slave bus extender via the cable, which is latched if in Read mode. In Write mode, the data cable drivers are enabled by gate SRMR.

d. Enable Cable Strobe Driver CSTRD, through gate DMST, which, in turn, clears the Enable Master flip-flop (ENM), thus preparing to clear the master flip-flop when STRB-N is negated and to set it again when STRB-N is asserted while SACK-N is present. When STRB-N is negated by a master controller, the bus extender located in the same chassis (master) clears its master flip-flop, and disables all the address, data, byte, RITE and HCYC drivers mentioned in item b. STRB-N is delayed by a 50-nanosecond delay line in the slave bus extender plus gate delays in the master bus extender to ensure that addresses, data and commands are stable before detection of STRB-N at the receiver end of the slave controller.

SELECT ACKNOWLEDGE

Select Acknowledge, CSAK-N, is driven across the cable by the BXR when the auxiliary chassis has been selected by SELx-N. The BXR latches SACK-N if the previous strobe from the auxiliary chassis is negated, therefore, output HAKR-N of the 120-nanosecond one-shot is high. SACK-N remains asserted internally in the BXR for 120 nanoseconds beyond assertion of STRB-N by the auxiliary chassis. SACK-N is kept asserted on the main chassis for at least 120 nanoseconds after being negated on the auxiliary chassis INFIBUS. Therefore SACK-N is not negated before STRB-N is detected at the main chassis INFIBUS.

The BXD does not latch SACK-N when it originates in the auxiliary chassis. However, to prevent the Bus Control Unit (BCU) from selecting any service request originating in the auxiliary chassis until STRB-N is received there, SACK-N is latched in the BXD and on the main chassis INFIBUS for 120 nanoseconds beyond assertion of STRB-N by the main chassis.

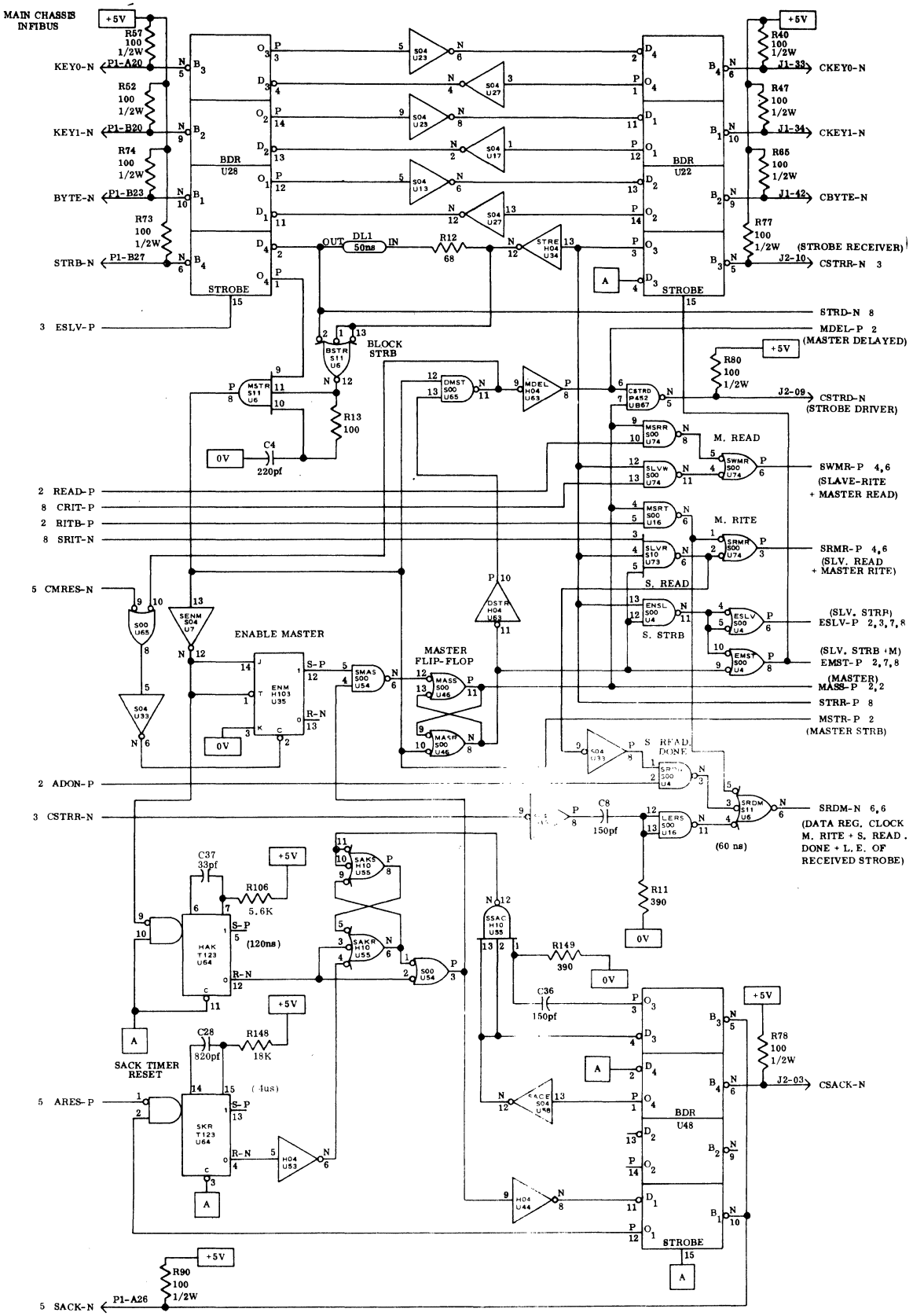
The 4-microsecond one-shot in the BXD functions to reset the SACK latch when a pseudo-SACK is generated by the BCU.

BXD
BXR

MASTER/SLAVE CONTROL, AND SELECT ACKNOWLEDGE LOGIC (BXD, LD Sheet 3) (continued)

KEY SOURCE LOGIC DEFINITIONS

CBYTE-N, CKEY0-N, CKEY1-N	Cable drivers/receivers of BYTE and KEY bits, the drivers of which are enabled by EMST-P to transmit these bits along with the address. See Address description (BXD LD sheet 7).
CSACK-N	Select acknowledge received from the auxiliary INFIBUS.
CSTRR-N	Received strobe from the BXR which enables the slave mode in the BXD.
CSTRD-N	Strobe cable driver, enabled by the master extender to transmit STRB-N to the slave extender.
EMST-P	Enables the cable bus drivers to transmit address (including KEY bits), RITE-N, BYTE-N, and HCYC-N.
ESLV-P	Enables the INFIBUS drivers of AB00-N - AB15-N, STRB-N, RITE-N, BYTE-N and HCYC-N in the BXD when a slave. Simultaneously, ESLV-P in the BXR is negated to disable these bus drivers. This signal is always negated in the master and asserted in the slave.
MASS-P	Set in the master extender and reset in the slave, the set output of this flip-flop enables the master read and write modes (through SWMR-P, SRMR-P), the cable drivers for Half-Cycle and Strobe, and the set input to the Read/Modify/Write flip-flop for the read half cycle. At the end of the write Half-cycle, enables the Done reshape logic which reshapes DONE-N received from the slave to be transmitted on the INFIBUS of the master.
MDEL-P	Master Strobe delayed — asserted in the master extender to enable the Done logic at the end of the read half cycle.
MSTR-P	Master strobe asserted in the master extender to enable the master flip-flop and read/modify/write flip-flop. MSTR-P is negated in the slave extender.
SRDM-N	Clears the data register at leading edge of received strobe. Loads the data register in Master Write mode and at Done time in the slave read mode.
SRMR-P	SRMR-P Slave Read or Master Rite, used together with SWMR-P. In Master Rite, the master extender latches and transmits data to the slave extender. In Slave Read mode, the slave extender latches and transmits the data at DONE-N time. SRMR-P enables the cable drivers and SWMR-P disables the INFIBUS drivers.
STRD-N	Delayed strobe received from the BXR. The leading edge clears the interrupt select flip-flop in the BXD.
STRR-P	Strobe received from the BXR. The trailing edge (strobe negated) clears Rite Simulated flip-flop RTS.
SWMR-P	Slave Write or Master Read, used together with SRMR-P. SWMR enables data INFIBUS drivers and SRMR-P (negated) disables data cable drivers.



SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 3 of 8

BXD
BXR

QUIT, REQUEST C, SELECT D, HOLD-N AND DATA (BXD, LD Sheet 4)

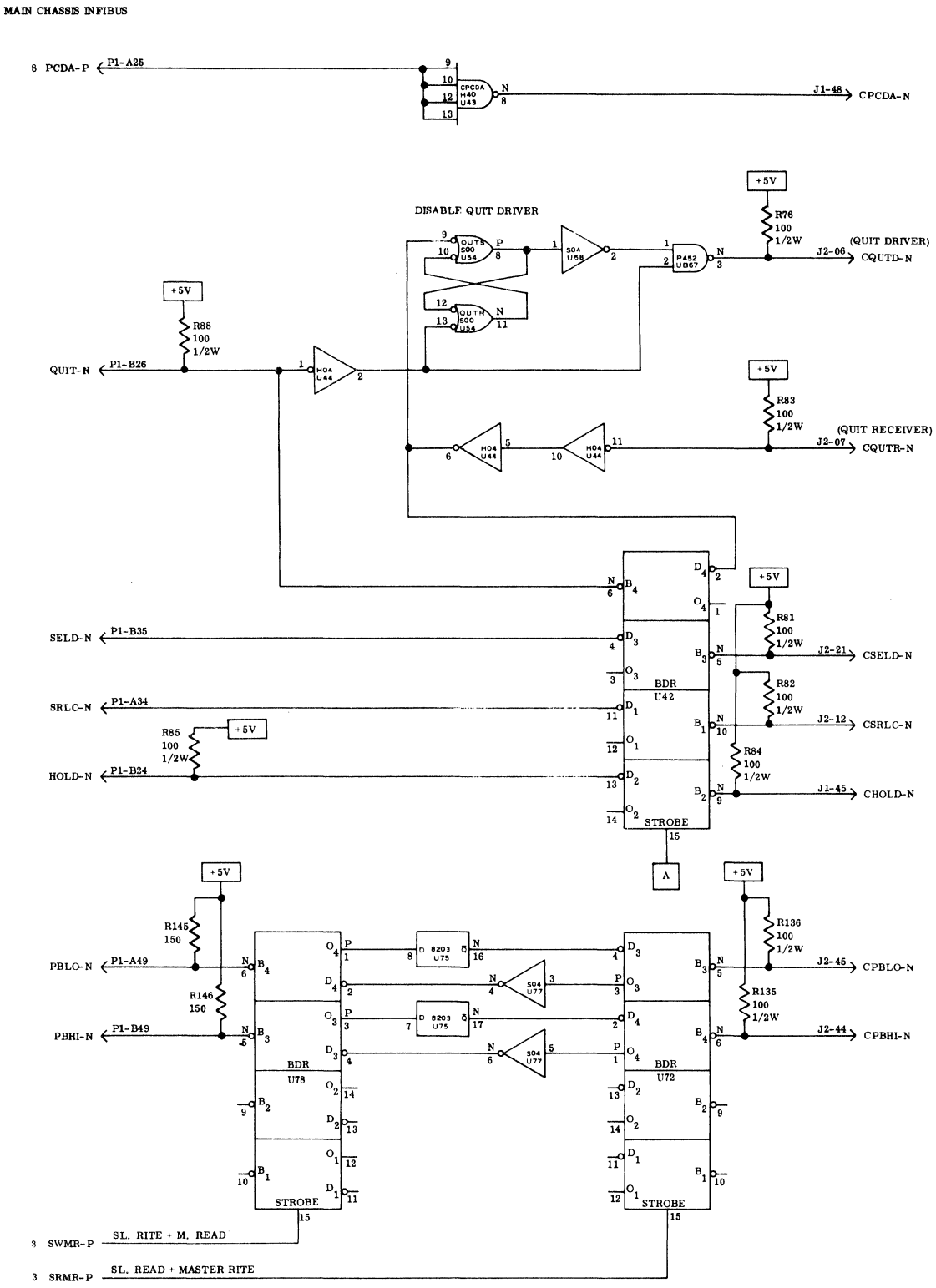
The Quit logic consists of a cable driver, CQUTD-N, and a cable receiver CQUTR-N. The Quit driver is normally enabled to drive QUIT-N from the main chassis INFIBUS. A Quit signal received from the BXR, disables the Quit Driver and the received Quit is driven onto the main chassis INFIBUS.

The Service Request Computer (CSRLC-N), Select Device (SELD-N) and Hold (CHOLD-N) signals are driven by the BXD to the BXR. Their drivers are always enabled.

Data bits CPBLO-N and CPBHI-N are bi-directional and are driven along with data bits CDB00-N through CDB15-N. The BXD receives the data in the Master Read or Slave Rite mode at which time signal SWMR-P enables the bus drivers. The cable drivers are disabled by SRMR-P. In Master Rite or Slave Read mode the BXD latches the data from the main INFIBUS and transmits it to the BXR. The BXR bus drivers are enabled and its cable drivers are disabled.

KEY SOURCE LOGIC DEFINITIONS

CPCDA-N	Precedence chain cable driver which sends the precedence pulse to the auxiliary chassis. This pulse is delayed 50 nanoseconds and reshaped to 50 ± 10 nanoseconds by the BXR before transmission onto the auxiliary chassis.
CQUTD-N, CQUTR-N	The Quit cable driver and receiver, respectively. The Quit driver is disabled if the source of Quit is from the auxiliary chassis through CQUTR-N. If the source is from the INFIBUS, the driver is enabled.
CSELD-N, CSRLC-N CHOLD-N	Cable drivers for the Select Device, Service Request Computer, and Hold signals, respectively, all sent from the BXD to the BXR. These cable drivers are always enabled.
CPBLO-N, CPBHI-N	Data bits transferred along with CDB00-N through CDB15-N to carry memory parity status for right and left bytes, respectively.



BXD
BXR

SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 4 of 8

SERVICE REQUEST LINES AND POWER STATUS (BXD, LD Sheet 5)

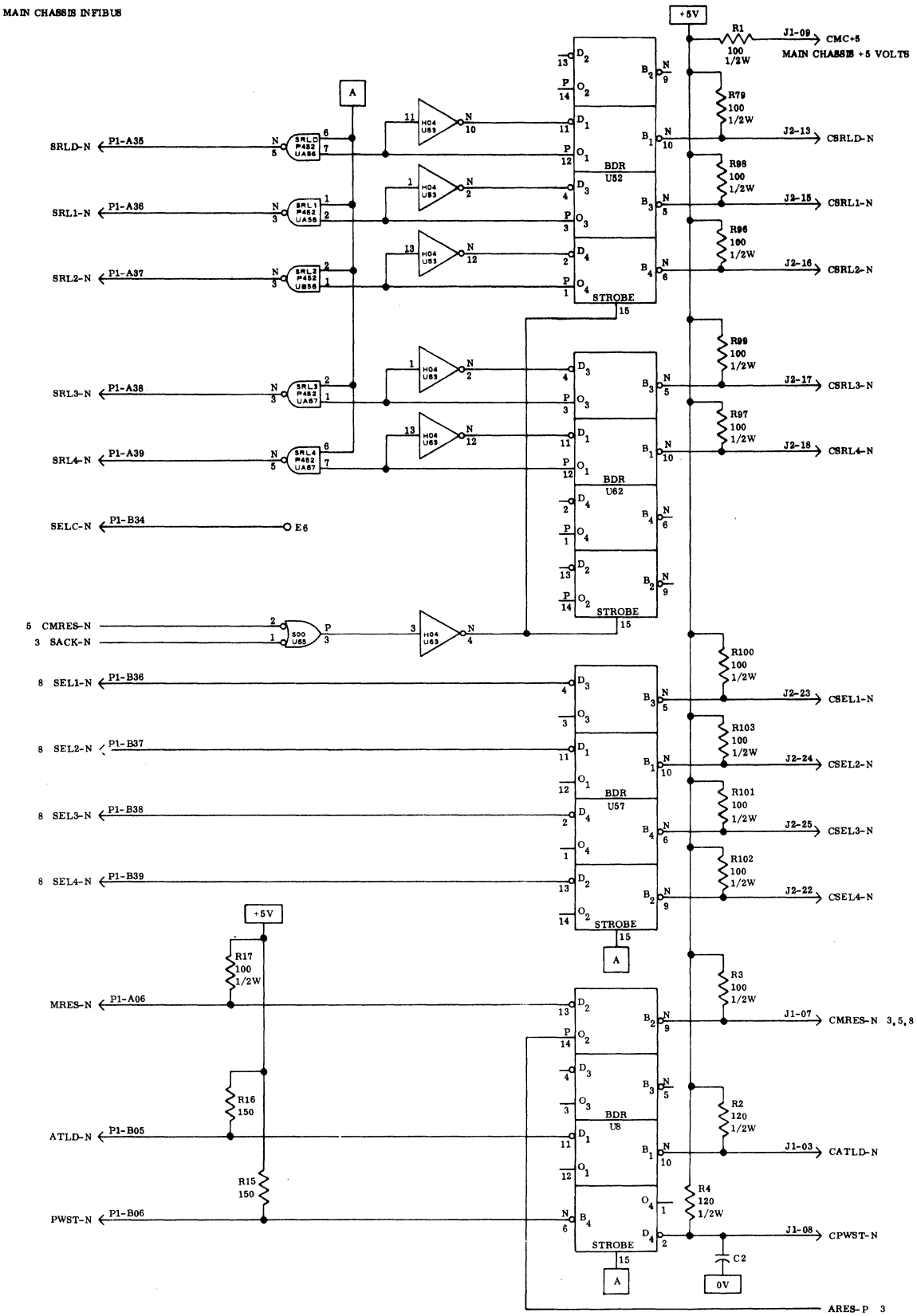
Bus extender lines CSRLD-N, CSRL1-N through CSRL4-N, and CPWST-N are received by the BXD and driven by the BXR. The service request lines contain inverters on the output (D) pin of each bus driver/receiver that is connected back to the driver (D) input to implement a latch. The latches are enabled in the BXD until Select Acknowledge (SACK-N) is asserted, or the system is reset (CMRES-N). Power status does not contain a latch but is driven directly through the BXD.

EXTENDER LINES FROM BXD TO BXR

The lines shown on LD sheet 5 other than the service request lines described above are driven by the BXD and received by the BXR. Their bus drivers/receivers are always enabled.

KEY SOURCE LOGIC DEFINITIONS

CSEL1-N thru CSEL4-N	Lines to carry select signals from the bus controller, in response to a service request, to select the highest precedence requesting modules.
CATLD-N	Extender line to carry autoload signal from the BXD to the auxiliary chassis.
CMRES-N	Cable driver to send master reset from the BXD to BXR.
CPWST-N	Bus driver to place power status received from the BXR onto the main chassis INFIBUS.
CSRLD-N, CSRL1-N thru CSRL4-N	Service request lines which are latched in the BXD until a requesting system module is selected or indicated by select acknowledge (SACK-N).
CMC+5	Positive pull up to +5v transmitted from the main INFIBUS, through the BXD to the BXR.



BXD
BXR

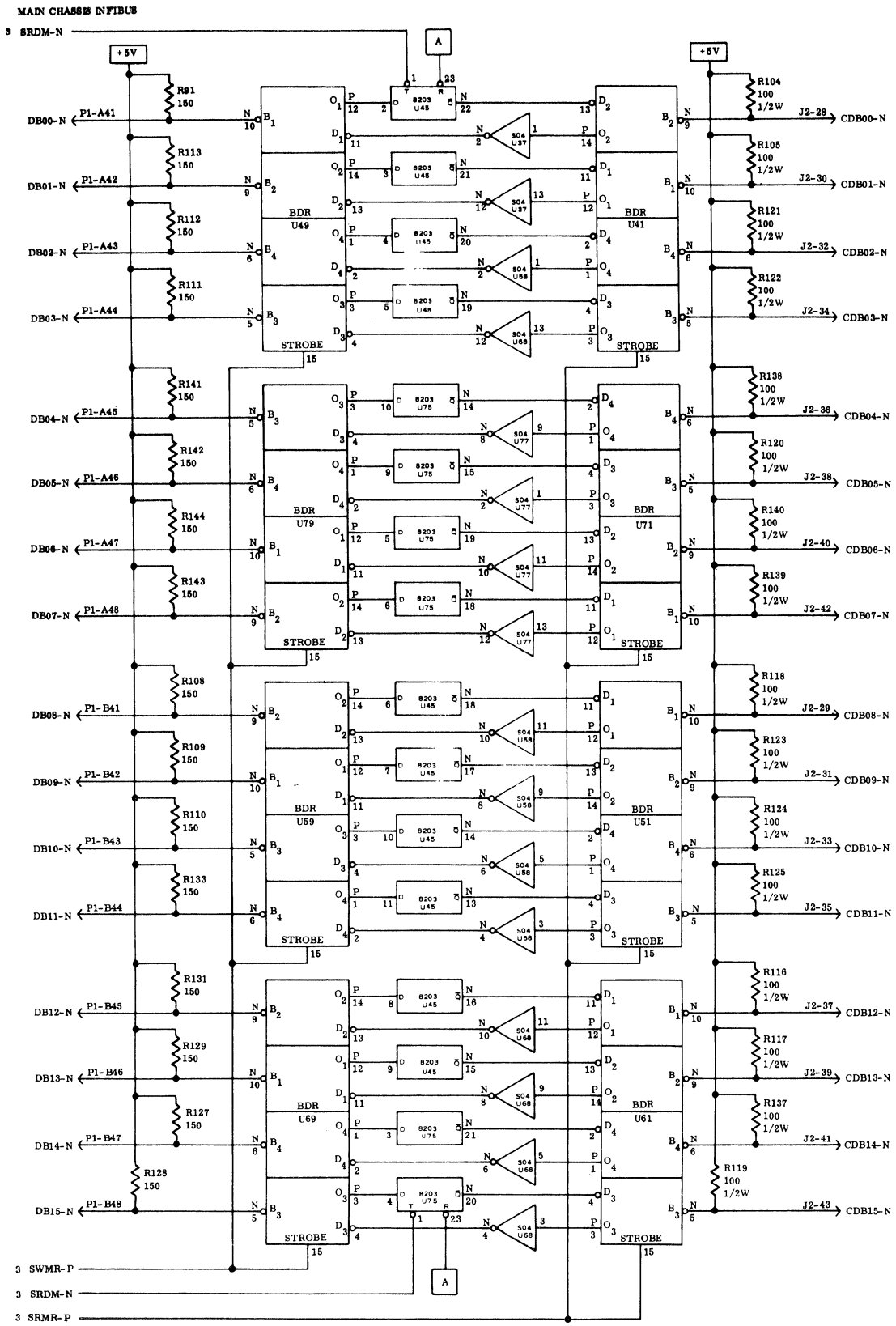
SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 5 of 8

DATA LATCHES, BUS AND CABLE DRIVERS/RECEIVERS (BXD, LD Sheet 6)

The sixteen data lines are bi-directional. Data latches are interconnected between the cable drivers/receivers and bus drivers/receivers. A similar circuit arrangement is contained on the BXR. The cable drivers are enabled, by SRMR-P, on the circuit card that is transmitting, and the INFIBUS drivers are enabled by SWMR-P on the circuit card receiving the data. For example, the BXR latches and transmits the data in the master write and slave read modes, and the BXD receives the data in the slave write and master read modes, and its INFIBUS drivers are enabled. The cable drivers of the receiving extender are disabled.

KEY SOURCE LOGIC DEFINITIONS

CDB00-N thru CDB15-N	Cable drivers/receivers in the bus extender used to transfer data between the BXD and BXR, the direction depending on the master/slave and read/write modes.



BXD
BXR

SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 6 of 8

ADDRESS LATCHES, BUS AND CABLE DRIVERS/RECEIVERS (BXD, LD Sheet 7)

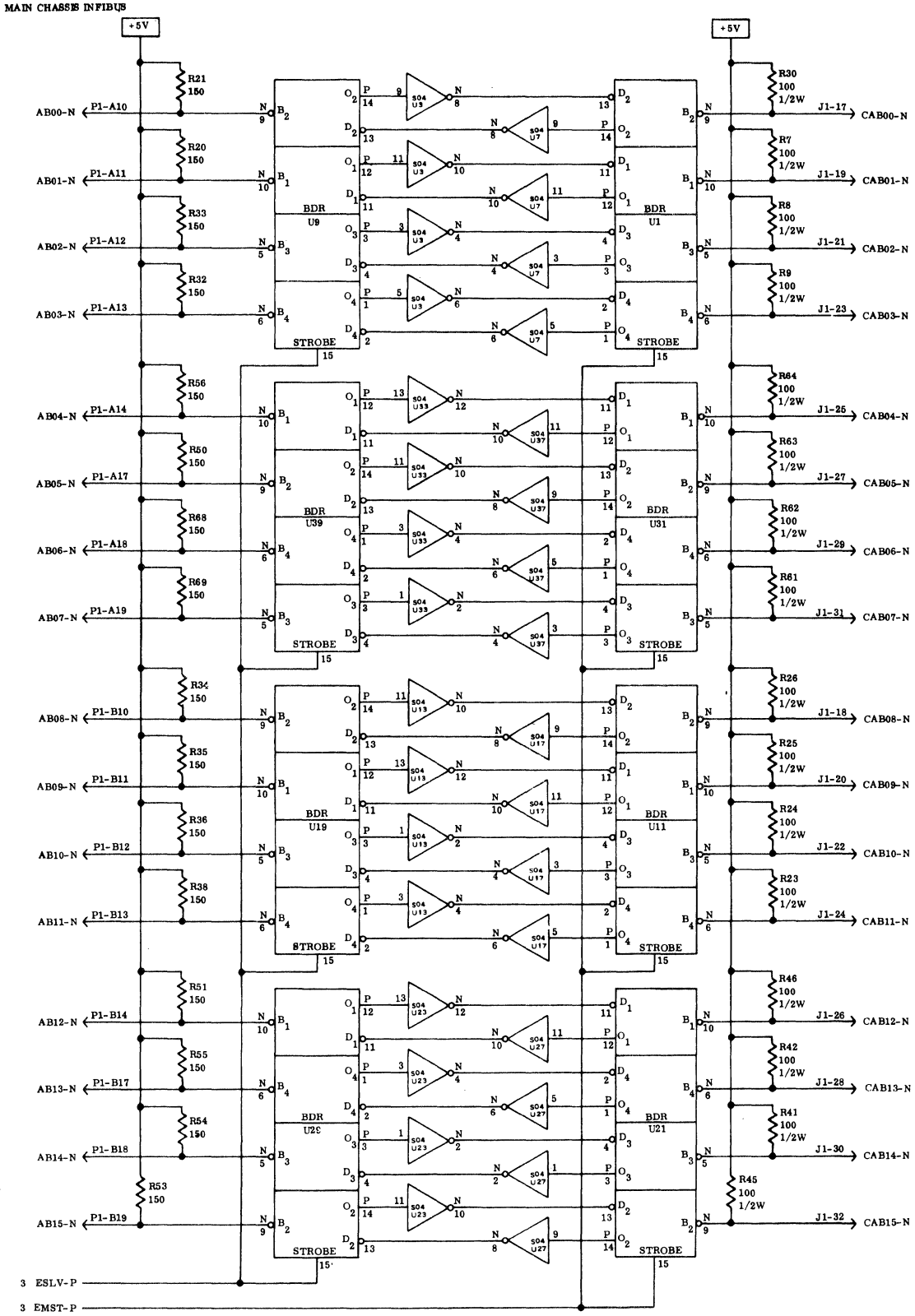
The sixteen address lines are bi-directional. The INFIBUS drivers in the master extender are disabled (ESLV-P negated) and the cable drivers are enabled (EMST-P asserted) to drive the address across the cable to the slave extender. The address is latched in the slave extender and remains latched until strobe (CSTRR-N) is negated.

Other INFIBUS terms transmitted by ESLV-P and EMST-P:

HCYC-N, RITE-N, KEY0-N (ALT.), DONE-N	(Sheet 2)
KEY0-N, KEY1-N, BYTE-N, STRB-N	(Sheet 3)
KEY1-N (ALT.)	(Sheet 8)

KEY SOURCE LOGIC DEFINITIONS

CAB00-N thru CAB15-N	Address cable drivers/receivers used to transfer the address between the BXD and BXR, the direction depending on the master/slave and read/write modes.



BXD
BXR

SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 7 of 8

CONTROL PANEL, POWER FAIL/RESTART, AND SLAVE RITE (BXD, LD Sheet 8)

Cable drivers for control panel signals MINH-N, REPB-N, and EXAT-N are uni-directional, driven by the BXR and received by BXD. RUNN-N is uni-directional driven by the BXD and received by the BXR. These cable drivers are always enabled. Signal KEY1-N (alt.) is bi-directional and transmitted with the address. See address description (BXD, LD Sheet 7).

Power fail/restart lines PRIN-N, PRAL-N, PFIN-N and LFIN-N are interconnected directly by the extender cable without drivers or receivers.

Slave Rite signals CRIT-P and SRIT-P are asserted:

a. when an interrupt is detected causing Rite Simulate flip-flop RTS to set.

b. at the end of a read half cycle when HCYC-N negates during Done time.

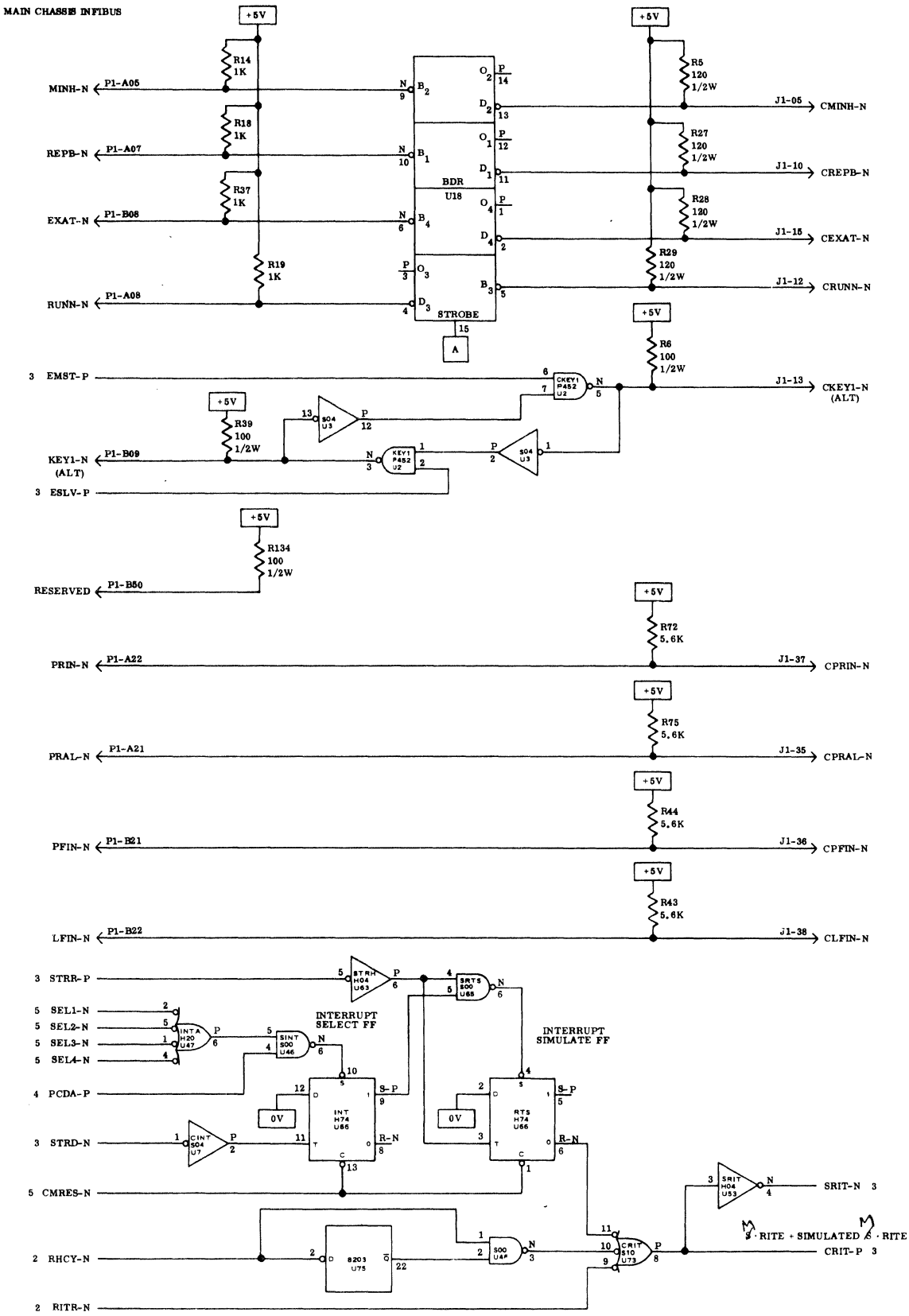
c. when Rite Received signal RITR-N is received from the BXR (master).

The interrupt select flip-flop, INT, monitors the select interrupt lines and precedence pulse. Detecting an interrupt sets flip-flop INT and, consequently, the internal Rite Simulate flip-flop, RTS. As a result, signal CRIT-P enables the slave write signal (SWMR-P Sheet 3) to turn on the data bus driver/receivers for writing the address of the interrupting device placed on the data bus during interrupt.

SRIT-N is asserted at the end of the read half-cycle to disable the data bus driver/receivers. This is accomplished when latch U75 is triggered with the data latches at DONE-N time and the slave half cycle (RHCY-N) negates. When RHCYC-N negates at the end of the read half cycle, SRIT-N (BXD, LD sheet 3) is asserted which disables slave read signal SRMR-P, disabling the data bus drivers/receivers.

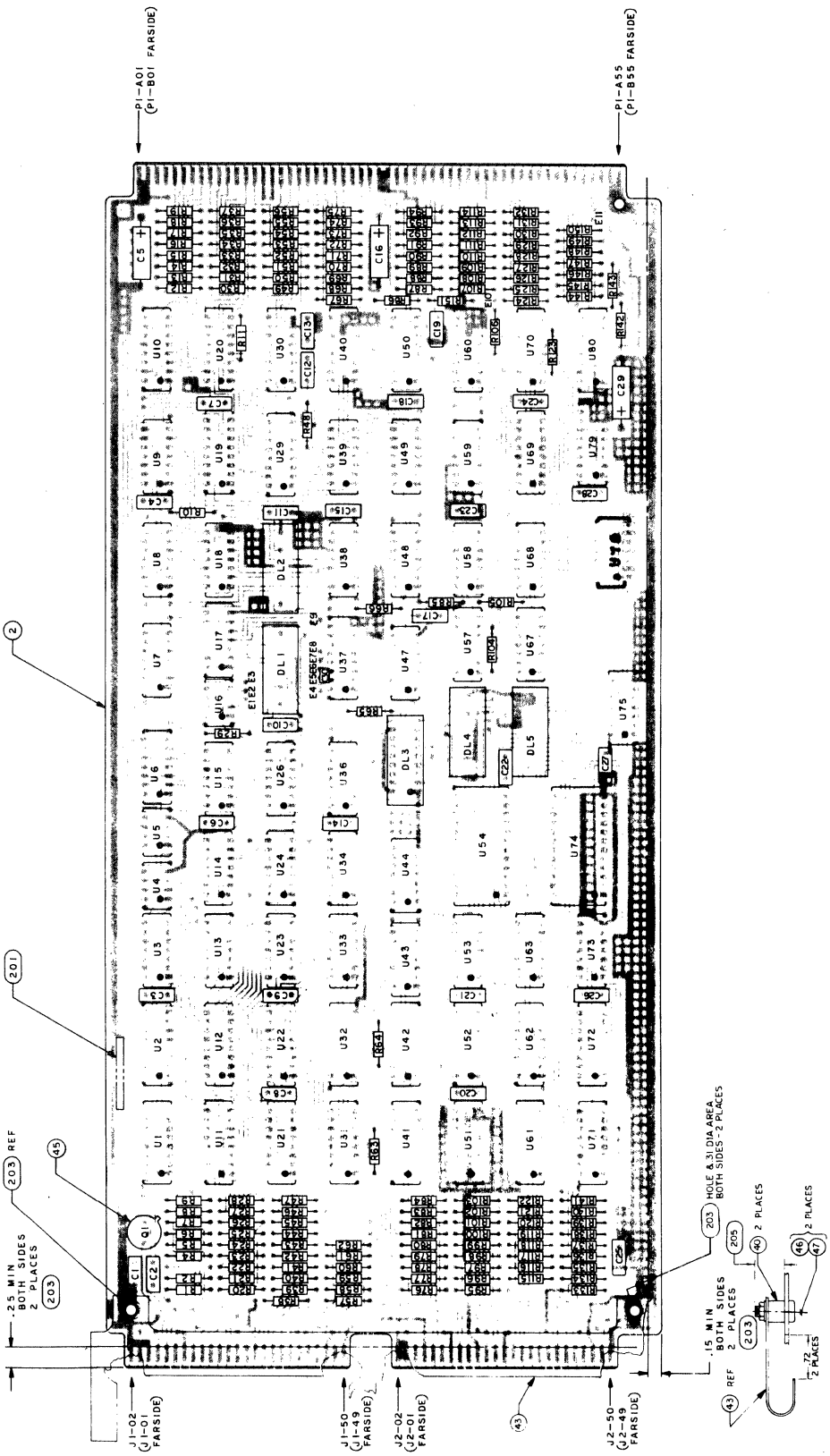
KEY SOURCE LOGIC DEFINITIONS

CMINH-N, CREPB-N CEXAT-N	Bus drivers for Master Interrupt Inhibit, Reset Push Button, and External Attention, all originating in the system control panel and which are driven by the BXR and received by the BXD. These bus drivers are always enabled.
CRUNN-N	Cable driver for RUNN-N signal generated by all processors to light the halt or idle indicators on the system control panel.
CPRIN-N, CPRAL-N, CPFIN-N, CLFIN-N	Power Fail/Restart and Line Frequency lines extended through the BXD and BXR with no drivers or receivers.
CRIT-P	Enables Slave Rite when RITR-N is received from the BXR, or simulated Slave Rite mode when a selected interrupt is sensed.
SRIT-N	Disables Slave Read mode at the end of the read half cycle, or during Write mode.



SUE 1828 Bus Extender Driver BXD, Logic Diagram
LD2001002275-1, Rev. A, Sheet 8 of 8

BXD
BXR



SUE 1829 Bus Extender Receiver BXR, Circuit Card Assembly 2001002276-1, Rev. A, Sheet 1

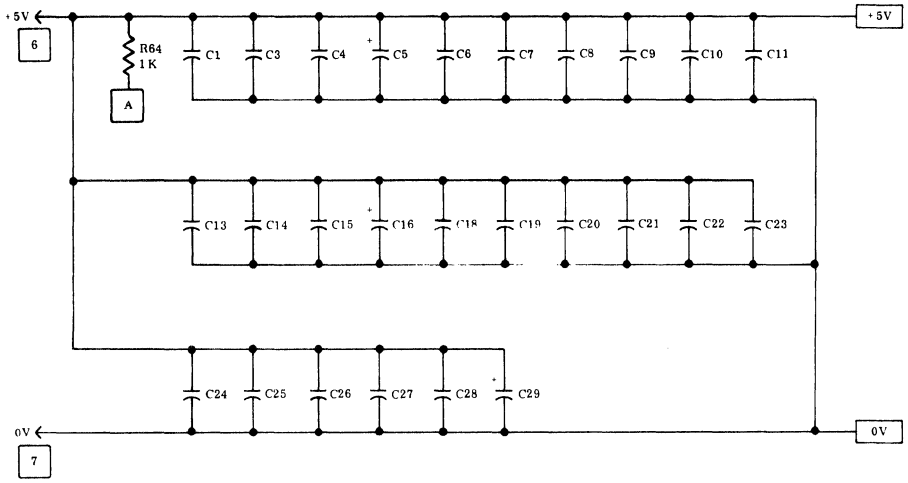
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1μf, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33μf, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATORS ARE ABBREVIATED. FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V, EXCEPT H103, PIN 4 +5V, PIN 11 0V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR, PIN 7 AND 8 0V, PIN 16 +5V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V.

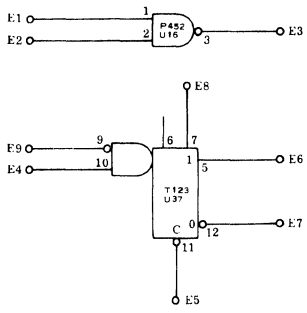
[6] +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51.

[7] 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J1-1, 2, 4, 6, 11, 14, 39, 41, 46, 47, 49, 50; J2-1, 2, 4, 8, 11, 14, 19, 20, 26, 27, 46, 47, 49, 50.

8. -15V CONNECTOR PINS ARE: P1-A52, A53, B52, B53.
9. +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4.



SPARE GATES



BXD
BXR

SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 1 of 8

READ/WRITE CONTROL AND DONE LOGIC (BXR, LD Sheet 2)

With master flip-flop MASS-P (BXR, LD sheet 3) set, and HCYC-N asserted on the auxiliary INFIBUS, Half-Cycle signal CHCYD-N is driven across the cable, and Read/Modify/Write flip-flop is set during the read half-cycle. When DONE-N is received from the Slave Controller, HCYC-N is negated and defines the end of the read half cycle. After the modify portion of the cycle, the write half-cycle starts when RITE-N, address, and new data are asserted by the the master controller. Address lines remain latched during the entire half-cycle mode in the slave bus extender until STRB-N is negated. During the write half-cycle, the master bus extender allows for an inherent 75-nanosecond skew. This skew occurs between the data enable cable driver lines, delay line, and associated gates RITC, RITB, and SRMR and the write cable driver CRITN-N, the same delay line, and RITD gates.

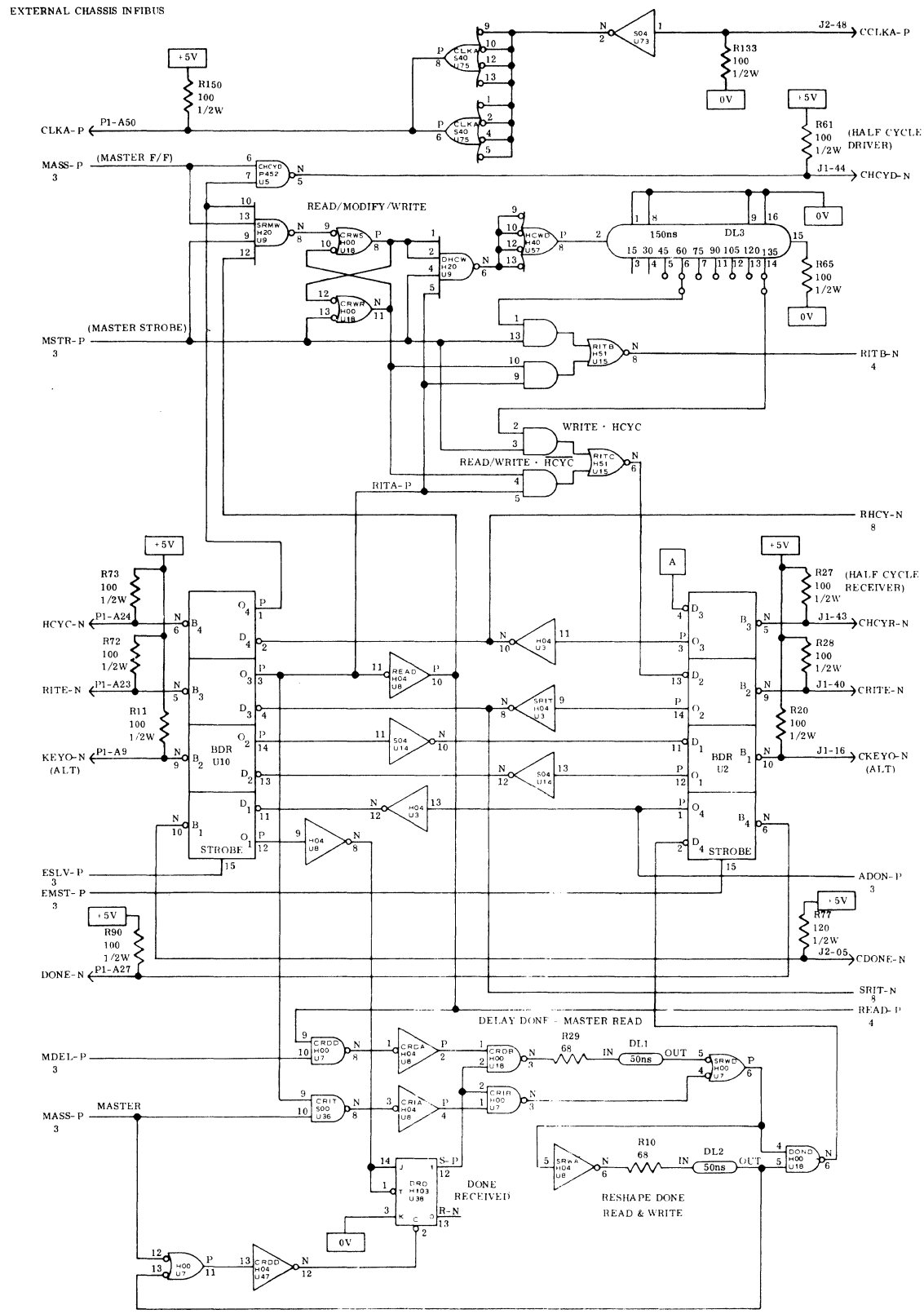
DONE LOGIC

In the master read mode, after master flip-flop MASS is set, MDEL-P (BXR LD sheet 3) enables the DONE logic when the master extender receives CDONE-N from the slave extender and Done-Received flip-flop (DRD) is set. The received Done is delayed 50 nanoseconds to allow for the data received to be stable at the receiver of the master controller before its receipt of DONE-N. Done-Received is cleared 120 nanoseconds after it has been set. DONE-N is reshaped to 50 ± 10 nanoseconds before being asserted on the master chassis INFIBUS.

In the write mode, gates CRIT and CRIB in the DONE logic are enabled and no delay in DONE-N occurs. However, DONE-N is reshaped, and the Done-Received flip-flop is cleared 60 nanoseconds after it has been set. In the slave bus extender, the Done-Received flip-flop (DRD) remains cleared by MASS-P, which is negated.

KEY SOURCE LOGIC DEFINITIONS

ADON-P	Activated with receipt of DONE-N to enable the Slave Read Done term (SRDM-N, BXR sheet 3) which clocks the data register.
CCLKA-P	The 25-MHz clock from the main chassis.
CDONE-N	The cable driver receiver for the DONE pulse generated by the receiving system module. to signal the end of a read or write half cycle.
CHCYD-N	The half-cycle cable driver. HCYC-N is used by the BXR with READ-P to detect the read portion of a read/modify/write cycle.
CHCYR-N	The cable receiver of the half-cycle line received by the BXR during a slave read cycle to become RCHY-N.
CKEY0-N (ALT)	Memory Protect key transmitted with the address. See address description, BXD LD sheet 7.
CRITE-N	The cable RITE-N line that transmits and receives the write mode control signal.
READ-P	Generated when term RITE-N is not asserted on the INFIBUS. Used along with HCYC-P to define the master read mode.
RHCY-N	Received Half-Cycle from the BXD, used in the BXR to disable the data bus drivers receivers at the end of a read half-cycle during slave read mode, through RSSR-P.
RITB-N	Master write derived from RITE-N and used in the BXR to enable SRDM-N which clocks the data register, and SRMR-P which enables the data cable bus drivers receivers.
SRIT-N	Slave write signal received from the BXD to enable the write half cycle. Enables data bus drivers receivers in the BXR (through RSSR-P) during the slave write mode.



SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 2 of 8

BXD
BXR

MASTER/SLAVE CONTROL, AND SELECT ACKNOWLEDGE LOGIC (BXR, LD Sheet 3)

Assertion of STRB-N and the presence of SACK-N at an INFIBUS enables the BXD or BXR on that INFIBUS to function in the master mode by setting Enable Master flip-flop ENM, latching SACK-N for 120 nanoseconds after STRB-N is sensed, and setting master flip-flop MASS. The master flip-flop functions to:

a. Enable, through gate EMST, the cable drivers of address (AB00-N - AB15-N), BYTE-N, RITE-N and HCYC-N, and to enable receipt of DONE via the cable.

b. Disable, through gate ESLV, INFIBUS drivers of STRB-N, Address, BYTE-N, RITE-N and HCYC-N.

c. Enable, through gate SWMR, the data received from the slave bus extender via the cable, which is latched if in Read mode. In Write mode, the data cable drivers are enabled by gate SAMR.

d. Enable Cable Strobe Driver CSTRD, through gate DMST, which, in turn, clears the Enable Master flip-flop (ENM), thus preparing to clear the master flip-flop when STRB-N is negated and to set it again when STRB-N is asserted while SACK-N is present. When STRB-N is negated by a master controller, the bus extender located in the same chassis (master) clears its master flip-flop, and disables all the address, data, byte, RITE and HCYC drivers mentioned in item b. STRB-N is delayed by a 50-nanosecond delay line in the slave bus extender plus gate delays in the master bus extender to ensure that addresses, data and commands are stable before detection of STRB-N at the receiver end of the slave controller.

SELECT ACKNOWLEDGE

Select Acknowledge, CSAK-N, is driven across the cable by the BXR when the auxiliary chassis has been selected by SELx-N. The BXR latches SACK-N if the previous strobe from the auxiliary chassis is negated, therefore, output HAKR-N of the 120-nanosecond one-shot is high. SACK-N remains latched internally in the BXR for 120 nanoseconds beyond assertion of STRB-N by the auxiliary chassis. SACK-N latch is kept asserted on the main chassis for at least 120 nanoseconds after being negated on the auxiliary chassis INFIBUS. Therefore SACK-N is not negated before STRB-N is detected at the main chassis INFIBUS.

The BXD does not latch SACK-N when it originates in the auxiliary chassis. However, to prevent the Bus Control Unit (BCU) from selecting any service request originating in the auxiliary chassis until STRB-N is received there, SACK-N is latched in the BXD and on the main chassis INFIBUS for 120 nanoseconds beyond assertion of STRB-N by the main chassis.

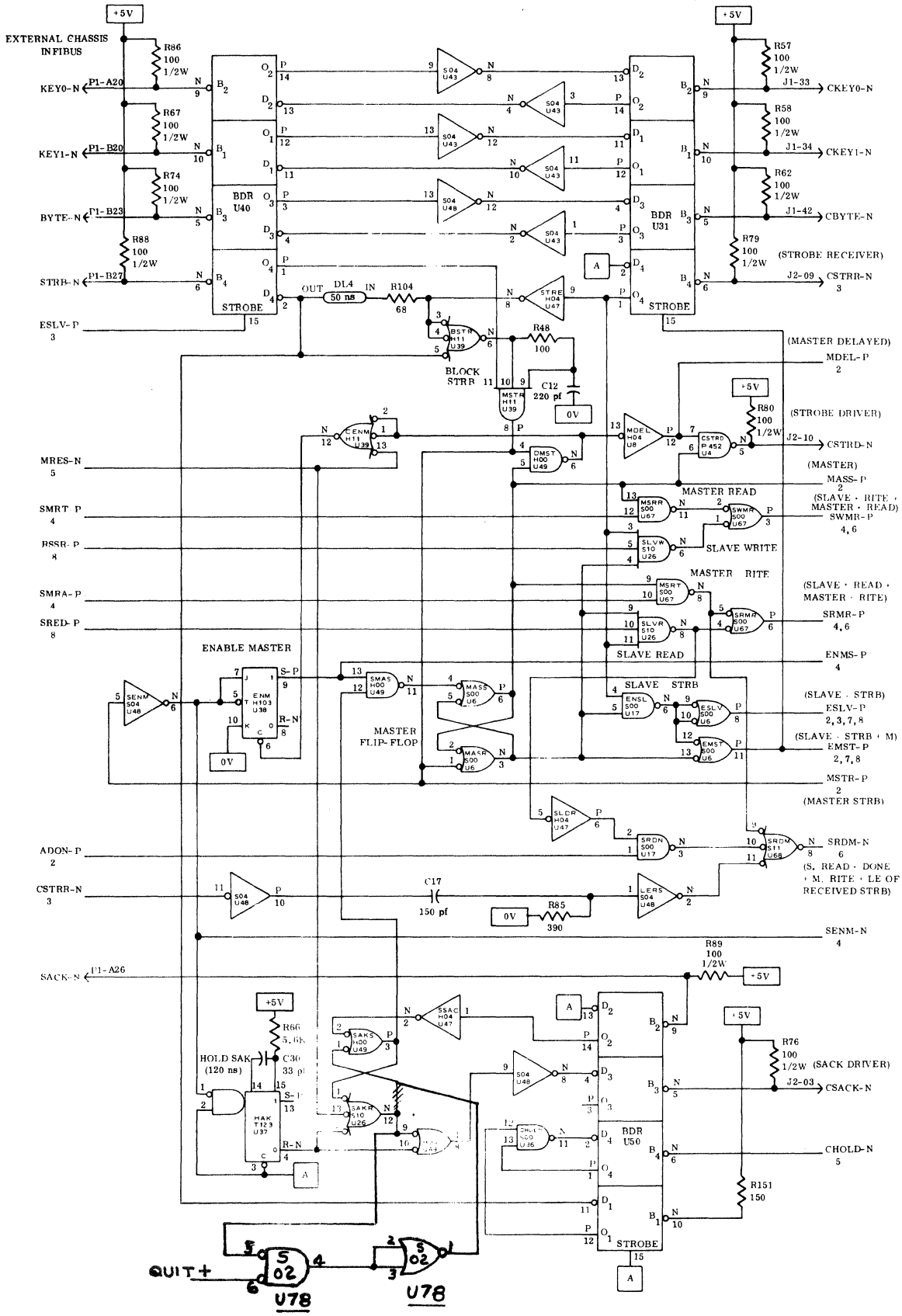
The 4-microsecond one-shot in the BXD functions to reset the SACK latch when a pseudo-SACK is generated by the BCU.

BXD
BXR

MASTER/SLAVE CONTROL, AND SELECT ACKNOWLEDGE (BXR, LD Sheet 3) (continued)

KEY SOURCE LOGIC DEFINITIONS

CBYTE-N, CKEY0-N, CKEY1-N	Cable drivers/receivers of BYTE and KEY bits, the drivers of which are enabled by EMST-P to transmit these bits along with the address. See Address description (BXR LD sheet 7).
CSACK-N	Select acknowledge driver from the auxiliary INFIBUS to the BXD.
CSTRR-N	Received strobe from the BXD which enables the slave mode in the BXR.
CSTRD-N	Strobe cable driver, enabled by the master extender to transmit STRB-N to the slave extender.
EMST-P	Enables the cable bus drivers to transmit address (including KEY bits), RITE-N, BYTE-N, and HCYC-N.
ENMS-P	Triggers the interrupt select flip-flop when Enable Master flip-flop is set.
ESLV-P	Enables the INFIBUS drivers of AB00-N - AB15-N, STRB-N, RITE-N, BYTE-N and HCYC-N in the BXR when a slave. Simultaneously, ESLV-P in the BXD is negated to disable these bus drivers. This signal is always negated in the master and asserted in the slave.
MASS-P	Set in the master extender and reset in the slave, the set output of this flip-flop enables the master read and write modes (through SWMR-P, SRMR-P), the cable drivers for Half-Cycle and Strobe, and the set input to the Read/Modify/Write flip-flop for the read half cycle. At the end of the write Half-cycle, enables the Done reshape logic which reshapes DONE-N received from the slave to be transmitted on the INFIBUS of the master.
MDEL-P	Master Strobe delayed — asserted in the master extender to enable the Done logic at the end of the read half cycle.
MSTR-P	Master strobe asserted in the master extender to enable the master flip-flop and Read/Modify/Write flip-flop. MSTR-P is negated in the slave extender.
SENM-N	Triggers the interrupt simulate flip-flop when Master Strobe, MSTR-P, is generated.
SRDM-N	Clears the data register at leading edge of received strobe. Loads the data register in Master Write mode and at Done time in the slave read mode.
SRMR-P	SRMR-P Slave Read or Master Rite, used together with SWMR-P. In Master Rite, the master extender latches and transmits data to the slave extender. In Slave Read mode, the slave extender latches and transmits the data at the end of DONE-N Read mode, the slave extender latches and transmits the data at DONE-N time. SRMR-P enables the cable drivers and SWMR-P disables the INFIBUS drivers.
STRR-P	Strobe received from the BXD. The trailing edge (strobe negated) clears Rite Simulated flip-flop RTS.
SWMR-P	Slave Write or Master Read, used together with SRMR-P. SWMR enables data INFIBUS drivers and SRMR-P (negated) disables data cable drivers.



SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 3 of 8

BXD
BXR

MASTER READ/RITE, PRECEDENCE PULSE, DATA, AND QUIT (BXR, LD Sheet 4)

Master Read signal SMRT-P is asserted to enable the master read mode if no interrupt select line is active.

Master Rite signal SMRA-P is asserted when an interrupt is detected, setting Rite Simulate flip-flop RTS, or when Rite signal RITB-N is asserted, and the BXR is the master.

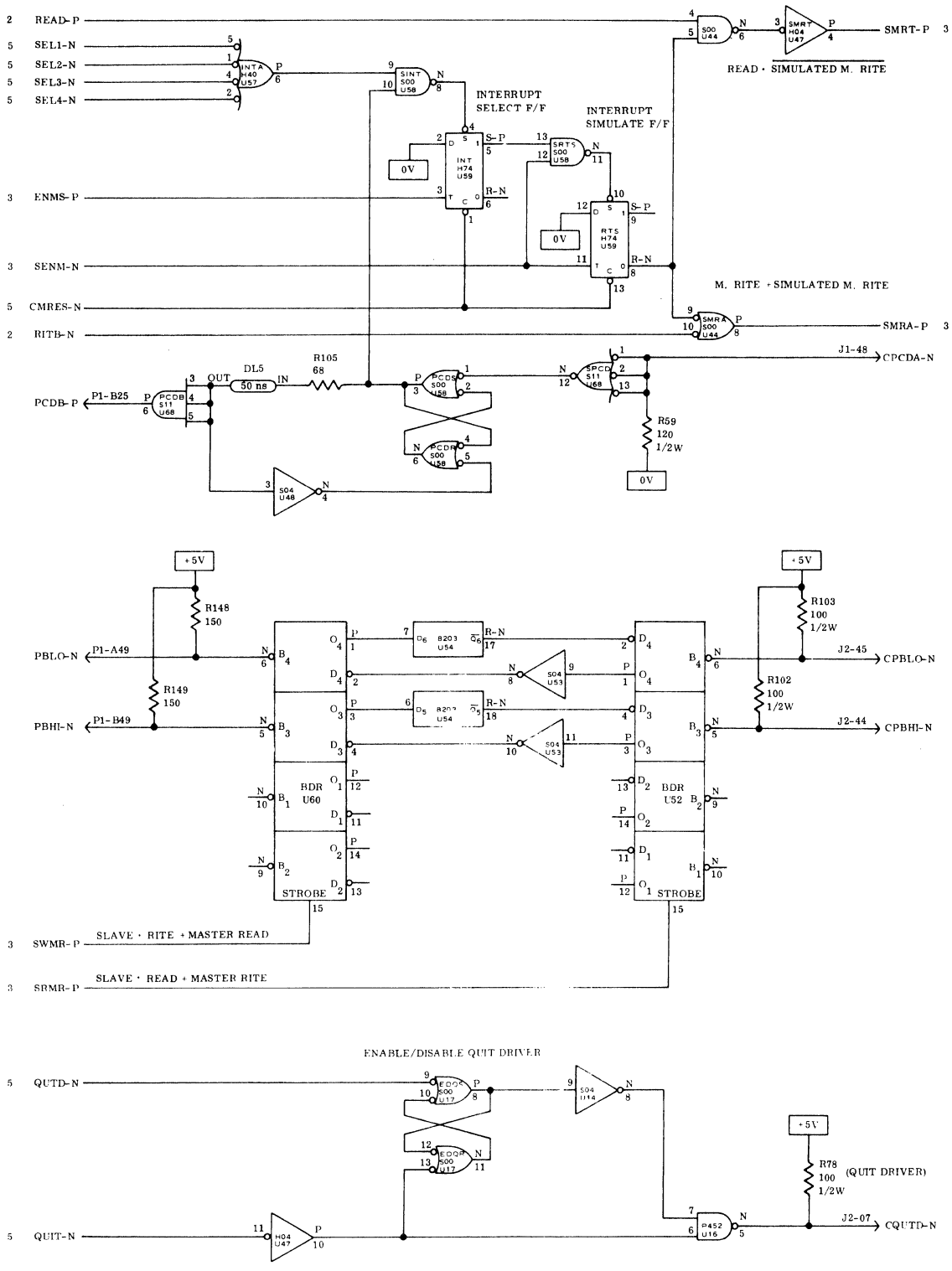
The Interrupt Select flip-flop, INT, monitors the select interrupt lines and precedence pulse. Detecting an interrupt sets flip-flop INT which, in turn, sets the internal Rite Simulate flip-flop, RTS. As a result, signal SMRA-P enables the master write signal (SRMR-P sheet 3) to turn on the data bus driver/receivers for writing the address of the interrupting device placed on the data bus during interrupt.

Data bits CPBLO-N and CPBHI-N are bi-directional and are driven along with data bits CDB00-N through CDB15-N. The BXR receives the data in the Master Read or Slave Rite mode at which time signal SWMR-P enables the bus drivers. This cable drivers are disabled by SRMR-P. In Master Rite or Slave Read mode the BXR latches the data from the auxiliary INFIBUS and transmits it to the BXD. The BXD bus drivers are enabled and its cable drivers are disabled at that time.

The Quit logic consists of a cable driver, CQUTD-N, enabled or disabled cable receive signal QUTD-N. The Quit driver is normally enabled to drive QUIT-N from the auxiliary chassis INFIBUS. A Quit signal received from the BXD, disables the Quit Driver.

KEY SOURCE LOGIC DEFINITIONS

CPCDA-N, PCDB-P	Precedence chain receiver/driver which places the precedence pulse on the auxiliary chassis. CPCDA-N is delayed 50 nanoseconds and reshaped to 50 ± 10 nanoseconds by the BXR before transmission onto the auxiliary chassis as PCDB-P.
CPBLO-N, CPBHI-N	Data bits transferred along with CDB00-N through CDB15-N to carry parity status for right and left bytes, respectively.
CQUTD-N	The Quit driver is disabled if the source of Quit is from the main chassis through CQUTR-N (LD sheet 5). If the source is from the auxiliary INFIBUS, the driver is enabled.
SMRT-P, SMRA-P	SMRT-P asserted, enables the Master Read mode if no interrupt select line is active. SMRA-P enables the Master Write mode during an interrupt and during a Write cycle.



BXD
BXR

SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 4 of 8

SERVICE REQUEST AND SELECT LINES (BXR, LD Sheet 5)

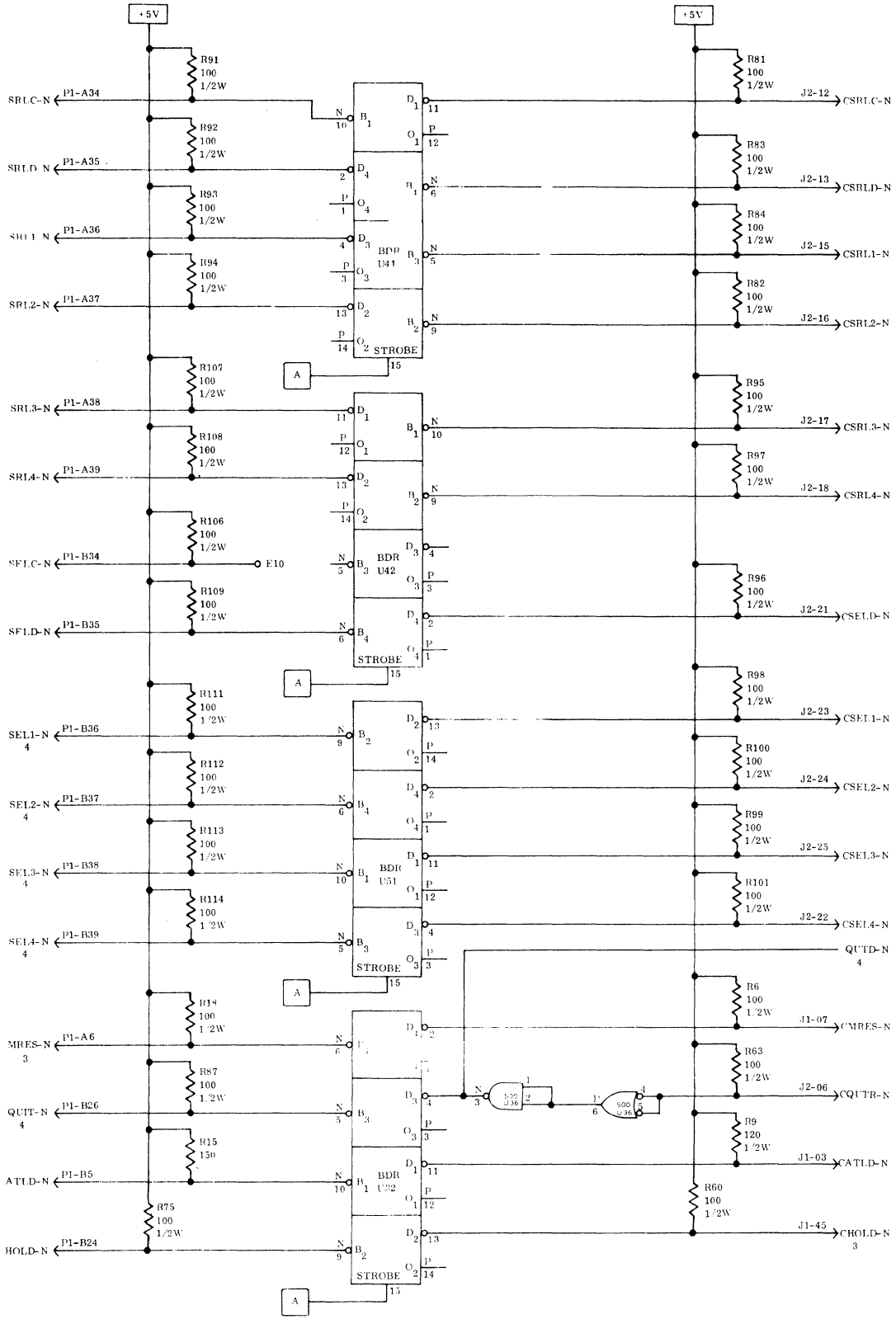
Bus extender lines CSRLD-N, and CSRL1-N through CSRL4-N are driven by the BXR and received by the BXD where thay are latched. The latches are enabled in the BXD until Select Acknowledge (SACK-N) is asserted, or the system is reset (CMRES-N).

EXTENDER LINES FROM BXR to BXD

The extender lines shown on BXR, LD sheet 5, other than the service request lines described above, are received by the BXD and driven by the BXR. Their bus drivers/receivers are always enabled.

KEY SOURCE LOGIC DEFINITIONS

CSELD-N, CSEL1-N thru CSEL4-N	Lines to carry select signals from the bus controller, in response to a service request, to select the highest precedence requesting modules. Received in the BXD and driven by the BXR.
CATLD-N	Extender line to receive the autoload signal in the BXR and drive it onto the auxiliary INFIBUS.
CMRES-N	Bus driver to receive master reset from the BXD and drive it onto the auxiliary INFIBUS.
CSRLC-N CHOLD-N	Bus drivers for the Service Request Computer and Hold signals, respectively, received in the BXR from the BXD and driven onto the auxiliary INFIBUS. These drivers are always enabled.
CSRLD-N, CSRL1-N thru CSRL4-N	Service request lines driven by the BXR and received by the BXD. They are latched in the BXD until a requesting system module is selected as indicated by Select Acknowledge.
CQUTR-N, QUTD-N	The QUIT receiver and bus driver.



SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 5 of 8

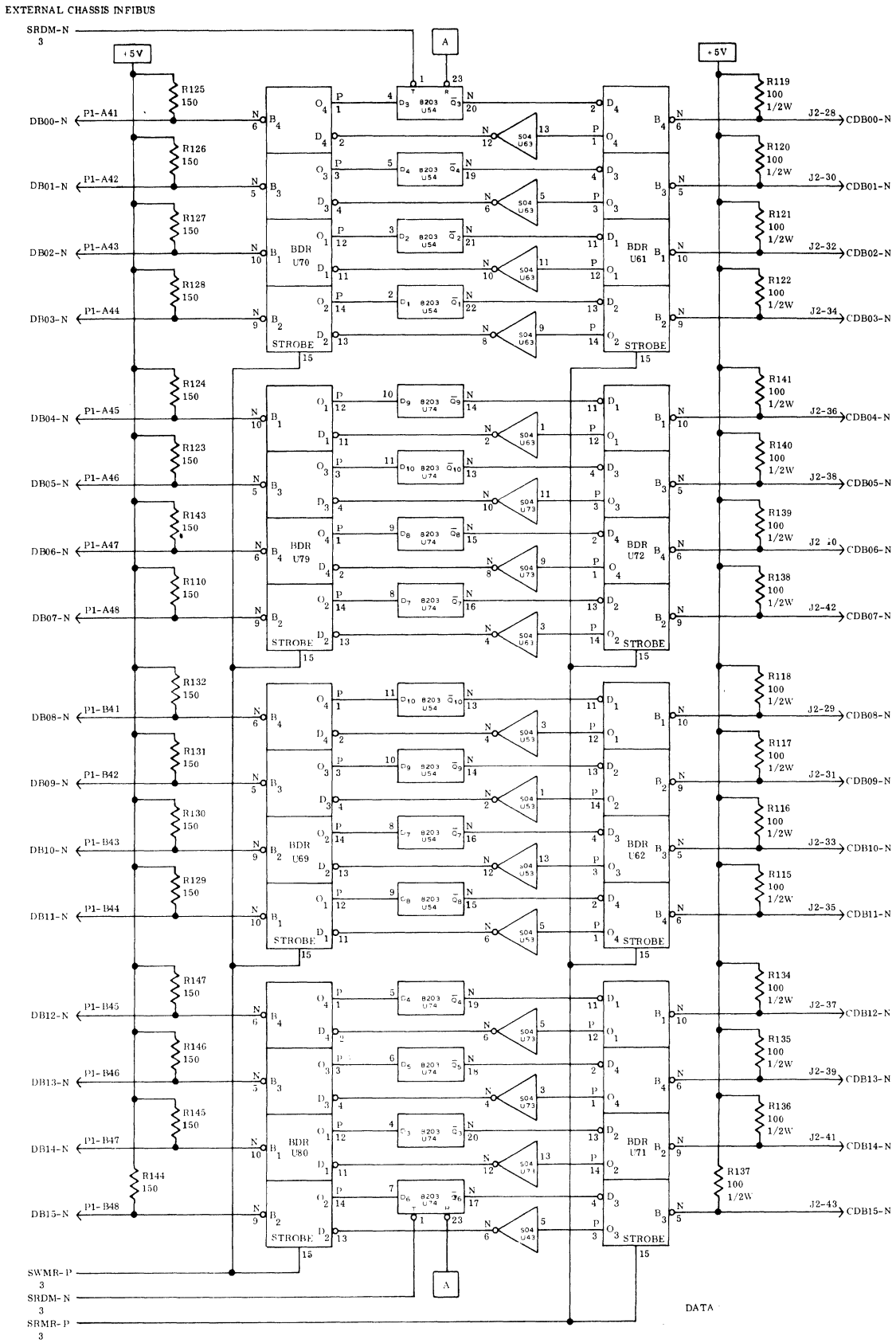
BXD
BXR

DATA LATCHES, BUS AND CABLE DRIVERS/RECEIVERS (BXR, LD Sheet 6)

The sixteen data lines are bi-directional. Data latches are interconnected between the cable drivers/receivers and bus drivers/receivers. A similar circuit arrangement is contained on the BXD. The cable drivers are enabled, by SRMR-P, on the circuit card that is transmitting, and the INFIBUS drivers are enabled by SWMR-P on the circuit card receiving the data. For example, the BXR latches and transmits the data in the master write and slave read modes, and the BXD receives the data in the slave write and master read modes, and its INFIBUS drivers are enabled. The cable drivers of the receiving extender are disabled.

KEY SOURCE LOGIC DEFINITIONS

CDB00-N thru CDB15-N	Cable drivers/receivers in the bus extender used to transfer data between the BXD and BXR, the direction depending on the master/slave and read/write modes.



BXD
BXR

SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 6 of 8

ADDRESS LATCHES, BUS AND CABLE DRIVERS/RECEIVERS (BXR, LD Sheet 7)

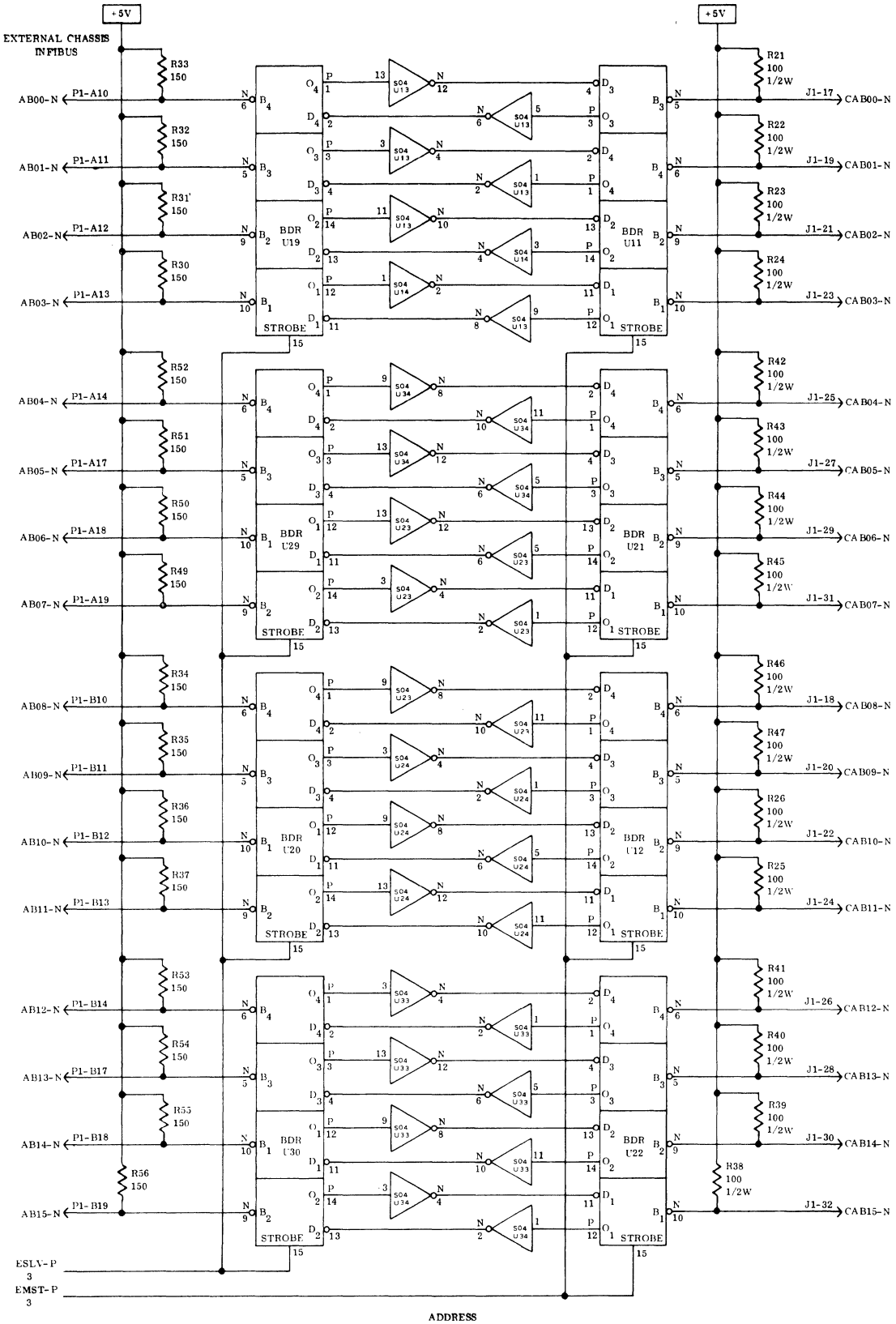
The sixteen address lines are bi-directional. The INFIBUS receivers in the master extender are disabled (ESLV-P negated) and the cable drivers are enabled (EMST-P asserted) to drive the address across the cable to the slave extender. The address is latched in the slave extender and remains latched until strobe (CSTRB-N) is negated.

Other INFIBUS terms transmitted by ESLV-P and EMST-P:

HCYC-N, RITE-N, KEY0-N (ALT.), DONE-N	(Sheet 2)
KEY0-N, KEY1-N, BYTE-N, STRB-N	(Sheet 3)
KEY1-N (ALT.)	(Sheet 8)

KEY SOURCE LOGIC DEFINITIONS

CAB00-N thru CAB15-N	Address cable drivers/receivers used to transfer the address between the BXD and BXR, the direction depending on the master/slave and read/write modes.



BXD
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SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 7 of 8

CONTROL PANEL, POWER FAIL/RESTART AND STATUS, AND SLAVE READ/RITE (BXR, LD Sheet 8)
Cable drivers for control panel signals MINH-N, REPB-N, and EXAT-N are uni-directional, driven by the BXR and received by BXD. RUNN-N is uni-directional driven by the BXD and received by the BXR. These cable drivers are always enabled. Signal KEY1-N (alt.) is bi-directional and transmitted with the address. See address description (BXR, LD sheet 7).

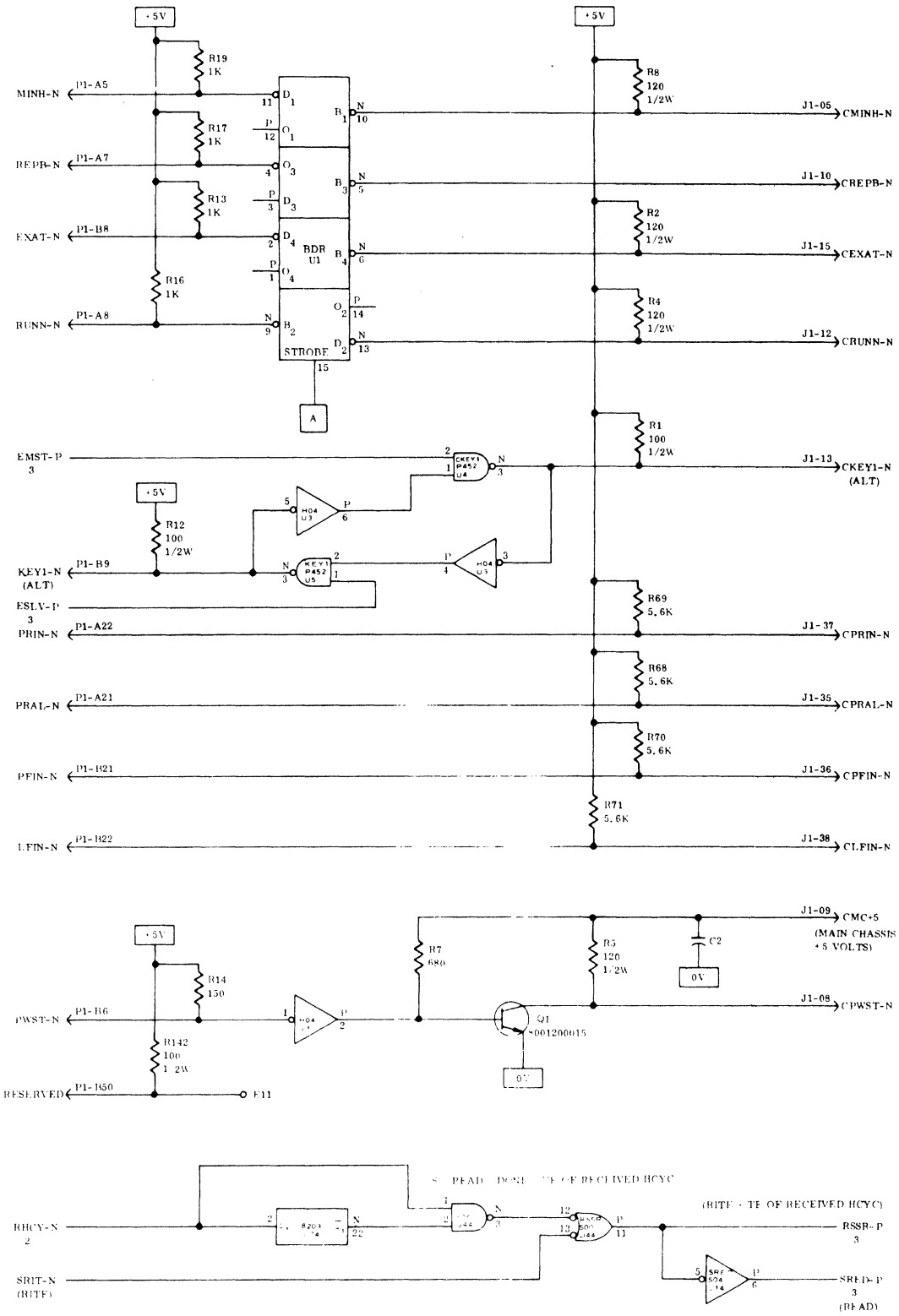
Power fail/restart lines PRIN-N, PRAL-N, PFIN-N and LFIN-N are interconnected directly by the extender cable without drivers or receivers. Power status is sent from the auxiliary chassis to the bus controller through CPWST-N. Normally this signal is negated when power is present, and asserted about 2.2 to 3 milliseconds before loss of regulation due to power failure.

Signals SRED-P and RSSR-P enable the slave read and write modes, respectively. SRED-P enables the data register clock and cable driver enabling signal during slave read mode. At end of the read half cycle, SRED-P negates to disable the data cable drivers. RSSR-P enables the data bus drivers (through SWMR-P) to drive the data onto the auxiliary INFIBUS during the slave write mode.

KEY SOURCE LOGIC DEFINITIONS

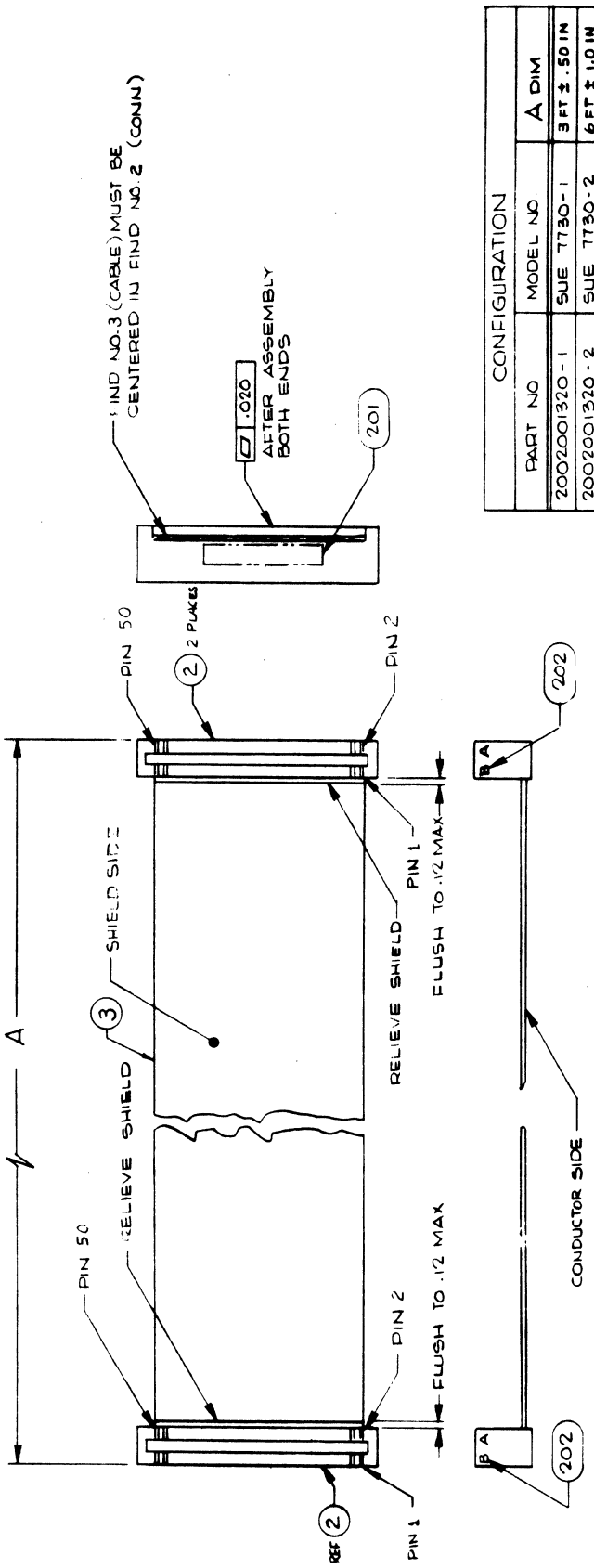
CMINH-N, CREPB-N CEXAT-N	Bus drivers for Master Interrupt Inhibit, Reset Push Button, and External Attention, all originating in the system control panel and which are driven by the BXR and received by the BXD. These bus drivers are always enabled.
CRUNN-N	Cable driver for RUNN-N signal generated by all processors to light the halt and idle indicators on the system control panel.
CMC+5	Positive 5-volts transmitted through the extender cable from the main chassis.
CPRIN-N, CPRAL-N, CPFIN-N, CLFIN-N	Power Fail/Restart and Line Frequency lines extended through the BXD and BXR with no drivers or receivers.
CPWST-N	Power status cable line from the auxiliary chassis used to transmit the power status indication to the bus controller.
RSSR-P	Enables the data bus driver/receivers through SWMR-P during the slave write mode and at the end of the Read portion of the Read/Modify/Write cycle.
SRED-P	Enables data cable drivers through SRMR-P and data register clock SRDM-N during slave read mode.

EXTERNAL CHASSIS INFIBUS



SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 8 of 8

BXD
BXR



SUE 7730-1, -2, -3 Cable Assembly
2002001320, Rev. A, Sheet 1

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002275-1		BXD-CKT CARD ASSY		USED ON SUE 1828	1
002		001	0001		1001005193-1		PRINTED WRG BD, BXD			2
003		001	0001		8001300006-1		CAPACITOR		C37 .1 IS	3
004	F	030	0001		8001300101-1		CAPACITOR		C1,2,3,5,7,C9 THRU C27,C29,30, 32,33,34,35 .25 IS	4
005		002	0001		8001300311-2		CAPACITOR		C6,31 .8 IS	5
006		002	0001		8001300202-59		CAPACITOR		C8,36 .25 IS	6
007		001	0001		8001300202-67		CAPACITOR		C4 .25 IS	7
008		001	0001		8001300070-1		CAPACITOR		C28 .25 IS	8
009		003	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R12,31,48 .5 IS	9
010		001	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R13 .5 IS	10
011		036	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R15,16,20,21,R32 THRU R36,R38,50, 51,53,54,55,56, 68,69,91,R108 THRU R113,R127, 128,129,131,133, R141 THRU R146 .5 IS	11
012		002	0001		RL07S391G		RESISTOR	MIL-R-22684/1	R11,149 .5 IS	12
013		005	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R14,18,19,37,126 .5 IS	13
014		005	0001		RL07S562G		RESISTOR	MIL-R-22684/1	R43,44,72,75,106 .5 IS	14
015		000								15
016	B	077	0001		TYPE RG1/4-100	11502	RESISTOR	IRC, INC	R1,3,R6 THRU R10,R17,R22 THRU R26,R30,R39 THRU R42,R45,46,47, 49,52,57,58,R60 THRU R67,R70,71, 73,74,R76 THRU R85,R88,90,R96 THRU R105,R116 THRU R125,R134 THRU R140,R147 .5 IS RG1/4-100 OHMS 5 PCT	16
017	B	007	0001		TYPE RG1/4-120	11502	RESISTOR	IRC, INC	R2,4,5,27,28,29, 59 .5 IS RG1/4-120 OHMS 5 PCT	17
018		001	0001		RL07S1836		RESISTOR	MIL-R-22684/1	R148 .5 IS	18
019	F	002	0001		8001800042-1		ICP		U24,26 (74H00)	19
020	F	005	0001		8001800044-1		ICP		U34,36,44,53,63 (74H04)	20
021	F	001	0001		8001800048-1		ICP		U47 (74H20)	21
022	F	001	0001		8001800052-1		ICP		U43 (74H40)	22
023	F	001	0001		8001800054-1		ICP		U14 (74H51)	23
024	F	001	0001		8001800069-1		ICP		U35 (74H103)	24

BXD
BXR

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
025		029	0001		8001800123-1		ICP		U1,8,9,11,18,19,21,22,28,29,31,32,38,39,41,42,48,49,51,52,57,59,61,62,69,71,72,78,79 (BDR)	25
026	F	001	0001		8001803121-1		ICP		U66 (74H74)	26
027	F	006	0001		8001803198-1		ICP		U4,16,46,54,65,74 (74S00)	27
028	F	011	0001		8001803200-1		ICP		U3,7,13,17,23,27,33,37,58,68,77 (74S04)	28
029	F	001	0001		8001803202-1		ICP		U73 (74S10)	29
030	F	001	0001		8001803203-1		ICP		U6 (74S11)	30
031	F	001	0001		8001803220-1		ICP		U76 (74S140)	31
032		002	0001		9223-SS-115-7	06540	SPACER	AMATOM		32
033		005	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U2.UA56,UB56,UA67,UB67	33
034		001	0001		8001803155-1		ICP		U64 (74123)	34
035		002	0001		N8203N	18324	ICP	SIGNETICS	U45,75	35
036		001	0001		8001800046-1		ICP		U55 (74H10)	36
037	F	001	0001		8001600007-1		DELAY LINE, TAPPED		DL2	37
038	F	003	0001		8001600008-1		DELAY LINE, FIXED		DL1,3,4	38
		001	0001		1001005412-1		RETAINER, I/O CONN			39
040		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		40
041		REF	0001		LD2001002275-1		LOGIC DIAGRAM			41
042		002	0001		MS51957-16	96906	SCREW, MACHINE		4-40 X 7/16 LG	42
043		002	0001		9002100000-1		NUT, LOCK WASHER		4-40	43

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARKING (IDENTIFY).			201
202		REF	0001				AREA TO BE FREE OF SOLDER.			202
203		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			203
204		REF	0001				COMPONENT HEIGHT .395 MAX.			204
205		REF	0001				PROTRUSION SIDE 2 .075 MAX. LEADS TO BE VISIBLE THRU SOLDER.			205
206		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010 INCH/INCH IN GENERAL AREA AND .005 INCH/INCH IN CONNECTOR AREA.			206
207		REF	0001				SQUARE PAD DENOTES CATHODE END (STRIPE) OF DIODE, OR POSITIVE (+) END OF CAPACITOR.			207
208		REF	0001				RECTANGULAR PAD AND DOT OR SLOTTED END OF ICP DENOTES PIN 1.			208
209		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			209
210		A/R	0001		LECP1075		HARDWARE.			210
211		000								211
212		000								212

BXD
BXR

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002276-1		BXR-CKT CARD ASSY		SUE 1829	1
002		001	0001		1001005203-1		PRINTED WRG BD, BXR			2
003		003	0001		8001300311-2		CAPACITOR		C5,16,29 .8 IS	3
004		024	0001		8001300101-1		CAPACITOR		C1,2,3,4,C6 THRU C11,C13,14,15, C18 THRU C28 .25 IS	4
005		001	0001		8001300202-67		CAPACITOR		C12 .25 IS	5
006		001	0001		8001300202-59		CAPACITOR		C17 .25 IS	6
007		001	0001		8001300006-1		CAPACITOR		C30 .1 IS	7
008		004	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R10,29,104,105 .5 IS	8
009		001	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R48 .5 IS	9
010		037	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R14,15,R30 THRU R37,R49 THRU R56,R110,R123 THRU R132,R143 THRU R149,R151 .5 IS	10
011		001	0001		RL07S391G		RESISTOR	MIL-R-22684/1	R85 .5 IS	11
012		001	0001		RL07S681G		RESISTOR	MIL-R-22684/1	R7 .5 IS	12
013		005	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R13,16,17,19,64 .5 IS	13
014		005	0001		RL07S562G		RESISTOR	MIL-R-22684/1	R66,R68 THRU R71 .5 IS	14
		000								15
016		000								16
017		000								17
018	B	089	0001		TYPE RG1/4	11502	RESISTOR	IRC, INC	R1,6,11,12,18, R20 THRU R28, R38 THRU R47, R57,58,R60 THRU R63,R65,67,R72 THRU R76,R78 THRU R84.R86 THRU R103,R106 THRU R109,R111 THRU R122,R133 THRU R142,R150 .5 IS RG1/4 100 OHMS 5 PCT.	18
019	B	007	0001		TYPE RG1/4	11502	RESISTOR	IRC, INC	R2,4,5,8,9, 59,77 .5 IS RG1/4 120 OHMS 5 PCT.	19
020		000								20
021		003	0001		8001800042-1		ICP		U7,18,49 (74H00)	21
022		003	0001		8001800044-1		ICP		U3,8,47 (74H04)	22
023		001	0001		8001800047-1		ICP		U39 (74H11)	23
024		001	0001		8001800048-1		ICP		U9 (74H20)	24
025		001	0001		8001800052-1		ICP		U57 (74H40)	25

BXD
BXR

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
026		001	0001		8001800054-1		ICP		U15 (74H51)	26
027		001	0001		8001800069-1		ICP		U38 (74H103)	27
028		028	0001		8001800123-1		ICP		U1,2,10,11,12, 19,20,21,22,29, 30,31,32,40,41, 42,50,51,52,60, 61,62,69,70,71, 72,79,80 (BDR)	28
029		000								29
030		001	0001		8001803121-1		ICP		U59 (74H74N)	30
031		001	0001		8001803155-1		ICP		U37 (74123N)	31
032		006	0001		8001803198-1		ICP		U6,17,36,44,58, 67 (74S00N)	32
033		011	0001		8001803200-1		ICP		U13,14,23,24,33, 34,43,48,53,63, 73 (74S04N)	33
034		001	0001		8001803202-1		ICP		U26 (74S10N)	34
035		001	0001		8001803203-1		ICP		U68 (74S11N)	35
036		001	0001		8001803207-1		ICP		U75 (74S40N)	36
037		003	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U4,5,16	37
038		000								38
039		002	0001		N8203N	18324	ICP	SIGNETICS	U54,74	39
		002	0001		9223-SS-115-7	06540	SPACER	AMATOM		40
041		001	0001		8001600007-1		DELAY LINE, TAPPED		DL3	41
042		004	0001		8001600008-1		DELAY LINE, FIXED		DL1,2,4,5	42
043		001	0001		1001005412-1		RETAINER, I/O CONN			43
044		001	0001		8001200015-1		TRANSISTOR		Q1 (TO5)	44
045		001	0001		1005000041-1		PAD, TRANSISTOR		TO5	45
046		002	0001		MS51957-16	96906	SCREW, MACHINE		4-40 X 7/16 LG	46
047		002	0001		9002100000-1		NUT, LOCK WASHER		4-40	47
048		000								48
049		000								49
050		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		50
051		000								51
052		000								52
053		REF	0001		LD2001002276-1		LOGIC DIAGRAM			53

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARKING (IDENTIFY).			201
202		000								202
203		REF	0001				AREA TO BE FREE OF SOLDER.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205		REF	0001				COMPONENT HEIGHT .395 MAX.			205
206		REF	0001				PROTRUSION SIDE 2, .075 MAX., LEADS TO BE VISIBLE THRU SOLDER.			206
207		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010 INCH/INCH IN GENERAL AREA AND .005 INCH/INCH IN CONNECTOR AREA.			207
208		REF	0001				SQUARE PAD DENOTES CATHODE END (STRIPE) OF DIODE, OR POSITIVE (+) END OF CAPACITOR, OR PIN 1 OF XFR.			208
209		REF	0001				RECTANGULAR PAD AND DOT OR SLOTTED END OF ICP DENOTES PIN 1.			209
210		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			210
211		A/R	0001		LECP1075		HARDWARF			211

BXD
BXR

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		20020001320-1		CABLE ASSY		SUE 7730-1	1
002	002	0001		3415-0001	75037	PRINTED CKT CONN	3M CO	50 CONTACT 25POS DUAL READOUT	2
003	003	0001		3476/50	75037	CABLE, FLAT RIBBON	3M CO	28AWG 50 COND SHIELDED, 2 DRAIN APPROX FT REQD	3

SUE 7730-1, -2, -3 Cable Assembly, Parts List
PL2002001320, Rev. A, Sheet 2

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		20020001320-2		CABLE ASSY		SUE 7730-2	1
002	002	0001		3415-0001	75037	PRINTED CKT CONN	3M CO	50 CONTACT 25POS DUAL READOUT	2
003	006	0001		3476/50	75037	CABLE, FLAT RIBBON	3M CO	28AWG 50 COND SHIELDED, 2 DRAIN APPROX FT REQD	3

BXD
BXR

SUE 7730-1, -2, -3 Cable Assembly, Parts List
PL2002001320, Rev. A, Sheet 3

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2002001320-3		CABLE ASSY		SUE 7730-3	1
002		002	0001		3415-0001	75037	PRINTED CKT CONN	3M CO	50 CONTACT 25POS DUAL READOUT	2
003		010	0001		3476/50	75037	CABLE, FLAT RIBBON	3M CO	28AWG 50 COND SHIELDED, 2 DRAIN APPROX FT REQD	3

SUE 7730-1, -2, -3 Cable Assembly, Parts List
PL2002001320, Rev. A, Sheet 4

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	5-20-74	
B	ECN 0140	5-19-75	

BXD
BXR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

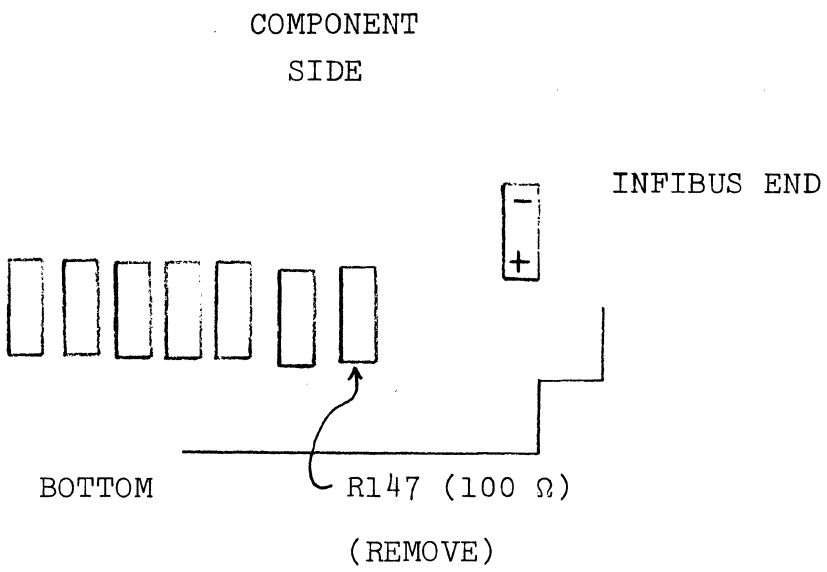
DRAWING TITLE

BXD STANDARD MODIFICATION

SIZE	CODE IDENT NO.	DRAWING NO.
A		BXD-15

SCALE	REV	SHEET
	B	1 OF 2

1. This modification cleans up the CLKA signal on the Infibus. Both the CMB and BXD must be modified or the BCU will be overloaded.
2. Remove R147 (100 Ω) from the bottom edge at the Infibus end of the BXD on the component side of the board.
3. Stamp ECN 140 in the upper left hand corner without overstamping existing stamps.



APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	9/21/76	
B	ECN 0284	4/12/78	EC

BXD
BXR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER R. Katsuki 5/2/78

APP'D FOR REL. R. Katsuki 5/21/78

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BXR STANDARD MODIFICATION

SIZE	CODE IDENT NO.	DRAWING NO.
A		BXR-15

SCALE	REV	SHEET
	B	1 OF 4

BXR ASSEMBLY

1. Good for revision levels: ALL

2. Parts required:

BBN#	PART	QTY
2	WW pins	14
130	Plastic Tag	1
162	74S02	1
181	Nylon Screw	1

3. Instructions:

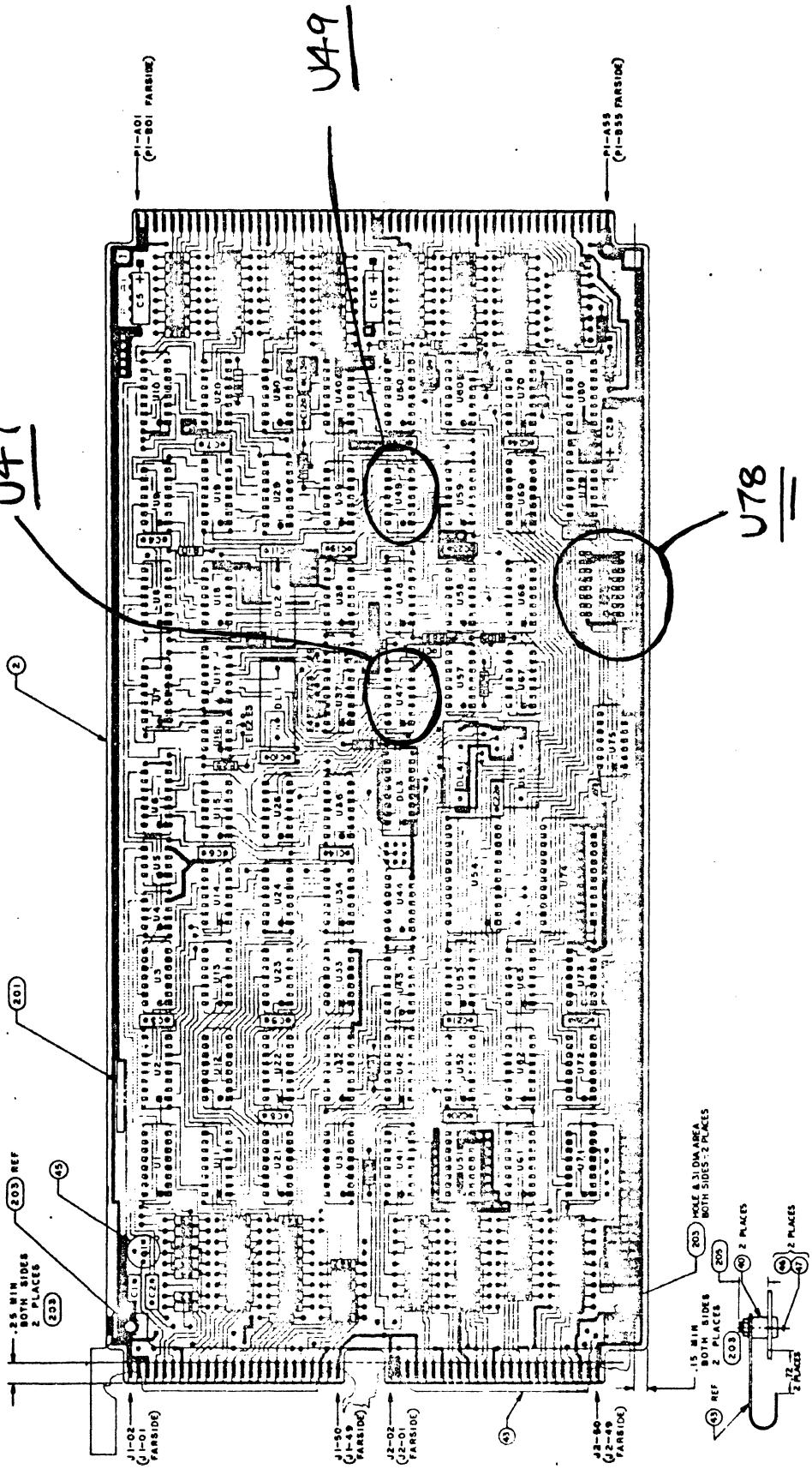
   a. Attach tag with board type and serial number to lower left-hand corner.

   b. Install 74S02 and 14 wirewrap pins in U78.

   c. Cut IC lead at U49:1 close to the board and lift the lead.

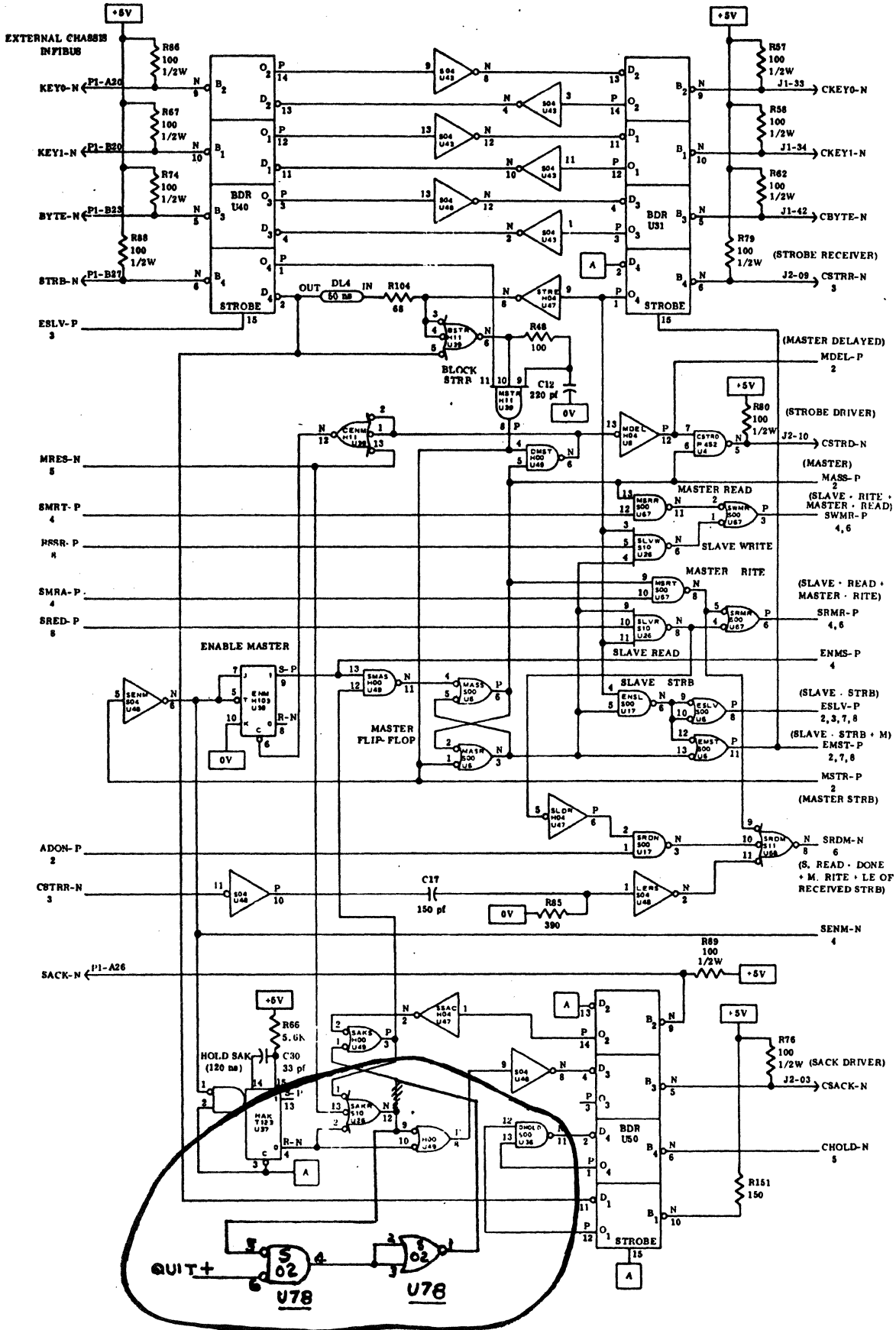
   d. Connect the following, wirewrapping except as noted: (Route wires under components)

      U78:1→U49:1 (wrap and solder to lifted lead at U49:1)
      U78:2→U78:3
      U78:3→U78:4
      U78:5→U49:9 (solder through hole at U49:9)
      U78:6→U47:10 (solder through hole at U47:10)
      U78:7→U79:8 (solder through hole at U79:8)



SUE 1829 Bus Extender Receiver BXR, Circuit Card Assembly 2001002276-1, Rev. A, Sheet 1

BXD
BXR



SUE 1829 Bus Extender Receiver BXR, Logic Diagram
LD2001002276-1, Rev. A, Sheet 3 of 8

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/12/75	

SEE BXD-Ø2

BXD
BXR

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER 751296

APP'D FOR REL 751296

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

BXD SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		BXD-2Ø

SCALE	REV	SHEET
	A	1 OF 1

Checksum/Block Transfer

CBT-Ø2 Logic Description

CBT-Ø5 Technical Reference

CBT-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED FOR PRODUCTION	8-30-74	
B	ECN 0117	12-13-74	
C	ECN 0218	7-14-76	

CBT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CBT - LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		CBT-02

SCALE	REV	SHEET
	C	1 OF 7

CBT LOGIC DESCRIPTION

The Checksum/Block Transfer Card (CBT) is a single card module whose operation is described in the CBT functional specification. Interfacing to a DMA, it allows transference of data from a source (transmit) to a destination (receive) buffer, calculation of a 16-bit cyclic checksum, or both simultaneously. In this detailed description of the implemented logic, signals signed "+" are true when at a TTL high level, and signals signed "-" are true when at a TTL low level, with a few isolated exceptions.

Source and Destination Control (CBT20)

For a checksum operation CHCKF will be true, and for a transfer operation XFERF will be true. If either of these is true, CKFER will be true. When performing a transfer, the destination end pointer must be written prior to writing the source end pointer, which starts the operation. When the destination pointer is written, the DMA raises STRTR (100-150 ns) which direct-sets WDEND, guaranteeing that DSTBD will be false. When a transfer is not desired, XFERF being false also insures that DSTBD is false. However, in the event that CKFER is false, indicating neither check nor transfer operations scheduled, GONOP will be true, and when the source end pointer is written to the DMA to start the operation, STRTT (100-150 ns) will cause the assertion of STNOP, setting NOPFF and INTFF to give the NOOP status bit and cause an interrupt request. WDEND is direct cleared the next time INTFF comes true. NOPFF is cleared by the next STBSY.

When CKFER is true and DSTBD is false, STRTT will cause STBSY, direct setting BUSYF, and RDYFT, and direct clearing NOPFF. STRTT alone will also direct clear LSTGO, EOBFF, STOPC, COUNT and the 4-bit counter whose output is DONET. Since BUSYF and RDYFT are true, REDYT is raised to the DMA and a source data word will be requested.

When the DMA responds with NOWTX (40-60 ns) to present the data to the device, RDYFT is direct cleared. If CHCKF is true, SWIPF (source word in progress) will be direct set. If XFERF is true, the leading edge of NOWTX will set DWIPF, raising REDYR to the DMA for a destination data request. When the DMA raises NOWRX (1 microsecond) to strobe the transferred data, DWIPF (destination word in progress) is direct cleared.

Checksum calculation is controlled by a 4-bit shift counter. When STSWI goes false after setting SWIPF, STOPS will be set. Following this, the first negation of CLOCK (80 ns period, derived from the INFIBUS clock) sets STOPC, after which the next negation of CLOCK sets COUNT, which enables the 74161 counter. The next 15 negations of CLOCK (rise of CLOCK-) increment the counter as the check register is being shifted. The 15th negation will produce a count of 1111, asserting DONET, which direct clears STOPS and STOPC. The next negation increments the counter to 0000 and clears COUNT, for a total of 16 clocks during the time that COUNT is true. The negation of COUNT clears SWIPF since LSTCK is false, to indicate completion of calculation for the current source data word.

When SWIPF goes false if CHCKF is true, and when DWIPF goes false if XFERF is true, or when the appropriate one of these goes false when only one operation is in progress, NXDWD comes true, setting RDYFT on its leading edge as long as EOBTX is false. This causes the next source data word request and the above procedure is repeated for subsequent words.

There are three different end conditions -- source end of buffer, source end of buffer with last checksum, and destination end of buffer. The last condition is an error case.

For a simple source end of buffer, the DMA will raise EOBTX while REDYT is true for the last word of the buffer. When either or both the checksum shifting and destination data request have completed, the leading edge of NXTWD will not set RDYFT, since EOBTX will be true; instead, the leading edge negation of BUSYF holds several of the control flops direct cleared and the trailing edge of BUSYF edge sets INTFF. This raises DOINT to the DMA to request a source interrupt. When the DMA responds with INTDN (40-60 ms), this signal direct clears INTFF and the operation is complete.

Due to the implementation of the checksum hardware, to end up with the actual checksum in the checksum register read by the program requires 16 extra shifts after the last buffer for a given calculation. Setting bit 15 of the source end pointer sets LASTF to indicate the last packet. In this case, when the DMA raises EOBTX during the last source word access, CHCKF will be true for the check operation and COUNT will be false since a word calculation is not presently in progress, so NOWTX direct sets LSTCK. When the last source word has been subjected to its 16 shifts, COUNT again goes false, SWIPF will remain set and LSTGO

will be set since LSTCK is true, but LSTCK itself will be cleared since it had been true -- all of this on the negation of COUNT. At the same time, the assertion of LSTGO direct sets STOPS and STOPC on the next assertion of CLOCK, since COUNT is false, allowing the 16 extra shifts. When COUNT next goes false, SWIPF and LSTGO will be cleared, since LSTCK is false. The negation of SWIPF will cause the assertion of NXTWD and, as before, its leading edge will clear BUSYF.

Finally, if the receive buffer will overflow with transfer of the next source data word to the destination buffer, the DMA will raise EOBRX during the request for the last available word in the destination buffer. When NXTWD next comes true, if EOBTX is not true, another transfer would overfill the destination buffer. Therefore, for XFERF true, EOBRX true, and EOBTX true, STEOB is asserted, and the assertion of NXTWD sets EOBFF to indicate end of destination buffer status. Since STEOB is true, making UNBSY true, the leading edge of NXTWD clears BUSYF, causing an interrupt request as above.

In the event of a data access quit, the appropriate data access request flop is direct cleared and BUSYF is direct cleared by QUITX, the OR of the two quit signals from the DMA. For a source quit, the DMA request will assert QUITT (80-100 ns), whose leading edge will set QUINT, since BUSYF is still true causing an interrupt request. In the event of a quit during an interrupt request, QUITT direct clears INTFF and, since BUSYF is now false, will guarantee that QUINT is cleared on its leading edge.

Data Registers (CBT21)

There are four data registers -- the available checksum feedback register (74S195s), the readable checksum result register (74164s), the source data register (74166s), and the destination data register (74174s).

Initialization of the feedback register is done either by loading an initial value or by clearing. When a check operation is not in progress, SWIPF will be false and writing to DMA register 111 will cause the DMA to assert DDPWR (100-150 ns), on whose leading edge the desired initial data is clocked into the 74S195 shift registers. Initially clearing the register is done by setting bit 0 in the source end pointer. If CHCKF is true, STRTT will direct clear the register to all zeros.

CBT

When the check operation is in progress, SWIPF is true, causing clock pulses to the register to shift rather than load, the register. While COUNT is true, the leading edge of CLOCK will shift the contents of this register. As long as LSTGO is false, the result of the four tap XOR network will be the serial input to the register. During the final 16 shifts of a last checksum operation, however, LSTGO will be true and the serial input will be held at zero. The 74164 readable checksum register is a 16-bit shift register, which shifts on the leading edge of CLKOK while COUNT is true. It will at any time contain the last 16 bits that appeared at CKSUM. During a checksum operation, or after an intermediate buffer has been checked, this will be identical to the contents of the feedback register, and its contents may be written as the initial checksum value for subsequent buffers. After a last checksum buffer, the readable register will contain the correct checksum such that appending it to the buffer or series of buffers and recalculating the checksum will result in reading a zero checksum at the conclusion of the operation.

Taps are chosen to conform with the IBM CRC16 and the CCITT polynomials. The 74S157 selector is controlled by CRC16, which is asserted for the switch in the operated position, giving the IBM checksum. The XOR network is straightforward.

The 74166 source data register supplies the data input to the XOR network for the feedback register. It is leading edge loaded with bus data when the DMA asserts NOWTX following a source data request, since RDYFT is true. With NOWTX and RDYFT false, CLOCK shifts the data into the XOR while COUNT is true. Following each word, the contents of this register will be zero, allowing for the proper result on a final buffer checksum.

The destination data register allows the destination bus access to take place in parallel with the source checksum calculation. It is loaded on the leading edge of NOWTX when the DMA responds to a source data request.

Device Status and Switches (CBT22)

When the DMA asserts GVSTT when source status is being read, open collector gates pull down the active status lines (STS09-STS15) as indicated in the functional specification. When device-type data is being read and GVDTX is asserted, the type of checksum appears at STS00, and a hardwired 3 at STS08 and STS09. Destination read status is unused.

Switches for device address, PID address, and source PID level are implemented in the usual manner. An operated switch is a 1 in that bit position. Address switches use passive pullups while the PID switches connect the correct inverters to the open collector status bus (STS01-STS07). The input to the inverters is GVPIT asserted by the DMA to read the source PID level. The destination PID level function is unused.

The error logic consists of two pieces. When CLEAR is asserted and ERRFF is false, the negation of BUSYF sets ERRFF, so that a CLEAR when BUSYF is true sets ERRFF. This error condition is ORed with the other possible error conditions -- destination QUIT (QUITD), NO OP source (NOPFF), destination end of buffer (EOBFF) -- to assert ERROR to the DMA source and destination error lines. Each side of the DMA internally ORes the quit condition into its error status. All the device error conditions are cleared by writing the source end pointer (STRTT asserted). Also, when BUSYF is true, ERROR will be held true.

Since only the source status is used, the destination quit signal must be latched to drive a source status bit and the source error line. This function is accomplished by QUITR direct setting QUITD. That flop is gated to the open collector status bus and ORed into ERROR. The OR of QUITR and QUITT, QUITX is applied to the control logic.

The last buffer information is contained in two flops. LASTF is set on the leading edge of STRTT when bit 15 is set in the source end pointer. This indicates the last source buffer. The negation of BUSYF at the end of the operation sets LASTS and when XFERF is true and ERROR false, raises LASTP to the destination side of the DMA, indicating the last buffer of a transfer was transferred without error.

The type of operation to be performed is given by writing the appropriate source status. The leading edge of STBST (100-150 ms), reads DBR14 into XFRSN and DBR15 into CKSYN to set status for a transfer operation and a checksum operation respectively. Either or both may be set, but if neither is set the control logic will report an error when the source end pointer is written. The trailing edge of STBST clocks these two flops into XFERF and CHCKF, which appear as read source status and are applied to the control logic for transfer or for checksum operations. CKFER is true when either of these flops is set. If the bus data disagrees with the present state of these two flops during STBST, as indicated by the XOR signals CGXFR and CGCHK,

CBT

CLEAR is asserted during STBST. These status bits can be direct cleared only by a master reset passed through the DMA (MRES, 500 microseconds).

Other components of CLEAR are RESER and RSTRR, destination reset and restart, and RESET and RSTRT, source reset and restart. Restart is writing the begin pointer. All of the above signals are 100-150 ms.

Bus and DMA Interconnection (CBT23)

The bus data lines are driven and received by the standard CMI bus driver/receiver. The drivers are enabled either by assertion of DDPRD, asserted by the DMA when register 111 is used, or assertion of NOWRX in response to a destination data request.

The 74S158 data selectors gate the destination data buffer to the BDR driver inputs when NOWRX is asserted. Otherwise, the readable checksum register appears at the driver inputs.

The 25MHz INFIBUS clock CLKAB is received by a Schottky inverter which toggles CLOCK to produce the 80 ns period shift clock. Aside from precedence pulse passing, no other bus lines are used.

DMA connection is in the usual way. Unused lines are left unconnected with the exception of the destination interrupt request line. Since only the source interrupt is used, the destination line is tied low.

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED FOR PRODUCTION	8-30-74	

CBT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER 1/16/76 (AM)

APP'D FOR REL 1/16/76 (AM)

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

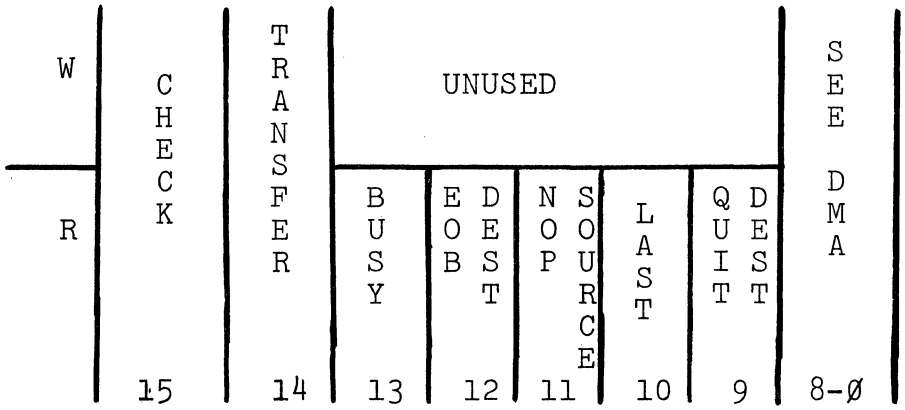
CBT TECHNICAL REF.

SIZE	CODE IDENT NO.	DRAWING NO.
A		CBT-05

SCALE	REV	SHEET 1 OF 2

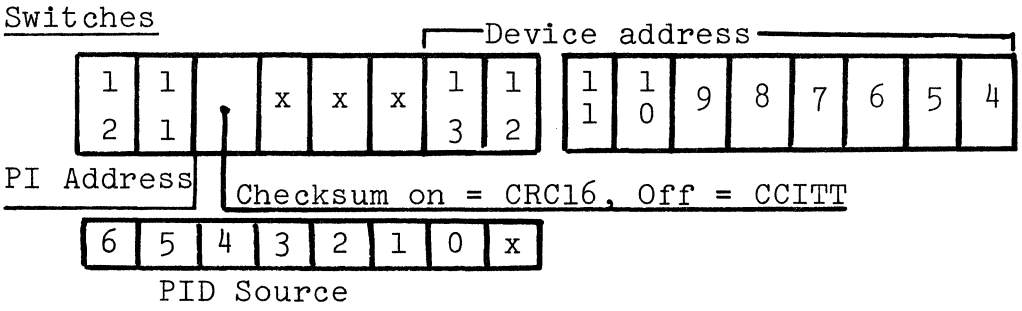
See DMA

Status - address FXXXC (source)



Note: address FXXX6 (destination) - see DMA

Switches



Jumpers - none

CBT

CBT-2Ø SCHEMATICS

12	11	10	9	8	7	6	5	4	3	2	1	
				7400	7400	7474	7474	74S74	74S74	7474	74S74	A
				7408	7408	7408	74S11	74S11	74S11	7400	7400	B
			SWITCH-8 P1 ADDRESS	SWITCH-8 ADDRESS	RES. 4.7K Δ	7400	7451	74S00	74S86	74161	7402	C
			SWITCH-8 P1D LEVEL	7403	7403	7411	74166	74S195	74174	74174	74174	D
			7411	7405	7405	DRES Vcc 1K 1K 1K 1K 1 2 3 4	74166	74S195	74S157	74S158	BDR DBR00- ↓ DBR03-	E
			7400	7402	7486	74S04	74164	74S195	74S158	74S158	BDR DBR04- ↓ DBR07-	F
			7474	7474	7474	74S74	74164	74S195	74S158	BDR DBR12- ↓ DBR15-	BDR DBR08- ↓ DBR11	G

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	9 27 74

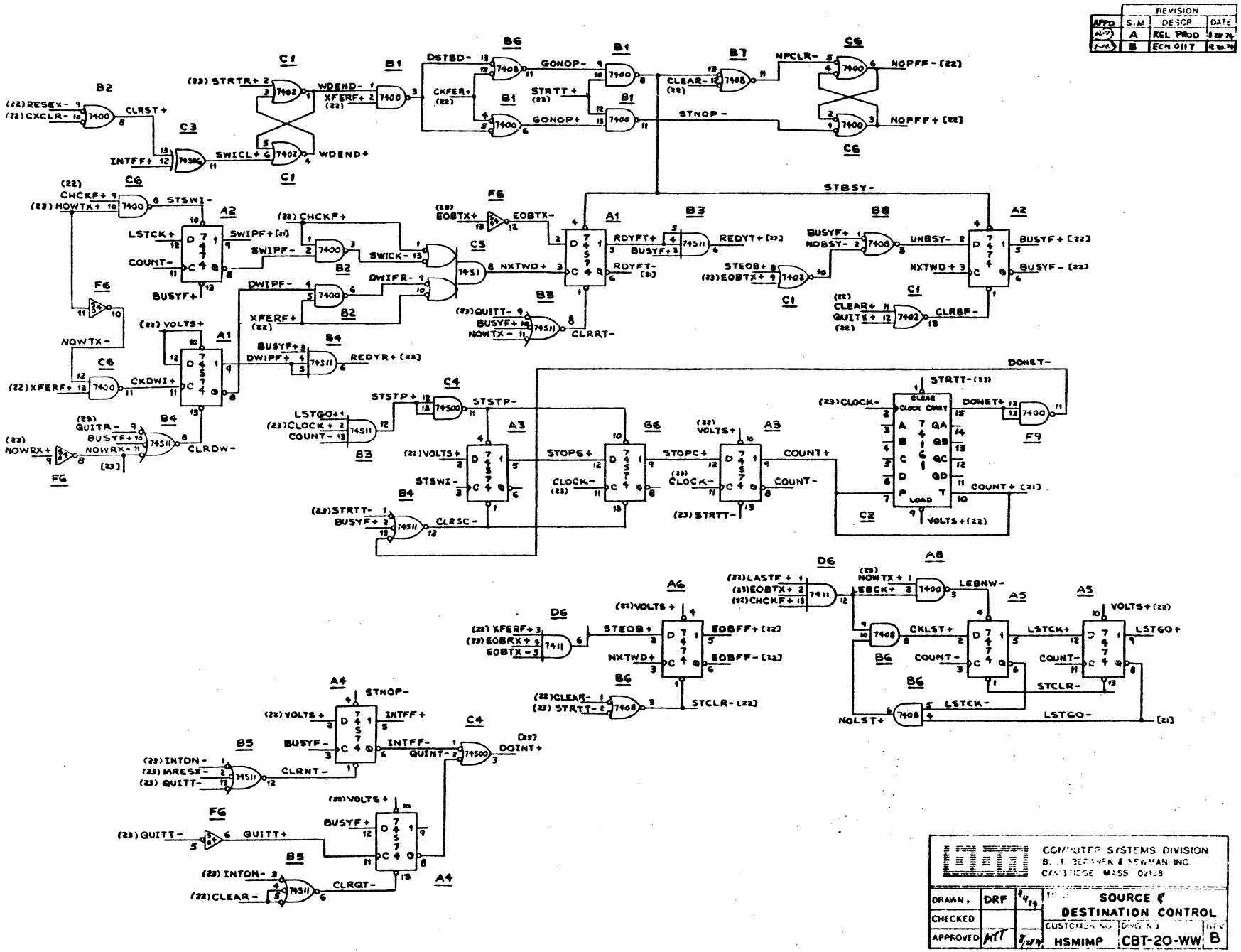
NOTES :

TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8 28 73	TITLE	INTEGRATED CIRCUIT LAYOUT	
CHECKED					
APPROVED	MJT	9/27/74	CUSTOMER/NO. HSMIMP	DWG NO. CBT-00-WW	REV A

CBT


REVISION
APPD | S.M | DESCR | DATE
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B | ECN 0117
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STSTP+
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STOPS+
STOPC+
COUNT+
COUNT-
CLRDW-
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CLEAR-
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BUSYF-
UNBSY-
NOWTX+
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NOWRX+
NOWRX-
CKDWI+
LSTCK+
LSTGO-
COUNT-
VOLTS+
CHCKF+
LSTGO+1
COUNT-13
RESEX-
CXCLR-
CLRST+
INTFF+
STRTR+
QUITR-
INTDN-
MRESX-
QUITT-
CLEAR-
EOBTX+
EOBTX-
EOBRX+
CHCKF+13
LASTF+
EBCK+
EOBTX+2
EOBRX+4
EOBTX-5
XFERF+3
STRTT-2
CLEAR-1
STRTT-1
BUSYF+2
BUSYF+10
BUSYF+8
BUSYF+1
NDBSY-2
STEOB+
STEOB+8
EOBTX+9
CLEAR+11
QUITX+12
CLOCK+2
CLOCK-13
CLOCK-
STRTT-(23)
VOLTS+(22)
COUNT+(21)
LSTCK-
STRTT-(23)
A1
A2
A3
A4
A5
A6
A8
B1
B2
B3
B4
B5
B6
B7
B8
C1
C2
C3
C4
C5
C6
D6
F6
F9
G6
7400
7402
7408
7411
74500
74511
74S51
74S74
74S77
74S86
7451
CBT-20-WW
B
DRAWN. DRF
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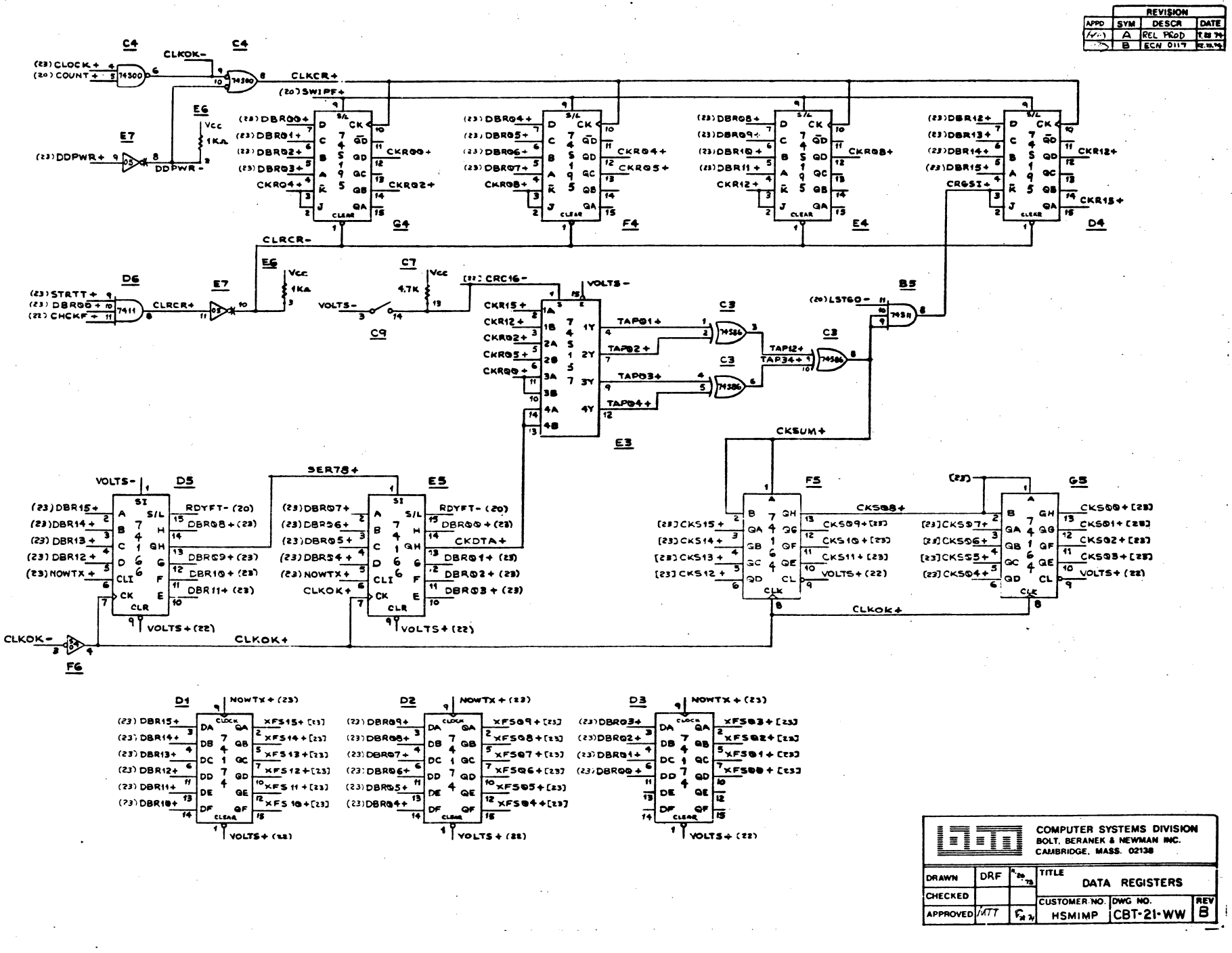
APPROVED MIT
SOURCE & DESTINATION CONTROL
HSMIMP
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE MASS 02138


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD
B | ECN 0117
C4
CLKOK-
(23) CLOCK +
(20) COUNT +
74S00
74S00
CLKCR+
(20) SWIPF+
E6
Vcc
1KA
E7
(23) DDPWR+
DDPWR-
(23) DBR00+
(23) DBR01+
(23) DBR02+
(23) DBR03+
CKR04+
CKR00+
CKR02+
G4
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CKR12+
CKR08+
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(23) DBR14+
(23) DBR15+
CRGSI+
CKR12+
CKR15+
D4
CLRCR-
D6
(23) STRTT+
(23) DBR00+
(22) CHCKF+
7411
CLRCR+
E6
Vcc
1KA
C7
4.7K
Vcc
VOLTS-
C9
(22) CRC16-
VOLTS-
CKR15+
CKR12+
CKR02+
CKR05+
CKR00+
TAP01+
TAP02+
TAP03+
TAP04+
C3
74S86
TAP12+
TAP34+
E3
B5
(20) LSTGO-
74S11
CKSUM+
VOLTS-
D5
(23) DBR15+
(23) DBR14+
(23) DBR13+
(23) DBR12+
(23) NOWTX+
RDYFT- (20)
DBR08+ (23)
DBR09+ (23)
DBR10+ (23)
DBR11+ (23)
VOLTS+ (22)
SER78+
E5
(23) DBR07+
(23) DBR06+
(23) DBR05+
(23) DBR04+
(23) NOWTX+
CLKOK+
RDYFT- (20)
DBR00+ (23)
CKDTA+
DBR01+ (23)
DBR02+ (23)
DBR03+ (23)
VOLTS+ (22)
F5
(23) CKS15+
(23) CKS14+
(23) CKS13+
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CKS08+
CKS09+ (23)
CKS10+ (23)
CKS11+ (23)
VOLTS+ (22)
(23)
G5
(23) CKS07+
(23) CKS06+
(23) CKS05+
(23) CKS04+
CKS00+ (23)
CKS01+ (23)
CKS02+ (23)
CKS03+ (23)
VOLTS+ (22)
CLKOK+
CLKOK-
F6
CLKOK+
D1
NOWTX+ (23)
(23) DBR15+
(23) DBR14+
(23) DBR13+
(23) DBR12+
(23) DBR11+
(23) DBR10+
XFS15+ (23)
XFS14+ (23)
XFS13+ (23)
XFS12+ (23)
XFS11+ (23)
XFS10+ (23)
VOLTS+ (22)
D2
NOWTX+ (23)
(23) DBR09+
(23) DBR08+
(23) DBR07+
(23) DBR06+
(23) DBR05+
(23) DBR04+
XFS09+ (23)
XFS08+ (23)
XFS07+ (23)
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XFS05+ (23)
XFS04+ (23)
VOLTS+ (22)
D3
NOWTX+ (23)
(23) DBR03+
(23) DBR02+
(23) DBR01+
(23) DBR00+
XFS03+ (23)
XFS02+ (23)
XFS01+ (23)
XFS00+ (23)
VOLTS+ (22)
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138
DRAWN DRF
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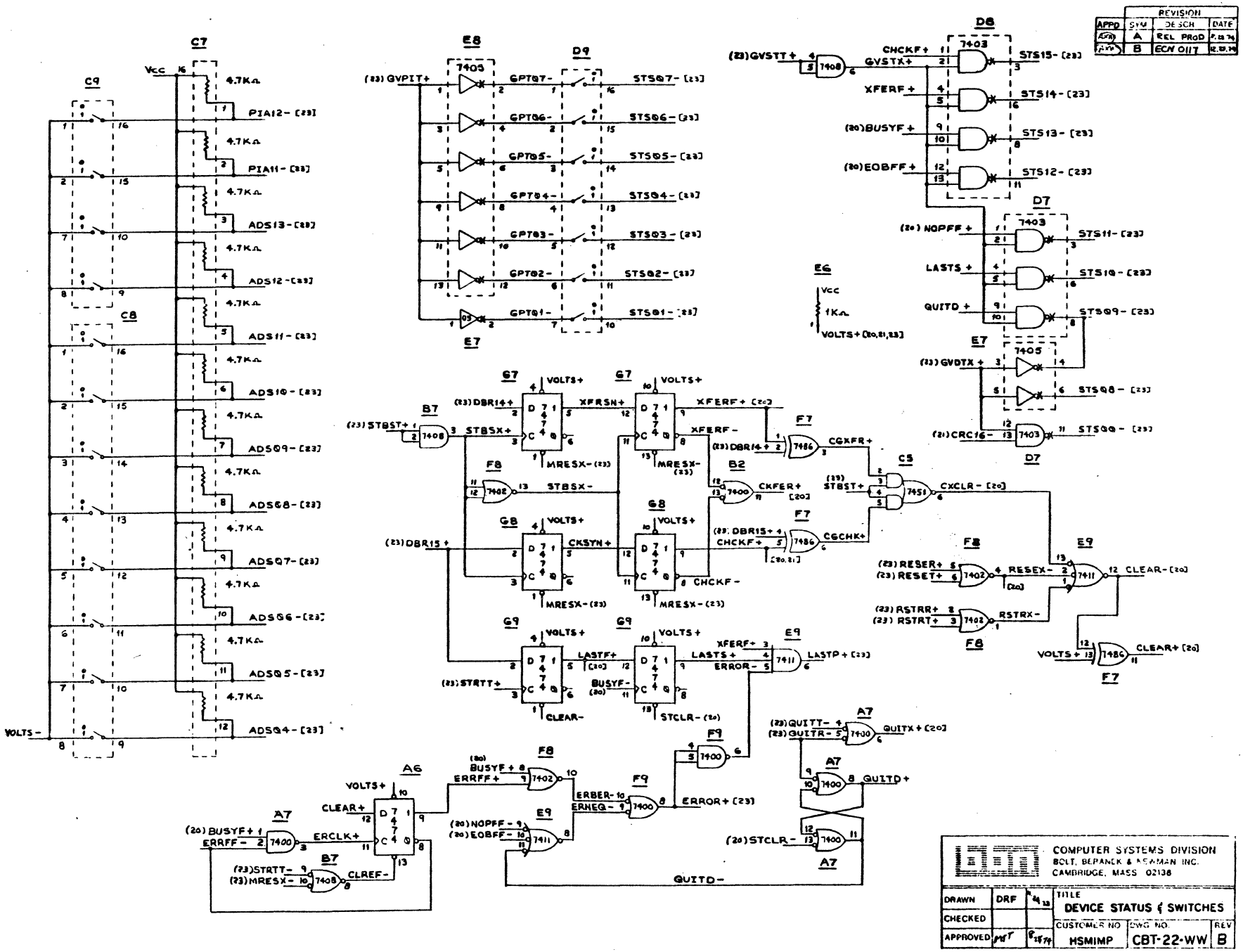
APPROVED MTT
TITLE
DATA REGISTERS
CUSTOMER NO. HSMIMP
DWG NO. CBT-21-WW
REV B
CBT



COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138			
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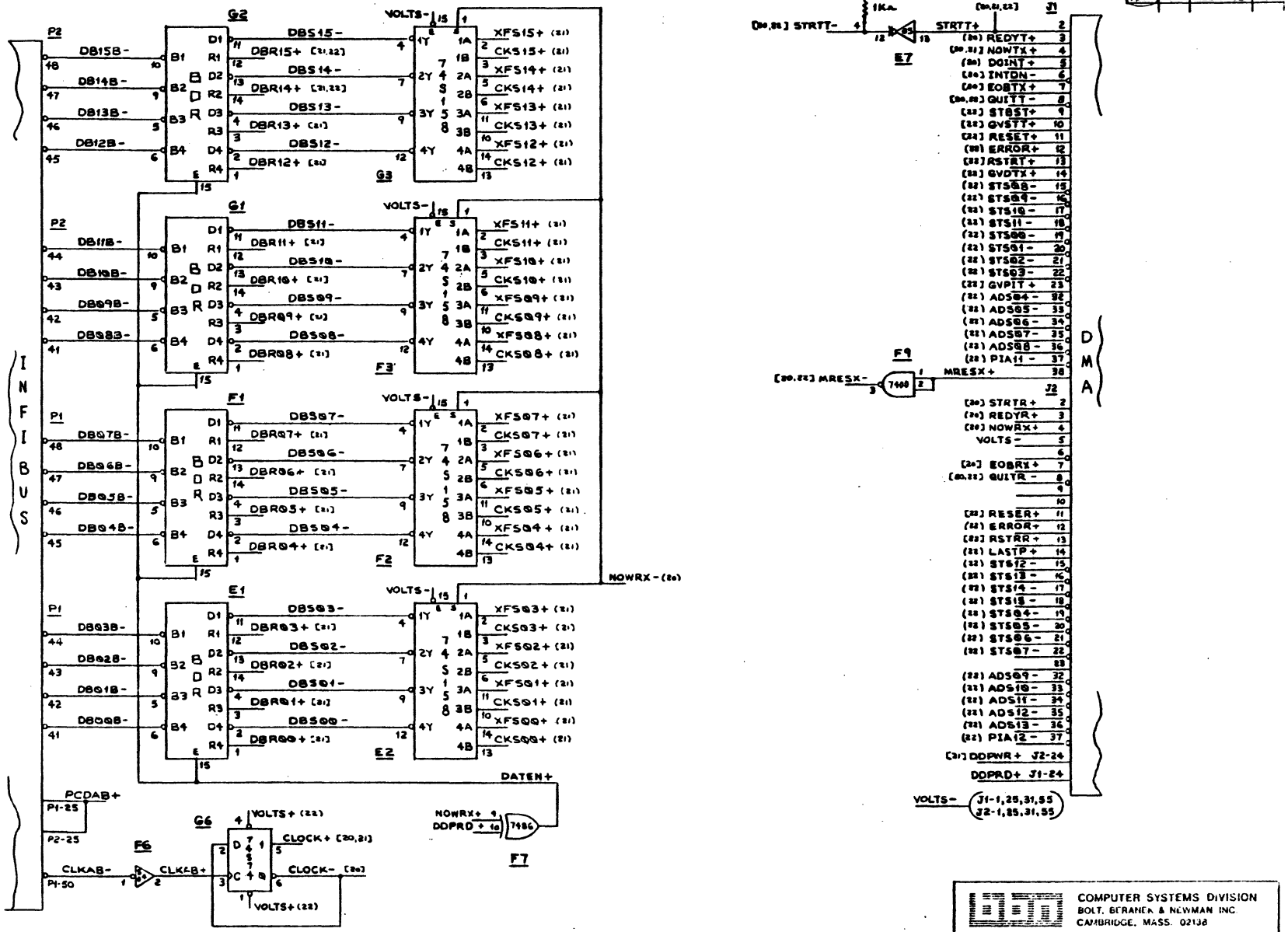
CHECKED			
APPROVED	[illegible]	5/74	CUSTOMER NO: HSMIMP DWG NO: CBT-22-WW REV: B



REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF		TITLE	BUS & DMA INTERCONNECTION
CHECKED			CUSTOMER NO.	DWG NO. / REV
APPROVED			HSMIMP	CBT-23-WW / A

CBT

Processor Arithmetic Control Unit

CPA-Ø2 Logic Description

CPA-Ø5 Technical Reference

CPA-15 Standard Modifications

CPA-2Ø Schematic

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE FOR PRODUCTION		

SEE CPB-02

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/9/75

CHECKER

ENGINEER 751206

APP'D FOR REL 751206

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CPA LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		CPA-02

SCALE	REV	SHEET 1 OF 1

CPA

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	5-[illegible]-74	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CPA

CONTRACT NO:	
DRAFTSMAN	
CHECKER	
ENGINEER	
APP'D FOR REL	
APP'D (CUSTOMER)	

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CPA TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		CPA-05

SCALE	REV	SHEET
	A	1 OF 2

CPA - Processor Arithmetic Control Unit Lockheed

See also CPB-Ø5

Status - address FFXO

X is 1 for processor 0, 3 for processor 1

See CPA-Ø1

Note: processor connected to BCU is always #0.

Switches -- none

Jumpers

Processor Number

Number	J2	J3
0	1 to 2	1 to 2
1	-	1 to 2
2	1 to 2	-
3	-	-

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	5 [illegible]	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CPA

CONTRACT NO:	
DRAFTSMAN	
CHECKER	
ENGINEER	
APP'D FOR REL	
APP'D (CUSTOMER)	

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CPA ASSY MODIFICATION

SIZE	CODE IDENT NO.	DRAWING NO.
A		CPA-15

SCALE	REV	SHEET
	A	1 OF 3

Card Type CPA Modification Standard

Card Function: Processor Arithmetic

Modification Description:

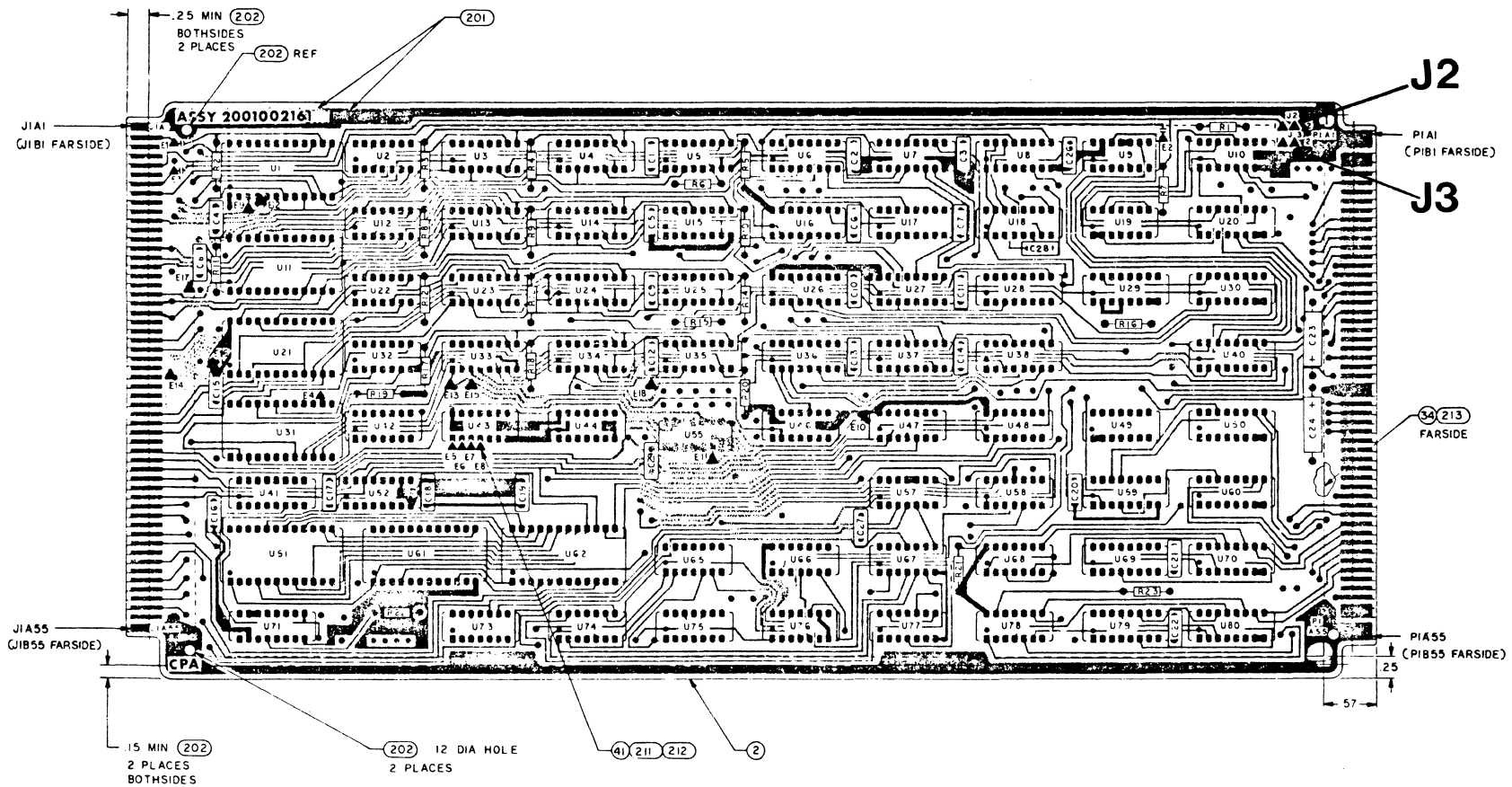
Selects processor number 1. This is defeated by BCU connection to processor Ø.

Implementation: See drawing attached.

Jumper J3-1 to J3-2 with 30 ga solid wire wrapped to each pin.

Make sure J2 is not jumpered.

Jumpers are at upper right corner of board.


.25 MIN (202)
BOTHSIDES
2 PLACES
(202) REF
(201)
ASSY 2001002161
J2
J3
J1A1
(J1B1 FARSIDE)
P1A1
(P1B1 FARSIDE)
(34) (213)
FARSIDE
J1A55
(J1B55 FARSIDE)
P1A55
(P1B55 FARSIDE)
CPA
.25
57
.15 MIN (202)
2 PLACES
BOTHSIDES
(202) 12 DIA HOLE
2 PLACES
(41) (211) (212)
(2)

CPA

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SEE CPB-Ø2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CPA

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER 12/8/75

APP'D FOR REL 12/8/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CPA SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		CPA-2Ø

SCALE	REV	SHEET 1 OF 1

Processor Control Board

CPB-Ø2 Logic Description

CPB-Ø5 Technical Reference

CPB-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	[illegible]	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR RELEASE

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CPB LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		CPB-Ø2

SCALE	REV	SHEET OF
	A	

CPB

SUE 1110A, 1111A, and 1112A PROCESSORS

MAINTENANCE BULLETIN M1110A/11A/12A

CPB

1463

May 74

CONTENTS

CPB

LIST OF ILLUSTRATIONS

LIST OF TABLES

PREFACE

This maintenance bulletin is written primarily for system user and service personnel with backgrounds in digital systems. Refer to Reference Bulletin R1110A/11A/12A for related general information, and to General System Bulletin G3 for a description of the SUE Processor Instruction Sets. For a description of the microcodes, refer to the micro-assembly list and flow charts for the respective processors as follows:

SUE 1110 Revision C, 8-27-73
SUE 1111 Revision C, 8-24-73
SUE 1112 Revision C, 9-10-73

SUE 1110A/1111A/1112A PROCESSORS
MAINTENANCE BULLETIN

INTRODUCTION

This bulletin contains detailed information about the SUE 1110A, 1111A, and 1112A Processors. SUE 1110A is the general purpose processor, SUE 1111A is the decimal arithmetic processor designed for business applications, and SUE 1112A is the scientific double-precision processor. The three processors are logically identical except for their microprograms stored in Read Only Memories (ROMs), and each can operate both as a central processor unit (CPU) in single and multi-processor systems, and as a secondary processor in multi-processor systems.

The processors are designed to be independent of other system modules and to minimize use of the INFIBUS. They contain their own buses for inter-register transfers, and each operates on data received from either a system memory module or directly from an input-output controller. All three processors perform the basic instruction set used for general purpose applications, and their respective extended instruction sets. The instructions are described in General System Bulletin G3.

All SUE processors perform their respective instructions under control of a microprogram using 36-bit control words. On SUE 1110A the microprogram is stored in nine, 1024-bit ROMs organized in 256 by 4-bit words. These ROMs are addressed in straight 8-bit binary using full on-chip decoding. On SUE 1111A and 1112A, the microprogram is stored in nine 2048-bit ROMs organized in 512 by 4-bit words to accommodate the larger instruction sets of these processors. The 2048-bit ROMs are addressed in straight 9-bit binary with full on-chip decoding.

CPB

In addition to the nine ROM control storage microcircuits, each processor contains two 1024-bit ROMs organized in 256, 8-bit control words that form a look-up table. These ROMs are enabled and addressed by the current word from microprogram storage.

DESCRIPTION

Each SUE processor is contained on two, multi-layer printed circuit cards measuring 6-1/4 by 13-1/2 inches. The circuit card containing the arithmetic-logic unit is the CPA. The other card containing the ROM microcircuits and control logic is the CPB. Both cards plug into adjacent slots on the INFIBUS and are interconnected on their back edge by an interconnect module containing either two or three connectors depending on the processor function in the system. The first processor installed in any SUE system is interconnected with the bus controller and assumes central processor functions. Therefore, the interconnect module for the CPU is an ICM containing three connectors. Any secondary processor in the system is interconnected by an IDM module containing two connectors. Neither the ICM nor the IDM circuit cards contain discrete or logical circuit components. They provide only pin-to-pin wiring connections between the circuit cards.

Central processors (interconnected by an ICM) in SUE systems are denoted by a -1 suffix such as 1110A-1. Secondary processors (interconnected by an IDM) are denoted by a -2 suffix such as 1110A-2.

INSTALLATION CONSIDERATIONS

The central processor module is plugged into the INFIBUS immediately to the left of the bus controller (BCU), viewing the chassis from the module insertion end. The CPB must be inserted in the next adjacent slot left of the bus controller, and the CPA must be inserted in the next slot left of the CPB. An ICM circuit card is then plugged into the CPA, CPB and BCU circuit cards to interconnect their back edge connectors (J1).

Secondary processors in multiprocessor systems must be installed in any two adjacent slots left of the CPU, the CPA inserted left of the CPB. An IDM circuit card is then plugged into the CPA and CPB to interconnect their back edge connectors (J1). Location of secondary processors in the chassis is a matter of judgment. Modules closest to the BCU have highest precedence for bus access.

All edge connectors on SUE circuit cards are keyed to avoid improper insertion between the INFIBUS and an interconnect circuit card; but the interconnect circuit cards are not keyed to avoid improper relative locations of CPA and CPB. Refer to CPA and CPB designations etched on the circuit cards when installing processor modules.

PROCESSOR ADDRESS JUMPERS

Jumper connections at J2 and J3 (see Logic Diagram LD2001002161, Sheet 8) are provided on the CPA to encode the address assigned to the processor for addressing by another system module. Four processors can be addressed in a system: binary 00, 01, 10, and 11. An installed jumper encodes binary 0; no jumper a binary 1. In SUE standard practice, the CPU is forced to address 00 by signals CPU0, CPU1 from the BCU through the interconnect module. If the BCU is not connected to the CPU, (i.e. because of an extender card during maintenance) then the CPU address comes only from the jumpers. In that case, and for all secondary processors, both jumpers J2-1, -2 and J3-1, -2 must be connected on the CPA to encode the processor address. Table 1 lists the addresses and corresponding jumpers.

Table 1. Processor Address Jumpers

Processor		Jumpers Installed	
Number	Binary Address	J3-1 to J3-2 (Lower)	J2-1 to J2-2 (Upper)
1 (CPU)	0 0	Yes	Yes
2	0 1	Yes	No
3	1 0	No	Yes
4	1 1	No	No

CPB

ROM ADDRESS JUMPERS

On SUE 1111A and 1112A processors, the S register is extended to 12 bits by a third 4-bit synchronous counter component, and address jumpers are installed on the CPB at terminals J2-A1 to J2-A2 and J2-B1 to J2-B2 to extend the most significant ROM address bits as needed to address the larger ROMs. (See Logic Diagram LD2001002169-1 Sheet 2.) The ROM address jumpers are installed on the CPB as indicated in Table 2.

Table 2. ROM Address Jumpers

Processor Model	CPB Jumpers Installed	
	J2-A1 to J2-A2	J2-B1 to J2-B2
1110A	Yes	Yes
1111A	Yes	No
1112A	Yes	No

SINGLE-STEP JUMPER

A jumper is provided on the CPB that allows single-step sequencing through the microcode from the control panel for processor maintenance tests. Jumper J3-1 connected to J3-2 disables the gate that normally enables the run clock, and allows single-step operation only.

LOGIC ORGANIZATION

Figure 1 is a functional block diagram of the processor logic that shows the general data flow within the processor. The blocks in Figure 1 are keyed to the CPA and CPB logic diagrams by the alpha-numeric designations in the upper left-hand corner of each block. The numeric denotes the sheet number on which the related CPA or CPB logic diagram is located.

SUE processors are organized around the arithmetic logic unit (ALU) and ROM microcode control. The Address (A), Transmit (T), and Receive (R) registers are interfaced with the INFIBUS and data from these registers are selectable for

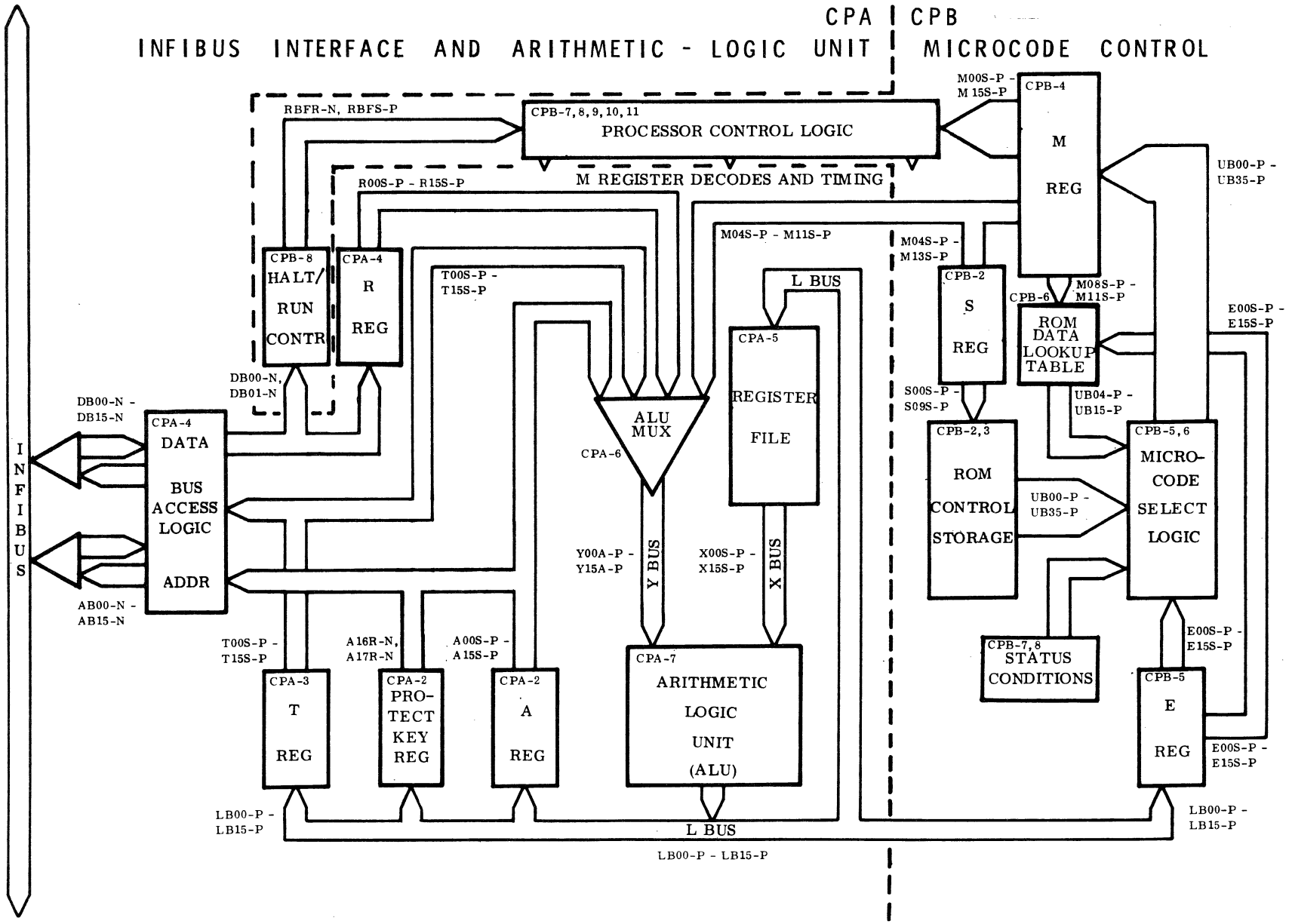


Figure 1. SUE 1110A, 1111A and 1112A Functional Block Diagram

input to the ALU, depending on the decode of the current microcontrol word in the M register. The current word in the M register is decoded to supply control and timing functions throughout the processor.

INFIBUS INTERFACE AND ARITHMETIC LOGIC UNIT (CPA)

The ALU can process two 16-bit operands in parallel received through the X and Y buses. The ALU, ALU multiplexer, and register file all respond to commands from the current microcode word from the M register. The multiplexer responds to the two bit microcode Y field and selects a 16-bit operand from the A, T, or R registers; or a masked literal from the microcode L1-L2 fields for input to the ALU. The other sixteen bit operand is received from one of twelve registers in the register file.

The ALU responds to the A and T fields of the microcode word which specifies one of 16 logical or one of 16 arithmetic functions to be performed. The ALU performs the functions on the two ALU inputs, and on an arithmetic carry-in that adds to the least significant bit position. Output of the ALU is 16 bits that represent the microstep results. The results may be written into the A, T, or E register and/or one of the file registers through the L bus.

The register file consists of twelve 4-by-4 flip-flop arrays that make up twelve 16-bit registers. Decodes of the four-bit microcode X field select one of the twelve registers to read input from the L bus or to write output to the ALU through the X bus. If the X field selects a nonexistent file as input (i.e. bits 15 to 12), then a word containing all ONEs is read out. The twelve registers in the file include the program counter (register R0), seven general registers (R1 through R7), status register (R8), instruction register (R9), and two registers, firmware A and firmware B, that are used to store temporary results. Of the twelve registers, R0 through R9 are accessible to the programmer but access to firmware A and firmware B is not included in the normal instruction repertoire.

Most of the processor interface logic to the INFIBUS is contained on the CPA, but some bus control signals are received by the CPB. Registers A, T, and R are interfaced with the INFIBUS. The A register holds the address that is placed on the INFIBUS to address another system module; the T register holds the data to be transmitted; and the R register receives data from the INFIBUS. All three registers are gated to the ALU for logical or arithmetic combinations with the selected file register.

The interface logic also contains address recognition logic to recognize when the processor is being addressed by another system module to transfer data. The processor responds by receiving or transmitting the contents of the control register if specifically addressed or any other selected file register when the microprogram has properly halted.

Bits A16R-N and A17R-N of the A register are held in two flip-flops that make up the Protect Key register. These bits are available for use in systems equipped with memory protect or bank select/extended memory features.

MICROCODE CONTROL (CPB)

The microcode control logic consists of three registers, Sequence (S), Microcode (M), and Emulation (E); the ROM control storage and microcode select logic; ROM data lookup table; status logic; processor control logic; and halt/run flip-flops. Register S is a twelve bit counter (only eight or nine bits are used) that addresses the ROM control storage and is automatically incremented by a clock pulse to sequence the microprogram. The M register receives the 36-bit microcode control word that specifies both the action of the current microstep and modifications of the next sequential step. M register outputs are decoded into enabling terms and distributed with clock pulses throughout the processor by the processor control logic.

CPB

The E register holds sixteen bits which may be tested or used to modify the microcode. E register fields correspond to the macro-instruction word being emulated

and specify instruction code, addressing mode, general register, index register, or a shift count. Bits E3 thru E0 also can operate as a loop counter.

The ROM data lookup table contains 256 eight-bit words. When enabled and addressed by the current microcontrol word in the M register, and a four-bit field from the E register, the table output is ANDed with the literal fields of the next control word from ROM control storage. Other status conditions, when enabled by the current control word, also can be ANDed into the literal fields of the next control word. The microcode select logic forms the AND of the ROM control storage and the other enabled functions and places the control word into the M register. Because of an inherent look-ahead feature in the processor, the next control word is being read while the current word is being executed.

The control register consists of two flip-flops: halt and run. Halt buffers a request to halt that is used by the microcode to enter a halt routine. Run flip-flop controls the clock and may be turned off by the microcode or turned on by writing into the run flip-flop from the INFIBUS. The reset side of the run flip-flop, instead of the set side, asserts the clock enable.

MICROCODE WORD FORMAT

The microcode word format is shown in Figure 2. Fields in the word are related to the organization and functions of the processors. Conditional test and skip or jump microsteps are provided to minimize the length of the microprograms.

35 34 33	32	31 30 29 28	27 26	25 24	23 22 21 20	19 18	17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2 1 0
S	T	A	C	D	X	F	Y	M	L_2	L_1	Z	W

Figure 2. Microcode Word Format

S FIELD, BITS 35 THRU 33: MICROCODE TYPE

Specifies type of microcommand. The type may be a normal sequential step, special command, branch, memory synchronize, or conditional jump command. Values of S cause special interpretation of the D, M and L fields:

S = 0, Sequential step
S = 1, Sequential step and enable special commands
S = 2, Branch
S = 3, Wait for bus access to complete
S = 4, Jump if condition false
S = 5, Jump if condition true
S = 6, Jump if selected bit of T Register is false
S = 7, Jump if selected bit of T Register is true

T FIELD, BIT 32: LOGICAL OR ARITHMETIC FUNCTION
A FIELD, BITS 31 THRU 28: ALU CODE

The four bits of A select one of sixteen logical functions if T = ZERO, or one of sixteen arithmetic functions if T = ONE, to be performed by the ALU as indicated in Tables 3 and 4.

CPB

Table 3. ALU Logical Codes, T = 0

A Field Hexidecimal	Logical Function	Description	Symbolic
0	Complement X	Output a 1 for every 0 in X	$\overline{X}$
1	Nor	Output a 1 for every 0 in X and Y	$\overline{X \text{ or } Y}$
2	Mask Y	Output a 1 for every 0 in X and 1 in Y	$\overline{X}$ and Y
3	Clear	Output all ZEROs	0
4	NAND	Output a 1 for every 0 in X or Y	$\overline{X \text{ and } Y}$
5	Complement Y	Output a 1 for every 0 in Y	$\overline{Y}$
6	Exclusive OR	Output a 1 for every bit of X and Y that differ	$X \oplus Y$
7	Mask X	Output a 1 for every 1 in X and 0 in Y	X and $\overline{Y}$
8	Insert in Y	Output a 1 for every 0 in X or 1 in Y	$\overline{X}$ or Y
9	Equal	Output a 1 for every bit of X and Y that are alike	$\overline{XY}$ or XY
A	Transfer Y	Output a 1 for every 1 in Y	Y
B	AND	Output a 1 for every 1 in X and Y	X and Y
C	ONEs	Output all ONEs	1
D	Insert in X	Output a 1 for every 1 in X or 0 in Y	X or $\overline{Y}$
E	Inclusive OR	Output a 1 for every 1 in X or 1 in Y	X or Y
F	Transfer X	Output a 1 for every 1 in X	X

Table 4. ALU Arithmetic Codes, T = 1

A Field Hexadecimal	Arithmetic Function	Description	Symbolic
0	Increment X	X plus Carry	X+CYIN
1		X or Y plus Carry	X∨Y+CYIN
2		X or Y Not plus Carry Not	$X \vee \overline{Y} + \overline{CYIN}$
3	Carry Skip Test	All ONEs plus Carry	-1+CYIN
4		X plus X and Y Not plus Carry	$X + X \cdot \overline{Y} + CYIN$
5		X or Y plus X and Y plus Carry	X∨Y+X·Y+CYIN
6	Subtract	Subtract Y from X (with or without Carry)	X+Y+CYIN
7		X and Y Not minus 1 plus Carry	$X \cdot \overline{Y} - 1 + CYIN$
8	Masked Add	X plus X AND Y plus Carry	X+X·Y+CYIN
9	Add	X plus Y plus Carry	X+Y+CYIN
A	Conditionally complement Y by X	Complement Y if X=0 and CYIN = 1 Transfer Y if X=-1 and CYIN = 1	$X \vee \overline{Y} + X \cdot Y + CYIN$
B		X and Y minus 1 plus Carry	X·Y-1+CYIN
C	Shift X left	X plus X plus Carry	X+X+CYIN
D		X or Y plus X plus Carry	X+X∨Y+CYIN
E		X or Y Not plus X plus Carry	$X + X \vee \overline{Y} + CYIN$
F	Decrement X	All ONEs plus X plus Carry	X-1+CYIN

CPB

C FIELD, BITS 27 AND 26: CARRY CONTROL

Specifies option of adding or subtracting a Carry-In to the ALU and also controls setting of Carry and Overflow status flip-flops.

If bit T = 0 a logical ALU operation:

C = 0, No change
C = 1, Set Carry Status
C = 2, Clear Carry and Overflow Status
C = 3, Not allowed (results undefined)

If bit T = 1 and an ALU operation with A $\neq$ 2 or 6:

C = 0, No carry in, Carry and Overflow status not changed
C = 1, Carry in, Carry and Overflow status not changed
C = 2, No carry in, Carry and Overflow change enabled
C = 3, Carry in, Carry and Overflow change enabled

If bit T = 1, and an ALU operation with A = 2 or 6:

C = 0, Carry in is a ONE, Carry and Overflow status not changed
C = 1, Carry in is complemented, Carry and Overflow status is not changed
C = 2, Carry in is a ONE, Carry and Overflow status change enabled
C = 3, Carry in is complemented, Carry and Overflow status change enabled

D FIELD, BITS 25 AND 24: DO NEXT ORDER CONTROL

Selects the option of skipping the next micro order either unconditionally or based on the ALU output being all ONEs or the jump condition being met.

If S = 0, 1, 2, or 3 (i.e., bit 35 = 0) :

D = 0, Do next order
D = 1, Do next order if output of ALU is all ONEs
D = 2, Skip next order if output of ALU is all ONEs
D = 3, Skip next order unconditionally

If S = 4, 5, 6, or 7 (i.e., bit 35 = 1):

D = 0, Do next order
D = 1, Do next order if Jump condition is true
D = 2, Skip next order if Jump condition is true
D = 3, Skip next order unconditionally

X FIELD, BITS 23 THRU 20: REGISTER FILE SELECT

Selects one of twelve registers in register file for ALU input and/or to receive output of ALU:

X = 0, Program Counter
X = 1, General Register 1
X = 2, General Register 2
X = 3, General Register 3
X = 4, General Register 4
X = 5, General Register 5
X = 6, General Register 6
X = 7, General Register 7
X = 8, Status Register
X = 9, Instruction Register
X = A, Register A
X = B, Register B
X = C, D, E, F, Literal: FFFF (input only)

F FIELD, BITS 19 AND 18: NEXT ORDER X FIELD SOURCE

Selects source of the address bits for next access to register file. These registers may be selected by the AR and XR fields of the instruction word format, the X field of the microcode, or the least significant bits of an address on the INFIBUS:

F = 0, X field of microcode
F = 1, XR field of instruction ANDed with X field of next micro-order
F = 2, AR field of instruction ANDed with X field of next micro-order
F = 3, Address bits 4 to 1 ANDed with X field of next micro-order

Y FIELD, BITS 17 AND 16: Y INPUT TO ALU SELECT

Selects the R, A or T Registers for input to the ALU. When Y = 3, operates with the M field to enable or disable the transfer of the two microcode literal fields L2 and L1 to the four 4-bit fields of Y:

Y = 0, R register
Y = 1, A register
Y = 2, T register
Y = 3, L Field Control (see M Field)

CPB

M FIELD, BITS 15 THRU 12: MULTI FUNCTION

This field operates with other fields for different functions. When Y = 3, it controls mapping of literals L2 and L1 fields to the ALU's Y input. See table 5. When S = 1 and L2 = 7, it specifies the type of shift to perform. When S = 2, it is part of the branch address. When S = 4 or 5, it specifies conditional jump codes. See table 6. When S = 6 or 7, it specifies a bit position in the T register to be tested.

Table 5. Literal Field Input to ALU, Y = 3

M Field (Hexadecimal)	L2 Enabled	L1 Enabled	L2 Enabled	L1 Enabled
	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
M = 0	Yes	Yes	Yes	Yes
M = 1	Yes	Yes	Yes	No
M = 2	Yes	Yes	No	Yes
M = 3	Yes	Yes	No	No
M = 4	Yes	No	Yes	Yes
M = 5	Yes	No	Yes	No
M = 6	Yes	No	No	Yes
M = 7	Yes	No	No	No
M = 8	No	Yes	Yes	Yes
M = 9	No	Yes	Yes	No
M = A	No	Yes	No	Yes
M = B	No	Yes	No	No
M = C	No	No	Yes	Yes
M = D	No	No	Yes	No
M = E	No	No	No	Yes
M = F	No	No	No	No
NOTE: Bits not enabled are ZERO				

S = 1, L2 = 7, Shift Code:

M = 0, 8 Left arithmetic
M = 1, 9 Left logical, linked
M = 2, A Left logical, open
M = 3, B Left logical, closed
M = 4, C Right Arithmetic
M = 5, D Right logical, linked
M = 6, E Right logical, open
M = 7, F Right logical, closed

S = 2: Bits 13 and 12 of the M field are used with L2 and L1 to specify up to a 10-bit branch address.

Table 6. Conditional Jump Codes, S = 4 or 5

M Field, (Hexadecimal)	Conditional Jump Codes	Symbolic
M = 0	Halt flip-flop set	HBFS
M = 1	Interrupt condition false	NEXT
M = 2	Bit 00 of R Register	R00S
M = 3	Class 0, 4, 8, or 12	$\overline{\text{E13S}}$ $\overline{\text{E12S}}$
M = 4	All ONEs flip-flop set	ONES
M = 5	Carry flip-flop set	CRYS
M = 6	Overflow flip-flop set	OVFS
M = 7	Abort flip-flop set	BAES
M = 8	Loop count complete	EMAX
M = 9	Extended Address	E03S
M = A	Indirect Address	E07S
M = B	Byte mode	E11S
M = C	Class 4 to 7, or 12 to 15	E14S
M = D	Not used	-
M = E	Indirect Address	E07S
M = F	Not used	-

CPB

S = 6 or 7: M field specifies the bit position ($0\text{-}F_{16}$) of the T Register to be tested.

L2 FIELD, BITS 11 THRU 8: LITERAL FIELD 2

When Y = 3, it is a four-bit literal that is gated to the ALU Y input. See table 4. When S = 1, it is a special command. For S = 2 through 7, L2 represents the most significant bits of the control storage branch or jump addresses. For Z = 1 and L1 = 0, 4, 8, or 12, L2 represents the four most significant bits of the jump table address.

S = 1, Special Command:

L2 = 0, Not used
L2 = 1, Clear RBFS
L2 = 2, Load P key
L2 = 3, Select interrupt
L2 = 4, Enable next order C, V
L2 = 5, Enable next order N, Z, O
L2 = 6, Set HBFS
L2 = 7, Shift (shift type specified by M field)
L2 = 8, Reset abort
L2 = 9, Read word
L2 = A, Write word
L2 = B, Not used
L2 = C, Not used
L2 = D, Read with byte allow
L2 = E, Write with byte allow
L2 = F, Not used

S = 2: L2 represents bits 7, 6, 5 and 4 of the 10-bit branch address. Bits 9 and 8 are contained in the M field. Bits 3 thru 0 are contained in L1.

S = 3, 4, 5, 6, 7: L2 represents bits 7, 6, 5 and 4 of the 8-bit jump address. Bits 3 thru 0 are contained in L1.

L1 FIELD, BITS 7 THRU 4: LITERAL FIELD 1

When Y = 3, it is a four-bit literal that is gated to the ALU Y input. For S = 2 thru 7, it represents the four least significant bits of branch or jump addresses. When Z = 1, L1 field specifies the source to be used to modify the L (or M) fields of the next micro instruction, or it specifies which E register field is to be used as the least significant four bits of the data lookup table address (used to modify the next micro-instruction L field).

Z FIELD, BIT 3: LITERAL ENABLE

When Z = 1 this field is used to enable special interpretation of L2 and L1 fields to select a four-bit field from the E register, or other sources, for generation of special literals on the next micro instruction:

L1, Bits 7 and 6 = 0, Select E03 thru E00

L1, Bits 7 and 6 = 1, Select E07 thru E04

L1, Bits 7 and 6 = 2, Select E11 thru E08

L1, Bits 7 and 6 = 3, Select E15 thru E12

L1, Bits 5 and 4 = 0, Table output to L field (bits 11 to 04)
(table address is L2 with selected E field)

L1, Bits 5 and 4 = 1, Interrupt level to L field bits 8 and 7

L1, Bits 5 and 4 = 2, CPU number to L field bits 10, 9

L1, Bits 5 and 4 = 3, Output bits of E (selected by L1 bits 7 and 6)
to M field, (bits 15 thru 12)

W FIELD, BITS 2 THRU 0: WRITE ALU OUTPUT

Selects register file specified in X field and/or one of A, T, or E registers or loop counter to receive the ALU output. For W = 5, 6, or 7, both the register file and A, T, or E register are selected to receive ALU output, respectively. For W = 0 or 4, the ALU 1 signal is copied into the ONEs flip-flop:

W = 0, None
W = 1, A register
W = 2, T register
W = 3, Loop Counter
W = 4, Register file, selected by X
W = 5, Register file selected by X and the A register
W = 6, Register file selected by X and the T register
W = 7, E register and file selected by X

CPB

INTERCONNECT MODULE PIN ASSIGNMENTS

Pin assignments for interconnect modules ICM and IDM are listed in Table 7.

Table 7. CPA-CPB Interconnect Module Pin Assignments

Pin Number	Source*	J1-Axx	Load*	Source*	J1-Bxx	Load*	Pin Number
01	-	-	-	-	-	-	01
02	CPA-7	ALU1-P	CPB-7	CPB-7	ARCK-P	CPA-2	02
03	CPB-9	STAT-N	BCU-2	BCU-5	DNOL-P	CPB-9	03
04	CPB-7	SCM3-N	BCU-3	BCU-2	NEXT-N	CPB-7	04
05	BCU-6, CPA-8	CPU0-P	CPA-8, CPB-6	BCU-6, CPA-8	CPU1-P	CPA-8, CPB-6	05
06	BCU-3	IL0R-N	CPB-6	BCU-3	IL1R-N	CPB-6	06
07	CPB-4	ONLN-P	CPA-2	CPB-7	RE03-N	CPA-5	07
08	CPB-4	M10S-P	CPA-6	CPB-7	WE03-N	CPA-5	08
09	-	-	-	CPB-10	XSET-N	CPA-5	09
10	-	-	-	CPB-4	M20S-P	CPA-5	10
11	CPB-4	M11S-P	CPA-6	CPB-4	M08S-P	CPA-6	11
12	-	-	-	CPB-7	RE47-N	CPA-5	12
13	-	-	-	CPB-7	WE47-N	CPA-5	13
14	CPA-7	LB11-P	CPB-5	-	-	-	14
15	CPB-7	RE8B-N	CPA-5	-	-	-	15
16	CPB-7	WE8B-N	CPA-5	CPA-7	LB09-P	CPB-5	16
17	-	-	-	-	-	-	17
18	-	-	-	-	-	-	18
19	CPB-4	M21T-P	CPA-5	CPB-4	M09S-P	CPA-6	19
20	CPA-7	LB08-P	CPB-5	CPB-4	M06S-P	CPA-6	20
21	CPA-7	LB10-P	CPB-5	CPA-7	LB07-P	CPB-5	21
22	-	-	-	CPB-4	M04S-P	CPA-6	22
23	-	-	-	CPB-4	M07S-P	CPA-6	23
24	CPA-2	A16R-N	CPB-6	CPB-4	M05S-P	CPA-6	24
25	CPA-2	A17R-N	CPB-6	CPB-4	M20T-P	CPA-5	25
26	-	-	-	CPB-4	M32T-P	CPA-7, 8	26
27	-	-	-	CPB-4	M28T-P	CPA-7	27
28	-	-	-	CPB-4	M29T-P	CPA-7	28
29	-	-	-	CPB-4	M31T-P	CPA-7	29
30	-	-	-	CPB-4	M30T-P	CPA-7	30
31	-	-	-	CPA-7	LB03-P	CPB-5	31
32	CPA-7	LB04-P	CPB-5	CPB-4	M21S-P	CPA-5	32
33	CPA-7	LB05-P	CPB-5	CPB-7	SCM2-N	CPA-2	33
34	CPA-7	LB06-P	CPB-5	CPB-4	M13R-N	CPA-8	34
35	-	-	-	CPB-7	TSHF-P	CPA-8	35
36	CPA-4	R00S-P	CPB-7	CPB-9	WOLN-P	CPA-4	36
37	CPB-4	M16S-P	CPA-6	CPA-7	LB02-P	CPB-5	37
38	CPB-4	M17S-P	CPA-6	CPA-7	LB00-P	CPB-5	38
39	CPB-7	STSR-P	CPA-3, 8	-	-	-	39
40	CPA-8	SARC-P	CPB-9	CPA-7	LB01-P	CPB-5	40
41	CPB-4	M12S-P	CPA-3, 6, 8	CPA-4	T15R-N	CPB-6	41
42	CPB-7	STSL-P	CPA-3, 8	CPB-9	RDCK-P	CPA-4	42
43	CPB-4	M26S-P	CPA-8	-	-	-	43
44	-	-	-	CPA-4	T00R-N	CPB-6	44
45	CPB-4	M27S-P	CPA-8	CPB-4	M14S-P	CPA-3, 6	45
46	CPA-3	BIT1-N	CPB-7	CPB-4	M13S-P	CPA-3	46
47	-	-	-	-	-	-	47
48	CPA-8	STRC-P	CPB-9	-	-	-	48
49	-	-	-	CPB-10	CKTR-N	CPA-3	49
50	CPA-7	LB15-P	BCU-2, CPB-5	CPB-4	M15S-P	CPA-3, 6	50
51	CPA-7	LB13-P	BCU-2, CPB-5	-	-	-	51
52	CPA-7	LB14-P	BCU-2, CPB-5	CPA-8	OVFS-P	CPB-6	52
53	CPA-7	LB12-P	BCU-2, CPB-5	CPA-8	CRYS-P	CPA-3, CPB-6	53
54	CPB-9	DALE-N	CPB-9	CPB-9, 10	CKTS-P	CPA-8	54
55	-	-	-	-	-	-	55

*The digits in the Source and Load columns refer to the logic diagram sheet number for the circuit card indicated. The logic diagrams for the CPA and CPB are contained in this bulletin, and for the BCU in maintenance bulletin M1810.

DRAWINGS AND PARTS LISTS

The drawings and parts lists that follow in this bulletin are listed below. Each of the logic diagrams is accompanied by a brief description that explains the purpose of the logic in the system, and definitions of key logic terms that originate on the corresponding diagram.

Drawings or Parts List	Drawing Number	Sheets
Arithmetic and Logic Unit CPA, Circuit Card Assembly	2001002161	1
Arithmetic and Logic Unit CPA, Logic Diagram	LD2001002161-1	1 thru 8
Control Board CPB, Circuit Card Assembly	2001002169	1
Control Board CPB, Logic Diagram	LD2001002169-1	1 thru 11
Interconnect Module ICM, Circuit Card Assembly	2001002166	1
Interconnect Dual Module IDM, Circuit Card Assembly	2001002232	1
Arithmetic and Logic Unit CPA, Parts List	PL2001002161-1	2,3
Control Board CPB, Parts List		
SUE 1110A-1, 1110A-2	PL2001002169-5	8,9
SUE 1111A-1, 1111A-2	PL2001002169-6	10,11
SUE 1112A-1, 1112A-2	PL2001002169-8	12,13
Parts List Notes	PL2001002169	14
Wire List	PL2001002169	15
Interconnect Module ICM, Parts List	PL2001002166-0,-1	2,3
Interconnect Dual Module IDM, Parts List	PL2001002232-1	2

PROCESSOR TIMING

CPB

Processor timing is shown in figures 3 and 4. Figure 3 shows the arithmetic and logic cycle times, figure 4 shows the halt/file access/start sequence. Timing is controlled by a 150-nanosecond tapped delay line as indicated on CPB logic diagram LD2001002169-1, Sheet 10. Refer to sheet 10 and to sheet 8 of the diagram to correlate the signal mnemonics in figures 3 and 4 with the logic.

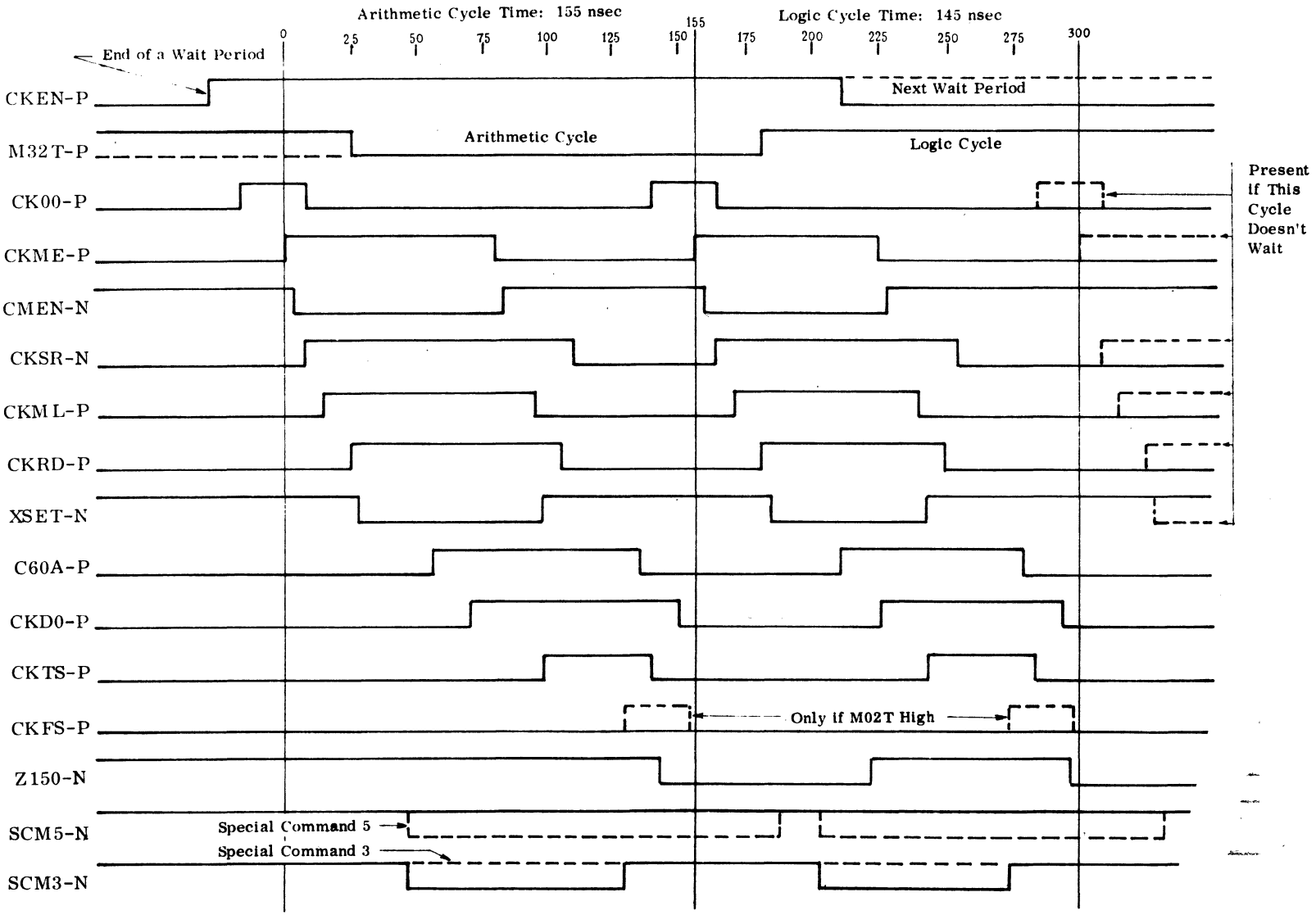


Figure 3. Arithmetic and Logic Cycle Times

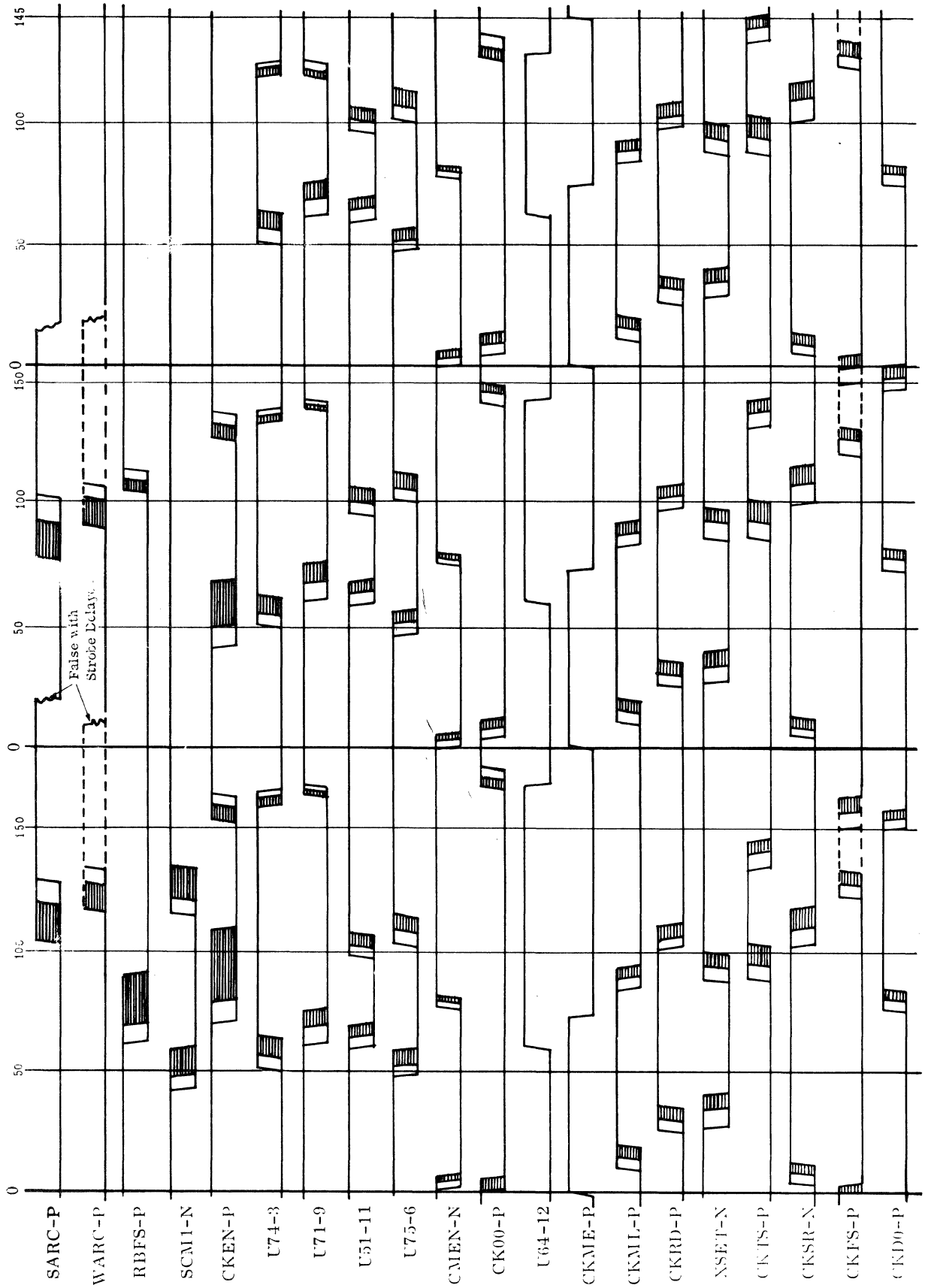
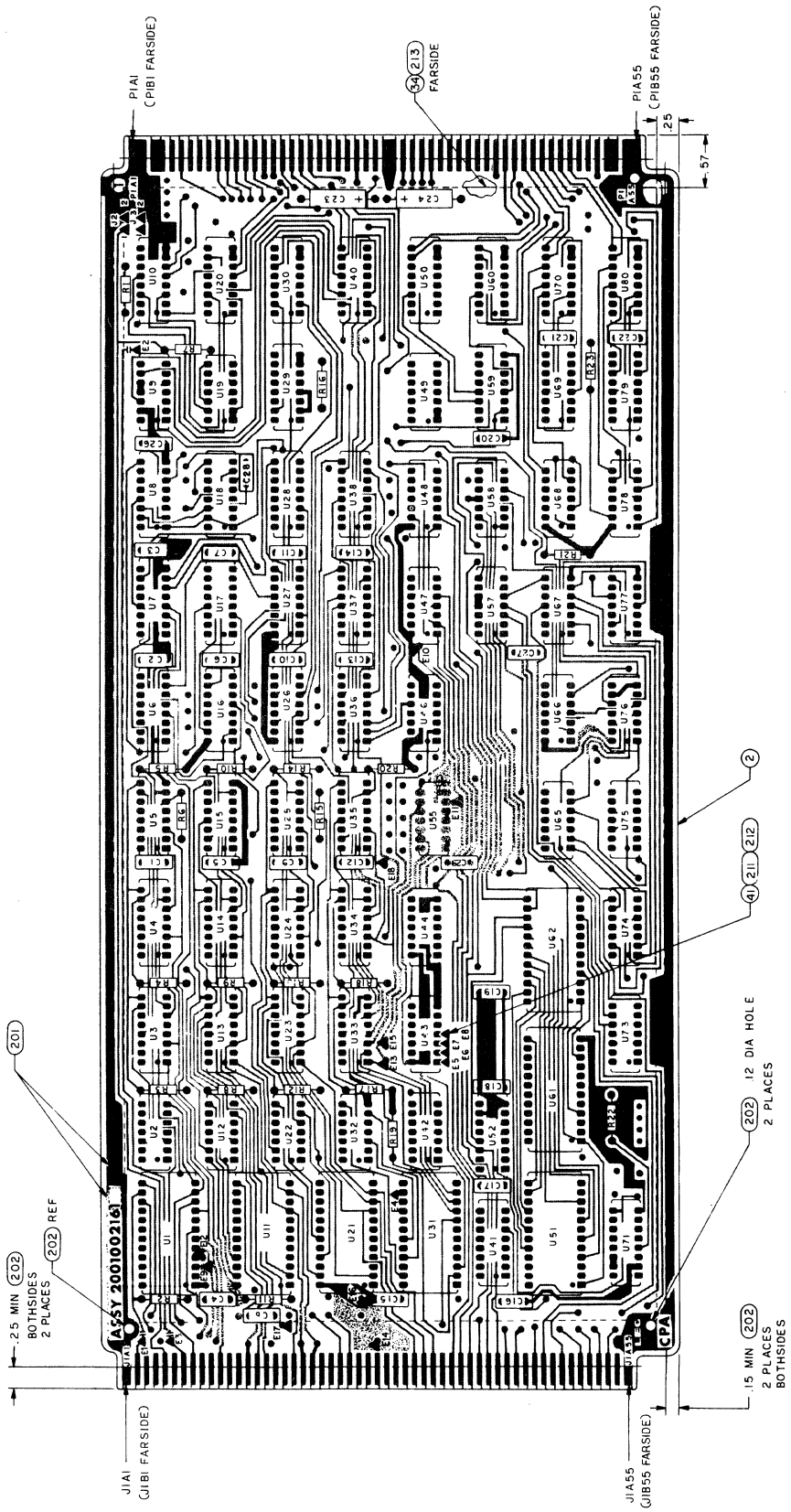


Figure 4. Halt/File Access/Start Sequence Timing

CPB



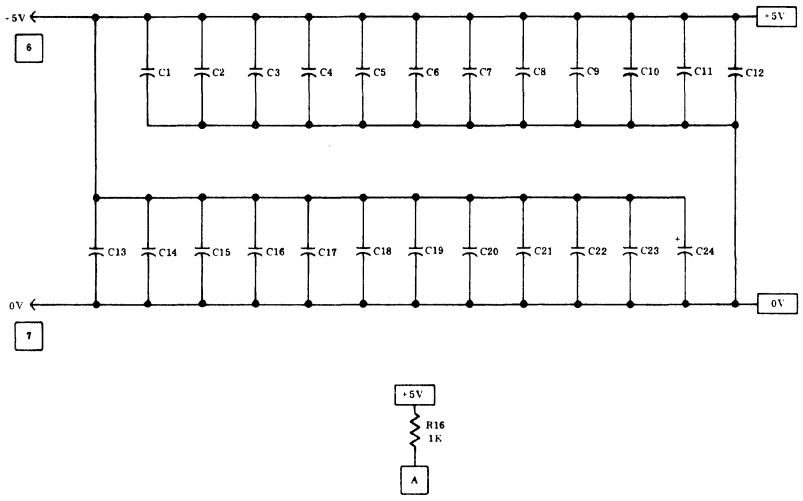
Arithmetic and Logic Unit CPA, Circuit Card Assembly
2001002161, Rev. D, Sheet 1

NOTES:

1. ALL RESISTORS ARE IN OHMS ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1 μf, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33 μf, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST (REFERENCE LIST ON DRAWING 8001800200).
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (14 PIN ICP) PIN 7 0V, PIN 14 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR AND T153 PIN 7 AND 8 0V, PIN 16 +5V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V.

6 +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29 AND B51.

7 0V CONNECTOR PINS ARE: P1-A1, A55, B1 AND B55.



CPB

Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 1 of 8

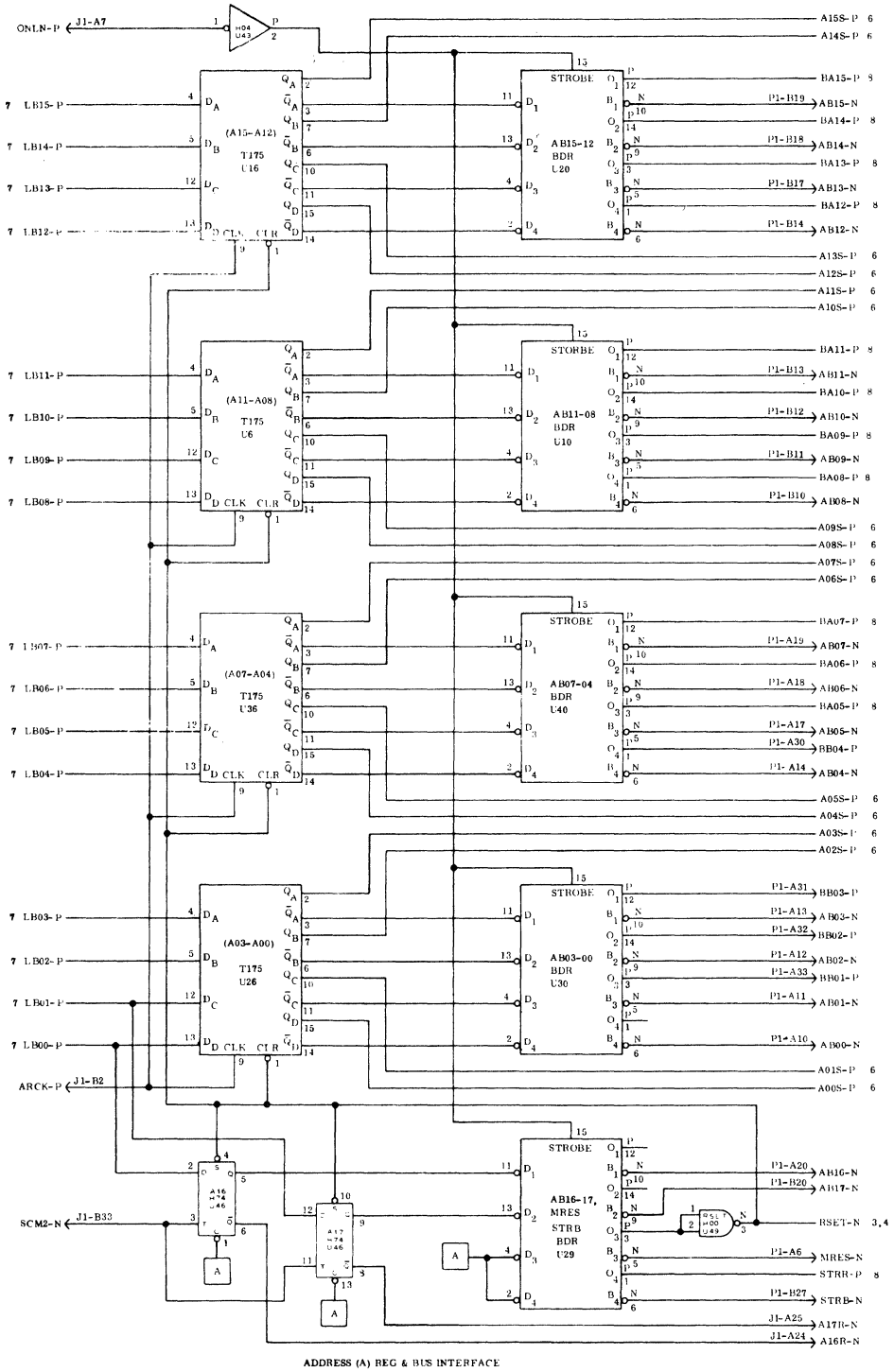
ADDRESS (A) REGISTER AND BUS INTERFACE, CPA (LD2001002161-1, Sheet 2)

The address (A) register serves the following functions:

1. Holds the address sent on the INFIBUS during a memory cycle. The address is gated onto the INFIBUS by ONLN-P which strobes the address bus driver/receivers.
2. Receives outputs from the ALU and provides inputs to the ALU multiplexer. The A register is loaded by ARCK-P.
3. Serves as a working register for the microcode.

KEY SOURCE LOGIC DEFINITIONS

AB00-N thru AB17-N	Negative INFIBUS signals that connect to the address bus drivers/receivers and are used to either send or receive the address.
ARCK-P	Address register clock from CPB, that clocks the address from the ALU into the A register.
A00S-P thru A15S-P	Address register bits sent to the ALU multiplexer inputs.
A16R-N, A17R-N	Protect Key register bits transmitted on INFIBUS lines KEY0 and KEY1, respectively.
BA05-P thru BA15-P	Bus driver/receiver outputs for the 11 high order address bits on the INFIBUS used to recognize when this processor is being addressed by another master device.
BB01-P thru BB04-P	Bus driver/receiver outputs for the four low order bits of a word address used to select the file register (i.e., word) to be accessed when the processor is halted and addressed by another master device such as a control panel.
MRES-N	Master Reset line on the INFIBUS.
ONLN-P	On-Line enabling signal for the address bus drivers that comes from the CPB and is active when the processor is granted the INFIBUS data cycle.
RSET-N	CPA reset signals from master reset on the INFIBUS used to reset all CPA registers except the carry and overflow flip-flops.
SCM2-N	Special Command clock signal to load the Key register flip-flops (A16 and A17) from the two least significant bits of the ALU.
STRB-N	Data cycle strobe on the INFIBUS.
STRR-P	Data cycle strobe received from INFIBUS before the de-skewing delay.



ADDRESS (A) REG & BUS INTERFACE

CPB

Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 2 of 8

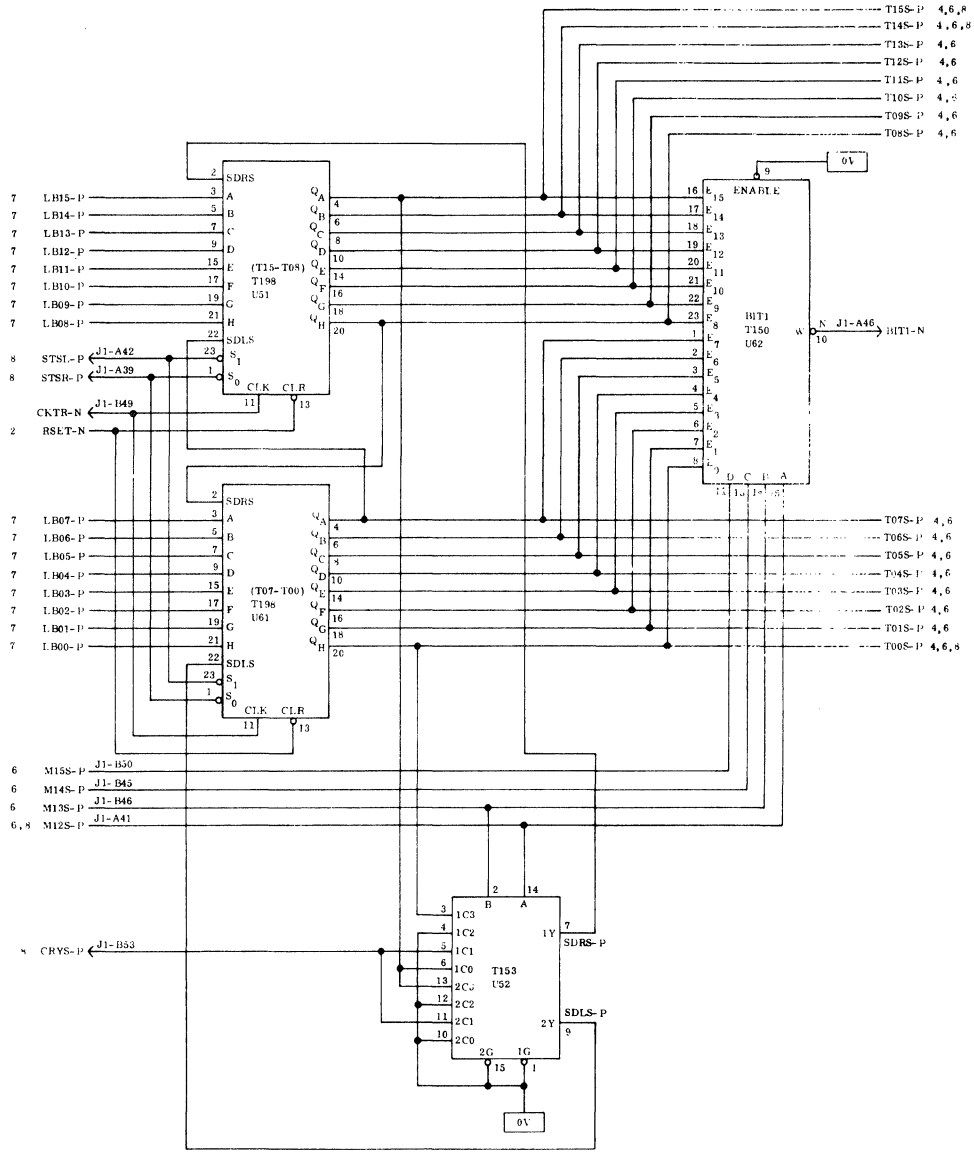
TRANSMIT (T) REGISTER AND BIT TEST, CPA (LD2001002161-1, Sheet 3)

The T-Register holds the data that is sent on the INFIBUS during a memory write cycle. This register may also be selected as an input to the ALU and used for a general working register with shift capability.

The T Register is composed of two coupled 8 bit left/right parallel in/out shift registers (24 pins each). It is clocked by the rising edge of CKTR-N which is free running. Shifting occurs when STSL-P (left) or STSR-P (right) is asserted (low). When neither is asserted, the T-Register outputs remain stable and when both are asserted the ALU outputs (LB00 to LB15) are loaded into the T Register. Shift-in bits are provided at either end by a dual, 4-to-1 multiplexer that selects bit 00, bit 15, the Carry flip-flop or ZERO under control of M12S-P and M13S-P, two of the shift control bits.

KEY SOURCE LOGIC DEFINITIONS

BIT1-N	A bit sampled from the T Register by the 16-to-1 multiplexer. The bit is addressed by M12 through M15 and is used to condition a Jump and Skip in the microcode sequence.
T00S-P thru T15S-P	Transmit Register positive outputs to the ALU 4-Bus Multiplexer and the data inverters feeding the INFIBUS data drivers.
CKTR-N	Clock T Register, a free-running clock to the T Register.
STSL-P, STSR-P	Select T, Shift Left/Right, coded command inputs to designate left shift, right shift, load, or hold.
CRYS-P	Output from the Carry flip-flop used in this logic to allow shifting in the Carry bit.
SDLS-P, SDRS-P	Select Data, Shift Left/Right, the left and right shift inputs to the T Register.
M12S-P thru M15S-P	Control bits from the M Register used as select signals for multiplexers to select the shift-in bits to the T Register or the test output bit for Jump control.



TRANSMIT (T) REG & BIT TEST

CPB

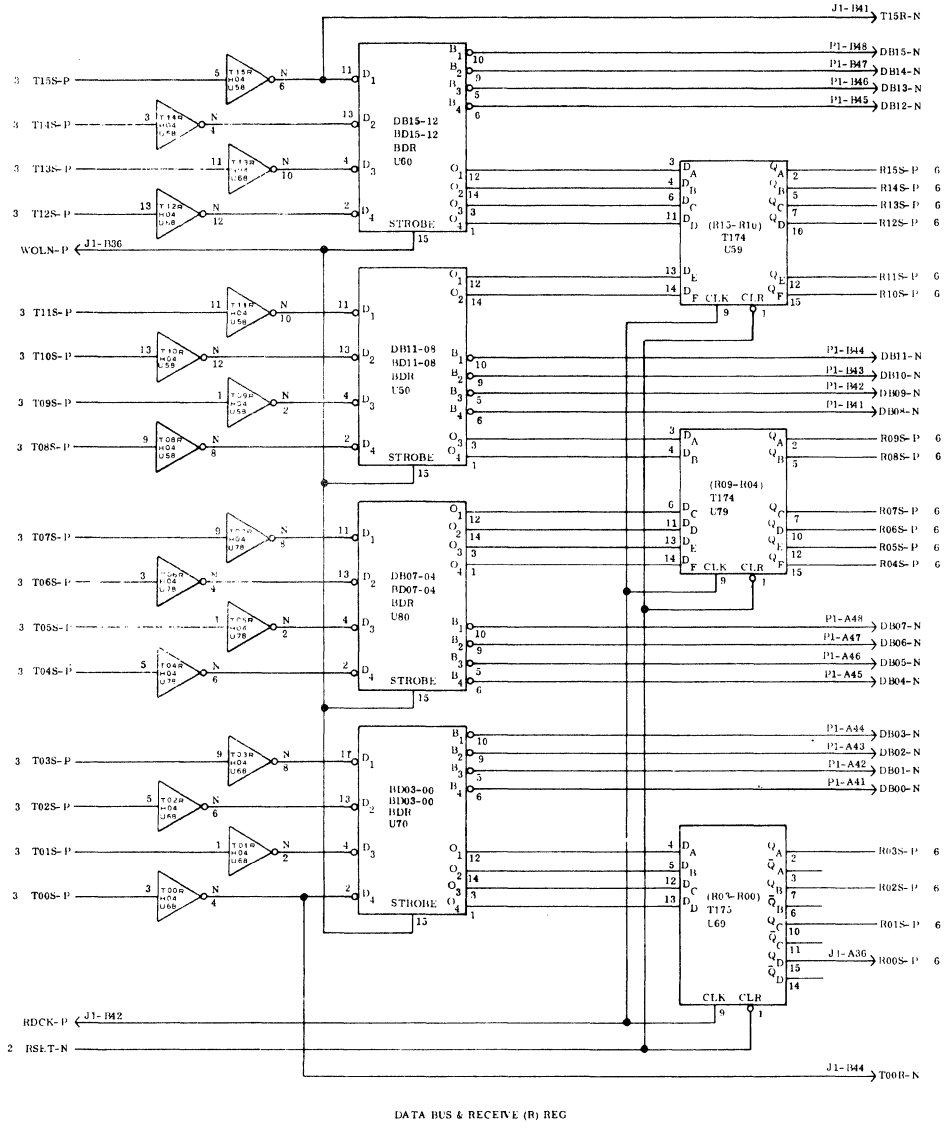
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 3 of 8

DATA BUS AND RECEIVE (R) REGISTER, CPA (LD2001002161-1, Sheet 4)

The receive (R) register holds data received from the INFIBUS during a memory read cycle and may be selected as an input to the ALU. The R Register positive inputs are from the data bus drivers/receivers which interface negatively to the INFIBUS. The inputs to the bus drivers/receivers are through inverters to the T Register positive outputs.

KEY SOURCE LOGIC DEFINITIONS

DB00-N thru DB15-N	INFIBUS data lines driven and received by their respective bus driver/ receivers.
R00S-P thru R15S-P	R-register outputs to the ALU multiplexer. R00S-P also is an input to the test multiplexer.
RDCK-P	Read Clock, the clock for the R register developed by the interface logic from the read data strobe.
T00R-N, T15R-N	Inverted outputs (least- and most-significant T register bits) that are sent to the CPB to provide status information (i.e. odd and negative) from the T register.
WOLN-P	Write On-Line, the enable signal to the bus driver/receivers that places the T-register data on the INFIBUS data lines during a memory write cycle.
T00S-P thru T15S-P	T register bits that represent the data sent on the INFIBUS during a memory write cycle.



DATA BUS & RECEIVE (R) REG

CPB

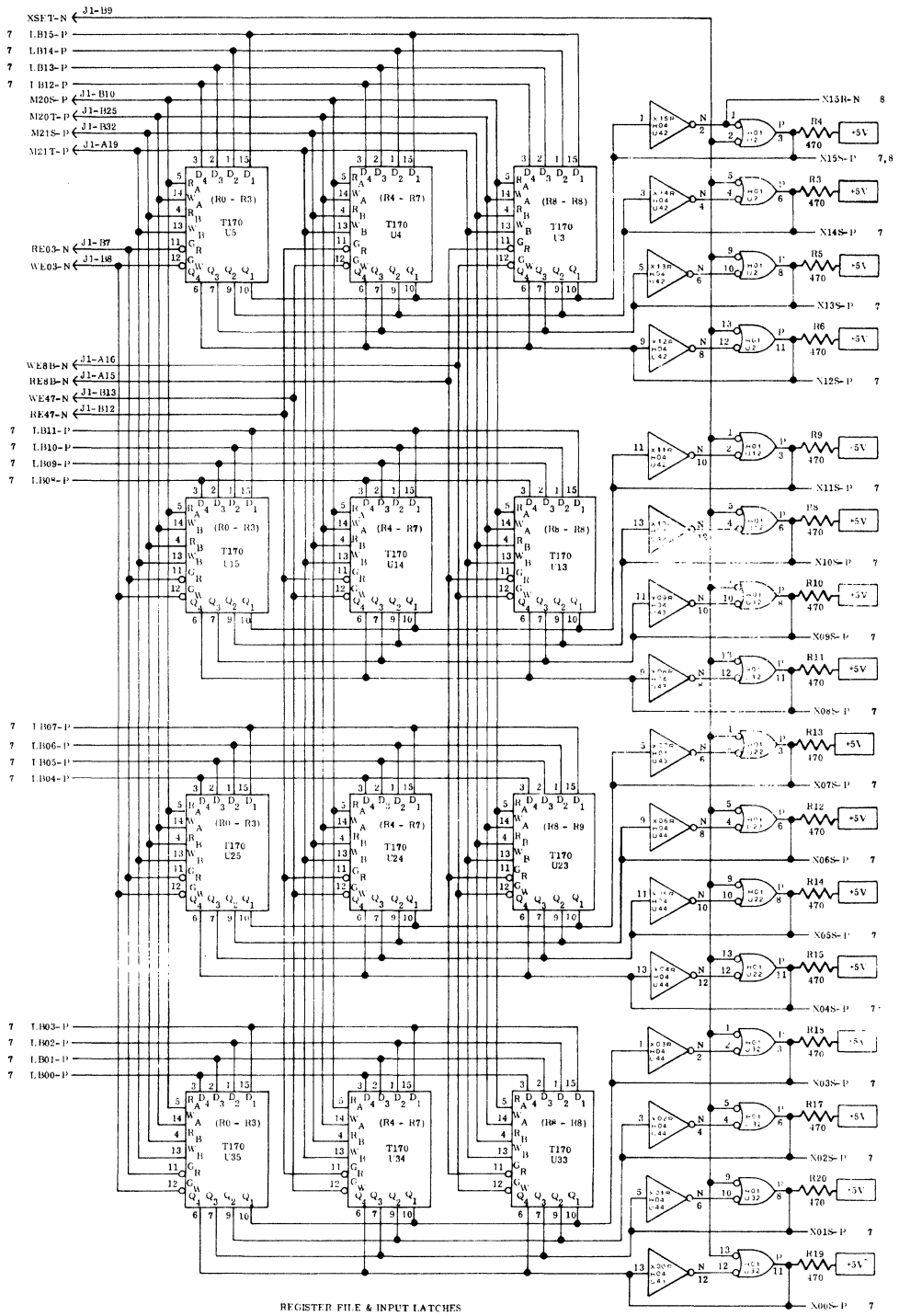
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 4 of 8

REGISTER FILE AND INPUT LATCHES, CPA (LD2001002161-1, Sheet 5)

The register file comprises three sets of four register file components with each component having a four-bit by four-word capacity. Each set of four components has a sixteen-bit by four-word capacity and together the total file capacity is sixteen bits by twelve words. A word is read from the file by enabling one set of components and addressing one its four words. The outputs of the component sets are open collectors that are AND-connected together and applied to the ALU X inputs. Also, an open-collector latch is connected to each output to maintain the low signals at the X input after the read enable is removed from the register file prior to writing into the same word of the file. The latches, which do not insert a delay into the data paths, are released to go high after the X input is needed no longer.

KEY SOURCE LOGIC DEFINITIONS

M20S-P, M21S-P, M20T-P, M21T-P	M register bits from the X field used to address one of four words in the register file either to be read (M20S-P, M21S-P early) or to be written into (M20T-P, M21T-P late).
RE03-N, RE47-N, RE8B-N	Read enable bits 0 to 3, 4 to 7, and 8 to B decoded from M22 and M23 (X field - early) which enables the read function in one of the three sets of file register components.
WE03-N, WE47-N, WE8B-N	Write enable bits 0 to 3, 4 to 7, and 8 to B decoded from M22 and M23 (X field - late) which enables the write function in one of the three sets of file register components.
XSET-N	The latch control term to either allow the latched (low) signal to unlatch (X SET low) or to keep them latched (X SET high).
X00S-P thru X15S-P, and X15R-N	The X inputs to the ALU composed of the common AND connection of the open collector outputs of the files and latches. X15R-N is the inversion of the sign bit X15S-P. Both of these signals are used to control the overflow logic.



REGISTER FILE & INPUT LATCHES

CPB

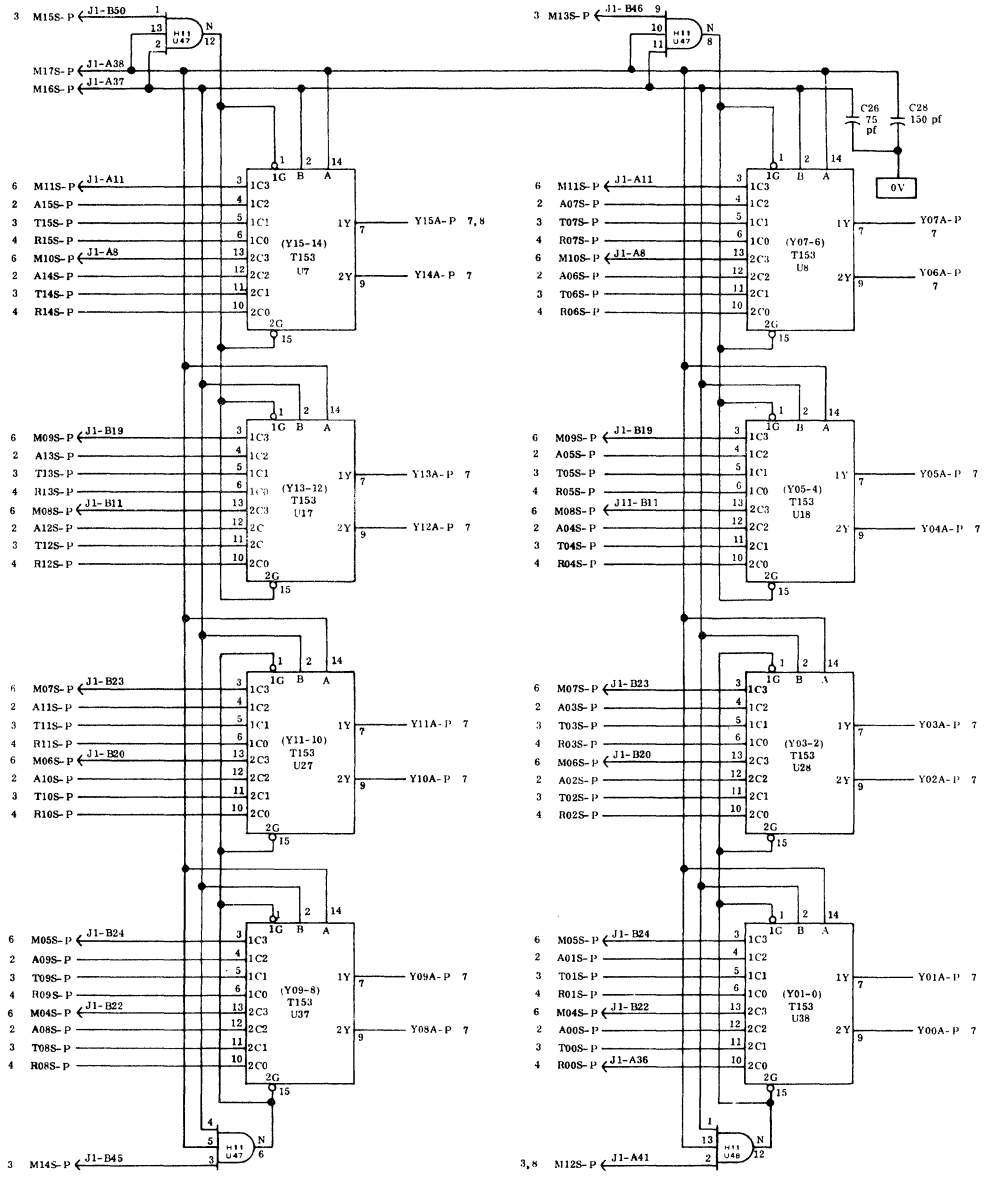
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 5 of 8

ALU INPUT MULTIPLEXER, CPA (LD2001002161-1, Sheet 6)

The Y inputs to the ALU are taken from eight, dual 4-to-1 multiplexers. The multiplexers, under control of bits 16 and 17 in the M Register, select either one of registers R, A, T, or a zoned literal value from M register field L1 and L2 (bits 4 to 7 and 8 to 11, respectively). Each multiplexer output is enabled in four-bit zones by four AND gates so that all outputs are enabled if any one of registers R, A, or T is selected. However, if the literal fields are selected, the enabling is under control of M field, bits M12 to M15. Outputs of multiplexers not enabled are zero.

KEY SOURCE LOGIC DEFINITIONS

M16S-P, M17S-P	Y field of the M Register that selects the multiplexer input and enables the multiplexer if the literal is not being selected (by forcing the AND enable gate output low).
M12S-P thru M15S-P	M field of the M Register that controls enabling of the multiplexers when the literal value is being selected. For a multiplexer to be not enabled, the literal value must be selected and the corresponding mask bit must be high.
M04S-P thru M11S-P	L1 and L2 fields of the M register used here as an 8-bit literal value for a multiplexer input. The 8 bits are sent to both the most- and least-significant inputs to be enabled under zone control.
R00S-P thru R15S-P, T00S-P thru T15S-P, A00S-P thru A15S-P	The Positive outputs of each of the three working registers R, T, and A used as data to the other three multiplexer inputs.
Y00A-P thru Y15A-P	The positive multiplexer outputs going to the ALU Y inputs. Y15A-P is also used by the overflow detection logic.



ALU INPUT MULTIPLEXER

CPB

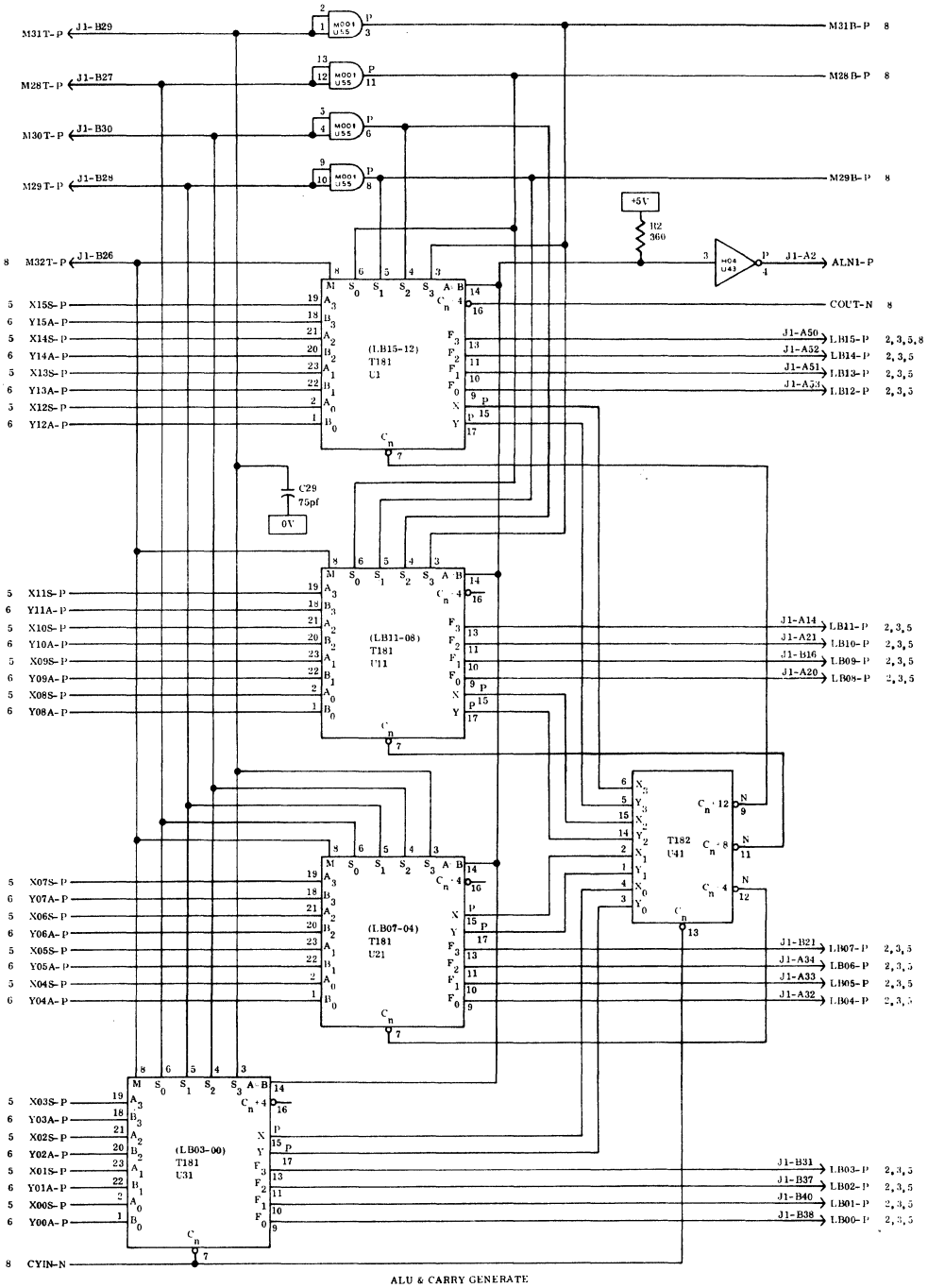
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 6 of 8

ALU AND CARRY GENERATE, CPA (LD2001002161-1, Sheet 7)

The ALU is the function generator for the processor combining two 16-bit inputs, X and Y, and producing a 16-bit result. Sixteen logical and 16 arithmetic (i.e. involving carry logic) combinations can be made. The type of combination is selected by 5 control inputs. A carry input is accepted and a carry output generated with carry preparation being enhanced by U41, a look-ahead carry generator. An output that indicates when the ALU outputs are all high is used to detect zero and equality under certain algorithms.

KEY SOURCE LOGIC DEFINITIONS

M32T-P	The control input that determines the operation mode: high for logical and low for arithmetic.
M28T-P thru M31T-P, M28B-P thru M31B-P	The control inputs that select the function being generated. The repeaters (MxxB-P) are added to distribute the signal loading and also to drive carry selection, carry store, and overflow detection logic.
CYIN-N	Negative carry input to both the least-significant bit and the carry look-ahead logic.
X00S-P thru X15S-P Y00S-P thru Y15S-P	The ALU function inputs from the register file (X) and the A, T, or R register and literal multiplexer (Y). Y multiplexer for the A, T, or R registers or literal.
LB00-P thru LB15-P	The ALU outputs which constitute a logic bus to distribute the ALU results to the file register and/or one of registers A, T, or E (via the back connector). LB12-P thru LB15-P is also picked up by the BCU from the back connector to store the interrupt enable bits whenever file register 8 (status) is written into. LB15-P also is used by the overflow detection logic.
COUT-N	The negative carry output used to store carry results and to detect overflow.
ALU1-P	The cumulative signal generated by the open collector outputs of all the ALU chips indicating when all the ALU outputs are ONEs (high). It is used by the CPB to control skips and jumps and provide status information.



CPB

Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 7 of 8

CARRY AND OVERFLOW, CPA (LD2001002161-1, Sheet 8)

The carry and overflow logic may be affected by arithmetic, logic, or shift operations. Set or reset conditions are combinations of shift control and ALU arithmetic or logic controls. Both operations can occur simultaneously. Also, the same timing signal (CKTS-P) is used on the DC inputs and the clock input, with clocking on the trailing edge.

The following are normal modes of control:

1. LOGIC MODE — M26 sets carry.
2. LOGIC MODE — M27 resets carry and overflow.
3. ARITHMETIC MODE — M27 enables carry load and overflow detection.
4. SHIFT MODE — Either arithmetic or linked shift enables carry load; also, left shift enables overflow detection. Overflow can occur on logical left linked shift. (ALU code 'OF', logical pass X, supresses arithmetic overflow logic.)

SLAVE ADDRESS RECOGNITION, CPA (LD2001002168-1, Sheet 8)

The address lines are monitored to recognize when the processor address space is accessed. The J2 and J3 links are conditionally grounded to detect the number (0, 1, 2, or 3) to which this processor responds. These links are grounded also by the BCU so that the processor which is the CPU, is always addressed as processor ZERO.

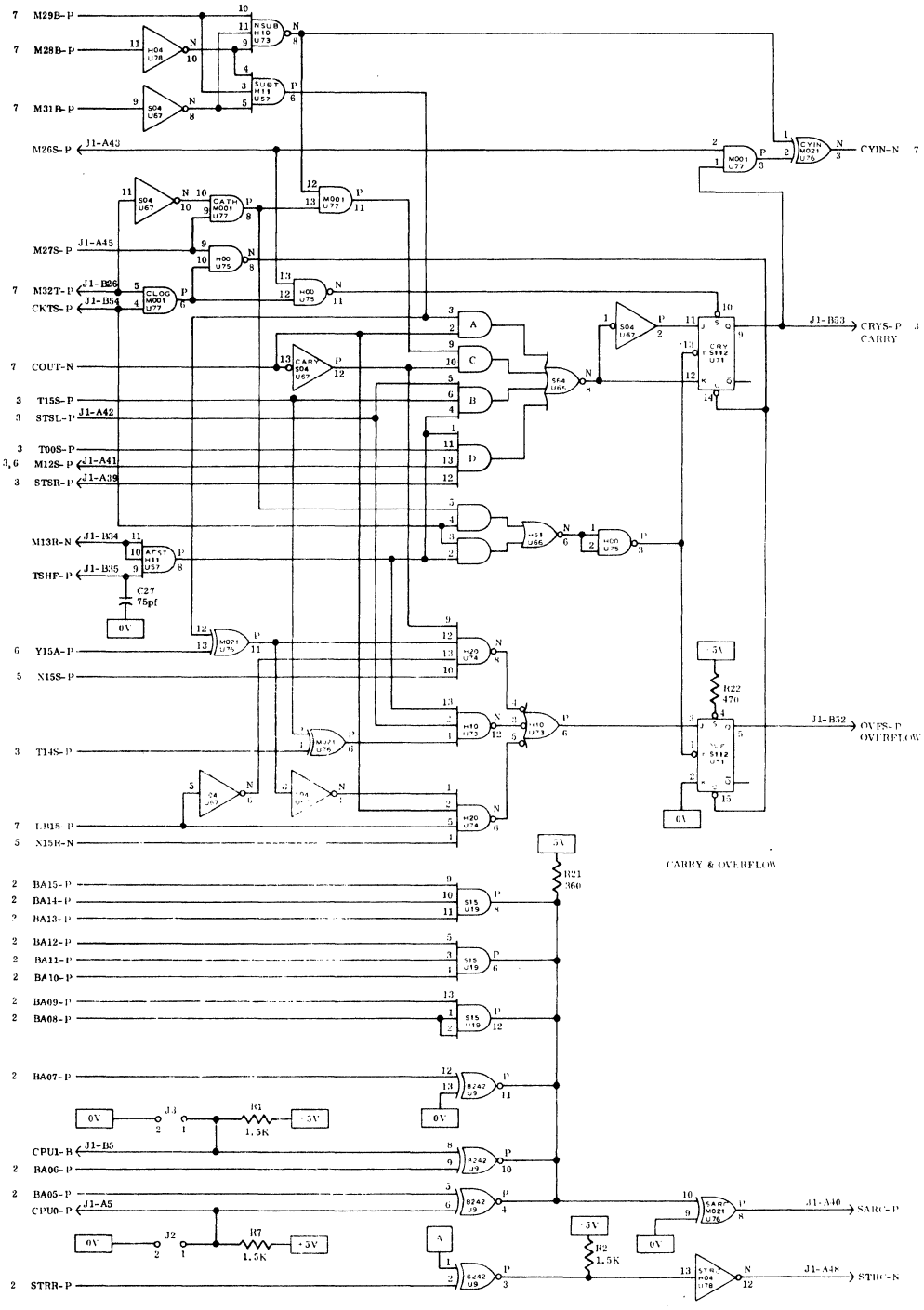
KEY SOURCE LOGIC DEFINITIONS

Carry and Overflow

CKTS-P	Clocks ac and dc inputs to both carry and overflow.
CYIN-N	Negative carry input to the ALU logic derived under control of M-Register bits 26, 28, 29 and 31, and the state of the carry flip-flop. Normally, CYIN-N is either ZERO or carry true based on M26S-P (0 or 1, respectively); but when the ALU function code is 2 or 6 (subtract modes), then CYIN-N is either ONE or carry false, respectively.
CRYS-P	Carry flip-flop true output that may be set by M26S-P or reset by M27S-P during a logic cycle (M32T-P = 1); or it may be loaded from the carry output (COUT-N) by M27S-P during an arithmetic cycle (M32T-P = 0). Carry is loaded also during an arithmetic or logical linked shift cycle with data taken from the MSB or LSB of the T register based on left or right shift respectively.
OVFS-P	Overflow flip-flop true output that is reset (along with carry) by M27S-P during a logic cycle. This is the only reset for overflow. Overflow may be set only by either an arithmetic (logical linked) left shift where bits 15 and 14 differ in the T Register, or it may be set by an arithmetic operation when M27S-P is enabling the overflow detection logic. An overflow condition for the add mode occurs either when X, Y, and carry out are all ZERO and the sum is ONE (all for bit 15), or when X, Y, and carry out are all ONE and the sum is ZERO. For subtract mode, overflow occurs either when X and carry out are ZERO, and Y and the sum equal ONE, or when X and carry out are ONE, and Y and the sum equal ZERO.

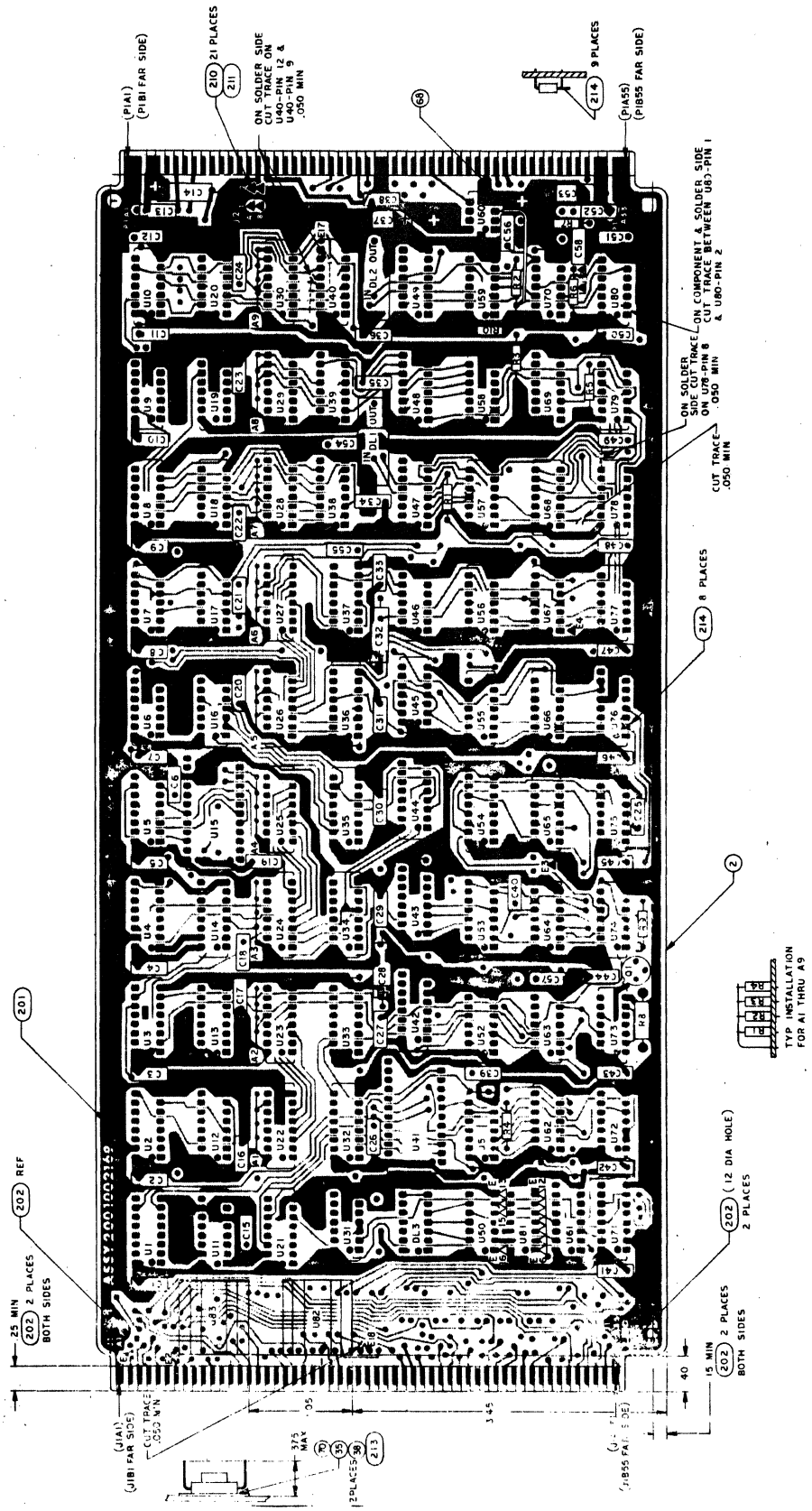
Slave Address Recognition

SARC-P	Positive signal showing recognition of the processor's address space on the address bus.
STRC-N	The delayed negative strobe output from the INFIBUS which is sent to the CPB with SARC-P to initiate a slave memory cycle when both are asserted.



CPB

Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 8 of 8



Control Board CPB, Circuit Card Assembly
2001002169, Rev. D, Sheet 1

NOTES: UNLESS OTHERWISE SPECIFIED

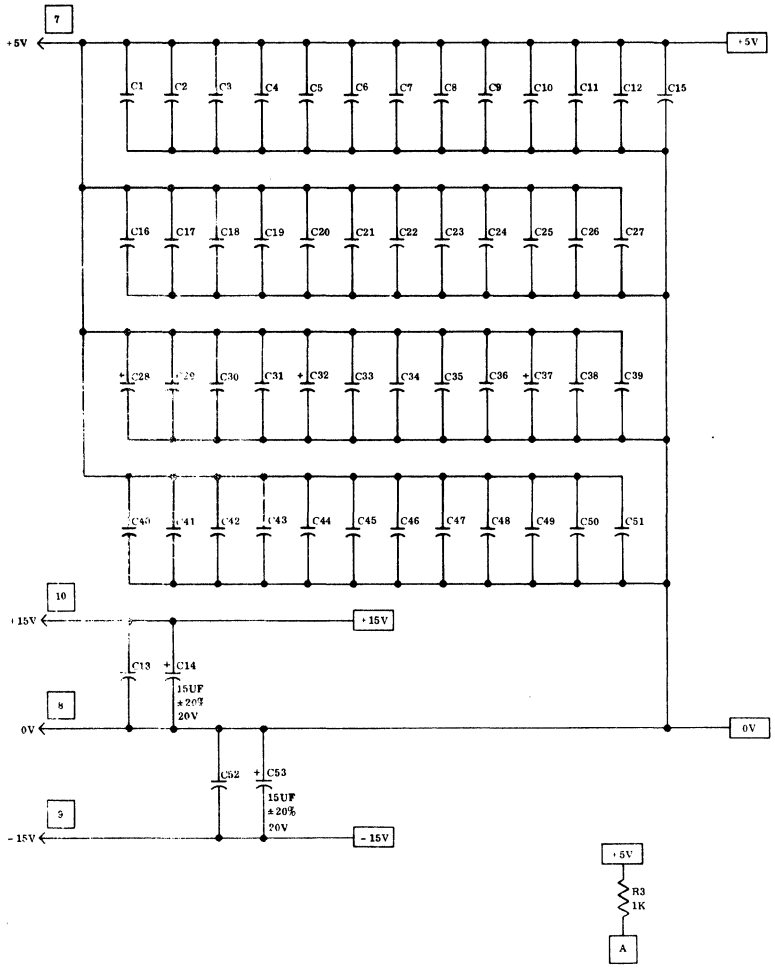
1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL RESISTOR CLUSTERS ARE 470 OHMS, ±2%, 1/8W.
3. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
4. ALL POLARIZED CAPACITORS ARE 33UF, ±20%, 10V.
5. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
6. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR, PIN 7 AND 8 0V, PIN 16 +5V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V.

7 +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51.

8 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55.

9 -15V CONNECTOR PINS ARE: P1-A52, A53, B52, B53.

10 +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4.



CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 1 of 11

SEQUENCE COUNTER AND ROMS 1 THRU 9, CPB (LD2001002169-1, Sheets 2 and 3)

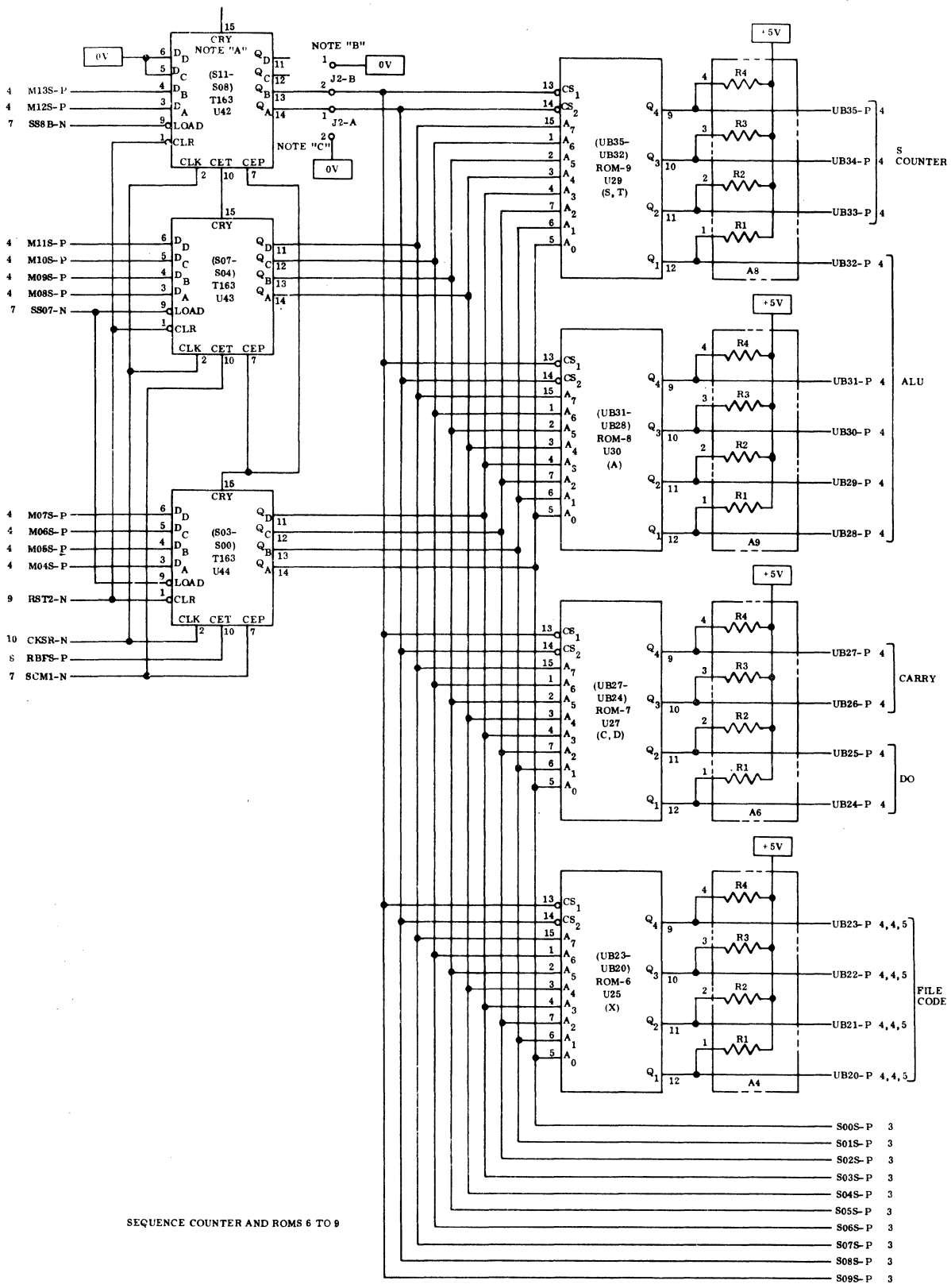
Sheet 2 shows the S register and most significant 4 ROMs; sheet 3 shows the least significant 5 ROMs. Jumper J2-A1,A2 and J2-B1,B2 are installed on SUE 1110 circuit cards to accommodate 8-bit addressing and U42 may not be installed. On SUE 1111 and 1112 circuit cards, U42 is installed and jumper J2-A1,A2 is removed, thereby allowing 9-bit ROM addressing. The ROMs are each 4 bits by 256 words for model 1110 or 512 words for models 1111 and 1112.

The S register is a 12 bit (or 8 bit) counter that normally addresses the ROM sequentially. However, a microcode jump occurs when the S register is loaded from the L1 and L2 (and sometimes M) fields. Also the counter stops incrementing when the Run flip-flop is turned off by a microcode hold (Special Command 1).

KEY SOURCE LOGIC DEFINITIONS

S00S-P thru S09S-P	Sequential S counter outputs used to address and enable the ROM control memory.
SCM1-N, RBFS-P	The two inputs that control counter incrementing. If either signal is low, the counter does not increment.
CKSR-N	The counter clock used for both incrementing and loading.
SS07-N	Used to load the low order 8 bits (L1 and L2 fields, M04 thru M11) on class codes 2 thru 7 (Jump and Conditional Branch).
SS8B-N	Used to load the high order 2 bits (2 LSB's of M field, M12 and M13) on class code 2 (Jump).
UB35-P thru UB00-P	All open collector ROM outputs which go to the M register (sheet 4); many of these ROM outputs may be modified by another open collector output and tied with them.
UB30-P, UB28-P, UB02-P	Tied to some NAND gates to the INFIBUS to modify the micro-command executed while Halted to provide appropriate response to a read or a write request addressing the processor.
UB23-P thru UB20-P	Connected to a 3-to-1 multiplexer that allows the file selection to be modified by either the E register or INFIBUS address lines.
UB11-P thru UB04-P	Connected to 2 table ROMs and some multiplexers to allow modification of the literal fields (L1 and L2) by status information or by tabled information.
UB15-P thru UB12-P	Connected to a multiplexer to allow Branch condition or Shift control (M field) to be controlled from the E register.

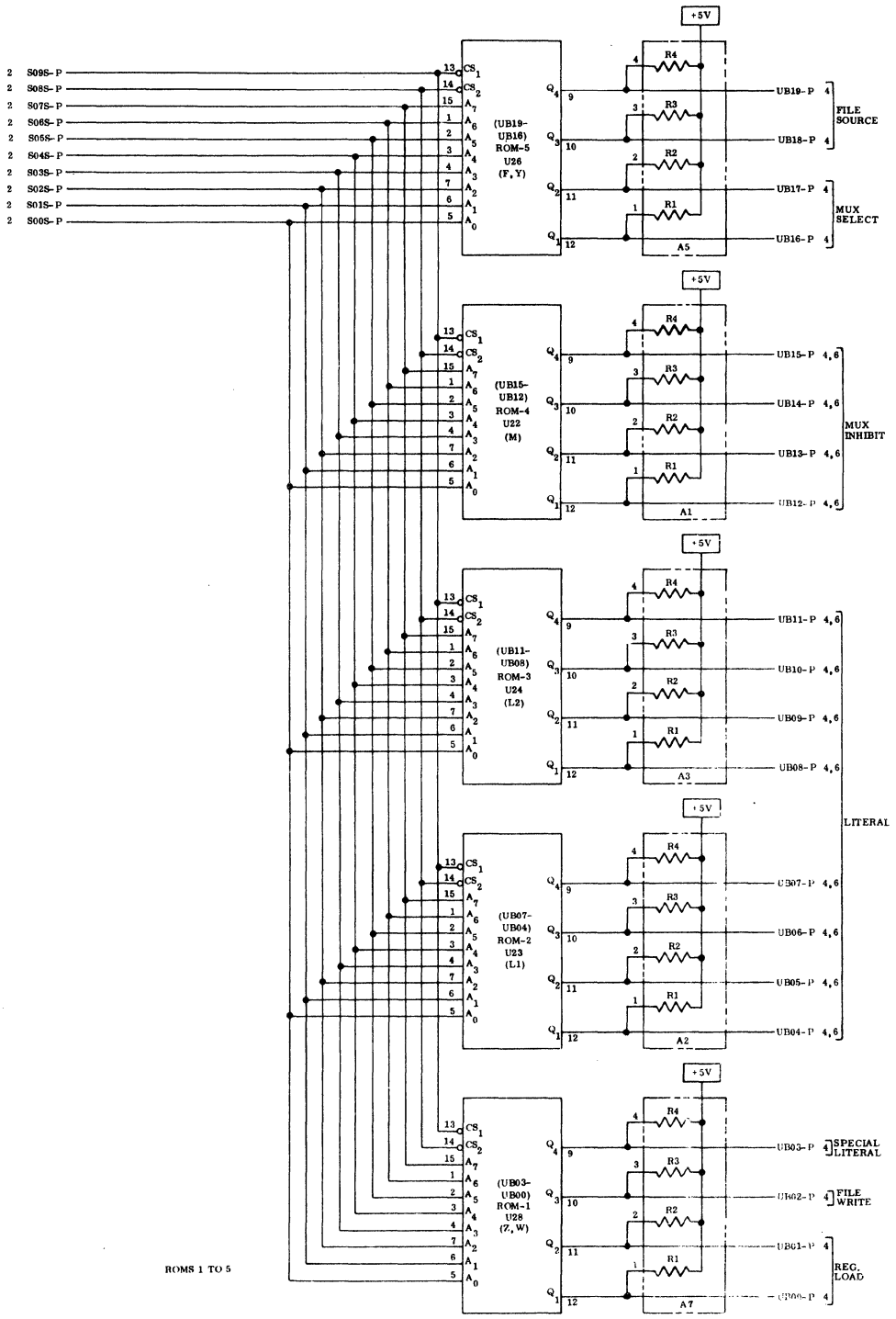
NOTE A: THIS CHIP IS INSTALLED FOR ROM SIZES OF 512 OR 1024 WORDS.
NOTE B. THIS JUMPER IS INSTALLED FOR ROM SIZES OF 256 OR 512 WORDS.
NOTE C: THIS JUMPER IS INSTALLED FOR ROM SIZES OF 256 WORDS.



SEQUENCE COUNTER AND ROMS 6 TO 9

CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 2 of 11



CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 3 of 11

MICRO-INSTRUCTION (M) REGISTER, CPB (LD2001002169-1, Sheet 4)

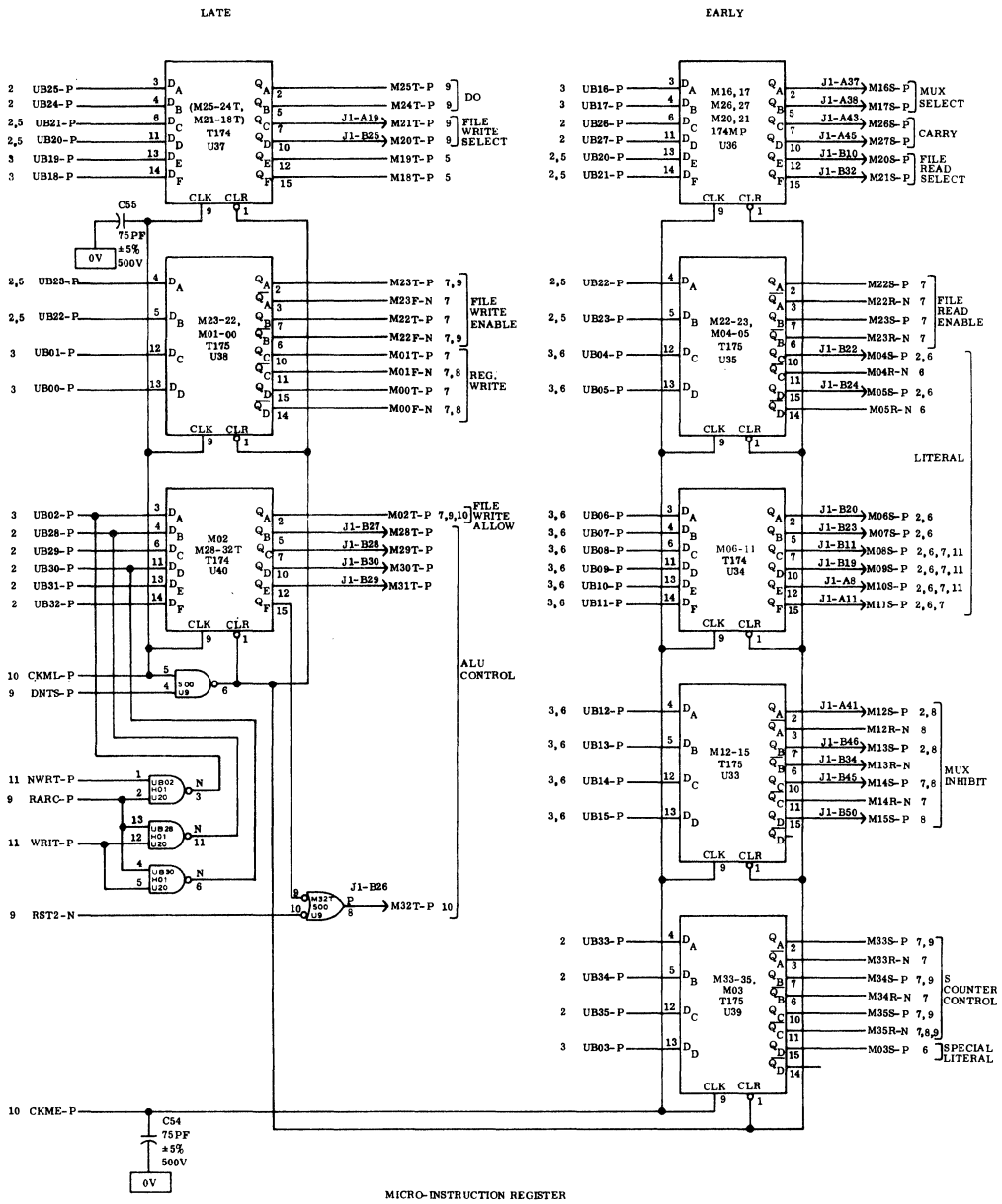
The micro-instruction register is divided into two parts, an early section clocked by the leading edge of CKME-P and a late section clocked by the leading edge of CKML-P (about 20 nanoseconds later). Functions which must be decoded quickly (such as the read file address) are driven by the early section, and functions which must be maintained late in the cycle (such as the write file address) are driven by the late section. The UB lines are the inputs to this register which contains D type flip-flops. Because the file read address and the file write address are derived from the same microcode field, UB20-P thru UB23-P drive inputs of both the early and late sections of the M register. When the DNTS-P signal from the DONT flip-flop is asserted, CKML-P also resets the entire M register by the DC clear inputs.

The following diagram shows the M register bits in each section, and which of the M register flip-flops have complementary outputs available (D) and which have only the singular outputs (S). The diagram also shows field definitions.

3			3	2						2	1								1	0								0	Bit
5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	Number
D	D	D						S	S			D	D	S	S			S	S	D	D	D	D	S	S	S	S	S	S	D	D	D				EARLY (S)
			S	S	S	S	S			S	S	D	D	S	S	S	S																S	D	D	LATE (T)
S			T	A				C		D		X				F		Y		M				L2				L1			Z	W				FIELD CODE

KEY SOURCE LOGIC DEFINITIONS

M35S-P thru M33S-P, M35R-N thru M33R-N (S Field)	Dual rail outputs decoded to control loading of the S counter and enabling the Special Command logic.
M32T-P (T Field)	Derived from a NAND gate giving the OR of the master reset signal (via RST2-N) and the buffered negation of the ROM output from bit 32 (via U40-15). This forces all machine cycles to be logical during reset since this signal controls the logic/arithmetic mode in the ALU's and in the clock generating logic.
M31T-P thru M28T-P (A Field)	Controls the function in the ALU's on the CPA. They also drive repeaters that share the ALU control load and help control the carry and overflow logic.
M27S-P, M26S-P (C Field)	Controls the carry and overflow logic on the CPA.
M25T-P, M24T-P (D Field)	Controls the logic allowing the DONT flip-flop to be set which gives the skip capability to the microcode.
M23S-P thru M20S-P, M23R-N thru M20R-N (early X Field)	Decoded to read enable the file (23 and 22) and to select the word (21 and 20) to be read from the Register file.
M23T-P thru M20T-P, M23F-N thru M20F-N (late X Field)	Decoded to write enable the file (23 and 22) and to select the word (21 and 20) to be written back to the register file if the file write bit (M02) is on.
M19T-P, M18T-P (F Field)	Used to enable and select inputs to a multiplexer that provides X field modification of the next micro-instruction.
M17S-P, M16S-P (Y Field)	Used to enable and select inputs to the Y input multiplexer for the ALUs.
M15S-P thru M12S-P, M15R-N thru M12R-N (M Field)	Used to select a test condition, address a bit in the T register to test, control the type of shift, select the ZERO zones when using a literal value, and give the two most significant bits of a jump address.
M11S-P thru M04S-P (L2 and L1 Fields)	Used to provide literal values, Jump and Branch addresses, select a special control function (L2), and select a Z control modification of the next micro-instruction.
M03S-P (Z control bit)	Used to enable special modification logic for the M, L2, or L1 fields of the next micro-command.
M00T-P thru M03T-P, M00F-N thru M01F-N (W Field)	Specifies whether or not to write into the file (M03) and/or which of registers T, A, or R to write into (M02, M01).
RARC-P, NWRT-P, WRIT-P	Control modification of the ALU operation and the file write enable to facilitate reading and writing into the file register via the INFIBUS while the processor is halted.



CPB

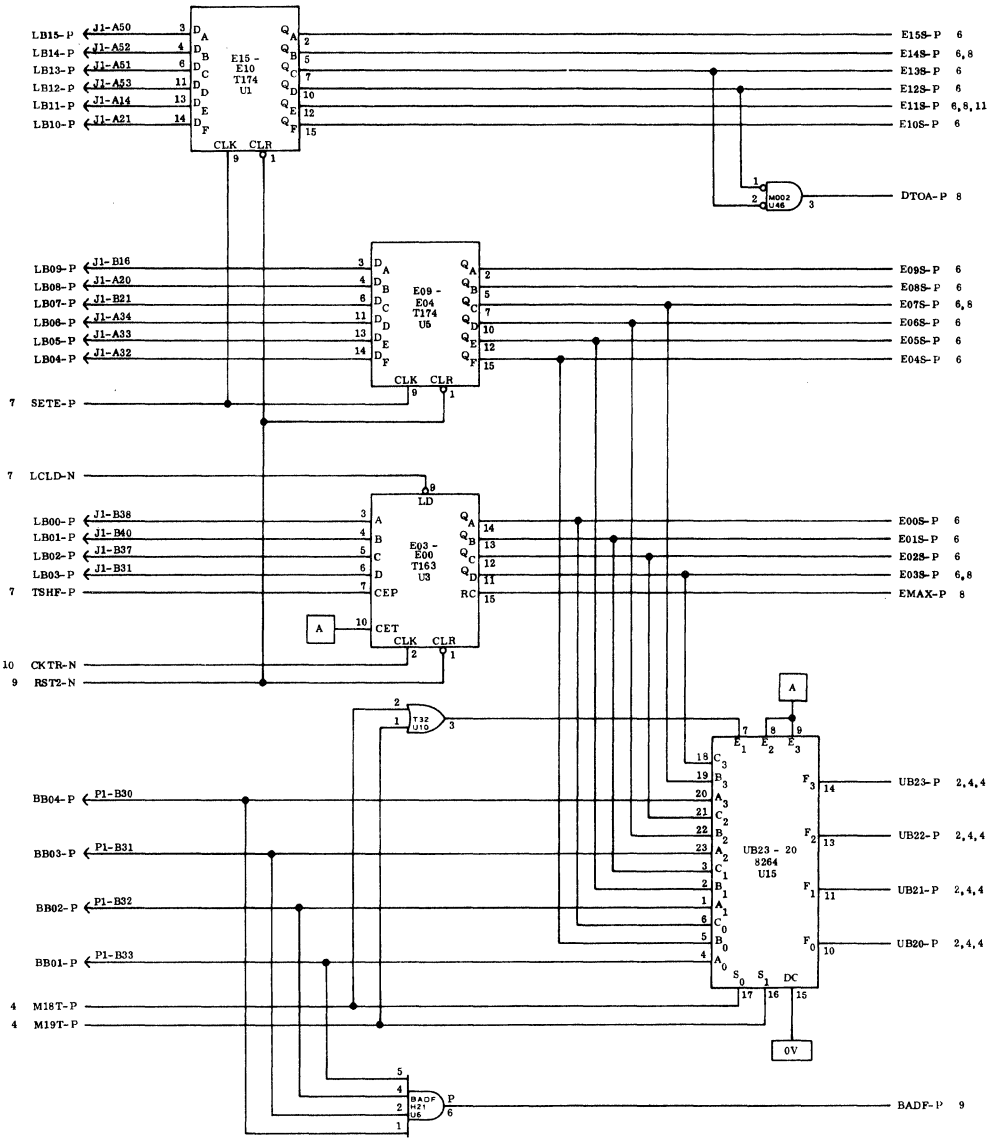
Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 4 of 11

E REGISTER, CPB (LD2001002169-1, Sheet 5)

The E register holds a duplicate of the target instruction to be emulated. Many of its active outputs may be interrogated by a test multiplexer. It is also multiplexed to modify the X or M fields, or to address the table ROM. Bit 11 conditionally controls byte mode memory cycles. The four least significant bits are in a counter component and may be used to control shifts, etc. The maximum value of the counter may also be tested.

KEY SOURCE LOGIC DEFINITIONS

EMAX-P	An input to the test multiplexer indicating when the counter has reached maximum value (i.e. E00 thru E03 are all 1).
DTOA-P	An input to the test multiplexer indicating both E12S-P and E13S-P are low. It is used to differentiate target instruction class codes 0, 4, 8, and A from the rest.
BADF-P	Helps to indicate when register F is being addressed by the INFIBUS so that the control register can be accessed.
E00S-P thru E15S-P	The outputs of the E register going to various steering and test multiplexers.
UB20-P thru UB23-P	The open collectors of the X field input to the M register. The multiplexer (U15) selects 1 of 2 fields from the E register, or 4 low order word address lines from the INFIBUS, or nothing to modify the X field.
SETE-P	The clock to load the 12 most significant bits of the E register from the ALU outputs when M00 thru M02 are all true.
LCLD-N, CKTR-N	The enable and the clock respectively, to load the 4 least significant bits of the E register from the ALU outputs when M00 and M02 are both true.
TSHF-P	The count enable to count up the 4 least significant bits of the E register during a shift operation.



EMULATION INSTRUCTION REGISTOR
AND X FIELD MODIFICATION MULTIPLEXER

CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 5 of 11

Z MODIFICATION AND SPECIAL COMMANDS 4 AND 5, CPB (LD2001002169-1, Sheet 6)

One of four special functions can be enabled by the Z field, bit M03. The particular function is selected by M04 and M05.

Function 3 provides modification of the next M field (M12 to M15) by the output of a multiplexer selecting (under control of M06 and M07) one of the four hexadecimal fields from the E register.

Function 0 uses the same multiplexer output to address 1 of 16 words from a page in a table ROM (U12 and U13). The specific page (1 of 16 in the table) is explicitly addressed by M08 thru M11 in the M register. The table ROM output modifies the L2 and L1 fields of the next micro-instruction.

Function 1 modifies M07 and M08 of the next micro-instruction with the current I/O interrupt level coming from the CPU.

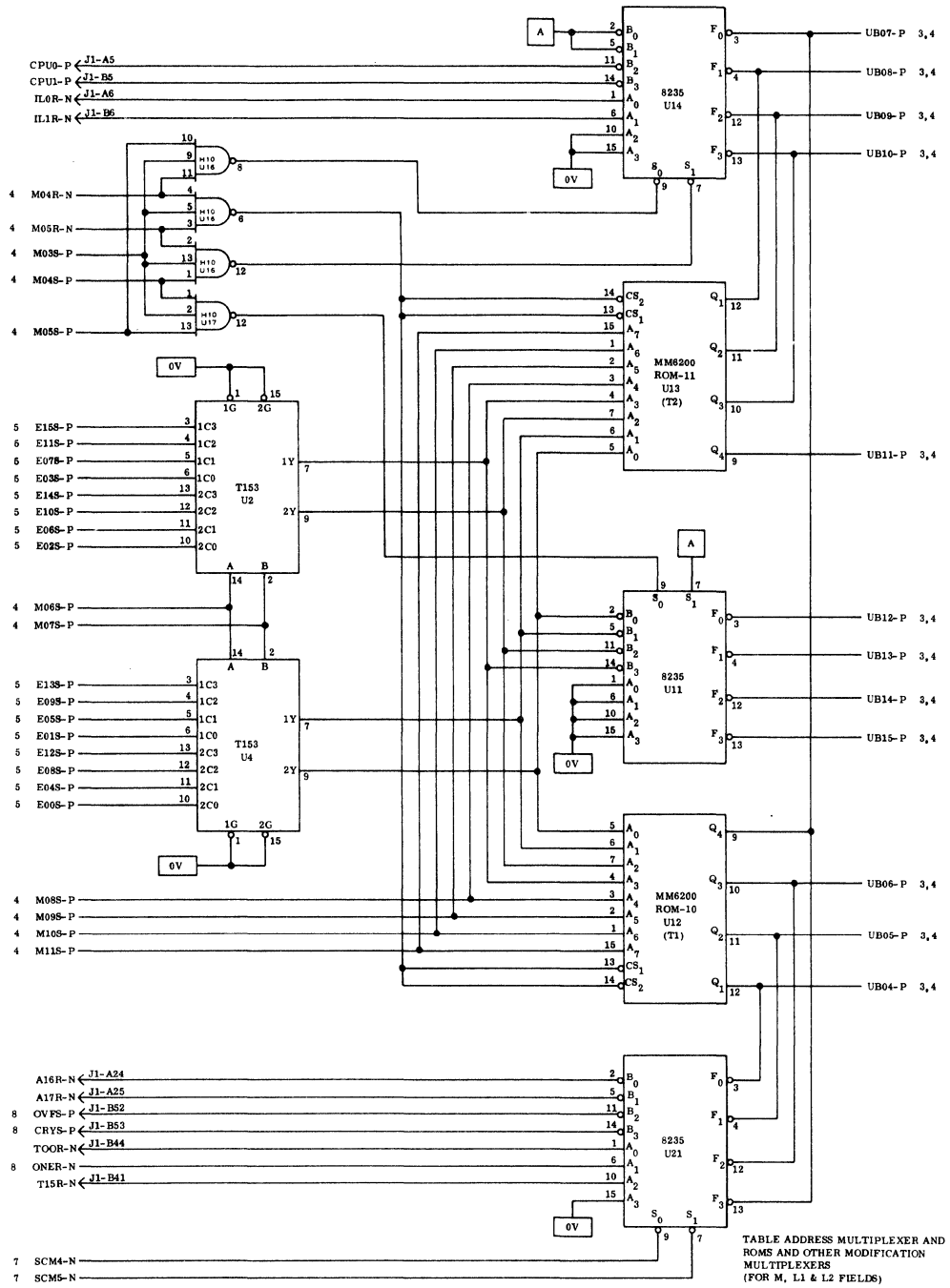
Function 2 modifies M09 and M10 of the next micro-instruction with the processor number.

Special Command 4 modifies M04 thru M07 (L1) of the next micro-instruction with the inverted Key bits (A16R and A17R) and with the Overflow and Carry flip-flops (each in respective order).

Special Command 5 modifies M04 thru M06 of the next micro-instruction with the least significant bit from the register, the output of the All Ones flip-flop, and the most significant bit of the T register (each in respective order).

KEY SOURCE LOGIC DEFINITIONS

UB04-P thru UB15-P	The open collector inputs to the M, L2, and L1 fields of the M register. The ROMs (U12 and U13) and the multiplexers (U11, U14, and U21) may modify these signals as they come into the M register thus giving the modification of the next micro-instruction.



CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 6 of 11

FILE ENABLE TERMS, TEST MULTIPLEXER,... CPB (LD2001002169-1, Sheet 7)

The logic shown on LD sheet 7 performs a variety of functions:

The read and write enable signals (RExx-N and WExx-N) are generated to allow reading from the register files and writing into the files.

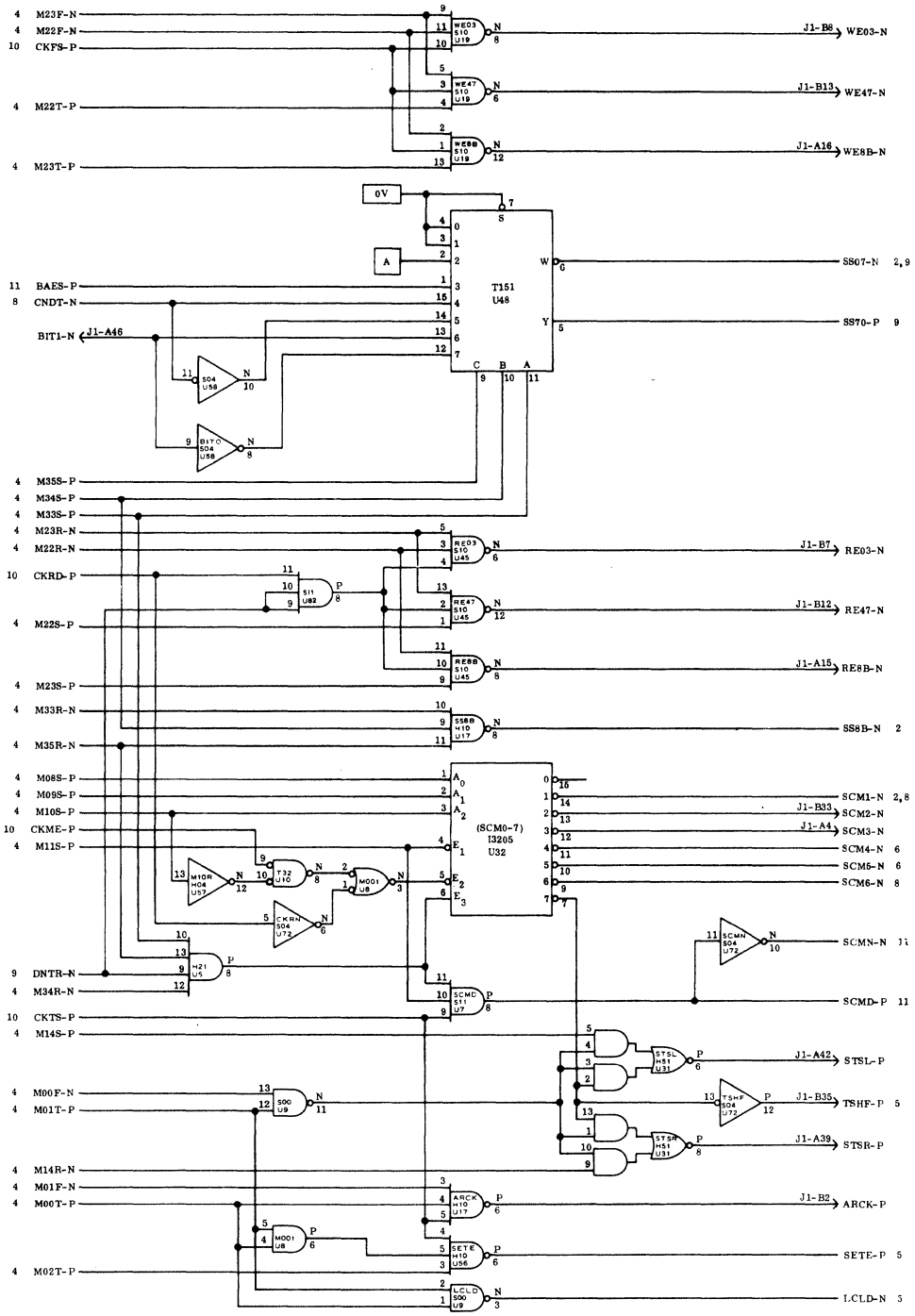
The multiplexer (U48) and gate addressed by the S field code (M33 thru M35) provide the micro-sequence load enable (i.e. branch) controls used to load the sequence counter and Dont flip-flop.

Special Commands (SCMx-N) including shifts and memory accesses, are activated when the S field code equals ONE

The clock enable terms shown in the lower part of the drawing are generated to load the A and E registers.

KEY SOURCE LOGIC DEFINITIONS

ARCK-P	Enabled clock to load the A register from the ALU outputs.
LCLD-N	Loads enable for the four least significant bits of the E Register.
SETE-P	Enabled clock to load the 12 most significant bits of the E Register.
RE03-N, RE47-N, RE8B-N, WE03-N, WE47-N, WE8B-N	Read Enable, Write Enable for the register file.
SCMD-P	Special command to initiate memory access with CKTS-P as clocking term.
SCMN-N	Negation of SCMD-P used to reset the Abort flip-flop on any memory access including no-cycle request.
SCM1-N thru SCM6-N	Specific decodes for special commands 1 thru 6 (active low). Timing for commands 1 thru 3 are different than timing for commands 4 thru 6.
SS8B-N	Decode of Jump Class to enable load of most significant bits of the micro-sequence (S) counter.
STSL-P, STSR-P	Active low T register mode control lines. If both are low the T register loads; if one only is low the T register shifts (left on STSL, right on STSR) and if both are high the T register is stable.
SS07-N, SS70-N	Positive and negative outputs of the micro-sequence control to enable load of eight low order bits of the micro-sequence counter (SS07-N) and to input the Dont flip-flop multiplexer for skip control.
TSHF-P	Special Command 7 (active high) for general shift control.



FILE ENABLE TERMS, TEST MULTIPLEXER, SPECIAL COMMAND DECODE, REG E AND A CLOCKS AND ENABLE TERMS

CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 7 of 11

JUMP MULTIPLEXER, NEXT FLIP-FLOP, ALL-ONES FLIP-FLOP, ... CPB (LD2001002169-1, Sheet 8)

E register bits and other status are addressed by the M field via the jump multiplexer to determine conditional jumps in the microcode.

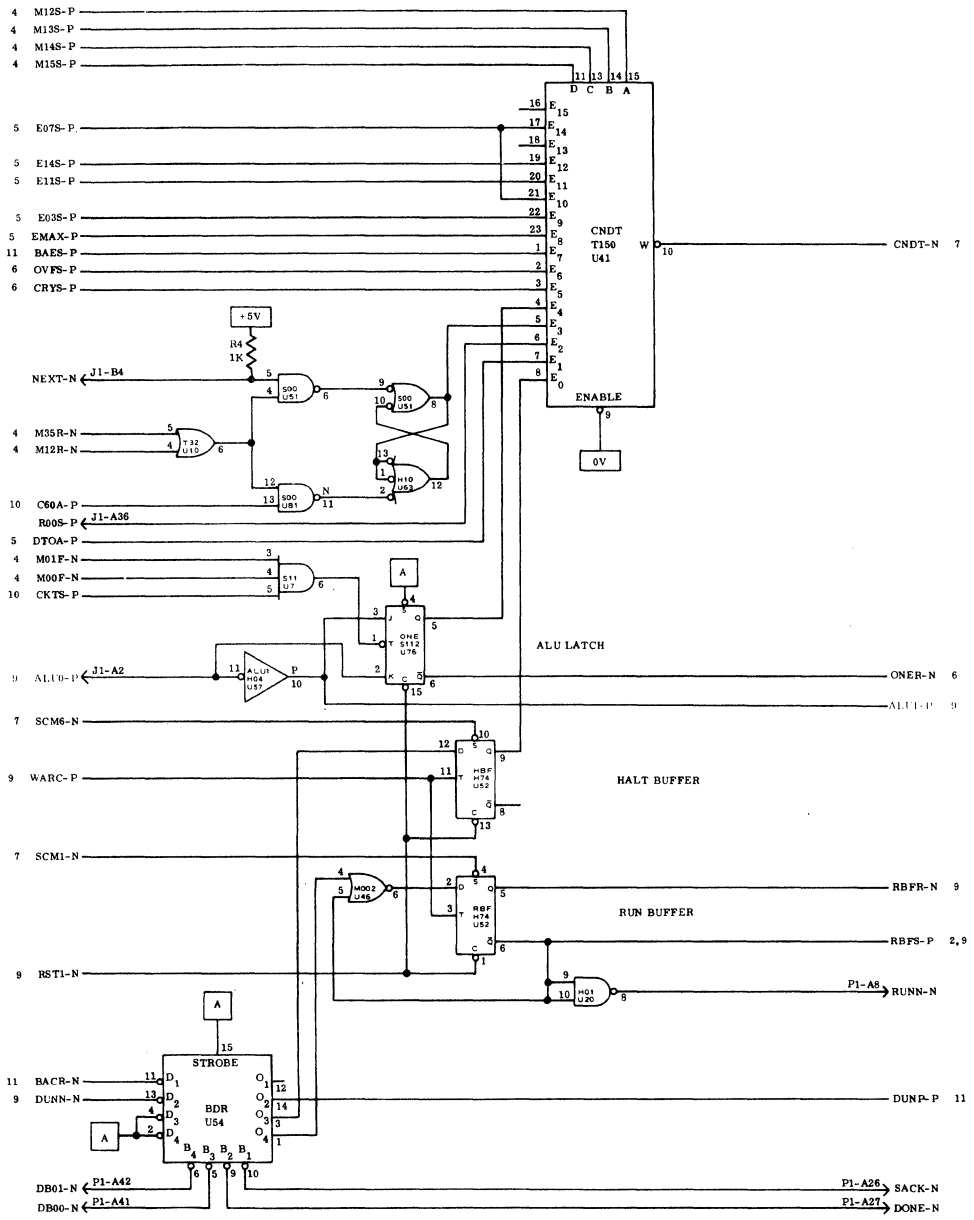
A pending interrupt is buffered in the NEXT flip-flop.

The Halt and Run flip-flops may be loaded from the INFIBUS (however, the Run may be set only from the INFIBUS)

The Ones flip-flop is loaded from the ALU result if none of registers A, T, or R is loaded.

KEY SOURCE LOGIC DEFINITIONS

ALU0-P	The negation of ALU1-P used for the inverse input to the K terminal and to the Dont flip-flop multiplexer U47 (sheet 9).
NEXT-N	The asynchronous signal from the BCU indicating an interrupt is pending. It must be buffered to prevent a race condition in the CNDT-N output.
CNDT-N	The output sampled from various status conditions in the system and used to control conditional branching in the microcode.
DB00-N, DB01-N	The two low order data inputs from the INFIBUS which may be clocked into the control register (Halt and Run flip-flops) to start and stop the operation.
DONE-N	The INFIBUS signal sent when responding as a slave device and received when acting as a master device.
DUNP-P	The received DONE-N signal used to complete a memory cycle and strobe the read data from the INFIBUS.
HALT Buffer	A flip-flop set either externally via the INFIBUS or by the microcode Special Command 6 and that may be interrogated by the microcode to check for a Halt request.
ONER-N	The negative side of the All-Ones flip-flop used to help provide the status to load into the status register via the multiplexer U21 (sheet 9).
RBFR-N, RBFS-P	The outputs of the Run flip-flop used to increment the sequence (S) counter and generate system clocks while running or when halted.
R00S-P	The least significant bit of the R register used as a test input for detecting multi-level indirect addressing.
RUNN-N	Drives the INFIBUS line to light the Run indicator on the control panel.
SACK-N	The INFIBUS signal sent to acknowledge selection of the CPU for the next INFIBUS (memory) cycle.



JUMP TEST MULTIPLEXER, NEXT BUFFER, PART OF INFIBUS INTERFACE, CONTROL AND ALL ONES FLIP FLOPS

CPB

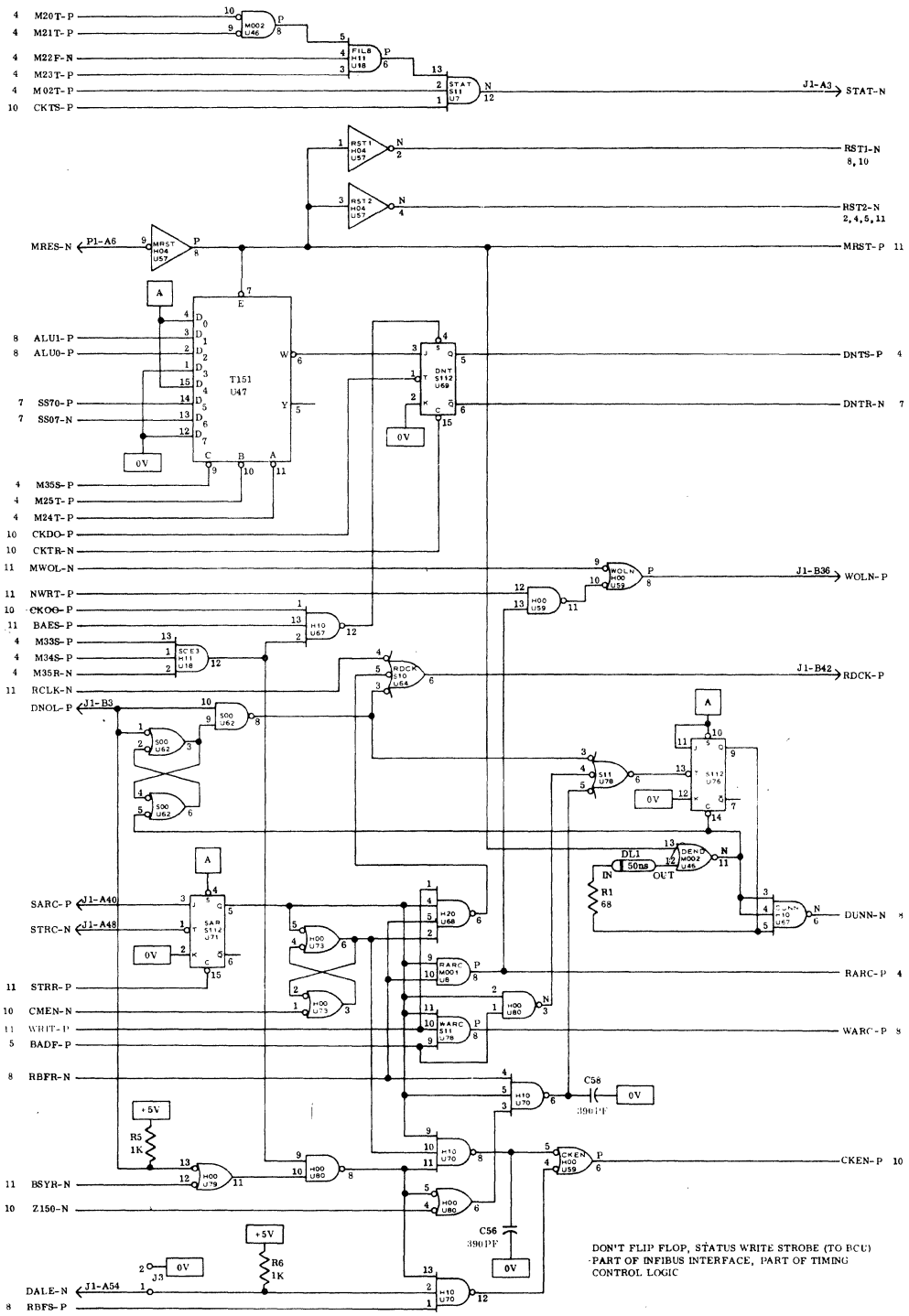
Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 8 of 11

DONT FLIP-FLOP, STATUS WRITE STROBE, ... CPB (LD2001002169-1, Sheet 9)

The logic on LD sheet 9 controls: access to the INFIBUS data lines (WOLN-P, RDCK-P); slave cycles (RARC-P, WARC-P, DUNN-N); clock sequence initiation after a WAIT micro-step (CKEN-P); clearing of M register for NO-OP micro-steps (DNTS-P, DNTR-N); general processor hardware reset (MRST-P, RST1-N, RST2-N); and writing to the interrupt mask flip-flops in the BCU (STAT-N).

KEY SOURCE LOGIC DEFINITIONS

CKEN-P	Interrupts the clock sequence when low. One input (pin 4) allows normal running unless the RUN flip-flop is reset, a Wait micro-step is encountered, or DALE is grounded. The other input allows a single clock sequence to be generated from the INFIBUS interface logic.
DALE-N	Single micro-step control input, when grounded, CKEN must be activated by the control panel Run button (via the INFIBUS and through gate U70, pin 8) to generate individual clock sequences.
DNTS-P, DNTR-N	Outputs of the Dont flip-flop that cause the micro-instruction currently being fetched to be reset as it is buffered in the M register, thus, giving a no-operation.
DNOL-P	The Device Number On Line signal coming from the BCU to indicate that a controller has placed its device number on the INFIBUS data lines for pick up by the CPU.
DUNN-N	A pulse (greater than 50 nanoseconds) generated by reset, or at the end of a processor slave cycle, to signal the completion of the INFIBUS data cycle and strobe the output data in read.
MRST-P	The positive master reset pulse originated by the control panel reset function.
RARC-P	Enables the logic to modify the ALU code and write file bit in the M register during the micro-steps executed with the run flip-flop off (i.e. halted) while acting as a slave device.
RDCK-P	The clock for the R register (in the CPA) to enable data from the INFIBUS to be loaded into the R register.
RST1-N, RST2-N	The negative master reset pulse originated by the control panel reset function.
STAT-N	The signal to the BCU indicating that the status register is being written into. It is used to clock the four most significant bits from the ALU bus into the BCU interrupt mask flip-flops.
WARC-P	Clocks the control flip-flops (Run and Halt) to receive data from the INFIBUS when the control register is written into.
WOLN-P	The write enable to send data from the T register through inverters and bus drivers out onto the INFIBUS data lines.



CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 9 of 11

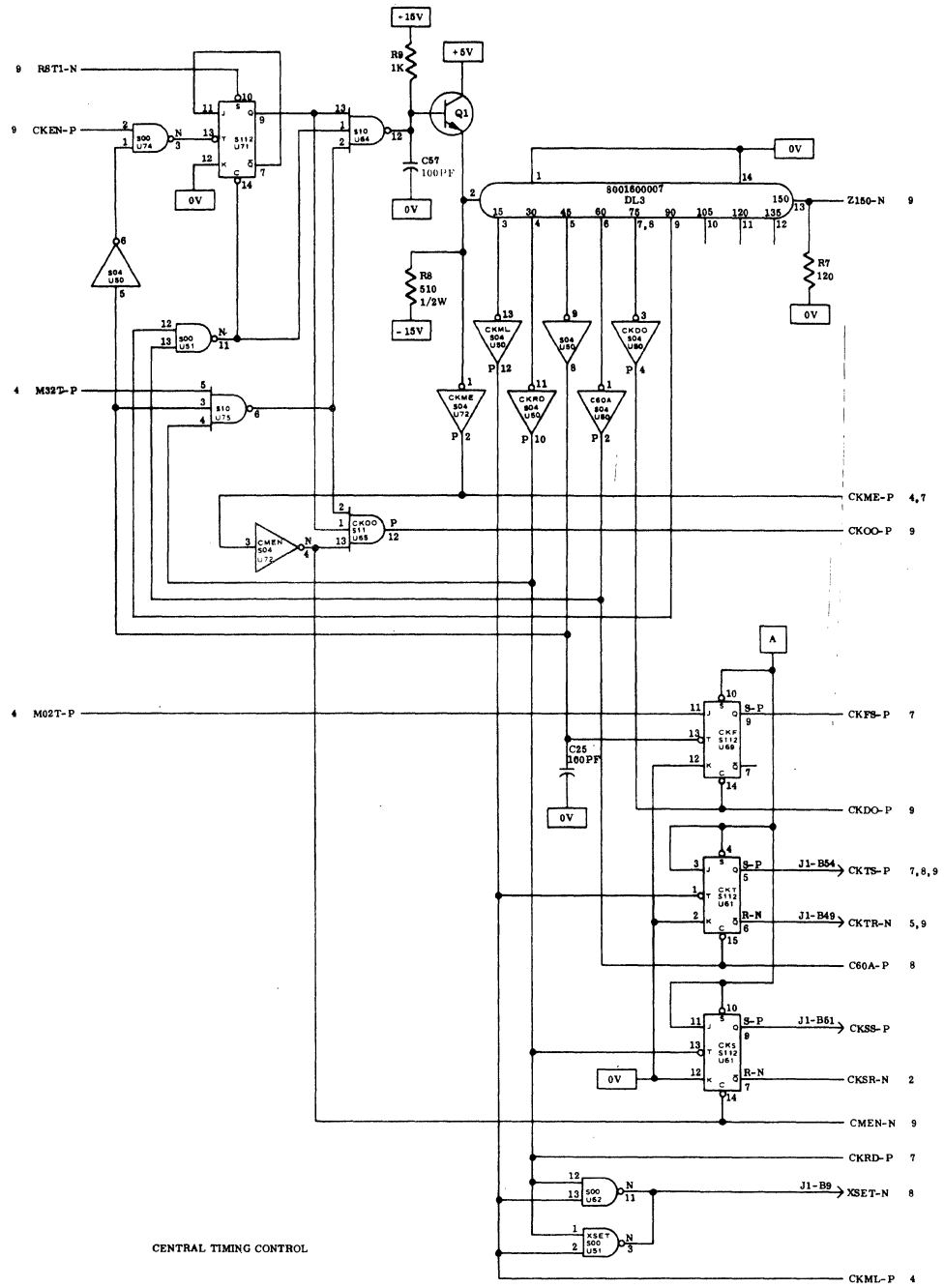
CENTRAL TIMING CONTROL, CPB (LD2001002169-1, Sheet 10)

The various clocking terms are generated from a 150-nanosecond tapped delay line. The delay line is driven by an emitter follower, its outputs are buffered by inverters, and it is terminated with a 120-ohm resistor. The taps are at 15-nanosecond intervals and the various timing relationships needed are derived by combining them with gates and flip-flops and tuning where necessary with capacitors. The basic signal traverses the delay line and recirculates with the opposite polarity to give a length effectively greater than 150 nanoseconds. The recirculation path is controlled by M32T-P to give two basic cycle times for logical ALU operations (shorter) and for arithmetic ALU operations (longer). Circulation is stopped while CKEN-P is low during a Wait micro-step. Short (logic) cycles are forced during the reset pulse (RST1-N). Signal M02T-P is an enabling term for the CKFS-P clock used to write to the file registers.

See figures 3 and 4 at the beginning of the drawing section for clock timing. Figure 3 shows how signals are re-initiated after a wait micro-instruction. The first cycle is arithmetic (155 nanoseconds) and the second cycle is logical (145 nanoseconds). Figure 4 shows the relative timing for a halt, file access, or start sequence.

KEY SOURCE LOGIC DEFINITIONS

C60[illegible]1	Resets the interrupt buffer (CPB sheet 8) when the NEXT pulse is not present.
CKDO-P	Clocks the Dont flip-flop by its trailing edge late in the cycle. It also clears the CKFS-P flip-flop at the same time.
CKFS-P	Clocks the file write enable (select) terms to generate a short write pulse to the enabled file register components late in the cycle.
CKME-P	Clocks the ROM outputs into the early portion of the M register at the beginning of the cycle. It also extends timing on special commands 4, 5, 6 and 7 (shifts).
CKML-P	Clocks the ROM outputs into the late portion of the M register early in the cycle and clears the entire M register if the Dont flip-flop is set.
CKRD-P	Enables the file read-select gates and controls the timing for special commands 1 through 7.
CKSR-N, (CKSS-P)	Clocks the S counter for incrementing or loading a new ROM address.
CKTR-N,CKTS-P	Used widely to clock the T, E, and A registers, the Dont, Carry, Overflow, Ones, and Memory Control flip-flops and the interrupt MASKS in the Bus Control Unit (BCU).
CK00-P	Sets the Dont flip-flop when a memory abort takes place during a wait condition.
CMEN-N	Resets the NAND latch shown on sheet 9 that is used to interlock controls during slave memory operations.
XSET-N	Controls the file latches between reading the file registers.
Z150-N	Drives a gate to trigger the DUNN-N signal at the end of a slave memory cycle when the processor is halted.



CPB

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 10 of 11

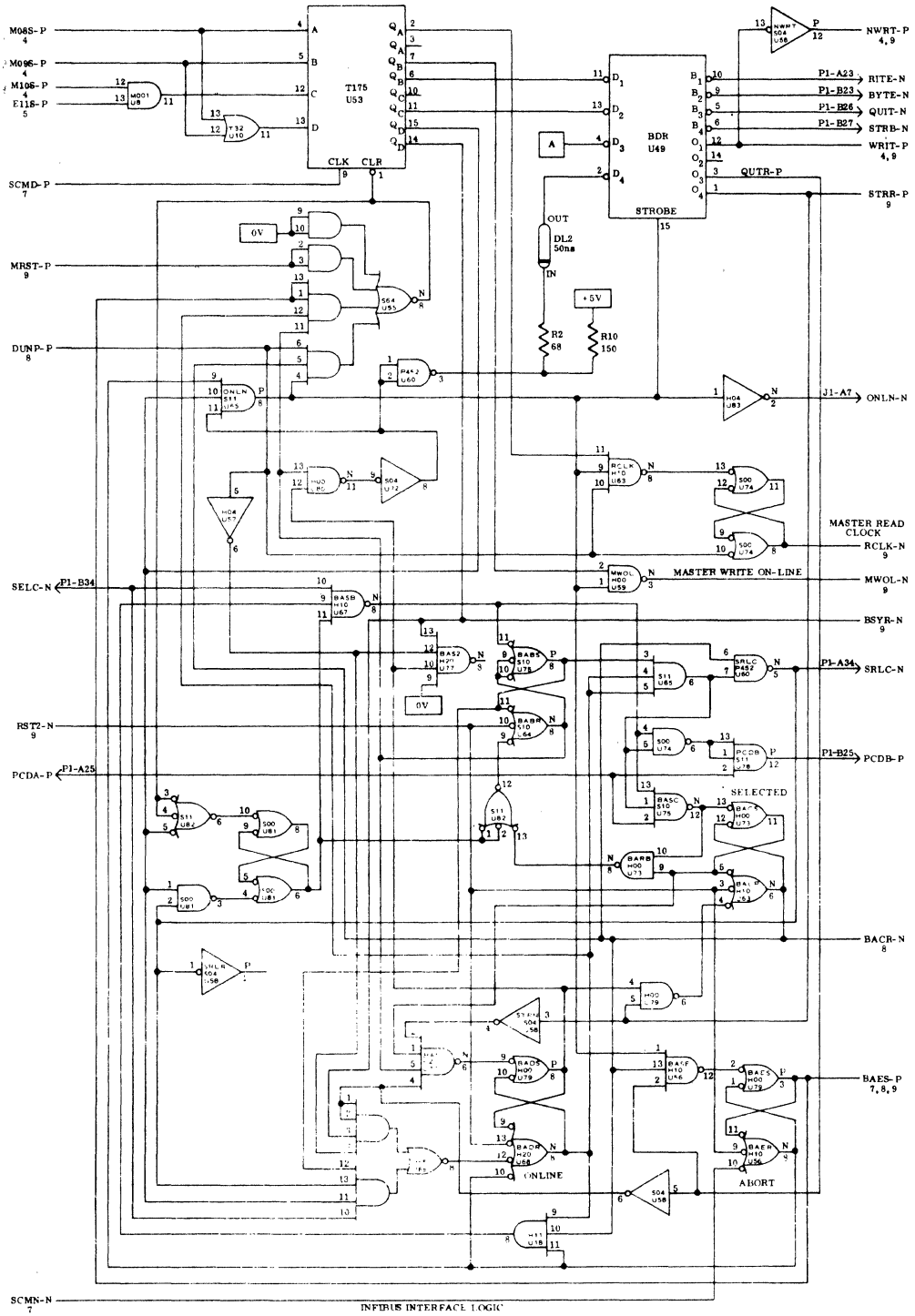
INFIBUS INTERFACE LOGIC, CPB (LD2001002169-1, Sheet 11)

The logic shown on sheet 11 controls the interface between the processor and the INFIBUS during a master memory access cycle. The logic provides the asynchronous interlocks required to maintain the bus dicipline during a read or a write cycle.

The capability to properly control a read-modify-write (RMW) cycle is not included, but when a RMW cycle is attempted, a write cycle is performed with the T register also writing into the R register via the data bus. Then the write portion of the RMW sequence performs a normal write cycle.

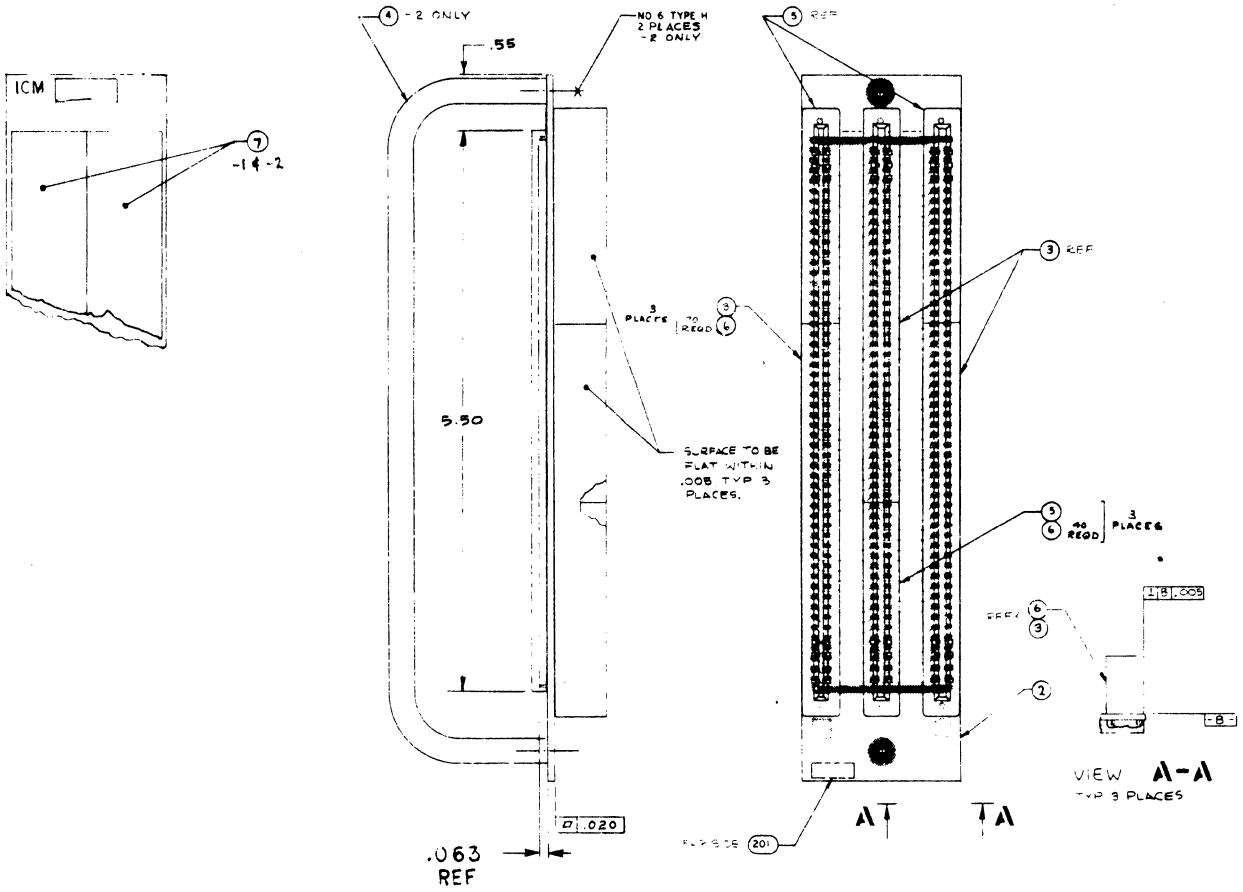
KEY SOURCE LOGIC DEFINITIONS

BACR-N	Not selected — used to: enable the INFIBUS request signal (SRLC-N), enable and acknowledge bus selection, and enable either the cycle completion or the abort condition.
BAES-P	The buffered memory abort condition used to cause a jump and skip on a Wait micro-instruction.
BSYR-N	No memory cycle is in progress, allowing normal clock generation to proceed on a Wait micro-instruction.
BYTE-N	The INFIBUS control signal requesting half word memory operation.
MWOL-N	The enabling term generated by the master memory write cycle logic to place data from the T register onto the INFIBUS. MWOL-N is combined with the enabling term for the slave memory read cycle.
NWRT-P, WRIT-P	Write control signals received from the INFIBUS and used during a slave memory cycle to select the ALU operation and to control writing to the control register, the file register, and placing data out on the INFIBUS.
ONLN-N	A general enabling signal for control outputs to the INFIBUS and read, write and abort controls. ONLN-P is true when the processor goes on-line and stays true until the cycle completes or is aborted.
PCDB-P	The outgoing precedence pulse generated by the incoming precedence pulse and disabled by having the proper select conditions and a request waiting.
QUIT-N	The INFIBUS signal that causes the present memory cycle to abort. Generated by the bus controller, it sets the abort flip-flops if the processor is selected and on line.
RCLK-N	The pulse generated by the master memory read cycle logic to clock data from the INFIBUS to the register. It is combined with the clocking term for the slave memory write cycle.
RITE-N	The INFIBUS control signal requesting a write operation to memory.
SRLC-N	Service Request level C on the INFIBUS used to request the next available data cycle from the BCU.
STRB-N	The INFIBUS control signal used to strobe the address, write data and cycle controls sent out from the processor during a master memory cycle.
STRR-P	The strobe received from the INFIBUS and used by the slave cycle to remove the reset from the self address recognition flip-flop (SAR) and used by the master cycle to enable the reset of the selected flip-flop and disable the set of the On-Line flip-flop.

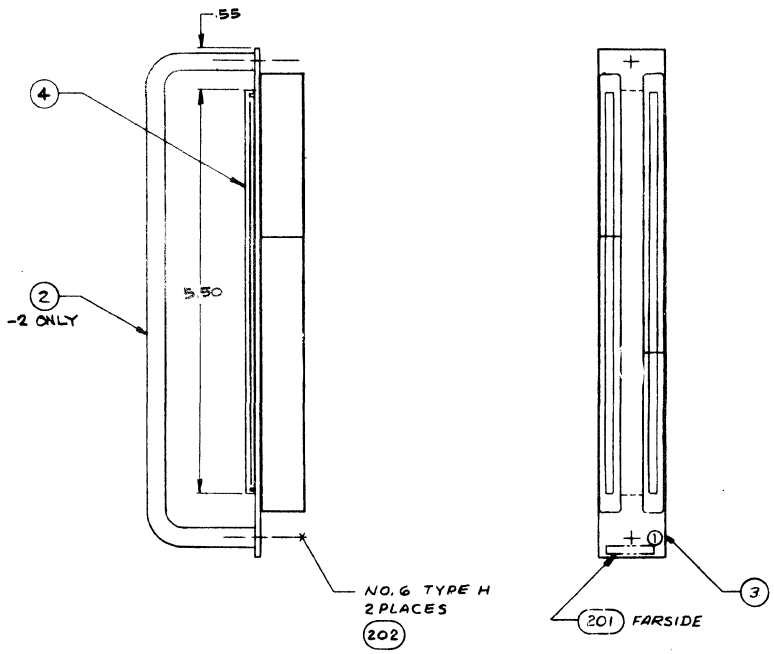


Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 11 of 11

CPB



Interconnect Module ICM, Circuit Card Assembly
2001002166, Rev. C, Sheet 1



CPB

Interconnect Dual Module IDM, Circuit Card Assembly
2001002232, Rev. B, Sheet 1

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002161-1		CPA-CKT CARD ASSY		USED ON SUE 1110A-1/1110A-2	1
002		001	0001		1001004810-5		PRINTED WRG BD, CPA		NOTE 213	2
003		003	0001		8001800047-1		ICP		U47,48,57 (74H11)	3
004		002	0001		8001800042-1		ICP		U49,75 (74H00)	4
005		004	0001		8001800043-1		ICP		U2,12,22,32 (74H01)	5
006		006	0001		8001800044-1		ICP		U42,43,44,58,68, 78 (74H04)	6
007		001	0001		8001800046-1		ICP		U73 (74H10)	7
008		001	0001		8001800048-1		ICP		U74 (74H20)	8
009		001	0001		8001800054-1		ICP		U66 (74H51)	9
010		001	0001		8001803200-1		ICP		U67 (74S04)	10
011		001	0001		8001800117-1		ICP		U62 (74150)	11
012		009	0001		8001803165-1		ICP		U7,8,17,18,27, 28,37,38,52 (74153)	12
013		012	0001		8001803178-1		ICP		U3,4,5,13,14,15, 23,24,25,33,34, 35 (74170)	13
014		005	0001		8001803181-1		ICP		U6,16,26,36,69 (74175)	14
		002	0001		8001803195-1		ICP		U51,61 (74198)	15
016		001	0001		8001803121-1		ICP		U46 (74H74)	16
017		001	0001		8001803204-1		ICP		U19 (74S15)	17
018		001	0001		8001803208-1		ICP		U65 (74S64)	18
019		001	0001		8001803212-1		ICP		U71 (74S112)	19
020		002	0001		N74H08N	18324	ICP	SIGNETICS	U55,77	20
021		000	0001		MC3001P	04713	ICP	MOTOROLA	U55,77	20A
021		001	0001		8001803211-1		ICP		U76 (74S86)	21
022		004	0001		8001803183-1		ICP		U1,11,21,31 (74181)	22
023		001	0001		8001803184-1		ICP		U41 (74182)	23
024		001	0001		N8242A	18324	ICP	SIGNETICS	U9	24
025		009	0001		8001800120-1		ICP		U10,20,29,30,40, 50,60,70,80 (BDR)	25
026		002	0001		8001803180-1		ICP		U59,79 (74174)	26
027		018	0001		RL07S471G		RESISTOR	MIL-R-22684/1	R3,4,5,6,R8 THRU R20,R22 .5 IS	27
028		003	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R1,7,23 .5 IS	28
029		002	0001		RL07S361G		RESISTOR	MIL-R-22684/1	R21,2 .5 IS	29
030		000								30
031		003	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C26,27,29 .25 IS	31

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MAT NOTE(S) REF DESIGNATION(S)	FIN NO.
032	002	0001		8001300311-2		CAPACITOR		C23,24 .8 IS	32
033	022	0001		8001300101-1		CAPACITOR		C1 THRU C22 .25 IS	33
034	001	0001		1001005395-1		SHIELD		NOTE 213	34
035	REF	0001		LD2001002161-1		LOGIC DIAGRAM			35
036	A/R	0001		SN60/SN63		SOLDER	QQ-S-571		36
037	022	0001		1005000764-1		PIN, TERMINAL		NOTE 210	37
038	003	0001		22AWG WHT		TUBING (TEFLON)	MIL-I-22129	APPROX INCH REQD	38
039	001	0001		CM05FD151J03		CAPACITOR	MIL-C-5/18	C28 .25 IS	39
040	A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 211	40
041	048	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX INCH REQD	41
042	000								42
043	000								43
				SPEC/DWG/STD		NOTES:			200
				LECP1049-1		MARKING (IDENTIFY).			201
						AREA TO BE FREE OF SOLDER			202
						TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
						COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REFERENCE DESIGNATIONS.			204
						MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
						PROTRUSION (SIDE 2) .075 MAXIMUM.			206
									207
						MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
						SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			209
						TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			210
						SPOT BOND JUMPER WIRES FIND NUMBER 41 USING FIND NUMBER 40.			211
						INTERCONNECT WIRING			212
						FROM TO REMARKS			
						E1 E8 FIND NO. 41			
						E3 E5 FIND NO. 41			
						E6 E2 FIND NO. 41			
						E7 E4 FIND NO. 41			
						E9 E10 FIND NO. 41			
						E11 E12 FIND NO. 41			
						E13 E14 FIND NO. 41			
						E15 E16 FIND NO. 41			
						E17 E18 FIND NO. 41			
						INSTALL SHIELD (FIND NUMBER 34) AFTER FLOW SOLDER OPERATION.			213

CPB

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002169-5		CPB-CKT CARD ASSY		USED ON SUE 1110A-1, 1110A-2	1
002		001	0001		1001004809-5		PRINTED WRG BD, CPB		NOTE 211	2
003		004	0001		80018000042-1		ICP		U59, 73, 79, 80 (74H00)	3
004		001	0001		80018000043-1		ICP		U20 (74H01)	4
005		002	0001		80018000044-1		ICP		U57, 83 (74H04)	5
006		006	0001		80018000046-1		ICP		U16, 17, 56, 63, 67, 70 (74H10)	6
007		001	0001		80018000047-1		ICP		U18 (74H11)	7
008		002	0001		80018000048-1		ICP		U68, 77 (74H20)	8
009		001	0001		80018000049-1		ICP		U6 (74H21)	9
010		001	0001		80018000054-1		ICP		U31 (74H51)	10
011		001	0001		80018000058-1		ICP		U66 (74H55)	11
012		000								12
013		001	0001		80018000117-1		ICP		U41 (74150)	13
014		002	0001		80018000118-1		ICP		U47, 48 (74151)	14
015		002	0001		80018003165-1		ICP		U2, 4 (74153)	15
016		000								16
017		003	0001		80018003173-1		ICP		U3, 43, 44 (74163)	17
018		005	0001		80018003180-1		ICP		U1, 5, 34, 37, 40 (74174)	18
019		005	0001		80018003181-1		ICP		U33, 35, 38, 39, 53 (74175)	19
020		001	0001		80018003121-1		ICP		U52 (74H74)	20
021		004	0001		80018003198-1		ICP		U51, 62, 74, 81 (74S00)	21
022		003	0001		80018003200-1		ICP		U50, 58, 72 (74S04)	22
023		004	0001		80018003202-1		ICP		U19, 45, 64, 75 (74S10)	23
024		004	0001		80018003203-1		ICP		U7, 65, 78, 82 (74S11)	24
025		001	0001		80018003208-1		ICP		U55 (74S64)	25
026		004	0001		80018003212-1		ICP		U61, 69, 71, 76 (74S112)	26
027		001	0001		74R00MP	07933	ICP	RAYTHEON	U9 (74R00)	27
028		000	0001		80018003198-1		ICP		U9 (74S00)	27a
029		001	0001		MC3001P	04713	ICP	MOTOROLA	U8	28
030		001	0001		MC3002P	04713	ICP	MOTOROLA	U46	29
031		001	0001		80018003137-1		ICP		U10 (7432)	30
032		001	0001		80018003218-1		ICP		U32 (74S138)	31
033		001	0001		N8264N	18324	ICP	SIGNETICS	U15	32
034		003	0001		N8235B	18324	ICP	SIGNETICS	U11, 14, 21	33

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U60	34
036		002	0001		AS-143-U-3	06776	SOCKET	ROBINSON NUGENT	NOTE 213	35
037		002	0001		8001800120-1		ICP		U49,54 (BDR)	36
038		001	0001		74R174MP	07933	ICP	RAYTHEON	U36 (174MP)	37
039		000	0001		8001803180-1		ICP		U36 (74174)	37a
040		002	0001		NO.4416X3/4	26066	TAPE	3M CO	.75 X .70 LONG APPROX INCH REQD NOTE 213	38
041		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R9 .5 IS	39
042		001	0001		RL20S511G		RESISTOR	MIL-R-22684/2	R8 .6 IS	40
043		001	0001		RL07S121G		RESISTOR	MIL-R-22684/1	R7 .5 IS	41
044		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	42
045		004	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R3,4,5,6 .5 IS	43
046		002	0001		CM04FD101J03		CAPACITOR	MIL-C-5/18	C25,57 .25 IS	44
047		001	0001		8001200001-1		TRANSISTOR		Q1	45
048		002	0001		8001600008-1		DELAY LINE, FIXED		DL1,DL2	46
049		001	0001		8001600007-1		DELAY LINE, TAPPED		DL3	47
050		047	0001		8001300101-1		CAPACITOR		C1 THRU C13, C15 THRU C24, C26,27,29,30,31, C33 THRU C36, C38 THRU C52 .25 IS	48
051		003	0001		8001300311-2		CAPACITOR		C28,32,37 .8 IS	49
052		002	0001		8001300333-2		CAPACITOR		C14,53 .8 IS	50
053		021	0001		1005000764-1		PIN, TERMINAL		NOTE 210	51
054		000								52
055		001	0001		1005000796-41		READ ONLY MEMORY		U28	53
056		001	0001		1005000796-42		READ ONLY MEMORY		U23	54
057		001	0001		1005000796-43		READ ONLY MEMORY		U24	55
058		001	0001		1005000796-44		READ ONLY MEMORY		U22	56
059		001	0001		1005000796-45		READ ONLY MEMORY		U26	57
060		001	0001		1005000796-46		READ ONLY MEMORY		U25	58
061		001	0001		1005000796-47		READ ONLY MEMORY		U27	59
062		001	0001		1005000796-48		READ ONLY MEMORY		U30	60
063		001	0001		1005000796-49		READ ONLY MEMORY		U29	61
064		001	0001		1005000796-26		READ ONLY MEMORY		U12	62
065		001	0001		1005000796-27		READ ONLY MEMORY		U13	63
066		009	0001		1001004974-1		RESISTOR CLUSTER		A1 THRU A9	64
067		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65
068		REF	0001		LD2001002169-1		LOGIC DIAGRAM			66
069		000								67
070		004	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX FT REQD	68
071		002	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C54,55 .25 IS	69
072		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 215	70
073		002	0001		CM05FD391J03-		CAPACITOR	MIL-C-5/18	C56,58 .25 IS	71
074		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R10	72

CPB

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002169-6		CPB-CKT CARD ASSY		USED ON SUE 1111A-1,1111A-2	1
002		001	0001		1001004809-5		PRINTED WRG BD, CPB		NOTE 211	2
003		004	0001		8001800042-1		ICP		U59,73,79,80 (74H00)	3
004		001	0001		8001800043-1		ICP		U20 (74H01)	4
005		002	0001		8001800044-1		ICP		U57,83 (74H04)	5
006		006	0001		8001800046-1		ICP		U16,17,56,63,67, 70 (74H10)	6
007		001	0001		8001800047-1		ICP		U18 (74H11)	7
008		002	0001		8001800048-1		ICP		U68,77 (74H20)	8
009		001	0001		8001800049-1		ICP		U6 (74H21)	9
010		001	0001		8001800054-1		ICP		U31 (74H51)	10
011		001	0001		8001800058-1		ICP		U66 (74H55)	11
012		000								12
013		001	0001		8001800117-1		ICP		U41 (74150)	13
014		002	0001		8001800118-1		ICP		U47,48 (74151)	14
015		002	0001		8001803165-1		ICP		U2,4 (74153)	15
016		000								16
017		004	0001		8001803173-1		ICP		U3,42,43,44 (74163)	17
018		005	0001		8001803180-1		ICP		U1,5,34,37,40 (74174)	18
019		005	0001		8001803181-1		ICP		U33,35,38,39,53 (74175)	19
020		001	0001		8001803121-1		ICP		U52 (74H74)	20
021		004	0001		8001803198-1		ICP		U51,62,74,81 (74S00)	21
022		003	0001		8001803200-1		ICP		U50,58,72(74S04)	22
023		004	0001		8001803202-1		ICP		U19,45,64,75 (74S10)	23
024		004	0001		8001803203-1		ICP		U7,65,78,82 (74S11)	24
025		001	0001		8001803208-1		ICP		U55 (74S64)	25
026		004	0001		8001803212-1		ICP		U61,69,71,76 (74S112)	26
027		001	0001		74R00MP	07933	ICP	RAYTHEON	U9 (74R00)	27
028		000	0001		8001803198-1		ICP		U9 (74S00)	27A
029		001	0001		MC3001P	04713	ICP	MOTOROLA	U8	28
030		001	0001		MC3002P	04713	ICP	MOTOROLA	U46	29
031		001	0001		8001803137-1		ICP		U10 (7432)	30
032		001	0001		8001803218-1		ICP		U32 (74S138)	31
033		001	0001		N8264N	18324	ICP	SIGNETICS	U15	32
034		003	0001		N8235B	18324	ICP	SIGNETICS	U11,14,21	33

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U60	34
036		003	0001		AS-143-U-3	06776	SOCKET	ROBINSON NUGENT	NOTE 213	35
037		002	0001		8001800120-1		ICP		U49,54 (BDR)	36
038		001	0001		74R174MP	07933	ICP	RAYTHEON	U36 (174MP)	37
039		000	0001		8001803180-1		ICP		U36 (74174)	37a
040		003	0001		NO.4416X3/4	26066	TAPE	3M CO	.75 X .70 LONG APPROX INCH REQD NOTE 213	38
041		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R9 .5 IS	39
042		001	0001		RL20S511G		RESISTOR	MIL-R-22684/2	R8 .6 IS	40
043		001	0001		RL07S121G		RESISTOR	MIL-R-22684/1	R7 .5 IS	41
044		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	42
045		004	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R3,4,5,6 .5 IS	43
046		002	0001		CM04FD101J03		CAPACITOR	MIL-C-5/18	C25,57 .25 IS	44
047		001	0001		8001200001-1		TRANSISTOR		Q1	45
048		002	0001		8001600008-1		DELAY LINE, FIXED		DL1,DL2	46
049		001	0001		8001600007-1		DELAY LINE, TAPPED		DL3	47
050		047	0001		8001300101-1		CAPACITOR		C1 THRU C13, C15 THRU C24, C26,27,29,30,31, C33 THRU C36, C38 THRU C52 .25 IS	48
051		003	0001		8001300311-2		CAPACITOR		C28,32,37 .8 IS	49
052		002	0001		8001300333-2		CAPACITOR		C14,53 .8 IS	50
053		021	0001		1005000764-1		PIN, TERMINAL		NOTE 210	51
054		000								52
055		001	0001		1005000856-31		READ ONLY MEMORY		U28	53
056		001	0001		1005000856-32		READ ONLY MEMORY		U23	54
057		001	0001		1005000856-33		READ ONLY MEMORY		U24	55
058		001	0001		1005000856-34		READ ONLY MEMORY		U22	56
059		001	0001		1005000856-35		READ ONLY MEMORY		U26	57
060		001	0001		1005000856-36		READ ONLY MEMORY		U25	58
061		001	0001		1005000856-37		READ ONLY MEMORY		U27	59
062		001	0001		1005000856-38		READ ONLY MEMORY		U30	60
063		001	0001		1005000856-39		READ ONLY MEMORY		U29	61
064		001	0001		1005000796-26		READ ONLY MEMORY		U12	62
065		001	0001		1005000796-27		READ ONLY MEMORY		U13	63
066		009	0001		1001004974-1		RESISTOR CLUSTER		A1 THRU A9	64
067		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65
068		REF	0001		LD2001002169-1		LOGIC DIAGRAM			66
069		000								67
070		004	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX FT REQD	68
071		002	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C54,55 .25 IS	69
072		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 215	70
073		002	0001		CM05FD391J03		CAPACITOR	MIL-C-5/18	C56,58 .25 IS	71
074		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R10	72

CPB

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002169-8		CPB-CKT CARD ASSY		USED ON SUE 1112A-1, 1112A-2	1
002		001	0001		1001004809-5		PRINTED WRG BD, CPB		NOTE 211	2
003		004	0001		8001800042-1		ICP		U59, 73, 79, 80 (74H00)	3
004		001	0001		8001800043-1		ICP		U20 (74H01)	4
005		002	0001		8001800044-1		ICP		U57, 83 (74H04)	5
006		006	0001		8001800046-1		ICP		U16, 17, 56, 63, 67, 70 (74H10)	6
007		001	0001		8001800047-1		ICP		U18 (74H11)	7
008		002	0001		8001800048-1		ICP		U68, 77 (74H20)	8
009		001	0001		8001800049-1		ICP		U6 (74H21)	9
010		001	0001		8001800054-1		ICP		U31 (74H51)	10
011		001	0001		8001800058-1		ICP		U66 (74H55)	11
012		000								12
013		001	0001		8001800117-1		ICP		U41 (74150)	13
014		002	0001		8001800118-1		ICP		U47, 48 (74151)	14
015		002	0001		8001803165-1		ICP		U2, 4 (74153)	15
016		000								16
017		004	0001		8001803173-1		ICP		U3, 42, 43, 44 (74163)	17
018		005	0001		8001803180-1		ICP		U1, 5, 34, 37, 40 (74174)	18
019		005	0001		8001803181-1		ICP		U33, 35, 38, 39, 53 (74175)	19
020		001	0001		8001803121-1		ICP		U52 (74H74)	20
021		004	0001		8001803198-1		ICP		U51, 62, 74, 81 (74S00)	21
022		003	0001		8001803200-1		ICP		U50, 58, 72 (74S04)	22
023		004	0001		8001803202-1		ICP		U19, 45, 64, 75 (74S10)	23
024		004	0001		8001803203-1		ICP		U7, 65, 78, 82 (74S11)	24
025		001	0001		8001803208-1		ICP		U55 (74S64)	25
026		004	0001		8001803212-1		ICP		U61, 69, 71, 76 (74S112)	26
027		001	0001		74R00MP	07933	ICP	RAYTHEON	U9 (74R00)	27
028		000	0001		8001803198-1		ICP		U9 (74S00)	27*
029		001	0001		MC3001P	04713	ICP	MOTOROLA	U8	28
030		001	0001		MC3002P	04713	ICP	MOTOROLA	U46	29
031		001	0001		8001803137-1		ICP		U10 (7432)	30
032		001	0001		8001803218-1		ICP		U32 (74S138)	31
033		001	0001		N8264N	18324	ICP	SIGNETICS	U15	32
034		003	0001		N8235B	18324	ICP	SIGNETICS	U11, 14, 21	33

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U60	34
036		003	0001		AS-143-U-3	06776	SOCKET	ROBINSON NUGENT	NOTE 213	35
037		002	0001		8001800120-1		ICP		U49,54 (BDR)	36
038		001	0001		74R174MP	07933	ICP	RAYTHEON	U36 (174MP)	37
039		000	0001		8001803180-1		ICP		U36 (74174)	37a
040		003	0001		NO.4416X3/4	26066	TAPE	3M CO	.75 X .70 LONG APPROX INCH REQD NOTE 213	38
041		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R9 .5 IS	39
042		001	0001		RL20S511G		RESISTOR	MIL-R-22684/2	R8 .6 IS	40
043		001	0001		RL07S121G		RESISTOR	MIL-R-22684/1	R7 .5 IS	41
044		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	42
045		004	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R3,4,5,6 .5 IS	43
046		002	0001		CM04FD101J03		CAPACITOR	MIL-C-5/18	C25,57 .25 IS	44
047		001	0001		8001200001-1		TRANSISTOR		Q1	45
048		002	0001		8001600008-1		DELAY LINE, FIXED		DL1,DL2	46
049		001	0001		8001600007-1		DELAY LINE, TAPPED		DL3	47
050		047	0001		8001300101-1		CAPACITOR		C1 THRU C13, C15 THRU C24, C26,27,29,30,31, C33 THRU C36, C38 THRU C52 .25 IS	48
051		003	0001		8001300311-2		CAPACITOR		C28,32,37 .8 IS	49
052		002	0001		8001300333-2		CAPACITOR		C14,53 .8 IS	50
053		021	0001		1005000764-1		PIN, TERMINAL		NOTE 210	51
054		000								52
055		001	0001		1005000856-41		READ ONLY MEMORY		U28	53
056		001	0001		1005000856-42		READ ONLY MEMORY		U23	54
057		001	0001		1005000856-43		READ ONLY MEMORY		U24	55
058		001	0001		1005000856-44		READ ONLY MEMORY		U22	56
059		001	0001		1005000856-45		READ ONLY MEMORY		U26	57
060		001	0001		1005000856-46		READ ONLY MEMORY		U25	58
061		001	0001		1005000856-47		READ ONLY MEMORY		U27	59
062		001	0001		1005000856-48		READ ONLY MEMORY		U30	60
063		001	0001		1005000856-49		READ ONLY MEMORY		U29	61
064		001	0001		1005000796-39		READ ONLY MEMORY		U12	62
065		001	0001		1005000796-40		READ ONLY MEMORY		U13	63
066		009	0001		1001004974-1		RESISTOR CLUSTER		A1 THRU A9	64
067		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65
068		REF	0001		LD2001002169-1		LOGIC DIAGRAM			66
069		000								67
070		004	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX FT REQD	68
071		002	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C54,55 .25 IS	69
072		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 215	70
073		002	0001		CM05FD391J03		CAPACITOR	MIL-C-5/18	C56,58 .25 IS	71
074		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R10	72

CPB

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARK PART NUMBER 2001002169-1.			201
202		REF	0001				AREA TO BE FREE OF SOLDER.			202
203		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REFERENCE DESIGNATIONS.			204
205		REF	0001				MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
206		REF	0001				PROTRUSION (SIDE 2) .075 MAXIMUM.			206
207		000								207
208		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209		REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			209
210		REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN INSTALLATION.			210
211		REF	0001				FOR ASSEMBLIES -5 AND -9 ADD JUMPER (FIND NO. 58) FROM J2A1 TO J2A2 AND FROM J2B1 TO J2B2.			211
212		000								212
213		REF	0001				TAPE DOWN SOCKET FIND NUMBER 35 TO FIND NUMBER 2 USING FIND NUMBER 38 AND FIND NUMBER 70.			213
214		REF	0001				"X" DENOTES ICP LEAD TO BE BENT TO HORIZONTAL POSITION. PRECAUTION SHOULD BE TAKEN NOT TO BREAK OR CRACK LEADS.			214
215		REF	0001				SPOT BOND JUMPER WIRE (FIND NUMBER 68) USING FIND NUMBER 70 TO FIND NUMBER 2.			215
216		REF	0001				CONTINUED ON NEXT PAGE.			216

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
216						WIRE LIST (215).			216

REMARKS	FROM	TO	FIND NO.
	U60-2	U60-1	68
	U60-1	U65-11	
	U82-3	U82-4	
	U82-4	U53-1	
	E6	U82-5	
	U82-5	U53-15	
	U82-6	E15	
	E13	E10	
(214)	U67-11	E11	
	E11	E14	
	E14	U82-2	
	U82-2	U82-1	
	E9	E8	
	E7	U66-13	
(214)	U66-2	U66-1	
(214)	U64-9	U82-12	
	U82-13	U73-8	
(214)	U65-5	U65-4	
	U77-9	U77-7	
	E2	U83-2	
	E3	U83-1	
	U82-11	U50-10	
	U82-8	U45-2	
	U82-10	U82-9	
	U82-9	U69-6	
(214)	U67-4	E4	
	U47-3	U57-10	
	U47-2	U57-11	
(214)	U57-11	U76-2	
(214)	U76-2	E1	
(214)	U75-9	U75-10	
	U60-3	R2,R10	
	U83-7	U82-7	
	U82-7	E12	
	U83-14	U82-14	
	U83-14	E16	
	U80-2	U70-5	
	U80-1	U78-9	
	U68-1	U78-10	
	U40-9	E17	
	U40-12	E18	68

CPB

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		20001002166-0		ICM-CKT CARD ASSY		PROCUREMENT ONLY	1
002		001	0001		10010004808-1		PRINTED WRG BD, ICM			2
003		003	0001		121-7360-035	71468	INSULATOR, ECP4	ITT CANNON	70 POS (DUAL 35)	3
004		003	0001		121-7360-020	71468	INSULATOR, ECP4	ITT CANNON	40 POS (DUAL 20)	5
005		330	0001		030-7331-001	71468	CONTACT, ECP4	ITT CANNON	.094 THK BD	6

Interconnect Module, ICM, Parts List
PL2001002166-0, Rev. C, Sheet 2

	SYM	QTY REQD	SERIAL NO START	SERIAL NO END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		20001002166-1		ICM-CKT CARD ASSY		USED ON SUE 1110-1	1
002		001	0001		20001002166-0		ICM-CKT CARD ASSY			2
003		000								3
004		000								4
005		000								5
006		000								6
7		012	0001		4508 .75 WIDE	04963	FOAM TAPE	3M CO	APPROX INCH REQD	7

CPB

Interconnect Module, ICM, Parts List
PL2001002166-1, Rev. C, Sheet 3

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002232-1		IDM-CKT CARD ASSY		USED ON SUE 1110	1
002		000								2
003		001	0001		1001005188-1		CONNECTOR ASSY, IDM			3
004		006	0001		4508 .75 WIDE	04963	FOAM TAPE	3M CO	APPROX INCH REQD	4

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CPB

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CPB TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		CPB-05

SCALE	REV	SHEET
	A	1 OF 2

CPB - Processor Control Board Lockheed

also see CPA-Ø5

Status -

see CPA-Ø1

Switches - none

Jumpers ROM Size

Size	J2-A	J2-B
256	1 to 2	1 to 2
512	1 to 2	-
1024	-	-

U42 is installed for ROM sizes of 512 or 1024 words

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	- - -	

SEE CPB-Ø2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CPB

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER

APP'D FOR REL 12/8/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

CPB SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		CPB-2Ø

SCALE	REV	SHEET
	A	1 OF 1

Processor Control Board

CPC-Ø5 Technical Reference

FIGURE 5

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12-16-74	

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN	
	CHECKER	DRAWING TITLE: CPC TECHNICAL REF
	ENGINEER	
	APP'D FOR REL	SIZE: A; CODE IDENT NO.; DRAWING NO.: CPC-05
	APP'D (CUSTOMER)	SCALE; REV A; SHEET / OF

CPC

CPC - Processor Control Board Lockheed

also see CPA-Ø5

Status -

see CPA-Ø1

Switches - none

Jumpers

ROM Size

Size	J2-A	J2-B
256	1 to 2	1 to 2
512	1 to 2	-
1024	-	-

U42 is installed for ROM sizes of 512 or 1024 words