B 9499-6
DISK DRIVE ELECTRONIC CONTROLLER

TECHNICAL MANUAL
VOLUME 1

OPERATION AND MAINTENANCE

Burroughs

FIELD ENGINEERING

Library Binder 349A

Printed in U.S. America

March 1978

Form 2011342

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INTRODUCTION

This Field Engineering Technical Manual is prepared in a revised format as follows:

1) Volume 1, Operation and Maintenance
2) Volume 2, Illustrated Parts
3) Volume 3, Theory of Operation

The division of the manual into volumes provides a more complete concentration of the subject matter with respect to machine maintenance and theory.

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SECTION 1
FUNCTION AND OPERATION

GENERAL DESCRIPTION

Disk Drive Electronic Controller

The B 9499-6 Disk Drive Electronic Controller (DDEC) interfaces one B 1700 or B 1800 Series computer to a maximum of 8 disk drives. The disk drives may be any mix of B 9484-2, –5 or B 9494-4 drives (205, 206, or 207).

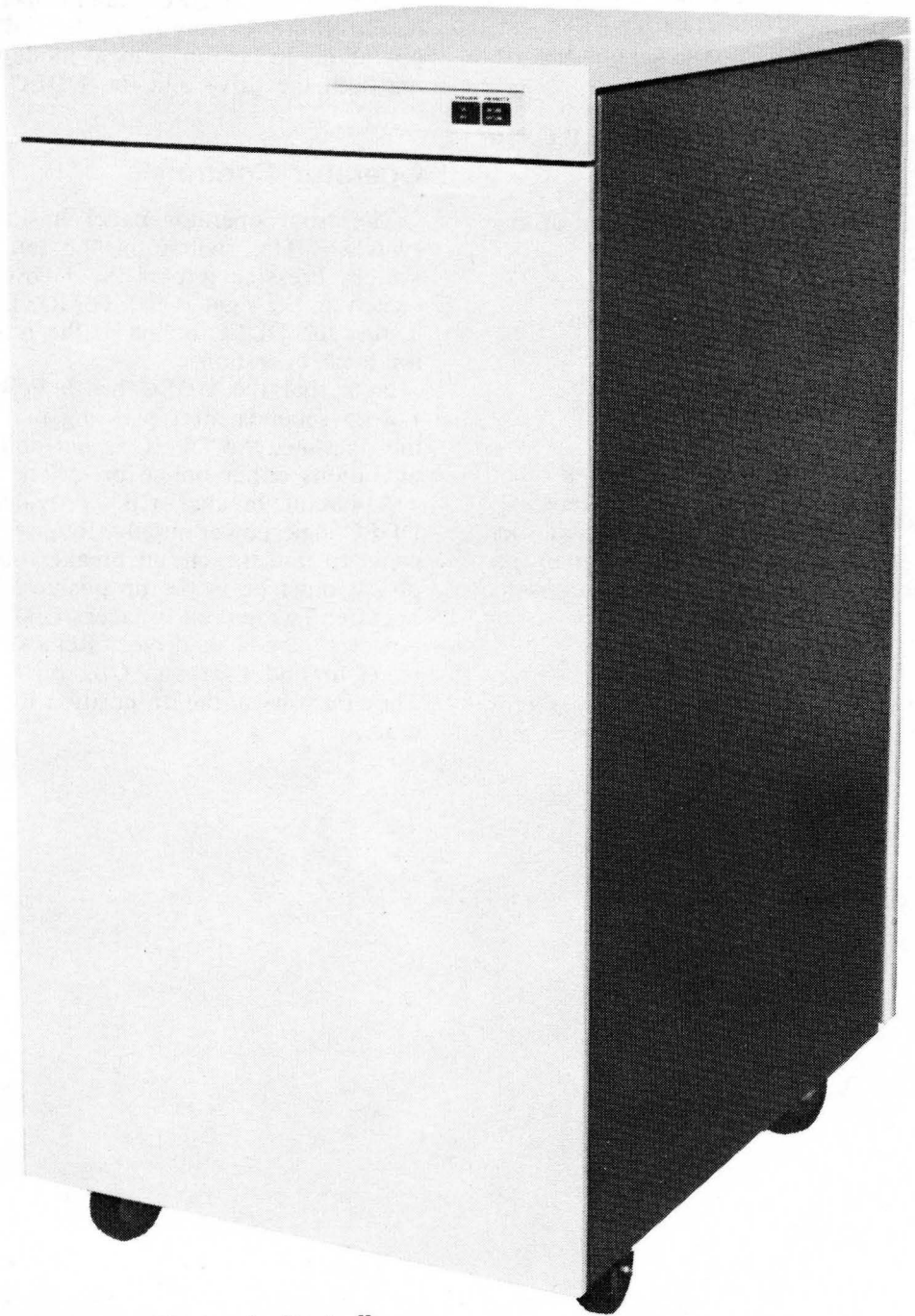


Figure 1-1. Disk Drive Electronic Controller

Subsystem

The DDEC receives commands from the Disk Pack Control (D.P.C.) in the central system, and interfaces with the required drive in order to complete the command. A typical command from the D.P.C. might be:

Read on unit 5 starting at sector 472824.

The following is the function of DDEC:

1) Select the required unit.
2) Decode the sector address into cylinder, Head and sector address for the type of drive.
3) Issue a seek command if necessary.
4) Read the addresses on the track until the required address is read.
5) Read the data into the DDEC, convert it from serial to parallel and transfer to the D.P.C. 16 bits at a time.
6) At the conclusion of the operation, report a result descriptor to the D.P.C. informing it of any errors detected during the operation.

NOTE

This is an over-simplified explanation intended to illustrate the operation in general terms. Actual operating details may be obtained in Volume 3, Theory of Operation.

In addition to reading, the DDEC performs other operations such as write, initialize, verify, relocate, read maintenance, and read Extended Result Descriptor. The intention of this volume is not to explain each of these operations. Volume 3 explains each in detail.

Error Detection

Error protection code (firecode) for every sector on disk enables the DDEC to detect read errors and to inform the system. The system retries a read operation if a read error occurs. Software attempts correction of a read error.

The DDEC can do error correction on a B 9494-4 (207) disk drive. It does error correction on a single sector basis when asked by the processor.

Local Operation

On line operations are simulated by a field engineer using the DDEC maintenance panel. Maintenance logic throughout the DDEC allows all operations to be run in local mode for troubleshooting both the drive and the DDEC.

Operator Controls

The front operator panel has two push button switches. The switch on the left is the POWER switch. Pressing it puts the DDEC on or off. The switch on the right is the REMOTE switch. Pressing it puts the DDEC online to the processor or offline for local operation.

Note that the DDEC has a Power Reset Timer. For 25 seconds after pressing the power switch to the on state, the DDEC is not able to perform any operations either online or offline.

A circuit breaker CB3 provides power to the DDEC logic power supply. Remove the DDEC front panel to find the circuit breaker on the Power Supply. It must be in the up position for the DDEC to operate. Two circuit breakers CB1 and CB2 provide power to the disk drives. Remove the DDEC rear panel to find CB1 and CB2 on the power supply. They must be in the up position for the drives to operate.

SECTION 2
INSTALLATION

SITE REQUIREMENTS

Floor Space

	Inches	CM
Width	22	54
Depth (including maintenance clearance)	102	257
Height	44	112

Normally the DDEC is bolted to one disk drive or between two drives.

Power

Input power is wired directly by an electrician. The wiring must enter the DDEC through the hole in the frame base at the right side. The DDEC can be powered by 60 Hz or 50 Hz power, either phase to phase or phase to neutral. Input voltage must be 208 to 240 volts AC. Many alternatives are given in this section under the title Power Conversions. Note that if the DDEC is wired to a single phase either line to line or line to neutral, a 1 x 4 Configuration is the maximum.

The DDEC provides power to the disk drives. Since the drives can be a mixture of B 9484-5 (206) and B 9494 - 4 (207), total power requirements for the subsystem can vary. Table 2-1 gives combinations of frequency and voltage and the drive and DDEC power requirements for each. Use Table 2-1 to calculate the total subsystem power requirement.

Cable Length

Four cable kits are available for the disk subsystem using the 206/DDEC

Cable Kits Part Number	1 x 2 2781 0050	1 x 4 2781 0068	1 x 6 2783 3680	1 x 8 2783 3698
I/O Cable 12 Ft.	1			
I/O Cable 14 Ft.		1	2	2
A/C GND 2 Ft.		1	1	2
A/C GND 3 Ft.	1	1	2	2
DC Logic GND 3 Ft.	2	2	4	4
DC Logic GND 4.5 Ft.		2	2	4

Environment

Operating
Temperature - 60 to 100 degrees F.
- 16 to 38 degrees C.
Relative humidity 10 to 90 percent.

Shipping and storage
Temperature - 50 to 160 degrees F.
- 45 to 71 degrees C.
Relative humidity up to 95 percent

Unpacking Instructions

The DDEC is shipped from the factory in a crate. The crate is a pallet, cushion supports for the DDEC, tri-wall card board top and four sided box. The DDEC is in a polyethylene bag. Styrofoam edge guards are put between the DDEC and the crate. The pallet, sides and top are held together with two straps.

To remove the DDEC from the packing crate:
1) Remove the two straps holding all together.
2) Remove the cardboard top.
3) Remove the edge guards from inside the crate.
4) Lift the cardboard box from the DDEC.
5) Remove the polyethylene bag from the D DEC.
6) Lift the DDEC from the pallet. At least two people are required to lift the DDEC safely.

DDEC Installation

After uncrating the DDEC, place it in approximately the position where it is finally to be installed. Before any drives are placed beside it, some check-out and cabling must be done.

Preinstallation Checkout

The following checks must be made with no power applied to the DDEC
1) Remove the front, rear, and side panels from the DDEC
2) At the rear of the DDEC remove the tape which holds the circuit cards in the card cage.
3) Press each circuit card to be sure it is fully inserted into the backplane.
4) On the power supply on the base of the cabinet, remove the six bolts which hold the power supply cover to the sides.
5) Inspect the power supply for shipping damage including loose wires, scraped wires or loose components.
6) On the outside of the power supply, at the right rear side locate the AC/DC ground shorting jumper wire. Remove the nut securing one end of this wire and pull that end from it s stud.
7) Using a VOM or DVM measure the resistance between the frame and the DC ground stud on the backplane. The DC ground stud is on the right side of the backplane when facing the

wired side. The resistance should be greater than one megohm.
8) Replace the shorting jumper wire removed in step 6.
9) Remove the AC cover on the right side of the power supply.
10) Switch CB3 to the down (off) position. CB3 is located on the front cover of the power supply.
11) Using a VOM or DVM measure the resistance between TB1 terminals 1, 2, 3 and 4. All combinations must measure greater than one megohm.
12) Switch CB3 to the up (on) position. The resistance between TB1-1 and TB1-2 must be low but is greater than 0.6 ohm. Switch CB3 to the down (off) position.
13) Replace the power supply top cover.

Table 2-1. Subsystem Power Requirements

UNIT	FREQ.	VOLTAGE	START CURRENT A	WORST CASE A	VA	BTU/HR	KCAL/HR
B9284-2/5	60HZ	208v	21.0	7.0	1455	3975	1000
205/206		240	24.2	8.0	1920	5240	1340
DUAL	50	200	22.6	7.5	1500	4090	1030
DRIVE		220	25.0	8.2	1804	4930	1242
		230	23.2	7.7	1770	4840	1218
		240	27.2	9.0	2160	5900	1488
B9494-2	60	208					
(SINGLE							
SPINDLE		240					
207							
DRIVE)	50	200					
		220					
		230					
		240					
B9494-4	60	208		8.5	1768	4820	1214
(DUAL							
SPINDLE		240		7.0	1680	4590	1158
207							
DRIVE)	50	200		8.0	1600	4360	1100
		220		7.8	1730	4720	1190
		230		7.5	1725	4710	1188
		240		6.6	1585	4320	1090
B9499-6	60	208	N/A	2.1	436	1190	300
206/7							
DDEC		240	N/A	1.9	456	1245	314
	50	200	N/A	2.4	480	1310	330
		220	N/A	2.2	484	1321	333
		230	N/A	2.2	506	1380	348
		240	N/A	2.1	504	1375	350

AC Power Input

Power input cables must be installed by an electrician. The field engineer must determine the specifications of the available power. If the available power is not the same as the required power as stamped on the machine label, some change must be made to the DDEC. See the changes below the heading *Power Conversions* in this section.

The following procedure is to be used to connect the AC input lines to the DDEC

1) Remove the AC cover from the right side of the power supply.
2) The hole-piece through which the input cable passes to TB1 is designed for conduit pipe to be clamped. The conduit must pass up through the hole in the DDEC base, then turn 90 degrees to be clamped at the hole-piece beside TB1
3) If the normal 3 phase, neutral, and ground input wires are provided, connect.

Phase A	to	TB1 - 1
Phase B	to	TB1 - 2
Phase C	to	TB1 - 3
Neutral	to	TB1 - 4
Ground	to	E7 (stud under and to the left of TB1)

4) Replace the AC cover.

Verify that the transformer tap chosen on the DDEC power supply at TB3 is rated the same as the input voltage. The method for making changes is under the heading *Voltage Tap Conversion* in this section.

DDEC to D.P.C. Cabling

The interface between the DDEC and the D.P.C. in the processor is a 25-wire coaxial cable. Before positioning drives beside the DDEC install the processor interface cable. Pass the cable up through the hole in the base of the DDEC cabinet and bring it to the rear of the card cage. Attach it to circuit card 16 (third card from left in the lower row of cards). The processor end must connect to the D.P.C. at the I/O connector panel.

Subsystem Installation

Before proceeding with these installation steps be sure that all AC input wiring to the DDEC has been done, that the necessary conversions have been made to the DDEC power wiring, and that the processor interface cable has been installed in the DDEC

Cabinet Bolting Procedure

The disk drives are shipped each with a set of brackets to bolt it to the drive or DDEC next to it. Install the bolting hardware using the procedure which follows, position the drives beside the DDEC and level all cabinets, and then complete the wiring for the subsystem.

1) Remove all panels from all cabinets.
2) Sort front and rear bolting brackets. In a set there are two long brackets painted black for the cabinet front members. There are two small brackets which are cadmium plated. They are for the cabinet rear members.
3) Move the cabinets near to their final positions but leave one or two feet between them.
4) Mount left-hand and right hand front brackets to adjacent vertical frame members at the front of the cabinets. Each is secured with four 8-32 screws with lock washers and flat washers. Do not tighten the mounting hardware until alignment has been done.
5) Mount left-hand and right-hand rear brackets to adjacent vertical frame members at the rear of the cabinets. Each is secured with two 8-32 screws with lock washers and flat washers. Do not tighten the mounting hardware until alignment has been done.
6) Move the first drive into it's final position beside the DDEC
7) On the cabinets just aligned, move the front bracket which has slotted mating holes so that it is flush with the front of the frame and tighten it's mounting screws. Move the adjacent bracket with tapped holes so that it is behind the bracket on the other cabinet. Tighten the mounting hardware.

NOTE

Step 7 requires sliding the cabinets apart and back together several times to place the brackets correctly. Remember that the bracket with slotted holes must finally overlap the bracket with tapped holes when the cabinets are brought together. This permits the screws which hold the brackets together to be installed and tightened from the outside of the cabinet.

8) Repeat step 7 for the rear brackets.
9) Follow the above procedure for all cabinets. Finally move all cabinets to their positions with front and rear brackets overlapping correctly.
10) Level the cabinets and align their top panels by lowering and adjusting the four levelling jacks in each cabinet.
11) Install two 8-32 screws, lock-washers and flat washers in each set of front brackets and one screw and washer in each set of rear brackets.

Cabling

For B 9495-5 (206) disk drives a cable trough is formed along the rear of the cabinets. All interconnecting cables are laid in the J member brackets behind the rear frame uprights on each drive. This permits the rear covers to be installed on the drives and DDEC with no cable interference.

For B 9494-4 (207) disk drives a cable trough is formed along the top of the cabinets. Remove the top covers of the drives and lay interconnecting cables in the trough. To reach the DDEC the cables pass down the cable trough on the side of the drive closest to the DDEC More cabling information is found in the installation section of the drive technical manual.

Power Distribution

The disk drives in the subsystem are powered from the four receptacles at the rear of the DDEC power supply. Before proceeding, place all circuit breakers in the off position.

Lay the drive power cables in the cable trough and insert the plug for each in one receptacle at the rear of the DDEC Store excess cable at the drive.

Grounding

Ground cables come as part of the cable kits. They are green. The heavy gauge cables are AC ground cables. The lighter gauge cables are DC ground cables.

The installation section of the drive technical manuals has information about ground interconnection which is useful.

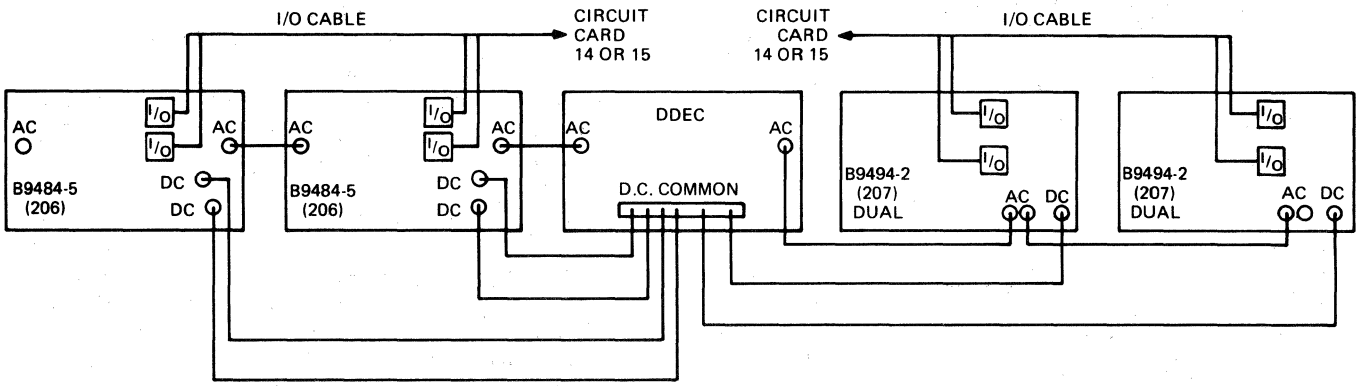


Figure 2-1. Cabling Configuration Example

Figure 2-1 gives an example of a 1 x 8 mixed subsystem with four B 9494-4 (207) drives and four B 9484-5 (206) drives. The AC and DC ground cables are shown in figure 2-1.

The following rules apply to ground cables in the subsystem:

1) Link all the machines in a *daisy chain* between AC ground connections.
2) Each DC ground in the drives must be joined with a separate wire to the DC common terminal block at the rear of the DDEC power supply. The common ground point where AC ground and DC ground are joined is the DDEC The B 9494-4 (207) drive has only one DC ground for both drives since the DC power supply is common. The B 9484-5 (206) has a separate DC ground for each spindle.
3) Route all ground wires in the cable trough.

AC - DC Ground Jumper

The DDEC provides a common connection for AC and DC ground. The DDEC is shipped with AC ground and DC ground joined by a jumper wire.

If isolation is required between AC ground and DC ground remove the jumper wire. It is located on the right side of the power supply, at the rear of the DDEC. It joins the two terminals labelled E2 (DC ground) and E6 (AC ground).

DDEC/DPD Cables

The drive interface coaxial cable is provided in the cable kit. One cable is required for four spindles (two drives). For units 0, 1, 2 and 3 connect one interface cable to circuit card 14. For units 4, 5, 6 and 7 connect one interface cable to circuit card 15.

Lay the drive interface cables along the bases at the rear of the 206 drives and along the cable troughs on top of the 207 drives (top cover removed). Connect the interface plugs to the drive receptacles. The plugs are marked 1 to 4 corresponding to spindle address 0 to 3 and 4 to 7.

See figure 2-1 for an example of cabling. Also see the installation section of the drive technical manuals for more cabling information.

Configuration Switches

Document 07.03.01 in the T and F Document package shows two sets of switches which designate to the DDEC the subsystem configuration.

Drive Present Switch

This is located on circuit card 04. It is a set of eight switches in a dual-in-line package at location B4 on the card. Figure 2-2 shows which switch corresponds to each drive unit. The on position designates that unit present. Set these switches to indicate the same drive units present as the jumper chip in the DPC indicates.

Drive Type Switch

This is located on circuit card 03 at location D1. In the on position, the switch designates the unit a B 9494-4 (207) type drive. In the off position, the switch designates the unit a B 9484-2/5 (205/206) type

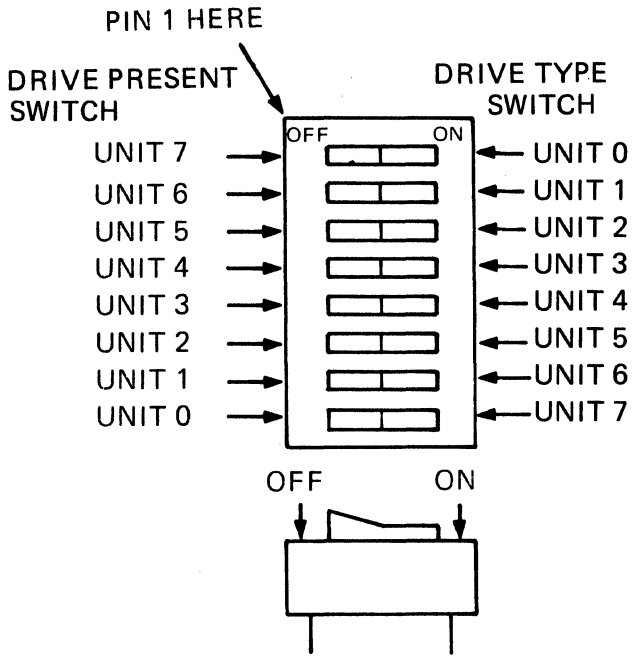


Figure 2-2 Configuration Switch

drive. These switches must be correct for the DDEC to communicate with the drive. The unit type jumpers in the DPC must correspond also. See the jumper chip instructions for the disk pack control in the processor.

Power Conversions

The DDEC is shipped from the factory wired for one of the following configurations:

1) 60 Hz, 3 phase, line to line voltage of 208 to 240 volts.
2) 50 Hz 3 phase, line to line voltage of 208 to 240 volts.

The field engineer must check which transformer primary tap is used at TB3 on the power supply. If the tap used is different from the input voltage available, change the connection at TB3. See *Voltage Tap Conversion* in this section.

The DDEC label is attached to the base of the machine, behind the front panel. It gives the configuration for which the DDEC is wired. If there is any difference between that configuation and the power available, one or more of the following deviations must be made.

1) 50 to 60 Hz Conversion
2) 60 to 50 Hz Conversion
3) Single Phase Conversion
4) Phase to Neutral Conversion
5) Voltage Tap Conversion

50 to 60 Hz Conversion

1) In 50 to 60 Hz conversion kit check that the transformer supplied bears part number 2783 6683.
2) Ensure that all AC power is removed from DDEC by first disconnecting any known power source.
3) Remove all side panels by loosening the two clamps at the bottom of the frame below each panel with a 7/16 inch open end wrench, then raising each panel and pulling it away from the frame at the top end.
4) Remove the AC cover on the right side of the power supply with a flat screwdriver applied to its four screws. With an AC voltmeter measure between all terminals of TB1. There should be no voltage indicated.
5) Remove the six screws securing the top cover of the power supply using a flat screwdriver. Slide the top cover forward and out of the machine.
6) Remove the four screws securing the front cover of the power supply. Allow the front cover to rest loosely away from the power supply.
7) Unplug J7 and P7 and remove P7 from the front panel with a flat screwdriver used to compress the springs holding it to the sheet metal.
8) On the printed circuit board on the top of the power supply module, remove the screw holding the white wire to the board in the front, left corner, marked TB4, 5V out (left terminal).
9) In the same location as step 8, remove the screw holding two black wires to the board, marked +5VRTN (right terminal).
10) At TB3 in the lower, front right corner of the power supply module, remove the screw holding the green/yellow wire to the separate terminal screw with a ground sign ⏚ (above TB3).
11) At TB3 remove all wires from the terminal screws.
12) Remove the two screws securing the front of the power supply module to the base of the DDEC using a long flat screwdriver.
13) Loosen but do not remove the corresponding two screws securing the rear of the power supply module.
14) Grasping the power supply module by its built in handles on the front, pull it slightly forward then tip it up and lift it from the power supply and place it on a table.
15) Unplug the three secondary output wires of the transformer from the top of the printed circuit board. These wires are brown, brown and purple and are plugged onto terminals marked F, B, and A. (it does not matter which brown wire goes to F or which goes to B).
16) Using a flat screwdriver remove the three screws holding the two red wires and one blue wire to terminals marked C, E, and D on the top of the circuit board. (it does not matter which red wire goes to C, or which goes to E).

17) Remove the two large screws and four washers holding C103 and the two screws and four washers holding C102 (both are marked) to the printed circuit board on top of the power supply.
18) Using a Phillips screwdriver remove the seven screws around the edge of the circuit board then raise the board from the metal frame and set it on one side. At this time note the part number stamped on the 50 Hz transformer. It should be 2783 7244.
19) At the inside of TB3 described in step 10, unplug the blue wire from the terminal marked *com* (far right). Unplug the black wire from the terminal marked 200V (second from right). Unplug the orange wrie from the terminal marked 220V (third from right). Unplug the yellow wire from the terminal marked 230V (fourth from right). Unplug the red wire from the terminal marked 240V (fifth from right).
20) At the rear base of the power supply module, remove the rubber cap covering the end of C101) Unplug the two white wires from the terminals of C101, (it does not matter which white wire goes to which terminal).
21) Unbolt the transformwer from the base by removing the four nuts using a 7/16 inch nut driver. Lift the transformer from the power supply.
22) From the 50Hz - 60Hz conversion kit take the transformer and ensure the part number stamped on it is 2783 6683. If correct, bolt it to the base of the power supply module using the four nuts removed in step 21) Place the transformer so that the side with wires is on the inside of the power supply.
23) Remove the label above TB3 indicating a 50Hz power supply and replace with the 60Hz from the kit with new voltage assignments for the terminals.
24) Remove the label showing the part number of the power supply module as 2782 3789 and replace it with the new lable from the conversion kit with part number 2783 7872.
25) Plug the blue wire from the transformer which has a plug end into the rear of TB3 at the terminal marked common (far right). Plug the black wire onto TB3 terminal marked 208V (second from right). Plug the orange wire onto TB3 terminal marked 240V (third from right).
26) Plug the two white wires on to each terminal of C101 at the left rear base of the power supply. Replace the rubber cap on C101) (It does not matter which white wire goes to which terminal.
27) Replace the circuit board on the metal frame, taking care to hold the remaining transformer wires so that they curl around the front of the board to its top without pinching them between any components. Secure the board to the metal with the seven Phillips screws removed in step 18.
28) Plug one brown wire from the transformer onto the circuit board terminal marked F at the center front of the board. Plug the other brown wire onto the board terminal marked B. It does not matter which brown wire goes to terminal F and which goes to terminal B or which red wire goes to terminal C and which goes to terminal E. Plug the purple wire onto the board terminal marked A. Using the screws removed in step 16, fasten one red wire from the transformer to the board terminal marked C, the other red wire to the board terminal marked E, and the blue wire to the board terminal marked D.
29) Secure the two capacitors C102 and C103 to the circuit board using the two screws for each removed in step 17.
30) Reinstall the power supply module in the base of the DDEC by setting it forward of its final position, and then sliding it to the rear to engage the two screws securing it to the base at the rear. Refit two screws at front and tighten all four screws.
31) Connect the white wire to the TB4 terminal marked 5 Volt (left terminal) in the left front corner of the circuit board using the screw removed in step 8.
32) Connect the two black wires to TB4 terminal marked 5VRTN (right terminal) using the screws removed in step 9.
33) Connect the green/yellow ground wire to the TB3 terminal marked with the ground sign ⏚ above TB3 using the screw removed in step 10.
34) At TB3 in the lower front right corner of the power supply module, connect one white AC input wire, along with the white wire from each of the two sheathed fan harness cables all to TB3 terminal marked *com* (far right terminal). The other white AC input wire along with the black wire from each of the sheathed fan harness cables should be connected to the appropriate terminal of TB3 depending on the voltage source. Determine from the electrician what voltage the source is before connecting these wires. The second from right terminal is for 208V input. The third from right terminal is for 240V input. It does not matter which white AC input wire goes to *com,* and which goes to the voltage input terminal.
35) Mark in ink the power conversion label 2783 7608 with the correct voltage, frequency and phase information, and attach this adjacent to the machine nameplate label at the rear.
36) With circuit breaker CB3 on front cover power supply turned off, apply AC power source

to the machine. With an AC voltmeter measure the voltage between TB3-1 and the other terminal of TB3 connected in step 34. Be sure that the terminals used on TB3 in step 34 correspond to the voltage measured here. Change the terminal used in step 34 if necessary, being sure AC source is disconnected before making changes.

37) Using the four screws removed in step 6, fasten the front cover power supply to the rear cover power supply.
38) Using the six screws removed in step 5, fasten the top cover power supply to the rear cover power supply.
39) Refit the AC cover over TB1 and secure with the four screws removed in step 4.
40) Turn CB3 and check that all fans operate.
41) Refit all side panels to the DDEC by engaging them in the two holes at the top, then tightening the two clamps in the frame below each panel.

60 to 50 Hz Conversion

1) In 60 to 50 Hz conversion kit check that the transformer supplied bears part number 2783 7244.
2) Ensure that all AC power is removed from DDEC by first disconnecting any known power source.
3) Remove all side panels by loosening the two clamps at the bottom of the frame below each panel with a 7/16 inch open end wrench, then raising each panel and pulling it away from the frame at the top end.
4) Remove the AC cover on the right side of the power supply with a flat screwdriver applied to its four screws. With an AC voltmeter measure between all terminals of TB1) There should be no voltage indicated.
5) Remove the six screws securing the top cover of the power supply using a flat screwdriver. Slide the top cover forward and out the machine.
6) Remove the four screws securing the front cover of the power supply. Allow the front cover to rest loosely away from the power supply.
7) Unplug J7 from P7 and remove P7 from the front panel with a flat screwdriver used to compress the springs holding it to the sheet metal.
8) On the printed circuit board on the top of the power supply module, remove the screw holding the white wire to the board in the front, left corner, marked TB4, 5V out (left terminal).
9) In the same location as step 8, remove the screw holding two black wires to the board, marked +5VRTN (right terminal).
10) At TB3 in the lower, front right corner of the power supply module, remove the screw holding the green/yellow wire to the separate terminal screw with a ground sign ⏚ (above TB3).
11) At TB3 remove all wires from the terminal screws.
12) Remove the two screws securing the front of the power supply module to the base of the DDEC using a long flat screwdriver.
13) Loosen but do not remove the corresponding two screws securing the rear of the power supply module.
14) Grasping the power supply module by its built in handles on the front, pull it slightly forward then tip it up and lift it from the power supply and place it on a table.
15) Unplug the three secondary output wires of the transformer from the top of the printed circuit board. These wires are brown, brown and purple and are plugged onto terminals marked F, B, and A. It does not matter which brown wire goes to F, or which goes to B.
16) Using a flat screwdriver remove the three screws holding the two red wires and one blue wire to terminals marked C, E, and D on the top of the circuit board. (it does not matter which red wire goes to C or which goes to E).
17) Remove the two large screws and four washers board on top of the power supply.
18) Using a Phillips screwdriver remove the seven screws around the edge of the circuit board then raise the board from the metal frame and set it to one side. At this time note the part number stamped on the 60Hz transformer. It should be 2783 6683.
19) At the inside of TB3 described in step 10, unplug the blue wire from the terminal marked *com* (far right). Unplug the black wire from the terminal wire from the terminal marked 240V (third from right).
20) At the rear base of the power supply module, remove the rubber cap covering the end of C101) Unplug the two white wires from the terminals of C101, (it does not matter which white wire goes to which terminal).
21) Unbolt the transformer from the base by removing the four nuts using a 7/16 inch nut driver. Lift the transformer from the power supply.
22) From the 60Hz - 50Hz conversion kit take the transformer and ensure the part number stamped on it is 2783 7244. If correct bolt it to the base of the power supply module using the four nuts removed in step 21) Place the transformer so that the side with wires is on the inside of the power supply.
23) Remove the label above TB3 indicating a 60Hz power supply and replace with the 50Hz label from the kit with new voltage assignments for the terminals.
24) Remove the label showing the part number of

the power supply module as 2783 7872 and replace it with the new label from the conversion kit with part number 2783 3789.

25) Plug the blue wire from the transformer which has a plug end into the rear of TB3 at the terminal marked common (far right). Plug the black wire onto TB3 terminal marked 200V (second from right). Plug the orange wire onto TB3 terminal marked 220V (third from right). Plug the yellow wire onto TB3 terminal marked 230V (fourth from right). Plug the red wire onto TB3 terminal marked 240V (fifth from right).
26) Plug the two white wires on to each terminal of C101 at the left rear base of the power supply. Replace the rubber cap on C101) (It does not matter which white wire goes to which terminal).
27) Replace the circuit board on the metal frame, taking care to hold the remaining transformer wires so that they curl around the front of the board to its top without pinching them between any components. Secure the board to the metal with the seven Phillips screws removed in step 18.
28) Plug one brown wire from the transformer onto the circuit board terminal marked F at the center front of the board. Plug the other brown wire onto the board terminal marked B. It does not matter which brown wire goes to terminal C and which goes to terminal E. Plug the purple wire onto the board terminal marked A. Using the screws removed in step 16, fasten one red wire from the transformer to the board terminal marked C, the other red wire to the board terminal marked E, and the blue wire to the board terminal marked D.
29) Secure the two capacitors C102 and C103 to the circuit board using the two screws for each removed in step 17.
30) Reinstall the power supply module in the base of the DDEC by setting it forward of its final position then sliding it to the rear to engage the two screws securing it to the base at the rear. Refit 2 screws at front and tighten all four screws.
31) Connect the white wire to the TB4 terminal marked 5V out (left terminal) in the left front corner of the circuit board using the screw removed in step 8.
32) Connect the two black wires to TB4 terminal marked 5VRTN (right terminal) using the screw removed in step 9.
33) Connect the green/yellow ground wire to the terminal marked with the ground sign ⏚ above TB3 using the screw removed in step 10.
34) At TB3 in the lower front right corner of the power supply module, connect one white AC input wire, along with the white wire from each of the two sheathed fan harness cables all to TB3 terminal marked *com* (far right terminal). The other white AC input wire along with the black wire from each of the sheathed fan harness cables should be connected to the appropriate terminal of TB3 depending on the voltage source. Determine from the electrician what voltage the source is before connecting these wires. The second from right terminal is for 200V input. The third from right terminal is for 222V input. The fourth from right terminal is for 230V input. The fifth from right terminal is for 240V input. It does not matter which white AC input wire goes to *com* and which goes to the voltage input terminal.
35) Mark in ink the power conversion label 2783 7608 with the correct voltage, frequency and phase information and attach this adjacent to the machine nameplate label at the rear.
36) With circuit breaker CB3 on front cover power supply turned off, and CB1 and CB2 on rear cover power supply turned off, apply AC power source to the machine. With an AC voltmeter measure the voltage between TB3-1 and the other terminal of TB3 connected in step 34. Be sure that the terminals used on TB3 in step 34 correspond to the voltage measured here. Change the terminal used in step 34 if necessary, being sure AC source is disconnected before making changes.
37) Using the four screws removed in step 6, fasten the front cover power supply to the rear cover power supply.
38) Using the six screws removed in step 5, fasten the top cover power supply to the rear cover power supply.
39) Refit the AC cover over TB1 and secure with the four screws removed in step 4.
40) Turn CB3 on and check that all fans operate.
41) Refit all side panels to the DDEC by engaging them in the two holes at the top, then tightening the two clamps in the frame below each panel.

Single Phase Conversion

Use this method when only 2 phase power is available. Line to line voltage is 208 to 240 volts. Figure 2-3 shows the method of connecting the input power.

1) Connect line 1 to TB1 terminal 1 and terminal 3.
2) Connect line 2 to TB1 terminal 2.
3) Connect neutral to TB1 terminal 4.
4) Connect ground to E7 below TB1.

If the single phase method of installation is used, only J3 and J4 may be used to power drives. J3 is the lower left receptacle on the front panel power

supply. J4 is the upper right receptacle. The drives are wired in the normal line to line manner.

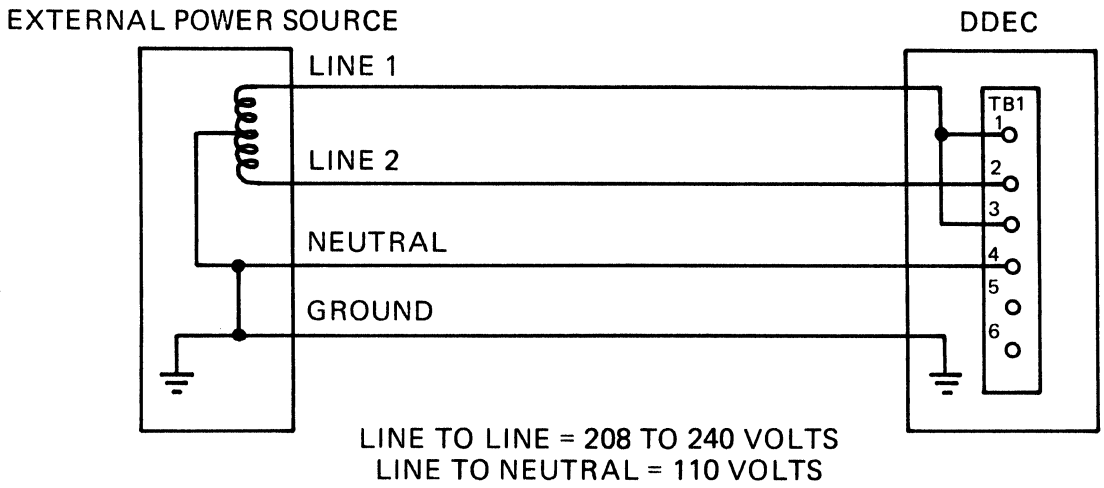


Figure 2-3. Single Phase Input Power Connection

Line to Neutral Conversion

When the 206/7 DDEC is powered from an AC source which provides 200 VAC to 240 VAC measured from line to neutral, two conversions must be done.

1) Rewire the power distribution in the DDEC according to the following procedure.
2) Select the correct transformer tap according to the procedure below the heading *Voltage Tap Conversion*.

The following rewiring procedure must be performed to install the DDEC with line to neutral AC input power. Figure 2-4 shows the conversion.

1) Remove the power supply top cover.
2) Find TB6. It is bolted to the inside of the power supply on the right-hand side.
3) Find CB3. It is bolted to the inside of the front cover of the power supply.
4) Unplug the quick-connect and wire from CB3 terminal 1. This wire can be identified by its extra length.
5) Uncoil the wire removed in step 4 and pass it down the right side of the power supply. Plug the quick-connect to TB6 terminal 7.
6) Be sure the wire does not interfere with the fan for the power supply.
7) Replace the power supply top cover.

Any disk drives powered from the DDEC must be converted to line-neutral operation.

Voltage Tap Conversion

Use this procedure when the input voltage is greater than the transformer tap rating for which the DDEC power supply is wired. The primary tap of the power supply transformer must be chosen to correspond to the input voltage. Figure 2-5 is TB3, located on the power supply module, front right corner. TB3 terminals are marked for the appropriate tap. Terminal 1 must have one input line connected as well as one wire from each of the fan harness cables. The other input line must go to the correct terminal of TB3 according to the line voltage. Remaining fan harness wires connect to the same terminal.

Checkout Procedure

The following steps must be used when doing a check out of the DDEC and the subsystem after installation.

Power on Checks

1) Be sure that all the requirements have been met in this section for powering the DDEC and cabling it to the drives and the processor.
2) Be sure that all installation steps for the drives have been followed.
3) Move the switch on CB3 at the front of the power supply to the up position. Off and offline should be indicated on the front operator panel switches. If on or online is indicated, press the switch to change it to off or offline.
4) Check that the three fans are operating. One is on the front of the power supply. Two are on the sides of the card cage.
5) Look through the two fans on the card cage to see that the airflow switches are activated. The vanes on these switches may be caught due to shipping vibration.

DC Voltage Check

1) Press the power switch on the operator panel to light the on indicator.
2) Using a DVM, measure the voltage between the two studs on the backplane. The stud on

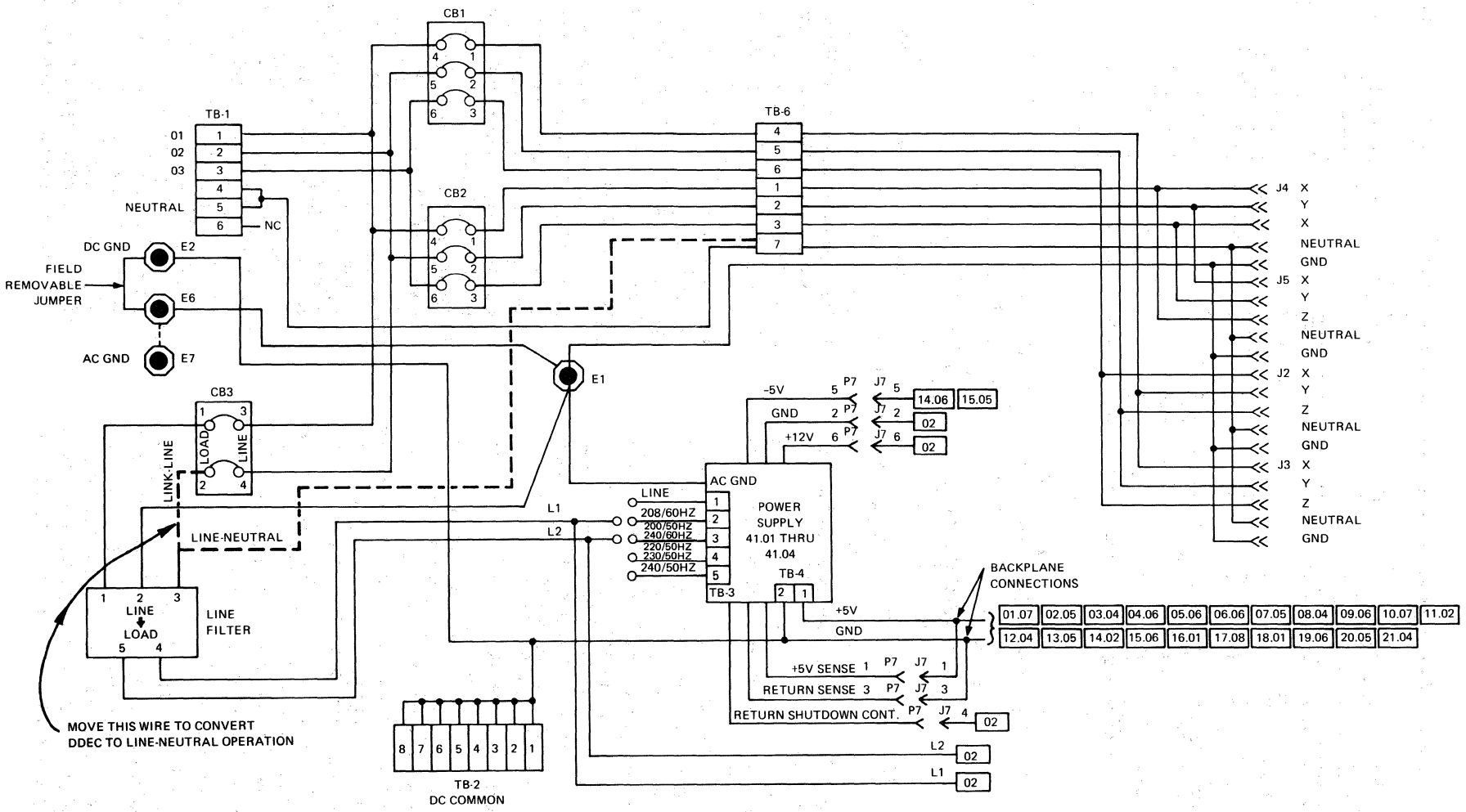


Figure 2-4. Schematic Showing Line-Neutral Conversion

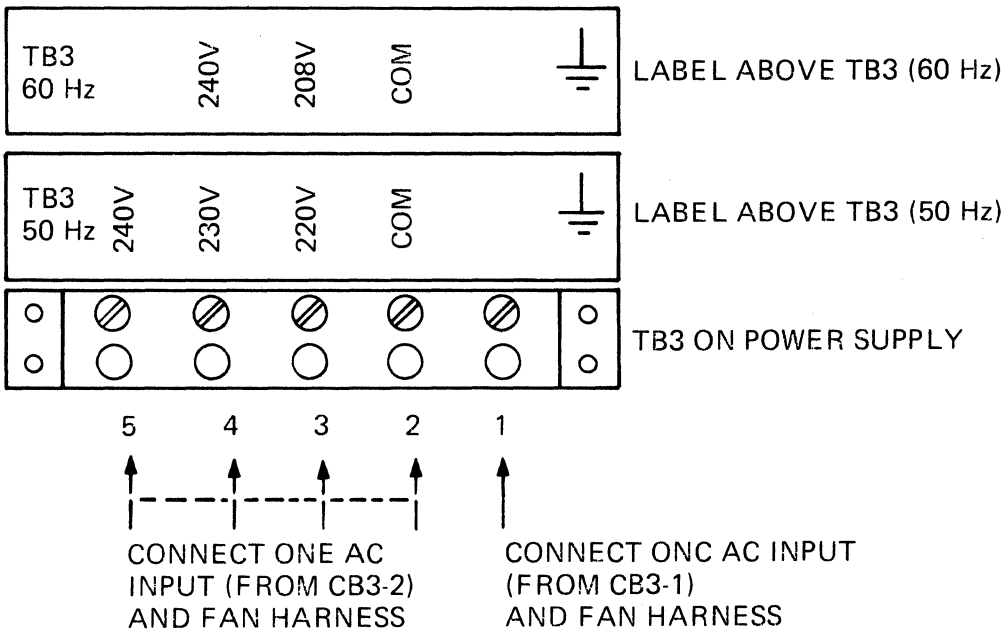


Figure 2-5. TB3 Connections

the left must be +5 volts referenced to the stud on the right (DC ground).

3) Measure the voltage at the backplane pin QHC01. It must be –5 volts referenced to the DC ground stud.
4) Adjust the +5 volts and –5 volts using potentiometer adjusting tool. The adjusting potentiometers are located on the rear edge of the printed circuit card of the power supply unit. The top cover of the power supply must be removed in order to adjust the voltages. Sheet 07.03.02 of the Test and Field Documents package illustrates the voltage adjustment.

Clock Frequency Check

1) Using a frequency counter or oscilloscope, measure the internal DDEC clock at the backplane test point DDE17. Be sure that the drive clock is not selected at this time. To ensure the clock at the test point is *local clock*, put DDEC offline and press MSTR CLEAR on the maintenance panel.
2) There is no adjustment of the local clock frequency. The frequency must be between 9.25 MHz and 10.75 MHz.

Local Operations

1) At the rear of the DDEC observe the address counter display. Some LED's should be illuminated.
2) Press MSTR CLEAR on the maintenance panel. All LED's on the maintenance panel are illuminated while MSTR CLEAR is pressed.
3) Do a test operation from the maintenance panel. Section 4 of this technical manual gives details for doing operations in local mode. The result descriptor must be NR and OL since the drive is not powered on.
4) Power on a drive. Ensure that the write enable switch on the drive is not illuminated.
5) Repeat a test operation with a drive powered on the heads loaded. The result descriptor must have no error bits set.
6) Test all operations on one drive. Use caution. Write, initialize, and relocate operations destroy customer data and system software. For all such operations, install a scratch pack or use only the maintenance cylinder.
7) Power On all drives in the subsystem and verify that operations can be performed with each in local mode.

Online Operations

1) Press the REMOTE switch on the operator panel of the DDEC to light the online button.
2) At the processor, use the latest revision of the Disk Pack Diagnostic and its listing to exercise the disk subsystem.
3) If no problems exist in local mode and under test from the processor, installation is complete. Replace all panels on the DDEC and drives.
4) Cold start and clear start as instructed in the System Software Operational guide in order to prepare the system for customer use.

SECTION 3
DOCUMENTATION AND COMPONENTS

REFERENCE DOCUMENTS

The following is a list of publications which apply to the B 9499-6 DDEC.

Field Engineering Technical Manual:	Form Number:
Volume 1, Operation and Maintenance	2011342
Volume 2. Parts Catalogue	2011359
Volume 3. Theory of Operation	2011367
Reference Card	3026929

Test and Field Documents

General

The T & F documents are divided into Sections as shown in table 3-1.

Table 3-1. T & F Sections

Section	Contents
01	Index
02	Block Diagrams
03	Flow Charts
04	Timing Diagrams
05	Control Equations
06	I.C. Locations
07	Assembly and Set-up Details
08	Backplane Circuit Lists
09	Schematics
10	MTR

Each section is divided into subjects and each subject has a number of physical pages associated with it. Each page is numbered according to section, subject no., and physical page number.

Example:

03.08.01 Page 1 of the flow chart for data transfer
03.08.02 Page 2 of the flow chart for data transfer
09.04.06 Page 6 of the schematic, DM-ERD control OP code Decode.

Description

Index

The index lists each subject in each section, giving the section no., subject no., title of subject, and the Engineering Document Number.

Block Diagrams

The block diagrams are intended to assist in understanding the structure of the unit. The overall block diagram contains the main blocks. Each of the blocks in the overall block diagram contains a reference. This reference is a page where a block diagram of each of the main blocks can be found.

In the individual block diagrams, a reference number in each block points to the schematic page where the logic can be seen.

Flow Charts

The flow charts consist of an overall mode flow diagram, showing how the modes link together and an individual flow for each mode.

An individual mode flow chart is depicted in figure 3-1. The flow generally starts at the top left hand and flows from left to right. If the conditions above the double horizontal line are met, the action below the double horizontal line is performed. The action performed is sometimes different depending on whether the unit selected is a 206 or 207. In some cases 206 or 207 is shown as a condition. In some cases, two actions are given, however, one action has (206) next to it and the other has (207). In some cases the flow splits into two, one for 206 and the other for 207.

Control Equations

The control equations are contained in section 5. They are the equations for the control logic only - not the complete unti. The control logic consists of the logic that controls the flows. The unit was designed from these equations.

Schematics

The schematics are cross-referenced for easy signal tracing. Refer to figure 3-2 for details about cross-referencing, IC types, IC locations, backplane pin locations, IC pin numbering, etc.

In most cases the signal is named according to the function if performs. The Glossary of Terms in appendix A of this technical manual explains each signal and gives the schemtatic page where the signal is sourced. A mixture of positive and negative logic is used in TTL. When negative logic is used, signal name is terminated with a slash (/). Also the signal starts from a negation symbol (bubble) and goes into a bubble.

NAND, NOR, AND, OR gates are drawn in the way in which they are used. Figures 3-3 and 3-4 show the same logical function. The schematic shown in figure 3-3 is used because it is visually easier to understand.

The backplane locations of each printed circuit board is marked on sheet 1 of the schematic for each board. For example, on page 09.10.01 of the T & F

Document package, the words E UPPER are printed above the page number. Sheet one of the schematics for circuit board ten is 09.10.01. 10. Circuit board 10 corresponds on the backplane to the upper set of pins in column E.

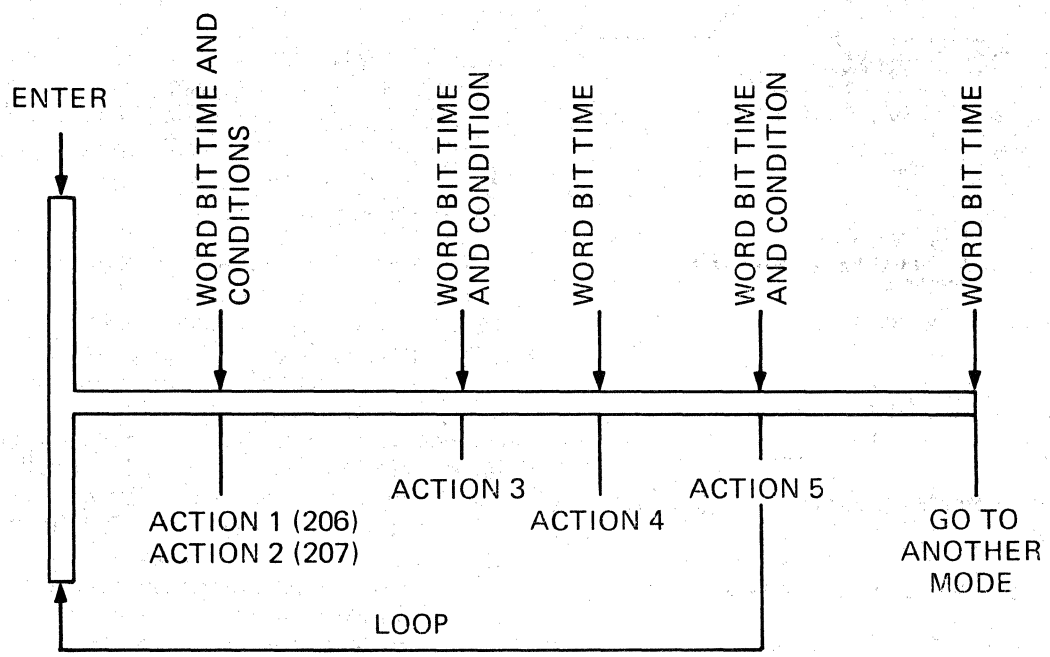


Figure 3-1. Flow Chart Example

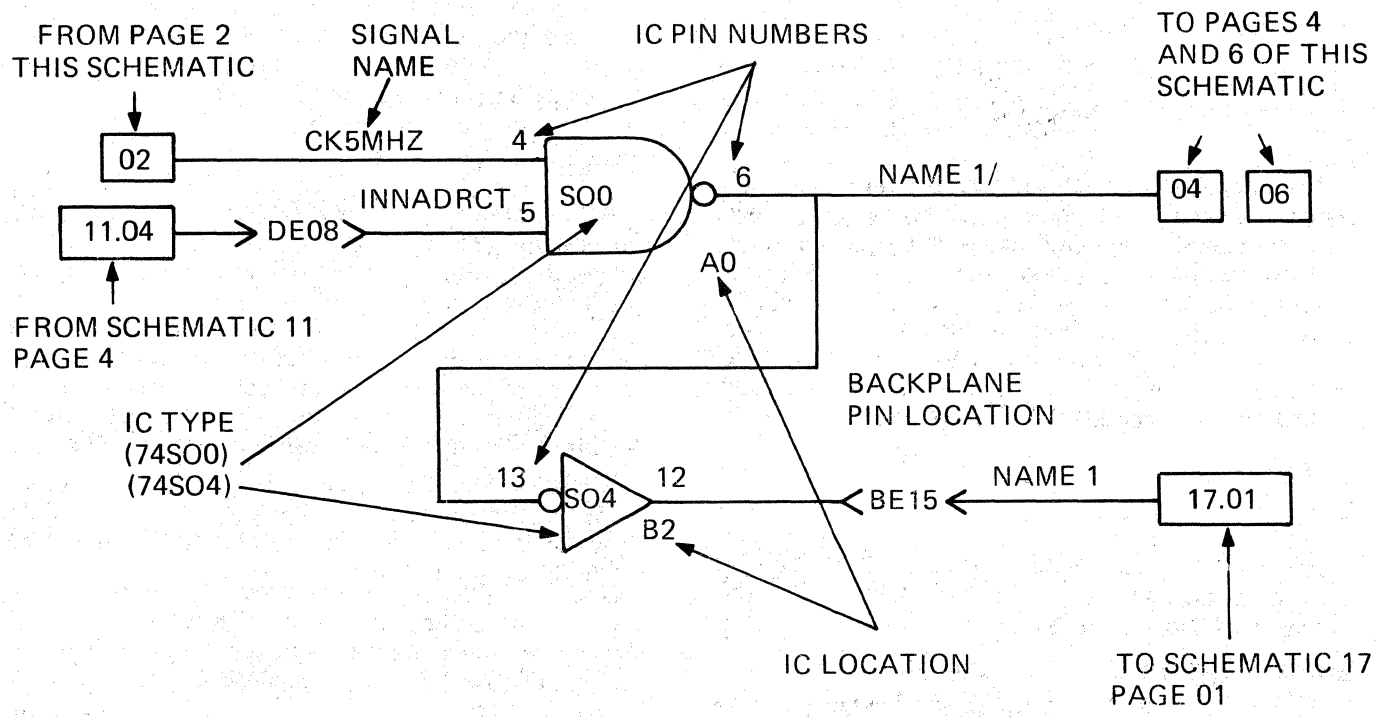


Figure 3-2. Schematic Details

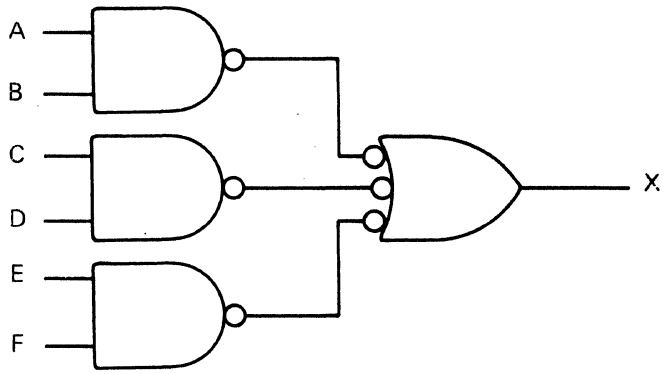


Figure 3-3. Negative or Function

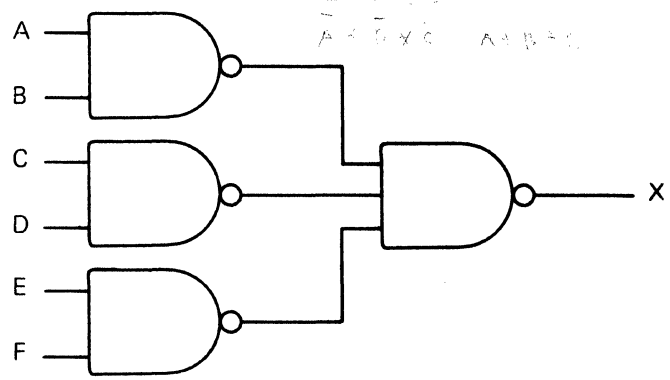


Figure 3-4. Positive NAND Function

Backplane Wirelist

Section 08 of the T & F Documents contains the Backplane Wirelist. Signal names are listed in alphabetical order. The first column after the name is the source pin for that signal.

The *From* and *To* columns name every pin which is wired into each network. The last column gives the level of the backplane wire on the pins. Level 1 is closest to the base of the pins. Level 2 is further out on the pins. There are only 2 levels of backplane wiring.

Component Location System

Backplane Pins

Backplane pins are called up on the schematics and the backplane wire list according to the following example:

QFE23

Refer to figure 3-5 to locate this pin.

Q - is marked along the top of the backplane. This marks a card slot which may be upper or lower.

F - is marked along the sides of the backplane. This gives a horizontal reference to identify 60 pins for each card slot.

E - is marked at the top of a column of pins. This marks a vertical row of pins on the etch side of the card slot.

23 - is marked at the sides of the backplane. This identifies the pin.

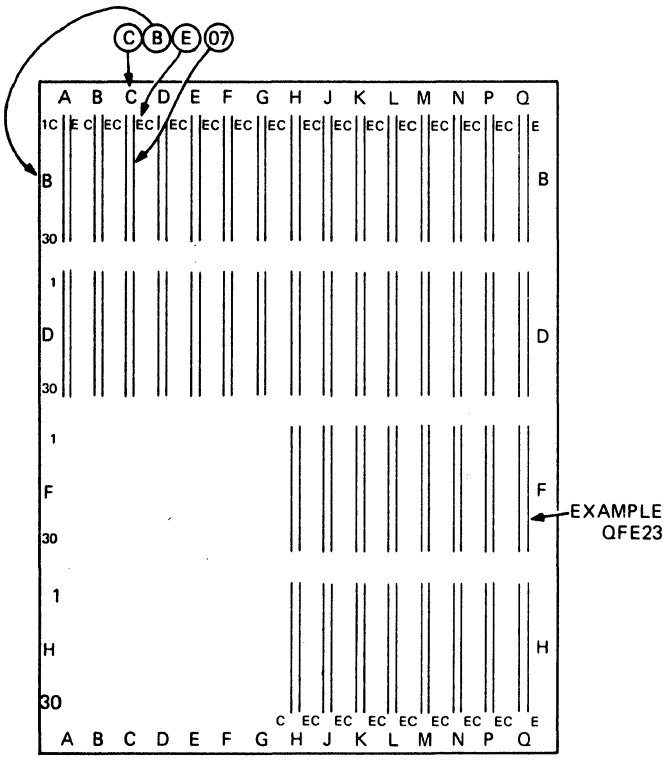


Figure 3-5. Front View Backplane

Printed Circuit Boards

IC Locations

Figure 3-6 shows the component side of a typical printed circuit board. The columns of ICs are lettered from A to H. The rows are numbered from 0 to 5. Schematics refer to IC locations by a letter and a number. For example C3. This is column C, row 3.

Edge Connector Contact Numbering

Figure 3-6 shows the component side of a typical printed circuit board. Backplane contacts are at the right side of figure 3-6. Each contact has a four character designation. For example HE19.

1st Character	This can be B, D, F, or H. B is for the top half and D is for the bottom half of a board located in the upper row of cards in the DDEC. F and H are for the top half and bottom half of a board located in the lower row of cards in the DDEC.

2nd Character	This can be C for the component side of the card or E for the etched side of the card.
3rd and 4th Character	Are the pin number from 1 to 30.

Frontplane contacts are shown on the left edge of the card in figure 3-6. On a circuit board with one set of frontplane contacts, they are numbered from 1 to 20. The prefix is FC for component side and FE for etch side. Circuit board 13 has two sets of frontplane contacts. The prefix GC is the top of the card, component side. Prefix GE is the top of the card, etch side. Prefix HC is the bottom of the card, component side. Prefix HE is the bottom of the card, etch side.

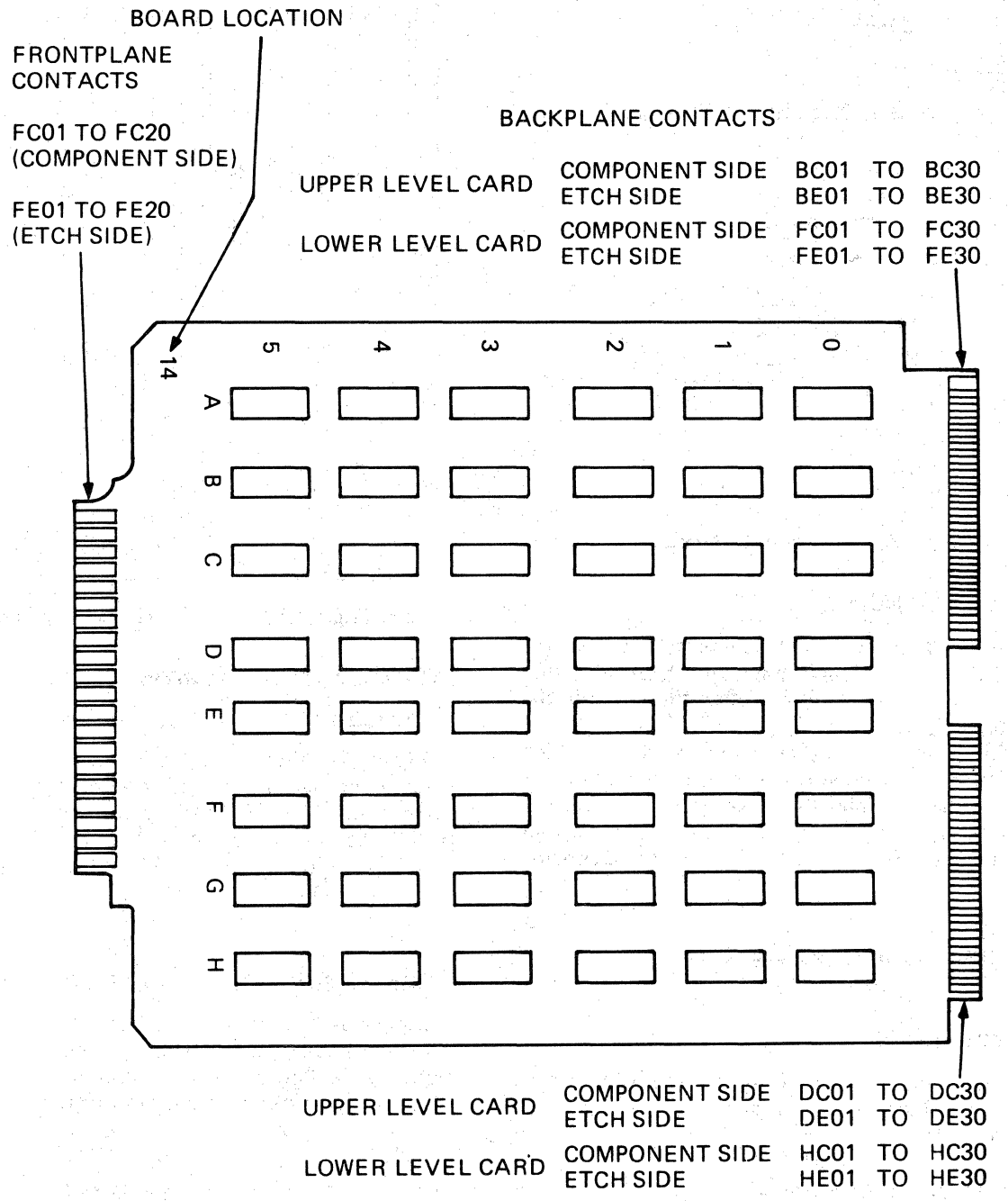


Figure 3-6. Typical PCB

Component Reference Charts

GENERAL DESCRIPTION

In the unit schematics ICs are identified by an abbreviated manufacturers number.

example:

S251 means 74S251

A list of abbreviations is contained at the front of the Schematics. T.T.L. is used with the exception of a few specialized ICs. A description of the T.T.L. family types is given in table 3-2.

Table 3-2. TTL Family Types

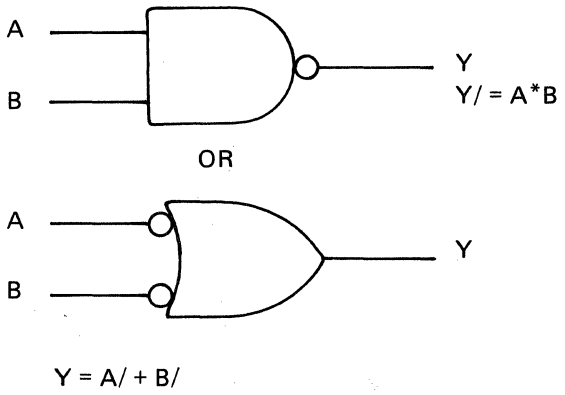
SERIES	GATES		FLIP-FLOPS
	Propogation Delay	Power Dissipation	Max Clock Frequency
74LSnn (Low Power Schottky)	9.5 ns	2 mw	45 MHz
74L nn (Low Power)	33 ns	1 mw	3 MHz
74Snn (Schottky)	3 ns	19 mw	125 MHz
74 nn (Standard)	10 ns	10 mw	35 MHz
74Hnn (High Power)	6 ns	22 mw	50 MHz

Schottky T.T.L. contains Schottky barrier diode clamped inputs in order to prevent saturation of the inputs and lower output resistances. These two factors provide low propogation times. Schottky T.T.L. is used for high speed applications. Schottky T.T.L. should never be tied to ground due to excessive heat dissipation when the output is in the high state. No T.T. L. should be tied to +5V since this destroys the output transistor when the output tries to go low.

Three State logic is used on the data buses in the unit. The three states are: High, Low and High Impedence. This enables many outputs to be connected to a bus, however, all except one is in high impedence mode. The output not in high impedence mode determines whether the bus is high or low.

REFERENCE CHARTS

SCHEMATIC:



PIN NUMBERING:

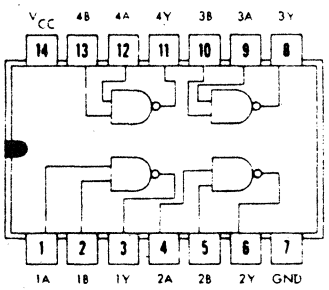
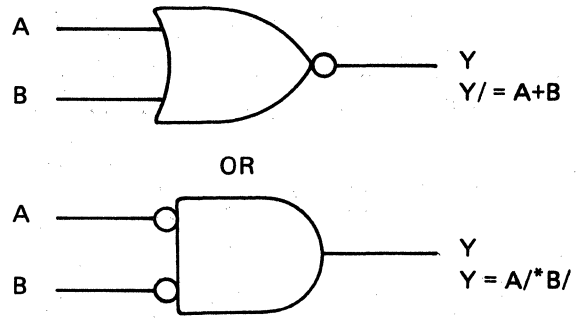


Figure 3-7. 7400 74S00 Quad 2-Input Positive NAND Gate

SCHEMATIC:



PIN NUMBERING:

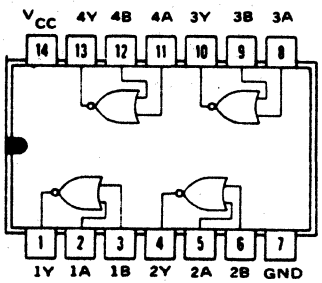
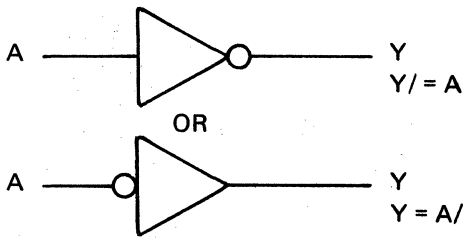


Figure 3-8. 7402 74S02 Quad 2-Input Positive NOR Gate

SCHEMATIC:



PIN NUMBERING:

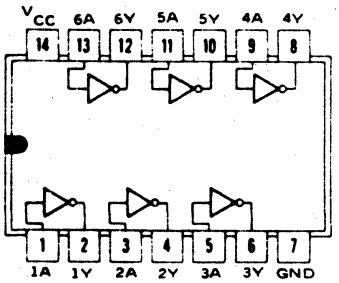
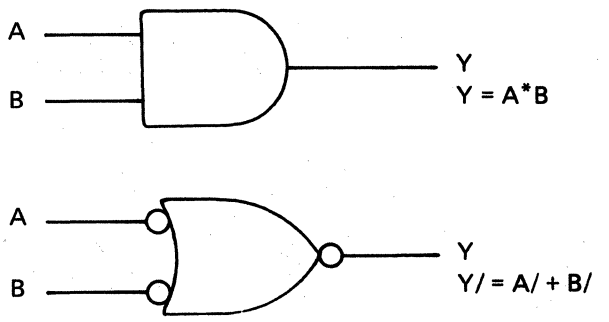


Figure 3-9. 7404 74S04 74H04 Hex Inverter

SCHEMATIC:



PIN NUMBERING:

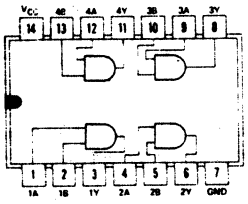


Figure 3-10. 7408 74S08 Quad 2-Input and Gate

SCHEMATIC: PIN NUMBERING:

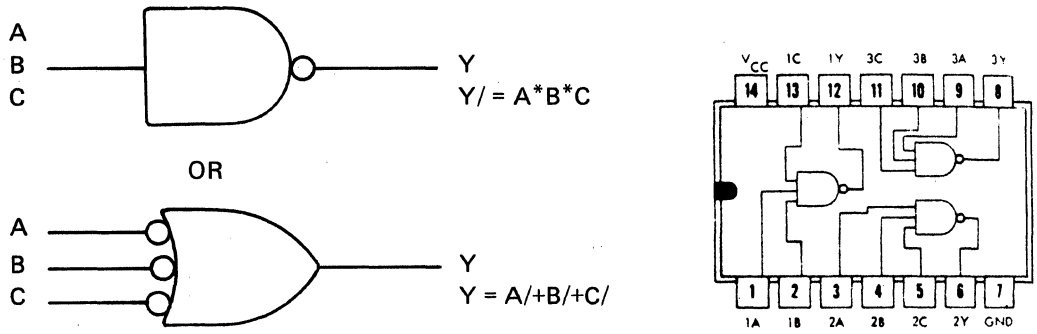


Figure 3-11. 7410 74S10 Triple 3-Input Positive NAND Gate

SCHEMATIC: PIN NUMBERING:

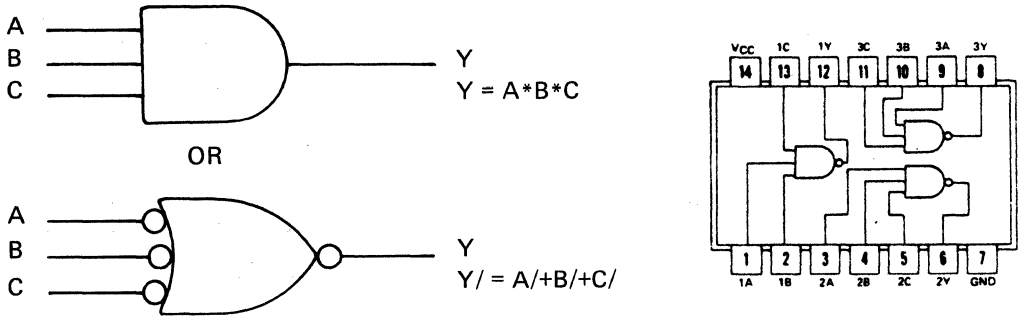


Figure 3-12. 74S11 Triple 3-Input Positive and Gates

SCHEMATIC: PIN NUMBERING:

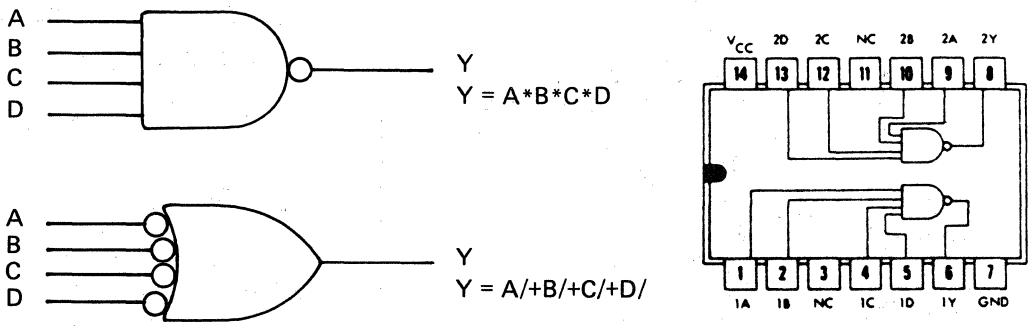
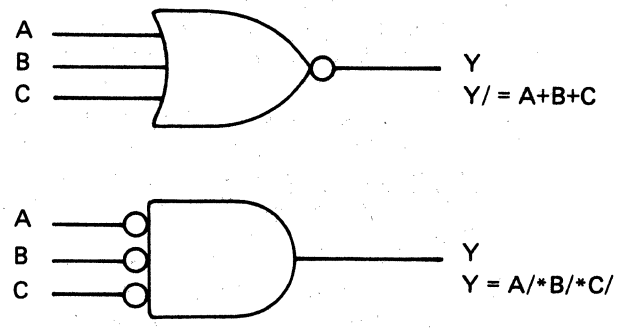


Figure 3-13. 7420, 74S20 Dual 4-Input Positive NAND Gates

SCHEMATIC:



PIN NUMBERING:

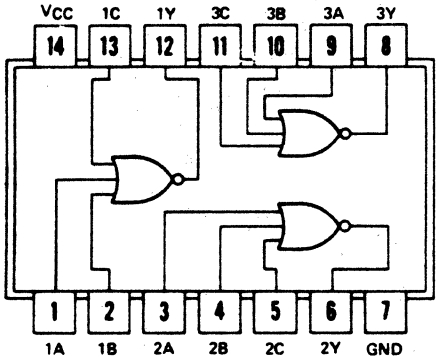
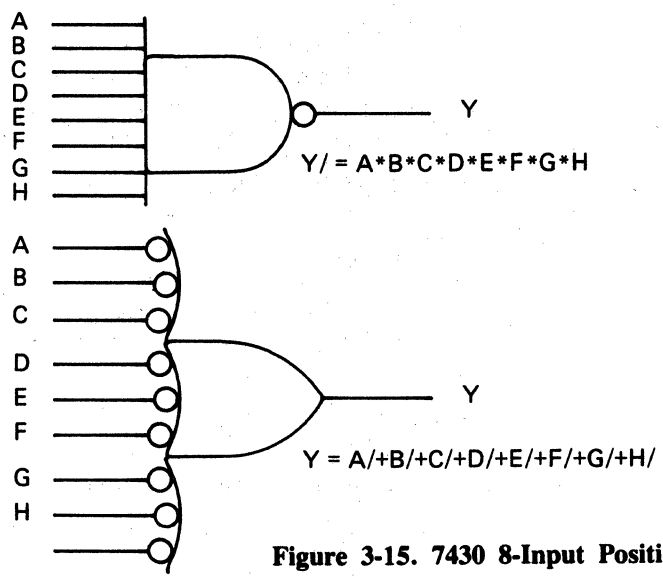


Figure 3-14. 7427 Triple 3-input Positive NOR gates

SCHEMATIC:



PIN NUMBERING:

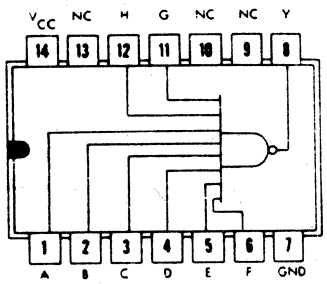
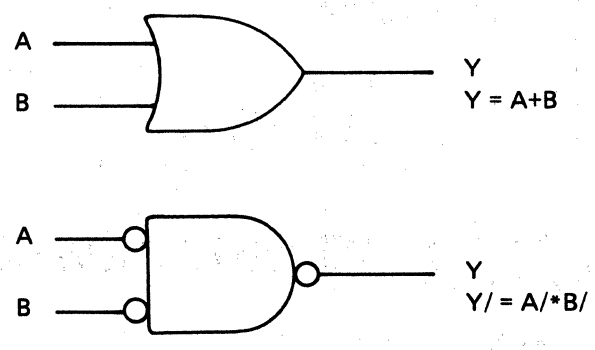


Figure 3-15. 7430 8-Input Positive NAND Gate

SCHEMATIC:



PIN NUMBERING:

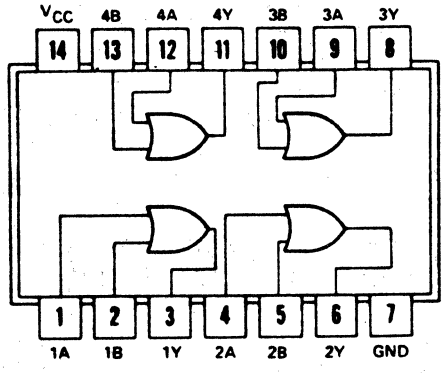
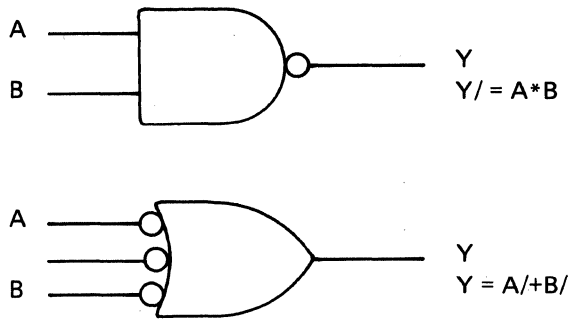


Figure 3-16. 7432 Quad 2-Input Positive or Gates

SCHEMATIC:



PIN NUMBERING:

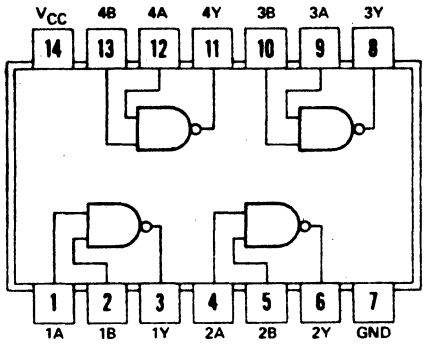
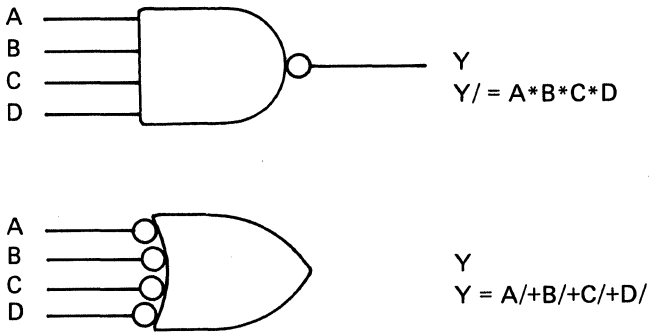


Figure 3-17. 7437 Quad 2-Input NAND Buffers

SCHEMATIC:



PIN NUMBERING:

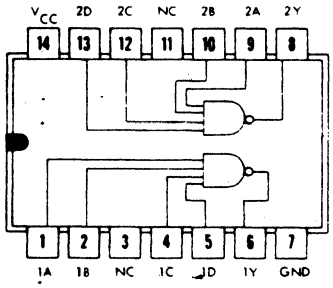
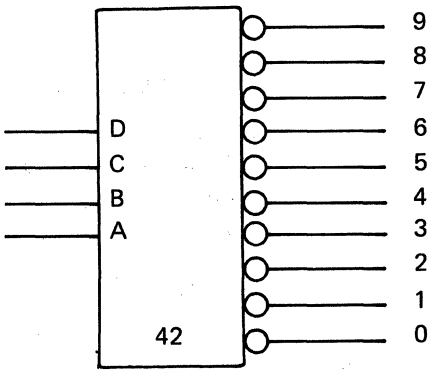


Figure 3-18. 7440 74S40 Dual 4-Input NAND Buffers

SCHEMATIC:



PIN NUMBERING:

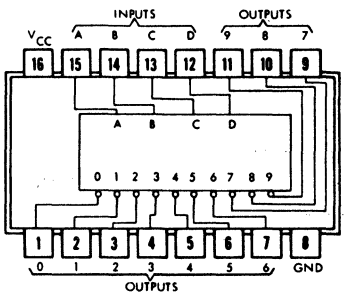
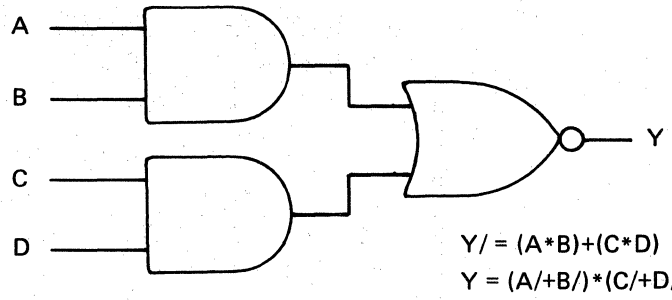


Figure 3-19. 7442 4-10 Line Decoder

Description:

The 7442 is a BCD to decimal decoder. A Binary input zero through nine is decoded to make one output low. (The rest are high). Input values from 10-15 are invalid and all outputs are held high. Inputs A, B, C and D are weighted 1, 2, 4 and 8 respectively.

SCHEMATIC:



PIN NUMBERING:

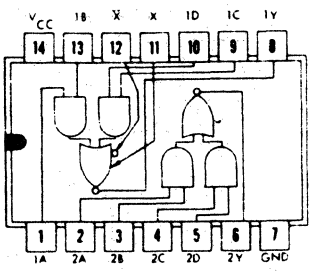
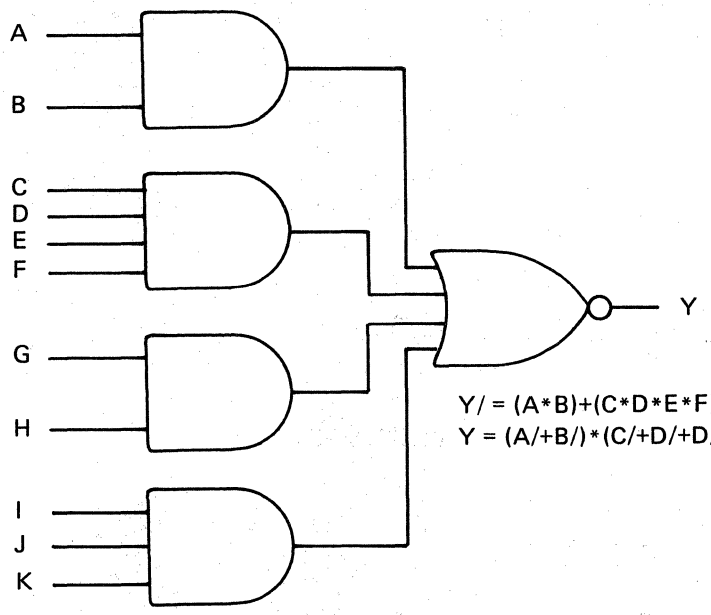


Figure 3-20. 74H51 Dual 2-Wide 2-Input and OR Invert Gates

SCHEMATIC:



PIN NUMBERING:

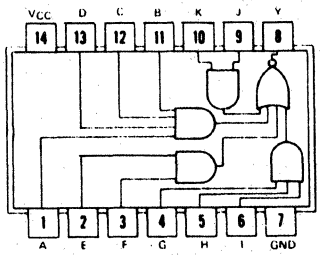
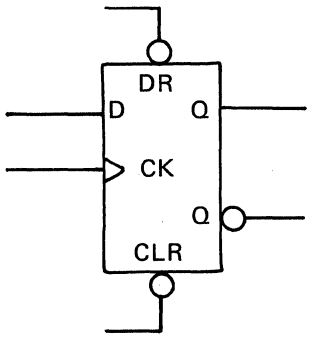


Figure 3-21. 74S64 4-2-3-2 - Input and-OR-Invert Gates

SCHEMATIC:



PIN NUMBERING:

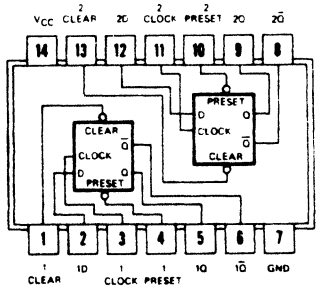
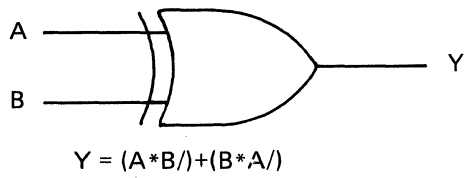


Figure 3-22. 7474 74S74 Dual D-Type Flipflop

Description:

The flipflop can be set by a low on PR and reset by a low on CLR. The positive edge of the clock triggers the flipflop. If D is high the flipflop sets on the clock, if D is low the flipflop resets on the clock.

SCHEMATIC:



PIN NUMBERING:

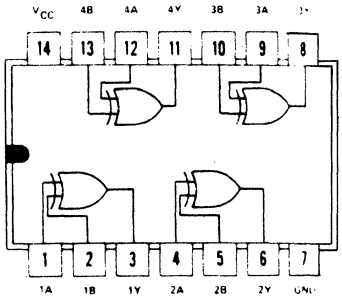
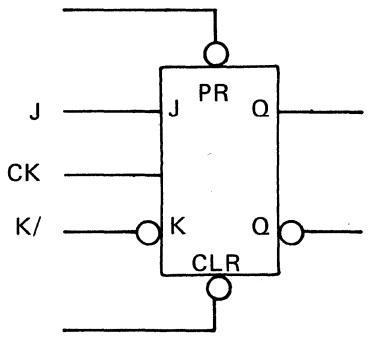


Figure 3-23. 7486 74S86 Quad 2-Input Exclusive OR Gates

SCHEMATIC:



PIN NUMBERING:

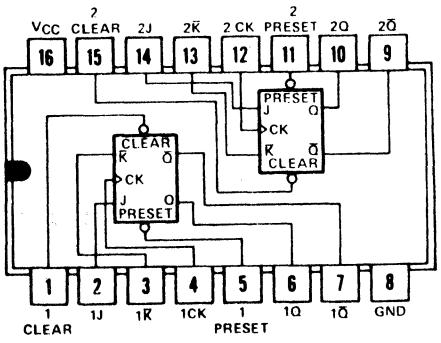


Figure 3-24. 74S109 Dual J K/ flipflop

Description:

A low on PR sets the flipflop. A low on CLR resets the flipflop.

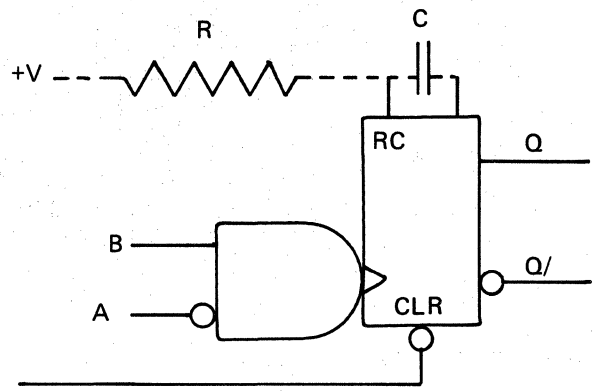
If J is low and K/ low, the flipflop resets on the positive edge of the clock.

If J is high and K/ is high the flipflop sets on the positive edge of the clock.

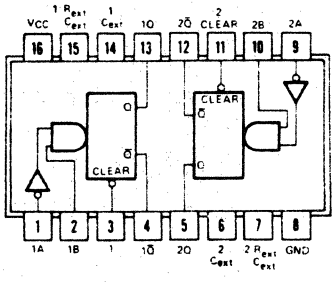
If J is high and K/ is low, the flipflop toggles (changes state) on the leading edge of the clock.

If J is low and K/ is high there is no change in the state of the flipflop when the clock occurs.

SCHEMATIC:



PIN NUMBERING:



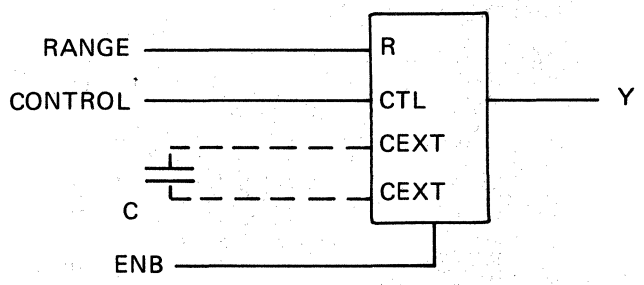
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Figure 3-25. 74123 Dual Retriggerable Monostable Multivibrator

Description:

A low CLR resets the timer. (Q Low and Q/high). When the input conditions are met (B high and A low) a pulse is generated at the output with the length dependent on R and C. The output pulse can be extended by retriggering the IC before it has timed out. The output pulse extends a length depending on RC.

SCHEMATIC:



PIN NUMBERING:

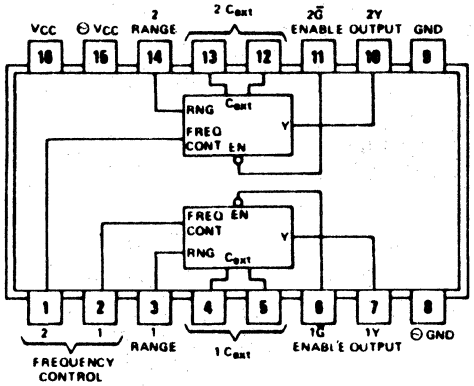
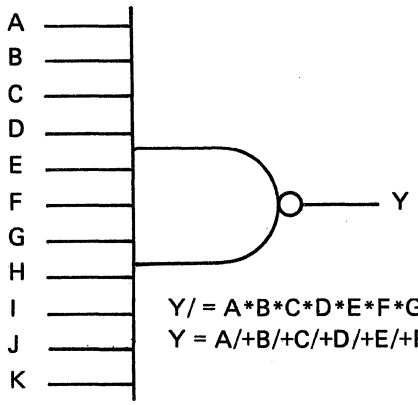


Figure 3-26 74S124 Dual Voltage-Controlled Oscillator

Description:

When enable goes low, the output is enabled, giving a square wave out-put. The frequency is dependent on CEXT, Range Voltage and control voltage.

SCHEMATIC:



PIN NUMBERING:

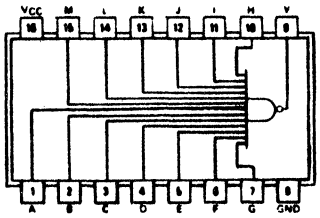
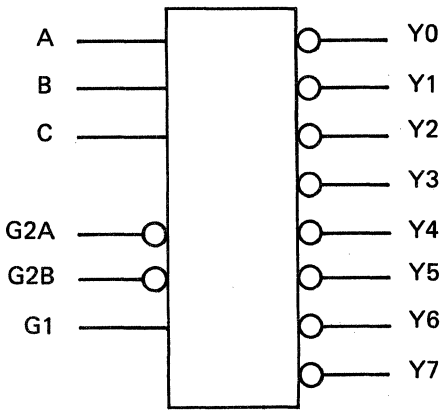
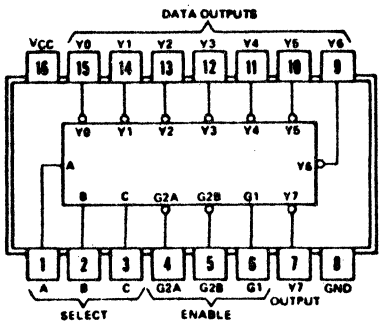


Figure 3-27. 74S133 13-Input Positive NAND Gates

SCHEMATIC:



PIN NUMBERING:



INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

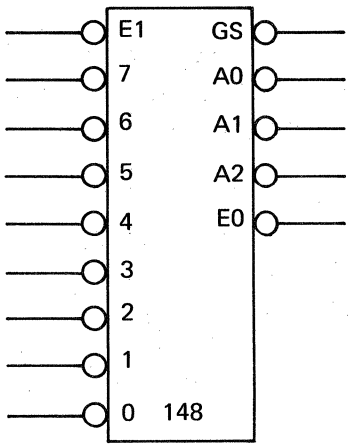
H = high level, L = low level, X = irrelevant

Figure 3-28. 74S138 Decoder/ Demultiplexor

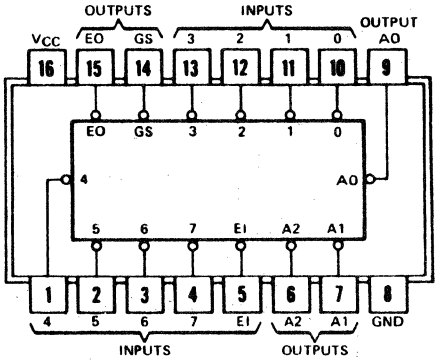
Description:

When G2A and G2B are both low, the inverted state of G1 is gated to one of the outputs Y0-7. The output selected is determined by the binary input of A, B, C.

SCHEMATIC:



PIN NUMBERING:



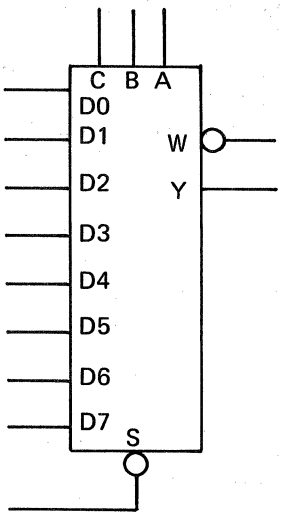
INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Figure 3-29. 74148 8 to 3 Line Priority Encoder

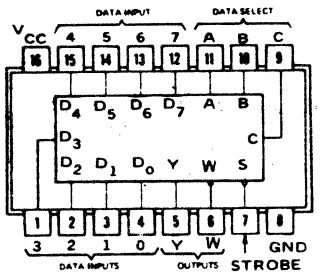
Description:

This IC encodes 8 line data input into 3-line Binary (Octal). E1 must be low in order to enable the IC. If two or more inputs are made low simultaneously, then the highest input has priority. EO is low when all inputs are high. GS goes low if any input 0-7 goes low.

SCHEMATIC:



PIN NUMBERING:



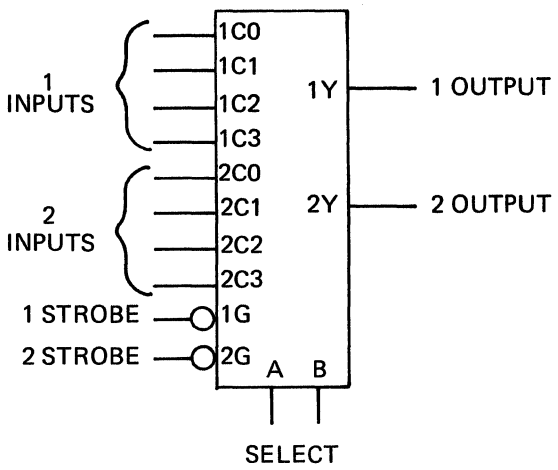
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Figure 3-30. 74151 Data Selector/Multiplexor

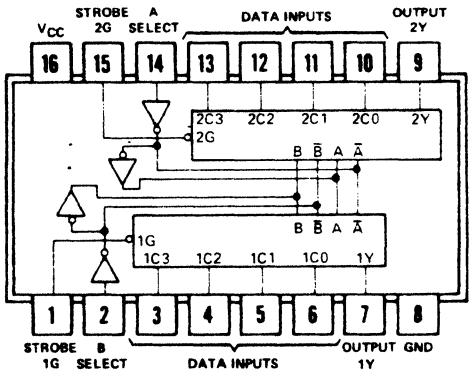
Description:

This IC selects one of eight inputs to be gated to Y. W is the inverse of Y. A, B and C determine which input is selected. S (Strobe) must be low to enable the IC.

SCHEMATIC:



PIN NUMBERING:



TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

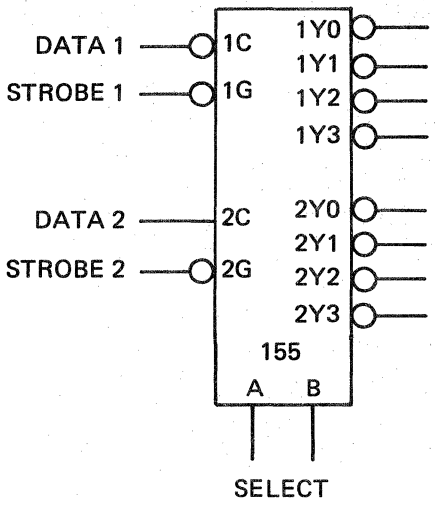
Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

Figure 3-31. 74S153 Dual 4-to-1 Data Selector/ Multiplexor

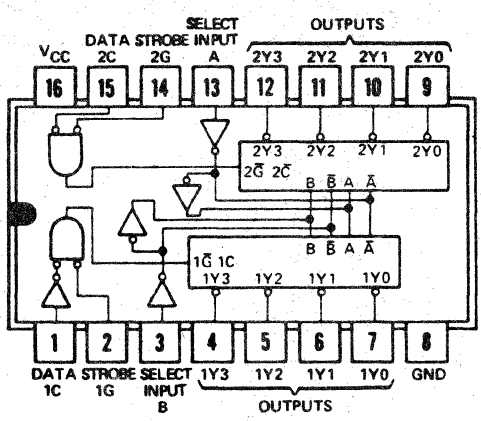
Description:

This IC contains two data selectors. Each selector is enabled by a low strobe input. When strobe is low, one input out of four is gated to the output. The input selected depends on the binary value of A and B. A and B are common to both selectors.

SCHEMATIC:



PIN NUMBERING:



3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

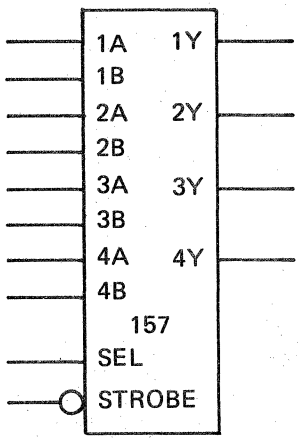
INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Figure 3-32. 74155 Dual 2-to-4 Line Decoder/ Demultiplexor

Description:

Each half is enabled when its strobe goes low. The DATA input is gated to one of four outputs depending on the binary value of A and B.

SCHEMATIC:



PIN NUMBERING:

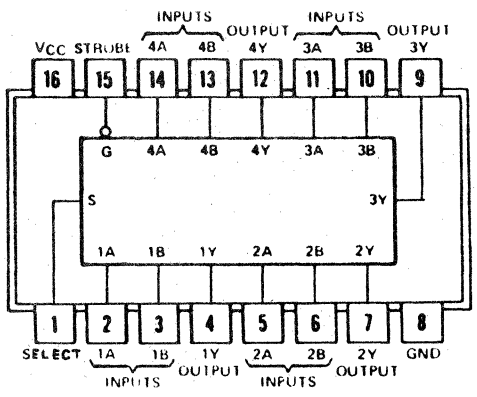


Figure 3-33 74157 Quad 2-1 Line Data Selector/ Multiplexor

FUNCTION TABLE

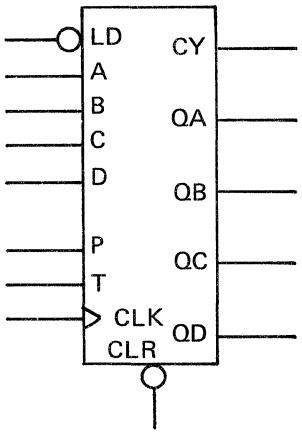
INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'S157	'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

Description:

The IC is enabled when Strobe is low. A 4-bit word is selected from one of two sources and is routed to four outputs. A low SELECT selects the A inputs, a high SELECT selects the B INPUTS.

SCHEMATIC:



PIN NUMBERING:

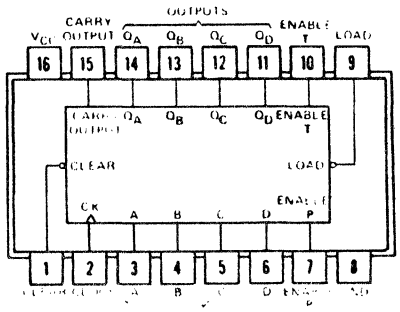


Figure 3-34. 74161 Synchronous 4-Bit Binary Counter

Description:

A low CLR clears the counter to zero regardless of CLOCK, LOAD, etc. The counter can be present to a value by inputtng the binary value on A, B, C and D and making LOAD (LD) low. Presetting occurs on the leading edge of the next clock pulse.

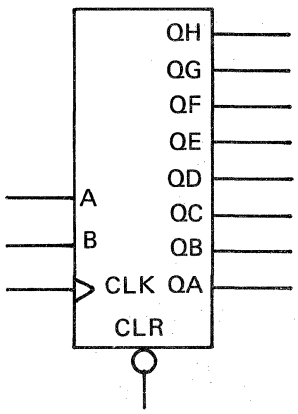
Counting is only permitted when both ENABLE inputs P and T are high. Counting occurs at the leading edge of each CLOCK pulse. CARRY output is high during a count of 15. This can be used to enable a cascaded counter. The counter restarts at 0 on the next clock after 15.

74163 74S163 Synchronous 4-Bit Counter

Description:

The 74163 is identical to the 74161 except that the CLEAR input is synchronous. When CLEAR is made low, the counter resets to zero on the leading edge of the next clock pulse.

SCHEMATIC:



PIN NUMBERING:

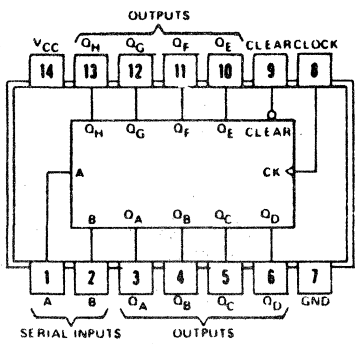
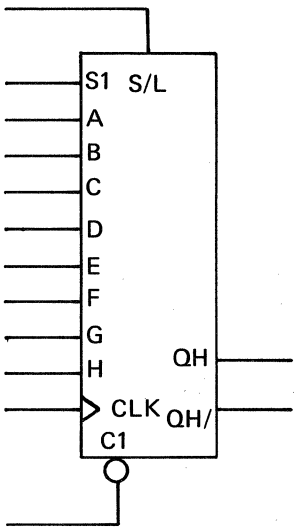


Figure 3-35. 74164 8-Bit Parallel-Out Shift Registers

Description:

A low CLEAR (CLR) resets all the outputs to low. A and B form an AND gate input. Shifting occurs at the positive edge of the clock pulse. Shifting is in the direction A to B, B to C etc. If both inputs are high QA is high after the clock pulse. If A or B (or both) are low QA is low after the clock. Each clock pulse shifts the data one position. The new data is fed into QA and the old data in QH is lost unless connected externally to another shift register (or some other storage device).

SCHEMATIC:



PIN NUMBERING:

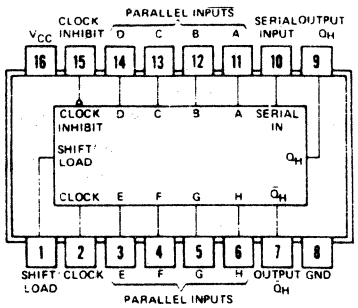
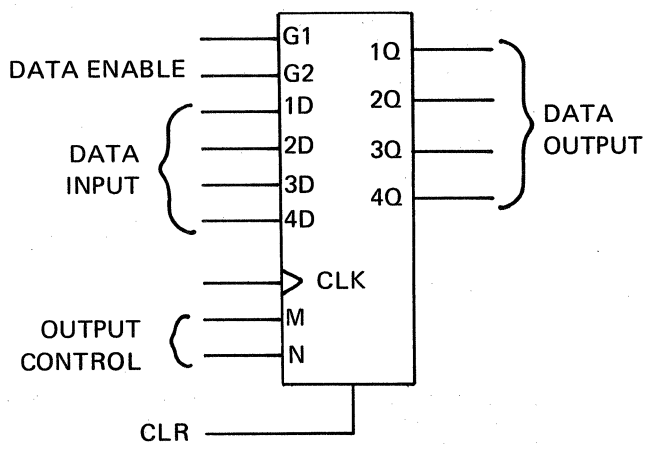


Figure 3-36. 74165 Parallel-Load 8-Bit Shift Register

Description:

The data on A through H is parallel loaded into the shift register on a high to low transition of the SHIFT/LOAD input (S/L). When S/L is high the IC is in shift mode. Provided that CLOCK INHIBIT (CI) is high, a shift occurs on the positive transition of the clock (CLK). Shifting occurs in the direction SERIAL IN SI to A, A to B etc. Complementary outputs of QH are provided.

SCHEMATIC:



PIN NUMBERING:

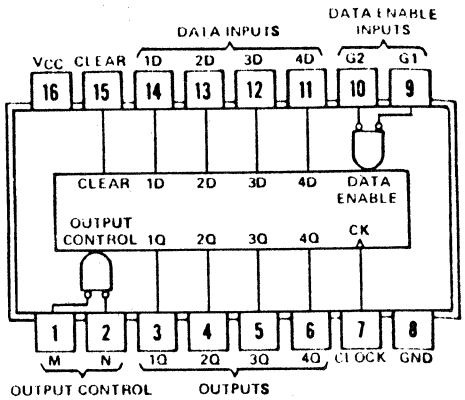


Figure 3-37 74173 4-Bit D-Type Register with 3-State Output

FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

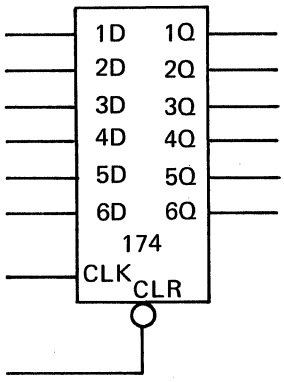
When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low to high-level transition
X = irrelevant (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established.

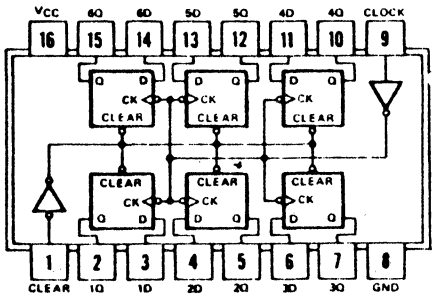
Description:

When either M or N (or both) are high, the outputs are disabled to the high impedence state, however, the action of the flipflops is not affected. A high CLR resets all the flipflops. When both DATA ENABLE inputs are low, data at the D inputs are loaded into their respective flipflops on the next positive transition of the CLOCK (CLK). If D is high, its flipflop sets. If D is low its flipflop resets.

SCHEMATIC:



PIN NUMBERING:



FUNCTION TABLE
(EACH FLIP FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$↑
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

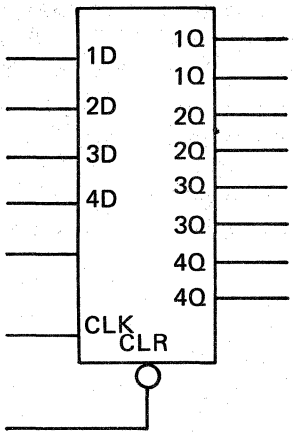
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state

Figure 3-38. 74174 Hex D-Type Flip-flops with Clear

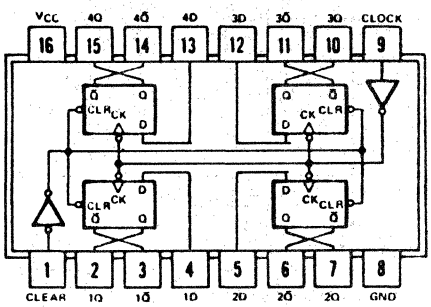
Description:

This IC contains 6 D type flipflops. A low CLEAR resets all the Q outputs to low. On the positive transition of the CLOCK each flipflop sets or resets depending on the state of its D input.

SCHEMATIC:



PIN NUMBERING:



(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q̄†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

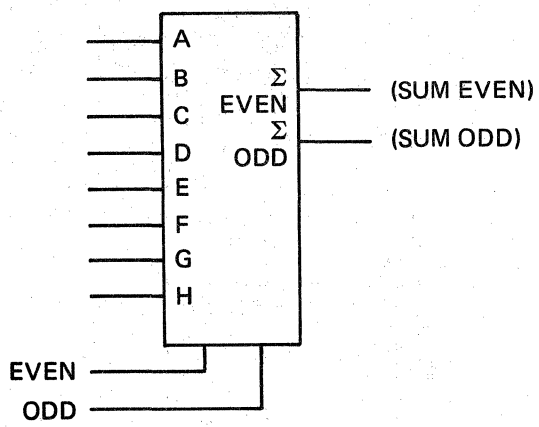
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established
† = '175, 'LS175, and 'S175 only

Figure 3-39. 74175 Quad D-Type Flip-flops with Clear

Description:

Each flipflop is reset by a low Clear. The data on the D input is transferred to the flipflop on the positive transition of the clock.

SCHEMATIC:



PIN NUMBERING:

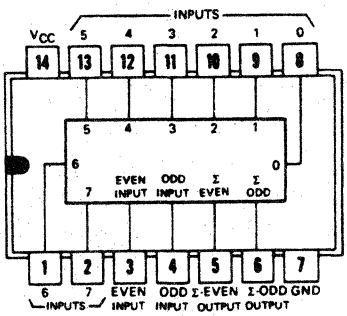
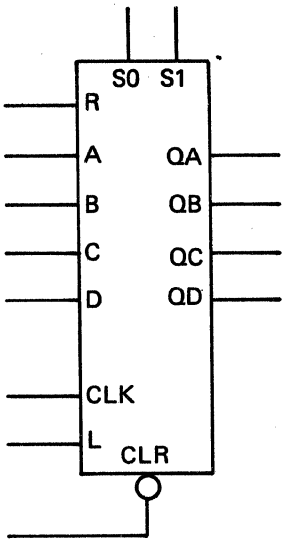


Figure 3-40. 74180 9-Bit Odd/Even Parity Generator/Checker

Description:

This IC is used to generate or check 8 bits for parity. More than 8 bits can be checked by cascading the ICs. Refer to the FUNCTION Table for an explanation of the IC operation.

SCHEMATIC:



PIN NUMBERING:

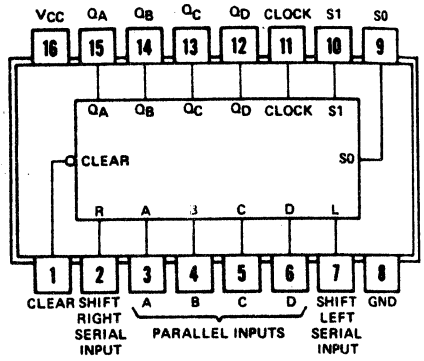


Figure 3-41. 4-Bit Bidirectional Universal Shift Registers

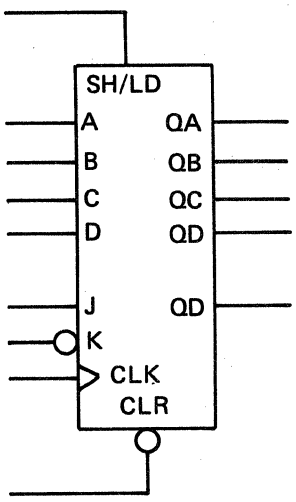
Description:

This IC has 4 modes of operation controlled by SO and S1.

1) Parallel load (SO and S1 high).
2) Shift right in the direction QA to QD (S0 high, S1 low).
3) Shift left in the direction QD to QA (S0 low, S1 high).
4) Inhibit clock (do nothing) (S0 low, S1 low).

Clocking occurs on the positive transition of the Clock pulse. A low CLEAR overrides all functions to reset the flipflops.

SCHEMATIC:



PIN NUMBERING:

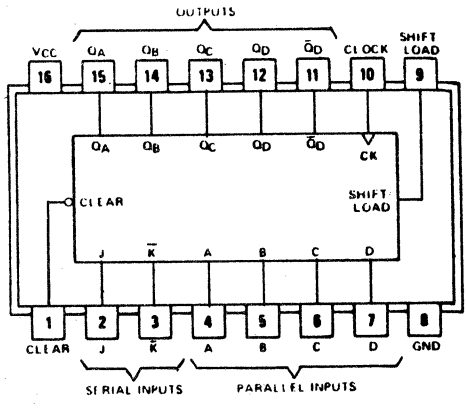


Figure 3-42. 74195 74S195 4-Bit Parallel-Access Shift Registers

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\bar{Q}_D$
			J	$\bar{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\bar{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\bar{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\bar{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock

Description:

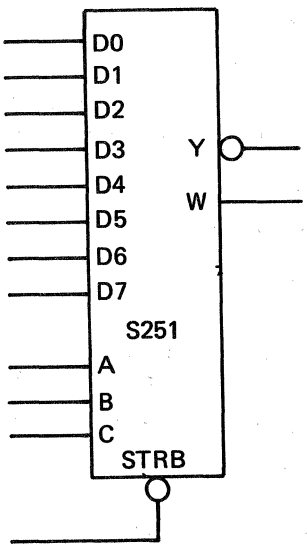
This shift register has two modes of operation depending on Shift/Load:

1) Parallel load (Shift/Load Low).
2) Shift in the direction QA to QD (Shift/LOad high).

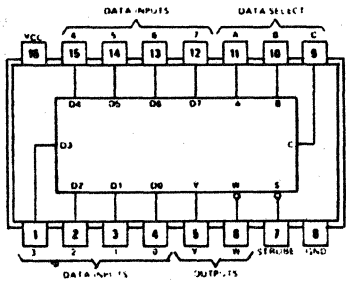
In parallel load mode, the data is loaded from the parallel inputs A through D.

In shift mode the input is taken from the JK/input, if J and K/ are both low QA resets at the positive clock transition. If J and K/ are both high, QA sets at the next positive clock transition. If J is high and K/ is low QA toggles (changes state) at the next positive clock transition. Loading and shifting occur at the positive edge of the clock. A low CLEAR, overrides all controls to reset the flipflops.

SCHEMATIC:



PIN NUMBERING:



INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

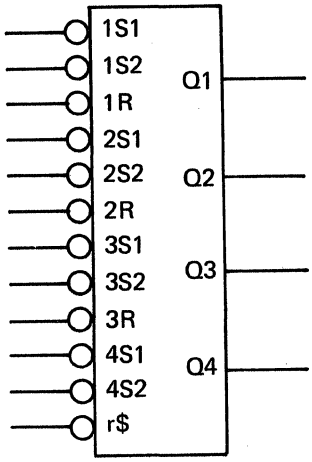
H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

Figure 3-43. 74S251 8-1 Data Selector/ Multiplexor with 3-State Output

Description:

One of eight data sources is selected depending on the binary weight of A, B and C. Y and W are complementary outputs. The 3-state output permits this IC to be connected to a common bus. When STROBE is high, all output transistors are disabled so that the IC neither drives nor loads the lines. When STROBE is low, the output is enabled.

SCHEMATIC:



PIN NUMBERING:

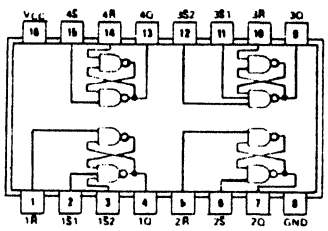
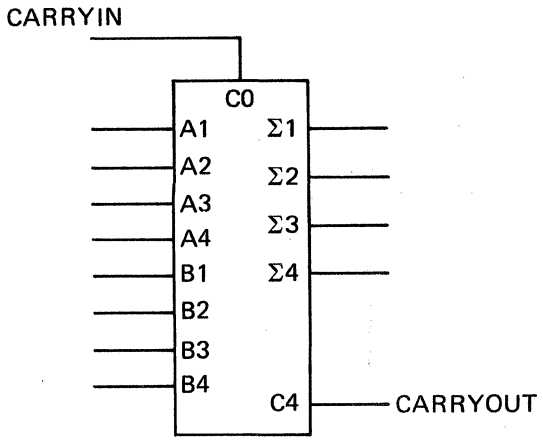


Figure 3-44. 74279 Quad R/S Latches

Description:

In the quiescent state, all inputs are high. A low on Reset input resets the latch. A low on either (or both) set inputs sets the latch. If the set and reset inputs are both low, the output is high, however, the state of the latch when the lows are removed may be either high or low.

SCHEMATIC:



PIN NUMBERING:

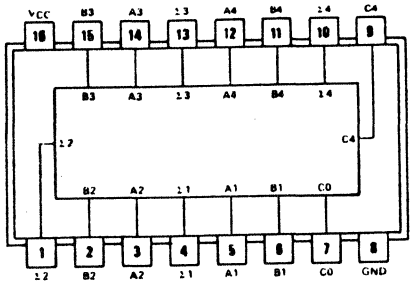


Figure 3-45 74283 4-Bit Binary Adder with Fast Carry

Description:

This IC adds together two 4-bit binary numbers and a possible carry in (C0). The output is sum 1, 2, 3, and 4, and a possible carry out produced by the

4 bit (C4). Example:

Bit position	4	3	2	1	
A Input	1	0	1	1	(11)
B Input	0	1	0	1	(5)
Carry Input				1	(1)
Sum	0	0	0	1	(1)
Carryoutput	1				(16)

By inputting the complement of a number, and a carry in, substraction is achieved.

Example: Subtract 5 from 11 (answer 6)
(Complement of 5)

Bit position	4	3	2	1	
A Input	1	0	1	1	(11)
B Input	1	0	1	0	(10)
Carry Input				1	
Sum	0	1	1	0	(6)
Carry Out	1				

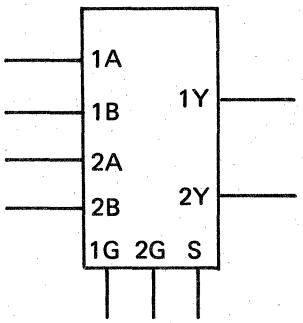
A carry out indicates that the sum is correct. If a carry out does not occur, this indicates that the sum is in complementary form plus one.
(Complement of 11)

Example: Subtract 11 from 5 (Answer –6)

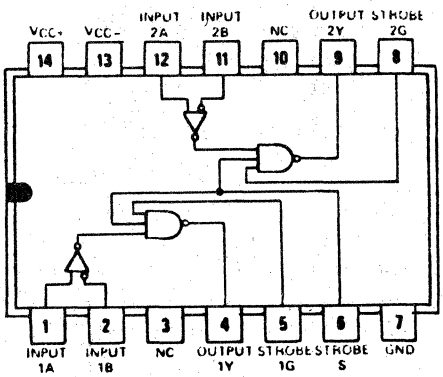
Bit position	4	3	2	1	
A Input	0	1	0	1	(5)
B Input	0	1	0	0	(4)
Carry in					(1)
Sum	1	0	1	0	(10)
Carry out	0				

The complement of 10 is 5, plus 1 equals 6. No carry out indicates a minus answer.

SCHEMATIC:



PIN NUMBERING:



DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

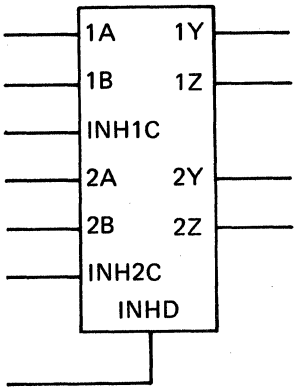
Figure 3-46. 75101 Dual Line Receivers

Description:

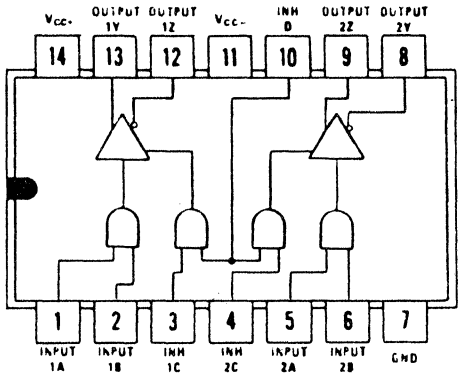
This receiver is used for differential input lines. The two receivers are enabled by a high STROBE, and a high gate input to each receiver. When the A input is 25 millivolts or greater more positive than the B input the output is high. If A is 25 millivolts or greater, more negative than B, the output is low.

The use of differential lines reduces common mode rejection. That is, a noise spike on both inputs at the same time, duration and magnitude may not be seen at the output. This is due to the fact that the difference between inputs is the critical factor.

SCHEMATIC:



PIN NUMBERING:



LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

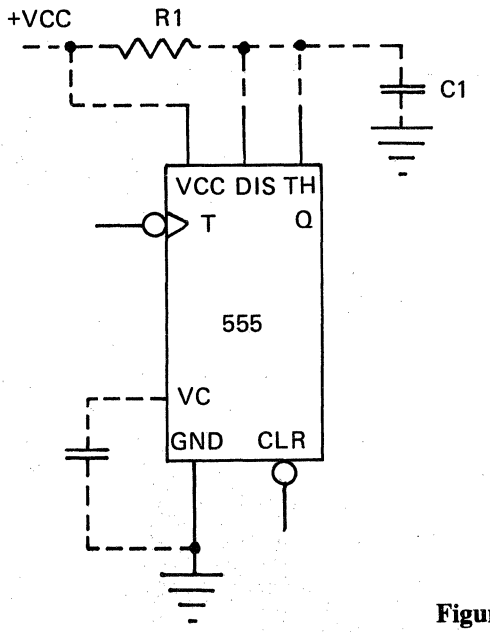
Low output represents the on state
High output represents the off state

Figure 3-47. 75110 Dual Line Driver

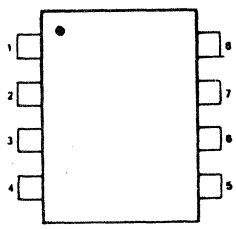
Description:

Both drivers are enabled by a high on INHIBIT D and a high on INHIBIT C for each driver. When the driver is enabled, the output Y is high if A and B inputs are both high. Y is low if one or both inputs A and B are low. Z complements Y. When the driver is inhibited the output goes high in a high impedance state, allowing the output lines to be used as a bus, by other components connected to the same line.

SCHEMATIC:



PIN NUMBERING:



V PACKAGE
(Top View)

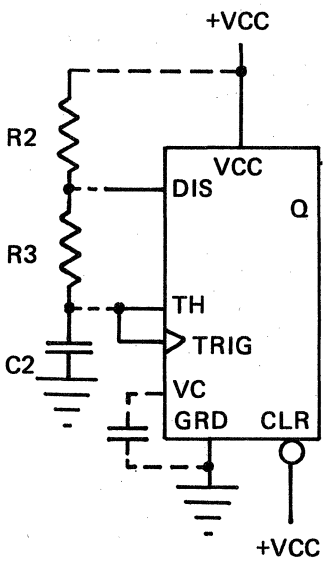
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

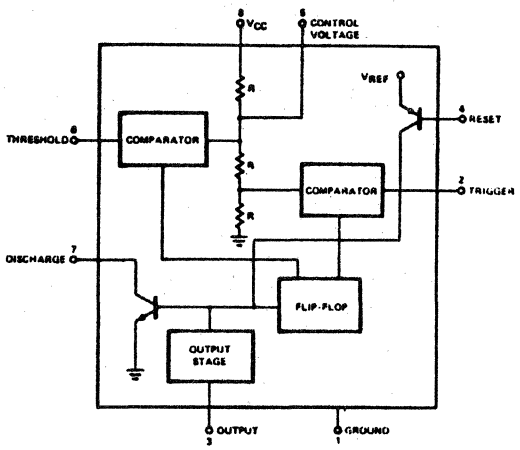
Description: (Timer)

When used as a timer, it triggers on a negative edge when the input voltage reaches 1/3 VCCF. The output goes positive for 1.1 x RC secs, regardless of any trigger pulses occurring during this time. CLR going low resets the output to low. If TRIG and CLR are tied together, the output goes low at the negative edge of the input signal and goes high for 1.1 x RC secs. starting at the positive edge.

Figure 3-48. 555 Timer

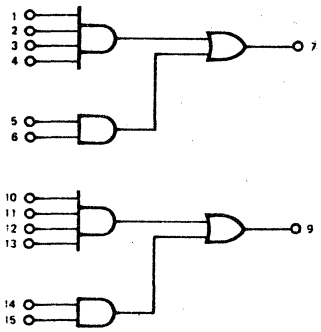
SCHEMATIC:





Description: (Oscillator)
In the oscillator configuration, the frequency is determined by R2, R3 and C2. The duty cycle is determined by the ratio of R2 to R3.

SCHEMATIC:



PIN NUMBERING:

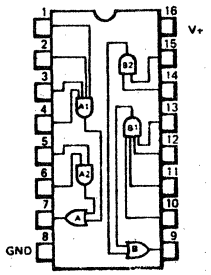
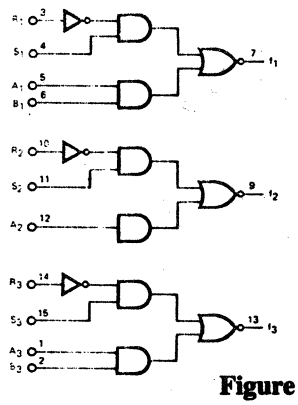


Figure 3-49. 8T23 Dual Single-Ended Line Driver

Description:
These drivers have open emitters, permitting wired OR functions with several drivers on one line. A resistor is required on the output to pull the line down to low level. Special circuitry prevents transients during power-up or Power-down.

SCHEMATIC:



PIN NUMBERING:

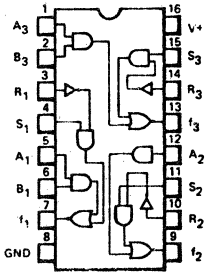
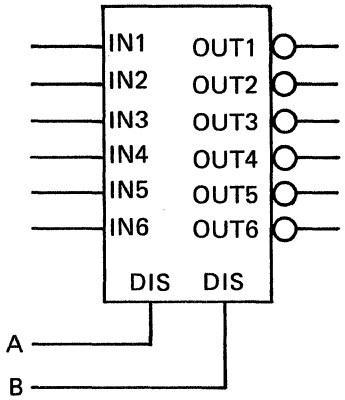


Figure 3-50. 8T24 Triple Line Receiver

Description:

The inputs are TTL and DTL compatable. An input of 1.7 or greater is intepreted as a logical one. Inputs of 0.7 volts or less are interpreted as a logical zero, as is an open circuit input.

SCHEMATIC:



PIN NUMBERING:

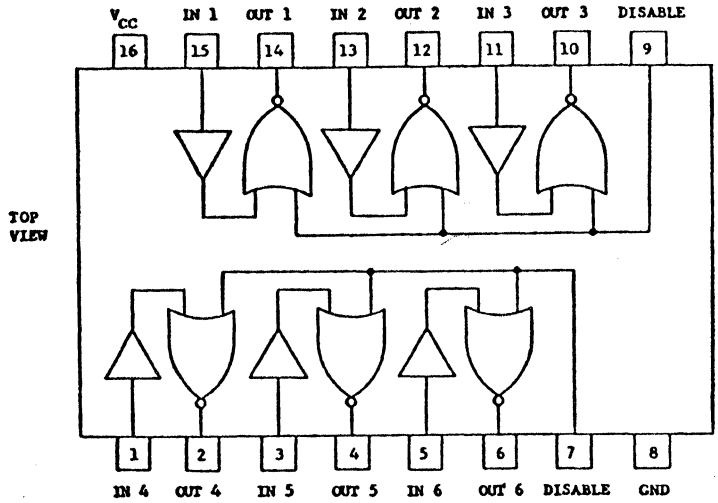


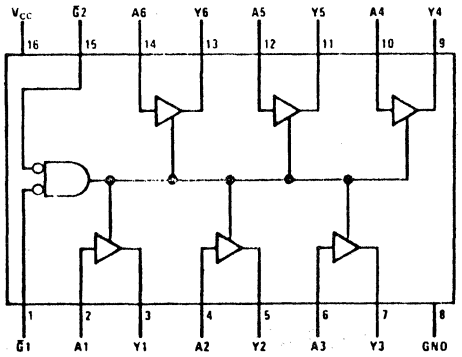
Figure 3-51. 8T37 DM8837 Hex Receiver with Hysteresis

Description:

A high on A causes outputs 1,2 and 3 to go low, regardless of the input. A low A enables outputs 1,2 and 3. The output is inverted.

The input voltage must go above approximately +2V for the output to go low. The input must then drop to approximately +1.3V before the output goes high.

PIN NUMBERING:

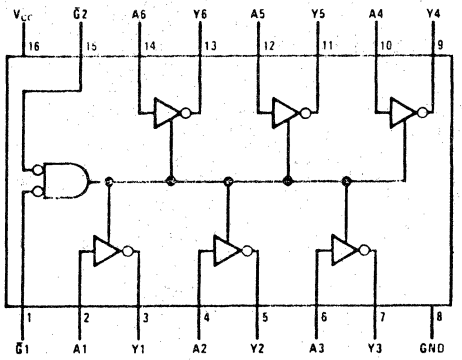


Description:

This IC features six non-inverting buffers. If G1 or G2 goes high, the output goes into high impedance state. This allows the IC to be used in bus applications. When G1 and G2 are low, A1=Y1, A2=Y2, etc.

Figure 3-52. DM8095 Tri-state Hex Buffers

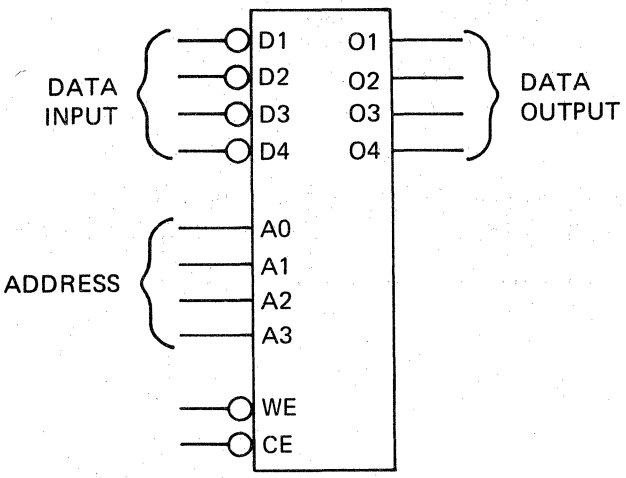
PIN NUMBERING:



Description:
This IC contains six inverters. When G1 or G2 is high, the outputs are high impedance. When G1 and G2 are both low, A1=Y1/, A2=Y2/, etc.

Figure 3-53. DM 8096 Tri-state Hex Inverter

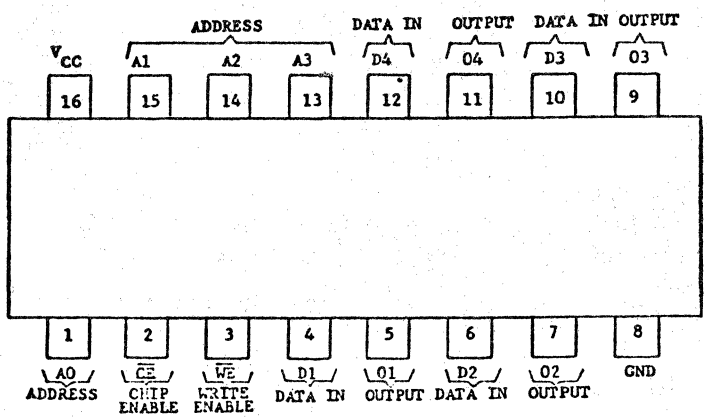
SCHEMATIC:



Description
In order to perform a read or a write operation, CHIP ENABLE (CE) must be low. If CE is high, the outputs are in high impedance state. This allows other ICs to operate on common output lines. A write is performed by making WRITE ENABLE (WE) low. When WE is low the data Input is written into the word addressed by the address Input (Binary 0 to 15). When WE is low, the outputs are high impedance.

A read is performed with CE low and WE high. The output lines contain the complement of the data previously written into the word addressed by the A inputs.

PIN NUMBERING:



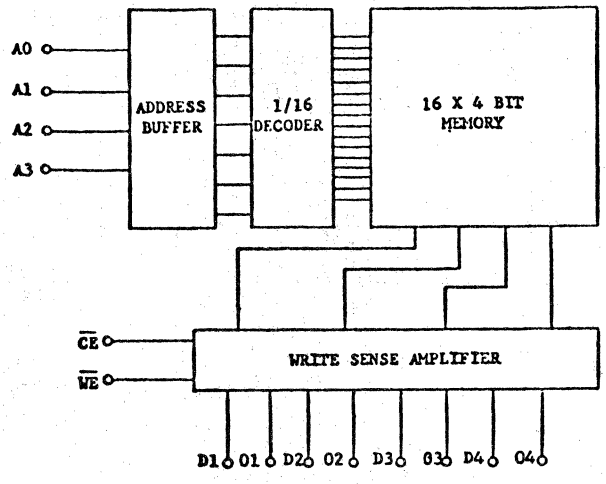
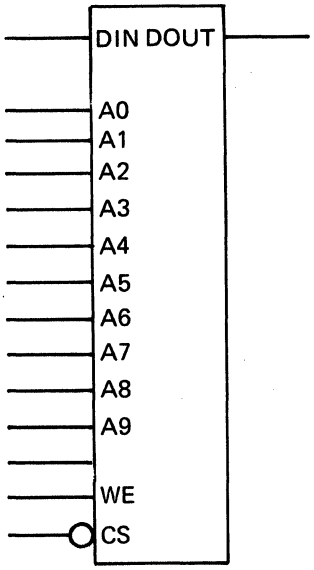


Figure 3-54 MM6561 Random Access Memory 16 x 4 Tri-state Output

SCHEMATIC:



PIN NUMBERING:

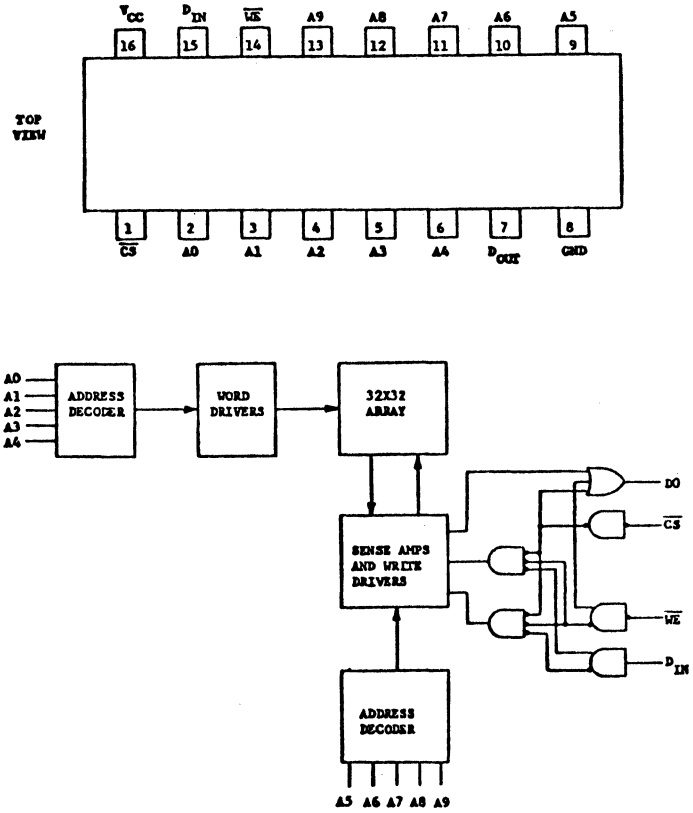


Figure 3-56. 93415 1024 x 1 Random Access Memory

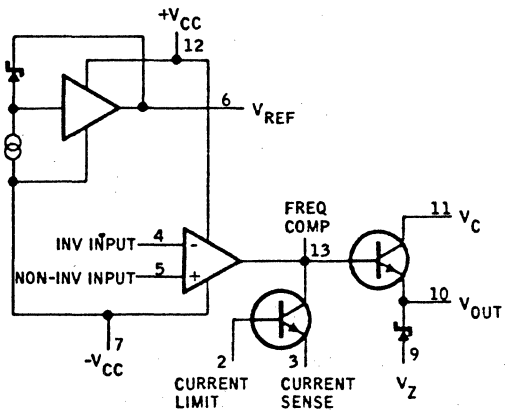
Description:

This IC can store 1024 bits of information, accessible one at a time. The CHIP SELECT (CS) input must be low in order to read or write. When CS is high, the output is open collector, it is actually floating. An external resistor is required to pull the level high.

When CS is low the IC is selected. When WRITE ENABLE is high, Reading takes place. DATAOUT (DOUT) contains the bit that was previously written in the cell addressed by the A inputs. When WE is low, the DATA input is written into the cell addressed by the A inputs.

Reading is not destructive.

SCHEMATIC:



PIN NUMBERING:

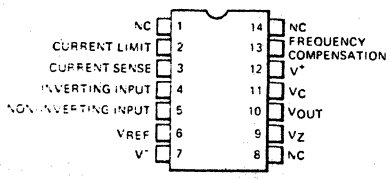


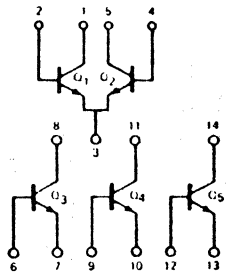
Figure 3-57. 723 Voltage Regulator

CHARACTERISTICS TABLE

SUPPLY VOLTAGE ($+V_{CC}$ TO $-V_{CC}$)	40 VOLTS, MAX
INPUT VOLTAGE RANGE	9.5 TO 40 VOLTS
OUTPUT VOLTAGE RANGE	2.0 TO 37 VOLTS
INPUT-OUTPUT VOLTAGE DIFFERENTIAL	3.0 TO 38 VOLTS
MAX OUTPUT CURRENT	150 MILLIAMPERES
REFERENCE VOLTAGE	6.95 TO 7.35 VOLTS
LINE/LOAD REGULATION	BETTER THAN 0.6 PERCENT

Description:
The 723 is a positive or negative voltage regulator. It is used in the DDEC as a control and power for other regulators. Shutdown is accomplished by grounding the frequency compensation pin. Regulation is accomplished by changing Vout when the sensed output is different from a reference voltage. Current limiting is accomplished by shutting off the regulator when the voltage on Pin 2 (current limit) is more positive than the voltage on Pin 3 (current sense).

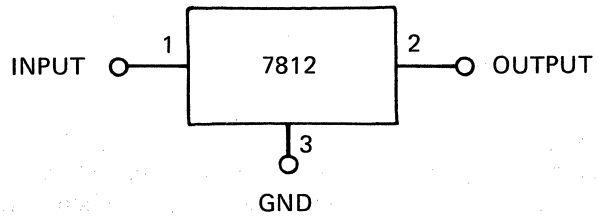
Schematic with pin numbering:



Description:
The 3086 is a package of 5 silicon NPN transistors. Two of the transistors (Q1 and Q2) are internally connected to form a differential pair. Three transistors are independent.

Figure 3-57. 3086 Transistor Array

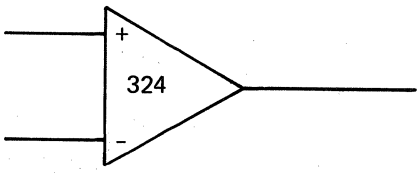
SCHEMATIC:



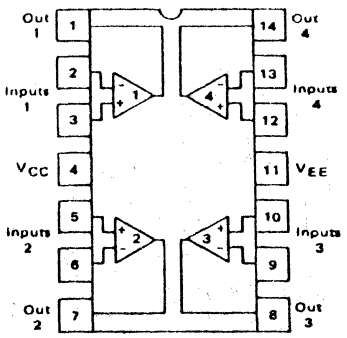
Description:
The 7812 is a three terminal regulator with a fixed regulated output of 12 volts. It has internal thermal protection and current limiting.

Figure 3-58. 7812 Voltage Regulator

SCHEMATIC:



PIN NUMBERING:



Description
The 324 is a package of four independent general purpose operational amplifiers.

Figure 3-59. 324 Operational Amplifier

SECTION 4
MAINTENANCE TECHNIQUES

LOCAL OPERATION

GENERAL DESCRIPTION

Special maintenance circuits enable all DDEC functions except the processor interface to be run when the DDEC is offline. Push buttons and switches on the maintenance panel, allow the F.E. to enter any initiate words in maintenance memory, then have the DDEC do the designated operation. Table 4-1 gives the uses for each word of maintenance memory and gives the meaning of all DDEC operation codes. With the correct combination of switches it is possible to do variations of the basic operations such as:

1) Loop on one head.
2) Loop on one sector.
3) Loop on operation.
4) Ignore all errors.
5) Ignore read data errors (firecode errors).
6) Alternate two operations.

The address display on the opposite side of the DDEC from the maintenance panel indicates the sector, head, and cylinder on which the DDEC is attempting an operation. The F.E. can use this information and the hexadecimal address scheme for the disk being used to help him do local operations from the maintenance panel. The disk address scheme is generated from the Disk Pack Diagnostic program.

At the end of a DDEC operation the result descriptor is displayed on the maintenance panel vertical display. Table 4-4 gives the meanings for the abbreviations printed on the left side of the display. Volume 3, Theory of Operation, Section 1 gives the meanings for each bit of the result descriptor.

Switch Functions

Volume 3, Section 5 also gives an expanation of the maintenance panel switch functions.

NOTE

After pressing the on switch on the operator control panel, there is a 25 second delay before the DDEC is ready to be used. Until that time, the maintenance panel switches are disabled. Use figure 4-1 to find the switches on the maintenance panel which are listed below.

Table 4-1. Maintenance Memory Word Usage

0	Initiate Word 1 First OP
1	Initiate Word 2 First OP
2	Data Word First OP
3	ERD Word 1 or 16 Bits Firecode on an Alternate OP
4	ERD Word 2 or 16 Bits Firecode on an Alternate OP
5	ERD Word 3
6	ERD Word 4
7	Not Used
8	Initiate Word 1 Second OP
9	Initiate Word 2 Second OP
10	Data Word Second OP
11	16 Bits Firecode on an Alternate OP
12	16 Bits Firecode on an Alternate OP
13	Not Used
14	Not Used
15	Not Used

Table 4-2. Initiate Words

INFORMATION LINES	INITIATE WORD 1	INITIATE WORD 2
INFO 00 LSB	OP1	B2*5
INFO 01	OP2	B2*6
INFO 02	OP3	B2*7
INFO 03	N0	B2*8
INFO 04	U1	B2*9
INFO 05	U2	B2*10
INFO 06	U3	B2*11
INFO 07	U4	B2*12
INFO 08	N1	B2*13
INFO 09	N2	B2*14
INFO 10	N3	B2*15
INFO 11	B2*0	B2*16
INFO 12	B2*1	B2*17
INFO 13	B2*2	B2*18
INFO 14	B2*3	B2*19
INFO 15 MSB	B2*4	B2*20

OP1, OP2, OP3 – Opcode field
U1, U2, U3, U4 – Unit address field
N0, N1, N2, N3 – Opcode variant bits
B2*0 – B2*20 – Sector address field

DATA INPUT

At the right side of the maintenance panel 16 Momentary switches are mounted vertically. They are used to set the bits of the initiate words and data which is to be executed at start time. An associated light-emitting diode (LED) lights when one of these buttons is pressed.

Table 4-3. OPCODE Decode

OPCODE DECODE	OPCODE FIELD OP1	OP2	OP3	VARIANT BITS N0	N1	N2	N3
Read 206	0	0	0	PLO	OF	E/L	I
Read 207	0	0	0	PLO	CR	E/L	–
Read Maintenance	0	0	1	–	–	0	–
Read Extended Status	0	0	1	–	–	1	–
Write 206	0	1	0	–	–	–	–
Write 207	0	1	0	–	–	F	–
Initialise	0	1	1	–	–	S	P
Relocate #1 (Data Specified)	1	0	0	–	N	N	N
Relocate #2 (Data=Address Field)	1	0	1	–	N	N	N
Verify	1	1	0	–	N	N	N
Testop	1	1	1	–	–	C	W

NNN = (1-5) Spare Sector Number in Binary
C = 1 Clear Seek Status Condition
P = 1 Full Pack
P = 0 Track Only
W = 0 Normal Test Op.
W = 1 Remote Power Down
PLO = 1 Enable Early / Late Strobe
E/L = 1 Late Strobe
E/L = 0 Early Strobe
S = 1 Data Specified
S = 0 Data = Address Field
OF = 1 Offset
I = 1 Offset In
I = 0 Offset Out
F = 1 Diagnostic Write Fire Code
CR = 1 Error Correction Read

LOAD

A momentary switch to load the sixteen bit word from the vertical LED display at. The word is loaded into the maintenance memory location at the top of the panel. Pressing this switch loads one memory word and also advances the memory address counter to the next word.

CLEAR

A momentary switch to clear the two LED displays. This resets the memory address counter to word zero, as well as clearing the sixteen bit display. If the toggle switch DISP ENBL is up, pressing clear only clears the sixteen bit display.

START

A momentary switch which causes the DDEC to do the operation specified by the initiate words contined in maintenance memory.

STEP MEMORY

If the switch DISP ENBL is up, this momentary switch advances the memory address counter each time it is pressed. The sixteen bit word contained in each memory location is displayed in the vertical LED display after stopping

MSTR CLR

A momentary push button which sends a clearing signal throughout the DDEC to many flags, flipflops and the extended status register. It forces the DDEC to the idle state. This does not clear maintenance memory of any previously loaded information.

STOP

A momentary switch which stops the DDEC in an orderly way. When the STOP button is pressed, the DDEC may halt and display the A.E. bit. This does not mean that an address error has occurred. The DDEC simply terminated during an address search.

Table 4-4. R.D. and E.R.D. Decodes

L.E.D.	RESULT DESCRIPTOR	0000 ERD WORD 1	0000 ERD WORD 2	0000 ERD WORD 3	0000 ERD WORD 4	INFO LINE
FCO	FIRE CODE ERROR	SECTOR 64	N3	ILLEGAL CYLINDER	ADDRESS OVERFLOW	00
WLO	WRITE LOCKOUT OR E.C.	HEAD 1	N2	ILLEGAL HEAD *	BAD DM RESPONSE	01
SSO	SEEK STATUS	HEAD 2	N1	SEEK AND NOT READY	RPM LOW	02
NRO	NOT READY	HEAD 4	N0	WRITE PROTECT AND WREN	TEMP. CRITICAL	03
OLO	OFF LINE	LOW	UNIT 1	WRITE DATA MISSING	TEMP. WARNING	04
USO	DRIVE UNSAFE	CYL 1024	UNIT 2	MAINTENANCE MODE	D.C. UNSAFE	05
DSO	DATA SYNC ERROR	CYL 1	UNIT 4	SEQUENTIAL FORMAT	HEAD SELECT FAULT	06
AEO	ADDRESS ERROR	CYL 2	OP 3		SEE NOTE 2	07
STO	SEEK INCOMPLETE	CYL 4	OP 2	207	SEE NOTE 3	08
NPO	DRIVE NOT PRESENT	CYL 8	OP 1	206		09
O		CYL 16	SECTOR 1	CM ERROR	CARRIAGE HITS STOP	10
O		CYL 32	SECTOR 2	INDEX MISSING	OFF TRACK AND WRITE	11
O		CYL 64	SECTOR 4	NO READ DATA	SEEK INCOMPLETE	12
O		CYL 128	SECTOR 8	ADDRESS MARK MISSING	OFFSET AND SEEK *	13
TPO	TRANSMISSION PARITY	CYL 256	SECTOR 16	DRIVE CLOCK ERROR	OFFSET AND WREN *	14
TDO	TRY DIAGNOSTICS	CYL 512	SECTOR 32	DDEC FAN FAILURE	SPINDLE ADDRESS ERROR	15

* 206 ONLY

NOTE 1: IF CM ERROR IS ON, DRIVE STATUS IS REPLACED BY THE CM RECEIVED IN ERROR.

NOTE 2: NO MFM TRANSITIONS (206 AND 207) OR, DRIVE CLOCK ERROR (207).

NOTE 3: WRITE CURRENT AND NO WRITE GATE OR WRITE GATE AND NO WRITE CURRENT.

DISP ENBL

UP. This allows the step MEM pushbutton to advance the memory address counter and to display the current memory word in the vertical LEDs.

HALT ON ERR

UP. The DDEC stops for any error detected. When stopped, the result descriptor is displayed in the vertical LEDs and the sector in error is displayed in the address display. Table 4-4 gives the meaning of the result descriptor bits. For firecode errors the address displayed is one sector beyond the sector in error.

CENTER. The Off-Position allows firecode (read) errors without stopping but these are reported in the result descriptor when the DDEC

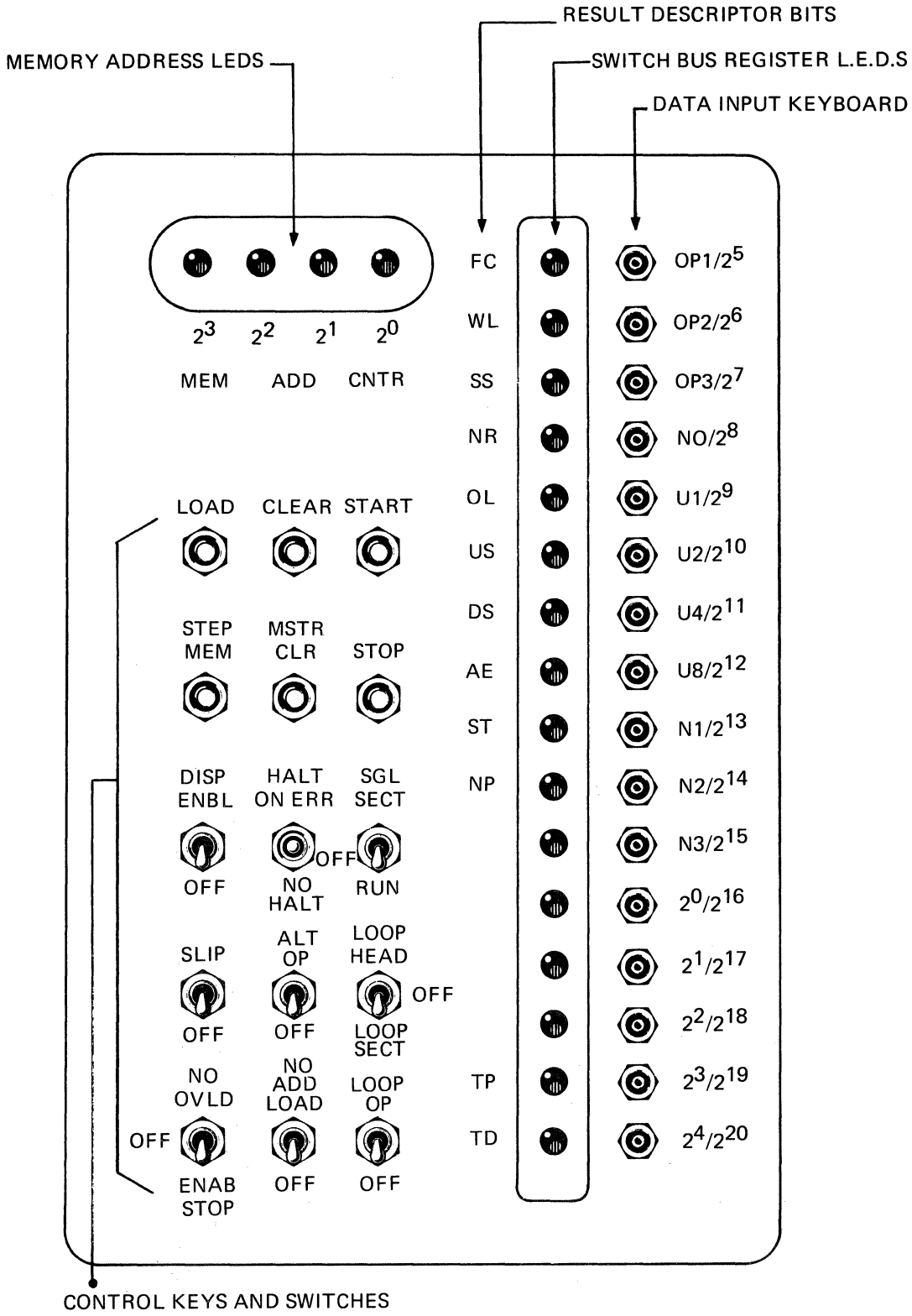


Figure 4-1. Maintenance Panel

stops for another reason.

DOWN. The NO HALT position forces the DDEC to continue to do sequential address searches, ignoring address errors. If a sector address is found and the data read, firecode errors and data sync errors are ignored.

SGL SECT/RUN

UP. This makes all operations except initialize one sector operations. The address in the initiate words is the sector used. Some operations are by default single sector operations.

DOWN. This allows normal incremental operations

SLIP

UP. This is local mode equivalent of losing EXECUTE from the processor. It stops data transfer until the switch is put down.

DOWN. This is the normal operating position.

ALT OP

UP. Two areas of maintenance memory are used as sources of initiate words and data alternately. These are memory address counter locations 0,1 and 2 for one set of instructions and locations 8, 9, and 10 for the other set of instructions. Each time the DDEC starts it uses the initiate words not used the last time.

DOWN. In this position, only the operation defined by the initiate and data words at memory locations 0,1 and 2 is performed.

LOOP HEAD/LOOP SECT

UP. If no single sector conditions override, the operation is done on a single track continuously.

CENTER. All operations are done normally.

DOWN. In all operations except initialize, only the sector address in the initiate words is used. The operation is done continuously on that sector.

NO OVLP/ENAB STOP

UP. If a seek is required in order to find the first sector after starting, the DDEC sends a seek command, waits for the drive to complete the seek, then does the operation required. This is an immediate seek.

CENTER. If a seek is required to find the first sector after starting the DDEC sends a seek command, then stops and displays the result descriptor which is NOT READY since the drive is seeking. The DDEC must be started again to continue the operation.

DOWN, ENABSTOP enables the clockstopper feature described in section 4. This switch down also makes the memory address counter at the top of the panel indicate the mode in which the DDEC is operating.

NO ADDLOAD

UP. The starting address for an operation is the address contained in the DDEC address decoder instead of the address contained in the initiate words in maintenance memory.

DOWN. This is the normal position. The starting address of an operation is that contained in the initiate words in maintenance memory.

LOOP OP

UP. If an operation is stopped for any reason, it starts again as though the Start Button had been pressed. A TRY DIAGNOSTIC bit in the result descriptor prevents normal looping of the operation. Section 4 gives an explanation of the Enable Clear Diagnostics feature for this problem. With HALT ON ERR switch up, LOOP OP switch has no effect when an error of any kind occurs.

DOWN. This is the normal position. The end of an operation stops the DDEC

Entering an Address in the Initiate Words

Part of initiate word 1 and all of initiate word 2 are the hexadecimal sector address where the DDEC must perform its operation. In local operation this address must be loaded into maintenance memory as initiate words 1 and 2. The least-signigicant bit is labelled 2^0 on the maintenance panel. Initiate word 1 must contain 2^0 through 2^4 of the address as marked on the panel. Initiate word w must contain 2^5 through 2^{20} of the address as marked in the right column on the panel. These steps must be followed when loading an address:

1) Change addresses to hexadecimal. Table 4-5 is a conversion guide.
2) Press the switches for the five least-significant bits of the address at the same time as the OP code and variants. Combined, they must be loaded as initiate word 1 into memory address 0.
3) When the memory address counter is at address 1, press the switches for the remaining 16 bits of the sector address. This is initiate word 2. Load initiate word 2 into memory address 1.

Initialize Operation

Use caution. Customer data and system software is destroyed by initializing. The F.E. must install a scratch pack or use only the maintenance cylinder for all initialize operations.

Full Pack Initialize With Data.

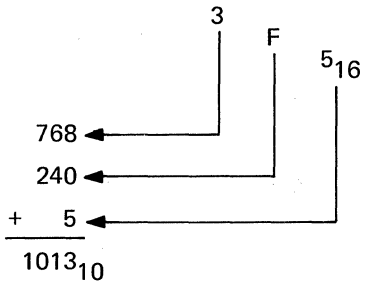
1) Set the maintenance panel switches to the normal positions as in table 4-6.
2) Push MSTR CLR and CLEAR. This clears both displays on the maintenance panel. This is address 0 of maintenance memory.
3) Press OP2 and OP3 for the initialize OP code and N2 and N3 to select variants for specifying the data to be written and to specify a full pack initialize.

If the unit number of the disk drive to be initialized is not 0 press U1, U2, U4, or U8 to address the drive correctly in binary.

Table 4-5. Decimal-to-Hexadecimal Conversion

6		5		4		3		2		1	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	5	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15

HEXADECIMAL TO DECIMAL



DECIMAL TO HEXADECIMAL

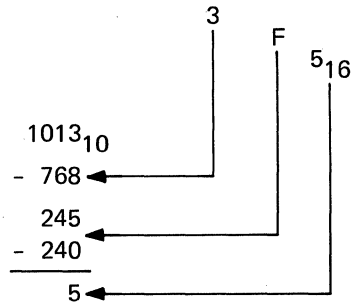


Table 4-6. Normal Position of Maintenance Panel Toggle Switches

Switch Designation	Normal Position
DISP ENBL	Down
HALT ON ERR	Center (off)
SGL SECT	Down (run)
SLIP	Down (off)
ALT OP	Down (off)
LOOP HEAD	Center (off)
NO OVLP	Up
NO ADD LOAD	Down (off)
LOOP OP	Down (off)

4) This completes initiate word 1 so press LOAD once.
5) The memory address counter should have stepped to address one. Press LOAD again. This makes initiate word 2 all zeros.
6) Address 2 of maintenance memory must contain the data to be written repeatedly in the data field of all sectors. Select any data pattern by pressing the switches.
7) Press LOAD to load the data pattern in Memory Address 2.
8) Press START to begin the full pack initialize operation.

A normal end for full pack initialize is with sector 0, head 0, last cylinder +1 in the address decoder display.

Full Pack Initialize with Header

This is done the same as a full pack initialize with data except that the N2 bit in initiate word 1 is not set. This operation repeats the header (sector address) in the data field. The result is a more complex data field and more of an exercise for the drive.

Single Track Initialize

Enter the initiate words for single track initialize the same as for the full pack initialize with these exceptions.

1) Do not press N3 in initiate word 1.
2) Enter a hexadecimal address in initiate words 1 and 2. See the instructions given before in this section to enter an address in the initiate words. For single track initialize the address must be the address for sector 0 of the track to be initialized.

Read Operation

1) Set the maintenance panel switches to the normal positions as in table 4-6.
2) Press MSTR CLR and CLR. This clears both displays.
3) Press the correct unit switches (binary) for the drive being used. The read OP code is 0 so no other buttons need to be pressed in initiate word 0.
4) Press LOAD to load initiate word 1 into maintenance memory. Press LOAD again to load all zeros into initiate word 2. Memory address 3 is not used for a read OP.
5) Press START to read the disk from sector 0 to the last sector on disk.

To begin reading at a particular sector, load the hexadecimal address of that sector into initiate words 1 and 2. This is described early in this section under the heading *Entering an Address in the Initiate Words*.

Table 4-3 gives the meanings for the variants of the read operation.

Write Operation

Use caution. Customer data and system software are destroyed by the write operation. The F.E. must install a scratch pack or use only the maintenance cylinder for all write operations.

1) Set the maintenance panel switches to the normal positions as in table 4-6.
2) Press MSTR CLR and CLEAR. This clears both displays.
3) Press OP2 for the write OP code. Press the correct unit numbrs in binary for the drive to be used. Initiate word 1 is complete.
4) Press LOAD. This loads initiate word 1 into maintenance memory and steps memory to address 1. Press LOAD again to load initiate word 2 (all zeros) and to step memory to address 2.
5) Address 2 in maintenance memory must contain 16 bits of data. This word is written repeatedly in the data fields. Press switches to select the data pattern wanted. The first bit of data written is taken from the bottom of the maintenance panel display.
6) Press LOAD to load the data word into maintenance memory.
7) Press START to write from sector 0 to the last sector on disk.

See under the heading *Entering an Address in the Initiate Words* to begin writing at a particular sector.

Table 4-3 gives the meanings of the variants which are used for a write OP.

Read Maintenance Operation

Read maintenance is single sector read. It does not need the normal address comparison to locate the required sector for reading. Instead, the DDEC does a *dead reckoning* search from the index mark of the disk by counting clocks. At the correct time the DDEC sends a read data command to the disk. The data sent to the DDEC from disk is first address field, then data field and firecode. This is useful to the F.E. when a sector address cannot be found. By choosing a good trigger point he can see the address field in that location.

1) Set the maintenance panel switches to the normal positions as in table 4-6.
2) Press MSTR CLR and CLEAR. This clears both displays.
3) Press OP3 for the read maintenance OP code. Press the correct unit numbers in binary for the drive to be used.
4) The sector address in hexadecimal must be specified for this operation.

The method is described under the heading *Enter an Address in the Initiate Words* in this section.

5) Press LOAD to load the completed initiate word 1 into maintenance memory and to step memory to address 1.
6) Press the correct switches to give the rest of the hexadecimal sector address in initiate word 2.
7) Press LOAD to load initiate word 2 into memory. Address 3 is not used for read maintenance OP.
8) Press START to do a read maintenance of the sector.

It is normal to stop with A.E. as the result descriptor after a read maintenance operation.

Relocate Operation

Use caution. Customer data and system software are destroyed by the relocate operation. The F.E. should install a scratch pack or use the maintenance cylinder for relocate operations.

1) Set the maintenance panel switches to the normal positions as in table 4-6.
2) Press MSTR CLR and CLR. This clears both displays.
3) Press OP1, the Op code for relocate with data. Press the correct unit number in binary for the drive being used.

4) The variants N1, N2 and N3 specify the spare sector in binary to use for relocation. Press N1 to specify the first spare.
5) The hexadecimal address of the sector to relocate must be entered in initiate words 1 and 2. The method is described under the heading *Entering an address in the Initiate Words* in this section.
6) Press LOAD to load the complete initiate word 1.
7) Press the switches to complete the sector address.
8) Press LOAD to load initiate word 2 into memory.
9) Press the switches to specify a data pattern to be written in the relocated sector.
10) Press LOAD to load the data pattern into address 2.
11) Press START to do the relocate operation.

Spare Sector Verify Operation

Use this operation to find if a spare sector is available or if it is used.

Spare sector verify is entered like relocate with these differences:

1) The Op code is OP1 and OP2.
2) The address given in initiate words 1 and 2 must be the address of a sector on the spares head of the cylinder being verified.

At the end of the operation the result is all zeros for an available spare and A.E. for a used spare.

Alternate Operations

Use caution. Customer data and system software are destroyed by initialize, write, or relocate operations. Install a scratch pack or use the maintenance cylinder for those operations.

The DDEC fetches initiate and data words from two areas of maintenance memory. Two different operations can be done alternately on the same drive unit or alternately on two different drive units. Two uses are:

1) Alternate seeks for checking the servo.
2) Alternate write/read to check data.

Here is an example of an alternate operation.

1) Set the maintenance panel switches to the normal positions as in table 4-6.

Make these changes:

SGL SECT - UP
ALT OP - UP
LOOP OP - UP

2) Press MSTR CLR and CLEAR. This clears both displays.
3) Press the correct unit numbers in binary for the drive to be used. Do not press the Op code switches or address switches. The first operation is a read on sector 0.
4) Press LOAD to load initiate word one into memory.
5) Press LOAD to load initiate word 2 (all zeros) into address 1. Press load 7 times. The memory address counter must indicate binary 8. This is the memory location to contain the second set of initiate words.
6) Press N2 for a write operation. Press the same unit numbers as in step 3.
7) Choose an address for the write opeation. The method for loading this address is described under the heading *Entering an Address in the Initiate Words* in this section. Press the correct address switches to complete initiate word 1.
8) Press LOAD to load initiate word 1 of the alternate operation.
9) The memory address counter is binary 9. Press the switches to complete the address started in initiate Word 1.
10) Press LOAD to load initiate word 2 of the alternate operation.
11) Press the switches to select a data pattern to write in the alternate operation.
12) Press LOAD to load the data word into memory address 10.
13) Press START to do the alternate operation automatically.

Each operation is one sector long because SGL SECT is up. The operation restarts automatically because LOOP OP is up. The operation switches alternately because ALT OP is up.

Read Extended Status Operation

If T.D. (try diagnostics) is set in the result descriptor it means:

1) An exception occurred in either the DDEC or the drive.
2) An extended result descriptor is locked in the DDEC The E.R.D. can be extracted for analysis by performing a read extended status operation.
3) Pressing MSTR CLR unlocks the DDEC but loses the E.R.D. information.

Volume 3, Section 1 gives a further explanation of the T.D. bit in the result descriptor, as well as the E.R.D. To do a read extended status operation follow these steps:

1) Set the maintenance panel switches to the normal positions as in table 4-6.
2) Press CLEAR only. This clears both displays.
3) Press OP3 and variant N2. This is the read extended status Op code.
4) Press LOAD to load initiate word 0 into memory.
5) Press START to do the read extended status operation. The normal end to the operation is a result descriptor with no error bits. The memory address counter must display binary 7.

6) Press CLEAR, this resets the memory address counter to address 0.
7) Move DISP ENBL switch to the up position.
8) Press STEP MEM to advance the memory address counter. Table 4-7 gives the meaning for each bit of the E.R.D. which is displayed in the vertical L.E.D.s. Memory address location 3, 4, 5, and 6 contain E.R.D. words 1, 2, 3, and 4.

General Troubleshooting

Drive/DDEC Fault Isolation

Use the maintenance features of the DDEC to isolate DDEC problems from drive problems. These tests can quickly isolate a problem.

1) Use different drives with the same DDEC interface.

If	Then
The problem is always there.	DDEC or cable is at fault
The problem changes.	DDEC is probably at fault.
The problem goes away.	Drive is probably at fault.

2) Use the same drive but different DDEC interface.

If	Then
The problem is always there.	Use test 1.
The problem changes.	No determination can be made.
The problem goes away.	DDEC or cable is at fault.

3) For a read or write problem, write and read the disk at various cylinders and with different heads. The DDEC processes all read data the same. The drive may have a problem reading or writing different parts of the disk.
4) Look at all result descriptors and extended result descriptors. The drive status register may be recorded in the E.R.D. This often tells exactly the problem. Some bits of the E.R.D. are DDEC exceptions which explain the problem. Volume 3, Section 1 gives the meanings for the bits of the result descriptor and extended result descriptor. Table 4-4 in this volume can be used as a reference.

DDEC/DPC Fault Isolation

1) Offline, attempt to reproduce problems by doing the same operation from the maintenance panel. Most DDEC/drive problems can be reproduced this way.
2) Processor interface and D.P.C. problems are not detected offline. Put the DDEC online and run the Disk Pack Diagnostic test routine. Using the Disk Pack Diagnostic routine:

Symptom	Probable Cause
A result descriptor with transmission parity bit set	Data is being lost between the DPC and DDEC while it is being transferred in parallel. Run the DPC self test.
Data bits missing when reading but no firecode error or transmission parity error. Determine if read is wrong or if write is wrong	Serial to parallel data conversion is wrong in the DDEC for a read or parallel to serial conversion is wrong in the DDEC for a write.
Data shift	DDEC clock to the processor.

Voltage Margins

Use this procedure when a DDEC problem is too intermittent to troubleshoot. Adjusting the IC supply voltage close to the limits of their specification may cause the intermittent problem to happen more often. This makes troubleshooting easier.

1) Remove the top cover from the power supply.
2) Measure the voltage on the backplane +5 volt stud. Figure 4 shows the location of R115 on the power supply to adjust +5 volts and the +5 volt stud on the backplane to measure +5 volts.
3) Use a potentiometer adjustment tool to turn potentiometer R115 clockwise to increase the voltage. Do not go beyond +5.25 volts while adjusting the voltage, operate the DDEC to see if the problem exists.
4) Turn potentiometer R115 counter clockwise to decrease the voltage. Do not go beyond +4.75 volts. Operate the DDEC to see if the problem exists.

Use the same method to change the –5 volt supply by turning potentiometer R163. Do not go beyond –5.25 or –4.75 when changing this voltage. Figure 4-2 shows the location of R163 on the power supply and QHC30 on the backplane to measure –v volts. This –5 volts is used in the DDEC only to power the differential line drivers and receivers at the drive interface.

Clear Diagnostic Feature

The clear diagnostic feature lets the field engineer loop an operation in local mode when a T.D. bit is set in the result descriptor. Normally, a T.D. bit set in the result descriptor prevents more operations on that drive unit.

How to use the clear diagnostic feature:

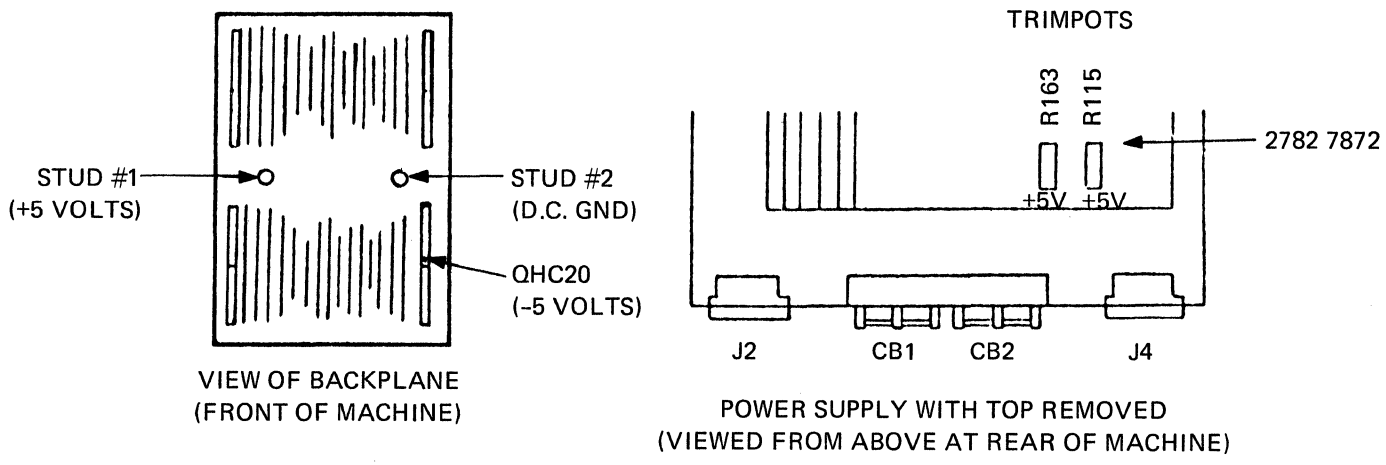


Figure 4-2. Voltage Adjustments

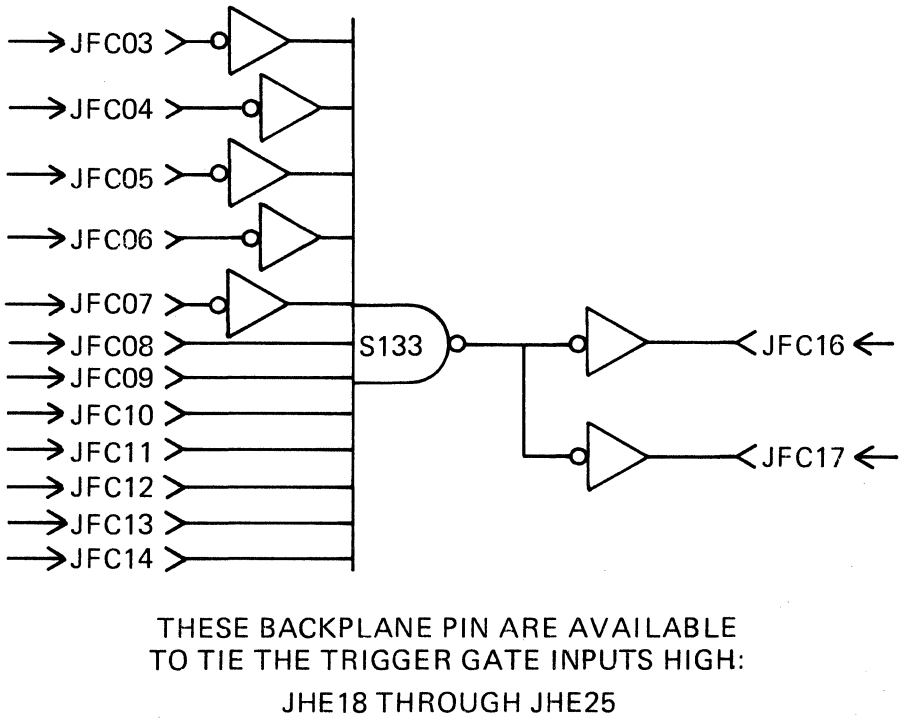


Figure 4-3. Trigger Gate

1) Use a wire jumpr from ENCLDIAG/ to a ground pin on the backplane.
2) Move the LOOP OP switch to the up position.
3) Do the local mode operation normally.

If a T.D. error stops the DDEC when the clear diagnostic feature is enabled and LOOP OP is up, the E.R.D. register is cleared and the T.D. is cleared. The operation is restarted normally.

Displaying the Firecode

The firecode of a sector is displayed on the maintenance panel in local mode. With the ALT OP switch in the up position the firecode for the first sector read is stored in maintenance memory. Follow these steps to display the firecode of a sector:

1) Load into maintenance memory addresses 0 and 1 and read Op code and the hexadecimal address of the sector to be read.
2) Place all maintenance panel switches in the normal positions as in table 4-6.
3) Place ALT OP switch in the up position. Place SGL SECT switch in the up position.
4) Press the START button once.
5) Place DISP ENBL switch in the up position.

Press STEP MEM until the memory address counter displays a binary 4. In the vertical display 16 bits of firecode are displayed Press STEP MEM to display memory address 5 which is the other 16 bits of firecode. Figure 4-4 shows the 2 words of firecode displayed.

Note that the firecode for the 207 drive is 56 bits long but that the above procedure displays only the first 32 bits. Some examples of firecode for certain data patterns are given in table 4-7.

Clock Stopper Feature

The clock stopper is a maintenance feature to stop the DDEC clocks and deselect the drive. Using this feature, a field engineer halts the DDEC when he wants and looks at logic states throughout the machine. Local Operation (offline):

1) Use a wire jumper to connect the trigger signal (any low to high transition) to pin DDC28 on the backplane.
2) Move the switch ENAB stop to the down position.

Remote Operation (online):

1) Use a wire jumper to connect the trigger signal (any low to high transition) to pin DDC28 on the backplane.
2) Use a wire jumper to connect the signal ENABSTOP/ to a ground pin.
3) After the stop clock has been used, remove the wire jumper to the signal ENABSTOP/. This prevents noise from triggering the clock stopper flipflop.

Trigger Gate Feature

On circuit board 20 in location J LOWER a trigger gate is wired to the backplane for field use. Figure 4-3 is a schematic with backplane inputs and outputs noted.

Inputs:

1) Use wire jumpers to the backplane input pins. The inputs can be from 0 to 8 high true signals and from 0 to 5 low true signals.
2) Use wire jumpers to connect unused inputs to ground or to the pull-up pins listed in figure 4-3.

Outputs:

1) One output pin JFC16 is a Schottky output for speed. This output is suitable for triggering the stop clock feature.
2) One output pin JFE17 is a standard output. It is suitable for triggering test instruments.

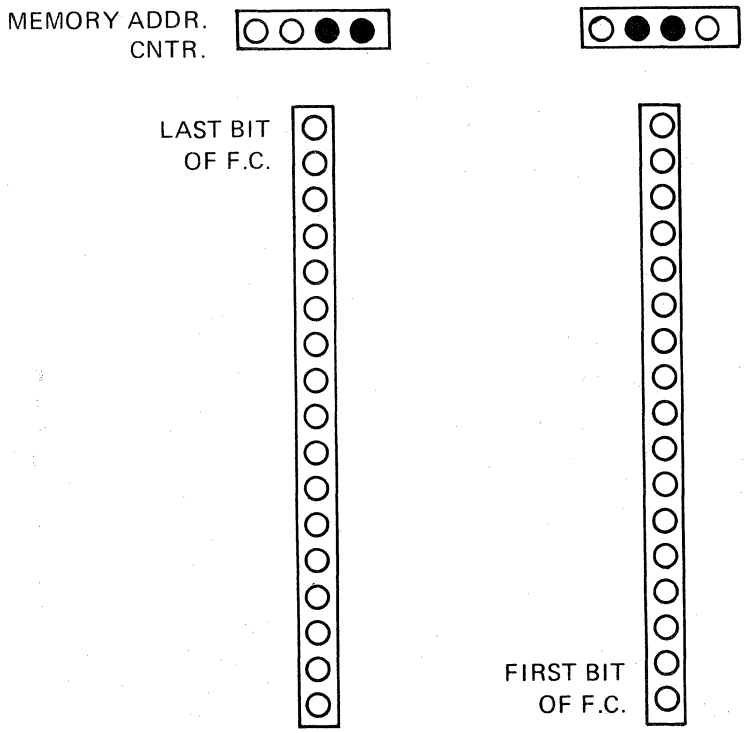


Figure 4-4. Display of Firecode

Table 4-7. Firecode Examples

DATA REPEATED	206 FIRECODE	207 FIRECODE
8001	200311A1	200311A1A2D7BA
0101	2001ADB2	2001ADB24CA264
FDFD	EAAA4AF3	EAAA4AF3725360
6363	A42284B9	A42284B9CB81C5
5555	A66AAD32	A66AAD3235E8F5
AAAA	OCF55065	OCF55065DEFF5D
8888	OF3BBF84	OF3BBF84B266CF
FFFF	AA9FFD57	AA9FFD57EB17A8
1111	A1F772F0	A1F772F0ECDBD1
0000	00000000	00000000000000
6DB6	8017BF1B	8017BF1BE8F28D
E4C6	0FECC576	0FECC576FC0BC1

EXTENDED RESULT DESCRIPTOR USAGE

If the TRY DIAGNOSTICS bit is set in the result descriptor at the end of an operation, the DDEC is locked out from that unit until a Read Extended Status Op is performed. The processor does a Read Extended Status operation and receives from the DDEC 64 bits of extended reult descriptor (E.R.D.).

This is put in the F.E. log when on system software or printed on the line printer when the Disk Pack Diagnostic test routine is used. In local operation, the E.R.D. is stored in maintenance memory for analysis after a Read Extended Status operation.

Volume 3, Theory of Operation, Section 1 under EXTENDED RESULT DESCRIPTOR gives the meaning for the different parts of the extended result descriptor. The method of doing the Read Extended Status operation is given in this section of Volume 1. Table 4-8 gives the meaning of all ERD bits.

CM Error

Notice in table 4-8 that if bit 10 word 3 in the ERD is set, a CM error has been detected by the drive. The CM in error is returned from the drive to the DDEC and stored in the ERD.

If the CM error bit is low, bits 09 to 01 of word 3 and bits 15 to 01 of word 4 are the drive status returned after a send status CM.

Some bits of the ERD are exceptions detected by the DDEC They are:

Fan Fail

The two fans mounted on the card cage of the DDEC have air switches. If air stops passing the switches the switches open. This causes a T.D. in the result descriptor and an E.R.D. is logged.

Drive Clock OK/

This means the drive clock is not good. This bit sets if drive clock transitions stop for more than three and one-half clock periods.

Address Mark Missing

A missing address mark does not cause an exception to stop the DDEC It gives a T.D. in the result descriptor if an address error occurs.

No Read Data Transitions

This does not cause an exception to stop the DDEC It gives a T.D. in the result descriptor if an address error occurs. The read data transitions that are detected missing are the sync character for the address.

Index Mark Missing

This bit is set when the drive does not send an index mark detected DM within 25ms of a request for index from the DDEC.

Bad DM Response

This bit is set for one of the following reasons:

1) the drive does not send a NOT READY DM after a seek CM or after a headswitch CM on the 207 drive.
2) A ROGER DM is not received within 65ms of a CM.
3) A ROGER DM is not received within 2 words, 3 bits of a READ ADDRESS MARK CM in MODE 5 or MODE 9.

Address Overflow

This bit is set if the sector address contained in the initiate words is beyond the maximum address of the drive unit being used.

Maintenance Log (ELOG)

System software keeps a log of errors which occur on peripherals. Figure 4-5 gives an example of a disk error in the log.

Result Descriptor

The result descriptor in the ELOG is the system result descriptor. It is made up from information about the system I/O operation and from the result descriptor sent by the DDEC Refer to the technical manual for the disk pack control being used. It gives the meaning for each bit of the system result descriptor. Here are some frequently used bits in the disk pack result descriptor:

bit 03	firecode error
bit 10	sector address error
bits 22 and 23	together indicate a TRY Diagnostic condition. An ERD is also printed.

Extended Result

The extended result is all zeros if no T.D. bits are in the result descriptor. The ERD is given in hexadecimal format. Change the ERD to bit format, then decode it according to table 4-8.

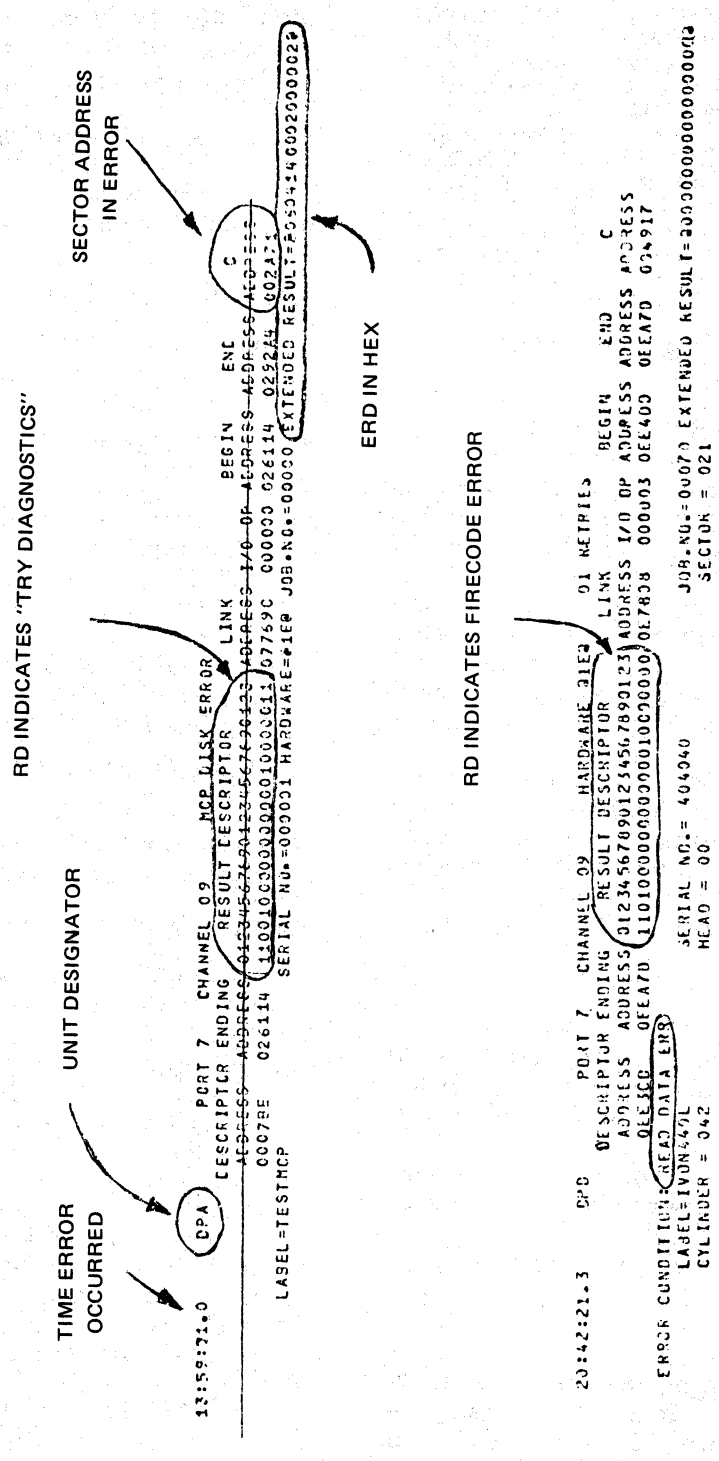


Figure 4-5. Disk Errors in the E-l0g (two formats are shown)

Word 1

INFO	NN	15	Cyl	add 2* 9	Address Decode
"	"	14		" 2* 8	
"	"	13		" 2* 7	
"	"	12		" 2* 6	
"	"	11		" 2* 5	
"	"	10		" 2* 4	
"	"	09		" 2* 3	
"	"	08		" 2* 2	
"	"	07		" 2* 1	
"	"	06		" 2* 0	
"	"	05		" 2* 10	
"	"	04		Zero	
"	"	03	Head	add 2*2	
"	"	02	Head	add 2*1	
"	"	01	Head	add 2*0	
INFO	NN	00	Sector	add 2*6	

Word 2

INFO	NN	15	Sector	add 2*5	Address Decode
"	"	14		" 2*4	
"	"	13		" 2*3	
"	"	12		" 2*2	
"	"	11		" 2*1	
"	"	10	Sector	add 2*0	
"	"	09	OP1		Command from DPC
"	"	08	OP2		
"	"	07	OP3		
"	"	06	U4		
"	"	05	U2		
"	"	04	U1		
"	"	03	N0		
"	"	02	N1		
"	"	01	N2		
INFO	NN	00	N3		

INFO	NN	15	Fan Fail	
"	"	14	Drive Clock OK/	
"	"	13	Address Mark Missing	
"	"	12	No Read Data Transitions	
"	"	11	Index Mark Missing	
"	"	10	CM Error = 0	CM Error = 1
"	"	09	DM09 *SR01 – 206	CM01 – Mark
"	"	08	DM10 *SR02 – 207	CM02 – Write/
"	"	07	DM11 *SR03 – '0'	CM03 – Read/
"	"	06	DM12 *SR04 – '0'	CM04 – Address Mode (206) Servo Search/ (207)
"	"	05	DM13 *SR05 – Maintenance Mode	CM05 – Parity Even
"	"	04	DM14 *SR06 – Write Data Missing	CM06 – Continue
"	"	03	DM15 *SR07 – '0'	CM07 – Address/Control
"	"	02	DM16 *SR08 – Seek and Not Ready	CM08 – Head or Cyl/Offset On (206)
"	"	01	DM17 *SR09 – Illegal Head	CM09 – Add Info – Offset In (206)
INFO	NN	00	DM18 *SR10 – Illegal Cylinder	CM10 – Add Info – Data Strobe Early

Word 4

INFO	NN	15	DM19 *SR11 – Spindle Address Error	CM11 – Add Info – Data Strobe Late
"	"	14	DM20 *SR12 – Offset During Write Enable (206) – '0' (207)	CM12 – Add Info – Power Up
"	"	13	DM21 *SR13 – Offset during Seek (206) – '0' (207)	CM13 – Add Into – Power Down
"	"	12	DM22 *SR14 – Seek Incomplete	CM14 – Add Info – Restore
"	"	11	DM23 *SR15 – Offtrack and Write Enable	CM15 – Add Info – Send Status
"	"	10	DM24 *SR16 – Carriage Hits Stop	CM16 – Add Info – Find Index
"	"	09	DM25 *SR17 – '0' (206) – Servo Lost (207)	CM17 – Add Info – '0'
"	"	08	DM26 *SR18 – Write Current and No Gate	CM18 – Add Info – '0'
"	"	07	DM27 *SR19 – No MFM Transitions (206, 207) or Drive Clock Error (207)	CM19 – Add Info – Reset Maint.
"	"	06	DM28 *SR20 – Head Select Fault	CM20 – Add Info – Set Maint.
"	"	05	DM29 *SR21 – DC Power Fault	CM21 – Write Enable
"	"	04	DM30 *SR22 – Temperature Warn.	CM22 – '0'
"	"	03	DM31 *SR23 – Temperature Critical	CM23 – Parity Even
"	"	02	DM32 *SR24 – RPM Less than 3420	CM24 – End
"	"	01	Bad ON Response	
INFO	NN	00	Address Overflow	

Table 4-8. Extended Result Descriptor

SECTION 5
ADJUSTMENTS

ADJUSTMENTS

Power Supply Adjustments

There are only two adjustments in the power supply. The +5 volt and –5 volt supplies can be adjusted for output voltage.

+5 Volt Adjustment

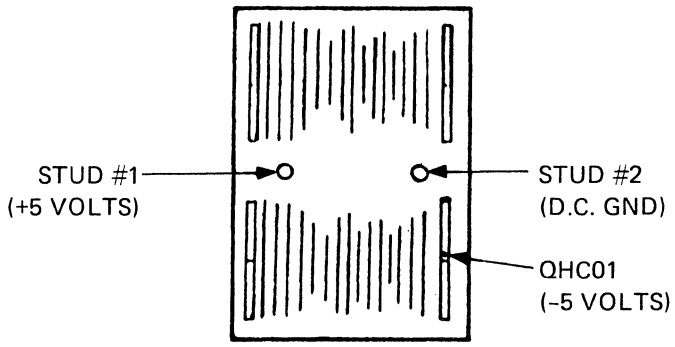
Figure 5-1 shows the backplane points to monitor the +5 volts. It also shows the location of the potentiometers in the power supply for adjusting the +5 and –5 volt supplies. Follow this procedure to adjust the +5 volts.

1) Remove the top cover of the power supply by first removing the six 10-32 screws with washers that hold it down.
2) Using a DVM, put the positive lead on the +5 volt stud on the backplane and the negative lead on the DC ground stud on the backplane. Refer to figure 5-1 for the stud locations.
3) Press the power switch on the operator panel so that the on light is illuminated.
4) Use a potentiometer adjusting tool to adjust R115 in the power supply while observing the voltage at the backplane on the DVM. Adjust the +5 volts accoding to table 5-1.
5) Proceed to the –5 volt adjustment.

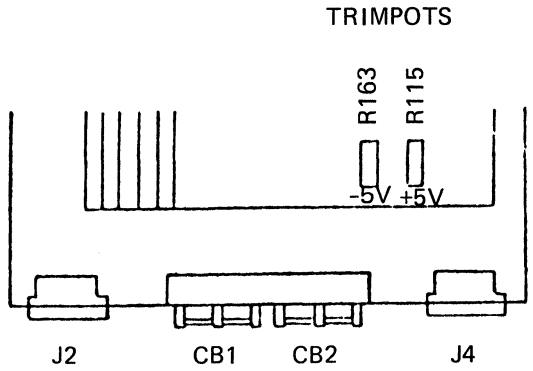
–5 Volt Adjustment

Perform the +5 volt adjustment as described earlier, then folow this procedure for adjusting the –5 volts.

1) Attach the positive lead of the DVM to pin QHC01 on the backplane. The negative lead remains on the DC ground stud.
2) Use a potentiometer adjusting tool to adjust R163 in the power supply. Observe the voltage at the backplane on the DVM. Adjust the –5 volts according to table 5-1.
3) Disconnect the DVM. Switch off the DDEC Replace the top cover of the power supply and the 6 screws that hold it down.



VIEW OF BACKPLANE
(FRONT OF MACHINE)



POWER SUPPLY WITH TOP REMOVED
(VIEWED FROM ABOVE AT REAR OF MACHINE)

Figure 5-1. Power Supply Adjustments

Local Clock Check

The 206/7 DDEC has a local oscillator with a fixed frequency. It is located on board 11. It should be checked on installation and when troubleshooting. To check the local clock do the following:

1) Attach a frequency counter or oscilloscope to the backplane pin DDE17. This is the signal CK10TEST.
2) At the operator panel press the power switch to illuminate the on button. Be sure the DDEC is offline.
3) Observe the clock frequency. It must fall within the range given in table 5-1.

Table 5-1. Summary of Adjustments

ADJUSTMENT	TEST POINT	ADJUST TO
+5 volts	+5 volt stud	+5v ± 1%
-5 volts	QHC01	-5v ± 1%
Local Clock	D.D.E.17	10MHZ ± 5%

APPENDIX A

SIGNAL GLOSSARY

Signal Name	Description	Schematic Page
ACCYL2*N	Address counter cylinder	01.04
ACHED2*N	Address counter head outputs	01.04
ACSEC2*N	Address counter sector outputs	01.04
ADBIT12	Address bit 12	01.03
ADCKNWD2	Address clock not word 2	01.01
ADCLOCK	Address clock	01.01
ADCMPEN	Address compare enable	15.02
ADCRYOUT	Address carry out	01.02
ADCYLHD	Hi for cyl decode low for head	01.01
ADCYL2*N	Address cylinder bits	01.03
ADDOVER	Address over limit (illegal)	06.05
ADDREQL	Address equal	15.03
ADDRINDX	Address mark or index	04.03
ADDVFLAG	Address over flag	06.05
ADHED2*N	Address head bits	01.02
ADHED2*2	Address head bit 4	01.03
ADLDREG	Address load register	01.01
ADMKER	Address mark error	12.04
ADMPXRNN	Address multiplexer output	01.02
ADMRK127	Address mark counter = 127	15.01
ADRIDXUP	Address or index up edge det	03.06
ADSEC2*N	Address sector bits	01.03
ADSNCBF	Buffered address sync flop	06.03
ADSNCFF	Address sync flip-flop	15.01
ADSTATE0	State 0 of decode control	01.01
ALTGOWERZ	Alternate go write zeros	10.02
ALTOPS	Alternate operations	23.02
ALTOPS	Alternate operations	13.01
AMKER207	Address mark error (207 only)	03.06
BADDMRSP	Bad drive message response	03.02
BITN	Bit n of address constant	01.01
BITNNA	Bit decimal outputs	18.02
BITNNB	Bit decimal outputs	19.01
BIT2*N	Bit counter output	18.01
BUFDATA	Write data to drive	14.07
BUFDCM	Buffered controller message	14.04
BUSY	DDEC busy	12.04
BUSYEXCH	Exchange busy flip-flop set	11.02
CEMRDATA	Format RD data for correction	21.04
CKADDMEM	Clock address memory	11.02
CKALTOPS	Clock alternate ops	13.02
CKCLRADR	Clock clear address	13.03
CKDPC	Clock to the DPC	10.04
CKIHBT	Clock inhibit (EPC generator)	15.02
CKINTWRD	Clock initiate word	10.07
CKRDBFFR	Clock read buffer	16.05
CKSKSTAT	Clock seek status flip-flop	12.03
CKWORD1	Clockinitiate word 1.	01.01
CK10DRV	10 mhz clock from drive	14.-05
CK10MHZ	10 mhz clock	11.04
CK10MHZA/	Main 10mhz clock	11.04
CK10MHZB/	Main 10mhz clock	11.04
CK10TEST	Test point for 10 mhz clock	11.04
CK5MHZ	5 mhz clock	11.04
CLADMKCT	Clear address mark counter	15.01
CLALSKST	Clear all seek status FFS	12.03
CLDSKLOC	Clear disk location counter	06.04
CLEAR	Clear push button	13.01
CLFMCNTR	Clear format counter	09.01
CLMD4FLP	Clear mode 4 flip-flop	06.01
CLRDIAG	Clear TD condition	03.06

APPENDIX A CONT.

Signal Name	Description	Schematic
CLRDMERR	Clear DM error	11.01
CLRLATCH	Clear latch	13.02
CLSECLOC	Clear sector location counter	06.01
CMADDMRK	Generate an address mark CM	07.06
CMENABL	Controller message enagle	07.05
CMERROR	Controller message error	04.03
CMGOIDLE	Generate a go idle CM	05.02
CMJMP30	Load CM counter to 30	14.01
CMLINN	CM line to drive n	14.07
CMLINN	Controller message line N	15.06
CMLNN	Long CM bit nn	14.03
CMLNN	Long CM bit nn	14.02
CMLOAD	Controller message load	05.03
CMMODEN	CM modes (decimal)	14.01
CMMODE2*N	CM modes	07.06
CMR/W	Read/write bit of CM	05.04
CMSEL	Select the drive	03.02
CMSELSPR	Generate a spare head CM	03.04
CMSTART	Controller message start	05.03
CMST30	CM counter in state 30	14.01
CMS21+29	CM counter in state 21 or 29	14.01
CM2–0M11	Head CM in mode 11	03.06
CNTROGDM	Roger DM count	04.02
CNTSHTDM	Short DM count	04.02
CONTROL	On off switch (front panel)	40.02
CRADCLR	Correction address clear	21.03
CRADINC	Correction address increment	21.03
CRMMDIN1	Correction memory data in(1)	21.02
CRMMDIN2	Correction memory data in(2)	21.02
CRMMDOT1	Correction memory data out(1)	21.01
CRMMDOT2	Correction memory data out(2)	21.01
CRMMWE	Correction memory write enable	21.03
CRM521ZR	Error corr mode 5 and 21 zeros	20.04
CRSRDBT	Correctable serial di-bit	21.02
CRSRDTOT	Corrected serial data out	20.06
CT747	Count 747	21.01
CT748	Count 748	21.01
CYLERREN	Cylinder error enable	15.02
CYLHDEQL	Cylinder and head equal	15.03
DATANN	Maint. memory output bits(16)	13.06
DATANN	Data bus lines	17.07
DATANN	Data bus lines	17.03
DATANN	Data bus lines	17.06
DATANN	Data bus lines	16.03
DATANN	Data bus lines	16.02
DATANN	Data bus lines	17.02
DATANN	Data bus lines	17.05
DEADSTOP	Stop 10mhz clock	11.02
DMBUF	Drive message buffer	04.01
DMCK10	DM 10mhz clock	04.02
DMCLK	DM clock	04.02
DMCNTHLT	DM counter halt	04.02
DMCNUE	DM continue	04.03
DMCRYOUT	DM counter carry out	04.02
DMCS2*N	DM counter outputs	04.02
DMCS30	DM counter at state 30	04.02
DMDTAIN	Drive message data in	14.05
DMERDFF1	DM-erd flip-flop 1	04.06
DMERDFF2	DM-erd flip-flop 2	04.06
DMEXCEPT	Drive message exception	04.04
DMFAULT	Drive message fault	04.04
DMLINX	DM line from drive x	14.07
DMRCVD	DM received	04.01
DMSRCK	DM shift register clock	04.01
DMSRCLR	DM shift register clear	04.01
DMCRCLRT	DM shift register clear	04.06
DMSRENB	DM shift register enable	04.01
DMSRFFK	DM shift reg ff (k term)	04.03

APPENDIX A CONT.

Signal Name	Description	Schematic
DMSTART	Drive message start	04.01
DMSTASNN	Drive message status bits	17.04
DPCBUSY	Disk pack control busy	16.02
DPCCLOCK	Disk pack control clock	16.02
DPCEXCBF	Buffered execute from dpc	16.02
DPCEXCTE	Disk pack control execute	16.02
OPCPAR	Disk pack control parity	16.02
DPCPARBF	Buffered parity to/from DPC	16.02
DPCREADY	Disk pack control ready	16.02
DPCRECV	DPC receiving	16.01
DPCRMOTE	Remote signal to DPC	16.01
DPCSEL	Disk pack control select	16.02
DPCSELBF	Buffered select from DPC	16.02
DPECEXC	dpec exception	11.01
DRIVCKOK	Drive clock ok	11.04
DRNCLK	Drive n clock	15.05
DRNCLK	Drive n clock	14.06
DRNDM	Drive n drive message	14.07
DRNDM	Drive n drive message	15.06
DRNDTA	Drive n data	15.05
DRNDTA	Drive n data	14.06
DRNPRSNT	Drive not present	04.08
DRONLINE	Drive on line	04.03
DRREADY	Drive ready	04.03
DRTHERE	Drive there	02.05
DRTHRCK	Drive there check	12.04
DRUNSAFE	Drive unsafe	17.08
DRXMIT	Drive transmit	10.03
DSKLOCEQ	Disk location equal	02.05
DTALINNX	Negative diff data to drive x	14.06
DTALINNX	Negative diff data to drive x	15.05
DTALINPX	Positive diff data to drive x	15.05
DTALINPX	Positive diff data to drive x	14.06
DTAREGNN	Data register bits (16)	13.05
DTSNCSTF	Data sync start found	15.01
DTSNDSLD	disable loop op when DTSNCSTF/	15.01
DTSYNCER	Data sync error	12.02
ECCUSED	Error correction used	20.04
ENABLWR	Enable write	11.03
ENABSTOP	Enable stop clock feature	23.02
ENADRCT	INNADRCT delayed one bit	01.01
ENCD32BT	Encode 24 firecode using 32 BT	20.06
ENCKTEST	Enable clock test	03.02
ENCLDIAG	Enable clear diagnostics	04.08
ENDMDE8	End mode 8	08.01
ENDOFCYL	End of cylinder	01.07
ENDOFPAK	End of pack	01.07
ENDOFTRK	End of track	01.06
ENSCXFR	End sector transfer	12.02
ENSELTRM	Allow select to terminate	03.01
ENSNCDET	Enable sync character detect	12.01
ENSTATER	Enable status errors	04.01
EPCCLR	Clear error protection code	15.02
ERCCKINH	CKDPC inhibit during err corr	21.04
ERCRMDNN	Error correction mode n	21.04
ERDCLR	ERD clear	04.05
ERDENRD	Enable all zeros rd in senderd	10.01
ERDFCFB	Buffered erd flip-flop c.	04.05
ERDFFA	Extended result flip-flop A	04.05
ERDFFB	Extended result flip-flop B	04.05
ERDFFC	Extended result flip-flop C	04.05
ERDFFD	Extended result flip-flop D	04.05
ERDXFREN	ERD transfer enable	04.05
ERDXMTNG	ERD transmitting	04.05
ERRCORCT	Error correct	12.05
EXCHBUSY	Exchange busy to DPC	16.02
EXECUTE	Execute	16.01

APPENDIX A CONT.

Signal Name	Description	Schematic
EXTTRIG	Standard output of trigger gt	20.06
FANFAIL	DDEC logic gate fan failure	11.01
FCDDESEL	Forced deselect	11.04
FCDHDTOS	Forced head to spares head	03.04
FCDRRDY	Force drive not ready	07.04
FEERTEST	Fire code error test point	10.06
FIRCRERR	Fire code error	10.06
FIRCMPEN	Fire code compare enable	09.01
FIREIN	Input to firecode (207)	14.07
FIRINBUF	Input to firecode gen (206)	14.07
FIREIN24	Input to 24 bit F C gen (207)	20.06
FIRENCEN	Fire encode enable	09.08
FIREONBS	Firecode on bata bus	03.04
FIREOUT	Firecode output	20.06
FIRESHEN	Fire code shift enable	09.08
FIRNN	Fire code shift register bits	20.03
FIRNN	Fire code shift register bits	20.02
FIRNN	Firecode shift register bits	20.01
FLAGWRTN	Flag written	12.02
FMCNTF	Format counter full	09.07
FMCNTN	Format counter decimal outputs	09.07
FMGOIDLE	Format go idle	09.06
FMIDLING	Format idling	09.01
FMRDATA	Format read data	09.02
FMRFIRE	Format read fire code	09.02
FMSENDRD	Format send result descriptor	09.02
FMTS0	Format control state zero	10.01
FMWRADDR	Format write address	0905
FMWRDATA	Format write data	09.04
FMWRFIRE	Format write fire code	09.04
FMWRONES	Format write ones	09.05
FMWRZERO	Format write zeros	09.03
FNSWFAIL	Fan failure switch	40.02
FRENCD	Fire encode	10.04
FRENCDP	Fire encode (207 - 24 bit)	10.04
FRENCD24	Fire encode 24 bit	20.01
FRR+WMDE	Firecode read or write mode	20.01
FRRDMD	Fire read mode	09.08
FRWTMD	Fire write mode	10.04
GM9F4207	Go to mode 9 from 4 (207 only)	03.05
GSGTOENC	Any go to is in progress	08.05
GTMDNDLD	Go to mode n delayed one clock	07.01
GTMD15DLD	Go to mode 15 delayed one clk	07.04
GTMNDLD	Go to mode n delayed one clock	08.01
GT1+15DL	Go to mode 1 or 15 delayed	09.06
HDCNTCLR	Clear head counter	01.06
HDCNTEN	Head count enable	01.06
HDCTST23	Header counter state 23	15.02
HDCTST31	Header counter state 31	15.02
HEADERR	Head error (in drive)	17.08
HEAD2*N	Head select binary output	16.05
HEDRERR	Header error	11.03
IDLE	Idle mode	11.01
IDXMRKER	Index mark error	16.04
ILLCYL	illegal cylinder	17.08
IMMDSEEK	Immediate seek	12.05
INADRMRK	Increment address mark counter	06.03
INSECLOC	Enable sector location CNTR	06.02
INDSKLOC	Increment disk location cntr	06.04
INDXSRCH	Index pulse search	11.02
INFONN	Information lines nn	16.02
INFRENCD	Inhibit fire encode	20.06
INH24REG	Inhibit 24 shift reg (207 fc)	21.04
INITBF	Initialise op	10.03
INITCONT	Initialise continue	08.01
INITIAL	Initialize operation	04.07
INNADRCT	Increment address counter	06.03

APPENDIX A CONT.

Signal Name	Description	Schematic
INTLSECN	Interleave sector n	02.01
INTTRIG	SCHOTTKY output of trigger GT	20.06
INUNITCT	Increment unit counter	03.06
ISELECT	Derivative of DDEC select line	16.01
JMMF2	J Term, memory control FF2	21.03
KMMF1	K term, memory control FF1,	21.03
KMMF2	K term memory control FF2.	21.03
KTRMINSL	K term of inselcloc flip-flop	05.05
LDFORBOT	Load for beginning of track	19.02
LDPRDBT	Load paralell di-bit	21.03
LDPSPREG	Load paral/serial/paralel reg	09.08
LDRDBFDL	Load read buffer delayed	15.03
LDRDBFFR	Load read buffer	09.08
LDSECLOC	Load sector location counter	15.01
LDSRDBT	Load serial di-bit	21.02
LDWRBFFR	Load write buffer	09.08
LEDNN	Light emitting diode nn	13.06
LNDMFLFF	Long DM fail flip-flop	03.05
LOAD	Load push button	13.01
LOADAC	Load address counter	15.02
LOC=0	Disk location equals zero	02.01
LOCEXEC	Local execute (slip)	23.02
LOCLEXEC	Maintenance execute signal	13.01
LOC89	Disk location equals 89	02.01
LONGDM	Long drive message	04.03
LONGDMS	Long drive message sensed	07.03
LOOPHEAD	Loop head	13.01
LOOPHEAD	Loop head	23.02
LOOPMD10	Loop in mode 10	12.02
LOOPOP	Loop operation	13.01
LOOPOP	Loop operations	23.02
LOOPSEC	Loop sector	13.01
LOOPSEC	Loop sector	23.02
MAINCLR	Main clear reset	16.05
MAINMD*N	Mode flip-flops (binary)	08.05
MASTRCLR	Master clear	13.01
MDE4-RWV	Mode 4 and read write or verify	08.04
MDE4FLOP	Mode 4 flip-flop	03.05
MDE5FLAG	Mode 5 flag	03.05
MDE8FLAG	Mode 8 flag	03.05
MDE9FLAG	Mode 9 flag	03.05
MEMUN2*N	Memory address unit bits 02.04	
MEMWRTEN	Memory write enable	02.04
MFIRCDEN	Maint firecode enable	13.02
MMSCLR	Memory flip-flops clear	21.03
MMSN	Memory state n	21.02
MMSO	Memory state 0	21.02
MNCLRRAW	Main clear raw reset pulse	16.05
MNERWD1	Maintenance erd word 1	04.05
MNTAD2*N	Maintenance memory address	13.02
MNTCK1A	Maintenance clock 1A	13.02
MNTCK1B	Maintenance clock 1B	13.02
MNTDESEL	Maintenance de-select	03.04
MNTMEME	Maint. memory enable	13.02
MNTRDEN	Maintenance rd enable	10.01
MNTSEL	Maintenance select DDEC	13.04
MNTWREN	MAINT. write enable	13.02
MODEN	Mode n	05.06
MODENA	Mode n	07.05
MODENC	Mode n	06.06
MPXRSELA	Multiplexer select A	15.03
MPXRSELB	Multiplexerselect B	15.03
NEEDTOWR	Need to write	09.08
NN	N variant bits	17.01
NOADD-LO	No address load	23.02
noaddld	No address load	13.01
NOEXCH	No exchange	04.08

APPENDIX A CONT.

Signal Name	Description	Schematic
NOHALTERR	No halt on error	11.03
NOROGDM	No roger DM	03.01
NRMUNST	Normally unsettled	03.02
NROGMDE5	No roger DM in mode 5	07.02
NROGMDE9	No roger DM in mode 9	07.03
NSPHD206	Not spare head and unit is 206	11.02
NTSTNRMT	Not a test op and not offline	16.05
NWRTMD6	No write in mode 6	09.04
OFFSETEN	Offset enable (variant)	12.05
OFFSETIN	Offset in	12.05
OLD=NEW	Old cylinder equals new cyl.	02.04
OPFIR	Output fire code register	10.05
OPN	Operation code n bits	17.01
OVRLAPDS	Disable overlapping seek	13.01
OVRLAPDS	Disable overlapping seek	23.02
PARGENOP	Parity generator output	17.03
PBCLEAR	Push button clear	23.02
PBHALTER	Push button halt on error	13.01
PBHALTER	Pushbutton halt on error	23.02
PBLOAD	Push button load	23.02
PBMNCLR	Push button main clear	16.05
PBMSTCLR	Pushbutton master clear	13.01
PBMSTCLR	Pushbutton master clear	23.02
PBNOHALT	Push button no halt	13.01
PBNOHALT	Pushbutton no halt	23.02
PBSTART	Push button start	23.02
PBSTMEM	Push button step memory	23.02
PBSTOP	Stop pushbutton	23.02
PCLADMCT	Part of clear add mark CNTR 04.07 Phase lock oscillator	06.04
PLOEARLY		04.07
PLOLATE	Phase lock oscillator late	04.07
PMFRPOL	Pre-mult and fire polynomial	20.01
PM5KINSL	Part 5 of K term of insecloc	05,04
PNGNNFRN	Part n of go to mode n from n	07.02
PNINDKLC	Part n increment disk log CNTR	20.01
PRMPOL	Pre-multiplication polynomial	20.01
PROC DATA	Processor data	04.07
PRVUNSEL	Previously unselecte	04.03
PSPSEROT	Serial data out of the PSP reg	17.02
PTENDCYL	Part of end of cylinder	01.06
PTNGMNN	Part n of go to mode nn	07.02
PTNJINSL	Part n of J term for INSELOC	06.01
PTXCMLOD	Part x cm load	05.02
PTXGMD15	Part x of go to mode 15	07.03
PT1CLSLC	Part 1 of CLSECLOC	07.01
PT1CMLOD	Part 1 CM load	05.01
PT2CMLOD	Part 2 CM load	05.01
PT3CMLOD	Part 3 CM load	05.01
PT4CMLOD	Part 4 CM load	05.01
PT7GMD15	Part 7 go to mode 15	03.01
PWRRESET	Power on reset	16.05
PWRRSYNC	Power on reset synchronized	16.05
P1BDMRSP	Part 1 bad DM response	12.02
P1GTM9F9	Part 1 go to mode 9 from 9	03.05
P1INADMK	Part 1 of INADRMK	06.04
P2BDMRSP	Part 2 bad DM response	12.02
P2GTM9F9	Part 2 go to mode 9 from mode 9	15.03
RAWCKDPC	Raw clock to DPC	09.07
RAWDTAIN	Raw data in	14.05
RDATA	Read data	09.01
RDBIT01	Result descriptor bit 01	20.06
RDBIT15	Result descriptor bit 15	11.02
RDBUFFEN	Read buffer enable	10.01
RDMAINT	Read maintenance operation	04.07
RDYSTATS	Ready status	16.02
READ	Read operation	04.07
READY	DDEC ready to transfer data	12.04

APPENDIX A CONT.

Signal Name	Description	Schematic
RELADDR	Relocate using address data	04.07
RELDATA	Relocate using DPC data	04.07
RELOC	Reloate operation	12.05
RELPASS2	Second pass of relocate op	12.05
REMOTE	Remote (on line)	13.01
REMOTSW	Online switch (front panel)	40.02
RESDESEN	Result descriptor enable	10.01
RESTORE	Restore or rezero (the drive)	11.01
REVSDONE	Revolutions done (256 ADMKS)	15.01
ROGERDM	Mark bit DM	04.01
ROGERINC	INCSECLOC when roger DM received	05.04
RWV	Read write or verify	11.03
SECMPXRBN	Sector multiplexer	02.02
SECNTCLR	Clear sector counter	01.06
SEEKINCL	Seek incomplete	17.08
SELECT	Select	17.08
SEL84ADR	Select sector 84 address	12.05
SEND ERD	Read extended result descr.op.	04.07
SENDSTS	Send status	11.01
SERDTA=0	Serial data = zeros	09.08
SERDTAIN	Serial data in	11.03
SERHEDR	Serial header	02.03
SERMPXRO	Serial multiplexer 0	10.03
SERMPXR1	Serial multiplexer 1	10.03
SERTOPSP	Serial data to PSP registers	21.03
SERVOERR	Servo error	12.04
SETSKSTS	Set seek status	12.03
SETXBUSY	Set exchange busy flip-flop	07.02
SGLSECTR	Single sector switch	13.01
SGLSECTR	Single sector	23.02
SKSTATUS	Seek status	15.04
SPAREHED	Spare head	11.02
SPRVRFY	Spare sector verify	12.05
SRD	Send result descriptor	09.01
SRDTDLYD	Serial data delayed	10.06
STADRCMP	Start address compare	15.01
START	Start local operation	13.04
STBLKRDY	Force drive status to not ready	12.03
STDTAXFR	Start data transfer	15.01
STEPENAB	Step enable	13.02
STEPMEM	Step to next memory address	13.01
STERDOUT	Start erd out Ext. Result Descr.	11.02
STMMRD	Start memory read	21.04
STMMWT	Start memory write	09.075
STOP	Stop pushbutton	13.01
STROBADR	Strobeaddress	06.05
STRTLTCH	Start latch	13.01
STUKDATA	SERDATAIN stuck high or low	11.02
ST25TIMR	Start 25ms timer	11.02
ST250TMR	Start 250 microsecond timer	03.06
ST8TIMR	Start 8 second timer	03.02
SWBUSEN	Switch bus enable	13.02
SWDSPEN	Enable stepping of maint. add	13.01
SWDSPEN	Switch display enable	23.02
SWLOCAL	Switch to local 10 mhz clock	03.02
SWNN	Maintenance panel switches	23.01
SWTODR	Switch to drive 10 mhz clock	03.02
S0CTRL	S0 control	15.02
S1CTRL	S1 control	15.02
TESTOP	Test operation	04.07
TMOT25MS	25 msec timeout	16.04
TMOT25OU	250 usec timeout	16.04
TMOT8SEC	8 second timeout	16.04
TM250206	250 usec timeout and 206	06.02
TRCKDPC	Transfer clock to DPC	03.04
TRGTRESN	Pull up test point n	20.05
TRYDIAG	Try diagnostics	04.05

APPENDIX A CONT.

Signal Name	Description	Schematic
TSTSTKDT	Test stuck data	12.01
UNITEQL	Unit equal	03.03
UNITNSEL	Unit n selected	14.05
UNIT2*N	Unit select bits	17.01
VERIFY	Verify operation	04.07
WDTA32BT	Write 32 bit firecode for 207	20.06
WFRS0	Fire state machine state zero	10.01
WNNA	Word decimal outputs	18.02
WNNB	Word decimal outputs	19.02
WNNB	Word decimal outputs	19.01
WNNBNN	Word nn bit nn	19.04
WNNBNNA	Word nn bit nn decodes	18.06
WNNBNNA	Word nn bit nn decodes	18.03
WNNBNNA	Word nn bit nn decodes	18.05
WNNBNNA	Word nn bit nn decodes	18.04
WNNBNNB	Word nn bit nn decodes	19.05
WNNBNNB	Word nn bit nn decodes	19.06
WORD2*N	Word counter output	18.01
WRADR	Write address	09.01
WRD	Write data	09.01
WRDA	Write data	09.01
WRD0-31A	Word counter is at 0 thru 31	18.01
WRFIR	Write fircode	09.01
WRITDIAG	Diagnostic write fire code	12.05
WRITE	Write operation	04.07
WRITEA	Buffered write	09.04
WRLOKOUT	Write lockout	17.08
WRTMD6	Write in mode 6	09.04
WRZ	Write zeros	09.01
WR1	Write ones	09.01
WR32HEDR	Write 32 bit address header	10.03
WTPROCDT	Write processor data	09.08
W64B	Word 64 (bit 0)	19.02
W96-127B	Word 96 to 127	19.02
XMENABLE	Transmit enable	10.01
XMEN+TD	Transmission error or try diag	11.02
XMITENAB	Transmit enable	16.01
XMTNPERR	Transmission parity error	17.03
206-207	High when unit selected is 206	03.03
206BFM	Buffered 206/207 (hi for 206)	06.01
207BFM	Buffered 206/207 (hi for 207)	06.01
207FRER	Firecode error (207 only)	20.04
21ZR	21 zeros	20.04
24ZR	24 zeros	20.05

USEFUL TEST AND TRIGGER POINTS

Signal	Description	Backplane Pin
ADRIDXUP	Pulses high when an address or	
ADRIDXUP	Index mark detect DM rec,d	MDC23
Bit2*0		LHE28
Bit2*1		LHE27
Bit2*3		LHE11
BIT2*2		LHE10
BIT2 3		LHE11
BUFDCM	Controller message	QFC30
CK10DRV	10 mhz clock from drive	QHE06
CK10TEST	Local or drive clock	DDE17
DMDATAIN	Drive message (inverted)	QHE19
ENCLDIAG/	Jumper this to GND to enable	
ENCLDIAG/	The clear diagnostic feature	LBC09
FIRMCMPEN	Goes high at start of FDC22	
	FRERRTEST F.C.error on sector just read	EBE24
INTTRIG	Triggering output of trig gate JFC16	
MODE01		GBE20
MODE02		GBE06

APPENDIX A CONT.

Signal	Description	Backplane Pin
MODE03		GBC05
MODE04		GBE03
MODE05		GBC03
MODE06		GBE04
MODE07	Mode signals are high	GBE20
MODE08	for the time the DDEC	GBE06
MODE09	Is in that mode	GBC05
MODE10		GBE16
MODE11		GBC15
MODE12		GBE13
MODE13		GBC12
MODE14		GBE12
MODE15		GBC16
RAWDTAIN	Data to and from the drives	QFE23
RDATA	GOES HIGH AT START OF DATA RD.	FDE23
STOPCLOK	Triggers the clock stopper	DDC28
STOPCLOK	Feature when ENBSTP SW is down	DDC28
TRGPNTNN	(5 low true 8 high true)	TO15
TRGPNTNN	Triggering inputs of TRIG gate	JFC03
TRGPNTNN	(5 low true 8 high true)	TD15
TRM32BT	End of first 32 bits of 207 FC	HHE28
WORD2 0	Binary output of sector	LFE25
WORD2*1	Location counter	LFC25
WORD2*2		LFC15
WORD2*3		LFC14
WORD2*4		LFE14
WORD2 5		LFE23
WORD2 6		LFE22
WRADR	Start of address write	FDE15
WRD	Goes high at start of data WRT	FBE25
WRFIR	goes high at start of F.C. WRT.	FDC14