*Revision via ECN 5785, January 1976. Changed pages go from A to B, B to C, C to D, and D to E revision level with new pages at A revision. ECN is distributed with revised pages as a record of what has changed.

Revision via ECN 5804, March 1976. Changed pages go from A to B, B to C, C to D, D to E, and E to F revision level with new pages at A revision. ECN is distributed with revised pages as a record of what has changed.

*Latest Rev.
Per ECN 6784

*Revision via ECN 6343, October 1976. Changed pages go from A to B, B to C, C to D, D to E, E to F, and F to G revision level with new pages at A revision. ECN is distributed with revised pages as a record of what has changed.

Revision via ECN 6784, April 1977. Changed pages go from A to B, B to C, C to D, D to E, E to F, F to G, and G to H revision level with new pages at A revision. ECN is distributed with revised pages as a record of what has changed.

INTRODUCTION TO THE NEW TEST & FIELD EDITION OF THE B1700 HARDWARE RULES

This Test and Field edition of the B1700 Hardware Rules includes information specifically for field use. The T & F edition is identified by the eight digit number A 2211 2569 A.

The source document for this edition is the B1700 Hardware Rules (A 2201 6150). It is intended that where necessary the source document and this edition will be kept in step.

The contents include most of the source data, only omitting material of interest primarily to the designer. The sections in this edition are numbered as in the source book. The source Introduction (below) states the scope of the book; only omissions are references to design matters not included in this edition.

INTRODUCTION to the B1700 HARDWARE RULES

This is the fourth issue of B1700 Hardware Rules for use in the design of the B1700 family of systems. Since the publication of the first set of logic rules in December 1968, the family of circuits has expanded.

The hardware rules specified herein are a culmination of all the previous sets of logic and circuit rules and supersede them. They are intended for use in the B1700 family of systems, with the CTL, TTL, Silicon Gate, P MOS and other special circuits. It is the intent of these rules to allow maximum flexibility in design, and at the same time to achieve minimum propagation delays, acceptable waveforms and stability.

A comprehensive set of terms are defined so that consistent understanding, interpretation and application of the rules will result.

The document contains circuit parameters for the CTL, Small and Medium scale integrated circuits. Some TTL circuits, which are used in scratchpad, M string and main memories, as well as for Code Conversion, are also described. P MOS circuits are used for serial and random access memory. The interface circuits which talk to and from peripheral input output equipments are also incorporated. Delay lines, resistor and capacitor networks are included due to their usage in the systems.

A comprehensive summary of the device characteristics is provided for quick and easy reference.

The circuits are packaged on a 12 X 12 PC board. The card details and guidelines for circuit placement are described in section 5.

The B1700 family processors operate at 2, 4, or 6 M HZ clock rate. The clock system characteristics are described in section 7.

INTRODUCTION to the B1700 HARDWARE RULES (Continued)

Signals propagate on the card, between cards, and to other card housings, on both the front plane and back plane, and out of the mainframe as well.

Supplements and revisions will be issued periodically to keep the information correct and up to date.

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DEFINITION OF TERMS

The following is a partial list of definitions for those terms that are used in the B1700 Circuit Rules.

Power Supply Voltages:

The power supply voltages used in the B1700 are as follows:

V_{EE} Negative Logic Power Supply Voltage

nominal -2.0 volts
tolerance $\pm$0.1 volts

V_{cc} Positive Logic Power Supply Voltage

nominal 4.75 volts
tolerance $\pm$0.25 volts

V_{11} Negative Line Driver/Receiver Power Supply Voltage

nominal -12.0 volts
tolerance $\pm$0.6 volts

V_{22} Positive Line Driver/Receiver Power Supply Voltage

nominal 12.0 volts
tolerance $\pm$0.6 volts

Guaranteed Input Thresholds:

Those voltage levels at the input which determine the threshold region of a logic element. For CTL MSI devices these guaranteed input thresholds are:

V_{IL} = 0.8V @ T_j = 25° C
= 0.65V @ T_j = 100° C
V_{IH} = 1.25V @ T_j = 25° C
= 1.10V @ T_j = 100° C

Where T_j is the temperature of the semiconductor junctions on the chip

Example: At T_j = 25° C

Input voltage greater than 1.25 volts is a logical "1".

Input voltage less than 0.8 volts is a logical "0".

Threshold Sensitive:

Any input to a logic element whereby the input voltage is quantized to represent a logical "0" or logical "1" is considered to be threshold sensitive.

When applied to MSI devices, the quantizing levels are understood to be equal to the Guaranteed Input Thresholds.

DEFINITION OF TERMS (Continued)

Restored True Level:

Voltage levels at the output of a logic element that satisfy the following conditions:

$2.4V \leq V_{oH} \leq 3.35V \quad @ \quad T_j = 25° C$

$2.3V \leq V_{oH} \leq 3.35V \quad @ \quad T_j = 100° C$

Where V_{oH} is the logical "1" voltage at the output.

The above equalities should apply for all acceptable DC loading of the device.

Restored False Level:

Voltage levels at the output of a logic element that satisfy the following conditions:

$-1.0V \leq V_{oL} \leq -0.55V \quad @ \quad T_j = 25° C$

$-1.0V \leq V_{oL} \leq -0.40V \quad @ \quad T_j = 100° C$

Where V_{oL} is the logical "0" voltage at the output.

The above inequalities should apply for all acceptable DC loading of the output.

Nominal True Level:

2.5 volts

Nominal False Level:

-0.7 volts

Restorer:

A logic element that will always have output voltages which correspond to either a Restored False Level or a Restored True Level.

Gate Element:

Any logic element for which the voltage swing at the output is always less than any voltage excursion at the input (s).

Gate Offset:

For a CTL gate element the output voltage will be determined by the most negative input voltage. In general, when this input voltage is at a true level the output will be less than the input; and when this input is at a false level the output will be greater than the input. The absolute magnitude of the difference between the output voltage and the most negative input voltage is the gate offset. True and false offset voltages are approximately equal to 200 millivolts/gate element.

Logic Level:

To describe the effects of gate elements on the true and false logic voltages, it has become convenient to define logic levels that correspond to transmission of a restored level through several gate elements.

Level 0 is the output of a restorer and level n is the output of a cascade of n gates that is being driven by a restorer

DEFINITION OF TERMS (Continued)

'AND' Function (•):	A true output occurs when all inputs are true. Basic CTL gates perform the 'AND' function.
'OR' Function (+):	A true output occurs if any input is true. The 'OR' function is provided by wiring together the outputs of two or more CTL logic elements.
Exclusive 'OR' Function (⊕):	A true output occurs if an odd number of inputs is true.
Risetime (T_R):	The time difference between the 10% voltage point and the 90% voltage point on the positive going edge of a waveform.
Falltime (T_F):	The time difference between the 90% voltage point and the 10% voltage point on the negative going edge of a waveform.
Propagation Delay Time (T_d):	The time difference between the +1.0 volt point on the input waveform and the +1.0 volt point on the resultant output waveform.
Pulldown Resistor:	A resistor connected from the output of a logic element to the V_{EE} supply voltage. The purpose of the pulldown resistor is to reduce the output falltime.
CTL Gate Load:	One CTL gate load is equal to a 2 kilohm pulldown resistor in parallel with 5 pF.
DC False Level CTL Load (n_f):	The ratio of DC load current produced by a Nominal False Level to that current which would be produced in a CTL gate load by the same voltage (i.e., load current divided by 0.65 mA).
DC True Level CTL Load (n_t):	The ratio of DC load current produced by a Nominal True Level to that current which would be produced in a CTL gate load by the same voltage (i.e., load current divided by 2.25 mA).
DC Input Loading:	The load, at nominal levels, of the input to a device.
DC Output Loading:	The load presented by the output of a logic element when that output is being driven by a source which is wire 'OR'ed with that element.
Output Drive Capability:	The number of DC True Level CTL Loads that a logic element will be able to drive at its output and still maintain the proper logic level.

DEFINITION OF TERMS (Continued)

DC Output Drive Capability/Package:	The total number of DC True Level CTL Loads that may be driven by all outputs of logic elements within an IC package. This results from the maximum power that can be dissipated by the dual in-line package.
Logic String:	Gate logic between two restorers.
Clocked Logic String:	Logic between two clocked restorers.
Line:	Wire or etching that connects two or more circuits or pulldowns.
Source:	Circuit driving a line.
Line Loads:	The number of loads, external to a source, that are connected to a line. This includes the output loading of other sources.
Tap:	Short length of etching (less than 6 inches) which connects one or more circuits (via a card connector) to any point along a backplane wire except at the ends of a backplane wire.
'Y'	That point on a line where a signal source can emanate in two directions. Each path of a 'Y' is called a leg. When that point is not a signal source, it is a tap.

3.0 Device Descriptions. This section of the B1700 Hardware Rules carries functional descriptions of those integrated circuits approved for use in the B1700 systems. Both passive and active devices are included.

CTL (Complementary Transistor Logic) Circuits. Those integrated circuits which have CTL input or output levels are described in subsection 3.1.

TTL or T^2L (Transistor-Transistor Logic) Circuits. Describes those TTL integrated circuits to be used in the B1700. Subsection, 3.2.

MOS (Metal Oxide Semiconductor) Integrated Circuits. Describes serial and random access memory devices for the B1700. Subsection, 3.3.

Interface Circuits. Line drivers, receivers, and sense amplifiers are described herein. Subsection 3.4.

Miscellaneous Circuits. Descriptions of passive components, networks and linear amplifiers used in the B1700. Subsection 3.5.

AFAN

3.1 CTL Integrated Circuits

Element Type:	AFAn
Standard Assembly Number:	1904 0179
Manufacturer's Type:	9822
Circuit Designation:	Dual Full Adder/Subtractor

Description of Operation:

The AFAn consists of two separate adder/subtractor circuits with a common mode control, M0. A logical zero (one) input to the M0 line will cause the circuit to add (subtract). All inputs are threshold sensitive. Outputs are restored. Inputs A and B are the bits to be added (subtracted) and C is the carry (borrow) input. The functions computed are A + B or A - B. Output S is the sum or difference output, and outputs P and G are used with the CFBn Carry Logic Gate to comprise a fast adder.

Type of Package: 16 Pin Dual In-line

DC Input Loading:

A0 B0 A1 B1	Data Inputs	0.8 CTL Loads
C0 C1	Carry/Borrow Inputs	0.8 CTL Loads
M0	Mode Control Input	0.8 CTL Loads

DC Output Loading:

S0 S1	Sum Outputs	No Load (diode to ground)
P0 P1	Propagate Outputs	No Load (diode to ground)
G0 G1	Generate Outputs	No Load (diode to ground)

DC Output Drive Capability: 12 CTL Loads

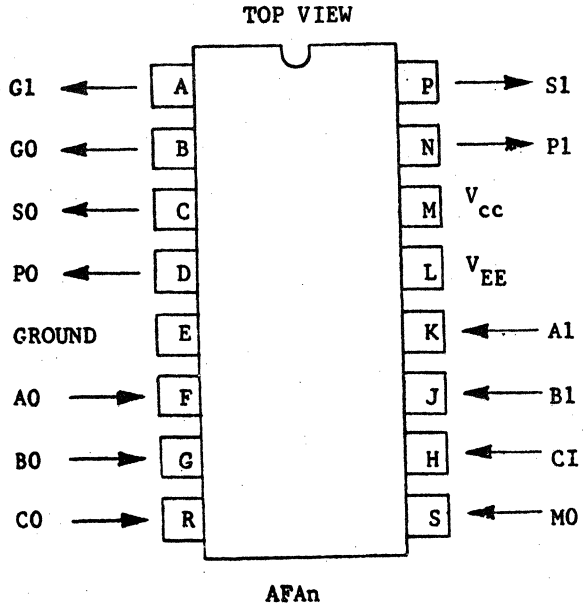
DC Output Drive Capability/Package: 72 CTL Loads

Input Levels Allowed: Levels 0, 1, 2, 3, 4

Output Levels Generated: Level 0

Propagation Delay Time: 22 ns

Pin Locations:



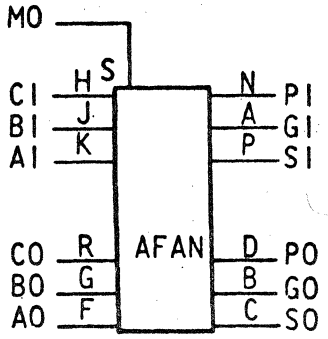
AFAn

Logic Equations:

$$S_n = C_n \cdot (\overline{A}_n \cdot \overline{B}_n + A_n \cdot B_n) + \overline{C}_n \cdot (\overline{A}_n \cdot B_n + A_n \cdot \overline{B}_n)$$

$$G_n = M0 \cdot \overline{A}_n \cdot B_n + \overline{M0} \cdot A_n \cdot B_n$$

$$P_n = M0 \cdot (\overline{A}_n \cdot \overline{B}_n + A_n \cdot B_n) + \overline{M0} \cdot (\overline{A}_n \cdot B_n + A_n \cdot \overline{B}_n)$$



FUNCTIONAL DIAGRAM

AMCN

3.1 CTL Integrated Circuits (Continued)

Element Type:	AMCn
Standard Assembly Number:	1123 9134
Manufacturer's Type:	CTL 9030
Circuit Designation:	8 Bit Memory

Description of Operation:

The AMCn 8 Bit Memory is a semiconductor active memory with 4 words of 2 bits each. Inputs are threshold sensitive and comprise four write lines, four read lines and two data lines. The two data outputs are not restored and represent two levels of degradation. Reading one word is possible, while writing a second word. Also, the same information can be stored into four words simultaneously. Each output must be fully loaded with 3.5 CTuL loads to -2V.

Type of Package: 14 Pin Dual In-line

DC Input Loading @ V_i = -0.7V/2.5V:

I0 I1	Data Inputs	0/1.5 CTL Loads
R0 R1 R2 R3	Read Enable Inputs	0/1.5 CTL Loads
W0 W1 W2 W3	Write Enable Inputs	0/2.5 CTL Loads

DC Output Loading:

Q0 Q1	Data Outputs	No Load

DC Output Drive Capability: 3.5 CTL Loads

DC Output Drive Capability/Package: 7 CTL Loads

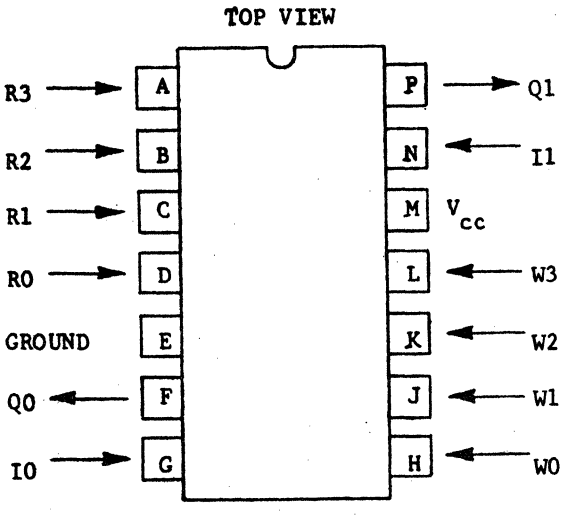
Input Levels Allowed: Levels 0, 1, 2, 3, 4

Output Levels Generated: Level 2

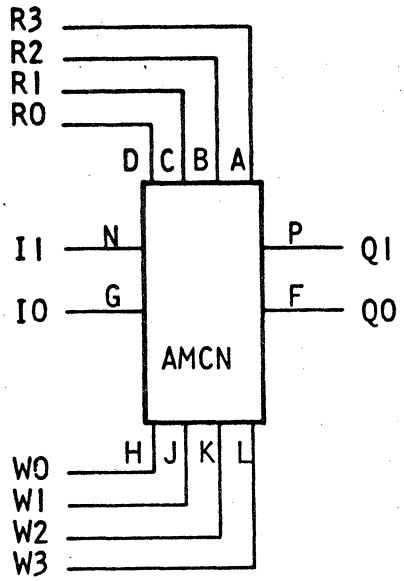
Propagation Delay Times:

Read Access	27 ns
Data Set-up	17 ns
Minimum Write Pulse Width	27 ns

Pin Locations:



AMCn



FUNCTIONAL DIAGRAM

BG-N/BF-N

3.1 CTL Integrated Circuits (Continued)

Element Type:	BF-n/BG-n
Standard Assembly Number:	1705 7563
Manufacturer's Type:	9856
Circuit Designation:	Dual Buffer (2,2)

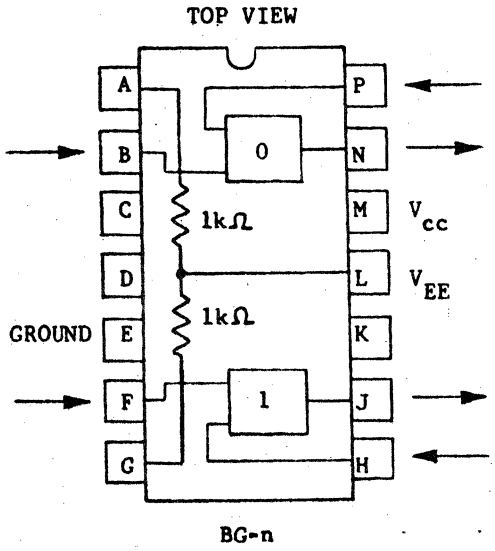
Description of Operation:

Each buffer has two inputs and performs the AND function. All inputs are threshold sensitive and the output level is restored. The package includes two separate resistors connected to V_{EE}, representing 2 CTL loads.

Type of Package:	14 Pin Dual-in-line
DC Input Loading:	0.8 CTL Loads
DC Output Loading:	No Load
DC Output Drive Capability:	24 CTL Loads
DC Output Drive Capability/Package:	48 CTL Loads
Input Levels Allowed:	0, 1, 2, 3, 4
Output Levels Generated:	0
Propagation Delay Times:	10 ns

NOTE: BF-n and BG-n specify the same device. The two names orginated from D/A program options. Currently both designations are equivalent.

Pin Locations:

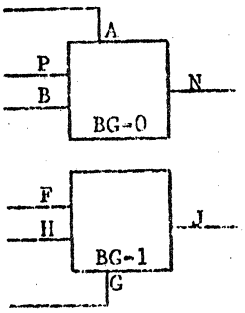


BG-n

Logic Equations:

N = P•B

J = F•H



FUNCTIONAL DIAGRAM

BHAN

3.1 CTL Integrated Circuits (Continued)

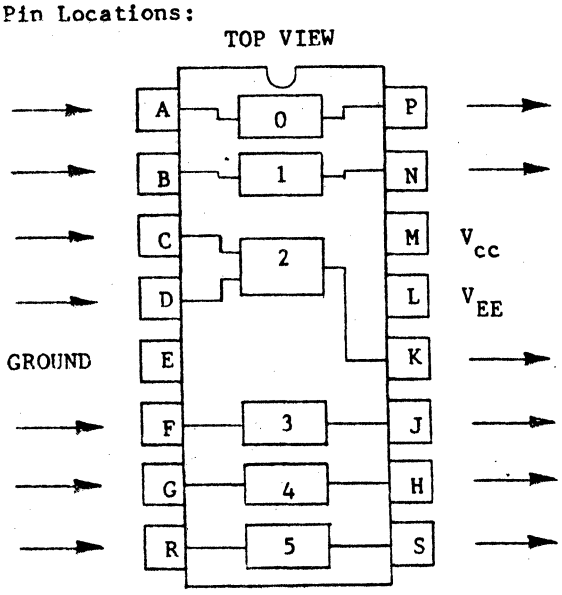
Element Type:	BHAn
Standard Assembly Number:	1904 0245
Manufacturer's Type:	CTL 9816
Circuit Designation:	Hex Restorer

Description of Operation:

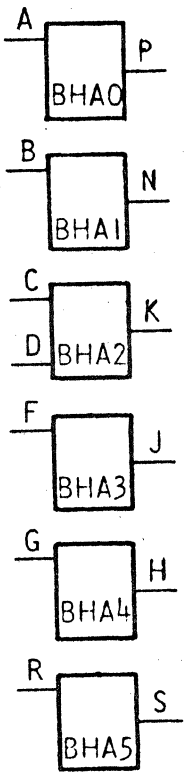
The BHAn Hex Restorer contains six independent circuits in one package. Each circuit is non-inverting and provides a restored output. One of the six circuits has two inputs and produces an "AND" function. All Inputs are threshold sensitive.

Type of Package:	16 Pin Dual In-line
DC Input Loading:	0.8 CTL Loads
DC Output Loading:	No Load (diode to ground)
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	48 CTL Loads
Input Levels Allowed:	Levels 0, 1, 2, 3 or 4
Output Levels Generated:	Level 0
Propagation Delay Times:	12 ns

Pin Locations:



BHAn



FUNCTIONAL DIAGRAM

CFAN

3.1 CTL Integrated Circuits (Continued)

Element Type:	CFAn
Standard Assembly Number:	1904 0195
Manufacturer's Type:	CTL 9824
Circuit Designation:	4 Bit Comparator
Description of Operation:	

The CFAn 4 Bit Comparator performs a parallel comparison of two binary numbers A0,...,A4 and B0,...,B4 where A0, B0 are the least significant and A4, B4 are the most significant bits of the two numbers. The three outputs of the comparator indicate whether A is less than B, equal to B or greater than B. Inputs are threshold sensitive and outputs are restored.

Type of Package:		16 Pin Dual In-line
DC Input Loading:		
A0 A1 A2 A3 A4	Data Input-A	0.8 CTL Loads
B0 B1 B2 B3 B4	Data Input-B	0.8 CTL Loads
DC Output Loading:		
AL AE AG		No Load (diode to ground)
DC Output Drive Capability:		12 CTL Loads
DC Output Drive Capability/Package:		36 CTL Loads
Input Levels Allowed:		Levels 0, 1, 2, 3, 4
Output Levels Generated:		Level 0
Propagation Delay Times:		
Any Input to Any Output		28 ns

Inputs

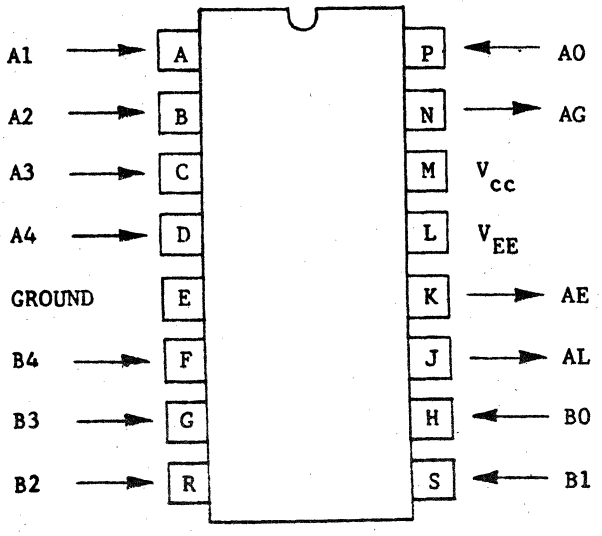
(A0,...,A4)	VS	(B0,...,B4)
A	Equal	B
A	Less Than	B
A	Greater Than	B

Outputs

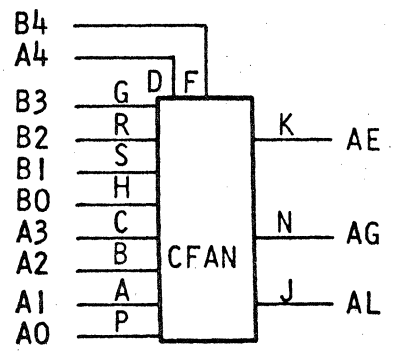
AG	AL	AE
0	0	1
0	1	0
1	0	0

Pin Locations:

TOP VIEW



CFAn



FUNCTIONAL DIAGRAM

CFBN

3.1 CTL Integrated Circuits (Continued)

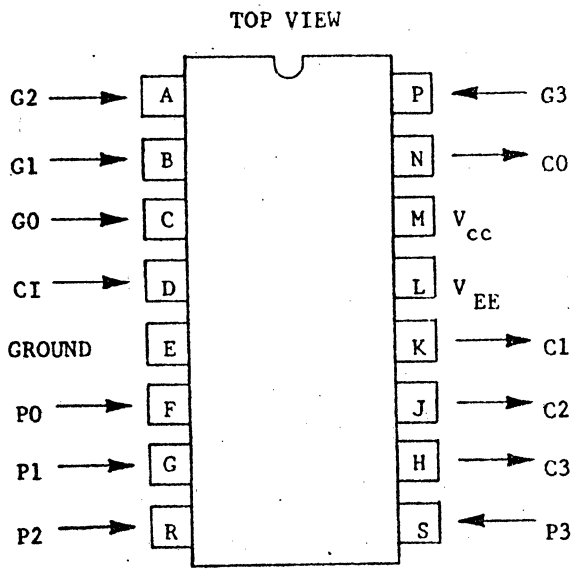
Element Type:	CFBn
Standard Assembly Number:	1909 0513
Manufacturer's Type:	CTL 9823
Circuit Designation:	Carry Logic Gate

Description of Operation:

The CFBn Carry Logic Gate provides the necessary gating for a "high speed" look ahead carry (borrow) for an adder (subtractor) circuit. Each Carry Logic Gate is used in conjunction with a group of four full adder/subtractors. Inputs to the gate are the propagate and generate outputs of the adder/subtractor. Outputs of the gate will be the carry inputs to the adder/subtractor circuits. Inputs are not threshold sensitive and outputs are degraded one offset level below the inputs.

Type of Package:			16 Pin Dual In-line
DC Input Loading:			
	G0 G1 G2 G3	Generate Inputs	1 CTL Load
	P0 P1 P2 P3	Propagate Inputs	1 CTL Load
	CI	Carry Input	1 CTL Load
DC Output Loading:			No Load
DC Output Drive Capability:			12 CTL Loads
DC Output Drive Capability/Package:			48 CTL Loads
Input Levels Allowed:			Levels 0, 1, 2, 3
Output Levels Generated:			Input Level +1
Propagation Delay Times:			6 ns

Pin Locations:



CFBn

Logic Equations:

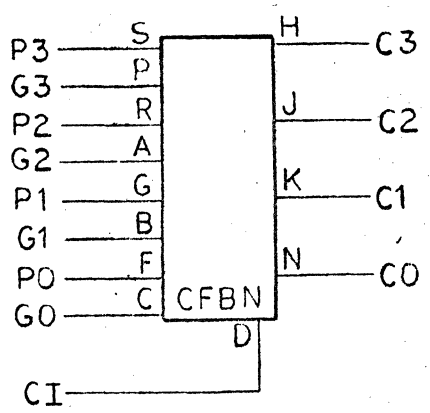
$$C_0 = G_0 + P_0 \cdot C_I$$

$$C_1 = G_1 + P_1 \cdot C_0$$

$$C_2 = G_2 + P_2 \cdot C_1$$

$$C_3 = G_3 + P_3 \cdot (G_2 + P_2 \cdot (G_1 + P_1 \cdot C_0))$$

NOTE: CI does not propogate thru to C3.



FUNCTIONAL DIAGRAM

DFAN

3.1 CTL Integrated Circuits (Continued)

Element Type:	DFAn
Standard Assembly Number:	1904 0161
Manufacturer's Type:	CTL 9838
Circuit Designation:	1 of 8 Decoder

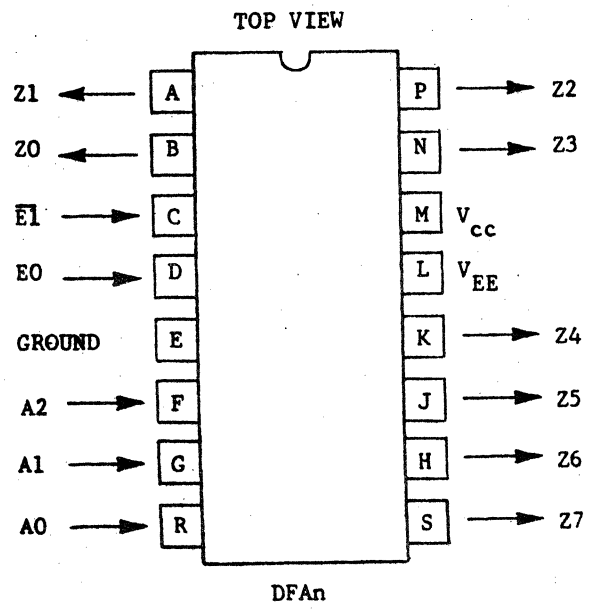
Description of Operation:

The DFAn 1 of 8 Decoder converts a three bit address A0, A1, A2 to one of eight mutually exclusive outputs Z0, ..., Z7. The circuit has an enable line E0 and an inhibit line $\overline{E1}$. Inputs are threshold sensitive and outputs are restored.

Type of Package:		16 Pin Dual In-line
DC Input Loading:		
A0 A1 A2	Address Inputs	0.8 CTL Loads
E0 $\overline{E1}$	Enable, Inhibit	0.8 CTL Loads
DC Output Loading:		
Z0 Z1 Z2 Z3	Decoded Outputs	No Load (diode to ground)
Z4 Z5 Z6 Z7	Decoded Outputs	No Load (diode to ground)
DC Output Drive Capability:		12 CTL Loads
DC Output Drive Capability/Package:		96 CTL Loads
Input Levels Allowed:		Levels 0, 1, 2, 3, 4
Output Levels Generated:		Level 0
Propagation Delay Times:		
Address to Output		12 ns
Enable/Inhibit to Output		12 ns

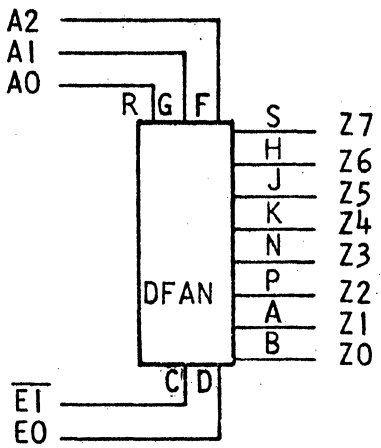
The data inputs (A0, A1, A2) must be stable a minimum of 5ns prior to enabling the decoder if elimination of logic noise is necessary.

Pin Locations:



DFAn Continued

DFAN



FUNCTIONAL DIAGRAM

Truth Table:

Inputs					Outputs							
EO	$\overline{EI}$	A2	A1	A0	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7
1	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0	0
1	0	0	1	1	0	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	1	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	0	0	0	1	0
1	0	1	1	1	0	0	0	0	0	0	0	1
0	X	X	X	X	0	0	0	0	0	0	0	0
X	1	X	X	X	0	0	0	0	0	0	0	0

X = don't care bits - may be 0 or 1.

EFAN

3.1 CTL Integrated Circuits (Continued)

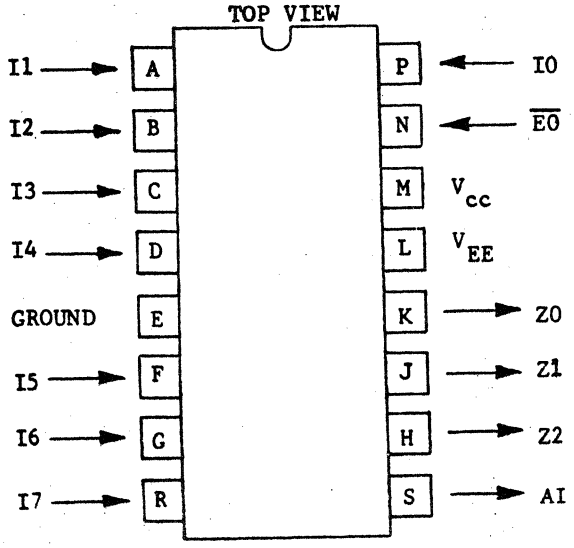
Element Type:	EFAn
Standard Assembly Number:	1914 0748
Manufacturer's Type:	CTL 9883
Circuit Designation:	Priority Encoder

Description of Operation:

The EFAn Priority Encoder is designed to provide a three bit address Z0, Z1 and Z2 which corresponds to the highest priority true input that exists on data inputs I0, ... I7. The circuit has an inhibit line $\overline{EO}$. When the inhibit is true, the address outputs remain at a logical zero. An output AI will be true if any one of the data lines is true. Inputs are threshold sensitive and outputs are restored.

Type of Package:		16 Pin Dual In-line
DC Input Loading:		
I0 I1 I2 I3	Data Inputs	0.8 CTL Loads
I4 I5 I6 I7	Data Inputs	0.8 CTL Loads
$\overline{EO}$	Inhibit Input	0.8 CTL Loads
DC Output Loading:		
Z0 Z1 Z2	Address Outputs	No Load (diode to ground)
AI	Input Indicator	No Load (diode to ground)
DC Output Drive Capability:		12 CTL Loads
DC Output Drive Capability/Package:		48 CTL Loads
Input Levels Allowed:		Levels 0, 1, 2, 3, 4
Output Levels Generated:		Level 0
Propagation Delay Times:		
Input to Address Output		16 ns
Input to AI Output		16 ns
Inhibit to Address Output		16 ns

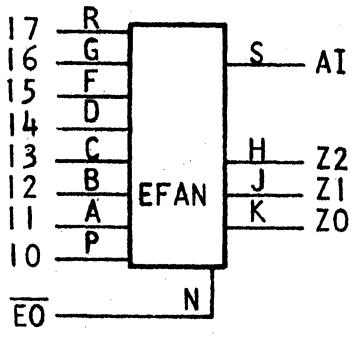
Pin Locations



EFAn

EFAN

EFAn Continued



FUNCTIONAL DIAGRAM

Truth Table:

INPUTS									OUTPUTS			
I7	I6	I5	I4	I3	I2	I1	I0	$\overline{EO}$	AI	Z2	Z1	Z0
X	X	X	X	X	X	X	X	1	*	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	1	X	0	1	0	0	1
0	0	0	0	0	1	X	X	0	1	0	1	0
0	0	0	0	1	X	X	X	0	1	0	1	1
0	0	0	1	X	X	X	X	0	1	1	0	0
0	0	1	X	X	X	X	X	0	1	1	0	1
0	1	X	X	X	X	X	X	0	1	1	1	0
1	X	X	X	X	X	X	X	0	1	1	1	1

X don't care bits - may be 0 or 1.

* AI = I0+I1+I2+I3+I4+I5+I6+I7

FFAN

3.1 CTL Integrated Circuits (Continued)

Element Type:	FFAn
Standard Assembly Number:	1779 6137
Manufacturer's Type:	CTL 9828
Circuit Designation:	Dual JK/D Flip-Flop

Description of Operation:

The FFAn Dual JK/D Flip-Flop contains two storage elements that may be used in the JK or D-set mode depending upon the state of the mode control lines. Each flip-flop has a separate mode control. A false (true) input to the mode control line will enable the JK (D-set) modes of operation. A common clock is provided for the flip-flops. Transition will occur on the negative going edge of the clock. Inputs are threshold sensitive and outputs are restored.

Type of Package: 16 Pin Dual In-line

DC Input Loading:

J0 K0 D0	Data Inputs	0.8 CTL Loads
J1 K1 D1	Data Inputs	0.8 CTL Loads
M0 M1	Mode Control Inputs	0.8 CTL Loads
P0	Clock Inputs	0.8 CTL Loads

DC Output Loading:

Q0 $\overline{Q0}$	F/F Outputs	No Load (diode to ground)
Q1 $\overline{Q1}$	F/F Outputs	No Load (diode to ground)

DC Output Drive Capability: 12 CTL Loads

DC Output Drive Capability/Package: 48 CTL Loads

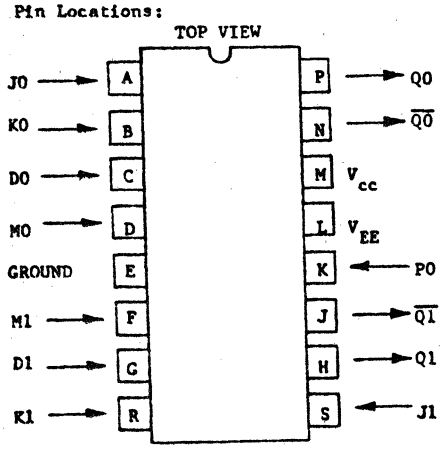
Input Levels Allowed: Except Clock — Levels 0, 1, 2, 3, 4
Clock — Levels 0, 1, 2

Output Levels Generated: Level 0

Propagation Delay Times:

Clock (-) to Output	17 ns
Data Set-up Time	10 ns
JK to D Enable Set-up Time	10 ns
D to JK Enable Set-up Time	10 ns
Minimum Clock Pulse Width	17 ns

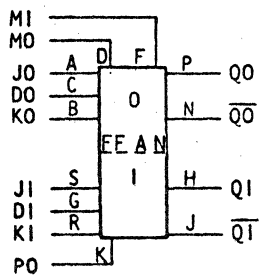
Pin Locations:



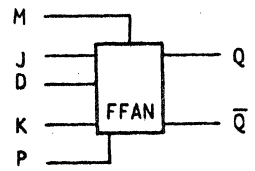
FFAn

Mode Control Logic:

M_n	Mode of Operation
0	JK $(\overline{K}_n \cdot Q_n + J_n \cdot \overline{Q}_n) \rightarrow Q_n$
1	D-Set $D_n \rightarrow Q_n$



FUNCTIONAL DIAGRAM
ENTIRE CHIP



FUNCTIONAL DIAGRAM
ONE DEVICE

When the same single ended outputs of both flip-flops are loaded with more than 3 MSI loads and both outputs can switch simultaneously then both Vcc and Vee must be bypassed with .1 uf within 1.5" of the device (see std ckt section for details).

GFBN

3.1 CTL Integrated Circuits (Continued)

Element Type:	GFBn
Standard Assembly Number:	1916 5851
Manufacturer's Type:	CTL 9854
Circuit Designation:	Dual AND Gates (4,4)
Description of Operation:	

Type of Package:	14-Pin Dual-in-Line
DC Input Loading:	1 CTL Load
DC Output Loading:	1 CTL Load
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	24 CTL Loads
Input Levels Allowed:	0, 1, 2, 3
Output Levels Generated:	Input Level +1
Propagation Delay Times:	6 ns

Because these gates are linear devices, the delay of a cascade of gates is:

n = 1	Td = 6ns
n = 2	Td = 8.5ns
n = 3	Td = 11ns
n = 4	Td = 12ns

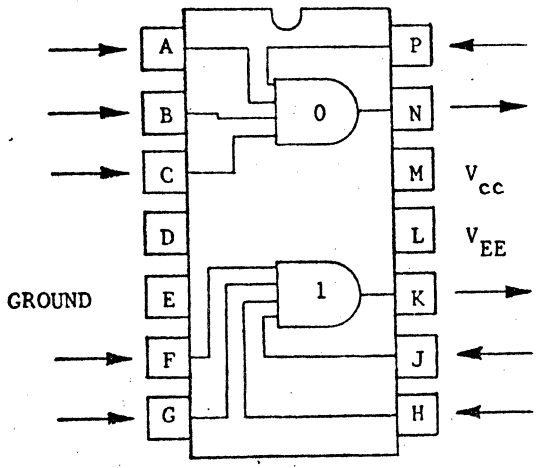
Logic Equations:

N = A•B•C•P

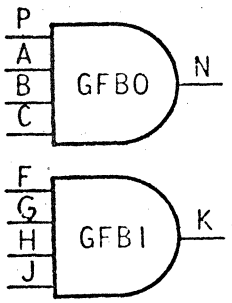
K = F•G•H•J

Pin Locations:

TOP VIEW



GFBn



FUNCTIONAL DIAGRAM

GFEN

3.1 CTL Integrated Circuits (Continued)

Element Type:	GFEn
Standard Assembly Number:	1916 5133
Manufacturer's Type:	CTL 9865
Circuit Designation:	Quad Gates (1,1,1,1)
Description of Operation:	
Type of Package:	14 Pin Dual-in-Line
DC Input Loading:	1 CTL Load
DC Output Loading:	1 CTL Load
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	48 CTL Loads
Input Levels Allowed:	0, 1, 2, 3
Output Levels Generated:	Input Level +1
Propagation Delay Times:	6 ns

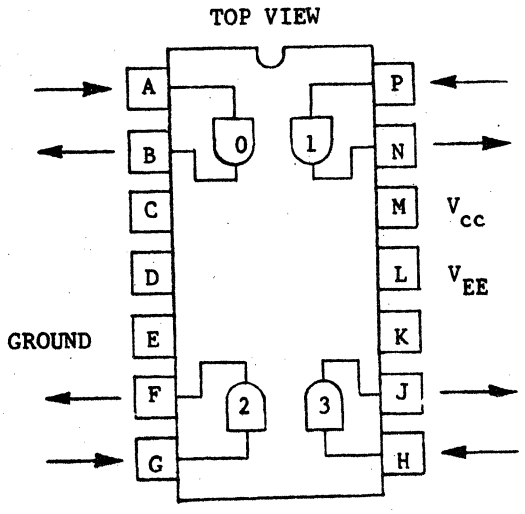
Because these gates are linear devices, the delay of a cascade of gates is:

n = 1	Td = 6ns
n = 2	Td = 8.5ns
n = 3	Td = 11ns
n = 4	Td = 12ns

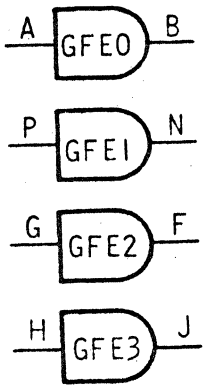
Logic Equations:

B = A
F = G
J = H
N = P

Pin Locations:



GFEn



FUNCTIONAL DIAGRAM

GFFN

3.1 CTL Integrated Circuits (Continued)

Element Type:	GFFn
Standard Assembly Number:	1916 5794
Manufacturer's Type:	CTL 9866
Circuit Function:	Quad AND, AND/OR Gates (2,2,2+2)

Description of Operation:

Two of the AND functions are directly available. The other two are internally wired-OR and the combined function is externally available.

Type of Package:	14 Pin Dual In-line
DC Input Loading:	1 CTL Load
DC Output Loading:	1 CTL Load
DC Output Drive Capability	12 CTL Loads
DC Output Drive Capability/Package:	36 CTL Loads
Input Levels Allowed:	0, 1, 2, 3
Output Levels Generated:	Input Level +1
Propagation Delay Times:	6 ns

Because these gates are linear devices, the delay of a cascade of gates is:

n = 1	Td = 6ns
n = 2	Td = 8.5ns
n = 3	Td = 11ns
n = 4	Td = 12ns

Logic Equations:

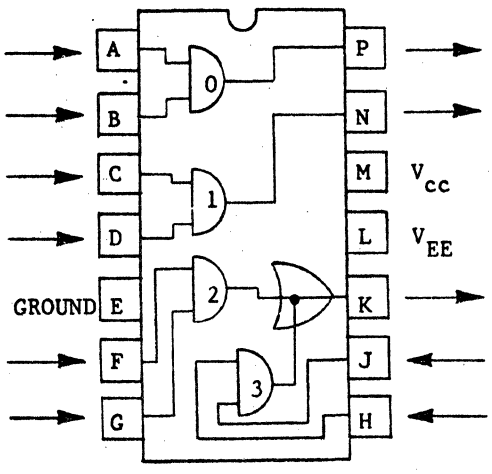
$P = A \cdot B$

$N = C \cdot D$

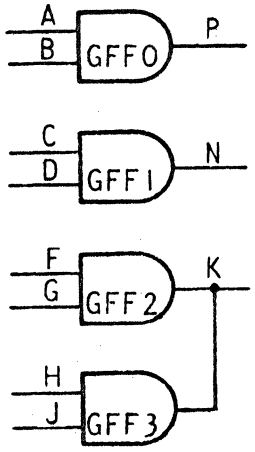
$K = F \cdot G + H \cdot J$

Pin Locations:

TOP VIEW



GFFn



FUNCTIONAL DIAGRAM

GFIN

3.1 CTL Integrated Circuits (Continued)

Element Type:	GFIn
Standard Assembly Number:	1911 9098
Manufacturer's Type:	CTL 9875
Circuit Designation:	Triple AND Gates (4,3,3)
Description of Operation:	
Type of Package:	14 Pin Dual-in-Line
DC Input Loading:	1 CTL Load
DC Output Loading:	1 CTL Load
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	36 CTL Loads
Input Levels Allowed:	0, 1, 2, 3
Output Levels Generated:	Input Level +1
Propagation Delay Times:	6 ns

Because these gates are linear devices, the delay of a cascade of gates is:

n = 1	Td = 6ns
n = 2	Td = 8.5ns
n = 3	Td = 11ns
n = 4	Td = 12ns

Logic Equations:

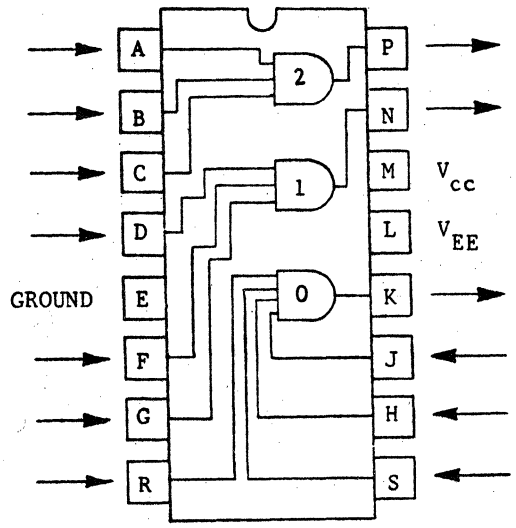
P = A•B•C
N = D•F•G
K = R•S•H•J

AND GATE 4, 3, 3

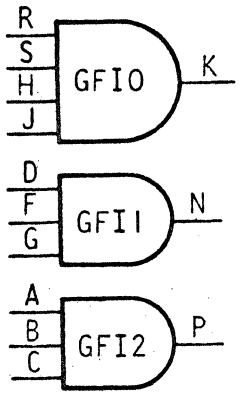
CTL 9875 GFIN

Pin Locations:

TOP VIEW



GFIn



FUNCTIONAL DIAGRAM

GFJN OR GLJN *

3.1 CTL Integrated Circuits (Continued)

Element Type:	GFJn
Standard Assembly Number:	1911 9106
Manufacturer's Type:	CTL 9874
Circuit Designation:	Quad AND Gates (3,2,2,2)
Description of Operation:	

Type of Package:	16 Pin Dual-in-Line
DC Input Loading:	1 CTL Load
DC Output Loading:	1 CTL Load
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	48 CTL Loads
Input Levels Allowed:	0, 1, 2, 3
Output Levels Generated:	Input Level+1
Propagation Delay Times:	6 ns

Because these gates are linear devices, the delay of a cascade of gates is:

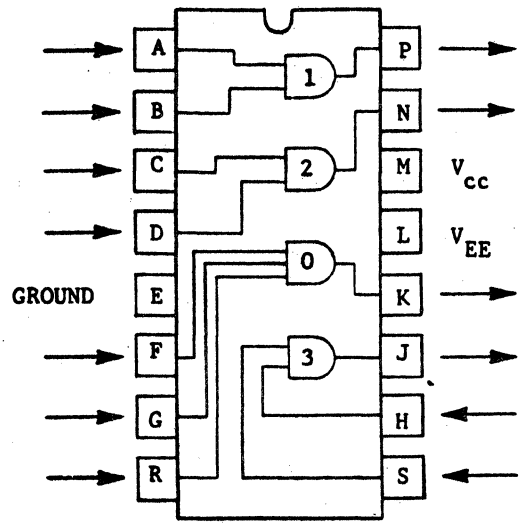
n = 1	Td = 6ns
n = 2	Td = 8.5ns
n = 3	Td = 11ns
n = 4	Td = 12ns

Logic Equations:

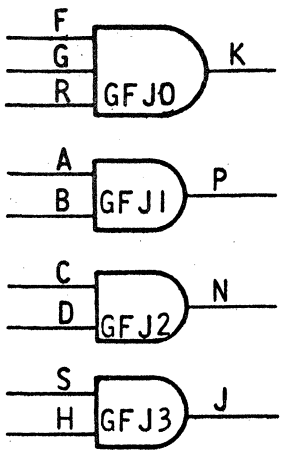
P = A·B
N = C·D
K = F·G·R
J = H·S

Pin Locations:

TOP VIEW



GFJn



FUNCTIONAL DIAGRAM

* GFJN is the preferred current designation for this chip and should be used. GLJN originally implied use of the chip as a black box (for DA processing), now no longer the case. Both designations currently yield exactly the same results through DA processing.

GFKN

3.1 CTL Integrated Circuits (Continued)

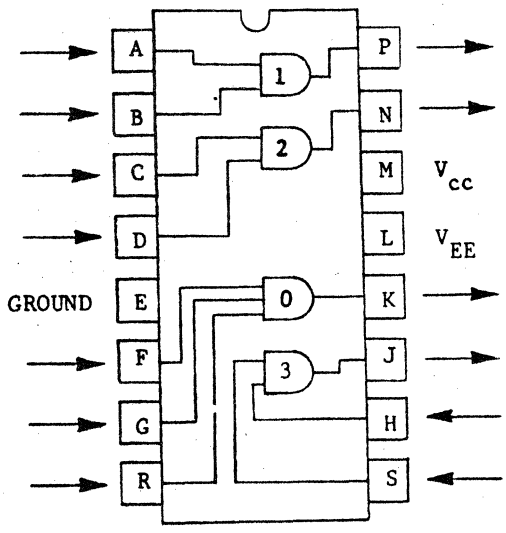
Element Type:	**GFKn**
Standard Assembly Number:	1918 4282
Manufacturer's Type:	CTL 9863
Circuit Designation:	Quad AND Gates (3,2,2,2)
Description of Operation:	
Type of Package:	16 Pin Dual-in-Line
DC Input Loading:	No Load
DC Output Loading:	No Load
DC Output Drive Capability:	12 CTL loads
DC Output Drive Capability/Package:	48 CTL loads
Input Levels Allowed:	0, 1, 2, 3
Output Levels Generated:	Input Level +1
Propagation Delay Times:	6 ns

Because these gates are linear devices, the delay of a cascade of gates is:

n = 1	Td = 6ns
n = 2	Td = 8.5ns
n = 3	Td = 11ns
n = 4	Td = 12ns

Pin Locations:

TOP VIEW



GFKn

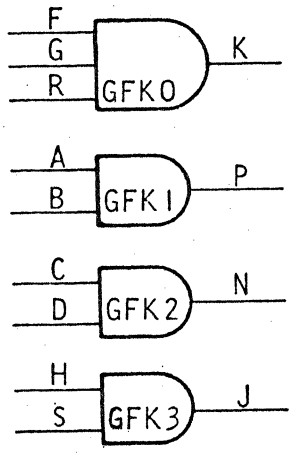
Logic Equations:

P = A•B

N = C•D

K = F•G•R

J = H•S



FUNCTIONAL DIAGRAM

IF-N

3.1 CTL Integrated Circuits (Continued)

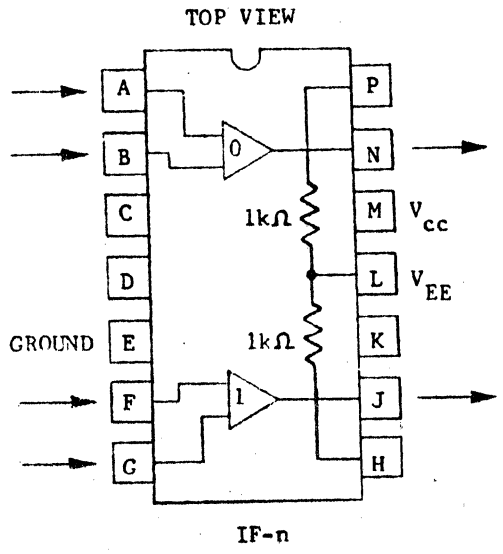
Element Type:	IF-n
Standard Assembly Number:	1705 7480
Manufacturer's Type:	CTL 9852
Circuit Designation:	Dual Inverter (2,2)

Description of Operation:

Each inverter has two inputs and performs the NOR function. All inputs are threshold sensitive and the output level is restored. The package includes two separate resistors connected to V_{EE}, each representing 2 CTL loads.

Type of Package:	14 Pin Dual-in-Line
DC Input Loading:	0.8 CTL Loads
DC Output Loading:	1 CTL Load
DC Output Drive Capability:	24 CTL Loads
DC Output Drive Capability/Package:	48 CTL Loads
Input Levels Allowed:	0, 1, 2, 3, 4
Output Levels Generated:	0
Propagation Delay Times:	12nS Fan out of 12
	15nS Fan out of 24

Pin Locations:

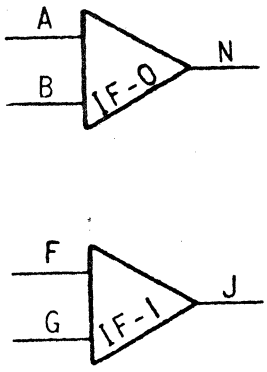


IF-n

Logic Equations:

$$N = \overline{A + B}$$

$$J = \overline{F + G}$$



FUNCTIONAL DIAGRAM

IHAN

3.1 CTL Integrated Circuits (Continued)

Element Type:	IHAn
Standard Assembly Number:	1904 0252
Manufacturer's Type:	CTL 9806
Circuit Designation:	Hex Inverter

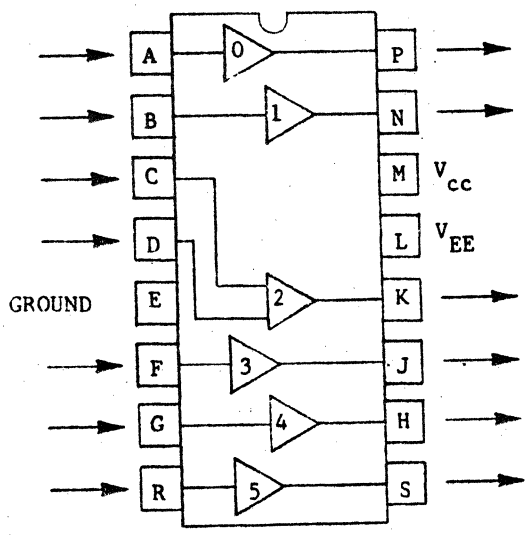
Description of Operation:

The IHAn Hex Inverter contains six inverting circuits in one package. One of the six circuits has two inputs and produces a "NOR" function. Inputs are threshold sensitive and outputs are restored.

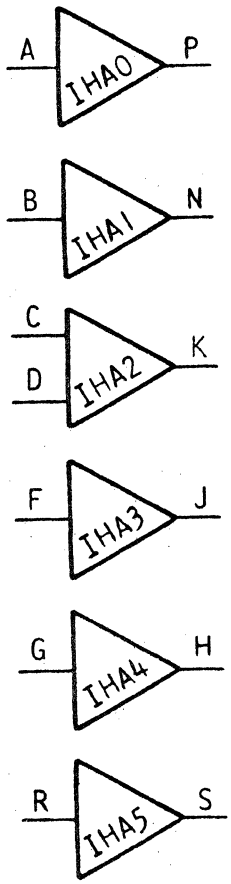
Type of Package:	16 Pin Dual In-line
DC Input Loading:	0.8 CTL Loads
DC Output Loading:	No Load (diode to ground)
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	48 CTL Loads
Input Levels Allowed:	Levels 0, 1, 2, 3, 4
Output Levels Generated:	Level 0
Propagation Delay Times:	12 ns

Pin Locations:

TOP VIEW



IHAn



FUNCTIONAL DIAGRAM

LFAN

3.1 CTL Integrated Circuits (Continued)

Element Type: LFAn
Standard Assembly Number: 1779 6145
Manufacturer's Type: CTL 9834
Circuit Designation: Quad Latch
Description of Operation:

The LFAn Quad Latch contains four storage elements with common mode control lines M0 and M1. Four modes of operation are possible. These are: 1) No Action: 2) Bit Set; 3) Clear; and 4) D-Set. The circuit has two clock inputs, P0 and P1. Transition between logic states will take place on the positive going edge of the "AND" function for the two clock inputs. A common read enable line E0 allows an interrogation of the device states. E0 false will render the output false.

Type of Package: 16 Pin Dual In-line

DC Input Loading:

I0 I1 I2 I3	Data Inputs	0.8 CTL Loads
M0 M1	Mode Control Inputs	0.8 CTL Loads
P0 P1	Clock Inputs	0.8 CTL Loads
E0	Read Enable Input	0.8 CTL Loads

DC Output Loading:

Q0 Q1 Q2 Q3	Latch Outputs	No Load (diode to ground)

DC Output Drive Capability: 12 CTL Loads

DC Output Drive Capability/Package: 48 CTL Loads

Input Levels Allowed:

Data Inputs I0, I1, I2, I3	Levels 0, 1, 2, 3, 4
Mode Controls M0, M1	Levels 0
Clock Inputs P0, P1,	Level 0
Read Enable	Levels 0, 1, 2, 3

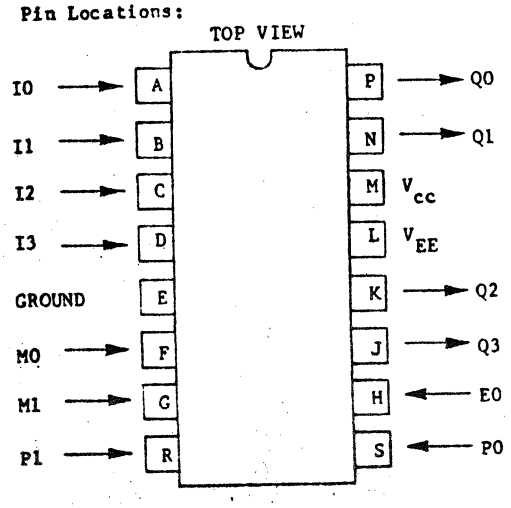
NOTE: Clock and Mode Control input lines must be restored externally to avoid "notch" problems.

Output Levels Generated: Level 0

Propagation Delay Times:

Data to Output	22 ns
Mode Controls to Output	22 ns
Clock (+) to Output	22 ns
Read Enable to Output	12 ns
Data & Mode Control Set-up Time	12 ns
Minimum Clock Pulse Width	17 ns

Pin Locations:



MFAN

3.1 CTL Integrated Circuits (Continued)

Element Type:	MFAn
Standard Assembly Number:	1904 0187
Manufactuer's Type:	**CTL 9881**
Circuit Designation:	8-Input Multiplexer

Description of Operation:

The 8-input multiplexer contains fully on-chip binary decoding data selection. The Enable input performs the enabling function for the chip.

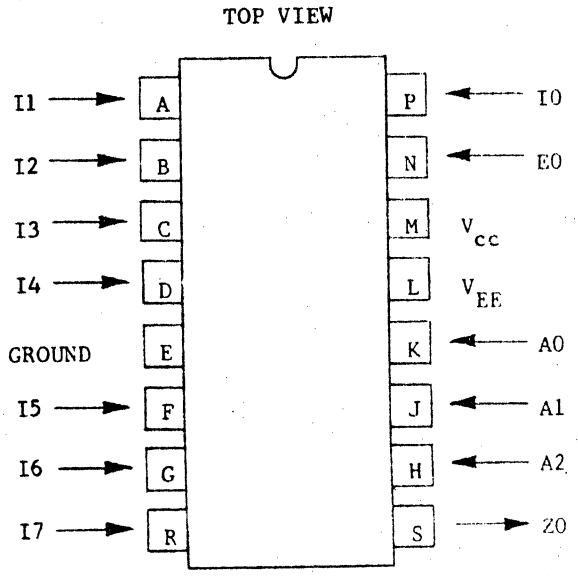
Type of Package:	16 Pin Dual In-Line
DC Input Loading:	
I0 I1 I2 I3 Data Inputs	0.8 CTL Loads
I4 I5 I6 I7 Data Inputs	0.8 CTL Loads
A0 A1 A2 E0 Address/Enable	0.8 CTL Load
DC Output Loading:	No Load (Diode connected to ground)
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	12 CTL Loads
Input Levels Allowed:	0, 1, 2, 3, 4
Output Levels Generated:	0
Propagation Delay Times:	
Data to Output	16 ns
Address to Output	20 ns
Enable to Output	16 ns

The data and address inputs must be stable a minimum of 5ns prior to enabling the multiplexor for eliminating inputs logic noise effects.

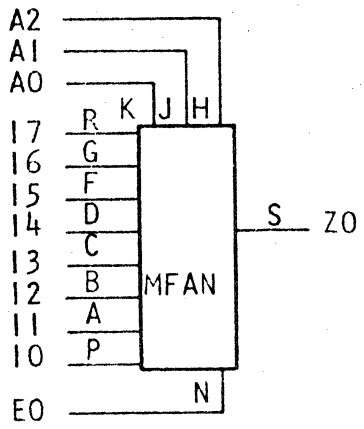
Logic Equations:

$$Z_0 = (I_0 \cdot \bar{A}_0 \cdot \bar{A}_1 \cdot \bar{A}_2 + I_1 \cdot A_0 \cdot \bar{A}_1 \cdot \bar{A}_2 + I_2 \cdot \bar{A}_0 \cdot A_1 \cdot \bar{A}_2 + I_3 \cdot A_0 \cdot A_1 \cdot \bar{A}_2 + I_4 \cdot \bar{A}_0 \cdot \bar{A}_1 \cdot A_2 + I_5 \cdot A_0 \cdot \bar{A}_1 \cdot A_2 + I_6 \cdot \bar{A}_0 \cdot A_1 \cdot A_2 + I_7 \cdot A_0 \cdot A_1 \cdot A_2) \cdot E0$$

Pin Locations:



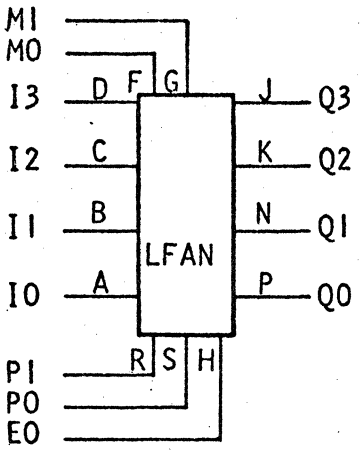
MFAn



FUNCTIONAL DIAGRAM

LFAN

3.1 CTL Integrated Circuits (Continued)



FUNCTIONAL DIAGRAM

Mode Control Logic:

M1	M0	Modes of Operation	
0	0	No Action	$Q_n \rightarrow Q_n$
0	1	Bit Set	$(I_n+Q_n) \rightarrow Q_n$
1	0	Clear	$0 \rightarrow Q_n$
1	1	D-Set	$I_n \rightarrow Q_n$

NOTE: 1. When the circuit is in the Bit Set mode during the clock pulse, the latch traps the true input and does not change state again.

Operation of the LFAn Quad Latch during the D-Set mode will be as follows:

a) After both clock lines become true, the output On will follow the inputs In.

b) After 1 or both clocks become false, the output will remain latched in that state which occurred immediately prior to the negative transition of the clock (S).

TIME t							TIME (t+1)
E0	P0	P1	M0	M1	I	Q	Q
1	0	0	X	X	X	1	1
1	0	0	X	X	X	0	0
1	1	1	0	0	X	1	1
1	1	1	0	0	X	0	0
1	1	1	1	0	0	1	1
1	1	1	1	0	0	0	0
1	1	1	0	1	X	X	0
1	1	1	1	0	1	X	1
1	1	1	1	1	0	X	0
1	1	1	1	1	1	X	1

$$Q_i\ (t+1) = (P0 \cdot P1 \cdot M0 \cdot Ii + Qi \cdot \bar{M}1 + Qi \cdot \overline{P0 \cdot P1})$$

$$i = 0, 1, 2, 3$$

NOTE: It is suggested that the mode lines be steady a mode control set-up time before the positive edge of the clock and held till the trailing edge with the hold time = 0nS. This is important if the stored data is important otherwise the mode controls may be changed during the positive clock time. If the mode lines are changed during the positive clock the previously stored data will be lost.

MOPN

3.1 CTL Integrated Circuits (Continued)

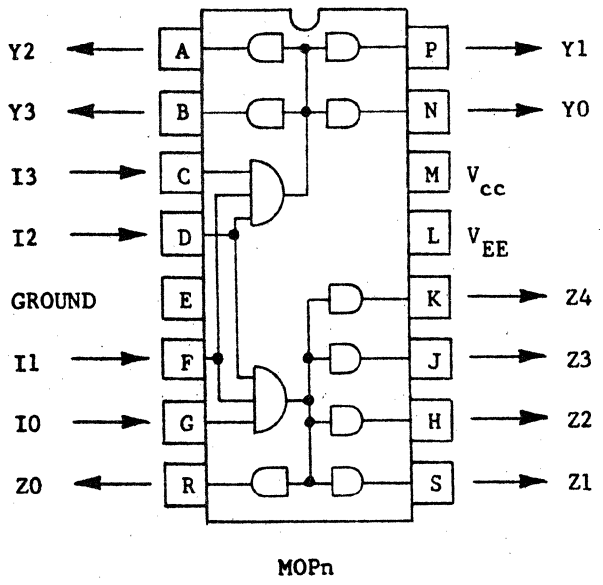
Element Type:	MOPn
Standard Assembly Number:	1916 6115
Manufacturer's Type:	CTL 9877
Circuit Designation:	Micro-operator

Description of Operation:

The MOPn Micro-operator is a special circuit consisting of two 3 input AND gates and several isolated outputs per gate. The Micro-operator has four inputs I0, I1, I2 and I3. One AND gate has five isolated outputs (inputs are I0, I1 and I2) while the second AND gate has four isolated outputs (inputs are I1, I2 and I3). Inputs are threshold sensitive and outputs are restored.

Type of Package:	16 Pin Dual In-line
DC Input Loading:	
I0 I1 I2 I3	No Load
DC Output Loading:	
Y0 Y1 Y2 Y3	No Load (diode to ground)
Z0 Z1 Z2 Z3 Z4	No Load (diode to ground)
DC Output Drive Capability:	12 CTL Loads
DC Output Drive Capability/Package:	60 CTL Loads
Input Levels Allowed:	Levels 0, 1, 2, 3, 4
Output Levels Generated:	Level 0
Propagation Delay Times:	14 ns

Pin Locations:

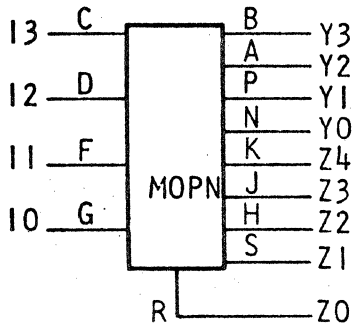


MOPn

Logic Equations:

Y0 = I1·I2·I3
Y1 = I1·I2·I3
Y2 = I1·I2·I3
Y3 = I1·I2·I3

Z0 = I0·I1·I2
Z1 = I0·I1·I2
Z2 = I0·I1·I2
Z3 = I0·I1·I2
Z4 = I0·I1·I2



FUNCTIONAL DIAGRAM

RFAN

3.1 CTL Integrated Circuits (Continued)

Element Type:	RFAn
Standard Assembly Number:	2201 4096
Manufacturer's Type:	3405
Circuit Designation:	3 Bit Register
Description of Operation:	

The RFAN 3 Bit Register consists of three storage elements (Flip-Flops) together with the necessary internal gating to perform several logical operations depending upon the states of three mode control lines MO, M1 and M2. The functions available are: 1) No Action; 2) Bit Reset 3) D-Set; 4) Bit Set; 5) Binary Addition; 6) Binary Subtraction; 7) Shift Up; and 8) Shift Down. The circuit also has a synchronous reset line RO. The QO, Q1 and Q2 transitions will occur on the negative going edge of the clock PO. The carry output during addition and subtraction is asynchronous, and is valid a maximum of 24 ns after the inputs are stable. CI and CO are synchronous when shifting. The inputs are not fully threshold sensitive. Outputs are restored.

The carry output of a chip should not be fedback into the inputs of the same chip.

Type of Package: 16 Pin Dual In-Line

DC Input Loading @ V_i = -0.7V/2.5V

I0 I1 I2	Data Inputs	0.4/0.8 CTL Loads
CI	Carry In	0.4/0.8 CTL Loads
CO	Carry Out	0.4/0.8 CTL Loads
MO M1 M2	Mode Control Inputs	0.4/0.8 CTL Loads
PO RO	Clock, Clear Inputs	0.4/0.8 CTL Loads

DC Output Loading:

QO Q1 Q2	Register Outputs	No Load (diode to ground)
CI	Carry In	0.4/0.8 @ V_o = -0.7V/2.5V
CO	Carry Out	No Load

DC Drive Capability:

QO Q1 Q2	Register Outputs	12 CTL Loads
CI CO	Carry In, Carry Out	8 CTL Loads

DC Drive Capability/Package:

QO Q1 Q2	Register Outputs	36 CTL Loads
CI CO	Carry In, Carry Out	16 CTL Loads

Input Levels Allowed:

I0 I1 I2	Data Inputs	Levels 0, 1, 2
CI,CO	Carry In, Carry Out	Levels 0, 1, 2
MO M1 M2	Mode Control Inputs	Level 0, 1, 2
PO	Clock	Level 0, 1, 2
RO	Clear Input	Levels 0, 1, 2

Output Levels Generated:

QO Q1 Q2	Register Outputs	Level 0
CI CO	Carry In, Carry Out	Level 1 (Not Input +1)

RFAN

3.1 CTL Integrated Circuits (Continued)

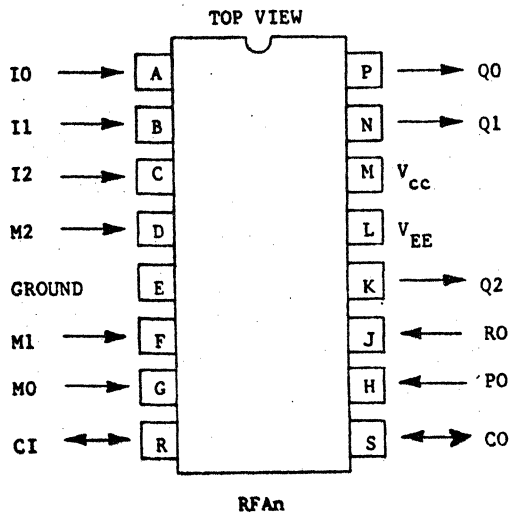
Propagation Delay Times:

Clock (-) to Output	21 ns
Clock (-) to CO	39 ns
Clock (-) to CI	39 ns
Carry In to Carry Out	24 ns
Mode Control to CO	38 ns
Data Set-up Time (Add & Subtract)	24 ns
Data Set-up Time (other modes)	11 ns
Clear Set-up Time	17 ns
Mode Control Set-up Time	28 ns
Data, Mode and Clear Hold Times	6 ns
Minimum Clock Pulse Width	17 ns*

* Clock Pulses less than this minimum may cause loss of stored data (even in "NO-ACTION" mode).

RFAN

Pin Locations:



Mode Control Logic:

M2	M1	M0	Modes of Operation
0	0	0	No Action $Q_n \rightarrow Q_n$
0	0	1	Bit Reset $(I_n + \overline{Q}_n) \rightarrow \overline{Q}_n$
0	1	0	D-Set $I_n \rightarrow Q_n$
0	1	1	Bit Set $(I_n + Q_n) \rightarrow Q_n$
1	0	0	Add (See Below)
1	0	1	Subtract (See Below)
1	1	0	Shift Up $C_i \rightarrow Q_0 \rightarrow Q_1 \rightarrow Q_2 = C_o$
1	1	1	Shift Down $C_0 \rightarrow Q_2 \rightarrow Q_1 \rightarrow Q_0 = C_i$

ADD The bits I0, I1 and I2 are added to Q0, Q1 and Q2, and the result will replace Q0, Q1 and Q2. CI is the carry input and CO the carry output. I0 and Q0 are the least significant bits.

SUBTRACT The bits I0, I1 and I2 are subtracted from Q0, Q1 and Q2 and the result will replace Q0, Q1 and Q2. Ci is the borrow input and CO is the borrow output. I0 and Q0 are the least significant bits.

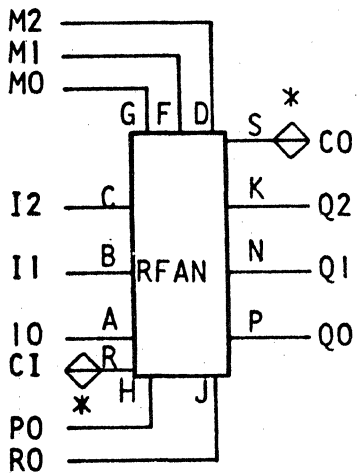
RFAN

RFAN Continued :

M2	M1	M0	In	Qn(t)	Qn(t+1)	FUNCTION	
0	0	0	X	0	0	NO ACTION	Jn=0,Kn=0
			X	1	1		
0	0	1	0	0	0	BIT RESET	Jn=0,Kn=In
			0	1	1		
			1	X	0		
0	1	0	0	X	0	D-SET	Qn ← In
			1	X	1		
0	1	1	0	0	0	BIT SET	Jn=In, Kn=0
1	0	0				ADD: Qn+In+CI Qn(t+1) ← SUM CO = CARRY OUTPUT	
1	0	1				SUBTRACT: Qn-In and Ci is BORROW INPUT Qn(t+1) ← DIFFERENCE CO = BORROW OUTPUT	
1	1	0				SHIFT UP: CO=Q2 ← Q2←Q1←Q0←Ci	
1	1	1				SHIFT DOWN: CO→Q2→Q1→Q0, Ci=Q0	

3) The Carry Input Ci and Carry Output CO are Bidirectional lines.

4) The Clear Operation (Line RO) is synchronous and absolute; it overrides any concurrent Mode Control.



FUNCTIONAL DIAGRAM

RFBN

3.1 CTL Integrated Circuits (Continued)

Element Type:	RFBn
Standard Assembly Number:	2201 4062
Manufacturer's Type:	3406.
Circuit Designation:	4 Bit Register

Description of Operation:

The RFBn 4 Bit Register contains four storage elements supplied with the proper gating circuitry, to perform several logical operations depending upon the state of the mode control lines M0, M1, and M2. The possible modes of operation are: 1) Bit Set; 2) D-Set; 3) Complement and 4) Shift Up. The clear operation (Line R0) is synchronous and absolute, it overides any concurrent Mode Control. Transitions of the storage elements will occur on the negative going edge of the clock pulse. Inputs I0, I1, I2, and I3 are fully threshold sensitive, while the mode lines M0, M1, and M2; the clock P0; and clear R0 have wider threshold regions. Outputs of the 4 Bit Register will be restored.

Type of Package: 16 Pin Dual In-line

DC Input @ V_i = -.7V/2.5V:

I0 I1 I2 I3	Data Inputs	0.4/0.8 CTL Loads
M0 M1 M2	Mode Control Inputs	0.4/0.8 CTL Loads
P0 R0	Clock, Clear Inputs	0.4/0.8 CTL Loads

DC Output Loading:

Q0 Q1 Q2 Q3	Register Outputs	No Load (diode to ground)

DC Output Drive Capability: 12 CTL Loads

DC Output Drive Capability/Package: 48 CTL Loads

Input Levels Allowed:

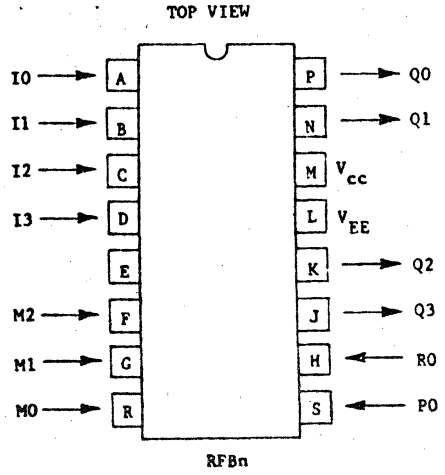
I0 I1 I2 I3	Data Inputs	Levels 0, 1, 2, 3, 4
M0 M1 M2 M3	Mode Control Inputs	Levels 0, 1, 2
P0	Clock Input	Level 0
R0	Clear Input	Levels 0, 1

Output Levels Generated: Level 0

Propagation Delay Times:

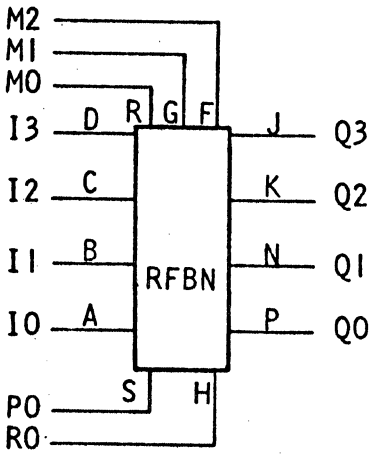
Clock (-) to Output	21 ns
Data Set-up Time	6 ns
Clear Set-up Time	19 ns
Mode Control Set-up Time	28 ns
Data, Mode and Clear Hold Times	7 ns
Minimum Clock Pulse Width	20 ns

Pin Locations:



RFBN Continued:

RFBN



FUNCTIONAL DIAGRAM

Mode Control Logic:

M2	M1	M0	Modes of Operation
0	0	0	Bit Set (In+Qn)→Qn
0	0	1	D-Set In→Qn
0	1	0	Complement In⊕Qn→Qn
0	1	1	Not Defined
1	0	0	Shift Up I0→Q0→Q1→Q2→Q3
1	0	1	Not Defined
1	1	0	Not Defined
1	1	1	Not Defined

The undefined mode control combinations should never exist while the 4 Bit Register is being clocked.

The set-up and hold time requirements between any data input and the clock input must be observed in all modes of operation, i.e, even for cases where the device is previously preset to a state that changes in the data input should not cause any output change. An example is input data changing from high to low with the device output already set to high and mode controls at D-Set.

RFZN

3.1 CTL Integrated Circuits (Continued)

Element Type:	RFZN
Standard Assembly Number:	1779 6152
Manufacturer's Type:	9843
Circuit Designation:	3 Bit Register
Description of Operation:	

The RFZN is a CTL III 3-bit register. Its operation is exactly identical to that of the RFAN. Refer to page 25 of this Section for details of usage.

RF-N

3.1 CTL Integrated Circuits (Continued)

Element Type:	RF-N
Standard Assembly Number:	1779 6160
Manufacturer's Type:	9844
Circuit Designation:	4 Bit Register
Description of Operation:	

The RF-N is a CTL III 4-bit register. Its operation is exactly identical to that of the RF8N. Refer to page 28 of this Section for details.

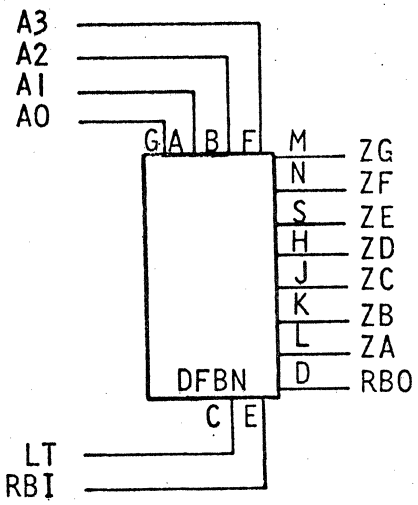
3.2 TTL/DTL INTEGRATED CIRCUITS

Element Type:
Standard Assembly No:
Manufacturer/Manufacturer's Type:
Circuit Designation:

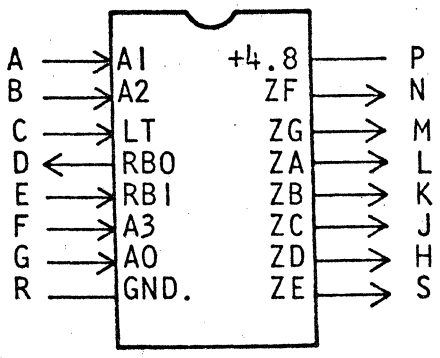
Description of Operation:

DFBN

DFBN
2205 8242
Fairchild U6B930759X
Seven Segment Decoder



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM
16 PIN DIP

(7) TRUTH TABLE

INPUTS						OUTPUT							
LT	RBI	A3	A2	A1	A0	ZA	ZB	ZC	ZD	ZE	ZF	ZG	RBO
0	X	X	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	1	1	1	1	1	1	0	1
1	X	0	0	0	1	0	1	1	0	0	0	0	1
1	X	0	0	1	0	1	1	0	1	1	0	1	1
1	X	0	0	1	1	1	1	1	1	0	0	1	1
1	X	0	1	0	0	0	1	1	0	0	0	1	1
1	X	0	1	0	1	1	0	1	1	0	1	1	1
1	X	0	1	1	0	1	0	1	1	1	1	1	1
1	X	0	1	1	1	1	1	1	0	0	0	0	1
1	X	1	0	0	0	1	1	1	1	1	1	1	1
1	X	1	0	0	1	1	1	1	1	0	1	1	1
1	X	1	0	1	0	0	0	0	1	1	0	1	1
1	X	1	0	1	1	0	0	0	1	0	0	1	1
1	X	1	1	0	0	0	1	1	0	0	1	1	1
1	X	1	1	0	1	1	0	1	1	0	1	1	1
1	X	1	1	1	0	0	0	0	1	1	1	1	1
1	X	1	1	1	1	0	0	0	0	0	0	0	1

X: Don't care bits

DFBN

TTL 9307

SEVEN SEGMENT DECODER

(1) The device is a T^2L compatible logic circuit. It accepts 4-bit BCD 8421 code input and produces appropriate outputs for selection of segments in a seven segment matrix display.

(2) The BCD code input is applied to four address inputs (A0 thru A3). The outputs for segment selection (ZA thru ZG) will be true according to the truth table given below.

(3) Two additional inputs provide facilities for lamp test (LT) and ripple blanking (RBI). A ripple blanking output is also available (RBO). The proper interconnection of RBI and RBO in multidigit displays allows for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number.

(4) To interface the Seven Segment decoder with CTL logic, consult Section 5.

(5) The Seven Segment Decoder drives Fairchild FND 10, Single Digit Numeric Display. A 500Ω pull-up resistor to the +4.75v supply is required.

(6) Propagation delay td = 550ns max.

1024-BIT READ ONLY MEMORY

3.2 TTL/DTL Integrated Circuits

ELEMENT	TYPE	PART NO.	FUNCTION	
MI1N		1918 3599	EBD1C/ASCII	(MSB)
MI2N		1918 3607	EBCD1C/ASCII	(LSB)
MI3N		1918 3615	ASCII/EBC1C	(MSB)
MI4N		1918 3623	ASCII/EBCD1C	(LSB)
MH1N		2201 4146	HOLLERITH/EBCD1C	(LSB)
MH2N		2201 4153	HOLLERITH/EBCD1C	(MSB)
MH3N		2201 4161	EBCD1C/HOLLER1TH	(LSB)
MH4N		2201 4179	EBCD1C/HOLLER1TH	(MSB)
MJ1N		2204 4200	96 COL CODE/EBCD1C	(LSB)
MJ2N		2204 4218	96 COL CODE/EBCD1C	(MSB)
MJ3N		2204 4226	EBCD1C/96 COL CODE	(LSB)
MJ4N		2204 4234	EBCD1C/96 COL CODE	(MSB)
MK1N		2204 5124	EBCD1C/BCL + PAR	(LSB)
MK2N		2204 5132	EBCD1C/BCL + PAR	(MSB)
RM1N		2208 0014	EBCD1C/KATAKANA	(LSB)
RM2N		2208 0022	EBCD1C/KATAKANA	(MSB)

1024-BIT READ ONLY MEMORY

3.2 TTL/DTL Integrated Circuits

Element Type: TTL
Circuit Designation: 1024 Bit ROM
Description of Operation:

(1) The circuit is a T^2L logic compatible Read Only Memory organized as 256 words of 4 bits each. The memory has 8 address lines A0 thru A7, Enable inputs $\overline{C1}$ and $\overline{C2}$, and 4 outputs O1 thru O4. This device is used for code conversion.

(2) Logical false levels applied simultaneously at the two Enable inputs are needed to enable the chip, otherwise the chip is disabled and a true voltage is forced at all outputs.

(3) Information on how to interface this device is contained in Section 5.

(4) The memory outputs can be tied together to perform a wired and function (positive logic).

(5) Both inputs and outputs are shown in the bit code format tables using Binary "1" to represent a true voltage level and Binary "0" to represent a false voltage level.

(6) The codes of the following ROMs are inverted and, therefore, the outputs must be fed through inverters to obtain the true code translation:

Inverting Output ROM s

RM1N	MK1N	MI1N
RM2N	MK2N	MI2N
		MI3N
		MI4N

However, the codes of the following ROMs are not inverted, and code translation is obtained directly.

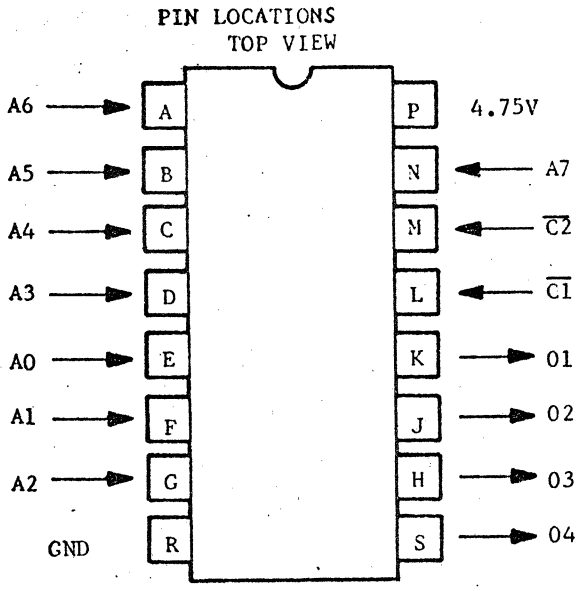
Non Inverting Output ROM s

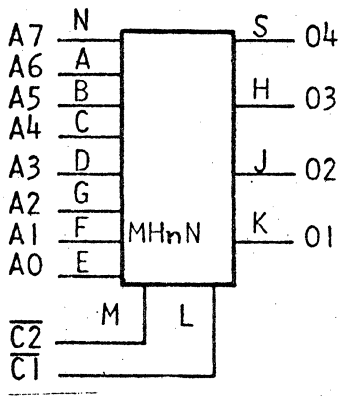
MH1N	MJ1N
MH2N	MJ2N
MH3N	MJ3N
MH4N	MJ4N

1024 BIT READ ONLY MEMORY

3.2 TTL/DTL Integrated Circuits

Type of Package:		16 Pin Dual In-line
DC Input Loading:		
A0 A1 A2 A3	Address Inputs	-1.6 mA/0.04 mA
A4 A5 A6 A7	Address Inputs	@V_i = 0.45V/
$\overline{C1}$ $\overline{C2}$	Memory Enable Inputs	
Output Drive Capability:		
01 02 03 04	ROM Outputs	15 mA @ V_O = 0.45V
Output Leakage Current:		-0.10 mA @ V_O = 5.25V
Type of Output:		Open Collector
Interfacing:		Refer to TTL/CTL Interfacing Rules
Propagation Delay Times:		
Address to Output		60 ns
Memory Enable to Output		40 ns





FUNCTIONAL DIAGRAM

MI1N

1024-BIT READ ONLY MEMORY

MI1N EBCDIC TO ASCII CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	7	40	D	60	D	80	3
01	F	21	7	41	5	61	D	81	9
02	F	22	7	42	5	62	4	82	9
03	F	23	7	43	5	63	4	83	9
04	6	24	7	44	5	64	4	84	9
05	F	25	F	45	5	65	4	85	9
06	7	26	E	46	5	66	4	86	9
07	8	27	E	47	5	67	4	87	9
08	6	28	7	48	5	68	4	88	9
09	7	29	7	49	5	69	4	89	9
0A	7	2A	7	4A	A	6A	8	8A	3
0B	F	2B	7	4B	D	6B	D	8B	3
0C	F	2C	7	4C	C	6C	D	8C	3
0D	F	2D	F	4D	D	6D	A	8D	3
0E	F	2E	F	4E	D	6E	C	8E	3
0F	F	2F	F	4F	D	6F	C	8F	3
10	E	30	6	50	D	70	4	90	3
11	E	31	6	51	5	71	4	91	9
12	E	32	E	52	5	72	4	92	9
13	E	33	6	53	5	73	4	93	9
14	6	34	6	54	5	74	4	94	9
15	7	35	6	55	5	75	4	95	9
16	F	36	6	56	5	76	3	96	9
17	7	37	F	57	5	77	3	97	8
18	E	38	6	58	4	78	3	98	8
19	E	39	6	59	4	79	9	99	8
1A	6	3A	6	5A	A	7A	C	9A	3
1B	7	3B	6	5B	D	7B	D	9B	3
1C	E	3C	E	5C	D	7C	B	9C	3
1D	E	3D	E	5D	D	7D	D	9D	3
1E	E	3E	6	5E	C	7E	C	9E	3
1F	E	3F	E	5F	A	7F	D	9F	2

MI1N

1024-BIT READ ONLY MEMORY

MI1N EBCDIC TO ASCII CODE FORMAT (CON'T.):

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	2	B3	2	C6	B	DB	1	EE	0
A1	8	B4	2	C7	B	DC	0	EF	0
A2	8	B5	2	C8	B	DD	0	F0	C
A3	8	B6	2	C9	B	DE	0	F1	C
A4	8	B7	2	CA	1	DF	0	F2	C
A5	8	B8	1	CB	1	E0	A	F3	C
A6	8	B9	1	CC	1	E1	6	F4	C
A7	8	BA	1	CD	1	E2	A	F5	C
A8	8	BB	1	CE	1	E3	A	F6	C
A9	8	BC	1	CF	1	E4	A	F7	C
AA	2	BD	1	D0	8	E5	A	F8	C
AB	2	BE	1	D1	B	E6	A	F9	C
AC	2	BF	1	D2	B	E7	A	FA	0
AD	2	C0	8	D3	B	E8	A	FB	0
AE	2	C1	B	D4	B	E9	A	FC	0
AF	2	C2	B	D5	B	EA	0	FD	0
B0	2	C3	B	D6	B	EB	0	FE	0
B1	2	C4	B	D7	A	EC	0	FF	0
B2	2	C5	B	D8	A	ED	0		
				D9	A				
				DA	1				

NOTE:

1). Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MI2N

1024-BIT READ ONLY MEMORY

MI2N EBCDIC TO ASCII CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	F	40	F	60	2	80	C
01	E	21	E	41	F	61	0	81	E
02	D	22	D	42	E	62	D	82	D
03	C	23	C	43	D	63	C	83	C
04	3	24	B	44	C	64	B	84	B
05	6	25	5	45	B	65	A	85	A
06	9	26	8	46	A	66	9	86	9
07	0	27	4	47	9	67	8	87	8
08	8	28	7	48	8	68	7	88	7
09	2	29	6	49	7	69	6	89	6
0A	1	2A	5	4A	4	6A	3	8A	B
0B	4	2B	4	4B	1	6B	3	8B	A
0C	3	2C	3	4C	3	6C	A	8C	9
0D	2	2D	A	4D	7	6D	0	8D	8
0E	1	2E	9	4E	4	6E	1	8E	7
0F	0	2F	8	4F	E	6F	0	8F	6
10	F	30	F	50	9	70	5	90	5
11	E	31	E	51	6	71	4	91	5
12	D	32	9	52	5	72	3	92	4
13	C	33	C	53	4	73	2	93	3
14	2	34	B	54	3	74	1	94	2
15	A	35	A	55	2	75	0	95	1
16	7	36	9	56	1	76	F	96	0
17	8	37	B	57	0	77	E	97	F
18	7	38	7	58	F	78	D	98	E
19	6	39	6	59	E	79	F	99	D
1A	D	3A	5	5A	2	7A	5	9A	4
1B	0	3B	4	5B	B	7B	C	9B	3
1C	3	3C	B	5C	5	7C	F	9C	2
1D	2	3D	A	5D	6	7D	8	9D	1
1E	1	3E	1	5E	4	7E	2	9E	0
1F	0	3F	5	5F	1	7F	D	9F	F

MI2N

1024-BIT READ ONLY MEMORY

MI2N EBCDIC TO ASCII CODE FORMAT (CON'T.)

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	E	B3	4	C6	9	DB	0	EE	7
A1	1	B4	3	C7	8	DC	F	EF	6
A2	C	B5	2	C8	7	DD	E	F0	F
A3	B	B6	1	C9	6	DE	D	F1	E
A4	A	B7	0	CA	7	DF	C	F2	D
A5	9	B8	F	CB	6	E0	3	F3	C
A6	8	B9	E	CC	5	E1	0	F4	B
A7	7	BA	D	CD	4	E2	C	F5	A
A8	6	BB	C	CE	3	E3	B	F6	9
A9	5	BC	B	CF	2	E4	A	F7	8
AA	D	BD	A	D0	2	E5	9	F8	7
AB	C	BE	9	D1	5	E6	8	F9	6
AC	B	BF	8	D2	4	E7	7	FA	5
AD	A	C0	4	D3	3	E8	6	FB	4
AE	9	C1	E	D4	2	E9	5	FC	3
AF	8	C2	D	D5	1	EA	B	FD	2
B0	7	C3	C	D6	0	EB	A	FE	1
B1	6	C4	B	D7	F	EC	9	FF	0
B2	5	C5	A	D8	E	ED	8		
				D9	D				
				DA	1				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000
1 = 0001
2 = 0010
3 = 0011
4 = 0100
5 = 0101
6 = 0110
7 = 0111
8 = 1000
9 = 1001
A = 1010
B = 1011
C = 1100
D = 1101
E = 1110
F = 1111

MI3N

1024-BIT READ ONLY MEMORY

MI3N ASCII TO EBCDIC CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	B	40	8	60	8	80	D
01	F	21	B	41	3	61	7	81	D
02	F	22	8	42	3	62	7	82	D
03	F	23	8	43	3	63	7	83	D
04	C	24	A	44	3	64	7	84	D
05	D	25	9	45	3	65	7	85	E
06	D	26	A	46	3	66	7	86	F
07	D	27	8	47	3	67	7	87	E
08	E	28	B	48	3	68	7	88	D
09	F	29	A	49	3	69	7	89	D
0A	D	2A	A	4A	2	6A	6	8A	D
0B	F	2B	B	4B	2	6B	6	8B	D
0C	F	2C	9	4C	2	6C	6	8C	D
0D	F	2D	9	4D	2	6D	6	8D	F
0E	F	2E	B	4E	2	6E	6	8E	F
0F	F	2F	9	4F	2	6F	6	8F	E
10	E	30	0	50	2	70	6	90	C
11	E	31	0	51	2	71	6	91	C
12	E	32	0	52	2	72	6	92	E
13	E	33	0	53	1	73	5	93	C
14	C	34	0	54	1	74	5	94	C
15	C	35	0	55	1	75	5	95	C
16	C	36	0	56	1	76	5	96	C
17	D	37	0	57	1	77	5	97	F
18	E	38	0	58	1	78	5	98	C
19	E	39	0	59	1	79	5	99	C
1A	C	3A	8	5A	1	7A	5	9A	C
1B	D	3B	A	5B	B	7B	3	9B	C
1C	E	3C	B	5C	1	7C	9	9C	F
1D	E	3D	8	5D	A	7D	2	9D	E
1E	E	3E	9	5E	A	7E	5	9E	C
1F	E	3F	9	5F	9	7F	F	9F	1

MI3N

1024-BIT READ ONLY MEMORY

MI3N ASCII TO EBCDIC CODE FORMAT (CON'T.)

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	B	B3	9	C6	7	DB	4	EE	2
A1	B	B4	9	C7	7	DC	4	EF	2
A2	B	B5	9	C8	7	DD	4	F0	2
A3	B	B6	9	C9	7	DE	4	F1	2
A4	B	B7	9	CA	6	DF	4	F2	2
A5	B	B8	9	CB	6	E0	4	F3	2
A6	B	B9	9	CC	6	E1	4	F4	1
A7	B	BA	8	CD	6	E2	4	F5	1
A8	B	BB	8	CE	6	E3	4	F6	1
A9	A	BC	8	CF	6	E4	4	F7	1
AA	A	BD	8	D0	6	E5	4	F8	1
AB	A	BE	8	D1	5	E6	4	F9	1
AC	A	BF	8	D2	5	E7	4	FA	0
AD	A	C0	8	D3	5	E8	3	FB	0
AE	A	C1	8	D4	5	E9	3	FC	0
AF	A	C2	8	D5	5	EA	3	FD	0
B0	A	C3	7	D6	5	EB	3	FE	0
B1	A	C4	7	D7	5	EC	3	FF	0
B2	9	C5	7	D8	4	ED	3		
				D9	4				
				DA	4				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MI4N
1024-BIT READ ONLY MEMORY

MI4N ASCII TO EBCDIC CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	F	40	3	60	6	80	F
01	E	21	0	41	E	61	E	81	E
02	D	22	0	42	D	62	D	82	D
03	C	23	4	43	C	63	C	83	C
04	8	24	4	44	B	64	B	84	B
05	2	25	3	45	A	65	A	85	A
06	1	26	F	46	9	66	9	86	9
07	0	27	2	47	8	67	8	87	8
08	9	28	2	48	7	68	7	88	7
09	A	29	2	49	6	69	6	89	6
0A	A	2A	3	4A	E	6A	E	8A	5
0B	4	2B	1	4B	D	6B	D	8B	4
0C	3	2C	4	4C	C	6C	C	8C	3
0D	2	2D	F	4D	B	6D	B	8D	6
0E	1	2E	4	4E	A	6E	A	8E	5
0F	0	2F	E	4F	9	6F	9	8F	4
10	F	30	F	50	8	70	8	90	F
11	E	31	E	51	7	71	7	91	E
12	D	32	D	52	6	72	6	92	5
13	C	33	C	53	D	73	D	93	C
14	3	34	B	54	C	74	C	94	B
15	2	35	A	55	B	75	B	95	A
16	D	36	9	56	A	76	A	96	9
17	9	37	8	57	9	77	9	97	7
18	7	38	7	58	8	78	8	98	7
19	6	39	6	59	7	79	7	99	6
1A	0	3A	5	5A	6	7A	6	9A	5
1B	8	3B	1	5B	5	7B	F	9B	4
1C	3	3C	3	5C	F	7C	5	9C	B
1D	2	3D	1	5D	5	7D	F	9D	B
1E	1	3E	1	5E	0	7E	E	9E	1
1F	0	3F	0	5F	2	7F	8	9F	E

MI4N
1024-BIT READ ONLY MEMORY

MI4N ASCII TO EBCDIC CODE FORMAT (CON'T.)

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	E	B3	C	C6	3	DB	C	EE	5
A1	D	B4	B	C7	2	DC	B	EF	4
A2	C	B5	A	C8	1	DD	A	F0	3
A3	B	B6	9	C9	0	DE	9	F1	2
A4	A	B7	8	CA	F	DF	8	F2	1
A5	9	B8	7	CB	5	E0	7	F3	0
A6	8	B9	6	CC	4	E1	6	F4	5
A7	7	BA	F	CD	3	E2	5	F5	4
A8	6	BB	E	CE	2	E3	4	F6	3
A9	E	BC	D	CF	1	E4	3	F7	2
AA	D	BD	C	D0	0	E5	2	F8	1
AB	C	BE	B	D1	F	E6	1	F9	0
AC	B	BF	A	D2	5	E7	0	FA	5
AD	A	C0	9	D3	4	E8	5	FB	4
AE	9	C1	8	D4	3	E9	4	FC	3
AF	8	C2	7	D5	2	EA	3	FD	2
B0	7	C3	F	D6	1	EB	2	FE	1
B1	6	C4	5	D7	0	EC	1	FF	0
B2	D	C5	4	D8	F	ED	0		
				D9	E				
				DA	D				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MH1N

1024-BIT READ ONLY MEMORY

MH1N HOLLERITH TO EBCDIC LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	0	20	0	40	0	60	0	80	0
01	1	21	1	41	1	61	1	81	1
02	2	22	2	42	2	62	2	82	2
03	3	23	3	43	3	63	3	83	3
04	4	24	4	44	4	64	4	84	4
05	5	25	5	45	5	65	5	85	5
06	6	26	6	46	6	66	6	86	6
07	7	27	7	47	7	67	7	87	7
08	8	28	8	48	8	68	8	88	8
09	9	29	9	49	9	69	0	89	9
0A	A	2A	0	4A	A	6A	A	8A	A
0B	B	2B	B	4B	B	6B	B	8B	B
0C	C	2C	C	4C	C	6C	C	8C	C
0D	D	2D	D	4D	D	6D	D	8D	D
0E	E	2E	E	4E	E	6E	E	8E	E
0F	F	2F	F	4F	F	6F	F	8F	F
10	9	30	9	50	9	70	9	90	9
11	1	31	1	51	1	71	1	91	1
12	2	32	2	52	2	72	2	92	2
13	3	33	3	53	3	73	3	93	3
14	4	34	4	54	4	74	4	94	4
15	5	35	5	55	5	75	5	95	5
16	6	36	6	56	6	76	6	96	6
17	7	37	7	57	7	77	7	97	7
18	8	38	8	58	8	78	8	98	8
19	9	39	9	59	9	79	0	99	9
1A	A	3A	A	5A	A	7A	A	9A	A
1B	B	3B	B	5B	B	7B	B	9B	B
1C	C	3C	C	5C	C	7C	C	9C	C
1D	D	3D	D	5D	D	7D	D	9D	D
1E	E	3E	E	5E	E	7E	E	9E	E
1F	F	3F	F	5F	F	7F	F	9F	F

MH1N

1024-BIT READ ONLY MEMORY

MH1N HOLLERITH TO EBCDIC LSB CODE FORMAT

HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT
A0	0	B3	3	C6	6	DB	B	EE	E
A1	1	B4	4	C7	7	DC	C	EF	F
A2	2	B5	5	C8	8	DD	D	F0	9
A3	3	B6	6	C9	0	DE	E	F1	1
A4	4	B7	7	CA	A	DF	F	F2	2
A5	5	B8	8	CB	B	E0	0	F3	3
A6	6	B9	0	CC	C	E1	1	F4	4
A7	7	BA	A	CD	D	E2	2	F5	5
A8	8	BB	B	CE	E	E3	3	F6	6
A9	0	BC	C	CF	F	E4	4	F7	7
AA	A	BD	D	D0	9	E5	5	F8	8
AB	B	BE	E	D1	1	E6	6	F9	0
AC	C	BF	F	D2	2	E7	7	FA	A
AD	D	C0	A	D3	3	E8	8	FB	B
AE	E	C1	1	D4	4	E9	0	FC	C
AF	F	C2	2	D5	5	EA	A	FD	D
B0	9	C3	3	D6	6	EB	B	FE	E
B1	1	C4	4	D7	7	EC	C	FF	F
B2	2	C5	5	D8	8	ED	D		
				D9	0				
				DA	A				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MH2N

1024-BIT READ ONLY MEMORY

MH2N HOLLERITH TO EBCDIC MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	4	20	F	40	6	60	D	80	5
01	F	21	6	41	D	61	A	81	C
02	F	22	E	42	D	62	A	82	C
03	F	23	E	43	D	63	A	83	C
04	F	24	E	44	D	64	A	84	C
05	F	25	E	45	D	65	A	85	C
06	F	26	E	46	D	66	A	86	C
07	F	27	E	47	D	67	A	87	C
08	F	28	E	48	D	68	A	88	C
09	7	29	6	49	5	69	A	89	4
0A	7	2A	E	4A	5	6A	A	8A	4
0B	7	2B	6	4B	5	6B	A	8B	4
0C	7	2C	6	4C	5	6C	A	8C	4
0D	7	2D	6	4D	5	6D	A	8D	4
0E	7	2E	6	4E	5	6E	A	8E	4
0F	7	2F	6	4F	5	6F	A	8F	4
10	F	30	E	50	D	70	A	90	C
11	3	31	2	51	1	71	E	91	0
12	3	32	2	52	1	72	6	92	0
13	3	33	2	53	1	73	6	93	0
14	3	34	2	54	1	74	6	94	0
15	3	35	2	55	1	75	6	95	0
16	3	36	2	56	1	76	6	96	0
17	3	37	2	57	1	77	6	97	0
18	3	38	2	58	1	78	6	98	0
19	3	39	2	59	1	79	2	99	0
1A	3	3A	2	5A	1	7A	E	9A	0
1B	3	3B	2	5B	1	7B	E	9B	0
1C	3	3C	2	5C	1	7C	E	9C	0
1D	3	3D	2	5D	1	7D	E	9D	0
1E	3	3E	2	5E	1	7E	E	9E	0
1F	3	3F	2	5F	1	7F	E	9F	0

MH2N

1024-BIT READ ONLY MEMORY

MH2N HOLLERITH TO EBCDIC MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	C	B3	4	C6	9	DB	D	EE	B
A1	8	B4	4	C7	9	DC	D	EF	B
A2	8	B5	4	C8	9	DD	D	F0	B
A3	8	B6	4	C9	9	DE	D	F1	7
A4	8	B7	4	CA	9	DF	D	F2	7
A5	8	B8	4	CB	9	E0	7	F3	7
A6	8	B9	0	CC	9	E1	B	F4	7
A7	8	BA	C	CD	9	E2	B	F5	7
A8	8	BB	C	CE	9	E3	B	F6	7
A9	8	BC	C	CF	9	E4	B	F7	7
AA	8	BD	C	D0	9	E5	B	F8	7
AB	8	BE	C	D1	5	E6	B	F9	3
AC	8	BF	C	D2	5	E7	B	FA	F
AD	8	C0	6	D3	5	E8	B	FB	F
AE	8	C1	9	D4	5	E9	B	FC	F
AF	8	C2	9	D5	5	EA	B	FD	F
B0	8	C3	9	D6	5	EB	B	FE	F
B1	4	C4	9	D7	5	EC	B	FF	F
B2	4	C5	9	D8	5	ED	B		
				D9	1				
				DA	0				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MH3N

1024-BIT READ ONLY MEMORY

MH3N EBCDIC TO HOLLERITH LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	9	20	9	40	0	60	0	80	9
01	1	21	1	41	1	61	1	81	1
02	2	22	2	42	2	62	2	82	2
03	3	23	3	43	3	63	3	83	3
04	4	24	4	44	4	64	4	84	4
05	5	25	5	45	5	65	5	85	5
06	6	26	6	46	6	66	6	86	6
07	7	27	7	47	7	67	/	87	7
08	8	28	8	48	8	68	8	88	8
09	9	29	9	49	9	69	9	89	0
0A	A	2A	A	4A	A	6A	0	8A	A
0B	B	2B	B	4B	B	6B	B	8B	B
0C	C	2C	C	4C	C	6C	C	8C	C
0D	D	2D	D	4D	D	6D	D	8D	D
0E	E	2E	E	4E	E	6E	E	8E	E
0F	F	2F	F	4F	F	6F	F	8F	F
10	9	30	9	50	0	70	0	90	9
11	1	31	1	51	1	71	1	91	1
12	2	32	2	52	2	72	2	92	2
13	3	33	3	53	3	73	3	93	3
14	4	34	4	54	4	74	4	94	4
15	5	35	5	55	5	75	5	95	5
16	6	36	6	56	6	76	6	96	6
17	7	37	7	57	7	77	7	97	7
18	8	38	8	58	8	78	8	98	8
19	9	39	9	59	9	79	9	99	0
1A	A	3A	A	5A	A	7A	A	9A	A
1B	B	3B	B	5B	B	7B	B	9B	B
1C	C	3C	C	5C	C	7C	C	9C	C
1D	D	3D	D	5D	D	7D	D	9D	D
1E	E	3E	E	5E	E	7E	E	9E	E
1F	F	3F	F	5F	F	7F	F	9F	F

MH3N

1024-BIT READ ONLY MEMORY

MH3N EBCDIC TO HOLLERITH LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	9	B3	3	C6	6	DB	B	EE	E
A1	1	B4	4	C7	7	DC	C	EF	F
A2	2	B5	5	C8	8	DD	D	F0	0
A3	3	B6	6	C9	0	DE	E	F1	1
A4	4	B7	7	CA	A	DF	F	F2	2
A5	5	B8	8	CB	B	E0	A	F3	3
A6	6	B9	0	CC	C	E1	1	F4	4
A7	7	BA	A	CD	D	E2	2	F5	5
A8	8	BB	B	CE	E	E3	3	F6	6
A9	0	BC	C	CF	F	E4	4	F7	7
AA	A	BD	D	D0	0	E5	5	F8	8
AB	B	BE	E	D1	1	E6	6	F9	0
AC	C	BF	F	D2	2	E7	7	FA	A
AD	D	C0	0	D3	3	E8	8	FB	B
AE	E	C1	1	D4	4	E9	0	FC	C
AF	F	C2	2	D5	5	EA	A	FD	D
B0	9	C3	3	D6	6	EB	B	EE	E
B1	1	C4	4	D7	7	EC	C	FF	F
B2	2	C5	5	D8	8	ED	D		
				D9	0				
				DA	A				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MH4N

1024-BIT READ ONLY MEMORY

MH4N EBCDIC TO HOLLERITH MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	B	20	7	40	0	60	4	80	A
01	9	21	3	41	B	61	2	81	A
02	9	22	3	42	B	62	7	82	A
03	9	23	3	43	B	63	7	83	A
04	9	24	3	44	B	64	7	84	A
05	9	25	3	45	B	65	7	85	A
06	9	26	3	46	B	66	7	86	A
07	9	27	3	47	B	67	7	87	A
08	9	28	3	48	B	68	7	88	A
09	9	29	3	49	8	69	2	89	B
0A	9	2A	3	4A	8	6A	C	8A	A
0B	9	2B	3	4B	8	6B	2	8B	A
0C	9	2C	3	4C	8	6C	2	8C	A
0D	9	2D	3	4D	8	6D	2	8D	A
0E	9	2E	3	4E	8	6E	2	8E	A
0F	9	2F	3	4F	8	6F	2	8F	A
10	D	30	F	50	8	70	E	90	C
11	5	31	1	51	D	71	F	91	C
12	5	32	1	52	D	72	F	92	C
13	5	33	1	53	D	73	F	93	C
14	5	34	1	54	D	74	F	94	C
15	5	35	1	55	D	75	F	95	C
16	5	36	1	56	D	76	F	96	C
17	5	37	1	57	D	77	F	97	C
18	5	38	1	58	D	78	F	98	C
19	5	39	1	59	4	79	0	99	D
1A	5	3A	1	5A	4	7A	0	9A	C
1B	5	3B	1	5B	4	7B	0	9B	C
1C	5	3C	1	5C	4	7C	0	9C	C
1D	5	3D	1	5D	4	7D	0	9D	C
1E	5	3E	1	5E	4	7E	0	9E	C
1F	5	3F	1	5F	4	7F	0	9F	C

MH4N

1024-BIT READ ONLY MEMORY

MH4N EBCDIC TO HOLLERITH MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	6	B3	E	C6	8	DB	D	EE	7
A1	6	B4	E	C7	8	DC	D	EF	7
A2	6	B5	E	C8	8	DD	D	F0	2
A3	6	B6	E	C9	9	DE	D	F1	0
A4	6	B7	E	CA	B	DF	D	F2	0
A5	6	B8	E	CB	B	E0	2	F3	0
A6	6	B9	F	CC	B	E1	7	F4	0
A7	6	BA	E	CD	B	E2	2	F5	0
A8	6	BB	E	CE	B	E3	2	F6	0
A9	7	BC	E	CF	B	E4	2	F7	0
AA	6	BD	E	D0	6	E5	2	F8	0
AB	6	BE	E	D1	4	E6	2	F9	1
AC	6	BF	E	D2	4	E7	2	FA	F
AD	6	C0	A	D3	4	E8	2	FB	F
AE	6	C1	8	D4	4	E9	3	FC	F
AF	6	C2	8	D5	4	EA	7	FD	F
B0	E	C3	8	D6	4	EB	7	FE	F
B1	E	C4	8	D7	4	EC	7	FF	F
B2	E	C5	8	D8	4	ED	7		
				D9	5				
				DA	D				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MJ1N

1024-BIT READ ONLY MEMORY

MJ1N 96 COL CODE TO EBCDIC LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	0	20	0	40	0	60	0	80	0
01	1	21	1	41	1	61	1	81	1
02	2	22	2	42	2	62	2	82	2
03	3	23	3	43	3	63	3	83	3
04	4	24	4	44	4	64	4	84	4
05	5	25	5	45	5	65	5	85	5
06	6	26	6	46	6	66	6	86	6
07	7	27	7	47	7	67	7	87	7
08	8	28	8	48	8	68	8	88	8
09	9	29	9	49	9	69	9	89	9
0A	A	2A	A	4A	A	6A	A	8A	A
0B	B	2B	B	4B	B	6B	B	8B	B
0C	C	2C	C	4C	C	6C	C	8C	C
0D	D	2D	D	4D	D	6D	D	8D	D
0E	E	2E	E	4E	E	6E	E	8E	E
0F	F	2F	F	4F	F	6F	F	8F	F
10	0	30	0	50	0	70	0	90	0
11	1	31	1	51	1	71	1	91	1
12	2	32	2	52	2	72	2	92	2
13	3	33	3	53	3	73	3	93	3
14	4	34	4	54	4	74	4	94	4
15	5	35	5	55	5	75	5	95	5
16	6	36	6	56	6	76	6	96	6
17	7	37	7	57	7	77	7	97	7
18	8	38	8	58	8	78	8	98	8
19	9	39	9	59	9	79	9	99	9
1A	0	3A	A	5A	0	7A	A	9A	A
1B	B	3B	B	5B	B	7B	B	9B	B
1C	C	3C	C	5C	C	7C	C	9C	C
1D	D	3D	D	5D	D	7D	D	9D	D
1E	E	3E	E	5E	E	7E	E	9E	E
1F	F	3F	F	5F	F	7F	F	9F	F

MJ1N

1024-BIT READ ONLY MEMORY

MJ1N 96 COL CODE TO EBCDIC LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	0	B3	3	C6	6	DB	B	EE	E
A1	1	B4	4	C7	7	DC	C	EF	F
A2	2	B5	5	C8	8	DD	D	F0	A
A3	3	B6	6	C9	9	DE	E	F1	1
A4	4	B7	7	CA	A	DF	F	F2	2
A5	5	B8	8	CB	B	E0	0	F3	3
A6	6	B9	9	CC	C	E1	1	F4	4
A7	7	BA	A	CD	D	E2	2	F5	5
A8	8	BB	B	CE	E	E3	3	F6	6
A9	9	BC	C	CF	F	E4	4	F7	7
AA	A	BD	D	D0	0	E5	5	F8	8
AB	B	BE	E	D1	1	E6	6	F9	9
AC	C	BF	F	D2	2	E7	7	FA	A
AD	D	C0	0	D3	3	E8	8	FB	B
AE	E	C1	1	D4	4	E9	9	FC	C
AF	F	C2	2	D5	5	EA	A	FD	D
B0	A	C3	3	D6	6	EB	B	FE	E
B1	1	C4	4	D7	7	EC	C	FF	F
B2	2	C5	5	D8	8	ED	D		
				D9	9				
				DA	A				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MJ2N

1024-BIT READ ONLY MEMORY

MJ2N 96 COL CODE TO EBCDIC MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	4	20	6	40	0	60	2	80	C
01	F	21	D	41	B	61	9	81	7
02	F	22	D	42	B	62	9	82	7
03	F	23	D	43	B	63	9	83	7
04	F	24	D	44	B	64	9	84	7
05	F	25	D	45	B	65	9	85	7
06	F	26	D	46	B	66	9	86	7
07	F	27	D	47	B	67	9	87	7
08	F	28	D	48	B	68	9	88	7
09	F	29	D	49	B	69	9	89	7
0A	7	2A	5	4A	3	6A	1	8A	F
0B	7	2B	5	4B	3	6B	1	8B	F
0C	7	2C	5	4C	3	6C	1	8C	F
0D	7	2D	5	4D	3	6D	1	8D	F
0E	7	2E	5	4E	3	6E	1	8E	F
0F	7	2F	5	4F	3	6F	1	8F	F
10	F	30	D	50	B	70	9	90	7
11	6	31	C	51	2	71	8	91	E
12	E	32	C	52	A	72	8	92	6
13	E	33	C	53	A	73	8	93	6
14	E	34	C	54	A	74	8	94	6
15	E	35	C	55	A	75	8	95	6
16	E	36	C	56	A	76	8	96	6
17	E	37	C	57	A	77	8	97	6
18	E	38	C	58	A	78	8	98	6
19	E	39	C	59	A	79	8	99	6
1A	5	3A	4	5A	1	7A	0	9A	E
1B	6	3B	4	5B	2	7B	0	9B	E
1C	6	3C	4	5C	2	7C	0	9C	E
1D	6	3D	4	5D	2	7D	0	9D	E
1E	6	3E	4	5E	2	7E	0	9E	E
1F	6	3F	4	5F	2	7F	0	9F	E

MJ2N

1024-BIT READ ONLY MEMORY

MJ2N 96 COL CODE TO EBCDIC MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	E	B3	4	C6	3	DB	A	EE	9
A1	5	B4	4	C7	3	DC	A	EF	9
A2	5	B5	4	C8	3	DD	A	F0	2
A3	5	B6	4	C9	3	DE	A	F1	0
A4	5	B7	4	CA	B	DF	A	F2	0
A5	5	B8	4	CB	B	E0	A	F3	0
A6	5	B9	4	CC	B	E1	1	F4	0
A7	5	BA	C	CD	B	E2	1	F5	0
A8	5	BB	C	CE	B	E3	1	F6	0
A9	5	BC	C	CF	B	E4	1	F7	0
AA	D	BD	C	D0	3	E5	1	F8	0
AB	D	BE	C	D1	A	E6	1	F9	0
AC	D	BF	C	D2	2	E7	1	FA	8
AD	D	C0	8	D3	2	E8	1	FB	8
AE	D	C1	3	D4	2	E9	1	FC	8
AF	D	C2	3	D5	2	EA	9	FD	8
B0	6	C3	3	D6	2	EB	9	FE	8
B1	4	C4	3	D7	2	EC	9	FF	8
B2	4	C5	3	D8	2	ED	9		
				D9	2				
				DA	A				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Deciaml:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MJ3N

1024-BIT READ ONLY MEMORY

MJ3N EBCDIC TO 96 COL CODE LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	0	20	0	40	0	60	0	80	0
01	1	21	1	41	1	61	1	81	1
02	2	22	2	42	2	62	2	82	2
03	3	23	3	43	3	63	3	83	3
04	4	24	4	44	4	64	4	84	4
05	5	25	5	45	5	65	5	85	5
06	6	26	6	46	6	66	6	86	6
07	7	27	7	47	7	67	7	87	7
08	8	28	8	48	8	68	8	88	8
09	9	29	9	49	9	69	9	89	9
0A	A	2A	0	4A	A	6A	0	8A	A
0B	B	2B	B	4B	B	6B	B	8B	B
0C	C	2C	C	4C	C	6C	C	8C	C
0D	D	2D	D	4D	D	6D	D	8D	D
0E	E	2E	E	4E	E	6E	E	8E	E
0F	F	2F	F	4F	F	6F	F	8F	F
10	A	30	0	50	A	70	0	90	0
11	1	31	1	51	1	71	1	91	1
12	2	32	2	52	2	72	2	92	2
13	3	33	3	53	3	73	3	93	3
14	4	34	4	54	4	74	4	94	4
15	5	35	5	55	5	75	5	95	5
16	6	36	6	56	6	76	6	96	6
17	7	37	7	57	7	77	7	97	7
18	8	38	8	58	8	78	8	98	8
19	9	39	9	59	9	79	9	99	9
1A	A	3A	A	5A	A	7A	A	9A	A
1B	B	3B	B	5B	B	7B	B	9B	B
1C	C	3C	C	5C	C	7C	C	9C	C
1D	D	3D	D	5D	D	7D	D	9D	D
1E	E	3E	E	5E	E	7E	E	9E	E
1F	F	3F	F	5F	F	7F	F	9F	F

MJ3N

1024-BIT READ ONLY MEMORY

MJ3N EBCDIC TO 96 COL CODE LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	0	B3	3	C6	6	DB	B	EE	E
A1	1	B4	4	C7	7	DC	C	EF	F
A2	2	B5	5	C8	8	DD	D	F0	0
A3	3	B6	6	C9	9	DE	E	F1	1
A4	4	B7	7	CA	A	DF	F	F2	2
A5	5	B8	8	CB	B	E0	0	F3	3
A6	6	B9	9	CC	C	E1	1	F4	4
A7	7	BA	A	CD	D	E2	2	F5	5
A8	8	BB	B	CE	E	E3	3	F6	6
A9	9	BC	C	CF	F	E4	4	F7	7
AA	A	BD	D	D0	0	E5	5	F8	8
AB	B	BE	E	D1	1	E6	6	F9	9
AC	C	BF	F	D2	2	E7	7	FA	A
AD	D	C0	0	D3	3	E8	8	FB	B
AE	E	C1	1	D4	4	E9	9	FC	C
AF	F	C2	2	D5	5	EA	A	FD	D
B0	0	C3	3	D6	6	EB	B	FE	E
B1	1	C4	4	D7	7	EC	C	FF	F
B2	2	C5	5	D8	8	ED	D		
				D9	9				
				DA	A				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MJ4N

1024-BIT READ ONLY MEMORY

MJ4N EBCDIC TO 96 COL CODE MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	4	20	6	40	0	60	2	80	C
01	F	21	5	41	B	61	1	81	7
02	F	22	D	42	B	62	9	82	7
03	F	23	D	43	B	63	9	83	7
04	F	24	D	44	B	64	9	84	7
05	F	25	D	45	B	65	9	85	7
06	F	26	D	46	B	66	9	86	7
07	F	27	D	47	B	67	9	87	7
08	F	28	D	48	B	68	9	88	7
09	F	29	D	49	B	69	9	89	7
0A	7	2A	F	4A	3	6A	B	8A	F
0B	7	2B	5	4B	3	6B	1	8B	F
0C	7	2C	5	4C	3	6C	1	8C	F
0D	7	2D	5	4D	3	6D	1	8D	F
0E	7	2E	5	4E	3	6E	1	3E	F
0F	7	2F	5	4F	3	6F	1	8F	F
10	5	30	D	50	1	70	9	90	7
11	E	31	C	51	A	71	8	91	6
12	E	32	C	52	A	72	8	92	6
13	E	33	C	53	A	73	8	93	6
14	E	34	C	54	A	74	8	94	6
15	E	35	C	55	A	75	8	95	6
16	E	36	C	56	A	76	8	96	6
17	E	37	C	57	A	77	8	97	6
18	E	38	C	58	A	78	8	98	6
19	E	39	C	59	A	79	8	99	6
1A	6	3A	4	5A	2	7A	0	9A	E
1B	6	3B	4	5B	2	7B	0	9B	E
1C	6	3C	4	5C	2	7C	0	9C	E
1D	6	3D	4	5D	2	7D	0	9D	E
1E	6	3E	4	5E	2	7E	0	9E	E
1F	6	3F	4	5F	2	7F	0	9F	E

MJ4N

1024-BIT READ ONLY MEMORY

MJ4N EBCDIC TO 96 COL CODE MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	E	B3	4	C6	3	DB	A	EE	9
A1	D	B4	4	C7	3	DC	A	EF	9
A2	5	B5	4	C8	3	DD	A	F0	1
A3	5	B6	4	C9	3	DE	A	F1	0
A4	5	B7	4	CA	B	DF	A	F2	0
A5	5	B8	4	CB	B	E0	A	F3	0
A6	5	B9	4	CC	B	E1	9	F4	0
A7	5	BA	C	CD	B	E2	1	F5	0
A8	5	BB	C	CE	B	E3	1	F6	0
A9	5	BC	C	CF	B	E4	1	F7	0
AA	D	BD	C	D0	3	E5	1	F8	0
AB	D	BE	C	D1	2	E6	1	F9	0
AC	D	BF	C	D2	2	E7	1	FA	8
AD	D	C0	8	D3	2	E8	1	FB	8
AE	D	C1	3	D4	2	E9	1	FC	8
AF	D	C2	3	D5	2	EA	9	FD	8
B0	5	C3	3	D6	2	EB	9	FE	8
B1	4	C4	3	D7	2	EC	9	FF	8
B2	4	C5	3	D8	2	ED	9		
				D9	2				
				DA	A				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MK1N

1024-BIT READ ONLY MEMORY

MK1N EBCDIC TO BCL+PAR LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	F	40	F	60	F	80	F
01	F	21	F	41	F	61	E	81	F
02	F	22	F	42	F	62	F	82	F
03	F	23	F	43	F	63	F	83	F
04	F	24	F	44	F	64	F	84	F
05	F	25	F	45	F	65	F	85	F
06	F	26	F	46	F	66	F	86	F
07	F	27	F	47	F	67	F	87	F
08	F	28	F	48	F	68	F	88	F
09	F	29	F	49	F	69	F	89	F
0A	F	2A	F	4A	3	6A	F	8A	F
0B	F	2B	F	4B	4	6B	4	8B	F
0C	F	2C	F	4C	1	6C	3	8C	F
0D	F	2D	F	4D	2	6D	5	8D	F
0E	F	2E	F	4E	5	6E	1	8E	F
0F	F	2F	F	4F	0	6F	F	8F	F
10	F	30	F	50	F	70	5	90	F
11	F	31	F	51	F	71	F	91	F
12	F	32	F	52	F	72	F	92	F
13	F	33	F	53	F	73	F	93	F
14	F	34	F	54	F	74	F	94	F
15	F	35	F	55	F	75	F	95	F
16	F	36	F	56	F	76	F	96	F
17	F	37	F	57	F	77	F	97	F
18	F	38	F	58	F	78	F	98	F
19	F	39	F	59	F	79	F	99	F
1A	F	3A	F	5A	1	7A	2	9A	F
1B	F	3B	F	5B	4	7B	4	9B	F
1C	F	3C	F	5C	3	7C	3	9C	F
1D	F	3D	F	5D	2	7D	0	9D	F
1E	F	3E	F	5E	1	7E	2	9E	F
1F	F	3F	F	5F	0	7F	0	9F	F

MK1N

1024-BIT READ ONLY MEMORY

MK1N EBCDIC TO BCL+PAR LSB CODE FORMAT

HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT
A0	F	B3	F	C6	9	DB	F	EE	F
A1	F	B4	F	C7	8	DC	F	EF	F
A2	F	B5	F	C8	7	DD	F	F0	5
A3	F	B6	F	C9	6	DE	F	F1	E
A4	F	B7	F	CA	F	DF	F	F2	D
A5	F	B8	F	CB	F	E0	F	F3	C
A6	F	B9	F	CC	F	E1	F	F4	B
A7	F	BA	F	CD	F	E2	D	F5	A
A8	F	BB	F	CE	F	E3	C	F6	9
A9	F	BC	F	CF	F	E4	B	F7	8
AA	F	BD	F	D0	5	E5	A	F8	7
AB	F	BE	F	D1	E	E6	9	F9	6
AC	F	BF	F	D2	D	E7	8	FA	F
AD	F	C0	5	D3	C	E8	7	FB	F
AE	F	C1	E	D4	B	E9	6	FC	F
AF	F	C2	D	D5	A	EA	F	FD	F
B0	F	C3	C	D6	9	EB	F	FE	F
B1	F	C4	B	D7	8	EC	F	FF	F
B2	F	C5	A	D8	7	ED	F		
				D9	6				
				DA	F				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

MK2N

1024-BIT READ ONLY MEMORY

MK2N EBCDIC TO BCL+PAR MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	F	40	A	60	9	80	F
01	F	21	F	41	F	61	E	81	F
02	F	22	F	42	F	62	F	82	F
03	F	23	F	43	F	63	F	83	F
04	F	24	F	44	F	64	F	84	F
05	F	25	F	45	F	65	F	85	F
06	F	26	F	46	F	66	F	86	F
07	F	27	F	47	F	67	F	87	F
08	F	28	F	48	F	68	F	88	F
09	F	29	F	49	F	69	F	89	F
0A	F	2A	F	4A	C	6A	F	8A	F
0B	F	2B	F	4B	8	6B	E	8B	F
0C	F	2C	F	4C	8	6C	A	8C	F
0D	F	2D	F	4D	8	6D	A	8D	F
0E	F	2E	F	4E	C	6E	B	8E	F
0F	F	2F	F	4F	C	6F	F	8F	F
10	F	30	F	50	C	70	9	90	F
11	F	31	F	51	F	71	F	91	F
12	F	32	F	52	F	72	F	92	F
13	F	33	F	53	F	73	F	93	F
14	F	34	F	54	F	74	F	94	F
15	F	35	F	55	F	75	F	95	F
16	F	36	F	56	F	76	F	96	F
17	F	37	F	57	F	77	F	97	F
18	F	38	F	58	F	78	F	98	F
19	F	39	F	59	F	79	F	99	F
1A	F	3A	F	5A	E	7A	B	9A	F
1B	F	3B	F	5B	D	7B	B	9B	F
1C	F	3C	F	5C	9	7C	F	9C	F
1D	F	3D	F	5D	D	7D	F	9D	F
1E	F	3E	F	5E	D	7E	E	9E	F
1F	F	3F	F	5F	9	7F	A	9F	F

MK2N

1024-BIT READ ONLY MEMORY

MK2N EBCDIC TO BCL+PAR MSB CODE FORMAT

HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT
A0	F	B3	F	C6	C	DB	F	EE	F
A1	F	B4	F	C7	8	DC	F	EF	F
A2	F	B5	F	C8	8	DD	F	F0	F
A3	F	B6	F	C9	C	DE	F	F1	B
A4	F	B7	F	CA	F	DF	F	F2	B
A5	F	B8	F	CB	F	E0	7	F3	F
A6	F	B9	F	CC	F	E1	F	F4	B
A7	F	BA	F	CD	F	E2	E	F5	F
A8	F	BB	F	CE	F	E3	A	F6	F
A9	F	BC	F	CF	F	E4	E	F7	B
AA	F	BD	F	D0	9	E5	A	F8	B
AB	F	BE	F	D1	D	E6	A	F9	F
AC	F	BF	F	D2	D	E7	E	FA	F
AD	F	C0	C	D3	9	E8	E	FB	F
AE	F	C1	8	D4	D	E9	A	FC	F
AF	F	C2	8	D5	9	EA	F	FD	F
B0	F	C3	C	D6	9	EB	F	FE	F
B1	F	C4	8	D7	D	EC	F	FF	F
B2	F	C5	C	D8	D	ED	F		
				D9	9				
				DA	F				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

RM1N

1024-BIT READ ONLY MEMORY

RM1N EBCDIC TO KATAKANA LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	F	40	F	60	2	80	F
01	F	21	F	41	F	61	0	81	9
02	F	22	F	42	F	62	F	82	8
03	F	23	F	43	F	63	F	83	7
04	F	24	F	44	F	64	F	84	6
05	F	25	F	45	F	65	F	85	5
06	F	26	F	46	F	66	F	86	5
07	F	27	F	47	F	67	F	87	4
08	F	28	F	48	F	68	F	88	0
09	F	29	F	49	F	69	F	89	F
0A	F	2A	F	4A	F	6A	F	8A	4
0B	F	2B	F	4B	1	6B	3	8B	F
0C	F	2C	F	4C	3	6C	F	8C	3
0D	F	2D	F	4D	F	6D	F	8D	2
0E	F	2E	F	4E	4	6E	1	8E	1
0F	F	2F	F	4F	F	6F	F	8F	0
10	F	30	F	50	F	70	F	90	F
11	F	31	F	51	F	71	F	91	E
12	F	32	F	52	F	72	F	92	D
13	F	33	F	53	F	73	F	93	C
14	F	34	F	54	F	74	F	94	B
15	F	35	F	55	F	75	F	95	A
16	F	36	F	56	F	76	F	96	9
17	F	37	F	57	F	77	F	97	8
18	F	38	F	58	F	78	F	98	7
19	F	39	F	59	F	79	F	99	6
1A	F	3A	F	5A	F	7A	F	9A	5
1B	F	3B	F	5B	A	7B	C	9B	F
1C	F	3C	F	5C	E	7C	F	9C	F
1D	F	3D	F	5D	F	7D	F	9D	4
1E	F	3E	F	5E	F	7E	2	9E	3
1F	F	3F	F	5F	F	7F	0	9F	2

RM1N

1024-BIT READ ONLY MEMORY

RM1N EBCDIC TO KATAKANA LSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
A0	F	B3	F	C6	9	DB	F	EE	F
A1	F	B4	F	C7	8	DC	F	EF	F
A2	1	B5	F	C8	7	DD	F	F0	F
A3	0	B6	F	C9	6	DE	F	F1	E
A4	F	B7	F	CA	F	DF	F	F2	D
A5	E	B8	F	CB	F	E0	F	F3	C
A6	D	B9	F	CC	F	E1	F	F4	B
A7	C	BA	4	CD	F	E2	C	F5	A
A8	B	BB	3	CE	F	E3	B	F6	9
A9	A	BC	2	CF	F	E4	A	F7	8
AA	9	BD	1	D0	F	E5	9	F8	7
AB	F	BE	D	D1	5	E6	8	F9	6
AC	8	BF	B	D2	4	E7	7	FA	F
AD	7	C0	F	D3	3	E8	6	FB	F
AE	6	C1	E	D4	2	E9	5	FC	F
AF	5	C2	D	D5	1	EA	F	FD	F
B0	F	C3	C	D6	0	EB	F	FE	F
B1	F	C4	B	D7	F	EC	F	FF	F
B2	F	C5	A	D8	E	ED	F		
				D9	D				
				DA	F				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

RM2N

1024-BIT READ ONLY MEMORY

RM2N EBCDIC TO KATAKANA MSB CODE FORMAT

HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT	HEXA-DECIMAL INPUT	OUTPUT
00	F	20	F	40	D	60	D	80	F
01	F	21	F	41	F	61	D	81	D
02	F	22	F	42	F	62	F	82	D
03	F	23	F	43	F	63	F	83	D
04	F	24	F	44	F	64	F	84	D
05	F	25	F	45	F	65	F	85	D
06	F	26	F	46	F	66	F	86	C
07	F	27	F	47	F	67	F	87	C
08	F	28	F	48	F	68	F	88	C
09	F	29	F	49	F	69	F	89	B
0A	F	2A	F	4A	F	6A	F	8A	A
0B	F	2B	F	4B	D	6B	D	8B	F
0C	F	2C	F	4C	C	6C	F	8C	A
0D	F	2D	F	4D	F	6D	F	8D	A
0E	F	2E	F	4E	D	6E	C	8E	A
0F	F	2F	F	4F	F	6F	F	8F	A
10	F	30	F	50	F	70	F	90	9
11	F	31	F	51	F	71	F	91	9
12	F	32	F	52	F	72	F	92	9
13	F	33	F	53	F	73	F	93	9
14	F	34	F	54	F	74	F	94	9
15	F	35	F	55	F	75	F	95	9
16	F	36	F	56	F	76	F	96	9
17	F	37	F	57	F	77	F	97	9
18	F	38	F	58	F	78	F	98	9
19	F	39	F	59	F	79	F	99	9
1A	F	3A	F	5A	F	7A	F	9A	9
1B	F	3B	F	5B	D	7B	D	9B	F
1C	F	3C	F	5C	D	7C	F	9C	F
1D	F	3D	F	5D	F	7D	F	9D	9
1E	F	3E	F	5E	F	7E	C	9E	9
1F	F	3F	F	5F	F	7F	8	9F	9

RM2N

1024-BIT READ ONLY MEMORY

RM2N EBCDIC TO KATAKANA MSB CODE FORMAT

HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT	HEXA-DECIMAL INPUT	HEXA-DECIMAL OUTPUT
A0	F	B3	F	C6	B	DB	F	EE	F
A1	F	B4	F	C7	B	DC	F	EF	F
A2	9	B5	F	C8	B	DD	F	F0	C
A3	9	B6	F	C9	B	DE	F	F1	C
A4	8	B7	F	CA	F	DF	F	F2	C
A5	8	B8	F	CB	F	E0	F	F3	C
A6	8	B9	F	CC	F	E1	F	F4	C
A7	8	BA	8	CD	F	E2	A	F5	C
A8	8	BB	8	CE	F	E3	A	F6	C
A9	8	BC	8	CF	F	E4	A	F7	C
AA	8	BD	8	D0	F	E5	A	F8	C
AB	F	BE	D	D1	B	E6	A	F9	C
AC	8	BF	D	D2	B	E7	A	FA	F
AD	8	C0	F	D3	B	E8	A	FB	F
AE	8	C1	B	D4	B	E9	A	FC	F
AF	8	C2	B	D5	B	EA	F	FD	F
B0	F	C3	B	D6	B	EB	F	FE	F
B1	F	C4	B	D7	A	EC	F	FF	F
B2	F	C5	B	D8	A	ED	F		
				D9	A				
				DA	F				

NOTE:

1) Inputs are A0, A1, A2, A3, A4, A5, A6, A7, where A0 is the least significant and A7 is the most significant.

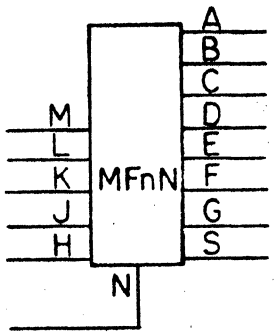
2) Outputs are: 01, 02, 03, 04, where 01 is the least significant and 04 is the most significant digit.

3) In Hexa-Decimal:

0 = 0000	8 = 1000
1 = 0001	9 = 1001
2 = 0010	A = 1010
3 = 0011	B = 1011
4 = 0100	C = 1100
5 = 0101	D = 1101
6 = 0110	E = 1110
7 = 0111	F = 1111

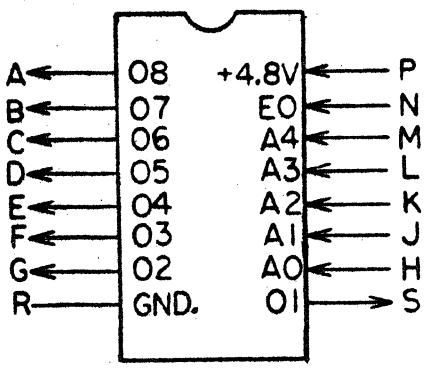
256-BIT READ-ONLY MEMORY

MμL 9034 - NOTED MFnN SA 1918-NOTED



FUNCTIONAL DIAGRAM

ELEMENT TYPE	FAIRCHILD NO.	PART NO.	FUNCTION
MF4N	40249	3516	XLTR.-EBCDIC TO BCL 1/4
MF5N	40250	3524	XLTR.-EBCDIC TO BCL 2/4
MF6N	40251	3532	XLTR.-EBCDIC TO BCL 3/4
MF7N	40252	3540	XLTR.-EBCDIC TO BCL 4/4
MF8N	40253	3557	XLTR.-BCL TO EBCDIC 1/2
MF9N	40254	3565	XLTR.-BCL TO EBCDIC 2/2



PIN LOCATION DIAGRAM

16 PIN DIP

MFNN

256-BIT READ ONLY MEMORY

(1) The circuit is a T^2L Logic Compatible organized as 32 words of 8-bits each. The memory has 5 address lines A0 thru A4, one Enable input, $\overline{E0}$, and 8 outputs 01 thru 08. The words are selected by the five address lines.

(2) The codes of these ROMs are not inverted, and thus code translation is obtained directly. MF4N, MF5N, MF6N, and MF7N should be combined to translate from EBCDIC, 8-bits code to BCL, 6-bits code. MF8N and MF9N should be combined to translate from BCL, 6-bits code to the EBCDIC, 8-bits code.

(3) Logical False level applied at the Enable input is needed to enable the chip, otherwise the chip is disabled and True level voltage is forced at all outputs.

(4) Consult Section 5 for interface information.

(5) Address inputs or Enable input maximum current is -1.6ma at +.4 volts, and .10ma at +4.5 volts.

(6) The memory outputs offer the possibility of the wire-OR connection.

(7) Output current is 10ma at +.4 volts and -.20ma at +5.5 volts.

(8) Both inputs and outputs are shown in the bit code format tables using Binary 1 to represent a true voltage level and Binary 0 to represent false voltage level.

(9) Maximum delay time:

Address to output, td=50ns.
Memory Enable to output, td=50ns.

MF4N MF5N

256 BIT READ ONLY MEMORY

EBCDIC → BCL

MF4N CODE FORMAT		MF5N CODE FORMAT	
BINARY INPUT	BINARY OUTPUT	BINARY INPUT	BINARY OUTPUT
00000	010000	00000	100000
01010	111100	00001	010001
01011	111011	01011	011011
01100	111110	01100	011100
01101	111101	01101	011010
01110	111010	01110	001110
01111	111111	11010	001101
10000	110000	11011	001011
11010	011110	11100	001100
11011	101011	11101	001111
11100	101100	11110	011101
11101	101101	11111	011111
11110	101110		
11111	101111		

NOTE:

1) Inputs are A0, A1, A2, A3, A4 where A0 is the least significant digit and A4 is the most significant.

2) Outputs are 01, 02, 03, 04, 05, 06 where 01 is the least significant digit and 06 is the most significant.

3) Inputs that are not tabulated have ZERO outputs.

MF6N

MF7N

256 BIT READ ONLY MEMORY

EBCDIC → BCL

MF6N CODE FORMAT		MF7N CODE FORMAT	
BINARY INPUT	BINARY OUTPUT	BINARY INPUT	BINARY OUTPUT
00000	111010	00000	000000
00001	110001	00010	010010
00010	110010	00011	010011
00011	110011	00100	010100
00100	110100	00101	010101
00101	110101	00110	010110
00110	110110	00111	010111
00111	110111	01000	011000
01000	111000	01001	011001
01001	111001	10000	001010
10000	101010	10001	000001
10001	100001	10010	000010
10010	100010	10011	000011
10011	100011	10100	000100
10100	100100	10101	000101
10101	100101	10110	000110
10110	100110	10111	000111
10111	100111	11000	001000
11000	101000	11001	001001
11001	101001		

NOTES:

1) Inputs are A0, A1, A2, A3, A4 where A0 is the least significant digit and A4 is the most significant.

2) Outputs are 0i, 02, 03, 04, 05, 06 where 01 is the least significant digit and 06 is the most significant.

3) Inputs that are not tabulated have ZERO outputs.

MF8N

MF9N

256 BIT READ ONLY MEMORY

BCL → EBCDIC

MF8N CODE FORMAT		MF9N CODE FORMAT	
BINARY INPUT	**BINARY OUTPUT**	**BINARY INPUT**	**BINARY OUTPUT**
00000	01101111	00000	01100000
00001	11110001	00001	11010001
00010	11110010	00010	11010010
00011	11110011	00011	11010011
00100	11110100	00100	11010100
00101	11110101	00101	11010101
00110	11110110	00110	11010110
00111	11110111	00111	11010111
01000	11111000	01000	11011000
01001	11111001	01001	11011001
01010	11110000	01010	11010000
01011	01111011	01011	01011011
01100	01111100	01100	01011100
01101	01111010	01101	01011101
01110	01101110	01110	01011110
01111	01111101	01111	01011111
10000	01000000	10000	01010000
10001	01100001	10001	11000001
10010	11100010	10010	11000010
10011	11100011	10011	11000011
10100	11100100	10100	11000100
10101	11100101	10101	11000101
10110	11100110	10110	11000110
10111	11100111	10111	11000111
11000	11101000	11000	11001000
11001	11101001	11001	11001001
11010	01101101	11010	11000000
11011	01101011	11011	01001011
11100	01101100	11100	01001010
11101	01111110	11101	01001101
11110	01011010	11110	01001100
11111	01111111	11111	01001111

NOTES:

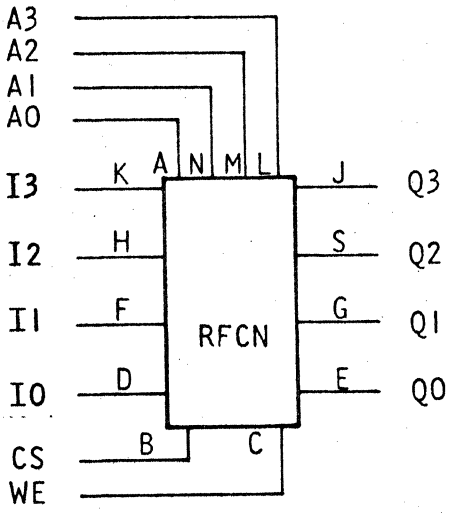
1) **Inputs are A0, A1, A2, A3, A4 where A0 is the least significant digit and A4 is the most significant.**

2) **Outputs are 01, 02, 03, 04, 05, 06, 07, 08 where 01 is the least significant digit and 08 is the most significant.**

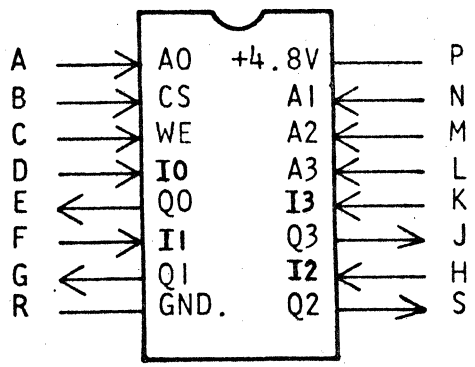
RFCN

3.2 TTL/DTL Integrated Circuits

Element Type: RFCN
Standard Assembly Number: 2205 2609
Circuit Designation: **64 Bit Memory**
Description of Operation:



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM
16 PIN DIP

RFCN

SA 2205 2609

64-BIT MEMORY

1) The circuit is T^2L organized as 16 words of 4-Bits each. Inputs to the chip are 4 Data Input lines I0 thru I3, 4 Address Lines A0 thru A3, one Chip Select $\overline{CS}$, and one Write Enable line WE. Outputs of the chip are Data Output lines Q0 thru Q3.

2) A logic zero on the Chip Select line permits addressing of each of the sixteen words thru the address lines. A logic one on the Chip Select input forces the outputs HIGH, and prevents addressing of the sixteen words.

   A logic zero on the Write Enable input allows the data present on the Data Inputs to be transferred in the addressed word. A logic one on the Write Enable causes nondestructive transfer of the word through the sense amplifiers to the Data Outputs.

CHIP SELECT (CS)	WRITE ENABLE (WE)	FUNCTION
0	0	WRITE
0	1	READ
1	X	NO ACTION

3) Inputs shall alwasy be driven by a CTL restoring element with the right external pull-down resistor connected from the restoring element output to ground.

4) Output of the chip is the complement of the data input.

5) The outputs shall always be connected to CTL restoring elements and an external pull-up resistor, connected from the memory outputs to the V_{CC} supply voltage.

6) The memory outputs offer the possibility of the wire-OR connection.

7) Maximum Read access time measured from the leading edge of the address = 45 ns.

8) Maximum access time measured from the negative going edge of the chip select = 27 ns.

9) Minimum Write Enable pulse width = 30 ns.

10) Maximum recovery time after Write Enable trailing edge = 45 ns.

11) Write Enable negative going edge shall follow the address by 5 ns. minimum, and the positive going edge shall precede the new address by 5 ns. minimum.

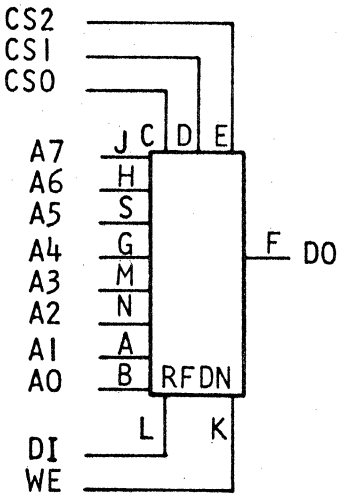
12) Data Set-up time is 30 ns; data Hold time is 5 ns. Both are measured relative to the positive going edge of the WE pulse.

13) The CTL interface rules within section 5, Hardware Rules Book, should be complied with.

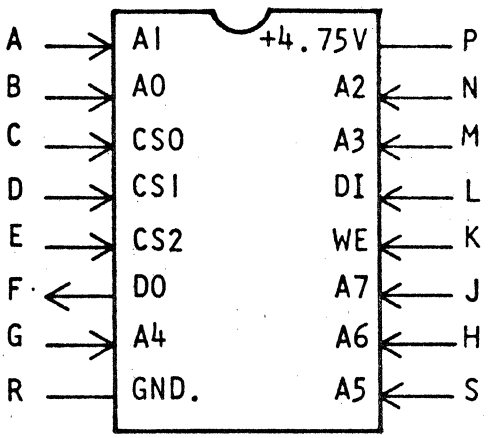
RFDN

3.2 TTL/DTL Integrated Circuits

Element Type: RFDN
Standard Assembly Number: 2206 1626
Circuit Designation: 256-BIT MEMORY
Description of Operation:



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM
16 PIN DIP

RFDN

256 BIT MEMORY SA 2206 1626

1. This is a TTL monolithic circuit organized as 256 x 1-bit words. Inputs to the chip are eight address lines, A0 thru A7, three Chip-Select lines, $\overline{CS0}$ thru $\overline{CS2}$, a Write Enable line, WE, and one Data Input, DI. The circuit has only one output pin, the Data Output DO.

2. All three Chip-Select inputs have to be held at a logic zero to enable the package. A logic one at any of the Chip-Select inputs disables the device.

3. A logic zero applied to the Write Enable input, simultaneously with all CS inputs held at a logic zero, will allow the data present at the Data Input to be written into the addressed word.

4. When the WE input is held at a logic one, and the device is enabled (CS low), the data stored in the addressed memory word is available at the Data Output line DO. The data present at the DO terminal is the complement of the input data written into that addressed word.

5. The following table summarizes the device operation:

$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	WE	FUNCTION
0	0	0	0	WRITE
0	0	0	1	READ
X	X	1	X	NO ACTION
X	1	X	X	NO ACTION
1	X	X	X	NO ACTION

note: X = don't care.

6. Inputs shall always be driven by CTL restoring elements with an external pull-down resistor, connected from the restoring element to ground.

7. The output shall always be connected to fully threshold sensitive CTL restoring elements (those accepting 4th level). An external pull-up resistor, connected from the memory output to the V_{cc} supply voltage shall always be used.

RFDN

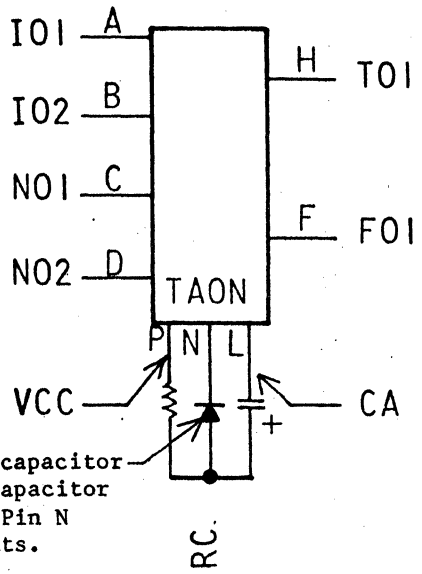
SA 2206 1626

8. The open-collector output can be wired-OR together with other packages.
9. Maximum access time from Address inputs is 70 ns.
10. Maximum access time from Chip Select input is 55 ns.
11. Minimum Write Enable pulse width is 55 ns.
12. Write Enable negative going edge shall follow the address and/or chip-select transition by 15 ns minimum. The positive going edge of WE shall precede the new address or chip-select transition by 15 ns minimum.
13. Data Set-up time relative to the positive going transition of WE is 55 ns minimum Data Hold time relative to the positive going transition of WE is 15 ns minimum.
14. Maximum Write Recovery time, after the positive going transition of WE, is 70 ns.
15. See section 5, Hardware Rules Book, for the circuitry to interface CTL to TTL.
16. The false level input current for this device is -1.0 mA @ V_{fi} = +.4V.

TAON

3.2 TTL/DTL Integrated Circuits

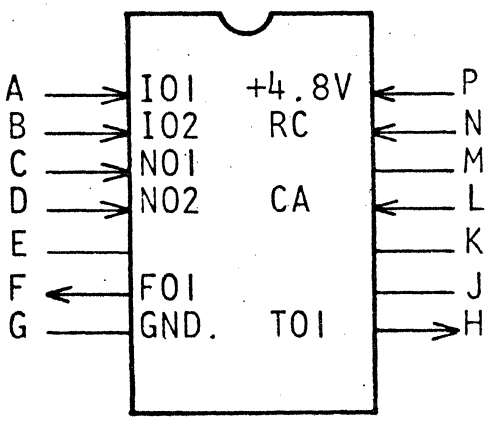
Element Type: TAON
Standard Assembly Number: 1901 7102
Circuit Designation: Monostable Multivibrator
Description of Operation:



NOTE: Diode shown is required only when timing capacitor CA is an electrolytic type. With other capacitor types, the diode should not be used, and Pin N connected directly to the timing components.

FUNCTIONAL DIAGRAM

VALUES OF EXTERNAL RESISTOR AND CAPACITOR DETERMINED BY DESIGNER.



PIN LOCATION DIAGRAM
14 PIN DIP

TAON

MONOSTABLE MULTIVIBRATOR

1) The circuit is T^2L logic compatible multivibrator with four inputs, two of which I01 and I02 are active level low and two, N01 and N02 are active level high. The multi has two complementary outputs T01 and F01.

2) The multi may be used as a leading edge trigger thru N01 and N02 inputs or a trailing edge trigger thru I01 and I02 inputs.

3) When the triggering conditions are met, the external effective capacitor is discharged and a new cycle begins.

4) The triggering conditions are $(\overline{I01}+\overline{I02})$ N01·N02 or as shown in the following table:

I01	I02	N01	N02
0	0	1	1
0	1	1	1
1	0	1	1

5) Successive inputs with a period shorter than the time delay results in a continuous true output.

6) Consult Section 5 for interface information.

7) Input maximum current is -1.6 ma at +.45 volts and .06 ma at +4.5V.

8) T01 output gives a true level output during the timing period and false level during the quiescent time. F01 gives the complement of T01.

9) The used outputs shall always be connected to CT_uL restoring elements and external pull-up resistors, connected from the multi output to the V_{CC} supply voltage.

10) Output current is 9.1 ma at .45 V, -6.66 ma at 1.6V, and -.72 ma at 2.4V.

11) External timing resistor and capacitor are required to obtain the right pulse width. The resistor may vary from 5K to 50K ohms.

12) Minimum input pulse width is 40 ns.

13) Minimum output pulse width is 65 ns.

14) Maximum time delay between the +1.5 V point on the negative going edge of the input pulse and the +1.5V point on the positive going edge of T01 output or negative going edge of F01, td = 50 ns.

15) The formula for the output pulse width is:

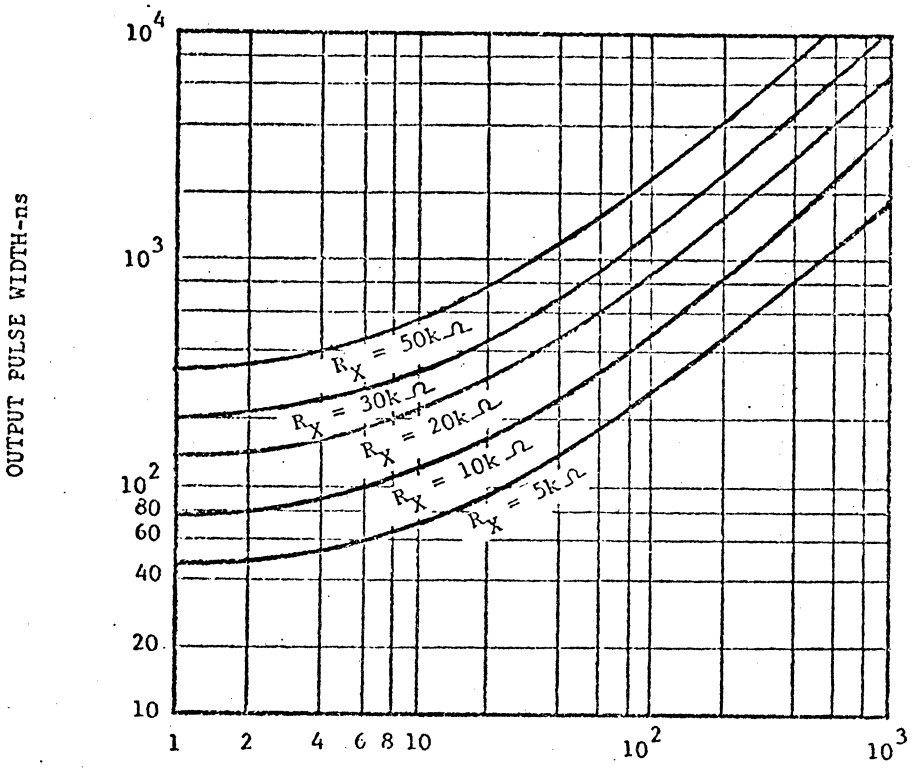
$$T \approx .32\ RC \left[1 + \frac{0.7}{R}\right]$$

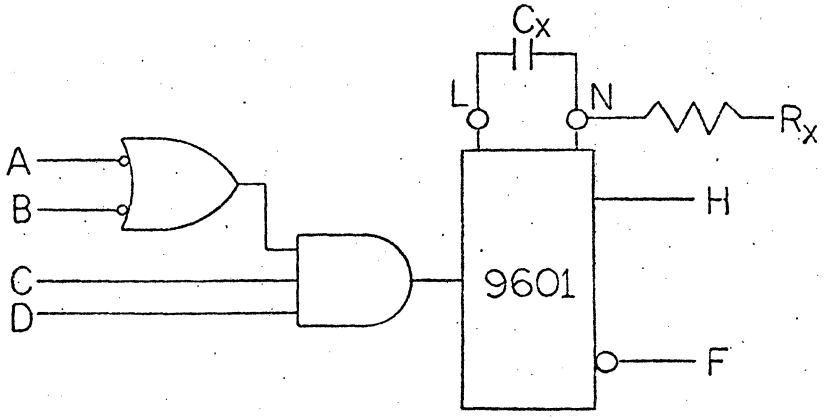
C > 1000 pf, R is Kohms, C in pf, T in ns.
R and C are the external timing resistor and capacitor.

TAON

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

[For $C_X \geq 10^3$ pF, $t = 0.32\ R_X C_X \left(1 + \frac{0.7}{R_X}\right)$]





LOGIC DIAGRAM

IHCN

3.2 TTL/DTL Integrated Circuits

Element Type:	IHCN
Standard Assembly Number:	1471 4356
Manufacturer's Type:	DTL-9936
Circuit Designation:	DTL Hex Inverter
Description of Operation:	

DTL HEX INVERTER

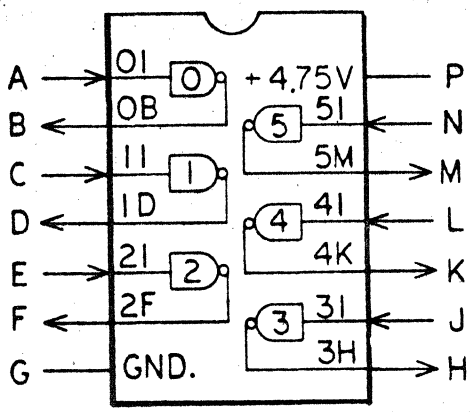
(1) Six Diode Transistor logic inverters with one input each are contained in 14 pin DIP package.

(2) Inputs:
Vi (Low) = +1.1 volt maximum
Vi (High) = +1.9 volt minimum
Iin (max) = -1.5ma at Vi (Low)
Iin (max) = +5μa at Vi (High)

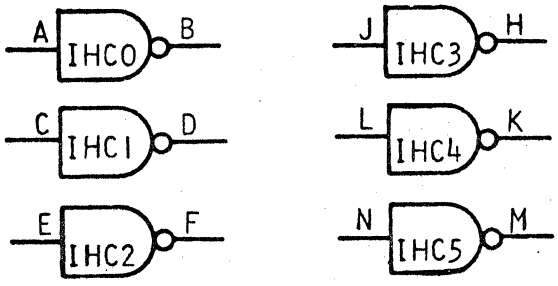
(3) Outputs:
Vo (Low) = +.6 volt maximum
Vo (High) = +2.6 volt minimum
Io (max) = -30ma at Vo (Low)
Io (max) = 300μa at Vo (High)

(4) Propagation Delay:
Negative input to positive output = 80ns maximum
Positive input to negative output = 35ns maximum

(5) Use the CTL to TTL interface circuitry for this DTL device.



PIN LOCATION DIAGRAM
14 PIN DIP



FUNCTIONAL DIAGRAM

IHDN

3.2 TTL /DTL Integrated Circuits

Element Type: IHDN
Standard Assembly Number: 1674 4963
Circuit Designation: TTL Open Collector
Description of Operation: Hex Inverter

TTL HEX INVERTER

(1) Six TTL inverter drivers with open collector, high voltage outputs are contained in a 14 DIP package.

(2) The inverter has high sink-current capability and can convert bipolar voltage levels to MOS levels.

(3) Input is fully compatible with TTL.

(4) Maximum voltage supply applied to the output through a resistor, Von = +30 volts.

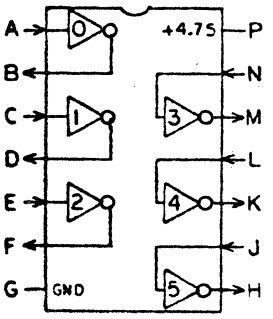
(5) At VCC = +4.75
Vin (Low) = +.8 volt maximum
Vin (High) = +2.0 volts minimum

(6) At VCC = +4.75, Voh = + 30 volts
Vout (Low) = +.7 volt maximum. Io = 40 ma maximum

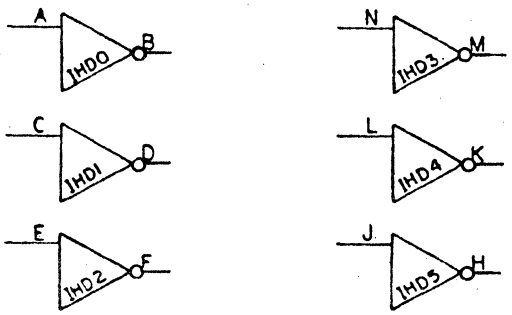
(7) At CL = 15pf, RL = 100 ohms, Voh = +20 volts:
Delay time from +1.5V level of input positive transition to 50% point of output negative transition, td = 15 ns max.

Delay time from -1.5V level of input negative transition to 50% point of output positive transition, td = 23 ns max.

(8) The interfacing rules in Section 5, Hardware Rules Book, should be complied with.



PIN LOCATION DIAGRAM
14 PIN DIP



FUNCTIONAL DIAGRAM

IDCN

3.2 TTL/DTL Integrated Circuits

Element Type: IDCN
Standard Drawing Number: S 1471 4398
Circuit Designation: Dual Expandable Nand Gate
Description of Operation:

1. Two DTL 4 input nand gates with an expander input are contained in a 14 pin dual in line package. The output is an open collector; thus a pull-up resistor is required.

2. The expander input allows increased number of inputs by addition of discrete diodes or other expander elements.

3. Inputs:

   a. $V_{iL} \leq 1.1V$

   b. $V_{iH} \geq 1.9V$

   c. $I_{iL} \leq |-1.5|$ mA @ $V_{iL} = +.4V$

   d. $I_{iH} \leq 5\ \mu A$ @ $V_{iH} = 4.0V$

4. Outputs:

   a. $V_{oL} \leq +.4V$ @ $I_{oL} = 36$ mA

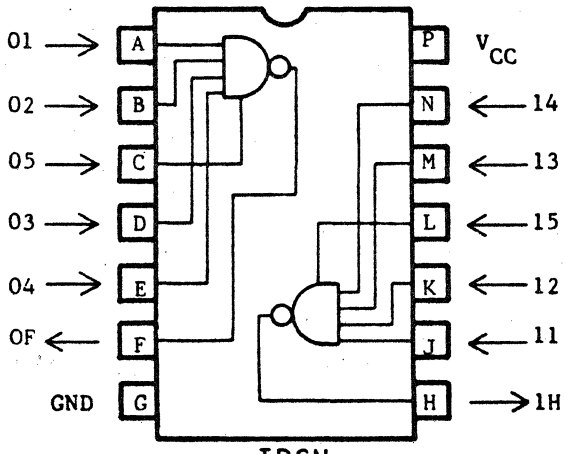
   b. Output leakage current $\leq 200\ \mu A$ @ $V_{oH} = 4.5V$

5. Propagation Delay:

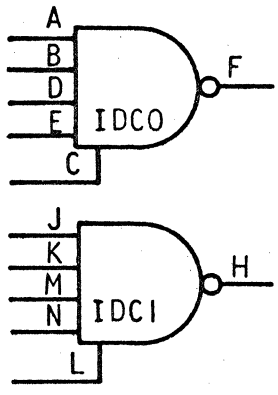
   a. Input (-) to output (+) ≤ 55 ns

   b. Input (+) to output (-) ≤ 35 ns

Pin Location Diagram:



IDCN



FUNCTIONAL DIAGRAM

Positive Logic:

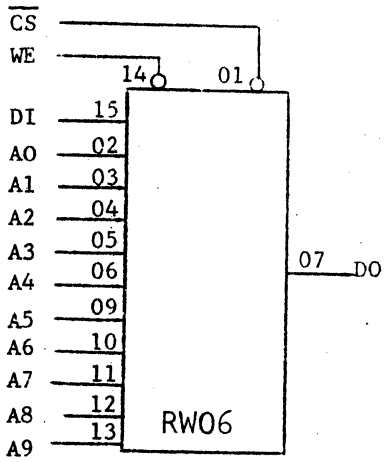
$$OF = \overline{01 \cdot 02 \cdot 03 \cdot 04 \cdot 05}$$

$$1H = \overline{11 \cdot 12 \cdot 13 \cdot 14 \cdot 15}$$

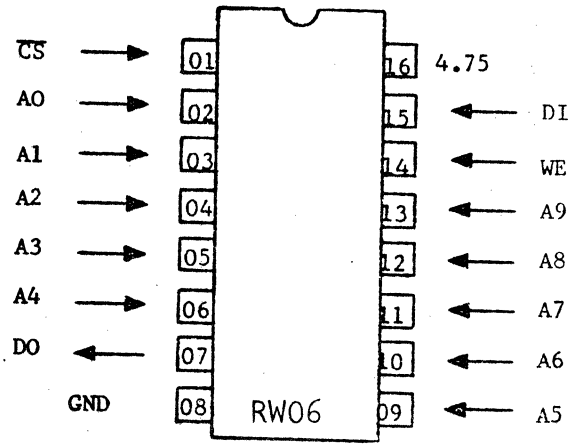
RW06

3.2 TTL/DTL Integrated Circuits

Element Type:	RW06
Standard Assy Number:	1449 1104
Manufacturer/Manufacturer's Type:	Fairchild/93415
Circuit Designation:	1024-Bit Memory
Description of Operation:	Open Collector



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM

RW06

1024 BIT RAM RW06 1449 1104

1. The device is a bipolar monolithic circuit organized as 1024 1 bit words. Inputs to the chip are ten active high address lines (A0 thru A9), one active low chip select line ($\overline{CS}$), an active low write enable line (WE) and one data input (DI). There is a single data output (DO).

2. A logic zero applied to the write enable input with a zero simultaneously at the chip select line will allow the data present at the input to be written into the addressed word.

3. When the WE input is held high and the chip is selected ($\overline{CS}$ is low), the data stored in the addressed memory location is available uninverted at the data output line DO.

4. The following table summarizes the device operation:

$\overline{CS}$	WE	FUNCTION
0	0	Write
0	1	Read
1	X	No action

Note: X = don't care.

5. Inputs shall always be driven by CTL restoring elements with an external pull down resistor, connected from the input of the memory to ground (not to V_{ee}). Consult Section 5 for interface information.

6. The output shall always be connected to fully threshold sensitive CTL restoring elements (those accepting 4th level). An external pull-up resistor, connected from the memory output to the V_{cc} supply voltage shall be used. Refer to Section 5.3 for details.

7. The open collector output can be wire-ORed with other packages.

8. Maximum address access time t_{da} = 70 ns.

9. Maximum chip select access time t_{dcs} = 55 ns.

1024 BIT RAM RW06 1449 1104

10. The minimum address set-up time (t_{asu}) must be 20 ns and the minimum chip select set-up time must be 15 ns.

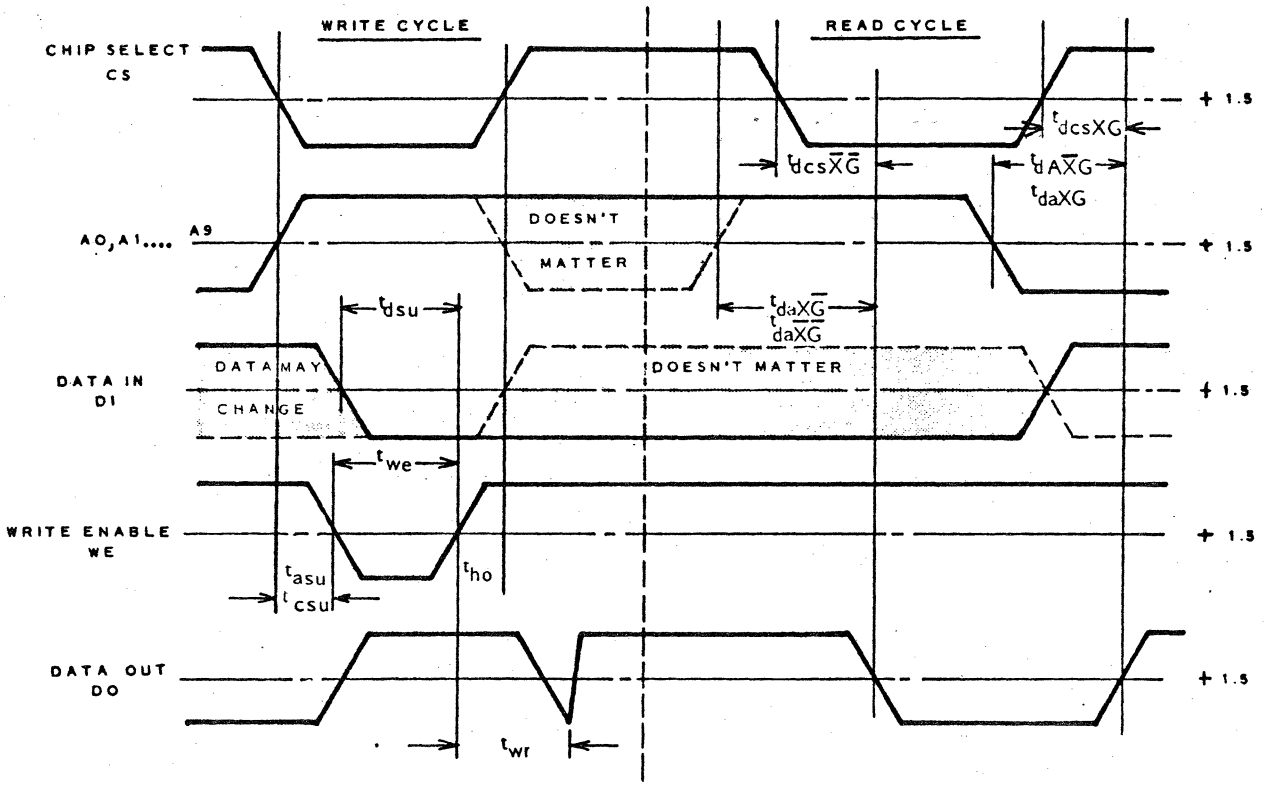
11. Both the address and chip select hold times (t_{ho}) must be greater than 15 ns.

12. Write enable pulse width must be a minimum of 55 ns.

13. Data set-up time relative to the positive going edge of WE pulse must be 60 ns minimum and data hold time relative to the same edge must be 15 ns.

14. Maximum write recovery time t_{wr} is 70 ns.

15. See the following page for the timing diagram.



NOTE: X & G is the positive going edge of the input and output pulse, respectively.
$\overline{X}$ & $\overline{G}$ is the negative going edge of the input and output pulse, respectively.

TIMING DIAGRAM

P001

3.2 TTL/DTL Integrated Circuits

Element Type:	P001
Standard Assembly Number:	1447 9455
Manufacturer/Manufacturer's Type:	Harris/7610-5 Signetics/82S26
Circuit Designation:	256 X 4 PROM OPEN COLLECTOR

Description of Operation:

1) The P001 is a 1024 bit field programmable read only memory organized as 256 4 bit words. There are eight address inputs A0,---A7, four open collector outputs Q0,---Q3, and two active low chip enable inputs CE1 and CE2.

2) The memory is enabled only if CE1 and CE2 are both at a low level. If either CE1 or CE2 is at a high level, the four outputs go high.

3) The outputs are open collector and therefore can be wire "ANDed" with a single pull-up resistor. See Section 5 for interface rules.

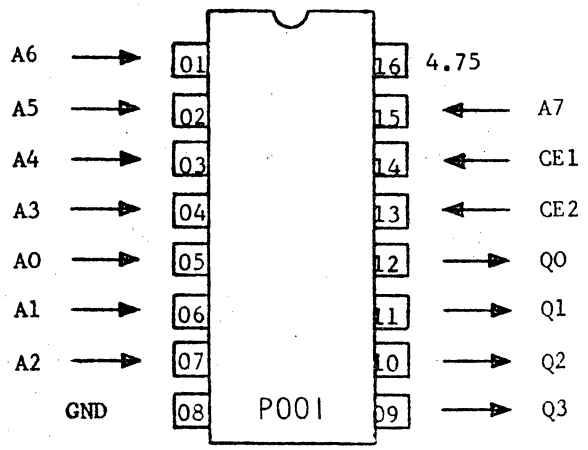
4) Input Currents
Iil = -1.6mA @ Vi = 0.4V Iih = .06mA @ Vi = 2.4V

5) Output Drive
Iol = 16mA @ Vo = .45V Ioh = .02mA @ Vo = 2.4V

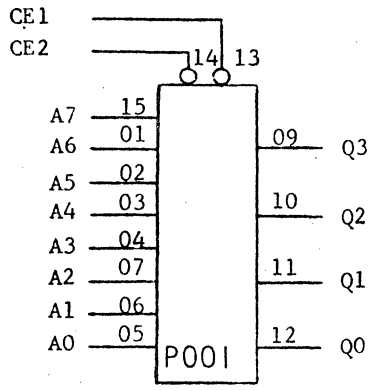
6) Maximum Address Access Time = 70nS.

7) Maximum Chip Enable Delay = 40nS.

8) For interface and programming information see Section 5.



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

P002

****OBSOLETE**** REPLACED BY PR08

3.2 TTL/DTL Integrated Circuits

Element Type:	P002
Standard Assembly Number:	1449 2060
Manufacturer/Manufacturer's Type:	Signetics/82S23 Harris/JM 7602-5
Circuit Designation:	32 x 8 PROM

Description of Operation:

1) The P002 is a 256 bit field programmable read only memory organized as 32 8 bit words. There are five address inputs A0,...,A4, eight open collector outputs Q0,..., Q7, and an active low chip enable $\overline{CE}$.

2) If the chip enable is high, all eight outputs will go high.

3) The outputs are open collector and can therefore be wired "ANDed" with a single pull up resistor. See section 5 for interface rules.

4) Input Currents:

I_{IL} = -0.4 mA @ V_i = 0.45V I_{IH} = 0.08 mA @ V_i = 2.4V

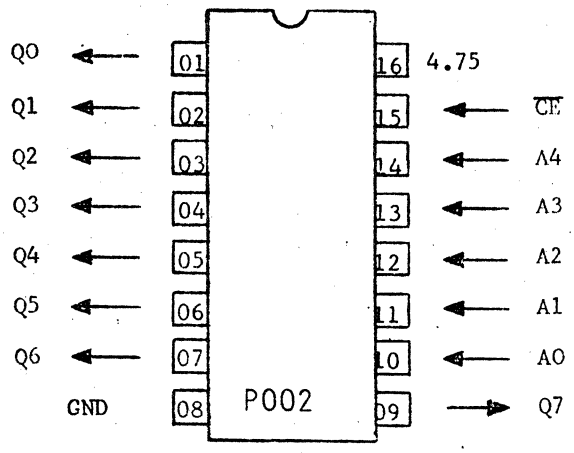
5) Output Drive:

I_{OL} = 16 mA @ V_o = 0.45V I_{OH} = .1 mA @ V_o = 2.4V

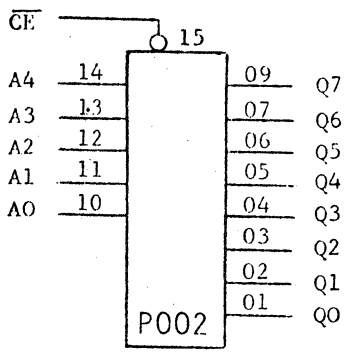
6) Propogation Delays:

Address Access Time	55 ns
Chip Enable Delay	35 ns

7) For interface and programming information consult Section 5.



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

S2-N

3.2 TTL Integrated Circuits

Element Type:	S2-N
Standard Assembly Number:	1447 3797
Manufacturer/Manufacturer's Type:	TI/74157
Circuit Designation:	FSC/9322
Description of Operation:	Quad 2-input Multiplexer

The S2-N features four 2-input multiplexers with common address and enable inputs. Each 2-input multiplexer has the capability of routing data from one of its two inputs to its totem pole output. A high on address input A selects the IA1, IB1, IC1, and ID1 inputs while a low on A selects the IA0, IB0, IC0, and ID0 inputs. Data on the selected input is presented uninverted at the output. For normal multiplexer operation a low level must be present on the enable input; a high level on the enable input disables the multiplexer by forcing all four multiplexer outputs to a low level. The S2-N comes in a 16 pin DIP.

Propagation Delay Times: (To Output)

Data to Output	t_{d+}	25 ns
	t_{d-}	18 ns
Enable to Output	t_{d+}	30 ns
	t_{d-}	25 ns
Select to Output	t_{d+}	35 ns
	t_{d-}	30 ns

TRUTH TABLE

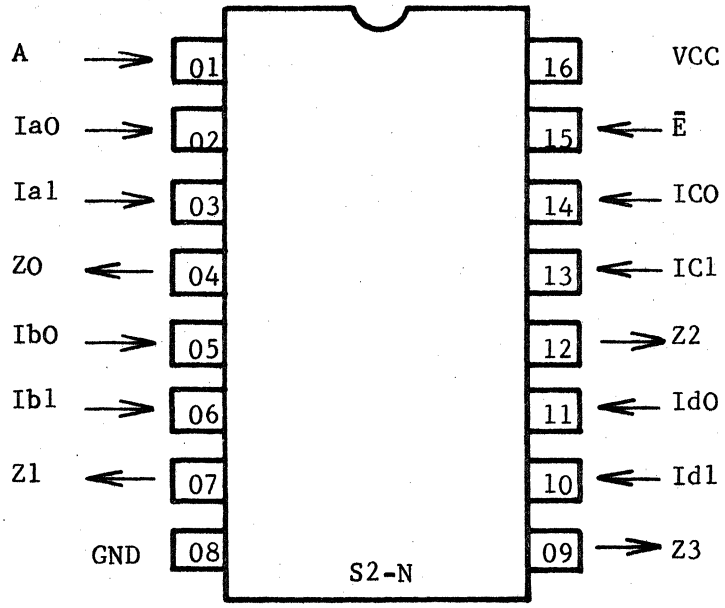
Enable	Select Input	Inputs		Output
$\overline{E}$	A	IX0	IX1	ZX
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

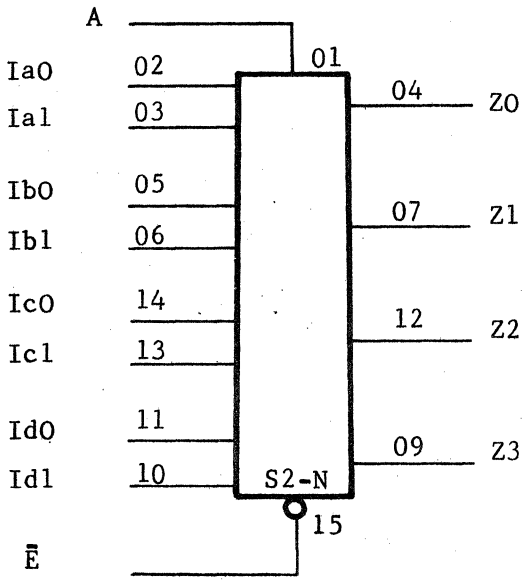
Logic Equation:

$$Z_X = (\overline{A}I_{X1} + SI_{X2}) \cdot \overline{E}$$

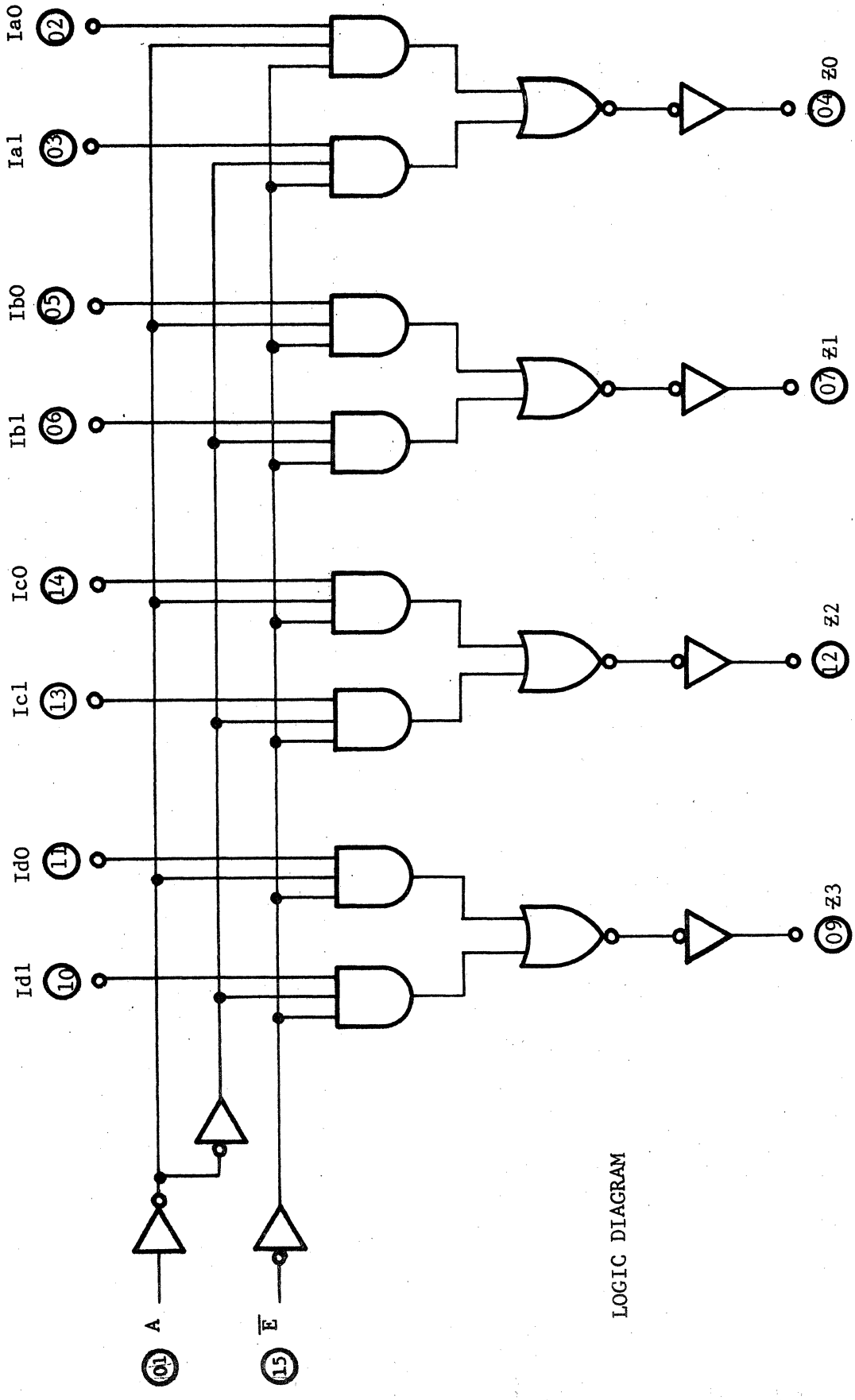
Pin Locations:

Top View





FUNCTIONAL DIAGRAM



LOGIC DIAGRAM

S4-N

3.2 TTL/DTL Integrated Circuits

Element Type:	S4-N
Standard Assembly Number:	1447 3714
Manufacturer/Manufacturer's Type:	T.I., Signetics/74153 Fairchild/93153
Circuit Designation:	Dual 4-Bit Data Selector

Description of Operation:

1) The S4-N consists of two 4-Input TTL multiplexers with common addressing A0 and A1, and independent active low enable inputs EA and EB. Data on the selected input (I0,I1,I2,I3) is routed non-inverted to the Totem Pole output Z.

2) For normal operation the appropriate enable must be at a low level. A high on the enable forces all outputs low regarless of the state of the data or the address inputs.

3) Input Currents:

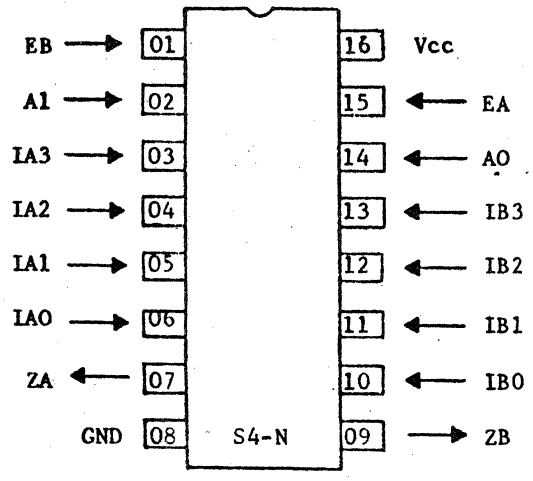
I_{IL} = -1.6 mA @ V_i = 0.4V I_{IH} = .04 mA @ V_i = 2.4V

4) Output Drive:

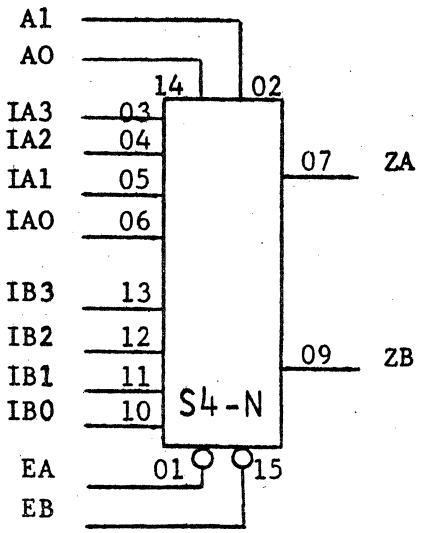
I_{OL} = 16 mA @ V_o = 0.4V I_{OH} = .04 mA @ V_o = 2.4V

5) Propagation Delays:

Data to Output	t_{pd+}	25 ns
	t_{pd-}	27 ns
Address to Output	t_{pd+}	41 ns
	t_{pd-}	38 ns
Enable to Output	t_{pd+}	37 ns
	t_{pd-}	27 ns



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

3.2 TTL/DTL Integrated Circuits

Element Type:	PR4N
Standard Assembly Number:	2319 5274
Manufacturer/Manufacturer's Type:	Fairchild/93417
Circuit Designation:	256 X 4 PROM OPEN COLLECTOR

Description of Operation:

1) The PR4N is a 1024 bit field programmable read only memory organized as 256 4 bit words. There are eight address inputs A0,---A7, two active low chip enables CS1 and CS2, and four open collector outputs Q0,---,Q3.

2) The memory is enabled only if CS1 and CS2 are both at a low level. When either chip enable is high all four outputs go high.

3) The four outputs are open collector and can therefore be wire "ANDed". Consult Section 5 for interface rules.

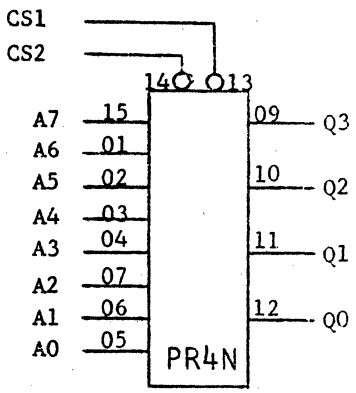
4) Input Currents
Iil = -0.4mA @ Vi = .4V Iih = .04mA @ Vi = 2.4V

5) Output Drive
Iol = 16mA @ Vo = .45V Ioh = .1mA @ Vo = 2.4V

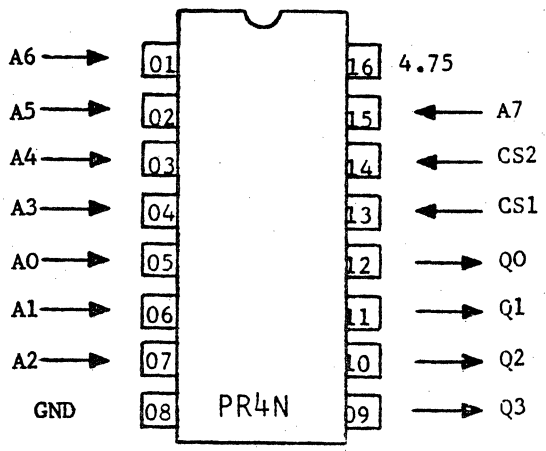
6) Maximum Address Access Time = 40nS.

7) Maximum Chip Enable Delay = 25nS.

8) Consult Section 5 for interface and programming information.



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM

PR5N

3.2 TTL/DTL Integrated Circuits

Element Type:	PR5N
Standard Assembly Number:	2319 5282
Manufacturer/Manufacturer's Type:	Fairchild/93436
Circuit Designation:	512 X 4 PROM
	OPEN COLLECTOR

Description of Operation:

1) The PR5N is a 2048 bit field programmable read only memory organized as 512 4 bit words. There are nine address inputs A0,---,A8, an active low chip select CS, and four open collector outputs Q0,---,Q3.

2) The memory is enabled when CS is at a low state. A high on CS causes all four outputs to go high.

3) The outputs are open collector and can therefore be wire "ANDed".

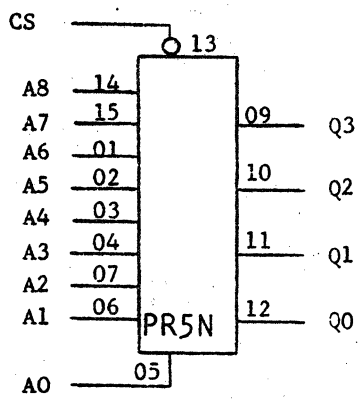
4) Input Currents
Iil = -0.4mA @ Vi = 0.45V Iih = .04mA @ Vi = 2.4V

5) Output Drive
Iol = 16mA @ Vo = .45V Ioh = .1mA @ Vo = 2.4V

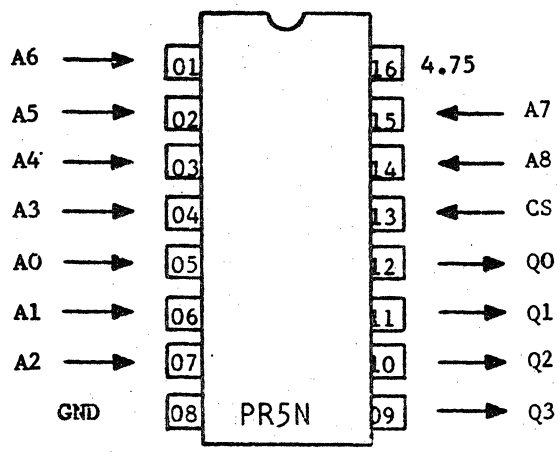
6) Maximum Address Access Time = 60nS.

7) Maximum Chip Enable Delay = 35nS.

8) For interface and programming information consult Section 5.



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM

LD4N

3.2 TTL/DTL Integrated Circuits

Element Type:	LD4N
Standard Assembly Number:	2602 2889
Manufacturer/Manufacturer's Type:	T.I./74S140
	Fairchild/9S140
Circuit Designation:	Dual 4-Input NAND Line Driver

Description of Operation:

1) The LD4N performs a dual 4-Input NAND function. Its high current Totem-Pole output stage can drive 40mA while maintaining a +2.0V true level output voltage and can sink 60mA while maintaining a +0.5V False level.

2) Input Currents:

I_{IL} = 4.0mA @ V_i = 0.5V I_{IH} = .08mA @ V_i = 2.4V

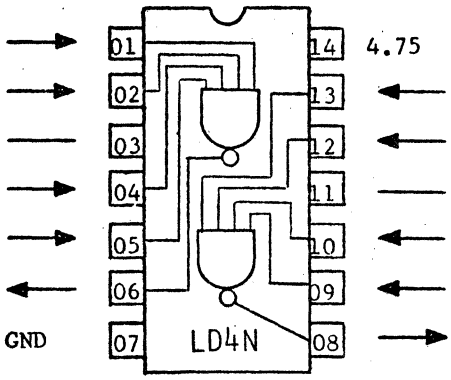
3) Output Drive:

I_{OL} = 60mA @ V_o = 0.5V I_{OH} = 40mA @ V_o = 2.1V

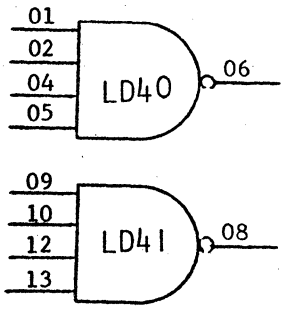
4) This device should not be used to directly interface to CTL elements because of considerably reduced low level noise margin.

5) Propagation Delays:

Input to Output tpd+ = 13 ns
tpd- = 13 ns



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

T3AH

3.2 TTL/DTL Integrated Circuits

Element Type:	T3AH
Standard Assembly Number:	1447 3557
Manufacturer/Manufacturer's Type:	T.I., Signetics/74H11 Fairchild/93H11
Circuit Designation:	Triple 3-Input AND Gate

Description of Operation:

1) The T3AH contains three TTL 3-Input AND functions in one 14 pin DIP. The outputs are Totem Pole.

2) Input Currents:

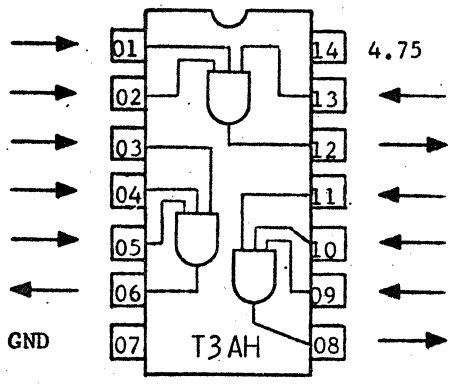
I_{IL} = -2.0 mA @ V_i = 0.4V I_{IH} = .04 mA @ V_i = 2.4V

3) Output Drive:

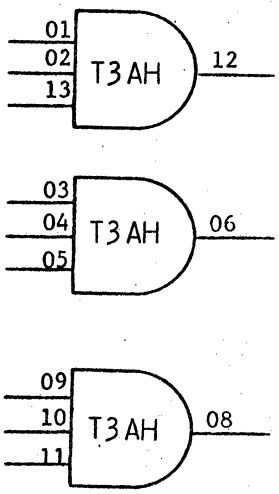
I_{OL} = 20 mA @ V_o = 0.4V I_{OH} = 2 mA @ V_o = 2.4V

4) Propagation Delays:

t_{pd+} = 19 ns
t_{pd-} = 16 ns



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

T2HN

3.2 TTL/DTL Integrated Circuits

Element Type:	T2HN
Standard Assembly Number:	1479 0240
Manufacturer/Manufacturer's Type:	T.I. Signetics/74H00 Fairchild/94H00
Circuit Designation:	Quad 2-Input NAND Gate

Description of Operation:

1) The T2HN contains four dual-input TTL NAND functions in one 14 pin DIP. The device has Totem Pole outputs.

2) Input Currents:

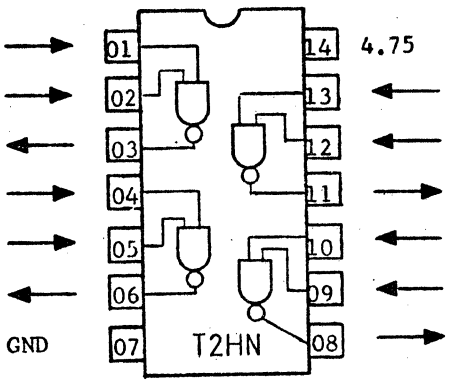
I_{IL} =-2.0 mA @ V_i = 0.4V I_{IH} = .04 mA @ V_i = 2.4V

3) Output Drive:

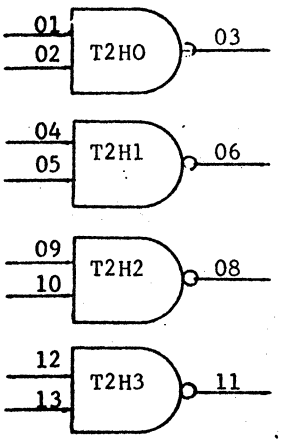
I_{OL} = 20mA @ V_o = 0.4V I_{OH} = 2 mA @ V_o = 2.4V

4) Propagation Delays:

tpd+ = 17 ns
tpd- = 14 ns



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

BTSN

3.2 TTL/DTL Integrated Circuits

Element Type:	BTSN
Standard Assembly Number:	1948 5051
Manufacturer/Manufacturer's Tupe:	National/DM8097 Signetics/8T97
Circuit Designation:	Tri-State Hex Buffer

Description of Operation:

1) The BTSN is a TTL Hex Buffer with tri-state inputs and outputs. In addition to having normal TTL 'True' and 'False' input and output levels, tri-state buffers have a high impedance OFF state. The inputs and outputs are brought to a high impedance state by placing the disable inputs at high level. Four of the buffers are controlled by one disable input DIS4 and the remaining two are controlled by DIS2.

2) Input Currents:

I_{IL} = -1.6mA @ V_i = 0.4V I_{IH} = .04mA @ V_i = 2.4V

High impedence state

I_{IL} = -.04 mA @ V_i = 0.5V I_{IH} = .04mA @ V_i = 2.4V

3) Output Drive:

I_{OL} = 38mA @ V_o = 0.4V I_{OH} =-5.2mA@ V_o = 2.4V

DC load of an output at the high impedance state

I_L = -.04 mA@ V_o = 0.4V I_H = .04mA @ V_o = 2.4V

4) Propagation Delays:

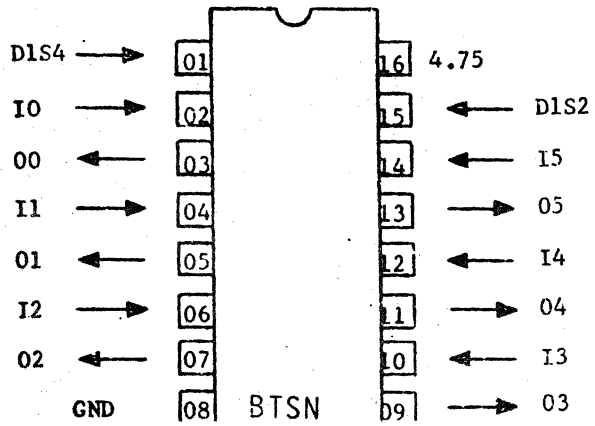
Data input to output tpd+ = 23 ns
tpd- = 26 ns

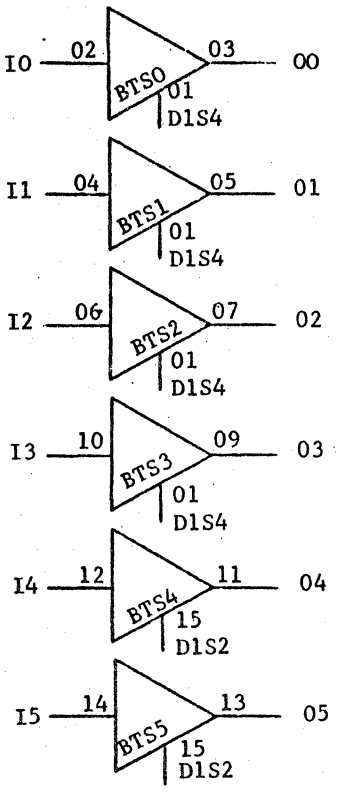
From a logic 1 Output On state to a high impedance Off state 25 ns

From a logic 0 Output On state to a high impedance Off state 33 ns

From a high impedance Off state to a logic 1 Output On state 40 ns

From a high impedance Off state to a logic 0 Output On state 45 ns





FUNCTIONAL DIAGRAM

CR4N

3.2 TTL/DTL Integrated Circuits

Element Type:	CR4N
Standard Assembly Number:	1447 3771
Manufacturer/Manufacturer's Type:	T.I./74161 Fairchild/9316
Circuit Designation:	4 Bit Binary Counter

Description of Operation:

1) The CR4N is a synchronous, presettable, 4-Bit binary counter. Inputs include clock (CK), an active-low clear ($\overline{CL}$), four parallel data inputs D0, ..., D3, and three mode controls: Load, Enable P, and Enable T. There are four data outputs, Q0, ..., Q3 and a carry output C. To count, all three mode controls must be high. Synchronous operation is achieved by utilizing a J-K Master-slave flip-flop arrangment for each bit with common clocking. When the clock is low, the data path to the master flip-flop is enabled, and this data is transferred to the slave and output on the LOW-to-HIGH level clock transition. When the clock is HIGH, the master is inhibited and the master-to-slave data path is enabled. During the HIGH-to-LOW level clock transition, the slaves are inhibited while the masters are enabled to accept new data. Presetting of the counter is accomplished by forcing the load input LOW. Loading is synchronous and occurs at the LOW-to-HIGH level clock transition, and the load input overrides the enable inputs. See the Mode Selection Truth table. The carry output is high only when all four outputs and the enable T input are HIGH. See the Carry Generation Truth table. In normal operation, HIGH-to-LOW level transition at enable P or T should only occur when the clock is HIGH, and LOW-to-HIGH level transitions at the load input with clock LOW should be avoided if the enable inputs are HIGH during the transition. N-bit counters can be realized with no additional elements by cascading CR4N packages. Clear is asynchronous.

2) Input Currents:

Clear, Enable P, Data

I_{IL} = -1.6mA @ V_i = 0.4V I_{IH} = .04mA @ V_i = 2.4V

Clock, Load, Enable T

I_{IL} = -3.2mA @ V_i = 0.4V I_{IH} = .06mA @ V_i = 2.4V

3) Output Drive:

Outputs Q0, ..., Q3

I_{OL} = 12mA @ V_O = 0.4V I_{OH} = 6mA @ V_O = 2.4V

Carry Output C

I_{OL} = 16mA @ V_O = 0.4V I_{OH} = 8mA @ V_O = 2.4V

4) Propagation Delays:

Clock to Output (Load input low)	tpd+	33 ns	
	tpd-	37 ns	
Clock to Output (Load input high)	tpd+	28 ns	
	tpd-	31 ns	
Clock to Ripple Carry	tpd+	44 ns	
	tpd-	43 ns	
Enable T to Ripple Carry	tpd+	23 ns	
	tpd-	23 ns	
Clear to Output	tpd-	46 ns	
Clear Recovery Time		28 ns	
Clear Pulse Width		24 ns	MIN
Clock Pulse Width		30 ns	MIN
Enable P and Data Set-up Time		22 ns	
Load Set-up Time		28 ns	
		0 ns	

CR4N

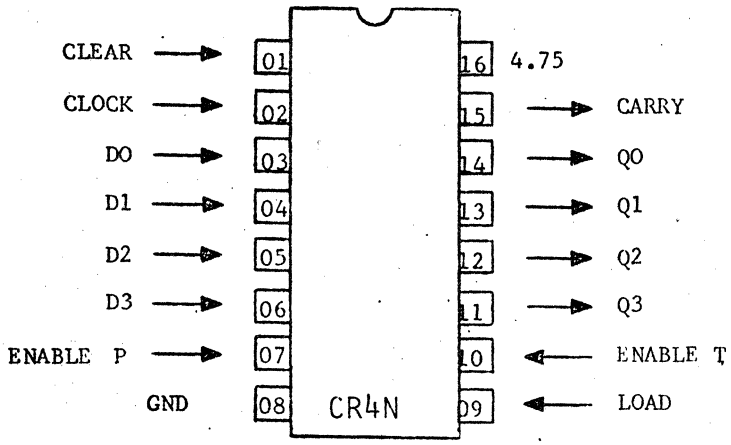
MODE SELECTION

CLEAR	LOAD	ENABLE P	ENABLE T	MODE
L	X	X	X	RESET
H	L	L	L	PRESET
H	L	L	H	PRESET
H	L	H	L	PRESET
H	L	H	H	PRESET
H	H	L	L	NO CHANGE
H	H	L	H	NO CHANGE
H	H	H	L	NO CHANGE
H	H	H	H	COUNT

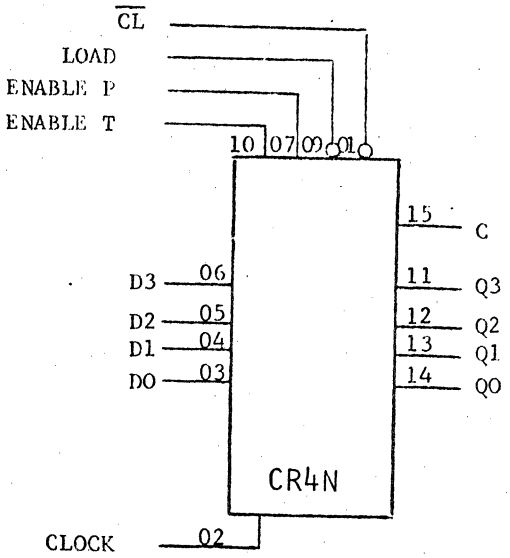
X = Don't Care

CARRY INPUT GENERATION

ENABLE T	(Q0.Q1.Q2.Q3)	CARRY OUTPUT
L	L	L
L	H	L
H	L	L
H	H	H



PIN LOCATION DIAGRAM

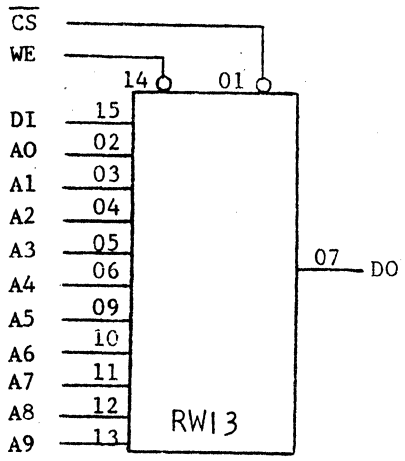


FUNCTIONAL DIAGRAM

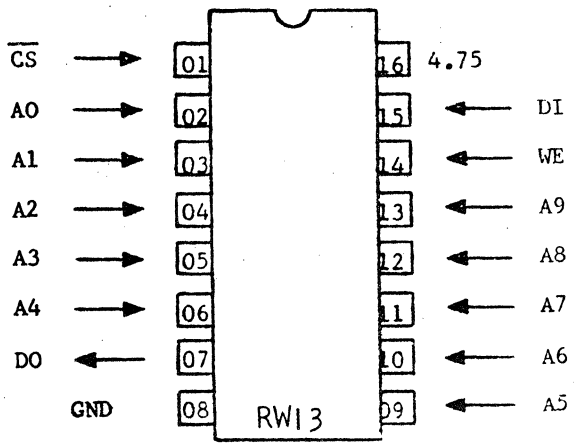
RW13

3.2 TTL/DTL Integrated Circuits

Element Type:	RW13
Standard Assy Number:	2540 0656
Manufacturer/Manufacturer's Type:	Fairchild/93415
Circuit Designation:	High Speed 1024 Bit Memory
Description of Operation:	Open Collector



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM

HIGH SPEED 1024 BIT MEMORY RW13 SA 2540 0656

1. The device is a bipolar monolithic circuit organized as 1024 1 bit words. Inputs to the chip are ten active high address lines (A0 thru A9), one active low chip select line ($\overline{CS}$), an active low write enable line (WE) and one data input (DI). There is a single data output (DO).

2. A logic zero applied to the write enable input with a zero simultaneously at the chip select line will allow the data present at the input to be written into the addressed word.

3. When the WE input is held high and the chip is selected ($\overline{CS}$ is low), the data stored in the addressed memory location is available uninverted at the data output line DO.

4. The following table summarizes the device operation:

$\overline{CS}$	WE	FUNCTION
0	0	WRITE
0	1	READ
1	X	NO ACTION

NOTE: X = Don't Care

5. Inputs shall always be driven by CTL restoring elements with an external pull down resistor, connected from the input of the memory to ground (not to V_{ee}). See Sec. 5 for interfacing rules.

6. The open collector output can be wire-ORed with other packages.

7. Maximum address access time t_{da} = 50 ns

8. Maximum chip select access time t_{dcs} = 35 ns

9. The minimum address set-up time (t_{asu}) must be 40 ns and the minimum chip select set-up time must be 40 ns.

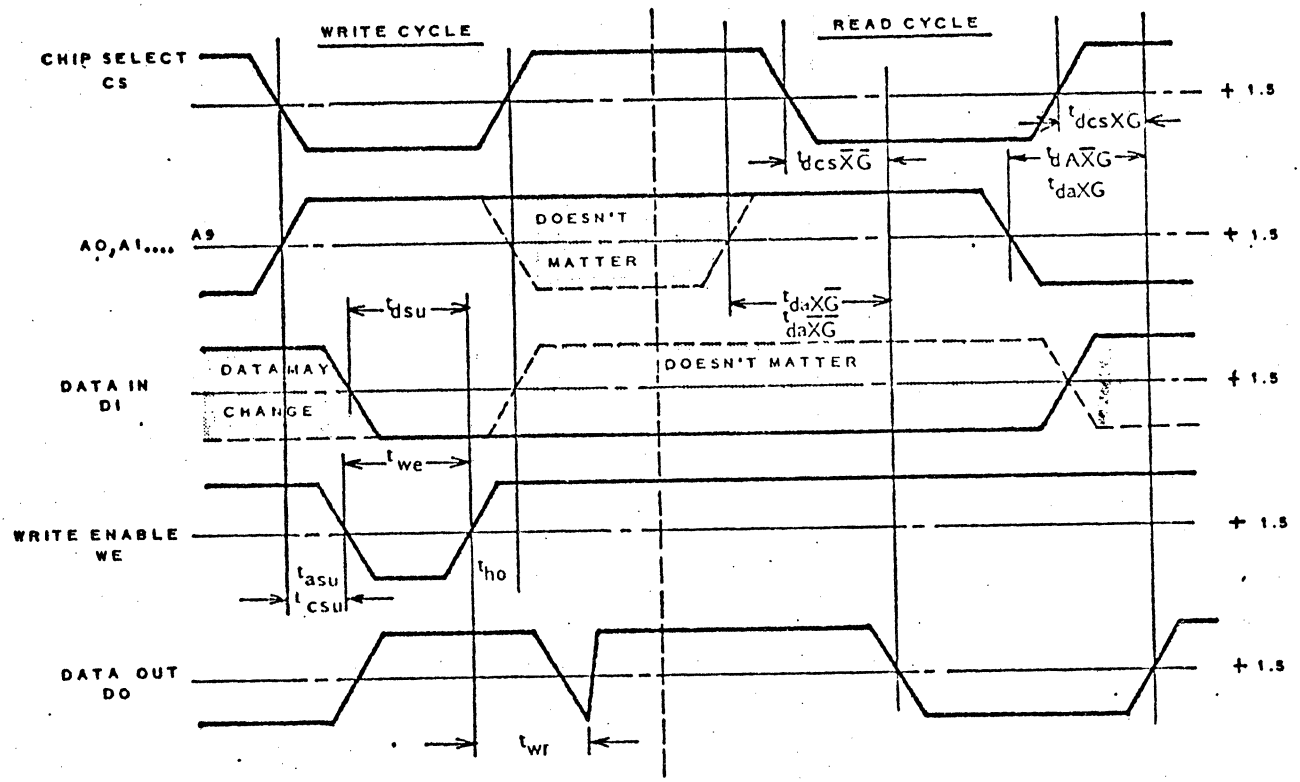
10. Both the address and chip select hold times (t_{ho}) must be greater than 10 ns.

11. Write enable pulse width must be a minimum of 40 ns.

12. Data set-up time relative to the positive going edge of WE pulse must be 40 ns minimum and data hold time relative to the same edge must be 10 ns.

13. Maximum write recovery time t_{wr} is 70 ns.

14. See the following page for the timing diagram.



NOTE: X & G is the positive going edge of the input and output pulse, respectively.
$\overline{X}$ & $\overline{G}$ is the negative going edge of the input and output pulse, respectively.

TIMING DIAGRAM

PR08

3.2 TTL/DTL Integrated Circuits

Element Type:	PR08
Standard Assembly Number:	2607 6075
Manufacturer/Manufacturer's Type:	Signetics/82S23 Harris/7602-5
Circuit Designation:	32 X 8 PROM OPEN COLLECTOR

Description of Operation:

1) The PR08 is a 256 bit field programmable read only memory organized as 32 8 bit words. There are five address inputs A0,---,A4, eight open collector outputs Q0,---,Q7 and an active low chip enable CE.

2) If the chip enable is high, all outputs will go high and the memory is disabled.

3) The outputs are open collector and can therefore be wire "ANDed" with a single pull-up resistor.

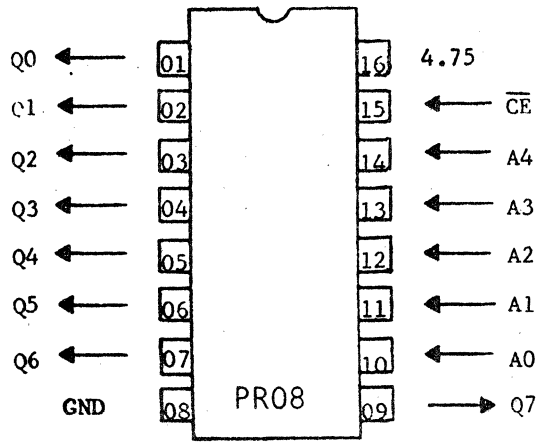
4) Input Currents
Iil = -.4mA @ Vi = .45V Iih = .08mA @ Vi = 2.4V

5) Output Drive
Iol = 16mA @ Vo = .45V Ioh = .1mA @ Vo = 2.4V

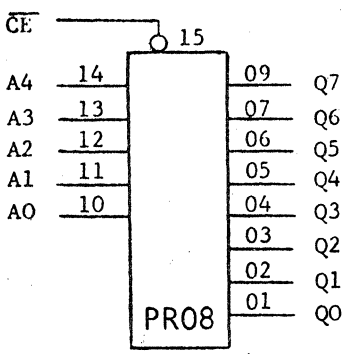
6) Maximum Address Access Time = 60nS.

7) Maximum Chip Enable Delay = 40nS.

8) For interface and programming information consult Section 5.



PIN LOCATION DIAGRAM

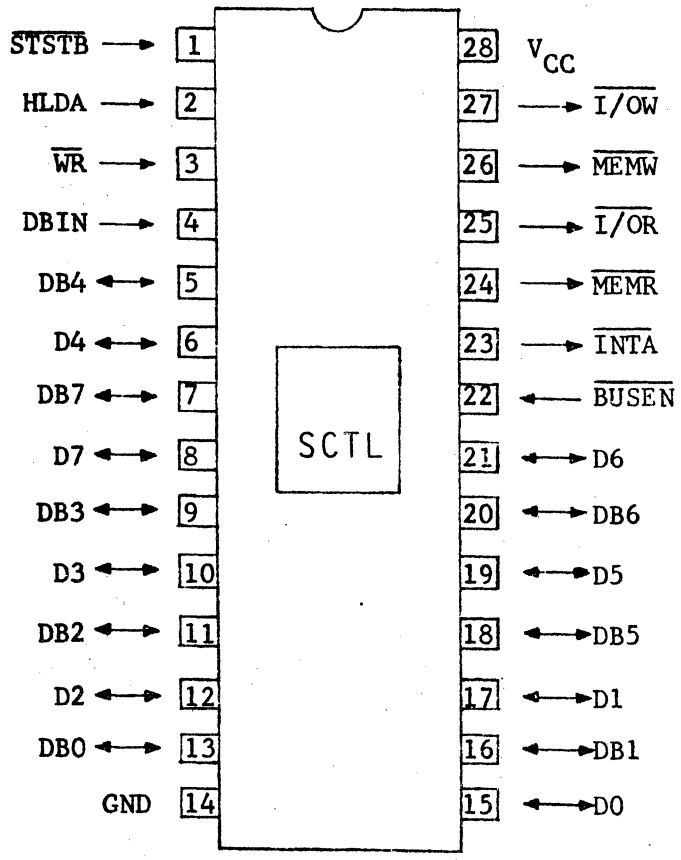


FUNCTIONAL DIAGRAM

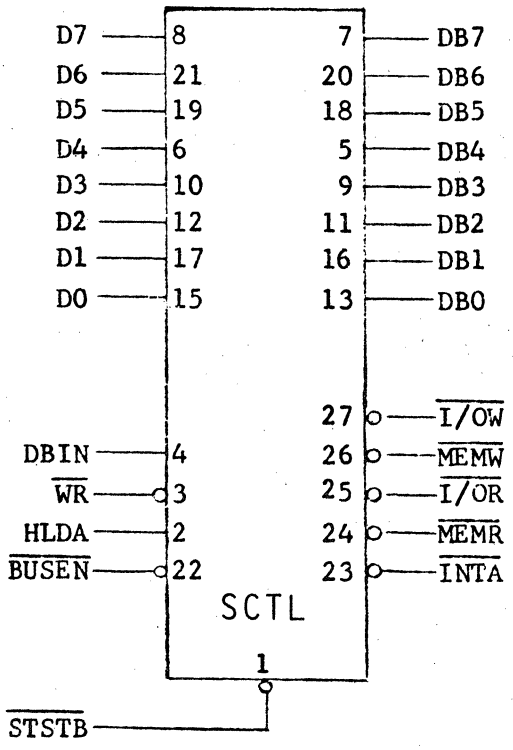
SCTL

3.2 TTL/DTL Integrated Circuits (Continued)

Element Type:	SCTL
Standard Assembly Number:	1959 5727
Manufacturer/Manufacturer's Type:	Intel/8228
Circuit Designation:	System Controller
Description of Operation:	



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

TTL SCTL 1959 5727

1) The SCTL is a Schottky Bipolar circuit in a 28 pin ceramic DIP. It is a single chip System Controller for use in microcomputer systems based on the 8080 microprocessor (MCPU). An 8 bit parallel Bi-Directional Bus Driver section provides isolation of the CPU Data Bus from memory and I/O. All driver outputs are tri-state with a high TTL fan-out capability on the system side. An 8 bit Status Latch stores "status" information during each machine cycle of the MCPU. A Gating Array decodes these status information together with other corresponding control signals from the MCPU, and issues accordingly control commands for the Bus Driver section and I/O commands for direct interface to the same family RAM, ROM, and I/O components.

2) The SCTL input/output pins are:

D7-D0	Data Bus input/output (MCPU side)
D87-D80	System Bus input/output (System side)
$\overline{\text{I/OR}}$	I/O Read output (to I/O components)
$\overline{\text{I/OW}}$	I/O Write output (to I/O components)
$\overline{\text{MEMR}}$	Memory Read output (to RAM's, ROM's, etc.)
$\overline{\text{MEMW}}$	Memory Write output (to RAM's, ROM's, etc.)
$\overline{\text{INTA}}$	Interrupt Acknowledge output (to interrupt control)
DBIN	Data Bus In input (from MCPU)
HLDA	Hold Acknowledge input (from MCPU)
$\overline{\text{WR}}$	Write control input (from MCPU)
$\overline{\text{BUSEN}}$	Bus Enable input
$\overline{\text{STSTB}}$	Status Strobe input

3) At the beginning of each machine cycle, the MCPU issues "status" information on its data bus. A Low on the Status Strobe ($\overline{\text{STSTB}}$) line stores this in the Status Latch.

4) The Gating Array generates the "Read" control outputs ($\overline{\text{MEMR}}$, $\overline{\text{I/OR}}$, $\overline{\text{INTA}}$) by gating the appropriate status bits with DBIN and HLDA. It also provides bus driver control to maintain proper bus flow on the bi-directional bus lines.

5) "Write" control outputs ($\overline{\text{MEMW}}$, $\overline{\text{I/OW}}$) are generated by the logical combination of the appropriate status bits with the $\overline{\text{WR}}$ input. Again, control is provided to direct bus flow. Correlation between the status word and the control outputs is shown in Table 1. All control outputs are active Low.

TTL SCTL 1959 5727

6) For "Read" operation, DBIN should be High. A Low on DBIN disables all control outputs to a High voltage level, and all 8080 data bus output buffers to their high impedance "off" state. A High on the HLDA input will disable the control outputs to High. It also interrupts the communication in the bi-directional bus section so that the CPU data bus outputs will maintain their current contents. D7-D0 outputs are latched.

7) For "Write" operation, $\overline{WR}$ should be Low. A High on $\overline{WR}$ will disable all control outputs to a High voltage level. It has no effect during the Read cycle.

8) A High on the $\overline{BUSEN}$ line will asynchronously force all control outputs and system data bus outputs to their high impedance "off" state. It has no effect on the CPU data bus outputs.

9) Electrical Characteristics

Input Threshold Voltages		
Vil maximum		0.8V
Vih minimum		2.0V
Output Voltages		
Vol maximum,	D7-D0	0.45V @ Iol = 2 mA
	all other outputs	0.45V @ Iol = 9 mA
Voh minimum,	D7-D0	3.6V @ Ioh = -10 uA
	all other outputs	2.4V @ Ioh = -1 mA
Input Loading		
Iil maximum,	$\overline{STSTB}$	-500 uA @ Vil = 0.4V
	D2, D6	-750 uA "
	all other inputs	-250 uA "
Iih maximum,	D87-D80	20 uA @ Vih = 2.4V
	all other inputs	100 uA "
Output Drive		
Iol maximum,	D7-D0	2 mA @ Vol < 0.45V
	all other outputs	10 mA " "
Ioh maximum,	D7-D0	-10 uA @ Voh > 3.6V
	all other outputs	-1.0 mA @ Voh > 2.4V
Off State Output Current		
Io(off) minimum		-100 uA @ Vo = 0.45V
maximum		100 uA @ Vo = Vcc
Supply Current Icc maximum		190 mA @ Vcc = 5.25V
Power Supply Voltage Vcc		5V ± 5%

TTL SCTL 1959 5727

10) Switching Characteristics

Status Strobe Pulse Width min.	tpw	25 ns
Status inputs D7-D0 Setup time, min.	tss	10 ns
Status inputs D7-D0 Hold time, min.	tsh	20 ns
Setup Time, System Bus inputs D87-D80 to HLDA, minimum	tds	10 ns
Hold Time, D87-D80 to HLDA, min.	tdh	20 ns
Propagation Delay Time, maximum		
$\overline{\text{STSTB}}$ to Control outputs	tdc	60 ns
$\overline{\text{DBIN}}$ to " "	trr	35 ns
$\overline{\text{WR}}$ to " "	twr	45 ns
DBIN to 8080 Data Bus D7-D0	tre	60 ns
Syatem Bus D87-D80 to 8080 Data bus during "Read"	trd	45 ns
$\overline{\text{D7-D0}}$ to D87-D80 during "Write"	twd	45 ns
$\overline{\text{STSTB}}$ to D87-D80	twe	45 ns
$\overline{\text{BUSEN}}$ to D87-D80	te	35 ns
HLDA to Control outputs	thd	30 ns

11) Interface Rules

The 8080A Data Bus has an input requirement of Vih min =3.3V and an output requirement of Iol max =1.9 mA. These conditions are guaranteed by the CPU Data bus outputs of the SCTL. Hence no external interface is required between the MCPU and the System Controller.

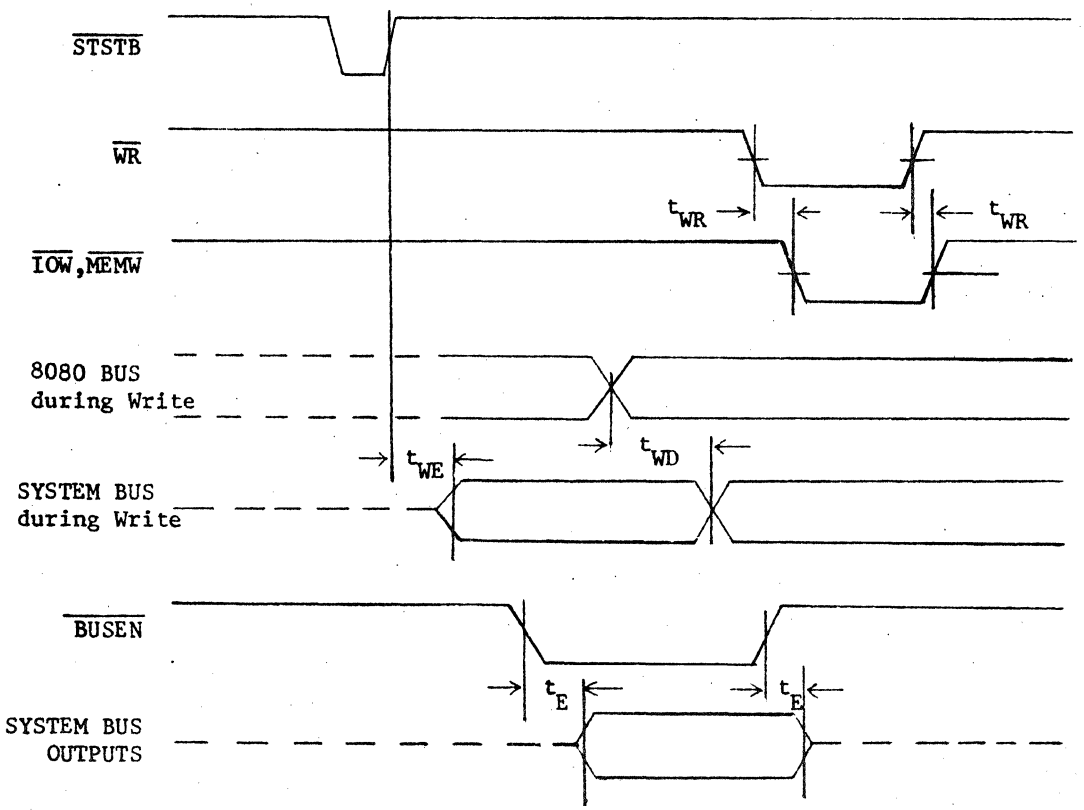
D7-D0 outputs are latched so that when HLDA is active (High), these bus lines will maintain their contents. All bus outputs are tri-state, a feature to facilitate DMA activities.

Interfacing to all input/output pins of the SCTL follows rules as defined for interfacing with TTL circuits, noting however, the difference in output drive capabilities of the CPU Data Bus outputs as compared to the others. As the SCTL is a Schottky device, the Low level output voltage limit is 0.45V instead of the 0.4V for standard TTL circuits.

TTL SCTL 1959 5727

TYPE OF MACHINE CYCLE		STATUS WORD ON CPU DATA BUS								CONTROL SIGNAL	
NAME	(N)	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	PREVIOUS STATE NOT INTA	PREVIOUS STATE INTA
Instr Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$	$\overline{INTA}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$	$\overline{INTA}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	NONE	$\overline{INTA}$
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$	$\overline{INTA}$

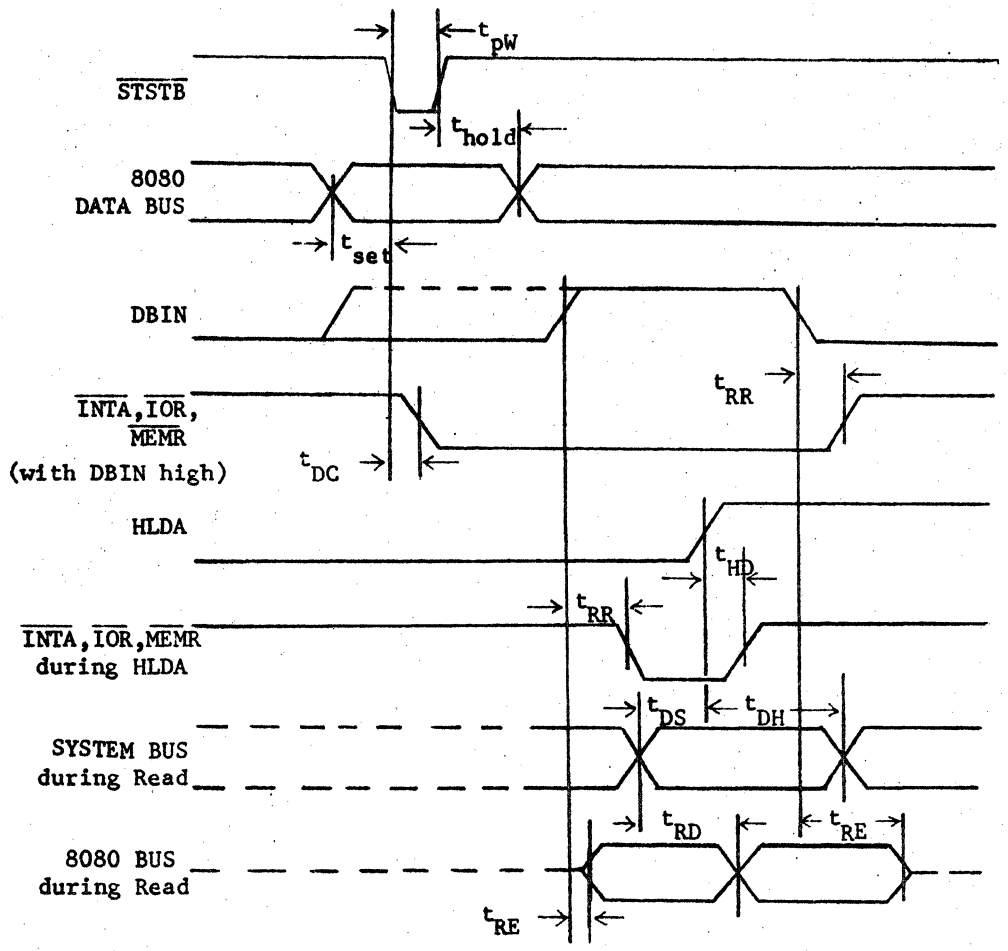
STATUS WORD CHART



WRITE TIMING

C_L = 100 pF

SCTL



C_L = 100 pF

READ TIMING

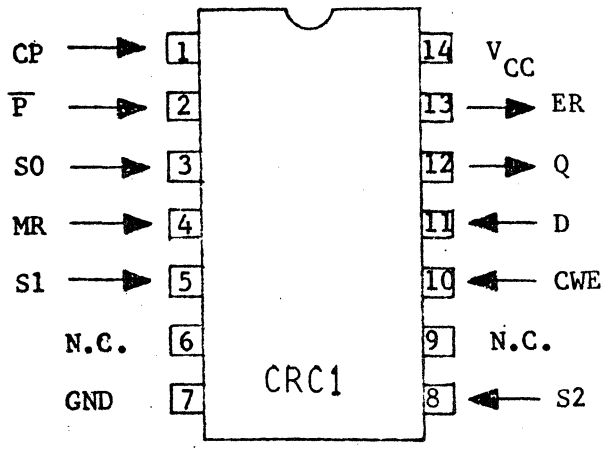
CRC1

3.2 TTL/DTL Integrated Circuits (continued)

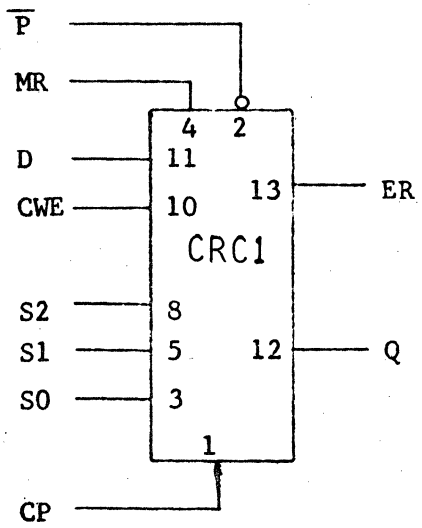
Element Type:	CRC1
Standard Assembly Number:	1269 7561
Manufacturer/Manufacturer's Type:	FSC/9401
Circuit Designation:	CRC Generator/Checker
Description of Operation:	

1) The CRC Generator/Checker is used for error detection in serial digital data transmission. It is a macrologic TTL chip in a 14 pin DIP. The input/output pins are:

S2-S0	Polynomial Select Inputs
D	Data Input
CP	Clock Input (operates on falling edge)
CWE	Check Word Enable Input
$\overline{P}$	Preset Input (Active Low)
MR	Master Reset Input
Q	Data Output
ER	Error Output



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

TTL CRC1 1269 7561

2) When used at the transmitter end, it accepts an input data stream via D when CWE is high. Data is entered at the falling edge of the clock CP. When CWE goes low, it signals the end of the data stream. A 16 bit check sum generated internally is then shifted out via Q, to be appended to the original data stream. This check sum is actually the remainder of dividing the data stream by a chosen polynomial. A set of eight polynomials can be choosed from, through the select inputs S2-S0. They are listed in Table 1.

SELECT CODE			CHECK POLYNOMIAL	REMARKS
S_2	S_1	S_0		
0	0	0	$X^{16} + X^{15} + X^2 + 1$	CRC-16
0	0	1	$X^{16} + X^{14} + X + 1$	CRC-16 REVERSE
0	1	0	$X^{16} + X^{15} + X^{13} + X^7 + X^4 + X^2 + X^1 + 1$	
0	1	1	$X^{12} + X^{11} + X^3 + X^2 + X + 1$	CRC-12
1	0	0	$X^8 + X^7 + X^5 + X^4 + X + 1$	
1	0	1	$X^8 + 1$	LRC-8
1	1	0	$X^{16} + X^{12} + X^5 + 1$	CRC-CCITT
1	1	1	$X^{16} + X^{11} + X^4 + 1$	CRC-CCITT REVERSE

Table 1

3) When used at the receiver end, the CRC1 monitors an input data stream plus the corresponding check sum via input D. If the input contains no error, the Error Output ER will go low. ER is valid only after the last check bit has been entered and remains so until the next high-low transition of CP or until the device has been preset or reset.

4) A high on the Master Reset (MR) asynchronously clears the 16 internal registers. A low on the Preset ($\overline{P}$) asynchronously sets all the registers for the case of 16 bit check polynomials; or only the most significant 12 or 8 registers for the case of 12 or 8 bit check polynomials, with the remaining bits being cleared.

TTL CRC1 1269 7561

5) Electrical Characteristics

Input Threshold Voltages	
Vil maximum	0.8V
Vih minimum	2.0V
Output Voltages	
Vol maximum	0.4V @ Iol = 4 mA
Voh minimum	2.4V @ Ioh = -400 uA
Input Loading	
Iil maximum	-0.25 mA @ Vil = 0.4V,
Iih maximum	40 uA @ Vih = 2.4V,
Output Drive	
Iol	4 mA @ Vol = 0.4V
Ioh	-400 uA @ Voh = 2.4V

6) Switching Characteristics

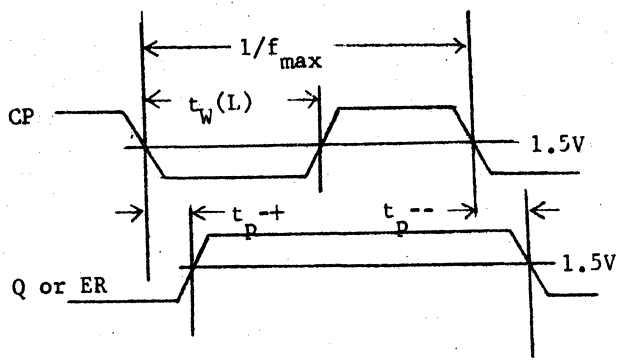
Clock Frequency		DC to 12 MHz
Minimum clock pulse width (low) tw(L)		35 ns
Propagation Delay, maximum		
Clock CP to Data output Q	td--	55 ns
	td-+	55 ns
Clock CP to Error output ER	td--	60 ns
	td-+	60 ns
Preset $\overline{P}$ to Q or ER	td-+	60 ns
Reset MR to Q ro ER	td+-	60 ns
Set-up Time, minimum		
Data D to Clock CP		55 ns
Check Word Enable CWE to CP		55 ns
Hold Time, minimum		
Data D to CP		5 ns
CWE to CP		5 ns
Preset pulse width, minimum		35 ns
Master Reset pulse width, minimum		35 ns
Recovery Time		
$\overline{P}$ or MR to CP, maximum		45 ns

TTL CRC1 1269 7561

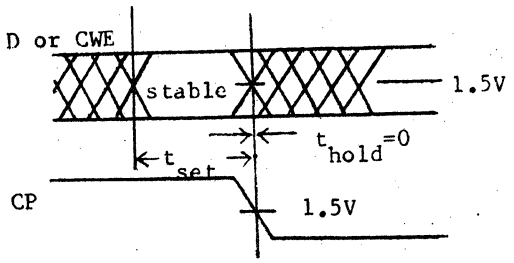
7) Interface Rules

Rules pertaining to standard TTL devices applies when interfacing the CRC1 with other circuits. Note that output drive capabilities in the False state is only about 3 TTL loads (taking 1.6 mA as a standard TTL Low level input load) instead of 10, common for other TTL devices.

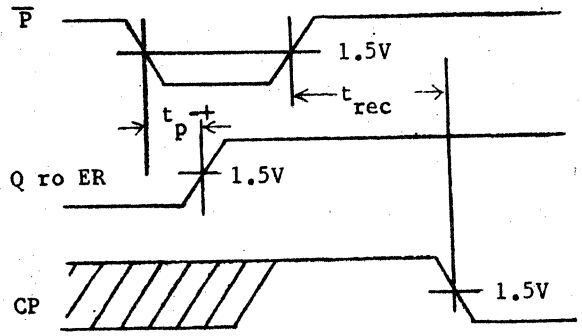
8) Functionality tests had been conducted on the CRC-CCITT check polynomial only. Use of this device under any other choice of polynomial must be consulted with Circuits.



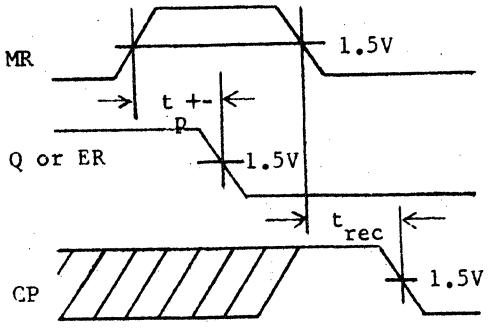
PROPAGATION DELAYS, CP TO Q OR ER



SET-UP AND HOLD TIMES, D AND CWE TO CP



PROPAGATION DELAYS, $\overline{P}$ TO Q OR ER;
RECOVERY TIME, $\overline{P}$ TO CP



PROPAGATION DELAYS, MR TO Q OR ER;
RECOVERY TIME, MR TO CP

C_L = 50 pF

TIMIMG DIAGRAMS

3.2 TTL/DTL Integrated Circuits (Continued)

Element Type:	B2CN
Standard Assembly Number:	1447 3581
Manufacturer/Manufacturer's Type:	TI,Signetics/7438 Fairchild/9N38
Circuit Designation:	Quad 2-Input NAND Buffer, open collector

Description of Operation:

1) The B2CN provides four 2-input NAND buffers in a 14 pin DIP. Each of the open collector outputs requires an external pull-up resistor to supply the TRUE level drive current. Outputs can be tied together to perform a wired positive AND function.

2) Input Loading

Iil = -1.6 mA @ Vil=0.4V Iih = 40 uA @ Vih=2.4V

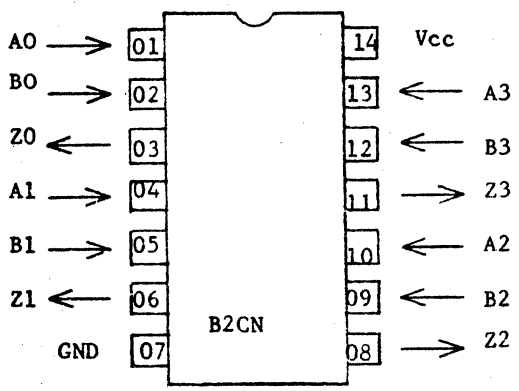
3) Output Drive

Iol = 48 mA @ Vol=0.4V Ioh = 250 uA @ Voh=2.4V

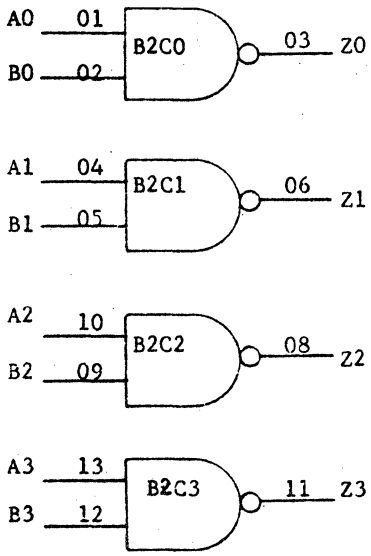
4) Output Voltage maximum 5.5V

5) Propagation Delay Times:

Input to Output	td-+	30 ns
	td+-	24 ns



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

3.2 TTL/DTL Integrated Circuits (Continued)

Element Type:	ITSN
Standard Assembly Number:	1948 5069
Maunfacturer/Manufacturer's Type:	NS/DM8098 Signetics/8T98
Circuit Designation:	Tri-State Hex Inverter

Description of Operation:

1) The ITSN is a TTL hex inverter with tri-state inputs and outputs in a 16 pin DIP. In addition to having normal TTL TRUE and FALSE input and output levels, it has a high impedance off state. The inputs and outputs are brought to this off state by placing the disable inputs at High. Four of the inverters are controlled by a single common disable input DIS4 and the remaining two by DIS2.

2) Input Loading

Iil = -1.6 mA @ Vil=0.4V Iih = 40 uA @ Vih=2.4V

High Impedance State (Inverter Inputs Only)

Iil(Hi-Z)= -40 uA @ Vil=0.5V Iih(Hi-Z)= 40 uA @ Vih=2.4V

3) Output Drive

Iol = 32 mA @ Vol=0.4V Ioh = -5.2 mA @ Voh=2.4V

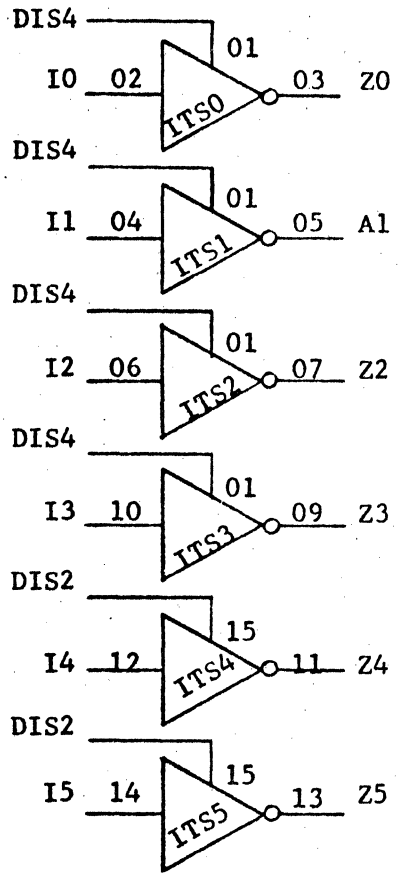
Output Loading in the High Impedance State

Iol(Hi-Z)= -40 uA @ Vol=0.4V Ioh(Hi-Z)= 40 uA @ Voh=2.4V

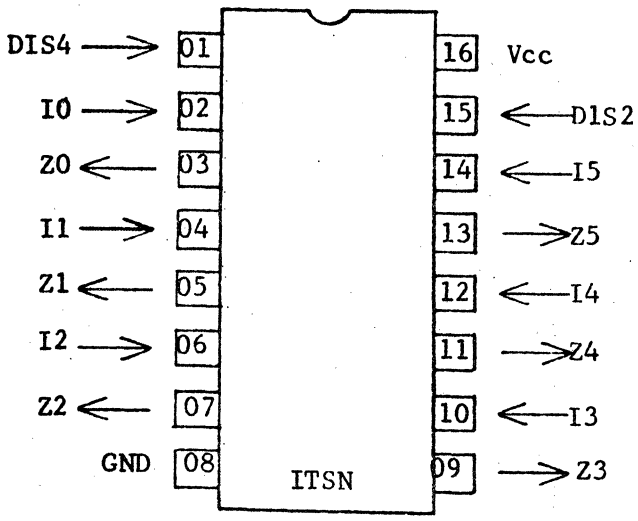
4) Propagation Delay Times:

Data Input to Output	td-+	23 ns
	td+-	22 ns
Output High On state to Hi-Z Off state	tHZ	17 ns
Output Low On state to Hi-Z Off state	tLZ	33 ns
Hi-Z Off state to Output High On state	tZH	41 ns
Hi-Z Off state to Output Low On state	tZL	43 ns

ITSN



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM

B2TS

3.2 TTL/DTL Integrated Circuits (Continued)

Element Type:	B2TS
Standard Assembly Number:	2602 7300
Manufacturer/Manufacturer's Type:	TI/74126
	NS/DM8094
Circuit Designation:	Quad Tri-State Buffer
Description of Operation:	

1) The B2TS provides four tri-state, single-input buffers in a 14 pin DIP. A separate control input Dn for each buffer is used to gate the output onto the high impedance state when the control input is Low. With the control input High, the other input simply passes the non-inverted data through the buffer.

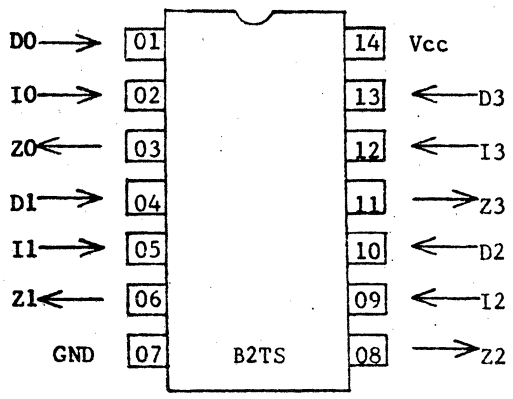
2) Input Loading
   Iil = -1.6 mA @ Vil=0.4V Iih = 40 uA @ Vih=2.4V

3) Output Drive
   Iol = 16 mA @ Vol=0.4V Ioh = -2 mA @ Voh=2.4V

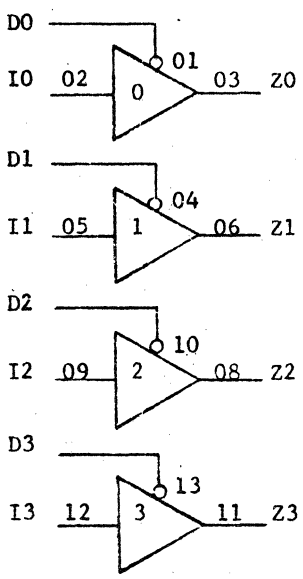
   Output Loading in the high impedance state
   Iol(Hi-Z)= -40 uA @ Vol=0.4V Ioh(Hi-Z)= 40 uA @ Voh=2.4V

4) Propagation Delay Times:

Data Input to Output	tpd+	22 ns
	tpd-	24 ns
Output High On state to Hi-Z Off state	tHZ	25 ns
Output Low On state to Hi-Z Off state	tLZ	24 ns
Hi-Z Off state to Output High On state	tZH	27 ns
Hi-Z Off state to Output Low On state	tZL	31 ns



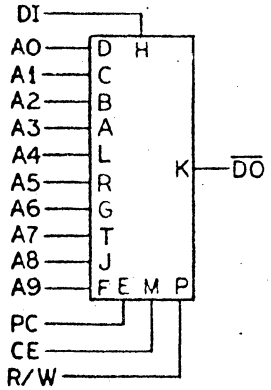
PIN LOCATION DIAGRAM



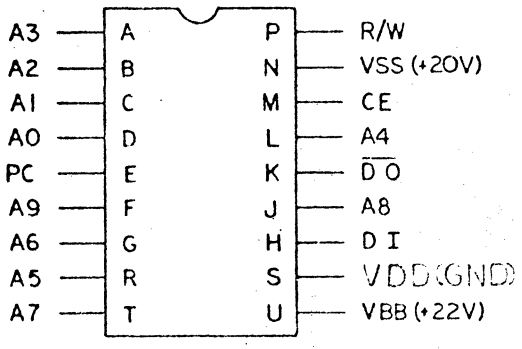
RAM1

3.3 MOS INTEGRATED CIRCUITS (continued)

Element Type:	RAM1
Standard Assembly Number:	1674 5150
Circuit Designation:	1024 BIT MEMORY



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM

18 PIN DIP

MOS

RAM 1

SA16745150

1024-BIT MOS DYNAMIC MEMORY

(1) MOS silicon gate, 1024 words by 1 bit random access memory chip, fully decoded, and packaged in 18 pin DIP.

(2) The information is retained in the form of a voltage on the capacitance of an internal node - Since the voltage will decay with time due to leakage, each cell in the array must be refreshed before a certain maximum period of time has elapsed, and this is why it is called a Dynamic memory.

(3) Three power supplies will be used:
Vdd, Drain voltage = GND
Vss, Source voltage = +19V
Vbb, Substrate voltage = +23V

(4) Inputs are: 10 address lines A0 thru A9, Precharge input (PRE), Chip Enable (CE), Read/Write (R/W), and Data input line (DI).

(5) Address, Clock and Data input voltages are:
VH = +19 volts minimum
VL = +3 volts maximum

(6) The memory cycle is controlled by two negative clock signals called Precharge and Chip Enable. The writing of new information is controlled by a third negative clock signal called Write Enable.

(7) Readout is non-destructive and the output voltage swing = 40mv minimum at RL = 100Ω and CL = 100pf.

(8) Data written in the memory is inverted at the output.

(9) The memory requires periodic data refreshing which is accomplished by cycling through Read Cycle A0 thru A4 inputs at least every 2 milliseconds.

(10) Precharge signal can be applied in the absence of CE without affecting stored data. CE, however, cannot be applied in the absence of PC signal without destroying stored data.

(11) For interfacing with CTTL, high voltage drivers are used at all inputs and sense amplifiers at the output.

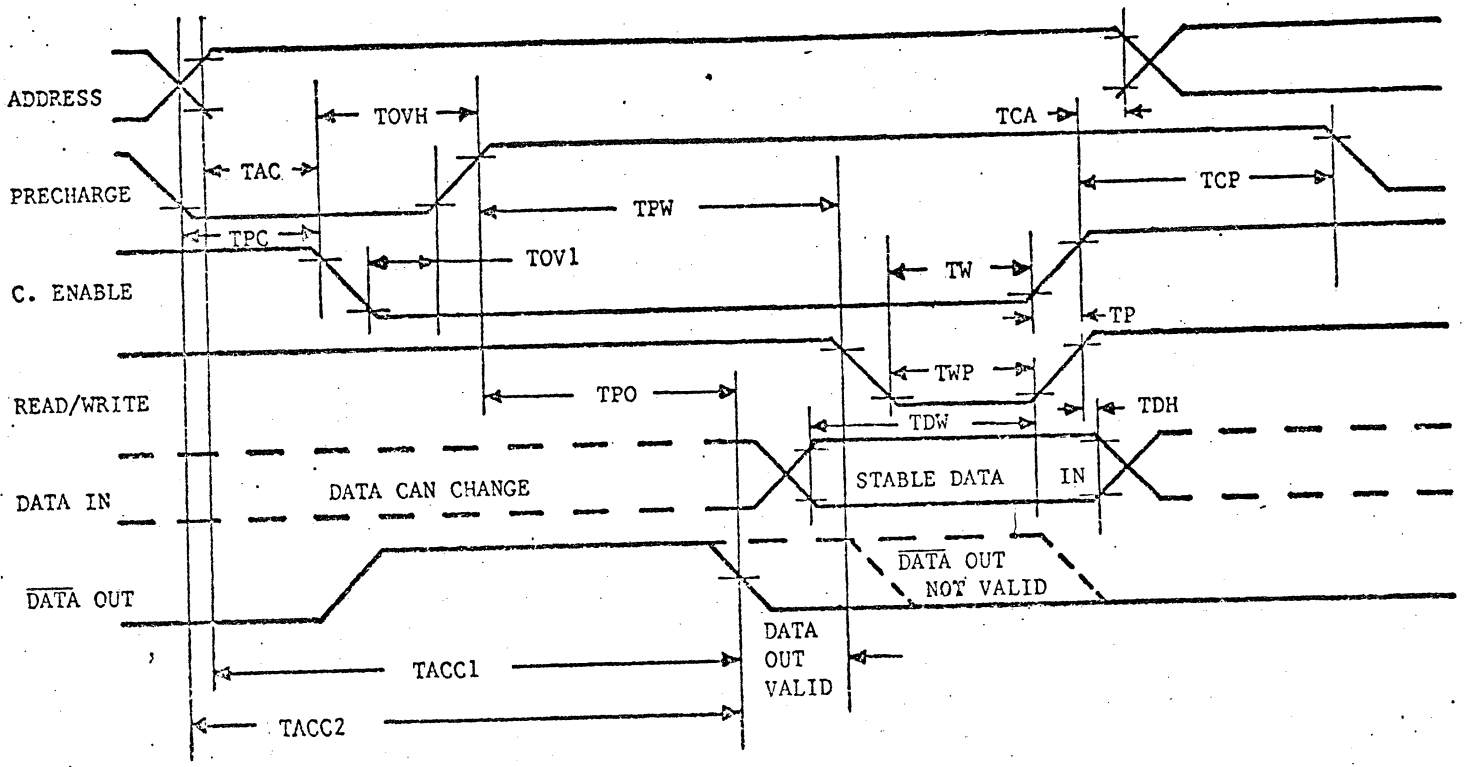
(12) Memory outputs offer the possibility of wire-OR connection.

(13) For timing see READ/WRITE cycle.

RAMI

READ/WRITE CYCLE

MOS DYNAMIC MEMORY



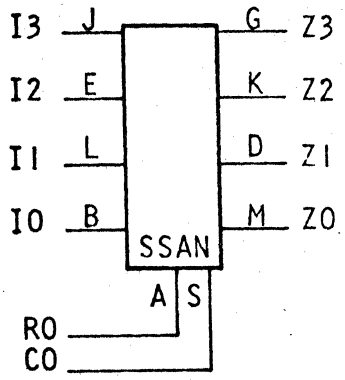
TAC (address to cenable set up time)= 30nS MIN
TPC (precharge to cenable delay)= 60nS MIN
TOVH (precharge & cenable overlap, high)= 80nS MAX
TOV1 (precharge & cenable overlap, low)= 5nS MIN
10 nS MAX
TPW (precharge to read/write delay)= 110nS MIN
500nS MAX
TWP (read/write pulse width)= 20nS MIN
TW (read/write set up time)= 20nS MIN

TDW (data set up time)= 40nS MIN
TDH (data hold time)= 10nS MIN
TP (relationship between cenable and read/write)= 0nS MAX
TCP (cenable to precharge delay)= 40nS MIN
TCA (cenable to address hold time)= 10nS MIN
TACC1 (address to output access)= 150nS MIN
TACC2 (precharge to output access)= 180nS MIN
TPO (end of precharge to output delay)= 75nS MAX

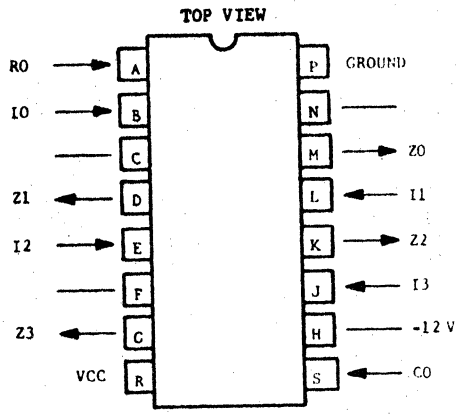
SSAN

3.3 MOS INTEGRATED CIRCUITS (continued)

Element Type:	SSAN
Standard Assembly Number:	2207 1716
Manufacturer's Type:	5061 D
Circuit Designation:	Quad 100 Bit Shift Register
Description of Operation:	



FUNCTIONAL DIAGRAM



PIN LOCATION DIAGRAM
16 PIN DIP

SSAN

QUAD 100-BIT SHIFT REGISTER

1. The SSAN is a Quad 100-Bit MOS Static Shift Register. Inputs to the chip are the 4 Data input lines, IO thru I3, the Clock line CO and the Recirculate input RO. Outputs are lines ZO thru Z3.

2. A logic one applied to the Recirculate input RO enables the recirculate function and disables the data inputs to the registers. A logic zero to the same line RO allows input data to be fed into the Registers.

3. The circuit operates with two power supplies V_{CC} and V_{GG}. V_{CC} is nominally 4.75V and V_{GG} is nominally -12V. V_{DD} shall be connected to ground.

4. Input levels for the Data and Recirculate inputs are compatible with CTL restored levels. A pull-down resistor, 287 OHMS to GROUND, is required to be connected to the CTL output driving the register inputs. The clock input is to be driven by a T^2L device with a pull-up resistor capable of supplying sufficient true level current @ Vin = 3.75v.

5. Output levels are compatible with CTL threshold sensitive inputs (4th level) Only 1 CTL load can be driven by each MOS Register output.

6. Maximum Data and Clock rate are 2.0 MHz.

7. Clock line normal state is a logic zero. A logic one activates the device. Data is fed into the register during the clock negative going transition. Data is available at the outputs after the clock negative going transition.

8. Minimum Clock pulse width is 240 ns. Maximum Clock pulse width is 10 μs.

9. Clock to Output delay is 295 ns, measured from the clock negative going transition.

10. Set-up time for all inputs (Data and Recirculate) is 120 ns measured relative to the clock negative going transition.

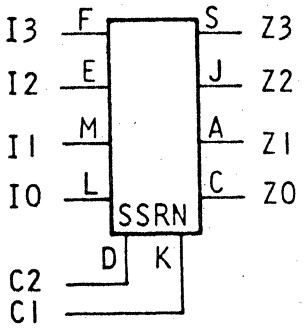
11. Hold time for all inputs (Data and Recirculate) is 60 ns, measured relative to the clock negative going transition.

12. Registers can be connected in parallel or in series to form any size of buffer desired.

SSRN

3.3 MOS INTEGRATED CIRCUITS (continued)

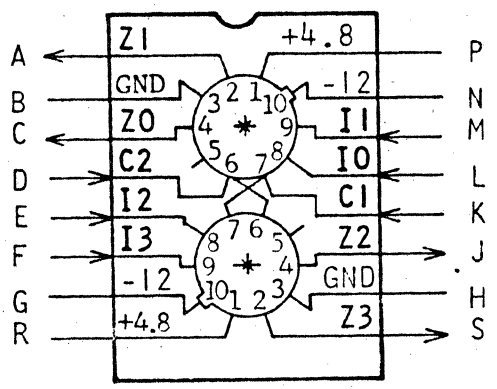
Element Type:	SSRN
Standard Assembly Number:	2204 9761
Circuit Designation:	Dual 100 Bit Shift Register
Description of Operation:	



FUNCTIONAL DIAGRAM

* THIS REPRESENTS A TMS3101LC

TOP VIEW



PIN LOCATION DIAGRAM FOR 2 SSRN
IN A 16 PIN JUMPER CHIPS

SSRN

MOS TMS 3101LC

SA 2204 9761

100 BIT SHIFT REGISTERS

1) SSRN is two Dual 100-Bit shift registers of TMS 3101LC type mounted on one DIP jumper chip and wired to use common clock lines C1 and C2. Inputs to the four shift registers are I0, I1, I2 and I3. The outputs are Z0, Z1, Z2 and Z3.

2) The Dual 100-Bit shift register is P-channel MOS low threshold device packaged in a hermetic 10 lead TO-100 can. It requires two-phase negative going non-overlapping clocks for its operation.

3) The circuit operates with two power supplies:

   VCC = +4.75 V $\pm$ 5%, VNN = -12 V $\pm$ 5%, and ground potential

4) Data present at the input during the positive-going transition of the clock C1 is the information that will be stored in the first storage element and the shifting cycle is completed during the negative period of C2.

5) C1 shall remain high and C2 low when the register is not shifting data.

6) Input levels:

   Data Input

   +2.5 V $\leq$ True Level $\leq$ +5.0 V
   False = +.55 volts minimum

   Clock Input

   +3.0 $\leq$ True $\leq$ +5.0 V
   -12.6 $\leq$ False $\leq$ -10.5 V

7) Input Capacitance:

   Data input Ci $\simeq$ 12 pf
   Clock input Ci $\simeq$ 55 pf

8) Clock:

   See Figure 6, page 14 for Clock Timing Waveforms.

9) Input set up time before the positive going edge of C1

   t = 155 ns Min.

10) Input hold time after the positive going edge of C1

    t = 15 ns Min.

MOS TMS 3101LC

SSRN

SA 2204 9761

100 BIT SHIFT REGISTERS (CON'T)

11) Propagation delay time after the negative going edge of C2

td = 125 ns max.

12) Output levels driving 1 CTuL load

True = +2.00 volt min.
False = +.25 volt max.

13) Possible CTuL to MOS interface for Data input is described in Figure 1.

14) Clock driver for Phase 2 and Phase 1 which can drive up to 8 dual MOS registers is described in Figures 2 and 4.

15) Registers can be connected in parallel or in series to form any size of buffer desired.

16) The -12V supply for these devices must be bypassed. The required amount of decoupling is one 0.47μf capacitor (part number 2010 2240) for every four individual dual 100 Bit Shift Registers. For the wire wrapped cards, the -12V supply must be bypassed by installing a capacitor as close as possible to the shift registers on the 0 side between an unused minus 12V power pin and the ground plane which surrounds the pin. For the etched cards, the capacitors are to be installed where provisions for discrete components are made near the -12V bus.

17) The clock driver circuit using a GB4N, GB7N, GB8N, and GB9N (Figures 4 and 5) shall be used wherever the system clock pulse width is 167 ns or less. Systems with a clock pulse width greater than 167 ns may use either of the two interface circuits.

SSRN

CTL → MOS INTERFACE FOR SSRN

FOR DATA LINES ONLY

DP1N - 8 DIODES, TYPE 13
RPNN - 13 500Ω RES.
RP2N - 13 2.5 KΩ RES.

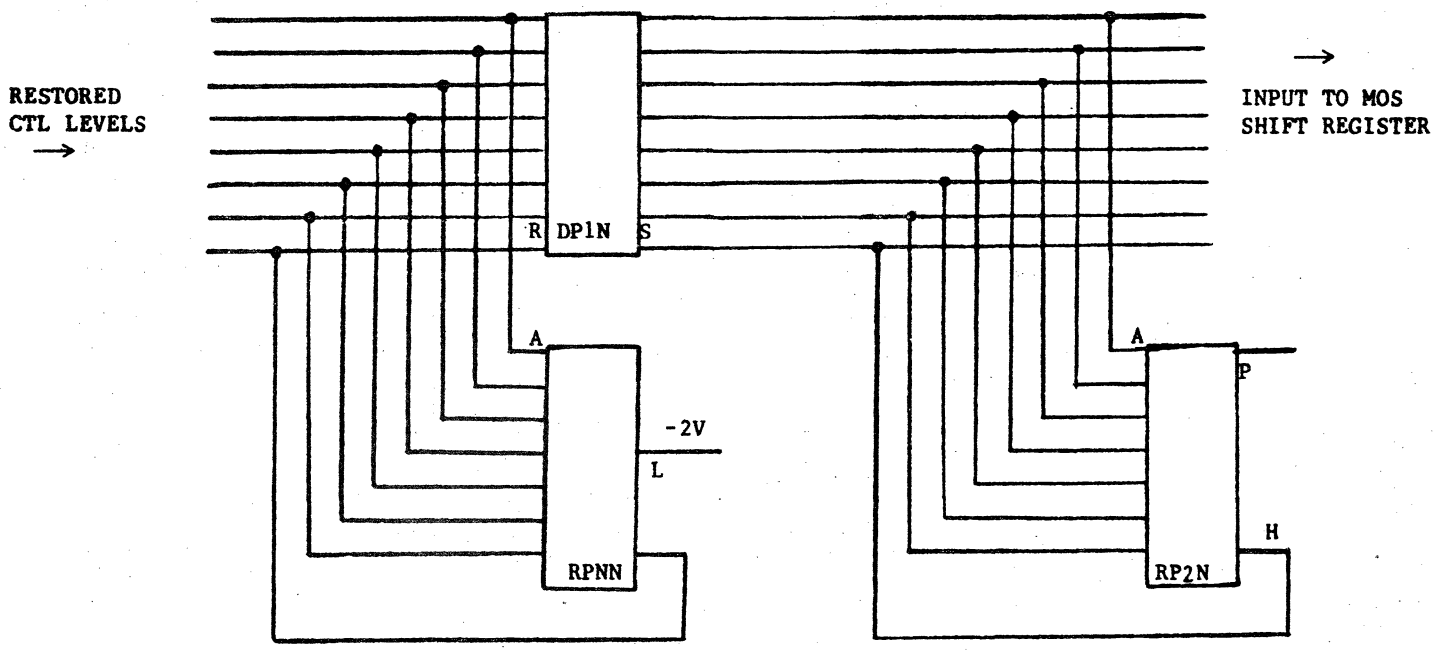


FIGURE 1

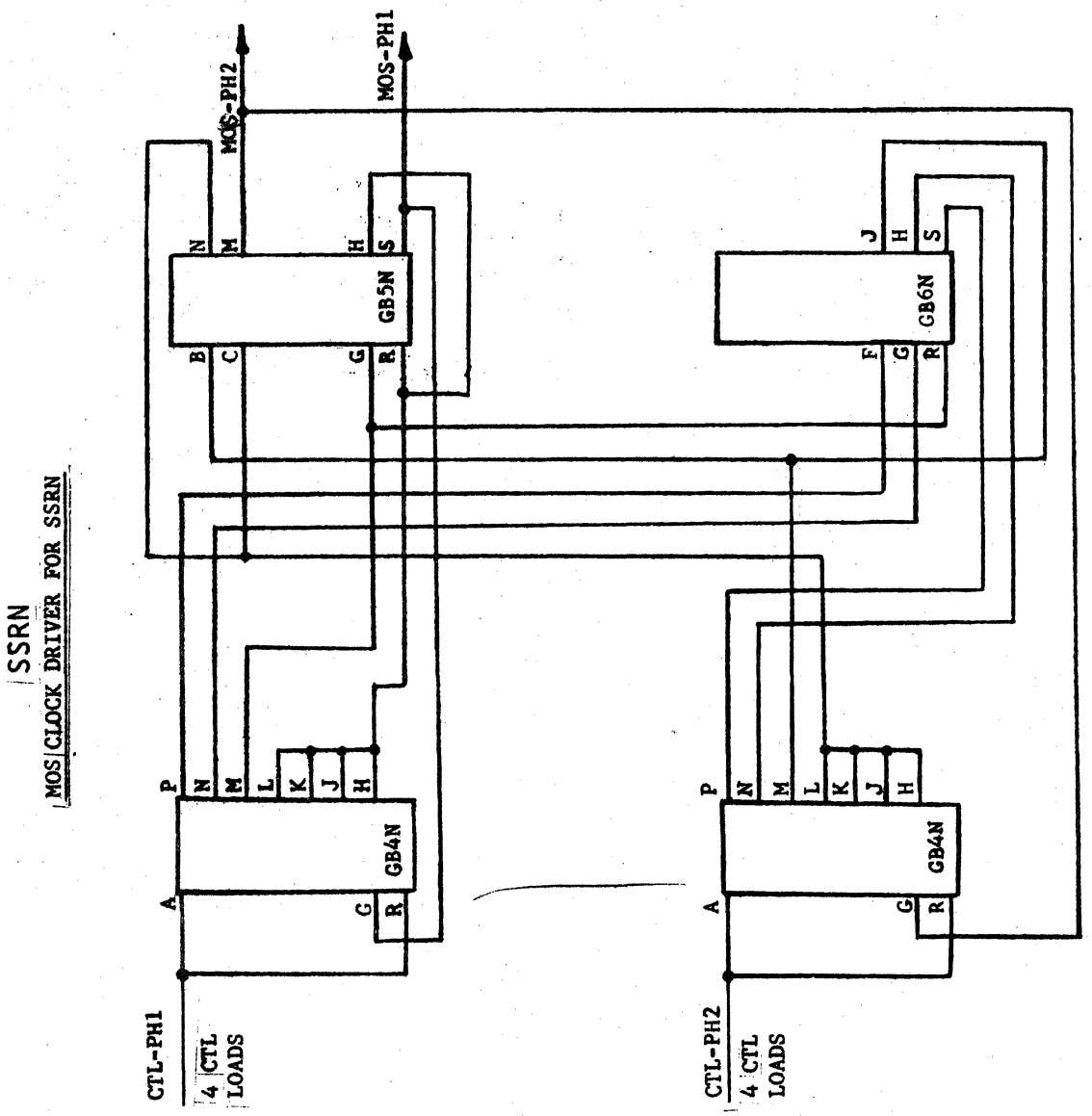


FIG. 2

GB4N: 7 Resistors (178,196, 681, 681, 1.47K, 1.47K, 1.47K) ½W,
One Diode (Type 4).

GB5N: Four type BJ transistors, 2 Resistors (287 Ohms).

GB6N: Two type AT transistors
Two 1μf capacitors
Two 287 Ohm Resistors

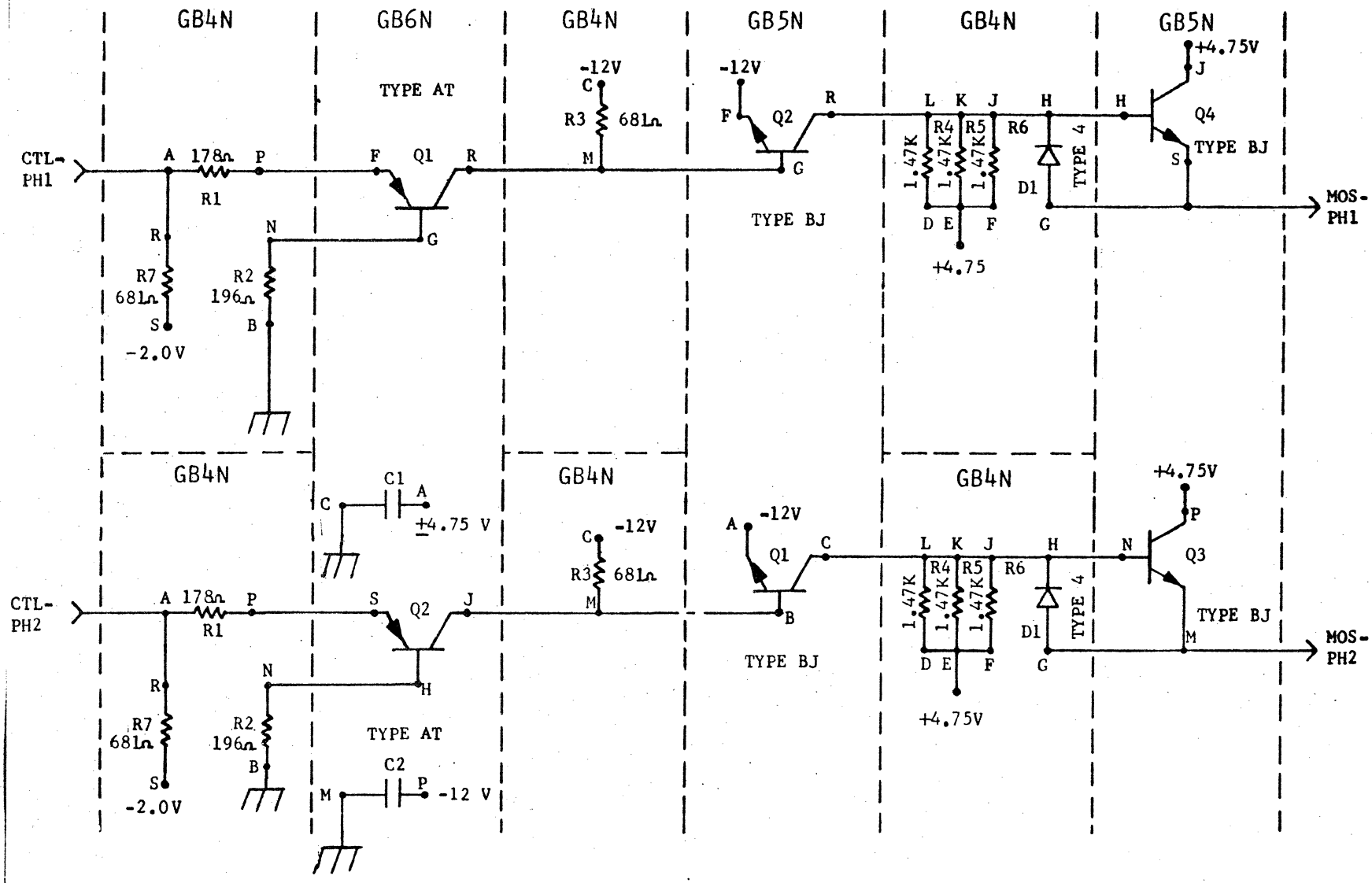


FIG. 3 DETAIL SCHEMATIC FOR MOS CLOCK DRIVER CIRCUITS PHASE 1 AND PHASE 2 USING GB4N, GB5N, GB6N INTERFACE.

SSRN

MOS CLOCK DRIVER FOR SSRN

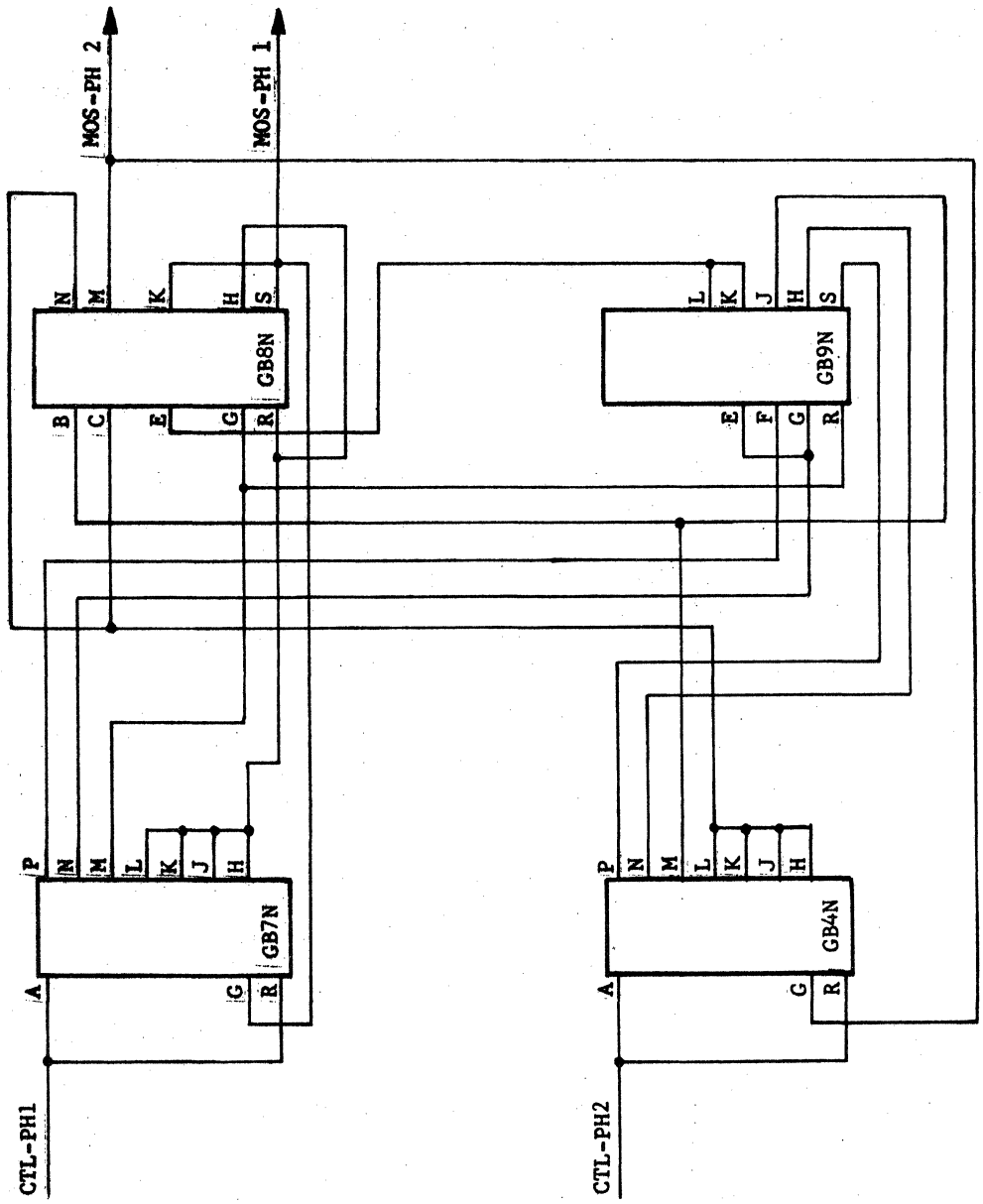


FIG. 4

GB4N: 7 Resistors (178, 196, 681, 681, 1.47K, 1.47K, 1.47K) 1/4 W, One Diode (Type 4).

GB7N: 7 Resistors (178, 750, 681, 681, 1.47K, 1.47K, 1.47K) 1/4 W, One Diode (Type 4).

GB8N: Four Type BJ transistors, one 82 pf capacitor, one 287 Ohm Resistor.

GB9N: Two Type AT transistors, Two 1 μf capacitors
One Type 23 Diode, One 3.16K Resistor.

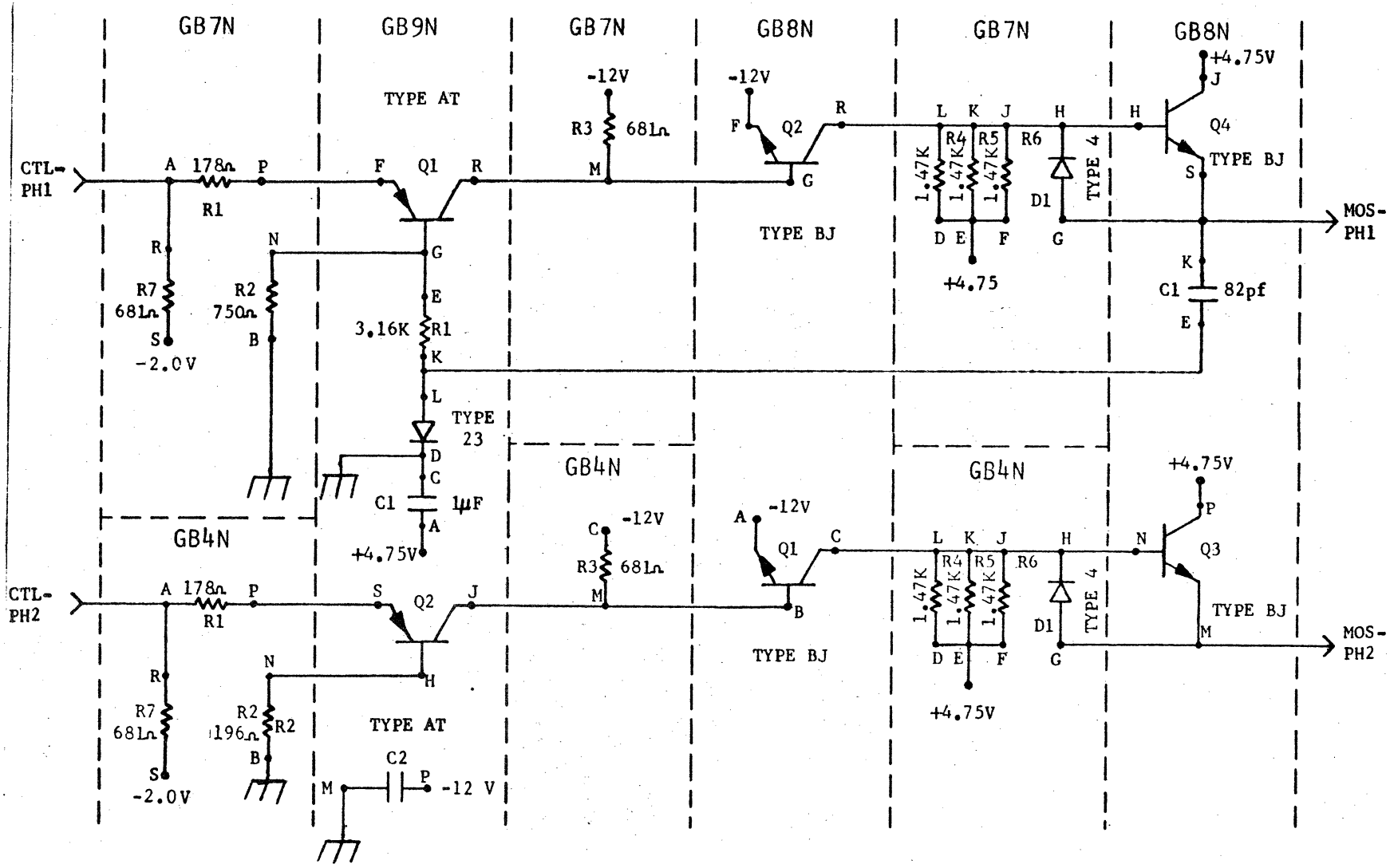


FIG. 5 DETAIL SCHEMATIC FOR MOS CLOCK DRIVER CIRCUITS PHASE 1 AND PHASE 2 USING GB4N, GB7N, GB8N, GB9N INTERFACE.

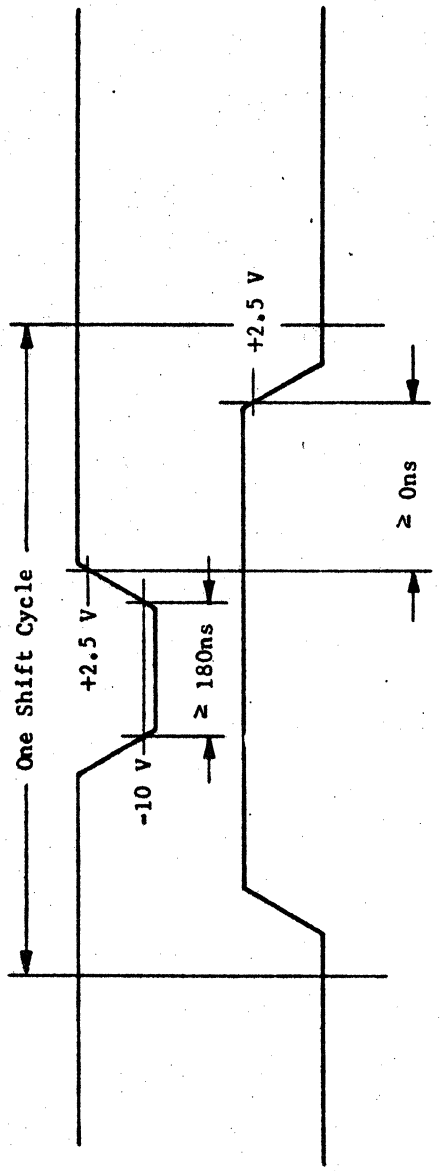


FIGURE 6
CLOCK PULSE TIMING

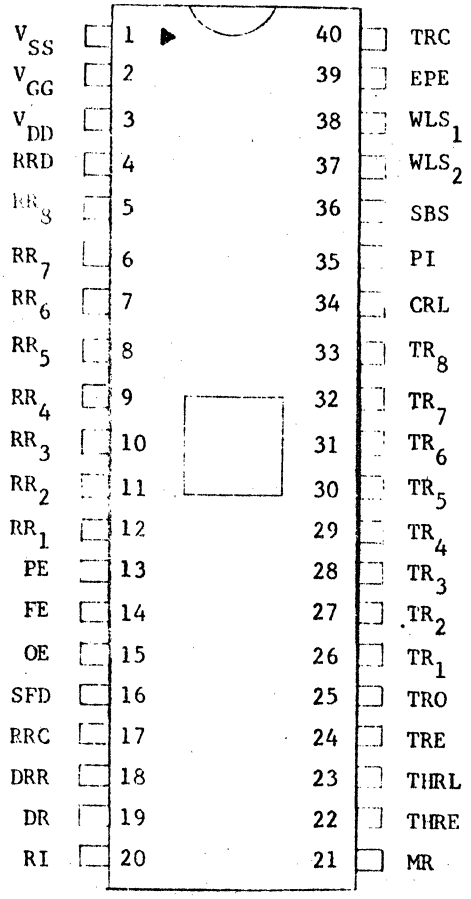
UART

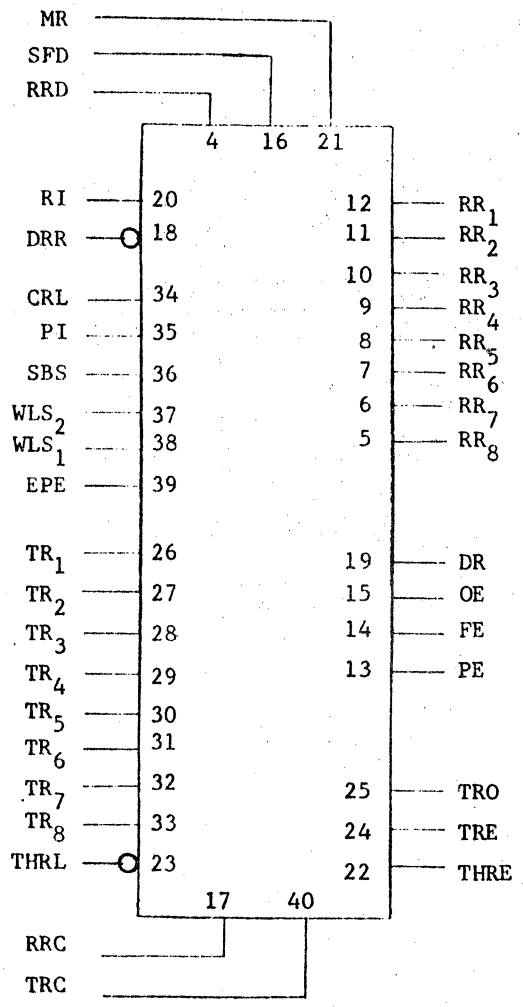
3.3 MOS Integrated Circuits (continued)

Element Type:	UART
Standard Assembly Number:	2315 2127
Manufacturer's Type:	W.D./TR1602A
Circuit Designation:	Asynchronous Receiver/Transmitter

Pin locations:

TOP VIEW





FUNCTIONAL DIAGRAM

MOS UART 2315 2127

Universal Asynchronous Receiver/Transmitter

(1) MOS/LSI silicon gate packaged in 40 pin DIP. It is a programmable device for interfacing an asynchronous serial data channel of a peripheral with parallel data.

(2) The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. These control bits are generated according to the programmed control inputs.

(3) The receiver section converts a serial word with start, data, parity, and stop bits into parallel data. It verifies proper code transmission by checking for valid start, parity, and stop bits.

(4) Both transmitter and receiver sections are double buffered, allowing parallel data to be loaded while serial data is being sent, and parallel data to be read out while serial data is being received.

(5) The transmitter and receiver controls are both programmed from the common control lines. A high on the Control Register Load (CRL) will strobe the bits inputed at PI (Parity Inhibit), SBS (Stop Bits Select), WLS_2 - WLS, (Word Length Select), and EPE (Even Parity Enable) into their corresponding control flip-flops. The CRL can also be hardwired high. The data code length can be either 5, 6, 7, or 8 bits. Parity may be even or odd, and its generation and checking may be inhibited. The number of stop bits may be one or two, except when transmitting a 5 bit code, one and one half are generated.

(6) Loading of parallel data (from TR_8-TR_1 inputs) into the Transmitter Holding Register should be done only when the Transmitter Holding Register Empty (THRE) is giving a high level output. Loading is effected by strobing the Transmitter Holding Register Load (THRL) to a LOW. Data is transferred to the Transmitter Register by sensing THRL returning to High and the Transmitter Register being empty (TRE goes high). The new character, once assembled and complete with start, parity, and stop bit(s) is outputed automatically through the TRO (Transmitter Register Output). Characters of less than 8 bits are right justified, with TR_1 as the least significant bit and the excess bits disregarded. When no data is being transmitted, the TRO output remains high. Transmission begins at the high-low transition of the Start bit.

(7) Serial data is received on the Receiver Input (RI). RI must be held high when data is not being received. A start detect circuitry locates the start bit (high-low) transition. It then checks the center of the start bit. If the input is still low, the signal is considered valid and subsequent data bits are loaded into the Receiver Register. The receiver data is checked for Parity Error (PE) and Framing Error (FE), and the corresponding error flags are updated (a high level indicates error) for each new character. For characters of less than 8 bits, the code is right justified with RR1 as the least significant bit and the truncated bits forced to a low level output voltage. The completed data is automatically transferred to the Receiver Holding Register (RHR) and the Data Received (DR) line is set to high, indicating that the received data (RR_8-RR_1) is available for sampling. After the data has been sampled, the Data Received Reset (DRR) should be strobed to low to reset the DR line. If DR is not reset before the next word is transferred to the RHR, Overrun Error (OE) occurs and the OE flag will be set (to high). The OE flag remains unchanged until another new character is transferred to the RHR. The RR_8-RR_1 data outputs are tri-state outputs and can be disconnected from those of the RHR by applying a high level voltage to Receiver Register Disconnect (RRD).

(8) All status flags (PE, FG, OE, THRE, and DR) are tri-state outputs and can be disabled by setting the Status Flags Disconnect (SFD) high.

(9) Strobing the Master Reset (MR) to high will clear the logic. It resets the Transmitter Register, the Receiver Holding Register, PE, FE, OE, DRR and sets TRO, THRE, and TRE.

(10) The Transmitter Register Clock (TRC) and the Receiver Register Clock (RRC) are the timing elements used to determine the length of bits transmitted and the center location of bits received. These clocks operate at 16 times the desired bit shift rate.

(11) Three power supplies are used:

V_{DD} = GND V_{ss}= 4.75V$\pm$0.25V V_{GG} = -12V $\pm$ 0.6V (5%)

(12) Electrical Characteristics:

Input Currents:

I_{IL} = -1.6mA @ V_{IL} = 0.4V I_{IH} = 40 μA @ V_{IH} = 2.4V

Output Drive:

I_{OL} = 1.6mA @ V_{OL} = 0.4V I_{OH} = -100 μA @ V_{OH} = 3.75V

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(12) Continued:

Input Voltages are:

V_{IH} minimum	Vss - 1.5V
V_{IL} maximum	0.8V @ Vss = 4.75V

Output Voltages are:

V_{OH} minimum	V_{ss}- 1.0V @ I_{OH} = -100 μA
V_{OL} maximum	0.4V @ I_{OL} = 1.6 mA

(13) Switching Characteristics:

Clock Frequency	DC to 320KHz max.
Clock Pulse Width (TRC,RRC) minimum	1 μs
CRL, THRL, DRR Pulse Width minimum	200 ns
MR pulse width minimum	500 ns
Coincidence Time, t_c minimum	200 ns
Hold Time, t_{hold} minimum	20 ns
Set Time, t_{set} minimum	0 ns
Propagation Delay	
SFD to Output, RRD to Output	
t_{dLH} maximum	800 ns
t_{dHL} maximum	500 ns
AC input load maximum at 1 MHz	20 pf
AC output load maximum at 1 MHz	20 pf

(14) Interface with CTL and Standard TTL devices:

UART is directly compatible with totem pole type standard TTL devices without the use of external resistors. For an open collector TTL output driving an UART input, an external pull-up resistor should be used.

None of the CTL devices can be used at the input of the UART, since the CTL outputs need to be pulled down, and the internal pull-up of the UART input prevents the same. For UART driving CTL inputs or a mixture of TTL and CTL inputs, the rules of Section 5.3.4 apply.

Unused UART inputs can be left open where a high is needed.

Interfacing UART with Schottky TTL or other special circuits should be consulted with the Circuits Section.

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PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} Power Supply	V_{SS}	+5 volts supply
2	V_{GG} Power Supply	V_{GG}	-12 volts supply
3	V_{DD} Power Supply	V_{DD}	Ground
4	Receiver Register Disconnect	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8-RR_1 data outputs.
5 - 12	Receiver Holding Register Data	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR_1 as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	Parity Error	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line. This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line.
14	Framing Error	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit; ie., the bit following the parity bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line.
15	Overrun Error	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data REceived Flag was not reset before the next character was transferred to the REceiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line.
16	Status Flags Disconnect	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	Receiver Register Clock	RRC	The receiver clock frequency is sixteen times the desired receiver bit shift rate.

PIN DEFINITIONS (CONT)

PIN NUMBER	NAME	SYMBOL	FUNCTION
18	Data Received Reset	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	Data Received	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	Receiver Input	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	Master Reset	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter Register, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	Transmitter Holding Register Empty	THRE	A high-level output Voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	Transmitter Holding Register Load	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	Transmitter Register Empty	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	Transmitter Register Output	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage, V_{OH}, to a low-level output voltage, V_{OL}.

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PIN DEFINITIONS (CONT)

PIN NUMBER	NAME	SYMBOL	FUNCTION
26 - 33	Transmitter Register Data Inputs	TR_1 - TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR_1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	Control Register Load	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	Parity Inhibit	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output to V_{OL}. If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.
36	Stop Bit(s) Select	SBS	This line selects the number of STOP bits to be transmitted after the PARITY bit. A high-level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. Selection of two STOP bits when programming a five bit word generates 1.5 STOP bits.
37 - 38	Word Length Select	WLS_2 - WLS_1	These two lines select the character length (exclusive of parity) as follows:

WLS_2	WLS_1	Word Length
V_{IL}	V_{IL}	5 bits
V_{IL}	V_{IH}	6 bits
V_{IH}	V_{IL}	7 bits
V_{IH}	V_{IH}	8 bits

39	Even Parity Enable	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	Transmitter Register Clock	TRC	The transmitter clock frequency is sixteen times the desired transmitter shift rate.

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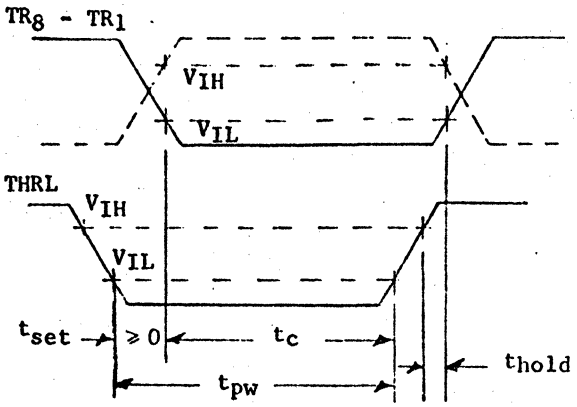
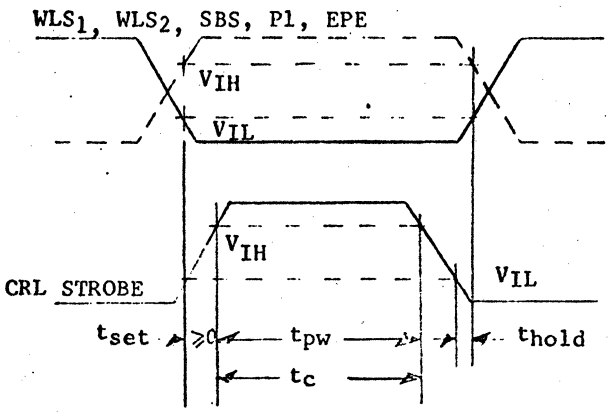
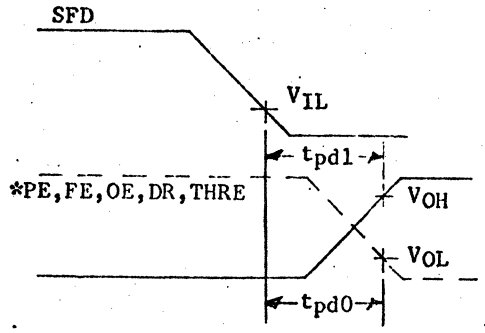


DATA INPUT LOAD CYCLE

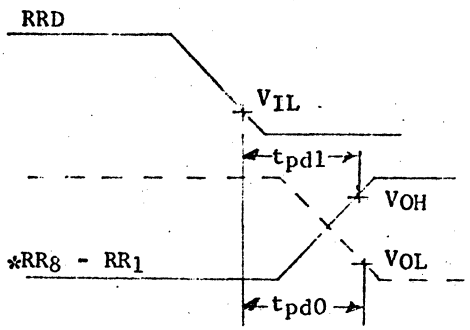


CONTROL REGISTER LOAD CYCLE



*OUTPUTS PE, FE, OR, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM V_{IL} TO V_{IH}

STATUS FLAG OUTPUT DELAYS



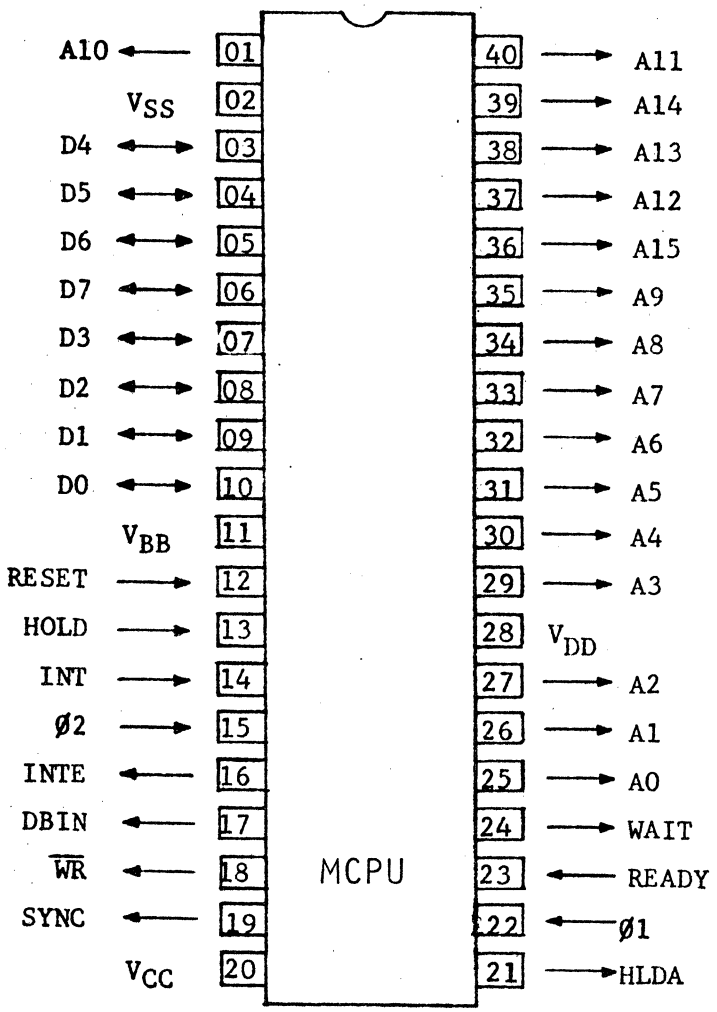
*RR_8 - RR_1 ARE DISCONNECTED AT TRANSITION OF RRD FROM V_{IL} TO V_{IH}

DATA OUTPUT DELAYS

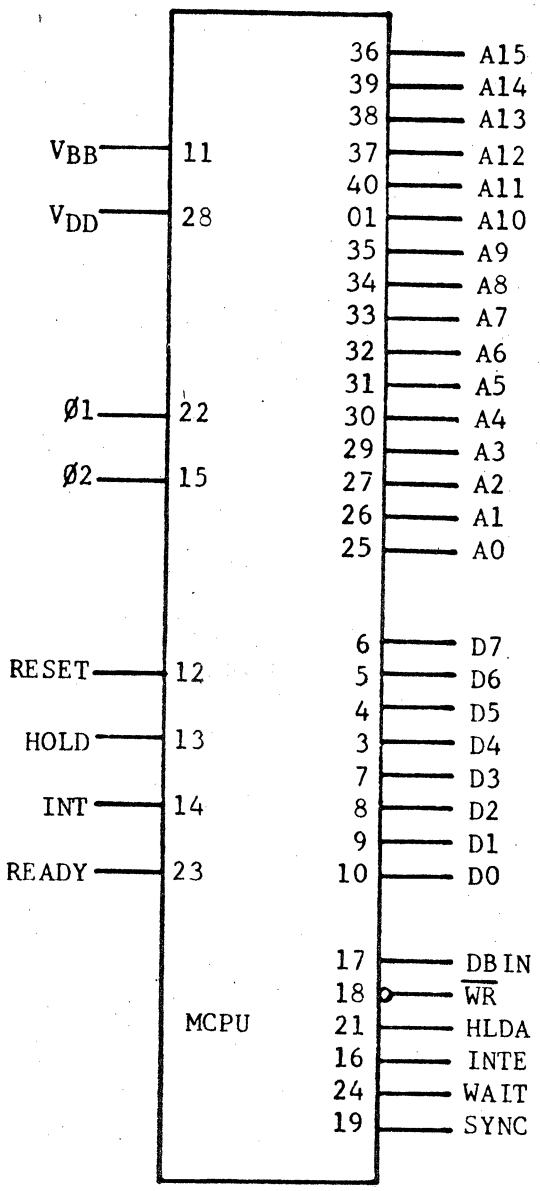
MCPU

3.3 MOS Integrated Circuits (continued)

Element Type: MCPU
Standard Assembly Number: 1959 5719
Manufacturer/Manufacturer's Type Intel/8080A
Circuit Designation: 8 bit Microprocessor
Description of Operation:



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

MOS MCPU 1959 5719

1) The MCPU is a general purpose, single-chip, 8 bit parallel microprocessor. It is an N-Channel Silicon Gate MOS/LSI circuit in a 40 pin DIP.

2) The processor has a 16 bit Address Bus (A15-A0) that may be used to directly address up to 64K bytes of memory. The memory may be any combination of ROM's and RAM's. Data is transferred into or out of the processor on a separate 8 bit bi-directional data bus. Six 8 bit general purpose registers are available to the programmer and can be used singly or in pairs for both 8 and 16 bit operations. An 8 bit accumulator is the primary working register for most of the arithmetic and logic operations.

3) The processor also has built-in control logic to handle general purpose stack operations, push-down stack for subroutine calls and returns, and vectored interrupt.

4) The following describes the function of all input/output pins of the MCPU:

A15-A0 A 16 bit Address Bus with tri-state outputs. It can address up to 64K bytes of memory or 256 input and 256 output devices. A0 is the LSB.

D7-D0 An 8 bit Bi-Directional Data Bus with tri-state outputs It provides two way data and instruction communication between the processor and all external units. Also, at the first clock of each machine cycle, the MCPU outputs a status word on this data bus. D0 is the LSB.

Ø1,Ø2 These two phase, high-level clock signals provide the basic timing for all internal operations in the processor.

SYNC The SYNChronize output signal indicates the start of each processor cycle and the presence of status information on the Data Bus.

DBIN A High on the Data Bus IN output indicates to external circuits that the bi-directional data bus is in the input mode and incoming data may be gated onto the bus lines.

READY The READY input synchronizes the processor with external units. If after sending an address out, the MCPU does not receive a READY input, the processor will enter a Wait state until READY goes back to High. Processing will then resume.

WAIT A High on the WAIT output indicates that the processor has entered the Wait state and is prepared to accept a READY from the current external operation.

WR A Low on the WRite output signals valid data on the Data Bus, to be written into memory or I/O components.

HOLD The HOLD input allows an external device to cause the processor to enter the Hold state and relinquish control over the Address and the Data Buses. Both buses will enter their high impedance OFF state.

HLDA The MCPU acknowledges that it is in the Hold state by giving a High on the Hold Acknowledge output. HLDA signal appears after the rising edge of clock Ø1 while the Address and Data Buses will enter their OFF state after the rising edge of clock Ø2.

INTE The INTerrupt Enable output signal shows the status of the interrupt enable flip-flop, indicatng whether or not the processor will accept interrupts.

RESET A High on the RESET input will initialize the processor by clearing the program counter, the instruction register, the interrupt enable flip-flop, and the hold acknowledge flip-flop. It should be active for at least 3 clock periods. The general registers are not cleared.

5) Table 1 is a summary of the processor instruction set. For details concerning programming, refer to the Intel 8080 User's Maunal.

6) Electrical Characteristics

Input Threshold Voltages

Vil maximum		0.8V
Vih minimum,	clock inputs Ø1,Ø2	9.0V
	all other inputs	3.3V

Output Voltages

Vol maximum	0.45V @ Iol = 1.9 mA
Voh minimum	3.7V @ Ioh = -150 uA

MOS MCPU 1959 5719

Input Loading	
Iil Data Bus D7-D0, Input mode	-2 mA @ 0 <=Vil <=0.8V
Iih " " "	10 uA @ 0.8V<=Vih<=Vcc
Input Leakage Currents	
Clock inputs Ø1, Ø2	+10 uA max
	-10 uA min @ 0<=Vi<=Vdd
all other inputs	+10 uA max
	-10 uA min @ 0<=Vi<=Vcc
Address and Data bus outputs in the OFF state	+10 uA max @ Vi=0.45V
	-100 uA min @ Vi=Vcc
Output Drive	
Iol	1.9 mA @ Vol <=0.45V
Ioh	-150 uA @ Voh >=3.7V
Supply Current	
Idd maximum	70 mA @ Vdd = 12V
Icc maximum	80 mA @ Vcc = 5V
Ibb maximum	1 mA @ Vbb = -5V
Supply Voltages	
Vdd	12V ± 5%
Vcc	5V ± 5%
Vbb	-5V ± 5%
Vss	Ground

7) Switching Characteristics

Clock Period	tcy	0.48 usec to 2.0 usec.
Clock Rise and Fall Time, max.	tr,tf	50 ns
Clock Ø1 Pulse Width, min.	tØ1	60 ns
Clock Ø2 Pulse Width, min.	tØ2	220 ns
Set-up Time, minimum		
Data to Ø1 during DBIN	tds1	30 ns
Data to Ø2 during DBIN	tds2	150 ns
READY to Ø2	trs	120 ns
INT to Ø2	tis	120 ns
HOLD to Ø2	ths	140 ns
Hold Time, minimum		
Ø2 to control signals INT, HOLD, READY	th	5 ns
Ø2 to Data during DBIN	tdh	50 ns
DBIN to Address during HLDA	tah	-20 ns

MOS MCPU 1959 5719

Propagation Delay Time, maximum		
Ø2 to Address Outputs, max.	tda	200 ns
Ø2 to Data outputs	tdd	220 ns
Clock Ø1 or Ø2 to control outputs SYNC, $\overline{WR}$, WAIT, HLDA	tdc	120 ns
Ø2 to Data bus enter Input mode	tdi	140 ns
Ø2 to INTE	tie	200 ns
Ø2 to DBIN	tdf	140 ns
Ø2 to Address or Data bus enter OFF state during HOLD	tfd	120 ns
Ø1 (Low) to SYNC, DBIN	tdØ1	160 ns
$\overline{HLDA}$ to Float	thf	= td3+trØ2-50 ns
$\overline{WR}$ to Float	twf	= td3+trØ2-10 ns
Minimum Time Requirement for		
Ø1- to Ø2-	td1	5 ns
Ø2- to Ø1+	td2	70 ns
Ø1+ to Ø2+	td3	80 ns
Address stable prior to $\overline{WR}$	taw	= 2tcy-td3-trØ2-140 ns
Output Data stable prior to $\overline{WR}$	tdw	= tcy-td3-trØ2-170 ns
Output Data stable from $\overline{WR}$	twd	= twf if HLDA
		= td3+trØ2+10 ns if not
Address stable from $\overline{WR}$	twa	= twd

8) Interface Rules

Inputs are not directly TTL compatible. For the clock inputs Ø1 and Ø2, the minimum Vih is 9V. Use of the 8224 clock circuit would provide this drive without external interface circuitry. Otherwise an open collector TTL device (such as IHDN) with a 1KΩ pull-up to +12V can be used. For all other inputs, the required minimum Vih is 3.3V. The 8228 System Controller (SCTL) has the necessary drive capability on its data bus outputs to the MCPU. For other situations where TTL must drive an MCPU input a resistor of value <=1KΩ must be used as a pull-up to Vcc on that pin. Refer to Section 5 for fan-in/fan-out considerations involving pull-up resistors.

The outputs of the MCPU are directly TTL compatible but with an output drive of only one TTL unit load per output.

Interfacing the MCPU with any other logic family must be handled through the Circuits Section.

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
$MOV_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11

TABLE 1 - SUMMARY OF PROCESSOR FUNCTIONS

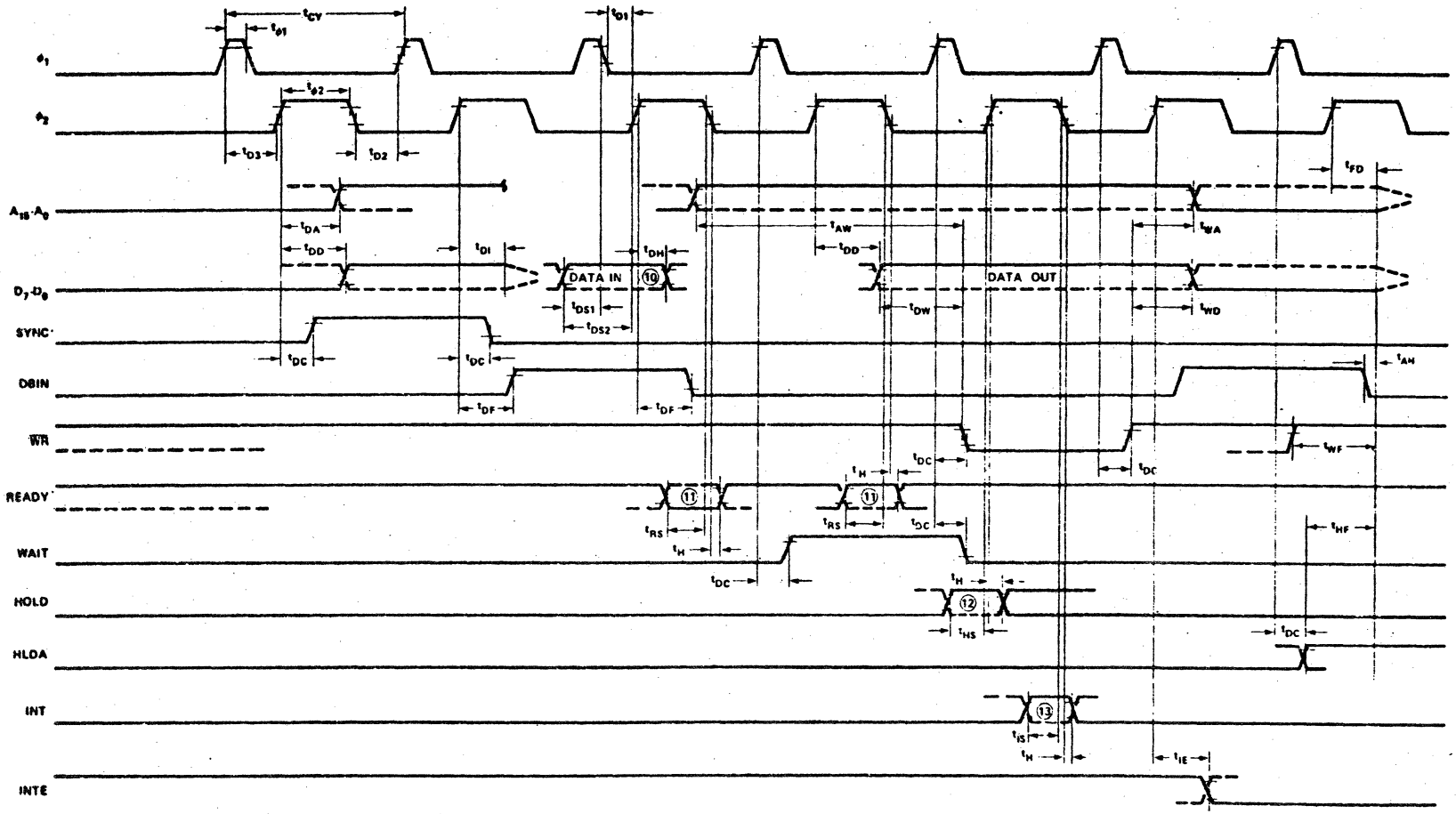
MCPU

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

TIMING WAVEFORMS

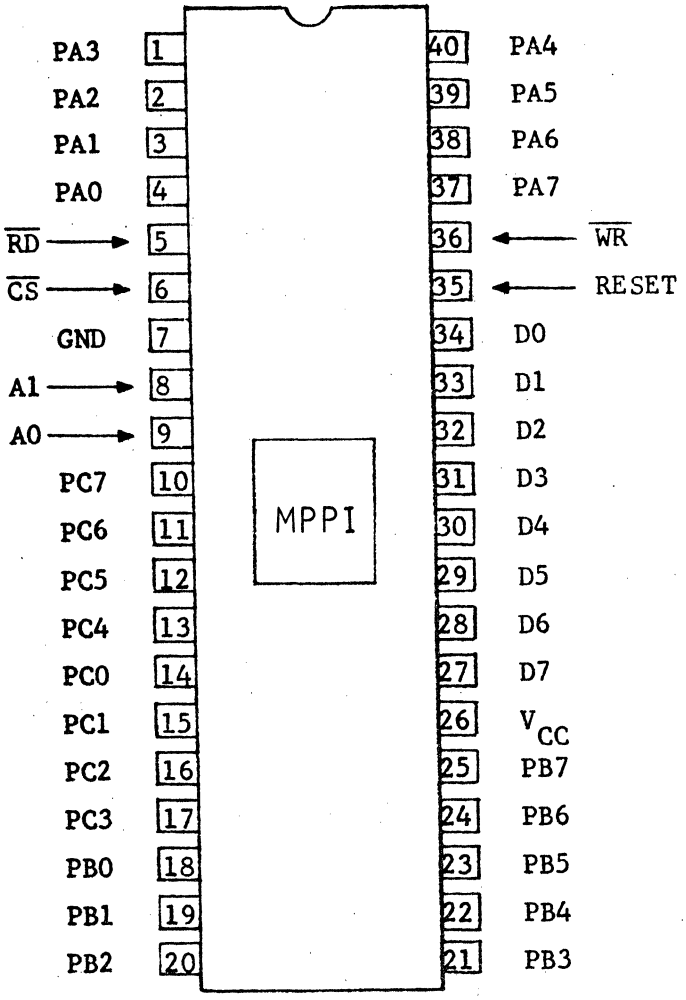
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



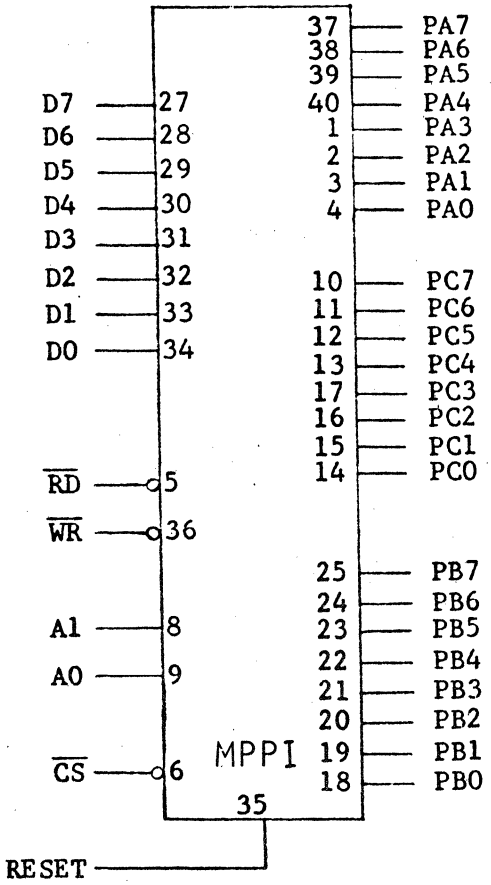
3.3 MOS Integrated Circuits (continued)

Element Type: MPPI
Standard Assembly Number: 2219 4534
Maunfacturer/Manufacturer's Type: Intel/8255
Circuit Designation: Programmable Peripheral Interface

Description of Operation:



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

MOS MPPI 2219 4534

1) The MPPI is a general purpose programmable I/O device designed for use with the MCPU microprocessor. It is a Silicon-Gate N-Channel MOS integrated circuit in a 40 pin ceramic DIP. Its inut/output pins are:

D7-D0	Bi-Directional Data Bus (System side)
PA7-PA0	Port A I/O Pins
PB7-PB0	Port B I/O Pins
PC7-PC0	Port C I/O Pins
$\overline{CS}$	Chip Select input
$\overline{RD}$	Read control input
$\overline{WR}$	Write control input
A1-A0	Port Address Select inputs

2) The MPPI Programmable Peripheral Interface functions as a system software controlled I/O component between the MCPU data bus and the peripheral equipment. A Read/Write Control Logic Block manages all of the internal and external transfer of both data and control or status words. It accepts address signals and I/O commands from the MCPU, and in turn, issues commands to both the Group A and Group B Control Blocks.

3) The Chip Select ($\overline{CS}$) control line enables the communication between the MPPI and the central system. The Read ($\overline{RD}$) line enables the MPPI to send data or status information to the MCPU on the Bi-Directional Data Bus D7-D0. The Write ($\overline{WR}$) line enables the MCPU to write data or control words into the MPPI. All 3 control signals are active Low. The A1 and A0 lines select one of the three I/O ports or the Control Word Register. The combination of these control inputs define the functioning of the MPPI, as listed in Table 1.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A ==> DATA BUS
0	1	0	1	0	PORT B ==> DATA BUS
1	0	0	1	0	PORT C ==> DATA BUS
					OUTPUT OPERATION(WRITE)
0	0	1	0	0	DATA BUS ==> PORT A
0	1	1	0	0	DATA BUS ==> PORT B
1	0	1	0	0	DATA BUS ==> PORT C
1	1	1	0	0	DATA BUS ==> CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS ==> 3-STATE
1	1	0	1	0	ILLEGAL CONDITION

TABLE 1 8225 BASIC OPERATION

4) A High on the RESET input clears all internal registers including the Control Registers and the mask flip-flops (INTE's) All ports (A, B, and C) are set to the input mode.

5) The 24 I/O pins are divided into 2 Groups, A and B, each with its own control block. Control Block A governs Port A (PA7-PA0) and Port C Upper (PC7-PC4) while Control Block B governs Port C Lower (PC3-PC0) and Port B (PB7-PB0). By programming Control Words into the Control Blocks, the PPI can be used in 3 modes of I/O operations in addition to the bit set/reset operation. The format of the corresponding control words are shown in Figures 1 and 2.

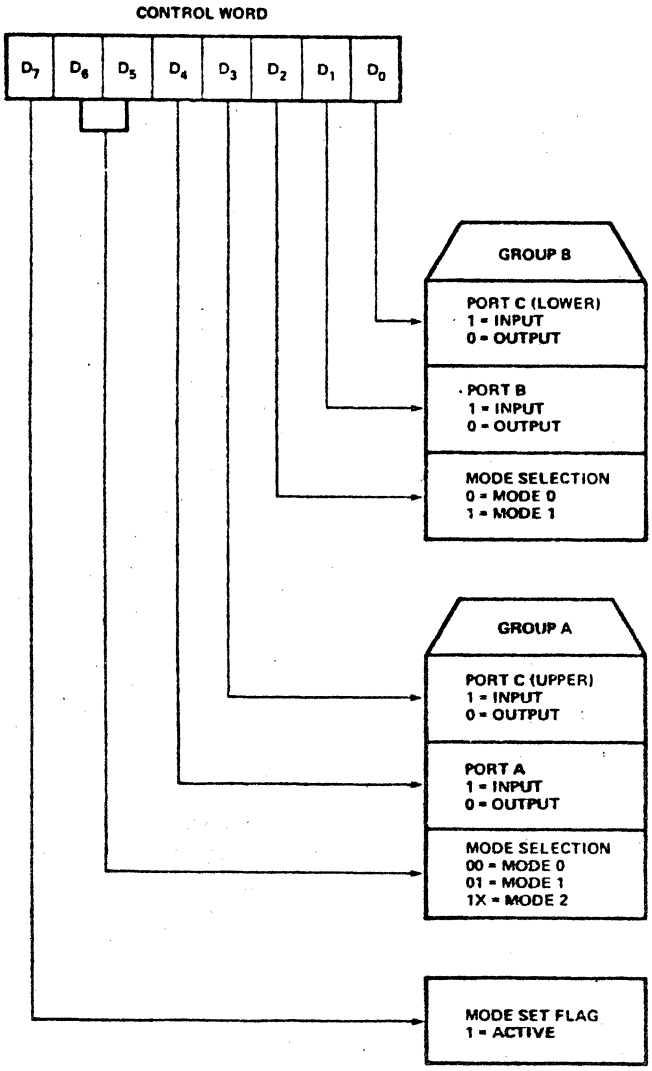


Figure 1: Mode Definition Format

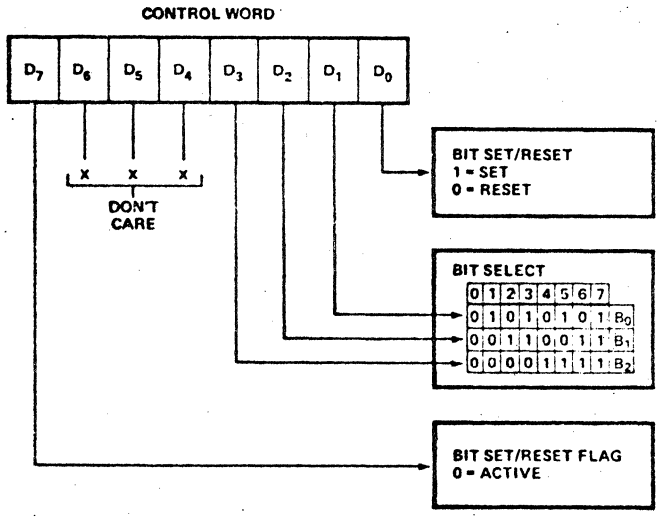


Figure 2: BIT Set/Reset Format

MOS MPPI 2219 4534

5.1 Bit Set/Reset Operation
Any of the 8 bits of Port C can be set or reset by a single write instruction.

5.2 Mode 0 Operation (Basic Input/Output)
The 24 I/O pins are organized into two 8 bit ports and two 4 bit ports, any of which can be chose as inputs or outputs. Outputs are latched, inputs are not. 16 different combinations are possible in this mode. No handshaking is provided or required.

5.3 Mode 1 Operation (Strobed Input/Output)

The I/O pins are organized into two groups, each consisting of an 8 bit data port and a 4 bit control/data port. The 8 bit ports can be either inputs or outputs, both latched. The 4 bit ports are for handshaking. The input handshaking signals include:

$\overline{STB}$ (Strobe) -- An active Low signal to load data into the input latch.
IBF (Input Buffer Full) -- A High on this acknowledges the receiving of data into the input latch. It is set by the falling edge of the $\overline{STB}$ input and is reset by the rising edge of the $\overline{RD}$ input.
INTR (Interrupt Request) -- A High on this input allows an input device to interrupt and request service from the CPU. It is set by the rising edge of $\overline{STB}$ if both IBF and INTE are High. It is reset by the falling edge of $\overline{RD}$.

The output handshaking signals include:

$\overline{OBF}$ (Output Buffer Full) -- An active Low output signal to indicate that the CPU has written data onto the specified port. It is set by the rising edge of $\overline{WR}$ and reset by the falling edge of $\overline{ACK}$.
$\overline{ACK}$ (Acknowledge) -- An Low on this input informs the CPU that data has been received by the output equipment.
INTR -- A High on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of $\overline{ACK}$ when both $\overline{OBF}$ and INTE are High. It is reset by the falling edge of WR.

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5.4 Mode 2 Operation (Strobed Bi-Directional Bus I/O)

Port A is used as an 8 bit bi-directional bus port, with 5 bits from port C serving as handshaking signals lines. Both inputs and outputs are latched. The handshaking signals include:

INTR -- A High on this output allows interruption of the CPU for both input and output operations.
$\overline{OBF}$ --- The $\overline{OBF}$ output will go Low to indicate that the CPU has written data onto Port A.
$\overline{ACK}$ --- A Low on this input enables the tri-state output buffers of Port A to send out data. A High on $\overline{ACK}$ will switch the port A outputs to their high impedance OFF state.
$\overline{STB}$ --- An active Low input to load data into the input latch.
IBF --- A High on this output will indicate that data has been loaded into the input latch.

6) Electrical Characteristics

Input Threshold Voltages	
Vil maximum	0.8V
Vih minimum	2.0V
Output Voltages	
Vol maximum	0.4V @ Iol = 1.6 mA
Voh minimum	2.4V @ Ioh = -100 uA
Input Loadings	
Iil	15 uA @ Vil = 0.4V
Iih	70 uA @ Vih = 2.4V
Output Drive	
Iol	1.6 mA @ Vol <=0.4V
Ioh	-100 uA @ Voh >=2.4V
Darlington Drive Current (available on any 8 pins from Ports B or C)	
Ioh	2 mA @ Voh = 1.5V
Supply Current Icc	50 mA @ Vcc = 4.75V
Supply Voltage Vcc	5V ± 5%

MOS MPPI 2219 4534

7) Switching Charactteristics

Pulse Width,		
$\overline{WR}$ min.	twp	430 ns
$\overline{ACK}$ min.	tak	500 ns
$\overline{STB}$ min.	tst	350 ns
$\overline{RD}$ min.	trp	430 ns
Set-up Time, minimum		
Data Bus D7-D0 to $\overline{WR}$	tdw	30 ns
Address A1-A0 to $\overline{WR}$	taw	150 ns
Chip Select $\overline{CS}$ to $\overline{WR}$	tcw	150 ns
D7-D0 to Read $\overline{RD}$	tir	200 ns
A1-A0 to $\overline{RD}$	tar	200 ns
$\overline{CS}$ to $\overline{RD}$	tcr	200 ns
Peripheral to Strobe $\overline{STB}$	tps	200 ns
Hold Time, minimum		
D7-D0 to $\overline{WR}$	twd	400 ns
A1-A0 to $\overline{WR}$	twa	200 ns
$\overline{CS}$ to $\overline{WR}$	twc	160 ns
D7-D0 to $\overline{RD}$	thr	100 ns
A1-A0 to $\overline{RD}$	tra	200 ns
$\overline{CS}$ to $\overline{RD}$	trc	150 ns
Peripheral to $\overline{STB}$	tph	150 ns
Propagation Delay, maximum		
$\overline{WR}$ to Outputs	twb	500 ns
$\overline{RD}$=0 to System Bus D7-D0	trd	500 ns
$\overline{RD}$=1 to D7-D0	tod	500 ns
$\overline{ACK}$=0 to Outputs	tad	500 ns
ACK=1 to Outputs	tkd	300 ns
$\overline{WR}$=1 to $\overline{OBF}$=0	two	300 ns
$\overline{ACK}$=0 to $\overline{OBF}$=1	tao	500 ns
$\overline{STB}$=0 to IBF=1	tsi	600 ns
$\overline{RD}$=1 to IBF=0	tri	300 ns

8) Interface Rules

All input/output voltages are fully TTL compatible. Input loadings differ slightly from nominal TTL values. Output drive capability is significantly less, roughly 1 TTL unit load per output.

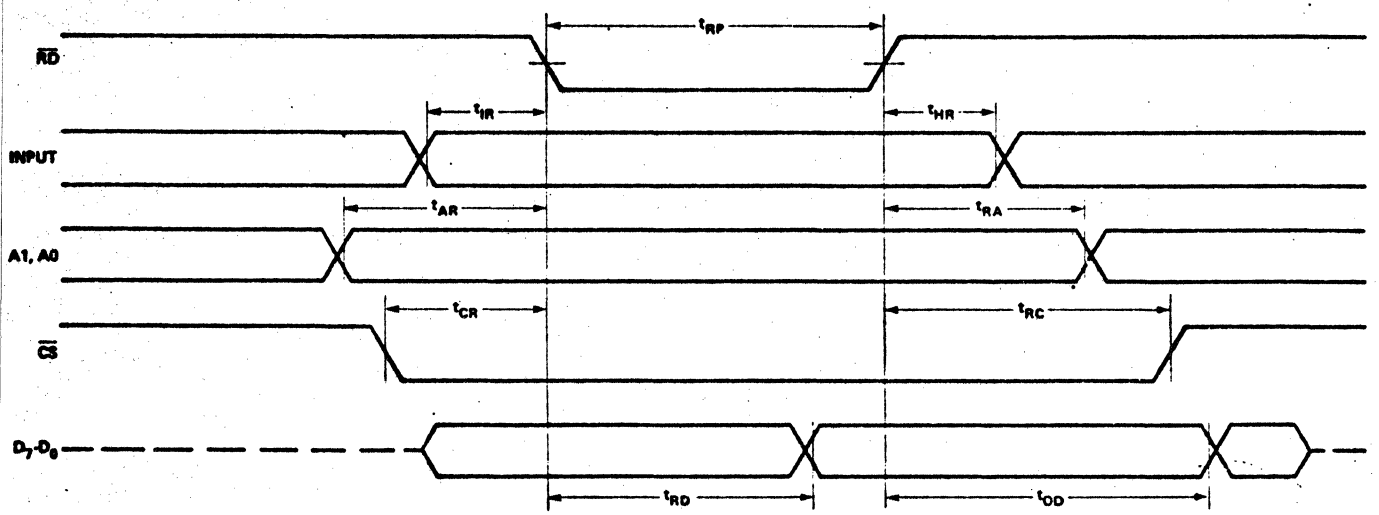
MOS MPPI 2219 4534

The I/O Port Outputs are capable of sourcing enough High level current (2 mA @ 1.5V typically) to directly drive Darlington type drivers and high-voltage displays that requires such source current. A maximum of 8 output buffers can be choosed randomly from among Port A, B and C outputs at a time.

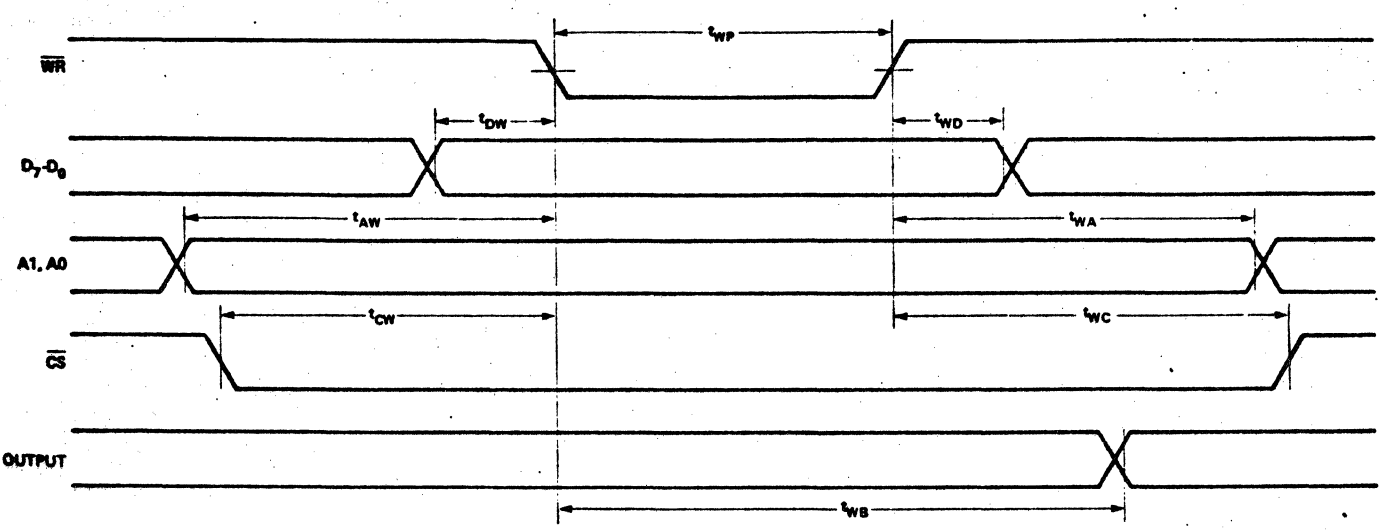
Interfacing to all MPPI input/output pins follow rules as defined for standard TTL circuits, except for the different input and output loadings. Refer to Section 5 for details.

Unused inputs will appear as Low, but are extremely susceptible to noise and have long decay time (in the order of seconds) when switching from High to Open. An unused input must, therefore, be terminated to ground through a 1KΩ resistor where a Low is desired, and to Vcc through a 1KΩ resistor where a High is needed.

MPPI

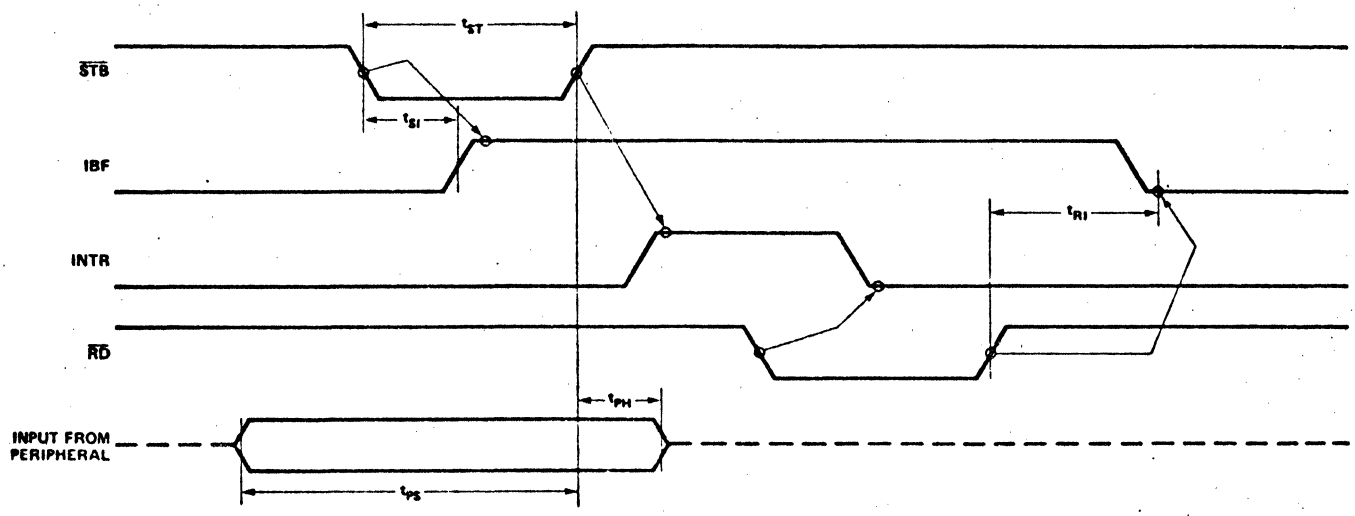


Mode 0 (Basic Input)

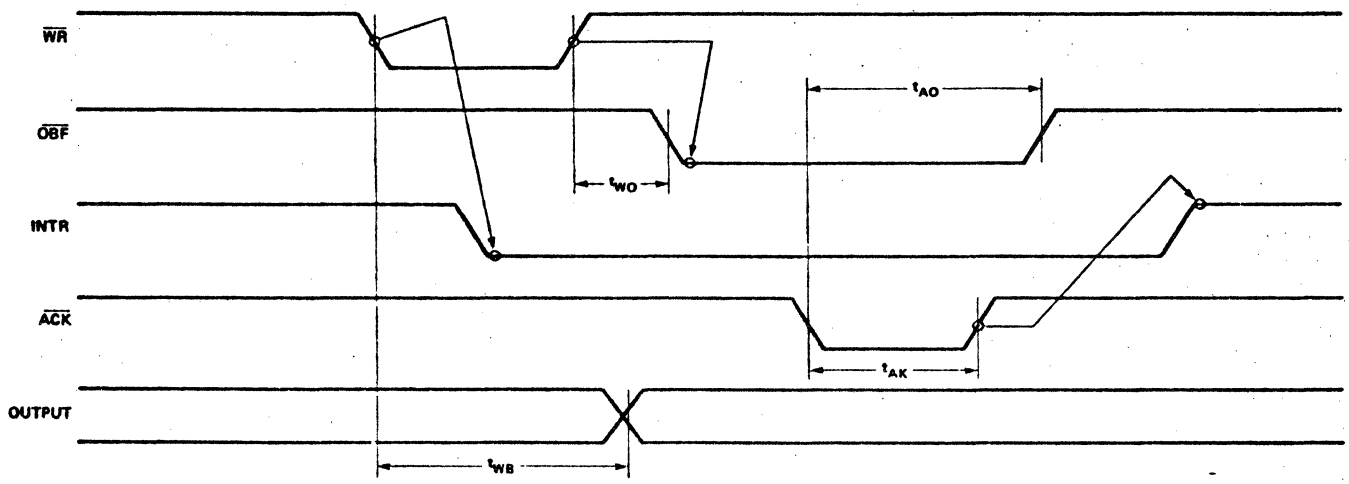


Mode 0 (Basic Output)

MPPI

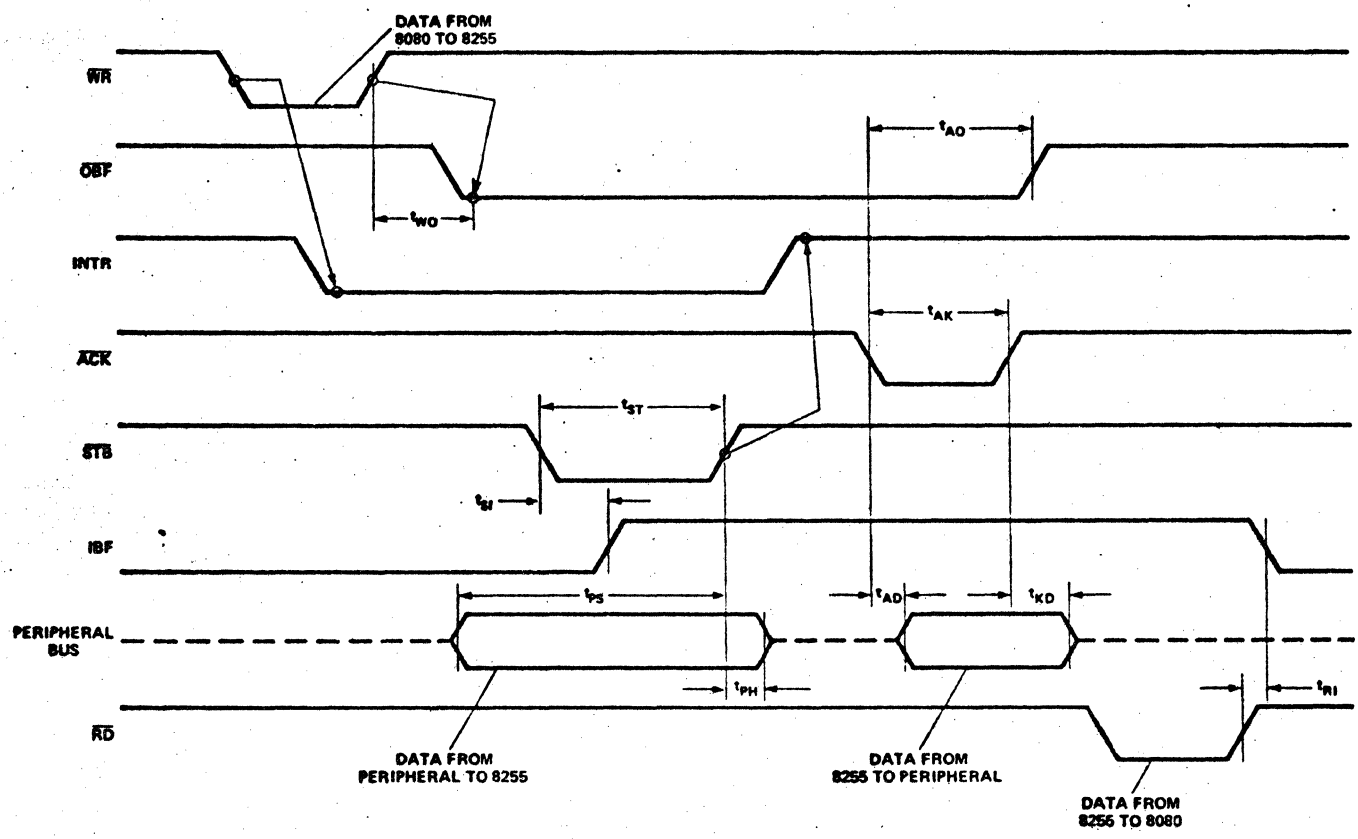


Mode 1 (Strobed Input)



Mode 1 (Strobed Output)

MPPI



Mode 2 (Bi-directional)

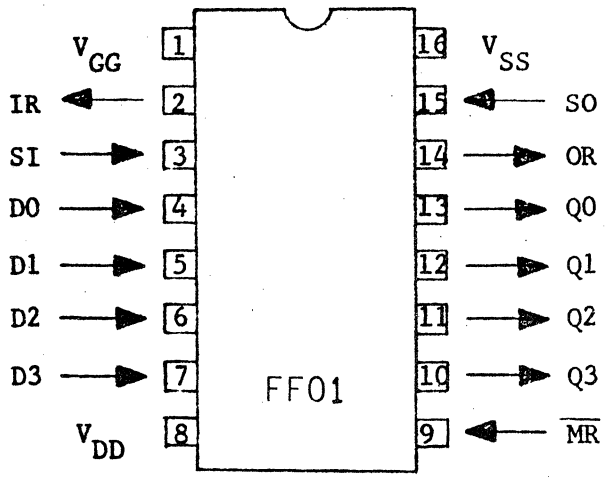
FF01

3.3 MOS Integrated Circuits (continued)

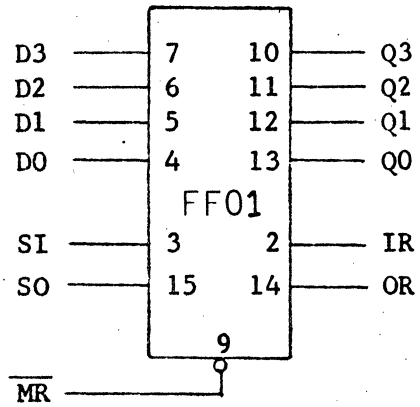
Element Type:	FF01
Standard Assembly Number:	1448 9165
Manufacturer/Manufacturer's Type:	FSC/3341
Circuit Designation:	64x4 FIFO Memory
Description of Operation:	

1) The FF01 is a 64 word x 4 bit First-In-First-Out Serial Memory, with completely independent input and output clocks designed for both synchronous and asynchronous buffer applications. The device is a Silicon-Gate P-Channel MOS circuit in a 16 pin DIP. The input/output pins are:

D3-D0	Memory data inputs
Q3-Q0	Memory data outputs
SI	Shift In signal input
SO	Shift Out signal input
IR	Input Ready output
OR	Output Ready output
$\overline{MR}$	Master Reset input



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

MOS FF01 1448 9165

2) Data input is effected when both Input Ready (IR) and Shift In (SI) are High. The 4 bit word presented at the D3-D0 data input lines will be read into the FF01 Input Stage which is actually the first of the 64 4-bit internal registers. IR will go Low to temperorily prevent external changes on the data lines to affect the information already read in. When SI is returned to Low, the data in this first register propagates to the second provided that register is empty. Once data is transferred out of the first register, IR will go High indicating the chip is ready to accept new data. If the memory is full, data in the Input Stage will not be transferred, and hence IR will remain Low. The sequence in which IR and SI go High or Low do not matter as long as the minimum High and Low Overlap Time requirements are satisfied.

3) Once data is enterec into the second register, an internal clock will automatically cause it to rippie through the internal registers toward the Output Stage provided there are empty registers ahead. Thus all input data will eventually line up at the output end in a First-In-First-Out order. tpt defines the time required for a data to bubble from the Input Stage all the way to the Output Stage in a previously empty device.

4) Valid data at the output lines Q3-Q0 is indicated by a High on the Output Ready (OR) line. Transfer of subsequent data to the Output Stage is effected when both the OR line from the device and the Shift Out (SO) line to the device are High. This causes OR to go Low, but the output data is maintained until both OR and SO are Low. Then the contents of the adjacent (4 bit) register, provided it is full, will be transferred to the Output Stage. OR will go High indicating that new data is available for external sampling. If the memory has been emptied, OR will remain Low. Note that, in such a case, the last data will remain at the Output Stage until it is being forced out by new incoming data, even though it is presently invalid as indicated by OR sitting at Low. Once again, the timing of the SO and OR signals will not matter as long as the minimum High and Low Overlap Times are guaranteed.

5) A Low on the Master Reset ($\overline{MR}$) will asynchronously reset all control registers and put IR to High and OR to Low. It does not reset the data registers and hence the last output will remain at the Q3-Q0 lines. But once again, this is indicated as invalid data by OR sitting at Low.

MOS FF01 1448 9165

If $\overline{MR}$ returns to High at the point where SI is held High, then data on D3-D0 will be instantly written into the first location of the memory and IR will go Low. If $\overline{MR}$ returns to High at the point where SO is held High, the first data that comes in through the Input Stage will fall through to the Output Stage, OR will go High for one internal clock cycle and then back to Low. But output data will remain locked in while subsequent data line up behind the Output Stage. It will be forced out of memory only when SO is brought back to Low.

6) When the output data changes as a result of a pulse on SO, OR always goes Low before there is any change in the output data; and always stays Low until after the new data has appeared on the outputs. So anytime OR is High, there is good, stable data on the outputs. IR and OR may also be used as status signals indicating that the FF01 is completely full (IR stays Low for at least tpt) or completely empty (OR stays Low for at least tpt).

7) Electrical Characteristics

Input Threshold Voltages	
Vil maximum	0.8V
Vih minimum	Vss - 1V
Input Pull-up Initiation Voltage, all inputs except MR	
Vpup maximum	2.4V @ Vss = 4.75V
Output Voltages	
Vol maximum	0.4V @ Iol = 1.6 mA
Voh minimum	Vss - 1.0V @ Ioh = 0.3 mA
Input Loading	
Iil	-1.0 uA @ Vol = 0.4V
Iih	-500 uA @ Voh = 2.4V
Output Drive	
Iol	1.6 mA @ Vol < 0.4V
Ioh	-0.3 mA @ Voh > Vss-1.0V
Supply Voltages	
Vss	5V ± 10%
Vgg	-12V ± 10%
Vdd	Ground

MOS FF01 1448 9165

8) Switching Characteristics

Input Ready High Time, max.	tir+	550 ns
Input Ready Low Time, max.	tir-	550 ns
Control Overlap High Time, min.	tov+	100 ns
Control Overlap Low Time, min.	tov-	100 ns
Data Input Stable Time, min.	tdsi	650 ns
Data Input Delay Time, max.	tdd	25 ns
Output Ready High Time, max.	tor+	500 ns
Output Ready Low Time, max.	tor-	850 ns
Data Through-put Time, max.	tpt	32 us
Data Hold Time, min.	tdh	75 ns
Master Reset Pulse Width, min.	tmrw	400 ns
Data Output Available Time, min.	tda	5 ns

9) Interface Rules

A special pull-up circuit is provided on all inputs except MR. The internal pull-up resistor is effectively connected only when the voltage present at the input goes above the Input Pull-up Initiation Voltage Vpup. This guarantees the minimum Vih of Vss-1V with a nominal TTL High at the input. When going Low, the external driver must overcome a current barrier Ibar. Once this is achieved, the iuput current drops to about zero and the internal pull-up resistor is disconnected so it provides no steady-state loading problem to the driver.

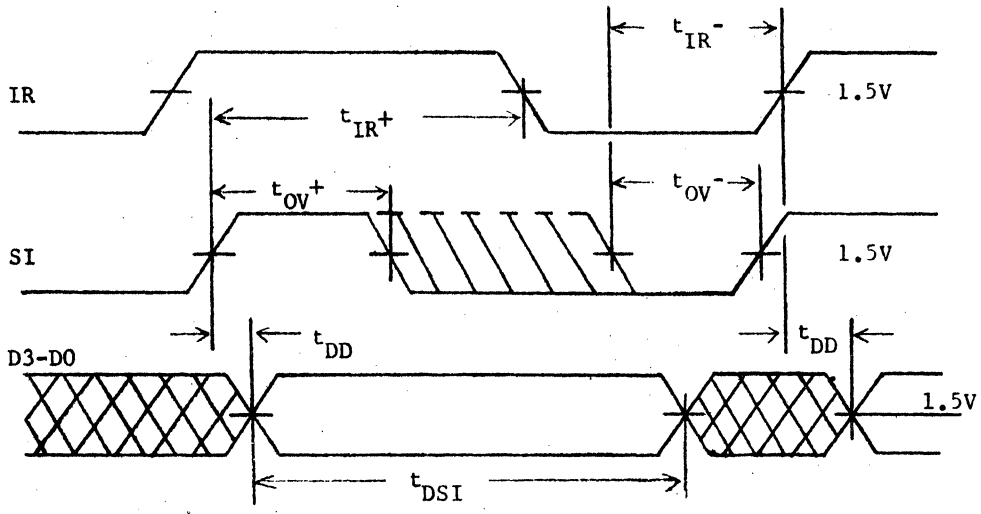
Interfacing to all inputs but $\overline{MR}$ follows the rules defined for interfacing TTL inputs as described under Section 5. Note that in order to guarantee operation up to Vss = 5.25V, the High level voltage provided by the driver must be > 3.0V (Vbar). As for $\overline{MR}$, the driver must always provide a Vih of > Vss-1V.

Interfacing to all outputs follow the rules defined for standard TTL outputs, bearing in mind that the output drive capability of the FF01 outputs are less than the nominal TTL values.

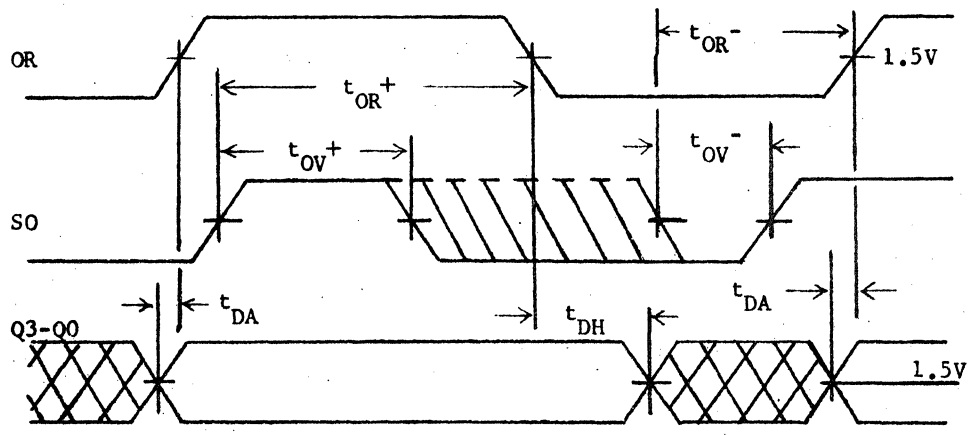
Unused inputs are stable in the High state. At Low, each input must be terminated by a 1 KΩ resistor to ground.

FF01

1448 9165



INPUT TIMING



OUTPUT TIMING

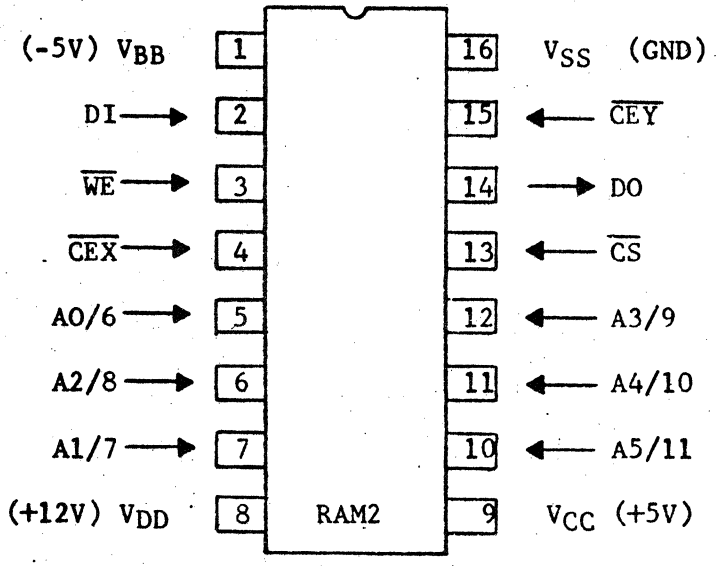
C_L = 100 pF

RAM2

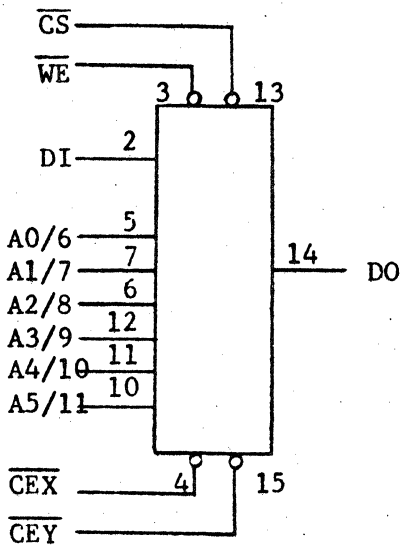
3.3 MOS Integrated Circuits (Continued)

Element Type: RAM2
Standard Assembly Number: 2623 5945
Manufacturer/Manufacturer's Type: Mostek/MK4096P
Circuit Designation: 4K Bit Dynamic Memory

Description of Operation:



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

MOS RAM2 2623 5945

1) The RAM2 is a 4096x1 bit N channel MOS dynamic random access memory packaged in a 16 pin DIP.

2) The information is retained as a charge on the capacitance of an internal node. Because of leakage, each cell must therefore be refreshed periodically.

3) Four modes of operation are defined for the memory array: read only, write only, read-modify-write, and refresh only.

4) The 12 address bits required to decode 1 of the 4096 cell locations are multiplexed onto the 6 addrress pins. The Row Address Strobe $\overline{CEX}$ latches the 6 row address bits (A0-A5) into the on chip row address latch. The Column Address Strobe $\overline{CEY}$ latches the 6 column address bits (A6-A11) into the column address latch plus the Chip Select ($\overline{CS}$) into the chip.

5) Data input is strobed into an on chip register by a combination of $\overline{WE}$ and $\overline{CEY}$. The last of these signals making its negative transition is the strobe for the data in register.

6) At the beginning of each memory cycle, the state of the data out latch depands on the previous memory cycle. At access time the tri-state output will assume the proper state for the type of cycle performed. There is no data inversion. When unselected ($\overline{CS}$ high), the tri-state output latch will remain in its open-circuit condition regardless of $\overline{WE}$.

7) The RAM2 requires periodic refreshing of the memory cells. This is accomplished by performing a memory cycle at each of the 64 row addresses every 2.1 ms or less. Any one of the read, write, or read-modify-write cycles will refresh the selected row, regardless of the state of $\overline{CS}$. But with the exception of read only cycles, the chip should be unselected during refresh to prevent writing data into the memory.

8) Electrical Characteristics

Input Voltages
Vil max. = 0.8V Vih min. for $\overline{CEX}$, $\overline{CEY}$, $\overline{WE}$ = 3.0V
for all other inputs =2.4V

Output Voltages
Vol max. = 0.4V Voh min. = 2.4V

Input Loading
Iil, Iih max. = 10 uA

MOS RAM2 2623 5945

Output Drive
Iol = 2 mA @ Vol = 0.4V Ioh = -5 mA @ Voh = 2.4V
Io leakage (chip disabled) = 10 uA

Supply Voltages

Vdd	+12V ± 10%
Vbb	-5V ± 10%
Vss	Ground
Vcc	+5V ± 10%

9) Switching Characteristics

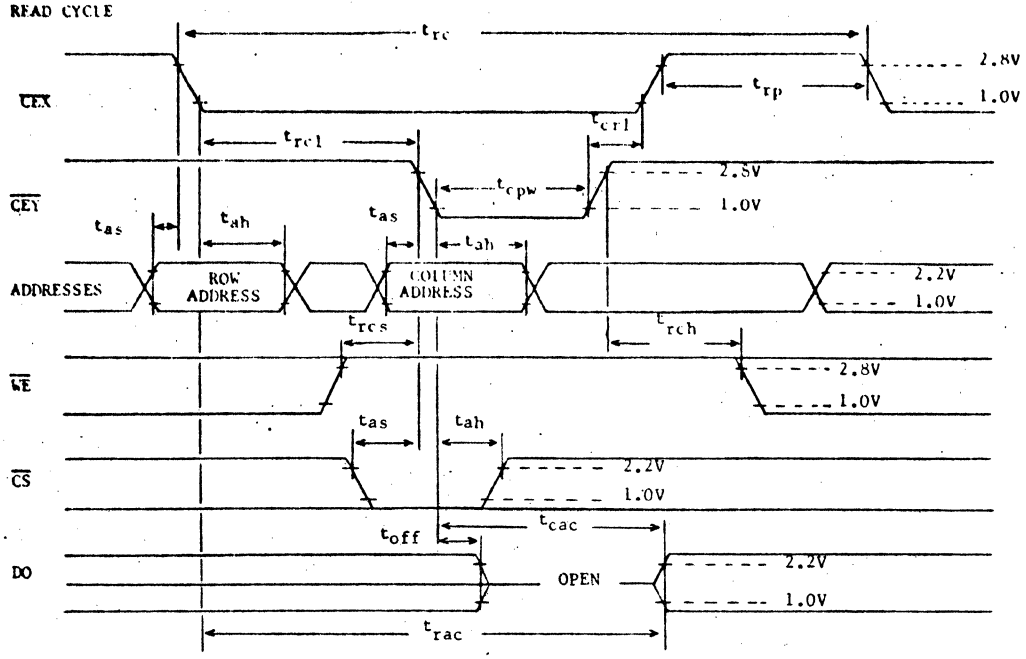
Read or Write Cycle Time		tRC	500 ns min.
Access Time From $\overline{CEX}$ Going Low		tRAC	290 ns max.
Access Time From $\overline{CEY}$ Going Low		tCAC	165 ns max.
Output Buffer Turn-off Delay		tOFF	80 ns max.
Pulse Width,			
Read Command		tRPW	165 ns min.
Write Command		tWP	165 ns min.
Column Address Strobe		tCPW	165 ns min.
Set-up Time,			
Read or Write Command	tRCS,	tWCS	0 ns
Address		tAS	0 ns
Data-In		tDS	0 ns
Hold Time,			
Read Command		tRCH	0 ns
Write Command		tWCH	130 ns min.
Address		tAH	85 ns min.
Data-In		tDH	130 ns min.
Row Address Strobe Precharge		tRP	125 ns min.
Row to Column Strobe Lead Time		tRCL	125 ns min.
Column to Row Strobe Lead Time		tCRL	-50 ns min.
			+50 ns max.
Write to Column Lead		tCWL	165 ns min.
Modify Time		tMOD	0 ns min.
			10 us max.
Refresh Time		tRFSH	2.1 ms max.

10) Interface Rules

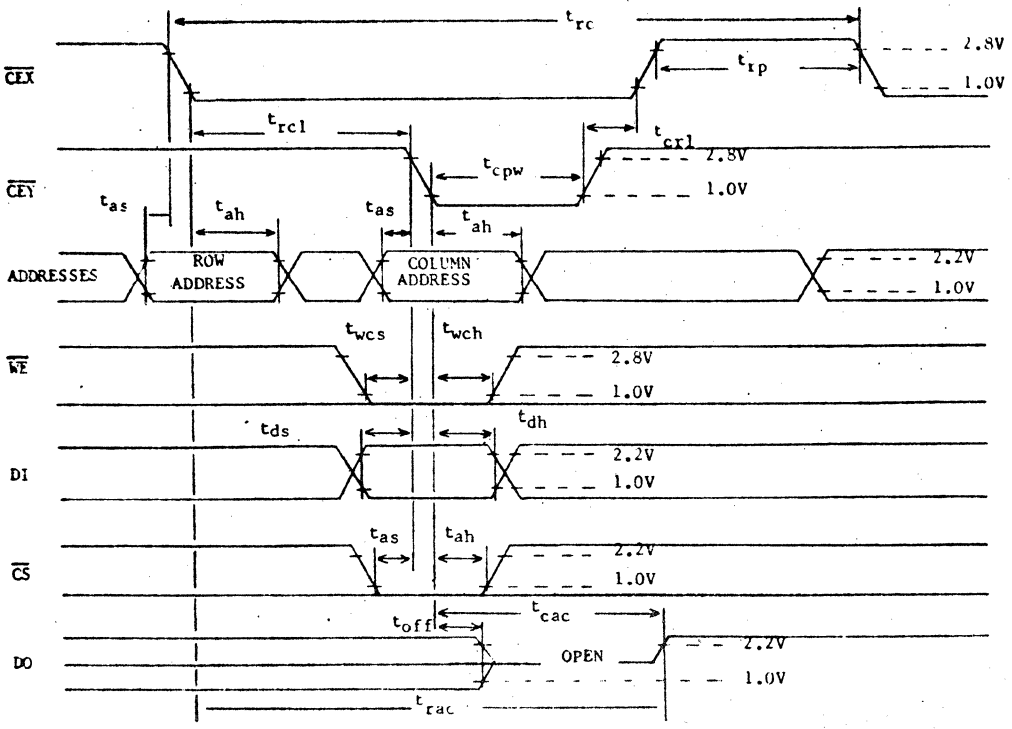
All inputs and output of the RAM2 are fully TTL compatible. The output, however, is limited in its Low level current sinking capability (1 TTL load). Interfacing the RAM2 with other logic families should be handled in conjunction with the Circuits Section.

RAM2

READ CYCLE

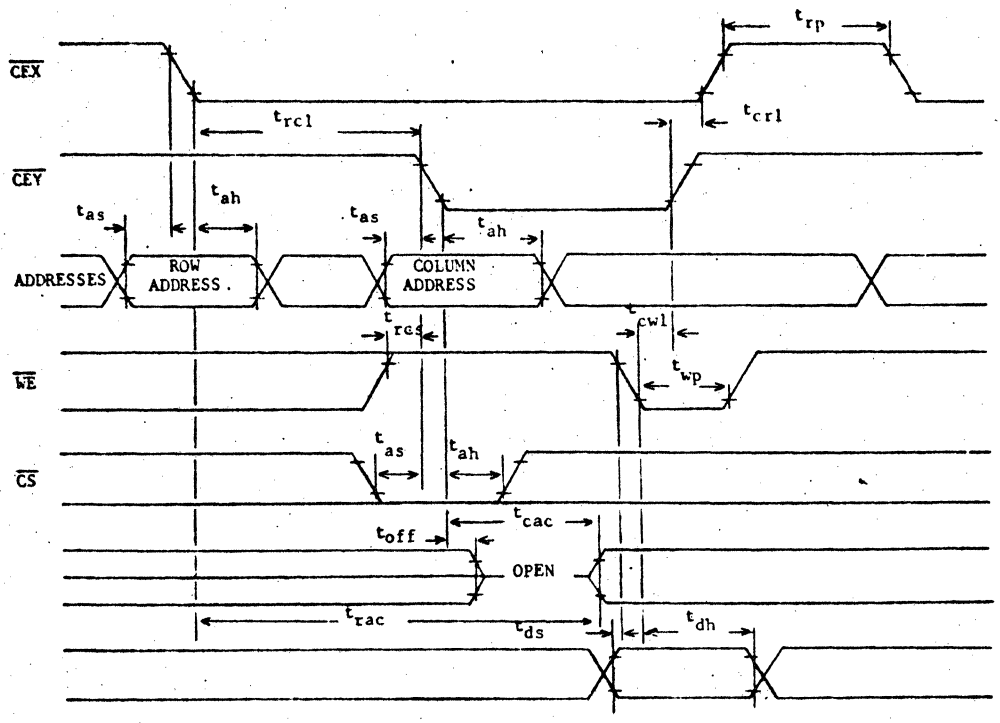


WRITE CYCLE



RAM2

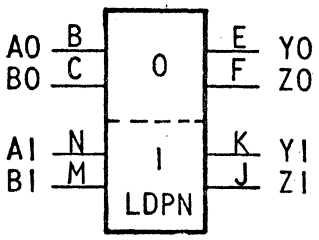
READ/MODIFY/WRITE CYCLE



3.4 INTERFACE CIRCUITS

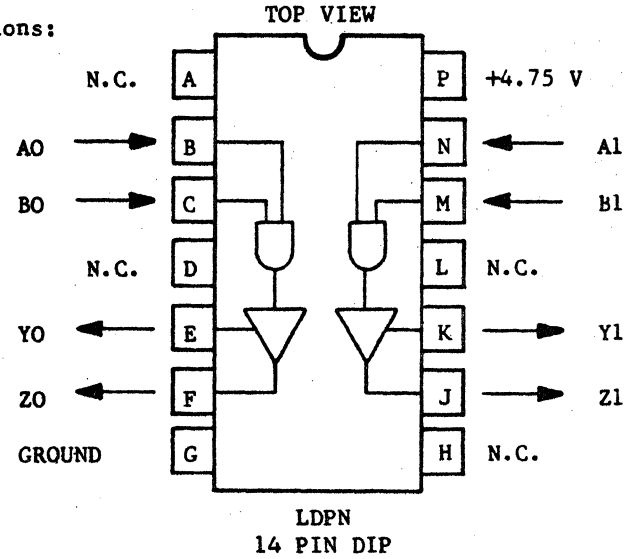
LDPN

Element Type	LDPN
Standard Assembly Number:	SA 2207 8299
Manufacturer/Manufacturer's Type:	National Semiconductor/DH0034C
Circuit Designation	Dual Interface Line Driver
Description of Operation:	



FUNCTIONAL DIAGRAM

Pin Locations:



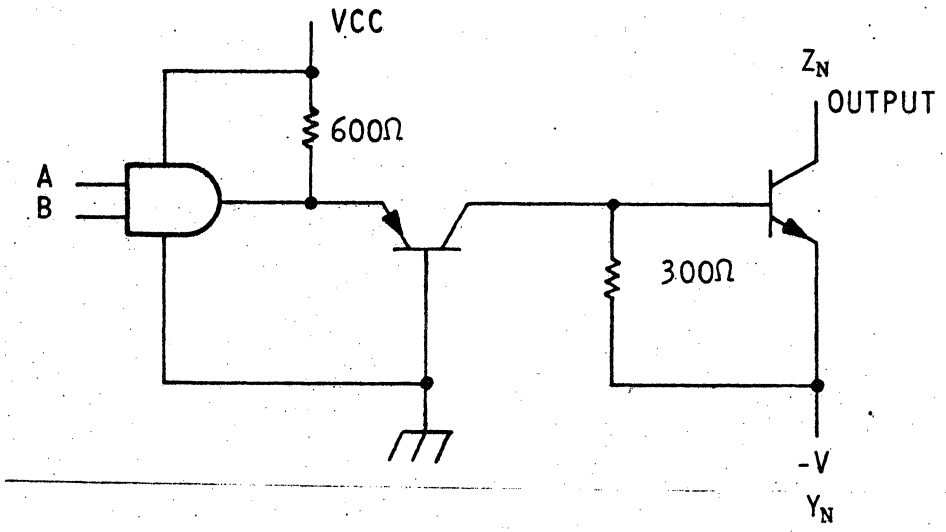
LDPN
14 PIN DIP

LDPN

1. This device is used for level shifting. The inputs are TTL compatible while the output levels are determined by the user's design for the output stage.

2. The collector and emitter of the output transistor are accessible through pins on the package.

3. Schematic :



4. Approximate Delay Time

tpd+ ≈ 60 ns
tpd- ≈ 25 ns

5. Consult Standard Circuits for applications of this device.

LRPN

3.4 Interface Circuits

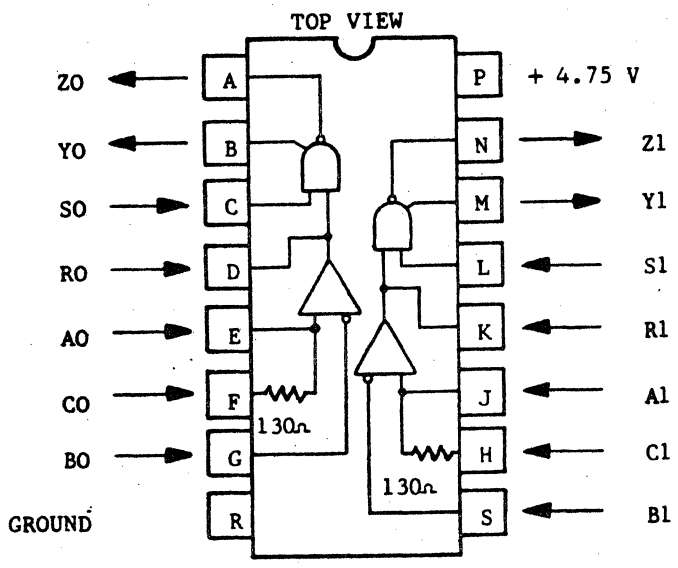
Element Type	LRPN
Standard Assembly Number:	SA 2207 8273
Manufacturer / Manufacturer's Type:	Fairchild/uA 9615
Circuit Designation	Dual Interface Line Receiver
Description of Operation:	

1. This device is a line receiver with differential inputs. It can receive ±500 mV of differential data. The output is TTL compatible.
2. One power supply nominally at 4.75V is required for operation.
3. The device has strobe inputs for each of the receivers, also available is a response control pin for controlling the response time with an external capacitor. The output has an uncommitted collector with an active pull-up available on an adjacent pin. A 130Ω terminating resistor is available at the input.
4. Approximate Delay Time

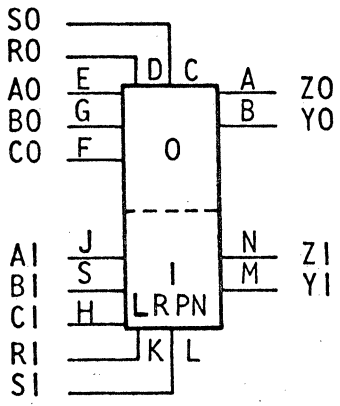
   tpd+ ≈ 75 ns
   tpd- ≈ 75 ns

5. Consult Standard Circuits for applications of this device.

Pin Locations:



LRPN
16 PIN DIP



FUNCTIONAL DIAGRAM

LDGN

Element Type: LDGN
Standard Assembly Number: 2201 7602
Manufacturer /Manufacturer's Type: Motorola MC1488L
Circuit Designation: Quad EIA Line Driver

Description of Operation:

1) T^2L Logic compatible circuit designed to interface terminal equipment with data communications equipment in conformance with the specifications of EIA standards RS-232-C.

2) The package consists of three, two-input AND gate drivers and a single input driver.

3) +12 volts and -12 volts power supplies are required.

4) Discrete diodes must be externally connected from both power lines to each package to meet all power-off fault conditions.

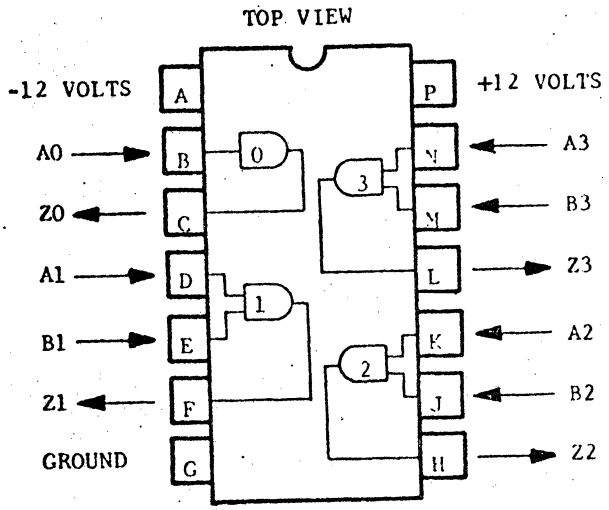
5) Inputs shall be driven by a restoring CTul element with a pull-down resistor connected to -2V supply as shown in Table I, Page 8, under SAMN.

6) A minimum capacity of 300 pf must be connected from each output terminal to ground to insure a slew of less than 30V/us. The slew = $\frac{dv}{dt} = \frac{1.2 \times 10^4}{C}$, where C is in pf, $\frac{dv}{dt}$ in volt/us.

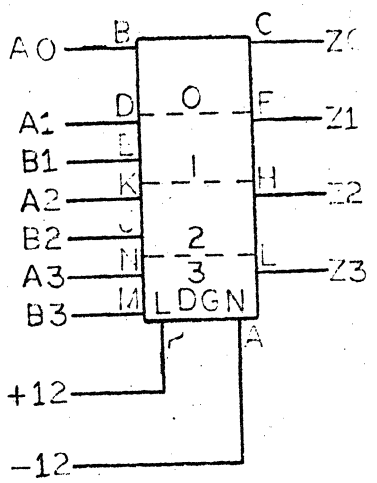
7) Output levels generated: VOH +6 volts @ Vin = .8 volt
VOL -6 volts @ Vin =1.9 volt

8) Propagation Delay Time = Tpd^- = 30ns @ 3KΩ and 15pf load
Tpd^+ = 250ns @ 3KΩ and 15pf load

PIN LOCATIONS



LDGN



FUNCTIONAL DIAGRAM

LRGN

Element Type	LRGN
Standard Assembly Number	2201 7628
Manufacturer/Manufacturer's Type	Motorola 1489 AL
Circuit Designation	Quad EIA Line Receiver

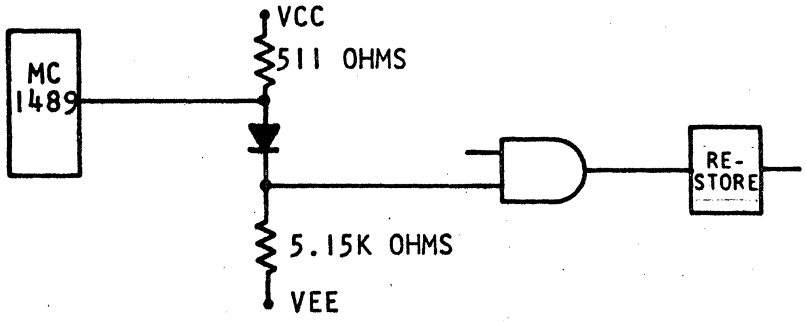
Description of Operation:

1) The circuit is T^2L logic compatible designed to interface between data communication and data processing equipment according to the EIA, RS-232C standards.

2) The package consists of four receivers. Each receiver has one input, a response-control, and a single T^2L compatible output.

3) +4.75 volts is the only power supply required.

4) Outputs shall drive CTuL restoring elements and a pull-up resistor connected to VCC supply as shown in Table II. Another possible connection to allow one level of gating is shown below:

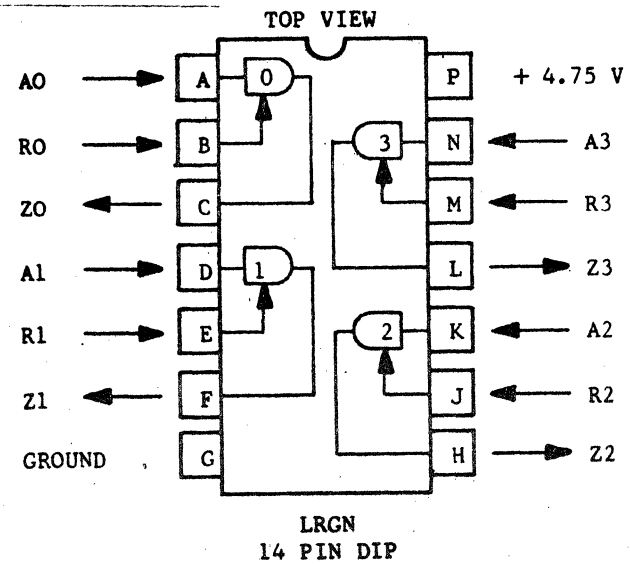


5) Any input level above +2.25 volts will result in a CTuL false output, and any input level more negative than +.75 volt will result in a CTuL true output, and open input will result in a CTuL true output.

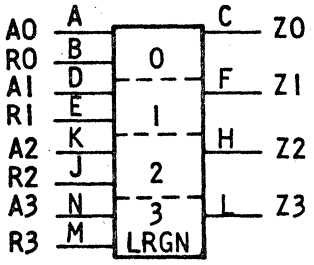
6) The response control is used to limit the receiver bandwidth to improve noise rejection. A capacitor is connected from the response control to ground to utilize this feature. Typically 500 pf capacitor allows the receiver to reject 500 ns maximum pulse at +6 volts maximum amplitude.

7) The propagation delay time = Tpd^- = 100 ns maximum
Tpd^+ = 60 ns maximum

Pin Locations:



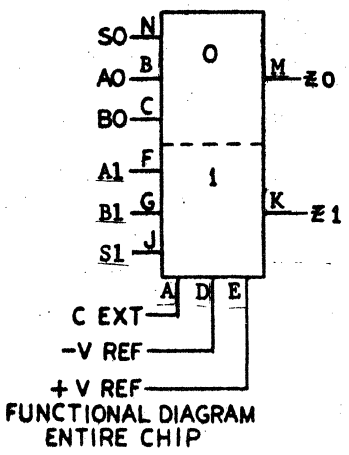
LRGN
14 PIN DIP



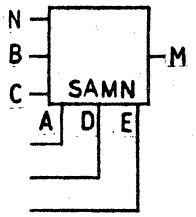
FUNCTIONAL DIAGRAM

SAMN

Element Type	SAMN
Standard Assembly Number:	1677 7682
Manufacturer/Manufacturer's Type:	TI/SN 7524
Circuit Designation	Dual Sense Amplifier
Description of Operation:	

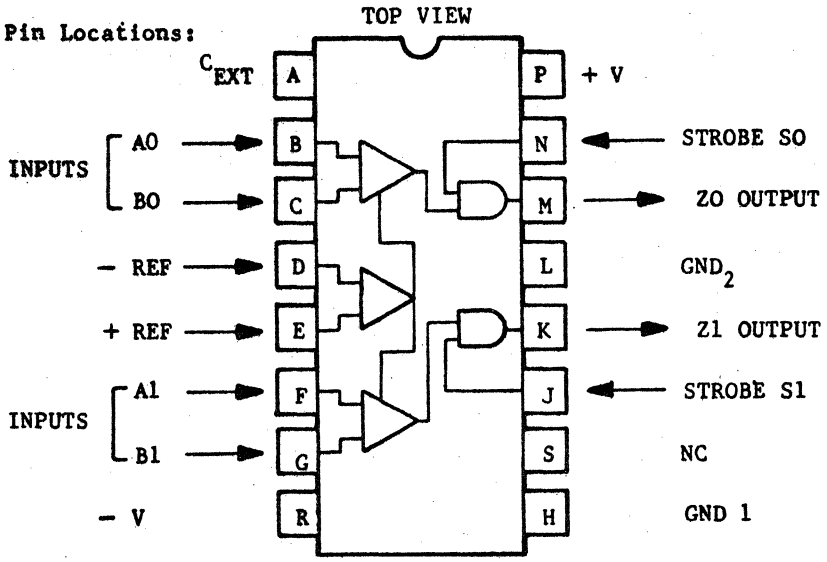


FUNCTIONAL DIAGRAM
ENTIRE CHIP



FUNCTIONAL
DIAGRAM
ONE DEVICE

Pin Locations:



SAMN
16 PIN DIP

SAMN

T^2L

16777682

DUAL SENSE AMPLIFIER

(1) The chip contains two linear sense amplifiers in a 16 DIP.

(2) Each amplifier has two independent signal inputs and one strobe input, but both have two common reference voltage inputs, -Vref and +Vref.

(3) Both signal inputs and reference inputs are differential Voltage inputs applied at the terminals of an input pair whether reference or signal. Strobe gate input is with respect to ground.

(4) Truth Table:

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

where A is a differential voltage between signal inputs pair. S is the strobe input.

(5) Power supplies used are +4.75v and -5v.

(6) The differential input threshold voltage applied at the terminals of the signal inputs is decided by the differential inputs at the reference terminals, Vref.

(7) Minimum Vin (True) = 21mv., Minimum Vout (True) = +1.5 @ Vref = 16mv.
Maximum Vin (False) = 12mv., Maximum Vout (False) = +.4v @ Vref = 16mv.

(8) Minimum Strobe (True) = +2.0v.
Maximum Strobe (False) = +.4v.

(9) External capacitor, Cext 100pf to ground insures stable operation.

(10) Maximum propagation delay time:
Positive going edge of signal to positive going edge of Vout = 40ns.
Negative going edge of signal to negative going edge of Vout = 60ns.
Positive going edge of strobe to positive going edge of Vout = 30ns.
Negative going edge of strobe to negative going edge of Vout = 30ns.

SAMN

TABLE I

EXTERNAL RESISTORS

	CTL Fan-out		No. of T^2L Loads Driven	Resistors			
	Spec.	Used		Value ohms	Tol. ° /°	Dissip. Watts	BURROUGHS Part No.
Pull-up	-	-	-	348	1	.25	
Pull-down	24	19	16	82.5	1	.50	1142 7002
	12	10	8	162	1	.25	1142 6921
	12	5	4	348	1	.25	1142 7002

TABLE II

COMBINED FAN-OUT/WIRE-OR CAPABILITY

No. of Wire-OR Outputs	Fan-out CTL Loads
Up to 16	Up to 3

SBMN

3.4 INTERFACE CIRCUITS

Element Type: SBMN

Standard Assembly Number: 1673 0004

Circuit Designation: Dual Comparator/Sense Amplifier

Description of Operation:

I Gate Characteristics:

1. V_{ih} = 2.0V minimum
2. V_{il} = .8V maximum
3. V_{ol} = .4V maximum @ I_i = 16ma
4. V_{oh} = 4.5V minimum @ 4.5ma
5. I_{oh} = .25ma maximum @ $V_o = V_{cc}$
6. I_{ih} (SO & S1) = 40μA maximum

   I_{ih} (SC) = 80μA maximum
7. I_{il} (SO & S1) = -1.6 mA maximum

   I_{il} (SC) = -3.2 mA maximum
8. T_{dl} -+ $\leq$ 17ns

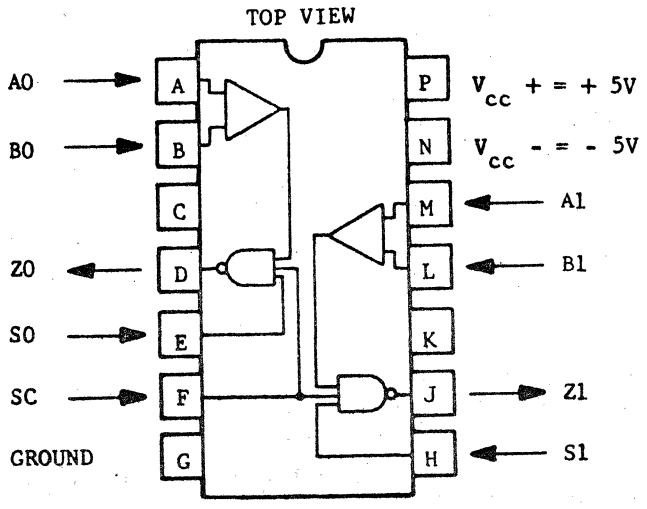
   T_{dl} +- $\leq$ 17ns

II Amplifier Characteristics:

1. I_{ih} = 75μA maximum @ V_i = 25mV, V_{ic} = $\pm$ 2.0VDC
2. I_{il} = -10μA maximum @ V_i = -25mV, V_{ic} = $\pm$ 2.0VDC
3. I_{is} = 10μA maximum @ V_i = $\pm$10mV
4. T_{dl}-- = 20ns
5. T_{dl}++ = 35ns

PIN LOCATIONS

TOP VIEW



IQAN

3.3 MOS INTEGRATED CIRCUITS (Continued)

Element Type:	IQAN
Standard Assembly Number:	1674 4971
Manufacturer / Manufacturer's Type:	CLR 5003
Circuit Designation:	Quad MOS Clock Driver
Description of Operation:	

(1) Four monolithic high voltage, high current inverters are contained in a 14 Pin DIP package.

(2) The driver is intended for use as an interface circuit to translate bipolar logic level signals to high voltage MOS signals.

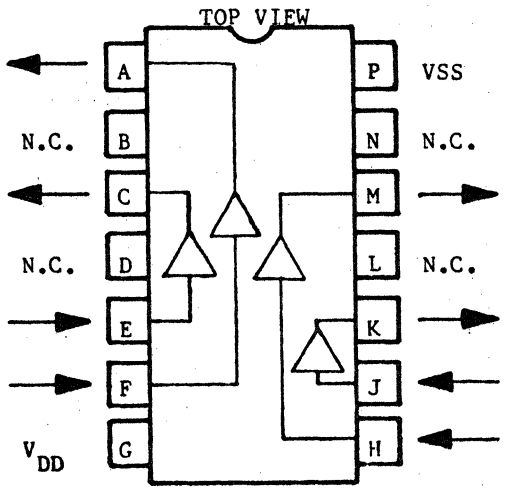
(3) Power Supplies:
Source supply of the MOS circuit (VSS)
Drain supply of the MOS circuit (VDD)

(4) Outputs:
Vout (High) = VSS-4 volts minimum
Vout (Low) = VDD+2 volts maximum
Iout (Peak) = ±60 ma maximum

(5) At VSS = +20V, VDD = 0
Vin (Low) = .6V maximum, Iin = +1.5 ma.
Vin (High) = +1.0V minimum, Iin = +8 ma.

(6) Propagation delay depends on VSS, VDD, and the load capacitance.
At VSS = 21V, VDD = Ground, and CL = 250pf td = 45ns maximum.

PIN LOCATIONS:



IQAN

LDAN

Element Type	LDAN
Standard Drawing Number	2600 2766
Manufacturer/Manufacturer's Type	Signetics/8T23 Texas Instruments/SN75123
Circuit Designation	**Dual IBM Interface Line Driver**

Description of Operation:

1. This dual line driver is designed to drive terminated lines such as coxial cables or twisted pair. This device meets the IBM System/360 IO Interface Specification for interface drivers. The outputs of these drivers may be wired 'OR'.

2. The inputs are TTL compatible.

3. Input Characteristics:

   a. V_{ih} = 2.0V minimum

   b. V_{il} = .8V maximum

   c. Input Clamp Voltage $V_{clamp} \leq |-1.5V|$ @ I_{il} = -12 mA

   d. $I_{il} \leq |-1.6|$ mA @ V_{il} = .4V

   e. $I_{ih} \leq$ 40 μA @ V_{ih} = 4.5V

4. Output Characteristics:

   a. $V_{oh} \geq$ 2.86V @ I_{oh} = 59.3 mA

   V_{cc} = 4.75V

   b. $V_{ol} \leq$ .15V @ I_{ol} = -240 μA

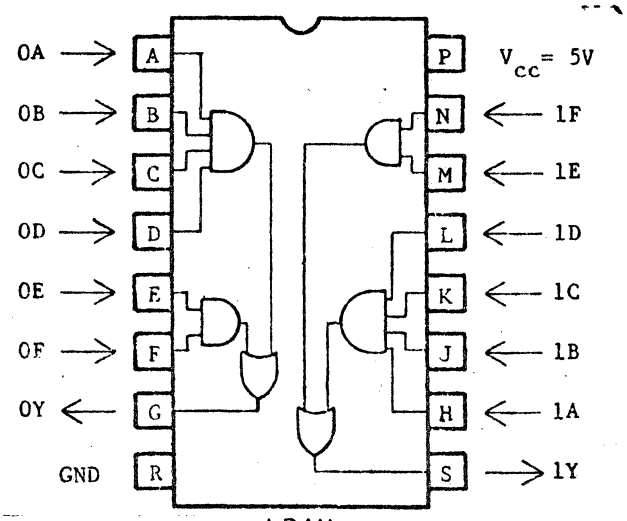
   c. Output Leakage Current $\leq$ 40 μA @ V_{oh} = 3.0V

5. Delay Times:

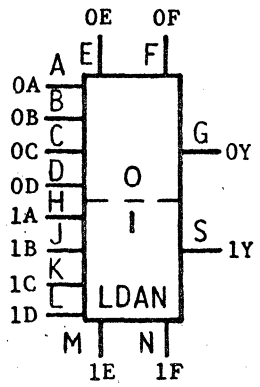
   a. The delay times are specified for a load of 50n in parallel with 100 pf to ground.

      1. Turn - on Delay $\leq$ 25 ns
      2. Turn - off Delay $\leq$ 35 ns

Pin Locations:



LDAN
Positive Logic Y = ABCD+EF

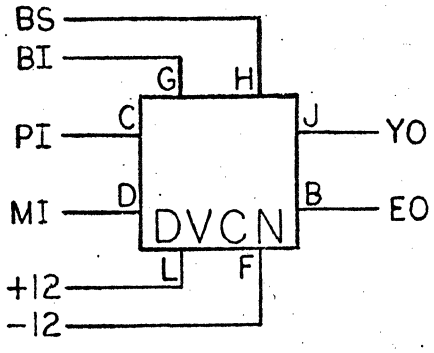


FUNCTIONAL DIAGRAM

DVCN

3.4 Interface Circuits

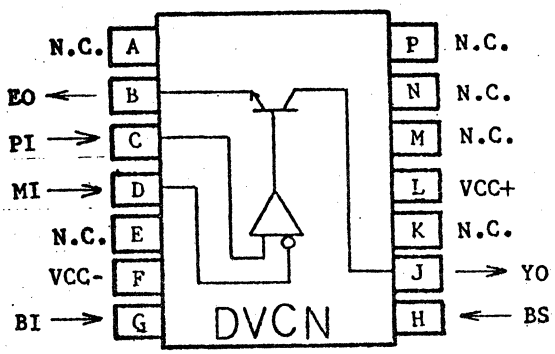
Element Type: S-1269 7041
Standard Assembly Number: T.I./72311
Manufacturer/Manufacturer's Type: Differential Comparator
Circuit Designation:
Description of Operation:



FUNCTIONAL DIAGRAM

Pin Locations:

TOP VIEW



1) This device is primarily used in the BDI interface. It is designed to operate from Vcc+ = 5 volts, Vcc- = Ground to Vcc+ =+15 volts, Vcc- =-15 volts, and all inputs and outputs can be completely isolated from system ground if desired.

2) There are two differential inputs to the device, PI and MI. A maximum of 10 mV of offset voltage is necessary to drive the output HIGH or LOW. Offset and bias currents into the differential inputs are negligible.

3) Both the collector (YO) and the emitter (EO) of the output transistor are brought out to package pins.

   Max voltage between YO and Vcc- = 35 volts
   Max voltage between EO and Vcc- = 25 volts

   $V_{OL} \leq 0.4V$ @ 8mA collector current with input offset $\geq$ 10 mV

   $V_{OL} \leq 1.5V$ @ 50mA collector current with input offset $\geq$ 10mV

4) Balance (BI) and balance/strobe (BS) inputs are provided. To balance the output, a 3KΩ trimpot is connected between BI and BS, with the wiper connected to Vcc+ through a 3KΩ resistor. To strobe, BS is forced LOW, and the output transistor is turned OFF regardless of all other inputs.

   Low Level (0.4V) strobe input current ≤ -4.0mA

5) Approximate delay times:

   $T_{pd}+ \approx 150$ nsec

   $T_{pd}- \approx 215$ nsec

6) Information regarding the use and applications of this device is available upon consultation with Standard Circuits. This device is intended for use in the BDI Line Adapter.

LDDN

3.2 TTL/DTL Integrated Circuits

Element Type:	LDDN
Standard Assembly Number:	2475 2222
Manufacturer's Type:	75110
Circuit Designation:	Dual Line Driver
Description of Operation:	

Dual Line Driver

1) Two TTL compatible (12ma) Line Drivers are contained in a 14 pin Dual in Line package.
2) The Line Driver operates on a nominal $\pm$ 5V supply.
3) The inhibit feature allows the devices to be used in party-line or data-bus applications.
4) V_{IH} Max = 5.5v Min = 2V

   V_{IL} Max = 0.8v Min = 0V
5) Input Currents (High Level)

Inputs	V_{IH} = 2.4v	I_{IH} = 40μA Max
Inhibits (C1,C2)	V_{IH} = 2.4v	I_{IH} = 40μA Max
Inhibits (D)	V_{IH} = 2.4V	I_{IH} = 80μA Max

6) Input Currents (Low Level)

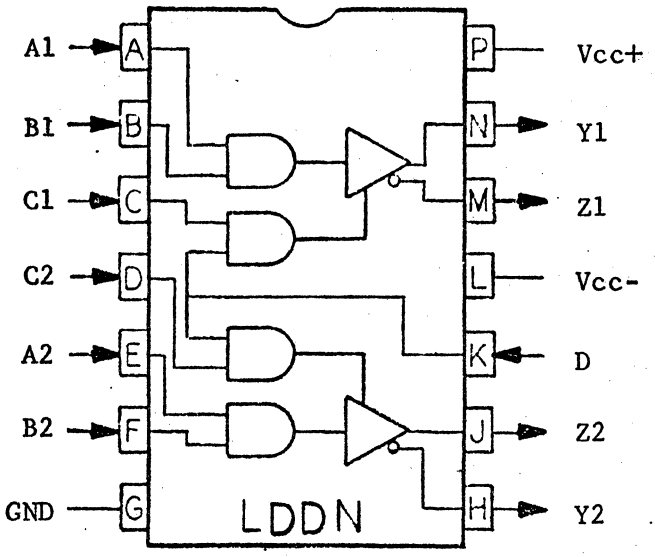
Inputs	V_{IL} = 0.4v	I_{IL} = -3 ma Max
Inhibits (C1,C2)	V_{IL} = 0.4v	I_{IL} = -3 ma Max
Inhibits (D)	V_{IL} = 0.4v	I_{IL} = -6 ma Max

7) On state output current 3.5 ma Min, 6.5 ma Max. with V_{cc} $\pm$ Min.
8) OFF state output current 100 μA Max. with V_{cc} $\pm$ Min.
9) At C_L = 40 pf and R_L = 50 Ω

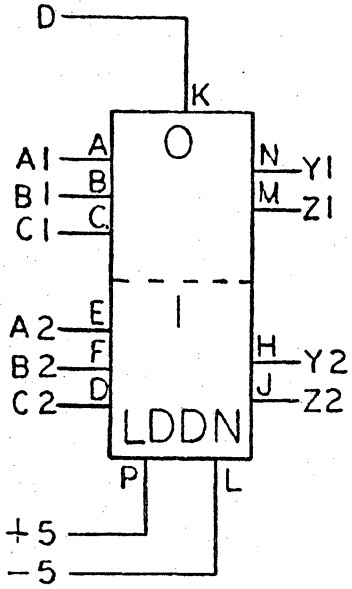
   Propagation delay input to output td = 20ns Max.

   Propagation delay inhibit to output td = 30ns Max.
10) This device is intended for use in the BDI Line Adapter ONLY.

    Information regarding its use or application is available from Standard Circuits.



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

LOGIC INPUTS		INHIBIT DR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	H	H
X	X	X	L	H	H
L	X	H	H	L	H
X	L	H	H	L	H
H	H	H	H	H	L

TRUTH TABLE

X = Don't care

Low output represents the on state

High output represents the off state

IQBN

3.4 Interface Circuits

Element Type:	IQBn
Standard Assembly Number:	1673 0319
Manufacturer/Manufacturer's Type:	Intel/3207
Circuit Designation:	Quad Bipolar-to-MOS Level Shifter and Driver

Description of Operation:

1) The IQBn is quad bipolar to MOS level shifter and driver with TTL compatible inputs.

2) The device operates with three power supplies and one ground. One supply is V_{CC} intended for use by the bipolar input section. It also uses V_{SS} and V_{BB} for the MOS section.

3) The IQBn has two enable inputs for each pair of data inputs.

4) Input Currents

Data	-0.25mA @ V_i = 0.45V	.01mA @ V_i = 5.0V
Enables	-0.50mA @ V_i = 0.45V	.02mA @ V_i = 5.0V

5) Input Voltages

V_{IL} = .80V Max. V_{IH} = 2.0V Min.

6) Output Currents

I_{OL} = 100mA @ V_o = 4V I_{OH} = -100mA @ V_o = V_{SS} - 4V

V_{CC} = 5.0V V_{BB} = 22V V_{SS} = 19V

7) Output Voltages

V_{OL} = 0.8 Max. with all inputs at 2.0V

V_{OH} = V_{SS} - 0.8V with all inputs at .85V

8) Delays

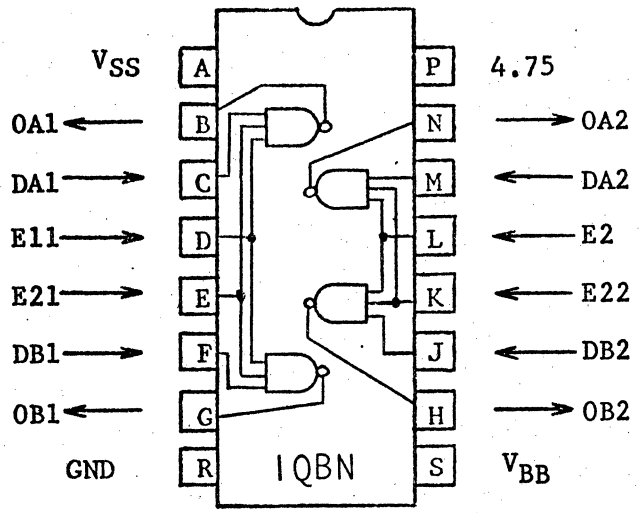
Input to Output Leading edge tpd+ = 20.0 ns @ C_L = 100 pf
= 24.0 ns @ C_L = 200 pf

Input to Output Trailing edge tpd- = 29.0 ns @ C_L = 100 pf
34.0 ns @ C_L = 200 pf

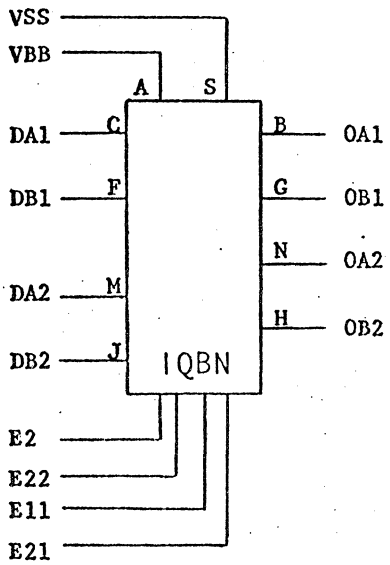
Output Rise Time 20 ns Max at C_L = 100 pf and 30 ns Max. at C_L = 200 pf

Output Fall Time 25 ns Max at C_L = 100 pf and 35 ns Max. at C_L = 200 pf

9) Maximum skew between any output in the same package is less than or equal to 7 ns.



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

T1BR

3.4 Interface Circuits (Continued)

Element Type:	T1BR
Standard Assembly Number:	2604 2044
Manufacturer/Manufacturer's Type:	National/DM8837 Signetics/8T37
Circuit Designation:	Hex Bus Receiver with Hysteresis

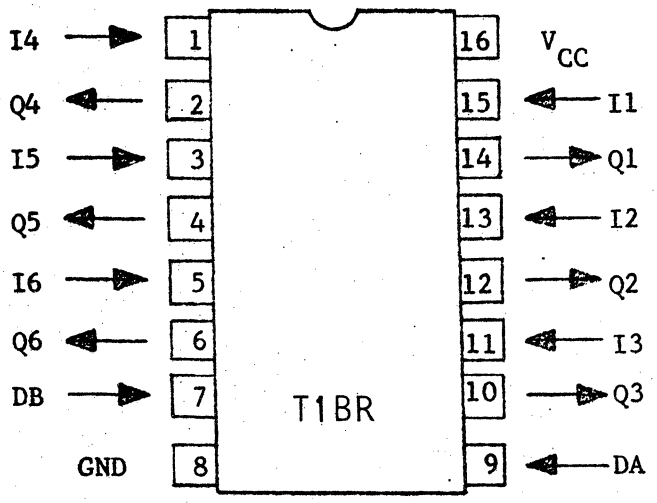
Description of Operation:

1) The T1BR is a hex bus receiver with hysteresis organized as two triple receivers with separate disable lines for each group. It is a TTL monolithic integrated circuit in a 16 pin DIP.

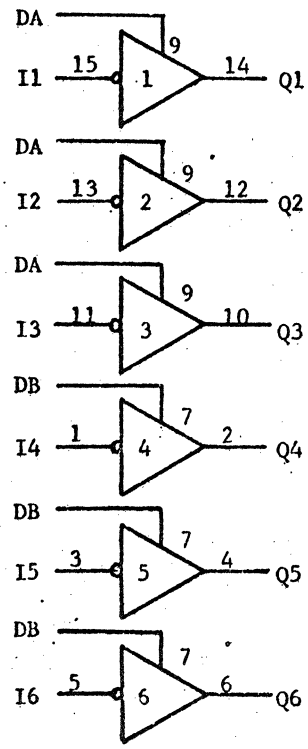
2) A "High" on the disable input (DA or DB) will force the corresponding receiver outputs Low. When enabled (disable input Low), the receiver senses the voltage level on the bus line and inverts it at the output.

3) Electrical Characteristics:

Input Threshold Voltages	
Disable Inputs DA, DB	
Vil max.	0.8V
Vih min.	2.0V
Receiver Inputs I6-I1	
Vil max.	0.8V
Vih min.	2.5V



PIN LOCATION DIAGRAM



FUNCTIONAL DIAGRAM

Interface T18R 2604 2044

Noise Margin, Receiver Inputs 0.85V

Output Voltages
- Vol max. 0.4V @ Iol = 16 mA
- Voh min. 2.4V @ Ioh = -400 uA

Input Loading
- Disable Inputs DA, DB
  - Iil max. -3.2 mA @ Vil = 0.4V
  - Iih max. 50 uA @ Vih = 2.4V
- Receiver Inputs I6-I1
  - Iil max. 10 uA @ Vil = 0.4V
  - Iih max. 50 uA @ Vih = 2.4V

Output Drive
- Iol 16 mA @ Vol = 0.4V
- Ioh -400 uA @ Voh = 2.4V

4) Switching Characteristics:

Propagation Delay, max.

Receiver Input to Output	td-+	43 ns
	td+-	37 ns
Disable Input to Output	td-+	18 ns
	td+-	18 ns

5) Interface Rules

The outputs and disable inputs of the T18R are fully TTL compatible. The receiver inputs have built-in hysteresis to provide extra noise immunity. This means input voltage to the receiver must cross over the Vil or Vih thresholds to guarantee correct response. Once achieved, the input can increase (from Vil max.) or decrease (from Vih min.) for the amount <= the noise margin and the output will not change. The low input current to the receiver inputs allows up to 27 driver/receiver pairs to be tied to a common bus.

Choice of external terminations on the bus line should be handled in conjunction with Circuits.

S140

3.4 Interface Circuits

Element Type:	S140
Standard Assembly Number:	2602 2889
Manufacturer/Manufacturer's Type:	T.I./74S140 Fairchild/9S140
Circuit Designation:	Dual 4-Input NAND Line Driver

Description of Operation:

1) The S140 performs a dual 4-Input NAND function. Its high current Totem-Pole output stage can drive 40mA while maintaining a +2.0V true level output voltage and can sink 60mA while maintaining a +0.5V False level.

2) Input Currents:

I_{IL} = 4.0mA @ V_i = 0.5V I_{IH} = .08mA @ V_i = 2.4V

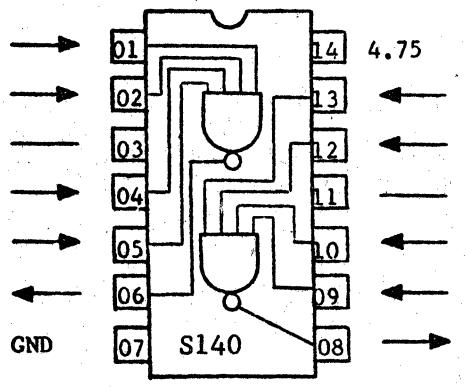
3) Output Drive:

I_{OL} = 60mA @ V_o = 0.5V I_{OH} = 40mA @ V_o = 2.1V

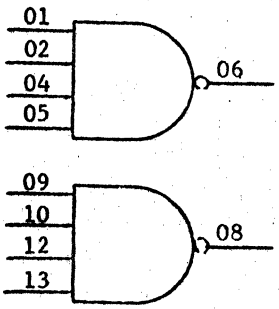
4) This device should not be used to directly interface to CTL elements because of considerably reduced low level noise margin.

5) Propagation Delays:

Input to Output tpd+ = 13 ns
tpd- = 13 ns



PIN LOCATION DIAGRAM

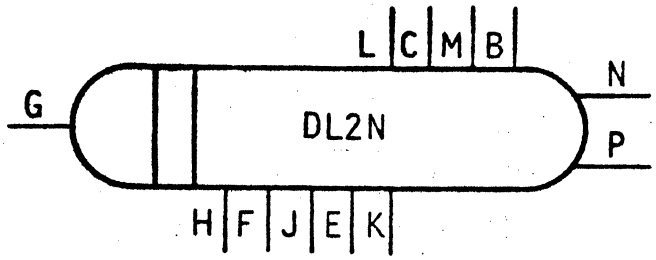


FUNCTIONAL DIAGRAM

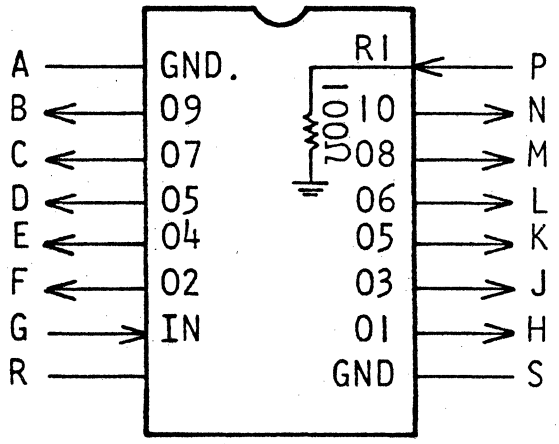
3.5 MISCELLANEOUS CIRCUITS

20 NSEC DELAY LINE

DL2N SA 2200 8478



FUNCTIONAL DIAGRAM
PINS "D" AND "K" ARE SAME TAP



PIN LOCATION DIAGRAM
16 PIN DIP

DL2N

20 NS DELAY LINE

1) The input should be driven by a restored element with fanout capability of 20 loads. A 178 ohm 1/4 watt resistor to -2 volts must terminate the input net.

2) The delay line output should be terminated at T10 by a 100 ohm 1/4 watt resistor to ground. The internal resistance may be used for this purpose by connecting pins P and N.

3) Maximum loading per package is 2 buffers and 4 no load gates or 6 no load gates, and the gates should be restored.

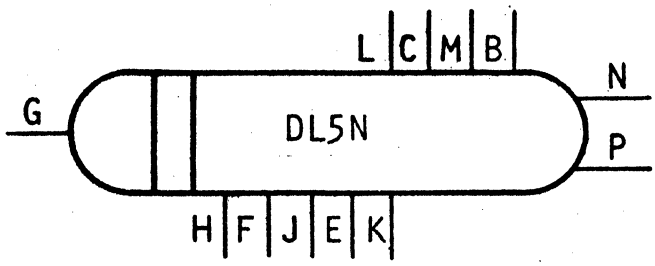
4) Total delay is 20 $\mp$ 2ns broken into 10 equal increments, each is 2 $\mp$ 1 ns referenced to the input as shown in the table below:

PIN	TIME DELAY (ns)
H	2
F	4
J	6
E	8
K	10
L	12
C	14
M	16
B	18
N	20

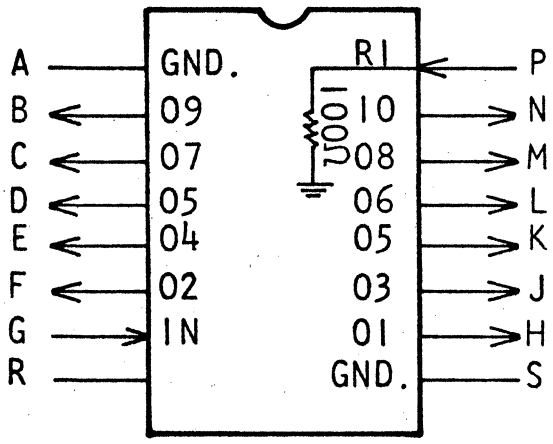
NOTE: The worst case tap to tap delay for this device shall be $\leq$ 3nS.

50 NSEC DELAY LINE

PE DL5N SA 2200 8486



FUNCTIONAL DIAGRAM
PINS "D" & "K" ARE SAME TAP



PIN LOCATION DIAGRAM
16 PIN DIP

DL5N

50 NS DELAY LINE

1) The input should be driven by a restored element with fanout capability of 20 loads. A 178 ohm 1/4 watt resistor to -2 volts must terminate the input net.

2) The delay line output should be terminated at T10 by a 100 ohm 1/4 watt resistor to ground. The internal resistance may be used for this purpose by connecting pins P and N.

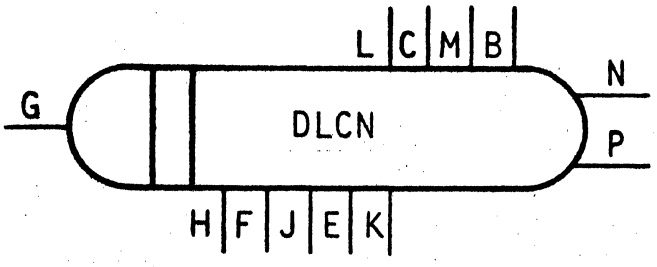
3) Maximum loading per package is 2 buffers and 4 no load gates or 6 no load gates, and the gates should be restored.

4) Total delay is 50 $\mp$ 3 ns broken into 10 equal increments, each is 5 $\mp$ 2 ns referenced to the input as shown in the table below:

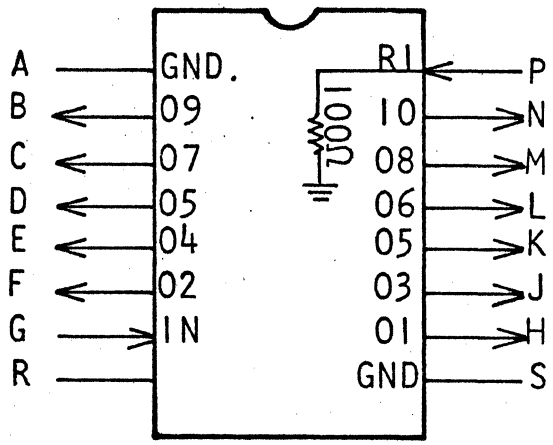
PIN	TIME DELAY (ns)
H	5
F	10
J	15
E	20
K'	25
L	30
C	35
M	40
B	45
N	50

100 NSEC DELAY LINE

PE DLCN SA 2200 8494



FUNCTIONAL DIAGRAM
PINS "D" & "K" ARE SAME TAP



PIN LOCATION DIAGRAM
16 PIN DIP

DLCN

100 NS DELAY LINE

1) The input should be driven by a restored element with fanout capability of 20 loads. A 178 ohm 1/4 watt resistor to-2 volts must terminate the input net.

2) The delay line output should be terminated at T10 by a 100 ohm 1/4 watt resistor to ground. The internal resistance may be used for this purpose by connecting pins P and N.

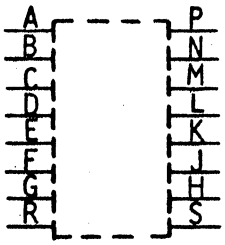
3) Maximum loading per package is 2 buffers and 4 no load gates or 6 no load gates, and the gates should be restored.

4) Total delay is 100 $\mp$ 5 ns broken into 10 equal increments, each is 10 $\mp$ 3 ns referenced to the input as shown in the table below:

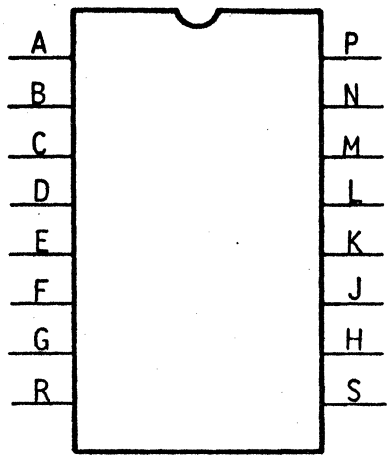
PIN	TIME DELAY (ns)
H	10
F	20
J	30
E	40
K	50
L	60
C	70
M	80
B	90
N	100

GENERAL BLACK BOX FOR DISCRETE COMPONENTS

GBNN



SPACE REQUIREMENTS FOR COMPONENTS DICTATES NUMBER OF INPUT/OUTPUT LINES. SPACE NEEDS MAY NECESSITATE TRANSCRIPTION OF MORE THAN ONE GBNN.



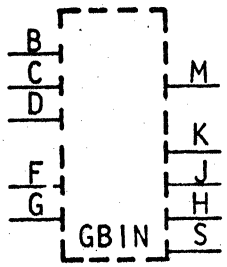
PIN LOCATION DIAGRAM
16 PIN DIP

DTL TO CTL LEVEL CHANGER

PART #1

GBIN

2204 4291



GBIN & GB2N MUST BE CHIPLOCKED TOGETHER, SAME LINE, GBIN ON LEFT

SEE PAGE 30 FOR THE CIRCUIT SCHEMATIC

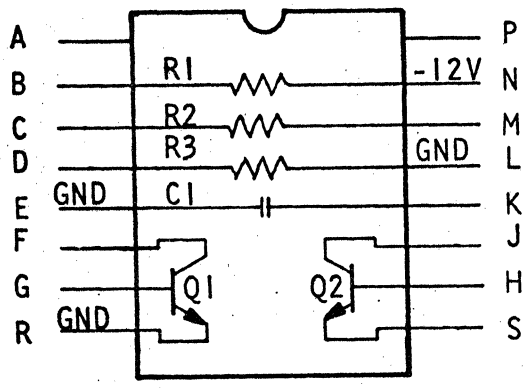
R1 - 562 Ω ¼W. 1111 8676

R2 - 511 Ω ¼W. 1111 8668

R3 - 196 Ω ¼W. 1111 8569

C1 - 100UUF 100V CAP 1100 9487

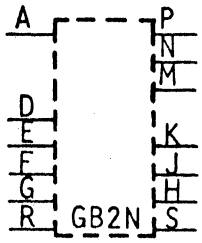
Q1, Q2 - TRANSISTOR-TYPE BA 1123 7336



PIN LOCATION DIAGRAM
16 PIN DIP

DTL TO CTL LEVEL CHANGER
PART #2
GB2N

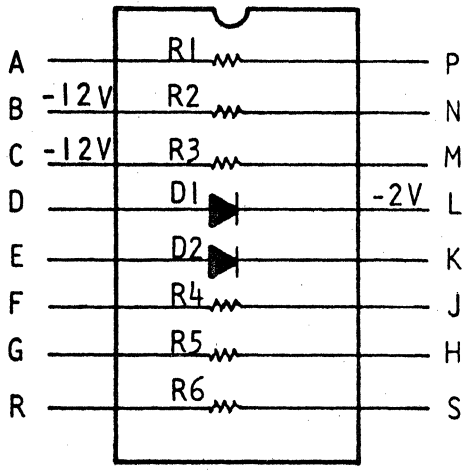
2204 4309



GBIN & GB2N MUST BE CHIPLOCKED TOGETHER, SAME LINE, GBIN ON LEFT

SEE PAGE 30 FOR INTERCONNECTIONS

R1 - 61.9Ω 1111 8445
R2 - 10K Ω 1111 8973
R3 - 2.87KΩ 1111 8841
R4 - 19.6KΩ 1111 9047
R5 - 1KΩ 1111 8734
R6 - 825Ω 1111 8718
D1, D2 - DIODE-SIL 1N4448 2208 6011

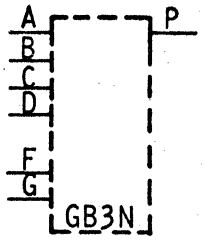


PIN LOCATION DIAGRAM
16 PIN DIP

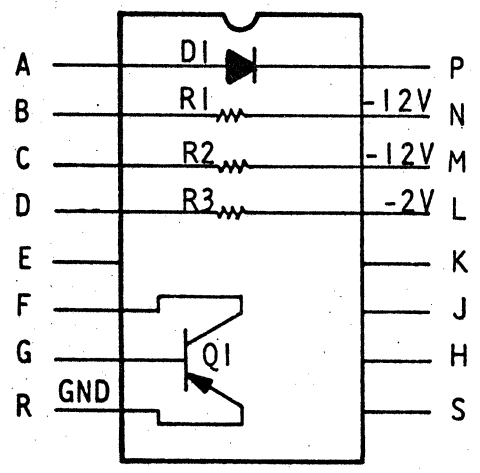
CTL TO DTL LEVEL CHANGER

GB3N

2204 4319



D1 - DIODE-TYPE 23		1124 1023
R1 - 1.21K ¼W		1111 8759
R2 - 511Ω ¼W		1111 8668
R3 - 1KΩ ¼W		1111 8734
Q1 - TRANSISTOR-TYPE	BD	1123 7369

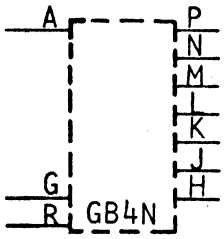


PIN LOCATION DIAGRAM
16 PIN DIP

CTL TO MOS CLOCK CONVERSION

PART #1

GB4N
2204 4325



TWO GB4N'S, ONE GB5N & ONE GB6N MUST BE CHIPLOCKED TOGETHER, ON TWO ROWS, GB4N & GB5N ON UPPER ROW GB4N & GB6N ON LOWER ROW. FOR SCHEMATIC AND INTERCONNECTION DIAGRAM, SEE SSRN CHIP. Section 3.3 PAGE 11

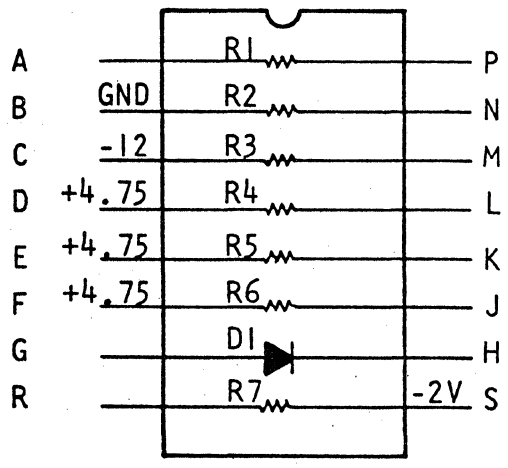
R1 - 178Ω ½W 1111 8551

R2 - 196Ω ½ W 1111 8569

R3, R7 - 681Ω ½W 1111 8692

R6, R4, R5 - 1.47KΩ ½W 1111 8775

D1 - DIODE-TYPE 4 1170 4855



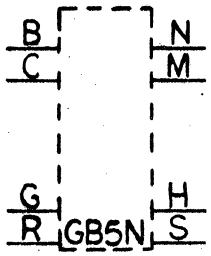
PIN LOCATION DIAGRAM
16 PIN DIP

CTL TO MOS CLOCK CONVERSION

PART#2

GB5N

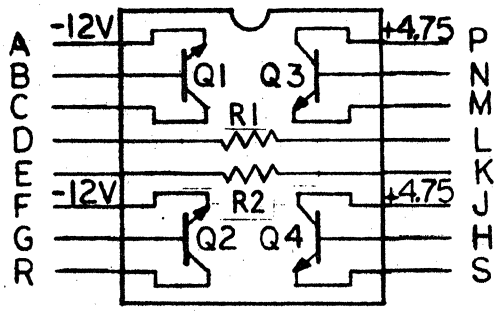
2204 4333



GB5N MUST BE USED WITH GB4N & GB6N.
SEE SHEET FOR GB4N FOR DETAILS.

Q1, Q2, Q3, Q4 - TRANSISTOR-TYPE BJ 1141 6062

R1, R2 — 287 OHM ¼ W 1111 8601



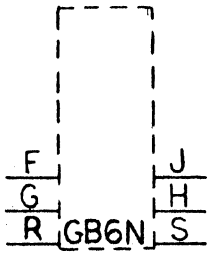
PIN LOCATION DIAGRAM
16 PIN DIP

CTL TO MOS CLOCK CONVERSION

PART # 3

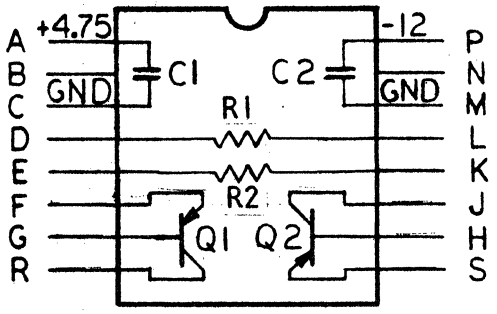
GB6N

2204 4341



GB6N MUST BE USED WITH GB4N & GB5N
SEE SHEET FOR GB4N FOR DETAILS

C1, C2	1.0UF 50V CAP.	1907 8815
Q1, Q2	TRANSISTOR-TYPE AT	1120 0482
R1, R2	287 OHM ¼ W	1111 8601



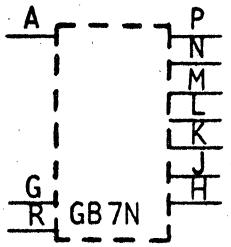
PIN LOCATION DIAGRAM

CTL TO MOS CLOCK CONVERSION

PART #4

GB7N

2210 9821



ONE GB4N, ONE GB7N, ONE GB8N & ONE GB9N MUST BE CHIPLOCKED TOGETHER, ON TWO ROWS, GB7N & GB8N ON UPPER ROW GB4N & GB9N ON LOWER ROW. FOR SCHEMATIC AND INTERCONNECTION DIAGRAM, SEE SSRN CHIP. Section 3.3 PAGE 13

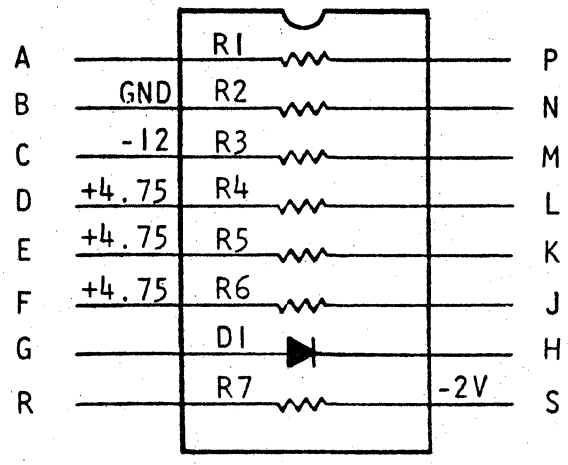
R1 - 178Ω ¼W 1111 8551

R2 - 750 Ω 1/4 W 1111 8700

R3, R7 - 681Ω ¼W 1111 8692

R6, R4, R5 - 1.47KΩ ¼W 1111 8775

D1 - DIODE-TYPE 4 1170 4855



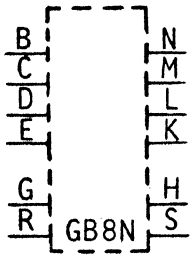
PIN LOCATION DIAGRAM
16 PIN DIP

CTL TO MOS CLOCK CONVERSION

PART #5

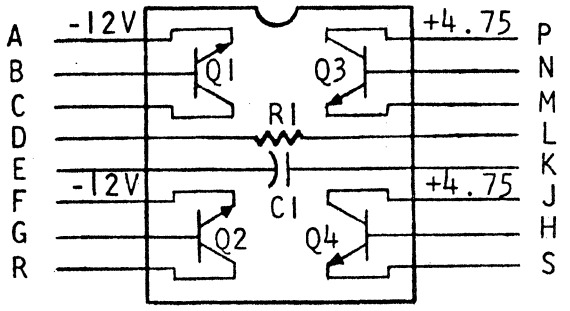
GB8N

2210 9839



GB8N MUST BE USED WITH GB4N, GB7N, & GB9N
SEE SHEET FOR GB7N FOR DETAILS

R1 - 287Ω ½W 1111 8601
C1 - 82pf 2208 7837
Q1, Q2, Q3, Q4 - TRANSISTOR-TYPE BJ 1141 6062



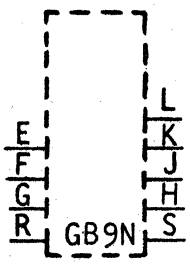
PIN LOCATION DIAGRAM
16 PIN DIP

CTL TO MOS CLOCK CONVERSION

PART #6

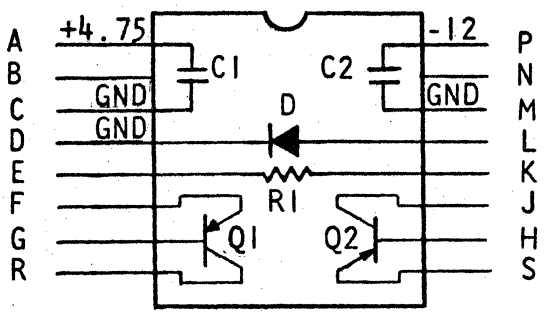
GB9N

2210 9847

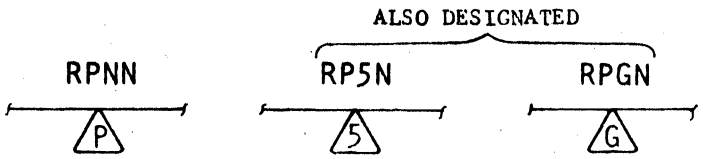


GB9N MUST BE USED WITH GB4N, GB7N & GB8N
SEE SHEET FOR GB7N FOR DETAILS

D - DIODE-TYPE 23 1124 1023
C1, C2 - 1.0UF 50V CAP. 1907 8815
Q1, Q2 - TRANSISTOR-TYPE AT 1120 0482
R1 - 3.16K 1/4 W 1111 8858



PIN LOCATION DIAGRAM
16 PIN DIP



3.5 MISCELLANEOUS CIRCUITS (Continued)

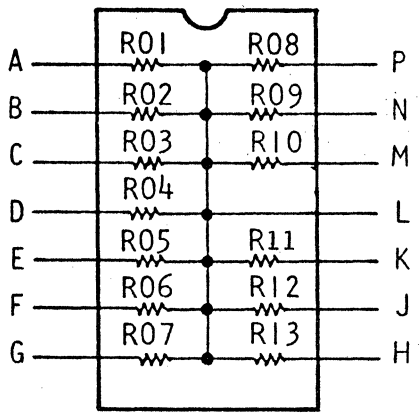
Element Type:	**RPNN**
Standard Assembly Number:	2200 8320
Manufacturer/Manufacturer's Type:	CTS
Circuit Designation:	500 ohm Resistor Pack
Description of Operation:	

(1) The RPNN is a resistor network containing 13 thick film resistors in a 14 pin DIP.

(2) Each resistor is 500Ω ± 5%

(3) Maximum Power Dissipation/Resistor: 77mW
Maximum Power Dissipation/Package: 1000mW

RPNN - PIN L CONNECTED TO -2.0V
RP5N - PIN L CONNECTED TO +4.75V
RPGN - PIN L CONNECTED TO GND



R01—R13 = 500 Ω

PIN LOCATION DIAGRAM
14 PIN DIP

RP2N
13 RESISTOR PACKAGE
S 2205 6188

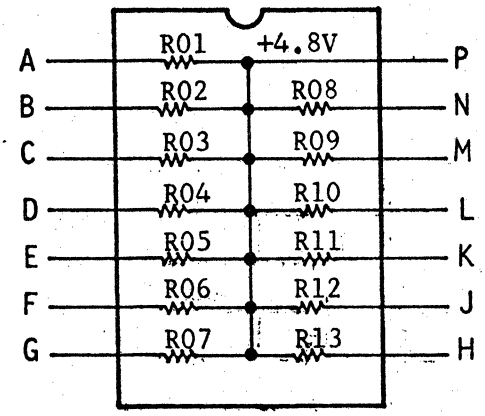
⚠2 FUNCTIONAL DIAGRAM

SPECIFICATION

Rx = 2.2 K OHMS

MAXIMUM POWER PER LOAD: 0.375 MW

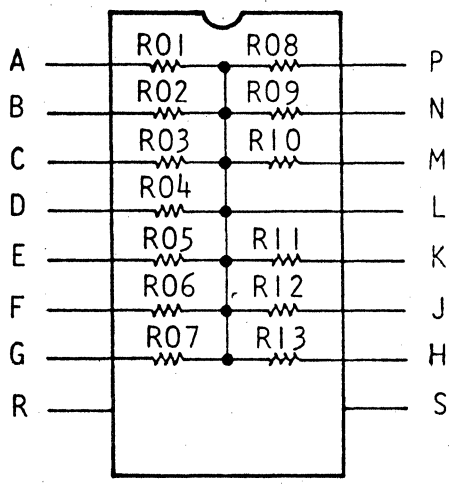
MAXIMUM POWER PER PACKAGE: 1.5 WATTS



PIN LOCATION DIAGRAM
14 PIN DIP

13 MIXED RESISTOR PACK

	RP6N		RP8N	
	VALUE	L	VALUE	L
R01	420	4	420	4
R02	280	6	210	8
R03	280	6	210	8
R04	335	5	560	3
R05	280	6	210	8
R06	280	6	210	8
R07	420	4	420	4
R08	420	4	420	4
R09	280	6	210	8
R10	280	6	210	8
R11	280	6	210	8
R12	280	6	210	8
R13	420	4	420	4



PIN LOCATION DIAGRAM
16 PIN DIP

RP6N - PIN L CONNECTED TO -2.0V
RPYN - PIN L CONNECTED TO +4.75V
RPZN - PIN L CONNECTED TO GND

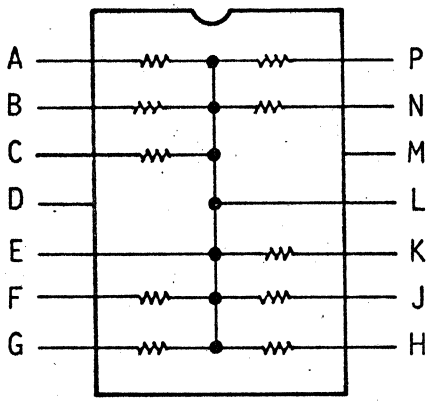
RP8N - PIN L CONNECTED TO -2.0V
RPWN - PIN L CONNECTED TO +4.75V
RPXN - PIN L CONNECTED TO GND

RPAN 1675 0754

200 OHM RESISTOR PACKAGE (10 RESISTORS)

1) Ten resistors are contained in a 14 pin dual-in-line package as shown below.

2) R = 200 ± 5% at 100 mw. maximum power.

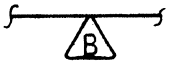


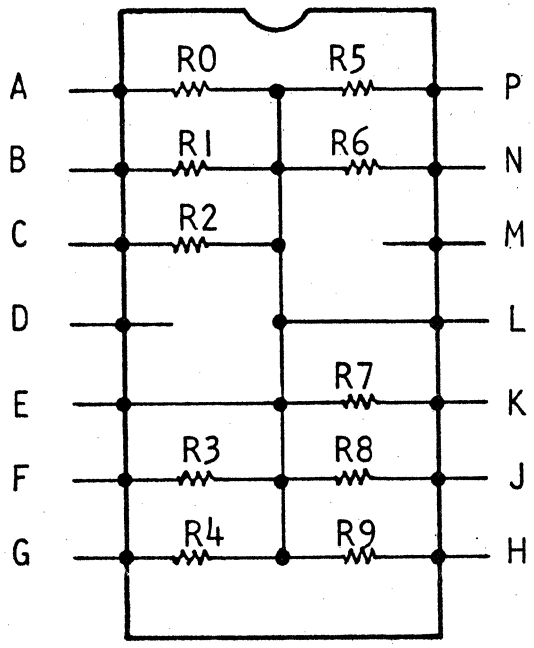
RPBN 1675 0556

1K RESISTOR PACKAGE (10 RESISTORS)

(1) Ten resistors are contained in a 14 pin dual-in-line package as shown below.

(2) R = 1000Ω± 50Ω at 150 mw. maximum power.



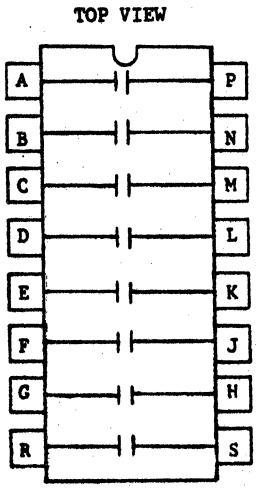


CP1N

Element Type	CP1N
Standard Assembly Number:	2208 4834
Manufacturer/Manufacturer's Type:	Corning Glass/D00049
Circuit Designation	Capacitor Network
Description of Operation:	

1. Capacitance: 200pf $\pm$ 10%
2. DC Voltage: 30V DC max.

Pin Locations:



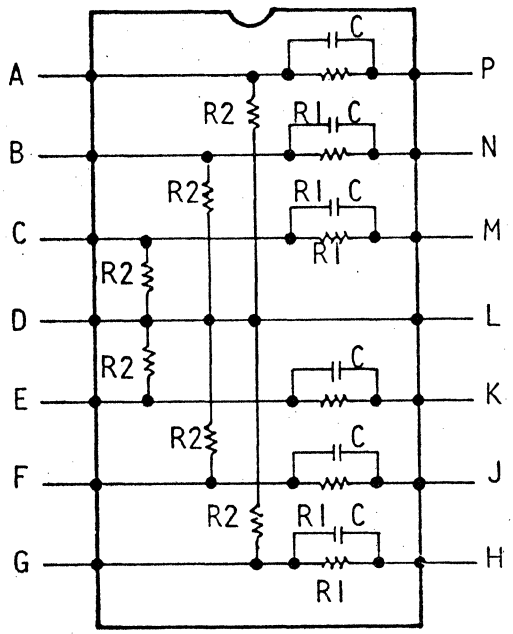
CP1N

RPCN 1675 0580

RESISTOR-CAPACITOR PACKAGE

(1) Twelve resistors and six capacitors are connected as shown below, and contained in a 14 pin DIP.

(2) R1 = 120Ω ± 6Ω at 100 mw maximum power.
R2 = 200Ω ± 10Ω at 100 mw maximum power.
C = 270 pf ± 54 pf, V (break down) > 50 volts.



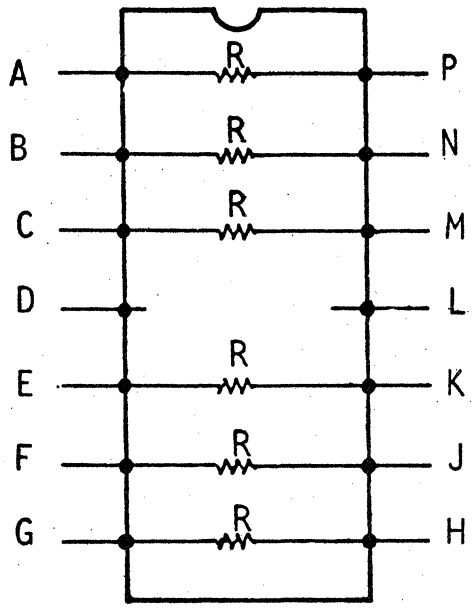
PIN
DIAGRAM

RPDN 1675 0572

25 OHM RESISTOR PACKAGE (6 RESISTORS)

(1) Six resistors are contained in a 14 pin dual-in-line package as shown below.

(2) R = 25 OHMS $\pm$ 5% at 200 mw maximum power.



PIN
DIAGRAM

RPEN

3.5 MISCELLANEOUS CIRCUITS (Continued)

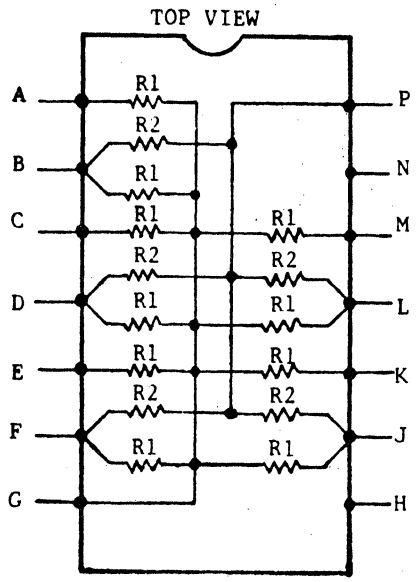
Element Type:	RPEN
Standard Assembly Number:	1677 1032
Circuit Designation:	Resistor Network
Description of Operation:	

(1) 15 resistors are contained in a 14 pin, Dual-In-Line package

(2) R1 = 100Ω ± 2%
R2 = 9KΩ ± 2%

(3) The maximum continuous power dissipation capability of each resistor in the network shall be .1 watt.

PIN LOCATIONS:



RPEN

IC VIDEO AMP

3.5 MISCELLANEOUS CIRCUITS (Continued)

Element Type:

Standard Assembly Number: 2200 8460

Circuit Designation: I.C. Video Amplifier

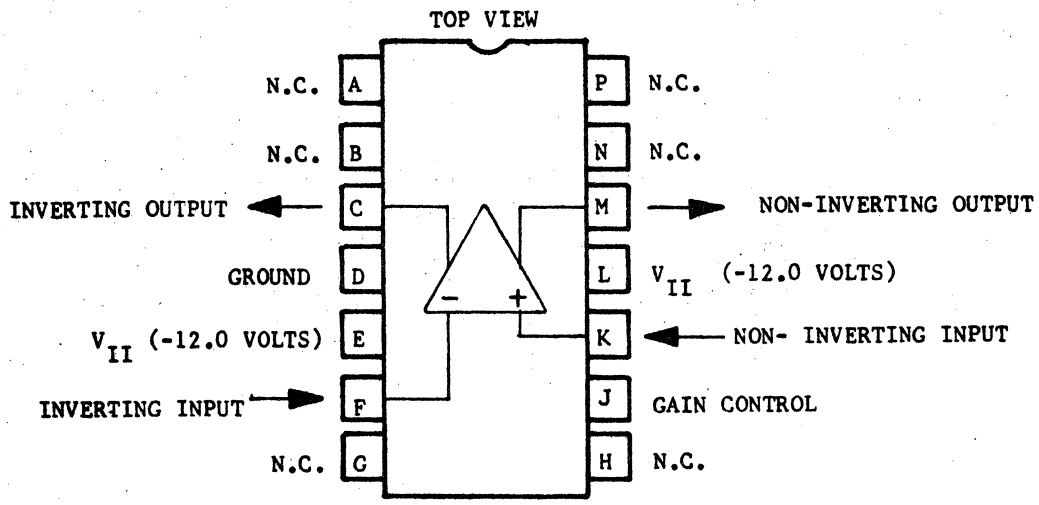
Description of Operation:

The 2200-8460 video amplifier is the feedback element that maintains oscillations of the crystal.

Features of this video amplifier are internal input biasing, open collector current source output and an internal design such that the output limits symmetrically for either a positive or negative input overdrive. Internal biasing is such that no internal element is saturated due to input overdrive. Output impedance is constant over any part of the operational cycle.

Consult the circuits and Packaging Section on use of this device.

PIN LOCATIONS:



RPFN

Element Type: RPFN
Standard Drawing Number: S-1918 3573
Circuit Designation: Resistor Network
Machine No.: 614

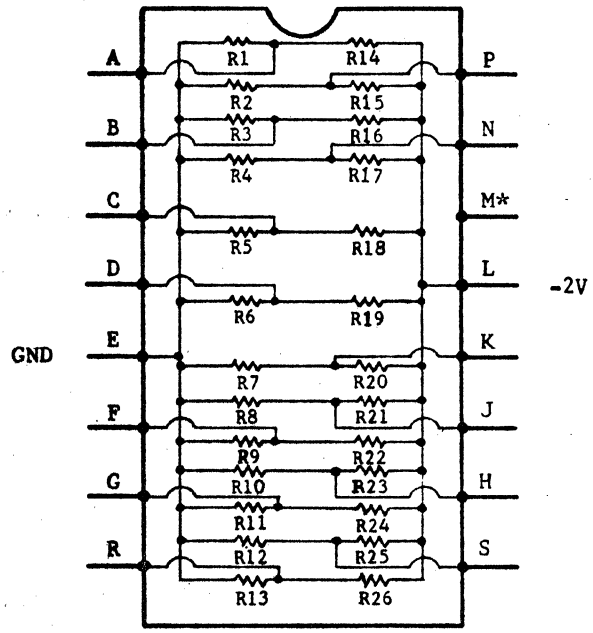
1. Power Rating:

   a. 60 milliwatt maximum per element
   b. 1.5 watt total per package

2. Resistance Value

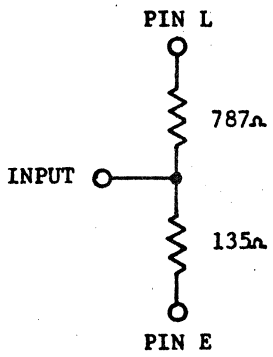
Machine Number	R1 THRU R13		R14 THRU R26	
	Value (Ohms)	Tol. %	Value (Ohms)	Tol. %
614	135	2	787	2

Pin Location Diagram



RPFN

There are 13 resistor networks each with the following configuration:



* Not internally connected (+4.75V acceptable)

JPRN

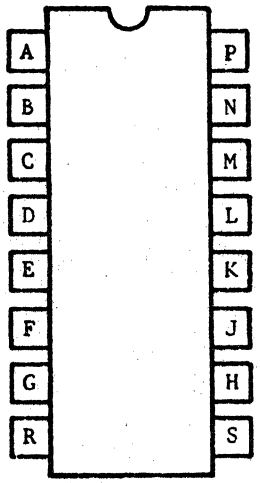
3.5 Miscellaneous Circuits (Continued)

Element Type: JPRN
Standard Assembly Number: None
Circuit Designation: Header - 16 Pin (not a chip)
Description of Operation:

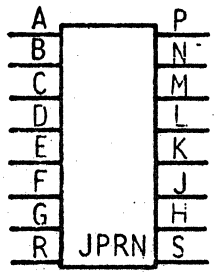
This device has no logic content. A blank 16 pin Socket Header (S-2201 4732) is used for the discretionary wiring (installed in the header) to make a JPRN function. Jumper wiring configurations are shown in a special Jumper Chip Instruction T & F document.

Pin Locations:

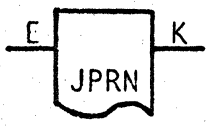
TOP VIEW



FUNCTIONAL DIAGRAM



OR MAY BE SHOWN
AS SINGLE JUMPERS



R6nn

3.5 Miscellaneous Circuits (continued)

Element Type: R6nn
Standard Assembly Number: S2212 2725 - 2212 2782
Circuit Designation: Single-in-line Resistor Package
Description of Operation:

The R6nn contains seven thick film resistors with one end in common in an eight pin, single-in-line package. Each resistor can dissipate .3 Watts. There are a number of values available.

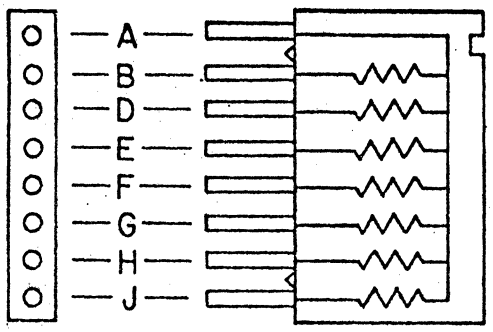
					Part Number	GND	SCHEMATIC SYMBOLS -2.0	+4.75
R6n0	contains	seven	330Ω	resistors	2212 2725	10	20	30
R6n1	"	"	220Ω	"	2212 2733	11	21	31
R6n2	"	"	100Ω	"	2212 2741	12	22	32
R6n3	"	"	150Ω	"	2212 2758	13	23	33
R6n4	"	"	470Ω	"	2212 2766	14	24	34
R6n5	"	"	680Ω	"	2212 2774	15	25	35
R6n6	"	"	1KΩ	"	2212 2782	16	26	36

R6nn ← Indicates value of resistors
R6nn ← Indicates usage where

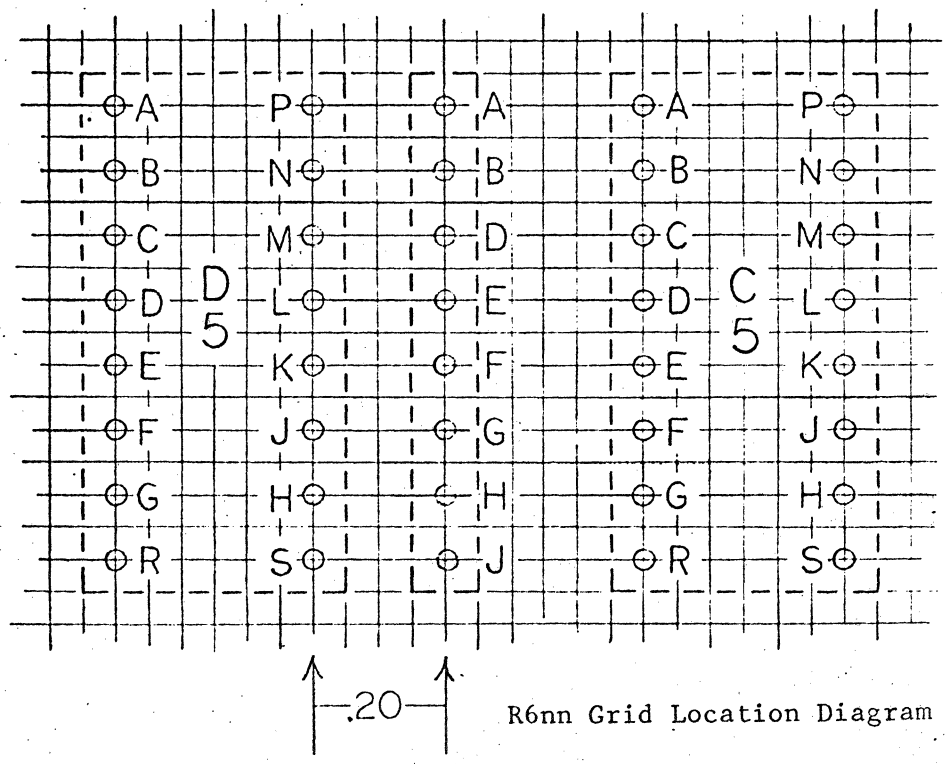
TO BE SHOWN INSIDE A TRIANGLE

R61n = Resistor to ground
R62n = Resistor to -2.0v
R63n = Resistor to +4.75v

Note: See section 12 page 9 for schematic representation.



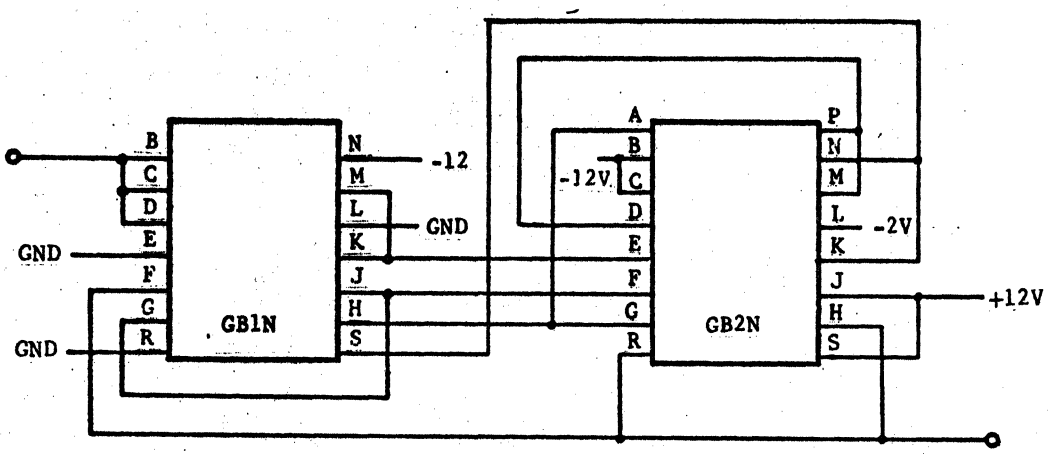
LOGIC DIAGRAM



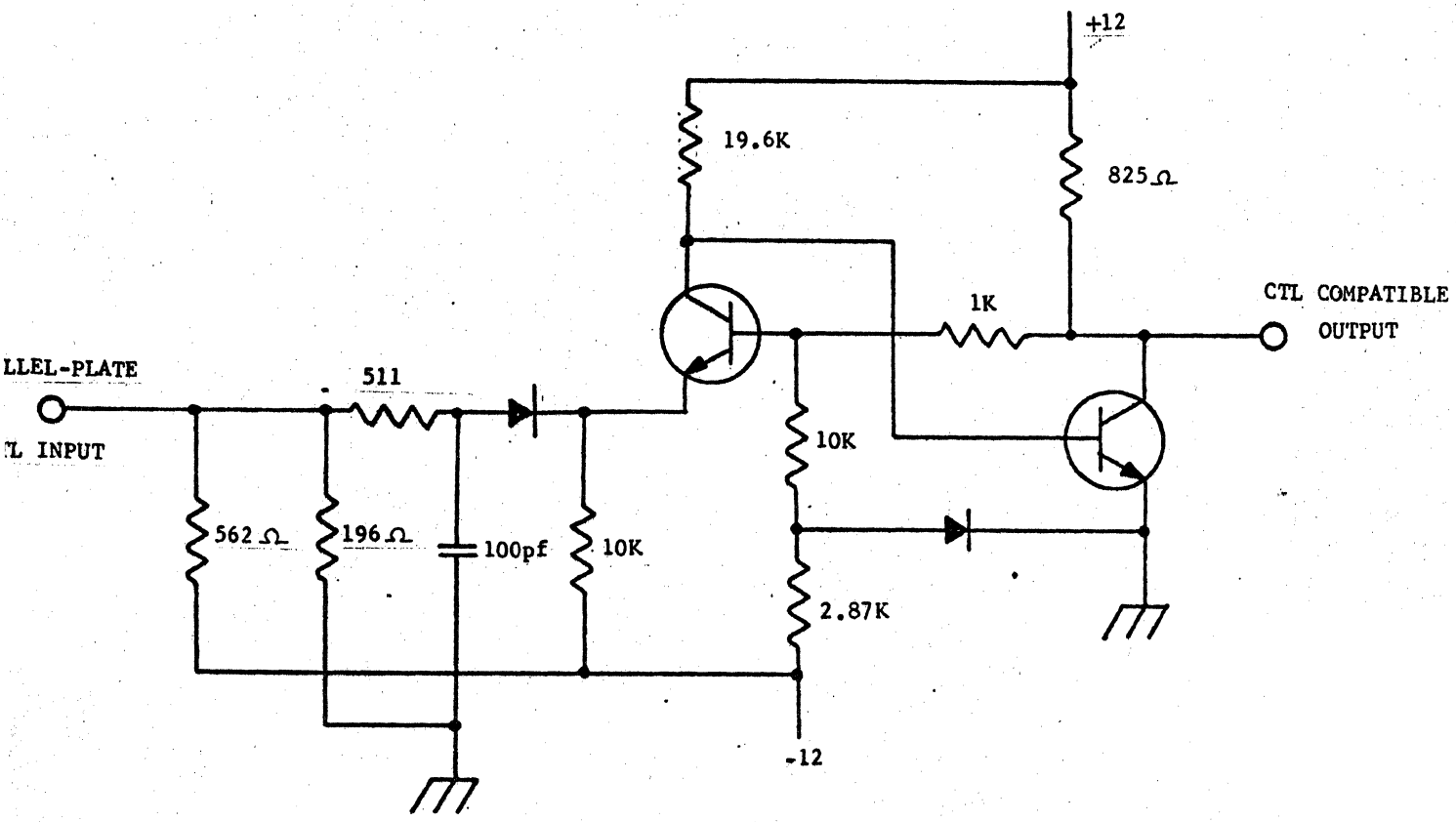
R6nn Grid Location Diagram

GB1N & GB2N

INTERCONNECTION SCHEMATICS



LOGIC INTERCONNECTS



SCHEMATIC

RPON

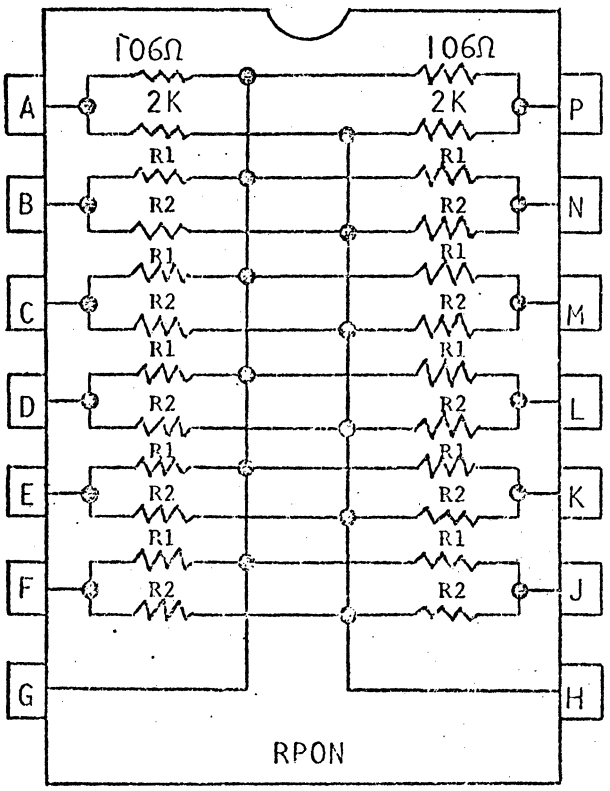
3.5 Miscellaneous Circuits

Element Type: RPON
Standard Assembly Number: 2540 0904
Circuit Designation: Resistor Network

Description of Operation:

1) The RPON contains 24 resistors in a 14 pin dual in line package as shown below.

2) R1 = 106 ohms ± 2% at 150mW per resistor
R2 = 2K ohms ± 2% at 100mW per resistor



PIN LOCATION DIAGRAM

RPSN

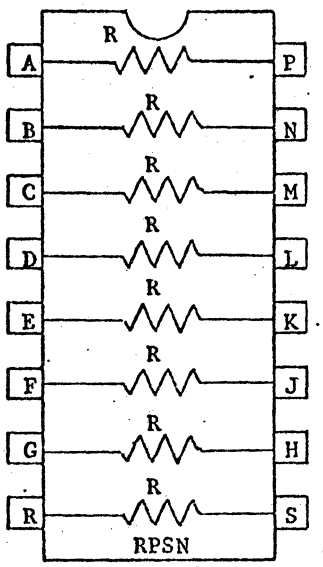
3.5 Miscellaneous Circuits

Element Type: RPSN
Standard Assembly Number: 2539 9965
Circuit Designation: Resistor Network

Description of Operation:

1) The RPSN contains eight 25Ω resistors in a single 16 pin dual in line package as shown below.

2) R = 25 ohms ± 10% at 120mW per resistor.



PIN LOCATION DIAGRAM

OSCC

3.5 Miscellaneous Circuits (continued)

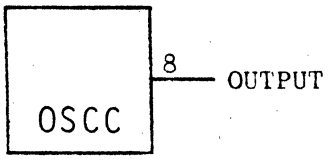
Element Type:	OSCC
Standard Assembly Number:	2314 2847
Manufacturer/Manufacturer's Type:	Motorola/K1091A
Circuit Designation:	12 MHz Crystal Clock Oscillator

Description of Operation:

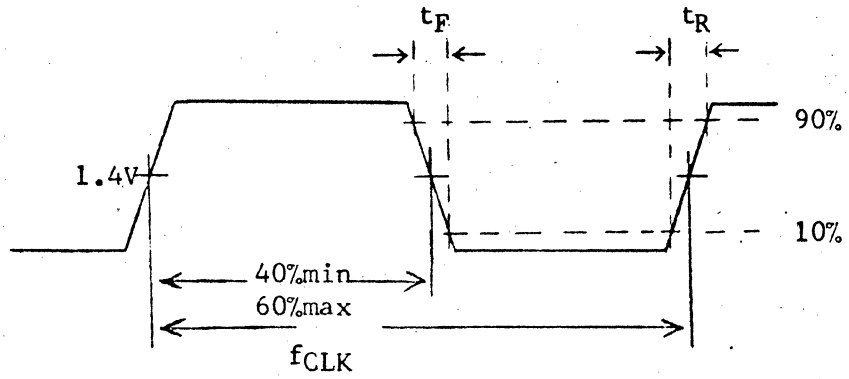
The crystal oscillator provides a 12 MHz square wave output accurate to ± 0.01%.

The OSCC is contained in a 14 pin DIP. The only input connections required are Vcc and Ground.

Output is TTL compatible with a worst case 60/40 duty cycle at the 1.4V level.



FUNCTIONAL DIAGRAM



OUTPUT WAVEFORM

OSCD

3.5 Miscellaneous Circuits (continued)

Element Type:	OSCD
Standard Assembly Number:	2212 2592
Manufacturer/Manufacturer's Type:	Motorola/K1100A
Circuit Designation:	307.2 KHz Crystal Clock Oscillator

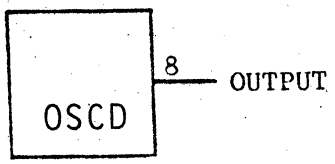
Description of Operation:

The crystal oscillator provides a 307.2 KHz square wave output accurate to ± 0.01%.

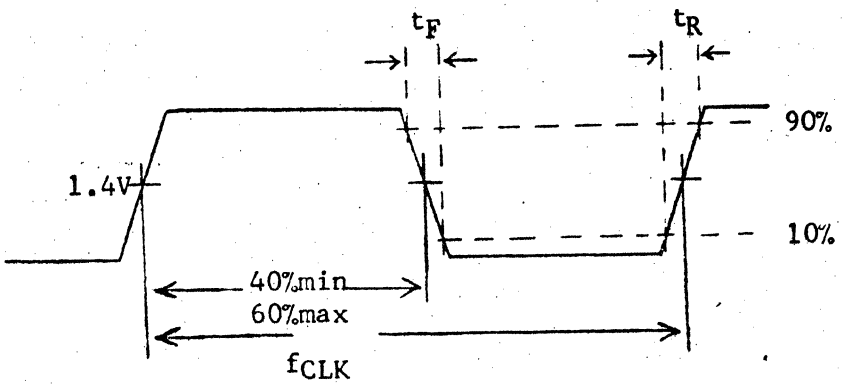
The OSCD is contained in a hermatically sealed package having 4 pins with dual-in-line spacing. The only input connections required are Vcc and Ground.

Output is TTL compatible with a worst case 60/40 duty cycle at the 1.4V level. Output waveform rise and fall times are 15 ns max.

Output drive capability:
Iol = 16 mA @ Vol=0.4V Ioh = -400 uA @ Voh=2.4V



FUNCTIONAL DIAGRAM



OUTPUT WAVEFORM

4.0 DEVICE SUMMARY

Summaries of the input and output loading and the propagation delay times for the CTL, TTL/DTL, and interface circuits are given in the following Tables:

CTL Devices	Table 4-1
TTL/DTL Devices	Table 4-2
Interface Devices	Table 4-3

TABLE 4-1 CTL SUMMARY

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT LOADING L	INPUT LOADING H	OUTPUT DESIGNATIONS	OUTPUT DRIVE PIN	OUTPUT DRIVE PKG	OUTPUT LOADING	AC PARAMETERS	VALUE (ns)
AFAn	Dual Adder/Subtractor	A0 B0 C0 M0 A1 B1 C1	0.8	0.8	S0 G0 P0 S1 G1 P1	12	72	0	Input to Output	22 Max.
AMCn	8 Bit Memory	I0 I1	0	1.5	Q0 Q1	3.5	7	0	Read Access Time	27 Max.
		R0 R1 R2 R3	0	1.5					Data Set-up Time	17 Max.
		W0 W1 W2 W3	0	2.5					Minimum Write Pulse Width	27
BG-N	Dual Buffer (2,2)		0.8	0.8		24	48	0	Input to Output	10 Max.
BHAn	Hex Restorer		0.8	0.8		12	48	0	Input to Output	12 Max.
CFAn	4 Bit Comparator	A0 A1 A2 A3 A4 B0 B1 B2 B3 B4	0.8	0.8	AL AE AG	12	36	0	Input to Output	28 Max.
CFBn	Carry Logic Gate	P0 P1 P2 P3 G0 G1 G2 G3 C1	1	1	C0 C1 C2 C3	12	48	0	Input to Output	6 Max.
DFAn	1 of 8 Decoder	A0 A1 A2 E0 $\overline{E1}$	0.8	0.8	Z0 Z1 Z2 Z3 Z4 Z5 Z6 Z7	12	96	0	Address to Output Enable to Output	12 Max. 12 Max.
EFAn	Priority Encoder	I0 I1 I2 I3 $\overline{I4}$ I5 I6 I7 $\overline{E0}$	0.8	0.8	Z0 Z1 Z2 AI	12	24	0	Input to Address Output Input to AI Output Inhibit to Output	16 Max. 16 Max. 16 Max.
FFAn	Dual JK/D Flip Flop	J0 K0 D0 J1 K1 D1 M0 M1	0.8	0.8	Q0 $\overline{Q0}$ Q1 $\overline{Q1}$	12	48	0	Clock (-) to Output Data Set Up Time JK to D Mode Set Up Time D to JK Mode Set Up Time Minimum Clock Pulse Width	17 Max. 10 Max. 10 Max. 10 Max. 17
GFBn	Dual AND Gates (4,4)		1	1		12	24	1	Input to Output	6 Max.
GFEn	Quad Gates (1,1,1,1)		1	1		12	48	1	Input to Output	6 Max.
GFFn	Quad AND, AND/OR Gates (2,2,2+2)		1	1		12	36	1	Input to Output	6 Max.
GFIn	Triple AND Gates (4,3,3)		1	1		12	36	1	Input to Output	6 Max.
GFJn	Quad AND Gates (3,2,2,2)		1	1		12	48	1	Input to Output	6 Max.
GFKn	Quad AND Gates (3,2,2,2)		0	0		12	48	0	Input to Output	6 Max.
IF-n	Dual Inverter (2,2)		0.8	0.8		24	48	1	Input to Output (FO=12) Input to Output (FO=24)	12 Max. 15 Max.

TABLE 4-1 CTL SUMMARY (continued)

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT LOADING L	INPUT LOADING H	OUTPUT DESIGNATIONS	OUTPUT DRIVE PIN	OUTPUT DRIVE PKG	OUTPUT LOADING	AC PARAMETERS	VALUE (ns)
IHAn	Hex Inverter		0.8	0.8		12	48	0	Input to Output	12 Max.
LFAn	Quad Latch	I0 I1 I2 I3 M0 M1 P0 P1 E0	0.8	0.8	Q0 Q1 Q2 Q3	12	48	0	Data to Output Mode Controls to Output Clock (+) to Output Read Enable to Output Data & Mode Set Up Time Minimum Clock Pulse Width	22 Max. 22 Max. 22 Max. 12 Max. 12 Max. 17
MFAn	8 Input Multiplexer	I0 I1 I2 I3 I4 I5 I6 I7 A0 A1 A2 E0	0.8	0.8	Z0	12	12	0	Data to Output Address to Output Enable to Output	16 Max. 20 Max. 16 Max.
MOPn	Micro-operator	I0 I1 I2 I3	0	0	Y0 Y1 Y2 Y3 Z0 Z1 Z2 Z3 Z4	12	60	0	Input to Output	14 Max.
RFAn, RFZN	3 Bit Register	I0 I1 I2 CI M0 M1 M2 P0 R0 C0	0.4	0.8	Q0 Q1 Q2 CI C0	12 8 8	52	0 0.4/0.8 0	Clock (-) to C0 Clock (-) to Output Clock (-) to CI Carry In to Carry Out Mode Control to C0 Data Set Up Time (+ & -) Data Set Up Time (other) Clear Set Up Time Mode Control Set Up Time Data, Mode, and Clear Hold Time Minimum Clock Pulse Width	39 Max. 21 Max. 39 Max. 24 Max. 38 Max. 24 Max. 11 Max. 17 Max. 28 Max. 6 Max. 17
RFBn, RF-N	4 Bit Register	I0 I1 I2 I3 M0 M1 M2 P0 R0	0.4	0.8	Q0 Q1 Q2 Q3	12	48	0	Clock (-) to Output Data Set Up Time Clear Set Up Time Mode Control Set Up Time Data, Mode, and Clear Hold Time Minimum Clock Pulse Width	21 Max. 6 Max. 19 Max. 28 Max. 7 Max. 20

NOTE: Propagation delays for a logic string of non-restoring gate elements should be calculated by using a Root Sum Square (RSS) law.

Example: two 6 ns gates and one 7 ns gate in series
Total Time Delay = SQRT $(6^2 + 6^2 + 7^2) = 11.0$ ns

All other propagation delay times are additive.

TABLE 4-2 TTL/DTL SUMMARY

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT CURRENTS @ Vi = LOAD	INPUT CURRENTS @ Vi = LEAK	OUTPUT DESIGNATIONS	TYPE	OUTPUT "LOW" CURRENT	OUTPUT HIGH OR LEAKAGE CURRENT	AC PARAMETERS	VALUE (ns)
MI1N	EBCDIC/ASCII (MSB) Code Converter	A0 A1 A2 A3 A4 A5 A6 A7 $\overline{C1}$ $\overline{C2}$	-1.6 mA 0.45V	.04 mA 4.5V	01 02 03 04	OC	15 mA @ V_O=0.45V	L 0.1mA @ V_O=5.25V	Address to Output Enable to Output	60 Max. 40 Max.
MI2N	EBCDIC/ASCII (LSB) Code Converter									
MI3N	ASCII/EBCDIC (MSB) Code Converter									
MI4N	ASCII/EBCDIC (LSB) Code Converter									
MH1N	HOLLERITH/EBCDIC (LSB) Code Converter									
MH2N	HOLLERITH/EBCDIC (MSB) Code Converter									
MH3N	EBCDIC/HOLLERITH (LSB) Code Converter									
MH4N	EBCDIC/HOLLERITH (MSB) Code Converter									
MJ1N	96 COL/EBCDIC (LSB) Code Converter									
MJ2N	96 COL/EBCDIC (MSB) Code Converter									
MJ3N	EBCDIC/96 COL (LSB) Code Converter									
MJ4N	EBCDIC/96 COL (MSB) Code Converter									
MK1N	EBCDIC/BLC+PAR (LSB) Code Converter									
MK2N	EBCDIC/BCL+PAR (MSB) Code Converter									
RM1N	EBCDIC/KATAKANA (LSB) Code Converter									
RM2N	EBCDIC/KATAKANA (MSB) Code Converter									

TABLE 4-2 TTL/DTL SUMMARY (continued)

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT CURRENTS @ Vi = LOAD	INPUT CURRENTS @ Vi = LEAK	OUTPUT DESIGNATIONS	TYPE	OUTPUT "LOW" CURRENT	OUTPUT HIGH OR LEAKAGE CURRENT	AC PARAMETERS	VALUE (ns)
MF4N	EBCDIC/BCL 1/4 Code Converter	A0 A1 $\overline{A2}$ A3 A4 $\overline{EO}$	-1.6mA +0.40V	0.10mA 4.5V	01 02 03 04 05 06 07 08	OC	10 mA @ V_o=0.40V	L -.2mA @ V_o=5.5V	Address to Output Enable to Output	50 Max. 50 Max.
MF5N	EBCDIC/BCL 2/4 Code Converter	↓	↓	↓	↓	↓	↓	↓	↓	↓
MF6N	EBCDIC/BCL 3/4 Code Converter									
MF7N	EBCDIC/BCL 4/4 Code Converter									
MF8N	BCL/EBCDIC 1/2 Code Converter									
MF9N	BCL/EBCDIC 2/2 Code Converter									
RFCn	64 Bit Memory	I0 I1 I2 I3 $\overline{A0}$ A1 A2 A3 $\overline{CS}$ $\overline{WE}$	-1.2mA +0.45V	0.06mA 4.5V	Q1 Q2 Q3 Q4	OC	15 mA @ V_o=0.45V	L 0.1mA @ V_o=5.25V	Address to Output Enable to Output Minimum Write Enable Pulse Width Recovery Time After Write Enable	45 Max. 27 Max. 30 45 Max.
RFDn	256 Bit Memory	A0 A1 A2 A3 $\overline{A4}$ $\overline{A5}$ $\overline{A6}$ $\overline{A7}$ $\overline{CS0}$ $\overline{CS1}$ $\overline{CS2}$ DI $\overline{WE}$	-0.26mA +0.45V	0.01mA 5.25V	DO	OC	15 mA @ V_o=0.45V	L 0.1mA @ V_o=5.25V	Address to Output Enable to Output Minimum Write Enable Pulse Width Recovery Time After Write Enable	70 Max. 55 Max. 55 70 Max.
RW06	1024 Bit Memory	A0 A1 A2 A3 A4 A5 A6 A7 $\overline{A8}$ A9 DI $\overline{WE}$ $\overline{CS}$	-0.4mA +0.40V	0.02mA 4.5V	DO	OC	16 mA @ V_o=0.40V	L 50μA @ V_o=4.5V	Address to Output Enable to Output Minimum Write Enable Pulse Width Recovery Time After Write Enable	70 Max. 55 Max. 55 70 Max.
IHDN	Hex Inverter	01 21 31 41 51 11	-1.6mA +0.45V	0.10mA 4.5V	OB 1D 2F 3M 4K 5H	OC	40 mA @ V_o=0.7V	L .25mA @ V_o=30V	Input to Output t_{d-+} t_{d+-}	23 Max. 15 Max.
IHCN	Hex Inverter (DTL)	01 11 21 31 41 51	-1.5mA +1.1V	5μA 1.9V	OB 1D 2F 3H 4K 5M	Actv	V_o=0.6V	H 10mA @ V_o=2.6V	Input to Output t_{d-+} t_{d+-}	50 Max. 35 Max.

TABLE 4-2 TTL/DTL SUMMARY (CONTINUED)

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT CURRENTS @ Vi = LOAD	LEAK	OUTPUT DESIGNATIONS	TYPE	OUTPUT "LOW" CURRENT	OUTPUT HIGH OR LEAKAGE CURRENT	AC PARAMETERS	VALUE (ns)
TAOn	Re-triggerable Monostable Multivibrator	I0 I1 I2 I3	-1.6mA +0.45V	0.06mA 4.5V	QT QF	TP	9.1 mA @ V_o=0.45V	H -6.7mA V_o=1.6V -0.72mA V_o=2.4V	Negative Trigger In to True Out Negative Trigger In to Comp. Out Minimum Input Pulse Width Minimum True Output Pulse Width	50 Max. 50 Max. 40 65
DFBN	Seven Segment Decoder	A0 A1 A2 A3 RBI LT	-1.5mA -0.75mA -6.4mA +0.45V	5μA 5μA 25μA 4.5V	ZA ZB ZC ZD ZE ZF ZG RBO	Actv	10 mA @ V_o=0.45V 2.4mA @ V_o=-.45V	H 0mA @ V_o=4.3V H -70μA V_o=2.7V	Input to Output	550 Max.
IDCN	Dual Expandable Nand Gate	01 02 03 04 05 11 12 13 14 15	-1.5mA +0.40V	5μA 4.0V	OF IH	OC	36 mA @ V_o=0.40V	L 200μA @ V_o=4.5V	Input to Output t_{d-+} t_{d+-}	55 Max. 35 Max.
S2-N	Quad 2- Input Multiplexer	IaO Ia1 IbO Ib1 IcO Ic1 IdO Id1 A $\overline{E}$	-1.6mA +0.40V	40μA 2.4V	ZO Z1 Z2 Z3	TP	16 mA @ V_o=0.40V	H -.8mA @ V_o=2.4V	Data to Output t_{d-+} t_{d+-} Enable to Output t_{d-+} t_{d+-} Select to Output t_{d-+} t_{d+-}	25 Max. 18 30 25 35 30
POO1	256x4 PROM	AO A1 A2 A3 A4 A5 A6 A7 CE1 CE2	-1.6mA 0.4V	-.06mA 2.4V	QO Q1 Q2 Q3	OC	16 mA @ V_o = 0.45V	L .02 mA @ V_o = 2.4V	Address Access Enable to Out	70 Max. 40 Max.
POO2	32x8 PROM	AO $\overline{A1}$ A2 A3 A4 $\overline{CE}$	-0.4 mA 0.45V	-0.04mA 2.4V	QO Q1 Q2 Q3 Q4 Q5 Q6 Q7	OC	16 mA @ V_o = 0.45V	L .02 mA @ V_o = 2.4V	Address Access Enable to Output	55 Max. 35 Max.
PR4N	256x4 PROM	AO A1 A2 A3 A4 A5 A6 A7 CS1 CS2	-.4 mA 0.4V	0.04 mA 2.4V	QO Q1 Q2 Q3	OC	16 mA @ V_o = 0.45V	L 0.1 mA @ V_o = 2.4V	Address Access Enable to Output	40 Max. 25 Max.
PR5N	512x4 PROM	AO A1 A2 A3 A4 A5 A6 A7 A8 CS	-.4 mA 0.45V	0.04 mA 2.4V	QO Q1 Q2 Q3	OC	16 mA @ V_o = 0.45V	L 0.1 mA @ V_o = 2.4V	Address Access Enable to Output	60 Max. 35 Max.
S4-N	Dual 4-Bit Data Selector	EA EB AO A1 IAO IA1 IA2 IA3 IBO IB1 IB2 IB3	-1.6 mA 0.4V	0.04 mA 2.4V	ZA ZB	TP	16 mA @ V_o = 0.4V	H .04 mA V_o = 2.4V	Data to Output t_{pd+} t_{pd-} Address to Output t_{pd+} t_{pd-} Enable to Output t_{pd+} t_{pd-}	25 Max. 27 Max. 41 Max. 38 Max. 37 Max. 27 Max.

TABLE 4-2 TTL/DTL SUMMARY (Continued)

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT CURRENTS @ Vi = LOAD	INPUT CURRENTS @ Vi = LEAK	OUTPUT DESIGNATIONS	TYPE	OUTPUT "LOW" CURRENT	OUTPUT HIGH OR LEAKAGE CURRENT	AC PARAMETERS	VALUE (ns)
T3AH	Triple 3 Input AND Gate		-2 mA 0.4V	0.04 mA 2.4V		TP	20 mA @ V_o = 0.4V	H 2 mA V_o = 2.4V	Input to Output tpd+	19 Max.
									tpd-	16 Max.
T2HN	Quad 2-Input NAND Gate		-2 mA 0.4V	0.04 mA 2.4V		TP	20 mA V_o = 0.4V	H 2 mA V_o = 2.4V	Input to Output tpd+	17 Max.
									tpd-	14 Max.
BTSN	Tri-State Hex Buffer	I0 I1 I2 I3 I4 I5 DIS4 DIS2	-1.6 mA 0.4V (norm.) .4 mA	0.04 mA 2.4V	O0 O1 O2 O3 O4 O5	TS	38 mA @ Vo = 0.4V (norm.) .4 mA	H 2.5 mA Vo = 2.4V (norm.) .04 mA	Data In to Output tpd+	23 Max.
									tpd-	26 Max.
									High Impedance tpZH	40 Max.
									tpZL	45 Max.
		I0-I5 Only	0.5 V (high)				Vo = 0.4V (high)	Vo = 2.4V (high)	tpHZ	25 Max.
									tpLZ	33 Max.
CR4N	4 Bit Binary Counter	Clear, Data Enable P	-1.6 mA 0.4V	.04 mA 2.4V	Q0 Q1 Q2 Q3	TP	12 mA @ Vo = 0.4V	H 6 mA Vo = 2.4V	Clock to Output (load low) tpd+	33 Max.
									tpd-	37 Max.
		Clock, Load Enable T	-3.2 mA 0.4V	.06 mA 2.4V	C		16 mA @ Vo = 0.4V	8 mA Vo = 2.4V	Clock to Output (load high) tpd+	28 Max.
									tpd-	31 Max.
									Clock to Carry tpd+	44 Max.
									tpd-	43 Max.
									Enable T to Carry tpd+	23 Max.
									tpd-	23 Max.
									Clear to Output tpd-	46 Max.
									Clear Recovery Time	28 Max.
									Clear Pulse Width	24 Min.
									Clock Pulse Width	30 Min.
									Enable P and Data Set-up Time	22 Max.
									Load Set-up Time	28 Max.
									Hold Time Any Input	0
RW13	1024 Bit RAM	A0 A1 A2 A3 A4 A5 A6 $\overline{A7}$ A8 A9 DI $\overline{WE}$ $\overline{CS}$	-0.4 mA 0.4V	.02 mA 4.5V	DO	OC	16 mA @ Vo = 0.4V	L 50μA Vo = 4.5V	Address to Output	50 Max.
									Enable to Output	35 Max.
									Min. WE Pulse Width	40
									Recovery Time after Write Enable	70 Max.

TABLE 4-2 TTL/DTL SUMMARY (CONTINUED)

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT CURRENTS @ Vi = LOAD	LEAK	OUTPUT DESIGNATIONS	TYPE	OUTPUT CURRENTS LOW @ Vo=	HIGH OR LEAKAGE @ Vo=	AC PARAMETERS		VALUE
B2CN	Quad 2-Input NAND Buffer	A0 B0 A1 B1 A2 B2 A3 B3	-1.6 mA 0.4 V	40µA 2.4V	Z0 Z1 Z2 Z3	OC	48 mA Vo = 0.4V	L 250µA Vo = 2.4V	-Input to Output	td-+ tdt-	27 21
B2TS	Quad Tri-State Buffer	I0 D0 I1 D1 I2 D2 I3 D3	-1.6 mA 0.4 V	40µA 2.4V	Z0 Z1 Z2 Z3	TS	16 mA Vo = 0.4V (norm.) -40µA Vo = 0.4V (hi Z)	H -2 mA Vo = 2.4V (norm) 40µA VO = 2.4V (hi Z)	-Data Input to Output -Disable Input to Output	td+ td- tZH tZL tHZ tLZ	20 22 25 29 23 22
TTSN	Tri-State Hex Inverter	I0 I1 I2 I3 I4 I5 D152 D154 I0 - I5 only	-1.6 mA 0.4V (norm) -40µA 0.5V (hi Z)	40µA 2.4V 40µA 2.4V	Z0 Z1 Z2 Z3 Z4 Z5	TS	32 mA Vo = 0.4V (norm) -40µA Vo = 0.4V (hi Z)	H -2.5 mA Vo = 2.4V (norm) 40µA Vo = 2.4V (hi Z)	-Data Input to Output -Disable Input to Output	td-+ tdt- tZH tZL tHZ tLZ	21 20 39 41 15 31
CRC1	CRC Generator/ Checker	D SO S1_S2 CP CWE P MR	-0.25 mA 0.4V	4.µA 2.4V	Q ER	TP	4 mA Vo = 0.4V	H -400µA Vo = 2.4V	-Clock pulse width, -Reset or preset width -Clock to Data output -Clock to Error output -Preset to Output -Reset to Output -Set up time, Data or CWE to clock -Hold time, Data or CWE to Clock -Recovery time, reset or preset to clock	tw(L) td-- td-+ td-- td-+ td-+ td+-	35 Min. 35 Min. 55 Max. 55 Max. 60 Max. 60 Max. 60 Max. 60 Max. 55 Min. 55 Min. 45 Min.

TABLE 4-2 TTL/DTL SUMMARY (CONTINUED)

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT CURRENTS @ Vi = LOAD	INPUT CURRENTS @ Vi = LEAK	OUTPUT DESIGNATIONS	TYPE	OUTPUT CURRENTS LOW @ Vo=	OUTPUT CURRENTS HIGH OR LEAKAGE @ Vo=	AC PARAMETERS	VALUE
SCTL	System Controller	DO D1 D3 D4 D5 D7	-250μA 0.4V	100μA 2.4V	DO D1 D2 D3 D4 D5 D6 D7	TS	2 mA Vo = 0.45V (norm)	H -10μA Vo = 3.6V	-$\overline{\text{STSTB}}$ pulse width tpW	25 Min.
									-$\overline{\text{STSTB}}$ to CPU Data Bus	
									Set up time tss	10 Min.
									Hold time tsH	20 Min.
		D2 D6	-750uA 0.4V	100uA 2.4V	DBO DB1 DB2 DB3 DB4 DB5 DB6 DB7	TS				
							10mA Vo = 0.45V (norm)	H -1mA Vo = 2.4V (norm)	-System Data Bus to $\overline{\text{HLDA}}$	
		DB0 DB1 SB2 DB3 DB4 DB5 DB6 DB7	-250uA 0.4V	20uA 2.4V	$\overline{\text{MEMR}}$ $\overline{\text{MEMW}}$ $\overline{\text{IOR}}$ $\overline{\text{IOW}}$	TS			Set up time tDS	10 Min.
									Hold time tDH	20 Min.
		$\overline{\text{STSTB}}$	-500uA 0.4V	100uA 2.4V	$\overline{\text{INTA}}$				-$\overline{\text{STSTB}}$ to Control Outputs tDC	60 Max.
		DBIN HLDA	-250uA 0.4V	100uA 2.4V			-100uA Vo = 0.45V (Hi Z all outputs)	100uA Vo = 5V (Hi Z all outputs)	-DBIN to Control Outputs tRR	35 Max.
		$\overline{\text{WR}}$ $\overline{\text{BUSEN}}$	-250uA 0.4V	100uA 2.4V					-$\overline{\text{WR}}$ to Control Outputs tWR	45 Max.
									-DBIN to CPU Data Bus tRE	60 Max.
									-System Data Bus to CPU Data Bus during Read tRD	45 Max.
									Write tWD	45 Max.
									-$\overline{\text{STSTB}}$ to System Data Bus tTE	45 Max.
									-$\overline{\text{BUSEN}}$ to System Data Bus tE	35 Max.
									-HLDA to Control Outputs tHD	30 Max.

TABLE 4-3 INTERFACE CIRCUITS SUMMARY

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATIONS	INPUT CURRENTS @ Vi = LOW	INPUT CURRENTS @ Vi = HIGH	OUTPUT DESIGNATIONS	OUTPUT CURRENTS LOW	OUTPUT CURRENTS HIGH	AC PARAMETERS	VALUE (ns)
LDAN	Dual IBM Interface Line Driver	OA OB OC OD OE OF 1A 1B 1C 1D 1E 1F	-1.6 mA 0.40 V	.04 mA 4.5 V	OY 1Y	-0.24 mA V_o=0.15V	59.3 mA V_o=3.11V	Input to Output tpd+ @ Z_L=50Ω & tpd- 100pf to gnd	25 Max. 35 Max.
LDPN	Dual Interface Line Driver	A0 A1 B0 B1	-1.6 mA 0.40 V	1.0 mA 5.5V			100 mA Max.	Input to Output tpd+ tpd-	65 Max. 35 Max.
LRFN	Dual Interface Line Receiver	A0 B0 C0 A1 B1 C1			Z0 Z1	15 mA V_o=0.45V	-5 mA V_o=2.4V	Input to Output Z_L=3.9K & 30pf tpd+ Z_L=390 & 30 pf tpd-	75 Max. 75 Max.
		SO S1	-2.4 mA 0.45V	5 uA 4.5V					
LDGN	Quad EIA Line Driver	A0 A1 A2 A3 B1 B2 B3	1.3 mA 0V	.01 mA 5.0V	Z0 Z1 Z2 Z3	V_{OH}=+6V & V_{OL}=-6V with R_L equal to 3K ohms		Input to Output tpd+ tpd- @ Z_L=3K & 15 pf	250 Max. 30 Max.

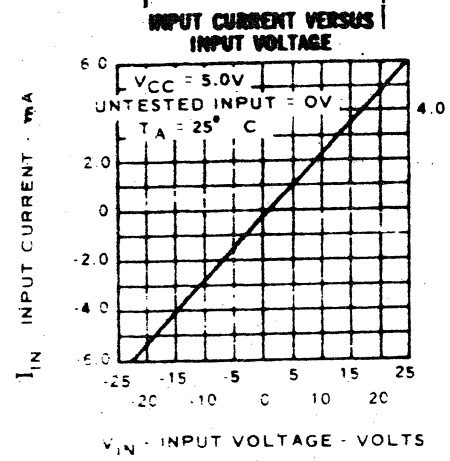


TABLE 4-3 INTERFACE CIRCUITS SUMMARY (CONTINUED)

TYPE	DEVICE DESCRIPTION	INPUT DESIGNATION	INPUT CURRENTS @ Vi = LOW	INPUT CURRENTS @ Vi = HIGH	OUTPUT DESIGNATION	OUTPUT CURRENTS LOW	OUTPUT CURRENTS HIGH	AC PARAMETERS	VALUE (ns)
LRGN	Quad EIA Line Receiver	AO A1 A2 A3	-8.3 to -3.6 mA @ -25V -.43 mA @ -3.0V	8.3 to 3.6 mA@ 25V .43 mA@ 3.0V	ZO Z1 Z2 Z3	10 mA 0.45V	-5.0 mA 2.6 to 5.0V	Input to Output R_L=390 ohms tpd+ R_L=3.9K ohms tpd-	60 Max. 100 Max.
SAMN	Dual Sense Amplifier	AO A1 BO B1	0.075 mA 0V		ZO Z1	16 mA 0.40V	-.4 mA 2.4V	Amplifier Delay tpd++ @Z_L=288 ohms & 15pf tpd--	40 Max. 60 Max.
		SO S1	-1.6 mA 0.4V	1 mA 5.25V				Strobe Delay tpd++ @Z_L=288 ohms & 15pf tpd--	30 Max. 50 Max.
SBMN	Dual Comparator/ Sense Amplifier	AO A1 BO B1	-.01 mA -25mV Vic=-2V	.075 mA 25mV Vic=+2V	ZO Z1	V_{OL}=.4V R_L=330 to Vcc	V_{OH}=4.5V R_L=1K to Vcc	Amplifier Delay tpd++ @Z_L=470 & 15pf tpd--	35 Max. 20 Max.
		SO S1	-1.6 mA 0V	.04 mA 2.4V				Gate Delay tpd+- @ Z_L=470 & 15pf tpd-+	17 Max. 17 Max.
		SC	-3.2 mA 0V	.08 mA 2.4V					
IQAN	Quad MOS Driver		1.5 mA 0.60V	8.0 mA 1.0V		V_{SS}=-4V V_{DD}=+2V Io=+60mA		Input to Output @V_{SS}=21V V_{DD}= 0V & C_L=250pf	45 Max.
DVCN	Differential Compa.	BS	-4.0 mA 0.40V		YO	8 mA 0.40V	50 mA 1.5V	Input to Output tpd+ tpd-	150 215
LDDN	Dual Line Driver	A1 B1 C1 A2 B2 C2	-3.0 mA 0.40V	.04 mA 2.4V	Y1 Z1 Y2 Z2	6.5 mA 0.40V	.1 mA 5.0V	Input to Output td Inhibit to Output td @ Z_L=50 ohms & 40 pf	20 Max. 30 Max.
		D	-6.0 mA 0.40V	.08 mA 2.4V					
IQBN	Quad MOS Driver	DA1 DA2 DB1 DB2 E11 E21 E2 E22	-.25mA 0.45V -.5 mA 0.45V	.01 mA 5.0V .02 mA 5.0V	OA1 OA2 OB1 OB2	100 mA 4.0V	-100 mA 15V	Input to Output tpd+ tpd- @ C_L= 200 pf	24 Max. 34 Max.
T1BR	Hex Bus Receiver With Hysteresis	I1 I2 I3 I4 I5 I6 DA DB	10uA 0.4V -3.2mA 0.4V	50uA 2.4V 50uA 2.4V	Q1 Q2 Q3 Q4 Q5 Q6	16mA 0.4V	-400uA 2.4V	Receiver Input to Output td-+ tdt- Disable Input to Output td-+ tdt-	40 Max. 34 Max 15 Max. 15 Max.
S140	Dual 4-Input		4 mA 0.5V	0.08 mA 2.4V		60 mA @ V_o= 0.5V	40 mA @ V_o= 2.1V	Input to Outout tpd+ tpd-	13 Max 13 Max

NUMERICAL

STANDARD ASSEMBLY	MACH NO	DA DESC	DESCRIPTION	LOGIC FAM	ELECTRICAL SPEC (REV)	DOC CONT
1123 9050 C	105	IA-N	DUAL INVERTER	CTL	1120 0995 E	MSP
1123 9092 C	108	BA-N	DUAL BUFFER	CTL	1120 0938 D	MSP
1123 9100 C	112	FA-0	J/K FLIP FLOP	CTL	1121 2958 E	MSP
1123 9134 C	103	AMCN	8 BIT MEMORY CELL	CTL	1124 5776 D	MSP
1269 7041		DVCN	DIFFERENTIAL COMP.			
1269 7561		CRC1	CRC GENERATOR/CHECKER	TTL	1269 7561 A	DOWN
1447 3557		T3AH	TRIPLE 3 INPUT AND	TTL	1447 3557	DOWN
1447 3581		B2CN	OPEN COLLECTOR BUFFER	TTL	1447 3581 C	DOWN
1447 3714		S4-N	DUAL 4 INPUT MUX	TTL	1447 3714	DOWN
1447 3771		CR4N	4 BIT BINARY COUNTER	TTL	1447 3771	DOWN
1447 3797 A		S2-N	QUAD 2 IN MUX	TTL	1447 3797	DOWN
1447 9455		P001	256 X 4 PROM	TTL	1447 9455	DOWN
1448 9165		FF01	64x4 FIFO MEMORY	MOS	1448 9165 A	DOWN
1449 1104		RW06	1024 BIT RAM	TTL	1449 1104	DOWN
1471 4356 D	56	IHCN	HEX INVERTER	DTL	1471 4356 D	PLYM
1471 4398	98	IDCN	2 X 4 BUFFER	DTL	1471 4398	PLYM
1479 0240		T2HN	QUAD 2 INPUT NAND	TTL	1479 0240	DOWN
1673 0004 B	513	S8MN	DUAL SENSE AMP.	TTL		EMSO
1673 0319		IQBN	TTL TO MOS LVL CONV		1673 0319	EMSO
1674 4963 E		IHDN	OPEN COLLEC. HEX INV	TTL	1674 4963 E	DOWN
1674 4971 B		IQAN	QUAD MOS DRIVER			EMSO
1674 5150 D		RAM1	1024 BIT MEMORY	MOS		EMSO
1675 0572		RPON	25 OHM RESISTOR PACK			EMSO
1675 0580		RPCN	RES/CAP PACKAGE			EMSO
1675 0754 A		RPAN	200 OHM RESISTOR PACK			EMSO
1677 7682		SAMN	DUAL SENSE AMPLIFIER	TTL		EMSO
1705 7480	305	IF-N	DUAL INVERTER	CTL	1705 7498 D	LSPT
1705 7563	308	BF-N	DUAL BUFFER	CTL	1705 7571 B	LSPT
1779 6137	167	FFAN	DUAL JK/D FLIP FLOP	CTL	1780 3123 C	SBP
1779 6145	168	LFAN	QUAD LATCH	CTL	1910 2458 E	SBP
1779 6152	169	RFZN	3-BIT REGISTER	CTL	1780 4196 C	LSPT
1779 6160	170	RF-N	4-BIT REGISTER	CTL	1779 5956 A	LSPT
1901 7102 A	118	TAON	MONOSTABLE MULTI	TTL	1904 0062 C	MSP
1904 0161 B	703	DFAN	1 OF 8 DECODER	CTL	1909 0471 F	SBP
1904 0179	708	AFAN	DUAL FULL ADD/SUB	CTL	1910 2482 G	SBP
1904 0187 B	704	MFAN	8 INPUT MULITPLIXER	CTL	1910 2441 E	SBP
1904 0195	706	CFAN	4-BIT COMPARATOR	CTL	1910 2466 E	SBP
1904 0245	702	BHAN	HEX RESTORER	CTL	1909 0463 E	SBP
1904 0252	701	IHAN	HEX INVERTER	CTL	1909 0455 F	SBP
1907 7726	501		DUAL OP AMPLIFIER			MSP
1909 0513 B	707	CFBN	CARRY LOGIC GATE	CTL	1910 2474 E	SBP
1911 9098 C	415	GFIN	4,3,3 GATE	CTL	1929 4701 C	MSP
1911 9106 C	420	GFJN	3,2,2,2 GATE	CTL	1929 4693 B	MSP
1914 0748 B	722	EFAN	PRIORITY ENCODER	CTL	1914 0755 E	SBP
1916 5133 C	410	GFEN	1,1,1,1 GATE	CTL	1929 4679 B	MSP
1916 5158 C	411	GBFN	8 INPUT GATE	CTL	1929 4636 A	MSP
1916 5794 C	404	GFFN	2,2,2,2 GATE	CTL	1929 4677 B	MSP

NUMERICAL (Continued)

STANDARD ASSEMBLY	MACH NO	DA DESC	DESCRIPTION	LOGIC FAM	ELECTRICAL SPEC (REV)	DOC CONT
1916 5851 C	407	GFBN	4,4 AND GATE	CTL	1929 4628 B	MSP
1916 6115 C	419	MOPN	MICRO OPERATOR	CTL	1916 6131 B	MSP
1918 3599 C	724	MI1N	EBCDIC ASCII MSB	TTL	1918 3631 B	MSP
1918 3607 C	725	MI2N	EBCDIC ASCII LSB	TTL	1918 3631 B	MSP
1918 3615 C	726	MI3N	ASCII EBCDIC MSB	TTL	1918 3631 B	MSP
1918 3623 C	727	MI4N	ASCII EBCDIC LSB	TTL	1918 3631 B	MSP
1918 4282 D	414	GFKN	3,2,2,2 GATE (NL)	CTL	1929 4644 B	MSP
1942 6428 A	775	DFRN	DUAL LINE RECEIVER	CTL	1942 6436 B	MSP
1948 5051		BTSN	TRI-STATE HEX BUFFER	TTL	1948 5051	MSP
1948 5069		ITSN	TRI-STATE HEX INV.	TTL	1948 5069 A	MSP
1959 5719		MCPU	8 BIT MICROPROCESSOR	MOS	1959 5719	MSP
1959 5727		SCTL	SYSTEM CONTROLLER	TTL	1959 5727	MSP
2200 8320 B	618	RPNN	500 OHM RES PACK			SBP
2200 8460 B	511		VIDEO AMPLIFIER		2201 5044 B	SBP
2200 8478 A	615	DL2N	20 NSEC DELAY LINE		2201 5010 A	SBP
2200 8486 A	616	DL5N	50 NSEC DELAY LINE		2201 5028 B	SBP
2200 8494 A	617	DLCN	100 NSEC DELAY LINE		2201 5036 B	SBP
2201 4062	746	RFBN	4-BIT REGISTER	CTL	2201 4104 F	SBP
2201 4096	745	RFAN	3-BIT REGISTER	CTL	2201 4054 E	SBP
2201 4146 B	749	MH1N	HOLL EBCDIC LSB	TTL	1918 3631 B	MSP
2201 4153 B	750	MH2N	HOLL EBCDIC MSB	TTL	1918 3631 B	MSP
2201 4161 B	747	MH3N	EBCDIC HOLL LSB	TTL	1918 3631 B	MSP
2201 4179 B	748	MH4N	EBCDIC HOLL MSB	TTL	1918 3631 B	MSP
2201 7602 2	143	LDGN	QUAD LINE DRIVER		2201 7602 2	SBP
2204 4200 C	753	MJ1N	96 COL EBCDIC LSB	TTL	1918 3631 B	MSP
2204 4218 C	754	MJ2N	96 COL EBCDIC MSB	TTL	1918 3631 B	MSP
2204 4226 C	755	MJ3N	EBCDIC 96 COL LSB	TTL	1918 3631 B	MSP
2204 4234 C	756	MJ4N	EBCDIC 96 COL MSB	TTL	1918 3631 B	MSP
2204 4291 A		GB1N	DTL CTL LVL CONV			SBP
2204 4309 A		GB2N	DTL CTL LVL CONV			SBP
2204 4317 A		GB3N	CTL DTL LVL CONV			SBP
2204 4325 A		GB4N	CTL MOS CLK CONV			SBP
2204 4333 A		GB5N	CTL MOS CLK CONV			SBP
2204 4341 A		GB6N	CTL MOS CLK CONV			SBP
2204 4358 A		DP1N	DISCR DIODE ARRAY			SBP
2204 4366 A		DP2N	DISCRETE DIODE ARRAY			SBP
2204 5124 C	757	MK1N	EBCDIC BCL PAR LSB	TTL	1918 3631 B	MSP
2204 5132 C	758	MK2N	EBCDIC BCL PAR MSB	TTL	1918 3631 B	MSP
2204 9761 B	142	SSRN	DUAL 100 BIT S/R	MOS	2204 9779 D	SBP
2205 2609 C	752	RFCN	64 BIT MEMORY	TTL	2205 2617 B	SBP
2205 6188		RP2N	2.2K RESISTOR PACK			SBP
2206 1626 A	765	RFDN	256 BIT MEMORY	TTL	2206 1634 C	SBP
2206 6922	633	RP6N	RESISTOR NETWORK			SBP
2206 6930	634	RP8N	RESISTOR NETWORK			SBP
2207 1716 B	772	SSAN	QUAD 100 BIT S/R	MOS	2207 1724 E	SBP
2207 8273 A	779	LRPN	DUAL LINE RECEIVER		2201 6216 A	SBP
2207 8299 A	780	LDPN	DUAL LINE DRIVER		2201 6224 A	SBP

NUMERICAL (Continued)

STANDARD ASSEMBLY	MACH NO	DA DESC	DESCRIPTION	LOGIC FAM	ELECTRICAL SPEC (REV)	DOC CONT
2208 0014 C	776	RM1N	EBCDIC KATAKANA LSB	TTL	1918 3631 B	MSP
2208 0022 C	777	RM2N	EBCDIC KATAKANA MSB	TTL	1918 3631 B	MSP
2208 4834	631	CP1N	200 PF CAP PACK			
2210 9821 A		GB7N	DISCRETE ASSEMBLY			SBP
2210 9839 A		GB8N	DISCRETE ASSEMBLY			SBP
2210 9847 A		GB9N	DISCRETE ASSEMBLY			SBP
2212 2592		OSCD	307.2 KHz XTAL.CLK.OSC.			SBP
2219 4534		MPPI	PROG PERIPHERAL INTRF.	MOS	2219 4534	SBP
2314 2847		OSCC	12 MHz XTAL.CLK.OSC			SBP
2315 2127		UART	ASY. REC./TRANS.	MOS	2315 2127	VIEJ
2319 5274 A		PR4N	256 X 4 PROM	TTL	2319 5274 A	VIEJ
2319 5282 A		PR5N	512 X 4 PROM	TTL	2319 5282 A	VIEJ
2475 2222		LDDN	DUAL LINE DRIVER	TTL		
2540 0656		RW13	1024 BIT RAM	TTL	1449 1104 C	DOWN
2602 2889		S140	DUAL 4 INPUT LINE DRV	TTL	2602 2889	DOWN
2602 7300		B2TS	QUAD TRI-STATE BUFFER	TTL	2602 7300 D	DOWN
2604 2044		T1BR	HEX RECEIVER/HYSTRS	TTL	2604 2044 B	DOWN
2607 6075		PR08	32 x 8 PROM	TTL	2607 6075 A	DOWN
2623 5945		RAM2	4K BIT DYNAMIC RAM	MOS	2623 5945 A	EMSO

DOCUMENT CONTROL PLANT ABREVIATIONS ARE AS FOLLOWS:

SBP - CSG/SANTA BARBARA
MSP - CSG/PASADENA
PLYM - PLYMOUTH PLANT
EMSJ - ELECTRONIC MEMORY SYSTEMS ORGANIZATION (PISCATAWAY, N.J.)
LSPT - CSG/TREDYFFRIN
DOWN - CSG/DOWNINGTOWN
VIEJ - CSG/MISSION VIEJO

ALPHABETICAL

STANDARD ASSEMBLY	MACH NO	DA DESC	DESCRIPTION	LOGIC FAM	ELECTRICAL SPEC (REV)	DOC CONT
1904 0179	708	AFAN	DUAL FULL ADD/SUB	CTL	1910 2482 G	SBP
1123 9134 C	103	AMCN	8 BIT MEMORY CELL	CTL	1124 5776 D	MSP
1123 9092 C	108	BA-N	DUAL BUFFER	CTL	1120 0938 D	MSP
1705 7563	308	BF-N	DUAL BUFFER	CTL	1705 7571 B	LSPT
1904 0245	702	BHAN	HEX RESTORER	CTL	1909 0463 E	SBP
1948 5051		BTSN	TRI-STATE HEX BUFFER	TTL	1948 5051	MSP
1447 3581		B2CN	OPEN COLLECTOR BUFFER	TTL	1447 3581 C	DOWN
2602 7300		B2TS	QUAD TRI-STATE BUFFER	TTL	2602 7300 D	DOWN
1904 0195	706	CFAN	4-BIT COMPARATOR	CTL	1910 2466 E	SBP
1909 0513 B	707	CFBN	CARRY LOGIC GATE	CTL	1910 2474 E	SBP
2208 4834	631	CP1N	200 PF CAP PACK			
1269 7561		CRC1	CRC GENERATOR/CHECKER	TTL	1269 7561 A	DOWN
1447 3771		CR4N	4 BIT BINARY COUNTER	TTL	1447 3771	DOWN
1904 0161 B	703	DFAN	1 OF 8 DECODER	CTL	1909 0471 F	SBP
1942 6428 A	775	DFRN	DUAL LINE RECEIVER	CTL	1942 6436 B	MSP
2200 8478 A	615	DL2N	20 NSEC DELAY LINE		2201 5010 A	SBP
2200 8486 A	616	DL5N	50 NSEC DELAY LINE		2201 5028 B	SBP
2200 8494 A	617	DLCN	100 NSEC DELAY LINE		2201 5036 B	SBP
2204 4358 A		DP1N	DISCR DIODE ARRAY			SBP
2204 4366 A		DP2N	DISCRETE DIODE ARRAY			SBP
1269 7041		DVCN	DIFFERENTIAL COMP.			
1914 0748 B	722	EFAN	PRIORITY ENCODER	CTL	1914 0755 E	SBP
1123 9100 C	112	FA-O	J-K FLIP FLOP	CTL	1121 2958 E	MSP
1779 6137	7167	FFAN	DUAL JK/D FLIP FLOP	CTL	1780 3123 C	SBP
1448 9165		FF01	64x4 FIFO MEMORY	MOS	1448 9165 A	DOWN
1916 5158 C	411	GBFN	8 INPUT GATE	CTL	1929 4636 A	MSP
2204 4291 A		GB1N	DTL CTL LVL CONV			SBP
2204 4309 A		GB2N	DTL CTL LVL CONV			SBP
2204 4317 A		GB3N	CTL CTL LVL CONV			SBP
2204 4325 A		GB4N	CTL MOS CLK CONV			SBP
2204 4333 A		GB5N	CTL MOS CLK CONV			SBP
2204 4341 A		GB6N	CTL MOS CLK CONV			SBP
2210 9821 A		GB7N	DISCRETE ASSEMBLY			SBP
2210 9839 A		GB8N	DISCRETE ASSEMBLY			SBP
2210 9847 A		GB9N	DISCRETE ASSEMBLY			SBP
1916 5851 C	407	GFBN	4,4 AND GATE	CTL	1929 4628 B	MSP
1916 5133 C	410	GFEN	1,1,1,1 GATE	CTL	1929 4679 B	MSP
1916 5794 C	404	GFFN	2,2,2,2 GATE	CTL	1929 4677 B	MSP
1911 9098 C	415	GFIN	4,3,3 GATE	CTL	1929 4701 C	MSP
1911 9106 C	420	GFJN	3,2,2,2 GATE	CTL	1929 4693 B	MSP
1918 4282 D	414	GFKN	3,2,2,2 GATE (NL)	CTL	1929 4644 B	MSP
1123 9050 C	105	IA-N	DUAL INVERTER	CTL	1120 0995 E	MSP

ALPHABETICAL (Continued)

STANDARD ASSEMBLY	MACH NO	DA DESC	DESCRIPTION	LOGIC FAM	ELECTRICAL SPEC (REV)	DOC CONT
1471 4398	98	IDCN	2 X 4 BUFFER	DTL	1471 4398	PLYM
1705 7480	305	IF-N	DUAL INVERTER	CTL	1705 7498 D	LSPT
1904 0252	701	IHAN	HEX INVERTER	CTL	1909 0455 F	SBP
1471 4356 D	56	IHCN	HEX INVERTER	DTL	1471 4356 D	PLYM
1674 4963 E		IHDN	OPEN COLLEC. HEX INV	TTL	1674 4963 E	DOWN
1674 4971 B		IQAN	QUAD MOS DRIVER			EMSO
1673 0319		IQBN	TTL TO MOS LVL CONV		1673 0319	EMSO
1948 5069		ITSN	TRI-STATE HEX INVERTER	TTL	1948 5069 A	MSP
2475 2222		LDDN	DUAL LINE DRIVER	TTL		
2201 7602 2	143	LDGN	QUAD LINE DRIVER		2201 7602 2	SBP
2207 8299 A	780	LDPN	DUAL LINE DRIVER		2201 6224 A	SBP
2602 2889		S140	DUAL 4 INPUT LINE DRV	TTL	2602 2889	DOWN
1779 6145	168	LFAN	QUAD LATCH	CTL	1910 2458 E	SBP
2207 8273 A	779	LRPN	DUAL LINE RECEIVER		2201 6216 A	SBP
1959 5719		MCPU	8 BIT MICROPROCESSOR	MOS	1959 5719	MSP
1904 0187 B	704	MFAN	8 INPUT MULTIPLEXER	CTL	1910 2441 E	SBP
2201 4146 B	749	MH1N	HOLL EBCDIC LSB	TTL	1918 3631 B	MSP
2201 4153 B	750	MH2N	HOLL EBCDIC MSB	TTL	1918 3631 B	MSP
2201 4161 B	747	MH3N	EBCDIC HOLL LSB	TTL	1918 3631 B	MSP
2201 4179 B	748	MH4N	EBCDIC HOLL MSB	TTL	1918 3631 B	MSP
1918 3599 C	724	MI1N	EBCDIC ASCII MSB	TTL	1918 3631 B	MSP
1918 3607 C	725	MI2N	EBCDIC ASCII LSB	TTL	1918 3631 B	MSP
1918 3615 C	726	MI3N	ASCII EBCDIC MSB	TTL	1918 3631 B	MSP
1918 3623 C	727	MI4N	ASCII EBCDIC LSB	TTL	1918 3631 B	MSP
2204 4200 C	753	MJ1N	96 COL EBCDIC LSB	TTL	1918 3631 B	MSP
2204 4218 C	754	MJ2N	96 COL EBCDIC MSB	TTL	1918 3631 B	MSP
2204 4226 C	755	MJ3N	EBCDIC 96 COL LSB	TTL	1918 3631 B	MSP
2204 4234 C	756	MJ4N	EBCDIC 96 COL MSB	TTL	1918 3631 B	MSP
2204 5124 C	757	MK1N	EBCDIC BCL PAR LSB	TTL	1918 3631 B	MSP
2204 5132 C	758	MK2N	EBCDIC BCL PAR MSB	TTL	1918 3631 B	MSP
1916 6115 C	419	MOPN	MICRO OPERATOR	CTL	1916 6131 B	MSP
2219 4534		MPPI	PROG PERIPHERAL INTRF.	MOS	2219 4534	SBP
2314 2847		OSCC	12 MHz XTAL.CLK.OSC			SBP
2212 2592		OSCD	307.2 KHz XTAL.CLK.OSC			SBP
1447 9455		P001	256 X 4 PROM	TTL	1447 9455	DOWN
2607 6075		PR08	32 X 8 PROM	TTL	2607 6075 A	DOWN
2319 5274 A		PR4N	256 X 4 PROM	TTL	2319 5274 A	VIEJ
2319 5282 A		PR5N	512 X 4 PROM	TTL	2319 5282 A	VIEJ
1674 5150 D		RAM1	1024 BIT MEMORY	MOS		EMSO
2623 5945		RAM2	4K BIT DYNAMIC RAM	MOS	2623 5945 A	EMSO
1779 6152	169	RFZN	3-BIT REGISTER	CTL	1780 4196 C	LSPT
2201 4096	745	RFAN	3-BIT REGISTER	CTL	2201 4054 E	SBP
2201 4062	746	RFBN	4-BIT REGISTER	CTL	2201 4104 F	SBP
1779 6160	170	RF-N	4-BIT REGISTER	CTL	1779 5956 A	LSPT

ALPHABETICAL (Continued)

STANDARD ASSEMBLY	MACH NO	DA DESC	DESCRIPTION	LOGIC FAM	ELECTRICAL SPEC (REV)	DOC CONT
2205 2609 C	752	RFCN	64 BIT MEMORY	TTL	2205 2617 B	SBP
2206 1626 A	765	RFDN	256 BIT MEMORY	TTL	2206 1634 C	SBP
2208 0014 C	776	RM1N	EBCDIC KATAKANA LSB	TTL	1918 3631 B	MSP
2208 0022 C	777	RM2N	EBCDIC KATAKANA MSB	TTL	1918 3631 B	MSP
1675 0754 A		RPAN	200 OHM RES PACK			EMSO
1675 0580		RPCN	RES/CAP PACKAGE			EMSO
1675 0572		RPON	25 OHM RESISTOR PACK			EMSO
2200 8320 B	618	RPNN	500 OHM RES PACK			SBP
2205 6188		RP2N	2.2K RESISTOR PACK			SBP
2206 6922	633	RP6N	RESISTOR NETWORK			SBP
2206 6930	634	RP8N	RESISTOR NETWORK			SBP
1449 1104		RW06	1024 BIT RAM	TTL	1449 1104	DOWN
2540 0656		RW13	1024 BIT RAM	TTL	1449 1104 C	DOWN
1677 7682		SAMN	DUAL SENSE AMPLIFIER	TTL		EMSO
1673 0004 B	513	SBMN	DUAL SENSE AMP.	TTL		EMSO
1959 5727		SCTL	SYSTEM CONTROLLER	TTL	1959 5727	MSP
2207 1716 B	772	SSAN	QUAD 100 BIT S/R	MOS	2207 1724 E	SBP
2204 9761 B	142	SSRN	DUAL 100 BIT S/R	MOS	2204 9779 D	SBP
1447 3797 A		S2-N	QUAD 2 IN MUX	TTL	1447 3797	DOWN
1447 3714		S4-N	DUAL 4 INPUT MUX	TTL	1447 3714	DOWN
1901 7102 A	118	TAON	MONOSTABLE MULTI.	TTL	1904 0062 C	MSP
2604 2044		T18R	HEX RECEIVER/HYSTRS.	TTL	2604 2044 B	DOWN
1479 0240		T2HN	QUAD 2 INPUT NAND	TTL	1479 0240	DOWN
1447 3557		T3AH	TRIPLE 3 INPUT AND	TTL	1447 3557	DOWN
2315 2127		UART	ASY. REC./TRANS.	MOS	2315 2127	VIEJ
1907 7726	501		DUAL OP AMPLIFIER			MSP
2200 8460 B	511		VIDEO AMPLIFIER		2201 5044 B	SBP

DOCUMENT CONTROL PLANT ABREVIATIONS ARE AS FOLLOWS:

SBP - CSG/SANTA BARBARA
MSP - CSG/PASADENA
PLYM - PLYMOUTH PLANT
EMSO - ELECTRONIC MEMORY SYSTEMS ORGANIZATION (PISCATAWAY, N.J.)
LSPT - CSG/TREDYFFRIN
DOWN - CSG/DOWNINGTOWN
VIEJ - CSG/MISSION VIEJO

4.2 Comparative Costs

The basic assumption is that a selected gate cost within each category (CTL, TTL/DTL, and MOS) is taken as 1.00, or unity. Costs for other complex devices within each category are compared to unity.

CTL Integrated Circuits

Number	DA #	Brief Description	Rel. Cost
1904	0179	AFAN Dual Fl Adder/Sub	3.69
1123	9134	AMCN 8 Bit Memory	2.14
1705	7563	GB-N Dual Buffr (2,2)	1.00
1904	0245	BHAN Hex Restorer	1.29
1904	0195	CFAN 4 Bit Comparator	4.05
1909	0513	CFBN Carry Logic Gate	4.02
1904	0161	DFAN 1 of 8 Decoder	4.48
1914	0748	EFAN Priority Encoder	4.21
1909	0505	FFAN Dual JK/D F-Flop	3.69
1916	5851	GFBN Dl And Gates 4,4	1.05
1916	5133	GFEN Qd Gates 1,1,1,1	1.05
1916	5794	GFFN Qd And Gates	1.05
1911	9098	GFIN Triple And Gates	1.17
1911	9106	GFJN Qd And Gates (3,2,2,2)	1.17
1918	4282	GFKN Qd And Gates(3,2,2,2)	1.17
1705	7480	IF-N Dual Invrtr. (2,2)	1.05
1904	0252	IHAN Hex Inverter	1.40
1904	0203	LFAN Quad Latch	4.05
1904	0187	MFAN 8 Inpt Multiplxr	3.90
1916	6115	MOPN Micro Operator	1.52
2201	4096	RFAN 3 Bit Register	19.88
2201	4062	RFBN 4 Bit Register	10.24

CTL III

2309	1804	AFAN Dual Fl Adder/Sub	4.38
2309	1887	FFAN Dual JK/D F-Flop	4.52
2308	6234	BG-N Dual Buffr (2,2)	1.31
2308	6275	BHAN Hex Restorer	1.31
2309	1846	CFAN 4 Bit Comparator	5.38
2309	1861	LFAN Quad Latch	5.95
2309	2141	RFBN 4 Bit Register	7.43

TTL/DTL Integrated Circuits

Number	DA #	Brief Description	Rel. Cost
1901	7102	TAON Mnstble Multivib.	1.24
1471	4356	IHCN DTL Hex Invrter.	1.00
1674	4963	IHCN TTL Hex Invrter.	1.12
2205	2609	RFCN 64 Bit RAM	8.00
2206	1626	RFDN 256 Bit RAM	10.00
2212	6403	RW06 1K RAM	39.20
1447	9455	POO1 256 x 4 PROM	18.00
1449	2060	POO2 32 x 8 PROM	13.00
1447	3797	S2-N Quad 2-In Max.	2.20
		1K ROMs	13.60

MOS Integrated Circuits

Number	DA #	Brief Description	Rel. Cost
1674	5150	RAM1 1024 Bit Memory	1.03
2207	1716	SSAN Quad 100 Bit Shift Register	1.00
2204	9761	SSRN Dual 100 Bit Shift Register	1.11

5.0 CARD IMPLEMENTATION & INTERFACE RULES

5.1 B-1700 Card Description

5.1.1 Size

The B-1700 card dimensions are as shown in Figure 5-1. They are approximately 11.750 inches by 14.250 inches.

5.1.2 Card Edge Contacts

Each card is equipped with 50 edge contacts on each side. Figures 5-1 and 5-2 show the contacts and their code designations.

5.1.3 Device Accommodations

DIPS - Mounting facilities are provided for 120 D.I.P. I.C. devices. They are mounted on the component side as shown in Figure 5-1. Position designations are by letter row plus number row as in Figure 5-1. Individual D.I.P. lead pins are designated from A to S as shown in Figure 5-3. Letters I, O, and Q are not used.

Bus Bars - Provisions have been made for the mounting of up to 5 bus bars on the component side as shown in Figure 5-1.

Coax Connector - Each board has provision for mounting one coax connector for clock connection if needed. This is shown in the two views of Figure 5-4.

Frontplane Connectors - There are four positions for frontplane connectors, as shown in Figure 5-4. Each connector has 50 contacts. It can be used to provide 25 individual signals or 12 signal pairs for memory daisy chain.

Internal Resistors - One or two discrete resistors may be substituted for a D.I.P. I.C. package, as shown in Figure 5-4, unless mounted on a Header chip as in Fig. 5-7 where 8 1/4 w Resistors, Diodes, etc. may be mounted.

Pull Down Resistors - The use of discrete resistors is provided for at the bus bar end of the D.I.P. I.C. location, as shown in Figure 5-4 and 5-5. Normal use is for the resistor to be tied to -2.0V. For special requirements it can be tied to 4.75V or ground. Resistor Network packages are the preferred component to be used when numerous pull downs are required; however, discrete resistors may be used when I.C. chip locations are not available or only a minimum number of resistors are required. Pins R & S of I.C. locations shall not be used for mounting a resistor. These resistors should be placed at the end of the net.

Frontplane Resistor Buses - Provisions have been made for tapping or terminating up to 100 resistors to two buses at the front card edge. Each group of 50 has an X or Y designation plus position number and letter. This is shown in Figure 5-4 on the component side. The two frontplane resistor buses are provided for pull down/load resistors of frontplane signals, or for internal circuits when a frontplane signal does not have a pull down/load resistor. See Figure 5-6. Preferred usage is to have the outboard bus at -2.0V and the inboard bus at +4.75V or ground. The standard artwork coverfile and DA programs exist for preferred usage. In the event a non-standard usage is required for a particular application, the Standard Packaging Section should be contacted.

Internal Filter Capacitors - The Cover File provides pads for 30 internal filter capacitors. The capacitors filter the VCC (+4.75V) supply to ground. Six capacitors may be mounted above each bus bar. See PAGE 11.

Ground Mesh - A separate ground mesh is formed on each half of the board by first tying the four backplane ground pins together with a horizontal etch; second by tying the three front plane connector ground lines together with a combination of vertical and horizontal etch; and lastly, by joining these two ground circuits with vertical etch that extends from the top of the board to the bottom and interconnects to the bus bar ground pins and the pins that require ground at the chip locations. See PAGE 11.

Power Connections - Typical Power Connections from the bus bars to the D.I.P. I.C. devices are shown in PAGE 11.

Locations C0 and D0 show connections for a 14 Pin TTL Device; locations F0 and F1, a 16 Pin TTL Device. Location D1 shows connections for a resistor package that requires -2.0 Volts. Other locations show CTL Power Connections.

Power connections to discrete internal resistors are shown at resistor locations: A0, A1 and B0 of PAGE 11. Resistor A0 is connected to -2.0 Volts (B0Z);A0Y is the signal side of the resistor.

Resistor A1 is connected to +4.75 Volts (B1Z);A1W is the signal side.

Resistor B0 is connected to ground (B0Y);C0Z is the signal side.

Buses for -12 Volts are provided in a special Cover File. See PAGE 11 Ref. A. Connections from these buses to D.I.P. I.C. locations are made by placing a via at the intersection of either horizontal grid 117 or 125 and any even vertical grid. From this via, vertical etch must extend one grid either up or down and horizontal etch may extend

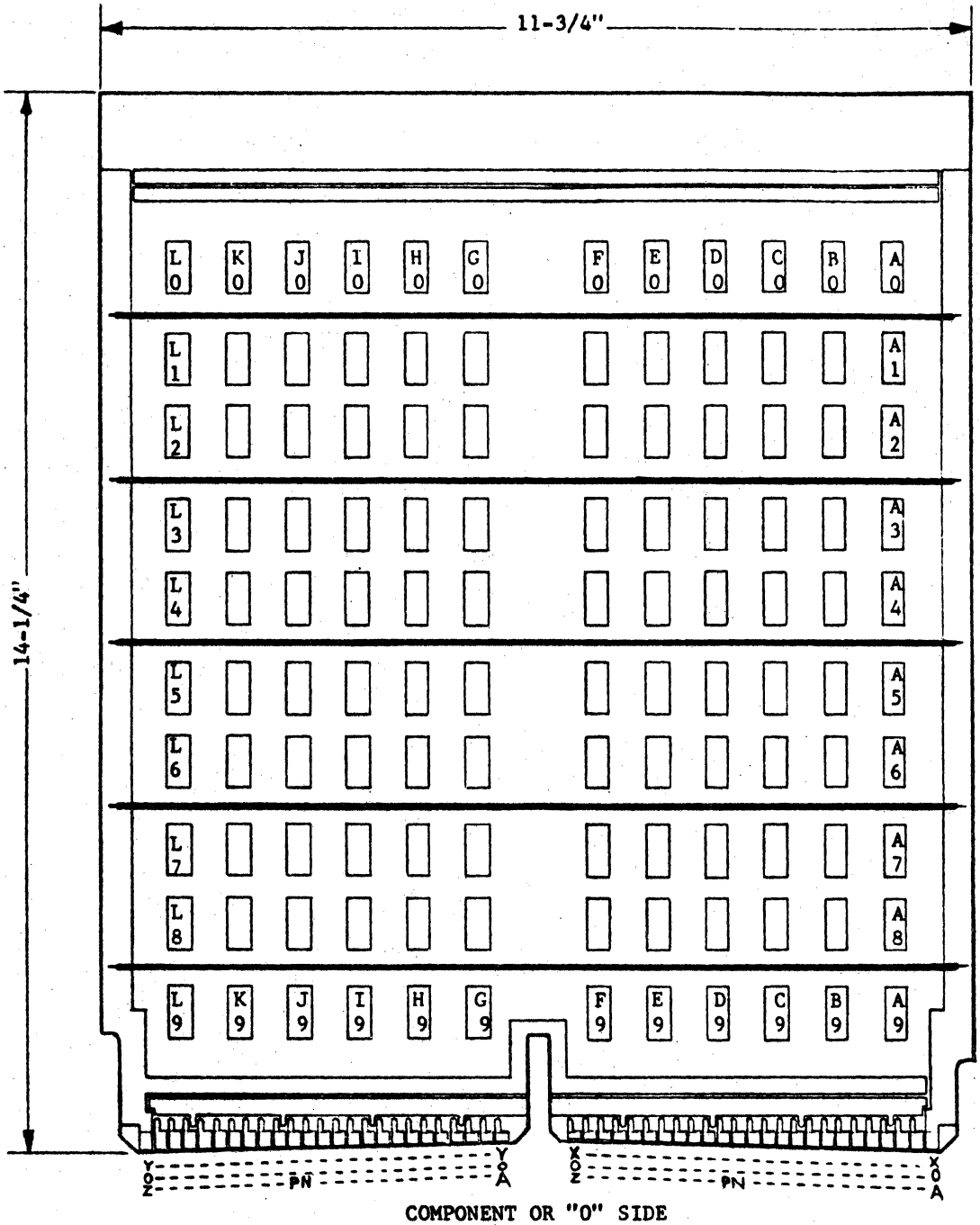
left or right to the desired I.C. location. See PAGE 11 Ref. B.

The -12 Volt cover file also provides capabilities for filter capacitors on the -12 Volt buses above each bus bar. See PAGE 11 Ref. C.

If -12 Volts is not required on a board, the -12 Volt cover file is not used and these 4 vertical grids may be used for running etch of logic signals. Vias or feed-throughs can not be placed on the two inner grids. See PAGE 11 Ref. D. The holes for the -12 Volt filter capacitors will not appear on a non -12 Volt board and horizontal etch may pass through these areas.

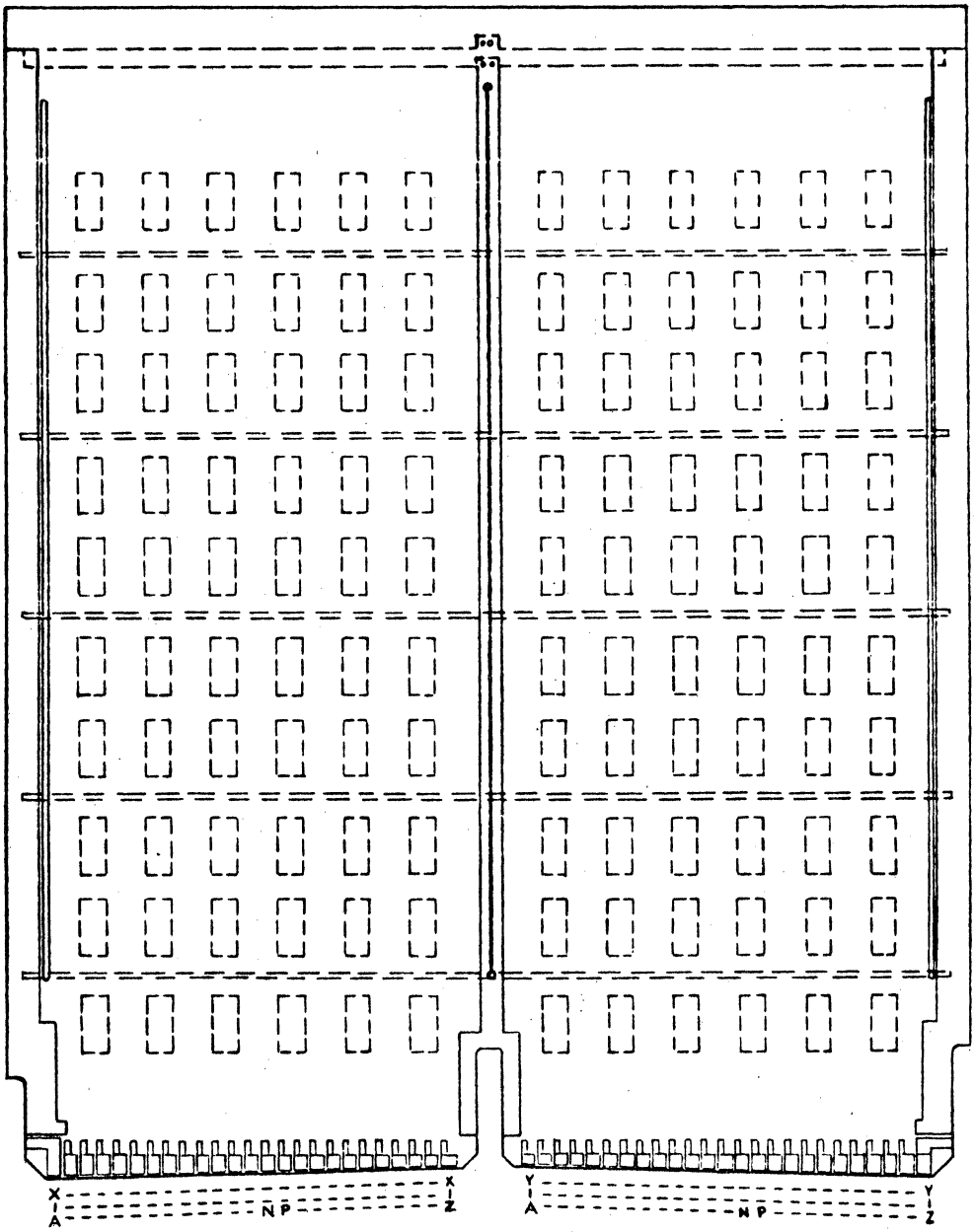
Vias - Vias or feed-throughs can not be placed side by side; they must be on a diagonal. Vias may be placed at any grid intersection that has not been eradicated. See PAGE 11 Ref. E for Do's and don'ts.

Critical Nets - All clock nets are critical. They must be wired serially and may not have stubs longer than 2". Terminating resistor must be located within 2" of the end of net.



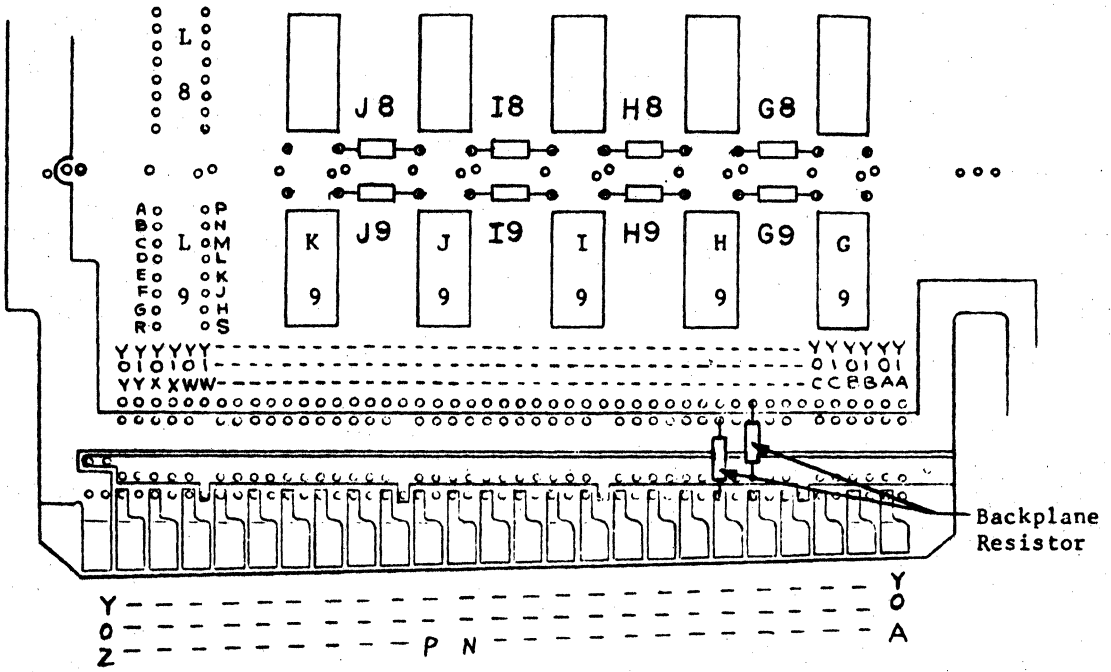
COMPONENT OR "0" SIDE

Fig. 5-1

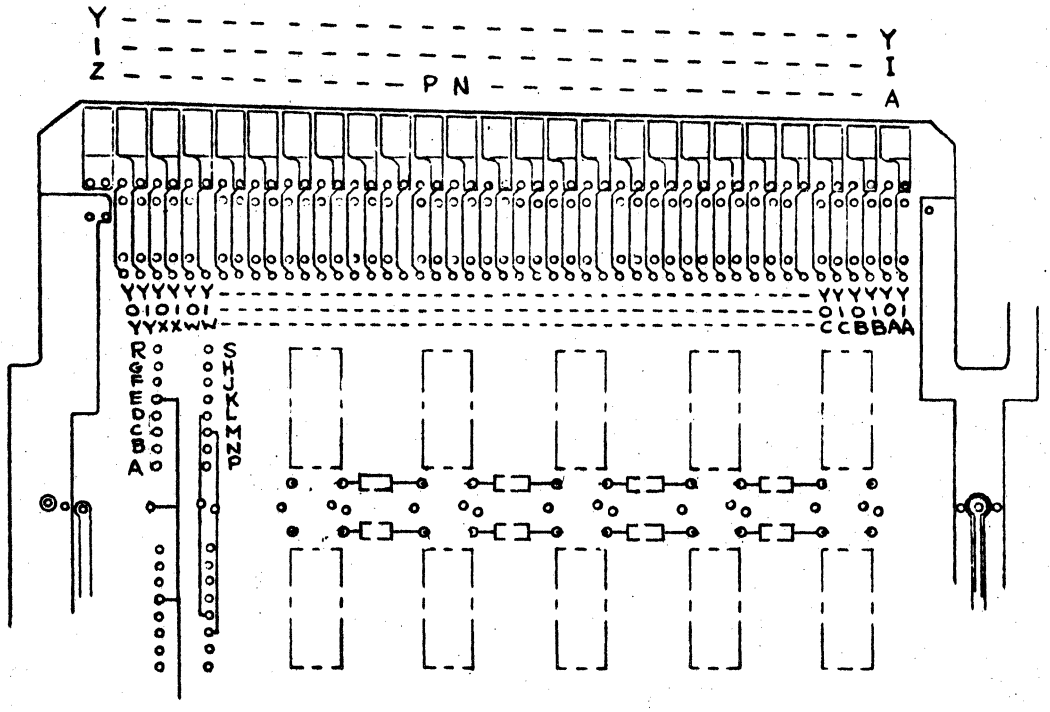


SOLDER OR "1" SIDE

Fig. 5-2

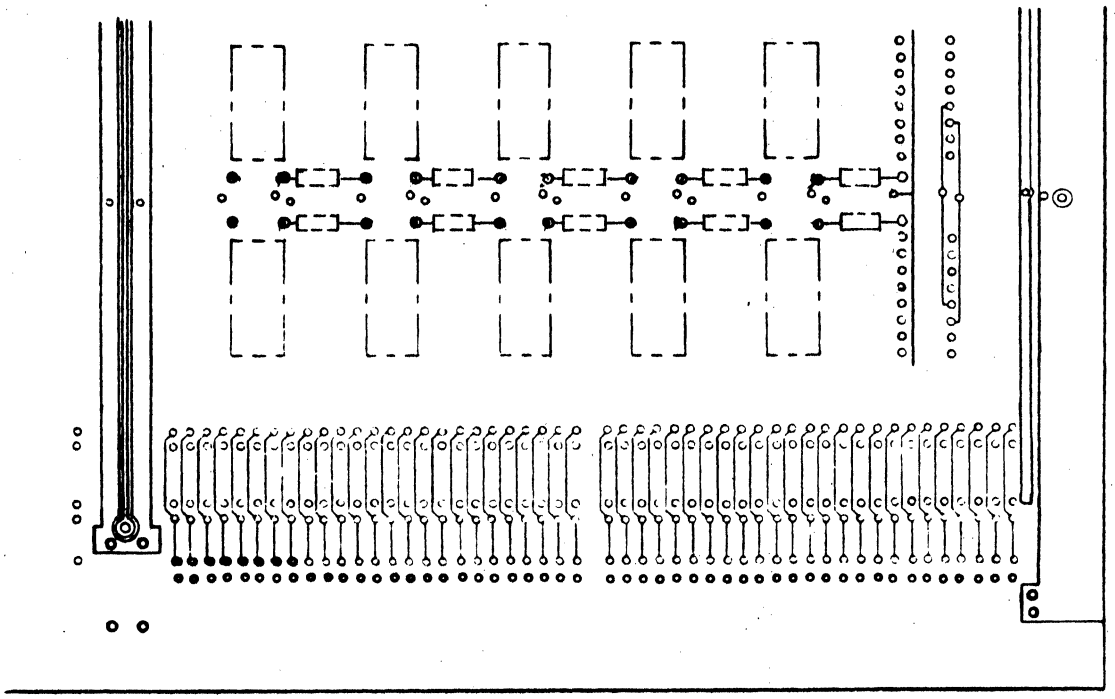


COMPONENT OR "0" SIDE

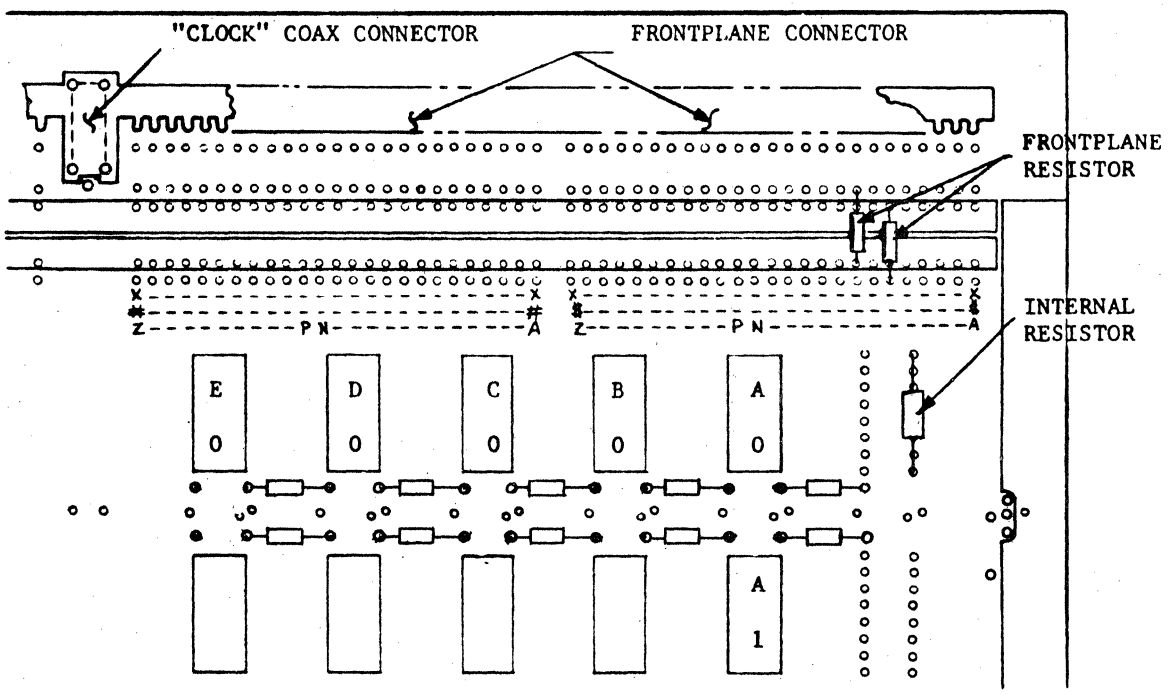


SOLDER OR "1" SIDE

Fig. 5-3



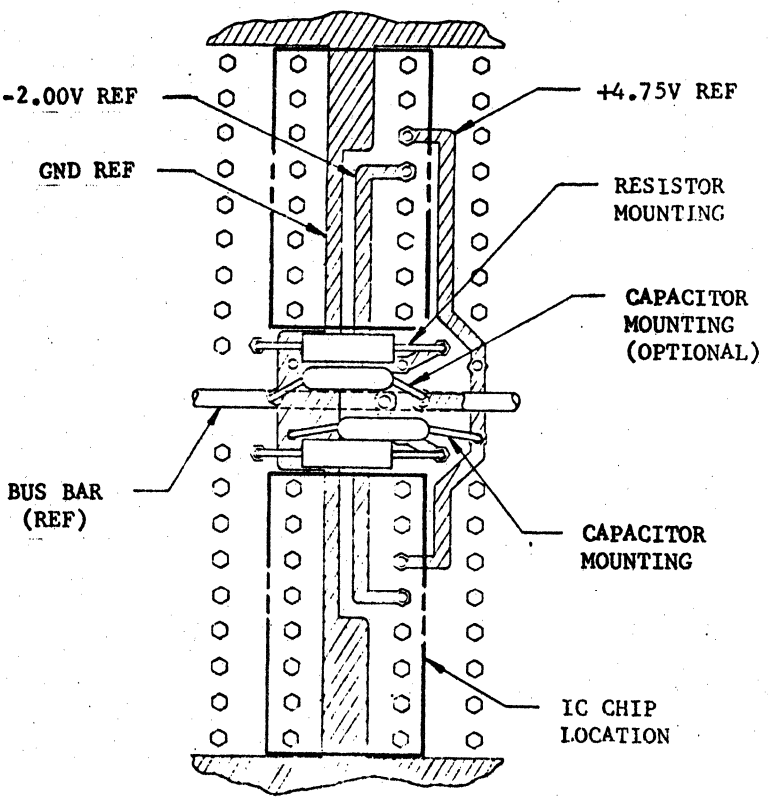
SOLDER OR "1" SIDE



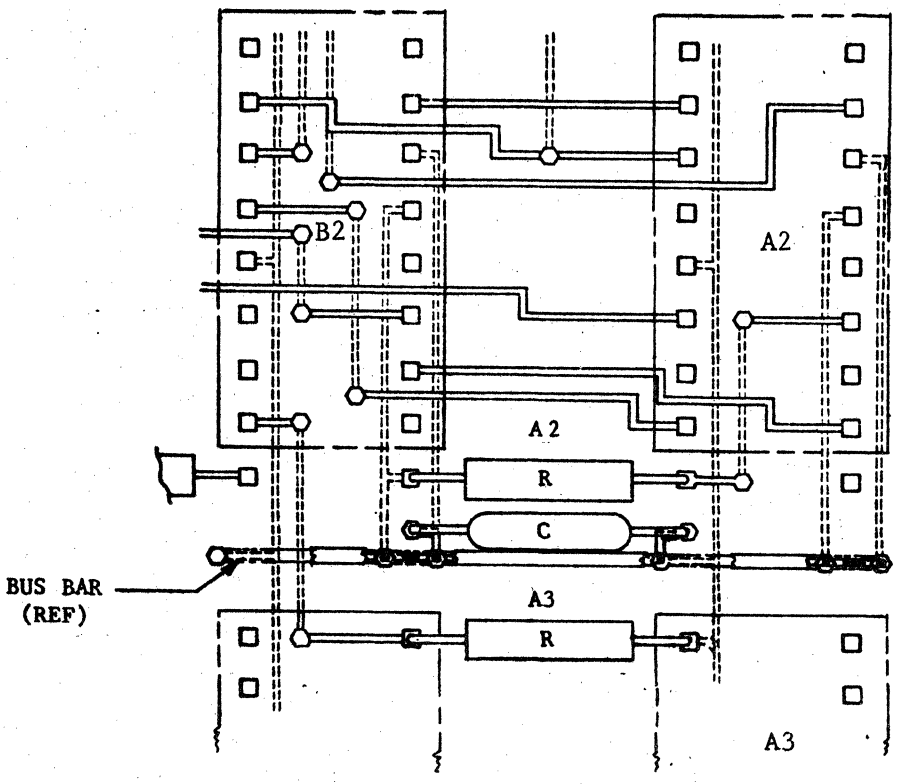
COMPONENT OR "0" SIDE

Fig. 5-4

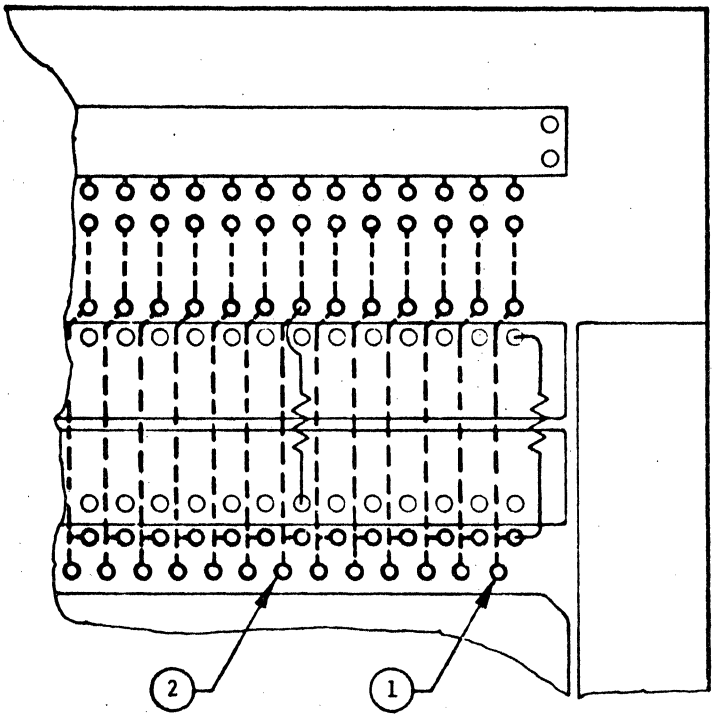
FIGURE 5.5



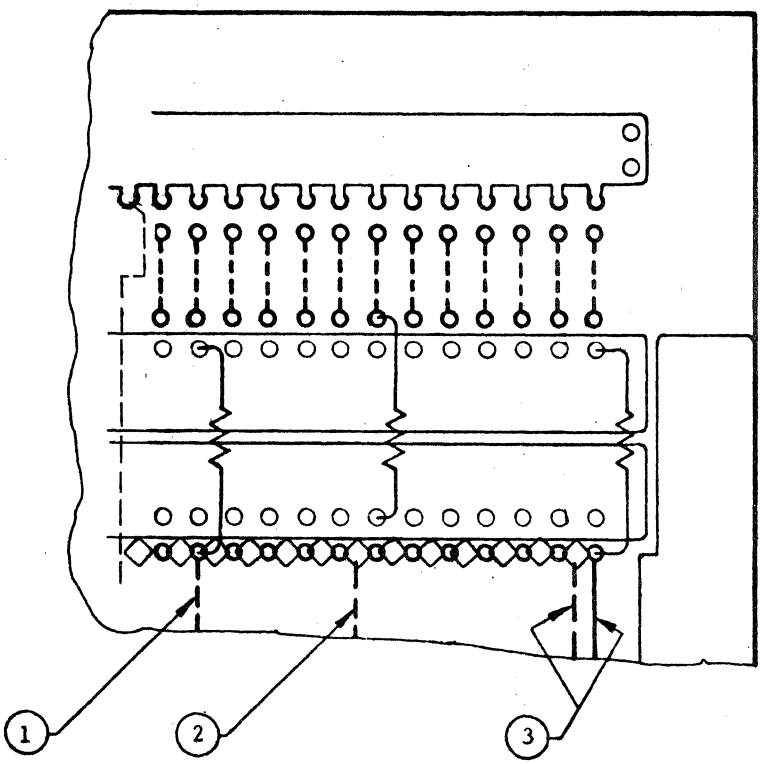
WIRE/WRAP



ETCHED CARD



WIRE WRAP BOARD



ETCHED BOARD

(1) Frontplane signal to pull down or termination resistor.

(2) Frontplane signal to pull up or termination resistor.

(3) Frontplane signal with no pull-down/load resistor, resistor location used for internal pull-down/load.

FIGURE 5-6

5.1.3 Cont'd.

Backplane Resistors - Up to 88 backplane resistors can be implemented on the 1700 card. Their position is described by an X or Y location plus a letter pair and 0 or 1 designation. This is shown on the component side in Figure 5-3. They are terminated at their other end at one of two buses having ground or -2 volts.

Fixed Pin Usage - The following backplane pins have a fixed usage:

Pins X0A and X1A --- +4.75 volts
" Y0Z " Y1Z --- -2.0 volts
" X1D " X1J --- Ground
" X1Q " X1W --- "
" Y1D " Y1J --- "
" Y1Q " Y1W --- "

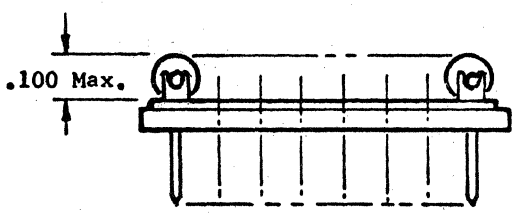
Optional Pin Usage - The following backplane pins have optional usage:

Pins X0Z and/or Y1A --- -12.0 volts
Pin X0W Clock

Computer Mainframe DC Voltage Supplied to Peripherals - Any DC voltage which must be supplied to a peripheral from the computer mainframe must not be routed through the peripheral logic control card and its interface ribbon cable. DC voltage can be provided by the addition of discrete wire from the interface connector to the DC voltage power source in the computer mainframe. These voltages are limited to -2.0V, +4.75V, +12.0V and -12.0V.

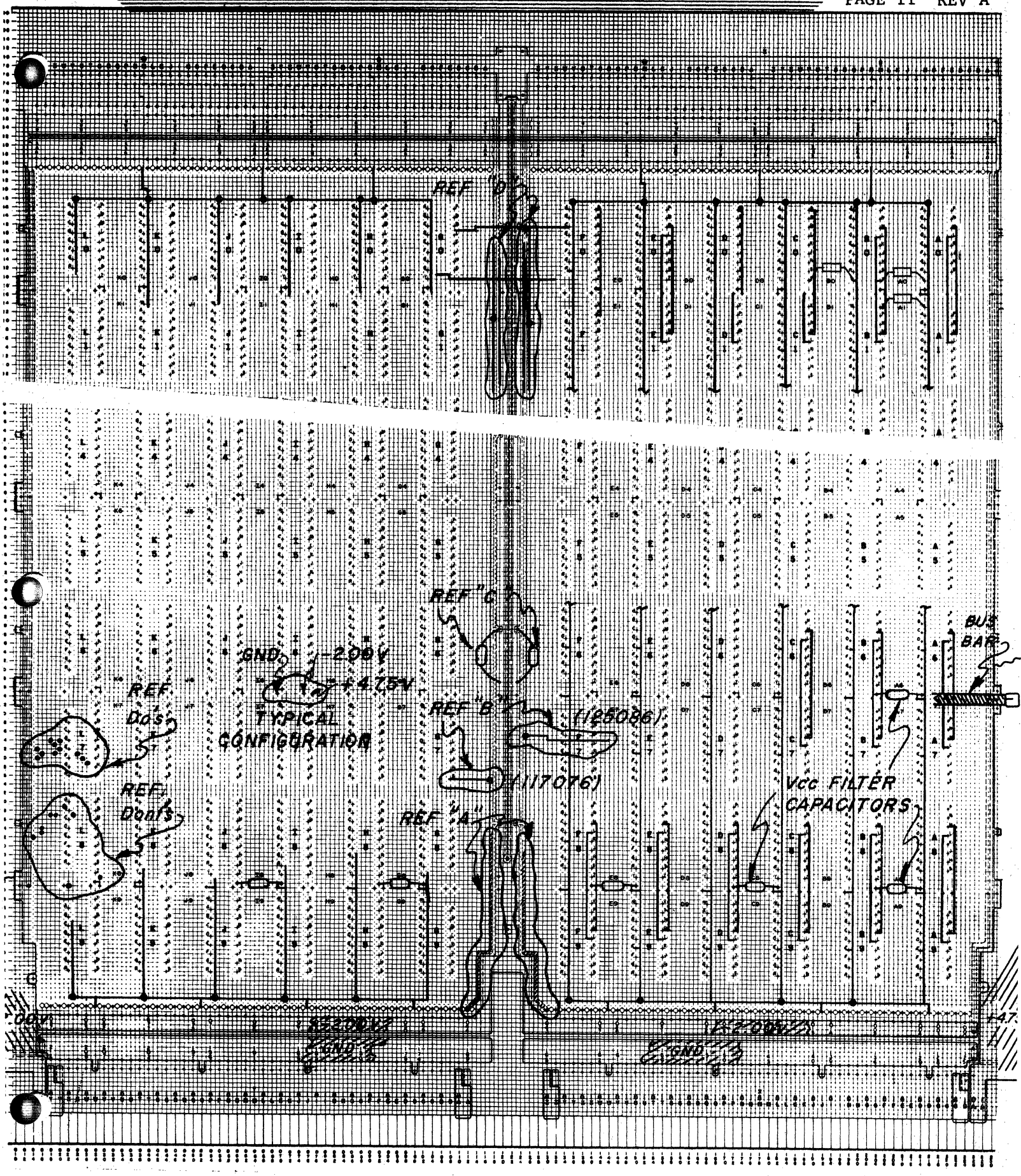
Card to Card I.C. Jumper Cables - In the event that insufficient frontplane and/or backplane pins are available to intra/inter-connect a card to another unit or card within the unit, the use of an I.C. jumper cable may be required. This is a cable which plugs into a 16 pin I.C. socket at either end. Two such cables exist, P/N 2206 3416 a 12 conductor cable and P/N 2210 0762 a 16 conductor cable, each of a given length. Their use is undesireable except in extreme conditions. When an I.C. jumper cable is found necessary, their receiving sockets should be preferably located in the frontplane or "0" I.C. chip location column. If said location cannot be made available, another even numbered column should be used, such as "2", "4", etc., as close to the frontplane as possible, so that the cable can pass over the card bus bars and so that the cable covers a minimum number of other I.C. devices.

Use of Sockets with Header Assemblies - When assemblies are made on 16 pin headers (P/N 2201 4732), they may be used in I.C. sockets only if no component, wiring, solder, etc., extend more than .100 inch above the top surface of the header plaque. Those header assemblies which may be used in sockets are therefore generally limited to wired jumpers, 1/4W resistors and diodes. See Figure 5-7. All higher assemblies must be soldered directly into the board and shall not exceed .400 inch above board in height.



HEADER ASSEMBLY

FIGURE 5-7



ETCHED BOARD LAYOUT (REF)

5.1.4 Modified 120 Chip P.C. Board

In order to improve design and assembly efficiency the 120 chip board was modified on 10/31/74. Following is a list of the modifications. Examples of the modifications are given on page 10.

1. NO vias are permitted as follows:
   a. Horizaontally, vertically or diagonally adacent to IC or resistor mounting pads. Ref. absence of grid intersections on layout sheet at IC locations, frontplane, backplane and IC load resistor locations.
   b. Horizontally or vertically adacent to the bus bar mounting pads. Ref. absence of grid intersections on layout sheet.
   c. Vertically along the voltage buses at the edges and along the clock ground bus in the center of the board, X-axis coordinates 014, 015 partial, 118, 124 and 228 on boards without -12V. Additionally, on boards with -12V, vertically along the -12V bus, X-axis coordinates 117 and 125. Ref. absence of grid intersections on layout sheet for "without -12V" condition.

2. Power circuits, -2V and +4.75V, are not permitted as follows:
   a. Between or dog-leg between bus bar pads.
   b. Adjacent to bus bar pad of different potential, including ground.
   c. Horizontally between or adjacent to IC or resistor mounting pads on the normal vertical run or solder side.
   d. Vertically adjacent to IC or resistor mounting pads on the normal horizontal run or component side.

3. No circuit is permitted to occupy the grid intersection used by bus bar capacitor connection, as this connection occurs on both sides of the board.

   Placement of Bypass Capacitors and Resistors.
   a. The bypass capacitors along the bus bar were inserted in the same vias as the bus bar leads. In the modified board, separate vias are provided for the bypass capacitors placed along the bus bars.
   b. Previously resistors were placed in line with the IC location; resistors for the modified board are placed between IC locations.

4. Vias diagonally adjacent to bus bar pads are discouraged. They are permitted if no other solution exists for routing.

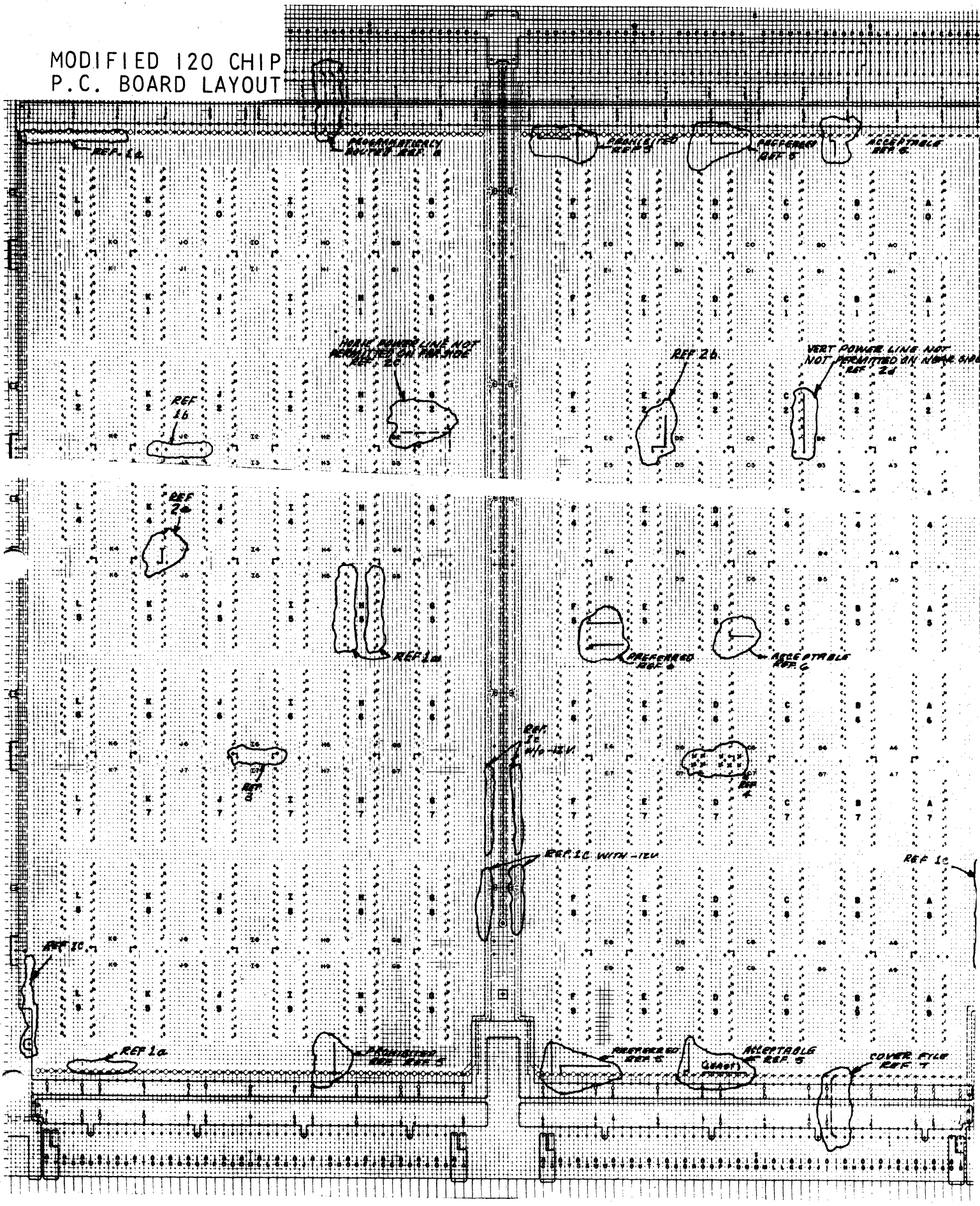
5. Circuits to frontplane and backplane load resistors must rout straight in. Dog-leg connections between pads are prohibited. Additonally, horizontal runs are prohibited in the first grid below the frontplane resistor pins, either side, Y-axis coordinate 254.

6. Circuits which dog-leg between pads to an IC pin or resistor are discouraged. They are permitted if no other solution exists for routing.

7. All manual routing to the backplane shall stop at Y-axis coordinate 24. Further routing to connector contacts is handled by the coverfile.

8. All manual routing to the frontplane shall stop at Y-axis coordinate 255. Further routing to connector pins is handled programmatically by Design Automation.

MODIFIED 120 CHIP P.C. BOARD LAYOUT



5.2 Unused Inputs

5.2.1 CTL Inputs

Inputs of CTL circuits which have internal pulldown resistors shall be set to a logical true level according to the following preferred order:

a) Unused input connected to the output of an unused inverter. The fanout of the inverter is not to exceed its DC Output Drive Capability.

b) Connect the unused input to V_{cc} through a resistance given by Table 5-1. The value of the resistance depends upon the number of CTL inputs that are to be held at the logical true level.

c) Connect the unused input to V_{cc}.

d) Unused and used inputs may be connected together. The logical operation of the circuit should not be changed when this type of connection is employed.

The last two alternatives are to be avoided if possible.

Inputs of CTL circuits which do not have internal pulldown resistors and are to be set to the logical true level shall be tied to the V_{cc} supply.

CTL inputs with internal pulldown resistors that are to be placed at the logical false level shall be left open-circuited.

Those CTL inputs without internal pulldown resistors shall be connected to the V_{EE} supply in order to set them to a logical false level.

5.2.2 TTL Inputs

Unused TTL inputs that are to be placed at a logical true level shall be connected to Vcc through a 1kΩ ½W resistor. Up to 25 inputs may be driven by each 1kΩ resistor. TTL inputs that are to be set at logical false shall be connected to ground.

5.2.3 MOS Inputs

Unused MOS inputs shall be tied directly to Vcc where a True is intended and to ground where a False is needed.

5.3 Interfacing Rules

The interfacing rules give the circuitry to be used whenever CTL and TTL elements are interfaced. Applications of these rules will insure that adequate noise margin and compatible DC levels will be applied to TTL and CTL inputs. Detailed time delay calculations are given in Section 9. For simplicity in the determination of interface resistor values, a 'unit' approach will be used with a 'unit' being equal to the worst case CTL input current of 2.82 mA. This approach will allow direct correlation to CTL loading factors. An example of the unitized values is given below:

A TTL input current of		is equal to a unit load of	
	.25mA		.09
	.4 mA		.14
	1.0 mA		.35
	1.6 mA		.57
	2.0 mA		.7

Tables 5-2 and 5-3 contain a summary of the input and output loading factors for the devices of interest.

Three basic types of interface will be discussed.

1) Resistor pull down to ground
2) Resistor pull up to Vcc
3) Resistor divider - one to ground, one to V_{EE}

Regardless of the type of interface network used, it is the responsibility of the designer to choose the appropriate value of termination resistance. A brief explanation of the thought behind the tables is therefore necessary to assure proper use.

A few basic concepts must be kept in mind. First, 'Input Current' flows <u>into a CTL input</u> in the high state but <u>out of a TTL input</u> in the low state. Second, it is necessary to assure that TTL false level inputs do not exceed +0.4V. TTL outputs are capable of sinking current while CTL outputs source current. With the above mentioned information in mind, it is possible to discuss interfacing techniques in terms of the resistors used as termination rather than the devices. For example, a pull up resistor of 42.2Ω will source 41.9 unit loads into a TTL output. A familiarization with this type of terminology would be highly beneficial to a thorough understanding of the interface techniques used.

5.3.1 CTL to TTL

The application of these rules is valid for all TTL devices. The Circuits Group should be consulted in special cases for interfaces different from that specified here.

TTL circuits shall always be driven by CTL restoring elements. CTL outputs shall not be directly wired to TTL outputs. When interfacing CTL outputs to TTL inputs, four things must be kept in mind.

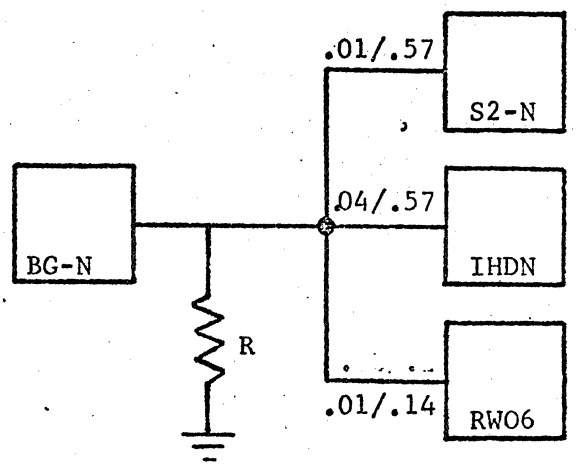
1) The interface technique must assure an input false level ≤.4V. This assures proper noise margin.
2) The CTL output must have sufficient drive to properly operate the interface circuit.
3) The CTL output must be restored. (i.e. Level 0 generator)
4) The TTL input must not be allowed to go more negative than -.4V.

Two methods of interface are possible. First, the CTL element driving a TTL is terminated by a resistor to ground. Second, CTL can interface to TTL through a resistor divider network with one resistor going to ground and the other to V_{EE}. The designer shall select the most appropriate for each particular application.

5.3.2 Termination Resistor to Ground

The CTL driving element is not to have any resistor pull down to V_{EE}. Also, only TTL inputs are to be driven. CTL and TTL inputs cannot be mixed when using this technique. Refer to Figure 5-8. Table 5-6 gives the information necessary to determine the value of the termination resistor. To use the table, first determine the fanout of the CTL driver to be used and consider only the resistors listed for that fan out or a lesser fan out. It should be considered standard practice to load the driver as fully as possible. Second, determine the total low level input loading by summing up the individual load factors. Then select a resistor value capable of sinking the required amount of current.

Consider the following example for clarification.



BG-N fan out = 24

Procedure:
1) Fan out = 24
2) Total low level input loading .57 + .57 + .14 = 1.28
3) From Table 5-6, all resistors ≤ 110Ω are capable of sinking the current.
4) The BG-N has sufficient drive capability

5.3.2 Continued

The value of the terminating resistor selected affects the fall time of the signal waveform. The fall time is a function of the resistor value, number of inputs driven, and length of wiring. The formula below gives the fall time delay:

$$t = (1.609)\left[5 \times 10^{-12}\ (n) + 1 \times 10^{-12}\ (L)\right] R - 2.5$$

where n = number of inputs

L = Length of etch in inches

R = Value of terminating resistor in ohms

t = Time in nanoseconds

5.3.3 Resistor Divider Network

With this divider network, it is possible to drive more TTL inputs than a single resistor to ground and to drive TTL and CTL inputs simultaneoulsy. Refer to Figure 5-9.

When using this interface technique, it is important to remain aware of the fan out of the CTL driving element, and the number of CTL and TTL inputs. When the divider network is used to drive TTL only, a specific set of resistor values will be used to allow maximum drive capability and best noise margin. The appropriate values can be chosen from Table 5-4.

If the interface circuit is used where any CTL inputs will be driven, then the resistor to ground will be specified according to the fan out capability of the driver, and the resistor to V_{EE} (R_2) will be variable and determined by the number of CTL inputs. Table 5-5 indicates the value of R_1 to ground for a given fan out. The correct value of R_2 can be selected from Table 5-7.

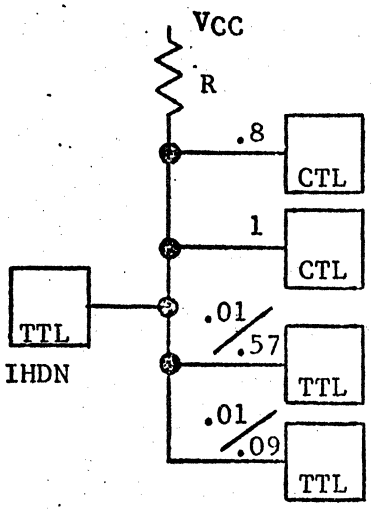
5.3.4 TTL to TTL and CTL

Three modes of interface are possible. First, TTL to TTL, second TTL to CTL, and third, TTL to both TTL and CTL inputs. Either type of TTL output, totem pole or open collector, can be used in any of the modes but only open collector can be used for the wire "AND". Figures 5-10 and 5-11 show the difference between the outputs.

When interfacing to CTL inputs only restoring CTL elements shall be used. TTL outputs shall not be "OR" tied to CTL outputs. Regardless of mode, two parameters are of primary importance when selecting the correct value of pull up resistor. First, the resistor must be capable of providing adequate true level drive and second, the resistor must not overdrive the TTL output when in the low state.

5.3.4 Continued

To determine the correct value of pull up resistor, add up the CTL input loading to be driven and choose a value from the appropriate column of Table 5-6. Next determine if the TTL output is capable of sinking the number of unit loads the resistor will deliver (Table 5-6) and other TTL inputs present. Examine the following example for further explanation.



Total true level loads
.8 + 1 + .01 + .01 = 1.82

Table 5-6 indicates a value of 383Ω is adequate to drive the inputs.

A 383Ω resistor will source 4.6 unit loads into the TTL output.

Total false level loads
4.6 + .57 + .09 = 5.26
since the IHDN will sink 14.2 units the value of R chosen is adequate

When interfacing TTL Totem Pole outputs to TTL inputs only, it may not be necessary to use an external pull up resistor. To determine this, add up the total number of TTL high level unit loads to be driven and compare this value to the output drive capability of the driver.

5.3.5 Equations for Checking Termination Values

This section is primarily for the use of DA personnel.

Variables Defined:

- n = Number of CTL unit loads
- n_a = number of .8 CTL inputs
- n_b = number of 1 CTL inputs
- n_c = number of TTL and CTL true level input unit loads
- n_{th} = number of TTL unit loads (high level)
- n_{tl} = number of TTL unit loads (low level)
- n_o = total number of TTL unit loads into TTL output
- FI = total number of unit loads a TTL output can sink
- FO = Fan out of CTL driver
- R_1 = Resistor to ground in resistor divider network
- R2 = Resistor to V_{EE} in resistor divider network

5.3.5 Continued

1) To check the value of R to ground in the single resistor to ground termination network for CTL to TTL interface.
   a) $FO \geq \frac{887}{R}$ assures sufficient drive
   b) $n_{tl} \leq \frac{147}{R}$ specific maximum number of TTL unit load inputs allowed
2) To check value of R_2 to V_{EE} in the resistor divider network for CTL to TTL and CTL inputs.
   a) $R_2 \geq \frac{1600}{FO - \frac{887}{R_1} - n}$ assures sufficient drive
   b) $R_2 \leq \frac{1600}{\frac{376}{R_1} - n}$ assures proper noise margin and protection of TTL inputs
   c) $n_{tl} \leq .28n_b + .23n_a + \frac{674}{R_2} + .05$ *

   * Specifies maximum number of TTL unit loads allowed.
3) To check value of R to Vcc used to interface TTL to TTL and CTL inputs.
   a) $R \leq \frac{745}{n_c}$ assures adequate true level drive
   b) $FI \geq n_o$ where $n_o = \frac{1773}{R} + n_{tl}$

5.3.6 Special Restrictions Concerning TTL Elements

The following information is intended as a summary of special consideration that must be kept in mind when using TTL devices. This is not a list of all applicable rules.

1) Maximum Etch Length must be observed when circuits are layed out.
   a) Schottky TTL outputs must be within five (5) inches of etch of the most distant receiving element.
   b) High Speed "H" TTL outputs must be within 10 inches of etch of the most distant receiving element.
   c) Standard TTL outputs are allowed 20 inches of etch between input and output. Table 5-2 contains a summary of the TTL devices and type of output.
2) Observe the limitation on the number of wire 'AND' open collector outputs permitted. (Table 5-9)
3) Pull-up resistors should be located at the most distant point from the driver (as close to final receiver as possible).
4) TTL outputs shall not be wire 'ANDed' on the backplane.
5) A pull-up resistor ≤ 287Ω should be used when open collectors are to be wire 'ANDed.'

6) If more than 2 TTL devices are present on any bus bar, then every TTL device using that bus bar should be by-passed with a .1μf capacitor within 1.5 inches of the device.

7) Final copies of truth tables of PROMs that will be released in the design must have all locations defined. This is necessary because pre-programmed state is not known and therefore cannot be guaranteed. This rule holds even if the designer is not concerned with unused locations. ALL LOCATIONS MUST BE DEFINED IN THE FINAL RELEASE PROGRAMMING SPECIFICATION and as a result all locations in the PROM will be programmed.

5.3.7 CTL to CTL

The outputs of CTL devices shall be loaded with resistors to the V_{EE} supply, for speed critical nets. If additional resistive loading is required, the RPnn or SIPN In-line Resistor Networks are to be used for this purpose. If loading by discrete resistance is required and the resistor network cannot be used, then the values of resistance shall be taken from Table 5-10.

CTL outputs may be wired together to perform a logical 'OR' function. The rules governing the application of wired 'OR' connections are the same as those rules for CTL outputs driving CTL inputs. That is, a CTL output which is wired 'OR' with other CTL outputs with internal pull downs is loaded by those internal pull downs. Thus, in order to sum the DC loading on any CTL output, all CTL inputs and pull down resistor values must be accounted for, as well as all wired 'OR' CTL outputs with internal pull down resistances. No-load outputs and inputs present no DC loads to driving elements and are therefore not counted, but they do offer capacitive loading. See Figure 5-12 for an example of summing CTL loads.

CTL outputs with internal pull downs are listed below.

'OR' tied nets can <u>not</u> be loaded heavier than the weakest source in that net. Multiple outputs in the same package (BG-N, IF-N, etc.) can <u>not</u> be 'OR' tied for the purpose of expanding fanout beyond the individual outputs capability.

Element Type	Description	Output Loading
GFBn	Dual And Gates (4,4)	1 CTL Load
GFEn	Quad Gates (1,1,1,1)	
GFFn	Quad And, And/Or Gates (2,2,2 + 2)	
GFIn	Triple And Gates (4,3,3)	
GFJn	Quad And Gates (3,2,2,2)	
IF-n	Dual Inverter	
RFAn	3 Bit Register CI (Carry In)	0.8 $\overline{\text{CTL}}$ Load

5.3.8 Interfacing the 8080A Family Devices

The 8080A microprocessor (MCPU) and its related peripheral devices consist of P and N channel Silicon-Gate MOS, standard TTL, and Schottky TTL circuits. All of the MOS circuits have built-in input and output stages to make them TTL compatible with the exceptions as noted below:

MCPU	Clock inputs Ø1,Ø2	$V_{IH} \geq 9V$
	All other inputs	$V_{IH} \geq 3.3V$
SCTL	CPU Data Bus outputs	$V_{OH} \geq 3.6V$
FF01	Master Reset input	$V_{IH} \geq V_{SS} - 1V$ $V_{SS} = 5V \pm 5\%$
	All other inputs	$V_{IH} \geq 3V$ $(=V_{BAR})$
TIBR	Receiver inputs	Have built-in hysteresis

When interfacing these circuits with other logic families, apply the rules governing TTL circuits where the input or output is TTL compatible. For the others, special arrangement (Such as an open collector TTL with external pull-up resistor) may be necessary and should be handled in conjuction with the Circuits Section.

When tri-state outputs are connected together, at no time should one output be in the active High State while another output is in the active Low State. When driving a node connected to TTL inputs with one or more tri-state outputs, at least one output must be in either the High or Low state in order to guarantee the logic level of that node, unless a resistor termination is present at that node (as will be in the case of transmission lines).

DTL/TTL Unit Loading Summary

DEVICE	INPUT LOADING HIGH	INPUT LOADING LOW	TYPE	OUTPUT LOADING LOW	PROCESS
DF8N			TP	3.5	Standard
A0-A3	.01	.53			
R8I	.01	.27			
LT	.01	2.30			
RFCN	.02	.43	OC	5.3	Standard
RFDN	.01	.09	OC	5.3	Standard
RH06	.01	.14	OC	5.7	Schottky
RH13	.01	.14	OC	5.7	Schottky
IHCN	.01	.57	ACT	10.6	Standard
IHDN	.04	.57	OC	14.2	Standard
IDCN	.01	.53	OC	12.8	Standard
S2-N	.01	.57	TP	5.7	Standard
S4-N	.01	.57	TP	5.7	Standard
TAON	.02	.57	TP	3.2	Standard
1K ROMS	.01	.57	OC	5.3	Standard
256 ROM	.01	.57	OC	5.3	Standard
P001	.09	.57	OC	5.7	Schottky
PR08	.01	.14	OC	5.7	Schottky
PR4N	.01	.14	OC	5.7	Schottky
PR5N	.01	.14	OC	5.7	Schottky
T3AH	.01	.70	TP	7.1	Standard
T2HN	.01	.70	TP	7.1	Standard
8TSN					Standard
normal	.01	.57	TS	13.5	
high Z	.01	.01		.01	
CR4N					Standard
CL,EP,D	.01	.57	TP		
CLK,ET,L	.02	1.14			
Outputs				4.3	
Carry				5.7	
B2CN	.01	.57	OC	17.0	Standard
B2TS			TS		Standard
normal	.01	.57		5.7	
high Z				.01	
ITSN			TS		Standard
normal	.01	.57		11.4	
high Z	.01	.01		.01	

Table 5-2

Pull-up Resistors for Unused CTL Inputs

Number of CTL Loads	Resistance Value (ohms)	Percent Tolerance	Power Dissipation	Burroughs Part Number
1	619	2	0.25 W	1111 8684
2	316	2	0.25 W	1111 8619
3	220	2	0.25 W	2206 6807
4	160	2	0.25 W	2206 6781
5	130	2	0.25 W	2206 6765
6	110	2	0.25 W	2206 6831
7	91	2	0.25 W	2206 6823
8	82	2	0.25 W	2206 6732
9	75	2	0.25 W	1111 8460
10	61.9	2	0.25 W	1111 9445

Table 5-1

Interface Circuits Unit Loading Summary

DEVICE	INPUT LOADING HIGH	INPUT LOADING LOW	OUTPUT TYPE	OUTPUT LOADING LOW
LODN			ACT	2.3
C1,C2	.01	1.1		
D	.03	2.1		
DATA	.01	1.1		
SBMN				5.7
S0,S1	.01	.57		
SC	.03	1.1		
IQAN	2.80	.53		
LDAN	.01	.57	OC	21
IQBN			ACT	
DATA	.01	.09		
T1BR			TP	
DA,DB	.02	1.14		
I6-I1	.02	.01		
Q6-Q1				5.67
S140	.03	1.42	TP	21.3

Table 5-3

CTL Fan	Resistor to Ground	Resistor to VEE	Maximum TTL Units Allowed
24	56.2	220 (discrete) 220 (package)	6.4
12	100	422	3.2
8	160	681 (discrete)	1.7
	150*	680 (package)	

*160 ohms is preferred but 150 may be used when a large number of nets are involved.

Table 5-4

CTL Driver Fanout	R1 to GND
8	162
12	100
24	56.2

Table 5-5

RESISTOR INTERFACE TABLE
(Not including Resistor Divider)

RESISTOR VALUE	# OF UNIT LOADS R WILL SOURCE INTO A TTL OUTPUT		# OF TRUE LEVEL UNIT LOADS R CAN DELIVER AS PULL-UP TO Vcc		# OF UNIT LOADS R CAN SINK AS A PULLDOWN TO GROUND	CTL FAN OUT REQUIRED TO DRIVE R WHEN USED AS TERM. TO GROUND
	TTL to CTL	TTL to TTL	TTL to CTL	TTL to TTL	CTL to TTL	CTL to TTL
42.2	41.9	17.6	3.3	24
51.1	34.6	14.5	2.8	24
56.2	31.4	13.2	2.5	24
61.9	28.5	12.0	2.3	24
68.1	25.9	10.9	2.1	24
75	23.6	9.9	1.9	12
82	21.5	9.1	1.7	12
91	19.4	8.2	1.6	12
100	17.7	7.4	1.4	12
110	16.1	6.7	1.3	12
120	14.7	6.2	1.2	8
130	13.6	5.8	1.1	8
150	11.8	4.9	.9	
160	11.0	4.6	.9	
180	9.8	4.1	.8	
200	8.8	3.7	.7	
220	8.0	3.4	.6	
237	7.5	3.1	.6	
261	6.8	2.8	.5	
287	6.2	2.6	.5	
330	5.4	2.3	.4	
348	5.1	2.1	.4	
383	4.6	1.9	.4	
422	4.2	1.8	.3	
464	3.8	1.6	.3	
470	3.8	1.6	.3	
500	3.7	1.5	.3	
511	3.6	1.5	.3	
562	3.1	1.3	.3	
619	2.9	1.2	.2	
681	2.6	1.1	.2	
750	2.4	1.0	.2	
825	2.1	.9	.2	
909	1.9	.8	.2	
1K	1.8	.7	.1	
1.1K	1.6	.6	.1	
1.21K	1.5	.6	.1	
1.33K	1.3	.6	.1	

TABLE 5- 6

RESISTOR INTERFACE TABLE (Cont.)

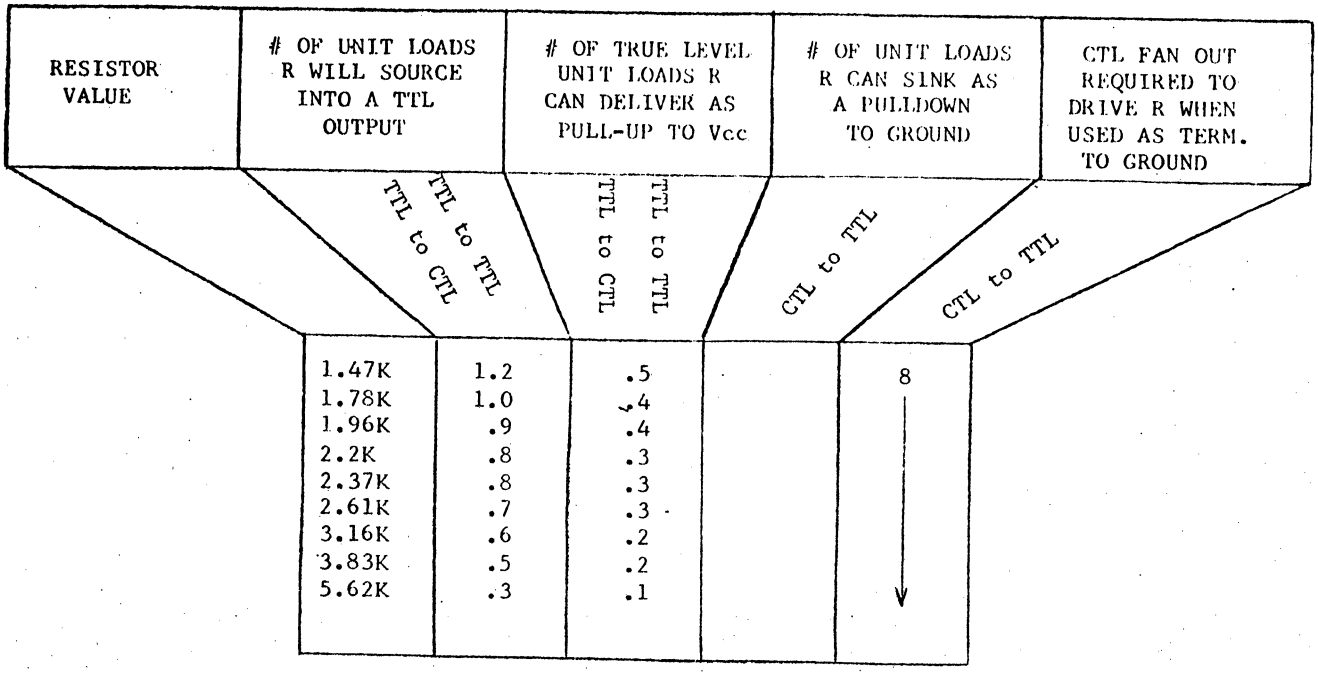


TABLE 5- 6
(Continued)

Where possible, try to use resistor values available in packages. Particularly when several similar interfaces must be made.

Package values available:
100 Ω
150 Ω
220 Ω
330 Ω
470 Ω
500 Ω
680 Ω
1K Ω
2.2K Ω

RESISTOR DIVIDER NETWORK

CTL to TTL

CTL INPUT LOADING	NUMBER OF TTL UNIT LOADS ALLOWED					
	R_2	FAN OUT 24	R_2	FAN OUT 12	R_2	FAN OUT 8
.8	237	3.1	562	1.4	1K	.9
1	237	3.1	619	1.4	1.1K	.9
1.6	261	3.0	825	1.3	1.96K	.8
1.8	287	2.9	909	1.3	2.61K	.8
2.0	287	2.9	1K	1.3	3.83K	.7
2.4	316	2.8	1.21K	1.3		
2.6	316	2.8	1.47K	1.2		
2.8	348	2.8	1.78K	1.2		
3.0	348	2.8	2.37K	1.15		
3.2	383	2.7				
3.4	383	2.7				
3.6	422	2.7				
3.8	422	2.7				
4.0	464	2.6				
4.2	511	2.6				
4.4	511	2.6				
4.6	562	2.5				
4.8	619	2.4				
5.0	681	2.4				
5.2	681	2.4				
5.4	750	2.4				
5.6	909	2.3				
5.8	1K	2.3				
6.0	1.1K	2.3				

TABLE 5- 7

8080A & PERIPHERALS UNIT LOADING SUMMARY *

DEVICE	INPUT LOADING HIGH	INPUT LOADING LOW	TYPE	OUTPUT LOADING LOW	PROCESS
MCPU(8080A)					NMOS
D7-D0	.01	.71		.67	
all others		.01		.67	
SCTL			TP		Schottky
D7-D0	.04	.27		.71	
D87-D30	.01	.09		3.54	
STSTB		.18		3.54	
all others	.04	.09		3.54	
MPPI	.03	.01		.57	NMOS
CRCN	.02	.09	TP	2.84	Standard
FIFO	.18	.01		.57	PMOS

Table 5-8

* All values given in CTL unit loads, 1 CTL unit load = 2.82 mA

Wire "AND" Outputs

Number of CTL Inputs	Number of Wire "AND" TTL Outputs
1	Up to 16
2	Up to 7
3	Up to 2
4	Up to 1
4.2	0

Table 5-9

Table 5-10: CTL Load Resistors

Equivalent Loading To VEE	Equivalent Loading To GND	Resistor Value	Burroughs Part Number	Remarks
38.6	21.4	42.2	1111 8403	A
31.9	17.7	51.1	1111 8429	A
29.0	16.1	56.2	1111 8437	A
26.3	14.6	61.9	1111 8445	B
23.9	13.3	68.1	1111 8452	B
21.7	12.1	75	1111 8460	B
21	11.7	82	2206 6732	C
18.5	10.3	91	2206 6823	C
16.8	9.3	100	2206 6740	C
			2212 2741	PACKAGE A
15.3	8.5	110	2206 6831	C
14	7.8	120	2206 6757	C
12.9	7.2	130	2206 6765	C
11.2	6.2	150	2206 6773	C
			2212 2758	PACKAGE A
10.5	5.8	160	2206 6781	C
9.3	5.2	180	2206 6799	C
8.4	4.7	200	2206 6849	C
7.6	4.2	220	2206 6807	C
			2212 2733	PACKAGE C
6.9	3.8	237	1111 8585	C
6.2	3.5	261	1111 8593	B
5.7	3.2	287	1111 8601	C
5.2	2.9	316	1111 8619	C
4.9	2.7	330	2212 2725	PACKAGE C
4.7	2.6	348	1111 8627	C
4.2	2.3	383	1111 8635	B
3.9	2.1	422	1111 8643	C
3.5	1.9	464	1111 8650	B
3.5	1.9	470	2212 2766	PACKAGE C
3.3	1.8	500		PACKAGE C
3.2	1.8	511	1111 8668	C
2.9	1.6	562	1111 8676	C
2.6	1.5	619	1111 8684	B
2.4	1.3	680	2212 2774	PACKAGE B
2.4	1.3	681	1111 8692	B
2.1	1.2	750	1111 8700	B

Table 5-10: CTL Load Resistors

Equivalent Loading

TO VEE	TO GND	RESISTOR VALUE	BURROUGHS PART NUMBER	REMARKS
1.9	1.1	825	1111 8718	C
1.8	1	909	1111 8726	B
1.6	.9	1K	1111 8734	B
			2212 2782	PACKAGE B
1.5	.8	1.1K	1111 8742	B
1.3	.7	1.21K	1111 8759	B
1.2	.7	1.33K	1111 8767	B
1.1	.6	1.47K	1111 8775	B
.9	.5	1.78K	1111 8791	B
.8	.4	1.96K		B
.8	.4	2.2K		
.7	.4	2.37K	1111 8825	B
.6	.3	2.61K		B
.5	.3	3.16K	1111 8858	B
.4	.2	3.83K		B
.3	.2	5.62K	1111 8916	B

REMARKS:
A - Not acceptable as termination to VEE because of overloading.
B - Not recommended as proper termination to VEE.
C - Recommended as termination to VEE.

Termination Resistors

Termination Point	Resistor Value (ohms)	Percent Tolerance	Power Dissipation	Burroughs Part Number
VEE Supply	511	2	0.25 W	1111 8668
Ground	133	2	0.25 W	1111 8528

Table 5-11

5.4 Circuit Interconnection Restrictions

The following rules apply to CTL devices unless otherwise stated:

a) A maximum of four gate levels is allowed between restoring elements. Levels 3 and 4 shall have a maximum of 18 total DC CTL loads and the etching between the output of the third level gate and the input to the fourth level gate shall not exceed 6 inches. Four levels of gating is not recommended.

b) Level 2, 3 and 4 outputs of gates shall not be connected to the backplane. The output of a level 1 gate that is located on the backplane may not be wire 'OR' connected with other elements.

c) Backplane wires of length greater than 12 inches shall be considered as one level of gating. Thus a level 1 gate which goes through more than 12 inches of backplane wire cannot have more than two gating levels on the next card.

d) Wire 'OR' connections on the backplane shall not have a total length of backplane wire exceeding 30 inches. All wire 'OR' configurations shall be terminated in DC CTL loads to the V_{EE} supply up to the full device fanout capability. The termination shall be centralized as much as possible.

e) Backplane connector pins shall be serially wired. Branching is not allowed. Wire routing is to be determined by the minimum total length of wire that can be achieved. Backplane wires of length greater than 36 inches shall be considered to be transmission lines and are to be terminated close to the receivers with the resistors given in Table 5-11

f) Line etching between any input and any output on a card shall not be greater than 20 inches.

g) Preferably the length of etching for taps on a backplane wire shall be less than 6 inches. A maximum of 4 loads per tap is allowed. Equal resistance and capacitive loading per length of backplane wire is desirable.

(h) TTL devices shall not be wire 'OR' connected on the backplane. Pull-up resistors, pull-down resistors, and CTL interfacing circuits shall be placed on the same card with the associated TTL logic elements. Total length of wire 'OR' etching for TTL devices shall be kept to less than 36 inches. Length of etching between any input and any output shall be less than 12 inches.

(i) Unidirectional transmission lines of characteristic impedance equal to 100 ohms may be driven by restoring elements if the line is terminated at the receiving end by the resistors of Table 5-11. The CTL load of the termination resistors is 10. Frontplane ribbon cables (1.7 ns/ft. delay) have a characteristic impedance between 90 and 110 ohms. The coaxial cables (1.45 ns/ft. delay) with dog house connectors have an impedance of 95 $\pm$ 3 ohms.

(j) Bidirectional transmission lines of characteristic impedance equal to 100 ohms must be driven at both ends by dual buffers or dual inverters and shall be terminated at each end by the resistors given by Table 5-11. The CTL load of the dual termination is 20.

(k) Critical nets should be wired serially with stubs up to 1 inch allowed. Terminating resistors should be placed at the end of the net.

(l) The elements that delay line outputs may drive are restricted to the following element types:

1. BG-N
2. IF-N
3. BHAN
4. IHAN
5. S140
6. No Load Gates

5.5 Circuit Placement Restrictions

The following is a list of circuit placement priorities to be observed in the design of the B/1700:

1) Clock distribution circuitry shall be placed on the row next to the backplane connector pins. This circuitry shall be symmetrically located on the printed circuit card so that clock skew can be kept to a minimum.

2) Line drivers and line receivers shall be placed on the row adjacent to the frontplane connector pins.

3) Gates driving a backplane wire are to be placed preferably next to the backplane connector pin being driven.

4) Circuits that input from other cards or output to other cards shall be placed close to the appropriate input/output connector pin.

5) Circuits shall be placed in such a manner as to minimize the total length of etching for wired 'OR' connections.

5.6 Clock Line Loading

No more than 24 AC loads and 12 active DC loads are allowed. The net should be terminated with at least 12 passive loads. Net length should be limited to 24".

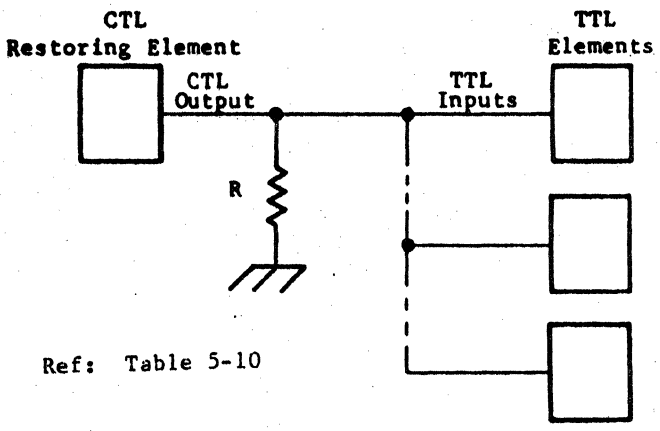


Figure 5-8: Resistor to Ground CTL to TTL Interfacing

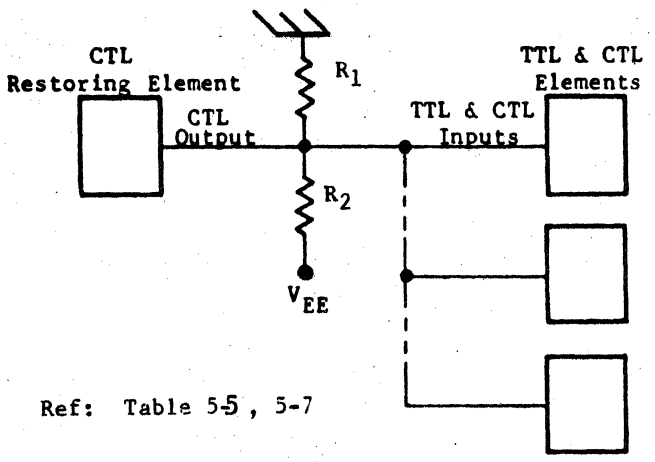


Figure 5-9: Resistor Divider Network CTL to TTL Interfacing

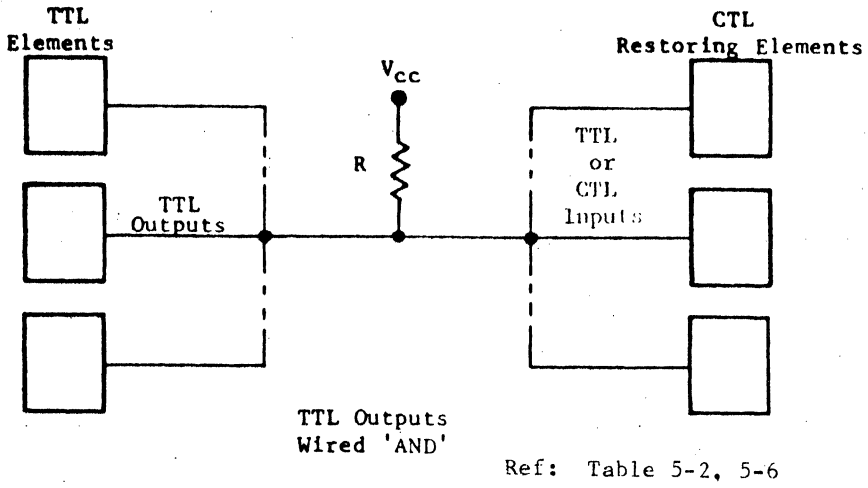


Figure 5-10: Open Collector Output TTL to CTL Interface

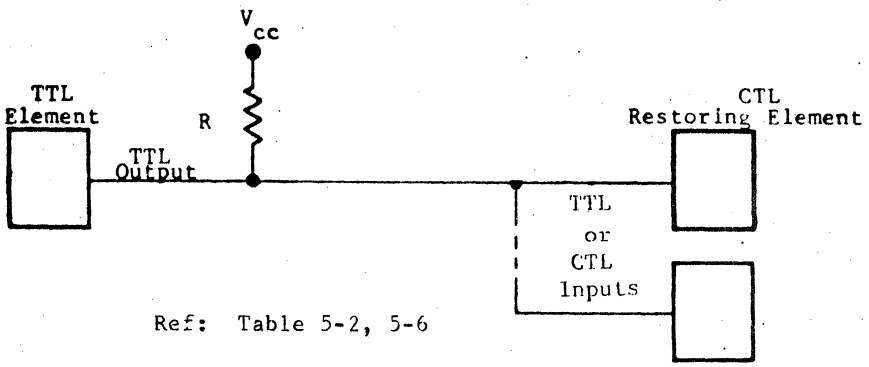
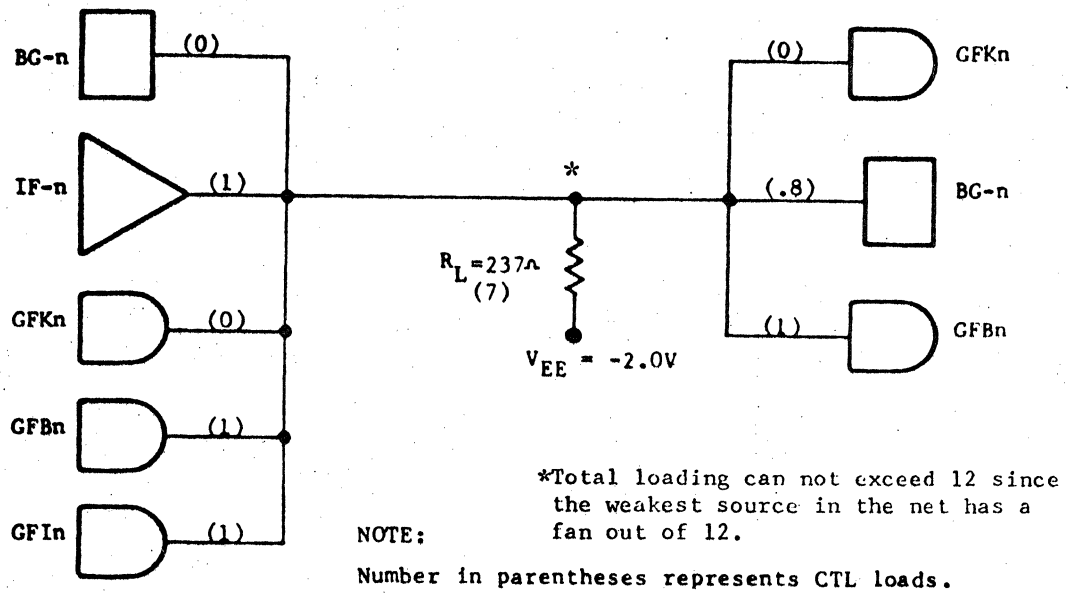


Figure 5-11: Totem Pole Output TTL to CTL Interface



*Total loading can not exceed 12 since the weakest source in the net has a fan out of 12.

NOTE: Number in parentheses represents CTL loads.

Figure 5-12: Example of Output and Input Loading of CTL Outputs

Given: 5 CTL outputs requiring a total of 12 CTL loads.

Find: Value of pull down resistor (R_L).

Rule: The sum of all the CTL input loads (CTL_{IL}) plus all the CTL output loads (CTL_{OL}) plus the load provided by the pull down resistor (R_L) must equal the total load (L_{TOTAL}) required by the CTL output devices, or:

$$\Sigma CTL_{IL} + \Sigma CTL_{OL} + \Sigma R_{CTL\ LOADS} = L_{TOTAL}$$

To find R_L, then,

$$L_{TOTAL} = 12.0$$

$$\Sigma CTL_{IL} = 0 + 0.8 + 1.0 = 1.8$$

$$\Sigma CTL_{OL} = 0 + 1.0 + 1.0 + 1.0 = 3.0$$

$$L_{TOTAL} - R_{CTL\ LOADS} = 4.8$$

$$\therefore R_{CTL\ LOADS} = 12.0 - 4.8 = 7.2\ CTL\ LOADS$$

The actual resistance value may be selected from table 5-10. It is that resistor which provides a CTL load closest to, but not exceeding, 7.2. In this case, the value of R_L turns out to be 237Ω.

6.0 CLOCK DISTRIBUTION

6.1 B1714 Central Clock Distribution. The central system clock distribution is shown in Figure 1. It consists of an 8 MHz oscillator driving a buffer, which is used as a clock driver. The 8MHz signal from the buffer is passed on to the central system backplane. From the backplane, it is distributed to all using cards. In addition, the 8MHz output from the buffer is used internally on the source card to drive a divide-by-two Flip-Flop. This produces two phases of 4MHz (4MHz and $\overline{4MHz}$). The 4MHz signal is the basic clock for the system. Both signals are buffered on to the backplane through clock drivers. These signals are distributed on the backplane to all using cards.

6.1.1 For all these lines, the receiver which is the farthest away from the source is terminated by a resistor on the backplane of the card. The value of the resistor is selected to load the driver to approximately 20 CTμL loads.

6.1.2 The 4MHz signal also passes through a buffer into a delay line (50 nanoseconds). This in turn is routed through a buffer driven to a standard 95.3 ohm coaxial cable to the I/O distribution card. This buffer has its output connected through a pull down resistor, 178 ohm, ½ watt to -2 volts.

6.2 B1712 Central Clock Distribution. The B1712 clock is generated the same as the B1714 clock, except that the oscillator 8MHz signal is divided in half prior to the central system backplane distribution and the divide-by-two Flip-Flop. This produces two phases of 2MHz (2MHz and $\overline{2MHz}$) Clock. See Fig. 1, upper left.

6.3 I/O Clock Distribution. The I/O distribution card receives the early clock (Fig. 2) (SCPE) from the Processor. It goes through a DL5N, then is buffered to feed 6 dog houses on it's front plane. System clocks of all I/O backplanes are picked up from these 6 dog houses. (Dog houses are small shielded connectors).

6.3.1 The distribution card uses one of the above 6 clocks, passing it through a fine delay line (DL2N) and generating 10 independent clocks for distribution to 9 (maximum) cards on the standard I/O backplane and one for it's own use. Each receiving card is required to load it's independent clock (SCPMn) to 8 CTL loads (or equivalent). (See SCPCO term in Fig. 2.)

6.3.2 Two BHANs are used to distribute these 10 clocks. The DL2N is tapped at a point which synchronizes the 9 backplane clock to (up to) 10 nsecs delayed from the processor master clock.

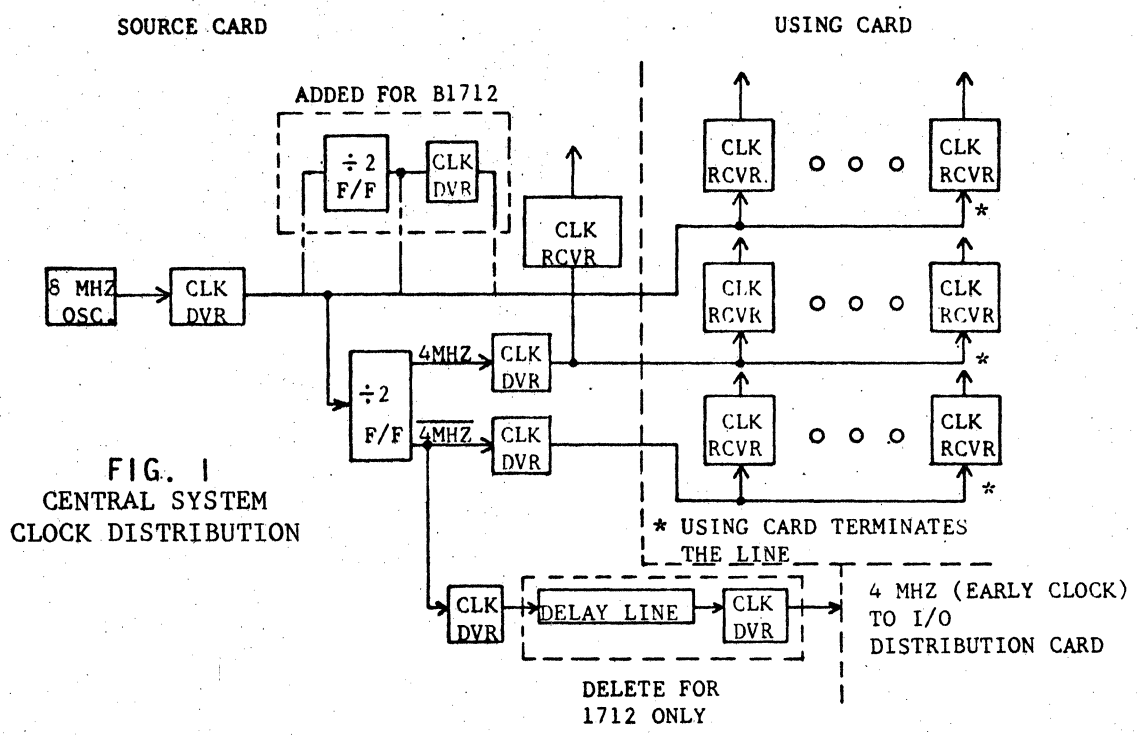


FIG. 1
CENTRAL SYSTEM
CLOCK DISTRIBUTION

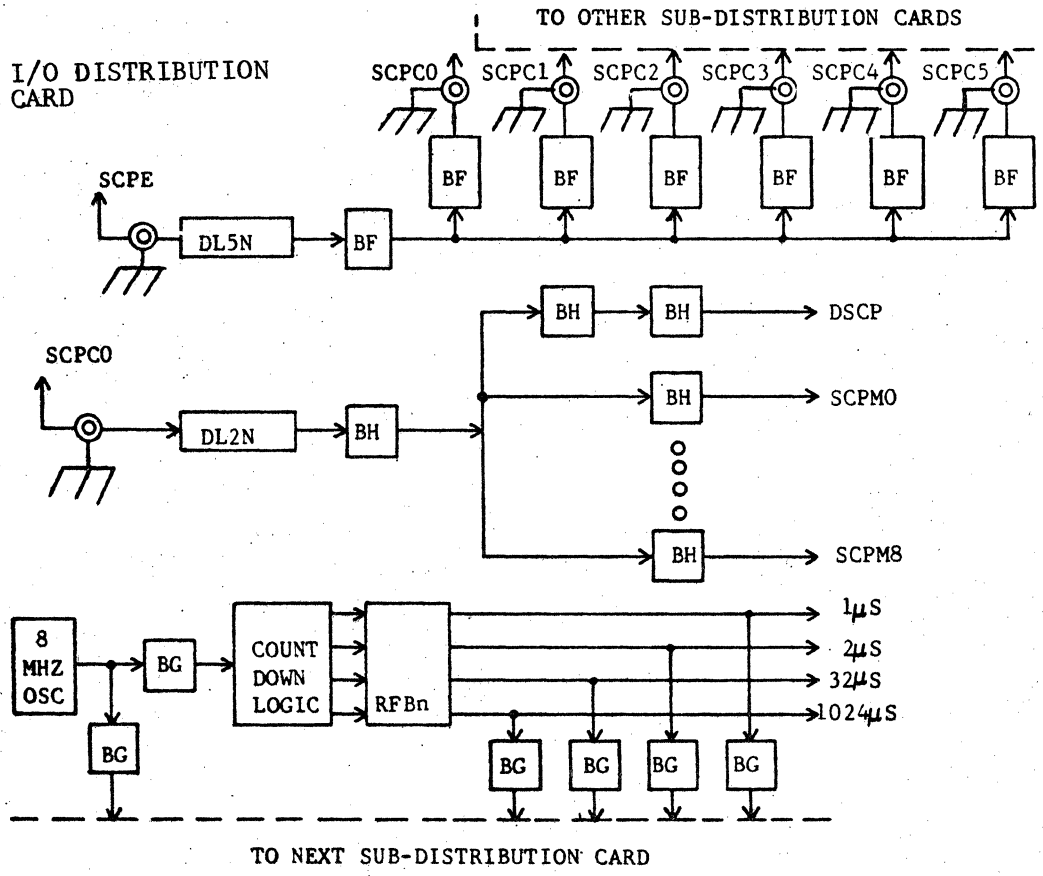


FIG. 2 I/O CLOCK DISTRIBUTION

6.3.3 For I/O controls that need slow clocks for timers etc., an 8 MHz crystal is stepped down through 3 bit registers to provide 1,4,32 and 1024 miscrosecond signals, each one system clock wide, and synchronized with the system clock by re-establishing through a 4 bit register. See Fig. 2.

6.3.4 These 4 slow clocks as well as the raw 8 MHz (asynchronous) clock are also buffered and sent to the next sub-distribution for use down the daisy chain. Each sub-distribution card re-establishes the 4 slow clocks through a 4 bit register before putting it on it's backplane.

6.3.5 See Figure 2 for the I/O clock distribution block diagram.

6.4 B1726 CLOCK MODULE.

6.4.1 B1726 Clock Module Oscillator Circuit. The 2200 8460 video amplifier is the feedback element that maintains oscillations of the crystal. Features of this video amplifier are internal input biasing, open collector current source output and an internal design such that the output limits symmetrically for either a positive or negative input overdrive. Internal biasing is such that no internal element is saturated due to input overdrive. Output impedance is constant over any part of the operational cycle.

6.4.2 The oscillator is connected as shown in Figure 3. At the start of operation, any noise generated by the video amplifier produces a voltage in R_1. A component of this noise is at the series resonance where the crystal looks purely resistive. This is feed-back to the input at R_2; since this is positive feedback, the amplitude quickly builds up to an equilibrium point where the video amplifier current source is either on or off.

6.4.3 The crystal at series resonance looks like a resistor (Fig. 3) and forms a divider network with R_2 such that a loop gain of about plus five is formed. At overtone, or spurious modes, the crystal series resistance is specified to be much higher so the resultant divider network with R_2 lowers the loop gain so much that oscillations cannot be maintained in these modes and therefore, the oscillator always oscillates at the fundamental frequency.

6.4.4 The capacitor C_1 is used to connect the negative end of R_2 to the ground end of R_1 at crystal frequencies. The other video amplifier output is the same as the output that drives R_1 except that it is out of phase with it. This inverted output drives R_3. The video amplifier output looks like a current switch of about 6.5 Ma nominal flowing to -12 volts or zero Ma. This current produces an approximately square wave signal of about 1.4 volts P-P at R_3. The 9819 is a

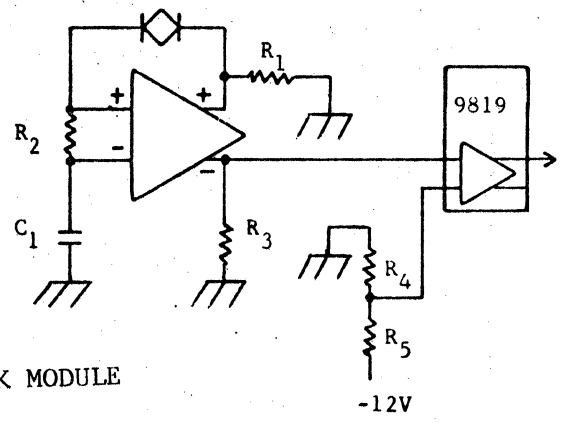


FIG. 3

B1726 CLOCK MODULE
OSCILLATOR

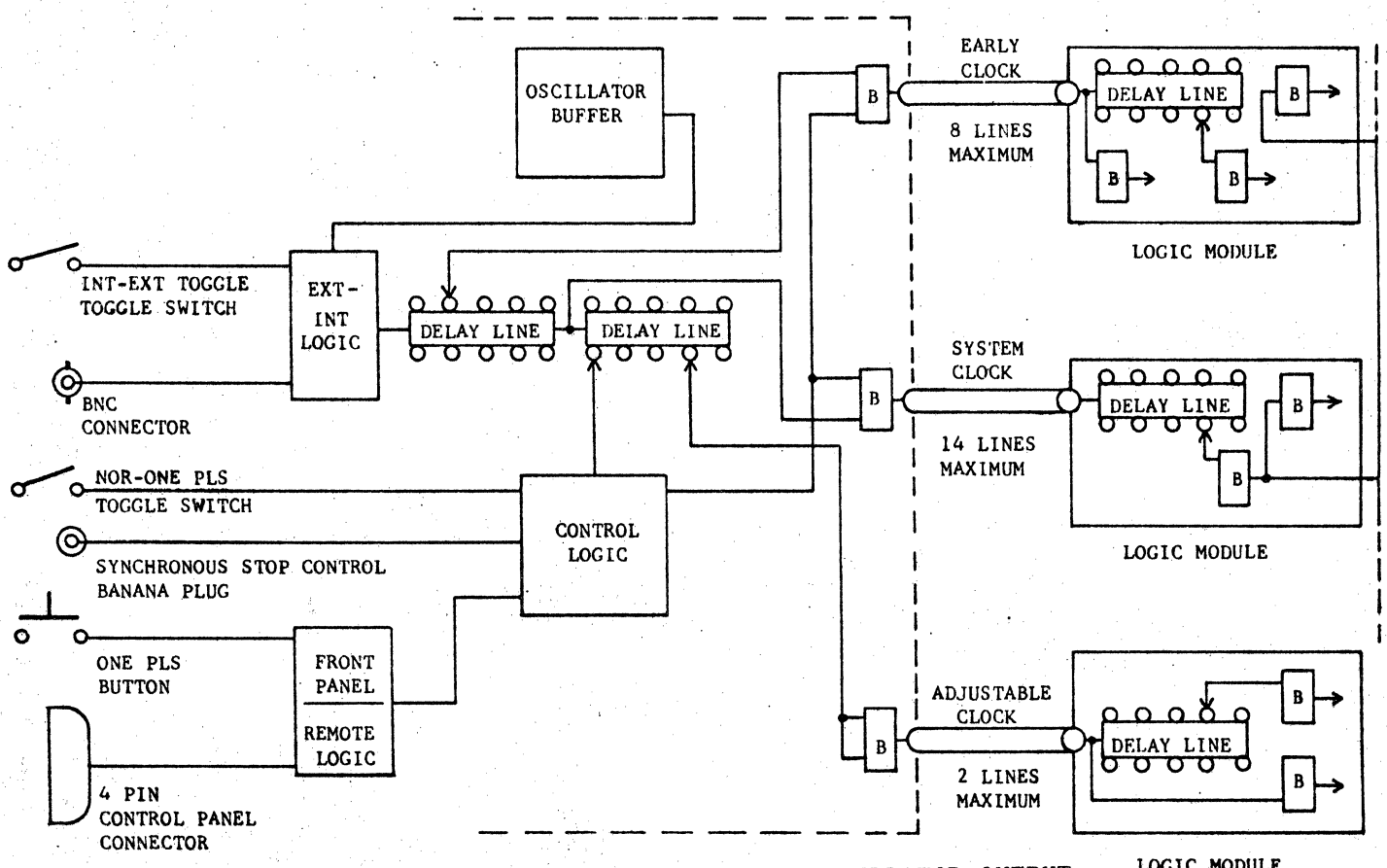


FIG. 4 OSCILLATOR OUTPUT TO BOARD OUTPUT

differential input, CTL output level translator.

6.4.5 Resistors R_4 and R_5 form a voltage divider that provides a DC reference voltage equal to the average voltage on the R_3 side of the 9819 and a symmetrical output results. (Fig. 3).

6.4.6 Since the video amplifier output current is a function of -12 voltage, the voltage at R_3 is a function of -12 voltage. The divider network R_4 and R_5 voltage is equally a function of -12 voltage so no symmetry change results due to changes in -12 power. Very small changes in symmetry result from V_{cc} and V_{ee} due to the 9819 design, but they can be neglected.

6.4.7 The oscillator is built on a small etched board and is completely shielded by the main board ground plane and a removable top cover. With shielding and the noise reduction design, the oscillator jitter problems are negligible compared to earlier clock oscillator designs.

6.5 OSCILLATOR OUTPUT TO BOARD OUTPUT. The flow path is straight forward and conventional through two 50NS delay lines as shown in Figure 4. The output of the first delay line is used to drive the system clock buffers. Taps on the first delay line produce a signal ahead of the system clock and are used to provide the early clock. Taps are provided at jumper chip location G3 to set early clock nominally 40NS ahead of the system clock referenced at coaxial connector outputs. Some taps on both the first and second delay line are fed to jumper chip at E3. When a jumper is placed from a pin to pin K, the adjustable clock output is energized. Taps are provided to adjust the adjustable clock from ahead of the system clock by 25NS to after the system clock by 35NS in nominal 5NS increments.

6.6 Control Logic. The INT - EXT toggle switch allows either the internal oscillator or the BNC connector to be the signal source for the clock card, Figure 4.

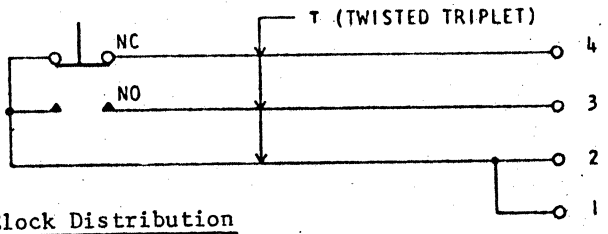
6.6.1 The NOR - ONE PLS toggle switch when placed in the ONE PLS position, synchronously stops the clock such that no clock pulses are "shaved", Figure 4.

6.6.2 The banana plug on the front panel also synchronously stops the clock when energized with a CTL true level.

6.6.3 Not all clocks are stoppable by the synchronous stop controls, and run continuously. Only Early Clocks, lines 5 through 8, and system clock lines 1 through 6 can be synchronously stoppped. The clock line functions are labeled on the front panel of the clock card.

6.6.4 When in the ONE PLS position, the push button is energized and a single pulse is produced for each push of the ONE PLS button. See Figure 4.

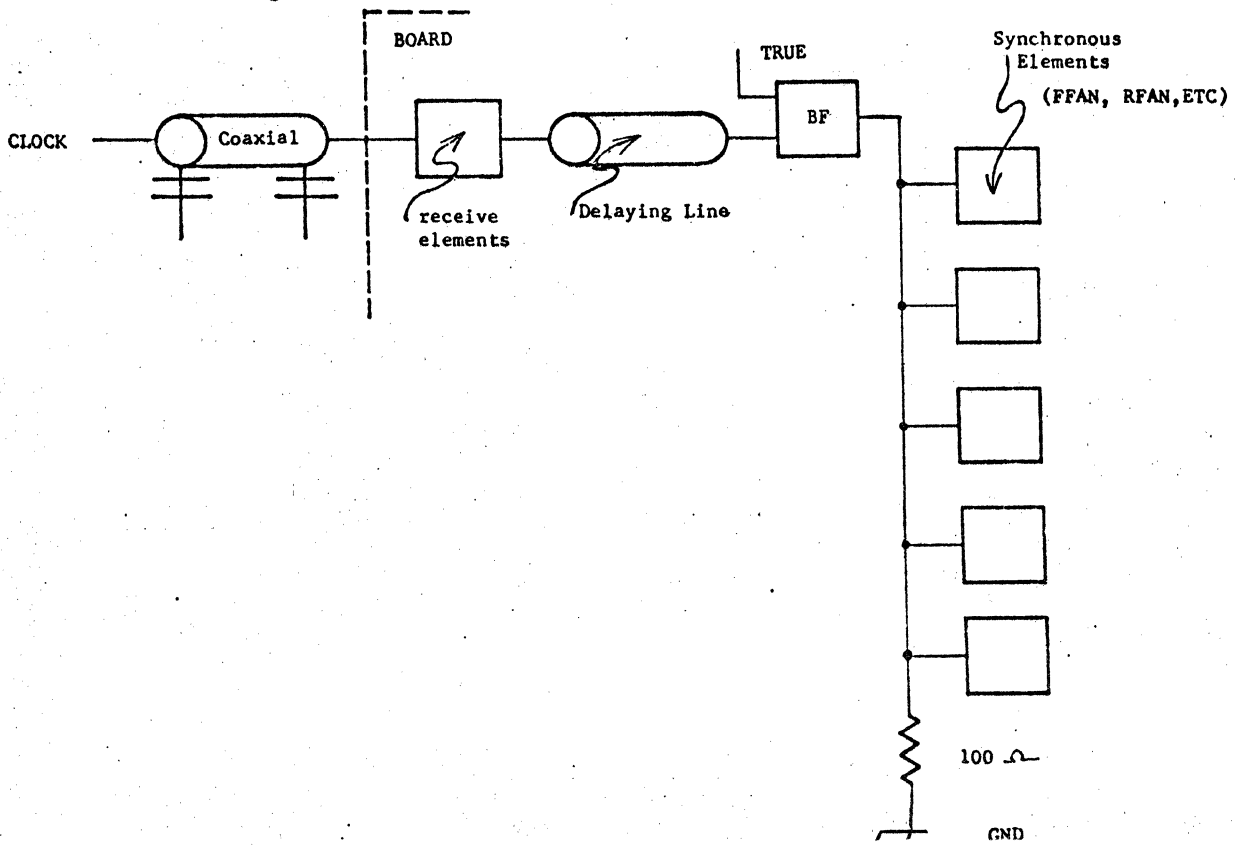
6.6.5 The 4 pin control panel connector can be used to connect a remote single pulse control on the clock. When pin 1 is connected to pin 2, the front panel button is disabled and the remote button can be connected as shown below, and in Figure 4.



6.7.0 Guideline for Clock Distribution

A. The clock which is distributed to any of the synchronous elements (FFAN, RFAN, RFBN, and LFAN) should be distributed without branching or T's and the element farthest away from the source should be terminated by a 100Ω resistor to ground. No gating of the clock signal should be allowed; thus, all unused inputs of the dual buffers in the clock distribution must be tied true.

B. This improves reflections on the distribution line, improves the fall times of the clock waveform and still allows fan out greater than 10. Also it prevents "shaved" clock pulses from being generated from gated clock buffers.



6.8 B1820 Clock Module.

6.8.1 The Oscillator. The B1820 clock scheme uses an encapsulated 12MHz TTL Crystal oscillator as the primary source. This is divided by a CTL flip-flop to provide the primary system clock frequency of 6MHz. The division process assures symmetry.

6.8.2 The Distribution Scheme. See Figure 6. The logical OR of the Single Pulse output, the External Clock and the main clock is sent to four BG-N buffers which in turn drive the calibration and reference delay lines. The first buffer supplies an I/O Clock to the backplane which is received by the I/O Distribution Card and conditioned as needed before distribution to the I/O controls. The second network supplies 6 clocks by means of coax for use in the MBU, port interchange and other such activities requiring clock signals. The third net provides two backplane clocks for use by the processor. The fourth net provides an MBU coax clock that can not be stopped by the Stop Input.

6.8.3 The Calibration Circuitry. Each of the four buffers mentioned previously drives a calibration section composed of one or more delay lines and a corresponding JPRN header chip used to select the appropriate tap on the delay line. The appropriate tap is determined by the timing requirements of the section being clocked. A reference tap is provided for aligning all clocks.

An additional calibration circuit is provided for the backplane clocks that drive the processor. The purpose of this circuitry is to control positive pulse width to within 2nS of the nominal 83nS.

6.8.4 The Control Circuitry. Four controls are provided on the front of the module. The first is a push button used to emit single pulses when the second control switch (Single Pulse or Continuous Operation) is in the Single Pulse mode. The third switch selects the source of oscillation (external or internal). This switch is not present on units in the field and must be added if needed. The fourth controls the syncronous stop feature which can be activated by a pulse being applied at the frontplane or backplane Stop inputs. A doghouse is also provided to bring the External Clock signal on card. As was the case with the control switch, this dog house is not on field units and must be added if needed.

.5 The Receiving Circuitry. See Figure 5. All processor cards that receive the backplane clocks do so with a BG-N in position F9. This buffer in turn drives a delay line which can go to other buffers or no load gates for distribution on the card. The on card nets are limited to 24", and 12 active DC loads to control on card skew.

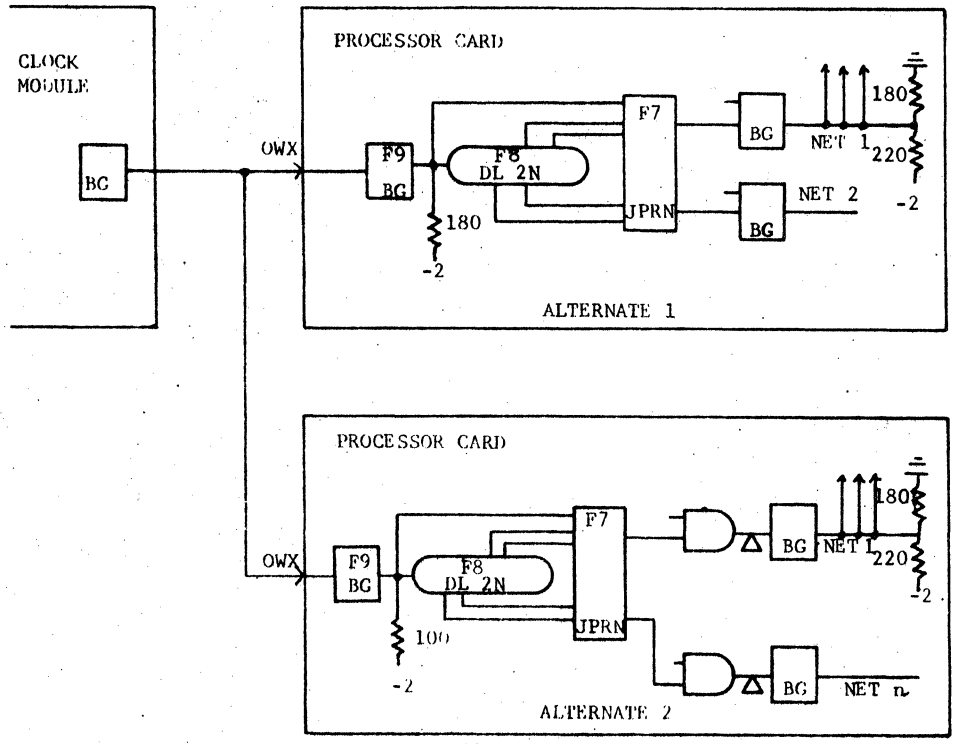


Figure 5 CLOCK RECEIVING CIRCUITRY

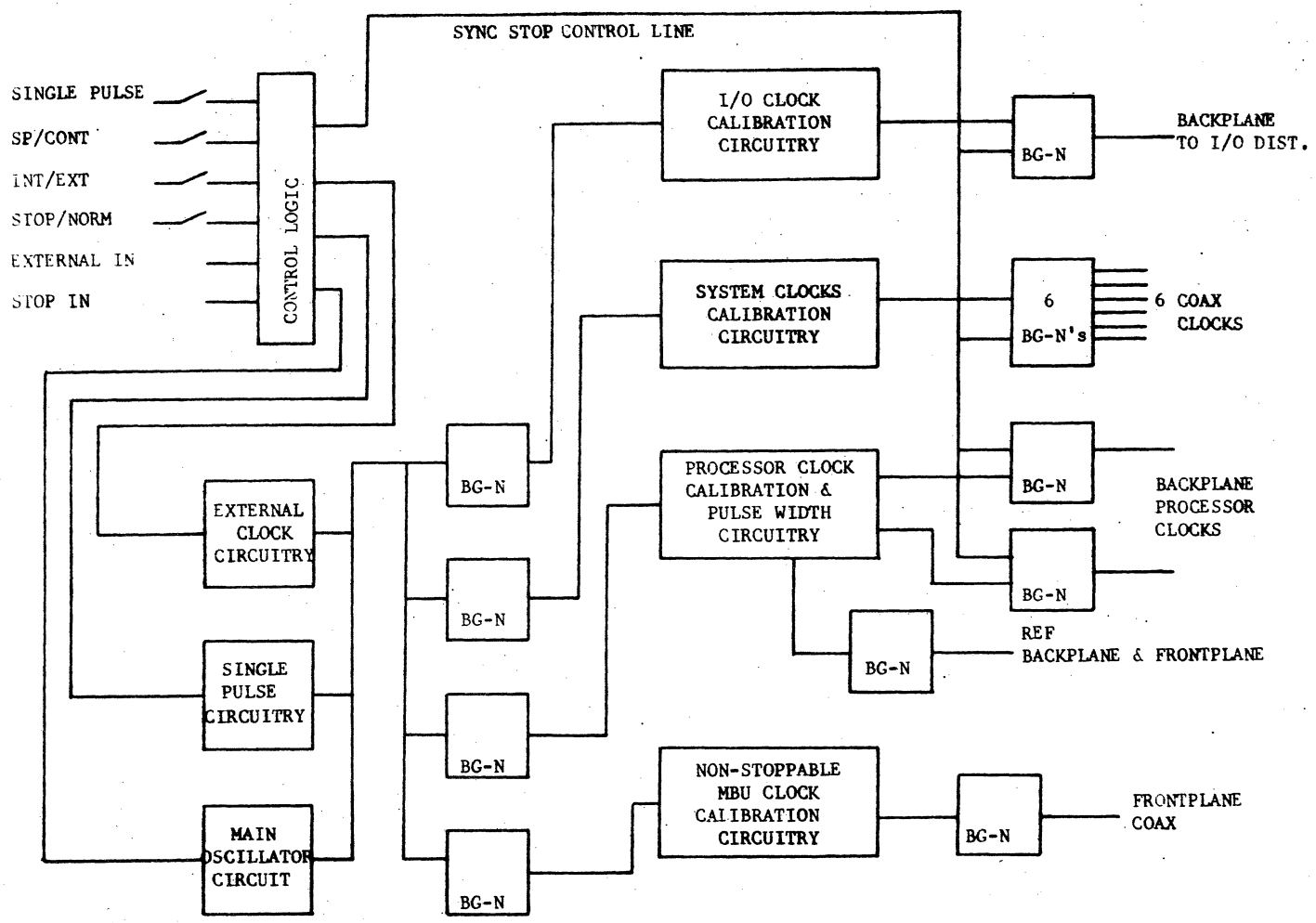


FIGURE 6 1820 CLOCK DISTRIBUTION

7.0 DATA TRANSMISSION RULES

7.1 Cable Rules

7.1.1 D.C. Considerations :

Two factors which influence the rules most severely are D.C. resistance of the line and the termination resistance. D.C. resistance and mismatched termination resistance both reduce output amplitude at the end of the line.

The voltage drop due to D.C. resistance is proportional to the length of the line and inversely proportional to the wire diameter. Under true level worst case conditions a 26 gauge coax will have 16 mv drop at the end of a 10 ft. line which is terminating with 100 ohm to -0.5 volt.

A mismatch between the termination resistance (R_L) and the characteristics impedance (Z_L) of that line will cause an increase or decrease in the voltage at the end of the line. This increase or decrease is a function of the reflection coefficient φ .

$$\varphi = \frac{R_L - Z_L}{R_L + Z_L}$$

The increase or decrease in signal amplitude due to mismatch will be temporary in nature, however, its effect must be considered as a D.C. problem as the shift in voltage lasts considerably longer than the switching time of the circuitry. The shift in voltage will not be significant after twice the transit time of the cable. Under worst case conditions for a coax cable this mismatch could cause a 75 millivolt shift and a 150 millivolt shift for ribbon lines.

7.1.2 Termination Considerations :

A line should always be terminated into its characteristic impedance. The 96 $^{+4}_{-6}$ ohm coaxial line should always be terminated with a 95.3 ohm resistor or proper delay line. The ribbon lines have a nominal impedance of 100 $\pm$ 10 ohms and should be terminated with a 100 ohm resistor.

Lines driven from only a single source at the near end of the line need only be terminated at the far end of the line.

Multiple source lines must be terminated at both ends of the line.

7.1.3 A.C. Considerations :

There will be short term transients on the information due to poor grounding, stray inductance and stray capacitance. These factors should not cause significant problems provided the construction techniques presently contemplated are used. If new construction techniques are used then they must be evaluated for these factors.

Cross talk is not a problem in the case of coax cables, but it is a significant problem in ribbon cables. Cross talk in the ribbon cable can have magnitudes as high as 0.2 volts and a duration of twice the transit time of the cable provided a ground line is between every signal line in the cable. If no ground line is between signal lines, cross talk will be greater.

7.2 Driver/Receiver

7.2.1 Line Driver

The dual buffer or dual inverter (BG-N and IF-N) is used to drive terminated lines; normally a network of 121 ohms to ground and 511 ohms to V_{ee} is used to terminate the line. This network is normally placed at the receiver end of a one way line, and at both ends of a two way or "Party" Line. Each network is equal to 11 CTL loads.

7.2.2 Line Receiver

Any CTL restoring element can be used as a line receiver. The termination network should be placed as close to the receiver as possible. By placing the termination near the receiver, crosstalk problems are minimal.

8.0 TIMING RULES

8.1 Delay Line Rules

Delay lines are always terminated into their characteristic impedance. The delay line is always driven by a CTL buffer or another delay line. When being driven by a buffer, the output of the buffer must have a 178 ohm ½ Watt pull-down resistor connected from its output to the -2 volt bus and the delay line output must have a terminating resistor equal to the delay line characteristic impedance connected to ground. The terminating impedance can be obtained by internal connection, jumpering Pin N to Pin P.

Delay lines may be cascaded to obtain longer time delays. Only the last delay line in the cascaded group is to be terminated. The first delay line of the group is driven the same as a single delay line. Due to signal loss and decay of rise and fall times, the maximum delay should be limited to less than 150 ns. Rise and fall times are approximately degraded by the root of the sum of the squares formula (RSS Rule). The taps along the delay line must not be heavily loaded. A maximum of two buffers and up to 4 no load gates or 6 no load gates and no buffers can be connected to any delay line. The no load gate outputs must be restored to become fully compatible CTL logic. The far end of the delay line is the only place that is to be terminated. Under no circumstance is a tap to be terminated or used to drive another delay line.

8.2 MULTI TIMING RULES

The purpose of these rules is to normalize the use of TAOn retriggerable one-shot as an asynchronous/synchronous timer.

OUTPUT - Pin H gives a false output ($\leq$0.45V) during the quiescent time, and a true output ($\geq$1.50 volts) during the timing period. Pin F gives the complement of this function.

RANGE AND TOLERANCES - The nominal timing periods ranges from 1 microsecond to 2 seconds. The tolerances depends on the variations of the total external resistance, and of some internal parameters of the capacitor used. Particularly, the variation in capacitance and leakage current of the capacitor as a function of temperature. For further information in regard to tolerances and other possible ranges of application, consult the Circuit Design Group.

TRIGGERING CONDITIONS - At least one of the inputs A and B must be held false, and both of the input pins C and D must be held true to trigger package.

Retriggerable operation - Each time the output of the internal logic circuit goes true, the external capacitor is discharged and a new cycle is started. Retriggering will not occur if the retrigger pulse comes within 0.224 C_x (pf) ns after the initial trigger pulse. To trigger the TAOn use all inputs of the same input gate, i.e., A & B or C & D, according to the selected triggering mode. Whenever negative triggering is used, tie pins C and D to V_{cc}, either directly or through a 500 ohms resistance. Up to 20 TTL unused inputs can be tied to the same resistor. If positive triggering is employed, ground pins A and B. Fig. 8.1 shows the two recommended connections of the input gating.

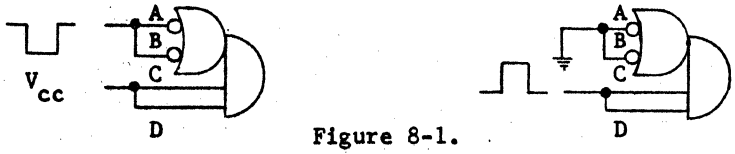


Figure 8-1.

Non-retriggerable operation - In situations where non-retriggerable operation is required, and the TAOn is negatively triggered, tie the complementary output (pin F) back to one active level low input (pin A or B). Use the other pin for triggering. (See Fig. 8-2) If the TAOn is positively triggered retriggering may be inhibited by tying pin F back to one active level high input (C or D) and using the other pin for triggering.

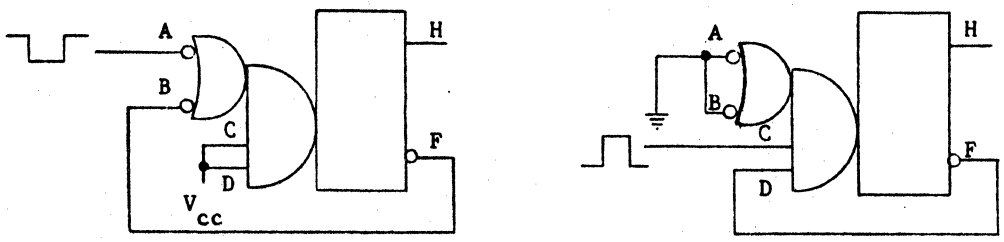


Figure 8-2.

8.2.1 TIMING COMPONENTS

A timing capacitor connected between pin N and L, two resistors, one fixed and one adjustable, connected as indicated in Fig. 8-3, are required. A trimming resistor is used to compensate for production tolerances in the IC itself (± 10%), capacitor, and resistors, plus any error due to the inaccuracy of the formula employed to compute the timing period.

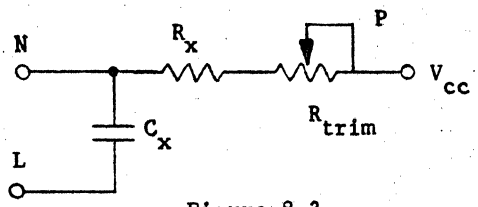


Figure 8-3.

R_x must be equal or greater than 5K, while the total resistance, $R_x + R_{trim}$, should not exceed 50 K under any circumstances. When electrolytic-type capacitors are to be used, the total resistance must not exceed 30 K, in order to maintain the ratio of the charging current to the leakage current much higher than one.

8.2.4 Applications

8.2.4.1 Retriggerable Asynchronous Timer

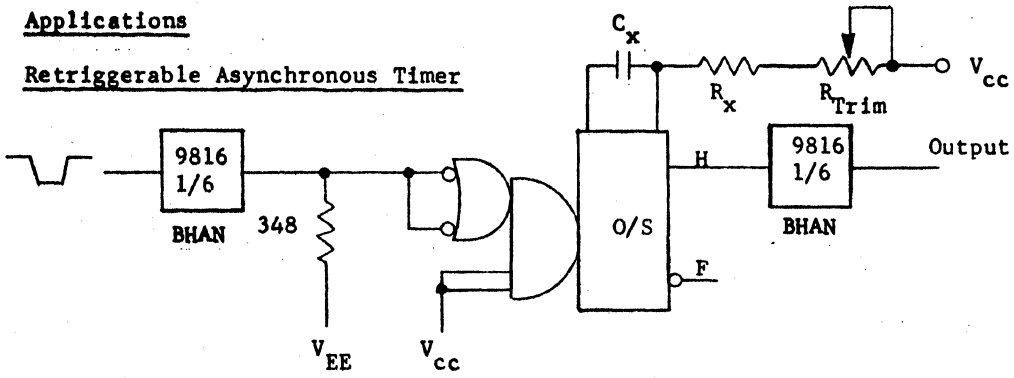


Fig. 8-6. RETRIGGERABLE ASYNCHRONOUS TIMER CIRCUIT

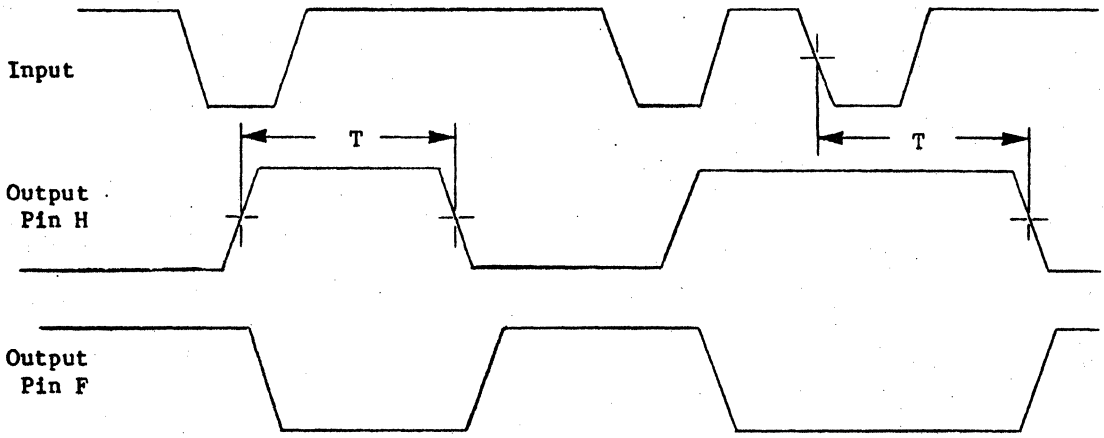


Fig. 8-7. TYPICAL WAVEFORMS FOR THE ASYNCHRONOUS TIMER

8.2.4.2 Synchronous Timer - The leading and trailing edge of the output pulse are synchronized with the trailing edge of the pulse clock. The circuit may be retriggered immediately after the conclusion of a timing cycle. The input signal must go true 15 nsec. prior to the trailing edge of the clock. Its pulse width may be of any duration. If the input pulse is longer than the output pulse plus 1 clock period, the circuit will retrigger and initiate a new timing cycle. (See Figures 8-8 and 8-9)

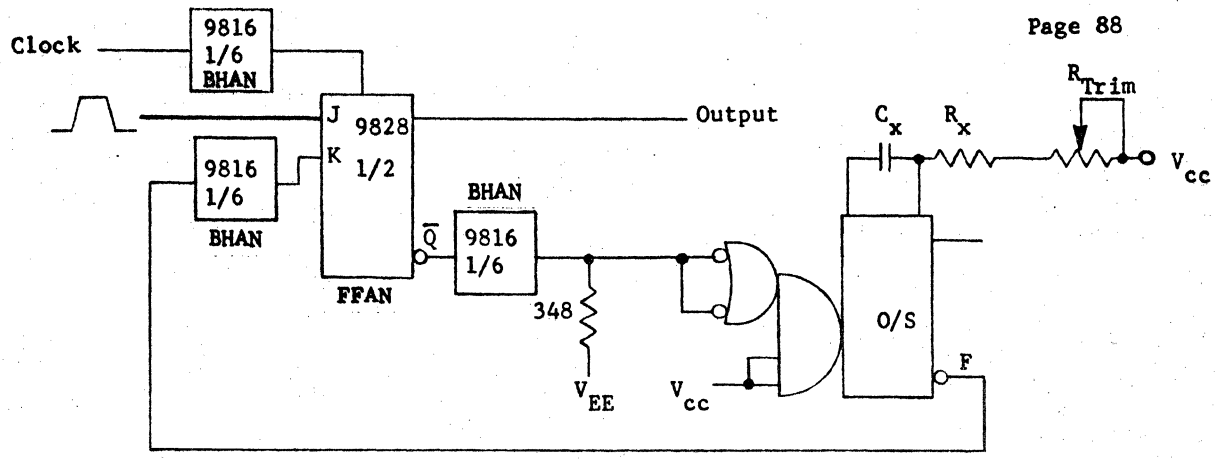


Fig. 8-8. SYNCHRONOUS TIMER

For high values of capacitance, solid tantalum capacitors (Sprague-type 150 D) with a working voltage WVDC = 15V, must be used. They can tolerate five percent of the rated voltage in the reverse direction at 85° C.

For selection of timing components consult the Standard Circuits Section, Dept. 6480.

All external timing components must be mounted as close as practicable to the circuit in order to minimize stray capacitance and reduce noise pickup.

8.2.2 PULSE WIDTH COMPUTATION

For $C_x \geq 1000$ pf, the output pulse width is approximated by $T = .320\ C_x\ (R+0.7)$

Where R is the total timing resistance in Kilohms.

C_x is in pF

T is in nsec.

For pulse widths less than 500 nsec, the propagation delay should be added to the value given by (1)

The retrigger pulse width is calculated as shown in Fig. 8-4.

Minimum output pulse width: 65 nsec.

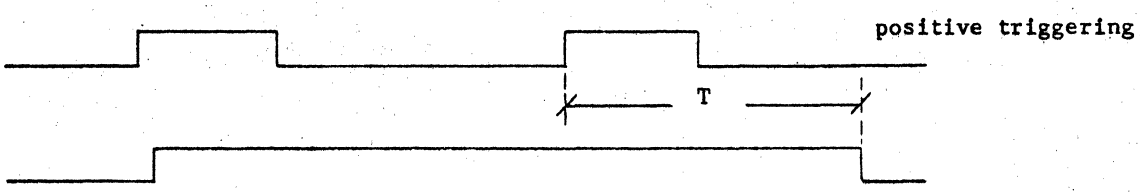


Figure 8-4.

8.2.3 INPUT TRIGGER PULSE

Minimum input pulse width: $(T_i)_{min}$ = 40 ns (see Fig. 8-5)

Trigger input delay: $T_{pd+} \leq 50$ ns

$T_{pd-} \leq 50$ ns

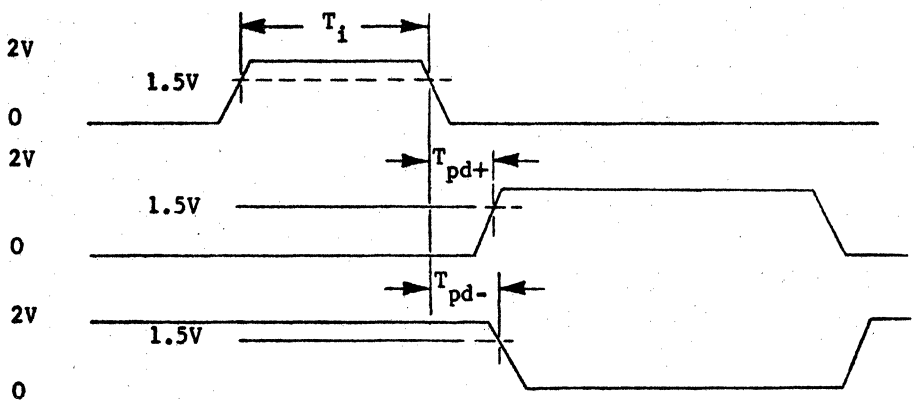


Figure 8-5

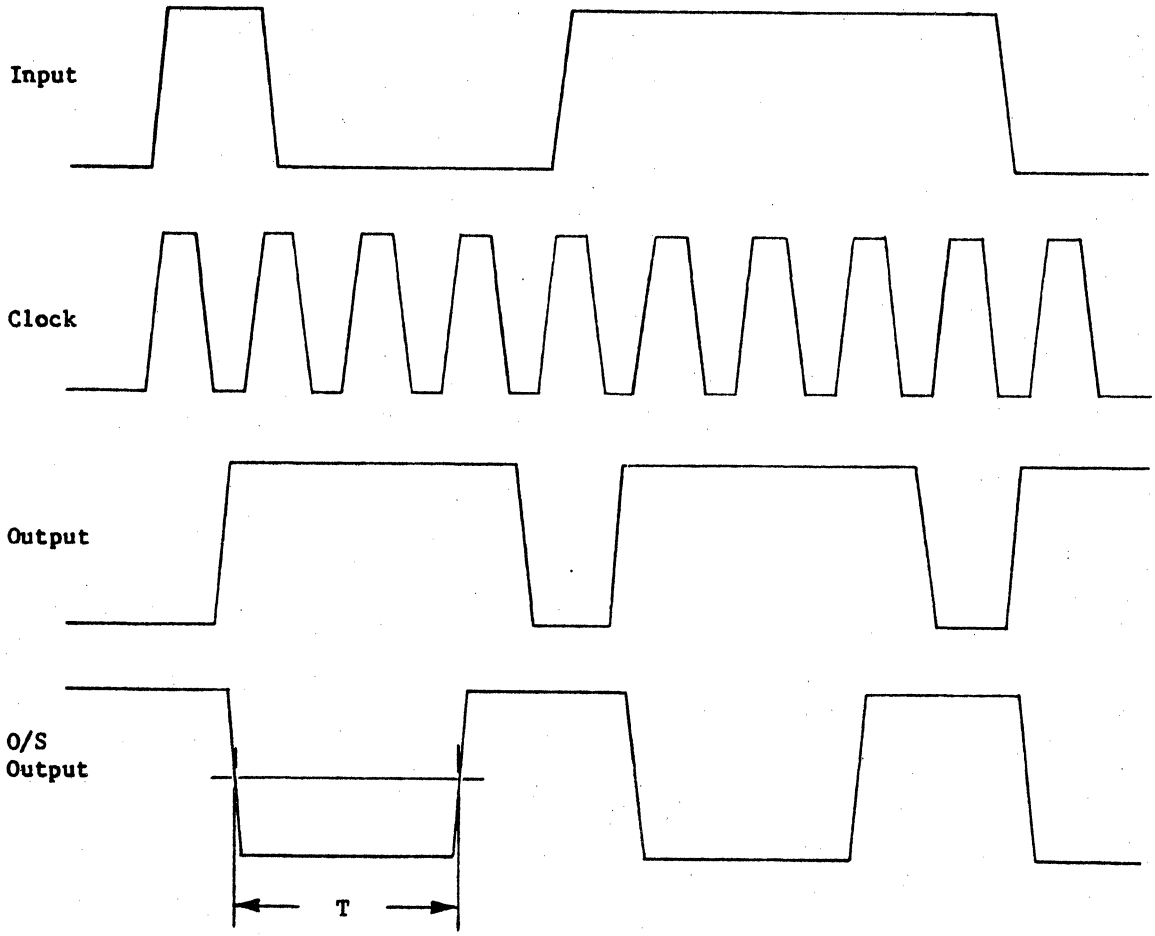


Fig. 8-9. SYNCHRONIZED MULTI WAVEFORMS

11.0 POWER SUPPLY CALCULATIONS

Tables 11-1 and 11-2 give the worst-case figures corresponding to the supply currents for the CTL and TTL integrated circuits, according to the following terminology:

I_{CC}: Current drawn from V_{CC} supply (+4.75 V nominal)

I_{EE}: Current to V_{EE} supply (-2.0 V nominal)

I_{GND}: Current to ground

I_{11}: Current to V_{11} supply (-12.0 V nominal)

I_{22}: Current drawn from V_{22} supply (+12.0 V nominal.)

The information given in these tables is based on the data available at the present time and will be subject to change as new data becomes available.

11.1 Current Calculations

Supply currents do not include in most cases the effect of loads.

Total currents for each chip can be calculated as follows:

a) CTL Chips

$$I'_{CC(1)} = I_{CC(Table)} + 3\ mA \times N_L{}^*$$

$$I'_{EE(1)} = I_{EE(Table)}$$

$$I''_{GND(1)} = I_{GND(Table)}$$

b) TTL Chips

$$I'_{CC(2)} = I_{CC(Table)}$$

$$I'_{GND(2)} = I_{GND(Table)}$$

or

$$I''_{CC(2)} = I_{GND(Table)}$$

The last value includes the current drawn from the V_{CC} supply by the external pull-up load resistors.

---

*N_L = Total No. of loads to the chip output. It includes CTL inputs and discrete resistors, on the same card or off-card, expressed in terms of CTL loads.

In all the above stated equations, primed (') terms refer to the total current per chip. Double primed (") terms refer to the sum of the chip current plus the current drawn by the external associated resistors.

The term N_L is the total output load to the chip, both CTL inputs or discrete pull-down resistors to V_{EE}, on the same card or off-card, expressed in terms of CTL loads.

The current to the V_{EE} supply due to discrete pull-down resistors may be computed as follows:

$$I_{EE(3)} = 3 \text{ mA} \times N_{LR}$$

Where N_{LR} is the number of discrete pull-down resistors on the card expressed in terms of CTL loads.

The total current values per card may be calculated as follows:

$$I_{CC(T)} = \sum (I'_{CC(1)} + I''_{CC(2)})$$
$$I_{EE(T)} = \sum (I'_{EE(1)} + I_{EE(3)})$$
$$I_{GND(T)} = \sum (I'_{GND(1)} + I'_{GND\ (2)})$$
$$I_{11(T)} = \sum (I'_{II(3)})$$

11.2 Power Dissipation Calculations

The power dissipation for each chip can be calculated as follows:

a) CTL Chips

$$P'_{d(1)}(\text{mW}) = 5.0 \times I_{CC(\text{Table})} + 2.1 \times I_{EE(\text{Table})} + 12.5 \text{ mW} \times N_i + 7.5 \text{ mW} \times N_L$$

Where N_i is the number of inputs that the chip has.

b) TTL Chips

$$P'_{d(2)}(\text{mW}) = 5.0 \times I_{CC(\text{Table})}$$

or

$$P''_{d(2)}(\text{mW}) = 5.0 \times I_{GND(\text{Table})}$$

The last value includes the power dissipated in the external pull-up load resistors.

In all the above stated equations, primed (') terms refer to the total dissipation per chip. Double primed (") terms refer to the power dissipated in the chip itself plus the additional power dissipated in the external discrete resistors associated with the chip.

The term N_L has the same meaning as in Sec. 11.1.

The term N_i represents the number of inputs that the chip has.

The power dissipation in discrete pull-down resistors may be computed as follows:

$$P_{d(3)} = 15 \text{ mW} \times N_{LR}$$

Where N_{LR} has the same meaning as in Sec. 11.1

The total dissipation per card may be calculated as follows:

$$P_{d(T)}(\text{mW}) = \sum (P'_{d(1)} + P''_{d(2)} + P_{d(3)})$$

TABLE 11-1-MAXIMUM SUPPLY CURRENTS-CTL INTEGRATED CIRCUITS

Element Type	Assembly Number	Description	Maximum Currents (mA)*					Remarks
			I_{CC}	I_{EE}	I_{GND}	I_{11}	I_{22}	
AFAn	1904 0179	Dual Adder/Subtractor	114	87	50	--	--	
AMCn	1123 9134	8-Bit Memory	50	--	60	--	--	
BG-n	1705 7563	Dual Buffer (2,2)	45	60	7	--	--	Pull-down resistors not connected
BHAn	1904 0245	Hex Restorer	80	80	20	--	--	
CFAn	1904 0195	4-Bit Comparator	92	110	60	--	--	
CFBn	1909 0513	Carry Logic Gate	105	75	2	--	--	
DFAn	1904 0161	1 of 8 Decoder	115	106	35	--	--	
EFAn	1914 0748	Priority Encoder	105	96	20	--	--	

* Supply currents do not include the effect of loads, unless the contrary is stated.

TABLE 11-1 MAXIMUM SUPPLY CURRENTS-ECL INTEGRATED CIRCUITS (Continued)

Element Type	Assembly Number	Description	Maximum Currents (mA)*					Remarks
			I_{CC}	I_{EE}	I_{GND}	I_{11}	I_{22}	
FFAn	1779 6137	Dual JK/D Flip-Flop	125	130	50	--	--	--
GFBn	1916 5851	Dual AND Gate (4,4)	15	36	2	--	--	--
GFEn	1916 5133	Quad Gates (1,1,1,1)	30	37	2	--	--	--
GFFn	1916 5794	Quad AND, AND/OR Gates (2,2,2+2)	30	47	2	--	--	--
GFIn	1911 9098	Triple AND Gates (4,3,3)	22	48	2	--	--	--
GFJn	1911 9106	Quad AND Gates (3,2,2,2)	30	50	2	--	--	--
GFKn	1918 4282	Quad AND Gates (3,2,2,2)	28	28	2	--	--	No load Gates
IF-n	1705 7480	Dual Inverter (2,2)	30	30	15	--	--	Pull-down resistors not connected
IHAn	1904 0252	Hex Inverter	71	53	35	--	--	
LFAn	1779 6145	Quad Latch	82	98	7	--	--	--
MFAn	1904 0187	8-Input Multiplexer	151	146	25	--	--	--
MOPn	1916 6115	Micro-Operator	50	45	7	--	--	--
RFAn	2201 4096	3-Bit Register	160	65		--	--	--
RFBn	2201 4062	4-Bit Register	115	60		--	--	--
RFZN	1779 6152	3-Bit Register	160	65		--	--	--
RF-N	1779 6160	4-Bit Register	115	60		--	--	--

* Supply currents do not include the effect of loads, unless the contrary is stated.

Table 11-2: MAXIMUM SUPPLY CURRENTS TTL

TYPE	Assembly Number	Description	Maximum Currents (mA) Icc	Ignd
MI1N	1918 3599	EBCDIC/ASCII Code Conv. (MSB)	130	195
MI2N	1918 3607	EBCDIC/ASCII Code Conv. (LSB)		
MI3N	1918 3615	ASCII/EBCDIC Code Conv. (MSB)		
MI4N	1918 3623	ASCII/EBCDIC Code Conv. (LSB)		
MH1N	2201 4146	HOLLERITH/EBCDIC Code Conv. (LSB)		
MH2N	2201 4153	HOLLERITH/EBCDIC Code Conv. (MSB)		
MH3N	2201 4146	EBCDIC/HOLLERITH Code Conv. (LSB)		
MH4N	2201 4179	EBCDIC/HOLLERITH Code Conv. (MSB)		
MJ1N	2204 4200	96 COL CODE/EBCDIC Code Conv. (LSB)		
MJ2N	2204 4218	96 COL CODE/EBCDIC Code Conv. (MSB)		
MJ3N	2204 4226	EBCDIC/96 COL CODE Code Conv. (LSB)		
MJ4N	2204 4234	EBCDIC/96 COL CODE Code Conv. (MSB)		
MK1N	2204 5124	EBCDIC/BCL + PAR Code Conv. (LSB)		
MK2N	2204 5132	EBCDIC/BCL + PAR Code Conv. (MSB)		
RM1N	2208 0014	EBCDIC/KATAKANA Code Conv. (LSB)		
RM2N	2208 0022	EBCDIC/KATAKANA Code Conv. (MSB)		
MF4N	1918 3516	EBCDIC/BCL 1/4 Code Conv.	80	160
MF5N	1918 3524	EBCDIC/BCL 2/4 Code Conv.		
MF6N	1918 3532	EBCDIC/BCL 3/4 Code Conv.		
MF7N	1918 3540	EBCDIC/BCL 4/4 Code Conv.		
MF8N	1918 3557	BCL/EBCDIC 1/2 Code Conv.		
MF9N	1918 3565	BCL/EBCDIC 2/2 Code Conv.		

Table 11-2: MAXIMUM SUPPLY CURRENTS TTL (Continued)

TYPE	Assembly Number	Description	Maximum Currents (mA) Icc	Ignd
RFCN	2205 2609	64 Bit RAM	105	165
RFDN	2206 1626	256 Bit RAM	135	150
TAON	1901 7102	MONOSTABLE MULTI VIBRATOR	25	35
IHCN	1471 4356	DTL HEX INVERTER	20	110
IHDN	1674 4963	TTL HEX INVERTER	42	82
IDCN	1471 4398	DTL 2 x 4 BUFFER	25	97
RW06	1449 1104	1024 BIT RAM	160	176
P001	1447 9455	256 x 4 PROM	120	184
PR08	2607 6075	32 x 8 PROM	130	258
S2-N	1447 3797	QUAD 2-IN MUX	48	112
S4-N	1447 3714	QUAL 4-IN MUX	60	124
PR4N	2319 5274	256 x 4 PROM	130	194
PR5N	2319 5282	512 x 4 PROM	130	194
T3AH	1447 3557	TRIPLE 3-IN AND	48	120
T2HN	1479 0240	QUAD 2-IN NAND	40	136
BTSN	1948 5051	TRI-STATE HEX BUFFER	85	313
CR4N	1447 3771	4 BIT BINARY COUNTER	101	181
RW13	2540 0656	1024 BIT RAM	160	176
B2CN	1447 3581	OPEN COLLECTOR BUFFER	54	246

Table 11-2: MAXIMUM SUPPLY CURRENTS TTL (Continued)

TYPE	Assembly Number	Description	Maximum Currents (mA) Icc	Ignd
B2TS	2602 7300	QUAD TRI-STATE BUFFER	62	126
ITSN	1948 5069	TRI-STATE HEX INVERTER	77	269
CRCN	1269 7561	CRC GENERATOR/CHECKER	90	98
SCTL	1959 5727	SYSTEM CONTROLLER	190	320

LOGIC POWER SUPPLY

The logic power supply is a compact, low voltage, high current supply. It provides:

+ 4.75 VDC ± .5V
- 2.00 VDC ± .5V
+12.00 VDC ± .5V
-12.00 VDC ± .5V

MEMORY POWER SUPPLY

The memory supply provides the following voltages:

+19.00 VDC ± 1V
- 5.00 VDC ± 1V
+23.00 VDC ± 1V * See explanation below

* The +23 volt supply is a +4 volt supply floating on the +19 volt supply.

Refer to the Field Engineering Manual for information on adjustment, troubleshooting and maintenance.

The system margins given in this section are not intended for use in the field but rather are given as an aid to in-plant engineering personnel. Furthermore, they are not intended to hold true under 'extended' conditions.

SYSTEM MARGINS

B1714

VOLTAGE	NOMINAL SETTING	MARGIN HIGH	MARGIN LOW
+ 4.75	+ 4.85 ± .01	+ 5.0	+ 4.6
- 2.00	- 2.05 ± .01	- 2.1	- 1.95
+12.00	+12.00 ± .10	+12.5	+11.5
-12.00	-12.00 ± .10	-12.5	-11.5
+20.00	+19.00 ± .10	+18.5	+19.5
+23.00	+ 4.00 ± .01 diff	+ 3.75 diff	+ 4.25 diff
- 5.00	- 5.00 ± .01	- 5.10	- 4.90

B1726

VOLTAGE	NOMINAL SETTING	MARGIN HIGH	MARGIN LOW
+ 4.75	+ 4.85 ± .01	+ 5.05	+ 4.65
- 2.00	- 2.08 ± .01	- 2.15	- 2.02
+12.00	+12.00 ± .10	+12.5	+11.5
-12.00	-12.00 ± .10	-12.5	-11.5
+20.00	+19.00 ± .10	+19.5	+18.5
+23.00	+ 4.00 ± .01 *	+ 4.25 *	+ 3.75 *
- 5.00	- 5.00 ± .01	- 5.10	- 4.90

B1820

VOLTAGE	NOMINAL SETTING	MARGIN HIGH	MARGIN LOW
+ 4.75	+4.95 ± .01	+5.15	+4.75
-2.00	-2.15 ± .01	-2.25	-2.05
+12.00	+12.00 ± .10	+12.50	+11.50
-12.00	-12.00 ± .10	-12.50	+11.50
+20.00	+19.00 ± .10	+19.50	+18.50
+23.00	+ 4.00 ± .01 *	+ 4.25*	+ 3.75 *
-5.00	-5.00 ± .01	-5.10	-4.90

* These figures stand for differential voltages on top of the " +20V " voltage.

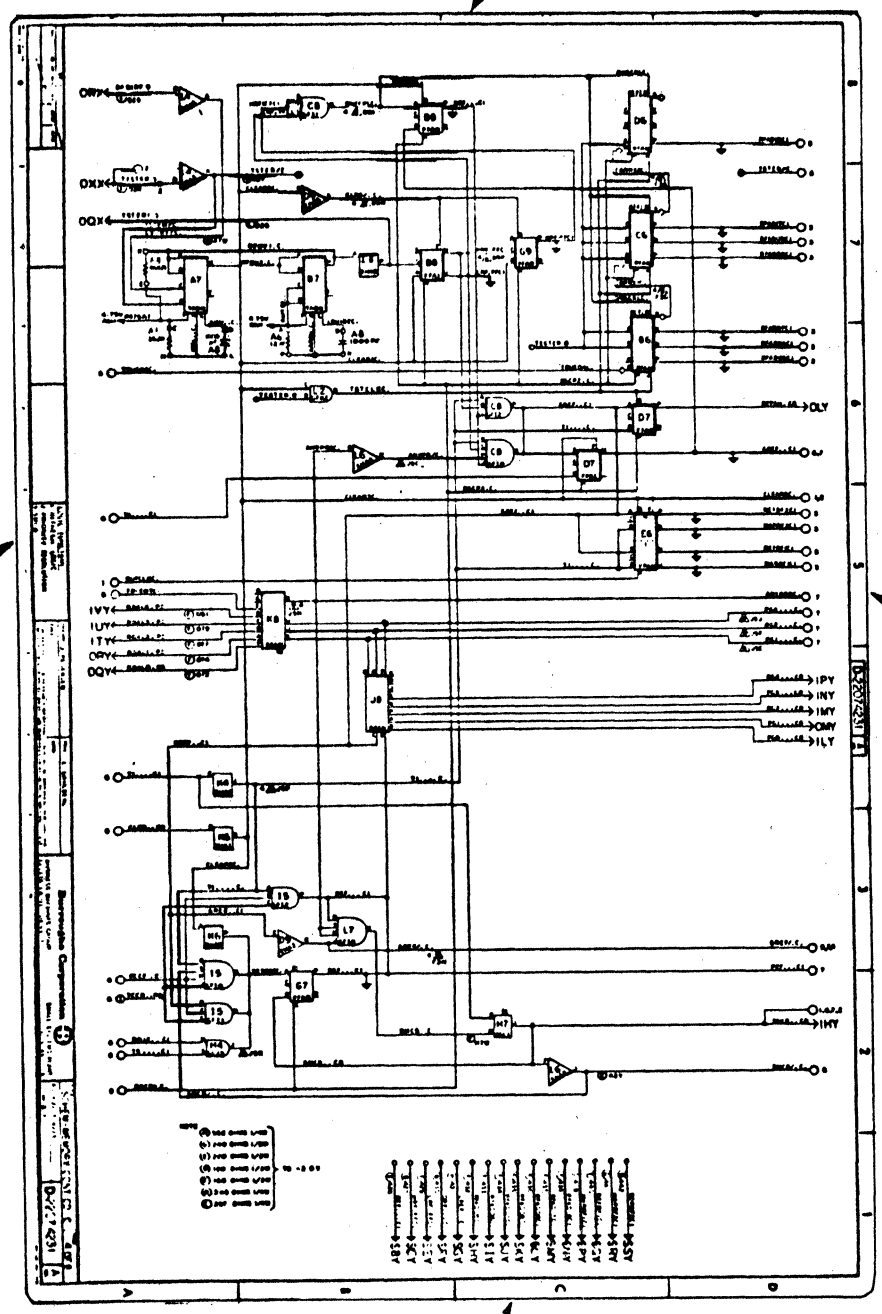
Appendix on Logic Schematic Symbols

Frontplane inputs (connectors) at the top of the schematic only.

Top of schematic for Zoning purposes.

Backplane Inputs (connectors) at the left of the schematic only.

Backplane Outputs (connectors) at the right of the schematic only.



Left side of schematic for Zoning purposes.

Right side of schematic for Zoning purposes.

Frontplane outputs (connectors) at the bottom of the schematic only.

Bottom of schematic for Zoning purposes.

The schematic is read with the title block turned to the left, as shown above. Logic flow is left-to-right whenever possible.

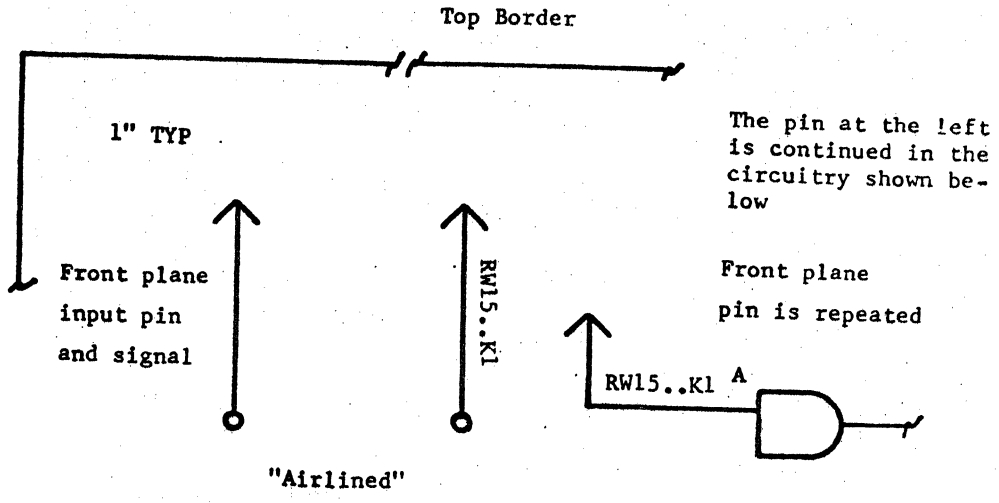
Signal names consist of 8 characters. The last character of the mnemonic name is a (0), (1) or (.). The use of these characters are defined as follows:

0 Signal entering or leaving Backplane connector.

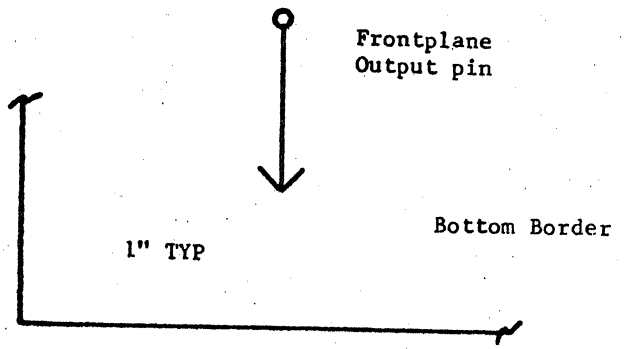
1 Signal entering or leaving Frontplane connector.

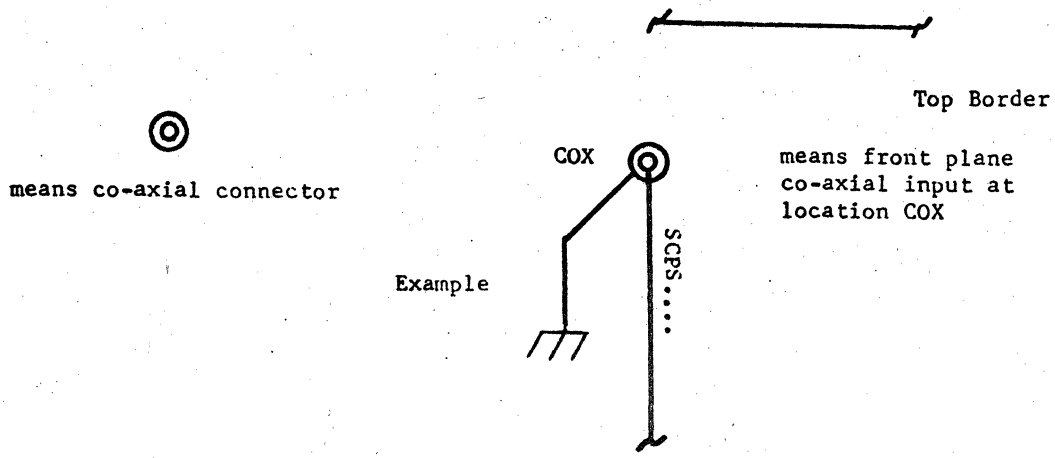
. Signal generated and used within the card.

Appendix on Logic Schematic Symbols (Continued)

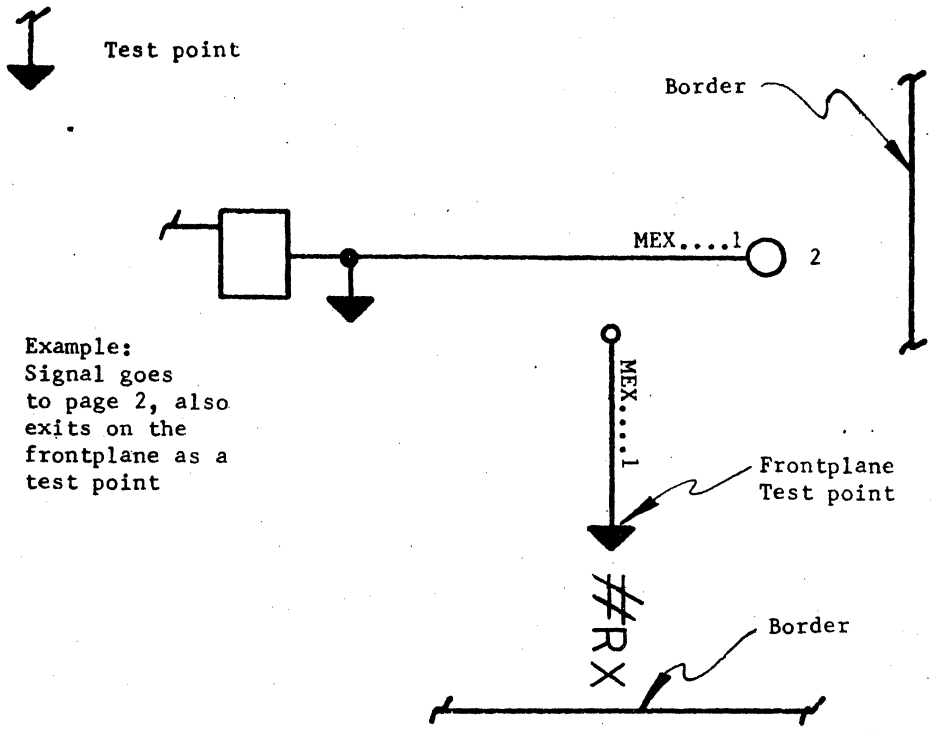


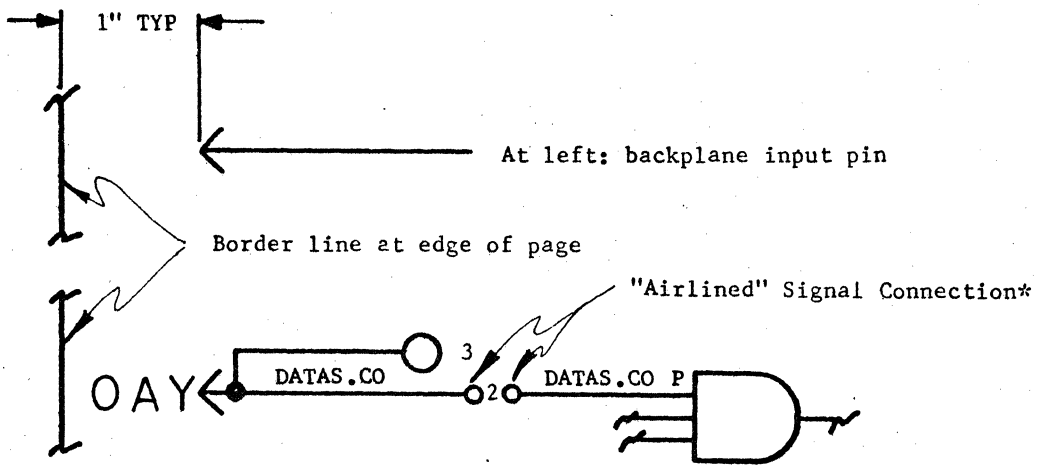
*"Airline" is a term applied to a method of symbolizing continuity when signal lines cannot be conveniently connected. Points common to the interrupted circuit are identified by the same signal name.





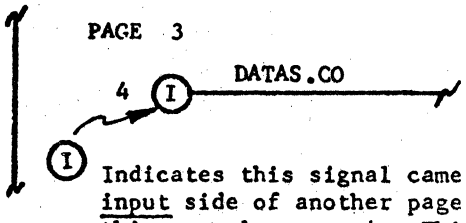
Appendix on Logic Schematic Symbols (Continued)



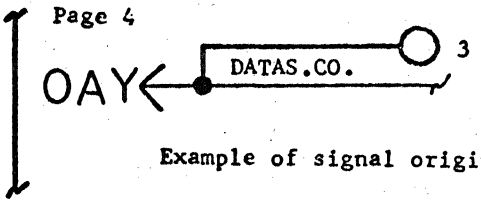


Example:
Above: Signal enters page thru backplane pin OAY as the source. Continuation of net (sinks) on the same page are represented by small open circles. The number by this symbol represents the number of "airlined" connections to be found. If there is no number, then one "airline" connection will be found. The 3 by the large open circle indicates that the net continues on Page 3 as an input.

Appendix on Logic Schematic Symbols (Continued)



Indicates this signal came from input side of another page, in this example, page 4. This only applies to backplane pins.

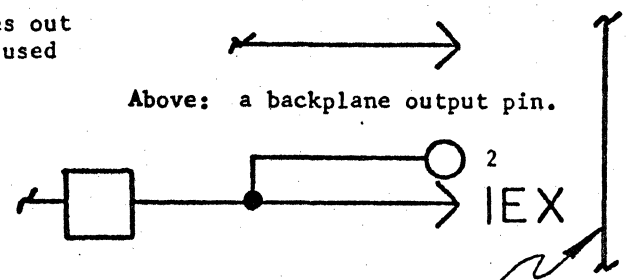


Example of signal origin

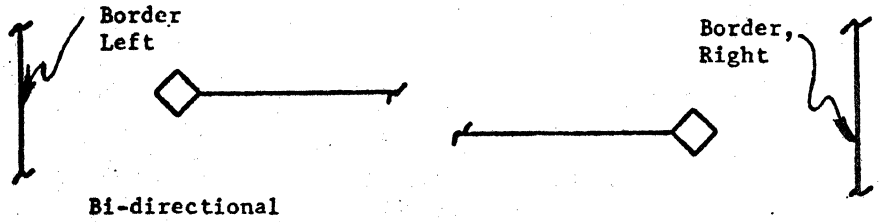
3 represents page number

---

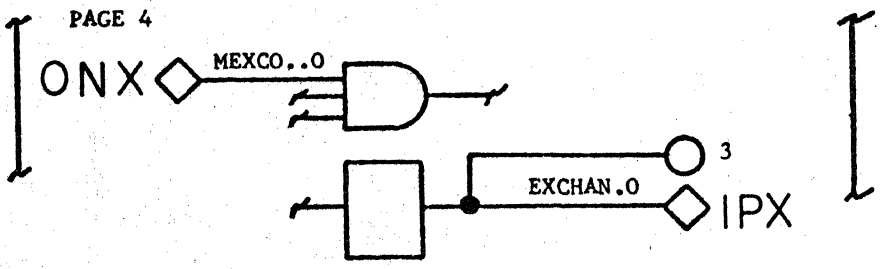
ample
low: Signal starts on this page, goes out backplane pin 1EX, and is also used on page 2.



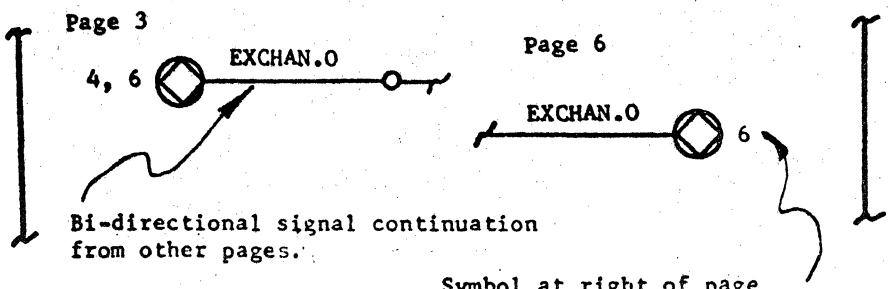
Above: a backplane output pin.



Bi-directional input/output pins



Example above shows Bi-direction input/output pins at backplane entry (left) and backplane exit (right).

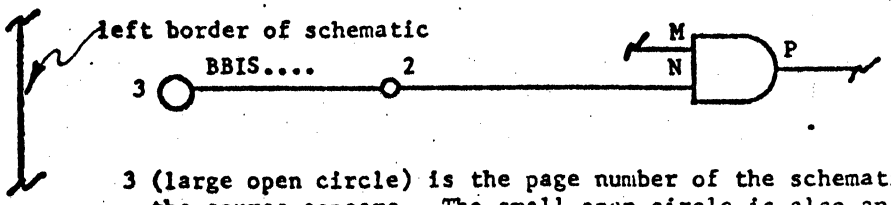


Bi-directional signal continuation from other pages.

Symbol at right of page is used to indicate multiple source of a net.

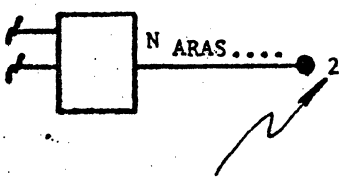
Appendix on Logic Schematic Symbols (Continued)

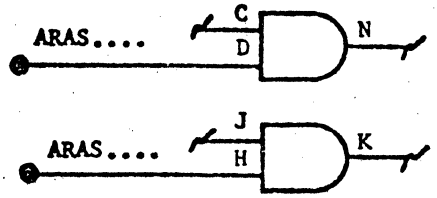
○ Means logic at this point originates off the page.



3 (large open circle) is the page number of the schematic on which the source appears. The small open circle is also an indication that the source is not generated from this page. The number 2 is the number of times signal BBIS.... is found airlined on this page.

● means logic is generated on this page, and leaves the page.



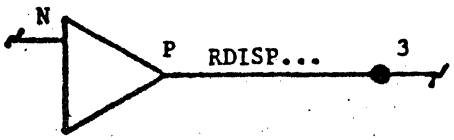


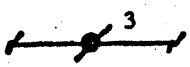
● 2 means signal ARAS.... is the source for two sinks (inputs) found to the right of the source on the same page.

BACKFEED SYMBOL

Representation for signals with both source and sink used on the same page. Backfeed symbolizes that the inputs can be found to the left of the source as well as to the right.

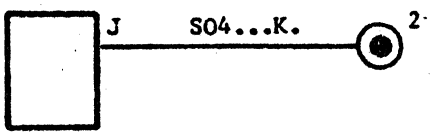
Example

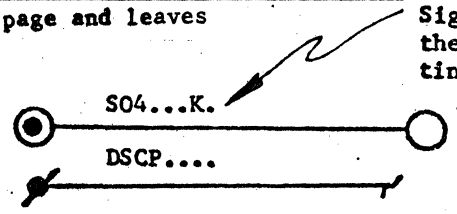




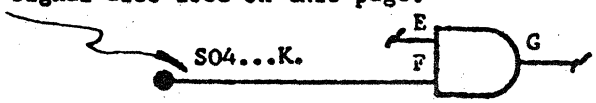
3. Example means the signal RDISP... is found three times on the page. The sinks can be on the left of the source (backfeed) and/or the right of the source.

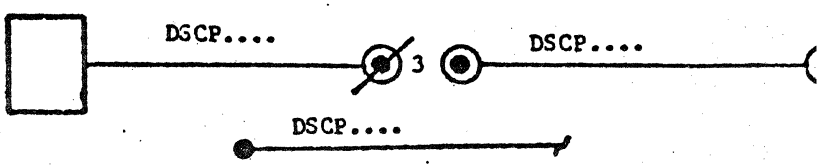
◉ means logic is generated on this page and leaves the page.





Signal also used on this page.

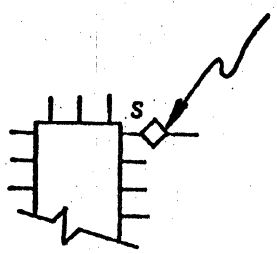




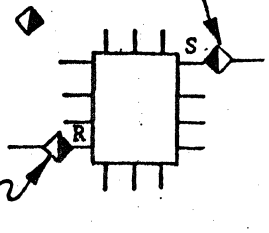
If there is no number of sinks to be found, then only one symbol will be shown leaving

This combination of symbols on the same page is also

Appendix on Logic Schematic Symbols (continued)



Indicates Bi-directional signal in or out of a Logic Element

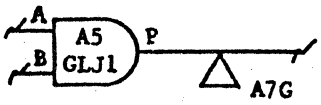


Indicates signal input

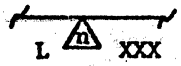
Indicates signal output

means 150 ohm, 1/8 W, resistor to ground on the solder side of the board

Example:



Above: the 150 ohm resistor is soldered to pin G of the chip at location A7.



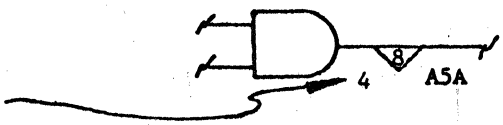
means resistor within a resistor chip

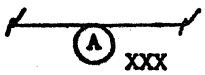
n - Type of resistor chip - - - - - - - - - The letter or number code is derived from Element Type designations, for example: (P) is RPNN, (8) is RP8N.

XXX - Chip location & Pin

L - Number of Loads

Example: A5 is the chip location. A is the chip pin for the resistor. 4 is the number of loads.



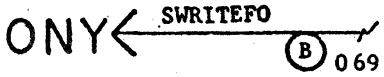


Discrete Resistor

A - Refers to Drawing note at bottom of Schematic page.

XXX - Resistor location

Example: Frontplane or Backplane resistor



Note: (B) 348 OHM 1/4 W, to -2.0V.

Locations 000 thru 212: at backplane connector.
Locations 250 thru 474: at frontplane connector.

Appendix on Logic Schematic Symbols (continued)

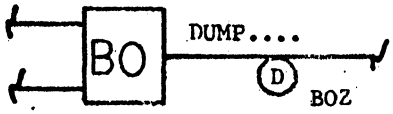
Example: Discrete Resistor Located between IC Chip and Bus Bar

Note: (D) 160 OHM 1/2W, to -2.0V

B9W will be part of the net with the other end of the discrete (B9X) Receiving Power.

Discrete resistor s located between the different letter designated rows on the circuit board and near the Bus.

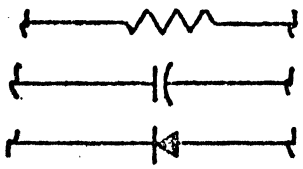
Example:



(D) OHM, 1/2W to GND

Any discrete resistor pin (XovY, WorZ) may be connected to the net. The other end at the resistor will receive power.

MISCELLANEOUS DISCRETE
COMPONENTS USED IN CHIP POSITIONS
(GENERALLY GBNN)



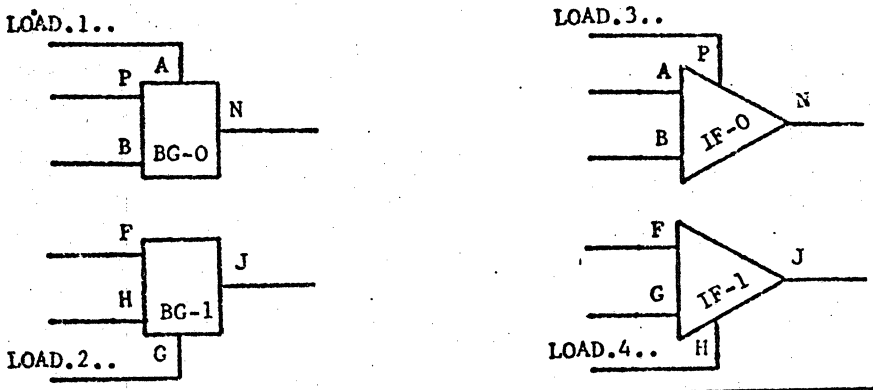
Example:

There are two available resistors in the BG-N chip and the IF-N chip.

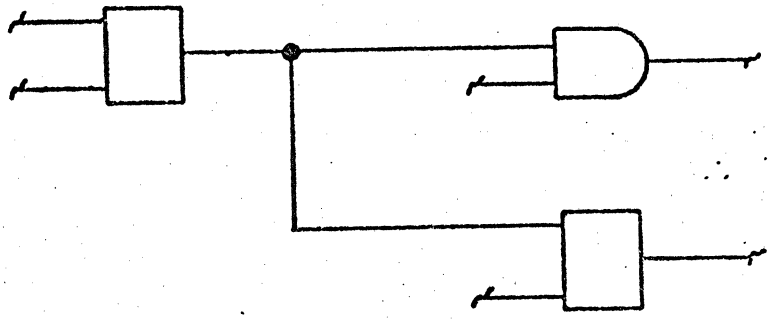
These resistors are 1 K OHM to Vee, representing 2 CTL loads.

Access through pins A and/ or G for the BG-N, and pins P and/or H for the IF-N.

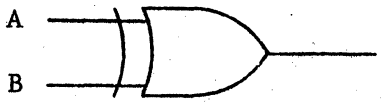
Schematically represented.



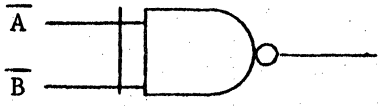
A dark solid circle on a line is a schematic representation of a line intersection. There is no implication of etch patterns or via holes



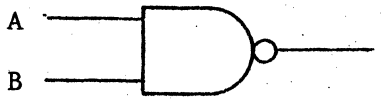
TTL DUAL SYMBOLS



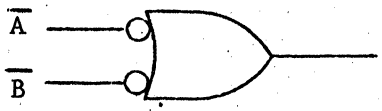
EXCLUSIVE OR



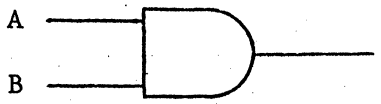
DUAL OF EXCLUSIVE OR



NAND GATE

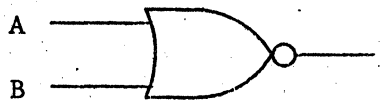


DUAL OF NAND GATE

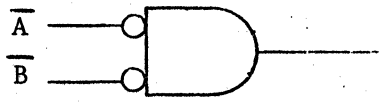


AND GATE

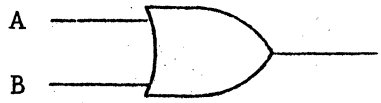
DUAL OF AND GATE



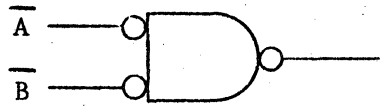
NOR GATE



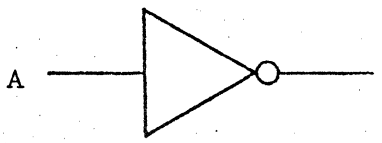
DUAL OF NOR GATE



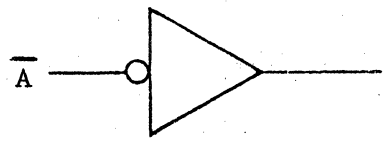
OR GATE



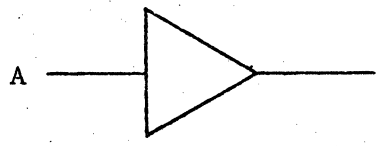
DUAL OF OR GATE



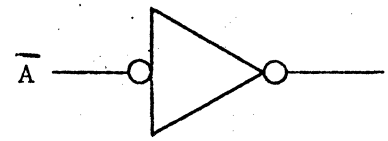
INVERTER



DUAL OF INVERTER



BUFFER



DUAL OF BUFFER

DISCRETE COMPONENT NAME LIST

VALUE	POWER DISSIP.	PART NUMBER	TO GROUND	TO -2V	TO 4.75	TO -12	TO +12
42.2	1/4	1111 8403	RG67				
51.1	1/4	1111 8429	RG25		R419		
56.2	1/4	1111 8437	RG21				
61.9	1/4	1111 8445	RG20		R418		
68.1	1/4	1111 8452	RG65				
75	1/4	1111 8460	RG15		R432		
82	1/2*	2206 6732	RG35	RX35	R430		
91	1/2*	2206 6823	RG34	RX34	R429		
100	1/2*	2206 6740	RG33	RX33	R428		
110	1/2*	2206 6831	RG32	RX32	R427		
120	1/2*	2206 6757	RG31	RX31	R426		
130	1/2*	2206 6765	RG30	RX30	R425		
150	1/2*	2206 6773	RG46	RX45	R424		
160	1/2*	2206 6781	RG45	RX44	R423		
180	1/2*	2206 6799	RG44	RX43	R422	R300	
200	1/2*	2206 6849	RG43	RX42	R431	R307	
220	1/2*	2206 6807	RG42	RX41	R421	R308	
237	1/4	1111 8585	RG49	RX08	R441		
261	1/4	1111 8593	RG09	RX03	R442		
287	1/4	1111 8601	RG04	RX07	R417		
316	1/4	1111 8619	RG00	RX06	R435		
348	1/4	1111 8627	RG28	RX21	R400		
383	1/4	1111 8635	RG62	RX51	R455		
422	1/4	1111 8643	RG48	RX15	R413		
464	1/4	1111 8650	RG24	RX27	R401		
511	1/4	1111 8668	RG26	RX04	R402		
562	1/4	1111 8676	RG02	RX28	R440		
619	1/4	1111 8684	RG29	RX39	R434		
681	1/4	1111 8692	RG55	RX49	R443	R305	
750	1/4	1111 8700	RG61	RX58	R454		
825	1/4	1111 8718	RG47	RX25	R411	R306	R500
909	1/4	1111 8726	RG56	RX55	R444		
1K	1/4	1111 8734	RG27	RX02	R404		R501
1.1K	1/4	1111 8742	RG01	RX56	R439		
1.21K	1/4	1111 8759	RG57	RX53*	R456		
1.33K	1/4	1111 8767	RG58		R445		

DISCRETE COMPONENT NAME LIST (CONTINUED)

VALUE	POWER DISSIP.	PART NUMBER	TO GROUND	TO -2V	TO 4.75	TO -12	TO +12
1.47K	1/4	1111 8775	RG60	RX13*	R407		
1.78K	1/4	1111 8791			R458		
1.96K	1/4	1111 8809		RX01*	R414		
2.15K	1/4	1111 8817		RX47*	R459		R502
2.37K	1/4	1111 8825			R457		
2.61K	1/4	1111 8833			R446		
3.16K	1/4	1111 8858	RG36		R447		
3.83K	1/4	1111 5574					
5.62K	1/4	1111 8916		RX59*	R452		
21.5K	1/4	1111 9054			R453		
MISCELLANEOUS COMPONENTS							
300PF	CAP	1920 2134	RG40				
470PF	CAP	2300 5531	RG51				
1000PF	CAP	2300 5572	RG52				
1UF	CAP	1907 8815	RG59				
33UF	CAP	2010 0715	RG92				
.01UF	CAP	2300 5697	RG53				
.1UF	CAP	2300 5820	RG39				
1.0UF	CAP	2200 7058	RG54				
DIODE		2208 6011	RG91	RX91			

* THIS DEVICE IS A 1/2 WATT RESISTOR IN A 1/4 WATT BODY.

FRONTPLANE RESISTOR LIST

PIN	GND +4.75	-2V -12V	PIN	GND +4.75	-2V -12V	PIN	GND +4.75	-2V -12V	PIN	GND +4.75	-2V -12V
$AX	250	375	#AX	275	400	$AY	300	425	#AY	325	450
B	251	376	B	276	401	B	301	426	B	326	451
C	252	377	C	277	402	C	302	427	C	327	452
D	253	378	D	278	403	D	303	428	D	328	453
E	254	379	E	279	404	E	304	429	E	329	454
F	255	380	F	280	405	F	305	430	F	330	455
G	256	381	G	281	406	G	306	431	G	331	456
H	257	382	H	282	407	H	307	432	H	332	457
I	258	383	I	283	408	I	308	433	I	333	458
J	259	384	J	284	409	J	309	434	J	334	459
K	260	385	K	285	410	K	310	435	K	335	460
L	261	386	L	286	411	L	311	436	L	336	461
M	262	387	M	287	412	M	312	437	M	337	462
N	263	388	N	288	413	N	313	438	N	338	463
P	264	389	P	289	414	P	314	439	P	339	464
Q	265	390	Q	290	415	Q	315	440	Q	340	465
R	266	391	R	291	416	R	316	441	R	341	466
S	267	392	S	292	417	S	317	442	S	342	467
T	268	393	T	293	418	T	318	443	T	343	468
U	269	394	U	294	419	U	319	444	U	344	469
V	270	395	V	295	420	V	320	445	V	345	470
W	271	396	W	296	421	W	321	446	W	346	471
X	272	397	X	297	422	X	322	446	X	347	472
Y	273	398	Y	298	423	Y	323	448	Y	348	473
$ZX	274	399	#ZX	299	424	$ZY	324	449	#ZY	349	474

BACKPLANE RESISTOR LIST

PIN	-2.0	GND	PIN	-2.0	GND	PIN	-2.0	GND	PIN	-2.0	GND
1AX			0AX			1AY	044	169	0AY	045	170
B	000	125	B	001	126	B	046	171	B	047	172
C	002	127	C	003	128	C	048	173	C	049	174
D	GND		D	004	129	D	GND		D	050	175
E	005	130	E	006	131	E	051	176	E	052	177
F	007	132	F	008	133	F	053	178	F	054	179
G	009	134	G	010	135	G	055	180	G	056	181
H	011	136	H	012	137	H	057	182	H	058	183
I	013	138	I	014	139	I	059	184	I	060	185
J	GND		J	015	140	J	GND		J	061	186
K	016	141	K	017	142	K	062	187	K	063	188
L	018	143	L	019	144	L	064	189	L	065	190
M	020	145	M	021	146	M	066	191	M	067	192
N	022	147	N	023	148	N	068	193	N	069	194
P	024	149	P	025	150	P	070	195	P	071	196
Q	GND		Q	026	151	Q	GND		Q	072	197
R	027	152	R	028	153	R	073	198	R	074	199
S	029	154	S	030	155	S	075	200	S	076	201
T	031	156	T	032	157	T	077	202	T	078	203
U	033	158	U	034	159	U	079	204	U	080	205
V	035	160	V	036	161	V	081	206	V	082	207
W	GND		W	037	162	W	GND		W	083	208
X	038	163	X	039	164	X	084	209	X	085	210
Y	040	165	Y	041	166	Y	086	211	Y	087	212
1ZX	042	167	0ZX	043	168	1ZY			0ZY		