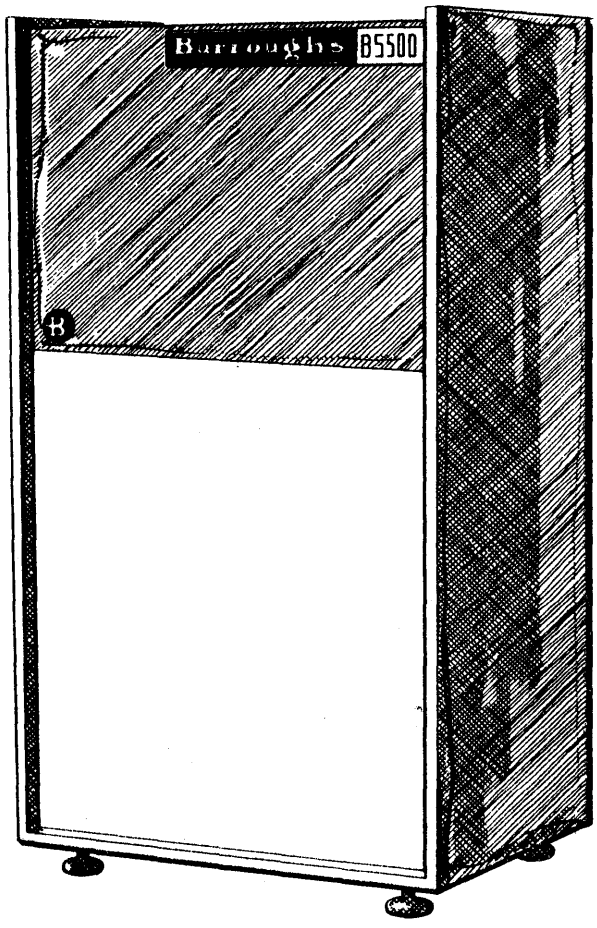
Burroughs

B 461

CORE MEMORY

FIELD TRAINING PACKAGE



SELF STUDY COURSE

PRINTED IN U.S.AMERICA

3-31-65

INTRODUCTION

This course is to be used by an individual who has been previously trained on the B 5500 and the B 460 Core Memory. The purpose of this training package is to give the student a working knowledge of the B 461 Core Memory.

The contents of this package are for the students aid in learning the B 461. It is suggested that the enclosed outline and review questions be followed.

The following are the contents of this package:

One B 461.51 Core Memory Technical Manual

A recommended Course Outline

One set of Review Questions

One set of Answer Sheets

Special Handouts

Printed in U.S. America

B 461 SELF STUDY COURSE OUTLINE

I. Introduction
   A. Read Subjects 1.1 thru 1.6
   B. Review Questions

II. Operation
   A. On-line
      1. Read Subject 2.1
      2. Review Questions
   B. Off-line
      1. Read Subject 2.2
      2. Review Questions

III. Core Stack
   A. Read Subject 3.1
   B. Assembly and Disassembly - Read Subjects 5.5 and 5.6
   C. Review Questions

IV. Addressing
   A. Read Subject 3.2
   B. Circuits
      1. Subject 3.6 (DRAC)
      2. Subject 3.7 (SWAD)
      3. Subject 3.10 (FFN7) - No Delay Flip-flop
   C. Review Questions

V. Read/Write Control
   A. Read Subject 3.3
   B. Circuits
      1. Subject 3.8 (DRIC)
      2. Subject 3.9 (AMS)
   C. Review Questions

VI. Memory Timing
   A. Read Subject 3.4
   B. Circuits
      1. Subject 3.11 (DSW1)
      2. Subject 3.12 (DY I)
      3. Subject 3.13 (DURW)
      4. Subject 3.14 (STMD)
      5. Subject 3.15 (MURW)
      6. Subject 3.16 (MUFW)
   C. Adjustments - Read Subject 5.1
   D. Review Questions

VII. Parity
   A. Read Subject 3.5
   B. Review Questions

VIII. Power
- A. Read Subject 3.17
- B. Circuits
  - 1. Subject 3.23 (SWVS)
  - 2. Subject 3.24 (SWHV)
- C. Regulators
  - 1. Subject 3.18 (-15V)
  - 2. Subject 3.19 (-30V Read/Write)
  - 3. Subject 3.20 (-30V Inhibit)
  - 4. Subject 3.21 (+30V)
  - 5. Subject 3.22 (-6T Regulator)
- D. Adjustments
  - 1. Input - Subject 5.3
  - 2. Unit Regulators - Subject 5.4
- E. Review Questions

IX. Clock & Clock Control
- A. Read Subject 3.25
- B. Circuits - Subject 3.26
- C. Adjustments - Subject 5.2
- D. Review Questions

X. Maintenance Control
- A. Maintenance Control Switches - Subject 3.27
- B. Start Logic - Subject 3.29
- C. Continue Circuits - Subject 3.32
- D. Clear Circuits - Subject 3.33
- E. Review Questions

XI. Pattern Control
- A. Pattern Control and Test Circuits - Subject 3.28
- B. Pattern Control Logic - Subject 3.30
- C. Pattern Control Checking - Subject 3.31
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XII. Maintenance Procedures and Aids
- A. Preventive Maintenance - Subject 6.1 through 6.5
- B. Marginal Testing - Subject 6.6
- C. Maintenance Panel Switches and Indicators - Subject 6.7
- D. Core Characteristics - Subject 6.8
- E. Component Locator - Subject 6.9
- F. Assembly Locations - Subject 6.10
- G. Terminations and Routings - Subject 6.11
- H. Troubleshooting Aids - Subject 6.12 through 6.19
- I. Review Questions

XIII. Installation
- A. Introduction - Subject 7.1
- B. Cabling - Subject 7.2 through 7.3
- C. Power
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  2. Applying Power to Cabinet - Subject 7.5
  3. Applying Power to Module - Subject 7.6
  4. Regulator Check
     - a. Subject 7.7 -6T reg.
     - b. Subject 7.8 -15 reg.
     - c. Subject 7.9 -30 regs.
- D. Manual Check - Subject 7.10
- E. Installation Stack Mounting Assembly - Subject 7.11
- F. Operations Check
  1. Local - Subject 7.12
  2. Remote - Subject 7.13

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B 461 CORE MEMORY

The following is a list of changes to be made in Central Control and the B 5500 Processor when replacing a B 460 Core Memory with a B 461 Core Memory.

Central Control A Rack

The following locations require a A 03 cut when the B 5500 is using a B 460 Core Memory and a A 3 cut when using a B 461 Core Memory. These changes control the gating to reset the Memory Cycle Flip-flops in Central Control. This allows the Memory Cycle Flip-flop for a Memory Module to reset at the same time the Crosspoint Flip-flop resets.

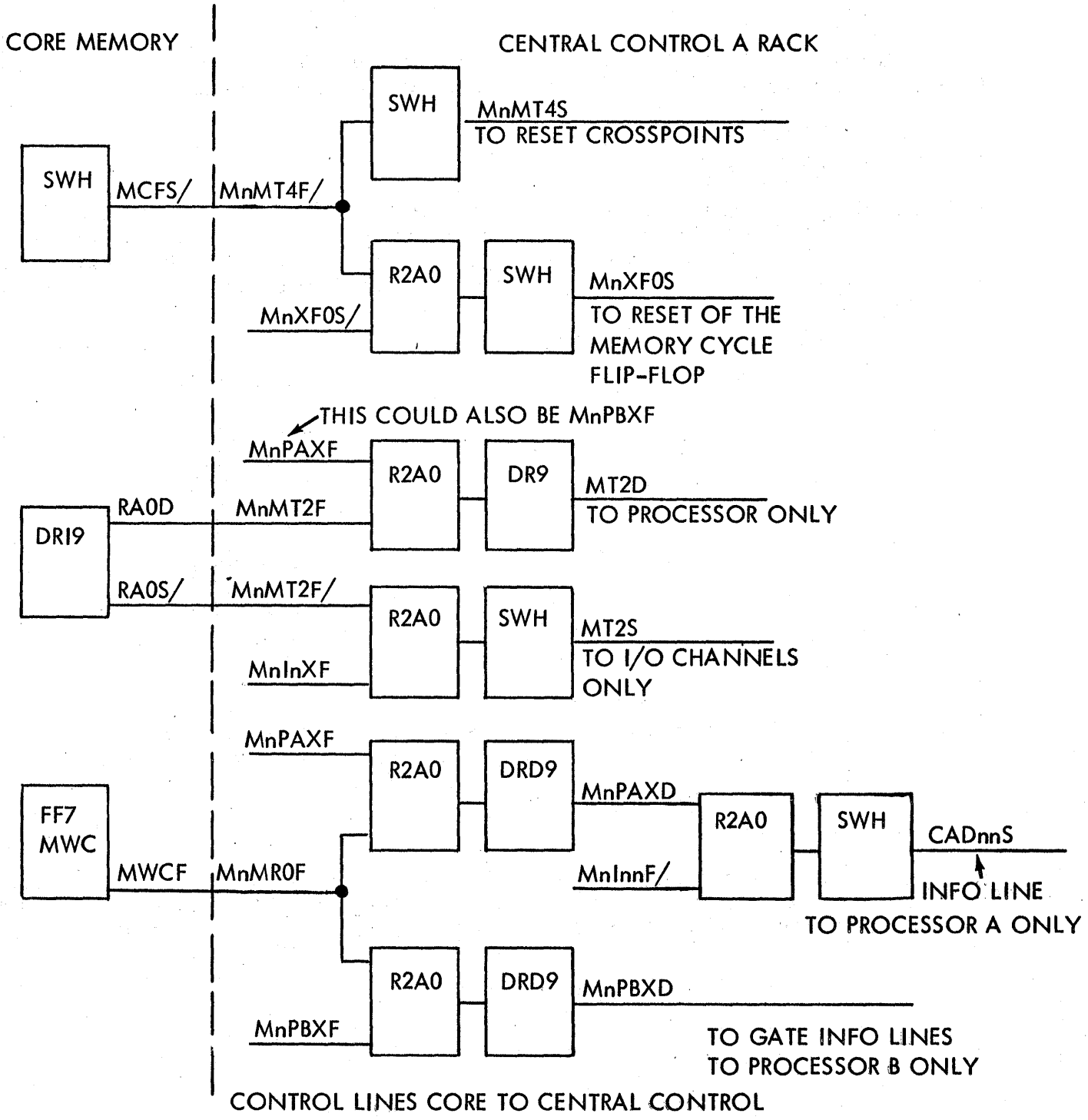
MEMORY MODULE	STICK LOCATION	CENTRAL CONTROL D. A. PAGE
0	AAA8Y7	55.10.02.1
1	AAB8Y7	55.11.02.1
2	AAC8Y7	55.12.02.1
3	AAD8Y7	55.13.02.1
4	ABA2Y2	55.14.02.1
5	ABB2Y2	55.15.02.1
6	ABC2Y2	55.16.02.1
7	ABD2Y2	55.17.02.1

NOTE

The above changes are referenced by Field Engineering Technical Memo B 5000 - No. 66-P, dated December 18, 1964.

Processor D Rack

Reference D. A. Page 65.70.06.0; the stick at location DEB8Y2 is to be installed for a B 461 (4 μs) Memory and not installed for the B 460 (6 μs) Memory. This stick will activate the term MTOL for setting E17F, reference the SECL & FETCH flow chart for the B 5500.


CORE MEMORY
CENTRAL CONTROL A RACK
SWH
MnMT4S
TO RESET CROSSPOINTS
SWH
MCFS/
MnMT4F/
R2A0
SWH
MnXF0S
MnXF0S/
TO RESET OF THE
MEMORY CYCLE
FLIP-FLOP
THIS COULD ALSO BE MnPBXF
MnPAXF
R2A0
DR9
MT2D
TO PROCESSOR ONLY
DR19
RA0D
MnMT2F
RA0S/
MnMT2F/
R2A0
SWH
MT2S
TO I/O CHANNELS
ONLY
MnInXF
MnPAXF
R2A0
DRD9
MnPAXD
R2A0
SWH
CADnnS
FF7
MWC
MWCF
MnMR0F
MnInnF/
INFO LINE
TO PROCESSOR A ONLY
R2A0
DRD9
MnPBXD
MnPBXF
TO GATE INFO LINES
TO PROCESSOR B ONLY
CONTROL LINES CORE TO CENTRAL CONTROL

B 461 REVIEW QUESTIONS

I. Introduction

1. Each B 5261 Memory Subsystem can contain up to _____ Memory Modules.

2. Which Memory Modules are located on which of the following racks? (Consider both Memory Subsystems)

   a. Rack A _____ c. Rack D _____

   b. Rack B _____ d. Rack E _____

3. Each Memory Module has a capacity of _____ words, each Memory Subsystem has a maximum capacity of _____ words, and a maximum size Memory System has a capacity of _____ words.

4. The B 461 Memory has a memory cycle time of _____.

5. The B 461 Memory has a read access time of _____ and a write access time of _____.

6. There are three modes of Off-line operation in the B 461. They are:

   a.

   b.

   c.

B 461 REVIEW QUESTIONS

II. On-Line Operation

1. Match the following logical terms:

a.	RAOD	AOOS
b.	MCFS/	WOOD
c.	MWCF	MT4F/
d.	RAOS/	MT2F
e.	MSTD	MT2S
f.	MISD	MROF

2. What actions occur with the memory strobe pulse (STTP) during a remote memory read operation?

3. What actions occurs with the memory strobe pulse during a remote memory write operation?

4. What condition will set the Error Flip-flop (MERF) during a remote memory operation? At what time during the memory cycle will this flip-flop be set?

5. When will RSPD be used to clear the Memory Module?

6. When operating the Memory On-Line, what registers and flip-flops are cleared by MICD? MACD?

7. The multi MS1M is TRUE for the entire memory cycle and its purpose is to enable the X and Y address switches.

TRUE FALSE

8. The purpose of MRWP is to:

a. Initiate the Post Write Disturb Pulse.
b. Initiate the Inhibit timing multi.
c. Create a delay between the read and write portions of a memory cycle.
d. Initiate a check of the information register for the correct parity.

B 461 REVIEW QUESTIONS

II. Off-Line Operation

1. At what count will the pulse counter be for the following stops?

   A. Single Cycle
   B. Stop-On-Final Address (AUTO)
   C. Stop-On-Final Address (MANUAL)
   D. Stop on Error

2. What two functions are caused by MWCF being set in a LOCAL operation?

3. The pulse counter must be at a count of zero and the Memory Module must be in LOCAL to count the address register with the STEP MAR button on the maintenance panel.

   TRUE FALSE

4. The MAR+1 at MPC=0, reference Figure 2.2-7, is used to count the address register prior to initiating a memory cycle when the START button is depressed.

   TRUE FALSE

   Qualify your answer.

5. When operating in LOCAL what registers and/or flip-flops are cleared by MICD? MACD?

6. What condition(s) will set MERF during a LOCAL memory operation?

7. When placing the Pattern Control Switch in the complement position, PCCL, the Memory will be forced to an Auto type of operation.

   TRUE FALSE

B 461 REVIEW QUESTIONS

III. Core Stack

1. What effect does a temperature change have on the characteristics of a ferro-magnetic core?

2. If the temperature of a core is decreased then the drive current required to change the state of the core is (increased/decreased).

3. What effect does a temperature change have upon the operation of a core stack?

4. There are _____ usable core planes in the B 461 Core Memory with _____ cores on each core plane.

5. Each time there is drive current in a X and Y line through the B 461 Core Memory there will be _____ half selected cores and _____ full selected cores on each core plane.

B 461 REVIEW QUESTIONS

IV. Addressing

1. The Address Register contains an address of 4527:

   A. Which X address switch will be selected?
   B. Which Y address switch will be selected?
   C. Which X read/write driver will be selected?
   D. Which Y read/write driver will be selected?
   E. Which X matrix transformer will be selected?
   F. Which Y matrix transformer will be selected?

2. For question number 1, what is the logical equation for selecting the Y read driver? Y address switch?

3. There are _____ transformer boards with _____ transformers on each board.

4. The odd numbered transformer boards are mounted (furthest/closest) from/to the core stack.

5. What is the purpose of a SWAD package?

6. How many matrix transformers are selected by each address switch? By each read/write driver?

7. Why are two levels (MACD and RSPD) used for the clearing of the Address Register?

8. The flip-flop FFN7 is used in the address register instead of the FF7. Why?

9. What useful purpose does ACDF accomplish?

10. Referencing Figure 3.2-10, when are each of the five AND gates into A+1D used?

B 461 REVIEW QUESTIONS

V. Read/Write Control

1. There are _____ information lines from Central Control to Core Memory and _____ information lines from Core Memory to Central Control.

2. How much drive current is provided by an Inhibit Driver?

3. In the Inhibit Driver package, what is the purpose of the diode CR6?

4. What is the status of the transistors in a Sense Amplifier during quiescence? (No input signal)

5. Under what conditions are the following used to set information into the memory information register?

   MISD

   RISD

   WISD

6. Reference Figure 3.3-2, what is the logic for generating the correct parity in the information register?

B 461 REVIEW QUESTIONS

VI. Memory Timing

1. What is the only difference between a memory read cycle and a memory write cycle?

2. What are the two basic methods of timing in the B 461 Core Memory and what is the function of each of these timing methods?

3. What is the logic for developing the following levels?

   A. MSTD

   B. RAOD

   C. MCFS/

4. What is accomplished by each of the following multi's and what is the time delay of each one?

   A. MS1M

   B. MR2M

   C. STTP

   D. MRWP

   E. MIHM

   F. MW2M

   G. MICM

5. Explain the various conditions for triggering MS1M.

6. Which of the multi's in the multi train are adjustable and what portion of their output is adjustable?

B 461 REVIEW QUESTIONS

VII. PARITY

1. Why is a parity check necessary in the B 461?

2. What type of parity check is used in the B 461? ODD EVEN

3. What happens if PERL is true during a memory read operation?

4. What happens if PERL is true during a memory write operation?

5. The following bits are set in the information register:

   I01F, I08F, I09F, I11F, and I17F

   What will be the status of EABS and PERL?

B 461 REVIEW QUESTIONS

VIII. Power & Power Control

1. List the power regulators contained within each Memory Module.

2. With all switches in the normal position and system power off, what is the status (picked or dropped) of the following relays:

   AJK1
   AJK2
   AJK3
   AJK4

3. What is the reason for the 150 ms delay in the pick of the relay AJK4?

4. What is the purpose of TODM? How long is its delay?

5. The -30V I, R and W will vary with a change in the temperature of the core stack. How is this voltage change accomplished?

6. Where is the -6T used and what is its purpose?

7. A voltage failure is indicated in a Memory Module, what is the status (picked or dropped) of the relays in the relay power control?

8. Is a TRUE or a FALSE level required to turn on the -30V regulators in a Memory Module? To turn on the +30V regulator?

9. What is the base of the transistor Q1 in the -6T regulator connected to?

10. How large a voltage change is required before an over or under voltage failure is indicated in a Memory Module?

11. If the core stack temperature is 70° F then the -15V regulator should be set to _____ volts.

12. If the core stack temperature is 70° F then the -30I regulator should be set to _____ volts.

B 461 REVIEW QUESTIONS

IX. Clock & Clock Control

1. What determines the memory clock pulse width when in Local and Remote?

2. What is the correct variable bias setting for the B 461?

3. What practical use can be made of the Inhibit Local Clock Switch on the maintenance panel?

B 461 REVIEW QUESTIONS

X. Maintenance Control

1. With the LOCAL/REMOTE switch in remote, what will be the status (True or False) of the following levels:

   a. TRML
   b. PCCL
   c. PCNL
   d. AUTL
   e. MANL
   f. SFAL

2. How long will MSTL be True each time the START button is depressed?

3. What is the purpose of MSTF?

4. Under what condition is the information register not cleared by MSTL?

5. What does the term P03S indicate when it is TRUE?

6. Describe the conditions that will make the level CTUS false.

B 461 REVIEW QUESTIONS

XI. Pattern Control

1. How does the address register affect the pattern generated in a checkerboard operation?

2. Which bits of the information register are affected by the TCBL switch?

3. What configuration of maintenance switches would be used to manually insert information into memory address 2345?

4. With the Pattern Control Switch in the complement position the term _____ will be true resulting in an operation of _____ memory cycles at each memory address.

5. What are the differences between a PCNL and PCCL operation?

6. What will be written into memory address 2347 if the memory is in checkerboard, worst case, the word True/Complement switch is in complement, all of the bit switches are in the True position, and this is the second memory cycle at this address?

7. During an Auto or Checkerboard operation how is an error detected and how is this error indicated?

B 461 REVIEW QUESTIONS

XII. Maintenance Procedures & Aids

1. What is the recommended frequency for checking the Memory margins and timing?

2. Which voltages are varied when running logic margins? Stack margins?

3. What are the minimum requirements to be met with Strobe margins?

4. What test pattern (or patterns) are used when running the -30 I R and W and the -6T margins?

5. What is the minimum overall margin (independent of pattern) for the following:

   -30I _____
   -30R _____
   -30W _____
   -6T _____

6. How can the -6T regulator be checked to see that it tracks the -12 correctly?

7. Give the package location of the Sense Amp and Inhibit Driver for information bit 22.

   Sense Amp -
   Inhibit Driver -

8. The SYSTEM power indicator on the maintenance panel comes on with the _____ volt and the LOCAL power indicator comes on with the _____ volt supply.

B 461 ANSWER SHEETS

I. Introduction

1. Four

2. a. Modules 2 or 6
   b. Modules 3 or 7
   c. Modules 1 or 5
   d. Modules 0 or 4

3. 4096, 16,384, 32,768

4. 4 μs,

5. 2 μs, 1 μs

6. a. Manual
   b. Automatic
   c. Checkerboard

II. On-Line Operation

1. a. RAOD - MT2F
   b. MCFS/- MT4F/
   c. MWCF - MROF
   d. RAOS/- MT2S
   e. MSTD - AOOS
   f. MISD - WOOD

2. The information read from the stack is set into the information register.

3. If an even number of bits are set in the information register then generate the correct parity (ODD) by setting bit 49 in the information register.

4. If a parity error exists during a memory read operation MERF will be set with a clock pulse at a pulse counter setting of two (MPC = 2).

5. When the system clock is in single or double pulse as indicated by the level SPUS at MPC = 3.

6. MICD clears only the information register.
   MACD clears MWRF and the address register.

7. TRUE

8. b and c

B 461 ANSWER SHEETS

II. Off-Line Operation

1. a. 0 c. 3
   b. 3 d. 3

2. MWCF will result in information being written in the complement of the pattern indicated by the pattern control switches.

   MWCF will also inhibit the counting of the address register when it is set to result in four memory cycles at each core address.

3. FALSE - can be at any pulse count.

4. TRUE - only if restarting from a stop on error condition.
   FALSE - not normally done at this time.

5. MICD - information register and the Error Flip-flop (MERF).
   MACD - none. MACD is not developed when operating in LOCAL.

6. A parity error when doing a manual read.
   A pattern error (not parity error) exists when doing an Auto memory operation.

7. FALSE - the CHECKERBOARD/UNIFORM switch forces an Auto operation.

III. Core Stack

1. The permeability of the core will decrease as the temperature of the core increases. This change in permeability will tend to make the core's hysteresis loop less square.

2. Increased.

3. An increase in core temperature will flatten the core's hysteresis loop and generate more noise in the stack, therefore the drive current through the core is decreased. A decrease in core temperature will make the core more stable, requiring an increase in drive current to change the state of the core.

4. 49, 4096

5. 126, 1

IV. Addressing

1. a. X20S
   b. Y40S
   c. XR7D and XW7D
   d. YR5D and YW5D
   e. 27
   f. 45

B 461 ANSWER SHEETS

2. YR5D = A07F • A08F/ • A09F • MR2M
   Y40S = A10F/ • A11F/ • A12F • MS1M

3. 4, 32

4. Furthest

5. The output of each SWAD package is connected to the primary center tap of eight matrix transformers, allowing one of these eight transformers to be selected by a read/write driver. The SWAD will complete a path for current to the +30V supply for this selected transformer.

6. 8, 8

7. MACD is the normal clear for the address register and is used when the system clock is in the normal mode of operation as indicated by the term SPUL/. The level RSPD is used to clear the address register when the system clock is in single or double pulse mode of operation. MACD is developed by the multi train and it coincides in time with MICM and RSPD is developed with the pulse counter equal to three.

8. The FFN7 type of flip-flop, with the delay removed from the flip-flop circuit, is used to allow the address lines in the memory to be in their proper configuration prior to the initiation of the multi timing which occurs before the trailing edge of the TO clock pulse.

9. The flip-flop, ACDF, along with the cross-coupled switches of the address register, is used when counting the address register to overcome the delay removed from the FFN7 flip-flops.

10. AND #1 Used to develope A+1D when the STEP MAR button is depressed.
    AND #2 Used when the memory is operated in Manual to count the address register at the completion of each memory cycle.
    AND #3 Used when operating the Memory Module in Auto (or Checkerboard) to count the address register at the completion of a memory write cycle. A two or four cycle operation is determined by MWCF/ in the SHUNT AND.
    AND #4 Used in Auto (or Checkerboard) if a stop had occurred.
    AND #5 Used in Manual if a stop had occurred.

V. Read/Write Control

1. 48, 49

2. Approximately 250 ma.

3. To provide a path for a rapid decay of the inhibit current when the driver is turned off.

4. To reduce the noise on the output of a Sense Amplifier.

B 461 ANSWER SHEETS

5. Q1 and Q2 are conducting, operated class A.
   Q3 is cut off.
   Q4 is in saturation.

6. MISD - used during a remote memory write operation to set the information to be written into the information register and to set MWRF.

   RISD - used during all memory read operations to strobe the Sense Amp. outputs into the information register.

   WISD - used when in an Auto or Checkerboard operation to set the correct pattern of information into the information register.

7. 149F = + MWRF • STTP • PERL • TRML REMOTE
   + MANL • MWRF • STTP • PERL LOCAL and MANUAL

VI. Memory Timing

1. Information read is not set into the information register at strobe time for a memory write operation.

2. Pulse counter - counts with each clock pulse to sync the operation of the multi timing with logical operations which are controlled by the system clock.
   Multi timing train - initiated by a clock pulse but otherwise completely independent of the system clock, used to generate the timing levels necessary for proper operation of the core stack.

3. MSTD = AOOS • TRML • MP1F/ • MP2F/
   RAOD = MP1F • MWRF/ • MP2F
   MCFS/= MP1F/ + TRML/ + MP2F/ - This equation is written to make MCFS/TRUE.

4. All times indicated are in microseconds.

   a. MS1M - 2.7 True for the entire memory cycle this multi is the enabling level to the SWAD packages. It is also used to trigger MR2M.
   b. MR2M - 1.0 True output for the read portion of a memory cycle during which it provides an enabling level to the X and Y read current drivers. It is also used to trigger the Strobe multi and the read to write delay multi.
   c. STTP - .15 Developes the Strobe timing pulse during the read portion of a memory cycle.
   d. MRWP - .3 or greater. Developes a delay between the read and write portions of a memory cycle.
   e. MIHM - 1.18 During the write portion of a memory cycle, gated with the information register, enables the inhibit current drivers. This multi also provides a holdover to MS1M to insure that MS1M does not time out and it triggers MW2M and MICM.

f. MW2M - 1.0 Provides the enabling level for the X and Y write current drivers and provides a holdover for MIHM.

g. MICM - .15 Used at the end of a memory cycle to provide the clear pulse for the memory module.

5. MS1M = + MSTD•CCP-6 Used in REMOTE
+ MSTL•CCP-6•MP1F/•MP2F/ Used in LOCAL with the START button
+ MSTF•CCP-6•MP1F/•MP2F/ Used in LOCAL and continuous.

6. MR2M - trailing edge only
STTP - leading edge only
MW2M - trailing edge only

VII. Parity

1. Parity is checked in the B 461 to test the validity of the information read from the core stack.

2. ODD

3. PERL during a memory write operation will result in the correct parity being generated by setting I49F at Strobe time (STTP).

4. PERL during a memory read operation indicates that an error exists in the information read from the core stack and will result in the Error Flip-flop being set (MERF).

5. EABS will be TRUE
PERL will be FALSE

VIII. Power & Power Control

1. -30I, -30R, -30W, +30, -15, and -6T.

2. AJK1, AJK2, AJK3 are all picked, AJK4 is dropped.

3. To allow sufficient time for the B 5500 power supply to come up to prevent an incorrect voltage fail indication.

4. Initiates the turning on of the -30V regulators and the 30ms delay prevents a false voltage fail indication.

5. A change in stack temperature will change the resistance of the thermistor, mounted next to the core stack, which will reslut in a change in the -15V regulator output. The -15V change will then change the -30V regulator outputs. This change is such that an increase in temperature will make the -15 and the -30 (I R and W) to go more positive.

B 461 ANSWER SHEETS

6. Goes to all Sense Amplifiers to provide a threshold for the class A amplifiers in the Sense Amps.

7. All picked.

8. FALSE to turn on the -30 I, R, and W. TRUE to turn on the +30.

9. To the -6T adjusting pot on the maintenance panel.

10. 25% increase for an over voltage fail and 30 to 35% decrease for an under voltage fail.

11. Approx. -15.4V. (Reference, Figure 5.4-1)

12. Approx. -32.7V. (Reference, Figure 5.4-2)

IX. Clock & Clock Control

1. LOCAL - By the MUFW located at AAC6A2 in the Module.
REMOTE - In Central Control at the BO& Line Driver.

2. 0.5 V

3. Only method by which the local clock can be inhibited to allow manual setting of flip-flops via the maintenance panel.

X. Maintenance Control

1. a. TRUE
b. FALSE
c. FALSE
d. FALSE
e. FALSE
f. TRUE or FALSE (not affected by the LOCAL/REMOTE switch)

2. MSTL, due to the synchronizer circuit, will be TRUE for only one clock pulse time.

3. Used as a control flip-flop when in LOCAL to initiate a memory cycle and count the address register and complement the Write Flip-flop (MWRF).

4. A Manual write operation

5. When TRUE indicates that the pulse counter is equal to zero or three.

6. Reference, Figure 3.32-1; CTUS will be FALSE if any one of the following are TRUE:

TRML - TRUE when LOCAL/REMOTE switch is in REMOTE.

TSCL - TRUE for a single cycle operation.

B 461 ANSWER SHEETS

CAG005 • MWCF/ • MWRF • SFAL - Auto operation with the STOP-ON-FINAL-ADDRESS switch in the STOP position and the address register equals 7777.

CAG005 • MANL • SFAL - Stop final address when in a Manual operation.

MERF • SOEL - Error Flip-flop is set and the STOP-ON-ERROR switch in the STOP position.

XI. Pattern Control

1. The address register will change the pattern being read or written every second address and then completely reverse this pattern every two hundred addresses. This is accomplished by examining the state of A02F and A08F.

2. 6, 12, 18, 24, 30, 36, 42, 48 and 49

3. LOCAL/REMOTE switch in Local
UNIFORM/CHECKERBOARD switch in Uniform
SINGLE CYCLE/CONTINUOUS switch in Single Cycle
MANUAL/AUTO switch in Manual
Set the address register to 2345
Set the information into the information register
Depress the START button to initiate a memory cycle

4. PCCL, 4

5. A PCNL operation is a two cycle operation and the PCCL is a four cycle operation in which the complement of the pattern indicated by the word and bit TRUE/COMPLEMENT switches is also tested.

6. Pattern written will be all ones.

7. The pattern is checked by comparing the information register to the pattern control circuitry. The information is tested for the specific configuration of bits as indicated by the pattern control circuitry. If an error does exist, an incorrect configuration of bits, then the error is indicated by setting the Error Flip-flop (MERF).

XII. Maintenance Procedures & Aids

1. Quarterly

2. Logic margins: -12 and -L2 (also the clock pulse width is varied)
Stack margins: -30I, -30R, -30W, and the -6T

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3. Total of 120 ns. margin with a minimum of 50 ns. on either side of the nominal setting of 630 ns. from the leading edge of MR2M.

4. Checkerboard true - PCCL and PCNL
   Checkerboard complement - PCCL and PCNL
   Uniform true - PCCL

5. -30R - 3.00V Reference, Table 6.6-1
   -30W - 2.25V
   -30I - 4.50V
   -6T - 0.75V

6. By placing a meter between the -6T and the -12V the difference should remain constant within 0.1V as the -12V is varied from -11V to -13V.

7. Sense Amp - AAD6A0 Reference, Section 6.10
   Inhibit Driver - ACC6N0

8. +100, -30I