Burroughs Corporation

ELECTRODATA M & E DIVISION
PASADENA CALIFORNIA

CHANGE SHEET

TITLE
BASIC MAINTENANCE TEST ROUTINES, B5500

A- 11187275

REV. A

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REV. LTR.	CONT. DOC. & NO.	DFT-MAN	CHKR.	APP'D BY & DATE	PAGE	LINE OR ¶	REVISION DESCRIPTION
A	ER 1635A	H.R	[illegible]	[illegible] 6-7-65			Released

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1 INTRODUCTION

1.1 General

The four Basic Test Routines perform a checkout of part of the processor logic. The areas of the processor logic tested are those used by the Control Section of the General Test Routine.

The operators tested in varying degrees of completeness depending on the extent of their functional usage by the GCR are:

Initiate - Initiate for Test

Store for Interrupt - Store for Test

Conditional and Unconditional Branch

Literal Call

Load

Duplicate

Exchange

B Store

Dial A

Dial B excluding DIB 0

Compare Field

Transfer bits

Index

Interrogate Interrupt

Initiate I/O

Set S

1.2 Assumptions

Throughout the construction of the Basic Tests a number of assumptions were made. For the successful use of the Basic Test Routines, these same assumptions, as listed below, must stay true while the routines are run.

a) The design of the processor is correct. The physical implementation of the design is as described by the equations in the Processor Logic Book, except for the possible presence of component failure(s) of the type(s) given in c) below.

b) The following logic functions work properly:

1) Loading of Memory Modules #0 and #1 from magnetic tape or cards

2) Proper fetching and execution of the conditional halt operator

3) The setting of the J and L registers to the various required values occurs properly within the operator's tested.

4) The inhibit logic that affects the T-register decoding of the tested operators.

c) Failures looked for by the Basic Test Routines are of the following types:

Faulty gating logic (open diodes).

Flip-Flop stuck in one of the two states.

Note: Failures detected are caught through the occurrence of erroneous flip-flop states. Errors identical in their effects to those listed above are automatically covered.

d) Only single failures within a function occur.

Note: The consequence of this assumption is that multiple failures within the same function (e.g. those affecting more than one bit in a register

1.2 Assumptions (Cont'd)

transfer) generally have unpredictable effects on the routines.

e) Logic functions checked out early in a test routine run do not fail during the rest of the run.

1.3 Related Documents

B5500 Processor MTR Basic Tests (1 through 4) Program Listings	11187317 11187366 11187416 11187465
B5500 Processor MTR Basic Test Error Look-Up (1 through 4)	11187333 11187382 11187432 11187481
B5500 Processor MTR Tape Loader Program Listing	11187572
B5500 Processor MTR Binary Card Loader Program Listing	11187515
B5500 Processor MTR Alpha Card Loader Program Listing	11187549
B5500 MTR Card Punch-Out Routine Program Listing	11187606
B5500 Processor MTR Test Tape	11187614

2 DESCRIPTION

2.1 General

The following rules were followed in writing the tests:

a) Minimize the amount of yet untested logic from test case to test case.

b) Attempt to reduce the effects of multiple failures.

c) Allow the start of the routines at any test case.

2.2 Error Indication

a) Single Failures

For each Basic Test Routine an Error Book is made available containing an error index list. This list is sorted by the location of the error halts. The error indication is accomplished by keyed Conditional Halt Operators. The key is the C and L register contents plus occasionally the contents of the S register for a finer breakdown. The comment associated with each

2.2 Error Indication (Cont'd)

halt gives the type of failure, the operator tested, and the test case number. Thus the test case can be located within the ESAP listing and a manual stepping through the failing action can be done. Relying on the notes given with specific error halt locations is seldom sufficient. Manual stepping through is necessary for the confirmation of the failure suggested in the Error Book and for additional information about the failing logic.

b) Multiple Failures

The Basic Test Routines were not written to catch multiple failures within a function. The occurrence of a multiple failure would generally destroy information essential for the proper functioning of the test routines. To minimize the occurrence of information destruction, the memory cells not used by the Test Routine are filled with conditional halt operators. These halts are not referenced in the Error Book. They can only be reached if certain multiple failures have occurred. These multiple failures would not then destroy the program. To give some information about an error of this type, a list of S settings is supplied with each basic test routine. The associated test case number is printed next to each S setting. If an error of the above type occurs which does not alter the S value, the failing test case can be located. Manual stepping through this test case should then aid in obtaining the necessary diagnostic information.

2.3 Auxiliary Programs for Loading

Four auxiliary routines have been written for loading the Basic Test Routines either from magnetic tape or from punched alpha cards. The auxiliary routines are:

a) Binary Loader

The Binary Loader consists of two binary punched cards. It loads alpha cards punched in the format of the ESAP machine deck. Only the Basic Operators are utilized in this loader.

b) Memory Punch

This program punches the contents of memory on cards in a special format. Nine words of information are punched in each card plus a sequence number in Columns 73-80. Punching starts from memory location 400 octal, then proceeds sequentially through location 10400 octal. This program uses an operator set not restricted to the basic operators.

Note: This punch program is used four times to create the four basic test program decks.

c) Alpha Card Loader

This program loads the cards punched by the Memory Punch program. Each of the back-up decks can be loaded by this program and each Basic Test Routine can be executed manually. This program utilizes only the Basic Operators.

d) Tape Loader - Chaining Routine

This program automatically reads each Basic Test Routine from magnetic tape and initiates its execution for a specified number of times. When all Basic Test Routines have been executed, the General Control Routine is read in from tape and control is transferred to it.

2.4 Options

2.4.1 Loading Options

Basic Test Routines may be loaded into memory from magnetic tape or from punched cards. The Routines on tape may be loaded automatically or manually.

2.4.1.1 When Automatic Tape Loading Should be Used

Automatic tape loading of the Basic Test Routines, by utilizing the Tape To Memory program, should be attempted only when no erroneous conditions in the basic logic are anticipated.

2.4.1.2 When Manual Tape Loading Procedure Should be Used

a) When erroneous conditions are known or suspected to be present in the basic logic.

b) When a failure has been detected during automatic loading.

c) When tape loading is impossible automatically.

2.4.1.3 When Back-Up Decks Should be Used

Back-up card decks for each routine are supplied to the field engineer to input basic test routines into storage when no method of tape input is possible.

2.4.2 Program Control Options

2.4.2.1 Looping

a) Altering the number of times Routine Execution is to be performed

1) For all routines:

Stopping Point For Change: The final card of the Tape To Memory program transfers control from Program Loading to Program Execution.

2.4.2.1 Looping (Cont'd)

Remove this card before loading. The machine will halt after loading and before execution for manual memory alterations.

Alteration: "MAXLP", the number of times that all routines are to be executed, is contained in memory cell 334. Normally this cell contains an octal 1,000 value. It may be manually changed to any value desired. Only the last 15 bits will be considered by the program.

Re-Entry: To initiate Program Execution following a manual change of this nature:

Push Master Clear button.

Set C Register to 10410.

Set S Register to 100.

Set E Register 16 Bit ON

Push Single Pulse button.

2) For A Particular Routine:

At any time during the Execution Phase of a test routine, the processor may be halted by setting the Exit switch to ON position. The above manual changes may then be made to affect the current and all subsequent Basic Test Routines.

b) Repetitive Execution of a Portion of a Basic Test Routine

ESAP listings of each routine show the overall sequence in which the test cases within that routine are executed. Within each test case, the lower 15 bits of the Initiate Control Word serve as a pointer to the

2.4.2.1 Looping (Cont'd)

Interrupt Return Control Word of the test to be executed next in sequence. These lower 15 bits may be altered manually to change the execution sequence of the test cases.

1) Stopping Point For Change:

Use the Exit Switch halting procedure as described under 2) on the previous page.

2) Alteration:

The execution sequence of test cases is the same as their sequence on the program listing. Changing of the INCW of any test case to point at the IRCW of a preceding test case will thus result in the following looping operation:

The test in which the change was made becomes the last test executed in the loop.

The test to which the altered pointer refers becomes the first test case of the loop.

Routine Loop Tally is disregarded.

Minimum size of loop could be one test case.

Maximum size of loop could be entire routine.

Changing of an INCW to point at the IRCW of a test following it on the ESAP list, results in the skipping of all test cases which fall between the two on the list.

3) Re-Entry:

Turn the Exit switch to OFF position.

2.4.2.2 Single Pulsing Through a Test Case (Using ESAP Program Listing)

a) Set the S Register to the address of the Initiate Control Word of the case. Set E16.

b) Set C Register and L Register so that they point at an Initiate For Test syllable (Octal Code 5111), with one exception. If (in Routine #4 only) the program string of the test case immediately preceding the desired one terminates with a Literal Call-Load-Initiate for Test set, C and L should point to the Literal Call syllable.

c) Set Clock Mode switch to "Single."

d) Begin single pulsing operation.

2.5 Operating Instructions

2.5.1 Automatic Loading From Tape - Tape To Memory Program

a) Initiation of Program

1) Set Stop On Operator switch to ON position.

2) Set Card Load Select switch to ON position.

3) Set INH CC103F switch to INH position.

4) Place the M.T.R. System tape on a MTT unit (A through F) and put the unit in Ready status.

5) Six Tape Unit Designate Cards are contained in the Tape To Memory program. Select the card for the tape unit chosen for input, and place it as the last to be read of these Designate cards.

6) Place Tape To Memory loader in card reader and make the unit ready.

7) Push the Halt button on the console.

8) Push the Load button on the console.

2.5.1 Automatic Loading From Tape - Tape To Memory Program (Cont'd)

b) Action of the Program

1) A Test Routine is called into memory from tape.

2) The Test Routine is executed the number of times prescribed by the Tape To Memory program.

3) Provided no error halts occur, the next routine is brought into memory from tape. See 2.2 in case of an error halt.

4) After execution of the final test routine (Routine #4), the General Control Routine is called into memory, and control is transferred to it.

2.5.2 Manual Loading of Routines From Tape

a) Description and Physical Layout of Routines on Tape:

1) The B5500 Basic Test consists of four Test Routines.

2) A Test Routine contains many individual Test Cases.

3) Ten Tape Records make up each Test Routine on magnetic tape.

4) Records of the Basic Test are followed by the records of the General Control Routine.

2.5.2 Manual Loading of Routines From Tape (Cont'd)

b) Reference Table for Manual Loading

ROUTINE RECORD SEQUENCE	BEGINNING MEMORY AREA	OCTAL RECORD LENGTH
1	400	1,000 words
2	1400	1,000
3	2400	1,000
4	3400	1,000
5	4400	1,000
6	5400	1,000
7	6400	1,000
8	7400	400
9	0	400
10	10,000	400

The above table indicates the memory areas into which each record of a basic test routine should be read.

A tape read descriptor is to be entered into memory manually, describing the input tape unit and the beginning memory area. After completion of the test routine read-in, care should be taken to restore the proper test routine information into the cell used for the tape read descriptor.

EXAMPLE: Location 140 may be used to store a Tape Read Descriptor to read in records 1 through 8. Then, remembering the contents of a location greater than 400, say 500, store in this cell a

2.5.2 Manual Loading of Routines From Tape (Cont'd)

Tape Read Descriptor, and read into the 0-400 area. Then restore the cell to its previous contents.

c) To Begin Manual Tape Read-In Operation:

1) Manually write into memory a Tape Read Descriptor.

2) Manually write into Octal memory location 10 (15 low order bits) the octal address of this tape read descriptor.

3) Push I/O Clear button.

4) Set I/O Local-Remote Switch to Local and all other I/O switches to the down position.

5) Push the I/O Start button to read one record from tape.

6) Check the Result Descriptor (in Octal location 14) for correctness.

7) Repeat the above steps necessary to read in the entire test routine.

d) Necessary Manual Cell Change (After Manual Read-in)

For Routine #1 Enter 0000000000002000 Into Location 6040

" " #2 " 0000000000401777 " " 6234

" " #3 " 0000000000001777 " " 3256

" " #4 " 0000000000007404 " " 5520

e) To Begin Execution:

1) Set S Register to 2000

2) Set C Register to 2000

3) Set L Register equal to 1

4) Set E Register 16 Bit ON

5) Push Single Pulse Button. If no error occurs, the routine will loop indefinitely.

2.5.3 Loading A Test Routine From Back-Up Card Deck

a) Place Card To Memory program in front of test routine card deck, place in Card Reader, and make the unit ready.

b) Push Master Clear, Halt, and Load buttons.

c) For the execution of the test routine loaded from cards

1) Set S Register to 2000

2) Set C Register to 2000

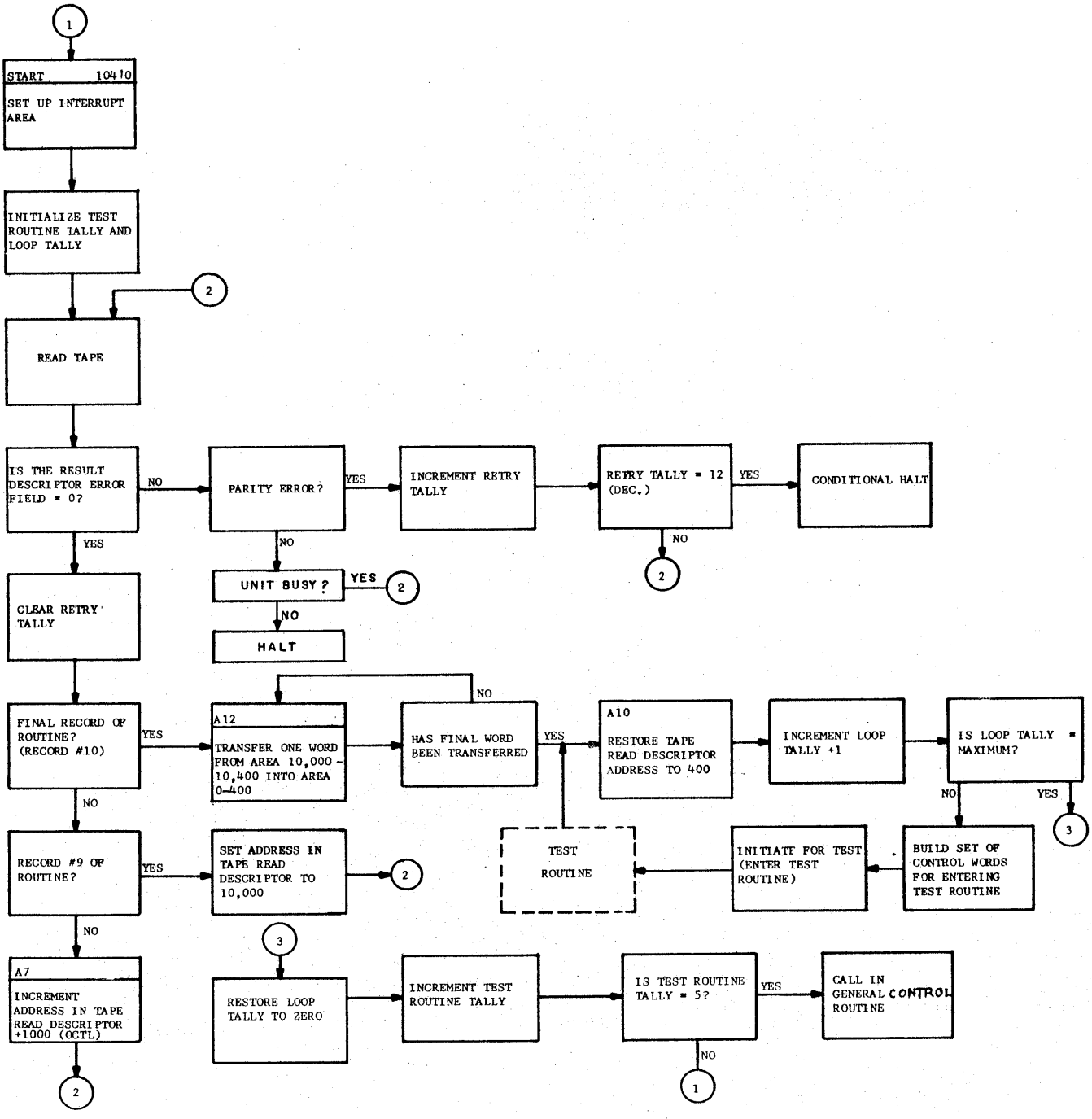
3) Set L Register equal to 1

4) Set E Register 16 Bit ON

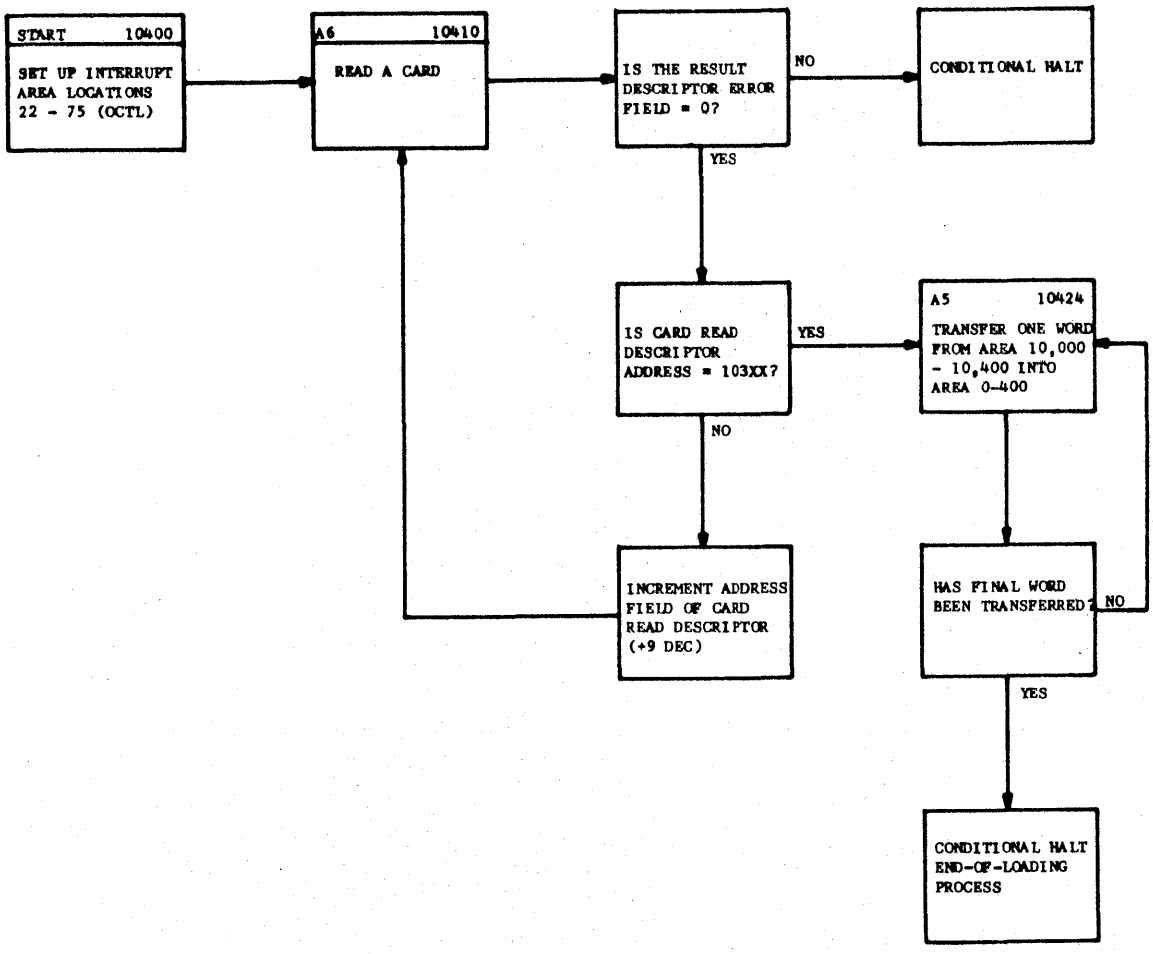
5) Push Single Pulse button. If no error occurs, the routine will loop indefinitely.

3. FLOW CHARTS

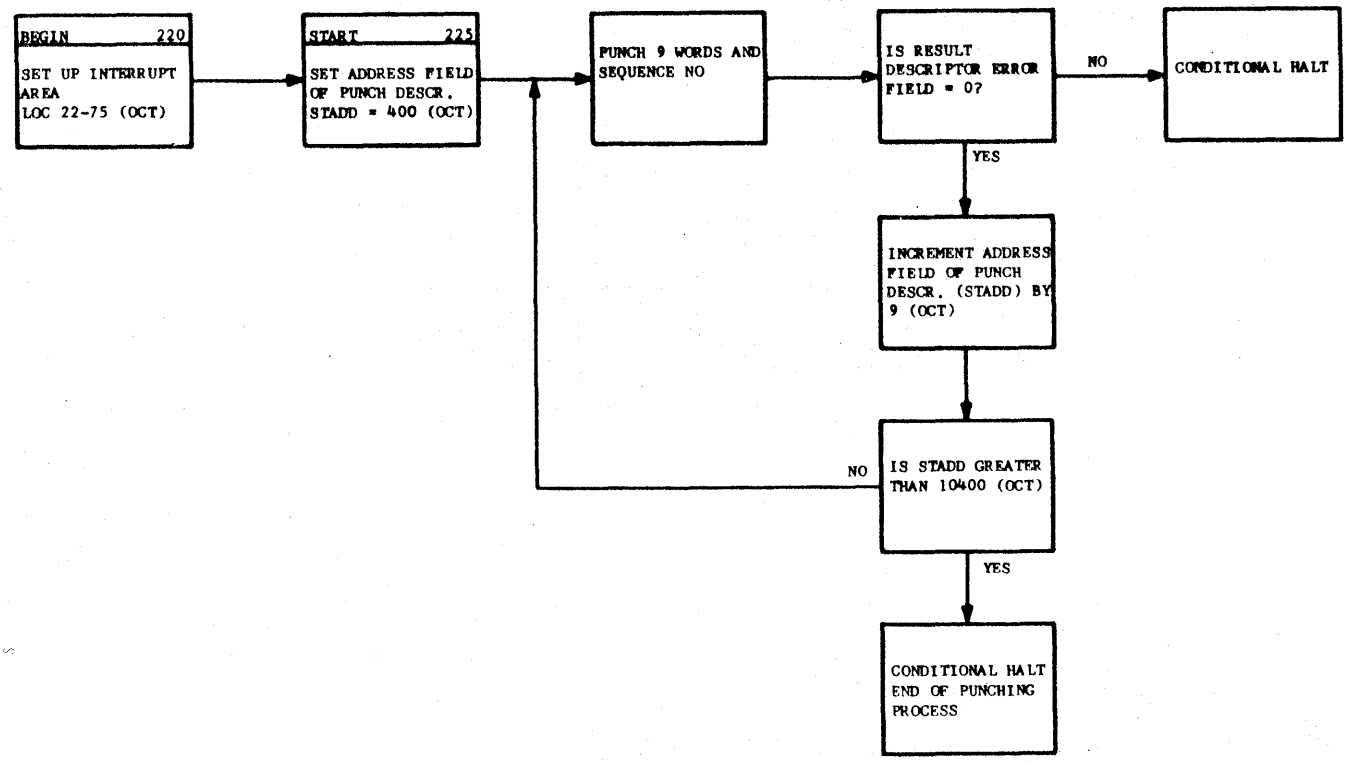
3.1 Tape to Memory Routine



3.2 Card to Memory Routine



3.3 Memory Punchout Routine



4. APPENDIX

Recreation of Magnetic Tape

For recreation of the Basic Test part of the magnetic tape, do the following for each Test Routine:

a - Read the corresponding program deck

b - Insert conditional halts (2411) in the following octal locations:

For Test Routine #1

0001-0110

0112-0121

0123-0125

0127-0137

0141-0166

0171

0200-0261

0265-0270

0277-0347

0351-0357

0361-0373

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For Test Routine #2

0000-0110

0112-0121

0123

0125-0255

0257-0261

0263

0265-0347

0351-0357

0361-0370

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For Test Routine #3

0001-0002	0221	0340
0004	0223	0342-0344
0010-0016	0225	0346-0347
0020-0026	0230	0351
0031-0046	0232-0235	0353-0356
0051-0056	0237	0360-0361
0061-0067	0242-0247	0363-0366
0073	0252	0371
0075-0077	0254	0374
0103	0256-0263	
0105-0107	0265	
0136-0144	0267-0270	
0146-0147	0272-0277	
0152-0153	0302-0303	
0156-0172	0306	
0174	0310-0314	
0203	0316-0321	
0205	0323-0324	
0207	0326-0331	
0212-0217	0333-0336	

4. APPENDIX (Con't.)

For Test Routine #4

0001-0032

0036-0061

0064-0075

0101

0103-0347

0351-0377

c - In location 0350 (octal) insert:

For Test Routine #1 0000000000002000

For Test Routine #2 0000000004401777

For Test Routine #3 0000000000001777

For Test Routine #4 0000000000007404

d - In the following locations insert:

Test Routine #1 location (octal) 6040 0000000000011005

Test Routine #2 location (octal) 6234 0000000000011005

Test Routine #3 location (octal) 3256 0000000000011005

Test Routine #4 location (octal) 5520 0000000000011005

4. APPENDIX (Con't.)

e - After the information is complete in memory for each of the Test Routines, write the contents of memory on magnetic tape in 10 records as follows:

ROUTINE RECORD SEQUENCE	BEGINNING MEMORY AREA	OCTAL RECORD LENGTH
1	400	1,000 words
2	1,400	1,000 words
3	2,400	1,000 words
4	3,400	1,000 words
5	4,400	1,000 words
6	5,400	1,000 words
7	6,400	1,000 words
8	7,400	400 words
9	0,000	400 words
10	10,000	400 words

Repeat steps (a) through (e) for all four Basic Test Routines.

TEST ROUTINE CHECKOUT RECORD

DATE	PRGMR	SYSTEM	REMARKS
12-15-64	agl	B5500 Processor, Two Memory Modules	