B700
PROCESSOR

(INCLUDES B705, B711, B771, and B772)

INTRODUCTION AND OPERATION

FUNCTIONAL DETAIL

CIRCUIT DETAIL

ADJUSTMENTS

MAINTENANCE PROCEDURES

INSTALLATION PROCEDURES

RELIABILITY IMPROVEMENT NOTICES

OPTIONAL FEATURES

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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INDEX

Page No.

INTRODUCTION AND OPERATION - SECTION I

Page No.

FUNCTIONAL DETAIL - SECTION II

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SECTION

1

INTRODUCTION
AND
OPERATION

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INTRODUCTION

The B 700 series Central/Terminal Processing Unit (CPU/TPU) is a free-standing cabinet that is the central operating and controlling element in the B 711/B 771 system interface shown in Figure I-1. This manual covers the B 705 and B 711 CPU's used in B 711 Systems, and the B 771 TPU used in B 771 Systems. The general features of the CPU/TPU, with its covers removed, are shown in Figure I-2. The CPU/TPU is a word-addressable unit with an 8 to 24 K-word memory capacity (16 to 48 K-bytes) and has a processor speed of 1 MHz.

There are expansion provisions for interfacing peripheral devices in addition to those shown in Figure I-1. Table I-1 lists the complete complement of peripheral devices and their associated I/O Controls (IOC's or DDP's) available for use in the B 711 and B 771 applications of the CPU/TPU.

GENERAL FUNCTIONAL ORGANIZATION AND CHARACTERISTICS

Figure I-3 is a general functional block diagram of the (CPU/TPU), which consists of the following major operational sections of the central system:

a. The processor section, which contains the timing, the logic and control circuitry used in arithmetic, Boolean, shifting, I/O interfacing, memory controls, and system control operations.
b. The firmware store section, which stores microinstructions in a shared core memory (microprogram memory or MPM) and the nanoinstructions in read-only integrated-chip nanoprogram memory (NPM).
c. The Data/Program Memory (DPM) section, which stores data and user programs in the remainder of the shared core memory.
d. The I/O control or DDP section, which consists of the elements used in interfacing and controlling the peripheral devices used in the system. This section also includes the load interface for the peripheral device used as system loader.
e. The system power section, which provides and controls regulated operating voltages for the system.
f. The Field Engineering (FE) control section, which provides test capabilities to isolate system malfunctions.

The B 700 CPU's or TPU's are unlike conventional processors in that the basic logic operations are organized into controlled building blocks external to the processor section. The logic in these building blocks is not like the normal hard-wired control logic used in conventional processors. Instead, the control logics are replaced by control signals generated by the firmware store section. This approach adds a great deal of flexibility to the processor and utilizes a minimum amount of hardware.

PROCESSOR SECTION

The processor section is the major section of the CPU/TPU and performs operations defined by the program stored in the firmware store section under the control of microcodes and nanocodes. The processor section is subdivided into five units: the logic unit, the memory control unit, the control unit, the clock generator, and the external operation controls (EO).

LOGIC UNIT

The Logic Unit (LU) performs the shifting, arithmetic, and logic functions; provides a set of scratch-pad registers for temporary data storage; and provides the registers for the data interfaces to and from the device dependent ports and S-level memory (DPM). The elements comprising the logic unit are described below.

A Registers (A1, A2 and A3)

The A registers are 16-bit registers used for the temporary storage of data being transferred from the Barrel Switch (BSW) to the adder. Any or all A registers may be selected for input from BSW. The registers serve as a primary input to the adder and are individually selectable.

B Register

The B register is a 16-bit register which provides the primary interface from both S-level (data/program) memory and the device dependent ports. It serves as the secondary input to the adder, and can be used for temporary storage of certain information resulting from arithmetic operations. The only destination for this data is the adder. The nanocode allows the manipulation of the least significant bit, most significant, and/or the 14 central bits of the B-register contents upon transfer to the adder.

Memory Information Register (MIR)

The MIR is a 16-bit register used primarily to buffer information being written in memory or sent to a device. MIR can be loaded only by the barrel switch output. Output from the MIR is to main memory, a device dependent port, or to the B register.

Adder

The adder performs the arithmetic and Boolean operations on data from the B-register, literal/counter register(s), alternate microprogram count register, or base register/memory address register. Output from the adder goes unconditionally to the barrel switch but may also be sent to the B-register if so specified.

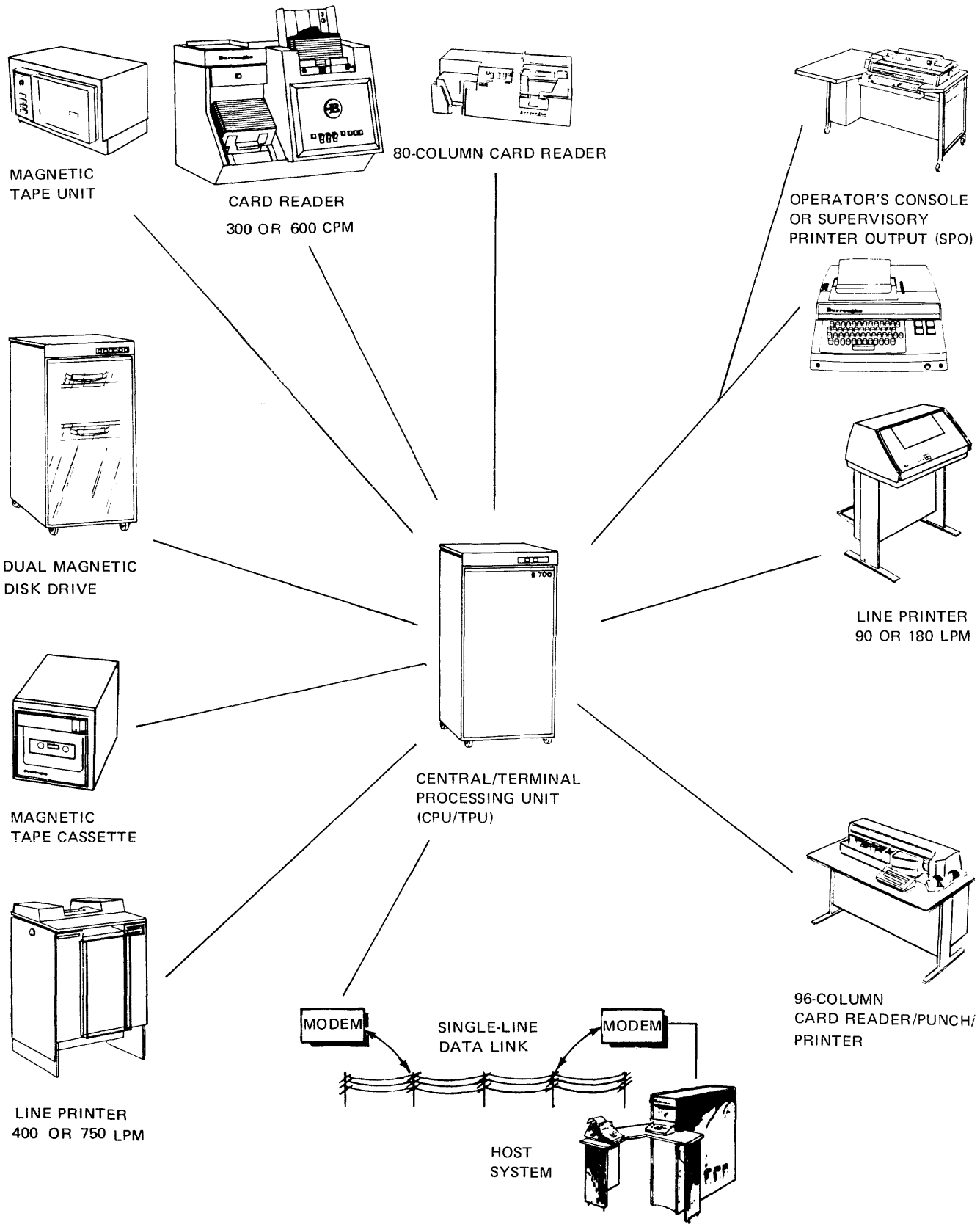


Fig. I-1 SYSTEM INTERFACE OF CENTRAL/TERMINAL PROCESSING UNIT (CPU/TPU)

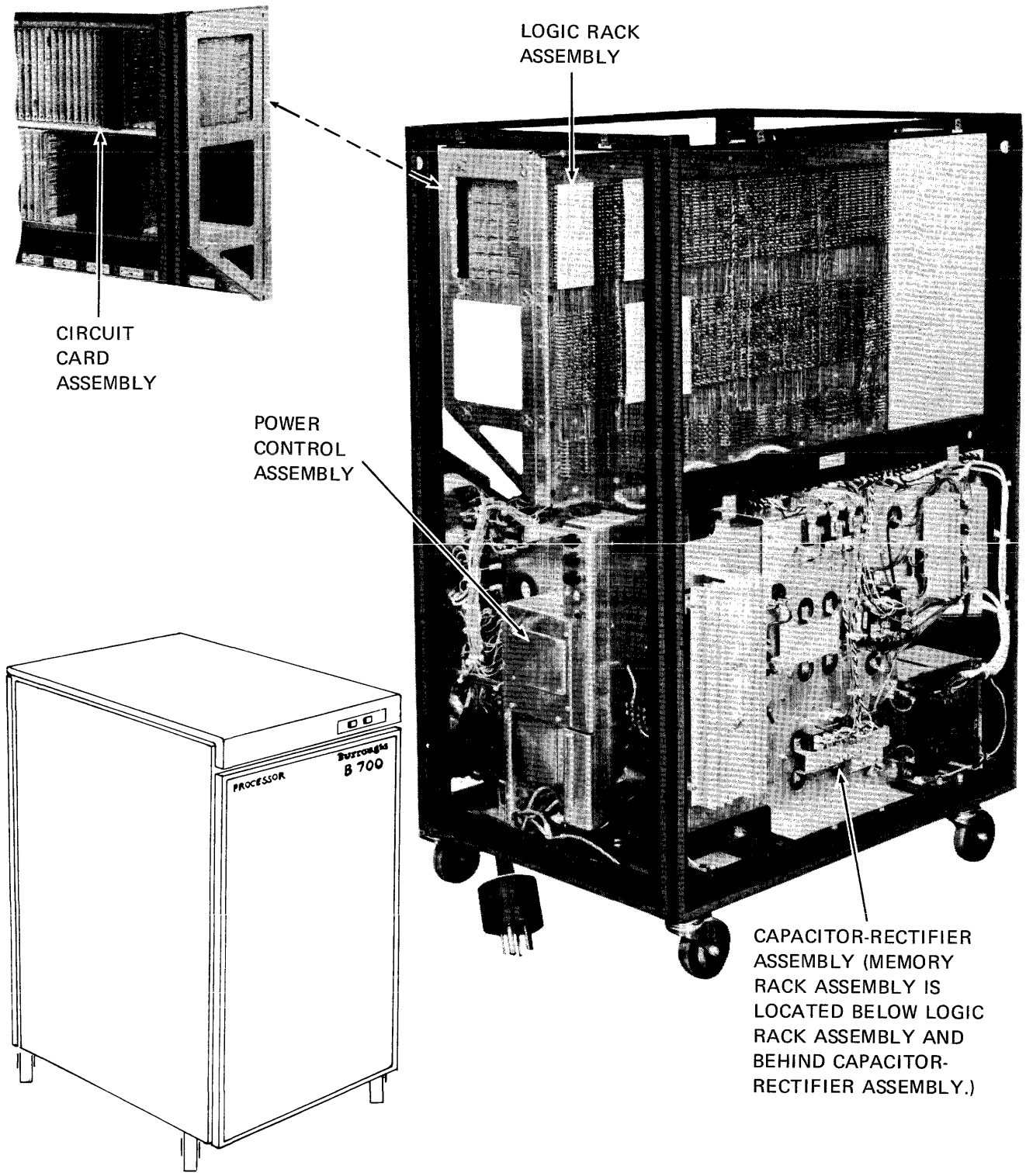


Fig. I-2 B700 CENTRAL/TERMINAL PROCESSING UNIT (CPU/TPU), PHYSICAL FEATURES

TABLE I-1. PERIPHERAL, CONTROL, AND OPTION COMPLEMENT

PERIPHERAL UNIT	ASSOCIATED I/O CONTROL		SYSTEM APPLICATION
	MODEL	PART NO.	
B 9343 Console Printer	B 043	Not Applicable	B 711
A9114 Card Reader	B 111	1448 0347	B 711
A9119 Card Reader	B 311	1448 0321	B 711
B 9115/9116 Card Reader	B 115	1449 4876	B 711/B 771
A9122-1 Paper Tape Reader (PPT/EPC)	B 121	1448 9181	B 711
A9222-1 Paper Tape Punch (PPT/EPC)	B 221	1449 0296	B 711
A988 Line Printer	B 245	1448 0404	B 711
A/B 9247-x Line Printer	B 244	1448 0362	B 711/B 771
A/B 9249-x Line Printer	B 243	1448 0388	B 711/B 771
A9491-2 Magnetic Tape Unit	B 391	1448 2228	B 711
A/B 9490-25 Magnetic Tape Cassette	B 392	1448 8654	B 711/B 771
A9419-x Reader/Punch/Printer	B 311	1448 0321	B 711
B 9418-2 Reader/Punch/Recorder	B 418-2	1448 0321	B 711/B 771
B 9344 Supervisory Printer Output (SPO)	B 44	1449 4884	B 771
A/B 9480-xx Disk Cartridge Drive	B 489	1448 0313	B 711/B 771
Single-Line Data Communications Link	B 351	1449 5709	B 771
A9481-xx Dual Disk Cartridge Drive	B 489	1448 0313	B 711/B 771

Barrel Switch (BSW)

The Barrel Switch (BSW) is a matrix of gates used to shift a parallel input data word a number of places left or right, end-off, or end-around. The shift amount is specified by the contents of the Shift Amount Register (SAR). Data input to the barrel switch is from the adder. Destinations are the A registers, B register, memory information register, alternate microprogram count register, memory address register, either base register, or the shift amount register.

MEMORY CONTROL UNIT

The Memory Control Unit (MCU) is used primarily for memory and device addressing. The elements comprising the MCU are described below.

Microprogram Count Register (MPCR)

The MPCR is a 14-bit register which contains the instruction address for the microprogram. MPCR contains the current instruction address except when an "EXECUTE" instruction is performed. MPCR can be loaded by a type II instruction or with the output of the incrementer. MPCR output goes to both the incrementer and the AMPCR.

Alternate Microprogram Count Register (AMPCR)

The AMPCR is a 14-bit register which contains the jump or return address for program jumps and subroutine returns within microprograms. The address is one less than the position to be jumped to and two less than the position to be returned to. AMPCR can be loaded from MPCR, from the 14 LSB of the barrel switch, or by a type II microinstruction fetch from microprogram memory. AMPCR output goes to the incrementer.

Incrementer

The incrementer adds 0, 1 or 2 to the selected input from either MPCR or AMPCR. The output of the incrementer is the input to the MPCR and also provides an address to the microprogram memory. The MPAD address controls select both the input source and the amount to be incremented.

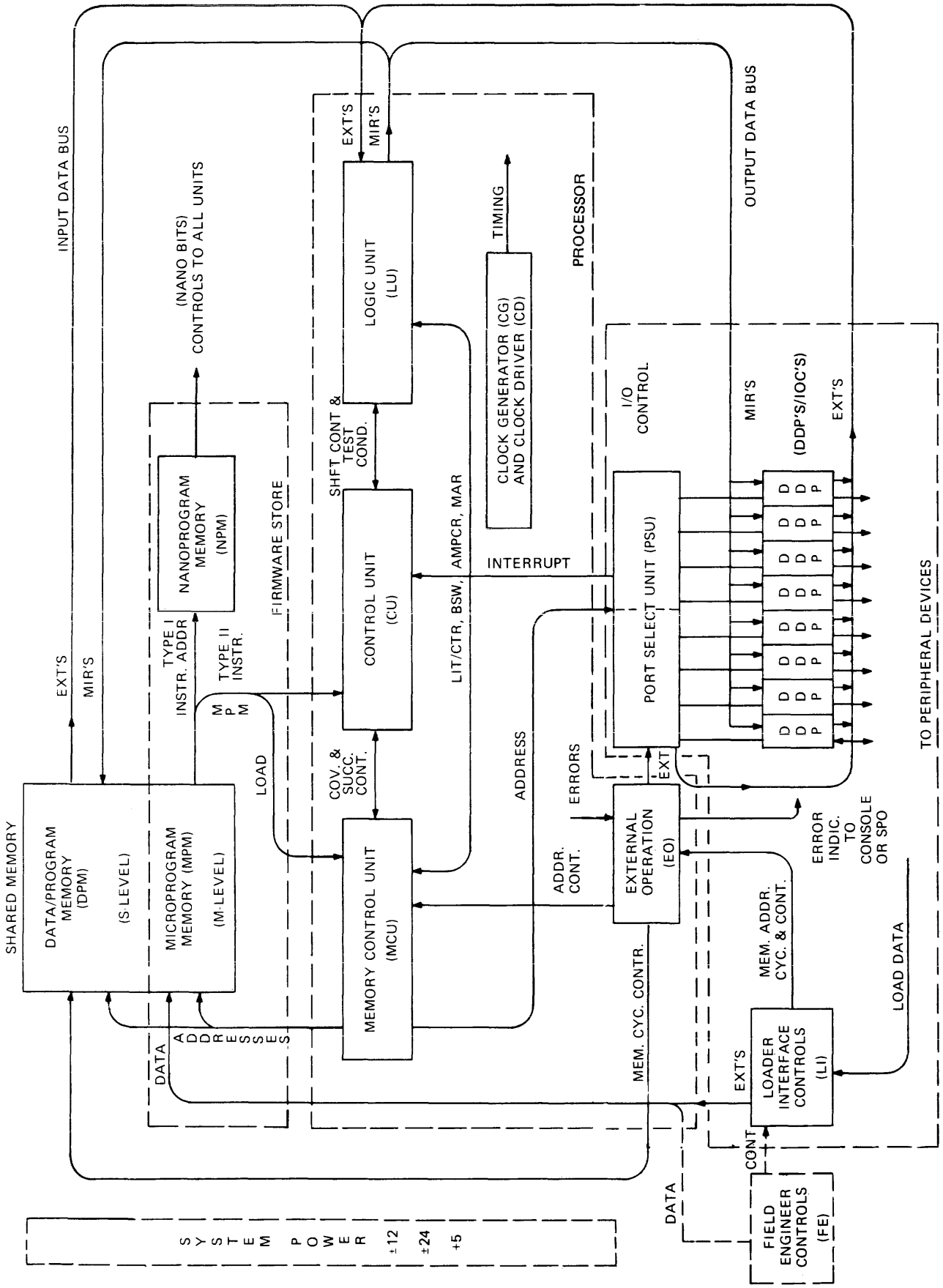


Fig. I-3 B700 CPU/TPU FUNCTIONAL BLOCK DIAGRAM

Microprogram Address Controls (MPAD)

The MPAD controls are used to control the loading of MPCR and AMPCR, the selection of MPCR and AMPCR input to the incrementer, and the selection of the value (0, 1, or 2) to be used in incrementing. The selection of controls and a true or false successor (testing for alternative actions) is done during phase 1 of the microinstruction and involves the results of condition testing and successor determination associated with bits 1 through 16 of the nanoinstruction. If a type II microinstruction is executed, the controls for a step successor are forced.

Memory Address Register (MAR)

The MAR is an eight bit register which holds the eight LSB of a memory address. MAR is concatenated to either base register 1 or base register 2 to form the absolute address. MAR may be loaded from either the least significant byte of the barrel switch or from the literal register. The output is to S-level memory. The MAR along with the currently selected concatenated register may also be sent to the adder.

Base Register 1 (BR1)

Base register 1 is an eight-bit register which holds a device address or the base address of a 256-word block of memory data. When used for a memory address, BR1 is concatenated with MAR to form an absolute memory address that is transferred by the output select gates to S-level memory. The concatenated registers may also be sent to the adder.

When used to hold a device address, (BR1 is interfaced by the output select gates to the port select unit, where it is used to address the DDP to be used. The input to BR1 is from the most significant byte of BSW. Once placed in the selected mode by a memory/device command, BR1 remains selected until a command is issued selecting BR2.

Base Register 2 (BR2)

Base register 2 functions exactly like BR1, thus providing a second register for holding memory/device addresses. Once placed in the selected mode by a memory/device command, BR2 remains selected until a command is issued selecting BR1.

Output Selection Gates (OS)

The output selection gates select the specific source (BR1/MAR or BR2/MAR) of S-level memory or device addresses. A Read/Write "1" command selects BR1/MAR; whereas, Read/Write "2" selects BR2/MAR. If no source is specified, the register selection remains unchanged. OS output is to the port select unit and/or to the adder.

Counter (CTR)

The CTR is an eight-bit counter used for loop control and other counting functions. CTR is loaded via the MAR/CTR selection gates from either the literal register or the least significant byte of the barrel switch. CTR can be used as an input to the adder, right-justified with zero fill. A counter overflow results in setting the Counter Overflow flag (COV) in the control unit condition register; COV is reset either by testing the bit or by loading the counter with a new value.

Literal Register (LIT)

The LIT is an eight-bit register used as temporary storage for literals in the microprogram. LIT is loaded from microprogram memory using a type II microinstruction. LIT may be used as an input to the adder, left-justified with zero fill, and/or via the MAR/CTR input selection gates to either the counter register or the MAR.

MAR/CTR Input Selection Gates

The selection gating consists of eight bits and is used to select an input to the MAR from either the LIT register or the low-order eight bits of BSW. These functions are mutually exclusive.

Control Register

The control register is a 40-bit register used to store all control signals from the nanomemory that are not used in phase 1. Certain control signals are decoded before being strobed into the control register while others are decoded on output. Gate delays introduced into the control signal sequence determine whether the coding is done before or after the register. The register includes both MPAD controls and phase 3 controls and thus contains their respective clock gating networks. The control register is physically contained in the MCU but distributes nanocontrols to all sections of the processor.

CONTROL UNIT

The Control Unit (CU) performs two main control functions: CU is used for shift amount control and for the storage of condition indicators, data and status interrupts, and status indicators. The control register, located within the MCU, distributes nanocontrols throughout the processor. The elements comprising the control unit are described below.

Shift Amount Register

The shift amount register and its associated logic is used to control the loading of shift amounts and the sequencing of shift operations. (Refer to barrel switch description for details.)

Condition Bits

The condition register has 16 selectable condition bits, only one of which may be selected and tested by a nanoinstruction. If an attempt is made to reset and set a condition bit at the same time, the set will dominate except on counter overflow (COV), in which case the reset will dominate.

CLOCK GENERATOR AND CLOCK DRIVER

The Clock Generator (CG) contains a 10-MHz oscillator and a divider which produce the 1-MHz system clock (S-clock), that is a 50 nanosecond pulse every microsecond. The S-clock is distributed throughout the processor, except to the logic unit. The logic unit is clocked by phase 3 clock (3-clock), derived from S-clock. The main function of the phase 3 clock is to inhibit destination register selection during an extended phase 3 condition; these registers are clocked upon phase 3 completion. A third set of controls on the CG board is used for generating the clear signals to the processor elements. The Clock Driver (CD) contains drivers for clock pulse buffering and distribution.

EXTERNAL OPERATION CONTROLS (EO)

Memory and device operations are mutually exclusive due to the fact that both share common input busses. The selection of either memory or a device is controlled through the decoding of nanobits. These bits, which are sent to a holding register in the EO controls, specify whether a memory operation or a device operation is to take place, define the function that is to be performed, and select the base register to be used in the addressing operation. If a memory read or write operation is indicated, the command is fully decoded, and the appropriate interface signals are generated to the memory.

Device read and write operations are decoded before being sent to the port selector, where they are buffered and gated so as to cause the device operations to be terminated at the proper times. However, the Address/Status Request (ASR) signal is decoded directly from the nanobits and sent to the port selector as a separate signal without gating. This is to allow immediate enabling of the status word lines to the external bus since the status word is returned to the processor in the same clock time.

The error indications held by EO have the following meanings:

a. Memory loader parity read error detected in the media data during read-in of data from memory loader to microprogram memory.
b. MPM parity error detected in the MPM portion of shared memory.
c. Read-after-write MPM parity error detected during load on microprogram memory read-after-write check during loading from console paper tape reader.
d. DPM parity error detected in the DPM portion of shared memory.
e. NPM parity error detected in nanoprogram memory word.
f. Memory address limit error exceeds memory limit register setting.

FIRMWARE STORE SECTION

The firmware store section, utilizing core memory for microprogram storage and ROM IC chip memory for nanoprogram storage, contains the necessary systematic controls for the processor section. Core memory is also used for data/program storage; therefore, the address and data control is accomplished by shared memory controls. (Refer to data program memory section.) The microprogram core memory (MPM) outputs are called microprogram codes and are actual 16-bit instructions. (See Figure I-4.) The instructions are classified as either type I for nanomemory addressing or type II for loading specific registers within the processor section. The nanoprogram memory (NPM) outputs are called nanocodes and are actual 55-bit instructions. (See Figure I-4.) Nanoinstructions have three major classifications: (1) no conditional logic, (2) conditional logic met, and (3) conditional logic not met.

Correct parity is generated when writing and checked when reading in microprogram memory storage with bit 17. Bit 56 in nanoprogram memory storage is used to check parity when reading nanocodes. Odd parity is used for MPM and NPM.

DATA/PROGRAM MEMORY SECTION

The Data/Program Memory (DPM) section is that portion of core memory which is controlled by shared memory logic in conjunction with external operations and contains user type data and S-level programs.

SHARED MEMORY CONTROLS

Microprogram memory and S-level memory share the same physical memory in the B 705, B 711 and B 771. The shared memory (SM) controls are used for addressing both segments of memory and for transferring data to/from memory.

The size of shared memory ranges from a minimum of 8,192 words (16,384 bytes) to a maximum of 24,576 words (49,152 bytes) when all memory options are exercised. Extensions to memory are in physical increments of 4,096-word (8,192-byte) or 8,192-word (16,384-byte) modules. A hardware address limit is provided which allows setting the size of "addressable" memory in 2,048-word (4,096-byte) increments; the specification of a memory address in excess of the address limit will result in an error condition.

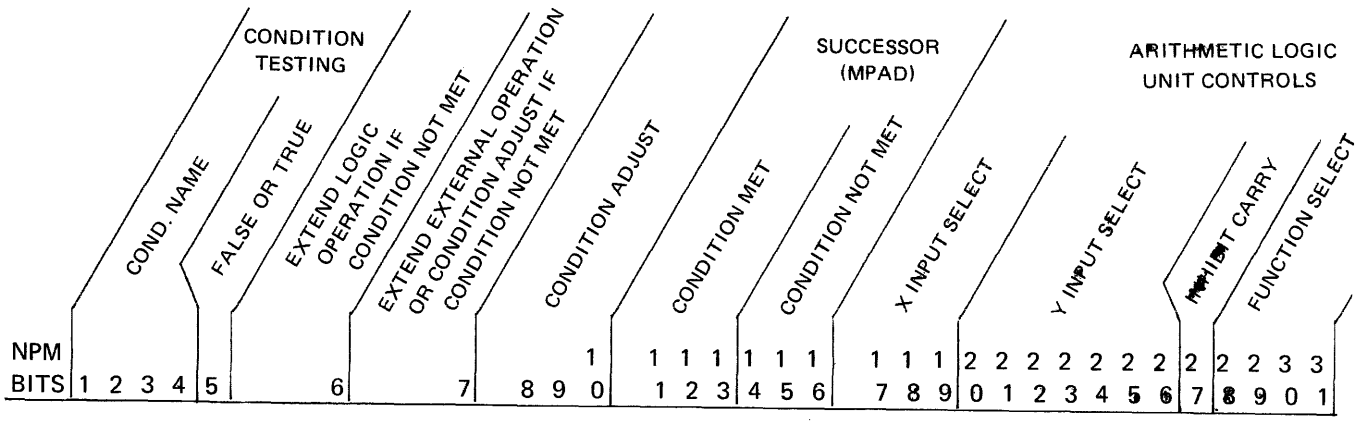
MICROPROGRAM CODES

MPM BITS

1 2 3 4 5 6 7 8 9	10 11 12 13 14 15 16	17
0 0	AMPCR	PARITY BIT
0 1	MPCR & INCR	
1 0	MPCR & INCR	
1 1 0 0	SAR	LIT
1 1 0 1	SAR	0 0 0 0 0 0 0 0
1 1 1 0 0 0 0 0		LIT
1 1 1 1	NANOADDRESS	

0 = UNUSED

NANOPROGRAM CODES



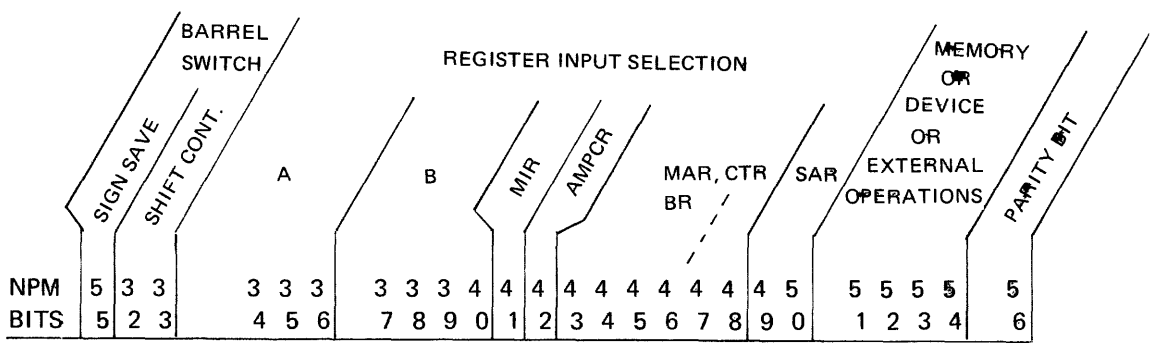


Fig. I-4 MICROPROGRAM AND NANOPROGRAM CODES

The hardware address limit is a wired-in value initially set at the factory. Any change to this value requires rewiring of the address limit in the backplane. (Refer to Section VIII.)

Because the memory is shared by S-level and MPM, provisions are made for addressing the two segments separately. The memory controls contain selection gating for accepting the memory address from either the BR/MAR (for S-level memory) or from the incrementer (for MPM memory), as determined by the appropriate memory controls. Up to a maximum of 16,384 words (32,768 bytes) of the shared memory may be reserved for MPM, depending on the requirements of the microprogram. The division between S-level and MPM is soft, allowing the upper limit of MPM to be varied at the discretion of the system software designer.

S-LEVEL MEMORY OPERATION

Addressing of S-level memory is accomplished by use of an external operation command which specifies a memory read or write operation. In this case the external operation controls enable the appropriate control signals, causing the next memory address to be taken from output select lines 1 through 16. Data being written to S-level memory is transferred via the SM controls from the MIR bus of the processor. Data read from memory goes only to the B register of the processor via the SM controls and the external bus. All data transfers to/from S-level memory are in 16-bit parallel. Parity is generated for all words written into memory and is checked on all words read from memory.

I/O CONTROL SECTION

The I/O control section is the interface for communciation between peripheral devices and the processor. The I/O control section is also referred to as the DDP section. The I/O control section is subdivided into three units: the port select unit, the I/O controls, and the loader interface controls.

PORT SELECT UNIT

The Port Select Unit (PSU) interfaces two groups of four I/O Controls (IOC's) or Device Dependent Ports (DDP's). It receives the device address from the base registers. Interrupt priority is established on all unaddressed devices by producing the device address on the status EXT's. Input or output control for devices is established here.

I/O CONTROLS OR DDP'S

The I/O control section contains up to eight DDP's, which are also referred to as I/O Controls (IOC's). Wherever possible the I/O control arrangement within the CPU/TPU cabinet is such that any of the different types of I/O's can occupy any I/O position. Some exceptions would be the B 705/711 Console Control, B 771 Single Line Controls, B 771 Supervisory Printer Control, and the B 771 Card Reader Control. Some other I/O control location limitations would be interrupt priority considerations. Position 8 has highest; postion 1 has lowest priority. System installation procedures specify priority needed for system configurations. Non-standard I/O controls are those that exceed four cards. Each I/O control is designed to interface the external device by converting levels, interpreting signals, converting data bit serial to bit parallel and vice versa, syncronizing timing, and buffering data.

The firmware selects a device for access by sending to the PSU the device address contained in the base register (BR1 or BR2) pointed to by the read/write command. This binary address, sent via the output select (OS) gates, defines the device DDP to the port selectors, as shown in Figure I-5.

The most significant bit of the address is used by each I/O control to specify control or data word format. (NOTE: Control format on a device read is status information.) Input information to the addressed I/O control comes from the processor section MIR. Output information from the addressed I/O control EXT's 1-16) is made available only to the B register in the processor section.

Interrupts are always sent from the I/O controls to the port selector, even though the control may not be addressed. Interrupts from unaddressed I/O controls are an Input Request (IRQ) to the processor-section control unit from the highest priority device and are generated by either Status Interrupt (STINT) or Data Interrupt (DINT). Handling of the interrupt condition is the responsibility of the firmware store program. The program must issue an address status request command, placing the reason for interrupt from the I/O control on the EXT's along with the address of the I/O control position from the port selector. Interrupts from addressed I/O controls to the processor-section control unit are an unsolicited request (URQ) for a Status Interrupt (STINT) and a solicited request (SRQ) for a Data Interrupt (DINT). Handling of these interrupts is also the responsibility of the firmware store program. One of the peripheral devices (usually the card reader or console memory loader) is designated as a Firmware Store Loader.

LOADER INTERFACE CONTROLS

Loader Interface (LI) Controls permit data to be sent directly from loading device I/O control to microprogram core memory input to write one word at a time including generated parity bit. The words are written sequentially up through core memory when the load switch is enabled on CPU/TPU cabinet.

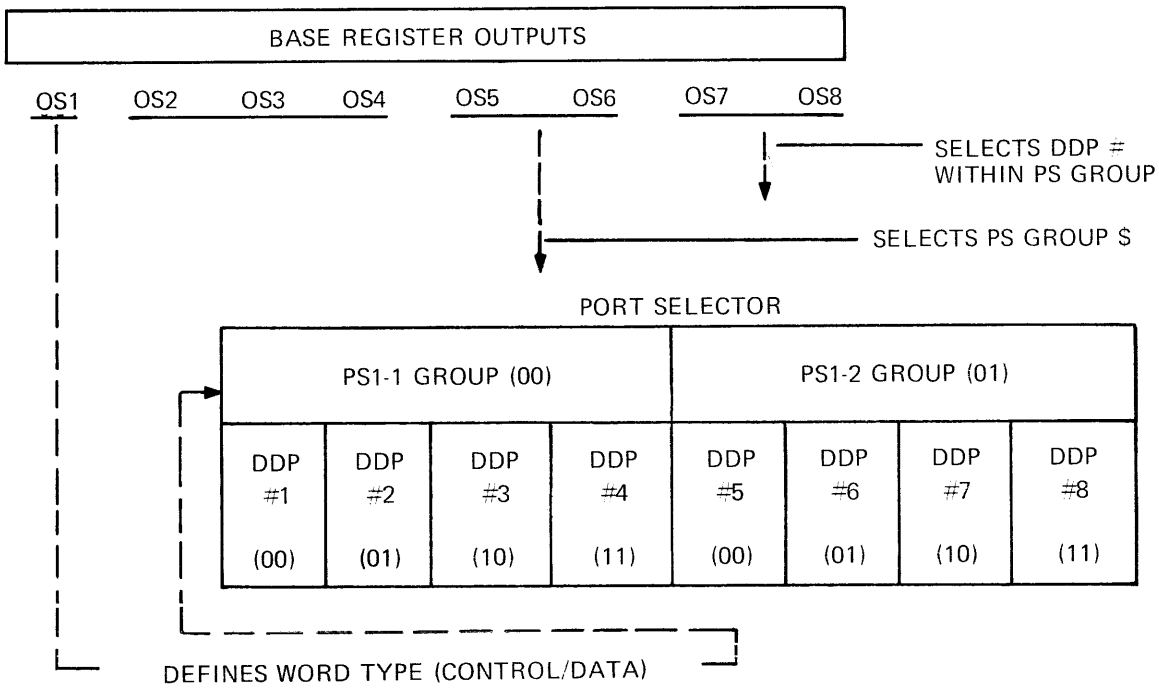


Fig. I-5 DDP SELECTION

SYSTEM POWER SECTION

The CPU/TPU receives its input power directly from the facility-supplied power source, and through the internal power distribution, the CPU/TPU provides power to all connected system peripherals. There is different power distribution circuitry for domestic international units to compensate for power supply frequency and voltage variables on international systems.

The AC controls provide the means for properly sequencing the power on and off functions. Part of this sequence is the control of the core memory data save input. For normal turn-on/turn-off operations, the memory cycle initiate is inhibited and the data save input is controlled to ensure preservation of the core memory contents.

FIELD ENGINEERING CONTROL SECTION

The Field Engineering cards (FE1 through FE4) are used by the field engineer to isolate system malfunctions. They provide for two modes of operation: (1) a memory test mode which is used to establish confidence in and/or troubleshoot the MPM/NPM portions of memory, and (2) an MTR mode which is used to isolate system malfunctions other than in the MPM/NPM memory. Section V discusses each mode of operation and describes the functions provided by the operator controls including the arrangement of controls and indicators on the FE cards.

Card slots are wired into each CPU to accept the FE cards; however, the cards themselves are not always installed in the equipment. These cards are part of the standard test equipment provided for the sites.

OPERATIONAL DESCRIPTION AND APPLICATIONS

In CPU applications, the firmware is the interpreter of the user program. The user program consists of macroinstructions (S-level) which are interpreted into the required sequences of microprogram steps that control the hardware through the necessary logic and arithmetic functions. In this manner, the macroinstructions of the user program are executed through firmware interpretation.

The CPU applications, the firmware is the interpreter of the user program. The user program consists of macroinstructions which are interpreted into the required sequences of microprogram steps that control the hardware through the necessary logic and arithmetic functions. In this manner, the macroinstructions of the user program are executed through firmware interpretation.

In TPU applications, the firmware is dedicated mostly to specific operations instead of interpretation of user programs. The TPU requires a data communication link to and from a central processing system, which would then be referred to as the host system. (The TPU is, in effect, a preprocessor.)

Figure I-6 is an operational-flow block diagram of the CPU/TPU. The microinstructions are stored in the microprogram memory (MPM) and are identified as either type I or II instructions. A type I microinstruction is used to address the nanoprogram memory (NPM) and select one nanoinstruction. Type II microinstructions are used to load

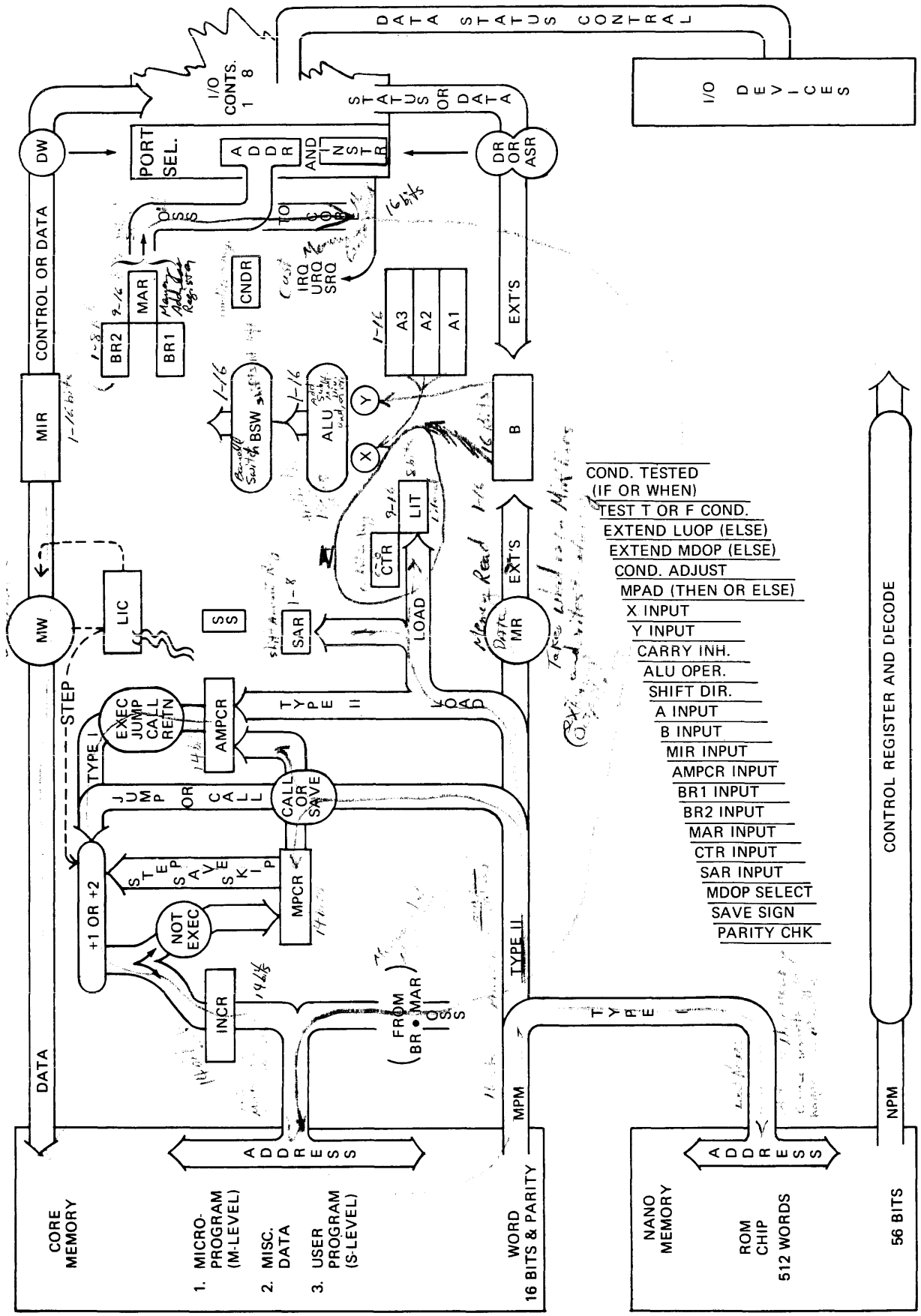


Fig. I-6 CPU/TPU OPERATIONAL BLOCK DIAGRAM

literal constants and microprogram address counts into selected registers and counters.

The means of implementing the hardware functions of a CPU or TPU is by the microcode and nanocode present at any given clock time. The nanocode has up to 512 different word combinations that are addressable from the microcode. The required flow through a firmware program is accomplished using three registers and incrementing logic. The first register, Microprogram Counter (MPCR) retains the present program address during most operations. The second register, the Alternate Program Counter (AMPCR) retains an alternate address that the program may use at some successive operation. The third register, the Incrementer (INCR) actually addresses core memory for the present instruction. The next address, the INCR would produce depends on the program's present instruction. Possibilities would be, MPCR plus one or two, AMPCR plus one or two, and also the address content of MPM plus one. The nanodecode MPAD equivalents or type II microcode equivalents determine the selection.

Each instruction, as it is addressed by the INCR, is said to be "fetched." The type I instruction cannot be executed until some successive instruction. The type II instruction is however complete on each fetch cycle. Only type I instructions have the ability to produce both fetch and execute cycles. (Basically, a fetch cycle stores nanobits in the control register, and an execute cycle uses them.) This feature makes it possible to establish, first the hardware logic function, second the loading of register values to satisfy desired inputs to the function, and third the execution of the logic function. Details of the above process are explained under "phasing" in Section II.

The user requires a microprogram so constructed that it can either interpret some intermediate program language or perform all the duties of a standard communications terminal. In either case, the microprogram must somehow be stored in core memory. The loader interface control in conjunction with the load switches and cold starting procedures are used to store the microprogram in core memory and make the hardware begin to function.

Figure I-7 is a block diagram of the CPU microprogram from the initial B7MPL statements to loading into the CPU. The systems microprogrammer constructs B7MPL statements as source information to a Medium System Computer containing a B700 microprogram language assembler. The assembler produces an output of the microprogram in compact hex code on either paper tape or cards along with a listing of the program. The following programs are generated in this manner:

a. Three types of cold start programs identifying a specific I/O device for further cold start data.
b. A disk primer for central processor applications.
c. The interpreter to implement different intermediate languages.
d. Warm start programs for central processing systems that have already had the cold start procedures completed.
e. The different Maintenance Test Routines (MTR's) for diagnosing system faults.
f. Bootstrap loader for terminal processor.
g. Stand-alone RJE program for terminal processor.

CENTRAL PROCESSING UNIT (CPU)

When cold starting the CPU; (1) the cold start program is loaded in core memory through the loader interface; (2) the cold start program loads the disk primer program from any of three different I/O devices and then it transfers control to the disk primer program; (3) the disk primer program initializes the disk cartridge in preparation for more programs and then loads the segments of the interpreter programs on the disk cartridge, including any necessary utility programs to implement loading user programs. Transfer to the interpreter program is accomplished at the end of the last loaded program. At this point, the system has completed the cold start process.

A warm start is accomplished to bring interpreter data from an already cold-started disk back into core memory. (See Figure I-8.) As in the cold start procedures, the warm start microprogram is first loaded into core memory via the load interface control in conjunction with the load switch. Second, the warm start microprogram then reads the disk cartridge interpreter data and writes it into core memory. When it is completed, the warm start microprogram transfers control to the interpreter microprogram system configuration subroutine.

After the system configuration has been introduced to the system from console keyboard following a cold or warm start, the interpreter program returns to the ready mode. In the ready mode, the interpreter has four basic options: (1) restart any user or utility program that was present in core memory; (2) load a new user or utility program from disk to core memory; (3) enter any of the system micro-utilities; or (4) enter system date.

Figure I-8 is a block diagram of a user program from the initial COBOL statements to loading into the CPU. The user or utility programs originate at applications software. The applications programmer constructs COBOL source statements to be compiled by a medium system processor. The COBOL compiler produces an S-level code output with a listing.

Any program that the user desires to execute must first be stored on disk cartridge. One of three different loader utility programs must have been stored on disk at cold start time and can now be loaded to core memory using the load function when the interpreter is in the ready mode. The header of this utility program is examined (Figure I-8, step 3) to see if any additional interpreter segments (delay binding) are needed (Figure I-8, step 4)

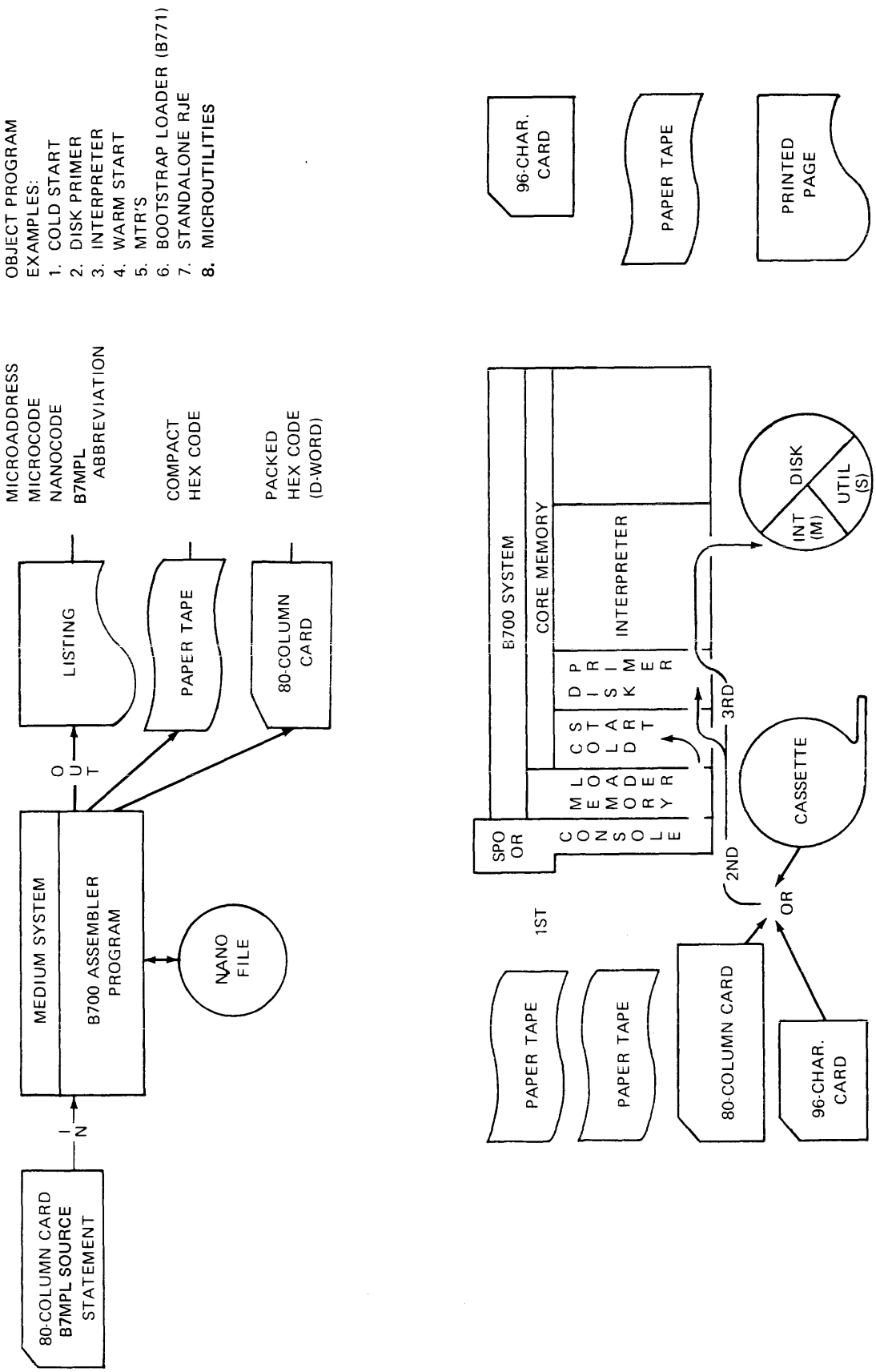


Fig. I-7 CPU MICROPROGRAM BLOCK DIAGRAM

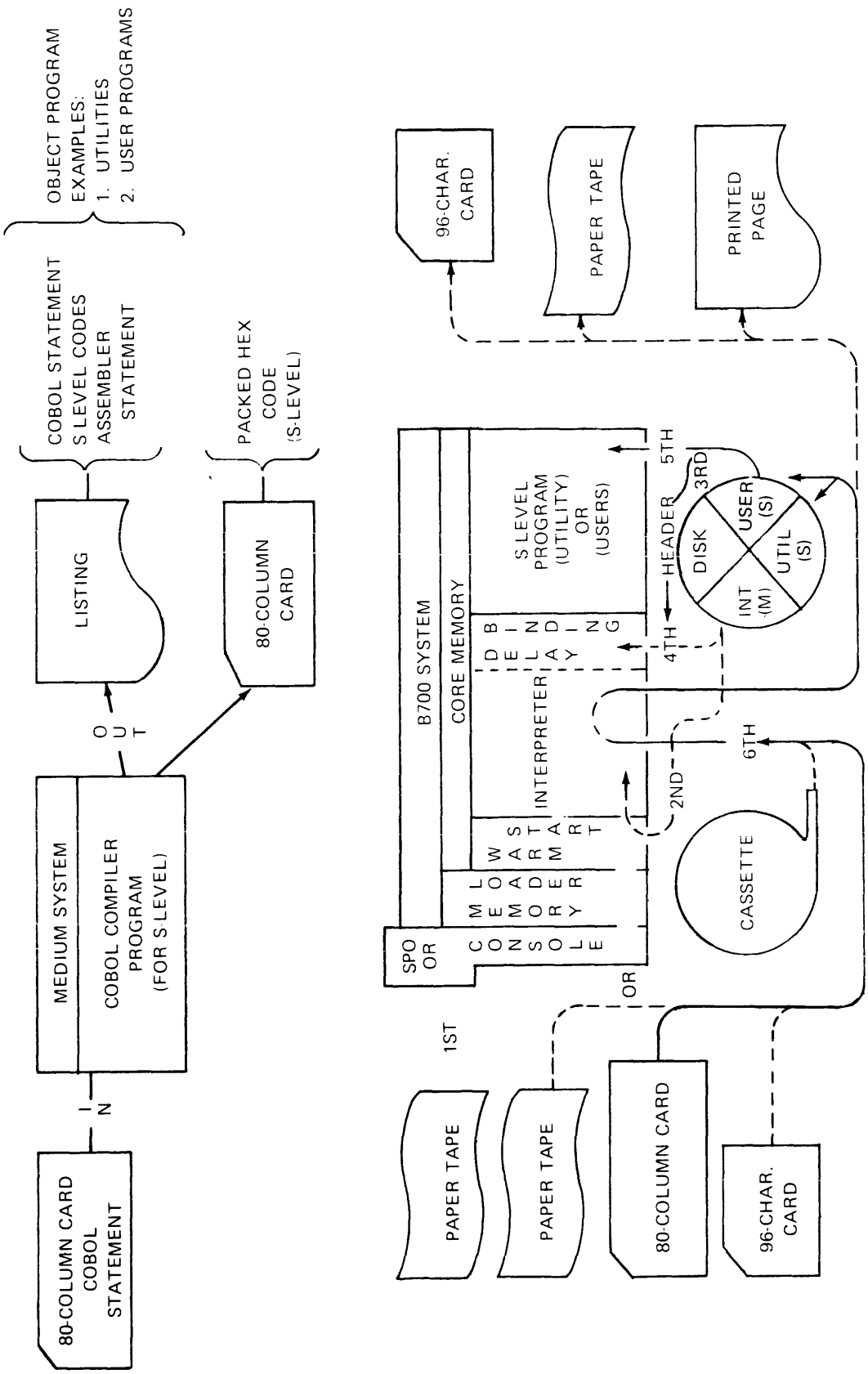


Fig. I-8 USER PROGRAM BLOCK DIAGRAM

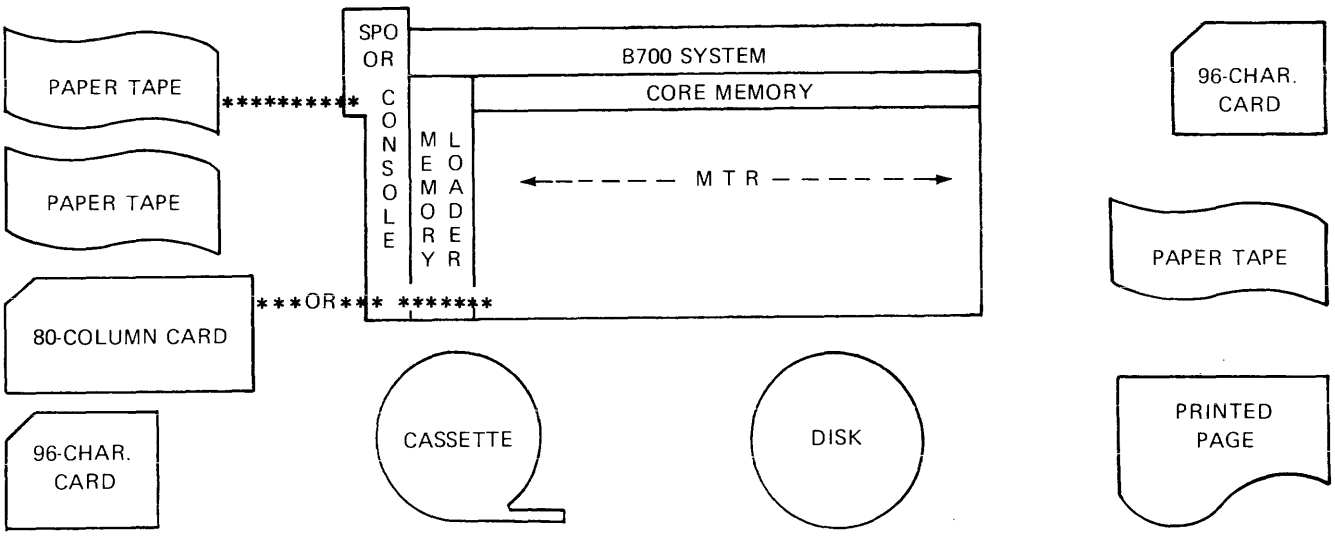


Fig. I-9 MTR BLOCK DIAGRAM

from disk to execute this new program. The S-level utility program now in core memory (Figure I-8, step 5) is examined by the interpreter to determine the different steps the interpreter program must take to achieve the results the S-level utility program desires. In the example on Figure I-8, step 6, it is desired to load additional user programs from the 80-column card I/O device to the disk cartridge. All machine functions are handled via the interpreter microprogram. Any other user or utility program to be executed would follow the same general pattern. Refer to the **System Software Operation Manual, 1067410** and **System Reference Manual, 1066198** for detailed instructions.

Figure I-9 is a block diagram of loading the MTR program into the CPU/TPU. Unlike the users utilization of the processing system, the field engineer uses Maintenance Test Routines (MTR), which are stand-alone microprograms that exercise only the hardware specified within the test routine. No interpreter program is necessary for these applications. All MTR's are loaded to the core memory via load interface control in conjunction with the load switch. At the completion of the load, control is turned over to the MTR program.

TERMINAL PROCESSING UNIT (TPU)

The TPU has two basic modes of operation: (1) Remote Job Entry (RJE) mode only and (2) (RJE) with local processing and on-board compiler. The local processing and on-board compile operation is interpretive, as described for the central processor unit. The RJE applications imply the transmission of large batches of data both to and from the central (host) system.

The purpose of an RJE system is to increase the utilization and convenience of using a central data processing system located some distance from where its input data is produced and its output data is utilized. Remote Job Entry can be an efficient and convenient method of submitting jobs from a remote work station or terminal via a data communication line into the job stream of a central or host system.

The host RJE system allows the following functions to be entered by a remote terminal in a format and sequence exactly as if the functions were entered on an input device at the host computer site:

a. Introduction of programs from a remote input device for execution by the host system.
b. Introduction of data from a remote input device for processing by the host system.
c. Dispersing of data produced by the host system to an output device on either the initiating or requesting remote job terminal and/or the host system.
d. Monitoring and controlling of programs on the host system via a remote supervisory console.

Figure I-10 is a block diagram of loading the RJE microprogram into the TPU. When cold starting the TPU, (1) the bootstrap loader program is loaded into core memory through the loader interface (memory loader), and then (2) the bootstrap loader loads the RJE microprogram, the data communications line parameters, and the system configuration specifications. Control is then turned over to the RJE microprogram for on-line and off-line utilization of hardware. The cold start process must be repeated if it is desired to change the parameters or the system configuration. Refer to the B 771 Software Operational Guide for details.

NOTE

The Maintenance Test Routines (MTR's) are handled the same as in the CPU application.

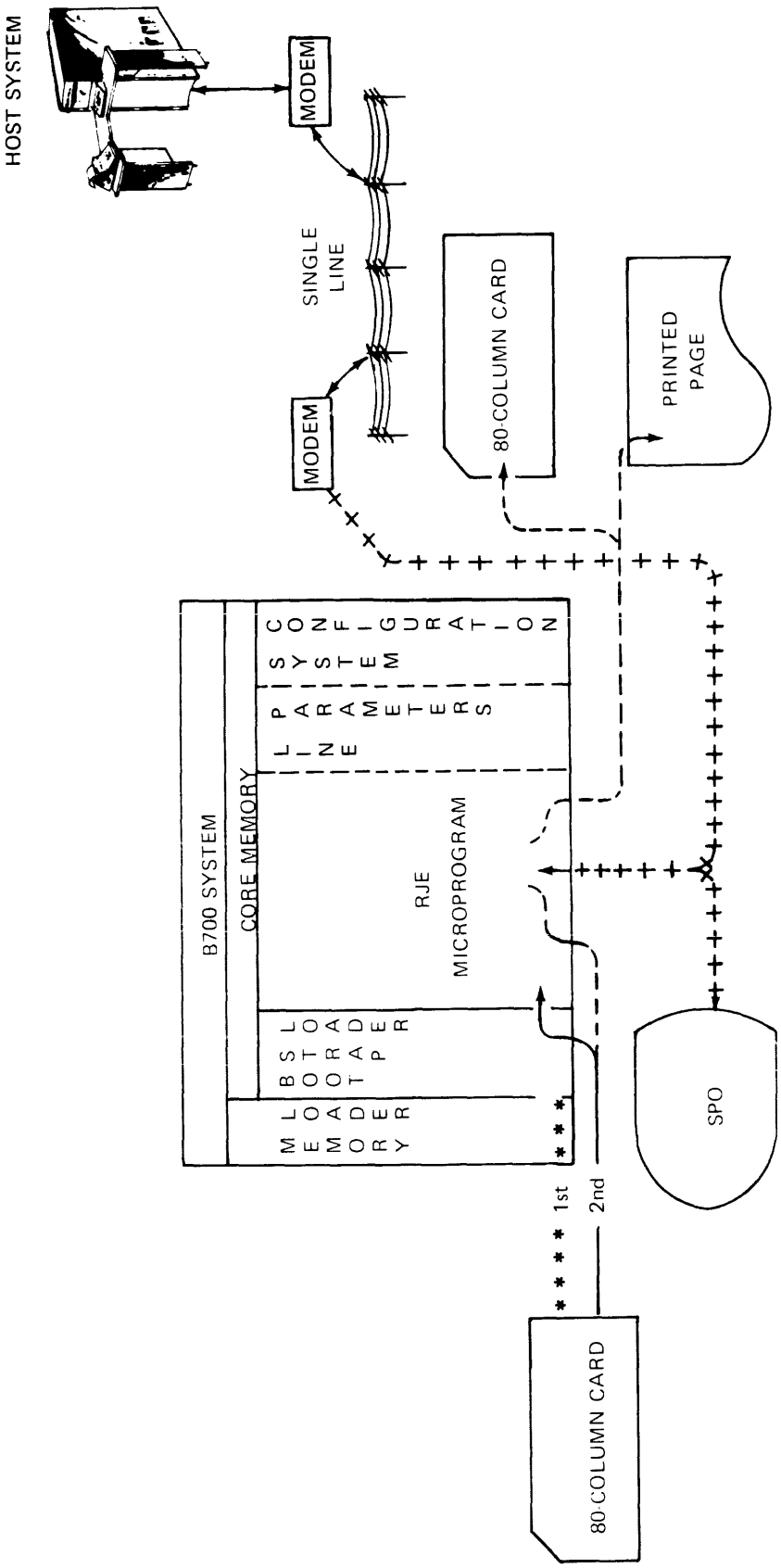


Fig. I-10 TPU RJE MICROPROGRAM BLOCK DIAGRAM

GLOSSARY OF TERMS AND SYMBOLS

The glossary of terms and symbols is divided into three parts. The first part lists the abbreviations, acronyms, and terms that apply to the system. The second part lists the logic signal prefixes, and the third part lists the logic signals of the processor. The logic signal prefixes indicate the logic section of the processor that generates the signals.

ABBREVIATIONS, ACRONYMS, AND TERMS

Building Block	The primary functional units of an interpreter-based system configuration.
B7MPL Assembler	A program utilizing English written source statements to produce binary patterned code for micromemory and/or nanomemory as its object output.
B7MPL Source Language	B700 Microprogramming Language. A set of abbreviated English statements used as source to the B7MPL Assembler.
Central Processor Unit (CPU)	The central main-frame unit in a B 705/B 711 System.
COBOL	Common Business Oriented Language used as a source language for compiling S-level programs.
Compiler Program or Assembler Program	A manufacturer-furnished program capable of translating a symbolic coded program (such as COBOL or FORTRAN) into machine code (machine executable statements). The input data to a compiler (symbolic coded program) is called the source program (source deck if cards), and the output data is code (machine executable statements) called the object program.
CPM	Synonomous with DPM central processor memory or data program memory.
Data/Program Memory (DPM) (also "S" memory)	Provides storage for data and conventional program in an emulation application and functions similarly to the main memory modules of a conventional computer system.
Device	Peripheral equipments such as, disk files, disk pack drives, magnetic tape units, high-speed line printers, card readers, etc., and various sensors usually found in special data processing applications. The function of devices is to provide the unique input/output medium for each system application.
Delayed Binding	The non-commitment of resources until the actual need for these resources arises. Binding occurs at program load (from disk) time.
Device Dependent Port (DDP) or (IOC)	The device dependent port (DDP) or input/output control (IOC) permits any device to be interfaced with a port selector. This is accomplished by providing specific device electrical interfacing such as, logic level conversion, line driver/receiver capability, and timing and synchronization when required (as in the case of disk files, disk pack drives, and magnetic tape units).
Disk Directory	A table on disk pointing to the location of each file in a disk subsystem or disk pack. To avoid wasting disk space the directory grows as necessary.
End-Around Shift	A right shift operation in which the bit or bits which would be shifted out of a register are reinserted into the more significant end.
End-Off Shift	A shift operation in either the left or right direction, in which the bit or bits shifted out of the register are lost. Vacated bit positions may be automatically filled with zeros.
Emulate	Imitate another system or machine's hardware registers and machine language structure.

Fatal Error	Errors that will impare the proper functioning of a system. Such as: Hardware, Address Limit, or I/O errors. Fatal errors provide alert alarm, print, display, and program halt.
Firmware	The firmware consists of the combination of microinstructions and nanoinstructions which are contained in the firmware store (Microprogram Memory and Nanomemory).
Firmware Program	The firmware program refers to one or several microprograms which constitute a fully operational program.
Firmware Store	The firmware store refers to the Microprogram Memory (MPM) and the Nanomemory (NPM) which contain the microinstruction and nanoinstructions.
Host System	The primary system in a multi-system or subsystem network.
Input/Output Controller (IOC)	Same as device dependent port (DDP).
Interpreter	A firmware program capable of emulating another machine's instruction set.
Katakana	A Japanese business-oriented character set.
Large Scale Integration (LSI)	The implementation of more than 100 bipolar logical gates in a single integrated circuit chip.
M-Level Language (M-Language)	Microlanguage, the language that is used for developing microprogramings.
Medium Scale Integration (MSI)	The implementation of 20 to 100 bipolar gates in a single integrated circuit chip.
Microinstruction (M-instruction)	A discrete instruction, which is contained in the Microprogram Memory (MPM) of the processor unit, that performs a set of basic functions in parallel. A microinstruction is comprised of a unique set of microcodes and may contain a constant (literal) or an address of a nanoinstruction in nanomemory. A Type I microcode specifies an address of a nanoinstruction in the Nanomemory. A Type II microcode specifies constant values to be loaded into the Shift Amount Register (SAR), Alternate Microprogram Count Register (AMPCR), Literal register (LIT), or both the SAR and LIT registers, also includes MPCR and INCR.
Microprogram (M-program)	A microprogram is comprised of a set of microinstructions or microsequences.
Microsequence (M-sequence)	A sequence of microinstructions that performs a basic function.
Microprogram Memory (MPM or M memory)	The Microprogram Memory (MPM) is one of the major functional units of the processor unit which stores microinstructions that characterize the actual or virtual machine for a given application. The MPM can be implemented as a read-only memory (ROM) or as a read/write memory (RWM).
Nanocodes	A set of 56 code bits that provide control of the desired logical function within the processor unit.
Nanoinstruction	A single instruction stored in the nanomemory of the firmware store, the contents of which constitute 56 unique nanocode signals for controlling the hardware logic of the processor unit.

Nanomemory	The nanomemory is one of the major functional units of the processor unit that stores 56 specific enable signals (nanobits).
Overlay Area	A reserved area in memory for placing additional segments of a program that would normally be too large to be placed in memory all at once.
Program Generator	This is a program capable of generating complete programs according to specifications received from the programmer.
Read-Only Memory (ROM)	A memory that stores data not alterable by program instruction.
RPG	Report Program Generator. (See program generator.)
S-Instruction	A primitive instruction which emulates a machine instruction in a conventional computer.
S-Level Language (S-language)	A language equivalent to the assembly or object language in a conventional computer, such as: source language, advanced assemblers, basic assemblers, and machine language.
S-Memory	The memory which contains the S-programs that are executed and the data on which these S-programs operate. The S-memory is also referred to as SM.
S-Program	A named set of S-instructions.
SPM	Scratch pad memory. A variable area in memory defined by the users program.
SPO	Supervisory printer output.
Small Scale Integration (SSI)	The implementation of 5 to 20 logical gates in a single integrated circuit chip.
Terminal Processor Unit (TPU)	The central main-frame unit in a B 771 System
Transistor-Transistor-Logic (TTL)	A family of transistor circuits used to implement digital logic networks, and characterized by its high speed, large capacitance drive capability and excellent noise immunity.
Virtual Machine	The image, characteristics, and functional results of one specific machine emulated by another.
"Z" Register	The "Z" register section contains a collection of registers and selection gates in the Memory Control Units (MU's) of the processor unit, which include a loadable Counter (CTR), and the Literal register (LIT).

PROCESSOR LOGIC SIGNAL PREFIXES

AC	Alternating current power Control
AD	Core memory control
CC	Console Control (B705/711 only)
CD	Clock Distribution control
CG	Clock Generation control
CO	Configuration card (B771)
CR	A9114 80-column Card Reader I/O control (B705/711)
CRT	A9115 80-column Card Reader I/O control (B771)
CU	Control (decision) Unit
DA	Core memory control
DC	Disk Cartridge I/O control
DD	Device Dependent port or I/O control common's
DP	Same as above
EO	External Operation control
EXT	External "Output Bus"
FE	Field Engineering control
IH	Core memory control and modules
LC	Single Line I/O control (B771)
LI	Load Interface control
LU	Logic Unit
MM	Minimonitor
MPM	Microprogram Memory (core memory output bus)
MU	Memory control Unit
NM	Nanomemory
OL	Overlay control and memory (B705/711)
PO	ODEC Printer I/O control
PP	Potter Printer
PS	Port Select unit
PT	Tire Printer I/O control
RC	96-character card I/O control
RE	Core memory control
SM	Shared Memory control
SP	Supervisory Printer I/O control (B771)
SY	System frame
Snum	Core memory modules
TC	Tape Cassette I/O control
TPP	Paper Tape Punch I/O control
TPR	Paper Tape Reader I/O control
WR	Core memory control and modules

PROCESSOR LOGIC SIGNAL GLOSSARY

ACDSV±24	Data Save control Voltages to memory (ground when active).
ACK1C2+24	AC relay K1 normally open switch contacts.
ACK2B2+24	AC relay K2 normally open switch contacts.
ACK2COIL	AC relay K2 pick coil (ground to pick coil).
ACPONCL/	System power-on clear level used to clear and preset processor and I/O control logic circuits when power is turned on (ground when active).
ACPOWDN	System Power Down from three different sources: a. Programmatic use of console or SPO control word b. Under or over DC voltage sensed c. AC sense failure (ground when active).
ADDSTRn (n=1-3)	Address Strobe Timing signal to three different core memory modules. (EOSMC+20 nanosec.)
CDSCLKn (n=A-L)	System Clock Pulses regenerated and distributed to processor and I/O control logics. (Note: C, D or I only in B705/711.)
CDSCLKPn (n=1-8)	Same as above. (Note: 6A, 7A and 8 in B771 only.)
CGCLEAR/, CGCLEARA, CGCLEARB, and CGCLEARC	System Clear signals generated from system clear pushbuttons, completion of F.E. test sequence, or system power on clear. CLEARB is used specifically for clearing I/O controls and nanobit 38 control, and an alternate means of being generated is when any of the following five hardware errors are first detected: a. MPM parity b. DPM parity c. NPM parity d. DPM address limit e. NPM illegal write in B705/711 only; load error in B771.
CGCSB	Memory Cycle Start Bit used to generate LI3SMC signal which goes to core memory for generating memory timing. During power up or error stops this signal is held off.
CGFECLK/	Field Engineering Clock Signal used to clock latches and flip-flops on FE3 card for MEM test, single pulse, and proceed controls. This pulse is delayed approximately 700 nanosec from system clock.
CGMDAF	Memory Data Available flip-flop. D input used to develop memory parity check timing.
CGPCLR/	Preclear signal generated from system clear push buttons or power-on clear. Used on the load interface and shared memory cards.
CGSCLKn (n=1-2)	Basic System Clock. 1 is used for phase I clocked logic. 2 is used for phase III clocked logic.
CG100	100 nanosec signal generated from 10 MHz counter every 200 nanosecs. Used for shared memory parity control.
CG100D	Same as above but delayed.
CG3CLKn (n=A-D)	Regenerated basic clock to phase III clock controlled by inhibit/gating.
CUADD01/ CUADD16/	Adder bits 1 and 16 are inverted in the CU for use in the LST and MST condition tests.
CUEL	Enable Left shift control to first section of Barrel Switch (LU) from Shift Controls (CU). This signal is true for both left shift and right end around (circular) shifts.
CUER	Enable Right shift control to first section of Barrel Switch (LU) from shift controls (CU). This signal should be true at all times except during a left shift.
CUEXTOP	Signal from Condition Register Logic (CU) which enables an external (Memory or Device) operation. Used by Port Select Unit.
CULSBCL	Signal used to force bit into LSB of BSW (LU4) under control of shift store logic (CU). This signal is tied to ground on all LU cards except the one containing the least significant bit.
CUMSBCL	Signal used to force bit into MSB of BSW (LU) under control of shift store logic (CU). This signal is tied to ground on all LU cards except the one containing the most significant bit.

CUREXT/	Reset "EXT" signal is low when a test on "EXT" is performed (CU). May be used to reset flip-flop generating "EXT" condition in some special I/O systems.
CUSARn (n=1-6)	Six control signals from the Shift Amount Register (CU) to the Barrel Switch (LU). Bits 1 and 2 control the first section of the Barrel Switch, and bits 3 and 6 control the second section.
CUSC	Successor Control signal from Condition Register (CU), indicating that selected condition test was met. Used by MPAD Controls (MU).
CUSC/	Successor Control signal from Condition Register (CU), indicating that the selected condition test was not met. Used by MPAD Controls (MU).
DATSAV±24	Data Save control signal from AC2 card renamed in core memory.
DDPnICnn (n=1-8) (nn=01-50)	I/O control 1 thru 8 device interface cable signal pins 01-50. Note: I/O's 1, 7 and 8 are dedicated for card reader, single line, and SPO controls on B771. I/O 8 is for console on B705/711.
$DDPn_1 2Bn_2$ (n_1=1-8) (n_2=A-B)	I/O control 1 thru 8 logic signals between data 9-16 and data 1-8 cards.
$DDPn_1 3Bn_2$ (n_1=1-8) (n_2=A-G)	I/O control 1 thru 8 logic signals between data 9-16, data 1-8, and control cards.
$DDPn_1 4Bn_2$ (n_1=1-8) (n_2=A-H)	I/O control 1 thru 8 logic signals between data 9-16, data 1-8, control and special cards.
DPnDINT/ (n=1-8)	Unique Data Interrupt signal from any of 8 I/O controls to the port select unit. Used to generate SRQ or IRQ.
DPnSINT/ (n=1-8)	Unique Status Interrupt signal from any of 8 I/O controls to the port select unit. Used to generate URQ or IRQ.
$DPn_1 A2Bn_2$ (n_1=6,7) (n_2=A-D)	Interconnect signals in modified extended I/O control areas for I/O's 6 or 7 used for single line controls. Interconnecting cards 5 to 6 and 7 to 8 (B771).
$DPN_1 A3Bn_2$ (n_1=6,7) (n_2=A-G)	Same as above for interconnecting cards 6, 7 and 8 (B771).
$DPn_1 A4Bn_2$ (n_1=6,7) (n_2=A-H)	Same as above for interconnecting cards 5, 6, 7, and 8 (B771).
EOASR/	Address and Status Request signal to the port selector from EO. This signal is decoded from bits 51 to 54 of the Control Register and cause the Port Selector to gate to the EXT Bus the address and status of the highest priority DDP generating an IRQ signal.
EOBnn (nn=51-53)	Signal from External Operation control register corresponding to nanobits 51 through 53. They control memory or I/O read and write functions for memory on the external operation card for I/O's on the port select unit cards.
EODATCY	Data Cycle when low places incrementer output on memory address lines. When high gates OS lines to memory address lines. Separates core memory into MPM and DPM (SM).
EOERRIND	Error Indicator signal when high lights error indicator on the console following the first detection of an error. The only means of extinguishing the light is by means of the system clear push button (B705/711 only).
EOERRST/	This signal when low permits the system to enter the fatal error loop by forcing the micro program address lines equal to zero and clearing any previous data cycle, also it generates CGCLEARB to clear I/O's and nanobit 38 in preparation for loop.
EOESTOP/	Error Stop signal used to stop basic system clock, after a 2nd hardware error is detected, after any field engineering test card error, or after loader error.
EOFORT2/	Force Type two – inhibits logic unit function.
EOINDn (n=1-3)	These three signals are sent to the console (B705/711) or SPO (B771) to light the "D" (B705/711) or status (B771) indicators to the configuration of the hardware errors.
EOINHSP/	Inhibit Step disables the increment register from loading a new micro program address.
EOMDSB	Memory Data Strobe gates memory data register to external bus when a BEX is generated following a data cycle.
EOOSEL	Output Select signal from control register (EO) to output select gates 1 through 8 (MU). When high, enables BR2 through output selection gates, when low, BR1. This signal will remain in the last state selected until changed by an EXTOP operation. Clear causes this signal to go to the low state and is set by nanobit 54..
EOSMC/	Refer to LI3SMC/.

EOWRITE/ Write signal from the memory control logic to the data (S) memory. When in the LOW state, specifies a memory WRITE operation. Also used for write to core on memory load from load interface control.

EXTnn/ (nn=01-16) External signal bus – made up from outputs of each I/O, memory data (not MPM), load interface, FE test cards, and port select unit (ext. 05-08). Sent to B register input or memory when in load interface mode. (Note: Configurator card also produces EXT's on B771.)

FECLEAR/ Clear signal generated from error reset push button on FE3 card or system clear push buttons provided that no error stop exists. This signal clears FEAC counter (01-16).

FEEQUAL/ This signal from the FE1 card when low implies that a comparison of memory output data to one of three memory input patterns is equal (excluding parity bit).

FEEQ1-8 This signal from the FE2 card when high implies that the most significant 8 bits of the above statement is true.

FEOLTST/ This signal from the FE4 card when low signifies the FE test is at SC=8 for the purpose of enabling the nanoparity check logic on LI3 card.

FESCLK/ An inverted system clock pulse from the FE3 card used to clock the sequence flip-flops on the FE4 card.

FETEST This signal is high if the FE4 card is installed and its MEM/MTR switch is MEM position. It is used to inhibit FE clear from FE error reset, inhibit error stop detection from all sources outside FE test boards, and enables test sequencing and memory error detection.

FE1UPCNT The FEAC (FE address counter) is located on two different cards (FE1 and FE2), 8 bits on each. This signal is the carry up-count from least significant to most significant 8 bit groups.

FE2AC03 and FE2AC04 Outputs of FEAC bit 3 and 4 used to determine when end of 4K or 8K memory stack address has been reached.

FE3DSELB and FE3DSELC The data patterns are selected by these two signals during test sequence counts. The three patterns are:

B	C		
0	0	=	FEAC pattern
0	1	=	All 1's pattern
1	0	=	All 0's pattern
1	1		

FE3DSEL0 and FE3DSEL1 The FE1 and 2 indicators are lit by control from these two signals generated from SEL0 and SEL1 toggle switches. The indicator information is:

SEL0	SEL1	
0	0	FEAC CNTR
0	1	Incrementer
1	0	MIR
1	1	MPM

FE3ERRPB This signal is low when the reset error push button is held depressed. It is used to clear the FE error flip-flop.

FE3LADDR This signal when high signifies that the last address for a 4K or 8K memory module has been reached during test sequence counts (1-6). At sequence count 8 it signifies that the nanomemory last address has been reached.

FE3MPAR A high signal signifying either a nanomemory or core memory parity error. Used to set the stop flip-flop if test switch is in stop on error position.

FE3PCLR/ When in normal/MTR mode, this signal as a low is a clear pulse for the error, stop, and sequence flip-flops which had been used in MEM test mode.

FE3PERR/ This is a core memory parity error regenerated and used to set the error flip-flop.

FE3PROC/ Proceed signal generated by PRO push button. When low it is used to reset the stop flip-flop and continue the test sequence.

FE3SS/ When in the memory test mode this signal being low enables steps in the incrementer logic.

FE3STNA When in the MTR mode this signal goes high as the force step push button is depressed permitting one step to take place in microprogram.

FESTNAR Same as above except this signal goes low.

FE4CLR	This signal when high generates a system clear at the completion of each test sequence.
FE4MPT1M	When high this signal signifies the test mode being in sequences 1 through 6 and not at last address. When combined with FE4SC1B it generates memory write logic.
FE4SC1B	The high output of sequence count 1 flip-flop. See above for use.
FE4SC1+2	Test sequence count equal to one or two. Used for pattern generation control.
FE4SC3BB	This signal when high signifies the sequence flip-flop 8 being set.
FE4SEL	This signal when high signifies the test sequence is either SC=3 or SC=4 and is used for data pattern generation control.
FE4STAC	This signal when high permits FEAC to count +1. FEAC has three means of being counted: a. In MTR mode while not waiting counting clock pulses. b. In test mode SC=1-6 counting addresses. c. In test mode SC=8 counting nano parity bit 56.
FE4STOPF	This signal when high has stopped the sequence count, one address beyond error or at the end of sequence 8 if IRQ switch is on. It also enables the use of the proceed push button.
FE4STPF/	This is the reset output of the above named flip-flop.
IHBTn (n=1-3)	Core memory inhibit timing signal generated during write half of memory cycle for each of 3 modules.
$IHBn_1n_1n_2$ (n_1n_1=017-17) (n_2=1-3)	17 different inhibit driver signals through each of three modules in core memory.
LCCTSID2	Signal available for I/O's single line control #2 (B771 not used at this time).
LCCTSIND	Clear to send indicator for I/O's single line control 1 (B771, not used at this time).
LCDSTID2	Signal available for I/O's single line control 2 (B771 not used at this time).
LCRDTIND	Receive data indicator for I/O's single line control 1. Used to light receiving indicator on supervisory printer (B771).
LCRVID2	Signal available for I/O's single line control 2 (B771, not used at this time).
LCSDRIND	Send data ready indicator for I/O's single line control 1 (B771 not used at this time).
LCXDTIND	Transmit data indicator for I/O's single control 1 used to light transmitting indicator on supervisory printer (B771).
LCXTMID2	Transmit data indicator for I/O's single line control 2 (B771, not used at this time).
LDSE	Same as LIDSE in B705/711 (B771).
LIALDAT	Allow Data to permit loader punch card information from columns 17-80 to be gated onto the EXT bus for data to memory (B771).
LIALLRC	Allow Longitudinal Redundancy Check on loader punched cards for columns 9 through 80 (B771).
LICCE66/	Code Comparator Equals 66 start code (B705/711only).
LICLR/	Used to clear LIALLRC and LIADAT flip-flops from column 80 of loader card or system clear (B771).
LIDSE/	A low signal when the load/normal switch on the processor is placed in the load position. It is used to set the load flip-flop when the system clear push button is depressed or power-on sequence has been initiated and completed.
LIENSHF	This signal when high permits the upper and lower digits of a tape frame to be shifted into the EXT register.
LIERR/	This signal when low signifies that either a longitudinal parity error or a memory parity error has occurred while loading paper tape or cards.
LIEVEN/	Low signifies even columns of loader cards for columns 17 through 80 (B771).
LIFORT2	Force Type II, to enable incrementing the memory address with each load information word from paper tape or punched cards.
LILCCSN (n=1-2)	Longitudinal Check Character Strobe. These signals clock a check register for every frame of tape data after the start code has been detected and up to the LRC frame after a stop code has been detected (B705/711 only).

LILOAD	The set output of the load flip-flop, which is true when system is in the load mode. When this signal is low, it clears the loader EXT register when the system is in the normal mode (indirect thru LIALLDAT on B771).
LILRCER/	Longitudinal Redundancy Check Error. Low when any 9th frame of data, after start code has been detected, places the LCC register not equal to zero, or if exclusive or of columns 9 through 80 on loader cards is not equal to zero (B771).
LILRCNZ/	Longitudinal Check Register Not equal to Zero (used in the above example).
LIMDOS/	Memory Data Output Strobe. Only used if system monitor or overlay features are used. Signal is low if features are not installed.
LIMEMCY/	Memory Cycle used to generate the start memory cycle to core memory during load for each word of loader tape or card data.
LIMEW/	This signal when low gates out load ext data to memory and enables a write memory cycle.
LIMRC/	This signal during load mode inhibits memory parity error detection except for two memory cycles after load data write (LIMEW/).
LINGRPn (n=0-3)	These signals control the addressing of 4 nanomemory groups of words from MPM bits 6 and 8 (B705/711 only).
LINHSTP/	Inhibit Step. This signal is sent to memory address control to inhibit incrementing at all times during load mode except immediately following the load data memory cycle.
LINPE/	Nanoparity Error. This signifies a parity error if the total number of bits in a 56 bit word are even at the time when either type I microinstructions or FE nanotests are being performed.
LIOCT02	Octal 2 bit value from loader card rows 2, 3, 6 or 7. (B771).
LIOCT04	Octal 4 bit value from loader card rows 4, 5, 6 or 7. (B771).
LIODD/	Low signifies Odd columns of loader cards for columns 17 through 80. Note: Columns less than 17 are considered to be odd (B771).
LIPCLRA/	Preclear A (regenerated from CGPCLR/) used to clear load interface and memory parity before clearing other logic.
LIPECLR/	Parity Error Clear used specifically for clearing the memory parity error flip-flop from either system clear, power-on clear, or initiate load.
LISB/	Loader state B distinguishes between keyboard memory loader tape upper or lower characters (B705/711 only).
LISPE/	Shared Parity Error. This signal is the regeneration of memory parity error during load mode and is used to light indicator on console or SPO.
LISTP/	Stop Code. A latched level signifying that a stop code (4000) has been detected and is used to reset the start/stop flip-flop (B705/711 only).
LI3DTM17	Data To Memory bit 17. This signal is sent to memory from the output of the odd parity generator to be written in the parity plane of core memory.
LISOCT01	Special Octal 1 bit value from rows 1, 3, 5, 7 or 9 of loader cards (B771).
LISOCT08	Special Octal 8 bit value from row 8 of loader card (B771).
LISTOER/	Stop Or Error. When low from system clear, LRC error, stop push button on card reader, or any punch in rows 1, 3, 5, 7 or 9 of the column that indicates a stop card (B771).
LI3SMC/	Start Memory Cycle. In all cases this signal starts memory timing at core memory control.
LUABT	Adder Bits True signal from adder outputs (LU) to condition register (CU) for testing. This is an open-collector "AND" signals with pullup on the CU card.
LUADnn (nn=01-16)	Adder output signals from the ALU (LU) to the barrel switch (LU). Also used as an input to the B register via the B-input select gates (LU). Number of signals is equal to word length of machine. The most and least significant bits are also used for condition testing (CU) and as inputs to the shift store flip-flop (CU).
LUADINnn (nn=01-16)	Adder input signals from Y-select gates (LU) to adder (LU). Number of signals is equal to word length of machine. ADIN01 is most significant bit.
LUBSWnn (nn=-1-16)	Barrel switch outputs (LU) used as the major data output of the logic unit for all but I/O purposes. The number of signals is equal to the machine word length. These signals provide data inputs to the A register (LU), the B-input select gates (LU), the MIR (LU), the SAR (6 or less least significant bits only) (CU), the MAR, the CTR (8 LSB only) (MU), the Base Registers, BR1 and BR2 (next least significant 8 bits only) (MU), and the AMPCR (14 least significant bits only) (MU).

LUBS2nn (nn=01-16) — Barrel switch 1st stage outputs to second stage inputs.

LUCARnn/ (nn=01, 05, 09, 13) — Carry signal generated by group carry circuit (LU) indicating a carry out of bit "nn" of the adder. Used as an input to bit "nn-1" of the adder (LU). The most significant bit carry (LUCAR01/ is used to test for adder overflow (CU).

LUCAR9G1 — Carry bit from adder 9 position gated by carry inhibit control. Inhibit command prevents carry from least significant byte to most significant byte of the adder.

LUCOMP and LUCOMP/ — Complement. These signals are used for complement control of the B register on BC8 and BC4 functions.

LUCOMPnn (nn=01, 05, 09, 13) — These signals set the B register bits in the absence of a carry on BC8 and BC4 functions as follows:

Comp	01		05		09		13	
BC8	3	4			11	12		
BC4	3	4	7	8	11	12	15	16

B REG

LUENBCLK — Enable B register Clock. Low only if nanobits 37-49 are equal to zero.

LUMIRnn/ (nn=01-16) — Output data from processors memory information register (LU) to I/O controls, data memory, and FE indicators.

LUNB37/, LUNB39, and LUNB40 — These signals are the regeneration of nanobits needed for the B register input selection control (LU).

MMDOS, MMFDC/, and MMIMAD/ — These signals used by factory only. With feature removed pull up resistors keep signals high.

MPMDATAV — Signal from core memory to processor signifying Memory Data is Available following read portion of a memory cycle. (B705/711 only, not used at this time).

MPMnn (nn=01-17) — 17 individual data bit outputs of core memory at completion of any memory cycle. If the memory cycle is specifically for program memory, then the MPM's are decoded to type I or type II instructions.

MUACTLn (n=1-2) — Two control signals from control register (MU) to X-select gates (LU).

ACTL1	ACTL2	
0	0	Select A3 Register
0	0	Select A2 Register
1	0	Select A1 Register
1	1	Select "Z" Inputs (LIT, CTR, or EXT if any)

MUAM-MCA — Transfer MPCR to AMPCR signal from MPAD controls to AMPCR input select gates and strobe enables.

MUAM-MP — Transfer MPM 14 least significant bits to AMPCR signal from MPAD controls to AMPCR input select gates and strobe enables.

MUAMODEA — Adder Mode signal generated by the control register (MU) to control the MSI adder chips (LU). When true specifies arithmetic operation, when false specifies logical operation. (See MUASn1n2.)

MUAMnn (nn=X, 00-12) — AMPCR outputs (14 bits) from MU. Used as inputs to the least signficant 14 bits of the Y-select gates (LU). All corresponding LU inputs above the least significant 14 bits are tied to ground.

MUAPLSn (n=1-2) — AMPCR Plus 1 or Plus 2 to be placed into increment register (EXEC, JUMP, CALL or RETN).

MUASn1n2 (n_1=0-3) (n_2=A-B) — Adder Select controls:

Nanobit 28-31	MUASn 3210	Mode	Select Operation	
0	1001	A	X+Y	X plus Y
1	0001	L	NOR	$\overline{X}$ and $\overline{Y}$
2	0010	L	NRI	$\overline{X}$ and Y
3	1001	A	X+Y+1	X plus Y plus 1
4	0100	L	NAN	$\overline{X}$ or $\overline{Y}$
5	1101	A	OAD	X plus (X or Y)
6	0110	L	XOR	(X and $\overline{Y}$) or ($\overline{X}$ and Y)
7	0111	L	NIM	X and $\overline{Y}$
8	1000	L	IMP	$\overline{X}$ or Y
9	1001	L	EQV	(X and Y) or ($\overline{X}$ and $\overline{Y}$)
10	1000	A	ADD	X plus (X and Y)
11	1011	L	AND	X and Y
12	0110	A	X-Y-1	X plus $\overline{Y}$
13	1101	L	RIM	X or $\overline{Y}$
14	1110	L	OR	X or Y
15	0110	A	X-Y	X plus $\overline{Y}$ plus 1

MUAn$_1$Cn$_2$ (n_1=1-2) (n_2=1, 5, 9) — Carry bits between the full adder chips that generate AMPCR +1 or +2 to the incrementer.

MUBORC — Signal generated from type II Branch Or Call. Used to enable MPM input plus 1 to the incrementer.

MUCIN/ — Carry Input to LSB of adder (LU) and corresponding group carry circuit (LU). Generated by control register (MU) for arithmetic operations "X+Y+1" or "X-Y."

MUCOV — Counter overflow signal indicates that the counter (MU) had reached a count of 255 (all one's). After the next count the COV flip-flop in the condition register (CU) will be set.

MUCTRn (n=1-8) — Eight bit output from the Counter register (MU) used as input to the most significant bits of the X-select gates (LU) and the Y-select gates (LU). These signals form a portion of the "Z" register inputs.

MUDN41 — Signal from control register (MU) corresponding to nanobit 41. Enables strobe pulse to MIR register (LU).

MUDN42 — Signal from control register (MU) corresponding to nanobit 42. Enables strobe pulse to AMPCR (MU).

MUDN43 — Signal from control register (MU) corresponding to nanobit 43. Enables strobe pulse to base register BR1 (MU).

MUDN44 — Signal from control register (MU) corresponding to nanobit 44. Enables strobe pulse to base register BR2 (MU).

MUDN48/ — Signal from control register (MU) corresponding to the complement of nanobit 48. Enables transfer of data to CTR (MU) and reset of COV flip-flop (CU). Transfer of data to CTR will override increment counter command (bit 47) should they occur simultaneously.

MUENBn/ (n=1-3) — Three signals from the control register (MU) to the Y-select gates (LU) used to inhibit unwanted bits during LIT, CTR, or EXT transfers through Y-select gates. If all three signals are true, they produce a "ZERO" output from the Y-select gates (ENB1-MSB/ENB2-CENTER/ ENB3-LSB).

MUINCREN — Increment register input enable from MPAD controls (MU).

MUINCnn (nn=X, 00-12) — Incrementer outputs (address) to microprogram memory.

MUINH8/ — Inhibit 8 bit carry signal generated by control register (MU) from nanobit 27. When false, inhibits carry out of 8 bit groups of the adder (LU).

MULIT-MP — Transfer MPM data to LIT signal from MPAD controls (MU) to LIT register (MU). Enables strobe pulse to LIT register.

MULITn (n=1-8) — Eight bit output from the literal register (MU), used as input to the least significant bits of the X-select gates (LU) and the Y-select gates (LU). These signals form a portion of the Z register inputs. These signals are also used as inputs to the CTR and MAR (MU).

MUMPCREN — MPCR input enable from MPAD controls (MU) to MPCR register. Enables strobe to MPCR causing MPCR to store incrementer inputs.

MUMPLSn (n=1-8) — MPCR plus 1 or plus 2 to be placed into increment register and includes also MPM plus 1 (STEP, SAVE, or SKIP instruction).

MUn_1Cn_2 (n_1=1,2) (n_2=1,5,9) — Carry bits between full adder chips that generate MPCR+1 or +2 and MPM+1 to the incrementer register.

MUNB20 — Signal from control register (MU) corresponding to nanobit 20. Controls the most significant bit of the Y-select gates (LU). On all LU cards except the one containing the most significant bit, this signal is tied to ground.

MUN21/ — Signal from control register (MU) corresponding to complement of nanobit 21. Controls the most significant bit of the Y-select gates (LU). On all LU cards except the one containing the most significant bit, this signal is tied to the appropriate MUENBn/ signal.

MUNB25 — Signal from control register (MU) corresponding to nanobit 25. Controls the least significant bit of the Y-select gates (LU). On all LU cards except the one containing the least significant bit, this signal is tied to ground.

MUNB26/ — Signal from control register (MU) corresponding to complement of nanobit 26. Controls the least significant bit of the Y-select gates (LU). On all LU cards except the one containing the least significant bit, this signal is tied to the appropriate MUENBn/ signal.

MUNB34 — Signal from control register (MU) corresponding to nanobit 34. Enables strobe pulse to A1 register (LU).

MUNB35 — Signal from control register (MU) corresponding to nanobit 35. Enables strobe pulse to A2 register (LU).

MUNB36 — Signal from control register (MU) corresponding to nanobit 36. Enables strobe pulse to A3 register (LU).

MUNB37 — Signal from control register (MU) corresponding to nanobit 37. Controls B-input select gates (LU).

MUNB38 — Signal from control register (MU) corresponding to nanobit 38. Controls B-input select gates (LU). Also used by memory control logic to determine when a "BEX" operation is performed.

MUNB39 — Signal from control register (MU) corresponding to nanobit 39. Controls B-input select gates (LU).

MUNB40/ — Signal from control register (MU) corresponding to complement of nanobit 40. Controls B-input select gates (LU). Also used by memory control logic to determine when a "BEX" operation is performed.

MUNQEn (n=1-3) — Three enable signals to X-select gates (LU) from control register (MU). Used to inhibit unwanted bits during LIT, CTR or EXT transfers through X-select gates. If all three signals are false, produces "ZERO" output from X-select gates (NQE1-MSB/NQE2-CENTER/NQE3-LSB).

MUOSnn (nn=01-16) — Output Select bits from MAR (bits 9-16) and BR1 and BR2 (bits 1-8) generated on MU and used as inputs to the 16 bits of the Y-select gates (LU). OS signals provide address information to Data (S) Memory, either directly or via buffers. Bits 5 through 8 (and their complements) are used by PS1 to designate a selected DDP, and additional OS bits may be used by certain DDP's for further addressing controls.

MUSAR-MP — Transfer MPM bits 5 through 8 to shift amount register. This signal is true when MPM word contains a "1100" or "1101" in MPM bits 1 through 4 (type II instruction).

MUSELBA1 and MUSELBB1 — These two signals are developed by nanobits 22 through 24 for adder Y-input selection control. Selection is as follows:

22	23	24	SELBB1	SELBA1	Y-input
–	0	0	0	0	B Reg MCL
–	0	1			MS8 LS8 Both
0	1	0	0	1	CTR, LIT or Z
1	1	0	1	0	AMPCR to LS14
1	1	1	1	1	MS8 LS8 BR1 or BR2, MAR

– equals don't care

MUTYPE2	Signal generated by MPAD controls (MU) to indicate that a Type II instruction is to be executed. Used by the condition register (CU), and the memory and device controls (EXTOP controls).
MU3CLKI/	Phase 3 clock inhibit from MPAD controls (MU) to clock control and buffering (CG). When low, signal inhibits generaton of phase 3 clock pulses.
NMBnn (nn=01-16)	The first 16 output bits of nanomemory words prior to being inverted for determination of conditional status, program instruction destination, and condition adjust. Inversion required due to heavy loading of these bits.
NMNnn (nn=01-56)	These signals are the inversion of the first 16 nanobits and the direct outputs of bit 17 through 56. At this point all nanobits have a high value for a true representation.
NMPARn (n=1-2)	These two signals indicate the odd or even bit count of each nano word. Each signal handles half of the bits, and if they are opposite, odd nanoparity is indicated, which is correct.
OLAY/	Used only by overlay feature. When feature is not installed, a pullup resistor keeps signal high (B705/711).
OLCLR	Active only when overlay feature is installed (B705/511).
OLDEC/	Same as above (B705/711).
OLERR/	Used only by overlay feature signal floats high when feature is not installed (B705/711).
OLMDSOS	Used only by overlay feature. When feature is not installed, a pullup resistor keeps signal high (B705/711).
OLNLD	Active only when overlay feature is installed (B705/711).
OLNS3/	Same as above (B705/711).
OLNWTn (n=1-4)	Active only when overlay feature and read/write nanomemory is installed (B705/711).
OLPRES/	Active only when overlay feature is installed (B705/711).
OLRDCY/	Used only by overlay feature. When feature is not installed a pullup resistor keeps signal high.
PSENAB2/	Port select enable signal used to disable lowest priority port and its I/O control interrupts of unaddressed ports (1 through 4).
PSENSTn/ (n=1-8)	Unique enable status signal to the highest priority interrupting non-addressed I/O controls to permit status information to be placed on EXT's 1 through 3 and 9 through 16. EXT's 4 through 8 are used by the Port Selector to signify the address of the I/O control whose status was enabled.
PSINSTn (n=1-2)	Both of these signals are used to signify to the 8 different I/O controls that the data on MIR lines is a control instruction or status information returned on the EXT lines. OS Bit 1 from either BR1 or BR2 generates these signals.
PSIRQ/	Input Request signal from the Port Select Unit (PS1) to the condition register (CU). This is an open collector signal with pullup on the CU. Signal in the low state indicates that a DDP which is UNSELECTED is generating a status or data interrupt. (Can also be generated by FE toggle switch.)
PSREADn/ (n=1-8)	Unique "Read from I/O Control" signal to any of 8 I/O controls. When active (low) the I/O control places either data or status information on the EXT lines.
PSSRQ/	Solicited Request signal from the port select unit (PS1) to the condition register (CU). Signal in the low state indicates that the selected DDP is generating a Data Interrupt. Open collector signal with pullup on the CU board.
PSURQ/	Unsolicited Request signal from the port select unit (PS1) to the condition register (CU). Signal in the low state indicates that the selected DDP is generating a status interrupt. Open collector signal with pullup on the CU board.
PSWRITn/ (n=1-8)	Unique "Write to I/O control" signal to any of 8 I/O controls. When active (low), the I/O control receives either control instruction or data on the MIR lines.
READSTRn (n=1-3)	Core memory read strobe timing signal. Enables the output of the sense amplifiers in one of three modules.
RESETn (n=1-3)	Core memory reset timing signal used to reset data registers in one of three modules.
SMADRnn/ (nn=01-16)	Address lines from processor to core memory.
SMAEF/	Address error flag indicates maximum memory address has been exceeded as indicated by hard-wired address limit.

SMDATCY	Shared Memory Data Cycle. When high, a memory data cycle is indicated, the address is selected from the BRn and MAR, and the memory output is clocked to the EXT's. When low, a memory program cycle is indicated, and the address is selected from the INCR.
SMDOS	Used by overlay feature only. Occurs approximately 200 nanoseconds prior to CGSCLKn (B705/711).
SMDTMnn (nn=01-16)	Shared Memory Data To Memory. Data from MIR or loader interface to memory.
SMDTM17	Parity bit for odd parity in core memory.
SMEWN	Used only for overlay feature. Occurs approximately 100 nanoseconds prior to CGSCLKn (705/711).
SMEXT/	External interrupt. Occurs every 125 milliseconds from real time clock or F.E. toggle switch.
SMMPMn (n=1-4)	MPM bit 1 through 4 gated out to MU for determination of instruction type on a microprogram memory cycle.
SMPCHKn (n=1-2)	These two signals check for odd parity read from memory.
SMNGPn (n=0-2)	These signals control the addressing of 3 nanomemory groups of words from MPM bits 6 and 8 (B771).
SMPERR	Memory Parity Error. High if the 17 MPM bits have even bit count.
SMPGENn (n=1-2)	These signals generate odd or even bit count levels for generation of bit 17 (parity bit) to memory.
SMPG12	The results of the above statement (low) for bit 17.
SYCLRPB and SYCLRPB/	System Clear Push Button signals.
$Sn_1n_1n_2$ and Sn_1n_1/n_2 (n_1n_1=01-17) (n_2=1-3)	Sense line outputs from core memory's 17 different planes within any of three modules.
WRITESTRn (n=1-3)	Core memory Write Strobe. Enables new data into the data register to be written in write half of memory cycle in any of three modules.
XCREADTn (n=1-3)	Core memory "X" common switch read timing input signal gated to three modules.
XCWRITETn (n=1-3)	Core memory "X" common switch write timing input signal gated to three modules.
XCn_1n_2 (n_1=0-7) (n_2=1-3)	Core memory's eight different "X" common switch outputs in three separate modules.
XDREADTn (n=1-3)	Core memory "X" driver switch read timing input signal gated to three separate modules.
XDYDWRTTn (n=1-3)	Core memory's "X" and "Y" driver switch write timing input signals gated to three separate modules.
$XNDn_1n_2$ (n_1=0-7) (n_2=1-3)	Core memory's eight different negative driver switch outputs in three separate modules.
$XPDn_1n_2$ (n_1=0-7) (n_2=1-3)	Core memory's eight different positive driver switch outputs in three separate modules.
YCREADT4Kn (n=1-3)	Core memory "Y" common switch read timing input signals for lower 4,096 words in three separate modules.
YCREADT8Kn (n=1-3)	Core memory "Y" common switch read timing input signals for upper 4,096 words in three separate modules.
YCWRITET4Kn (n=1-3)	Core memory "Y" common switch write timing input signals for lower 4,096 words in three separate modules.
YCWRITET8Kn (n=1-3)	Core memory "Y" common switch write timing input signals for upper 4,096 words in three separate modules.
$YCn_1n_1n_2$ (n_1n_1=00-15) (n_2=1-3)	Core memory's 16 different "Y" common switch outputs in three separate modules.
YDREADTn (n=1-3)	Core memory "Y" driver switch read timing input signal in three separate modules.
$YNDn_1n_2$ (n_1=0-7) (n_2=1-3)	Core Memory's eight different negative driver switch outputs in three separate modules.
$YPDn_1n_2$ (n_1=0-7) (n_2=1-3)	Core memory's eight different positive driver switch outputs in three separate modules.

B700

PROCESSOR

(INCLUDES B705, B711, B771, and B772)

SECTION

II

FUNCTIONAL
DETAIL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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PROCESSOR SECTION

INTRODUCTION

This section presents the functional detail of the Central/Terminal Processing Unit (CPU/TPU). The section is divided into the following four subsections to aid in locating specific functional detail descriptions:

a. Processor section.
b. Main (core) memory section.
c. I/O device control section.
d. Power supply section.

GENERAL

The Processor is the major building block of a B700 Computer system which contains the "minimally-committed" logic or hardware that is controlled by the program residing in the firmware store. (See Figure II-1.) The firmware store is comprised of a Microprogram Memory (MPM) and Nanomemory (NM). The Microprogram Memory provides the logical sequence of operations in the order that the Processor must perform them as defined by the microinstructions. The Nanomemory (NM) provides the logical control levels to the Processor and the port selector.

The Processor minimally-committed logic or hardware is contained in the following units: Logic Unit (LU1 through LU5 cards), Control Unit (CU1 and CU2 cards), Memory Control Unit (MU1 through MU5 cards), the External Operation Control (EO card), the Shared Memory Control (SM1 through SM3 cards), and the clock circuits (CG and CD cards). (Refer to core memory subsection for Shared Memory Control, SM1 through SM3.)

The logic or hardware of the processor essentially performs those operations which the microprogram directs it to perform. Information concerning the functional operation of the processor is presented under the following headings:

a. Firmware Store (MPM and NM).
b. Logic Unit (LU1 through LU5).
c. Control Unit (CU1 and CU2).
d. Memory Control Unit (MU1 through MU5).
e. External Operation Control (EO).
f. Clock Generation and Distribution (CG and CD).

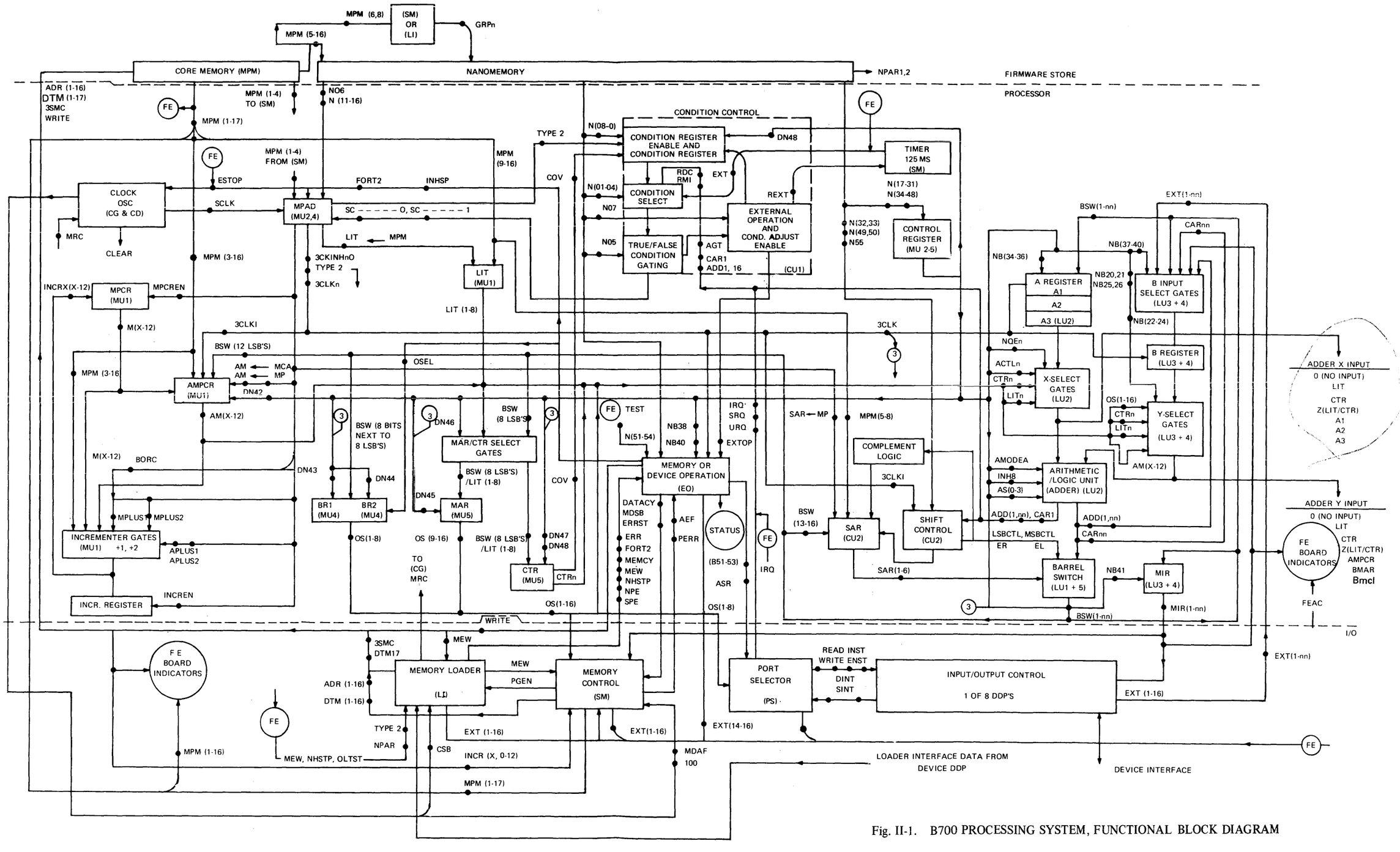


Fig. II-1. B700 PROCESSING SYSTEM, FUNCTIONAL BLOCK DIAGRAM

FIRMWARE STORE (MPM AND NM)

The firmware store consists of the Microprogram Memory (MPM) and Nanomemory (NM). The Microprogram Memory (MPM), which is one of the major functional units of the processor, contains the microinstructions that provide the logical sequence of operations that are to be performed by the processor. The microinstruction consists of two levels: the microcode and the nanocode. The microcode consists of 16 bits, which may contain a nanomemory address for selecting a nanocode or preset values that are to be loaded into the Literal register (LIT), Shift Amount Register (SAR), Alternate Microprogram Count Register (AMPCR), or the Incrementer (INCR) and Microprogram Count (MPCR) Registers. The Nanomemory (NM) provides the logic control levels to the processor and the port selector. The nanocode, which is contained in the nanomemory, consists of 56 bits that are used to enable 56 nanobit control levels in parallel. See Figure II-2 for the input and output control signals of the microprogram memory and Nanomemory.

The Incrementer register output signals (INCRX through INCR12), which are generated in the Memory Control Unit (MU1-1 through MU1-4), provide addressing capability of the Microprogram Memory (MPM) through Shared memory controls ADR1-16. The Write Signal from the EO card and the Memory Data inputs (DTM01 through DTM17) along with Start Memory Cycle are inputs because a Read/Write Memory (RWM) configuration is used for the microprogram memory.

The Microprogram Memory output bits (MPM1 through MPM17) are sent to the various control circuits in the processor as follows: MPM bits 1 through 4 are used by the Microprogram Address Controls (MPAD CNTL) on the MU2 card; bits 3 through 16 are inputs to the Alternate Microprogram Count Register (AMPCR) on MU1-1 through MU1-4 cards; bits 9 through 16 are inputs to the Literal register (LIT) on the MU1-2 and MU1-3 cards; bits 5 through 8 are inputs to the Shift Amount Register (SAR) input select gates on the CU2 card; and MPM bit 17 is used for parity checking. See the microcode format shown in Figure II-3 for further details about the MPM bits. MPM bits 6 through 16 (least significant 11 bits) are used by the nanomemory as group and address information. Nanomemory consists of two groups of 256 addressable 56-bit nanowords.

Nanomemory is a read-only memory constructed from LSI chips assembled on four individual printed circuit cards. Each card contains seven memory chips, capable of producing 256 different output combinations. Thus one card can produce 256 half-NANO words (28 bits). Table II-1 lists all available nanowords. The nanobit output signals (N01 through N55) are used as enable control levels in the processor. See the nanoword contents and nanocode format information provided in Figure II-3.

The firmware store (MPM and nanomemory) is characterized by the unique ability of maintaining changeable nanocodes and microinstruction phasing. The microcode controls and nonocode controls which are generated by microprogramming, are reflected in the contents of either the microprogram memory or nanomemory.

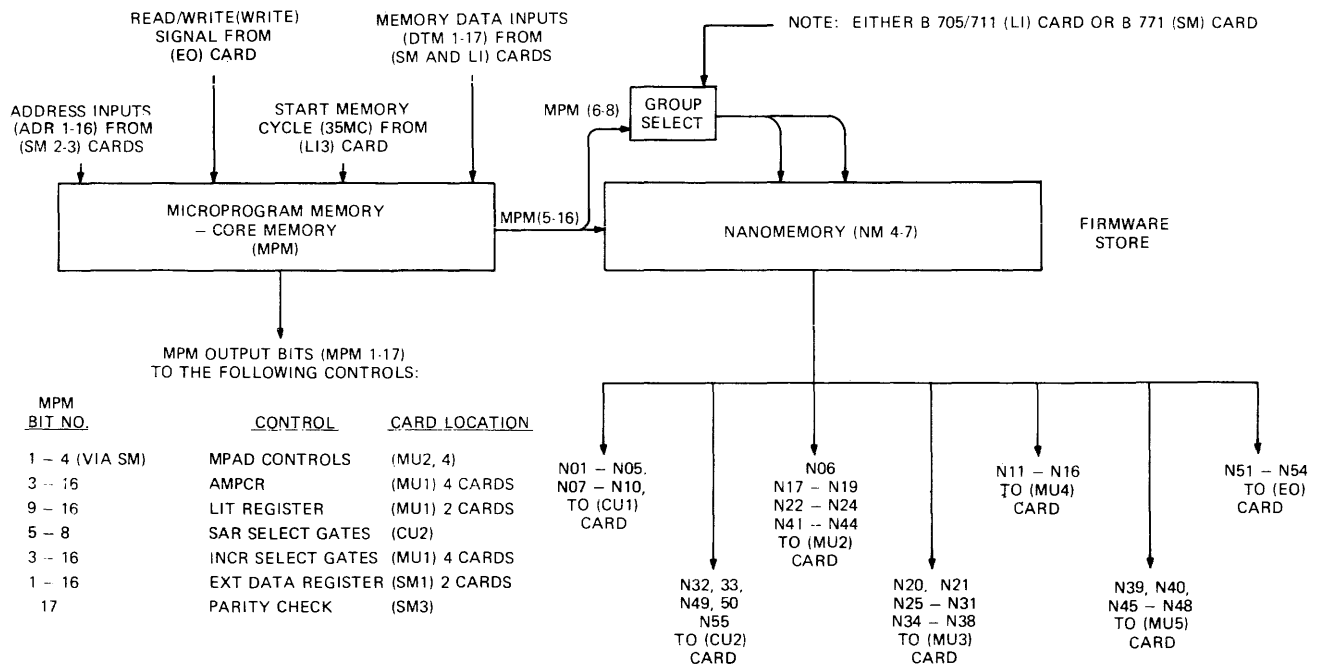


Fig. II-2. MICROPROGRAM MEMORY (MPM) AND NANOMEMORY (NPM), BLOCK DIAGRAM

NANOWORD CONTENTS

1-4	Condition Selection
5	Successor Condition
6	Phase 3 Modifier
7	Memory/Device/Condition Adjust Modifier
8-10	Condition Adjust
11-13	Microprogram Address Controls; SC = 1
14-16	Microprogram Address Controls; SC = 0
17-19	X – Selection to Adder
20-26	Y – Selection to Adder
27	Inhibit Carry Between Bytes
28-31	Adder Operation
32-33	Shift Selection
34-36	A Register Input Selection
37-40	B Register Input Selection
41	MIR Input Selection
42	AMPCR Input Selection
43	BR1 Input Selection
44	BR2 Input Selection
45-46	MAR Input Selection
46-48	Counter Input Selection
49-50	SAR Input Selection
51-54	Memory/Device Operation
55	Sign Store Control

1-16,51-54	Phase 1 Operations
17-33	Phase 3 Controls
34-50,55	Destination Controls (Executed at Termination of Phase 3)

MPM MICROCODE

	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	Type
	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	
D→	1 1 0 1	SAR	∅ ∅ ∅ ∅ ∅ ∅ ∅ ∅		II
C.	1 1 0 0	SAR	LIT (literal Reg.)		II
	0 0	AMPCR			II
	1 1 1 0	∅ ∅ ∅ ∅	LIT		II
	1 1 1 1	*	N ADDRESS		I
	0 1	MPCR * INCR			II
	1 0	AMPCR Replaced by MPCR [illegible]			II

* If = 0, indicates nanoword was loaded following this MPM word (used by loader only).

∅ Not used.

Type II instr. have at least one '0' bit

Type I always 'F'

SAR - Shift Amount Register

M42 start

NOTES

CONDITION SELECTION MNEMONICS

ABT = ADDER BITS TRUE
AOV = ADDER OVERFLOW
COV = COUNTER OVERFLOW
EXT = EXTERNAL INTERRUPT REQUEST (125 MS TIMER)
GC1 = GLOBAL CONDITION 1
GC2 = GLOBAL CONDITION 2

LC3 = LOCAL CONDITION 3

IRQ = INPUT REQUEST
LC1 = LOCAL CONDITION 1
LC2 = LOCAL CONDITION 2
LST = ADDER LEAST SIGNIFICANT BIT
MST = ADDER MOST SIGNIFICANT BIT
RDC = READ COMPLETE
RMI = READY MIR
SRQ = SOLICITED REQUEST
URQ = UNSOLICITED REQUEST

NANOCODE

1 2 3 4	CONDSEL
0 0 0 0	GC1
0 0 0 1	GC2
0 0 1 0	LC1
0 0 1 1	LC2
0 1 0 0	MST
0 1 0 1	LST
0 1 1 0	ABT
0 1 1 1	AOV
1 0 0 0	COV
1 0 0 1	RMI
1 0 1 0	RDC
1 0 1 1	IRQ
1 1 0 0	EXT
1 1 0 1	LC3
1 1 1 0	SRQ
1 1 1 1	URQ

5 **FT** (Successor Condition) Next will execute next instr.

0	SC = 1 if CONDSEL is FALSE
1	SC = 1 if CONDSEL is TRUE

6 **LUC** (Phase 3 Modifier)

0	Do Phase 3 operations unconditionally
1	Do Phase 3 operations if SC = 1

7 **MDC** (MDOP & CNDADJ Modifier)

0	Do MDOP and CNDADJ unconditionally
1	Do MDOP and CNDADJ if SC = 1

8 9 10	CNDADJ	(Do if MDC = 1)
0 0 0	-------	
0 0 1	Set LC2	
0 1 0	Set GC2	
0 1 1	Reset GC2	
1 0 0	Set LC3	
1 0 1	Reset GC1	
1 1 0	Set GC1	
1 1 1	Set LC1	

Fig. II-3 MICROCODE FORMAT, NANOWORD CONTENTS, AND NANOCODE FORMAT (SHEET 1 OF 2)

MPAD CONTROLS

Used if SC=1

11	12	13	
0	0	0	WAIT
0	0	1	STEP
0	1	0	SAVE
0	1	1	SKIP
1	0	1	JUMP
1	0	0	EXEC
1	1	0	CALL
1	1	1	RETN

Used if SC=0

14	15	16
0	0	0
0	0	1
0	1	0
0	1	1
1	0	1
1	0	0
1	1	0
1	1	1

X Selection to Adder

17	18	19	
0	0	0	Zero
0	0	1	LIT (To LS Byte)
0	1	1	CTR (To MS Byte)
1	0	0	Z (CTR /LIT)
1	0	1	A1
1	1	0	A2
1	1	1	A3

Y Selection to Adder

20	21	22	23	24	25	26	
0	0						Zero in MS Bit
0	1						B in MS Bit
1	0						$\overline{B}$ in MS Bit
1	1						1 in MS Bit
		0	0	0			ZERO
0	0	0	0	1	0	1	LIT (To LS Byte)
0	1	0	1	1	0	0	CTR (To MS Byte)
		1	0	0			B
0	1	1	0	1	0	1	Z (CTR/ LIT)
0	0	1	1	0	0	1	AMPCR
0	1	1	1	1	0	1	BMAR (OS)
					0	0	ZERO in LS Bit
					0	1	B in LS Bit
					1	0	$\overline{B}$ in LS Bit
					1	1	1 in LS Bit

27

0	Allow
1	Inhibit

28	29	30	31	ADOP	MNEMONIC
0	0	0	0	X + Y	ADD
0	0	0	1	$\overline{X} \vee \overline{Y}$	NOR
0	0	1	0	$\overline{X} \cdot Y$	NRI
0	0	1	1	X + Y + 1	ADD + 1
0	1	0	0	$\overline{X \cdot Y}$	NAND
0	1	0	1	(X v Y) + X	OAD
0	1	1	0	X ⊗ Y	XOR
0	1	1	1	$X \cdot \overline{Y}$	NIM
1	0	0	0	$\overline{X} \vee Y$	IMP
1	0	0	1	$\overline{X \otimes Y}$	EQV
1	0	1	0	X + (X · Y)	AAD
1	0	1	1	X · Y	AND
1	1	0	0	X − Y − 1	SUB-1
1	1	0	1	$X \vee \overline{Y}$	RIM
1	1	1	0	X v Y	OR
1	1	1	1	X − Y	SUB

32 33

0	0	-
0	1	R
1	0	L
1	1	C

Shift Selection

No Shift
Right End Off
Left End Off
Right Circular

34 35 36

0			A1 Unchanged
1			BSW → A1
	0		A2 Unchanged
	1		BSW → A2
		0	A3 Unchanged
		1	BSW → A3

A Register Input Selection

37 38 39 40

0	0	0	0	None
0	0	0	1	Complement of 4-bit carries (BC4)
1	0	0	0	ADDER (BAD)
1	0	0	1	Complement of 8-bit carries (BC8)
1	0	1	0	BSW v ADDER (BBA)
1	0	1	1	BSW
1	1	0	0	EXT (BEX)
1	1	0	1	MIR (BMI)
1	1	1	0	BSW v EXT (BBE)
1	1	1	1	BSW v MIR (BBI)

B Register Input Selection

41

0	No Change
1	BSW → MIR

MIR Input Selection

42

0	No Change
1	BSW Least Bits → AMPCR

AMPCR Input Selection

43

0	No Change
1	BSW Next Least Byte → BR1

BR1 Input Selection

44

0	No Change
1	BSW Next Least Byte to BR2

BR2 Input Selection

45 46

0		No Change
1	0	LIT to MAR
1	1	BSW Least Byte to MAR

MAR Input Selection

46 47 48

-	0	0	No Change
0	0	1	$\overline{LIT}$ to CTR (LCTR)
1	0	1	$\overline{BSW}$ Least Byte to CTR (CTR)
-	1	0	Increment CTR (MOD 256) (INC)

Counter Input Selection

49 50

0	0	No change
0	1	Complement SAR (CSAR)
1	0	BSW Least Bits → SAR (SAR)

SAR Input Selection

51 52 53 54

0	0	0	0	No Change
0	0	0	1	- - -
0	0	1	0	MR1
0	0	1	1	MR2
0	1	0	0	DLD
0	1	0	1	- - -
0	1	1	0	MW1
0	1	1	1	MW2
1	0	0	0	ASR
1	0	0	1	ASE
1	0	1	0	DR1
1	0	1	1	DR2
1	1	0	0	USEL
1	1	0	1	USEL
1	1	1	0	DW1
1	1	1	1	DW2

MDOP

55

0	$\overline{SHIFT}$ - NO ACTION/SHIFT - ENDOFF → SSF
1	$\overline{SHIFT}$-AOV → SSF/SHIFT-ENDOFF → SSF → BSW

SSC

56

0	PARITY (ON OR OFF TO MAKE TOTAL
1	BITS ODD)

Fig. II-3 MICROCODE FORMAT, NANOWORD CONTENTS, AND NANOCODE FORMAT
(SHEET 2 OF 2)

Functional Detail

TABLE II-1. NANO LIST

MICRO CODE	NANO ADDRS		NANO CODE
		FIRST GROUP OF 256	
F000	0000 *	WAIT.	0000 0000 0000 0100
F001	0001	A1.	0009 A000 0000 0100
F002	0002 *	IF GC1 STEP ELSE SKIP.	080B 0000 0000 0100
F003	0003	A1 EQV B.	0009 AC52 0000 0000
F004	0004	A1 EQV B000.	0009 A012 0000 0100
F005	0005 *	IF GC1 STEP ELSE RETN.	080F 0000 0000 0000
F006	0006 *	SET GC1.	0189 0000 0000 0100
F007	0007	A1 – AMPCR.	0009 0640 4000 0100
F008	0008 *	IF GC1 SKIP.	0819 0000 0000 0100
F009	0009	A1 = A1 AND LIT.	0009 A156 4000 0100
F00A	000A	A1 = A1 – LIT.	0009 A15E 4000 0000
F00B	000B	A1 = A1 L.	0009 A001 4000 0100
F00C	000C *	RESET GC1.	0149 0000 0000 0100
F00D	000D	A1 = A1 R.	0009 A000 C000 0100
F00E	000E *	IF NOT GC1 EXEC.	0021 0000 0000 0100
F00F	000F	A1 = A1 – 1.	0009 A0DE 4000 0000
F010	0010	A1 = A1 + B.	0009 AC40 4000 0100
F011	0011	A1 = A1 + LIT.	0009 A140 4000 0000
F012	0012	A1 = A1 + 1.	0009 A0C0 4000 0000
F013	0013	A1 = A2.	0009 C000 4000 0000
F014	0014 *	IF LC1 SKIP.	2819 0000 0000 0000
F015	0015 *	IF LC2 SKIP.	3819 0000 0000 0100
F016	0016	A1 = A3.	0009 E000 4000 0100
F017	0017	A1 = B.	0009 0C40 4000 0100
F018	0018 *	SET LC1.	01C9 0000 0000 0000
F019	0019 *	SET LC2.	0049 0000 0000 0000
F01A	001A *	SET LC3.	0109 0000 0000 0000
F01B	001B	A1 = B L.	0009 0C41 4000 0000
F01C	001C	A1 = BMAR.	0009 0F40 4000 0100
F01D	001D	A1 = LIT.	0009 2000 4000 0100
F01E	001E *	IF LC3 SKIP. (Bit 5 is insignificant.)	D819 0000 0000 0000
F01F	001F *	RESET GC2.	00C9 0000 0000 0100
F020	0020	A1 = LIT + B.	0009 2C40 4000 0000
F021	0021	A2.	0009 C000 0000 0100
F022	0022	A2 EQV B000.	0009 C012 0000 0100
F023	0023	A2 = AMPCR.	0009 0640 2000 0100
F024	0024	A2 = A1.	0009 A000 2000 0000
F025	0025	A2 = A2 C.	0009 C001 A000 0000
F026	0026	A2 = A2 L.	0009 C001 2000 0100
F027	0027	A2 = A2 R.	0009 C000 A000 0100
F028	0028	A2 = A2 OR B.	0009 CC5C 2000 0000
F029	0029	A2 = A2 + LIT.	0009 C140 2000 0000
F02A	002A	A2 = A2 + 1.	0009 C0C0 2000 0000
F02B	002B	A2 = A2 – 1.	0009 C0DE 2000 0000
F02C	002C	A2 NAN LIT.	0009 C148 0000 0000
F02D	002D	A2 = A2 AND LIT.	0009 C156 2000 0100
F02E	002E *	IF COV SKIP. (Bit 5 is insignificant.)	8819 0000 0000 0000
F02F	002F	A2 = A2 OR LIT.	0009 C15C 2000 0100

NOTE: * INDICATES ENTRY OUT OF ALPHABETICAL ORDER.

Functional Detail

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F030	0030 *	INC.	0009 0000 0002 0000
F031	0031	A2 = A2 + B.	0009 CC40 2000 0100
F032	0032	A2 - A3.	0009 E000 2000 0100
F033	0033	A2 = B.	0009 0C40 2000 0100
F034	0034	A2 = B000.	0009 0000 2000 0000
F035	0035	A2 - BMAR.	0009 0F40 2000 0100
F036	0036	A2 = B L.	0009 0C41 2000 0000
F037	0037	A2 = B R.	0009 0C40 A000 0000
F038	0038	A2 = LIT.	0009 2000 2000 0100
F039	0039	A2 = LIT L.	0009 2001 2000 0000
F03A	003A	A2 = LIT + B.	0009 2C40 2000 0000
F03B	003B	A3.	0009 E000 0000 0000
F03C	003C	A3 EQV B.	0009 EC52 0000 0100
F03D	003D	A3 EQV B000.	0009 E012 0000 0000
F03E	003E	A3 EQV LIT.	0009 E152 0000 0000
F03F	003F	A3 EQV Z.	0009 ED52 0000 0000
F040	0040	A3 – B.	0009 EC5E 0000 0100
F041	0041	A3 = AMPCR.	0009 0640 1000 0100
F042	0042	A3 = A1.	0009 A000 1000 0000
F043	0043	A3 = A2.	0009 C000 1000 0000
F044	0044	A3 = A3 C.	0009 E001 9000 0100
F045	0045	A3 = A3 L.	0009 E001 1000 0000
F046	0046	A3 = A3 R.	0009 E000 9000 0000
F047	0047	A3 = A3 AND LIT.	0009 E156 1000 0000
F048	0048	A3 = A3 OR B.	0009 EC5C 1000 0100
F049	0049	A3 = A3 XOR B.	0009 EC4C 1000 0000
F04A	004A	A3 = A3 OR LIT.	0009 E15C 1000 0000
F04B	004B	A3 = A3 – 1.	0009 E0DE 1000 0100
F04C	004C	A3 = A3 + 1.	0009 E0C0 1000 0100
F04D	004D	A3 = A3 + B.	0009 EC40 1000 0000
F04E	004E	A3 = A3 + LIT.	0009 E140 1000 0100
F04F	004F	A3 = A3 – LIT.	0009 E15E 1000 0100
F050	0050 *	IF ABT SET LC1.	6BC9 0000 0000 0000
F051	0051	A3 = B.	0009 0C40 1000 0100
F052	0052	A3 = B L.	0009 0C41 1000 0000
F053	0053	A3 = B R.	0009 0C40 9000 0000
F054	0054	A3 = B000.	0009 0000 1000 0000
F055	0055	A3 = B001.	0009 00C0 1000 0000
F056	0056	A3 = BMAR.	0009 0F40 1000 0100
F057	0057	A3 = LIT L.	0009 2001 1000 0000
F058	0058	A3 = LIT.	0009 2000 1000 0100
F059	0059	A3 = LIT AND B.	0009 2C56 1000 0100
F05A	005A	A3 = Z.	0009 8000 1000 0100
F05B	005B	AMPCR = B.	0009 0C40 0040 0100
F05C	005C	AMPCR = A1.	0009 A000 0040 0000
F05D	005D	ASE.	0009 0000 0000 2500
F05E	005E	ASR.	0009 0000 0000 2000
F05F	005F	B.	0009 0C40 0000 0000
F060	0060	B = AMPCR.	0009 0640 0800 0100
F061	0061	B = A1 L.	0009 A001 0B00 0100
F062	0062	B = A1 AND LIT.	0009 A156 0B00 0100

NOTE: * INDICATES ENTRY OUT OF ALPHABETICAL ORDER.

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F063	0063	B = A1 + B.	0009 AC40 0B00 0100
F064	0064	B = A1 – B.	0009 AC5E 0B00 0100
F065	0065	B = A1 OR B.	0009 AC5C 0B00 0000
F066	0066	B = A1.	0009 A000 0B00 0000
F067	0067	B = A1 R.	0009 A000 8B00 0100
F068	0068	B = A2.	0009 C000 0B00 0000
F069	0069	B = A2 R.	0009 C000 8B00 0100
F06A	006A	B = A2 L.	0009 C001 0B00 0100
F06B	006B	B = A2 + B.	0009 CC40 0B00 0100
F06C	006C	B = A2 OR B.	0009 CC5C 0B00 0000
F06D	006D	B = A2 AND LIT.	0009 C156 0B00 0100
F06E	006E	B = A3 + B.	0009 EC40 0B00 0000
F06F	006F	B = A3 OR B.	0009 EC5C 0B00 0100
F070	0070	B = A3 – B.	0009 EC5E 0B00 0000
F071	0071	B = A3.	0009 E000 0B00 0100
F072	0072	B = A3 R.	0009 E000 8B00 0000
F073	0073	B = A3 L.	0009 E001 0B00 0000
F074	0074	B = A3 AND LIT.	0009 E156 0B00 0000
F075	0075	B = BTT0.	0009 0C00 0B00 0000
F076	0076	B = B111.	0009 001A 0B00 0100
F077	0077	B = B001.	0009 00C0 0B00 0000
F078	0078	B = B0TT.	0009 0440 0B00 0000
F079	0079	B = B100.	0009 1800 0B00 0000
F07A	007A	B = B1TT.	0009 1C40 0B00 0000
F07B	007B	B = B000.	0009 0000 0B00 0000
F07C	007C	B = B L.	0009 0C41 0B00 0000
F07D	007D	B = B C.	0009 0C41 8B00 0100
F07E	007E	B = B + 1.	0009 0C46 CB00 0100
F07F	007F	B = B R.	0009 0C40 8B00 0000
F080	0080	B = BMAR.	0009 0F40 0B00 0100
F081	0081	B = NOT CTR R.	0009 6010 8B00 0000
F082	0082	B = LIT L.	0009 2001 0B00 0000
F083	0083	B = LIT + B.	0009 2C40 0B00 0000
F084	0084	B = LIT NRI B.	0009 2C44 0B00 0100
F085	0085	B = LIT XOR B.	0009 2C4C 0B00 0000
F086	0086	B = LIT AND B.	0009 2C56 0B00 0100
F087	0087	B = LIT OR B.	0009 2C5C 0B00 0100
F088	0088	B = LIT – B.	0009 2C5E 0B00 0000
F089	0089	B = LIT.	0009 2000 0B00 0100
F08A	008A	B = Z.	0009 8000 0B00 0100
F08B	008B	BBI = B.	0009 0C40 0F00 0000
F08C	008C	BMI, MIR = B.	0009 0C40 0D80 0000
F08D	008D	BMI.	0009 0000 0D00 0000
F08E	008E	BR2 = A2 OR B100.	0009 D81C 0010 0100
F08F	008F	BR2 = LIT L.	0009 2001 0010 0000
F090	0090	BR2 = A2.	0009 C000 0010 0000
F091	0091	CALL.	0036 0000 0000 0100
F092	0092	CSAR.	0009 0000 0000 4000
F093	0093	CSAR, B = B L.	0009 0C41 0B00 4100
F094	0094	CTR = B001 + 1.	0009 00C6 0005 0100
F095	0095	CTR = B.	0009 0C40 0005 0000
F096	0096	DR1 BEX.	0009 0000 0C00 2900
F097	0097	DR2 BEX.	0009 0000 0C00 2C00

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F098	0098	DW2.	0009 0000 0000 3D00
F099	0099	DW1.	0009 0000 0000 3800
F09A	009A	EXEC.	0024 0000 0000 0100
F09B	009B	IF ABT LUOP, JUMP.	6C29 0000 0000 0000
F09C	009C	IF ABT JUMP.	6829 0000 0000 0100
F09D	009D	IF ABT SKIP.	6819 0000 0000 0100
F09E	009E	IF AOV SKIP.	7819 0000 0000 0000
F09F	009F	IF COV JUMP.	8829 0000 0000 0000
F0A0	00A0	IF EXT SKIP.	C819 0000 0000 0100
F0A1	00A1	IF GC1 JUMP.	0829 0000 0000 0100
F0A2	00A2	IF GC2 SKIP.	1819 0000 0000 0000
F0A3	00A3	IF IRQ EXEC.	B821 0000 0000 0100
F0A4	00A4	IF IRQ JUMP.	B829 0000 0000 0000
F0A5	00A5	IF LC1 STEP.	2809 0000 0000 0100
F0A6	00A6	IF LC1 JUMP.	2829 0000 0000 0000
F0A7	00A7	IF LC1 SET LC1 ELSE SKIP.	2BC8 0000 0000 0000
F0A8	00A8	IF LC1 SET LC1 SKIP.	2BD9 0000 0000 0000
F0A9	00A9	IF LC2 STEP.	3809 0000 0000 0000
F0AA	00AA	IF LC2 JUMP.	3829 0000 0000 0100
F0AB	00AB	IF LC2 SET LC2 ELSE SKIP.	3A4B 0000 0000 0100
F0AC	00AC	IF LC2 SET LC2 SKIP.	3A59 0000 0000 0100
F0AD	00AD	IF LC3 STEP.	D809 0000 0000 0100
F0AE	00AE	IF LC3 SET LC3 SKIP.	D819 0000 0000 0000
F0AF	00AF	IF LC3 SET LC3 ELSE SKIP.	D808 0000 0000 0000
F0B0	00B0	IF LST SET LC1.	5BC9 0000 0000 0000
F0B1	00B1	IF LST JUMP.	5829 0000 0000 0100
F0B2	00B2	IF LST SKIP.	5819 0000 0000 0100
F0B3	00B3	IF MST SKIP.	4819 0000 0000 0000
F0B4	00B4	IF NOT ABT JUMP.	6029 0000 0000 0000
F0B5	00B5	IF NOT ABT SKIP.	6019 0000 0000 0000
F0B6	00B6	IF NOT AOV JUMP.	7029 0000 0000 0100
F0B7	00B7	IF NOT AOV SKIP.	7019 0000 0000 0100
F0B8	00B8	IF NOT COV SKIP.	8019 0000 0000 0100
F0B9	00B9	IF NOT COV JUMP.	8029 0000 0000 0100
F0BA	00BA	IF NOT EXT SKIP.	C019 0000 0000 0000
F0BB	00BB	IF NOT GC1 SKIP.	0019 0000 0000 0000
F0BC	00BC	IF NOT GC2 SKIP.	1019 0000 0000 0100
F0BD	00BD	IF NOT IRQ SKIP.	B019 0000 0000 0100
F0BE	00BE	IF NOT LC1 JUMP.	2029 0000 0000 0100
F0BF	00BF	IF NOT LC1 SKIP.	2019 0000 0000 0100
F0C0	00C0	IF NOT LC2 SKIP.	3019 0000 0000 0000
F0C1	00C1	IF NOT LC3 SKIP.	D019 0000 0000 0100
F0C2	00C2	IF NOT LST JUMP.	5029 0000 0000 0000
F0C3	00C3	IF NOT LST SKIP.	5019 0000 0000 0000
F0C4	00C4	IF NOT MST SKIP.	4019 0000 0000 0100
F0C5	00C5	IF SRQ THEN DR2 BEX SKIP.	EE19 0000 0C00 2D00
F0C6	00C6	IF SRQ DW2 SKIP.	EA19 0000 0000 3D00
F0C7	00C7	IF URQ SET LC2 ELSE JUMP.	FA4D 0000 0000 0100
F0C8	00C8	INC IF COV SKIP.	8819 0000 0002 0100
F0C9	00C9	JUMP.	002D 0000 0000 0100
F0CA	00CA	LCTR.	0009 0000 0001 0000
F0CB	00CB	LIT EQV B.	0009 2C52 0000 0100

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F0CC	00CC	LIT – B.	0009 2C5E 0000 0100
F0CD	00CD	LIT NAN B.	0009 2C48 0000 0000
F0CE	00CE	LMAR.	0009 0000 0008 0000
F0CF	00CF	MAR1 = AMPCR.	0009 0640 002C 0100
F0D0	00D0	MAR1 = A1.	0009 A000 002C 0000
F0D1	00D1	MAR1 = A2.	0009 C000 002C 0000
F0D2	00D2	MAR1 = A3.	0009 E000 002C 0100
F0D3	00D3	MAR1 = A3 + LIT.	0009 E140 002C 0100
F0D4	00D4	MAR1 = A3 + 1.	0009 E000 002C 0100
F0D5	00D5	MAR1 = B.	0009 0C40 002C 0100
F0D6	00D6	MAR1 = B + 1.	0009 0C46 002C 0100
F0D7	00D7	MAR1 = BMAR + 1.	0009 0F46 002C 0100
F0D8	00D8	MAR1 = LIT.	0009 2000 002C 0100
F0D9	00D9	MAR1 = LIT + B.	0009 2C40 002C 0000
F0DA	00DA	MIR = AMPCR.	0009 0640 0080 0100
F0DB	00DB	MIR = A1	0009 A000 0080 0000
F0DC	00DC	MIR = A1 + B.	0009 AC40 0080 0100
F0DD	00DD	MIR = A2.	0009 C000 0080 0000
F0DE	00DE	MIR = A3.	0009 E000 0080 0100
F0DF	00DF	MIR = A3 OR B.	0009 EC5C 0080 0100
F0E0	00E0	MIR = A3 OR LIT.	0009 E15C 0080 0000
F0E1	00E1	MIR = B.	0009 0C40 0080 0100
F0E2	00E2	MIR = B C.	0009 0C41 8080 0100
F0E3	00E3	MIR = B + 1.	0009 0C46 0080 0100
F0E4	00E4	MIR = B L.	0009 0C41 0080 0000
F0E5	00E5	MIR = B R.	0009 0C40 8080 0000
F0E6	00E6	MIR = B000.	0009 0000 0080 0000
F0E7	00E7	MIR = B001.	0009 00C0 0080 0000
F0E8	00E8	MIR = B111.	0009 001A 0080 0100
F0E9	00E9	MIR = BMAR.	0009 0F40 0080 0100
F0EA	00EA	MIR = LIT.	0009 2000 0080 0100
F0EB	00EB	MIR = LIT AND B.	0009 2C56 0080 0100
F0EC	00EC	MIR = LIT OR B.	0009 2C5C 0080 0100
F0ED	00ED	MIR = LIT + B.	0009 2C40 0080 0000
F0EE	00EE	MIR = LIT L.	0009 2001 0080 0000
F0EF	00EF	MIR = Z.	0009 8000 0080 0100
F0F0	00F0	MIR = 0 + Z + 1.	0009 0D46 0080 0000
F0F1	00F1	MR1.	0009 0000 0000 0800
F0F2	00F2	MR1 A1 = A1 + 1.	0009 A0C0 4000 0900
F0F3	00F3	MW1.	0009 0000 0000 1900
F0F4	00F4	SAR = B.	0009 0C40 0000 8100
F0F5	00F5	SAVE.	0012 0000 0000 0100
F0F6	00F6	SET GC2.	0089 0000 0000 0000
F0F7	00F7	SKIP.	001B 0000 0000 0100
F0F8	00F8	WHEN IRQ STEP.	B808 0000 0000 0000
F0F9	00F9	WHEN RDC BEX.	AC08 0000 0C00 0000
F0FA	00FA	WHEN RDC BEX, MAR1 = BMAR + 1.	AC08 0F46 0C2C 0000
F0FB	00FB	WHEN RMI MAR1 = BMAR + 1.	9C08 0F46 002C 0000
F0FC	00FC	WHEN SRQ STEP.	E808 0000 0000 0000
FoFD	00FD	WHEN URQ STEP.	F808 0000 0000 0100
F0FE	00FE	Z EQV B.	0009 8C52 0000 0100
F0FF	00FF	0 EQV B.	0009 0C52 0000 0000

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
		SECOND GROUP OF 256	
F100	0100	AMPCR = A1 + AMPCR.	0009 A640 0040 0100
F101	0101	AMPCR = A3.	0009 E000 0040 0100
F102	0102	AMPCR = A2.	0009 C000 0040 0000
F103	0103	AMPCR = A2 + AMPCR.	0009 C640 0040 0100
F104	0104	AMPCR = A3 + AMPCR.	0009 E640 0040 0000
F105	0105	AMPCR = AMPCR + 1.	0009 0646 0040 0100
F106	0106	AMPCR = LIT + B.	0009 2C40 0040 0000
F107	0107	ASE, BMI, MAR1 = B, JUMP.	002D 0C40 0D20 2400
F108	0108	ASR BEX.	0009 0000 0C00 2000
F109	0109	A1 – LIT – 1.	0009 A158 0000 0100
F10A	010A	A1 = LIT EQV B.	0009 2C52 4000 0000
F10B	010B	A1 = A1 C.	0009 A001 C000 0000
F10C	010C	A1 = A1 NIM B.	0009 AC4E 4000 0000
F10D	010D	A1 = A1 OR B.	0009 AC5C 4000 0000
F10E	010E	A1 = B + 1.	0009 0C46 4000 0100
F10F	010F	A1 = B000.	0009 0000 4000 0000
F110	0110	A1 = B111 R.	0009 001A C000 0000
F111	0111	A1 EQV LIT.	0009 A152 0000 0100
F112	0112	A1 EQV Z.	0009 AD52 0000 0100
F113	0113	A1 = LIT – B.	0009 2C5E 4000 0000
F114	0114	A1 EQV 0, IF COV SKIP.	8819 A012 0000 0000
F115	0115	A1 = Z.	0009 8000 4000 0100
F116	0116	A2 EQV B.	0009 CC52 0000 0000
F117	0117	A2 EQV LIT.	0009 C152 0000 0100
F118	0118	A2 EQV 0, IF LC2 SET LC2 SKIP.	3A59 C012 0000 0100
F119	0119	A2 – B.	0009 CC5E 0000 0000
F11A	011A	A2 – B – 1.	0009 CC58 0000 0000
F11B	011B	A2 – LIT.	0009 C15E 0000 0100
F11C	011C	A2 RIM LIT.	0009 C15A 0000 0000
F11D	011D	A2 = A2 + AMPCR.	0009 C640 2000 0100
F11E	011E	A2 = A2 – B.	0009 CC5E 2000 0100
F11F	011F	A2 = A2 – LIT.	0009 C15E 2000 0000
F120	0120	A2 = A2 XOR LIT.	0009 C14C 2000 0000
F121	0121	A2 = A2 XOR B111.	0009 C012 2000 0000
F122	0122	A2 = A3 L.	0009 E001 2000 0000
F123	0123	A2 = B C.	0009 0C41 A000 0100
F124	0124	A2 EQV Z.	0009 CD52 0000 0100
F125	0125	A2 = LIT C.	0009 2001 A000 0100
F126	0126	A2 = LIT AND B.	0009 2C56 2000 0100
F127	0127	A2 = LIT – B.	0009 2C5E 2000 0000
F128	0128	A2 = Z.	0009 8000 2000 0100
F129	0129	A2 BC4 = A3 + B.	0009 EC40 2100 0100
F12A	012A	A3 NAN B.	0009 EC48 0000 0000
F12B	012B	A3 – B – 1.	0009 EC58 0000 0100
F12C	012C	A3 – LIT.	0009 E15E 0000 0000
F12D	012D	A3 = A2 C.	0009 C001 9000 0000
F12E	012E	A3 = A2 L.	0009 C001 1000 0100
F12F	012F	A3 = A2 R.	0009 C000 9000 0100
F130	0130	A3 = A3 AND B.	0009 EC56 1000 0100
F131	0131	A3 = A3 – B.	0009 EC5E 1000 0000
F132	0132	A3 = A3 NIM B.	0009 EC4E 1000 0100

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F133	0133	A3 = A3 AND B110.	0009 E0CE 1000 0000
F134	0134	A3 = A3 – B C, IF NOT AOV SET LC1, JUMP ELSE JUMP.	73ED EC5F 9000 0100
F135	0135	A3 = A3 – B C, IF AOV SET LC1, JUMP ELSE JUMP.	7BED EC5F 9000 0000
F136	0136	A3 = A3 XOR LIT.	0009 E14C 1000 0100
F137	0137	A3 = B110.	0009 00DA 1000 0100
F138	0138	A3 = B111 L.	0009 001B 1000 0000
F139	0139	A3 = B111 R.	0009 001A 9000 0000
F13A	013A	A3 = B + 1.	0009 0C46 1000 0100
F13B	013B	A3 = LIT NRI B.	0009 2C44 1000 0100
F13C	013C	A3 = LIT + B.	0009 2C40 1000 0000
F13D	013D	A3 = 0 + LIT..	0009 0140 1000 0000
F13E	013E	A3 SSC = A2 L.	0009 C001 1000 0200
F13F	013F	A3 SSC = A2 R.	0009 C000 9000 0200
F140	0140	A3 SSC = LIT + B.	0009 2C40 1000 0300
F141	0141	B = A1 AND B.	0009 AC56 0B00 0000
F142	0142	B = A1 XOR B.	0009 AC4C 0B00 0100
F143	0143	B = A2 AND B.	0009 CC56 0B00 0000
F144	0144	B = A2 NIM B.	0009 CC4E 0B00 0000
F145	0145	B = A2 XOR B.	0009 CC4C 0B00 0100
F146	0146	B = A2 – LIT.	0009 C15E 0B00 0000
F147	0147	B = A2 C.	0009 C001 8B00 0000
F148	0148	B = A3 – 1.	0009 E0DE 0B00 0100
F149	0149	B = A3 + 1.	0009 E0C0 0B00 0100
F14A	014A	B = A3 AND B.	0009 EC56 0B00 0100
F14B	014B	B = A3 C.	0009 E001 8B00 0100
F14C	014C	B = A3 NRI B.	0009 EC44 0B00 0100
F14D	014D	B - A3 NRI B C.	0009 EC45 8B00 0100
F14E	014E	B = A3 XOR B R.	0009 EC4C 8B00 0100
F14F	014F	B = A3 R, IF ABT SKIP.	6819 E000 8B00 0000
F150	0150	B = B000 JUMP.	002D 0000 0B00 0000
F151	0151	B = B001 JUMP.	002D 00C0 0B00 0000
F152	0152	B = B100 JUMP.	002D 1800 0B00 0000
F153	0153	B = B101.	0009 18C0 0B00 0000
F154	0154	B = B111 R.	0009 001A 8B00 0000
F155	0155	B = B01T.	0009 189A 0B00 0000
F156	0156	B = BT00.	0009 0800 0B00 0100
F157	0157	B = BT0T.	0009 0840 0B00 0000
F158	0158	B = BTT1.	0009 0CC0 0B00 0000
F159	0159	B = BFTF.	0009 1480 0B00 0100
F15A	015A	B = CTR.	0009 6000 0B00 0000
F15B	015B	B = LIT – 1.	0009 20DE 0B00 0100
F15C	015C	B = LIT NRI B C.	0009 2C45 8B00 0100
F15D	015D	B = LIT XOR B L.	0009 2C4D 0B00 0100
F15E	015E	B = Z AAD B.	0009 8C54 0B00 0000
F15F	015F	B = Z IMP B.	0009 8C50 0B00 0100
F160	0160	B = Z NAN B.	0009 8C48 0B00 0100
F161	0161	B = Z NOR B.	0009 8C42 0B00 0100
F162	0162	B = 0 – B.	0009 0C5E 0B00 0100
F163	0163	B = 0 – B – 1.	0009 0C58 0B00 0100
F164	0164	B = 0 – LIT.	0009 015E 0B00 0000
F165	0165	B = 0 – LIT – 1.	0009 0158 0B00 0000

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F166	0166	BAD A3 = A3 + B.	0009 EC40 1800 0100
F167	0167	BBI = B R.	0009 0C40 8F00 0100
F168	0168	BC4.	0009 0000 0100 0000
F169	0169	BC4 CSAR, A3 = A3 – B C.	0009 EC5F 8100 4000
F16A	016A	BC4 SAR = B001.	0009 00C0 0100 8100
F16B	016B	BC8.	0009 0000 0900 0100
F16C	016C	BR1 = LIT L.	0009 2001 0020 0000
F16D	016D	BR2 = A3 L.	0009 E001 0010 0000
F16E	016E	BR2 = B.	0009 0C40 0010 0100
F16F	016F	BR2 = B1TT.	0009 1C40 0010 0000
F170	0170	CSAR A1 = A3 L.	0009 E001 4000 4100
F171	0171	CSAR A3 = B R.	0009 0C40 9000 4100
F172	0172	CSAR, B = B C.	0009 0C41 8B00 4000
F173	0173	CSAR BC4 A3 = A3 + B C.	0009 EC41 9100 4000
F174	0174	CSAR MIR = B000.	0009 0000 0080 4100
F175	0175	CTR = A1.	0009 A000 0005 0100
F176	0176	CTR = A1, IF ABT SKIP.	6819 A000 0005 0100
F177	0177	CTR = A2 R.	0009 C000 8005 0000
F178	0178	CTR = A3.	0009 E000 0005 0000
F179	0179	CTR = BMAR + 1.	0009 0F46 0005 0000
F17A	017A	CTR = CTR + LIT + 1.	0009 6146 0005 0100
F17B	017B	CTR EQV 0.	0009 6012 0000 0100
F17C	017C	CTR = LIT + CTR	0009 2B00 0005 0100
F17D	017D	DLD.	0009 0000 0000 1000
F17E	017E	DR2 BEX, BR2 = B.	0009 0C40 0C10 2C00
F17F	017F	IF ABT LUOP ELSE SKIP.	6C0B 0000 0000 0000
F180	0180	IF ABT RESET GC1.	6B49 0000 0000 0100
F181	0181	IF ABT RESET GC2.	6AC9 0000 0000 0100
F182	0182	IF ABT SET LC2.	6A49 0000 0000 0000
F183	0183	IF AOV JUMP.	7829 0000 0000 0000
F184	0184	IF GC1 SET LC1 SKIP.	0BD9 0000 0000 0100
F185	0185	IF GC1 SET LC2 SKIP.	0A59 0000 0000 0100
F186	0186	IF GC1 STEP ELSE EXEC.	080C 0000 0000 0000
F187	0187	IF GC1 STEP ELSE JUMP.	080D 0000 0000 0100
F188	0188	IF GC1 STEP ELSE SAVE.	080A 0000 0000 0000
F189	0189	IF GC1 STEP ELSE WAIT.	0808 0000 0000 0100
F18A	018A	IF GC1 RETN.	0839 0000 0000 0000
F18B	018B	IF GC1 SAVE.	0811 0000 0000 0000
F18C	018C	IF GC1 WAIT.	0801 0000 0000 0100
F18D	018D	IF IRQ, ASR, BEX, JUMP.	BE29 0000 0C00 2100
F18E	018E	IF IRQ SKIP.	B819 0000 0000 0000
F18F	018F	IF LC1 A2 = A2 + 1.	2C09 C0C0 2000 0100
F190	0190	IF LC1 INC.	2C09 0000 0002 0100
F191	0191	IF LC1 SET LC1 ELSE JUMP.	2BCD 0000 0000 0000
F192	0192	IF LC2 SET LC2 ELSE JUMP.	3A4D 0000 0000 0100
F193	0193	IF LC2 SET LC2 JUMP.	3A69 0000 0000 0100
F194	0194	IF LC3 SET LC3 ELSE JUMP.	DB0D 0000 0000 0000
F195	0195	IF LST CALL.	5831 0000 0000 0100
F196	0196	IF LST SET GC1.	5B89 0000 0000 0100
F197	0197	IF LST SET LC2.	5A49 0000 0000 0000
F198	0198	IF LST SET LC2 SKIP.	5A59 0000 0000 0100
F199	0199	IF NOT ABT RESET GC1.	6349 0000 0000 0000

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F19A	019A	IF NOT ABT SET GC1.	6389 0000 0000 0000
F19B	019B	IF NOT ABT SET LC1.	63C9 0000 0000 0100
F19C	019C	IF NOT GC1 JUMP.	0029 0000 0000 0000
F19D	019D	IF NOT GC1 SET GC1 JUMP.	03A9 0000 0000 0100
F19E	019E	IF NOT GC1 STEP ELSE SKIP.	000B 0000 0000 0000
F19F	019F	IF NOT GC2 JUMP.	1029 0000 0000 0100
F1A0	01A0	IF NOT GC2 LUOP SKIP.	1419 0000 0000 0000
F1A1	01A1	IF NOT GC2 SET GC2 JUMP.	12A9 0000 0000 0100
F1A2	01A2	IF NOT LC1 SET LC1.	23C9 0000 0000 0000
F1A3	01A3	IF NOT LC1 SET LC1 ELSE SKIP.	23CB 0000 0000 0100
F1A4	01A4	IF NOT LC1 SET LC1 SKIP.	23D9 0000 0000 0100
F1A5	01A5	IF NOT LC1 SET LC1 JUMP.	23E9 0000 0000 0100
F1A6	01A6	IF NOT LC2 SET LC2 JUMP.	3269 0000 0000 0000
F1A7	01A7	IF NOT LC3 JUMP.	D029 0000 0000 0100
F1A8	01A8	IF NOT LC3 SET LC3 JUMP.	D329 0000 0000 0100
F1A9	01A9	IF NOT LC3 SET LC3 SKIP.	D319 0000 0000 0100
F1AA	01AA	IF NOT LST SET GC2 JUMP.	52A9 0000 0000 0000
F1AB	01AB	IF NOT MST JUMP.	4029 0000 0000 0100
F1AC	01AC	IF NOT IRQ JUMP.	B029 0000 0000 0100
F1AD	01AD	IF NOT SRQ SKIP.	E019 0000 0000 0100
F1AE	01AE	IF NOT URQ SKIP.	F019 0000 0000 0000
F1AF	01AF	IF MST JUMP.	4829 0000 0000 0000
F1B0	01B0	IF MST SET LC1.	4BC9 0000 0000 0100
F1B1	01B1	IF SRQ THEN DW2 JUMP.	EA29 0000 0000 3D00
F1B2	01B2	IF URQ SET GC1 ELSE JUMP.	FB8D 0000 0000 0000
F1B3	01B3	IF URQ SET GC2 ELSE JUMP.	FA8D 0000 0000 0100
F1B4	01B4	IF URQ SET LC2.	FA49 0000 0000 0000
F1B5	01B5	IF URQ SKIP.	F819 0000 0000 0100
F1B6	01B6	INC, B= BMAR.	0009 0F40 0B02 0000
F1B7	01B7	INC IF COV JUMP.	8829 0000 0002 0100
F1B8	01B8	INC, IF NOT COV SKIP ELSE STEP.	8019 0000 0002 0000
F1B9	01B9	INC, SAVE.	0012 0000 0002 0000
F1BA	01BA	LIT EQV 0.	0009 2012 0000 0000
F1BB	01BB	LIT IMP B.	0009 2C50 0000 0000
F1BC	01BC	MAR1 = A1 + LIT.	0009 A140 002C 0000
F1BD	01BD	MAR1 = A2 + 1.	0009 C0C0 002C 0000
F1BE	01BE	MAR1 = A2 + B.	0009 CC40 002C 0100
F1BF	01BF	MAR1 = A2 + LIT.	0009 C140 002C 0000
F1C0	01C0	MAR1 = A3 + AMPCR.	0009 E640 002C 0000
F1C1	01C1	MAR1 = A3 – B.	0009 EC5E 002C 0000
F1C2	01C2	MAR1 = B R. (B711)	0009 0C40 802C 0000
F1C2	01C2	MAR1 = B R, SKIP. (B705)	001B 0C40 802C 0000
F1C3	01C3	MAR1 = B001.	0009 00C0 002C 0000
F1C4	01C4	MAR1 = B001 + 1.	0009 00C6 002C 0000
F1C5	01C5	MAR1 = BMAR + 1 IF NOT COV JUMP ELSE SAVE.	802A 0F46 002C 0100
F1C6	01C6	MAR1 = LIT XOR BMAR.	0009 2F4C 002C 0000
F1C7	01C7	MIR = AMPCR + 1.	0009 0646 0080 0100
F1C8	01C8	MIR = A1 L.	0009 A001 0080 0100
F1C9	01C9	MIR = A2 L.	0009 C001 0080 0100

TABLE II-1. NANO LIST (Cont.)

MICRO CODE	NANO ADDRS		NANO CODE
F1CA	01CA	MIR = A2 + B.	0009 CC40 0080 0100
F1CB	01CB	MIR = A2 OR B.	0009 CC5C 0080 0000
F1CC	01CC	MIR = A2 OR LIT.	0009 C15C 0080 0100
F1CD	01CD	MIR = A3 L	0009 E001 0080 0000
F1CE	01CE	MIR = A3 R.	0009 E000 8080 0000
F1CF	01CF	MIR = A3 AND B.	0009 EC56 0080 0100
F1D0	01D0	MIR = A3 AND LIT.	0009 E156 0080 0000
F1D1	01D1	MIR = A3 AND LIT L.	0009 E157 0080 0100
F1D2	01D2	MIR = A3 +B.	0009 EC40 0080 0000
F1D3	01D3	MIR = A3 – B.	0009 EC5E 0080 0000
F1D4	01D4	MIR = B, SAVE.	0009 0C40 0080 0100
F1D5	01D5	MIR = B001 + 1.	0009 00C6 0080 0000
F1D6	01D6	MIR = NOT CTR R.	0009 6010 8080 0000
F1D7	01D7	MIR = Z + B001.	0009 80C0 0080 0100
F1D8	01D8	MIR = 0 AAD Z.	0009 0D54 0080 0000
F1D9	01D9	MIR = 0 OAD B000.	0009 000A 0080 0000
F1DA	01DA	MIR = 0 OAD Z.	0009 0D4A 0080 0000
F1DB	01DB	MIR = 0 + Z.	0009 0D40 0080 0000
F1DC	01DC	MIR = 0 – Z.	0009 0D5E 0080 0000
F1DD	01DD	MIR = 0 – Z – 1.	0009 0D58 0080 0000
F1DE	01DE	MIR BC8 = A1 + B IC.	0009 AC60 0980 0000
F1DF	01DF	MR1, A3 = B R.	0009 0C40 9000 0900
F1E0	01E0	MR1, CTR = B.	0009 0C40 0005 0900
F1E1	01E1	MR1, IF LC1 STEP.	2819 0000 0000 0800
F1E2	01E2	MR1, INC.	0009 0000 0002 0900
F1E3	01E3	MR1, MIR = B.	0009 0C40 0080 0800
F1E4	01E4	MW1, A2 = A2 + 1.	0009 C0C0 2000 1800
F1E5	01E5	MW1, INC, A3 = A3 XOR B.	0009 EC4C 1002 1900
F1E6	01E6	RESET GC1, SAVE	0152 0000 0000 0100
F1E7	01E7	RETN.	003F 0000 0000 0100
F1E8	01E8	SAR = A2 R.	0009 C000 8000 8100
F1E9	01E9	SAR = A3 R.	0009 E000 8000 8000
F1EA	01EA	SAR = B L.	0009 0C41 0000 8000
F1EB	01EB	SET GC1, JUMP.	01AD 0000 0000 0100
F1EC	01EC	WHEN RDC BEX JUMP.	AC28 0000 0C00 0100
F1ED	01ED	WHEN RDC THEN BEX, A1 = A1 + 1, JUMP	AC28 A0C0 4C00 0000
F1EE	01EE	WHEN RDC THEN BEX, A2 = A2 + 1, JUMP.	AC28 C0C0 2C00 0000
F1EF	01EF	WHEN RDC BEX A3 = B.	AC08 0C40 1C00 0000
F1F0	01F0	WHEN RDC BEX CTR = B.	AC08 0C40 0C05 0100
F1F1	01F1	WHEN RDC BEX, MAR1 = A1.	AC08 A000 0C2C 0100
F1F2	01F2	WHEN RDC BEX, MAR1 = B, JUMP.	AC28 0C40 0C2C 0100
F1F3	01F3	WHEN RDC THEN BEX, MAR1 = BMAR +1, JUMP.	AC28 0F46 0C2C 0100
F1F4	01F4	WHEN RMI A1 = A1 + 1, JUMP.	9C28 A0C0 4000 0000
F1F5	01F5	WHEN RMI A2 = A2 + 1, JUMP.	9C28 C0C0 2000 0000
F1F6	01F6	WHEN RMI THEN MAR1 = BMAR + 1, JUMP.	9C28 0F46 002C 0100
F1F7	01F7	WHEN RMI MAR1 = LIT.	9C08 2000 002C 0000

Microcode Controls

The microcode controls stored within the Microprogram Memory can perform any one of the following functions:

a. Setting the Shift Amount Register (SAR).
b. Setting both the Shift Amount Register (SAR) and Literal register (LIT).
c. Setting the Literal register (LIT).
d. Specifying the microprogram memory address for the Alternate Microprogram Count Register (AMPCR).
e. Specifying the microprogram memory address for the Incrementer (INCR) and microprogram count register (MPCR).
f. Specifying a nanomemory address of a nanocode.

Nanocode Controls

The nanocode controls contained in the nanomemory may be constructed in a general or specific manner relative to the functions that the nanocode controls are to perform. A nanocode control may specify any or all of the following operations:

a. Testing specific conditions (Condition Selection).
b. Selecting successors (Successor Condition).
c. Selecting Logic Unit conditions (Phase 3 Modifier).
d. Selecting external operation conditions (Memory/Device/Condition Adjust Modifier).
e. Setting specific flag bits (Condition Adjust).
f. Selecting specific operands upon which logical operations are to be performed (MPAD Controls).
g. Selecting inputs to the Arithmetic/Logic Unit (X-Selection to Adder and Y-Selection to Adder).
h. Inhibiting the bit carries for the allowable Adder operations (Inhibit Carry Between Bytes).
i. Specifying any of the allowable Arithmetic/Logic Unit operations (Adder Operation).
j. Shifting the output of the Adder (Shift Selection).
k. Selecting specific destinations which are to receive inputs or remain unchanged during a specific operation (A Register Input Selection, B Register Input Selection, MIR Input Selection, or AMPCR Input Selection).
l. Selecting input data to the Base Registers (BR1 or BR2), Memory Address Register (MAR), Counter (CTR), and Shift Amount Register (SAR).
m. Reading from or writing to a memory or external device (Memory/Device Operation).
n. Performing the sign save control function.

Microinstruction Phasing

The execution of a microinstruction requires one or more sequential time periods designated phase 1, phase 3, or extended phase 3. The interval of time from the trailing edge of one clock pulse to the trailing edge of the next clock pulse is considered as one phase of a microinstruction. (See Figure II-4.)

Some microinstructions can occur during phase 1, while others can occur during phase 1 and phase 3 time intervals. Other microinstructions occur during a phase 1, extended phase 3, and phase 3 time interval. Phases of successive microinstructions always overlap one another, so that phase 1 of a current microinstruction can be executed simultaneously with phase 3 of a prior microinstruction. The overlapping of microinstruction phases allows for the start of the execution of a new microinstruction each time a new clock period starts. Therefore, it can be stated that one microinstruction can be executed in one clock time.

A microinstruction may contain either a constant (Type II microinstruction) or the address of a nanoinstruction (Type I microinstruction). For a Type II microinstruction, phase 1 provides sufficient time to execute the instruction (completion of the STEP successor and literal assignment) and therefore, require no additional phases. For a Type I microinstruction, the following information describes the events that occur in each of the three phases.

Phase 1: Condition testing and adjusting, and selection of the controls for the next instruction address computation (successor microprogram address control), initiation of memory and device operations, and the setup for Logic Unit operation (phase 3). (See Figure II-3.)

Extended Phase 3: Holding phase for Logic Unit operation phase 3 controls.

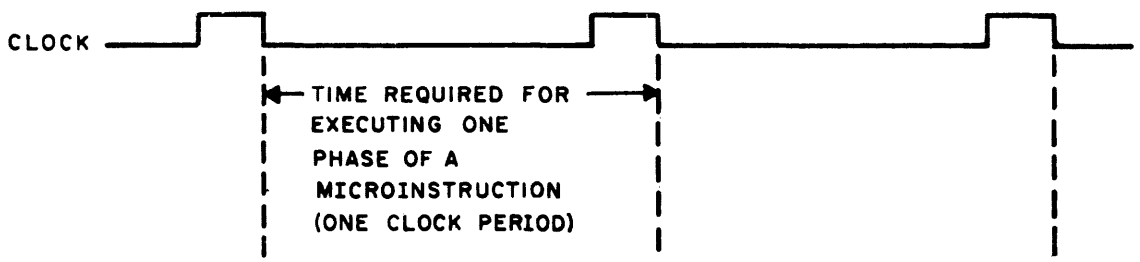


Fig. II-4. CLOCK PULSES AND PHASE RELATIONSHIP

Phase 3: Initiation and completion phase for performing Logic Unit operations and to change destination registers as specified in the logic operation. (See Figure II-3.)

All Type I microinstructions which do not contain a conditional logical operation always have a phase 1 and a phase 3. However, those Type I microinstructions which contain a conditional logical operation can be divided into two categories: those which meet the specified conditions, or those that do not meet the specified conditions. The Type I microinstructions that meet the conditions require a phase 1 and 3 for the execution of the operation to be completed. The Type I microinstructions that do not meet conditions require only a phase 1 for the complete execution of the operation. Phase 1 occurs at each clock time, and phase 3 completes the execution of a Logic Unit operation.

The controls for phase 3, which are contained in the Control Register of the Memory Control units (MU2 through MU5 cards) and the Shift Control Register of the CU2 card, are divided into two parts: the Logic Unit operations and the destination controls.

The Logic Unit operations are as follows:

a. X-selection to Adder.
b. Y-selection to Adder.
c. Inhibit carry between bytes.
d. Adder operation
e. Shift selection.

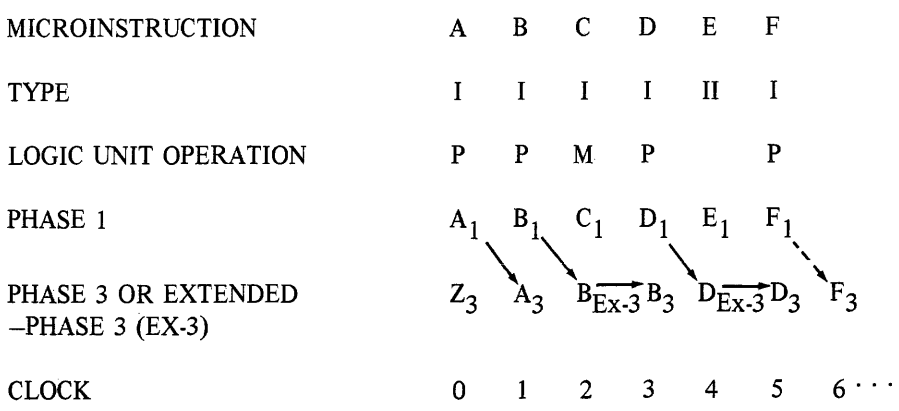
The destination controls are used to perform the following functions:

a. A-register input selection.
b. B-register input selection.
c. Memory Information Register (MIR) input selection.
d. Alternate Microprogram Count Register (AMPCR) input selection.
e. Base Register (BR1) input selection.
f. Base Register (BR2) input selection.
g. Memory Address Register (MAR) input selection.
h. Counter (CTR) input selection.
i. Shift Amount Register (SAR) input selection.
j. Shift Store Control (SCC).

See Figure II-3 for nanocode information pertinent to Logic Unit operations and destination controls.

The Logic Unit operation controls (phase 3 controls from decoded nanobits 17 through 33) are provided by the Control Register and are present from the beginning to the end of phase 3. The destination controls, which are executed at the end of phase 3, cause the contents of the destination registers to be changed. However, the destination registers are not changed until the occurrence of the clock pulse which signals the end of phase 3 and simultaneously reloads the Control Register from the execution of a new Logic Unit operation. The destination controls are decoded nanobits 34 through 50 and 55 from the Control Register on the MU and CU cards.

An extended phase 3 interval is the designation given to a phase 3 clock time whose Logic Unit operation is in the process of being performed, but whose destination register change is postponed for one or more clock periods. An explanation of the need for an extended phase 3 interval is presented in the following text and Figure II-5.



NOTE:
FOR A LOGIC UNIT OPERATION , A "P" INDICATES PRESENT AND AN "M" INDICATES MISSING.

Fig. II-5 TYPICAL EXAMPLE OF PHASED EXECUTION OF MICROINSTRUCTION

A B700 Processing system processes microinstructions in parallel; therefore, the processor always expects to process phase 1 of one microinstruction and phase 3 of another microinstruction, concurrently. To ensure the existence of a phase 3 interval which occurs concurrently with a phase 1 interval, the phase 3 interval in process is delayed until the occurrence of another phase 3 interval for a subsequent microinstruction.

The external operations (Memory/Device operations, nanobits 51 through 54) occur following phase 1 and are independent of any phase 3 instruction.

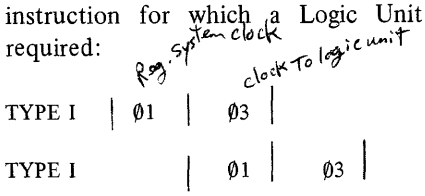
The phased execution of a sequence of microinstructions is presented in Figure II-5, in which each microinstruction is symbolically represented by letters A through F. The type of operation (Type I or II), the presence or absence of a Logic Unit operation, phase information, and clock intervals are also shown. A subscript indicates the particular phase; an ex-3 subscript indicates an extended phase 3 that was originally a phase 3. A "present" designation opposite Logic Unit operation indicates that the Type I instruction requires the execution of a phase 3 Logic Unit operation. A "missing" designation indicates that the Logic Unit operation was conditional and that the condition required for execution was not met.

The phase 3 or extended phase 3 (EX-3) in process is determined by the presence of a Logic Unit operation. As indicated in Figure II-5, the previous phase 3 (Z_3) is completed, and then the next clock initiates the new phase 3 (microinstructions A, B, D, and F) of a Logic Unit operation required for Type I microinstructions. A previous phase 3 is extended if a Logic Unit operation is not required, as indicated for microinstruction C. At this point, microinstruction C creates an extended phase 3 (B_{EX-3}) for the microinstruction at B. Microinstruction D, which is a Type I microinstruction with a Logic Unit operation present, completes the phase 3 for microinstruction B. Microinstruction E which is Type II creates an extended phase 3 (D_{EX-3}) for microinstruction D. The presence of Type II microinstruction E delays the D microinstruction input to the destination registers until the end of phase 1 at microinstruction F time (clock 6); thereby, forcing microinstruction D to use destination register values that occur after clock time 5. Microinstruction E indicates how a Type II microinstruction can affect the results of a previous Type I microinstruction.

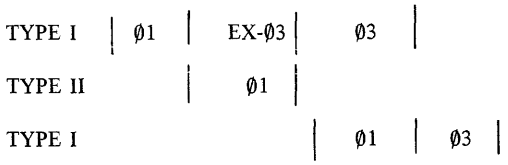
Microprogram timing is a critical consideration in the execution of microprogramming in a B700 Processing system. The following timing definitions are presented concerning phase information:

a. Phase 1 of a microinstruction is always executed in parallel with phase 3 or extended phase 3 of another microinstruction. (Refer to examples A and B in Figure II-6.)

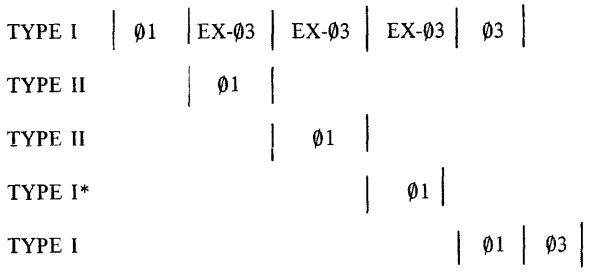
A. Type I Microinstruction followed by a Type I microinstruction for which a Logic Unit operation is required:



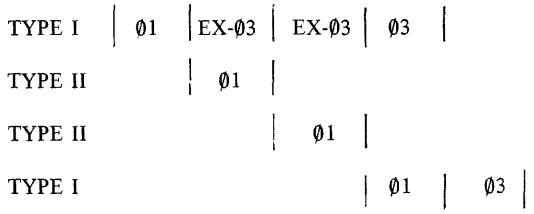
B. Type I microinstruction followed by a Type II microinstruction and a Type I microinstruction for which a Logic Unit operation is required:



C. Type I microinstruction followed by two Type II microinstructions and two Type I microinsructions:



D. Type I microinstruction followed by two Type II microinstruction and a Type I microinstruction for which a Logic Unit operation is required:



NOTE:
The asterisk (*) indicates that this Type I microinstruction consists of only phase 1.

Fig. II-6 PHASING OF TYPE I AND TYPE II MICROINSTRUCTIONS

b. An extended phase 3, which is otherwise known as a phase 3 inhibit or delayed phase 3, occurs due to succession by either a Type II or a Type I microinstruction that contains a conditional Logic Unit operation that has not been satisfied. (See example C of Figure II-6.)
c. An extended phase 3 of a Type I microinstruction, which consists of both phase 1 and phase 3, is not completed until the occurrence of another Type I microinstruction which consists of both phases. (See example D of Figure II-6.)
d. Any microinstruction which causes either an extended phase 3 to be initiated or prolongs an existing extended phase 3 is executed between phase 1 and phase 3 of the affected Type I microinstruction. (See example C of Figure II-6.)

Microprogram Instruction Sequencing

The sequence of logical events that occur in the execution of a microinstruction is presented in Figure II-7. The sequence of events (steps 1 through 11) are used in the following text to describe the logical events which occur in the execution of a microinstruction. The first group of steps (sequence of events) that occur are common to both Type I and Type II microinstructions as follows:

1. Development of the Microprogram Address (MPAD). The MPAD Control (MPAD CNTL) is set by the previous microinstruction and, at this time, the MPAD CNTL determines the selection of the Microprogram Count Register (MPCR) or the Alternate Microprogram Count Register (AMPCR).
2. Selection of the correct increment amount (+1 or +2).
3. The microinstruction is read from the Microprogram Memory (MPM).
4. A decode of the MPM word is performed to determine if it is a Type I or II microinstruction.

If the MPM word is a Type II microinstruction, the following sequence of events occur. At the same time that the Type II microinstruction occurs, the phase 3 portion of a previous Type I microinstruction is executed; however, this parallel phase 3 interval is not completed at the end of the clock period (one clock time). Therefore, the destination registers remain unchanged and the phase 3 interval is extended (EX-3) for an additional clock period for the previous Type I microinstruction. The following steps (sequence of events) apply for the Type II microinstruction as shown on Figure II-7:

5(a). The low order bits (LSB's) of the microinstruction are used as literal values.
11(a). A STEP successor is sent to the MPAD CNTL.
11(b). The literals are clocked to the specified registers (SAR, LIT, SAR and LIT, or AMPCR).

If the Microprogram word is a Type I microinstruction, the following sequence of events occur. (See Figure II-7 and refer to Table II-2.) At the same time that the Type I microinstruction occurs, the phase 3 of a previous Type I microinstruction is executed. However, the completion of this phase 3 portion of the previous Type I microinstruction is dependent upon the requirement of a new phase 3 during the execution of the phase 1 portion of the current Type I microinstruction. The following steps (sequence of events) apply for the Type I microinstruction as shown on Figure II-7.

5(b). The low order bits (LSB's) of the microinstruction are used to address the Nanomemory (NM).
6. The nanocode is read from the Nanomemory.
7. The resultant nanocode is decoded.
8. Selection of the condition to be tested (nanobits N1 through N4).
9. Determination of whether the selected true or complement (false) condition has been met (nanobit N5).
10.(a). Determination of whether a new Logic Unit operation (LUOP) is required by this microinstruction (nanobit N6). If the Logic Unit operation (LUOP) to be performed is unconditional or if the test condition was met (condition=true), a new Logic Unit operation (LUOP) is required to complete the phase 3 of the previous microinstruction.
10(b). Determination of whether an external operation (EXTOP) is required by this microinstruction (refer to nanobit N7). An external operation (EXTOP) is required if it is to be performed unconditionally or if the test condition is met (condition=true).
11(c). If an external operation (EXTOP) is to be performed, enable the condition adjust (CNDADJ, nanobits N8 through N10) and memory/device operations (MDOP, nanobits N51 through N54) unless their selection values are ZERO.
11(d). If a new Logic Unit operation (LUOP) is required, the destination portion of the current phase 3 is completed and the new phase 33 controls are decoded and loaded into the Control Register. (Refer to nonobits N17 through N50 and N55.)
11(e). The MPAD CNTL's are loaded with either a true or false successor depending upon which test condition was met; successor conditions=1 (true)or 0 (false). (Refer to nanobits N11 through N16.)
11(f) If applicable, the tested condition is reset.

The following information is applicable for a Type I microinstruction during a phase 3 or extended phase 3 interval. (See Figure II-7 and refer to Table II-2.)

While phase 1 of the current microinstruction is in process, the phase 3 of a previous microinstruction is executed. If a new phase 3 interval is not required at the end of the current phase 1, the phase 3 is extended (EX-3) during the next phase 1 interval until a new phase 3 is re-

quired. The sequence of events (steps) for a Type I microinstruction during a phase 3 or extended phase 3 interval are as follows:

1(a). Selection of X input to Adder. (Refer to nanobits N17 through N19.)

1(b). Selection of Y input to Adder. (Refer to nanobits N20 through N26.)

3(b). Inhibit carries between 8-bit bytes, if required. (Refer to nanobit N27.)

3(b). Select and perform Adder operation (ADOP). (Refer to nanobits N28 through N31.)

7. At this time, the dynamic conditions from the Adder are available for testing. (Refer to step 8 of the previous Type I, phase 1 microinstruction description.)

9. Selection of shift direction and performance of shift functions. (Refer to nanobits N32 and N33.)

11(g). The destination registers are changed at this time if the current phase 1 requires a new phase 3; otherwise, the phase 3 interval is extended (EX-3) and re-executed during the next phase 1 interval of a microinstruction. During the sequence of events, any or all of the following registers may be changed. (Refer to nanobits N34 through N50 and N55.)

a. A Registers.
b. B Register.
c. Memory Information Register (MIR).
d. Alternate Microprogram Count Register (AMPCR).
e. Base Register 1 (BR1).
f. Base Register 2 (BR2).
g. Memory Address Register (MAR).
h. Counter (CTR).
i. Shift Amount Register (SAR).
j. Sign Save Control (SSC).

Table II-2 indicates the Nanomemory decoding functions that occur during phase 1, at the end of phase 1, during phase 3, and at the end of phase 3.

Microprogramming

Microprogramming is a means of controlling the data and data flow in a sequential manner to perform a given function. Microprogramming is the format that the designer uses to specify the action, function, and the state of each of the B700 system logic elements at every clock cycle time. In this manner, microprogramming replaces the function of hardware sequential logic that is used in a system configuration to execute an instruction which requires more than one clock time. Therefore, it can be stated that microprogramming is essentially similar to sequential logic design.

The microprogram is written in the B700 Microprogram Language (B7MPL), which is the source language for a computer program designed to convert English language statements defining the action of the Processor for each clock cycle into binary patterns for the Microprogram Memory (MPM) and Nanomemory (NM). The B7MPL structure consists of a number of reserved words and operators that are used to specify the action of the Processor for each clock cycle. Refer to Table II-3 for the B7MPL reserved words and terminal characters used in the program listings.

A microinstruction or nanoinstruction is a statement that specifies the action of the processor for one clock cycle and requires one word in the Nanomemory (NM) as indicated by the following example:

CSAR, LMAR, A1=A1+B

The value of the Shift Amount Register (SAR) is complemented, the contents of the Literal Register (LIT) are placed in the Memory Address Register (MAR), and the contents of the A1 Register are added to the contents of the B Register and the result is stored in the A1 Register.

B7MPL provides the capability for conditional branching to a subroutine or other instruction strings with reserved words (Successor words) such as STEP, SKIP, CALL, EXEC, WAIT, SAVE, JUMP, and RETN. In the example previously described, there is no Successor word; thus the STEP instruction is implied. This implied STEP instruction causes the Processor to step to the next microinstruction in sequence in the Microprogram. The following is an example of a conditional instruction:

IF LC1 THEN A1=A1+B JUMP ELSE STEP.

If the Local Condition Bit 1 is true, the indicated operations that follow the THEN statement are performed and a JUMP is made to the instruction address that is currently in the Alternate Microprogram Count Register plus 1 (AMPCR+1). If the Local Condition Bit 1 is false, then the action indicated after the ELSE statement occurs; a STEP is made to the next instruction in sequence.

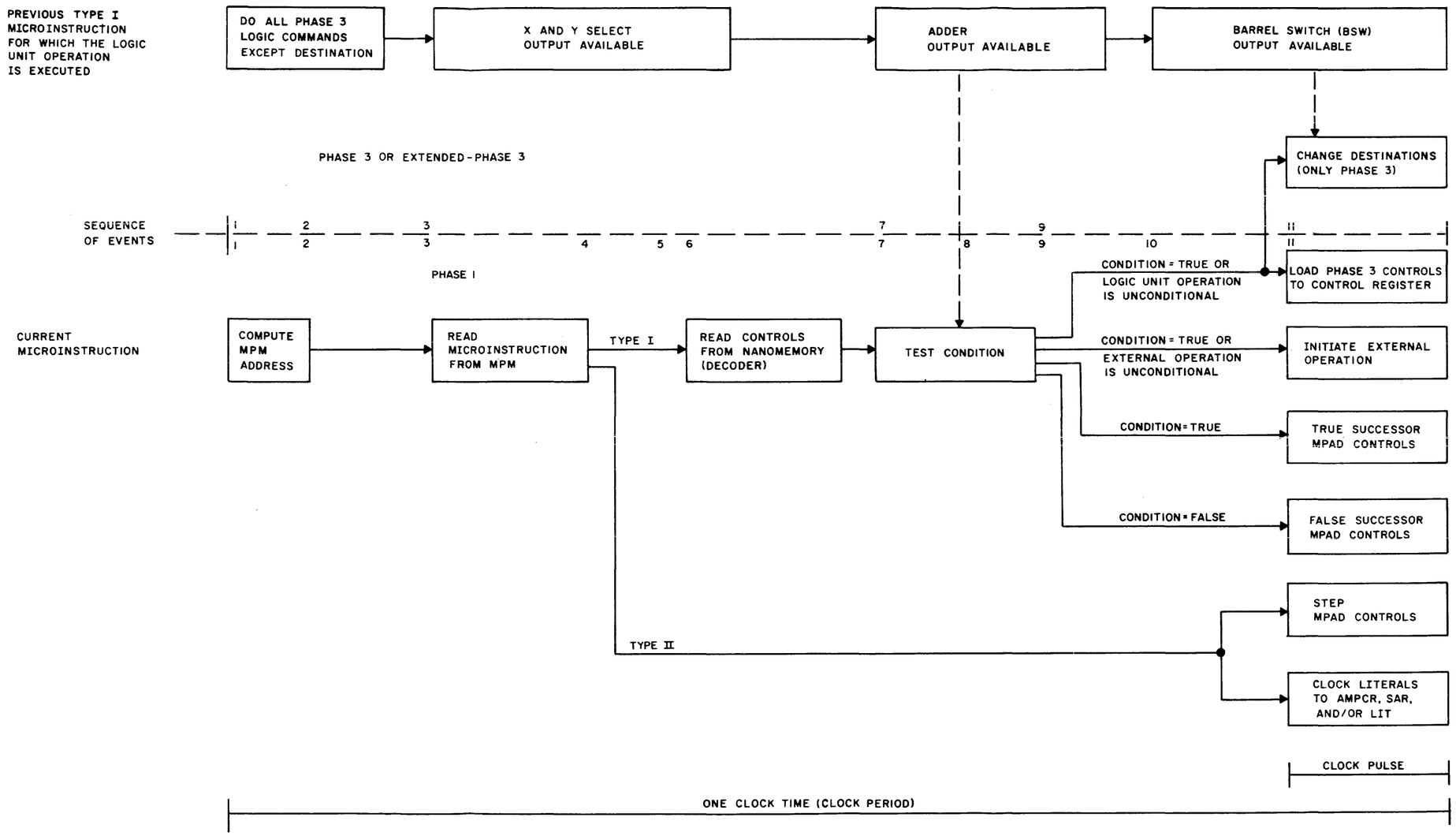


Fig. II-7. MICROINSTRUCTION SEQUENCING DIAGRAM

TABLE II-2 NANOMEMORY DECODING

Phase and Control Information	Nanomemory Bit No.	Function
DURING PHASE 1:		
Conditional Controls	1-4	Condition Selection (CONDSEL)
	5	Successor Condition (True/False)
	6	Logic Unit Condition (Phase 3 Modifier)
	7	Memory/Device/Condition Adjust Modifier (MDOP and CNDADJ Modifier)
AT END OF PHASE 1:		
Successor Determination	11-16	Microprogram Address Controls (MPAD CNTL)
External Operation	8-10	Condition Adjust (CNDADJ)
	51-54	Memory/Device Operation (DOP). Request signals for memory or peripheral device operations.
PHASE 3:		
Adder Operation Commands	17-19	X Selection to Adder
	20-26	Y Selection to Adder
	27	Inhibit Carry Between 8-Bit Bytes
	28-31	Adder or Logic Operation
	32 and 33	Shift Selection (right, left, circular determined by amount in SAR)
AT END OF PHASE 3:		
Destination Specifiers	34-36	A Registers (A1, A2, and A3) Input Selection from Barrel Switch (BSW)
	37-40	B Register Input Selection
	41	MIR Input Selection from BSW
	42	AMPCR Input Selection from BSW
	43	Base Register 1 (BR1) Input Selection from BSW
	44	Base Register 2 (BR2) Input Selection from BSW
	45 and 46	MAR Input Selection from BSW or LIT
	46-48	Counter (CTR) Input Selection from LIT, BSW, or Increment CTR
	49-50	SAR Input Selection from Complement SAR (CSAR) or BSW
	55	Sign Save Control (SSC)

TABLE II-3. B7MPL RESERVED WORDS AND OPERATORS

Reserved Word	Function
A1	A1 Register X Select to Adder or destination operator
A2	A2 Register X Select to Adder or destination operator
A3	A3 Register X Select to Adder or destination operator
AAD	ANDed add logic operator: X input plus (X input ANDed with Y input) = X+(XY)
ABT	Adder Bit true; Adder output all ONES
AMPCR	Alternate Microprogram Count Register Y-Select to Adder or destination operator from Barrel Switch.
AND	Logical operator AND: X AND Y = XY.
AOV	Adder overflow, dynamic condition of previous microinstruction which uses the Adder.
ASCII	Identifies a "ASCII" character string.
ASE	Forces concatenation of the BR2 register with MAR for subsequent BMAR.
ASR	Status request for highest priority unselected device; also forces concatenation of the BR1 register with MAR for subsequent BMAR.
B	B Register Y-Select to Adder or destination operator (to B Register from Barrel Switch).
BAD	Destination operator: To B register Input Selection from Adder.
BBA	Destination operator: To B Register Input Selection from Adder ORed with Barrel Switch output.
BBE	Destination operator: To B Register Input Selection from External data bus ORed with Barrel Switch output.
BB1	Destination operator: To B Register Input Selection from prior Memory Information Register (MIR) contents ORed with Barrel Switch output.
BC4	Destination operator: To B Register Input Selection from Adder "not 4-bit carry" (complement of 4-bit carry).
BC8	Destination operator: To B Register Input Selection from Adder "not 8-bit carry" (complement of 8-bit carry).
BEX	Destination operator: To B Register Input Selection from External data bus.
BMAR	Y Selection to Adder of the Base Register 1 (BR1) or Base Register 2 (BR2) concatenated with the Memory Address Register (MAR) output.
BMI	Destination operator: To B Register Input Selection from prior MIR contents.
BOUND	Ensures that a specified area will not cross over a specified SYNC boundary. exam BOUND (nn_1) MOD (nn_2) nn_1 = size in D-words of area placed in bounds. nn_2 = SYNC value of area. If condition is not satisfied, the address counter is increased to the next module level.
BR1	Base Register 1
BR2	Base Register 2.
C	Circular shift right the entire Adder output; operation takes place in the Barrel Switch.
CALL	Call a procedure: Use AMPCR+1 as address; exchange AMPCR+1 and MPCR.
CAMPCR	Synonomous with CPCR
COMP	Complement as appropriate for literal destination.
CONT or CONTINUE	Pseudo operator used in the segment statement which causes the next microaddress or nanoaddress assigned to be greater than the greatest address previously used in the program.
COV	Counter overflow condition.
CNST	Pseudo operator that is used to generate a microcode with a specified value.
CPCR	Call Program Counter (TYPE II); MPCR and INCR are replaced by Microcode +1; AMPCR is replaced by prior MPCR.

TABLE II-3. B7MPL RESERVED WORDS AND OPERATORS (Cont'd.)

CSAR	Complement Shift Amount Register (SAR).
CTR	Counter (CTR) Register.
DATE	Constants containing Julian date.
DEFINE	Used for local DEFINE statements.
DEFINITIONS	A reserved label used to identify a group of parameter definitions.
DLD	Device Load: Used in special system configurations that use an LIC or configuration card.
DR1	Device Read 1: Read from device specified by Base Register 1 (BR1).
DR2	Device Read 2: Read from device specified by Base Register 2 (BR2).
DW1	Device Write 1: Write to device specified by Base Register 1 (BR1).
DW2	Device Write 2; Write to device specified in Base Register 2 (BR2).
EBCDIC	Identifies a "EBCDIC" character string.
ELSE	Sequential operator.
EQV	Equivalence logical operator: X EQV Y.
EXEC	Executes out of sequence: Use AMPCR+1 ad address.
EXT	External condition bit: set externally and reset by testing (real-time clock).
FINISH	Reserved label, which terminates the source input dect.
GC1	Global Condition Bit 1: A set condition causes this bit to be set. Testing this condition bit does not cause resetting of the condition bit.
GC2	Global Condition Bit 2: Refer to explanation for GC1.
IC	Inhibit carries.
IF	Sequential operator which starts the conditional part of an instruction.
IMP	Logical operator Imply: X IMP Y.
INC	Increment Counter; set Counter Overflow (COV) if overflow.
IOL	Initiate memory overlay.
IRQ	Interrupt from locked but unselected device. This interrupt can be either a status or data interrupt.
JUMP	Jump to address in Alternate Microprogram Count Register (AMPCR+1); then, place that address in the Microprogram Count Register (MPCR).
L	Left shift end-off the entire Adder output, right fill with ZEROS. This operation takes place in the Barrel Switch (BSW).
LC1	Local Condition Bit 1: Can be set or tested (reset by test).
LC2	Local Condition Bit 2: Can be set or tested (reset by test).
LC3	Local Condition Bit 3: Can be set or tested (reset by test).
LCTR	One's complement of the Literal Register contents will be placed in the Counter (CTR) and Counter Overflow (COV) will be reset.
LIT	Literal Register: set with a literal and can be an input to the Adder, the Memory Address Register (MAR), or the Counter (CTR).
LMAR	Literal Register contents will be placed in the Memory Address Register (MAR).
LOCN	Pseudo operator used to advance microprogram instruction address to the specified address, or to previously declared label, plus or minus literal offset.
LST	Least significant bit of the Adder output; dynamic condition of the previous microinstruction which uses the Adder.
LUOP	Pseudo operator used to generate a default Logic Unit operation.
MAR	Memory Address Register.

TABLE II-3. B7MPL RESERVED WORDS AND OPERATORS (Cont'd.)

MAR1	Combination parameter specifying Base Register (BR1) and Memory Address Register (MAR).
MAR2	Combination parameter specifying Base Register (BR2) and Memory Address Register (MAR).
MICRO	Pseudo operator that identifies a control parameter that is used to set the micro-address when segmenting.
MIR	Memory Information Register.
MPCR	Mark Program Counter (TYPE II); MPCR and INCR are replaced by Microcode +1; AMPCR remains unchanged.
MR1	Memory Read 1: Read the contents from the memory address specified by Base Register (BR1) and Memory Address Register (MAR).
MR2	Memory Read 2: Read the contents from the memory address specified by Base Register (BR2) and Memory Address Register (MAR).
MST	Most significant bit of the Adder output; dynamic condition from previous micro-instruction specifying an Adder operation.
MW1	Memory Write 1: Write the contents of the Memory Information Register (MIR) into the memory address specified by Base Register (BR1) and the Memory Address Register (MAR).
MW2	Memory Write 2: Write the contents of the Memory Information Register (MIR) into the memory address specified by Base Register (BR2) and the Memory Address Register (MAR).
NAN	Logical operator Not AND: X NAN Y.
NIM	Logical operator Not Imply: X NIM Y.
NOR	Logical operator NOR: X NOR Y.
NOT	Complement monadic or condition operator: NOT X
NR1	Logical operator Not Reserve Imply: X NRI Y.
OAD	Logical operator ORed ADD: X input plus (X input ORed with Y input).
OR	Logical operator OR: X OR Y.
PROGRAM-ID	Bracket word which begins a program.
R	Right shift end-off of the entire Adder output, left fill with ZEROS.
RDC	Read Complete bit: set when external data from External Bus is ready for input to the B Register via the B Input Select gates. This bit is reset by testing.
RELATIVE	Used with SEGMENT.
RENAMES	Pseudo operator used to indicate definition type.
RESET	Reset the specified Condition Bit.
RESV	Pseudo operator that is used to reserve a specified number of data area words or microprogram words.
RETN	Return: use AMPCR+2 as address and as new content of the Microprogram Count Register (MPCR).
RIM	Logical operator Reverse Imply: X RIM Y.
RLOC	Reset location counter to last location previously stored in stack by LOCN.

TABLE II-3. B7MPL RESERVED WORDS AND OPERATORS (Cont'd.)

RMI	Ready MIR bit: set externally when data has been accepted from the Memory Information Register (MIR). This bit is reset by testing.
SAR	Shift Amount Register.
SAVE	Save the MPCR in the AMPCR: use MPCR+2 as the Microprogram address and as the next MPCR.
SEGMENT	Pseudo used to control program segmentation by the assembler.
SET	Set the Condition Bit specified: either LC1, LC2, INT, GC1, or GC2.
SIZE	Size of specified SEGMENT is stored in MPCR, AMPCR, CPCR, or CNST.
SKIP	Skip the next microinstruction: use MPCR+2 as the Microprogram address and as the next MPCR.
SRQ	Solicited Request bit: set externally and reset by testing.
SSC	Shift Store Control: store the first shift-off bit and load the opposite bit or store the Adder Overflow (AOV) condition.
START	Reserved label which indicates the beginning of the microstatements.
STEP	Step to next microinstruction: use MPCR+1 as Microprogram address and as next MPCR.
SYNC	Pseudo operator which causes the microprogram address to be advanced to the next multiple of the specified value.
THEN	Sequential operator for true alternative of a conditional instruction.
URQ	Unsolicited Request bit: set externally and reset by testing.
USEL	Place all devices in unselected mode.
VALUE IS	Pseudo operator used to indicate definition type.
WAIT	Wait Condition bit: Microprogram address is in the MPCR. The MPCR and AMPCR remain unchanged.
WHEN	Same as IF, except that a false-successor of WAIT is produced.
XOR	Logical Operator Exclusive OR: X XOR Y.
Z	Counter (CTR) output in 8 MSB's and Literal register (LIT) outputs in 8 LSB's used as input to the Adder via X-Select and Y-Select gates. In system configurations with word lengths larger than 16 bits, ZOPT inputs from an external source are used for the center bits.
ZERO	Hexadecimal value @0000@ is placed in number of memory locations specified by literal value.
+	Arithmetic Operator Add: X + Y.
-	Arithmetic Operator Subtract: X - Y.
=	Assignment or set operator.
@	Indicates hexadecimal value.

LOGIC UNIT (LU1 THROUGH LU5)

The Logic Unit (LU1 through LU5 card assemblies) is one of the major functional units of the processor. The Logic Unit is used to perform all of the arithmetic, Boolean logic, and shifting operations in the B700 Processing system. The Logic Unit consists of the following functional circuits:

a. A Register (A1, A2, and A3).
b. X-Select Gates.
c. B Register and Associated Input Selection Gates.
d. Y-Select Gates.
e. Arithmetic/Logic Unit (ALU or Adder) and Group Carry Gates.
f. Barrel Switch (BSW) and Associated Control Circuits.
g. Memory Information Register (MIR).

See Figure II-1 for the functional circuits of the Logic Unit and their interconnection with the other functional units of the Processing system. Figure II-8 is a functional block diagram of the Arithmetic/Logic Unit (Adder) and associated input circuits.

The Logic Unit provides for a system word length of 16-bits. Each Logic Unit card assembly (LU2 through LU4) is designed for a four-bit configuration; therefore, a 16-bit system configuration requires four LU2, two LU3, and two LU4 card assemblies. The following registers within the Logic Unit contain 16-bits in four-bit increments: the A registers (A1, A2, and A3), the B register, and the memory information register (MIR).

A Registers (A1, A2, and A3)

The three A registers are functionally identical and are used for temporary data storage within the Processing system and serve as a primary input to the Arithmetic/Logic Unit (Adder).

Any or all of the A registers may be loaded with the Barrel Switch (BSW) output during one operation. The presence of nanobit control pulse (NB34) from the Control Register of the Memory Control Units (MU3 card) enables the clock pulse to the A1 register. Nanobit control pulse (NB35) enables the clock pulse to the A2 register and NB36 enables the clock pulse to register A3. The phase 3 clock signal (3CLKB*C) from the clock generator circuits of the CG card is used as the clock pulse to the A registers.

The nanobit control signals (NB34, NB35, and NB36) correspond to the nanobits (N34, N35, and N36) from the Nanomemory. These nanobits are used to determine A register input selection. (See nanobits 34 through 36 on Figure II-3.) If nanobit N34 is at a 0 level, the A1 register is unchanged. If N34 is at a 1 level, the Barrel Switch (BSW) output is sent to register A1. Likewise, if nanobit N35 or N36 is at a 0 level, the respective A register (A2 or A3) remains unchanged.

If either of these nanobits is at a 1 level, the appropriate BSW output is sent to the respective A register (A2 or A3).

The outputs of these three A registers are sent to the X-select gates, which select the appropriate input (A1, A2, A3, Z, LIT, CTR, or ZEROS) to the Arithmetic/Logic Unit (Adder).

X-Select Gates

The X-select gates are used to select the X input to the Arithmetic/Logic Unit (ALU or Adder). The X selection to the Adder consists of the following inputs: ZERO, LIT, CTR, Z(CTR/LIT), A1, A2, or A3.

Three signals (NQE1, NQE2, and NQE3) from the Control Register in the Memory Control Units (MU2 card) are used as enable signals for the X-select gates. These three enable signals are used to inhibit unwanted bits during a Literal register (LIT) and Counter (CTR) transfers through the X-select gates. If all three enable signals are false (NQE1, NQE2, and NQE3), a ZERO output is generated from the X-select gates. The NQE1 enable signal is used for the most significant byte (8-bits) during Counter (CTR) transfer through the X-select gates. Only enable signals NQE1 and NQE3 are used in a 16-bit system configuration to transfer Counter (CTR) and Literal register (LIT) inputs through the X-Select gates. The NQE3 enable signal is used for the least significant byte (8-bits) during Literal register (LIT) input transfer through the X-select gates.

Two additonal control signals (ACTL1 and ACTL2) from the Control Register of the Memory Control Circuits (MU2 card) are used as controls for the selection of the A Register and Z inputs in the X-select gates. The following list indicates the levels for the ACTL signals and the functions specified:

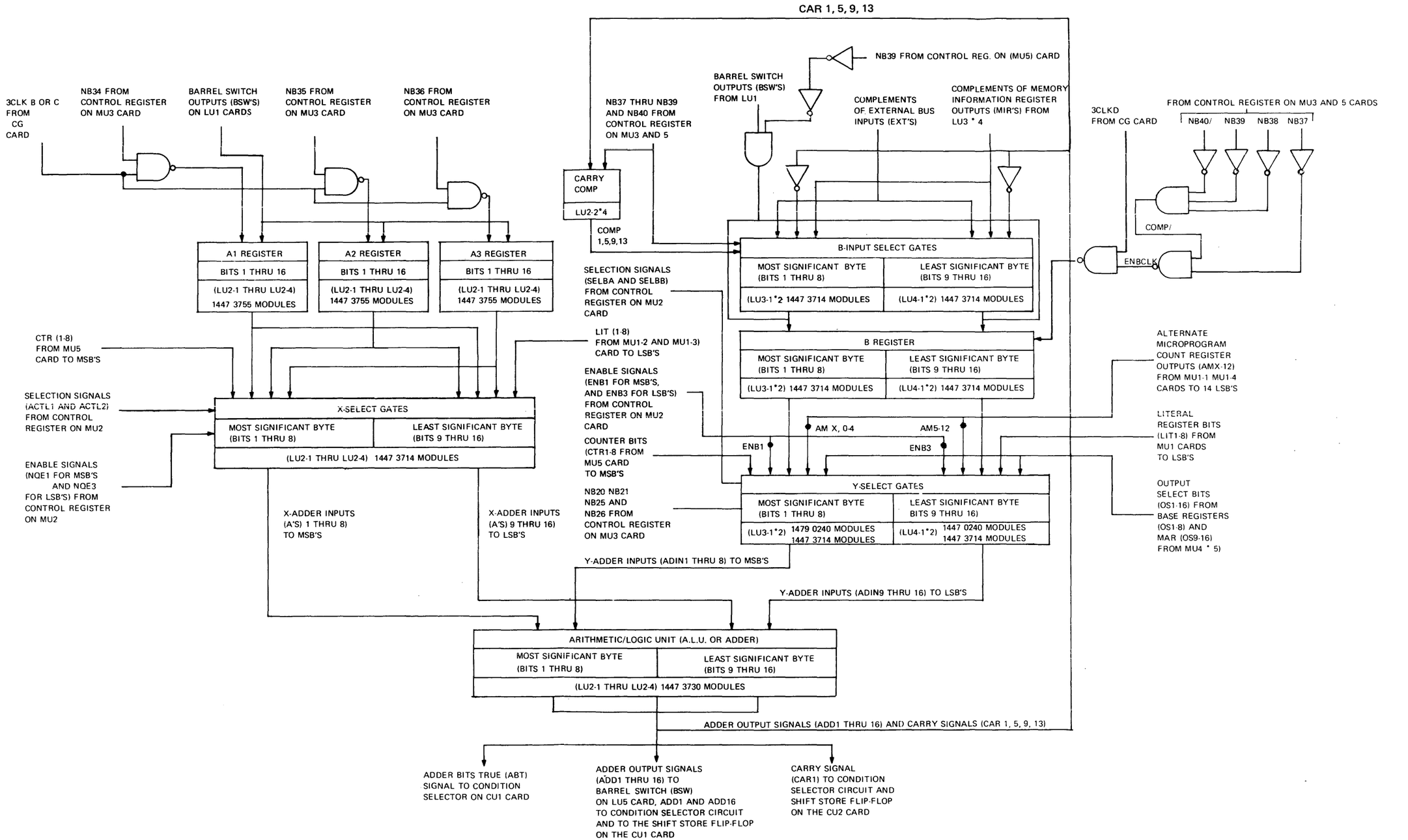


Fig. II-8. ARITHMETIC/LOGIC UNIT (ADDER) AND ASSOCIATED INPUT CIRCUITS, FUNCTIONAL BLOCK DIAGRAM

ACTL1	ACTL2	Function Specified
0	0	Selection of A3 Register.
0	1	Selection of A2 Register.
1	0	Selection of A1 Register.
1	1	Selection of Z inputs (CTR/LIT).

Nanobits N17 through N19 from the Nanomemory are sent to the Control Register input gates on the MU2 card to generate the aforementioned enable and control signals (NQE and ACTL signals). These nanobit signals (N17 through N19) are used to determine X Selection to the Adder (refer to nanobits 17 through 19 on Figure II-3). The following list indicates the nanobit codes for X-selection to the Arithmetic/Logic Unit (ALU or Adder):

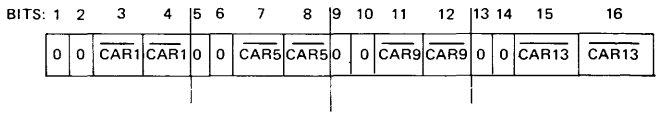
Nanobits 17	18	19	X-Selection To Adder
0	0	0	ZERO
0	0	1	Literal Register (LIT) to most significant byte
0	1	1	Counter (CTR) to least significant byte
1	0	0	Z inputs (CTR/LIT)
1	0	1	A1 Register
1	1	0	A2 Register
1	1	1	A3 Register

The output signals from the X-select gates are sent to the Arithmetic/Logic Unit (ALU or Adder).

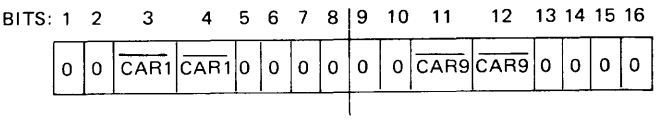
B Register and Associated Input Selection Gates

The B register and associated input selection gates are the primary interface between the main memory and the Device Dependent Ports (DDP's). The B register serves as the secondary input to the Arithmetic/Logic Unit (Adder) and can store certain arithmetic operation functions, such as complements of carries (BC4 and BC8). Figure II-9 shows the gating of the complement of group carries. The B register can be loaded via the B input selection gates with any of the following inputs during one operation (one instruction):

a. Barrel Switch outputs (BSWnn signals).
b. Adder output (ADDnn signals).
c. External bus (EXTnn signals) for processor status information, from Data/Program Memory, from the Device Dependent Ports (DDP's), or for system configuration data.
d. The complements of the carries of the four-bit Adder groups (CAR1, 5, 9, and 13 signals) are placed in the two least-significant bits (LSB's) of the corresponding four-bit B register groups, with ZERO's in the remaining bits. The following example is for a four-bit B register groups (BC4):



e. The complements of the carries of the eight-bit Adder groups (CAR01, 09 signals) are placed in the third and fourth bits of each 8-bit group (byte), with ZERO's in the remaining bits. The following example is for an eight-bit B register groups (BC8):



f. Barrel Switch outputs (BSW1-16 signals) ORed with Adder outputs (ADD1-16 signals).
g. Barrel Switch outputs ORed with data from the External Bus (EXT1-16 signals).
h. Contents of the Memory Information Register (MIR1-16 signals).
i. Barrel Switch outputs ORed with the contents of the Memory Information Register (MIR1-16 signals).

Nanobit control signals NB37, NB38, NB39, and NB40 that are not from the Control Register of the Memory Control Unit (MU3 and 5 card) and which correspond to nanobits N37 through N40 of the Nanomemory, are used to control B register input selection. (Refer to nanobits N37 through N40 on Figure II-3.) If nanobits N37 through N40 are at a 0 level, there is no change in the B register. The presence of a 0001 in nanobits N37 through N40 indicates the input source selection of the complement of four-bit carries (BC4) from the Adder to the B register. A 1000 in nanobits N37 through N40 indicates the input source selection of the Adder output (BAD) to the B register. The following list indicates the remaining nanobit codes for B register input source selection:

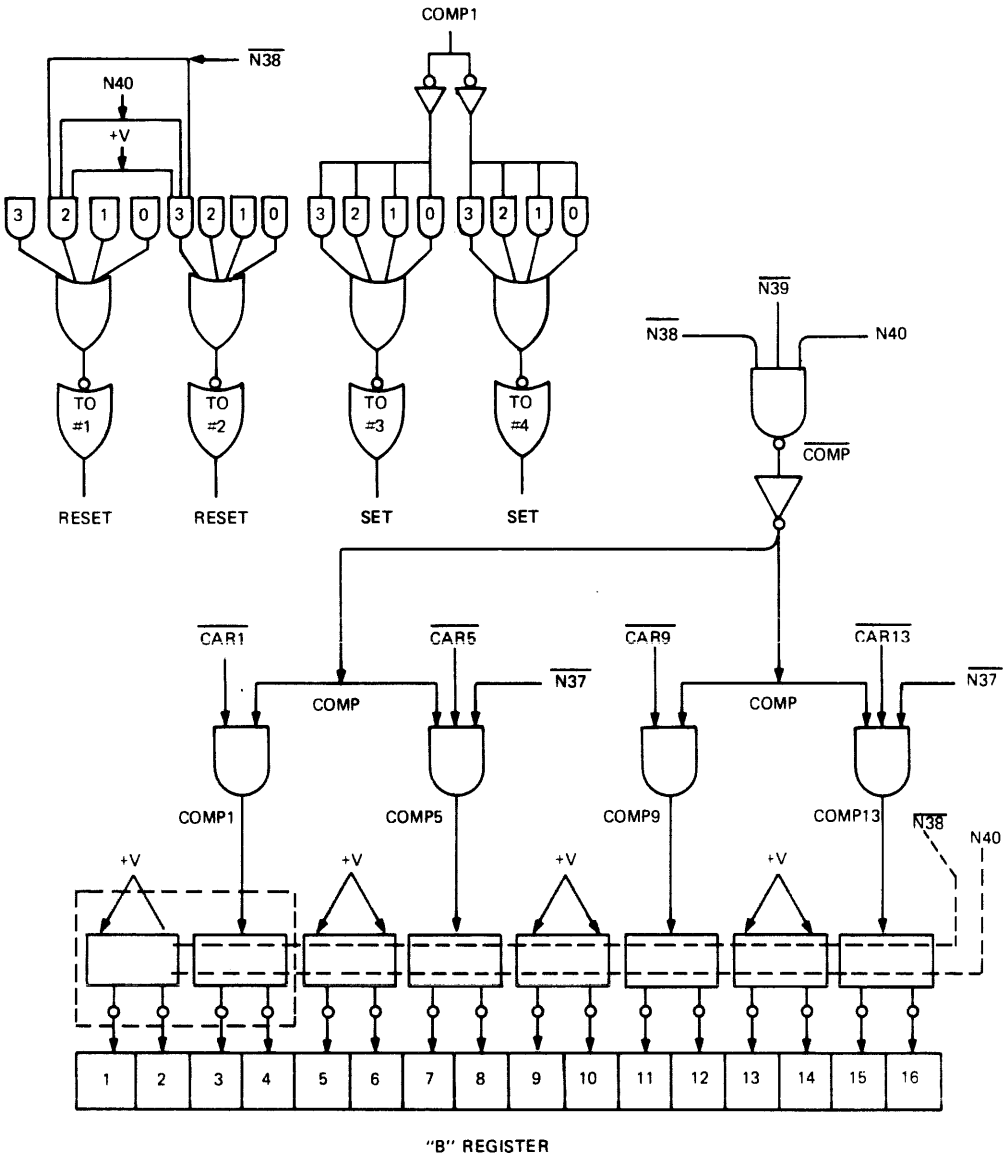
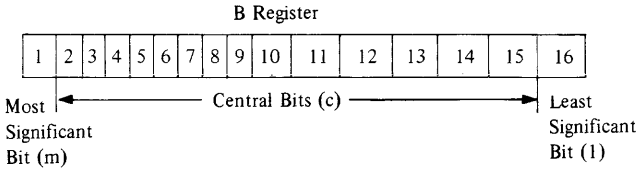


Fig. II-9. GATING OF THE COMPLEMENT OF GROUP CARRIES

Nanobits 37	38	39	40	B Register Input Source	Reserved Word
1	0	0	1	Complement of 8-bit carries from Adder	BC8
1	0	1	0	Barrel Switch outputs ORed with Adder outputs	BBA
1	0	1	1	Barrel Switch (BSW) outputs	B
1	1	0	0	External inputs from External Bus	BEX
1	1	0	1	Contents of the Memory Information Register (MIR)	BMI
1	1	1	0	Barrel Switch outputs ORed with data from the External Bus	BBE
1	1	1	1	Barrel Switch outputs ORed with the data from the Memory Information Register (MIR)	BBI

The B register is 16-bits in length. The word length, minus 2, determines the number of central bits contained in the B register. The number of central bits is 14. The following example presents the 16-bit word, which contains 14 central bits:



In this example, the B register can be represented by B or Bmcl, where B denotes the B register, m denotes the most significant bit (MSB), c denotes the central bits, and the l denotes the least significant bit (LSB).

The output of the B register is sent to true/complement selection gates (Y-select gates) which are divided into three sections: the most significant bit (m), the least significant bit (l) and the remaining central bits (c). Each of these three sections is controlled independently and may contain either 0's, 1's the true contents (T) or the complement (ONE's complement) of the contents (F) of the respective bits in the B register. Although there are no programmatic restrictions on the m, c, and l specifiers, the central bits (c) configuration is restricted, by the hardware, to a 0 or T function. Due to this hardware limitation when a Bxlx or a BxFx are specified, their complements are used (Bx0x or BxTx). The following example specifies the conditions that are represented by the following Bmcl specifiers for a 16-bit system configuration:

Bmcl Specifier (MOST / CENTER / LEAST)		Condition
B 0 – –		ZERO in Bit 1 (MSB) to ALU Y input
B T – –		True value of B reg Bit 1 (MSB) to ALU Y input
B F – –		Complement value of B reg Bit 1 (MSB) to ALU Y input
B 1 – –		ONE in bit 1 (MSB) to ALU Y input
B – 0 –		ZERO's in bits (2 through 15) to ALU Y input
B – T –		True value of B reg bits (2 through 15) to ALU Y input
B – F –	*	Complement value of B reg bits (2 through 15) to ALU Y input
B – 1 –	*	ONE's in bits (2 through 15) to ALU Y input
B – – 0		ZERO in bit 16 (LSB) to ALU Y input
B – – T		True value of B reg bit 16 (LSB) to ALU Y input
B – – F		Complement value of B reg bit 16 (LSB) to ALU Y input
B – – 1		ONE in bit 16 (LSB) to ALU Y input

NOTE: – indicates insignificant bit.
* requires complement Y input operation.

The actual contents of the B register or a modified configuration of its contents are sent to the Y-Select gates. As stated previously, the B register can be represented as B or Bmcl. The use of B alone implies that the actual contents of the B register, as a unit, are sent to the Y-Select gates. The use of Bmcl enables a reconfiguration of the contents of the B register to be sent to the Y-Select gates, without affecting the actual contents of the B register.

Y-Select Gates

The Y-select gates are used to select the Y input to the Arithmetic/Logic Unit (ALU or Adder). The Y selection to the Adder consists of the following inputs: ZERO, B, LIT, CTR, Z(CTR/LIT), AMPCR, or BMAR.

Two enable signals (ENB1 and ENB3) from the Control Register in the Memory Control unit (MU2 card) are two out of eight control signals used by the Y-select gates. These two enable signals are used to inhibit unwanted bits during Literal register (LIT), or Counter (CTR) transfers through the Y-Select gates. If both enable signals are true (ENB1 and ENB3), a ZERO output is generated from the Y-Select gates bits 2 through 15. The ENB1 enable signal is used for the most significant byte (8-bits) transfer of Counter (CTR) inputs through the Y-Select gates. The ENB3 enable signal is used for the least significant byte (8-bits) transfer of Literal register (LIT) inputs through the Y-Select gates.

Two more control signals (SELBA and SELBB) from the Control Register on the MU2 card are used as controls for the selection of the following inputs to the Y-Select gates: B register, Alternate Microprogram Count Register (AMPCR). Base Register 1 or Base Register 2 with Memory Address Register (MAR), or Z inputs (CTR/LIT). The following list indicates the levels for the SELB selection control signals and the function specified at these levels:

SELBA	SELBB	Function Specified
0	0	Selection of B register (bit 1 through 16)
1	0	Selection of CTR for MS byte and LIT for LS byte
0	1	Selection of AMPCR (bits X, 0 through 12) for 14 least significant bits.
1	1	Selection of BR1 or BR2 and MAR (OS bits 1 through 16)

The remaining four control signals used by the Y-Select gates are nanobit control signals NB20, NB21, NB25, and NB26 from the Control Register of the Memory Control units (MU3 card). Nanobit control signal NB20 corresponds to nanobit N20 from the Nanomemory. This

signal, along with NB21, controls the most significant bit (MSB) of the Y-Select gates. Nanobit control signal NB20 is connected to ground on all LU3 and LU4 cards (Y-Select gates) except for the LU3-1 card that contains the most significant bit (Y-MSB Select gate).

Nanobit control signal NB21 corresponds to nanobit N21 from the Nanomemory. This signal, along with NB20, controls the most significant bit (MSB) of the Y-Select gates. The nanobit control signal NB21 input is connected to ground or ENB3 on all LU3 and LU4 cards (Y-Select gates) except for the LU3-1 card that contains the most significant bit (Y-MSB Select gate).

Nanobit control signal NB25 corresponds to nanobit N25 from the Nanomemory. This signal, along with NB26, controls the least significant bit (LSB) of the Y-Select gates. Nanobit control signal NB25 is connected to ground on all LU3 and LU4 cards (Y-Select gates, except for the LU4-2 card that contains the least significant bit (Y-LSB Select gate).

Nanobit control signal NB26 corresponds to nanobit N26 from the Nanomemory. This signal, along with NB25, controls the least significant bit (LSB) of the Y-Select gates. The nanobit control signal NB26 input is connected to ground an ENB1 on all LU3 and LU4 cards (Y-Select gates), except for the LU4-2 card that contains the least significant bit (Y-LSB Select gate).

Nonobits N20 through N26 from the Nanomemory are sent to the Control Register input circuits on the MU2 and MU3 cards to generate the aforementioned enable and selection control signals (ENB1 and ENB3, SELBA and SELBB, NB20, NB21, NB25, and NB26). Nanobit signals N20, N21, N25, and N26 are direct inputs to the Control Register flip-flop on the MU3 card that generate the respective nanobit control signals (NB20, NB21, NB25, and NB26). Nanobit signals N22, N23, and N24 are sent to the Control Register input gates on the MU2 card that are used in the generation of enable signals (ENB1 through ENB3) and selection control signals (SELBA and SELBB). These nanobit signals (N20 through N26) are used to determine Y-Selection to the Adder. (Refer to nanobits N20 through N26 on Figure II-3.) The list below indicates the nanobits codes for Y-selection to the Arithmetic/Logic Unit (ALU or ADDER).

The output signals from the Y-Select gates (ADIN01 through 16 signals) are sent to the Arithmetic/Logic Unit (ALU or Adder).

Arithmetic/Logic Unit (ALU or Adder)

The Arithmetic/Logic Unit (ALU or Adder) is the unit which performs all of the arithmetic and Boolean operations allowed in the Processing system configuration. The inputs to the Arithmetic/Logic Unit can be comprised

Nanobits							
20	21	22	23	24	25	26	Y-Selection to Adder
0	0						ZERO (0) to the most significant bit (MSB) of Adder.
0	1						B register MSB to MSB of Adder.
1	0						Complement of B register LSB to the LSB of the Adder.
1	1						ZERO to Adder.
		0	0	0			ZERO to Adder.
0	0	0	0	1	0	1	Literal Register (LIT) to least significant byte (8-bits) of Adder.
0	1	0	1	1	0	0	Counter (CTR) to most significant byte (8-bits) of Adder.
		1	0	0			B register input to Adder.
0	1	1	0	1	0	1	Z inputs (CTR/LIT) to Adder.
0	0	1	1	0	0	1	Alternate Microprogram Count Register (AMPCR) to 14 LSB's of Adder.
0	1	1	1	1	0	1	Base Register 1 or Base Register 2 and Memory Address Register (MAR) to 16 LSB's of Adder.
					0	0	ZERO (0) to least significant bit (LSB) of Adder.
					0	1	B register LSB to LSB of Adder.
					1	0	Complement of B register LSB to LSB of Adder.
					1	1	ONE (1) to the least significant bit (LSB) of Adder.

of various combinations of the following:

a. A Register (A1, A2, or A3)
b. B Register.
c. Z inputs (CTR/LIT).
d. Alernate Microprogram Count Register (AMPCR).
e. Base Register 1 or Base Register 2 and Memory Address Register (MAR).
f. Literal Register (LIT).
g. Counter (CTR).

The microinstruction of the program specifies two of the various operands upon which the Arithmetic/Logic Unit (ALU or Adder) is to function. Each of the two specified operands (registers) are gated into two gate circuits: X-Select gates and Y-Select gates.

The X-Select gates provide the following inputs to the ALU as the "A" input signals: A1 Register, A2 Register, A3 Register, Z inputs (CTR/LIT). Counter (CTR) to most significant byte (8-bits), and Literal Register (LIT) for least significant byte (8-bits). The X-Select gates function only as a register selector.

The Y-Select gates provide the following inputs to the ALU as ADIN1 through 16 signals: B register, Z inputs (CTR/LIT), Counter (CTR) to the most significant byte (8-bits) of the ALU, Literal Register (LIT) to the least significant byte (8-bits) of the ALU, Alternate Microprogram Count Register (AMPCR) to the 14 least significant bits of the ALU, and Base Register 1 or Base Register 2 along with Memory Address Register (MAR) to all 16-bits of the ALU. The Y-Select gates permit the masking of the B register to the ALU without affecting the original values contained in the B register. The Y-Select gates also function as a register selector.

The four Adder Selection control signals (AS0 through AS3) are generated by the Control Register of the Memory Control Units (MU3 card). These Adder selection control signals are used in conjunction with the AMODE signal to select the proper arithmetic or logic operation of the Arithmetic/Logic Unit MSI module. The AMODE (Adder mode) signal is generated by the Control Register of the Memory Control Units (MU3 card). When the AMODE signal is true, this indicates that an arithmetic operation is to be performed by the Arithmetic/Logic Unit. When the AMODE signal is false, a logical operation is to be performed by the Arithmetic/Logic Unit. The following list indicates the levels of the AMODE and AS0 through AS3 signals and the selected operation to be performed by the Arithmetic/Logic Unit:

NOTE

In the following list, a + symbol represents a plus (add function), a – symbol represents a minus (subtract function), a v symbol represents an OR function, a v symbol represents an exclusive-OR function, and a · symbol represents an AND function.

AMODE	AS3	AS2	AS1	AS0	Specified Operation	Reserved Word
1	1	0	0	1	X+Y	+ (add)
0	0	0	0	1	$\overline{X \vee Y}$	NOR
0	0	0	1	0	$\overline{X} \cdot Y$	NIR
1	1	0	0	1	X+Y+1	+ +1 (add +1)
0	0	1	0	0	$\overline{X \cdot Y}$	NAN
1	1	1	0	1	(XvY)+X	OAD
0	0	1	1	0	C v Y	XOR
0	0	1	1	1	$X \cdot \overline{Y}$	NIM
0	1	0	0	0	$\overline{X} \vee Y$	IMP
0	1	0	0	1	$\overline{X \textcircled{v} Y}$	EQV
1	1	0	0	0	X+(X·Y)	AAD
0	1	0	1	1	X·Y	AND
1	0	1	1	0	X–Y–1	– –1 (subtract –1)
0	1	1	0	1	XvY	RIM
0	1	1	1	0	XvY	OR
1	0	1	1	0	X–Y	– (subtract)

Nanobits N27 through N31 from the Nanomemory are sent to the Control Register flip-flops of the Memory Control Units (MU3 card). The outputs from these Control Register flip-flops (NB27 through NB31) are sent to the various Control Register output gates, which are used to generate the following control signals: AMODE, AS0 through AS3, CIN, and INH8. These control signals are used by the Arithmetic/ Logic Unit to perform various arithmetic and logic functions.

The Adder Mode (AMODE) and Adder Selection control signals (AS0 through AS3) are the same as those described in the previous text. The Carry Input (CIN) signal is sent to the least-significant bit (LSB) of the Arithmetic/Logic Unit on the LU2-4 card. The Carry Input signal is used for the following arithmetic operations: X+Y+1 and X–Y. The Inhibit 8-bit carry signal (INH8/) from the output gate of Control Register flip-flop NB27 corresponds to nanobit N27 from the Nanomemory. When the Inhibit 8-bit NOT carry signal is false, it inhibits the carryout of the eight-bit groups of the Adder (Arithmetic/Logic Unit). This signal is gated with the Carry (CAR09) from least Byte, which is generated on the LU2-3 card, and is sent to the LU2-2 card which contains the least bit of eight most significant bits (eight MSB's) of the Adder. Nanobit signal N27 is used to determine whether a carry between eight-bit bytes is allowed or inhibited. (Refer to nanobit N27 on Figure II-3.) The nanobit code for the inhibiting of carries between eight-bit bytes is as follows:

Nanobit 27	Function Specified
0	Allow carry between 8-bit bytes.
1	Inhibit carry between 8-bit bytes.

Nanobit signals N28 through N31 are used to determine Arithmetic/Logic Unit operation. Reference should be made to the previous list describing Adder Selection control signals (AS0 through AS3). Adder Mode signal (AMODE), and the operation specified by the designated logic levels for those control signals. Because nanobits N28 through N31 are used to generate the aforementioned signals, the following list should also be used in determining Arithmetic/Logic Unit operation:

NOTE

In the following list, a + symbol represents an add function, a - symbol represents a subtract function, a V symbol represents an OR function, a V symbol represents an exclusive-OR funetion, and a · symbol represents an AND function.

Nanobits 28	29	30	31	Specified Operation	Reserved Word
0	0	0	0	X+Y	+ (add)
0	0	0	1	$\overline{X \vee Y}$	NOR
0	0	1	0	X·Y	NR1
0	0	1	1	X+Y+1	+ +1 (add +1)
0	1	0	0	$\overline{X \cdot Y}$	NAN
0	1	0	1	(XvY)+X	OAD
0	1	1	0	$X \textcircled{v} Y$	XOR
0	1	1	1	X·Y	NIM
1	0	0	0	$\overline{X} \vee Y$	IMP
1	0	0	1	$\overline{X \textcircled{v} Y}$	EQV
1	0	1	0	X+(X·Y)	AAD
1	0	1	1	X·Y	AND
1	1	0	0	X–Y–1	– –1 (subtract –1)
1	1	0	1	$X \vee \overline{Y}$	RIM
1	1	1	0	XvY	OR
1	1	1	1	X–Y	– (subtract)

A circuit description of an Arithmetic Logic Unit module (1447 3730) is presented in Section III. The output functions on the table of arithmetic operations and table of logic functions in Section III are represented by letter designations A and B. The A designation corresponds to an X, and the B designation corresponds to a Y, as specified in the previous description.

The Adder output signals (ADD01 through 16) from the Arithmetic/Logic Unit are sent to the Barrel Switch (BSW) on the LU5 card and are also used as inputs to the B register via the B input select gates on the LU3 and LU4 cards. The most significant bit (MSB) and least significant bit (LSB) of the Adder output signals are sent to the Condition Selector circuits of the Control Unit (CU1 card) for condition testing. The MSB and LSB of the Adder output signals are also sent to the Shift Store control gates of Shift Control Register on the CU2 card via the CU1 card.

The complement four-bit and eight-bit carry signals (CAR1, 5, 9 and 13), which are also generated by the ALU, are sent to the respective B input select Complement Control gates on the LU2-1 through LU2-4 cards. Refer to the B register and associated input selection gates, along with Figure II-10, for information concerning the four-bit and eight-bit carry signals.

The carry signals (CAR1, 5, 9 and 13) are sent to the next higher-significant Arithmetic/Logic Unit module on the LU2-1 through LU2-4 cards. The carry signal indicates a carry out of bit 1, 5, 9, or 13 of the ALU's. The respective carry signal is used as an input to bit "nn-1" of the ALU module. For example, the CAR13 signal is sent to the ALU module that contains Adder bit-12 (nn-1) and CAR9 carry signal is sent to the CN input of the ALU module that contains Adder bit-9. The most significant carry bit signal (CAR1) is sent to the Condition Selection circuits of the Control Unit (CU1 card) for Adder overflow (AOV) test purposes.

Barrel Switch (BSW) And Associated Control Circuits

The Barrel Switch (BSW) is a matrix of gates used to shift a parallel input data word a number of places to the left or right, either end-off or end-around. See Figures II-1 and II-11 for a functional block diagram of the Barrel Switch (BSW) and shift control circuits.

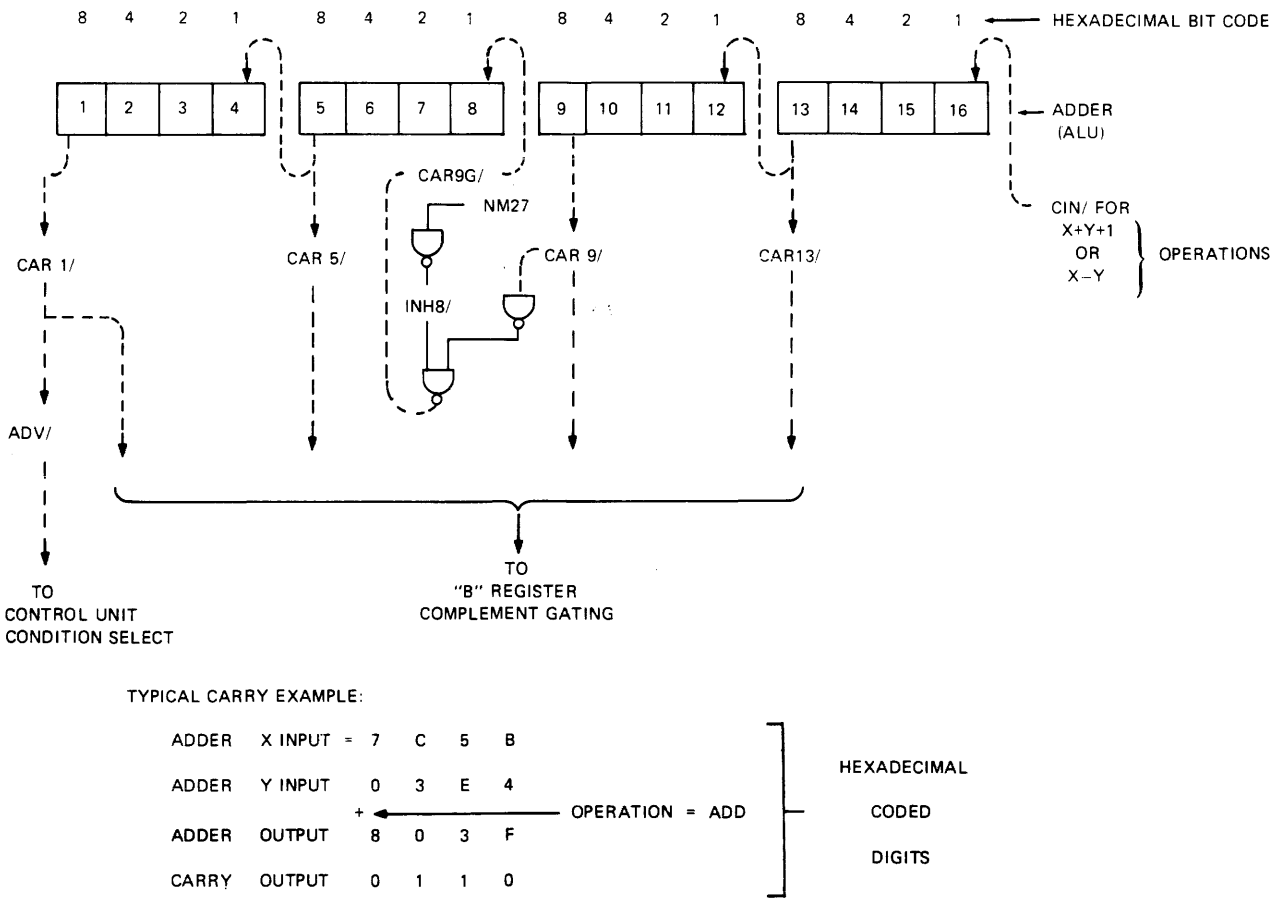


Fig. II-10. ADDER CARRIES

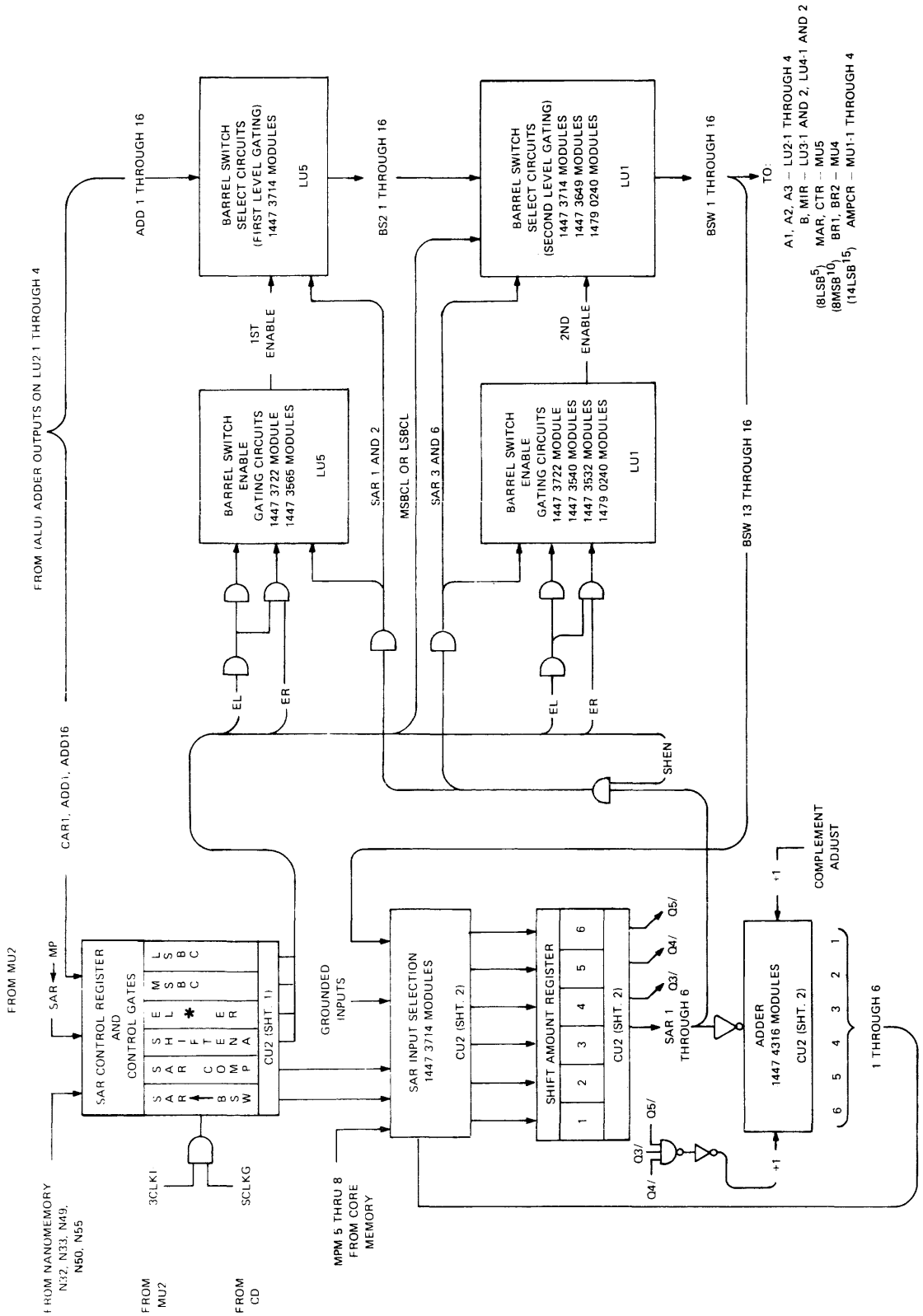


Fig. II-11. BARREL SWITCH (BSW) AND SHIFT REGISTER CONTROL CIRCUITS, BLOCK DIAGRAM BLOCK DIAGRAM

The Barrel Switch (BSW) Enable Gating circuits consist of the BSW Control gate modules (1447 3722) and their associated input gate circuits. The BSW enable gates generate two sets of internal Enable Shift signals. These Enable Shift signals are used to control shifting operations in the first and second level of gating of the Barrel Switch (BSW). The following list indicates which internal enable shift signals are used by the Barrel Switch (BSW) first and second level gates:

Internal Enable Shift Signals	BSW Outputs Enabled
First stage most significant four-bit group	BS201, BS202, BS203, BS204
First stage second most significant four-bit group	BS205, BS206, BS207, BS208
First stage third most significant four-bit group	BS209, BS210, BS211, BS212
Second stage most significant bit	BSW01
Second stage second most significant bit	BSW02
Second stage third most significant bit	BSW03
Second stage least significant bit	BSW16
Second stage second least significant bit	BSW15
Second stage third least significant bit	BSW14
Second stage fourth least significant bit	BSW13

These enable shift signals are generated from the SAR signals of the output gates of the Shift Amount Register (SAR) on the Control Unit (CU2 card) and the Enable Left shift and Enable Right shift control signals (EL and ER) of the shift control circuits, which are also located on the CU2 card. The Enable Left shift signal is true (EL) for both left shifts and right end around (circular) shifts. The Enable Right shift signal (ER) is true at all times except during a left shift. The Enable Left shift and Enable Right shift signals are controlled by the "Shift Selection" nanobits (N32 and N33) from the Nanomemory. The list below provides the nanobit codes for Shift Selection, the Shift operation performed, and the values for ER, EL, and SAR.

For information concerning the use of the Enable Right shift (ER) and Enable Left shift (EL) signals, refer to the Shift Operations information contained under the Shift Amount Register (SAR) heading and the Shift Control Register heading of the CU2 card.

Left shift Barrel Switch operations are actually right shifts using the 2's complement of the desired shift amount value; therefore, all left shifts must be preceded by a Complement SAR Function on the desired shift amount or the 2's Complement as a predetermined constant loaded from MPM to SAR.

The SAR signals CSAR1 and CSAR2 from the output gates of the Shift Amount Register (SAR) control the first level of gating of the Barrel Switch. Signals CSAR3 and CSAR6 control the second level of gating of the Barrel Switch (BSW). Information concerning the SAR signals and their "complements" for system configurations with word lengths of 16-bits is provided in the Shift Operations functional description under the Shift Amount Register (SAR) heading of the CU2 card.

When the internal Enable Shift signals are at a high level, these signals inhibit that particular controlled Barrel Switch bit or group of Bits by forcing it to ZERO. When an Enable Shift signal is at a low level, the particular Barrel Switch bits associated with the signals are enabled.

Nanobits N32	Nanobits N33	Shift Operation	ER	EL	SAR Lines
0	0	No shift	1	0	All ZEROS
0	1	Shift right end-off	1	0	SAR value
1	0	Shift left end-off	0	1	SAR value
1	1	Circular shift (right end around)	1	1	SAR value

Functional Detail

SELECT B and A				STROBE DATA		LOW OUTPUTS	LOW OUTPUTS	
1st STAGE → SAR	1	2		EL	ER	1Y	2Y	
2nd STAGE → SAR	3	6						
0	0			0	0	NONE	0	HIGH = ENABLE;
0	0			1	0	0	NONE	
0	0			1	1	NONE	NONE	
0	1			0	1	NONE	1	LOW = DISABLE FOR 1st OR 2nd STAGE BSW OUTPUT CONTROL
0	1			1	0	1	NONE	
0	1			1	1	NONE	NONE	
1	0			0	1	NONE	2	
1	0			1	0	2	NONE	
1	0			1	1	NONE	NONE	
1	1			0	1	NONE	3	
1	1			1	0	3	NONE	
1	1			1	1	NONE	NONE	

The BSW enable gate modules (1447 3722), which generate the internal enable shift signals use two select inputs (A and B) for SAR inputs 2 and 1, or SAR3 and 6, respectively to direct data input or complement data input through to one of four outputs on eigher 1Y or 2Y gates. 1Y uses NORMAL data input and a strobe gate, while 2Y uses complement data input and a strobe gate. The data and strobe gate inputs are from Enable Left (EL) and Enable Right (ER) shift signals. The above list illustrates the various combinations of EL, ER, and SAR signals to the modules:

The 1Y or 2Y outputs for the first stage are sent to the gating module (1447 3563) to develop only three group enabling signals. When any of these three signals is high, the four BS2nn first stage outputs are disabled at one time.

The second stage BSW enable gating functions just as the first stage, except that SAR3 and SAR6 are used for selecting. The final outputs of the enable gates are used to disable seven different BSW output signals.

The functional equations for the internal enable shift signals are as follows:

ENABLE 1st STAGE MOST SIG. 4-BITS = $ER \cdot EL + \overline{ER} \cdot EL(SAR1 + SAR2) + ER \cdot \overline{EL}(\overline{SAR1 + SAR2})$

ENABLE 1st STAGE 2nd MOST SIG. 4-BITS = $ER \cdot EL + \overline{ER} \cdot EL \cdot SAR1 + ER \cdot \overline{EL} \cdot \overline{SAR1}$

ENABLE 1st STAGE 3rd MOST SIG. 4-BITS = $ER \cdot EL + \overline{ER} \cdot EL(SAR1 \cdot SAR2) + ER \cdot \overline{EL}(\overline{SAR1 \cdot SAR2})$

ENABLE 2nd STAGE MOST SIG. BIT = $EL + ER \cdot \overline{EL}(\overline{SAR3 + SAR6})$

ENABLE 2nd STAGE 2nd MOST SIG. BIT = $EL + ER \cdot \overline{EL} \cdot \overline{SAR3}$

ENABLE 2nd STAGE 3rd MOST SIG. BIT = $EL + ER \cdot \overline{EL}(\overline{SAR3 \cdot SAR6})$

ENABLE 2nd STAGE LEAST SIG. BIT = ER

ENABLE 2nd STAGE 2nd LEAST SIG. BIT = $ER + \overline{ER} \cdot EL(SAR3 \cdot SAR6)$

ENABLE 2nd STAGE 3rd LEAST SIG. BIT = $ER + \overline{ER} \cdot EL \cdot SAR3$

ENABLE 2nd STAGE 4th LEAST SIG. BIT = $ER + \overline{ER} \cdot EL(SAR3 + SAR6)$

The Shift Amount Register (SAR) value (0 through 15) and the shifting of Adder ouput signals ADD1 through ADD16 during a left shift (L) or right shift (R) are shown in Figure II-12. Figure II-12 indicates the Barrel Switch first level of gating. The Barrel Switch inter-connection signals BS21 through BS216 are used between the first and second levels of gating of the Barrel Switch. For a ZERO shift, BS201 through BS216 output signals are the equivalent of the ADD01 through ADD16 input signals.

Figure II-12 indicates the Barrel Switch second level of gating. Barrel Switch output signals BSW1 through BSW16 use the corresponding BS2nn outputs from the first level of BSW gating which had been shifted only for shifts in increments of 4 in (SAR), and accomplishes the shifts required for increments of 1, 2, or 3 (the balance of the shifting not done in the first stage).

Barrel Switch output signals BSW1 through BSW16 are used as the major data outputs of the Logic Unit (LU1 card) that are sent to the following Processor cards:

BSW Destinations	Card Location
A Registers (A1, A2, and A3)	Logic Unit (LU2-1 through 4)
B-Input Select Gates	Logic Unit (LU3-1 and 2, LU4-1 and 2)
Memory Information Register (MIR)	Logic Unit (LU3-1 and 2, LU4-1 and 2)
Shift Amount Register (SAR), four LSB's of BSW	Control Unit (CU2)
Memory Address Register (MAR), eight LSB's of BSW	Memory Control Unit (MU5)
Counter (CTR), eight LSB's of BSW	Memory Control Unit (MU5)
Base Registers (BR1 and BR2), eight MSB's of BSW	Memory Control Unit (MU4)
Alternate Microprogram Count Register (AMPCR), LSB's of BSW	Memory Control Unit (MU1-1 through 4)

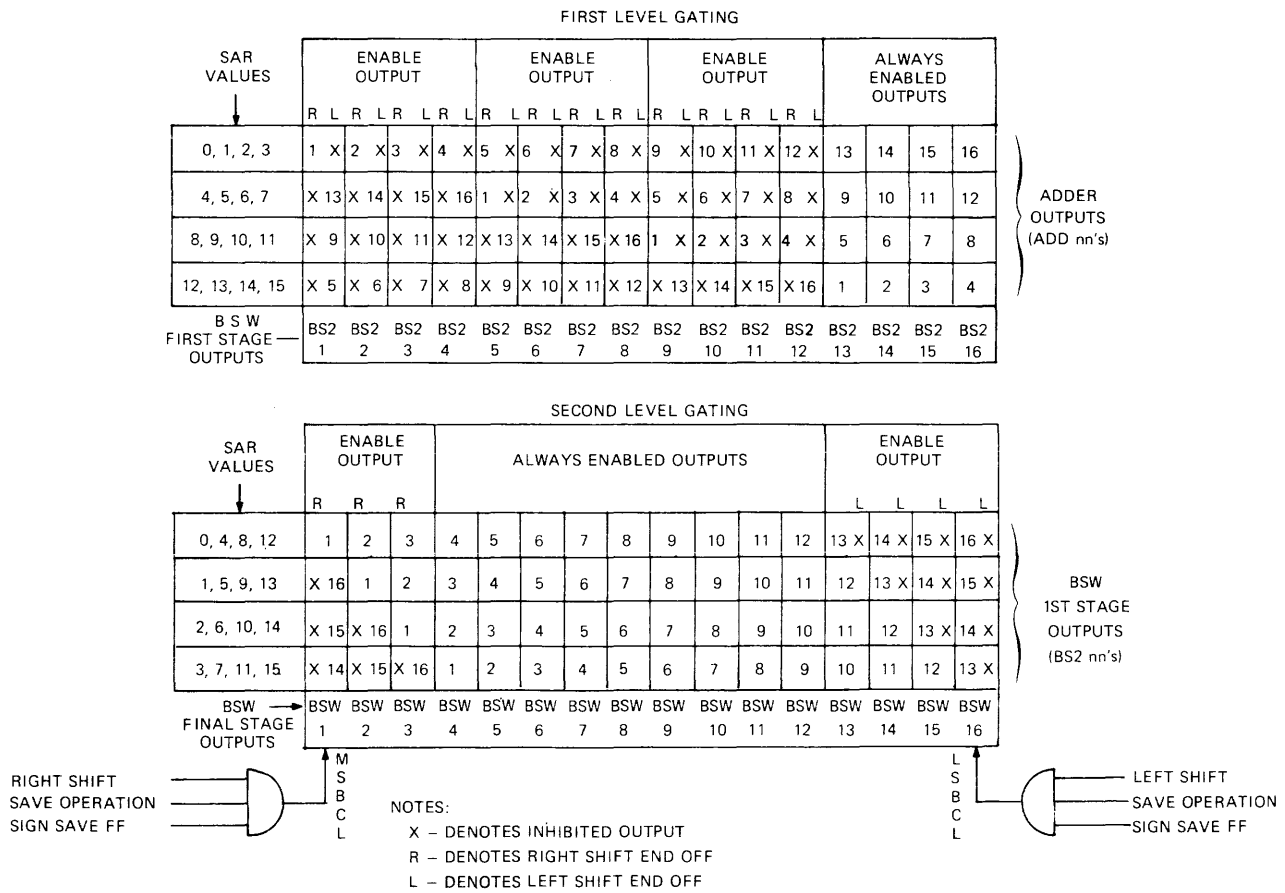


Fig. II-12. BARREL SWITCH (BSW) GATING

Memory Information Register (MIR)

The Memory Information Register (MIR), which is located on the LU3-1 and LU3-2, LU4-1 and LU4-2 card assemblies, is used to buffer output information that is written into Data/Program Memory (DPM), or sent to a peripheral device. See Figure II-1 for the MIR interface within the Processing system. The MIR is also used as input to the "B" Register for processor manipulation of data.

Barrel Switch outputs BSW01 through BSW16 are applied to the respective MIR flip-flops. Control signal DN41 from the Control Register of the Memory Control Unit (MU2 card), which corresponds to nanobit N41 from the Nanomemory, enables the clock pulse to the Memory Information Register. The DN41 signal and the phase 3 clock signal (3CLKD), are applied to NAND gate and are used to clock the MIR flip-flops. Nanobit signal N41 from the Nanomemory is used to determine MIR input selection, as follows:

Nanobit 41	MIR Input Selection
0	No change in the contents of the MIR.
1	Barrel Switch (BSW) outputs to the MIR.

The Clear signal (CLEAR) is used to reset the MIR. MIR outputs (MIR01 through MIR16 signals), which supply output data from the processor, are sent to the Data/Program Memory (DPM), the Device Dependent Port (DDP) for a peripheral device, or can be used as inputs to the B input select gates of the B register.

Figure II-13 is a functional block diagram of the Processing system output area, which includes the input and output logic circuits associated with the MIR. This diagram presents the interface between the Output Select circuits (Base Register 1, Base Register 2, and Memory Address Register), MIR, Port Selector (PS1 card), "S" Memory (DPM), and Device Dependent Ports (DDP's).

CONTROL UNIT (CU1 AND CU2)

The Control Unit (CU1 and CU2) card assemblies can be divided into the following three functional areas: the Shift Amount Register (SAR) and associated control circuits, the Condition Register, and the Shift Control Register and associated control circuits. (See Figure II-1.) Figures II-11 and II-14 are functional block diagrams of the shift control circuits and show the Barrel Switch interface and Condition Register and control circuits.

Shift Amount Register (SAR)

The functions of the SAR and its associated logic circuits are:

a. To load shift amounts from the Microporgram Memory (MPM) or Barrel Switch (BSW) into the SAR for use in shifting operations.
b. To generate the required controls for the Barrel Switch (BSW) to perform the shift operation indicated by the control from the Nanomemory (NM).
c. To generate the complement of the SAR contents, where the complement is defined as the amount that will restore the bits of a word to their original position after an end-around shift of "N".

A literal is loaded into the Shift Amount Register (SAR) from the Microprogram Memory (MPM) by a Type II instruction. The transfer of MPM data to the Shift Amount Register signal (SAR-MPM) is generated by the Microprogram Address (MPAD) controls on MU2. This signal is true when a Microprogram Memory word contains a "1100" or "1101" in the first four bits of the word. Refer to the microcode information for a Type II instruction under microinstruction format heading presented under the Microprogram Memory (MPM) at the beginning of Section II in this manual. (See Figure II-3.)

The bit generated from the Shift Control Register that corresponds to bit-49 of the nanocode (N49) will load the four least significant bits of the Barrel Switch (BSW), which is located on the Logic Unit (LU1) card assembly, into the Shift Amount Register (SAR).

The Shift Amount Register (SAR) and associated logic circuits control the Barrel Switch shift operations, the number of bits to be shifted, and allows either right or left end-off shifts or end-around shifts (circular shifts).

The shift control of the Barrel Switch is accomplished by the Shift Selection bits (N32 and N33) of the Nanomemory (NM). The following list provides the nanobit code for Shift Selection operation:

Nanobits 32	33	Shift Selection Operation	Reserved Word
0	0	No Shift	
0	1	Right shift end-off the entire Adder output, left fill with ZERO's.	R
1	0	Left shift end-off the entire Adder output, right fill with ZERO's.	L
1	1	Circular shift right the entire Adder output (shift end-around).	C

The shift amounts are stored in bits 1, 2, 3 and 6 of the SAR. The SAR gated output signals SAR1 and SAR2 control the first section (level of gating) of the Barrel Switch. Signals SAR3 and SAR6 control the second section of the Barrel Switch. Figure II-15 specifies the contents of the SAR (six bits) for shift amounts of 1 through 15 and their complements for a 16-bit configuration.

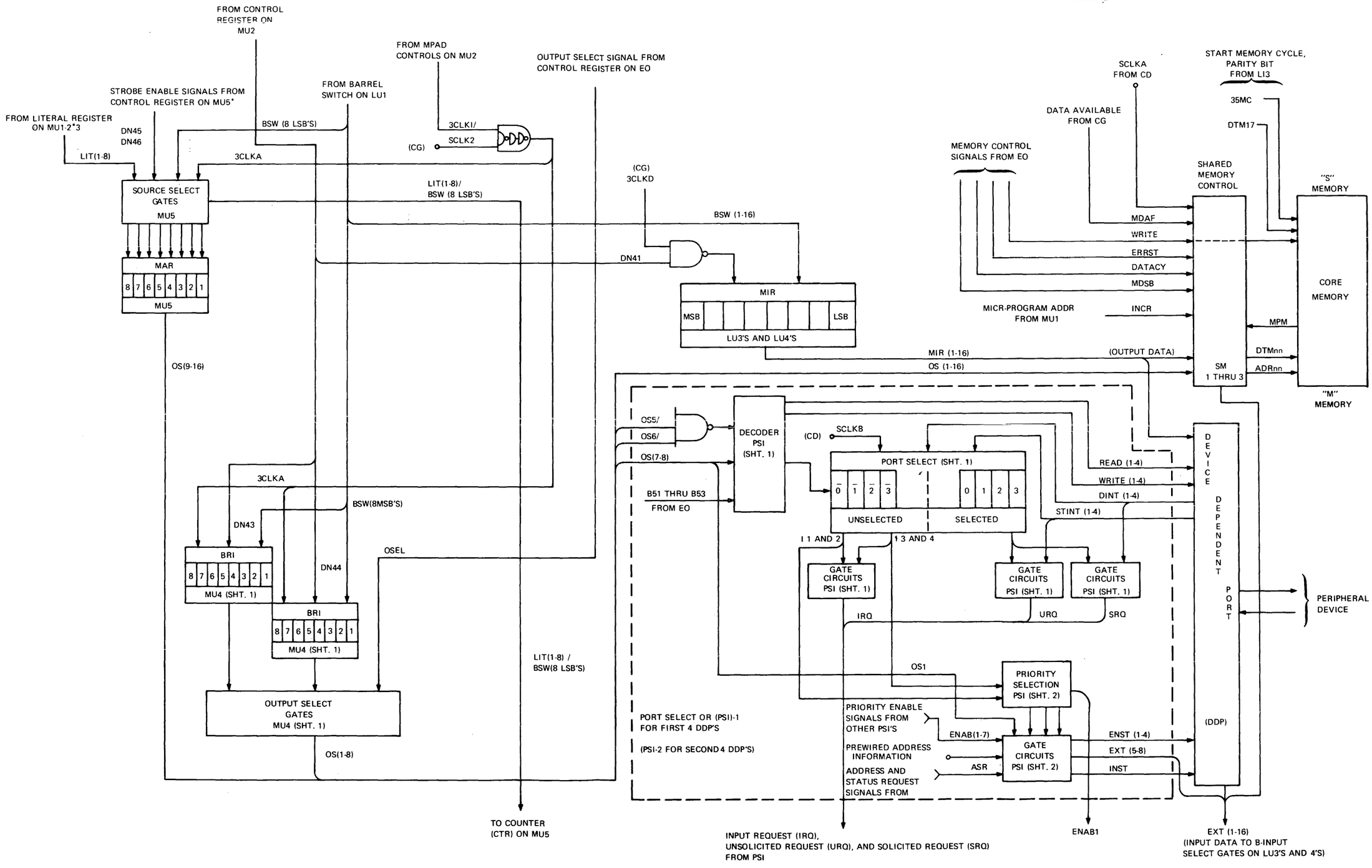


Fig. II-13. OUTPUT AREA, BLOCK DIAGRAM

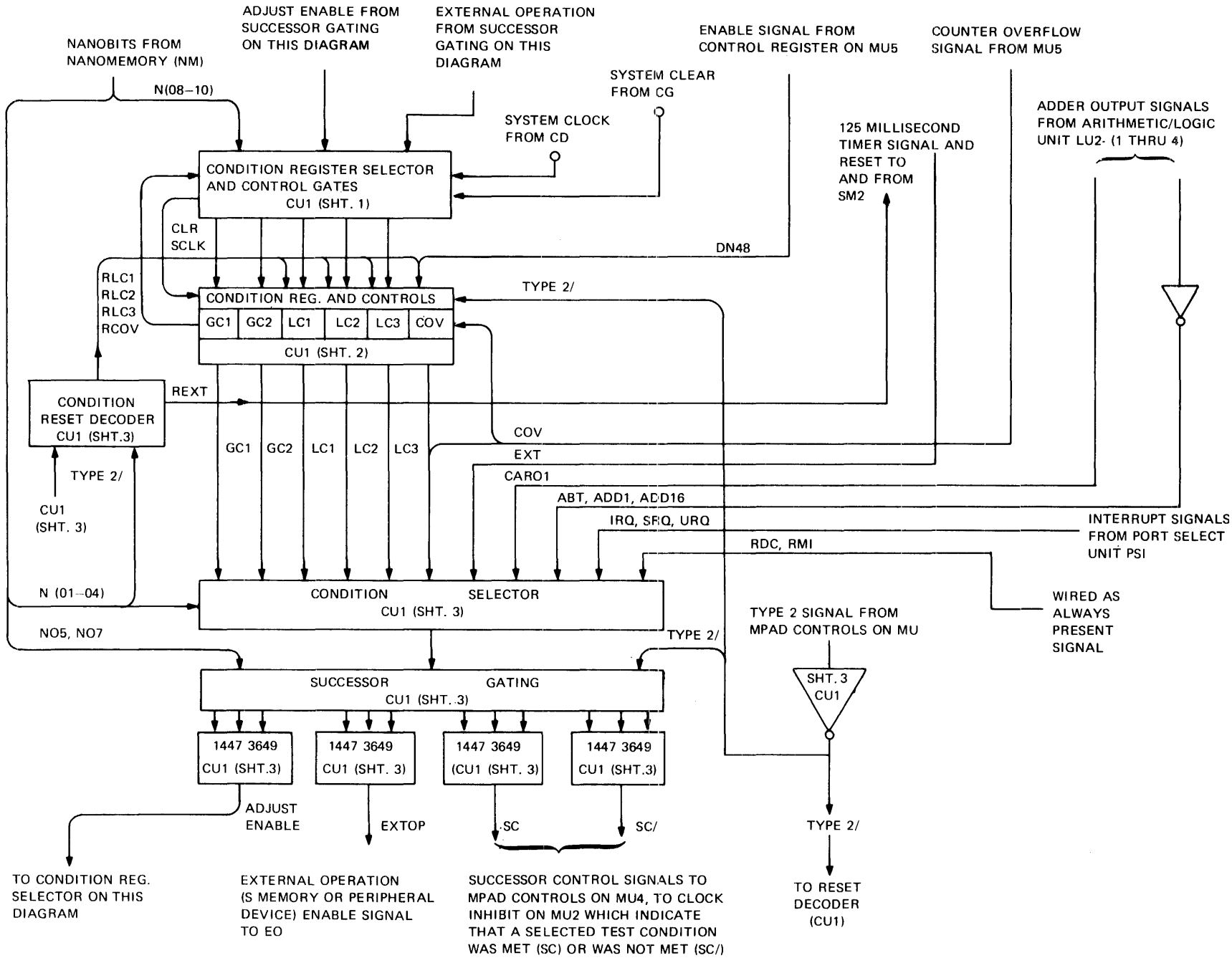


Fig. II-14. CONDITION REGISTER AND CONTROL CIRCUITS, BLOCK DIAGRAM

The no-shift operation requires the Barrel Switch to allow the Arithmetic/Logic Unit (Adder) output to gate through the Barrel Switch with a ZERO shift. Because the SAR may have a shift amount stored in it, the shift amount lines to the Barrel Switch must be forced to ZERO. The enable control lines ER and EL may only be in the equivalent of right shift end-off state at this time.

The SAR control logic controls the Barrel Switch with two enable shift control signals (ER and EL) for end-off or end-around operations. The "enable for right shift" (ER signal) controls the data that is being shifted to the right. The "enable for left shift" (EL signal) controls data that is shifted end-around into the left side of the Barrel Switch. The truth table configuration for these two shift enable signals and the function performed is as follows:

ER	EL	Function
0	0	None (can not occur)
0	1	Enable shift left end-off
1	0	Enable shift right end-off
1	1	Enable shift right end-around (circular shift)

The following truth table configuration relates the SAR controls to the Barrel Switch (BSW) controls:

SAR CONTROLS			BSW CONTROLS		
N32	N33	SAR CONTENTS	ER	EL	SHIFT AMOUNT TO BSW (SAR)
0	0	Non-zero	1	0	All zeros
0	1	Non-zero	1	0	Contents of SAR
1	0	Non-zero	0	1	Contents of SAR
1	1	Non-zero	1	1	Contents of SAR
0	0	All zeros	1	0	All zeros
0	1	All zeros	1	0	All zeros
1	0	All zeros	0	1	All zeros
1	1	All zeros	1	0	All zeros

LOGIC UNIT WIDTH
16 BITS

BIN.	SAR						COMPLEMENT					
	1	2	3	4	5	6						
0	0	0	0	X	X	0	0	0	0	X	X	0
1	0	0	0	X	X	1	1	1	1	X	X	1
2	0	0	1	X	X	0	1	1	1	X	X	0
3	0	0	1	X	X	1	1	1	0	X	X	1
4	0	1	0	X	X	0	1	1	0	X	X	0
5	0	1	0	X	X	1	1	0	1	X	X	1
6	0	1	1	X	X	0	1	0	1	X	X	0
7	0	1	1	X	X	1	1	0	0	X	X	1
8	1	0	0	X	X	0	1	0	0	X	X	0
9	1	0	0	X	X	1	0	1	1	X	X	1
10	1	0	1	X	X	0	0	1	1	X	X	0
11	1	0	1	X	X	1	0	1	0	X	X	1
12	1	1	0	X	X	0	0	1	0	X	X	0
13	1	1	0	X	X	1	0	0	1	X	X	1
14	1	1	1	X	X	0	0	0	1	X	X	0
15	1	1	1	X	X	1	0	0	0	X	X	1

NOTES: 1. THE COMPLEMENTS SHOWN ARE NOT TRUE COMPLEMENTS.
2. AN X INDICATES UNUSED BIT POSITION.
3. A BIN INDICATES BINARY EQUIVALENT.

Fig. II-15. SHIFT AMOUNTS AND THEIR COMPLEMENTS

SAR Complementing

The bit generated from the shift control register that corresponds to bit 50 of the nanocode (N50) causes the complement of the SAR to be loaded into SAR. Figure II-15 indicates the required complement of the SAR contents for this 16-bit word system configuration. The shift amount is in binary form, while the complement (COMP) is the 2's complement of the shift amount. A ground is wired in the X position for the BSW and MPM inputs to the SAR input select circuits. Only SAR bits 1, 2, 3, and 6 are used at the BSW.

Condition Register And Associated Logic Circuits

The Condition Register and associated logic circuits of the Control Unit (CU) perform the following four major functions. (See Figure II-14.)

a. Selects one of 16 condition bits for use in performing conditional operations.
b. Stores six resettable Condition bits in the Condition register.
c. Decodes nanobits from nanomemory (NM) for resetting, setting, or to request the setting of certain bits in the Condition register.

Condition Selection (CONDSEL) and Condition Adjust (CNDADJ)

The 16 condition bits of the Condition Register and associated logic circuits act as error indicators, interrupts, status indicators, and lockout indicators. Six of the condition bits are generated by the Condition Register; six condition bits are from external sources; the four remaining condition bits are generated during one clock time in the Logic Unit. Only one of these 16 conditions can be selected and tested in each microinstruction. Each condition can be tested for either a ZERO or a ONE and is used in conditional, memory conditional, Logic Unit condition, and in Type I microinstructions which determine the Successor Control (SC) selection. The six condition bits generated by the Condition Register and control circuits are:

a. First Global Condition (GC1).
b. Second Global Condition (GC2).
c. First Local Condition (LC1).
d. Second Local Condition (LC2).
e. Third Local Condition (LC3).
f. Counter Overflow (COV).

The first Global Condition bit (GC1) is set and reset locally (refer to Condtion Adjust) within the Processor as a programable flag bit. This Global Condition bit cannot be reset by testing. The functional description for the second Global Condition (GC2) is similar to that described for the first Global Condition (GC1).

The first Local Condition (LC1) bit is used for temporary storage of Boolean conditions (as a flag bit) within the Processor. This Local Condition bit is set locally (refer to Condition Adjust) by the Processor and reset locally by testing. The functional descriptions for the second and third Local Condition (LC2) and (LC3) are similar to that described for the first Local Condition (LC1).

The Counter Overflow (COV) condition bit is used to record overflows from the Counter Register (CTR), which is located in the Memory Control units (MU5 card). This condition bit is set whenever an increment counter operation (INC) causes the Counter (CTR) to overflow. This condition bit is reset when tested or whenever the Counter (CTR) is loaded from either the Barrel Switch (BSW) or the Literal register (LIT). When an attempt is made to set and reset this condition bit at the same clock time, the reset condition is dominant. Any test on this condition bit actually tests the "logical OR" of this bit with the true overflow from the Counter (CTR). The COV condition bit is set if the Counter (CTR) is all ONEs and an increment operation (INC) was in the Type I instruction whose phase 3 is currently being executed. Signal DN48 from the Control Register of the Memory Control units (MU5 card) is used as an input to a gate circuit, along with an output of the Condition Reset Decode module to reset the Counter Overflow flip-flop of the Condition Register. The DN48 signal corresponds to the complement of nanobit N48 from the Nanomemory.

The Condition Selection for Global Conditions, Local Conditions, and Counter Overflow are controlled by nanobits N01 through N04 from the Nanomemory which specify the particular condition to be tested. The following list provides the nanobit code for Condition Selection of the aforementioned conditions, how the condition is set

Nanobits					How Condition Set or Reset		Dominant
1	2	3	4	Condition Selection			Function
0	0	0	0	Global Condition 1 (GC1)	CAJ	CAJ	Set
0	0	0	1	Global Condition 2 (GC2)	CAJ	CAJ	Set
0	0	1	0	Local Condition 1 (LC1)	CAJ	Test	Set
0	0	1	1	Local Condition 2 (LC2)	CAJ	Test	Set
1	1	0	1	Local Condition 3 (LC3)	CAJ	Test	Set
1	0	0	0	Counter Overflow (COV)	Overflow	Test	Reset

and reset, and the resultant condition (dominant function) when the condition bit is both set and tested in the same microinstruction:

CAJ is Condition Adjust; nanobits N08 through N10.

The Condition Adjust provides the means by which condition bits can be set to ONE or reset to ZERO. The Condition Adjust operation takes place at the end of a phase 1 operation. The Condition Adjust for the Global Conditions and Local Conditions are controlled by nanobits N08, N09, and N10 from the Nanomemory which specify the particular condition to be adjusted. The following list provides the nanobit code for Condition Adjust of the aforementioned conditions:

Nanobits 8	9	10	Condition Adjust Function
0	0	0	No change
0	1	1	Set Local Condition 2 (LC2)
0	1	0	Set Global Condition 2 (GC2)
0	1	0	Set Global Condition 2 (GC2)
0	1	1	Reset Global Condition 2 (GC2)
1	0	0	Set Local Condition 3 (LC3)
1	0	1	Reset Global Condition 1 (GC1)
1	1	0	Set Global Condition 1 (GC1)
1	1	1	Set Local Condition 1 (LC1)

The six condition bits generated by external sources are as follows:

a. Ready Memory Information Register (RMI).
b. Read Complete (RDC).
c. Input Request (IRQ).
d. External Interrupt (EXT).
e. Solicited Request (SRQ).
f. Unsolicited Request (URQ).

The Ready Memory Information Register (RMI signal) is always present (low active) on the Condition Select module of the Condition Control circuits on the CU1 card.

The Read Complete (RDC signal) is always present (low active) on the Condition Select module of the Condition Control circuits on the CU1 card. Because the Read Cycle is completed in one clock time, RDC always indicates that data is available from a memory read operation (MR1 or MR2).

The Input Request (IRQ signal) from the Port Selector (PS1 card) is sent to the Condition Select module of the Condition Control circuits on the CU1 card. When this signal is at a low level, it indicates that a DDP which is unselected and is generating a Status Interrupt (STINT) or Data Interrupt (DINT).

The External Interrupt (EXT signal) from the Shared Memory Control (SM2) is sent to the Condition Select module of the Condition Control circuits on the CU1 card. When this signal is at a low level, it indicates that a real time Counter is set equal to 125 milliseconds.

The Solicited Request (SRQ signal) from the Port Selector (PS1 card) is also sent to the Condition Select module. When this signal is at a low level, it indicates that the selected DDP is generating a Data Interrupt (DINT).

The Unsolicited Request (URQ signal) from the Port Selector (PS1 card) is also sent to the Condition Select module. When this signal is at a low level, it indicates that the selected DDP is generating a Status Interrupt (STINT).

The Condition Selection for the Ready MIR (RMI), the Read Complete (RDC), Input Request (IRQ), External Interrupt (EXT), Solicited Request (SRQ), and Unsolicited Request (URQ) conditions are controlled by nanobits N01 through N04 from the Nanomemory. The following list provides the nanobit code for Condition Selection of the aforementioned conditions:

Nanobits 1	2	3	4	Condition Selection
1	0	0	1	Ready Memory Information Register (MIR)
1	0	1	0	Read Complete (RDC)
1	0	1	1	Input Request (IRQ)
1	1	0	0	External Interrupt (EXT)
1	1	1	0	Solicited Request (SRQ)
1	1	1	1	Unsolicited Request (URQ)

Nanobit signals N01 through N04 are applied to the Condition Reset Decode module and the Condition Selection module of the Condition Control circuits to control Condition Selection for the six condition bits generated by external sources.

In addition to the aforementioned 12 condition bits, the four remaining condition bits are generated in the Logic Unit (LU2 (1 through 4) cards) during a phase 3 operation for the previous fetched instruction. The four condition bits from the Logic Unit are as follows:

a. Most Significant Bit Condition (MST).
b. Least Significant Bit Condition (LST).
c. Adder Bits True (ABT).
d. Adder Overflow (AOV).

The Most Significant Bit condition (MST) is the state of the most significant bit (MSB) of the Adder output during the preceding microinstruction (independent of shifting). The MSB from the Adder, signal ADD1, is sent to the Condition Selection module of the Condition Control circuits from the MSB Arithmetic/Logic Unit (ALU) module on the LU2-1 card.

The Least Significant Bit condition (LST) is the state of the least significant bit (LSB) of the Adder

output during the preceding microinstruction (independent of shifting). The LSB from the Adder, signal ADD16, is sent to the Condition Selection module of the Condition Control circuits from the LSB Arithmetic/Logic Unit (ALU) module on the LU2-4 card.

The Adder Bits True (ABT signal) from the Arithmetic/Logic Unit (ALU) modules on the LU2 (1 through 4) cards are sent to the Condition Selection module of the Condition Control circuits. This signal indicates that all of the outputs from the Adder are all ONES during the phase 3 portion of the previously fetched microinstruction. Adder output signals ADD1 through ADD16 are all ONES for this condition.

The Adder Overflow (CAR1 signal), which is the most significant bit carry from the LU2-1 card, is sent to the Condition Select module of the Condition Control circuits. The AOV condition is the carry out of the most significant bit of the Adder for the previous fetches microinstruction.

The Condition Selection for the Most Significant Bit condition (MST), the Least Significant Bit condition (LST), Adder Bits True (ABT), and Adder Overflow (AOV) conditions are controlled by nanobits N01 through N04 from the Nanomemory which specify the particular condition to be tested. The following list provides the nanobit code for Condition Selection of the aforementioned conditions:

Nanobits 1 2 3 4	Condition Selection	Reset by Testing
0 1 0 0	Most Significant Bit of Adder (MST)	No
0 1 0 1	Least Significant Bit of Adder (LST)	No
0 1 1 0	Adder Bits True (ABT)	No
0 1 1 1	Adder Overflow (AOV)	No

Successor Controls (SC)

The output signals from the Successor Control (SC) modules of the Condition Control circuits are used in the conditional part of the microinstruction to specify the true-successor (SC = 1) and the false successor (SC = 0). Successor Control signal SC=1 indicates that the selected condition test was met. Successor Control signal SC = 0 indicates that the selected condition test was not met. The Successor Control output signals are sent to the Microprogram Address (MPAD) controls of the Memory Control Units (MU4 card).

Nanobit Signal N05, the Condition tested equal true or false (true), and the Type 2 Signal inverted are applied through successor gating to the 1447 3649 gating modules producing logical outputs as illustrated in the following equations:

SC = (N05/+CONDITION)·(N05+CONDITION/) ·TYPE 2/

SC/ = (N05/+CONDITION/)·(N05+CONDITION) TYPE2/

Nanobit Signal N05 selects the level of the Condition being tested for successor determination. When the Condition level being tested is met (true), the true-successor is performed (SC = 1). A true-successor must appear with each condition test. If the condition being tested is not met, or is false, the false-successor is performed (SC=0). A false-successor is optional; therefore, if a false-successor is not present, the successor STEP causes the next microinstruction in sequence to be performed. The successor STEP is performed by the Microprogram Address (MAPD) controls by incrementing the contents of the Microprogram Count Register (MPCR) by +1. The Successor Condition (SC) is controlled by nanobit N05, as follows:

Nanobit 5	Function Specified
0	Test for false state of specified condition. SC=1 if Condition Selection (CONDSEL) is false.
1	Test for true state of specified condition. SC-1 if Condition Selection (CONDSEL) is true.

Refer to the Microprogram Address (MPAD) controls information contained under the Memory Control unit heading for information concerning the Successor Controls (SC) and their operation with the MPAD controls.

External Operation

Nanobit signal N07 from nanomemory is applied along with nanobit N05, the Condition being tested equal to true or false (true/), and the type 2 signal inverted, to gating modules 1447 3649. The following output signals as illustrated in the following logical equations:

EXTOP = (N05+CONDITION/+N07/) · (N05+CONDITION+N07/) · TYPE2/

ADJUST ENABLE = (N05 · CONDITION · TYPE2/) +(N05/ · CONDITION/ · TYPE2/)+(N07/ · TYPE2/)

The external operation (EXTOP) output signal is sent to the external operations Control (EO card) to Control Memory or Device functions, and the adjust enable signal along with (EXTOP) signal is sent to the Condition Adjust Circuits to control the setting and resetting of global and local flags.

The (EXTOP) signal used to enable Memory or Device operations (MDOP) and the Condition Adjust (CNDADJ) enable signal is controlled by nanobit N07 as follows:

Nanobit 7	Function Specified
0	Perform Memory or Device Operation (MDOP) and Condition Adjust (CNDADJ) unconditionally.
1	Perform MDOP and CNDADJ if Successor Control SC=1.

Shift Control Register And Associated Circuits

The Shift Control Register (SCR) and associated circuits are comprised of six flip-flops and associated input and output gate circuits. (See Figure II-1-9.) The following six flip-flops in SCR are used for Shift Amount Register (SAR) input selection, shift selection, and Save Sign Control (SSC):

a. BSW→SAR.
b. Complement SAR.
c. Shift Right.
d. Shift Left.
e. Saved Sign Bit,
f. Save Sign Control.

Shift Amount Register (SAR) Input Selection

The SAR input selection is controlled by the Shift Control Register flip-flops: BSW→SAR and Complement SAR. The input to these fip-flops is controlled by nanobit N49 or N50 from the Nanomemory. The gated output signal from the BSW→SAR flip-flop is sent to the SAR input select circuits of the CU2 card (sheet 2 of logic diagram). The gated output signal from the Complement SAR flip-flop is also sent to the SAR input select circuits.

When the Shift Amount Register is used (SAR←BSW), the four least significant bits of the Barrel Switch (BSW) are placed in the SAR (1, 2, 3, and 6) flip-flops. When the complement SAR (CSAR) is used , the contents of the SAR are complemented. (See Figure II-15.)

Nanobit signals N49 and N50 from the Nanomemory control Shift Amount Register (SAR) input selection as follows:

Nanobits 49	50	Function Specified
0	0	No change in the contents of the Shift amount register (SAR).
0	1	The contents of the SAR are complemented (CSAR).
1	0	The four least significant bits of the Barrel Switch (BSW) are placed in the SAR.

Shift Selection

The Shift selection is controlled by the Shift Control Register flip-flops: Shift Right and Shift Left. The input to these flip-flops are controlled by nanobits N33 and N32. The gated output signals (ER and EL) are sent to the Barrel Switch Shift Control circuits of the Logic Unit (LU1 and LU5 cards). The gated output signal (SHEN) is sent to the SAR output select circuits for shift control. This signal indicates that a shift condition is present.

The Enabled Left shift control signal (EL) is sent directly to the BSW shift control circuits. This signal is true (high level), for both left shift and right end-around (circular) shifts. The Enable Right shift control signal (ER) is also sent to the BSW shift control circuits. This signal should be true (high level) at all times except during a shift-left operation. The number of bits to be shifted is obtained from the current contents of the Shift Amount Register (SAR) at the start of the phase 3 clock which executes the shift instruction. Nanobits N32 and N33 are used to generate the Shift Selection control signals as indicated in the following list:

Nanobits 32	33	Function Specified
0	0	No shift.
0	1	Indicates a right end-off shift with left ZERO fill. The shift amount is contained in the SAR. Which determines the actual number of bits to be shifted to the right.
1	0	Indicates a left end-off shift with right ZERO fill. The shift amount is located in the SAR, which contains the complement of the number of bits to be shifted to the left. The complement must be stored in the SAR because all shifting operations are performed as right shifts.
1	1	Indicates a right end-around (circular) shift. The shift amount is located in the SAR, which contains the actual number of bits to be shifted to the right.

Refer to the shift operatons description under the Shift Amount Register (SAR) heading for additional information.

Save Sign Control

The Save Sign Control (SSC) is comprised of the Shift Control Register flip-flops: Save Sign Control and Saved Sign Bit. The Save Sign Control flip-flop input is

provided by nanobit N55 from the Nanomemory. The Input Data (D) to the Saved Sign bit flip-flop is provided by an AND-OR-INVERT gate circuit. The inputs to this gate circuit are as follows: the LSB output of the Adder (ADD16/) and the set output of the Shift Right flip-flop; the MSB output of the Adder (ADD1/) and the set output of the Shift Left flip-flop; and the MSB carry signal (CAR1/), SHEN/, and the set output of the Save Sign Control flip-flop.

When the Save Sign Control (SSC) operation is used and a shift operation is being executed, the first end bit shifted is stored in the Saved Sign Bit flip-flop (SSF). Either the MSB or LSB of the Adder output (ADDnn01/ or 16/) is stored in the SSF, depending upon the shift operation (shift right or shift left). Simultaneously, the prior bit stored in the Saved Sign Bit flip-flop (SSF) is placed in the opposite end bit position of the Barrel Switch (BSW) by either signal MSBCL or LSBCL. Signal LSBCL is used to force a bit into the least significant bit (LSB) of the Barrel Switch second-level gating in the Logic Unit (LU1 card). Signal MSBCL is used to force a bit into the most significant bit (MSB) of the Barrel Switch second level of gating in the Logic Unit (LU1 card).

When the Save Sign Control (SSC) is not used and a shift operation (shift right on shift left) is executed, the first end-off bit is stored in the Saved Sign Bit flip-flop (SSF) and no other action occurs. (Signal's LSBCL or MSBCL are not generated.) When SSC is used and shift operation is not being executed (signal SHEN is not present), the Adder Overflow (AOV), which is indicated by the presence of the CAR1 signal, is stored in Saved Sign Bit flip-flop (SSF). No other action occurs at this time. When SSC is not used and a shift operation is not being executed, no change takes place in the Save Sign Control circuits.

Nanobit N55 is used to determine the Shift Store Control function as follows:

Nanobit 55	With Shift Operation (SHIFT)	Without Shift Operation (SHIFT)
0	First end-off bit of Adder to Saved Sign Bit flip-flop (SSF). SHIFT:END-OFF→SSF	No change SHIFT: NO ACTION
1	First end-off bits of the Adder to the Saved Sign Bit flip-flop prior (SSF) to the oposite end-bit of the Barrel Switch (BSW). SHIFT:END-OFF→SSF→BSW	Adder Overflow (AOV) to the Saved Sign Bit flip-flop (SSF) SHIFT:AOV→SSF

MEMORY CONTROL UNIT (MU1 THROUGH MU5)

The Memory Control Units (MU1-1 through MU1-4, MU2, MU3, MU4 and MU5 card assemblies) can be divided into the following four functional areas: the Microprogram Address (MPAD) section, the Memory/Device address section, the Z Register section and the Control Register section. Figure II-16 is a functional block diagram of the Microprogram Count Register (MPCR), Alternate Microprogram Count Register (AMPCR), Incrementer (INCR), and the Microprogram Address (MPAD) controls. The Base Registers (BR1 and BR2), the Memory Address Register (MAR), and associated output select gates are shown in Figure II-13. Figure II-17 is a functional block diagram of the Literal Register (LIT) and Counter Register (CTR) with associated input/output circuits.

Microprogram Address (MPAD) Section

The Microprogram Address (MPAD) section consists of the Microprogram Count Register (MPCR), Alternate Microprogram Count Register (AMPCR), the Incrementer (INCR), the MPAD Controls, and the associated control logic circuits. The MPAD section is used to address the Microprogram Memory (MPM) and is also used to determine the sequencing of microinstructions in the MPM. The MPAD controls of the MPAD section are used to control the loading of the MPCR, loading of the AMPCR, selection of inputs to the Incrementer (INCR), loading of the Shift Amount Register (SAR) from the MPM, loading of the Literal register (LIT) from the MPM, and the generation of the Type II instruction control signal and the phase 3 clock inhibit signal.

Microprogram Count Register (MPCR)

The Microprogram Count Register (MPCR) is a 14-bit register which contains the microinstruction address counter for the Microprogram Memory (MPM). The MPCR contains the current microinstruction address for all successors with the exception of Execute (EXEC). For further information concerning successors, refer to the information provided under the MPAD Controls heading. The MPCR is located on Memory Control unit card assemblies MU1-1, MU1-2, MU1-3 and MU1-4. The MPCR can only be loaded with output data from the Incrementer Register select gates, which are also located on the MU1-1 through MU1-4 cards. The output signals from the Incrementer select gates (INCRXX through INCRX120) are applied directly to the D input of the respective MPCR flip-flop (MX through M12). The clock inputs (C) to the MPCR flip-flops are provided by NAND gates with the following inputs: ScLKn and MPCREN. Signal ScLKn is the system clock from the clock circuits of the Clock Generator (CG card). Signal MPCREN is the input enable signal from the MPAD Controls on the MU4 card. This signal enables the strobe to the MPCR which causes the

Functional Detail

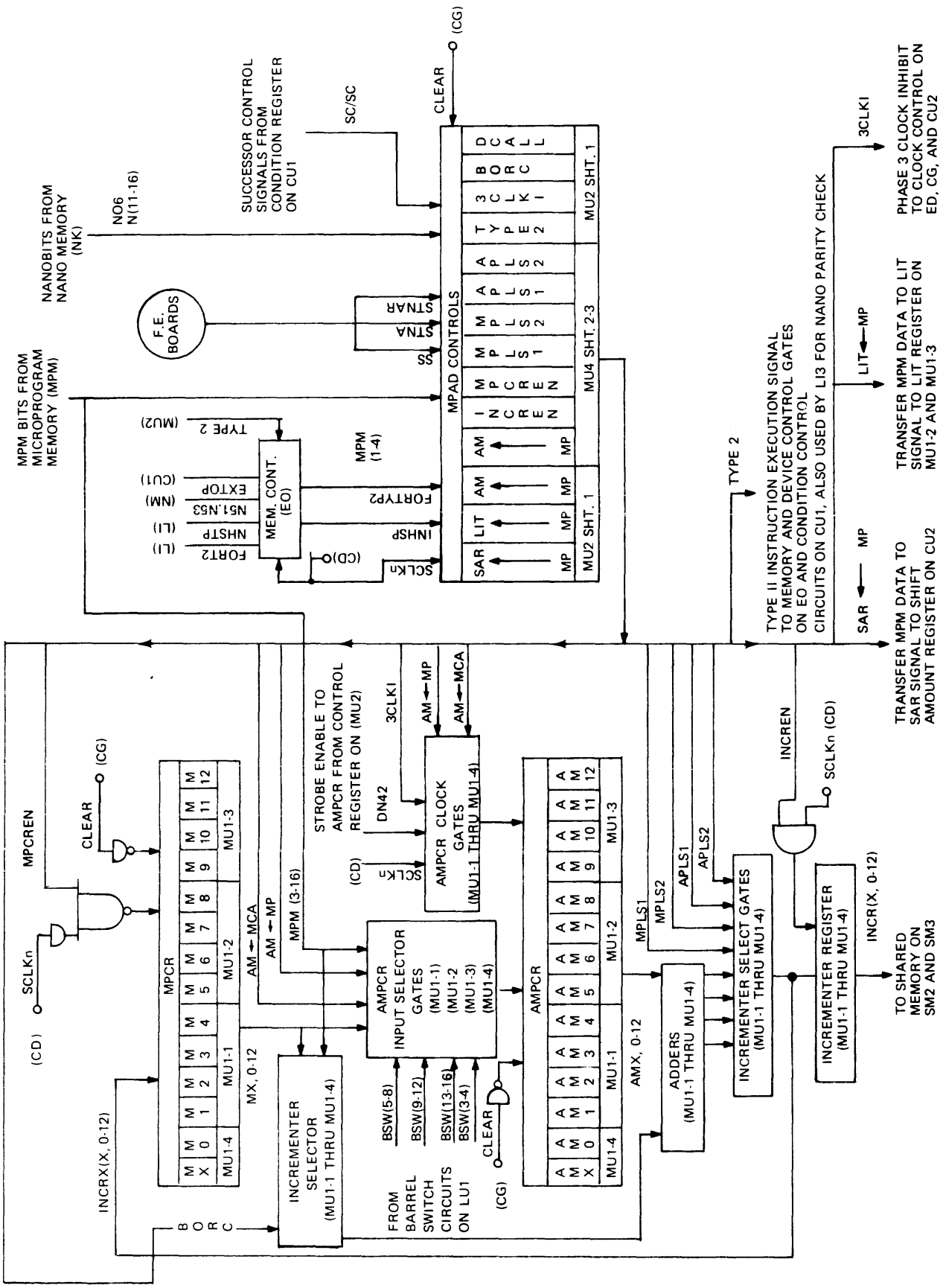


Fig. II-16. MICROPROGRAM COUNT REGISTER (MPCR), ALTERNATE MICROPROGRAM COUNT REGISTER (AMPCR), AND MICROPROGRAM ADDRESS (MPAD) CONTROLS, FUNCTIONAL BLOCK DIAGRAM

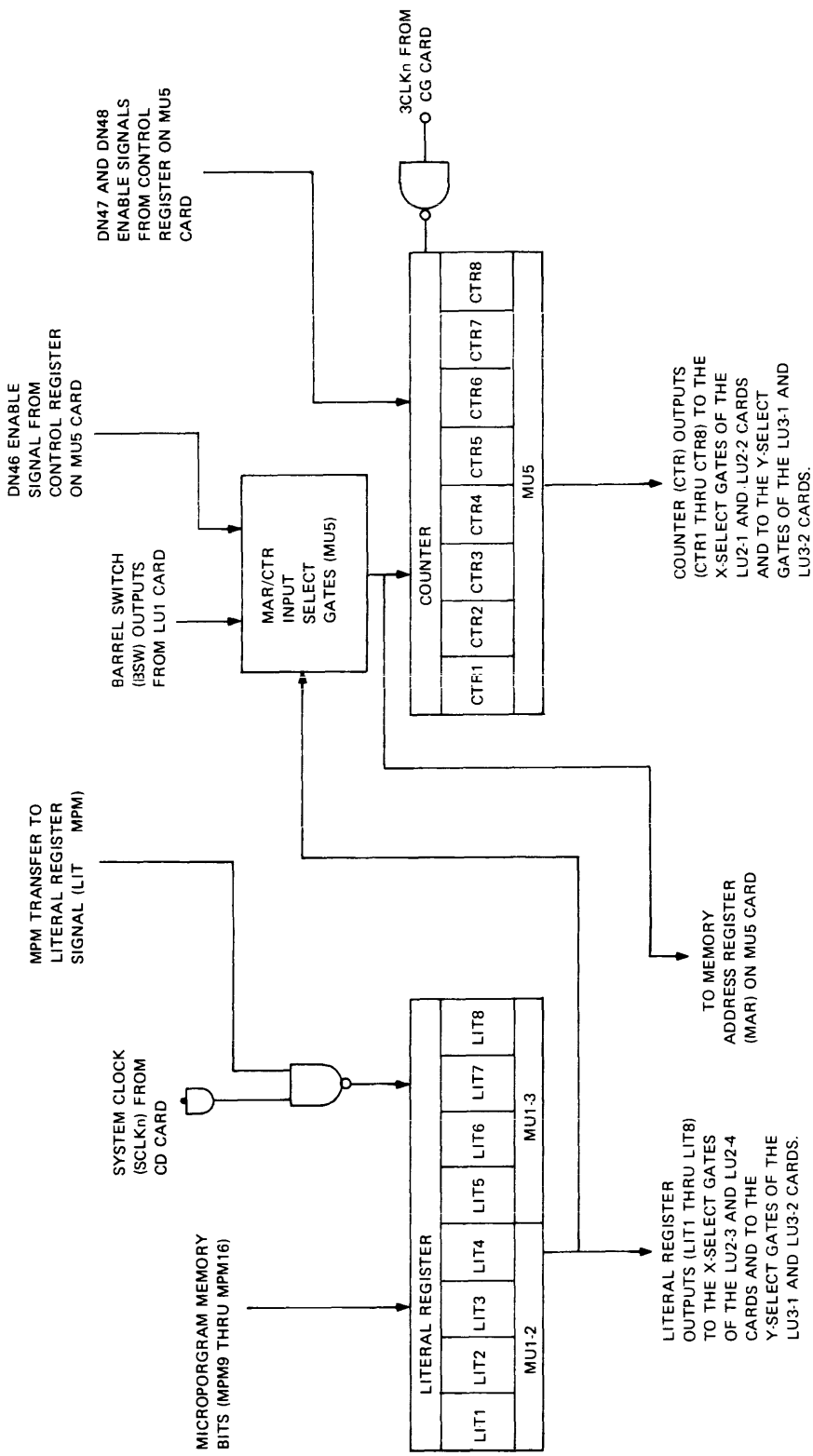


Fig. II-17. COUNTER (CTR) AND LITERAL REGISTER (LIT), FUNCTIONAL BLOCK DIAGRAM

MPCR to store Incrementer Register select gate outputs (INCRXX through INCRX12).

The outputs from the MPCR flip-flops (MX through M12---1 signals) are sent to the Incrementer Selector and are also used as inputs to the AMPCR input selector gates. MPCR output signals MX and M0 are generated on the MU1-4 card, signals M1 through M4 are generated on the MU1-1 card, signals M5 through M8 are generated on the MU1-2 card, and signals M9 through M12 are generated on the MU1-3 card. These MPCR output signals are sent to the respective Incrementer input gate circuits (M+1 Adder or M+2 Adder) and AMPCR input select gates.

Alternate Microprogram Count Register (AMPCR)

The Alternate Microprogram Count Register (AMPCR) is a 14-bit register which contains the jump, execute, call, and return addresses for instruction flow of routines and subroutines within the microprogram that is contained in the Microprogram Memory (MPM). For further information concerning the successors JUMP, CALL, EXEC (execute), and RETN (return), refer to the information provided under the MPAD Controls heading. The address contained in the Alternate Microprogram Count Register (AMPCR) is usually one less than the address to be jumped to or returned to. The (AMPCR) may also be used as temporary storage of microprogram data.

The AMPCR is located on Memory Control Unit card assemblies MU1-1 through MU1-4. The AMPCR can be loaded from the MPCR, the Microprogram Memory (MPM), or the 14 least significant bits (LSB's) from the Barrel Switch (BSW) which is located in the Logic Unit (LU1 card).

The inputs to the AMPCR input select gates are the MX through M12 signals from the MPCR, the MPM3 through MPM16 signals from the Microprogram Memory, and the 14 LSB's of the Barrel Switch signals BSW03 through BSWnn16. Input transfer signals AM MCA and AM MP are sent to the AMPCR input select gates and also to the AMPCR clock gates from the MPAD Controls of the MU2 and MU4 cards. Signal AM MCA is used to transfer MPCR outputs (MX through M12 signals) to the AMPCR. Signal AM MP is used to transfer Microprogram Memory outputs (MPM3 through MPM16 signals) to the AMPCR.

The data inputs (D) of the AMPCR flip-flops (AMX through AM12) are provided from the respective outputs from the AMPCR input select gates. The clock inputs (C) to the AMX through AM12 flip-flops are provided by the outputs from AND-OR-INVERT gates with the following inputs: SCLKn, AM MCA, AM MP, phase 3 clock inhibit (3CLKI), and DN42. DN42 is from the Control Register on the MU2 card and corresponds to nanobit N42 from the Nanomemory. Signal SCLKn is the system clock signal which is present for phase 1 and phase 3 operations from the clock circuits on the CD card. The phase 3 operation is inhibited during Type II microinstructions or when conditional Logic Unit microinstructions are not executed (condition not met). Signal 3CLKI is the phase 3 clock inhibit signal from the MPAD Controls on the MU2 card. When this signal is at a low level, the generation of phase 3 clock operation is inhibited.

Nanobit N42, which corresponds to the DN42 output signal from the Control Register on the MU2 card, is used to control AMPCR input selection as follows:

Nanobit 42	AMPCR Function Specified
0	No change in AMPCR.
1	Twelve least significant bits (14 LSB's) of the Barrel Switch (BSW) entered in the AMPCR.

When loading data into the AMPCR from the Barrel Switch (BSW), the storing of BSW data does not take place until the phase 3 clock time of the next Type I microinstruction occurs. However, the storing of the AMPCR contents into a register does occur within the clock time for that microinstruction in which the transfer appears.

Incrementer Register (INCR)

The Incrementer Register (INCR) and associated gate circuits add a one (+1) or two (+2) to the selected Incrementer Register input from the Microprogram Count Register (MPCR), the Type II Branch or Call Microcode (MPM) or Alternate Microprogram Count Register (AMPCR). The Incrementer Register (INCR) is a 14-bit register which increments by a +1 or +2 the address of the next microinstruction to be executed by the microprogram.

The Incrementer Adder gates (M+1, M+2, AM+1, and AM+2 Adder gate circuits) receive input signals MX through M12 or MPM3 through MPM16 from the MPCR/MPM Selector and input signals AMX through AM12 from the AMPCR. The outputs from these gates are sent to the respective Incrementer register AND-OR-INVERT input gate, along with one of the following control signals from the MPAD controls of the MU4 card: MPLUS1, MPLUS2, APLUS1, and APLUS2. Signal MPLUS1 and MPLUS2 are the transfer MPCR signal to the Incrementer Register select gates. When these signals are at a high level, they indicate an increment of +1 or +2 for the respective signal. Signals APLUS1 and APLUS2 are the transfer AMPCR signals to the Incrementer Register input gates. When these signals are at a high level, they indicate an increment of +1 or +2 for the respective signal.

The clock input (C) of the Incrementer Register is provided by two input AND gates with the following input signals: INCREN and SCLKn. Signal INCREN is the Incrementer Register (INCR) input enable signal from the MPAD Controls of the MU4 card. This signal enables the strobe to the INCR which causes the INCR to store the Incrementer Register select gate outputs (INCRXX through INCRX12). Signal SCLKn is the system clock from the clock circuits on the CD card.

The carry output signals from the M+1 and M+2 Adder gate circuits of the Incrementer are as follows: M1C1, M2C1, M1C5, M2C5, M1C9, and M2C9. These signals are the MPCR+1 and MPCR+2 Adder carries from the respective bit-1, bit-5 or bit-9 of the M+1 and M+2 Adder gate circuits (C4 output of Adder circuit). These carry signals are used as inputs to the CO inputs of the other M+1 and M+2 Adder gate circuits of the Incrementer.

The carry output signals from the AM+1 and AM+2 Adder gate circuits of the Incrementer are as follows: A1C1, A2C1, A2C5, A2C5, A1C9, and A2C9. These signals are the AMPCR+1 and AMPCR+2 Adder carries from the respective bit-1, bit-5, or bit-9 of the AM+1 and AM+2 Adder gate circuits (C4 output of Adder circuit). These carry signals are used as inputs to the CO inputs of the other AM+1 and AM+2 Adder gate circuits of the Incrementer.

The output signals (INCRX through INCR12) from the Incrementer Register (INCR) are used to provide address information in the Microprogram Memory. The output signals (INCRXX through INCRX12) from the Incrementer Register select gates are sent to the respective data (D) input of the Microprogram Count Register (MPCR) flip-flops.

Microprogram Address Control (MPAD CNTL)

The Microprogram Address Control (MPAD CNTL) circuits are used to control the loading of the Microprogram Count Register (MPCR), the loading of the Alternate Microprogram Count Registers (AMPCR) from the MPCR, the selection of inputs used by the incrementer circuits, and also the selection of values to be used by the incrementer circuits. The MPAD Controls are also used to decode control bits from the Microprogram Memory to determine the destination for the contents of the remaining bits in an MPM word.

The MPAD Controls are used to generate the controls that are required to perform the following eight Successor commands: WAIT, STEP, SAVE, SKIP, JUMP, EXEC, CALL, and RETN. The controls for these eight Successor functions (commands) are determined by nanobit inputs from the Nanomemory and the true or false Successor Control (SC) functions from the Successor Control circuits of the Control (SC) functions from the Successor Control circuits of the Control Unit (CU1 card). The MPAD Controls are also used to decode control bits from the Microprogram Memory (MPM) to determine the destinations for the contents of the remaining bits in an MPM word for Type I and Type II microinstructions.

The MPAD Control gate circuits that are used to generate the control signals for loading the MPCR (MPCREN signal), loading the AMPCR from the MPCR (AM←MCA signal), and selecting the inputs to the Incrementer Register are controlled by nanobits N11 through N16 and Successor Control signals SC/ and SC. The following list provides the nanobit code, the Successor Control (SC) used, and the Successor function for the MPAD Controls:

Nanobits Used If SC=1:				Nanobits Used If SC=0:		
11	12	13	Successor Function	14	15	16
0	0	0	WAIT	0	0	0
0	0	1	STEP	0	0	1
0	1	0	SAVE	0	1	0
0	1	1	SKIP	0	1	1
1	0	0	EXEC	1	0	0
1	0	1	JUMP	1	0	1
1	1	0	CALL	1	1	0
1	1	1	RETN	1	1	1

Table II-4 indicates the contents of the Microprogram Count Register (MPCR), Alternate Microprogram Count Register (AMPCR), and Incrementer Register (INCR) when the specified Successor function is executed. The logic level of the various control signals is also specified to perform the applicable Successor function and Type II microinstruction.

NOTE

An A in any column of Table II-4 indicates the AMPCR. An I indicates the INCR, an M indicates the MPCR, and an X indicates an insignificant condition.

The following logical equations are given for the MPAD Control functions listed in Table II-4:

$$\overline{MPLUS1} = [SC \cdot \overline{N11}(N12 + \overline{N13})] + [\overline{SC} \cdot \overline{N14}(\overline{N15} + \overline{N16})] + TYPE2$$

$$\overline{APLUS1} = [SC \cdot N11(\overline{N12} + \overline{N13})] + [\overline{SC} \cdot N14(\overline{N15} + \overline{N16})]$$

$$MPLUS2 = [(SC \cdot \overline{N11} \cdot N12 \cdot N13)] + [(\overline{SC} \cdot \overline{N14} \cdot N15 \cdot N16)]$$

$$APLUS2 = [(SC \cdot N11 \cdot N12 \cdot N13)] + [(\overline{SC} \cdot N14 \cdot N15 \cdot N16)]$$

$$\overline{MPCREN} = [SC \cdot (N12 + N13)] + [\overline{SC} \cdot (N15 + N16) \cdot \overline{INHSP}]$$

TABLE II-4. MPAD CONTROL FUNCTIONS

Register or Control	Successor Function and Type II Microinstruction										
	WAIT	STEP	SAVE	SKIP	JUMP	EXEC	CALL	RETN	TYPE II STEP	TYPE II JUMP	TYPE II CALL
MPCR	M	M+1	M+1	M+2	A+1	M	A+1	A+2	M+1	MPM+1	MPM+1
AMPCR	A	A	M	A	A	A	M	A	A	A	M
INCR	I	M+1	M+1	M+2	A+1	A+1	A+1	A+2	M+1	MPM+1	MPM+1
MPLUS1	X	1	1	0	0	0	0	0	1	1	1
APLUS1	X	0	0	0	1	1	1	0	0	0	0
MPLUS2	X	0	0	1	0	0	0	0	0	0	0
APLUS2	X	0	0	0	0	0	0	1	0	0	0
MPCREN	0	1	1	1	1	0	1	1	1	1	1
INCREN	0	1	1	1	1	1	1	1	1	1	1
AM MC	0	0	1	0	0	0	1	0	0	0	1
3SLKI	0	0	0	0	0	0	0	0	1	1	1
BORC	0	0	0	0	0	0	0	0	0	1	1
DCALL	0	0	0	0	0	0	0	0	0	0	1

INCREN = [SC·(N11 + N12 + N13) + $\overline{SC}$·(N14 + N15 + N16)] · $\overline{INHSP}$

AM←MCA = [SC·(N12·$\overline{N13}$)] + [$\overline{SC}$·(N15·$\overline{N16}$)] + DCALL

3CLKI = TYPE2 + $\overline{SC}$·N06

TYPE2 = $\overline{MPM1}$ + $\overline{MPM2}$ + $\overline{MPM3}$ + $\overline{MPM4}$ + FORT2 + SS + FORCE STEP + CLEAR

BORC = DCALL + ($\overline{MPM1}$·MPM2·$\overline{FORT2}$·$\overline{SS}$)

DCALL = MPM1·$\overline{MPM2}$·$\overline{FORT2}$·$\overline{SS}$

MPLUS1 and MPLUS2 are the transfer MPCR to the Incrementer signals. When at a high level, the MPLUS1 or MPLUS2 signal indicates an increment of +1 or +2. APLUS1 and APLUS2 transfer the AMPCR to the Incrementer. When at a high level, the APLUS1 or APLUS2 signals indicate an increment of +1 or +2. MPCREN is the MPCR strobe enable signal, which causes the MPCR to store Incrementer outputs. INCREN is the Incrementer Register (INCR) strobe enable signal, which causes the INCR to store inputs from the Incrementer select gates. The input INHSP inhibit step) holds the Incrementer Register and MPCR during DPM operations and during MEM Read cycles for Load (LI) operations. AM MCA is the transfer MPCR-to-AMPCR signal, which is sent to the AMPCR Input Select gates and clock gates inputs of the AMPCR. 3CLKI is the phase 3 clock inhibit signal which is used by the external memory control on the EO card, the phase 3 clock circuits on the CG card, the AMPCR clock gates on the MU1-1 through MU1-4 cards, and the Shift Control Register input circuits of the CU2 card. The inputs used to generate the phase 3 clock inhibit signal (3CLKI) are: SC·N06 + TYPE2. Signal SC/ is the Successor Control signal from the Condition Control circuits on the CU1 card which indicates that the selected condition was not met. Signal N06 is a nanobit from the Nanomemory that is used to control the phase 3 modifier functions as follows:

Nanobit N06	Phase 3 Modifier (Logic Unit Condition)
0	Perform phase 3 operations unconditionally.
1	Perform phase 3 operations if SC=1.

The TYPE2 signal is used to indicate that a Type II microinstruction is executed. The TYPE2 signal is sent to the Condition Control circuit of the CU1 card, the Memory or Device control circuit of the EO card, the MPLUS1 circuit of the MU4 card, and the Nano Parity Check circuit on the LI3 card. BORC is the Type II branch or call signal used to select MPM as an input to the M+1 incrementer. When at a high level, MPM+1 is sent to the Incrementer Register. DCALL is the Type II direct call signal used to allow the AMPCR to be replaced by MPCR.

There are eight Successor functions, and any one of these functions can be used whenever a Successor is specified in the microinstruction. (Refer to Table II-4.) A WAIT Successor causes the present instruction, whose address is in the Microprogram Count Register (MPCR), to be repeated. The contents of the MPCR, the Alternate Microprogram Count Register (AMPCR), and the Incrementer Register (INCR) are not changed at this time.

A STEP Successor causes the next instruction in sequence to be executed. The contents of the MPCR are incremented by 1 (MPCR+1), but the contents of the AMPCR remain unchanged. The contents of the INCR contain MPCR+1. The absence of a Successor in a microinstruction causes a STEP to be performed.

A SAVE Successor causes the next instruction in sequence to be executed and the current Microprogram Memory (MPM) address to be saved in the AMPCR. This Successor is used to SAVE an address.

A SKIP Successor causes the next instruction in sequence to be skipped and the next instruction following it to be executed. The contents of the MPCR are incremented by 2 (MPCR+2), and the contents of the AMPCR are not changed. The contents of the INCR contain MPCR+2.

A JUMP Successor causes a branch in the sequence of instructions by transferring control to the AMPCR. The next instruction to be executed is the instruction whose address is indicated by the contents of the AMPCR+1. The contents of the MPCR are replaced with the contents of the AMPCR+1. The AMPCR remains unchanged, and the contents of the INCR contain AMPCR+1.

An EXEC Successor causes the execution of one non-sequential instruction whose address is AMPCR+1. The contents of both the MPCR and AMPCR are not changed, but control for the sequencing of instructions remains with the MPCR. The contents of INCR contain AMPCR+1.

A CALL Successor causes a branch in the sequencing of instructions by transferring control to the AMPCR. The next instruction to be executed is the instruction whose address is indicated by the contents of AMPCR+1. The contents of the MPCR are replaced with the contents of AMPCR+1. The contents of the AMPCR are replaced with the contents of the MPCR, and the contents of the INCR are AMPCR+1.

A RETN Successor causes a branch in the sequencing of instructions by transferring control to the AMPCR. The next instruction to be executed is the instruction whose address is indicated by the contents of AMPCR+2. The contents of the MPCR are replaced with the contents of AMPCR+2. The AMPCR remains unchanged, and the contents of the INCR contain AMPCR+2.

For a TYPE II STEP instruction, the contents of the MPCR and INCR contain MPCR+1, and the contents of the

AMPCR remain unchanged.

A TYPE II JUMP instruction causes a branch in the sequence of instructions by transferring control to the Type II microcode least significant 14-bits. The next instruction to be executed in the instruction whose address is indicated by the contents of MPM (3 through 16) plus 1. The contents of MPCR are replaced with the contents of MPM (3 through 16) plus 1. The AMPCR remains unchanged, and the contents of the INCR contain MPM (3 through 16) plus 1.

A TYPE II CALL instruction causes a branch in the sequencing of instructions by transferring control to the Type II microcode 14 least significant bits. The next instruction to be executed is the instruction whose address is indicated by the contents of MPM (3 through 16) plus 1. The contents of MPCR are replaced with the contents MPM (3 through 16) plus 1. The contents of AMPCR are replaced with the contents of MPCR, and the contents of INCR are MPM (3 through 16) plus 1.

Functionally, the Microprogram Address (MPAD) is determined by what is contained in the MPAD Controls at the start of phase 1. Refer to the information contained under the Microinstruction Phasing and Microprogram Instruction Sequencing headings for detailed information pertinent to phase 1. Either the true successor (SC=1) with the values contained in nanobits N11, N12, and N13, or the false successor (SC=0) with the values contained in nanobits N14, N15, and N16, is loaded into the MPAD Controls. This is determined by the value of the Successor Control (SC) functions from the Condition Control circuits of the CU1 card during phase 1.

The MPAD Controls are also used to decode control bits MPM1 through MPM4 from the Microprogram Memory (MPM). These MPM control bits are used to determine the destination register or registers for the remaining bits in an MPM word for either Type I or Type II instructions. The destination register can be the Shift Amount Register (SAR). Literal register (LIT). Alternate Microprogram Count Register (AMPCR). Microprogram Count Register (MPCR), Incrementer Register (INCR) or both the SAR and LIT for a Type II instruction. See Figure II-18 for information concerning MPM control bits. MPM destination bits, Type of microinstruction, and functional operation.

The SAR←MP signal transfers Microprogram Memory (MPM) data to the Shift Amount Register (SAR) of the SAR Control circuits on the CU2 card. This signal is true when an MPM word contains a "1100" or "1101" in the first four MPM control bits.

The following list specifies the logical equations that are used to generate the various MPAD Control functions

MICROCONTROLS

	MPM BIT LOCATION																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	INSTR. TYPE
HEX. CODE→	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	
AMPCR =	0	0	LOAD AMPCR														II
MPCR =(Jump)	0	1	LOAD INCR & MPCR +1														II
CPCR =(Call)	1	0	AMPCR REPLACED BY MPCR LOAD INCR & MPCR +1														II
SAR =, LIT =	1	1	0	0	LOAD SAR				LOAD LIT								II
SAR =	1	1	0	1	LOAD SAR				∅ ---------- ∅								II
LIT =	1	1	1	0	∅ ----- ∅				LOAD LIT								II
ALL OTHERS	1	1	1	1	@ NANO ADDRESS												I

B7MPL RESERVED WORDS

NOTE: ∅ = Unused

@ = This bit is not used for addressing.

Fig. II-18

which require MPM inputs:

$SAR \leftarrow MP = MPM1 \cdot MPM2 \cdot \overline{MPM3}$

$AM \leftarrow MP = MPM1 \cdot \overline{MPM2}$

$LIT \leftarrow MP = MPM4 \cdot MPM1 \cdot MPM2$

$TYPE2 = \overline{MPM1} + \overline{MPM2} + \overline{MPM3} + \overline{MPM4} + 3SS + FORT2 + FORCE\ STEP$

$BORC = DCALL + (\overline{MPM1} \cdot MPM2 \cdot \overline{FTYP2})$

$DCALL = MPM1 \cdot \overline{MPM2} \cdot \overline{FTYP2}$

The AM←MP signal transfers MPM data into the Alternate Microprogram Count Register (AMPCR) through the AMPCR Input Select gates. This signal is sent to the AMPCR clock gates on the MU1-1 through MU1-4 cards. This signal is true when an MPM word contains 00 in the first two MPM control bits.

The LIT←MP signal transfers MPM data into the Literal Register (LIT). This signal is sent to the LIT strobe enable gates on the MU1-2 and MU1-3 cards. This signal is true when an MPM word contains 1110 in the first four MPM control bits or a 1100 in the first four MPM control bits.

The TYPE2 signal indicates that a Type II microinstruction is to be executed. The Type 2 signal is sent to the Condition Control circuit of the CU1 card and the Memory or Device control circuits of the EO card. This signal is true when an MPM word contains a 0 in any one of the first four MPM control bits or when the Sequential Mode signal (SS), the Force Type II operation signal (FORT2), or the output from the Force Step flip-flop is present. The Sequential Mode signal (SS) is from the MTR/MEM switch on Field Engineering card FE3. When at a low level, this signal causes all Microprogram instructions to be executed as Type II microinstructions to force sequential stepping through the entire Microprogram Memory (MPM). The Force Type II operation signal (FORT2) is from the data cycle of the external operation card of which also receives a force step signal from the load interface cards. A Load Interface card is used when the Microprogram Memory (MPM) is a read/write memory (RWM). The Load Interface card acts as the interface between an input device, such as a Card Reader, and the read/write memory (RWM) is used when loading memory. The Force Step flip-flop output is generated from the FORCE STEP push button inputs on FE3. When signal STNAR goes low, a single Force Type II pulse is generated. When signal STNA goes low, the circuits are reset to permit the generation of another Force Step pulse. The BORC (branch or call) signal selects MPM as input to incrementer. DCALL gates MPCR to AMPCR. FTYP2 is generated as follows: FTYP2 = FORT2 · SS

Memory/Device Address Section

The memory/device address section of the Memory Control Unit is comprised of the following registers and associated gate circuits: the Memory Address Register (MAR), Base Register 1 (BR1), Base Register 2 (BR2), and Output Select gates. MAR, BR1, and BR2 are located on the MU4 and MU5 cards. (See Figure II-13.)

The Memory Address Register is an eight-bit register which contains the least significant eight-bits of the Memory/Device address. The outputs from this register are concatenated onto the least significant end of either the outputs from Base Register 1 or Base Register 2 to form the complete memory/device address.

MAR may be loaded from either the least significant byte (eight LSB's) of the Barrel Switch (BSW) on the LU1 card or the Literal register (LIT) on the MU1-2 and MU1-3 cards. The outputs from BSW or LIT are sent to the MAR/CTR input select gates.

The eight LSB's from the Barrel Switch are enabled as inputs to the MAR by enable control signal DN46. When this signal is false, the Literal Register inputs (LIT1 through LIT8) are enabled as inputs to the MAR. The enable control signal DN46, which is generated by the Control Register on the MU5 card, corresponds to nanobit N46 from the Nanomemory. The strobe enable signal DN45, which is also generated by the Control Register on the MU5 card, is used as an input to a NAND gate circuit along with the phase 3 clock signal (3CLKA). The output of this NAND gate circuit is applied to the clock (CP) inputs of the MAR flip-flops (MAR1 through MAR8). Signal DN45 corresponds to nanobit N45 from the Nanomemory.

Nanobits N45 and N46 are used to control Memory Address Register input selection as follows:

Nanobits 45	46	MAR Input Selection
0	—	No change in the MAR.
1	0	Literal register (LIT) inputs (LIT1 through LIT8) are sent to the MAR (LMAR).
1	1	Eight least significant bits (least significant byte) of the Barrel Switch output are sent to the MAR.

The Output Select signals (OS9 through OS16) from the Memory Address Register (MAR) are used as inputs to the least significant bits of the Y-Select gates on the LU3 and LU4 cards. OS9 through OS16 are concatenated with OS1 through OS8 of the Base Register (BR1 or BR2) and are used as inputs to all 16-bits of the Y-Select gates on the LU3 and LU4 cards. The BRn and MAR Output Select signals (OS1 through OS16) also provide address information to Data/Program Memory through the Shared Memory cards (SM1 through 3).

Base Register 1 is an eight-bit register which contains the base address of a 256-word block of data or a device address. The output from BR1 is applied to the Output Select gates, which generate Output Select signals OS1 through OS8. These Output Select bits are concatenated with the Output Select bits from the Memory Address Register (MAR) to form an absolute memory or device address that is sent to the 16-bits of the Y-Select gates on the LU3 and LU4 cards. Output Select signals from BR1 are also sent to the Port Selector (PS1 cards). (See Figure II-13.) The inputs to BR1 are from the most significant eight-bits of the Barrel Switch (BSW) output.

These Barrel Switch (BSW) outputs are applied directly to the parallel data (P) inputs of the BR1 flip-flops and BR2 flip-flops. The strobe enable signal DN43, which is generated by the Control Register of the Memory Control Unit on the MU2 card, is an input to a NAND gate circuit along with the phase 3 clock signal (3CLKA). The output of this NAND gate is sent to the clock (CP) inputs of the BR1 flip-flops. Strobe enable signal DN43 corresponds to nanobit N43 from the Nanomemory. Nanobit N43 is used as the control for Base Register 1 input selection as follows:

Nanobit N43	Base Register 1 Input Selection
0	No change in the contents of Base Register 1.
1	Next eight LSB's to the least significant byte of the Barrel Switch (BSW) are sent to BR1.

Base Register 2 (BR2) is an eight-bit register which usually contains the base address of a 256-word block of data or a device address. The output from the BR2 is applied to the Output Select gates, which generate Output Select signals (OS1 through OS8). These Output Select bits are concatenated with the Output Select bits from the Memory Address Register (MAR) to form an absolute memory or device address that is sent to the 16-bits of the Y-Select gates on the LU3 and LU4 cards. Output Select signals from BR2 are also sent to the Port Selector (PS1 cards). (See Figure II-13.) Inputs to BR2 are from the eight-bits of the most significant byte of the Barrel Switch output.

These Barrel Switch outputs are applied directly to the Parallel data (P) inputs of the BR2 and BR1 flip-flops. The strobe enable signal DN44, which is generated by the Control Register of the Memory Control unit on the MU2 card, is an input to a NAND gate circuit along with the phase 3 clock signal (3CLKA). The output of this NAND gate is sent to the clock (CP) inputs of the BR2 flip-flops. Strobe enable signal DN44 corresponds to nanobit N44 from the Nanomemory. Nanobit N44 is used as the control for Base Register 2 input selection as follows:

Nanobit N44	Base Register 2 Input Selection
0	No change in the contents of Base Register 2.
1	The eight-bits of the most significant byte of the Barrel Switch (BSW) are sent to BR2.

The Output Select (OS) gates, which are located on the MU4 and MU5 cards, are used for selecting data memory addresses or device addresses from either Base Register 1 or Base Register 2. The outputs from these Output Select gates are concatenated with the Output Select bits from the Memory Address Register to form an absolute data memory (16-bit) or device (8-bit) address that can also be sent to the Y-Select gates on the LU3 and LU4 cards. The output from BR1 and MAR can be represented as BR1/MAR or MAR1. Likewise, the output from BR2 and MAR can be represented as BR2/MAR or MAR2. The Output Select signal (OSEL), generated by the EO card, is used to transfer BR2 outputs through the OS gates.

shown in Figure II-19.

CTR is located on the MU5 card and LIT is located on the MU1-2 and MU1-3 cards. (See Figure II-17.) The eight-bits of the Counter (CTR provide the most-significant byte of the Z Register and the eight-bits from the Literal Register (LIT) provide the least significant byte of the Z Register as indicated in Figure II-19.

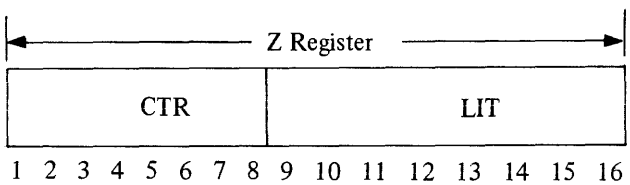


Fig. II-19

The Counter (CTR), which is eight-bits in length, is used for loop control and various count functions. CTR is comprised of two UP Counter modules (1447 3771) and can be loaded from either the Literal register or the least significant byte of the Barrel Switch by means of the MAR/CTR input select gate circuits. The CTR output signals (CTR1 through CTR8) are used as inputs to the most significant bits (MSB's) of the X-Select gates on the LU2 cards and the Y-Select gates on the LU3 and LU4 cards. The CTR can also be incremented by ONE. When the CTR overflows (CTR is incremented to an all ONES condition, which causes an all ZERO condition at the next clock pulse), the Counter Overflow bit (COV) is set in the Condition Register on the CU1 card. The Counter Overflow (COV) bit is reset by either testing or loading the CTR.

Enable signals DN47 and DN48 are used as control signals for the CTR most-significant bit and least-significant bit modules. Signal DN47 enables the CTR to increment if

signal DN48 is false. DN48 enables the transfer of data to the CTR and resets the Counter Overflow (COV) flip-flop in the Condition Register of the CU1 card. The transfer of data (LIT or BSW outputs) to CTR will override increment CTR controls (signal DN47), if these conditions occur simultaneously. Enable signal DN46 is used to allow the Barrel Switch inputs or Literal Register inputs to be transferred through the MAR/CTR input select gates. When this signal is at a high level, it enables the transfer of the Barrel Switch inputs through the select gates. Likewise, when this signal is at a low level, the transfer of Literal Register inputs through the MAR/CTR input select gates occurs.

The DN46, DN47, and DN48 signals, which are outputs from the Control Register of the MU5 card, correspond to nanobit signals N46, N47, and N48 from the Nanomemory. N46, N47, and N48 are used to control CTR input selection as follows:

Nanobit 46	47	48	Counter (CTR) Input Selection
-	0	0	No change in the contents of the CTR.
0	0	1	Literal register outputs (LIT) are sent to the Counter (LCTR).
1	0	1	Least significant byte of Barrel Switch outputs (BSW) are sent to the Counter (CTR).
-	1	0	Increment Counter (Modulo 256), (INC)

The Literal register (LIT) is an eight-bit register which receives data inputs from the Microprogram Memory (MPM). MPM outputs MPM9 through MPM16 are sent to the parallel (P) inputs of the Literal register flip-flops. The clock (CP) input of the LIT flip-flops are enabled by the output from a two-input NAND gate. These inputs are the system clock (SCLKF) and the transfer signal (LIT MP). LIT MP is the transfer MPM data-to-LIT signal, which is generated by the MPAD Controls on the MU2 card. This signal enables the strobe pulse to the LIT register.

Control Register Section

The Control Register, which is located in the Memory Control Unit on the MU2, MU3, MU4, and MU5 cards, is used to store the nanomemory control signals that are not used in phase 1 operations. Figure II-20 is a functional block diagram of the Control Register and associated logic circuits of the Memory Control Unit cards.

Some of the nanobit control signals from the Nanomemory are decoded before being strobed into the Control Register. Nanobit signals N17 through N19 and N22 are applied to the inputs of decoded gate circuits instead of being applied directly to the data inputs of the applicable Control Register flip-flops. The following nanobit signals are applied directly to the data input of the corresponding Control Register flip-flops: N20 through N31 and N34 through N48.

Nanobit control signals N17 through N19 are used in the generation of the ACTL1, ACTL2, NQE1, NQE2, and NQE3 signals. The ACTL signals are used to select the inputs to the X-Select gates on the LU2 cards. The NQE signals are used as enable signals to the respective portion of the X-Select gates. NQE1 is used to enable inputs to the most-significant bit portion of the X-Select gates, and the NQE3 signal is used to enable inputs to the least-significant bit portion of the X-Select gates. The NQE signals are used to inhibit unwanted bits during Literal register output. Counter output, or External (EXT) bit transfer through the X-Select gates of the LU2 cards.

Nanobit signals N20 and N21 are used by the Control Register to generate nanobit decode signals NB20 and NB21. NB20 and NB21 control are sent to the most significant bit of the Y-Select gates of the LU3 and LU4 cards. Nanobit control signal NB20---1 is connected to ground on all LU3 and LU4 cards, except the LU3-1 card that contains the MSB of the Y-Select gates. The nanobit control signal NB21 is also connected to the LU3-1 card that contains the MSB to the Y-Select gates.

Nanobit signals N22 through N24 are used in the generation of the ENB1, ENB2, ENB3, SELBA, and SELBB control signals. ENB enable signals are used to select inputs to the Y-Select gates on the LU3 and LU4 cards. ENB1 controls the most-significant bits, and ENB3 controls the least-significant bits. SELB control signals are used to select various inputs to the Y-Select gates on the LU3 and LU4 cards.

Nanobit signals N25 and N26 are used in the generation of decoded nanobit control signals NB25 and NB26. Nanobit control signal NB25, which is generated by the Control Register on the MU3 card, is used to control the least-significant bit of the Y-Select gates on the LU3 and LU4 cards. This signal is connected to ground on all LU3 and LU4 cards, except the LU4-2 card that contains the LSB of the Y-Select gates. Nanobit control signal NB26, which is also generated by the Control Register on the MU3 card, is also used to control the LSB of the Y-Select gates on the LU4-2 card.

Nanobit signals N27 through N31 are sent to the data input of the respective Control Register flip-flops NB27 through NB31 on the MU3 card. The outputs from these flip-flops are applied to decode output gates, which are used to generate the Adder select control signals (AS0, AS1, AS2, and AS3), CArry Input signal (CIN), Inhibit 8-bit Carry signal (INH8), and Adder Mode signal (AMODE) that are sent to the Arithmetic/Logic Unit on the LU2-1 through LU2-4 cards. The four Adder control signals (AS0 through AS3) are used in conjunction with the

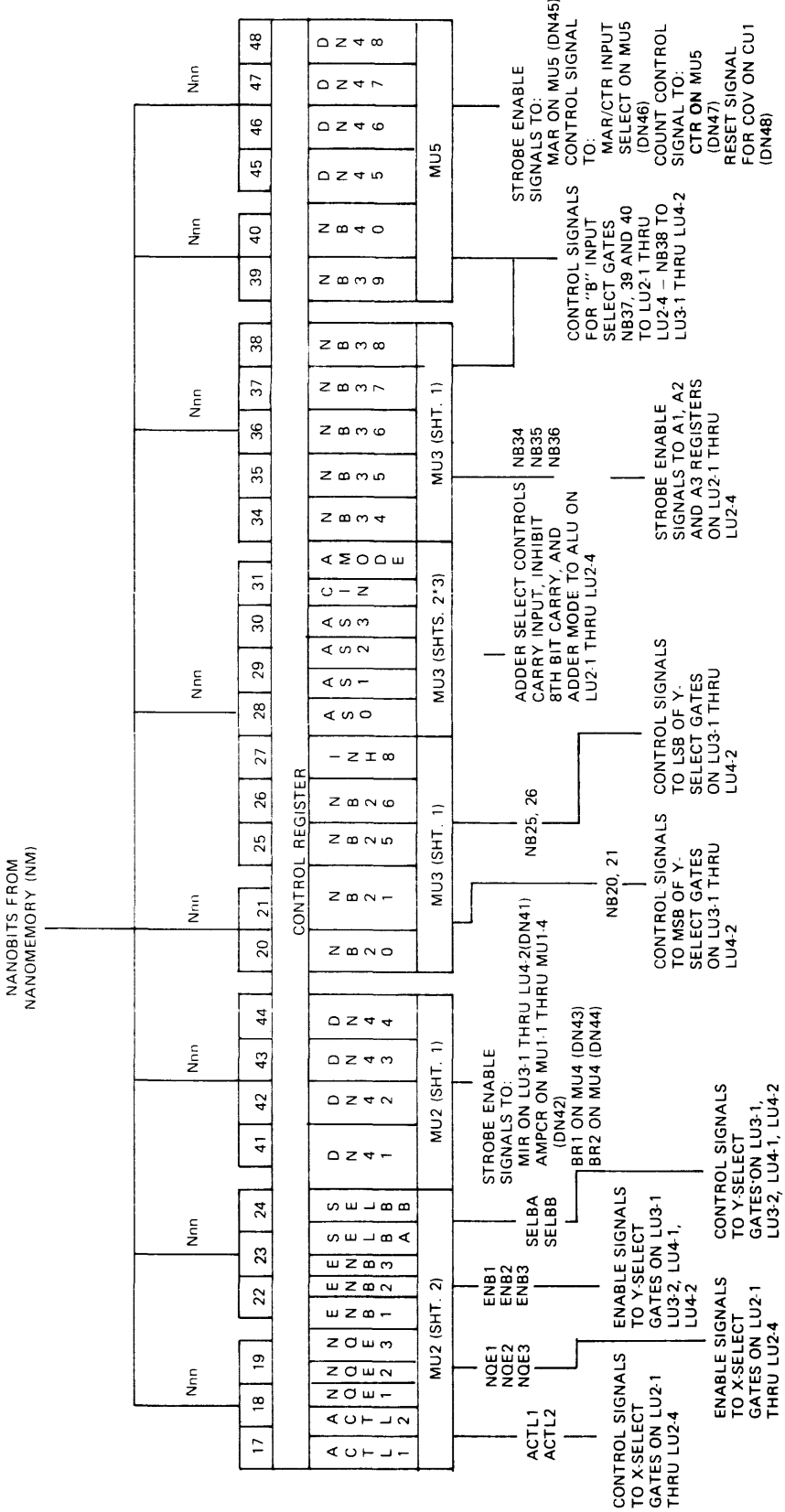


Fig. II-20. CONTROL REGISTER AND ASSOC. LOGIC OF MEMORY CONTROL UNIT, BLOCK DIAGRAM

AMODE signal to select the proper arithmetic or logic operation of the Arithmetic/Logic Unit modules (1447 3730) on the LU2 cards. Carry Input signal (CIN) is sent to the least significant bit of the Adder for arithmetic operations "X+Y+1 or X-Y". The Inhibit 8-bit carry signal (INH8), when false, is used to inhibit the carry out of the least-significant eight-bit group of the Adder.

Nanobit signals N34 through N36 are sent to the data input of the respective Control Register flip-flops NB34 through NB36 on the MU3 card. The outputs from these flip-flops are sent to the A Register on the LU2 cards. Signal N34 is used to enable the strobe pulse to the A1 Register. Signal N35 is used to enable the strobe pulse to the A2 Register, and signal N36 is used to enable the strobe pulse to the A3 Register on the LU2 cards.

Nanobit signals N37 through N40 are sent to the respective Control Register flip-flops NB37 through NB40 on the MU3 and MU5 cards. The outputs from these flip-flops are sent to the B Input Control and Select gates of the B Register on the LU2-1, LU2-2, LU2-4, LU3-1, LU3-2, LU4-1 and LU4-2 cards. Signals NB37, NB38, NB39, and NB40 are used as inputs to the B Input Select gates to control B Register input selection. Signals NB38 and NB40 are also sent to the Memory Control circuits on the EO card to determine when a BEX operation (data from an external source is placed in the B Register) is to be performed.

Nanobit signals N41 through N48 are sent to the data (P) input, of the respective Control Register flip-flops on the MU2 and MU5 cards. The outputs from these flip-flops (DN41 through DN48) are used to enable the strobe pulses to various registers to control input selection. Signal DN41 is used to enable the strobe pulse to the Memory Information Register on the LU3-1 through LU4-2 cards for the MIR input selection. Signal DN42 is used to enable the strobe pulse to the Alternate Microprogram Count Register (AMPCR) on the MU1-1 through MU1-4 cards for AMPCR input selection. Signal DN43 is used to enable the strobe pulse to Base Register 1 on the MU4 card for BR1 input selection. Signal DN44 is used to enable the strobe pulse to Base Register 2 on the MU4 card for BR2 input selection.

Nanobit control signal DN45 is used to enable the strobe pulse to the Memory Address Register on the MU5 card for MAR input selection. Nanobit control signal DN46 is used to enable Barrel Switch outputs to transfer through the MAR/CTR selection gates. When this signal is false, Literal Register outputs are permitted to transfer through the MAR/CTR selection gates on the MU5 card. Nanobit control signal NB47 is used to enable CTR to increment if signal DN48 is false. Signal DN48 is used to enable the transfer of data to CTR on the MU5 card and also to reset the Counter Overflow (COV) flip-flop in the Condition Register of the Condition Control circuits on the CU1 card. Signals DN45 and DN46 are used to control MAR input selection, and signals DN46, DN47, and DN48 are used to control Counter (CTR) input selection.

There are five remaining Control Register flip-flops on the Control Unit card (CU2) and four control flip-flops on the External Operation Control card (EO). Refer to the functional description of the Shift Control Register and associated control circuits on the CU2 card, or the Control Register and associated control circuits of the EO card.

EXTERNAL OPERATION CONTROL (EO)

External operation control is divided into: (a) the Memory and Device Control and (b) the Memory Hardware Error Control. (See Figure II-21.) The memory and Device Control consists of the Control Register and its input/output gating that decodes nanobit signals from nanomemory which are used to control memory/device operations.

Memory and Device Control

Nanobit signals N51 through N54 from the Nanomemory are sent either directly to the data (D) input of the respective Control Register flip-flop or to the memory/device input control gate circuits. The function of signals are as follows:

Nanobits				Memory/Device Operation Specified
51	52	53	54	
0	0	0	0	No change
0	0	0	1	– – –
0	0	1	0	Memory Read 1 (MR1): Read the contents from memory at the memory address specified by Base Register 1 and the Memory Address Register (BR1/MAR).
0	0	1	1	Memory Read 2 (MR2): Read the contents from memory at the memory address specified by Base Register 2 and the Memory Address Register (BR2/MAR).
0	1	0	0	Device Load (DLD): Used in system configurations that use a con card. Only affects control register 51.
0	1	1	0	Memory Write 1 (MW1): Write the contents of the Memory Information Register (MIR) into the memory address specified by Base Register 1 and the Memory Address Register (BR1/MAR).

Functional Detail

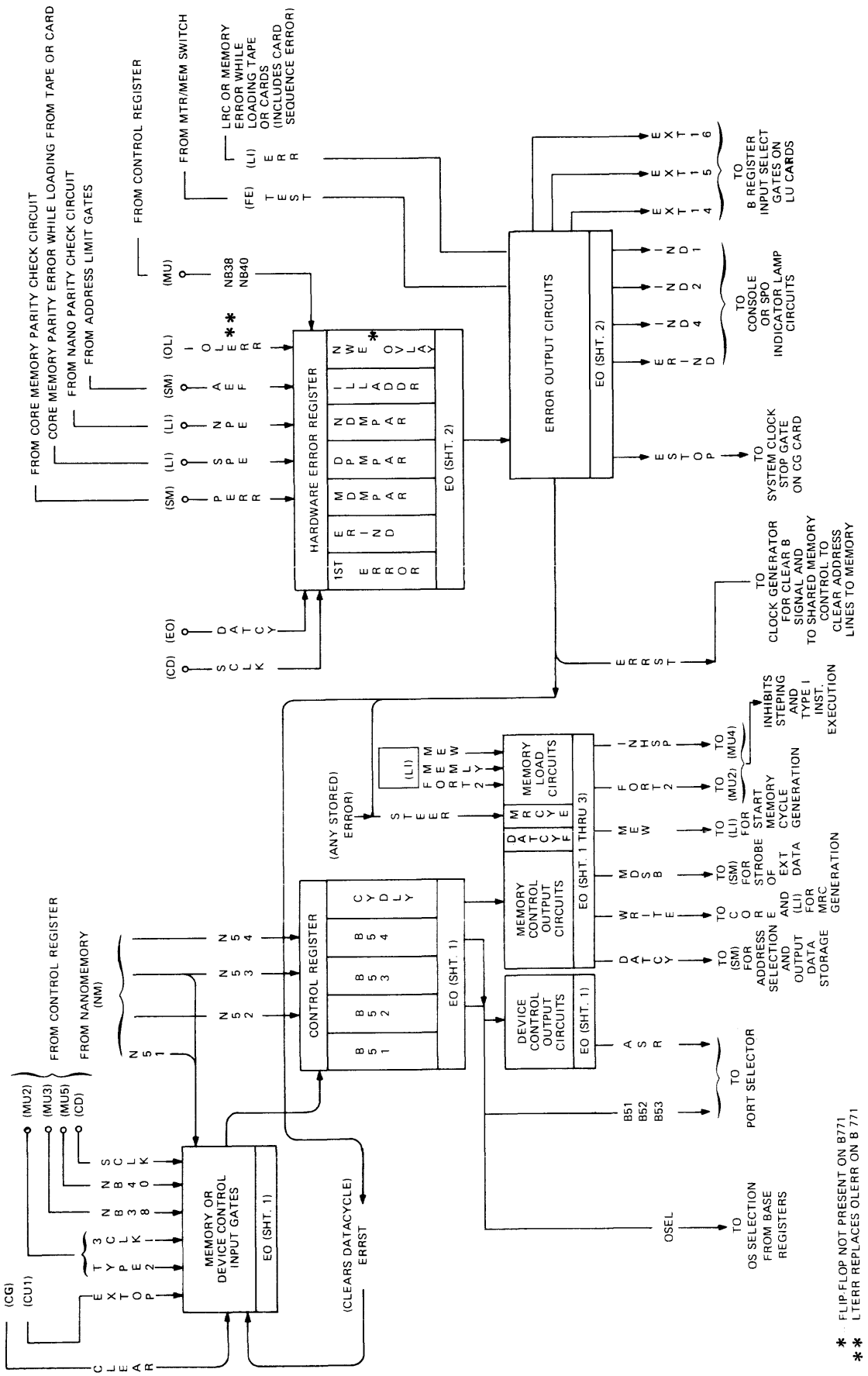


Fig. II-21. EXTERNAL OPERATION (EO) CARD, BLOCK DIAGRAM

0	1	1	1	Memory Write 2 (MW2): Write the contents of the Memory Information Register (MIR) into the memory address specified by Base Register 2 and the Memory Address Register (BR2/MAR).
1	0	0	0	ASR: Status Request for highest priority unselected device.* Select BR1 for device or memory address lines.
1	0	0	1	ASE: Select BR2 for device or memory address lines.*
1	0	1	0	Device Read 1 (DR1): Read from device specified by device address in Base Register 1.
1	0	1	1	Device Read 2 (DR2): Read from device specified by device address in Base Register 2.
1	1	1	0	Device Write 1 (DW1): Write the contents of the Memory Information Register (MIR) to the device specified by the device address in Base Register 1.
1	1	1	1	Device Write 2 (DW2): Write the contents of the Memory Information Register to the device specified by the device address in Base Register 2.

Note: * Indicates no change in port selector address.

Simultaneous access to both MPM and S-Level Memory is not allowed in B 711 system because they share the same physical memory. The B 711 implementation is such that microinstructions are read from MPM under control of the MCU, whereas S-Level Memory can be accessed only upon the execution of an instruction from nanoprogram memory specifying a memory read or write operation. Whenever an S-Level Memory operation is called for, the following sequence of events occur: (a) the phase 1 of the instruction is completed, including the selection of memory/external operation controls; (b) the accessing of S-Level Memory is delayed during the next clock period, allowing the next instruction to be read from MPM and its phase 1 to be executed; (c) at the next (second) clock the S-Level Memory is cycled and the read or write operation is performed.

During the delay noted in (b), the memory address register or the memory information register contents may be changed if destination selection is completed before the memory cycle occurs. If the next instruction is a type I which consists of two phases, any changes will occur before the memory is cycled because the destination selection (Phase 3) will have been completed. If, however, the next instruction is a Type II or a Type I in which a condition is not met, no change occurs until after the memory cycle because an extended Phase 3 condition delays the destination register selection.

During the time the S-Level Memory Cycle is in progress, all logic unit operations are suspended and an extended Phase 3 condition is forced on the in-process instruction. No instruction executes a Phase 1 operation during this time because MPM cannot be accessed. Following the cycling of S-Level Memory, execution of instructions from MPM resumes.

There are seven flip-flops in the EO memory/device control circuits: B51 through B54, CYDLY (Memory Cycle Delay), MRCYE (Memory Read Cycle), and DATCYF (Data Cycle). The outputs from the B51 through B54 flip-flops correspond to the nanobit signals N51 through N54 and their complements. The B51 through B53 and the OSEL (Output Select) signals are used to perform the various Memory/Device Operations discussed in the previous text concerning nanobit control of memory/device operations.

Output signal DATCY is used to indicate that a DPM memory operation is in process and that a "BEX" operation (data from the External Data Bus is placed in the B Register), or a subsequent device operation has not occurred. DATCY is sent to the Shared Memory Control (SMC) to gate the address to Data/Program Memory, and to allow the memory output data to be clocked into the data register. The MRCYE and CYDLY flip-flops are set by the following External Operation Equations: $CYDLY = EXTOP \cdot \overline{N51} \cdot N53 \cdot \overline{TYPE2} \cdot SCLK$, $MRCYE = CYDLY \cdot \overline{B52} \cdot SCLK$. The MRCYE flip-flop is reset by a "BEX" operation (for read), or the occurrence of a second External Operation as indicated by Figure II-22.

The RDC output signal on the Condition Control circuits of the CU card is always present. The Memory Data Output Strobe (MDSB signal) is sent to Data/Program Memory. When the MDSB signal is at a high state, this allows the data memory to gate data to the External Data Bus. This signal remains at a high state as long as a DPM Memory Read Operation is present.

The Read/Write output signal (WRITE) is sent to Data/Program Memory. When the WRITE signal is true, it indicates that a Memory Write operation (MW1 or MW2) is to be performed. This signal remains true for Memory Write operations as long as a Memory Operation is present. The inputs to the NAND gate circuit used to generate the WRITE output signal are from the Q output of the B52 flip-flop (indicates the presence of a write condition) and the gated output of the DATCYF flip-flop (indicates a

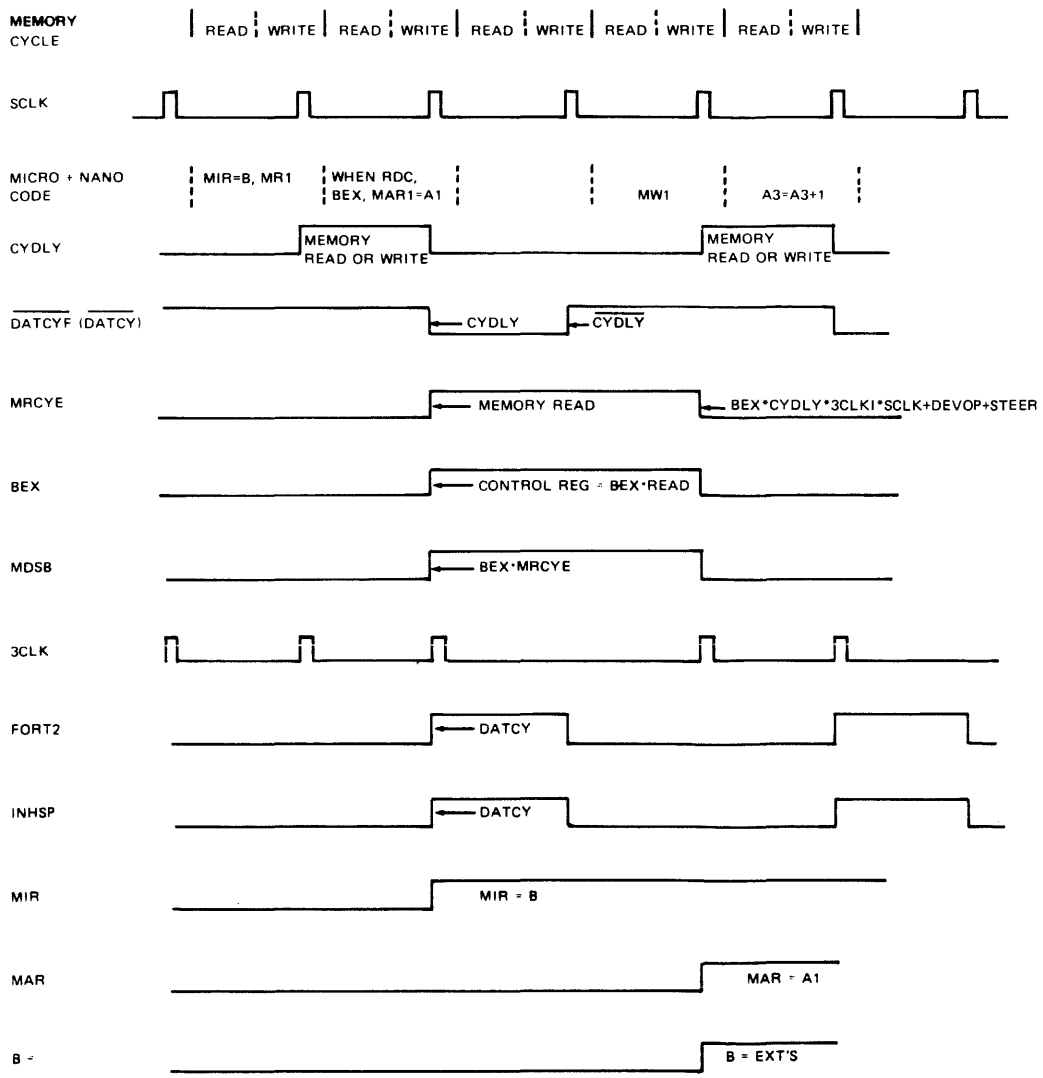


Fig. II-22. MEMORY OPERATIONS CYCLE, TIMING DIAGRAM

Memory Operation in progress).

The Memory Enable Write signal for core memory (MEW) is sent to the loader card to generate start memory cycle (SMC) to core memory. When the $\overline{\text{SMC}}$ signal is at a low state, this causes initiation of a memory cycle.

The input signals FORT2, MEMCY, and MEW to the Memory Control Circuits are from the loader interface cards. FORT2 generates the FORT2 output that forces the MPAD Logic to step, as in the DPM Memory Cycle. MEMCY Signal requests the memory cycles necessary for storing information from Loader Device. MEW selects the Memory Write operation necessary for storing data from Loader Device. Note: Read Cycles would also be needed for parity checking. The output signal INHS) is needed to inhibit the stepping that has been forcedon the MPAD logic for both loader read cycles and DPM operations. (Refer to the loader interface control description.)

The remaining output signal (ASR) from the Device Control circuits of the EO card is used in port select circuits. The Address and Status Request for an unselected device (ASR signal) is sent to a Part Selector (PS1 card). This signal is decoded from nanobits N51 through N54 from the Nanomemory by EO Control Register flip-flops B51 through B54. This signal causes the Port Selector (PS1) to gate the address and direct the status to the External Data Bus of the highest priority DDP that is causing the generation of an IRQ signal.

The ASE function of the EO card sets control register bit-54 and causes the content of BR2 to be placed on the output select (OS) lines. The DLD function of the EO card, leaving the control register unchanged, is used to enable the Configuration Card (CON1) to produce on the EXT's system hardwired configuration data. The following illustrates the possible configuration data:

Ext 1 2 3 4 5 6 7 8 9 10 11	12	13	14	15	16
ZEROS	0=DIL	0=RPG	0=B700	0=FULL DISK	0=CONSOLE
	1=$\overline{\text{DIL}}$	1=$\overline{\text{RPG}}$	1=B770	1=HALF DISK	1=SPO

Memory Hardware Error Control

The memory hardware error control section of the External Operation (EO) card consists of up to seen error flip-flops of the error register and the error output circuits. (See Figure II-21.)

The error conditions of the system are automatically detected by the hardware. When any such error is detected, an error counter is stepped and the error information is placed on the External Bus through the three least significant bits (14 through 16), the memory address lines will be forced to all zero's, allowing entrance to an error recovery routine (fatal error loop). The software can then interrogate the error information on the EXT Bus through the execution of a BEX, (if a Console is used) the left most indicator on the indicator panel will be illuminated (Red) and (in any system configuration) all the DDP's will be reset.

If a second harware-sensed error is encountered, the system clock stops and the appropriate error pattern is displayed on either SPO or CONSOLE indicators. (All previous error indicators are reset.) When the system clear pushbutton is pressed the error counter is reset and the system clock is restarted to allow a retry attempt. If recovery is unsuccessful after repeated retries, the cause of the error must be corrected. Figure II-23 illustrates the timing of the error recovery procedure.

Tables II-5 and II-6 illustrate the actual Console and SPO error indicator combinations and their meanings.

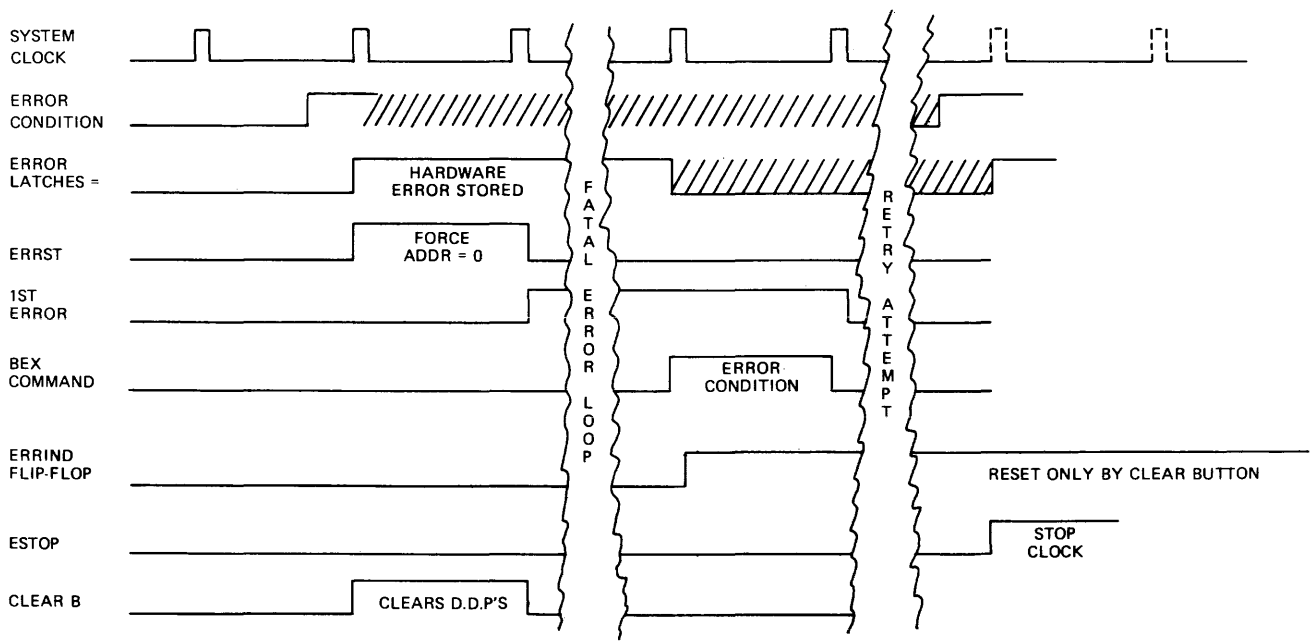


Fig. II-23. FATAL ERROR AND RETRY TIMING

TABLE II-5. CONSOLE INDICATION OF HARDWARE ERRORS

"D" INDICATOR PATTERN	ERROR MESSAGE	DESCRIPTION
80	PPT – Parity	Hardware detected a parity error in paper tape data during the read-in of data from the console memory loader to MPM.
81	MPM – Parity	Hardware detected a parity error in the MPM portion of shared memory while attempting to access a microinstruction, or a parity error was detected in the MPM read-after-write check during loading from the console paper tape reader.
82	DPM – Parity	Hardware detected a parity error in the DPM portion of shared memory while attempting to read or write data memory.
83	NPM – Parity	Hardware detected a parity error in an NPM word while attempting to read a NANO instruction
84	DPM – Over – Limit	Hardware detected a memory address in excess of the memory limit register setting: that is, an attempt was made to read or write outside the physical confines of the memory.

NOTE: Following any hardware error condition, the "system clear" pushbutton must be depressed if an attempt is to be made to re-run the system; otherwise a second hardware error causes the processor clock to stop. In this event, the "0" indicators will display only the second digit of the error pattern, and no error message is printed.

TABLE II-6. STATUS INDICATORS FOR SUPERVISORY PRINTERS

Status	Meaning
0 0 X	Parity error detected in the microprogram memory (MPM).
0 X 0	Parity error detected during the fetching (reading) of a data word from the memory.
0 X X	Parity error detected in a nanoprogram (control) memory word or the program addressed a nonexistent nano word.
X 0 0	Memory address exceeds memory limit register setting.
X 0 X	Error detected during the loading of cards (in "Load" mode). Either card parity error or sequence error.

CLOCK GENERATION AND DISTRIBUTION (CG AND CD)

The Clock and Clear circuits are contained on the Clock Generator (CG) and Clock Driver (CD) cards. The clock circuits consist of the 10-MHz crystal controlled clock oscillator and clock control flip-flops which develop system clock pulses, phase 3 clock pulses, and memory timing. Clock drive buffers are provided for distributing the clock pulses. (See Figure II-24.)

The phase 3 clock pulse (3CLKn) signal is sent to the Logic Unit (LU2 through LU4) and Memory Control Unit (MU3 through MU5). The phase 3 clock signal is inhibited during Type II microinstructions or when conditional Type I logic instructions are not to be executed (condition not met).

The system clock (SCLKn) signal is sent to all clocked logic elements not using the phase 3 clock signal.

The System Clock (SCLKn) signal is developed from the output of a gating circuit whose inputs are from: (1) the 10-MHz clock oscillator, (2) a flip-flop which indicates that a hexadecimal counter has reached a count equal of 7, and (3) an error controlled stop signal (ESTOP) gate. When

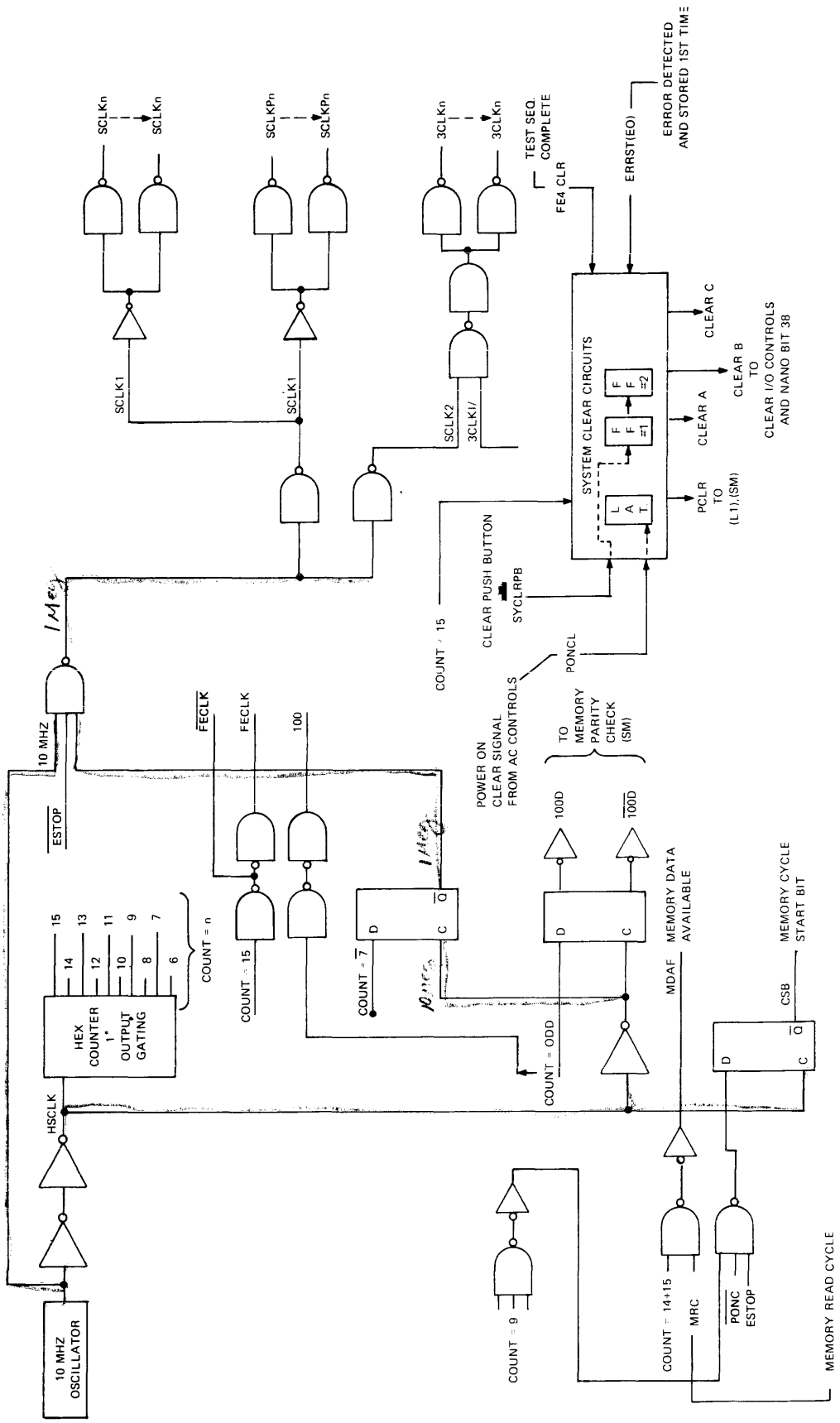


Fig. II-24. CLOCK AND CLEAR DISTRIBUTION (CG AND CD), BLOCK DIAGRAM

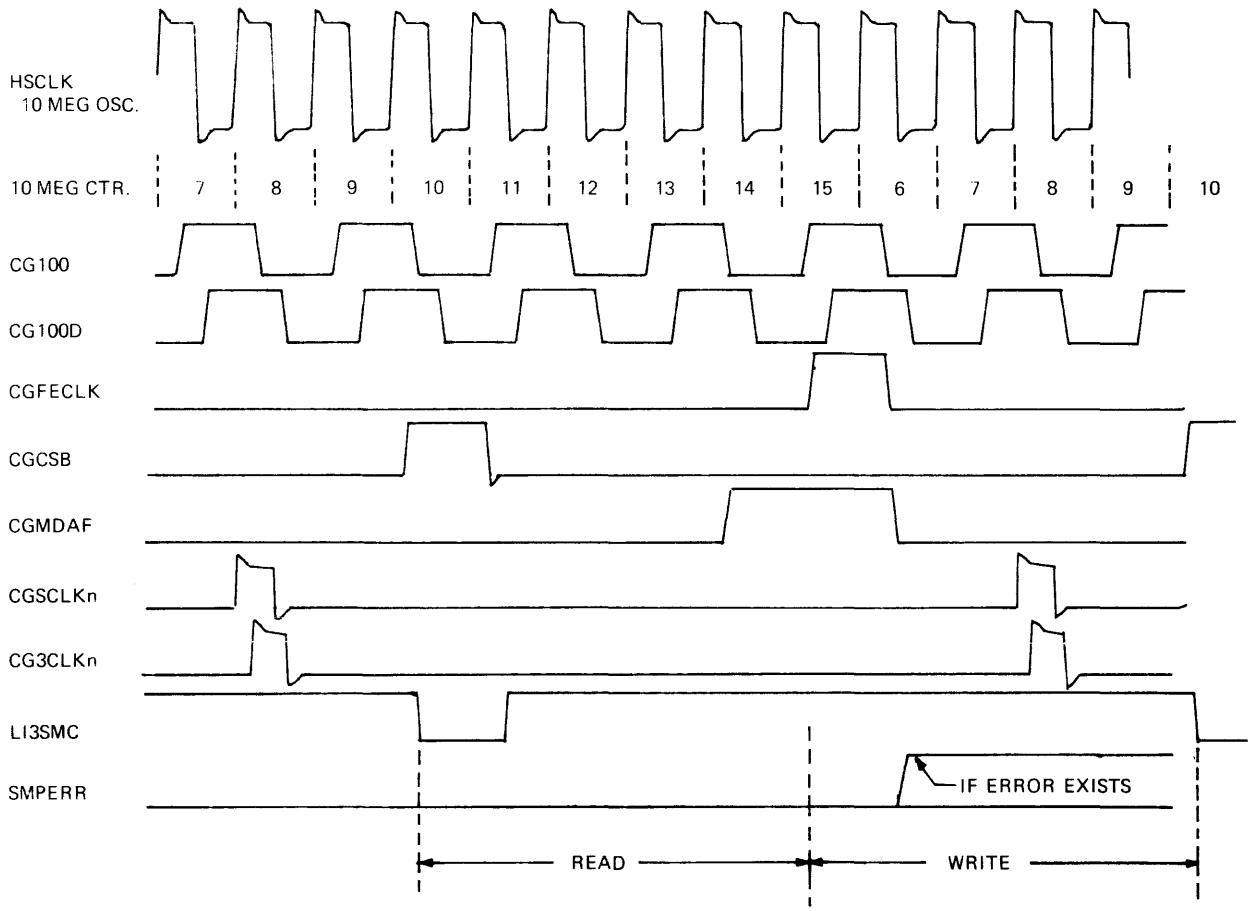


Fig. II-25. CLOCK GENERATOR, TIMING DIAGRAM

these inputs are all present, a 1-MHz system clock is produced. The hexadecimal counter used in the system clock circuit (Figure II-24) has only ten different usable output values ranging from a preset value of 6 and reaching a maximum count of 15 (by counting 10-MHz clocks). Timing diagram II-25 illustrates the relationship of signals used in developing the system clock signal. Single-stepping of the system clock pulses is accomplished by controlling the error stop logic signal from the F.E. cards single pushbutton, in conjunction with the NORM/SGL toggle switch.

Logic signals CG100, CG100D, CGCSB, CGFECLK, and CGMDAF are used for F.E. card and memory control timing. (See Figure II-24.) The F.E. clock (FECLK) is used to clock latches and flip-flops on the FE3 card when performing memory test, single pulsing, or proceeding from one test to the next. FECLK is delayed approximately 700 nonoseconds from system clock and is always present at a 1-MHz rate. The Cycle Start Bit (CSB) is used to enable the development of a Core Memory Cycle Start Time (LI3SMC). (See Figure II-25.) After a Memory Cycle has been started, Memory Data Available signal (MDAF) indicates that data has been read from memory. The 100/100D signals are used to establish the memory parity check time when Memory Data Available (MDAF) is true. A Memory Cycle begins with signal CSB, reads from core, checks parity and writes back old data or inserts new data to core. SMPERR is the signal that indicates an incorrect parity condition exists.

Input signal LIMRC, used to enable memory data available, indicates that the memory cycle was needed for reading from core memory.

The Clear Circuits of the clock generator card (CG) consists of a series of clear latches, associated gating, and the clear signal drive buffers. A system clear signal may be generated by powering up the system or by depressing any of the system clear pushbuttons.

The power on clear signal (ACPONCL) is present approximately 0.85 to 1.00 seconds during the power-up sequence. Signal ACPONCL is then latched when the clock control hexadecimal counter output equals 15. The output of the ACPONCL Latch clears the System Clear Pushbutton (SYSCLRB) flip-flop 1. When the clock control hexadecimal counter output is again equal to 15 (1 microsecond later) the SYCLRB flip-flop 2 is reset. The cleared flip-flop (SYSCLRB-1) also produces a Preclear signal (PCLR) used to clear memory parity check logic on the Shared Memory

(SM3) card and the Memory Loader logic on the Loader Interface (LI3 and LI4) cards.

The set output of SYCLRB flip-flop 2 is a low level that generates all the necessary clear signals through the clear buffers. (See Figure II-24.)

Use of the system clear pushbuttons utilizes the same sequence of events as the power on clear, excluding the use of the power-on clear latch.

Alternate methods of generating the system clear signals are from FE4CLR of the F.E. cards, indicating the completion of the current Test sequence, and EOERRST of the external operations control, indicating first error has been encountered. (Refer to memory hardware error control description.)

MAIN (CORE) MEMORY SECTION

GENERAL

The main (core) memory section of the CPU consists of one to three memory modules and a control board assembly, which comprise the functional Data/Program Memory (DPM) and the Microprogram Memory (MPM), Shared Memory (SM) controls, and Load Interface Controls (LIC). The DPM is the storage medium for all object/user programs and program data. The MPM stores the set of microinstructions. Core memory addressing and loading is controlled by the SM controls and the LIC.

The core memory is a read/write (destructive-read) toroidal core memory with a 1-microsecond cycle time. Figure VI-6 shows the layout of the core memory section, which is at the bottom right side of the CPU cabinet, as viewed from the front operator's panel.

Two sizes of core memory modules are used: a full-size module which has a capacity of 8,192 words, and a half-size module which has a capacity of 4,096 words. (One core-memory word is two bytes, or 16-bits, in length and has an additional bit for odd parity.) These modules are commonly referred to as the 8-K word and 4-K word modules, respectively.

As shown in Figure VI-6, each module is made up of three double-size boards and one core stack assembly. Two digit board assemblies are used for data control; each contains 17 data latches, 17 sense amplifiers for reading core memory, and 17 inhibit drivers to control the writing of data. An X/Y select board assembly contains circuits that temporarily store and decode memory addresses.

The core stack assembly consists of two permanently-joined double-size boards that contain the memory cores and associated wiring.

The control board assembly is not part of any module and is used for selecting modules, generating timing signals, and regulating the +15 and -15 volt dc sources for use in the memory modules. A terminator board is also provided in the memory section for terminating logic signal lines and eliminating noise.

Circuit board and core stack assemblies are located by use of a five-character reference designation. This designation consists of the rack and panel designator (PB), the board row (D or F for upper or lower part of board, respectively), and the board slot or column designator (as indicated in Figure VI-9). For example, circuit board PBDE1 is the upper part of the digit board assembly in slot E1.

CORE STACK ASSEMBLY

Each core stack assembly consists of an assemblage of memory cores on 17 electrical planes, one for each of the core memory word bits (16 data, 1 parity). A full-size memory module stack uses planes containing 8,192 cores to provide the 8,192-word capacity.

Memory Cores

The memory cores used in the core stack assembly are of the three-wire destructive-read configuration. (See Figure II-26.) One wire is shared by an X driver switch and an X common switch; another wire is shard by a Y driver switch and a Y common switch; and another wire is shared by a sense amplifier and an inhibit driver. The X and Y driver/common switch lines intersect the core for addressing purposes. The sense amplifier/inhibit driver line is used for reading data and controlling data inputs.

An individual core represents one bit of data and has two magnetic states: the ONE (1) state and the ZERO (0) state. An 800-milliampere current flow is required to change the state of a core.

When data is written into a core, a current of 400 milliamperes is driven down its interesecting X and Y lines. (See Figure II-27.) If a 1-bit is being written, the intersected core changes its magnetic flux to the ONE state if the associated inhibit driver is off.

If a 0-bit is being written (Figure II-28), the associated inhibit driver provides a 400-milliampere flow in opposition to the X line to cancel the effect of the X line. Thus, with only the Y-line effective, the core remains in the ZERO state to represent a 0-bit.

To read out the contents of core memory, 400 milliamperes of current is driven down selected X and Y address lines in the direction opposite to that used for a write operation. If a selected core is in the ONE-state, this reverse current flow causes the core to change to the ZERO state. (See Figure II-29.) This change in flux induces a small voltage into the sense amplifier line. The related sense amplifier produces an amplified output representing the logic ONE (1)-bit level.

If the core is in the ZERO state when being read, there is no change in flux and no induced voltage in the output occurs. (See Figure II-30.) The sense amplifier thus produces a level representing a logic ZERO (0)-bit.

The following three operations summarize the memory core applications:

a. The X and Y drivers and common switches drive current through the selected cores to read or write data in accordance with the address decoding of a word.
b. A related inhibit driver is controlled by data being written. That is, if the data is a ONE-bit, the driver is held in the off condition to allow the core to switch to the ONE state. Conversely, if the data is a ZERO bit, the driver is turned on to oppose the X current and hold the core in the ZERO state.
c. A corresponding sense amplifier reflects the switching or non-switching condition of a core to produce an amplified output representing a ONE or ZERO bit.

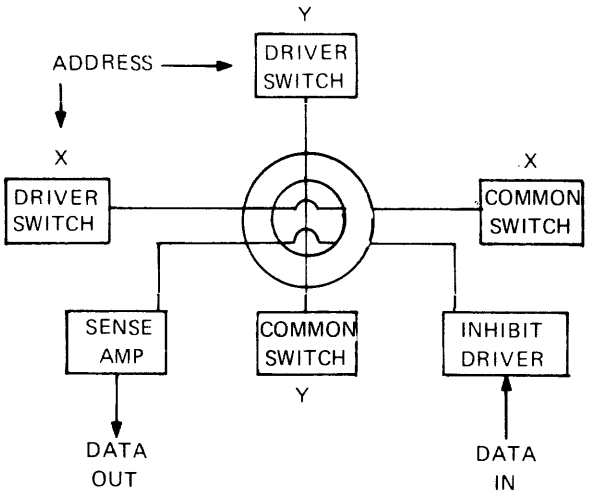


Fig. II-26. THREE-WIRE CORE CONFIGURATION

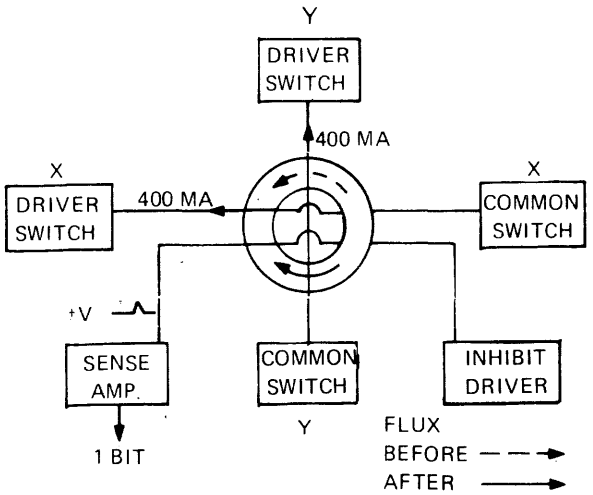


Fig. II-29. READING A ONE (1) BIT

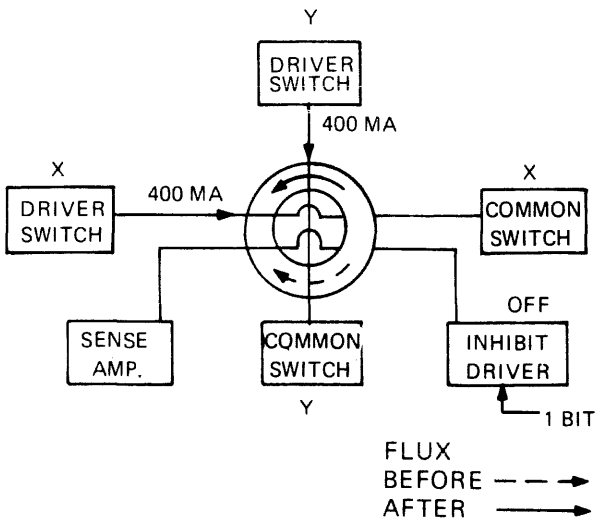


Fig. II-27. WRITING A ONE (1) BIT

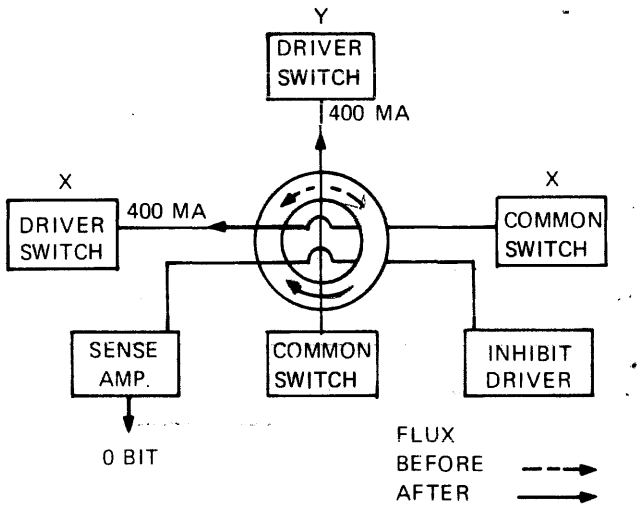


Fig. II-30. READING A ZERO (0) BIT

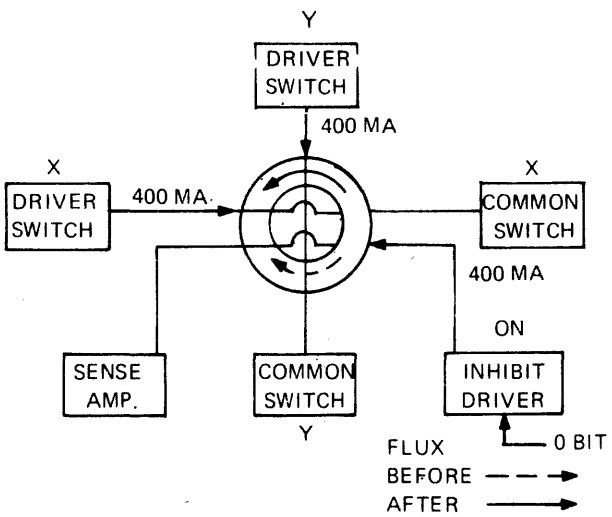


Fig. II-28. WRITING A ZERO (0) BIT

As seen from the previous descriptions, the core memory is a destructive read memory and requires a write operation immediately after a read operation to rewrite or restore any data read out of memory.

Memory Planes

To enable specific addressing and assigning data positions, memory cores are assembled and configured into 17 separate electrical planes. Each plane is configured into a 64x128 core matrix to enable addressing of 8,192 locations. Figure II-31 shows the layout of the core plane for bit 8.

There also are corresponding X and Y address lines for each coordinate. For every X-Y coordinate, there is a discrete core location that is intersected. Likewise, each core is intersected by only one distinct set of lines.

In the B 700 core memory, the addressing of an entire word (16 data bits, plus a parity bit) requires 17

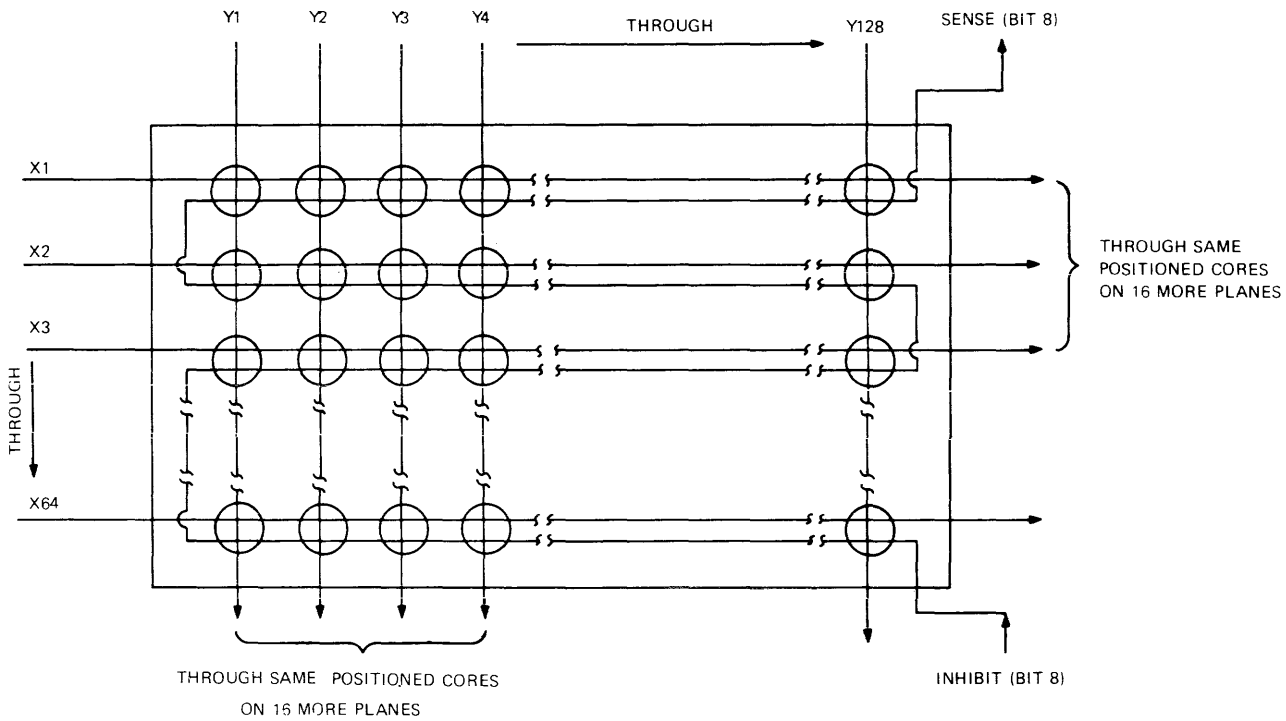


Fig. II-31. CORE STACK ELECTRICAL PLANE LAYOUT (EXAMPLE: BIT 8)

electrical planes sharing common cores in all 17 planes. Regardless of which core is selected by X and Y address lines, all cores on each plane are relative to one data bit of the core memory word. As shown in Figure II-31, one inhibit line controls the writing of bit 8 for any selected core of the possible 8,192. Likewise, there is only one sense line for reading the entire array.

Figure II-32 shows the routing of one set of core memory lines through common core locations in all memory planes. One X and Y driver switch and common switch are decoded from the address, and the corresponding intersect core in all 17 planes make up the full core memory word.

During a write operation, the processor sends 17 write data bits in parallel to memory, where they simultaneously enable or disable corresponding inhibit driver to write a 0 or 1 bit in the selected core. (For example, bit-5 selects the inhibit driver for plane 5.) During a read operation, all 17 sense amplifiers simultaneously detect a 0 or 1 bit change in the addressed cores and send 17 data bits in parallel back to the processor.

For each of the 8,192 combinations in the X and Y line plane matrix, one different core in each of the 17 planes is selected. A full word write operation (16 bits plus parity) is accomplished by assigning one inhibit driver and core plane to each of the 17 bit positions of the word. Likewise, a full word read operation is accomplished by having one sense amplifier for each plane or bit position.

MAIN MEMORY INTERFACE AND CONTROL

The main memory interface and control between a core stack and the processor is contained on four boards in the memory rack: the X-Y address, control, and (two) digit boards. Figure II-33 shows the signal flow of the interface and control for main (core) memory. The control board is required only in the basic memory module, and each additional memory module requires only an X-Y address board and two digit boards.

The control board contains a delay line and gates to produce the read, write, and strobe signals for memory cycle timing. Taps on the delay line are used to select the rise and fall times of memory timing signals, and gating is used to selet the addressed memory module. The control board provides timing for the X and Y Common switches (XC and YC) and the X and Y Driver switches (XD and YD) of the X-Y address board. The X-Y address board provides the X and Y Common signals (XC and YC) and both Positive and Negative X and Y Driver signals (XPD, XND, YPD, and YND) for the core stack. Timing signals from the control board and 16 data signals, plus parity, are applied to the digit boards for the 17 Inhibit signals (IHB) for the core stack. Both ends of the 17 sense lines (S) from the core stack are applied to the digit boards for reading data.

MAIN MEMORY TIMING

All timing signals used in main memory are generated and controlled by circuitry on the control board assembly. Memory timing signals are derived from a delay line pack-

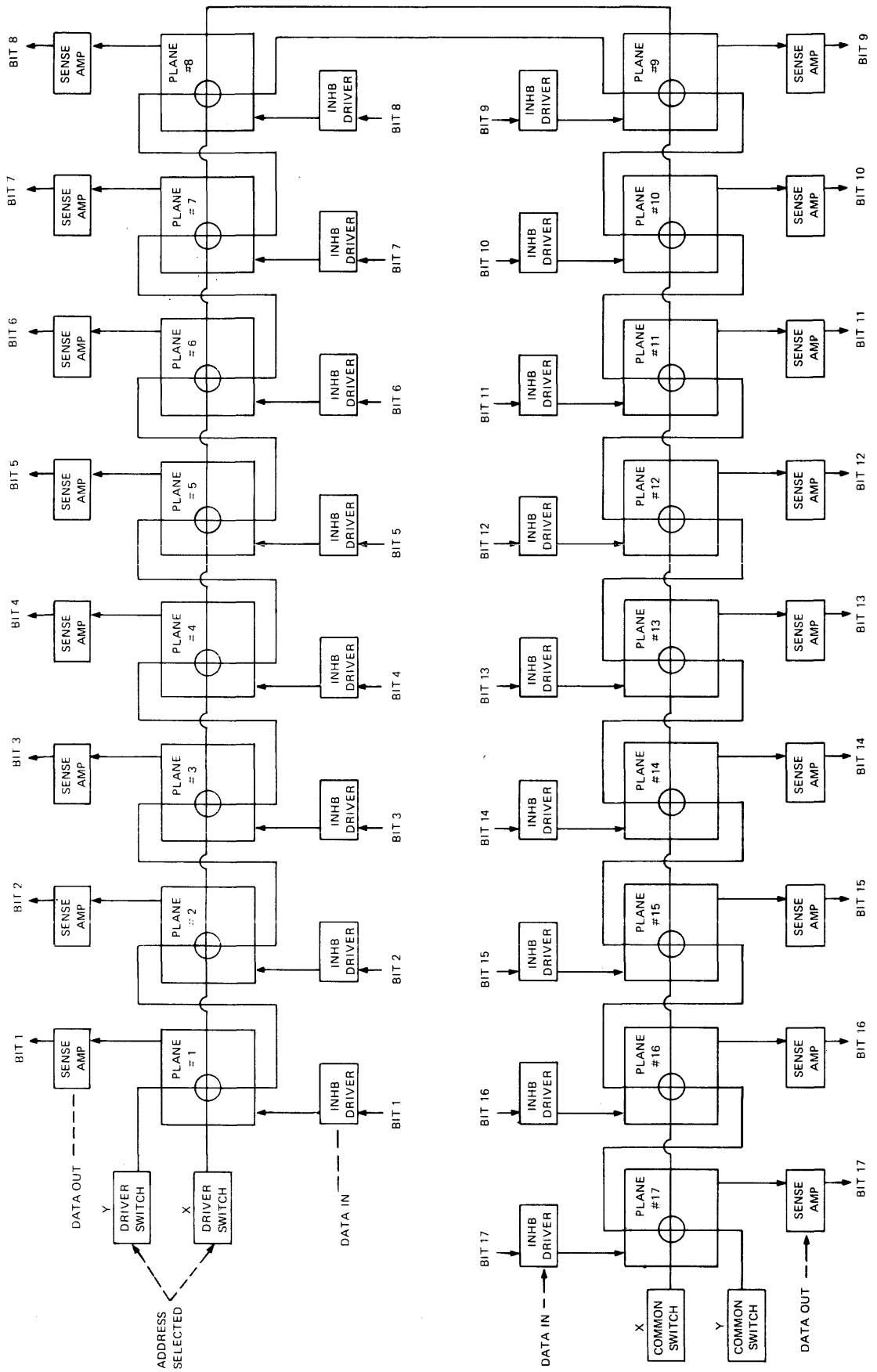


Fig. II-32. LINE ROUTING THROUGH COMMON CORE LOCATIONS

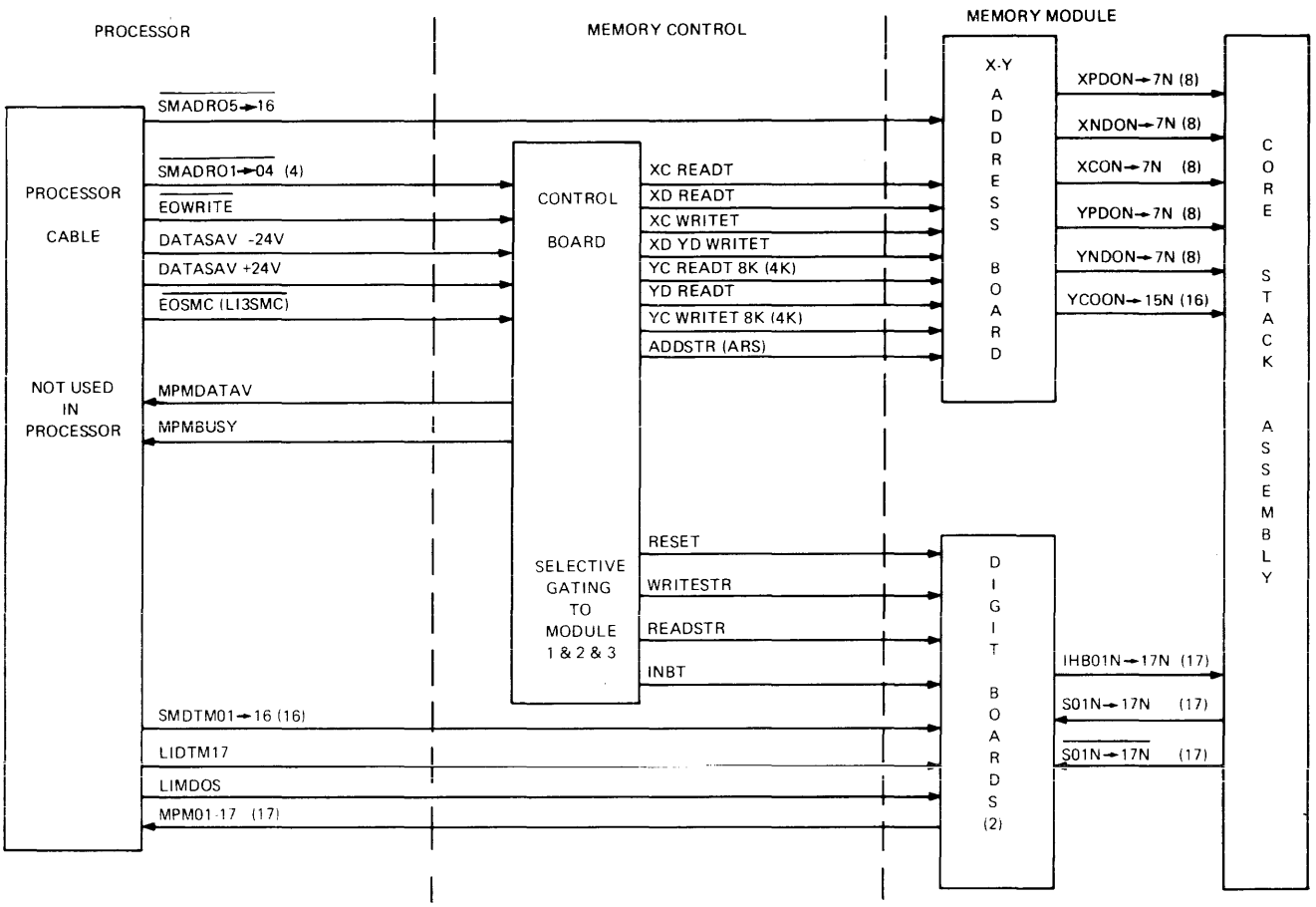


Fig. II-33. MEMORY MODULE INTERFACE AND CONTROL

age which is triggered once at the beginning of every main-memory cycle. One complete main memory cycle is 1 microsecond, or the duration between two processor clock pulses.

The sequence of timing for one main memory cycle is shown in Figure II-34. The Start Memory Cycle signal (EOSMC/ or EOSMC) is used as the 0-nanosecond or starting reference for all other timing signals. All signals except EOSMC/ originate on the control board assembly. This signal originates in the processor section and occurs at the beginning of every main memory cycle. EOSMC/ is a negative signal that triggers the delay line package.

The Address-Strobe timing signal (ADDSTR) is distributed to the X-Y select board assemblies in each core memory module, where it enables the address latches to receive the shared memory address lines from the processor section.

The Reset timing signal (RESET) is distributed to the digit board assemblies in each core memory module, where it resets all data latches at the beginning of every memory cycle.

The X-Driver Read-Timing signal (XD READT) is distributed to the X-Y select board assemblies, where it turns on the selected X-driver switch during the read operation in a memory cycle.

The X-Common Read-Timing signal (YD READT) is sent to a module X/Y address board, where it turns on the selected X common switch during the read half of the memory cycle.

The Y-Driver Read-Timing signal (YD READT) is sent to a module X/Y address board, where it turns on the selected Y driver switch during the read half of the memory cycle.

The Y-Common Read-Timing 8-K and Y Common Read-Timing 4-K signals (YC READT 8-K and 4-K) are sent to a module X/Y address board, where they turn on the selected Y-common switch during the read half of a memory cycle, YC READT 8-K is used for a full-size module, and YC WRITET 4-K is used for a half-size module.

The Read-Strobe timing signal (READSTR) is sent to the module digit boards to enable the sense amplifiers during the read half of a memory cycle. READSTR remains false during a processor memory write operation. READSTR has adjustable delay line taps to meet the specifications of each core stack assembly.

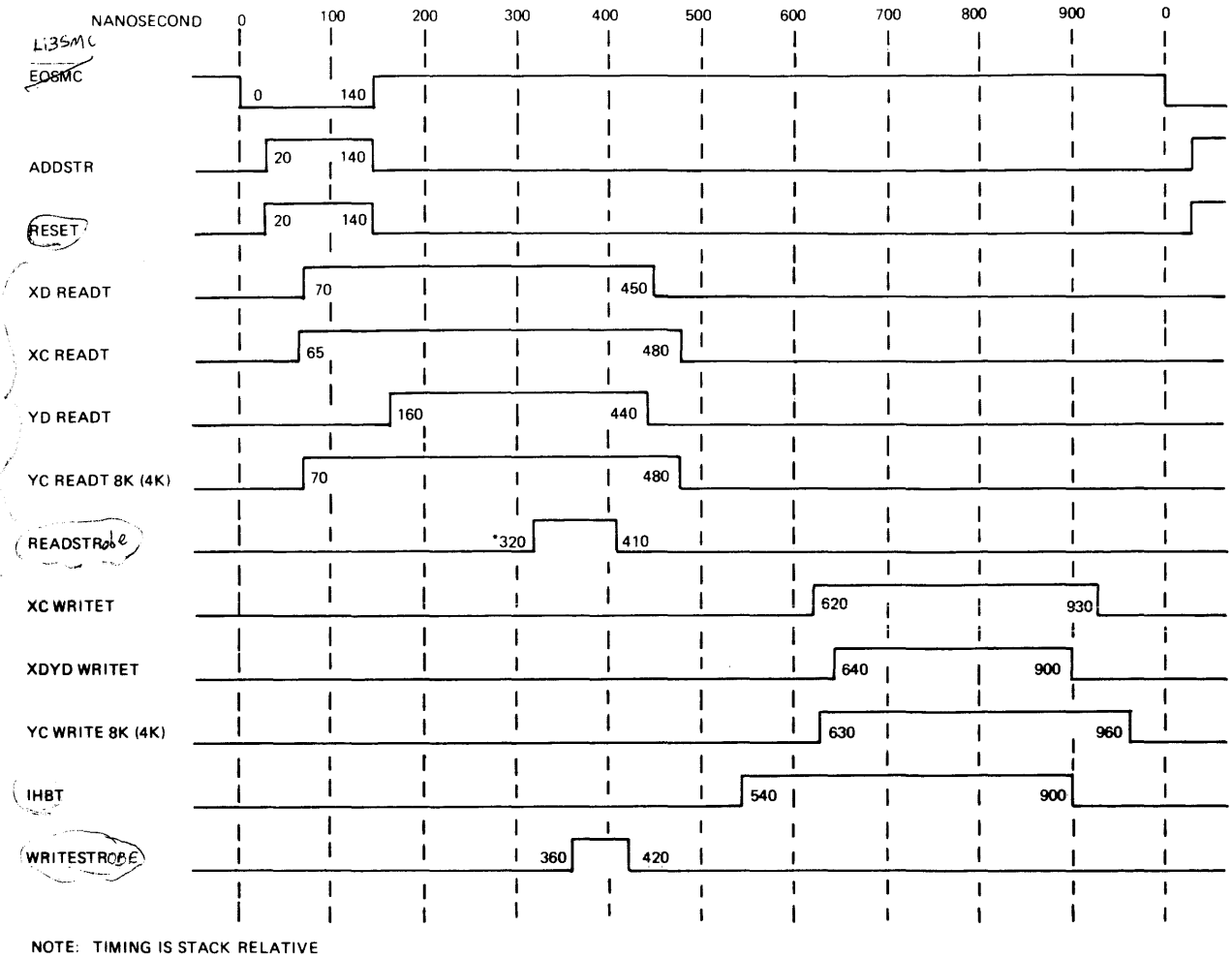


Fig. II-34. CORE MEMORY TIMING

The X-Common Write-Timing signal (XC WRITET) is sent to a module X/Y address board, where it turns on the selected X common switch during the write half of the memory cycle.

The X-Driver-Y-Driver Write-Timing signal (XDYD WRITET) is sent to a module X/Y address board, where it turns on the selected X and Y driver switches during the write half of a memory cycle.

The Y-Common Write-Timing 8-K and Y-Common Write-Timing 4-K signals (YC WRITE 8-K and 4-K) are sent to the module X/Y address board, where they turn on the selected Y-common switch during the write half of the memory cycle. YC WRITET 8-K is used for a full-size module, and YC WRITET 4-K is used for a half-size module.

The Inhibit-Timing signal (IHBT) is sent to the module digit boards to enable the inhibit drivers on the write half of a memory cycle.

The Write-Strobe timing signal (WRITESTR) is sent to the module digit boards, where it provides a clock pulse for the data latches to receive new data from the processor on the shared memory data lines. WRITESTR remains false during a processor memory read operation.

MEMORY ADDRESSING OPERATIONS

Origin and Control of Addresses

Figure II-35 shows the overall core memory addressing operation involving the processor, memory control unit, and a memory module. Core memory addresses are originated by the processor Incrementor (INCR). The INCR is a 14-bit register that addresses core memory on an instruction read or on a write operation controlled by the Load Interface Control (LIC). Base Register 1 (BR1) or Base Regiseter 2 (BR2), when used with the Memory Address Register (MAR), produces 16-bit core memory addresses. These addresses are used in performing a Memory Read (MR) or Memory Write (MW) operation for program data.

Twelve bits of an address are sent to the core memory module. Six address bits set X address latches which select

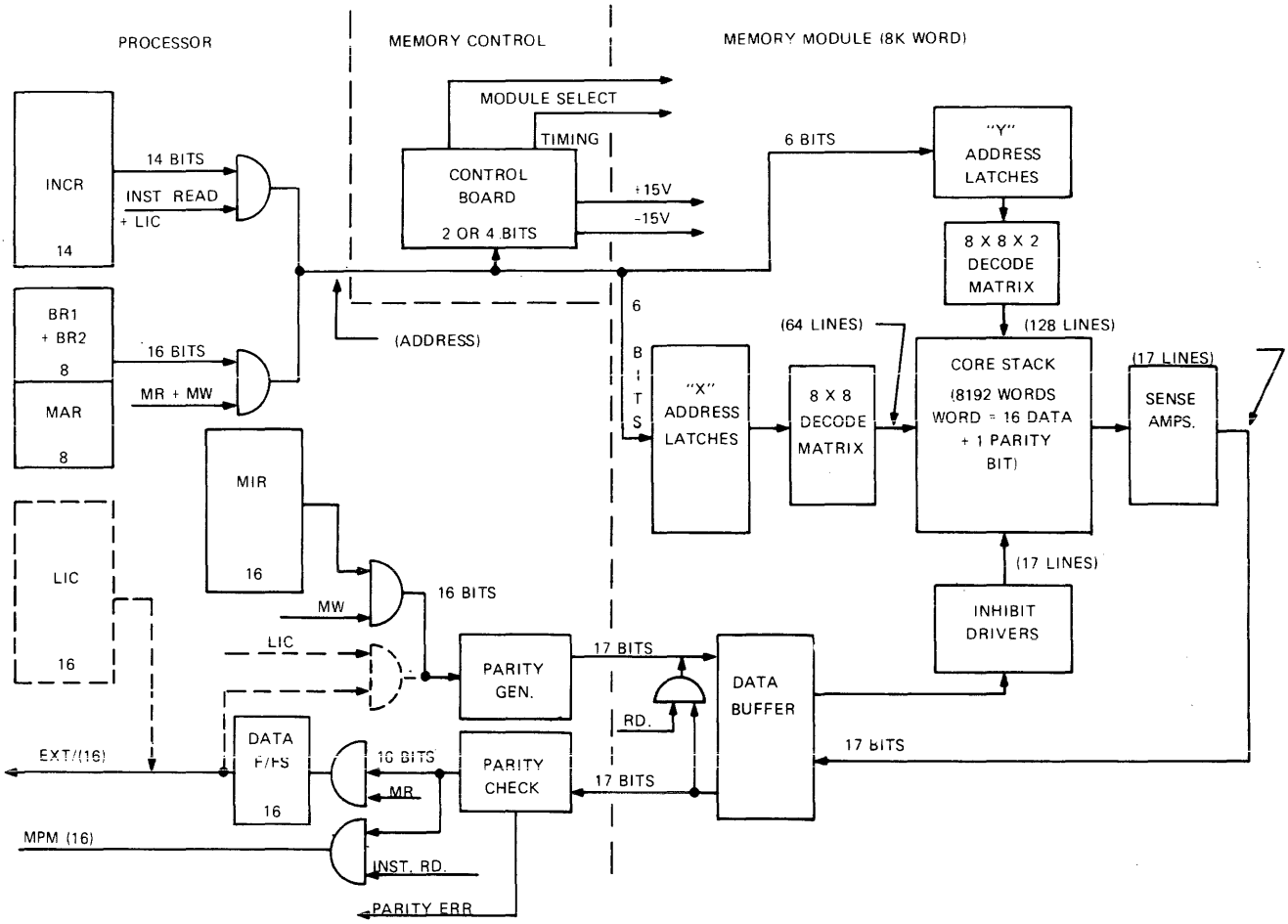


Fig. II-35. CORE MEMORY BLOCK DIAGRAM

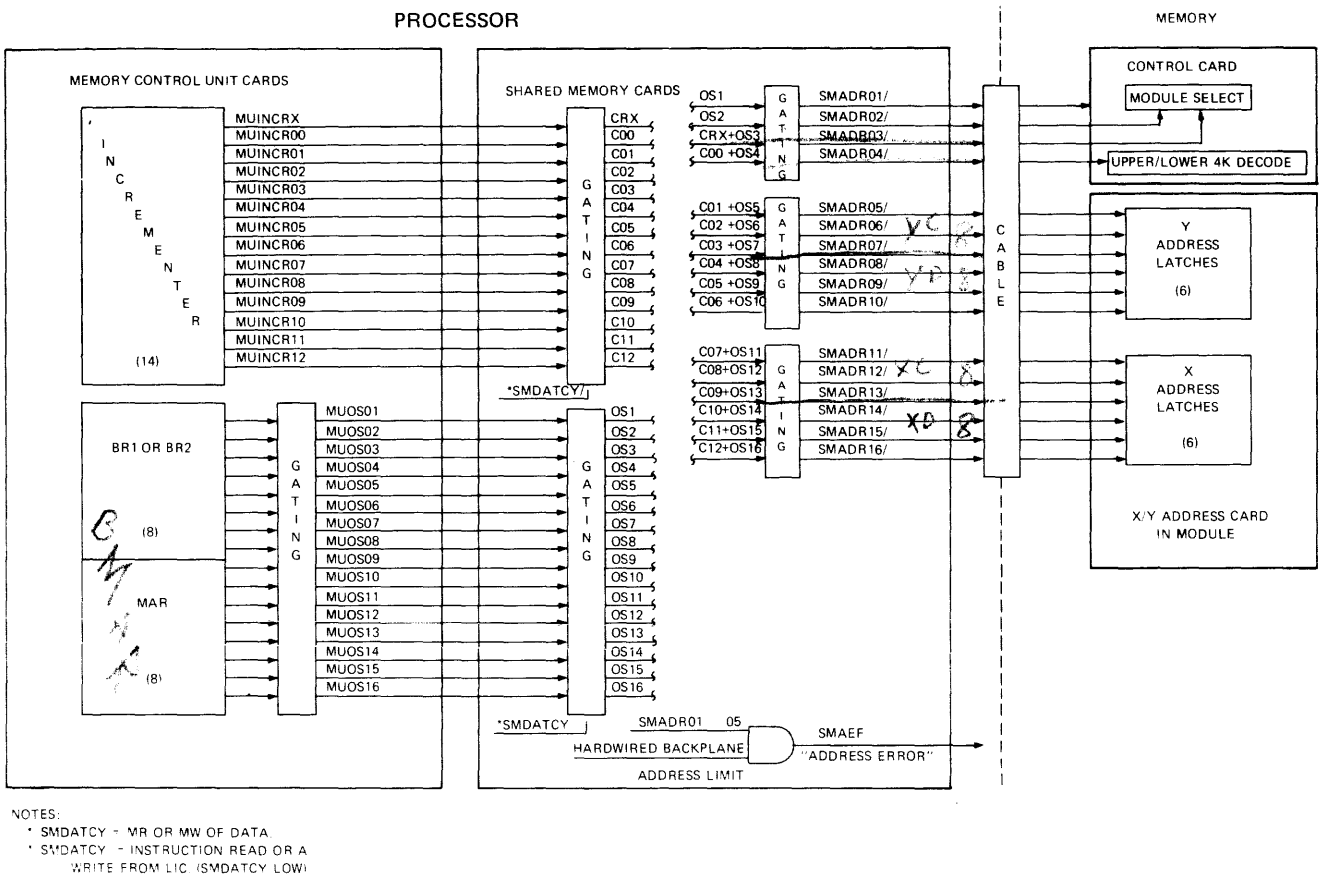
one of the 64 core stack lines by use of an 8-by-8 decoding matrix. Six address bits are used by the Y address latches for an 8-by-2 decoding matrix to select one of the 128 core stack Y lines. The remaining four address bits from BR and MAR or two bits from INCR are sent to the memory control board for module selection and module size decoding.

Figure II-36 shows the detailed addressing interface. The core memory address registers are located on the Memory Control Unit (MCU) cards in the processor. If BR1 or BR2 and MAR are used, their 16-bit output is first placed on MUOS lines 1 through 16 for gating to the Shared Memory (SM) cards. If the Shared Memory Data Cycle (SMDATCY) signal is true, the MUOS bits are placed on Shared Memory Address lines 1 through 16 (SMADR01/ through SMADR16/) for transfer to memory. If the address source is the incrementor, outputs MUINCRX through MUINC12 are gated to shared memory address lines 3 through 16 for transfer to memory because signal SMDATCY is low.

In the shared-memory cards, address lines SMADR01 through SMADR05 are compared to a hardwired address limit. If this limit is exceeded, the address error failure signal goes low (SMAEF1) and is detected by the processor error-detection logic.

Address lines SMADR01/ through SMADR04/ are sent to the control board in memory, where SMADR02/ and SMADR03/ are used to select one of the three possible core modules. SMADR04/ is used to decode an address in the upper or lower 4-K area of the selected module. (SMADR01/ is not used.) Address lines SMADR05/ through SMADR16/ are sent to the X/Y address board in the selected module. SMADR05/ through SMADR10/ set six-address latches for Y-line selection, while SMADR11/ through SMADR16/ set six X-address latches for X-line selection.

A core memory address can be displayed by the FE board indicators in hexadecimal notation. The indicator hexadecimal value, and the corresponding bit positions of the shared memory address lines are shown in Figure II-37. Also shown is the bit relationship between the incrementor, BR1 or BR2, and MAR to the address lines. For example, shared memory address line (SMADR) 16 is displayed as 1 of the D digit on the FE boards, and its source is either incrementor bit-12 or MAR bit-8. One example of a hexa-



NOTES:
* SMDATCY = MR OR MW OF DATA
* SMDATCY = INSTRUCTION READ OR A WRITE FROM LIC (SMDATCY LOW)

Fig. II-36. CORE MEMORY ADDRESSING INTERFACE

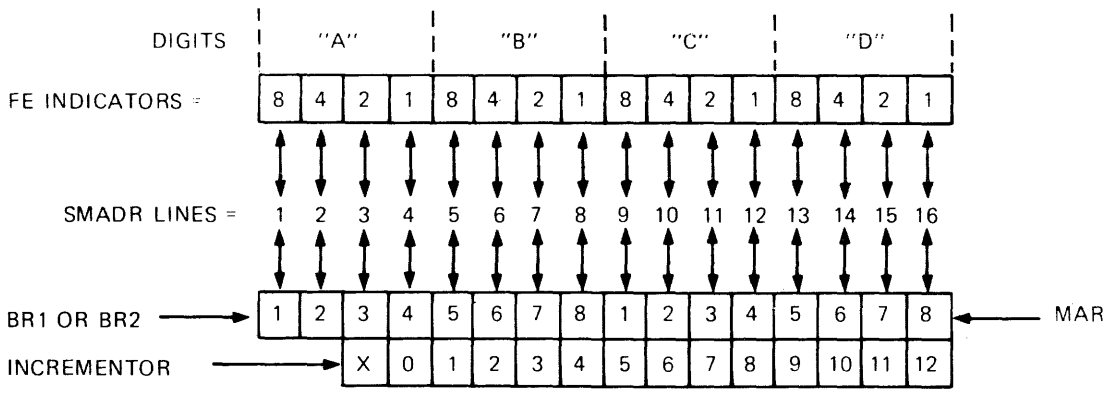


Fig. II-37. SHARED-MEMORY BIT POSITIONS

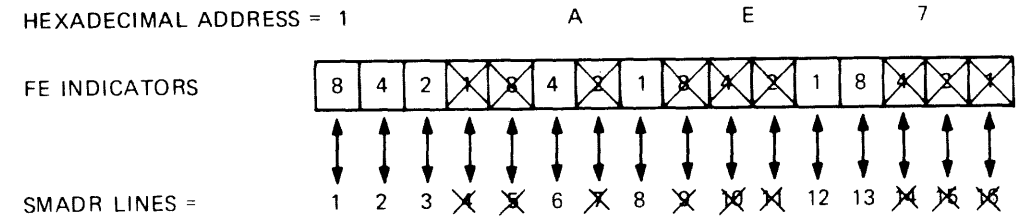


Fig. II-38. EXAMPLE OF MEMORY ADDRESS ON FE INDICATORS

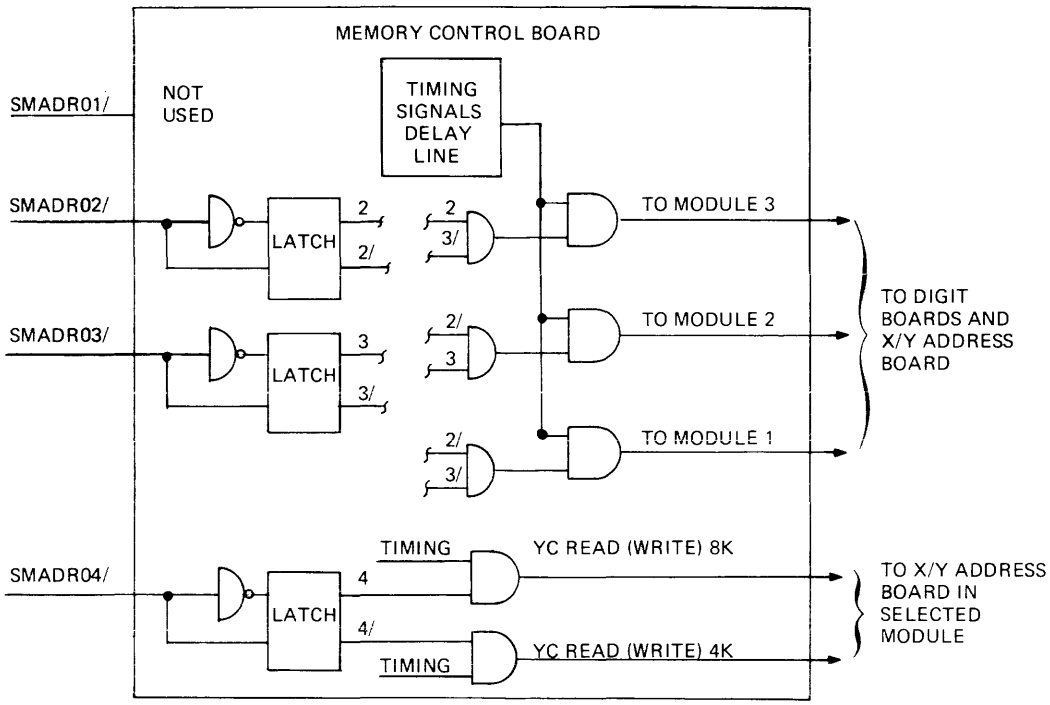


Fig. II-39. MEMORY CONTROL BOARD MODULE SELECTION

decimal address display is shown in Figure II-38, along with the selected SMADR lines.

Figure II-39 shows the memory control board logic used by signals SMADR01/ through SMADR04/ to select and address a memory module. SMADR02/ and SMADR03/ are used to select which module is to be addressed. These address bits set latches whose outputs are decoded to select one of the three modules. The module is selected when the address decoding enables all timing signals to that module. (Address bits 2/ and 3/ select module 1, bits 2/ and 3 select module 2, and bits 2 and 3/ select module 3.) SMADR04/ sets a latch whose output determines if the upper or lower 4-K area of the module is addressed. If SMADR04/ is true, the YC READ (WRITE) 4-K timing signal is sent to the selected module for Y-line decoding of the lower 4-K addresses. If SMADR04 is false, the YC READ (WRITE) 8-K signal is used.

X-Line and Y-Line Decoding

After a module is selected, there are 8,192 addresses that can be decoded by the selection of intersecting X and Y lines. As shown in Figure II-40, SMADR bits 5 through 10 and SMADR bit-4 (stack size) select the Y line. SMADR 11 through 16 complete the address decoding by selecting an X line.

Figure II-41 shows the X-line decoding. When the Address-Strobe timing signal (ADDSTRn, where n is module number) is received by the selected module, X-address bits SMADR11/ through SMADR16/ set latches on the module X/Y board. The latch outputs for SMADR11/

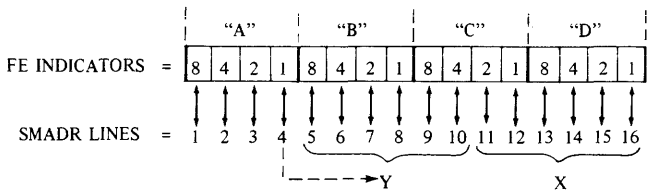


Fig. II-40. X-LINE AND Y-LINE DECODING

through SMADR13/ are decoded octally to select one of eight X-common switches. Likewise, SMADR14/ through SMADR16/ latch outputs are decoded to select one of eight X-driver switches. The outputs of the X-driver switches and common switches are sent to the core stack assembly, where they form an 8-by-8 matrix to select one of the 64 X-lines through the cores.

As an example, hexadecimal address 09F7 indicates that SMADR11, 12, 14, 15, and 16, are high (true) and SMADR13 is low (false). As shown in Figure II-41, the address lines are received in their inverted states; therefore, SMADR11/, 12/, 14/, 15/ and 16/ are low and set their latches, while SMADR13/ is high and resets its latch. With 13/, 12 and 11 high, X-common switch 1 (XC1N) is selected and X-driver switch 0 is selected with 14, 15, and 16 high.

There are two possible outputs from X-driver switch 0: (1) XPD0N, which is the positive output (+15 VDC), and (2) XND0N, which is the negative output (-15 VDC). X-common switch 1 has two possible voltage outputs: +15 VDC or -15 VDC (XC1N). The timing signals from the control board determine which outputs are used.

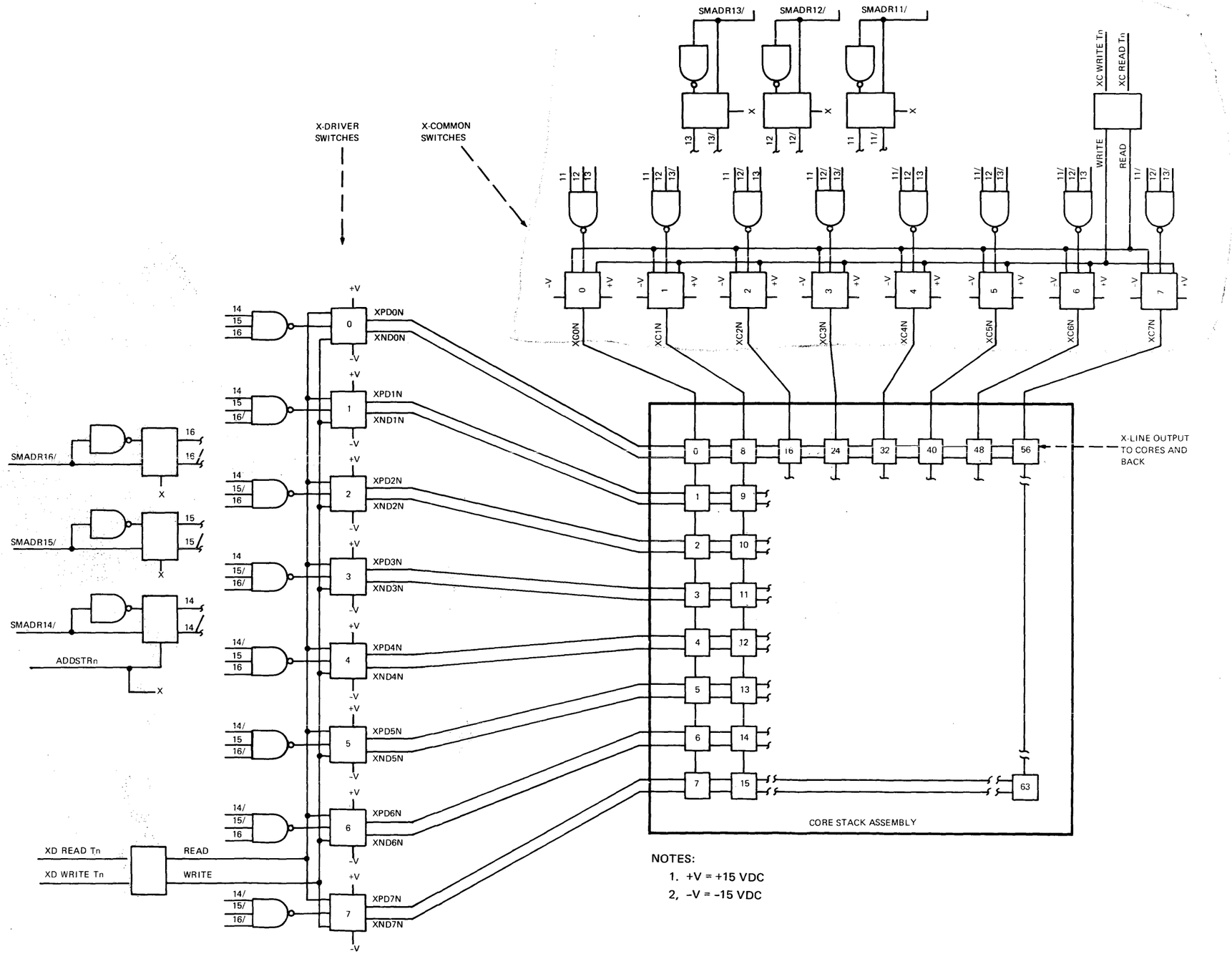
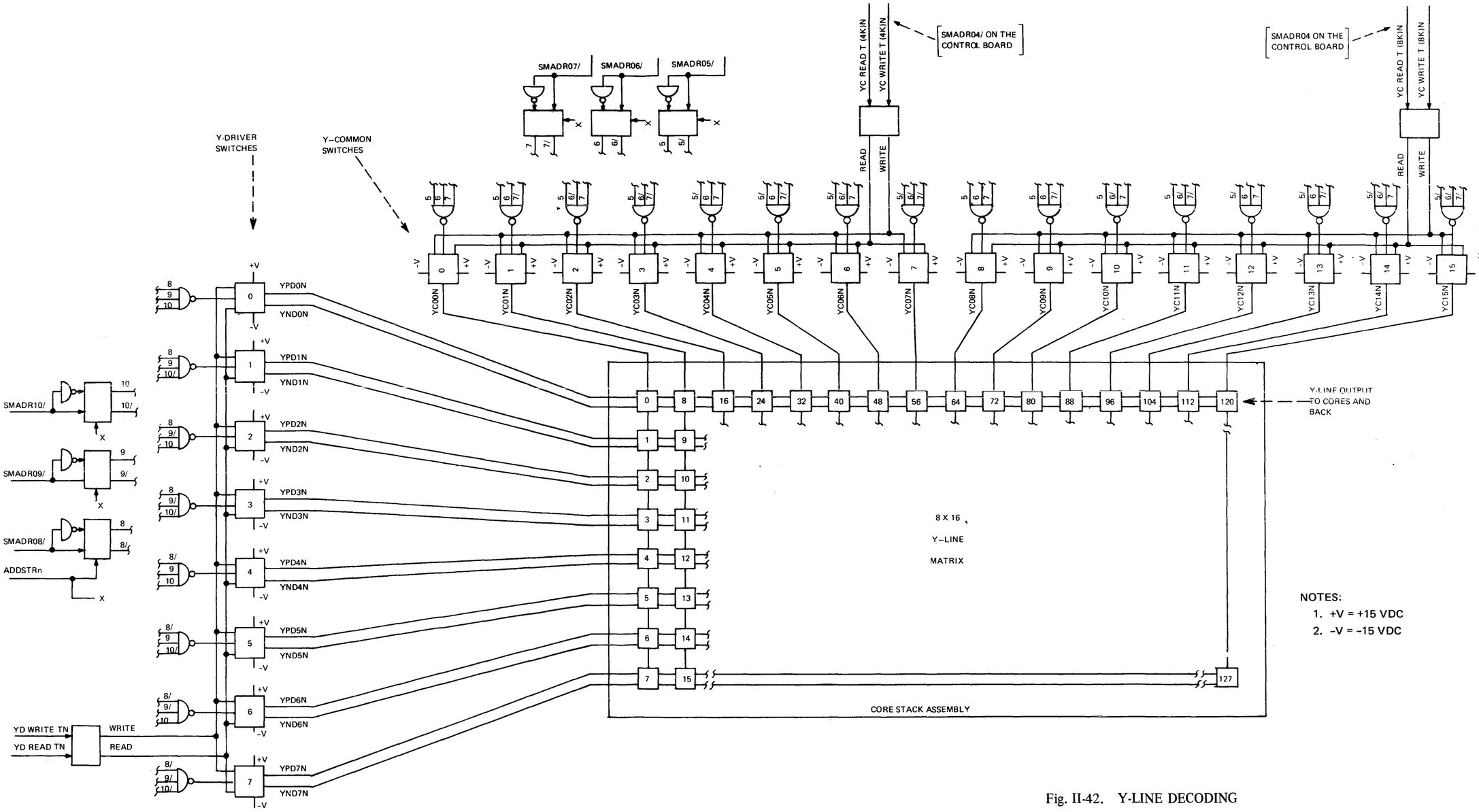


Fig. II-41. X-LINE DECODING



NOTES:
1. +V = +15 VDC
2. -V = -15 VDC

Fig. II-42. Y-LINE DECODING

During the read half of a memory cycle, X-Driver Read Timing (XD READ Tn) is true, and the positive output of the driver (XPD0N) is selected. X-Common Read Timing (XC READ Tn) is also true to switch the negative output of the common switch (XC1N = 15 VDC). Outputs XPD0N and XC1N are sent to the core stack assembly, where they make up an 8-by-8 matrix to select and drive current down one of the 64 possible X lines. For example, X-line 8 current flows from XC1N through the cores and back to XPD0N.

During the write half of a memory cycle, X-Driver Write Timing (XD WRITE Tn) is true to select the negative output of the driver (XND0N). X-Common Write Timing (XC WRITE Tn) is also true to switch the positive output of the common switch (XC1N = +15 VDC). Outputs XND0N and XC1N are sent to the core stack assembly, where they select the same X line as the read half of the memory cycle; only the current flow is reversed. Current flow is now from XND0N through the cores and back to XC1N.

Figure II-42 shows the Y-line decoding. Y-line selection is accomplished in the same manner as the X-line selection. Y-line selection also uses eight driver switches, but has either eight or 16 common switches for a 4-K or 8-K module, respectively.

When the address strobe timing signal (ADDSTRn) is received by the selected module. Y-address bits SMADR08/ through SMADR10/ set latches whose outputs select one of eight driver switches. SMADR05/ through SMADR07/ set latches whose outputs select two common switches: one of the common switches numbered 0 through 7, and one of the switches numbered 8 through 15. SMADR04/ controls the Y-common timing signals (YC READ/WRITE 4-K and YC READ/WRITE 8-K) which then enables one of the two common switches previously selected. The output of the Y-driver and common switches are sent to the core stack assembly, where they make up an 8-by-16 matrix to select one of the possible 128 Y lines through the cores. When a 4-K module is used, Y-common switches 8 through 15 are omitted and the core stack assembly contains an 8-by-8 Y-line matrix.

An example of Y-line decoding is described for hex address 09F7. In reference to Figure II-40, it is determined that lines 5, 8, 9, and 10 of SMADR are high (true) and lines 4, 6 and 7 are low (false). In Figure II-42, lines 05/, 08/, 09/, and 10/ of SMADR are low and set their respective latches, while lines 06/ and 07/ are high and reset their respective latches. When latch outputs 8, 9, and 10 are high, Y-driver switch 0 is selected. When latch outputs 5, 6/, and 7/ are high, Y-common switches 3 and 10 are selected.

During the read half of the memory cycle, Y-Driver Read Timing signal (YD READTn) is true and enables the negative output of the selected driver switch. That is, if YND0N SMADR04/ is high, Y-Common Read Timing signal (YC READ T 4K n) is true and enables the positive output of the selected common switch 0 through 7 (YC03N). Outputs YND0N and YC03N are sent the core stack assembly, where they select and drive one of the 128 Y lines (line 24, for example). The current flow is from YND0N, through the cores, and to YC03N.

During the write half of the memory cycle, Y-driver write timing signal (YD WRITE Tn) is true and enables the positive output of the selected driver switch (for example: YPD0N). When SMADR04/ is high, the Y-Common Write Timing signal (YC WRITE T 4K n) is true and enables the negative output of the selected common switch 0 through 7 (for example: YC03N). Outputs YPD0N and YC03N are sent to the core stack assembly, where they select the same Y line as the read half of the memory cycle. However, the current flow is reversed (from YC03N through the cores and back to YPD0N).

X- and Y-Common and Driver Switches

In Figure II-43, X-driver switch 0 and X-common switch 1 are shown with the selected X-line 8 in the matrix on the core stack assembly. When the address selects X-driver switch 0, pins 5 and 7 of transformer chip T220M are grounded. During the read half of the memory cycle, the READ timing signal applies a positive voltage to pin 6 of T220M. A positive potential occurs on pin 11, and Q1 is turned on to apply +15 volts (signal XPD0N) to CR24 on the core stack assembly.

When the address selects X-common switch 1, pins 2 and 3 of transformer chip T158H are also grounded. The positive READ timing signal on pin 1 induces a positive potential on pin 16 and turns on Q3. The -15 volts on Q3 becomes signal XC1N that is applied to pin A of coil Z3 in the core stack assembly. XC1N is then routed through the cores on X wire 8 and returns to pin C of coil Z3. From pin D of Z3, the -15 volts forward biases CR24 which uses the +15 volts XPD0N signal as the common return. Current flow is from -15 volts on the common switch through the cores and back to the +15 volts on the driver switch.

In the write half of the memory cycle, the basic difference is the direction of the current flow. The address still applies a ground on pins 5 and 7 of X driver switch 0 and pins 2 and 3 of X common switch 1. The WRITE timing signal applies a positive voltage to pin 4 of T158H for X-common switch 1. A positive potential occurs at pin 13 and turns on Q4. Q4 applies +15 volts (signal XC1N) to the core stack assembly. The WRITE timing signal also applies a positive voltage to pin 8 of T220M of X-driver switch 0. A positive potential is felt on pin 9 and turns on Q2. The -15 volt is applied as signal XND0N to CR23 on the core stack assembly. CR23 is forward-biased, and the -15 volts is sent through coil Z3 (pins D and C), through the cores on X wire 8 and back through coil Z3 (pins B and A). The +15 volts (signal XC1N) is used as the voltage common. Current

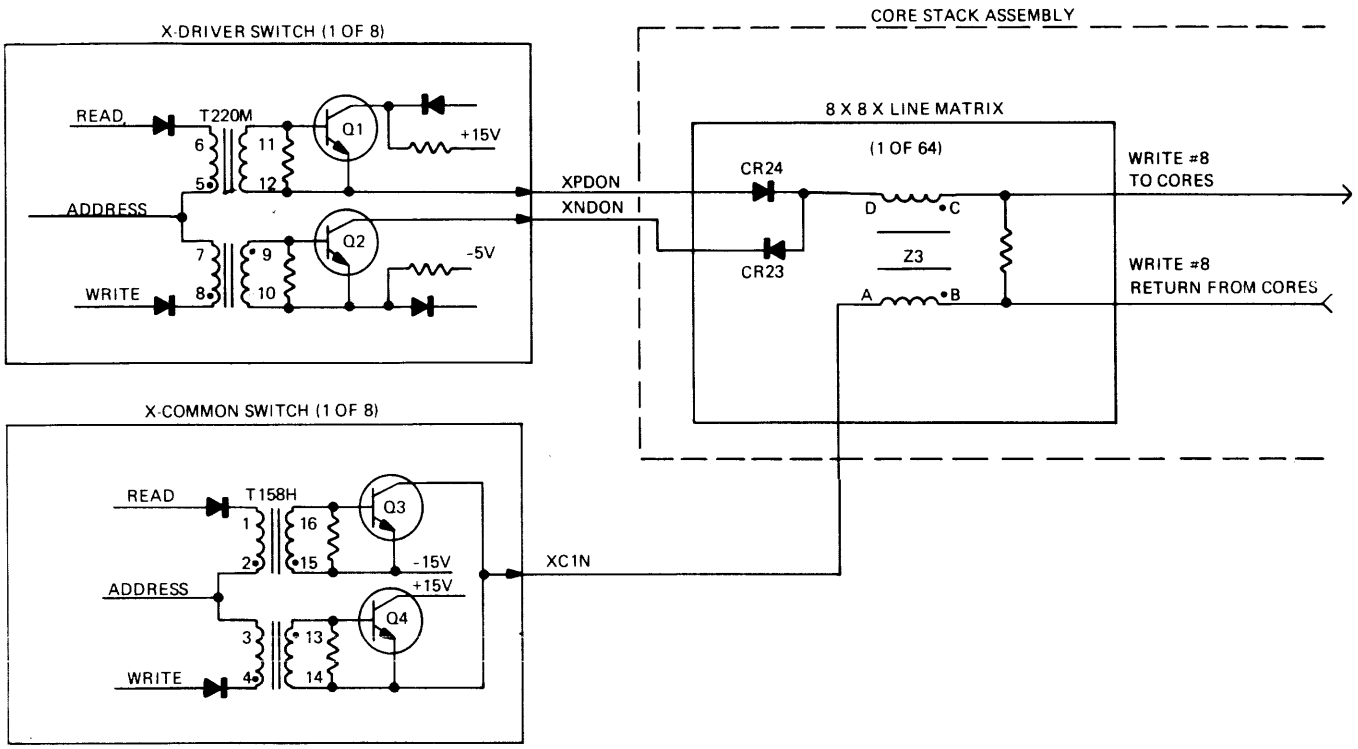


Fig. II-43. X-DRIVER AND COMMON SWITCHES FOR X-LINE 8 SELECTION

flow is from the -15 volts on the driver switch through the cores and back to the +15 volts on the common switch. The Y-driver and common switches operate in the same manner as described for the X-driver and common switches.

READING AND WRITING DATA

Origin and Gating of Data

Data is written and read back 16-bits in parallel, or one core memory word at a time. Data is written to core memory from two possible sources. One source is the Memory Information Register (MIR); the other is the Loader Interface Control (LIC). (See Figure II-35.)

When a Memory Write operation (MW) is performed, the 16 data bits from MIR are sent through a parity generation circuit where odd parity (bit-17) is produced. The data is then sent to a 17-bit data buffer on the digit boards in core memory. The output of the data buffer controls 17 inhibit drivers, which in turn enable or disable the writing of 1-bits in the core stack.

The other data source, LIC, is the hardware-controlled loading of paper tape through the console paper tape loader. Data bits are also written in parallel to core memory from this source.

When data is read from core memory, the output of the core stack is detected by 17 sense amplifiers. The output of these sense amplifiers feed the data buffer where the information is latched up. The data buffer output is returned to the processor, where parity is checked. If the operation is a Memory Read operation (MR), the 16 data bits are placed on the External bus lines (EXT's) of the processor. If the operation is an Instruction Read operation (INST. RD.), the data is placed on the microprogram Memory lines (MPM). The output of the data buffer is also fed back into itself for restoring the data on the write half of the memory cycle.

Data Transfer to Core Memory

The two sources of data transfers to core memory are shown in Figure II-44. The inverted outputs (LUMIR01/ through LUMIR16/) of MIR are sent in parallel to a multiplexer in the shared memory area of the processor. The Load Interface Control (LIC) in the processor has a 16-bit shift register whose output is inverted and placed on the External bus lines (EXT01/ through EXT16/) to the multiplexer. The multiplexer determines which input source to memory is to be used. The LIC logic is used for the hardware-controlled paper tape reader operations. Signal LIMEW goes high to the multiplexer and gates signals EXT01/ through EXT16/ onto shared memory data lines SMDTM01 through SMDTM16.

When a processor memory write operation is performed, LIMEW is low to the multiplexer, and inputs LUMIR01/ through LUMIR16/ are gated to the SMDTM01 through SMDTM16 data lines. Shared memory data lines 01 through 16 are sent through a parity generation circuit to

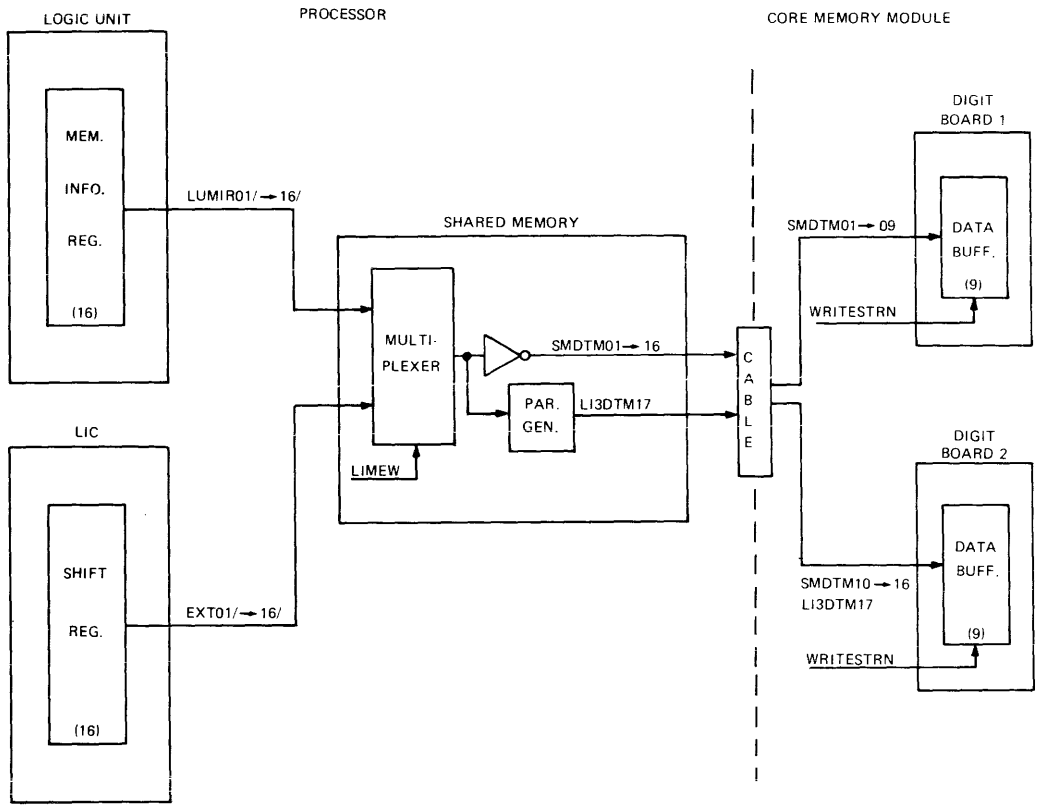


Fig. II-44. CORE MEMORY DATA TRANSFER

generate an odd parity bit (LI3DTM17). The 17 data lines are sent from shared memory to core memory through a cable.

When the selected module receives the Write Strobe timing signal (WRITESTRN), the data is latched up in the selected module data buffer. The buffer in the module is contained in two identical boards. Digit board 1 receives nine data bits, (SMDTM01 through SMDTM09) while digit board 2 receives nine data bits, (SMDTM10 through SMDTM16 and LI3DTM17) and has one spare latch.

Data Transfer From Core Memory

When the Memory Data Out Strobe timing signal (LIMD0S/) is received by the selected module the information in its data buffer is placed on the MPM01 through MPM17 data lines. (See Figure II-45.) The data lines are sent through a cable to the shared memory area of the processor, where parity is checked. If parity is bad, the Shared Memory Parity Error signal (SMPERR) goes true.

There are two kinds of memory read operations: one is for accessing machine language instructions, the other is for all other types of data. When accessing information other than machine language or microinstructions, the SMCLKA/ signal comes true to latch up the data on MPM lines 01 through 16. When processor instruction BEX is executed, signal EOMDSB comes true to gate the data onto external bus lines ETX01/ through EXT16/.

When a microinstruction is accessed, the SMCLKA/ signal stays false and prevents the latching of the data lines. MPM lines 01 through 16 are gated directly to the processor logic controlled by the instruction that is read.

Core Memory Module Digit Boards

All data handling is accomplished on the two identical digit boards found in each core memory module. Because one core memory word is 17-bits long and each digit board is capable of handling nine bits of data, the second digit board has one unused circuit. Figure II-46 shows the digit boards of a memory module, and Figure II-47 shows the circuit used for data bit one of a memory module.

Each digit board contains nine data latches for the temporary storage of data to be written into memory or read out of memory. Digit board 1 receives and stores nine data lines (SMDTM01 through SMDTM09) from the processor, and sends data back to the processor on MPM lines 01 through 09. Digit board 2 receives and stores the other eight bits of data from the processor. The data latches receive data lines SMDTM10 through SMDTM16 and parity bit LIDTM17 and return data to the processor over data lines MPM10 through MPM17.

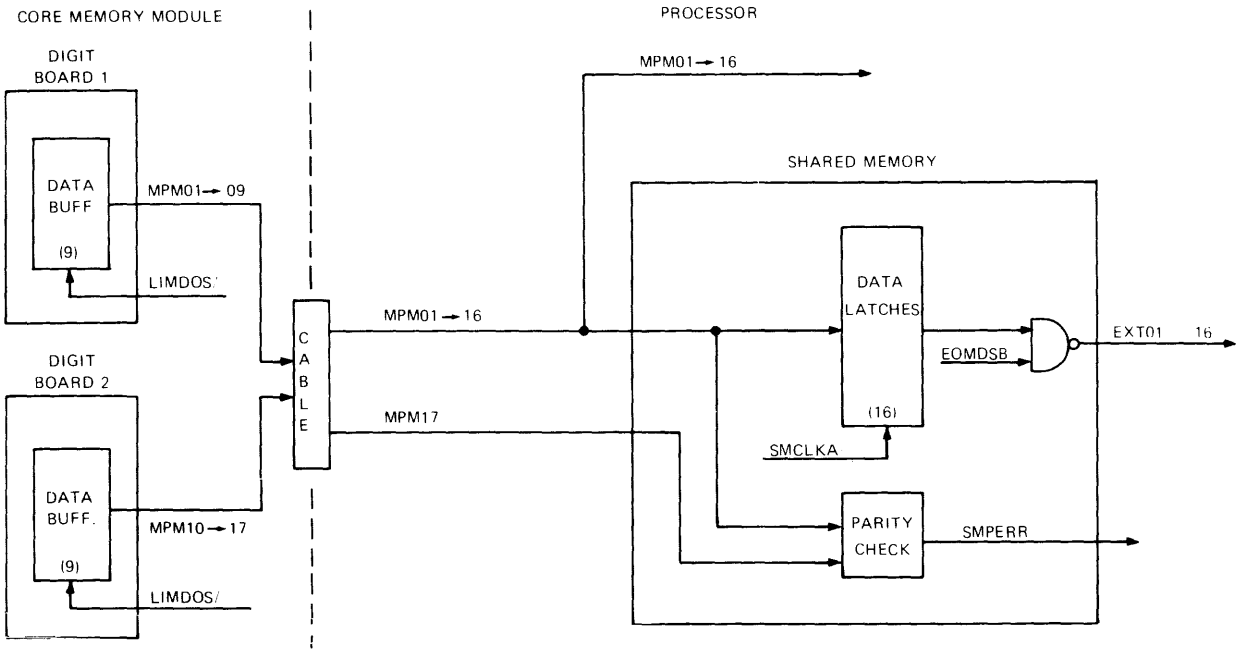


Fig. II-45. DATA TRANSFER FROM CORE MEMORY

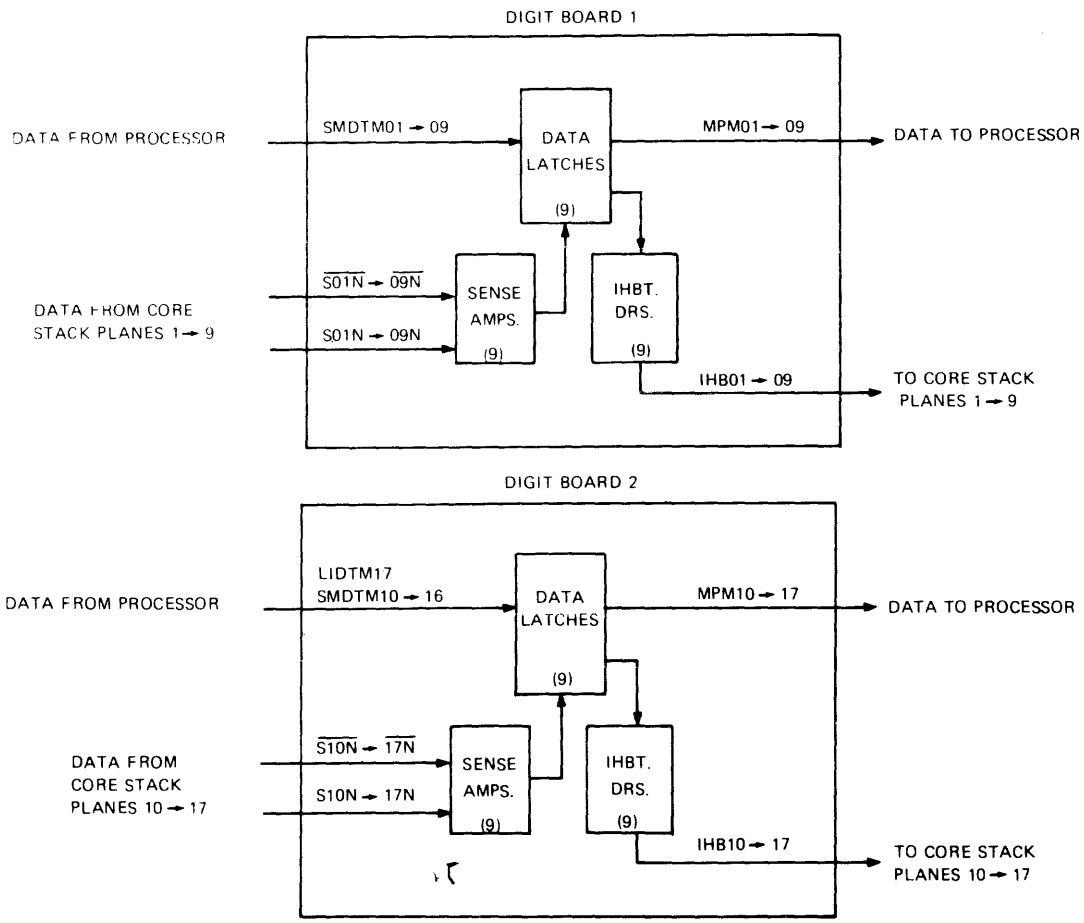


Fig. II-46. CORE MEMORY MODULE DIGIT BOARDS

Functional Detail

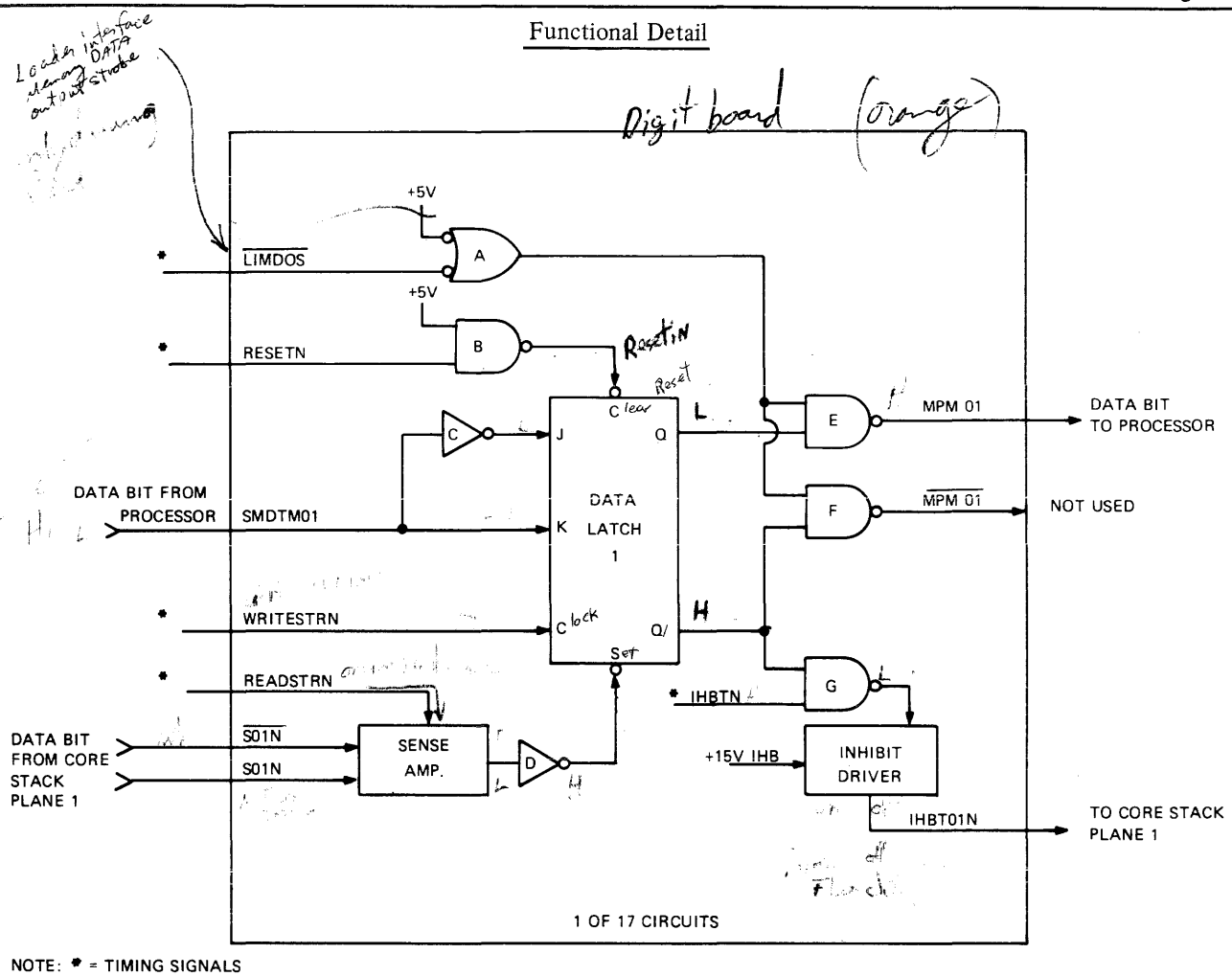


Fig. II-47. DATA BIT ONE CIRCUIT OF A MEMORY MODULE

The digit boards also contain the inhibit drivers, which are used to control the writing of data into the cores. On digit board 1, the output of the data latches control nine inhibit drivers. Outputs IHBT01 through IHBT09 are sent to the core stack to control writing in planes 1 through 9, respectively. On digit board 2, the eight data latch outputs are used to control eight inhibit drivers. Inhibit driver outputs IHBT10 through IHBT17 are sent to the core stack to control writing in planes 10 through 17, respectively.

The sense amplifiers are also contained on the digit boards. The nine sense amplifiers on digit board 1 receive the core outputs from planes 1 through 9 in the true state (S01N through S09N) and the false state ($\overline{\text{S01N}}$ through $\overline{\text{S09N}}$), respectively. If a 1-data bit is read, a true or false signal occurs, and the sense amplifier output sets the corresponding data latch. On digit board 2, the sense amplifiers receive the true states (S10N through S17N) and the false states ($\overline{\text{S10N}}$ through $\overline{\text{S17N}}$) from core planes 10 through 17, respectively. If a 1-data bit is read, a true or false signal occurs, and the sense amplifier output sets the corresponding data latch. If a 0-bit is read, neither signal occurs, and the corresponding data latch remains reset.

DATA PARITY GENERATION AND CHECKING

Parity Generation for Memory Write Operation

As shown in Figure II-48, odd parity is generated on the shared memory boards in the processor. Parity is generated from the SMDTM01/ through SMDTM16/ data signals while data is being transferred to core memory.

SMDTM01/ through SMDTM08/ are gated by exclusive OR gates A through G to make up signal SMPGEN1. SMDTM09/ through SMDTM16/ are gated by exclusive OR gates H through P to produce signal SMPGEN2. SMPGEN1 and SMPGEN2 are inputs to exclusive OR gate R, whose output is inverted through NAND gate S on an LIC board. The resultant output is LI3DTM17, which is the parity bit data bit-17 sent to core memory.

If the number of 1-bits is even, both SMPGEN1 and SMPGEN2 are either high or low. Identical inputs to exclusive OR gate R produce a low output. This low output is inverted by NAND gate S to make LI3DTM17 high and add a 1-bit to the data. Thus, the total number of 1-bits is odd.

If the number of 1-bits is odd, SMPGEN1 and SMPGEN2 are opposite in state (one is high and the other is

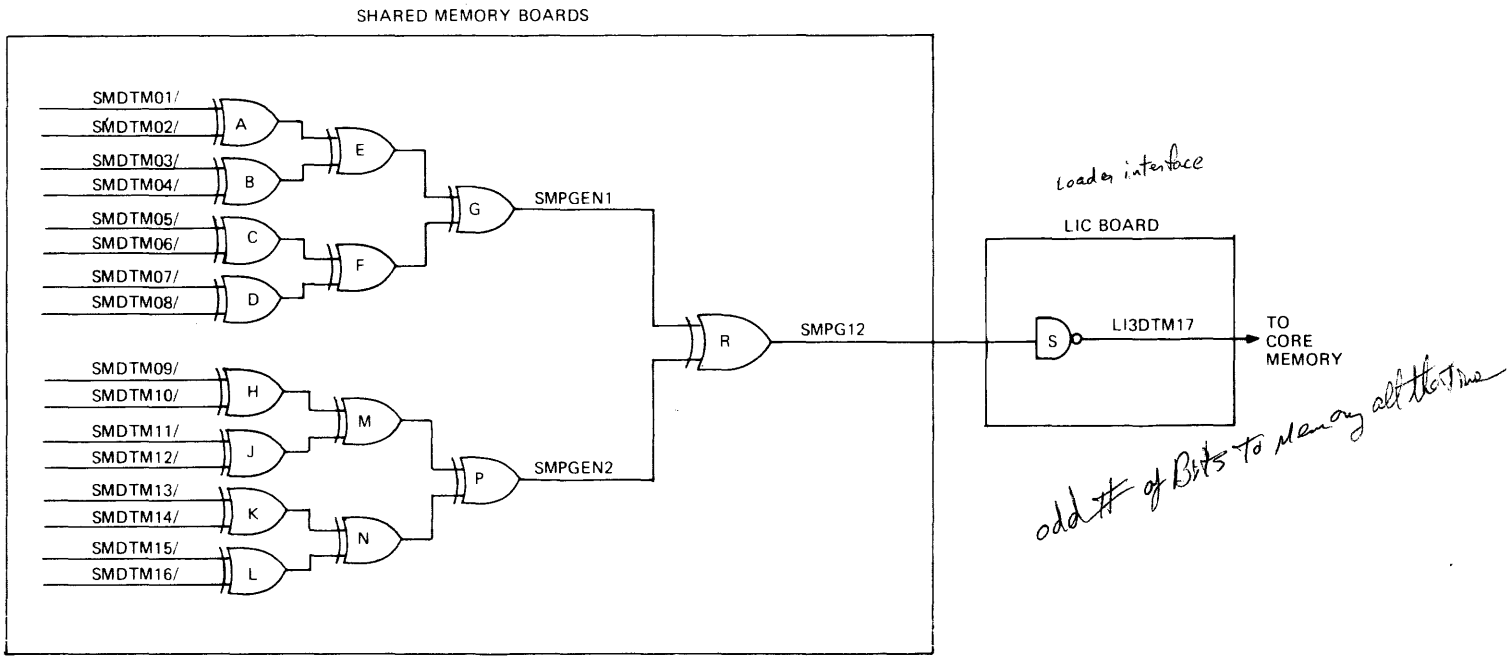


Fig. II-48. DATA PARITY GENERATION

low). Opposite inputs to exclusive OR gate R produce a high output. This output is inverted by NAND gate S and makes LI3DTM17 low, leaving the total number of 1-bits odd.

Parity Checking for Memory Read Operation

As shown in Figure II-49, parity is checked on the shared memory boards in the processor while data is being transferred from core memory into the processor. Parity is checked by generating new parity from MPM lines 01 through 16 in the same manner as the parity bit is generated for memory write operation. The new parity is compared to the parity bit read from core to determine if it is correct.

MPM lines 01 through 08 are gated by exclusive OR gates A through G to produce signal SMPCHK1. MPM09 through MPM16 are gated by exclusive OR gates H through P to produce signal SMPCHK2. SMPCHK1 and SMPCHK2 are inputs to exclusive OR gate R, whose output is gated by exclusive OR gate S with the parity bit from memory (MPM17). The output of exclusive OR gate S is the D input to the shared-memory parity error flip-flop. When there is no parity error, the D input should be high and keep the flip-flop set. Output Q/ is low and the shared-memory parity error signal SMPERR is false.

If MPM01 through MPM16 are an even number of 1-bits, SMPCHK1 and SMPCHK2 are both high or both low. Identical inputs to exclusive OR gate R produces a low output. If the parity is correct, MPM17 should be high (1-bit). The high and low through exclusive OR gate S produce a high output to the D input of the parity error flip-flop, thus keeping it set. A low input to reset the latch and produce a parity error (SMPERR is true) can be produced in two ways. First if the parity bit was bad (MPM is low), the two low inputs into exclusive OR gate S result in a low output that resets the parity error flip-flop. Thus, signal SMPERR goes true. Secondly, if an odd number of bits were picked up or dropped on MPM lines 01 through 16, SMPCHK1 and SMPCHK2 would be opposite inputs to exclusive OR gate R and produce a high output. This high is gated in exclusive OR gate S with the high on MPM17 and produces a low output from gate S to reset the flip-flop. Again, signal SMPERR goes true.

If MPM lines 01 through 16 have an odd number of 1-bits, SMPCHK1 and SMPCHK2 are opposites. The output of exclusive OR gate R is high, and MPM17 is low (0-bit) if parity is correct. The low and high input to exclusive OR gate S produces a high out to keep the parity error flip-flop set.

A parity error occurs if the parity bit (MPM17) is incorrect. (MPM17 should be low, but is high.) The two highs into exclusive OR gate S produce a low output to reset the flip-flop and make SMPERR true. Also, if an odd number of bits were picked up or dropped, SMPCHK1 and SMPCHK2 would be alike. The output of exclusive OR gate R is low, and because MPM17 is low into exclusive OR gate S, a low output is produced to again reset the flip-flop and make SMPERR true.

CORE MEMORY ADDRESS ERROR DETECTION

Address errors are checked for on the processor shared memory boards. Address errors occur when the

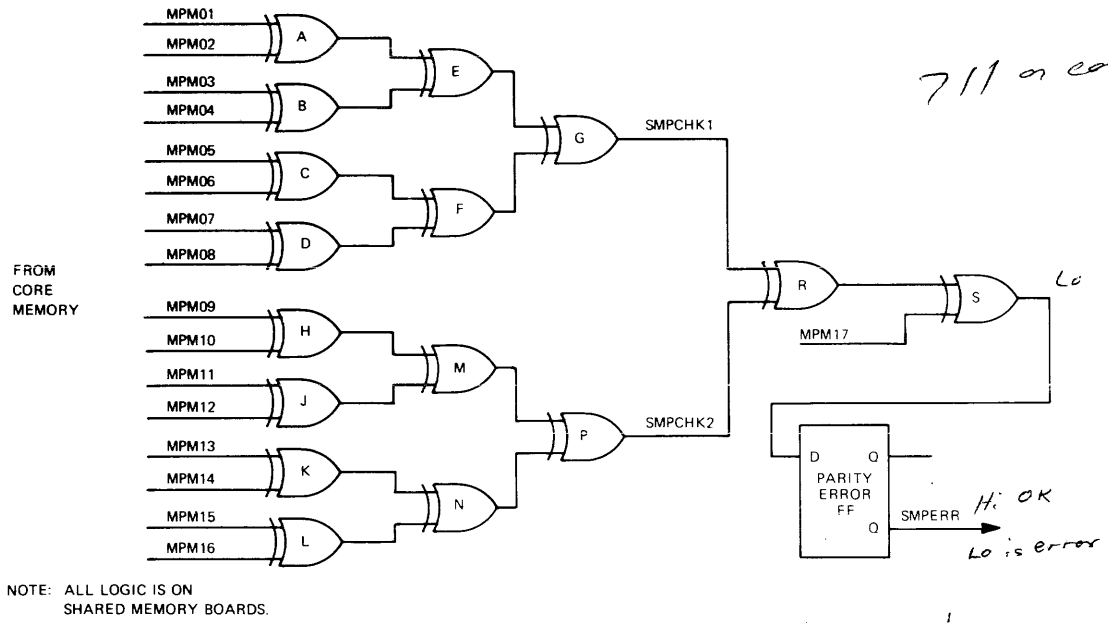


Fig. II-49. PARITY ERROR DETECTION

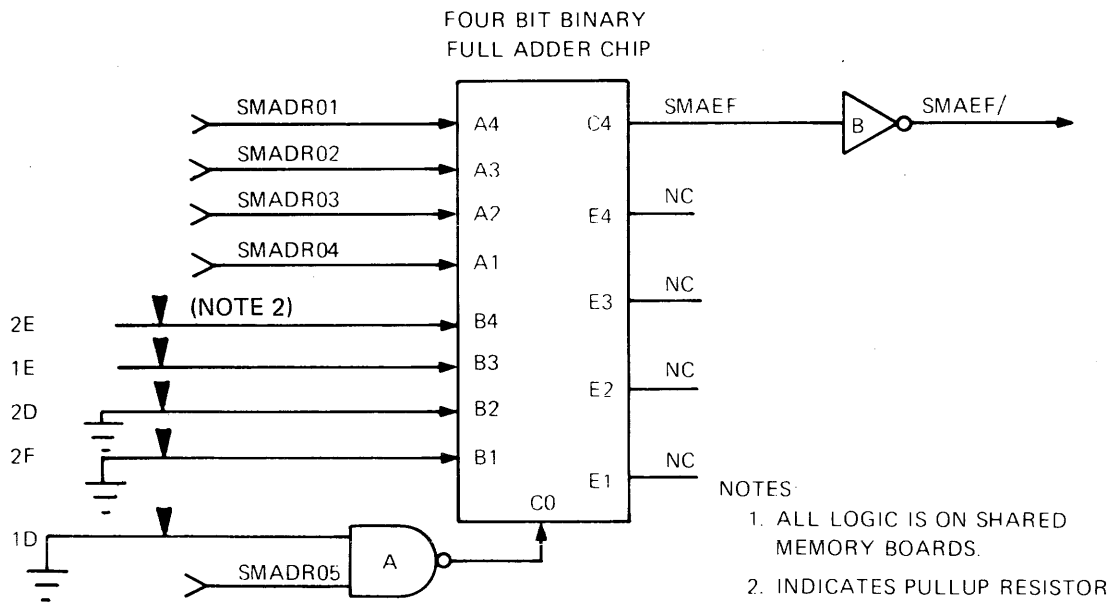


Fig. II-50. ADDRESS ERROR DETECTION

address exceeds the amount of core memory installed in the system. The address lines are compared to a hard-wired backplane address limit. This limit is wired during installation of the processor and must be changed whenever a core memory module is added or removed. (Refer to Section VI.)

Figure II-50 shows the address error detection scheme. The comparison is done by a four-bit binary full adder chip, which is capable of adding two hexadecimal digits and handling all internal carries during an add operation. Shared memory address lines 01 through 04 comprise 1-digit input to the adder chip on pins A4, A3, A2, and A1. The other digit input on B4, B3, B2, and B1 is the result of the address limit installed on the backplane. CO is the carry input to the chip and is controlled by shared memory address line 05 and the backplane wired limit. E4, E3, E2, and E1 (binary bit outputs) are not used. C4 is the most significant carry output from the addition of the two digits. If a carry is produced from the addition of the address lines and the wired limit, C4 is high, and the shared memory address error (SMAEF) signal is true.

As shown in the following example, the backplane is wired for 32 K-bytes or 16 K-words. A 16 K-word capacity requires two full core memory modules with a maximum hexadecimal address of 2FFF. An example of addition using the maximum address is as follows:

A4, A3, A2, A1 =	0 0 1 0	2(FFF)
B4, B3, B2, B1 =	1 1 0 0	Backplane
	1	CO is high
C4 = 0	1 1 1 1	

In this example, the comparison of the maximum address with the backplane limit by addition does not generate an address error because a C4 is 0 (zero).

An example of addition using an error address is as follows:

	1 1 1	Internal carries
A4, A3, A2, A1 =	0 0 1 1	3 (000 through FFF)
B4, B3, B2, B1 =	1 1 0 0	Backplane
	1	CO is high
C4 = 1	0 0 0 0	

In this example, the address exceeded the backplane limit and, as a result of the addition, C4 equals a 1. Thus SMAEF goes true.

LOADER INTERFACE CONTROLS (LIC)

In the B 700 Systems there are two types of Loader Interface Controls (LIC's); one uses the paper tape memory loader (as in the B 711 Systems) to load paper tape program data to memory, and the other use the 80-Column Card Reader (as in the B 771 Systems) to load card program data to memory.

Paper Tape Memory Loader

The paper tape memory Loader Interface Control is contained on cards LI3 and LI4. LI3 contains primarily the control circuitry, and LI4 contains the buffering, storage, and data-characters gating circuits. (See Figure II-51.) The Loader Interface Control is designed to load four hexadecimal digits (one word) of program data to core memory, beginning at address zero, incrementing with each new word of data and stopping after reading and storing a stop code (4000) from paper tape. (See Figure II-52.)

Each two frames of paper tape equal one word of data. Every ninth frame of data is a longitudinal redundancy character used to check the validity of the previous eight frames. A start coder (66) must be decoded before any data may be stored in memory. The Tape Character Counter then tallies the frames of data 1 through 9. Three memory cycles are requested at the end of every two frames of data (example TC=2, 4, 6, or 8); the first memory cycle writes the data into core; the remaining two memory cycles read back the stored data to check the vertical parity validity of each data word.

The loading of data to memory may be terminated by an LRC error (LILRCER) or Vertical Parity error (SMPERR). Flow chart Figure II-53 and timing diagram Figure II-54 illustrate the use of the logic circuitry within the Loader Interface Control and the Memory Loader.

Card Reader Memory Loader

The 80-Column Card Loader interface consists of the LI5 and LI6 cards. These circuit cards interface the card reader I/O control with the core memory for direct loading of card program data into memory. (See Figure II-55.)

The loading begins whenever the load switch on the processor is stored in the load position (illuminated red). When the Load flip-flop is set, the start card cycle level is generated to feed cards. Table II-7 lists the predetermined card format that allows sequence checking and Longitudinal redundancy checking (LRC), along with the usual memory cycle error checking that exists in the shared memory logic circuits. Sequence checking is made in column 3 only, beginning with value 1 and returning to value 0 after exceeding a count of 9. Longitudinal parity checking employs the use of an LRC check register which is complemented with any ONE (1) bits of the output of the packed Hexadecimal decoder. The LRC Register is enabled only for columns 9 through 80. The contents of the LRC Register should be equal to zero (0) at the end of each card if columns are read satisfactorily. Table II-8 lists the loader card deck code conversions. The LI80F flip-flop indicates the last column of each card. The Stop flip-flop indicates that a one punch was read from column 13 of the end card. Timing chart Figure II-56 and block diagram Figure II-55 illustrate the step-by-step logical progression through the Card Reader Loader Interface Circuitry. Memory cycles are generated after reading two columns of data, beginning at column 17 of each card. The memory address is incremented after read-checking the column data previously written. This provides confidence in the memory program data. The detection of any loader error terminates the load and requires a complete restart of card decks to be loaded.

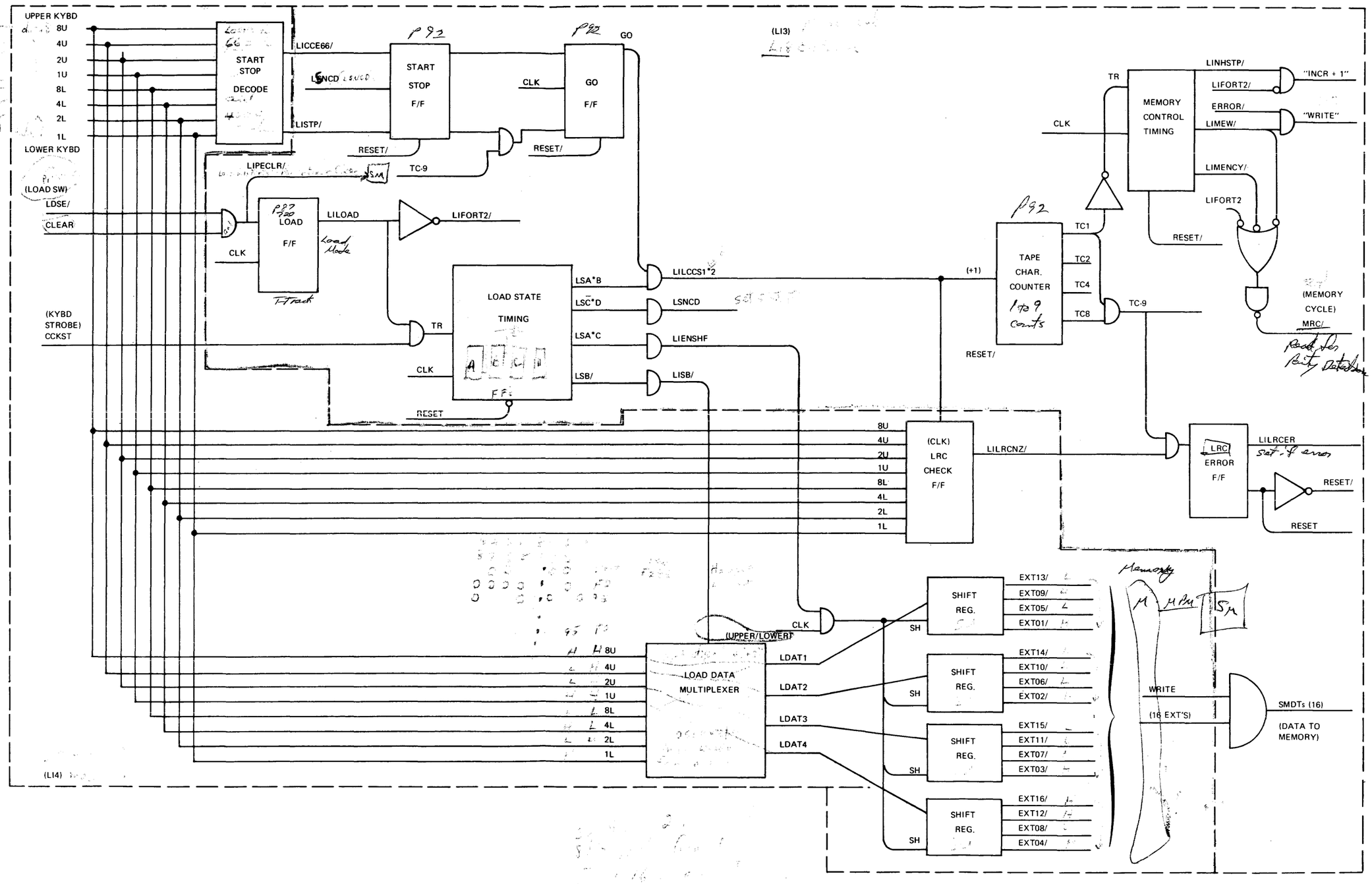


Fig. II-51. PAPER TAPE MEMORY LOADER INTERFACE CONTROL (LIC), BLOCK DIAGRAM

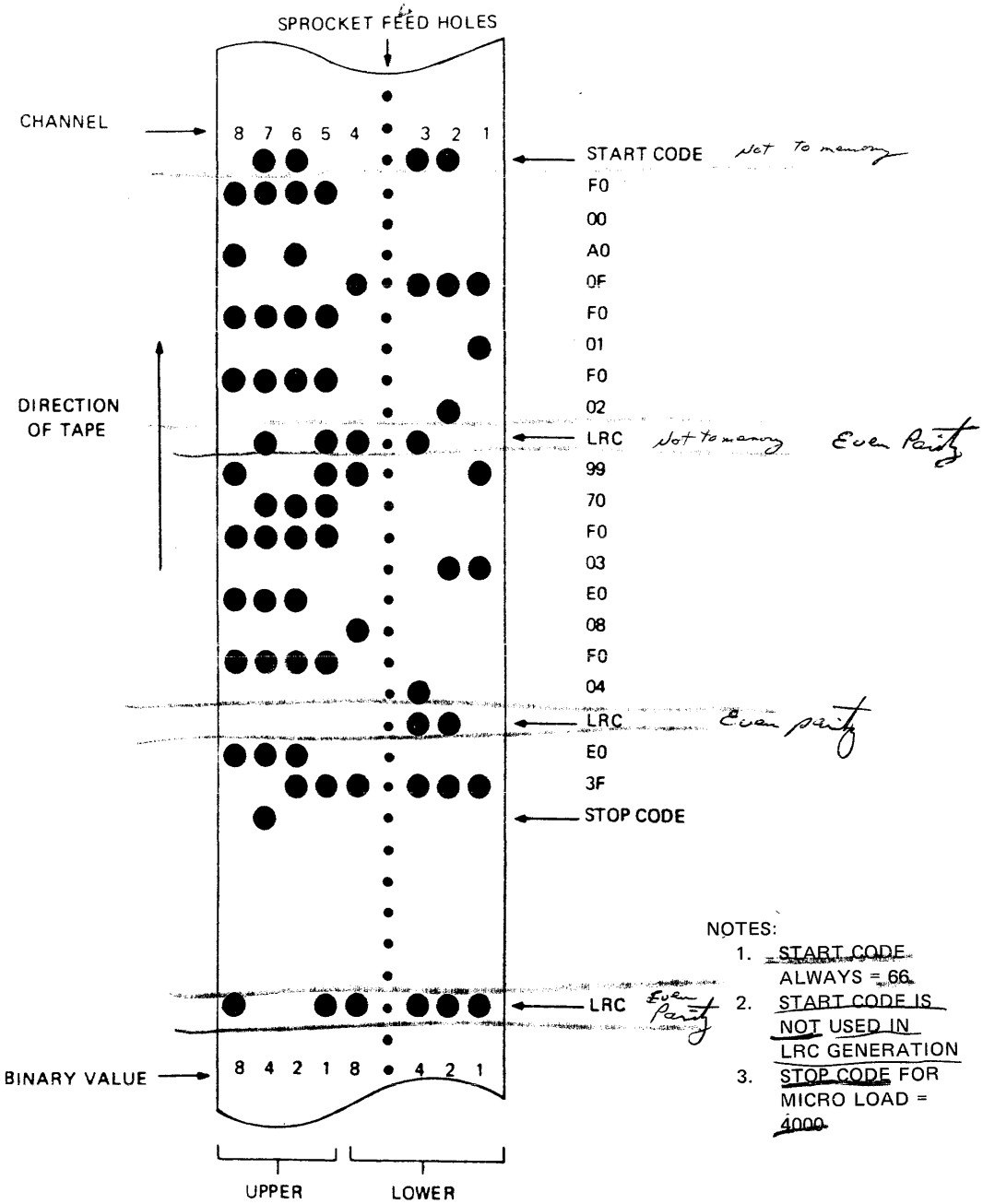


Fig. II-52. PUNCHED-PAPER TAPE COMPACT OBJECT CODE

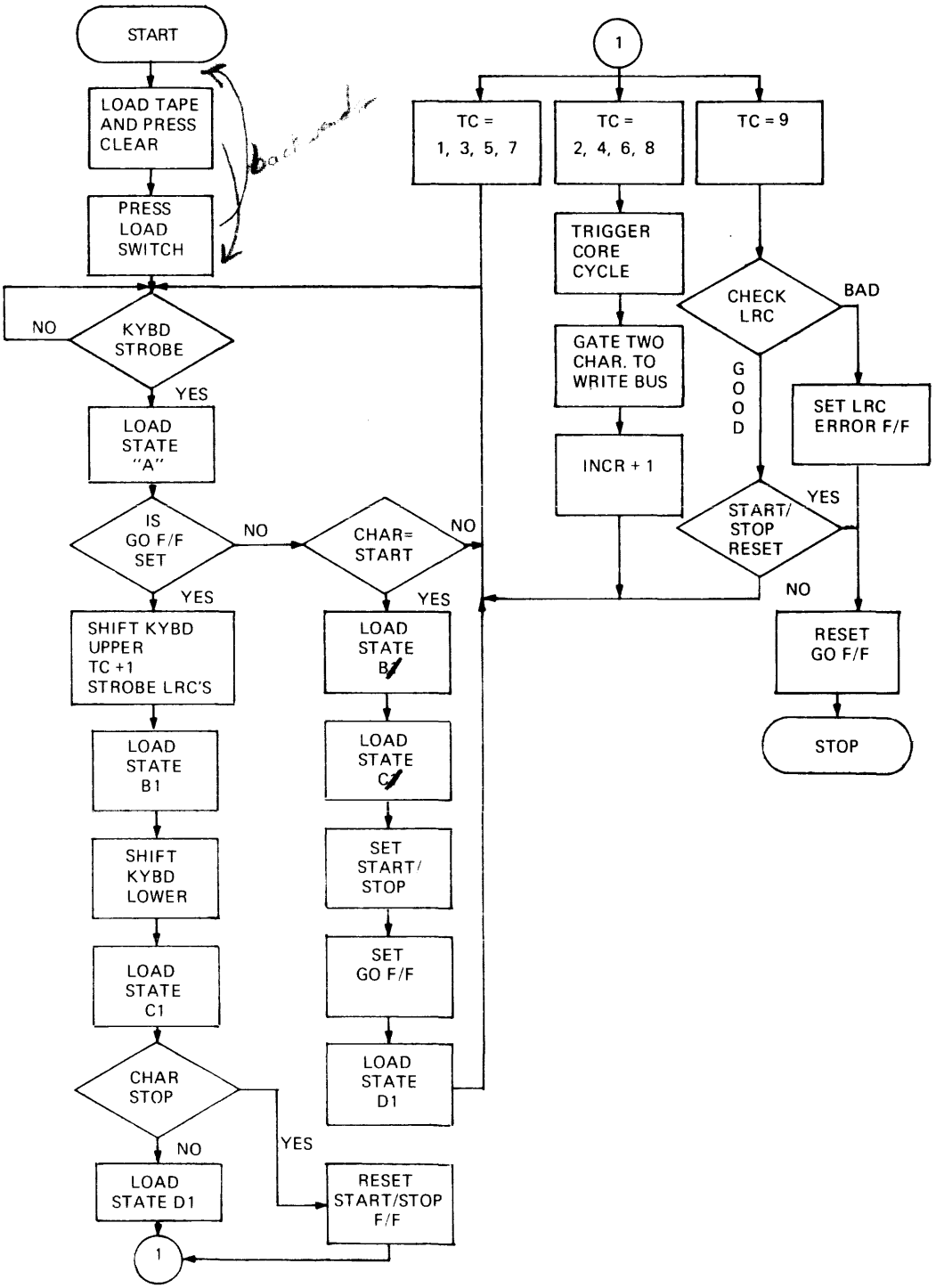


Fig. II-53. LOADER INTERFACE CONTROL (LIC) FLOW CHART FOR PAPER TAPE MEMORY LOADER

Functional Detail

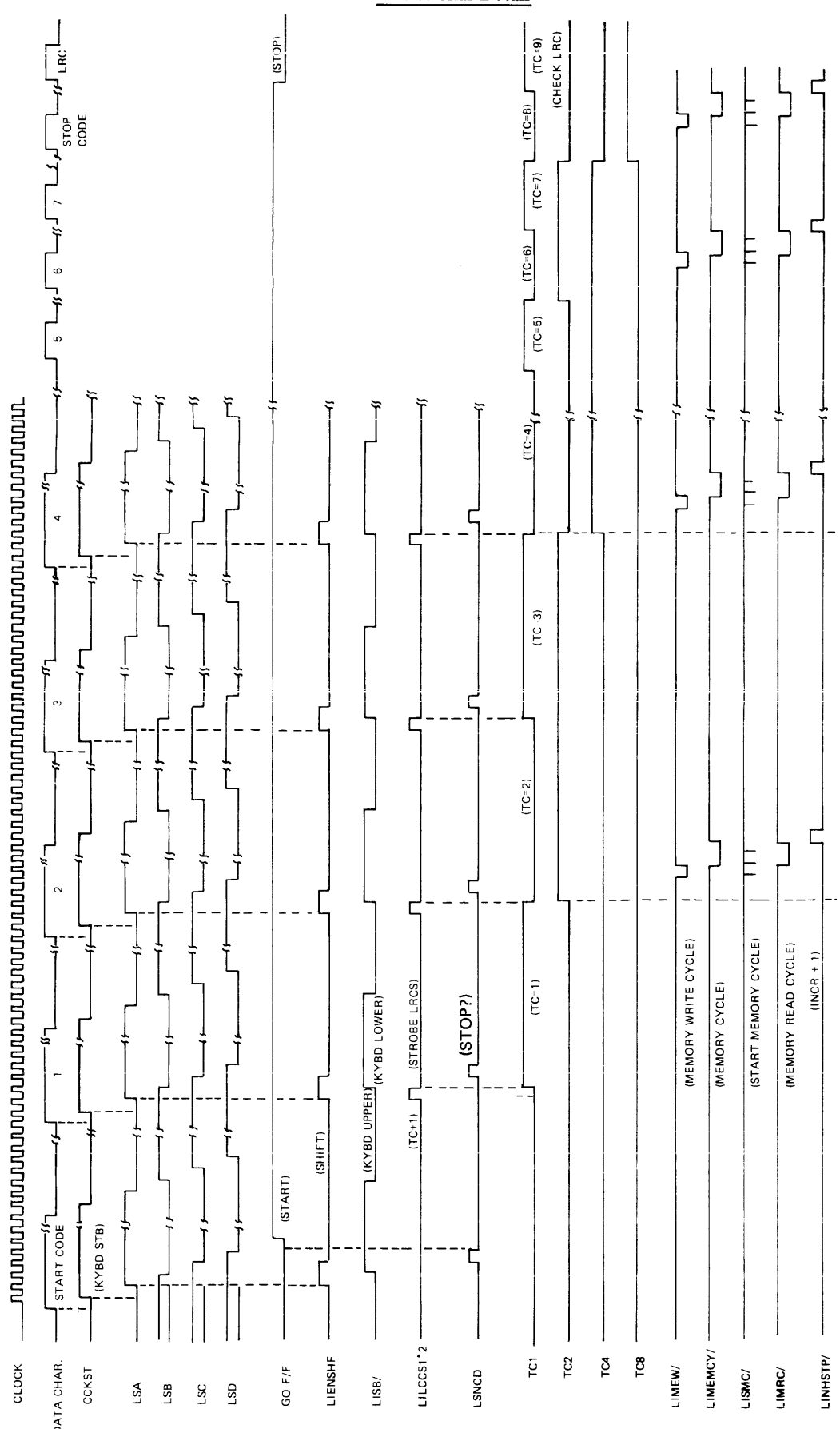


Fig. II-54. PAPER TAPE MEMORY LOADER INTERFACE CONTROL (LIC), TIMING DIAGRAM

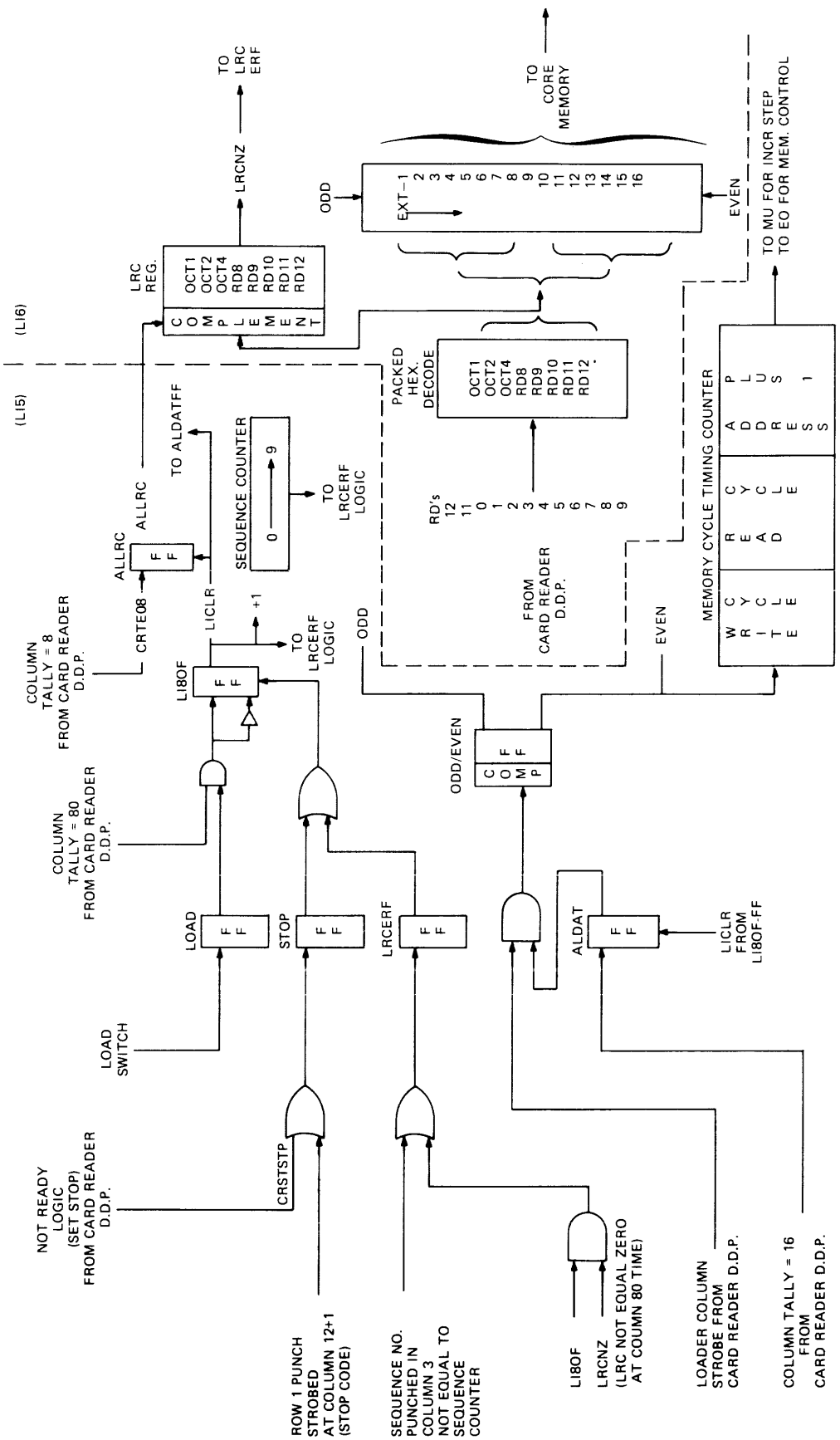


Fig. II-55. CARD READER MEMORY LOADER INTERFACE CONTROL (LIC), BLOCK DIAGRAM

TABLE II-7. CARD FORMAT

Column	Function
1-3	Sequence number: specifies the sequential number of the card in relation to the card deck. Consists of three columns. Each representing a decimal digit. Column 1 designates hundreds, column 2 designates tens, and column 3 designates units.
4-8	Not used.
9	LRC: Contains the longitudinal redundancy character (even parity) which is calculated from all following columns.
10, 11	Not used.
12	Word numbers: specifies the number of 16-bit words on the card. (Not used by loader)
13	Stop: A punch in row 1 of column 13 specifies that the card is a stop card, indicating that the previous card was the last card of the deck. The absence of a punch in row 1 specifies that the card is a data card.
14	Not used.
15, 16	Start address: Represents the direct MPM starting address in 4-bit octal code. Column 15 is the most significant column (not used by loader). The loader start address is always zero.
17-80	Data: A punch in row 1 of column 13 specifies that the card is a stop card and that columns 23 and 24 specify the number of cards in the card deck. The absence of a punch in row 1 of column 13 specifies that the card is a data card and that columns 17 through 80 contain data. Blank columns in the data field are loaded into MPM as zeros.

TABLE II-8. CODE CONVERSIONS, LOADER CARD DECK

INT. CODE	CARD CODE	INT. CODE	CARD CODE	INT. CODE	CARD CODE	INT. CODE	CARD CODE
00	Blank	20	0	40	11	60	11-0
01	1	21	0-1	41	11-1	61	11-0-1
02	2	22	0-2	42	11-2	62	11-0-2
03	3	23	0-3	43	11-3	63	11-0-3
04	4	24	0-4	44	11-4	64	11-0-4
05	5	25	0-5	45	11-5	65	11-0-5
06	6	26	0-6	46	11-6	66	11-0-6
07	7	27	0-7	47	11-7	67	11-0-7
08	8	28	0-8	48	11-8	68	11-0-8
09	8-1	29	0-8-1	49	11-8-1	69	11-0-8-1
0A	8-2	2A	0-8-2	4A	11-A-2	6A	11-0-8-2
0A	8-2	2A	0-8-2	4A	11-8-2	6A	11-0-8-3
0B	8-3	2B	0-8-3	4B	11-8-3	6B	11-0-8-3
0C	8-4	2C	0-8-4	4C	11-8-4	6C	11-0-8-4
0E	8-6	2E	0-8-6	4E	11-8-6	6E	11-0-8-6
0F	8-7	2F	0-8-7	4F	11-8-7	6F	11-0-8-7
10	9	30	0-9	50	11-9	70	11-0-9
11	9-1	31	0-9-1	51	11-9-1	71	11-0-9-1
12	9-2	32	0-9-2	52	11-9-2	72	11-0-9-2
13	9-3	33	0-9-3	53	11-9-3	73	11-0-9-3
14	9-4	34	0-9-4	54	11-9-4	74	11-0-9-4
15	9-5	35	0-9-5	55	11-9-5	75	11-0-9-5
16	9-6	36	0-9-6	56	11-9-6	76	11-0-9-6
17	9-7	37	0-9-7	57	11-9-7	77	11-0-9-7
18	9-8	38	0-9-8	58	11-9-8	78	11-0-9-8
19	9-8-1	39	0-9-8-1	59	11-9-8-1	79	11-0-9-8-1
1A	9-8-2	3A	0-9-8-2	5A	11-9-8-2	7A	11-0-9-8-2
1B	9-8-3	3B	0-9-8-3	5B	11-9-8-3	7B	11-0-9-8-3
1C	9-8-4	3C	0-9-8-4	5C	11-9-8-4	7C	11-0-9-8-4
1D	9-8-5	3D	0-9-8-5	5D	11-9-8-5	7D	11-0-9-8-5
1E	9-8-6	3E	0-9-8-6	5E	11-9-8-6	7E	11-0-9-8-6
1F	9-8-7	3F	0-9-8-7	5F	11-9-8-7	7F	11-0-9-8-7

TABLE II-8. CODE CONVERSIONS, LOADER CARD DECK (CONT'D.)

INT. CODE	CARD CODE	INT. CODE	CARD CODE	INT. CODE	CARD CODE	INT. CODE	CARD CODE
80	12	A0	12-0	C0	12-11	E0	12-11-0
81	12-1	A1	12-0-1	C1	12-11-1	E1	12-11-0-1
82	12-2	A2	12-0-2	C2	12-11-2	E2	12-11-0-2
83	12-3	A3	12-0-3	C3	12-11-3	E3	12-11-0-3
84	12-4	A4	12-0-4	C4	12-11-4	E4	12-11-0-4
85	12-5	A5	12-0-5	C5	12-11-5	E5	12-11-0-5
86	12-6	A6	12-0-6	C6	12-11-6	E6	12-11-0-6
87	12-7	A7	12-0-7	C7	12-11-7	E7	12-11-0-7
88	12-8	A8	12-0-8	C8	12-11-8	E8	12-11-0-8
89	12-8-1	A9	12-0-8-1	C9	12-11-8-1	E9	12-11-0-8-1
8A	12-8-2	AA	12-0-8-2	CA	12-11-8-2	EA	12-11-0-8-2
8B	12-8-3	AB	12-0-8-3	CB	12-11-8-3	EB	12-11-0-8-3
8C	12-8-4	AC	12-0-8-4	CC	12-11-8-4	EC	12-11-0-8-4
8D	12-8-5	AD	12-0-8-5	CD	12-11-8-5	ED	12-11-0-8-5
8E	12-8-6	AE	12-0-8-6	CE	12-11-8-6	EE	12-11-0-8-6
8F	12-8-7	AF	12-0-8-7	CF	12-11-8-7	EF	12-11-0-8-7
90	12-9	B0	12-0-9	D0	12-11-9	F0	12-11-0-9
91	12-9-1	B1	12-0-9-1	D1	12-11-9-1	F1	12-11-0-9-1
92	12-9-2	B2	12-0-9-2	D2	12-11-9-2	F2	12-11-0-9-2
93	12-9-3	B3	12-0-9-3	D3	12-11-9-3	F3	12-11-0-9-3
94	12-9-4	B4	12-0-9-4	D4	12-11-9-4	F4	12-11-0-9-4
95	12-9-5	B5	12-0-9-5	D5	12-11-9-5	F5	12-11-0-9-5
96	12-9-6	B6	12-0-9-6	D6	12-11-9-6	F6	12-11-0-9-6
97	12-9-7	B7	12-0-9-7	D7	12-11-9-7	F7	12-11-0-9-7
98	12-9-8	B8	12-0-9-8	D8	12-11-9-8	F8	12-11-0-9-8
99	12-9-8-1	B9	12-0-9-8-1	D9	12-11-9-8-1	F9	12-11-0-9-8-1
9A	12-9-8-2	BA	12-0-9-8-2	DA	12-11-9-8-2	FA	12-11-0-9-8-2
9B	12-9-8-3	BB	12-0-9-8-3	DB	12-11-9-8-3	FB	12-11-0-9-8-3
9C	12-9-8-4	BC	12-0-9-8-4	DC	12-11-9-8-4	FC	12-11-0-9-8-4
9D	12-9-8-5	BD	12-0-9-8-5	DD	12-11-9-8-5	FD	12-11-0-9-8-5
9E	12-9-8-6	BE	12-0-9-8-6	DE	12-11-9-8-6	FE	12-11-0-9-8-6
9F	12-9-8-7	BF	12-0-9-8-7	DF	12-11-9-8-7	FF	12-11-0-9-8-7

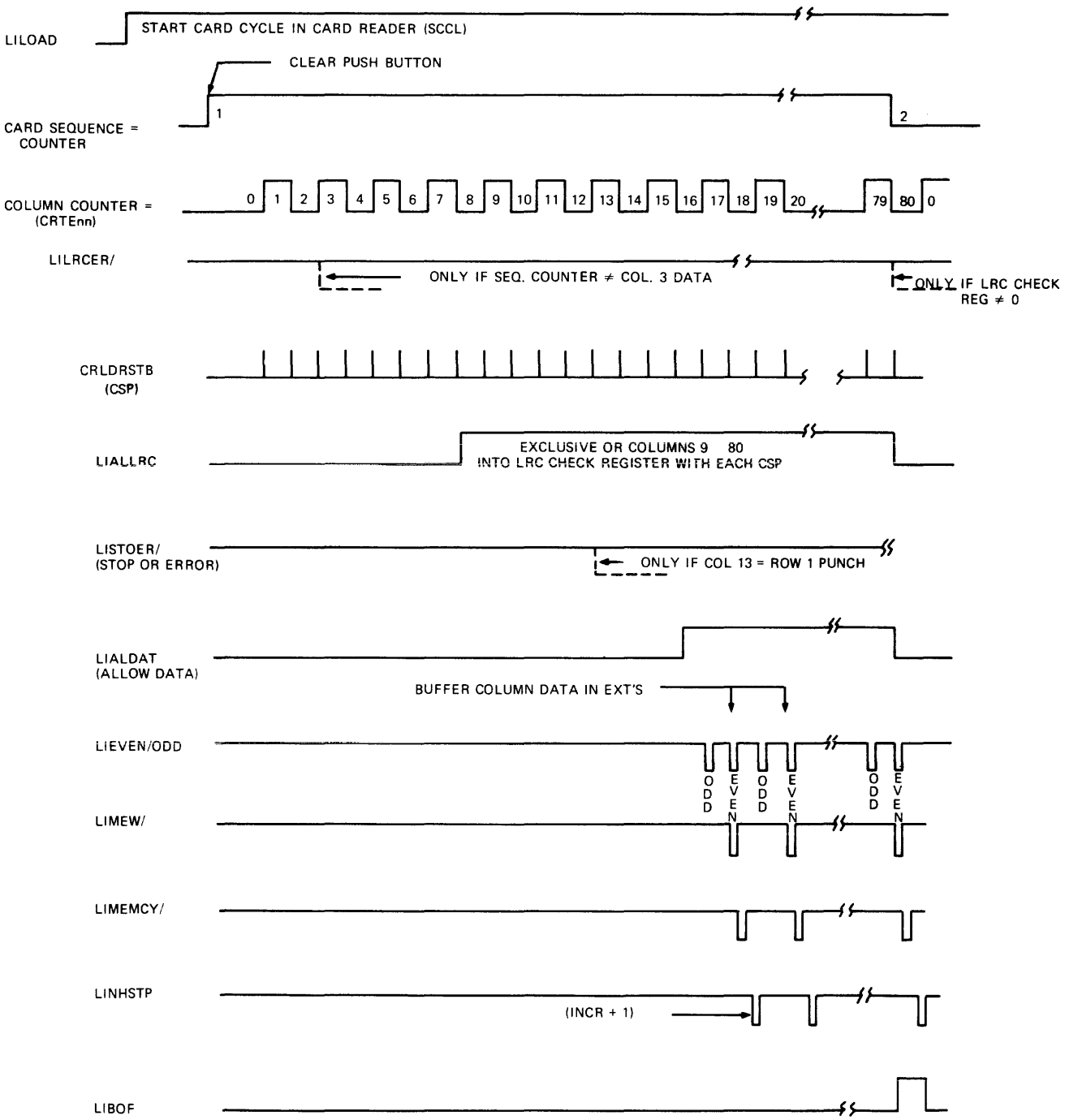


Fig. II-56. CARD READER MEMORY LOADER INTERFACE CONTROL (LIC), TIMING DIAGRAM

I/O DEVICE CONTROL

GENERAL

The Processor has control of each device through the Port Select Unit (PSU) and Input/Output Controls (IOC's or DDP's). Each device is different and requires its own unique I/O Control; however, the Processor addresses and communicates with devices in a similar manner. Figure II-57 shows the I/O device control interface.

The Memory Information Register (MIR) is the output from the Processor and it is common to all devices. Also common to all devices is the External Bus (EXT), which is the input to the Processor by way of the B Register. Because MIR and EXT lines are shared, it is necessary to select or address each I/O Control separately and only one at a time. This is one function of the PSU. Another function of the PSU is to enable the I/O Controls to receive information from the devices (Device Read) or send information to them (Device Write). Interrupts, and their priority, is the last function of the PSU.

PORT SELECTION (FIGURE II-57)

As discussed previously, one function of the PSU is I/O Control addressing. There are eight possible addresses. The address of the I/O Control is determined by its location in the logic rack. Each specific I/O Control location has a corresponding cable connection for the device. (Refer to Section VI.) The priority of the device is determined by the location of the control and device. The console or SPO **must** be in location (or port) 8. This is fixed because the console or SPO has the highest priority and it also has a unique set of I/O Control cards and cables. Most other devices can be utilized from any port, as long as the hardware configuration reflects their location.

DEVICE ADDRESSING

Device Addressing originates in the Base Registers (BR1 or BR2). (See Figure II-58.) It is placed there by the microprogram when it is necessary to use a device. External Operation Bits (EOB) 51 through 53 select device operation and Device Read (DR) or Device Write (DW). Nanomemory bit-54 (NMN54) selects BR1 or BR2 for device addressing. A device becomes addressed when the port is selected by sending the device address in BR1 or BR2 on the Output Select Lines (OS 5/, 6/, 7, and 8) to the PSU. This is done with a Device Read or Device Write nanoinstruction. The PSU is composed of two Port Selector Cards. Port Selector PS1-1 addresses ports 1 through 4 and Port Selector PS1-2 addresses ports 5 through 8. Each Port Selector Card is identical. The -1 or -2 designation is determined by the card location in the logic rack. Device addresses, binary 0 through 7, correspond to ports 1 through 8.

Figure II-59 illustrates the execution of a Device Write from BR2 (DW2) to the console. The console address is 8, but since 0 is significant, it is represented binarily as 7 in the least significant bits of the BR. MUOS06/, when low selects PS1-2, which controls ports 5 through 8. MUOS07 and MUOS08, when high, select the fourth port controlled by the selected Port Selector. The output of the BR in conjunction with the EOB's, develop one active signal from the PSU. PSWRIT8/ becomes low active to select the console I/O Control when DW2 is executed.

SENDING INFORMATION TO AN I/O CONTROL

A device write (DW) nanoinstruction is also used to send an I/O Control a control word or data word. An example of a word format is illustrated in Figure II-60. A control word is constructed in MIR by the microprogram. Its purpose is to initiate an I/O operation. For example, if a customer program requires an operator input from the console keyboard, the microprogram builds a control word to enable the logic to accept keyboard inputs. A control word defines the function to be performed. When a control word is sent to the I/O Control, MUOS01 must be set. (See Figure II-59.) This is the instruction bit and it is sent to the I/O Control when the Device Address is sent to the PSU. (See Figure II-61A.) In order to send a control word to the I/O Control, a DW must be executed. The device address from BR selects the I/O Control through the PSU. The instruction bit indicates that the information in MIR is a control word, as opposed to a data word.

RECEIVING A DATA WORD FROM AN I/O CONTROL

Figure II-60 illustrates a data word format. In the case of the console, the keyboard eight-bit key code appears to the I/O Control as a data word. When a key is depressed, this code is sent to the Processor by a Device Read (DR) nanoinstruction. (PSREAD8/ is active.) Another requirement to read data, instead of sending a control word, is that the instruction bit must be low. (See Figures II-59 and II-61.) The Processor receives an interrupt when the key is depressed, and this is what indicates activity from the keyboard.

INTERRUPTS

It is not until an interrupt is generated from a keyboard that a DR is executed by the Processor. The effect of this is shown in Figure II-62. Depressing a key generates a Data Interrupt (DINT) in the I/O Control. Due to the fact that the console is **selected**, the PSU sends a Solicited Request (SRQ) to the Condition Register in the Processor. This condition is expected, because the control word enabled the keyboard logic. The microprogram tests for the SRQ by means of a nanoinstruction. When it is active, because a key was depressed, DR is executed. DR not only retrieves data from the I/O Control, it also resets DINT so it can be set by the next key activated.

Figure II-63 illustrates the logic to generate an SRQ. When a key is depressed, DINT8/ from the console I/O Control is low active into the PSU. At this time, PSWRIT8/

is low active, so Q3/ is low. The outputs at gate pins D1-8, D1-11 and B3-8 are high. Because PSWRIT8/ is active, the device is selected. The combined inputs of DINT8/ and PSWRIT8/ at chip D7 causes a low form pin 7. PSSRQ/ goes low active. This is the result of a DINT from a selected device which would be followed by a DR in the case of the console keyboard being enabled.

Another type of interrupt is a Status Interrupt (SINT). See Figure II-60, the console status word relates the condition or status of the device and can be interrogated by the Processor at any time. Interrupt Not Honored (INH) is active if a key was depressed on the console and the previous key code was not read. INH generates a SINT. Figure II-62 shows SINT as an input to the PSU, just like DINT. The PSU sends an Unsolicited Request (URQ) to the Condition Register in the Processor if the device is selected. The logic for this operation (Figure II-63) is similar to the generation of an SRQ. Once again, the microprogram is checking conditions in the Condition Register. When the URQ is active, the Processor must read status. This is accomplished by executing a DR with the Instruction Bit set. (See Figure II-61C.) The status word is sent to the B register; from there the microprogram determines which status bit or bits are active. The result depends on the microprogram.

I/O OPERATION

In reference to the example of selecting the console I/O Control, sending a control word, generating interrupts, reading data, and returning status words can be related by Figure II-64 and explained by the flow chart Figure II-65.

Before this point, the console has been considered selected. The next example of communication is initiated by pressing the console Ready button when the console is unselected. Assume the Processor is reading 80-column cards and storing the data on disk at the time the Ready button is activated.

If the disk was the last device selected and the card reader finished another card at the same time the console Ready button was depressed, an Interrupt Request (IRQ) is generated from both devices. An IRQ is an interrupt from an **unselected** device and it is casued by a DINT or SINT. The microprogram issues an Address and Status Request (ASR) when it finds IRQ active. Only the address of the highest priority device will be sent to the Processor along with the status word. Determining which status word to send is the final function of the PSU. See PS1-1 and PS1-2 logic diagrams in the FT&R documentation.

DINT 3/ from the card reader and SINT 8/ from the console are both low active in the example, and these develop I3/ and I8/ low active, respectively. I8/ generates PSENAB2/ low active, which disables the output from PS1-1. PS1-1 controls ports 1 through 4. I8/, in conjunction with EOASR/ low active, develops PSENST8/ low active. This signal to the console I/O Control sends the status bits on the EXT lines to the B Register. (See Figure II-61C.) I8/ also places the address of the console on the EXT lines by activating EXT06/-08/. The status and address are sent to the B Register as a status word simultaneously. (See Figure II-60.) EXT03/ is low active as a result of pressing the Ready button. At a convenient time, the microprogram initializes the console (possibly after reading the card reader data), and the system go is ready. In any case, the processor services the card reader, because it also generated in IRQ.

DEVICE I/O CONTROLS

Figure II-66 through II-78 show the hardware configuration and communication between the Processor and each of the B 700 I/O control and device interfaces.

DEVICE CONTROL (CONTINUED)

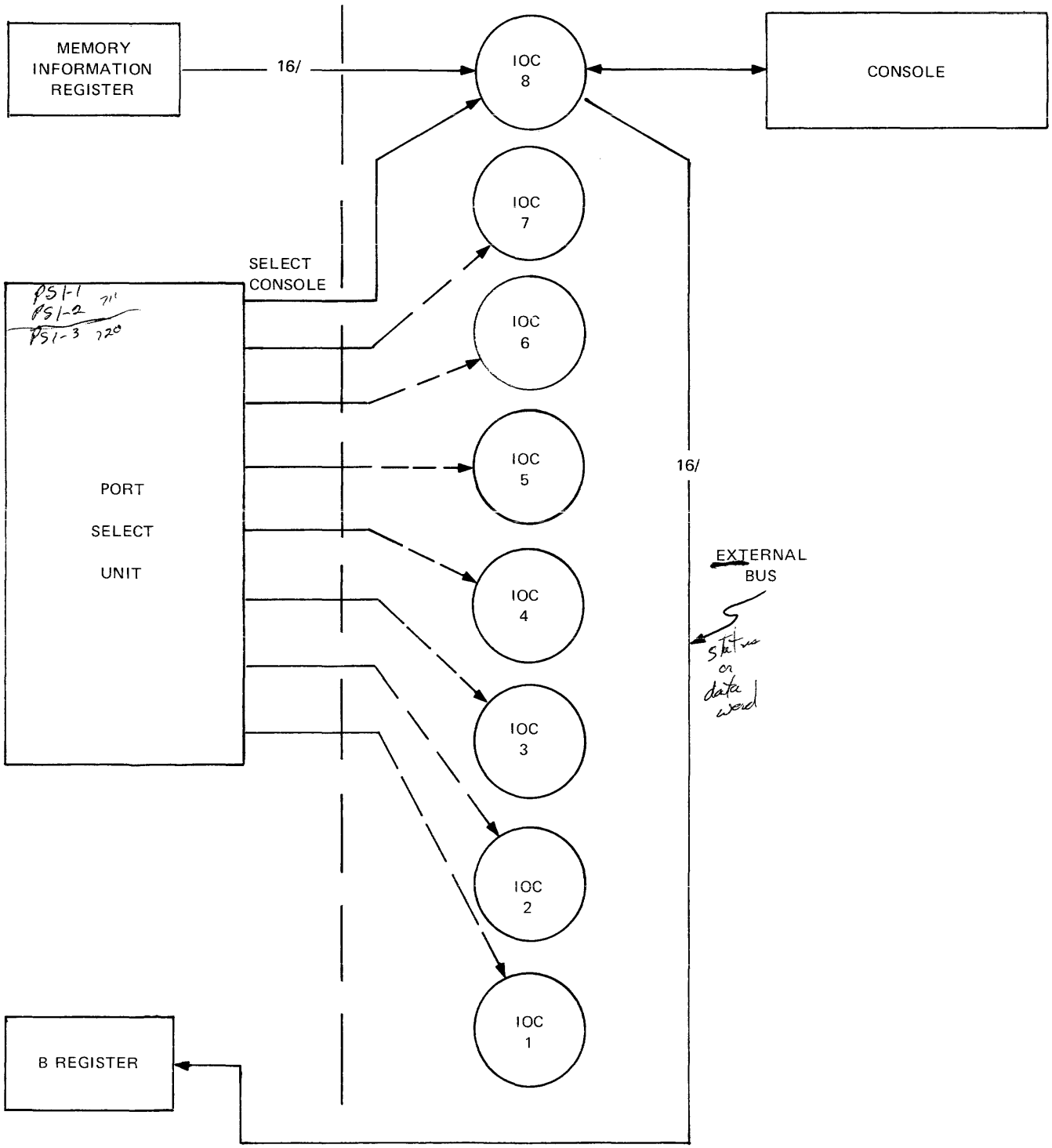


Fig. II-57 I/O DEVICE CONTROL INTERFACE

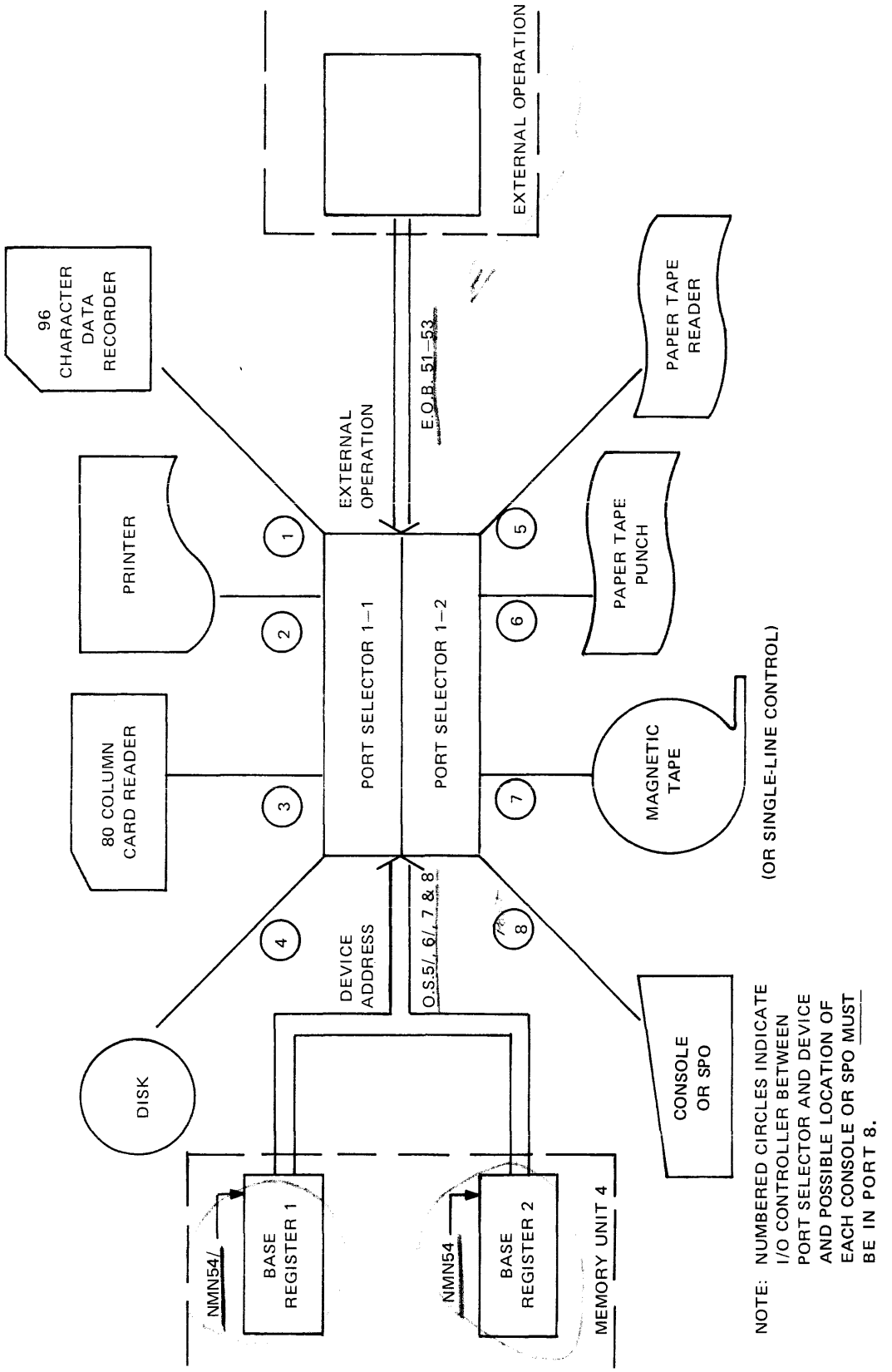


Fig. II-58 PORT SELECTION (DEVICE ADDRESSING)

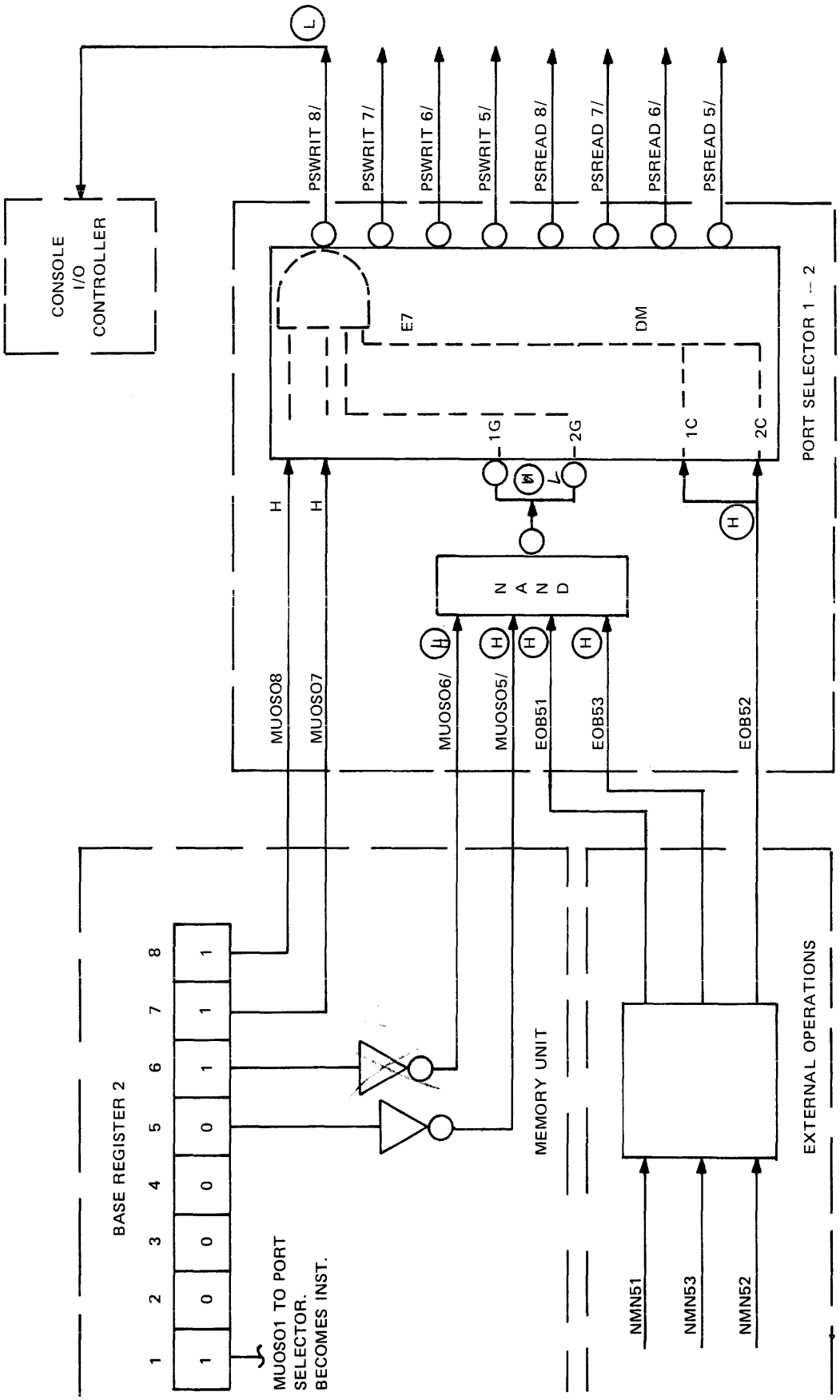
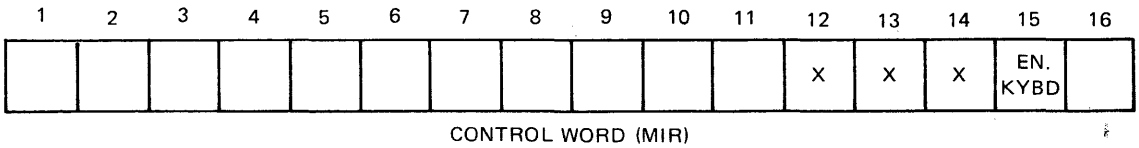
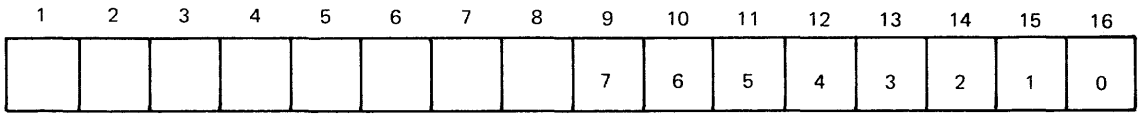


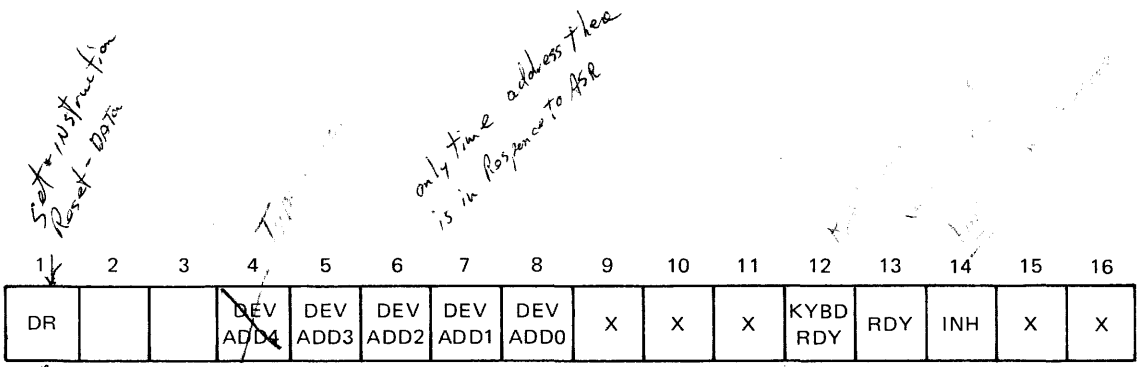
Fig. II-59 DEVICE WRITE FROM BR2 (DW2) TO CONSOLE



CONTROL WORD (MIR)



DATA WORD (B REGISTER)



STATUS WORD (B REGISTER)

NOT USED

X — USED FOR FUNCTIONS OTHER THAN KEYBOARD

Fig. II-60 CONSOLE KEYBOARD WORD FORMATS

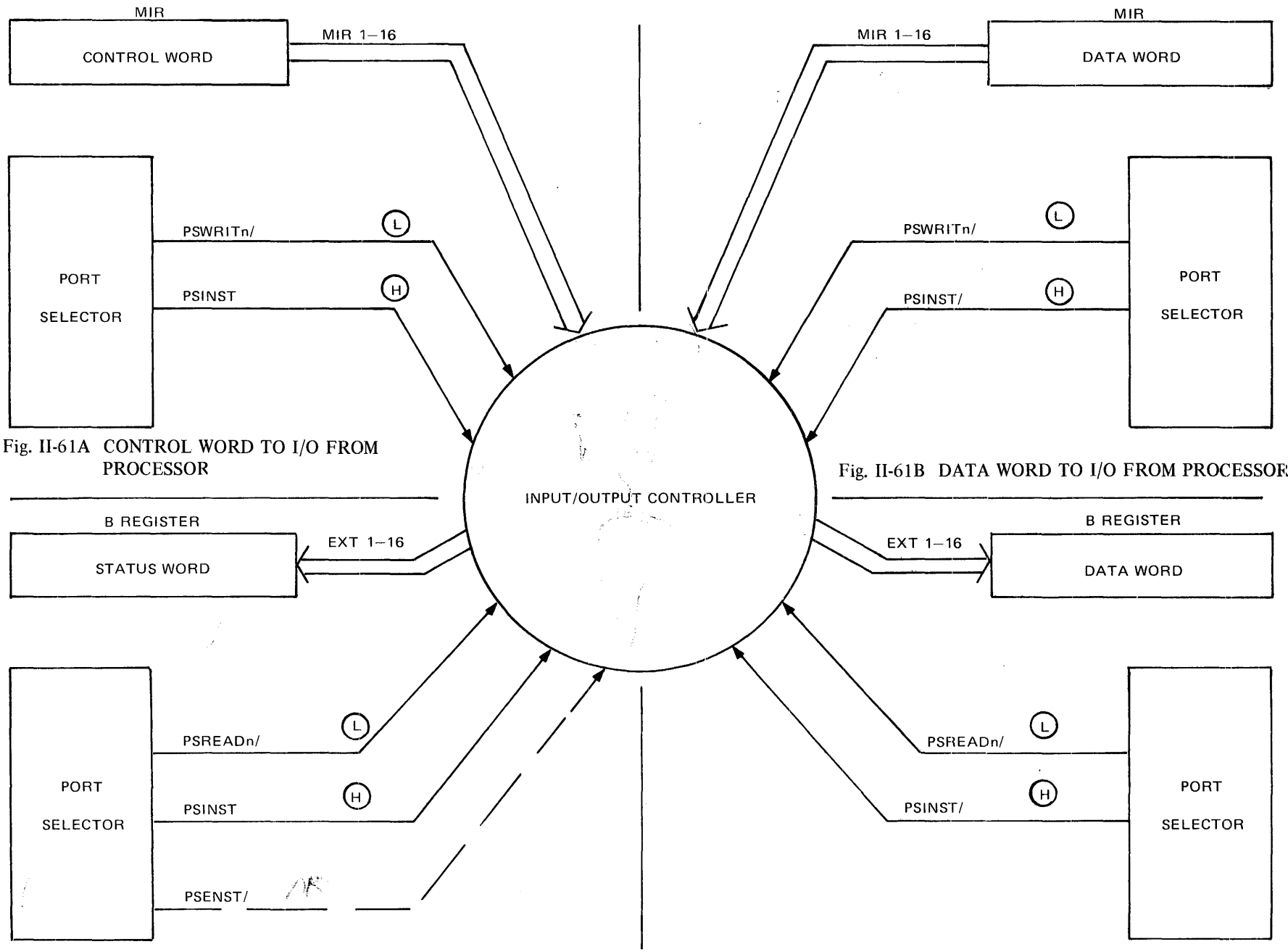


Fig. II-61A CONTROL WORD TO I/O FROM PROCESSOR

Fig. II-61B DATA WORD TO I/O FROM PROCESSOR

Fig. II-61C STATUS WORD FROM I/O TO PROCESSOR

Fig. II-61D DATA WORD FROM I/O TO PROCESSOR

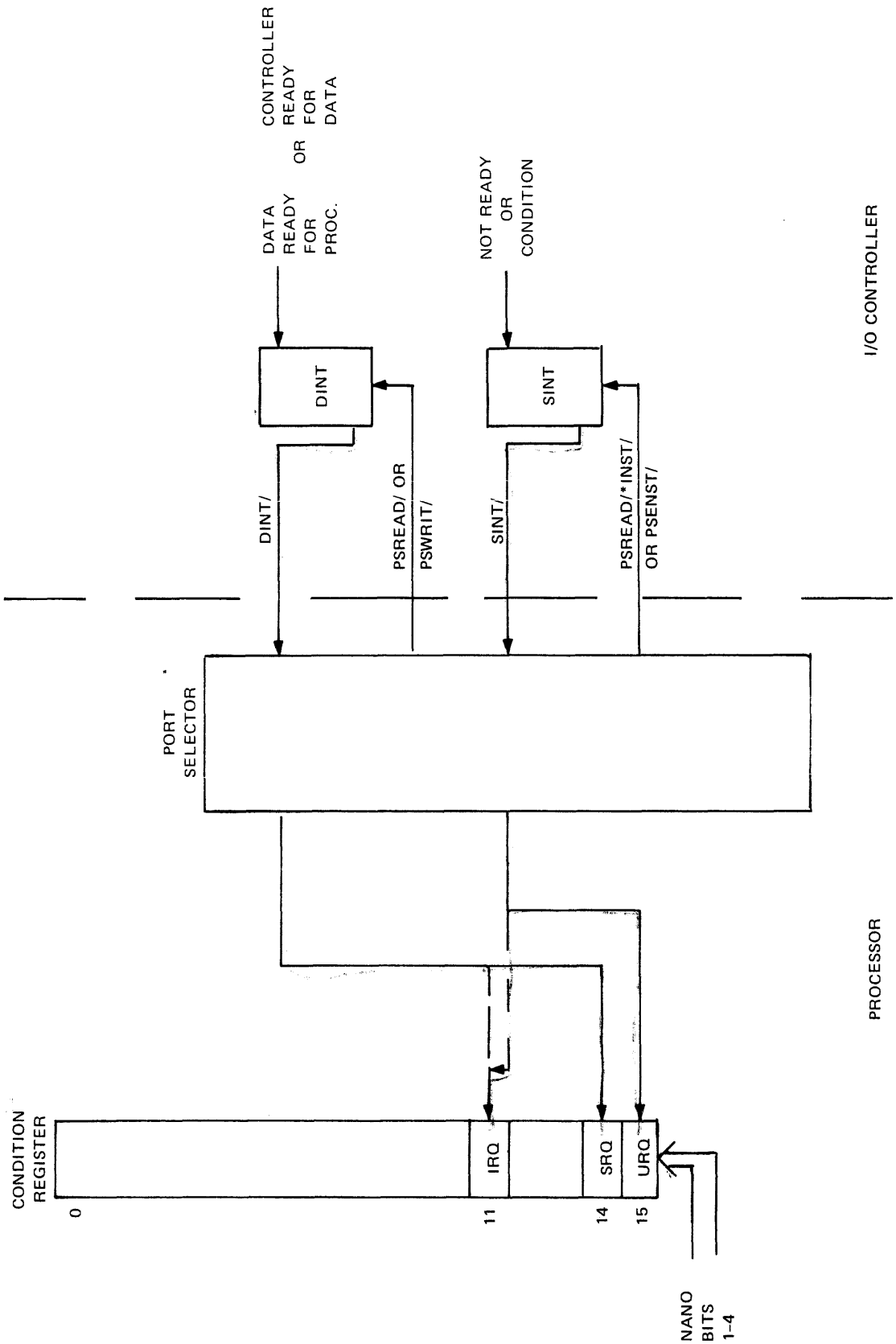


Fig. II-62 INTERRUPT FLOW

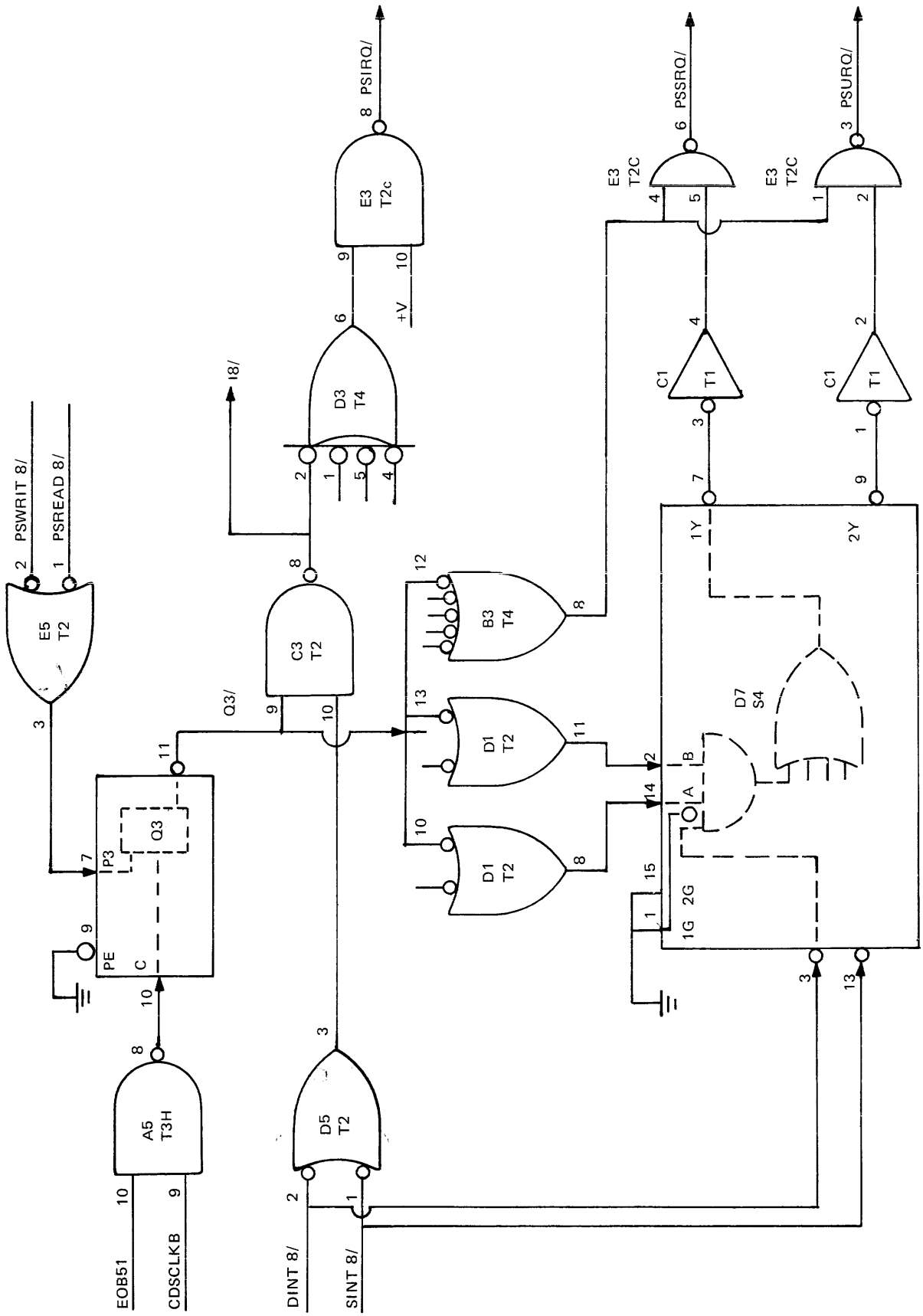


Fig. II-63 GENERATION OF INTERRUPTS (PORT SELECTOR 1-2)

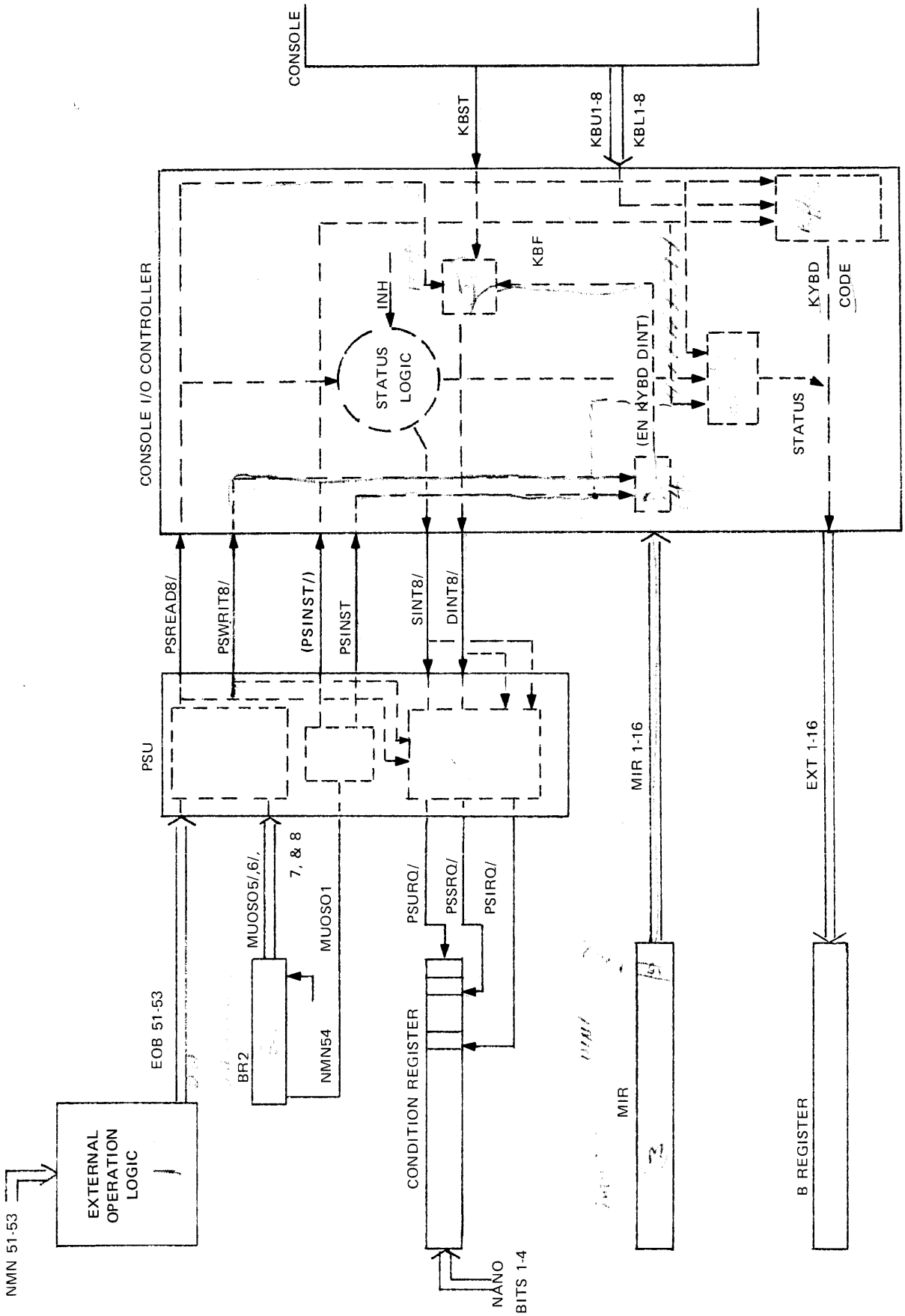


Fig. II-64 CONSOLE KEYBOARD OPERATION

Functional Detail

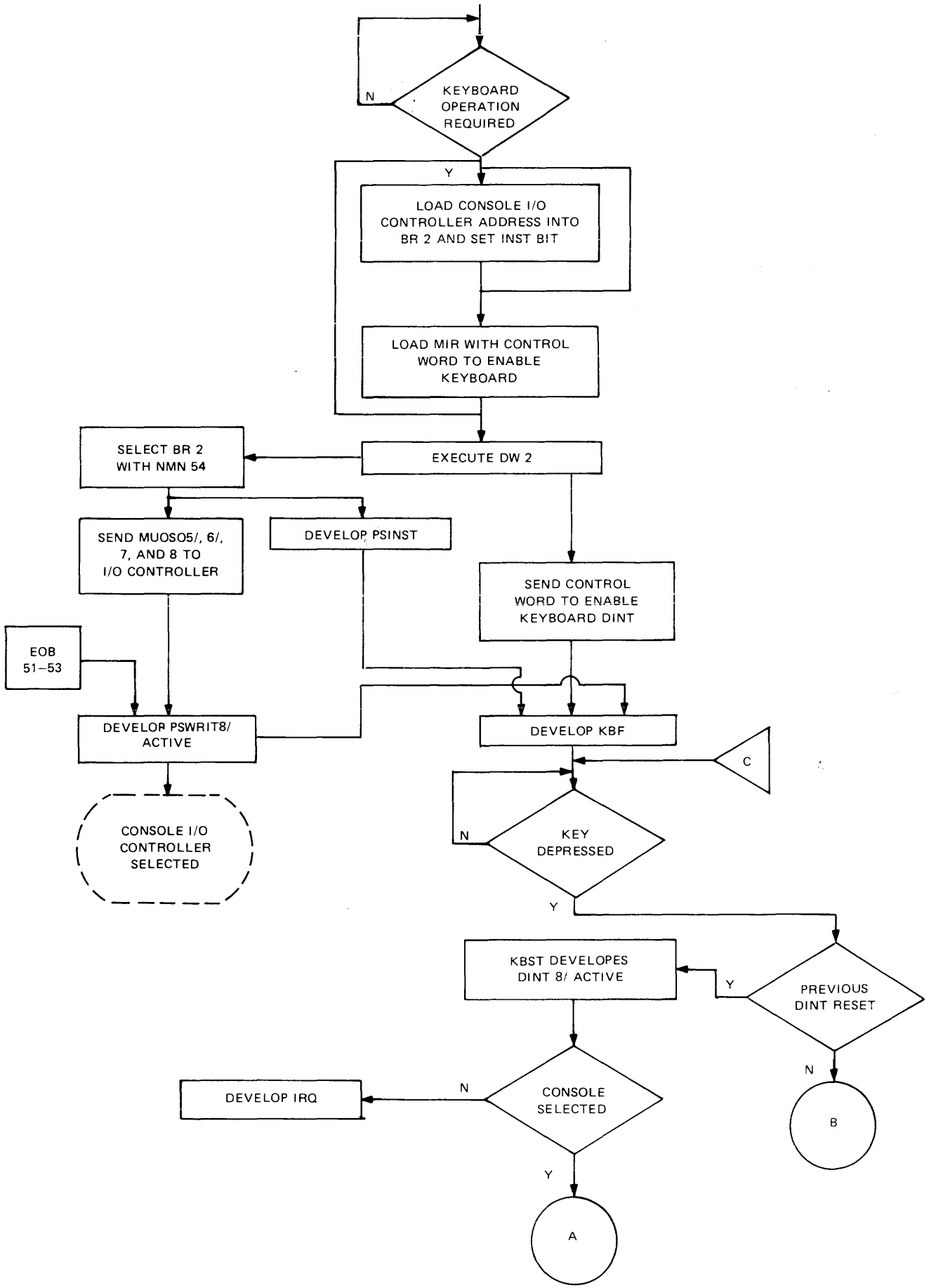


Fig. II-65 CONSOLE KEYBOARD OPERATION (SHEET 1 OF 2)

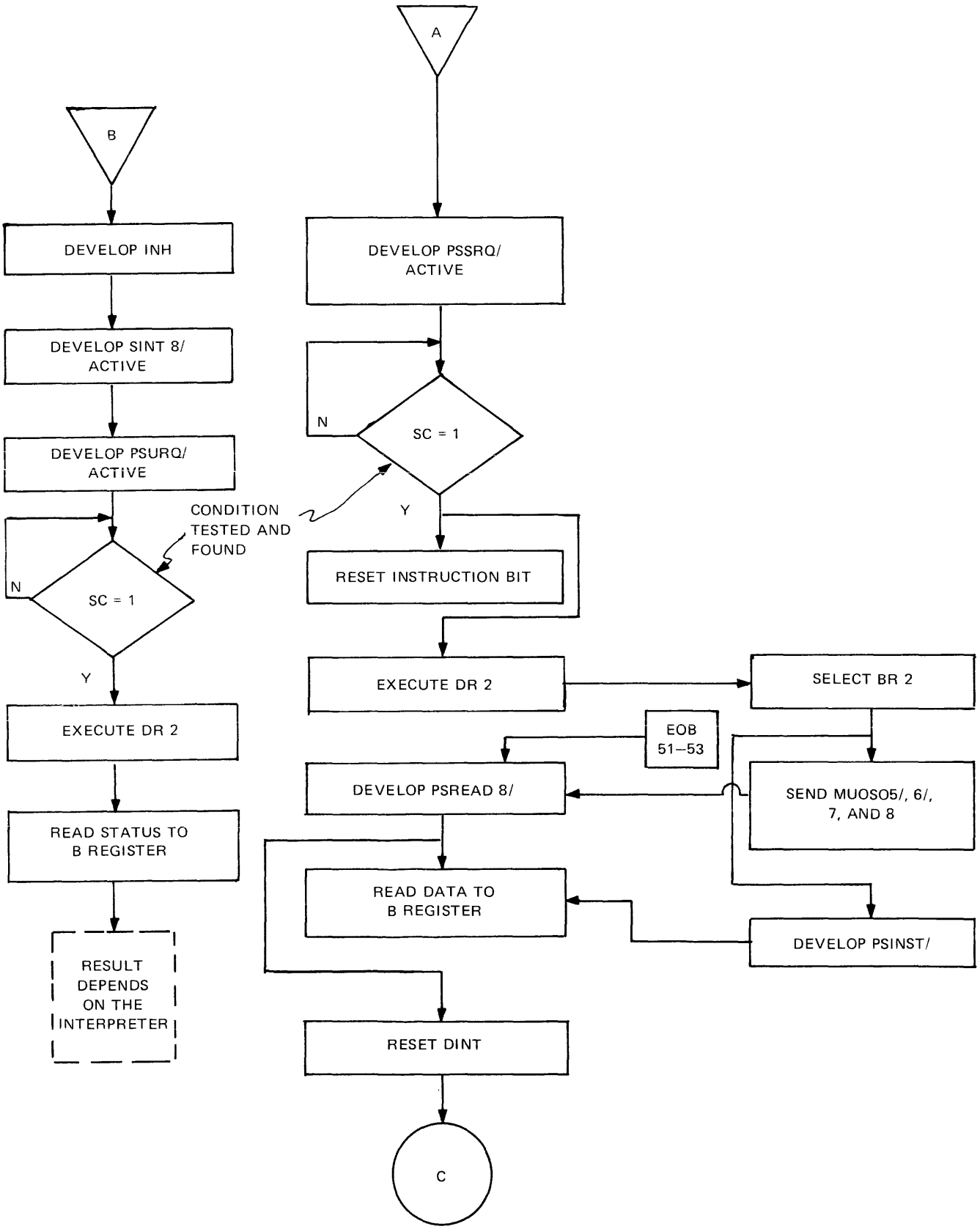


Fig. II-65 CONSOLE KEYBOARD OPERATION (SHEET 2 OF 2)

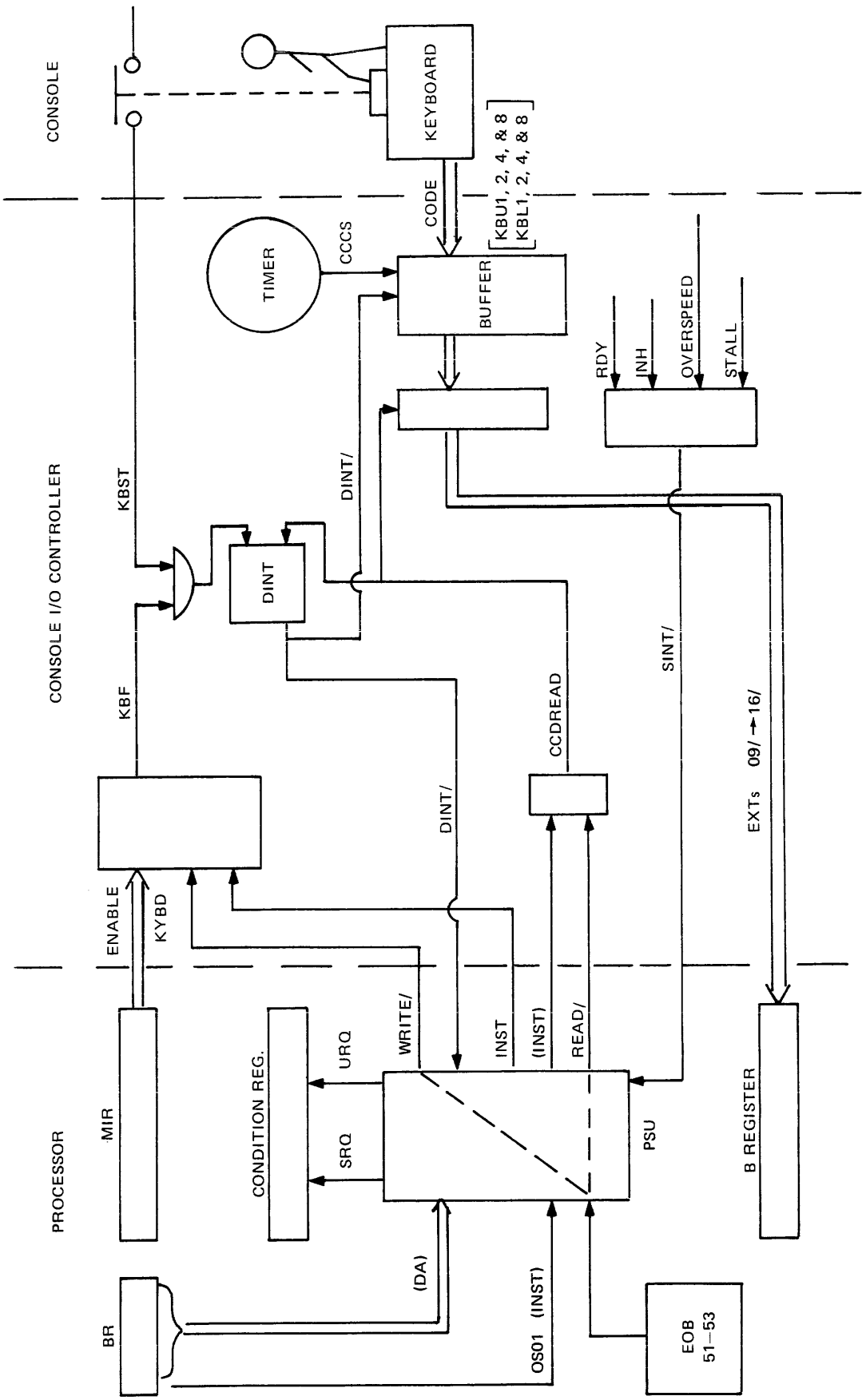


Fig. II-66 READ FROM CONSOLE KEYBOARD

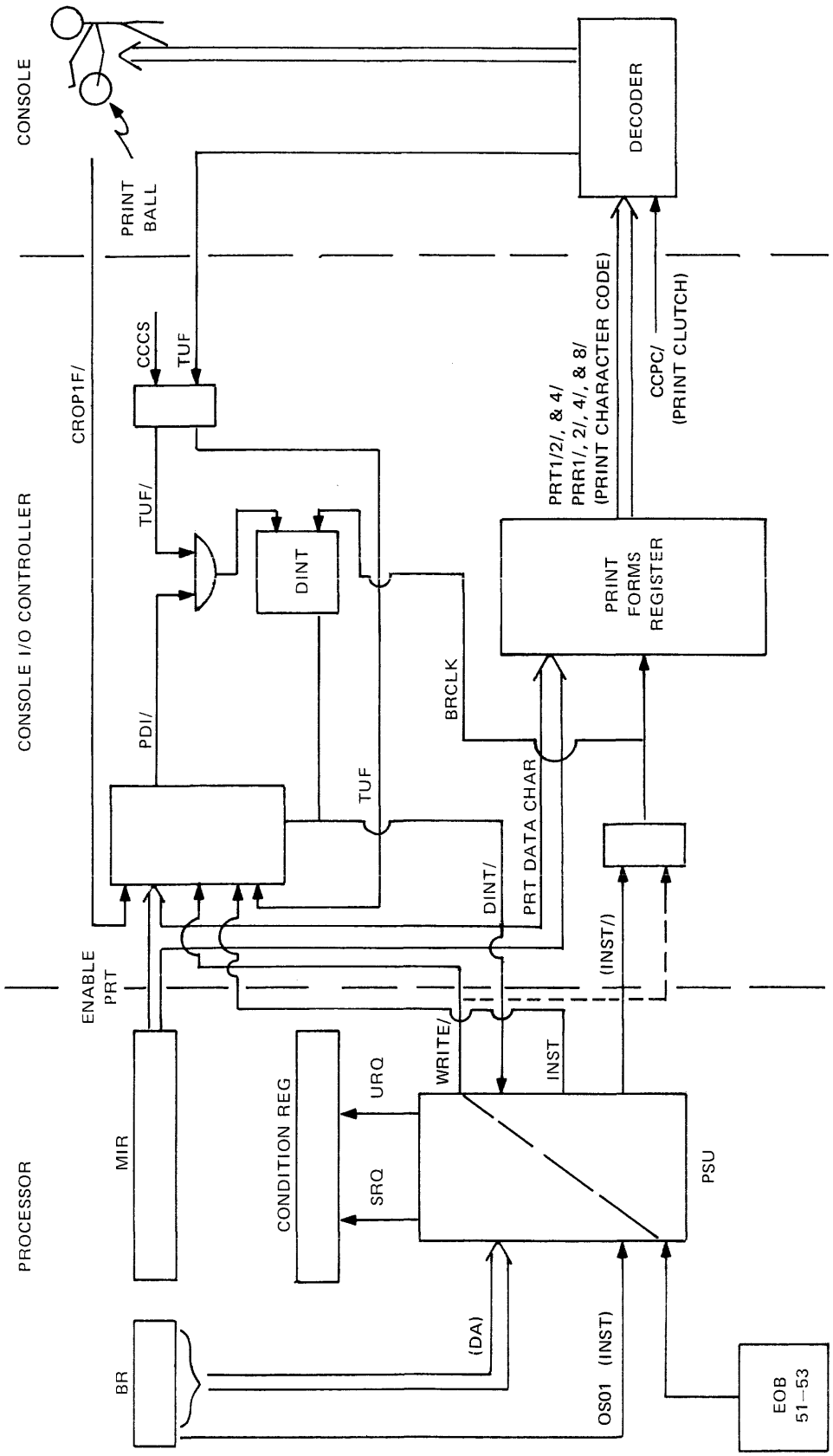


Fig. II-67 WRITE TO CONSOLE PRINTER

Functional Detail

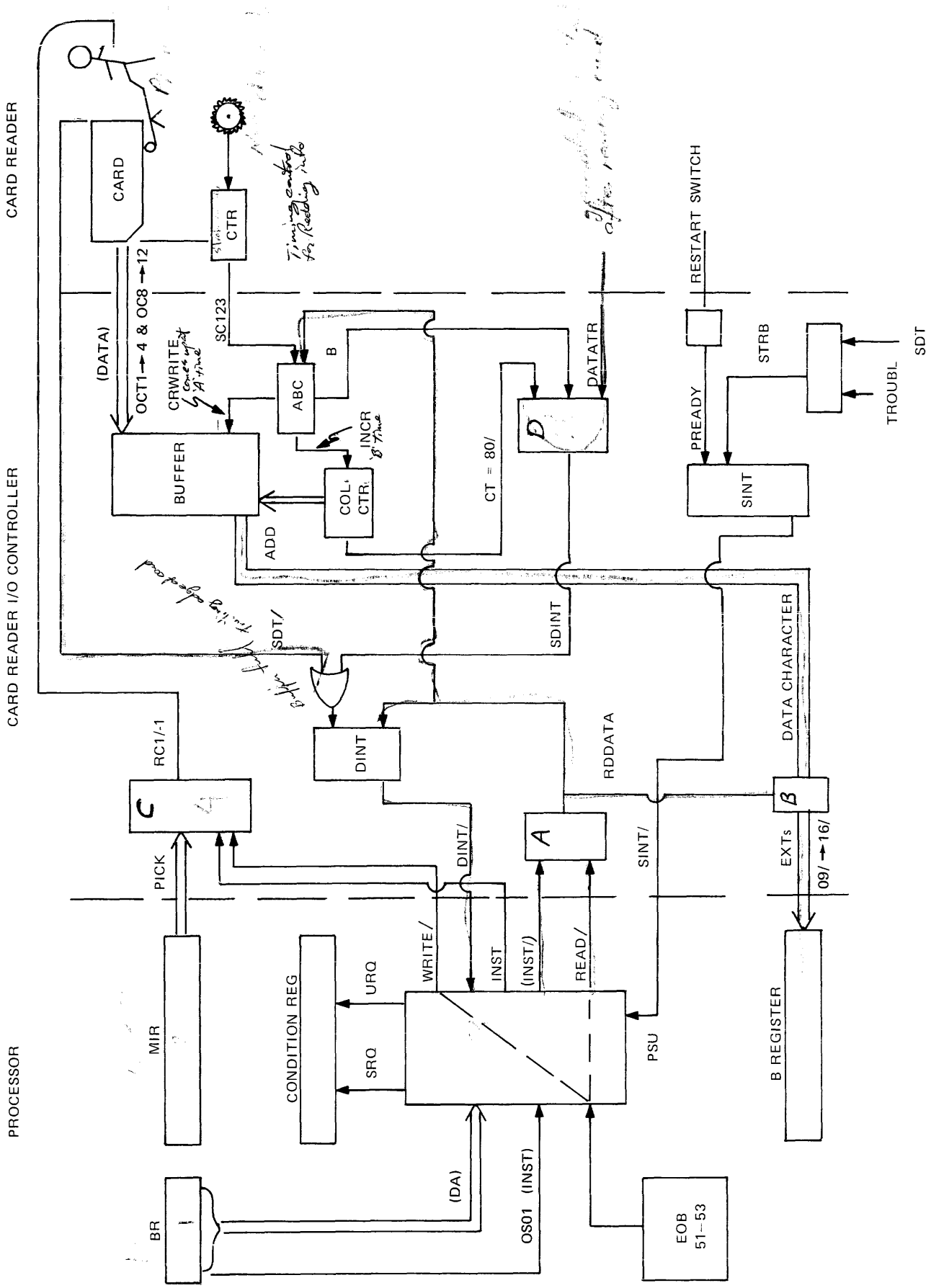


Fig. II-68 READ FROM CARD READER

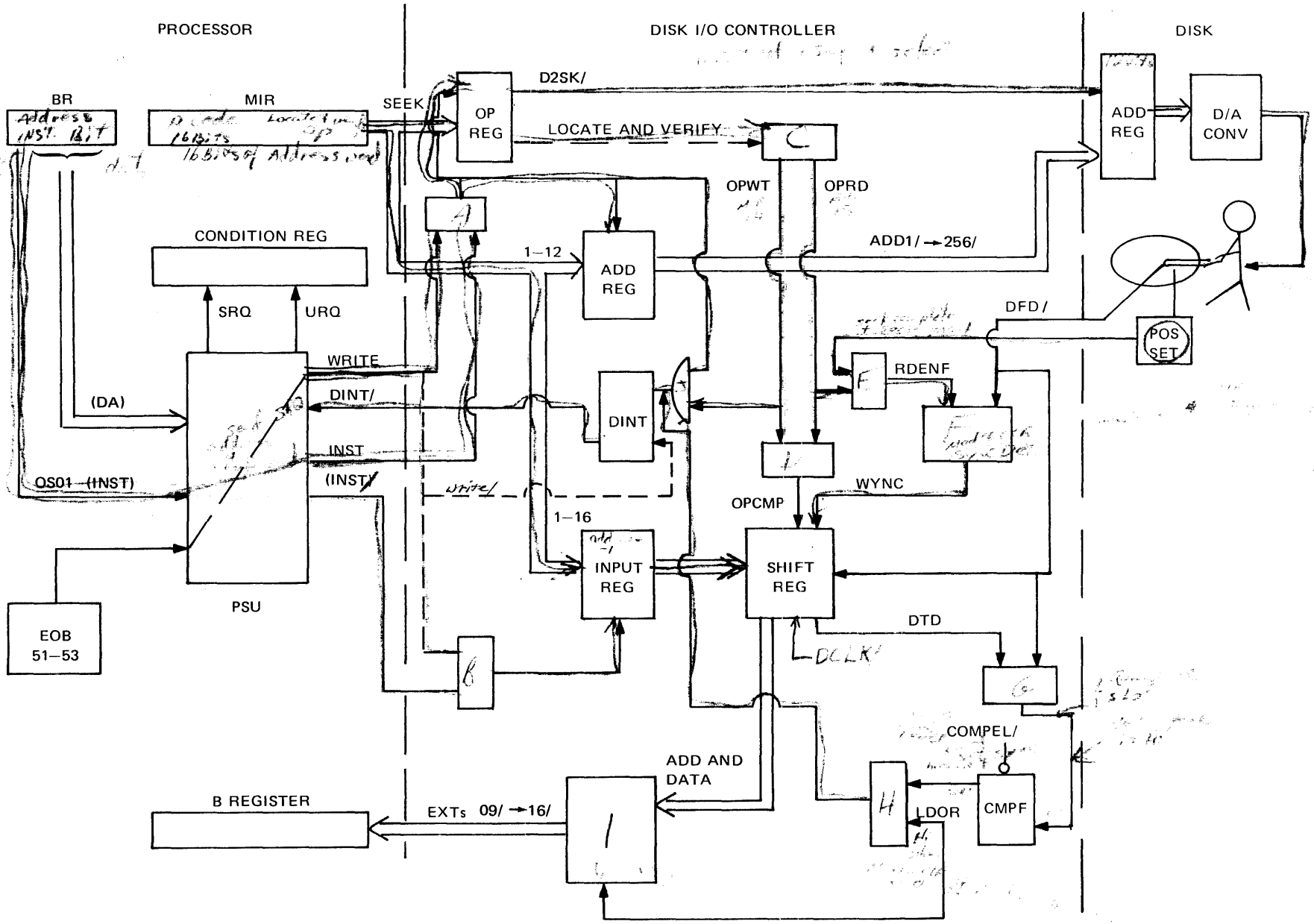


Fig. II-69 SEEK/LOCATE AND VERIFY

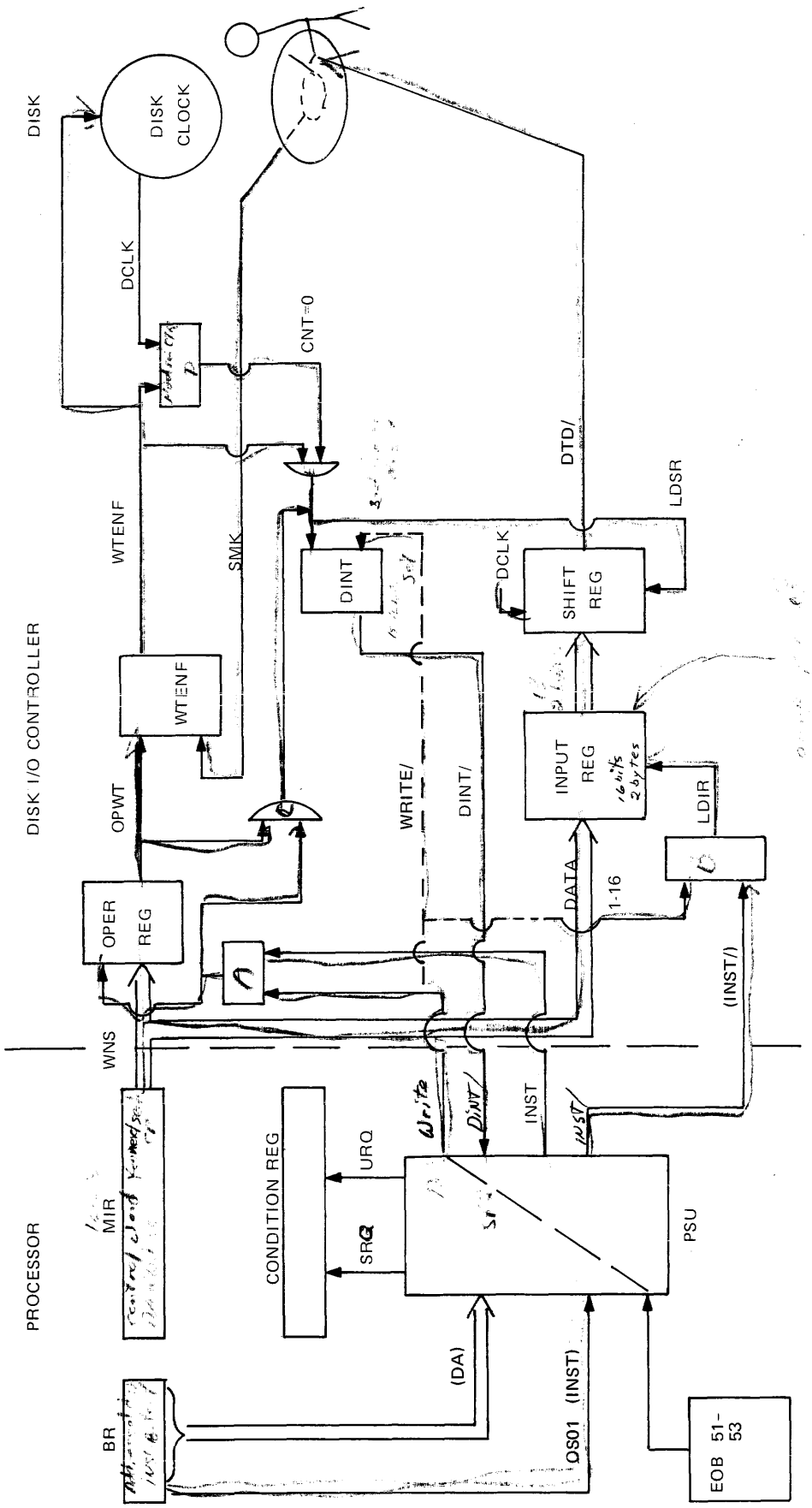


Fig. II-70 WRITE TO DISK

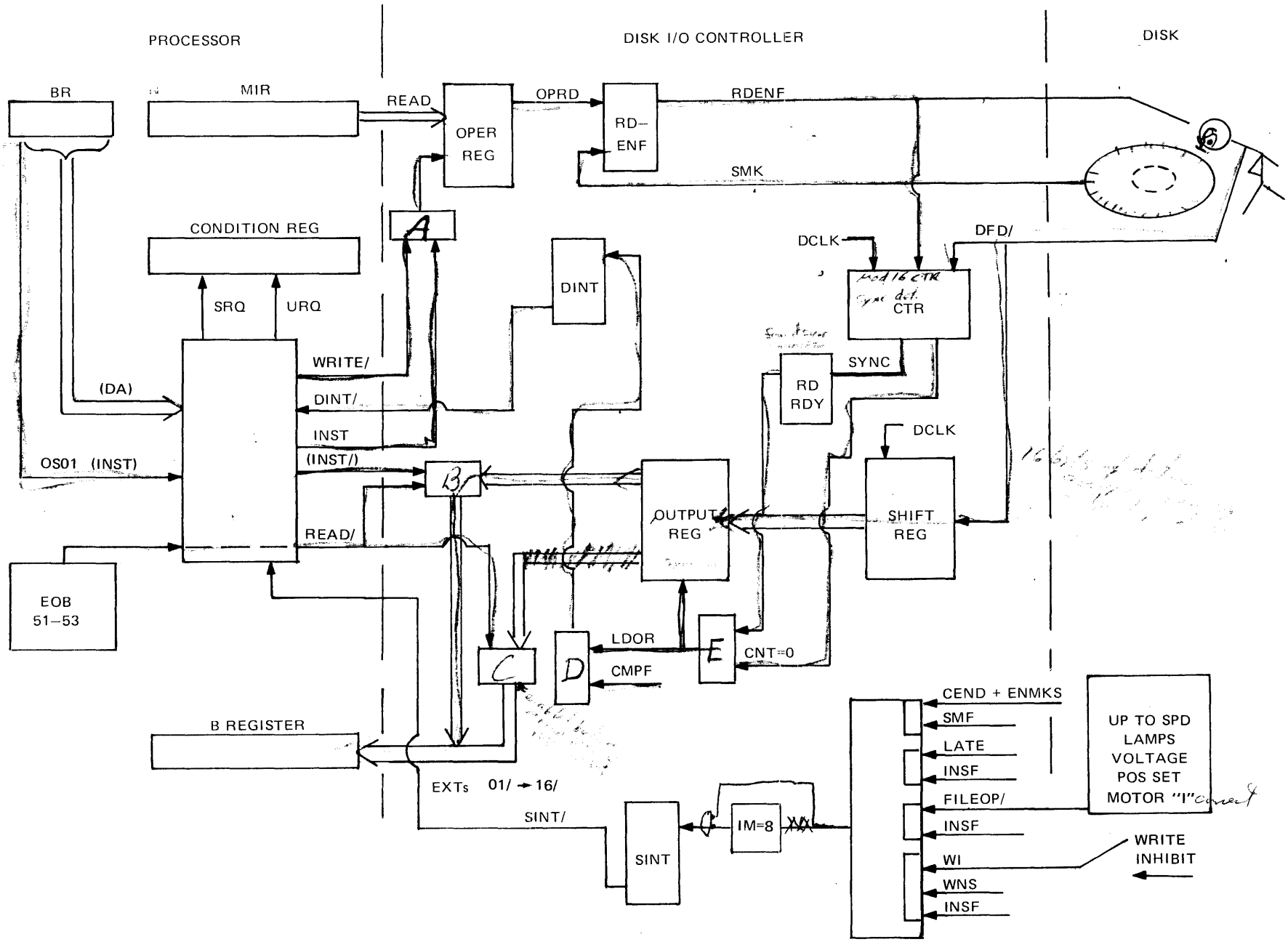


Fig. II-71 READ FROM DISK

Functional Detail

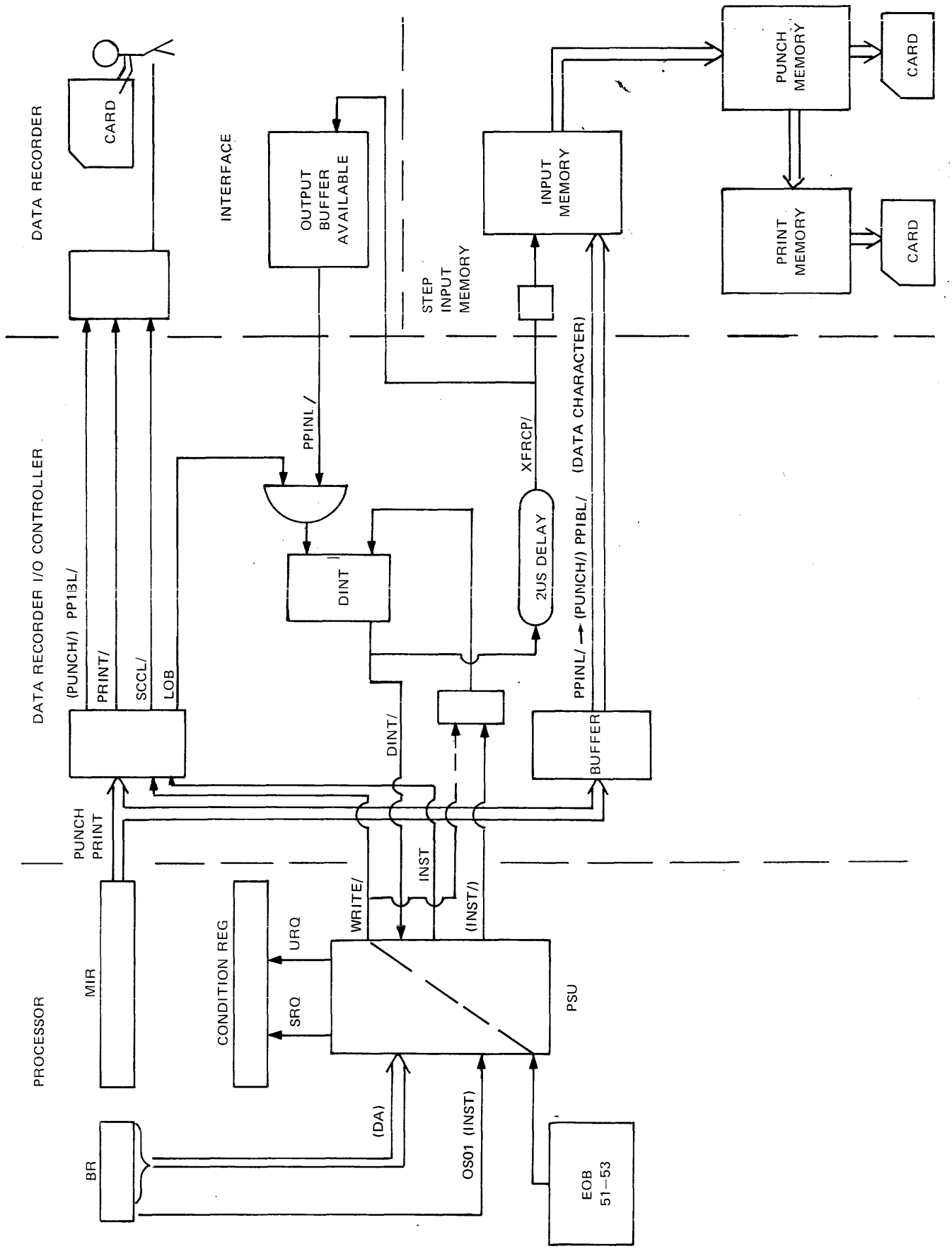


Fig. II-72 WRITE TO DATA RECORDER

Functional Detail

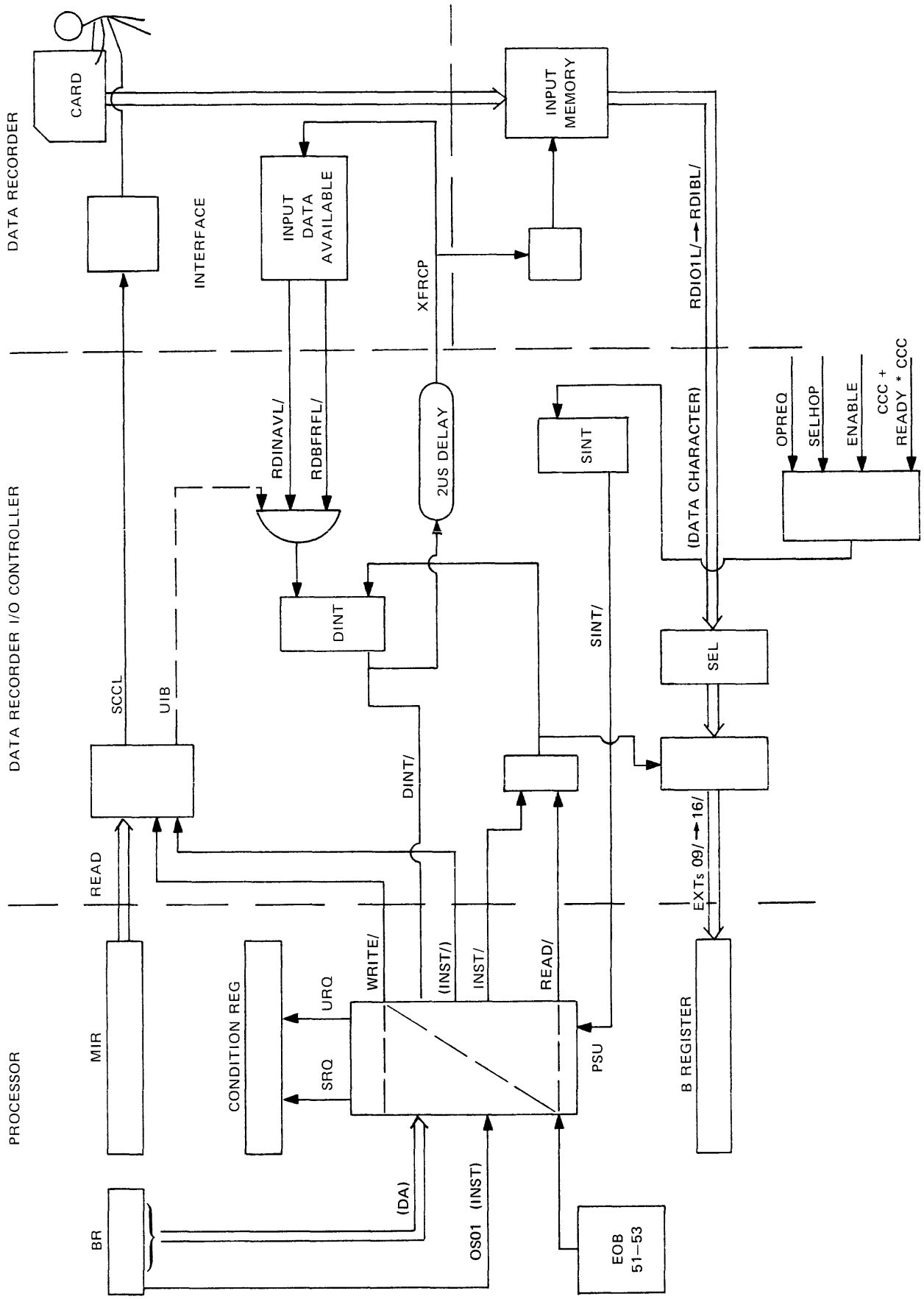


Fig. II-73 READ FROM DATA RECORDER

Functional Detail

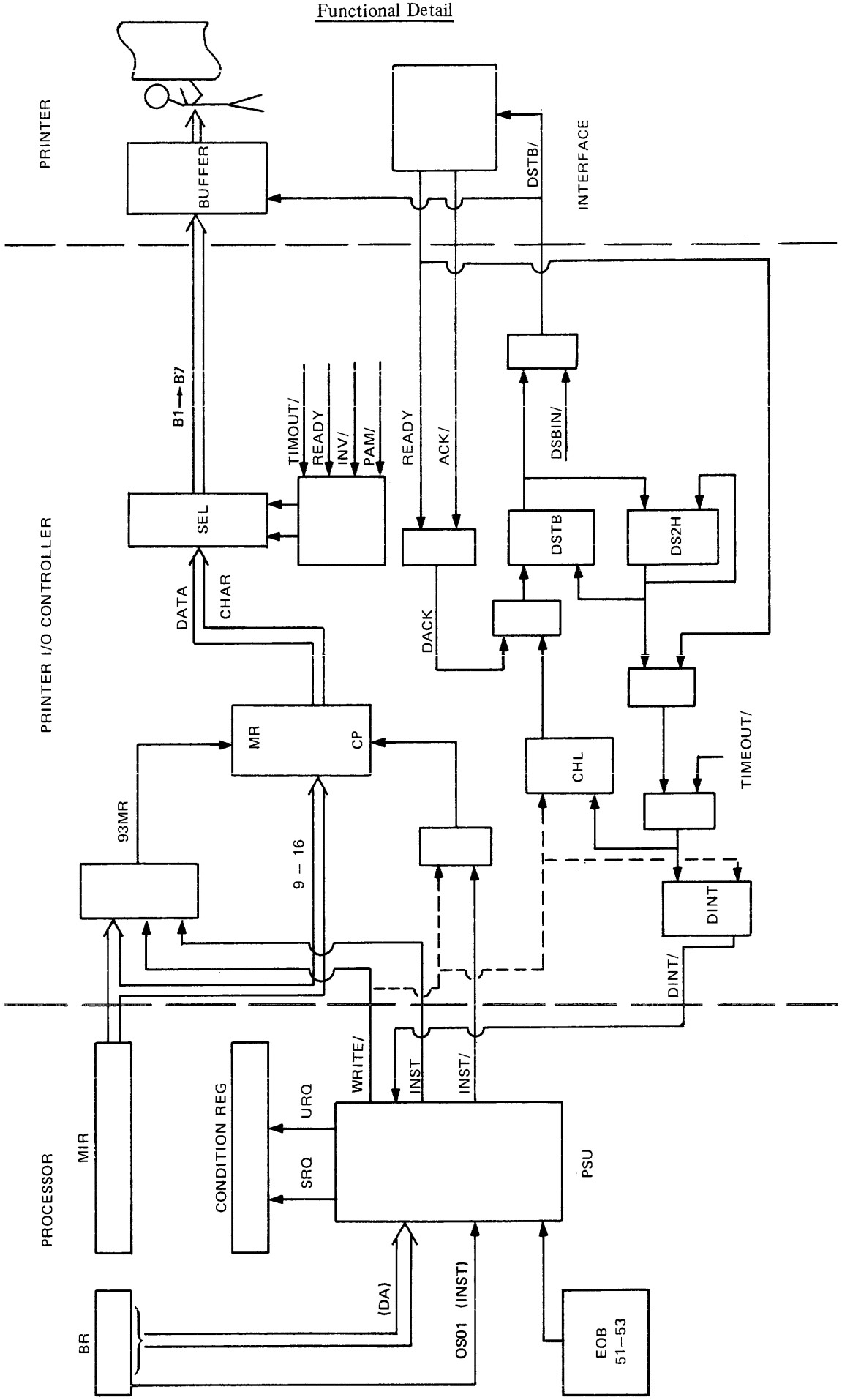


Fig. II-74 WRITE TO PRINTER (9249)

Functional Detail

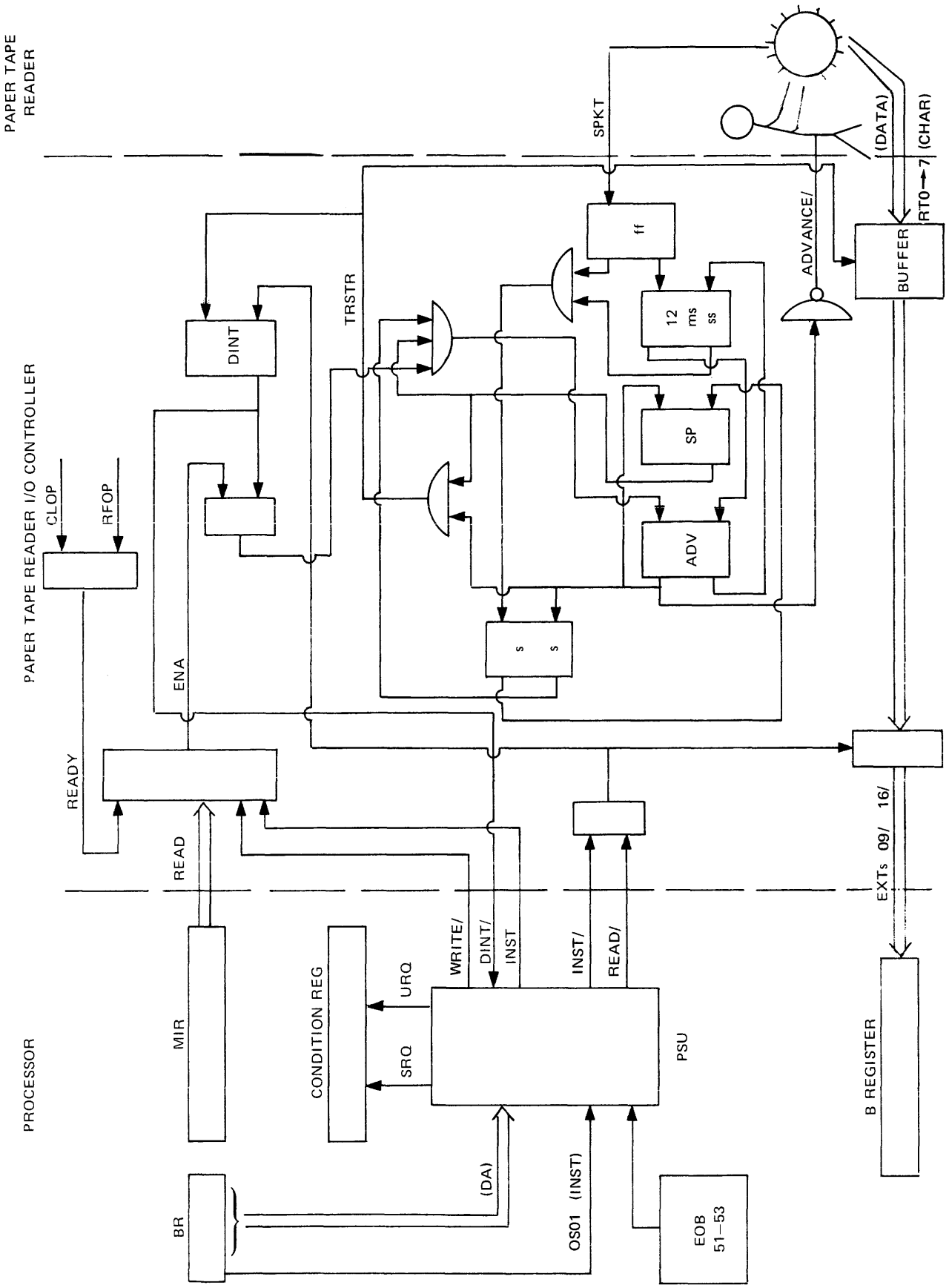


Fig. II-75 READ FROM PAPER TAPE READER

Functional Detail

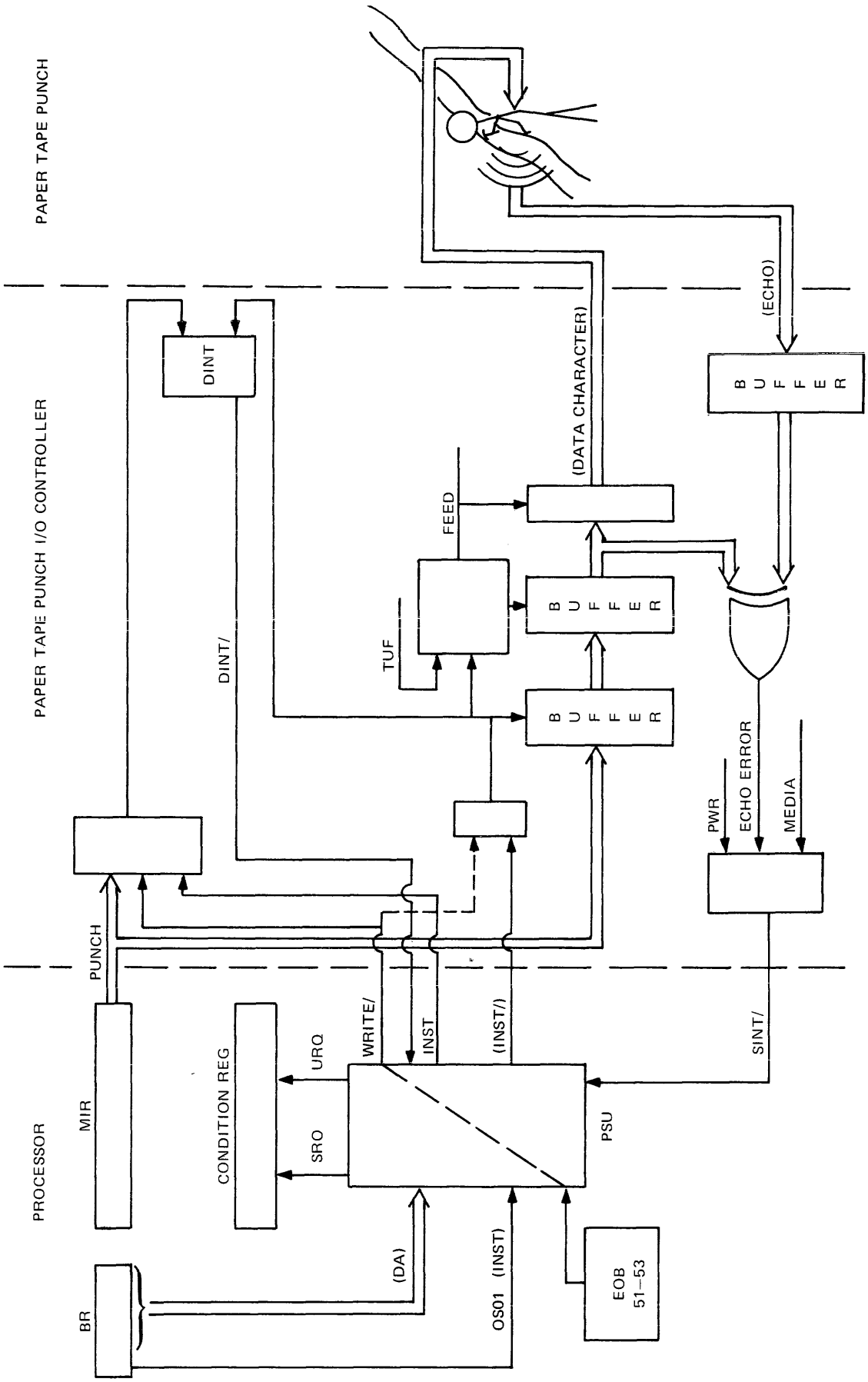


Fig. II-76 WRITE TO PAPER TAPE PUNCH

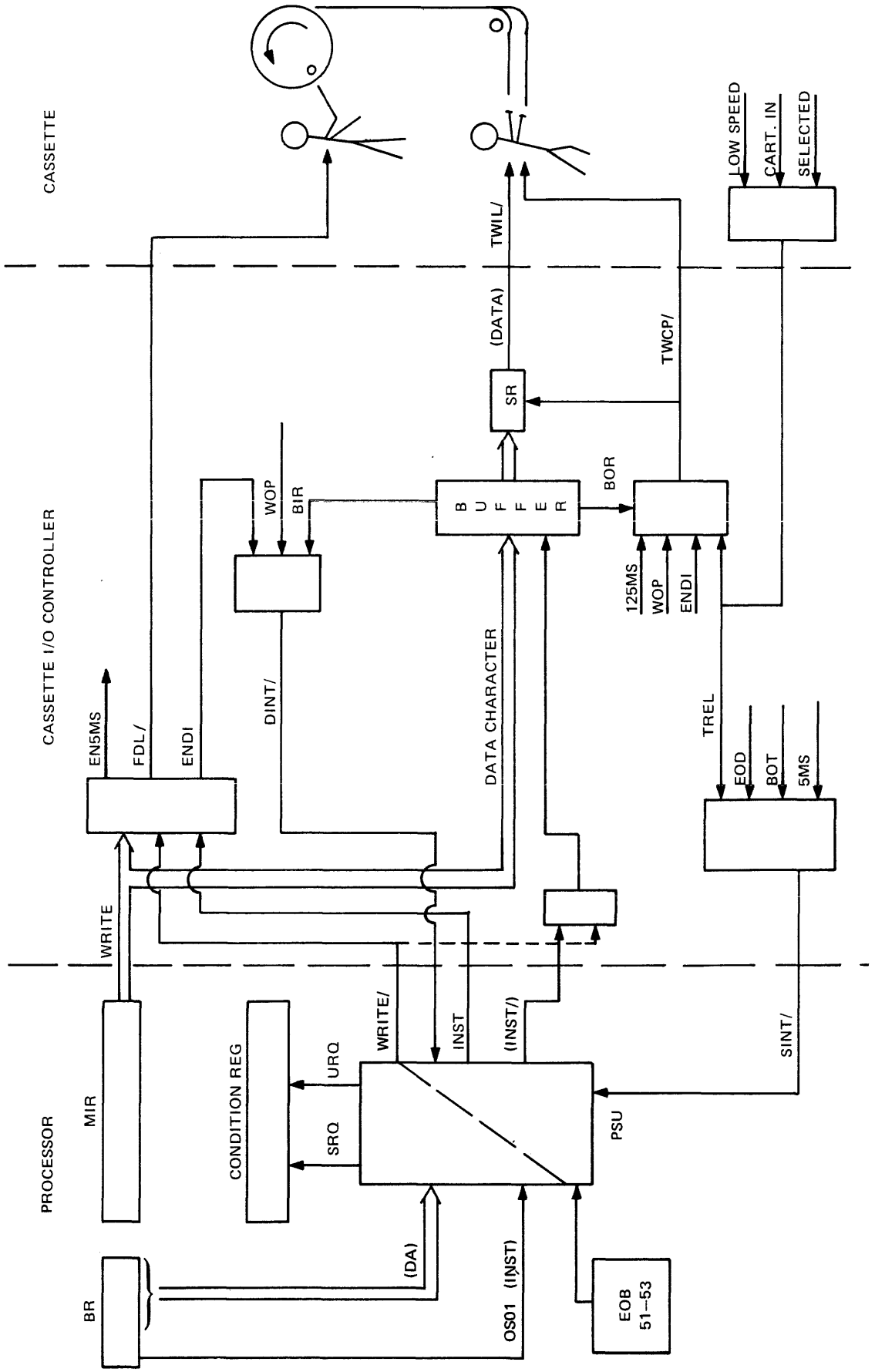


Fig. II-77 WRITE TO CASSETTE

Functional Detail

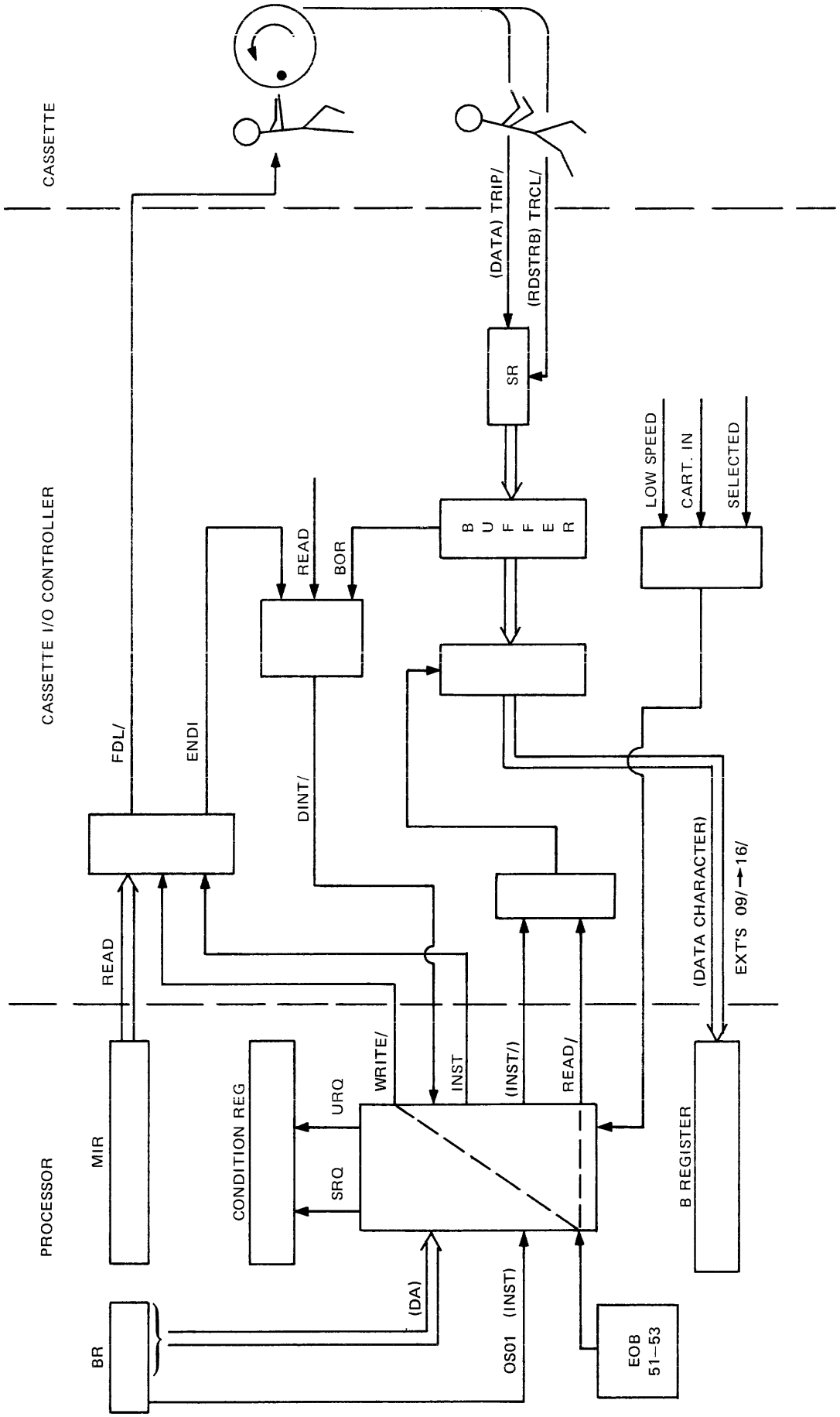


Fig. II-78 READ FROM CASSETTE

POWER SUPPLY SECTION

GENERAL

The Power Supply develops +5, +12, -12, +24 and -24 VDC during the Power Up sequence. Designed into the sequence are separate sense circuits for 24 VAC at the secondary and undervoltage detection. The reference voltage used for Undervoltage Protection is also monitored. The table below lists the DC voltage minimums for the Undervoltage Protection Circuit to become active:

DC Voltage	Minimum
+5	+4.2
+12	+10.2
-12	-10.2
+24	+20.4
-24	-20.4

In the event that the Logic Turn-Off (Ready Button), the AC Sense Circuit, or the Undervoltage Detection Circuit becomes active, the system cycles through a Power Down Sequence. During power up and while the voltages are being developed, an SCR Inhibit Circuit prevents the system from entering a power down sequence because of an undervoltage condition. Besides this, a Data Save feature is incorporated. Data Save will turn off the memory drivers if one of the above three conditions exist.

Figures II-79, II-80, and II-81 are block and flow diagrams of the AC controls and power up/down sequences described in the following paragraphs. Figure II-82 illustrates the timing of the signals for the Power On, Fault Detection Power Down, and Emergency off sequences.

POWER UP/DOWN SEQUENCES

With line voltage through the circuit breakers, depressing the Power On Switch energizes K1. Contacts K1A and K1B activate the ±12 and ±24 VDC power supply. There is a 300-400 ms delay before these voltages become available. When the +24 VDC supply reaches +17 VDC (approximately), K2 energizes. Contacts K2A provide a self-hold path for K1. Contact K2B initiate the 500 ms delay and energize K3. Contacts K3A and K3B activate the +5 VDC power supply, which takes about 200 ms to become available. In addition, AC is applied to the blowers, decoder motor, 80 column card reader, and paper tape unit(s).

Power On Clear, SCR Inhibit, and Data Save have been active up until the 500 ms delay has terminated. After the 500 ms delay, an undervoltage condition or loss of AC would cause power down. At the end of the second delay, Power On Clear deactivates. Logic Turn Off is enabled and may cause Power Down if initiated. If none of these conditions exist, then the Power Up Sequence is complete.

If an Undervoltage, Logic Turn Off, or absence of 24 VAC conditions exist, the Power Down sequence would initiate. In turn, the SCR conducts de-energizing K2. K1 and K3 de-energize, eliminating the source of DC. Power On Clear is generated, and Data Save activates (after a 4μs delay) to preserve memory. All power is removed and the system is off.

POWER LOGIC

The AC Sense, Logic Turn Off, and Undervoltage Detection are all contained on the AC1 board. The AC2 board contains the 500 MS Timer, SCR Inhibit, Data Save and Power On Clear circuits. Each of these circuits will be discussed by component designation in the schematics. for the AC1 and AC2 boards. (See Volume I of FT&R Documentation.)

AC Sense

The 24 VAC from the secondary is sensed at pins 2W and 2X. The circuit becomes active if this voltage is lost by causing Q3 to cut off. Q4 and Q5 then conduct, producing a low output at pin 2N (POWDN). See SCR Inhibit for further detail.

Logic Turn Off

This circuit is designed to power the system down when the Ready Button is depressed. The input at pin 2L, called PWRO/, is active when it is low. Depressing the Ready Button causes PWRO/ to activate and Q1 conducts. As a result, Q2 conducts and pin 2N (POWDN) becomes low. Figure II-83 shows the programmatic connection between the Ready pushbutton and PWR01. Refer to the SCR Inhibit description for further details.

Undervoltage Detection

All DC voltages are monitored by the circuit. One input to each Differential Comparator (U1A, U1B, U2A, U2B, U3A, and U3B) is a regulated positive voltage (Reference Voltage). The other input is the voltage to be monitored. Zener diode VR1 is the regulating component. Refer to the following table for the monitoring comparator for each voltage:

Voltage	Monitored At
+5	U1A
+12	U2A
+24	U2B
-12	U3A
-24	U3B
Reference Voltage	U1B

If the voltage being monitored is lower than the minimum, then the output of the comparator is high. Any comparator or comparators with a high output opens the series current path through transistors Q8-Q13. As a result of an undervoltage condition, Q6 cuts off and Q7 conducts.

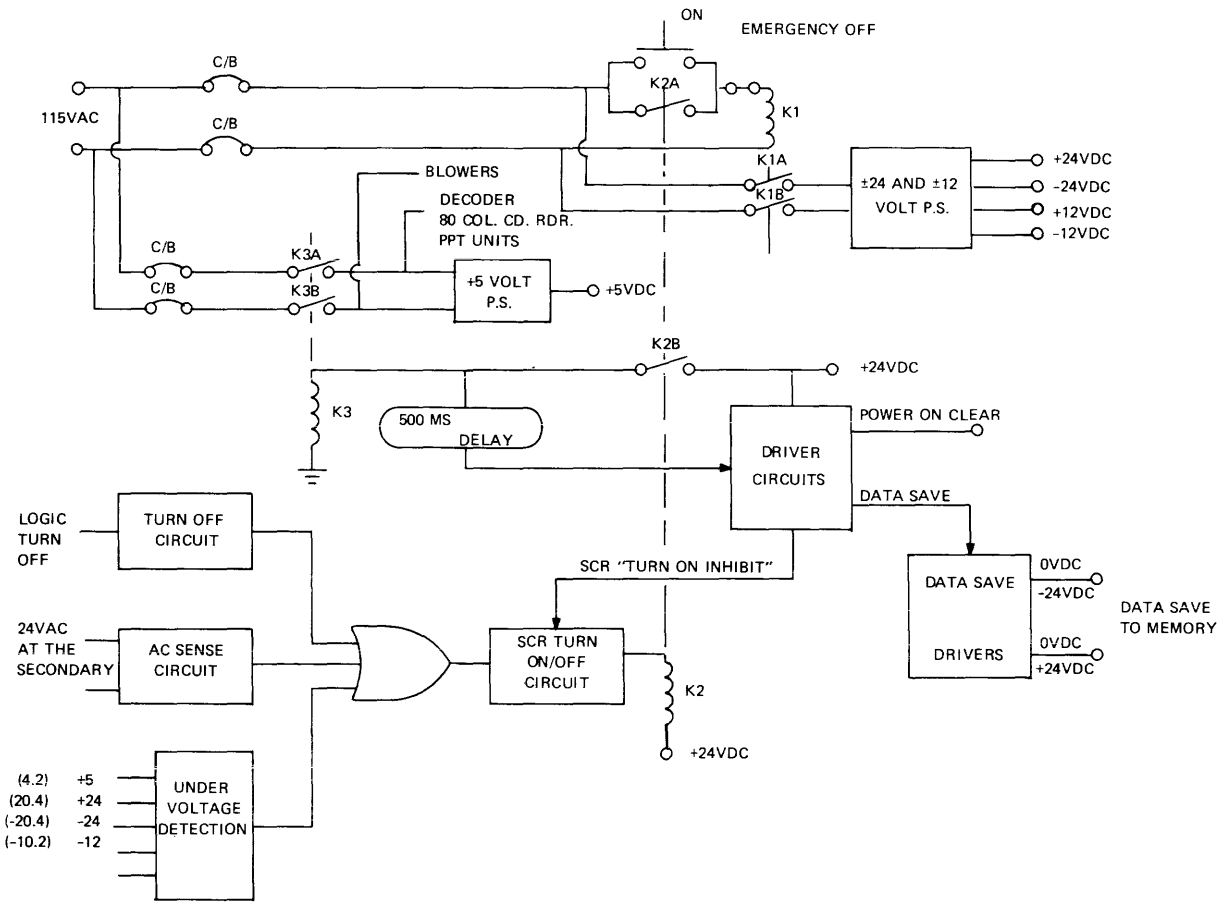


Fig. II-79 AC CONTROLS

This causes POWDN at pin 2N to become low. See SCR Inhibit for further detail.

500 MS Timer

The 500 ms Timer provides a delay to allow time for the power supply voltages to develop and stabilize before activating the logic. C5 starts to charge as soon as K2 energizes. Approximately 500 ms after C5 starts charging, the unijunction Q1 is biased into conduction. This causes the SCR (Q2) to trigger, and Q3 conducts. Q3 conducting supplies a positive voltage (24 VT1) to the SCR Inhibit (Base of Q16) and Data Save (Base of Q20) circuits. In the meantime, the conducting unijunction discharges C5 and Q1 cuts off. C5 charges again, and biases Q1 into conduction a second time. Q4 triggers, because the reverse bias had been removed by Q6 and Q7 from diode CR3, 4 ms after the first 500 ms delay. The effect of this is to place 24 VT2 on the base of Q9 (via Q5).

SCR Inhibit

During the initial 500 ms, after applying DC power, Q16 is held cut off by the 500 ms timer. Q17 conducts during this time, and prevents the SCR (Q13) from conducting because CR4 is reverse biased. At this time, Q11 is conducting because of the undervoltage condition that exists initially. After the timer times out, Q16 conducts; Q17 cuts off; CR4 is enabled; and the SCR may be triggered. Q11 should have cut off before the end of the 500 ms. The SCR is only triggered if Turn Off, AC Sense, or Undervoltage is active.

In the condition that one of these is active, the output from pin 2N on the AC1 board would be a low signal. This signal is called POWDN and it is an input to the AC2 board at pin 2V. Q11 conducts; the SCR is triggered; Q12 and Q14 conduct, cutting off Q15 which de-energizes relay K2. PD + K1DROP is developed through CR6 as a result of Q12 conducting. K2 de-energizing will de-energize K1. C9 on the AC2 board starts to discharge and Q18 conducts, maintaining PD + K1DROP at 24V. PD + K1DROP causes Q19 to conduct and, after a 4 us delay, Q20 cuts off. The Data Save transistors Q23 and Q24 are activated by Q21 cutting off. Q22 cuts off; Q23 conducts; and DSV + 24 (Pin 2E) goes to 0V. Q24 conducts, therefore DSV -24 (Pin 2H) also goes to 0V. The

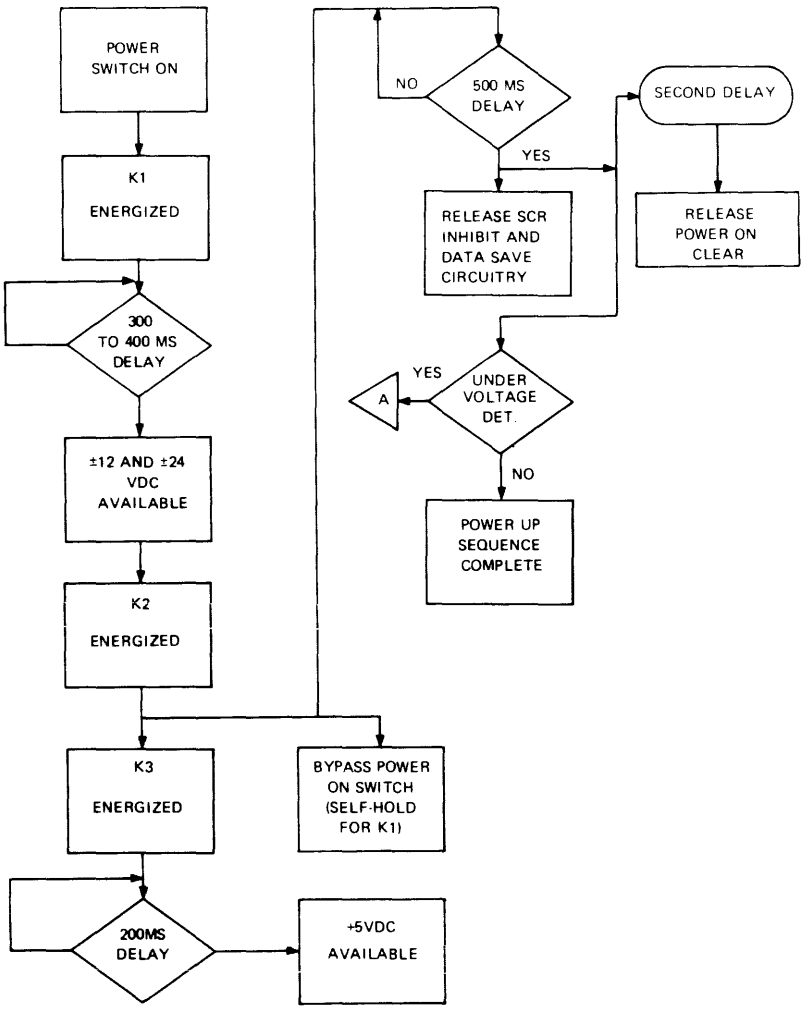


Fig. II-80 POWER UP

effect of this is to disable the memory drivers. A 4 us delay was incorporated to allow the memory cycle in progress, at the point of the failure, time to execute.

DATA SAVE (Figures II-84 and II-85)

The Data Save feature removes power from the core memory driver circuits, so that a loss of logic control cannot disturb the data stored in memory.

During the initial 500 ms after applying DC power, Q20 is cut off (24 VT1 not yet developed); Q21 and Q22 are cut off; Q23 and Q24 are conducting. Q23 is the +24 volt Data Save transistor, and Q24 is the -24 volt Data Save transistor. Each of these provides a zero volt level, out pins 2E and 2H respectively. The effect of this is to inhibit the +15 VDC and -15 VDC power supplies on the Memory System Control Board. After the timer times out, 24 VT1 causes Q20 to conduct and pins 2E and 2H (DSV ±24) go to +24 VDC and -24 VDC respectively. At this time, the 15 volt power supplies generate regulated outputs.

If and when POWDN becomes active (see SCR Inhibit), both outputs from the Data Save circuits return to zero after a 4 μs delay. This allows the present memory cycle time to execute. At pins 2KU and 1DU on the Memory Systems Control Board this zero volt level causes SCR's to trigger. SCR Q12C triggers because Q15P conducts, and SCR Q15C triggers because the gate is at zero volts and the cathode is at -15 VDC. Both SCR's receive a positive signal in respect to the cathode and remain conducting. The 15 volts from both supplies are grounded, thus turning off the memory drivers.

POWER ON CLEAR

PONCL/ is a low signal, during the initial 500 ms delay and through the second delay. (Figure II-82) after DC power is applied. The purpose includes clearing registers, resetting flip-flops, etc. Before the 500 ms timer times' out, Q9 is cut off and Q10 is conducting. The output at pin 2I, which is PONCL/, is low. After the second delay, Q9

conducts and Q10 cuts off. As a result, PONCL/ becomes high. This signal must stay high during the remainder of the time that the system is operating.

In the event of POWDN becoming active, PD + K1DROP (see SCR Inhibit for further detail) causes Q8 to conduct, and Q9 cuts off. Q10 conducts so PONCL/ goes low.

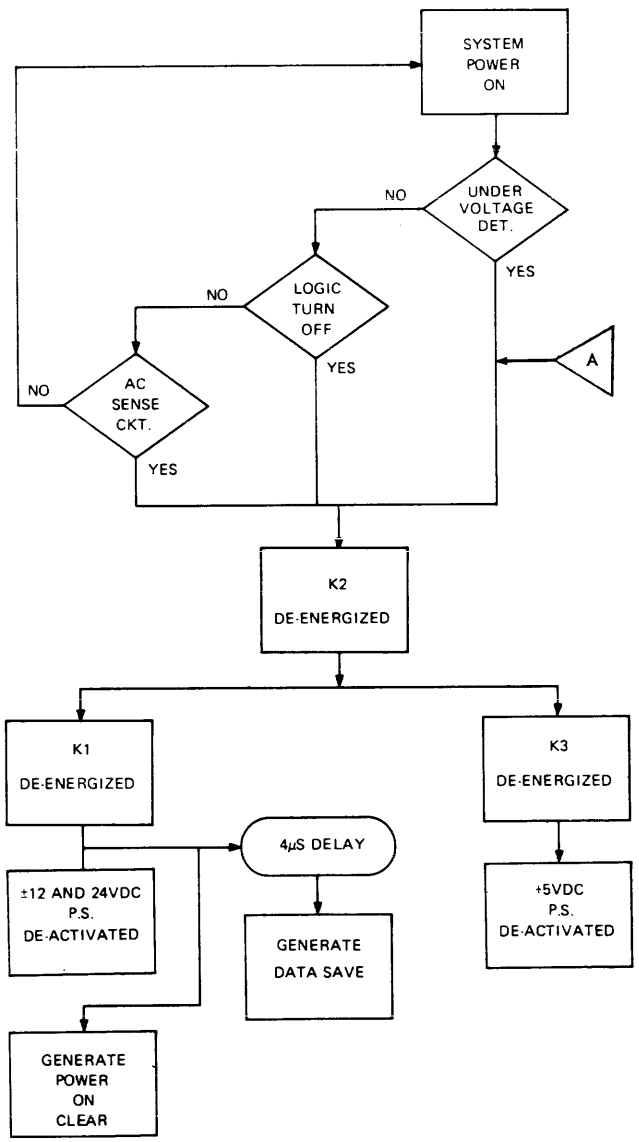


Fig. II-81 POWER DOWN

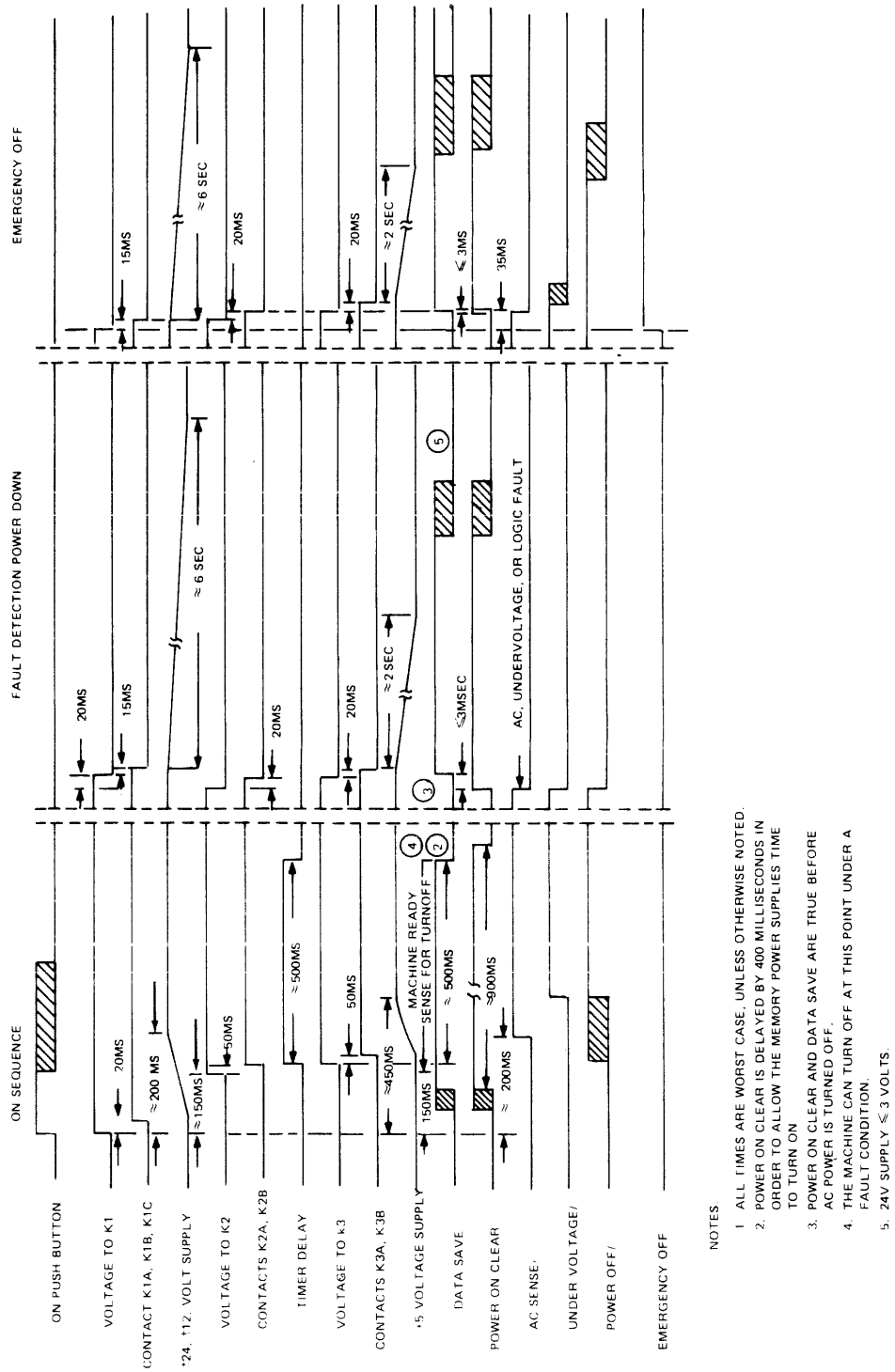


Fig. II-82 POWER ON, FAULT DETECTION POWER DOWN, AND EMERGENCY OFF TIMING SEQUENCES

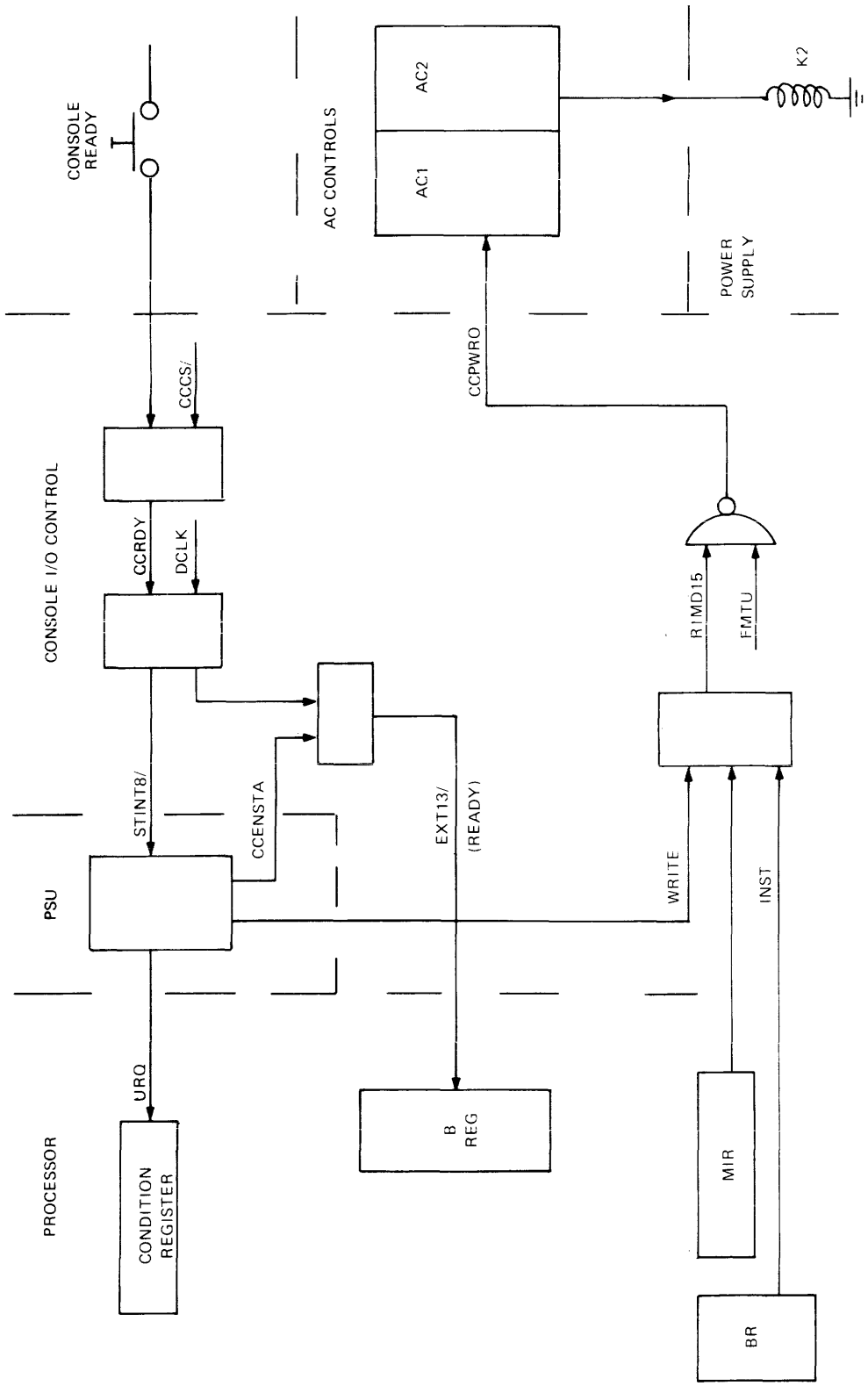


Fig. II-83 PROGRAMMATIC POWER-DOWN FROM READY PUSHBUTTON

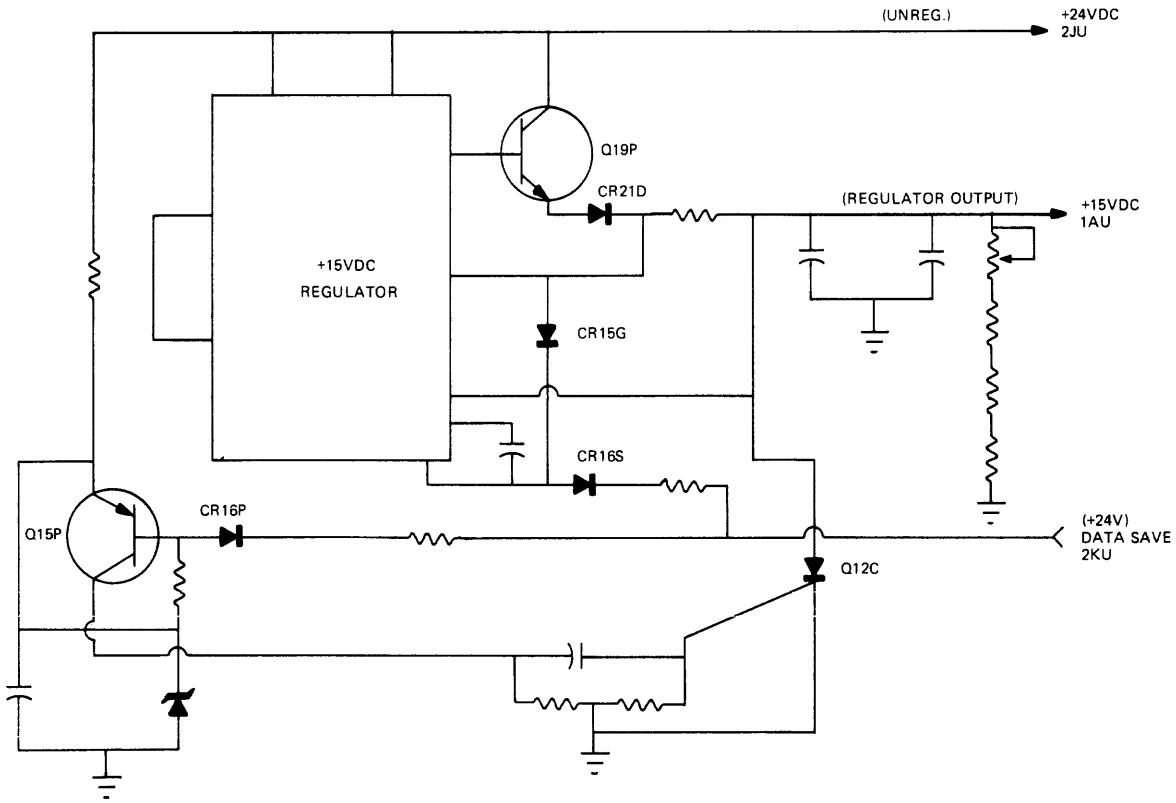


Fig. II-84 +15VDC POWER SUPPLY

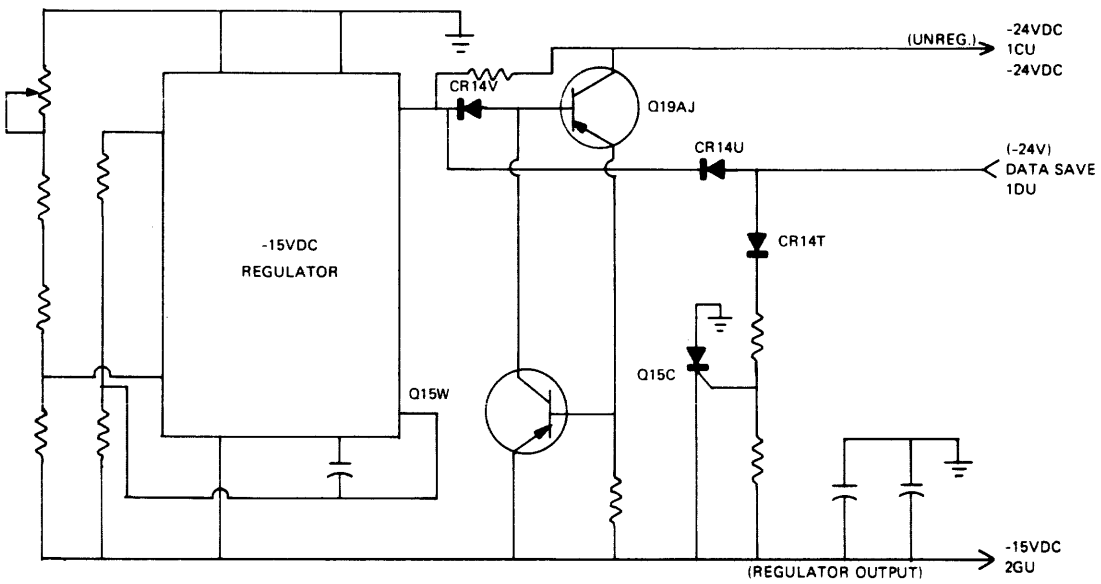


Fig. II-85 -15VDC POWER SUPPLY

B700

PROCESSOR

SECTION

III

CIRCUIT
DETAIL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

AA335830

Printed in U. S. America 9-16-74

For Form 1064482

INDEX

SECTION III INDEX

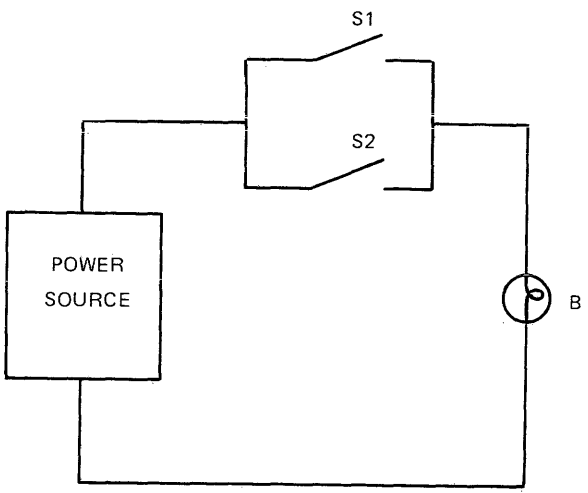
INTRODUCTION

In order for the B700 to perform its complex functions at high speeds, the use of many different electronic components, or chips, is necessary. These chips comprise the logic of the computer. They perform such functions as gating, counting, arithmetic, conversion, and storage.

It is the purpose of this section to explain the symbols and operation of these chips. With each symbol, a physical layout of the chip is shown illustrating internal pin and part numbers. The exception to this is certain symbols used to illustrate the function of the chip, rather than the actual type chip used. High speed chips may be substituted for regular chips, but the reverse is not true. In addition, an explanation on reading the Circuit List is included. Lastly, card and component location is described.

The logic is designed with two levels. A high level (TRUE) is +5 volts, and a low level (FALSE) is 0 volts. These levels represent conditions or data in the computer. The chips or logic will use these levels to perform the complex functions of the system.

For selected components a truth table is shown. This table illustrates all possible combinations of input levels and output levels, for conditions that exist simultaneously. Refer to the example below.

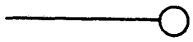


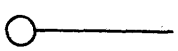
TRUTH TABLE

S1	S2	B
L	L	L
H	L	H
L	H	H
H	H	H

H – SWITCH CLOSED OR LIGHT ON
L – SWITCH OPEN OR LIGHT OFF
S1 AND S2 – SWITCHES
B – LIGHT

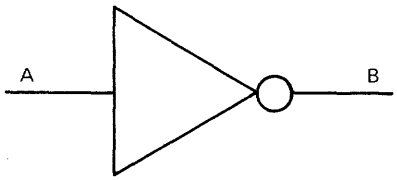
SYMBOLS


INPUT INVERTED PRIOR TO GATE.


OUTPUT INVERTED FROM GATE.

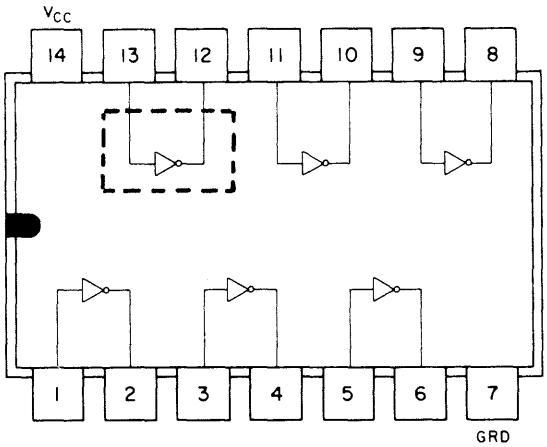
Circuit Detail

1. HEX INVERTER



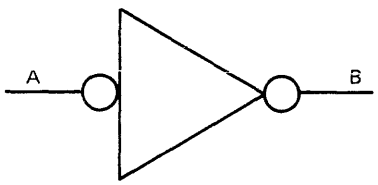
A	B
L	H
H	L

THE NAME HEX COMES FROM THE FACT THAT THERE ARE SIX INVERTERS PER CHIP. THE INPUT IS THE INVERSE OF THE OUTPUT.



1447 3532
1479 7971 (HIGH SPEED)

2. ISOLATION AMPLIFIER

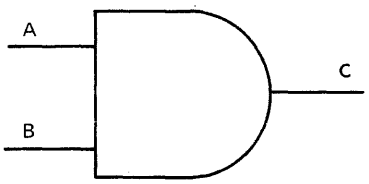


A	B
L	L
H	H

THE AMPLIFIED OUTPUT IS THE SAME LOGIC LEVEL AS THE INPUT.

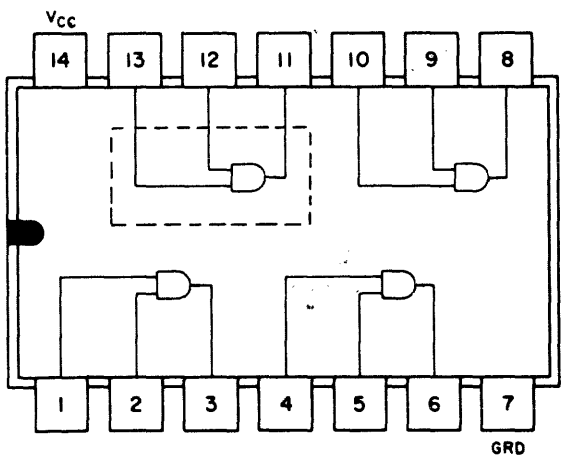
3. AND GATE

Both inputs Hi → Hi out
any Lo – Lout

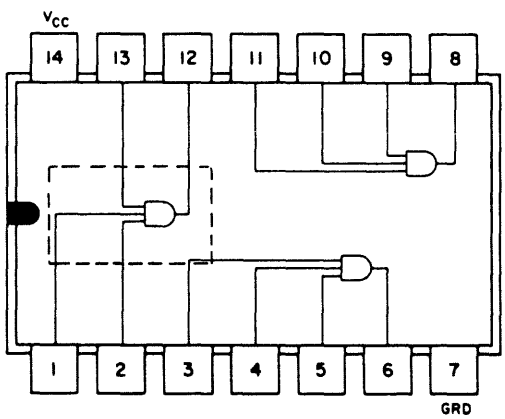


A	B	C
L	L	L
H	L	L
L	H	L
H	H	H

ALL INPUTS HIGH PRODUCE A HIGH OUTPUT.



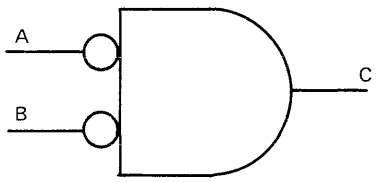
1447 3524



1447 3557

Circuit Detail

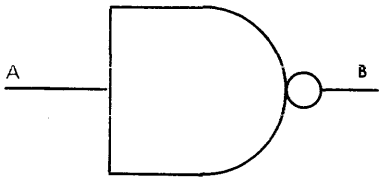
4. LOW ACTIVATED AND GATE



A	B	C
L	L	H
H	L	L
L	H	L
H	H	L

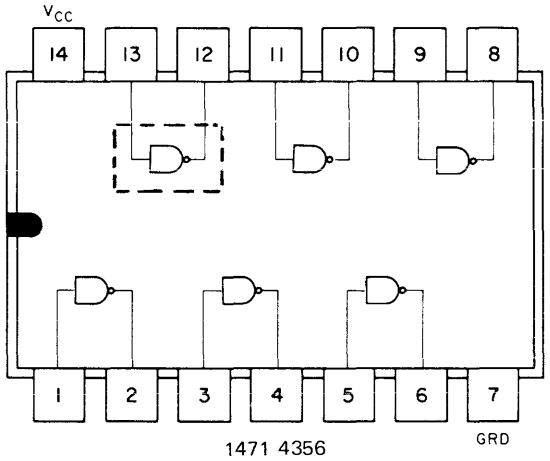
ALL INPUTS LOW PRODUCE A HIGH OUTPUT.

5. NAND GATES

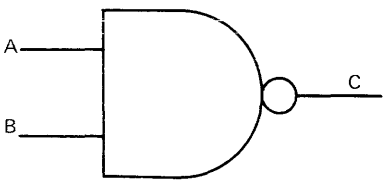


A	B
L	H
H	L

NAND GATE CHIPS MAY HAVE SINGLE INPUTS OR MULTIPLE INPUTS. THE SINGLE INPUT NAND GATE FUNCTIONS THE SAME AS THE HEX INVERTER. THE OUTPUT IS THE INVERSE OF THE INPUT

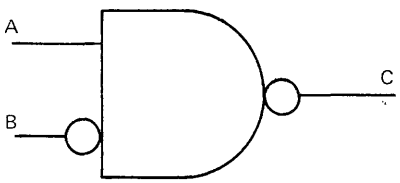


1471 4356



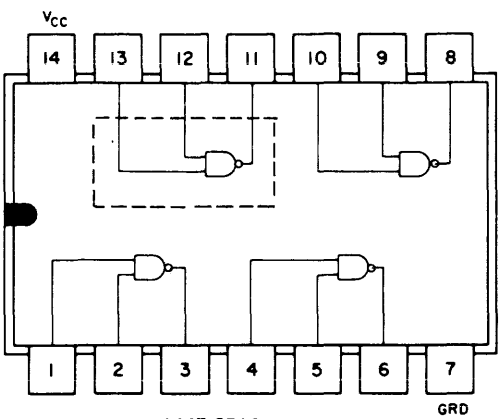
A	B	C
L	L	H
H	L	H
L	H	H
H	H	L

ALL INPUTS HIGH PRODUCE A LOW OUTPUT



A	B	C
L	L	H
H	L	L
L	H	H
H	H	H

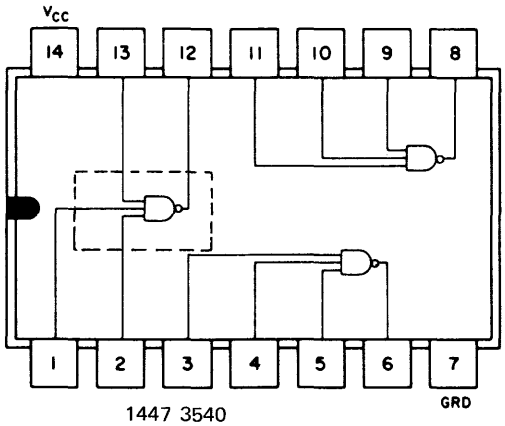
INPUT B IS INVERTED PRIOR TO THE GATE.



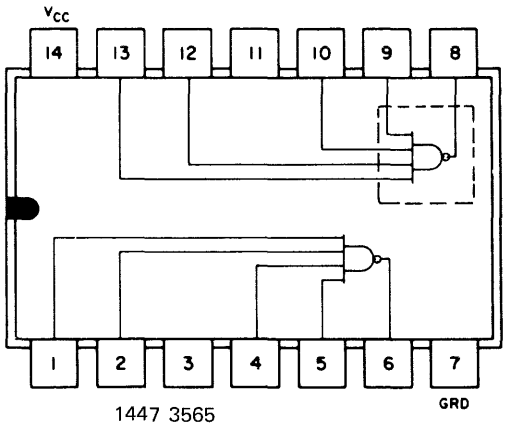
1447 3516
1447 3581*
1479 0240 (HIGH SPEED)

Circuit Detail

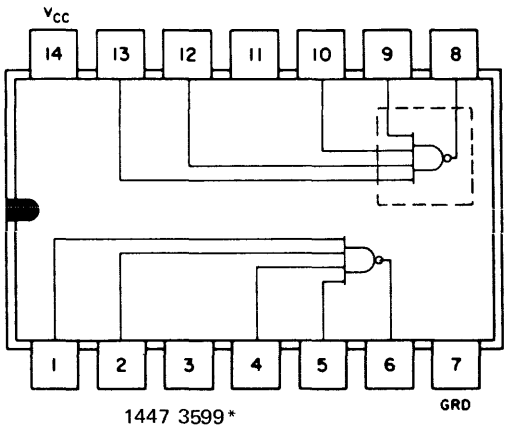
5. NAND GATES (cont'd)



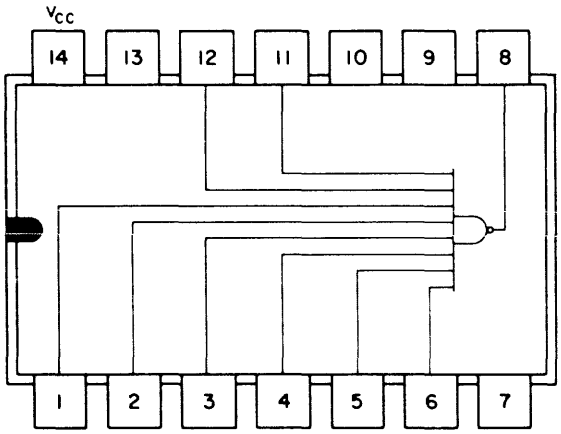
1447 3540
1486 8780 (HIGH SPEED)



1447 3565
1479 0265 (HIGH SPEED)



1447 3599*
1447 3631* (HIGH SPEED)

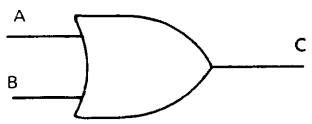


1447 3573

*THESE CHIPS ARE REFERRED TO AS NAND BUFFERS (OPEN COLLECTOR). THEY ARE USED WHEN A HIGHER DRIVE IS REQUIRED (MORE THAN THE NORMAL NUMBER OF CIRCUITS). THIS REQUIRES EXTERNAL VOLTAGE.

6. OR GATE

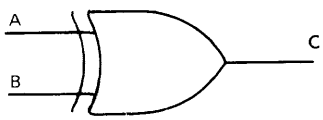
A	B	C
L	L	L
H	L	H
L	H	H
H	H	H



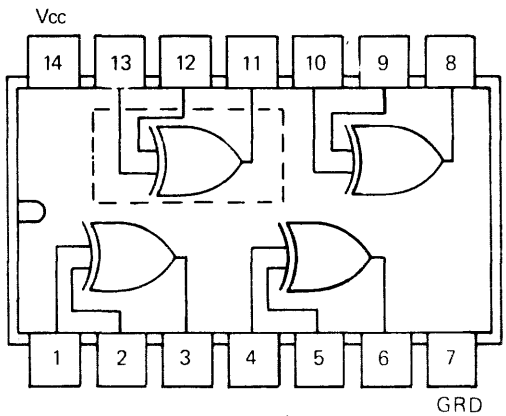
ANY INPUT OR INPUTS HIGH WILL PRODUCE A HIGH OUTPUT.

7. EXCLUSIVE OR GATE

A	B	C
L	L	L
H	L	H
L	H	H
H	H	L

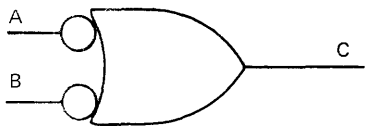


ONE INPUT HIGH AND ALL OTHERS LOW WILL PRODUCE A HIGH OUTPUT.



1447 3698

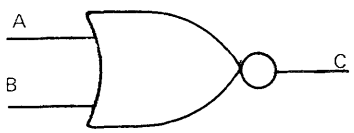
8. LOW ACTIVATED OR GATE



A	B	C
L	L	H
H	L	H
L	H	H
H	H	L

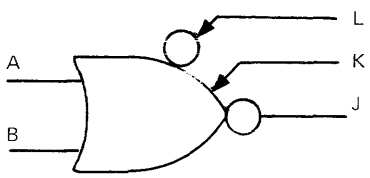
THE LOW ACTIVATED OR GATE FUNCTIONS IDENTICALLY TO THE NAND GATE. ANY INPUT OR INPUTS LOW PRODUCE A HIGH OUTPUT.

9. NOR GATE



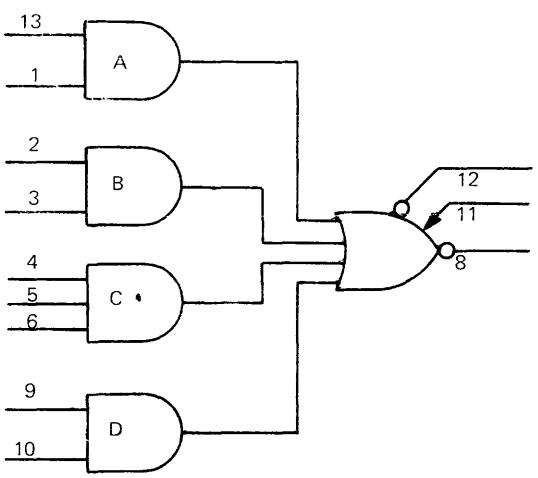
A	B	C
L	L	H
H	L	L
L	H	L
H	H	L

ANY INPUT OR INPUTS HIGH PRODUCE A LOW OUTPUT.

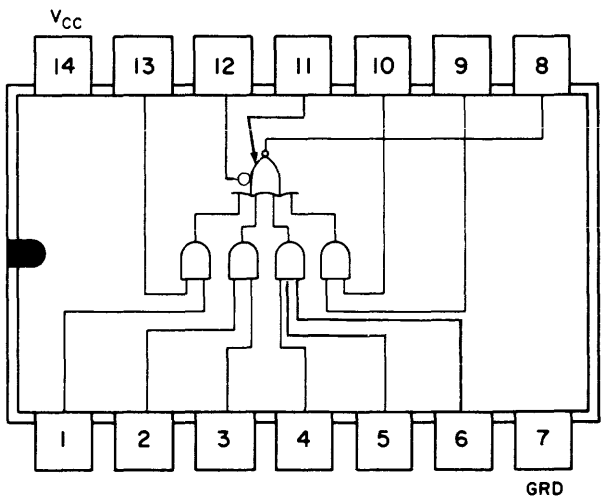


FUNCTIONS SIMILARLY TO THE REGULAR NOR GATE. L AND K ARE EXPANDER INPUTS. L IS INVERTED BEFORE THE NOR GATE AND K ACTS LIKE A AND B. A LOW SIGNAL AT L WILL PRODUCE A LOW OUTPUT. A HIGH SIGNAL AT K WILL CAUSE THE OUTPUT TO BE LOW.

10. 2x2x2x3 AND-OR-INVERTER



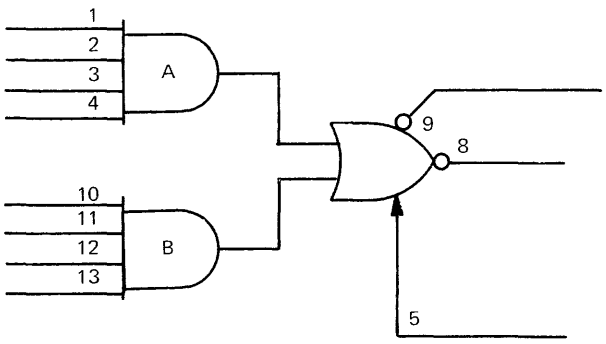
A HIGH OUTPUT FROM ANY AND GATE(S) [A, B, C OR D] WILL PRODUCE A LOW FROM THE NOR GATE



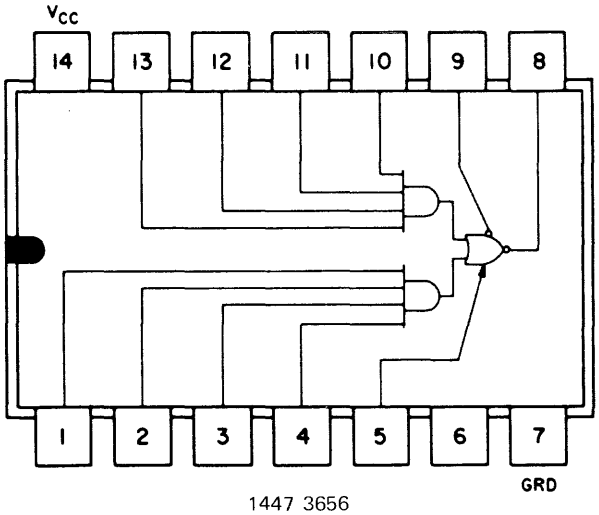
1447 3649

Circuit Detail

11. 4x4 AND-OR-INVERTER



A HIGH OUTPUT FROM ANY AND GATE(S) [A OR B] WILL PRODUCE A LOW FROM THE NOR GATE.



1447 3656

12. D TYPE EDGE TRIGGERED FLIP FLOP

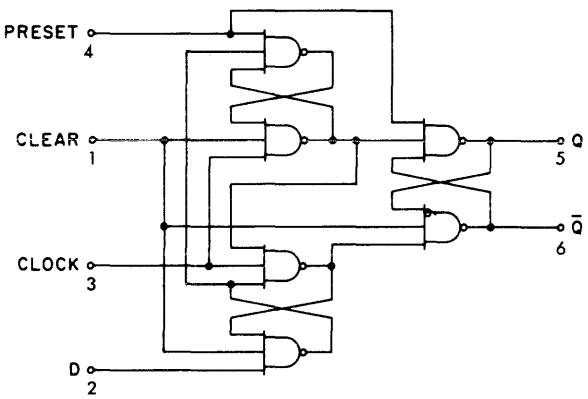
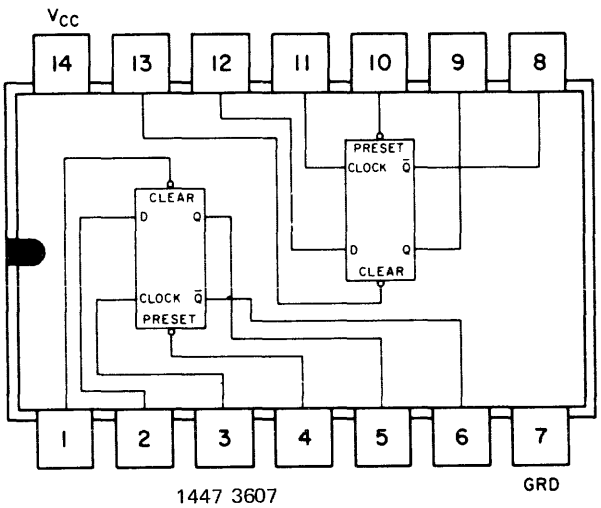


FIG. 12A

THERE ARE TWO IDENTICAL FLIP-FLOPS (FIG. 12A) ON EACH CHIP (FIG. 12B).



1447 3607
1447 3623 (HIGH SPEED)

FIG. 12B

t_n	t_n+1	
INPUT D	OUTPUT Q	OUTPUT Q
L	L	H
H	H	L

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse.

FIG. 12C

12. D TYPE EDGE TRIGGERED FLIP FLOP (cont'd)

The output labeled Q (Fig. 12A) is the set output, and the output labeled $\overline{Q}$ (Q not) is the reset output. These are complementary, meaning their levels are always opposite. When Q is high the FF is set. It is reset when Q is low. The last condition (set or reset) does not change unless the inputs change.

Preset or Clear low at any time, will unconditionally set or reset the FF, respectively.

The D – input is used to control the output at clock times. A clock is a series of continuous pulses. Clock pulses are of constant width and repetition rate. The output will change on the low to high transition (leading edge) of the clock pulse. The D – input can only be active when Preset and Clear are both high. Refer to the truth table for results of a D – input (Fig. 12C).

13. J-K MASTER SLAVE FF

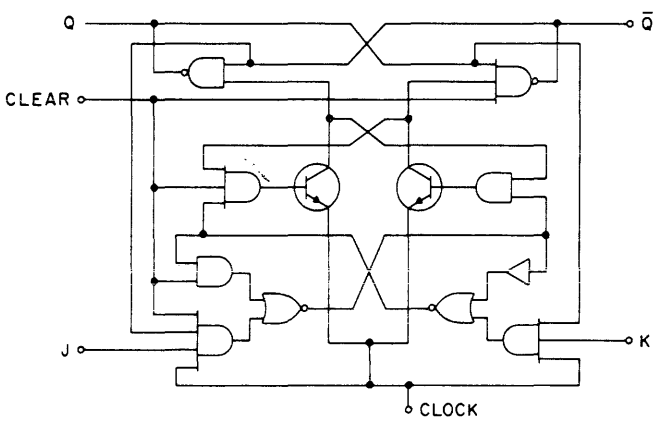
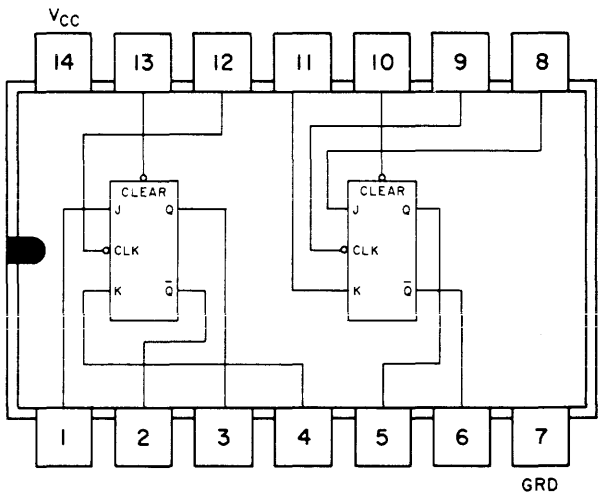


FIG. 13A



1447 3615

FIG. 13B

THERE ARE TWO IDENTICAL FLIP FLOPS (FIG. 13A) ON EACH CHIP (FIG. 13B).

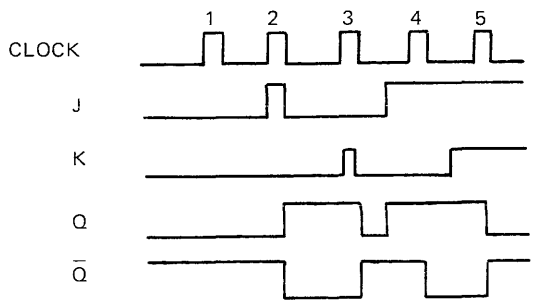


FIG. 13C TIMING

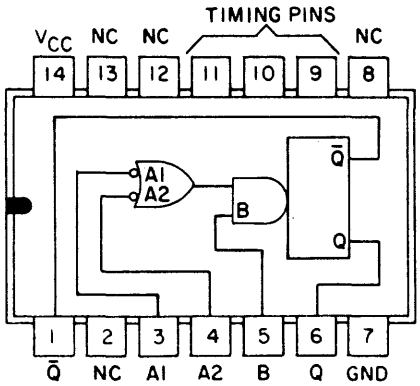
CLOCK	J	K	Q	$\overline{Q}$
1	L	L	L	H
2	H	L	H	L
3	L	H	L	H
4	H	H	OPPOSITE TO Toggles	
5	H	H	LAST CONDITION	

NOTE: IF THE J AND K INPUTS STAY HIGH, THE FF WILL COMPLEMENT ON EVERY CLOCK PULSE.

Clear as a low input will unconditionally reset the FF (Fig. 13A and B). The J and K inputs (set and reset, respectively) control the output, if Clear is high. The output changes states only when the clock pulse (refer to D – FF) goes from a high to a low (Fig. 13C). This is the trailing edge of the clock pulse. Initially, a reset condition was assumed for the truth table and timing diagram. If the FF was set initially, no change would occur at the output until the third clock pulse. When J and K inputs are low, no change in the outputs takes place unless the FF is set and Clear goes low.

14. MQNOSTABLE MULTIVIBRATOR

Circuit Detail



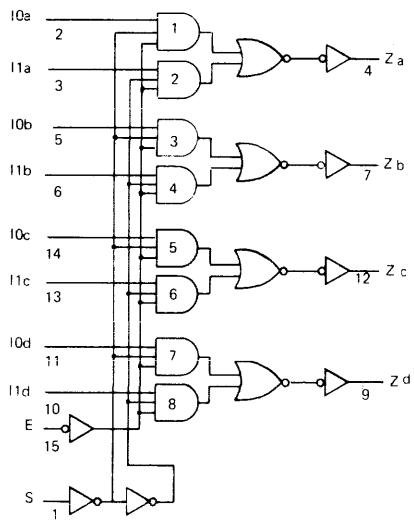
1447 3706
FIG. 14A

A1	A2	B	OUTPUT
L	L	H	ONE SHOT
H	L	H	ONE SHOT
L	H	H	ONE SHOT
H	H	H	
L	L	L	
H	L	L	INHIBIT
L	H	L	
H	H	L	

FIG. 14B

Input B at the And Gate (Fig. 14A) is to enable or inhibit the monostable. Another name for this circuit is a one shot. When B is high the FF can be triggered. This is done by a low input to either A1 or A2. The resulting output is a single pulse, whose width is controlled by external timing components. Therefore, after triggering, the input has no effect on the output. The output pulse width may be varied from 40 nanoseconds to 40 seconds. With no external timing components the circuit produces a 30 nanosecond pulse. If the input trigger repetition time is less than the output pulse width, the output will not change as long as this condition exists. The previous statement has one exception – the first trigger.

15. QUAD 2 INPUT MULTIPLEXOR



1447 3797
FIG. 15A

$\bar{E}$	S	INPUT GATES
H	L	NONE
H	H	NONE
L	L	1, 3, 5, AND 7
L	H	2, 4, 6, AND 8

FIG. 15B

To enable the And Gates (Fig. 15A), $\bar{E}$ must be low. Only one And Gate, feeding each Nor Gate, will be enabled at any one time. The level of S determines which And Gates are enabled (Fig. 15B). The enabled And Gates will transfer Iox and Ilx to Zx, where x represents a, b, c, or d. This circuit selects one set of four bits (Ioa, Iob, Ioc, Iod) or the other(Ila, Ilb, Ilc, Ild).

16. DUAL TWO-LINE TO FOUR-LINE DECODER/DEMULTIPLEXOR MODULE

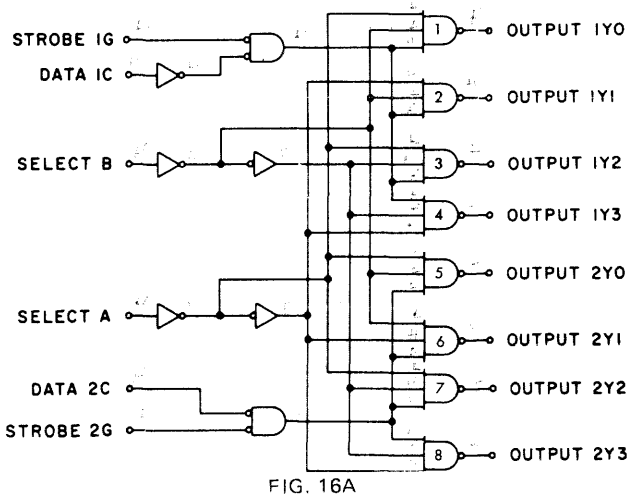
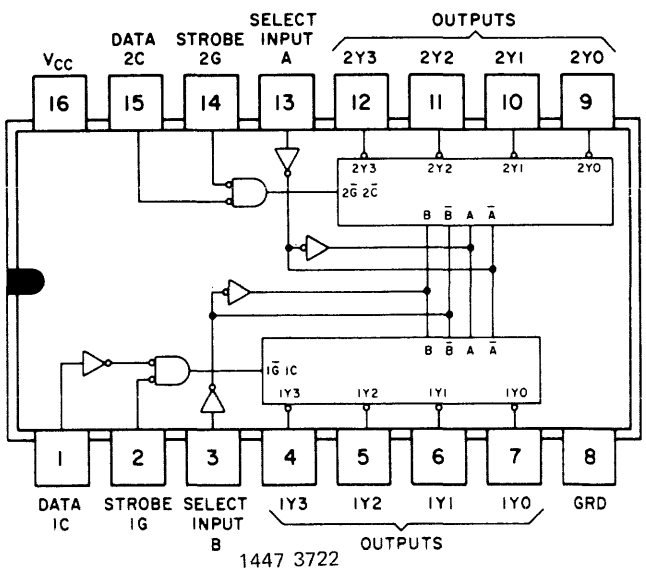


FIG. 16A



1447 3722
FIG. 16B

Circuit Detail

16. DUAL TWO-LINE TO FOUR-LINE DECODER/DEMULTIPLEXOR MODULE (cont'd)

With both strobes low (Fig. 16A), serial input data at 1C and 2C will transfer to the outputs. Select A and Select B inputs enable corresponding pairs of output gates. Each input data line (1C and 2C) feeds four output lines in steps (0, 1, 2, and 3). Refer to Figs. 16C and D.

ASSUME:

1. STROBES 1G AND 2G ARE LOW
2. DATA PULSES INPUT AT 1C AND 2C.

SELECT A	SELECT B	OUTPUT GATES
L	L	1 AND 5
H	L	2 AND 6
L	H	3 AND 7
H	H	4 AND 8

FIG. 16C

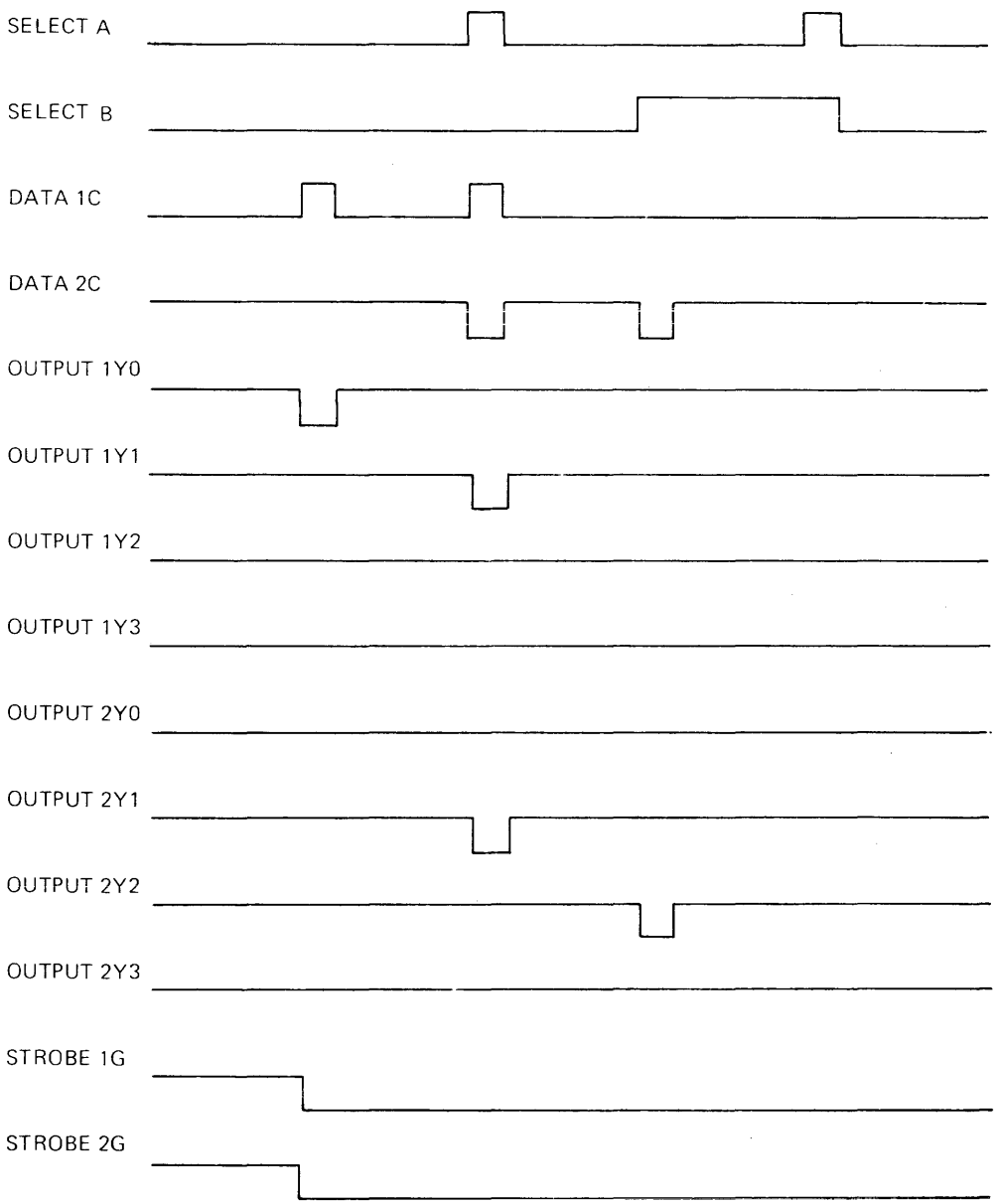


FIG. 16D

Circuit Detail

17. DUAL FOUR-LINE TO ONE-LINE DATA SELECTOR/MULTIPLEXOR MODULE

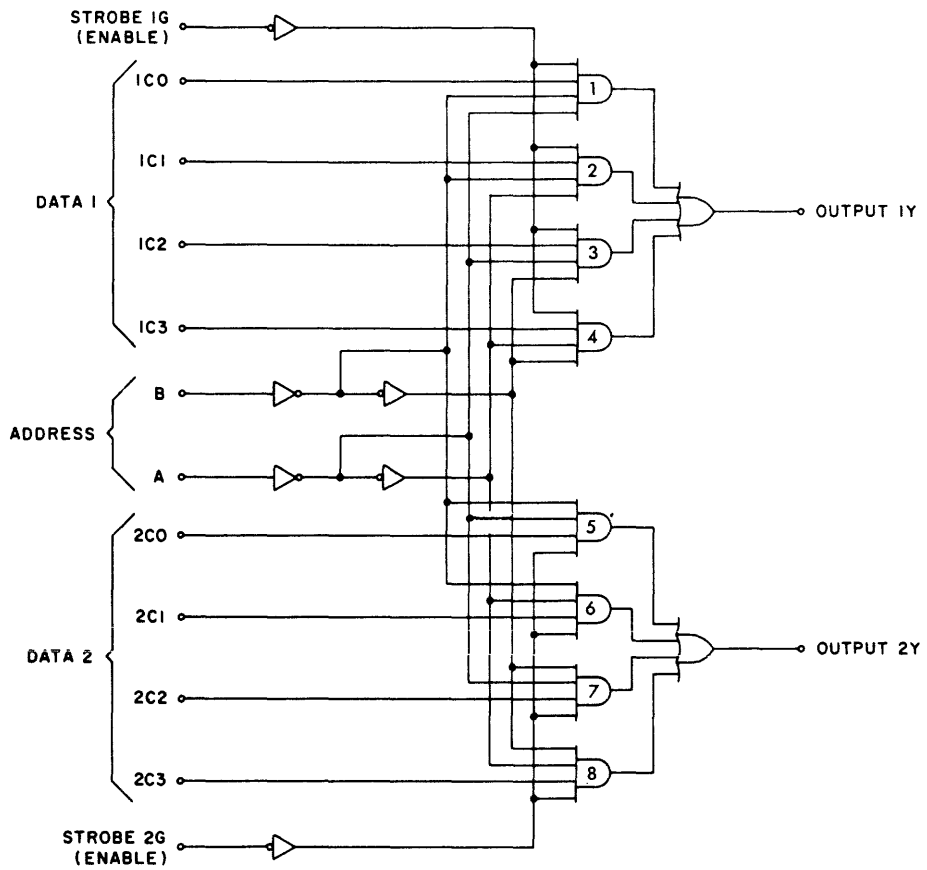
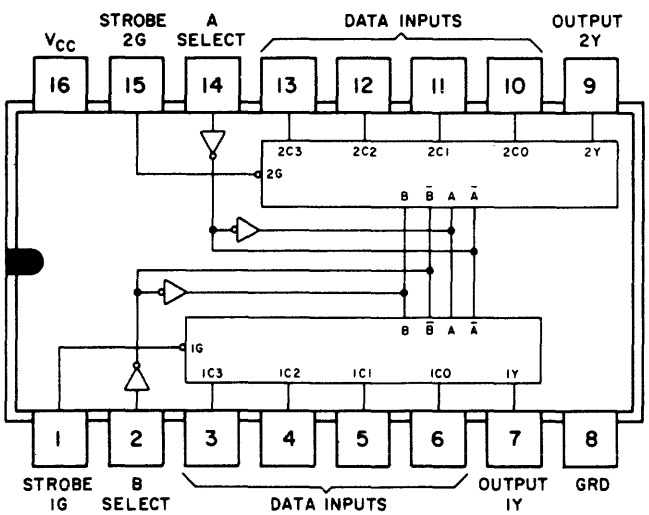


FIG. 17A

With both strobes low (Fig. 17A), parallel input data at 1 and 2 will transfer to the outputs, serially as controlled by the address inputs. Address A and Address B inputs enable corresponding pairs of input gates (1 through 8). Each set of input data lines (1C0, 1C1, 1C2, and 1C3 or 2C0, 2C1, 2C2, and 2C3) feeds one output (1Y or 2Y). Refer to Fig. 17C and D.



1447 3714

FIG. 17B

ASSUME:

1. STROBES 1G AND 2G ARE LOW.
2. DATA INPUT AT 1 AND 2.

ADDRESS A	ADDRESS B	INPUT GATES
L	L	1 AND 5
H	L	2 AND 6
L	H	3 AND 7
H	H	4 AND 8

FIG. 17C

17. DUAL FOUR-LINE TO ONE-LINE DATA SELECTOR/MULTIPLEXOR MODULE (cont'd)

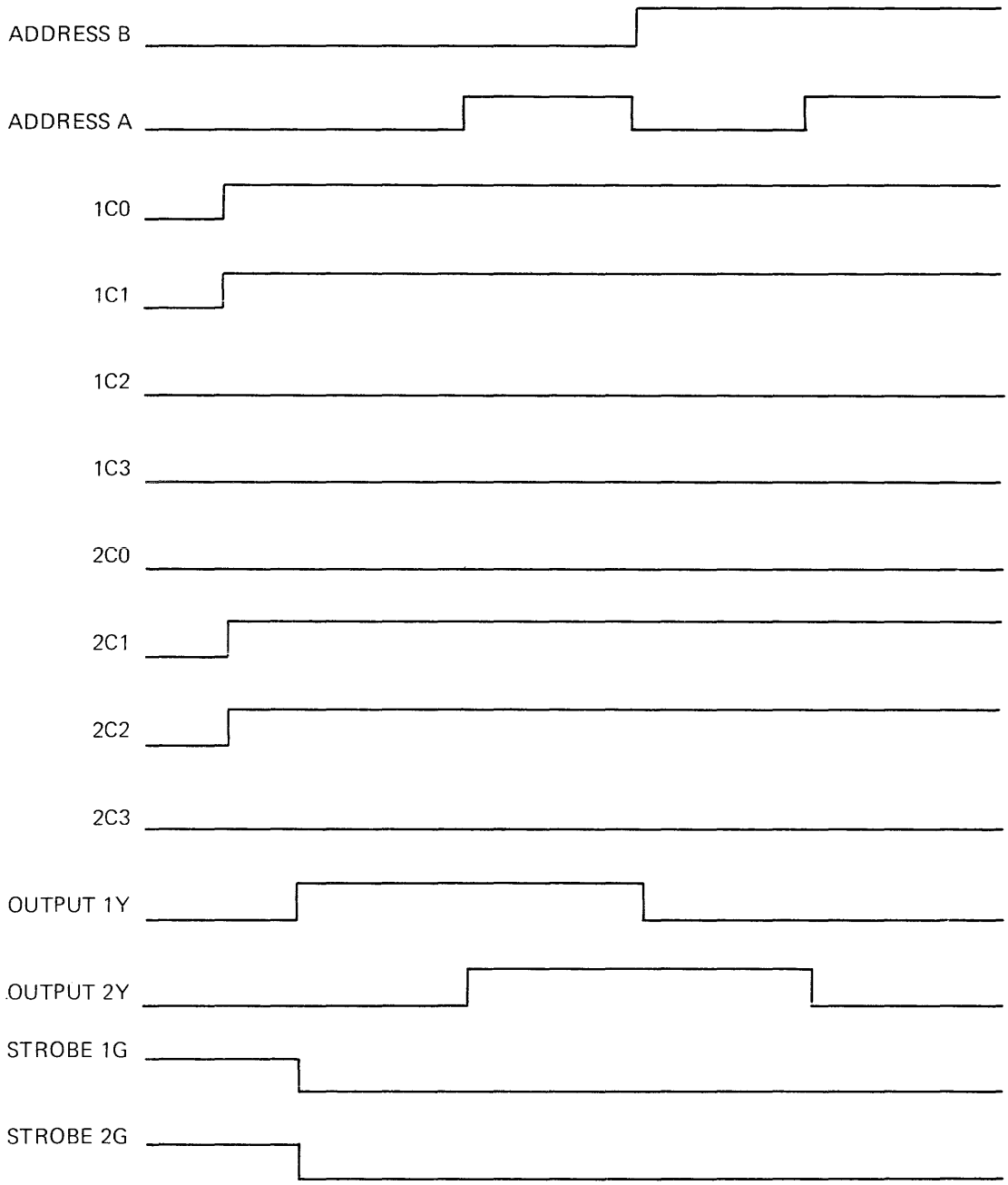


FIG. 17D

Circuit Detail

18. SIXTEEN BIT DATA SELECTOR/MULTIPLEXOR MODULE

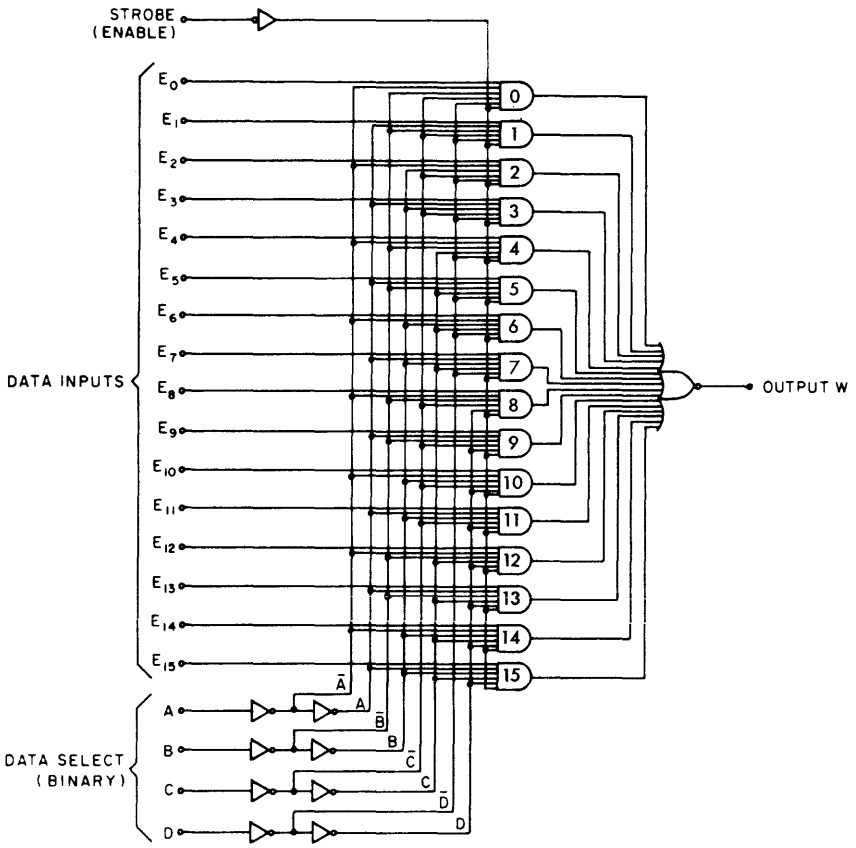


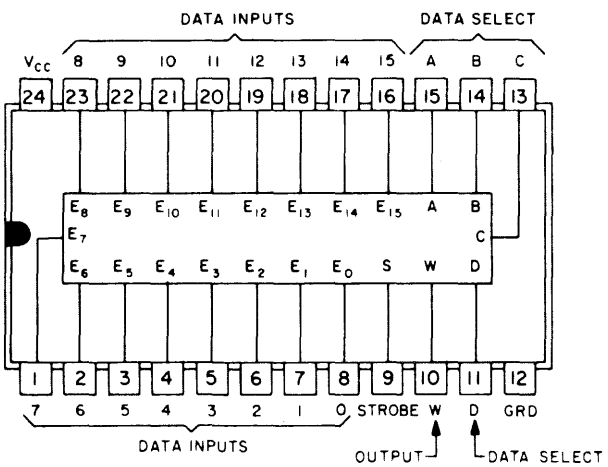
FIG. 18A

ASSUME:

STROBE IS LOW.

DATA SELECT				INPUT
D	C	B	A	GATE
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

FIG. 18C



1447 4324

FIG. 18B

With strobe low (Fig. 18A) parallel data inputs are transferred to output W, serially. Data Select will enable each gate sequentially. The binary input from Data Select enables the corresponding gate. Refer to Fig. 18C.

Circuit Detail

19. FOUR BIT BINARY COUNTER MODULE

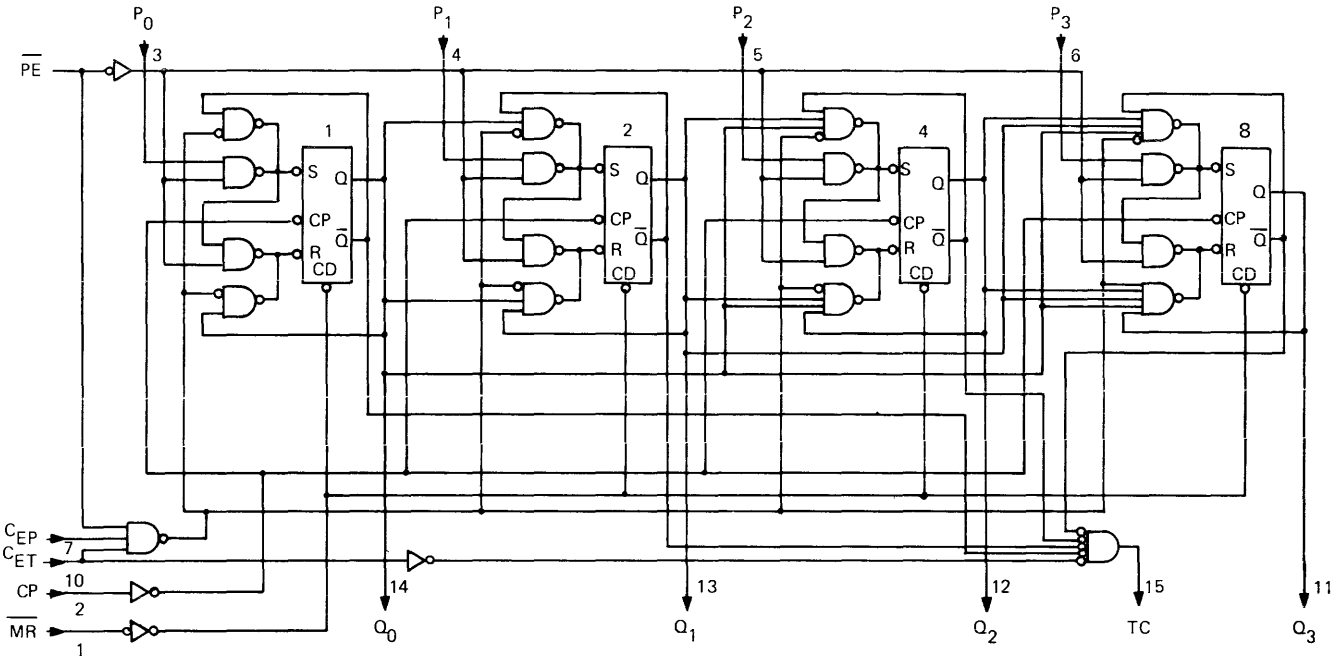
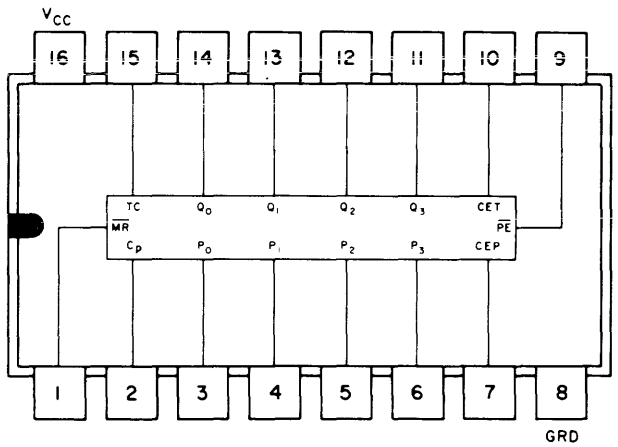


FIG. 19A



1447 3771

FIG. 19B

MODE SELECTION

$\overline{PE}$	CE (COUNT ENABLE)	MODE
H	H	COUNT UP
H	L	NO CHANGE
L	X	PRESETTING

WHERE CE = CEP · CET

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE CONDITION

FIG. 19C

THERE IS ONE CIRCUIT (FIG. 19A) PER CHIP (FIG. 19B).

PIN NAMES

$\overline{PE}$	PARALLEL ENABLE (ACTIVE LOW) INPUT
P_0, P_1, P_2, P_3	PARALLEL INPUTS
CEP	COUNT ENABLE PARALLEL INPUT
CET	COUNT ENABLE TRICKLE INPUT
Cp	CLOCK ACTIVE HIGH GOING EDGE INPUT
$\overline{MR}$	MASTER RESET (ACTIVE LOW) INPUT
Q_0, Q_1, Q_2, Q_3	PARALLEL OUTPUTS
TC	TERMINAL COUNT OUTPUT

When $\overline{MR}$ is low (Fig. 19A) all four FF's will reset. To allow operation of the counter, $\overline{MR}$ must be high. Each FF has a binary weight as shown in Fig. 19A.

When $\overline{PE}$ is low, the FF's can be preset to a number between 0 and 15 by the parallel inputs (P0, P1, P2, and P3). In the count up mode (Fig. 19C), counting will start either from zero or a preset value. FF one is enabled in the count up mode and complements on every clock pulse. As each FF sets, the next one is enabled to be set.

Circuit Detail

20. FOUR BIT SHIFT REGISTER MODULE

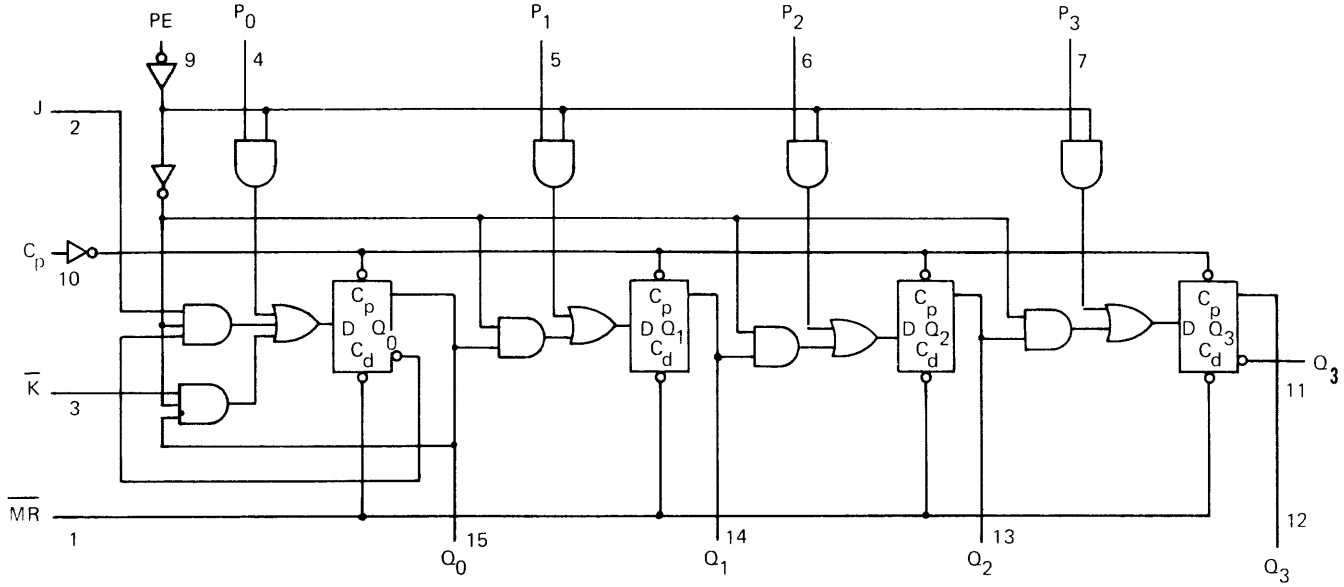
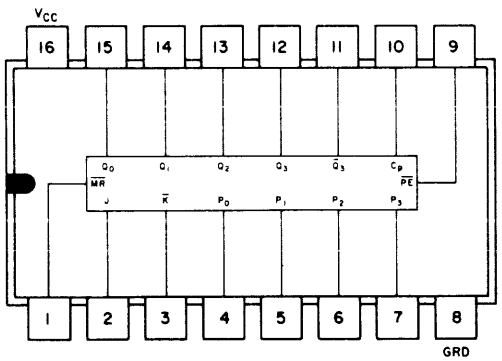


FIG. 20A



1447 3755

FIG. 20B

PIN NAMES

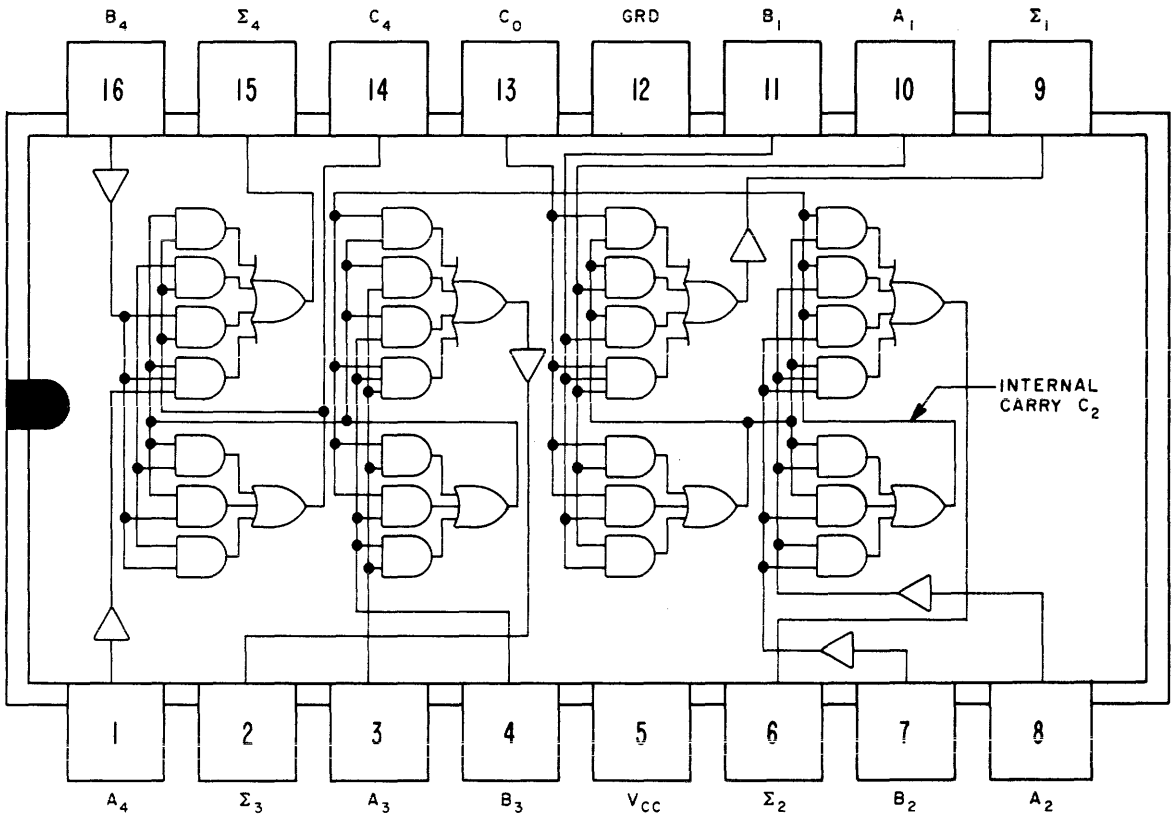
$\overline{PE}$	PARALLEL ENABLE (ACTIVE LOW) INPUT
P_0, P_1, P_2, P_3	PARALLEL INPUTS
J	FIRST STAGE J (ACTIVE HIGH) INPUT
$\overline{K}$	FIRST STAGE K (ACTIVE LOW) INPUT
Cp	CLOCK ACTIVE HIGH GOING EDGE INPUT
$\overline{MR}$	MASTER RESET (ACTIVE LOW) INPUT
Q_0, Q_1, Q_2, Q_3	PARALLEL OUTPUTS
$\overline{Q}_3$	COMPLEMENTARY LAST STAGE OUTPUT

FIG. 20C

$\overline{MR}$ resets all FF's when low (Fig. 20A). This signal must be high to allow operation of the shift register. With $\overline{PE}$ low, the parallel inputs (P0, P1, P2, and P3) determine the next condition of the shift registers. When $\overline{PE}$ is high, a one bit shift to the right (during clock time) is performed with data entering the first stage FFthrough the JK inputs.

Circuit Detail

21. FOUR BIT BINARY FULL ADDER MODULE



1447 4316
FIG. 21A

INPUT							OUTPUT					
				WHEN C_0=L			WHEN C_0=H					
						WHEN C_2=L						WHEN C_2=H
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4			
L	L	L	L	L	L	L	H	L	L			
H	L	L	L	H	L	L	L	H	L			
L	H	L	L	H	L	L	L	H	L			
H	H	L	L	L	H	L	H	H	L			
L	L	H	L	L	H	L	H	H	L			
H	L	H	L	H	H	L	L	L	H			
L	H	H	L	H	H	L	L	L	H			
H	H	H	L	L	L	H	H	L	H			
L	L	L	H	L	H	L	H	H	L			
H	L	L	H	H	H	L	L	L	H			
L	H	L	H	H	H	L	L	L	H			
H	H	L	H	L	L	H	H	L	H			
L	L	H	H	L	L	H	H	L	H			
H	L	H	H	H	L	H	L	H	H			
L	H	H	H	H	L	H	L	H	H			
H	H	H	H	L	H	H	H	H	H			

FIG. 21B

SOLUTION: ASSUME C0 = L

1. FROM CHART
   a. E1 = 0, E2 = 0 AND C2 = 1
   b. E3 = 1, E4 = 1 AND C4 = 0
2. ANSWER 0 0 1 1 = 12

REFER TO FIG. 21A

NOTE: INPUT CONDITIONS AT A1, A2, B1, B2, AND C0 ARE USED TO DETERMINE OUTPUTS E1 AND E2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, A4, B3, AND B4 ARE THEN USED TO DETERMINE OUTPUTS E3, E4, AND C4.

C0 – CARRY FROM LAST TWO DIGITS
C2 – CARRY FROM A1 + B1, A2 + B2
C4 – CARRY FROM PRESENT TWO DIGITS

EXAM:	7	+	5	=	12
BITS	A1	A2	A3	A4	
	1	1	1	0	= 7
BITS	B1	B2	B3	B4	
	1	0	1	0	= 5

Circuit Detail

22. FOUR BIT BINARY ARITHMETIC LOGIC UNIT

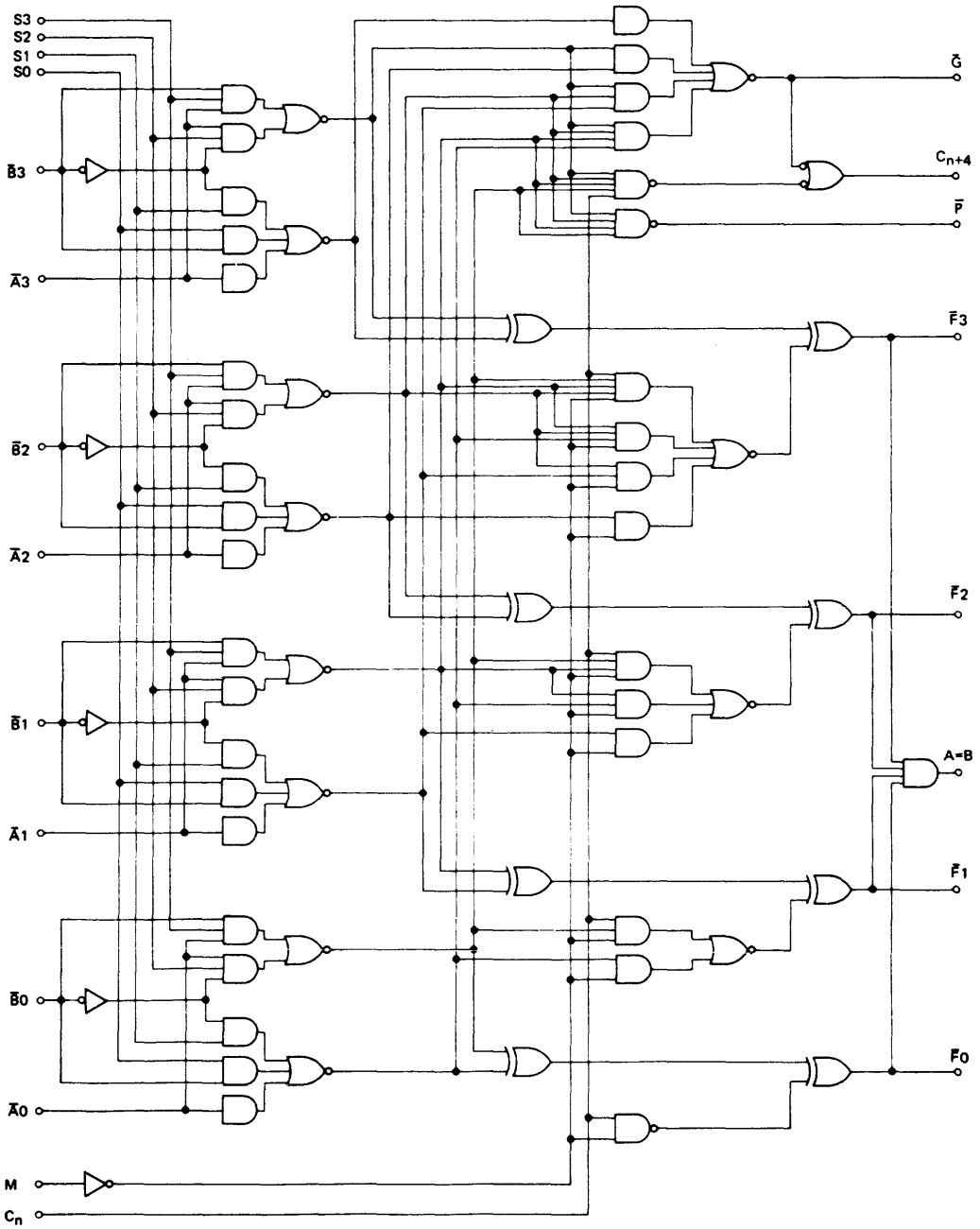


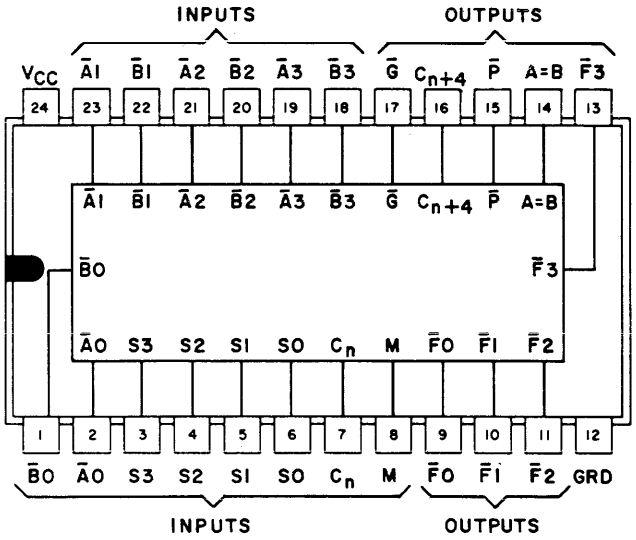
FIG. 22A

The arithmetic logic unit (Fig. 22A) can perform 16 binary arithmetic operations (Figs. 22C and D) on two four bit digits. These operations are selected by the four function – select lines (S0, S1, S2, and S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries are enabled by applying a low-level voltage to the mode control input (M). A full look-ahead scheme is provided for fast, simultaneous carry generation with a group carry propagate (P) and carry generate (G) for four bits. When the ripple-carry input (Cn) and ripple-carry output (Cn + 4) are used, addition of four bits is accomplished in 24 nanoseconds and addition of two eight-bit characters is accomplished in 36 nanoseconds.

Circuit Detail

22. FOUR BIT BINARY ARITHMETIC LOGIC UNIT (cont'd)

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A minus B minus 1 which requires the end-around or forced carry to provide A minus B. Refer to Fig. 22E for the various designators described in the above text.



1447 3730
FIG. 22B

TABLE OF ARITHMETIC OPERATIONS

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOW LEVELS ACTIVE	HIGH LEVELS ACTIVE
L	L	L	L	F = A MINUS 1	F = A
L	L	L	H	F = AB MINUS 1	F = A + B
L	L	H	L	F = AB MINUS 1	F = A + B
L	L	H	L	F = MINUS 1 (2'S COMPLE	F = MINUS 1 (2'S COMPLEMENT)
L	H	L	L	F = A PLUS [A+B]	F = A PLUS AB
L	H	L	H	F = AB PLUS [A+B]	F = [A+B] PLUS AB
L	H	H	L	F = A MINUS B MINUS 1	F = A MINUS B MINUS 1 *
L	H	H	H	F = A + B	F = AB MINUS 1
H	L	L	L	F = A PLUS [A+B]	F = A PLUS AB *
H	L	L	H	F = A PLUS B	F = A PLUS B *
H	L	H	L	F = AB PLUS [A+B]	F = [A+B] PLUS AB
H	L	H	H	F = A + B	F = AB MINUS 1
H	H	L	L	F = A PLUS A1	F = A PLUS A1
H	H	L	H	F = AB PLUS A	F = [A+B] PLUS A *
H	H	H	L	F = AB PLUS A	F = [A+B] PLUS A
H	H	H	H	F = A	F = A MINUS 1

NOTES: MODE CONTROL (M) AND C_n LOW.

* = ARITHMETIC OPERATION PERFORMED BY ALU IN INTERPRETER

1 = EACH BIT IS SHIFTED TO NEXT MORE SIGNIFICANT POSITION.

FIG. 22C

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION–SELECT INPUTS
C_n	7	CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GRD	12	GROUND

FIG. 22E

TABLE OF LOGIC FUNCTIONS

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	NEGATIVE LOGIC	POSITIVE LOGIC
L	L	L	L	F = A	F = A
L	L	L	H	F = AB	F = A + B *
L	L	H	L	F = A + B	F = AB *
L	L	H	H	F = LOGICAL H	F = LOGICAL L
L	H	L	L	F = A + B	F = AB *
L	H	L	H	F = B	F = B
L	H	H	L	F = A + B	F = A + B *
L	H	H	H	F = A + B	F = AB *
H	L	L	L	F = AB	F = A + B *
H	L	L	H	F = A + B	F = A + B *
H	L	H	L	F = B	F = B
H	L	H	H	F = A + B	F = AB *
H	H	L	L	F = LOGICAL L	F = LOGICAL H
H	H	L	H	F = AB	F = A + B *
H	H	H	L	F = AB	F = A + B *
H	H	H	H	F = A	F = A

NOTES: MODE CONTROL (M) HIGH, C_n IRRELEVANT.

* = LOGIC FUNCTION PERFORMED BY ALU IN INTERPRETER.

FIG. 22D

Circuit Detail

23. LOOK AHEAD CARRY GENERATOR MODULE

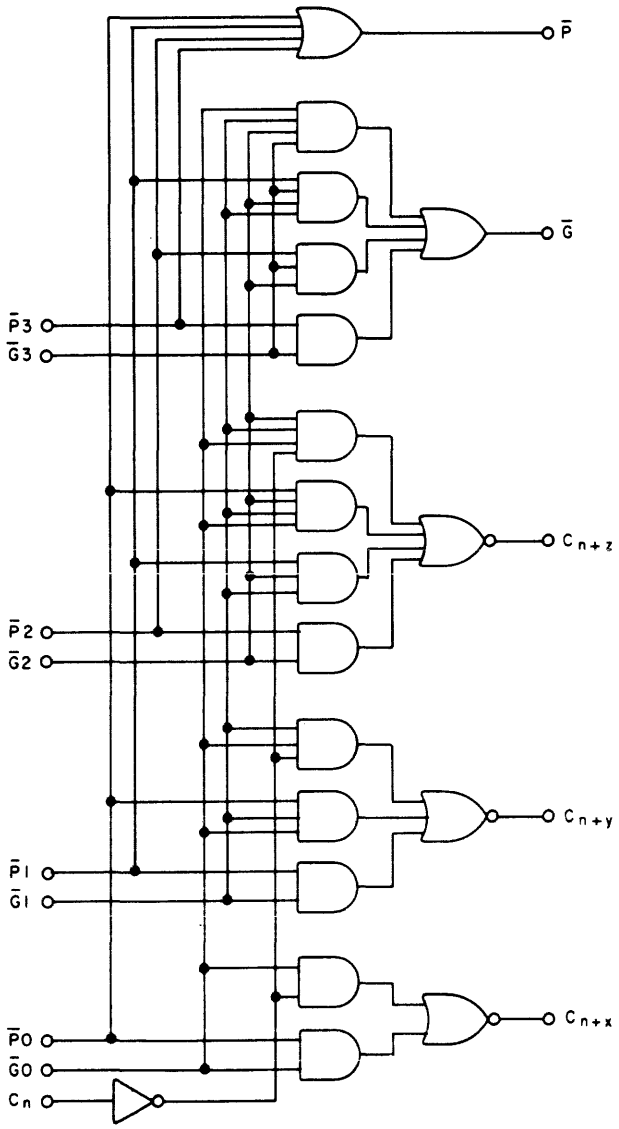
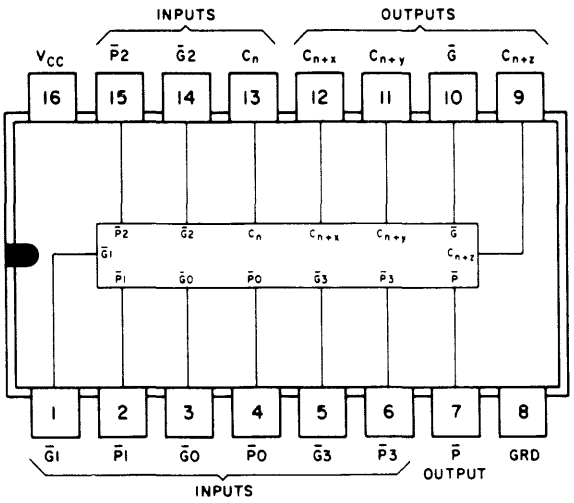


FIG. 23A



1447 3748

FIG. 23B

PIN DESIGNATIONS

DESIGNATION	PIN NOS	FUNCTION
$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3$	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
$\bar{P}0, \bar{P}1, \bar{P}2, \bar{P}3$	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	CARRY OUTPUTS
$\bar{G}$	10	ACTIVE-LOW CARRY GENERATE OUTPUT
$\bar{P}$	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GRD	8	GROUND

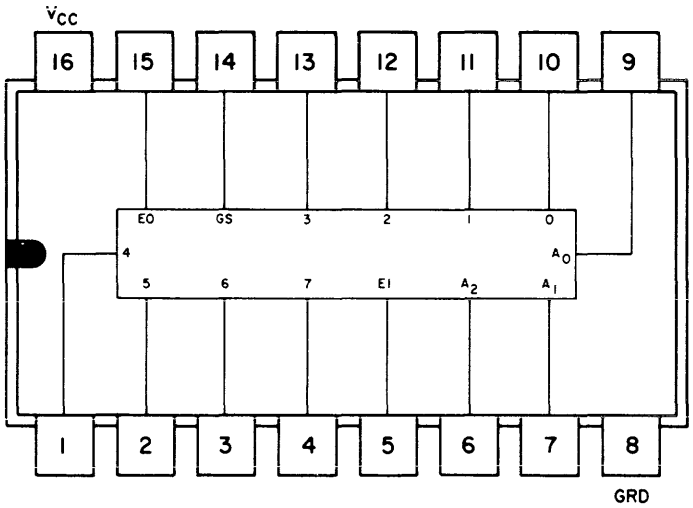
FIG. 23C

This look-ahead carry generator module (Fig. 23A) is capable of anticipating a carry across four binary adders or group of adders. Carry, generate-carry, and propagate-carry functions are provided.

The module is used in conjunction with the arithmetic logic unit module to provide high-speed look-ahead capability for up to n-bit words. Carry inputs and outputs of the module are in their form and the carry propagate (P) and the carry generate (G) are in the negated form; therefore, the carry (input, outputs, generate, and propagate) functions of the look-ahead circuit are implemented in the compatible forms.

Circuit Detail

24. EIGHT INPUT PRIORITY ENCODER MODULE



1447 3789
FIG. 24A

E1	0	1	2	3	4	5	6	7	GS	A_0	A_1	A_2	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

FIG. 24B

This module is a multipurpose encoder (Fig. 24A) designed to accept eight active low-level inputs and produce a binary weighted output code of the highest order input.

A priority is assigned to each active low level input (Fig.24B) so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output. (Input seven has the highest priority.) An active low level enable input (E1) and active low level enable output (E0) are provided to expand priority encoding to more inputs. This is accomplished by connecting the more significant encoder enable output (E0) to the next less significant encoder enable input (E1). In addition, a group signal (GS) is provided which is active if any input and E1 is a low level.

25. 256-BIT, BIPOLAR, RANDOM ACCESS MEMORY MODULE (RAM)

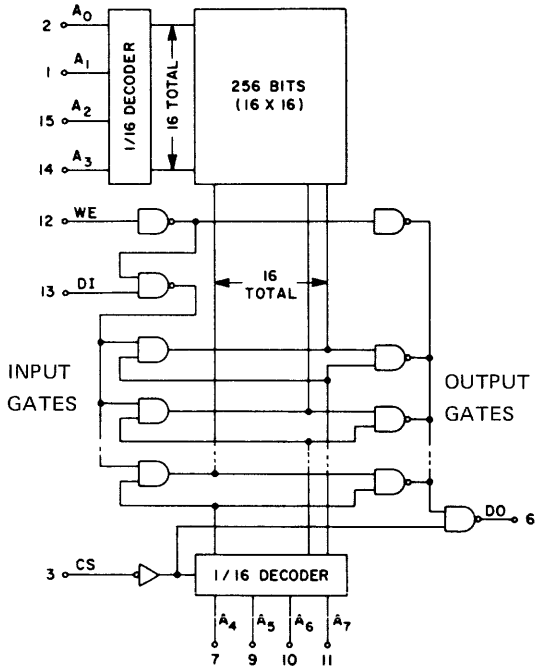
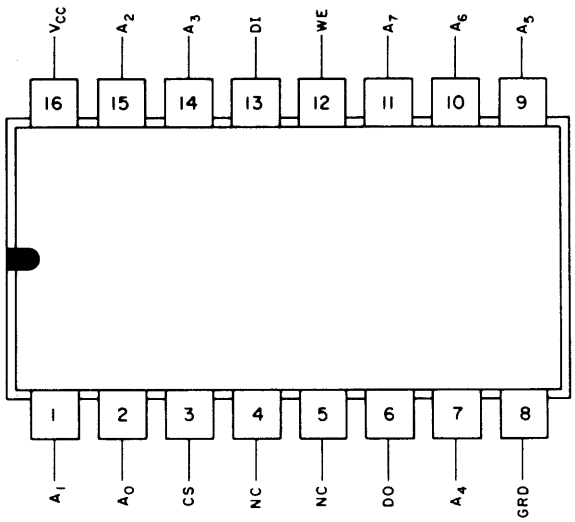


FIG. 25A



1447 8598
FIG. 25B

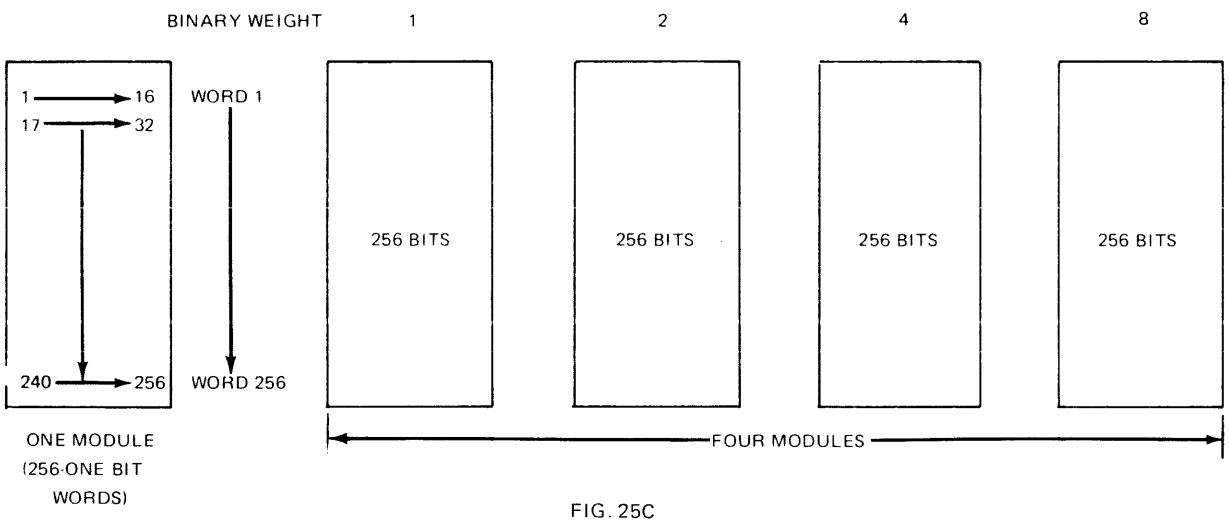


FIG. 25C

The high speed 256-bit RAM module (Fig. 25A) is organized in a 16 x 16 bit configuration. Each module contains 256 bits. Refer to Fig. 25C.

In the example above, four 256 bit modules are represented. if another bit is needed, another module would be required, etc.

On chip address decoding, A0 through A7 (Fig. 25A) is divided into two groups: the least significant bits and the most significant bits of the address. The four least significant bits address one set of sixteen bits. The four most significant bits address one bit within the sixteen. The output is enabled by Chip Select (CS) being at a low level. If Write Enable (WE) is at a high level, the addressed bit is read out at DO. If Write Enable is at a low level and Data In (DI) is active, the incoming bit will be written into the module.

26. 256x4 READ ONLY MEMORY (ROM)

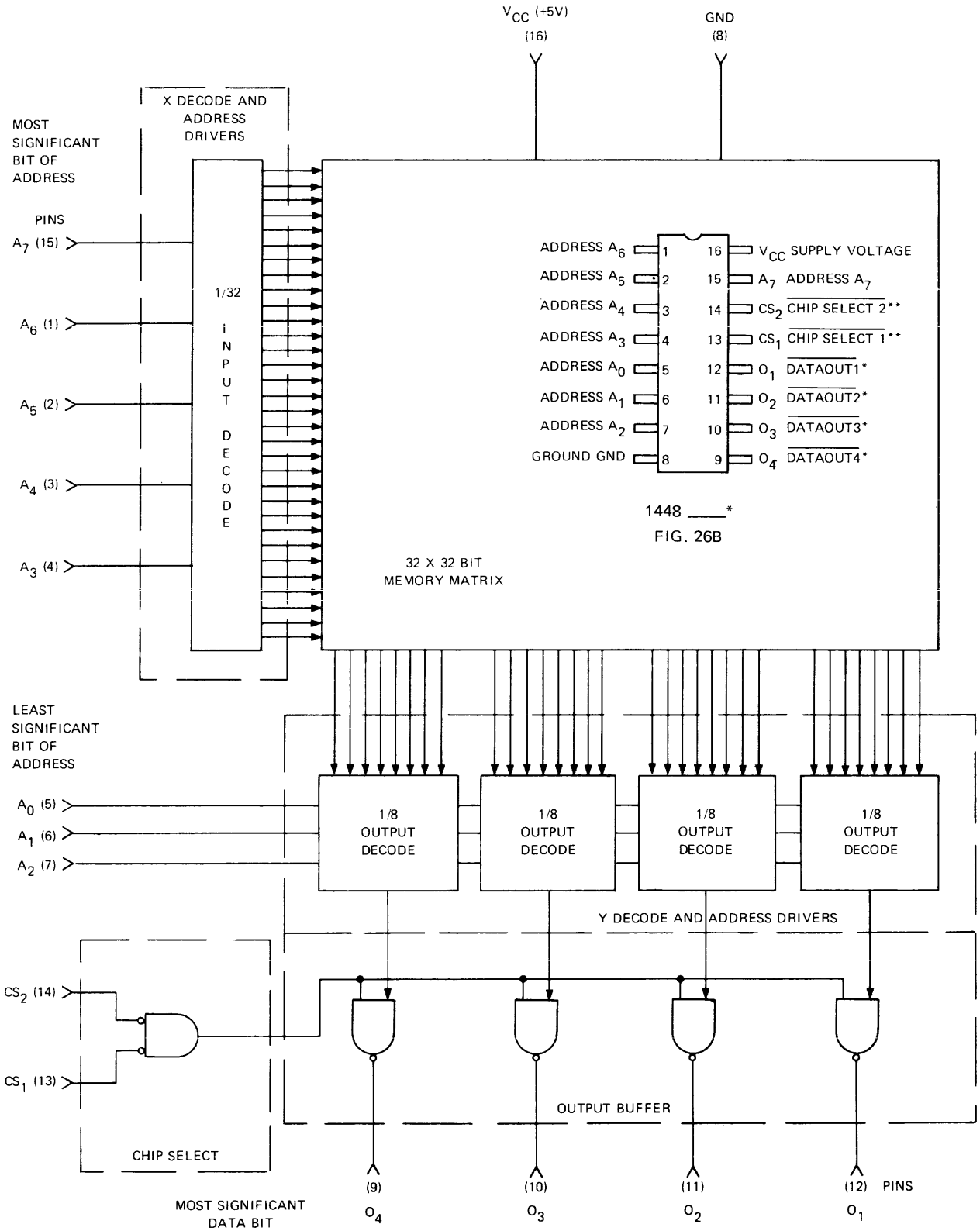


FIG. 26A

*PART NUMBER DEPENDS ON THE NANO CODE CONTAINED IN THE CHIP.

Circuit Detail

26. 256x4 READ ONLY MEMORY (ROM) (cont'd)

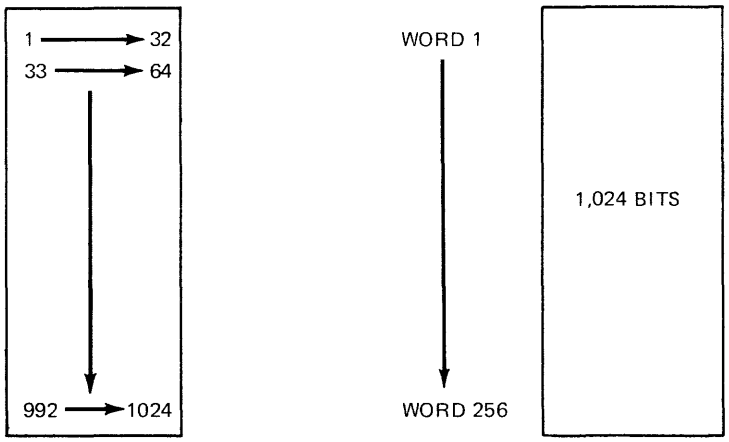


FIG. 26C

The high speed 256 x 4 ROM module (Fig. 26A) is organized in a 32 x 32 bit array. Each module contains 1,024 bits. Refer to Fig. 26C.

In the example above, 256-four bit words are represented. If it was necessary to have 256-eight bit words, then one additional module would be required, etc.

On chip address decoding A0 through A7 (Fig. 26A) is divided into two groups: the least significant bits and the most significant bits of the address. The five most significant bits address one set of 32 bits and the three least significant address one bit from each group of eight. The output buffer is enabled by Chip Select (CS_n) being at a low level and the result is four bits at the output (01, 02, 03, and 04).

27. 16x4 RANDOM ACCESS MEMORY (RAM)

The high speed 16 x 4 RAM module (Fig. 27A) is organized in a 16 x 4 bit configuration. Each module contains 64 bits. Refer to Fig. 27D.

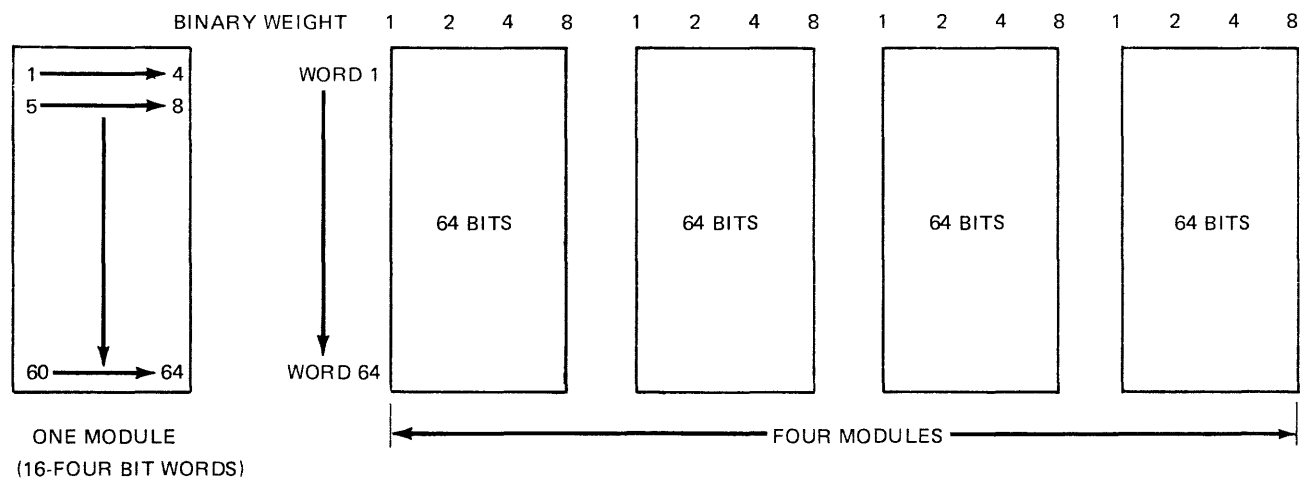


FIG. 27D

27. 16x4 RANDOM ACCESS MEMORY (RAM) (cont'd)

In the example in Fig. 27D, four-64 bit modules are represented. If another four bits are needed, then another module would be required, etc.

On chip address decoding, A0 through A5 (Fig. 27A) is divided into two groups; the least significant bits and the most significant bits of the address. The two most significant bits address one of the four modules. The four least significant bits address one set of four bits within the module.

If the Write Enable (WE) input is at a low level at this time, four data input bits (DI1, DI2, DI3, and DI4) are written into the module. If the Write Enable (WE) input is at a high level, four data bits are read out of the module at DO1, DO2, DO3, and DO4.

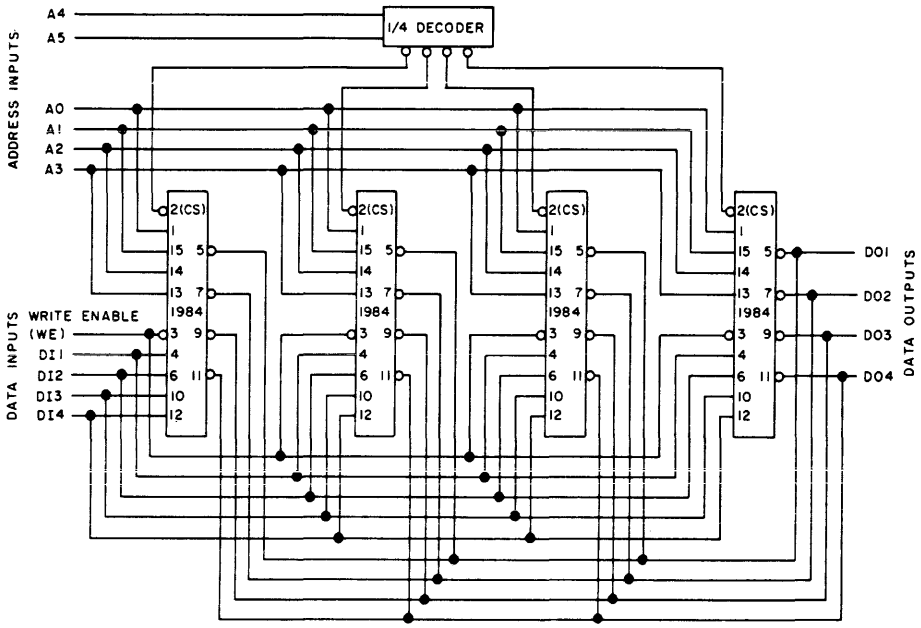
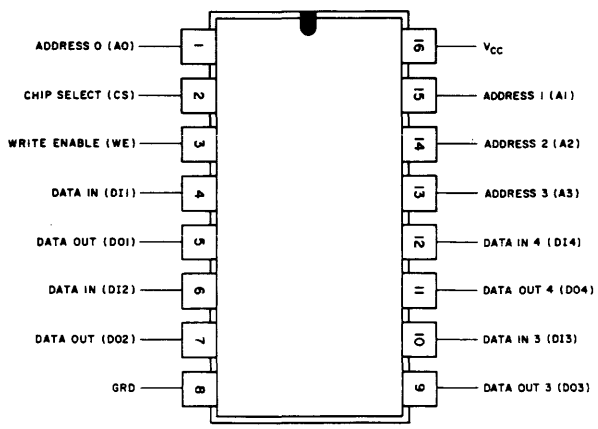


FIG. 27A



1447 3672

FIG. 27B

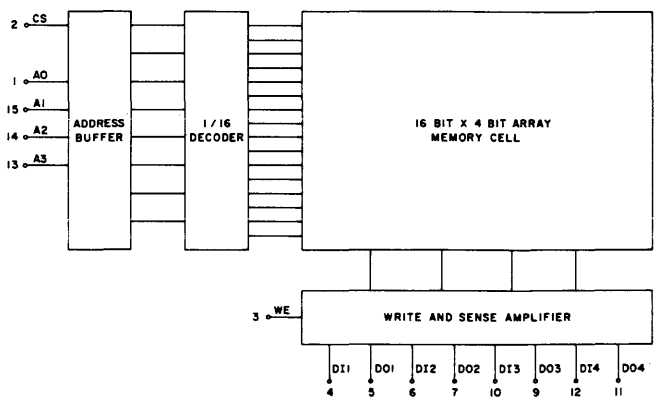


FIG. 27C

Circuit Detail

28. 64-WORD x 4-BIT FIRST-IN-FIRST-OUT SERIAL MEMORY (FIFO)

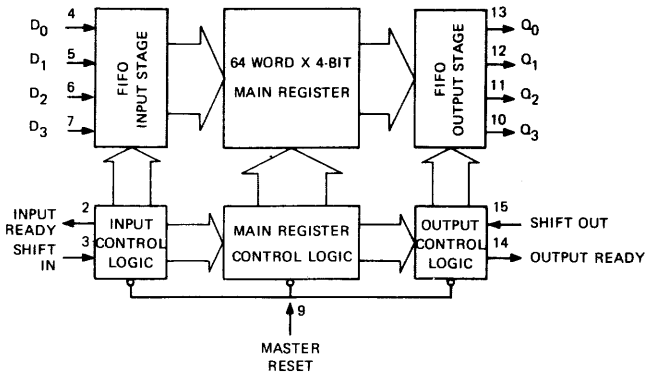
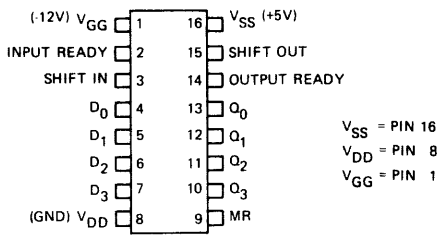


FIG. 28A



1448 9156
FIG. 28B

The four bits of data on the D_0 through D_3 inputs (Fig. 28A) are entered into the first bit location when both Input Ready (IR) and Shift In (SI) are high. This causes IR to go low, but data will stay locked in the first bit locations until both IR and SI are brought low. Then it will propagate to the second bit locations, provided the location is empty. When data is transferred, IR will go high indicating that the device is ready to accept new data. If the memory is full, IR will stay low. Once data is entered into the second cell, the transfer of any full cell to the adjacent empty cell is automatic. Thus data will stack up at the end of the device while empty locations will "bubble" to the front.

When data has been transferred into the last cell, Output Ready (OR) goes high, indicating the presence of valid data at the output Q_0 through Q_3. The shifting out of data is initiated when both the OR and the Shift Out (SO) signals are high. This causes OR to go low; Output data is maintained until both OR and SO are low. Then the content of the adjacent cell (provided it is full) will be transferred into the last cell, causing OR to go high again. If the memory has been emptied, OR will stay low.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full, or completely empty, respectively. In either case the signal would stay low.

29. TIMER

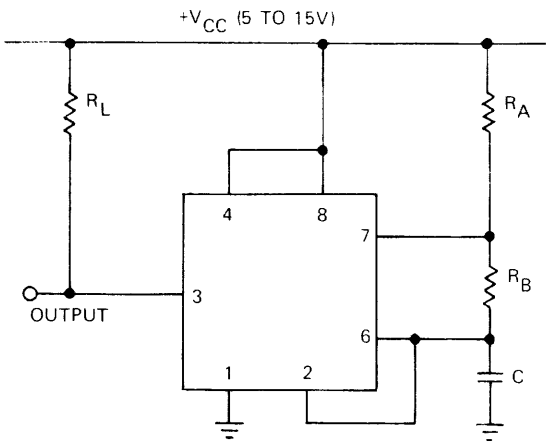


FIG. 29A

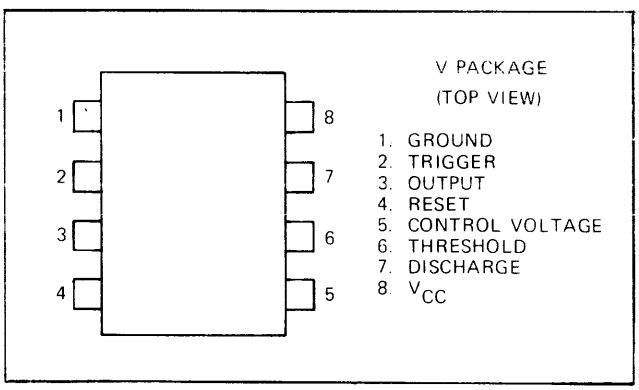


FIG. 29B

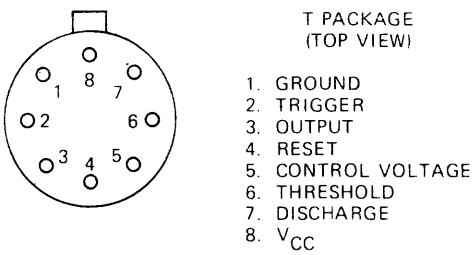


FIG. 29C

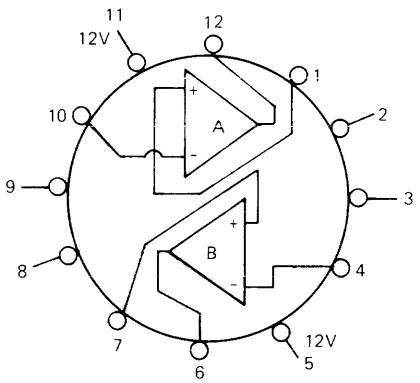
With the circuit connected as shown in Fig. 29A, the Timer will trigger itself and run free as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. The duty cycle may be set by the ratio of these two resistors. The capacitor charges between 1/3 Vcc and 2/3 Vcc. Therefore, the frequency is independent of the supply voltage. This configuration provides very stable operation.

Circuit Detail

30. HIGH SPEED DIFFERENTIAL COMPARATOR

Each circuit has a non-inverting input and an inverting input (Fig. 30A). For circuit A, the non-inverting input is pin 1, and for circuit B, pin 7. The inverting input in circuit A is pin 10 and for circuit B, pin 4.

When the non-inverting input is more positive than the inverting input, the output will be high. When the non-inverting input is less positive than the inverting input, the output will be low.



1447 4406
FIG. 30B

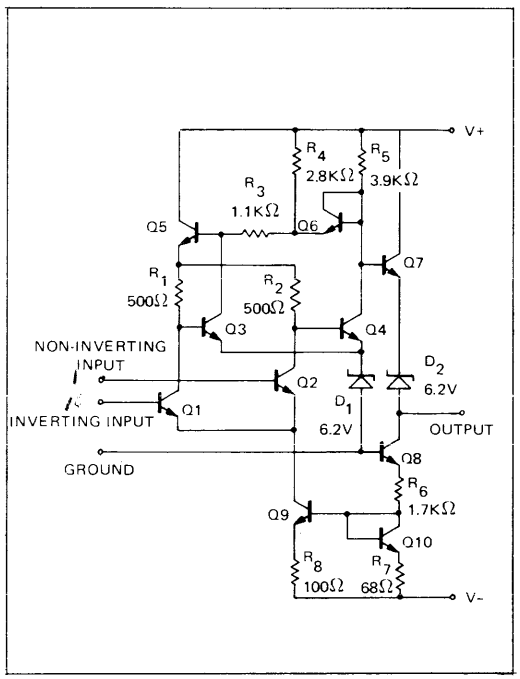


FIG. 30A

CIRCUIT LIST

INTRODUCTION

Before referring to the system schematics for signal tracing, the Circuit List is consulted. This is an alphabetical listing of all the signals used in the machine. The voltage buses are listed at the end. Associated with each signal is the backplane pin where it originates, points of distribution, and pivot points. The Processor, Memory, and I/O controls each have their own Circuit List. One page from a Circuit List is shown in Fig. III-1.

CIRCUIT LIST

Notations:

a. LF – logic frame
b. + – signal point of origin
c. numbers after pin locations are wiring level* numbers
d. The pivot or shield pins are the points that the wire is routed around
e. The Circuit Index is the first signal that appears on the page.

EXAMPLE: MUOSO8

a. MUOSO8 originates at pin FS1T level 1 and 2 (distinguished by +).

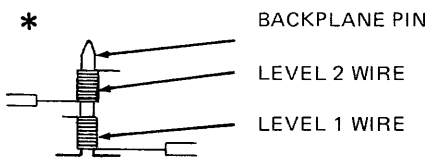
b.

Pin	Connects to pin	Pivot Points	
DI5L 2	DROU 2	DI6S	DQ9T
DR0U 1	DR3U 1	DR1T	DR2T
DR3U 2	+FS1T 2	FR4B	FS0C
+FS1T 1	FW0C 1	FU6S	FU7D

CARD AND PIN LOCATIONS

The logic rack is a junction point for all the printed circuit cards in the Processor. It also provide P-J connections for power, memory, I/O controls and the MTR meter. Fig. III-2 illustrates the logic rack from the frontplane side. This is the side where the cards are inserted and removed. The opposite side is called the backplane. The logic rack is divided into planes. The "A" plane is everything below the logic rack. The "B" plan is the P-J connectors. The "C" and "E" planes contain ground and voltage buses on the backplane side. The cards are located on planes "D" and "F".

Across the "E" plane on the frontplane side is the card location label. The label is divided into sets of ten (0 through 9) and each set has a different letter. Across the "A" plane is the P-J location label.



Circuit Detail

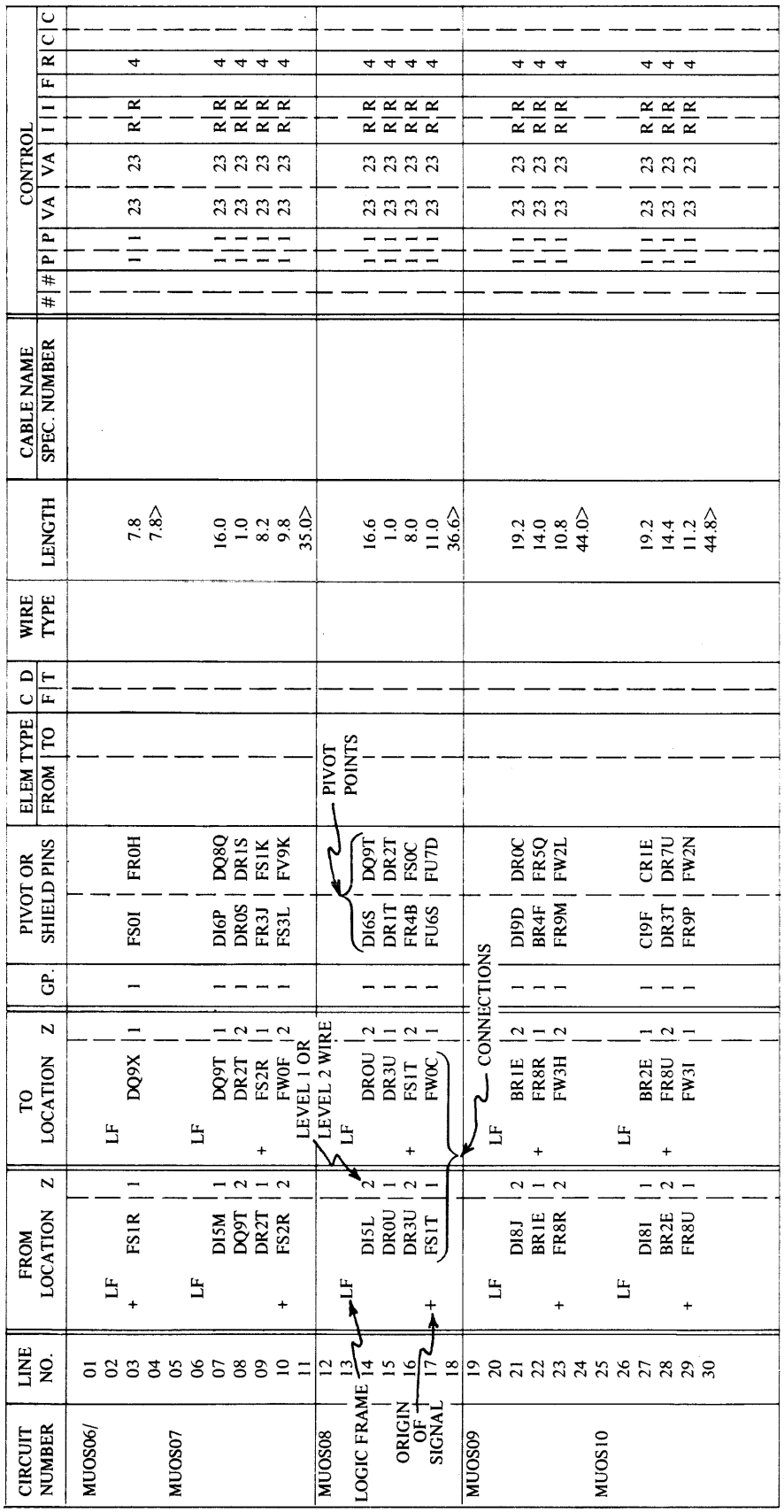


Fig. III-1 CIRCUIT LIST

Circuit Detail

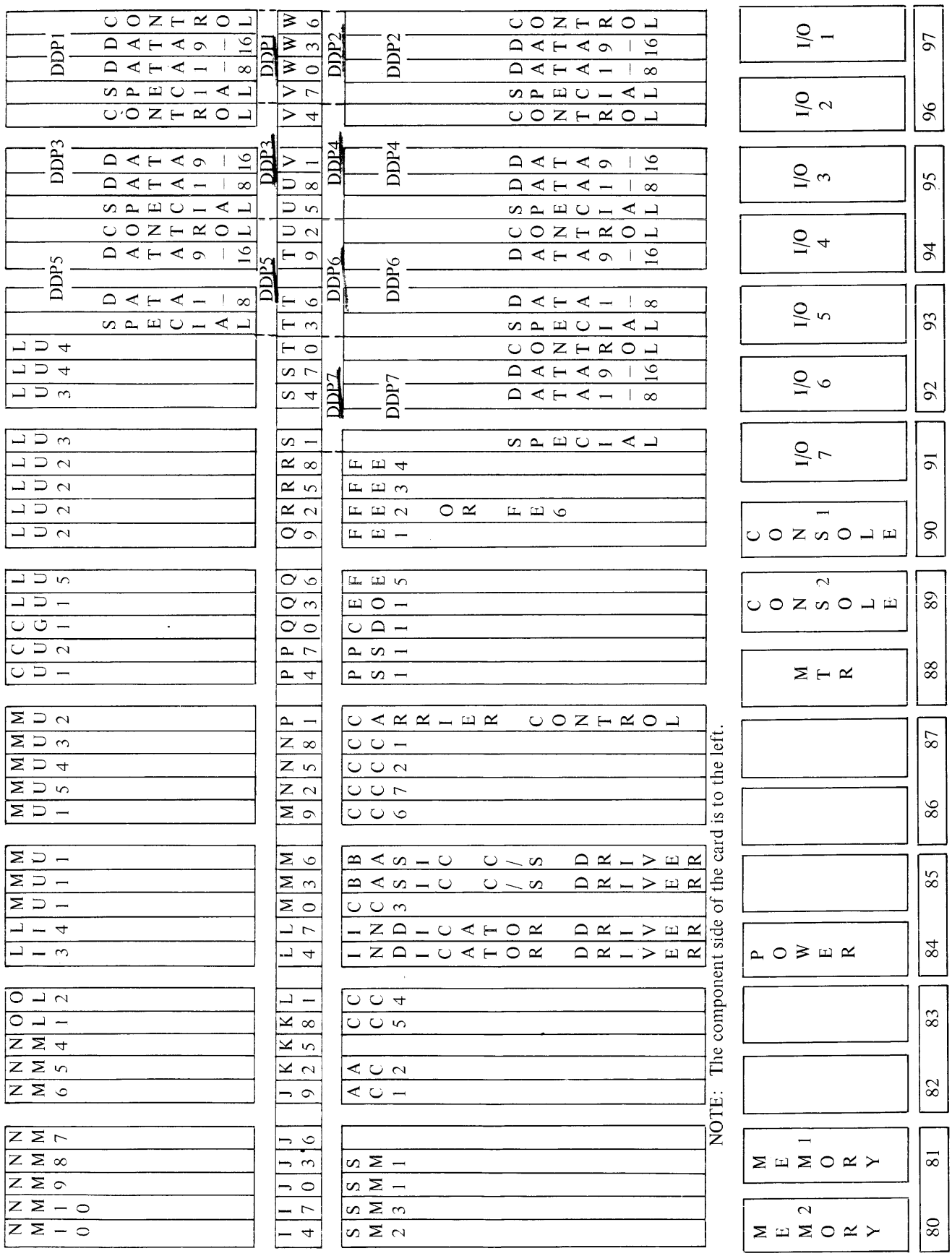
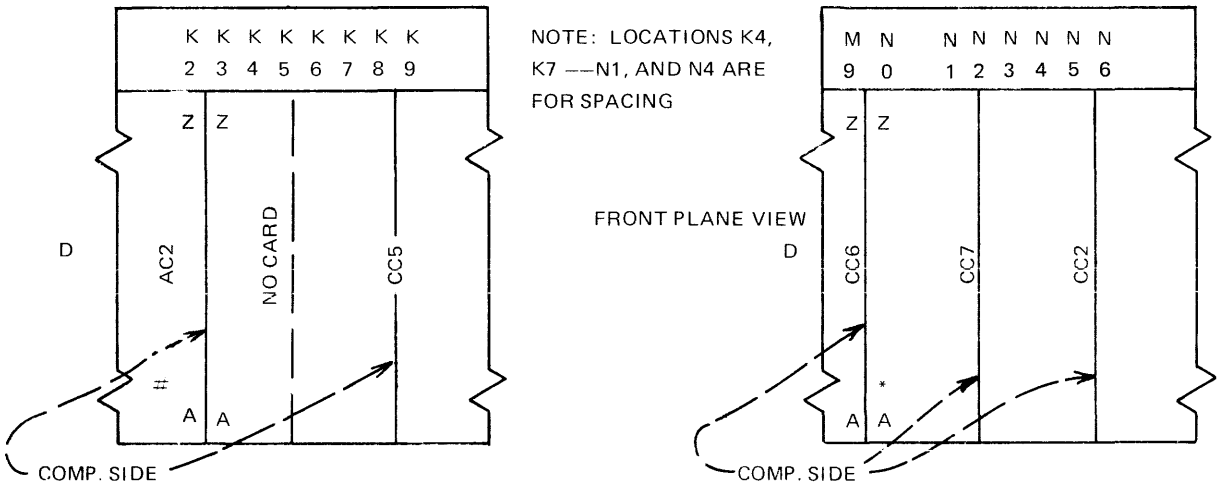


Fig. III-2 LOGIC RACK (FRONT PLANE VIEW)

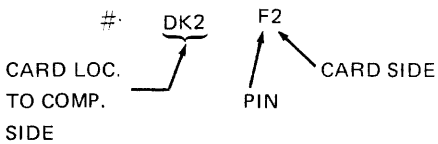
Card locations are always referenced to the component side. For example, Q9 is the card location to the component side of the FE1 and LU2 cards. To distinguish the plane, the card location is preceded by a "D" or "F". At location DM0, the CC3 card is found. In this way, there can only be one card in each location.

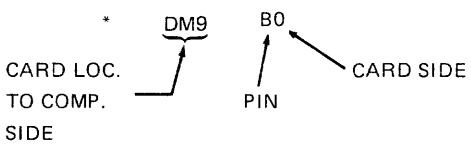
On cards containing chips only, there are four sets of connectors. Two are on the backplane side of the card and two are on the frontplane side of the card. The cards with discrete components only, have two sets of connectors. These are on the backplane side. Each set is lettered A through Z, with the exception of "O".

Since there are pins (connectors) on both sides of the card (component and non-component), the non-component side also has a location. For the AC2 card, the non--component side is DK3. The non-component side of the CC6 card is DN0. Refer to the diagrams below.

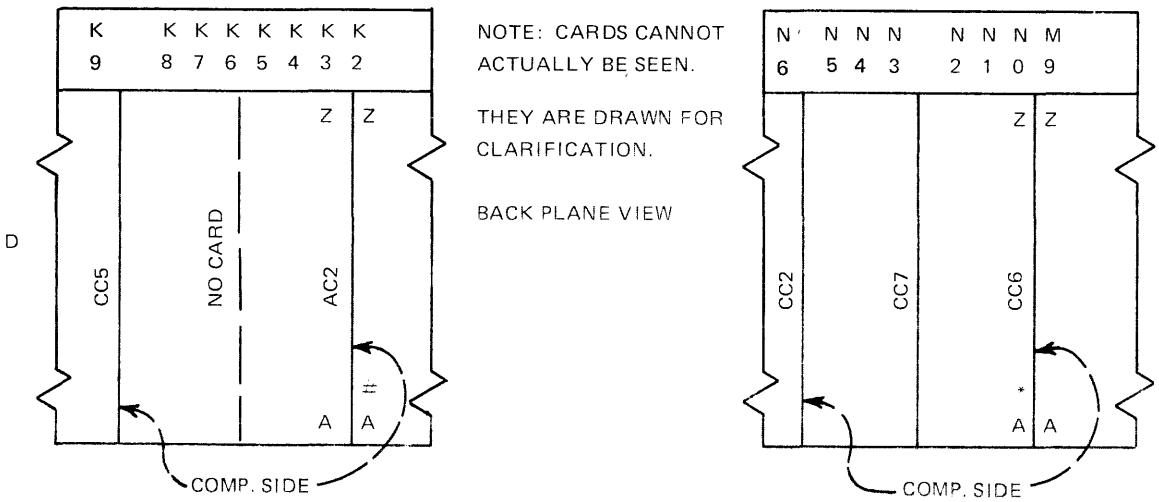


Frontplane pins are identified by locating the side of the card, and then the pin. Refer to the examples below.

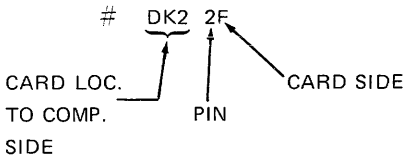


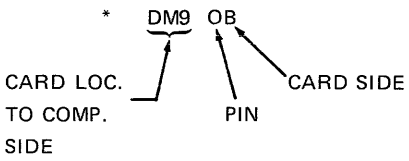


Backplane pins are located in a similar manner to the frontplane pins. Refer to the examples below.



Circuit Detail





A backplane pin is differentiated from a frontplane pin by reversing the order of the pin-side portion of the location. In other words, a frontplane pin location has the card location and then a letter/number combination. The backplane pin location has the card location and then a number/letter combination.

Pins on the P-J connectors are located the same way as any backplane pin, except the plane is identified as "B".

CARD TO SCHEMATIC LIST

The schematics are arranged in groups, or sheets. Each group has a letter identifier (Fig. III-3). Each card has its own section within the sheet. This is specified by the first two digits of the schematic location. If more than one page is required within the section, it will be indicated by additional numbers. Refer to the example below.

EXAMPLE: MU2 (card name)

a. From Fig. III-3 the location is: Sheet A.021 and .022

b. Sheet A (sheet) .02 (section) 1 and 2 (pages)

Tracing signals from card to card is done the same way as locating the card schematic. The signal name will have its source or destination listed by sheet, section, and page.

CARD TO SCHEMATIC LIST

CARD NAME	SCHEMATICS
MU1 – 1, 2, 3 & 4	Sheet A.011 thru .018
MU2	.021 & .022
MU3	.031
MU4	.041
MU5	.051
LU1	Sheet B.011
LU2 – 1, 2, 3 & 4	.021 thru .024
LU3	.031 & .032
LU4	.041
LU5	.051
CU1	Sheet C.011
CU2	.021 & .022
CG1	Sheet D.011
CD1	Sheet E.011
NM1	Sheet F.011 thru .018
NM2	.021 & .022
NM3	.031
OL	Sheet G.011
LI1	Sheet H.011
LI2	.021
SM1 – 1 & 2	Sheet I.011 & .012
SM2	.021 & .022
SM3	.031
PS1	Sheet J.011 thru .014
EO1	.021 & .022
CC0	Sheet K.011 thru .013
CC1	.021
CC2	.031
CC3	.041
CC4	.051
CC5	.061
CC6	.071
CC7	.081
CC8	.091 thru .094
CC9	.101 thru .104

Fig. III-3 CARD TO SCHMATIC LIST

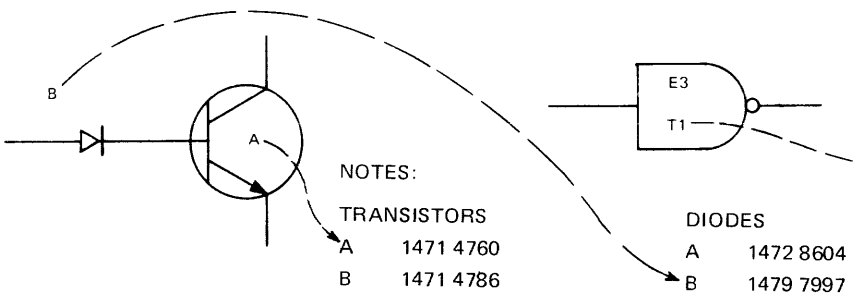
CARD TO SCHEMATIC LIST

CARD NAME	SCHEMATICS	CARD NAME	SCHEMATICS
DC1	Sheet L.011	PC1	Sheet P.011
DC2	.021	PC2	.021
DC3	.031	PC3	.031
DC4	.041	PC4	.041
CR1	Sheet M.011	FE1	Sheet Q.011
CR2	.021 & .022	FE2	.021
CR3	.031 & .032	FE3	.031
CR4	.041 & .042	FE4	.041
RC1	Sheet N.011		
RC2	.021		
RC3	.031		
RC4	.041		

Fig. III-3 (Cont'd)

COMPONENT IDENTIFICATION

For transistors, diodes, and Integrated Circuits (I.C.'s), on the schematics there will be letters or letter-number combinations inside the symbol. This letter corresponds to a part number under Notes on the first reference page. The part numbers may be listed in several columns under Notes. Refer to the example below.



CODE	PART NO.	QTY.
	1447 5396	1
SU	1447 3755	2
B4	1447 3599	1
T8	1447 3573	2
T4H	1479 0265	5
T3H	1486 8780	1
T2H	1479 0240	2
T1H	1479 7971	1
T1	1447 3532	2
DL	1447 3623	3

PIN AND COMPONENT LOCATIONS ON PRINTED CIRCUIT CARDS

Three types of cards are used in this system. The first card described will contain integrated circuit components only. The second type will have discrete components only, while the third will be made up of both discrete and integrated circuit components. To readily locate any component and its connections to the card, a sequence of alpha and numeric designations is used. The letters and numbers are printed near the edge of the card. The source of the component location is the schematic.

PIN AND COMPONENT LOCATIONS ON INTEGRATED CIRCUIT CARDS

Fig. III-4 shows the typical layout of an integrated circuit card, labeling the coordinates used for locating a component, its individual connection points, and the backplane and frontplane connector pads on the card itself.

Normally, front plane pins are used for testing purposes. That is, these are signals that do not leave the card. The B700, in some cases, uses the frontplanes of two cards by connecting them together. All references to Fig. III-4 are made when the card is viewed with the 1A marking in the upper right hand corner and the A3 marking in the upper left hand corner. The 1A through 1Z designations from top to bottom represent the backplane connectors A through Z, with letter "O" excluded. The frontplane connectors A3 through Z3 are shown on the left side and again the letter "O" is not used. The reverse side of the card (not shown) is marked 2A through 2Z for the backplane, and A4 through Z4 for the frontplane connections. The above description is with the card out of the logic rack. With the card in the logic rack, only the letter is significant. For example, pin 1F on the card when it is out of the logic rack may be identified as DK2 2F with the card in the rack. It all depends on the card location. The frontplane pin B4 may be identified as DM9 B0. Refer to the diagrams included in the Card and Pin Locations discussion of this section. Notice that even with the card out of the rack, the frontplane pins are defined as a letter/number and the backplane pins by a number/letter.

The schematics identify the card pins (backplane) using the method with the card out of the rack. Only backplane pins are specified, for these are the inputs and outputs of the card. The exception to this is when front plane connectors are used.

The card is divided into six rows (A-F) from top to bottom to denote the vertical location of the component connection point. Numerals 1, 3, 5, and 7 across both top and bottom edges from left to right are used to specify the horizontal location.

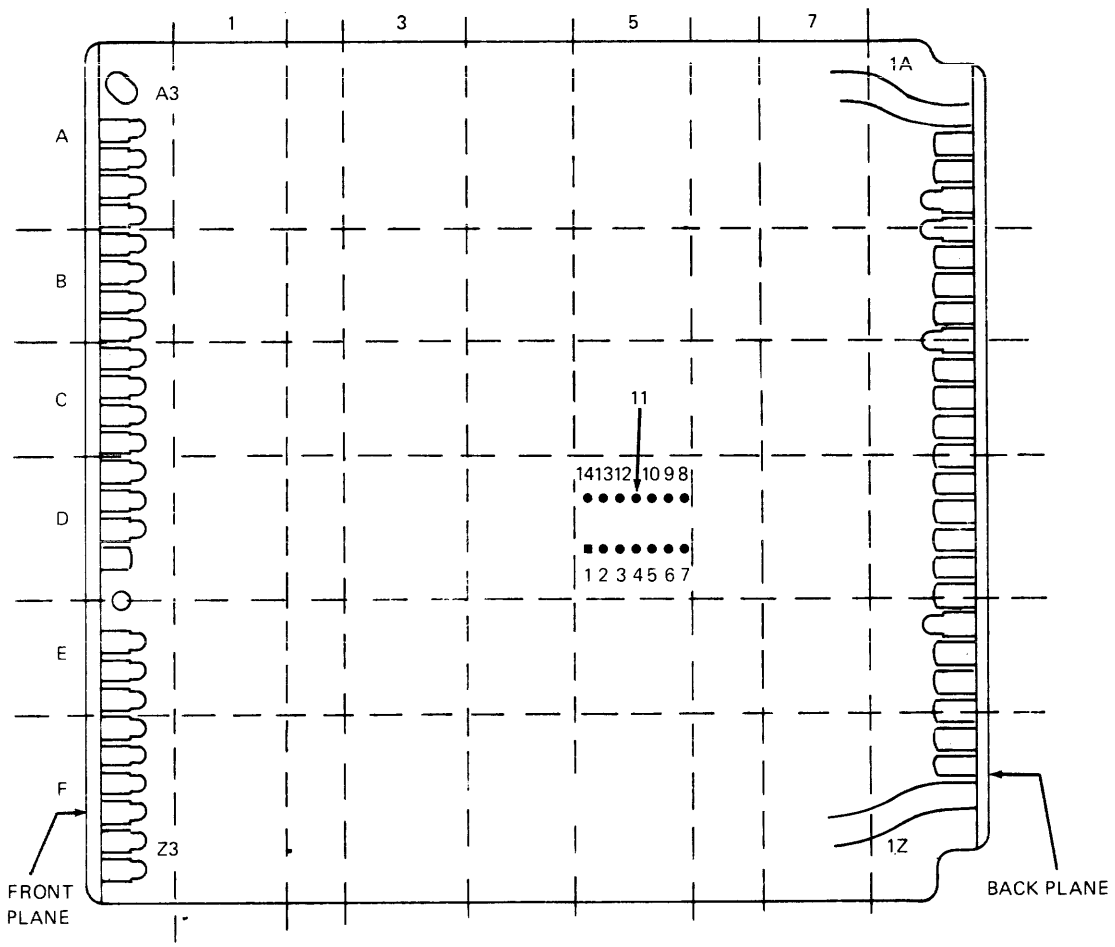


Fig. III-4

These coordinates are used to define specific areas on the card. The vertical location is always specified first, such as F2, C5, D3, etc. This location is included in the schematic symbol.

Each of these areas is further broken down by lettering a specific point for the individual connections of a component. All the chip locations are labeled 1 through 14 (A→N). In Fig. III-4 only one set of connections is shown. For example, chip location D5, pin 11 is pointed out. Pin 1 is identified by a square pad connection.

COMPONENT LOCATIONS ON DISCRETE COMPONENT CARDS

The layout of a printed circuit card containing discrete components only, is shown in Fig. III-5. All references are made to the component side of the card. At the right edge, 1A through 1Z represent the backplane connection pads A through Z, with the letter "O" omitted. The same edge of the card, but on the reverse side, is marked 2A through 2Z, which again denotes pads for backplane connections. There are no frontplane connections or pads on this type of card.

The card is divided into vertical areas, designated A through F, starting from the top. Each area is further divided into ten locations. A0, A1, A2, etc., through A9, B0 through B9, etc.

Horizontal locations are specified by seven areas A through G from left to right starting with A the the left or frontplane edge. Again, each area except G contains ten individual locations B0 through B9, C0 through C9, etc. Area G has only three locations G0, G1, and G2.

Each of the component connections to the card is specified by both a vertical and a horizontal coordinate on the schematics with the vertical coordinate always given first.

EXAMPLE 1: The diode illustrated in Fig. III-5 is located at E2B2, E2B8.

EXAMPLE 2: Resistor location shown is F0D0, F6D0.

EXAMPLE 3: Transistor location shown has three sets of coordinates. The schematic specifies one for each leg. Emitter connection is shown at E5E4, collector at E8E7, and base at E8E4.

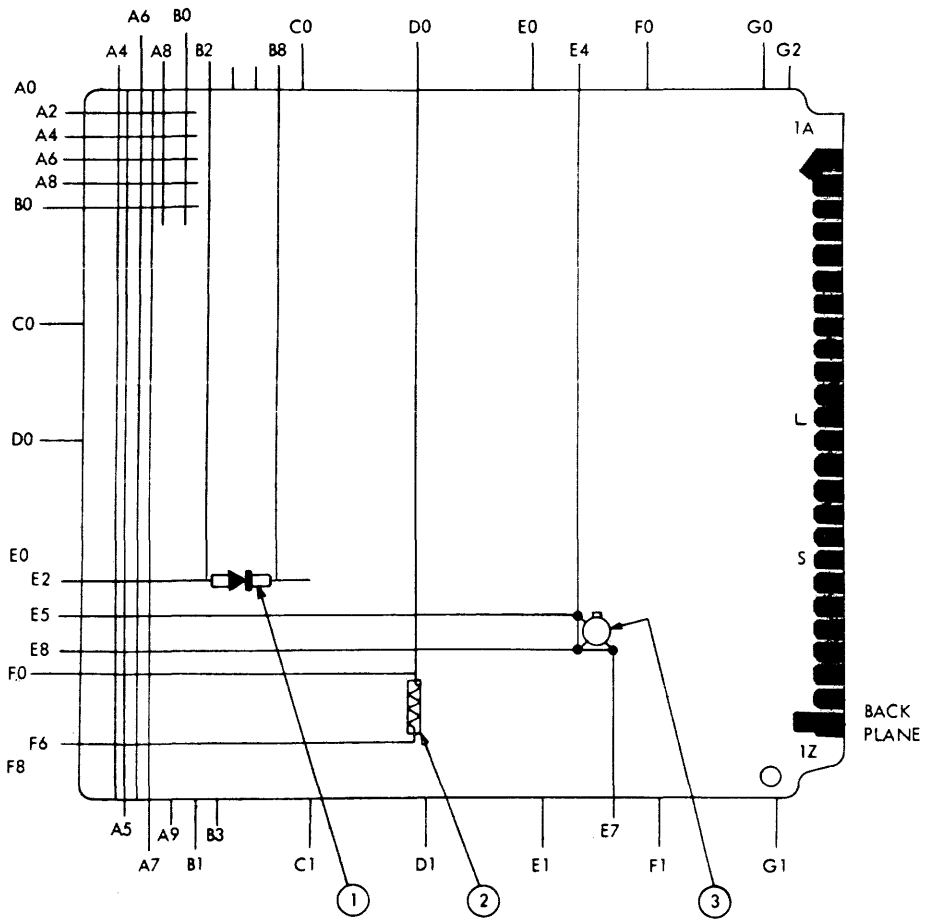


Fig. III-5

COMPONENT LOCATIONS ON I.C. AND DISCRETE COMPONENT CARDS

Fig. III-6 shows the layout of a card containing both discrete components and integrated circuits. Facing the component side of the card with the 1A marking at the upper right hand corner and A3 marking at the upper left hand corner, the backplane connection pads 1A through 1Z, with letter "O" omitted, are shown at the right side. The pads A3 through Z3 at the left side are frontplane terminals. The pads on the reverse side of the card will be 2A through 2Z for the backplane and A4 through Z4 for the frontplane.

From left to right the card is divided into seven horizontal areas, A through G. Each area, except G, is further divided into ten locations, A0 through A9, B0 through B9, etc. From top to bottom, six vertical areas, A through F, are used. Each area is subdivided into ten locations, A0 through A9, B0 through B9, etc. The intersections of the vertical and horizontal area locator lines identify the component location and its connection points, with the vertical locating coordinate always given first.

EXAMPLE: The chip shown is located at D3D8

On this type of card an integrated circuit chip is located by specifying only the A connector point of the chip. A notch or dot on the chip identifies the end of the chip containing the "A" terminal.

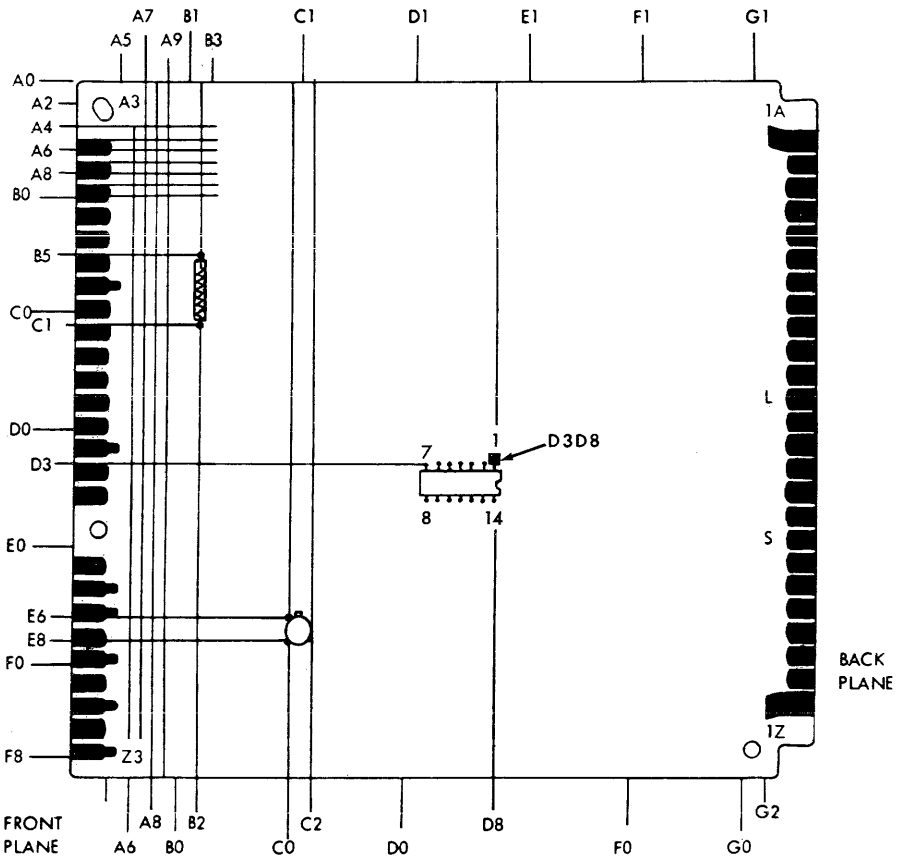


Fig. III-6

B700
PROCESSOR

SECTION
IV

Burroughs

ADJUSTMENTS

FIELD ENGINEERING

TECHNICAL MANUAL

Printed in U. S. America 9-16-74

For Form 1064482

5 VOLTS TAP ADJUSTMENT FOR THE B711 PROCESSOR

This procedure covers the tap adjustment for the 5 volts power supply, when installing the B711 processor unit, to ensure that the voltage at the backplane is within the specified limits.

PREREQUISITES

The following parameters are required to be within their specified limits during this procedure:

A. Main Voltage – 107 to 127 volts RMS
International Service: +5 to -10 percent of the specified nominal service.
This voltage can be checked at CB1-2 (Line) and TB3-A5 (Neutral).

B. Main Frequency: ±1 percent of the specified value.

C. Ambient Room Temperature: 50° to 104° F.

The tap adjustment involves the two leads marked "+" and "-" which are connected to the constant voltage transformer of the processor 5 volts power supply. The tap adjustment compensates for manufacturing variations in the power supply component parts and for the power distribution wires to the backplane, backplane loading, and drift due to temperature changes. Once the tap adjustment is made, no further adjustment need be made unless the medial backplane voltage limits are not met or there is a load change, a component change or a defective component. The latter should be corrected.

PROCEDURES FOR 5 VOLT ADJUSTMENT

STEP 1. All printed circuit (PC) cards shall be installed in the processor unit. It is to be noted that the card complement of a processor will vary depending on the number of peripheral devices and the size of memory.

STEP 2. Apply main power and measure the +5 volt memory backplane voltage at BG9A. Put ground lead on BH0E.

NOTE: A voltmeter capable of measuring voltages within the range of 3.5 to 6.0 volts DC at 1% accuracy is required.

STEP 3. Turn power off. From Table IV-1, determine the number of tap steps necessary using the voltage reading taken in Step 2.

A. A single boost (+) step consists of either:
   a. Moving the negative (-) lead to the next lower terminal number if the positive (+) lead is on terminal 1 and the negative (-) lead is on a terminal other than terminal 1.
   b. Moving the positive (+) lead to the next higher terminal number if the negative (-) lead is on terminal 1.
   NOTE: Positive (+) lead may also be on terminal 1.

B. A single buck (-) step consists of either:
   a. Moving the positive (+) lead to the next lower terminal number if the negative (-) lead is on terminal 1 and the positive (+) lead is on a terminal other than terminal 1.

MEMORY BACKPLANE VOLTAGE (VDC)			NO. OF TAP STEPS REQUIRED	
COLD SYSTEM (See Note 1)	WARM SYSTEM (See Note 2)	HOT SYSTEM (See Note 3)	BUCK (-)	BOOST (+)
4.08 – 4.24	4.03 – 4.19	3.98 – 4.14		+5
4.25 – 4.42	4.20 – 4.37	4.15 – 4.32		+4
4.43 – 4.59	4.38 – 4.54	4.33 – 4.49		+3
4.60 – 4.77	4.55 – 4.72	4.50 – 4.67		+2
4.78 – 4.94	4.73 – 4.89	4.68 – 4.84		+1
4.95 – 5.15	4.90 – 5.10	4.85 – 5.05		NONE
5.16 – 5.32	5.11 – 5.27	5.06 – 5.22		-1
5.33 – 5.50	5.28 – 5.45	5.23 – 5.40		-2
5.51 – 5.67	5.45 – 5.62	5.41 – 5.57		-3
5.68 – 5.85	5.63 – 5.80	5.58 – 5.75		-4
5.86 – 6.02	5.81 – 5.97	5.76 – 5.92		-5

NOTES: (1) A cold system is one which has been on for 03 minutes or less and was off for several hours preceding the turn on.
(2) A warm system is one which has been on for less than two hours and more than 30 minutes.
(3) A hot system is one which has been on for two hours or more, or was off for 15 minutes or less after having been on for several hours.

TABLE IV-1

b. Moving the negative (-) lead to the next higher terminal number if the positive (+) lead is on terminal 1.
NOTE: Negative (-) lead may also be on terminal 1.

STEP 4. After tap adjustment in Step 3, apply power and measure the 5 volt backplane voltages. Measure the memory backplane voltage at BG9A, ground lead being on BH0E. Also measure two logic backplane voltages at backplane locations FR3-A, GND FR2-A and DP2-Z, GND DP1-Z. The average of the three backplane readings shall be 4.90 to 5.25 volts for a hot system, 4.85 to 5.20 volts for a warm system, and 4.80 to 5.15 volts for a cold system.

READJUSTMENT

If the average backplane voltage is outside the limits or if the number of PC cards increased or decreased by more than eight single or four double (memory) cards, a readjustment of the tap is necessary.

B711 MEMORY ADJUSTMENTS

A. Voltage Adjustments

The voltage adjustment shall be performed at an ambient room temperature of 75° ± 5° F. A digital voltmeter must be used.

Procedure

STEP 1. X-Y Voltages

The X-Y voltages shall be +16V and -16V, ± 0.1V.

1.1 +16 Volt Adjustment

a. At the core memory backplane, connect the positive lead of the DVM to Pin DG7A and the negative lead to ground.

b. If the voltage is not +16V ± 0.1V, adjust potentiometer R18C located on the memory control board. (See Figure IV-1.)

1.2 -16 Volt Adjustment

a. At the core memory backplane, connect the positive lead of the DVM to Pin DG8G and the negative lead to ground.

b. If the voltage is not -16V ± 0.1V, adjust potentiometer R19C located on the memory control board. (See Figure IV-1.)

STEP 2. VREF (Inhibit) Voltage

The VREF (Inhibit) voltage shall be +11.3V ± 0.1V.

a. At the core memory backplane, connect the positive lead of the DVM to Pin DG8B and the negative lead to ground.

b. If the voltage is not +11.3V ± 0.1V,

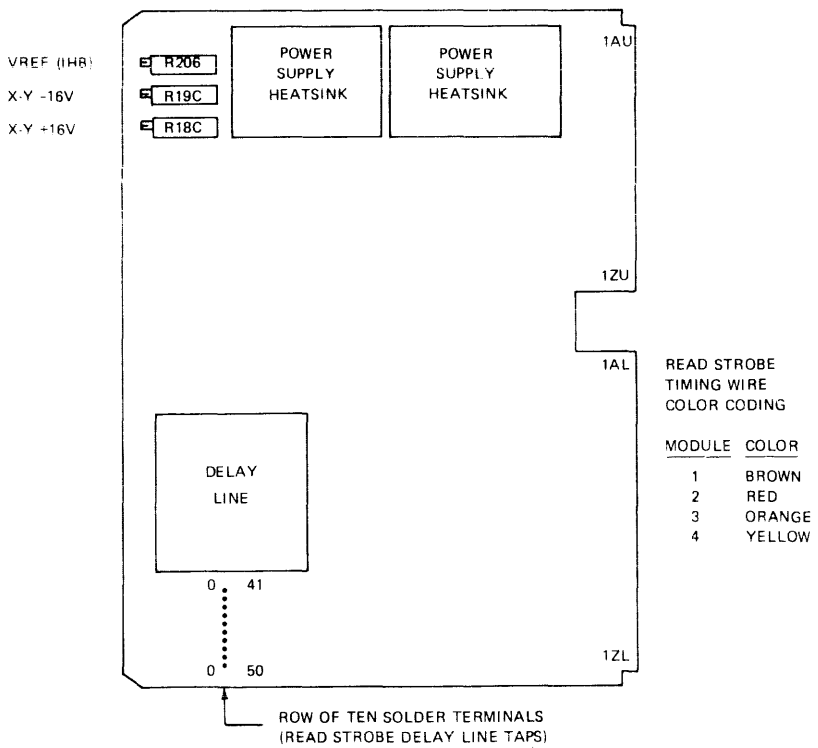


Fig. IV-1 CONTROL BOARD ADJUSTMENT POINTS

adjust potentiometer R20C located on the memory control board. (See Figure IV-1.)

STEP 3. Inhibit Voltage

The Inhibit voltage shall be +15.5V± 0.1V. Step 2 must be completed before this step.

a. At the core memory backplane, connect the positive lead of the DVM to Pin DF8D and the negative lead to ground.

b. If the voltage is not +15.5V ± 0.1V, adjust potentiometer R4N located on the Inhibit power supply circuit board. (See Figure IV-3.)

STEP 4. Sense Threshold Voltage

The sense threshold voltage shall be the value listed as "VREF" on the label attached to the core stack assembly and shall have a tolerance of ± 0.1V. This voltage must be checked on all the memory digit boards.

a. Step 1 must be completed before this step.

b. At the digit board, connect the positive lead of the DVM to the threshold voltage test point and the negative lead to ground. (See Figure IV-2.)

c. If the voltage is not within the tolerance stated, adjust potentiometer R66K of this digit board.

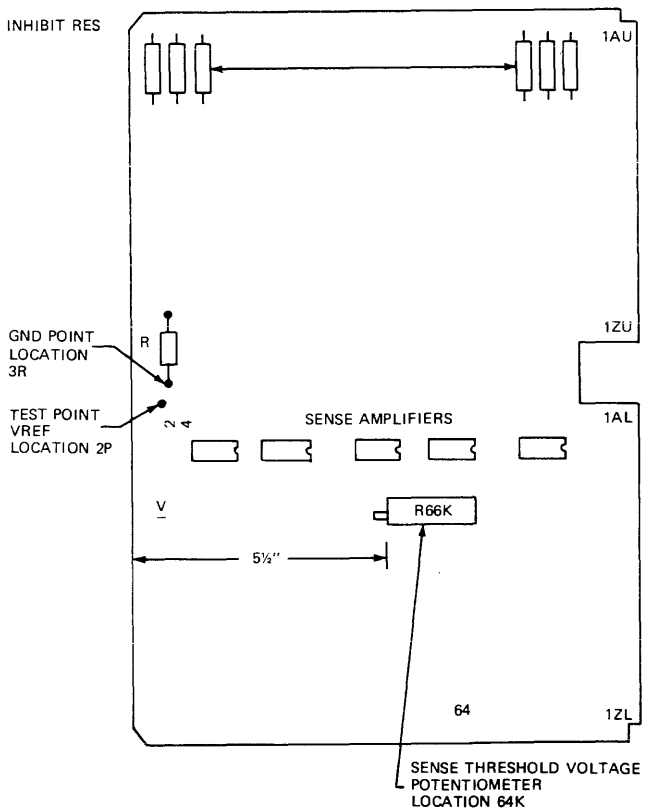


Fig. IV-2 DIGIT BOARDS TEST AND ADJUSTMENT POINTS

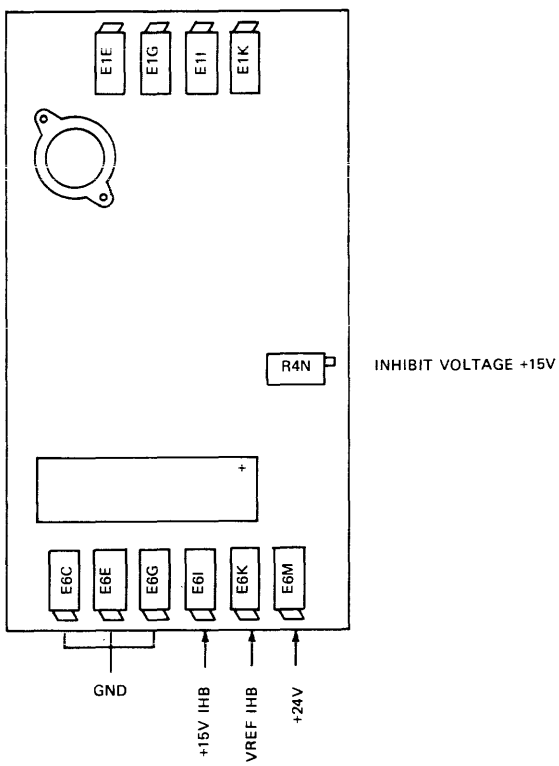


Fig. IV-3 INHIBIT POWER SUPPLY TEST AND ADJUSTMENT POINTS

READ STROBE TIMING SET-UP

This adjustment may be necessary when installing a memory module or when replacing a control board or stack board. Located on each stack board is a sticker as shown in Figure IV-4.

For this adjustment the read strobe timing and DL tap No. are used. When installing a memory module or a memory stack, the stack label will identify the DL tap number and the read strobe timing in nanoseconds for proper operation of the memory.

The DL tap number refers to one of ten possible delay line taps located on the control board (DL 41 to 50). Refer to Figure IV-1. This DL tap number is then the tap used to connect the read strobe timing wire. Each memory module has its own read strobe timing wire as shown on Figure IV-1. The read strobe timing refers to the delay between signal YD read timing - (x) and signal read strobe - (x), x being the module number. By moving the read strobe timing wire between taps 41 to 50, the delay is either increased or decreased, since signal YD read timing - (x) is generated for a fixed tap source, tap 18. For this adjustment, tap 18 in reference to time is "0" and tap 41 is 115 nsec (5 nsec delay per tap). Since the timing check is made from the backplane, an average of 15 nsec must be added to the read strobe timing taps (41 to 50) to correct circuit delay. Table IV-2 shows the delays that are encountered during this adjustment.

See Memory Installation Procedures in Memory FT & R Documents.

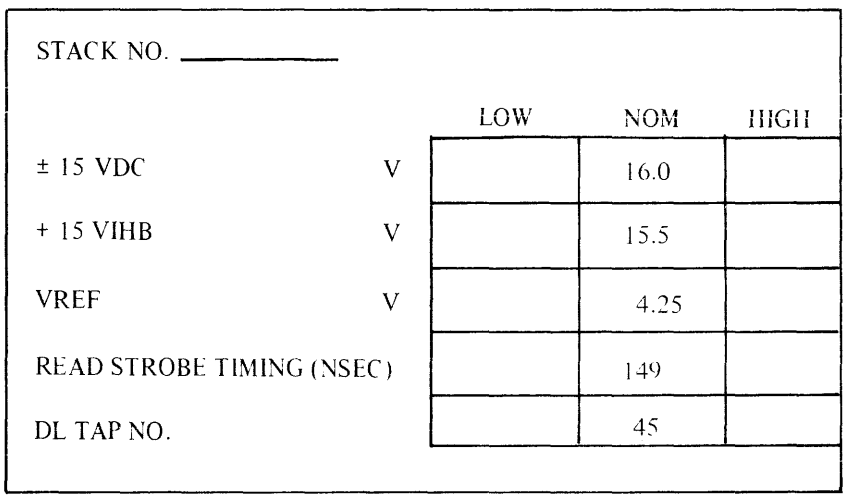


Fig. IV-4 STACK STICKER

	DL TAPS	ACTUAL DELAY FROM DL INPUT	DELAY FROM TAP 18	DELAY USED FOR ADJUSTMENTS
YD Read Timing -(x)	18	90 nsec	0 nsec	0 nsec
Read Strobe -(x)	41	205 nsec	115	130
	42	210	120	135
	43	215	125	140
	44	220	130	145
	45	225	135	150
	46	230	140	155
	47	235	145	160
	48	240	150	165
	49	245	155	170
	50	250	160	175

EXAMPLE: If for proper memory module operation, the delay between signal YD Read Timing -(x) and Signal Read Strobe -(x) should be 149 nsec, Tap No. 45 will be used to connect the Read Strobe Timing wire.

TABLE IV-2

B700

PROCESSOR

(INCLUDES B 705/711 AND B 771)

SECTION

V

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

MAINTENANCE
PROCEDURES

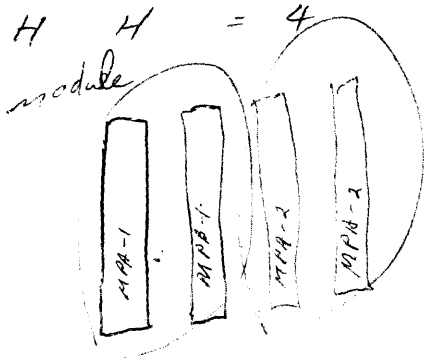
Printed in U. S. America 9-16-74

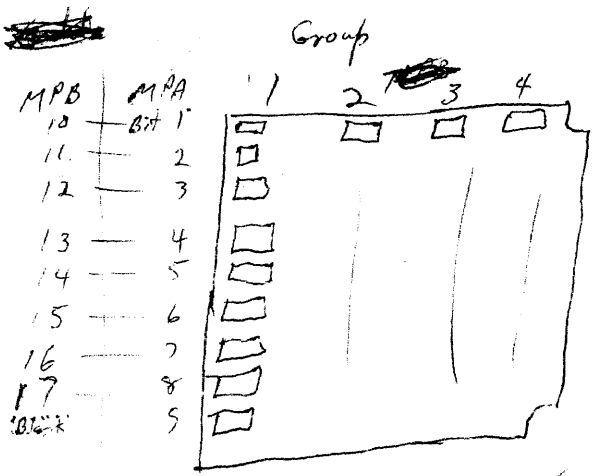
For Form 1064482

EO card
Sect II p 65

Group select

IN'CR 05	06	
L	L	= 1
L	H	= 2
H	L	= 3
H	H	= 4





for 2nd stack memory PAD 15 p to gnd.

FIELD ENGINEERING (FE) CARDS

The four FE cards are designed to aid the Field Engineer to detect and isolate problems arising in the micro program memory, nano program memory or portions of the memory control unit. The FE cards are also used in operating the MTR's.

FE CONTROLS AND INDICATORS

FE 1 and FE 2 Indicators

FE 1 and FE 2 contain 16 indicators in four groups of four. The indicators are symbolized as such: FE 2 A Indicators 1, 2, 3, 8 and B Indicators 1, 2, 4, 8. FE 1 C Indicators 1, 2, 4, 8 and D Indicators 1, 2, 4, 8. See Figure V-1. A indicators being the most significant digit and D indicators being the least significant digit.

The 16 indicators provide visual displays for monitoring MTR operation. The displays are:

1. Micro Program Memory (MPM) Bits 1-16
2. Memory Information Register (MIR) Bits 1-16
3. Micro Program Incrementer (INCR) Bits 1-14
4. FE Address Counter (AC) Bits 1-16

These displays are selected by switches SEL 0 and SEL 1 on FE 3.

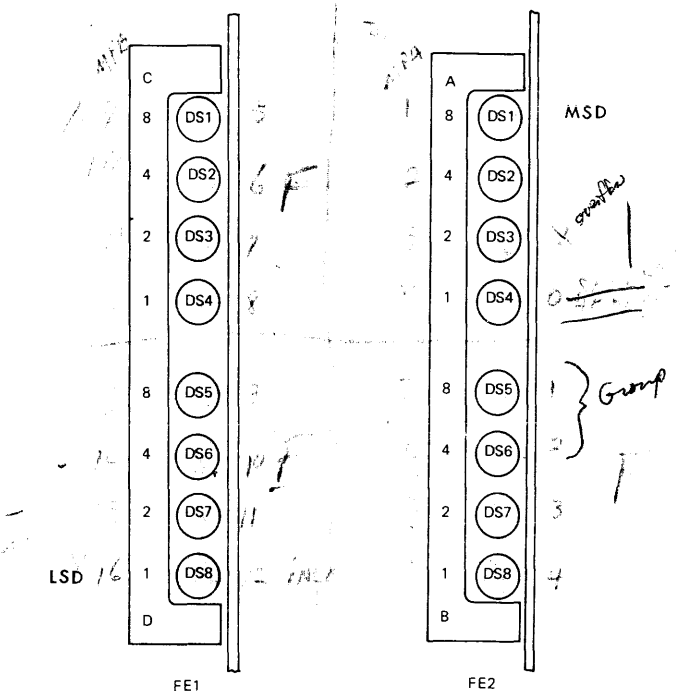


Fig. V-1 FE1 and FE 2 CARDS

FE3 Pushbuttons

FE3 (Figure V-2) contains four pushbuttons as follows:

1. FST – Force Step
   Produces a force step signal causing the MPCR to step one location. It is used when the wait indicator (FE 4) is lit while in the MTR mode.
2. SGL – Single Pulse
   When the NORM/SGL pulse toggle switch is in the SGL position, pressing SGL generates one system clock pulse.
3. PRO – Proceed
   This pushbutton performs two functions when in Test mode:
   a) Whenever the stop indicate is turned on, pressing PRO resets the stop FF (FE 4), allowing the test to continue.
   b) If the REP/NORM (FE 4) toggle switch is set to REP position, it causes the sequence counter to step one count, when the PRO pushbutton is pressed.
4. RER – Reset Error
   RER pushbutton causes the error FF to reset. If the MTR/MEM (FE 4) toggle switch is set to the MTR position, pressing RER pushbutton causes the address (clock) counter to reset.

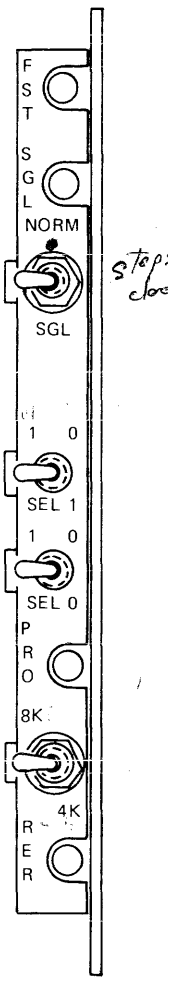


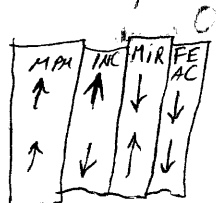
Fig. V-2 FE 3 CARD

FE 3 Toggle Switches

The FE 3 toggle switches are as follows:

1. NORM/SGL – Normal-Single Pulse
   This switch allows single clock pulses to occur when set to the SGL position and the SGL pushbutton is pressed. When this switch is in the NORM position, the clock is free running. This switch is used in either the MTR or MEM mode.
2. SEL 0 and SEL 1 – Select
   These switches allow one of four functions to be displayed on the A, B, C and D indicators located on FE 1 and FE 2. Selection is as follows:

SEL 0	SEL 1	Function
0	0	Address/Parity Clock Counter
1	0	MIR
0	1	INCR
1	1	MPM



3. 8K/4K
   The 8K/4K switch allows the operator to test the first 8K or 4K memory module using three different test patterns.

FE 4 Indicators and Controls

FE 4 contains seven indicators and four toggle switches. They are as follows (see Figure V-3):

Indicators:

1. WAIT
   The WAIT indicator designates whether or not a wait is being performed in the processor when the MTR/MEM (FE 4) toggle switch is set to the MTR position.
2. ERR – Error
   The ERR indicator displays the output of the error flip-flop (FE 4). The ERR indicator is on when there is an inequality in between data from the MPM and data from the pattern generator, NANO or MPM parity error turns this indicator on. It is reset by the RER pushbutton (FE 3) or if the MTR/MEM (FE 4) toggle switch is set to the MTR position.
3. STOP
   The STOP indicator displays the output of the stop flip-flop (FE 4). In MPM mode, the STOP indicator is on when the system clock is disabled by the FE logic. The indicator is turned off by the PRO PB (FE 3) or if the MTR/MEM (FE 4) toggle switch is set to the MTR position.
4. SC1 – SC8 – Sequence Counter Indicators representing the four bits of the sequence counter SC1 is the least significant bit and SC8 is the most significant bit. Table V-1 list the functions represented by the SC indicators and counts.

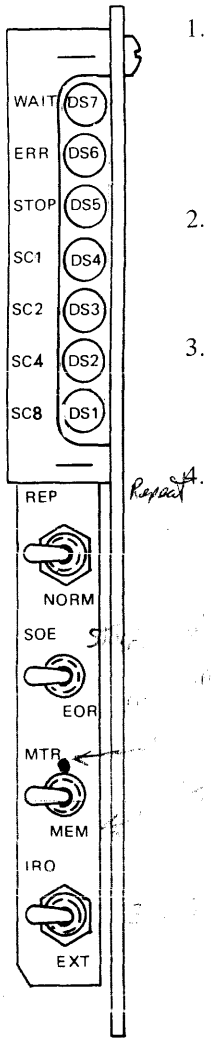


Fig. V-3 FE4 CARD

Toggle Switches:

1. REP/NORM – Repeat Normal
   This switch allows a given sequence count (SC1-6) to be repeated (recycled continuously) when set to the REP position. The memory test is executed in the normal sequence when the switch is in the NORM position.
2. SOE/EOR – Stop on Error/Error Override
   This switch in the SOE position will cause the memory test to stop when an error occurs or if in the EOR position, overrides the error condition.
3. MTR/MEM
   This switch in the MEM position permits testing the MPM and NPM; in the MTR position, permits a program to be executed from the MPM.
4. IRQ/OFF/EXT
   This switch enables a number of functions depending upon the position of the MTR/MEM.

   The switch set to the IRQ position forces PSIRQ/ to go false, and when set to the EXT position, it forces SMEXT/ to go false. The IRQ/EXT switch set to the OFF position removes the input to both PSIRQ/ and SMEXT/. The IRQ/EXT switch is used by the MTR programs to perform various testing functions.

   When the MTR/MEM toggle switch is in the MEM position and the IRQ/EXT toggle switch is in the OFF or EXT position, the memory test will be executed continuously. If the IRQ/EXT switch is in the IRQ position, the memory test steps through SC=0 to SC=8 and then stops. To recycle the memory test again, press the PRO PB (FE 3).

Maintenance Procedures

TABLE V-1. SEQUENCE COUNTER FUNCTIONS

SC INDICATORS LIT	SEQUENCE COUNTER STATUS				FUNCTION
	SC8	SC4	SC2	SC1	
None (SC=0)	0	0	0	0	Clear processor and FE address counter.
SC1 (SC=1)	0	0	0	1	Write test pattern 1 for 4K or 8K.
SC2 (SC=2)	0	0	1	0	Read and check (bit-per-bit) pattern 1 written by SC=1 count (SC1 indicator) above.
SC1, SC2 (SC=3)	0	0	1	1	Write complement of pattern written by SC=1 count. (Refer to Table V-2.)
SC4 (SC=4)	0	1	0	0	Read and check pattern written by SC=3 count.
SC1, SC4 (SC=5)	0	1	0	1	Write address of each location into itself.
SC2, SC4 (SC=6)	0	1	1	0	Read and check increase count written by SC=5.
SC1, SC2, SC4 (SC=7)	0	1	1	1	Clear processor and FE address counter.
SC8 (SC=8)	1	0	0	0	Count all parity bits found in NPM. NOTE: Shared-memory logic checks parity of of each nanoprogram memory word.
SC3, SC0 (SC=9)	1	0	0	1	Go to SC=0.

TABLE V-2. MPM MEMORY TEST PATTERNS

TEST PATTERN	CORE ADDRESS (INCREMENTER)	DECIMAL EQUIVALENT	DATA PATTERNS	
			EVEN ADDRESSES	ODD ADDRESSES
Test Pattern 1 for 8K (SC=1 and SC=2)	0000 thru 0FFF	0 thru 4095	0's	1's
	1000 thru 1FFF	4096 thru 8191	1's	0's
Test Pattern 2 for 8K (SC=3 and SC=4)	0000 thru 0FFF	0 thru 4095	1's	0's
	1000 thru 1FFF	4096 thru 8191	0's	1's
Test Pattern 1 for 4K (SC=1 and SC=2)	0000 thru 07FF	0 thru 2047	0's	1's
	0800 thru 08FF	2048 thru 4095	1's	0's
Test Pattern 2 for 4K (SC=3 and SC=4)	0000 thru 07FF	0 thru 2047	1's	0's
	0800 thru 08FF	2048 thru 4095	0's	1's

MEMORY TESTS

MPM Exercise

The FE cards will exercise the MPM by storing three different test patterns in the memory. The patterns are a worst case pattern, the complement of the worst case pattern and the address of a location written into itself, which results in an increasing count stored in memory. These patterns are enabled by the sequence counter. Table V-2 lists the worst case and complement patterns 1 and 2 for 4K and 8K.

NPM Exercise

The FE cards will address each NPM word and count the number of parity values being generated. When all values are counted and the last address is read, the stop indicator will be turned on. The final tally of the parity values can be seen on the A, B, C and D indicators located on FE 1 and FE 2 with toggle switches SEL 0 and SEL 1 to the "1" position. This talley is then compared with the expected results in the operating instructions to determine if a failure occurred.

MTR Functions

The FE cards are used in conjunction with each MTR program. They provide switches, pushbuttons and indicators for manual operations. Toggle switches, pushbuttons and indicators that are used are as follows: NORM/SGL (FE 3) toggle switch, the SGL and FST (FE 3) pushbuttons, the SEL 0 and SEL 1 (FE 3) toggle switches, the A, B, C and D indicators (FE 1 and FE 2), the WAIT indicator, the MTR position of the MTR/MEM toggle switch, and the IRQ/EXT toggle switch.

Logic Description

The logic for memory testing and program monitoring is distributed on the four FE cards with appropriate controls and indicators mounted on the front edge of each card. The functional blocks are:

1. Address/Parity and Clock Pulse Counter

   This counter located on FE 1 and FE 2 performs a number of functions:

   a. As address counter during SC=1 through SC=6 in the MEM mode.
   b. As a parity counter during SC=8 (NPM test).
   c. As a clock pulse counter when in the MTR mode. Clock pulses are counted between wait operations.

   The counter is constructed out of four CB elements providing 16 stages. It is cleared by the RER PB (FE 3) when in the MTR mode (FE 4) or the clear signal provided by the clock generator card in the MEM mode. The counter is stepped by a clock pulse during MTR mode. During the MEM mode, it is incremented each time a new address is required for SC=1-SC=6 or a NANO parity bit set (Bit 56) in SC=8) (NPM test).

Pattern Generator

The pattern generator located on FE 1 and FE 2 enables the output of the counter or generates 16 ones or 16 zeros via S2 elements to be transmitted to the memory via T2C's, and to the comparator circuits.

Comparator Circuits/Error FF/Stop FF

The comparator located on FE 1 and FE 2 performs a bit per bit compare of values found on the MPM bus with the bits from the pattern generator logic. The error flip-flop located on FE 4 is set (at P2 time) if there is an inequality during SC=2, 4 and 6. When the SOE/EOR toggle switch (FE 4) is set to the SOE position, the stop FF will set and force the test to stop if an inequality occurs. The stop FF will also be set during SC=8 when the last NPM address is read.

Display Selector

The SEL 0 and SEL 1 toggle switches located on FE 3 route data from one of four sources to the A, B, C and D indicators located on FE 1 and FE 2. The four sources are MPM, MIR, INCR and AC/PAR/CLK COUNTER.

Sequence Counter and Decoding Circuits

The Sequence Counter (SC) located on FE 4 is a four-stage counter implemented by the use of a CB element. The SEQ counter outputs are displayed on the front of FE 4. They are also routed to a decoder employing a DM element also located on FE 4.

Phases

There are two phases used during memory test. They are P1 and P2. The phase flip-flop is located on FE 4.

Functions Performed at P1 Time

1. Step Address Counter
2. Compare MPM with expected Values during Read Operations for SC=2, 4 or 6.
3. Enable Write when SC=1, 3 or 5.

Functions Performed During P2 Time

1. Clear or Step Sequence Counter
2. Clear or Step MPCR
3. Clear Address Counter

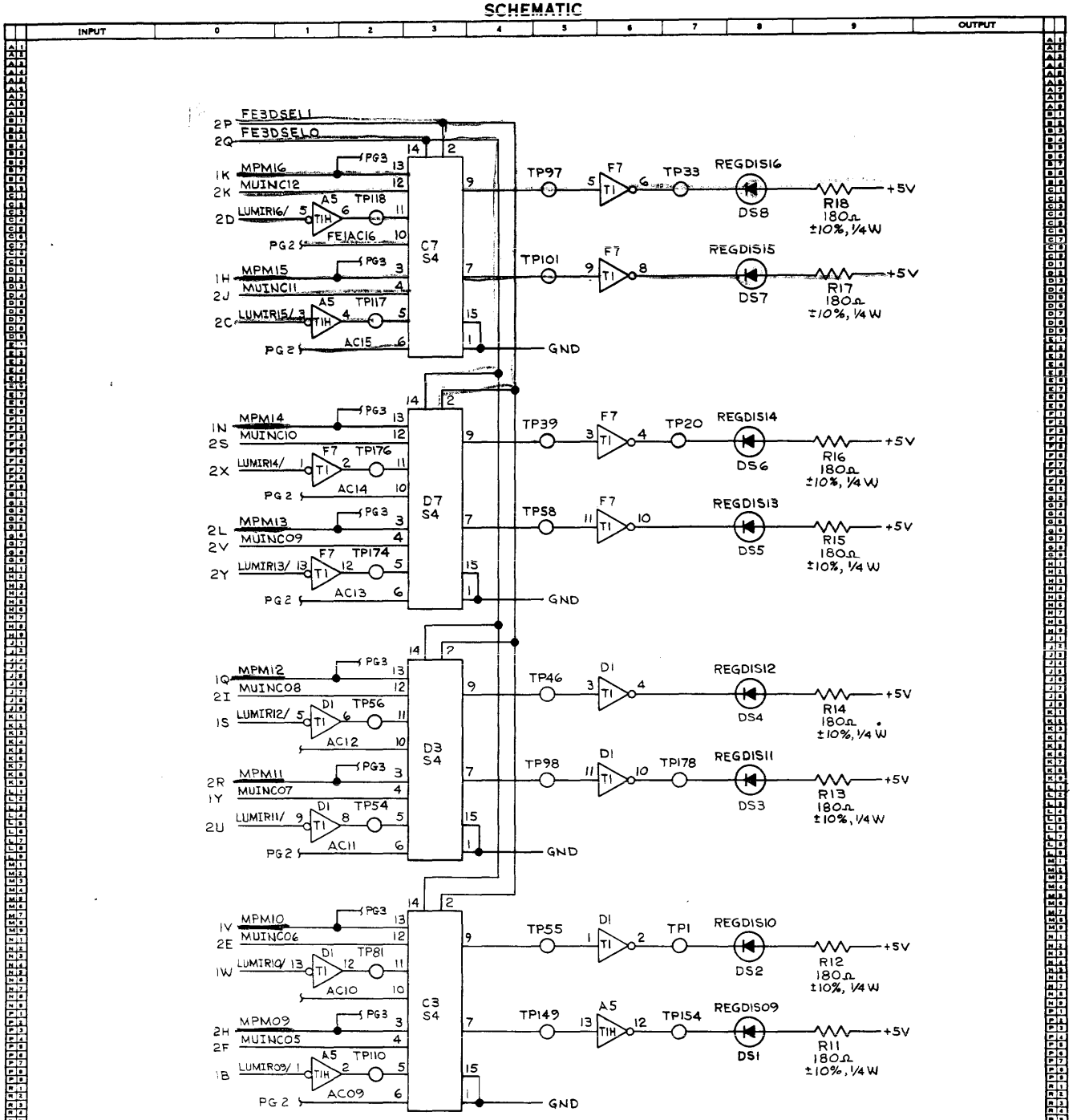
The Phase FF is inhibited by the output of the Stop FF, or by the MTR/MEM switch when in the MTR position.

Last Address FF

The LADDR FF is used to store occurrence of the last address pulse.

FE1

SCHEMATIC



CODE	PART NO.	QTY
	1447 5396	1
X4	447 3698	2
T2C	1447 3581	4
T2	1447 3516	1
TIH	479 7971	1
T1	1447 3532	2
S4	447 3714	4
S2	447 3797	2
C8	1447 3771	2

CC 2-9520

SH Q.011

Burroughs Corporation
MAGNETIC SYSTEMS PLANT DOWNINGTOWN, PA 19335

PRODUCTION

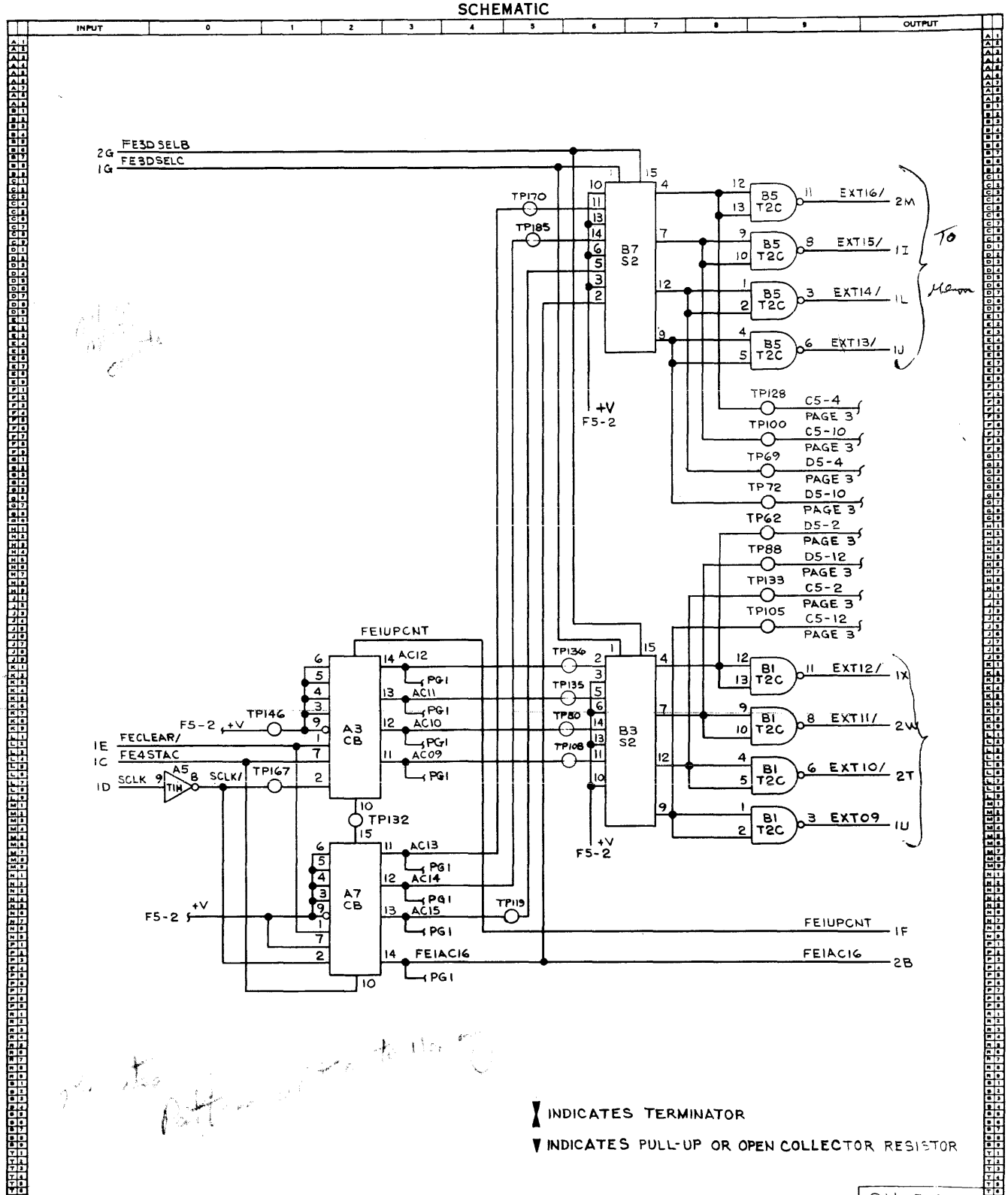
TITLE FE1, FIELD ENGINEERING CARD 1
SYSTEM B700
DRAWN B. FEGER
APPROVED W. MAN. H. CASWELL
CHECKED R. WALTZ
RELEASED 3-2-72
DWG. NO. 1448 1956
PAGE 1 OF 3
REV. LETTER B PER ECN 755 REDRAWN W/O CHG

PRINTED IN U. S. AMERICA

DTN 96 4-71

FE 1-2

SCHEMATIC



SH.0.012

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SYSTEM B700
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DWG. NO. 1448 1956
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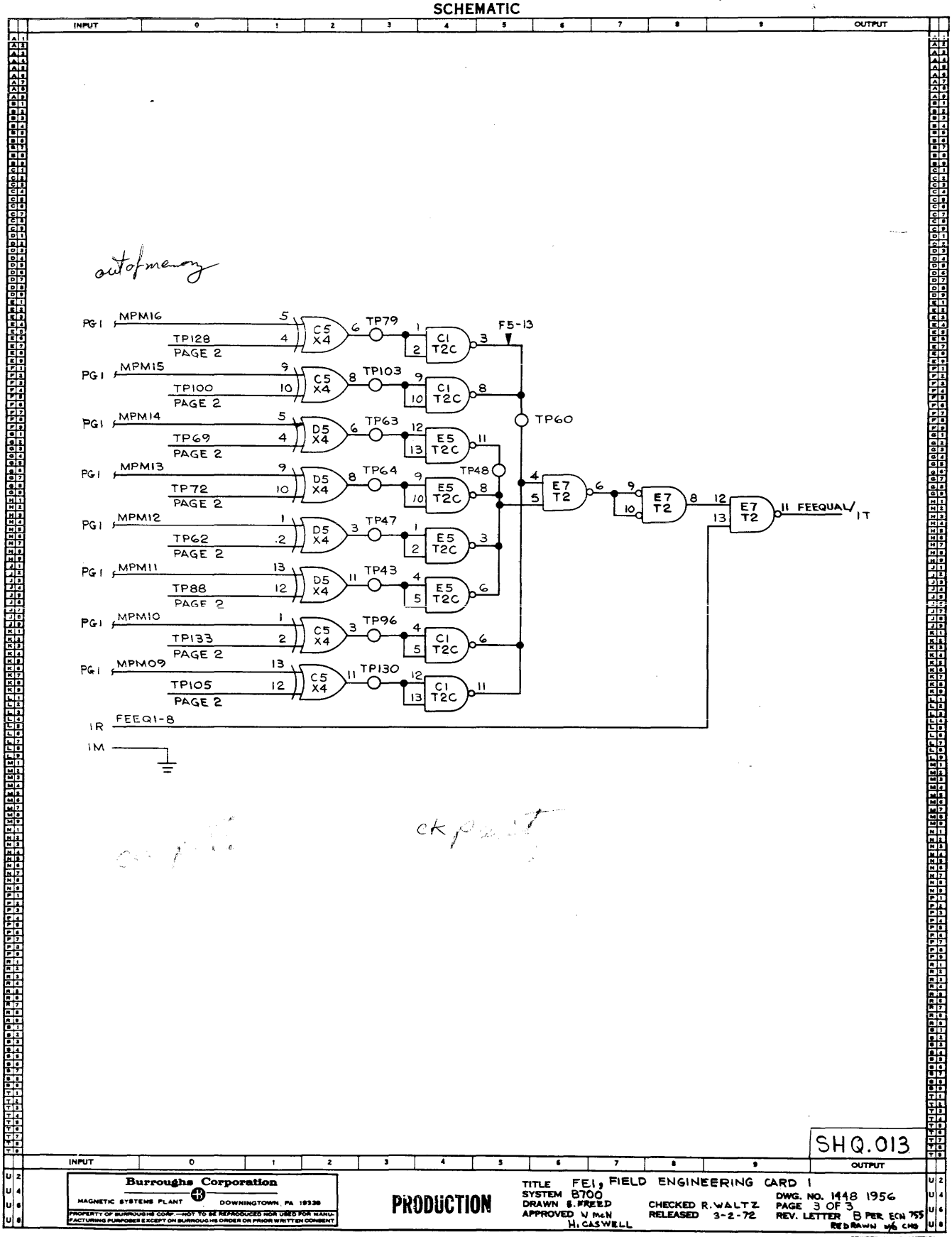
Maintenance Procedures

FE1-3

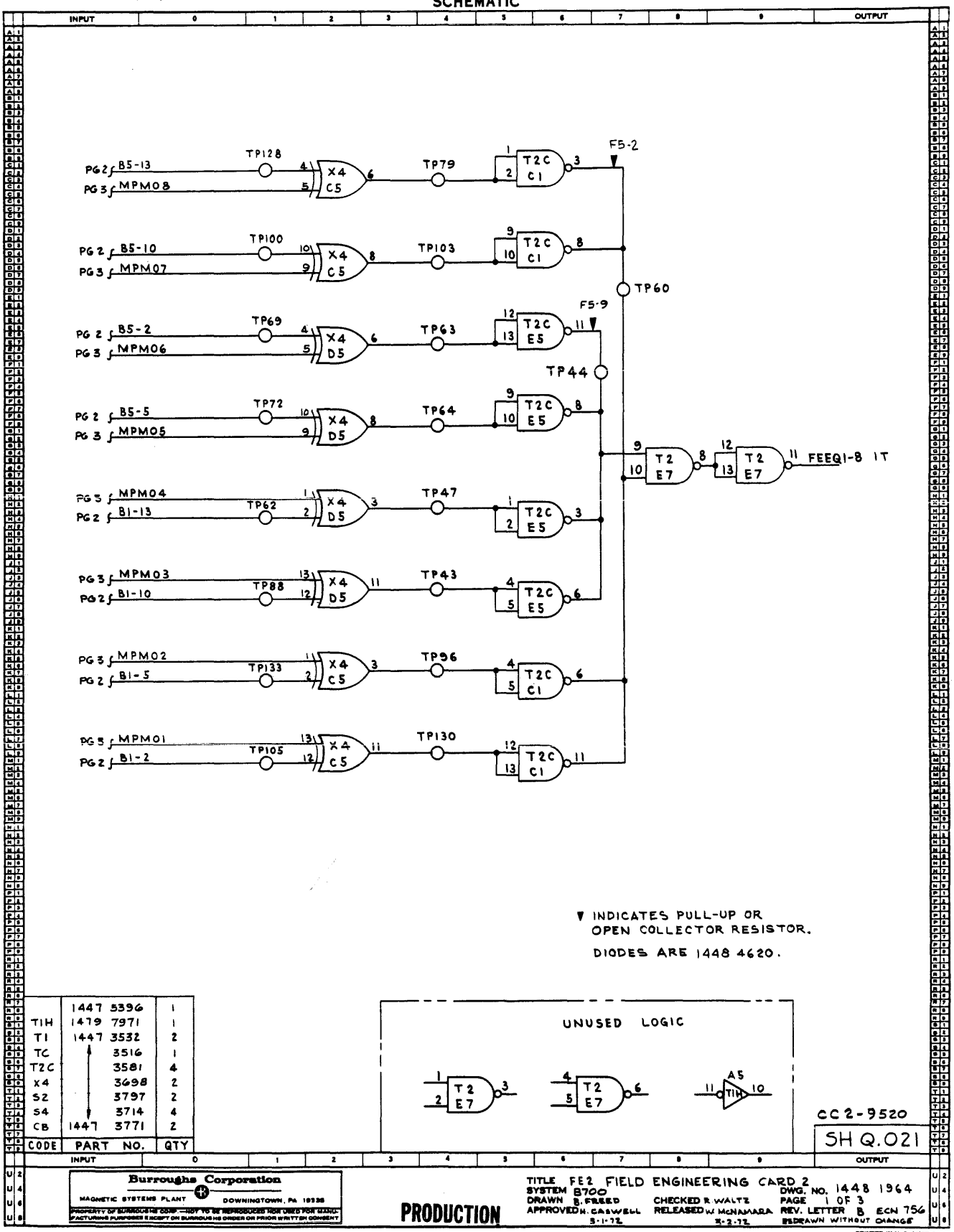
SCHEMATIC



Maintenance Procedures

FE 2-1

SCHEMATIC



▼ INDICATES PULL-UP OR OPEN COLLECTOR RESISTOR.

DIODES ARE 1448 4620.

CODE	PART NO.	QTY
	1447 5396	1
TIH	1479 7971	1
TI	1447 3532	2
TC	3516	1
TZC	3581	4
X4	3698	2
S2	3797	2
S4	3714	4
CB	1447 3771	2

UNUSED LOGIC

CC2-9520

SH Q.021

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TITLE FE2 FIELD ENGINEERING CARD 2
SYSTEM B700
DRAWN B. FREED
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DWG. NO. 1448 1964
PAGE 1 OF 3
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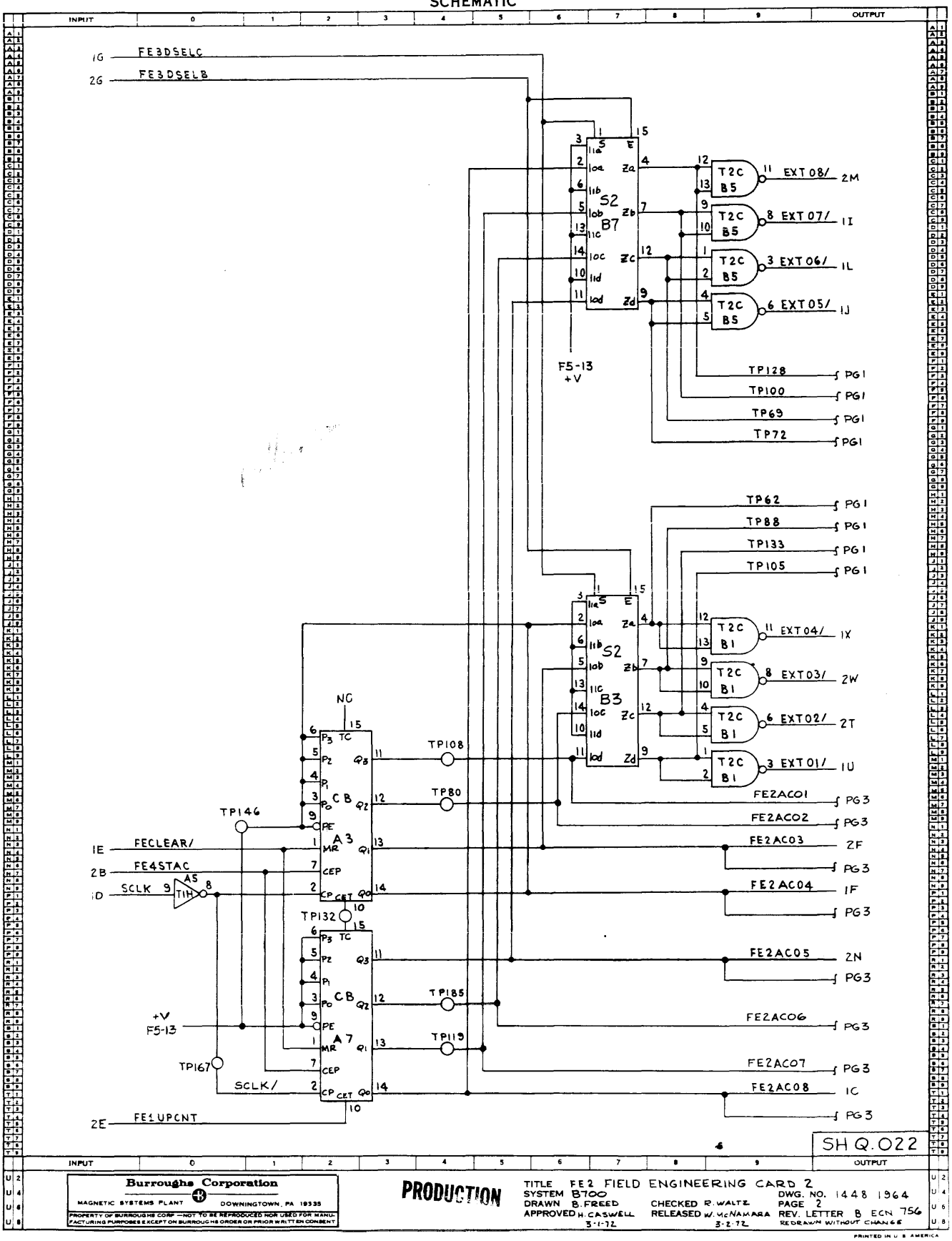
FE2-2

SCHEMATIC



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SYSTEM B700
DRAWN B. FREED
APPROVED H. CASWELL 3-1-72
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RELEASED W. McNAMARA 3-2-72
DWG. NO. 1448 1964
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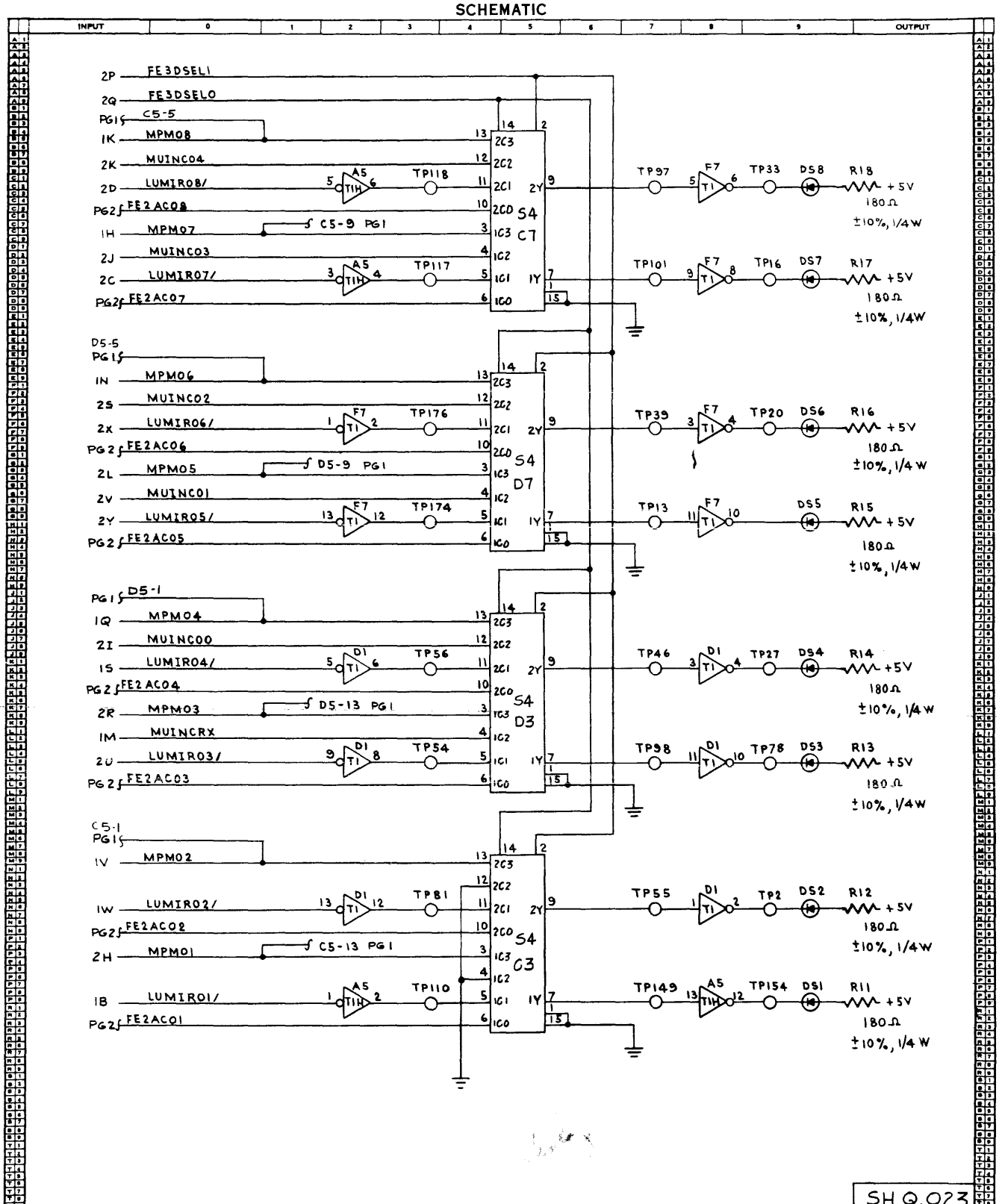
FE2-3

SCHEMATIC



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SYSTEM B700 DWG. NO. 1448 1964
DRAWN B. FREED CHECKED R. WALTZ PAGE 3
APPROVED H. CASWELL RELEASED W. McNAMARA REV. LETTER B ECN 756
3-1-72 3-2-72 REDRAWN WITHOUT CHANGE

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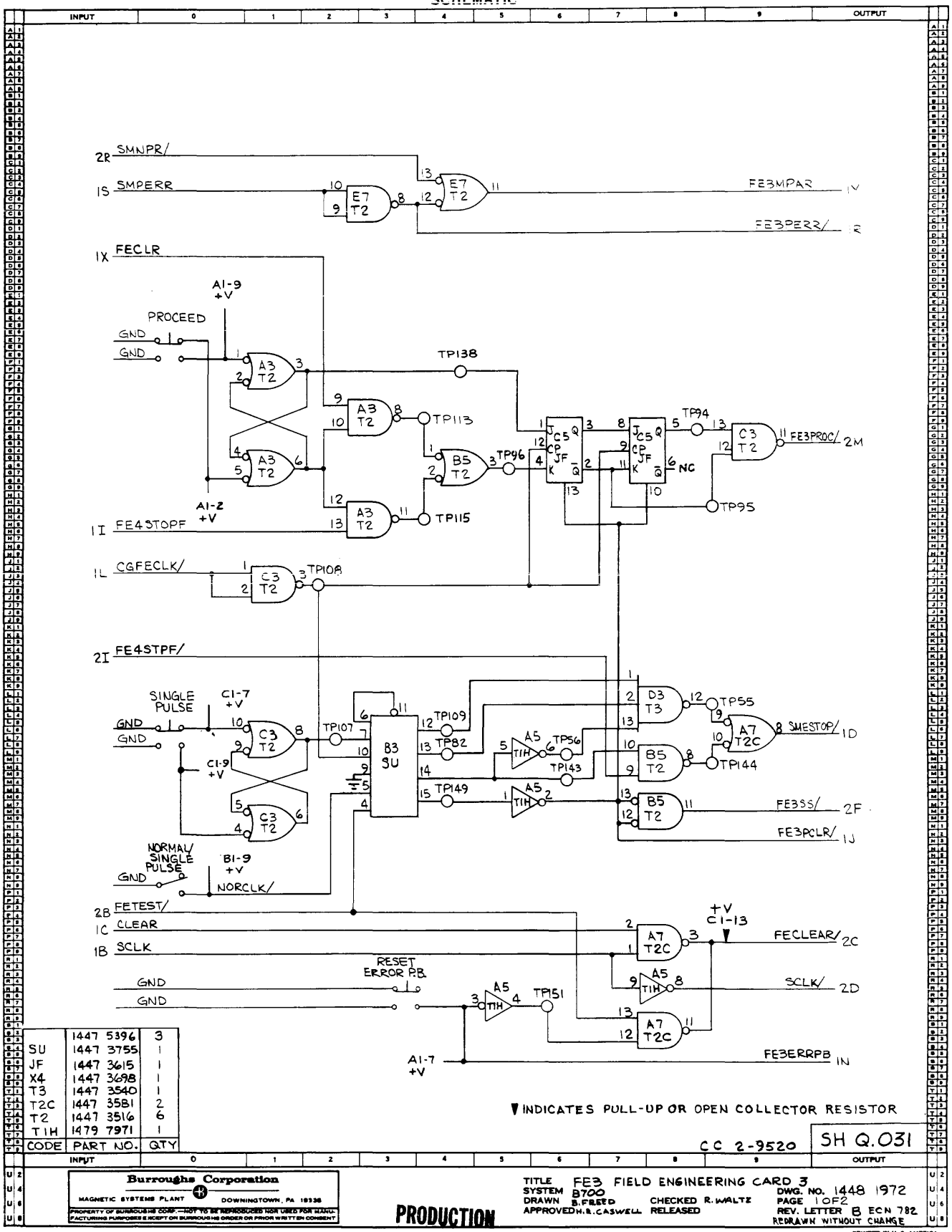
FE 3-1

SCHEMATIC



CODE	PART NO.	QTY
	1447 5396	3
SU	1447 3755	1
JF	1447 3615	1
X4	1447 3698	1
T3	1447 3540	1
T2C	1447 3581	2
T2	1447 3516	6
TIH	1479 7971	1

▼ INDICATES PULL-UP OR OPEN COLLECTOR RESISTOR

CC 2-9520 SH Q.031

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SYSTEM B700
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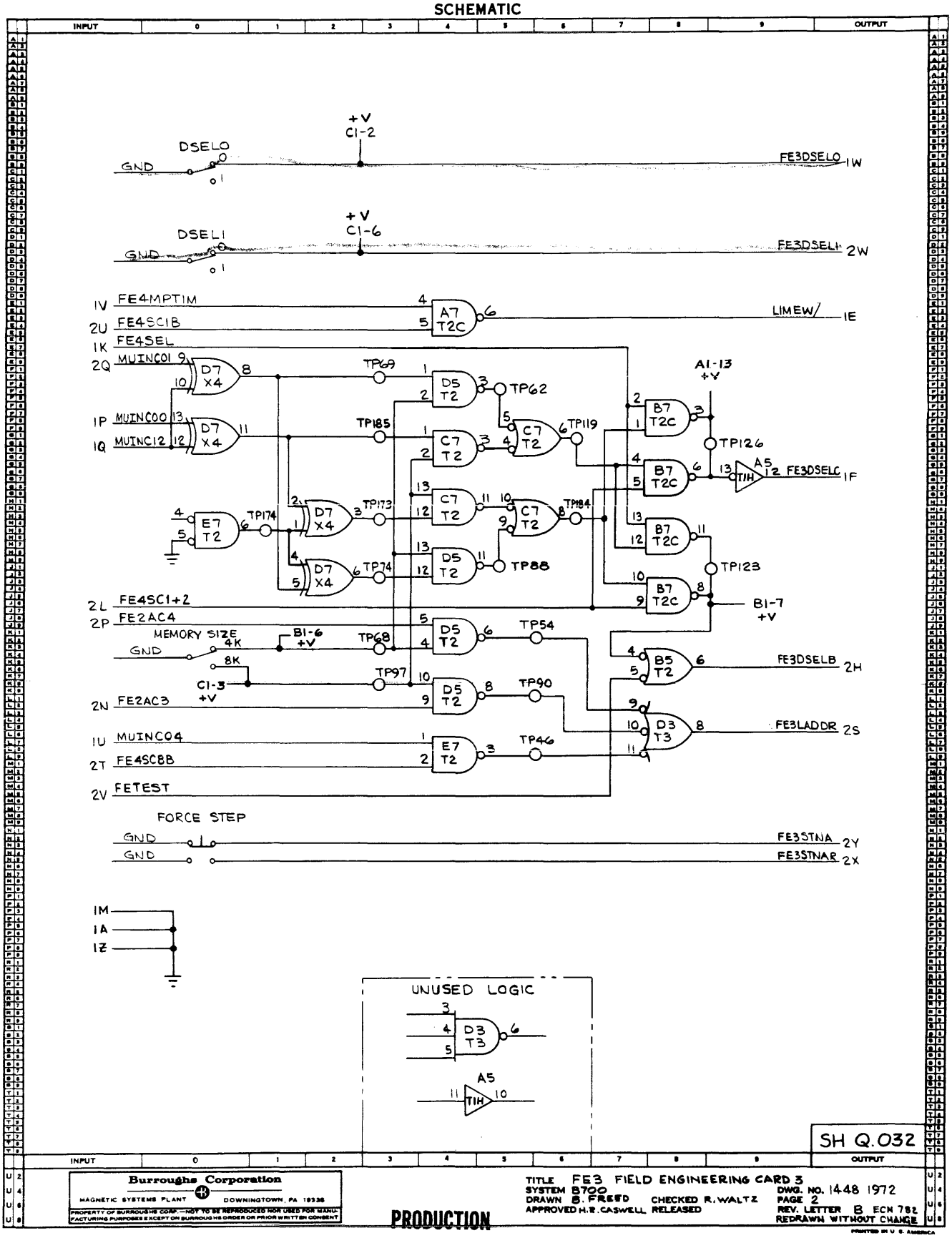
APPROVED H.E.CASWELL RELEASED
DWG. NO. 1448 1972
PAGE 1 OF 2
REV. LETTER B ECN 782
REDRAWN WITHOUT CHANGE

DTN 96 4-71

SCHEMATIC



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SYSTEM B700
DRAWN B. FREED CHECKED R. WALTZ
APPROVED H.R. CASWELL RELEASED
DWG. NO. 1448 1972
PAGE 2
REV. LETTER B ECN 782
REDRAWN WITHOUT CHANGE

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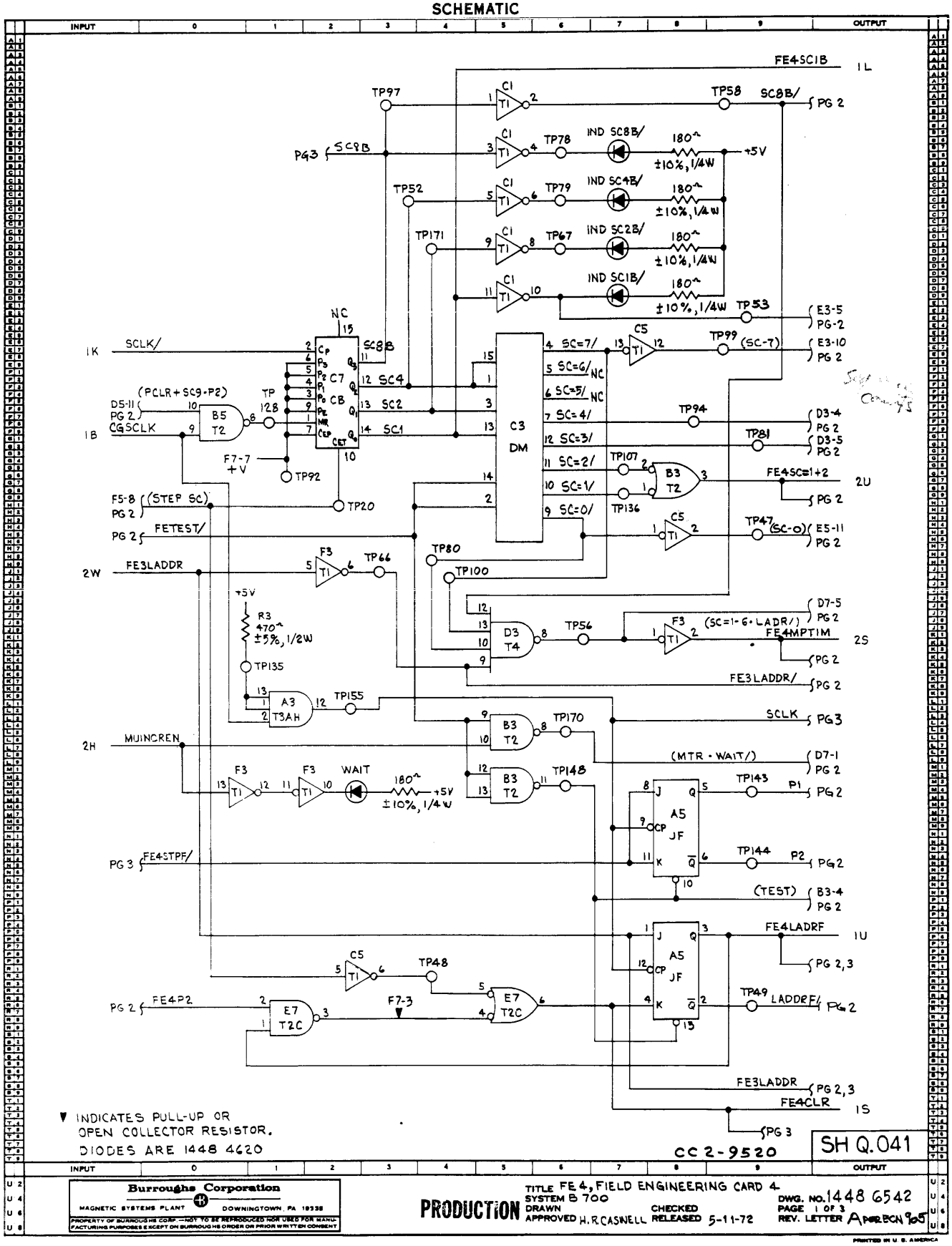
SCHEMATIC


FE4SC1B
TP97
TP58
SC8B/
PG 2
TP78
IND SC8B/
180^ ±10%, 1/4W
+5V
PG3 SC8B
TP52
TP79
IND SC4B/
TP171
TP67
IND SC2B/
IND SC1B/
TP53
E3-5 PG-2
NC
SC8B
SCLK/
TP99
(SC-7)
E3-10 PG 2
SC4
SC2
SC1
C7
CB
C3 DM
SC=7/
SC=6/ NC
SC=5/ NC
SC=4/
SC=3/
SC=2/
SC=1/
SC=0/
TP94
D3-4 PG 2
TP81
D3-5 PG 2
(PCLR+SC9-P2)
D5-11 PG 2 CGSCLK
B5 T2
TP 128
F7-7 +V
TP92
TP107
TP136
FE4SC=1+2
2U
F5-8 (STEP SC) PG 2
TP20
FETEST/ PG 2
TP47 (SC-0)
E5-11 PG 2
TP80
TP100
FE3LADDR
TP66
+5V
R3 470^ ±5%, 1/2W
TP135
TP56
D7-5 PG 2
(SC=1-6-LADR/)
FE4MPTIM
2S
FE3LADDR/ PG 2
A3 T3AH
TP155
SCLK PG3
MUINCREN
TP170
(MTR-WAIT/)
D7-1 PG 2
WAIT
TP148
TP143
P1 PG 2
A5 JF
PG 3 FE4STPF/
TP144
P2 PG2
(TEST)
B3-4 PG 2
FE4LADRF
1U
PG 2,3
TP48
PG 2 FE4P2
E7 T2C
F7-3
TP49
LADDRF/ PG 2
FE3LADDR
PG 2,3
FE4CLR
1S
PG 3
▼ INDICATES PULL-UP OR OPEN COLLECTOR RESISTOR.
DIODES ARE 1448 4620
CC 2-9520
SH Q.041
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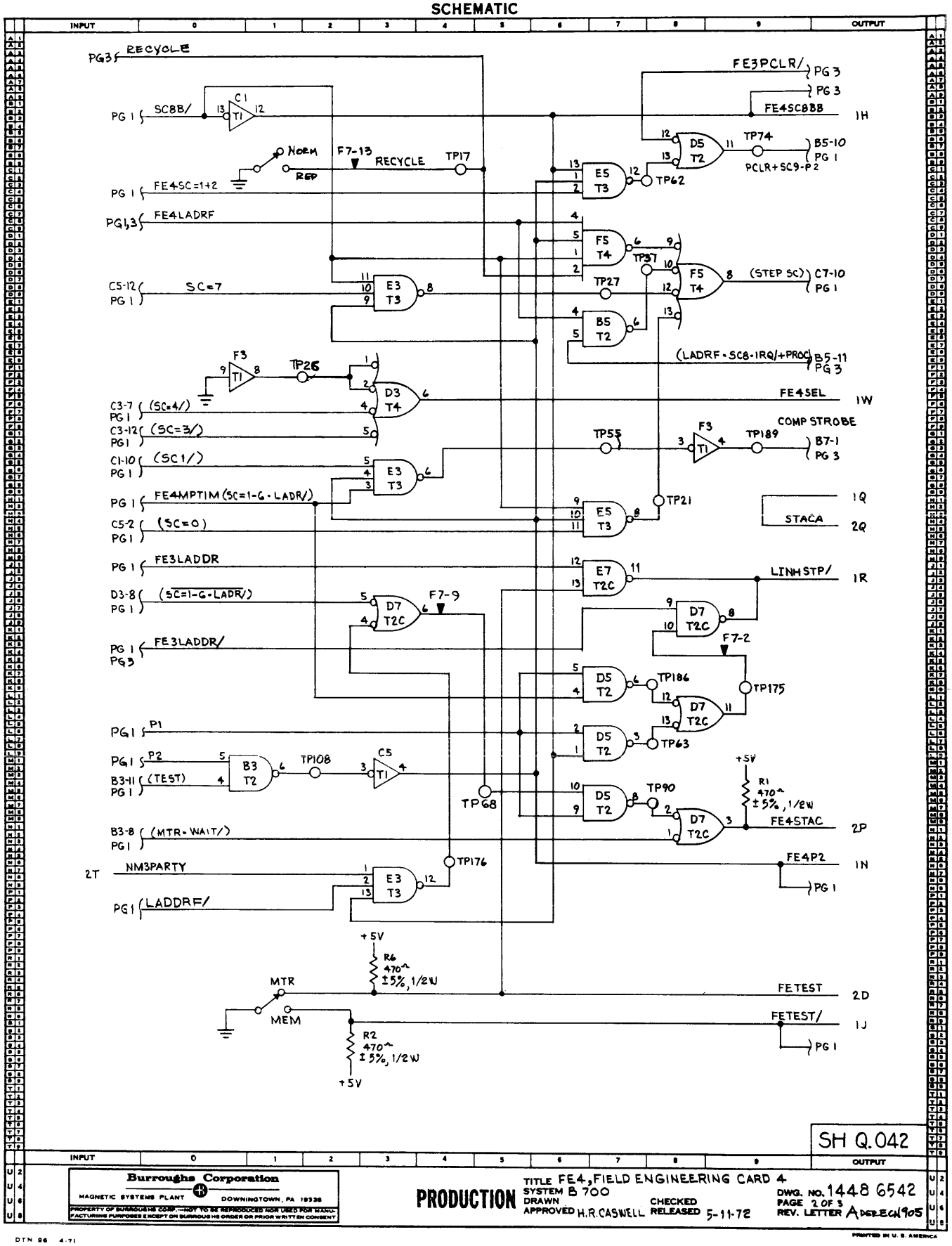
SYSTEM B 700
DRAWN
APPROVED H.R.CASWELL
CHECKED
RELEASED 5-11-72
DWG. NO. 1448 6542
PAGE 1 OF 3
REV. LETTER A PER ECN 905

SCHEMATIC



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SYSTEM B 700
DRAWN
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DWG. NO. 1448 6542
PAGE 2 OF 3
REV. LETTER A DER ECN 905

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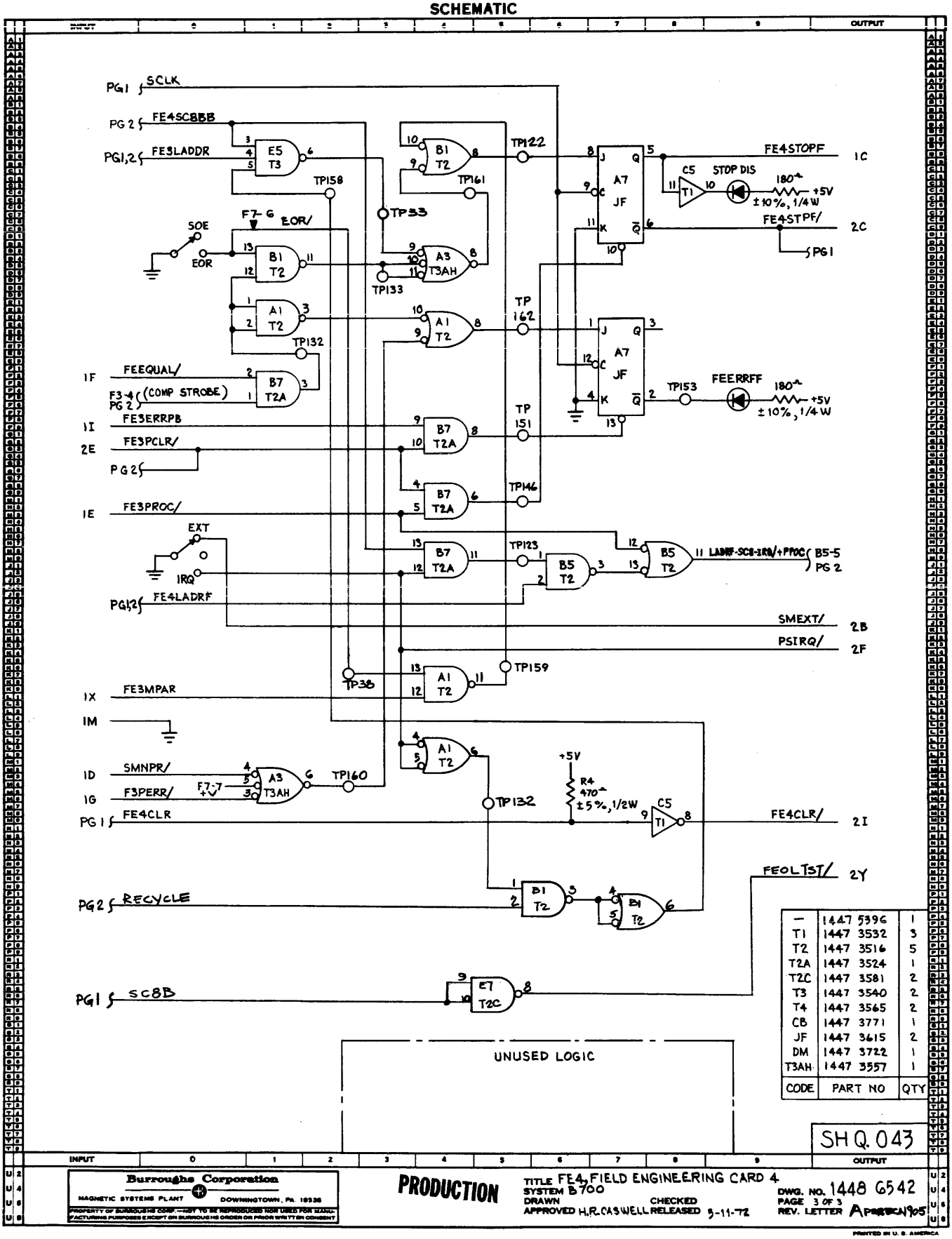
SCHEMATIC



CODE	PART NO	QTY
—	1447 5396	1
T1	1447 3532	3
T2	1447 3516	5
T2A	1447 3524	1
T2C	1447 3581	2
T3	1447 3540	2
T4	1447 3565	2
CB	1447 3771	1
JF	1447 3615	2
DM	1447 3722	1
T3AH	1447 3557	1

SH Q. 043

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MAGNETIC SYSTEMS PLANT — DOWNINGTOWN, PA. 19335

PRODUCTION

TITLE FE4, FIELD ENGINEERING CARD 4
SYSTEM B700
DRAWN
CHECKED
APPROVED H.R. CASWELL RELEASED 9-11-72
DWG. NO. 1448 6542
PAGE 3 OF 3
REV. LETTER A

MTR METER

The maintenance test routine meter is a special meter designed for use with the MTR system. The meter has a twofold purpose. It will register the duty cycle of a signal and also verify that the signal is within electrical specifications. An explanation of these two functions will be given later.

The MTR meter does not contain an internal power source. It obtains its operating voltages from the Processor Unit being tested. The meter requires a +12 volt, a -12 volt and a ground connection in order to function properly. This is obtained by connecting the 50 pin connector of the MTR meter to J88 of the Processor Unit being tested. J88 is located at coordinate BP3 of the Processor Unit logic section.

The meter contains five pushbuttons, a lamp, a banana type connector plug and a meter face labeled duty cycle. The five pushbuttons are labeled CLOCK, RESET, DUTY CYCLE, X10 and INVERT. The lamp is labeled ELEC. TEST. The banana type connector plug is labeled SIG. The signal test lead supplied with the MTR meter is connected to the connector plug marked SIG. With the meter connected to J88 and the machine turned on, the electrical test lamp should be lit. The following is a description of the function of each of the five pushbuttons:

RESET

The reset button works in conjunction with the electrical test lamp. With the test lead connected to a backplane pin with a valid signal available, depression of the reset button should extinguish the lamp. If the lamp does not extinguish, this means the signal being tested is not within electrical specifications.

The electrical specifications for the Processor Unit signals are as follows:

A. A true signal must have an amplitude greater than +2.5 volts.
B. A false signal must have an amplitude less than +.4 volts.
C. The time lapse between +.4 and +2.5 volts on a signal rise or signal fall must not exceed 2 microseconds.

CLOCK

The clock button is used to check the rise and fall time of the clock pulses. It divides the time lapse by 10; therefore, if the time lapse is greater than .2 microseconds, the indicator will light. The clock button checks only the time lapse; therefore, the reset button must be depressed first.

DUTY CYCLE

When the duty cycle button is held depressed, the meter will register in percent the duty cycle of the signal being checked. The duty cycle of a signal is defined as the time the signal is true or in the "1" state. For example, if a signal is true for 25 ms, then false for 25 ms and continues at this rate, it will register 50% duty cycle on the meter when the duty cycle button is held depressed.

NOTE: Depression of the duty cycle button will cause the electrical test lamp to light; therefore, requiring depression of the reset button to extinguish the test lamp when checking the next signal.

X10

The X10 button when depressed along with the duty cycle button will alter the meter range to read 10% at full scale. Always read the duty cycle without the X10 first to verify that the value is below 10%. This will prevent possible meter damage.

INVERT

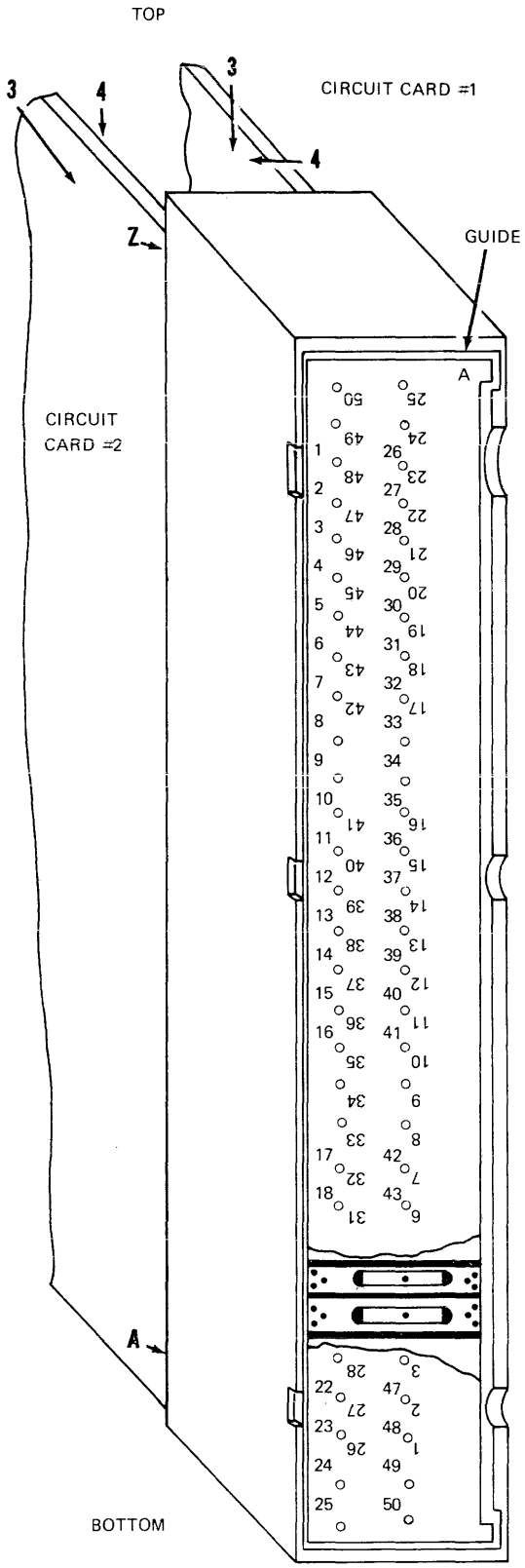
When the invert button is depressed along with the duty cycle button, the duty cycle reading will be inverted. For example, if a signal registers 20% when the duty cycle button is depressed, the same signal will register 80% when the invert button is depressed along with the duty cycle button. If the inverted reading registers less than 10%, the X10 button may be depressed along with the duty cycle and invert buttons to enable a more accurate reading.

The sequence for using the MTR meter is first depress the reset button to test the electrical specifications of the signal. If the signal is within specification, meaning the lamp does turn out, then read the duty cycle of the signal. The reason for following this sequence is that the meter circuit will register a duty cycle for any signal with an amplitude greater than +1.3 volts, but a signal that is less than +2.5 volts is out of electrical specification.

CAUTION: The MTR meter should be used only on the backplane of the Processor Unit as the meter is designed for reading signals with an amplitude of +30 volts. Any voltage greater than +30 volts will result in damage to the meter.

FRONTPLANE CONNECTORS

Frontplane connectors (Figure V-4) are used on the CPU/TPU frontplane to interconnect adjacent I/O control (IOC/DDP) cards. Figure V-4 shows the installation of a frontplane connector (1534 3940) on cards 1 and 2 (right-to-left) in an IOC location. Also shown are the card pin interconnections and corresponding test points on the face of connector. Figure V-5 is an electrical schematic and representative interconnection diagram. Refer to Section VI for I/O control card functions, IOC/DDP card locations, and foreplane connector locations.



INTERCONNECTIONS AND TEST POINTS *

PIN(S) (TEST POINTS)	FROM CKT. CARD 1	TO CKT. CARD 2	PIN(S) (TEST POINTS)	FROM CKT. CARD 1	TO CKT. CARD 2
50	Z3	Z4	25	Z4	Z3
49	Y3	Y4	24	Y4	Y3
1, 48	X3	X4	26, 23	X4	X3
2, 47	W3	W4	27, 22	W4	W3
3, 46	V3	V4	28, 21	V4	V3
4, 45	U3	U4	29, 20	U4	U3
5, 44	T3	T4	30, 19	T4	T3
6, 43	S3	S4	31, 18	S4	S3
7, 42	R3	R4	32, 17	R4	R3
8	–	–	33		
9	–	–	34		
10, 41	Q3	Q4	35, 16	Q4	Q3
11, 40	P3	P4	36, 15	P4	P3
12, 39	N3	N4	37, 14	N4	N3
13, 38	M3	M4	38, 13	M4	M3
14, 37	L3	L4	39, 12	L4	L3
15, 36	K3	K4	40, 11	K4	K3
16, 35	J3	J4	41, 10	J4	J3
34	I3	I4	9	I4	I3
33	H3	H4	8	H4	H3
17, 32	G3	G4	42, 7	G4	G3
18, 31	F3	F4	43, 6	F4	F3
19, 30	E3	E4	44, 5	E4	E3
20, 29	D3	D4	45, 4	D4	D3
21, 28	C3	C4	46, 3	C4	C3
22, 27	B3	B4	47, 2	B4	B3
23, 26	A3	A4	48, 1	A4	A3
24	–	–	49		
25	–	–	50		

*INTERCONNECTIONS ARE SHOWN FOR FRONTPLANE CONNECTOR GUIDE SYMBOL "A" AT TOP-RIGHT CORNER AND FROM TOP TO BOTTOM OF CARDS. (SEE FIGURE V-5 FOR SCHEMATIC AND INTERCONNECTION DIAGRAM.) REVERSE PIN/TEST POINT COLUMNS IF FRONTPLANE CONNECTOR IS INSTALLED WITH GUIDE SYMBOL "A" AT BOTTOM-LEFT.

Fig. V-4 FRONTPLANE CONNECTOR

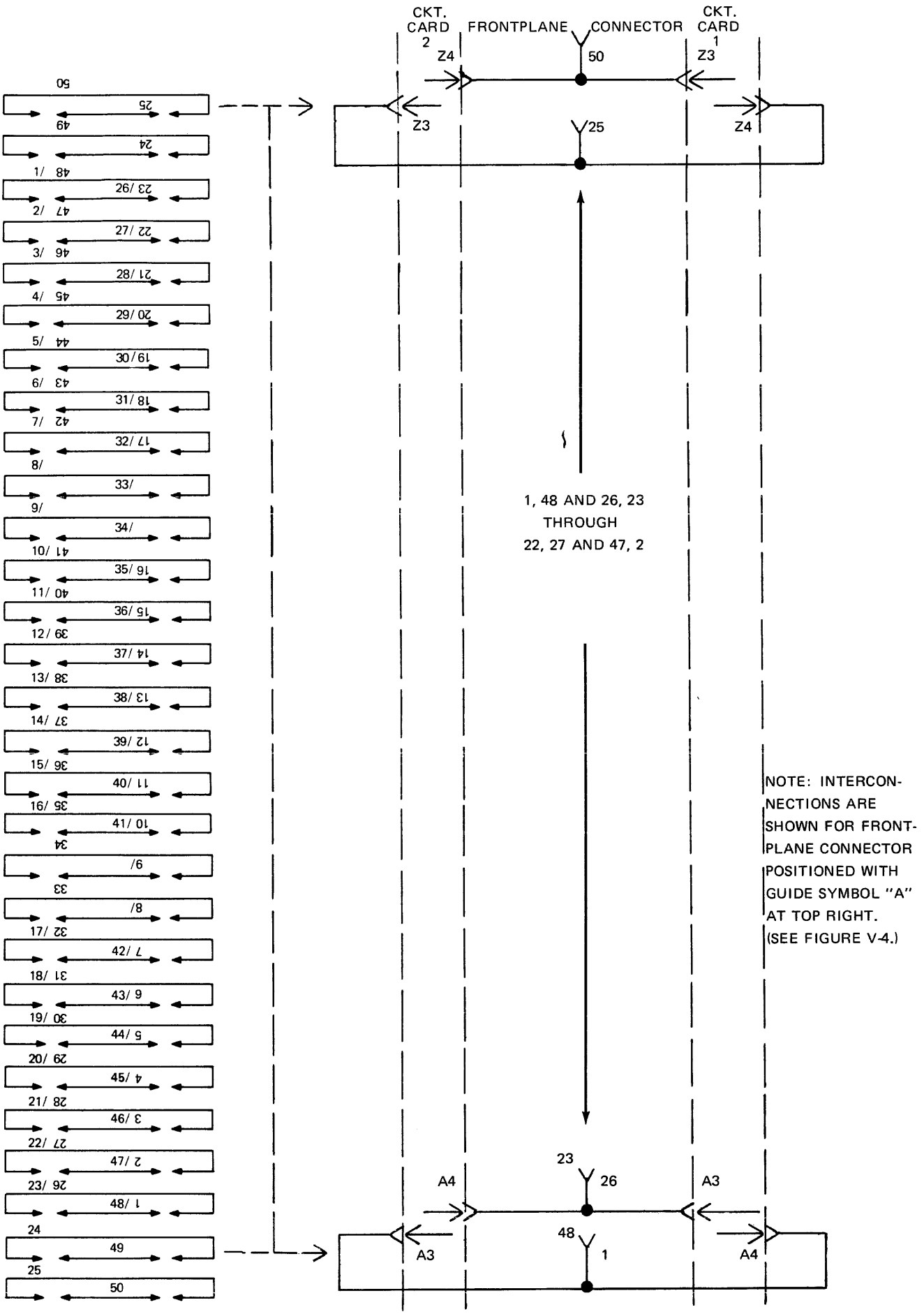


Fig. V-5 FRONTPLANE CONNECTOR SCHEMATIC AND REPRESENTATIVE INTERCONNECTIONS

FIELD TEST AND REFERENCE (FT&R) DOCUMENTATION

VOLUME I

Volume I of the FT & R documents includes:

1. Processor Logic Schematics
2. Circuit Card Assembly Drawings
3. Standard Assembly No. 2 14/16 & 16 Pin Drawings
4. Capacitor Rectifier Assembly Drawings
5. Power Control Assembly
6. Wire Lists, Cables and Harness
7. Timing Diagram for AC Control
8. Backplane Map, Logic Rack and Memory Rack
9. Connection Diagram for Cables
10. +5 Volt Tap Adjustment Procedure
11. Hardware Memory Address Limit Wiring Procedure

VOLUME II – BACKPLANE CIRCUIT LISTS

PROCESSOR

The Processor backplane circuit list is a circuit list of signal names in alphanumeric order. The signal names are related to the signal names on the logic drawing except for the interchangeable DDP's. Since the interchangeable DDP locations can contain any of the several peripheral DDP's, the true DDP signal name cannot be used. The signal names of the DDP's that will not appear as such in the Processor backplane circuit list are as follows:

1. DDP P.C. Card to an I/O Control
2. I/O Control to a DDP P.C. Card
3. DDP P.C. Card to a DDP P.C. Card Internal to a DDP Location

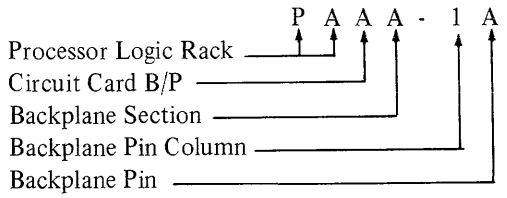
These three groups of signal names will appear in the Processor backplane circuit list as follows:

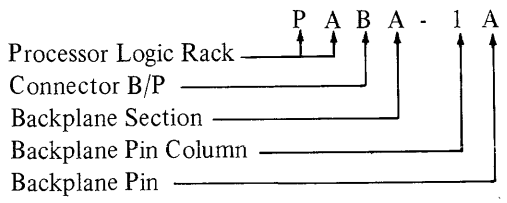
1. DDP P.C. Card to an I/O Control – the I/O control being the DDP connector (PA91-97)
   a. DDP (1-7) IC (01-50) EX DDP1IC01
      IC1-50 represents the 50 pin connector. DDP 1-7 represents the DDP location. IC1-50 can be related to the DDP signal name by use of the wire list for the I/O cable or adapter cable whichever connects to DDP connectors PA91-97.
2. I/O Control to a DDP P.C. Card – I/O control being the DDP connector (PA91-97)
   a. Same as No. 1.
3. DDP P.C. Card to a DDP P.C. Card Internal to a DDP Location. Each DDP location may contain up to four P.C. cards. Within each DDP backplane location there are several backplane pins wired together to form a bus between P.C. cards of a DDP. There are three busses for each DDP backplane location and they are named as follows:
   a. DDPn2B – Ex DDP12BA
   b. DDPn3B – Ex DDP13BA
   c. DDPn4B – Ex DDP14BA

   Figure V-6 (two sheets) shows the interconnection of the standard IOC/DDP four-card interface. Refer to the corresponding FT&R documents for specific interconnection diagrams.

DDP'S

Each peripheral DDP has a unique backplane circuit list. This circuit list is in alphanumeric order and can only be used if the peripheral DDP backplane templates are attached to the DDP backplane and the DDP connector backplane. The backplane pins of these DDP templates refer to:





MEMORY BACKPLANE

The memory backplane circuit list is a circuit list of signal names in alphanumeric order. The signal names are related to the signal names located on the memory logic drawings.

Processor to Memory Interconnections

Interconnections between the processor and memory section are from jacks PA80 and PA81 of the processor section to PB78 and PB79 of the memory section. Figure V-7 is a cross-reference chart to aid in tracing interconnections between these sets of jacks, which have different pin-referencing schemes. For example, as viewed from the backplane, pin 5 at location BI9A or PA80 is connected to pin 5 at location BF3E on PB78.

VOLUME III – MEMORY DOCUMENTS

The memory documents contain the memory installation instructions, system timing diagram and the parts lists, assembly drawings and schematics for all memory circuit boards.

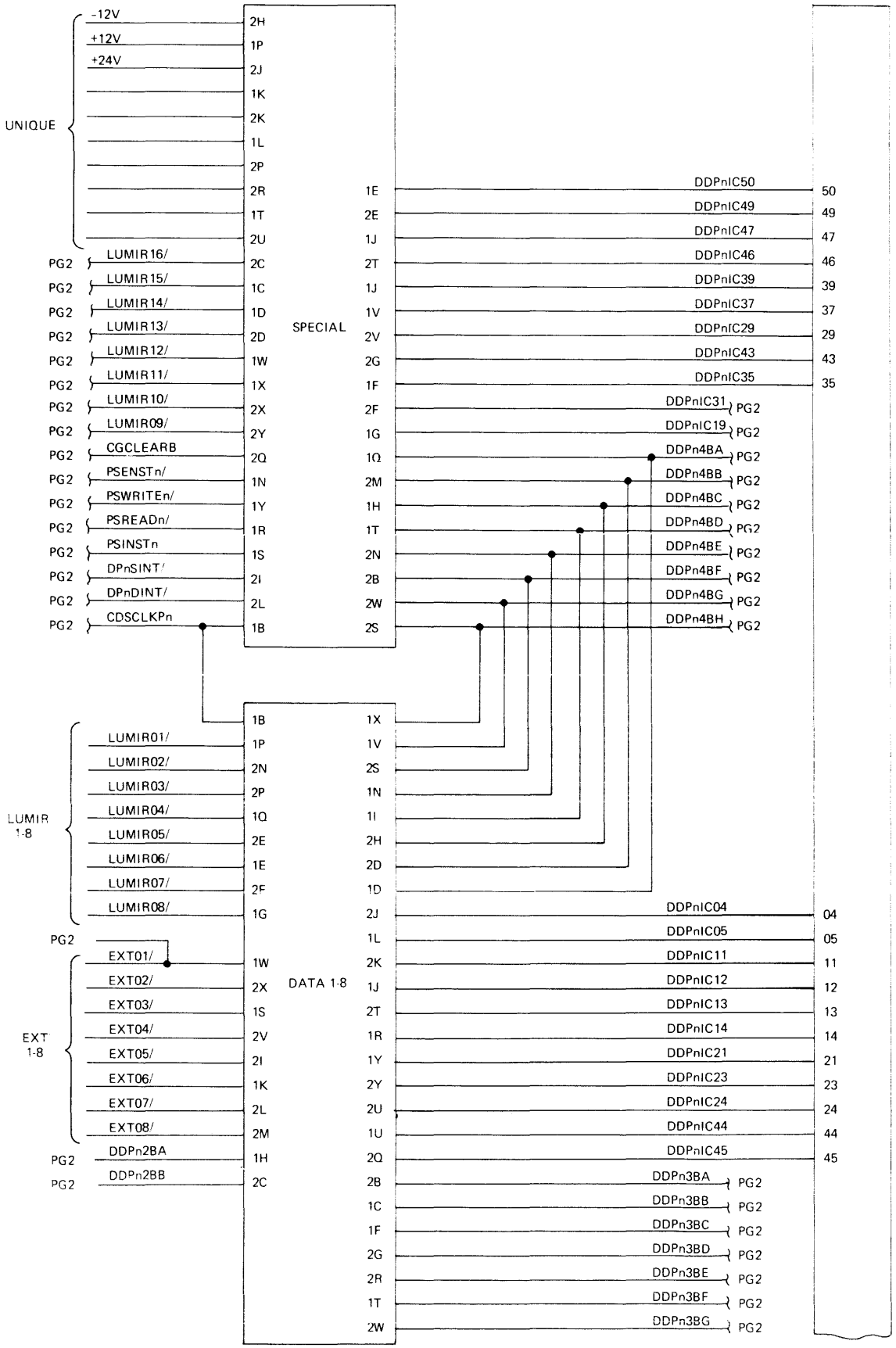


Fig. V-6 STANDARD IOC/DDP INTERCONNECTION DIAGRAM
(SHEET 1 OF 2)

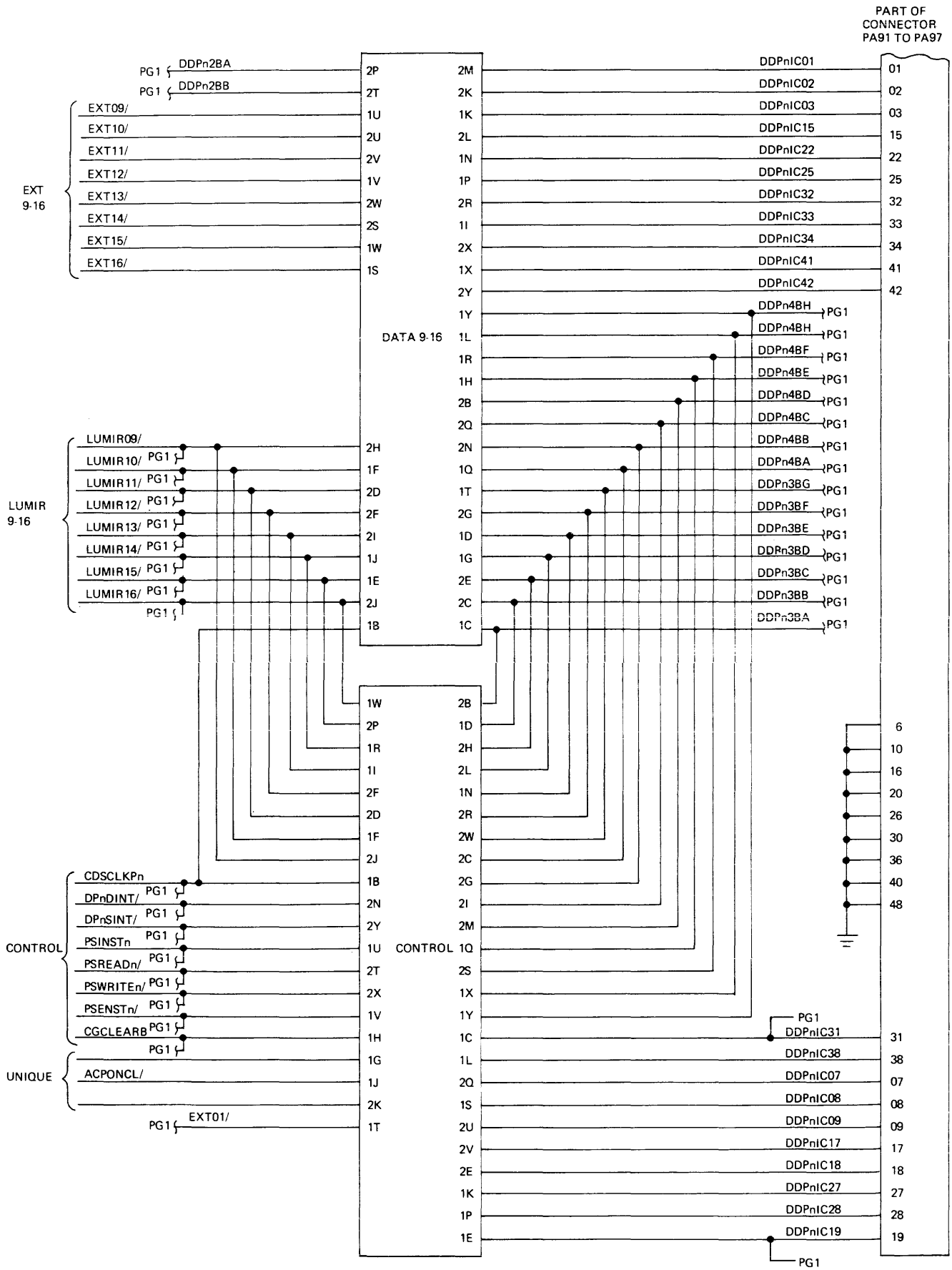


Fig. V-6 STANDARD IOC/DDP INTERCONNECTION DIAGRAM
(SHEET 2 OF 2)

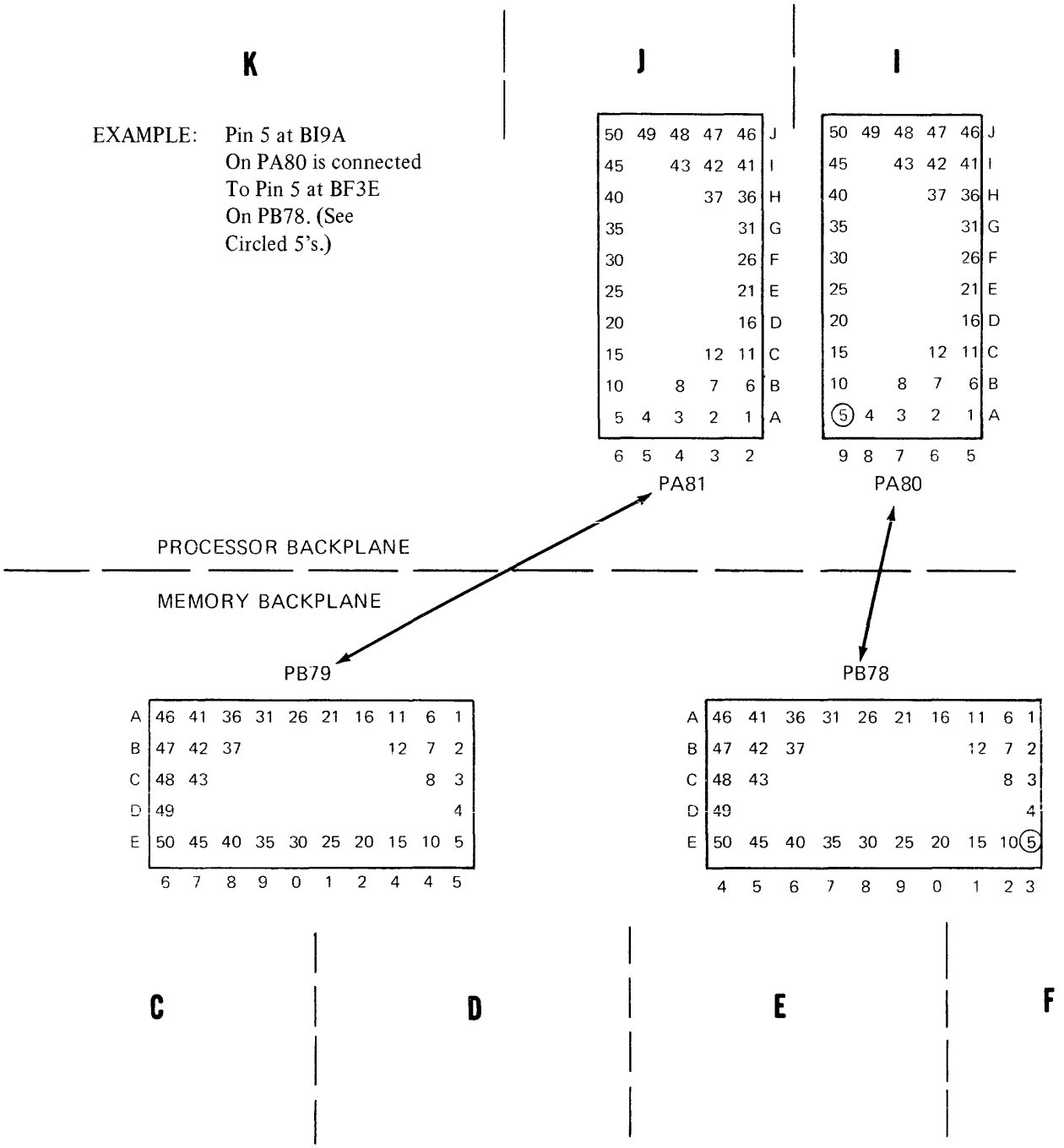


Fig. V-7 PROCESSOR-TO-MEMORY LOGIC CONNECTOR CROSS REFERENCE

SPECIAL MAINTENANCE AIDS AND TOOLS

The following is a list of the part numbers of the special maintenance aids and tools supplied for maintenance of the B700 processors:

1. Maintenance Test Routines
2. FE cards (Page 1):
   a. FE 1 (1447 5099).
   b. FE 2 (1447 5115).
   c. FE 3 (1447 5735).
   d. FE 4 (1448 8431).
3. Processor Card Extender Kit (1448 7102):
   a. Card Extender (1447 9026).
   b. Extender Cable (1447 7822).
4. Memory Card Extenders:
   a. MEXT. 1 (2538 2417) (used with memory control board and X-Y address board).
   b. MEXT. 2 (2538 2425) (used with memory digit board).
5. Tools:
   a. IC Insertion/Extraction Tool (1622 4206).
   b. IC Extraction Tool (1622 2689).
   c. Backplane Unwrap Tool (1622 5823).
   d. Backplane Wrap Tool (1622 3760)
   e. Connector Pin Extractor (1622 5401 or AMP 16-20 Type 11).
   f. Card Puller (1622 5468).
6. MTR meter (Page 16).

MAINTENANCE TEST ROUTINES

The approach used in detecting, diagnosing, and repairing failures in a B700 Processor is to run the appropriate Maintenance Test Routines (MTR's) and then replace or repair defective circuit chips or discrete components in accordance with the diagnostic information obtained from the MTR's. Additional manual diagnostic operations, using the technical manuals, FT&R documentation, and test equipment may be required by the Field Engineer to further diagnose and repair failures if the MTR's do not locate the defective component/circuit.

The MTR's are identified by a ten-digit ID number, or eight-digit part number, and a release date punched on the trailing end of each tape.

The ten-digit ID number is broken down into five groups:

Type	Plant Source	Machine Area	MTR Tape No.	Revision Level
X	XX	X_1X_2	XXX	XX
(a)	(b)	(c)	(d)	(e)

(a) All MTR tapes will use 4 for type (B700 Systems).

(b) Thirty (30) will designate the B700 plant source.

(c) The machine area is assigned as follows:

X_1	X_2	
0	0	Memory Loaders
0	1	Basic Processor
0	2	Data Memory
0	3	Disk
0	4	Operators Consoles
0	5	96 Column Equipment
0	6	Line Printer
0	7	80 Column Equipment
0	8	Paper Tape Equipment
0	9	Mag Tape Equipment (incl. Cassette)
1	0	Data Comm Equipment
1	1	Reader/Sorter
1	2	Utilities (MTR)
1	3	Undefined
1	4	Undefined
1	5	Undefined

(d) The MTR tape number is assigned sequentially beginning with 000 for each new machine.

(e) Revision levels are assigned sequentially beginning with 00 for first release and 01 for first revision.

Each MTR is provided with an Operator Instructions document (listing) which includes the MTR program listing, operating instructions, failure dictionary, and other relevant data, as applicable. Tables V-3 and V-4 list the MTR's for the B711 and B771 Systems, respectively.

A complete set of MTR documents is also contained in the B711 MTR Technical Manual, form 1066115. Figure V-8 is a flow diagram of the sequence of MTR implementation and failure diagnosis. Note that the memory, processor, and console MTR's must be implemented in the sequence indicated. One or more IOC/DDP MTR's may be run in any sequence, as required, after the memory, processor, and console MTR's have been run without failure indications.

TABLE V-3. B711 MAINTENANCE TEST ROUTINES (MTR'S)

MTR NAME	PROGRAM/TEST TAPE PART NUMBER	OPERATOR INSTRUCTIONS	REMARKS
FEMT	–	1448 6906	Memory of 8 K-words maximum
MEMLDR	1448 8506 and 1448 8514	1448 8498	Memory Loader
PROC	1448 6948	1448 6815	Processor MTR'S
BSW	1448 6955	1448 6823	Processor MTR'S
MCU	1448 6963	1448 6831	Processor MTR'S
CONS	1448 6997	1448 6864	B9343 Console and DDP (IOC)
CON96	1449 0940	1448 0866	96 Char Console
DPM	1448 6971	1448 6849	Memory up to 24 K-words
* * * I/O MTR'S (RUN AS REQUIRED) * * *			
DISK	1448 6989	1448 6856	A9480-x and DDP
RP96	1448 7003 and 1448 7961	1448 6880	A9419-x and DDP
PMTR	2602 9678	2602 9660	A988 and DDP
PMTR	2602 9678	2602 9660	A9249 and DDP
PMTR	2602 9678	2602 9660	A9247 and DDP
CR80	1448 7011 and 1448 7524	1448 6898	A9114 and DDP
TRDR	1449 0924 and 1448 7037	1449 0841	A9122 and DDP
TPNCH	1449 0932	1449 0858	A9222 and DDP
TC	1449 0916	1449 0833	A9490-25 and DDP
TM	1449 0874	1449 0791	A9491-2 and DDP

TABLE V-4 B771 MAINTENANCE TEST ROUTINES (MTR'S)

MTR NAME	PROGRAM/TEST TAPE PART NUMBER	OPERATOR INSTRUCTIONS	REMARKS
FEMT	–	1448 6906F	Memory of 8 K-words maximum
CMLDR	2601 4043	2601 4035	Memory loader
PROC	1448 6948	1448 6815C	Processor
BSW	1448 6955	1448 6823C	
MCU	1448 6963	1448 6831D	
SPO	1449 0908	1449 0825	
DPM	1448 6971	1448 6849B	Memory, data
* * * I/O MTR'S (RUN AS REQUIRED) * * *			
DISK	1448 6989	1448 6856C	A9481 and DDP
PMTR	2602 9678	2602 9660	A9249 and DDP A9247 and DDP
CR9115	2601 4274 and 2601 7608	2601 4266	A/B9115 and DDP
TC	1449 0916	1449 0833B	Tape Cassette
RP96	1448 7003 and 1448 7961	1448 6880B	
SLC	2601 4068	2601 4050	Data Comm

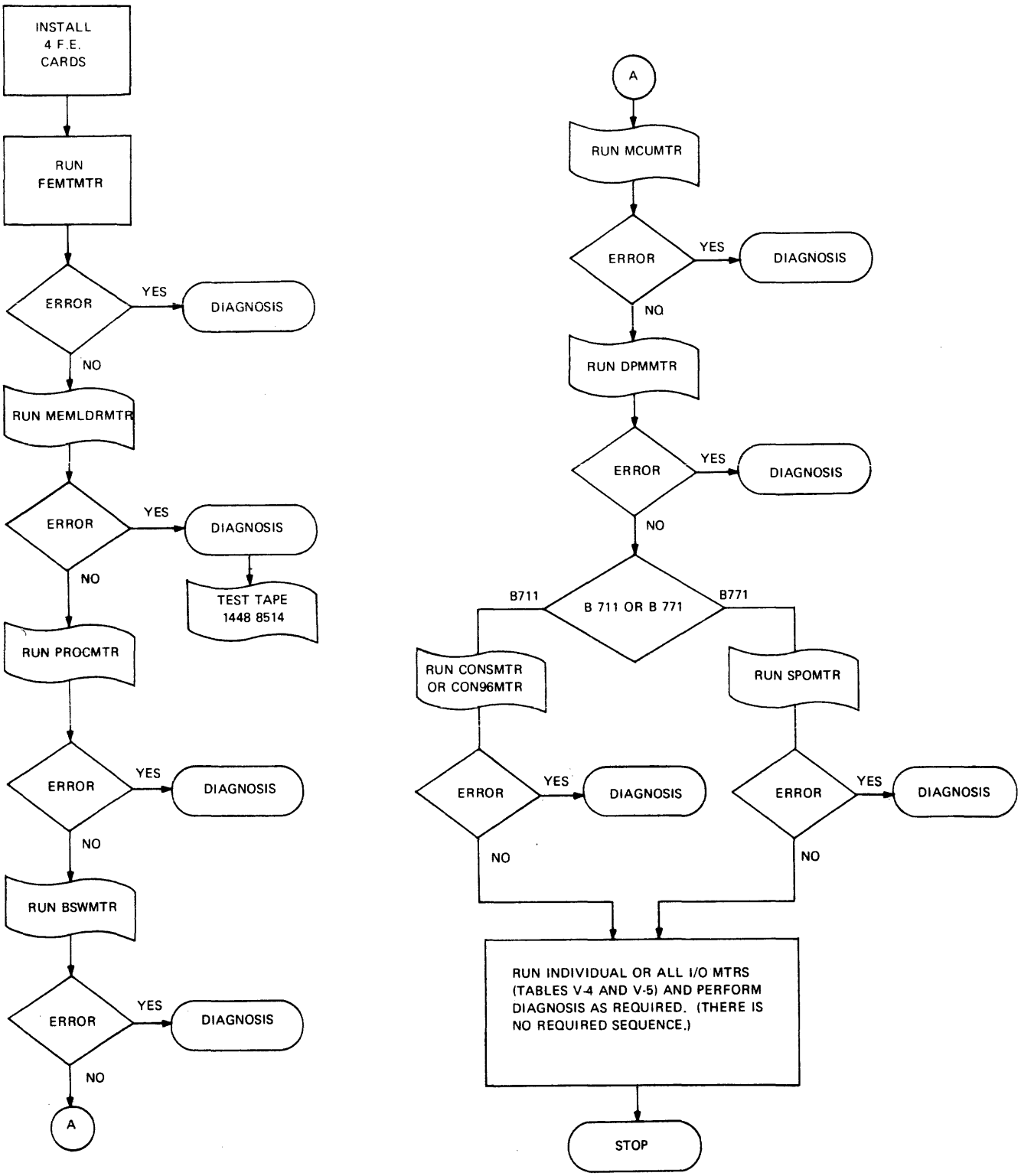


Fig. V-8 SEQUENCE OF MTR IMPLEMENTATION AND DIAGNOSTIC FLOW

B700
PROCESSOR

(INCLUDES B 705/711 AND B 771)

SECTION
VI

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

INSTALLATION
PROCEDURES

Printed in U. S. America 9-16-74

For Form 1064482

Installation Procedures

INTRODUCTION

The installation data and procedures contained in this section are applicable, to the most extent, only to the B705/711 or B771 Central/Terminal Processing Unit. Because the CPU/TPU comprises the major elements of a B711 or B771 System, some of this information covers system-level aspects. However, the B700 Planning and Installation manual (form 1061223) and the field engineering technical manuals for the various I/O controls (IOC's/DDP's) should be used in conjunction with this technical manual to ensure that all unit and system installation aspects are covered. To install a CPU/TPU, follow the installation guide in form 1061223 while referring to the applicable details in the following paragraphs of this section. Refer to the system-level data (such as system configurations/floor layouts, system/unit power requirements and connections, system cabling, and turnon/checkout procedures) in form 1061223.

Before proceeding with the installation of the CPU/TPU, the Optional Features section (VIII) of this manual and the IOC technical manuals should be consulted to gain familiarization with the options and variations of the units. Also refer to the Options section (IV) of the Planning and Installatiom manual, form 1061223.

All applicable decals may be installed as each task is completed, or after the entire installation is completed.

EQUIPMENT CONFIGURATIONS AND CHARACTERISTICS

The configuration of a system using the B705/711 or B771 processor depends on customer application and capacity requirements. The basic B711 system consists of a B705 or B711 Central Processing Unit (CPU) with the following:

a. Main-memory capacity of up to 48 K-bytes.
b. B9343 Console and Console Control.
c. B9480 Disk Cartridge Drive.
d. B489 Disk Cartridge Drive Control.

The basic B771 System consists of a B771 Terminal Processing Unit (TPU) with the following:

a. Main-memory capacity of up to 48 K-bytes.
b. B9344 SPO
c. B044 SPO Control
d. B9115/9116 80-Column Card Reader
e. B0115 Card Reader Control
f. B0351 Single-Line Control

Table I-1 lists the full complement of peripheral units, I/O controls (IOC's or DDP's), and options available for B711 and B771 installations.

B705/B711/B771 CPU/TPU CHARACTERISTICS

Dimensions:	Width	22 in. (56 cm.)
	Depth	30 in. (76 cm.)
	Height	44 in. (112 cm.)
Weight:	450 lb. (203 kg.) DOM, 475 lb. (215 kg.) INT	
Clearances:	Front	24 in. (61 cm.)
	Rear	12 in. (30.4 cm.)
	Left side	None
	Right side	None
Service Access:	24 in. (61 cm.)	all sides
Power and Heat:	Frequency	60 or 50 Hz ±1%
	Voltages	120/240 vac, 120/208 vac +5, -10% (DOM) 100 vac to 240 vac +5, -10% (INT)
	KVA	5.4 max.
	Watts	4900 max. (DOM), 5500 max. (INT)
	Circuit breaker L1	30 amps
	Circuit breaker L2	30 amps
	Power cord	15 ft., 3-wire ground (DOM) 15 ft., 2-wire ground (INT)
	Power plug	50 amp, 9452 Hubbell (DOM) Local requirements for INT
	Power receptacle	50 amp, 9450 Hubbell or equiv. (DOM) Local requirements for INT
	BTU/HR	5720 @ 60 Hz 6230 @ 50 Hz
	CFM	100

B705/B711/B771 CPU/TPU CHARACTERISTICS (CONTD.)

Operating Environment:	Temperature	60° to 100° (15.5° to 37.8° C)
	Relative humidity	10 to 80% without condensation
	Barometric pressure	20 to 32 inches of Mercury

NOTE: Raw water humidifiers may not be used. Anti-static wax on vinyl floors or computer carpeting is recommended to avoid static discharge.

I/O CONTROLS & DDP LOCATIONS							LIMIT REGISTER SETTING	MEMORY MODULES		
1	2	3	4	5	6	7		1	2	3
								16K BYTES		

Fig. VI-1 CONFIGURATION DECAL

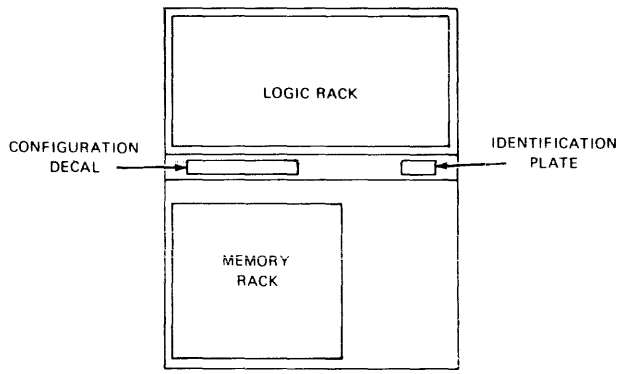


Fig. VI-2 LOCATION OF CONFIGURATION DECAL

CONFIGURATION DECAL

The configuration decal aids the Field Engineer in identifying the actual configuration of the system installed. This decal contains seven spaces for I/O controls (IOC's or DDP's), a space for the memory limit register setting, and three spaces for the memory module sizes. Figures VI-1 and VI-2 show the layout and cabinet location, respectively, of the configuration decal.

I/O Control (DDP) Locations

Figure VI-3 shows the entry contents of each IOC/DDP configuration decal and lists the style, name, and part number of each available IOC/DDP. Figure VI-4 shows a typical IOC/DDP configuration, as identified by the configuration decal.

AVAILABLE I/O CONTROLS (DDP'S)

Style No.	Name	Part No.
B0111	A9114 80 Col. CR	1448 0347
B0245	A988 Line Printer	1448 0404
B0311	A9419-2 96 Col. R/P/P	1448 0321
B0489	A9490-2 Disk	1448 0313
B0121	A9122 PPT/EPC Reader	1448 9181
B0392	A9490-2 Mag. Tape Cassette	1448 8654
B0243	A9249 Line Printer	1448 0338
B0244	A9247 Line Printer	1448 0362
B0221	A9222 PPT/EPC Punch	1449 0296
B0115	B9115/9116 Card Reader	1449 4876
B0391	A9491-2 Mag. Tape Unit	1448 2228
B0418-2	B9418-2 R/P/R	1448 0321
B044	B9344 SPO	1449 4884
B0351	Single Line Control	1449 5709

Fig. VI-3 I/O CONTROL DECAL AND IOC (DDP) LISTING

I/O CONTROLS & DDP LOCATIONS						
1	2	3	4	5	6	7
B0111 80 COL CR 1448 0347 BM1001-38				B0245 PRINTER 1448 0404 BM1001-38	B0311 96 COL 1448 0321 BM1001-38	B0489 DISK 1448 0313 BM1001-38

Fig. VI-4 TYPICAL I/O CONTROL CONFIGURATION DECAL

NFPA Type II Decals

When installing the A9114 Card Reader, A9122 Paper Tape Reader, or A9222 Paper Tape Punch in a B711 System, the "NFPA Type II" decal (1088 6836) supplied with the corresponding I/O control (DDP) must be affixed to the processor as follows:

1. For the A9114, affix decal to left of ID plate (Figure VI-2).
2. For the A9122 or A9222, remove the UL decal (482A) and replace it with the NFPA Type II decal (in the same location).
   See Figure VI-3 for a listing of the corresponding I/O controls.

Memory Address Limit Address Setting

As shown in Figure VI-1, a space is allocated on the configuration decal for entering the setting of the maximum addressable DPM (data/program memory) location. (Refer to Section VIII, Optional Features.)

Memory Modules

Three spaces are allocated on the configuration decal for identifying the memory module configuration. The following types of memory modules are available:

Style No.	Name	Part No.
B0011-1	8K bytes	1672 6390
B0011-2	16K bytes	1672 6382

Figure VI-5 shows the memory module decal entries and the actual decal for the B0011-2, which is the standard memory module used in the system.

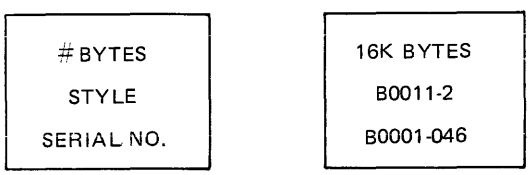


Fig. VI-5 MEMORY DECAL

MEMORY MODULE AND PROCESSOR CARD CONFIGURATIONS

Figure VI-6 shows the configuration of memory module printed circuit cards. It should be noted that, when a 4K-word (8K-byte) core stack module is used, it must be in the next unused module location after the last 8 K-word module location. (Refer to Section VIII.)

Figure VI-7 shows the configuration of printed circuit cards in the B705/B711 Processor foreplane. Figure VI-8 shows the card configuration for the B771 processor. The frontplane locations, card names, and card part numbers are identified in Figures VI-7 and VI-8.

Note that, in the B705/B711 CPU, cards CC6 (1448 0743) and CC7 (1447 4472) are used for a 64-character console, while cards CC6K (1448 7813) and CC7K (1448 8365) are used for a 94-character console.

I/O CONTROL (IOC/DDP) CONFIGURATIONS

The CPU/TPU has eight locations in which the cards comprising the various I/O controls (IOC's or DDP's) are installed. Locations DDP1 through DDP7 (Figures VI-7 and VI-8) are interchangeable locations which may accommodate any of the standard (up to four cards each) IOC's as determined by the I/O service priority assignments. (Refer to Section VIII.) Location DDP8 is always used for either the console IOC in the B705/711 or the SPO IOC in the B771. In the B771, the eight-card Single-Line Control is installed in locations DDP7A and DDP7B or DDP6A and DDP6B. (See Figure VI-8.) The B0115 Card Reader Control is normally allocated location DDP1 in the B771.

After the I/O service priority assignments have been established, install the IOC cards in the corresponding locations shown in Figures VI-7 and VI-8.

When the various IOC cards are installed in the backplane connectors, addtional interconnections must be made, as required, by installing standard frontplane connectors (1534-3940) on the frontplane pins of adjacent IOC cards. (A description of the frontplane connector is provided in Section V.)

Table VI-1 is a cross-reference chart that lists the identifiers (such as DC1 and DC2) and part numbers of the various IOC cards, the card function to identifier relationship, and the required frontplane connections. See Figures VI-7 and VI-8 for the corresponding backplane location of each card function (control, data 9-16, data 1-8, and special, right-to-left). Refer to Section III of the B700 Planning and Installation manuals for additional IOC/DDP configuration details.

CONFIGURATION CARD

The Configuration Card (CON-1, in backplane location DK-5) provides functional configuration information to the system. This card must be wired during installation in accordance with Table VI-2 and the specific site configuration.

Configuration wiring is accomplished by solder connections between the designated "common" terminals and the appropriate ZERO or ONE terminal on the plug-in socket headers provided for the CON-1 card.

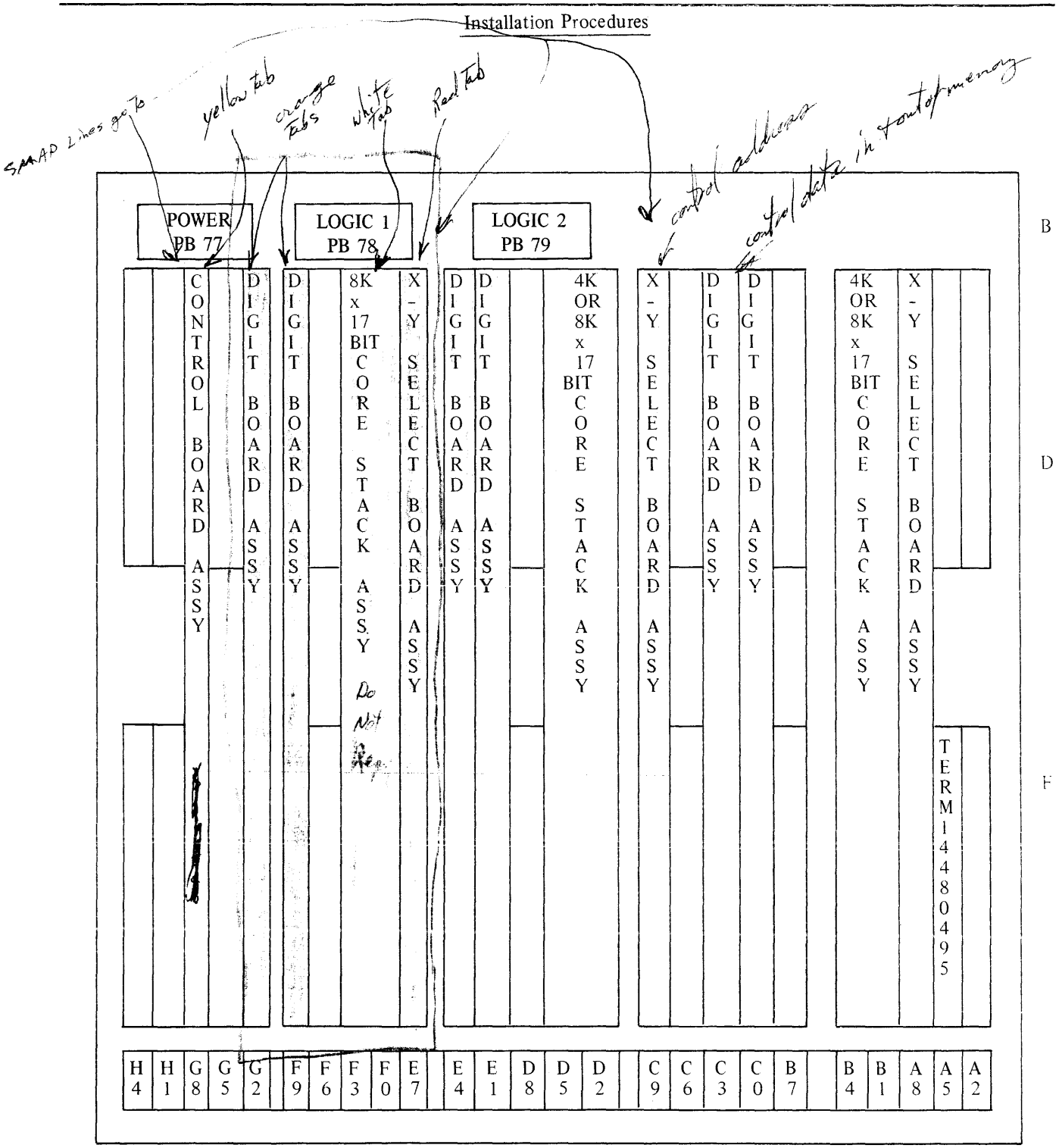


Fig. VI-6 MEMORY PRINTED CIRCUIT CARD LOCATION

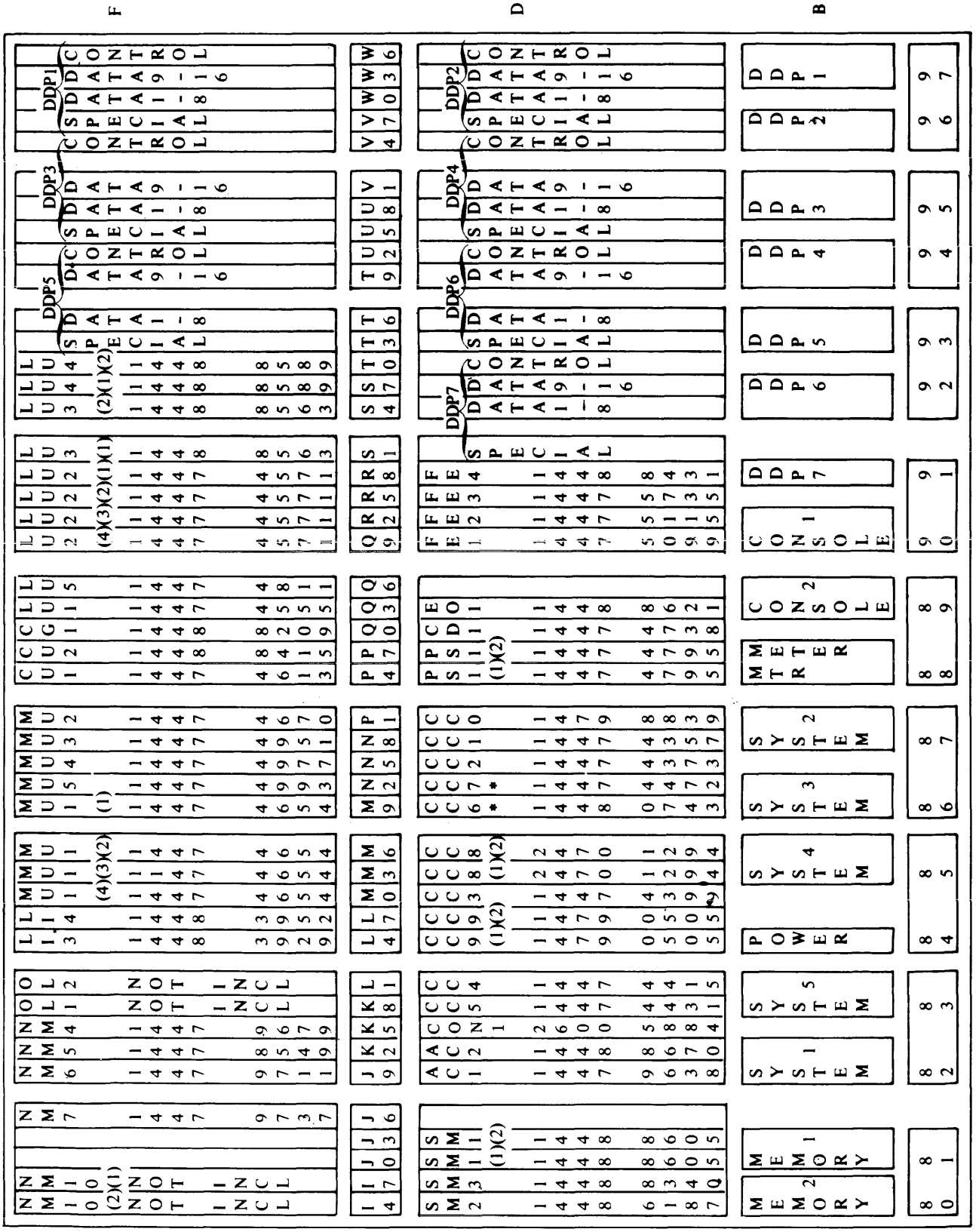


Fig. VI-7 B705/B711 CENTRAL PROCESSING UNIT (CPU), PRINTED CIRCUIT CARD LOCATIONS

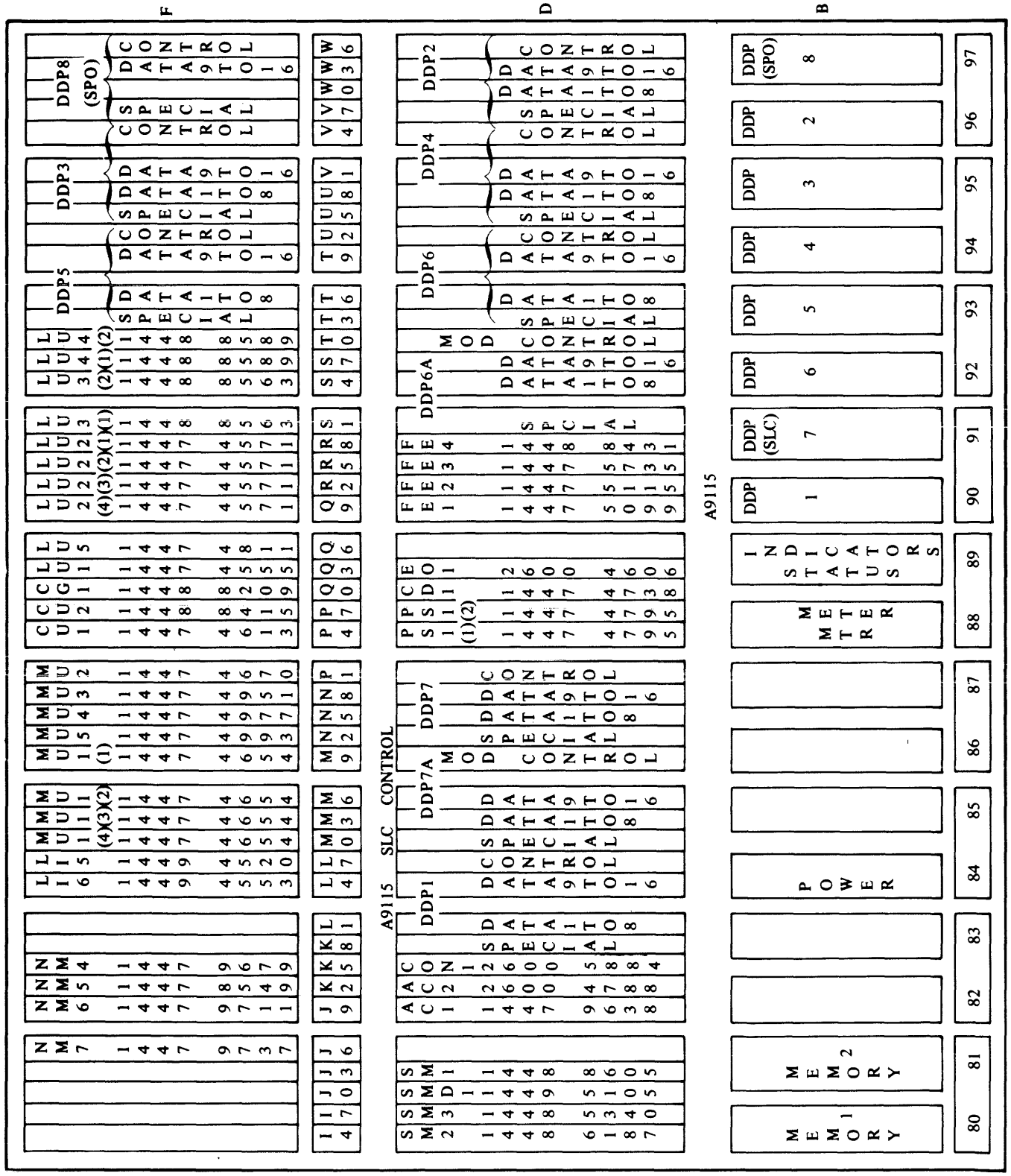


Fig. VI-8. B771 TERMINAL PROCESSING UNIT, PRINTED CIRCUIT CARD LOCATIONS

TABLE VI-1 I/O CONTROL (IOC/DDP) FUNCTION LOCATION AND FRONTPLANE CONNECTION CROSS REFERENCE

Control IOC/DDP)	Device	Card Functions/Identifiers				Frontplane Connections
		Control	Data 9-16	Data 1-8	Special	
B0489	A9480 Disk Drive	DC1 (1447 4530)	DC2 (1447 4498)	DC3 (1447 4514)	DC4 (1447 8507)	DC1 to DC2 and DC3 to DC4
B0311	A9419, 96-Col. RDR/PRT/PNCH	RC1 (1448 8241)	RC2 (1447 5214)	RC3 (1448 8290)	RC4 (1448 8324)	RC1 to RC2 and RC3 to RC4
B0111	A9114 80-Col. Card Reader	CR1 (1447 8747)	CR2 (1447 5719)	CR3 (1447 7509)	CR4 (1448 8233)	CR1 to CR2 and CR3 to CR4
B0243	A9249 Line Printer	PO1 (1447 9744)	PO2 (1447 9810)	PO3 (1447 9844)	–	PO2 to PO3
B0244	A9247 Line Printer	PT1 (1448 0016)	PT2 (1448 0032)	PT3 (1448 0057)	PT4 (1448 0073)	PT1 to PT2 and PT3 to PT4
B0245	A988 Line Printer	–	PP2 (1447 9950)	PP3 (1447 9976)	PP4 (1447 9992)	PP3 to PP4
B0391	A9491-2 Magnetic Tape Unit	TM1 (1447 9877)	TM2 (1447 9893)	TM3 (1447 9919)	TM4 (1447 9935)	TM1 to TM2 and TM3 to TM4
B0392	A9490-25 Magnetic Tape Cassette	TC1 (1448 9108)	TC2 (1448 9132)	TC3 (1448 9074)	TC4 (1449 0312)	TC1 to TC2 and TC3 to TC4
B0121	A9122 Paper Tape Reader	TPR1 (1449 0460)	TPR2 (1449 0494)	–	–	None
B0221	A9222 Paper Tape Punch	TPP1 (1449 0346)	TPP2 (1449 0379)	TPP3 (1449 0403)	TPP4 (1449 0437	TPP1 to TPP2 and TPP3 to TPP4
B044	B9344 SPO	SPO1 (1449 2458)	SPO2 (1449 2482)	–	SPO4 (1449 2516)	SPO1 to SPO2
B0115	B9115 or B9116 Card Reader	CRT1 (1449 5139)	CRT2 (1449 5162)	CRT3 (1449 5196)	CRT4 (1449 5220)	CRT1 to CRT2 and CRT3 to CRT4
B0351	Single Line Control (Data Comm)	SLC1 (1449 4348) SLC5 (1449 4462)	SLC2 (1449 4371) SLC6 (1449 3225)	SLC3 (1449 4405) SLC7 (1449 4496)	SLC4 (1449 4439) SLC8 (1449 3191)	SLC1 to SLC2, SLC4 to SLC5, and SLC6 to SLC7

Table VI-2 CONFIGURATION CARD (CON-1) OPTION WIRING

EXT BIT	DEFINITION	COMMON	FOR ZERO	FOR ONE
1	*	B7-5	B7-11	B7-10
2	*	B7-6	B7-9	B7-8
3	*	B7-12	B7-3	B7-4
4	*	B7-13	B7-1	B7-2
5	*	B5-5	B5-11	B5-10
6	*	B5-6	B5-9	B5-8
7	*	B5-12	B5-3	B5-4
8	*	B5-13	B5-1	B5-2
9	*	E5-5	E5-11	E5-10
10	*	E5-6	E5-9	E5-8
11	*	E5-12	E5-3	E5-4
12	0 = DIL** 1 = NO DIL	E5-13	E5-1	E5-2
13	0 = RPG 1 = NO RPG	E7-5	E7-11	E7-9
14	0 = B711 1 = B771	E7-6	E7-9	E7-8
15	0 = FULL DISK (TWO DRIVES) 1 = ½ DISK (ONE DRIVE) OR NO DISK	E7-12	E7-3	E7-4
16	0 = CONSOLE 1 = SPO	E7-13	E7-1	E7-2

* RESERVED EXT BIT-WIRE TO ZERO ONLY

** DIL IS DOWNINGTOWN IMPLEMENTATION LANGUAGE.

CPU/TPU POWER REQUIREMENTS

AC POWER DISTRIBUTION TO PERIPHERAL UNITS

Peripheral units that have separate power cords are connected to convenience outlets in the central power distribution box located in the central/terminal processor unit (CPU/TPU) cabinet. The number or combinations of peripheral units powered from this source must be limited to maintain the maximum CPU/TPU input current within the prescribed limit. Table VI-3 lists the primary power sources that can be used for the systems. Table VI-4 lists the maximum allowable steady-state line current for each source.

POWER DISTRIBUTION BOX WIRING

AC power is distributed within the CPU/TPU as follows:

a. Line A of the CPU/TPU power cord is distributed to a 20-amp Hubbell twist lock receptacle, or two standard receptacle outlets. These receptacles are mounted horizontally in the power distribution box. Line A receptacles must be used for the A988 or A9247 Line Printers. If the A988 or A9247 Line Printers are not used, other peripherals may be connected to line A receptacles. Table VI-5 shows the maximum current, for both the B711 and B771, that can be loaded on line A receptacles.

b. Line B of the CPU/TPU power cord is distributed to four standard two-wire, plus ground, receptacles which are mounted vertically in the power distribution box. These receptacles are used for peripheral devices other than the A988 and A9247 Line Printers.

c. Line B of the CPU/TPU power cord is also distributed internally to the connectors that are used for the following peripherals:
   1. A9114 80-Column Card Reader.
   2. A9122 Paper Tape Reader.
   3. A9222 Paper Tape Punch.

TABLE VI-3

PRIME POWER SOURCES

VOLTAGE (+5, -10%)	FREQUENCY (+ -1%)	PHASE
Domestic		
120/208V	60 Hz	Single Phase, 3 Wire & Gnd
120/240V	60 Hz	Single Phase, 3 Wire & Gnd
International		
100V		
110V		
115V		
120V	50 or 60 Hz	Single Phase, 2 Wire & Gnd
127V		
200V		
208V		
220V		
230V		
240V		

TABLE VI-4

VOLTAGE	CURRENT	
	60 Hz	50 Hz
120/208V	25A	N/A
120/240V	25A	N/A
100V	60A	65A
110V	55A	60A
115V	53A	58A
120V	50A	55A
127V	48A	53A
200V	30A	32A
208V	29A	31A
220V	28A	30A
230V	27A	29A
240V	25A	27A

TABLE VI-5

MAXIMUM CURRENT AVAILABLE FROM PROCESSOR POWER RECEPTACLES

LINE CONNECTION		100V	110V	115V	120V	127V	200V	208V	220V	230V	240V
A (J3)	B711	20.4	18.5	17.7	17.0	16.1	10.2	9.8	9.3	8.9	8.5
	B771	22.8	20.7	19.8	19.0	17.9	10.4	10.9	10.3	9.9	9.5
B	B711	20.1	18.2	17.2	16.7	15.8	10.0	9.7	9.1	8.7	8.3
(J1/J2)	B771	22.2	20.2*	19.3	18.5	17.5	11.1	10.6	10.1	9.6	9.2

* Limited to 15 amps for systems installed in Canada.

The maximum current available for peripheral devices on line B is shown in Table VI-5. Table VI-6 shows the maximum current load of each peripheral device. If the processor input current being drawn by the peripherals on lines A and B is the maximum allowed, then any additional peripherals must obtain power from a branch circuit other than the CPU/TPU branch circuit. All branch circuits, including the CPU/TPU branch circuit, should be protected by circuit breakers suitable for motor load application.

TABLE VI-6

CURRENT REQUIREMENT FOR PERIPHERAL DEVICES

SYSTEM	EQUIPMENT		100V	110V	115V	120V	127V	200V	208V	220V	230V	240V
711	A988	Line Printer	17.6	16.0	15.2	14.7	13.9	8.8	8.5	8.0	7.7	7.3
711/771	A9247	Line Printer	17.6	16.0	15.2	14.7	13.9	8.8	8.5	8.0	7.7	7.3
711/771	A9480-2	Disk Cartridge Drive	6.0	5.5	5.2	5.0	4.7	3.0	2.9	2.7	2.6	2.5
711/771	A9249	Line Printer	4.8	4.4	4.2	4.0	3.8	2.4	2.3	2.2	2.1	2.0
711	A9419-2	96-Col. Card Reader/ Punch/Data Recorder	3.2	3.0	2.8	2.7	2.5	1.6	1.6	1.5	1.4	1.4
711	A9114	80-Col. Card Reader	1.8	1.7	1.6	1.5	1.4	0.9	0.9	0.8	0.8	0.7
711	A9222	Paper Tape Punch	0.8	0.8	0.7	0.7	0.7	0.4	0.4	0.4	0.4	0.4
711	A9122	Paper Tape Reader	0.6	0.6	0.5	0.5	0.5	0.3	0.3	0.3	0.3	0.3
771	B9115	80-Col. Card Reader	2.9	2.6	2.5	2.4	2.3	1.5	1.4	1.3	1.3	1.2
771	B9344	SPO	6.0	5.4	5.2	5.0	4.8	3.0	2.9	2.7	2.6	2.5

GROUNDING REQUIREMENTS

The following grounding requirements apply to the installation of B711 or B771 System units:

a. An insulated grounding conductor must be installed as part of the branch circuit that supplies the unit or system. (This conductor should be identical in size and insulation to the grounded and ungrounded branch-circuit conductors, except that it is green, or green with one or more yellow stripes.)

b. The grounding conductor mentioned in item (a) must be used as the ground connector for all units.

c. The attachment-plug receptacles in the vicinity of the unit or system all must be of the grounding type, and the grounding conductors serving these receptacles must be connected to the grounding conductor that serves the unit or system.

WARNING

Improper grounding creates a potentially hazardous situation for the serviceman and operator. All units in the system have a grounding type power plug, and the power receptacles in the CPU/TPU have the ground terminal securely connected to the CPU/TPU frame. This method ensures a positive ground connection through the main power cord to building ground.

The equipment grounds for all units in the system must be connected to a common point. This requirement is met when all peripheral units receive power from the CPU power distribution box.

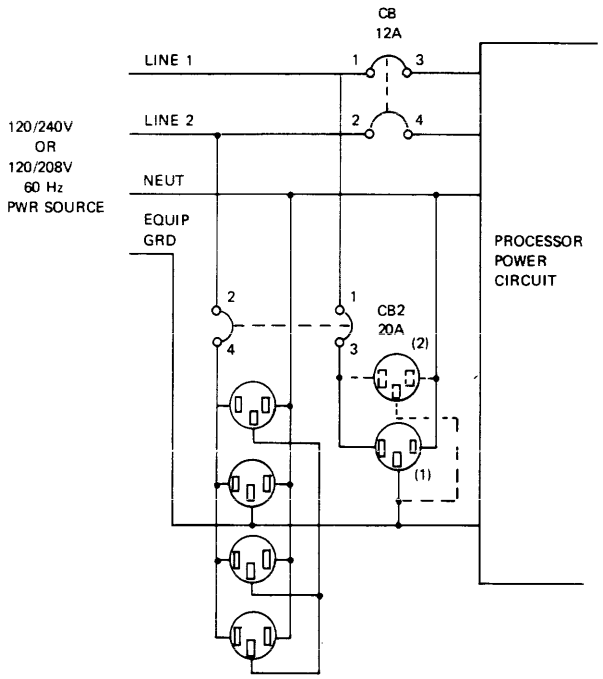
Measurements of leakage to ground established that the A9480 Disk, because of its filter capacitor network, causes system leakage currents in excess of 5 milliamperes. The warnings given above are thus required by UL Standard 478. There are also warning labels on the power control cover in the CPU/TPU and on the A9490 Disk.

The equipment ground for all units in the B711/B771 System must be tied to a common point. This requirement is met when peripherals receive power from the processor power outlet box.

If a separate branch circuit is used for any peripheral, the grounding wires of all such branches must be tied together at a common point at the power distribution panel. A single ground wire should then connect from the panel to the service ground or building ground. Conduit may not be used in place of a grounding conductor wire.

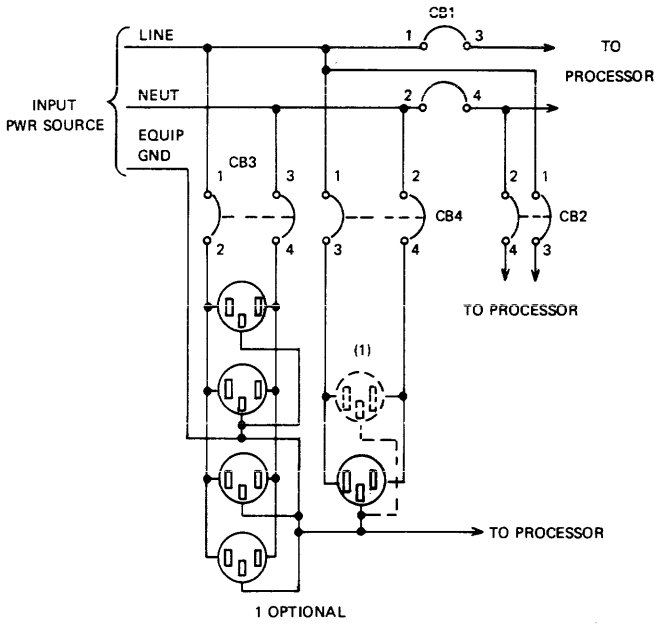
Figure VI-9, Domestic Input Power, shows the wiring of the input power to the processor and the convenience receptacles. Figure VI-10 shows the wiring for international applications.

Installation Procedures



NOTE: (1) SPECIAL RECEPTACLE FOR A988 POWER PLUG
HUBBELL 3330G
(2) OPTIONAL

Fig. VI-9 DOMESTIC INPUT POWER

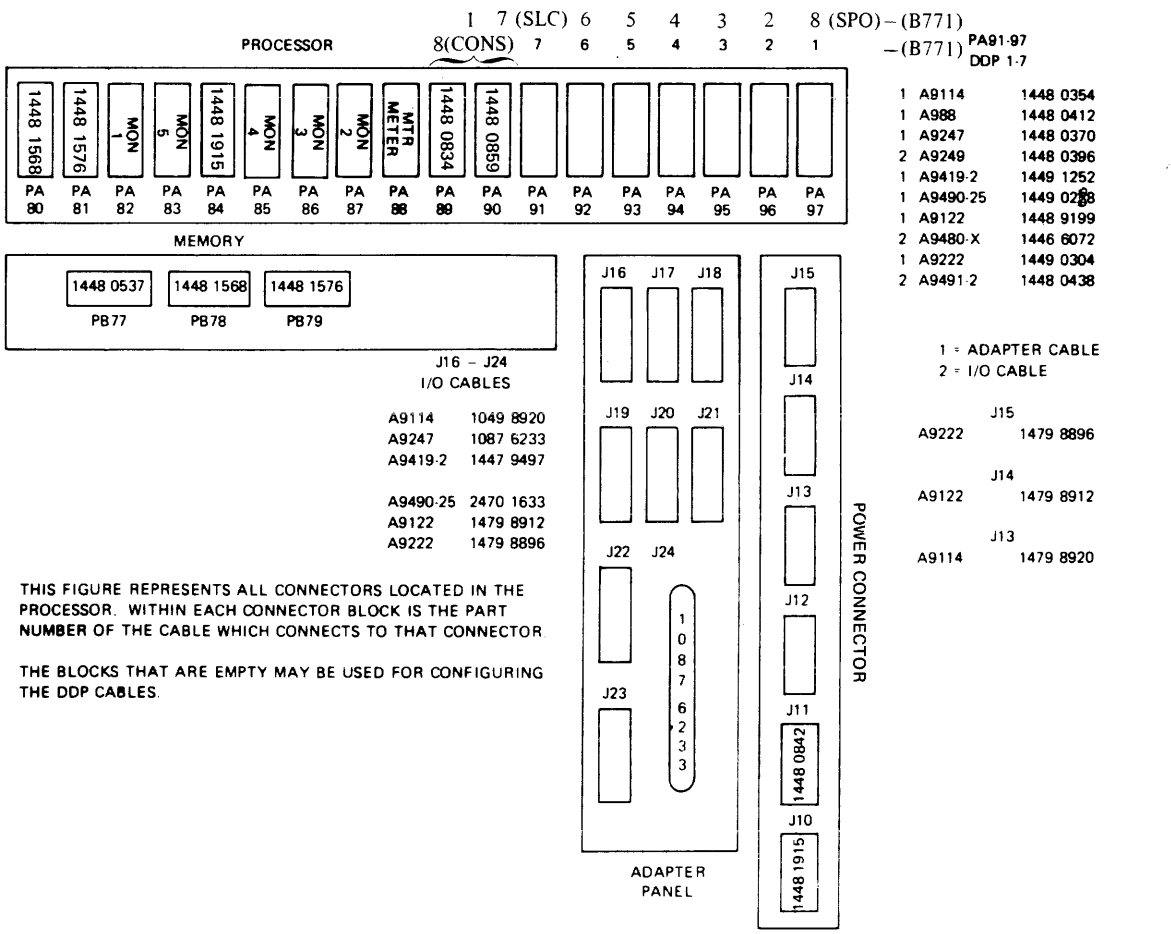


CB RATINGS

	100-127V 60 Hz	200-240V 60 Hz	100-127V 50 Hz	200-240V 50 Hz
CB1	15 AMPS	8 AMPS	15 AMPS	8 AMPS
CB2	15 AMPS	8 AMPS	15 AMPS	8 AMPS
CB3	20 AMPS	12 AMPS	20 AMPS	12 AMPS
CB4	20 AMPS	12 AMPS	20 AMPS	12 AMPS

Fig. VI-10 INTERNATIONAL INPUT POWER

IOC/DDP LOCATIONS



J16 – J24
I/O CABLES

A9114	1049 8920
A9247	1087 6233
A9419-2	1447 9497
A9490-25	2470 1633
A9122	1479 8912
A9222	1479 8896

THIS FIGURE REPRESENTS ALL CONNECTORS LOCATED IN THE PROCESSOR. WITHIN EACH CONNECTOR BLOCK IS THE PART NUMBER OF THE CABLE WHICH CONNECTS TO THAT CONNECTOR.

THE BLOCKS THAT ARE EMPTY MAY BE USED FOR CONFIGURING THE DDP CABLES.

Fig. VI-11 CPU/TPU PROCESSOR, MEMORY AND I/O CABLE CONNECTOR LOCATIONS

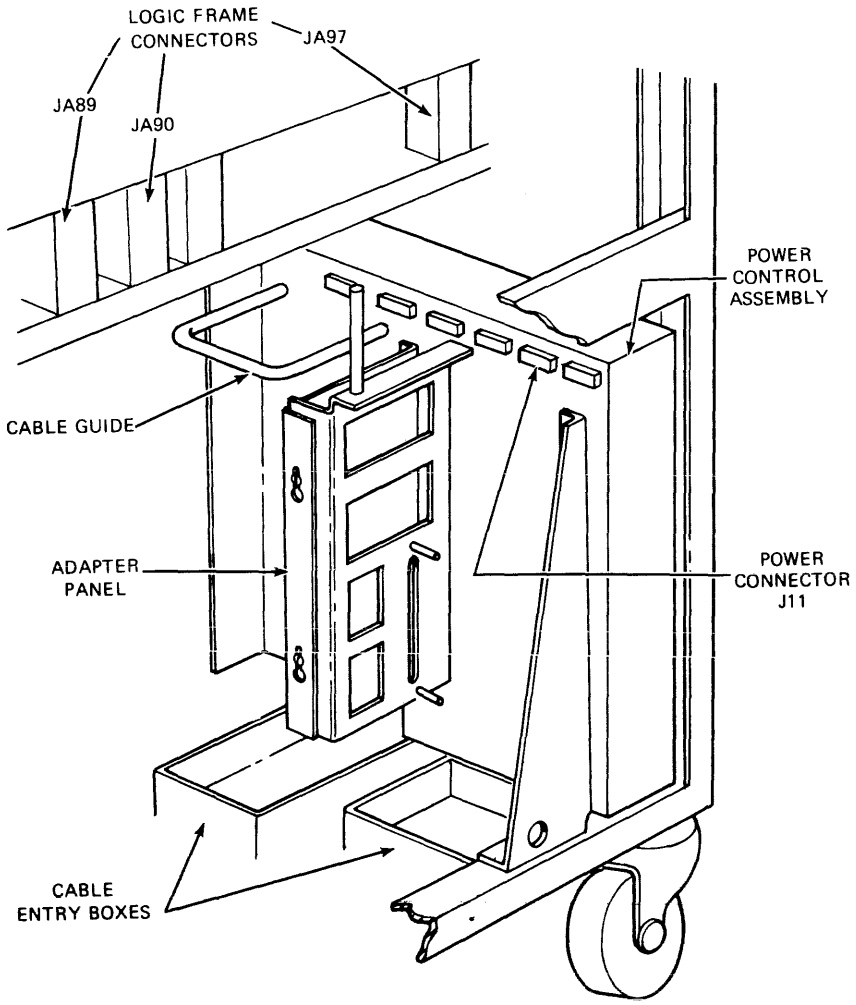


Fig. VI-12. PROCESSOR CABINET CABLE ENTRANCE AND CONNECTION FACILITIES

CABLE CONNECTIONS

After the primary AC input power wiring is completed (but **not** turned on), internal and external cables should be connected in the sequence indicated in the following paragraphs. Refer to the B700 Planning and Installation Manual, form 1061223, Sections III and IV, for detailed installation and option data regarding the configuration of I/O, adapter, and power cables and their connections. Also refer to the installation sections of the technical manuals supplied for each I/O control (IOC or DDP). Figure VI-11 identifies the cable connector locations. Figure VI-12 shows the locations of the connectors, panels, entry ports, and general layout of the rear section of the cabinet.

INTERNAL CPU/TPU CABLING

The four internal cables supplied with the CPU/TPU should be installed before any I/O or peripheral power connections are made. These four cables are connected as shown in Table VI-7. (See Figure VI-11.)

TABLE VI-7 INTERNAL CPU/TPU CABLE CONNECTIONS

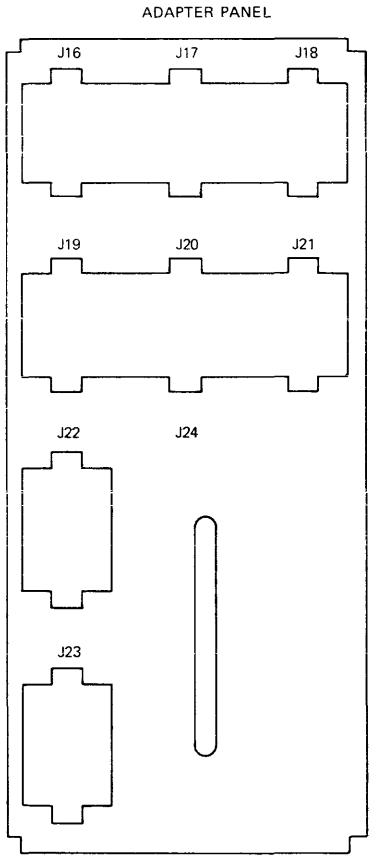
Cable Part No.	Connection	
	From	To
1448 1568	Processor connector PAJ80	Memory connector PBJ78
1448 1576	Processor connector PAJ81	Memory connector PBJ79
1448 1915	Processor connector PAJ84	Power supply connector J10
1448 0537	Processor power supply	Memory connector PBJ77

I/O ADAPTER CABLING

Many of the I/O controls (IOC's or DDP's) are supplied with adapter cables that interconnect the respective I/O card location backplane connectors (PAJ91 through PAJ97) with the interfacing peripheral device through connector blocks J16 through J24 on the adapter panel. (See Figure VI-13.) These cables are installed when each set of IOC cards is installed in the priority-allocated locations of the CPU/TPU foreplane. For some I/O interfaces, an adapter cable has a connection to one of the power supply connector blocks (J13, J14, or J15) located above the adapter panel. (See Figures VI-11 and VI-12.)

Table VI-8 lists the I/O adapter cables provided for specific IOC and device interfaces through the adapter panel. Corresponding CPU/TPU backplane connectors, power connectors, and adapter panel connectors are also shown. Note (Figure VI-11) the different IOC/DDP location to PA connection allocation for the B711 and B771.

An adapter panel decal is provided to record the adapter panel connections after they are established. (See Figure VI-14.) After the adapter cables are installed, record the style and part number of the peripheral device connected to each connector, as shown for J24 in Figure VI-14. The decal is normally affixed to the power distribution chassis panel adjacent to the adapter panel.



J16 through J23: I/O end of adapter cable.

J24: I/O end of adapter cable used for A9247 line printer.

J15: Power Connector for A9222.

J14: Power Connector for A9122.

J13: Power Connector for A9114.

J10, 11, 12: Used for internal BX Processor.

Fig. VI-13 I/O ADAPTER PANEL AND POWER CABLE CONNECTOR LOCATIONS

ADAPTER PANEL CONNECTOR ASSIGNMENTS	
CONN.	CONTROL/PERIPHERAL
J16	
J17	
J18	
J19	
J20	
J21	
J22	
J23	
J24	B0244 FOR A9247 PRINTER

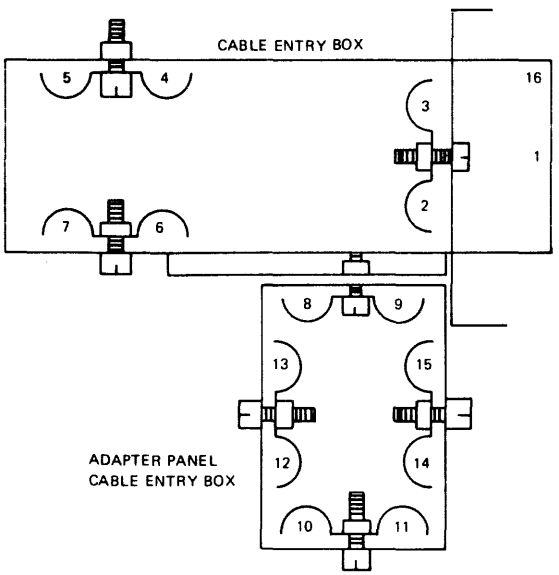
Fig. VI-14. ADAPTER PANEL CONNECTION DECAL

TABLE VI-8 I/O ADAPTER CABLES (B711/B771)

Interface		Adapter Cable Part No.	Adapter Panel Connector*	CPU/TPU and Power Connector**
Peripheral	IOC/DDP			
A9114-1 Card Reader	B0111	1448 0354	J16-J23	J-91-J97, J13
A9419-2 RD/Pnch/Rec	B0311	1449 1252	J16-J23	J91-J97
A988 Line Printer	B0245	1448 0412	J16-J23	J91-J97
A/B9247-X Line Printer	B0244	1448 0370	J24	J91-J97
A/B9490-25 Mag. Tape Cass.	B0392	1449 0288	J16-J23	J91-J97
A9122-1 Paper Tape RDR	B0121	1448 9199	J16-J23	J91-J97, J14
A9222-1 Paper Tape Pnch	B0221	1449 0304	J16-J23	J91-J97, J15
B9115/9116 Card Reader	B0115	1449 4892	J16-J23	J91-J97
B9418-2 Rdr/Pnch/Rcdr	B0311/ 418-2	1449 1252	J16-J23	J91-J97
A9491-2 Mag. Tape Unit	B0391	1448 0438	J16-J23	J91-J97

* Connect to **one** connector (J16 through J23), as determined by IOC/DDP location assignment.

** Connect to **one** connector (J91 through J97), as determined by IOC/DDP location assignment.



(1) A988 LINE PRINTER POWER CORD
(2) A988 LINE PRINTER I/O CABLE
(3) A9245 LINE PRINTER I/O CABLE
(4) A9480-11, 12 DISK I/O CABLE
(5-7) B9343 CONSOLE I/O CABLES
(*8-15) I/O CABLES FOR ROUTING TO ADAPTER PANEL
(16) POWER CORDS OF DEVICES TO CONVENIENCE OUTLETS
(*10) IS USED FOR THE A9247 LINE PRINTER, IF USED

Fig. VI-15 CABLE ENTRY BOXES AND RECOMMENDED ROUTING SEQUENCE

PERIPHERAL DEVICE I/O AND POWER CABLING

All I/O and power cables for peripheral devices are routed under the rear of the CPU/TPU cabinet and up through the two cable entry boxes shown in Figures VI-12 and VI-15. The smaller cable entry box is used for most of the device cables interfaced with the IOC/DDP's through the adapter panel. The larger cable entry box is used for power cords and those I/O cables connected directly to the IOC/DDP processor backplane connectors (PAJ91 through PAJ97).

In Figure VI-15, numbers keyed to a legend show the recommended sequence of routing the I/O and power cables. This typical sequence is recommended on the basis of cable size and weight and the accessibility of cable clamps and routing areas.

TABLE VI-9 PERIPHERAL DEVICE I/O AND POWER CABLES

Peripheral Device	Cable Part No. (See Notes.)	CPU/TPU Connection (Note 4)
A/B9480-xx Disk Cartridge Drive	1446 6072 (1)	PAJ91-PAJ97
B9343-x Console (Three cables; B711 only)	1448 0834 (2) 1448 0859 (2) 1448 0842 (2)	PAJ89 PAJ90 J11 (power supply)
A9114-1 Card Reader	1479 8920 (1)	J16-J23 and J13 (power supply)
A9419-2 RD/PNCH/RCDR	1447 9497 (3) or two ea. 2471 3059 (1)	J16-J23
A988 Line Printer	1065 3079 (1)	J16-J23
A/B9247-x Line Printer	1087 6233 (1)	J16-J23
A/B9249-x Line Printer	2106 3524 (1) or 1448 0396 (1)	PAJ91-PAJ97
A/B9490-25 Mag. Tape Cass.	2046 2990 (1)	J16-J23
A9122 Paper Tape Reader	1479 8912 (1)	J16-J23
A9222-1 Paper Tape Punch	1479 8896 (1)	J16-J23
B9344 SPO	1449 4918 (3)	PAJ97 (B771 only)
B9115/9116 Card Reader	2471 3059 (1)	J16-J23
B9418-2 RDR/PNCH/RCDR	Two ea. 2471 3059 (1)	J16-J23
A9491-2 Mag. Tape Unit	1448 0438 (3)	J16-J23

NOTES: (1) Cable is supplied with peripheral device.
(2) Cable is supplied with CPU/TPU.
(3) Cable is supplied with IOC/DDP.
(4) Connect to specific connector listed, or to **one** of the PAJ91 through PAJ97 connectors on the CPU/TPU backplane, or to **one** of the J16 through J23 connectors on the adapter panel.

Table VI-9 lists the peripheral device I/O and power cables that are routed through the entry boxes to either the adapter panel connector blocks (J16 through J24) or directly to the processor IOC/DDP connectors (PAJ90 through PAJ97). Note that a cable may be supplied with the CPU/TPU, the device, or the device IOC/DDP.

INSTALLATION CHECKOUT

After all installation and cabling tasks have been completed for the CPU/TPU, the CPU/TPU should be turned on and checked out on both a unit and system basis. Refer to Section III of the B700 Planning and Installation Manual, form 1061223, for complete instructions.

B700

PROCESSOR

(INCLUDES B 705/B711 AND B 771)

SECTION

VIII

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

OPTIONAL
FEATURES

Printed in U. S. America 9-16-74

For Form 1064482

DEVICE DEPENDENT PORT (I/O CONTROL) CONFIGURATION

The device dependent ports (DDP's) or I/O controls (IOC's) are grouped into two types: standard and non-standard. Standard DDP's/IOC's are interchangeable in any of the seven four-card DDP/IOC locations (1 through 7) and consist of a maximum of four cards each.

Non-standard DDP/IOC's are not interchangeable in the DDP/IOC locations and consist of more than four cards each. That is, the non-standard DDP/IOC's are special configurations dedicated to specific DDP/IOC locations. Presently, there are three non-standard DDP/IOC's: one for the 12-card B711 System console (B9343), one for the eight-card Single Line Control (SLC), and one for the four-card B771 SPO I/O control. (Refer to Section III of the B700 Planning and Installation Manual for complete details and listings of IOC/DDP locations for both the B705/711 and B771.)

DDP/IOC PRIORITY CLASSIFICATIONS

Each DDP/IOC backplane location has an I/O service priority classification, starting with the highest priority allocated to DDP/IOC location 8. This priority allocation is in relation to the system firmward and the classification of the interfacing peripheral devices into the following three groups:

Group	Device Type	Priority
1	Character	Highest
2	Dedicated	Intermediate
3	Buffered	Lowest

Table VIII-1 lists the classifications of the various B711/B771 peripheral devices and DDP/IOC's (by model number) under the three priority groups.

Table VIII-2 shows typical example of priority configurations for both the B711 and B771 systems.

A character device requires a DDP/IOC with a minimal number of eight-bit or 16-bit buffer registers. These buffers hold data temporarily until serviced within a given time interval, dependent on the data rate of the device. This type of device has a data rate slow enough to allow the device firmware to service a minimal unit of data, generally a single character.

A dedicated device also requires only a minimal number of buffers, but has a data rate high enough to require the device firmware to remain dedicated to the device until a full record of data has been sericed.

A buffered device has a full record (card image, print line) buffer. This type of device allows the device firmware to service data within real time requirements far less demanding than either of the above. To the firmware, the buffered device is much like a character device, with the firmware appropriately controlling the character rate in loading or unloading the buffer.

TABLE VIII-1 PERIPHERAL DEVICE AND DDP/IOC PRIORITY CLASSIFICATIONS

Group 1 Highest)		Group 2 (Intermediate)		Group 3 (Lowest)	
Peripheral	DDP/IOC	Peripheral	DDP/IOC	Peripheral	DDP/IOC
B9343	B9343	A9480	B0489	A9114	B0111
B9344	B044			B9115	B0115
SLC	B0351			A9419	B0311
A9490	B0392			A988	B0245
A9491	B0391			A/B9247	B0244
A9122	B0121			A/B9249	B0243
A9222	B0221				

TABLE VIII-2. TYPICAL PERIPHERAL AND DDP/IOC PRIORITY CONFIGURATIONS

B711 System			Device Address Code	B771 System		
Peripheral	DDP/IOC	Location (priority)		Peripheral	DDP/IOCQ	Location (priority)
B9343	B9343	8	7	B9344	B044	8
A9490-25	B0392	7	6	SLC	B0351	7 or 6
A9122	B0121	6	5	–	–	–
A9222	B0221	5	4	–	–	5
A9480	B0489	4	3	–	–	4
A9249	B0243	3	2	–	–	3
A9419	B0311	2	1	B9247	B0244	2
A9114	B0111	1	0	B9115	B0115	1

PREPARING A DDP/IOC CONFIGURATION

When installing a B711 or B771 system, list all peripherals in groups as classified in Table VIII-1. Starting with Group 1 peripherals and DDP/IOC location 7, assign the DDP/IOC locations.

NOTE: DDP/IOC location always contains the B9343 console (B711) or the B9344 SPO (B711).

After Group 1 peripherals are assigned, assign the group 2 peripherals and DDP/IOC's to the next highest locations. If no Group 2 peripherals are to be configured (as in the basic B771 system) proceed with Group 1.

After Group 2 peripherals are assigned, proceed with Group 1 and assign the next highest DDP locations.

MEMORY ADDRESS LIMIT WIRING

The memory address limit may be hard-wired from 8K words to 24K words in 2K-word increments, or 16K to 48K bytes in 4K-byte increments. An address error is generated when a memory address exceeds the set limit.

The memory address limit is prewired at the factory and is indicated by a decal on the Processor frame. Whenever the memory address limit is to be increased or decreased from the prewired setting, hard-wiring changes must be made at backplane location SM2 in accordance with Table VIII-3. Record the new address limit on the decal.

TABLE VIII-3 MEMORY ADDRESS LIMIT OPTION WIRING

ADDRESS* LIMIT	BACKPLANE PINS (LOCATION SM2)**				
	DI4D	DI5F	DI5D	DI4E	DI5E
8KW (16KB)	L	L	H	H	H
10KW (20KB)	H	H	L	H	H
12KW (24KB)	L	H	L	H	H
14KW (28KB)	H	L	L	H	H
16KW (32KB)	L	L	L	H	H
18KW (36KB)	H	H	H	L	H
20KW (40KB	L	H	H	L	H
22KW (44KB)	H	L	H	L	H
24KW (48KB)	L	L	H	L	H

*KW = kilo-words; KB = kilo-bytes.

**In the pin columns, "L" indicates a wire to be connected from designated pin to ground pin, "H" indicates that backplane pin is left floating (no wire).