60475001

CONTROL DATA CORPORATION

CDC® CYBER 18 COMPUTER SYSTEMS CENTRAL PROCESSOR

AA132, AA133, AA153, DT120, FC402

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

FIELD REPAIR GUIDE

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released per ECO 19002. This manual supersedes the applicable information in publications 96768681, 96768682, and
(9/78)	96768683, which are obsolete.
B	Manual revised; includes ECO 21461, providing new equipment under test instructions.
(9/79)	
C	Manual revised; includes ECO 21548, providing new part number for the FDD controller.
(9/79)	
D	Manual revised; includes ECO 21667, providing new printed wiring assembly part number and micro-memory switch settings.
(9/79)	
E	Manual revised; includes ECO 21813, providing new product information.
(1/80)	
F	Manual revised; includes ECO DS022009, providing CC628 display terminal information.
(10/80)	
G	Manual revised; includes ECO DS022083, providing miscellaneous changes.
(5/81)	
H	Manual revised; includes ECO DS022090, providing a new ac line filter.
(6/81)	
J	Manual revised; includes ECO DS022127, providing a new MOS memory interface address printed wiring assembly.
(12/81)	
K	Manual revised; includes ECO DS022172, providing a new MOS memory interface data printed wiring assembly.
(5/82)	
L	Manual revised; includes ECO DSO22187, providing a new MOS memory interface address printed wiring assembly,
(9/82)	addition of the FCC tested/compliance warning label and minor corrections.
M	Manual revised; includes ECO DS022206, providing clarification of the dual-processor backplane memory interface
(11/82)	cabling connections.
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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
AA132-A	12		
AA132-B	11		
AA132-C	11		
AA132-D	04		
AA133-A	19		
AA133-B	14		
AA153-A	07		
DT120-A	01		
FC402-A	02		

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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viii	M
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6-20	D
6-21	A
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6-23	D
6-24	G
6-25	F
6-26	E
6-27 thru 6-34	A
6-35	G
6-36	A
6-37	E
6-38 thru 6-41	A
6-42	G
6-43 thru 6-46	A
6-47	D
6-48	A
6-49	A
6-50	E
6-51 thru 6-54	A
6-55	E
6-56 thru 6-61	A
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PREFACE

This manual provides general maintenance information for the Control Data® CYBER 18 Computer Systems. This manual supports maintenance of equipments AA132-A/B/C/D, AA133-A/B, AA153-A and CYBER 18 systems containing processor equipments AA113 and AA109 with power supply equipments GD122-B and XA148-A. This document is applicable to systems consisting of not less than a minimum configuration (metal-oxide semiconductor (MOS) processor, tape cassette or flexible disk drive, and console display).

This manual contains information and procedures to aid maintenance personnel in performing onsite maintenance tasks on the basic processor equipment only. The subsystems contained in the computer system are supported by individual subsystem manuals. The maintenance approach of these manuals is to isolate faults by using the diagnostic decision logic tables (DDLTs) and to make repairs by using the corrective action procedures. Corrective action is accomplished by exchanging replaceable subassemblies rather than replacing components. When repair cannot be accomplished by exchanging subassemblies, a support customer engineer and additional documentation is required.

Refer to the following publications for further information regarding the CYBER 18 Computer Systems and subsystems.

Publication	Publication Number
722-10 (CC628-A/B) Display Terminal Hardware Maintenance Manual	62940003
AA132, AA133, AA153, GH447, GH461 CYBER 18 Equipment Cabinets Hardware Reference/Maintenance Manual	96768280
AT241, AT275, BA212, DT223 MOS Memory and Interface Hardware Maintenance Manual	96768600
AT314, AU115, BU272, CW218 I/O Expansion Subsystem Hardware Reference/Maintenance Manual	60475540
BA209-A, BA210-A, BA210-B, BS158-A 512-, 2048-, and 8192-Instruction Micro Memory Hardware Maintenance Manual	96767900
Basic Micro-Programmable Processor Hardware Maintenance Manual	39451400
BJ402, BJ701, BZ403, FA727, GB138, GB145 Module Drive Subsystem Field Repair Guide	60475051
BR704, FA111, FA750 Cartridge Disk Drive Subsystem Hardware Maintenance Manual	60475052
BR803, GD130, GD308, FA730 Flexible Disk Drive Subsystem Hardware Maintenance Manual	60475010
BW101, BW303, BW812, FA107 Magnetic Tape Transport (NRZI) Subsystem Field Repair Guide	60475041
BW305, DZ101, FA464, FA465 Magnetic Tape Transport (NRZI/PE) Dual Mode Subsystem Field Repair Guide	60475042
CA150, CA153, CA154, CC555, CC628, CT104, FC109, FC539, FJ441, FJ442 Terminal Equipment Subsystem Field Repair Guide	60475070
CB104, FC109, FC539, FH301 Card Reader Subsystem Field Repair Guide	60475031
CC614 Console Display Subsystem Field Repair Guide	60475021
CC555, CC628 Keyboard Display Terminal Subsystem Field Repair Guide	60475022

Publication	Publication Number
CL408, CL411, FC109, FC539, FH301 Line Printer Subsystem (Drum) Field Repair Guide	60475032
CT103, CT105, CT106, FC109, FC539, FH301 Line Printer Subsystem (Band) Field Repair Guide	60475033
CYBER 18 Computer Systems Overview Manual	60475000
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360
CYBER 18 Processor with MOS Memory (Macro Level) Hardware Reference Manual	96768300
DT120, DT195, FC402 Breakpoint Controller and Breakpoint Panel Hardware Maintenance Manual	96729000
DT610-A, DY221-A, FJ127-A, FJ128-A Buffered Communication Line Adapter Subsystem Field Repair Guide	60475130
DU137, DY192, DY198, GH447, GH461 Communication Multiplexer Subsystem Field Repair Guide	60475080
FA104, BE602 Tape Cassette Subsystem Hardware Maintenance Manual	60475060
FJ129-A, FJ448-A, FV678-A/B Synchronous Data Link Control Communication Line Adapter Subsystem Field Repair Guide	60475140
FV679, FV701 Auto Restart Loader Subsystem Field Repair Guide	60475120
Operational Diagnostic System (ODS) Version 2 Reference Manual	96768410

WARNING

This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference with radio communications. It has been tested to comply with the limits for Class A peripheral computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

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FIGURES

TABLES

The CYBER 18 Computer Systems are general-purpose systems that utilize micro- and micro-programmable central processing units (referred to in this manual as processors) and a variety of peripheral subsystems. The central processor(s) may be housed in either a single-processor equipment cabinet or a dual-processor cabinet. Single-processor configurations are designated by equipment numbers AA132-A, AA132-B (figure 1-1), or AA132-C (figure 1-2). Dual-processor configurations are designated by equipment numbers AA133-A, AA133-B or AA153-A (figure 1-4). In these equipments, the control panel, processor(s), power supplies, deadstart loading subsystem, and power distribution assembly are included in the designated equipment.

Prior to the new equipment number designations, the processor configurations were designated by the product numbers 18-10M, 18-20, 18-25 and 18-30. In these product-number-designated equipments, the cabinet with control panel, power supplies, power distribution box, and processor chassis were identified by individual equipment numbers. These configurations were furnished with power supplies manufactured either by Scott Electronics Corporation (GD122-B/XA148-A) or L. H. Research (no CDC equipment number). In the systems using the GD122-B power supplies, an additional +12 V dc power supply is included if the system contains a tape cassette subsystem; if the system contains a flexible disk drive, an additional -5 V dc power supply is included. In all equipment configurations that contain flexible disk drive subsystems, a +24 V dc power supply is furnished.

The processor is a multilevel processing unit that utilizes 16-bit macro-instruction words. It emulates the basic 1700 instruction repertoire plus an enhanced instruction set with an instruction execution time relative to a main memory cycle time of 600 nanoseconds. When used in a dual-processor configuration, it is the first processor.

The processor has the following features:

- I/O-TTY interface for teletypewriter (current mode operation) or console display (RS232-C operation)
- Internal TTL-level bus system that is functionally compatible with CDC 1700 A/Q or A/Q-DMA and NCR MO5 I/O peripheral requirements
- Auto-data transfer (ADT) operation mode
- Real-time clock interrupt facility
- Sixteen levels of micro/macro interrupt facilities to accommodate most system configurations
- Priority-oriented direct memory access (DMA) bus system

Additional expansion capabilities provide for:

- Interface to 131K words of MOS memory or 98K words of MOS memory and 98K-word error correction code MOS array modules
- Accommodation of either the 16K word MOS memory module or the 32K MOS memory module, which is expandable up to 131K words of internal MOS memory per processor or 96K words with error correction code
- Accommodation of the breakpoint panel
- Accommodation of random access micro memory up to 4K
- The backpanel of each input/output board position in the processor accepts a push-on cable connector for attaching the controller within the logic chassis to an associated peripheral device.

Input/output facilities provided by the prewired backpanel are as follows:

- 1700 A/Q or MO5 TTL-level peripheral devices (five slots)
- 1700 A/Q DMA TTL-level peripheral devices (four slots)
- Unassigned input/output board positions that provide standard input power only (one slot)

SINGLE-PROCESSOR SYSTEMS

The single-processor equipment cabinet (figures 1-1, 1-2, and 1-3) includes the table-top cabinet, control panel, power supply (±5 and ±12 V dc), flexible disk drive power supply (+24 V dc), ac power distribution, flexible disk drive (unit 0), cooling fans, and central processor.

The central processor includes the flexible disk drive controller and the following six basic processor printed wiring assemblies (PWAs):

- Status mode interrupt (SMI)
- Arithmetic logic unit (ALU)
- Control 1
- Control 2
- Transform
- I/O-TTY controller

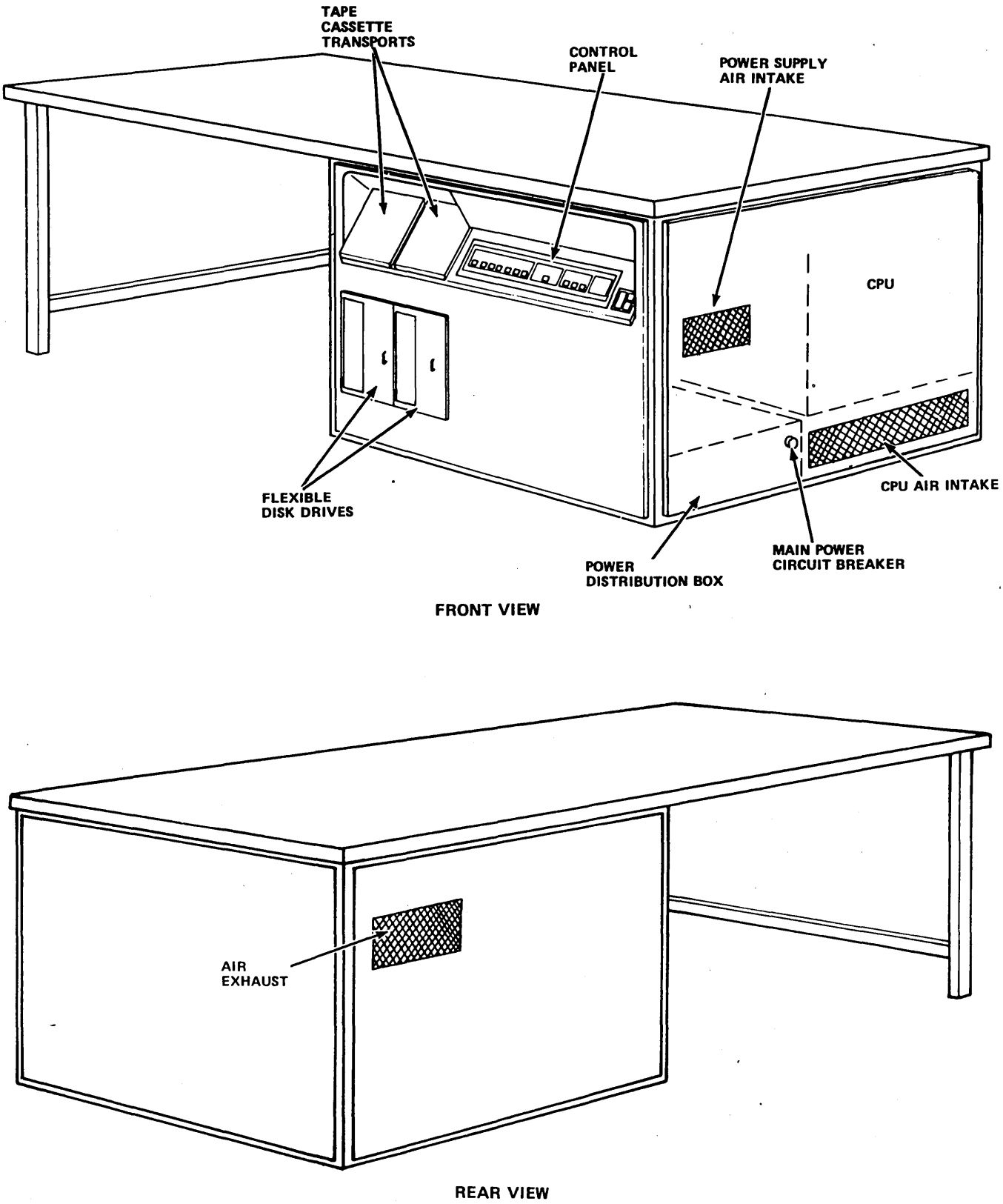
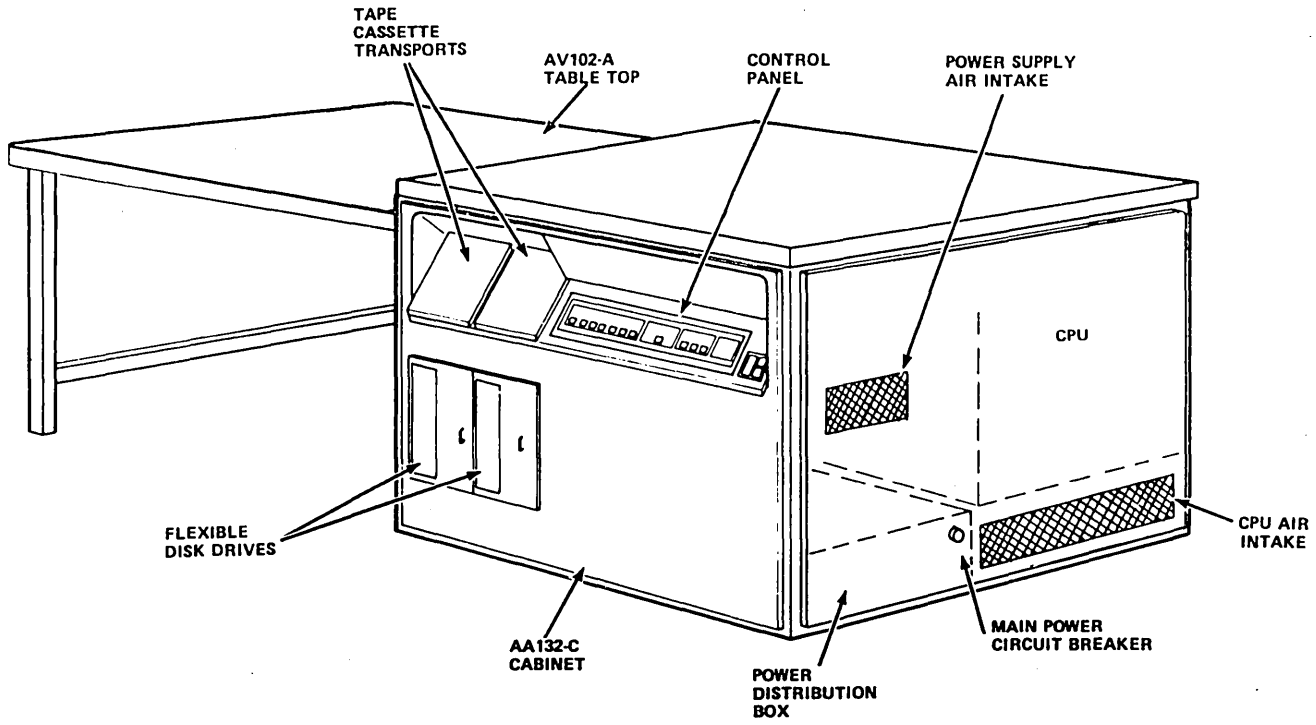
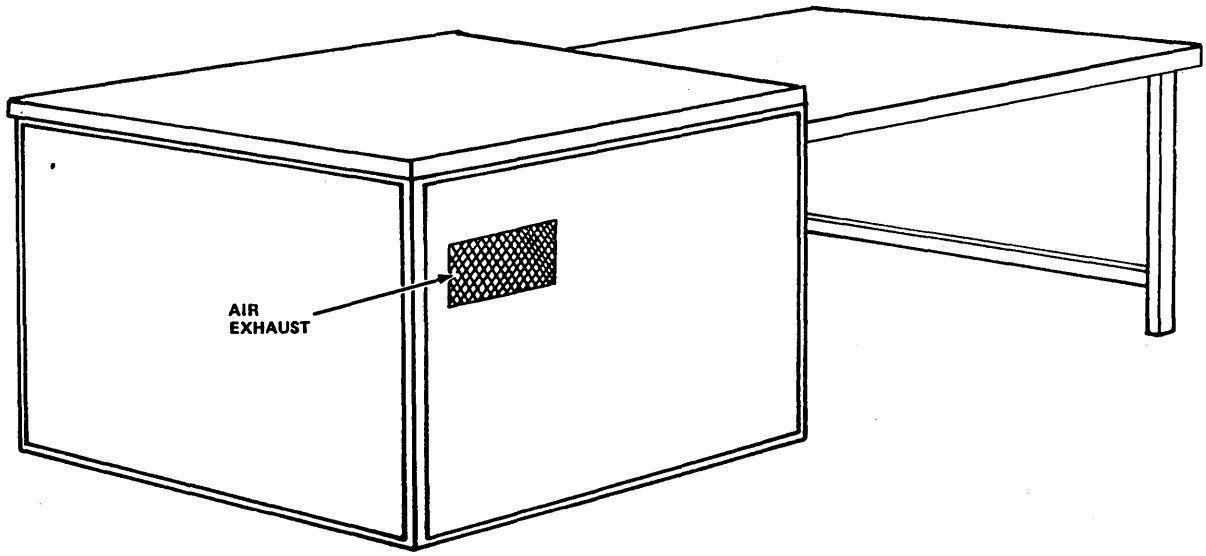


Figure 1-1. AA132-A/B Single-Processor Cabinet, Exterior Views



FRONT VIEW

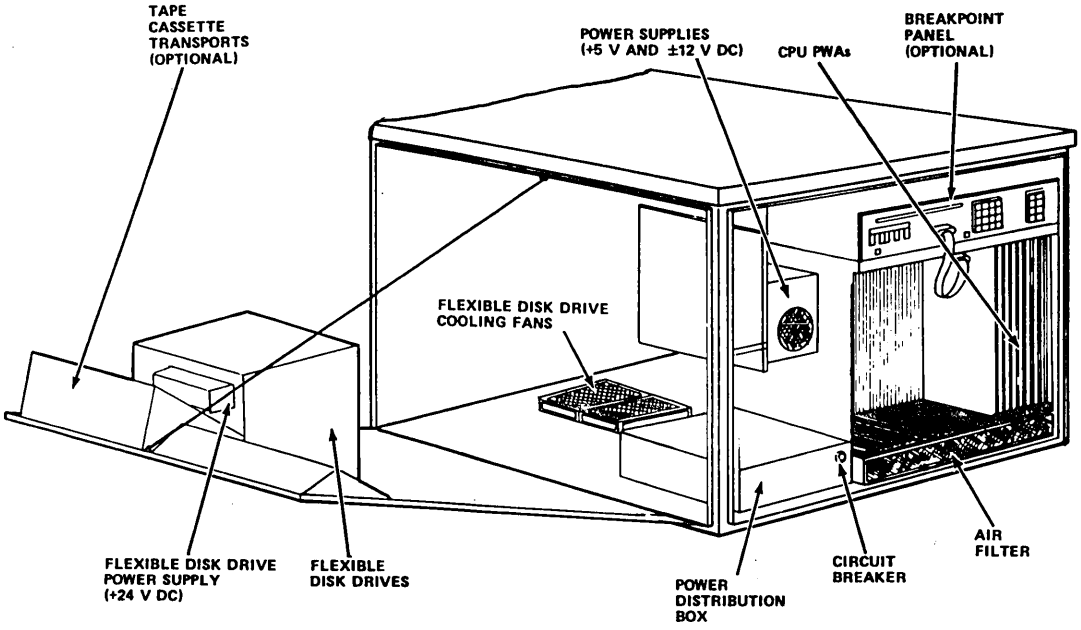


REAR VIEW

1207

Figure 1-2. AA132-C Single-Processor Cabinet, Exterior Views

FRONT VIEW



REAR VIEW

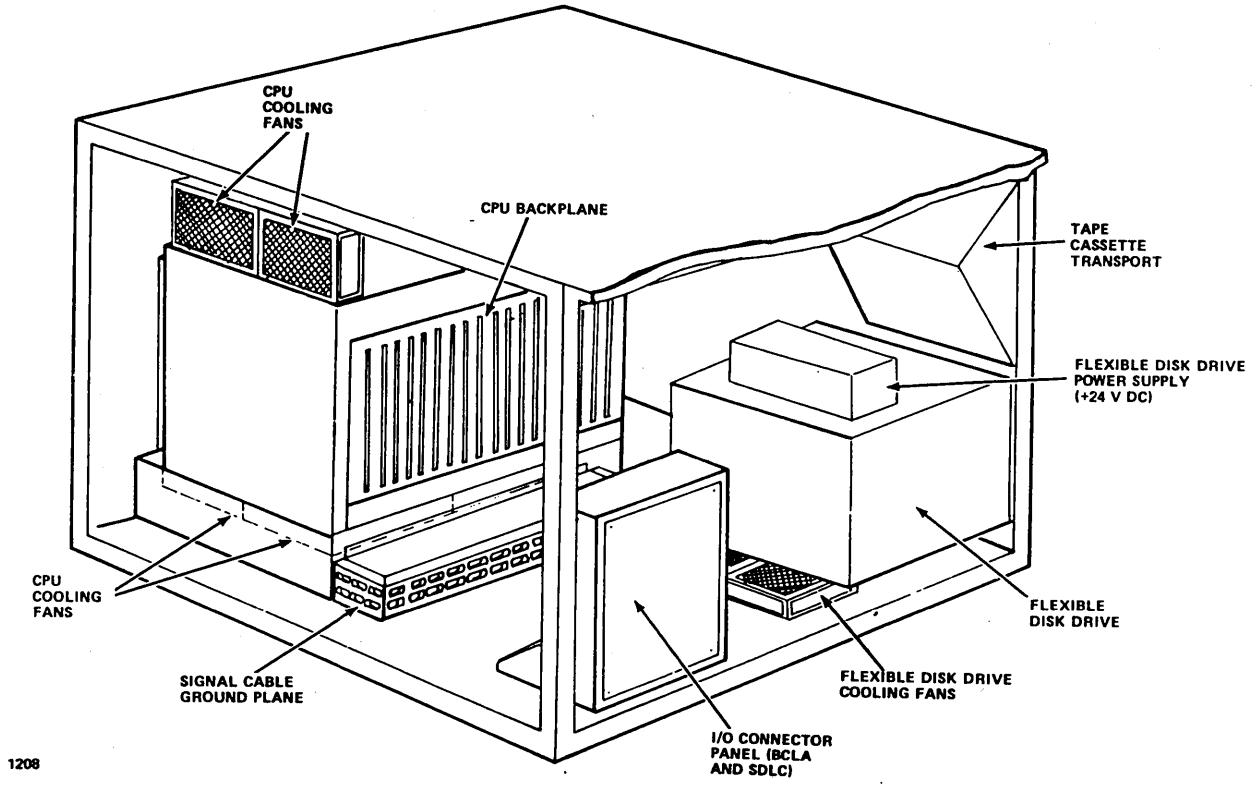


Figure 1-3. Single-Processor Cabinet Equipment Location, (Interior Views)

The processor also includes memory interface (address and data), as well as facilities for optional MOS main memory (16K to 131K words, 18-bit), micro memory (512 to 4096 words, 18-bit), and 11 peripheral controllers (five A/Q, four A/Q-DMA, one magnetic tape (NRZI), and one open for customer preference).

The basic processor with 16K words of MOS memory and a console display comprise the minimum system configuration for processor testing via the Operational Diagnostic System (ODS). The installed equipment normally operates on 120 V, 50/60 Hz input power. Where site power conditions are different, a power conversion transformer may be installed to convert 220 V, 230 V, 240 V, or 250 V ac to 120 V ac.

DUAL-PROCESSOR SYSTEMS

The dual-processor equipment cabinet (figures 1-4 and 1-5) includes the table-top cabinet, control panel, power supply (±5 and ±12 V dc), ac power distribution, cooling fans, two tape cassette transports, (or two flexible disk drives) and two processors (one timeshare processor and one communication processor with breakpoint panel†).

The timeshare processor includes the MOS memory interface (address and data), two MOS memory arrays (16K and 32K††), one micro memory (2K), and the following six basic processor printed wiring assemblies (PWAs):

- Status mode interrupt (SMI)
- Arithmetic logic unit (ALU)
- Control 1
- Control 2
- Transform
- I/O-TTY controller

The timeshare processor also includes the following peripheral controllers:

- One tape cassette controller (for cassette tape unit 0) or one flexible disk controller (for flexible disk drive unit 0)
- One magnetic tape (NRZI) controller††
- One storage module drive controller††
- One card reader/line printer controller††

The communication processor includes the six basic processor PWAs plus MOS memory interface (address and data) PWAs, two MOS memory arrays (32K each††), one micro memory (2K), and the following peripheral controllers:

- One tape cassette controller (for cassette transport unit 0) or one flexible disk controller (for flexible disk drive unit 0)
- Three multiplexer loop interface adapters (MLIA 1, 2, and 3)

Several peripheral controller slots are available for optional subsystems.

The installed equipment normally operates on 120 V, 50/60 Hz input power. Where site power conditions are different, a power conversion transformer may be installed to convert 220 V, 230 V, 240 V, or 250 V ac to 120 V ac.

The communication processor has the same features and options as the timeshare (or single) processors, except that it is the second processor in a dual-processor configuration. The communication processor shares the power distribution system and control panel with the timeshare processor.

The dual-processor configuration provides the following additional capability:

- The external ports of two MOS memory systems are directly interconnected to provide up to 262K words of common storage accessible by both processor ports and both DMA ports.
- The communication processor is installed in the cabinet opposite to the timeshare processor with interconnecting cables that are no longer than 4 feet (1.2 meters).

CONTROL PANEL

The control panel (figure 1-6) is mounted in the cabinet as illustrated in figures 1-1, 1-2, and 1-4. It contains switches and indicators that control and indicate operational conditions of the processor and selected subsystems (modem, flexible disk drive, and tape cassette). The modem switch and indicators are associated only with a dual communication line adapter when residing in slot F. The flexible disk drive and tape cassette switches and indicators are normally connected to slots D and E for the flexible disk drive controller and slot E for the tape cassette. Switches and indicators applicable to the processor are described in section 2 of this manual. Switches and indicators applicable to the modem, flexible disk drive, and tape cassette are described in the respective subsystem manual listed in the preface.

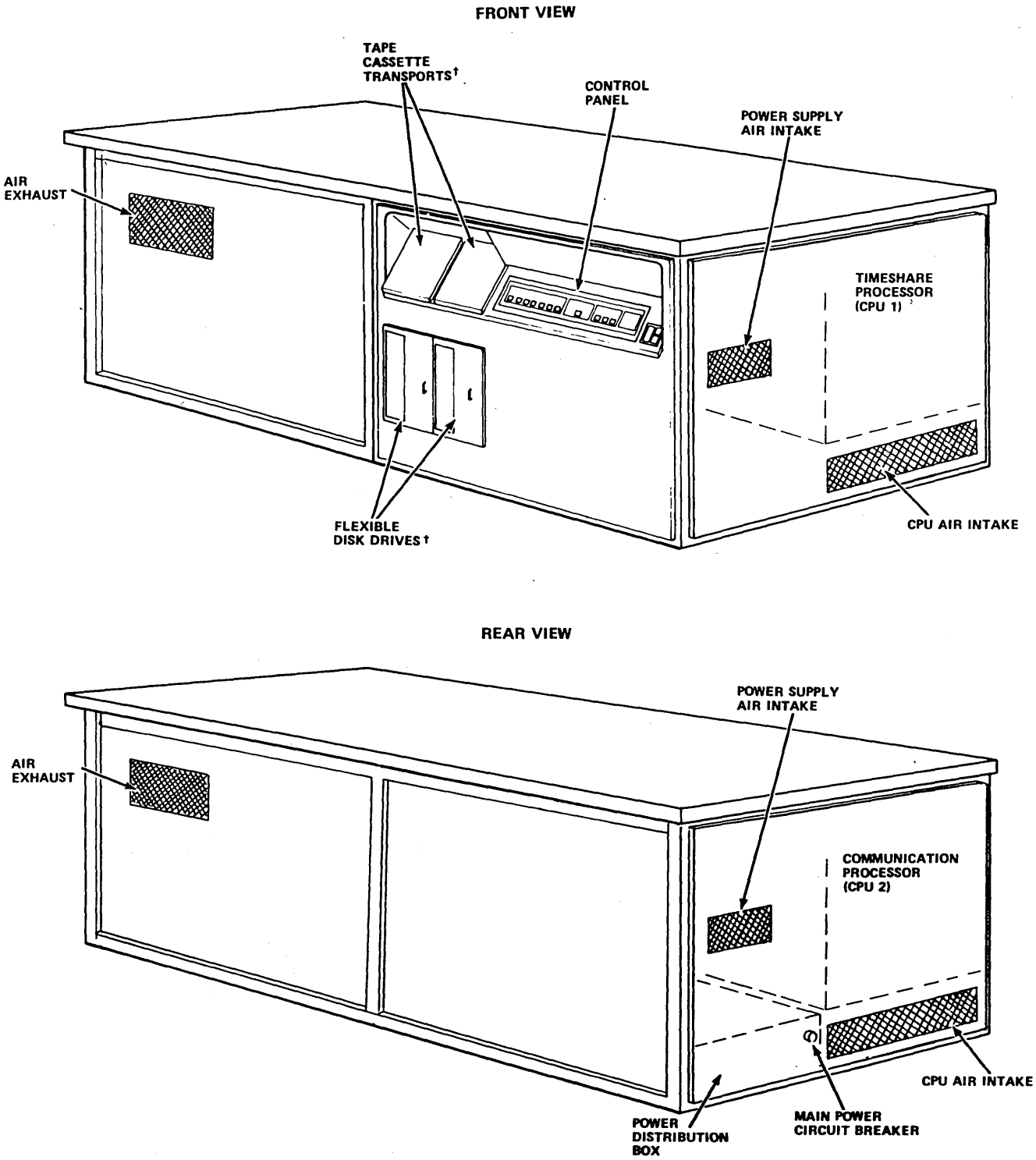
A single control panel configuration is used in both the single-processor and dual-processor equipment cabinet. The PANEL SELECT switch on the rear of the swing-down mounting frame directly below the control panel, is effective only on a dual-processor cabinet, since the associated CPU I and CPU II selection logic is contained only on the dual-processor multiplexer PWA.

BREAKPOINT PANEL AND CONTROLLER

The breakpoint panel provides interface to the micro/macro processor. It allows the operator to load and display all registers and memory within the processor via the breakpoint controller. It provides an operator interface to the function control register and permits setting and clearing all micro-processor control bits of the function control register. It also includes a 16-bit light-emitting diode display and limited keyboard interface. The breakpoint panel communicates with the processor via the breakpoint controller, which is a printed wiring assembly located within the processor logic chassis. The controller provides a programmable micro/macro breakpoint capability that is useful in debugging software and troubleshooting hardware.

Figure 1-7 illustrates the physical characteristics of the breakpoint panel, which is located behind the side panels of the cabinet.

†The breakpoint panel is on the CYBER 18-30 system only.
††Included in the CYBER 18-30 system only.



† DUAL PROCESSOR CONFIGURATION WILL CONTAIN EITHER TAPE CASSETTE TRANSPORTS OR FLEXIBLE DISK DRIVES.

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Figure 1-4. Dual-Processor Cabinet, Exterior Views

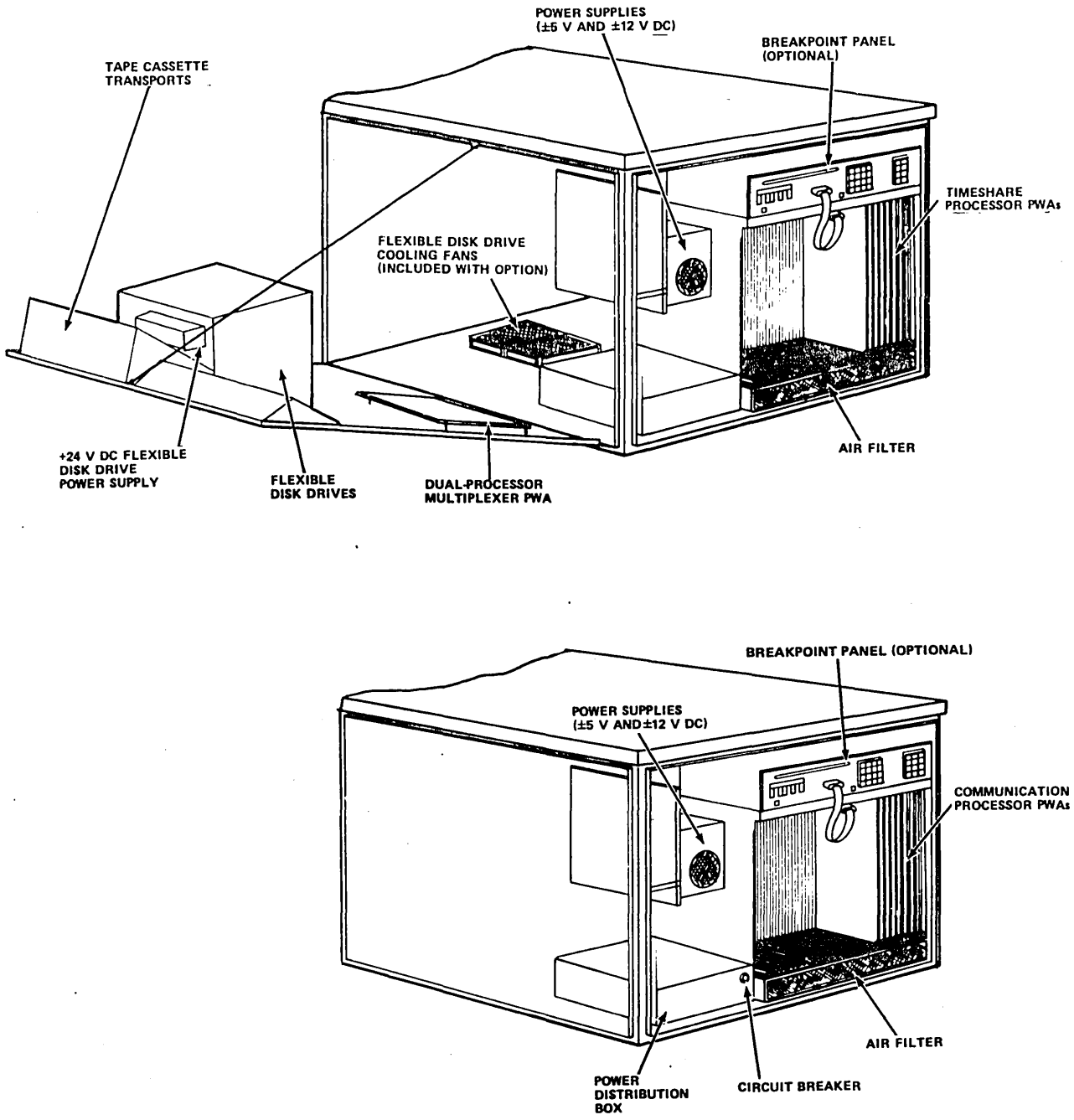


Figure 1-5. Dual-Processor Cabinet Equipment Location, Interior Views (Sheet 1 of 2)

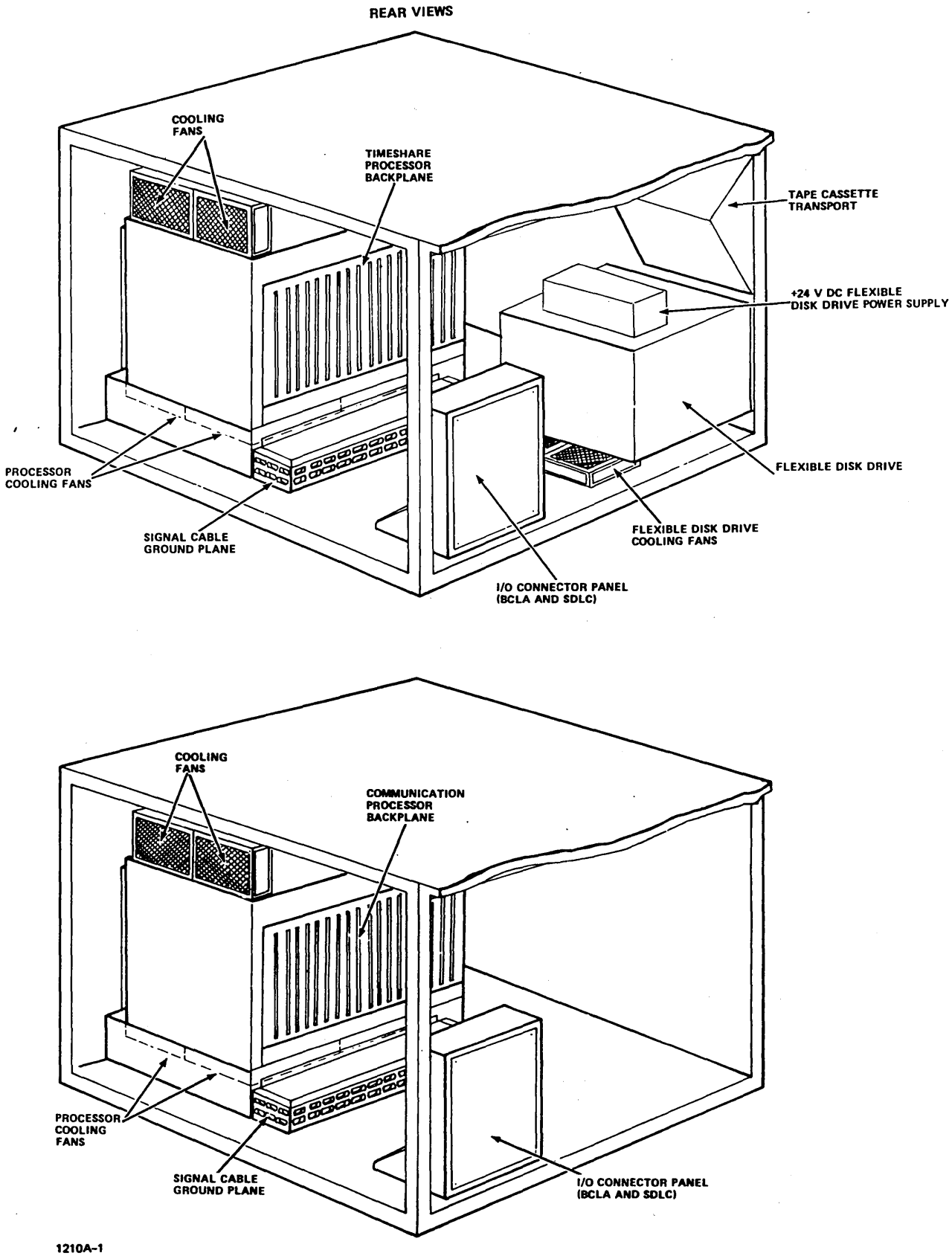


Figure 1-5. Dual-Processor Cabinet Equipment Location, Interior Views (Sheet 2 of 2)

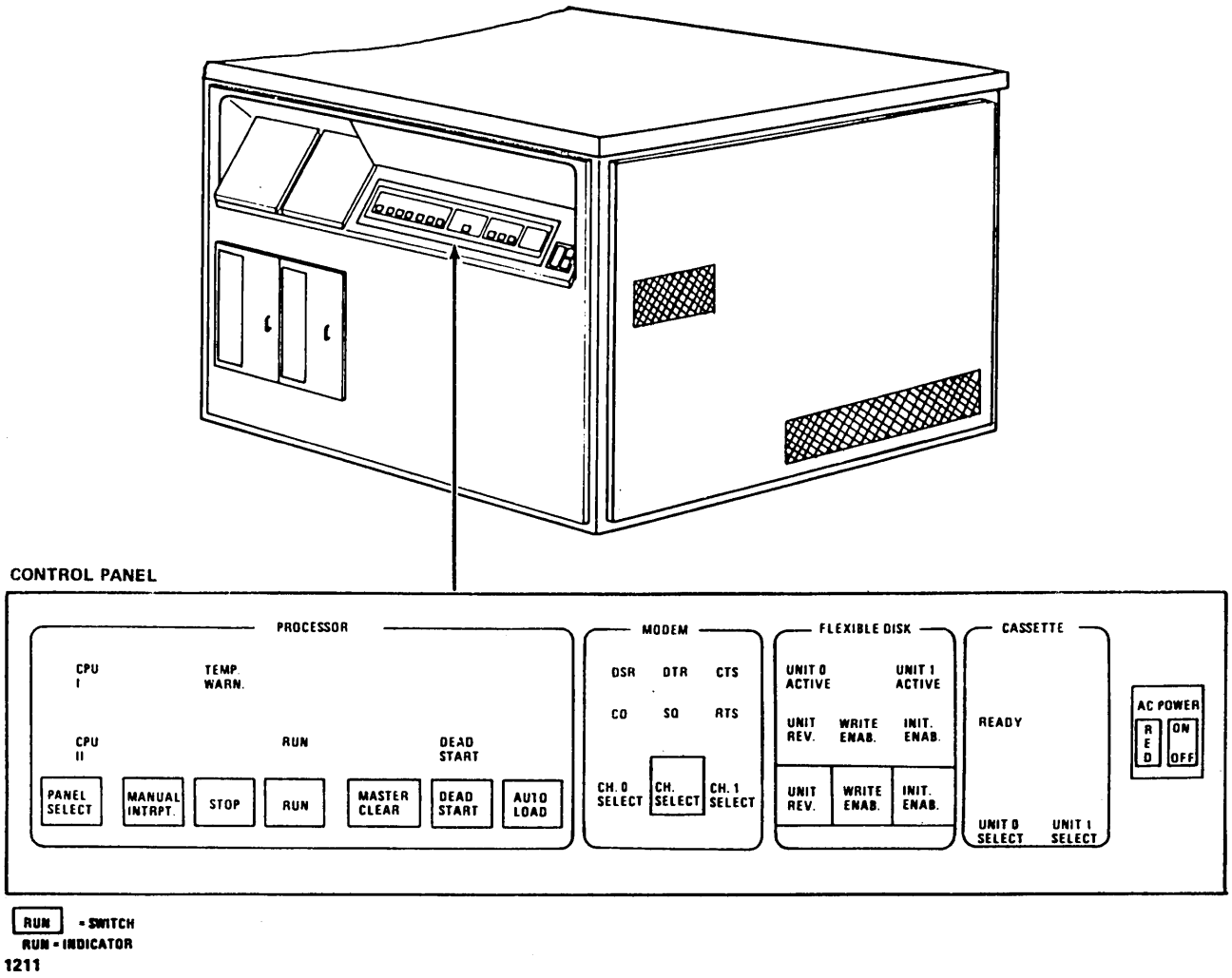


Figure 1-6. Processor Control Panel

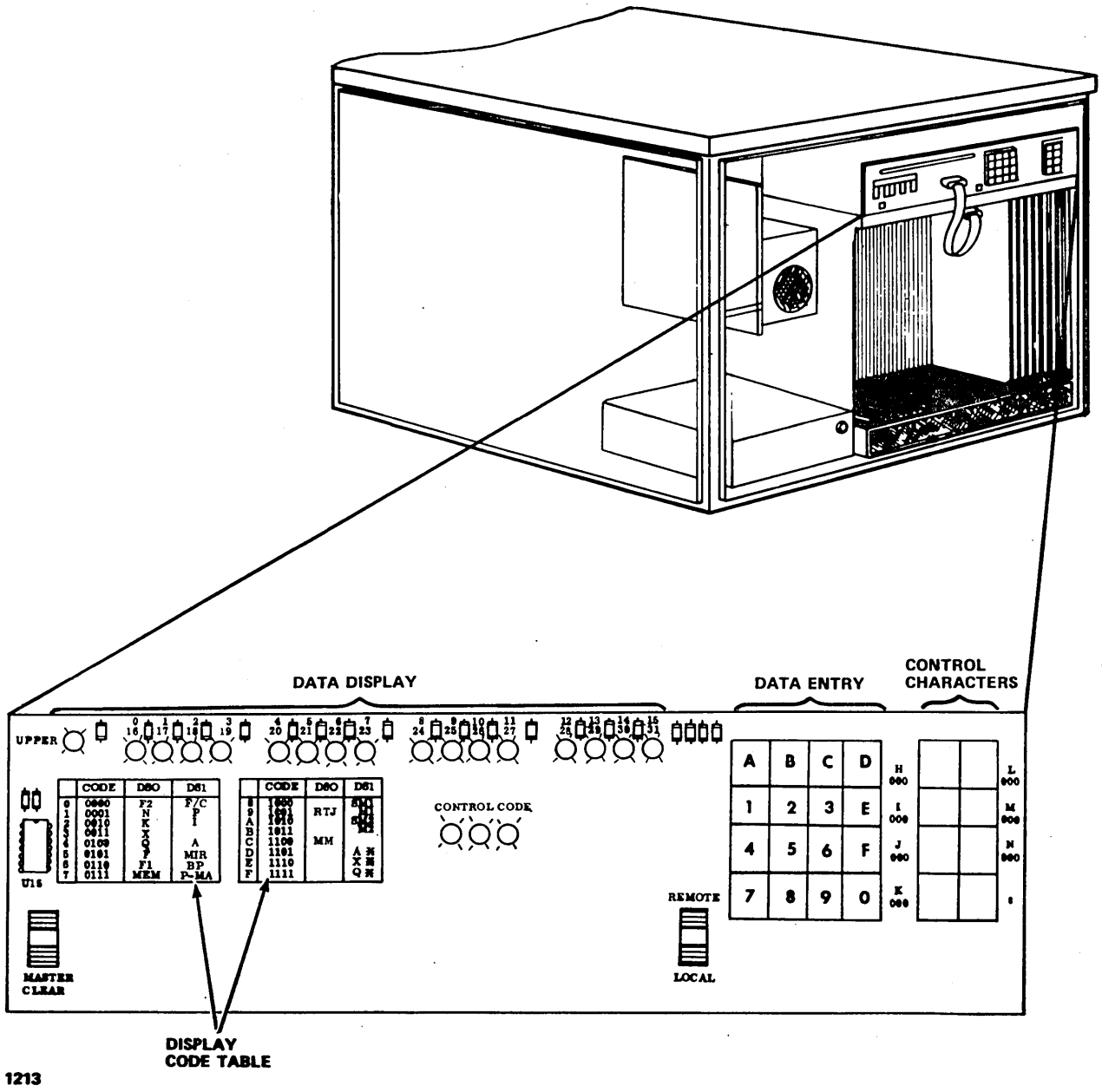


Figure 1-7. Breakpoint Panel Physical Characteristics

This section contains descriptions of the operator controls and indicators contained on the single- and dual-processor equipment cabinets that affect the system operation.

PROCESSOR, EQUIPMENT CABINET, AND CONTROL PANEL

Operator controls in the processor and equipment cabinet are limited to those associated with the control panel, power distribution system, and temperature alarm system. These switches and indicators are illustrated in figure 2-1.

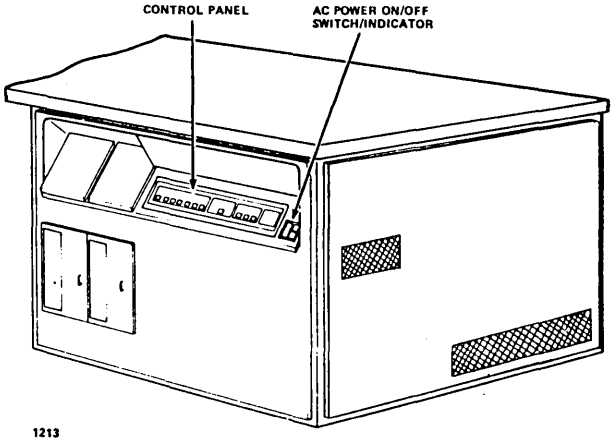


Figure 2-1. Processor Controls and Indicators

Operator control of the processor within a system configuration is via the console display and the control panel. These operator control units provide basic control functions including autoload, deadstart, master clear, stop, manual interrupt, and run. Figure 2-2 shows the location and identity of the controls and indicators on the control panel. Table 2-1 describes their functions.

Some maintenance actions described in the diagnostic decision logic tables (DDLTs) in section 6 must be performed in panel mode. This mode enables the display of various computer registers on the console display and the performance of necessary maintenance operations. Panel mode is entered by pressing the ESC key on the console display. Once in panel mode, entries are made on the console display as described in the DDLTs in section 6. Each entry is terminated by pressing the colon (:) or G key on the keyboard.

BREAKPOINT PANEL

The breakpoint panel and controller allow the operator to display all registers and to interface to the function control register, which allows the setting and clearing of control bits. The breakpoint panel and controller also permit setting of breakpoint for software and hardware analysis. The breakpoint panel is enabled by placing the LOCAL/REMOTE switch on the panel to the LOCAL position. Figure 2-3 illustrates the location of the control switches and indicators on the breakpoint panel. Table 2-2 briefly describes the function of the switches and indicators identified in figure 2-3. In the dual-processor system, each processor may be equipped with a breakpoint panel and controller.

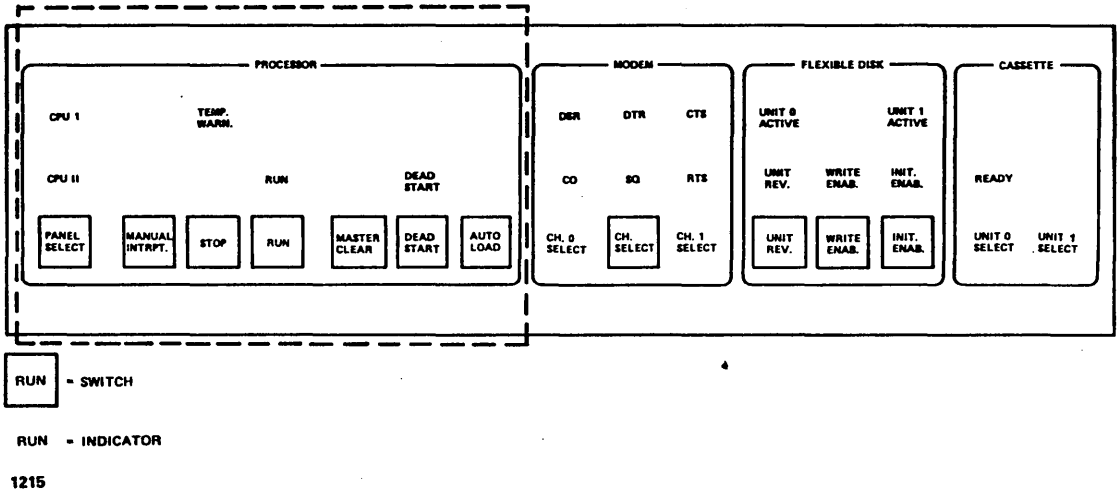


Figure 2-2. Processor Controls and Indicators on Control Panel

TABLE 2-1. PROCESSOR CONTROLS AND INDICATORS

Name	Type	Location	Function
AC POWER ON/OFF	Switch	Cabinet front panel	Applies ac power to or removes power from the processor
POWER ON	Indicator	Control panel	Indicates that power is applied to the processor
TEMP. WARN.	Indicator	Control panel	When illuminated, indicates that the temperature within the cabinet is above the safe operating limit (overtemperature condition)
MASTER CLEAR	Pushbutton switch	Control panel	Initiates a master clear to the processor and controllers within the processor
RUN	Pushbutton switch	Control panel	Initiates a macro run to the processor (resume operation)
RUN	Indicator	Control panel	When illuminated, indicates the processor is in run mode
STOP	Pushbutton switch	Control panel	Initiates a macro halt to the processor
MANUAL INTRPT.	Pushbutton switch	Control panel	Initiates a manual (external) interrupt to the processor. Used during diagnostic operations to access the diagnostic monitor
DEAD START	Pushbutton switch	Control panel	Initiates an autoload from an input device, using the transform as a loader
DEAD START	Indicator	Control panel	When illuminated, indicates a deadstart operation is in process
AUTO LOAD	Pushbutton switch	Control panel	Initiates an autoload from a mass storage device
CPU I	Indicator	Control panel	Indicates processor 1 is active (selected)
CPU II	Indicator	Control panel	Indicates processor 2 is active (selected)
PANEL SELECT	Pushbutton switch	Control panel	Used to select processor 1 or processor 2 for connection to the control panel. The console display is also connected to the selected processor.

NOTE: Modem, flexible disk drive, and cassette controls that also appear on the control panel are described in their respective subsystem manual.

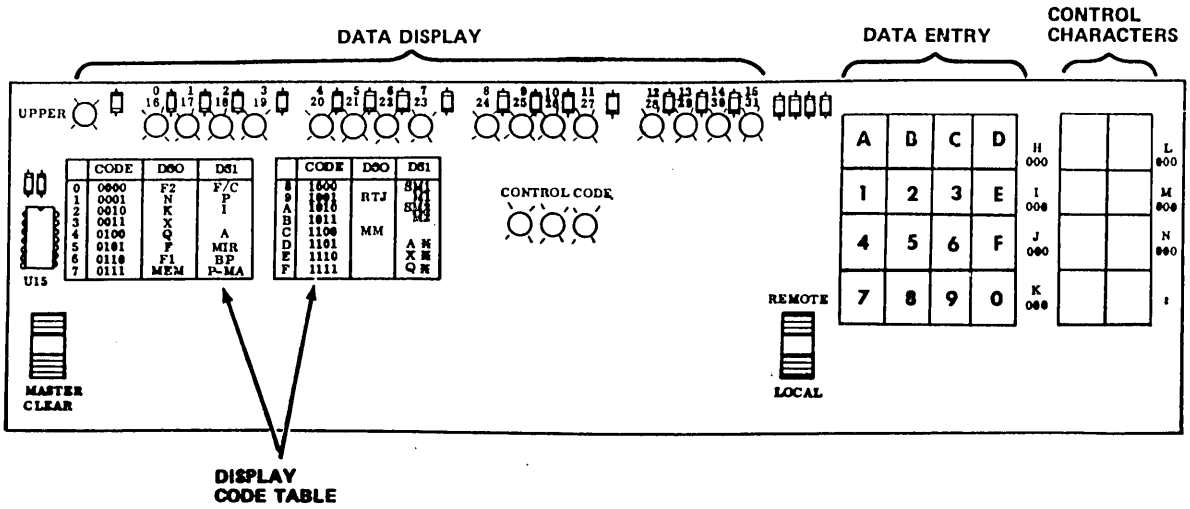


Figure 2-3. Breakpoint Panel Switches and Indicators

TABLE 2-2. BREAKPOINT PANEL SWITCH AND INDICATOR FUNCTIONS

Switch or Indicator	Type	Function
MASTER CLEAR	Momentary contact switch	Pressing this switch provides a master clear to the processor, memory, and all peripheral controllers within the processor.
REMOTE/LOCAL	Single-pole single-throw switch	In local mode, this switch enables use of the breakpoint panel. In remote, the normal console display entry mode is used.
Data display	Indicator	This 16-bit panel provides a display of register data as functions are performed.
UPPER	Indicator	When illuminated, this light-emitting diode indicates the upper 16 bits of any 32-bit register selected are being displayed. If not illuminated, the lower 16 bits are displayed.
CONTROL CODE	Indicator	This three-bit light-emitting diode display indicates the last control character entered.
Data entry	Pushbutton switches	These 16 momentary contact switches are used to enter hexadecimal data.
Control characters	Pushbutton switches	These eight momentary contact switches are used for entering control characters.

Refer to the installation manual listed in the preface for information applicable to installing the CYBER 18 systems and subsystems.

This section contains a list of replaceable assemblies for the single- and dual-processor equipment cabinets and a brief description of each replaceable assembly. Part numbers for replaceable assemblies may be found in section 7.

Illustrations of switch and jumper locations on the printed wiring assemblies are provided in this section. Tables are also included that list the switch and jumper selections available and that designate the switch settings and jumper connections for normal operation.

PROCESSOR REPLACEABLE ASSEMBLIES

The CYBER 18 processor is housed in a cabinet that includes power supplies, power distribution circuits, and a control panel. The replaceable assemblies that are applicable to a single-processor system are listed in table 4-1; the replaceable assemblies that are applicable to a dual-processor (timeshare) system are listed in table 4-2. The subassembly part numbers are listed in section 7. Printed wiring assembly (PWA) positions within the processor chassis are illustrated in figure 4-1. All printed wiring assemblies are 11 by 14 inches (279 by 356 millimeters) in size and each occupies one position (slot) within the processor chassis. Table 4-3 lists normal and optional PWA placements. Table 4-4 gives a brief description of these replaceable assemblies.

SWITCH/JUMPER SETTINGS, NORMAL OPERATION

MEMORY INTERFACE PWA

The memory interface (address) PWA contains printed-circuit-type switches for selection of direct memory access (DMA) priority. Figure 4-2 shows the location and normal settings of these switches for a CYBER 18 system.

I/O-TTY CONTROLLER PWA

This PWA provides an interface between the processor and a comment device (teletypewriter or console display). Communication rates (speeds) vary with the type of device used and the application. Therefore, the rate select switch (baud rate) on the I/O-TTY controller must be set to a rate compatible with the comment device. In the CYBER 18 configuration, the normally selected rate is 9600 baud. Figure 4-3 shows the location and normal operating position of these switches.

TRANSFORM PWA

The transform PWA provides for enable/disable of programmed read-only memory via a jumper located at position F13. When this jumper is installed, read-only micro memory on the PWA is enabled. Pages 0 and 1 are the assigned page numbers for this optional read-only memory. Figure 4-4 illustrates the location of the micro-memory select jumper for the CYBER 18 processor configuration.

READ/WRITE MICRO-MEMORY INSTALLATION CONFIGURATION

The 512- and 2048-instruction micro-memory PWAs may be installed in CYBER 18 systems in any combination using processor slots T and S. Note that the lowest page number is always 4 and that slot T is always used for a single PWA.

512-Instruction Micro-Memory PWA (One Page)

The switches shown in figure 4-5 provide for micro-memory page selection. Pages 0 and 1 of micro memory are reserved for optional read-only memory installed on the transform PWA. Pages 2 and 3 are not used. The lowest page number that can be used for read/write micro memory is page 4. Table 4-5 lists the standard configurations of read/write micro memory and the required processor slots for PWA installation.

2048-Instruction Micro-Memory PWA (Four Pages)

The switches shown in figure 4-6 provide for micro-memory page selection. Pages 0 and 1 of micro memory are reserved for optional read-only memory installed on the transform PWA. Pages 2 and 3 are not used. The lowest page number that can be used for read/write micro memory is page 4. Table 4-5 lists the standard configurations of read/write micro memory and the required processor slots for PWA installation.

MAGNETIC TAPE CONTROLLER

These equipment and interrupt jumpers are wire-wrap interconnections at the processor chassis backplane between the magnetic tape controller and the computer system (see table 4-6). These are special wires normally installed at the factory when a tape controller is provided.

BREAKPOINT PANEL

The breakpoint panel system consists of a breakpoint panel, a ribbon cable, and a controller, which are the only replaceable assemblies. They are illustrated in figure 4-7, and their functions are described in table 4-7. In a dual-processor system, each processor may have a breakpoint panel and controller. (See section 7 for subassembly part numbers.)

The breakpoint controller, if included in the system configuration, provides for entry of common computer control functions from the breakpoint panel. A basic part of the breakpoint controller is the function control register (FCR). This 32-bit register provides the breakpoint panel access to the central processor in a similiar manner to the way the console display accesses the central processor. Table 4-8 indicates the function control register bit assignments and table 4-9 lists the display code definitions.

TABLE 4-1. SINGLE-PROCESSOR SYSTEM REPLACEABLE ASSEMBLIES

Equipment	Replaceable Assemblies
Processor	Arithmetic logic unit (ALU) (PWA) Status mode interrupt (SMI) (PWA) Control 1 (PWA) Control 2 (PWA) Transform (PWA) I/O-TTY controller (PWA)† Memory interface (address) (PWA) Memory interface (data) (PWA) Flexible disk drive controller (PWA) Cooling fans
Processor options	512-instruction micro memory (PWA) 2048-instruction micro memory (PWA) Error correction code MOS array (PWA) 16K MOS memory (PWA) 32K MOS memory (PWA)
Cabinet	Temperature sensors Power distribution system: Ac power switch Triac Printed wiring assembly Line filter Circuit breaker Power supply (dual-processor equipment cabinets) ±5 V dc ±12 V dc Power supply (flexible disk drive) +24 V dc Power supply (system with GD122-B power source) ±5 V dc module ±12 V dc module +12 V dc, -9 V dc, and -5 V dc regulator Control panel Panel control (PWA) Chromeric switch Bezel Flexible disk drive

† Also provides interface to a console display.

TABLE 4-2. DUAL-PROCESSOR SYSTEM REPLACEABLE ASSEMBLIES

Equipment	Replaceable Assemblies
Timeshare processor (CPU 1)	Arithmetic logic unit (ALU) (PWA) Status mode interrupt (SMI) (PWA) Control 1 (PWA) Control 2 (PWA) Transform (PWA) (I/O-TTY controller (PWA)† Memory interface (address) (PWA) Memory interface (data) (PWA) Tape cassette controller (PWA) or Flexible disk drive controller (PWA) Cooling fans
Communication processor (CPU 2)	Arithmetic logic unit (ALU) (PWA) Status mode interrupt (SMI) (PWA) Control 1 (PWA) Control 2 (PWA) Transform (PWA) I/O-TTY controller (PWA)† Memory interface (address) (PWA) Memory interface (data) (PWA) Tape cassette controller (PWA) or Flexible disk drive controller (PWA) Cooling fans
Processor options (both processor)	512-instruction micro memory (PWA) 2048-instruction micro memory (PWA) Error correction code MOS array (PWA) 16K MOS memory (PWA) 32K MOS memory (PWA)
Cabinet	Temperature sensors Power distribution system Ac power switch Triac Printed wiring assembly Line filters Circuit breaker

†Also provides interface to a console display.

TABLE 4-2. DUAL-PROCESSOR SYSTEM REPLACEABLE ASSEMBLIES (Contd)

Equipment	Replaceable Assemblies
Equipment Cabinet	Power supply (dual-processor equipment cabinets) ±5 V dc ±12 V dc Power supply (flexible disk drive) +24 V dc Power supply (system with GD122-B power source) ±5 V dc module ±12 V dc module ±12 V dc, -9 V dc, -5 V dc regulator Control panel Panel control (PWA) Chromeric switch Bezel Dual-processor multiplexer (PWA) Tape cassette transport or Flexible disk drive

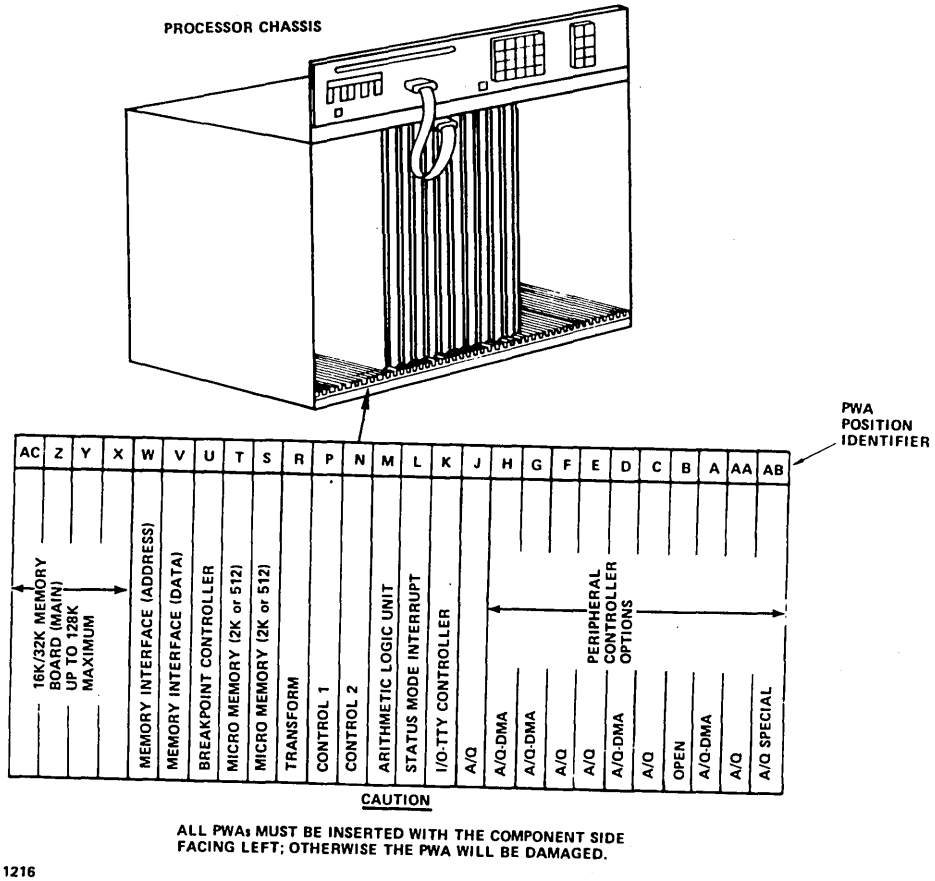


Figure 4-1. PWA Placement Diagram

TABLE 4-3. PROCESSOR NORMAL PWA PLACEMENT

Slot Location	Printed Wiring Assembly	Single Processor	Dual Processor	
			Timeshare	Communication
AC	MOS memory (16K/32K) or error correction code	x	x	x
Z	MOS memory (16K/32K)	x	x	x
Y	MOS memory (16K/32K)	x	4	4
X	MOS memory (16K/32K)	x	4	4
W	MOS memory interface (address)	1	1	1
V	MOS memory interface (data)	1	1	1
U	Breakpoint controller	x	x	4
T	512/2K instruction micro memory	x	1	1
S	512/2K instruction micro memory	x	x	x
R	Transform	1	1	1
P	Control 1	1	1	1
N	Control 2	1	1	1
M	Arithmetic logic unit (ALU)	1	1	1
L	Status mode interrupt (SMI)	1	1	1
K	I/O-TTY controller	1	1	1
J	Card reader/line printer controller	x	4	2
	Card reader/line printer/communication line adapter (CR/LP/CLA) controller	x	x	2
H	Module drive interface	x	4	2
	Carriage disk drive controller	x	x	2
	Tape cassette controller	-	-	4
	Flexible disk drive controller	-	-	3
G	Magnetic tape transport controller (NRZI phase-encoded)	x	4	-
	Multiplexer loop interface adapter	-	-	1
F	Dual-channel communication line adapter	x	x	-
	Eight-channel communication line adapter	x	x	-
	Multiplexer loop interface adapter	-	-	1
E	Flexible disk drive controller	1	3	-
	Tape cassette controller	x	4	-
	Multiplexer loop interface adapter	-	-	1
D	Synchronous data link controller	2	2	2
	Buffered communication line adapter (BCLA)	2	2	2
	Flexible disk drive controller	x	x	2
C	Restart loader	2	2	2
	Buffered communication line adapter expansion to BCLA in slot D	2	2	2

NOTES:

x Equipment option
1 Normally-supplied PWA complement
2 Options not supported by this manual
3 PWA Normally-supplied with the CYBER 18-25
4 PWA Normally-supplied with the CYBER 18-30
- Not applicable

TABLE 4-3. PROCESSOR NORMAL PWA PLACEMENT (Contd)

Slot Location	Printed Wiring Assembly	Single Processor	Dual Processor	
			Timeshare	Communication
B	Buffered communication line adapter expansion to BCLA in slot A	2	2	2
A	Buffered communication line adapter	2	2	2
AA	CYBER 18/1500 Adapter (IOM)	2	2	2
	Paper tape reader/paper tape punch controller	2	2	2
	A/Q expansion	2	2	2
AB	Magnetic tape transport controller (NRZI)	x	4	2

NOTES:

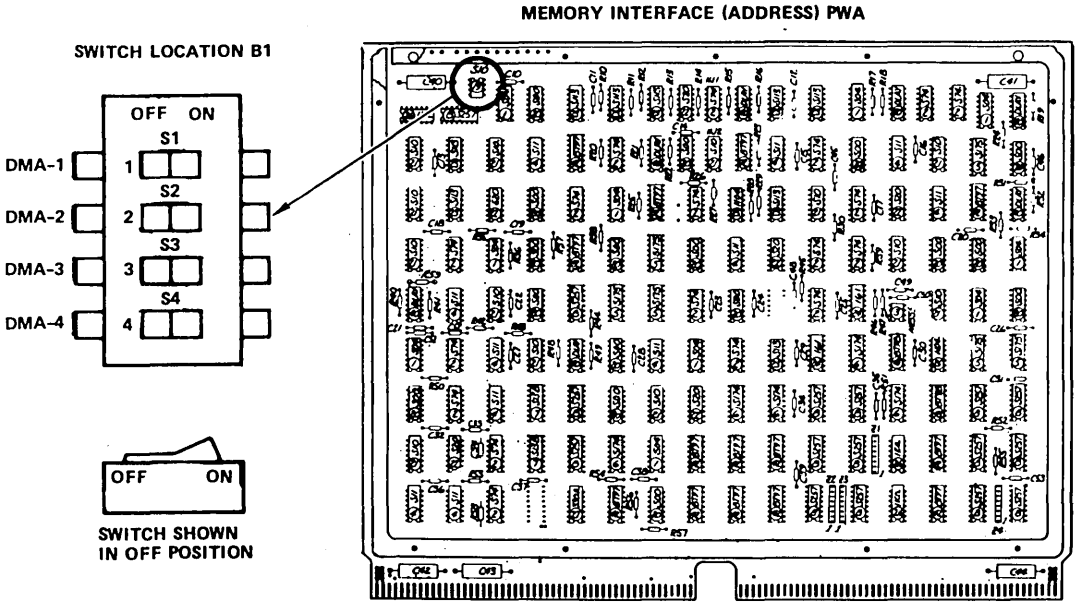
x Equipment option
1 Normally-supplied PWA complement
2 Options not supported by this manual
3 PWA Normally-supplied with the CYBER 18-25
4 PWA Normally-supplied with the CYBER 18-30
- Not applicable

TABLE 4-4. REPLACEABLE ASSEMBLY FUNCTIONAL DESCRIPTION

Replaceable Assembly	Description
Processor:	
Arithmetic logic unit	Provides arithmetic and logical capabilities, and data transfer organization of the processor
Status mode interrupt	Provides interrupt control for the processor
Control 1	Provides main timing and register control functions of the processor
Control 2	Provides all basic micro-processing control within the processor
Transform (with read-only memory)	Selects bits from various sources in the organization of the processor and transfers them to the micro-memory address register to start a sequence of micro instructions that emulate (using read-only memory) a 1700 macro instruction
I/O-TTY controller	Provides data and address signal drive circuits to peripheral controllers within the processor chassis. Also serves as interface to a console display
Memory interface (address); memory interface (data)	Two PWAs (address and data) that determine the main memory bank selected, insert and monitor parity and protect bits, and perform DMA data transfers
Cooling fans	Six muffin-type fans mounted on the bottom of the processor PWA chassis to provide cooling for the logic boards within the processor
Processor options:	
512-instruction micro memory; finalization kit	Functions as the micro-instruction storage unit for the processor. Provides read/write storage for 512 32-bit micro-control instructions. Developed for systems that require the processor to be reprogrammed or reorganized for a variety of applications
2048-instruction micro memory; finalization kit	Similar to the 512-instruction micro memory, except that it provides a 2048 32-bit micro-control instruction storage capabiliy for the processor

TABLE 4-4. REPLACEABLE ASSEMBLY FUNCTIONAL DESCRIPTION (Contd)

Replaceable Assembly	Description
Error correction code MOS array; finalization kit	Provides error correction for 96K words (18-bit) of MOS memory. Corrects single-bit errors and detects multiple-bit errors
MOS memory (16K); finalization kit	Consists of 16K words (18-bit) of MOS memory and serves as the macro memory in the processor
MOS memory (32K); finalization kit	Same as 16K MOS memory, except that it provides 32K words (18-bit) of macro memory
Cabinet:	
Temperature sensors	Desk-type cabinet housing the processor, power supplies, and control panel. Includes temperature sensors for high temperature warning
Power supply (GD122-B): ±5 V dc power supply ±12 V dc power supply Voltage regulator	These three power supplies provide dc voltages of ±5 V, ±12 V, and -5 V to the various circuits in the processor logic and memory. A power fail signal is sent to the control 1 PWA from the 5 V dc supply if its voltage drops below +4.75 V.
Power supply (L.H.) ±5 V dc ±12 V dc	This power supply (L.H. research) provides dc voltages of ±5 V and ±12 V to the processor logic, memory, and selected optional devices. A power fail signal is sent to the control 1 PWA if the +5 V supply output drops below 4.75 V.
Power distribution system: Printed wiring assembly Ac power switch Triac Line filter Circuit breaker	Provides distribution of ac power to the processor power supplies. Includes a main power ac power circuit breaker, RFI line filters to limit time transients and emissions, a printed wiring assembly that functions to limit current surges on startup, and a gate-controlled ac switch (triac) that operates in conjunction with the PWA when power has stabilized
Control panel: Panel control (PWA) Multiplexer (PWA) Chromeric switch Bezel	Attached to the cabinet and provides for operator control of the processor. These controls include: MASTER CLEAR, RUN, STOP DEADSTART, AUTOLOAD, CPU I/CPU II, PANEL SELECT, and MANUAL INTRPT. Also provided are controls and indicators for the communication line adapter channel status monitoring and tape cassette and flexible disk drive unit select.
Breakpoint panel	Provides operator interface to the micro/macro processor (via the breakpoint controller) and display of all registers and both micro and macro memory. Permits setting and clearing of processor function control bits.



PRIORITY CHANNEL ENABLE (LOCATION B1)

FUNCTION	LOCATION	NORMAL POSITION†
DMA-1	S1	OFF
DMA-2	S2	OFF
DMA-3	S3	OFF
DMA-4	S4	OFF

†NO PRIORITY SELECTED

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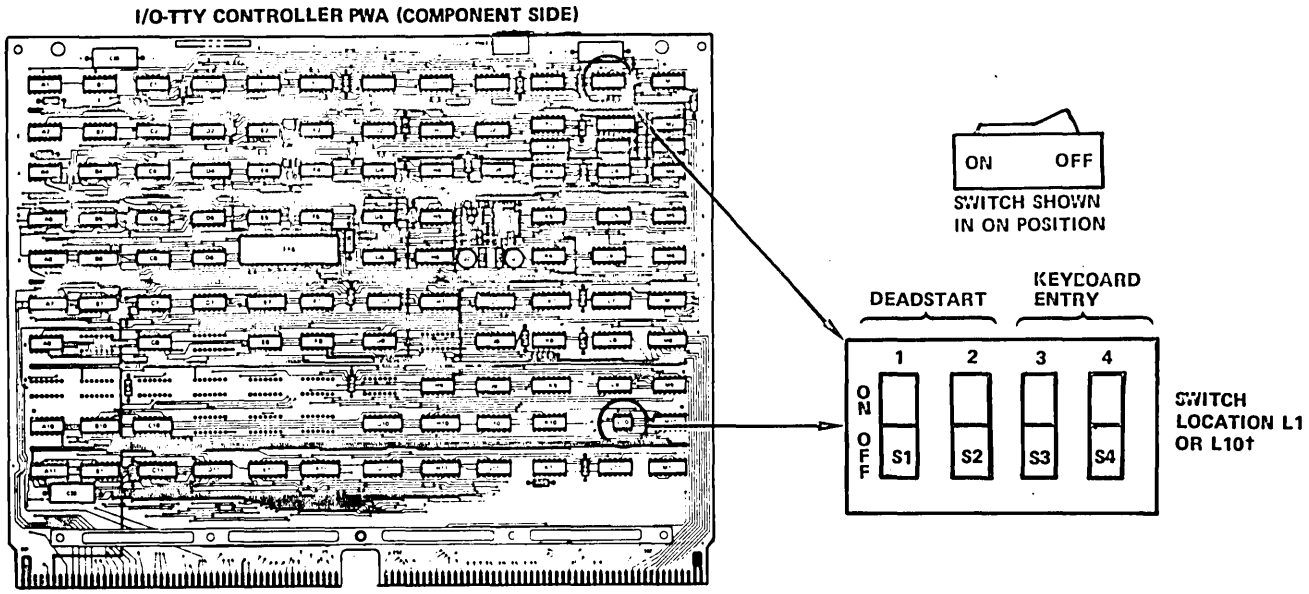
Figure 4-2. Memory Interface (Address) PWA Switches



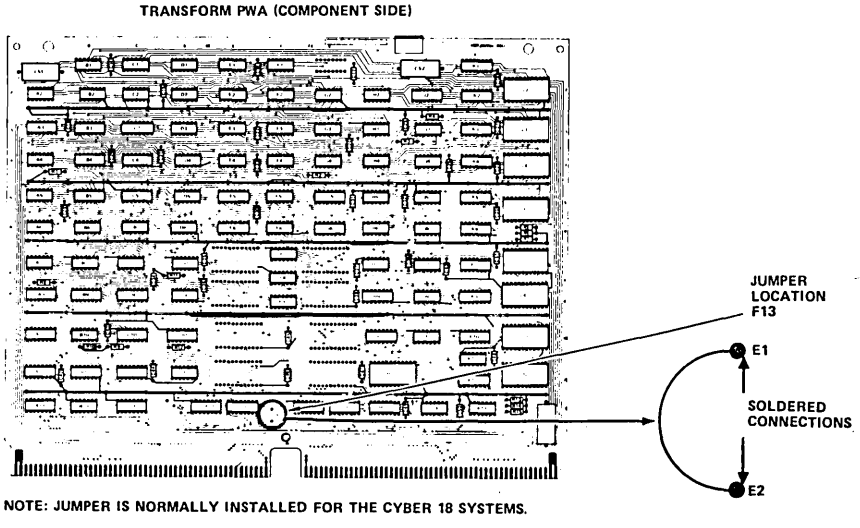
BAUD RATE SELECT (LOCATION L1 OR L10)†

RATE	DEADSTART		KEYBOARD ENTRY	
	SWITCH POSITION 1	SWITCH POSITION 2	SWITCH POSITION 3	SWITCH POSITION 4
110	ON	ON	ON	ON
300	ON	OFF	OFF	ON
1200	OFF	ON	ON	OFF
9600††	OFF	OFF	OFF	OFF
††NORMAL OPERATING POSITION				

†SWITCH LOCATION DEPENDS ON CONFIGURATION LEVEL:
B3 LOCATION L10
B4 LOCATION L1

1202

Figure 4-3. I/O-TTY Controller PWA Switches



NOTE: JUMPER IS NORMALLY INSTALLED FOR THE CYBER 18 SYSTEMS.

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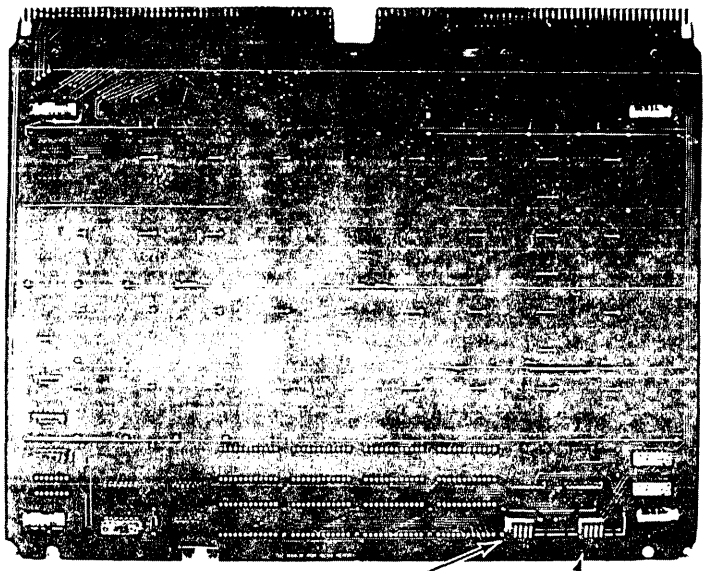
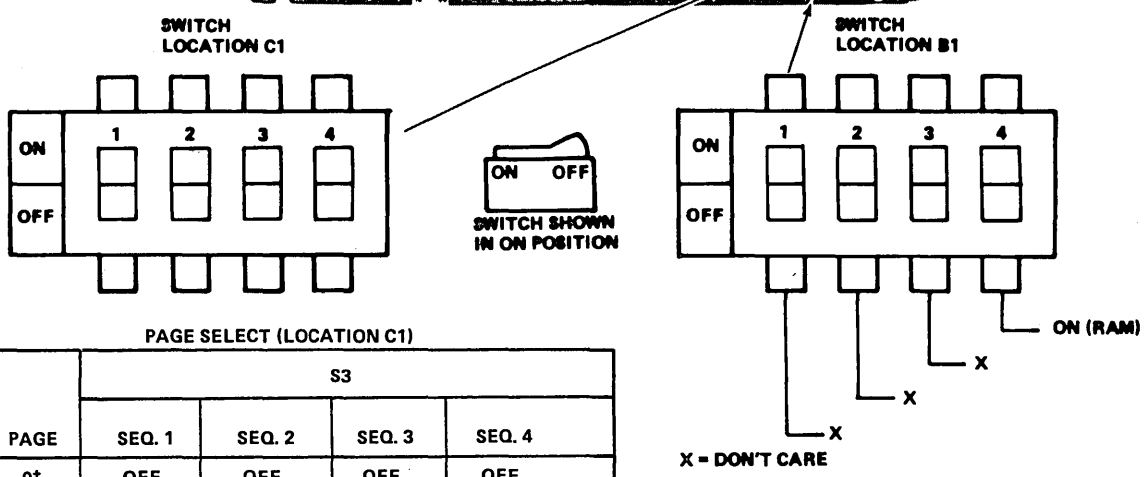
Figure 4-4. Transform PWA Jumper

512-INSTRUCTION MICRO-MEMORY PWA (COMPONENT SIDE)





PAGE SELECT (LOCATION C1)

PAGE	S3 SEQ. 1	S3 SEQ. 2	S3 SEQ. 3	S3 SEQ. 4
0†	OFF	OFF	OFF	OFF
1†	OFF	OFF	OFF	ON
2†	OFF	OFF	ON	OFF
3†	OFF	OFF	ON	ON
4††	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON
8†††	ON	OFF	OFF	OFF
9	ON	OFF	OFF	ON
10	ON	OFF	ON	OFF
11	ON	OFF	ON	ON
12	ON	ON	OFF	OFF
13	ON	ON	OFF	ON
14	ON	ON	ON	OFF
15	ON	ON	ON	ON

†PAGE SELECT SWITCHES SHOULD NOT BE SET TO PAGES 0 THROUGH 3.

††STANDARD SETTING FOR CYBER 18-30 CPU II (COMMUNICATION PROCESSOR)

†††STANDARD SETTING FOR ALL CPUs EXCEPT CYBER 18-30 CPU II.

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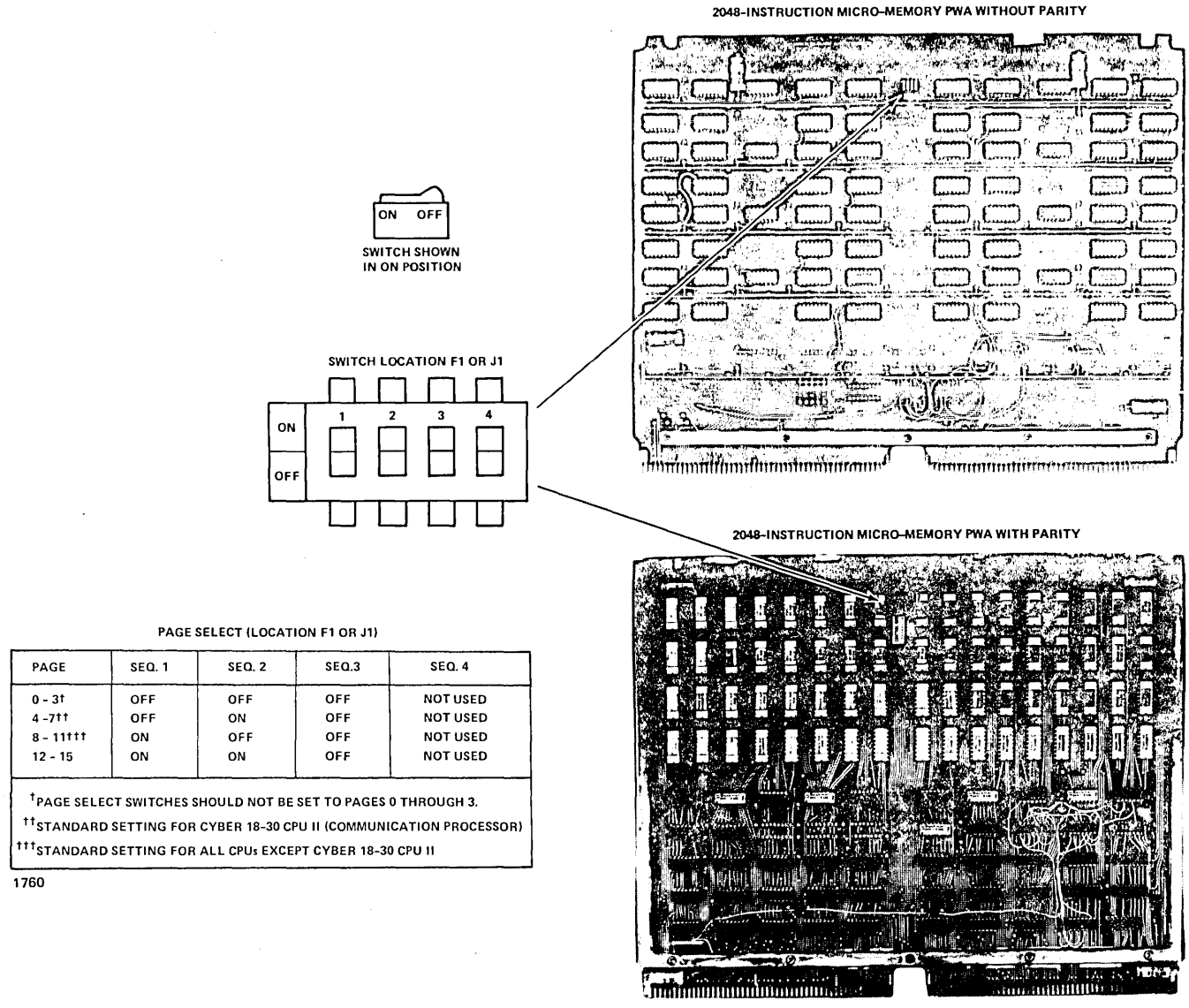
Figure 4-5. 512-Instruction Micro-Memory Page Select Switches

TABLE 4-5. STANDARD CONFIGURATIONS OF OPTIONAL MICRO-MEMORY PWA (READ/WRITE)

Number of Pages	Printed Wiring Assemblies Installed	Processor Slot
1	512 board	T
2†	512 board 512 board	T S
4	2048 board	T
5†	2048 board 512 board	T S
8†	2048 board 2048 board	T S

†For dual-board installation, slot T should contain the standard page(s) and slot S the next consecutively higher numbered page(s). See figures 4-5 and 4-6.



PAGE SELECT (LOCATION F1 OR J1)

PAGE	SEQ. 1	SEQ. 2	SEQ.3	SEQ. 4
0 - 3†	OFF	OFF	OFF	NOT USED
4 -7††	OFF	ON	OFF	NOT USED
8 - 11†††	ON	OFF	OFF	NOT USED
12 - 15	ON	ON	OFF	NOT USED

†PAGE SELECT SWITCHES SHOULD NOT BE SET TO PAGES 0 THROUGH 3.
††STANDARD SETTING FOR CYBER 18-30 CPU II (COMMUNICATION PROCESSOR)
†††STANDARD SETTING FOR ALL CPUs EXCEPT CYBER 18-30 CPU II

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Figure 4-6. 2048-Instruction Micro-Memory Page Select Switches

TABLE 4-6. ADDRESS AND INTERRUPT LINES

SPT/ Port Address Wiring				SSEL/ Select Line Wiring			
From Slot A		To Slot K		From Slot A		To SLot K	
Name	Pin	Name	Pin	Name	Pin	Name	Pin
SPT/	A227	SPT0/	K-99	SSEL/	A251	SSEL0/	K-293
SPT/	A227	SPT1/†	K-98	SSEL/	A251	SSEL1/†	K-294
SPT/	A227	SPT2/	K-97	SSEL/	A251	SSEL2/	K-295
SPT/	A227	SPT3/	K-96	SSEL/	A251	SSEL3/	K-290
SPT/	A227	SPT4/	K-94	SSEL/	A251	SSEL4/	K-296
SPT/	A227	SPT5/	K-93	SSEL/	A251	SSEL5/	K-297
SPT/	A227	SPT6/	K-95	SSEL/	A251	SSEL6/	K-298
SPT/	A227	SPT7/	K-92	SSEL/	A251	SSEL7/	K-299
RPINT/ Program Interrupt Wiring				RDINT/ Data Interrupt Wiring			
From Slot A		To Slot L		From SLot A		To Slot L	
Name	Pin	Name	Pin	Name	Pin	Name	Pin
RPINT/	A249	INT16/	L-69	RDINT/	A250	INT00/	L-227
RPINT/	A249	INT17/	L-269	RDINT/	A250	INT01/	L-27
RPINT/	A249	INT18/	L-270	RDINT/	A250	INT02/	L-32
RPINT/	A249	INT19/	L-70	RDINT/	A250	INT03/	L-232
RPINT/	A249	INT20/	L-72	RDINT/	A250	INT04/	L-28
RPINT/	A249	INT21/	L-272	RDINT/	A250	INT05/	L-31
RPINT/	A249	INT22/	L-271	RDINT/	A250	INT06/	L-231
RPINT/	A249	INT23/	L-71	RDINT/	A250	INT07/	L-228
RPINT/	A249	INT24/	L-73	RDINT/	A250	INT08/	L-30
RPINT/	A249	INT25/†	L-274	RDINT/	A250	INT09/†	L-230
RPINT/	A249	INT26/	L-74	RDINT/	A250	INT10/	L-229
RPINT/	A249	INT27/	L-273	RDINT/	A250	INT11/	L-29
RPINT/	A249	INT28/	L-277	RDINT/	A250	INT12/	L-33
RPINT/	A249	INT29/	L-276	RDINT/	A250	INT13/	L-226
RPINT/	A249	INT30/	L-77	RDINT/	A250	INT14/	L-233
RPINT/	A249	INT31/	L-275	RDINT/	A250	INT15/	L-234

† Standard system configuration

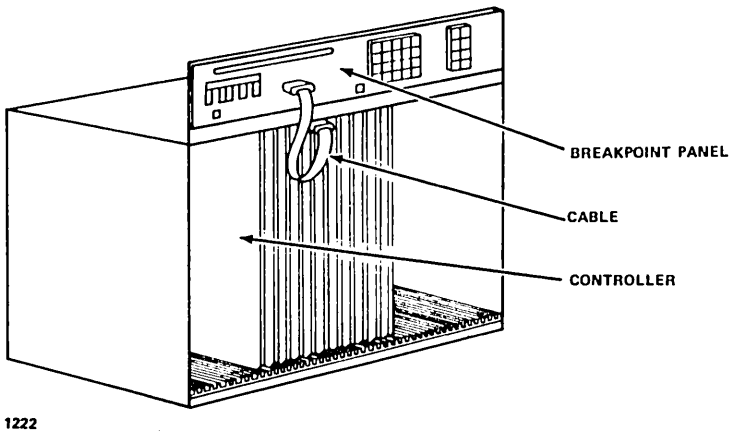


Figure 4-7. Breakpoint Panel Replaceable Assemblies

TABLE 4-7. BREAKPOINT PANEL REPLACEABLE SUBASSEMBLIES FUNCTIONAL DESCRIPTION

Replaceable Subassembly	Function
Breakpoint panel	Provides operator interface to the micro/macro processor (via the breakpoint controller) and display of all registers and both micro and macro memory. Permits setting and clearing of processor function control bits
Breakpoint controller	This printed wiring assembly occupies one slot in the processor chassis, provides a breakpoint capability, is compatible with either RS232 input/output or parallel inputs, and accommodates baud rates of 110, 300, 1200, and 9600.
Interface cable	This 1.5-foot (4.6-meter) ribbon cable connects the panel and controller and provides a path for data and control signal interchange.

TABLE 4-8. FUNCTION CONTROL REGISTER

Bit		Digit	Bit Definition	Bit		Digit	Bit Definition
00	00	(LSB)	Overflow				
01	01	7	Protected instruction				0 0 Breakpoint off
02	02		Protect fault	16	10		0 1 Instruction reference breakpoint
03	03		Parity error	17	11	3	1 0 Storage operand breakpoint
							1 1 All references breakpoint
04	04		Interrupt system active	18	12		Breakpoint instruction (breakpoint stop if clear)
05	05	6	Auto-restart enabled				
06	06		Micro running	19	13		Micro breakpoint, step, go, stop (macro if clear)
07	07		Macro running				
				20	14		Step
				21	15	2	Selective stop
08	08			22	16		Selective skip
09	09	5		23	17		Protect switch
10	0A		Enable auto-display	24	18		
11	0B		Enable console echo	25	19	1	
				26	1A		Display 1
12	0C		Enable micro memory write	27	1B		
13	0D		Multilevel indirect address				
		4	mode	28	1C		
14	0E			29	1D		
15	0F		Suppress console transmit	30	1E	0	Display 0
				31	1F	(MSB)	

TABLE 4-9. DISPLAY CODE DEFINITIONS

Code	Select Code	Display 1 (K Function)	Select Code	Display 0 (L Function)
0 0000	J10:	FCR	J00:	F2 (Addressed by N register)
1 0001	J11:	P†	J01:	N (MSBs)††
2 0010	J12:	I†	J02:	K (LSBs)††
3 0011			J03:	X
4 0100	J14:	A†	J04:	Q
5 0101	J15:	MIR	J05:	F
6 0110	J16:	BP-P/MA	J06:	F1 Addressed by K register Enabled by SM111
7 0111	J17:	BP-P/MA (Display only)	J07:	MEM
8 1000	J18:	SM1		
9 1001	J19:	M1	J09:	$\overline{\text{RTJ}}$
A 1010	J1A:	SM2		
B 1011	J1B:	M2		
C 1100			J0C:	MM
D 1101	J1D:	A*		
E 1110	J1E:	X*		
F 1111	J1F:	Q*		

† Used to address macro memory. The P and A registers are automatically incremented after each memory reference. The I register is not incremented after the memory reference.

†† The combined contents of these two registers are used to address micro memory. The K register is automatically incremented after each memory reference. The N register does not automatically increment.

This section contains diagrams (figures 5-1 through 5-13) and a table (table 5-1) illustrating the single- and dual-processor interconnections and the peripheral connections to the processor(s).

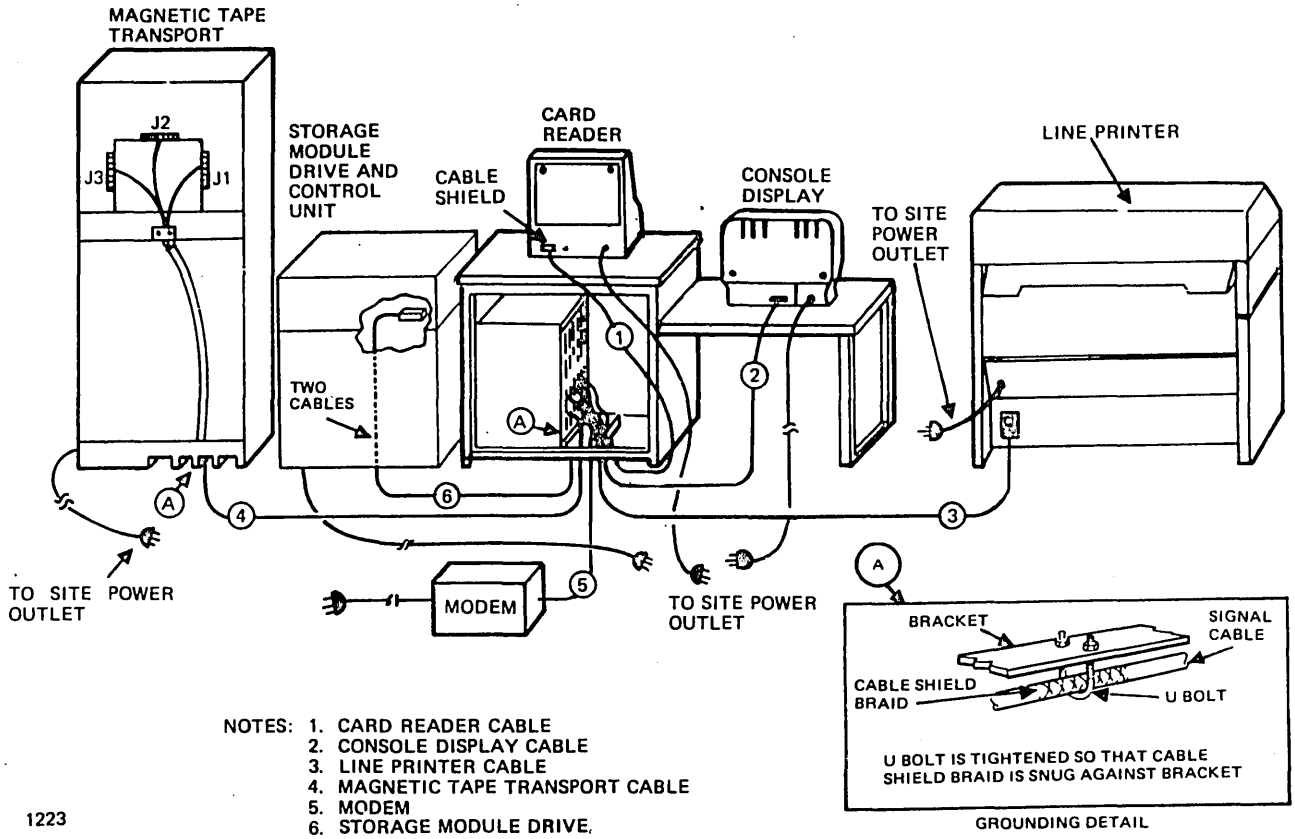


Figure 5-1. Site Cabling Diagram (Typical Single-Processor System)

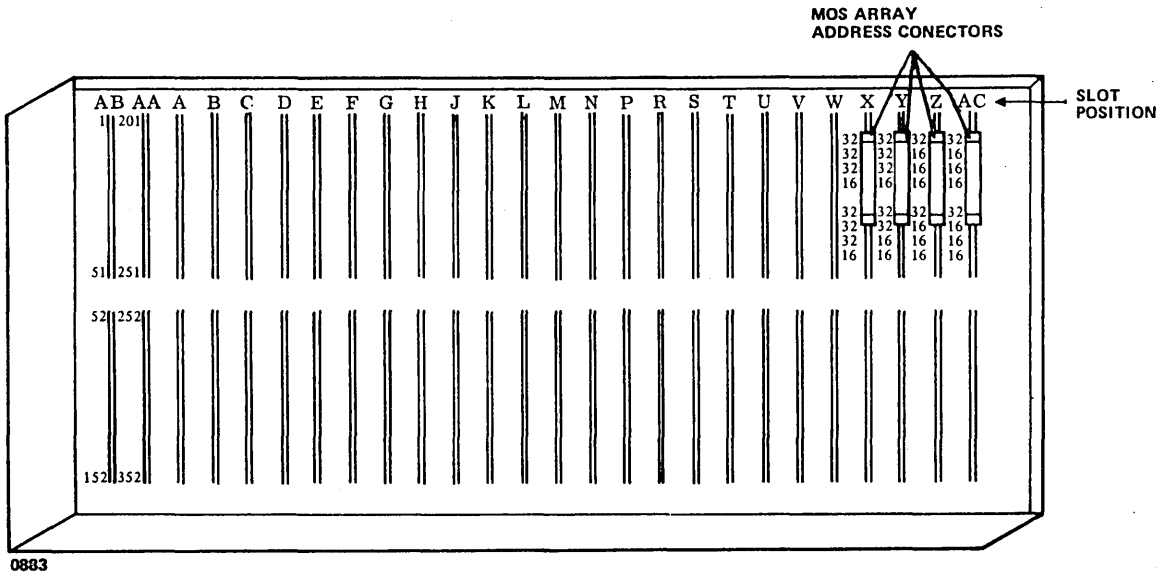
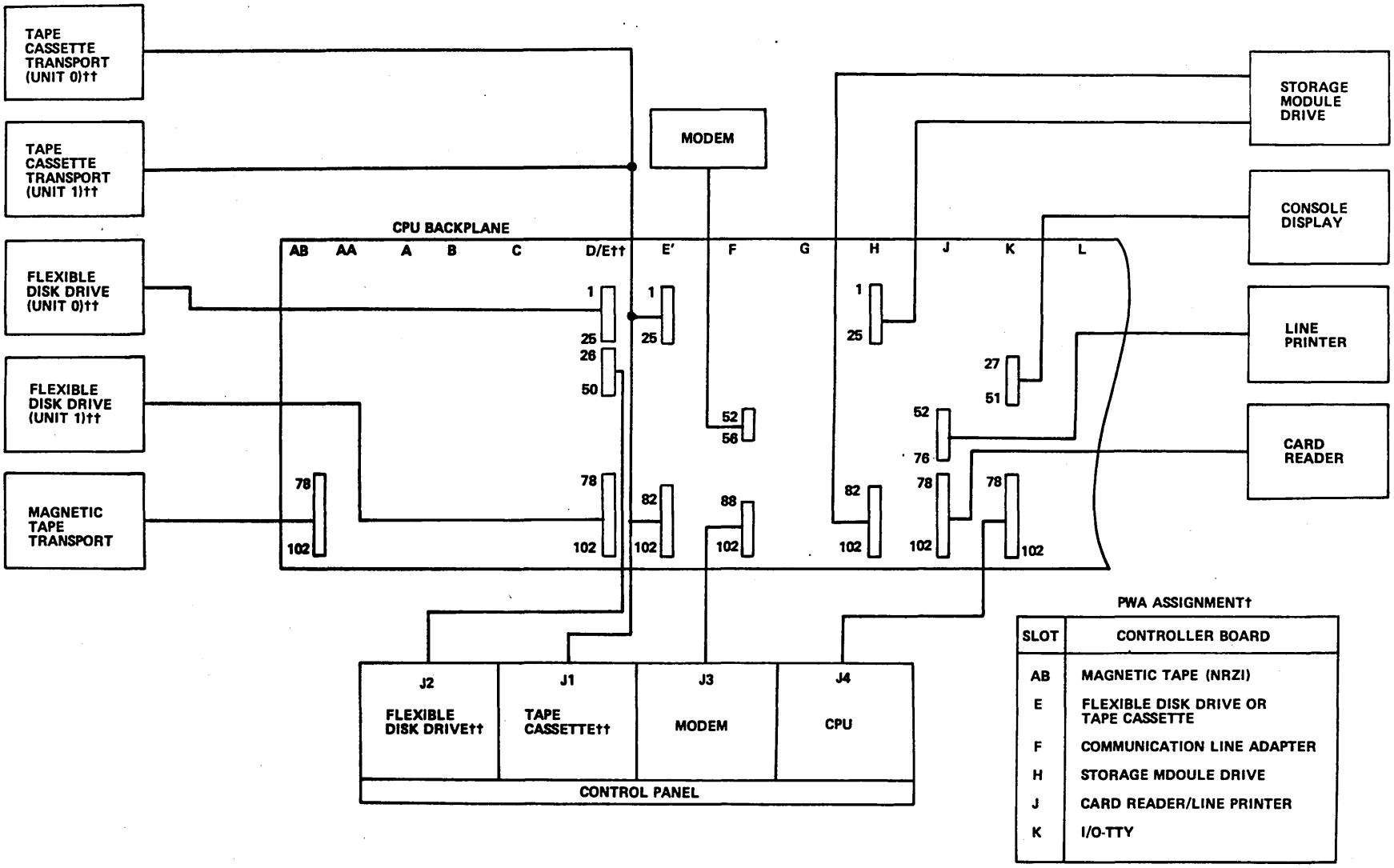


Figure 5-2. Single-Processor MOS Array Address Connectors

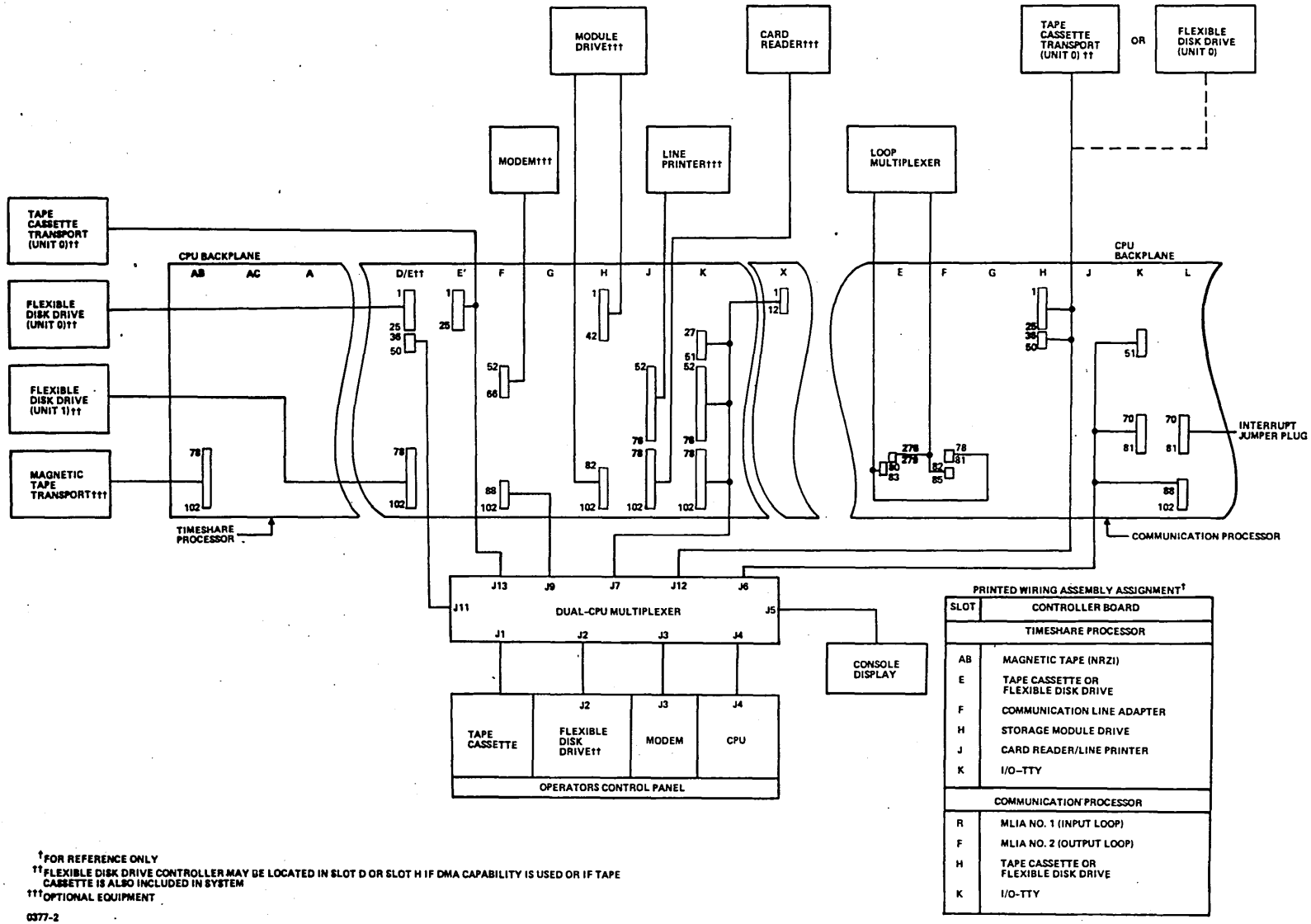


† FOR REFERENCE ONLY

†† FLEXIBLE DISK DRIVE CONTROLLER MAY BE LOCATED IN SLOT D IF DMA CAPABILITY IS USED OR IF TAPE CASSETTE IS ALSO INCLUDED

1224

Figure 5-3. Single-Processor Backplane Cabling



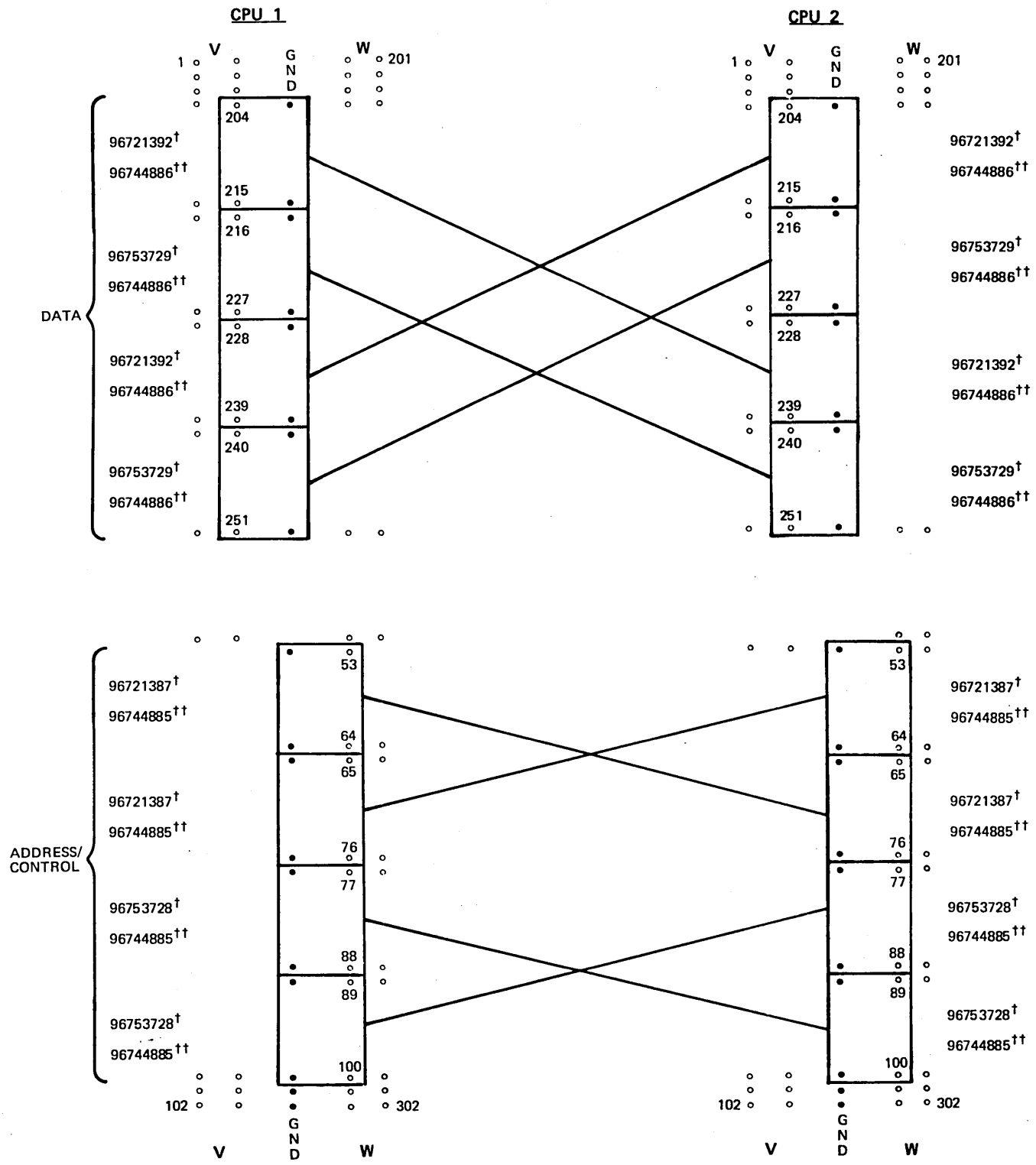
PRINTED WIRING ASSEMBLY ASSIGNMENT†

SLOT	CONTROLLER BOARD
	TIMESHARE PROCESSOR
AB	MAGNETIC TAPE (NRZI)
E	TAPE CASSETTE OR FLEXIBLE DISK DRIVE
F	COMMUNICATION LINE ADAPTER
H	STORAGE MODULE DRIVE
J	CARD READER/LINE PRINTER
K	I/O–TTY
	COMMUNICATION PROCESSOR
R	MLIA NO. 1 (INPUT LOOP)
F	MLIA NO. 2 (OUTPUT LOOP)
H	TAPE CASSETTE OR FLEXIBLE DISK DRIVE
K	I/O-TTY

†FOR REFERENCE ONLY
††FLEXIBLE DISK DRIVE CONTROLLER MAY BE LOCATED IN SLOT D OR SLOT H IF DMA CAPABILITY IS USED OR IF TAPE CASSETTE IS ALSO INCLUDED IN SYSTEM
†††OPTIONAL EQUIPMENT

0377-2

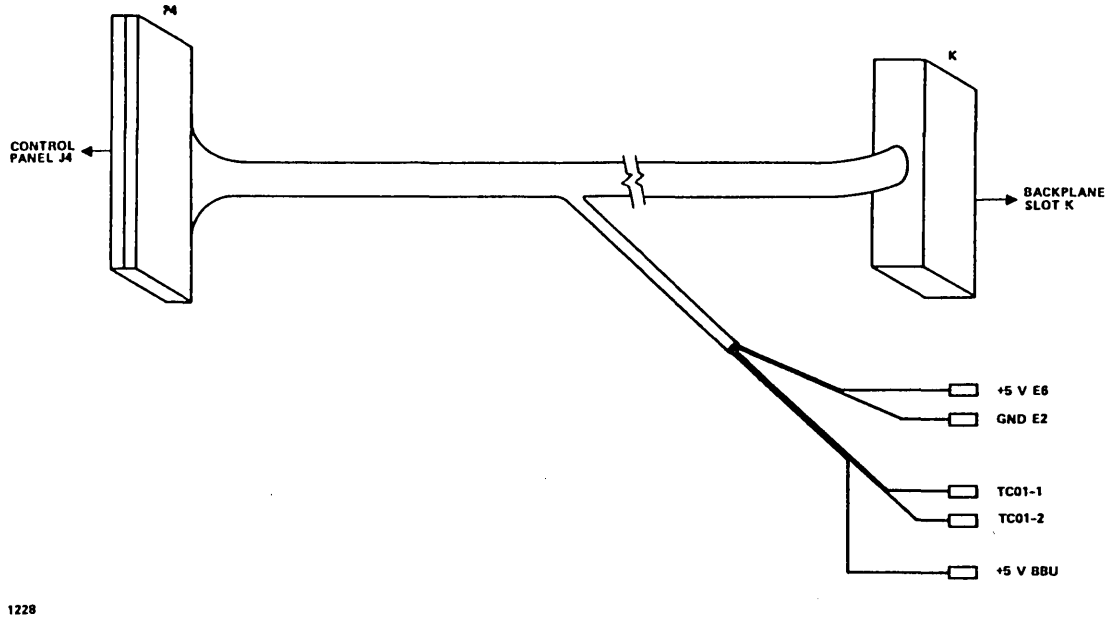
Figure 5-4. Dual-Processor Backplane Cabling



†CABLE ASSEMBLY PART NUMBERS FOR AA155-B, AND AA153-A (SERIES 07 AND UP).
††CABLE ASSEMBLY PART NUMBERS FOR AA133-A/B, AA134-A/B, AND AA153-A (THRU SERIES 06).

5051

Figure 5-5. Dual-Processor Backplane Memory Interface Cabling



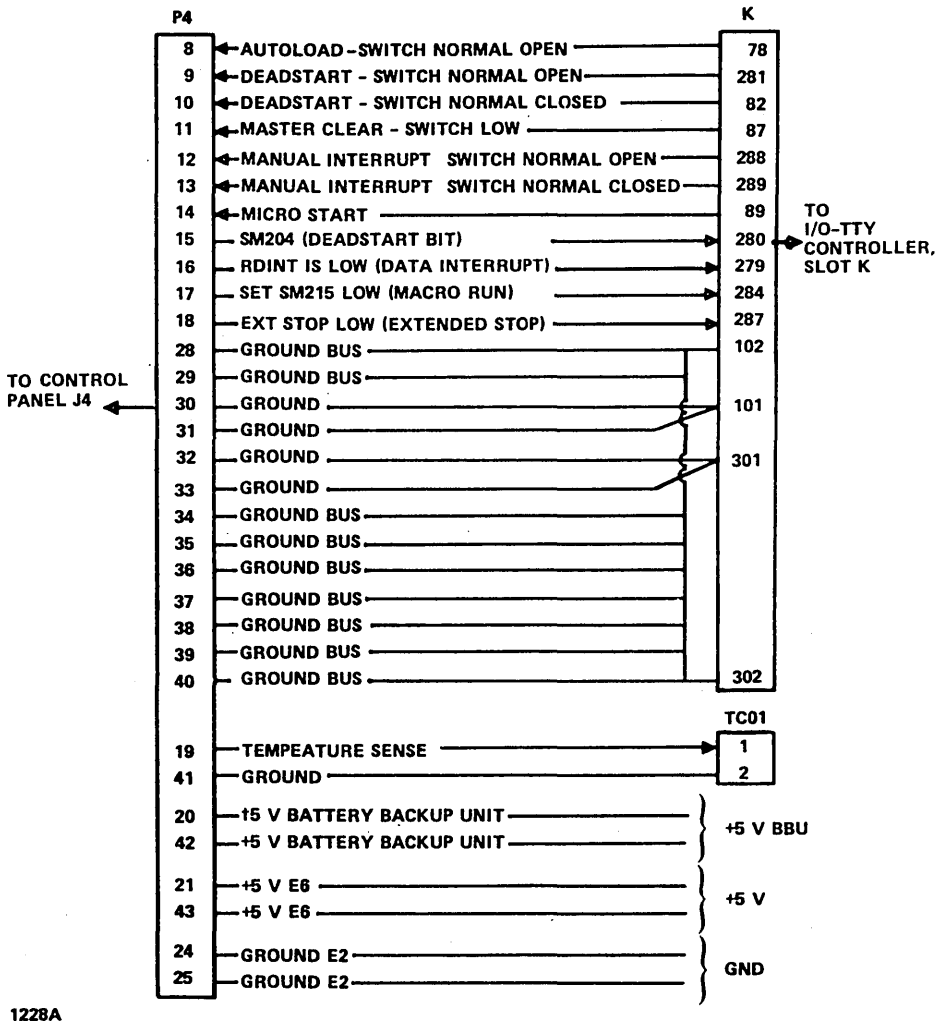


Figure 5-6. Single-Processor Control Panel Interface Cable

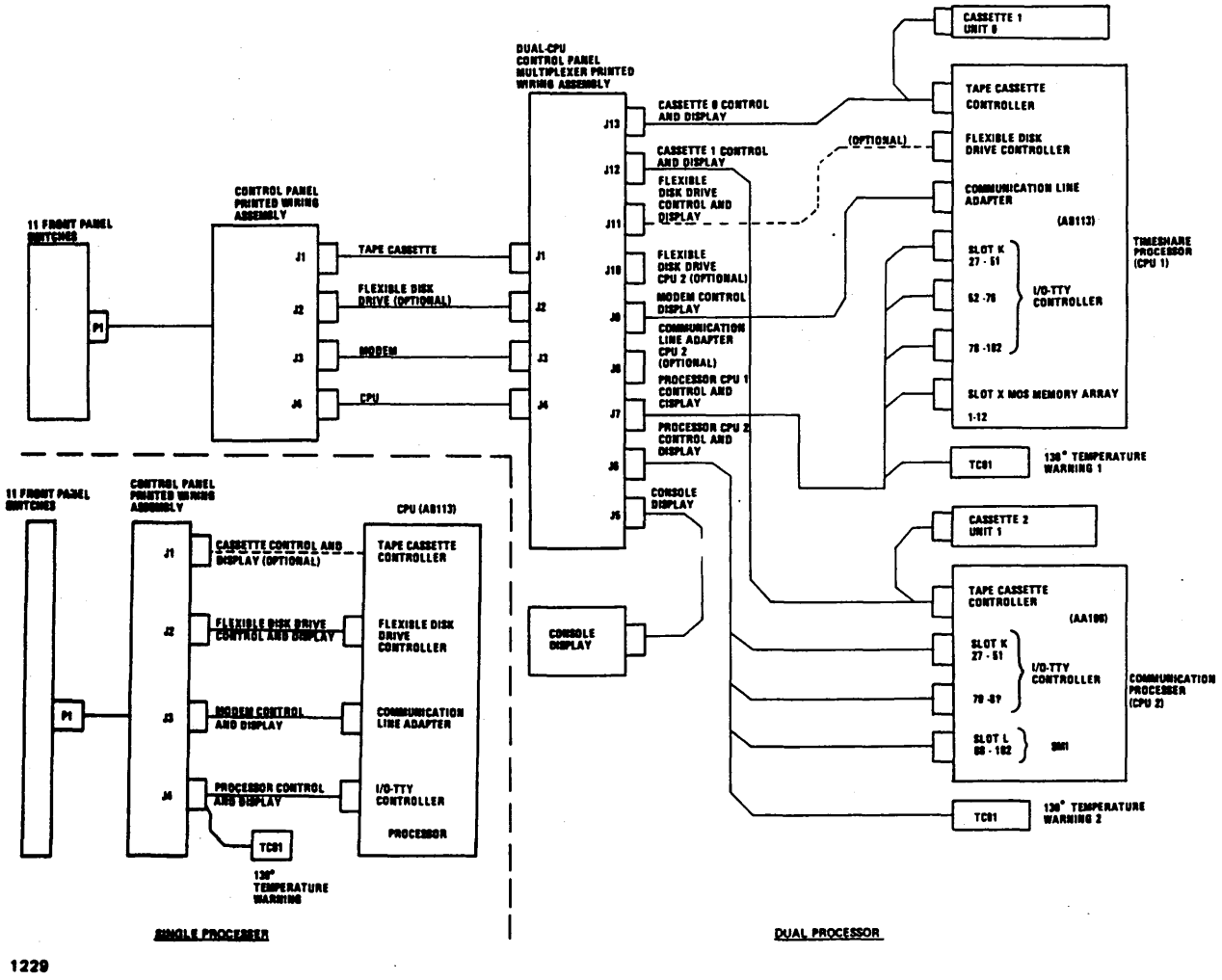
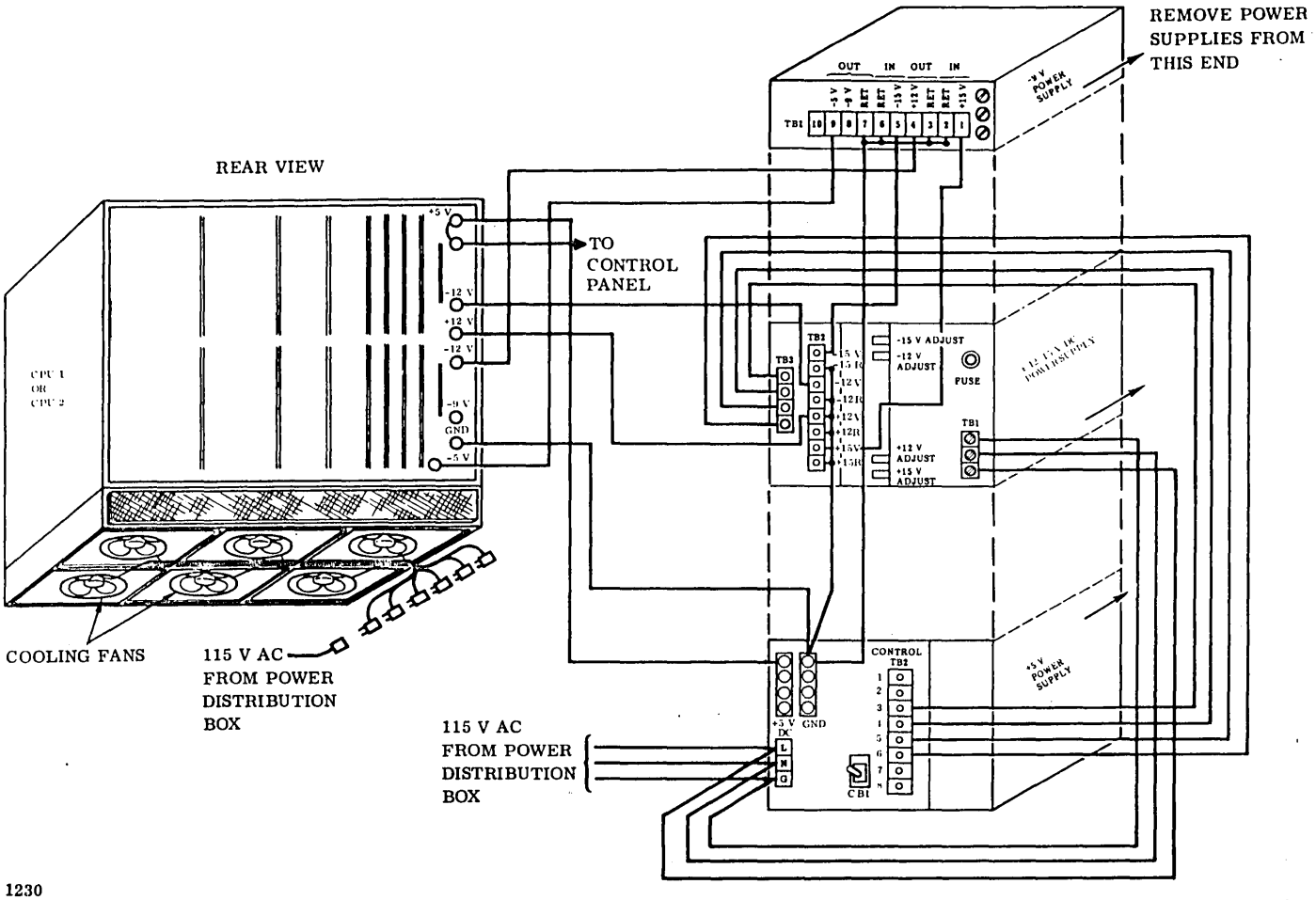
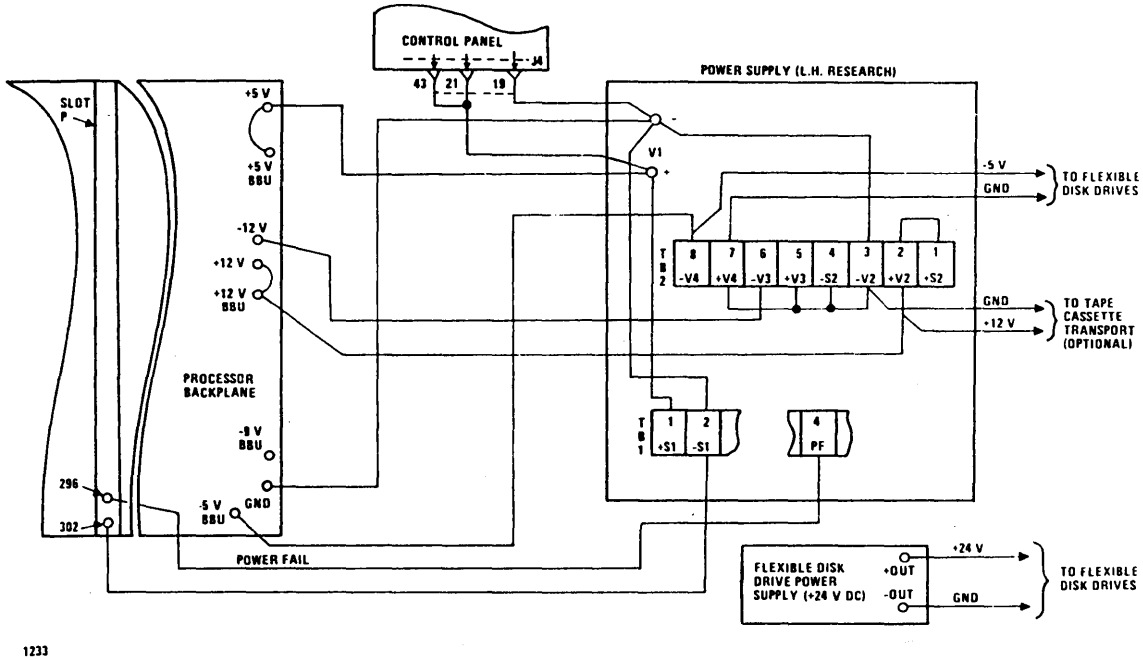


Figure 5-7. Dual-Processor Multiplexer and Control Panel Cabling



1230

Figure 5-8. Power Wiring Diagram (GD122-B Power Supply)



1233

Figure 5-9. Single-Processor Cabinet Dc Power Distribution Diagram

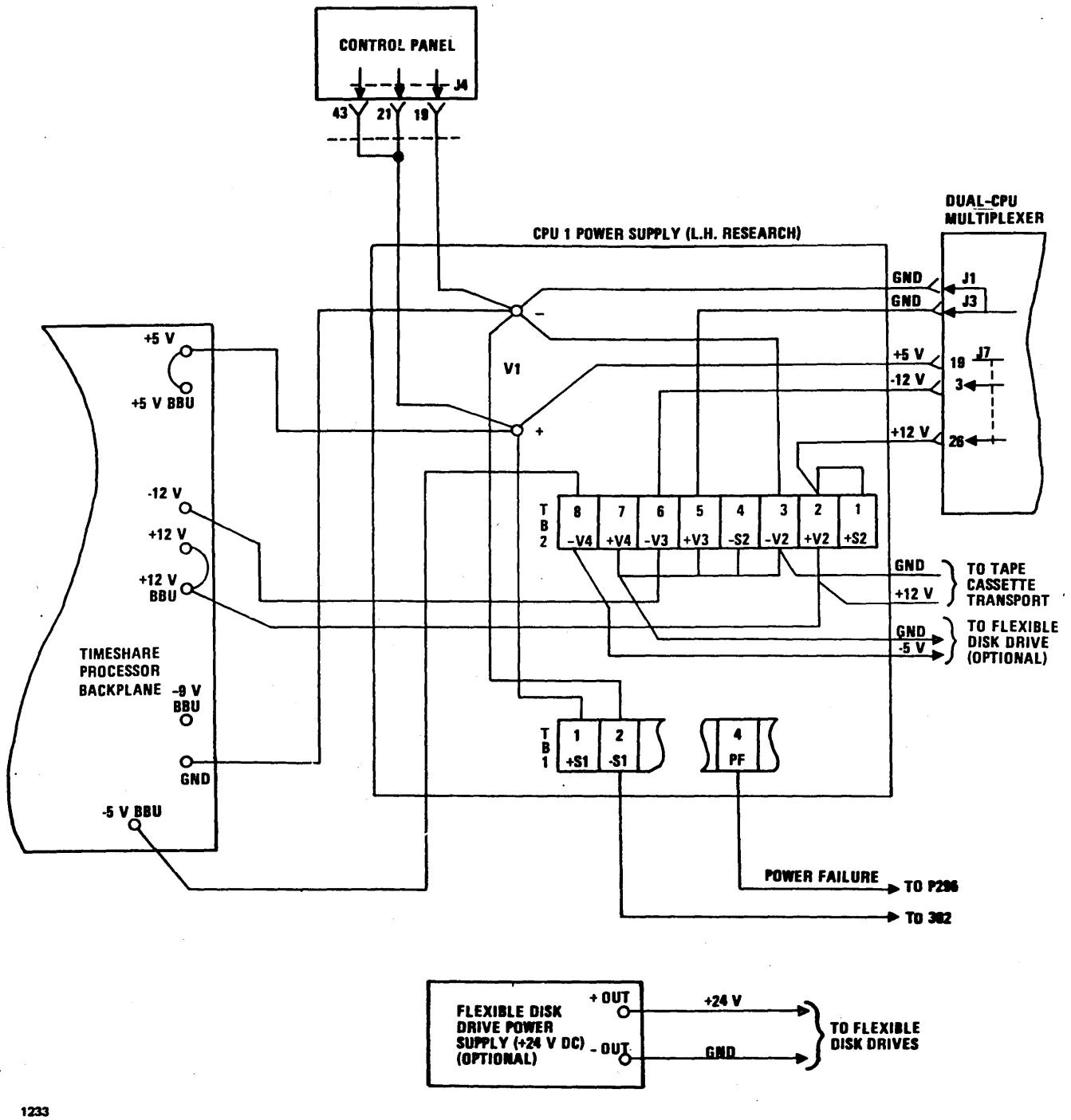


Figure 5-10. Dual-Processor Cabinet Dc Power Distribution Diagram (Sheet 1 of 2)

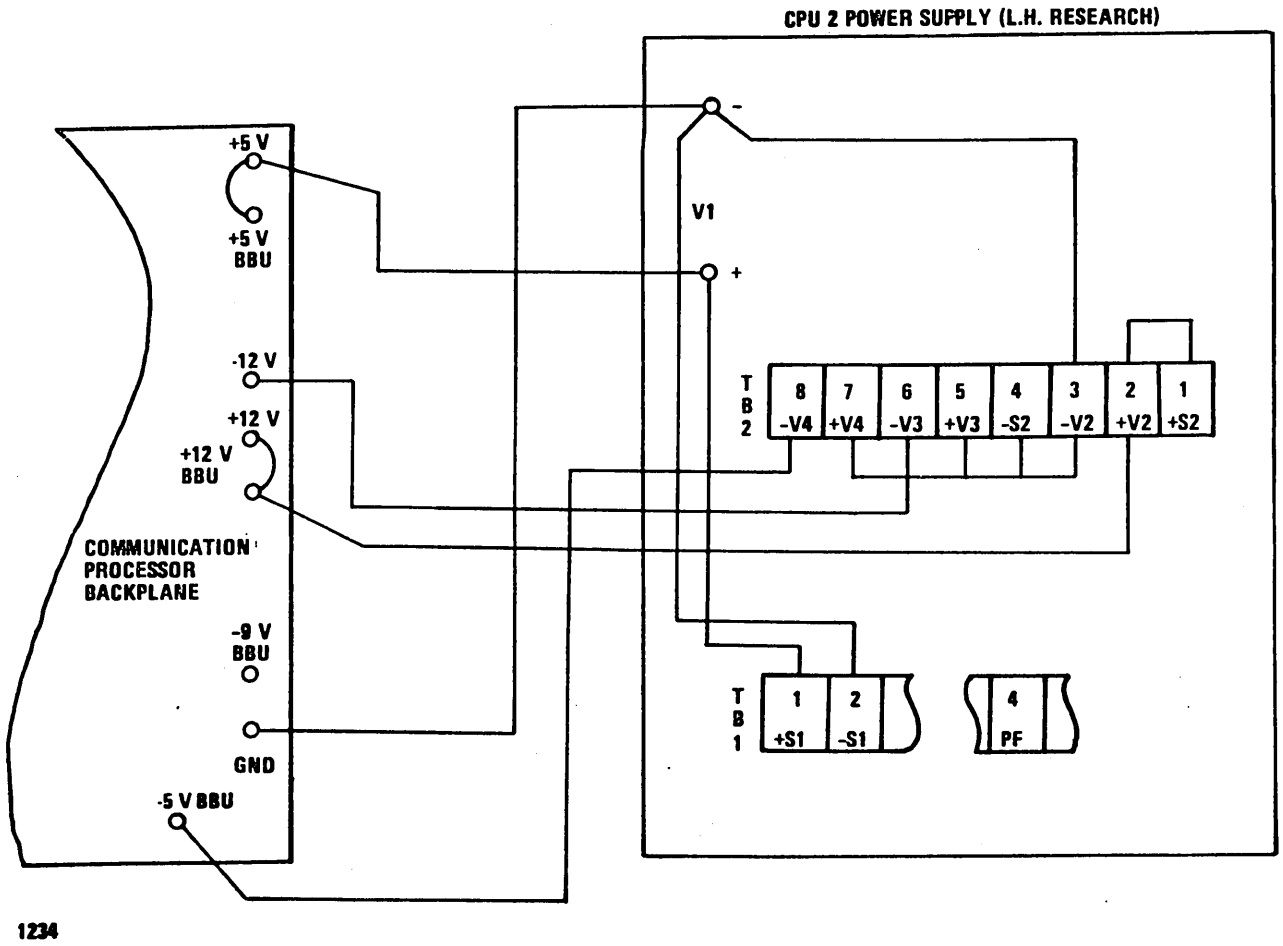


Figure 5-10. Dual-Processor Cabinet Dc Power Distribution Diagram (Sheet 2 of 2)

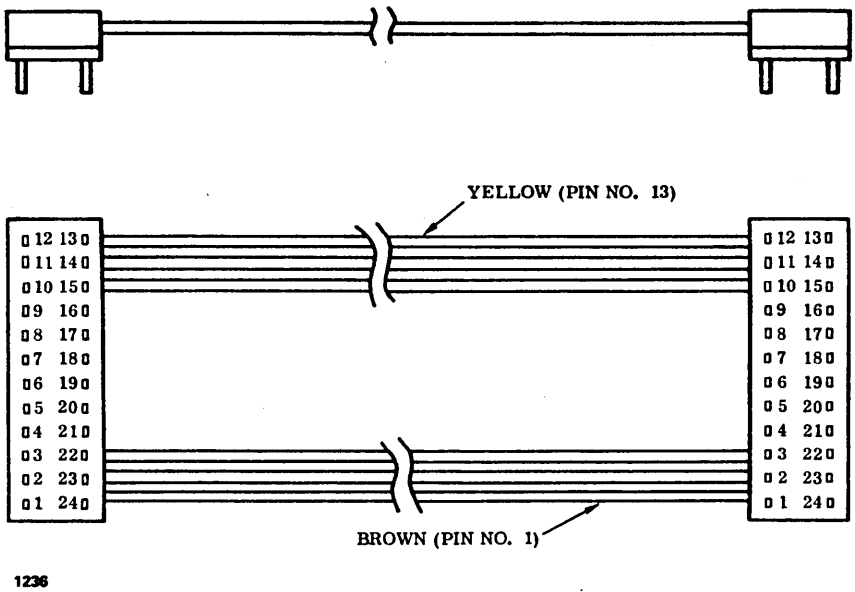


Figure 5-11. Breakpoint Panel - Signal Cable

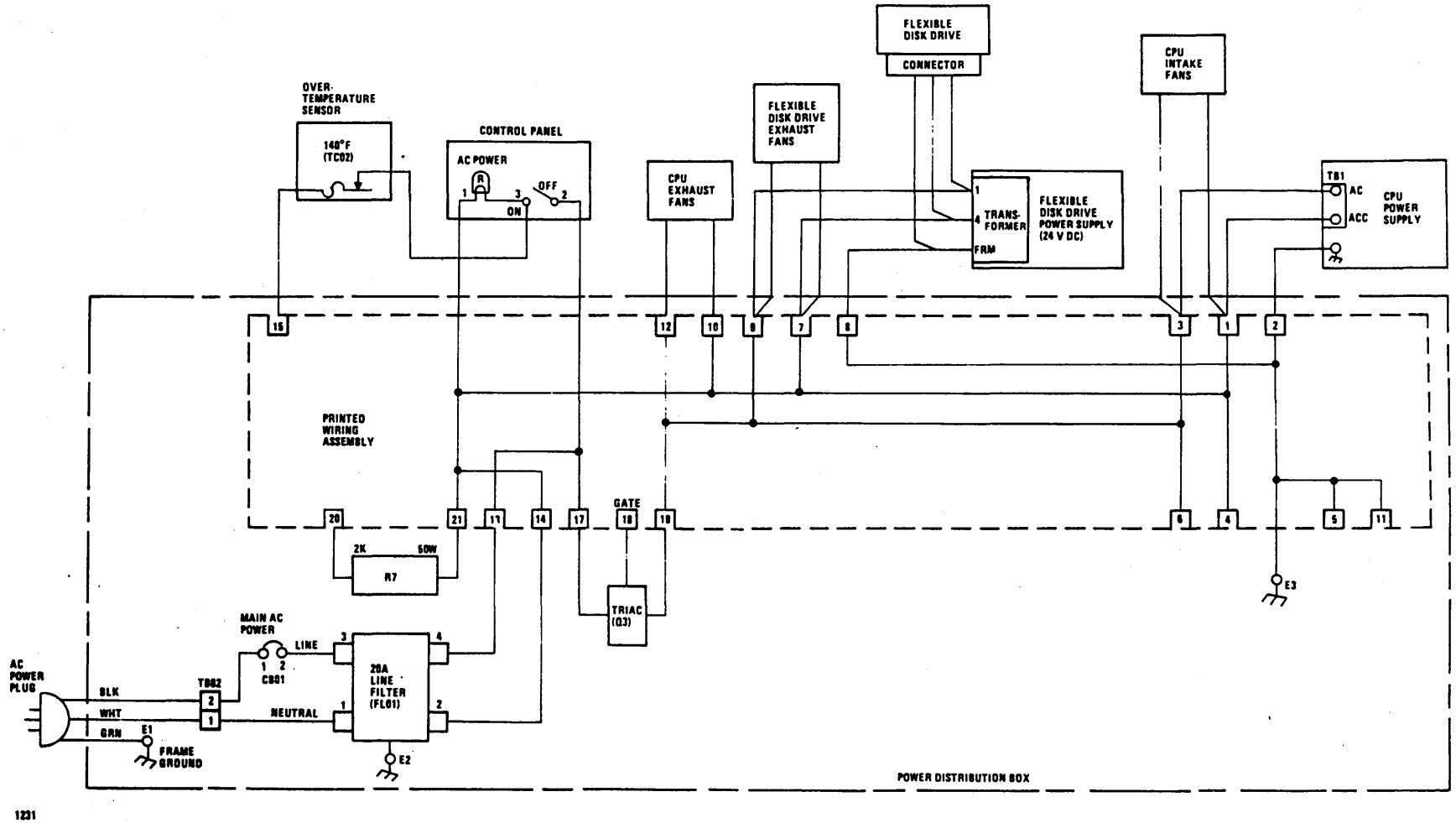


Figure 5-12. Single-Processor Cabinet Ac Power Distribution Diagram

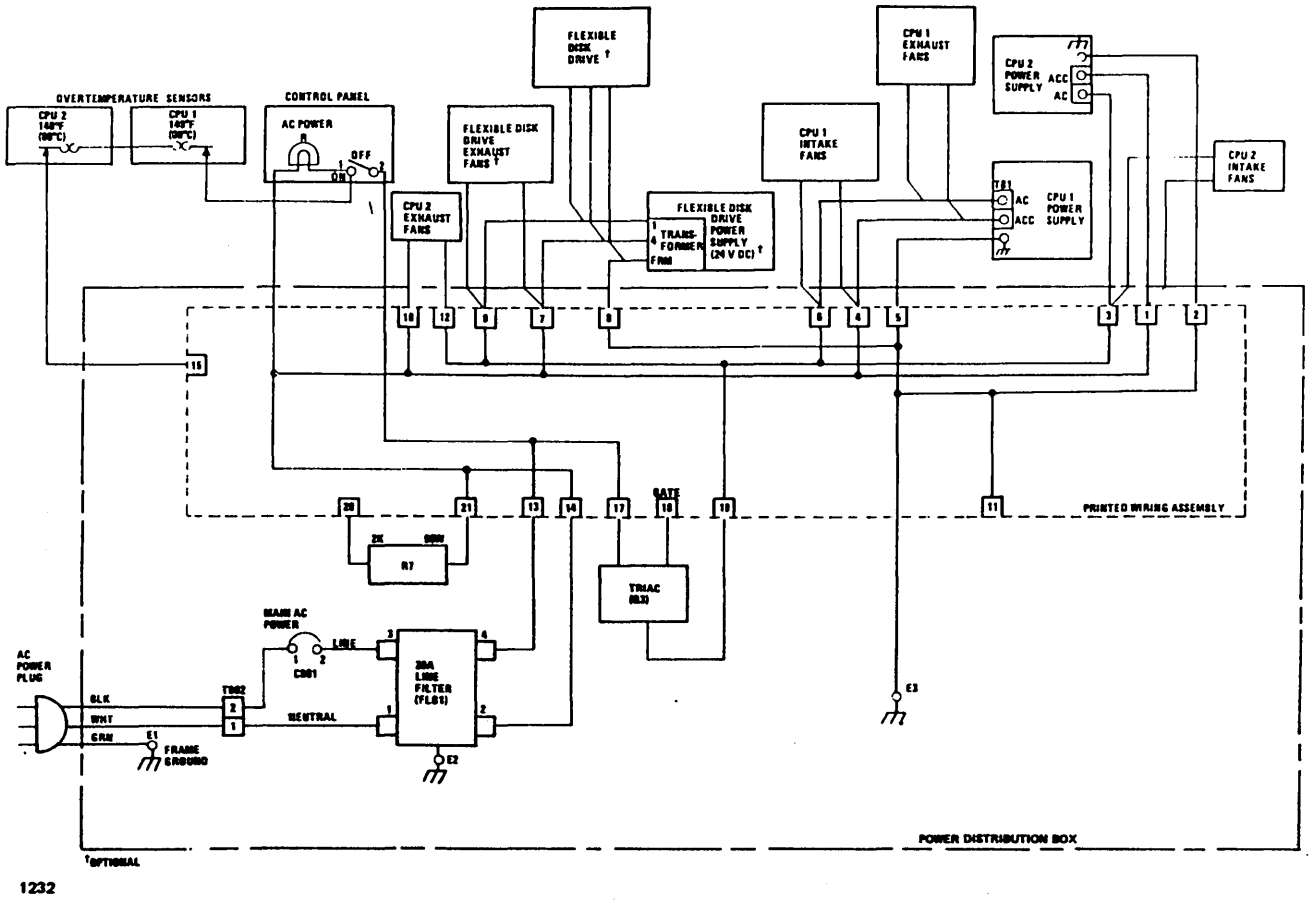


Figure 5-13. Dual-Processor Cabinet Ac Power Distribution Diagram

TABLE 5-1. MICRO/MACRO INTERRUPT WIRE TABLE

Interrupt Number	Type		Source		Destination		Application
	Micro	Macro	Slot	Pin	Slot	Pin	
0	00†		L	227	AB	250	Magnetic tape, auto-data transfer interrupt
1	01		L	27	K	242	Teletypewriter - console display, auto-data transfer interrupt
2	02		L	32			Paper tape reader/punch
3	03		L	332			
4	04		L	28	J	250	Line printer, auto-data transfer interrupt
5	05		L	31			
6	06		L	231			
7	07		L	228	E	250	Tape cassette, auto-data transfer interrupt
8	08		L	30			
9	09†		L	230	AB	250	Magnetic tape, auto-data transfer interrupt
10	10		L	229	H	250	Communication line adapter, auto-data transfer interrupt
10	10		L	229	J	277	Communication line adapter of card reader/line printer/communication line adapter
11	11		L	29	J	50	Card reader, auto-data transfer interrupt
12	12		L	33			
13	13		L	226			
14	14		L	233			
15	15		L	234			
16		00	L	39	R	277	Internal interrupt
17		01	L	269	K	58	I/O-TTY, program interrupt
18		02	L	270	AA	49	CYBER 18/1500 Adapter, paper tape reader/punch, A/Q expansion, dual-channel communication line adapter
19		03	L	70	AA	249	CYBER 18/1500 adapter
20		04	L	72	J	249	Line printer, program interrupt
21		05	L	272	K	75	Timeshare application (dual-processor only)

†Micro interrupts 00 and 09 are tied together by backpanel wiring on the micro interrupt jumper plug assembly.

TABLE 5-1. MICRO/MACRO INTERRUPT WIRE TABLE (Contd)

Interrupt Number	Type		Source		Destination		Application
	Micro	Macro	Slot	Pin	Slot	Pin	
22		06	L	271	C	249	Restart loader
23		07	L	71	E	249	Tape cassette or flexible disk drive, program interrupt
24		08	L	73	K	285	Real-time clock
25		09	L	274	AB	249	Magnetic tape, program interrupt
26		10	L	74	F	249	Communication line adapter, program interrupt
27		11	L	273	J	49	Card reader, program interrupt
28		12	L	277	G	249	Magnetic tape (NRZI/Phase-encoded), program interrupt
29		13	L	276	D	249	Flexible disk drive progrm interrupt
30		14	L	77	H	249	Storage module drive, or cartridge disk drive or flexible disk drive, program interrupt.
31		15	L	275	A	49	BCLA, SDLC, program interrupt

This section contains diagnostic decision logic tables (DDLTs) and corrective action procedures applicable to the single and dual processors. The DDLTs contain troubleshooting procedures that provide fault isolation of equipment malfunctions. The corrective action procedures provide for step-by-step removal and replacement of defective subassemblies.

The DDLT procedures consist of offline test sequences and/or the operational diagnostic system (ODS) tests contained on diskettes or cassette tapes. The ODS tests are used in conjunction with the DDLTs applicable to the subsystem. All ODS tests for a subsystem must use ODS programs contained on the same test medium, either diskettes or cassette tapes. Do not intermix test media during a system checkout.

MAINTENANCE AIDS

Operational diagnostic system (ODS) programs required to test the processor are:

LDCHK	MPRTC
MPINS	MIMEM
MPMOS	MIINS
MOSMA	PAGE1
DUCPU	

For part numbers of the ODS test programs, refer to the overview manual listed in the preface.

DESCRIPTION OF DIAGNOSTIC DECISION LOGIC TABLES (DDLTs)

The DDLTs identify and isolate equipment malfunctions in the replaceable assemblies. The DDLT analyzes a situation down to specific conditions and then directs the customer engineer to those actions that will correct the situation, with the most likely action listed first. The table is arranged in five sections: assumptions, conditions, responses, actions, and sequence of actions (see the DDLT example in figure 6-1).

ASSUMPTIONS

The upper section of the DDLT contains the prerequisites for the specific tests to be performed. The DDLT is valid only if all assumptions are true.

CONDITIONS

The center left section of the DDLT contains the conditions or tests to be made. They are in the form of questions that can be answered yes or no.

RESPONSES

The center right section of the DDLT contains the response to the question asked in the Conditions section. Note that each condition, or question, can be answered with a yes (Y) or a no (N). The example chosen for figure 6-1 has 10 unique situations, numbered from 1 to 10, left to right. The shaded area in the example shows the conditions that define situation 9. That is, the POWER ON indicator does not illuminate, all other indicators do not illuminate when the READ CHECK indicator/switch is pressed, and no single indicator illuminates.

The first condition should be examined for a yes or no response. The applicable response directs the operator to the next condition in the column until all conditions in that column have been analyzed. In figure 6-1, column 1 identifies an everything-is-normal situation for the tests made. Therefore, the Actions section in the lower left of the table directs the customer engineer: Go to sheet 2 of this table. The customer engineer then goes to sheet 2 of the table and does not waste time with further examination of sheet 1.

ACTIONS

The lower left quadrant lists actions to correct a situation.

SEQUENCE OF ACTIONS

The lower right section lists the sequence of the actions required to correct a situation, with each succeeding action being performed only if a previous action failed to correct the condition under test. The sequential numbering of actions reflects the probability of the corresponding action correcting the problem, with the most likely listed first. An X indicates that no sequence of actions is necessary, but the single action listed must be performed. Both actions and conditions may refer to other specific procedures to follow (for example, when checking and adjusting the power supply voltages). The customer engineer must exit from the table to perform the other procedure and then return to the same point in the table to answer any questions that are related to the procedure. He also continues from this point in the table if the fault still persists. The same is true if the customer engineer exits to another table or sheet of the same table but does not find the fault, and the action that called for the exit is not the last action in the sequence. The customer engineer must return to his original DDLT exit point and continue testing from there.

After taking corrective action, the customer engineer should rerun the DDLT starting at sheet 1 to make sure that the fault has been corrected.

USER NOTES

The following are precautions the customer engineer should keep in mind while performing diagnostic testing:

- If the DDLTs are run using a CC628 display terminal, observe the following functional changes when entering information through the keyboard:

To Enter	Press Simultaneously
ETX	CONTROL and C
CLEAR	CONTROL and X
ENTER-	CONTROL and \
ENTER+	CONTROL and [
LINE FEED	SHIFT and ↓

TABLE 6-51. CARD READER DDLT

Power On — Sheet 1 of 6

ASSUMPTIONS:

1. If card reader is load device, go to sheet 2 of this table.
2. Card reader power cord is connected to ac outlet.
3. Power is on (procedure 1).
4. Ensure card reader is not ready by pressing RESET.

(1)

CONDITIONS: (2) →	1	2	3	4	5	6	7	8	9	10
1. Is POWER ON indicator on card reader illuminated/	Y						N			
2. Press READ CHECK switch/indicator. Do all other indicators illuminate?	Y				N		Y	N		
3. Do any indicators illuminate?					Y	N		Y	N	
4. Press and release RESET switch/indicator. Does RESET indicator illuminate?	Y			N					(3)	
5. When RESET switch/indicator is pressed, do stacker springs and/or card drum turn?	Y		N							
6. Did motor power come up and then drop within 10 to 30 seconds after releasing RESET switch/indicator?	Y	N								
ACTIONS:										
1. Go to sheet 2 of this table.	X									
2. Check that toggle switch S1 (rear panel) is up. (5) ← (4)									1	
3. Check that removable power cord is connected securely to card reader.									2	
4. Check fuses (rear panel) and ac power.									3	
5. Check switch board and associated cabling (procedure 9). Replace if requred (procedure 10).				3	2	2	2		4	
6. Check +17-volt power supply (procedure 6).								1		
7. Check for +17 vdc between ground and control board connector P2, pins 2 and 3, and between ground and switch board connector, pins 2 and 3 (two pins joined by foil).								2		
8. Check cable between control board and switch board.								3		
9. Replace lamp in failing indicator (procedure 9).							1			

RESPONSES

SEQUENCE OF ACTIONS

NOTE: ARROWS AND CIRCLED NUMBERS INDICATE SEQUENTIAL FLOW OF ANALYSIS PROCEDURE.

Figure 6-1. Example of a Diagnostic Decision Logic Table

To Enter	Press Simultaneously
CARRIAGE RETURN	CR or NEW LINE
RESET	SHIFT and HOME
RUBOUT	DEL
BEL	CONTROL and G

- After any power to the computer is turned on or off, the computer should be master cleared.
- Power to the peripherals should be turned off before the power to the computer is turned off.
- Do not remove or install MOS memory array printed wiring assemblies in the processor with power applied to the processor logic cage.
- With the exception of the MOS memory array PWAs, the remaining processor and I/O controller PWAs may be removed or installed on the processor cage with power applied.
- Do not press any key on the console display while diagnostic media is being loaded.

Whenever the ESC key on the console display is pressed, the computer is placed into panel mode. This prevents further messages from being displayed on the console display. To a user it appears that the system is hung up. If the ESC key is accidentally pressed, the condition can be rectified by pressing the @ character on the keyboard.

The DDLTs presume all operator inputs are entered correctly. Any incorrect entry may cause the DDLT to direct an incorrect action. Hence, if any doubt exists about the accuracy of the operator entry, always repeat the sequence of DDLT steps that led up to an action before taking further actions.

If any characters are accidentally pressed on the console display, the KEYBOARD LOCK and ALERT lights on the display illuminate. If this occurs, the BREAK key must be pressed to continue.

ODS SOFTWARE

The use of the ODS diagnostic tests is described in the Operational Diagnostic System Reference Manual. The following information is excerpted from that manual.

If an erroneous test entry is made and executed during a level II† test, perform the following:

1. Simultaneously press the CONTROL and BEL keys on the console display.
2. Type in:

   ODS,ABRT,xxxxx

   where xxxxx is the ODS test mnemonic.
3. Press the CARRIAGE RETURN key. The remainder of the test loads.
4. Reload the test and return to the DDLT (sheet 1) of the device under test.

NOTE

If step 2 above cannot be performed, restart the Loadcheck diagnostic.

For error code typeouts not listed in the DDLTs, refer to the following:

Typeout	Description
GHOST INTERRUPT LINES xxxx	Level I tests. An unexpected interrupt was received. xxxx = A bit mask indicating which line was interrupted
MI	Level II tests. A manual interrupt (CONTROL and BEL) has been received, and the system is waiting for the ODS Level II command.
MI INPUT ERROR	Level II tests. The command did not begin with ODS. Press CONTROL and BEL and then re-enter the command.
ODS BUSY	Level II tests. ODS is currently processing the last command entered. Re-enter the command.
ODS ERROR xx	Level II tests. An operator command input error occurred during loading of the test or while the test was not processing. Re-enter the command correctly. xx = 01 Invalid command mnemonic 02 Third field must be entered 03 Invalid test availability 04 Command is not valid for the master parameter list 05 Too many field inputs for the command 06 Nonhexadecimal input 07 Invalid parameter 08 Invalid parameter index 09 Test not currently suspended 10 No change in parameter data input 11 Available memory has been exceeded 12 Test not found on library unit.
OV	Level II tests. An overflow of the monitor's useable memory has occurred. Reload the system.
PE	Level II tests. A macro MOS parity fault interrupt has occurred. Reload the system.
PF	Level II tests. A protect fault interrupt has occurred. Reload the system.
PW	Level II tests. A power failure protect interrupt has occurred. Reload the system.

DIAGNOSTIC DECISION LOGIC TABLES

Tables 6-1 through 6-11 are the DDLTs for the processor subsystem. The removal/replacement and testing procedures immediately follow the DDLTs.

† Level II tests are subsystem diagnostic programs that run under the ODS Monitor DDLT and are loaded by the Level II Monitor DDLT.

TABLE 6-1. LDCHK: LOADCHECK DDLT

ASSUMPTIONS:

1. The system overview manual listed in the preface has been reviewed.
2. The system is plugged into the power outlet.
3. The console display is plugged into the power outlet.
4. Power is turned on at each subsystem.

CONDITIONS:	1	2	3
1. Is this an AA132-A/B/C equipment system (single-processor)?	Y	N	
2. Is this an AA133-A/B or AA153-A equipment system (timeshare or dual-processor)?		Y	N
ACTIONS:			
1. Go to sheet 2 of this table.	X		
2. Go to sheet 3 of this manual.		X	
3. This manual is applicable only to the AA132-A/B/C, or AA133-A/B, or AA153-A equipments. Use the correct manual for the equipment under test.			X

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

1. This is an AA132-A/B/C equipment.
2. MASTER CLEAR on the control panel is pressed.
3. The CLEAR key on the keyboard is pressed to master clear the display (If the KEYBOARD LOCK indicator is illuminated, press the BREAK key to unlock).
4. The following is entered at the keyboard:

   Press ESC key
   Type J58G

CONDITIONS:	1	2	3	4	5	6	7	8
1. Did the screen clear when the CLEAR key on the keyboard was pressed?	Y							N
2. Does the screen display:								
J000008x0 or J000008x8	Y	N						
Jxxxxxxx1		Y	N					
Jxxxxxxx2			Y	N				
Jxxxxxxx4				Y	N			
Jxxxxxx8x					Y	N		
Jxxxxxxxx or *Jxxxxxxxx						Y	N	
where x may equal any number.								
ACTIONS:								
1. Go to sheet 4 of this table.	X							
2. Replace ALU, slot M (procedure 23).		1	7	7	5	6	4	
3. Replace breakpoint controller, slot U, if present (procedure 23).		2	6	5	3	2	10	
4. Replace SMI, slot L (procedure 23).		3	8	8	4	7	9	
5. Replace transform, slot R (procedure 23).		4	1	1	6	5	7	
6. Replace memory interface (data), slot V (procedure 25).		5	2	2	9	10	11	
7. Replace memory interface (address), slot W (procedure 25).		6	3	3	10	11	12	
8. Replace control 1, slot P (procedure 23).		7	9	9	1	4	5	
9. Replace control 2, slot N (procedure 23).		8	10	10	7	3	6	
10. Replace memory, slot X (procedure 24).		9	5	6	8	9	13	
11. Replace I/O-TTY, slot K (procedure 23).		10	4	4	2	8	8	3
12. Go to table 6-11.		11	11	11	11	12	14	

Continued on next page

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

Sheet 2 of 10 (Contd)

ACTIONS (Continued):		1	2	3	4	5	6	7	8
13.	Verify the power supplies (procedures 7, 9, and 11).							3	
14.	Ensure SHIFT LOCK on keyboard is released. Restart this sheet.						1		
15.	Check cabling to control panel PWA (figure 5-2).								1
16.	Replace control panel PWA (procedure 20).								4
17.	Run console display offline test. Refer to the console display subsystem manual listed in the preface if the console display is a CC614 equipment. If the console display is a CC555 equipment, go to the CRT1 table in the keyboard display terminal subsystem manual and perform the specified tests and checks.							2	2
18.	Verify that the baud rate switches on the I/O-TTY controller are set properly (figure 4-3).							1	
19.	Call next level of support.								5

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

1. Entry is made from sheet 1 of this table.
2. This is an AA133-A/B or AA153-A equipment (dual-processor).
3. The processor to be tested is selected by pressing PANEL SELECT on the control panel.
4. Tests are performed first on CPU 1. After completion of all Level I tests on CPU 1, tests must be performed on CPU 2.
5. MASTER CLEAR on the control panel is pressed.
6. The CLEAR key on the keyboard is pressed to master clear the display. (If the KEYBOARD LOCK indicator is illuminated, press the BREAK key to unlock.)
7. The following is entered at the keyboard:

   Press ESC key
   Type J58G

CONDITIONS:	1	2	3	4	5	6	7	8	9
1. Can the CPU be selected as in assumption 3?	Y								N
2. Did the screen clear when the CLEAR key on the keyboard was pressed?	Y							N	
3. Does the screen display:									
J000008x0 or J000008x8	Y	N							
Jxxxxxxx1		Y	N						
Jxxxxxxx2			Y	N					
Jxxxxxxx4				Y	N				
Jxxxxxx8x					Y	N			
Jxxxxxxxx or *Jxxxxxxxx						Y	N		
where x may equal any number.									
ACTIONS:									
1. Go to sheet 4 of this table.	X								
2. Replace ALU, slot M (procedure 23).		1	7	7	5	6	6		
2. Replace breakpoint controller, slot U, if present (procedure 23).		2	6	5	3	2	10		
4. Replace SMD, slot L (procedure 23).		3	8	8	4	7	9		
5. Replace transform, slot R (procedure 23).		4	1	1	6	5	7		
6. Replace memory interface (data), slot V (procedure 25).		5	2	2	9	10	11		
7. Replace memory interface (address), slot W (procedure 25).		6	3	3	10	11	10		
8. Replace control 1, slot P (procedure 23).		7	9	9	1	4	5		
9. Replace control 2, slot N (procedure 23).		8	10	10	7	3	4		
10. Replace memory, slot X (procedure 24).		9	5	6	8	9	12		
11. Replace I/O-TTY, slot K (procedure 23).		10	4	4	2	8	8	4	

Continued on next page

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ACTIONS (Continued):		1	2	3	4	5	6	7	8	9
12.	Go to table 6-11.		11	11	11	11	12	13		
13.	Ensure that SHIFT LOCK on the keybaord is released. Restart this sheet.						1			
14.	Verify the power supplies (procedures 7, 9, and 11).							3		
15.	Check cabling to the control panel and multiplexer (figure 5-5).								1	1
16.	Replace dual-processor multiplexer PWA (procedure 22).								2	2
17.	Replace control panel PWA (procedure 20).								3	3
18.	Run the console display offline test. Refer to the console display subsystem manual listed in the preface if this is a CC614 equipment. If the equipment is a CC555, go to the CRT1 table in the keyboard display subsystem manual and perform the specified tests and checks.							2		
19.	Verify that the baud rate switches on the I/O-TTY controller are set properly.							1		
20.	Call next level of support.								5	4

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 2 or sheet 3 of this table.

CONDITIONS:		1	2	3
1.	Is the load device a flexible disk?	Y	N	
2.	Is the load device a cassette?		Y	N
ACTIONS:				
1.	Go to sheet 5 of this table.	X		
2.	Go to sheet 6 of this table.		X	
3.	The Loadcheck diagnostic load device must be either a flexible disk or cassette. Restart this sheet with one of these load devices.			X

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

1. Insert the ODS Level I diskette into the unit 0 flexible disk drive (refer to the diskette loading procedure in the flexible disk drive subsystem manual listed in the preface).
2. Close the door of the unit.

CONDITIONS:	1	2	3	4
1. Is the UNIT REV. indicator on the control panel illuminated?	Y	N		
2. Is the WRITE ENAB. indicator on the control panel illuminated?		Y	N	
3. Press the DEADSTART switch. Does the DEADSTART indicator illuminate?			Y	N
ACTIONS:				
1. Press UNIT REV. switch. Return to Condition 1 if UNIT REV. indicator is now extinguished.	1			
2. Check cabling to control panel (figure 5-2 or 5-3).	2	2		
3. Replace control panel PWA (procedure 20).	3	3		
4. Press WRITE ENAB. switch. Return to Condition 2 if WRITE ENAB. indicator is now extinguished.		1		
5. Go to sheet 7 of this table.			X	
6. Restart this sheet. An operator error has probably occurred.				1
7. Use another diskette, if available.				2
8. Use another load device, if available. (Go to sheet 1 of this table.)				3
9. Replace flexible disk controller, slot D or E (procedure 23).				4
10. Replace SMI, slot L (procedure 23).				5
11. Replace breakpoint controller, slot U, if present (procedure 23).				6
12. Replace flexible disk drive (refer to the flexible disk drive subsystem manual).				7
13. Call next level of support.	4	4		8

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

1. Entry is made from sheet 4 of this table.
2. Read the Conditions below before going to the next assumption.
3. Insert the Level I cassette tape into the respective processor or tape cassette transport unit if this is a dual-processor system. Otherwise, insert tape into unit 0.
4. Close the lid and observe whether the cassette spools move in both directions, first rewinding and then loading to beginning of tape.

CONDITIONS:	1	2	3	4	5	6
1. Did the tape move in both directions?	Y				N	
2. Did the tape move in only one direction?					Y	N
3. After approximately five seconds, did the cassettte READY indicator illuminate?	Y			N		
4. Press DEADSTART switch. Does the DEADSTART indicator illuminate?	Y	N				
5. Did tape attempt to load?		Y	N			
ACTIONS:						
1. Go to sheet 7 of this table.	X					
2. Use another tape, if available.		3	2	2	1	1
3. Check cassette power supply voltages (refer to the tape cassette subsystem manual listed in the preface).					2	2
4. Replace the cassette drive (refer to the tape cassette subsystem manual).		6	7	5	3	6
5. Replace the cassette controller, slot E of CPU 1 or slot H of CPU 2 (procedure 23).		4	3	4	4	5
6. Restart this sheet. An operator error has occurred.		1				
7. Verify that the system is 9600 baud (refer to the tape cassette subsystem manual). If the system is not 9600 baud, set it to 9600 baud. If the system is 9600 baud, continue to the next action.		2				
8. Replace I/O-TTY, slot K (procedure 23).		5				
9. Replace SMI, slot L (procedure 23).		7	4			
10. Replace breakpoint controller, slot U, if present (procedure 23).		8				
11. Check power distirbution box (procedure 13).						3
12. Verify the processor power supplies (procedures 7, 9, and 11).						4
13. Call next level of support.		9	9	7	5	7

Continued on next page

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

Sheet 6 of 10 (Contd)

ACTIONS (Continued):	1	2	3	4	5	6
14. Ensure that the cassette tape has been inserted into the correct drive unit and the processor selected is correct.			1	1		
15. Check that cables on the control panel and multiplexer PWA, if present, are properly connected (figure 5-5).			5	3		
16. Replace dual-processor multiplexer PWA, if present(procedure 22).			8	6		
17. Replace control panel PWA (procedure 20).			6			

TABLE 6-1. LDCHK: LOAD CHECK DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 5 or 6 of this table.

CONDITIONS:	1	2	3	4	5	6	7	8
1. Does the screen display the following after approximately two minutes):								
123456 DPSR LEVEL XX RELEASED DATE MM/DD/YY	Y		N					
12345			Y	N				
1234				Y	N			
123					Y	N		
12						Y	N	
1							Y	N
2. Have all other deadstart devices on the system for which diagnostic load media are available been used?	Y	N						
ACTIONS:								
1. Go to table 6-2.	X							
2. Set up and deadstart system using another load device. Return to sheet 1.		X	2	2	2	2	2	2
3. Use another diskette or cassette tape, if available, and restart.			1	1	1	1	1	1
4. Replace memory, slot X (procedure 24).			3	7	3		3	
5. Replace memory interface (data), slot V (procedure 25).			4	8	4		4	
6. Replace memory interface (address), slot W (procedure 25).			5	9	5		5	
7. Replace ALU, slot M (procedure 23).			6	6	7		7	
8. Replace transform, slot R (procedure 23).			7	5	10		8	
9. Replace SMI, slot L (procedure 23).			8	10	8		6	

Continued on next page

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

Sheet 7 of 10 (Contd)

ACTIONS (Continued):		1	2	3	4	5	6	7	8
10.	Replace I/O-TTY, slot K (procedure 23).			9	3	9		9	
11.	Replace breakpoint controller, slot U, if present (procedure 23).								3
12.	Replace load device controller: cassette (slot E) or flexible disk controller (slot D or E). (See procedure 23.)				4				
13.	Go to sheet 8 of this table.						3		6
14.	Go to table 6-1 and replace any controller not replaced by a prior action.			10	11	14		10	
15.	Call next level of support.				12				
16.	Checkcables on control panel and multiplexer PWAs (figures 5-2 through 5-5).					11			
17.	Replace multiplexer PWA (procedure 22).					12			
18.	Replace control panel PWA (procedure 20).					13			
19.	Replace ECC array logic, slot AC (procedure 24).					6			5
20.	Run the console display offline test. Refer to the console display subsystem manual if the equipment is a CC614. Go to the CRT1 table in the keyboard display terminal subsystem manual if the equipment is a CC555 and perform the specified test and checks.								4

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

The following is entered on the keyboard:

Press ESC
Type J11G

(If the amber KEYBOARD LOCK indicator is on, press the blue BREAK key before completing the above.)

CONDITIONS:	1	2	3	4	5	6	7
1. Is RUN indicator illuminated?	Y	N					
2. Does the screen display:							
Jxxxxxxx0 or Jxxxxxxx1		Y	N				
Jxxxxxxx2 or Jxxxxxxx4			Y	N			
Jxxxxxxx6				Y	N		
Jxxxxxxx8 or JxxxxxxxC or Jxxxxxxx9					Y	N	
JxxxxxxxE						Y	N
where x may equal any number.							
ACTIONS:							
1. Go to sheet 9 of this table.		X					
2. Replace transform, slot R (procedure 23).	1		3	1	8	3	1
3. Replace memory interface (data), slot V (procedure 25).	5		4	2	3	1	4
4. Replace memory interface (address), slot W (procedure 25).	6		5	3	4	2	5
5. Replace memory, slot X (procedure 24).	4		8	5	2	4	3
6. Replace ALU, slot M (procedure 23).	3		1	6	7	7	6
7. Replace SMI, slot L (procedure 23).	2		2	7	5	6	2
8. Replace control 1, slot P (procedure 23).	8		6	8	9	8	7
9. Replace control 2, slot N (procedure 23).	9		7	9	10	9	8
10. Replace I/O-TTY, slot K (procedure 23).	7		9	4	6	5	9
11. Clear memory parity error (procedure 34).					1		
12. Replace micro memory, slot T (procedure 23).	10		10	10	11	10	10
13. Replace micro memory, slot S (procedure 23).	11		11	11	12	11	11
14. Check cables on control panel and multiplexer PWAs (figures 5-2 through 5-5).	12		12	12	13	12	12
15. Replace multiplexer PWA (procedure 22).	13		13	13	14	13	13
16. Replace control panel PWA (procedure 20).	14		14	14	15	14	14
17. Go to table 6-11.	15		15	15	16	15	15

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

1. KG is typed in at the keyboard.
2. Observe the console display for one of the following conditions.

CONDITIONS:	1	2	3	4	5	6	7	8	9	10	11	12
Does the screen display:												
1. K0056 or K0059 or K005C	Y	N										
2. K1003 or K1006 or K1009		Y	N									
3. K100C			Y	N								
4. K100F or K1011 or K1013 or K1015				Y	N							
5. K101A					Y	N						
6. K101C or K101E or K1020 or K1022 or K1024 or K1026						Y	N					
7. K1029							Y	N				
8. K102C								Y	N			
9. K102F									Y	N		
10. K1032										Y	N	
11. K1035											Y	N
ACTIONS:												
1. Replace memory, slot X (procedure 24).	1	6	6	4	5	7	6	6	6	6	6	
2. Replace memory interface (data), slot V (procedure 25).	2	7	7	8	8	4	8	7	8	7	7	
3. Replace memory interface (address), slot W (procedure 25).	3	8	8	9	9	5	9	8	9	8	8	
4. Replace SMI, slot L (procedure 23).	4	5	5	2	2	2	4	4	4	5	4	
5. Replace ALU, slot M (procedure 23).	5	2	3	3	3	3	3	3	3	3	3	
6. Replace transform, slot R (procedure 23).	6	1	4	5	4	6	1	5	1	4	5	
7. Replace control 2, slot N (procedure 23).	7	3	2	7	7	9	7	2	7	1	2	
8. Replace control 1, slot P (procedure 23).	8	4	1	6	6	8	2	1	2	2	1	
9. Replace I/O-TTY, slot K (procedure 23).	9	9	9	1	1	1	5	9	5	9	9	
10. Replace micro memory slot T (procedure 23).	10	10	10	10	10	10	10	10	10	10	10	
11. Replace micro memory, slot S (procedure 23).	11	11	11	11	11	11	11	11	11	11	11	
12. Check cables on control panel and multiplexer PWAs (figures 5-2 through 5-5).	12	12	12	12	12	12	12	12	12	12	12	
13. Replace multiplexer PWA (procedure 22).	13	13	13	13	13	13	13	13	13	13	13	
14. Replace control panel PWA (procedure 20).	14	14	14	14	14	14	14	14	14	14	14	
15. Go to table 6-11.	15	15	15	15	15	15	15	15	15	15	15	
16. Go to sheet 10 of this table.												X

TABLE 6-1. LDCHK: LOADCHECK DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2	3	4	5	6	7	8	9	10	11	12
Does the screen display:												
1. K1038 or K103B or K103E or K1041	Y	N										
2. K1044		Y	N									
3. K1047 or K104A or K104D or K1050 or K1053			Y	N								
4. K1056 or K1059 or K105C				Y	N							
5. K1073 or K1076 or K1079 or K107B or K107C or K107E or K107F					Y	N						
6. K1081 or K1082 or K1084 or K1085 or K1087 or K1088 or K108A						Y	N					
7. K108C							Y	N				
8. K108D or K1090								Y	N			
9. K1094 or K10DA									Y	N		
10. K10D5										Y	N	
11. K10D7 or K10E0 or K10E2											Y	N
ACTIONS:												
1. Replace transform, slot R (procedure 23).	1	5	1	6	1	1	4	1	4	3	4	1
2. Replace control 1, slot P (procedure 23).	2	1	2	8	4	4	3	4	1	2	1	3
3. Replace ALU, slot M (procedure 23).	3	3	3	5	2	2	2	2	2	1	2	4
4. Replace SMI, slot L (procedure 23).	4	4	4	4	5	5	5	5	5	5	5	5
5. Replace I/O-TTY, slot K (procedure 23).	5	9	5	9	9	9	9	9	9	9	9	9
6. Replace memory, slot X (procedure 24).	6	6	6	1	6	6	6	6	6	6	6	6
7. Replace control 2, slot N (procedure 23).	7	2	7	7	3	3	1	3	3	4	3	2
8. Replace memory interface (data), slot V (procedure 25).	8	7	8	2	7	7	7	7	7	7	7	7
9. Replace memory interface (address), slot W (procedure 25).	9	8	9	3	8	8	8	8	8	8	8	8
10. Replace micro memory, slot T (procedure 23).	10	10	10	10	10	10	10	10	10	10	10	10
11. Replace micro memory, slot S (procedure 23).	11	11	11	11	11	11	11	11	11	11	11	11
12. Check cables on control panel and multiplexer PWAs (figures 5-2 through 5-5).	12	12	12	12	12	12	12	12	12	12	12	12
13. Replace multiplexer PWA (procedure 22).	13	13	13	13	13	13	13	13	13	13	13	13
14. Replace control panel PWA (procedure 20).	14	14	14	14	14	14	14	14	14	14	14	14
15. Go to table 6-11.	15	15	15	15	15	15	15	15	15	15	15	15

TABLE 6-2. MPINS: INSTRUCTION TEST DDLT

ASSUMPTIONS:

1. For the remaining testing in tables 6-2 through 6-9 and all subsystems, all tests must be loaded from the same load device that the Loadcheck DDLT is loaded from. This requires a full set of diagnostics on either diskette or cassette.

2. After xxxxx? is displayed, the following is entered at the keyboard (if xxxxx is not displayed, go to table 6-10).

   Type MPINS
   Press CARRIAGE RETURN

   NOTE: xxxxx = test name

3. Observe the console display for the following conditions.

CONDITIONS:	1	2	3	4
1. Does the screen display: MPINS EXECUTING MPINS SUSPENDED BOT	Y		N	
2. Is the RUN indicator illuminated?			N	Y
3. Is the equipment one of the following? AA132-A or AA133-A with STO10428-1 installed or AA132-B/C or AA133-B or AA153-A	Y	N		
ACTIONS:				
1. Enter the following at the keyboard: Type GO Press CARRIAGE RETURN	1			
2. Go to sheet 2 of this table.	2			
3. Enter the following at the keyboard: Type 5, 9000 Press CARRIAGE RETURN Type B,0 Press CARRIAGE RETURN Type GO Press CARRIAGE RETURN		1		
4. Go to sheet 4 of this table.		2		
5. Replace control panel PWA (procedure 20).			1	
6. Go to table 6-11.			2	X

TABLE 6-2. MPINS: INSTRUCTION TEST DDLT (Contd)

ASSUMPTIONS:

1. System under test has a 1700 Emulator, version D or E.

   NOTE: Pertains to transform PWA's part numbers:

   96752129 96751081
   96752604 96720404
   96735700
   96837727

CONDITIONS:	1	2
1. Does the screen display the following: SET MULTI-LEVEL INDIRECT SWITCH OFF (ESC J40@GO CR) MPINS SUSPENDED SELF	Y	N

ACTIONS:		
1. Enter the following at the keyboard: Press ESC Type J40@GO Press CARRIAGE RETURN	1	
2. Go to sheet 3 of this table.	2	
3. Repeat the Loadcheck test and this test. Run parameters are incorrect.		1
4. Replace memory interface (data), slot V (procedure 25).		2
5. Replace memory interface (address), slot W (procedure 25).		3
6. Replace transform PWA, slot R (procedure 23).		4
7. Replace control 2, slot N (procedure 23).		5
8. Replace control 1, slot P (procedure 23).		6
9. Replace I/O-TTY, slot K (procedure 23).		7
10. Replace breakpoint controller (if present), slot U (procedure 23).		8
11. Replace SMI, slot L (procedure 23).		9
12. Replace ALU, slot M (procedure 23).		10
13. Call next level of support.		11

TABLE 6-2. MPINS: INSTRUCTION TEST DDLT (Contd)

ASSUMPTIONS:

1. System under test has a 1700 Emulator, version D or E.

   NOTE: Pertains to transform PWA's part numbers:

   96752129 96751081
   96752604 96720404
   96735700
   96837727

CONDITIONS:

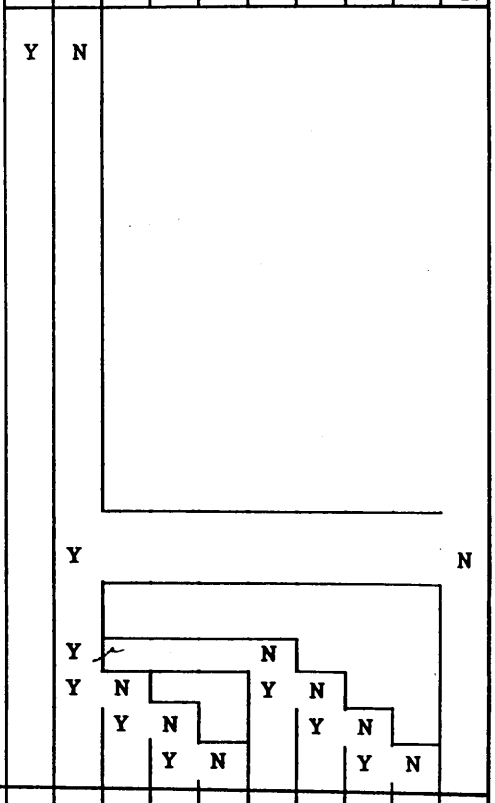
1. Is the following displayed on the screen after approximately 10 seconds:

   MPINS SECTION 0001
   MPINS SECTION 0002
   MULTI-LEVEL INDIRECT SWITCH IS EXPECTED
   TO BE OFF
   MPINS SECTION 0003
   MPINS SECTION 0004
   MPINS SECTION 0005
   MPINS SECTION 0006
   MPINS SECTION 0007
   MPINS SECTION 0008
   MPINS SECTION 0009
   MPINS SECTION 000A
   MPINS SECTION 000B
   MPINS COMPLETED 0001 PASSES
   SET MULTI-LEVEL INDIRECT SWITCH ON
   (ESC J42@GO CR)
   MPINS SUSPENDED SELF

2. Is RUN indicator illuminated?

3. Are any of the following action codes displayed?

   xx11 or xx12 or xx13 or xx14
   xx11 or xx21
   xx12 or xx22
   xx13 or xx23



ACTIONS:

1. Press ESC
   Type J42@GO
   Press CARRIAGE RETURN — 1

2. Go to table 6-3. — 2

3. Replace transform, slot R (procedure 23). — 1 1 1 1 2 2 2 2

Continued on next page

TABLE 6-2. MPINS: INSTRUCTION TEST DDLT (Contd)

Sheet 3 of 5 (Contd)

ACTIONS (Continuod):		1	2	3	4	5	6	7	8	9	10
4.	Replace ALU, slot M (procedure 23).		2	2	2	2	1	1	1	1	
5.	Replace control 1, slot P (procedure 23).		5	5	3	3	5	5	3	3	
6.	Replace control 2, slot N (procedure 23).		4	4	5	4	4	4	5	4	
7.	Replace SMI, slot L (procedure 23).		3	6	4	5	3	6	4	5	
8.	Replace memory, slots X, Y, Z, and AC (procedure 24).		6	7	6	6	6	7	6	6	
9.	Replace I/O-TTY, slot K (procedure 23).		9	3	9	9	9	3	9	9	
10.	Replace memory interface (data), slot V (procedure 25).		7	8	7	7	7	8	7	7	
11.	Replace memory interface (address), slot W (procedure 25).		8	9	8	8	8	9	8	8	
12.	Replace control panel PWA (procedure 20).										1
13.	Go to table 6-11.		10	10	10	10	10	10	10	10	2

TABLE 6-2. MPINS: INSTRUCTION TEST DDLT (Contd)

Sheet 4 of 5

ASSUMPTIONS:

1. Entry is made from sheet 1.
2. System under test does not have 1700 Emulator, version D or E.

   NOTE: Pertains to transform PWA's part numbers:

   96753001 96751046
   96753893 96752601

CONDITIONS:	1	2
1. Does the screen display the following? SET MULTI-LEVEL INDIRECT SWITCH OFF (ESC J40@GO CR) MPINS SUSPENDED SELF	Y	N
ACTIONS		
1. Enter the following at the keyboard: Press ESC Type J40@GO Press CARRIAGE RETURN	1	
2. Go to sheet 5 of this table.	2	
3. Repeat the Loadcheck test and this test. Run parameters are incorrect.		1
4. Replace memory interface (data), slot V (procedure 25).		2
5. Replace memory interface (address), slot W (procedure 25).		3
6. Replace transform, slot R (procedure 23).		4
7. Replace control 2, slot N (procedure 23).		5
8. Replace control 1, slot P (procedure 23).		6
9. Replace I/O-TTY, slot K (procedure 23).		7
10. Replace breakpoint controller (if present), slot U (procedure 23).		8
11. Replace SMI, slot L (procedure 23).		9
12. Replace ALU, slot M (procedure 23).		10
13. Call next level of support.		11

TABLE 6-2. MPINS: INSTRUCTION TEST DDLT (Contd)

ASSUMPTIONS:

1. System under test does not have a 1700 Emulator, version D or E.

   NOTE: Pertains to transform PWA's part numbers:

   96753001 96751046
   96753893 96752601

CONDITIONS:	1	2	3	4	5	6	7	8	9	10
1. Is the following displayed after approximately 10 seconds: MPINS SECTION 0001 MPINS SECTION 0002 MULTI-LEVEL INDIRECT SWITCH IS EXPECTED TO BE OFF MPINS SECTION 0003 MPINS SECTION 0004 MPINS SECTION 0005 MPINS SECTION 0006 MPINS SECTION 0007 MPINS SECTION 0008 MPINS SECTION 0009 MPINS COMPLETED 0001 PASSES SET MULTI-LEVEL INDIRECT SWITCH ON (ESC J42@GO CR) MPINS SUSPENDED SELF	Y	N								
2. Is the RUN indicator illuminated?		Y								N
3. Are any of the following codes displayed?										
xx11 or xx12 or xx13 or xx14		Y				N				
xx11 or xx21		Y	N			Y	N			
xx12 or xx22			Y	N			Y	N		
xx13 or xx23				Y	N			Y	N	
ACTIONS										
1. Enter the following at the keyboard: Press ESCAPE key Type J42@GO Press CARRIAGE RETURN Proceed to table 6-3.	X									
2. Replace control panel PWA (procedure 20).										1

Continued on next page

TABLE 6-2. MPINS: INSTRUCTION TEST DDLT (Contd)

Sheet 5 of 5 (Contd)

ACTIONS (Continued):		1	2	3	4	5	6	7	8	9	10
3.	Replace transform, slot R (procedure 23).		1	1	1	1	2	2	2	2	
4.	Replace ALU, slot M (procedure 23).		2	2	2	2	1	1	1	1	
5.	Replace control 1, slot P (procedure 23).		5	5	3	3	5	5	3	3	
6.	Replace control 2, slot N (procedure 23).		4	4	5	4	4	4	5	4	
7.	Replace SMI, slot L (procedure 23).		3	6	4	5	3	6	4	5	
8.	Replace memory, slots X, Y, Z, and AC (procedure 24).		6	7	6	6	6	7	6	6	
9.	Replace I/O-TTY, slot K (procedure 23).		9	3	9	9	9	3	9	9	
10.	Replace memory interface (data), slot V (procedure 25).		7	8	7	7	7	8	7	7	
11.	Replace memory interface (address), slot U (procedure 25).		8	9	8	8	8	9	8	8	
12.	Go to table 6-11.		10	10	10	10	10	10	10	10	2

TABLE 6-3. CUSTOMER INPUT

Sheet 1 of 1

ASSUMPTIONS:

Customer engineer discusses nature of problems with customer.

CONDITIONS:		1	2	3
1.	Does customer suspect a particular subsystem or retest after an action?	N	Y	
2.	Is the computer suspected of having the failure?		N	Y
ACTIONS				
1.	Go to table 6-4.	X		X
2.	Select the suspected subsystem from the list below and go to the applicable subsystem manual listed in the preface. Subsystems Card Reader Cartridge Disk Drive Communication Multiplexer CC614 Console Display CC628 Console Display Flexible Disk Drive CC555 Keyboard Display Terminal Line Printer (Band) Line Printer (Drum) Magnetic Tape Transport (NRZI) Magnetic Tape Transport (NRZI and Phase-Encoded) Storage Module Drive Tape Cassette Communication Line Adapter Eight-Channel CLA, DCCLA, Matrix Printer, etc. Communication Multiplexer		X	

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT

ASSUMPTIONS:

1. If this test is not to be run, go to table 6-5.
2. The Loadcheck DDLT (table 6-1) and the Instruction Test DDLT (table 6-2) run successfully in both processors of an AA133-A/B or AA153-A (dual-processor) equipment.
3. After xxxxx? is displayed, the following is entered at the keyboard (if xxxxx is not displayed, go to table 6-10):

   Type MPMOS
   Press CARRIAGE RETURN

   NOTE: xxxxx = test name
4. Observe the console display for the following conditions.

CONDITIONS:	1	2	3
1. Does the screen display: MPMOS EXECUTING MPMOS SUSPENDED BOT	Y		N
2. Is this CPU 2 of an AA133-A/B equipment?	Y	N	
ACTIONS			
1. Go to table 6-10.			X
2. At the keyboard, enter the parameter for executing out of CPU 1. Fill in the spaces below with run parameters as directed in procedure 26. Type A, Press CARRIAGE RETURN Type D, , Press CARRIAGE RETURN		1	
3. At the keyboard, enter the parameter for executing out of CPU 2. Fill in the spaces below as directed in procedure 26. Type A, Press CARRIAGE RETURN Type D, , Press CARRIAGE RETURN	1		
4. At the keyboard: Type GO Press CARRIAGE RETURN	2	2	
5. Go to sheet 2 of this table.	3	3	

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

Observe the console display for the following conditions.

CONDITIONS:	1	2
1. Does the screen display: SET MULTI-LEVEL INDIRECT SWITCH OFF (ESC J40@GO CR) MPMOS SUSPENDED SELF	Y	N
ACTIONS		
1. At the keyboard: Press ESC key Type J40@GO Press CARRIAGE RETURN	1	
2. Go to sheet 3 of this table.	2	
3. Repeat Loadcheck DDLT (table 6-1) and repeat this test. Operator error is suspected.		1
4. Call next level of support.		2

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
After several minutes delay does the screen display: MPMOS SECTION 0001 MPMOS SECTION 0003 MPMOS SECTION 0004 MPMOS SECTION 0005 MPMOS SECTION 0006 MPMOS COMPLETED 0001 PASSES SET MULTI-LEVEL INDIRECT SWITCH ON (ESC J42@GO CR) MPMOS SUSPENDED SELF	Y	N
ACTIONS		
1. At the keyboard: Press ESC key Type J42@GO Press CARRIAGE RETURN	1	
2. Go to sheet 4 of this table.	2	
3. Go to sheet 5 of this table.		X

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2	3
1. Does the screen display: MPMOS TERMINATED 0000 ERRORS	Y	N	
2. Is an error code displayed?		Y	N
ACTIONS			
1. Go to sheet 8 of this table.	X		
2. Repeat the Loadcheck DDLT (table 6-1) and repeat this test. Operator error is suspected.			1
3. Call next level of support.			2
4. Go to sheet 5 of this table.		X	

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 3 or 4 of this table.

CONDITIONS:	1	2	3	4	5	6	7
Does the screen display:							
1. 04E7	Y	N					
2. 04E8		Y	N				
3. 04E9			Y	N			
4. 04D0				Y	N		
5. xxx0 through xxx7					Y	N	
6. xxx8 through xxxF						Y	N
ACTIONS							
1. Repeat the Loadcheck DDLT (table 6-1) and repeat this test. Run parameters are incorrect.	1	1	1				
2. Replace memory interface (data), local slot V† (procedure 25).	2	3		1			3
3. Replace memory interface (address), local slot W (procedure 25).	3	4		2			2
4. Replace MOS array, local slot X (procedure 24).	4						
5. Replace MOS array, local slot Y (procedure 24).	5						
6. Replace MOS array, local slot Z (procedure 24).	6						
7. Replace MOS array, local slot AC (procedure 24).	7						
8. Replace ECC array, local slot AC (procedure 24).	8						
9. Replace 1700 transform, local slot R (procedure 23).	9			3			8
10. Replace control 2, local slot N (procedure 23).	10			4			9
11. Replace control 1, local slot P (procedure 23).	11			5			10
12. Replace I/O-TTY, local slot K (procedure 23).	12			6			11
13. Replace breakpoint controller (if present), local slot U (procedure 23).	13			7			12

† The local processor is the one in which the diagnostic resides.

Continued on next page

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ACTIONS (Continued):		1	2	3	4	5	6	7
14.	Replace SMI, local slot L (procedure 23).	14			8			13
15.	Replace ALU, local slot M (procedure 23).	15			9			14
16.	Run the Loadcheck DDLT (table 6-1) and run this test in the alternate processor.		2					1
17.	Replace memory interface (data), remote slot V (procedure 25).		5					5
18.	Replace memory interface (address), remote slot W (procedure 25).		6					4
19.	Replace cable at local slot V, pin 228.		7					
20.	Replace cable at local slot V, pin 240.		8					
21.	Replace cable at local slot W, pin 53.		9					6
22.	Replace cable at local slot W, pin 77.		10					7
23.	Verify proper placement of MOS address connectors at local slots Y through AC and reseat each one. Refer to the CYBER 18 Installation Manual.	16						
24.	Verify proper placement of array PWAs in local slots X through AC. See procedure 24.	17						
25.	Call next level of support.	18	11	2	10			15
26.	Go to sheet 6 of this table.					X		
27.	Go to sheet 7 of this table.						X	

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2	3	4	5	6	7	8	9	10	11	12	13
1. Does the screen display:													
xxx0	Y	N											
xxx6 or xxx7		Y	N										
xxx1			Y		N								
xxx2					Y		N						
xxx3							Y			N			
xxx4										Y		N	
2. Are there any 32K PWAs in the local processor?			Y	N	Y	N	Y		N				
3. Is there only one 32K PWA in the local processor?							Y	N		Y	N		
4. Are there only two 32K PWAs in the local processor?												Y	N
ACTIONS:													
1. Replace MOS array PWA in one of the following local slots (procedure 24):													
X	1	4	1	5	5	5	5	5	5	5	5	5	5
Y	5	5	5	1	1	6	6	1	6	6	6	6	6
Z	6	6	6	6	6	1	1	6	7	7	1	7	1
AC	7	1	7	7	7	7	7	7	1	1	7	1	7
2. Replace ECC array (if present), local slot AC (procedure 24).	2		2	2	2	2	2	2	2	2	2	2	2
3. Replace memory interface (data), local slot V (procedure 25).	3	2	3	3	3	3	3	3	3	3	3	3	3
4. Replace memory interface (address), local slot W (procedure 25).	4	3	4	4	4	4	4	4	4	4	4	4	4
5. Call next level of support.	8	7	8	8	8	8	8	8	8	8	8	8	8

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 5 of this table.

CONDITIONS:	1	2	3	4	5	6	7	8	9	10	11	12	13
1. Does the screen display:													
xxx8	Y	N											
xxxE or xxxF		Y	N										
xxx9			Y		N								
xxxA					Y		N						
xxxB							Y			N			
xxxC										Y		N	
2. Are there any 32K PWAs in the remote processor?			Y	N	Y	N	Y		N				
3. Is there only one 32K PWA in the remote processor?							Y	N		Y	N		
4. Are there only two 32K PWAs in the remote processor?												Y	N
ACTIONS:													
1. Replace MOS array PWA in one of the following remote slots (procedure 24):													
X	1	10	1	11	11	11	11	11	11	11	11	11	11
Y	11	11	11	1	1	12	12	1	12	12	12	12	12
Z	12	12	12	12	12	1	1	12	13	13	1	13	1
AC	13	1	13	13	13	13	13	13	1	1	13	1	13
2. Replace ECC array, remote slot AC (procedure 24).	2		2	2	2	2	2	2	2	2	2	2	2
3. Replace memory interface (data), remote slot V (procedure 25).	3	2	3	3	3	3	3	3	3	3	3	3	3
4. Replace memory interface (address), remote slot W (procedure 25).	4	3	4	4	4	4	4	4	4	4	4	4	4
5. Replace memory interface (data), local slot V (procedure 25).	5	4	5	5	5	5	5	5	5	5	5	5	5
6. Replace memory interface (address), local slot W (procedure 25).	6	5	6	6	6	6	6	6	6	6	6	6	6

Continued on next page

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ACTIONS (Continued):	1	2	3	4	5	6	7	8	9	10	11	12	13
7. Replace cable at local slot V, pin 228.	7	6	7	7	7	7	7	7	7	7	7	7	7
8. Replace cable at local slot V, pin 240.	8	7	8	8	8	8	8	8	8	8	8	8	8
9. Replace cable at local slot W, pin 53.	9	8	9	9	9	9	9	9	9	9	9	9	9
10. Replace cable at local slot W, pin 77.	10	9	10	10	10	10	10	10	10	10	10	10	10
11. Call next level of support.	14	13	14	14	14	14	14	14	14	14	14	14	14

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

1. Entry is made from sheet 4 of this table.
2. If this test is not to be run, go to table 6-5.
3. After xxxxx? is displayed, the following is entered at the keyboard (if xxxxx is not displayed, go to table 6-10):

   Type MOSMA
   Press CARRIAGE RETURN

   NOTE: xxxxx = test name
4. Observe the console display for the following conditions.

CONDITIONS:	1	2	3
1. Does the screen display: MOSMA EXECUTING MOSMA SUSPENDED BOT	Y		N
2. Is this CPU2 of an AA133-A/B or AA153-A equipment?	Y	N	
ACTIONS:			
1. Go to table 6-10.			X
2. At the keyboard, enter the parameters for executing out of CPU 1. Fill in the spaces below with run parameters as directed in procedure 26. Type A, Press CARRIAGE RETURN Type D, __,__,__,__ Press CARRIAGE RETURN Type 3, Press CARRIAGE RETURN		1	
3. At the keyboard, enter the parameters for executing out of CPU 2. Fill in the spaces below with run parameters as directed in procedure 26. Type A, Press CARRIAGE RETURN Type D, __,__,__,__ Press CARRIAGE RETURN Type 3, Press CARRIAGE RETURN	1		
4. At the keyboard: Type GO Press CARRIAGE RETURN	2	2	
5. Go to sheet 9 of this table.	3	3	

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

Observe the console display for the following conditions.

CONDITIONS:		1	2
1.	Does the screen display: SET MULTI-LEVEL INDIRECT SWITCH OFF (ESC J40@GO CR) MOSMA SUSPENDED SELF	Y	N
ACTIONS:			
1.	At the keyboard: Press ESC key Type J40@GO Press CARRIAGE RETURN	1	
2.	Go to sheet 10 of this table.	2	
3.	Repeat the Loadcheck DDLT (table 6-1) and repeat this test (from sheet 8). Operator error is suspected.		1
4.	Call next level of support.		2

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
After several minutes delay does the screen display:	Y	N
MOSMA SECTION 0007		
MOSMA SECTION 0008		
MOSMA SECTION 0009 (optional)		
MOSMA SECTION 000A		
MOSMA COMPLETED 0001 PASSES		
SET MULTI-LEVEL INDIRECT SWITCH ON (ESC J42@GO CR)		
MOSMA SUSPENDED SELF		

ACTIONS:		
1. At the keyboard: Press ESC key Type J42@GO Press CARRIAGE RETURN	1	
2. Go to sheet 11 of this table.	2	
3. Go to sheet 12 of this table.		X

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
Does the screen display: MOSMA TERMINATED 0000 ERRORS	Y	N
ACTIONS:		
1. Go to table 6-5.	X	
2. Repeat the Loadcheck DDLT (table 6-1) and repeat this test (from sheet 8). Operator error is suspected.		1
3. Call next level of support.		2

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 10 of this table.

CONDITIONS:	1	2	3	4	5	6	7	8
Does the screen display:								
1. 24C0 or 24CE	Y	N						
2. 24D0		Y	N					
3. 24E4, 24E5, 24E6, or 24E9			Y	N				
4. 24E7, 24EA, or 24EC				Y	N			
5. 24E8					Y	N		
6. xxx0 through xxx7						Y	N	
7. xxx8 through xxxF							Y	N
ACTIONS:								
1. Repeat the Loadcheck DDLT (table 6-1) and repeat this test (from sheet 8). Run parameters are incorrect.			1	1	1			
2. Replace memory interface (data), local slot V (procedure 25).	5	1		2	3			3
3. Replace memory interface (address), local slot W (procedure 25).	6	2		3	4			2
4. Replace MOS array, local slot X (procedure 24).	1			4				
5. Replace MOS array, local slot Y (procedure 24).	2			5				
6. Replace MOS array, local slot Z (procedure 24).	3			6				
7. Replace MOS array, local slot AC (procedure 24).				7				
8. Replace ECC array, local slot AC (procedure 24).	4			8				
9. Replace 1700 transform, local slot R (procedure 23).		3		9				8
10. Replace control 2, local slot N (procedure 23).		4		10				9
11. Replace control 1, local slot P (procedure 23).		5		11				10
12. Replace I/O-TTY, local slot K (procedure 23).		6		12				11

Continued on next page

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ACTIONS (Continued):	1	2	3	4	5	6	7	8
13. Replace breakpoint controller (if present), local slot U (procedure 23).		7		13				12
14. Replace SMI, local slot L (procedure 23).		8		14				13
15. Replace ALU, local slot M (procedure 23).		9		15				14
16. Run the Loadcheck DDLT (table 6-1), and run this test in the alternate processor.					2			1
17. Replace memory interface (data), remote slot V (procedure 25).					5			5
18. Replace memory interface (address), remote slot W (procedure 25).					6			4
19. Replace cable at local slot V, pin 228.					7			
20. Replace cable at local slot V, pin 240.					8			
21. Replace cable at local slot W, pin 53.					9			6
22. Replace cable at local slot W, pin 77.					10			7
23. Call next level of support.	7	10	2	16	11			15
24. Go to sheet 13 of this table.						X		
25. Go to sheet 14 of this table.							X	

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2	3	4	5	6	7	8	9	10	11	12	13
1. Does the screen display:													
xxx0	Y	N											
xxx6 or xxx7		Y	N										
xxx1			Y		N								
xxx2					Y		N						
xxx3							Y			N			
xxx4										Y		N	
2. Are there any 32K PWAs in the local processor?			Y	N	Y	N	Y		N				
3. Is there only one 32K PWA in the local processor?							Y	N		Y	N		
4. Are there only two 32K PWAs in the local processor?												Y	N
ACTIONS:													
1. Replace MOS array PWA in local slot (procedure 24):													
X	1	4	1	5	5	5	5	5	5	5	5	5	5
Y	5	5	5	1	1	6	6	1	6	6	6	6	6
Z	6	6	6	6	6	1	1	6	7	7	1	7	1
AC	7	1	7	7	7	7	7	7	1	1	7	1	7
2. Replace ECC array if present, local slot AC (procedure 24).	2		2	2	2	2	2	2	2	2	2	2	2
3. Replace memory interface (data), local slot V (procedure 25).	3	2	3	3	3	3	3	3	3	3	3	3	3
4. Replace memory interface (address), local slot W (procedure 25).	4	3	4	4	4	4	4	4	4	4	4	4	4
5. Call next level of support.	8	7	8	8	8	8	8	8	8	8	8	8	8

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 12 of this table.

CONDITIONS:	1	2	3	4	5	6	7	8	9	10	11	12	13
1. Does the screen display:													
xxx8	Y	N											
xxxE or xxxF		Y	N										
xxx9			Y		N								
xxxA					Y		N						
xxxB							Y			N			
xxxC										Y		N	
2. Are there any 32K PWAs in the remote processor?			Y	N	Y	N	Y		N				
3. Is there only one 32K PWA in the remote processor?							Y	N		Y	N		
4. Are there only two 32K PWAs in the remote processor?												Y	N
ACTIONS:													
1. Replace MOS array PWA in remote slot (procedure 24):													
X	1	10	1	11	11	11	11	11	11	11	11	11	11
Y	11	11	11	1	1	12	12	1	12	12	12	12	12
Z	12	12	12	12	12	1	1	12	13	13	1	13	1
AC	13	1	13	13	13	13	13	13	1	1	13	1	13
2. Replace ECC array, remote slot AC (procedure 24).	2		2	2	2	2	2	2	2	2	2	2	2
3. Replace memory interface (data), remote slot V (procedure 25).	3	2	3	3	3	3	3	3	3	3	3	3	3
4. Replace memory interface (address), remote slot W (procedure 25).	4	3	4	4	4	4	4	4	4	4	4	4	4
5. Replace memory interface (data), local slot V (procedure 25).	5	4	5	5	5	5	5	5	5	5	5	5	5

Continued on next page

TABLE 6-4. MPMOS AND MOSMA: MOS MAIN MEMORY DDLT (Contd)

ACTIONS (Continued):	1	2	3	4	5	6	7	8	9	10	11	12	13
6. Replace memory interface (address), local slot W (procedure 25).	6	5	6	6	6	6	6	6	6	6	6	6	6
7. Replace cable at local slot V, pin 228.	7	6	7	7	7	7	7	7	7	7	7	7	7
8. Replace cable at local slot V, pin 240.	8	7	8	8	8	8	8	8	8	8	8	8	8
9. Replace cable at local slot W, pin 53.	9	8	9	9	9	9	9	9	9	9	9	9	9
10. Replace cable at local slot W, pin 77.	10	9	10	10	10	10	10	10	10	10	10	10	10
11. Call next level of support.	14	13	14	14	14	14	14	14	14	14	14	14	14

TABLE 6-5. MPRTC: MEMORY PROTECT AND INTERRUPT SYSTEM TEST DDLT

ASSUMPTIONS:

1. If this test is not to be run, go to next table.

2. After xxxxx? is displayed, the following is entered at the keyboard (if xxxxx is not displayed, go to table 6-10):

   Type MPRTC
   Press CARRIAGE RETURN

   NOTE: xxxxx = test name

3. See the list below for operator actions as directed by diagnostic. Then observe the console display for the following conditions after approximately two minutes. Following program input requests, observe conditions.

Display message directive	Operator response
1. Clear protect and stop switches	1. Press ESC key 2. Type J20@GO 3. Press CARRIAGE RETURN
2. Set protect and clear stop switches	1. Press ESC key 2. Type J28@GO 3. Press CARRIAGE RETURN
3. Set protect and stop switches	1. Press ESC key 2. Type J2A@GO 3. Press CARRIAGE RETURN
4. Verify processor is halted at xxxx and restart	1. Press ESC key 2. Type J11GKG 3. Observe the value Knnnn, where nnnn portion equals the xxxx value in message. If not equal, go to next page and assume code 0651. If equal, type in I@ at the keyboard.
5. Set protect and clear stop switches	1. Press ESC key 2. Type J28@GO 3. Press CARRIAGE RETURN
6. Clear protect and set stop switches	1. Press ESC key 2. Type J22@GO 3. Press CARRIAGE RETURN

Continued on next page

TABLE 6-5. MPRTC: MEMORY PROTECT AND INTERRUPT SYSTEM TEST DDLT (Contd)

Sheet 1 of 2 (Contd)

CONDITIONS:		1	2	3	4	5	6	7	8
1.	Is MPRTC EXECUTING displayed?	Y						N	
2.	Is RUN indicator illuminated?							N	Y
3.	Is micro processor halted at address displayed in display message directive 4 (see previous sheet)?	Y				N			
4.	Is MPRTC TERMINATED displayed?	Y		N					
5.	Are action codes displayed?			Y	N	Y	N		
6.	Is there a ghost interrupt message?	N	Y						
1.	Go to table 6-6.	X							
2.	Go to table 6-10.							X	
3.	Go to sheet 2 of this table.			X		X			
4.	Go to sheet 2 of this table and assume action code 0651.						X		
5.	Go to sheet 2 of this table and assume action code 0657.								X
6.	Replace SMI, slot L (procedure 23).		1						
7.	Go to table 6-11.		2						
8.	Go to sheet 2 of this table and assume action code 0652.				X				

TABLE 6-5. MPRTC: MEMORY PROTECT AND INTERRUPT SYSTEM TEST DDLT (Contd)

ASSUMPTIONS:

1. A failure has been detected. The following analyzes and isolates the detected failure.
2. Observe the console display for any of the following conditions.

CONDITIONS:	1	2	3	4	5	6	7	8	9
Does the screen display:									
1. 0641 or 0642	Y	N							
2. 0651 or 0654 or 0656		Y	N						
3. 0652 or 0653			Y	N					
4. 0655				Y	N				
5. 0657 or 0621					Y	N			
6. 0661 or 06B2 or 06B3						Y	N		
7. 0671 or 0672							Y	N	
8. 06A1								Y	N
9. 06B1									Y
ACTIONS:									
1. Replace memory interface (data), slot V (procedure 25).	2	2	1		4	3	3	2	3
2. Replace memory interface (address), slot W (procedure 25).	3	3	2		5		4	3	4
3. Replace transform, slot R (procedure 23).	5	1	4	2	3	1	5	6	1
4. Replace SMI, slot L (procedure 23).	4	4	3	1	2	2	6	5	5
5. Replace memory, slot X (procedure 24).	1	5	5				2	4	2
6. Replace I/O-TTY, slot K (procedure 23).		6			1				
7. Check power supply voltages (procedures 7, 9, and 11).							1		
8. Restart this test (go back to sheet 1 of this table).								1	
9. Go to table 6-11.	6	7	6	3	6	4	7	7	6

TABLE 6-6. MIMEM AND MIINS: MICRO MEMORY AND MICRO INSTRUCTION TEST DDLT

MIMEM TEST		Sheet 1 of 8		
ASSUMPTIONS:				
1.	If this test is not to be run, go to table 6-7.			
2.	The equipment contains micro memory (slot S and/or T).			
3.	After xxxxx? is displayed, enter the following at the keyboard (if xxxxx is not displayed, go to table 6-10): Type MIMEM Press CARRIAGE RETURN NOTE: xxxxx = test name			
4.	Observe the console display for the following conditions.			
CONDITIONS:		1	2	3
1.	Does the screen display: MIMEM EXECUTING MIMEM SUSPENDED BOT	Y	N	
2.	Is RUN indicator illuminated?		N	Y
ACTIONS:				
1.	Fill in the spaces below with the run parameters as directed in procedure 33. At the keyboard: Type D, Press CARRIAGE RETURN Type 11, Press CARRIAGE RETURN Type GO Press CARRIAGE RETURN	1		
2.	Go to sheet 2 of this table.	2		
3.	Replace control panel PWA (procedure 20).		1	
4.	Go to table 6-11.		2	X

TABLE 6-6. MIMEM AND MIINS: MICRO MEMORY AND MICRO INSTRUCTION TEST DDLT (Contd)

MIMEM TEST	Sheet 2 of 8	
ASSUMPTIONS:		
CONDITIONS:	1	2
Within approximately 3 minutes does the screen display:	Y	N
MIMEM SECTION 0001 MIMEM SECTION 0002 MIMEM SECTION 0003 MIMEM SECTION 0004 MIMEM COMPLETED 0001 PASSES MIMEM TERMINATED 0000 ERRORS		
ACTIONS:		
1. Go to sheet 4 of this table.	X	
2. Go to sheet 3 of this table.		X

TABLE 6-6. MIMEM AND MIINS: MICRO MEMORY AND MICRO INSTRUCTION TEST DDLT (Contd)

MIMEM TEST											Sheet 3 of 8
ASSUMPTIONS:											
CONDITIONS:	1	2	3	4	5	6	7	8	9	10	11
Does the screen display:											
1. 02A4 or 0244	Y	N									
2. 02A5 or 0245		Y	N								
3. 02A6 or 0246			Y	N							
4. 02A7 or 0247				Y	N						
5. 02A8 or 0248					Y	N					
6. 02A9 or 0249						Y	N				
7. 02AA or 024A							Y	N			
8. 02AB or 024B								Y	N		
9. 02AC through 02AF or 024C through 024F									Y	N	
10. 0201 through 0204										Y	N
ACTIONS:											
1. Replace micro memory, slot T (procedure 23).	1	1	1	1							2
2. Replace micro memory, slot S (procedure 23).		2	2	2	1	1	1	1			3
3. Replace control 2, slot N (procedure 23).	2	3	3	3	2	2	2	2			
4. Replace control 1, slot P (procedure 23).	3	4	4	4	3	3	3	3			
5. Replace SMI, slot L (procedure 23).	4	5	5	5	4	4	4	4			
6. Replace transform, slot R (procedure 23).	5	6	6	6	5	5	5	5			
7. Replace ALU, slot M (procedure 23).	6	7	7	7	6	6	6	6			
8. Press MASTER CLEAR Press RUN Ensure that run parameters are correct (procedure 34). Restart test from sheet 1 of this table.									X	X	1
9. Go to table 6-10.											4
10. Call next level of support.	7	8	8	8	7	7	7	7			

TABLE 6-6. MIMEM AND MIINS: MICRO INSTRUCTION TEST DDLT (Contd)

MIINS TEST — Sheet 4 of 8

ASSUMPTIONS:

1. Entry is made from sheet 2 of this table.
2. At least one optional micro-memory PWA is installed in the processor to be tested (BA209 or BA210).
3. Page selection has been made per table 4-5.
4. After xxxx? is displayed, enter the following at the keyboard (If xxxxx? is not displayed, go to table 6-10.)

   Type MIINS
   Press CARRIAGE RETURN

   NOTE: xxxxx = test name

5. Observe the console display for the following conditions.

CONDITIONS:	1	2	3	4	5	6
1. Does the screen display: MIINS EXECUTING MIINS SUSPENDED BOT	Y				N	
2. Is RUN indicator illuminated?					N	Y
3. Is there one BA209 micro-memory PWA in slot T and no PWA in slot S? (Verify by removing the side panel of the processor and examining the FCO tags for slots T and S.)	N		Y			
4. Is the equipment under test one of the following: a. AA132-A or CPU 1 of AA133-A with STO10428-1 installed or b. AA132-B/C or CPU 1 of AA133-B or CPU 1 of AA153-A	Y	N	Y	N		
ACTIONS:						
1. At the keyboard: Type B,0 Press CARRIAGE RETURN			1	1		
2. At the keyboard: Type 5,0 Press CARRIAGE RETURN Type C,0 Press CARRIAGE RETURN		1		2		
3. At the keyboard: Type GO Press CARRIAGE RETURN	1	2	2	3		
4. Go to sheet 7 of this table.	2		3			
5. Replace control panel PWA (procedure 20).					1	
6. Go to table 6-11.					2	X
7. Go to sheet 5 of this table.		3		4		

TABLE 6-6. MIMEM AND MIINS: MICRO MEMORY AND MICRO INSTRUCTION TEST DDLT (Contd)

MIINS TEST	Sheet 5 of 8		
ASSUMPTIONS:			
CONDITIONS:		1	2
1.	Within approximately 30 seconds does the screen display:	Y	N
	MIINS SECTION 0001		
	MIINS SECTION 0002		
	MIINS SECTION 0003		
	MIINS SECTION 0004		
	MIINS SECTION 0005		
	MIINS SECTION 0006		
	MIINS SECTION 0007		
	MIINS SECTION 0008		
	MIINS COMPLETED 0001 PASSES		
	MIINS TERMINATED 0000 ERRORS		
ACTIONS:			
1.	Go to table 6-7.	X	
2.	Go to sheet 6 of this table.		X

TABLE 6-6. MIMEM AND MIINS: MICRO MEMORY AND MICRO INSTRUCTION TEST DDLT (Contd)

MIINS TEST — Sheet 6 of 8

ASSUMPTIONS:

CONDITIONS:	1	2	3	4	5	6	7	8
Does the screen display:								
1. 0E81 or 0E83	Y	N						
2. 0E82 or 0E84		Y	N					
3. 0E85			Y	N				
4. 0E86				Y	N			
5. 0E87					Y	N		
6. 0E88						Y	N	
7. 0E01							Y	N
ACTIONS:								
1. Restart this test (from sheet 4). The run parameters are incorrect.							X	
2. Replace ALU, slot M (procedure 23).	1	2	4	1	3	3		1
3. Replace control 1, slot P (procedure 23).	2	3	2	3	2	4		2
4. Replace control 2, slot N (procedure 23).	3	1	3	2	4	5		3
5. Replace transform, slot R (procedure 23).	4	7	1	4	5	6		4
6. Replace SMI, slot L (procedure 23).	5	4	7		1			5
7. Replace memory interface (address), slot W (procedure 25).	6	5	5			1		6
8. Replace memory interface (data), slot V (procedure 25).	7	6	6			2		7
9. Replace micro memory, slot T (procedure 23).	8	8	8	5	6	7		8
10. Replace micro memory, slot S (procedure 23).	9	9	9	6	7	8		9
11. Go to table 6-10.	10	10	10	7	8	9		10
12. Call next level of support.	11	11	11	8	9	10		11

TABLE 6-6. MIMEM AND MIINS: MICRO MEMORY AND MICRO INSTRUCTION TEST DDLT (Contd)

MIINS TEST	Sheet 7 of 8		
ASSUMPTIONS:			
Entry is made from sheet 4 of this table.			
CONDITIONS:		1	2
1.	Within approximately 30 seconds does the screen display:	Y	N
	MIINS SECTION 0001		
	MIINS SECTION 0002		
	MIINS SECTION 0003		
	MIINS SECTION 0004		
	MIINS SECTION 0005		
	MIINS SECTION 0006		
	MIINS SECTION 0007		
	MIINS SECTION 0008		
	MIINS SECTION 0009		
	MIINS COMPLETED 0001 PASSES		
	MIINS TERMINATED 0000 ERRORS		
ACTIONS			
1.	Go to table 6-7.	X	
2.	Go to sheet 7 of this table.		X

TABLE 6-6. MIMEM AND MIINS: MICRO MEMORY AND MICRO INSTRUCTION TEST DDLT (Contd)

MIINS TEST — Sheet 8 of 8

ASSUMPTIONS:

Entry is made from sheet 5 of this table.

CONDITIONS:	1	2	3	4	5	6	7	8	9	10
Does the screen display:										
1. 0E81 or 0E83	Y	N								
2. 0E82 or 0E84		Y	N							
3. 0E85			Y	N						
4. 0E86				Y	N					
5. 0E87					Y	N				
6. 0E88						Y	N			
7. 0E01							Y	N		
9. 0E89 or 0E8A or 0E8B or 0E8C or 0E8D									Y	N
ACTIONS										
1. Restart this test (from sheet 4). The run parameters are incorrect.							X			
2. Replace ALU, slot M (procedure 23).	1	2	4	1	3	3		1	4	1
3. Replace control 1, slot P (procedure 23).	2	3	2	3	2	4		2	3	2
4. Replace control 2, slot N (procedure 23).	3	1	3	2	4	5		3	5	3
5. Replace transform, slot R (procedure 23).	4	7	1	4	5	6		4	1	4
6. Replace SMI, slot L (procedure 23).	5	4	7		1			5	2	5
7. Replace memory interface (address), slot W (procedure 25).	6	5	5			1		6		6
8. Replace memory interface (data), slot V (procedure 25).	7	6	6			2		7		7
9. Replace micro memory, slot T (procedure 23).	8	8	8	5	6	7		8		8
10. Replace micro memory, slot S (procedure 23).	9	9	9	6	7	8		9		9
11. Go to table 6-10.	10	10	10	7	8	9		10	6	10
12. Call next level of support.	11	11	11	8	9	10		11	7	11

TABLE 6-7. PAGE1: MOS MEMORY PAGING FILE TEST DDLT

ASSUMPTIONS:

1. If this test is not to be run, go to table 6-8.
2. The MOS MAIN MEMORY DDLT (table 6-4) runs successfully in both processors.
3. After xxxxx? is displayed, the following is entered at the keyboard (if xxxxx? is not displayed, go to table 6-10):

   Type PAGE1
   Press CARRIAGE RETURN

   NOTE: xxxxx = test name
4. Observe the console display for the following conditions.

CONDITIONS:	1	2	3
1. Does the screen display: PAGE1 EXECUTING PAGE1 SUSPENDED BOT	Y		N
2. Is this CPU 2 of an AA133-A/B or AA153-A equipment?	Y	N	
ACTIONS			
1. Go to table 6-10.			X
2. At the keyboard, enter parameters for executing out of CPU 1: Fill in the spaces below with run parameter A as directed in procedure 26. Type A, Press CARRIAGE RETURN Type GO Press CARRIAGE RETURN		1	
3. At the keyboard, enter parameters for executing out of CPU 2: Fill in the spaces below with run parameter A as directed in procedure 26. Type A, Press CARRIAGE RETURN Type GO Press CARRIAGE RETURN	1		
4. Go to sheet 2 of this table.	2	2	

TABLE 6-7. PAGE1: MOS MEMORY PAGING FILE TEST DDLT (Contd)

Sheet 2 of 7

ASSUMPTIONS:

CONDITIONS:	1	2
1. Does the screen display: SET MULTI-LEVEL INDIRECT SWITCH OFF (ESC J40 @GO CR) PAGE1 SUSPENDED SELF	Y	N
ACTIONS		
1. At the keyboard: Press ESC Type J40@GO Press CARRIAGE RETURN	1	
2. Go to sheet 3 of this table.	2	
3. Go to sheet 7 of this table.		X

TABLE 6-7. PAGE1: MOS MEMORY PAGING FILE TEST DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
1. After several seconds delay, does the screen display: PAGE1 SECTION 0001 PAGE1 SECTION 0002 PAGE1 SECTION 0003 PAGE1 SECTION 0004 PAGE1 SECTION 0005 SET MULTI-LEVEL INDIRECT SWITCH ON (ESC J42@GO CR) PAGE1 SUSPENDED SELF	Y	N
ACTIONS:		
1. At the keyboard: Press ESC Type J42@GO Press CARRIAGE RETURN	1	
2. Go to sheet 4 of this table.	2	
3. Go to sheet 7 of this table.		X

TABLE 6-7. PAGE1: MOS MEMORY PAGING FILE TEST DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
Does the screen display: SET MULTI-LEVEL INDIRECT SWITCH OFF (ESC J40@GO CR) PAGE1 SUSPENDED SELF	Y	N

ACTIONS:			
1.	At the keyboard: Press ESC Type J40@GO Press CARRIAGE RETURN	1	
2.	Go to sheet 5 of this table.	2	
3.	Go to sheet 7 of this table.		X

TABLE 6-7. PAGE1: MOS MEMORY PAGING FILE TEST DDLT (Contd)

ASSUMPTIONS:		
CONDITIONS:	1	2
Does the screen display:	Y	N
PAGE1 COMPLETED 0001 PASSES SET MULTI-LEVEL INDIRECT SWITCH ON (ESC J42 @GO CR) PAGE1 SUSPENDED SELF		
ACTIONS:		
1. At the keyboard: Press ESC Type J42 @ GO Press CARRIAGE RETURN	1	
2. Go to sheet 6 of this table.	2	
3. Go to sheet 7 of this table.		X

TABLE 6-7. PAGE1: MOS MEMORY PAGING FILE TEST DDLT (Contd)

ASSUMPTIONS:		
CONDITIONS:	1	2
Does the screen display: PAGE1 TERMINATED 0000 ERRORS	Y	N
ACTIONS:		
1. Go to table 6-8.	X	
2. Go to sheet 7 of this table.		X

TABLE 6-7. PAGE1: MOS MEMORY PAGING FILE TEST DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 2, 3, 4, 5, or 6 of this table. An error has occurred.

CONDITIONS:	1	2	3
Does the screen display:			
1. 0301 or 0302	Y	N	
2. 0303, 0304, 0306, 0351, 0352, or 0353		Y	N
ACTIONS:			
1. Return to sheet 1, action 2, of this table. Parameter A is incorrect.	1		
2. Repeat the Loadcheck DDLT (table 6-1) and this test. Run parameters are incorrect.	2	1	1
3. Replace memory interface (data), local slot V† (procedure 25).			2
4. Replace memory interface (address), local slot W (procedure 25).			3
5. Replace transform, local slot R (procedure 23).			4
6. Replace control 2, local slot N (procedure 23).			5
7. Replace control 1, local slot P (procedure 23).			6
8. Replace I/O-TTY, local slot K (procedure 23).			7
9. Replace breakpoint controller (if present), local slot U (procedure 23).			8
10. Replace SMI, local slot L (procedure 23).			9
11. Replace ALU, local slot M (procedure 23).			10
12. Call next level of support.	3	2	11

†The local processor is the one in which the diagnostic resides.

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT

ASSUMPTIONS:

1. If this is not a AA133-A/B or AA153-A equipment, this test is not to be run. Go to table 6-9.
2. The MOS Main Memory DDLT (table 6-4), Memory Protect DDLT (table 6-5), and Micro Memory DDLT (table 6-6) run successfully in both processors.
3. Cassette drive and flexible disk drive for CPU 2 is empty.
4. CPU I is selected at the control panel.

CONDITIONS:	1	2	3	4	5	6	7
1. Press MASTER CLEAR at the control panel. Press G at the keyboard. Does the screen display G?	Y						N
2. Select CPU II at the control panel. Press G at the keyboard. Does the screen display G?	Y					N	
3. Select CPU I at the control panel. Press G at the keyboard. Does the screen display H0000000X0?	Y				N		
4. Select CPU II at the control panel. Press G at the keyboard. Does the screen display H000000X0?	Y			N			
5. Press DEADSTART at the control panel. Does DEADSTART indicator remain on?	Y		N				
6. Select CPU I and press MASTER CLEAR at the control panel. Select CPU II at the control panel. Is the DEADSTART indicator off?	Y	N					
ACTIONS							
1. Go to sheet 2 of this table.	X						
2. Replace I/O-TTY, slot K (CPU 1) (procedure 23).		1		1			
3. Replace panel multiplexer PWA (procedure 22).				2	2		1
4. Replace I/O-TTY, slot K (CPU 1) (procedure 23).			1		1		
5. Call next level of support.		2	2	3	3	X	2

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT (Contd)

ASSUMPTIONS:

1. CPU I is selected at the control panel and the MASTER CLEAR button is pressed.

2. The load device is a cassette:

   Level I tape is inserted into cassette drive for CPU 1.
   DEADSTART button is pressed.

   Or the load device is a flexible disk drive:

   Level I diskette is inserted into the diskette drive for CPU 1.
   DEADSTART button is pressed.

3. After xxxxx? is displayed, the following is entered at the keyboard (if xxxxx? is not displayed, go to table 6-10:

   Type DUCPU
   Press CARRIAGE RETURN

   NOTE: xxxx = test name

4. Observe the console display for the following conditions.

CONDITIONS:	1	2
1. Does the screen display: DUCPU EXECUTING DUCPU SUSPENDED BOT	Y	N
ACTIONS:		
1. Go to table 6-10.		X
2. At the keyboard: Type GO Press CARRIAGE RETURN	1	
3. Go to sheet 3 of this table.	2	

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
1. Does the screen display: DUCPU SECTION 0001 DUCPU SECTION 0002 DUCPU SECTION 0003 DUCPU SECTION 0004 DUCPU SECTION 0005 DUCPU SECTION 0006 DUCPU SECTION 0007 DUCPU SECTION 0008 DUCPU SECTION 0009 SET PROTECT SWITCHES - PNL SEL - ESC - J28@ - PNL SEL - J28@GO CR DUCPU SUSPENDED SELF	Y	N
ACTIONS:		
1. Press PANEL SELECT at the control panel.	1	
2. At the keyboard: Press ESC Type J28@	2	
3. Press PANEL SELECT at the control panel.	3	
4. At the keyboard: Type J28@GO Press CARRIAGE RETURN	4	
5. Go to sheet 4 of this table.	5	
6. Go to sheet 6 of this table.		X

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
Does the screen display: RST PROTECT SWITCHES - PNL SEL - ESC - J20@ - PNL SEL - J20@GO CR DUCPU SUSPENDED SELF	Y	N

ACTIONS:		
1. Press PANEL SELECT at the control panel.	1	
2. At the keyboard: Press ESC Type J20@	2	
3. Press PANEL SELECT at the control panel.	3	
4. At the keyboard: Type J20@GO Press CARRIAGE RETURN	4	
5. Go to sheet 5 of this table.	5	
6. Go to sheet 6 of this table.		X

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2
Does the screen display:		
DUCPU COMPLETED 0001 PASSES DUCPU TERMINATED 0000 ERRORS	Y	N
ACTIONS:		
1. Go to the subsystem test.	X	
2. Repeat this test. Operator error is suspected.		1
3. Call next level of support.		2

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT (Contd)

ASSUMPTIONS:

Entry is made from sheet 3 or 4 of this table. An error has occurred.

CONDITIONS:	1	2	3	4	5	6	7	8	9	10
Does the screen display:										
1. 0D01	Y	N								
2. 0D02		Y	N							
3. 0D03			Y	N						
4. 0D04				Y	N					
5. 0D05					Y	N				
6. 0D06						Y	N			
7. 0D07							Y	N		
8. 0D08								Y	N	
9. 0D09									Y	N
ACTIONS										
1. Repeat this test from sheet 2. Wrong parameter.	1									
2. Replace SMI, slot L (CPU 1) (procedure 23).		1	1	1	2	2		2	1	
3. Replace SMI, slot L (CPU 2) (procedure 23).				2	1	1	1	1	2	
4. Replace panel multiplexer PWA (procedure 22).		3		3	3	3		4	4	
5. Examine connectors at each end of panel multiplexer (CPU 1) and panel multiplexer (CPU 2) cable assemblies for loose fit or broken wires.		2						3	3	
6. Examine connector over backpanel pins 52-76 at slot K, CPU 2, for loose fit or broken wire.			2							
7. Examine interrupt jumper plug over back panel pins 70-81 at slot L, CPU 2, for loose fit or broken wire.							2			
8. Go to sheet 7 of this table.										X
9. Call next level of support.	2	4	3	4	4	4	3	5	5	

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT (Contd)

ASSUMPTIONS:

CONDITIONS:	1	2	3	4	5	6	7
Does the screen display:							
1. 0D0A	Y	N					
2. 0D0B		Y	N				
3. 0D0C			Y	N			
4. 0D0D				Y	N		
5. 0D10, 0D11, 0D14, 0D15, or 0D16					Y	N	
6. 0D12, 0D13, 0D17, 0D18, or 0D19						Y	N
ACTIONS							
1. Replace memory interface (data), CPU 1, slot V (procedure 25).	1	1	11	3	1	1	4
2. Replace memory interface (address), CPU 1, slot W (procedure 25).	2	2	12	4	2	2	5
3. Replace memory interface (data), CPU 2, slot V (procedure 25).	3	11	1	1	3	3	1
4. Replace memory interface (address), CPU 2, slot W (procedure 25).	4	12	2	2	4	4	2
5. Replace transform, CPU 1, slot R (procedure 23).	6	4					13
6. Replace control 1, CPU 1, slot P (procedure 23).	7	5					14
7. Replace control 2, CPU 1, slot N (procedure 23).	8	6					15
8. Replace ALU, CPU 1, slot M (procedure 23).	9	7					16
9. Replace SMI, CPU 1, slot L (procedure 23).	10	8					17
10. Replace I/O-TTY, CPU 1, slot K (procedure 23).	11	9					18
11. Replace 2K RAM, CPU 1, slot S (procedure 23).	12	10					19
12. Replace MOS array, CPU 1, slot X (procedure 24).	13	3	13	5			20
13. Replace MOS array, CPU 2, slot X (procedure 24).	5	13	3	13			3
14. Replace transform, CPU 2, slot R (procedure 23).			4	6			6
15. Replace control 1, CPU 2, slot P (procedure 23).			5	7			7

Continued on next page

TABLE 6-8. DUCPU: DUAL-PROCESSOR (DUAL-CPU) DDLT (Contd)

Sheet 7 of 7 (Contd)

ACTIONS (Continued):	1	2	3	4	5	6	7
16. Replace control 2, CPU 2, slot N (procedure 23).			6	8			8
17. Replace ALU, CPU 2, slot M (procedure 23).			7	9			9
18. Replace SMI, CPU 2, slot L (procedure 23).			8	10			10
19. Replace I/O-TTY, CPU 2, slot K (procedure 23).			9	11			11
20. Replace 2K RAM, CPU 2, slot S (procedure 23).			10	12			12
21. Replace cable at slot W, pin 77, CPU 2.					5		
22. Replace cable at slot W, pin 53, CPU 2.					6		
23. Replace cable at slot V, pin 240, CPU 2.					7		
24. Replace cable at slot W, pin 77, CPU 1.						5	
25. Replace cable at slot W, pin 53, CPU 1.						6	
26. Replace cable at slot V, pin 240, CPU 1.						7	
27. Call next level of support.	14	14	14	14	8	8	21

TABLE 6-9. LEVEL II MONITOR DDLT

ASSUMPTIONS:

1. Level I testing is complete. If this is a dual-processor (timeshare) system return to table 6-1 and test the second processor if this has not already been done.
2. If this is a dual processor system, CPU I is selected at the control panel.
3. MASTER CLEAR is pressed.
4. If the load device is a diskette:

   Level II diskette, volume 1 is loaded.
   DEADSTART is pressed.

   NOTE

   Additional diskettes (volume 2, and so forth) may be required to complete Level II testing. See procedure 35 to determine diskette contents.

5. If the load device is a cassette:

   Level II cassette is inserted.
   After READY indicator illuminates, press DEADSTART.

6. If 123456 is displayed, observe for conditions below. If 123456 is not displayed, try another Level II diskette or cassette. If the problem is not corrected, go to table 6-1.

CONDITIONS:	1	2	3	4	5	6	7
1. Is ODS x.x displayed, where x.x is the release level?	Y					N	
2. Is RUN indicator illuminated?						N	Y
3. Is this the first time entry is made to this table?	N	Y					
4. Press STOP. Does RUN indicator extinguish?		Y			N		
5. Press RUN; then press CONTROL and BEL keys simultaneously at the keyboard. Is MI displayed?		Y		N			
6. Does the customer suspect a particular unit?		Y	N				
ACTIONS (Continued):							
1. Go to table 6-10.						X	
2. Call next level of support.					4		
3. Check control panel cable connections.					1		
4. Replace control panel PWA (procedure 20).					2		
5. Replace SMI, slot L (procedure 23).				1	3		
6. Replace I/O-TTY, slot K (procedure 23).				2			
7. Go to table 6-11.				3			X

Continued on next page

TABLE 6-9. LEVEL II MONITOR DDLT (Contd)

ACTIONS (Continued):	1	2	3	4	5	6	7
8. Go to the DDLT of the peripheral subsystem under test or suspected (refer to the preface for manual number):	X	X	X				
Subsystem							
Card reader							
Cassette							
Flexible disk							
Dual-channel communication line adapter							
Single-channel communication line adapter							
Line printer (see note 3)							
Magnetic tape transport (NRZI)							
Storage module drive							
Magnetic tape transport (phase-encoded)							
Cartridge disk drive							
Keyboard display to eight-channel communication line adapter (see note 4)							
Matrix printer to eight-channel communication line adapter (see note 4)							
Eight-channel communication line adapter (see note 4)							

NOTES:

1. For any peripheral PWA replacement from this page on, restart the diagnostic by entering the following at the keyboard:

   Press CONTROL and BEL simultaneously
   Type ODS,RSTR,xxxxx

   Where xxxxx is the respective diagnostic test name mnemonic.

2. If an error occurs from this restart procedure, after performing a DDLT action, reload the test starting with the Loadcheck DDLT (table 6-3). This is necessary because the error may have been induced by performing the DDLT action.

3. For CT103/5 equipment, this test is a fault-detection-only DDLT (no fault isolation provided).

4. These tables are fault detection only.

5. If the load device controller is removed, the Level II Monitor DDLT must be reloaded.

TABLE 6-10. LOADER FAULT DDLT

Sheet 1 of 5

ASSUMPTIONS:

1. A loader error has occurred.

CONDITIONS:	1	2	3
1. Is the load device a flexible disk?	Y	N	
2. Is the load device a cassette?		Y	N
ACTIONS			
1. Go to sheet 2 of this table.	X		
2. Go to sheet 4 of this table.		X	
3. The flexible disk and cassette are the only load devices supported by this manual.			

TABLE 6-10. LOADER FAULT DDLT (Contd)

ASSUMPTIONS:

1. The load device is a flexible disk.
2. The following is typed at the keyboard:

   Press ESC
   Type J11G KG

3. Observe the console display for any of the following conditions. Where an x appears in the action code, the x may be 3 or 7.

CONDITIONS:	1	2	3	4	5	6	7	8
Does the screen display:								
1. KxFBC or KxFCO	Y	N						
2. KxFBE or KxFC2		Y	N					
3. KxFC4			Y	N				
4. KxFC6				Y	N			
5. KxFC8					Y	N		
6. KxFCA						Y	N	
7. KxFCC							Y	N
ACTIONS:								
1. Use another diskette (same program) if available.	1	1	1	1	1	1	1	
2. Verify that the equipment code for the flexible disk drive controller is correct (see the flexible disk drive subsystem manual).	2							
3. Replace I/O-TTY, slot K (procedure 23).	3	2	3	4	4	3		
4. Replace flexible disk drive controller, slot E (procedure 23).	4	3	2	2	2	2		
5. Replace ALU, slot M (procedure 23).	5	4	5	5	6	4		
6. Replace memory, slot X (procedure 24).	6		7	6			2	
7. Replace memory, slot Y (procedure 24).	7		8	7			3	

Continued on next page

TABLE 6-10. LOADER FAULT DDLT (Contd)

Sheet 2 of 5 (Contd)

ACTIONS (Continued):		1	2	3	4	5	6	7	8
8.	Replace memory interface (data), slot V (procedure 25).	8		9	8			4	
9.	Replace memory interface (address), slot W (procedure 25).	9		10	9			5	
10.	Replace SMI, slot L (procedure 23).	10	5	6	10	5	5		
11.	Replace control 2, slot N (procedure 23).	11	7	11	11	8			
12.	Replace control 1, slot P (procedure 23).	12	8	12	12	7			
13.	Replace flexible disk drive (refer to the flexible disk drive subsystem manual).	13	6	4	3	3	6		
14.	The diagnostic program being loaded is too large for available memory. Verify that memory jumper plugs are correct (refer to the CYBER 18 Installation Manual).							6	
15.	Go to sheet 3 of this table.								X
16.	Call next level of support.	14	9	13	13	9	7	7	

TABLE 6-10. LOADER FAULT DDLT (Contd)

ASSUMPTIONS:

1. The load device is a diskette.
2. The following is typed in at the keyboard:

   J14G KG

3. Observe the console display for any of the following conditions.

CONDITIONS:	1	2	3	4	5	6	7	8
Does the screen display?								
1. K0003	Y	N						
2. K0004		Y	N					
3. K0005			Y	N				
4. K0006				Y	N			
5. K0007					Y	N		
6. K0008 or K000A						Y	N	
7. K0009 or K000B							Y	N
ACTIONS:								
1. Use another diskette (same program) if available.	1	1	1	1	1	1	1	1
2. Replace memory, slot X (procedure 24).	2	6	7	6	5	6	8	6
3. Replace memory, slot Y (procedure 24).	3	7	8	7	6	7	9	7
4. Replace memory interface (data), slot V (procedure 25).	4	8	9	8	7	8	10	8
5. Replace memory interface (address), slot W (procedure 25).	5	9	10	9	8	9	11	9
6. The diagnostic program being loaded is too large for available memory. Verify that memory address connectors are positioned correctly (see the CYBER 18 Installation Manual).	6							
7. Replace flexible disk drive controller, slot E (procedure 23).	7	2	2	2	2	2	2	2
8. Replace I/O-TTY controller, slot K (procedure 23).	8	3	3	5	3	3	3	3
9. Replace ALU, slot M (procedure 23).	9	4	4	3	4	5	4	4
10. Replace SMI, slot L (procedure 23).	10	5	11	4	11	4	5	5

Continued on next page

TABLE 6-10. LOADER FAULT DDLT (Contd)

Sheet 3 of 5 (Contd)

ACTIONS (Continued):		1	2	3	4	5	6	7	8
11.	Replace control 2, slot N (procedure 23).	11	10	5	10	9	10	6	10
12.	Replace control 1, slot P (procedure 23).	12	11	6	11	10	11	7	11
13.	Replace flexible disk drive (refer to the flexible disk drive subsystem manual).	13	12			12		12	12
14.	Go to table 6-11.								13
15.	Call next level of support.	14	13	12	12	13	12	13	

TABLE 6-10. LOADER FAULT DDLT (Contd)

ASSUMPTIONS:

1. The load device is a cassette.
2. At the keyboard:

   Press ESC
   Type J11G KG

3. Observe the console display for any of the following conditions. Where an x appears in the action code, the x may be 3 or 7.

CONDITIONS:	1	2	3	4	5	6	7	8
Does the screen display:								
1. KxFCO or KxFC4 or KxFC8 or KxFCC	Y	N						
2. KxFBE or KxFC2 or KxFC6 or KxFCA		Y	N					
3. KxFAC			Y	N				
4. KxFAE				Y	N			
5. KxFBO					Y	N		
6. KxFB6						Y	N	
7. KxFBA							Y	N
ACTIONS								
1. Use another cassette (same program) if available.	1	1	1	1	1	1	1	
2. Verify that the equipment code for the cassette controller is correct (see the cassette subsystem manual).	2							
3. Replace I/O-TTY, slot K (procedure 25).	3	2	4	3	3	3		
4. Replace cassette controller, slot E in CPU 1 or slot H in CPU 2 (procedure 23).	4	3	2	2	2	2		
5. Replace ALU, slot M (procedure 23).	5	4	3	4	4	5	6	
6. Replace memory, slot X (procedure 24).	6		5				2	
7. Replace memory, slot Y (procedure 24).	7		6				3	
8. Replace memory interface (data), slot V (procedure 25).	8		7				4	

Continued on next page

TABLE 6-10. LOADER FAULT DDLT (Contd)

Sheet 4 of 5 (Contd)

ACTIONS (Continued):	1	2	3	4	5	6	7	8
9. Replace memory interface (address), slot W (procedure 25).	9		8				5	
10. Replace SMI, slot L (procedure 23).	10	5	9	5	5	4	7	
11. Replace control 2, slot N (procedure 23).	11	7	10	6	6	6	8	
12. Replace control 1, slot P (procedure 23).	12	8	11	7	7	7	9	
13. Replace cassette transport (refer to the cassette subsystem manual).	13	6		8	8	8		
14. The diagnostic program being loaded is too large for available memory. Verify that memory jumper plugs are correct (refer to the CYBER 18 Installation Manual in the preface).							10	
15. Go to sheet 5 of this table.								X
16. Call next level of support.	14	9	12	9	9	9	11	

TABLE 6-10. LOADER FAULT DDLT (Contd)

ASSUMPTIONS:

1. The load device is a cassette.
2. At the keyboard:

   Press ESC
   Type J14G KG

3. Observe the console display for any of the following conditions.

CONDITIONS:	1	2	3	4	5
Does the screen display:					
1. K0001 or K0002 or K0005	Y	N			
2. K0007		Y	N		
3. K009 or K000B or K000D or K000F			Y	N	
4. K000A or K000C or K000E or K010				Y	N
ACTIONS					
1. Use another cassette (same program) if available.	1	1	1	1	1
2. Replace cassette controller, slot E in CPU 1 or slot H in CPU 2 (procedure 23).	2	7	2	2	2
3. Replace I/O-TTY, slot K (procedure 23).	3	8	3	3	3
4. Replace ALU, slot M (procedure 23).	4	9	5	5	4
5. Replace SMI, slot L (procedure 23).	5	10	4	4	5
6. Replace control 1, slot P (procedure 23).	6	11	7	6	6
7. Replace control 2, slot N (procedure 23).	7	12	6	7	7
8. Replace memory, slot X (procedure 24).	8	2	8	8	8
9. Replace memory, slot Y (procedure 24).	9	3	9	9	9
10. Replace memory interface (data), slot V (procedure 25).	10	4	10	10	10
11. Replace memory interface (address), slot W (procedure 25).	11	5	11	11	11
12. Replace cassette transport (refer to the cassette subsystem manual).	12		12	12	12
13. The diagnostic being loaded is too large for available memory. Verify that memory address connectors are installed correctly (see the CYBER 18 Installation Manual).		6			
14. Go to table 6-11.					13
15. Call next level of support.	13	13	13	13	

TABLE 6-11. SYSTEM FAULT DDLT

Sheet 1 of 1

ASSUMPTIONS:

1. This DDLT satisfies system fault isolation and eliminates failure where peripheral controller faults occur in loading the computer.
2. After PWA replacement, restart at table 6-1.

CONDITIONS:		1	2	3
1.	Is load device a flexible disk?	Y	N	
2.	Is load device a cassette?		Y	N
ACTIONS:				
1.	Replace cassette controller, slot E in CPU 1 or slot H in CPU 2 (procedure 23).		1	
2.	Replace flexible disk controller, slot D or E (procedure 23).	1		
3.	Replace communication line adapter, slot F (procedure 23).	2	2	
4.	Replace magnetic tape controller, slot AB, (procedure 23).	3	3	
5.	Replace SMD controller, slot H (procedure 23).	4	4	
6.	Replace cartridge disk drive controllers, slot H (procedure 23).	5	5	
7.	Replace magnetic tape (phase-encoded) controller, slot G (procedure 23).	6	6	
8.	Replace eight-channel communication line adapter, slot F (procedure 23).	7	7	
9.	Go to the Flexible Disk DDLT in the flexible disk drive subsystem manual.	9		
10.	Go to the Cassette DDLT in the tape cassette subsystem manual.		8	
11.	Replace flexible disk drive (refer to the flexible disk drive subsystem manual).	8		
12.	Call next level of support.	10	9	X

PROCEDURES

1 VISUAL INSPECTION

To inspect the processor, perform the following:

1. Open the cabinet right side panel for access to processor 1 (figure 6-2) or left side panel for access to processor 2 (figure 6-3). Remove the processor cover plate (front panel) by releasing the two captive fasteners.
2. Check that the logic board (PWA) identifications (labeled at the front of the PWA edge) agree with the PWA placement table (table 4-3).
3. Check that all PWAs in the processor chassis are properly seated in their connectors by applying firm thumb pressure at the upper and lower corners of each PWA.
4. At the card reader/line printer controller, verify that the card feed switch is off (pointing toward the operator).
5. Remove the cabinet front panel. Unlatch and swing down the equipment mounting frame.
6. Check that all peripheral interconnection cables are correctly and fully connected to the processor backplane pins at their respective controller locations. Verify that the cable shields and cable clamps are installed. (See the CYBER 18 Computer Systems Installation Manual.)
7. Check that the circuit breaker on the power distribution box (figure 6-2 or 6-3) is set to the ON position.
8. Check that power supply fuses and circuit breakers are on and not blown.
9. Check the power supply fans by momentarily turning the power on (procedures 3 and 4).
10. Check that the processor cooling fans are operational (procedure 5).
11. Close and latch the equipment mounting frame. Replace and secure the cabinet front panel(s).

2 FAN FILTER CLEANING

To clean the fan filter, perform the following:

1. Remove the cabinet right side panel for access to processor 1 (figure 6-2) or the left side panel for access to processor 2 (figure 6-3).
2. Remove the filter from the chassis (see figure 6-2 or 6-3 for filter location). Use a vacuum cleaner to clean the front and back surfaces of the filter.
3. Check that the filter has been properly cleaned by holding the filter up to a light. No obvious dark areas should be seen. If it cannot be adequately cleaned, replace the filter.
4. Restore the filter to its housing. Replace and secure the cabinet side panel(s).

3 POWER TURN-ON

To turn the power on (figure 6-2 or 6-3), perform the following:

1. Check that the ac power cord from the processor cabinet power distribution box is connected to the site power outlet.
2. If the processor is being turned on for the first time, refer to procedures 7, 9, and 11 to verify that the voltages are within tolerance.
3. Place the POWER ON/OFF switch located on the control panel to the ON position. The POWER ON indicator should illuminate. If the POWER ON indicator does not illuminate, replace the lamp. If the indicator still does not illuminate, refer to procedures 7, 9, and 11 to check the power supplies.

4 POWER TURN-OFF

To turn the power off (figure 6-2 or 6-3), perform the following:

1. Press STOP and MASTER CLEAR on the control panel.
2. Place the control panel ON/OFF switch in the OFF position.

5 COOLING FANS CHECK

To check the cooling fans (figure 6-4), perform the following:

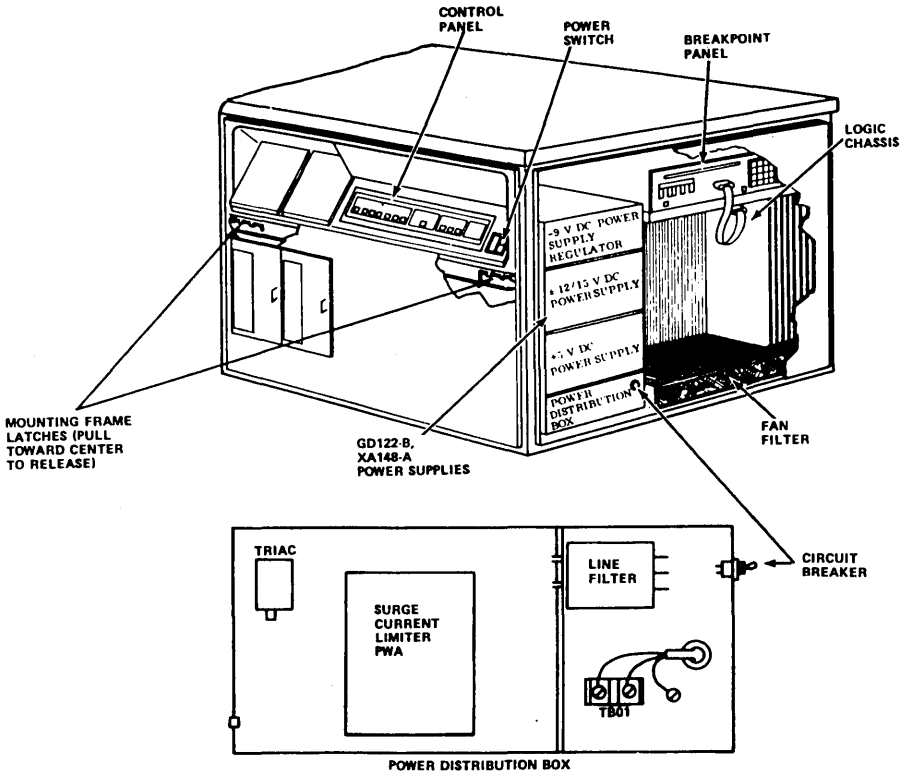
1. Remove the cabinet right side panel for access to processor 1 or the left side panel for access to processor 2. Remove the cabinet filter (see figure 6-2 or 6-3 for filter location).
2. Insert an inspection mirror into the air intake opening. Do not touch the running fan blades.
3. Direct the light from a flashlight into the mirror while angularly directing the mirror toward one of the six cooling fans.
4. Verify that the fan blades are in motion.
5. Repeat steps 3 and 4 for all six cooling fans.
6. Replace the cabinet filter.
7. Check that air is being exhausted from the back of the cabinet and power supply exhaust fans. If it is not, replace the power supply or cabinet exhaust fans (procedures 8 and 10).
8. Replace and secure the cabinet side panel(s).

6 COOLING FANS REPLACEMENT

To replace the cooling fans (figure 6-5), perform the following:

1. Turn the power off (procedure 4).
2. Remove the cabinet right side panel for access to processor 1 or left side panel for access to processor 2.

PROCESSOR WITH GD122-B AND XA148-A POWER SUPPLIES



PROCESSOR WITH L. H. RESEARCH POWER SUPPLY

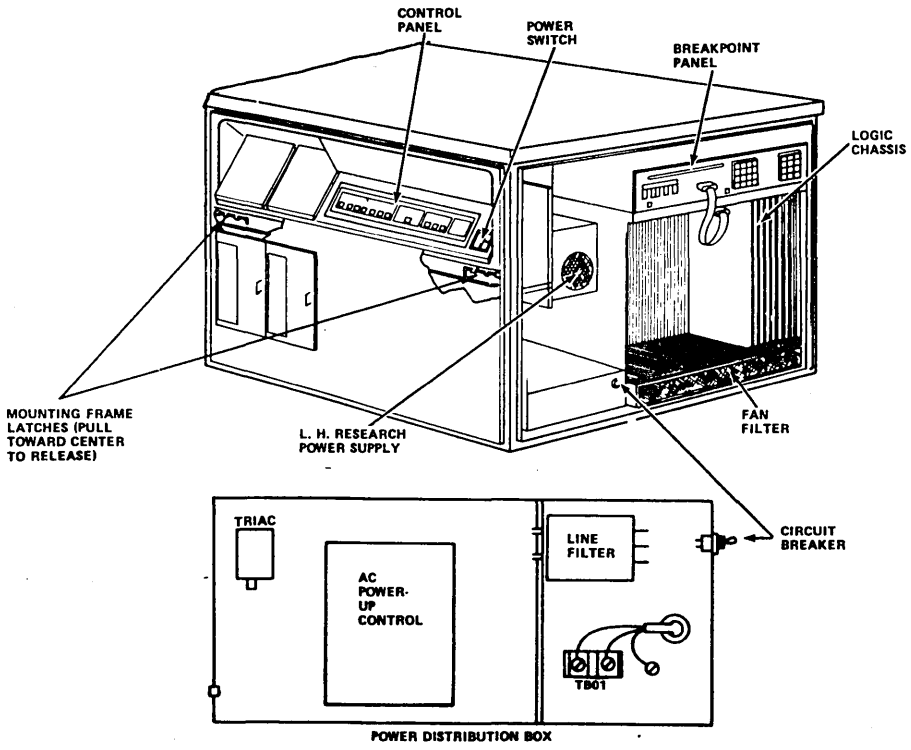


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Figure 6-2. Single-Processor Cabinet Parts Location

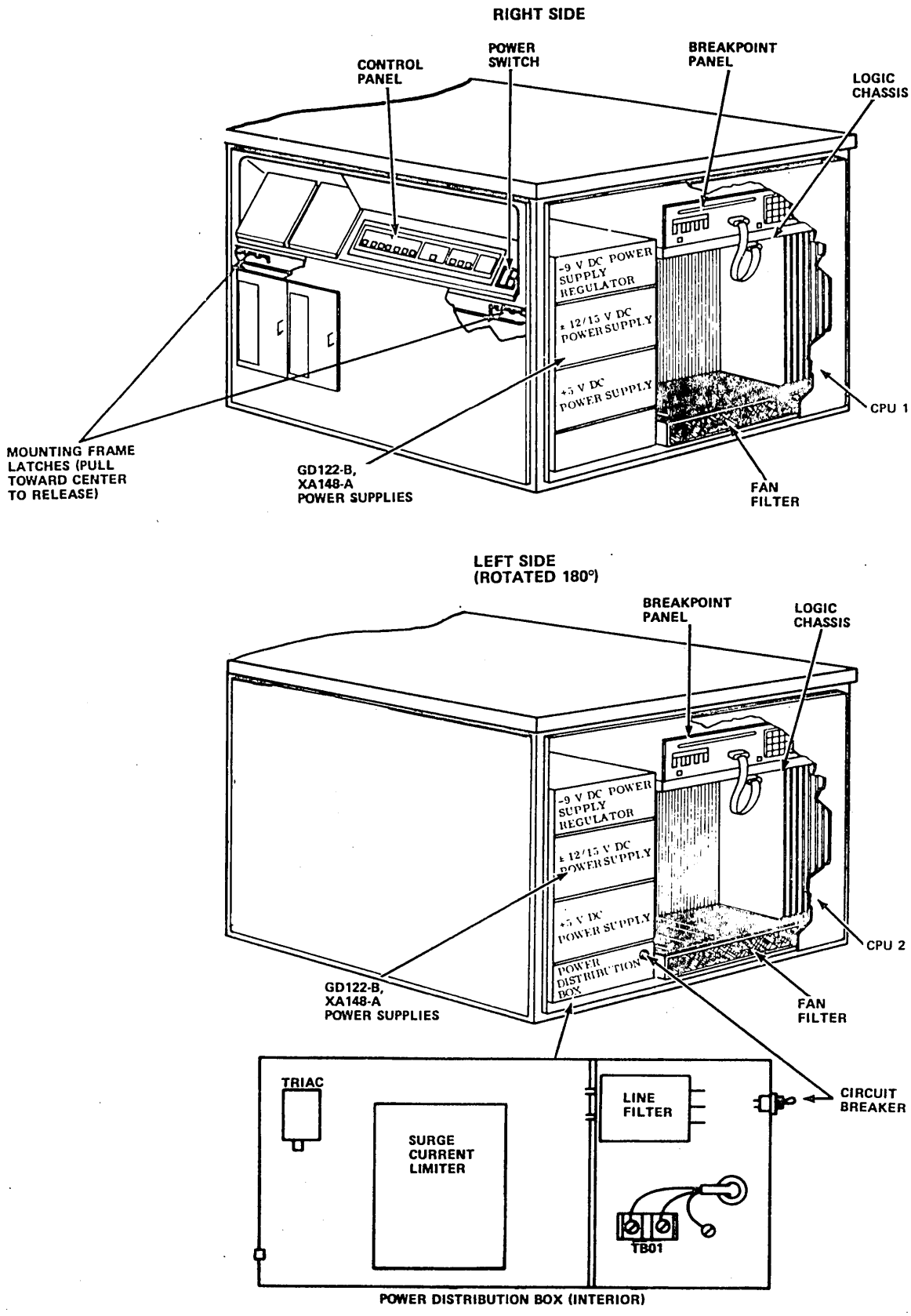


Figure 6-3. Dual-Processor Cabinet Parts Location (Sheet 1 of 2)

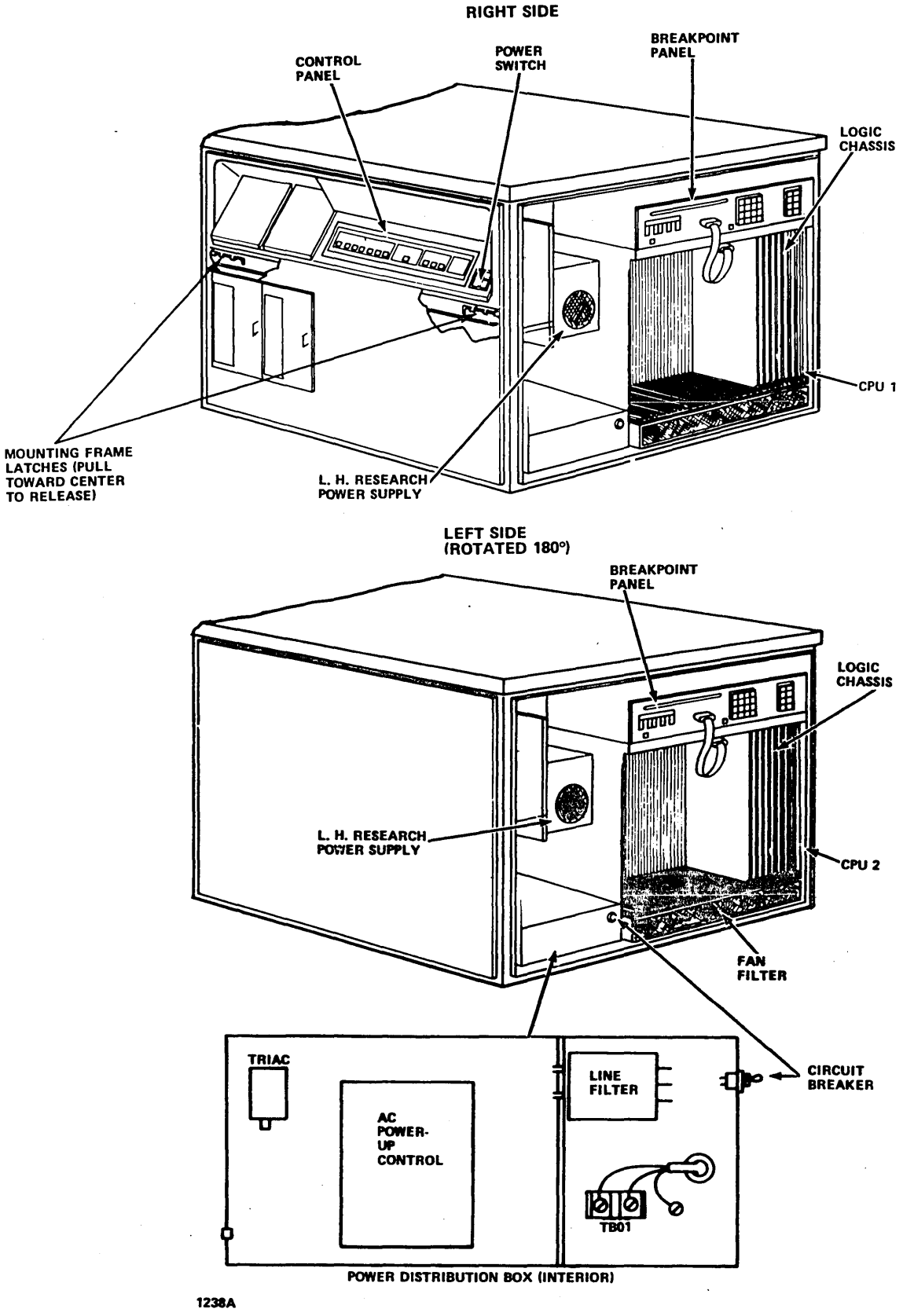


Figure 6-3. Dual-Processor Cabinet Parts Location (Sheet 2 of 2)

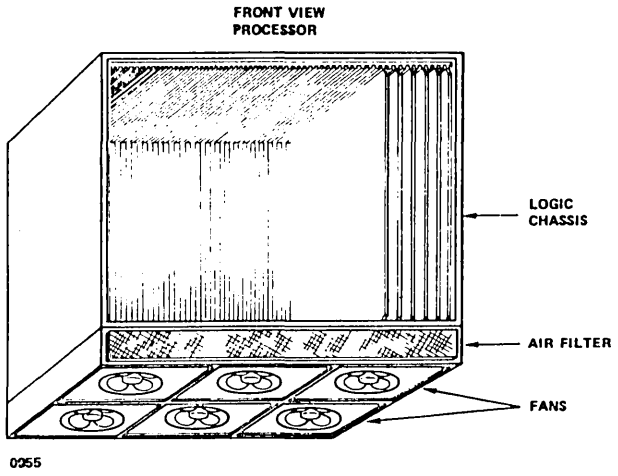


Figure 6-4. Processor Cooling Fans

3. Remove the cabinet filter (see figure 6-2 or 6-3 for filter location).

4. Using either a 1/4-inch open-end wrench, a 1/4-inch spin-tight wrench, or a Phillips-head screwdriver, remove the screws holding the cooling fan to be replaced.

5. Remove the power connect plug to the cooling fan.

6. Remove the screws and the fan grill from the old fan.

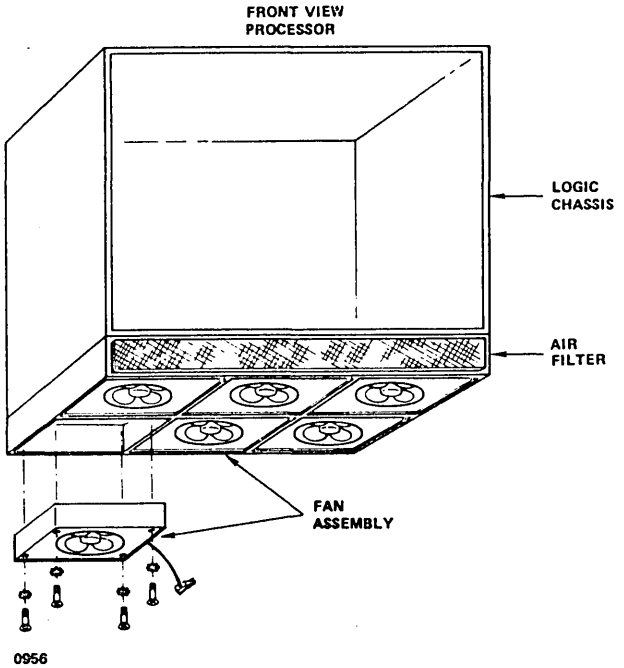


Figure 6-5. Cooling Fan Assembly

7. Before inserting the new fan into the chassis, orient the new fan so that the air flow notation arrows on the fan are pointing upward.

8. Insert the new fan and connect it to the power plug.

9. Install the fan grill and the screws on the fan, and fasten the assembly to the chassis.

10. Turn the power on (procedure 3), and verify proper operation (procedure 5).

11. Replace the cabinet filter and cabinet panel(s).

7 +5 V DC POWER SUPPLY CHECK

L.H. Research

To check the dc power supply (figure 6-6), perform the following:

1. Remove the cabinet front snap-on panel(s). Unlatch and swing down the equipment mounting frame (see figure 6-2 or 6-3).

2. Remove the cabinet side panel(s) and check that the cabinet blowers are running by detecting the air flow through the processor logic chassis. If they are not running, check the power connection to the site outlet.

3. Set a multimeter to a dc voltage range capable of clearly displaying 5 V dc.

4. Connect the negative lead of the multimeter to the -V1 terminal and the positive lead to the +V1 terminal. The meter should read 5 V ± 0.25 V dc. If the voltage is not correct (low), adjust the V1 ADJ potentiometer (a clockwise turn increases the voltage) until the correct level is attained. Connect the negative lead to -V4 and the positive lead to +V4. The meter should read 5 V ± 0.25 V dc. If the voltage is not correct, adjust the V4 ADJ potentiometer. Set the multimeter to a dc range capable of clearly displaying 12 V dc. Connect the negative lead to -V2 and the positive lead to +V2. The meter should read 12 V ± 0.6 V dc. If the voltage is not correct, adjust the V2 ADJ potentiometer. Connect the negative lead to -V3 and the positive lead to +V3. The meter should read 12 V ± 0.6 V dc. If the voltage is not correct, adjust the V3 ADJ potentiometer. If the power supply cannot be adjusted, replace the power supply (procedure 8).

5. If this is a dual-processor system, remove the rear cabinet panel and repeat the test on the second power supply. Replace and secure the equipment mounting frame and cabinet panels.

GD122-B

To check the +5 V dc power supply (see figure 6-7), perform the following:

1. Remove the cabinet front panel(s). Unlatch and swing down the equipment mounting frame (see figure 6-2 or 6-3).

2. Verify that the +5 V dc power supply circuit breaker (CB1) is on.

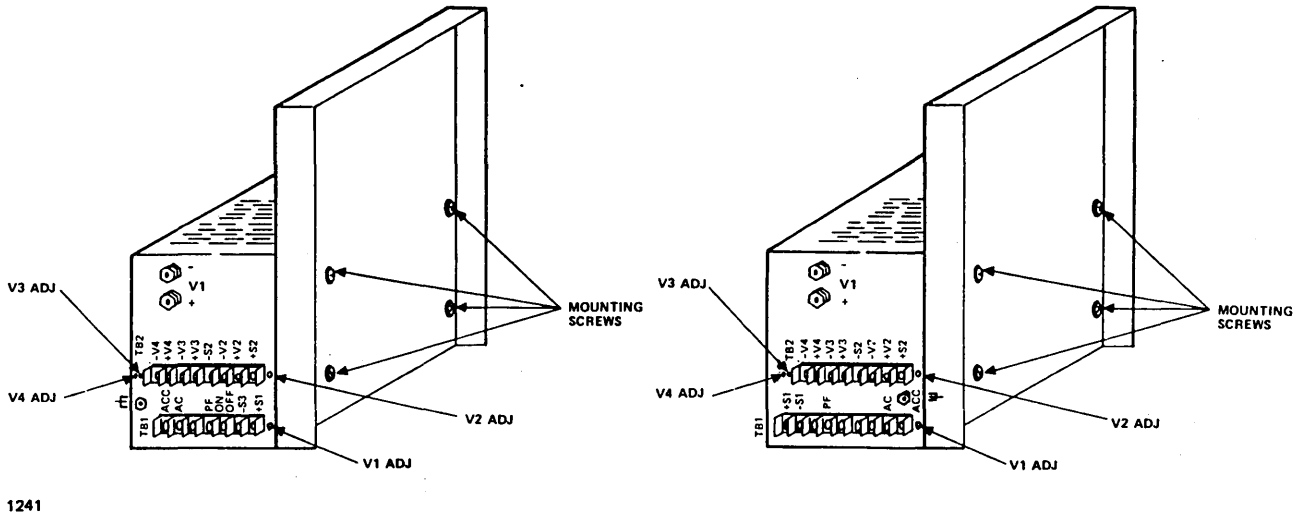


Figure 6-6. Power Supply and Mounting

3. Remove the cabinet side panel(s) and check that the cabinet blowers are running by detecting the air flow through the processor logic chassis. If they are not running, check the power connection to the site outlet.

4. Set a multimeter to a dc voltage range capable of clearly displaying 5 V dc.

5. Connect the negative lead of the multimeter to the +5 V RTN terminal and the positive lead to the +5 V OUT terminal. The meter should read 5 V dc ±0.25 V dc. If the voltage is not correct (low), adjust the VOLT ADJ potentiometer (a clockwise turn increases the voltage) until the correct level is attained. If the power supply cannot be adjusted, replace the +5 V dc power supply (procedure 8).

6. If this is a dual-processor system, remove the rear cabinet panel and repeat the test on the second power supply. Replace and secure the equipment mounting frame and cabinet panels.

8 +5 V DC POWER SUPPLY REPLACEMENT

L.H. Research

To replace the power supply (figure 6-7), perform the following:

1. Turn the power off (procedure 4) and disconnect the power cord from the primary source.

2. Remove the front and side panels. Unlatch and swing down the equipment mounting frame for processor 1. (Remove rear and left side panels for processor 2.)

3. Set a multimeter to a range capable of displaying 120 V ac. Connect the negative lead of the multimeter under the cover plate of TB1 on the power supply ACC terminal (figure 6-6). Connect the positive lead of the multimeter through the cover plate of TB1 to AC terminal.

NOTE

The multimeter should read zero voltage. If the multimeter does not read zero voltage, recheck the input ac power cord and disconnect it from the site power source.

4. Attach stick-on labels to the lugged wires connected to the +V1 and -V1 terminals. Identify (on the labels) the terminating location of each wire.

5. Remove the lugged wires from the +V1 and -V1 terminals using either a 1/2-inch open-end or spin-tight wrench.

6. Remove each wire from TB1, labeling it with its previous terminal location as it is removed, and remove ac ground (⏚) wire.

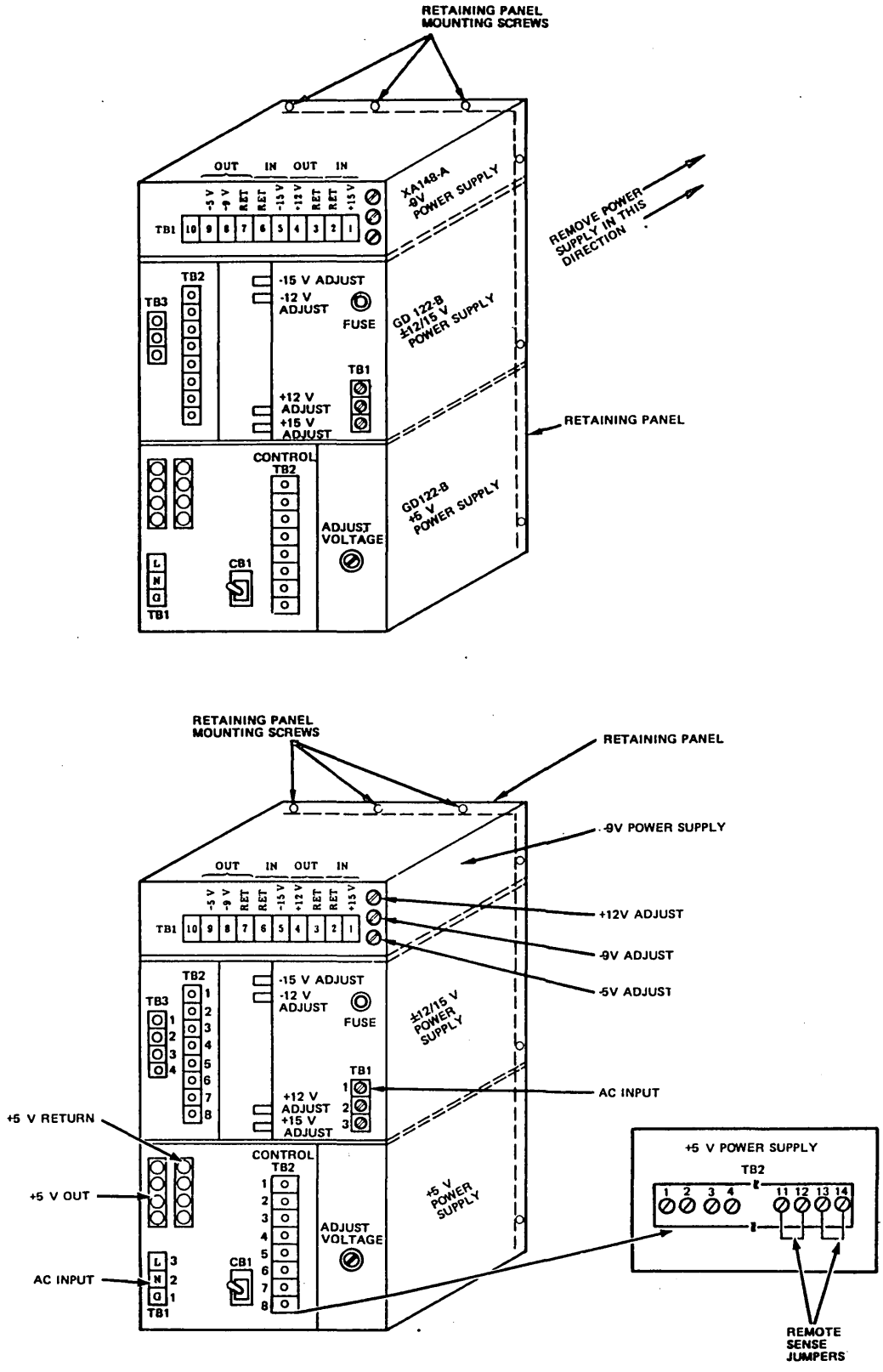


Figure 6-7. GD122-B and XA148-A Power Supplies

7. Remove each wire from TB2, labeling each with its previous location as it is removed.

8. Remove the four mounting screws from the power supply housing assembly.

9. Remove the power supply from its housing.

10. Install the new power supply onto the housing in the same orientation as the one that was removed.

11. Reconnect wires removed in step 6.

12. Turn the power on (procedure 3) and connect the negative lead of the multimeter, set to a range of displaying 10 V dc, to the -V1 terminal. Connect the positive lead of the multimeter to the +V1 terminal. The meter should read no greater than 5.5 V dc. If the meter reads greater than 5.5 V dc, adjust the V1 ADJ potentiometer on the power supply counterclockwise until a level of 5.5 V dc is attained.

13. Turn the power off (procedure 4) and connect the lugged wires (step 5) to the +V1 and -V1 terminals of the power supply. Ensure that the screws are tightened on the terminal.

14. Turn the power on (procedure 3) and again measure the voltage between the +V1 and -V1 terminals. Adjust the V1 ADJ potentiometer on the power supply until a level of 5 ± 0.25 V dc is attained. If the power supply cannot be adjusted, it may be necessary to obtain technical assistance.

15. Connect the negative lead to -V2 and the positive lead to +V2. The meter should read no greater than 13 V dc. If the meter reads greater than 13 V dc, adjust the V2 ADJ potentiometer clockwise until a level of 13 V dc is attained. Repeat for V3 (no greater than 13 V dc) and V4 (no greater than 5.5 V dc).

16. Turn the power off (procedure 4) and reconnect the wires removed from TB2 (step 7).

17. Turn the power on (procedure 3) and perform the power supply check (procedure 7) for V2, V3, and V4.

18. Disconnect the multimeter leads, replace the cover, and replace the cabinet panels.

19. Continue the DDLT testing sequence.

GD122-B

To replace the +5 V dc power supply (figure 6-7), perform the following:

1. Turn the power off (procedure 4), and disconnect the power cord from the primary source.

2. Remove the cabinet front and side panels. Unlatch and swing down the equipment mounting frame for processor 1. (Remove the rear and left side panels for processor 2).

3. Set a multimeter to a range capable of displaying 120 V ac. Connect the negative lead of the multimeter through the cover plate of TB1 on the +5 V dc power supply to terminal 3 (figure 6-7). Connect the positive lead of the multimeter through the cover plate of TB1 to terminal 1.

NOTE

The multimeter should read zero voltage. If the multimeter does not read zero voltage, recheck the input ac power cord and disconnect it from the site power source.

4. Attach stick-on labels to the lugged wires connected to the 5 V OUT and 5 V RTN terminals. Identify (on the labels) the terminating location of each wire.

5. Remove the lugged wires from the +5 V OUT and +5 V RTN terminals using either a 7/16-inch open-end or spin-tight wrench.

6. Remove each wire from TB1, labeling it with its previous terminal location as it is removed.

7. Remove each wire from TB2, labeling it with its previous location as it is removed.

8. Remove the nine retaining panel mounting screws at the rear of the power supply housing. Remove the retaining panel.

9. Remove the three screws in front of the power supply housing (power terminating end).

10. Remove the power supply from its housing by pulling the power supply out from the rear of the housing.

11. Install the new power supply into the housing in the same orientation as the one that was removed.

CAUTION

Severe electrical damage results to the system if remote sensing terminal jumpers are removed or left open with the power on.

12. Connect the +5 V dc power supply remote sense and return terminal jumpers on TB2 as illustrated in figure 6-7.

13. Reconnect the new power supply removed in steps 6 and 7 above. Do not perform step 5.

14. Turn the power on (procedure 3) and connect the negative lead of the multimeter (set to a range of displaying 10 V dc) to the +5 V RTN terminal. Connect the positive lead of the multimeter to the +5 V OUT terminal. Check that the circuit breaker switch (CB1) on the power supply is in the on position. The meter should read no greater than +5.5 V dc. If the meter reads greater than +5.5 V dc, adjust the VOLT ADJ potentiometer on the power supply counterclockwise until a level of +5.5 V dc is attained.

15. Turn the power off (procedure 4) and connect the lugged wires (step 5) to the +5 V OUT and +5 V RTN terminals of the power supply. Ensure that the screws are tightened on the terminal.

16. Turn the power on (procedure 3) and again measure the voltage between the +5 V OUT and +5 V RET terminals. Adjust the VOLT ADJ potentiometer on the power supply until a level of 5 V dc ± 0.25 V dc is attained. If the power supply cannot be adjusted, it may be necessary to obtain technical assistance.

17. Check the power fail signal level. To do this, connect the negative probe of the multimeter to terminal TB2-4 and the positive probe to TB2-3. The meter should read a voltage greater than +2.5 V dc but less than +5.5 V dc. If the voltage is not correct, check that the interconnection of the wires between this power supply and the ±15/±12 V dc power supply agree with table 6-12. If correct, then turn the power off (procedure 4) and remove the wires terminating at TB2-4 and TB2-3 of the +5 V dc power supply. Turn the power on (procedure 3) and again measure the voltage at these terminals as described above. If the voltage is correct, replace the ±15/±12 V dc power supply. If the voltage is not correct, replace the +5 V dc power supply.

18. Disconnect the multimeter leads, replace the cover, and replace the cabinet panels.

19. Continue the DDLT testing sequence.

9 ±15/±12 V DC POWER SUPPLY CHECK

To check the ±15/±12 V dc power supply (see figure 6-7), perform the following:

1. Remove the front panel from the processor cabinet. Unlatch and swing out the equipment mounting frame.

2. Remove the cabinet side panel(s) and check that the cabinet blowers are running by detecting air flow through the logic chassis. If they are not running, check the power connection to the site outlet.

3. Set a multimeter to a dc voltage range capable of clearly displaying 15 V dc.

4. Connect the multimeter leads to the TB2 terminals as described in table 6-13. Adjust the potentiometer as indicated. If the voltage cannot be adjusted, power down the system, asdescribed in procedure 4, and check the fuse (figure 6-7). If the power supply cannot be adjusted, replace the ±15/±12 V dc power supply (procedure 10).

5. If this is a dual-processor system, remove the rear cabinet panel and repeat the tests on the second power supply.

6. Secure the equipment mounting frame and cabinet panels.

7. Resume the DDLT testing sequence.

10 ±15/±12 V DC POWER SUPPLY REPLACEMENT

To replace the ±15/±12 V dc power supply (figure 6-7), perform the following:

1. Turn the power off (procedure 4), and disconnect the power cord from the primary source.

2. Remove the front and right side panels for access to processor 1. Unlatch and swing down the equipment mounting frame. (Remove the rear and left side panels for access to processor 2).

3. Set a multimeter to a range capable of displaying 120 V ac. Connect the negative lead of the multimeter through the cover plate of TB1 to terminal 3 on the ±15/±12 V dc power supply (figure 6-7).

   Connect the positive lead of the multimeter through the cover plate of TB1 to terminal 1.

   NOTE

   The multimeter should read zero voltage. If the multimeter does not read zero voltage, recheck the input ac power cord, disconnect it from the site power outlet, and repeat step 3.

TABLE 6-12. GD122-B POWER SUPPLY INTERCONNECTING WIRES (+5 and ±15/±12 V DC)

From	To
+5 V dc power supply	± 15/12 V dc power supply
TB1-1	TB1-1
TB1-2	TB1-2
TB1-3	TB1-3
TB2-3	TB3-1
TB2-4	TB3-2
TB2-5	TB3-3
TB2-6	TB3-4
+5 V dc power supply	+5 V dc power supply
TB2-11	TB2-12
TB2-13	TB2-14

TABLE 6-13. TEST VOLTAGE READINGS

Negative Lead	Positive Lead	Reading Should Be No Greater Than	If Reading is Greater, Adjust Potentiometer Counterclockwise to
TB2-8	TB2-7	15 V dc ± 0.7 V dc	+15 V dc
TB2-6	TB2-5	12 V dc ± 0.6 V dc	+12 V dc
TB2-3	TB2-4	12 V dc ± 0.6 V dc	-12 V dc
TB2-1	TB2-2	15 V dc ± 0.7 V dc	-15 V dc

4. Attach stick-on labels to the lugged wires connected to the terminals of TB2 and TB3.

5. Remove each wire from TB2 and identify on its label its previous terminal location on TB2. Remove each wire of TB3 and identify on its label its previous terminal location.

6. Remove the nine retaining panel mounting screws at the rear of the power supply housing and remove the retaining panel.

7. Remove the three screws in front of the power supply housing.

8. Remove the power supply from its housing by pulling it out from the rear of the housing.

9. Install the new power supply into the housing in the same orientation as the one that was removed.

10. Connect the new power supply in reverse order starting with step 8 and end with step 5 above. Do not reconnect the TB2 wires (step 5).

11. Turn the power on (procedure 3). Connect the negative and positive leads of a multimeter; set it to a range capable of displaying 15 V dc to the terminal locations described in table 6-14.

12. Turn off the power and connect the lugged wires (step 5) to terminal block TB2.

13. Turn the power on and again measure the voltage at terminal block TB2 (table 6-15). If the voltage cannot be adjusted, it may be necessary to obtain technical assistance.

14. Check the power fail signal level. To do this, set the multimeter to a range capable of displaying 5 V dc. Connect the negative probe of the meter to TB3-2 and the positive probe to TB3-1. The meter should read a voltage greater than +2.5 V dc less than +5.5 V dc. If the voltage is not correct, perform step 16 of procedure 8 (GD122-B power supply).

15. Disconnect the multimeter leads, and replace the cabinet panels.

16. Continue the DDLT testing sequence.

11 -9 V DC POWER SUPPLY CHECK

To check the -9 V dc power supply (figure 6-7), perform the following:

1. Remove the cabinet panel. Unlatch and swing down the equipment mounting frame.

2. Remove the cabinet side panel(s) and check that the power supply blowers are running by detecting air flow through the logic chassis. If the blowers are not running, check the power connection to the site outlet.

TABLE 6-14. TEST VOLTAGE READINGS (NOT LOADED)

Negative Lead	Positive Lead	Reading Should Be No Greater Than	If Reading Is Greater, Adjust Potentiometer Counterclockwise to
TB2-8	TB2-7	16.5 V dc	+15 V dc
TB2-6	TB2-5	13.2 V dc	+12 V dc
TB2-3	TB2-4	13.2 V dc	-12 V dc
TB2-1	TB2-2	16.5 V dc	-15 V dc

TABLE 6-15. TEST VOLTAGE READINGS (LOADED)

Negative Lead	Positive Lead	Reading Should Be No Greater Than	If Reading Is Not Correct, Adjust Potentiometer Counterclockwise to
TB2-8	TB2-7	15 V dc ± 0.7 V dc	+15 V dc
TB2-6	TB2-5	12 V dc ± 0.6 V dc	+12 V dc
TB2-3	TB2-4	12 V dc ± 0.6 V dc	-12 V dc
TB2-1	TB2-2	15 V dc ± 0.7 V dc	-15 V dc

3. Set a multimeter to a dc voltage range capable of displaying -9 V dc.
4. Connect the meter leads to -9 V dc test points TB1-7 (positive) and TB1-8 (negative). Adjust the potentiometer for -9 V dc ±0.5 V dc.
5. If the power supply cannot be adjusted, turn the power off (procedure 4) and replace the power supply (procedure 12).
6. If this is a dual-processor system, remove the rear cabinet panel and repeat the tests on the second power supply.
7. Secure the equipment mounting frame and cabinet panels.
8. Resume the DDLT testing sequence.

12 -9 V DC POWER SUPPLY REPLACEMENT

To replace the -9 V dc power supply (figure 6-7), perform the following:

1. Turn the power off and disconnect the power cord from the primary source.
2. Remove the front and right side panels for processor 1. Unlatch and swing down the equipment mounting frame. (Remove the rear and left side panels for processor 2).
3. Set a multimeter to a range capable of displaying 120 V ac. Connect the negative lead of the meter to TB1-3 and the positive lead to TB1-1 on the +5 V dc power supply (figure 6-7).

NOTE

The multimeter should read zero. If the meter reading is not zero volts, recheck and disconnect the input ac power from the site source.

4. Attach stick-on labels to the lugged wires connected to the terminals of TB1 of the -9 V dc power supply.
5. Identify each wire (with the labels) as to its location on the terminal block (figure 6-7).
6. Remove the identified wires from TB1 of the -9 V dc power supply.
7. Remove the nine mounting screws holding the retaining panel at the rear of the power supply housing (figure 6-7).
8. Remove the two screws at the left front of the power supply housing.
9. Remove the power supply by pulling it out from the rear of the housing.
10. Install the new power supply into the housing in the same orientation as the one that was removed.
11. Reconnect the wires identified in step 5 as input wires (TB1-1, TB1-2, TB1-5, and TB1-6) to the new power supply.
12. With the multimeter set to read 15 V dc, turn the processor power on (procedure 3) and make the voltage tests listed in table 6-16. (If +15 V dc or -15 V dc cannot be adjusted, perform procedures 7 and 9.)
13. Reconnect the remaining output wires to TB1-3, TB1-4, TB1-7, TB1-8, and TB1-9.
14. Make the voltage tests and readjustments as in step 12.
15. Disconnect the meter leads, and replace and secure the cabinet panels.
16. Continue the DDLT testing sequence.

13 POWER DISTRIBUTION BOX COMPONENTS CHECK

Checking components of the power distribution box requires the use of a vom and the following procedure (figure 6-8):

1. If this is a single-processor system, remove the front panel from the processor cabinet (figure 6-2). Release the latches and swing down the equipment mounting frame.
2. If this is a dual-processor system, remove the rear panel from the cabinet (figure 6-3).
3. Take out the six mounting screws, and remove the cover from the power distribution box.

TABLE 6-16. POWER SUPPLY VOLTAGE ADJUSTMENT

Negative Lead	Positive Lead	Reading Should Be	Adjust Potentiometer
TB1-2	TB1-1	+15 V dc	+15 V adjust on ±15 V dc/±12 V dc power supply
TB1-6	TB1-5	-15 V dc	-15 V adjust on ±15 V dc/±12 V dc power supply
TB1-3	TB1-4	+12 V dc	+12 V adjust on -9 V dc power supply
TB1-7	TB1-8	-9 V dc	-9 V adjust on -9 V dc power supply
TB1-7	TB1-9	-5 V dc	-5 V adjust on -9 V dc power supply

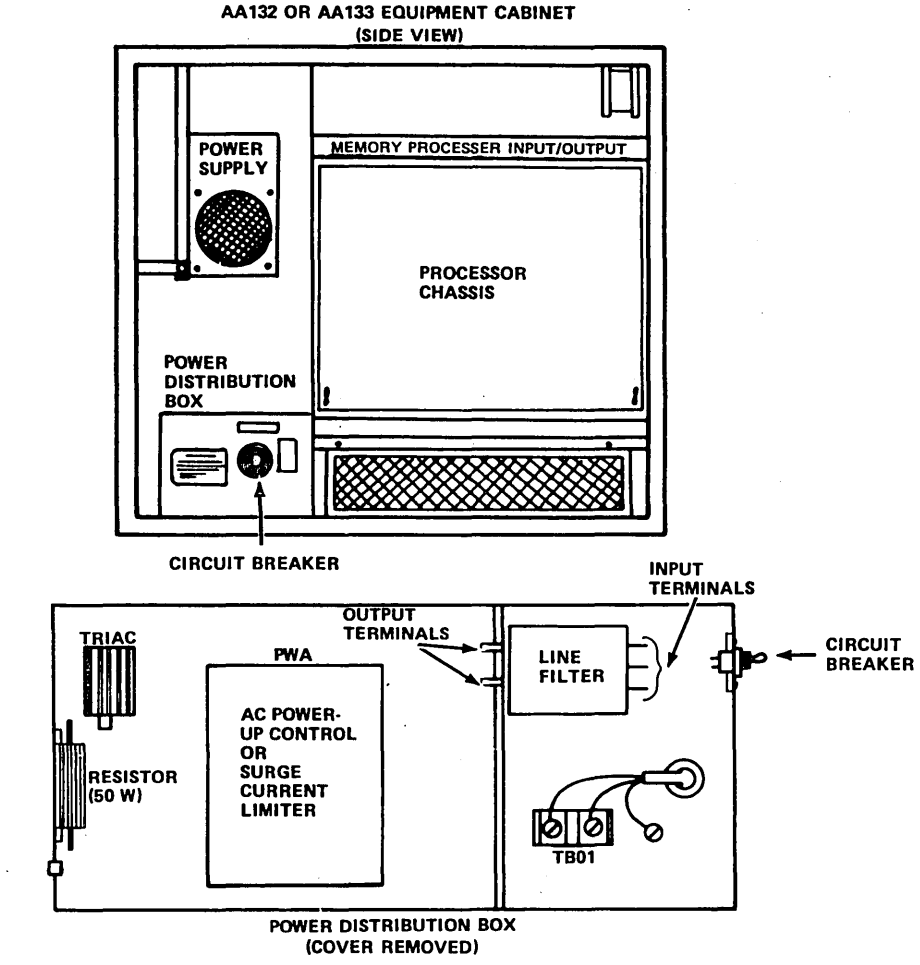


Figure 6-8. Power Distribution Box Parts Location

4. With the vom set to read 300 V ac, check the input voltage on terminals 1 and 2 of TB01. The voltage should be 120 V ac ±10 percent.

5. With the vom set to read 300 V ac, check the voltage on the output terminals of the line filter. The voltage should indicate approximately 0.8 percent less than step 4 when fully loaded.

6. With ac power off, measure the voltage across T1 and T2 of the triac. If the meter reads 120 V ac, the triac and surge current limiter PWA are all right. If the meter reads 0 V the triac is shorted and must be replaced (procedure 18). If the meter reads 70 V ac to 100 V ac, the surge current limiter PWA is bad and must be replaced (procedure 15).

   With ac power on, measure the voltage across T1 and T2 of the triac. If the meter reads 120 V ac, the triac is open and must be replaced (procedure 18). If the meter reads 0 V ac, the triac and PWA are all right. If the meter reads 70 V through 100 V ac, the PWA is bad and must be replaced (procedure 15).

7. Remove the meter leads and replace the cover on the power distribution box.

8. Close the equipment mounting frame, and reinstall the front panel on the cabinet.

9. Continue with the DDLT testing sequence.

14 AC LINE FILTER REPLACEMENT

To replace an ac line filter (figure 6-8), perform the following:

1. Turn off the power (procedure 4), and disconnect the power cord from the primary source.

2. Remove the front panel from the processor cabinet for a single-processor system. Then release the latches and swing down the equipment mounting frame.

3. Remove the rear panel from the cabinet for a dual-processor system.

4. Remove the six screws and take off the cover from the power distribution box.

5. Refer to figure 6-8 and locate the line filter.

6. Identify and remove the wires from the line filter.

7. Take out the four mounting screws and remove the line filter from the power distribution box.

8. Install the new line filter with the same orientation and before. Replace the mounting screws and wires.

9. Reinstall the power distribution box cover and replace the cabinet panels.

10. Reconnect the power cord to the primary power source, and continue the DDLT testing sequence.

15 POWER DISTRIBUTION BOX PWA REPLACEMENT

To replace the printed wiring assembly (PWA) in the power distribution box (figure 6-8), proceed as follows:

1. Turn off the power (procedure 4) and disconnect the power cord from the primary source.

2. Remove the front panel from the cabinet for a single-processor system. Release the latches and swing down the equipment mounting frame.

3. Remove the rear left panel from the cabinet for a dual-processor system.

4. Refer to figure 6-8 and locate the PWA.

5. Identify and remove the wires from the PWA.

6. Release the four mounting screws and remove the PWA and the standoffs.

7. Install the new PWA on the standoffs with the same orientation as before, and replace the four mounting screws.

8. Reconnect the wires to the PWA as they were marked, and replace the power distribution box cover.

9. Replace and secure the cabinet panels.

10. Reconnect the power cord to the primary power source and continue with the DDLT testing sequence.

16 POWER DISTRIBUTION BOX CIRCUIT BREAKER CHECK/REPLACEMENT

To check and/or replace the circuit breaker in the power distribution box, proceed as follows:

1. Turn off all power to the processor (procedure 4) and disconnect the power cord from the primary source.

2. Refer to figure 6-8 and locate the circuit breaker.

3. Remove the front and right side panels from the cabinet for a single-processor system. Then release the latches and swing down the equipment mounting frame.

4. Remove the rear and left side panels from cabinet for a dual-processor system.

5. Identify and remove the wires from the circuit breaker.

6. With an ohmmeter, check for continuity across the circuit breaker terminals. If no continuity is present, press the circuit breaker reset button and check again. If there is still no continuity, replace the circuit breaker.

7. Remove the circuit breaker by removing the two mounting screws on the outside of the power distribution box and pulling the circuit breaker out through the inside of the power distribution box.

8. Install the new circuit breaker with the same orientation as before. Replace the mounting screws. Reconnect the wires removed in step 5.

9. Reinstall the power distribution box cover and replace the cabinet panels.

10. Reconnect the power cord to the primary source and continue the DDLT testing sequence.

17 POWER DISTRIBUTION BOX RESISTOR ASSEMBLY REPLACEMENT

To replace the power distribution box resistor assembly (figure 6-8), perform the following.

1. Turn off the power (procedure 4) and disconnect the power cord from the primary power source.

2. Remove the front panel from the processor cabinet for a single-processor system. Release the latches and swing down the equipment mounting frame.

3. Remove the rear panel from the cabinet for a dual-processor system.

4. Refer to figure 6-8 and locate the resistor assembly.

5. Open the power distribution box cover by removing the six mounting screws.

6. Identify and remove the two wires from the PWA.

7. Remove the two resistor mounting screws.

8. Install the new resistor assembly, maintaining the same orientation.

9. Reconnect the wires removed in step 6.

10. Replace the power distribution box cover, and cabinet panels.

11. Reconnect site power to the system.

12. Continue the DDLT testing sequence.

18 TRIAC POWER SWITCH REPLACEMENT

To replace the triac power switch (figure 6-8), proceed as follows:

1. Turn off the power (procedure 4), and disconnect the power cord from the primary source.

2. Remove the front panel from the processor cabinet for a single-processor system. Release the latches and swing down the equipment mounting frame.

3. Remove the rear panel from the cabinet for a dual-processor system.

4. Refer to figure 6-8 and locate the triac.

5. Identify and remove the three triac wires from the surge current limiter PWA.

6. Using a 5/8-inch open-end wrench, carefully turn the triac counterclockwise to remove it from the heat sink.

7. Install the new triac in the heat sink and snug it down lightly with the wrench.

8. Reconnect the triac wires to the PWA, and reinstall the power distribution box cover.

9. Replace the cabinet panels and connect the power cord to the primary power source.

10. Continue the DDLT testing sequence.

19 POWER ON/OFF SWITCH CHECK/REPLACEMENT

To check or replace the processor POWER ON/OFF switch, proceed as follows:

1. Turn off power (procedure 4) and disconnect the power cord from the primary source

2. Remove the front panel from the processor cabinet.

3. Release the latches and pull the equipment mounting frame forward.

4. Refer to figure 6-2 or 6-3 to locate the switch.

5. Identify and remove wires from the switch. With an ohmmeter check for continuity across the switch terminals with the switch on, then off. If no change is noted on the ohmmeter, replace the switch.

6. Remove the switch by releasing the two spring locks at the top and bottom of the switch. Pull the switch straight out.

7. Install the new switch so that it is in the OFF position when the switch is down.

8. Reconnect the wires, close the equipment mounting frame, reinstall the cabinet panel, and connect the power cord to the primary power source.

9. Continue testing from the point of entry to this procedure.

20 CONTROL PANEL PWA REPLACEMENT

To replace the control panel PWA (figure 6-9), perform the following with the processor power off (procedure 4).

1. Pull out at the bottom of the right front panel and remove the panel from the cabinet.

2. Unlatch and swing down the equipment mounting frame.

3. Identify the cables and disconnect them from the PWA.

4. Remove the eight mounting screws and remove the PWA (figure 6-9).

5. Position the new PWA in the location vacated by the old assembly and install the mounting screws.

6. Reconnect the cables to the PWA.

7. Secure the equipment mounting frame and the front panels in their proper positions.

8. Restore power to the processor (procedure 3).

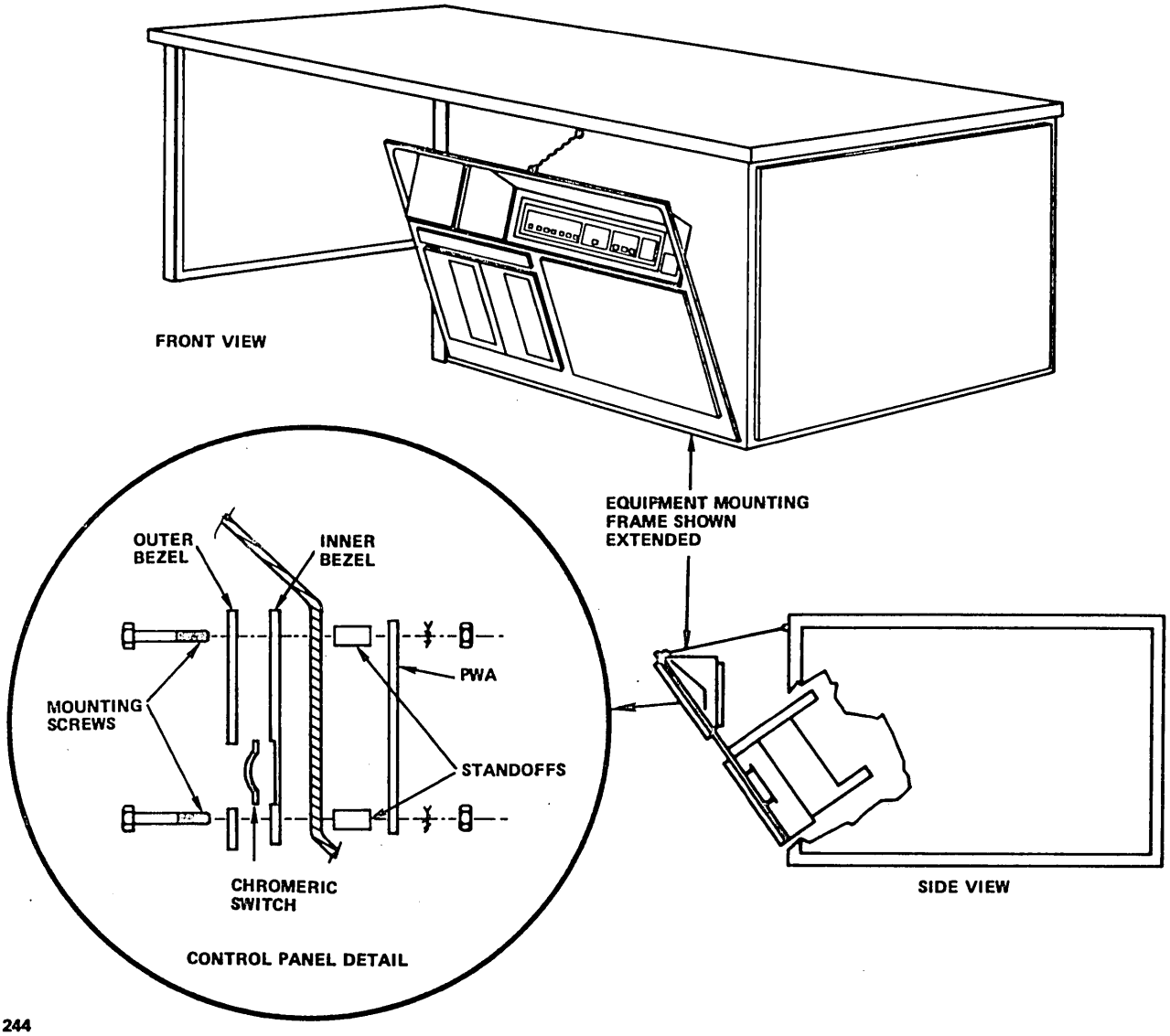


Figure 6-9. Control Panel Assembly

21 CONTROL PANEL SWITCH AND BEZEL REPLACEMENT

To replace a switch or bezel in the control panel (figure 6-9) proceed as follows:

1. Turn the power off (procedure 4).
2. Remove the front panel from the cabinet.
3. Remove the cable from the back of the switch assembly.
4. Reach through the mounting frame under the control panel and, while holding the PWA with the fingers on the inside and the bezel with the thumb on the outside, remove the eight mounting screws that hold the bezel plate to the control panel (figure 6-9).
5. Continue to hold the PWA in place and remove the bezel and switch assembly.
6. Temporarily re-install two mounting screws to retain the PWA in place while working on the switch and bezel assembly.
7. Separate the two sections of the bezel to expose the chromeric switch assembly (figure 6-9).
8. Remove and replace the switch assembly with a new one.
9. Reassemble the switch and two sections of the bezel. Replace the bezel plates if broken or damaged.
10. Reinstall the switch and bezel assembly by reversing steps 1 through 6.

22 DUAL-PROCESSOR MULTIPLEXER PWA REPLACEMENT

To replace the dual-processor multiplexer printed wiring assembly (figure 6-9), proceed as follows:

1. Turn off the POWER ON/OFF switch on the processor control panel.
2. Pull out at the bottom of the front panel and remove the panel from the cabinet.
3. Unlatch and swing down the equipment mounting frame.
4. Identify the cables and disconnect them from the PWA.
5. Remove the four mounting screws and lift out the PWA (figure 6-9).
6. Position the new PWA in the location vacated by the old assembly and install the mounting screws.
7. Reconnect the cables to the PWA.
8. Secure the equipment mounting frame.
9. Restore power to the processor.

23 BOARD (LOGIC) REPLACEMENT

To replace the logic boards (PWAs), perform the following.

1. Turn the power off (procedure 4).
2. Remove the right side panel from the cabinet for access to processor 1 (figure 6-2) or left side panel for access to processor 2 (figure 6-3).
3. Remove the processor cover plate by rotating the two captive fasteners one quarter turn counterclockwise.
4. Refer to table 6-17 and locate the processor or memory board to be replaced. Refer to table 6-22 for the peripheral controller locations.
5. Using the card extractor tool (card number 88911900) attached to the processor cover place, slide the PWA out of the chassis, and place it on a flat surface.
6. Before installing the new (PWA), verify that all jumpers and switches correspond to the normal operating positions as defined in section 4 or the subsystem manual.
7. Position the PWA in the front of the logic chassis with the component side facing left.
8. Slide the PWA carefully into the chassis. Seat the board into the connector by applying firm thumb pressure at the upper and lower corners of the PWA.
9. Turn the power on (procedure 3), and execute the DDLTs starting with table 6-1 to verify proper operation.
10. Replace the processor cover and secure the side panel on the cabinet.

24 MOS MEMORY PWA REPLACEMENT

1. Turn the power off (procedure 4).
2. Remove the right side panel from the cabinet for access to processor 1 and the left side panel for access to processor 2.

TABLE 6-17. PROCESSOR AND MEMORY BOARD LOCATION

To Replace	Remove and Replace	Slot
I/O-TTY logic	I/O-TTY board	K
SMI logic	SMI board	L
ALU logic	ALU board	M
Control 2 logic	Control 2 board	N
Control 1 logic	Control 1 board	P
Transform logic	Transform board	R
Micro-memory logic	Micro-memory board	S or T
Breakpoint logic	Breakpoint controller board	U
Memory interface logic (data)	Memory interface board (data)	V (see procedure 25)
Memory interface logic (address)	Memory interface board (address)	W (see procedure 25)
Memory	Memory board	X, Y, Z, AC (see procedure 24)

3. Remove the processor cover plate by rotating the two captive fasteners counterclockwise.

4. Refer to figure 6-10 and locate the memory PWA to be removed.

5. Using the extractor tool attached to the inside of the processor cover plate, slide the memory PWA out.

6. Position the new PWA in the vacated position with the component side of the PWA facing left.

7. Apply firm pressure at the upper and lower corners and seat the PWA into the backplane connector.

8. Refer to procedure 25, items 5 through 7, and verify the DMA priority switches on the memory interface PWA.

9. Replace the cover plate and the side panel, and turn on the processor power (procedure 3).

25 MEMORY INTERFACE PWA REPLACEMENT

1. With the power off, remove the right side panel from the processor cabinet for access to processor 1 or remove the left side panel for access to processor 2.

2. Remove the cover plate from the processor by rotating the two captive fasteners counterclockwise.

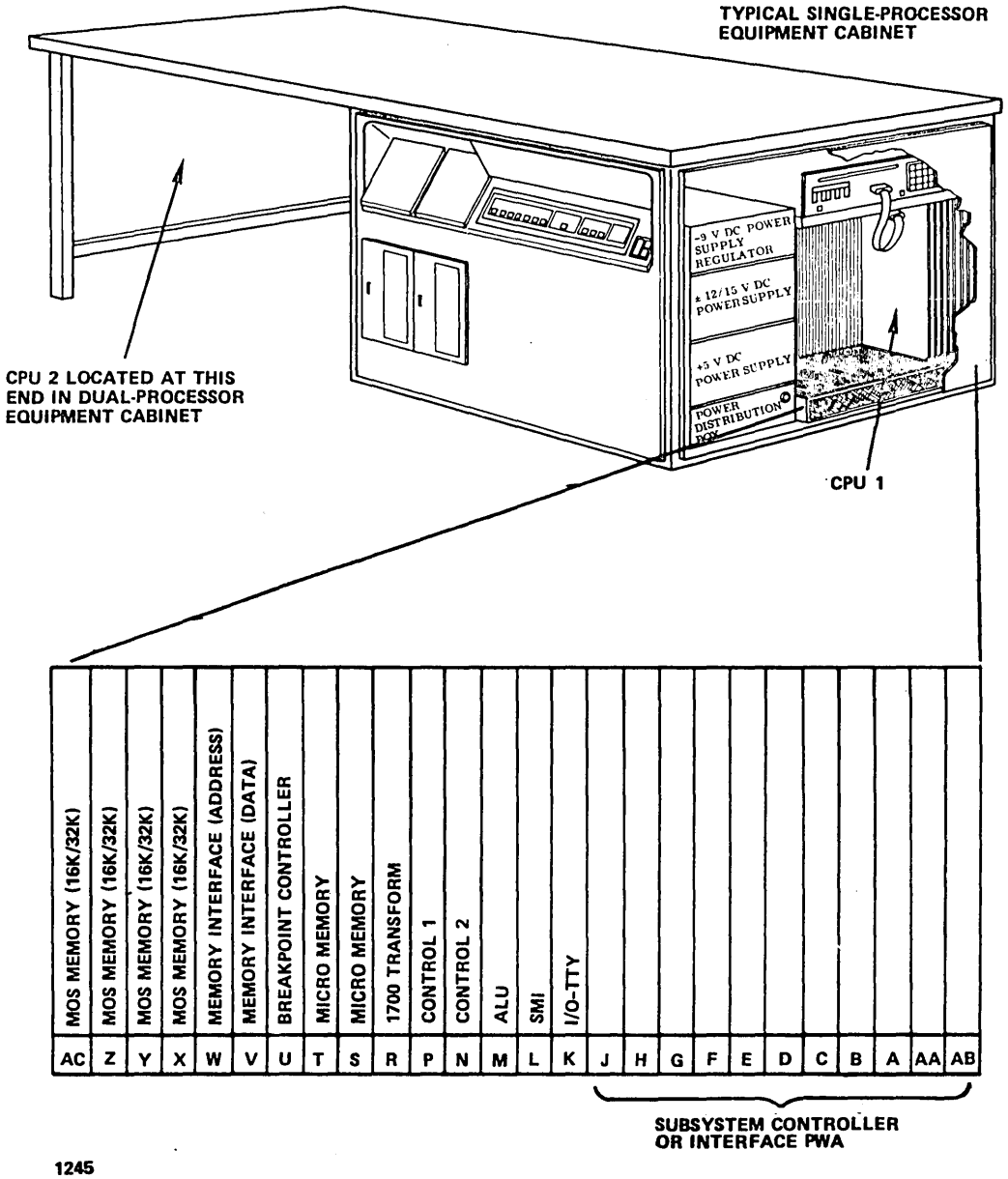


Figure 6-10. PWA Location

3. Refer to figure 6-10 and locate the memory interface PWAs (data and address).

4. Using the extractor tool attached to the front panel, slide the desired PWA(s) out.

5. Before installing new PWAs, DMA priority switches must be set. (Refer to figure 4-2 for normal settings.)

6. Position the new PWA(s) with new switch settings in the designated positions with the component side facing left.

7. Apply firm pressure at the upper and lower corners of the PWAs and seat them into their respective backplane connectors.

8. Replace the processor cover plate and side panels. Restore power to the processor.

26 MOS MAIN MEMORY RUN PARAMETERS

NOTES

1. Read the entire procedure before entering parameters in table 6-18.

2. In a dual-processor system, processor 1 is the AB113 and processor 2 is the AA109. The local processor is the one in which the diagnostic resides and can be either processor 1 or processor 2.

1. Examine the FCO tags on both sides of the front covers of processor 1 and processor 2 to determine the MOS memory configuration (slots X through AC). Fill in the equipment number columns of table 6-18.

2. Fill in the 16K blocks per PWA column of table 6-18 using the following information.

Equipment Number	PWA Type	16K Blocks per PWA
AT241	32K array	2
AT275	16K array	1
DT223	Error correction code array	0

Calculate the total number of 16K blocks per processor for each processor by adding up the 16K blocks per PWA in each processor.

3. Use the total number of 16K blocks for each processor (derived from table 6-18) and select the correct V, W, X, Y, Z parameters from table 6-19.

For example, if processor 1 is the local processor and has a total of six 16K blocks, follow the horizontal numbers at the top of table 6-19 to 6; and if processor 2 has a total of two 16K blocks, follow the vertical numbers at the left of the table to 2. At the point where they intersect on table 6-19 read the parameters:

V = 206
W = 2
X = 0
Y = 7FFF
Z = 7FFF

From table 6-20, determine the values for parameters T and U.

4. Utilizing the parameters derived from tables 6-19 and 6-20, enter the required test parameters as called for in the DDLTs:

DDLT/Test	Parameter Word and Input Values
Table 6-4, sheet 1, MPMOS test	A, _ _ _ → Parameter V D, _, _ _ _ _ → Parameter Z → Parameter W
Table 6-4, sheet 8, MOSMA test	A, _ _ _ → Parameter V D, _, _ _ _ _, _ → Parameter T → Parameter Y → Parameter X 3, _ _ _ _ → Parameter U
Table 6-7, sheet 1, PAGE1 test	A, _ _ _ → Parameter V

27 INTERRUPT/EQUIPMENT NUMBER ASSIGNMENT AND MULTIPLE SUBSYSTEMS TESTING

Tables 6-21 through 6-23 and figures 6-11 and 6-12 provide information on the standard interrupt and equipment number assignments. A completed copy of figure 6-11 should be installed on the processor chassis cover by the CE. This identifies the interrupt and equipment numbers assigned on that system. If one does not exist, it is necessary to fill out a blank copy of the form in order to run the system diagnostic when any nonstandard interrupts and equipment codes are used. (See steps outlined below under Diagnostic Parameter Changes for Nonstandard Interrupt/Equipment Number Assignments.)

TABLE 6-18. SYSTEM MOS MEMORY CONFIGURATION

Slot	Processor 1		Processor 2	
	Equipment Number	16K Blocks per PWA	Equipment Number	16K Blocks per PWA
X				
Y				
Z				
AC				
Total Number of 16K Blocks per Processor				

Table 6-21 identifies the normal/standard interrupt and equipment numbers that have been assigned to the various processor peripheral products. These are the recommended assignments and are used by most systems. When multiple equipments, specific equipment configurations, or software requirements create interrupt/equipment number conflicts, it is necessary for installing or maintaining personnel to change and log them accordingly.

All equipment numbers are selected on the individual controller/interface cards. Refer to the appropriate subsystem manual listed in the preface for specific details for selecting equipment numbers on the various peripherals.

Table 6-21 also shows the micro/macro interrupt output pin assignment for each of the controller/interfaces.

Table 6-22 lists the standard processor PWA slots and their types. For each slot position there is a list of equipment that is assigned. These assignments are for user convenience and may be interchanged to fit specific configurations. The only restriction is that A/Q-DMA controllers must be installed in A/Q-DMA slots. However, the flexible disk drive controller may be operated from either A/Q or A/Q-DMA slots.

Table 6-23 shows the standard interrupt wiring configuration for processor backplanes. The wiring configuration may be changed to meet system requirements.

Figure 6-12 is an example of how figure 6-11 might appear after being filled in to reflect a specific system.

If a system has multiple controllers installed, the second controller must use a nonstandard interrupt/equipment number assignment. The actual interrupt/equipment number used must be determined in order to run the diagnostic on the subsystem (see the steps outlined below under Determining Interrupt/Equipment Number Assignments for further information).

Determining Interrupt/Equipment Number Assignments

Perform the following to determine specific interrupt and equipment numbers:

1. Remove the cabinet side panel and processor cover plate.

2. Locate and remove the controller logic (PWA) from the logic chassis using the extractor tool provided on the inside of the front cover. Refer to table 6-22 for the controller PWA location.

3. Inspect the controller PWA jumpers and determine the equipment code of the subsystem (refer to the applicable subsystem manual).

4. Inspect the backplane wiring to determine which macro and micro interrupt lines are wired to the PWAs in question. In the case where an interrupt jumper plug is used, make sure the jumper plug and individual interrupt jumper wires are securely seated on the correct backplane pins. Refer to figures 6-11 and 6-12 and tables 6-21 through 6-23 to determine which interrupt lines are used.

Diagnostic Parameter Changes for Nonstandard Interrupt/Equipment Number Assignments

This procedure is used to change the diagnostic parameters for operation on a controller that has nonstandard assignments, and includes testing a second controller of a particular type. Perform the following:

1. Determine the assigned interrupt/equipment number used as described above.

TABLE 6-19. MOS MEMORY RUN PARAMETERS

16K Blocks per Remote Processor	16K Blocks per Local Processor								Parameters
	1	2	3	4	5	6	7	8	
	001	002	003	004	005	006	007	008	V
	0	0	0	0	1	1	1	1	W
0	0	0	0	0	1	1	1	1	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Z
	101	102	103	104	105	106	107	108	V
	2	2	2	2	2	2	2	2	W
1	0	0	0	0	0	0	0	0	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	3FFF	3FFF	3FFF	3FFF	3FFF	3FFF	3FFF	3FFF	Z
	201	202	203	204	205	206	207	208	V
	2	2	2	2	2	2	2	2	W
2	0	0	0	0	0	0	0	0	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	7FFF	7FFF	7FFF	7FFF	7FFF	7FFF	7FFF	7FFF	Z
	301	302	303	304	305	306	307	308	V
	2	2	2	2	2	2	2	2	W
3	0	0	0	0	1	1	1	1	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	BFFF	BFFF	BFFF	BFFF	BFFF	BFFF	BFFF	BFFF	Z
	401	402	403	404	405	406	407	408	V
	2	2	2	2	2	2	2	2	W
4	0	0	0	0	1	1	1	1	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	Z
	501	502	503	504	505	506	507	508	V
	3	3	3	3	3	3	3	3	W
5	0	0	0	0	1	1	1	1	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	3FFF	3FFF	3FFF	3FFF	3FFF	3FFF	3FFF	3FFF	Z
	601	602	603	604	605	606	607	608	V
	3	3	3	3	3	3	3	3	W
6	0	0	0	0	1	1	1	1	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	7FFF	7FFF	7FFF	7FFF	7FFF	7FFF	7FFF	7FFF	Z
	701	702	703	704	705	706	707	708	V
	3	3	3	3	3	3	3	3	W
7	0	0	0	0	1	1	1	1	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	BFFF	BFFF	BFFF	BFFF	BFFF	BFFF	BFFF	BFFF	Z
	801	802	803	804	805	806	807	808	V
	3	3	3	3	3	3	3	3	W
8	0	0	0	0	1	1	1	1	X
	3FFF	7FFF	BFFF	FFFF	3FFF	7FFF	BFFF	FFFF	Y
	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	Z

TABLE 6-20. ERROR CORRECTION CODE RUN PARAMETER

Local Processor, Slot AC	Parameter T	Parameter U
With Error Correction Code Array	3	789A
Without Error Correction Code Array	2	78A0

TABLE 6-21. RECOMMENDED EQUIPMENT AND INTERRUPT NUMBER ASSIGNMENTS

Peripheral Controller/Interface	Equipment Number	Standard Interrupt Assignment		Controller Backplane Interrupt Pin Assignment	
		Macro	Micro	Macro	Micro
Card reader/line printer (CR)	11	11†	11†	49	50
communication line (LP)	4	4†	4	249	250
adapter (CLA)	10	10	10	77	277
Card reader/line printer (CR)	11	11†	11†	49	50
(LP)	4	4†	4†	249	250
Cassette	7	7†	7†	249	250
Flexible disk drive (FDD) (A/Q)	7	7†	Not used	249	Not used
(A/Q-DMA)	13	13†	Not used	249	Not used
Module drive	14	14†	Not used	249	Not used
Dual-channel communication line adapter (DCCLA)	10	10†	10	249	250
Buffered communication line adapter (BCLA)	10	10†	10	249	250
Synchronous data link control communication line adapter (SDLC CLA)	10	10	Not used	249	Not used
Magnetic tape transport controller (NRZI)	9	9†	9†/0†	249	250
Magnetic tape transport controller (dual mode)	12	12	Not used	249	Not used
Cartridge disk drive	14	14†	Not used	249	Not used
Eight-channel communication line adapter	10	10†	Not used	249	250
Restart loader	6	6	Not used	249	Not used
Paper tape reader/paper tape punch	2	2†	2†	249	250
CYBER 18/1500 Series adapter††	2	2†	Not used	49	Not used
	3	3	Not used	249	Not used
A/Q expansion		Not assigned		249	250
DMA expansion		Not assigned		249	250

NOTE: When interrupt and equipment number assignments conflict, reselect these numbers as required.

† These interrupts are prewired in AA132-A and AA133-A processor backplanes.

†† The CYBER 18/1500 Series adapter cannot be installed in card slots that have deadstart backplanes.

This adapter is capable of providing up to eight interrupts that may be routed to the SMI board. Refer to the CYBER 18/1500 Series Adapter Hardware Reference/Maintenance Manual for additional pin assignments.

TABLE 6-22. STANDARD CONTROLLER SLOT ASSIGNMENTS

Slot	Type	Controller Type†
J	A/Q	Card reader/line printer, card reader/line printer/communication line adapter
H	A/Q-DMA	Module drive, cartridge disk drive
G	A/Q-DMA	Magnetic tape transport controller (dual mode)
F	A/Q	Eight-channel communication line adapter, dual-channel communication line adapter
E	A/Q	Flexible disk drive, cassette
D	A/Q-DMA	Synchronous data link control communication line adapter, buffered communication line adapter, flexible disk drive
C	A/Q	Restart loader, buffered communication line adapter expansion for slot D
B	Open††	Buffered communication line adapter for slot A
A	A/Q-DMA	Buffered communication line adapter, synchronous data link control communication line adapter, DMA expansion
AA	A/Q	Dual-channel communication line adapter, paper tape reader/paper tape punch, A/Q expansion
AB	SET/SAM	Magnetic tape transport (NRZI)

†The first device shown represents the primary slot assignment. The second and third devices represent alternate assignments. In system configurations with multiple devices or where configuration conflicts exist, it is necessary to rearrange slot assignments accordingly.

††Slot B is normally unwired and not used. It is reserved for future system expansion. The primary future assignment is to buffered communication line adapter expansion.

2. Reload the test diagnostic and change the equipment code parameters of the diagnostic from the applicable procedure listed below:

Subsystem	Diagnostic	Procedure
Dual-channel communication line adapter	CLA1A/2A	29
Card reader/ line printer controller	CRECO	28
Card reader	CR104	29
Line printer	LP408	29
Module drive	SMDDA	28
	SMDC4	28
	SMD01	28
Eight-channel communication line adapter	CLAxx	29
Cassette	CASEC	28
	CASET	29
Cartridge disk drive	CDD1	28
	CDD2	29
Magnetic tape drive	LCTT1	28
	LCTT2	29
	LCTTA	29
	LCTTB	29
Flexible disk drive	FDSxx	29

3. Change the interrupt parameters of the diagnostic from the applicable procedure listed below:

Subsystem	Diagnostic	Procedure
Dual-channel communication line adapter	CLA1A/2A	31
Card reader	CR104	31
	CRECO	
Line printer	LP408	31
	CRECO	
Module drive	SMDDA	30
	SMDCU	30
	SMD01	30

TABLE 6-23. STANDARD INTERRUPT WIRING

Backplane Pin Assignment for Macro Interrupt††			Backplane Pin Assignment for Micro Interrupt††	
Interrupt Number	Term Name	SMI Pin Assignment	Term Name	SMI Pin Assignment
0	RPINT16/	L-69†	Not used	L227†
1	RPINT17/	L-269†	RDINT01/	L-27†
2	RPINT18/	L-270	RDINT02/	L-32
3	RPINT19/	L-70	RDINT03/	L-232
4	RPINT20/	L-72	RDINT04/	L-28
5	RPINT21/	L-272†	RDINT05/	L-31
6	RPINT22/	L-271	RDINT06/	L-231
7	RPINT23/	L-71	RDINT07/	L-228
8	RPINT24/	L-73†	RDINT08/	L-30†
9	RPINT25/	L-274	RDINT09/	L-230
10	RPINT26/	L-74	RDINT10/	L-229
11	RPINT27/	L-273	RDINT11/	L-29
12	RPINT28/	L-277	RDINT12/	L-33†
13	RPINT29/	L-276	RDINT13/	L-220†
14	RPINT30/	L-77	RDINT14/	L-233†
15	RPINT31/	L-275	RDINT15/	L-234†

† These pin assignments cannot be used for interrupts on the MOS processor when it is used in 1700 emulation mode. They are used for internal processor functions.

†† Refer to table 6-21 for control interface pin assignments.

Subsystem	Diagnostic	Procedure
Eight-channel communication line adapter	CLAxx	31
Cassette	CASEC	30
	CASET	31
Cartridge disk drive	CDD1	30
	CDD2	31
Magnetic tape drive	LCTT1	30
	LCTT2	31
	LCTTA	31
	LCTTB	31
Flexible disk drive	FDSxx	31

4. Restore the processor cover plate and cabinet panels to their original positions.
5. Return to the DDLT and resume testing.

PROJECT: _____ PROCESSOR TYPE: _____ SITE NUMBER: _____

1. This form provides specific equipment and interrupt number assignment information for the above system.
2. The backplane interrupt wiring for the above equipment is shown in the Backplane Interrupt Pin Assignment column.
3. Equipment numbers as shown have been selected on respective peripheral controllers/interfaces.
4. Keep this form updated. Log all equipment and/or interrupt number changes that occur to the above system processor.

Product Number	Equipment Number	Description	Slot Assignment	Slot Type	Equipment Number	Interrupt Number	Interrupt Type	Backplane Interrupt Pin Assignment	
								Card Slot Origin	Destination
		CR	J	A/Q			MACRO		
							MICRO		
		LP					MACRO		
							MICRO		
		CLA					MACRO		
							MICRO		
			H	A/Q-DMA			MACRO		
							MICRO		
			G	A/Q-DMA			MACRO		
							MICRO		
			F	A/Q			MACRO		
							MICRO		
			E	A/Q			MACRO		
							MICRO		
			D	A/Q-DMA			MACRO		
							MICRO		
			C	A/Q			MACRO		
							MICRO		
			B	OPEN			MACRO		
							MICRO		
			A	A/Q-DMA			MACRO		
							MICRO		
			AA	A/Q			MACRO		
							MICRO		
							MACRO		
							MICRO		
			AB	SET/ SAM			MACRO		
							MICRO		

†SLOT B IS NORMALLY UNWIRED AND NOT USED: IT IS RESERVED FOR FUTURE SYSTEM EXPANSION.

Figure 6-11. System Equipment/Interrupt Number Assignments

PROJECT: SAMPLE SYSTEM PROCESSOR TYPE: AA132-A SITE NUMBER: XX01

1. This form provides specific equipment and interrupt number assignment information for the above system.
2. The backplane interrupt wiring for the above equipment is shown in the Backplane Interrupt Pin Assignment column.
3. Equipment numbers as shown have been selected on respective peripheral controllers/interfaces.
4. Keep this form updated. Log all equipment and/or interrupt number changes that occur to the above system processor.

Product Number	Equipment Number	Description	Slot Assignment	Slot Type	Equipment Number	Interrupt Number	Interrupt Type	Backplane Interrupt Pin Assignment	
								Card Slot Origin	Destination
1828-1	FH301-A	CR/LP Controller CR	J	A/Q	11	11	MACRO	J49	L273
							MICRO	J50	L29
		LP			4	4	MACRO	J249	L72
							MICRO	J250	L28
		Not used ~~CLA~~			—	—	MACRO	—	—
							MICRO	—	—
1833-4	FA111-A	CDD Controller	H	A/Q-DMA	14	14	MACRO	H249	L77
							MICRO	not used	not used
1860-5	FA464	MTTC (dual ~~mode~~)	G	A/Q-DMA	12	12	MACRO	G249	L277
							MICRO	not used	not used
			F	A/Q			MACRO		
							MICRO		
	FA730	FDD Controller	E	A/Q	7	7	MACRO	E249	L71
							MICRO	not used	not used
			D	A/Q-DMA			MACRO		
							MICRO		
1843-1	FJ441-A	Dual-channel CLA	~~AA~~ B	A/Q	2	2	MACRO	AA249	L270
							MICRO	AA250	L32
			B	OPEN			MACRO		
							MICRO		
			A	A/Q-DMA			MACRO		
							MICRO		
1828-1	FH301-A	CR/LP Controller CR	~~C~~ A	A/Q	6	6	MACRO	C49	L271
							MICRO	C50	L231
		LP			3	3	MACRO	C249	L70
							MICRO	C250	L232
			AB	SET/ SAM			MACRO		
							MICRO		

Figure 6-12. Sample Equipment/Interrupt Number Assignments

28 EQUIPMENT CODE DISPLAY/ CHANGE, LEVEL I

To display or change equipment codes needed by the diagnostic software, perform the following:

1. Press the CARRIAGE RETURN key to display the parameter control word.

2. Identify the equipment desired from figure 6-11. This equipment number corresponds to an equipment code as shown below:

Equipment Number	Equipment Code	Parameter Input
0	0	000x†
1	1	008x
2	2	010x
3	3	018x
4	4	020x
5	5	028x
6	6	030x
7	7	038x
8	8	040x
9	9	048x
10	A	050x
11	B	058x
12	C	060x
13	D	068x
14	E	070x
15	F	078x

3. To the right of the desired equipment code, identify the parameter input value required.

4. If a change is desired, insert this parameter value in the blanks below (step 5); otherwise, return to normal DDLT testing sequence.

5. Enter the following at the keyboard††:

   a. Type in 7, _ _ _ _
      → Parameter input to be inserted (see table in step 2)

   b. Press CARRIAGE RETURN.

   c. Return to procedure 27 and modify interrupt parameters as required.

29 EQUIPMENT CODE DISPLAY/ CHANGE, LEVEL II

To display or change equipment codes needed by the diagnostic software, perform the following:

1. Enter the following at the keyboard:

   a. Press CONTROL and BEL simultaneously.

   b. Type in:
      ODS, DPAR, _ _ _ _ _
      → Five-digit test mnemonic (see test executing message at display)

   c. Press CARRIAGE RETURN.

†x = 1 for CASEC, LIAT1, and LIAT2.
x = 0 for all other tests.

††For the CRECO test, enter the following at the keyboard:

a. Type in 7, _ _ _ _
   → Parameter input from table in step 1 that corresponds to card reader equipment code

b. Press CARRIAGE RETURN.

c. Type in A, _ _ _ _
   → Parameter input from table in step 1 that corresponds to line printer equipment code

d. Press CARRIAGE RETURN.

e. Return to procedure 27 and modify interrupt parameters as required.

2. Identify the equipment number for the subsystem to be tested from figure 6-11. This equipment number corresponds to an equipment code as shown below:

Equipment Number	Equipment Code	Parameter Input
0	0	000x†
1	1	008x
2	2	010x
3	3	018x
4	4	020x
5	5	028x
6	6	030x
7	7	038x
8	8	040x
9	9	048x
10	A	050x
11	B	058x
12	C	060x
13	D	068x
14	E	070x
15	F	078x

3. To the right of the desired equipment code, identify the corresponding parameter input value.

4. If a change is desired, insert this parameter input value in the blanks below (step 5); otherwise, return to normal DDLT testing sequence.

5. Enter the following at the keyboard and return to normal DDLT execution:

   a. Press CONTROL and BEL simultaneously.

   b. Type in:
   ODS, CPAR, _ _ _ _ _, 7, _ _ _ _

   - _ _ _ _ _ → Five-digit test mnemonic (see test executing message at display)
   - _ _ _ _ → Parameter input from table in step 2

   c. Press CARRIAGE RETURN.

   d. Return to procedure 27 and modify interrupt parameters as required.

30 MICRO AND MACRO INTERRUPT ASSIGNMENT DISPLAY/CHANGE, LEVEL I

To display or change the micro and/or macro interrupt assignments, (figure 6-11), perform the following:

1. Press the CARRIAGE RETURN key to display the parameter control word.

2. Observe parameter word 8. Caution must be used due to the fact that micro and macro interrupts are assigned in the same word. If only one word is to be changed, then the unchanged assignment must be re-entered. The word is broken down into four hexadecimal fields as follows:

   Word 8 0 0 _ _
   - _ _ → Macro interrupt
   - _ _ → Micro interrupt
   - 0 → Unused
   - 0 → Unused

3. If a change is desired, enter the following at the keyboard:† †

   a. Type in 8,00 _ _
   - _ _ → Macro interrupt assignment desired† † †
   - _ _ → Micro interrupt assignment desired† † †

   b. Press CARRIAGE RETURN.

4. Return to the normal DDLT testing sequence.

---

† x = 1 for CR104, LP408, CRUT1, CRUT2, CASET, LCTT2, and CDD2.
x = 0 for all other tests.

†† For the CRECO test, enter the following at the keyboard:

a. Type in 8,00 _ _
- _ _ → Card reader macro interrupt number.
- _ _ → Card reader micro interrupt number.

b. Press CARRIAGE RETURN.

c. Type In B,00 _ _
- _ _ → Line printer macro interrupt number.
- _ _ → Line printer micro interrupt number.

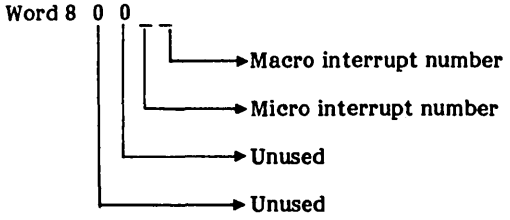
d. Press CARRIAGE RETURN.

††† Each interrupt is a single hexadecimal number.

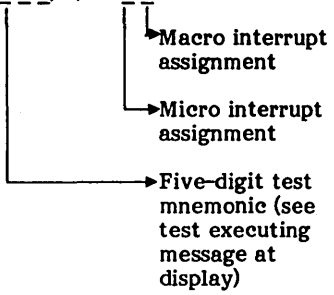
31 MICRO AND MACRO INTERRUPT ASSIGNMENT DISPLAY/CHANGE, LEVEL II

To display or change the micro and/or macro interrupt assignments (table 6-24), perform the following:

1. Enter the following at the keyboard:
   a. Press CONTROL and BEL simultaneously.
   b. Type in ODS,DPAR, _ _ _ _ _
      → Five-digit test mnemonic (see test executing message at display)
   c. Press CARRIAGE RETURN.
2. Observe parameter word 8. Caution must be used due to the fact that micro interrupts are assigned in the same word. If only one word is to be changed, then the unchanged assignment must be re-entered. The word is broken down as follows:



3. If a change is desired, enter the following at the keyboard:
   a. Press CONTROL and BEL simultaneously.
   b. Type in:
      ODS, CPAR, _ _ _ _ _, 8, 00 _ _



   c. Press CARRIAGE RETURN.
4. Return to the normal DDLT testing sequence.

32 MEMORY PARITY ERROR CLEARING

To clear a memory parity error, perform the following:

1. Master clear the system by pressing the MASTER CLEAR button on the control panel.
2. Press the ESC key on the console display keyboard.
3. Enter the following on the keyboard:

   K71602800:

4. Enter the following on the keyboard:

   K0000:

5. Enter the following on the keyboard:

   L6A03: 0D01: 18FD:

6. Press the MASTER CLEAR button on the control panel.
7. Press the ESC key on the keyboard.
8. Enter the following on the keyboard:

   K71602800:

9. Enter the following on the keyboard:

   K0000:

10. Enter the following on the keyboard to start the program:

    I:

11. After approximately three seconds, press MASTER CLEAR on the control panel.
12. Restart with table 6-1.

33 MICRO MEMORY TEST (MIMEM) RUN PARAMETERS

NOTES

1. Read the entire procedure before entering parameters into the computer as required by the DDLTs.
2. Some systems have only a single processor and some have dual processors. In a dual-processor system micro-memory tests are performed on both CPU 1 and CPU 2. The local processor is the one in which the diagnostic resides and can be either CPU 1 or CPU 2. When entering the test parameters into the computer as required by the DDLTs, be sure that the parameter is from the table for the CPU being tested.
3. The parameter changes that follow are valid only if the micro memories are switch-selected per table 4-5.

1. Remove the side panel from the cabinet of the processor being tested.

2. Examine the FCO tags for slots T and S on the front cover of the processor to determine what micro-memory features are installed. The following conditions may be observed:

   a. Slots T and S may both be empty. If slots T and S are empty, this processor does not contain micro-memory, and the MIMEM test cannot be run.

   b. Slots T and S may have only 1 slot filled. In the dual-processor equipment CPU 2 micro memory is always installed in slot T only.

      Determine from the FCO tag which of the following PWAs are installed in slot T or S. Place a check mark in the appropriate row below for the processor being tested.

      CPU 1 Test Parameters:

Slot S or T Equipment No.	Description	Parameter D	Parameter 11	Check if Applicable
BA209	512-Instruction Micro Memory	4	4	
BA210	1048-Instruction Micro Memory	7	7	

      CPU 2 Test Parameters:

Slot T (Only) Equipment No.	Description	Parameter D	Parameter 11	Check if Applicable
BA209	512-Instruction Micro Memory	4	4	
BA210	2048-Instruction Micro Memory	7	7	

   c. Slots T and S may both be filled (processor 1 only). Examine the FCO tags for slots T and S and determine which of the following boards are installed. Place a check in the appropriate row below for the processor being tested.

      CPU 1 Test Parameters:

Slot T Equipment No.	Slot S Equipment No.	Parameter D	Parameter 11	Check if Applicable
BA209	BA209	5	5	
BA210	BA210	B	B	
BA209	BA210	8	8	
BA210	BA209	8	8	

3. Using parameters D and 11 derived in the appropriate section above, enter these test parameters as called for in the DDLTs:

   D,——— (parameter D from appropriate table above)

   11,——— (parameter 11 from appropriate table above)

34 CASSETTE/DISKETTE RUN PARAMETERS (NONSTANDARD CONFIGURATIONS)

Standard CYBER 18 systems support either diskettes or cassettes, but not both. In systems that have both diskettes and cassettes, the standard ODS load device is the diskette. If the CASEC or CASET tests are being run with the diskette as the load device, or if the FDSKA test is being run with the cassette as the load device, run parameters must be modified as shown below.

CASEC Run With Diskette as Load Device

1. Remove the side panel from the cabinet of the processor being tested.
2. Examine the FCO tags for the A/Q slots and determine the location of the cassette controller.
3. Remove the cassette controller and determine the equipment code by comparing the equipment code switch setting with the equipment code select settings in the tape cassette subsystem manual.
4. Type

   8,t,u

   where t corresponds to the micro interrupt line and u corresponds to the macro interrupt line. Press CARRIAGE RETURN.
5. Type

   7, vvvv

   where vvvv is the parameter in table 6-24 corresponding to the equipment code. Press CARRIAGE RETURN.
6. Return to the tape cassette subsystem and continue the normal DDLT testing sequence.

CASET Run With Diskette as Load Device

1. Remove the side panel from the cabinet of the processor being tested.
2. Examine the FCO tags for the A/Q slots and determine the location of the cassette controller.
3. Remove the cassette controller and determine the equipment code by comparing the equipment code switch setting with the equipment code select settings in the tape cassette subsystem manual.
4. Press CONTROL and BEL simultaneously. Type

   ODS,CPAR,CASET,8,t,u

   where t corresponds to the micro interrupt line and u corresponds to the macro interrupt line. Press CARRIAGE RETURN.
5. Press CONTROL and BEL simultaneously. Type

   ODS,CPAR,CASET,7, vvvv

   where vvvv is the parameter in table 6-24 corresponding to the equipment code. Press CARRIAGE RETURN.

TABLE 6-24. CASSETTE AND DISKETTE RUN PARAMETERS

Equipment Code (In Hex.)	Parameter vvvv
0	000x†
1	008x
2	010x
3	018x
4	020x
5	028x
6	030x
7	038x
8	040x
9	048x
A	050x
B	058x
C	060x
D	068x
E	070x
F	078x

†x = 1 for CASEC, CASET
x = 0 for FDSKA

6. Return to the tape cassette subsystem and continue the normal DDLT testing sequence.

FDSKA Run With Cassette as Load Device

1. Remove the side panel from the cabinet of the processor being tested.
2. Examine the FCO tags for the A/Q-DMA slots and determine the location of the flexible disk drive controller.
3. Remove the flexible disk drive controller and determine the equipment code by comparing the equipment code switch setting with the adapter switch setting described in the flexible disk drive subsystem manual.
4. Press CONTROL and BEL simultaneously. Type

   ODS,CPAR,FDSKA,8,t

   where t corresponds to the equipment code in hexadecimal. This parameter changes the macro interrupt assignment. Press CARRIAGE RETURN.
5. Press CONTROL and BEL simultaneously. Type

   ODS,CPAR,CDSKA,7, vvvv

   where vvvv is the parameter in table 6-24 corresponding to the equipment code. Press CARRIAGE RETURN.
6. Return to the flexible disk drive subsystem and continue the normal DDLT testing sequence.

35 DETERMINING DISKETTE CONTENTS

To determine the contents of a diskette, perform the following:

1. Load the Level II Monitor test according to table 6-9.
2. After ODS x.x is displayed (x.x is the release level), enter the following at the keybaord:

   Press CONTROL and BEL keys simultaneously.

   Type ODS,LIST.

   Press CARRIAGE RETURN.
3. The response is a list of all tests contained on that diskette. After the Level II Monitor test is loaded, the contents of any other diskette (including level I diskettes) can be determined by loading the diskette in question and performing the actions in step 2.

36 BREAKPOINT PANEL REPLACEMENT

To replace the breakpoint panel (figure 6-10), perform the following:

1. Turn off power to the processor (procedure 4) and open the right side panel of the cabinet for access to processor 1 or the left side for access to processor 2.
2. Remove the interface cable from the breakpoint panel at connector J1 (procedure 38).
3. Remove the mounting screws at the bottom of the panel. See figure 6-13.
4. Replace the breakpoint panel with the new one by reversing the above steps.

37 BREAKPOINT CONTROLLER REPLACEMENT

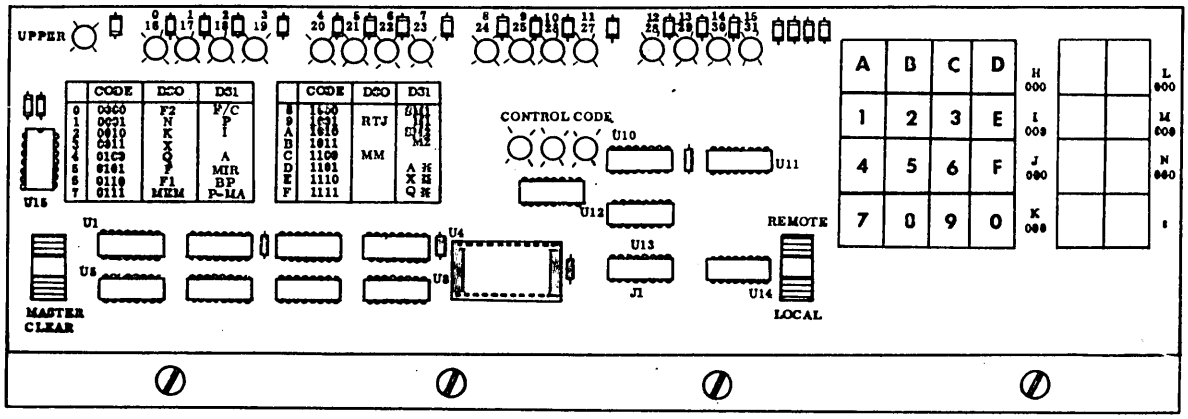
To replace the breakpoint controller, perform the following:

1. Open the right side panel of processor cabinet for access to processor 1 or the left side panel for access to processor 2.
2. Remove the processor cover plate by rotating the two captive fasteners.
3. Disconnect the interface cable from the controller (procedure 38).
4. Use the extractor tool attached to the cover plate and remove the controller. (Refer to figure 6-10 for the controller location.)
5. Position the new controller in front of the processor chassis so that the components are facing left. Reconnect the interface cable.
6. Insert the controller in its assigned position in the logic chassis and seat the controller by applying firm pressure at the top and bottom of the controller. The controller is properly installed only when fully seated.
7. Replace the extractor tool and the cover plate and close the side panel.

38 INTERFACE CABLE INSTALLATION

To install the interface cable (figure 6-14), perform the following:

1. Open the processor right side panel of the cabinet for access to processor 1 and the left side panel for access to processor 2.
2. Remove the processor cover plate by releasing the two captive fasteners.
3. Use the extractor tool attached to the cover plate and pull the controller out far enough to gain access to the interface cable connector. (Refer to figure 6-10 for the controller location.)
4. Remove the interface cable from the controller.
5. Remove the interface cable from the breakpoint panel at connector J1 (figure 6-14).
6. Replace the interface cable by reversing the above procedure.



1246

Figure 6-13. Breakpoint Panel Mounting

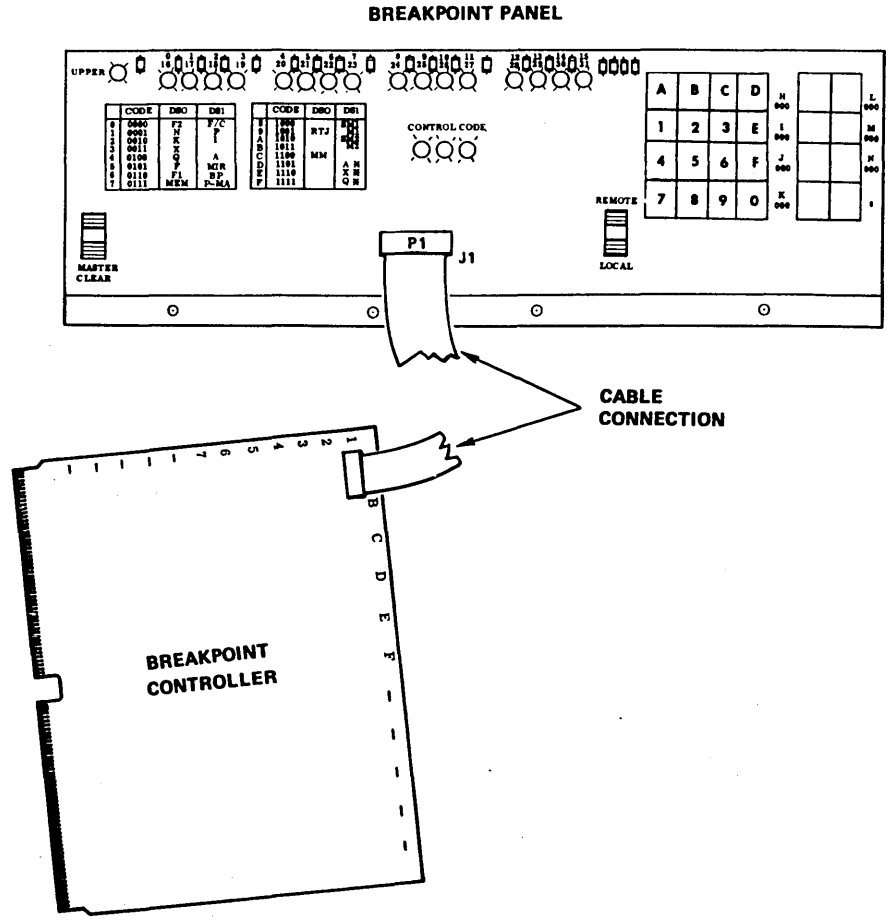


Figure 6-14. Interface Cable Connections

PARTS DATA 7

Table 7-1 lists the replaceable assemblies and their part numbers for the single and dual processors.

Maintenance of the breakpoint panel does not require any special tools or diagnostics. Tools and aids necessary to execute the DDLTs are identified in the procedures and tables associated with the breakpoint panel.

Table 7-2 is a list of replaceable assemblies and their part numbers for the breakpoint panel.

TABLE 7-1. PARTS DATA FOR PROCESSOR, CABINET, AND CONTROL PANEL

Assembly	Equipment No.	Spare Part	Part No.
Processor	AA132-A/B/C/D	Printed wiring assembly, I/O-TTY	96752182
		Printed wiring assembly, SMI	88989100
		Printed wiring assembly, ALU	88910201
		Printed wiring assembly, control 2	88909400
		Printed wiring assembly, control 1	96751017 or 96752114
		Printed wiring assembly, transform	96720404
		Printed wiring assembly, memory interface (data)	96890065
		Printed wiring assembly, memory interface (address)	96890630 or 96890551†
		Printed wiring assembly, FDD controller	96870860
		Cooling fans	94689900
Cabinet		Power supply (L.H. Research)	96754213 or 88984800
		Printed wiring assembly, control panel	96743737
		Switch, chromeric	96744793
		Sensor, temperature (130°F, 54.4°C)	51808108
		Sensor, temperature (140°F, 60°C)	51808116
		Filter, processor intake	00815483
		Switch, ac rocker	96744929
		Cooling fans	94689900
		Bezel, control panel - Front	96744883
		Back	96744882
		Power supply 24 V dc (FDD)	96753485

†Preferred part

TABLE 7-1. PARTS DATA FOR PROCESSOR, CABINET, AND CONTROL PANEL (Contd)

Assembly	Equipment No.	Spare Part	Part No.
Power Distribution		Printed wiring assembly	96754522
		Filter, ac line	96744778
		Circuit breaker (main power)	39283421
		Ac switch, triac	96756846
		Resistor (2K, 50W)	96753399
Power Supply	GD122-B	Power supply ± 5 V dc	88782623
		Power supply ± 12 V dc	88782634
		Regulator +12 V dc, -9 V dc, -5 V dc	96736300
		Fuse, 6.25 A	65267704
Processor	AA133-A/B or AA153-A	Same as AA132-A/B/C/D	
		Tape cassette controller (PWA)	96754569
		or	
		Flexible disk drive controller (PWA)	96870860
		Communication:	
		Printed wiring assembly, SMI	88909100
		Printed wiring assembly, ALU	88910201
		Printed wiring assembly, control 2	88909400
		Printed wiring assembly, control 1	96751017 or 96752114
		Printed wiring assembly, transform	96720404
		Printed wiring assembly, memory interface (data)	96890065
		Printed wiring assembly, memory interface (address)	96890630 or 96890551†
		Tape cassette controller PWA	96754569
		or	
		Flexible disk drive controller (PWA)	96870860
		MLIA (input loop)	74872399
		MLIA (output loop)	74872408
		MLIA (processor interface)	74872417
		Cooling fans	94689900
Cabinet		Same as for AA132-A/B/C/D (except for FDD power supply (24 V dc))	
		Dual-processor multiplexer (PWA)	98743744
Power Distribution		Same as for AA132-A/B/C/D	

† Preferred part

TABLE 7-1. PARTS DATA FOR PROCESSOR, CABINET, AND CONTROL PANEL (Contd)

Assembly	Equipment No.	Spare Part	Part No.
Options	AT275-B	16K MOS memory (PWA)	96743702
	AT241-B	32K MOS memory (PWA)	96743703
	BA209-A	512-instruction micro memory (PWA)	88908800
	BA210-B	2048-instruction micro memory (PWA)	96742600
	DT223-B	Error correction code MOS array	96738801
Peripheral controller	FA107-A	Magnetic tape controller	96753838
	GB138-A	SMD disk adapter	96752140
	GB145-A	Module drive adapter (PWA)	96890063
	GB145-B	Module drive adapter (PWA)	96890063
	GB145-D	Module drive adapter (PWA)	96890090
		Paddle board (PWA)	96870430
	FH301-A	Card reader/line printer controller	88909503
Power	GD122-B	Same as for AA132-A/B/C/D	

TABLE 7-2. PARTS DATA FOR BREAKPOINT PANEL

Assembly	Equipment No.	Spare Part	Part No.
Panel	DT120-A	-	96744573
		Cable, interface	88879721
		Switch	88889100/01
		Indicator	88887100
Controller	FC402-A	Breakpoint controller (PWA)	96744571

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COMMENT SHEET

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